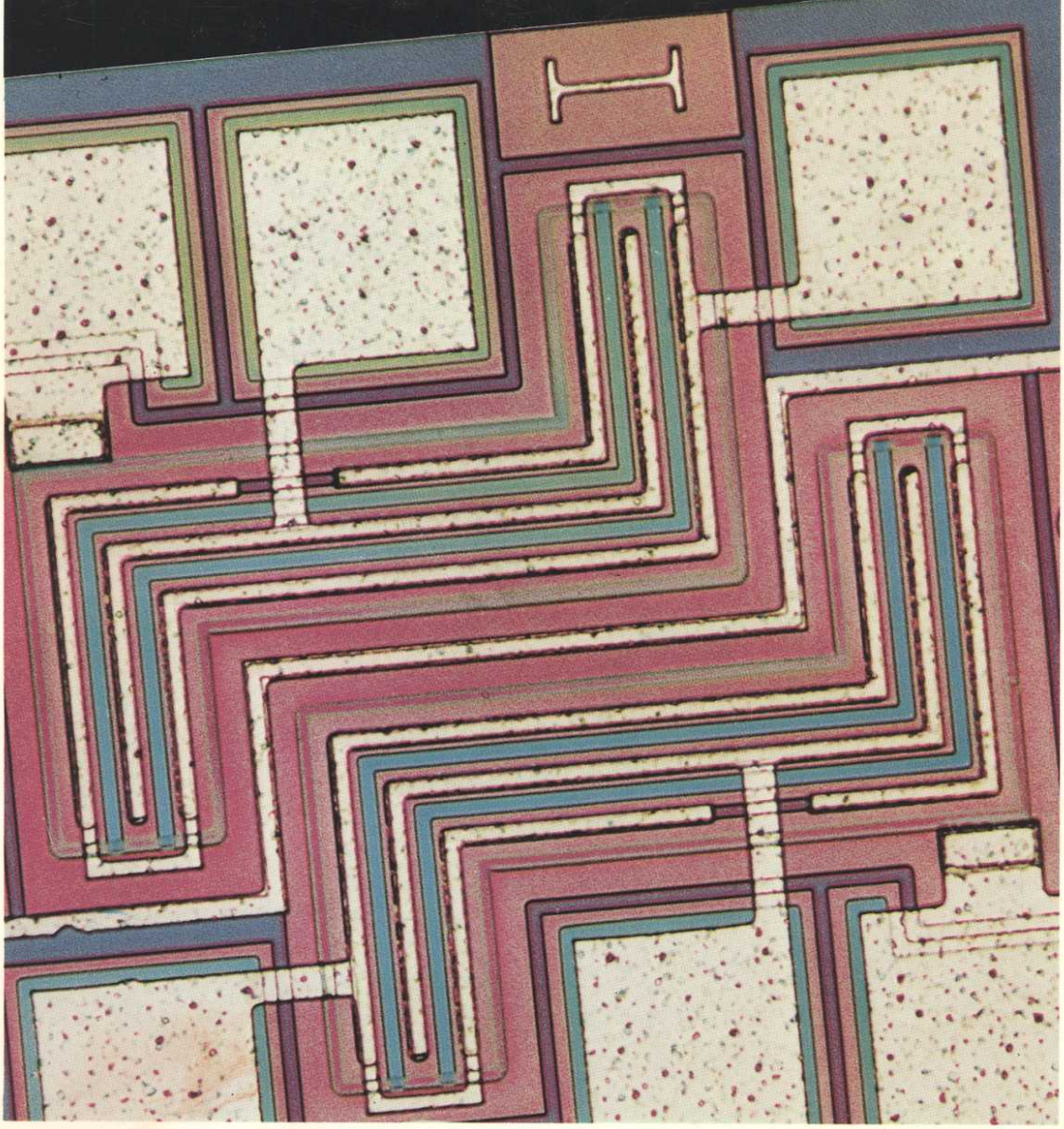
Mullard

TECHNICAL INFORMATION

86

Applications of field effect transistors



Applications of field effect transistors

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Mullard manufacture and market electronic components under the **Mullard, Philips** and **Signetics** brands

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TABLE 1

Mullard n-channel FETs

Type	No.	Outline	Application
Junction FET	BF245A to C	TO-92	d.c. to h.f. amplification
	BF246A to C	TO-92	v.h.f. to u.h.f. amplification, mixing, and switching
	BF256A to C	TO-92	v.h.f. to u.h.f. amplification and mixing
	BF410A to D	TO-92	v.h.f. amplification and mixing (from a low-voltage source)
	BFQ10 to BFQ16	TO-71	monolithic duals for differential amplification
	BFR30, BFR31	SOT-23	d.c. to h.f. amplification in hybrid circuits
	BFS21, BFS21A	2× TO-72	discrete matched-pair for differential amplification
	BFT46	SOT-23	low-level amplification in thick- and thin-film circuits
	BFW10 to BFW13	TO-72	low-noise v.h.f. amplifiers in professional equipment
	BFW61	TO-72	general-purpose amplification
	BSR56 to BSR58	SOT-23	low 'on' resistance switching for hybrid circuits
	BSV78 to BSV80	TO-18	low 'on' resistance switching
	2N3822	TO-72	high-voltage general-purpose h.f. amplification (low gate leakage and low capacitance)
	2N3823	TO-72	i.f. and r.f. amplification
	2N3966	TO-72	low-power switching, for example multiplexing
	2N4091 to 2N4093	TO-18	industrial switching
	2N4391 to 2N4393	TO-18	industrial chopping and switching
	2N4856 to 2N4861	TO-18	industrial chopping and switching
Depletion MOSFET	BF327	SOT-103	v.h.f. amplification (dual gate)
	BF981	SOT-103	low-noise v.h.f. communications equipment (dual gate)
	BFR29	TO-72	linear amplification requiring high input impedance
	BFR84	TO-72	v.h.f. amplification (dual gate)
	BFS28	TO-72	v.h.f. amplification (dual gate) with high input impedance
	BSV81	TO-72	switching and chopping
	3N211	TO-72	low-power gain-controlled r.f. and i.f., extremely low C_{rss} (dual gate)
Enhancement MOSFET	SD200 to SD203	TO-72	u.h.f. amplification (single gate)
	SD210 to SD215	TO-72	analogue and digital switching
	SD300	TO-72	v.h.f. to u.h.f. amplification and mixing (dual gate)
	SD303 to SD306	TO-72	v.h.f. to u.h.f. amplification and mixing (dual gate)
	SD6000	8-lead DIL	f.m./v.h.f. tuner-heads (double dual gate)

INTRODUCTION

Field effect transistors (FETs) are part of a wide range of active devices that confront the designer seeking to optimise a circuit. The choice of component in a particular application is governed by factors such as cost, ease of assembly, performance, and reliability, for example, which the engineer balances to produce a cost-effective design.

This publication shows how some of the FETs that are available from Mullard can be used advantageously in many applications. The information included ranges from detailed circuit designs to more general applications using the unique properties of FETs. The designer should remember always to consult the published data before deciding to include a particular device in a circuit.

A list of the FETs available from Mullard is given in Table 1, and full data can be obtained on request.

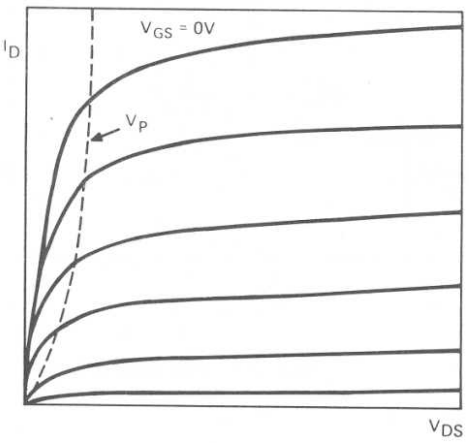


Fig.1 Typical output characteristics of FET

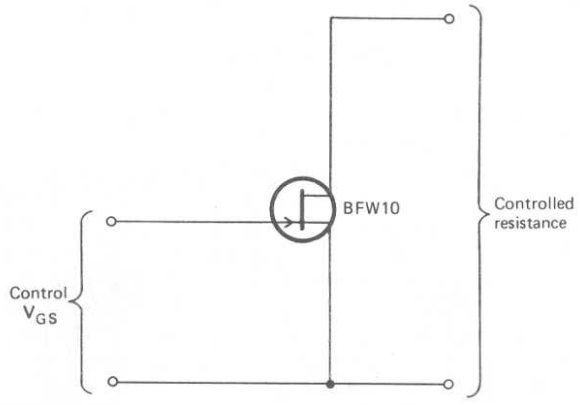
USING FETs AS VOLTAGE-CONTROLLED RESISTORS

Fig.1 shows a typical family of output characteristics for a depletion-mode FET. A closer examination of the characteristics of a typical FET, for small values of drain-source voltage V_{DS} (shown in Fig.2b), reveals that all the characteristics pass through the origin, and are approximately symmetrical and linear. Therefore the FET can readily be used as a voltage-controlled resistor, as shown in Fig.2a.

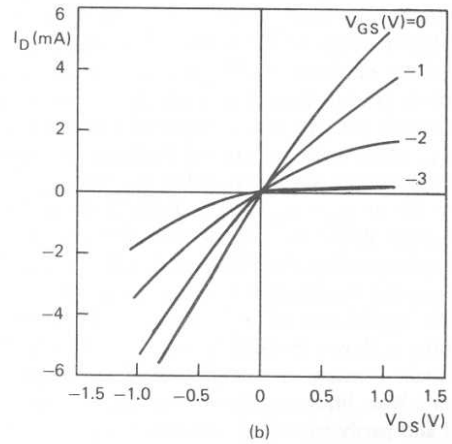
It can be shown that in the region covered by Fig.2b, the channel conductance g_{os} of a FET is given by:

$$g_{os} = \frac{I_{DSS}}{V_P^2}\{2(V_{GS} - V_P) - V_{DS}\}, \qquad (1)$$

where I_{DSS} is the drain current for zero gate-source voltage, V_P is the pinch-off voltage, V_{GS} is the gate-source voltage, and V_{DS} is the drain-source voltage. Clearly, g_{os} is approximately linearly related to V_{GS} only if V_{DS} is much less than V_P. Consequently it is



(a)



(b)

Fig.2 FET voltage-controlled resistor: (a) circuit (b) characteristics

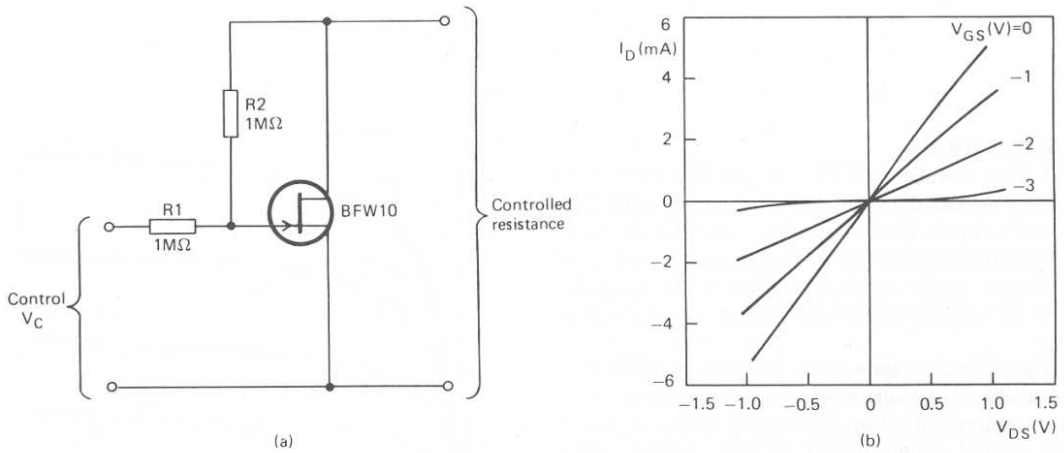


Fig.3 FET voltage-controlled resistor with feedback: (a) circuit (b) characteristics

necessary to provide feedback from the drain to the gate to improve the linearity, especially for large V_{DS} signals. A suitable circuit, shown in Fig.3a, uses two equal-value resistors R_1 and R_2 to provide the necessary feedback. The gate-source voltage V_{GS} is then given by:

$$V_{GS} = \tfrac{1}{2}(V_C + V_{DS}), \qquad (2)$$

where V_C is the control voltage.

Eq.2 can be combined with Eq.1 to give:

$$g_{os} = \frac{I_{DSS}}{V_P^2}(V_C - 2V_P). \qquad (3)$$

Clearly g_{os} is linearly related to the control voltage V_C, and Fig.3b confirms this to be the case. However, the use of feedback either reduces the resistance range for a fixed control voltage range, or requires an increased control voltage range for the same resistance range.

Measurements of the harmonic distortion generated by three different FETs used as voltage-controlled resistors are summarised in Table 2. The measurements were made with a 1 kHz sinewave of amplitude 500 mV r.m.s., either with or without feedback, and with the control voltage such that either $g_{os} = g_{os(on)}$ (that is $V_C = 0$) or $g_{os} = g_{os(on)}/10$. Table 2 shows that for minimum distortion over as wide a range of control voltage as possible, the FET used should have high values of I_{DSS} and V_P, and that feedback is essential.

An application of a FET as a voltage-controlled resistor is shown in Fig.4, in which the FET is used to maintain constant the amplitude of the output signal from a Wien bridge oscillator. The output signal is rectified and partly smoothed before it is applied to the gate of the FET which is in parallel with R_1, so controlling the gain of the amplifier. The d.c. bias and maximum gain of the amplifier is set solely by resistors R_1 and R_2, because the FET is isolated by capacitor C_1.

A FET may be used as a voltage-controlled attenuator, as Fig.5 shows. The advantages of such a circuit are first, the control applied to the gate of the FET is a d.c. voltage; and second, the lengths of the control leads are unimportant because the capacitive pick-up of stray signals associated with a.c. remote control is avoided.

Other applications of the FET as a voltage-controlled resistor include amplitude modulation, bandwidth control of tuned LC circuits, electronically-tuned RC filters, and automatic gain control. FETs can also be used with operational amplifiers to provide various circuit functions such as analogue multipliers, dividers, and reciprocal generators.

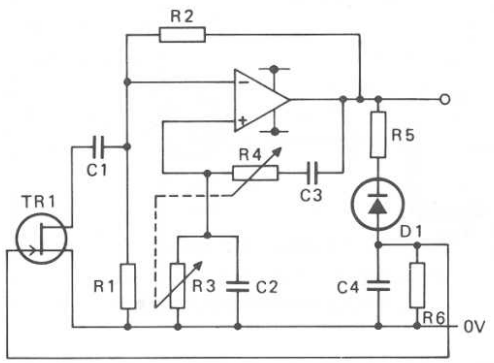


Fig.4 Oscillator incorporating FET for amplitude stabilisation

TABLE 2

Harmonic distortion measurements

		FET 1		FET 2		FET 3	
FET properties	I_{DSS}	high		medium		low	
	V_P	high		medium		low	
		Distortion (%)		Distortion (%)		Distortion (%)	
		2nd harmonic	3rd harmonic	2nd harmonic	3rd harmonic	2nd harmonic	3rd harmonic
Without feedback							
$g_{os} = g_{os(on)}$		0.1	0.2	0.2	0.2	0.9	0.8
$g_{os} = g_{os(on)}/10$		10.0	2.0	12.0	2.0	16.0	1.5
With feedback							
$g_{os} = g_{os(on)}$		0.2	0.2	0.1	0.1	0.2	0.2
$g_{os} = g_{os(on)}/10$		0.2	0.7	0.5	1.0	4.0	0.5

Signal voltage V_{DS} = 500 mV, signal frequency = 1 kHz

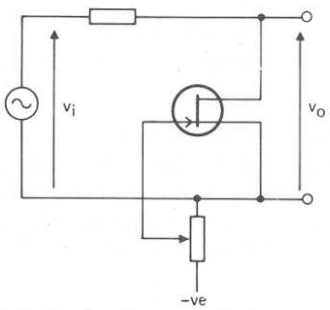


Fig.5 Simple voltage-controlled attenuator

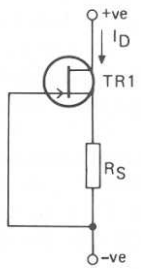


Fig.6 FET constant-current source with fixed resistor

JUNCTION FET AS A CONSTANT-CURRENT SOURCE

Examination of the typical output characteristics of a junction FET, as shown in Fig.1, reveals that the drain current is almost independent of the drain-source voltage provided that the drain-source voltage is greater than the pinch-off voltage. Thus the FET can be used as a constant-current source; a suitable circuit is shown in Fig.6.

In the circuit of Fig.6, the FET and a source resistance form a simple two-terminal constant-current circuit. However, FET characteristics show a wide spread in drain current at fixed V_{GS} and it is therefore necessary to make the source resistance adjustable, as shown in Fig.7, if a predetermined value of current is required. An alternative means of obtaining a predetermined current is either to select FETs having the correct current for use with a fixed value of resistance or, if their characteristics

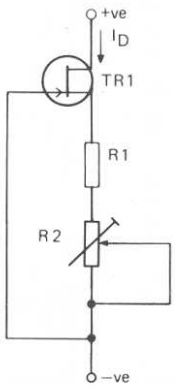


Fig.7 FET constant-current source with adjustable source resistor

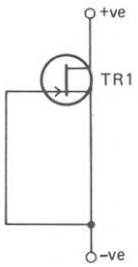


Fig.8 FET constant-current source with no source resistor

allow, to select FETs having the correct current at zero V_{GS} (that is, I_{DSS}). The latter method gives the very simple circuit shown in Fig.8. However, selecting devices will only be economic when a large number of FETs are available and the FETs not used in this application can be used elsewhere.

Constant-current drive for LEDs

To give constant brightness, a LED should be operated at constant current. If the LED is supplied from a stabilised voltage rail, the constant current can be fixed by a resistor in series with the LED. However, if the supply to the LED is unstabilised, a low-cost constant-current drive can be constructed using a FET, as described above. A practical example of a constant-current (10 mA) drive for a LED is shown in Fig.9. A suitable FET is the BF245C which has a spread of characteristics such that the source resistance must lie between 40 and 300 Ω for 10 mA constant current. The source resistor is therefore made from a fixed 39 Ω resistor and a 270 Ω variable resistor. The LED current can be set by measuring the potential difference across R_1 as R_2 is adjusted. The maximum value of the supply voltage V_S is equal to $V_{DS(max)}$ for the BF245C (30 V), plus the lowest forward voltage of the LED (1.5 V), plus the lowest potential drop across R_1 and R_2 (0.5 V), giving a total of 32 V. The minimum value of the supply voltage V_S is given by the minimum value of V_{DS} to maintain the drain current at the desired value (3.0 V), plus the largest potential drop across R_1 and R_2 (3.0 V), plus the largest forward voltage across the LED (2.5 V), giving a total of 8.5 V. With typical devices, little loss of light output occurs at supply voltages down to 5 V.

Component types and values for circuits using 10 and 20 mA LEDs are given in the Component Lists.

Polarity indicator

The circuit shown in Fig.10 is a modification of that shown in Fig.9, incorporating reverse-voltage protection by the addition of diode D_2 in anti-parallel to the LED, and resistor R_1 in series with the FET gate. The circuit can be used as a polarity indicator for voltages below 32 V, because the LED will only light when the polarity is as shown in Fig.10.

Component types and values for 10 and 20 mA versions of this circuit are given in the Component Lists.

Constant current for long-tail-pair

In the circuit of Fig.11, the FET is used to determine the combined emitter currents of a bipolar transistor long-tail-pair. A particular advantage of using a FET in this application is that it is theoretically possible to

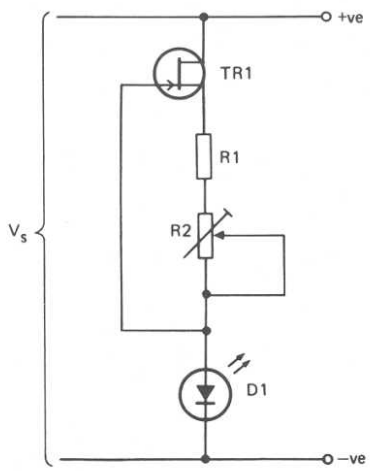


Fig.9 Constant-current drive for LED indicator

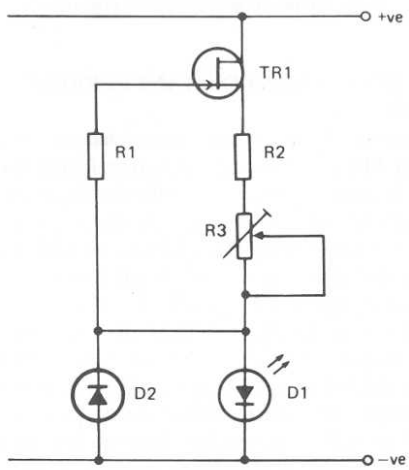


Fig.10 Polarity indicator

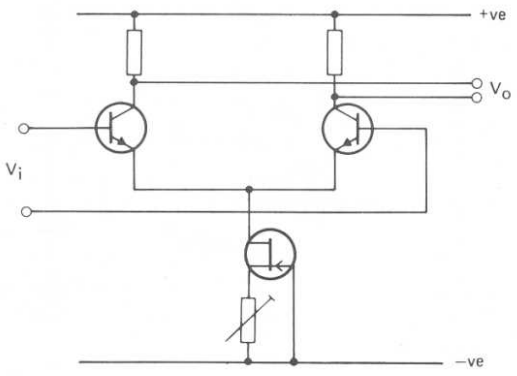


Fig.11 FET used to stabilise tail current of long-tail-pair

ensure that the tail current is independent of temperature. For each FET there exists a gate-source voltage $V_{GS(0)}$ and drain current $I_{D(0)}$ for which the temperature coefficient of drain current is zero. It can be shown theoretically that:

$$V_{GS(0)} = V_P + 0.63\ V, \qquad (4)$$

and

$$I_{D(0)} = I_{DSS}\left(\frac{0.63}{V_P}\right)^2. \qquad (5)$$

In practice, even if the drain current is set at $I_{D(0)}$, the tail current will still vary slightly with temperature, and Fig.12 shows the average spread of current drift when the drain current is set to $I_{D(0)}$ at 25°C.

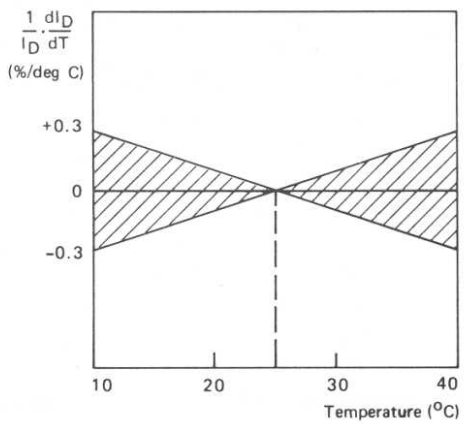


Fig.12 Typical temperature dependence of drain current

Constant-current drive for voltage reference diode

Fig.13 shows a FET constant-current source used to stabilise the current through a voltage reference diode. The circuit can be considered as an ideal constant-current source in parallel with a conductance g_o given by:

$$g_o = \frac{g_{os}}{1 + g_{fs}R_S}, \qquad (6)$$

where g_{fs} is the common-source small-signal forward transfer conductance of the FET. Therefore, supply voltage variations are reduced by a factor S given by:

$$S = \frac{1}{g_o r_z}, \qquad (7)$$

where r_z is the dynamic resistance of the voltage reference diode. Typically, S has a value of 4500.

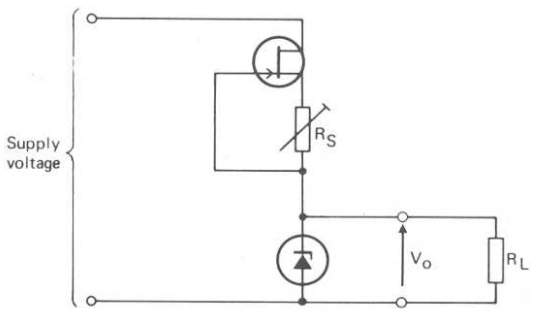


Fig.13 Stabilised current source for voltage reference diode

Linear sweep generator

The circuit of Fig.14 is a linear sweep generator using two FETs: TR_1 is a source follower and TR_2 supplies a constant current. Since the drain current of TR_1 is held constant by TR_2, the gate-source voltage remains constant and the output voltage accurately follows the gate voltage. When the switch is opened, capacitor C_1 charges,

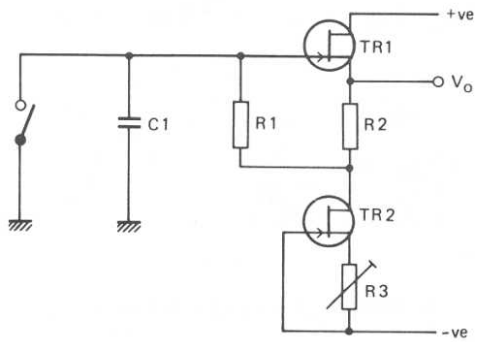


Fig.14 Linear sweep generator using FETs

the charging current being the sum of the current flowing through resistor R_1 and the gate current of the FET. The latter is very small (the gate leakage current) because the gate-source diode is reverse-biased. Thus the charging current is effectively determined by resistor R_1 only and is constant. The fall in gate voltage is therefore linear and, as the output voltage follows the gate voltage, the slope of the output waveform is also linear. The switch across C_1 may be replaced by a bipolar transistor or a FET, and so the circuit may be used to generate a sawtooth waveform. The capacitor charging time is controlled by the values of C_1 and R_1.

IMPEDANCE-MATCHING CIRCUIT FOR CAPACITOR MICROPHONE

The FET can be used advantageously to step down the high impedance of a capacitor microphone, which is inherently unsuitable for driving a bipolar transistor. If the input impedance of the bipolar transistor were high enough to give a reasonable transfer ratio, the noise factor would also be high; conversely if the input impedance were low enough to give a sufficiently low noise factor, the transfer ratio would be inadequate. The noise contribution of a FET remains extremely small, even at high source impedances, and therefore the noise contribution of an impedance-matching circuit embodying a BFW11 FET as a source follower is now considered.

Noise sources

The equivalent circuit of a capacitor microphone consists of a signal voltage source E_S in series with a capacitance C_S, as shown in Fig.15a. Typically, the sensitivity S of the microphone can be taken to be 10 mV/Pa, and its capacitance C_S to be about 33 pF. When the microphone is connected to an impedance-matching circuit, the noise contribution of the latter can be represented by a second voltage source E_{eq} in series with E_S, as shown in Fig.15b.

Fig.16 shows a representative impedance-matching circuit making use of a FET. Resistor R_p is the bias

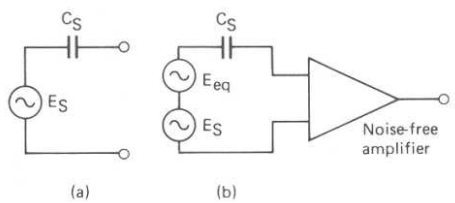


Fig.15 Equivalent circuit of capacitor microphone:
(a) microphone only
(b) including noise-voltage source due to impedance-matching network

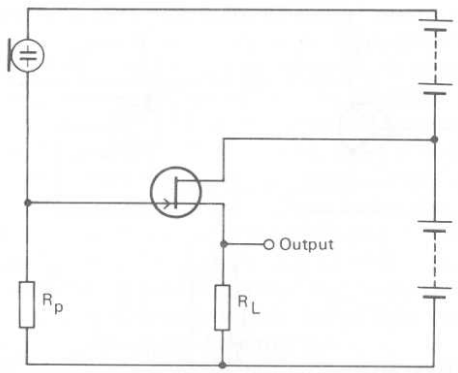


Fig.16 FET in impedance-matching network for capacitor microphone

resistor and is generally of the order of a few hundred-million ohms. The drain current of the FET is adjusted to the required value by means of a load resistance R_L of, say, 3 kΩ. However, since this resistance is shunted by $1/g_{fs}$, an impedance of less than 1 kΩ is usually presented to the following stage so that the latter can be equipped with a bipolar transistor in common-collector configuration without noticeably contributing towards the noise. The emitter resistance of this second stage can easily be matched to the cable which links the microphone to its amplifier.

A simple equivalent circuit showing the noise voltage source is given in Fig.17a. For purposes of analysis, this circuit can be expanded into the more detailed form of Fig.17b in which the several factors responsible for development of the equivalent noise voltage E_{eq} are shown separately. As shown in the figure, these are:

- E_n the equivalent noise voltage of the FET,
- I_p the noise current of resistor R_p,
- I_L the noise current of resistor R_L,
- I_n the equivalent shot noise current source due to the gate leakage current.

These noise sources are defined by the expressions:

$$\Delta|\overline{E_n}|^2 = A\Delta f/f + 4kT\Delta f/g_{fs}, \quad (8)$$

$$\Delta|\overline{I_p}|^2 = 4kT\Delta f/R_p, \quad (9)$$

$$\Delta|\overline{I_L}|^2 = 4kT\Delta f/R_L, \quad (10)$$

and

$$\Delta|\overline{I_n}|^2 = 2eI_G\Delta f, \quad (11)$$

in which the factor A varies slightly with the drain current and voltage, k is Boltzmann's constant, f is the frequency, T is the thermodynamic temperature, e is the

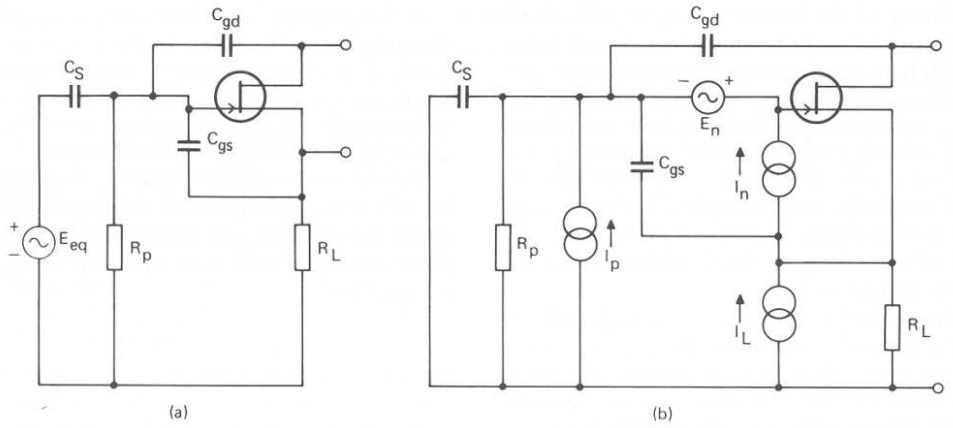


Fig.17 Equivalent circuit of network of Fig.16:
(a) without noise sources (b) with the various current and voltage noise sources

electron charge, Δf is the bandwidth, and I_G denotes the gate current. The variation of the equivalent noise is given in a simplified form by:

$$\Delta\overline{|E_{eq}|^2} = \frac{(\Delta\overline{|I_p|^2} + \Delta\overline{|I_n|^2})}{4\pi^2 f^2 C_S^2} + \left(1 + \frac{C_{is}}{C_S}\right)^2 \times \times \left(\Delta\overline{|E_n|^2} + \frac{\Delta\overline{|I_L|^2}}{g_{fs}^2}\right), \qquad (12)$$

where $C_{is} = C_{gd} + C_{gs}$, the input capacitance of the FET.

In the determination of the subjective effect of noise, it is customary to put the bandwidth Δf equal to $f/\sqrt{2}$ giving:

$$|E_{eq}|^2 = \int_{\frac{1}{2}f\sqrt{2}}^{f\sqrt{2}} \frac{\Delta\overline{|E_{eq}|^2}}{\Delta f}\,df, \qquad (13)$$

Thus, from Eqs.8, 9, 10, 11, 12 and 13, it can be shown that:

$$|E_{eq}|^2 = \frac{2 \times 10^{-2}}{fC_S^2}\left(\frac{4kT}{R_p} + 2eI_G\right) + + \left(1 + \frac{C_{is}}{C_S}\right)^2 \left(\frac{2kTf\sqrt{2}}{2g_{fs}/3 + R_L g_{fs}^2} + A \ln\frac{5}{3}\right). \qquad (14)$$

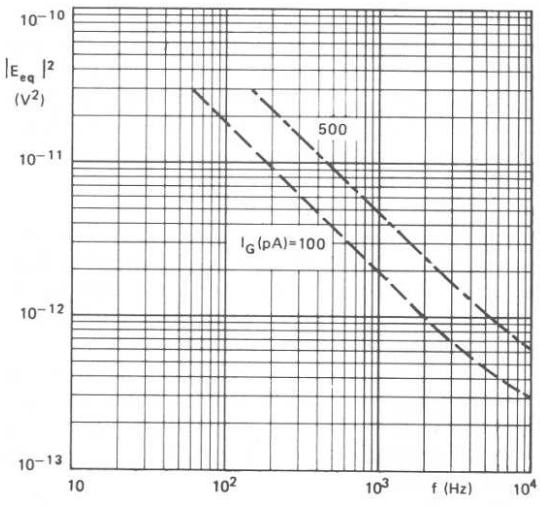


Fig.18 Equivalent noise voltage $|E_{eq}|^2$ as function of frequency for two values of gate current I_G

Given the values:

$C_S = 33$ pF $\quad R_p = 250$ MΩ $\quad g_{fs} \simeq 1$ mA/V
$C_{is} < 5$ pF $\quad R_L = 3$ kΩ $\quad A = 10^{-13}$ V²

it can be calculated from Eq.14 that with the maximum gate current of 500 pA:

$$|E_{eq}|^2 = 4.6 \times 10^{-9}/f + 7 \times 10^{-14} + 1.6 \times 10^{-17} f;$$

and with the typical gate current of 100 pA:

$$|E_{eq}|^2 = 2.0 \times 10^{-9}/f + 7 \times 10^{-14} + 1.6 \times 10^{-17} f.$$

In Fig.18 these values of $|E_{eq}|^2$ have been plotted as functions of f, and their relevance is described below.

Acoustic considerations

To relate the voltage E_{eq} to an equivalent noise, account must be taken of the sensitivities of the microphone and the human ear. As has already been stated, the sensitivity of the microphone may be taken to be 10 mV/Pa.

The sensitivity of the human ear to noise with a bandwidth Δf centred around a given frequency f (where $\Delta f = f/\sqrt{2}$) is indicated by the loudness level contours of Fig.19. Along the ordinate of the graph, sound pressure levels p_{rel} are expressed in decibels relative to a pressure $p_{0\,dB}$ of 20 μPa; along the abcissa, frequency is represented on a scale divided into octave intervals. The family of numbered curves shows how subjective judgement of noise loudness level varies with frequency, the standard of comparison on which each curve is based being noise centred on 1 kHz.

For the subjective increments of acoustic noise by which the curves are separated, the unit of measurement is the phon. Thus for noise centred on 1 kHz, a loudness level increment of 1 phon corresponds exactly to a sound pressure level increment of 1 dB. Below that frequency, 1 phon corresponds to less than 1 dB, and above it, to more than 1 dB, in proportion to the curvature and divergence of the curves.

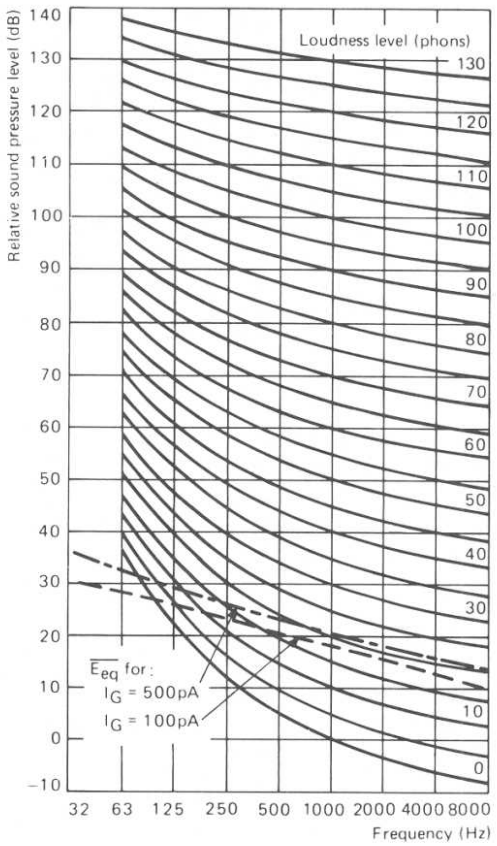


Fig.19 Equal loudness level contours showing how subjective impression of noise of bandwidth $f/\sqrt{2}$ varies with centre frequency f. Broken curves show equivalent noise from impedance-matching network for two values of gate current

In the frequency range covered by the graph, noises of equal pressure level seem to the human ear to grow louder as their centre frequency rises; moreover, as the trends and spacing of the curves indicate, the effect is more pronounced at low frequencies and loudness levels than at high frequencies and loudness levels.

To find what the noise voltage E_{eq} means in terms of acoustic noise superimposed on the output of the microphone, the ratio of E_{eq} to the sensitivity S of the microphone can be expressed as an equivalent sound pressure p_{eq} given by:

$$p_{eq} = E_{eq}/S. \qquad (15)$$

The ratio (expressed in dB) of p_{eq} to the 0 dB reference pressure then indicates the sound pressure level p_{rel} that corresponds to the noise voltage E_{eq}, and is given by:

$$p_{rel} = 20 \log (p_{eq}/p_{0\,dB}),$$
$$= 20 \log (E_{eq}/Sp_{0\,dB}). \qquad (16)$$

Evaluating this equation at several frequencies throughout the audio range gives a curve which, by superposition on the loudness level contours of Fig.19, indicates the apparent noise contribution at any frequency. The curve drawn in chain-dot line in Fig.19 shows the result when E_{eq} is evaluated on the basis of the maximum value of I_G (500 pA), and the curve in broken line when it is evaluated on the basis of the typical value (100 pA).

The two curves superimposed on the loudness level contours of Fig.19 represent sound pressure levels; what they mean in terms of apparent noise can be interpreted by reference to the contours they cross. At 4 kHz, for example, the chain-dot line indicates a sound pressure level p_{rel} of about 16 dB, and at that frequency such a level corresponds to a noise loudness level of about 21 phon. Hence, if I_G is maximum (500 pA), the noise contribution of the matching network at 4 kHz is 21 phon; similarly, if I_G is 100 pA (broken line curve), the sound pressure level at 4 kHz is about 13 dB and the noise contribution of the matching network 18 phon.

At lower frequencies, though the sound pressure level equivalent of the noise voltage rises, it does so less steeply than the loudness level contours; hence the noise contribution of the matching network diminishes. Thus, at 250 Hz the sound pressure level indicated by the broken line curve is about 23 dB, corresponding to a noise contribution of only about 13 phon.

That the two curves show the noise contribution of the network to be negligible throughout the frequency range of interest can be appreciated by reference to Table 3, in which average ambient noise levels encountered in spaces designed for various uses are shown.

From these considerations it is apparent that the BFW11 FET connected as a source-follower can easily satisfy the most stringent requirements likely to be

TABLE 3

Typical ambient noise loudness levels in various enclosed spaces

Broadcasting studio	15 phon
Concert hall and theatre (500 seats)	20 phon
Class room, music room, television studio, and sleeping room	25 phon
Conference room, cinema, hospital, church, courtroom, library, and living room	30 phon
Private office	40 phon
Restaurant	45 phon
Gymnasium	50 phon
Office (with typewriters)	50 phon
Workshop	65 phon

imposed on an impedance matching network for a capacitor microphone. The same is not true, however, if it is connected in common-source configuration. In that case the noise due to the load resistance R_L is augmented by the noise current I_{ef} of the emitter-follower to be driven, producing an increase in E_{eq} that is given by:

$$\Delta|E_{eq}|^2 \simeq |I_{ef}|^2/g_{fs}^2.$$

This may be as large as the contribution due to the thermal noise voltage E_n of the FET.

FETs IN PREAMPLIFIER FOR USE WITH SOLID-STATE RADIATION DETECTORS

Solid-state radiation detectors operate on the release by incident radiation of electron-hole pairs in the depletion layer of a reverse-biased pn junction. The electric field generated by the bias voltage drives the charge carriers out of the depletion layer, and the charge, which is proportional to the energy of the incident radiation, is fed to the input of a preamplifier. The output voltage of the preamplifier is proportional to the input charge and therefore to the energy of the incident radiation.

The resolution and stability of the electronic circuitry associated with a solid-state radiation detector play an important part in the overall performance of the energy-measuring system, and low-noise amplification is therefore essential.

Fig.20 is a block diagram of a simple spectrometer system associated with a solid-state detector. The amplified signal is fed to a pulse-height analyser which sorts incoming pulses into a series of channels, each one corresponding to a narrow energy range. A threshold amplifier may be included to reduce the number of channels required for high-energy radiation.

Fig.21 shows a high-gain preamplifier circuit using low-noise BFW11 FETs in the charge-sensitive section. Capacitive feedback ensures that a large capacitive load is presented to the detector to minimise the effects of changes in wiring capacitance and detector capacitance. The active input capacitance of the preamplifier is approximately equal to the product of feedback capacitance and loop gain, and the conversion gain (the ratio of output voltage amplitude to input charge) is approximately equal to the reciprocal of the active feedback capacitance. The decay time-constant of the charge-sensitive section is small, to avoid loss of resolution at high counting rates due to pulse pile-up.

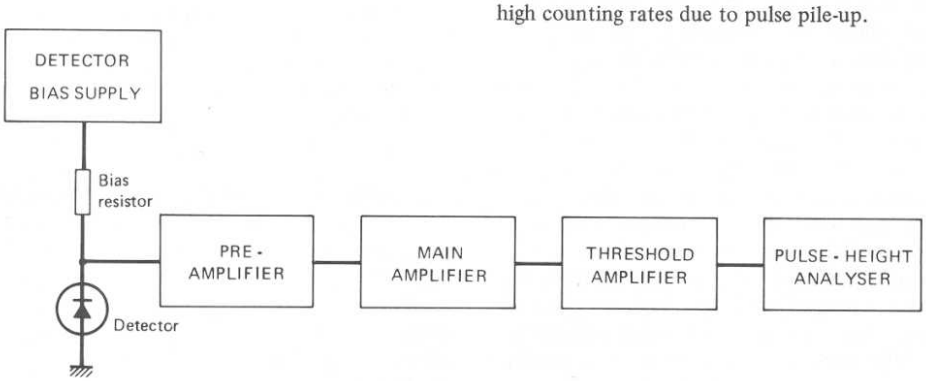


Fig.20 Block diagram of simple ionising radiation spectrometer incorporating solid-state detector

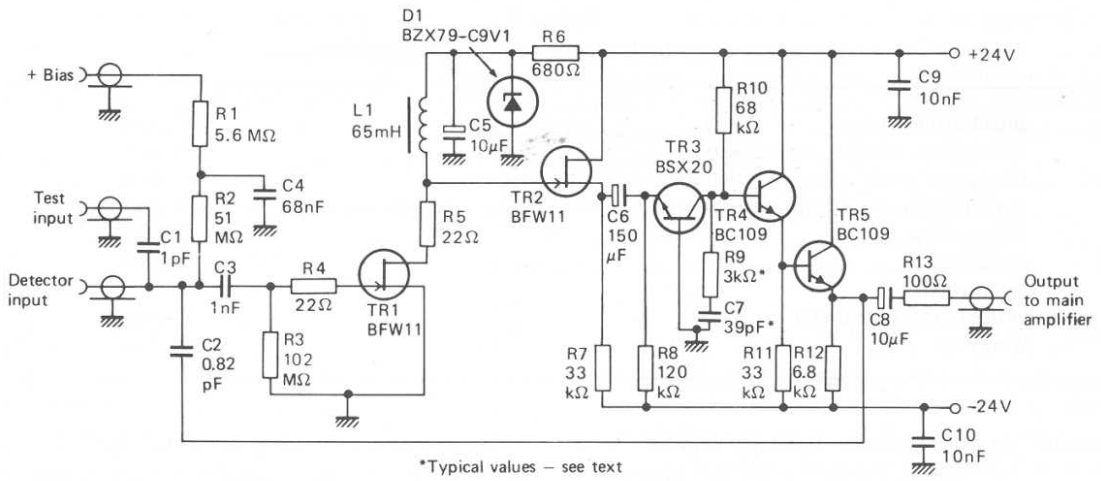


Fig.21 FETs in preamplifier for silicon surface-barrier detector

The remaining transistors form a conventional voltage amplifier, the high value of feedback ensuring high stability over extended periods of measurement. The preamplifier may be combined with a main amplifier with an input impedance of 100 Ω or higher.

The preamplifier converts the charge released in the detector into a voltage, the sensitivity being expressed either in terms of the detector output (V/C) or in terms of the energy of the incident radiation (V/keV). The output of the preamplifier is then fed to the main amplifier. Since the noise generated by the preamplifier is dependent on the time-constant of the main amplifier, bandwidth-limiting elements in the main amplifier (such as differentiating and integrating networks) are designed to minimise the noise contribution of the amplification system as a whole.

Fig.22 shows the noise contribution of the preamplifier, expressed as an equivalent noise energy in keV, as a function of detector capacitance and main amplifier time-constant. Since the magnitude of the charge released in the detector by a given radiation depends on the material of which the detector is made, the noise contribution is specified separately for silicon and germanium detectors. The minimum noise contribution of the preamplifier is indicated by the broken line.

The test input may be used to set up minimum preamplifier rise- and fall-times with minimum overshoot. With the preamplifier input loaded with a 100 pF screened capacitor, a pulse with rise- and fall-times less than 10 ns and a repetition rate of 2 MHz is applied to the test input, the pulse amplitude being adjusted to prevent amplifier overloading. The values of resistor R_9 and capacitor C_7 are adjusted to give minimum preamplifier rise- and fall-times with minimum overshoot.

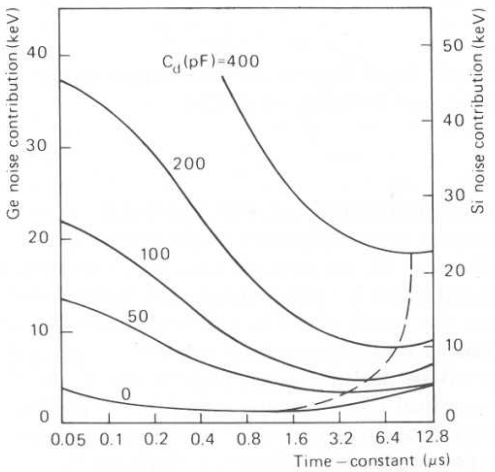


Fig.22 Noise contribution of preamplifier as function of detector capacitance and amplifier time-constant

Typical values of rise- and fall-times are 100 ns and 250 ns respectively.

PREAMPLIFIER FOR WIDEBAND OSCILLOSCOPE

The preamplifier shown in Fig.23 is a three-stage differential amplifier having outputs in antiphase with each other. Of the two inputs, one is for the signal and the other for adjusting the d.c. bias that controls the vertical shift. The FETs TR_1 and TR_2 are connected as source-followers to provide a low enough source impedance for the BFY90 transistors of the following stage to ensure that the gain of the BFY90s will remain constant at high

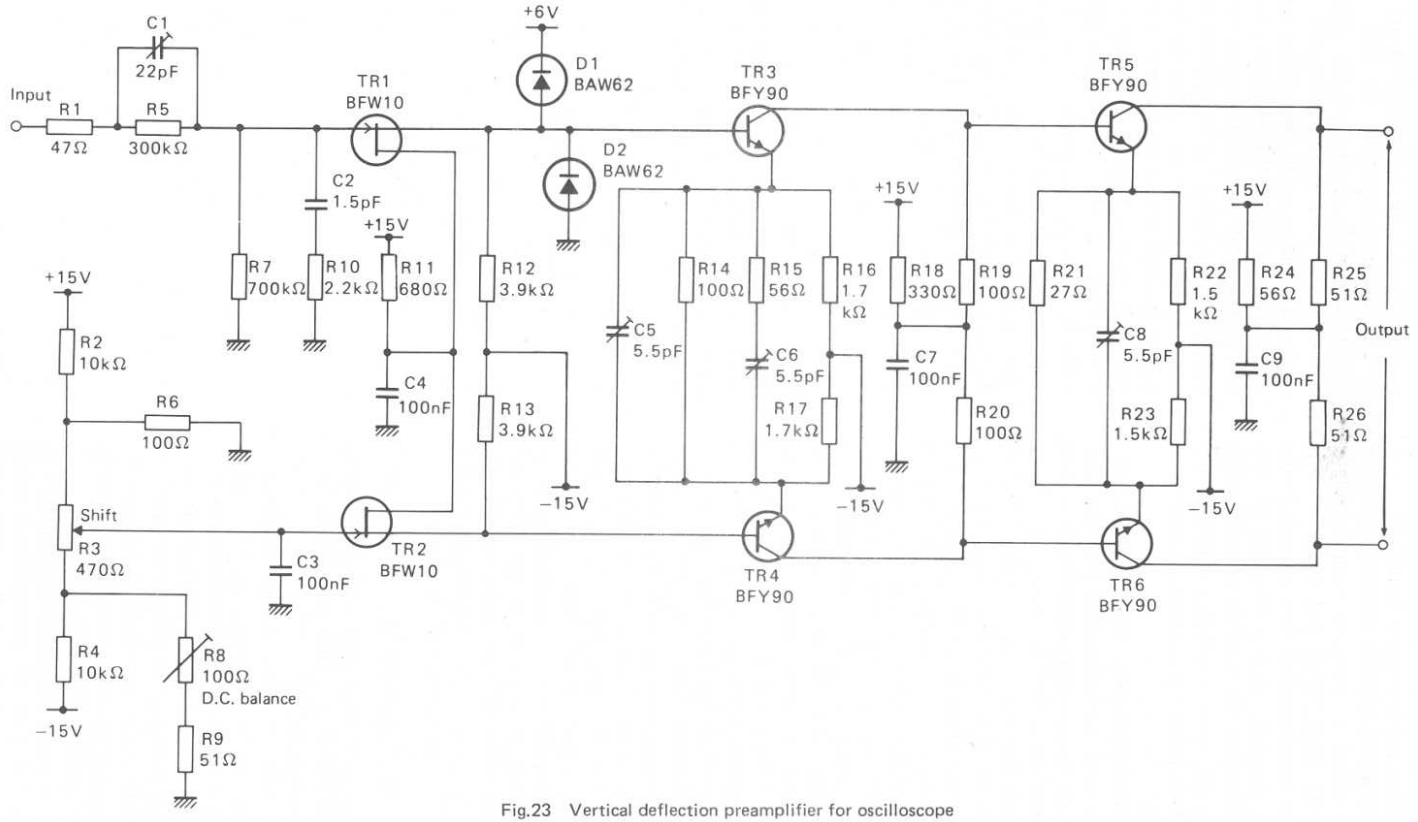


Fig.23 Vertical deflection preamplifier for oscilloscope

frequencies. A source-follower is particularly suitable for use in the input stage because of its low capacitance, high input impedance, and low output impedance.

During ordinary use of an oscilloscope it may happen that too high a voltage is accidentally applied to the signal input of the preamplifier, and measures must therefore be taken to safeguard all the transistors. In the circuit shown, the measures taken are twofold: the network R_1 and R_5 between the signal input and the gate of TR_1 limits the gate current, and the clamping diodes D_1 and D_2 limit both positive and negative excursions of the source voltage.

If a high positive voltage is applied to the signal input, diode D_1 and the diode formed by the gate-source junction of the FET are driven into conduction, the current through them being determined by resistor R_5. Under these circumstances the gate current of the FET can reach a maximum of 10 mA. If a large negative voltage is applied, the current through the FET decreases and D_2 conducts; in which case the source of TR_1 and the base of TR_3 will be clamped to a potential of approximately -0.7 V with respect to earth, even if the gate-drain breakdown voltage of TR_1 is exceeded. Here again the resistors R_5 and R_7 limit the magnitude of the gate current. However, the reverse currents due to large negative voltages, if they persist, can cause damage to the FET, so care must be taken not to keep the probe in contact with such a voltage any longer than necessary.

Capacitor C_1 shunting resistor R_5 prevents undue attenuation of high-frequency signals by the gate-drain and gate-source capacitances. When a high-voltage step function is applied to the signal input, C_1 is charged; for a short period a part of the charge current flows through the gate of the FET, and during this period the FET dissipates energy in the form of heat. The dissipated energy is approximately equal to the energy stored in capacitor C_1 at full charge. The maximum permissible surge energy the FET can withstand is 10 μJ, whence:

$$\tfrac{1}{2}C_1 V_{max}^2 < 10^{-5}\ \text{J}. \qquad (17)$$

Taking the maximum voltage permissible at the signal input to be about 300 V, according to Eq.17 the value of C_1 must be less than 200 pF.

In a test arrangement, rapid voltage transients of 300 V applied to the input by means of a mercury switch did not cause noticeable harm to the transistor.

The FET would, of course, be equally well protected if the diodes were connected to the gate, but then the capacitances of the diodes would unduly increase the total input capacitance. Moreover, their leakage currents would then lead to extra thermal drift.

The FET has an input impedance of about 10^{12} Ω, so the input impedance of the preamplifier is mainly determined by the sum of R_5 and R_7 which equals 1 MΩ. The real part of the input impedance of the circuit, measured at the gate of the FET, is negative for frequencies higher than 10 MHz. This is due to the capacitive load of the source-follower and the phase shift of the transconductance of the FET caused by the transit time of the electrons in the channel. At about 300 MHz, the phase shift reaches 45°. To maintain a positive impedance at all frequencies, a resistor R_{10} is connected in series with capacitor C_2 across the input. The positive real part of this impedance $(1/\omega^2 C_2^2 R_7)$ then overcompensates for the negative real part of the source-follower impedance, and so the input impedance remains positive for all frequencies. Fig.24 shows the input impedance as a function of frequency. Fig.25 is a similar graph of the real part (the input resistance), which is positive for frequencies below 400 MHz.

Since the gain must remain constant from d.c. to 300 MHz, the voltage gain per stage must be kept low. The gain can be stabilised by the adjustable shunt capacitor C_1 and the trimming capacitors in the emitter circuits of the second and third stages. Capacitor C_1 must be chosen so that:

$$R_5 C_1 = R_7\{C_2 + C_{gd} + (1-\alpha)C_{gs}\}, \qquad (18)$$

where C_{gd} is the gate-drain capacitance, C_{gs} is the gate-source capacitance, and α is the voltage gain of TR_1. Then, the voltage attenuation between signal input and the gate of the FET will be the same for a.c. and d.c. and equal to $R_7/(R_5 + R_7)$. From d.c. to 300 MHz the gain is about 3. For an input step function with a rise-time

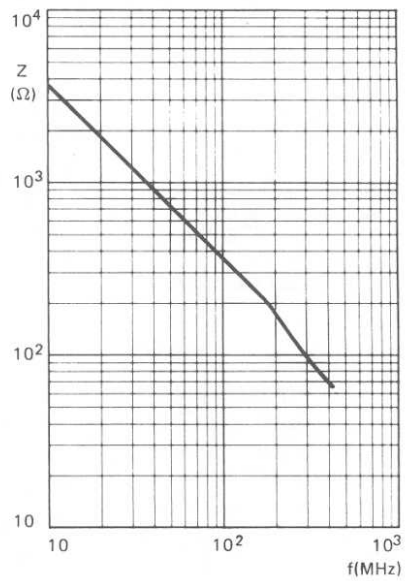


Fig.24 Variation of input impedance with frequency

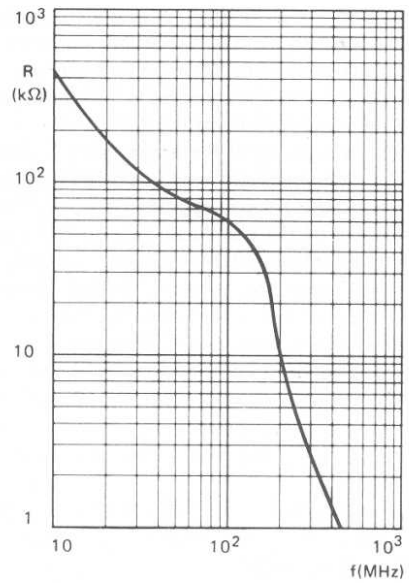


Fig.25 Variation of input resistance with frequency

of about 300 ps the rise-time at the output is about 900 ps, and there is less than 10% overshoot.

The equivalent thermal drift voltage $V_{GS(th)}$ of an n-channel FET is given by:

$$\frac{dV_{GS(th)}}{dT} = \frac{1}{2\mu}\frac{d\mu}{dT}(V_{GS} - V_P) + \frac{d\phi}{dT}, \qquad (19)$$

where $(1/\mu)(d\mu/dT)$ is the relative temperature coefficient of mobility and equals $-8 \times 10^{-3}\ K^{-1}$, V_P is the pinch-off voltage, and $d\phi/dT$ is the change of gate-channel diffusion voltage with temperature (approximately 2.2 mV/K).

The circuit described is a differential amplifier. If the thermal drift voltage of the second and third stages is ignored, and if TR_1 and TR_2 are thermally coupled, the total equivalent thermal drift voltage $dV_{in(th)}$ referred to the signal input will be:

$$\frac{dV_{in(th)}}{dT} = \frac{1}{2\mu}\frac{d\mu}{dT}\{(V_{GS} - V_P)_1 - (V_{GS} - V_P)_2\}, \qquad (20)$$

where the subscripts 1 and 2 refer to transistors TR_1 and TR_2 respectively. Thus the total drift voltage depends on the vertical shift setting, the thermal coupling of TR_1 and TR_2, and the difference between their pinch-off voltages. With the worst possible mismatch between TR_1 and TR_2, the maximum thermal drift is found to be 4 mV/K; with matching it can be limited to 500 μV/K or less, at zero shift setting.

In the range from d.c. to 300 MHz the effective noise signal, measured with the input open-circuited, is less than 200 μV, which is within the width of the electron beam on the screen of even the most sensitive oscilloscope.

TELEVISION CAMERA PREAMPLIFIER USING FETs IN CASCODE

Preamplifiers designed for use with a Plumbicon* television camera tube should satisfy three criteria. First, the preamplifier must have a low input noise, since this will be the determining element in the overall signal-to-noise ratio as Plumbicon camera tubes do not generate

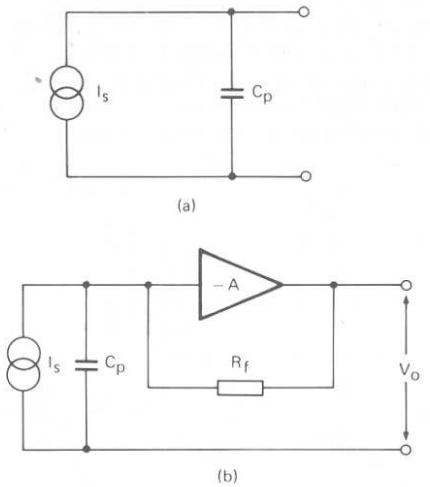


Fig.26 Equivalent circuit of output of Plumbicon tube:
(a) tube only
(b) tube and preamplifier with feedback applied

noise to any noticeable extent. Second, the preamplifier must have a high input impedance because the output from a Plumbicon camera tube can be considered to be a capacitor C_p in parallel with a current source I_s, as shown in Fig.26a. Third, the preamplifier must compensate for the fact that the voltage across C_p is inversely proportional to frequency, to ensure that the overall response is frequency independent.

A flat frequency response can be obtained by using overall current feedback, as shown in Fig.26b. Assuming that the gain of the amplifier is large, $V_o = I_s R_f$ which is frequency independent. However, at frequencies above 500 kHz the voltage gain begins to diminish, so that the

*Plumbicon is a registered trademark for camera tubes.

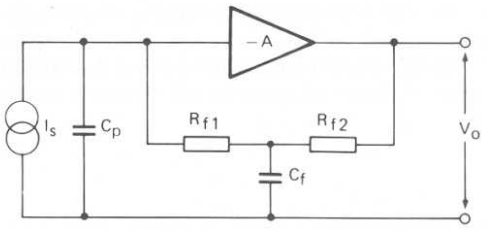


Fig.27 Partially decoupled preamplifier feedback loop

high-frequency response must be improved by partially decoupling the feedback loop as illustrated in Fig.27.

To meet the signal-to-noise ratio requirement, FETs are used in the first stage, because they are less noisy than bipolar transistors when operating with this order of signal-source capacitance. However, full advantage cannot be taken of the lower noise figures unless two FETs are used in cascode configuration. With a single FET input stage, the Miller capacitance reduces the gain at high frequencies and the noise contribution from the second stage becomes too high. A cascode arrangement of a bipolar transistor and a FET is also too noisy; two FETs in cascode give the best performance, and the signal-to-noise ratio of the amplifier is then mainly determined by the input stage noise.

The complete circuit of the preamplifier is shown in Fig.28. The input transistor used is type BSV79 because its input capacitance C_{is} is approximately the same as the capacitance of the Plumbicon tube mounted in the appropriate deflection coil assembly (C_p = 12 pF), thus ensuring that noise is minimised. In this circuit, the collector voltage of the output transistor TR_5 should be set at 28 V by adjusting potentiometer R_1, to avoid clipping of the output waveform at maximum signal amplitude. The drain current of the FETs is then approximately 18 mA. The voltage gain is adjusted by potentiometer R_{20}, and the frequency response by preset capacitor C_{12}.

Table 4 summarises some characteristics of the preamplifier shown in Fig.28. The r.m.s. noise voltage at the output of the preamplifier is shown as a function of frequency in Fig.29.

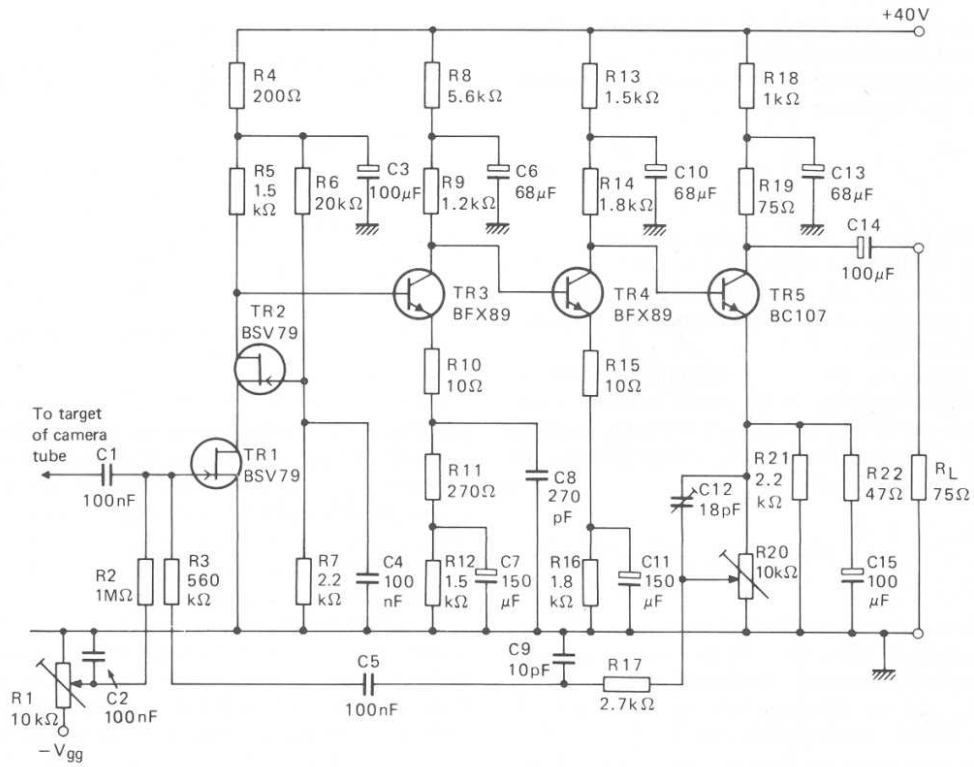


Fig.28 TV camera preamplifier using cascoded BSV79 FETs in the input stage

TABLE 4

Some characteristics of the preamplifier in Fig.28

Forward transfer impedance V_o/I_s (frequency range 40 Hz to 5.5 MHz, $R_L = 75\ \Omega$)	$1 \times 10^6\ \Omega$
Output impedance	$75\ \Omega$
Signal-to-noise ratio (ratio of peak-to-peak output voltage to toal r.m.s. noise voltage, at $I_s = 300$ nA peak-to-peak, in the frequency range 40 Hz to 5.5 MHz)	approx. 46 dB

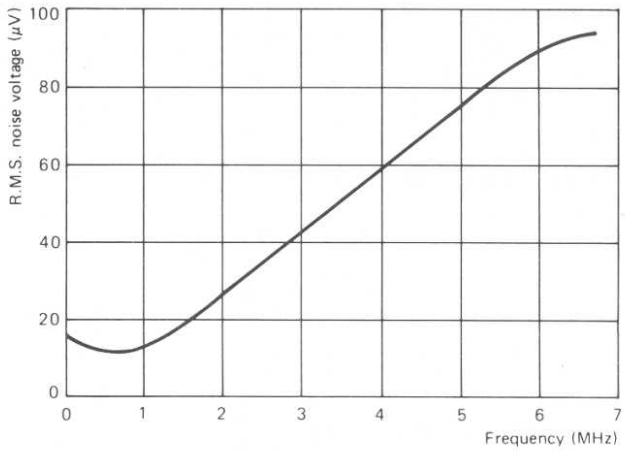


Fig.29 R.M.S. noise voltage at output as function of frequency for bandwidth of 5 kHz and load resistance of 75 Ω.

INTERFACE CIRCUITS USING MOSFETs

Modern electronic circuits often contain both digital and analogue functions, and there is therefore frequently a need to provide interfaces between the analogue and digital parts. An example of such an interface circuit is the electronic switch, a version of which is shown in Fig.30. This circuit uses two n-channel enhancement-mode MOSFETs types SD210 and SD214, though these can be replaced by types SD211 and SD215 respectively, if gate-protected devices are considered necessary. Integrated circuit versions of the electronic switch are also produced; for example, the HEF4066B and SD5000 each contain four switches.

An electronic switch can, for example, be used to interface from the voltage levels and low-power of LOCMOS logic to the voltage levels and high-power of bipolar transistors, as shown in Fig.31. Fig.32a shows an electronic switch used to provide the base drive for an output transistor in a switched-mode power supply. The transformer, shown in Fig.32b, provides isolation between the drive and output circuits, and the manner of winding eliminates the need for an interwinding screen to reduce interference.

Electronic switches have also been used in a novel sample-and-hold balancing and protection circuit for push-pull switched-mode power supplies. This circuit is fully described in Ref.1, and is shown schematically in Fig.33. Briefly, nearly balanced conduction in the output transistors is achieved by storing a voltage proportional to the collector current of one output transistor during one half-cycle of operation of the power supply; the collector current of the other output transistor is then monitored during the following half-cycle and, if it exceeds the stored level by more than a small amount, a signal is generated to terminate the base drive.

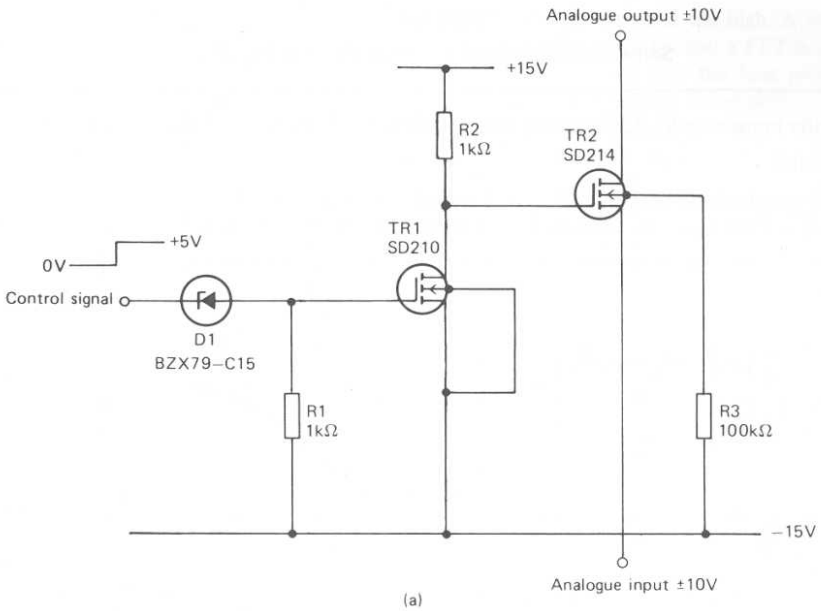


Fig.30 FET electronic switch:
(a) circuit (b) symbol

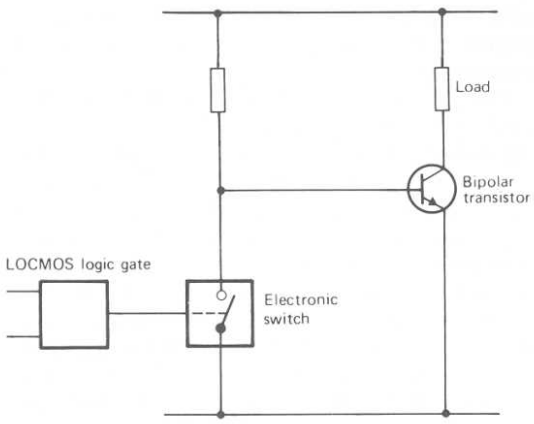


Fig.31 Interface from LOCMOS logic to bipolar transistor

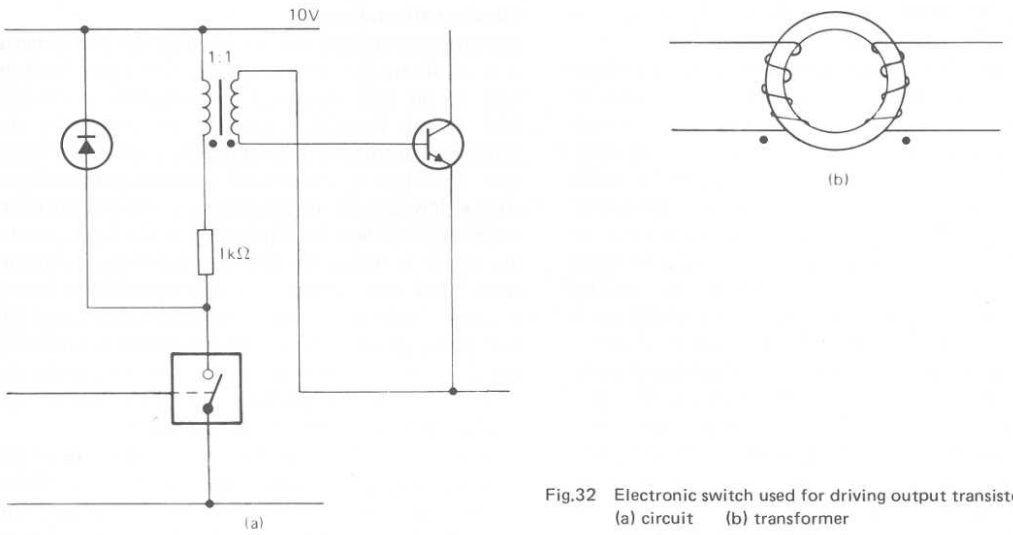
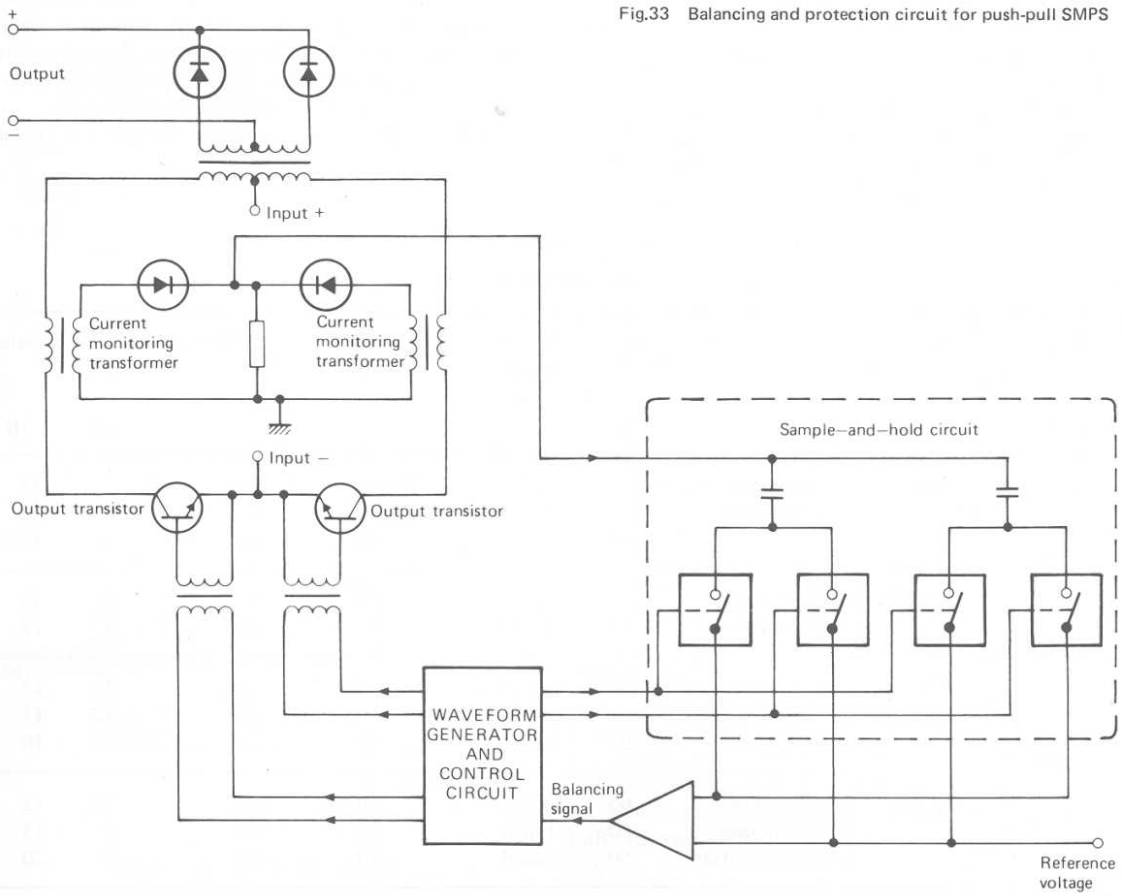


Fig.32 Electronic switch used for driving output transistor in SMPS: (a) circuit (b) transformer

Fig.33 Balancing and protection circuit for push-pull SMPS



R.F. APPLICATIONS OF FETs IN COMMUNICATIONS RECEIVERS

The junction FET is now widely used in the r.f. stages of h.f., v.h.f., and u.h.f. receivers, since it offers superior performance in terms of two critical factors, cross-modulation and intermodulation, and has noise properties equal to bipolar transistors. Cross-modulation is the transfer of the modulation on one carrier to the carrier of another signal. Intermodulation occurs when two or more interfering off-tune signals mix to produce a signal within the receiver passband. Both effects are caused by non-linearity in the transfer characteristic of the active device, the degree of intermodulation and cross-modulation depending on the third-order and higher-order odd terms in the transfer characteristic for an amplifier, and the fourth-order and higher-order even terms for a mixer. Clearly, if the active device had a perfect square-law characteristic neither effect would occur, but both bipolar transistors and FETs have higher-order terms in their characteristics. The FET, however, is superior to the bipolar transistor in this respect. For example, taking impedance differences into account, a 12 dB improvement in cross-modulation in a narrowband f.m. system, and a 20 dB improvement in a v.h.f. broadcast receiver, can be achieved by replacing a bipolar mixer by a FET.

Table 5 compares the noise performance of FETs and bipolar transistors in various configurations.

Circuit configurations

The cross-modulation and intermodulation performance of a circuit are functions of the interfering signal voltage level. In the common-source configuration, the voltage level of any interfering signal is stepped up by the matching transformer necessitated by a high input resistance. The input resistance in the common-gate configuration is low, and so for the same power input the interfering signal voltage level appearing at the input port of the device is higher for the common-source configuration. Thus cross-modulation and intermodulation occur at lower levels in a common-source amplifier, and for best performance the common-gate circuit is preferred. The argument also applies to mixer circuits, where the input signal should be applied to the source and the local oscillator output to the gate for best results.

Table 5 shows that the best gain and noise figure are obtained from a neutralised common-source amplifier. However, since the values of feedback capacitance and input impedance are high, neutralisation is needed to maintain stability; otherwise the load impedance, and consequently the gain, must be low. The common-gate amplifier, on the other hand, has low feedback capacitance and gives stable gain well into the u.h.f. band. Clearly the choice of configuration must depend on the relative emphasis placed on cross-modulation and intermodulation, and noise and gain in each application.

A third alternative is available: the cascode circuit

TABLE 5

Noise performance at r.f.

Frequency	Device	Configuration	R_s	Source reactance	Approx. input resistance	Neutralisation	Noise figure	Gain
MHz			Ω		Ω		dB	dB
100	FET	common-source	1000	tuned	20 000	yes	2	18
		common-gate	200	tuned	200	no	4	12
		cascode	1000	tuned	3 000	no	3	17.5
	bipolar	common-base	100	opt. C	20	no	2	15
		common-base	20	tuned	20	no	3	17
470	FET	common-source	1000	tuned	1 000	yes	4	12
		common-gate	67	opt. C	140	no	4.5	11
		common-gate	67	tuned	140	no	5.5	10
	bipolar	common-base	66	opt. C	50	no	4.2	12
		common-base	50	tuned	50	no	5	15
		common-emitter	50	tuned	70	no	5	20

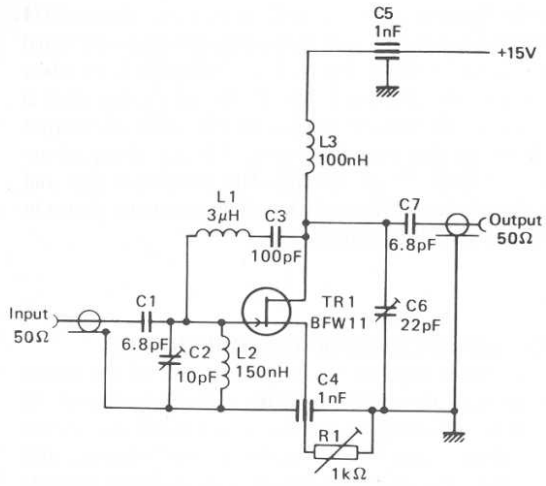


Fig.34 100 MHz common-source amplifier

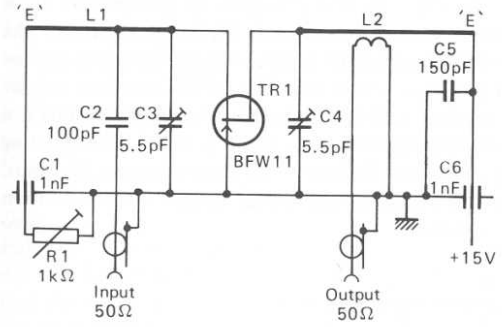


Fig.35 470 MHz common-gate amplifier

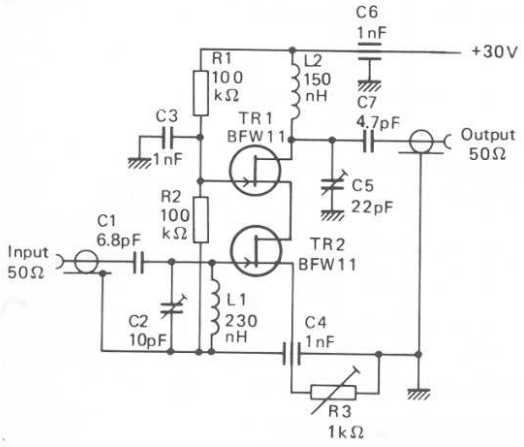


Fig.36 100 MHz cascode amplifier

provides a compromise between the good noise performance of the common-source circuit and the good stability of the common-gate circuit. The load of the common-source stage is the input impedance of the common-gate stage (about 200 Ω at 200 MHz), giving stability without neutralisation but still requiring care in construction because the stability factor is not high.

Biasing arrangements

To meet biasing requirements, either a source resistance or a constant-current source can be used if a negative line or a high-voltage positive line is available. It is important to appreciate the effect of a wide spread in I_{DSS} on the bias arrangment; the device should not be biased at $V_{GS} = 0$ V because the current with high-I_{DSS} devices would be unacceptably large. Normally, the device is operated at a value of V_{GS} equal to half the pinch-off voltage V_P. In a mixer, a bias voltage of $V_P/2$ is used, because this value results in a minimum for the fourth-order term in the transfer characteristic and therefore minimum cross-modulation and intermodulation. It should be remembered that the peak local oscillator amplitude should not exceed $V_P/2$, otherwise non-linearity increases and eventually the gate-source junction is driven into conduction.

A disadvantage of the cascode circuit is the large supply voltage needed to drive both devices into the saturation region.

Practical circuits

Practical amplifiers and mixers using FETs in various configurations are discussed below.

Amplifiers

Figs.34 to 36 show three r.f. amplifier circuits using BFW11 FETs in the common-source, common-gate, and cascode configurations.

For a 100 MHz neutralised common-source amplifier (Fig.34), fed from the optimum source resistance of 1 kΩ, a noise figure of 2 dB is typical. A similar amplifier designed for 470 MHz operation would give a noise figure of 4 dB. The common-gate amplifier of Fig.35 gives less gain than the previous circuit and slightly inferior noise performance. For the 470 MHz amplifier shown, the noise figure is typically 5.5 dB, and the power gain is 11 dB. By off-tuning the input slightly, the noise figure may be improved to 4.5 dB, but this is not a practical solution in a tuned amplifier. Fig.36 shows a 100 MHz cascode circuit with a typical noise figure of 3 dB. The two FETs should be selected for similar values of I_{DSS}.

Mixers

A mixer circuit is shown in Fig.37. The FET is biased at $V_{GS} = V_P/2$ and, again, careful circuit design is necessary to allow for a spread in values of I_{DSS}. With no oscillator drive, I_D is set to 2 mA.

The input signal is applied to the source, and the local oscillator signal to the gate. With this arrangement a noise figure of 9 dB is typical. A capacitively-tuned $\lambda/4$ transmission line is used as the tuning element for signal and local oscillator inputs. When using FETs in mixer circuits, the limiting factor in the conversion gain is often the dynamic impedance of the coil in the output circuit. In this design the value is 25 kΩ, giving an unloaded Q of 75 at 30 MHz. The conversion gain and signal blocking characteristics of the circuit are shown in Figs.38 and 39 respectively.

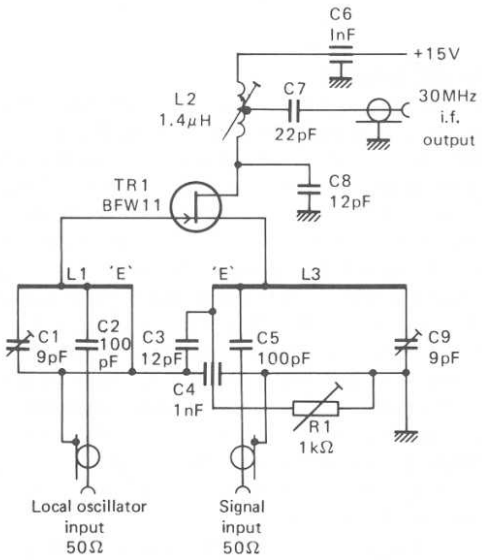


Fig.37 Mixer circuit

R.F. APPLICATIONS OF TETRODE MOSFETs

The tetrode MOS transistor possesses all of the advantages of junction FETs compared with bipolar transistors used at radio frequencies; that is, low noise, good intermodulation and cross-modulation performance, and excellent blocking characteristics. In addition, the tetrode MOS transistor allows the possibility of a cascode connected stage using a single transistor and also provides a simple means of gain control. The following three circuits use a BFS28 transistor to demonstrate these advantages and to show the particular merits of the BFS28 transistor; that is, good stability at high frequency and good conversion gain. The BFS28 transistor may be replaced by a BFR84 transistor (or a BF327 which is a plastic-encapsulated version), if a device incorporating gate-protection diodes is considered necessary. However, these transistors have a slightly inferior intermodulation performance.

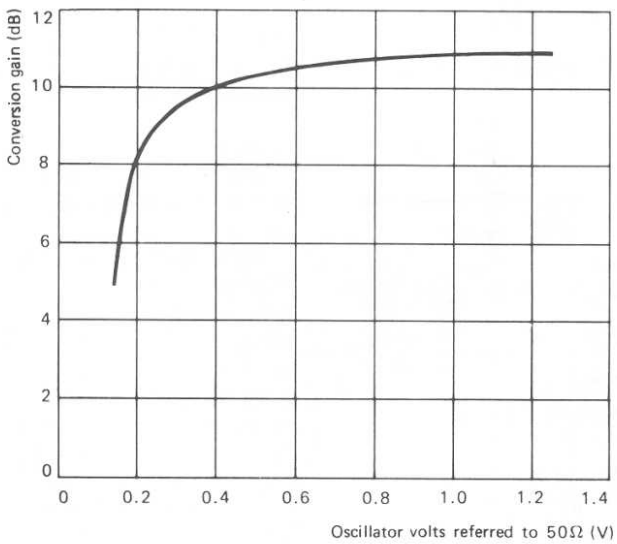


Fig.38 Conversion gain as function of oscillator voltage measured at drain current of 2 mA, with 3 dB bandwidth of 600 kHz, for device with $I_{DSS} = 4.4$ mA

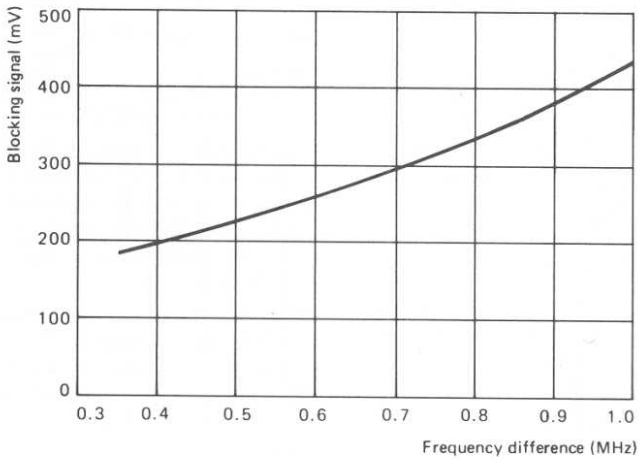


Fig.39 Blocking signal as function of frequency difference

BFS28 as amplifier at 200 MHz

The values in Table 6 indicate the performance obtained with a test amplifier operating at 200 MHz, as shown in Fig.40, compared with a BF200 bipolar transistor used in a similar type of circuit. The nominal d.c. setting of the FET amplifier is $V_D = 17$ V, $I_D = 10$ mA, and $V_{G2} = +8$ V.

Gain

Full gain control can be obtained by varying V_{G2} from +8 to −8 V. A comparison of Fig.41 with Fig.42 shows that the maximum gain is some 2 dB higher than with the BF200 bipolar transistor.

Noise figure

The noise figure of the BFS28 is slightly better than that of the bipolar transistor (see Figs.41 and 42).

TABLE 6

Comparison of BFS28 and BF200 as amplifiers at 200 MHz

Type	Gain dB	Noise figure dB
BFS28	18.0	3.9
BF200	16.0	5.1

Cross-modulation

The cross-modulation performance of the BFS28 is better by a factor of about five than the cross-modulation of the bipolar transistor (see Fig.43).

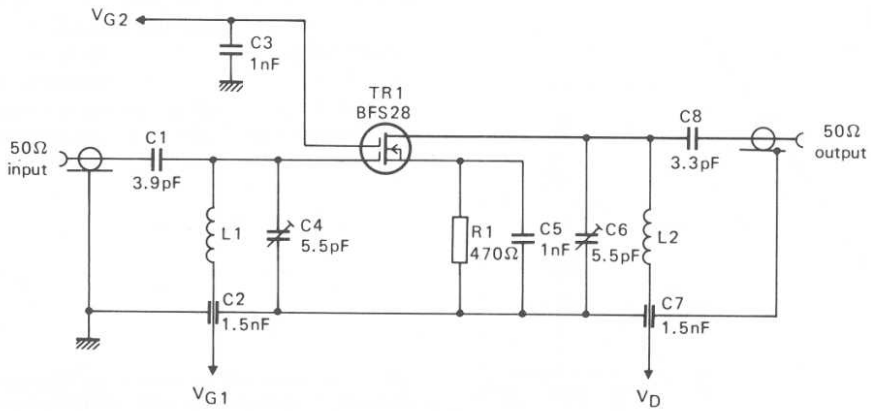


Fig.40 200 MHz amplifier using tetrode MOST

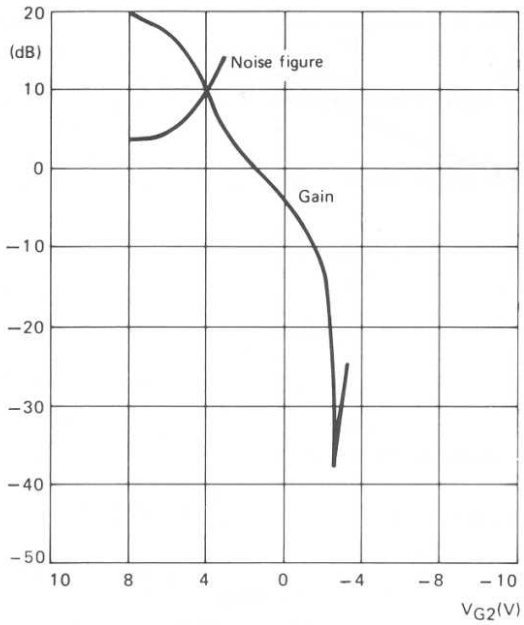


Fig.41 Noise figure and gain against gate voltage for typical BFS28, measured at drain voltage of 17 V and with gate 1 at +3 V

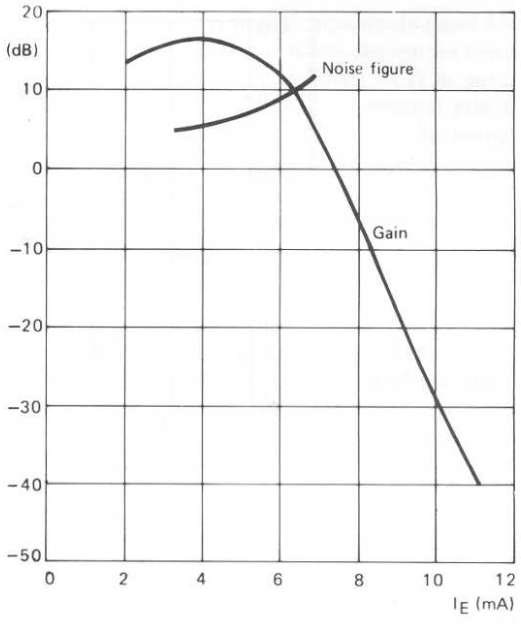


Fig.42 Noise figure and gain against emitter current for typical BF200, plotted for comparison with Fig.41. Measurements made on common-base amplifier with collector voltage of 12 V and emitter resistor of 27 Ω

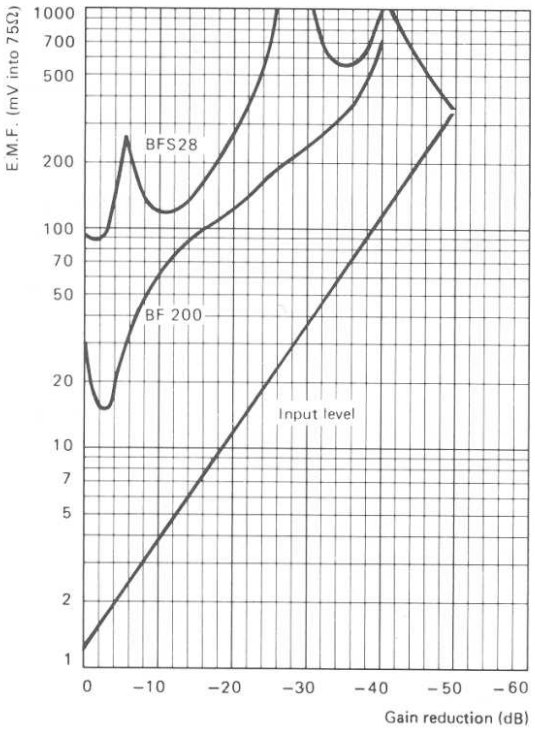


Fig.43 Interfering e.m.f. against gain for 1% cross-modulation, with wanted frequency of 200 MHz and interfering frequency of 205 MHz

Intermodulation

Since intermodulation is caused by the same high-order terms in the transfer characteristic that produce cross-modulation, the intermodulation performance may be expected to improve by the same factor (five) as cross-modulation.

Blocking

A blocking test applied to the mixer reveals that an interfering signal of 85 mV (across 50 Ω) at 400 kHz separation from the carrier produces a 3 dB attenuation of the carrier. The UK specification is for a minimum of 12.7 mV under these conditions; therefore r.f. amplification of up to 16.5 dB can be interposed between the aerial and the mixer without causing the receiver blocking performance to fall outside the specified limit.

BFS28 as amplifier at 470 MHz

To utilise the performance of the BFS28 at u.h.f., a strip-line amplifier has been constructed to operate at 470 MHz. The use of strip-lines offers several advantages: they are easier to construct with accurate inductance and capacitance than are lumped-component circuits; stray reactances are more easily controlled; construction in general is easier; production-line assembly of circuits is facilitated; they are more compact and lighter; and the technique is easily extended to higher frequencies.

The material used for the strip-line amplifier is p.t.f.e.-loaded glass-fibre, copper-clad on both sides giving a thickness of 1.6 mm. The dielectric constant of the insulation material is 2.75 and the thickness is 1.55 mm. The resonant line width is 1 mm and the ratio of free-space wavelength to effective wavelength (λ_0/λ_m) is 1.47. The line characteristic impedance is 100 Ω. The lines thus constructed give a loaded Q of about 50 and offer a load of 5 kΩ at their resonant frequency. A capacitance of about 3 pF is required for tuning to 470 MHz.

The circuit of the amplifier is shown in Fig.44. The 100 pF capacitors C_1 and C_{10} at the input and output offer a very low impedance. Gate 2 is heavily decoupled to maintain it at r.f. earth potential, and similar decoupling is used with the other d.c. connections. A power gain of typically 15 dB is obtainable with BFS28 transistors used in this circuit.

BFS28 as mixer at 470 MHz

Mixing at 470 MHz with the BFS28 can be carried out by applying the signal to gate 1 and injecting the local oscillator output into the source; gate 2 is kept well decoupled. This approach has been used in the mixer shown in Fig.45 which has been constructed using a strip-line design, as with the amplifier discussed previously.

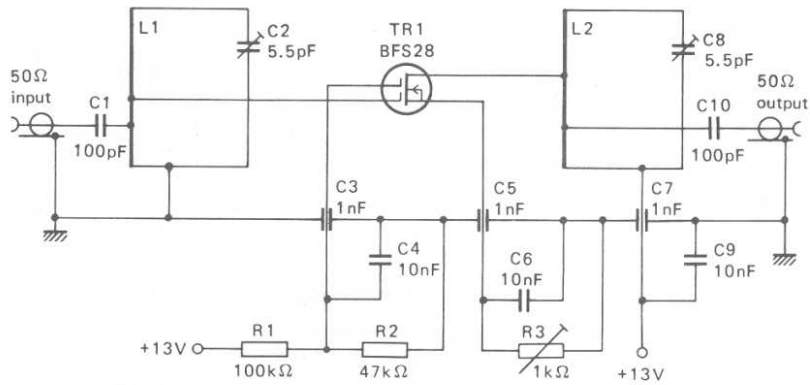


Fig.44 470 MHz amplifier

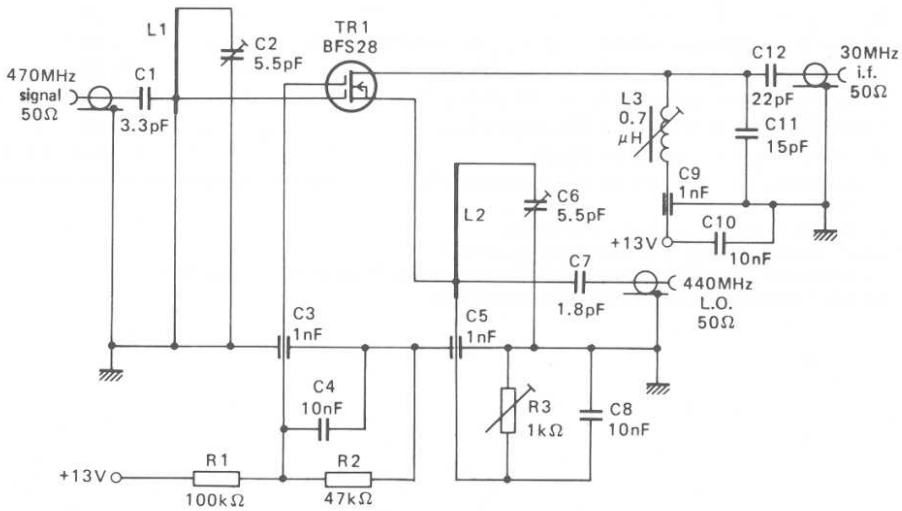


Fig.45 470 MHz mixer

The standard y-parameter technique is used to design the mixer. The signal and oscillator input tuned circuits are of high Q and so, for an input signal at 470 MHz, the source tuned to 440 MHz can be considered as earthed. Similarly, the transistor can be regarded as operating in the common-gate mode for the local oscillator injection.

Measurements made on the mixer shown in Fig.45 reveal that, for optimum gain conditions, the gain has an average value of 9.8 dB. For optimum noise conditions, the average noise figure is 13.3 dB with an average conversion gain of 8.8 dB. (The optimum gain conditions occur at $I_D \simeq 3$ mA and $V_{G1-S} \simeq 1.5$ V. The optimum noise conditions occur at $I_D \simeq 1$ mA and $V_{G1-S} \simeq -2$ V.) The above values occur under the following conditions:

V_{DS}	$= +13$ V,
V_{G2-S}	$= +4$ V,
signal e.m.f.	$= 2$ mV (into 50 Ω),
local oscillator e.m.f.	$= 2$ V (into 50 Ω).

F.M. TUNER FRONT-END WITH FET MIXER

A junction FET can be the best compromise between cost and ideal device characteristics when selecting a mixer for f.m. tuner front-ends. The circuit shown in Fig.46, which is fully described in Ref.2, uses a low-cost junction FET mixer in a simple but carefully optimised design to give an overall performance equal to (and in some respects better than) more complex designs. Performance figures for the circuit of Fig.46 are given in Table 7.

The local oscillator and r.f. signals are applied in series to the gate of the FET, and the consequent loose coupling between r.f. and oscillator circuits gives freedom from oscillator pulling for aerial input signal levels up to 250 mV e.m.f. (75 Ω). This configuration also has the advantages of giving a relatively high gain and requiring only low oscillator power.

REFERENCES

1. JANSSON, L. E., 'A sample-and-hold balancing and protection circuit for push-pull switched-mode power supplies', **Mullard Technical Communications**, Vol. 14, No. 140, October 1978, pp. 424 to 438.
2. MALCOLM, J. S., 'F.M. radio front-end with improved large signal handling performance', **Mullard Technical Communications**, Vol. 12, No. 119, July 1973, pp. 262 to 270.

TABLE 7

Performance of f.m. tuner front-end

Characteristic	Value	Notes
Gain	22 dB	
Noise figure	4 dB	
Repeat spot suppression relative to 20 μV e.m.f. wanted signal	82 dB	
Level of interfering signal for 1% intermodulation	26 dB	1, 2
Level of interfering signal for 1% cross-modulation	30 dB	1, 3
Level of interfering signal for 3 dB compression	38 dB	1, 4
Signal level for 5 kHz oscillator pulling	> 250 mV e.m.f.	

Notes
1) Relative to 1 mV e.m.f. (75 Ω) wanted signal
2) Interfering signal spaced 200 kHz from wanted signal
3) Interfering signal is 30% amplitude-modulated and spaced 3 MHz from wanted signal
4) Interfering signal spaced 400 kHz from wanted signal

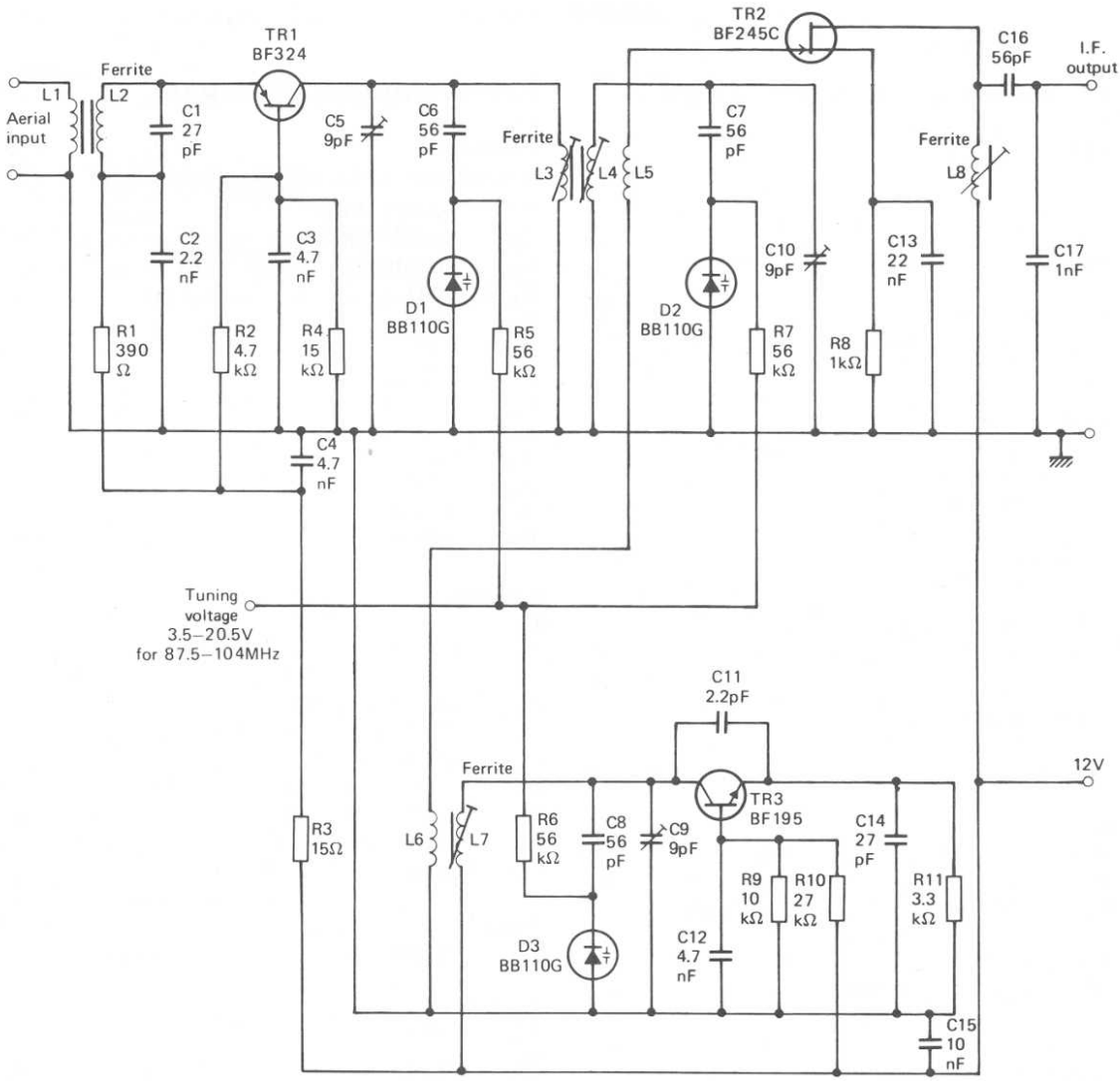


Fig.46 F.M. tuner front-end

COMPONENT LISTS

Constant-current drive for LED indicator (Fig.9)

Current	*10 mA*	*20 mA*	
Resistors			
R_1	39 Ω	68 Ω	CR25, ±10%
R_2	270 Ω	270 Ω	preset potentiometer
Transistor			
TR_1	BF245C	BF246B BSV78	
Diode			
D_1	CQX51 super-red CQY96 yellow CQY94 green		CQY24B red
Supply voltage			
V_S	8.5 to 32 V	12 to 28 V (BF246B) 12 to 43 V (BSV78)	

Polarity indicator (Fig.10)

Current	*10 mA*	*20 mA*	
Resistors			
R_1	1 kΩ	1 kΩ	CR25, ±10%
R_2	39 Ω	68 Ω	CR25, ±10%
R_3	270 Ω	270 Ω	preset potentiometer
Transistor			
TR_1	BF245C	BF246B BSV78	
Diodes			
D_1	CQX51 super-red CQY91 yellow CQY94 green		CQY24B red
D_2	BAW62		BAW62
Supply voltage			
V_S	8.5 to 32 V	12 to 28 V (BF246B) 12 to 43 V (BSV78)	

Radiation detector preamplifier (Fig.21)

Resistors

All resistors are CR25, ±5% except where noted

R_1	5.6 MΩ	VR37
R_2	51 MΩ	VR68
R_3	102 MΩ (2 x 51 MΩ)	VR68
R_4	22 Ω	
R_5	22 Ω	
R_6	680 Ω	
R_7	33 kΩ	
R_8	120 kΩ	
R_9	3 kΩ typical value	
R_{10}	68 kΩ	
R_{11}	33 kΩ	
R_{12}	6.8 kΩ	
R_{13}	100 Ω	

Capacitors

C_1	1 pF	
C_2	0.82 pF	
C_3	1 nF	311 51102
C_4	68 nF	357 81683
C_5	10 μF, 63 V	108 18109
C_6	150 μF, 40 V	108 17151
C_7	39 pF typical value	
C_8	10 μF, 63 V	108 18109
C_9	10 nF	344 55103
C_{10}	10 nF	344 55103

Inductor

L_1	65 mH

Transistors

TR_1	BFW11
TR_2	BFW11
TR_3	BSX20
TR_4	BC109
TR_5	BC109

Diode

D_1	BZX79-C9V1

Preamplifier for wideband oscilloscope (Fig.23)

Resistors

All resistors are CR25, ±5% except where noted

R_1	47 Ω
R_2	10 kΩ
R_3	470 Ω potentiometer
R_4	10 kΩ
R_5	300 kΩ MR25, ±2%
R_6	100 Ω
R_7	700 kΩ (680 kΩ + 20 kΩ) MR30, ±2%
R_8	100 Ω preset potentiometer
R_9	51 Ω
R_{10}	2.2 kΩ
R_{11}	680 Ω
R_{12}	3.9 kΩ
R_{13}	3.9 kΩ
R_{14}	100 Ω
R_{15}	56 Ω
R_{16}	1.7 kΩ
R_{17}	1.7 kΩ
R_{18}	330 Ω
R_{19}	100 Ω
R_{20}	100 Ω
R_{21}	27 Ω
R_{22}	1.5 kΩ
R_{23}	1.5 kΩ
R_{24}	56 Ω
R_{25}	51 Ω
R_{26}	51 Ω

Capacitors

C_1	22 pF 808 11229
C_2	1.5 pF
C_3	100 nF 344 25104
C_4	100 nF 344 25104
C_5	5.5 pF 808 11558
C_6	5.5 pF 808 11558
C_7	100 nF 344 25104
C_8	5.5 pF 808 11558
C_9	100 nF 344 25104

Transistors

TR_1	BFW10
TR_2	BFW10
TR_3	BFY90
TR_4	BFY90
TR_5	BFY90
TR_6	BFY90

Diodes

D_1	BAW62
D_2	BAW62

TV camera preamplifier (Fig.28)

Resistors

All resistors are CR25, ±5% except where noted

R_1	10 kΩ preset potentiometer
R_2	1 MΩ MR30, ±2%
R_3	560 kΩ
R_4	200 Ω MR25, ±2%
R_5	1.5 kΩ MR25, ±2%
R_6	20 kΩ MR25, ±2%
R_7	2.2 kΩ MR25, ±2%
R_8	5.6 kΩ
R_9	1.2 kΩ
R_{10}	10 Ω
R_{11}	270 Ω
R_{12}	1.5 kΩ
R_{13}	1.5 kΩ
R_{14}	1.8 kΩ
R_{15}	10 Ω
R_{16}	1.8 kΩ
R_{17}	2.7 kΩ
R_{18}	1 kΩ
R_{19}	75 Ω
R_{20}	10 kΩ preset potentiometer
R_{21}	2.2 kΩ
R_{22}	47 Ω

Capacitors

C_1	100 nF 344 51104
C_2	100 nF 344 25104
C_3	100 μF, 63 V 108 18101
C_4	100 nF 344 25104
C_5	100 nF 344 25104
C_6	68 μF, 63 V 108 18689
C_7	150 μF, 63 V 108 18151
C_8	270 pF 427 22701
C_9	10 pF 632 10109
C_{10}	68 μF, 63 V 108 18689
C_{11}	150 μF, 63 V 108 18151
C_{12}	18 pF 809 09003
C_{13}	68 μF, 63 V 108 18689
C_{14}	100 μF, 63 V 108 18101
C_{15}	100 μF, 63 V 108 18101

Transistors

TR_1	BSV79
TR_2	BSV79
TR_3	BFX89
TR_4	BFX89
TR_5	BC107

Electronic switch (Fig.30)

Resistors

R_1	1 kΩ	CR25, ±5%
R_2	1 kΩ	CR25, ±5%
R_3	100 kΩ	CR25, ±5%

Transistors

TR_1	SD210 or SD211
TR_2	SD214 or SD215

Diode

D_1	BZX79-C15

100 MHz common-source amplifier (Fig.34)

Resistor

R_1	1 kΩ preset potentiometer

Capacitors

C_1	6.8 pF	632 09688
C_2	10 pF	809 05002
C_3	100 pF	632 34101
C_4	1 nF	feedthrough capacitor
C_5	1 nF	feedthrough capacitor
C_6	22 pF	808 11229
C_7	6.8 pF	632 09688

Inductors

L_1	3 μH
L_2	150 nH
L_3	100 nH

Transistor

TR_1	BFW11

470 MHz common-gate amplifier (Fig.35)

Resistor

R_1	1 kΩ preset potentiometer

Capacitors

C_1	1 nF	feedthrough capacitor
C_2	100 pF	632 34101
C_3	5.5 pF	809 09001
C_4	5.5 pF	809 09001
C_5	150 pF	632 34151
C_6	1 nF	feedthrough capacitor

Inductors

Characteristic impedance of line is 70 Ω

L_1	60 mm of 6.5 mm o/d copper, tap at 40 mm from E
L_2	70 mm of 6.5 mm o/d copper, tap at 40 mm from E

Transistor

TR_1	BFW11

100 MHz cascode amplifier (Fig.36)

Resistors

R_1	100 kΩ	CR25, ±5%
R_2	100 kΩ	CR25, ±5%
R_3	1 kΩ	preset potentiometer

Capacitors

C_1	6.8 pF	632 09688
C_2	10 pF	808 11109
C_3	1 nF	629 02102
C_4	1 nF	feedthrough capacitor
C_5	22 pF	808 11229
C_6	1 nF	feedthrough capacitor
C_7	4.7 pF	632 09478

Inductors

L_1	230 nH
L_2	150 nH

Transistors

TR_1	BFW11
TR_2	BFW11

Mixer circuit (Fig.37)

Resistor

R_1 1 kΩ preset potentiometer

Capacitors

C_1 9 pF 809 09002
C_2 100 pF 632 34101
C_3 12 pF 632 10129
C_4 1 nF feedthrough capacitor
C_5 100 pF 632 34101
C_6 1 nF feedthrough capacitor
C_7 22 pF 632 34229
C_8 12 pF 632 10129
C_9 9 pF 809 09002

Inductors

Characteristic impedance of line for L_1 and L_3 is 70 Ω

L_1 85 mm of 6.5 mm o/d copper, gate tap at 26 mm from E, local oscillator input at 15 mm from E

L_2 1.4 μH

L_3 85 mm of 6.5 mm o/d copper, signal input tap at 9 mm from E, source tap at 17 mm from E

Transistor

TR_1 BFW11

200 MHz amplifier (Fig.40)

Resistor

R_1 470 Ω CR25, ±5%

Capacitors

C_1 3.9 pF 632 09398
C_2 1.5 nF feedthrough capacitor
C_3 1 nF 629 02102
C_4 5.5 pF 809 09001
C_5 1 nF 629 02102
C_6 5.5 pF 809 09001
C_7 1.5 nF feedthrough capacitor
C_8 3.3 pF 632 09338

Inductors

L_1 2 turns of 1.25 mm wire, length 2 mm, i/d 8 mm

L_2 2 turns of 0.90 mm silvered wire, wire length 20 mm, i/d 14 mm

Transistor

TR_1 BFS28 or BFR84 or BF327

470 MHz amplifier (Fig.44)

Resistors

R_1	100 kΩ	CR25, ±5%
R_2	47 kΩ	CR25, ±5%
R_3	1 kΩ	preset potentiometer

Capacitors

C_1	100 pF	632 34101
C_2	5.5 pF	809 09001
C_3	1 nF	feedthrough capacitor
C_4	10 nF	629 02103
C_5	1 nF	feedthrough capacitor
C_6	10 nF	629 02103
C_7	1 nF	feedthrough capacitor
C_8	5.5 pF	809 09001
C_9	10 nF	629 02103
C_{10}	100 pF	632 34101

Inductors

Inductors are tracks on double-sided copper-clad 1.6 mm thick p.t.f.e.-loaded glass-fibre board

L_1	52.6 mm long, 1 mm wide
L_2	50.8 mm long, 1 mm wide

Transistor

TR_1 BFS28 or BFR84 or BF327

470 MHz frequency mixer (Fig.45)

Resistors

R_1	100 kΩ	CR25, ±5%
R_2	47 kΩ	CR25, ±5%
R_3	1 kΩ	preset potentiometer

Capacitors

C_1	3.3 pF	632 09338
C_2	5.5 pF	809 09001
C_3	1 nF	feedthrough capacitor
C_4	10 nF	629 02103
C_5	1 nF	feedthrough capacitor
C_6	5.5 pF	809 09001
C_7	1.8 pF	632 09188
C_8	10 nF	629 02103
C_9	1 nF	feedthrough capacitor
C_{10}	10 nF	629 02103
C_{11}	15 pF	632 10159
C_{12}	22 pF	632 34229

Inductors

L_1 and L_2 are tracks on double-sided copper-clad 1.6 mm thick p.t.f.e.-loaded glass-fibre board

L_1	52.2 mm long, 1 mm wide
L_2	47.1 mm long, 1 mm wide
L_3	16½ turns of 0.45 mm wire on 4.5 mm former, 0.7 μH

Transistor

TR_1 BFS28, BFR84, or BF327

F.M. tuner front-end (Fig.46)

Resistors

All resistors are CR25, ±5%

R_1	390 Ω
R_2	4.7 kΩ
R_3	15 Ω
R_4	15 kΩ
R_5	56 kΩ
R_6	56 kΩ
R_7	56 kΩ
R_8	1 kΩ
R_9	10 kΩ
R_{10}	27 kΩ
R_{11}	3.3 kΩ

Capacitors

C_1	27 pF	632 34279
C_2	2.2 nF	629 02222
C_3	4.7 nF	629 02472
C_4	4.7 nF	629 02472
C_5	9 pF	809 09002
C_6	56 pF	632 34569
C_7	56 pF	632 34569
C_8	56 pF	632 34569
C_9	9 pF	809 09002
C_{10}	9 pF	809 09002
C_{11}	2.2 pF	632 09228
C_{12}	4.7 nF	629 02472
C_{13}	22 nF	629 02223
C_{14}	27 pF	632 34279
C_{15}	10 nF	629 02103
C_{16}	56 pF	632 34569
C_{17}	1 nF	629 02102

Inductors

L_1, L_2	4 and 2½ turns respectively, 0.400 mm t.n.a., bifilar-wound on 5 mm diameter former with core.
L_3, L_4	5 turns, 0.560 mm enamelled copper, spaced 1 diameter, on 5 mm diameter former with core.
L_5	3 turns, 0.400 mm t.n.a., bifilar-wound with L_4.
L_6	1 turn, 0.400 mm t.n.a., coupled to L_7.
L_7	5½ turns, 0.560 mm enamelled copper, spaced 1 diameter, on 5 mm diameter former with core.
L_8	20 turns, 3 x 0.063 mm litz, wound on 7 x 7 mm coil assembly.

Transistors

TR_1	BF324
TR_2	BF245C
TR_3	BF195

Diodes

D_1	BB110G
D_2	BB110G
D_3	BB110G