

# DATA ACQUISITION PRODUCTS CATALOG SUPPLEMENT



DATA ACQUISITION  
PRODUCTS CATALOG



 **ANALOG  
DEVICES**



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| AD536A        | 65S    | ADC-16Q               | 463(C) | SHA1134                           | 529(C) | 903         | 333S   |
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| AD544         | 37S    | AD DAC85              | 155S   | SMX2607                           | 564(C) | 907         | 594(C) |
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| AD565         | 121S   | DAC1009               | 339(C) | STX1003                           | 564(C) | 922         | 333S   |
| AD566         | 129S   | DAC1106/08            | 343(C) | STX2603                           | 564(C) | 923         | 333S   |
| AD570         | 199S   | DAC1118               | 347(C) | THS, THC Series                   | 305S   | 925         | 594(C) |
| AD571         | 207S   | DAC1125               | 349(C) | TSL1612/TSDC1608<br>thru TSDC1611 | 289S   | 934         | 333S   |
| AD572         | 395(C) | DAC1132               | 353(C) | 48                                | 69(C)  | 940         | 333S   |
| AD574         | 215S   | DAC1136/1137/<br>1138 | 167S   | 50/51                             | 71(C)  | 941         | 333S   |
| AD580         | 241(C) | DAC1422               | 179S   | 52                                | 75(C)  | 942         | 596(C) |
| AD581         | 71S    | DAC-10DF              | 365(C) | 171                               | 77(C)  | 943         | 333S   |
| AD582         | 509(C) | DAC-QM/QG             | 367(C) | 2B20                              | 93S    | 944         | 596(C) |
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| AD584         | 77S    | DAC-12QZ              | 375(C) | 2B30/31                           | 101S   | 946         | 596(C) |
| AD590         | 85S    | DAC-10Z/<br>MDA-10Z   | 377(C) | 2B35                              | 107S   | 949         | 333S   |
| AD741         | 65(C)  | DAS1128               | 565(C) | 234                               | 81(C)  | 951         | 333S   |
| AD1408/1508   | 295(C) | DAS1150/1151          | 329S   | 235                               | 85(C)  | 952         | 333S   |
| AD2020        | 403(C) | DSC1705/1706          | 261S   | 260                               | 89(C)  | 953         | 333S   |
| AD2023        | 407(C) | DTM1716/1717          | 265S   | 261                               | 91(C)  | 955         | 333S   |
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| AD2700/01/02  | 265(C) | HTS, HTC Series       | 293S   |                                   |        | 975         | 333S   |
| AD7501/02/03  | 537(C) | IDC Series            | 504(C) |                                   |        |             |        |
| AD7506/07     | 541(C) | MAS Series            | 235S   |                                   |        |             |        |
| AD7510D1      | 545(C) | MATV Series           | 241S   |                                   |        |             |        |
| AD7513        | 553(C) |                       |        |                                   |        |             |        |
| AD7516        | 557(C) |                       |        |                                   |        |             |        |
| AD7519        | 559(C) |                       |        |                                   |        |             |        |

\*Suffix C Refers to Main Catalog; Suffix S Refers to Supplement.



# **DATA ACQUISITION PRODUCTS CATALOG SUPPLEMENT**

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# Introduction

## USING THIS CATALOG SUPPLEMENT

*This Supplement includes some 70 products introduced subsequent to the publication of our Data Acquisition Products Catalog. If you do not already have the Data Acquisition Catalog (pictured on the front cover of this supplement) call the nearest sales office listed on the back cover.*

*Selection guides on pages 5S to 16S list all of the products described in either the main catalog or in this supplement and thus are comprehensive. Page numbers followed by an S are in this supplement—those followed by C will be found in the main catalog. The contents of both are organized in similar fashion.*

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# Selection Guides





# Operational Amplifiers

**SPECIFICATIONS** (typical at rated supply voltage and load, and  $T_A = 25^\circ\text{C}$ , unless noted otherwise)

| General Purpose IC's   | Offset Voltage<br>mV max  | $\Delta E_{os}/\Delta T \ddagger$<br>$\mu\text{V}/^\circ\text{C}$ max | Bias Current<br>nA max  | Slew Rate<br>V/ $\mu\text{s}$ | Page   |
|--|---|---|---|-------------------------------|--------|
| AD301A/201A/101A <sup>†</sup>  | 7.5/2/2   | 30/15/15  | 250/75/75   | 0.5 to 10*                    | 17(C)  |
| AD741/741C <sup>†</sup> Internal Comp.                               | 5.0/6.0   | No Spec.  | 500   | 0.5                           | 65(C)  |
| FET-Input Low Bias Current IC's and Module                           | Bias Current<br>pA max  | Offset Voltage<br>mV max  | $\Delta E_{os}/\Delta T \ddagger$<br>$\mu\text{V}/^\circ\text{C}$ max | Slew Rate<br>V/ $\mu\text{s}$ |        |
| AD515J/K/L   | 0.3/0.15/0.075  | 3/1/1   | 50/15/25  | 0.3 min                       | 15S    |
| AD545J/K/L/M   | 2/1/1/1   | 1/1/0.5/0.25  | 25/15/5/3   | 0.3 min                       | 41S    |
| 52J/K Module   | 3   | 0.5   | 3/1   | 0.25 min                      | 75(C)  |
| AD506J/K/L/S   | 15/10/5/10  | 3.5/1.5/1/1.5   | 75/25/10/50   | 3.0                           | 21(C)  |
| AD503J/K/S   | 15/10/10  | 50/20/20  | 75/25/50  | 3.0                           | 21(C)  |
| AD528J/K/S   | 30/15/15  | 3/1/1   | 50/25/25  | 50                            | 57(C)  |
| AD542J/K/L/S BIFET   | 50/25/25/25   | 2/1/0.5/1   | 20/10/5/15  | 3.0                           | 33S    |
| AD544J/K/L/S BIFET   | 50/25/25/25   | 2/1/0.5/1   | 20/10/5/15  | 12.0                          | 37S    |
| AD540J/K/S   | 50/25/25  | 50/20/20  | 75/25/50  | 6.0                           | 61(C)  |
| Electrometer IC and Modules  | Bias Current<br>fA max  | Offset Voltage<br>mV max  | $\Delta E_{os}/\Delta T \ddagger$<br>$\mu\text{V}/^\circ\text{C}$ max | Slew Rate<br>V/ms min         |        |
| 310J/K Inverting Module  | 10  | 10  | 30/10   | 0.4                           | 97(C)  |
| 311J/K Noninverting Module   | 10  | 10  | 30/10   | 0.4                           | 97(C)  |
| AD515J/K/L IC Differential   | 300/150/75  | 3/1/1   | 50/15/25  | 300                           | 15S    |
| High Accuracy Low-Drift IC's and Module                              | Offset<br>mV max  | $\Delta E_{os}/\Delta T \ddagger$<br>$\mu\text{V}/^\circ\text{C}$ max | Bias Current<br>nA max  | Slew Rate<br>V/ $\mu\text{s}$ |        |
| AD517J/K/L/S   | 0.150/0.05/0.025/0.05   | 3/1/0.5/1   | 5/2/1/2   | 0.1/0.1                       | 47(C)  |
| AD510J/K/L/S   | 0.1/0.05/0.025/0.05   | 3/1/0.5/1   | 25/13/10/13   | 0.1                           | 37(C)  |
| AD504J/K/L/M/S   | 2.5/1.5/0.5/0.5/0.5   | 5/3/1/0.5/1 nulled  | 200/100/80/80/80  | 0.12 to 2.5*                  | 25(C)  |
| 52J/K Module   | 0.5   | 3/1   | 0.003   | 0.25 min                      | 75(C)  |
| AD301AL <sup>†</sup>   | 0.5   | 5.0   | 30  | 0.5 to 10*                    | 17(C)  |
| AD741J/K/L/S   | 3/2/0.5/2   | 20/15/5/15 untrimmed  | 200/75/50/75  | 0.5                           | 65(C)  |
| High Accuracy Low-Drift Chopper Amplifier Modules                    | Offset<br>$\mu\text{V}$ max   | $\Delta E_{os}/\Delta T \ddagger$<br>$\mu\text{V}/^\circ\text{C}$ max | Bias Current<br>pA max  | Slew Rate<br>V/ $\mu\text{s}$ |        |
| 235J/K/L Inverting   | 25/25/15  | 0.5/0.25/0.1  | 100/50/50   | 0.3                           | 85(C)  |
| 234J/K/L Inverting   | 50/20/20  | 1.0/0.3/0.1   | 100   | 30                            | 81(C)  |
| 261J/K Low-Noise, Non-Inverting                                      | 25  | 0.3/0.1   | 300   | 100V/s                        | 91(C)  |
| 260J/K Low-Cost, Non-Inverting                                       | 25  | 0.3/0.1   | 300   | 100V/s                        | 89(C)  |
| Fast, Wideband IC's and Modules                                      | Settling Time<br>to 0.1%, $\mu\text{s}$   | Slew Rate<br>V/ $\mu\text{s}$ , min                                   | $\Delta E_{os}/\Delta T \ddagger$<br>$\mu\text{V}/^\circ\text{C}$ max | I <sub>BIAS</sub><br>nA max   |        |
| 50J/K Module   | 0.1 (INV, max)  | 500 (INV)   | 50/15   | 2                             | 71(C)  |
| 51A/B <sup>†</sup> Module (-25°C to +85°C)                           | 0.15 (INV, max)<br>0 to +70°C   | 400 (INV)   | 50/20   | 2                             | 71(C)  |
| (-55°C to +100°C Operating)  | 0.25 (INV, 0.05%)<br>-25°C to +85°C   |   |   |                               |        |
| HOS-050/050A <sup>†</sup> TO-8                                       | 0.08 (INV)  | 300 (INV)   | 150/35  | 2                             | 45S    |
| 48J/K Fast Settling Module   | 0.5 (0.01%, max)  | 110 (INV)   | 50/15   | 0.05/0.025                    | 69(C)  |
| AD509J/K/S IC  | 0.2/0.5 max/0.5 max   | 80/80/100   | 20 typ/30/30  | 250/200/200                   | 33(C)  |
| AD518J/K/S IC  | 0.8   | 50  | 10 typ/15/20  | 500/250/250                   | 53(C)  |
| AD528J/K/S FET-Input IC  | 0.8   | 50  | 50/25/25  | 0.03/0.015/0.015              | 57(C)  |
| AD507J/K/S IC  | 0.9   | 20/25/20  | 15 typ/15/20  | 25/15/15                      | 29(C)  |
| High-Output Modules  | max E <sub>out</sub>  | max I <sub>out</sub>  | $\Delta E_{os}/\Delta T \ddagger$<br>$\mu\text{V}/^\circ\text{C}$     | I <sub>BIAS</sub><br>pA max   |        |
| 171J/K   | ±140V   | ±10mA   | 50/15   | 50/20                         | 77(C)  |
| 50J/K  | ±10V  | ±100mA  | 50/15   | 2000                          | 71(C)  |
| 51A/B <sup>†</sup> -25°C to +85°C (Spec.)<br>(-55°C to +100°C Oper.) | ±10V  | ±100mA  | 50/20   | 2000                          | 71(C)  |
| Isolated Op Amp Modules  |   |   |   |                               |        |
| 277J/K/A   | Inverting, non-inverting, differential op-amp applications,<br>Input offset drift 3/1 $\mu\text{V}/^\circ\text{C}$ (nulled), bias current 20nA max,<br>CMR 160dB min at dc, 120dB min at 60Hz, max CMV 3500V rms<br>(60Hz, 1 min), ±2500V peak or dc, continuous, isolated power<br>output, ±15mA @ ±15V. |   |   |                               | 133(C) |

\*Inverting - Actual value depends on compensation.

<sup>†</sup>301A, 301AL, 0 to +70°C; 201A, -25°C to +85°C; 101A, -55°C to +125°C; 741C, 0 to +70°C; 741, -55°C to +125°C; HOS, -55°C to +125°C.

<sup>‡</sup>Temperature range suffixes (e.g. AD504J/K/L/M/S) J/K/L/M, 0 to +70°C; S, -55°C to +125°C; 51A/B, 277A, -25°C to +85°C.

# Instrumentation Amplifiers

|  | 606J/K/L/M<br>Module | AD522A/B/S<br>Hybrid IC          | 610J/K/L<br>Module        | AD521J/K/L/S<br>Monolithic IC            |
|--|----------------------|----------------------------------|---------------------------|--|
| Nominal Gain Range                         | 1 to 10,000V/V       | 1 to 1000                        | 1 to 10,000V/V            | 1 to 1000V/V                             |
| Gain Tempco, ppm/°C                        | ±15 max              | 2 max, G = 1<br>50 max, G = 1000 | ±15 max                   | ±(3 ± 0.05G) (J, K, L)<br>±(15 ± 0.4G) S |
| Nonlinearity, max<br>(G = 100)             | 0.002%               | 0.01%/0.005%/0.005%              | 0.01%                     | 0.2%/0.2%/0.1%/0.2% max                  |
| Offset Tempco RTI, μV/°C                   |                      |                                  |                           |  |
| G = 1                                      | 200/150/100/75 max   | 50/25/100 max                    | 200/150/150               | 400/150/75/150 max                       |
| G = 1000                                   | 2/1/0.5/0.25 max     | 6/2/6 max                        | 3/1/0.5 max               | 15/5/2/5 max                             |
| I <sub>BIAS</sub> , nA max                 | +60                  | ±25/15/25                        | +60                       | 80/40/40/40                              |
| I <sub>BIAS</sub> Tempco                   | -0.2nA/°C            | ±100/50/100pA/°C                 | -0.2nA/°C                 | 1/0.5/0.5/0.5nA/°C max                   |
| I <sub>OS</sub> , nA                       | ±1                   | ±20/10/20 max                    | ±5                        | 20/10/10/10 max                          |
| I <sub>OS</sub> Tempco, pA/°C              | ±20                  | ±100/50/100                      | ±20                       | 250/125/125/125 max                      |
| Noise, RTI, 0.1Hz - 10Hz, μV p-p           |                      |                                  |                           |  |
| G = 1                                      | 40(0.01 - 10Hz)      | 15                               | 50(0.01 - 10Hz)           | 225                                      |
| G = 1000                                   | 1 max (0.01 - 10Hz)  | 1.5                              | 2.5/2/2 max (0.01 - 10Hz) | 0.5                                      |
| CMR at rated CMV                           |                      |                                  |                           |  |
| 1kΩ Unbalance, Frequency:                  | DC to 100Hz          |                                  | DC to 100Hz               | DC to 60Hz                               |
| G = 1, dB min                              | 60                   | 75/80/75                         | 60                        | 70/74/74/74                              |
| G = 10, dB min                             | 80                   | 90/95/90                         | 80                        | 90/94/94/94                              |
| G = 100, dB min                            | 86                   | 100                              | 86                        | 100/104/104/104                          |
| G = 1000, dB min                           | 90                   | 100/110/100                      | 90                        | 100/110/110/110                          |
| Small-Signal Frequency Range               |                      |                                  |                           |  |
| -3dB, typ                                  |                      |                                  |                           |  |
| G = 100                                    | 100kHz               | 3kHz                             | 100kHz                    | 200kHz                                   |
| Settling Time to 0.1%,<br>±10V Output Step |                      |                                  |                           |  |
| G = 100                                    | 30μs                 | 5ms                              | 30μs                      | 10μs                                     |
| Temperature Ranges†                        | C                    | I/I/M                            | C                         | C/C/C/M                                  |
| Page                                       | 117(C)               | 113(C)                           | 121(C)                    | 47S                                      |

\*G = 1 to 1000, DC to 60Hz: 75/80/75dB for A/B/S  
†C: 0 to +70°C, I: -25°C to +85°C, M: -55°C to +125°C.

# Isolation Amplifiers

| APPLICATION                                    | PRIMARY CONSIDERATIONS  | FEATURES  | RECOMMENDED MODEL                            | PAGE             |
|--|---|---|--|------------------|
| Industrial and Medical Instrumentation         | Lowest Cost<br>High Performance<br>Patient Safety<br>High CMR, CMV          | ±0.05% Nonlinearity, ±75ppm/°C Gain Drift<br>2.0μA rms max leakage; Defibrillator Protection<br>Floating Power Supply: ±8.5V dc @ ±5mA min<br>110dB min CMR @ 60Hz; ±5kV pk CMV (Pulse)                       | 284J   | 137(C)<br>Note 1 |
| Industrial and Medical Instrumentation         | Multi-Channel<br>Reliability<br>High CMV, CMR<br>Isolated Supply            | External Synchronization; 100kHz Osc — model 281<br>Meets IEEE SWC Standard and UL 544 Leakage Std<br>5kV pk pulse differential and Input/Output CMV<br>110dB min CMR @ 60Hz; ±15V dc @ ±15mA Isolated Supply | 286J<br>281 (Osc)                            | 147(C)           |
| Industrial Instrumentation and Control Systems | Multi-Channel<br>High Accuracy<br>Low Cost<br>Smallest Size                 | External Synchronization; model 947 or 948 driver<br>0.05% max nonlinearity, 100ppm/°C max gain drift,<br>5μV/°C max input drift, Adjust. Gain, 1 to 1000V/V,<br>850V dc diff and in/out CMV, 1" x 1" x 0.56" | 288J<br>288K<br>947 (Driver)<br>948 (Driver) | 53S              |
| Industrial Instrumentation and Control Systems | Highest Accuracy<br>Versatility<br>High CMV/CMR<br>Isolated Supply          | 0.025% max nonlinearity, 1μV/°C max input drift,<br>Uncommitted High Performance Op Amp Front-End<br>160dB min CMR @ dc; 3.5kV rms CMV (1 min)<br>Floating Power Supply: ±15V dc @ ±15mA min                  | 277J<br>277K<br>277A                         | 133(C)           |
| Industrial Instrumentation and Control Systems | High Accuracy<br>Wide Input/Output Range<br>High CMV/CMR<br>Floating Output | 0.05% max nonlinearity, 5μV/°C max input drift,<br>±10V Input/Output Range; 2.5kV dc CMV (Continuous),<br>120dB min CMR @ 60Hz, Fully Guarded Inputs<br>3-Port Isolation; 200V dc CMV Outputs to Pwr Com      | 275J<br>275K<br>275L                         | 129(C)           |
| Industrial Instrumentation and Control Systems | High Accuracy<br>Low Impedance Output<br>High CMV/CMR                       | 0.03% max nonlinearity, 5μV/°C max input drift<br>±10V min Input/Output Range; ±5mA Output<br>Adjustable Gain, 1 to 1000V/V, 3000V rms 60Hz<br>Input/Output Isolation (1 min), 115dB CMR @ 60Hz               | 285J<br>285K<br>285L                         | 143(C)           |

<sup>1</sup> Product improved; new data sheet.



# Multipliers and Dividers

| Type                         | Characteristics   | Page   |
|------------------------------|---|--------|
| AD532J/K/S                   | General-purpose 4-quadrant IC, differential inputs, standard pinouts, pretrimmed to 1.0% max total error (K), 0.04%/°C max (S)  | 169(C) |
| AD533J/K/L/S                 | Lowest cost general-purpose 4-quadrant IC, external trim to 0.5% max total error (L)  | 175(C) |
| Model 435J/K                 | Highest-accuracy 4-quadrant, module, pretrimmed to 0.1% max total error (K), 0.01%/°C max (K)   | 199(C) |
| Model 429A/B†                | Widest-bandwidth 4-quadrant, module, full-power response to 2MHz min, slewing rate 120V/μs min, -3dB bandwidth 10MHz, small-signal, 1% settling-time 500ns; pretrimmed to 0.5% max error (B)  | 187(C) |
| AD534J/K/L/S/T               | High-accuracy internally-trimmed 4-quadrant IC multiplier featuring 0.25% max total error (L), low noise (90μV rms, 10Hz - 10kHz), and versatile differential input configuration.  | 179(C) |
| <b>DIVIDER</b>               |   |        |
| Model 436A/B                 | High-accuracy 2-quadrant divider-only module, pretrimmed to 0.25% max error (B, denominator $[V_x]$ range from +0.1V to +10V [ $ V_z  \leq  V_x $ ]), 2% max error over temperature (B), 1% max error 0 to +70°C                          | 203(C) |
| AD535J/K                     | IC 2-quadrant divider, pretrimmed for 0.5% max total error (K version) for 10:1 denominator range. Differential inputs permit choice of denominator range. Differential inputs permit choice of denominator polarity.                     | 59S    |
| <b>MULTIFUNCTION DEVICES</b> |   |        |
| Model 433J/B                 | Programmable multifunction module, $Y(Z/X)^m$ (10V/ $E_{REF}$ ), one-quadrant, m adjustable from 0.2 to 5, max division error 25mV (B, $V_z$ from 0.01V to 10V, $V_x$ from 0.1V to 10V, $V_z \leq V_x$ ), 1% max over temperature         | 191(C) |
| Model 434A/B                 | High-accuracy multifunction module, $YZ/X$ , one-quadrant, max division error pretrimmed to 0.25% max (B, $V_z$ from 0.01V to 10V, $V_x$ from 0.1V to 10V, $V_z \leq V_x$ , m = 1), 1% max over temperature (B), current or voltage input | 195(C) |
| AD531J/K/L/S                 | 4-quadrant XY/Iz IC multiplier with variable or programmable denominator (scale factor), can be externally trimmed to 0.5% max total error (L)  | 161(C) |

†Rated operating temperature ranges: J/K/L, 0 to +70°C; A/B, -25°C to +85°C; S/T, -55°C to +125°C

# Logarithmic Amplifiers

| MODEL                                    | CHARACTERISTICS  | PAGE   |
|--|--|--------|
| Model 755N/P<br>Log-antilog<br>amplifier | High performance: ±1% max log-conformity error for 6 decades of current (1nA to 1mA) and 4 decades of voltage (1mV to 10V), and 0.5% max conformity error for 4 decades of current (10nA to 100μA) and 3 decades of voltage (1mV to 1V), 1.5" x 1.5" x 0.4" module. Antilog output range: 4 decades, 1mV to 10V, K = 1, 2, 2/3 V/decade, $I_{ref} = 10\mu A$ (externally adjustable).  | 213(C) |
| Model 759N/P<br>Log-antilog<br>amplifier | Small size and low cost: 1.13" x 1.13" x 0.4" module, wide bandwidth 200kHz @ 1μA, ±2% max log-conformity error for 5 decades of current (10nA to 1mA) or 4 decades of voltage (1.0mV to 10V), and ±1% max conformity error for 4 decades of current (20nA to 200μA). Log operating range: 6 decades of current (1nA to 1mA) and 4 decades of voltage (1mV to 10V). Antilog output range: 4 decades (1mV to 10V), K = 1, 2, 2/3 V/decade, $I_{ref} = 10\mu A$ (externally adjustable). | 221(C) |
| Model 757N/P<br>Log-ratio<br>module      | Input dynamic range, 6 decades of current (1nA to 1mA), either channel, log conformity error ±1.0% max; for 4 decades (10nA to 100μA), log conformity error ±0.5% max. Log of voltage by using external resistors. K = 1 V/decade, ±1%, max, or externally programmable. Can be used for antilog operations.   | 217(C) |

**NOTE:**

The Complete log devices listed above and catalogued in this section are recommended for new designs. Model 752 log transconductor and model 751 basic log element, popular early devices for assembly in log circuits by the user, are still available. Data sheets will be provided upon request.

# RMS Converters

| MODEL        | CHARACTERISTICS  | PAGE   |
|--------------|--|--------|
| 442J/K/L†    | Wideband, low-drift, high-crest-factor module. Preadjusted for total max error $\pm 2\text{mV} \pm 0.15\%$ of reading, for sine waves, frequencies to 20kHz (100kHz typical), 0 to 2V rms input. User-trimmable to $\pm 0.5\text{mV} \pm 0.05\%$ , 10mV to 2V. Crest factor of 7 for 0.2% additional reading error. Bandwidth for 1% (rdg.) error 700kHz, and for -3dB 8MHz, for 2V rms signals. Averaging time-constant $1.5\text{ms} + C_{\text{ext}} \cdot 15\text{ms}/\mu\text{F}$ . Total-error max tempco ( $\pm 35\mu\text{V} \pm 0.01\%$ rdg.)/ $^{\circ}\text{C}$ (442L).                           | 235(C) |
| AD536AJ/K/S† | Monolithic IC rms/dB converter. Laser-wafer-trimmed for total max error $\pm 2\text{mV} \pm 0.2\%$ of reading (AD536K), sine waves at 1kHz (20kHz typ), 0 to 7V rms. Crest factor of 7 for 1% additional error. $\pm 3\text{dB}$ bandwidth 2MHz ( $1\text{V} < V_{\text{IN}} \leq 7\text{V}$ ). Averaging time constant per $\mu\text{F}$ of $C_{\text{ext}}$ , $25\text{ms}/\mu\text{F}$ . Total-error tempco ( $\pm 50\mu\text{V} \pm 0.005\%$ rdg.)/ $^{\circ}\text{C}$ max (K). Additional features include dB output with 60dB range, single-or dual-supply operation, and low power consumption - 1mA. | 65S    |

## NOTE:

The devices listed above and catalogued here are recommended for new designs. Models 440 and 441 are popular earlier models that are still available. Data sheets will be provided upon request.

†Rated operating temperature ranges: J/K/L, 0 to  $+70^{\circ}\text{C}$ ; S,  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

# Voltage References

|                    | MODEL              | CHARACTERISTIC  | PAGE   |
|--------------------|--------------------|---|--------|
| VOLTAGE REFERENCES | AD580J/K/L/M/S/T/U | Monolithic 3-terminal 2.5V @ 10mA reference. Output voltage to within $\pm 1\%$ (M, U), less than 10mV line regulation (4.5V to 30V), 10mV max load regulation (10mA change), and 10ppm/ $^{\circ}\text{C}$ change with temperature (M, U).   | 241(C) |
|                    | AD581J/K/L/S/T/U   | Monolithic 3-terminal laser-trimmed 10.000V $\pm 5\text{mV}$ @ 10mA voltage reference. Tempcos trimmed to within 5ppm/ $^{\circ}\text{C}$ max (0 to $+70^{\circ}\text{C}$ - L), and 10ppm/ $^{\circ}\text{C}$ max ( $-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ - U). Can be used in 2-terminal connection as high-performance "Zener diode" for positive or negative reference voltage.  | 71S    |
|                    | AD584J/K/L/S/T/U   | Monolithic, laser-trimmed to provide four programmable values of output voltage: 10.000V, 7.500V, 5.000V, 2.500V, with max error of $\pm 5\text{mV}$ , $\pm 4\text{mV}$ , $\pm 3\text{mV}$ , $\pm 2.5\text{mV}$ (L version) and max tempco of 5ppm/ $^{\circ}\text{C}$ (L version on 10V, 7.5V, 5V ranges). Other values of voltage available by connection of external resistors. Can be used in 2-terminal connection as high-performance "Zener diode" for negative reference ( $>  5\text{V} $ ) or as a current limiter. | 77S    |
|                    | AD2700J/L/S        | Hybrid high-accuracy $+10\text{V} \pm 2.5\text{mV}$ (L, U) @ 10mA, 3ppm/ $^{\circ}\text{C}$ (L, S, U)   | 265(C) |
|                    | AD2701J/L/S        | Hybrid high-accuracy $-10\text{V} \pm 2.5\text{mV}$ (L, U) @ 10mA, 3ppm/ $^{\circ}\text{C}$ (L, S, U)   | 265(C) |
|                    | AD2702J/L/S        | Hybrid high-accuracy dual $\pm 10\text{V} \pm 2.5\text{mV}$ (L, U) @ 10mA, 3ppm/ $^{\circ}\text{C}$ (U)   | 265(C) |

# Transducers, Conditioners, and Instrumentation

|                         |        |  | Page |
|-------------------------|--------|--|------|
| Temperature Transducers | AD590  | IC, 2-terminal, TO-52 can or miniature flatpack, $-5^{\circ}\text{C}$ to $+150^{\circ}\text{C}$ (218K to 423K) operating range, linear current output, $1\mu\text{A}/\text{K}$ , laser-trimmed for high accuracy.  | 85S  |
|                         | AC2626 | Stainless-steel temperature probe using AD590, same temperature range and electrical characteristics as the AD590, $3/16''$ outside diameter, $6''$ or $4''$ standard lengths, includes $3'$ of Teflon-coated lead wire, 2s response in stirred water, sensor electrically isolated from sheath ( $\pm 200\text{V}$ breakdown – case to leads).                      | 83S  |
| Signal Conditioners     | 2B31   | Module; complete signal conditioning function at low cost for bridge transducers, such as strain gages and RTD's; provides programmable excitation, amplification, and 3-pole low pass filter; CMR is 140dB min (60Hz, $G = 1000$ ); low offset drift $\pm 0.5\mu\text{V}/^{\circ}\text{C}$ max; nonlinearity $\pm 0.0025\%$ max.                                    | 101S |
|                         | 2B30   | Modular conditioner with same performance as 2B31, but without transducer excitation supply.   | 101S |
|                         | 2B20   | Modular voltage to current converter; provides 4-20mA output current for 0 to +10V input; low drift and nonlinearity, single supply operation.   | 93S  |
|                         | 2B22   | Modular isolated voltage to current converter; 4-20mA output; 1500V dc input to output isolation; internal isolated loop power supply.   | 91S  |
|                         | 2B35   | Module; precision triple-output transducer power supply; provides $\pm 15\text{V}$ amplifier power and programmable excitation output: voltage (+1V to +15V dc) or current ( $100\mu\text{A}$ to 10mA); provides excitation for transducers and signal conditioners.   | 107S |
| Instrumentation         | AD2040 | 3 digit low cost temperature indicator for use with AD590 or AC2626 temperature transducers; accurate to $\pm 1^{\circ} \pm 1$ digit; user programmable to readout in Celsius, Kelvin, Fahrenheit or Rankine; single +5V power supply, terminal block interface small size, panel mount.   | 111S |
|                         | AD2038 | 6 Channel Scanning Digital Thermometer for use with the AD590 and AC2626 temperature transducers; provides automatic, manual or logic controlled scan of the 6 inputs, high accuracy, $0.1^{\circ}$ resolution; has isolated analog input parallel BCD output, analog output; line powered.  | 109S |
|                         | AD2036 | 6 Channel Scanning Digital Thermometer for use with J, K or T type thermocouples; provides automatic, manual or logic controlled scan, self-contained cold-junction compensation and linearization; $^{\circ}\text{C}$ or $^{\circ}\text{F}$ readout; has isolated analog input, parallel BCD output, analog output; either line powered, +5V dc or +12V dc powered. | 259S |
|                         | AD2037 | 6 Channel $3\ 1/2$ digit scanning voltmeter with differential inputs and full scale programmability from $\pm 200\text{mV}$ to 6V; designed to interface printers, computers, transmitters, etc. for display, control logging etc.; has isolated analog input, parallel BCD output, analog output; line powered.   | 109S |



# D/A Converters

| Description               | Model §              | Resolution (Bits)   | Other   | See Page       |
|---------------------------|----------------------|---|---|----------------|
| General Purpose           | AD7523               | 8   | CMOS IC, 4-quadrant multiplying, lowest cost  | 313(C)         |
|                           | AD1408               | 8   | IC, replaces Motorola 1408/1508 directly  | 295(C)         |
|                           | AD559                | 8   | IC, high-performance alternative to Motorola 1408/1508  | 277(C)         |
|                           | AD7524               | 8   | CMOS IC, 4-quadrant multiplying, with $\mu$ P interface   | 317(C)         |
|                           | AD DAC-08            | 8   | IC, direct replacement for industry-standard DAC-08 85ns settling time, $\pm 1/4$ LSB guaranteed linearity over temperature   | 143S           |
|                           | AD7533               | 10  | CMOS IC, 4-quadrant multiplying, low cost   | 327(C)         |
|                           | AD7530               | 10  | CMOS IC, 4-quadrant multiplying   | 323(C)         |
|                           | AD561                | 10  | IC, internal reference, 250ns current settling  | 281(C)         |
|                           | DAC-10Z              | 10  | Module, voltage output 5 $\mu$ s settling to 0.05%  | 377(C)         |
|                           | MDA-10Z              | 10  | Module, 300ns settling to 0.05% current output  | 377(C)         |
|                           | AD7531               | 12  | CMOS IC, 4-quadrant multiplying, low cost   | 323(C)         |
|                           | AD DAC80             | 12  | IC, 3-chip improved replacement for standard DAC80, I and V versions  | 147S           |
|                           | AD DAC85             | 12  | IC, improved replacement for standard DAC85 over $-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$                              | 155S           |
|                           | AD DAC87             | 12  | IC, improved replacement for standard DAC87, monotonic over $-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ temperature range | 163S           |
|                           | DAC1009              | 12  | Module, voltage output, BCD optional  | 339(C)         |
|                           | DAC-12QZ             | 12  | Module, voltage output, complementary coding, BCD optional, 5 $\mu$ s settling  | 375(C)         |
|                           | DAC1118              | 12  | Module, voltage output, BCD optional  | 347(C)         |
| High Performance          | AD7541               | 12  | CMOS IC, 4-quadrant multiplying, pretrimmed   | 333(C)         |
|                           | AD566                | 12  | IC, monolithic replacement for AD562, current settling time 200ns   | 129S           |
|                           | AD562                | 12  | IC, current output, settling time 1.5 $\mu$ s   | 289(C)         |
|                           | AD565                | 12  | IC, monolithic replacement for AD563, current settling time 200ns   | 121S           |
|                           | AD563                | 12  | IC, current output, internal reference  | 289(C)         |
|                           | DAC-QS               | 12, 10, 8   | Module, voltage output, BCD optional  | 373(C)         |
|                           | DAC-QM               | 12, 10, 8   | Module, voltage output, BCD optional with input registers   | 367, 373(C)    |
|                           | DAC1132              | 12  | Module, voltage output, 2 $\mu$ s settling to 0.01%   | 353(C)         |
| DAC1422                   | 10                   | Module, 4-20mA current output, buffered digital input, powered from single ended +12V to +36V loop supply | 177S  |                |
| High Speed                | AD561                | 10  | IC, 250ns current settling, internal reference  | 113S           |
|                           | HDS                  | 12, 10, 8   | 24-pin DIP, 30/25/20ns current settling to 0.025%/0.1%/0.4%   | 179S           |
|                           | DAC1106/08           | 10, 8   | Module, 50/25ns current settling to 0.05%/0.02%   | 343(C)         |
|                           | MDSL                 | 12, 10, 8   | Module, 50/25/25ns current settling to 0.025%/0.1%/0.1%   | 191S           |
|                           | MDS                  | 12, 10, 8   | Module, TTL/ECL input, 40/20/15ns current settling to 0.025%/0.1%/0.4%  | 191S           |
|                           | MDD                  | 10, 8   | Module, deglitched, voltage output, 20MHz word rate   | 185S           |
|                           | DAC-10DF             | 10  | Module, deglitched, voltage output, 200ns max settling to $\pm 0.05\%$  | 365(C)         |
|                           | MDH                  | 12, 10, 8   | Module, 200/100/70ns voltage settling to 0.025%/0.1%/0.4%   | 191S           |
|                           | HDH                  | 12, 10, 8   | 24-pin DIP, 500/300/200ns voltage settling to 0.025%/0.1%/0.4%  | 179S           |
|                           | AD565                | 12  | IC, monolithic replacement for AD563, current settling time 200ns   | 121S           |
|                           | AD566                | 12  | IC, monolithic replacement for AD562, current settling time 200ns   | 129S           |
| High Resolution           | DAC-QM               | 16, 14  | Module, voltage output, BCD optional  | 367(C), 373(C) |
|                           | DAC1136 <sup>1</sup> | 16  | Module, voltage output, 18 $\mu$ s settling to $\pm 0.0015\%$   | 167S           |
|                           | DAC1137 <sup>1</sup> | 18  | Module, voltage output  | 167S           |
|                           | DAC1138 <sup>1</sup> | 18  | Module, voltage output 60 $\mu$ s settling to $\pm 0.00038\%$   | 167S           |
| Low Power † & Multiplying | AD7523               | 8   | CMOS IC, 4-quadrant multiplying, low cost   | 313(C)         |
|                           | AD7524               | 8   | CMOS IC, 4-quadrant multiplying, $\mu$ P-compatible   | 317(C)         |
|                           | AD7533               | 10  | CMOS IC, 4-quadrant multiplying, low cost   | 327(C)         |
|                           | AD7530               | 10  | CMOS IC, 4-quadrant multiplying   | 323(C)         |
|                           | AD7520               | 10  | CMOS IC, 4-quadrant multiplying   | 299(C)         |
|                           | AD7522               | 10  | CMOS IC, 4-quadrant multiplying, double-buffered serial-parallel, with $\mu$ P interface                                      | 307(C)         |
|                           | MDMS                 | 11, 10, 8   | Module, multiplying, 100ns current settling to $\pm 0.1\%$  | 189S           |
|                           | AD7525               | 3 1/2 BCD   | CMOS IC, multiplying (2-quadrant analog) "digital pot"  | 137S           |
|                           | AD7531               | 12  | CMOS IC, 4-quadrant multiplying, low cost   | 323(C)         |
|                           | AD7541               | 12  | CMOS IC, 4-quadrant multiplying, pretrimmed   | 333(C)         |
|                           | AD7521               | 12  | CMOS IC, 4-quadrant multiplying   | 299(C)         |
|                           | DAC1125              | 12  | Module, 4-quadrant, voltage out, low feedthrough 8.5mW power drain  | 349(C)         |

† All CMOS IC's are low power.

§ The products cataloged in this volume are those considered to be the most cost-effective for new designs.

A number of popular older products are still available; they are listed on pages 335S and 336S.

Data sheets are available upon request.

<sup>1</sup> Deglitcher, model Deglitcher IV, available; see data sheet.

# A/D Converters

| Description      | Model §                 | Resolution (Bits)                      | Other  | See Page |
|------------------|-------------------------|--|--|----------|
| General Purpose  | AD570                   | 8                                      | Monolithic IC, complete, pretrimmed, 3-state output  | 119S     |
|                  | AD7570                  | 10, 8                                  | CMOS IC, no missing codes, ratiometric, $\mu$ P-compatible                                   | 419(C)   |
|                  | AD571                   | 10                                     | Monolithic IC, I <sup>2</sup> L, complete including reference, pretrimmed                    | 207S     |
|                  | ADC-12QZ                | 12, 10                                 | Module, 40 $\mu$ s max conversion time, BCD optional   | 467(C)   |
|                  | AD ADC-80               | 12                                     | IC, complete, improved replacement for standard ADC 80                                       | 223S     |
| High Performance | AD574                   | 12                                     | IC, complete, 2-chip, microprocessor interface, 25 $\mu$ s conversion time                   | 215S     |
|                  | AD572                   | 12                                     | Hybrid IC, 25 $\mu$ s max conversion time, no missing codes over temperature                 | 395(C)   |
|                  | ADC1133                 | 12                                     | Module, 25 $\mu$ s max conversion time   | 457(C)   |
|                  | ADC1131                 | 14                                     | Module, 12 $\mu$ s max conversion time   | 453(C)   |
|                  | ADC1130                 | 14                                     | Module, 25 $\mu$ s max conversion time   | 453(C)   |
| ADC1100          | 11, 3 $\frac{1}{2}$ BCD | Module                                 | 431(C)   |          |
| Integrating      | AD7550                  | 13                                     | CMOS IC, 1ppm/ $^{\circ}$ C gain and offset TC, quad slope                                   | 411(C)   |
|                  | ADC141                  | 14                                     | Module, 5ppm/ $^{\circ}$ C gain TC   | 459(C)   |
|                  | ADC-17I                 | 4 $\frac{1}{2}$ BCD                    | Module, 5ppm/ $^{\circ}$ C gain TC   | 459(C)   |
|                  | ADC1105                 | 4 $\frac{1}{2}$ , 3 $\frac{1}{2}$ BCD  | Module, gated pulse-train output   | 441(C)   |
| Display          | AD2020                  | 3 Digit                                | IC, I <sup>2</sup> L dual-slope DPM chip   | 403(C)   |
|                  | AD2023                  | 3 Digit                                | DPM module for separate display  | 407(C)   |
| High Speed       | MATV-0820               | 8                                      | Module, 20MHz word rate, includes track-and-hold (30ps aperture)                             | 241S     |
|                  | MOD-1005                | 10                                     | Module, 5MHz word rate, includes track-and-hold (25ps aperture) 20MHz analog input bandwidth | 247S     |
|                  | ADC1109                 | 10                                     | Module, 4 $\mu$ s max conversion time  | 447(C)   |
|                  | ADC1103                 | 12, 10, 8                              | Module, 3.5/1.5/1.0 $\mu$ s max conversion time  | 437(C)   |
|                  | HAS                     | 12, 10, 8                              | 32-pin DIP, 2.8/1.7/1.5 $\mu$ s conversion time, no missing codes over temperature           | 232S     |
|                  | MAS                     | 12, 10, 8                              | Module, 2/1.5/1 $\mu$ s max conversion time, parallel and serial outputs                     | 235S     |
|                  | ADC1102                 | 12                                     | Module, 8 $\mu$ s max conversion time  | 435(C)   |
| ADC1131          | 14                      | Module, 12 $\mu$ s max conversion time | 453(C)   |          |
| High Resolution  | ADC1130/31              | 14                                     | Module, 25/12 $\mu$ s conversion time  | 453(C)   |
|                  | ADC-16Q                 | 16                                     | Module   | 463(C)   |
| Low Power        | AD7570                  | 10                                     | CMOS IC, no missing codes, ratiometric, $\mu$ P-compatible                                   | 419(C)   |
|                  | ADC1121                 | 12                                     | Module, CMOS logic, low power drain: 6 $\mu$ J/conversion, 300 $\mu$ W standby               | 449(C)   |
|                  | AD7550                  | 13                                     | CMOS IC, 1ppm/ $^{\circ}$ C gain and offset TC, quad-slope                                   | 411(C)   |

§ The products cataloged in this volume are those considered to be the most cost-effective for new designs. A number of popular older products are still available; they are listed on pages 335S and 336S. Data sheets are available upon request.

## V/F Converters

| Max F.S. Frequency | Model | Other  | See Page |
|--------------------|-------|--|----------|
| 10kHz              | 450   | Module, 0.005% max nonlinearity, max tempcos: offset – $20\mu\text{V}/^\circ\text{C}$ : gain – $25\text{ppm}/^\circ\text{C}$             | 481(C)   |
| 10kHz              | 456   | Module, 0.02% max nonlinearity, max tempcos: offset – $100\mu\text{V}/^\circ\text{C}$ : gain – $80\text{ppm}/^\circ\text{C}$             | 481(C)   |
| 20kHz              | 454   | Module, 0.005% max nonlinearity, max tempcos: offset – $20\mu\text{V}/^\circ\text{C}$ : gain – $25\text{ppm}/^\circ\text{C}$             | 481(C)   |
| 100kHz             | AD537 | IC, 0.07% max nonlinearity, low power, max tempcos: offset – $1\mu\text{V}/^\circ\text{C}$ (K): gain – $50\text{ppm}/^\circ\text{C}$ (K) | 251S     |
| 100kHz             | 452   | Module, 0.015% nonlinearity, max tempcos: offset – $30\mu\text{V}/^\circ\text{C}$ : gain – $50\text{ppm}/^\circ\text{C}$                 | 491(C)   |
| 100kHz             | 458   | Module, 0.01% nonlinearity, max tempcos: offset – $30\mu\text{V}/^\circ\text{C}$ : gain – $5\text{ppm}/^\circ\text{C}$                   | 495(C)   |
| 1MHz               | 460   | Module, 0.015% nonlinearity, max tempcos: offset – $30\mu\text{V}/^\circ\text{C}$ : gain – $15\text{ppm}/^\circ\text{C}$                 | 495(C)   |

## F/V Converters

| Max F.S. Frequency     | Model | Other  | See Page |
|------------------------|-------|--|----------|
| 100Hz–20kHz Adjustable | 451   | Module, 0.008% max nonlinearity, 30ms to full scale, max gain tempco – $50\text{ppm}/^\circ\text{C}$ | 485(C)   |
| 1kHz–200kHz Adjustable | 453   | Module, 0.008% max nonlinearity, 4ms to full scale, max gain tempco – $50\text{ppm}/^\circ\text{C}$  | 485(C)   |

## S/D and D/S Converters

| Model                    | Description   | Page |
|--------------------------|---|------|
| BDM 1615/1616/1617       | Binary-to-BCD Modulo $360^\circ$ Converters                     | 259S |
| DSC1705/1706             | Digital-to-Synchro Converters (12 or 14 Bits)                   | 261S |
| DTM1716/1717             | Digital Vector Generator  | 265S |
| SAC1763                  | Synchro-to-Linear dc Converter                                  | 269S |
| SBCD 1752/1753/1756/1757 | BCD Synchro-to-Digital Converters                               | 271S |
| SCM 1677                 | Digital-Angle-to-Digital Sine/Cosine Converter                  | 275S |
| SDC1700/1702/1704        | Synchro-to-Digital Converters (Low Profile, 10, 12 and 14 Bits) | 277S |
| SDC1725/1726             | Synchro-to-Digital Converters with 3-State Latched Outputs      | 283S |
| SPA1695                  | Synchro/Resolver Power Amplifier                                | 287S |
| TSL 1612                 | Processors for 2-Speed Synchro-to-Digital Conversion            | 289S |

# Sample-Hold Amplifiers

| Description     | Model    | Acquisition Time              | Other   | See Page |
|-----------------|----------|-------------------------------|---|----------|
| General Purpose | AD583    | 4 $\mu$ s to $\pm$ 0.1%       | IC, aperture time 50ns  | 513(C)   |
|                 | AD582    | 6 $\mu$ s to $\pm$ 0.1%       | IC, aperture time 150ns   | 509(C)   |
|                 | SHA1134  | 3.4 $\mu$ s to $\pm$ 0.01%    | Module, aperture jitter 5ns max   | 529(C)   |
|                 | SHA-1A   | 5 $\mu$ s to $\pm$ 0.01%      | Module, aperture jitter 5ns max   | 517(C)   |
|                 | SHA-5    | 15 $\mu$ s to $\pm$ 0.01%     | Module, aperture jitter 4ns   | 523(C)   |
| High Speed      | HTS-0025 | 20ns to 1%                    | DIP package, aperture jitter 20ps   | 293S     |
|                 | HTC-0300 | 100ns to 0.1%                 | DIP package, aperture jitter 100ps max  | 293S     |
|                 | THS-0025 | 25ns to 0.1%                  | Module, aperture jitter 20ps max  | 305S     |
|                 | THC-0300 | 100ns to 0.1%                 | Module, aperture jitter 100ps max   | 305S     |
|                 | SHA-2A   | 500ns to 0.01%                | Module, aperture jitter 250ps   | 519(C)   |
| Low Droop       | SHA-4    | 20 $\mu$ s to $\pm$ 0.01%     | Module, aperture jitter 5ns, 10 $\mu$ V/ms droop, settling time 20 $\mu$ s to $\pm$ 1mV, sample-to-hold | 523(C)   |
|                 | SHA-3    | 75 $\mu$ s to $\pm$ 0.01%     | Module, aperture jitter 5ns, 10 $\mu$ V/ms droop, setting time 100 $\mu$ s to $\pm$ 1mV, sample-to-hold | 523(C)   |
| High Resolution | SHA1144  | 8 $\mu$ s max to $\pm$ 0.003% | Module, aperture jitter 0.5ns, use with ADC1130/1131  | 299S     |
|                 | SHA-6    | 5ms to $\pm$ 0.00075%         | Module, use with ADC-16Q  | 525(C)   |

# Switches and Multiplexers

| Description          | Model    | Diagram   | See Page |
|----------------------|----------|---|----------|
| CMOS IC Switches     | AD7510DI | Dielectrically isolated Quad SPST; Address high closes switch | 545(C)   |
|                      | AD7511DI | Dielectrically isolated Quad SPST; Address low closes switch  | 545(C)   |
|                      | ADG201   | Dielectrically isolated Quad SPST, replace DG201              | 313S     |
|                      | ADG200   | Dielectrically isolated Dual SPST, replace DG200              | 309S     |
|                      | AD7512DI | Dielectrically isolated Quad SPDT                             | 545(C)   |
|                      | AD7516   | Quad SPST replaces CD4016A/4066A                              | 557(C)   |
|                      | AD7513   | Dual SPST   | 553(C)   |
|                      | AD7519   | Quad SPDT current-steering switch                             | 559(C)   |
| CMOS IC Multiplexers | AD7501   | 8-channel multiplexer, High enables                           | 537(C)   |
|                      | AD7503   | 8-channel multiplexer, Low enables                            | 537(C)   |
|                      | AD7502   | 4-channel differential multiplexer                            | 537(C)   |
|                      | AD7506   | 16-channel multiplexer  | 541(C)   |
|                      | AD7507   | 8-channel differential multiplexer                            | 541(C)   |
| Modular Multiplexer  | MPX-8A   | 8-channel, expandable to 64                                   | 561(C)   |

# Data Acquisition Subsystems

| Type                        | Model      | Description  | Page   |
|-----------------------------|------------|--|--------|
| Data Acquisition Subsystem* | AD363      | General-purpose 12-bit data-acquisition subsystem, with 30kHz throughput rate, in two 32-pin metal DIP packages. The analog input package accepts up to 16 single-ended or 8 differential channels, in combinations selected by a switchable mode control, and provides multiplexing, differential amplification, and sample-hold. The second package is a high-accuracy 12-bit successive-approximation A/D converter with parallel and serial output and a free unity-gain analog buffer. The packages are connected externally by an analog signal line and a digital control line. | 317S   |
|                             | DAS1128    | General-purpose 12-bit data-acquisition module. Accepts 8 differential or 16-single-ended inputs, performs multiplexing, sample-hold, and A/D conversion, with maximum throughput rate of 35kHz. Can be readily interfaced with microcomputer systems, via 8255 or PIA.  | 565(C) |
|                             | DAS1150/51 | General-purpose single-channel 12-bit data-acquisition modules with 25kHz throughput rate. Contain differential-input amplifier, sample-hold, and 12-bit successive-approximation A/D converter. DAS1150's amplifier has resistor-programmable gain from 1 to 1000; DAS1151's amplifier is software-programmable for gains of 1, 2, 4, 8.  | 329S   |

\*See also SHA1144 data sheet (page 299S) for AC1580 utility card for assembling 14-bit data-acquisition subsystems.





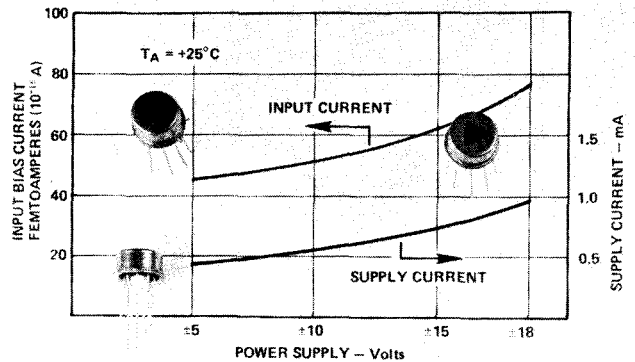
# Product Descriptions





## FEATURES

- Ultra Low Bias Current: 0.075pA max (AD515L)  
0.150pA max (AD515K)  
0.300pA max (AD515J)
- Low Power: 1.5mA max Quiescent Current  
(0.8mA typ)
- Low Offset Voltage: 1.0mV max (AD515 K & L)
- Low Drift: 15 $\mu$ V/ $^{\circ}$ C max (AD515K)
- Low Noise: 4 $\mu$ V p-p, 0.1 to 10Hz
- Low Cost



## PRODUCT DESCRIPTION

The AD515 series of FET-input operational amplifiers are second generation electrometer designs offering the lowest input bias currents available in any standard operational amplifier. The AD515 also delivers laser-trimmed offset voltage, low drift, low noise and low power, a combination of features not previously available in ultra-low bias current circuits. All devices are internally compensated, free of latch-up, and short circuit protected.

The AD515 delivers a new level of versatility and precision to a wide variety of electrometer and very high impedance buffer measurement situations, including photo-current detection, vacuum ion-gauge measurement, long term precision integration, and low drift sample/hold applications. The device is also an excellent choice for all forms of biomedical instrumentation such as pH/plon sensitive electrodes, very low current oxygen sensors, and high impedance biological microprobes. In addition, the low cost and pin compatibility of the AD515 with standard FET op amps will allow designers to upgrade the performance of present systems at little or no additional cost. The 10<sup>15</sup> ohm common mode input impedance, resulting from a solid bootstrap input stage, insures that the input bias current is essentially independent of common mode voltage.

As with previous electrometer amplifier designs from Analog Devices, the case is brought out to its own connection (pin 8) so that the case can be independently connected to a point at the same potential as the input, thus minimizing stray leakage to the case. This feature will also shield the input circuitry from external noise and supply transients, as well as reducing common mode input capacitance from 0.8pF to 0.2pF.

The AD515 is available in three versions of bias current and offset voltage, the "J", "K", and "L"; all are specified for rated performance from 0 to +70 $^{\circ}$ C and supplied in a hermetically sealed TO-99 package.

## PRODUCT HIGHLIGHTS

- The AD515 provides the lowest bias currents available in an integrated circuit amplifier.
  - The ultra low input bias currents are specified as the maximum measured at either input with the device fully warmed up on  $\pm 15$  volt supplies at +25 $^{\circ}$ C ambient with no heat sink. This parameter is 100% tested.
  - By using  $\pm 5$  volt supplies, input bias current can typically be brought below 50fA.
- The input offset voltage on all grades is laser trimmed to a level typically less than 500 $\mu$ V.
  - The offset voltage drift is the lowest available in an FET electrometer amplifier.
  - If additional nulling is desired, the amount required will have a minimal effect on offset drift (approximately 3 $\mu$ V/ $^{\circ}$ C per millivolt).
- The low quiescent current drain of 0.8mA typical and 1.5mA maximum, which is among the lowest available in operational amplifier designs of any type, keeps self-heating effects to a minimum and renders the AD515 suitable for a wide range of remote probe situations.
- The combination of low input noise voltage and very low input noise current is such that for source impedances from much over one Megohm up to 10<sup>11</sup> ohm, the Johnson noise of the source will easily dominate the noise characteristic.
- Every AD515 is subjected to long term, high temperature stabilization bakes, temperature cycled ten times from -65 $^{\circ}$ C to +150 $^{\circ}$ C, and given a high G shock test prior to final testing to insure reliability and long term stability.

# SPECIFICATIONS (typical @ +25°C with $V_S = \pm 15V$ dc, unless otherwise specified)

| MODEL  | AD515J                                | AD515K                       | AD515L                       |
|--|---------------------------------------|------------------------------|------------------------------|
| <b>OPEN LOOP GAIN (Note 1)</b>                         |                                       |                              |                              |
| $V_{out} = \pm 10V$ , $R_L \geq 2k\Omega$              | 20,000V/V min                         | 40,000V/V min                | 25,000V/V min                |
| $R_L \geq 10k\Omega$                                   | 40,000V/V min                         | 100,000V/V min               | 50,000V/V min                |
| $T_A = \text{min to max } R_L \geq 2k\Omega$           | 15,000V/V min                         | 40,000V/V min                | 25,000V/V min                |
| <b>OUTPUT CHARACTERISTICS</b>                          |                                       |                              |                              |
| Voltage @ $R_L = 2k\Omega$ , $T_A = \text{min to max}$ | $\pm 10V$ min ( $\pm 12V$ typ)        | *                            | *                            |
| @ $R_L = 10k\Omega$ , $T_A = \text{min to max}$        | $\pm 12V$ min ( $\pm 13V$ typ)        | *                            | *                            |
| Load Capacitance (Note 2)                              | 1000pF                                | *                            | *                            |
| Short Circuit Current                                  | 10mA min (25mA typ)                   | *                            | *                            |
| <b>FREQUENCY RESPONSE</b>                              |                                       |                              |                              |
| Unity Gain, Small Signal                               | 350kHz                                | *                            | *                            |
| Full Power Response                                    | 5kHz min (16kHz typ)                  | *                            | *                            |
| Slew Rate Inverting Unity Gain                         | 0.3V/ $\mu$ s min (1.0V/ $\mu$ s typ) | *                            | *                            |
| Overload Recovery Inverting Unity Gain                 | 100 $\mu$ s max (16 $\mu$ s typ)      | *                            | *                            |
| <b>INPUT OFFSET VOLTAGE (Note 3)</b>                   |                                       |                              |                              |
| vs. Temperature, $T_A = \text{min to max}$             | 3.0mV max (0.4mV typ)                 | 1.0mV max (0.4mV typ)        | 1.0mV max (0.4mV typ)        |
| vs. Supply, $T_A = \text{min to max}$                  | 50 $\mu$ V/ $^{\circ}$ C max          | 15 $\mu$ V/ $^{\circ}$ C max | 25 $\mu$ V/ $^{\circ}$ C max |
|  | 400 $\mu$ V/V max (50 $\mu$ V/V typ)  | 100 $\mu$ V/V max            | 200 $\mu$ V/V max            |
| <b>INPUT BIAS CURRENT</b>                              |                                       |                              |                              |
| Either Input (Note 4)                                  | 300fA max                             | 150fA max                    | 75fA max                     |
| <b>INPUT IMPEDANCE</b>                                 |                                       |                              |                              |
| Differential   | 1.6pF  10 <sup>13</sup> $\Omega$      | *                            | *                            |
| Common Mode  | 0.8pF  10 <sup>15</sup> $\Omega$      | *                            | *                            |
| <b>INPUT NOISE</b>                                     |                                       |                              |                              |
| Voltage, 0.1Hz to 10Hz                                 | 4.0 $\mu$ V (p-p)                     | *                            | *                            |
| f = 10Hz   | 75nV/ $\sqrt{\text{Hz}}$              | *                            | *                            |
| f = 100Hz  | 55nV/ $\sqrt{\text{Hz}}$              | *                            | *                            |
| f = 1kHz   | 50nV/ $\sqrt{\text{Hz}}$              | *                            | *                            |
| Current, 0.1 to 10Hz                                   | 0.003pA (p-p)                         | *                            | *                            |
| 10Hz to 10kHz  | 0.01pA rms                            | *                            | *                            |
| <b>INPUT VOLTAGE RANGE</b>                             |                                       |                              |                              |
| Differential   | $\pm 20V$ min                         | *                            | *                            |
| Common Mode, $T_A = \text{min to max}$                 | $\pm 10V$ min ( $\pm 12V$ typ)        | *                            | *                            |
| Common Mode Rejection, $V_{IN} = \pm 10V$              | 66dB min (94dB typ)                   | 80dB min                     | 70dB min                     |
| Maximum Safe Input Voltage (Note 5)                    | $\pm V_S$                             | *                            | *                            |
| <b>POWER SUPPLY</b>                                    |                                       |                              |                              |
| Rated Performance                                      | $\pm 15V$ typ                         | *                            | *                            |
| Operating  | $\pm 5V$ min ( $\pm 18V$ max)         | *                            | *                            |
| Quiescent Current                                      | 1.5mA max (0.8mA typ)                 | *                            | *                            |
| <b>TEMPERATURE</b>                                     |                                       |                              |                              |
| Operating, Rated Performance                           | 0 to +70 $^{\circ}$ C                 | *                            | *                            |
| Storage  | -65 $^{\circ}$ C to +150 $^{\circ}$ C | *                            | *                            |

\*Specifications same as AD515J.

## NOTES:

- Open Loop Gain is specified with or without nulling of  $V_{OS}$ .
- A conservative design would not exceed 750pF of load capacitance.
- Input Offset Voltage specifications are guaranteed after 5 minutes of operation at  $T_A = +25^{\circ}$ C.
- Bias Current specifications are guaranteed after 5 minutes of operation at  $T_A = +25^{\circ}$ C. For higher temperatures, the current doubles every +10 $^{\circ}$ C.
- If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can handle overload currents of 0.5mA indefinitely without damage. See next page.

Specifications and prices subject to change without notice.

## LAYOUT AND CONNECTION CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading. The AD515, with its combination of low offset voltage (normally eliminating the need for trimming), low quiescent current (minimal source heating, possible battery operation), internal compensation and small physical size lends itself very nicely to installation at the signal source or inside a probe. Also, as a result of the high load capacitance rating, the AD515 can comfortably drive a long signal cable.
2. The use of guarding techniques is essential to realizing the capability of the ultra-low input currents of the AD515. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation, and hence, no leakage. The guard will also act as a shield to reduce noise pickup and serves an additional function of reducing the effective capacitance to the input line. The case of the AD515 is brought out separately to pin 8 so that the case can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry, and reduces common-mode input capacitance to about 0.2pF. Figure 1 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and non-inverting applications. If pin 8 is not used for guarding, it should be connected to ground or a power supply to reduce noise.

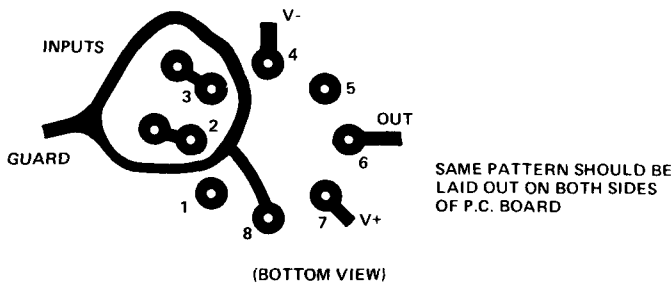


Figure 1. Board Layout for Guarding Inputs with Guarded TO-99 Package

3. Printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD515 can deliver. The best performance will be realized by using a teflon IC socket for the AD515; but at least a teflon stand-off should be used for the high-impedance lead. If this is not feasible, the input guarding scheme shown in Figure 1 will minimize leakage as much as possible; the guard ring should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.

4. Another important concern for achieving and maintaining low leakage currents is complete cleanliness of circuit boards and components. Completed assemblies should be washed thoroughly in a low residue solvent such as TMC Freon or high-purity methanol followed by a rinse with deionized water and nitrogen drying. If service is anticipated in a high contaminant or high humidity environment, a high dielectric conformal coating is recommended. All insulation materials except Kel-F or teflon will show rapid degradation of surface leakage at high humidities.

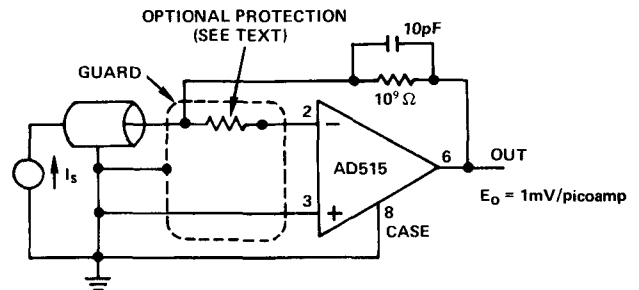


Figure 2. Picoampere Current-to-Voltage Converter Inverting Configuration

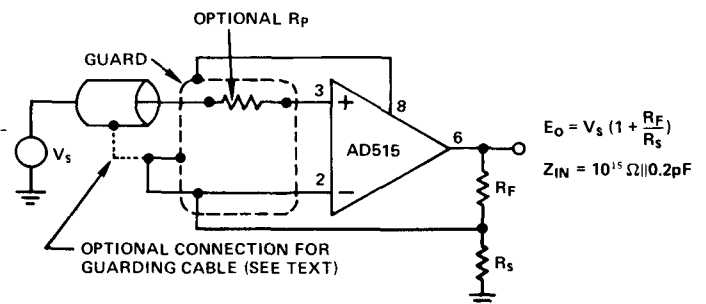


Figure 3. Very High Impedance Non-Inverting Amplifier

## INPUT PROTECTION

The AD515 is guaranteed for a maximum safe input potential equal to the power supply potential. The unique bootstrapped input stage design also allows differential input voltages of up to  $\pm 20$  volts (or within 10 volts of the sum of the supplies) while maintaining the full differential input resistance of  $10^{13} \Omega$ , as shown in Figure 10. This makes the AD515 suitable for low speed comparator situations employing a direct connection to a high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD515 requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 0.5mA (for example, 200k $\Omega$  for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figures 2 and 3 show proper connections.

## COAXIAL CABLE AND CAPACITANCE EFFECTS

If it is not possible to attach the AD515 virtually on top of the signal source, considerable care should be exercised in designing the connecting lines carrying the high impedance signal. Shielded coaxial cable must be used for noise reduction, but use of coaxial cables for high impedance work can add problems from cable leakage, noise, and capacitance. Only the best polyethylene or virgin teflon (not reconstituted) should be used to obtain the highest possible insulation resistance.

Cable systems should be made as rigid and vibration-free as possible since cable movement can cause noise signals of three types, all significant in high impedance systems. Frictional movement of the shield over the insulation material generates a charge which is sensed by the signal line as a noise voltage. Low noise cable with graphite lubricant such as Amphenol 21-537 will reduce the noise, but short rigid lines are better. Cable movements will also make small changes in the internal cable capacitance and capacitance to other objects. Since the total charge on these capacitances cannot be changed instantly, a noise voltage results as predicted from:  $\Delta V = Q/\Delta C$ . Noise voltage is also generated by the motion of a conductor in a magnetic field.

The conductor-to-shield capacitance of coaxial cable is normally about 30pF/foot. Charging this capacitance can cause considerable stretching of high impedance signal rise-time, thus cancelling the low input capacitance feature of the AD515. There are two ways to circumvent this problem. For inverting signals or low-level current measurements, the signal is carried on the line connected to the inverting input and shielded (guarded) by the ground line as shown in Figure 2. Since the signal is always at virtual ground, no voltage change is required and no capacitances are charged. In many circumstances, this will de-stabilize the circuit; if so, capacitance from output to inverting input will stabilize the circuit.

Non-inverting and buffer situations are more critical since the signal line voltage and therefore charge will change, causing signal delay. This effect can be reduced considerably by connecting the cable shield to guard potential instead of ground, an option shown in Figure 3. Since such a connection results in positive feedback to the input, the circuit may destabilize and oscillate. If so, capacitance from positive input to ground must be added to make the net capacitance at pin 3 positive. This technique can considerably reduce the effective capacitance which must be charged.

## Typical Performance Curves

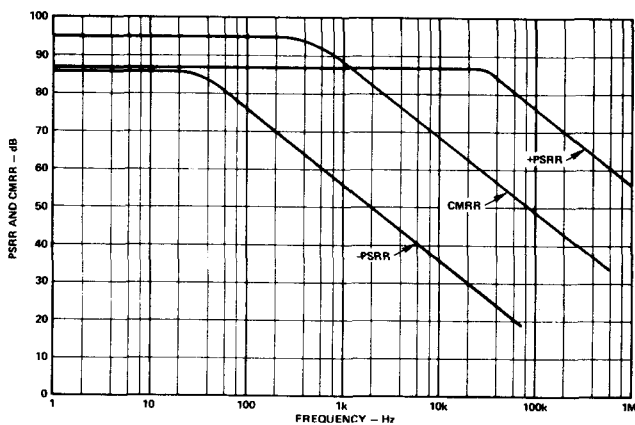


Figure 4. PSRR and CMRR Versus Frequency

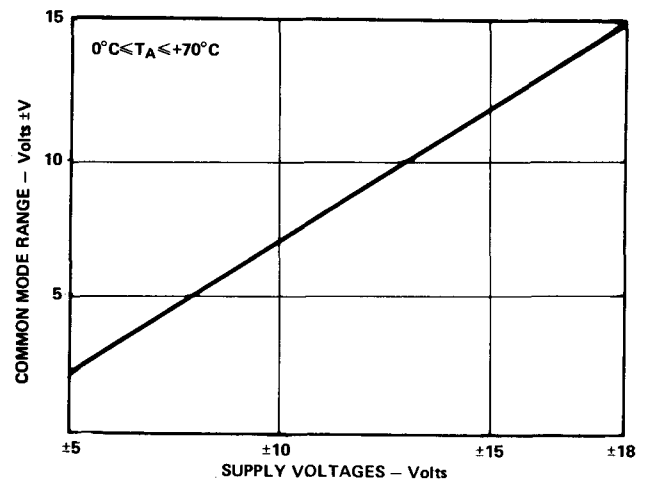


Figure 6. Input Common Mode Range Versus Supply Voltage

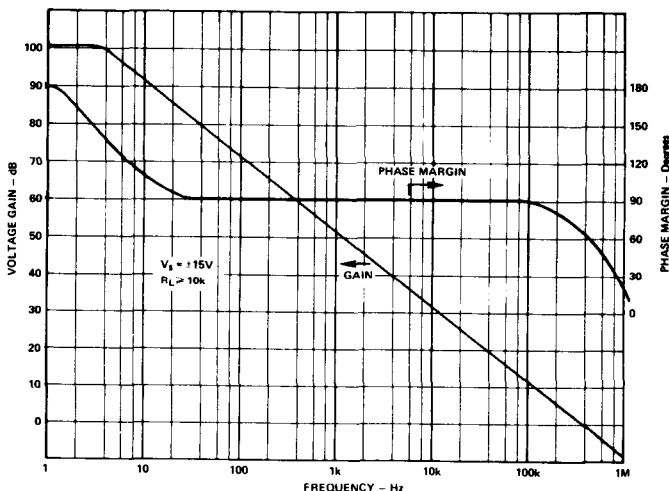


Figure 5. Open Loop Frequency Response

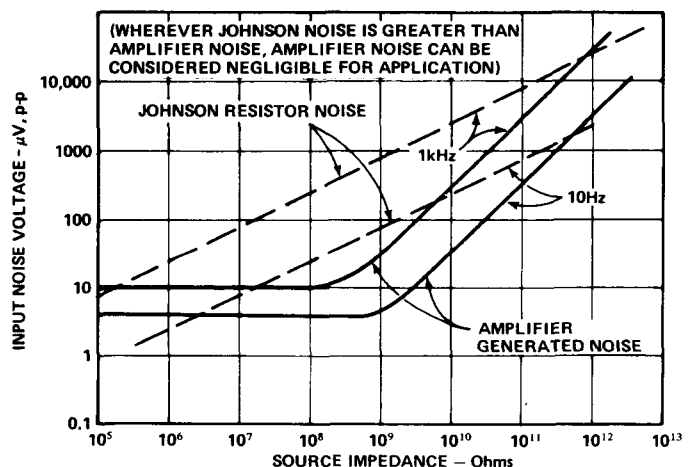


Figure 7. Peak-to-Peak Input Noise Voltage Versus Source Impedance and Bandwidth

## ELECTROMETER APPLICATION NOTES

The AD515 offers the lowest input bias currents available in an integrated circuit package. This design will open up many new application opportunities for measurements from very high impedance and very low current sources. Performing accurate measurements of this sort requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD515 and perhaps extending its performance limits.

- As with all junction FET input devices, the temperature of the FET's themselves is all-important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every  $10^{\circ}\text{C}$ ; therefore, every effort should be made to minimize device operating temperature.
- The heat dissipation can be reduced initially by careful investigation of the application. First, if it is possible to reduce the required power supplies, this should be done since internal power consumption contributes the largest component of self-heating. To minimize this effect, the quiescent current of the AD515 has been reduced to a level much lower than that of any other electrometer-grade device, but additional performance improvement can be gained by lowering the supply voltages, to  $\pm 5$  volts if possible. The effects of this are shown in Figure 8, which shows typical input bias current and quiescent current versus supply voltage.
- Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a  $2\text{k}\Omega$  load driven at 10 volts at the output will cause at least an additional 25 milliwatts dissipation in the output stage (and some in other stages) over the typical 24 milliwatts, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated. Therefore, although many DC performance parameters are specified driving a  $2\text{k}\Omega$  load, to reduce this additional dissipation, we recommend restricting the load impedance to be at least  $10\text{k}\Omega$ .

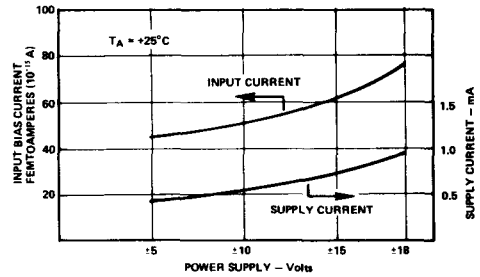


Figure 8. Input Bias Current and Supply Current Versus Supply Voltage

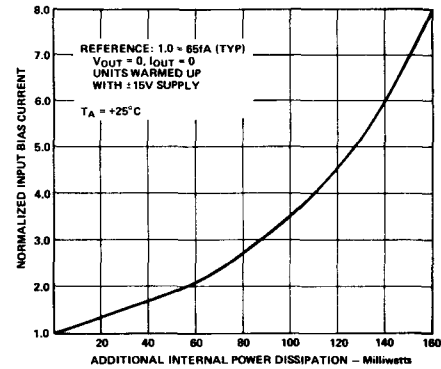


Figure 9. Input Bias Current Versus Additional Power Dissipation

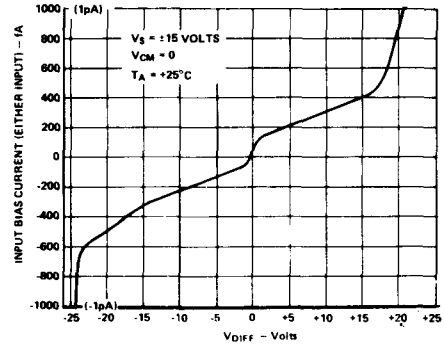
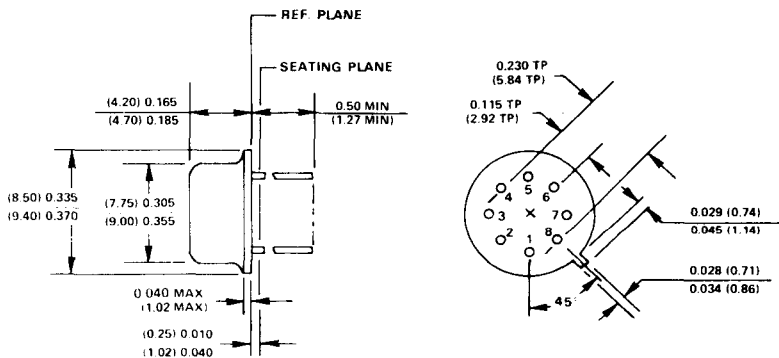


Figure 10. Input Bias Current Versus Differential Input Voltage

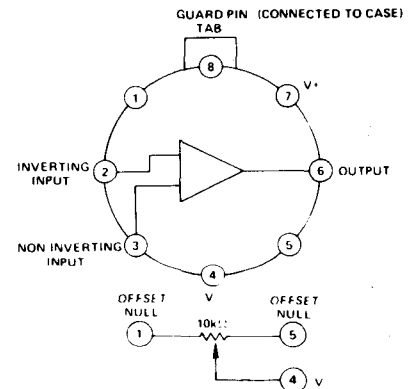
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TO-99

## PIN CONFIGURATION



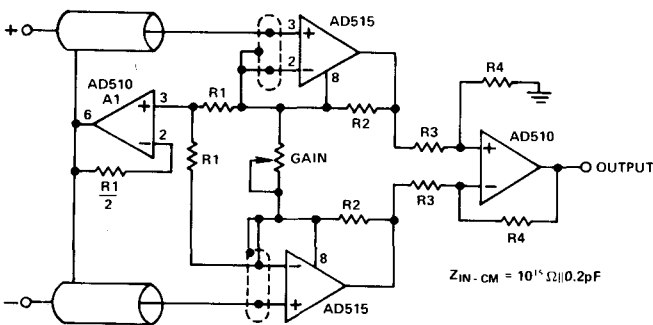
TOP VIEW

## AD515 CIRCUIT APPLICATION NOTES

The AD515 is quite simple to apply to a wide variety of applications because of the pre-trimmed offset voltage and internal compensation, which minimize required external components and eliminate the need for adjustments to the device itself. The major considerations in applying this device are the external problems of layout and heat control which have already been discussed. In circuit situations employing the use of very high value resistors, such as low level current to voltage converters, electrometer operational amplifiers can be destabilized by a pole created by the small capacitance at the negative input. If this occurs, a capacitor of 2 to 5pF in parallel with the resistor will stabilize the loop. A much larger capacitor may be used if desired to limit bandwidth and thereby reduce wideband noise.

Selection of passive components employed in high impedance situations is critical. High-megohm resistors should be of the carbon film or deposited ceramic oxide to obtain the best in low noise and high stability performance. The best packaging for high-megohm resistors is a glass body sprayed with silicone varnish to minimize humidity effects. These resistors must be handled very carefully to prevent surface contamination. Capacitors for any high impedance or long term integration situation should be of a polystyrene formulation for optimum performance. Most other types have too low an insulation resistance, or high dielectric absorption.

Unlike situations involving standard operational amplifiers with much higher bias currents, balancing the impedances seen at the input terminals of the AD515 is usually unnecessary and probably undesirable. At the large source impedances where these effects matter, obtaining quality, matched resistors will be difficult. More important, instead of a cancelling effect, as with bias current, the noise voltage of the additional resistor will add by root-sum-of-squares to that of the other resistor thus increasing the total noise by about 40%. Noise currents driving the resistors also add, but in the AD515 are significant only above  $10^{11}\Omega$ .



(ALL RESISTORS OF SAME NUMBER SHOULD BE MATCHED :0.1%)  
(BUFFER A1 BOOSTS COMMON MODE  $Z_{IN}$  BY DRIVING CABLE SHIELDS AT COMMON MODE VOLTAGE AND NEUTRALIZING CM CAPACITANCE)

Figure 11. Very High Impedance Instrumentation Amplifier

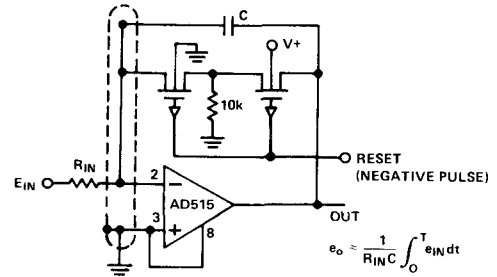


Figure 12. Low Drift Integrator with Low-Leakage Guarded Reset

## LOW-LEVEL CURRENT TO VOLTAGE CONVERTERS

Figure 2 shows a standard low-level current-to-voltage converter. To obtain higher sensitivity, it is obvious to simply use a higher value feedback resistor. However, high value resistors above  $10^9\Omega$  tend to be expensive, large, noisy and unstable. To avoid this, it may be desirable to use a circuit configuration with output gain, as in Figure 13. The drawback is that input errors of offset voltage drift and noise are multiplied by the same gain, but the precision performance of the AD515 makes the tradeoff easier.

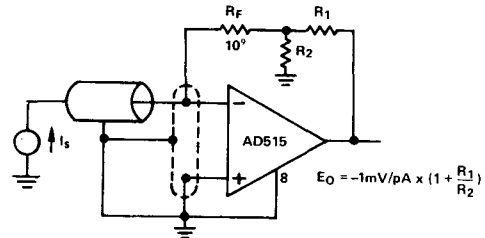


Figure 13. Picoampere to Voltage Converter with Gain

One of the problems with low-level leakage current testing or low-level current transducers (such as Clark oxygen sensors) is finding a way to apply voltage bias to the device while still grounding the device and the bias source. Figure 14 shows a technique in which the desired bias is applied at the non-inverting terminal thus forcing that voltage at the inverting terminal. The current is sensed by  $R_F$ , and the AD521 instrumentation amplifier converts the floating differential signal to a single-ended output.

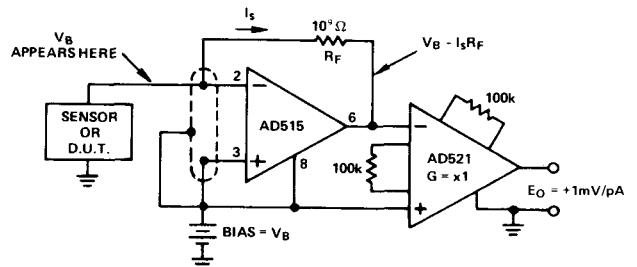
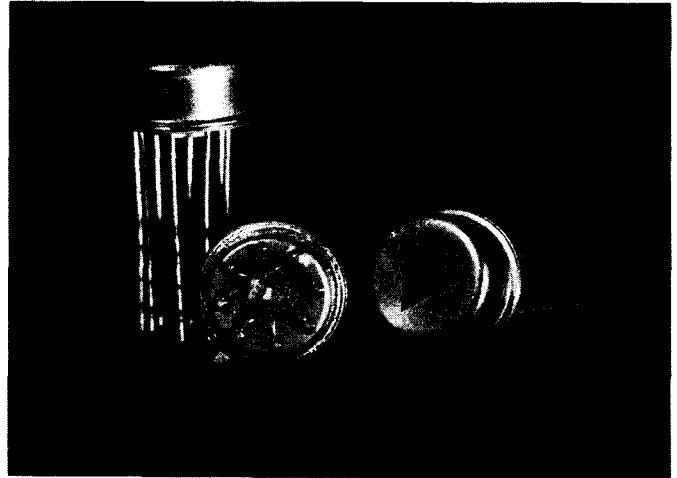


Figure 14. Current-to-Voltage Converter with Grounded Bias and Sensor

**FEATURES**

**Low Input Bias Current: 1nA max (AD517L)**  
**Low Input Offset Current: 0.25nA max (AD517L)**  
**Low  $V_{os}$ : 25 $\mu$ V max (AD517L), 150 $\mu$ V max (AD517J)**  
**Low  $V_{os}$  Drift: 0.5 $\mu$ V/ $^{\circ}$ C (AD517L)**  
**Internal Compensation**  
**Internal Compensation**  
**Low Cost.**

**PRODUCT DESCRIPTION**

The AD517 is a high accuracy monolithic op amp featuring extremely low offset voltages and input currents. Analog Devices' thermally-balanced layout and superior IC processing combine to produce a truly precision device at low cost.

The AD517 is laser trimmed at the wafer level (LWT) to produce offset voltages less than 25 $\mu$ V and offset voltage drifts less than 0.5 $\mu$ V/ $^{\circ}$ C unnullled. Superbeta input transistors provide extremely low input bias currents of 1nA max and offset currents as low as 0.25nA max. While these figures are comparable to presently available BIFET amplifiers at room temperature, the AD517 input currents decrease, rather than increase, at elevated temperatures. Open-loop gain in many IC amplifiers is degraded under loaded conditions due to thermal gradients on the chip. However, the AD517 layout is balanced along a thermal axis, maintaining open-loop gain in excess of 1,000,000 for a wide range of load resistances.

The input stage of the AD517 is fully protected, allowing differential input voltages of up to  $\pm V_S$  without degradation of gain or bias current due to reverse breakdown. The output stage is short-circuit protected and is capable of driving a load capacitance up to 1000pF.

The AD517 is well suited to applications requiring high precision and excellent long-term stability at low cost, such as stable references, followers, bridge instruments and analog computation circuits.

The circuit is packaged in a hermetically sealed TO-99 metal can, and is available in three performance versions (J, K, and L) specified over the commercial 0 to +70 $^{\circ}$ C range; and one version (AD517S) specified over the full military temperature range, -55 $^{\circ}$ C to +125 $^{\circ}$ C. The AD517S is also available with full processing to the requirements of MIL-STD-883, Level B.

**PRODUCT HIGHLIGHTS**

1. Offset voltage is 100% tested and guaranteed on all models. Testing is performed using a controlled-temperature drift bath following a 5 minute warm-up period.
2. The AD517 exhibits extremely low input bias currents without sacrificing CMRR (over 100dB) or offset voltage stability.
3. The AD517 inputs are protected (to  $\pm V_S$ ), preventing offset voltage and bias current degradation due to reverse breakdown of the input transistors.
4. Internal compensation is provided, eliminating the need for additional components (often required by high accuracy IC op amps).
5. The AD517 can directly replace 725, 108, and AD510 amplifiers. In addition, it can replace 741-type amplifiers if the offset-nulling potentiometer is removed.
6. Thermally-balanced layout insures high open-loop gain independent of thermal gradients induced by output loading, offset nulling, and power supply variations.
7. Every AD517 is baked for 48 hours at +150 $^{\circ}$ C, temperature cycled from -65 $^{\circ}$ C to +200 $^{\circ}$ C, and subjected to a high G shock test to assure reliability and long-term stability.



# SPECIFICATIONS

(typical @ +25°C and ±15V dc unless otherwise noted)

| MODEL   | AD517J                 | AD517K        | AD517L       | AD517S <sup>1</sup> |
|---|------------------------|---------------|--------------|---------------------|
| <b>OPEN LOOP GAIN</b>                               |                        |               |              |                     |
| $V_O = \pm 10V, R_L \geq 2k\Omega$                  | 10 <sup>6</sup> min    | *             | *            | *                   |
| $T_{min}$ to $T_{max}$                              | 500,000 min            | *             | *            | 250,000             |
| <b>OUTPUT CHARACTERISTICS</b>                       |                        |               |              |                     |
| Voltage @ $R_L \geq 2k\Omega, T_{min}$ to $T_{max}$ | ±10V min               | *             | *            | *                   |
| Load Capacitance                                    | 1000pF                 | *             | *            | *                   |
| Output Current                                      | 10mA min               | *             | *            | *                   |
| Short Circuit Current                               | 25mA                   | *             | *            | *                   |
| <b>FREQUENCY RESPONSE</b>                           |                        |               |              |                     |
| Unity Gain, Small Signal                            | 250kHz                 | *             | *            | *                   |
| Full Power Response                                 | 1.5kHz                 | *             | *            | *                   |
| Slew Rate, Unity Gain                               | 0.10V/μs               | *             | *            | *                   |
| <b>INPUT OFFSET VOLTAGE</b>                         |                        |               |              |                     |
| Initial Offset, $R_S \leq 10k\Omega$                | 150μV max              | 50μV max      | 25μV max     | **                  |
| vs. Temp., $T_{min}$ to $T_{max}$                   | 3.0μV/°C max           | 1.0μV/°C max  | 0.5μV/°C max | **                  |
| vs. Supply  | 25μV/V max             | 10μV/V max    | **           | **                  |
| ( $T_{min}$ to $T_{max}$ )                          | 40μV/V max             | 15μV/V max    | **           | 20μV/V max          |
| <b>INPUT OFFSET CURRENT</b>                         |                        |               |              |                     |
| Initial   | 1nA max                | 0.75nA max    | 0.25nA max   | **                  |
| $T_{min}$ to $T_{max}$                              | 1.5nA max              | 1.25nA max    | 0.4nA max    | 2nA max             |
| <b>INPUT BIAS CURRENT</b>                           |                        |               |              |                     |
| Initial   | 5nA max                | 2nA max       | 1nA max      | **                  |
| $T_{min}$ to $T_{max}$                              | 8nA max                | 3.5nA max     | 1.5nA max    | 10nA max            |
| vs. Temp, $T_{min}$ to $T_{max}$                    | ±20pA/°C               | ±10pA/°C      | ±4pA/°C      | **                  |
| <b>INPUT IMPEDANCE</b>                              |                        |               |              |                     |
| Differential  | 15MΩ    1.5pF          | 20MΩ    1.5pF | **           | **                  |
| Common Mode   | 2.0x10 <sup>11</sup> Ω | *             | *            | *                   |
| <b>INPUT NOISE</b>                                  |                        |               |              |                     |
| Voltage, 0.1Hz to 10Hz                              | 2μV p-p                | *             | *            | *                   |
| f = 10Hz  | 35nV/√Hz               | *             | *            | *                   |
| f = 100Hz   | 25nV/√Hz               | *             | *            | *                   |
| f = 1kHz  | 20nV/√Hz               | *             | *            | *                   |
| Current, f = 10Hz                                   | 0.05pA/√Hz             | *             | *            | *                   |
| f = 100Hz   | 0.03pA/√Hz             | *             | *            | *                   |
| f = 1kHz  | 0.03pA/√Hz             | *             | *            | *                   |
| <b>INPUT VOLTAGE RANGE</b>                          |                        |               |              |                     |
| Differential or Common Mode max Safe                | ±V <sub>S</sub>        | *             | *            | *                   |
| Common Mode Rejection, $V_{in} = \pm 10V$           | 94dB min               | 110dB min     | **           | **                  |
| Common Mode Rejection, $T_{min}$ to $T_{max}$       | 94dB min               | 100dB min     | **           | **                  |
| <b>POWER SUPPLY</b>                                 |                        |               |              |                     |
| Rated Performance                                   | ±15V                   | *             | *            | *                   |
| Operating   | ±(5 to 18)V            | *             | *            | ±(5 to 22)V         |
| Current, Quiescent                                  | 4mA max                | 3mA max       | **           | **                  |
| <b>TEMPERATURE RANGE</b>                            |                        |               |              |                     |
| Operating Rated Performance                         | 0 to +70°C             | *             | *            | -55°C to +125°C     |
| Storage   | -65°C to +150°C        | *             | *            | *                   |

## NOTES

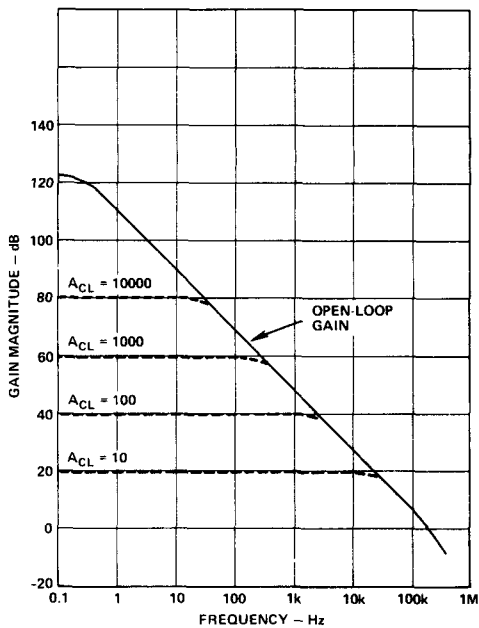
\*Specifications same as AD517J

\*\*Specifications same as AD517K

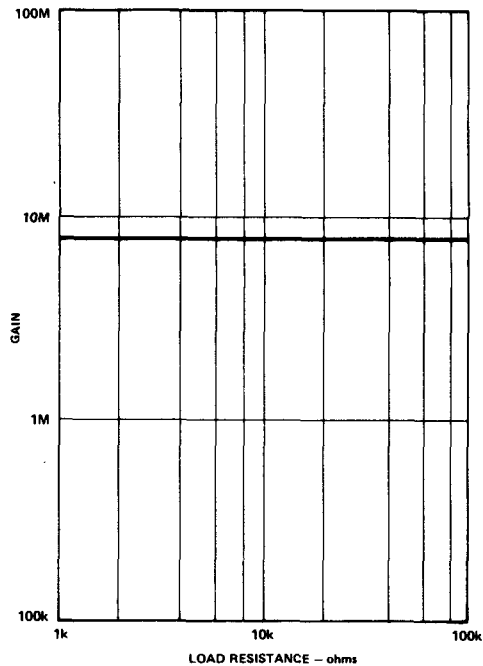
Specifications subject to change without notice.

<sup>1</sup>The AD517S is available fully processed and screened to the requirements of MIL-STD-883, Level B. Consult factory for pricing.

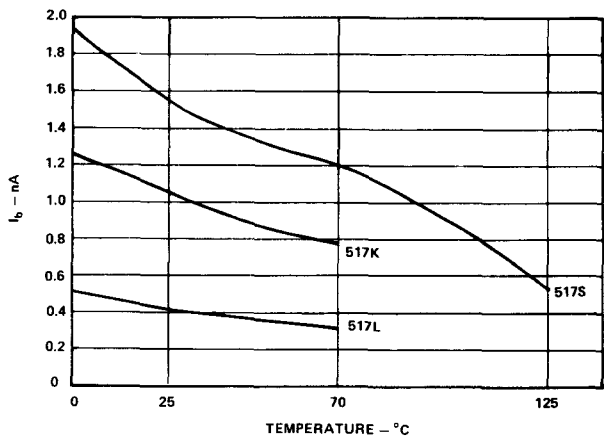
# Typical Performance Curves



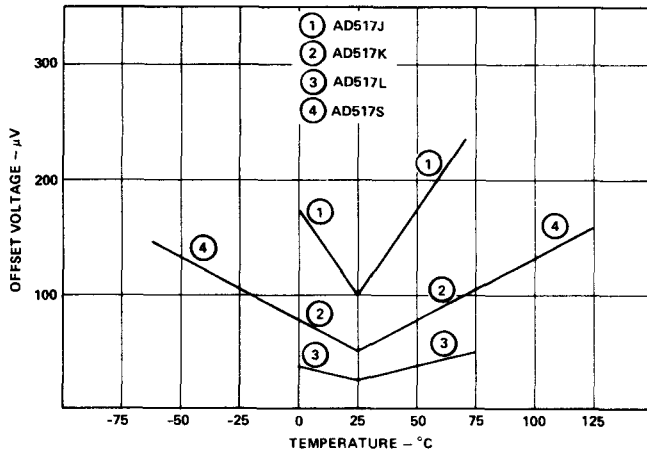
Small-Signal Gain vs. Frequency



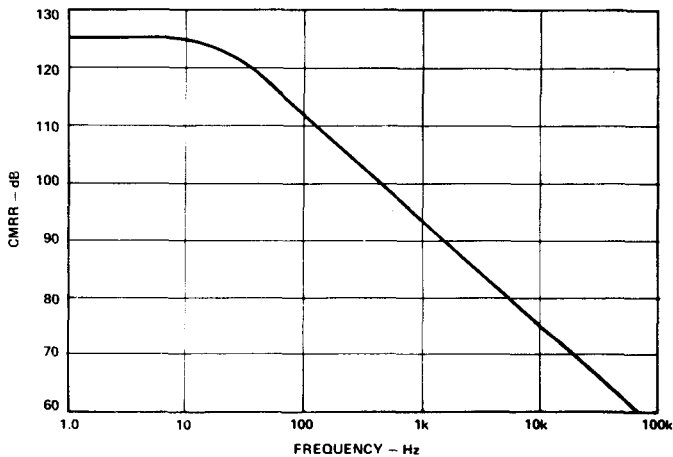
Open-Loop Gain vs. Load Resistance



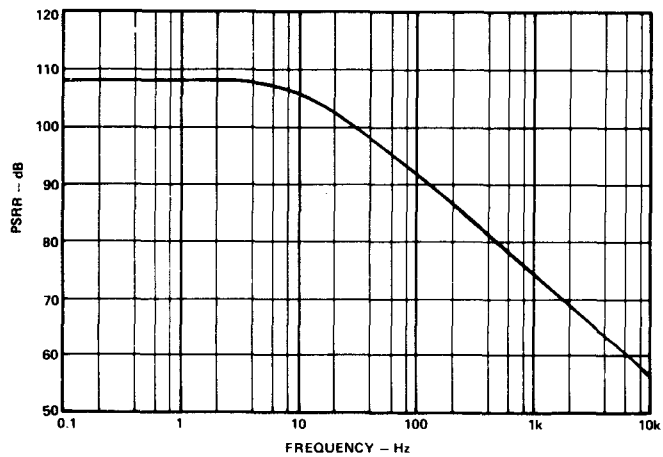
Input Bias Current vs. Temperature



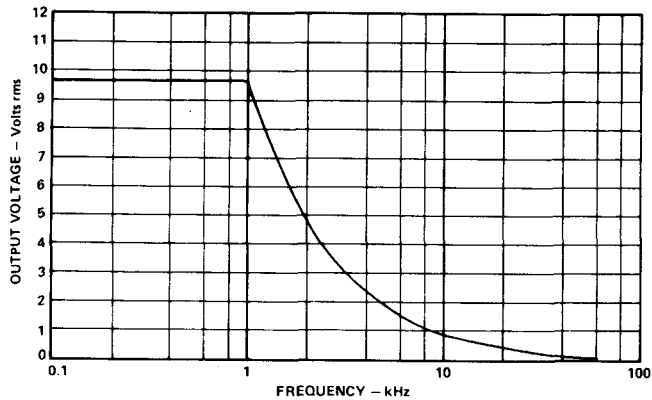
Max Untrimmed Offset Voltage vs. Temperature



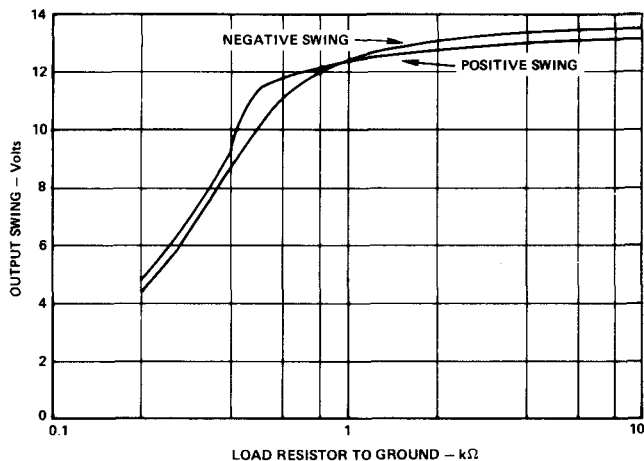
CMRR vs. Frequency



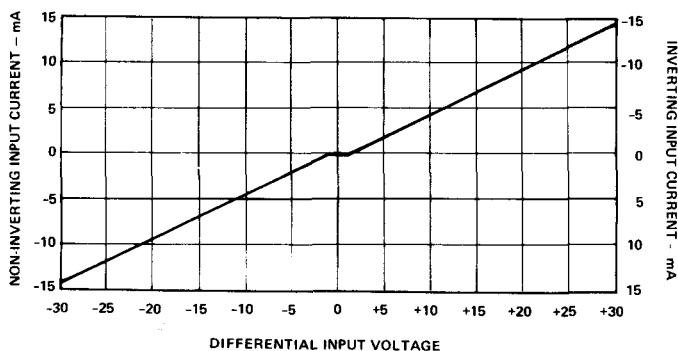
PSRR vs. Frequency



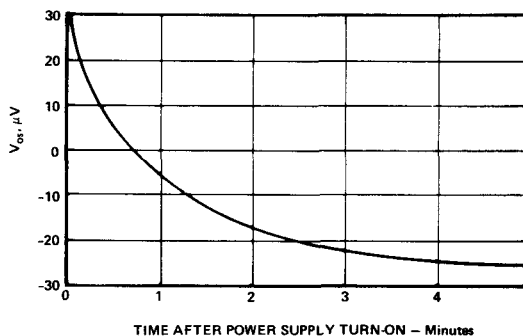
Maximum Undistorted Output vs. Frequency (Distortion  $\leq 1\%$ )



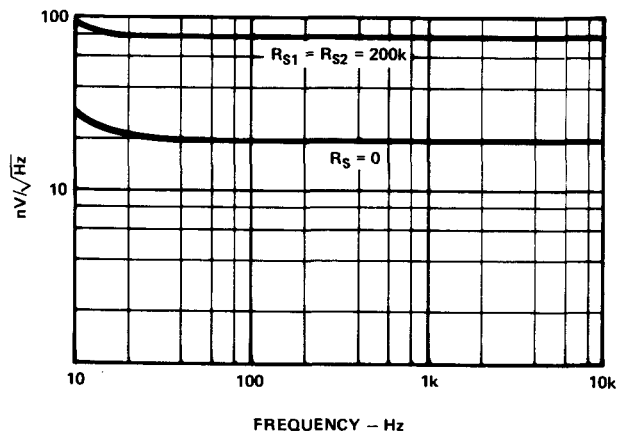
Output Voltage vs. Load Resistance



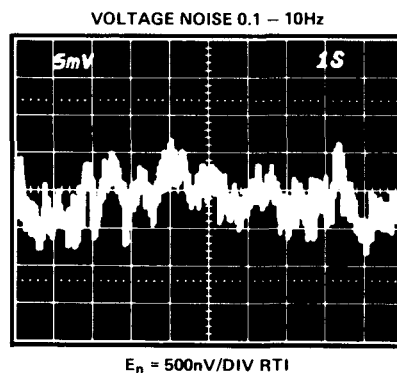
Input Current vs. Differential Input Voltage



Warm-Up Offset Voltage Drift



Total Input Noise Voltage vs. Frequency



Low Frequency Voltage Noise (0.1 to 10Hz)

## NULLING THE AD517

The internally-trimmed offset voltage of the AD517 will be low enough for most circuits without further nulling. However, in high precision applications, the AD517 may be nulled using either of the following methods:

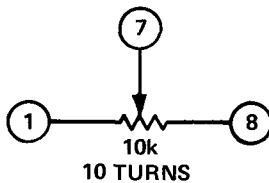
Figure 1A shows a simple circuit using a 10kΩ, ten-turn potentiometer. This circuit allows nulling to within several microvolts.

The circuit of Figure 1B is recommended in applications where nulling to within 1μV is desired. This circuit has the advantage that potentiometer instability effects are reduced by a factor of ten. Values of R<sub>1</sub>' and R<sub>2</sub>' are calculated as follows:

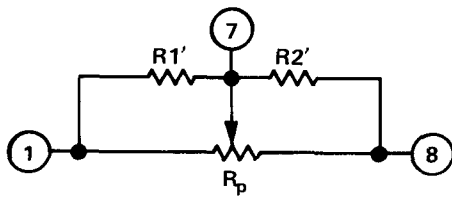
1. Null the offset to zero using a standard 10k pot, as shown in Figure 1A.
2. Measure pot halves R<sub>1</sub> and R<sub>2</sub>.
3. Calculate:

$$R_1' = \frac{R_1 \times 50k\Omega}{50k\Omega - R_1} \quad R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$$

4. Replace the pot with R<sub>1</sub>' and R<sub>2</sub>' using the closest value 1% metal film resistors.
5. Use a 100k, ten-turn pot for R<sub>p</sub> to complete the nulling.



A. Simple



B. High Precision

Figure 1. Nulling Circuits

## AN INSTRUMENT INPUT AMPLIFIER USING THE AD517L

The circuit shown in Figure 2 represents a typical input stage for laboratory instruments and panel meters. The amplifier is non-inverting and offers selectable gains from 1 to 1000 in decade steps.

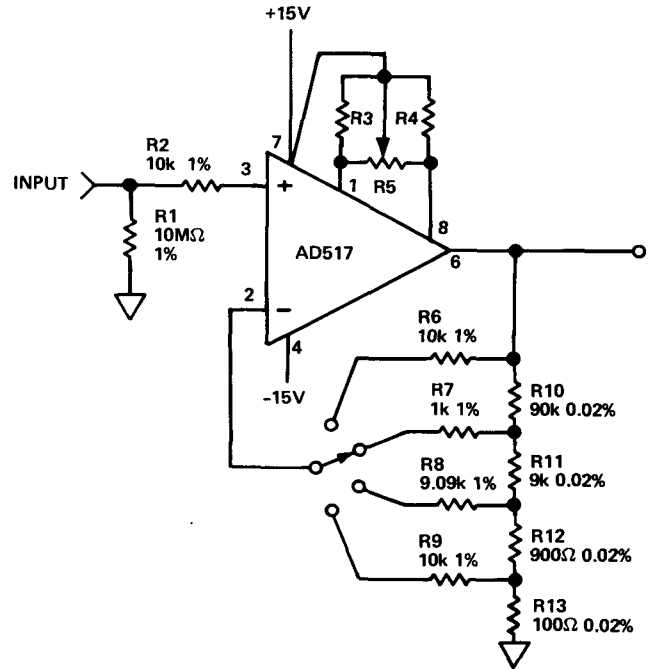


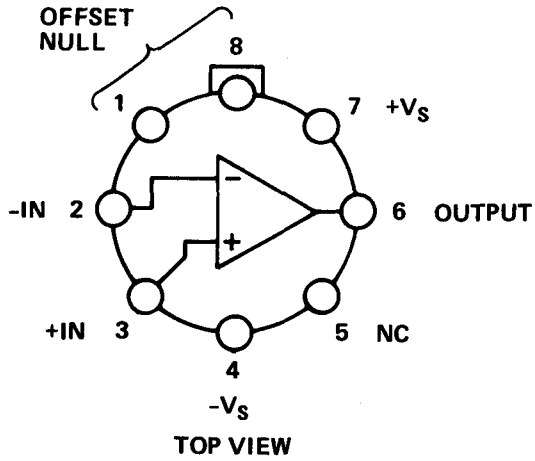
Figure 2. Stable Instrument Input Amplifier

Input impedance of this amplifier is 10 megohms, determined by resistor R<sub>1</sub>. The offset nulling network comprised of R<sub>3</sub>, R<sub>4</sub> and R<sub>5</sub> is the same one described earlier. If a less precise adjustment can be tolerated, a single 10k potentiometer can be substituted for R<sub>3</sub>, R<sub>4</sub> and R<sub>5</sub>.

Gain switching is accomplished in the feedback network. The divider consisting of R<sub>10</sub>, R<sub>11</sub>, R<sub>12</sub> and R<sub>13</sub> determines the gain by dividing the output and returning it to the inverting input of the amplifier. The ratio tolerances of these resistors uniquely determine the gain of the amplifier. The impedance seen by the inverting input is held constant at 10k ohms by R<sub>6</sub>, R<sub>7</sub>, R<sub>8</sub> or R<sub>9</sub> depending on the gain selected. Since input bias currents flow through equal resistances, the offset voltages produced will cancel each other. The input offset currents will produce an insignificant offset voltage on the order of 1 microvolt. If this offset is nulled out at the highest gain selected, it will be nulled on all ranges.

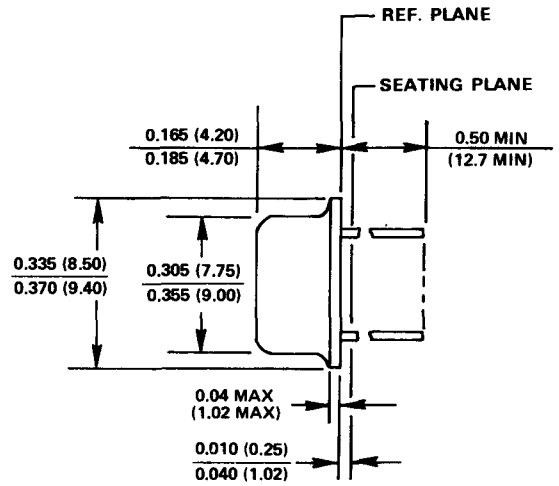
The AD517 offers excellent temperature stability in this circuit. Once the offset has been zeroed, the error produced by offset current drift will remain quite low due to the extremely low offset current drift of the AD517. A FET-input op amp would not work well in this application, since the input offset currents would double for each 10°C increase in temperature, soon exceeding the input offset currents of the AD517.

### PIN CONFIGURATION



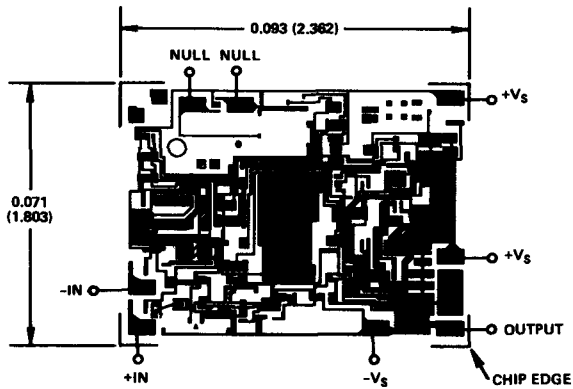
### OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

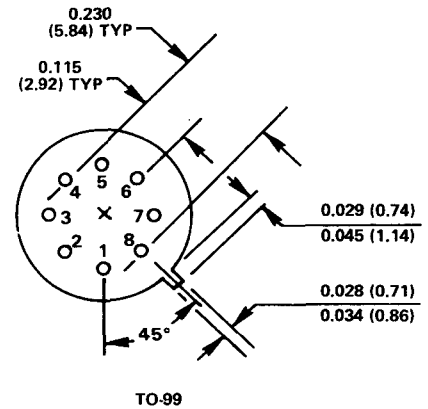


### CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).



THE AD517 IS AVAILABLE IN LASER-TRIMMED CHIP FORM. CONSULT CHIP CATALOG FOR DETAILS.



**FEATURES**

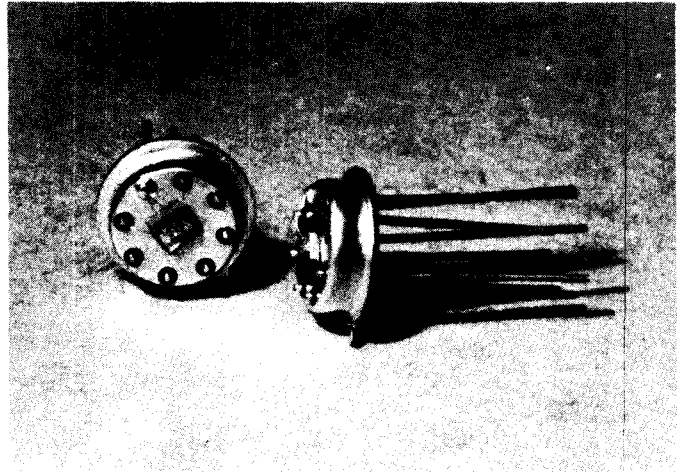
- Low Bias Current:** 25pA max, warmed-up (AD542K,L), 50pA max (AD542J)
- Low Offset Voltage:** 0.5mV max (AD542L), 1.0mV max (AD542K)
- Low Offset Voltage Drift:** 5 $\mu$ V/ $^{\circ}$ C max (AD542L), 10 $\mu$ V/ $^{\circ}$ C max (AD542K), 20 $\mu$ V/ $^{\circ}$ C max (AD542J)
- Low Quiescent Current:** 1.5mA max
- Low Price**

**PRODUCT DESCRIPTION**

The AD542 is a precision, monolithic FET-input operational amplifier fabricated with the most advanced BI-FET and laser trimming technologies. The AD542 offers bias currents significantly lower than currently available BI-FET devices: 25pA max, warmed-up for the AD542K and L, 50pA max for the AD542J. In addition, the offset voltage is laser trimmed to less than 0.5mV on the AD542L and 1.0mV on the AD542K utilizing Analog's exclusive laser-wafer-trimming (LWT) process. When combined with the AD542's low offset voltage drift (5 $\mu$ V/ $^{\circ}$ C max for "L", 10 $\mu$ V/ $^{\circ}$ C max for "K"), these features offer the user IC performance truly superior to existing BI-FET op amps — and at low, BI-FET pricing.

The key to BI-FET technology is the ion-implanted JFET. Ion-implantation (as opposed to diffusion) permits the fabrication of precision, matched JFET's on a monolithic bi-polar chip. Analog Devices optimizes the BI-FET process to produce bias currents lower than other popular BI-FET op amps and specifies each device for the maximum value at either input in the fully warmed-up condition. Additional benefits of this optimization include low voltage noise (2 $\mu$ V p-p, 0.1 — 10Hz), and low quiescent current.

The AD542 is recommended for any operational amplifier application requiring excellent dc performance at low and moderate costs. Precision instrument front ends requiring accurate amplification of millivolt level signals from megohm source impedances will benefit from the device's excellent combination of low offset voltage and drift, low bias current and low 1/f noise. High common mode rejection (80dB, min on the "K" and "L" versions) and high open-loop gain—even under heavy loading—ensures better than "12-bit" linearity in high impedance buffer applications. Additionally, band-



width and slew rate are much increased over presently available precision, bipolar op amps.

The AD542 is available in three versions: the "J", "K" and "L", all specified over the 0 to +70 $^{\circ}$ C temperature range and one version, "S", over the -55 $^{\circ}$ C to +125 $^{\circ}$ C military operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

**PRODUCT HIGHLIGHTS**

1. Improved BI-FET processing on the AD542 results in the lowest bias current available in a BI-FET op amp.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD542 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max (AD542L), thus eliminating the need for external nulling in many situations.
4. If offset nulling is required, the additional offset voltage drift induced will be minimal. (Offset voltage drift can increase an additional 3 $\mu$ V/ $^{\circ}$ C per mV of offset nulled.)
5. Low voltage noise (2 $\mu$ V, p-p), and low offset voltage drift enhance the AD542's performance as a precision op amp.
6. The 1.5mA max quiescent current enables the device to be used in numerous portable applications where low battery drain is essential. This is achieved without sacrificing open loop gain or the ability to drive up to a 10mA load.

# SPECIFICATIONS

(typical @ +25°C and  $V_S = \pm 15V$  dc unless otherwise specified)

| MODEL  | AD542J                         | AD542K                 | AD542L                | AD542S                 |
|--|--------------------------------|------------------------|-----------------------|------------------------|
| <b>OPEN LOOP GAIN<sup>1</sup></b>                    |                                |                        |                       |                        |
| $V_{out} = \pm 10V, R_L \geq 1k\Omega$               | 50,000 min                     | 150,000 min            | **                    | **                     |
| $R_L \geq 2k\Omega$                                  | 100,000 min                    | 300,000 min            | **                    | **                     |
| $T_A = \text{min to max}$                            | 100,000 min                    | 300,000 min            | **                    | **                     |
| <b>OUTPUT CHARACTERISTICS</b>                        |                                |                        |                       |                        |
| Voltage @ $R_L = 2k\Omega, T_A = \text{min to max}$  | $\pm 10V$ min ( $\pm 12V$ typ) | *                      | *                     | *                      |
| Voltage @ $R_L = 10k\Omega, T_A = \text{min to max}$ | $\pm 12V$ min ( $\pm 13V$ typ) | *                      | *                     | *                      |
| Short Circuit Current                                | 25mA                           | *                      | *                     | *                      |
| <b>FREQUENCY RESPONSE</b>                            |                                |                        |                       |                        |
| Unity Gain, Small Signal                             | 1.0MHz                         | *                      | *                     | *                      |
| Full Power Response                                  | 50kHz                          | *                      | *                     | *                      |
| Slew Rate, Unity Gain                                | 3.0V/ $\mu$ s                  | *                      | *                     | *                      |
| <b>INPUT OFFSET VOLTAGE<sup>2</sup></b>              |                                |                        |                       |                        |
| vs. Temperature                                      | 2.0mV max                      | 1.0mV max              | 0.5mV max             | **                     |
| vs. Supply, $T_A = \text{min to max}$                | $20\mu V/^\circ C$ max         | $10\mu V/^\circ C$ max | $5\mu V/^\circ C$ max | $15\mu V/^\circ C$ max |
| vs. Supply, $T_A = \text{min to max}$                | $200\mu V/V$ max               | $100\mu V/V$ max       | **                    | **                     |
| <b>INPUT BIAS CURRENT</b>                            |                                |                        |                       |                        |
| Either Input <sup>3</sup>                            | 50pA max                       | 25pA max               | **                    | **                     |
| Input Offset Current                                 | 5pA                            | 2pA                    | **                    | **                     |
| <b>INPUT IMPEDANCE</b>                               |                                |                        |                       |                        |
| Differential   | $10^{10}\Omega    2pF$         | *                      | *                     | *                      |
| Common Mode  | $10^{11}\Omega    2pF$         | *                      | *                     | *                      |
| <b>INPUT VOLTAGE RANGE</b>                           |                                |                        |                       |                        |
| Differential <sup>4</sup>                            | $\pm 20V$                      | *                      | *                     | *                      |
| Common Mode  | $\pm 10V$ min ( $\pm 12V$ typ) | *                      | *                     | *                      |
| Common Mode Rejection, $V_{in} = \pm 10V$            | 76dB min                       | 80dB min               | **                    | **                     |
| <b>POWER SUPPLY</b>                                  |                                |                        |                       |                        |
| Rated Performance                                    | $\pm 15V$                      | *                      | *                     | *                      |
| Operating  | $\pm(5 \text{ to } 18)V$       | *                      | *                     | *                      |
| Quiescent Current                                    | 1.5mA max                      | *                      | *                     | *                      |
| <b>VOLTAGE NOISE</b>                                 |                                |                        |                       |                        |
| 0.1-10Hz   | 2 $\mu V$ p-p                  | *                      | *                     | *                      |
| 10Hz   | $70nV/\sqrt{Hz}$               | *                      | *                     | *                      |
| 100Hz  | $45nV/\sqrt{Hz}$               | *                      | *                     | *                      |
| 1kHz   | $30nV/\sqrt{Hz}$               | *                      | *                     | *                      |
| 10kHz  | $25nV/\sqrt{Hz}$               | *                      | *                     | *                      |
| <b>TEMPERATURE RANGE</b>                             |                                |                        |                       |                        |
| Operating, Rated Performance                         | 0 to +70°C                     | *                      | *                     | -55 to +125°C          |
| Storage  | -65 to +150°C                  | *                      | *                     | *                      |

## NOTES:

<sup>1</sup> Open Loop Gain is specified with  $V_{OS}$  both nulled and unnullled.

<sup>2</sup> Input Offset Voltage specifications are guaranteed after 5 minutes of operation at  $T_A = +25^\circ C$ .

<sup>3</sup> Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at  $T_A = +25^\circ C$ . For higher temperatures, the current doubles every  $10^\circ C$ .

<sup>4</sup> Defined as voltage between inputs, such that neither exceeds  $\pm 10V$  from ground.

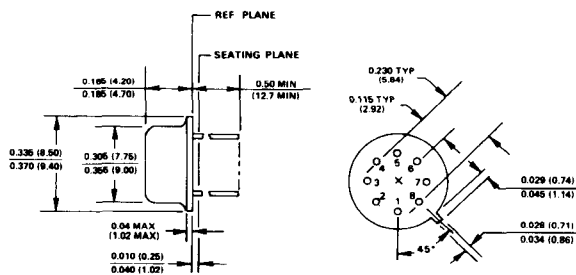
\*Specifications same as AD542J.

\*\*Specifications same as AD542K.

Specifications and prices subject to change without notice.

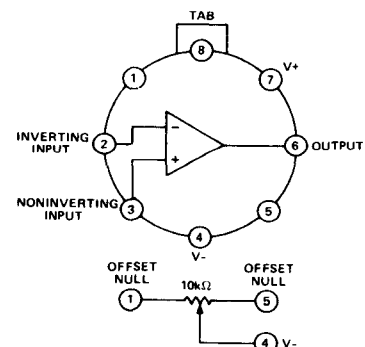
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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## PIN CONFIGURATION



TOP VIEW

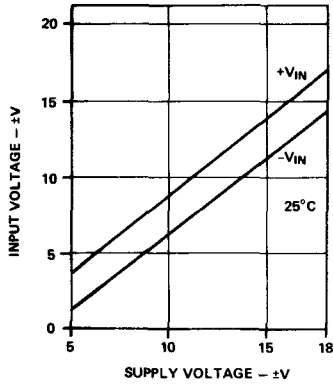


Figure 1. Input Voltage Range

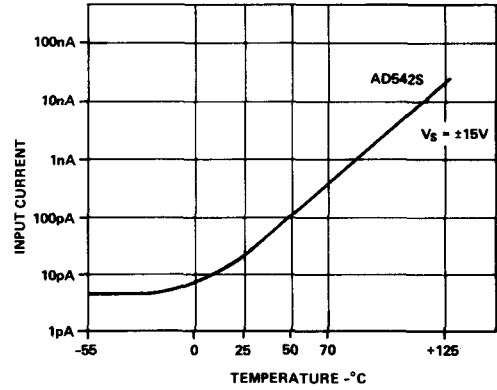


Figure 4b. Input Current vs. Temperature

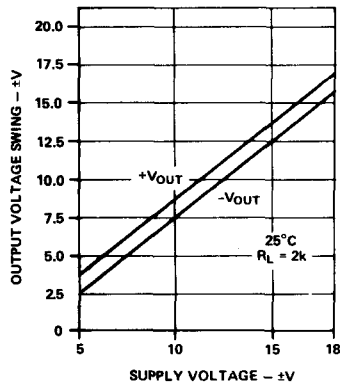


Figure 2. Output Swing

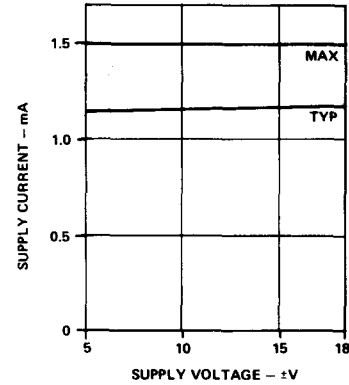


Figure 5. Supply Current

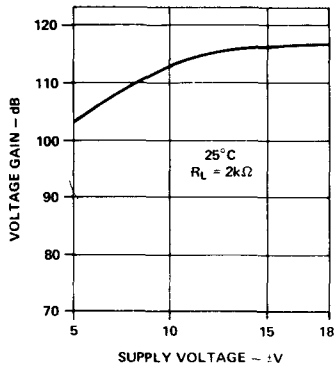


Figure 3. Voltage Gain

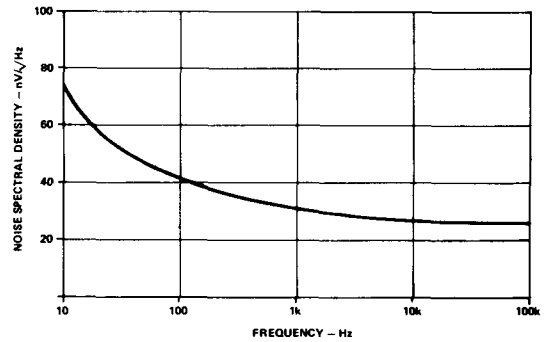


Figure 6. Input Noise Voltage, Spectral Density

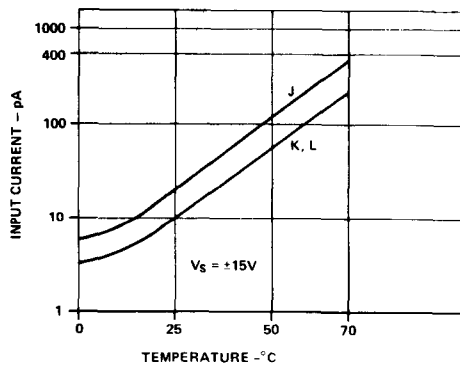


Figure 4a. Input Current vs. Temperature

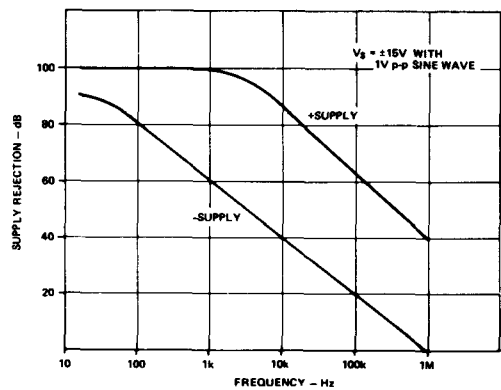


Figure 7. Power Supply Rejection



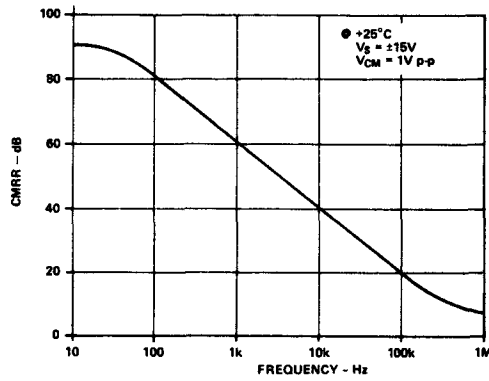


Figure 8. Common Mode Rejection

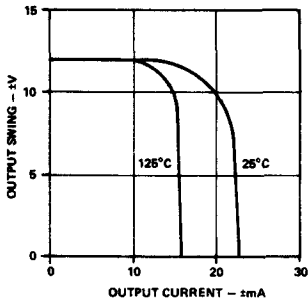


Figure 9. Current Limiting

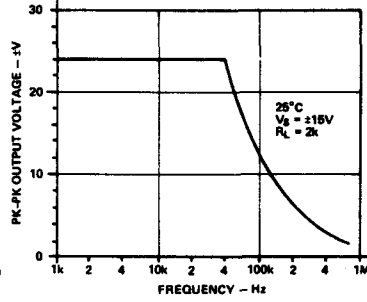


Figure 10. Large Signal Frequency Response

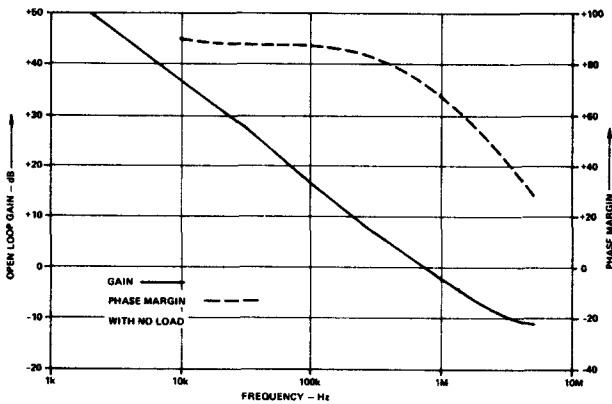


Figure 11. Open Loop Frequency Response

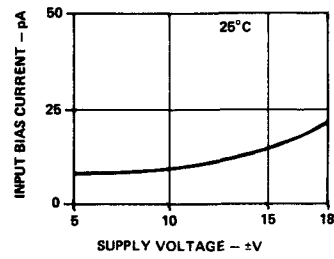


Figure 12. Input Bias Current vs. Supply Voltage

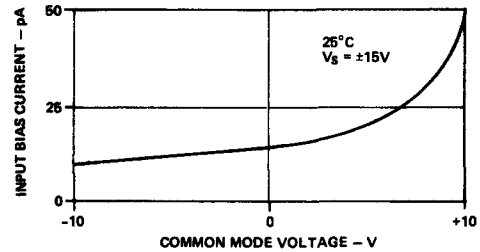


Figure 13. Input Bias Current vs. CMV

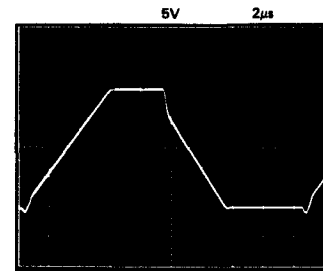


Figure 14a. Unity Gain Follower Pulse Response

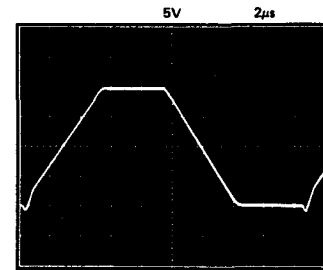


Figure 14b. Unity Gain Inverter Pulse Response

## APPLICATION

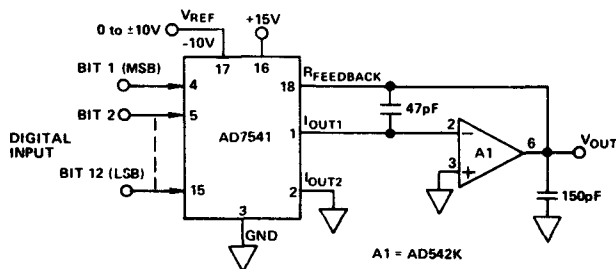


Figure 15a. AD542 Used as DAC Output Amplifier

$V_{REF}$  IN, 20V P-P, 33kHz  
 10V/DIV VERT, 5µs/DIV HORIZ.  
 $V_{OUT}$ , 5V/DIV VERT  
 5µs/DIV HORIZ.  
 SETTLING TIME: 15µs TO  
 0.01% ON 20V STEP

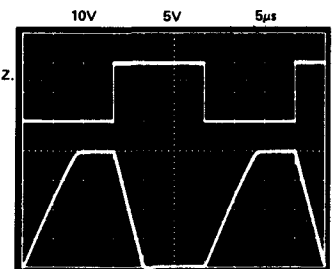


Figure 15b. Voltage Output DAC Settling Characteristic

The 1MHz bandwidth and low offset of the AD542 make it an excellent choice as an output amplifier for current-output D/A converters such as the AD7541, 12-bit CMOS DAC (1.8mV of amplifier offset could result in non-monotonic operation).

The photo above shows the output of the circuit of Figure 15a. The upper trace represents the reference input, and the bottom trace shows the output voltage for a digital input of all ones on the DAC. The 47pF capacitor across the feedback resistor compensates for the DAC output capacitance, and the 150pF load capacitor serves to minimize output glitches.

## PRELIMINARY TECHNICAL DATA

### FEATURES

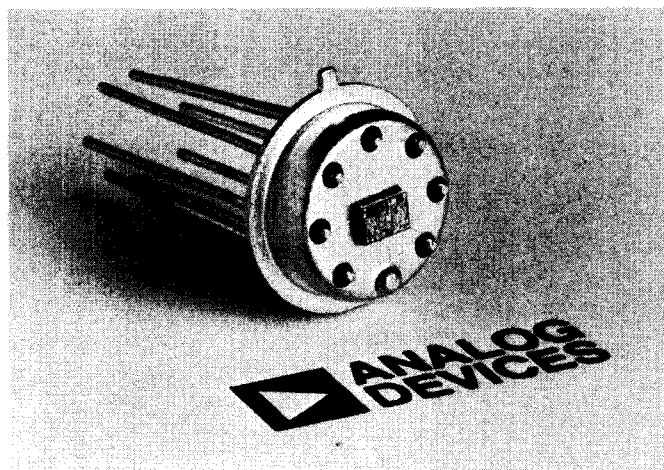
- Low Bias Current: 25pA max, warmed-up
- Low Offset Voltage: 500 $\mu$ V max
- Low Offset Voltage Drift: 5 $\mu$ V/ $^{\circ}$ C max
- Low Input Voltage Noise: 2 $\mu$ V p-p
- Low Quiescent Current: 2.8mA max
- High Slew Rate: 15V/ $\mu$ s
- Fast Settling to  $\pm$ 0.01%: 3 $\mu$ s

### PRODUCT DESCRIPTION

The AD544 is a high speed monolithic FET-input operational amplifier fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD544 offers bias currents significantly lower than currently available monolithic FET-input devices: 25pA max, warmed-up for the AD544K and L, 50pA max for the AD544J. In addition, the offset voltage is laser trimmed to less than 0.5mV on the AD544L and 1.0mV on the AD544K utilizing Analog's exclusive laser-wafer-trimming (LWT) process. When combined with the AD544's low offset voltage drift (5 $\mu$ V/ $^{\circ}$ C max for "L", 10 $\mu$ V/ $^{\circ}$ C max for "K"), these features offer the user IC performance truly superior to existing FET-input op amps—and at low, monolithic pricing.

The key technology required for monolithic JFET-input op amps is the ion-implanted JFET. Ion-implantation (as opposed to diffusion) permits the fabrication of precision, matched JFET's on a monolithic bipolar chip. Analog Devices optimizes the process to produce bias currents lower than other popular FET-input op amps and specifies each device for the maximum value at either input in the fully warmed-up condition. Additional benefits of this optimization include low voltage noise (2 $\mu$ V p-p, 0.1–10Hz), and low quiescent current.

The AD544 is recommended for any operational amplifier application requiring excellent ac and dc performance at low costs. Precision instrument front ends requiring accurate amplification of millivolt level signals from megohm source impedances will benefit from the device's excellent combination of low offset voltage and drift, low bias current and low 1/f noise. High common mode rejection (80dB, min on the "K" and "L" versions) and open-loop gain ensures better than "12-bit" linearity in high impedance buffer applications. Additionally, bandwidth and slew rate are greatly increased over presently available precision, bipolar op amps.



The AD544 is available in three versions: the "J", "K" and "L", all specified over the 0 to +70 $^{\circ}$ C temperature range and one version, "S", over the -55 $^{\circ}$ C to +125 $^{\circ}$ C operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

### PRODUCT HIGHLIGHTS

1. Improved bipolar and JFET processing on the AD544 results in the lowest bias current available in a high speed monolithic FET op amp.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD544 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max (AD544L), thus eliminating the need for external nulling in many situations.
4. If offset nulling is required, the additional offset voltage drift induced will be minimal. (Offset voltage drift can increase an additional 3 $\mu$ V/ $^{\circ}$ C per mV of offset nulled.)
5. Low voltage noise (2 $\mu$ V, p-p), and low offset voltage drift enhance the AD544's performance as a precision op amp.
6. The 2.5mA max quiescent current enables the device to be used in numerous portable applications where low battery drain is essential. This is achieved without sacrificing open loop gain or the ability to drive up to a 10mA load.
7. The high slew rate (13.0V/ $\mu$ s) and fast settling time to 0.01% (3.0 $\mu$ s) make the AD544 ideal for D/A, A/D, sample-and-hold circuits and high speed integrators.

# SPECIFICATIONS (typical @ +25°C and $V_S = \pm 15V$ dc unless otherwise specified)

| MODEL  | AD544J                             | AD544K                             | AD544L                            | AD544S <sup>1</sup>     |
|--|------------------------------------|------------------------------------|-----------------------------------|-------------------------|
| <b>OPEN LOOP GAIN<sup>2</sup></b>                    |                                    |                                    |                                   |                         |
| $V_{OUT} = \pm 10V, R_L \geq 2k\Omega$               | 30,000 min                         | 50,000 min                         | **                                | **                      |
| $T_A = \text{min to max } R_L = 2k\Omega$            | 20,000 min                         | 40,000 min                         | **                                | *                       |
| <b>OUTPUT CHARACTERISTICS</b>                        |                                    |                                    |                                   |                         |
| Voltage @ $R_L = 2k\Omega, T_A = \text{min to max}$  | $\pm 10V$ min ( $\pm 12V$ typ)     | *                                  | *                                 | *                       |
| Voltage @ $R_L = 10k\Omega, T_A = \text{min to max}$ | $\pm 12V$ min ( $\pm 13V$ typ)     | *                                  | *                                 | *                       |
| Short Circuit Current                                | 25mA                               | *                                  | *                                 | *                       |
| <b>FREQUENCY RESPONSE</b>                            |                                    |                                    |                                   |                         |
| Unity Gain, Small Signal                             | 2.0MHz                             | *                                  | *                                 | *                       |
| Full Power Response                                  | 200kHz                             | *                                  | *                                 | *                       |
| Slew Rate, Unity Gain                                | 15.0V/ $\mu s$ (5.0V/ $\mu s$ min) | 16.0V/ $\mu s$ (7.5V/ $\mu s$ min) | 17.0V/ $\mu s$ (10V/ $\mu s$ min) | **                      |
| <b>INPUT OFFSET VOLTAGE<sup>3</sup></b>              |                                    |                                    |                                   |                         |
| vs. Temperature                                      | 2.0mV max                          | 1.0mV max                          | 0.5mV max                         | **                      |
| vs. Supply, $T_A = \text{min to max}$                | 20 $\mu V/^\circ C$ max            | 10 $\mu V/^\circ C$ max            | 5 $\mu V/^\circ C$ max            | 15 $\mu V/^\circ C$ max |
| vs. Supply, $T_A = \text{min to max}$                | 200 $\mu V/V$ max                  | 100 $\mu V/V$ max                  | **                                | **                      |
| <b>INPUT BIAS CURRENT</b>                            |                                    |                                    |                                   |                         |
| Either Input <sup>4</sup>                            | 50pA max                           | 25pA max                           | **                                | **                      |
| Input Offset Current                                 | 5pA                                | 2pA                                | **                                | **                      |
| <b>INPUT IMPEDANCE</b>                               |                                    |                                    |                                   |                         |
| Differential   | 10 <sup>10</sup> $\Omega    2pF$   | *                                  | *                                 | *                       |
| Common Mode  | 10 <sup>11</sup> $\Omega    2pF$   | *                                  | *                                 | *                       |
| <b>INPUT VOLTAGE RANGE</b>                           |                                    |                                    |                                   |                         |
| Differential <sup>5</sup>                            | $\pm 20V$                          | *                                  | *                                 | *                       |
| Common Mode  | $\pm 10V$ min ( $\pm 12V$ typ)     | *                                  | *                                 | *                       |
| Common Mode Rejection, $V_{IN} = \pm 10V$            | 74dB min                           | 80dB min                           | **                                | **                      |
| <b>POWER SUPPLY</b>                                  |                                    |                                    |                                   |                         |
| Rated Performance                                    | $\pm 15V$                          | *                                  | *                                 | *                       |
| Operating  | $\pm (5 \text{ to } 18)V$          | *                                  | *                                 | *                       |
| Quiescent Current                                    | 2.5mA max (1.8mA typ)              | *                                  | *                                 | *                       |
| <b>VOLTAGE NOISE</b>                                 |                                    |                                    |                                   |                         |
| 0.1-10Hz   | 2 $\mu V$ p-p                      | *                                  | *                                 | *                       |
| 10Hz   | 35nV/ $\sqrt{Hz}$                  | *                                  | *                                 | *                       |
| 100Hz  | 22nV/ $\sqrt{Hz}$                  | *                                  | *                                 | *                       |
| 1kHz   | 18nV/ $\sqrt{Hz}$                  | *                                  | *                                 | *                       |
| 10kHz  | 16nV/ $\sqrt{Hz}$                  | *                                  | *                                 | *                       |
| <b>TEMPERATURE RANGE</b>                             |                                    |                                    |                                   |                         |
| Operating, Rated Performance                         | 0 to +70°C                         | *                                  | *                                 | -55°C to +125°C         |
| Storage  | -65°C to +150°C                    | *                                  | *                                 | *                       |

## NOTES:

<sup>1</sup> The AD537S/883B is an AD537S which is inspected and processed to the full requirements of MIL-STD-883, Level B. A complete listing of the tests is available on request.

<sup>2</sup> Open Loop Gain is specified with  $V_{OS}$  both nulled and unnulled.

<sup>3</sup> Input Offset Voltage specifications are guaranteed after 5 minutes of operation at  $T_A = +25^\circ C$ .

<sup>4</sup> Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at  $T_A = +25^\circ C$ . For higher temperatures, the current doubles every 10°C.

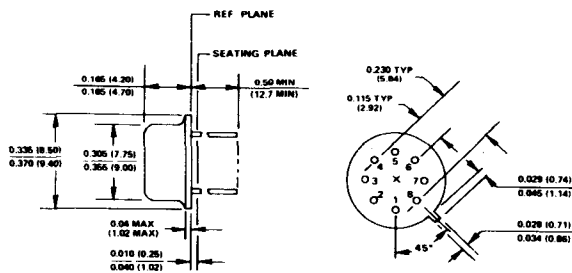
<sup>5</sup> Defined as voltage between inputs, such that neither exceeds  $\pm 10V$  from ground.

\* Specifications same as AD544J.  
\*\* Specifications same as AD544K.

Specifications and prices subject to change without notice.

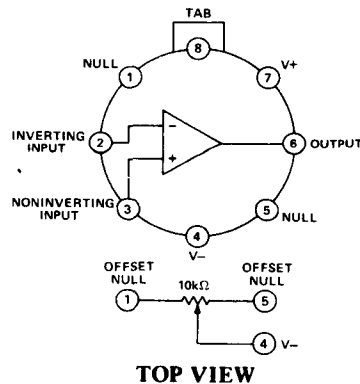
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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## PIN CONFIGURATION



TOP VIEW

# Typical Performance Curves

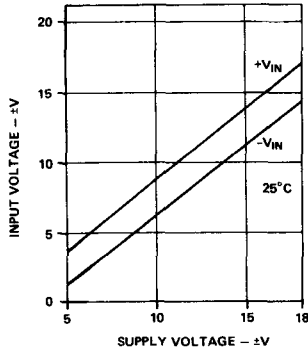


Figure 1. Input Voltage Range

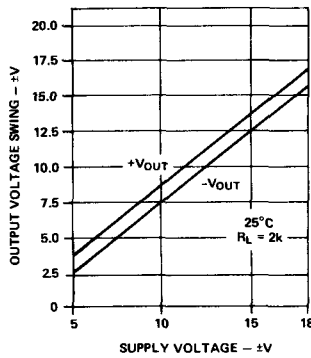


Figure 2. Output Swing

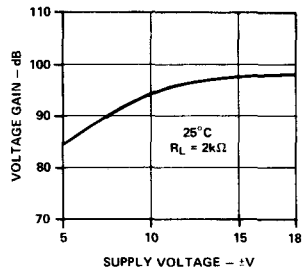


Figure 3. Voltage Gain

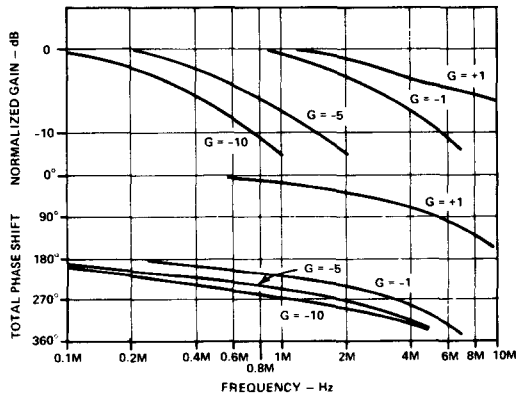


Figure 4. Closed Loop Gain & Phase vs. Frequency

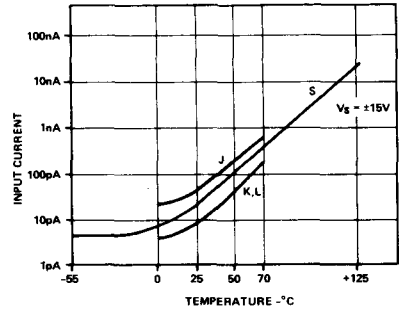


Figure 5. Input Current vs. Temperature

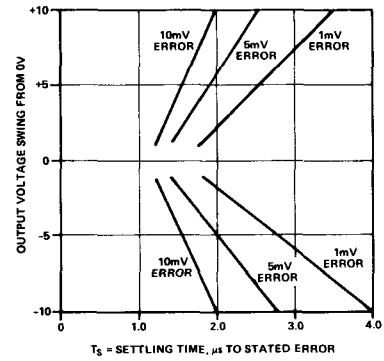


Figure 6. Output Settling Time vs. Output Swing and Error (Circuit of Figure 15a)

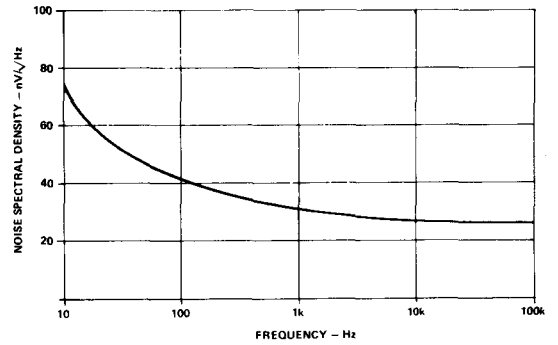


Figure 7. Input Noise Voltage Spectral Density

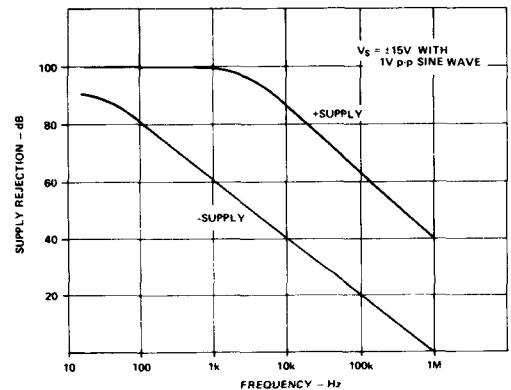


Figure 8. Power Supply Rejection

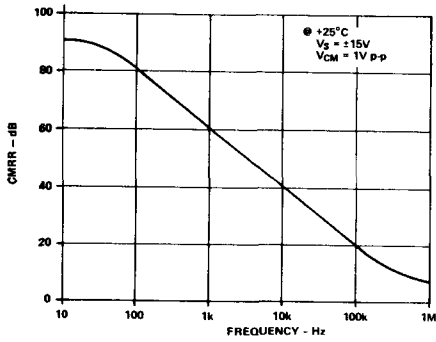


Figure 9. Common Mode Rejection

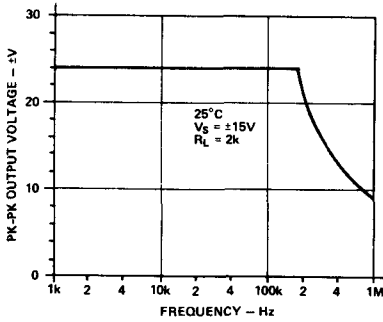


Figure 10. Large Signal Frequency Response

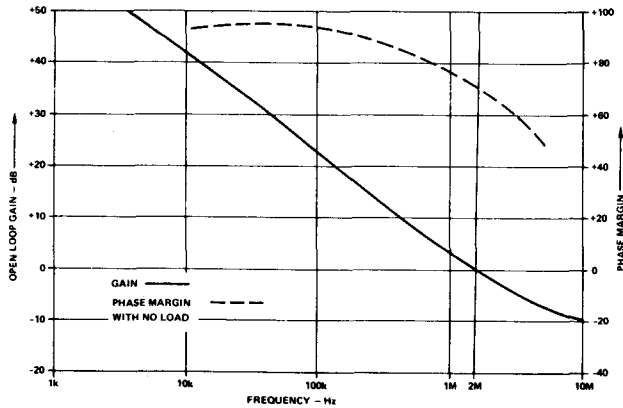


Figure 11. Open Loop Frequency Response

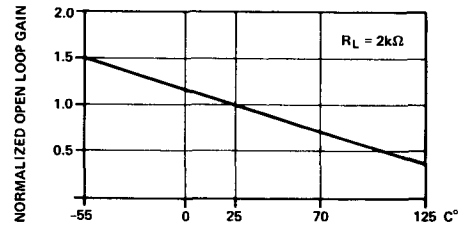


Figure 12. Open Loop Gain vs. Temperature

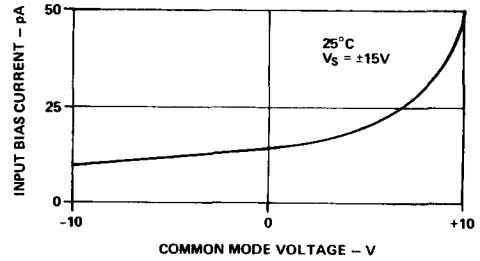


Figure 13. Input Bias Current vs. CMV

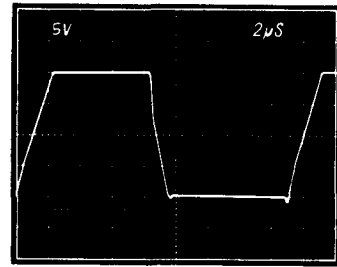


Figure 14a. Unity Gain Follower Pulse Response

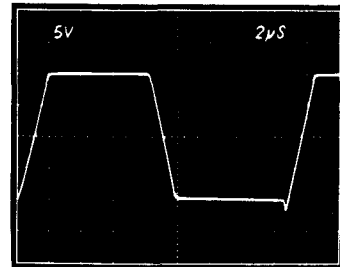


Figure 14b. Unity Gain Inverter Pulse Response

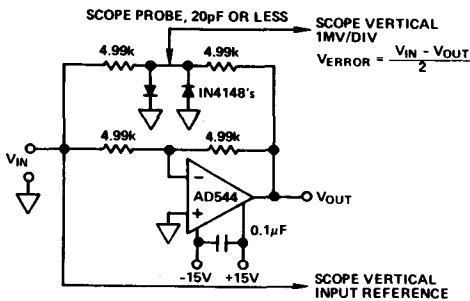


Figure 15a. Settling Times Test Circuit

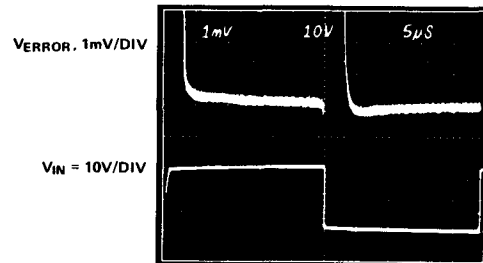


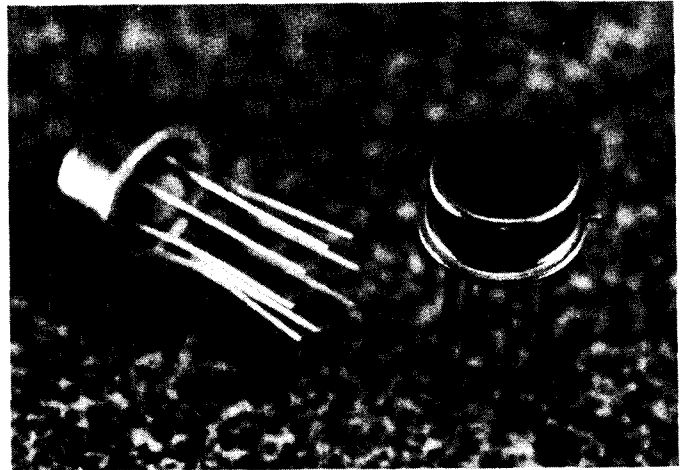
Figure 15b. Settling Characteristic Detail

The fast settling time ( $3.0\mu\text{s}$  to 0.01% for 20V p-p step) and low offset voltage make it an excellent choice as an output amplifier for current output D/A converters such as the AD565.

The upper trace of the oscilloscope photograph of Figure 15b shows the settling characteristic of the AD544. The lower trace represents the input to Figure 15a. The AD544 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain the optimum settling time.

**FEATURES**

- Low Offset Voltage:** 0.5mV max (AD545L), 0.25mV max (AD545M)
- Low Offset Voltage Drift:** 5 $\mu$ V/ $^{\circ}$ C max (AD545L), 3 $\mu$ V/ $^{\circ}$ C max (AD545M)
- Low Power:** 1.5mA max
- Low Bias Current:** 1pA max (AD545K, L, M)
- Low Noise:** 3 $\mu$ V p-p, 0.1 to 10Hz
- Low Cost**

**PRODUCT DESCRIPTION**

The AD545 is a precision FET-input operational amplifier with overall performance far superior to the general purpose IC FET-input op amp. The device is fabricated using a low leakage FET paired with a low power op amp. Bias current is specified as 2pA max for the AD545J and 1pA max for the AD545K, L and M. Offset voltage is laser trimmed to 0.5mV max for the AD545L, 0.25mV max for the AD545M. All devices also feature low voltage noise and power consumption. The AD545 is internally compensated, short circuit protected and free of latch-up.

The AD545 series offers a broad combination of performance features previously unavailable from a single device. For precision applications the AD545M specifies a 0.25mV max offset voltage, 3 $\mu$ V/ $^{\circ}$ C max drift and 1pA max bias current. The AD545J, with a 1mV max offset voltage, 25 $\mu$ V/ $^{\circ}$ C max drift and 2pA max bias current, is the best price performance choice at \$5.95 in 100's.

These devices are recommended for a variety of general purpose and precision applications requiring low bias currents and high input impedance such as pH/plon sensitive electrodes, photo-current detectors, biological microprobes, long term precision integrators and vacuum iongauge measurements. The versatility of the AD545 is further enhanced by its excellent low frequency noise (3 $\mu$ V p-p, 0.1 to 10Hz) and low power consumption (1.5mA max) for portable applications.

As with previous electrometer amplifier designs from Analog Devices, the case is guarded thus minimizing stray leakage. This feature will also shield the input circuitry from external noise and supply transients, as well as reducing common mode input capacitance from 0.8pF to 0.2pF.

The AD545 is available in four versions of bias current and offset voltage, the "J", "K", "L", and "M". All are specified from 0 to +70 $^{\circ}$ C and supplied in a hermetically sealed TO-99 package.

**PRODUCT HIGHLIGHTS**

1. The offset voltage on the AD545 is laser trimmed to a level typically less than 250 $\mu$ V. Offset voltage drift is significantly lower than previously available FET-input devices (3 $\mu$ V/ $^{\circ}$ C max for the AD545M). If additional external nulling is desired, the effect on drift is minimal (approximately 3 $\mu$ V/ $^{\circ}$ C per millivolt, nulled).
2. Bias current is specified as the maximum measured at either input with the device fully warmed up on  $\pm$ 15V supplies at +25 $^{\circ}$ C ambient.
3. The low quiescent current drain of 0.8mA typical, and 1.5mA max, is among the lowest of any IC op amp and keeps self heating to a minimum.
4. The combination of low input noise voltage and very low input noise current is such that for source impedances from much over one megohm up to 10<sup>11</sup> ohm, the Johnson noise of the source will easily dominate the noise characteristics.
5. Every AD545 is subjected to temperature cycling and a high G shock test prior to final test to insure reliability and long-term stability.

# SPECIFICATIONS (typical @ +25°C with $V_S = \pm 15V$ dc, unless otherwise specified)

| MODEL  | AD545J  | AD545K                              | AD545L                             | AD545M                             |
|--|---|-------------------------------------|------------------------------------|------------------------------------|
| <b>OPEN LOOP GAIN<sup>1</sup></b>                      |   |                                     |                                    |                                    |
| $V_{OUT} = \pm 10V$ , $R_L \geq 2k\Omega$              | 20,000V/V min                                     | 40,000V/V min                       | 40,000V/V min                      | 40,000V/V min                      |
| $R_L \geq 10k\Omega$                                   | 40,000V/V min                                     | 50,000V/V min                       | 50,000V/V min                      | 50,000V/V min                      |
| $T_A = \text{min to max}$ , $R_L \geq 2k\Omega$        | 15,000V/V min                                     | 25,000V/V min                       | 40,000V/V min                      | 40,000V/V min                      |
| <b>OUTPUT CHARACTERISTICS</b>                          |   |                                     |                                    |                                    |
| Voltage @ $R_L = 2k\Omega$ , $T_A = \text{min to max}$ | $\pm 10V$ min ( $\pm 12V$ typ)                    | *                                   | *                                  | *                                  |
| @ $R_L = 10k\Omega$ , $T_A = \text{min to max}$        | $\pm 12V$ min ( $\pm 13V$ typ)                    | *                                   | *                                  | *                                  |
| Load Capacitance <sup>2</sup>                          | 500pF   | *                                   | *                                  | *                                  |
| Short Circuit Current                                  | 10mA min (25mA typ)                               | *                                   | *                                  | *                                  |
| <b>FREQUENCY RESPONSE</b>                              |   |                                     |                                    |                                    |
| Unity Gain, Small Signal                               | 700kHz  | *                                   | *                                  | *                                  |
| Full Power Response                                    | 5kHz min (16kHz typ)                              | *                                   | *                                  | *                                  |
| Slew Rate Inverting Unity Gain                         | 0.3V/ $\mu\text{s}$ min (1.0V/ $\mu\text{s}$ typ) | *                                   | *                                  | *                                  |
| Overload Recovery Inverting Unity Gain                 | 100 $\mu\text{s}$ max (16 $\mu\text{s}$ typ)      | *                                   | *                                  | *                                  |
| <b>INPUT OFFSET VOLTAGE<sup>3</sup></b>                |   |                                     |                                    |                                    |
| vs. Temperature, $T_A = \text{min to max}$             | 1.0mV max   | 1.0mV max                           | 0.5mV max                          | 0.25mV max                         |
| vs. Supply, $T_A = \text{min to max}$                  | 25 $\mu\text{V}/^\circ\text{C}$ max               | 15 $\mu\text{V}/^\circ\text{C}$ max | 5 $\mu\text{V}/^\circ\text{C}$ max | 3 $\mu\text{V}/^\circ\text{C}$ max |
|  | 400 $\mu\text{V}/V$ max (50 $\mu\text{V}/V$ typ)  | 200 $\mu\text{V}/V$ max             | 200 $\mu\text{V}/V$ max            | 200 $\mu\text{V}/V$ max            |
| <b>INPUT BIAS CURRENT</b>                              |   |                                     |                                    |                                    |
| Either Input <sup>4</sup>                              | 2pA max   | 1pA max                             | 1pA max                            | 1pA max                            |
| <b>INPUT IMPEDANCE</b>                                 |   |                                     |                                    |                                    |
| Differential   | 1.6pF  10 <sup>13</sup> $\Omega$                  | *                                   | *                                  | *                                  |
| Common Mode  | 0.8pF  10 <sup>15</sup> $\Omega$                  | *                                   | *                                  | *                                  |
| <b>INPUT NOISE</b>                                     |   |                                     |                                    |                                    |
| Voltage, 0.1Hz to 10Hz                                 | 3.0 $\mu\text{V}$ (p-p)                           | *                                   | *                                  | 5 $\mu\text{V}$ (p-p) max          |
| f = 10Hz   | 55nV/ $\sqrt{\text{Hz}}$                          | *                                   | *                                  | *                                  |
| f = 100Hz  | 45nV/ $\sqrt{\text{Hz}}$                          | *                                   | *                                  | *                                  |
| f = 1kHz   | 35nV/ $\sqrt{\text{Hz}}$                          | *                                   | *                                  | *                                  |
| Current, 0.1 to 10Hz                                   | 0.01pA (p-p)                                      | *                                   | *                                  | *                                  |
| 10Hz to 10kHz  | 0.03pA rms  | *                                   | *                                  | *                                  |
| <b>INPUT VOLTAGE RANGE</b>                             |   |                                     |                                    |                                    |
| Differential   | $\pm 20V$ min                                     | *                                   | *                                  | *                                  |
| Common Mode, $T_A = \text{min to max}$                 | $\pm 10V$ min ( $\pm 12V$ typ)                    | *                                   | *                                  | *                                  |
| Common Mode Rejection, $V_{IN} = \pm 10V$              | 66dB min (80dB typ)                               | 70dB min                            | 76dB min                           | 76dB min                           |
| Maximum Safe Input Voltages <sup>5</sup>               | $\pm V_S$   | *                                   | *                                  | *                                  |
| <b>POWER SUPPLY</b>                                    |   |                                     |                                    |                                    |
| Rated Performance                                      | $\pm 15V$ typ                                     | *                                   | *                                  | *                                  |
| Operating  | $\pm 5V$ min ( $\pm 18V$ max)                     | *                                   | *                                  | *                                  |
| Quiescent Current                                      | 1.5mA max (0.8mA typ)                             | *                                   | *                                  | *                                  |
| <b>TEMPERATURE</b>                                     |   |                                     |                                    |                                    |
| Operating, Rated Performance                           | 0 to +70°C  | *                                   | *                                  | *                                  |
| Storage  | -65°C to +150°C                                   | *                                   | *                                  | *                                  |

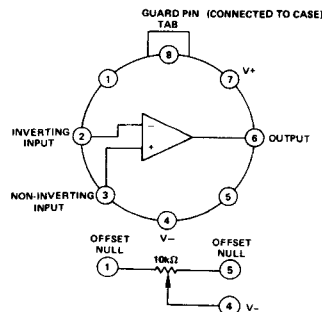
\*Specifications same as AD545J.

## NOTES

- Open Loop Gain is specified with or without nulling of  $V_{OS}$ .
- A conservative design would not exceed 500pF of load capacitance.
- Input Offset Voltage specifications are guaranteed after 5 minutes of operation at  $T_A = +25^\circ\text{C}$ .
- Bias Current specifications are guaranteed after 5 minutes of operation at  $T_A = +25^\circ\text{C}$ . For higher temperatures, the current doubles every +10°C.
- If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can handle overload currents of 0.5mA indefinitely without damage.

Specifications and prices subject to change without notice.

## PIN CONFIGURATION



TOP VIEW

## LAYOUT AND CONNECTION CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading.
2. The use of guarding techniques is essential to realizing the capability of the low input currents of the AD545. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation, and hence, no leakage. The guard will also act as a shield to reduce noise pickup and serves the additional function of reducing the effective capacitance to the input line. The case of the AD545 is brought out separately to pin 8 so that it can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry, and reduces common-mode input capacitance to about 0.2pF. Figure 10 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and non-inverting applications. If pin 8 is not used for guarding, it should be connected to ground or a power supply to reduce noise.
3. Printed circuit board layout and construction is critical in achieving low leakage performance. The best performance will be realized by using a teflon IC socket for the AD545 but at least a teflon stand-off should be used for the high-impedance lead. If this is not feasible, the input guarding scheme shown in Figure 10 will minimize leakage as much as possible and should be applied to both sides of the board. The guard ring is connected to a low impedance potential at

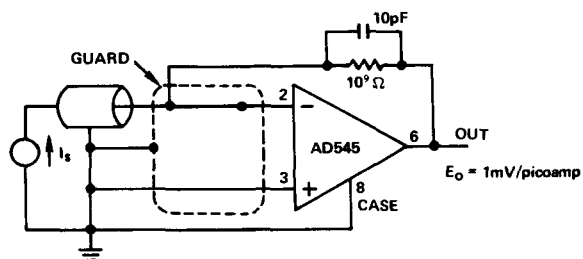


Figure 1. Picoampere Current-to-Voltage Converter Inverting Configuration

the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.

## APPLICATION NOTES

The AD545 offers one of the lowest input bias currents available in an integrated circuit package. Performing accurate measurements with this device requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD545 and extending its performance limits.

1. As with all junction FET input devices, the temperature of the FET's themselves is all-important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every  $10^{\circ}\text{C}$ ; therefore, every effort should be made to minimize device operating temperature.
2. The heat dissipation can be reduced initially by careful investigation of the application. First, if possible, reduce the required power supplies, since internal power consumption contributes the largest component of self-heating. The effects of this are shown in Figure 7, which shows typical input bias current and quiescent current versus supply voltage.
3. Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a  $2\text{k}\Omega$  load driven at 10 volts at the output will cause at least an additional 25 milliwatts dissipation in the output stage (and some in other stages) over the typical 24 milliwatts, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated; we recommend restricting the load impedance to be at least  $10\text{k}\Omega$ .

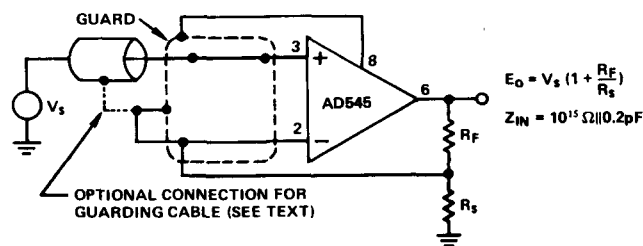


Figure 2. Very High Impedance Non-Inverting Amplifier



# Typical Performance Curves

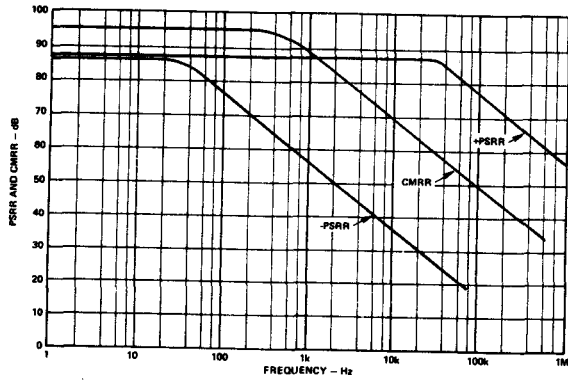


Figure 3. PSRR and CMRR Versus Frequency

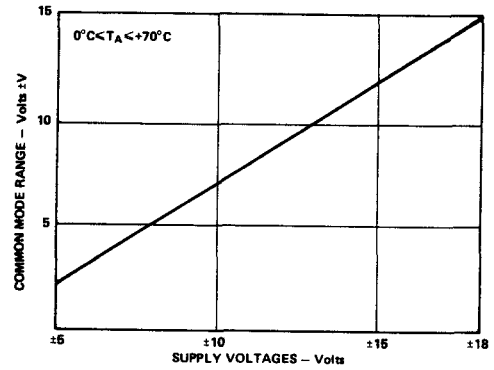


Figure 4. Input Common Mode Range Versus Supply Voltage

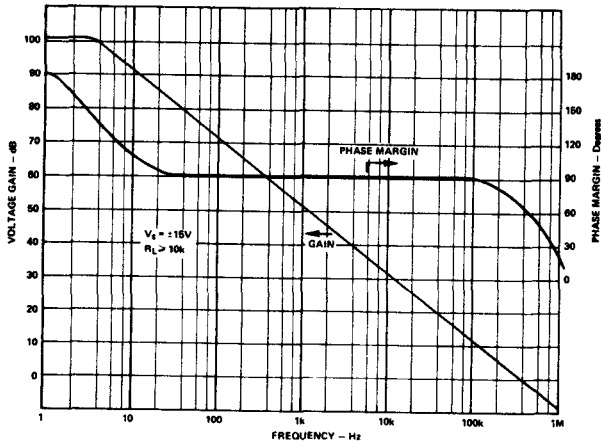


Figure 5. Open Loop Frequency Response

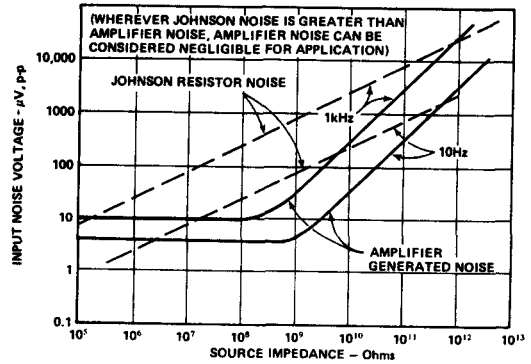


Figure 6. Peak-to-Peak Input Noise Voltage Versus Source Impedance and Bandwidth

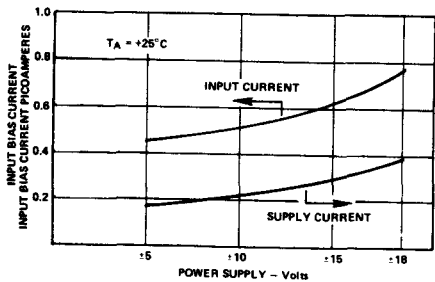


Figure 7. Input Bias Current and Supply Current Versus Supply Voltage

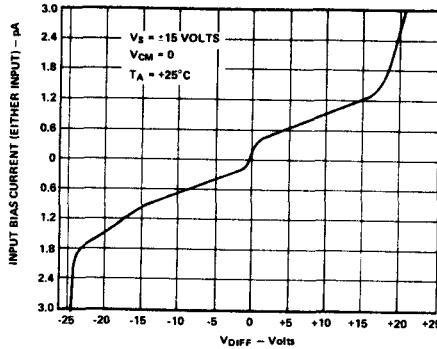


Figure 8. Input Bias Current Versus Differential Input Voltage

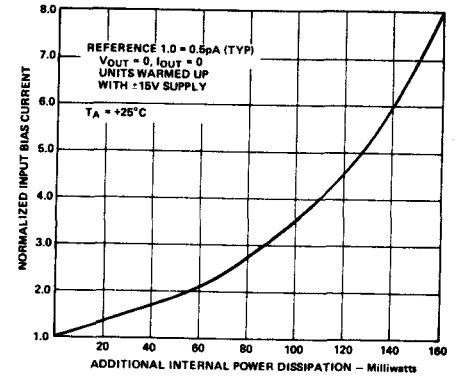


Figure 9. Input Bias Current Versus Additional Power Dissipation

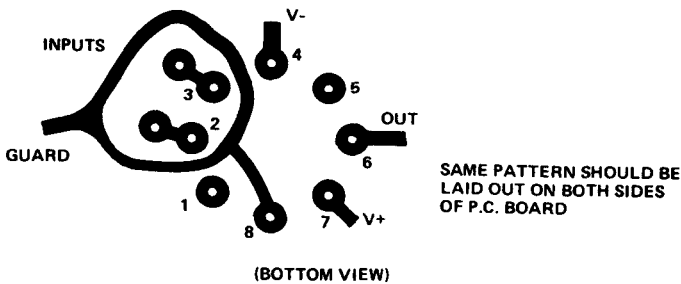
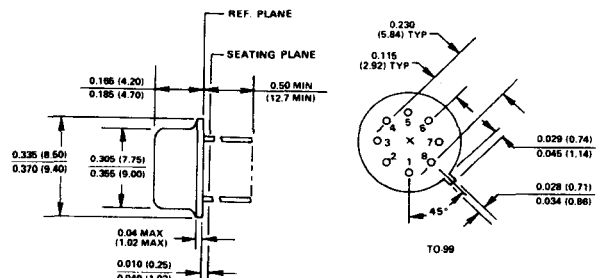


Figure 10. Board Layout for Guarding Inputs with Guarded TO-99 Package

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



### FEATURES

80ns Settling to 0.1%; 200ns Settling Time to 0.01%  
100MHz Gain Bandwidth Product  
55MHz 3dB Bandwidth  
100mA Output Capability @  $\pm 10V$   
Maximum Tempco of  $35\mu V/^\circ C$  (HOS-050A)

### APPLICATIONS

A to D Input Amplifier  
D to A Current Converter  
Video Pulse Amplifier  
CRT Deflection Amplifier  
Wideband Current Booster

### GENERAL DESCRIPTION

The HOS-050 and HOS-050A op amps are very high speed wideband operational amplifiers specially designed to complement the Analog Devices' line of high speed data acquisition products. Both models feature a 100MHz gain bandwidth product, slew rate of  $300\mu V/\mu s$  and settling time of 80ns to 0.1%.

Model HOS-050 has an input offset voltage of 25mV, typical; HOS-050A has an offset voltage of 10mV, typical. Both models have a rated output of  $\pm 100mA$ , min, and an exceptionally low input voltage noise of only  $7\mu V$  rms, dc to 2MHz, making them ideally suited for a broad range of video applications.

### D/A's AND FAST SETTLING

It used to be sufficient to specify op amps according to their slewing rates, bandwidth, and drive capability. Settling times were unimportant until the recent increase in the use of high speed video D/A converters. Since the conversion speed of D/A's can be limited by the settling time of the output amplifier, it has become essential to choose an op amp which will have a settling time which is compatible to the D/A.

Settling time is determined not only by the slew rate of an op amp, but also by the amount of overshoot and ringing experienced at the tail end of a step function change. This is largely due to the bandwidth limitations experienced in many op amps operating with closed loop gains greater than one. The HOS series avoids this problem since its 100MHz gain bandwidth product is more than large enough for most video applications.

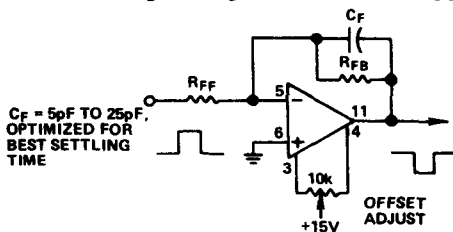
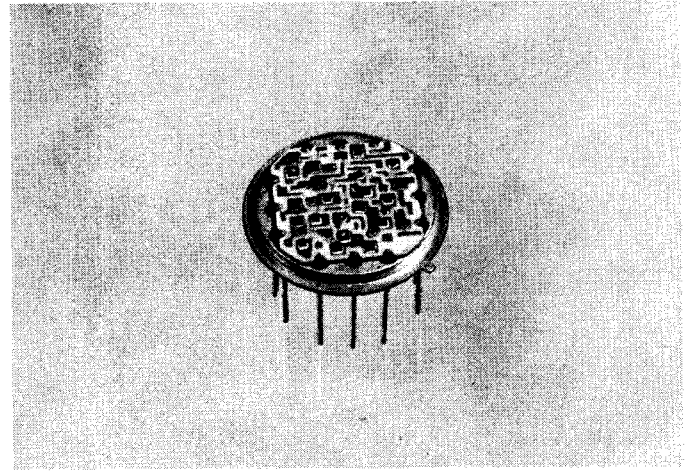


Figure 1. Settling Time Measurement



For example, at a gain of 1 in the inverting mode, it has a bandwidth of 55MHz and a settling time of 80ns to 0.1% for a 5-volt input step voltage.

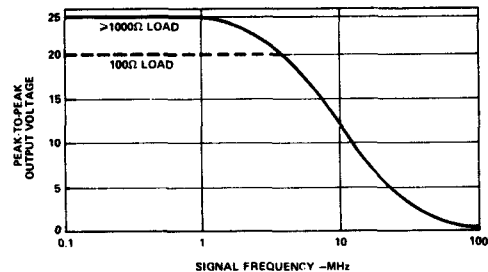


Figure 2. Output Voltage vs Signal Frequency

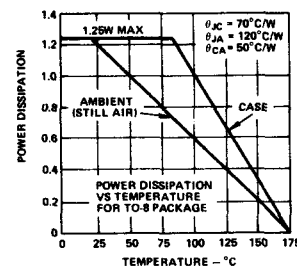


Figure 3. Power Dissipation vs Temperature

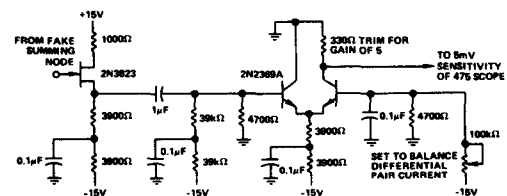


Figure 4. Settling Time Test Circuit for 0.01% Settling

For additional information on fast amplifiers, see Analog Devices' model 48, 50, 51 data sheets.

# SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise noted)

|   |   |
|---|---|
| <b>Model</b>  | HOS-050 (HOS-050A)  |
| <b>OPEN LOOP GAIN, DC</b><br>Load = 100Ω  | 100dB min   |
| <b>RATED OUTPUT<sup>1</sup></b><br>Voltage, $R_L \geq 100\Omega$<br>Current   | ±10V min<br>±100mA min  |
| <b>FREQUENCY RESPONSE</b> (Circuit of Figure 1)<br>Gain Bandwidth Product, $R_{FF} = R_{FB} = 500\Omega$<br>Small Signal Bandwidth, -3dB (See Table 1)<br>Full Power (See Figure 2 for 3% distortion levels)<br>Harmonic Distortion (See Table 2)<br>Slew Rate<br>Overload Recovery (50% overdrive) | 100MHz<br>55MHz<br>4MHz<br>-60dB<br>300V/μs<br>400ns                                    |
| <b>SETTLING TIME</b> to 0.1% Full Scale (See Table 3)<br>Inverting A = 1, $R_{FF} = R_{FB} = 500\Omega$<br>$V_{OUT} = \pm 5V/\pm 2.5V$<br>Noninverting A = 2, $R_{FF} = 500\Omega$ , $R_{FB} = 500\Omega$<br>$V_{OUT} = \pm 5V/\pm 2.5V$  | 100ns/80ns<br>200ns (135ns)   |
| <b>INPUT OFFSET VOLTAGE</b><br>Initial @ +25°C (adjustable to zero, see Figure 1)<br>vs. Temperature μV/°C<br>vs. Power Supply Voltage  | 35mV max (15mV max)<br>150 max (35 max)<br>±75μV/%                                      |
| <b>INPUT BIAS CURRENT</b><br>Initial @ +25°C<br>vs. Temperature   | 1mA typ, 2nA max<br>doubles/+10°C   |
| <b>INPUT IMPEDANCE</b><br>Differential<br>Common Mode   | 10 <sup>10</sup> Ω    5pF<br>10 <sup>10</sup> Ω    5pF                                  |
| <b>INPUT NOISE</b> ( $R_{FF} = 100\Omega$ , $R_{FB} = 1000\Omega$ )<br>dc to 100kHz<br>dc to 2MHz   | 5μV rms<br>7μV rms  |
| <b>INPUT VOLTAGE RANGE</b><br>Common Mode Voltage<br>Max Safe Differential Voltage<br>Common Mode Rejection   | ±10V min<br>±Supply Voltage<br>70dB   |
| <b>POWER SUPPLY</b><br>Voltage, Rated Performance<br>Voltage, Operating Range<br><br>Current, Quiescent max/typ<br>Power Consumption<br>Allowable Power Dissipation (See Figure 3)  | ±15V dc<br>±12V to ±18V<br>(Absolute max)<br>±25/±20mA<br>0.6W (quiescent)<br>1.25W max |
| <b>TEMPERATURE RANGE<sup>2</sup></b><br>Operating (See Figure 3 for derating)<br>Storage  | -55°C to +125°C (case)<br>-65°C to +150°C   |

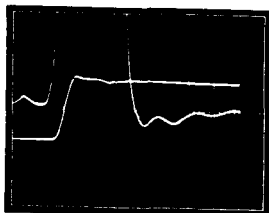
**NOTE**

<sup>1</sup> Output is short circuit protected for momentary shorts of 100ms or less.  
<sup>2</sup> With case temperature of +125°C, max junction temperature is +175°C.

Specifications subject to change without notice.

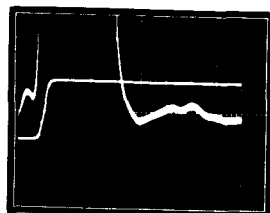
| $R_{FF}$ | $R_{FB}$ | Gain | Bandwidth |
|----------|----------|------|-----------|
| 500Ω     | 500Ω     | 1    | 55MHz     |
| 1000Ω    | 1000Ω    | 1    | 35MHz     |
| 500Ω     | 1000Ω    | 2    | 35MHz     |
| 250Ω     | 1000Ω    | 4    | 30MHz     |

Table 1.



5mV/DIV, 20ns/DIV

0.1% Settling, 5V Step



0.4mV/DIV, 50ns/DIV

0.01% Settling, 5V Step

## HARMONIC DISTORTION – INVERTING MODE

The following data are useful for video applications where driving a 50Ω or a 75Ω coax cable is desirable. It is assumed that the cable is source and load terminated. Therefore, a 50Ω cable represents a 100Ω load to the amplifier, and a 75Ω cable represents a 150Ω load.

|  |                                     |  |                                     |
|--|-------------------------------------|--|-------------------------------------|
| <b>Case I</b> DC load = 100Ω; Signal = 4MHz<br>Signal Output<br>2V p-p<br>4V p-p   | Harmonics<br>60dB down<br>55dB down | <b>Case IV</b> DC load = 150Ω; Signal = 5MHz<br>Signal Output<br>2V p-p<br>4V p-p  | Harmonics<br>60dB down<br>55dB down |
| <b>Case II</b> DC load = 150Ω; Signal = 4MHz<br>Signal Output<br>2V p-p<br>4V p-p  | Harmonics<br>65dB down<br>60dB down | <b>Case V</b> DC load = 1000Ω; Signal = 4MHz<br>Signal Output<br>2V p-p<br>4V p-p  | Harmonics<br>70dB down<br>60dB down |
| <b>Case III</b> DC load = 100Ω; Signal = 5MHz<br>Signal Output<br>2V p-p<br>4V p-p | Harmonics<br>60dB down<br>55dB down | <b>Case VI</b> DC load = 1000Ω; Signal = 5MHz<br>Signal Output<br>2V p-p<br>4V p-p | Harmonics<br>65dB down<br>55dB down |

Table 2. Harmonic Distortion – Inverting Mode

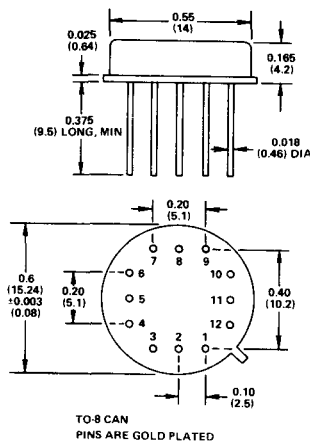
## P-P Output

| Voltage | to 1% FS | to 0.1% FS | to 0.05% FS | to 0.01% FS |
|---------|----------|------------|-------------|-------------|
| 10V     | 65ns     | 100ns      | 120ns       | 300ns       |
| 5V      | 50ns     | 80ns       | 90ns        | 200ns       |

Table 3. Settling Time – Inverting Mode (Measured with Gain of 1;  $R_{FF} = R_{FB} = 500\Omega$ )

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TO-8 CAN  
PINS ARE GOLD PLATED

## PIN DESIGNATIONS

| PINS | FUNCTION    |
|------|-------------|
| 1    | +V          |
| 2    | GROUND      |
| 3    | OFFSET ADJ* |
| 4    | OFFSET ADJ* |
| 5    | -INPUT      |
| 6    | +INPUT      |
| 7    | NC          |
| 8    | GROUND      |
| 9    | -V          |
| 10   | -V          |
| 11   | OUTPUT      |
| 12   | +V          |

\*PINS FOR CONNECTING OPTIONAL OFFSET POTENTIOMETER. SEE FIGURE 1.

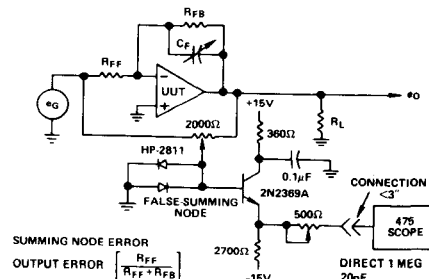


Figure 5. Settling Time Test Circuit for 0.1% Settling

## FEATURES

**Programmable Gains from 0.1 to 1000**  
**Differential Inputs**  
**High CMRR: 110dB min**  
**Complete Input Protection, Power ON and Power OFF**  
**Functionally Complete with the Addition of Two Resistors**  
**Internally Compensated**  
**Gain Bandwidth Product: 40MHz**  
**Output Current Limited: 25mA**  
**Extremely Low Cost**

## PRODUCT DESCRIPTION

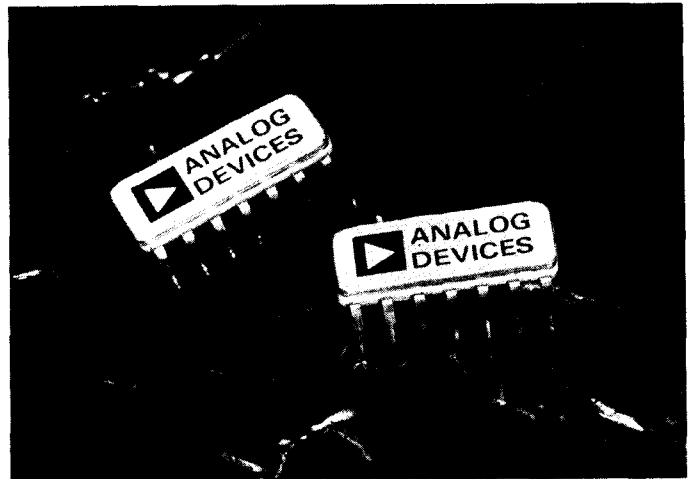
The AD521 is a second generation, low cost, monolithic IC instrumentation amplifier developed by Analog Devices. As a true instrumentation amplifier, the AD521 is a gain block with differential inputs and an accurately programmable input/output gain relationship.

The AD521 IC instrumentation amplifier should not be confused with an operational amplifier, although several manufacturers (including Analog Devices) offer op amps which can be used as building blocks in variable gain instrumentation amplifier circuits. Op amps are general-purpose components which, when used with precision-matched external resistors, can perform the instrumentation amplifier function.

An instrumentation amplifier is a precision differential voltage gain device optimized for operation in a real world environment, and is intended to be used wherever acquisition of a useful signal is difficult. It is characterized by high input impedance, balanced differential inputs, low bias currents and high CMR.

As a complete instrumentation amplifier, the AD521 requires only two resistors to set its gain to any value between 0.1 and 1000. The ratio matching of these resistors does not affect the high CMRR (up to 120dB) or the high input impedance ( $3 \times 10^9 \Omega$ ) of the AD521. Furthermore, unlike most operational amplifier-based instrumentation amplifiers, the inputs are protected against overvoltages up to  $\pm 15$  volts beyond the supplies.

The AD521 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "J" grade, the low drift "K" grade, and the lower drift, higher linearity "L" grade are specified from 0 to



+70°C. The "S" grade guarantees performance to specification over the full MIL-temperature range: -55°C to +125°C. All versions are packaged in a hermetic 14 pin DIP.

## PRODUCT HIGHLIGHTS

1. The AD521 is a true instrumentation amplifier in integrated circuit form, offering the user performance comparable to many modular instrumentation amplifiers at a fraction of the cost.
2. The AD521 is functionally complete with the addition of two resistors. Gain can be preset from 0.1 to more than 1000.
3. The AD521 is fully protected for input levels up to 15V beyond the supply voltages and 30V differential at the inputs.
4. Internally compensated for all gains, the AD521 also offers the user the provision for limiting bandwidth.
5. Offset nulling can be achieved with an optional trim pot.
6. The AD521 offers superior dynamic performance with a gain-bandwidth product of 40MHz, full peak response of 100kHz (independent of gain) and a settling time of 5 $\mu$ s to 0.1% of a 10V step.
7. Every AD521 is stabilization baked for 24 hours at +150°C and temperature cycled ten times from -65°C to +150°C, to ensure high reliability and excellent long-term stability.

# SPECIFICATIONS

(typical @  $V_S = \pm 15V$ ,  $R_L = 2k\Omega$  and  $T_A = 25^\circ C$  unless otherwise specified)

| MODEL  | AD521J   | AD521K  | AD521L                | AD521S                                |
|--|--|---|-----------------------|---------------------------------------|
| <b>GAIN</b>  |  |   |                       |                                       |
| Range (For Specified Operation, Note 1)  | 1 to 1000  | *   | *                     | *                                     |
| Equation   | $G = R_S/R_G V/V$                                  | *   | *                     | *                                     |
| Error from Equation  | ( $\pm 0.25 - 0.004G$ )%                           | *   | *                     | *                                     |
| Nonlinearity (Note 2)  |  | *   | *                     | *                                     |
| $1 < G \leq 1000$  | 0.2% max   | *   | 0.1% max              | *                                     |
| Gain Temperature Coefficient   | $\pm(3 \pm 0.05G)\text{ppm}/^\circ C$              | *   |                       | $\pm(15 \pm 0.4G)\text{ppm}/^\circ C$ |
| <b>OUTPUT CHARACTERISTICS</b>  |  |   |                       |                                       |
| Rated Output   | $\pm 10V, \pm 10mA$ min                            | *   | *                     | *                                     |
| Output at Maximum Operating Temperature  | $\pm 10V @ 5mA$ min                                | *   | *                     | *                                     |
| Impedance  | 0.1 $\Omega$                                       | *   | *                     | *                                     |
| <b>DYNAMIC RESPONSE</b>  |  |   |                       |                                       |
| Small Signal Bandwidth ( $\pm 3dB$ )   |  |   |                       |                                       |
| G = 1  | > 2MHz   | *   | *                     | *                                     |
| G = 10   | 300kHz   | *   | *                     | *                                     |
| G = 100  | 200kHz   | *   | *                     | *                                     |
| G = 1000   | 40kHz  | *   | *                     | *                                     |
| Small Signal, $\pm 1.0\%$ Flatness   |  |   |                       |                                       |
| G = 1  | 75kHz  | *   | *                     | *                                     |
| G = 10   | 26kHz  | *   | *                     | *                                     |
| G = 100  | 24kHz  | *   | *                     | *                                     |
| G = 1000   | 6kHz   | *   | *                     | *                                     |
| Full Peak Response (Note 3)  |  |   |                       |                                       |
| Slew Rate, $1 < G \leq 1000$   | 100kHz   | *   | *                     | *                                     |
| Settling Time (any 10V step to within 10mV of Final Value)                               | 10V/ $\mu s$                                       | *   | *                     | *                                     |
| G = 1  | 7 $\mu s$  | *   | *                     | *                                     |
| G = 10   | 5 $\mu s$  | *   | *                     | *                                     |
| G = 100  | 10 $\mu s$   | *   | *                     | *                                     |
| G = 1000   | 35 $\mu s$   | *   | *                     | *                                     |
| Differential Overload Recovery ( $\pm 30V$ Input to within 10mV of Final Value) (Note 4) |  |   |                       |                                       |
| G = 1000   | 50 $\mu s$   | *   | *                     | *                                     |
| Common Mode Step Recovery (30V Input to within 10mV of Final Value) (Note 5)             |  |   |                       |                                       |
| G = 1000   | 10 $\mu s$   | *   | *                     | *                                     |
| <b>VOLTAGE OFFSET (may be nulled)</b>  |  |   |                       |                                       |
| Input Offset Voltage ( $V_{OS1}$ )   |  |   |                       |                                       |
| vs. Temperature  | 3mV max (2mV typ)                                  | 1.5mV max (0.5mV typ)                             | 1.0mV max (0.5mV typ) | **                                    |
| vs. Supply   | $15\mu V/^\circ C$ max ( $7\mu V/^\circ C$ typ)    | $5\mu V/^\circ C$ max ( $1.5\mu V/^\circ C$ typ)  | $2\mu V/^\circ C$ max | **                                    |
| Output Offset Voltage ( $V_{OS0}$ )  | $3\mu V/\%$  | *   | *                     | *                                     |
| vs. Temperature  | 400mV max (200mV typ)                              | 200mV max (30mV typ)                              | 100mV max             | **                                    |
| vs. Supply (Note 6)  | $400\mu V/^\circ C$ max ( $150\mu V/^\circ C$ typ) | $150\mu V/^\circ C$ max ( $50\mu V/^\circ C$ typ) | $75\mu V/^\circ C$    | **                                    |
|  | $0.005V_{OS0}/\%$                                  | *   | *                     | *                                     |
| <b>INPUT CURRENTS</b>  |  |   |                       |                                       |
| Input Bias Current (either input)  |  |   |                       |                                       |
| vs. Temperature  | 80nA max   | 40nA max  | **                    | **                                    |
| vs. Supply   | $1nA/^\circ C$ max                                 | $500pA/^\circ C$ max                              | **                    | **                                    |
| Input Offset Current   | 2%/V   | *   | *                     | *                                     |
| vs. Temperature  | 20nA max   | 10nA max  | **                    | **                                    |
|  | $250pA/^\circ C$ max                               | $125pA/^\circ C$ max                              | **                    | **                                    |
| <b>INPUT</b>   |  |   |                       |                                       |
| Differential Input Impedance (Note 7)  |  |   |                       |                                       |
| Common Mode Input Impedance (Note 8)   | $3 \times 10^9 \Omega    1.8pF$                    | *   | *                     | *                                     |
| Input Voltage Range for Specified Performance (with respect to ground)                   | $6 \times 10^{10} \Omega    3.0pF$                 | *   | *                     | *                                     |
| Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9)       | $\pm 10V$  | *   | *                     | *                                     |
| Voltage at either input (Note 9)   | 30V  | *   | *                     | *                                     |
| Common Mode Rejection Ratio, DC to 60Hz with 1k $\Omega$ source unbalance                | $V_S \pm 15V$                                      | *   | *                     | *                                     |
| G = 1  | 70dB min (74dB typ)                                | 74dB min (80dB typ)                               | **                    | **                                    |
| G = 10   | 90dB min (94dB typ)                                | 94dB min (100dB typ)                              | **                    | **                                    |
| G = 100  | 100dB min (104dB typ)                              | 104dB min (114dB typ)                             | **                    | **                                    |
| G = 1000   | 100dB min (110dB typ)                              | 110dB min (120dB typ)                             | **                    | **                                    |
| <b>NOISE</b>   |  |   |                       |                                       |
| Voltage RTO (p-p) @ 0.1Hz to 10Hz (Note 10)  |  |   |                       |                                       |
| RMS RTO, 10Hz to 10kHz   | $\sqrt{(0.5G)^2 + (225)^2} \mu V$                  | *   | *                     | *                                     |
| Input Current, rms, 10Hz to 10kHz  | $\sqrt{(1.2G)^2 + (50)^2} \mu V$                   | *   | *                     | *                                     |
|  | 15pA (rms)   | *   | *                     | *                                     |
| <b>REFERENCE TERMINAL</b>  |  |   |                       |                                       |
| Bias Current   | 3 $\mu A$  | *   | *                     | *                                     |
| Input Resistance   | 10M $\Omega$                                       | *   | *                     | *                                     |
| Voltage Range  | $\pm 10V$  | *   | *                     | *                                     |
| Gain to Output   | 1  | *   | *                     | *                                     |
| <b>POWER SUPPLY</b>  |  |   |                       |                                       |
| Operating Voltage Range  | $\pm 5$ to $\pm 18$                                | *   | *                     | *                                     |
| Quiescent Supply Current   | 5mA max  | *   | *                     | *                                     |
| <b>TEMPERATURE RANGE</b>   |  |   |                       |                                       |
| Specified Performance  |  |   |                       |                                       |
| Operating  | 0 to $+70^\circ C$                                 | *   | *                     | $-55^\circ C$ to $+125^\circ C$       |
| Storage  | $-25^\circ C$ to $+85^\circ C$                     | *   | *                     | $-55^\circ C$ to $+125^\circ C$       |
|  | $-65^\circ C$ to $+150^\circ C$                    | *   | *                     | *                                     |

\*Specification same as AD521J.  
\*\*Specification same as AD521K.

Specifications and prices  
subject to change without notice.

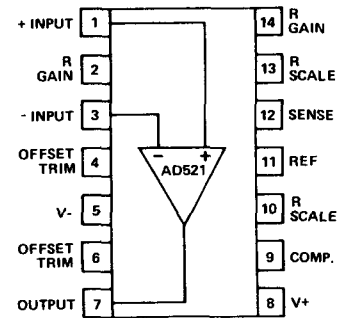
## NOTES:

- Gains below 1 and above 1000 are realized by simply adjusting the gain setting resistors. For best results, voltage at either input should be restricted to  $\pm 10V$  for gains equal to or less than 1.
- Nonlinearity is defined as the ratio of the deviation from the "best straight line" through a full scale output range of  $\pm 9$  volts. With a combination of high gain and  $\pm 10$  volt output swing, distortion may increase to as much as 0.3%.
- Full Peak Response is the frequency below which a typical amplifier will produce full output swing.
- Differential Overload Recovery is the time it takes the amplifier to recover from a pulsed 30V differential input with 15V of common mode voltage, to within 10mV of final value. The test input is a 30V, 10 $\mu$ s pulse at a 1kHz rate. (When a differential signal of greater than 11V is applied between the inputs, transistor clamps are activated which drop the excess input voltage across internal input resistors. If a continuous overload is maintained, power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as added thermal time constant, but will not damage the device.)
- Common Mode Step Recovery is the time it takes the amplifier to recover from a 30V common mode input with zero volts of differential signal to within 10mV of final value. The test input is 30V, 10 $\mu$ s pulse at a 1kHz rate. (When a common mode signal greater than  $V_S - 0.5V$  is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as an added thermal time constant, but will not damage the device.)

- Output Offset Voltage versus Power Supply Change is a constant 0.005 times the unnull'd output offset per percent change in either power supply. If the output offset is nulled, the output offset change versus supply change is substantially reduced.
- Differential Input Impedance is the impedance between the two inputs.
- Common Mode Input Impedance is the impedance from either input to the power supplies.
- Maximum Input Voltage (differential or at either input) is 30V when using  $\pm 15V$  supplies. A more general specification is that neither input may exceed either supply (even when  $V_S = 0$ ) by more than 15V and that the difference between the two inputs must not exceed 30V. (See also Notes 4 and 5.)
- 0.1Hz to 10Hz Peak-to-Peak Voltage Noise is defined as the maximum peak-to-peak voltage noise observed during 2 of 3 separate 10 second periods with the test circuit of Figure 10.

## DESIGN PRINCIPLE

Figure 3 is a simplified schematic of the AD521. A differential input voltage,  $V_{IN}$ , appears across  $R_G$  causing an imbalance in the currents through  $Q_1$  and  $Q_2$ ,  $\Delta I = V_{IN}/R_G$ . That imbalance is forced to flow in  $R_S$  because the collector currents of  $Q_3$  and  $Q_4$  are constrained to be equal by their biasing (current mirror). These conditions can only be satisfied if the differential voltage across  $R_S$  (and hence the output voltage of the



TOP VIEW

Figure 1. AD521 Pin Configuration

## TO-116

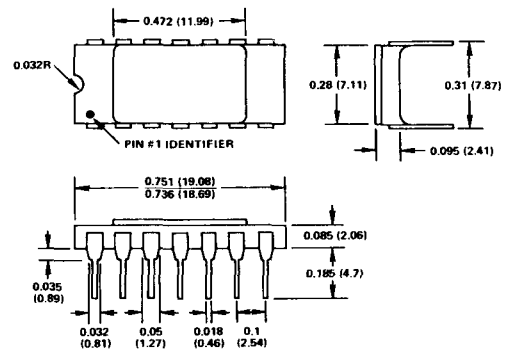


Figure 2. Physical Dimensions. Dimensions shown in inches and (mm).

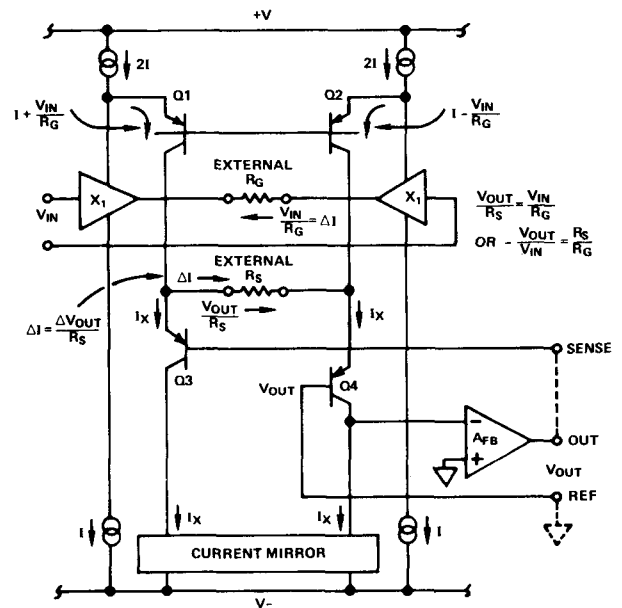


Figure 3. Simplified AD521 Schematic

AD521) is equal to  $\Delta I \times R_S$ . The feedback amplifier,  $A_{FB}$  performs that function. Therefore,  $V_{OUT} = \frac{V_{IN}}{R_G} \times R_S$  or  $\frac{V_{OUT}}{V_{IN}} = \frac{R_S}{R_G}$ .

## APPLICATION NOTES FOR THE AD521

These notes ensure the AD521 will achieve the high level of performance necessary for many diversified IA applications.

- Gains below 1 and above 1000 are realized by adjusting the gain setting resistors as shown in Figure 4 (the resistor,  $R_S$  between pins 10 and 13 should remain  $100k\Omega \pm 15\%$ , see application note 3). For best results, the input voltage should be restricted to  $\pm 10V$  especially for gain equal to or less than 1.
- Provide a return path to ground for input bias currents. The AD521 is an instrumentation amplifier, not an isolation amplifier. When using a thermocouple or other "floating" source, this return path may be provided directly to ground or indirectly through a resistor to ground from pins 1 and/or 3, as shown in Figure 5. If the return path is not provided, bias currents will cause the output to saturate. The value of the resistor may be determined by dividing the maximum allowable common mode voltage for the application by the bias current of the instrumentation amplifier.

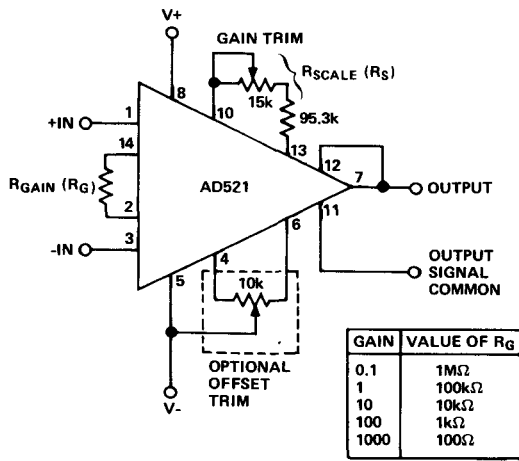
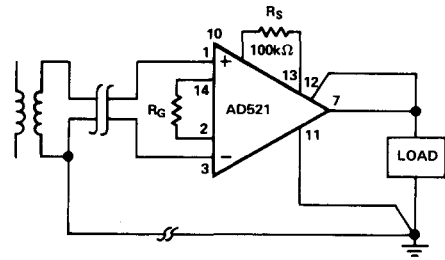
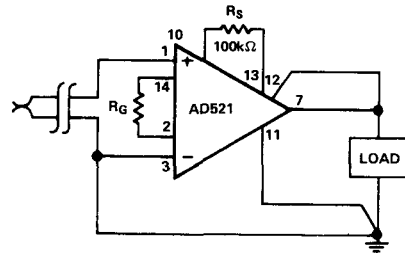


Figure 4. Operating Connections for AD521

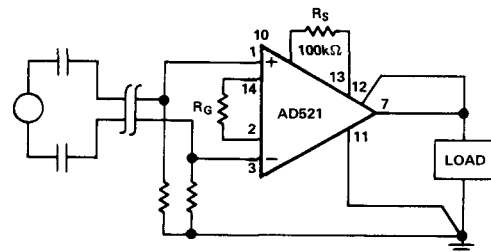
- The resistors between pins 10 and 13, ( $R_{SCALE}$ ) must equal  $100k\Omega \pm 15\%$  (Figure 4). If  $R_{SCALE}$  is too low (below  $85k\Omega$ ) the output swing of the AD521 is reduced. At values below  $80k\Omega$  and above  $120k\Omega$  the stability of the AD521 may be impaired.
- Do not exceed the allowable input signal range. The linearity of the AD521 decreases if the inputs are driven within 5 volts of the supply rails, particularly when the device is used at a gain less than 1. To avoid this possibility, attenuate the input signal through a resistive divider network and use the AD521 as a buffer, as shown in Figure 6. The resistor  $R/2$  matches the impedance seen by both AD521 inputs so that the voltage offset caused by bias currents will be minimized.



a). Transformer Coupled, Direct Return

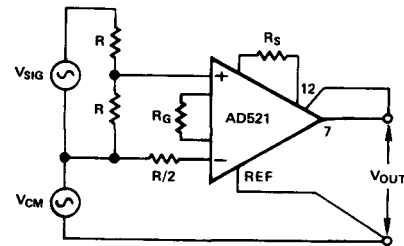


b). Thermocouple, Direct Return



c). AC Coupled, Indirect Return

Figure 5. Ground Returns for "Floating" Transducers



- INCREASE  $R_G$  TO PICK UP GAIN LOST BY R DIVIDER NETWORK
- INPUT SIGNAL MUST BE REDUCED IN PROPORTION TO POWER SUPPLY VOLTAGE LEVEL

Figure 6. Operating Conditions for  $V_{IN} \approx V_S = 10V$

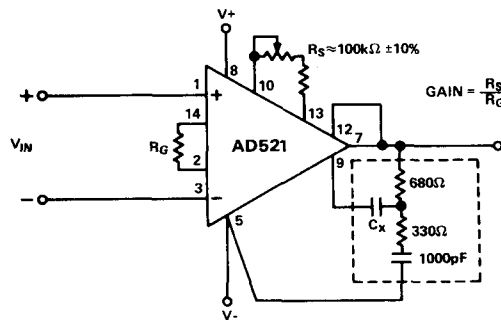
5. Use the compensation pin (pin 9) and the applicable compensation circuit when the amplifier is required to drive a capacitive load. It is worth mentioning that coaxial cables can "invisibly" provide such capacitance since many popular coaxial cables display capacitance in the vicinity of 30pF per foot.

This compensation (bandwidth control) feature permits the user to fit the response of the AD521 to the particular application as illustrated by Figure 7. In cases of extremely high load capacitance the compensation circuit may be changed as follows:

1. Reduce 680Ω to 24Ω
2. Reduce 330Ω to 7.5Ω
3. Increase 1000pF to 0.1μF
4. Set  $C_X$  to 1000pF if no compensation was originally used. Otherwise, do not alter the original value.

This allows stable operation for load capacitances up to 3000pF, but limits the slew rate to approximately 0.16V/μs.

6. Signals having frequency components above the Instrumentation Amplifier's output amplifier closed-loop bandwidth will be transmitted from V- to the output with little or no attenuation. Therefore, it is advisable to decouple the V-supply line to the output common or to pin 11.<sup>1</sup>



$$C_X = \frac{1}{100\pi f_t} \text{ when } f_t \text{ is the desired bandwidth.}$$

( $f_t$  in kHz,  $C_X$  in μF)

Figure 7. Optional Compensation Circuit

#### INPUT OFFSET AND OUTPUT OFFSET

When specifying offsets and other errors in an operational amplifier, it is often convenient to refer these errors to the inputs. This enables the user to calculate the maximum error he would see at the output with any gain or circuit configuration. An op amp with 1mV of input offset voltage, for example, would produce 1V of offset at the output in a gain of 1000 configuration.

In the case of an instrumentation amplifier, where the gain is controlled in the amplifier, it is more convenient to separate

errors into two categories. Those errors which simply add to the output signal and are unaffected by the gain can be classified as output errors. Those which act as if they are associated with the input signal, such that their effect at the output is proportional to the gain, can be classified as input errors.

As an illustration, a typical AD521 might have a +30mV output offset and a -0.7mV input offset. In a unity gain configuration, the total output offset would be +29.3mV or the sum of the two. At a gain of 100, the output offset would be -40mV or:  $30\text{mV} + 100(-0.7\text{mV}) = -40\text{mV}$ .

By separating these errors, one can evaluate the total error independent of the gain settings used, similar to the situation with the input offset specifications on an op amp. In a given gain configuration, both errors can be combined to give a total error referred to the input (R.T.I.) or output (R.T.O.) by the following formula:

$$\text{Total Error R.T.I.} = \text{input error} + (\text{output error/gain})$$

$$\text{Total Error R.T.O.} = (\text{Gain} \times \text{input error}) + \text{output error}$$

The offset trim adjustment (pins 4 and 6, Figure 4) is associated primarily with the output offset. At any gain it can be used to introduce an output offset equal and opposite to the input offset voltage multiplied by the gain. As a result, the total output offset can be reduced to zero.

As shown in Figure 8, the gain range on the AD521 can be extended considerably by adding an attenuator in the sense terminal feedback path (as well as adjusting the ratio,  $R_S/R_G$ ). Since the sense terminal is the inverting input to the output amplifier, the additional gain to the output is controlled by  $R_1$  and  $R_2$ . This gain factor is  $1 + R_2/R_1$ .

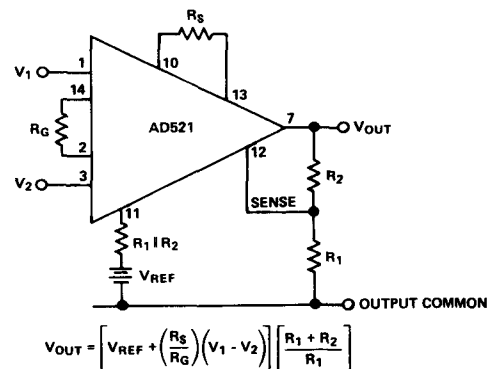


Figure 8. Circuit for utilizing some of the unique features of the AD521. Note that gain changes introduced by changing  $R_1$  and  $R_2$  will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

<sup>1</sup> For further details, refer to "An I.C. User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by A. Paul Brokaw. This application note is available from Analog Devices without charge upon request.



Where offset errors are critical, a resistor equal to the parallel combination of  $R_1$  and  $R_2$  should be placed between pin 11 and  $V_{REF}$ . This minimizes the offset errors resulting from the input current flowing in  $R_1$  and  $R_2$  at the sense terminal. Note that gain changes introduced by changing the  $R_1/R_2$  attenuator will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

When a predetermined output offset is desired,  $V_{REF}$  can be placed in series with pin 11. This offset is then multiplied by the gain factor  $1 + R_2/R_1$  as shown in the equation of Figure 8.

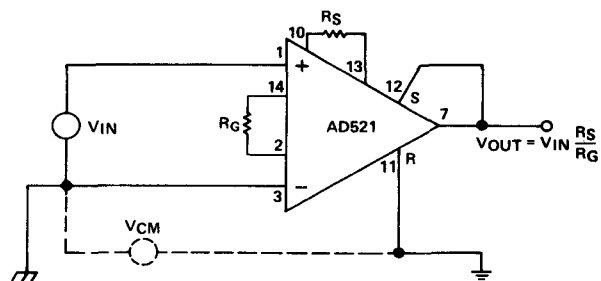


Figure 9. Ground loop elimination. The reference input, Pin 11, allows remote referencing of ground potential. Differences in ground potentials are attenuated by the high CMRR of the AD521.

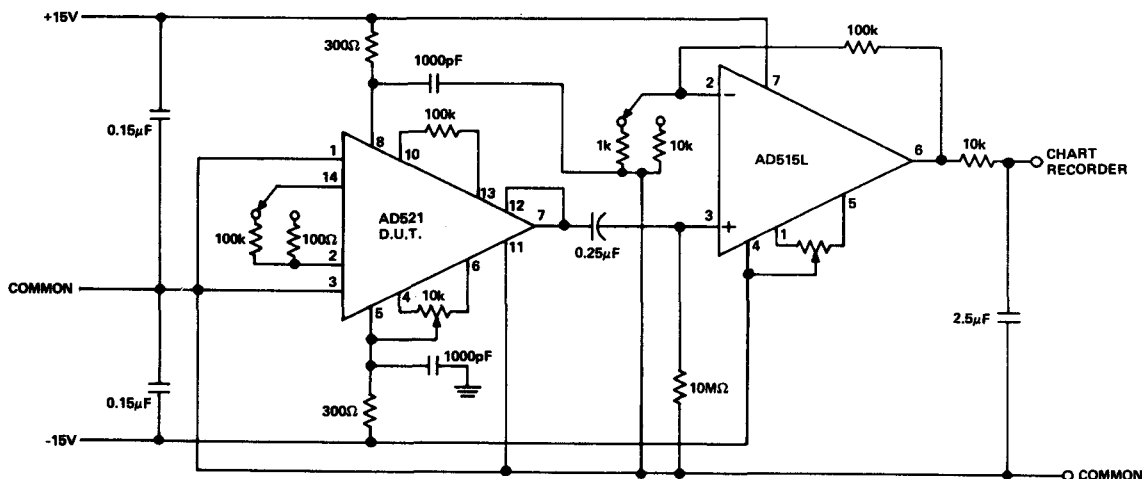


Figure 10. Test circuit for measuring peak to peak noise in the bandwidth 0.1Hz to 10Hz. Typical measurements are found by reading the maximum peak to peak voltage noise of the device under test (D.U.T.) for 3 observation periods of 10 seconds each.

### FEATURES

**Low Cost**

**Versatility: 3-Port Isolation**

**Multichannel**

**Adjustable Gain: 1 to 1,000V/V**

**Accuracy: Nonlinearity: 0.05% max (288K)**

**Low Gain Drift: 0.01%/°C max (288K)**

**Low Input Drift: 5μV/°C max (288K)**

**Single Supply Operation: +13.5V dc to +26V dc**

**High CMV Isolation: 850V dc**

### APPLICATIONS

**Transient Voltage Protection: Data Acquisition Systems**

**Isolated 10-Bit D/A Converters**

**Ground Loop Elimination: Industrial Process Control**

**Process Signal Isolator**

**Off-Ground Measurements**

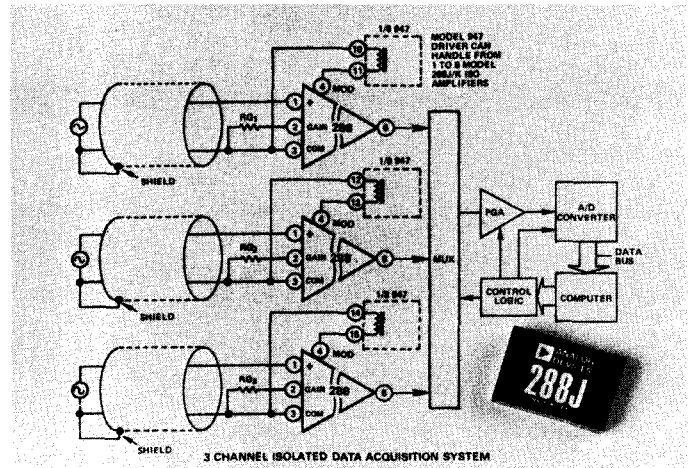
### GENERAL DESCRIPTION

Model 288 is an economy isolation amplifier offering both high accuracy, 0.05% (model 288K), and a unique transformer isolated, multichannel design with separate signal and modulator/demodulator modules. Designed for low level, multichannel industrial instrumentation and control applications, this new design can be applied to achieve 4-channel, 3-port isolated systems, or low cost 8-, 16- or 32-channel systems with complete input/output isolation and channel/channel isolation.

Available in two high accuracy selections, this design features guaranteed low nonlinearity, 0.05% max (model 288K), 0.1% max (model 288J) and guaranteed low gain drift, 100ppm/°C max (model 288K), 300ppm/°C max (model 288J). The low drift bipolar input stage, 5μV/°C max (288K), 10μV/°C max (288J), provides gain adjustment from 1 to 1,000V/V with a single external resistor. Front-end differential protection (850V dc, continuous) combined with high CMV (850V dc, continuous) and high CMR (92dB min @ 60Hz) facilitates low level precision measurements in the presence of harsh RFI. Model 288J/K will interrupt ground loops, leakage paths and high voltage transients to ±850V pk, providing dc to 3.5kHz (-3dB @ G = 1V/V) response.

### WHERE TO USE MODELS 288, 947, 948

Model 288 has been designed for multichannel data acquisition systems that have to handle dc sensor inputs such as thermocouples, strain gages and other low level signals in harsh industrial environments. Providing complete galvanic isolation and protection from line transients and fault voltages, model 288's low noise, high accuracy performance suggests applications such as process controllers, isolated 10-bit DAC's, current loop receivers, weighing systems, high CMV instrumentation and computer interface systems.



### DRIVER MODEL SELECTION

Model 288 requires external modulator and demodulator drive signals. Model 947 and 948 are available for driving up to 8 model 288J/K isolation amplifiers.

Model 947 offers 8 separate isolated modulator drive outputs for applications where complete input-to-input isolation as well as input-to-output isolation is required. For example, a single model 947 could be combined with four model 288J/K to configure a 4-channel 3-port isolated system (see page 55S).

Model 948 affords the same 850V dc input-to-output isolation for 1 to 8 model 288J/K isolation amplifiers with a common ground input reference as illustrated in Figure 1.

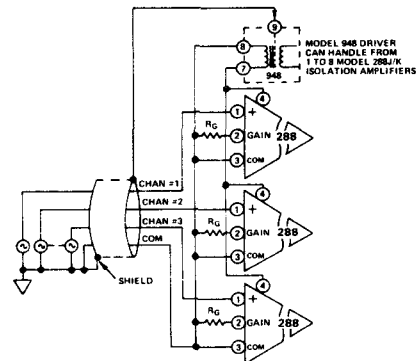


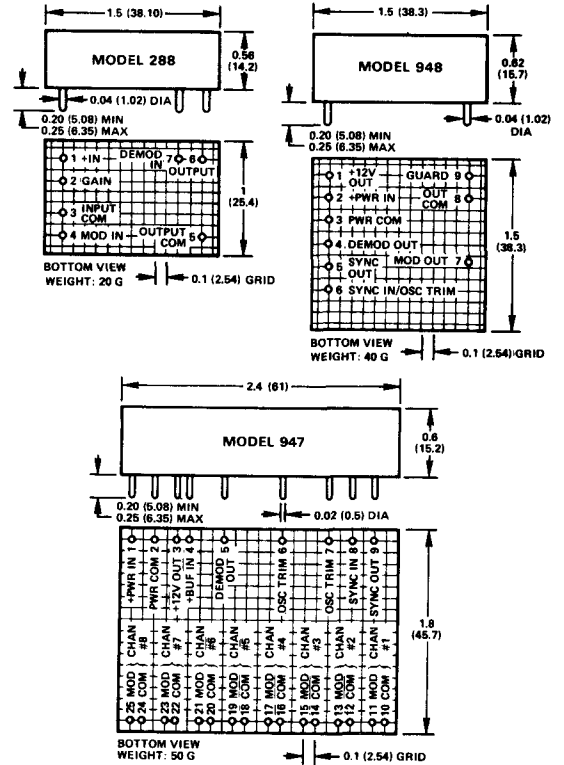
Figure 1. Application of Models 288/948 in Multichannel Data Isolation – (Note Common Signal Data Reference at Input)

# SPECIFICATIONS (typical @ +25°C over full range of power supply input unless otherwise noted, see note 1)

| Model  | 288J                                 | 288K                           |
|--|--------------------------------------|--------------------------------|
| <b>GAIN (NON-INVERTING)</b>                              |                                      |                                |
| Range (50kΩ Load)  | 1 to 1000V/V                         |                                |
| Gain Formula   | Gain = 1 + 100kΩ/R <sub>i</sub> (kΩ) |                                |
| Deviation from Formula                                   | ±4%                                  |                                |
| vs. Temperature (0 to +70°C) <sup>2</sup>                | ±0.01%/°C typ, ±0.03%/°C max         | ±0.0035%/°C typ, ±0.01%/°C max |
| vs. Time   | ±0.001%/1000 hours                   |                                |
| Nonlinearity, <sup>3</sup> ±5V Output (G = 1 to 1000V/V) | ±0.05% typ, ±0.1% max                | ±0.01% typ, ±0.05% max         |
| <b>INPUT VOLTAGE RATINGS</b>                             |                                      |                                |
| Linear Differential Range, G = 1V/V                      | ±5V min                              |                                |
| Safe Differential Input Voltage                          |                                      |                                |
| Continuous   | 240V rms max                         |                                |
| Pulse, 10ms Duration, 1 Pulse/sec                        | ±400V pk max                         |                                |
| CMV, Inputs to Outputs                                   |                                      |                                |
| ac, 60Hz, One Minute Duration                            | 750V rms                             |                                |
| Continuous, ac or dc                                     | ±850V pk max                         |                                |
| CMR, Inputs to Outputs, 60Hz, R <sub>S</sub> ≤ 1k        |                                      |                                |
| Balanced Source Impedance                                | 100dB                                |                                |
| 1kΩ Source Impedance Imbalance                           | 92dB min                             |                                |
| Leakage Current, Inputs to Outputs @ 115V ac, 60Hz       | 5.0μA rms max                        |                                |
| <b>OFFSET VOLTAGE, REFERRED TO INPUT</b>                 |                                      |                                |
| Initial, @ +25°C (Adjustable to zero)                    |                                      |                                |
| Gain = 500V/V  | ±0.5mV typ, ±1mV max                 | ±0.1mV typ, ±0.5mV max         |
| Gain = 1 to 1000V/V                                      | ±(1.0 + 50/G)mV max                  | ±(0.5 + 30/G)mV max            |
| vs. Temperature (0 to +70°C)                             |                                      |                                |
| Gain = 500V/V  | ±5μV/°C typ, ±10μV/°C max            | ±2μV/°C typ, ±5μV/°C max       |
| Gain = 1V/V  | ±250μV/°C typ, ±500μV/°C max         | ±100μV/°C typ, ±300μV/°C max   |
| Gain = 1 to 1000V/V                                      | ±(10 + 500/G)μV/°C max               | ±(5 + 300/G)μV/°C max          |
| vs. Supply Voltage                                       | ±(20 + 500/G)μV/V                    |                                |
| <b>INPUT BIAS CURRENT</b>                                |                                      |                                |
| Initial, @ +25°C   | ±25nA max                            |                                |
| vs. Temperature (0 to +70°C)                             | ±0.1nA/°C                            |                                |
| <b>INPUT IMPEDANCE</b>                                   |                                      |                                |
| Differential   | 10 <sup>8</sup> Ω    70pF            |                                |
| Overload   | 200kΩ                                |                                |
| Common Mode  | 10 <sup>8</sup> Ω    30pF            |                                |
| <b>INPUT NOISE</b>                                       |                                      |                                |
| Voltage, Gain = 500V/V                                   |                                      |                                |
| 0.01Hz to 10Hz   | 1.5μV p-p                            |                                |
| 10Hz to 1kHz   | 0.8μV rms                            |                                |
| Current  |                                      |                                |
| 0.01Hz to 10Hz   | 5pA pk-pk                            |                                |
| <b>FREQUENCY RESPONSE</b>                                |                                      |                                |
| Small Signal Bandwidth, -3dB                             |                                      |                                |
| Gain = 500V/V  | 400Hz                                |                                |
| Gain = 1V/V  | 3.5kHz                               |                                |
| Full Power Response, 10V pk-pk Output                    |                                      |                                |
| Gain = 500V/V  | 400Hz                                |                                |
| Gain = 1V/V  | 2.0kHz                               |                                |
| <b>RATED OUTPUT</b>                                      |                                      |                                |
| Voltage, 50kΩ Load                                       | ±5V min                              |                                |
| Output Impedance   | 1kΩ                                  |                                |
| Output Ripple, 1MHz Bandwidth                            | 2mV pk-pk                            |                                |
| <b>POWER SUPPLY<sup>4</sup></b>                          |                                      |                                |
| Voltage Range, Rated Performance                         | +13.5V dc to +26V dc                 |                                |
| Current, Quiescent, Model 947                            | +23mA @ V <sub>S</sub> = +15V dc     |                                |
| Current, Quiescent, Model 948                            | +15mA @ V <sub>S</sub> = +15V dc     |                                |
| <b>TEMPERATURE RANGE</b>                                 |                                      |                                |
| Rated Performance  | 0 to +70°C                           |                                |
| Operating  | -25°C to +85°C                       |                                |
| Storage  | -55°C to +85°C                       |                                |
| <b>PACKAGE SIZE</b>                                      |                                      |                                |
|  | 1.0" X 1.5" X 0.56"                  |                                |

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



## SPECIFICATIONS (typical @ +25°C over full range of power supply input unless otherwise stated)

| Model                        | 947(948)                                    |
|------------------------------|---|
| <b>OUTPUT</b>                |   |
| Frequency                    | 100kHz ±5%                                  |
| Waveform                     | Squarewave                                  |
| Voltage                      |   |
| Mod Drive                    | 22V p-p (18V p-p)                           |
| Demod Drive                  | 22V p-p (18V p-p)                           |
| Fan-Out <sup>1,2</sup>       | 8   |
| <b>POWER SUPPLY</b>          |   |
| Voltage, Rated Performance   | +13.5V dc to +26V dc                        |
| Current, Quiescent @ +15V dc |   |
| No Load                      | +23 (+15)mA                                 |
| Full Load <sup>3</sup>       | +40 (+32)mA                                 |
| <b>TEMPERATURE</b>           |   |
| Rated Performance            | 0 to +70°C                                  |
| Operating                    | -25°C to +85°C                              |
| Storage                      | -55°C to +85°C                              |
| <b>CASE SIZE</b>             |   |
|                              | 2.4" X 1.8" X 0.6"<br>(1.5" X 1.5" X 0.62") |

### NOTES:

- Specifications apply using either model 947 or model 948 mod/demod drive.
- Gain temperature drift is specified as a percentage of output signal level.
- Gain nonlinearity is specified as a percentage of output signal span.
- Power supply voltage ratings refer to models 947 or 948 mod/demod modules.

Specifications subject to change without notice.

### NOTES:

- Model 288J/K Mod Input and Demod Input represent unity load.
- For applications requiring more than eight 288's, additional 947's or 948's may be used in a master/slave mode. Refer to Figure 5.
- Full load consists of eight model 288's and a driver module (either 947 or 948).

Specifications subject to change without notice.

## ORDERING GUIDE

| Model | Type    | Socket  |
|-------|---------|---------|
| 288J  | Iso Amp | AC-1055 |
| 288K  | Iso Amp | AC-1055 |
| 947   | Driver  | AC-1056 |
| 948   | Driver  | AC-1057 |

# Applying the Multi-Channel Isolation Amplifier

## GUIDELINES ON INTERCONNECTION TECHNIQUES

To preserve the high CMR performance of model 288, care must be taken to keep the capacitance balanced about the input terminals. Best CMR performance will be achieved by using twisted shielded cable to reduce inductive and capacitive pickup. To reduce the effective cable capacitance, the cable shield should be connected to the common mode signal source by connecting the shield as close as possible to the signal low. To reduce capacitive coupling from input to output, dress all leads from the driver modules, models 947 or 948, short at the connection terminals and reduce the area formed by these leads. Input and output signal leads should be dressed away from the driver signals, demod and mod. Input leads should not be twisted together to reduce crosstalk noise.

## BASIC INTERCONNECTION – MODELS 288, 947 AND 948

### 4-CHANNEL 3-PORT ISOLATED SYSTEM

Figure 2 illustrates the basic interconnection between model 288J/K and 947 to provide a 4-channel system with 3-port

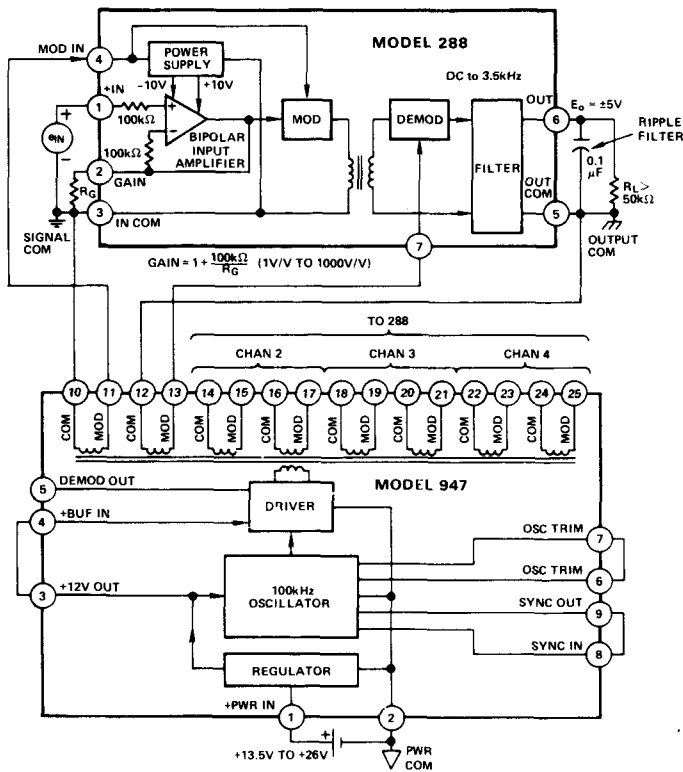
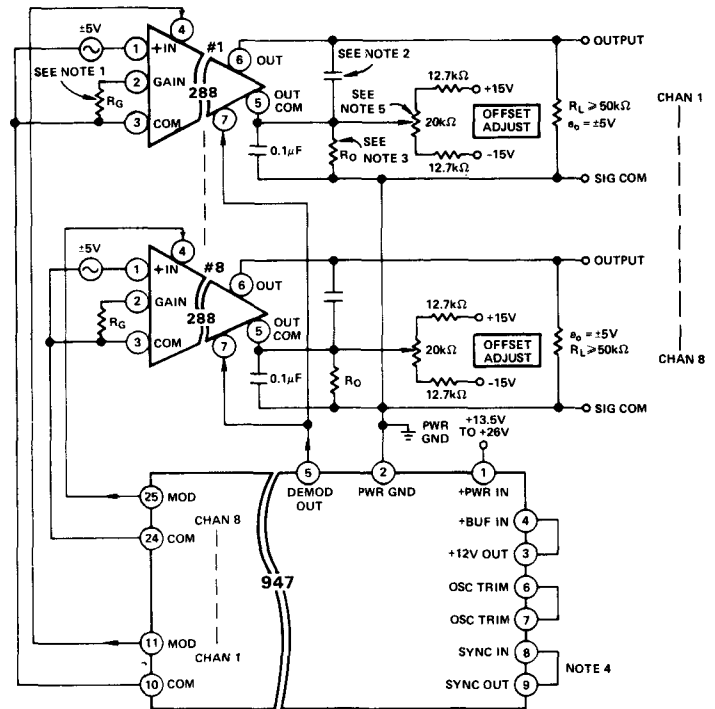


Figure 2. 4-Channel, 3-Port Isolated System

isolation. Total isolation exists between the input signal commons, the output signal commons and the power supply common. The model 947 provides two separate isolated drive signals for each 288 signal channel. Independent gain setting of each channel, from 1V/V to 1,000V/V, is available. To achieve the highest CMR performance, the input/output driver leads must be dressed to minimize capacitive cross-talk.

### 8-CHANNEL SYSTEM – MODELS 288 AND 947

Figure 3 illustrates the basic interconnection between a single model 947 and up to eight model 288 isolation amplifiers to provide complete input-to-output isolation as well as channel-to-channel isolation at the input. Each channel output is referenced to a common power supply ground. Offset voltage trimming is also provided for each channel. When offset voltage trimming is not required, the output common, pin 5, should be connected to the power common.



- NOTES:  
 1. GAIN FORMULA =  $1 + 100k\Omega/R_G (k\Omega)$ .  
 2. TO ROLL OFF NOISE AND OUTPUT RIPPLE, USE BANDWIDTH FORMULA  $(-3dB) = 1/2 \cdot C(1k\Omega)$ .  
 3. FOR GAINS = 1 TO 100V/V,  $R_0 = 200\Omega$ ; FOR GAINS = 100 TO 1000V/V,  $R_0 = 1k\Omega$ .  
 4. SEE DRIVER SYNCHRONIZATION, PAGE 4. FOR SYSTEMS WITH MORE THAN 8 CHANNELS.  
 5. OFFSET ADJUSTMENT POT SHOULD BE 10 OR 20 TURN CERMET TYPE.

Figure 3. 8-Channel System

## GAIN AND OFFSET TRIM PROCEDURE

In applying model 288, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak output error over the operating output voltage span. A calibration technique illustrating how to minimize the output error is shown below. In this example, model 288K is operating over an output span of +5V to -5V and a gain of 100V/V.

1. Apply  $E_{IN} = 0$  volts and adjust  $R_O$  for  $E_O = 0$  volts.
2. Apply  $E_{IN} = +0.05V$  dc and adjust  $R_f$  for  $E_O = +5.000V$  dc.
3. Apply  $E_{IN} = -0.05V$  dc and measure the output error (see curve a).
4. Adjust  $R_f$  until the output error is one half that measured in step 3 (see curve b).
5. Apply  $E_{IN} = +0.05V$  dc and adjust  $R_O$  until the output error is one half that measured in step 4 (see curve c).

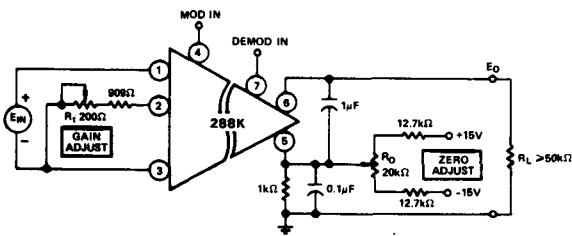
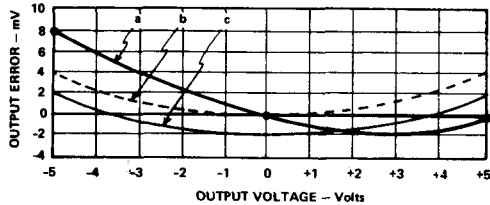


Figure 4. Gain and Offset Adjustment

## APPLICATION IN DATA ACQUISITION SYSTEMS HAVING MORE THAN 8 CHANNELS

**Driver Synchronization:** A single model 947 or model 948 driver can be applied in systems having from 1 to 8 data channels, as shown in Figures 3 and 10. Additional model 947's and 948's may be driven in a slave-mode, as shown in Figure 5, to expand the total system channels from 8 to virtually any number of channels.

**Optional Oscillator Adjustment:** Models 947 and 948 provide the user with a method to trim the internal 100kHz oscillator over a range of  $\pm 5\%$  (95kHz to 105kHz). This feature may be used when an external noise is "beating" with the 100kHz oscillator and a small trim adjustment of the oscillator frequency will eliminate the resulting noise frequency. As shown in Figure 5, a trim adjust,  $R_f$ , is installed between the OSC TRIM terminals. No specification changes occur when this trim adjustment is employed.

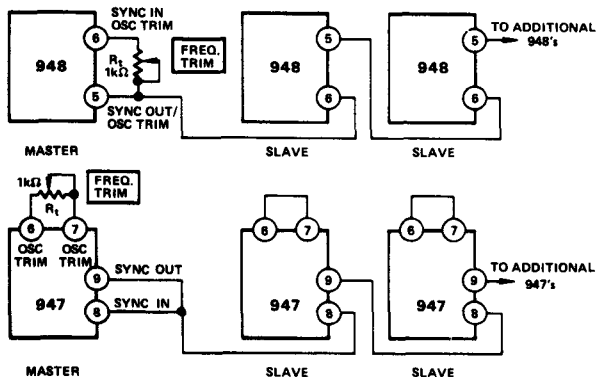


Figure 5. Model 948 and 947 Connections for Systems with Greater than 8 Channels

**Selecting Bandwidth:** In low frequency signal measurements, such as thermocouple temperature measurements, strain gage measurements and geophysical instrumentation, an external filter is used to select bandwidth and minimize output noise. As shown in Figure 6a, a capacitor connected between the OUT and OUT COM terminals will result in model 288's bandwidth set according to the following:  $f(-3dB) = \frac{1}{2\pi C(1k\Omega)}$ . For lowest noise performance, the filter capacitor should be located as close to the actual load as possible.

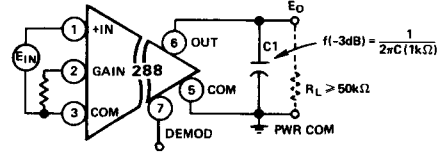


Figure 6a. Selecting Bandwidth with External Capacitor (C)

When used with a buffer amplifier as shown in Figure 6b below, a series resistor ( $R_S$ ) is used to lower the effective value of the filter capacitor required to achieve very low frequency (under 200Hz) noise filtering.

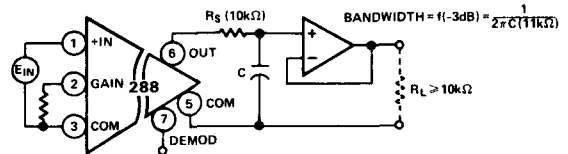


Figure 6b. Selecting Bandwidth with External Capacitor and Buffer

An active filter, as illustrated in Figure 6c will significantly improve 60Hz noise reduction at the output by providing a sharp rolloff characteristic. The 5Hz 3-pole active filter design illustrated in Figure 6c, will increase the 60Hz noise reduction by 50dB. Overall CMR performance of model 288 and the 5Hz active filter approaches 140dB @ 60Hz and 1kΩ imbalance.

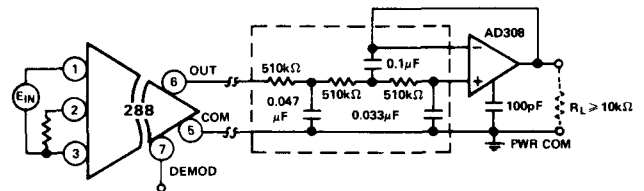


Figure 6c. Selecting Bandwidth with a 3-Pole 5Hz Active Filter

**Noise Reduction in Data Acquisition Systems:** In multichannel data acquisition systems using a multiplexer to select sequentially the channel for A/D conversion, a filter can be easily applied to reduce the input noise and select the channel bandwidth. As illustrated in Figure 7, a single 3-pole active filter is inserted at the mux output.

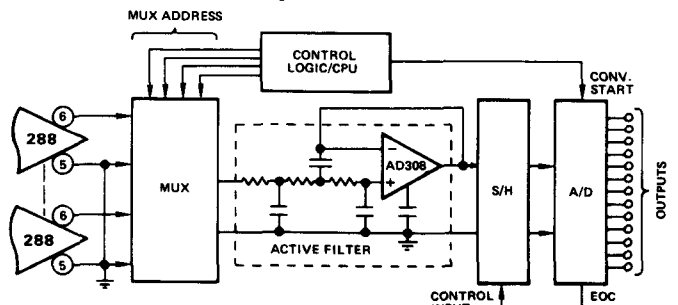


Figure 7. Applying Active Filter in Isolated Data Acquisition System to Select Bandwidth, Reduce Input Noise to A/D Converter and Increase CMR to 140dB @ 60Hz



## PERFORMANCE CHARACTERISTICS

**Gain Nonlinearity:** Linearity error is defined as the peak deviation of the output voltage from the best straight line and is specified as a % of the peak-to-peak output voltage span; e.g.,  $\pm 0.05\%$  @ 10V p-p output =  $\pm 5\text{mV}$  max RTO linearity error. Model 288 is available in two nonlinearity selections;  $\pm 0.05\%$  (288K) and  $\pm 0.1\%$  (288J)—max over the 10V p-p output span. The curves of Figure 12 illustrate typical linearity error over the 10V p-p ( $\pm 5\text{V}$ ) output span. At output levels less than 5V p-p ( $\pm 2.5\text{V}$ ), linearity error is typically less than  $\pm 0.025\%$  for both models 288J and 288K.

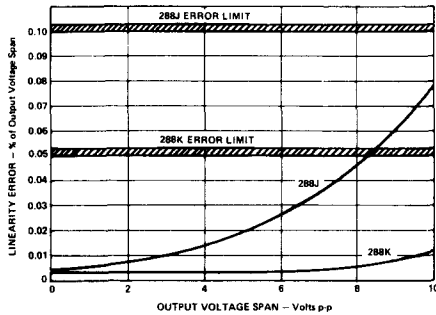


Figure 12. Gain Linearity Error vs. Output Voltage

**Common Mode Rejection:** Input-to-Output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and  $1\text{k}\Omega$  imbalance at a gain of 1V/V. Figure 13 illustrates CMR performance as a function of signal frequency and gain. CMR approaches 130dB at dc with source imbalances as high as  $1\text{k}\Omega$  in the INPUT COMMON lead (worst case condition).

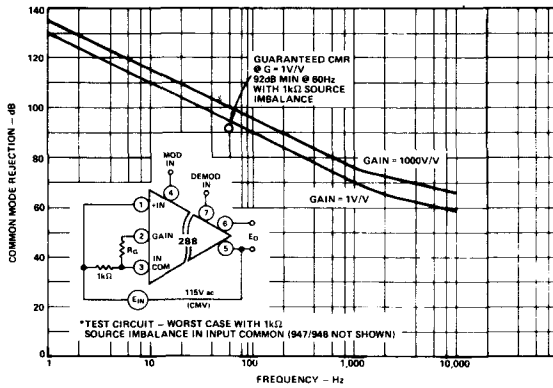


Figure 13. Common Mode Rejection vs. Frequency

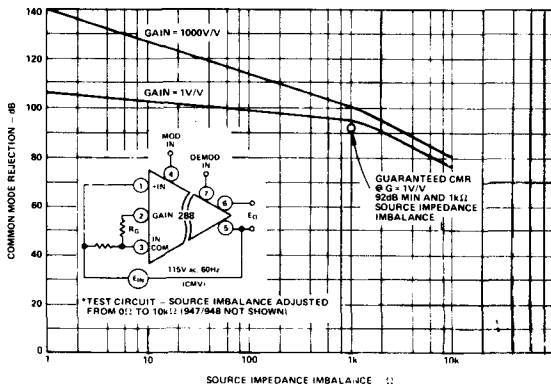


Figure 14. CMR vs. Source Impedance Imbalance

Figure 14 illustrates the effect of source imbalance on CMR performance at 60Hz and gains of 1V/V and 1,000V/V. CMR is typically 140dB at 60Hz, gain of 1,000V/V and a balanced source. CMR is maintained greater than 70dB for source imbalances up to 10k ohms.

**Input Offset Voltage Drift:** Model 288 is available in two drift selections:  $5\mu\text{V}/^\circ\text{C}$  (288K) and  $10\mu\text{V}/^\circ\text{C}$  (288J)—max, RTI,  $G = 500\text{V}/\text{V}$ . Total input voltage drift is composed of two sources (input and output stage drifts) and is gain dependent. The curves of Figure 15 illustrate the worst case total input drift (RTI) over the gain range of 1 to 1,000V/V.

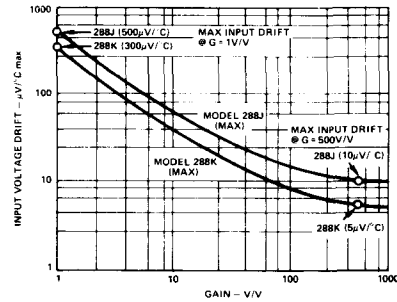


Figure 15. Max Input Offset Voltage Drift vs. Gain

**Input Voltage Noise:** Voltage noise, referred to input (RTI), is dependent on gain and bandwidth as illustrated in Figure 16. Rms voltage noise is shown in a bandwidth from 0.01Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.01Hz to 10Hz is  $1.5\mu\text{V}$  p-p at a gain of 500V/V. This value is derived by multiplying the rms value at  $f = 10\text{Hz}$  shown in Figure 16 ( $0.22\mu\text{V}$  rms) by 6.6.

For lowest noise performance, a low pass filter at the output should be used to selectively roll-off noise and undesired signal frequencies beyond the bandwidth of interest (see Figure 6).

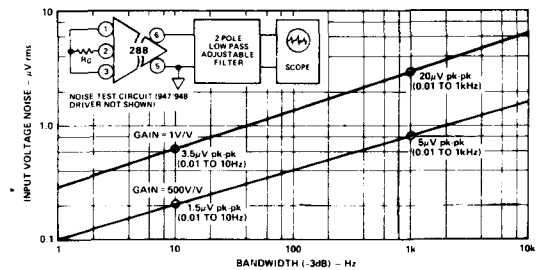


Figure 16. Input Voltage Noise vs. Bandwidth

**Frequency Response:** Small signal bandwidth and full power bandwidth versus gain are shown in Figure 17. For gains greater than 100V/V, both bandwidths are identical and approach 200Hz at  $G = 1000\text{V}/\text{V}$ . Full power response is measured with the output set at 10V p-p; small signal bandwidth ( $-3\text{dB}$ ) is measured with the output set at 100mV p-p.

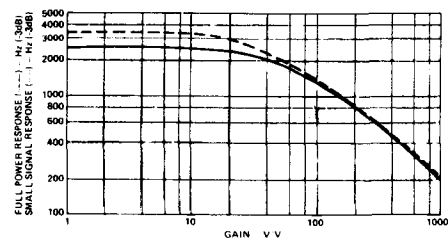


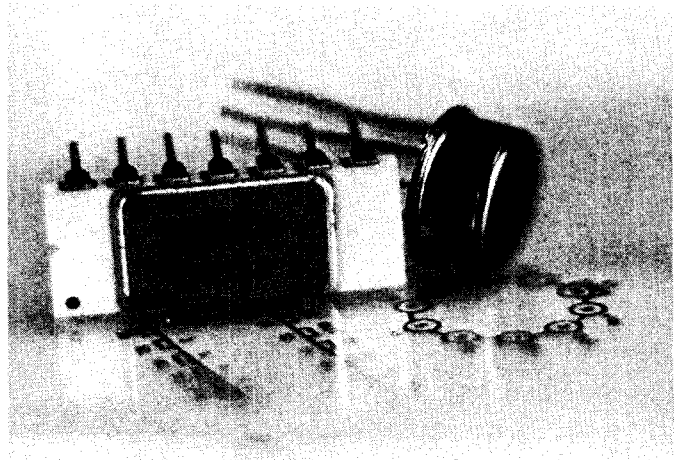
Figure 17. Full Power and Small Signal Bandwidth vs. Gain

**FEATURES**

- Pretrimmed to  $\pm 0.5\%$  max Error, 10:1 Denominator Range (AD535K)
- $\pm 2.0\%$  max Error, 50:1 Denominator Range (AD535J)
- All Inputs (X, Y and Z) Differential
- Low Cost, Monolithic Construction

**APPLICATIONS**

- General Analog Signal Processing
- Differential Ratio and Percentage Computations
- Precision AGC Loops
- Square-Rooting

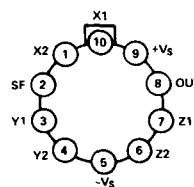

**PRODUCT DESCRIPTION**

The AD535 is a monolithic laser trimmed two-quadrant divider having performance specifications previously found only in expensive hybrid or modular products. A maximum divider error of  $\pm 0.5\%$  is guaranteed for the AD535K without any external trimming over a denominator range of 10:1;  $\pm 2.0\%$  max error over a range of 50:1. A maximum error of  $\pm 1\%$  over the 50:1 denominator range is guaranteed with the addition of two external trims. The AD535 is the first divider to offer fully differential, high impedance operation on all inputs, including the z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00; by means of an external resistor, this can be reduced by any amount down to 3.

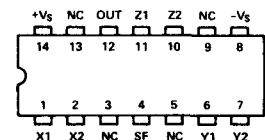
The extraordinary versatility and performance of the AD535 recommend it as the first choice in many divider and computational applications. Typical uses include square-rooting, ratio computation "pin-cushion" correction and AGC loops as illustrated in the applications section of the data sheet. The device is packaged in a hermetically sealed, 10-pin TO-100 can or 14-pin TO-116 DIP and made available in a  $\pm 1\%$  max error version (J) and a  $\pm 0.5\%$  max error version (K). Both versions are specified for operation over the 0 to  $+70^\circ\text{C}$  temperature range.

**PRODUCT HIGHLIGHTS**

1. Laser trimming at the wafer stage enables the AD535 to provide high accuracies without the addition of external trims ( $\pm 0.5\%$  max error over a 10:1 denominator range for the AD535K).
2. Improved accuracies over a wider denominator range are possible with only two external trims ( $\pm 0.5\%$  max error over a 20:1 denominator range for the AD535J).
3. Differential inputs on the X, Y and Z input terminals enhance the AD535's versatility as a generalized analog computational circuit.
4. Monolithic construction permits low cost and, at the same time, increased reliability.



**TO-100  
(TOP VIEW)**



**TO-116  
(TOP VIEW)**



# SPECIFICATIONS ( $V_S = \pm 15V$ , $R_L \geq 2k\Omega$ , $T_A = +25^\circ C$ unless otherwise stated)

| PARAMETER   | CONDITIONS                            | AD535J                                     | AD535K                       |   |
|---|---------------------------------------|--|------------------------------|---|
| TRANSFER FUNCTION                                       | Figure 2                              | $10 \frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$ | *                            |   |
| TOTAL ERROR <sup>1</sup>                                | No External Trims, Figure 2           |  |                              |   |
|   | $1V \leq X \leq 10V$ , $Z \leq  X $   | 1.0% max                                   | 0.5% max                     |   |
|   | $0.2V \leq X \leq 10V$ , $Z \leq  X $ | 5.0% max                                   | 2.0% max                     |   |
|   | With External Trims, Figure 5         |  |                              |   |
|   | $0.5V \leq X \leq 10V$ , $Z \leq  X $ | 1.0% max                                   | 0.5% max                     |   |
|   | $0.2V \leq X \leq 10V$ , $Z \leq  X $ | 2.0% max                                   | 1.0% max                     |   |
| TEMPERATURE COEFFICIENT                                 | $1V \leq X \leq 10V$ , $Z \leq  X $   | 0.01%/°C typ                               | *                            |   |
|   | $0.5V \leq X \leq 10V$ , $Z \leq  X $ | 0.02%/°C typ                               | *                            |   |
|   | $0.2V \leq X \leq 10V$ , $Z \leq  X $ | 0.05%/°C typ                               | *                            |   |
| SUPPLY RELATED<br>Error<br>$V_S = \pm 14V$ to $\pm 16V$ | $1V \leq X \leq 10V$                  | 0.1%/V typ                                 | *                            |   |
|   | $0.5V \leq X \leq 10V$                | 0.2%/V typ                                 | *                            |   |
|   | $0.2V \leq X \leq 10V$                | 0.5%/V typ                                 | *                            |   |
| SQUARE ROOTER<br>TOTAL ERROR <sup>1</sup>               | No External Trims, Figure 11          |  |                              |   |
|   | $1V \leq Z \leq 10V$                  | 0.4% typ                                   | *                            |   |
|   | $0.2V \leq Z \leq 10V$                | 0.7% typ                                   | *                            |   |
| NOISE <sup>2</sup>                                      | $X = 0.2V$ , $f = 10Hz$ to $10kHz$    | 4.5mV rms typ                              | *                            |   |
| BANDWIDTH   | $X = 0.2V$                            | 20kHz typ                                  | *                            |   |
| INPUT AMPLIFIERS <sup>3</sup>                           |                                       |  |                              |   |
|   | CMRR                                  | $f = 50Hz$ , 20V p-p                       | 60dB min                     | * |
|   | Bias Current                          |  | 2.0μA max                    | * |
|   | Offset Current                        |  | 0.1μA typ                    | * |
| Differential Resistance                                 |                                       | 10MΩ typ                                   | *                            |   |
| OUTPUT AMPLIFIER <sup>3</sup>                           |                                       |  |                              |   |
|   | Open-Loop Gain                        | $f = 50Hz$                                 | 70dB typ                     | * |
|   | Small Signal Gain-Bandwidth           | $V_{OUT} = 0.1V$ rms                       | 1MHz typ                     | * |
|   | 1% Amplitude Error                    | $C_{LOAD} = 1000pF$                        | 50kHz typ                    | * |
|   | Output Voltage Swing                  | $T_{min}$ to $T_{max}$                     | ±11V min                     | * |
|   | Slew Rate                             | $V_{OUT} = 20V$ p-p                        | 20V/μs typ                   | * |
|   | Settling Time                         | $V_{OUT} = 20V \pm 1\%$                    | 2μs typ                      | * |
|   | Output Impedance                      | Unity Gain, $f \leq 1kHz$                  | 0.1Ω typ                     | * |
| Wide-band Noise   | $f = 10Hz$ to $5MHz$                  | 1mV rms typ                                | *                            |   |
|   | $f = 10Hz$ to $10kHz$                 | 90μV rms typ                               | *                            |   |
| OUTPUT CURRENT  | $T_{min}$ to $T_{max}$ , $R_L = 0$    | 30mA max                                   | *                            |   |
| POWER SUPPLIES  |                                       |  |                              |   |
|   | Rated Performance                     |  | ±15V                         | * |
|   | Operating<br>Supply Current           | Quiescent                                  | ±8V min, ±18V max<br>6mA max | * |

## NOTES:

\*Specifications same as AD535J.

<sup>1</sup> Figures are given as a percent of full scale (i.e. 1.0% = 100mV).

<sup>2</sup> Noise may be reduced as shown in Figure 14.

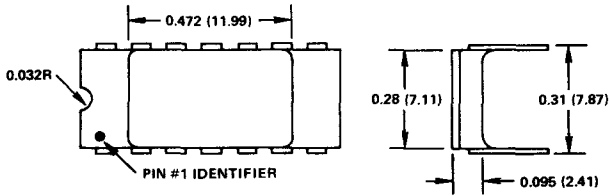
<sup>3</sup> See Figure 1 for definition of section.

Specifications subject to change without notice.

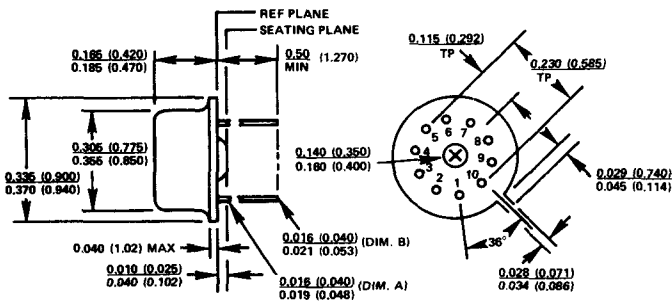
## PHYSICAL DIMENSIONS

Dimensions shown in inches and (mm).

### TO-116



### TO-100



## ABSOLUTE MAXIMUM RATINGS

|   |                 |
|---|-----------------|
| Supply Voltage  | ±18V            |
| Internal Power Dissipation  | 500mW           |
| Output Short-Circuit to Ground  | Indefinite      |
| Input Voltages, X <sub>1</sub> , X <sub>2</sub> , Y <sub>1</sub> , Y <sub>2</sub> , Z <sub>1</sub> , Z <sub>2</sub> | ±V <sub>S</sub> |
| Rated Operating Temp Range  | 0 to +70°C      |
| Storage Temp Range  | -65°C to +150°C |
| Lead Temp, 60s soldering  | +300°C          |

## FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the AD535. Inputs are converted to differential currents by three identical voltage to current converters, each trimmed for zero offset. The product of the X and Y currents is generated by a multiplier cell using Gilbert's translinear technique with an internal scaling voltage.

The difference between XY/SF and Z is applied to the high gain output amplifier. The transfer function can then be expressed...

$$V_{OUT} = A \left[ \frac{(X_1 - X_2)(Y_1 - V_{OUT})}{SF} - (Z_1 - Z_2) \right]$$

where A = open loop gain of output amplifier, typically 70dB at dc

X, Y, Z = input voltages

SF = scale factor, pretrimmed to 10.00V but adjustable by the user down to 3V.

In most cases the open loop gain can be regarded as infinite and SF will be 10V. Dividing both sides of the equation by A and solving the V<sub>OUT</sub>, we get...

$$V_{OUT} = 10V \frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$$

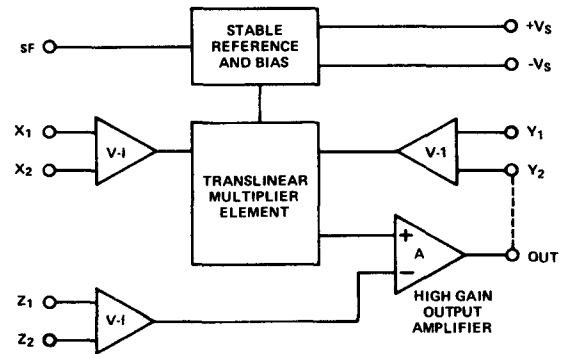


Figure 1. AD535 Functional Block Diagram

## SOURCES OF ERROR

Divider error is specified as a percent of full scale (i.e. 10.00V) and consists primarily of the effects of X, Y and Z offsets and scale factor (which are trimmable) as shown in the generalized equation....

$$V_{OUT} = (SF + \Delta SF) \left[ \frac{(Z_2 - Z_1) + Z_{OS}}{(X_1 - X_2) + X_{OS}} \right] + Y_1 + Y_{OS}$$

Note especially that divider error is inversely proportional to X, that is, the error increases rapidly with decreasing denominator values. Hence, the AD535 divider error is specified over several denominator ranges on page 60S. (See also Figure 12, AD535 Total Error as a function of denominator values.)

Overall accuracy of the AD535 can be significantly improved by nulling out X and Z offset as described in the applications sections. Figure 13 illustrates a factor of 2 improvement in accuracy with the addition of these external trims. The remaining errors stem primarily from scale factor error and Y offsets which can be trimmed out as shown in Figure 6.

Figure 14 illustrates the bandwidth and noise relationships versus denominator voltage. Whereas noise increases with decreasing denominator, bandwidth decreases, the net result given by the expression...

$$E_{N_{OUT}} (\text{wideband}) = \frac{1.26}{\sqrt{\left(\frac{X}{10}\right)}} \text{ mV rms}$$

External filtering can be added to limit output voltage noise even further. In this case...

$$E_{NO_{OUT}} \text{ (B.W. externally limited)} = \frac{0.9 \sqrt{f}}{\left(\frac{X}{10}\right)} \text{ mV rms}$$

where  $f$  = bandwidth in MHz of an external filter whose bandwidth is less than the noise bandwidth of the AD535. Table 1 provides calculated values of the typical output voltage noise, both filtered and unfiltered for several denominator values.

| X    | Noise<br>10Hz to 5MHz | Noise Limited by<br>External Filtering<br>10Hz to 10kHz |
|------|-----------------------|---|
| 0.2V | 8.9mV rms             | 4.5mV rms   |
| 0.5V | 5.6mV rms             | 1.8mV rms   |
| 1V   | 4.0mV rms             | 0.9mV rms   |
| 10V  | 1.3mV rms             | 0.09mV rms  |

Table 1. AD535 Calculated Voltage Noise

### APPLICATIONS

Figure 2 shows the standard divider connection without external trims. The denominator  $X$ , is restricted to positive values in this configuration.  $X$ ,  $Y$  and  $Z$  inputs are differential with high (80dB typical) CMRR permitting the application of differential signals on  $X$  and  $Z$  (see Figure 3).

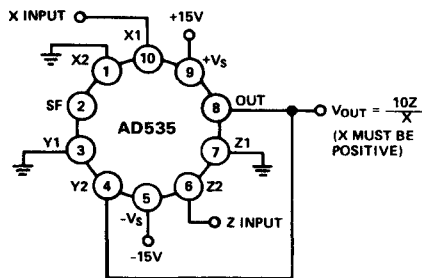


Figure 2. Divider Without External Trims

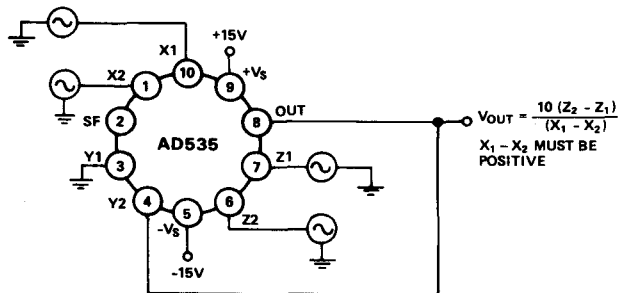


Figure 3. Differential Divider Connection

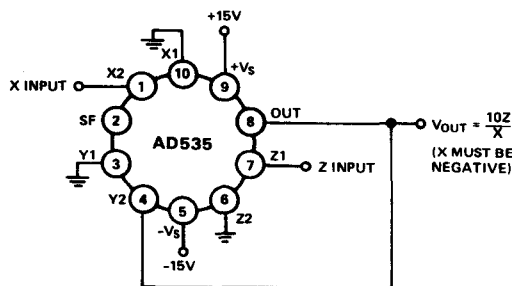


Figure 4. Divider Connection for Negative X Inputs

Negative denominator inputs are handled as shown in Figure 4. Note that in either configuration, operation is limited to two quadrants (i.e.  $Z$  is bipolar,  $X$  is unipolar).

A factor of two improvements in accuracy is possible by trimming the  $X$  and  $Z$  offsets as illustrated in Figure 5. To trim, set  $X$  to the smallest denominator value for which accurate computation is required (i.e.,  $X = 0.2V$ ). With  $Z = 0$ , adjust the  $Z_0$  trim for  $V_{OUT} = 0$ . Next, adjust the  $X_0$  trim for the best compromise when  $Z = +X$  ( $V_{OUT} = +10V$ ) and  $Z = -X$  ( $V_{OUT} = -10V$ ). Finally, readjust  $Z_0$  for the best compromise at  $Z = +X$ ,  $Z = -X$  and  $Z = 0$ . The remaining error (Figure 13) consists primarily of scale factor error, output offset and an irreducible nonlinearity component.

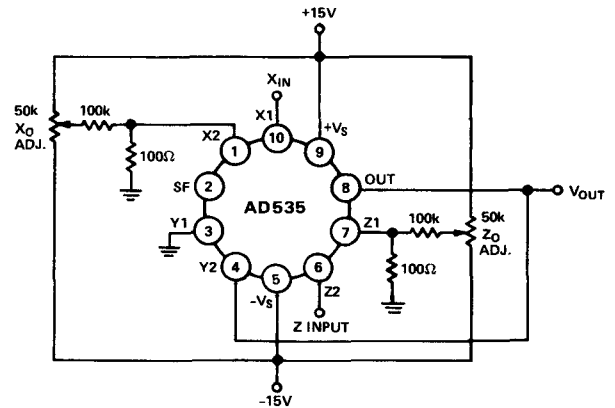


Figure 5. Precision Divider Using Two Trims

In certain applications, the user may elect to adjust  $SF$  for values between 10.00 and 3 by connecting an external resistor in series with a potentiometer between  $SF$  and  $-V_S$ . The approximate value of the total resistance for a given value of  $SF$  is given by the relationship:

$$R_{SF} = 5.4K \frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary  $R_{SF} \pm 25\%$  using the potentiometer. Note that the peak signal is always limited to  $1.25 SF$  (i.e.  $\pm 5V$  for  $SF = 4$ ).

The scale factor may also be adjusted using a feedback attenuator between  $V_{OUT}$  and  $Y_2$  as indicated in Figure 6. The input signal range is unaffected using this scheme.

Scale factor and output offset error can be minimized utilizing the four trim circuit of Figure 6. Adjustment is as follows:

1. Apply  $X = +0.2V$  (or the smallest required denominator value),  $Z = 0$  and adjust  $Z_0$  for  $V_{OUT} = 0$ .
2. Apply  $X = 0.2V$ . Then adjust the  $X_0$  trim for the best compromise when  $Z = +X$  ( $V_{OUT} = +10V$ ) and  $Z = -X$  ( $V_{OUT} = -10V$ ).
3. Apply  $X = +10V$ ,  $Z = 0$  and adjust  $Y_0$  for  $V_{OUT} = 0$ .
4. Apply  $X = +10V$ . Then adjust the scale factor ( $SF$ ) trim for the best compromise when  $Z = +X$  ( $V_{OUT} = +10V$ ) and  $Z = -X$  ( $V_{OUT} = -10V$ ).
5. Repeat steps 1 and 2.
6. Apply  $X = 0.2V$ . Then adjust the  $Z$  trim for the best compromise when  $Z = X$  ( $V_{OUT} = +10V$ ),  $Z = 0$  ( $V_{OUT} = 0$ ) and  $Z = -X$  ( $V_{OUT} = -10V$ ).

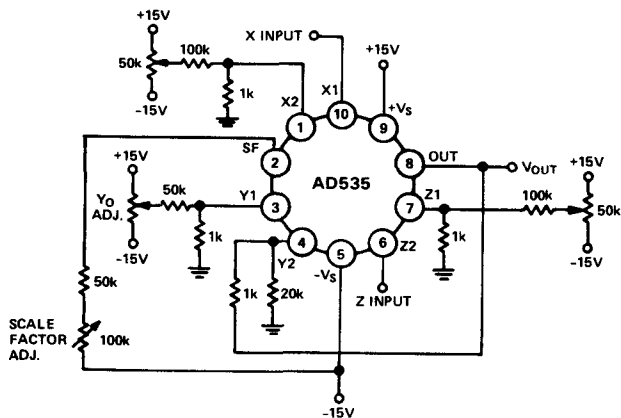


Figure 6. Precision Divider with Four External Adjustments

These trim adjustments can be made either by using two calibrated voltage sources and a DVM, or by using a differential scope, a low frequency generator, a voltage source and a precision attenuator. As shown in Figure 7, the differential scope subtracts the expected ideal output and thus displays only errors. Set the attenuation to  $\frac{X}{10}$ .

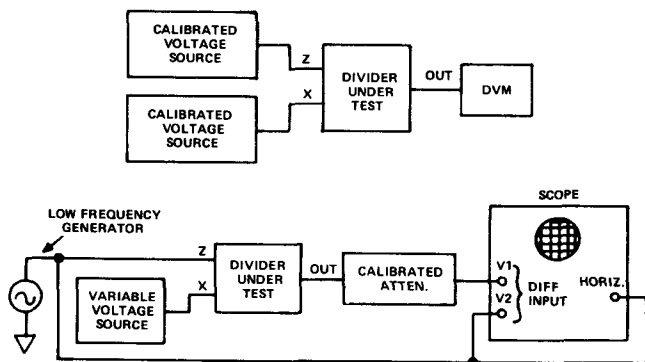


Figure 7. Alternate Trim Adjustment Set-Up

### PIN-CUSHION CORRECTION

A pin-cushion corrector eliminates the distortion caused by flat screen CRT tubes. The correction equations are:

$$V_{OH} = \frac{V_{IH}}{\sqrt{V_{IH}^2 + V_{IV}^2 + L^2}}$$

$$\text{and } V_{OV} = \frac{V_{IV}}{\sqrt{V_{IH}^2 + V_{IV}^2 + L^2}}$$

where:  $V_{OH}$  and  $V_{OV}$  are the horizontal and vertical output signals, respectively.

$V_{IH}$  and  $V_{IV}$  are the horizontal and vertical input signals, respectively.

$L$  is the length of the CRT tube.

In typical applications  $L$  (expressed in voltage) is roughly equal to full scale  $V_{IH}$  or  $V_{IV}$ . The result is that the expression,  $\sqrt{V_{IH}^2 + V_{IV}^2 + L^2}$ , varies less than 2:1 over the full range of values of  $V_{IH}$  and  $V_{IV}$ .

Major sources of divider error associated with small denominator values can thereby be minimized.

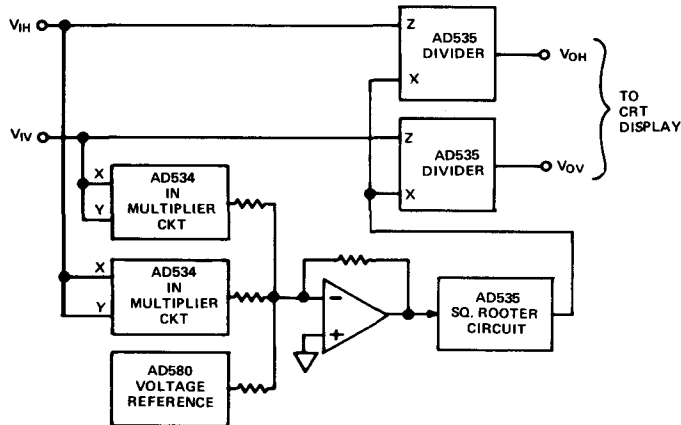


Figure 8. Pin-Cushion Corrector

Figure 9 shows an AGC loop using an AD535 divider. The AD535 lends itself naturally in this application since it is configured to provide gain rather than loss. Overall gain varies from 1 to  $\infty$  as the denominator is servoed to maintain  $V_{OUT}$  at a constant level.

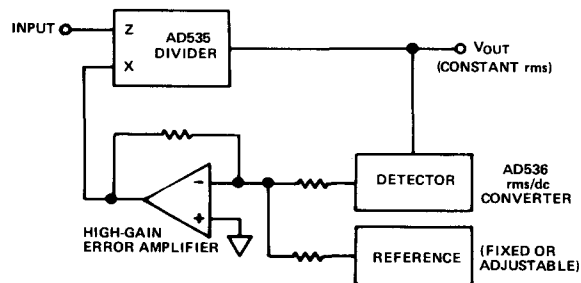


Figure 9. AGC Loop Using the AD536 rms/dc Converter as a Detector

Figure 10 shows a method for obtaining the time average as defined by:

$$\bar{X} = \frac{1}{T} \int_0^T X dt$$

where  $T$  is the time interval over which the average is to be taken. Conventional techniques typically provide only a crude approximation to the true time average, and furthermore, require a fixed time interval before the average can be taken. In Figure 10, the AD535 is used to divide the integrator output by the ramp generator output. Since the ramp is proportional to time, the integrator is divided by the time interval, thus allowing continuous, true time processing of signals over intervals varying by as much as 50:1.

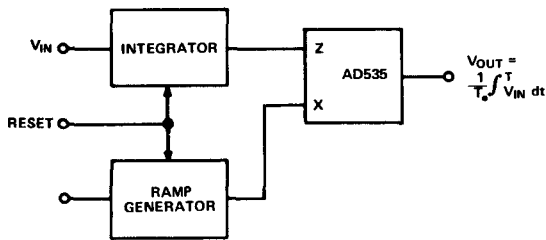


Figure 10. Time Average Computation Circuit

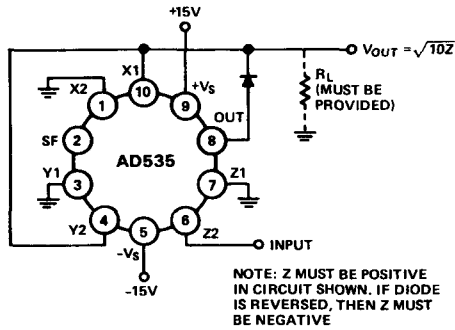


Figure 11. Square Rooter

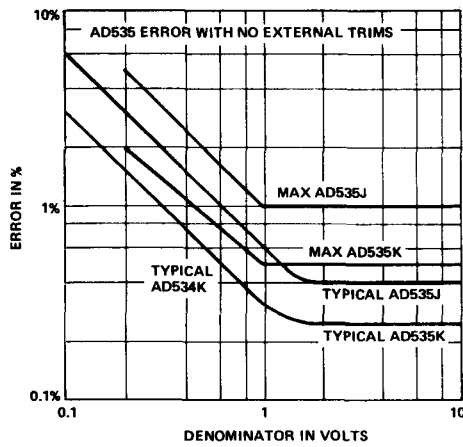


Figure 12. AD535 Error with No External Trims

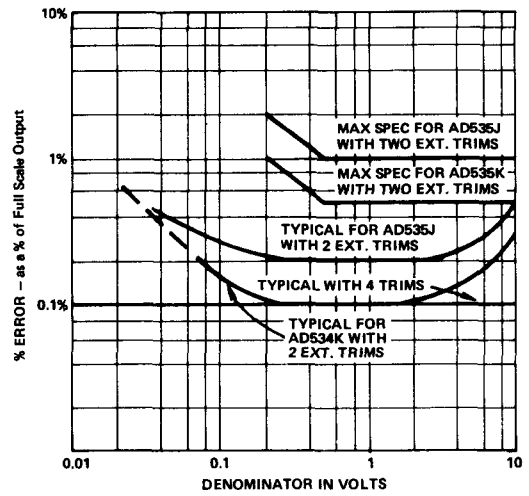


Figure 13. Errors with External Trims at 25°C

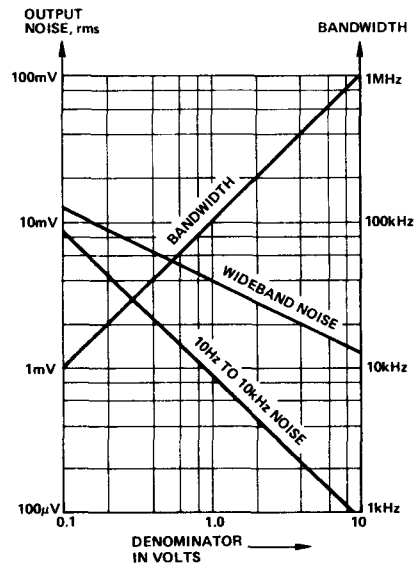


Figure 14. -3dB Bandwidth and Noise vs. Denominator

**FEATURES****True rms-to-dc Conversion****Laser-Trimmed to High Accuracy**

0.2% max Error (AD536AK)

0.5% max Error (AD536AJ)

**Wide Response Capability:**

Computes rms of ac and dc Signals

300kHz Bandwidth:  $V_{rms} > 100mV$ 2MHz Bandwidth:  $V_{rms} > 1V$ 

Signal Crest Factor of 7 for 1% Error

**dB Output with 60dB Range****Low Power: 1mA Quiescent Current****Single or Dual Supply Operation****Monolithic Integrated Circuit**

-55°C to +125°C Operation (AD536AS)

**Low Cost****PRODUCT DESCRIPTION**

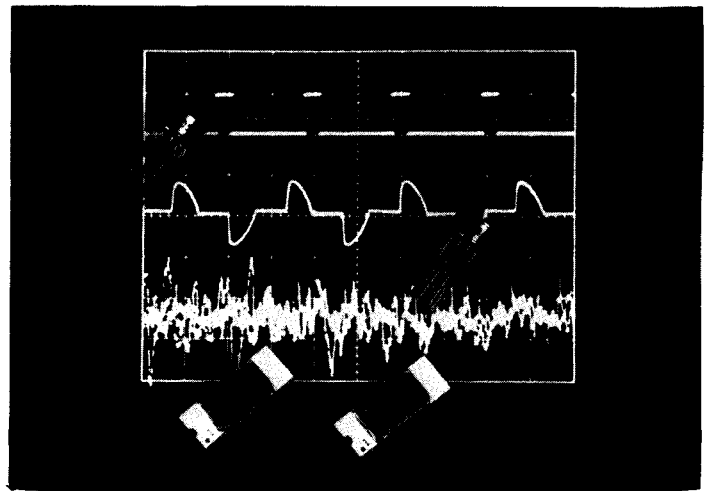
The AD536A is a complete monolithic integrated circuit which performs true rms-to-dc conversion. It offers performance which is comparable or superior to that of hybrid or modular units costing much more. The AD536A directly computes the true rms value of any complex input waveform containing ac and dc components. It has a crest factor compensation scheme which allows measurements with 1% error at crest factors up to 7. The wide bandwidth of the device extends the measurement capability to 300kHz with 3dB error for signal levels above 100mV.

An important feature of the AD536A not previously available in rms converters is an auxiliary dB output. The logarithm of the rms output signal is brought out to a separate pin to allow the dB conversion, with a useful dynamic range of 60dB. Using an externally supplied reference current, the 0dB level can be conveniently set by the user to correspond to any input level from 0.1 to 2 volts rms.

The AD536A is laser trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal), and full scale accuracy. As a result, no external trims are required to achieve the rated accuracy of the unit.

There is full protection for both inputs and outputs. The input circuitry can take overload voltages well beyond the supply levels. Loss of supply voltage with inputs connected will not cause unit failure. The output is short-circuit protected.

The AD536A is available in two accuracy grades (J, K) for commercial temperature range (0 to +70°C) applications, and one grade (S) rated for the full -55°C to +125°C military range. The AD536AK offers a maximum total error of  $\pm 2mV$



$\pm 0.2\%$  of reading and the AD536AJ and AD536AS have maximum errors of  $\pm 5mV \pm 0.5\%$  of reading. All three versions are available in either a hermetically sealed 14-pin DIP or a 10-pin TO-100 metal can.

**PRODUCT HIGHLIGHTS**

1. The AD536A computes the true root-mean-square level of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it relates directly to the power of the signal. The rms value of a statistical signal also relates to its standard deviation.
2. The crest factor of a waveform is the ratio of the peak signal swing to the rms value. The crest factor compensation scheme of the AD536A allows measurement of highly complex signals with wide dynamic range.
3. The only external component required to perform measurements to the fully specified accuracy is the capacitor which sets the averaging period. The value of this capacitor determines the low frequency ac accuracy, ripple level and settling time.
4. The AD536A will operate equally well from split supplies or a single supply with total supply levels from 5 to 36 volts. The one milliamper quiescent supply current makes the device well-suited for a wide variety of remote controllers and battery powered instruments.
5. The AD536A directly replaces the AD536, and provides improved bandwidth and temperature drift specifications.

# SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

| MODEL  | AD536AJ   | AD536AK  | AD536AS  |
|--|---|--|--|
| TRANSFER EQUATION  | $V_{OUT} = \sqrt{\text{avg. } (V_{IN})^2}$                        | *  | *  |
| <b>CONVERSION ACCURACY</b>   |   |  |  |
| Total Error, Internal Trim <sup>1</sup> (Fig. 1)<br>vs. Temperature, $T_{min}$ to +70°C<br>+70°C to +125°C | ±5mV ±0.5% of Reading, max<br>±(0.1mV ±0.01% Reading)/°C max<br>— | ±2mV ±0.2% of Reading, max<br>±(0.05mV ±0.005% of Reading)/°C max<br>— | ±(0.1mV ±0.005% of Reading)/°C max<br>±(0.3mV ±0.005% of Reading)/°C max |
| vs. Supply Voltage<br>dc Reversal Error  | ±(0.1mV ±0.01% Reading)/V<br>±0.05% of Reading                    | *  | *  |
| Total Error, External Trim <sup>1</sup> (Fig. 2)   | ±3mV ±0.3% of Reading   | ±2mV ±0.1% of Reading  | *  |
| <b>ERROR vs CREST FACTOR<sup>2</sup></b>   |   |  |  |
| Crest Factor 1 to 2  | Specified Accuracy  | *  | *  |
| Crest Factor = 3   | -0.1% of Reading  | *  | *  |
| Crest Factor = 7   | -1% of Reading  | *  | *  |
| <b>FREQUENCY RESPONSE<sup>3</sup></b>  |   |  |  |
| Bandwidth for 1% additional error (0.1dB)  |   |  |  |
| 10mV < $V_{IN}$ ≤ 100mV  | 6kHz  | *  | *  |
| 100mV < $V_{IN}$ ≤ 1V  | 40kHz   | *  | *  |
| 1V < $V_{IN}$ ≤ 7V   | 100kHz  | *  | *  |
| ±3dB Bandwidth   |   |  |  |
| 10mV < $V_{IN}$ ≤ 100mV  | 50kHz   | *  | *  |
| 100mV < $V_{IN}$ ≤ 1V  | 300kHz  | *  | *  |
| 1V < $V_{IN}$ ≤ 7V   | 2MHz  | *  | *  |
| AVERAGING TIME CONSTANT (Fig. 5)   | 25ms/μF $C_{AV}$  | *  | *  |
| <b>INPUT CHARACTERISTICS</b>   |   |  |  |
| Signal Range, ±15V Supply  | ±20V Peak   | *  | *  |
| Signal Range, +5V Supply   | ±5V Peak  | *  | *  |
| Safe Input, All Supply Voltages  | ±25V max  | *  | *  |
| Input Resistance   | 16.7kΩ ±25%   | *  | *  |
| Input Offset Voltage   | ±2mV max  | ±1mV max   | *  |
| <b>OUTPUT CHARACTERISTICS</b>  |   |  |  |
| Offset Voltage   | ±2mV max  | ±1mV max   | *  |
| vs. Temperature  | ±0.1mV/°C   | *  | ±0.2mV/°C max  |
| vs. Supply Voltage   | ±0.1mV/V  | *  | ±0.2mV/V max   |
| Voltage Swing, ±15V Supplies   | 0 to +10V min   | *  | *  |
| ±5V Supply   | 0 to +2V min  | *  | *  |
| Output Current   | (+5mA, -130μA) min  | *  | *  |
| Short Circuit Current  | +20mA   | *  | *  |
| Resistance   | 0.5Ω max  | *  | *  |
| <b>dB OUTPUT (Fig. 13)</b>   |   |  |  |
| Error, $V_{IN}$ 7mV to 7V rms, 0dB = 1V rms  | ±0.5dB  | ±0.2dB   | *  |
| Scale Factor   | -3mV/dB   | *  | *  |
| Scale Factor TC (Uncompensated, see Fig. 13<br>for Temperature Compensation)                               | -0.3% Reading/°C (-0.03dB/°C)                                     | *  | *  |
| $I_{REF}$ for 0dB = 1V rms   | 20μA (5μA min, 80μA max)  | *  | *  |
| $I_{REF}$ Range  | 1μA to 100μA  | *  | *  |
| <b>LOAD TERMINAL</b>   |   |  |  |
| $I_{OUT}$ Scale Factor   | 40μA/Volt rms   | *  | *  |
| $I_{OUT}$ Scale Factor Tolerance   | ±2.5%   | *  | *  |
| Output Resistance  | 10 <sup>8</sup> Ω   | *  | *  |
| Voltage Compliance   | - $V_S$ to (+ $V_S$ -2.5V)  | *  | *  |
| <b>BUFFER AMPLIFIER</b>  |   |  |  |
| Input and Output Voltage Range   | - $V_S$ to (+ $V_S$ -2.5V)min                                     | *  | *  |
| Input Offset Voltage, $R_S = 25k$  | ±4mV max  | *  | *  |
| Input Current  | 100nA typ, 300nA max  | *  | *  |
| Input Resistance   | 10 <sup>8</sup> Ω   | *  | *  |
| Output Current   | (5mA, -130μA) min   | *  | *  |
| Short Circuit Current  | +20mA   | *  | *  |
| Small Signal Bandwidth   | 1MHz  | *  | *  |
| Slew Rate <sup>4</sup>   | 5V/μs   | *  | *  |
| <b>POWER SUPPLY</b>  |   |  |  |
| Voltage, Rated Performance   |   |  |  |
| Dual Supply  | ±3.0V to ±18V   | *  | *  |
| Single Supply  | +5V to +36V   | *  | *  |
| Quiescent Current  |   |  |  |
| Total $V_S$ 5V to 36V, $T_{min}$ to $T_{max}$  | 2mA max (1mA typ)   | *  | *  |
| <b>TEMPERATURE RANGE</b>   |   |  |  |
| Rated Performance  | 0 to +70°C  | *  | -55°C to +125°C  |
| Storage  | -55°C to +150°C   | *  | *  |

<sup>1</sup> Accuracy is specified for 0 to 7V rms, dc or 1kHz sinewave input with the AD536A connected as in the figure referenced.

<sup>2</sup> Error vs crest factor is specified as an additional error for 1V rms rectangular pulse input, pulse width = 200μs.

<sup>3</sup> Input voltages are expressed in volts rms, and error is percent of reading.

<sup>4</sup> With 2k external pulldown resistor.

\*Specifications same as AD536AJ.

Specifications subject to change without notice.

## STANDARD CONNECTION

The AD536A is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD536A will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor,  $C_{AV}$ , as shown in Figure 5. Thus, if a  $4\mu\text{F}$  capacitor is used, the additional average error at 10Hz will be 0.1%, at 3Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with the input, as shown in Figure 3; the capacitor must be non-polar. If the AD536A is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with  $0.1\mu\text{F}$  ceramic discs as near the device as possible.

The input and output signal ranges are a function of the supply voltages; these ranges are shown in Figure 17. The AD536A can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the  $25\text{k}\Omega$  resistor. The buffer amplifier can then be used for other purposes. Further the AD536A can be used in a current output mode by disconnecting the  $25\text{k}\Omega$  resistor from ground. The output current is available at pin 8 (pin 10 on the "H" package) with a nominal scale of  $40\mu\text{A}$  per volt rms input, positive out.

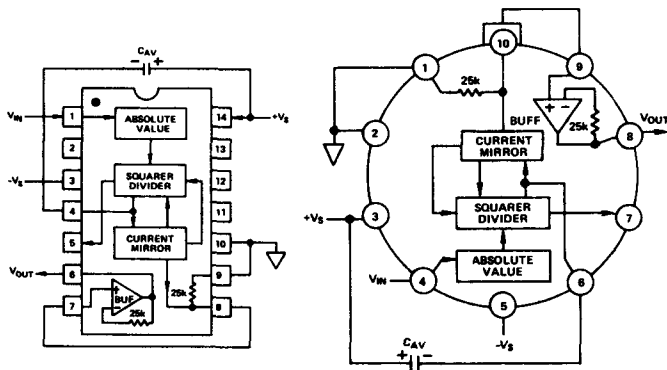


Figure 1. Standard rms Connection

## OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD536A, the external trims shown in Figure 2 can be added.  $R_4$  is used to trim the offset. Note that the offset trim circuit adds  $249\Omega$  in series with the internal  $25\text{k}\Omega$  resistor. This will cause a 1% increase in scale factor, which is trimmed out by using  $R_1$  as shown.

The trimming procedure is as follows:

1. Ground the input signal,  $V_{IN}$ , and adjust  $R_4$  to give zero volts output from pin 6. Alternatively,  $R_4$  can be adjusted to give the correct output with the lowest expected value of  $V_{IN}$ .
2. Connect the desired full scale input level to  $V_{IN}$ , either dc or a calibrated ac signal (1kHz is the optimum frequency); then trim  $R_1$  to give the correct output from pin 6, i.e., 1.000V dc input should give 1.000V dc output. Of course, a  $\pm 1.000$  peak-to-peak sinewave should give a 0.707V dc output. The remaining errors, as given in the specifications, are due to the nonlinearity.

The major advantage of external trimming is to optimize device performance for a reduced signal range; the AD536A is internally trimmed for a 7V rms full scale range.

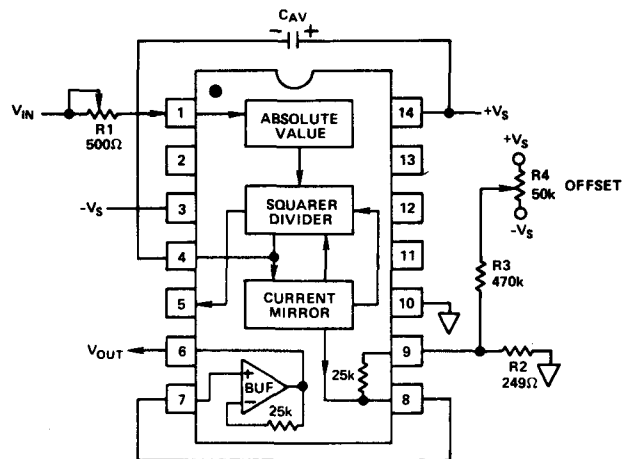


Figure 2. Optional External Gain and Output Offset Trims

## SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 require the use of approximately symmetrical dual supplies. The AD536A can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. The major limitation of this connection is that only ac signals can be measured since the differential input stage must be biased off ground for proper operation. This biasing is done at pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between  $+V_S$  and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 5 microamps of current flows into pin 10 (pin 2 on the "H" package). AC input coupling requires only capacitor  $C_2$  as shown; a dc return is not necessary as it is provided internally.  $C_2$  is selected for the proper low frequency break point with the input resistance of  $16.7\text{k}\Omega$ ; for a cut-off at 10Hz,  $C_2$  should be  $1\mu\text{F}$ . The signal ranges in this connection are slightly more restricted than in the dual supply connection. The input and output signal ranges are shown in Figure 17. The load resistor,  $R_L$ , is necessary to provide output sink current.

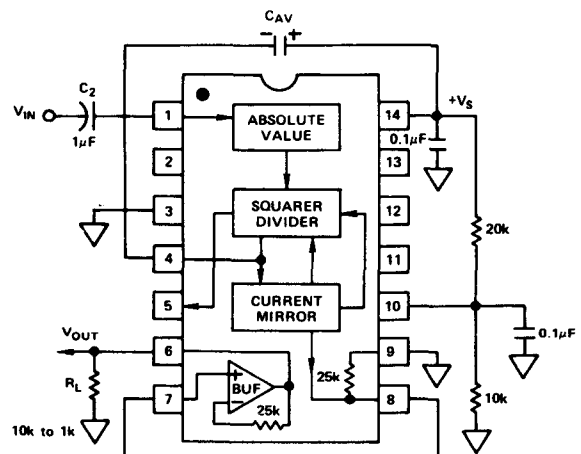


Figure 3. Single Supply Connection





**AD536A PRINCIPLE OF OPERATION**

The AD536A embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straight-forward computation of rms. The actual computation performed by the AD536A follows the equation:

$$V_{rms} = \text{Avg.} \left[ \frac{V_{IN}^2}{V_{rms}} \right]$$

Figure 9 is a simplified schematic of the AD536A; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage,  $V_{IN}$ , which can be ac or dc, is converted to a unipolar current  $I_1$ , by the active rectifier  $A_1, A_2$ .  $I_1$  drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2 / I_3$$

The output current,  $I_4$ , of the squarer/divider drives the current mirror through a low pass filter formed by  $R_1$  and the externally connected capacitor,  $C_{AV}$ . If the  $R_1, C_{AV}$  time constant is much greater than the longest period of the input signal, then  $I_4$  is effectively averaged. The current mirror returns a current  $I_3$ , which equals  $\text{Avg.} [I_4]$ , back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = \text{Avg.} [I_1^2 / I_4] = I_1 \text{ rms}$$

The current mirror also produces the output current,  $I_{OUT}$ , which equals  $2I_4$ .  $I_{OUT}$  can be used directly or converted to a voltage with  $R_2$  and buffered by  $A_4$  to provide a low impedance voltage output. The transfer function of the AD536A thus results:

$$V_{OUT} = 2R_2 I_{rms} = V_{IN \text{ rms}}$$

The dB output is derived from the emitter of  $Q_3$ , since the voltage at this point is proportional to  $-\log V_{IN}$ . Emitter follower,  $Q_5$ , buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current ( $I_{REF}$ ) to  $Q_5$  approximates  $I_3$ .

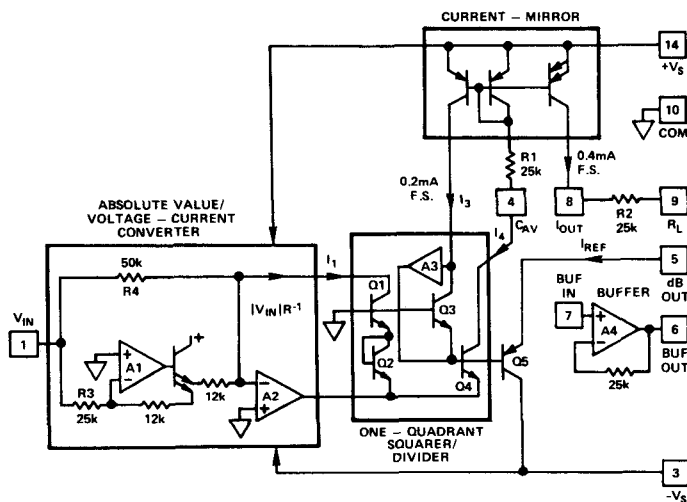
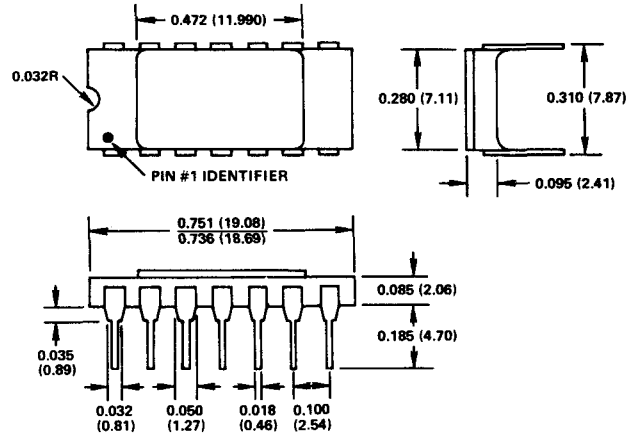


Figure 9. Simplified Schematic

**"D" PACKAGE (TO-116)**



**"H" PACKAGE (TO-100)**

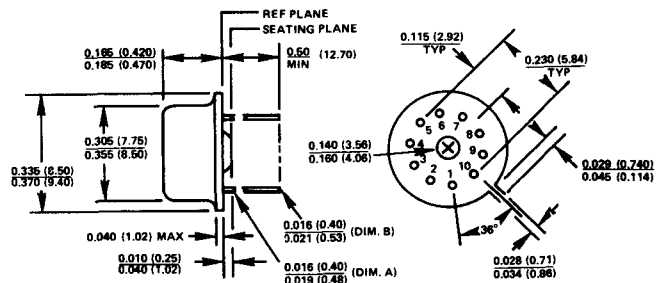
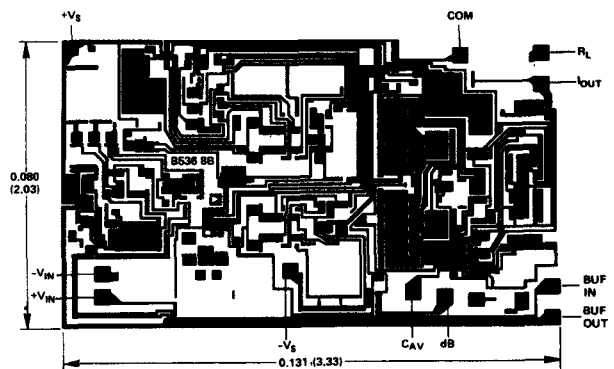


Figure 10. Physical Dimensions  
Dimensions shown in inches and (mm).



THE AD536A IS AVAILABLE IN LASER-TRIMMED CHIP FORM. CONSULT ANALOG DEVICES' CHIP CATALOG FOR SPECIFICATIONS AND APPLICATION DETAILS.

Figure 11. Chip Dimensions and Pad Layout.  
Dimensions shown in inches and (mm).

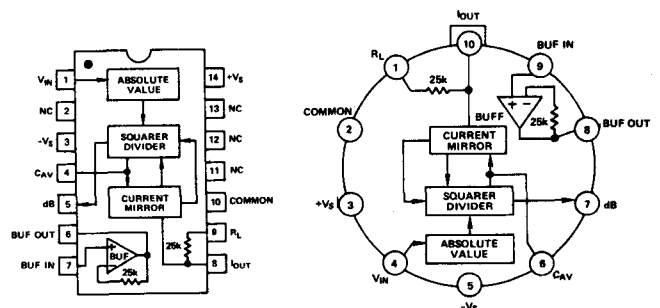


Figure 12. AD536A Pin Connections and Functional Diagram

### CONNECTIONS FOR dB OPERATION

A powerful feature added to the AD536A, which is not available in any other computing rms circuit, is the logarithmic or decibel output. The internal circuit which computes dB is very accurate and works well over a 60dB range. The connection for dB measurements is shown in Figure 13. The user selects the 0dB level by setting  $R_1$  for the proper 0dB reference current (which is set to exactly cancel the log output current from the squarer-divider at the desired 0dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the  $0.3\%/^{\circ}\text{C}$  temperature drift of the dB circuit. The special T.C. resistor,  $R_3$ , is available from Tel Labs, Londonderry, NH, type number Q-81. The linear rms output is available at pin 8 with an output impedance of  $25k\Omega$ ; thus some applications may require an additional buffer amplifier if this output is desired.

#### dB Calibration:

1. Set  $V_{IN} = 1.00\text{V dc}$
2. Adjust  $R_1$  for dB out = 0.00V
3. Set  $V_{IN} = +0.1\text{V dc}$
4. Adjust  $R_2$  for dB out = -2.00V

Any other desired 0dB reference level can be used by setting  $V_{IN}$  and adjusting  $R_1$  accordingly. Note that adjusting  $R_2$  for the proper gain automatically gives the correct temperature compensation.

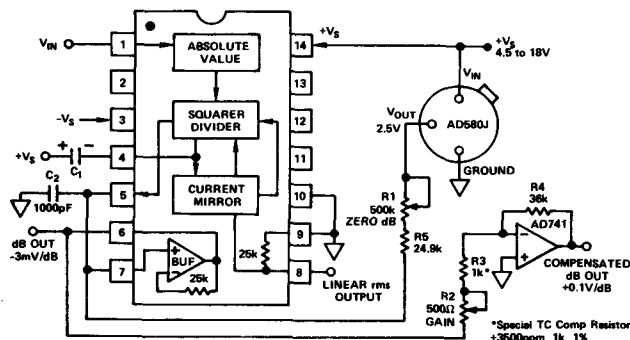


Figure 13. dB Connection

### FREQUENCY RESPONSE

The AD536A utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD536A at input levels from 10 millivolts to 1 volt rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and 3dB of reading additional error. For example, note that a 1 volt rms signal will produce less than 1% of reading additional error up to 100kHz. A 10 millivolt signal can be measured with 1% of reading additional error (100V) up to only 6kHz.

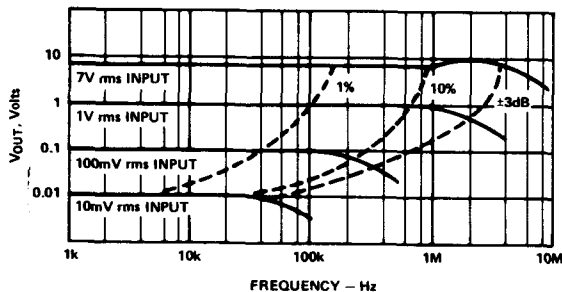


Figure 14. High Frequency Response

### AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms value of the signal ( $C.F. = V_p/V_{rms}$ ). Most common waveforms, such as sine and triangle waves, have relatively low crest factors ( $<2$ ). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 ( $C.F. = 1/\sqrt{\eta}$ ).

Figure 15 is a curve of reading error for the AD536A for a 1 volt rms input signal with crest factors from 1 to 10. A rectangular pulse train (pulse width  $100\mu\text{s}$ ) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 10 while maintaining a constant 1 volt rms input amplitude.

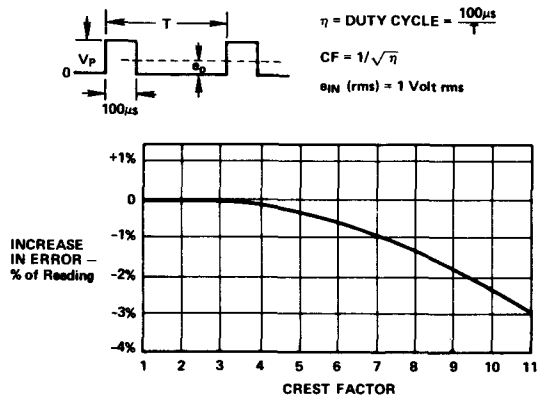


Figure 15. Error vs. Crest Factor

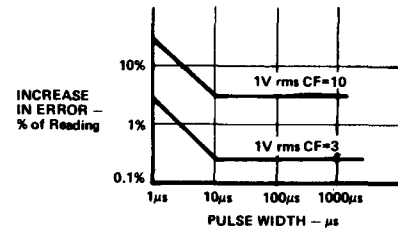


Figure 16. AD536A Error vs. Pulse Width Rectangular Pulse

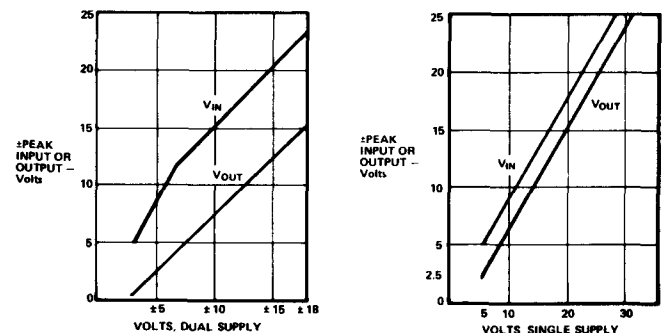


Figure 17. AD536A Input and Output Voltage Ranges vs. Supply

## FEATURES

- Laser-Trimmed to High Accuracy:**  
10.000 Volts  $\pm 5\text{mV}$  (L and U)
- Trimmed Temperature Coefficient:**  
5ppm/ $^{\circ}\text{C}$  max, 0 to  $+70^{\circ}\text{C}$  (L)  
10ppm/ $^{\circ}\text{C}$  max,  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  (U)
- Excellent Long-Term Stability:**  
25ppm/1000 hrs. (Non-Cumulative)
- Negative 10 Volt Reference Capability**
- Low Quiescent Current: 1.0mA max**
- 10mA Current Output Capability**
- 3-Terminal TO-5 Package**
- Low Cost**

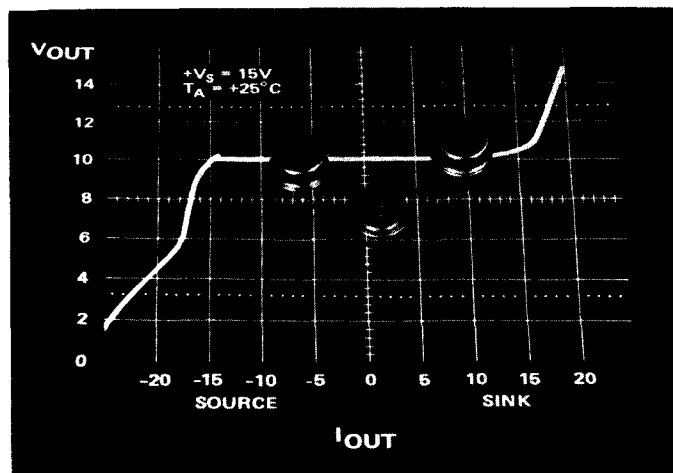
## PRODUCT DESCRIPTION

The AD581 is a three-terminal, temperature compensated, monolithic band-gap voltage reference which provides a precise 10.00 volt output from an unregulated input level from 12 to 40 volts. Laser Wafer Trimming (LWT) is used to trim both the initial error at  $+25^{\circ}\text{C}$  as well as the temperature coefficient, which results in high precision performance previously available only in expensive hybrids or oven-regulated modules. The 5mV initial error tolerance and 5ppm/ $^{\circ}\text{C}$  guaranteed temperature coefficient of the AD581L represent the best performance combination available in a monolithic voltage reference.

The band-gap circuit design used in the AD581 offers several advantages over classical zener breakdown diode techniques. Most important, no external components are required to achieve full accuracy and stability of significance to low power systems. In addition, total supply current to the device, including the output buffer amplifier (which can supply up to 10mA) is typically  $750\mu\text{A}$ . The long-term stability of the band-gap design is equivalent or superior to selected zener reference diodes.

The AD581 is recommended for use as a reference for 8, 10 or 12 bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD581J, K, and L are specified for operation from 0 to  $+70^{\circ}\text{C}$ ; the AD581S, T, and U are specified for the  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  range. The AD581S, T, and U grades are also available processed to MIL-STD-883A, Level B. All grades are packaged in a hermetically-sealed three-terminal TO-5 metal can.



## PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD581L has a maximum deviation from 10.000 volts of  $\pm 7.25\text{mV}$  from 0 to  $+70^{\circ}\text{C}$ , while the AD581U guarantees  $\pm 15\text{mV}$  maximum total error without external trims from  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .
2. Since the laser trimming is done on the wafer prior to separation into individual chips, the AD581 will be extremely valuable to hybrid designers for its ease of use, lack of required external trims, and inherent high performance.
3. The AD581 can also be operated in a two-terminal "Zener" mode to provide a precision negative 10 volt reference with just one external resistor to the unregulated supply. The performance in this mode is nearly equal to that of the standard three-terminal configuration.
4. Advanced circuit design using the band-gap concept allows the AD581 to give full performance with an unregulated input voltage down to 12 volts. With an external resistor, the device will operate with a supply as low as 11.4 volts.
5. Every AD581 is baked for 48 hours at  $+200^{\circ}\text{C}$ , temperature cycled 10 times from  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ , burned-in under power for 48 hours at  $+125^{\circ}\text{C}$ , and given a high G shock test prior to final test to ensure reliability and long-term stability.

# SPECIFICATIONS (typical @ $V_{IN} = +15V$ and $+25^{\circ}C$ unless otherwise noted)

| MODEL   | AD581J                                     | AD581K                                | AD581L                               | AD581S                               | AD581T                              | AD581U                              |
|---|--|---------------------------------------|--------------------------------------|--------------------------------------|-------------------------------------|-------------------------------------|
| <b>ABSOLUTE MAX RATINGS</b>                               |  |                                       |                                      |                                      |                                     |                                     |
| Input Voltage $V_{IN}$ to Ground                          | 40V  | *                                     | *                                    | *                                    | *                                   | *                                   |
| Power Dissipation @ $+25^{\circ}C$                        | 600mW                                      | *                                     | *                                    | *                                    | *                                   | *                                   |
| Operating Junction Temp. Range                            | $-55^{\circ}C$ to $+150^{\circ}C$          | *                                     | *                                    | *                                    | *                                   | *                                   |
| Storage Temperature Range                                 | $-65^{\circ}C$ to $+175^{\circ}C$          | *                                     | *                                    | *                                    | *                                   | *                                   |
| Lead Temperature<br>(Soldering, 10sec)                    | $+300^{\circ}C$                            | *                                     | *                                    | *                                    | *                                   | *                                   |
| Thermal Resistance<br>Junction-to-Ambient                 | $150^{\circ}C/Watt$                        | *                                     | *                                    | *                                    | *                                   | *                                   |
| Operating Temperature Range                               | 0 to $+70^{\circ}C$                        | *                                     | *                                    | $-55^{\circ}C$ to $+125^{\circ}C$ ** |                                     | **                                  |
| <b>OUTPUT VOLTAGE TOLERANCE</b>                           |  |                                       |                                      |                                      |                                     |                                     |
| (Error from nominal 10.000V output)                       | $\pm 30mV$ max                             | $\pm 10mV$ max                        | $\pm 5mV$ max                        | $\pm 30mV$ max                       | $\pm 10mV$ max                      | $\pm 5mV$ max                       |
| <b>OUTPUT VOLTAGE CHANGE</b>                              |  |                                       |                                      |                                      |                                     |                                     |
| Maximum Deviation from $+25^{\circ}C$                     |  |                                       |                                      |                                      |                                     |                                     |
| Value $T_{min}$ to $T_{max}$<br>(Temperature Coefficient) | $\pm 13.5mV$<br>(30ppm/ $^{\circ}C$ )      | $\pm 6.75mV$<br>(15ppm/ $^{\circ}C$ ) | $\pm 2.25mV$<br>(5ppm/ $^{\circ}C$ ) | $\pm 30mV$<br>(30ppm/ $^{\circ}C$ )  | $\pm 15mV$<br>(15ppm/ $^{\circ}C$ ) | $\pm 10mV$<br>(10ppm/ $^{\circ}C$ ) |
| <b>LINE REGULATION</b>                                    |  |                                       |                                      |                                      |                                     |                                     |
| $15V \leq V_{IN} \leq 30V$                                | 3mV max<br>(0.002%/V)                      | *                                     | *                                    | *                                    | *                                   | *                                   |
| $13V \leq V_{IN} \leq 15V$                                | 1mV max<br>(0.005%/V)                      | *                                     | *                                    | *                                    | *                                   | *                                   |
| <b>LOAD REGULATION</b>                                    |  |                                       |                                      |                                      |                                     |                                     |
| $0 \leq I_{OUT} \leq 5mA$                                 | 500 $\mu V$ /mA max<br>200 $\mu V$ /mA typ | *                                     | *                                    | *                                    | *                                   | *                                   |
| <b>QUIESCENT CURRENT</b>                                  |  |                                       |                                      |                                      |                                     |                                     |
|   | 1.0mA max<br>750 $\mu A$ typ               | *                                     | *                                    | *                                    | *                                   | *                                   |
| <b>TURN-ON SETTLING TIME TO 0.1%<sup>1</sup></b>          |  |                                       |                                      |                                      |                                     |                                     |
|   | 200 $\mu s$                                | *                                     | *                                    | *                                    | *                                   | *                                   |
| <b>NOISE</b>  |  |                                       |                                      |                                      |                                     |                                     |
| (0.1 to 10Hz)   | 50 $\mu V$ p-p                             | *                                     | *                                    | *                                    | *                                   | *                                   |
| <b>LONG-TERM STABILITY</b>                                |  |                                       |                                      |                                      |                                     |                                     |
|   | 25ppm/1000 Hrs.<br>(Non-Cumulative)        | *                                     | *                                    | *                                    | *                                   | *                                   |
| <b>SHORT CIRCUIT CURRENT</b>                              |  |                                       |                                      |                                      |                                     |                                     |
|   | 30mA                                       | *                                     | *                                    | *                                    | *                                   | *                                   |
| <b>OUTPUT CURRENT</b>                                     |  |                                       |                                      |                                      |                                     |                                     |
| Source @ $+25^{\circ}C$                                   | 10mA min                                   | *                                     | *                                    | *                                    | *                                   | *                                   |
| Source $T_{min}$ to $T_{max}$                             | 5mA min                                    | *                                     | *                                    | *                                    | *                                   | *                                   |
| Sink $T_{min}$ to $T_{max}$                               | 5mA min                                    | *                                     | *                                    | 200 $\mu A$ min                      | **                                  | **                                  |
| Sink $-55^{\circ}C$ to $+85^{\circ}C$                     | —  | —                                     | —                                    | 5mA min                              | **                                  | **                                  |

\*Specifications same as AD581J.

\*\*Specifications same as AD581S.

<sup>1</sup> See Figure 8.

Specifications and prices subject to change without notice.

## APPLYING THE AD581

The AD581 is easy to use in virtually all precision reference applications. The three terminals are simply primary supply, ground, and output, with the case grounded. No external components are required even for high precision applications; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The AD581 requires less than 1mA quiescent current from an operating supply range of 12 to 40 volts.

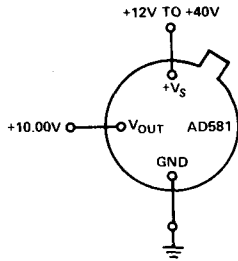


Figure 1. AD581 Pin Configuration (Top View)

An external fine trim may be desired to set the output level to exactly 10.000 volts within less than a millivolt (calibrated to a main system reference). System calibration may also require a reference slightly different from 10.00 volts. In either case, the optional trim circuit shown in Figure 2 can offset the output by up to  $\pm 30$  millivolts (with the  $22\Omega$  resistor), if needed, with minimal effect on other device characteristics.

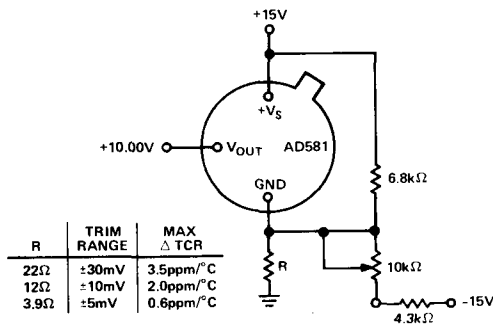
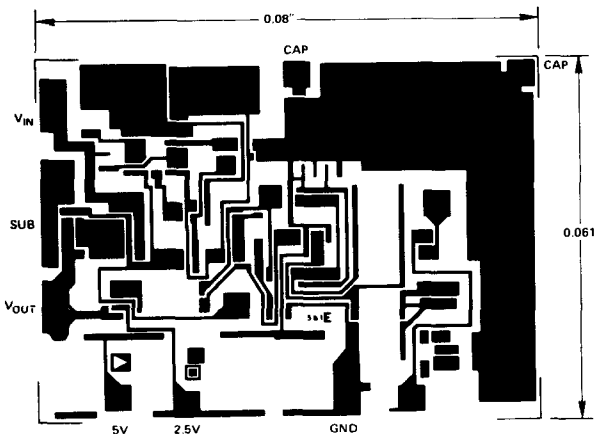


Figure 2. Optional Fine Trim Configuration



THE AD581 IS ALSO AVAILABLE IN LASER TRIMMED CHIP FORM WITH ALL SPECIFICATIONS GUARANTEED TO J-GRADE. THE CHIP HAS ADDITIONAL APPLICATION FLEXIBILITY NOT AVAILABLE IN THE THREE TERMINAL PACKAGED DEVICE. CONSULT FACTORY FOR FURTHER DETAILS.

Figure 3. AD581 Bonding Diagram

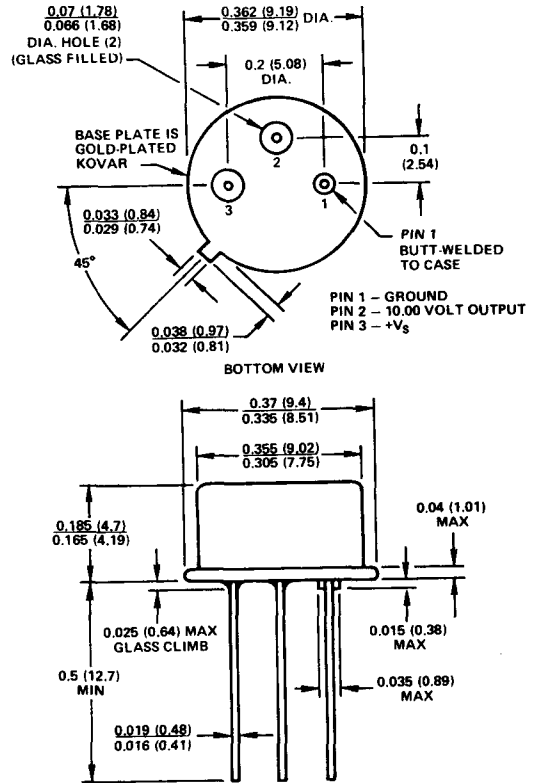


Figure 4. Outline Dimensions and Pin Designations. Dimensions shown in inches and (mm).

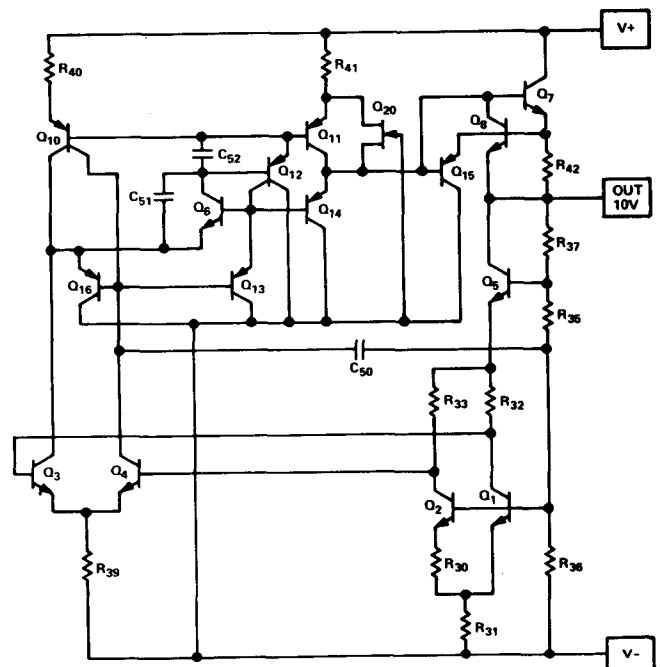


Figure 5. Simplified Schematic

## VOLTAGE VARIATION vs. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of nonlinearities in temperature characteristics, which originated in standard zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD581 consistently follows the S-curve shown in Figure 6. Five-point measurement of each device guarantees the error band over the -55°C to +125°C range; three-point measurement guarantees the error band from 0 to +70°C.

The error band which is guaranteed with the AD581 is the maximum deviation from the initial value at +25°C; this error band is of more use to a designer than one which simply guarantees the maximum total change over the entire range (i.e., in the latter definition, all of the changes could occur in the positive direction). Thus, with a given grade of the AD581, the designer can easily determine the maximum total error from initial tolerance plus temperature variation (e.g., for the AD581T, the initial tolerance is ±10mV, the temperature error band is ±15mV, thus the unit is guaranteed to be 10.000 volts ±25mV from -55°C to +125°C).

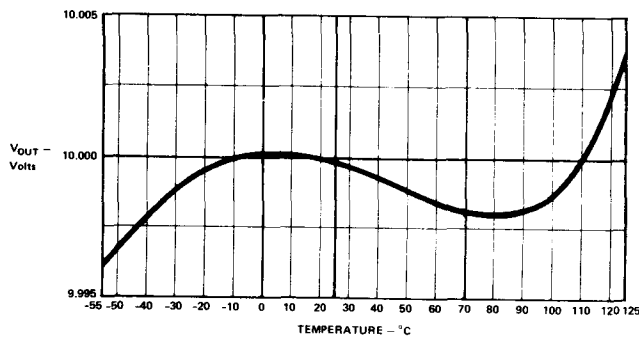


Figure 6. Typical Temperature Characteristic

## OUTPUT CURRENT CHARACTERISTICS

The AD581 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device are shown in Figure 7. Source current is displayed as negative current in the figure; sink current is

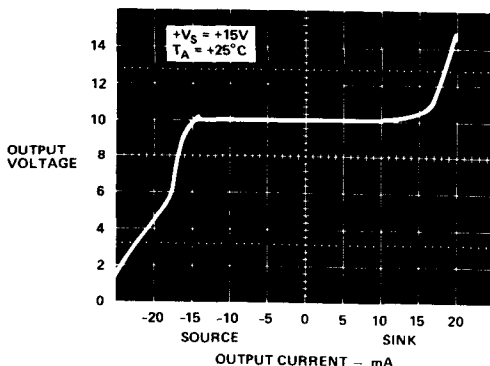


Figure 7. AD581 Output Voltage vs. Sink and Source Current

rent is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

## DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 8 displays the turn-on characteristic of the AD581. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 180μs, and there is no long thermal tail appearing after the point.

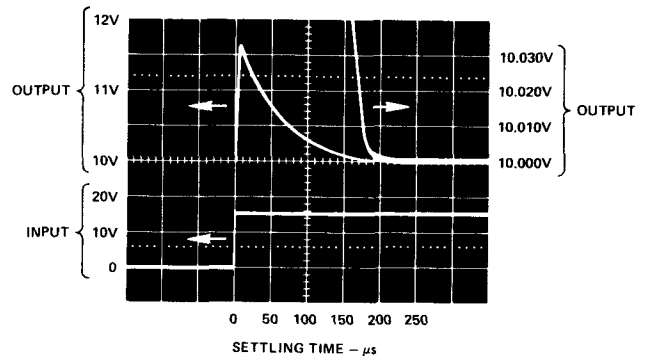


Figure 8. Output Settling Characteristic

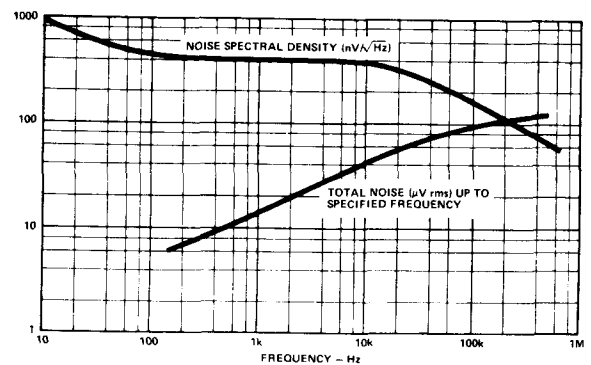


Figure 9. Spectral Noise Density and Total rms Noise vs. Frequency

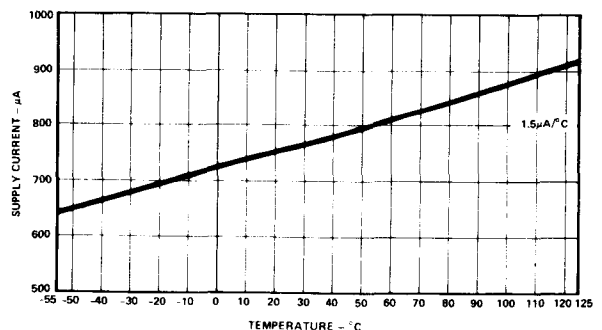


Figure 10. Quiescent Current vs. Temperature

### PRECISION HIGH CURRENT SUPPLY

The AD581 can be easily connected with power pnp or power darlington pnp devices to provide much greater output current capability. The circuit shown in Figure 11 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1 $\mu$ F capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

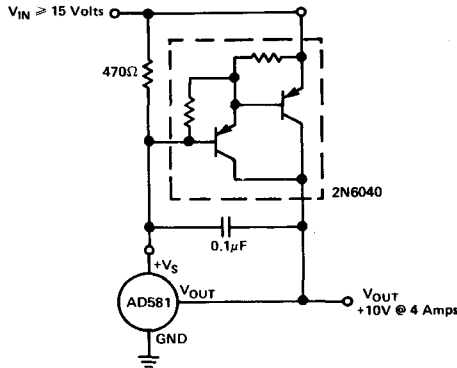


Figure 11. High Current Precision Supply

### CONNECTION FOR REDUCED PRIMARY SUPPLY

While line regulation is specified down to 13 volts, the typical AD581 will work as specified down to 12 volts or below. The current sink capability allows even lower supply voltage capability such as operation from 12V  $\pm$ 5% as shown in Figure 12. The 560 $\Omega$  resistor reduces the current supplied by the AD581 to a manageable level at full 5mA load. Note that other band-gap references, without current sink capability, may be damaged by use in this circuit configuration.

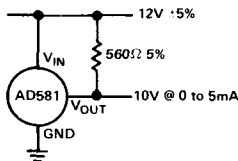


Figure 12. 12 Volt Supply Connection

### THE AD581 AS A CURRENT LIMITER

The AD581 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD581 approach is not limited to a defined set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor. Of course, the minimum voltage required to drive the connection is 13 volts. The AD580, which is a 2.5 volt reference, can be used in this type of circuit with compliance voltage down to 4.5 volts.

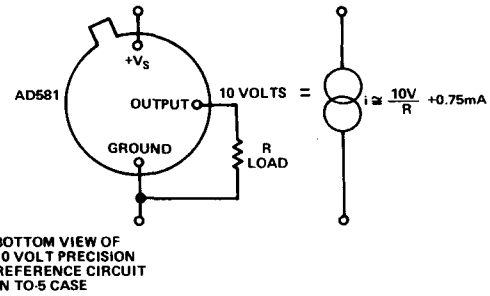


Figure 13. A Two-Component Precision Current Limiter

### NEGATIVE 10-VOLT REFERENCE

The AD581 can also be used in a two-terminal "zener" mode to provide a precision -10.00 volt reference. As shown in Figure 14, the V\_IN and V\_OUT terminals are connected together to the high supply (in this case, ground). The ground pin is connected through a resistor to the negative supply. The output is now taken from the ground pin instead of V\_OUT. With 1mA flowing through the AD581 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2 $\Omega$  typical to 2 ohms. It is essential to arrange the output load and the supply resistor, R<sub>S</sub>, so that the net current through the AD581 is always between 1 and 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard three-terminal mode. The operating temperature range is limited to -55°C to +85°C.

The AD581 can also be used in a two-terminal mode to develop a positive reference. V\_IN and V\_OUT are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 10.5 volts. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD581 always remains within its regulating range of 1 to 5mA.

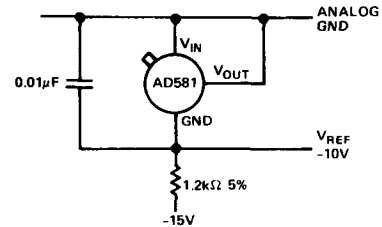


Figure 14. Two-Terminal -10 Volt Reference



### 10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD581 is ideal for application with the entire AD7520 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7570 10-bit A/D converter. In the standard hook-up, as shown in Figure 15, the +10 volt reference is inverted by the amplifier/DAC configuration to produce a 0 to -10 volt range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. If a 0 to +10 volt full scale range is desired, the AD581 can be connected to the CMOS DAC in its -10 volt "zener" mode, as shown in Figure 14 (the -10V<sub>REF</sub> output is connected directly to the V<sub>REF IN</sub> of the CMOS DAC). The AD581 will normally be used in the -10 volt mode with the AD7570 to give a 0 to +10 volt ADC range. This is shown in Figure 16. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

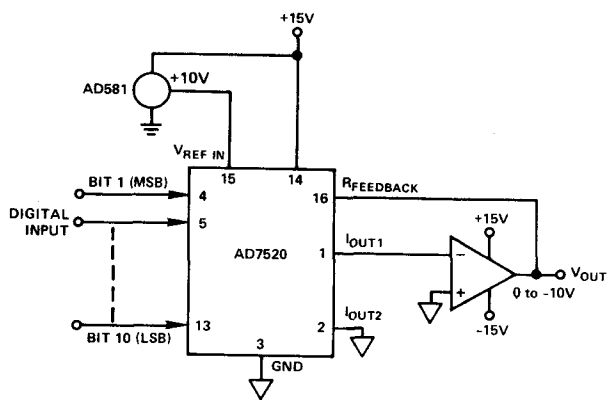


Figure 15. Low Power 10-Bit CMOS DAC Application

### PRECISION 12-BIT D/A CONVERTER REFERENCE

The AD562, like most D/A converters, is designed to operate with a +10 volt reference element. In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD581L (at 5ppm/°C) as the 10 volt reference guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C.

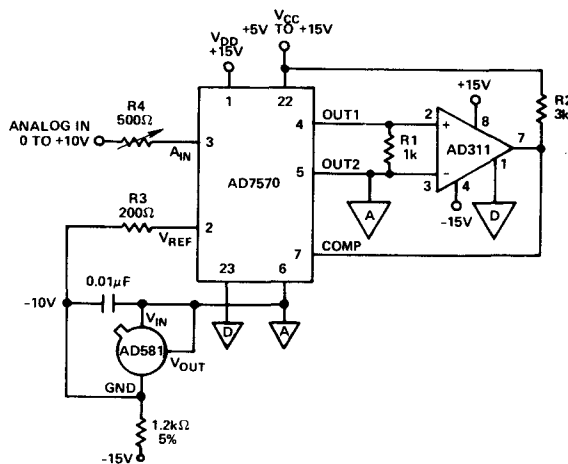


Figure 16. AD581 as Negative 10 Volt Reference for CMOS ADC

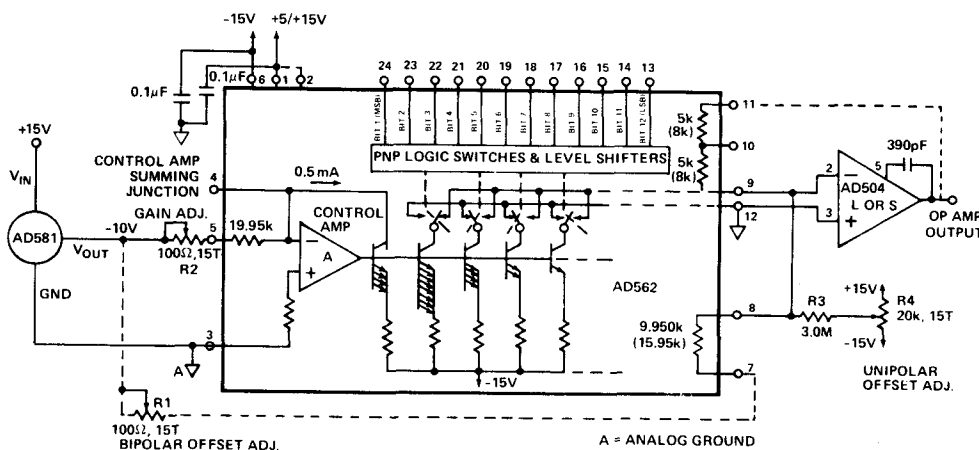


Figure 17. Precision 12-Bit D/A Converter

**FEATURES**

**Four Programmable Output Voltages:**  
10.000V, 7.500V, 5.000V, 2.500V  
**Laser-Trimmed to High Accuracies**  
**No External Components Required**  
**Trimmed Temperature Coefficient:**  
5ppm/°C max, 0 to +70°C (AD584LH)  
10ppm/°C max, -55°C to +125°C (AD584UH)  
**Zero Output Strobe Terminal Provided**  
**Two Terminal Negative Reference**  
**Capability (5V & Above)**  
**Output Sources or Sinks Current**  
**Low Quiescent Current: 1.0mA max**  
**10mA Current Output Capability**  
**Low Cost**

**PRODUCT DESCRIPTION**

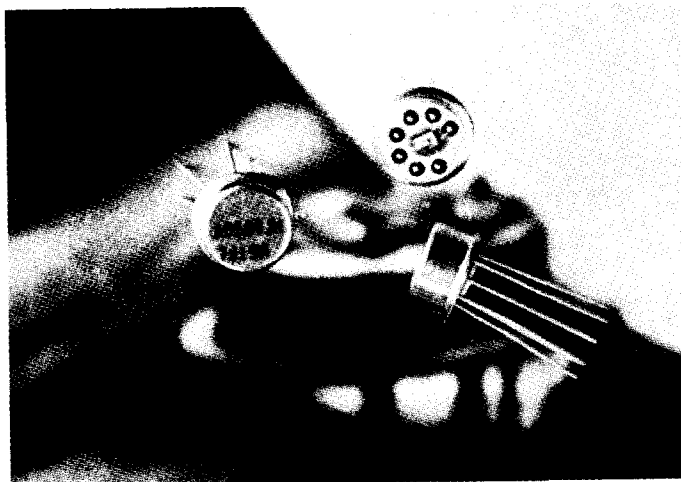
The AD584 is an eight-terminal precision voltage reference offering pin-programmable selection of four popular output voltages: 10.000V, 7.500V, 5.000V and 2.500V. Other output voltages, above, below or between the four standard outputs, are available by the addition of external resistors. Input voltage may vary between 4.5 and 40 volts.

Laser Wafer Trimming (LWT) is used to adjust the pin-programmable output levels and temperature coefficients, resulting in the most flexible high precision voltage reference available in monolithic form.

In addition to the programmable output voltages, the AD584 offers a unique strobe terminal which permits the device to be turned on or off. When the AD584 is used as a power supply reference, the supply can be switched off with a single, low-power signal. In the "off" state the current drain by the AD584 is reduced to about 100 $\mu$ A. In the "on" state the total supply current is typically 750 $\mu$ A including the output buffer amplifier.

The AD584 is recommended for use as a reference for 8, 10 or 12 bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters of up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD584J, K, and L are specified for operation from 0 to +70°C; the AD584S, T, and U are specified for the -55°C to +125°C range. The AD581S, T, and U grades are also available processed to MIL-STD-883B, Level B. All grades are packaged in a hermetically-sealed eight-terminal TO-99 metal can.

**PRODUCT HIGHLIGHTS**

1. The flexibility of the AD584 eliminates the need to design-in and inventory several different voltage references. Furthermore one AD584 can serve as several references simultaneously when buffered properly.
2. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD584LH has a maximum deviation from 10.000 volts of  $\pm 7.25$  mV from 0 to +70°C, while the AD584UH guarantees  $\pm 15$  mV maximum total error without external trims from -55°C to +125°C.
3. The AD584 can be operated in a two-terminal "Zener" mode at 5 volts output and above. By connecting the input and the output, the AD584 can be used in this "Zener" configuration as a negative reference.
4. The output of the AD584 is configured to sink or source currents. This means that small reverse currents can be tolerated in circuits using the AD584 without damage to the reference and without disturbing the output voltage (10V, 7.5V and 5V outputs).
5. Every AD584 is baked for 48 hours at +200°C, temperature cycled 10 times from -65°C to +150°C, and given a high-G shock test prior to final test to ensure reliability and long-term stability.

\*COVERED BY U.S. PATENT NO. 3,887,863.

# SPECIFICATIONS (typical @ $V_{IN} = +15V$ and $+25^{\circ}C$ unless otherwise noted)

| MODEL  | AD584JH                           | AD584KH               | AD584LH               | AD584SH                           | AD584TH               | AD584UH               |
|--|-----------------------------------|-----------------------|-----------------------|-----------------------------------|-----------------------|-----------------------|
| <b>ABSOLUTE MAX RATINGS</b>  |                                   |                       |                       |                                   |                       |                       |
| Input Voltage $V_{IN}$ to Ground   | 40V                               | *                     | *                     | *                                 | *                     | *                     |
| Power Dissipation @ $+25^{\circ}C$   | 600mW                             | *                     | *                     | *                                 | *                     | *                     |
| Operating Junction Temp. Range   | $-55^{\circ}C$ to $+150^{\circ}C$ | *                     | *                     | *                                 | *                     | *                     |
| Storage Temperature Range  | $-65^{\circ}C$ to $+175^{\circ}C$ | *                     | *                     | *                                 | *                     | *                     |
| Lead Temperature   |                                   |                       |                       |                                   |                       |                       |
| Soldering, 10sec)  | $+300^{\circ}C$                   | *                     | *                     | *                                 | *                     | *                     |
| Thermal Resistance   |                                   |                       |                       |                                   |                       |                       |
| Junction-to-Ambient  | $150^{\circ}C/Watt$               | *                     | *                     | *                                 | *                     | *                     |
| Operating Temperature Range  | 0 to $+70^{\circ}C$               | *                     | *                     | $-55^{\circ}C$ to $+125^{\circ}C$ | **                    | **                    |
| <b>OUTPUT VOLTAGE TOLERANCE</b>  |                                   |                       |                       |                                   |                       |                       |
| Maximum Error <sup>1</sup> for Nominal Outputs of:                               |                                   |                       |                       |                                   |                       |                       |
| 10.000V  | $\pm 30mV$                        | $\pm 10mV$            | $\pm 5mV$             | $\pm 30mV$                        | $\pm 10mV$            | $\pm 5mV$             |
| 7.500V   | $\pm 22mV$                        | $\pm 8mV$             | $\pm 4mV$             | $\pm 22mV$                        | $\pm 8mV$             | $\pm 4mV$             |
| 5.000V   | $\pm 15mV$                        | $\pm 6mV$             | $\pm 3mV$             | $\pm 15mV$                        | $\pm 6mV$             | $\pm 3mV$             |
| 2.500V   | $\pm 7.5mV$                       | $\pm 3.5mV$           | $\pm 2.5mV$           | $\pm 7.5mV$                       | $\pm 3.5mV$           | $\pm 2.5mV$           |
| <b>OUTPUT VOLTAGE CHANGE</b>   |                                   |                       |                       |                                   |                       |                       |
| Maximum Deviation from $+25^{\circ}C$ Value, $T_{min}$ to $T_{max}$ <sup>2</sup> |                                   |                       |                       |                                   |                       |                       |
| 10.000, 7.500, 5.000V Outputs  | 30ppm/ $^{\circ}C$                | 15ppm/ $^{\circ}C$    | 5ppm/ $^{\circ}C$     | 30ppm/ $^{\circ}C$                | 15ppm/ $^{\circ}C$    | 10ppm/ $^{\circ}C$    |
| 2.500V Output  | 30ppm/ $^{\circ}C$                | 15ppm/ $^{\circ}C$    | 10ppm/ $^{\circ}C$    | 30ppm/ $^{\circ}C$                | 20ppm/ $^{\circ}C$    | 15ppm/ $^{\circ}C$    |
| Differential Temperature Coefficients Between Outputs                            | 5ppm/ $^{\circ}C$ typ             | 3ppm/ $^{\circ}C$ typ | 3ppm/ $^{\circ}C$ typ | 5ppm/ $^{\circ}C$ typ             | 3ppm/ $^{\circ}C$ typ | 3ppm/ $^{\circ}C$ typ |
| <b>QUIESCENT CURRENT</b>   |                                   |                       |                       |                                   |                       |                       |
|  | 1.0mA max                         | *                     | *                     | *                                 | *                     | *                     |
| Temperature Variation  | $750\mu A$ typ                    | *                     | *                     | *                                 | *                     | *                     |
|  | $1.5\mu A/^{\circ}C$ typ          | *                     | *                     | *                                 | *                     | *                     |
| <b>TURN-ON SETTLING TIME TO 0.1%</b>   |                                   |                       |                       |                                   |                       |                       |
|  | 200 $\mu s$                       | *                     | *                     | *                                 | *                     | *                     |
| <b>NOISE</b>   |                                   |                       |                       |                                   |                       |                       |
| (0.1 to 10Hz)  | 50 $\mu V$ p-p                    | *                     | *                     | *                                 | *                     | *                     |
| <b>LONG-TERM STABILITY</b>   |                                   |                       |                       |                                   |                       |                       |
|  | 25ppm/1000 Hrs. (Non-Cumulative)  | *                     | *                     | *                                 | *                     | *                     |
| <b>SHORT CIRCUIT CURRENT</b>   |                                   |                       |                       |                                   |                       |                       |
|  | 30mA                              | *                     | *                     | *                                 | *                     | *                     |
| <b>LINE REGULATION (No Load)</b>   |                                   |                       |                       |                                   |                       |                       |
| $15V < V_{IN} < 30V$   | 0.002%/V                          | *                     | *                     | *                                 | *                     | *                     |
| $(V_{OUT} + 2.5V) < V_{IN} < 15V$  | 0.005%/V                          | *                     | *                     | *                                 | *                     | *                     |
| <b>LOAD REGULATION</b>   |                                   |                       |                       |                                   |                       |                       |
| $0 < I_{OUT} < 5mA$ , All Outputs  | 50ppm/mA max (20ppm/mA typ)       | *                     | *                     | *                                 | *                     | *                     |
| <b>OUTPUT CURRENT</b>  |                                   |                       |                       |                                   |                       |                       |
| $V_{IN} > V_{OUT} + 2.5V$  |                                   |                       |                       |                                   |                       |                       |
| Source @ $+25^{\circ}C$  | 10mA min                          | *                     | *                     | *                                 | *                     | *                     |
| Source $T_{min}$ to $T_{max}$  | 5mA min                           | *                     | *                     | *                                 | *                     | *                     |
| Sink $T_{min}$ to $T_{max}$  | 5mA min                           | *                     | *                     | 200 $\mu A$ min                   | **                    | **                    |
| Sink $-55^{\circ}C$ to $+85^{\circ}C$  | —                                 | —                     | —                     | 5mA min                           | **                    | **                    |

\*Specifications same as AD584JH.

\*\*Specifications same as AD584SH.

<sup>1</sup> At Pin 1.

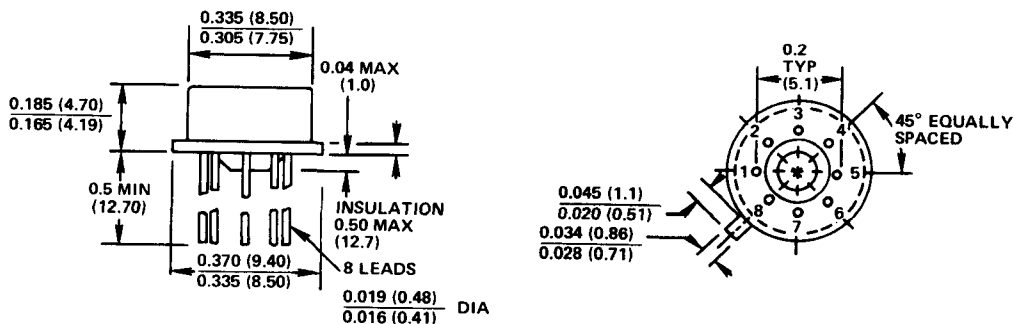
<sup>2</sup> Calculated as average over the operating temperature range.

Specifications and prices subject to change without notice.

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### TO-99 CAN



## APPLYING THE AD584

With power applied to pins 8 and 4 and all other pins open the AD584 will produce a buffered nominal 10.0V output between pins 1 and 4 (see Figure 1). The stabilized output voltage can be reduced to 7.5V, 5.0V or 2.5V by connecting the programming pins as follows:

| OUTPUT VOLTAGE | PIN PROGRAMMING                                 |
|----------------|---|
| 7.5V           | Join the 2.5V and 5.0V pins (2) and (3).        |
| 5.0V           | Connect the 5.0V pin (2) to the output pin (1). |
| 2.5V           | Connect the 2.5V pin (3) to the output pin (1). |

The options shown above are available without the use of any additional components. Multiple outputs using only one AD584, are also possible by simply buffering each voltage programming pin with a unity-gain noninverting op amp.

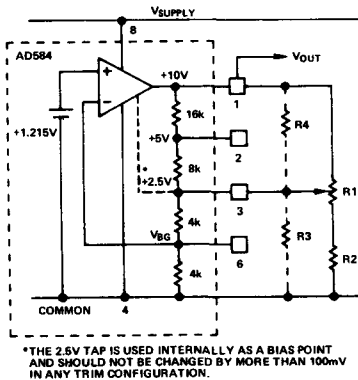


Figure 1. Variable Output Options

The AD584 can also be programmed over a wide range of output voltages, including voltages greater than 10V, by the addition of one or more external resistors. Figure 1 illustrates the general adjustment procedure, with approximate values given for the internal resistors of the AD584. The AD584 may be modeled as an op amp with a noninverting feedback connection, driven by a high stability 1.215 volt bandgap reference (see Figure 5 for schematic).

When the feedback ratio is adjusted with external resistors, the output amplifier can be made to multiply the reference voltage by almost any convenient amount, making popular outputs of 10.24V, 5.12V, 2.56V or 6.3V easy to obtain. The most general adjustment (which gives the greatest range and poorest resolution) uses R1 and R2 alone (see Figure 1). As R1 is adjusted to its upper limit the 2.5V pin 3 will be connected to the output, which will reduce to 2.5V. As R1 is adjusted to its lower limit, the output voltage will rise to a value limited by R2. For example, if R2 is about 6kΩ, the upper limit of the output range will be about 20V even for large values of R1. R2 should not be omitted; its value should be chosen to limit the output to a value which can be tolerated by the load circuits. If R2 is zero, adjusting R1 to its lower limit will result in a loss of control over the output voltage. If precision voltages are required to be set at levels other than the standard outputs, the 20% absolute tolerance in the internal resistor ladder must be accounted for.

Alternatively, the output voltage can be raised by loading the

2.5V tap with R3 alone. The output voltage can be lowered by connecting R4 alone. Either of these resistors can be a fixed resistor selected by test or an adjustable resistor. In all cases the resistors should have a low temperature coefficient to match the AD584 internal resistors, which have a negative T.C. less than 60ppm/°C. If both R3 and R4 are used, these resistors should have matched temperature coefficients.

When only small adjustments or trims are required, the circuit of Figure 2 offers better resolution over a limited trim range. The circuit can be programmed to 5.0V, 7.5V or 10V and adjusted by means of R1 over a range of about ±200mV. To trim the 2.5V output option, R2 (Figure 2) can be reconnected to the bandgap reference (pin 6). In this configuration, the adjustment should be limited to ±100mV in order to avoid affecting the performance of the AD584.

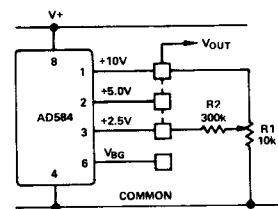


Figure 2. Output Trimming

## PIN DESIGNATION

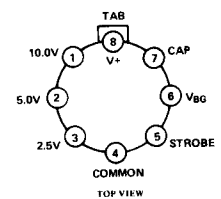
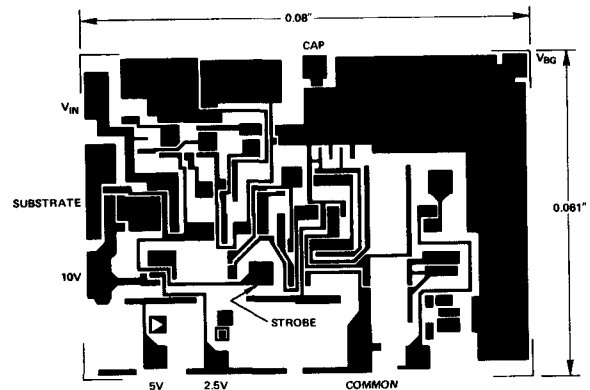


Figure 3. Pin Designations



THE AD584 IS ALSO AVAILABLE IN LASER-TRIMMED CHIP FORM WITH ALL SPECIFICATIONS GUARANTEED TO J-GRADE; +25°C SPECIFICATIONS ONLY. CONSULT FACTORY FOR FURTHER DETAILS.

Figure 4. Bonding Diagram

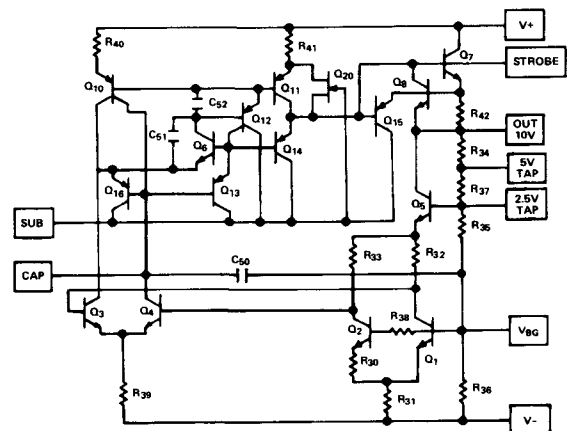


Figure 5. Schematic Diagram

# Performance of the AD584

## PERFORMANCE OVER TEMPERATURE

Each AD584 is tested at five temperatures over the  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  range to ensure that each device falls within the Maximum Error Band (see Figure 6) specified for a particular grade (i.e., S, T, or U grades); three-point measurement guarantees performance within the error band from 0 to  $+70^{\circ}\text{C}$ . (i.e., J, K, or L grades). The error band guaranteed for the AD584 is the maximum deviation from the initial value at  $+25^{\circ}\text{C}$ . Thus, given the grade of the AD584, the designer can easily determine the maximum total error from initial tolerance plus temperature variation. For example, for the AD584T, the initial tolerance is  $\pm 10\text{mV}$  and the error band is  $\pm 15\text{mV}$ . Hence, the unit is guaranteed to be  $10.000\text{ volts} \pm 25\text{mV}$  from  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

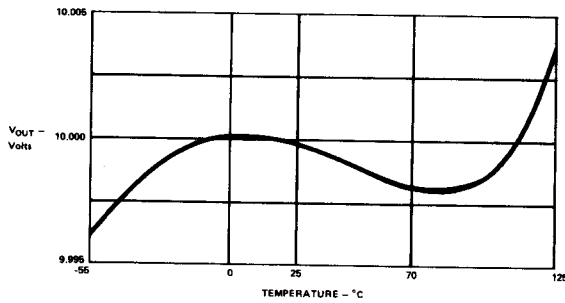


Figure 6. Typical Temperature Characteristic

## OUTPUT CURRENT CHARACTERISTICS

The AD584 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device is shown in Figure 7. Source current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA, when shorted to +15 volts, the sink current goes to about 20mA.

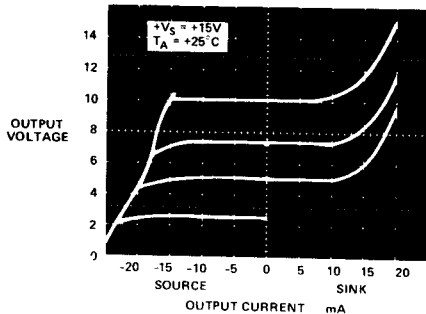


Figure 7. AD584 Output Voltage vs. Sink and Source Current

## DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 8 displays the turn-on characteristic of the AD584. Figure 8A is generated from cold-start operation

and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within  $\pm 1$  millivolt is about  $180\mu\text{s}$ , and there is no long thermal tail appearing after the point. Figure 8B demonstrates the settling characteristics using the strobe input (see Figure 11). Without compensation, the output of the AD584 typically settles within  $225\mu\text{s}$ . With a  $90\text{pF}$  capacitor across pins (5) and (3), critical damping is approximated, as shown in Figure 8B, with settling times  $< 5\mu\text{s}$ .

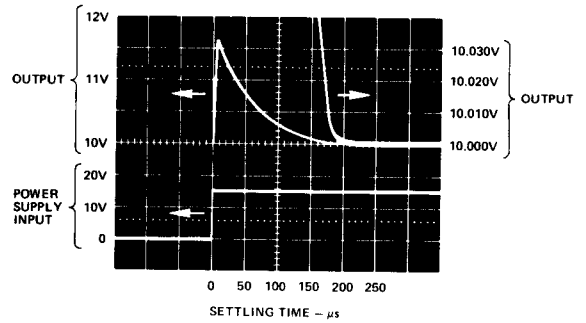


Figure 8a. Output Settling Characteristic

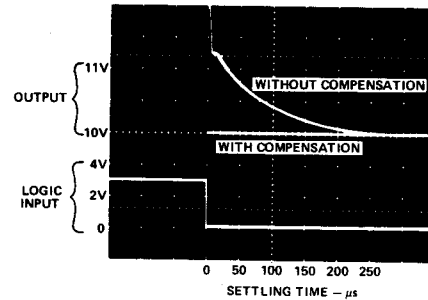


Figure 8b. Output Settling Characteristic

## NOISE FILTERING

The bandwidth of the output amplifier in the AD584 can be reduced to filter the output noise. A capacitor ranging between  $0.01\mu\text{F}$  and  $0.1\mu\text{F}$  connected between the Cap and  $V_{\text{BG}}$  terminals will further reduce the wideband and feedthrough noise in the output of the AD584, as shown in Figure 10.

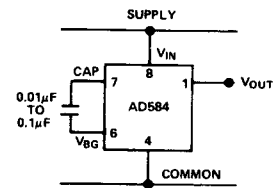


Figure 9. Additional Noise Filtering with an External Capacitor

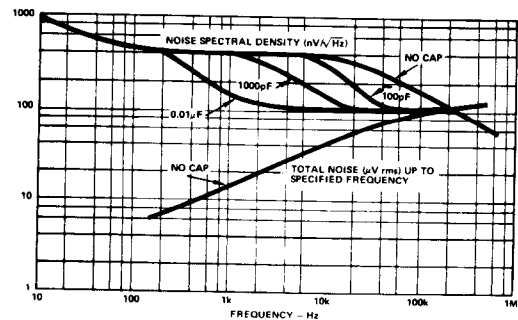


Figure 10. Spectral Noise Density and Total rms Noise vs. Frequency

## USING THE STROBE TERMINAL

The AD584 has a strobe input which can be used to zero the output. This unique feature permits a variety of new applications in signal and power conditioning circuits.

Figure 11 illustrates the strobe connection. A simple NPN switch can be used to translate a TTL logic signal into a strobe of the output. The AD584 operates normally when there is no current drawn from pin 5. Bringing this terminal low, to less than 200mV, will allow the output voltage to go to zero. In this mode the AD584 should not be required to source or sink current (unless a 0.7V residual output is permissible). If the AD584 is required to sink a transient current while strobed off, the strobe terminal input current should be limited by a 100Ω resistor as shown in Figure 11.

The strobe terminal will tolerate up to 5μA leakage and its driver should be capable of sinking 500μA continuous. A low leakage open collector gate can be used to drive the strobe terminal directly, provided the gate can withstand the AD584 output voltage plus one volt.

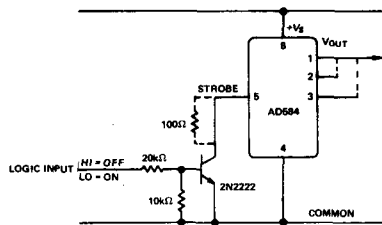


Figure 11. Use of the Strobe Terminal

## PRECISION HIGH CURRENT SUPPLY

The AD584 can be easily connected to a power PNP or power Darlington PNP device to provide much greater output current capability. The circuit shown in Figure 12 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

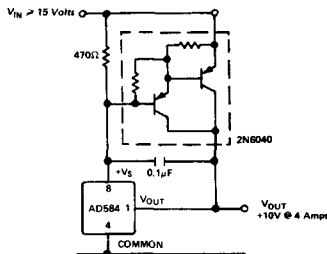


Figure 12. High Current Precision Supply

The AD584 can also use an NPN or Darlington NPN transistor to boost its output current. Simply connect the 10V output terminal of the AD584 to the base of the NPN booster and take the output from the booster emitter as shown in Figure 13. The 5.0V or 2.5V pin must connect to the actual output in this configuration. Variable or adjustable outputs (as shown in Figures 1 and 2) may be combined with +5.0V connection to obtain outputs above +5.0V.

## THE AD584 AS A CURRENT LIMITER

The AD584 represents an alternative to current limiter diodes which require factory selection to achieve a desired current.

Use of current limiting diodes often results in temperature coefficients of 1%/°C. Use of the AD584 in this mode is not limited to a set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor (see Figure 14). Of course, the minimum voltage required to drive the connection is 5 volts.

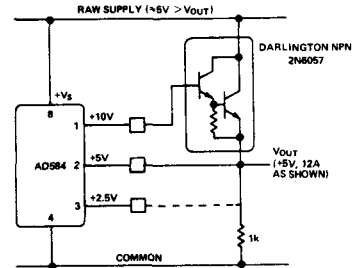


Figure 13. NPN Output Current Booster

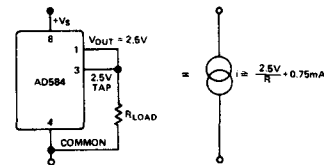


Figure 14. A Two-Component Precision Current Limiter

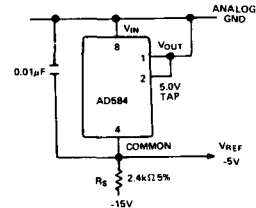


Figure 15. Two-Terminal -5 Volt Reference

## NEGATIVE REFERENCE VOLTAGES FROM AN AD584

The AD584 can also be used in a two-terminal "zener" mode to provide a precision -10, -7.5 or -5.0 volt reference. As shown in Figure 15, the  $V_{IN}$  and  $V_{OUT}$  terminals are connected together to the positive supply (in this case, ground). The AD584 common pin is connected through a resistor to the negative supply. The output is now taken from the common pin instead of  $V_{OUT}$ . With 1mA flowing through the AD584 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2Ω. It is essential to arrange the output load and the supply resistor,  $R_S$ , so that the net current through the AD584 is always between 1 and 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard three-terminal mode. The operating temperature range is limited to -55°C to +85°C.

The AD584 can also be used in a two-terminal mode to develop a positive reference.  $V_{IN}$  and  $V_{OUT}$  are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 0.5 volts above the desired output voltage. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD584 always remains within its regulating range of 1 to 5mA.

## 10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD584 is ideal for application with the entire AD7520 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7570 10-bit A/D converter. In the standard hook-up, as shown in Figure 16, the standard output voltages are inverted by the amplifier/DAC configuration to produce converted voltage ranges. For example, a +10V reference produces a 0 to -10V range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. If a 0 to +10 volt full scale range is desired, the AD584 can be connected to the CMOS DAC in its -10 volt "zener" mode, as shown in Figure 18 (the -10V<sub>REF</sub> output is connected directly to the V<sub>REF IN</sub> of the CMOS DAC). The AD584 will normally be used in the -10 volt mode with the AD7570 to give a 0 to +10 volt ADC range. This is shown in Figure 18. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

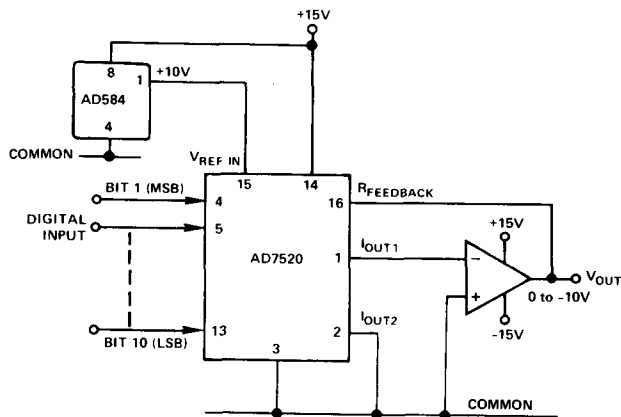


Figure 16. Low Power 10-Bit CMOS DAC Application

## PRECISION D/A CONVERTER REFERENCE

The AD562, like many D/A converters, is designed to operate with a +10 volt reference element (Figure 17). In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD584L (at 5ppm/°C) as the 10 volt reference

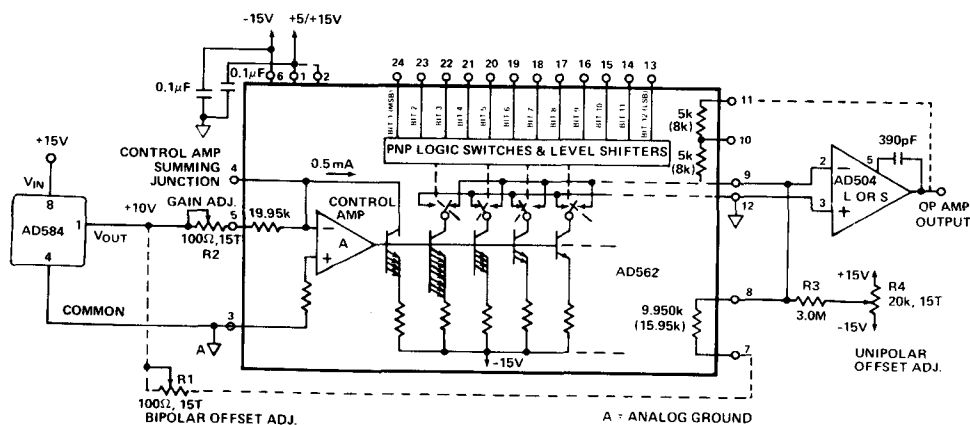


Figure 17. Precision 12-Bit D/A Converter

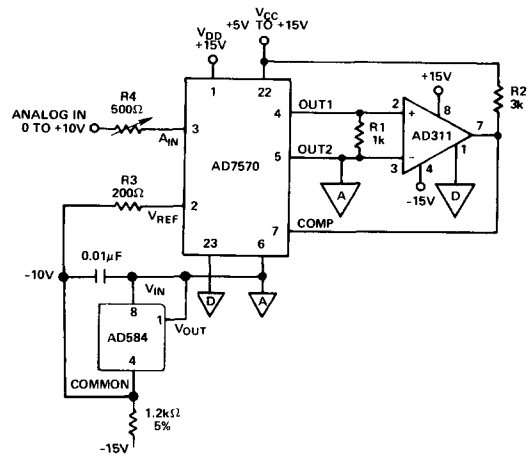


Figure 18. AD584 as Negative 10 Volt Reference for CMOS ADC

guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C. Figure 19 demonstrates the flexibility of the AD584 applied to another popular D/A configuration.

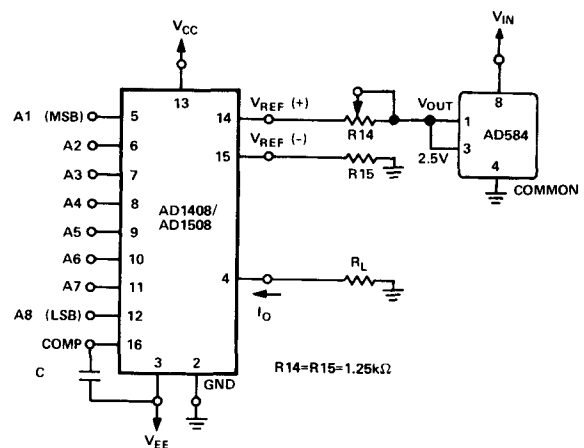
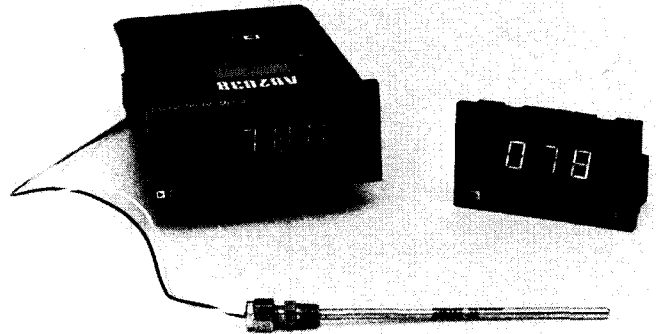


Figure 19. Current Output 8-Bit D/A

**FEATURES**

Linear Current Output:  $1\mu\text{A}/\text{K}$   
Wide Range:  $-55^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$   
Laser Trimmed Sensor (AD590) to  $\pm 0.5^{\circ}\text{C}$  Calibration Accuracy (AC2626M)  
Excellent Linearity:  $\pm 0.3^{\circ}\text{C}$  Over Full Range (AC2626M)  
6 Inch or 4 Inch Standard, Stainless Steel Sheath  
3/16 Inch in Outside Diameter  
3 Feet Teflon Coated Lead Wire  
Wide Power Supply Range +4V to +30V  
Low Cost  
Fast Response: 2 Seconds (In Stirred Water)  
Sensor Isolated From Sheath

**PRODUCT DESCRIPTION**

The AC2626 is a stainless steel tubular probe measuring 3/16 inch (4.76mm) in outside diameter and is available in 6 inch (152.4mm) or 4 inch (101.6mm) lengths. Based on the new AD590F, the probe is available in linearity grades of  $0.3^{\circ}\text{C}$ ,  $0.4^{\circ}\text{C}$ ,  $0.8^{\circ}\text{C}$  or  $1.5^{\circ}\text{C}$ .

The probe is designed for both liquid and gaseous immersion applications as well as temperature measurements in refrigeration or any general temperature monitoring application.

For taking measurements in pipes or other closed vessels, the AC2629 compression fitting is available. The AC2629 may be applied anywhere along the probe and is supplied in two materials. The low cost AC2629B is constructed of brass and the higher priced AC2629SS is made of stainless steel.

**PRODUCT HIGHLIGHTS**

The AC2626 is based on the AD590 temperature transducer, a two terminal integrated circuit which produces an output current linearly proportional to absolute temperature.

Costly linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AC2626.

Due to the high impedance current output of the AD590, the AC2626 is particularly useful in remote sensing applications, because of its insensitivity to voltage drops over lines. The output characteristics also make the AC2626 easy to multiplex.

In addition to temperature measurement, applications include temperature compensation, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry.

**DIRECT INTERFACE PRODUCTS**

For display and/or control applications, two companion products are available. The AD2038, 6 channel digital thermometer,

and the AD2040, low cost temperature indicator, were designed to be used in conjunction with the AC2626 (AD590).

1. The AD2038 is a low cost, ac line powered 6 channel digital scanning thermometer designed to interface to printers, computers, serial data transmitters, etc., for display, control, logging or transmission of multi-point temperature data. Channel selection is made via three methods: manual, using the switch provided on the front; auto/scan, where the AD2038 cycling on an internal clock can continually scan the six input channels or external selection, where control inputs provided on the rear connector enable channel selection via external BCD coding.
2. The AD2040 is a low cost, 3 digit temperature indicator. An internal precision voltage reference, resistor network and span and zero adjusts allow the AD2040 to read out directly in  $^{\circ}\text{C}$ ,  $^{\circ}\text{F}$ , K or R. User selectable readout as well as all other connection, i.e., +5V dc power and AC2626 (AD590) interface are all made via the terminal block on the rear.

**APPLICATION HINTS**

1. Under all operating conditions, 4V dc must be present across the AD590.
2. Use of twisted pair wiring is recommended, particularly for remote applications or in high noise environments. Shielded wire is desirable in severe noise environments.
3. For the lowest cost impact, the J and K grades are recommended if calibration means are convenient. Where probe interchangeability is desired, grades L and M are recommended.



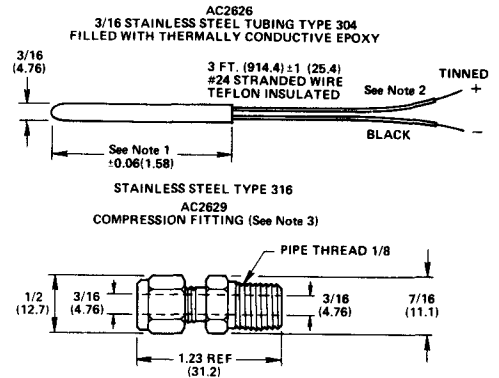
# SPECIFICATIONS

(typical @ +25°C and +5V unless otherwise specified)

| MODEL   | AC2626J         | AC2626K    | AC2626L    | AC2626M    |
|---|-----------------|------------|------------|------------|
| <b>ABSOLUTE MAXIMUM RATINGS</b>                           |                 |            |            |            |
| Forward Voltage ( $V_S$ )                                 | +44V            | *          | *          | *          |
| Reverse Voltage ( $V_S$ )                                 | -20V            | *          | *          | *          |
| Breakdown Voltage (Case to Leads)                         | ±200V           | *          | *          | *          |
| Rated Performance Temp. Range                             | -55°C to +150°C | *          | *          | *          |
| Storage Temperature Range                                 | -60°C to +170°C | *          | *          | *          |
| <b>POWER SUPPLY</b>                                       |                 |            |            |            |
| Operating Voltage Range                                   | +4V to +30V     | *          | *          | *          |
| <b>OUTPUT</b>   |                 |            |            |            |
| Nominal Current Output @ +25°C (298.2°K)                  | 298.2µA         | *          | *          | *          |
| Nominal Temperature Coefficient                           | 1µA/°C          | *          | *          | *          |
| Calibration Error @ +25°C                                 | ±5.0°C max      | ±2.5°C max | ±1.0°C max | ±0.5°C max |
| Absolute Error (over rated performance temperature range) |                 |            |            |            |
| Without External Calibration Adjustment                   |                 |            |            |            |
| Set to Zero   | ±10.0°C max     | ±5.5°C max | ±3.0°C max | ±1.7°C max |
| With +25°C Calibration Error                              |                 |            |            |            |
| Set to Zero   | ±3.0°C max      | ±2.0°C max | ±1.6°C max | ±1.0°C max |
| Nonlinearity  | ±1.5°C max      | ±0.8°C max | ±0.4°C max | ±0.3°C max |
| Repeatability <sup>1</sup>                                | 0.1°C           | *          | *          | *          |
| Long Term Drift <sup>2</sup>                              | 0.1°C max       | *          | *          | *          |
| Time Constant <sup>3</sup> (in stirred water)             | 2 sec.          | *          | *          | *          |
| Current Noise   | 40pA√Hz         | *          | *          | *          |
| <b>Power Supply Rejection</b>                             |                 |            |            |            |
| +4V ≤ $V_S$ ≤ +5V   | 0.5µA/V         | *          | *          | *          |
| +5V ≤ $V_S$ ≤ +15V  | 0.2µA/V         | *          | *          | *          |
| +15V ≤ $V_S$ ≤ +30V                                       | 0.1µA/V         | *          | *          | *          |
| Electrical Turn-On Time                                   | 20µs            | *          | *          | *          |
| + Lead Color  | yellow          | orange     | blue       | green      |

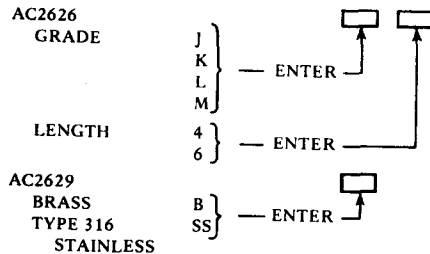
## MECHANICAL OUTLINE

Dimensions shown in inches and (mm).



- NOTE 1 Probes are available in 4-inch or 6-inch lengths. Other lengths are available; consult factory for price and delivery.
- NOTE 2 + lead wire is color coded: J, yellow; K, orange; L, blue; M, green.
- NOTE 3 When assembling compression fitting (AC2629) to probe, tighten the 1/2" nut 3/4's of a turn from finger tight.

## ORDERING GUIDE

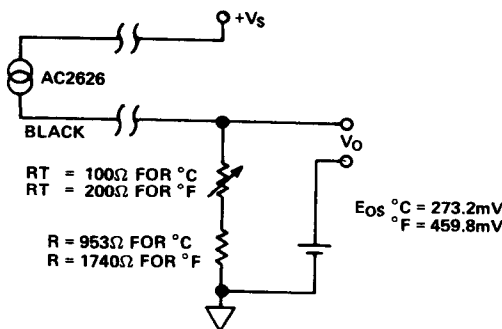


## NOTES

- <sup>1</sup> Maximum deviation between +25°C readings after temperature cycling between -55°C and +150°C; guaranteed, not tested.
- <sup>2</sup> Conditions: constant +5V, constant +125°C; guaranteed, not tested.
- <sup>3</sup> The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.

Specifications subject to change without notice.

## CALIBRATION



For most applications, a single point calibration is sufficient. With the probe at a known temperature, adjust  $R_T$  so that  $V_O$  corresponds to the known temperature.

If more detailed information is desired, see the AD590 data sheet and application note.

## FEATURES

**Linear Current Output:  $1\mu\text{A}/^\circ\text{K}$**   
**Wide Range:  $-55^\circ\text{C}$  to  $+150^\circ\text{C}$**   
**Probe Compatible Ceramic Sensor Package**  
**Two-Terminal Device: Voltage In/Current Out**  
**Laser Trimmed to  $\pm 0.5^\circ\text{C}$  Calibration Accuracy (AD590M)**  
**Excellent Linearity:  $\pm 0.3^\circ\text{C}$  Over Full Range Range (AD590M)**  
**Wide Power Supply Range:  $+4\text{V}$  to  $+30\text{V}$**   
**Sensor Isolation from Case**  
**Low Cost**

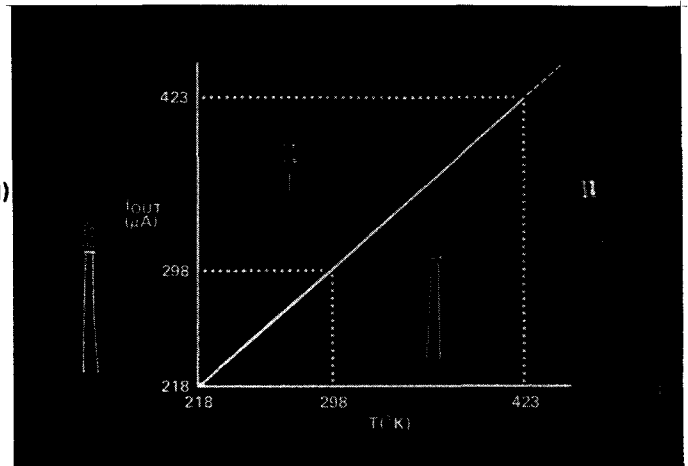
## PRODUCT DESCRIPTION

The AD590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. For supply voltages between  $+4\text{V}$  and  $+30\text{V}$  the device acts as a high impedance, constant current regulator passing  $1\mu\text{A}/^\circ\text{K}$ . Laser trimming of the chip's thin film resistors is used to calibrate the device to  $298.2\mu\text{A}$  output at  $298.2^\circ\text{K}$  ( $+25^\circ\text{C}$ ).

The AD590 should be used in any temperature sensing application below  $+150^\circ\text{C}$  in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AD590.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.



## PRODUCT HIGHLIGHTS

1. The AD590 is a calibrated two terminal temperature sensor requiring only a dc voltage supply ( $+4\text{V}$  to  $+30\text{V}$ ). Costly transmitters, filters, lead wire compensation and linearization circuits are all unnecessary in applying the device.
2. State-of-the-art laser trimming at the wafer level in conjunction with extensive final testing insures that AD590 units are easily interchangeable.
3. Superior interference rejection results from the output being a current rather than a voltage. In addition, power requirements are low ( $1.5\text{mW}$ 's @  $5\text{V}$  @  $+25^\circ\text{C}$ ). These features make the AD590 easy to apply as a remote sensor.
4. The high output impedance ( $>10\text{M}\Omega$ ) provides excellent rejection of supply voltage drift and ripple. For instance, changing the power supply from  $5\text{V}$  to  $10\text{V}$  results in only a  $1\mu\text{A}$  maximum current change, or  $1^\circ\text{C}$  equivalent error.
5. The AD590 is electrically durable: it will withstand a forward voltage up to  $44\text{V}$  and a reverse voltage of  $20\text{V}$ . Hence, supply irregularities or pin reversal will not damage the device.
6. The device is hermetically sealed in both a ceramic sensor package and in the TO-52 package. MIL-STD-883B processing to level B is available and, for large unit volumes, special accuracy requirements over limited temperature ranges can be satisfied by selections at final test. The device is also available in chip form.

# SPECIFICATIONS (typical @ +25°C and $V_S = 5V$ unless otherwise noted)

| MODEL  | AD590I             | AD590J      | AD590K     | AD590L     | AD590M     |
|--|--------------------|-------------|------------|------------|------------|
| <b>ABSOLUTE MAXIMUM RATINGS</b>  |                    |             |            |            |            |
| Forward Voltage (E+ to E-)   | +44V               | *           | *          | *          | *          |
| Reverse Voltage (E+ to E-)   | -20V               | *           | *          | *          | *          |
| Breakdown Voltage (Case to E+ or E-)                                   | ±200V              | *           | *          | *          | *          |
| Rated Performance Temperature Range <sup>1</sup>                       | -55°C to +150°C    | *           | *          | *          | *          |
| Storage Temperature Range <sup>1</sup>                                 | -65°C to +175°C    | *           | *          | *          | *          |
| Lead Temperature (Soldering, 10 sec)                                   | +300°C             | *           | *          | *          | *          |
| <b>POWER SUPPLY</b>  |                    |             |            |            |            |
| Operating Voltage Range  | +4V to +30V        | *           | *          | *          | *          |
| <b>OUTPUT</b>  |                    |             |            |            |            |
| Nominal Current Output @ +25°C (298.2°K)                               | 298.2µA            | *           | *          | *          | *          |
| Nominal Temperature Coefficient  | 1µA/°C             | *           | *          | *          | *          |
| Calibration Error @ +25°C  | ±10.0°C max        | ±5.0°C max  | ±2.5°C max | ±1.0°C max | ±0.5°C max |
| Absolute Error <sup>2</sup> (over rated performance temperature range) |                    |             |            |            |            |
| Without External Calibration Adjustment                                | ±20.0°C max        | ±10.0°C max | ±5.5°C max | ±3.0°C max | ±1.7°C max |
| With +25°C Calibration Error Set to Zero                               | ±5.8°C max         | ±3.0°C max  | ±2.0°C max | ±1.6°C max | ±1.0°C max |
| Nonlinearity   | ±3.0°C max         | ±1.5°C max  | ±0.8°C max | ±0.4°C max | ±0.3°C max |
| Repeatability <sup>3</sup>   | ±0.1°C/month max   | *           | *          | *          | *          |
| Long Term Drift <sup>4</sup>   | ±0.1°C max         | *           | *          | *          | *          |
| Current Noise  | 40pA/√Hz           | *           | *          | *          | *          |
| Power Supply Rejection   |                    |             |            |            |            |
| +4V ≤ $V_S$ ≤ +5V  | 0.5µA/V            | *           | *          | *          | *          |
| +5V ≤ $V_S$ ≤ +15V   | 0.2µA/V            | *           | *          | *          | *          |
| +15V ≤ $V_S$ ≤ +30V  | 0.1µA/V            | *           | *          | *          | *          |
| Case Isolation to Either Lead  | 10 <sup>10</sup> Ω | *           | *          | *          | *          |
| Effective Shunt Capacitance  | 100pF              | *           | *          | *          | *          |
| Electrical Turn-On Time <sup>5</sup>                                   | 20µs               | *           | *          | *          | *          |
| Reverse Bias Leakage Current <sup>6</sup><br>(Reverse Voltage = 10V)   | 10pA               | *           | *          | *          | *          |

\*Specifications same as AD590I

<sup>1</sup>The AD590 has been used at -100°C and +200°C for short periods of measurement with no physical damage to the device. However, the absolute errors specified apply to only the rated performance temperature range.

<sup>2</sup>See page 88S for explanation of error components. Note that ±1°C error is the equivalent of ±1µA error.

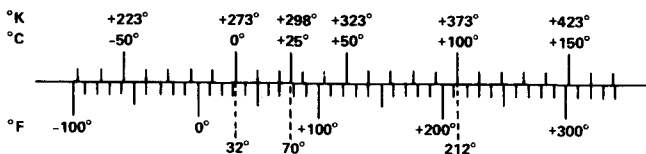
<sup>3</sup>Maximum deviation between +25°C readings after temperature cycling between -55°C and +150°C; guaranteed not tested.

<sup>4</sup>Conditions: constant +5V, constant +125°C; guaranteed, not tested.

<sup>5</sup>Does not include self heating effects; see page 89S for explanation of these effects.

<sup>6</sup>Leakage current doubles every 10°C.

Specifications subject to change without notice.



## TEMPERATURE SCALE CONVERSION EQUATIONS

$$^{\circ}\text{C} = \frac{5}{9} (^{\circ}\text{F} - 32)$$

$$^{\circ}\text{K} = ^{\circ}\text{C} + 273.15$$

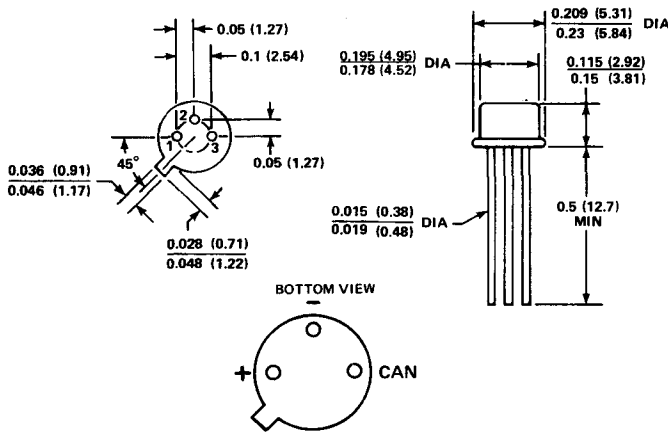
$$^{\circ}\text{F} = \frac{9}{5} ^{\circ}\text{C} + 32$$

$$^{\circ}\text{R} = ^{\circ}\text{F} + 459.7$$

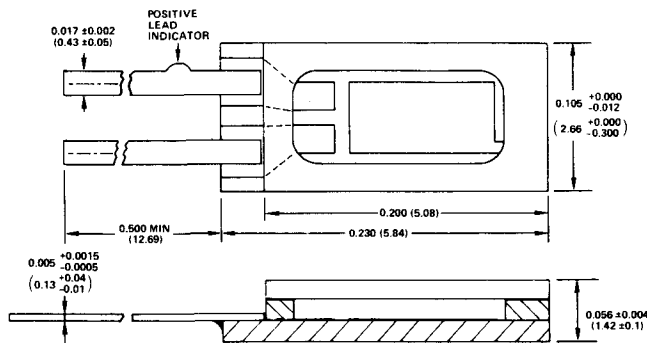
## OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).

### TO-52 PACKAGE: DESIGNATION "H"

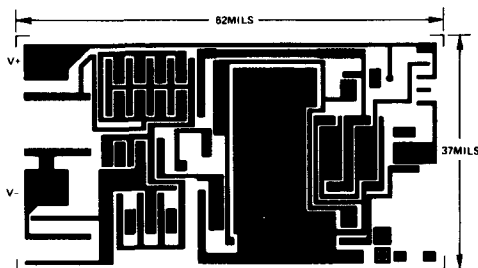


The 590H has 60 $\mu$  inches of gold plating on its Kovar leads and Kovar header. A resistance welder is used to seal the nickel cap to the header. The AD590 chip is eutectically mounted to the header and ultrasonically bonded to with 1 MIL aluminum wire. Kovar composition: 53% iron nominal; 29%  $\pm$ 1% nickel; 17%  $\pm$ 1% cobalt; 0.65% manganese max; 0.20% silicon max; 0.10% aluminum max; 0.10% magnesium max; 0.10% zirconium max; 0.10% titanium max; 0.06% carbon max.



### FLAT-PACK PACKAGE: DESIGNATION "F"

The 590F is a ceramic package with gold plating on its Kovar leads, Kovar lid, and chip cavity. Solder of 80/20 Au/Sn composition is used for the 1.5 mil thick solder ring under the lid. The chip cavity has a nickel underlay between the metalization and the gold plating. The AD590 chip is eutectically mounted in the chip cavity at 400°C and ultrasonically bonded to with 1 mil aluminum wire. Note that the chip is in direct contact with the ceramic base, not the metal lid.



Metalization Diagram

## CIRCUIT DESCRIPTION<sup>1</sup>

The AD590 uses a fundamental property of the silicon transistors from which it is made to realize its temperature proportional characteristic: if two identical transistors are operated at a constant ratio of collector current densities,  $r$ , then the difference in their base-emitter voltages will be  $(kT/q)(\ln r)$ . Since both  $k$ , Boltzman's constant and  $q$ , the charge of an electron, are constant, the resulting voltage is directly proportional to absolute temperature (PTAT).

In the AD590, this PTAT voltage is converted to a PTAT current by low temperature coefficient thin film resistors. The total current of the device is then forced to be a multiple of this PTAT current. Referring to Figure 1, the schematic diagram of the AD590, Q8 and Q11 are the transistors that produce the PTAT voltage. R5 and R6 convert the voltage to current. Q10, whose collector current tracks the collector currents in Q9 and Q11, supplies all the bias and substrate leakage current for the rest of the circuit, forcing the total current to be PTAT. R5 and R6 are laser trimmed on the wafer to calibrate the device at +25°C.

Figure 2 shows the typical V-I characteristic of the circuit at +25°C and the temperature extremes.

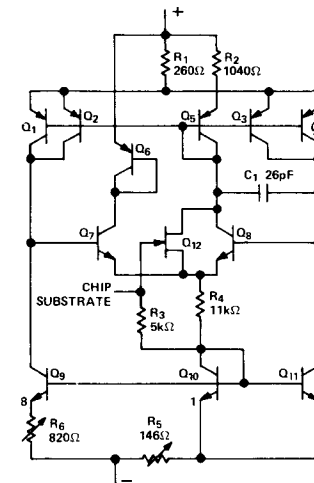


Figure 1. Schematic Diagram

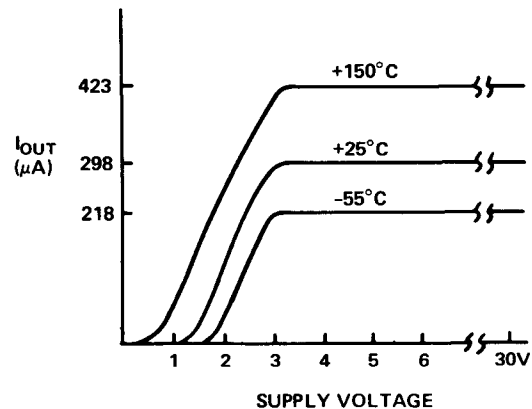


Figure 2. V-I Plot

<sup>1</sup> For a more detailed circuit description see M.P. Timko, "A Two-Terminal IC Temperature Transducer," IEEE J. Solid State Circuits, Vol. SC-11, p. 784-788, Dec. 1976.

## EXPLANATION OF TEMPERATURE SENSOR SPECIFICATIONS

The way in which the AD590 is specified makes it easy to apply in a wide variety of different applications. It is important to understand the meaning of the various specifications and the effects of supply voltage and thermal environment on accuracy.

The AD590 is basically a PTAT (proportional to absolute temperature)<sup>1</sup> current regulator. That is, the output current is equal to a scale factor times the temperature of the sensor in degrees Kelvin. This scale factor is trimmed to  $1\mu\text{A}/^\circ\text{K}$  at the factory, by adjusting the indicated temperature (i.e. the output current) to agree with the actual temperature. This is done with 5V across the device at a temperature within a few degrees of  $25^\circ\text{C}$  ( $298.2^\circ\text{K}$ ). The device is then packaged and tested for accuracy over temperature.

### CALIBRATION ERROR

At final factory test the difference between the indicated temperature and the actual temperature is called the calibration error. Since this is a scale factor error, its contribution to the total error of the device is PTAT. For example, the effect of the  $1^\circ\text{C}$  specified maximum error of the AD590L varies from  $0.73^\circ\text{C}$  at  $-55^\circ\text{C}$  to  $1.42^\circ\text{C}$  at  $150^\circ\text{C}$ . Figure 3 shows how an exaggerated calibration error would vary from the ideal over temperature.

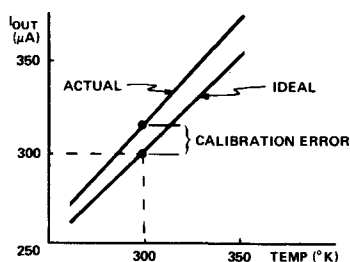


Figure 3. Calibration Error vs. Temperature

The calibration error is a primary contributor to maximum total error in all AD590 grades. However, since it is a scale factor error, it is particularly easy to trim. Figure 4 shows the most elementary way of accomplishing this. To trim this circuit the temperature of the AD590 is measured by a reference temperature sensor and R is trimmed so that  $V_T = 1\text{mV}/^\circ\text{K}$  at that temperature. Note that when this error is trimmed out at one temperature, its effect is zero over the entire temperature range. In most applications there is a current to voltage conversion resistor (or, as with a current input ADC, a reference) that can be trimmed for scale factor adjustment.

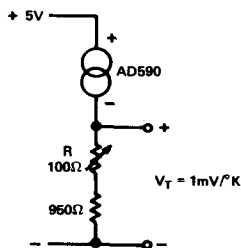


Figure 4. One Temperature Trim

### ERROR VERSUS TEMPERATURE: WITH CALIBRATION ERROR TRIMMED OUT

Each AD590 is also tested for error over the temperature range with the calibration error trimmed out. This specification could also be called the "variance from PTAT" since it is the maximum difference between the actual current over temperature and a PTAT multiplication of the actual current at  $25^\circ\text{C}$ . This error consists of a slope error and some curvature, mostly at the temperature extremes. Figure 5 shows a typical AD590K temperature curve before and after calibration error trimming.

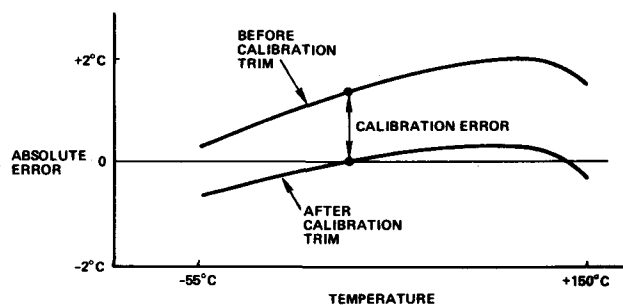


Figure 5. Effect of Scale Factor Trim on Accuracy

### ERROR VERSUS TEMPERATURE: NO USER TRIMS

Using the AD590 by simply measuring the current, the total error is the "variance from PTAT" described above plus the effect of the calibration error over temperature. For example the AD590L maximum total error varies from  $2.33^\circ\text{C}$  at  $-55^\circ\text{C}$  to  $3.02^\circ\text{C}$  at  $150^\circ\text{C}$ . For simplicity, only the larger figure is shown on the specification page.

### NONLINEARITY

Nonlinearity as it applies to the AD590 is the maximum deviation of current over temperature from a best-fit straight line. The nonlinearity of the AD590 over the  $-55^\circ\text{C}$  to  $+150^\circ\text{C}$  range is superior to all conventional electrical temperature sensors such as thermocouples, RTD's and thermistors. Figure 6 shows the nonlinearity of the typical AD590K from Figure 5.

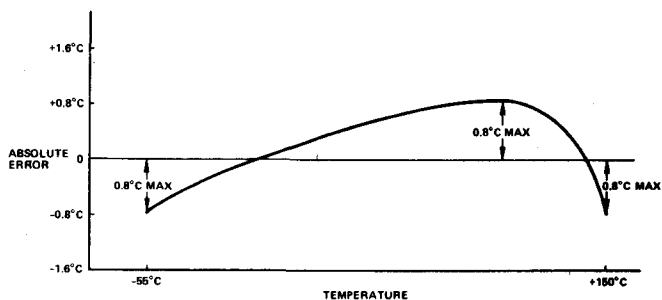


Figure 6. Nonlinearity

Figure 7A shows a circuit in which the nonlinearity is the major contributor to error over temperature. The circuit is trimmed by adjusting  $R_1$  for a 0V output with the AD590 at  $0^\circ\text{C}$ .  $R_2$  is then adjusted for 10V out with the sensor at  $100^\circ\text{C}$ . Other pairs of temperatures may be used with this procedure as long as they are measured accurately by a reference sensor. Note that for +15V output ( $150^\circ\text{C}$ ) the  $V+$  of the op amp must be greater than 17V. Also note that  $V-$  should be at least  $-4\text{V}$ : if  $V-$  is ground there is no voltage applied across the device.

<sup>1</sup>  $T(^{\circ}\text{C}) = T(^{\circ}\text{K}) - 273.2$ ; Zero on the Kelvin scale is "absolute zero"; there is no lower temperature.

# Understanding the AD590 Specifications

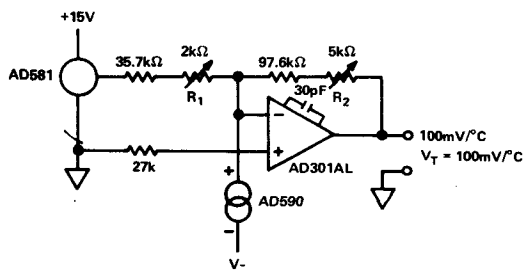


Figure 7A. Two Temperature Trim

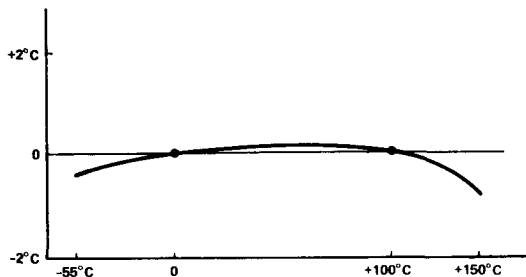


Figure 7B. Typical Two-Trim Accuracy

## VOLTAGE AND THERMAL ENVIRONMENT EFFECTS

The power supply rejection specifications given on page 86S show the maximum expected change in output current versus input voltage changes. The insensitivity of the output to input voltage allows the use of unregulated supplies. It also means that hundreds of ohms of resistance (such as a CMOS multiplexer) can be tolerated in series with the device.

It is important to note that using a supply voltage other than 5V does not change the PTAT nature of the AD590. In other words, this change is equivalent to a calibration error and can be removed by the scale factor trim (see page 88S).

The AD590 specifications are guaranteed for use in a low thermal resistance environment with 5V across the sensor. Large changes in the thermal resistance of the sensor's environment will change the amount of self-heating and result in changes in the output which are predictable but not necessarily desirable.

The thermal environment in which the AD590 is used determines two important characteristics: the effect of self heating and the response of the sensor with time.

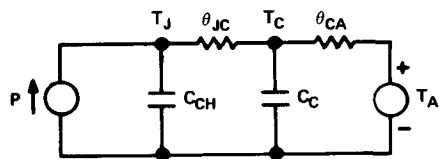


Figure 8. Thermal Circuit Model

Figure 8 is a model of the AD590 which demonstrates these characteristics. As an example, for the TO-52 package,  $\theta_{JC}$  is the thermal resistance between the chip and the case, about

$26^\circ\text{C}/\text{watt}$ .  $\theta_{CA}$  is the thermal resistance between the case and its surroundings and is determined by the characteristics of the thermal connection. Power source  $P$  represents the power dissipated on the chip. The rise of the junction temperature,  $T_J$ , above the ambient temperature  $T_A$  is:

$$T_J - T_A = P (\theta_{JC} + \theta_{CA}). \quad \text{Eq. 1}$$

Table 1 gives the sum of  $\theta_{JC}$  and  $\theta_{CA}$  for several common thermal media for both the "H" and "F" packages. The heat-sink used was a common clip-on. Using Equation 1, the temperature rise of an AD590 "H" package in a stirred bath at  $+25^\circ\text{C}$ , when driven with a 5V supply, will be  $0.06^\circ\text{C}$ . However, for the same conditions in still air the temperature rise is  $0.72^\circ\text{C}$ . For a given supply voltage, the temperature rise varies with the current and is PTAT. Therefore, if an application circuit is trimmed with the sensor in the same thermal environment in which it will be used, the scale factor trim compensates for this effect over the entire temperature range.

| MEDIUM                   | $\theta_{JC} + \theta_{CA} (^\circ\text{C}/\text{watt})$ |     | $\tau$ (sec)(Note 3) |      |
|--------------------------|--|-----|----------------------|------|
|                          | H  | F   | H                    | F    |
| Aluminum Block           | 30   | 10  | 0.6                  | 0.1  |
| Stirred Oil <sup>1</sup> | 42   | 60  | 1.4                  | 0.6  |
| Moving Air <sup>2</sup>  |  |     |                      |      |
| With Heat Sink           | 45   | —   | 5.0                  | —    |
| Without Heat Sink        | 115  | 190 | 13.5                 | 10.0 |
| Still Air                |  |     |                      |      |
| With Heat Sink           | 191  | —   | 108                  | —    |
| Without Heat Sink        | 480  | 650 | 60                   | 30   |

<sup>1</sup> Note:  $\tau$  is dependent upon velocity of oil; average of several velocities listed above.

<sup>2</sup> Air velocity  $\approx 9\text{ft}/\text{sec}$ .

<sup>3</sup> The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.

Table 1. Thermal Resistances

The time response of the AD590 to a step change in temperature is determined by the thermal resistances and the thermal capacities of the chip,  $C_{CH}$ , and the case,  $C_C$ .  $C_{CH}$  is about  $0.04 \text{ watt-sec}/^\circ\text{C}$  for the AD590.  $C_C$  varies with the measured medium since it includes anything that is in direct thermal contact with the case. In most cases, the single time constant exponential curve of Figure 9 is sufficient to describe the time response,  $T(t)$ . Table 1 shows the effective time constant,  $\tau$ , for several media.

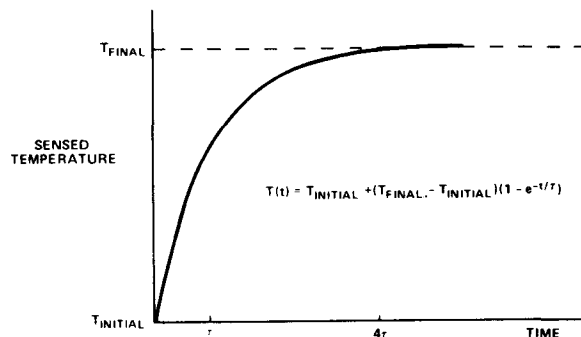


Figure 9. Time Response Curve

## GENERAL APPLICATIONS

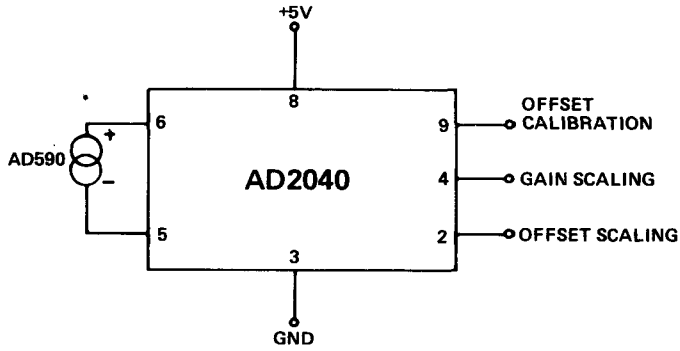


Figure 10. Variable Scale Display

Figure 10 demonstrates the use of a low-cost Digital Panel Meter for the display of temperature on either the Kelvin, Celsius or Fahrenheit scales. For Kelvin temperature Pins 9, 4 and 2 are grounded; and for Fahrenheit temperature Pins 4 and 2 are left open.

The above configuration yields a 3 digit display with  $1^{\circ}\text{C}$  or  $1^{\circ}\text{F}$  resolution, in addition to an absolute accuracy of  $\pm 2.0^{\circ}\text{C}$  over the  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range if a one-temperature calibration is performed on an AD590K, L, or M.

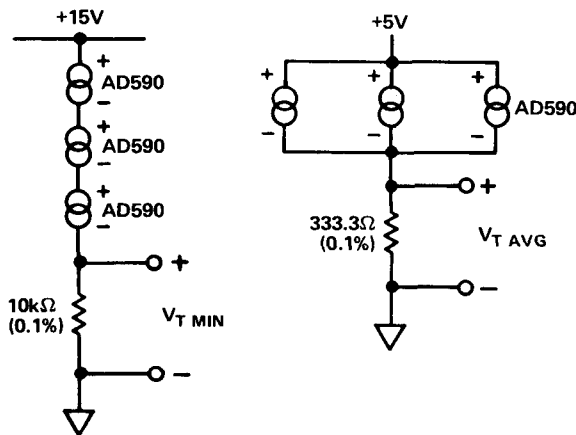


Figure 11. Series & Parallel Connection

Connecting several AD590 units in series as shown in Figure 11 allows the minimum of all the sensed temperatures to be indicated. In contrast, using the sensors in parallel yields the average of the sensed temperatures.

The circuit of Figure 12 demonstrates one method by which differential temperature measurements can be made.  $R_1$  and  $R_2$  can be used to trim the output of the op amp to indicate

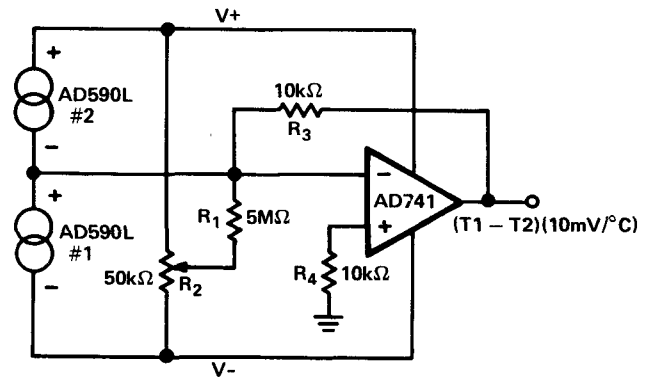


Figure 12. Differential Measurements

a desired temperature difference. For example, the inherent offset between the two devices can be trimmed in. If  $V+$  and  $V-$  are radically different, then the difference in internal dissipation will cause a differential internal temperature rise. This effect can be used to measure the ambient thermal resistance seen by the sensors in applications such as fluid level detectors or anemometry.

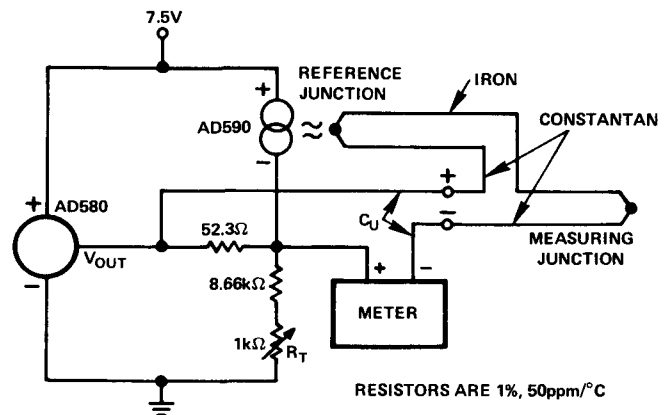


Figure 13. Cold Junction Compensation Circuit for Type J Thermocouple

Figure 13 is an example of a cold junction compensation circuit for a Type J Thermocouple using the AD590 to monitor the reference junction temperature. This circuit replaces an ice-bath as the thermocouple reference for ambient temperatures between  $+15^{\circ}\text{C}$  and  $+35^{\circ}\text{C}$ . The circuit is calibrated by adjusting  $R_T$  for a proper meter reading with the measuring junction at a known reference temperature and the circuit near  $+25^{\circ}\text{C}$ . Using components with the T.C.'s as specified in Figure 13, compensation accuracy will be within  $\pm 0.5^{\circ}\text{C}$  for circuit temperatures between  $+15^{\circ}\text{C}$  and  $+35^{\circ}\text{C}$ . Other thermocouple types can be accommodated with different resistor values. Note that the T.C.'s of the voltage reference and the resistors are the primary contributors to error.

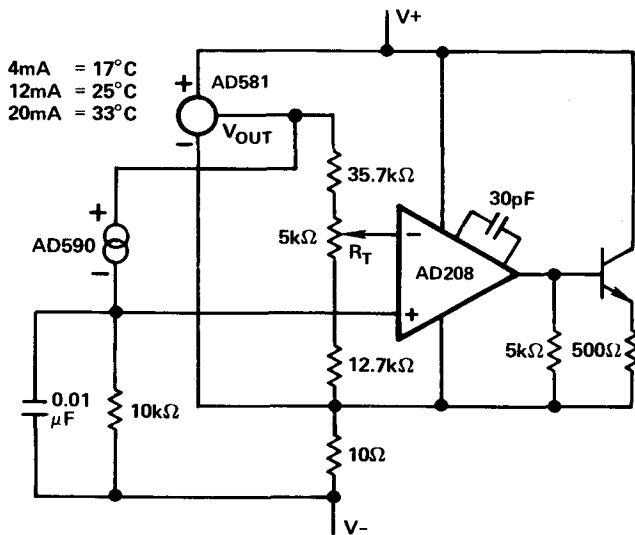


Figure 14. 4 to 20mA Current Transmitter

Figure 14 is an example of a current transmitter designed to be used with 40V, 1kΩ systems; it uses its full current range of 4mA to 20mA for a narrow span of measured temperatures. In this example the 1μA/°K output of the AD590 is amplified to 1mA/°C and offset so that 4mA is equivalent to 17°C and 20mA is equivalent to 33°C.  $R_T$  is trimmed for proper reading at an intermediate reference temperature. With a suitable choice of resistors, any temperature range within the operating limits of the AD590 may be chosen.

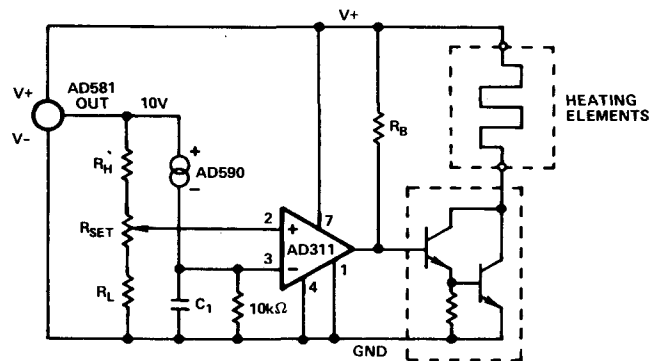


Figure 15. Simple Temperature Control Circuit

Figure 15 is an example of a variable temperature control circuit (thermostat) using the AD590.  $R_H$  and  $R_L$  are selected to set the high and low limits for  $R_{SET}$ .  $R_{SET}$  could be a simple pot, a calibrated multi-turn pot or a switched resistive divider. Powering the AD590 from the 10V reference isolates the AD590 from supply variations while maintaining a reasonable voltage (~7V) across it. Capacitor  $C_1$  is often needed to filter extraneous noise from remote sensors.  $R_B$  is determined by the  $\beta$  of the power transistor and the current requirements of the load.

Figure 16 shows how the AD590 can be configured with an 8 bit DAC to produce a digitally controlled setpoint. This

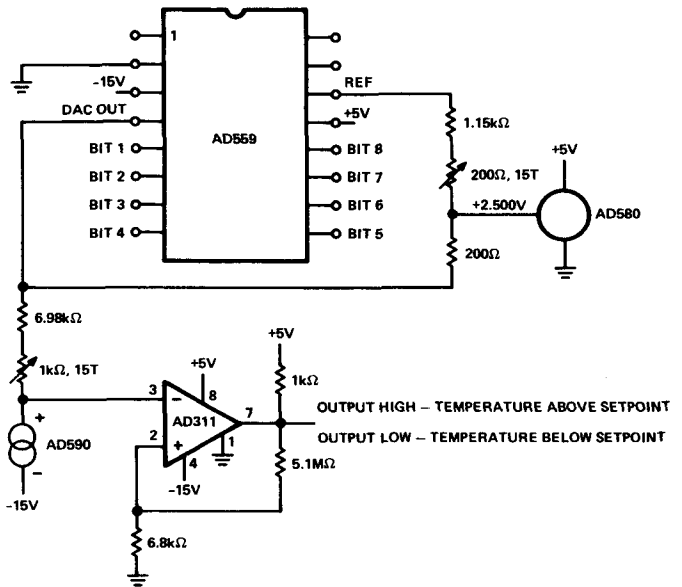


Figure 16. DAC Setpoint

particular circuit operates from 0 (all inputs high) to +51°C (all inputs low) in 0.2°C steps. The comparator is shown with 1°C hysteresis which is usually necessary to guard-band for extraneous noise; omitting the 5.1MΩ resistor results in no hysteresis.

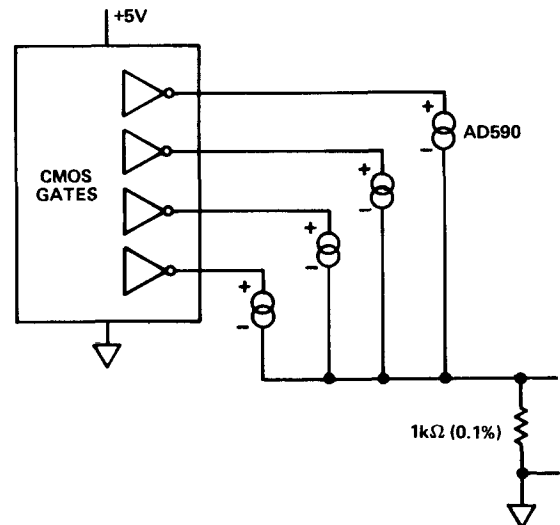


Figure 17. AD590 Driven from CMOS Logic

The voltage compliance and the reverse blocking characteristic of the AD590 allows it to be powered directly from +5V CMOS logic. This permits easy multiplexing, switching or pulsing for minimum internal heat dissipation. In Figure 17 any AD590 connected to a logic high will pass a signal current through the current measuring circuitry while those connected to a logic zero will pass insignificant current. The outputs used to drive the AD590's may be employed for other purposes, but the additional capacitance due to the AD590 should be taken into account.



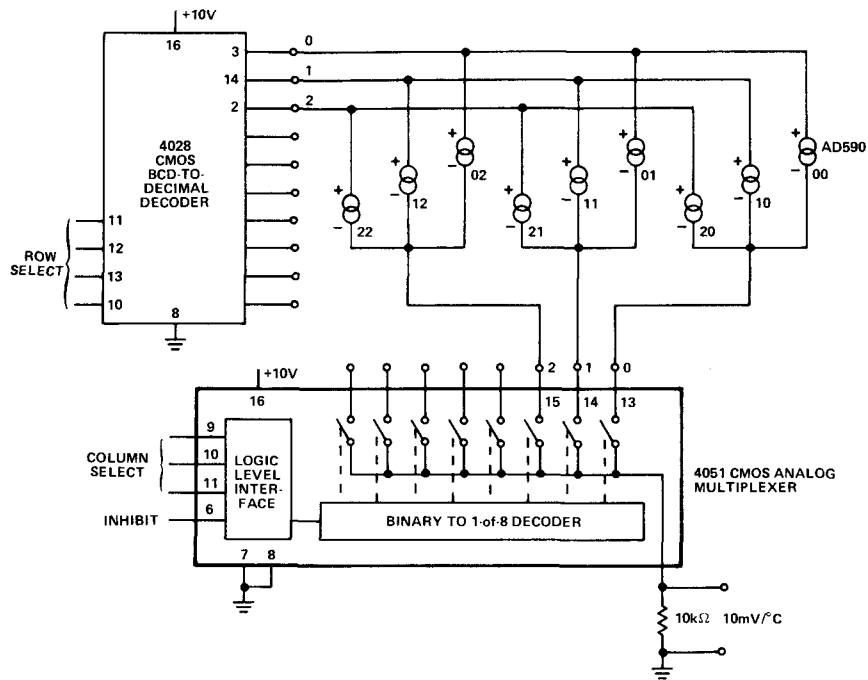


Figure 18. Matrix Multiplexer

CMOS Analog Multiplexers can also be used to switch AD590 current. Due to the AD590's current mode, the resistance of such switches is unimportant as long as 4V is maintained across the transducer. Figure 18 shows a circuit which combines the principal demonstrated in Figure 17 with an 8 channel CMOS Multiplexer. The resulting circuit can select one of eighty sensors over only 18 wires with a 7 bit binary word. The inhibit input on the multiplexer turns all sensors off for minimum dissipation while idling.

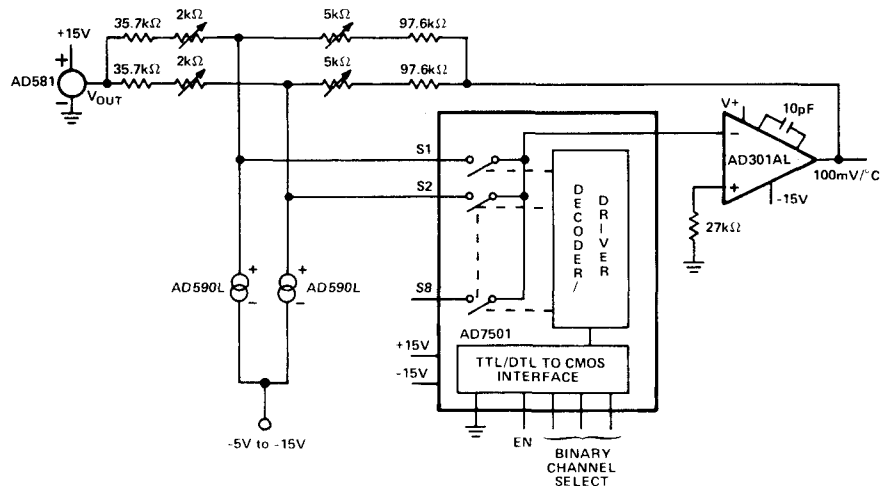


Figure 19. 8-Channel Multiplexer

Figure 19 demonstrates a method of multiplexing the AD590 in the two-trim mode (Figure 7). Additional AD590's and their associated resistors can be added to multiplex up to 8 channels of  $\pm 0.5^\circ\text{C}$  absolute accuracy over the temperature range of  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ . The high temperature restriction of  $+125^\circ\text{C}$  is due to the output range of the op amps; output to  $+150^\circ\text{C}$  can be achieved by using a  $+20\text{V}$  supply for the op amp.

### FEATURES

- Complete, No External Components Needed
  - Small Size: 1.1" x 1.1" x 0.4" Module
  - Input: 0 to +10V; Output: 4 to 20mA
  - Low Drift: 0.005%/°C max; Nonlinearity: 0.005% max (2B20B)
  - Wide Temperature Range: -25°C to +85°C
  - Single Supply: +10V to +32V
  - Meets ISA Std 50.1 for Type 3, Class L and U, Nonisolated Current Loop Transmitters
  - Economical
- ### APPLICATIONS
- Industrial Instrumentation and Control Systems
  - D/A Converter – Current Loop Interface
  - Analog Transmitters and Controllers
  - Remote Data Acquisition Systems

### GENERAL DESCRIPTION

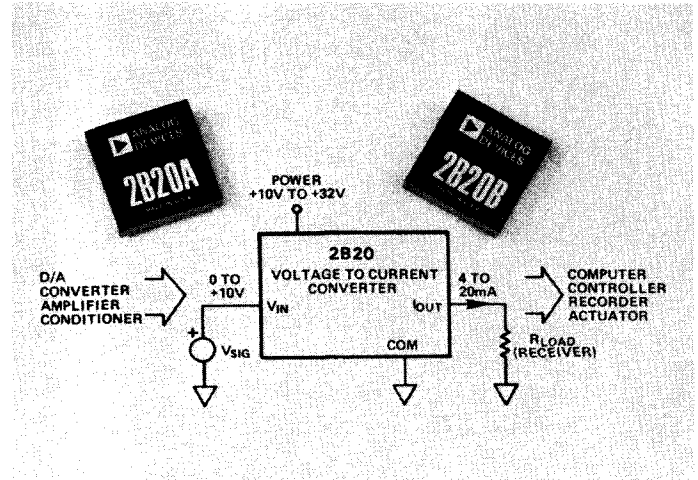
Model 2B20 is a complete, modular voltage-to-current converter providing the user with a convenient way to produce a current output signal which is proportional to the voltage input. The nominal input voltage range is 0 to +10V. The output current range is 4 to 20mA into a grounded load.

Featuring low drift (0.005%/°C max, 2B20B) over the -25°C to +85°C temperature range and single supply operation (+10V to +32V), model 2B20 is available in two accuracy grades. The 2B20B offers precision performance with nonlinearity error of 0.005% (max) and guaranteed low offset error of ±0.1% max and span error of ±0.2% max, without external trims. The 2B20A is an economical solution for applications with lesser accuracy requirements, featuring nonlinearity error of 0.025% (max), offset error of ±0.4% (max), span error of ±0.6% (max), and span stability of 0.01%/°C max.

The 2B20 is contained in a small (1.1" x 1.1" x 0.4"), rugged, epoxy encapsulated package. For maximum versatility, two signal input ( $V_{IN1}$  and  $V_{IN2}$ ) and two reference input ( $REF_{IN1}$  and  $REF_{IN2}$ ) terminals are provided. Utilizing terminals  $V_{IN1}$  and  $REF_{IN1}$  eliminates the need for any external components, since offset and span are internally calibrated. If higher accuracy (up to ±0.01%) is required, inputs  $V_{IN2}$  and  $REF_{IN2}$  with series trim potentiometers may be utilized.

### APPLICATIONS

Model 2B20 has been designed for applications in process control and monitoring systems to transmit information between subsystems or separated system elements. The 2B20 can serve as a transmission link between such elements of process con-



trol system as transmitters, indicators, controllers, recorders, computers, actuators and signal conditioners.

In a typical application, model 2B20 may act as an interface between the D/A converter output of a microcomputer based system and a process control device such as a variable position valve. Another typical application of the 2B20 may be as a current output stage of a proportional controller to interface devices such as current-to-position converters and current-to-pneumatic transducers.

### DESIGN FEATURES AND USER BENEFITS

**Process Signal Compatibility:** To provide output signal compatibility, the 2B20 meets the requirements of the Instrument Society of America Standard S50.1, "Compatibility of Analog Signals for Electronic Industrial Process Instruments" for Type 3, Class L and U, nonisolated current loop transmitters.

**External Reference Use:** For increased flexibility, when ratio-metric operation is desired, the 2B20 offers a capability of connecting an external reference (i.e., from multiplying D/A converter) to the  $REF_{IN2}$  terminal.

**Wide Power Supply Range:** A wide power supply range (+10V to +32V dc) allows for operation with either a +12V battery, a +15V powered data acquisition system, or a +24V powered process control instrumentation.

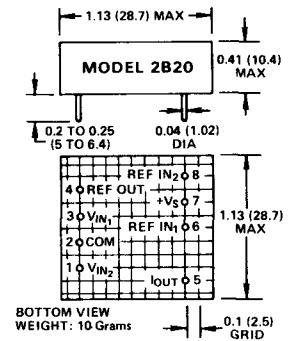
# SPECIFICATIONS

(typical @ +25°C and  $V_S = +15V$ , unless otherwise noted)

| Model   | 2B20A                      | 2B20B                       |
|---|----------------------------|-----------------------------|
| <b>INPUT SPECIFICATIONS</b>                   |                            |                             |
| Voltage Signal Range                          | 0 to +10V                  | *                           |
| Input Impedance                               | 10k $\Omega$               | *                           |
| <b>OUTPUT SPECIFICATIONS</b>                  |                            |                             |
| Current Output Range <sup>1</sup>             | 4 to 20mA                  | *                           |
| Load Resistance Range <sup>2</sup>            |                            |                             |
| $V_S = +12V$                                  | 0 to 350 $\Omega$ max      | *                           |
| $V_S = +15V$                                  | 0 to 500 $\Omega$ max      | *                           |
| $V_S = +24V$                                  | 0 to 950 $\Omega$ max      | *                           |
| <b>NONLINEARITY (% of Span)</b>               |                            |                             |
|   | $\pm 0.025\%$ max          | $\pm 0.005\%$ max           |
| <b>ACCURACY<sup>3</sup></b>                   |                            |                             |
| Warm-Up Time to Rated Specs                   | 1 minute                   | *                           |
| Total Output Error @ +25°C <sup>3,4</sup>     |                            |                             |
| Offset ( $V_{IN} = 0$ volts)                  | $\pm 0.4\%$ max            | $\pm 0.1\%$ max             |
| Span ( $V_{IN} = +10$ volts)                  | $\pm 0.6\%$ max            | $\pm 0.2\%$ max             |
| vs. Temperature (-25°C to +85°C)              |                            |                             |
| Offset ( $V_{IN} = 0$ volts)                  | $\pm 0.01\%/^{\circ}C$ max | $\pm 0.005\%/^{\circ}C$ max |
| Span ( $V_{IN} = +10$ volts)                  | $\pm 0.01\%/^{\circ}C$ max | $\pm 0.005\%/^{\circ}C$ max |
| <b>DYNAMIC RESPONSE</b>                       |                            |                             |
| Settling Time - to 0.1% of F.S.               |                            |                             |
| for 10V Step                                  | 25 $\mu s$                 | *                           |
| Slew Rate                                     | 2.5mA/ $\mu s$             | *                           |
| <b>REFERENCE INPUT<sup>5</sup></b>            |                            |                             |
| Voltage                                       | +2.5V dc                   | *                           |
| Input Impedance                               | 10k $\Omega$               | *                           |
| <b>POWER SUPPLY</b>                           |                            |                             |
| Voltage, Rated Performance                    | +15V dc                    | *                           |
| Voltage, Operating                            | +10V to +32V dc max        | *                           |
| Supply Change Effect (% of Span) <sup>6</sup> |                            |                             |
| on Offset                                     | $\pm 0.005\%/V$            | *                           |
| on Span                                       | $\pm 0.005\%/V$            | *                           |
| Supply Current                                | 6mA + $I_{LOAD}$           | *                           |
| <b>TEMPERATURE RANGE</b>                      |                            |                             |
| Rated Performance                             | -25°C to +85°C             | *                           |
| Storage                                       | -55°C to +125°C            | *                           |
| <b>CASE SIZE</b>                              |                            |                             |
|   | 1.125" X 1.125"<br>X 0.4"  | *                           |

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET: AC1016

## LOAD RESISTANCE RANGE

The load resistance is the sum of the resistances of all connected receivers and the connection lines. The 2B20 operating load resistance is power supply dependent and will decrease by 50 ohms for each 1 volt reduction in the power supply. Similarly, it will increase by 50 ohms per volt increase in the power supply, but must not exceed the safe voltage capability of the unit.

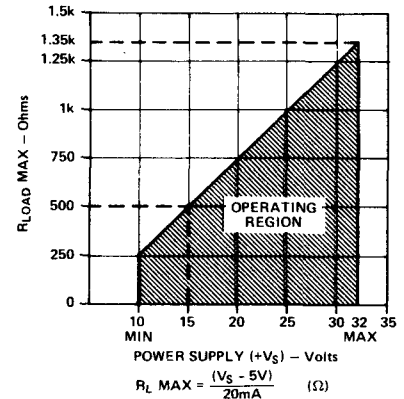


Figure 1. Maximum Load Resistance vs. Power Supply

\*Specifications same as 2B20A.

<sup>1</sup> Current output sourced into a grounded load over a supply voltage range of +10V to +32V.

<sup>2</sup> See Figure 1 for the maximum load resistance value over the power supply range.

<sup>3</sup> Accuracy is guaranteed with no external trim adjustments when REF<sub>IN</sub> is connected to REF<sub>OUT</sub>.

<sup>4</sup> All accuracy is specified as % of output span where output span is 16mA ( $\pm 0.1\% = \pm 0.016mA$  output error).

<sup>5</sup> Reference input is normally connected to the reference output (+2.5V dc).

<sup>6</sup> Optional trim pots may be used for calibration at each supply voltage.

Specifications subject to change without notice.

## PRINCIPLE OF OPERATION

The design of the 2B20 is comprised of high performance op amps, precision resistors and a high stability voltage reference to develop biasing and output drive capability. The 2B20 is designed to operate from a single positive power supply over a wide range of +10V to +32V dc and accepts a single ended, 0 to +10V voltage input. The internal reference has nominal output voltage of +2.5V (REF<sub>OUT</sub>) and is used to develop 4mA output current for a zero volts input when REF<sub>IN</sub> is connected to REF<sub>OUT</sub>.

The output stage of the 2B20 utilizes a sensing resistor in the feedback loop, so the output current is linearly related to the voltage input and independent of the load resistance. There is no minimum resistance for the loads driven by the 2B20; it can drive even a short circuit with no damage to the unit. The maximum resistance of the load as seen by the unit (resistance of the load plus the resistance of the connecting wire) is limited. The maximum external loop resistance, R<sub>L</sub>, is given by:

$$R_L (\Omega) \max = \left( \frac{+V_S - 5V}{20\text{mA}} \right)$$

Figure 1 (page 2) shows the operating region of the 2B20. The load must be returned to power supply common. The voltage appearing between I<sub>OUT</sub> (pin 5) and COM (pin 2) should not exceed V<sub>max</sub> = +V<sub>S</sub> - 5V. Exceeding this value (up to +32V dc) will not damage the unit, but it will result in a loss of linearity.

The basic connections of the 2B20 are shown in Figure 2.

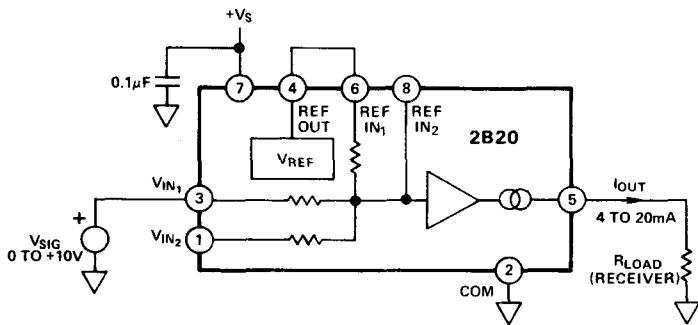


Figure 2. Basic Connections Diagram

## OPTIONAL CALIBRATION AND TRIM PROCEDURE

Model 2B20's factory trimmed offset error is ±0.1% max and span error is ±0.2% max (2B20B). In most applications, further trimming will not be required. If it is necessary to obtain calibrated accuracy of up to ±0.01%, or, if a high signal source resistance (with respect to 10kΩ) introduces calibration error, inputs VIN<sub>2</sub> and REF<sub>IN2</sub> and optional trim pots should be used with VIN<sub>1</sub> and REF<sub>IN1</sub> open. To perform external trims, connect 500Ω potentiometers in series with VIN<sub>2</sub> (span trim) and REF<sub>IN2</sub> (offset trim) as shown in Figure 3. Adjust span pot, monitoring voltage drop across R<sub>LOAD</sub>, to obtain an output voltage of 5.000V (I<sub>OUT</sub> = 20mA) for a +10V input. Next, with 0 volts input, adjust offset pot to obtain 1.000V output (I<sub>OUT</sub> = 4mA). Check both offset and span and retrim if necessary after each adjustment.

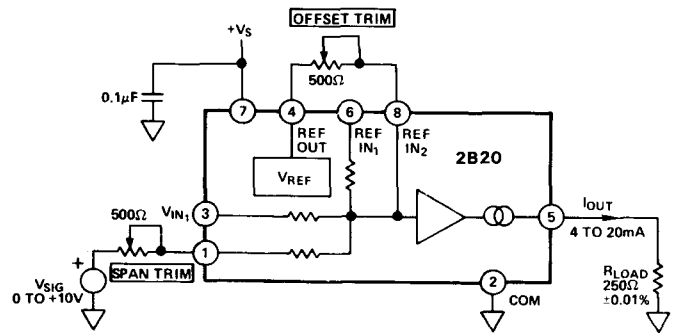


Figure 3. Model 2B20 Connections Using Optional Offset and Span Trims

## CONNECTING THE 2B20 FOR 0 TO 10mA OUTPUT

The 2B20 may be utilized in applications requiring 0 to 10mA current output for a 0 to 10V input voltage range. To obtain 0mA output for 0V input, REF<sub>IN1</sub> (pin 6) and REF<sub>IN2</sub> (pin 8) terminals should be left open. A typical output current error for a zero volts input (without trimming) is 0.1mA. The 2B20 span calibration may be adjusted by a 1kΩ potentiometer in series with the VIN<sub>2</sub> input. Basic connections of the 2B20 used to obtain a 0 to 10mA output are shown in Figure 4.

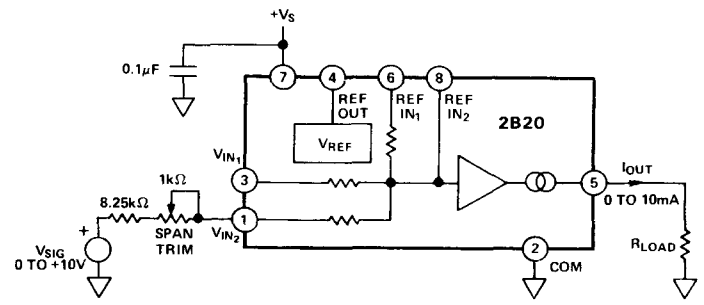


Figure 4. Model 2B20 Connected for 0 to 10mA Output Range

## OUTPUT PROTECTION

In many industrial applications, it may be necessary to protect the 4 to 20mA output from accidental shorts to ac line voltages. The circuit shown in Figure 5 can be used for this purpose. The maximum permissible load resistance will be lowered by a fuse resistance value when protection circuitry is utilized.

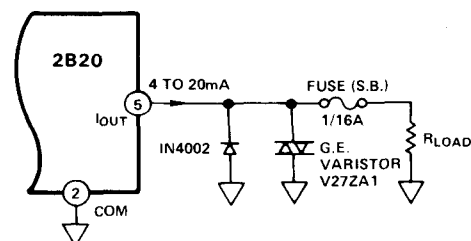


Figure 5. Output Protection Circuitry Connections

## APPLICATIONS

**Interfacing Voltage Output D/A Converters:** The 2B20 is well suited in applications requiring 4 to 20mA output from D/A converters. The voltage necessary to power the current loop can be derived from the same +15V supply that is used to power the converter. The D/A converter, such as the 12-bit AD DAC80, should be connected for operation on the unipolar 0 to +10V output range. This is shown in Figure 6. After the load resistor connection has been made, the current loop can be calibrated using the offset and span adjustment potentiometers associated with the 2B20 (or the AD DAC80). First, a digital input code of all zeros is loaded into the D/A, and the offset adjustment potentiometer is adjusted for a current output of exactly 4mA. Then, a digital code of all 1's is loaded into the D/A, and the span adjustment potentiometer is adjusted for a voltage across the load that corresponds to a current of 20mA  $-1\text{LSB} = 19.9961\text{mA}$ .

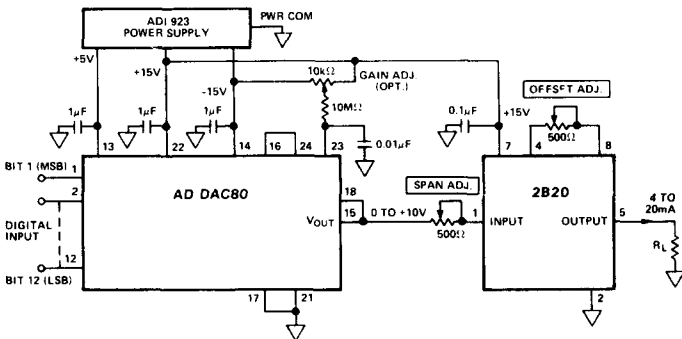


Figure 6. AD DAC80 - 4 to 20mA Current Loop Interface

**Interfacing Current Output D/A Converters:** To interface current output D/A converters, such as the AD562, a circuit configuration illustrated in Figure 7 should be used. Since the AD562 is designed to operate with an external +10V reference, the same external reference may be utilized by the 2B20 for ratiometric operation. The output of the AD562 is used to drive the summing junction of an operational amplifier to produce an output voltage. Using the internal feedback resistor of the AD562 provides a 0 to +10V output voltage range suitable to drive the 2B20.

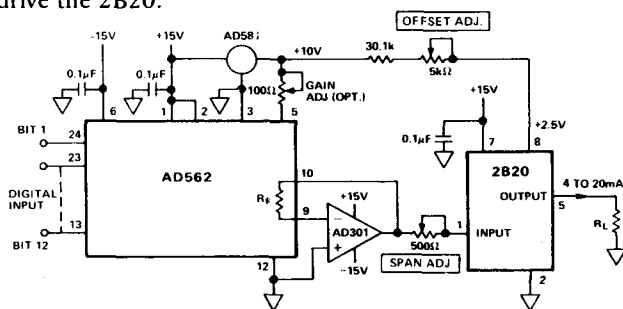


Figure 7. 12-Bit - 4 to 20mA Current Loop Interface

**Microcomputer - Current Loop Interface:** Figure 8 shows a typical application of the 2B20 in a multichannel microcomputer analog output system. When a microcomputer is to control a final control element, such as a valve positioner, servo-mechanism or motor, an analog output board with 4 to 20mA outputs is often necessary. The output boards typically have from one to eight channels, each with its own D/A converter. The 2B20, in a compact package, allows for an easy installation without any additional components and offers a 12 bit system compatible performance.

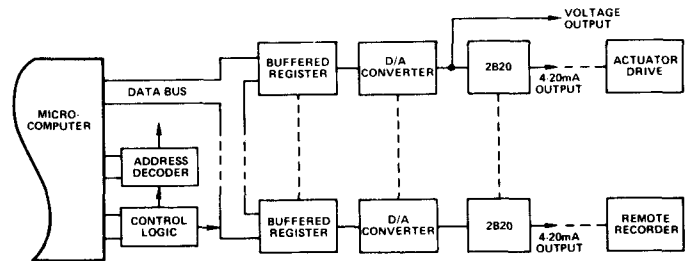


Figure 8. Microcomputer Analog Output Subsystem

**Pressure Control System:** In Figure 9, model 2B20 is used in a proportional pressure control system. The 3-15psi working pressure of a system is monitored with a pressure transducer interfaced by the model 2B31 signal conditioner. The high level voltage output of the 2B31 is converted to a 4 to 20mA to provide signal to the limit alarm and proportional control circuitry. A current-to-position converter controlling a motorized valve completes the pressure-control loop.

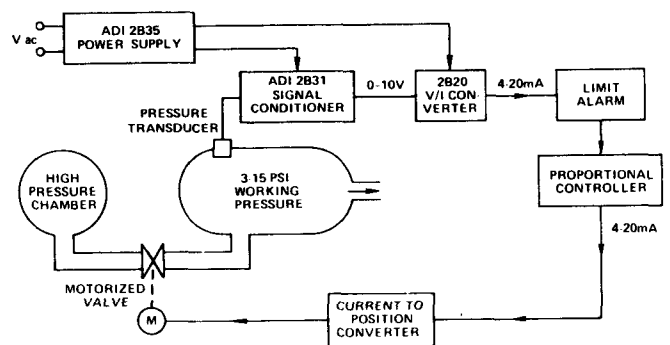


Figure 9. Proportional Pressure Control System

**Isolated 4 to 20mA Output:** For applications requiring up to  $\pm 1500\text{V}$  dc input to output isolation, consider using Analog Devices' model 2B22 isolated voltage-to-current converter.

### FEATURES

- Wide Input Range: 0 to +1V to 0 to +10V
- Standard Output Range: 4 to 20mA
- High CMV Input/Output Isolation: 1500V dc Continuous
- Low Nonlinearity: 0.05% max, 2B22L
- Low Span Drift: 0.005%/°C max, 2B22L
- Single Supply: +14V to +32V
- Meets IEEE Std 472: Transient Protection (SWC)
- Meets ISA Std 50.1: Isolated Current Loop Transmitters

### APPLICATIONS

- Industrial Instrumentation and Process Control
- Ground Loop Elimination
- High Voltage Transient Protection
- D/A Converter — Current Loop Interface
- Analog Transmitters and Controllers
- Remote Data Acquisition Systems

### GENERAL DESCRIPTION

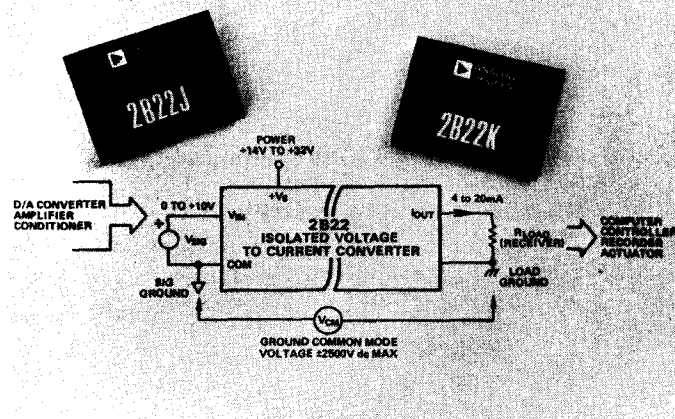
Model 2B22 is a high performance, compact voltage-to-current converter offering 1500V dc input to output isolation in interfacing standard process signals. The input stage of the model 2B22 is single resistor programmable to accept voltage ranges from 0 to +1V to 0 to +10V. The isolated output current range is 4 to 20mA, and the 2B22 can be operated with 0 to 1000Ω grounded or floating loads.

Using modulation techniques with transformer isolation for reliable performance, the 2B22 is available in three accuracy selections offering guaranteed nonlinearity error (2B22L: ±0.05% max, 2B22K: ±0.1% max, and 2B22J: ±0.2% max) and guaranteed low span drift: ±0.005%/°C max, ±0.01%/°C max, and ±0.015%/°C max, respectively. The internally trimmed span and offset errors are ±0.1% max for the 2B22L and ±0.25% max for the 2B22J/2B22K. Both span and offset are adjustable by the optional external potentiometers.

Featuring a wide range, single supply operation (+14V to +32V), the 2B22 provides isolated +28V loop power and is capable of delivering rated current into an external 0 to 1000Ω load resistance. The unique output stage configuration also allows the user to utilize an optional external loop power supply to interface systems designed for a two-wire operation.

### APPLICATIONS

Model 2B22 has been specifically designed for high accuracy applications in process control and monitoring systems to offer complete galvanic isolation and protection against damage from transients and fault voltages in transmitting information



between subsystems or separated system elements. The 2B22 meets the requirements of the Instrument Society of America Std. 50.1 "Compatibility of Analog Signals for Electronic Industrial Process Instruments" for Type 4, Class U isolated current loop transmitters.

In the industrial environment, model 2B22 can serve as a transmission link between such system elements as transmitters, indicators, controllers, recorders, computers, actuators and signal conditioners. In data acquisition and control systems, the 2B22 may act as an isolated interface between the D/A converter output of a microcomputer and standard 4 to 20mA analog loops.

### DESIGN FEATURES AND USER BENEFITS

**High Reliability:** Model 2B22 is a conservatively designed, compact, epoxy encapsulated module capable of reliable operation in harsh environments. To assure high reliability, the 2B22 has been designed to meet the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability).

**Process Signal Compatibility:** The versatile input stage design with a single resistor gain adjustment enables the 2B22 to accept any one of the standard inputs—0-1V, 0-10V, 1-5V; or 1-5mA, 4-20mA, 10-50mA; and provide standard, isolated 4-20mA output.

**Isolated Loop Power:** Internal 28V dc loop supply, completely isolated from the input power terminals (±1500V dc isolation), provides the capability to drive 0 to 1000Ω loads and eliminates the need for an external dc/dc converter.

# SPECIFICATIONS (typical @ +25°C and $V_S = +15V$ unless otherwise noted)

| Model   | 2B22J                       | 2B22K                       | 2B22L                        |
|---|-----------------------------|-----------------------------|------------------------------|
| <b>INPUT SPECIFICATIONS</b>                       |                             |                             |                              |
| Voltage Signal Range, $G = 1.6mA/V$               | 0 to +10V                   | *                           | *                            |
| $G = 16mA/V$                                      | 0 to +1V                    | *                           | *                            |
| Gain Range  | 1.6 to 16mA/V               | *                           | *                            |
| Maximum Safe Input                                | +15V                        | *                           | *                            |
| Input Impedance                                   | 10M $\Omega$                | *                           | *                            |
| <b>OUTPUT SPECIFICATIONS</b>                      |                             |                             |                              |
| Current Output Range                              | 4 to 20mA                   | *                           | *                            |
| Load Resistance Range, $V_S = +14V$ to +32V,      |                             |                             |                              |
| Internal Loop Power                               | 0 to 1000 $\Omega$ max      | *                           | *                            |
| Maximum Output Current, @ Input Overload          | 25mA                        | *                           | *                            |
| Output Ripple, 100Hz Bandwidth $G = 1.6mA/V$      | 60 $\mu A$ pk-pk            | *                           | *                            |
| <b>NONLINEARITY (% of Span)</b>                   |                             |                             |                              |
|   | $\pm 0.2\%$ max             | $\pm 0.1\%$ max             | $\pm 0.05\%$ max             |
| <b>CMV, INPUT TO OUTPUT</b>                       |                             |                             |                              |
| ac, 60Hz, 1 Minute Duration                       | 1500V rms                   | *                           | *                            |
| Continuous, ac or dc                              | $\pm 1500V$ pk max          | *                           | *                            |
| <b>CMR, INPUT TO OUTPUT</b>                       |                             |                             |                              |
| 60Hz, 1k $\Omega$ Source Imbalance                | 90dB                        | *                           | *                            |
| <b>ACCURACY<sup>1</sup></b>                       |                             |                             |                              |
| Warm Up Time to Rated Performance 5 Minutes       |                             |                             |                              |
| Total Output Error @ +25°C <sup>1,2</sup>         |                             |                             |                              |
| Offset ( $V_{IN} = 0V$ )                          | $\pm 0.25\%$ max            | $\pm 0.25\%$ max            | $\pm 0.1\%$ max              |
| Span ( $V_{IN} = +10V$ )                          | $\pm 0.25\%$ max            | $\pm 0.25\%$ max            | $\pm 0.1\%$ max              |
| vs. Temperature (0 to +70°C, $G = 1.6mA/V$ )      |                             |                             |                              |
| Offset ( $V_{IN} = 0V$ )                          | $\pm 0.01\%/^{\circ}C$ max  | $\pm 0.005\%/^{\circ}C$ max | $\pm 0.0025\%/^{\circ}C$ max |
| Span ( $V_{IN} = +10V$ )                          | $\pm 0.015\%/^{\circ}C$ max | $\pm 0.01\%/^{\circ}C$ max  | $\pm 0.005\%/^{\circ}C$ max  |
| vs. Temperature (0 to +70°C)                      |                             |                             |                              |
| Offset ( $V_{IN} = 0V$ , $G = 1.6mA/V$ to 16mA/V) | $\pm 0.01\%/^{\circ}C$      | $\pm 0.005\%/^{\circ}C$     | $\pm 0.0025\%/^{\circ}C$     |
| Span ( $G = 1.6mA/V$ to 16mA/V) <sup>3</sup>      | $\pm 0.015\%/^{\circ}C$     | $\pm 0.01\%/^{\circ}C$      | $\pm 0.005\%/^{\circ}C$      |
| <b>DYNAMIC RESPONSE</b>                           |                             |                             |                              |
| Settling Time - to 0.1% of F.S. for 10V Step      | 300 $\mu s$                 | *                           | *                            |
| Slew Rate   | 0.06mA/ $\mu s$             | *                           | *                            |
| <b>REFERENCE INPUT</b>                            |                             |                             |                              |
| Voltage   | +2.5V dc                    | *                           | *                            |
| Input Impedance                                   | 6k $\Omega$                 | *                           | *                            |
| <b>OSCILLATOR</b>                                 |                             |                             |                              |
| Frequency, Internal Oscillator                    | 100kHz $\pm 10\%$           | *                           | *                            |
| External Sync Input                               |                             |                             |                              |
| Frequency   | 100kHz $\pm 10\%$ max       | *                           | *                            |
| Waveform  | Square wave, 50% duty cycle | *                           | *                            |
| Voltage   | 20V p-p                     | *                           | *                            |
| <b>POWER SUPPLY</b>                               |                             |                             |                              |
| Voltage, Rated Performance                        | +15V dc                     | *                           | *                            |
| Voltage, Operating                                | +14V to +32V dc             | *                           | *                            |
| Supply Current (at Full Scale Output)             |                             |                             |                              |
| Using Internal Loop Power                         | 100mA                       | *                           | *                            |
| Using External Loop Power                         | 50mA                        | *                           | *                            |
| Supply Change Effect (% of Span)                  |                             |                             |                              |
| on Offset ( $V_{IN} = 0V$ )                       | $\pm 0.0005\%/V$            | *                           | *                            |
| on Span ( $V_{IN} = +10V$ )                       | $\pm 0.0005\%/V$            | *                           | *                            |
| <b>TEMPERATURE RANGE</b>                          |                             |                             |                              |
| Rated Performance                                 | 0 to +70°C                  | *                           | *                            |
| Operating   | -25°C to +75°C              | *                           | *                            |
| Storage   | -55°C to +85°C              | *                           | *                            |
| <b>CASE SIZE</b>                                  |                             |                             |                              |
|   | 2.2" X 3" X 0.6"            | *                           | *                            |

\*Specifications same as 2B22J.

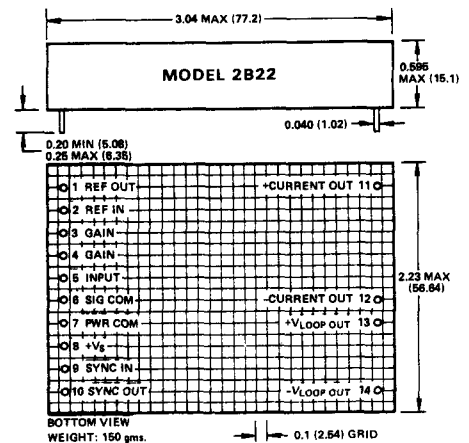
## NOTES

- Accuracy is guaranteed at  $G = 1.6mA/V$  with no external trim adjustments when connected as shown in Figure 1.
- All accuracy is % of span where span is 16mA ( $\pm 0.1\% = \pm 0.016mA$  error).
- Span T.C. for gains higher than 1.6mA/V is  $R_G$  dependent - a low T.C. ( $\pm 10ppm/^{\circ}C$ )  $R_G$  is recommended for best performance.

Specifications subject to change without notice.

## OUTLINE DIMENSIONS

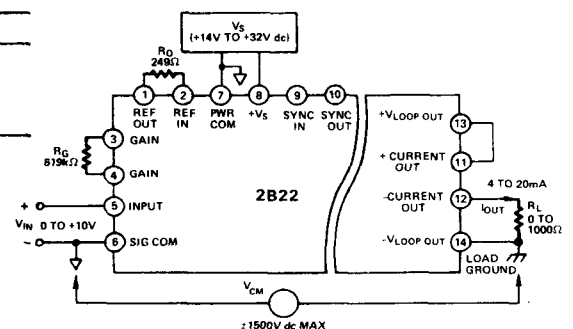
Dimensions shown in inches and (mm).



## MATING SOCKET:

### AC1579

**INTERCONNECTION DIAGRAM**  
Model 2B22 can be applied directly to achieve rated performance as shown in Figure 1 below. The input stage gain of 1.6mA/V, to convert a 0 to +10V signal into a 4 to 20mA output current, is obtained with the values shown. A single polarity power supply (+14V to +32V dc) should be connected to pin 8. To eliminate ground loops, the user should insure that the signal return (common) lead does not carry the power supply current. Power common (pin 7) and signal common (pin 6) should be tied at the power supply common terminal. The voltage difference between pins 6 and 7 should not exceed 0.2V. An internal dc-dc converter provides isolated output loop power (pins 13 and 14), which is connected externally to the current output terminals (pins 11 and 12) and a load resistance. The standard 4 to 20mA current output signal is delivered into any external load between zero and 1000 $\Omega$ .



NOTE: Resistors  $R_D$  and  $R_G$  are 1%, 50ppm/ $^{\circ}C$  Metal Film Type. Values shown are for  $G = 1.6mA/V$ . For  $G = 16mA/V$ , use 10ppm/ $^{\circ}C$   $R_G$  and 50ppm/ $^{\circ}C$   $R_D$ .

Figure 1. Basic Connections

# Applying the Isolated Voltage-to-Current Converter

## FUNCTIONAL DESCRIPTION

The high performance of model 2B22 is derived from the carrier isolation technique which is used to transfer both signal and power between the V/I converter's input circuitry and the output stage. High CMV isolation is achieved by the transformer coupling between the input amplifier, modulator section and the current output circuitry. The block diagram for model 2B22 is shown in Figure 2 below.

The 2B22 produces an isolated 4 to 20mA output current which is proportional to the voltage input and independent of the load resistance. The input amplifier operates single-ended and accepts a positive voltage within 0 to +10V range. Gain can be set from 1.6mA/V to 16mA/V by changing the gain resistor  $R_G$  to accommodate input ranges from 0 to +1V ( $G = 16\text{mA/V}$ ) to 0 to +10V ( $G = 1.6\text{mA/V}$ ). The transfer function is  $I_{OUT} = (4\text{mA} + G \times V_{IN})$ .

An internal, high stability reference has nominal output voltage of +2.5V (REF OUT) and is used to develop a 4mA output current for a 0 volts input. The terminals REF OUT (pin 1) and REF IN (pin 2) should be connected via the offset setting resistor  $R_O$ . For ratiometric operation, an external reference voltage can be connected to the REF IN terminal.

The 2B22 is designed to operate from a single positive power supply over a wide range of +14V to +32V dc. An internal dc-dc converter provides isolated +28V loop power which is independent of  $+V_S$ . The maximum resistance of the load  $R_L$  (resistance of the receivers plus the resistance of the connecting wire) is 1000 $\Omega$ . Since the loop power is derived from the input side, the current capability of the power supply ( $+V_S$ ) must be 100mA min to supply full output signal current.

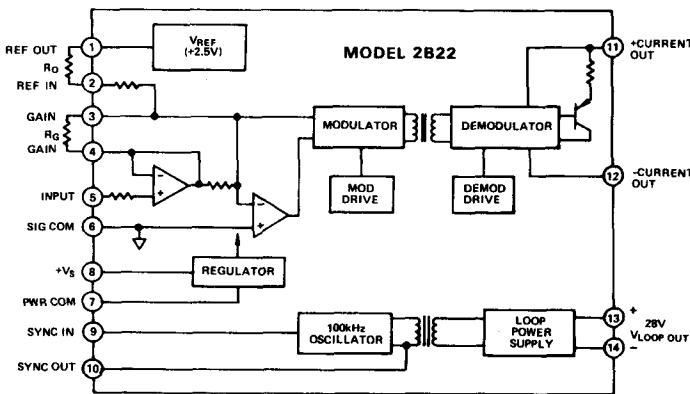


Figure 2. Block Diagram - Model 2B22

## OPTIONAL TRIM ADJUSTMENTS

Model 2B22 is factory calibrated for a 0 to +10V input range ( $G = 1.6\text{mA/V}$ ). As shipped, the 2B22 meets its listed specifications without use of any external trim potentiometers. Additional trim adjustment capability, to reduce span and offset errors to  $\pm 0.05\%$  max, is easily provided as shown in Figure 3. The span and offset trim pots are adjusted while monitoring the voltage drop across a precision (or known) load resistor. The following trim procedure is recommended:

1. Connect model 2B22 as shown in Figure 3.
2. Apply  $V_{IN} = 0$  volts and adjust  $R_O$  (Offset Adjust) for  $V_{OUT} = +2V \pm 4\text{mV}$ .

3. Apply  $V_{IN} = +10.00\text{V}$  and adjust  $R_G$  (Span Adjust) for  $V_{OUT} = +10V \pm 4\text{mV}$ .

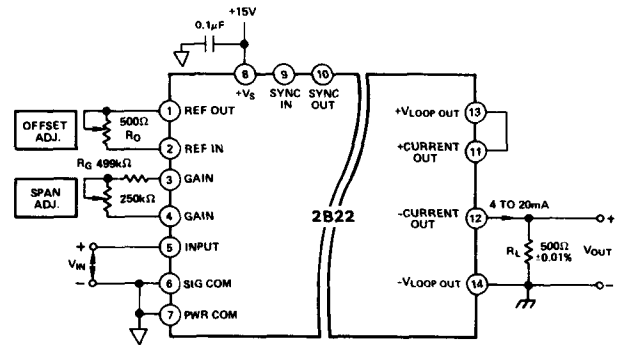


Figure 3. Optional Span and Offset Adjustment

## GAIN AND OFFSET SETTING

The gain of the 2B22 is a scale factor setting that establishes the nominal conversion relationship to accommodate +1V to +10V full scale inputs ( $V_{IN}$ ). The value of the gain setting resistor  $R_G$  is determined by:  $R_G (\text{k}\Omega) = 6.314\text{SF}/(10.1 - \text{SF})$  where SF is a scale factor equal to the value of  $V_{IN}$  F.S. Example: to convert a 0 to +1V input to the 4 to 20mA output,  $\text{SF} = 1$  and  $R_G = 693\Omega$ . Due to device tolerances, allowance should be made to vary  $R_G$  by  $\pm 5\%$  using the potentiometer.

The value of the offset resistor  $R_O$  is independent from the gain setting and given by the relationship:  $R_O (\text{k}\Omega) = 2.5 (V_{REF} - 2.4)$  where  $V_{REF}$  is the reference voltage applied. For example, the reference provided by the 2B22 is +2.5V and therefore  $R_O = 250\Omega$ . The accuracy of the  $R_O$  calculation from the above formula is  $\pm 5\%$ . When an external reference operation is desired (i.e. for ratiometric operation), connect the reference voltage via  $R_O$  to pin 2 and leave pin 1 open.

## EXTERNAL LOOP POWER OPERATION

For maximum versatility, the 2B22's output stage is designed to operate from the optional, isolated external loop power supply. This feature allows the user to interface systems wired for a two-wire operation. As shown in Figure 4, the same wiring is used for loop power and output. The load resistance is connected in series with an external dc power supply (+6V to +32V), and the current drawn from the supply is the 4 to 20mA output signal. The input stage of the 2B22 still requires  $+V_S$  power, but the current drain from  $+V_S$  is limited to 50mA. Use of an external loop power may require gain and offset trimming to obtain specified accuracy. The maximum series load resistance depends on the loop supply voltage as shown in Figure 4.

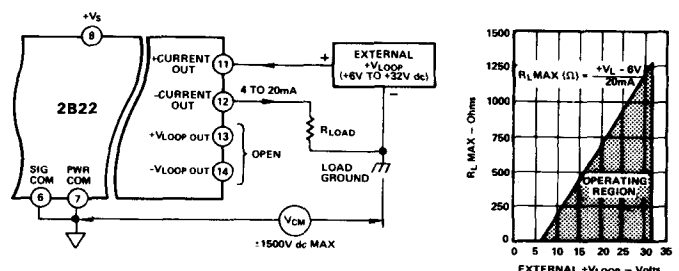


Figure 4. Optional External Loop Power Operation



## SYNCHRONIZING MULTIPLE 2B22'S

In applications where multiple 2B22's are used in close proximity, radiated individual oscillator frequencies may cause "beat frequency" related output errors. These errors can be eliminated by synchronizing multiple units by connecting the SYNC OUT (pin 10) terminal to the SYNC IN (pin 9) terminal of the adjacent 2B22. The SYNC OUT terminal of this "slaved" unit can be used to drive another adjacent 2B22 (Figure 5). For best accuracy, each 2B22 should be retrimmed when synchronizing connections are used.

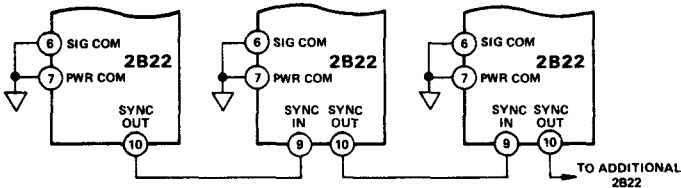


Figure 5. Multiple 2B22's Synchronization

## OUTPUT PROTECTION

The current output terminals (pins 11 and 12) are protected from shorts up to +32V dc but in many industrial applications, it may be necessary to protect the 4 to 20mA output from accidental shorts to ac line voltages. The circuit shown in Figure 6 can be used for this purpose. The maximum permissible load resistance will be lowered by a fuse resistance value when protection circuitry is utilized.

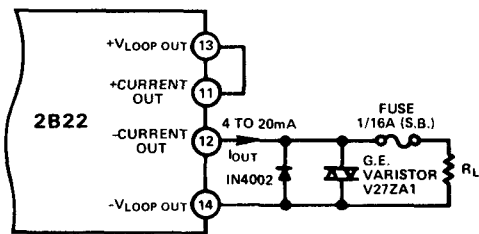


Figure 6. Output Protection Circuitry Connections

## APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

**Process Signal Isolator:** In process control applications, model 2B22 can be applied to interface standard process signals (e.g. 1 to 5mA, 4 to 20mA, 10 to 50mA, 1 to 5V) and convert them to isolated 4 to 20mA output. A typical hook-up of model 2B22 is illustrated in Figure 7, showing input resistor

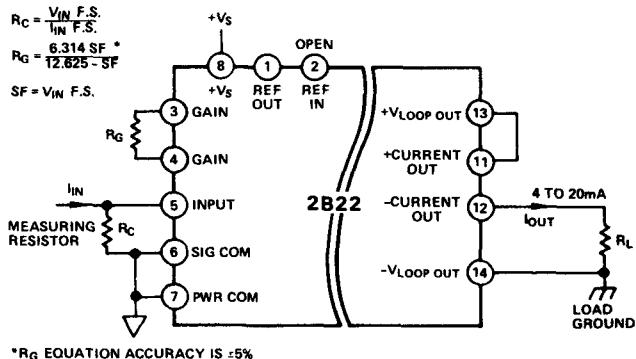


Figure 7. Process Signal Current Isolator

$R_C$  converting the current from a remote loop to a voltage input, and a span adjustment resistor  $R_C$ . A value of  $R_C$  should be selected to develop a minimum of +1V signal with full scale input current applied. For example, a 50 $\Omega$  resistor converts the 4 to 20mA current input to a 200mV to 1V voltage input, which the 2B22 isolates and converts to a 4 to 20mA output. The reference input (pin 2) is not connected since the process signal provides a desired offset.

**Isolated D/A Converter:** Model 2B22 offers total ground isolation and protection from high voltage transients in interfacing D/A converters to standard 4 to 20mA current loops. This requirement is common in a microcomputer-based control system. The voltage necessary to power the current loop can be derived from the same +15V supply that is used to power the D/A converter. The D/A converter, such as the 12-bit AD DAC80, should be connected for operation on the unipolar 0 to +10V output range. This is shown in Figure 8. After the load resistor connection has been made, the current loop can be calibrated using the offset and span adjustment potentiometers associated with the 2B22. First, a digital input code of all zeros is loaded into the D/A, and the offset adjustment potentiometer is adjusted for a current output of exactly 4mA. Then, a digital code of all one's is loaded into the D/A, and the span adjustment potentiometer is adjusted for a voltage across the load that corresponds to a current of 20mA less 1LSB (19.9961mA).

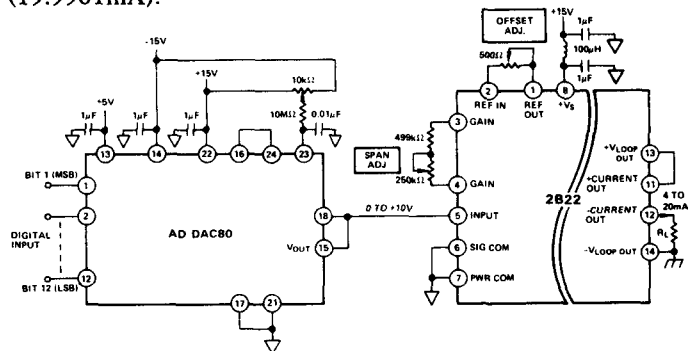


Figure 8. D/A Converter - Isolated 4 to 20mA Interface

**Pressure Transmitter:** In Figure 9, model 2B22 is used in a pressure transmitter application to provide complete input-output isolation and avoid signal errors due to ground loop currents. The process pressure is monitored with a strain gage type pressure transducer interfaced by the Analog Devices' model 2B30 transducer conditioner. The bridge excitation and system power is provided by the model 2B35 triple output power supply. The high level voltage output of the 2B30 is converted to the isolated 4 to 20mA current for transmission to a remote recorder or indicator.

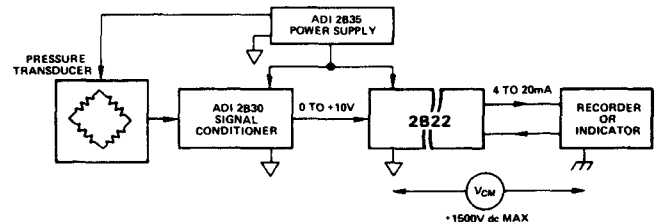


Figure 9. Isolated Pressure Transmitter

### FEATURES

#### Low Cost

#### Complete Signal Conditioning Function

Low Drift:  $0.5\mu\text{V}/^\circ\text{C}$  max ("L"); Low Noise:  $1\mu\text{V}$  p-p max

Wide Gain Range: 1 to 2000V/V

Low Nonlinearity: 0.0025% max ("L")

High CMR: 140dB min (60Hz,  $G = 1000\text{V}/\text{V}$ )

Input Protected to 130V rms

Adjustable Low Pass Filter: 60dB/Decade Roll-Off (from 2Hz)

Programmable Transducer Excitation: Voltage (4V to 15V @ 100mA) or Current (100 $\mu\text{A}$  to 10mA)

### APPLICATIONS

#### Measurement and Control of:

Pressure, Temperature, Strain/Stress, Force, Torque

Instrumentation: Indicators, Recorders, Controllers

Data Acquisition Systems

Microcomputer Analog I/O

### GENERAL DESCRIPTION

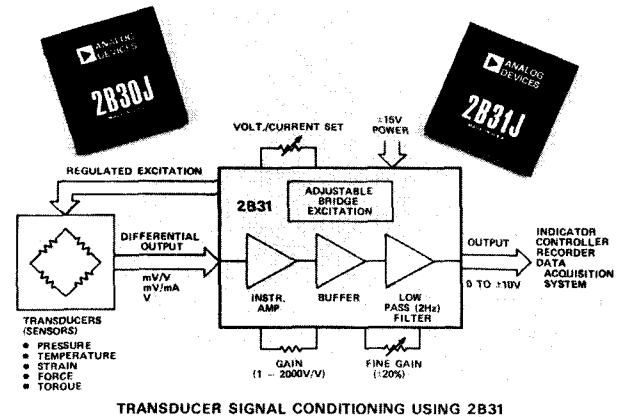
Models 2B30 and 2B31 are high performance, low cost, compact signal conditioning modules designed specifically for high accuracy interface to strain gage-type transducers and RTD's (resistance temperature detectors). The 2B31 consists of three basic sections: a high quality instrumentation amplifier; a three-pole low pass filter, and an adjustable transducer excitation. The 2B30 has the same amplifier and filter as the 2B31, but no excitation capability.

Available with low offset drift of  $0.5\mu\text{V}/^\circ\text{C}$  max (RT1,  $G = 1000\text{V}/\text{V}$ ) and excellent linearity of 0.0025% max, both models feature guaranteed low noise performance  $1\mu\text{V}$  p-p max, and outstanding 140dB common mode rejection (60Hz,  $\text{CMV} = \pm 10\text{V}$ ,  $G = 1000\text{V}/\text{V}$ ) enabling the 2B30/2B31 to maintain total amplifier errors below 0.1% over a  $20^\circ\text{C}$  temperature range. The low pass filter offers 60dB/decade roll-off from 2Hz to reduce normal-mode noise bandwidth and improve system signal-to-noise ratio. The 2B31's regulated transducer excitation stage features a low output drift (0.015%/°C max) and a capability of either constant voltage or constant current operation.

Gain, filter cutoff frequency, output offset level and bridge excitation (2B31) are all adjustable, making the 2B30/2B31 the industry's most versatile high-accuracy transducer-interface modules. Both models are offered in three accuracy selections, J/K/L, differing only in maximum nonlinearity and offset drift specifications.

### APPLICATIONS

The 2B30/2B31 may be easily and directly interfaced to a wide variety of transducers for precise measurement and control of pressure, temperature, stress, force and torque. For ap-



TRANSDUCER SIGNAL CONDITIONING USING 2B31

plications in harsh industrial environments, such characteristics as high CMR, input protection, low noise, and excellent temperature stability make 2B30/2B31 ideally suited for use in indicators, recorders, and controllers.

The combination of low cost, small size and high performance of the 2B30/2B31 offers also exceptional quality and value to the data acquisition system designer, allowing him to assign a conditioner to each transducer channel. The advantages of this approach over low level multiplexers include significant improvements in system noise and resolution, and elimination of crosstalk and aliasing errors.

### DESIGN FEATURES AND USER BENEFITS

**High Noise Rejection:** The true differential input circuitry with high CMR (140dB) eliminating common-mode noise pickup errors, input filtering minimizing RFI/EMI effects, output low pass filtering ( $f_c=2\text{Hz}$ ) rejecting 50/60Hz line frequency pickup and series-mode noise.

**Input and Output Protection:** Input protected for shorts to power lines (130V rms), output protected for shorts to ground and either supply.

**Ease of Use:** Direct transducer interface with minimum external parts required, convenient offset and span adjustment capability.

**Programmable Transducer Excitation:** User-programmable adjustable excitation source-constant voltage (4V to 15V @ 100mA) or constant current (100 $\mu\text{A}$  to 10mA) to optimize transducer performance.

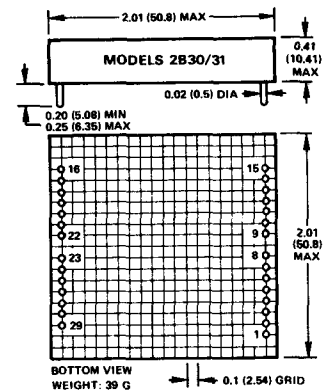
**Adjustable Low Pass Filter:** The three-pole active filter ( $f_c=2\text{Hz}$ ) reducing noise bandwidth and aliasing errors with provisions for external adjustment of cutoff frequency.

# SPECIFICATIONS (typical @ +25°C and V<sub>S</sub> = ±15V unless otherwise noted)

| MODEL  | 2B30J<br>2B31J  | 2B30K<br>2B31K       | 2B30L<br>2B31L         |
|--|---|----------------------|------------------------|
| <b>GAIN<sup>1</sup></b>                                  |   |                      |                        |
| Gain Range   | 1 to 2000V/V  | *                    | *                      |
| Gain Equation  | $G = (1 + 94k\Omega/R_G) [20k\Omega/(R_F + 16.2k\Omega)]$ | *                    | *                      |
| Gain Equation Accuracy                                   | ±2%   | *                    | *                      |
| Fine Gain (Span) Adjust. Range                           | ±20%  | *                    | *                      |
| Gain Temperature Coefficient                             | ±25ppm/°C max (±10ppm/°C typ)                             | *                    | *                      |
| Gain Nonlinearity  | ±0.01% max  | ±0.005% max          | ±0.0025% max           |
| <b>OFFSET VOLTAGES<sup>1</sup></b>                       |   |                      |                        |
| Total Offset Voltage, Referred to Input                  |   |                      |                        |
| Initial, @ +25°C   | Adjustable to Zero (±0.5mV typ)                           | *                    | *                      |
| Warm-Up Drift, 10 Min., G = 1000 vs. Temperature         | ±5μV RTI  | *                    | *                      |
| G = 1V/V   | ±150μV/°C max   | ±75μV/°C max         | ±50μV/°C max           |
| G = 1000V/V  | ±3μV/°C max   | ±1μV/°C max          | ±0.5μV/°C max          |
| At Other Gains   | ±(3 ± 150/G)μV/°C max                                     | ±(1 ± 75/G)μV/°C max | ±(0.5 ± 50/G)μV/°C max |
| vs. Supply, G = 1000V/V                                  | ±2.5μV/V  | *                    | *                      |
| vs. Time, G = 1000V/V                                    | ±3μV/month  | *                    | *                      |
| Output Offset Adjust. Range                              | ±1.5V   | *                    | *                      |
| <b>INPUT BIAS CURRENT</b>                                |   |                      |                        |
| Initial @ +25°C  | +200nA max (100nA typ)                                    | *                    | *                      |
| vs. Temperature (0 to +70°C)                             | -0.6nA/°C   | *                    | *                      |
| <b>INPUT DIFFERENCE CURRENT</b>                          |   |                      |                        |
| Initial @ +25°C  | ±5nA  | *                    | *                      |
| vs. Temperature (0 to +70°C)                             | ±40pA/°C  | *                    | *                      |
| <b>INPUT IMPEDANCE</b>                                   |   |                      |                        |
| Differential   | 100MΩ  47pF   | *                    | *                      |
| Common Mode  | 100MΩ  47pF   | *                    | *                      |
| <b>INPUT VOLTAGE RANGE</b>                               |   |                      |                        |
| Linear Differential Input                                | ±10V  | *                    | *                      |
| Maximum Differential or CMV Input Without Damage         | 130V rms  | *                    | *                      |
| Common Mode Voltage                                      | ±10V  | *                    | *                      |
| CMR, 1kΩ Source Imbalance                                |   | *                    | *                      |
| G = 1V/V, dc to 60Hz <sup>1</sup>                        | 90dB  | *                    | *                      |
| G = 100V/V to 2000V/V, 60Hz <sup>1</sup> dc <sup>2</sup> | 140dB min<br>90dB min (112 typ.)                          | *                    | *                      |
| <b>INPUT NOISE</b>                                       |   |                      |                        |
| Voltage, G = 1000V/V                                     |   | *                    | *                      |
| 0.01Hz to 2Hz  | 1μV p-p max   | *                    | *                      |
| 10Hz to 100Hz <sup>2</sup>                               | 1μV p-p   | *                    | *                      |
| Current, G = 1000  |   | *                    | *                      |
| 0.01Hz to 2Hz  | 70pA p-p  | *                    | *                      |
| 10Hz to 100Hz <sup>2</sup>                               | 30pA rms  | *                    | *                      |
| <b>RATED OUTPUT<sup>1</sup></b>                          |   |                      |                        |
| Voltage, 2kΩ Load <sup>3</sup>                           | ±10V min  | *                    | *                      |
| Current  | ±5mA min  | *                    | *                      |
| Impedance, dc to 2Hz, G = 100V/V                         | 0.1Ω  | *                    | *                      |
| Load Capacitance   | 0.01μF max  | *                    | *                      |
| <b>DYNAMIC RESPONSE (Unfiltered)<sup>2</sup></b>         |   |                      |                        |
| Small Signal Bandwidth                                   |   |                      |                        |
| -3dB Gain Accuracy, G = 100V/V                           | 30kHz   | *                    | *                      |
| G = 1000V/V  | 5kHz  | *                    | *                      |
| Slew Rate  | 1V/μs   | *                    | *                      |
| Full Power   | 15kHz   | *                    | *                      |
| Settling Time, G = 100, ±10V Output Step to ±0.1%        | 30μs  | *                    | *                      |
| <b>LOW PASS FILTER (Bessel)</b>                          |   |                      |                        |
| Number of Poles  | 3   | *                    | *                      |
| Gain (Pass Band)   | +1  | *                    | *                      |
| Cutoff Frequency (-3dB Point)                            | 2Hz   | *                    | *                      |
| Roll-Off   | 60dB/decade   | *                    | *                      |
| Offset (at 25°C)   | ±5mV  | *                    | *                      |
| Settling Time, G = 100V/V, ±10V Output Step to ±0.1%     | 600ms   | *                    | *                      |
| <b>BRIDGE EXCITATION (See Table 1) - Page 104S</b>       |   |                      |                        |
| <b>POWER SUPPLY<sup>4</sup></b>                          |   |                      |                        |
| Voltage, Rated Performance                               | ±15V dc   | *                    | *                      |
| Voltage, Operating                                       | ±(12 to 18)V dc   | *                    | *                      |
| Current, Quiescent                                       | ±15mA   | *                    | *                      |
| <b>TEMPERATURE RANGE</b>                                 |   |                      |                        |
| Rated Performance  | 0 to +70°C  | *                    | *                      |
| Operating  | -25°C to +85°C  | *                    | *                      |
| Storage  | -55°C to +125°C   | *                    | *                      |
| <b>CASE SIZE</b>   |   |                      |                        |
|  | 2" x 2" x 0.4" (51 x 51 x 10.2mm)                         | *                    | *                      |

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

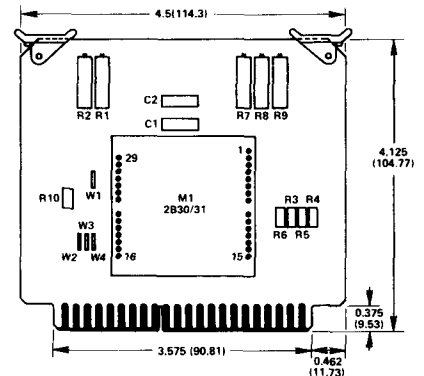


## PIN DESIGNATIONS

| PIN | FUNCTION              | PIN | FUNCTION                     |
|-----|-----------------------|-----|------------------------------|
| 1   | OUTPUT 1 (UNFILTERED) | 16  | EXC SEL 1                    |
| 2   | FINE GAIN (SPAN) ADJ. | 17  | I SEL                        |
| 3   | FINE GAIN (SPAN) ADJ. | 18  | VEXC OUT                     |
| 4   | FILTER OFFSET TRIM    | 19  | EXC OUT                      |
| 5   | FILTER OFFSET TRIM    | 20  | SENSE HIGH (+)               |
| 6   | BANDWIDTH ADJ. 3      | 21  | EXC SEL 2                    |
| 7   | OUTPUT 2 (FILTERED)   | 22  | REF OUT                      |
| 8   | BANDWIDTH ADJ. 2      | 23  | SENSE LOW (-)                |
| 9   | BANDWIDTH ADJ. 1      | 24  | REGULATOR +V <sub>R</sub> IN |
| 10  | R <sub>GAIN</sub>     | 25  | REF IN                       |
| 11  | R <sub>GAIN</sub>     | 26  | -V <sub>S</sub>              |
| 12  | -INPUT                | 27  | +V <sub>S</sub>              |
| 13  | INPUT OFFSET TRIM     | 28  | COMMON                       |
| 14  | INPUT OFFSET TRIM     | 29  | OUTPUT OFFSET TRIM           |
| 15  | +INPUT                |     |                              |

Note: Pins 16 thru 25 are not connected in Model 2B31

## AC1211 MOUNTING CARD



## AC1211 CONNECTOR DESIGNATIONS

| PIN | FUNCTION                     | PIN | FUNCTION              |
|-----|------------------------------|-----|-----------------------|
| A   | REGULATOR +V <sub>R</sub> IN | 1   | EXC SEL 1             |
| B   | SENSE LOW (-)                | 2   | I SEL                 |
| C   | REF OUT                      | 3   | VEXC OUT              |
| D   | REF IN                       | 4   | EXC OUT               |
| E   |                              | 5   | SENSE HIGH (+)        |
| F   |                              | 6   | EXC SEL 2             |
| G   |                              | 7   | OUTPUT OFFSET TRIM    |
| H   |                              | 8   |                       |
| K   | -V <sub>S</sub>              | 9   | -V <sub>S</sub>       |
| L   | +V <sub>S</sub>              | 10  | +V <sub>S</sub>       |
| M   |                              | 11  |                       |
| N   | COMMON                       | 12  | COMMON                |
| P   |                              | 13  |                       |
| R   | FINE GAIN ADJ.               | 14  |                       |
| S   | FINE GAIN ADJ.               | 15  |                       |
| T   | FILTER OFFSET TRIM           | 16  |                       |
| U   | FILTER OFFSET TRIM           | 17  | R <sub>GAIN</sub>     |
| V   | OUTPUT 2 (FILTERED)          | 18  | R <sub>GAIN</sub>     |
| W   | -INPUT                       | 19  | OUTPUT 1 (UNFILTERED) |
| X   | INPUT OFFSET TRIM            | 20  | BANDWIDTH ADJ. 1      |
| Y   | INPUT OFFSET TRIM            | 21  | BANDWIDTH ADJ. 3      |
| Z   | +INPUT                       | 22  | BANDWIDTH ADJ. 2      |

The AC1211 mounting card is available to assist in evaluation of the 2B30/2B31. The AC1211 is an edge connector card with pin receptacles for plugging in the 2B30/2B31. In addition, the AC1211 has provisions for installing the gain control resistors and the bridge excitation, offset adjustment and filter cutoff programming components. The AC1211 mates with a Cinch 251-22-30-160 (or equivalent) edge connector which is supplied with every card.

\*Specifications same as 2B30J/2B31J.

<sup>1</sup> Specifications referred to output at pin 7 with 3.75k, 1%, 25ppm/°C fine span resistor installed and internally set 2Hz filter cutoff frequency.

<sup>2</sup> Specifications referred to the unfiltered output at pin 1.

<sup>3</sup> Protected for shorts to ground and/or either supply voltage.

<sup>4</sup> Recommended power supply ADI model 902-2 or model 2B35 transducer power supply (for 2B30).

Specifications subject to change without notice.

## FUNCTIONAL DESCRIPTION

Models 2B30 and 2B31 accept inputs from a variety of full bridge strain gage-type transducers or RTD sensors and convert the inputs to conditioned high level analog outputs. The primary transducers providing direct inputs may be 60Ω to 1000Ω strain gage bridges, four-wire RTD's or two- or three-wire RTD's in the bridge configuration.

The 2B30 and 2B31 employ a multi-stage design, shown in Figure 1, to provide excellent performance and maximum versatility. The input stage is a high input impedance ( $10^8 \Omega$ ), low offset and drift, low noise differential instrumentation amplifier. The design is optimized to accurately amplify low level (mV) transducer signals riding on high common mode voltages ( $\pm 10V$ ), with wide (1-2000V/V), single resistor ( $R_G$ ), programmable gain to accommodate 0.5mV/V to 36mV/V transducer spans and 5Ω to 2000Ω RTD spans. The input stage contains protection circuitry for accidental shorts to power line voltage (130V rms) and RFI filtering circuitry.

The inverting buffer amplifier stage provides a convenient means of fine gain trim (0.8 to 1.2) by using a 10kΩ potentiometer ( $R_F$ ); the buffer also allows the output to be offset by up to  $\pm 1.5V$  by applying a voltage to the noninverting input (pin 29). For dynamic, high bandwidth measurements — the buffer output (pin 1) should be used.

The three-pole active filter uses a unity-gain configuration and provides low-pass Bessel-type characteristics—minimum overshoot response to step inputs and a fast rise time. The cutoff frequency (-3dB) is factory set at 2Hz, but may be increased up to 5kHz by addition of three external resistors ( $R_{SEL1}$  -  $R_{SEL3}$ ).

## INTERCONNECTION DIAGRAM AND SHIELDING TECHNIQUES

Figure 1 illustrates the 2B31 wiring configuration when used in a typical bridge transducer signal conditioning application. A recommended shielding and grounding technique for preserving the excellent performance characteristics of the 2B30/2B31 is shown.

Because models 2B30/2B31 are direct coupled, a ground return path for amplifier bias currents must be provided either by direct connection (as shown) or by an implicit ground path having up to 1MΩ resistance between signal ground and conditioner common (pin 28). The sensitive input and gain setting

terminals should be shielded from noise sources for best performance, especially at high gains. To avoid ground loops, signal return or cable shield should never be grounded at more than one point.

The power supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible.

## TYPICAL APPLICATION AND ERROR BUDGET ANALYSIS

Models 2B30/2B31 have been conservatively specified using min-max values as well as typicals to allow the designer to develop accurate error budgets for predictable performance. The error calculations for a typical transducer application, shown in Figure 1 (350Ω bridge, 1mV/V F.S., 10V excitation), are illustrated below.

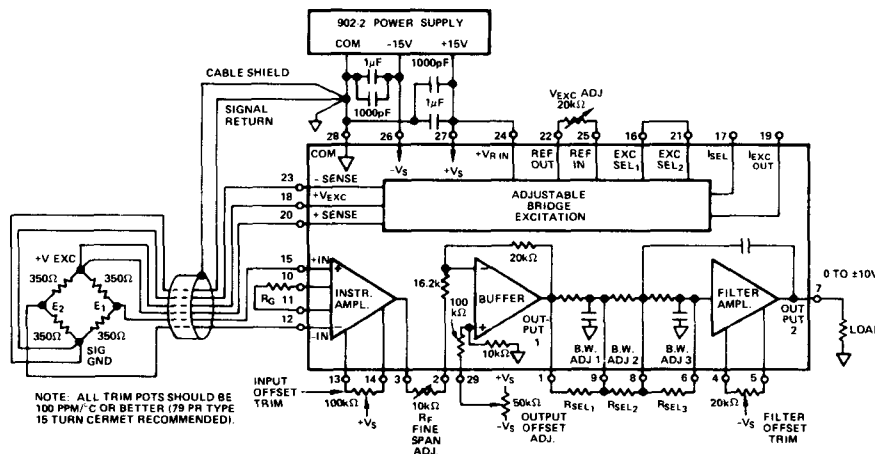
Assumptions: 2B31L is used,  $G = 1000$ ,  $\Delta T = \pm 10^\circ C$ , source imbalance is 100Ω, common mode noise is 0.25V (60Hz) on the ground return.

Absolute gain and offset errors can be trimmed to zero. The remaining error sources and their effect on system accuracy (worst case) as a % of Full Scale (10V) are listed:

| Error Source                    | Effect on Absolute Accuracy % of F.S. | Effect on Resolution % of F.S. |
|---------------------------------|---------------------------------------|--------------------------------|
| Gain Nonlinearity               | $\pm 0.0025$                          | $\pm 0.0025$                   |
| Gain Drift                      | $\pm 0.025$                           |                                |
| Voltage Offset Drift            | $\pm 0.05$                            |                                |
| Offset Current Drift            | $\pm 0.004$                           |                                |
| CMR                             | $\pm 0.00025$                         | $\pm 0.00025$                  |
| Noise (0.01 to 2Hz)             | $\pm 0.01$                            | $\pm 0.01$                     |
| <hr/>                           |                                       |                                |
| Total Amplifier Error           | $\pm 0.09175$ max                     | $\pm 0.01275$ max              |
| Excitation Drift                | $\pm 0.15$ ( $\pm 0.03$ typ)          |                                |
| <hr/>                           |                                       |                                |
| Total Output Error (Worst Case) | $\pm 0.24175$ max ( $\pm 0.1$ typ)    | $\pm 0.0127$ max               |

The total worst case effect on absolute accuracy over  $\pm 10^\circ C$  is less than  $\pm 0.25\%$  and the 2B31 is capable of 1/2 LSB resolution in a 12 bit, low input level system. Since the 2B31 is conservatively specified, a typical overall accuracy error would be lower than  $\pm 0.1\%$  of F.S.

In a computer or microprocessor based system, automatic recalibration can nullify gain and offset drifts leaving noise, nonlinearity and CMR as the only error sources. A transducer excitation drift error is frequently eliminated by a ratiometric operation with the system's A/D converter.



## BRIDGE EXCITATION (2B31)

The bridge excitation stage of the model 2B31 is an adjustable output, short circuit protected, regulated supply with internally provided reference voltage (+7.15V). The remote sensing inputs are used in the voltage output mode to compensate for the voltage drop variations in long leads to the transducer. The regulator circuitry input (pin 24) may be connected to +V<sub>S</sub> or some other positive dc voltage (pin 28 referenced) within specified voltage level and load current range. User-programmable constant voltage or constant current excitation mode may be used. Specifications are listed below in Table 1.

| MODEL  | 2B31J                          | 2B31K | 2B31L |
|--|--------------------------------|-------|-------|
| Constant Voltage Output Mode                                   |                                |       |       |
| Regulator Input Voltage Range                                  | +9.5V to +28V                  | *     | *     |
| Output Voltage Range   | +4V to +15V                    | *     | *     |
| Regulator Input/Output Voltage                                 |                                |       |       |
| Differential   | 3V to 24V                      | *     | *     |
| Output Current <sup>5</sup>                                    | 0 to 100mA max                 | *     | *     |
| Regulation, Output Voltage vs. Supply                          | 0.05%/V                        | *     | *     |
| Load Regulation, I <sub>L</sub> = 1mA to I <sub>L</sub> = 50mA | 0.1%                           | *     | *     |
| Output Voltage vs. Temperature (0 to +70°C)                    | 0.015%/°C max<br>0.003%/°C typ | *     | *     |
| Output Noise   | 1mV rms                        | *     | *     |
| Reference Voltage (Internal)                                   | 7.15V ±3%                      | *     | *     |
| Constant Current Output Mode                                   |                                |       |       |
| Regulator Input Voltage Range                                  | +9.5V to +28V                  | *     | *     |
| Output Current Range   | 100μA to 10mA                  | *     | *     |
| Compliance Voltage   | 0 to 10V                       | *     | *     |
| Load Regulation  | 0.1%                           | *     | *     |
| Temperature Coefficient (0 to +70°C)                           | 0.003%/°C                      | *     | *     |
| Output Noise   | 1μA rms                        | *     | *     |

Table 1. Bridge Excitation Specifications

## OPERATING INSTRUCTIONS

**Gain Setting:** The differential gain, G, is determined according to the equation:

$$G = (1 + 94k\Omega/R_G) [20k\Omega/(R_F + 16.2k\Omega)]$$

where R<sub>G</sub> is the input stage resistor shown in Figure 1 and R<sub>F</sub> is the variable 10kΩ resistor in the output stage. For best performance, the input stage gain should be made as large as possible, using a low temperature coefficient (10ppm/°C) R<sub>G</sub>, and the output stage gain can then be used to make a ±20% linear gain adjustment by varying R<sub>F</sub>.

**Input Offset Adjustment:** To null input offset voltage, an optional 100kΩ potentiometer connected between pins 13 and 14 (Figure 1) can be used. With gain set at the desired value, connect both inputs (pins 12 and 15) to the system common (pin 28), and adjust the 100kΩ potentiometer for zero volts at pin 3. The purpose of this adjustment is to null the internal amplifier offset and it is not intended to compensate for the transducer bridge unbalance.

**Output Offset Adjustment:** The output of the 2B30/2B31 can be intentionally offset from zero over the ±1.5V range by applying a voltage to pin 29, e.g., by using an external potentiometer or a fixed resistor. Pin 29 is normally grounded if output offset setting is not desired. The optional filter amplifier offset null capability is also provided as illustrated in Figure 1.

**Filter Cutoff Frequency Programming:** The low pass filter cutoff frequency may be increased from the internally set 2Hz by the addition of three external resistors connected as shown in Figure 1. The values of resistors required for a desired cutoff frequency, f<sub>c</sub>, are obtained by the equations below:

$$R_{SEL1} = 11.6 \times 10^6 / (2.67f_c - 4.34);$$

$$R_{SEL2} = 27.6 \times 10^6 / (4.12f_c - 7)$$

$$R_{SEL3} = 1.05 \times 10^6 / (0.806f_c - 1.3)$$

where R<sub>SEL</sub> is in ohms and f<sub>c</sub> in Hz. Table 2 gives values for R<sub>SEL</sub> for several common filter cutoff (-3dB) frequencies.

| f <sub>c</sub> (Hz) | R <sub>SEL1</sub> (kΩ)<br>(Pin 1 to 9) | R <sub>SEL2</sub> (kΩ)<br>(Pin 9 to 8) | R <sub>SEL3</sub> (kΩ)<br>(Pin 8 to 6) |
|---------------------|--|--|--|
| 2                   | Open                                   | Open                                   | Open                                   |
| 5                   | 1270.000                               | 2050.00                                | 383.000                                |
| 10                  | 523.000                                | 806.00                                 | 154.000                                |
| 50                  | 90.000                                 | 137.00                                 | 26.700                                 |
| 100                 | 44.200                                 | 68.10                                  | 13.300                                 |
| 500                 | 8.660                                  | 13.30                                  | 2.610                                  |
| 1000                | 4.320                                  | 6.65                                   | 1.300                                  |
| 5000                | 0.866                                  | 1.33                                   | 0.261                                  |

Table 2. Filter Cutoff Frequency vs. R<sub>SEL</sub>

**Voltage Excitation Programming:** Pin connections for a constant voltage output operation are shown in Figure 2. The bridge excitation voltage, V<sub>EXC</sub>, is adjusted between +4V to +15V by the 20kΩ (50ppm/°C) R<sub>VSEL</sub> potentiometer. For ratiometric operation, the bridge excitation can be adjusted by applying an external positive reference to pin 25 of the 2B31. The output voltage is given by: V<sub>EXC OUT</sub> = 3.265V<sub>REF IN</sub>. The remote sensing leads should be externally connected to the excitation leads at the transducer or jumpered as shown in Figure 2 if sensing is not required.

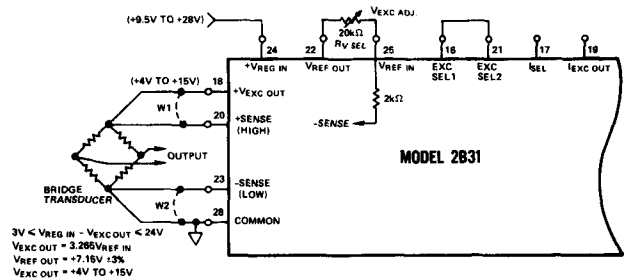


Figure 2. Constant Voltage Excitation Connections

**Current Excitation Programming:** The constant current excitation output can be adjusted between 100μA to 10mA by two methods with the 2B31. Figure 3 shows circuit configuration for a current output with the maximum voltage developed across the sensor (compliance voltage) constrained to +5V. The value of programming resistor R<sub>ISEL</sub> may be calculated from the relationship: R<sub>ISEL</sub> = (V<sub>REG IN</sub> - V<sub>REF IN</sub>)/I<sub>EXC OUT</sub>.

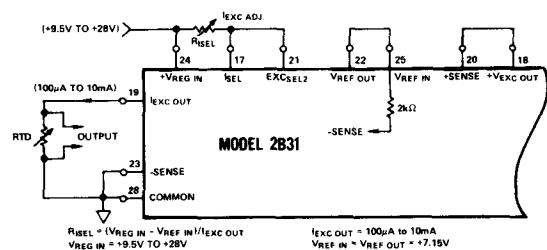


Figure 3. Constant Current Excitation Connections (V<sub>COMPL</sub> = 0 to +5V)

A compliance voltage range of 0 to +10V can be obtained by connecting the 2B31 as shown in Figure 4. The 2kΩ potentiometer R<sub>ISEL</sub> is adjusted for desired constant current excitation output.

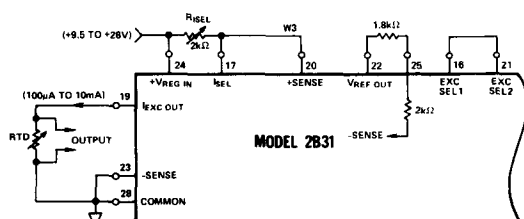


Figure 4. Constant Current Excitation Connections (V<sub>COMPL</sub> = 0 to +10V)

## APPLICATIONS

**Strain Measurement:** The 2B30 is shown in Figure 5 in a strain measurement system. A single active gage (120Ω, GF = 2) is used in a bridge configuration to detect small changes in gage resistance caused by strain. The temperature compensation is provided by an equivalent dummy gage and two high precision 120Ω resistors complete the bridge. The 2B35 adjustable power supply is set to a low +3V excitation voltage to avoid the self-heating error effects of the gage and bridge elements. System calibration produces a 1V output for an input of 1000 microstrains. The filter cutoff frequency is set at 100Hz.

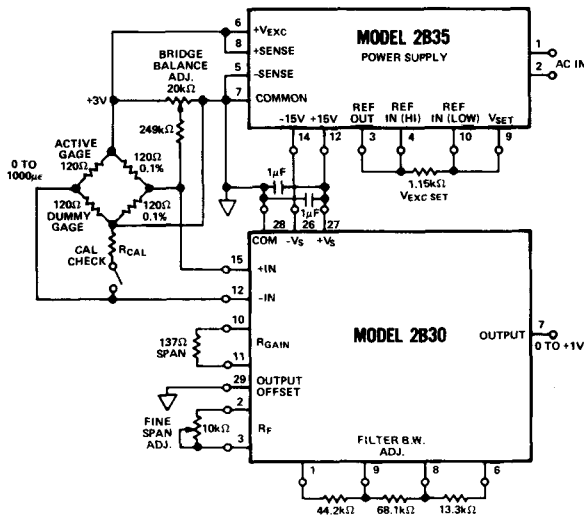


Figure 5. Interfacing Half-Bridge Strain Gage Circuit

**Pressure Transducer Interface:** A strain gage type pressure transducer (BLH Electronics, DHF Series) is interfaced by the 2B31 in Figure 6. The 2B31 supplies regulated excitation (+10V) to the transducer and operates at a gain of 333.3 to achieve 0-10V output for 0-10,000 p.s.i. at the pressure transducer. Bridge Balance potentiometer is used to cancel out any offset which may be present and the Fine Span potentiometer adjustment accurately sets the full scale output. Depressing the calibration check pushbutton switch shunts a system calibration resistor ( $R_{CAL}$ ) across the transducer bridge to give an instant check on system calibration.

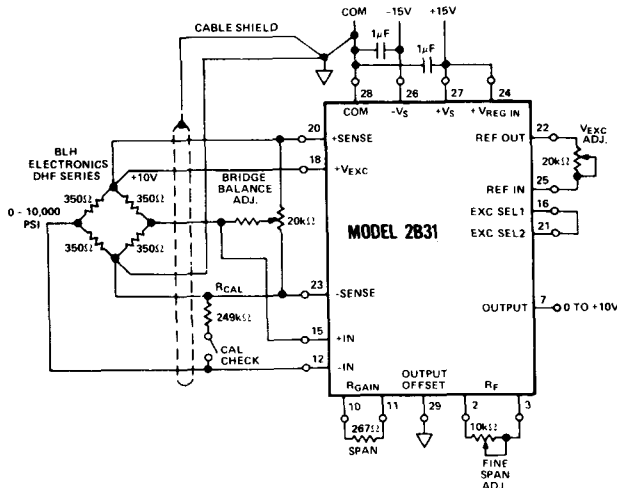


Figure 6. Pressure Transducer Interface Application

**Platinum RTD Temperature Measurement:** In Figure 7 model 2B31 provides complete convenient signal conditioning in a wide range (-100°C to +600°C) RTD temperature measurement system. YSI - Sostman four-wire, 100Ω platinum RTD (PT139AX) is used. The four wire sensor configuration, combined with a constant current excitation and a high input impedance offered by the 2B31, eliminates measurement errors resulting from voltage drops in the lead wires. Offsetting may be provided via the 2B31's offset terminal. The gain is set by the gain resistor for a +10V output at +600°C. Measurement resolution and repeatability is ±0.1°C.

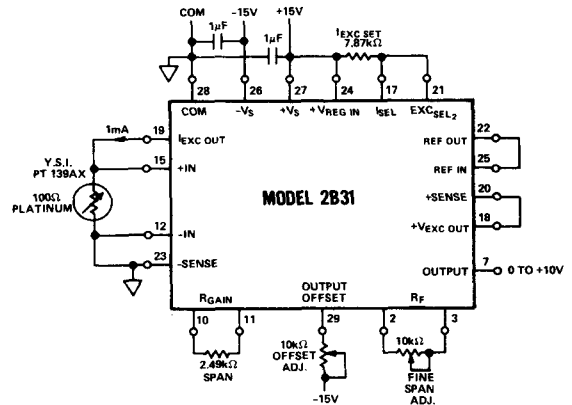


Figure 7. Platinum RTD Temperature Measurement

**Interfacing Three-Wire Sensors:** A bridge configuration is particularly useful to provide offset in interfacing to a platinum RTD and to detect small, fractional sensor resistance changes. Lead compensation is employed, as shown in Figure 8, to maintain high measurement accuracy when the lead lengths are so long that thermal gradients along the RTD leg may cause changes in line resistance. The two completion resistors ( $R_1$ ,  $R_2$ ) in the bridge should have a good ratio tracking (±5ppm/°C) to eliminate bridge error due to drift. The single resistor ( $R_3$ ) in series with the platinum sensor must, however, be of very high absolute stability. The adjustable excitation in the 2B31 controls the power dissipated by the RTD itself to avoid self-heating errors.

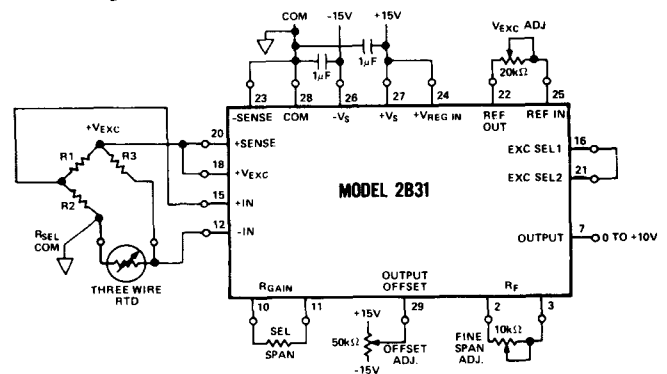


Figure 8. Three-Wire RTD Interface

**Linearizing Transducer Output:** To maximize overall system linearity and accuracy, some strain gage-type and RTD transducer analog outputs may require linearization. A simple circuit may be used with the 2B31 to correct for the curvature in the input signal. Consult factory for the application assistance.

**Data Acquisition System:** Figure 9 shows a typical application of the 2B30/2B31 in a low level, high speed microcomputer based data acquisition system. The advantages of this configuration are improvement in CMR enhanced by a low pass filter/channel provided by the 2B31, elimination of aliasing errors and crosstalk noise between input channels, improvement in system noise and resolution, and optimized, individual bridge excitation source for each channel.

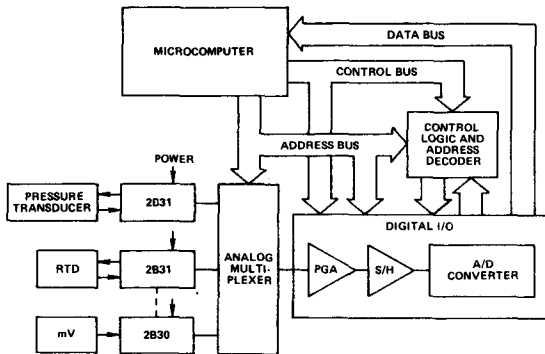


Figure 9. Use of the 2B30/2B31 in Data Acquisition System

### PERFORMANCE CHARACTERISTICS

**Input Offset Voltage Drift:** Models 2B30/2B31 are available in three drift selections:  $\pm 0.5$ ,  $\pm 1$  and  $\pm 3\mu\text{V}/^\circ\text{C}$  (max, RTI,  $G = 1000\text{V}/\text{V}$ ). Total input drift is composed of two sources (input and output stage drifts) and is gain dependent. Figure 10 is a graph of the worst case total voltage offset drift vs. gain for all versions.

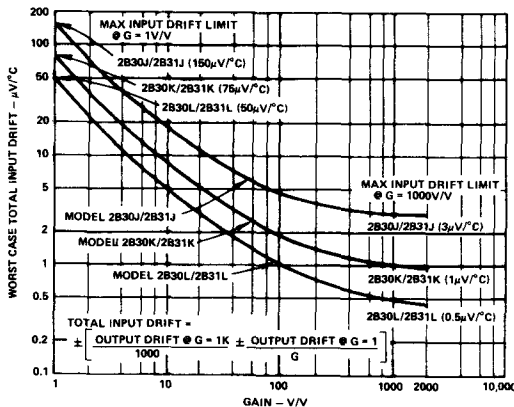


Figure 10. Total Input Offset Drift (Worst Case) vs. Gain

**Gain Nonlinearity and Noise:** Nonlinearity is specified as a percent of full scale (10V), e.g. 0.25mV RTO for 0.0025%. Three maximum nonlinearity selections offered are:  $\pm 0.0025\%$ ,  $\pm 0.005\%$  and  $\pm 0.01\%$  ( $G = 1$  to  $2000\text{V}/\text{V}$ ). Models 2B30/2B31 offer also an excellent voltage noise performance by guaranteeing maximum RTI noise of  $1\mu\text{V}$  p-p ( $G = 1000\text{V}/\text{V}$ ,  $R_S \leq 5\text{k}\Omega$ ) with noise bandwidth reduced to 2Hz by the low pass filter.

**Low Pass Filter:** The three pole Bessel-type active filter attenuates unwanted high-frequency components of the input signal above its cutoff frequency ( $-3\text{dB}$ ) with  $60\text{dB}/\text{decade}$  roll-off. With a 2Hz filter, attenuation of  $70\text{dB}$  at  $60\text{Hz}$  is obtained, settling time is  $600\text{ms}$  to  $0.1\%$  of final value with less than  $1\%$  overshoot response to step inputs. Figure 11 shows the filter response.

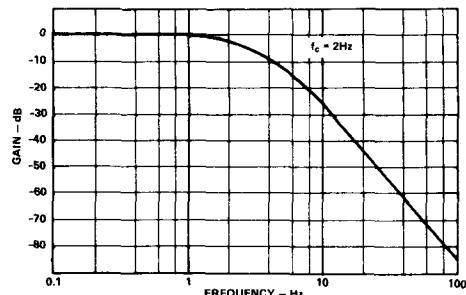


Figure 11. Filter Amplitude Response vs. Frequency

**Common Mode Rejection:** CMR is rated at  $\pm 10\text{V}$  CMV and  $1\text{k}\Omega$  source imbalance. The CMR improves with increasing gain. As a function of frequency, the CMR performance is enhanced by the incorporation of low pass filtering, adding to the  $90\text{dB}$  minimum rejection ratio of the instrumentation amplifier. The effective CMR at  $60\text{Hz}$  at the output of the filter ( $f_c = 2\text{Hz}$ ) is  $140\text{dB}$  min. Figure 12 illustrates a typical CMR vs. Frequency and Gain.

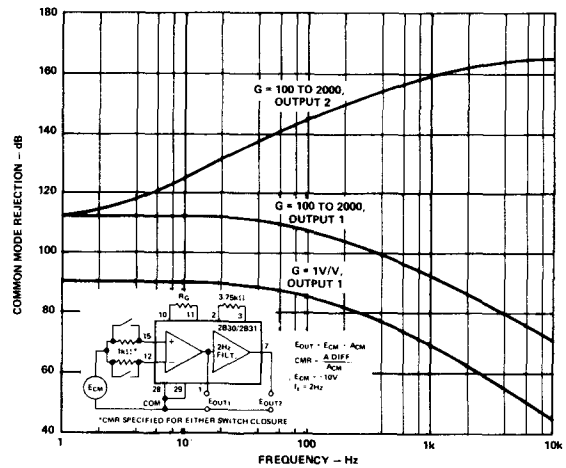


Figure 12. Common Mode Rejection vs. Frequency and Gain

**Bridge Excitation (2B31):** The adjustable bridge excitation is specified to operate over a wide regulator input voltage range ( $+9.5\text{V}$  to  $+28\text{V}$ ). However, the maximum load current is a function of the regulator circuit input-output differential voltage, as shown in Figure 13. Voltage output is short circuit protected and its temperature coefficient is  $\pm 0.015\% \text{V}_{\text{OUT}}/^\circ\text{C}$  max ( $\pm 0.003\% / ^\circ\text{C}$  typ). Output temperature stability is directly dependent on a temperature coefficient of a reference and for higher stability requirements, a precision external reference may be used.

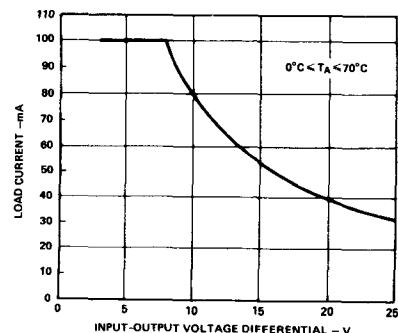


Figure 13. Maximum Load Current vs. Regulator Input-Output Voltage Differential

### FEATURES

**Resistor Programmable Voltage or Current Output**

Voltage: +1V dc to +15V dc @ 125mA max

Current: 100 $\mu$ A to 10mA ( $V_{COMPL} = +10V$ )

**Dual Fixed Output:  $\pm 15V$  dc @  $\pm 65mA$  max**

**Excellent Regulation: Line  $\pm 0.01\%$  max; Load  $\pm 0.02\%$  max**

**Low Drift: 0.006%/ $^{\circ}C$  max (2B35K)**

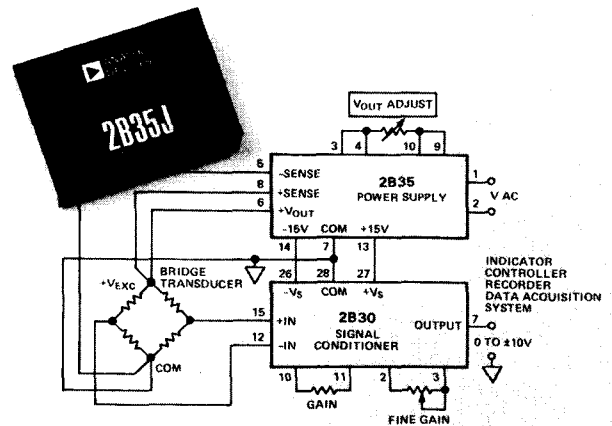
**No Derating Over  $-25^{\circ}C$  to  $+71^{\circ}C$  Operating Range**

### APPLICATIONS

**Measurement and Control Instruments and Systems**

**Excitation Source For:**

Strain Gages, Pressure Transducers, Load Cells,  
Torque Transducers, RTD's



BRIDGE TRANSDUCER SIGNAL CONDITIONING

### GENERAL DESCRIPTION

The 2B35 is a triple output modular power supply designed to provide regulated excitation to a wide variety of transducers as well as  $\pm 15V$  power for amplifiers and other analog circuits of an instrumentation system. The single-resistor programmable transducer excitation output may be operated in two modes: constant voltage, providing a +1V to +15V output or a constant current, adjustable from 100 $\mu$ A to 10mA.

The programmable output in the voltage mode features current rating of 0 to 125mA, suitable to excite four 350 $\Omega$  transducers at 10V. Current limiting protects the output against accidental overload and remote sensing corrects for the transducer cable resistance variations. In the constant current mode, externally set 100 $\mu$ A to 10mA output offers a 0 to +10V compliance voltage range. The  $\pm 15V$  outputs feature 0.5% tracking accuracy and current rating of 0 to  $\pm 65mA$  max.

Two accuracy selections are available offering guaranteed low temperature coefficient; 2B35K: 0.006%/ $^{\circ}C$  max and 2B35J: 0.05%/ $^{\circ}C$  max. Line and load regulation are also guaranteed; 2B35K: 0.01% and 0.02%, and 2B35J: 0.08% and 0.1%, max, respectively.

### APPLICATIONS

The 2B35 is designed for ac powered signal conditioning instrumentation applications used for data acquisition, control, indication or recording. This compact module may be applied as a power source for the model 2B30 strain gage transducer/RTD signal conditioner in a high accuracy transducer interface application. Some typical applications involve strain gages for stress/strain measurements, pressure transducers, load cells, torque transducers and RTD's.

### OPERATION

Figure 1 illustrates operation of the 2B35K providing an adjustable voltage output and dual 15V dc outputs. The resistor programmable output (+V<sub>OUT</sub>) is set between +1V to +15V by the R<sub>TRIM</sub>. R<sub>TRIM</sub> may be determined by using either the table shown in Figure 1 or the graph shown in Figure 2. For example, to provide an adjustable range from +1V to +6V, R<sub>TRIM</sub> should be a 5k $\Omega$  pot.

The remote sensing inputs (pins 5 and 8) are connected at the transducer (load) to the voltage output (SENSE HIGH to +V<sub>OUT</sub> and SENSE LOW to COMMON).

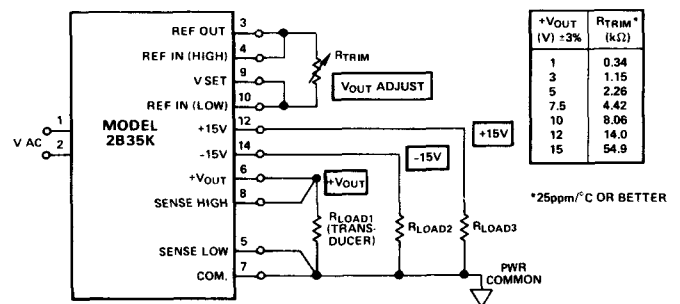


Figure 1. Model 2B35K Connection Diagram for Dual 15V dc and Adjustable +1V to +15V Output



# SPECIFICATIONS

(typical @ +25°C and 115V ac 60Hz unless otherwise noted)

| Model   | 2B35J              | 2B35K  |
|---|--------------------|--------|
| <b>INPUT</b>  |                    |        |
| Input Voltage Range <sup>1</sup>                          | 105V ac to 125V ac | *      |
| Input Frequency Range                                     | 50Hz to 400Hz      | *      |
| <b>ADJUSTABLE OUTPUT</b>                                  |                    |        |
| <b>Voltage Mode</b>                                       |                    |        |
| Output Voltage Range                                      | +1V to +15V dc     | *      |
| Output Voltage Stability                                  |                    |        |
| vs. Temperature - % $V_{OUT}/^{\circ}C$ max               | ±0.05              | ±0.006 |
| vs. Time - % $V_{OUT}/month$                              | ±0.01              | *      |
| Output Current (-25°C to +71°C) <sup>2</sup>              | 0 to 125mA max     | *      |
| Output Impedance - @ dc, max                              | 0.1Ω               | *      |
| Noise and Ripple (dc to 1MHz) - mV p-p max                | 1                  | *      |
| - mV rms max  | 0.25               | *      |
| <b>Regulation</b>   |                    |        |
| Line (full range) - % $V_{OUT}$ max                       | ±0.08              | ±0.01  |
| Load (no load to full load) - % $V_{OUT}$ max             | ±0.1               | ±0.02  |
| Remote Sensing Impedance                                  | 30kΩ               | *      |
| Short Circuit Current Limit <sup>3</sup> (-25°C to +71°C) | 200mA              | *      |
| <b>Current Mode</b>                                       |                    |        |
| Output Current Range                                      | 100μA to 10mA      | *      |
| Output Current Stability                                  |                    |        |
| vs. Temperature - % $I_{OUT}/^{\circ}C$ max               | ±0.05              | ±0.006 |
| vs. Time - % $I_{OUT}/month$                              | ±0.01              | *      |
| Compliance Voltage Range                                  | 0 to +10V          | *      |
| Noise and Ripple (dc to 1MHz) - μA p-p                    | 0.1                | *      |
| Line Regulation (full range) - % $I_{OUT}$ max            | ±0.08              | ±0.01  |
| <b>DUAL FIXED OUTPUTS</b>                                 |                    |        |
| Output Voltage  | ±15V dc            | *      |
| Voltage Error - mV max                                    | -0, +300           | *      |
| Accuracy Tracking (-15V Ref to +15V) - % max              | ±0.5               | *      |
| Stability vs. Temperature - %/ $^{\circ}C$ max            | ±0.02              | ±0.006 |
| Output Current <sup>4</sup>                               | 0 to ±65mA max     | *      |
| Output Impedance - @ dc, max                              | 0.1Ω               | *      |
| Noise and Ripple (dc to 1MHz) - mV p-p                    | 1                  | *      |
| - mV rms  | 0.25               | *      |
| <b>Regulation</b>   |                    |        |
| Line (full range - % max                                  | ±0.08              | ±0.01  |
| Load (no load to full load) - % max                       | ±0.1               | ±0.02  |
| Short Circuit Current Limit <sup>3</sup> (-25°C to +71°C) | ±180mA             | *      |
| <b>INPUT TO OUTPUT ISOLATION</b>                          |                    |        |
| Breakdown Voltage - Continuous, ac or dc                  | ±500V pk max       | *      |
| Isolation Resistance                                      | 50MΩ               | *      |
| <b>TEMPERATURE RANGE</b>                                  |                    |        |
| Operating, Rated Performance                              | -25°C to +71°C     | *      |
| Storage   | -25°C to +85°C     | *      |
| <b>MECHANICAL</b>   |                    |        |
| Case Dimensions - Inches                                  | 2.5 x 3.5 x 1.25   | *      |
| Weight - Grams  | 550                | *      |
| Mating Socket   | AC1212             | *      |

## NOTES

\*Specifications same as model 2B35J.

<sup>1</sup> Optional input voltage ranges: "E" Option; 205-240V ac, 50 to 400Hz  
 "F" Option; 90-110V ac, 50 to 400Hz  
 "H" Option; 220-260V ac, 50 to 400Hz

Order option desired as a suffix to model number.

<sup>2</sup> Maximum output current available over the entire output voltage and temperature range without derating.

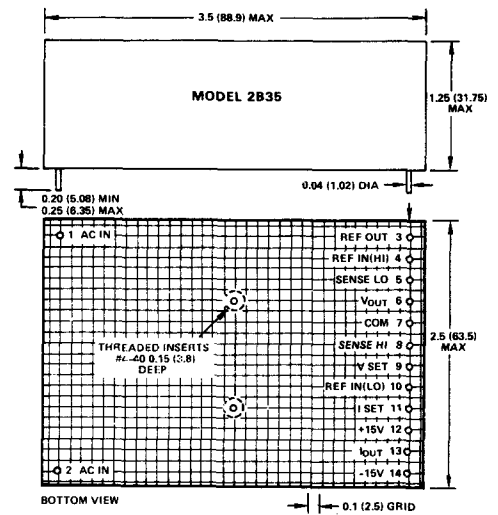
<sup>3</sup> Output protected for continuous short circuit over the temperature range.

<sup>4</sup> Unbalanced load operation is permissible for any combination of  $I_O$  and  $I_{IO}$  which does not exceed a total of 130mA.

Specifications subject to change without notice.

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



## MATING SOCKET: AC1212

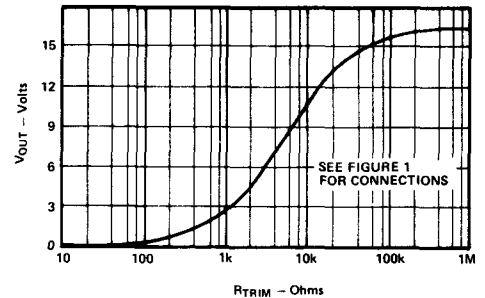


Figure 2. Voltage Output vs.  $R_{TRIM}$

## ADJUSTABLE CURRENT OUTPUT WITH DUAL 15V dc OUTPUTS

Pin connections to provide dual 15V dc and a constant current output are shown in Figure 3. The current output is adjusted from 100μA to 10mA via  $R_{TRIM}$ . The value of programming resistor  $R_{TRIM}$  may be calculated from the relationship:  $R_{TRIM} = 2.46/I_{OUT}$  where  $R_{TRIM}$  is in kΩ and  $I_{OUT}$  in mA.

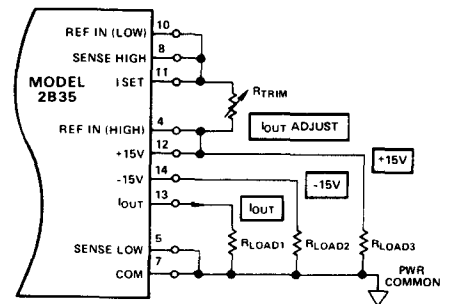


Figure 3. Model 2B35 Connection Diagram to Provide Dual 15V dc and Adjustable 100μA to 10mA Current Output

### FEATURES

- Automatic Scan of 6 Channel Inputs
- Manual Selection of Individual Channel
- External Channel Selection by BCD Code
- $\pm 199.9\text{mV}$  or  $\pm 1.999\text{V}$  dc Full Scale Range
- Isolated Analog Input
- Parallel BCD Output
- Accessible Gain Points for Implementation of Selectable Gain, to 6V dc F.S.
- $\pm 12\text{V}$  dc and  $+5\text{V}$  dc for External Use
- AD2038:** High Accuracy Temperature Measurements Used with AD590 Transducer
- 0.1° Resolution; 6 Channels
- $-55.0^\circ\text{C}$  to  $+150.0^\circ\text{C}$  ( $-67.0^\circ\text{F}$  to  $+199.9^\circ\text{F}$ )

### APPLICATIONS

- AD2037:** Multi-point Measurements for Data Acquisition, Logging and Control
- Data Processing from: Pressure and Flow Transducers; RTD and Thermistor Transducers; AD590 Temperature Transducers; LVDT and Level Transducers; Voltage and Current Sources.
- AD2038:** Temperature Monitoring in Laboratory, Manufacturing, and Quality Control

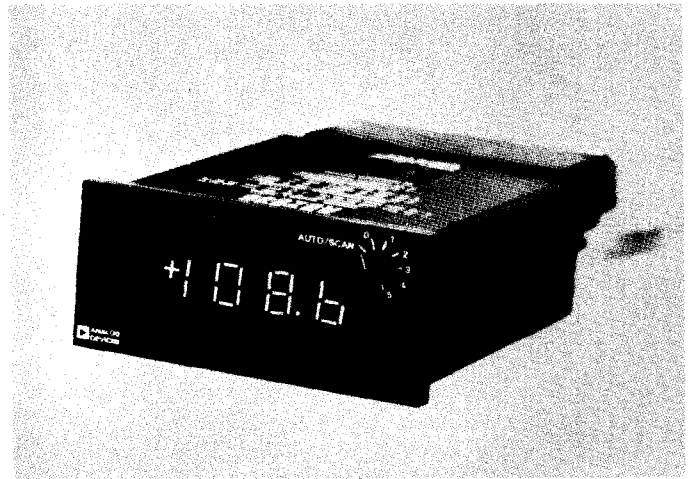
### AD2037 GENERAL DESCRIPTION

The AD2037 is a low cost 3 1/2 digit, ac line powered, 6 channel digital scanning voltmeter designed to interface to printers, computers, serial data transmitters, telephone lines, etc., for display, control, logging or transmission of multi-channel analog data. With appropriate external signal conditioning on each channel, the AD2037 becomes a versatile building block for a broad range of data acquisition, data logging, or control applications.

Channel selection is made via three methods: manual, using the switch provided on the front; Auto/Scan, where the AD2037 cycling on an internal clock can continually scan the 6 input channels; or External selection, where control inputs provided on the rear connector enables channel selection via external BCD code.

### AD2038 GENERAL DESCRIPTION

The AD2038 is a dedicated 6 channel digital scanning thermometer. Based on the AD2037 and designed to be used in conjunction with Analog Devices' AD590 Temperature Transducer, the AD2038 retains all of the input/output features of the AD2037 as well as the channel selection methods.

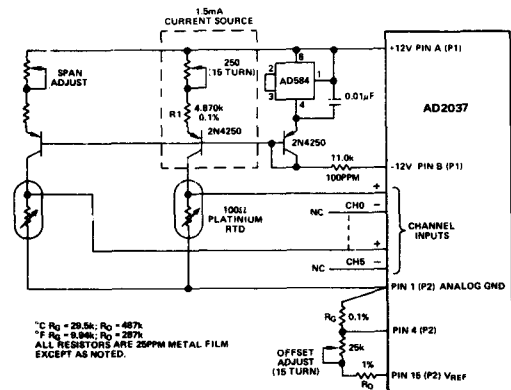


The AD2038 and AD590 will measure and display temperatures to  $\pm 1.3^\circ\text{C}$  accuracy over the temperature range of  $-55.0^\circ\text{C}$  to  $+150.0^\circ\text{C}$  ( $-67.0^\circ\text{F}$  to  $200.0^\circ\text{F}$ ), over limited temperature ranges around a calibration point, accuracies approach a few tenths of a degree.

### RTD THERMOMETER

The figure below shows a 3 wire, 0.1° resolution, nonlinearized RTD circuit. For many applications where repeatability is required linearization is not necessary. The transistor, resistor (R1) and potentiometer on each Channel form a 1.5mA current source.

This current through the RTD resistive element is converted to a voltage which is proportional to absolute temperature and measured by the AD2037. Conversion from absolute temperature to  $^\circ\text{C}$  or  $^\circ\text{F}$  requires an offset which is produced by the reference of the AD2037 and  $R_0$ .



*RTD Thermometer*

# SPECIFICATIONS (typical @ +25°C and nominal power supply voltage)

## DISPLAY OUTPUT

- Light emitting diode (LED), seven segment display readouts, 0.5" (13mm) high for 3 data digits, 100% overrange and polarity indication. Overload indicated by flashing display, polarity remains valid. There is no indication of out of sensor range on AD2038.
- Decimal Points (3) Selectable at Input Connector
- Display Blanking
- Sensor Disconnect Indication same as overload.

## ANALOG INPUT

- Opto/Transformer Isolated
- Configuration: Differential, isolated
- ±1.999V dc and ±199.9mV dc Full Scale Range
- Full Scale Range Programmable to 6V dc
- Input Impedance: 250MΩ
- Bias Current: 1.5nA
- Overvoltage Protection: (Continuous Without Damage)  
Normal Mode: ±30V pk  
Channel to Channel: ±30V pk

## ACCURACY

### AD2037

- ±0.05% Reading ±1 digit<sup>1</sup>
- Resolution: Programmable
- Temperature Range: 0 to +50°C operating; -25°C to +85°C storage
- Temperature Coefficient: Gain: 50ppm/°C  
Zero: 1.5μV/°C
- Warm-up Time to Rated Accuracy: Less than 5 minutes
- Settling Time to Rated Accuracy: 0.6 seconds (- full scale to + full scale)
- Max Voltage Between Channels: ±199.9mV FS; ±6.1V pk  
±1.999V FS; ±2.5V pk

### AD2038

- Resolution 0.1°
- Range -55°C to +150°C  
-67°F to +200°F
- Accuracy: (±0.1° digitizing error)<sup>2</sup>

|   | AD590J      | AD590K     | AD590L     | AD590M     |
|---|-------------|------------|------------|------------|
| Sensor calibrated at +25°C (over range) | ±3.2°C max  | ±2.2°C max | ±1.8°C max | ±1.2°C max |
| Uncalibrated Error at +25°C             | ±5.2°C max  | ±2.7°C max | ±1.2°C max | ±0.7°C max |
| Uncalibrated Error (over range)         | ±10.2°C max | ±5.7°C max | ±3.2°C max | ±1.9°C max |
| Nonlinearity (over range)               | ±1.7°C max  | ±1.0°C max | ±0.6°C max | ±0.5°C max |

- Temperature Coefficient: Span: 50ppm/°C  
Offset: 0.01 degrees/degree

## NORMAL MODE REJECTION

- 50dB at 50 - 60Hz (Additional capacitor filtering may be added between pins A and 4 with degradation of response time)

## COMMON MODE REJECTION

- Floated on Power Supply: 120dB at 250V rms max CMV, dV<sub>cm</sub>/dt 10<sup>6</sup>V/sec max, 1kΩ Imbalance

## CONVERSION RATE

- 5 Conversion/sec
- Hold and Read on Command

## POWER INPUT

- AC Line 50 - 400Hz, see Voltage Options Below
- Power Consumption - 5.8W @ 50 - 400Hz

## ANALOG OUTPUTS

- ±12V dc ±10% @ 10mA (Referenced to Isolation Analog Grd.)
- +5V dc ±5% @ 30mA
- Reference Voltage +6.4V ±1% (Referred to Analog Grd.) 25ppm/°C @ 50μA max output

## DATA OUTPUTS

**Isolated Parallel BCD Outputs** - 3 BCD digits, overrange, overload outputs (TTL Compatible, 4 TTL Loads). BCD data outputs are latched positive true logic. Overload output is Logic "0" for inputs greater than full scale range. Logic "1" when other data outputs are valid. Polarity output (TTL compatible, 4 TTL Loads latched) indicates positive polarity when high (Logic "1"). Digital outputs are fully isolated from input circuitry; all Logic levels reference to digital ground.

**Channel Address Outputs (CMOS/TTL Compatible 2 TTL Loads)** - BCD Channel number data outputs are positive true.

**Mode Output (CMOS/TTL Compatible 2 TTL Loads)** - Logic "1" indicates channel selection is by switch. Logic "0" indicates selection is by scanner or external control, useful in Microcomputer Interface.

**Data Ready (Data Ready) CMOS/TTL Compatible 2 TTL Loads** - Logic "1" ("0") indicates data from Scan Card is ready. Data remains valid until next clock pulse.

**Spare Inverter Output (CMOS/TTL Compatible 2 TTL Loads)** - Spare inverter supplied for customer convenience.

**Clock Out (CMOS/TTL Compatible, 2 TTL Loads)** - Indicates EOC. When clock pulse is high, latches are being updated, data is invalid. Data is valid on negative going edge for 198ms. Clock Out pulse is disabled when Data Hold line is low.

## ANALOG OUTPUT (P2 Pin A): 1mA max output

- AD2037:  $V_O = K V_{IN}$   
Where K is gain of programmable input amplifier. (K = 1 for 1.999V F.S. and K = 10 for 199.9mV)
- AD2038:  $V_O = (18.95mV/°C)T$  for T = °C  
 $V_O = (10.53mV/°F)(T-32)$  for T = °F  
error = ±6mV

## CONTROL INPUTS

**Display Blanking (TTL Compatible, 3 LSTTL Load)** - Logic "0" or grounding blanks entire display except for decimal points; Logic "1" or open circuit for normal operation. Display blanking has no effect on output data. Display is valid immediately upon removal of blanking input.

**Converter Hold (CMOS/TTL Compatible, 1 LSTTL Load)** - Logic "0" or grounding causes DPM to cease conversions and display data from last conversion; Logic "1" or open circuit for normal operation. After "Converter Hold" is removed, one or two conversions are needed before reading and BCD are valid.

**Decimal Points (Not TTL Compatible)** - Logic "0" or grounding illuminates desired decimal point. External drive circuitry must sink 35mA peak at a 25% duty cycle, when decimal point is illuminated.

**Data Hold (TTL Compatible, 1 TTL Load)** - Logic "0" inhibits updating of latched parallel output data. Logic "1" or open circuit allows data to be updated after each DPM conversion. This input has no effect on normal conversion of the DPM and its display.

**Scanner Enable (CMOS/TTL Compatible 1 LSTTL Load)** - Logic "1" will enable Scanner to control the channel selection. External channel input BCD lines can remain connected. A Logic "0" enables external channel selection.

**Scan (Scan) (CMOS/TTL Compatible, 1 LSTTL Load)** - A Logic "1" ("0") for <4 seconds will initiate a scan of six channels. To use Scan input, the Scan input must be a Logic "0". Both inputs have debounce circuitry. A momentary scan pulse while in the switch or external mode will initiate a sequence of six readings of the channel that is addressed then stop.

**Channel Address Input (CMOS/TTL Compatible 1 LSTTL Load)** - Logic "0" on Scanner Enable will allow use of external control. All other control inputs remain the same.

**Channel Address Increment (CMOS/TTL Compatible 1 LSTTL Load)** - Positive going edge will initiate sequence to the next channel.

**Spare Inverter Input (CMOS/TTL Compatible 1 LSTTL Load)** - Spare inverter supplied for customer convenience.

## CALIBRATION ADJUSTMENTS

- Gain
- Offset, Course
- Offset, Fine
- Span/per Channel (AD2038 only)
- Recommended Recalibration Interval: Six Months

## SIZE

- 3.92" x 1.67" H x 5.80" D (100 x 42 x 147mm)
- Panel Cutout 3.930" x 1.682" (99.8 x 42.7mm)

## WEIGHT

- 1.25 pounds (0.563 kg)

## OPTIONS<sup>3</sup>

- AD2037 Lens: 28 Red with ADI Logo  
Lens: 27 Red without ADI Logo
- AD2038 Lens 22-1, Red °C with ADI Logo  
Lens 22-2, Red °F with ADI Logo  
Lens 23-1, Red °C without ADI Logo  
Lens 23-2, Red °F without ADI Logo

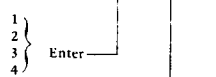
## CONNECTORS (2)

2 each, 30 pin, 0.156" Spacing Card Edge Connector  
Viking 2VK 15/1-2 or Equivalent  
Optional: Order AC1501

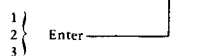
## ORDERING GUIDE

AD2037 or AD2038 -

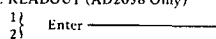
### POWER INPUT<sup>4</sup>



### SCAN RATE<sup>4</sup>



### TEMPERATURE SCALE READOUT (AD2038 Only)<sup>4</sup>



## Notes:

- <sup>1</sup> Guaranteed at 200mV full scale at +25°C and nominal power supply.
- <sup>2</sup> Overall accuracy of meter plus sensor over entire sensor range (guaranteed max) Meter is factory calibrated for ideal sensor.
- <sup>3</sup> Lens 22 (AD2038) Lens 28 (AD2037) supplied if no lens option is specified.
- <sup>4</sup> Only one option may be specified.

Specifications subject to change without notice.

### FEATURES

#### Low Cost

Accuracy to  $\pm 1.0^\circ \pm 1$  Digit

Temperature Range:  $-55^\circ\text{C}$  to  $+150^\circ\text{C}$   
 $-67^\circ\text{F}$  to  $+302^\circ\text{F}$   
 $218^\circ\text{K}$  to  $423^\circ\text{K}$   
 $425^\circ\text{R}$  to  $793^\circ\text{R}$

$^\circ\text{C}$ ,  $^\circ\text{F}$ ,  $^\circ\text{K}$  or  $^\circ\text{R}$  Readout

Single +5V Supply

Terminal Block Interface

Small Size, Panel Mount

### APPLICATIONS

Temperature Monitoring in Design, Laboratory,  
 Manufacturing and Quality Control



### GENERAL DESCRIPTION

The AD2040 is a low cost 3 digit temperature indicator. Based on the highly successful AD2026, low cost DPM, and designed to be used in conjunction with Analog Devices' AD590 temperature transducer, the AD2040 reads out directly in  $^\circ\text{C}$ ,  $^\circ\text{F}$ ,  $^\circ\text{K}$  or  $^\circ\text{R}$ . A precision voltage reference, resistor network and span and zero adjusts needed to implement display of the different temperature scales are all self contained. User selectable degree readout, as well as all other connections, ie. +5V power and AD590 interface are all made via the terminal block on the rear. If required, calibration adjustments are easily accessible. No mounting hardware of any kind is used. The AD2040 occupies less than 1 1/2" of space behind the panel.

The AD2040 and AD590 will measure and display temperatures from  $-55^\circ\text{C}$  to  $150^\circ\text{C}$  ( $-67^\circ\text{F}$  to  $302^\circ\text{F}$ ) with accuracy to  $\pm 1.0^\circ \pm 1$  digit. The display, converter, signal conditioning and sensor are all powered from a single +5V supply. Reliability is assured with the inherent simplicity and accuracy of the sensor combined with the highly efficient design of the AD2040.

### THE SENSOR

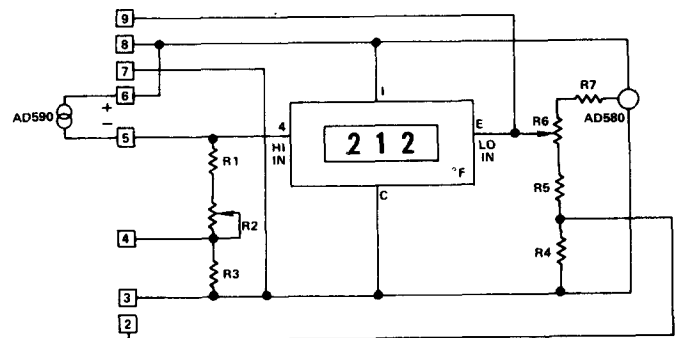
The AD590 is a laser calibrated, two terminal IC Temperature Sensor. Its output is a current ( $1\mu\text{A}$  per  $^\circ\text{K}$ ) linearly proportional to absolute temperature thus eliminating the need for linearization and cold junction compensation.

Due to the AD590's high impedance current output, it is insensitive to voltage drops over long lines thus enabling remote monitoring with no need for costly transmitters or special wire.

For normal applications the AD590J can be used and calibrated at a single temperature point. Where better linearity or sensor interchangeability is needed, the "K" and "L" versions are

available. All versions are available to MIL-STD-883A Class B processing.

The TO-52 may be mounted as is, or inserted in an appropriate probe. More detailed sensor information is available on the AD590 Data Sheet.



Block Diagram

Above is a block diagram of the AD2040, showing the AD2026 DPM, the current-to-voltage conversion resistors (R1, R2, R3), the offsetting resistance network (R4, R5, R6, R7), and the connections to the terminal strip. Attenuated voltage from the AD580, 2.5V reference, provides the offsets for readout on the F and C scales. Jumpers are connected by the user at the terminal strip to select the appropriate units of temperature for display.

# SPECIFICATIONS

(typical @ +25°C and nominal supply unless otherwise specified)

## ACCURACY

- Resolution: 1°
- Range: -55°C to +150°C  
-67°F to 320°F  
218°K to 423°K  
425°R to 793°R
- Accuracy: (±1 digit)<sup>1</sup>
  - With Calibration at 25°C
  - Uncalibrated Error at 25°C
  - Uncalibrated Error Over Range
  - Nonlinearity over Range

|  | <u>AD590J</u> | <u>AD590K</u> | <u>AD590L</u> | <u>AD590M</u> |
|--|---------------|---------------|---------------|---------------|
|  | ±3.2°C max    | ±2.2°C max    | ±1.8°C max    | ±1.2°C max    |
|  | ±5.2°C max    | ±2.7°C max    | ±1.2°C max    | ±0.7°C max    |
|  | ±10.2°C max   | ±5.7°C max    | ±3.2°C max    | ±1.9°C max    |
|  | ±1.7°C max    | ±1.0°C max    | ±0.6°C max    | ±0.5°C max    |

## DISPLAY OUTPUT

- 7 Segment, LED 0.5" (13mm) High for 3 Data Digits
- Sensor Disconnect Indication: ---- (for °C and °F only)
- DPM Positive Overload: EEE
- DPM Negative Overload: ----
- No Indication of Out of Sensor Range
- Temperature Coefficient:
  - Offset: 0.03 degrees/degree
  - Span: 70ppm/°C

## SIZE

- 3.43" W x 2.0" H x 1.65" D (87 x 52 x 42mm)
- Panel Cutout Required: 3.175 ± 0.015" x 1.810 ± 0.015" (80.65 ± 0.38 x 45.97 ± 0.38mm)

## WEIGHT

- 3 ounces (88 grams)

## INPUT IMPEDANCE

- °C, °K: 1.0K
- °F, °R: 1.8K

## CONVERSION RATE

- 4 Conversions Per Second

## POWER INPUT

- +5.0V ±5%; 160mA Avg.

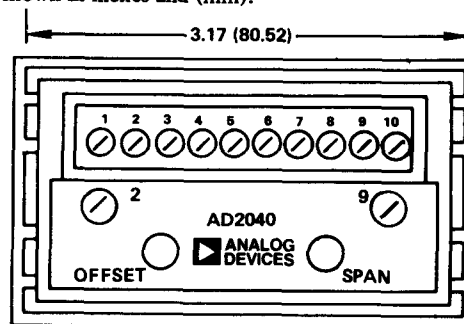
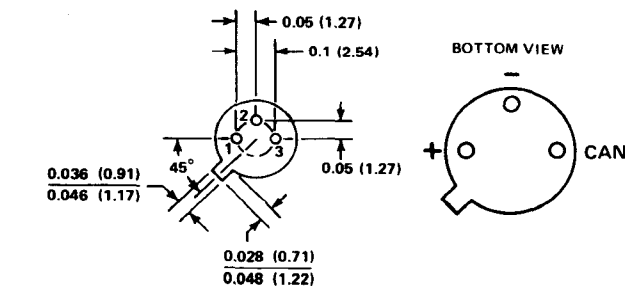
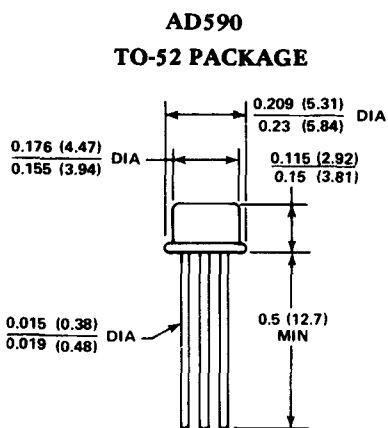
## CALIBRATION ADJUSTMENT

- Span
- Gain
- Zero
- Offset
- Recommended Recalibration Interval: Six Months

<sup>1</sup> Overall accuracy of meter plus sensor over entire range (guaranteed max). Specifications subject to change without notice.

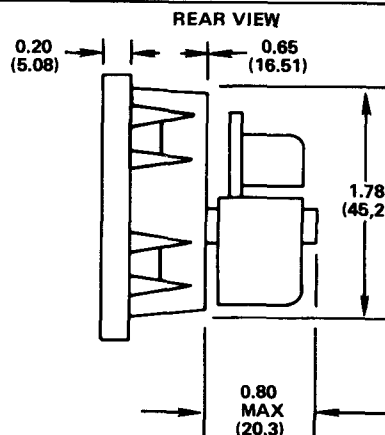
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



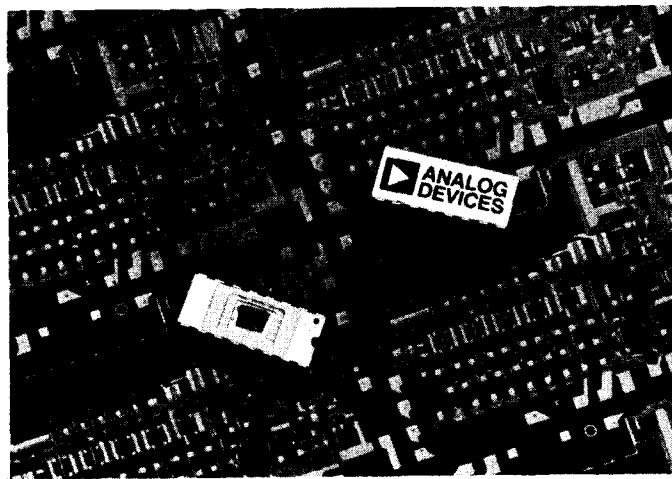
## AD2040

- N.C.
- °F Offset Scaling
- Signal GND
- °F Gain Scaling
- Sensor
- + Sensor
- Power GND
- +5V
- Offset Calibration
- N.C.



**FEATURES**

**Low Cost**  
**Complete Current Output Converter**  
**High Stability Buried Zener Reference**  
**Laser Trimmed to High Accuracy (1/4LSB Max Error, AD561K, T)**  
**Trimmed Output Application Resistors for 0 to +10,  $\pm 5$  Volt Ranges**  
**Fast Settling – 250ns to 1/2LSB**  
**Guaranteed Monotonicity Over Full Operating Temperature Range**  
**TTL/DTL and CMOS Compatible (Positive True Logic)**  
**Single Chip Monolithic Construction**  
**Hermetically-Sealed Ceramic DIP (All Grades)**

**PRODUCT DESCRIPTION**

The AD561 is an integrated circuit 10-bit digital-to-analog converter combined with a high stability voltage reference fabricated on a single monolithic chip. Using 10 precision high-speed current-steering switches, a control amplifier, voltage reference, and laser-trimmed thin-film SiCr resistor network, the device produces a fast, accurate analog output current. Laser trimmed output application resistors are also included to facilitate accurate, stable current-to-voltage conversion; they are trimmed to 0.1% accuracy, thus eliminating external trimmers in many situations.

Several important technologies combine to make the AD561 the most accurate and most stable 10-bit DAC available. The low temperature coefficient, high stability thin-film network is trimmed at the wafer level by a fine resolution laser system to 0.01% typical linearity. This results in an accuracy specification of  $\pm 1/4$ LSB max for the K and T versions, and 1/2LSB max for the J and S versions.

The AD561 also incorporates a low noise, high stability subsurface zener diode to produce a reference voltage with excellent long term stability and temperature cycle characteristics which challenge the best discrete zener references. A temperature compensation circuit is laser-trimmed to allow custom correction of the temperature coefficient of each device. This results in a typical full-scale temperature coefficient of 15ppm/ $^{\circ}$ C; the T.C. is tested and guaranteed to 30ppm/ $^{\circ}$ C max for the K and T versions, 60ppm/ $^{\circ}$ C max for the S, and 80ppm/ $^{\circ}$ C for the J.

All grades are packaged in a 16-pin hermetically-sealed ceramic dual-in-line package. The AD561J and K versions are specified for operation over the 0 to +70 $^{\circ}$ C temperature range, the AD561S and T for operation over the full military temperature range from -55 $^{\circ}$ C to +125 $^{\circ}$ C.

**PRODUCT HIGHLIGHTS**

1. Advanced monolithic processing and laser trimming at the wafer level have made the AD561 the most accurate 10-bit converter available while keeping costs consistent with large volume integrated circuit production. The AD561K and T have 1/4LSB max relative accuracy and 1/2LSB max differential nonlinearity. The low T.C. R-2R ladder guarantees that all AD561 units will be monotonic over the entire operating temperature range.
2. Digital system interfacing is simplified by the use of a positive true straight binary code. The digital input voltage threshold is a function of the positive supply level; connecting  $V_{CC}$  to the digital logic supply automatically sets the threshold to the proper level for the logic family being used. Logic sink current requirement is only 25 $\mu$ A.
3. The high speed current steering switches are designed to settle in less than 250ns for the worst case digital code transition. This allows construction of successive-approximation A/D converters in the 3 to 5 $\mu$ s range.
4. The AD561 has an output voltage compliance range from -2 to +10 volts, thus allowing direct current-to-voltage conversion with just an output resistor, omitting the op amp. The 40M $\Omega$  open collector output impedance results in negligible errors due to output leakage currents.
5. Every AD561 is subjected to long term stabilization bakes and temperature cycled ten times from -65 $^{\circ}$ C to +150 $^{\circ}$ C prior to final test to insure reliability and long-term stability.

# SPECIFICATIONS

( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = +5\text{V}$ ,  $V_{EE} = -15\text{V}$ , unless otherwise specified)

| MODEL  | AD561J       |  |                     | AD561K               |  |     | UNITS                         |  |
|--|--------------|--|---------------------|----------------------|--|-----|-------------------------------|--|
|  | MIN          | TYP  | MAX                 | MIN                  | TYP  | MAX |                               |  |
| RESOLUTION   | 10 Bits      |  |                     | 10 Bits              |  |     |                               |  |
| ACCURACY (Error Relative to Full Scale)                            |              | $\pm 1/4$<br>(0.025)                       | $\pm 1/2$<br>(0.05) | $\pm 1/8$<br>(0.012) | $\pm 1/4$<br>(0.025)                       |     | LSB<br>% of F.S.              |  |
| DIFFERENTIAL NONLINEARITY  |              | $\pm 1/2$                                  |                     | $\pm 1/4$            | $\pm 1/2$                                  |     | LSB                           |  |
| DATA INPUTS  |              |  |                     |                      |  |     |                               |  |
| TTL, $V_{CC} = +5\text{V}$   |              |  |                     |                      |  |     |                               |  |
| Bit ON Logic "1"   | +2.0         |  |                     | *                    |  |     | V                             |  |
| Bit OFF Logic "0"  |              |  | +0.8                |                      | *  |     | V                             |  |
| CMOS, $10\text{V} \leq V_{CC} \leq 16.5\text{V}$<br>(See Figure 1) |              |  |                     |                      |  |     |                               |  |
| Bit ON Logic "1"   | 70% $V_{CC}$ |  |                     | *                    |  |     | V                             |  |
| Bit OFF Logic "0"  |              |  | 30% $V_{CC}$        |                      | *  |     | V                             |  |
| Logic Current (Each Bit) ( $T_{\min}$ to $T_{\max}$ )              |              |  |                     |                      |  |     |                               |  |
| Bit ON Logic "1"   |              | +5   | +100                | *                    | *  |     | nA                            |  |
| Bit OFF Logic "0"  |              | -5   | -25                 | *                    | *  |     | $\mu\text{A}$                 |  |
| OUTPUT   |              |  |                     |                      |  |     |                               |  |
| Current  |              |  |                     |                      |  |     |                               |  |
| Unipolar   | 1.5          | 2.0  | 2.4                 | *                    | *  | *   | mA                            |  |
| Bipolar  | $\pm 0.75$   | $\pm 1.0$                                  | $\pm 1.2$           | *                    | *  | *   | mA                            |  |
| Resistance (Exclusive of Application Resistors)                    |              |  |                     |                      |  |     |                               |  |
| Unipolar Zero (All Bits OFF)                                       |              | 40M  |                     |                      | *  |     | $\Omega$                      |  |
| Capacitance  |              | 25   | 0.05                |                      | *  | *   | % of F.S.                     |  |
| Compliance Voltage   | -2           | -3   | +10                 | *                    | *  | *   | pF<br>V                       |  |
| SETTLING TIME TO 1/2LSB  |              |  |                     |                      |  |     |                               |  |
| All Bits ON-to-OFF or OFF-to-ON                                    |              | 250  |                     |                      | *  |     | ns                            |  |
| POWER REQUIREMENTS   |              |  |                     |                      |  |     |                               |  |
| $V_{CC}$ , +4.5V dc to +16.5V dc                                   |              | 8  | 10                  |                      | *  | *   | mA                            |  |
| $V_{EE}$ , -10.8V dc to -16.5V dc                                  |              | 12   | 16                  |                      | *  | *   | mA                            |  |
| POWER SUPPLY GAIN SENSITIVITY                                      |              |  |                     |                      |  |     |                               |  |
| $V_{CC}$ , +4.5V dc to +16.5V dc                                   |              | 2  | 10                  |                      | *  | *   | ppm of F.S./%                 |  |
| $V_{EE}$ , -10.8V dc to -16.5V dc                                  |              | 4  | 25                  |                      | *  | *   | ppm of F.S./%                 |  |
| TEMPERATURE RANGE  |              |  |                     |                      |  |     |                               |  |
| Operating  |              | 0 to +70                                   |                     |                      | *  | *   | $^\circ\text{C}$              |  |
| Storage  |              | -65 to +150                                |                     |                      | *  | *   | $^\circ\text{C}$              |  |
| TEMPERATURE COEFFICIENTS   |              |  |                     |                      |  |     |                               |  |
| With Internal Reference  |              |  |                     |                      |  |     |                               |  |
| Unipolar Zero  |              | 1  | 10                  |                      | 1  | 5   | ppm of F.S./ $^\circ\text{C}$ |  |
| Bipolar Zero   |              | 2  | 20                  |                      | 2  | 10  | ppm of F.S./ $^\circ\text{C}$ |  |
| Full Scale   |              | 15   | 80                  |                      | 15   | 30  | ppm of F.S./ $^\circ\text{C}$ |  |
| Differential Nonlinearity  |              | 2.5  |                     |                      | 2.5  |     | ppm of F.S./ $^\circ\text{C}$ |  |
| MONOTONICITY   |              |  |                     |                      |  |     |                               |  |
|  |              | Guaranteed over full operating temp. range |                     |                      | Guaranteed over full operating temp. range |     |                               |  |
| PROGRAMMABLE OUTPUT  |              |  |                     |                      |  |     |                               |  |
| RANGES (See Figs. 5, 6)  |              | 0 to +10                                   |                     |                      | *  |     | V                             |  |
|  |              | -5 to +5                                   |                     |                      | *  |     | V                             |  |
| CALIBRATION ACCURACY   |              |  |                     |                      |  |     |                               |  |
| Full Scale Error with Fixed 25 $\Omega$ Resistor                   |              |  |                     |                      |  |     |                               |  |
| Bipolar Zero Error with Fixed 10 $\Omega$ Resistor                 |              | $\pm 0.1$                                  |                     |                      | *  |     | % of F.S.                     |  |
| Full Scale Error with Fixed 10 $\Omega$ Resistor                   |              | $\pm 0.1$                                  |                     |                      | *  |     | % of F.S.                     |  |
| CALIBRATION ADJUSTMENT   |              |  |                     |                      |  |     |                               |  |
| RANGE  |              |  |                     |                      |  |     |                               |  |
| Full Scale (With 50 $\Omega$ Trimmer)                              |              | $\pm 0.5$                                  |                     |                      | *  |     | % of F.S.                     |  |
| Bipolar Zero (With 20 $\Omega$ Trimmer)                            |              | $\pm 0.2$                                  |                     |                      | *  |     | % of F.S.                     |  |

\*Specifications same as AD561J specs.  
Specifications subject to change without notice.

| MODEL  | AD561S              |  |                     | AD561T  |  |                 | UNITS            |
|--|---------------------|--|---------------------|---------|--|-----------------|------------------|
|  | MIN                 | TYP  | MAX                 | MIN     | TYP  | MAX             |                  |
| RESOLUTION   | 10 Bits             |  |                     | 10 Bits |  |                 |                  |
| ACCURACY (Error Relative to Full Scale)                          |                     | ±1/4<br>(0.025)                            | ±1/2<br>(0.05)      |         | ±1/8<br>(0.012)                            | ±1/4<br>(0.025) | LSB<br>% of F.S. |
| DIFFERENTIAL NONLINEARITY  |                     | ±1/2                                       |                     |         | ±1/4                                       |                 | LSB              |
| DATA INPUTS  |                     |  |                     |         |  |                 |                  |
| TTL, V <sub>CC</sub> = +5V                                       |                     |  |                     |         |  |                 |                  |
| Bit ON Logic "1"   | +2.0                |  |                     | **      |  |                 | V                |
| Bit OFF Logic "0"  |                     |  | +0.8                |         |  | **              | V                |
| CMOS, 10V ≤ V <sub>CC</sub> ≤ 16.5V<br>(See Figure 1)            |                     |  |                     |         |  |                 |                  |
| Bit ON Logic "1"   | 70% V <sub>CC</sub> |  |                     | **      |  |                 | V                |
| Bit OFF Logic "0"  |                     |  | 30% V <sub>CC</sub> |         |  | **              | V                |
| Logic Current (Each Bit) (T <sub>min</sub> to T <sub>max</sub> ) |                     |  |                     |         | **   | **              | nA               |
| Bit ON Logic "1"   |                     | +20  | +100                |         | **   | **              | μA               |
| Bit OFF Logic "0"  |                     | -25  | -100                |         | **   | **              |                  |
| OUTPUT   |                     |  |                     |         |  |                 |                  |
| Current  |                     |  |                     |         |  |                 |                  |
| Unipolar   | 1.5                 | 2.0  | 2.4                 | **      | **   | **              | mA               |
| Bipolar  | ±0.75               | ±1.0                                       | ±1.2                | **      | **   | **              | mA               |
| Resistance (Exclusive of Application Resistors)                  |                     | 40M  |                     |         | **   |                 | Ω                |
| Unipolar Zero (All Bits OFF)                                     |                     | 0.01                                       | 0.05                |         | **   | **              | % of F.S.        |
| Capacitance  |                     | 25   |                     |         | **   |                 | pF               |
| Compliance Voltage   | -2                  | -3   | +10                 | **      | **   | **              | V                |
| SETTLING TIME TO 1/2LSB  |                     |  |                     |         | **   |                 | ns               |
| All Bits ON-to-OFF or OFF-to-ON                                  |                     | 250  |                     |         |  |                 |                  |
| POWER REQUIREMENTS   |                     |  |                     |         |  |                 |                  |
| V <sub>CC</sub> , +4.5V dc to +16.5V dc                          |                     | 8  | 10                  |         | **   | **              | mA               |
| V <sub>EE</sub> , -10.8V dc to -16.5V dc                         |                     | 12   | 16                  |         | **   | **              | mA               |
| POWER SUPPLY GAIN SENSITIVITY                                    |                     |  |                     |         |  |                 |                  |
| V <sub>CC</sub> , +4.5V dc to +16.5V dc                          |                     | 2  | 10                  |         | **   | **              | ppm of F.S./°C   |
| V <sub>EE</sub> , -10.8V dc to -16.5V dc                         |                     | 4  | 25                  |         | **   | **              | ppm of F.S./°C   |
| TEMPERATURE RANGE  |                     |  |                     |         |  |                 |                  |
| Operating  |                     | -55 to +125                                |                     |         | **   | **              | °C               |
| Storage  |                     | -65 to +150                                |                     |         | **   | **              | °C               |
| TEMPERATURE COEFFICIENTS   |                     |  |                     |         |  |                 |                  |
| With Internal Reference  |                     |  |                     |         |  |                 |                  |
| Unipolar Zero  |                     | 1  | 10                  |         | 1  | 5               | ppm of F.S./°C   |
| Bipolar Zero   |                     | 2  | 20                  |         | 2  | 10              | ppm of F.S./°C   |
| Full Scale   |                     | 15   | 60                  |         | 15   | 30              | ppm of F.S./°C   |
| Differential Nonlinearity  |                     | 2.5  |                     |         | 2.5  |                 | ppm of F.S./°C   |
| MONOTONICITY   |                     | Guaranteed over full operating temp. range |                     |         | Guaranteed over full operating temp. range |                 |                  |
| PROGRAMMABLE OUTPUT RANGES (See Figs. 5, 6)                      |                     | 0 to +10<br>-5 to +5                       |                     |         | **<br>**                                   |                 | V<br>V           |
| CALIBRATION ACCURACY   |                     |  |                     |         |  |                 |                  |
| Full Scale Error with Fixed 25Ω Resistor                         |                     | ±0.1                                       |                     |         | **   |                 | % of F.S.        |
| Bipolar Zero Error with Fixed 10Ω Resistor                       |                     | ±0.1                                       |                     |         | **   |                 | % of F.S.        |
| CALIBRATION ADJUSTMENT RANGE                                     |                     |  |                     |         |  |                 |                  |
| Full Scale (With 50Ω Trimmer)                                    |                     | ±0.5                                       |                     |         | **   |                 | % of F.S.        |
| Bipolar Zero (With 20Ω Trimmer)                                  |                     | ±0.2                                       |                     |         | **   |                 | % of F.S.        |

\*\*Specifications same as AD561S specs.  
Specifications subject to change without notice.



## DIGITAL LOGIC INTERFACE

All standard positive supply logic families interface easily with the AD561. The digital code is positive true binary (all bits high, Logic "1", gives positive full scale output). The logic input load factor (100nA max at Logic "1", -25μA max at Logic "0", 3pF capacitance), is less than one equivalent digital load for all logic families, including unbuffered CMOS. The digital threshold is set internally as a function of the positive supply, as shown in Figure 1. For most applications, connecting V<sub>CC</sub> to the positive logic supply will set the threshold at the proper level for maximum noise immunity. For nonstandard applications, refer to Figure 1 for threshold levels. Uncommitted bit input lines will assume a "1" state (similar to TTL), but they are high impedance and subject to noise pickup. Unused digital inputs should be connected directly to ground or V<sub>CC</sub>, as desired.

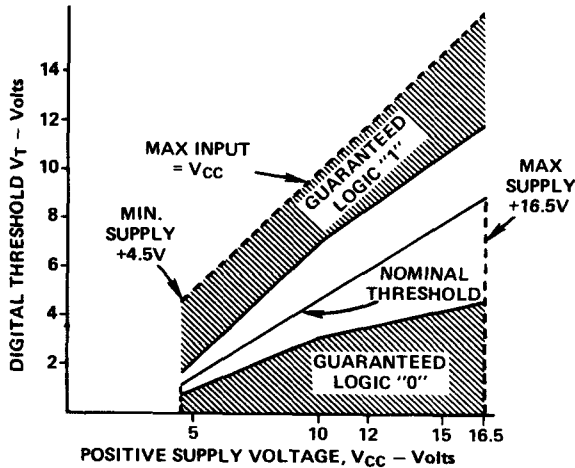
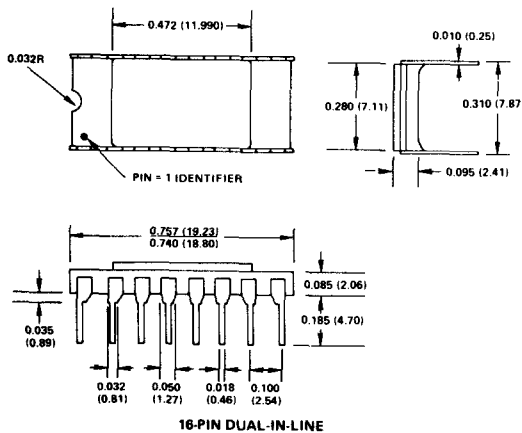


Figure 1. Digital Threshold Vs. Positive Supply



### OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Figure 2.

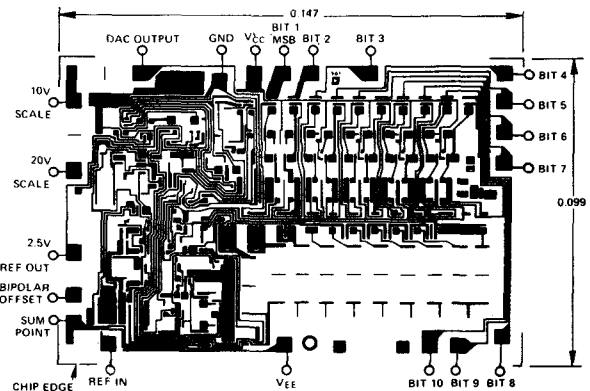
## THE AD561 OFFERS TRUE 10-BIT RESOLUTION OVER FULL TEMPERATURE RANGE

**ACCURACY:** Analog Devices defines accuracy as the maximum deviation of the actual, adjusted DAC output (see following page) from the ideal analog output (a straight line drawn from 0 to F.S. - 1LSB) for any bit combination. The AD561 is laser trimmed to 1/4LSB (0.025% of F.S.) maximum error at +25°C for the K and T versions - 1/2LSB for the J and S.

**MONOTONICITY:** A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a single-valued function of the input. All versions of the AD561 are monotonic over their full operating temperature range.

**DIFFERENTIAL NONLINEARITY:** Monotonic behavior requires that the differential nonlinearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 9.8mV change in the analog output (1LSB = 10V x 1/1024 = 9.8mV). If in actual use, however, a 1LSB change in the input code results in a change of only 2.45mV (1/4LSB) in analog output, the differential nonlinearity error would be 7.35mV, or 3/4LSB. The AD561K and T have a max differential linearity error of 1/2LSB.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 2.5ppm/°C could under worst case conditions for a temperature change of +25°C to +125°C add 0.025% (100 x 2.5ppm/°C of error). The resulting error could then be as much as 0.025% + 0.025% = 0.05% of F.S. (1/2LSB represents 0.05% of F.S.). To be sure of accurate performance all versions of the AD561 are therefore 100% tested to be monotonic over the full operating temperature range.



THE AD561 IS AVAILABLE IN A LASER TRIMMED CHIP FORM. THE CHIP OFFERS MORE APPLICATION FLEXIBILITY THAN THE 16-PIN PACKAGED DEVICE. PLEASE CONSULT FACTORY FOR CHIP APPLICATION DETAILS.

Figure 3. Chip Bonding Diagram

## AD561 ORDERING GUIDE

| MODEL        | TEMP RANGE    | ACCURACY @ +25°C | GAIN T.C. (of F.S./°C) |  |  |
|--------------|---------------|------------------|------------------------|--|--|
| AD561J       | 0 to +70°C    | ±½LSB max        | 80ppm max              |  |  |
| AD561K       | 0 to +70°C    | ±¼LSB max        | 30ppm max              |  |  |
| AD561S       | -55 to +125°C | ±½LSB max        | 60ppm max              |  |  |
| AD561S/883B* | -55 to +125°C | ±½LSB max        | 60ppm max              |  |  |
| AD561T       | -55 to +125°C | ±¼LSB max        | 30ppm max              |  |  |
| AD561T/883B* | -55 to +125°C | ±¼LSB max        | 30ppm max              |  |  |

\*The AD561S/883B and AD561T/883B are fully processed to MIL-STD-883A, Method 5004, Class B. The complete procedure list is available on request.

## CONNECTING THE AD561 FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510, AD741L, AD301AL) is used, excellent performance can be obtained in many situations without trimming. (A 5mV op amp offset is equivalent to 1/2LSB on a 10 volt scale). If a 25Ω fixed resistor is substituted for the 50Ω trimmer, unipolar zero will typically be within ±1/10LSB (plus op amp offset), and full scale accuracy will be within ±1LSB. Substituting a 10Ω resistor for the 20Ω bipolar offset trimmer will give a bipolar zero error typically within ±1LSB.

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±½LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25picofarad DAC output capacitance.

### FIGURE 5. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range.

#### STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust op amp trimmer, R<sub>1</sub>, until the output reads 0.000 volts (1LSB = 9.76mV).

#### STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 50Ω gain trimmer, R<sub>2</sub>, until the output is 9.990 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.23V full scale is desired (exactly 10mV/bit), insert a 120Ω resistor in series with R<sub>2</sub>.

### FIGURE 6. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.990 volts, with positive full scale occurring with all bits ON (all 1's).

#### STEP I . . . ZERO ADJUST

Turn ON MSB only, turn OFF all other bits. Adjust 20Ω trimmer R<sub>3</sub>, to give 0.000 output volts.

#### STEP II . . . GAIN ADJUST

Turn OFF all bits, adjust 50Ω gain trimmer to give a reading of -5.000 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, the op amp trimmer is unnecessary unless the untrimmed offset drift of the op amp is excessive.

### FIGURE 7. ±10 VOLT BUFFERED BIPOLAR OUTPUT

The AD561 can also be connected for a ±10 volt bipolar range with an additional external resistor as shown in Figure 7. A larger value trimmer is required to compensate for tolerance in the thin film resistors (which are trimmed to match the full scale current). For best full scale temperature coefficient performance, the external resistors should have a T.C. of -50ppm/°C. For applications requiring optimum performance, a ±10 volt bonding option is available on special order.

## PIN CONFIGURATION TOP VIEW

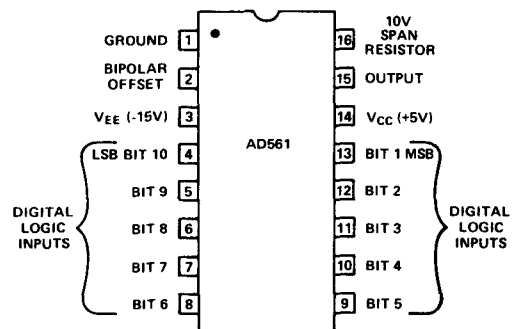


Figure 4.

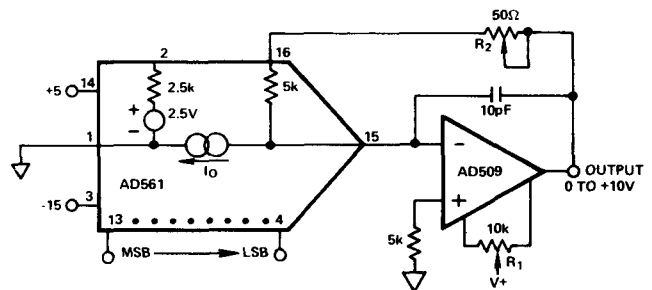


Figure 5. 0 to +10V Unipolar Voltage Output

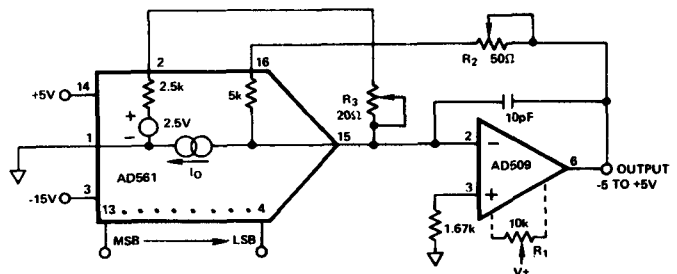


Figure 6. ±5V Buffered Bipolar Voltage Output

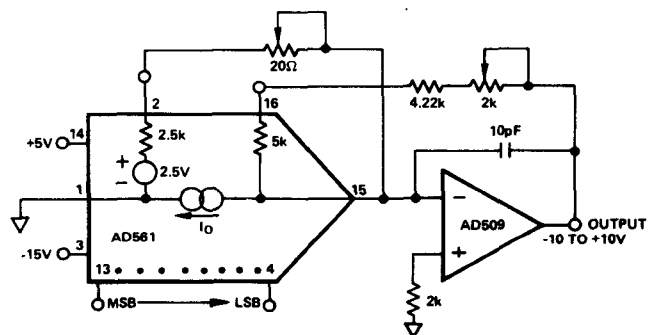


Figure 7. ±10V Buffered Voltage Output

## CIRCUIT DESCRIPTION

A simplified schematic with the essential circuit features of the AD561 is shown in Figure 8. The voltage reference, CR1, is a buried zener (or subsurface breakdown diode). This device exhibits far better all-around performance than the NPN base-emitter reverse-breakdown diode (surface zener), which is in nearly universal use in integrated circuits as a voltage reference. Greatly improved long term stability and lower noise are the major benefits the buried zener derives from isolating the breakdown point from surface stress and mobile oxide charge effects. The nominal 7.5 volt device (including temperature compensation circuitry) is driven by a current source to the negative supply so that the positive supply can be allowed to go as low as 4.5 volts. The temperature coefficient of each diode is determined individually; this data is then used to laser trim a compensating circuit to balance the overall T.C. to zero. The typical resulting T.C. is 0 to  $\pm 15 \text{ ppm}/^\circ\text{C}$ .

The negative reference level is inverted and scaled by  $A_1$  to give a +2.5 volt reference (which can be driven by the low positive supply). The AD561, packaged in the 16-pin DIP, has the +2.5 volt reference (REF OUT) connected directly to the input of the control amplifier (REF IN). The buffered reference is not directly available externally except through the  $2.5 \text{ k}\Omega$  bipolar offset resistor; it can still be used as a voltage reference as shown below in Figure 9.

The  $2.5 \text{ k}\Omega$  scaling resistor and control amplifier  $A_2$  then force a 1mA reference current to flow through reference transistor

$Q_1$ , which has a relative emitter area of 8A. This is accomplished by forcing the bottom of the ladder to the proper voltage. Since  $Q_1$  and  $Q_2$  have equal emitter areas and have equal  $5 \text{ k}\Omega$  emitter resistors,  $Q_2$  also carries 1mA. The ladder voltage drop constrains  $Q_7$  (with area 4A) to carry only 0.5mA;  $Q_8$  carries 0.25mA, etc.

The first four significant bit cells are scaled exactly in emitter area to match  $Q_1$  for optimum  $V_{BE}$  and  $V_{BE}$  drift match, as well as for beta match. These effects are insignificant for the lower order bits, which account for a total of only 1/16 of full scale. However, the 18mV  $V_{BE}$  difference between two matched transistors carrying emitter currents in a ratio of 2:1 must be corrected. This is done by forcing  $120 \mu\text{A}$  through the  $150 \Omega$  interbase resistors. These resistors and the R-2R ladder resistors are actively laser-trimmed at the wafer level to bring total device accuracy to better than  $\frac{1}{4} \text{ LSB}$ . Sufficient ratio accuracy in the last two bits is obtained by simple emitter area ratio such that it is unnecessary to use additional area for ladder resistors. The current in  $Q_{16}$  is added to the ladder to balance it properly but is not switched to the output; thus full scale is  $1023/1024 \times 2 \text{ mA}$ .

The switching cell of  $Q_3, Q_4, Q_5$  and  $Q_6$  serves to steer the cell current either to ground (BIT 1 low) or to the DAC output (BIT 1 high). The entire switching cell carries the same current whether the bit is on or off, thus minimizing thermal transients and ground current errors. The logic threshold, which is generated from the positive supply (see Digital Logic Interface) is applied to one side of each cell.

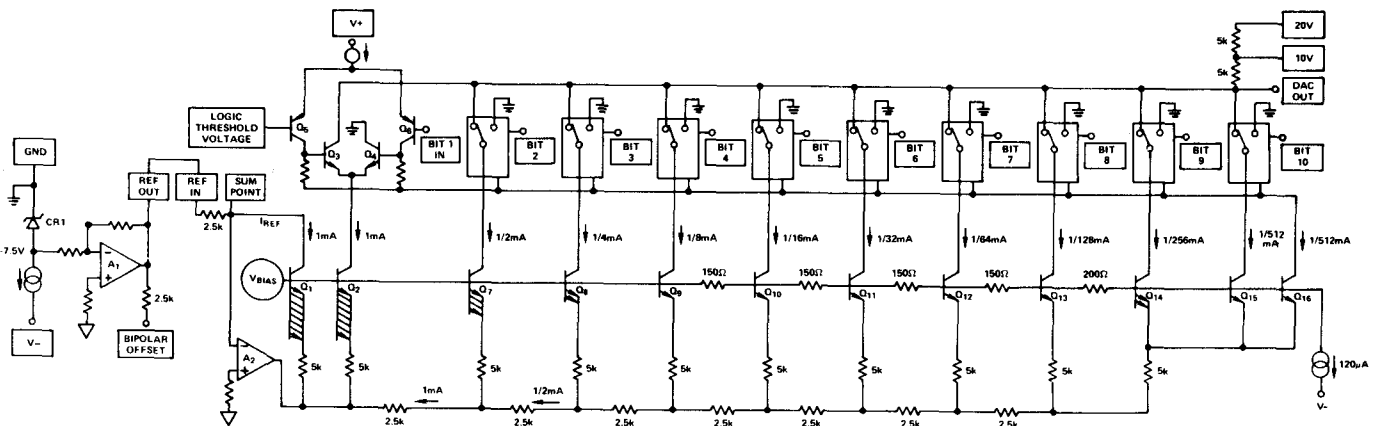


Figure 8. Circuit Diagram Showing Reference, Control Amplifier, Switching Cell, R-2R Ladder, and Bit Arrangement of AD561

## PRECISION LOW-NOISE REFERENCE

The precision reference of the AD561 can be brought out separately from the DAC to serve as a master system reference. Since the reference is connected through the  $2.5 \text{ k}\Omega$  bipolar offset resistor, it must be buffered externally, as shown here in Figure 9. The DAC section can still be operated independently in a unipolar mode, but internal thermal and ground loop effects will create crosstalk of about 0.01% with an ideal ground. The long term stability of this reference will be especially good, typically  $\pm 0.01\%$  per year or better. If the filter capacitor, C is not used, wideband output noise will be about 120ppm p-p (1.2mV p-p for 10 volts). If C is  $4.7 \mu\text{F}$ , wideband noise will be about  $25 \mu\text{V}$  p-p (10 volts out) and  $15 \mu\text{V}$  p-p from 0.1 to 10Hz.

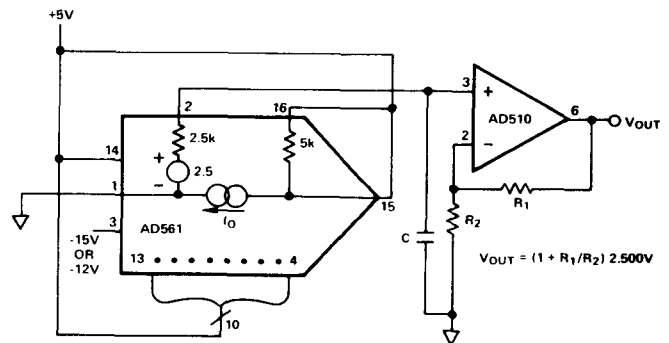


Figure 9. Precision Ultra Low Noise Reference

## SETTLING TIME

The high speed NPN current steering switching cell and internally compensated reference amplifier of the AD561 are specifically designed for fast settling operation. The typical settling time to  $\pm 0.05\%$  ( $\frac{1}{2}$ LSB) for the worst case transition (major carry, 011111111 to 100000000) is less than 250ns; the lower order bits all settle in less than 200ns. (Worst case settling occurs when all bits are switched, especially the MSB.) But full realization of this high speed performance requires strict attention to detail by the user in all areas of application and testing.

The settling time for the AD561 is specified in terms of the current output, an inherently high speed DAC operating mode. However, most DAC applications require a current-to-voltage conversion at some point in the signal path, although an unbuffered voltage level (not using an op amp) is suitable for use in a successive-approximation A/D converter (see next page), or in many display applications. This form of conversion can give very fast operation if proper design and layout is done. The fastest voltage conversion is achieved by connecting a low value resistor directly to the output, as shown in Figure 12. In this case, the settling time is primarily determined by the cell switching time and by the RC time constant of the AD561 output capacitance of 25 picofarads (plus stray capacitance) combined with the output resistor value. Settling to 0.05% of full scale (for a full scale transition) requires 7.6 time constants. This effect is important for  $R > 1k\Omega$ .

If an op amp must be used to provide a low impedance output signal, some loss in settling time will be seen due to op amp dynamics. The normal current-to-voltage converter op amp circuits are shown in the applications circuits using the fast settling AD509. The circuits shown settle to  $\pm \frac{1}{2}$ LSB in 600ns unipolar and 1.1 $\mu$ s bipolar. The DAC output capacitance, which acts as a stray capacitance at the op amp inverting input, must be compensated by a feedback capacitor, as shown. The value should be chosen carefully for each application and each op amp type.

Fastest operation will be obtained by minimizing lead lengths, stray capacitance and impedance levels. Both supplies should be bypassed near the devices; 0.1 $\mu$ F will be sufficient since the AD561 runs at constant supply current regardless of input code.

## POWER SUPPLY SELECTION

The AD561 will operate over a wide range of power supply voltages, with a total supply from 15.3 to 33 volts. Symmetrical supplies are not required, and in many applications not recommended.

The positive supply level determines the digital threshold level, as explained previously and shown in Figure 1. It is therefore recommended that  $V_{CC}$  be connected directly to the digital supply for best threshold match.

Positive output voltage compliance is unaffected by the positive supply level because of the open collector output stage design; thus the full +10 volt compliance is available even with a +5 volt  $V_{CC}$  level. Power supply rejection is excellent, so that digital supply noise will not be reflected to the output. but use of a 0.1 $\mu$ F bypass capacitor near the AD561 is recommended for decoupling.

## OUTPUT VOLTAGE COMPLIANCE

The AD561 has a typical output compliance range from -3 to +10 volts. The output current is unaffected by changes in the output terminal voltage over that range. This results from the use of open collector output switching stages in a cascode configuration, and gives an output impedance of 40M $\Omega$ . Positive compliance range is limited only by collector breakdown (and is independent of positive supply level), but the negative range is limited by the required bias levels and resistor ladder voltage. Negative compliance varies with negative supply, as shown in Figure 10. The compliance range is guaranteed to be -2 to +10 volts with  $V_{EE} = -15$  volts.

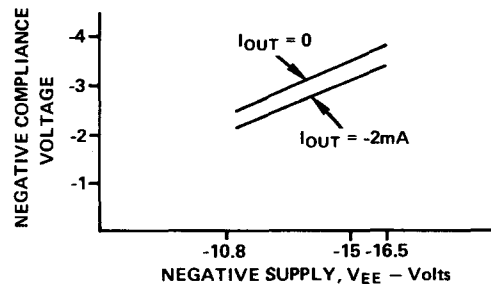


Figure 10. Typical Negative Compliance Range Vs. Negative Supply.

## DIRECT UNBUFFERED VOLTAGE OUTPUT

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 1 shows a connection using the gain and bipolar output resistors to give a  $\pm 1.66$  volt bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors ( $R_X$ ) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to -2mA unipolar output current and using the 2.5 volt reference voltage for bipolar offset. For example, setting  $R_X = 2.5k\Omega$  gives a  $\pm 1$  volt range with a 1k $\Omega$  equivalent output impedance. A 0 to +10 volt output can be obtained by connecting the 5k $\Omega$  gain resistor to 9.99 volts; again the digital code is complementary binary.

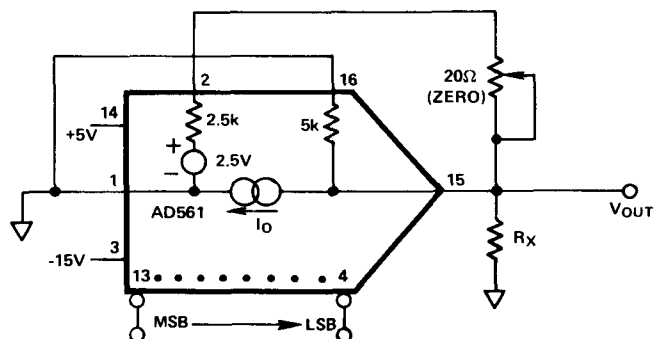


Figure 11. Unbuffered Bipolar Voltage Output

The nominal negative supply level is -15 volts, with an allowable range of -10.8 to -16.5 volts. The negative supply level affects the negative compliance range, as shown in Figure 10.

## HIGH SPEED 10-BIT A/D CONVERTERS

The fast settling characteristics of the AD561 make it ideal for high speed successive approximation A/D converters. The internal reference and trimmed application resistors allow a 10-bit converter system to be constructed with a minimum parts count. Shown here is a configuration using standard components; this system completes a full 10-bit conversion in  $5.5\mu\text{s}$  unipolar or  $12\mu\text{s}$  bipolar. This converter will be accurate to  $\pm 1/2\text{LSB}$  of 10 bits and have a typical gain T.C. of  $10\text{ppm}/^\circ\text{C}$ .

In the unipolar mode, the system range is 0 to 9.99 volts, with each bit having a value of  $9.76\text{mV}$ . For true conversion accuracy, an A/D converter should be trimmed so that a given bit code output results from input levels from  $1/2\text{LSB}$  below to  $1/2\text{LSB}$  above the exact voltage which that code represents. Therefore, the converter zero point should be trimmed with an input voltage of  $+4.9\text{mV}$ ; trim  $R_1$  until the LSB just begins to appear in the output code (all other bits "0"). For full scale, use an input voltage of  $+9.9985$  volts ( $10\text{ volts} - 1\text{LSB} - 1/2\text{LSB}$ ); then trim  $R_2$  again until the LSB just begins to appear (all other bits "1").

The bipolar signal range is  $-5.0$  to  $+4.99$  volts. Bipolar offset trimming is done by applying a  $+4.9\text{mV}$  input signal and trimming  $R_1$  for the LSB transition (MSB "1", all other bits "0").

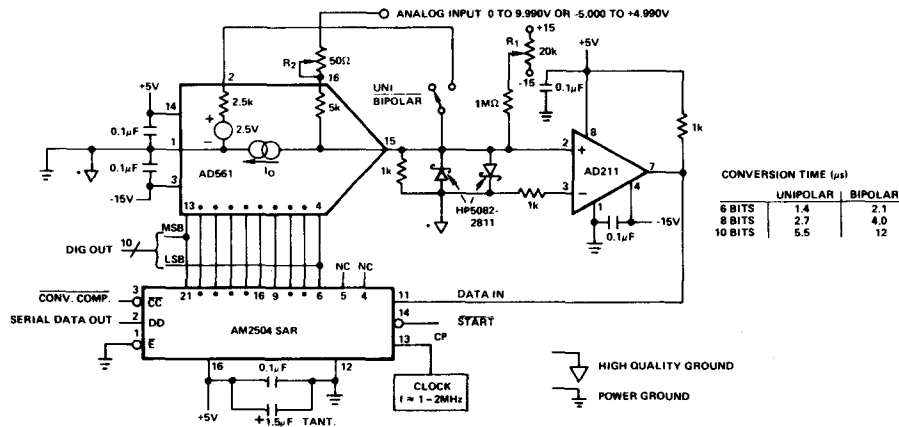


Figure 12. Fast Precision Analog to Digital Converter

## DIGITAL 4 TO 20mA OR 1 TO 5 VOLT CONVERTER

A direct digital 4 to 20mA or 1 to 5 volt line driver can be built with the AD561 as shown in Figure 13. The 2.5 volt reference is divided to provide 1 volt at the op amp non-inverting input — thus a zero input code results in a 1 volt output at the Darlington emitter ( $V_{\text{OUT}}$ ). The  $2\text{k}\Omega$  feedback resistance converts the nominal  $2\text{mA}$  ( $\pm 20\%$ ) full scale output from the AD561 to 4 volts, for a total output of 5 volts F.S. The voltage at the emitter forces a proportional current through the  $250\Omega$  (which appears at the collector as  $I_{\text{OUT}}$ ). The AD561 current is added to the  $4\text{--}20\text{mA}$  line; thus 5 volts full scale gives  $22\text{mA}$  in the current loop. For exactly  $20\text{mA}$ , trim the  $1\text{k}\Omega$  pot for  $4.5\text{V}$  F.S. (A single op amp circuit will not produce both 1 to 5 volt and 4 to 20mA outputs simultaneously.)

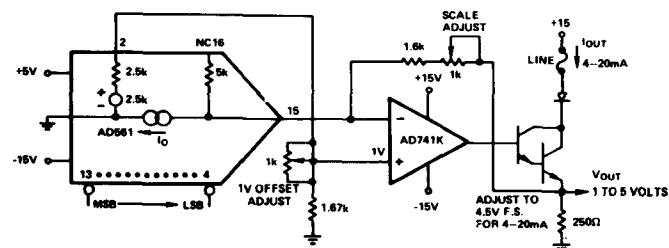


Figure 13. Digital 4 to 20mA or 1 to 5 Volt Line Driver

## 120S D/A CONVERTERS

Full scale is set by applying  $-4.995$  volts and trimming  $R_2$  for the LSB transition (all other bits "0"). In many applications, the pretrimmed application resistors are sufficiently accurate that external trimmers will be unnecessary, especially in situations requiring less than full 10-bit  $\pm 1/2\text{LSB}$  accuracy.

For fastest operation, the impedance at the comparator summing node must be minimized, as mentioned in the section on settling time. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance of  $1\text{k}\Omega$ ,  $1\text{LSB} = 2\text{mV}$ ) to the point that comparator performance will be sacrificed. A  $1\text{k}\Omega$  resistor is the optimum value for this application for 10-bit accuracy. The chart shown in the figure gives the speed of the ADC for  $\pm 1/2\text{LSB}$  accuracy (and no missing codes) for 6, 8 and 10-bit resolution.

A much faster converter can be constructed by using higher performance external components. Each individual high-order bit settles in less than  $250\text{ns}$ ; the low-order bits less than  $200\text{ns}$ . Because of this, a staged clock which speeds up for lower bits will improve the speed. Also, a faster comparator and Schottky TTL or ECL logic would be necessary. 10-bit converters in the  $3$  to  $5\mu\text{s}$  range could be built around the AD561 with these techniques.

## DIGITALLY PROGRAMMABLE SETPOINT COMPARATOR

Figure 14 demonstrates a high accuracy systems-oriented setpoint comparator. The 2.5 volt reference is buffered and amplified by the AD741K to produce an exact  $10.000$  volt reference which could be used as a primary system reference for several such circuits. The  $+10$  volt compliance of the AD561 then allows it to generate a zero to  $+10$  volt output swing through the  $5\text{k}\Omega$  application resistor without an additional op amp. The digital code for this system will be complementary binary (all 1's give  $0.00$  volts out).

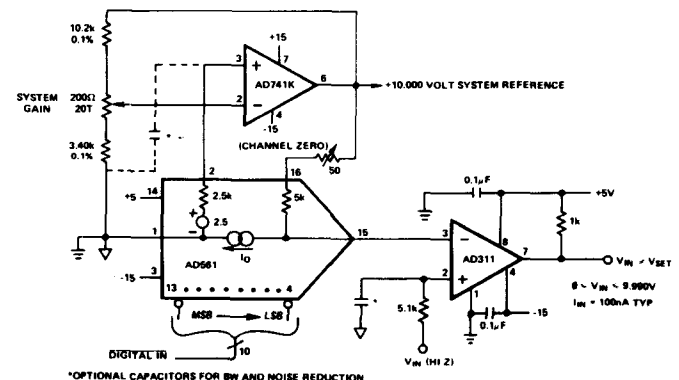


Figure 14. Digitally Programmable Set Point Comparator

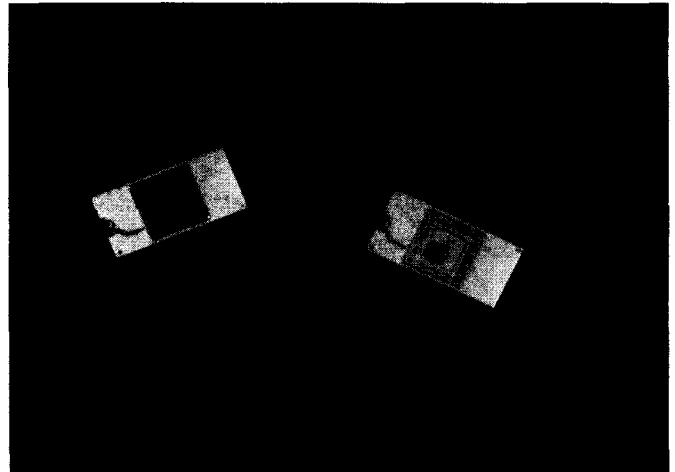
**FEATURES****Single Chip Construction****Very High Speed: Settles to 1/2LSB in 200ns****Full Scale Switching Time: 30ns****High Stability Buried Zener Reference on Chip****Monotonicity Guaranteed Over Temperature****Linearity Guaranteed Over Temperature — 1/2LSB max  
(AD565K, T)****Low Power: 225mW Including Reference****Pin-Out Compatible with AD563****Low Cost****PRODUCT DESCRIPTION**

The AD565 is a fast 12-bit digital-to-analog converter combined with a high stability voltage reference on a single monolithic chip. The AD565 chip uses 12 precision, high speed bipolar current steering switches, control amplifier, laser-trimmed thin film resistor network, and buried Zener voltage reference to produce a very fast, high accuracy analog output current.

The combination of performance and flexibility in the AD565 has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). The AD565 has a 10 — 90% full scale transition time under 35 nanoseconds and settles to within  $\pm 1/2$ LSB in 200 nanoseconds. The AD565 chips are laser-trimmed at the wafer level to  $\pm 1/8$ LSB typical linearity and are specified to  $\pm 1/4$ LSB max error (K, S, and T grades) at +25°C. This high speed and accuracy make the AD565 the ideal choice for high speed display drivers as well as fast analog-to-digital converters.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim both the absolute value of the reference as well as its temperature coefficient. The AD565 is thus well suited for wide temperature range performance with maximum linearity error to  $\pm 1/2$ LSB and guaranteed monotonicity over the full temperature range. Typical full scale gain T.C. is 10ppm/°C.

The AD565 is available in four performance grades and two package types. The AD565J and K are specified for use over the 0 to 70°C temperature range and are both available in either a 24-pin, hermetically-sealed, side-brazed ceramic DIP, or a 24 pin plastic DIP. The AD565S and T grades are specified for the -55 to +125°C range and are available in the ceramic package.

**PRODUCT HIGHLIGHTS**

1. The AD565 is a self-contained current output DAC and voltage reference fabricated on a single IC chip.
2. The device incorporates a newly developed\* fully differential, non-saturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562 with very fast switching times and an optimally-damped settling characteristic.
3. The internal buried zener reference is laser-trimmed to 10.00 volts with a  $\pm 1\%$  maximum error. The reference voltage is available externally and can supply up to 1.5mA beyond that required for the reference and bipolar offset resistors.
4. The chip also contains SiCr thin film application resistors which can be used either with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
5. The pin-out of the AD565 is compatible with the industry-standard AD563 so that a system can easily be upgraded to higher speed performance without board changes.
6. The single-chip construction makes the AD565 inherently more reliable than hybrid multi-chip designs. The AD565S and T grades with guaranteed linearity and monotonicity over the -55°C to +125°C range are especially recommended for high reliability needs in harsh environments. These units are available fully processed to MIL-STD-883, Level B.

\*Covered by patent numbers: 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and other patents pending.

# SPECIFICATIONS ( $T_A = +25^\circ\text{C}$ , $V_{CC} = +15\text{V}$ , $V_{EE} = -15\text{V}$ , unless otherwise specified)

| MODEL   | AD565J     |                         |            | AD565K                  |            |           | UNITS                 |
|---|------------|-------------------------|------------|-------------------------|------------|-----------|-----------------------|
|   | MIN        | TYP                     | MAX        | MIN                     | TYP        | MAX       |                       |
| <b>DATA INPUTS (Pins 13 to 24)</b>  |            |                         |            |                         |            |           |                       |
| TTL or 5 Volt CMOS ( $T_{\min}$ to $T_{\max}$ )                               |            |                         |            |                         |            |           |                       |
| Input Voltage   |            |                         |            |                         |            |           |                       |
| Bit ON Logic "1"  | +2.0       |                         | +5.5       | +2.0                    |            | +5.5      | V                     |
| Bit OFF Logic "0"   |            |                         | +0.8       |                         |            | +0.8      | V                     |
| Logic Current (each bit)  |            |                         |            |                         |            |           |                       |
| Bit ON Logic "1"  |            | +120                    | +260       | +120                    |            | +260      | $\mu\text{A}$         |
| Bit OFF Logic "0"   |            | +35                     | +75        | +35                     |            | +75       | $\mu\text{A}$         |
| <b>RESOLUTION</b>   |            |                         | 12         |                         |            | 12        | Bits                  |
| <b>OUTPUT</b>   |            |                         |            |                         |            |           |                       |
| Current   |            |                         |            |                         |            |           |                       |
| Unipolar (all bits on)  | -1.6       | -2.0                    | -2.4       | -1.6                    | -2.0       | -2.4      | mA                    |
| Bipolar (all bits on or off)  | $\pm 0.8$  | $\pm 1.0$               | $\pm 1.2$  | $\pm 0.8$               | $\pm 1.0$  | $\pm 1.2$ | mA                    |
| Resistance (exclusive of span resistors)                                      | 6k         | 8k                      | 10k        | 6k                      | 8k         | 10k       | $\Omega$              |
| Offset  |            |                         |            |                         |            |           |                       |
| Unipolar  |            | 0.01                    | 0.05       |                         | 0.01       | 0.02      | % of F.S.             |
| Bipolar (Figure 5, $R_2 = 50\Omega$ fixed)                                    |            | 0.05                    | 0.15       |                         | 0.05       | 0.1       | % of F.S.             |
| Capacitance   |            | 25                      |            |                         | 25         |           | pF                    |
| Compliance Voltage  |            |                         |            |                         |            |           | V                     |
| $T_{\min}$ to $T_{\max}$  | -1.5       |                         | +10        | -1.5                    |            | +10       | V                     |
| <b>ACCURACY (error relative to full scale) <math>+25^\circ\text{C}</math></b> |            |                         |            |                         |            |           |                       |
|   |            | $\pm 1/4$               | $\pm 1/2$  | $\pm 1/8$               | $\pm 1/4$  |           | LSB                   |
|   |            | (0.006)                 | (0.012)    | (0.003)                 | (0.006)    |           | % of F.S.             |
| $T_{\min}$ to $T_{\max}$  |            | $\pm 1/2$               | $\pm 3/4$  | $\pm 1/4$               | $\pm 1/2$  |           | LSB                   |
|   |            | (0.012)                 | (0.018)    | (0.006)                 | (0.012)    |           | % of F.S.             |
| <b>DIFFERENTIAL NONLINEARITY <math>+25^\circ\text{C}</math></b>               |            |                         |            |                         |            |           |                       |
| $T_{\min}$ to $T_{\max}$  |            | $\pm 1/2$               | $\pm 3/4$  | $\pm 1/4$               | $\pm 1/2$  |           | LSB                   |
|   |            | MONOTONICITY GUARANTEED |            | MONOTONICITY GUARANTEED |            |           |                       |
| <b>TEMPERATURE COEFFICIENTS</b>   |            |                         |            |                         |            |           |                       |
| With Internal Reference   |            |                         |            |                         |            |           |                       |
| Unipolar Zero   |            | 1                       | 2          | 1                       | 2          |           | ppm/ $^\circ\text{C}$ |
| Bipolar Zero  |            | 5                       | 10         | 5                       | 10         |           | ppm/ $^\circ\text{C}$ |
| Gain (Full Scale)   |            | 15                      | 30         | 10                      | 20         |           | ppm/ $^\circ\text{C}$ |
| Differential Nonlinearity   |            | 2                       |            | 2                       |            |           | ppm/ $^\circ\text{C}$ |
| <b>SETTLING TIME TO 1/2LSB</b>  |            |                         |            |                         |            |           |                       |
| All Bits ON-to-OFF or OFF-to-ON   |            | 200                     | 400        | 200                     | 400        |           | ns                    |
| <b>FULL SCALE TRANSITION</b>  |            |                         |            |                         |            |           |                       |
| 10% to 90% Delay plus Rise Time   |            | 15                      | 30         | 15                      | 30         |           | ns                    |
| 90% to 10% Delay plus Fall Time   |            | 30                      | 50         | 30                      | 50         |           | ns                    |
| <b>TEMPERATURE RANGE</b>  |            |                         |            |                         |            |           |                       |
| Operating   | 0          |                         | +70        | 0                       |            | +70       | $^\circ\text{C}$      |
| Storage (D Package)   | -65        |                         | +150       | -65                     |            | +150      | $^\circ\text{C}$      |
| Storage (N Package)   | -25        |                         | +100       | -25                     |            | +100      | $^\circ\text{C}$      |
| <b>POWER REQUIREMENTS</b>   |            |                         |            |                         |            |           |                       |
| $V_{CC}$ , +13.5 to +16.5V dc   |            | 3                       | 5          | 3                       | 5          |           | mA                    |
| $V_{EE}$ , -13.5 to -16.5V dc   |            | -12                     | -18        | -12                     | -18        |           | mA                    |
| <b>POWER SUPPLY GAIN SENSITIVITY</b>  |            |                         |            |                         |            |           |                       |
| $V_{CC} = +15\text{V}$ , $\pm 10\%$   |            | 3                       | 10         | 3                       | 10         |           | ppm of F.S./%         |
| $V_{EE} = -15\text{V}$ , $\pm 10\%$   |            | 15                      | 25         | 15                      | 25         |           | ppm of F.S./%         |
| <b>PROGRAMMABLE OUTPUT RANGE (see Figures 4,5,6)</b>                          |            |                         |            |                         |            |           |                       |
|   |            | 0 to +5                 |            | 0 to +5                 |            |           | V                     |
|   |            | -2.5 to +2.5            |            | -2.5 to +2.5            |            |           | V                     |
|   |            | 0 to +10                |            | 0 to +10                |            |           | V                     |
|   |            | -5 to +5                |            | -5 to +5                |            |           | V                     |
|   |            | -10 to +10              |            | -10 to +10              |            |           | V                     |
| <b>EXTERNAL ADJUSTMENTS</b>   |            |                         |            |                         |            |           |                       |
| Gain Error with Fixed $50\Omega$ Resistor for $R_2$ (Fig. 4)                  |            |                         |            |                         |            |           |                       |
| Bipolar Zero Error with Fixed $50\Omega$ Resistor for $R_1$ (Fig. 5)          |            | $\pm 0.1$               | $\pm 0.25$ | $\pm 0.1$               | $\pm 0.25$ |           | % of F.S.             |
| Gain Adjustment Range (Fig. 4)  | $\pm 0.25$ |                         |            | $\pm 0.25$              |            |           | % of F.S.             |
| Bipolar Zero Adjustment Range   | $\pm 0.15$ |                         |            | $\pm 0.15$              |            |           | % of F.S.             |
| <b>REFERENCE INPUT</b>  |            |                         |            |                         |            |           |                       |
| Input Impedance   | 15k        | 20k                     | 25k        | 15k                     | 20k        | 25k       | $\Omega$              |
| <b>REFERENCE OUTPUT</b>   |            |                         |            |                         |            |           |                       |
| Voltage   | 9.90       | 10.00                   | 10.10      | 9.90                    | 10.00      | 10.10     | V                     |
| Current (available for external loads)  | 1.5        | 2.5                     |            | 1.5                     | 2.5        |           | mA                    |
| <b>POWER DISSIPATION</b>  |            | 225                     | 345        |                         | 225        | 345       | mW                    |

| MODEL  | AD565S     |                         |            | AD565T     |                         |            | UNITS         |
|--|------------|-------------------------|------------|------------|-------------------------|------------|---------------|
|  | MIN        | TYP                     | MAX        | MIN        | TYP                     | MAX        |               |
| <b>DATA INPUTS (Pins 13 to 24)</b>                                 |            |                         |            |            |                         |            |               |
| TTL or 5 Volt CMOS ( $T_{min}$ to $T_{max}$ )                      |            |                         |            |            |                         |            |               |
| Input Voltage  |            |                         |            |            |                         |            |               |
| Bit ON Logic "1"   | +2.0       |                         | +5.5       | +2.0       |                         | +5.5       | V             |
| Bit OFF Logic "0"  |            |                         | +0.8       |            |                         | +0.8       | V             |
| Logic Current (each bit)   |            |                         |            |            |                         |            |               |
| Bit ON Logic "1"   |            | +120                    | +260       | +120       |                         | +260       | $\mu$ A       |
| Bit OFF Logic "0"  |            | +35                     | +75        | +35        |                         | +75        | $\mu$ A       |
| <b>RESOLUTION</b>  |            |                         | 12         |            |                         | 12         | Bits          |
| <b>OUTPUT</b>  |            |                         |            |            |                         |            |               |
| Current  |            |                         |            |            |                         |            |               |
| Unipolar (all bits on)   | -1.6       | -2.0                    | -2.4       | -1.6       | -2.0                    | -2.4       | mA            |
| Bipolar (all bits on or off)                                       | $\pm 0.8$  | $\pm 1.0$               | $\pm 1.2$  | $\pm 0.8$  | $\pm 1.0$               | $\pm 1.2$  | mA            |
| Resistance (exclusive of span resistors)                           |            |                         |            |            |                         |            |               |
|  | 6k         | 8k                      | 10k        | 6k         | 8k                      | 10k        | $\Omega$      |
| Offset   |            |                         |            |            |                         |            |               |
| Unipolar   |            | 0.01                    | 0.05       |            | 0.01                    | 0.02       | % of F.S.     |
| Bipolar (Figure 5, $R_2 = 50\Omega$ fixed)                         |            | 0.05                    | 0.15       |            | 0.05                    | 0.1        | % of F.S.     |
| Capacitance  |            |                         |            |            |                         |            |               |
| Compliance Voltage   |            | 25                      |            |            | 25                      |            | pF            |
| $T_{min}$ to $T_{max}$   | -1.5       |                         | +10        | -1.5       |                         | +10        | V             |
| <b>ACCURACY (error relative to full scale) +25°C</b>               |            |                         |            |            |                         |            |               |
|  |            | $\pm 1/8$               | $\pm 1/4$  |            | $\pm 1/8$               | $\pm 1/4$  | LSB           |
|  |            | (0.003)                 | (0.006)    |            | (0.003)                 | (0.006)    | % of F.S.     |
| $T_{min}$ to $T_{max}$   |            | $\pm 1/2$               | $\pm 3/4$  |            | $\pm 1/4$               | $\pm 1/2$  | LSB           |
|  |            | (0.012)                 | (0.018)    |            | (0.006)                 | (0.012)    | % of F.S.     |
| <b>DIFFERENTIAL NONLINEARITY +25°C</b>                             |            |                         |            |            |                         |            |               |
| $T_{min}$ to $T_{max}$   |            | $\pm 1/2$               | $\pm 3/4$  |            | $\pm 1/4$               | $\pm 1/2$  | LSB           |
|  |            | MONOTONICITY GUARANTEED |            |            | MONOTONICITY GUARANTEED |            |               |
| <b>TEMPERATURE COEFFICIENTS</b>                                    |            |                         |            |            |                         |            |               |
| With Internal Reference  |            |                         |            |            |                         |            |               |
| Unipolar Zero  |            | 1                       | 2          |            | 1                       | 2          | ppm/°C        |
| Bipolar Zero   |            | 5                       | 10         |            | 5                       | 10         | ppm/°C        |
| Gain (Full Scale)  |            | 15                      | 30         |            | 10                      | 15         | ppm/°C        |
| Differential Nonlinearity  |            | 2                       |            |            | 2                       |            | ppm/°C        |
| <b>SETTLING TIME TO 1/2LSB</b>                                     |            |                         |            |            |                         |            |               |
| All Bits ON-to-OFF or OFF-to-ON                                    |            | 200                     | 400        |            | 200                     | 400        | ns            |
| <b>FULL SCALE TRANSITION</b>                                       |            |                         |            |            |                         |            |               |
| 10% to 90% Delay plus Rise Time                                    |            | 15                      | 30         |            | 15                      | 30         | ns            |
| 90% to 10% Delay plus Fall Time                                    |            | 30                      | 50         |            | 30                      | 50         | ns            |
| <b>TEMPERATURE RANGE</b>   |            |                         |            |            |                         |            |               |
| Operating  | -55        |                         | +125       | -55        |                         | +125       | °C            |
| Storage (D Package)  | -65        |                         | +150       | -65        |                         | +150       | °C            |
| <b>POWER REQUIREMENTS</b>  |            |                         |            |            |                         |            |               |
| $V_{CC}$ , +13.5 to +16.5V dc                                      |            | 3                       | 5          |            | 3                       | 5          | mA            |
| $V_{EE}$ , -13.5 to -16.5V dc                                      |            | -12                     | -18        |            | -12                     | -18        | mA            |
| <b>POWER SUPPLY GAIN SENSITIVITY</b>                               |            |                         |            |            |                         |            |               |
| $V_{CC} = +15V, \pm 10\%$  |            | 3                       | 10         |            | 3                       | 10         | ppm of F.S./% |
| $V_{EE} = -15V, \pm 10\%$  |            | 15                      | 25         |            | 15                      | 25         | ppm of F.S./% |
| <b>PROGRAMMABLE OUTPUT</b>   |            |                         |            |            |                         |            |               |
| RANGE (see Figures 4,5,6)  |            | 0 to +5                 |            |            | 0 to +5                 |            | V             |
|  |            | -2.5 to +2.5            |            |            | -2.5 to +2.5            |            | V             |
|  |            | 0 to +10                |            |            | 0 to +10                |            | V             |
|  |            | -5 to +5                |            |            | -5 to +5                |            | V             |
|  |            | -10 to +10              |            |            | -10 to +10              |            | V             |
| <b>EXTERNAL ADJUSTMENTS</b>  |            |                         |            |            |                         |            |               |
| Gain Error with Fixed 50 $\Omega$ Resistor for R2 (Fig. 4)         |            |                         |            |            |                         |            |               |
|  |            | $\pm 0.1$               | $\pm 0.25$ |            | $\pm 0.1$               | $\pm 0.25$ | % of F.S.     |
| Bipolar Zero Error with Fixed 50 $\Omega$ Resistor for R1 (Fig. 5) |            |                         |            |            |                         |            |               |
|  |            | $\pm 0.05$              | $\pm 0.15$ |            | $\pm 0.05$              | $\pm 0.1$  | % of F.S.     |
| Gain Adjustment Range (Fig. 4)                                     | $\pm 0.25$ |                         |            | $\pm 0.25$ |                         |            | % of F.S.     |
| Bipolar Zero Adjustment Range                                      | $\pm 0.15$ |                         |            | $\pm 0.15$ |                         |            | % of F.S.     |
| <b>REFERENCE INPUT</b>   |            |                         |            |            |                         |            |               |
| Input Impedance  | 15k        | 20k                     | 25k        | 15k        | 20k                     | 25k        | $\Omega$      |
| <b>REFERENCE OUTPUT</b>  |            |                         |            |            |                         |            |               |
| Voltage  | 9.90       | 10.00                   | 10.10      | 9.90       | 10.00                   | 10.10      | V             |
| Current (available for external loads)                             | 1.5        | 2.5                     |            | 1.5        | 2.5                     |            | mA            |
| <b>POWER DISSIPATION</b>   |            | 225                     | 345        |            | 225                     | 345        | mW            |



**ABSOLUTE MAXIMUM RATINGS**

|   |   |
|---|---|
| V <sub>CC</sub> to Digital Common . . . . .             | 0 to +18V   |
| V <sub>EE</sub> to Digital Common . . . . .             | 0 to -18V   |
| Analog Common to Digital Common . . . . .               | ±1V   |
| Voltage on DAC Output (Pin 9) . . . . .                 | -3 to +12V  |
| Digital Inputs (Pins 13 to 24) to Digital Com . . . . . | -1.0 to +7.0V   |
| Ref In to Analog Common . . . . .                       | ±12V  |
| Bipolar Offset to Analog Common . . . . .               | ±12V  |
| 10V Span R to Analog Common . . . . .                   | ±12V  |
| 20V Span R to Analog Common . . . . .                   | ±24V  |
| Ref Out . . . . .                                       | Indefinite short to either Common<br>Momentary Short to V <sub>CC</sub> |
| Power Dissipation . . . . .                             | .1000mW   |

**THE AD565 OFFERS TRUE 12-BIT PERFORMANCE OVER THE FULL TEMPERATURE RANGE**

**ACCURACY:** Analog Devices defines accuracy as the maximum deviation of the actual, adjusted DAC output (see next page) from the ideal analog output (a straight line drawn from 0 to F.S. - 1LSB) for any bit combination. The AD565 is laser trimmed to 1/4LSB (0.025% of F.S.) maximum error at +25°C for the K and T versions - 1/2LSB for the J and S.

**MONOTONICITY:** A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a non-decreasing

function of the input. All versions of the AD565 are monotonic over their full operating temperature range.

**DIFFERENTIAL NONLINEARITY:** Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (1LSB = 10V x 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential linearity error would be 1.83mV, or 3/4LSB. The AD565K and T have a max differential linearity error of 1/2LSB, which is a tighter specification than simply guaranteeing monotonicity.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 1.0ppm/°C could under worst case conditions for a temperature change of +25°C to +125°C add 0.01% (100 x 1.0ppm/°C of error). The resulting error could then be as much as 0.01% + 0.006% = 0.016% of F.S. (1/2LSB represents 0.012% of F.S.). To be sure of accurate performance all versions of the AD565 are therefore 100% tested for monotonicity over the full operating temperature range.

**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

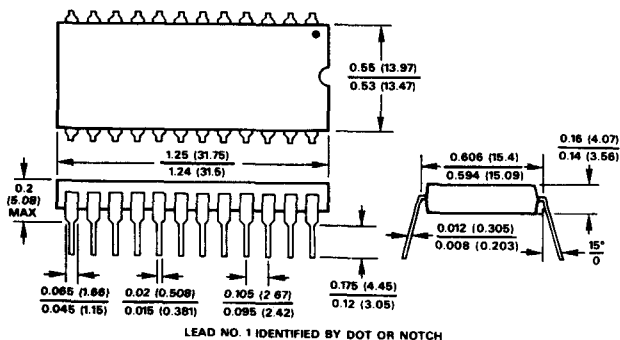


Figure 1. Molded Plastic Package (Type N) 24-Lead Dual-In-Line

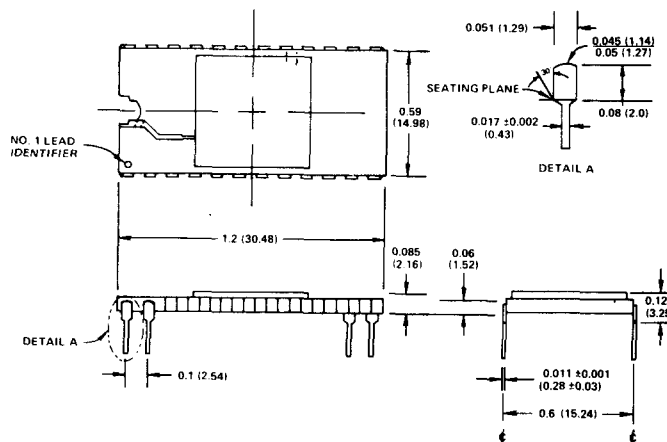


Figure 2. Hermetically-Sealed Ceramic Side-Brazed Package (Type D) 24-Lead Dual-In-Line

**AD565 ORDERING GUIDE**

**LINEARITY ERROR MAX @ 25°C**      **MAX GAIN T.C. (ppm of F.S./°C)**

| MODEL       | PACKAGE | TEMP RANGE    | LINEARITY ERROR MAX @ 25°C | MAX GAIN T.C. (ppm of F.S./°C) |
|-------------|---------|---------------|----------------------------|--------------------------------|
| AD565JN/BIN | Plastic | 0 to +70°C    | ±1/2LSB                    | 30                             |
| AD565JD/BIN | Ceramic | 0 to +70°C    | ±1/2LSB                    | 30                             |
| AD565KN/BIN | Plastic | 0 to +70°C    | ±1/4LSB                    | 20                             |
| AD565KD/BIN | Ceramic | 0 to +70°C    | ±1/4LSB                    | 20                             |
| AD565SD/BIN | Ceramic | -55 to +125°C | ±1/4LSB                    | 30                             |
| AD565TD/BIN | Ceramic | -55 to +125°C | ±1/4LSB                    | 15                             |

BCD versions of all models available July, 1979.

## CONNECTING THE AD565 FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50Ω fixed resistor is substituted for the 100Ω trimmer, unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

### FIGURE 4. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 8, should be grounded if not used for trimming.

#### STEP 1 . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 8 should then be connected to pin 5.

#### STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer, R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

### FIGURE 5. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

#### STEP 1 . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1, to give -5.000 volts output.

#### STEP . . . GAIN ADJUST

Turn ON all bits, adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

### FIGURE 6. OTHER VOLTAGE RANGES

The AD565 can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5 or ±2.5), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset either to ground for unipolar or to REF OUT for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 6.

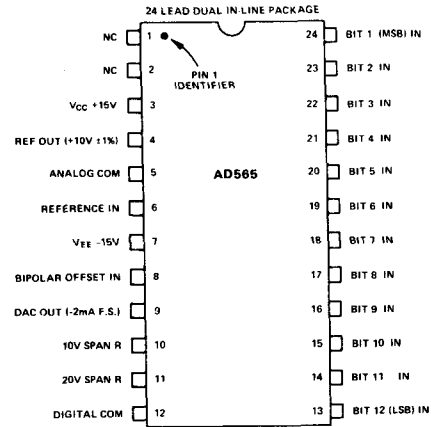


Figure 3.

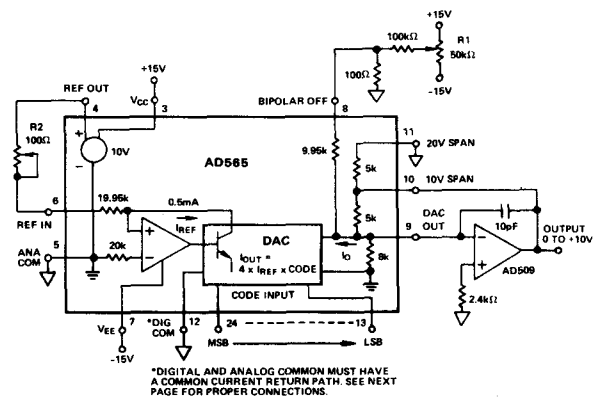


Figure 4. 0 to +10V Unipolar Voltage Output

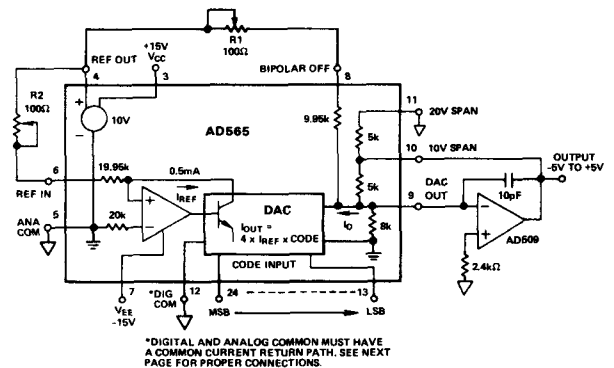


Figure 5. ±5V Bipolar Voltage Output

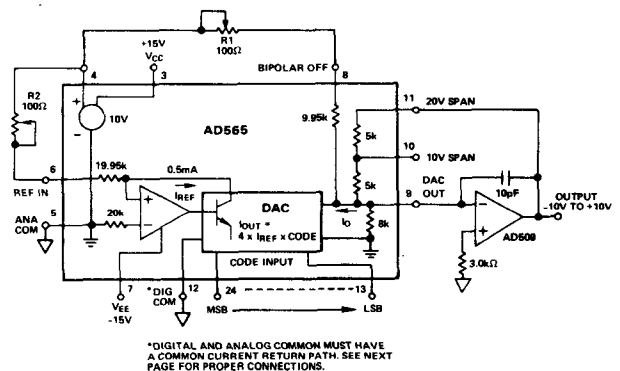


Figure 6. ±10V Voltage Output

### INTERNAL/EXTERNAL REFERENCE USE

The AD565 has an internal low-noise buried zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete zener reference diodes. The performance of the AD565 is specified with the internal reference driving the DAC since all trimming and testing (especially for full scale and bipolar) is done in this configuration.

The AD565 can be used with an external reference, but may not have sufficient trim range to accommodate a reference which does not match the internal reference. For external reference applications, the AD566 series is recommended.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5mA to Ref In and 1.0mA to Bipolar Offset, if used). A minimum of 1.5mA is available for driving external circuits. The reference is typically trimmed to  $\pm 0.2\%$ , then tested and guaranteed to  $\pm 1.0\%$  max error. The temperature coefficient is comparable to that of the full scale TC for a particular grade.

### DIGITAL INPUT CONSIDERATIONS

The AD565 uses a standard positive true straight binary code for unipolar outputs (all 1's give full scale output), and an offset binary code for bipolar output ranges. In the bipolar mode, with all 0's on the inputs, the output will go to negative full scale; with 100...00 (only the MSB on), the output will be 0.00 volts; with all 1's, the output will go to positive full scale.

The threshold of the digital input circuitry is set at 1.4 volts and does not vary with supply voltage. The input lines can interface with any type of 5 volt logic, TTL/DTL or CMOS, and have sufficiently low input currents to interface easily with unbuffered CMOS logic. The configuration of the input circuit is shown in Figure 7. The input line can be modelled as a 30k $\Omega$  resistance connected to a -0.7V rail.

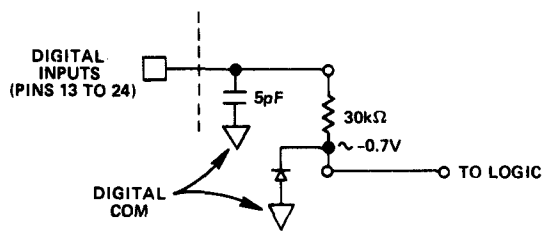


Figure 7. Equivalent Digital Input Circuit

### APPLICATION OF ANALOG AND DIGITAL COMMONS

The AD565 brings out separate analog and digital grounds to allow optimum connections for low noise and high speed performance. The two ground lines can be separated by up to 200 millivolts without any loss in performance. There may be some loss in linearity beyond that level. Up to  $\pm 1$  volt can be tolerated between the ground lines without damage to the device. If the AD565 is to be used in a system in which the two grounds will be ultimately connected at some distance from the device, it is recommended that parallel back-to-back diodes be connected between the ground lines near the device to prevent a fault condition.

The analog common at pin 5 is the ground reference point for the internal reference and is thus the "high quality" ground for the AD565; it should be connected directly to the analog refer-

ence point of the system. The digital common at pin 12 can be connected to the most convenient ground reference point; analog power return is preferred, but digital ground is acceptable. If digital common contains high frequency noise beyond 200mV, this noise may feed through the converter, so that some caution will be required in applying these grounds.

### OUTPUT VOLTAGE COMPLIANCE

The AD565 has a typical output compliance range from -2 to +10 volts. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8k in parallel with 25pF at the output terminal which produces an equivalent error current if the voltage deviates from analog common. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in nonlinear performance. Compliance limits are not affected by the positive power supply, but are a function of output current and negative supply, as shown in Figure 8.

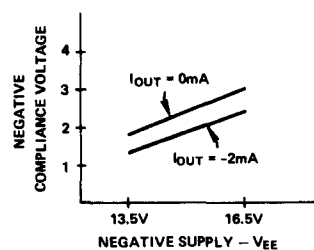


Figure 8. Typical Negative Compliance Range vs. Negative Supply

### MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD565, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further insure reliability, the AD565 is offered with 100% screening to MIL-STD-883, method 5004, Class B.

Table 1 details the test procedures of MIL-STD-883. Analog Devices subjects each part ordered with 883 screening to these tests on a 100% basis.

TABLE 1

| TEST                         | METHOD   |
|------------------------------|--|
| 1) Internal Visual (Pre cap) | 2010, Test Condition B   |
| 2) Stabilization Bake        | Method 1008, 24 hours @ +150°C                                 |
| 3) Temperature Cycling       | Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C      |
| 4) Constant Acceleration     | Method 2001, Test Condition E, Y1 plane, 30kg                  |
| 5) Seal, Fine and Gross      | Method 1014, Test Condition A and C                            |
| 6) Burn-in Test              | Method 1015, Test Condition B, 160 hours @ +125°C              |
| 7) Final Electrical Tests    | Performed 100% to all min and max specifications on data pages |
| 8) External Visual           | Method 2009  |

## SETTLING TIME

The high speed NPN current steering switching cell and internally compensated reference amplifier of the AD565 are specifically designed for fast settling operation. The typical settling time to  $\pm 0.01\%$  (1/2LSB) for the worst case transition (major carry or full scale step) is about 200ns; the lower order bits all settle in less than 200ns. (Worst case settling occurs when all bits are switched, especially the MSB).

The excellent high speed performance of the AD565 is demonstrated in these oscilloscope photographs. The measurements are made with the AD565 driving directly into an equivalent  $50\Omega$  load, and amplified with a low capacitance MOS-input, UHF amplifier. Both figures show the worst case situation, which is full scale transition from switching all bits OFF to ON.

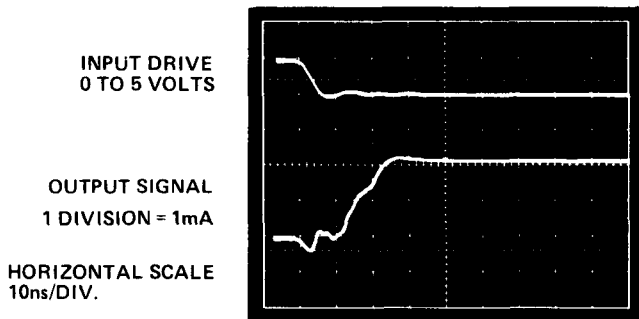


Figure 9. Full Scale Transition

The full transition characteristic is shown in Figure 9. There is about a 6-8ns delay, followed by a 10ns rise time and minimal overshoot. The transition in the other direction shows approximately a 20ns delay prior to a 10ns rise time. The slewing characteristics for smaller transitions show a similar characteristic.

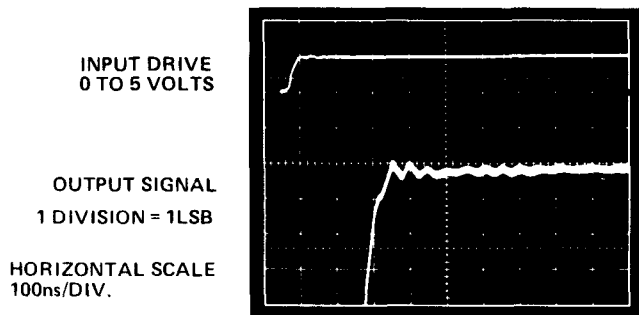


Figure 10. Settling Characteristic Detail

The fine detail of the full scale settling characteristic is shown in Figure 10. The equipment and circuitry used to make the measurements adds about 50ns to the actual device performance. The final portion of the signal slews to within 10LSB's in less than 150ns, reaches and stays within 1/2LSB in about 200ns, and shows less than 1/2LSB overshoot. The characteristic is completely settled out in less than 400ns.

## HIGH SPEED SYSTEM DESIGN

Full realization of this high speed performance requires strict attention to detail by the user in all areas of application and testing.

The settling time for the AD565 is specified in terms of the current output, an inherently high speed DAC operating mode.

However, most DAC applications require a current-to-voltage conversion at some point in the signal path, although an unbuffered voltage level (not using an op amp) is suitable for use in a successive-approximation A/D converter (see next page), or in many display applications. This form of current-to-voltage conversion can give very fast operation if proper design and layout is done. The fastest voltage conversion is achieved by connecting a low value resistor directly to the output, as shown in Figure 11. In this case, the settling time is primarily determined by the cell switching time and by the RC time constant of the AD565 output capacitance of 25 picofarads (plus stray capacitance) combined with the output resistor value. Settling to 0.01% of full scale (for a full scale transition) requires 9 time constants. This effect is important for an equivalent resistance over  $1k\Omega$ .

If an op amp must be used to provide a low impedance output signal, some loss in settling time will be seen due to op amp dynamics. The normal current-to-voltage converter op amp circuits are shown in the applications circuits on next page using the fast settling AD509. The circuits shown settle to  $\pm 1/2LSB$  in  $1\mu s$  unipolar or bipolar. The DAC output capacitance, which acts as a stray capacitance at the op amp inverting input, must be compensated by a feedback capacitor, as shown. The value should be chosen carefully for each application and each op amp type.

Fastest operation will be obtained by minimizing lead lengths, stray capacitance and impedance levels. Both supplies should be bypassed near the devices;  $0.1\mu F$  will be sufficient since the AD565 runs at constant supply current regardless of input code.

## DIRECT UNBUFFERED VOLTAGE OUTPUT FOR CABLE DRIVING

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 11 shows a connection using the gain and bipolar output resistors to give a  $\pm 1.60$  volt bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors ( $R_X$ ) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to  $-2mA$  unipolar output current and using the 10.0 volt reference voltage for bipolar offset. For example, setting  $R_X = 2.67k\Omega$  gives a  $\pm 1$  volt range with a  $1k\Omega$  equivalent output impedance.

This connection is especially useful for directly driving a long cable at high speed. Using a  $50\Omega$  resistor for  $R_X$  would allow interface to a  $50\Omega$  cable with a  $\pm 50mV$  full scale swing. Settling time would be very fast, as discussed in the section above.

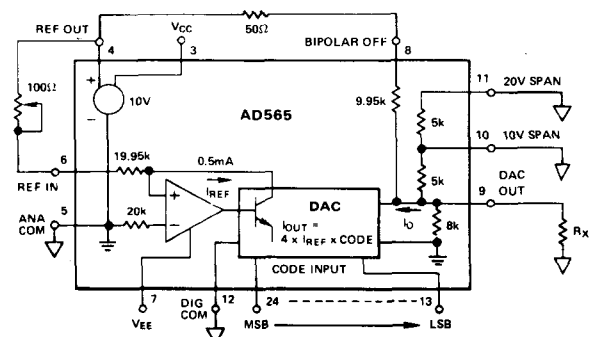


Figure 11. Unbuffered Bipolar Voltage Output

## HIGH SPEED 12-BIT A/D CONVERTERS

The fast settling characteristics of the AD565 make it ideal for high speed successive approximation A/D converters. The internal reference and trimmed application resistors allow a 12-bit converter system to be constructed with a minimum parts count. Shown in Figure 12 is a configuration using standard components; this system completes a full 12-bit conversion in  $10\mu\text{s}$  unipolar or bipolar. This converter will be accurate to  $\pm 1/2\text{LSB}$  of 12 bits and have a typical gain T.C. of  $10\text{ppm}/^\circ\text{C}$ .

In the unipolar mode, the system range is 0 to 9.9976 volts, with each bit having a value of 2.44mV. For true conversion accuracy, an A/D converter should be trimmed so that a given bit code output results from input levels from  $1/2\text{LSB}$  below to  $1/2\text{LSB}$  above the exact voltage which that code represents. Therefore, the converter zero point should be trimmed with an input voltage of +1.22mV; trim R1 until the LSB just begins to appear in the output code (all other bits "0"). For full scale, use an input voltage of +9.9963 volts (10 volts - 1LSB -  $1/2\text{LSB}$ ); then trim R2 until the LSB just begins to appear (all other bits "1").

The bipolar signal range is -5.0 to +4.9976 volts. Bipolar offset trimming is done by applying a -4.9988V input signal and trimming R1 for the LSB transition (all other bits "0").

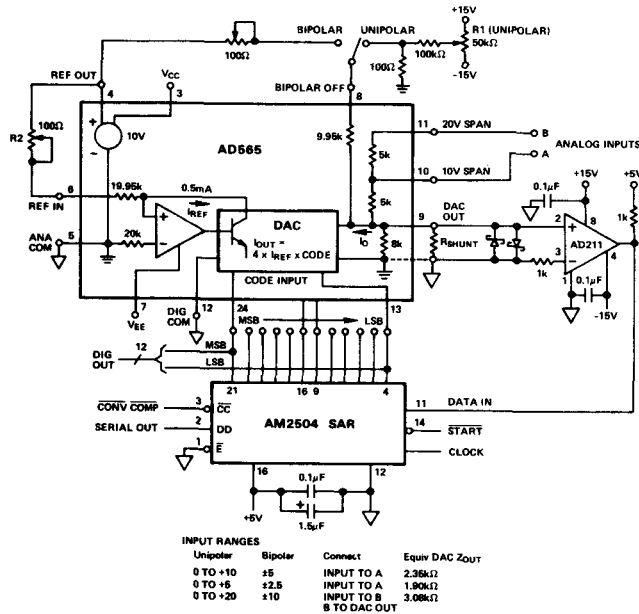


Figure 12. Fast Precision Analog to Digital Converter

Full scale is set by applying +4.9963 volts and trimming R2 for the LSB transition (all other bits "1"). In many applications, the pretrimmed application resistors are sufficiently accurate that external trimmers will be unnecessary, especially in situations requiring less than full 12-bit  $\pm 1/2\text{LSB}$  accuracy.

For fastest operation, the impedance at the comparator summing node must be minimized, as mentioned in the section on settling time. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance at the summing node of  $1\text{k}\Omega$ ,  $1\text{LSB} = 0.5\text{mV}$ ), to the point that comparator performance will be sacrificed. The contribution to this impedance from the DAC will vary with the input configuration, as shown in the input range table.

To prevent dynamic errors, the input signal should have a low dynamic source impedance, such as that of the AD509 high speed op amp.

## 128S D/A CONVERTERS

## HIGH-RESOLUTION CIRCUITS

16-bit resolution digital-to-analog converters can be built by cascading an AD565 12-bit DAC with an AD559 or AD1408 8-bit DAC. This technique can be used either to provide a 16-bit binary DAC or a 4-digit BCD\* DAC. By using an AD565K with  $\pm 1/8\text{LSB}$  typical linearity to 12 bits, the total circuit will typically achieve  $\pm 1/2\text{LSB}$  accuracy for 14 binary bits, and  $\pm 1/2$  least significant digit to 4 digits BCD. The binary configuration is shown in Figure 13. The AD559, with its thin film ladder network similar to the AD565, is preferred for good performance over temperature.

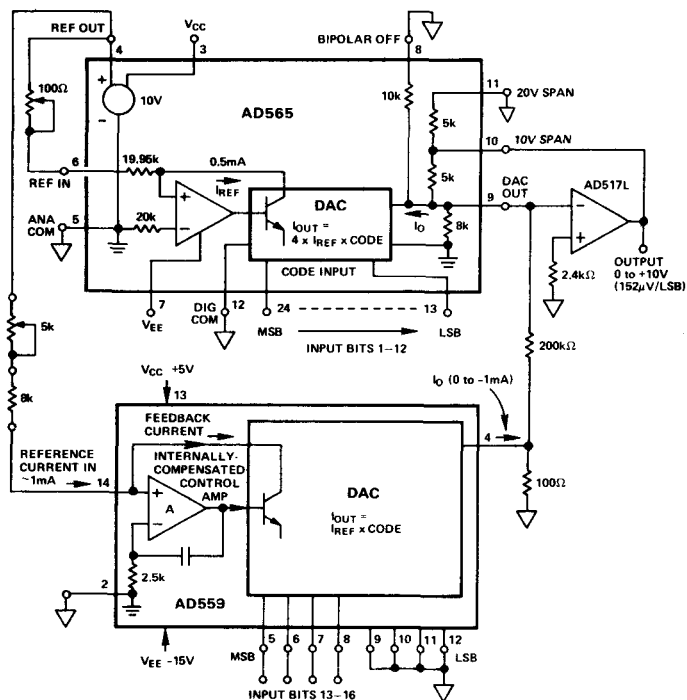


Figure 13. 16-Bit Binary DAC

## COMPLEMENTARY BINARY CODE CIRCUITS

The AD565 can be used in circuits where only a complementary binary code is available. This is done by connecting the 10 volt span resistor to the 10 volt reference and connecting the DAC output to a noninverting amplifier as shown in Figure 14. The  $8\text{k}\Omega$  DAC output impedance and the  $5\text{k}\Omega$  span resistor will form a divider which will give a full scale output voltage (with all bits off) to the amplifier of about 6.15 volts. To obtain a 10 volt full scale, the amplifier is shown with a gain network back to the inverting input.

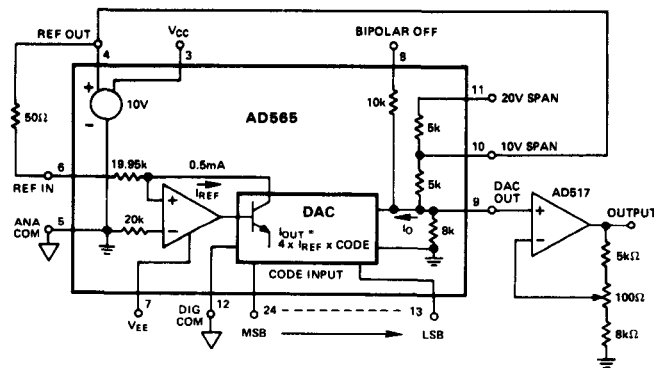
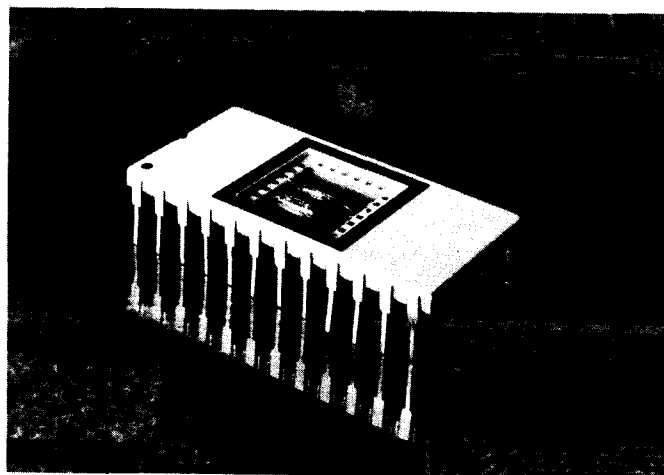


Figure 14. Complementary Output DAC

\*BCD units available July, 1979.

**PRELIMINARY TECHNICAL DATA****FEATURES****Single Chip Construction****Very High Speed: Settles to 1/2LSB in 200ns****Full Scale Switching Time: 30ns****Single Supply Operation****Monotonicity Guaranteed Over Temperature****Linearity Guaranteed Over Temperature – 1/2LSB max  
(AD566K, T)****Low Power: 180mW****Pin-Out Compatible with AD562****Low Cost****PRODUCT DESCRIPTION**

The AD566 is a fast 12-bit digital-to-analog converter which incorporates the latest advances in analog circuit design into a low power monolithic chip.

The AD566 chip uses 12 precision, high speed bipolar current steering switches, control amplifier and a laser-trimmed thin film resistor network to produce a very fast, high accuracy analog output current.

The combination of performance and flexibility in the AD566 has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). AD566 has a 10 – 90% full scale transition time under 35 nanoseconds and settles to within  $\pm 1/2$ LSB in 200 nanoseconds. The AD566 chips are laser-trimmed at the wafer level to  $\pm 1/8$ LSB typical linearity and are specified to  $\pm 1/4$ LSB max error (K and T grades) at +25°C. This high speed and accuracy make the AD566 the ideal choice for high speed display drivers as well as fast analog-to-digital converters.

The AD566 is available in four performance grades and two package types. The AD566J and K are specified for use over the 0 to +70°C temperature range and are available in either a 24-pin, hermetically-sealed, side-brazed ceramic DIP, or a 24-pin plastic DIP. The AD566S and T grades are specified for the -55°C to +125°C range and are available in the ceramic package.

**PRODUCT HIGHLIGHTS**

1. The combination of single supply operation with wide output compliance range allows optimum versatility in fast, low noise, accurate voltage output configurations without an output amplifier.
2. The device incorporates a newly developed\* fully differential, non-saturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562 with very fast switching times and an optimally-damped settling characteristic.
3. The chip also contains SiCr thin film application resistors which can be used with with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
4. The pin-out of the AD566 is compatible with the industry-standard AD562 so that a system can easily be upgraded to provide higher speed performance.
5. The single-chip construction makes the AD566 inherently more reliable than hybrid multi-chip designs. The AD566S and T grades with guaranteed linearity and monotonicity over the -55°C to +125°C range are especially recommended for high reliability needs in harsh environments. These units are available fully processed to MIL-STD-883, Level B.

\*Covered by patent numbers: 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and other patents pending.

# SPECIFICATIONS (T<sub>A</sub> = +25°C, V<sub>EE</sub> = -15V, unless otherwise specified)

| MODEL   | AD566J  |   |                 | AD566K                  |   |                 | UNITS                 |
|---|---|---|-----------------|-------------------------|---|-----------------|-----------------------|
|   | MIN   | TYP   | MAX             | MIN                     | TYP   | MAX             |                       |
| <b>DATA INPUTS (Pins 13 to 24)</b>  |   |   |                 |                         |   |                 |                       |
| TTL or 5 Volt CMOS (T <sub>min</sub> to T <sub>max</sub> )  |   |   |                 |                         |   |                 |                       |
| Input Voltage   |   |   |                 |                         |   |                 |                       |
| Bit ON Logic "1"  | +2.0  |   | +5.5            | +2.0                    |   | +5.5            | V                     |
| Bit OFF Logic "0"   | 0   |   | +0.8            | 0                       |   | +0.8            | V                     |
| Logic Current (each bit)  |   |   |                 |                         |   |                 |                       |
| Bit ON Logic "1"  |   | +120  | +300            |                         | +120  | +300            | μA                    |
| Bit OFF Logic "0"   |   | +35   | +100            |                         | +35   | +100            | μA                    |
| <b>RESOLUTION</b>   |   |   |                 |                         |   |                 |                       |
|   |   |   | 12              |                         |   | 12              | Bits                  |
| <b>OUTPUT</b>   |   |   |                 |                         |   |                 |                       |
| Current   |   |   |                 |                         |   |                 |                       |
| Unipolar (all bits on)  | -1.6  | -2.0  | -2.4            | -1.6                    | -2.0  | -2.4            | mA                    |
| Bipolar (all bits on or off)  | ±0.8  | ±1.0  | ±1.2            | ±0.8                    | ±1.0  | ±1.2            | mA                    |
| Resistance (exclusive of span resistors)  |   |   |                 |                         |   |                 |                       |
|   | 6k  | 8k  | 10k             | 6k                      | 8k  | 10k             | Ω                     |
| Offset  |   |   |                 |                         |   |                 |                       |
| Unipolar (adjustable to zero per Figure 5)  |   | 0.01  | 0.05            |                         | 0.01  | 0.05            | % of F.S.             |
| Bipolar (Figure 6 R <sub>1</sub> and R <sub>2</sub> = 50Ω fixed)  |   | 0.05  | 0.15            |                         | 0.05  | 0.1             | % of F.S.             |
| Capacitance   |   |   |                 |                         |   |                 |                       |
|   |   | 20  |                 |                         | 20  |                 | pF                    |
| Compliance Voltage  |   |   |                 |                         |   |                 |                       |
| T <sub>min</sub> to T <sub>max</sub>  | -1.5  |   | +10             | -1.5                    |   | +10             | V                     |
| <b>ACCURACY (error relative to full scale) +25°C</b>  |   |   |                 |                         |   |                 |                       |
|   |   | ±1/4<br>(0.006)   | ±1/2<br>(0.012) |                         | ±1/8<br>(0.003)   | ±1/4<br>(0.006) | LSB<br>% of F.S.      |
| T <sub>min</sub> to T <sub>max</sub>  |   | ±1/2<br>(0.012)   | ±3/4<br>(0.018) |                         | ±1/4<br>(0.006)   | ±1/2<br>(0.012) | LSB<br>% of F.S.      |
| <b>DIFFERENTIAL NONLINEARITY +25°C</b>  |   |   |                 |                         |   |                 |                       |
| T <sub>min</sub> to T <sub>max</sub>  | MONOTONICITY GUARANTEED                         |   | ±1/2<br>±3/4    | MONOTONICITY GUARANTEED |   | ±1/4<br>±1/2    | LSB                   |
| <b>TEMPERATURE COEFFICIENTS</b>   |   |   |                 |                         |   |                 |                       |
| Unipolar Zero   |   | 1   | 2               |                         | 1   | 2               | ppm/°C                |
| Bipolar Zero  |   | 5   | 10              |                         | 5   | 10              | ppm/°C                |
| Gain (Full Scale)   |   | 7   | 10              |                         | 2   | 3               | ppm/°C                |
| Differential Nonlinearity   |   | 2   |                 |                         | 2   |                 | ppm/°C                |
| <b>SETTLING TIME TO 1/2LSB</b>  |   |   |                 |                         |   |                 |                       |
| All Bits ON-to-OFF or OFF-to-ON   |   | 200   | 400             |                         | 200   | 400             | ns                    |
| <b>FULL SCALE TRANSITION</b>  |   |   |                 |                         |   |                 |                       |
| 10% to 90% Delay plus Rise Time   |   | 15  | 30              |                         | 15  | 30              | ns                    |
| 90% to 10% Delay plus Fall Time   |   | 30  | 50              |                         | 30  | 50              | ns                    |
| <b>POWER REQUIREMENTS</b>   |   |   |                 |                         |   |                 |                       |
| V <sub>EE</sub> , -13.5 to -16.5V dc  |   | -12   | -20             |                         | -12   | -20             | mA                    |
| <b>POWER SUPPLY GAIN SENSITIVITY</b>  |   |   |                 |                         |   |                 |                       |
| V <sub>EE</sub> = -15V, ±10%  |   | 15  | 25              |                         | 15  | 25              | ppm of F.S./%         |
| <b>PROGRAMMABLE OUTPUT</b>  |   |   |                 |                         |   |                 |                       |
| RANGE (see Figures 5, 6, 7)   |   | 0 to +5<br>-2.5 to +2.5<br>0 to +10<br>-5 to +5<br>-10 to +10 |                 |                         | 0 to +5<br>-2.5 to +2.5<br>0 to +10<br>-5 to +5<br>-10 to +10 |                 | V<br>V<br>V<br>V<br>V |
| <b>EXTERNAL ADJUSTMENTS</b>   |   |   |                 |                         |   |                 |                       |
| Gain Error with Fixed 50Ω Resistor for R <sub>2</sub> (Fig. 5)  |   | ±0.1  | ±0.25           |                         | ±0.1  | ±0.25           | % of F.S.             |
| Bipolar Zero Error with Fixed 50Ω Resistor for R <sub>1</sub> (Fig. 6)  |   | ±0.05   | ±0.15           |                         | ±0.05   | ±0.1            | % of F.S.             |
| Gain Adjustment Range (Fig. 5)  | ±0.25   |   |                 | ±0.25                   |   |                 | % of F.S.             |
| Bipolar Zero Adjustment Range   | ±0.15   |   |                 | ±0.15                   |   |                 | % of F.S.             |
| <b>REFERENCE INPUT</b>  |   |   |                 |                         |   |                 |                       |
| Input Impedance   | 15k   | 20k   | 25k             | 15k                     | 20k   | 25k             | Ω                     |
| <b>POWER DISSIPATION</b>  |   |   |                 |                         |   |                 |                       |
|   |   | 180   | 300             |                         | 180   | 300             | mW                    |
| <b>MULTIPLYING MODE PERFORMANCE (All Models)</b>  |   |   |                 |                         |   |                 |                       |
| Quadrants   | Two(2): Bipolar Operation at Digital Input Only |   |                 |                         |   |                 |                       |
| Reference Voltage   | +1V to +10V, Unipolar.                          |   |                 |                         |   |                 |                       |
| Reference Feedthrough (unipolar mode, all bits OFF, and 0 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough) | 40kHz typ                                       |   |                 |                         |   |                 |                       |
| Output Slew Rate 10%-90%  | 5mA/μs  |   |                 |                         |   |                 |                       |
| 90%-10%   | 1mA/μs  |   |                 |                         |   |                 |                       |
| <b>FULL POWER BANDWIDTH</b>   |   |   |                 |                         |   |                 |                       |
| Control Amplifier Small-Signal Closed-Loop Bandwidth  | 300kHz<br>1.8MHz                                |   |                 |                         |   |                 |                       |

Specifications subject to change without notice.

| MODEL   | MIN        | AD566S<br>TYP                                   | MAX                  | MIN        | AD566T<br>TYP           | MAX                  | UNITS            |
|---|------------|---|----------------------|------------|-------------------------|----------------------|------------------|
| <b>DATA INPUTS (Pins 13 to 24)</b>  |            |   |                      |            |                         |                      |                  |
| TTL or 5 Volt CMOS ( $T_{min}$ to $T_{max}$ )   |            |   |                      |            |                         |                      |                  |
| Input Voltage   |            |   |                      |            |                         |                      |                  |
| Bit ON Logic "1"  | +2.0       |   | +5.5                 | +2.0       |                         | +5.5                 | V                |
| Bit OFF Logic "0"   | 0          |   | +0.8                 | 0          |                         | +0.8                 | V                |
| Logic Current (each bit)  |            |   |                      |            |                         |                      |                  |
| Bit ON Logic "1"  |            | +120  | +300                 |            | +120                    | +300                 | $\mu$ A          |
| Bit OFF Logic "0"   |            | +35   | +100                 |            | +35                     | +100                 | $\mu$ A          |
| <b>RESOLUTION</b>   |            |   | 12                   |            |                         | 12                   | Bits             |
| <b>OUTPUT</b>   |            |   |                      |            |                         |                      |                  |
| Current   |            |   |                      |            |                         |                      |                  |
| Unipolar (all bits on)  | -1.6       | -2.0  | -2.4                 | -1.6       | -2.0                    | -2.4                 | mA               |
| Bipolar (all bits on or off)  | $\pm 0.8$  | $\pm 1.0$                                       | $\pm 1.2$            | $\pm 0.8$  | $\pm 1.0$               | $\pm 1.2$            | mA               |
| Resistance (exclusive of span resistors)  | 6k         | 8k  | 10k                  | 6k         | 8k                      | 10k                  | $\Omega$         |
| Offset  |            |   |                      |            |                         |                      |                  |
| Unipolar (adjustable to zero per Figure 5)  |            | 0.01  | 0.05                 |            | 0.01                    | 0.05                 | % of F.S.        |
| Bipolar (Figure 6 $R_1$ and $R_2 = 50\Omega$ fixed)   |            | 0.05  | 0.15                 |            | 0.05                    | 0.1                  | % of F.S.        |
| Capacitance   |            | 25  |                      |            | 25                      |                      | pF               |
| Compliance Voltage  |            |   |                      |            |                         |                      |                  |
| $T_{min}$ to $T_{max}$  | -1.5       |   | +10                  | -1.5       |                         | +10                  | V                |
| <b>ACCURACY (error relative to full scale) +25°C</b>  |            |   |                      |            |                         |                      |                  |
|   |            | $\pm 1/8$<br>(0.003)                            | $\pm 1/2$<br>(0.006) |            | $\pm 1/8$<br>(0.003)    | $\pm 1/4$<br>(0.006) | LSB<br>% of F.S. |
| $T_{min}$ to $T_{max}$  |            | $\pm 1/2$<br>(0.012)                            | $\pm 3/4$<br>(0.018) |            | $\pm 1/4$<br>(0.006)    | $\pm 1/2$<br>(0.012) | LSB<br>% of F.S. |
| <b>DIFFERENTIAL NONLINEARITY +25°C</b>  |            |   |                      |            |                         |                      |                  |
| $T_{min}$ to $T_{max}$  |            | $\pm 1/2$                                       | $\pm 3/4$            |            | $\pm 1/4$               | $\pm 1/2$            | LSB              |
|   |            | MONOTONICITY GUARANTEED                         |                      |            | MONOTONICITY GUARANTEED |                      |                  |
| <b>TEMPERATURE COEFFICIENTS</b>   |            |   |                      |            |                         |                      |                  |
| Unipolar Zero   |            | 1   | 2                    |            | 1                       | 2                    | ppm/°C           |
| Bipolar Zero  |            | 5   | 10                   |            | 5                       | 10                   | ppm/°C           |
| Gain (Full Scale)   |            | 7   | 10                   |            | 2                       | 3                    | ppm/°C           |
| Differential Nonlinearity   |            | 2   |                      |            | 2                       |                      | ppm/°C           |
| <b>SETTLING TIME TO 1/2LSB</b>  |            |   |                      |            |                         |                      |                  |
| All Bits ON-to-OFF or OFF-to-ON   |            | 200   | 400                  |            | 200                     | 400                  | ns               |
| <b>FULL SCALE TRANSITION</b>  |            |   |                      |            |                         |                      |                  |
| 10% to 90% Delay plus Rise Time   |            | 15  | 30                   |            | 15                      | 30                   | ns               |
| 90% to 10% Delay plus Fall Time   |            | 30  | 50                   |            | 30                      | 50                   | ns               |
| <b>POWER REQUIREMENTS</b>   |            |   |                      |            |                         |                      |                  |
| $V_{EE}$ , -13.5 to -16.5V dc   |            | -12   | -20                  |            | -12                     | -20                  | mA               |
| <b>POWER SUPPLY GAIN SENSITIVITY</b>  |            |   |                      |            |                         |                      |                  |
| $V_{EE} = -15V, \pm 10\%$   |            | 15  | 25                   |            | 15                      | 25                   | ppm of F.S./%    |
| <b>PROGRAMMABLE OUTPUT RANGE (see Figures 5, 6, 7)</b>  |            |   |                      |            |                         |                      |                  |
|   |            | 0 to +5   |                      |            | 0 to +5                 |                      | V                |
|   |            | -2.5 to +2.5                                    |                      |            | -2.5 to +2.5            |                      | V                |
|   |            | 0 to +10  |                      |            | 0 to +10                |                      | V                |
|   |            | -5 to +5  |                      |            | -5 to +5                |                      | V                |
|   |            | -10 to +10                                      |                      |            | -10 to +10              |                      | V                |
| <b>EXTERNAL ADJUSTMENTS</b>   |            |   |                      |            |                         |                      |                  |
| Gain Error with Fixed 50 $\Omega$ Resistor for R2 (Fig. 5)  |            | $\pm 0.1$                                       | $\pm 0.25$           |            | $\pm 0.1$               | $\pm 0.25$           | % of F.S.        |
| Bipolar Zero Error with Fixed 50 $\Omega$ Resistor for R1 (Fig. 6)  |            | $\pm 0.05$                                      | $\pm 0.15$           |            | $\pm 0.05$              | $\pm 0.1$            | % of F.S.        |
| Gain Adjustment Range (Fig. 5)  | $\pm 0.25$ |   |                      | $\pm 0.25$ |                         |                      | % of F.S.        |
| Bipolar Zero Adjustment Range   | $\pm 0.15$ |   |                      | $\pm 0.15$ |                         |                      | % of F.S.        |
| <b>REFERENCE INPUT</b>  |            |   |                      |            |                         |                      |                  |
| Input Impedance   | 15k        | 20k   | 25k                  | 15k        | 20k                     | 25k                  | $\Omega$         |
| <b>POWER DISSIPATION</b>  |            |   |                      |            |                         |                      |                  |
|   |            | 180   | 300                  |            | 180                     | 300                  | mW               |
| <b>MULTIPLYING MODE PERFORMANCE (All Models)</b>  |            |   |                      |            |                         |                      |                  |
| Quadrants   |            | Two(2): Bipolar Operation at Digital Input Only |                      |            |                         |                      |                  |
| Reference Voltage   |            | +1V to +10V, Unipolar.                          |                      |            |                         |                      |                  |
| Reference Feedthrough (unipolar mode, all bits OFF, and 0 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough) |            | 40kHz typ                                       |                      |            |                         |                      |                  |
| Output Slew Rate 10%-90%  |            | 5mA/ $\mu$ s                                    |                      |            |                         |                      |                  |
| 90%-10%   |            | 1mA/ $\mu$ s                                    |                      |            |                         |                      |                  |
| <b>FULL POWER BANDWIDTH</b>   |            |   |                      |            |                         |                      |                  |
| Control Amplifier Small-Signal Closed-Loop Bandwidth  |            | 300kHz  |                      |            |                         |                      |                  |
|   |            | 1.8MHz  |                      |            |                         |                      |                  |

Specifications subject to change without notice.





### THE AD566 OFFERS TRUE 12-BIT PERFORMANCE

**ACCURACY:** Analog Devices defines accuracy as the maximum deviation of the actual, adjusted DAC output (see page 6) from the ideal analog output (a straight line drawn from 0 to F.S. - 1LSB) for any bit combination. The AD566 is laser trimmed to 1/4LSB (0.025% of F.S.) maximum error at +25°C for the K and T version and to 1/2LSB for the J and S versions.

**MONOTONICITY:** A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a non-decreasing function of the input. All versions of the AD566 are monotonic over their entire operating temperature range.

**DIFFERENTIAL NONLINEARITY:** Monotonic behavior requires that the differential nonlinearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, if a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential nonlinearity error would be 1.83mV, or 3/4LSB. The AD566K and T have a max differential linearity error of 1/2LSB, which is a tighter specification than simply guaranteed monotonicity.

### ANALYZING DEVICE ACCURACY OVER THE TEMPERATURE RANGE

For the purposes of temperature drift analysis, the major device components are shown in Figure 3.

The input reference current to the DAC,  $I_{REF}$ , is developed from the external reference and will show the same drift rate as the reference voltage. The DAC output current,  $I_{DAC}$  which is a function of the digital input code, is designed to track  $I_{REF}$ ; if there is a slight mismatch in these currents over temperature, it will contribute to the gain T.C. The bipolar offset resistor,  $R_{BP}$ , and gain setting resistor,  $R_{GAIN}$ , also have temperature coefficients which contribute to system drift errors.

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input which calls for zero output to a point which is defined as full scale. A specification for total error over temperature assumes that both the zero and full scale points have been trimmed for zero error at +25°C. Total error is normally expressed a percentage of the full scale range. In the bipolar situation, this means the total range from  $-V_{FS}$  to  $+V_{FS}$ .

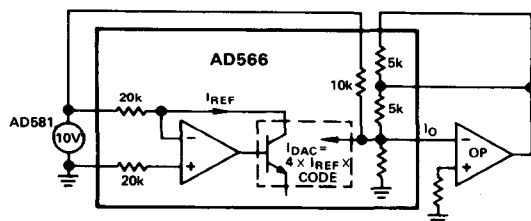


Figure 3. Bipolar Configuration

### MONOTONICITY AND LINEARITY

The initial linearity error of  $\pm 1/2$ LSB max and the differential linearity error of  $\pm 3/4$ LSB max guarantee monotonic performance over the range of  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . It can, therefore, be assumed that linearity errors are insignificant in computation of total temperature errors.

### UNIPOLAR ERRORS

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift of  $2\text{ppm}/^{\circ}\text{C}$  max (which comes from leakage currents) causes a linear shift in the transfer curve as shown in Figure 4. The gain drift causes a change in the slope of the curve which results from reference drift and the device gain drift. The device gain drift is the DAC drift and drift in  $R_{GAIN}$  relative to the DAC resistors for a total of  $10\text{ppm}/^{\circ}\text{C}$  max. Total absolute error due to all of these effects is guaranteed to be less than  $\pm 0.018\%$  of full scale from  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### BIPOLAR RANGE ERRORS

The analysis is slightly more complex in the bipolar mode. In this mode  $R_{BP}$  is connected to  $V_{REF}$  (see Figure 3) to generate a current which exactly balances the current of the MSB so that the output voltage is zero with the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in  $I_{REF}$  and thus  $I_{DAC}$ , so that  $I_{DAC}$  will always be exactly balanced by  $I_{BP}$  with the MSB turned on. This effect is shown in Figure 4. The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts discussed before will have the same effect on the bipolar offset. A mismatch of  $R_{BP}$  to the DAC resistors is usually the largest component of bipolar drift, but in the AD566 this error is held to  $10\text{ppm}$  max. The total of all these errors is held to  $\pm 0.39\%$  of full scale from  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Note that, in the bipolar ranges, full scale is defined as the total range from  $-V_{FS}$  to  $+V_{FS}$ .

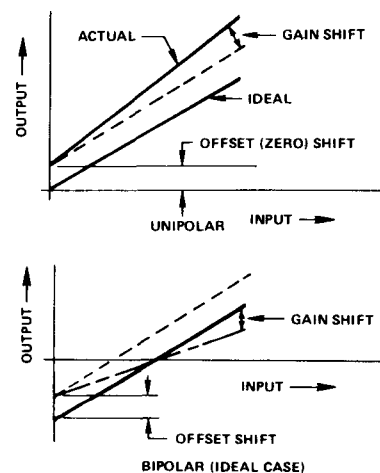


Figure 4. Unipolar and Bipolar Drifts

## CONNECTING THE AD566 FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50Ω fixed resistor is substituted for the 100Ω trimmer, unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

### FIGURE 5 UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 7, should be grounded if not used for trimming.

#### STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 7 should then be connected to pin 3.

#### STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer, R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

### FIGURE 6. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

#### STEP 1 . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1, to give -5.000 output volts.

#### STEP II . . . GAIN ADJUST

Turn ON all bits, adjust 100Ω gain trimmer R<sub>2</sub> to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

### FIGURE 7. OTHER VOLTAGE RANGES

The AD566 can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5V or +2.5V), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset resistor either to ground for unipolar or to V<sub>REF</sub> for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 7.

| DIGITAL INPUT |     | ANALOG OUTPUT   |                    |               |
|---------------|-----|-----------------|--------------------|---------------|
| MSB           | LSB | Straight Binary | Offset Binary      | Two's Compl.* |
| 000000000000  |     | Zero            | -Full Scale        | Zero          |
| 011111111111  |     | Mid Scale -1LSB | FS -1LSB           | +FS -1LSB     |
| 100000000000  |     | +1/2 FS         | Zero               | -FS           |
| 111111111111  |     | +FS -1LSB       | + Full Scale -1LSB | +FS -1LSB     |

\*Invert the MSB of the offset binary code with an external inverter to obtain two's complement.

Table 2. Digital Input Codes

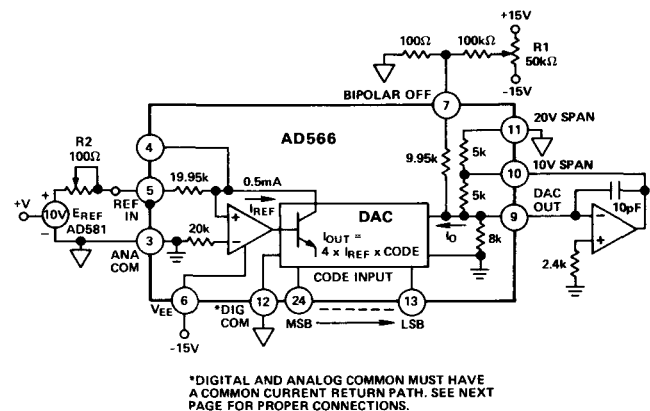


Figure 5. 0 to +10V Unipolar Voltage Output

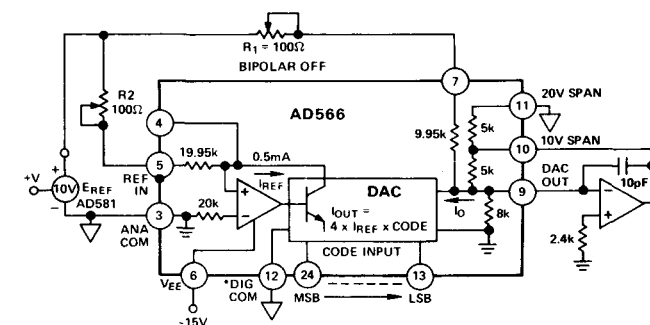


Figure 6. ±5V Bipolar Voltage Output

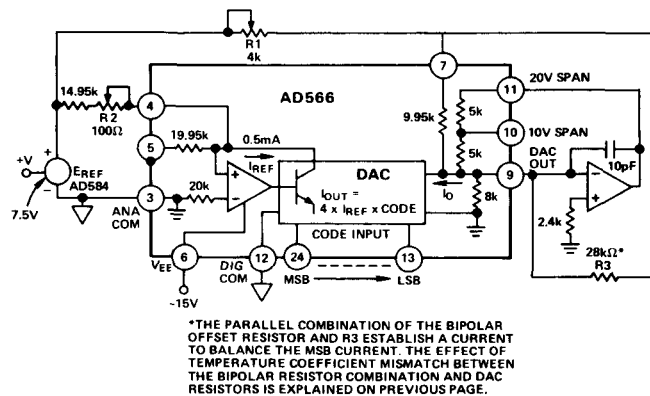


Figure 7. ±10V Voltage Output

## DIGITAL INPUT CONSIDERATIONS

The threshold of the digital input circuitry is set at 2.0 volts and does not vary with supply voltage. The input lines can interface with any type of 5 volt logic, TTL/DTL or CMOS, and have sufficiently low input currents to interface easily with unbuffered CMOS logic. The configuration of the input circuit is shown in Figure 8. The input line can be modelled as a  $30\text{k}\Omega$  resistance connected to a  $-0.7\text{V}$  rail.

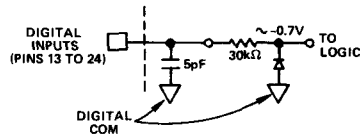


Figure 8. Equivalent Digital Input Circuit

## APPLICATION OF ANALOG AND DIGITAL COMMONS

The AD566 brings out separate analog and digital grounds to allow optimum connections for low noise and high speed performance. The two ground lines can be separated by up to 200 millivolts without any loss in performance. There may be some loss in linearity beyond that level. Up to  $\pm 1$  volt can be tolerated between the ground lines without damage to the device. If the AD566 is to be used in a system in which the two grounds will be ultimately connected at some distance from the device, it is recommended that parallel back-to-back diodes be connected between the ground lines near the device to prevent a fault condition.

The analog common at pin 3 is the ground reference point for the internal reference and is thus the "high quality" ground for the AD566; it should be connected directly to the analog reference point of the system. The digital common at pin 12 can be connected to the most convenient ground reference point; analog power return is preferred, but digital ground is acceptable. If digital common contains high frequency noise in excess of 200mV, this noise may feed through to the output of the converter, therefore some caution is required in applying these grounds.

## OUTPUT VOLTAGE COMPLIANCE

The AD566 has a typical output compliance range of  $-2$  to  $+10$  volts. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of  $8\text{k}\Omega$  in parallel with  $25\text{pF}$  at the output terminal which produces an equivalent error current if the voltage deviates from analog common. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in nonlinear performance. Compliance limits are a function of output current and negative supply, as shown in Figure 9.

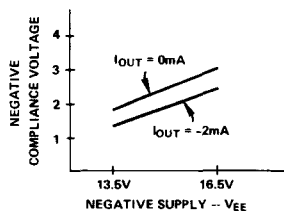


Figure 9. Typical Neg. Compliance Range vs. Neg. Supply

## HIGH SPEED SYSTEM DESIGN

Full realization of the AD566 high speed capabilities requires strict attention to detail by the user in all areas of application and testing.

The settling time for the AD566 is specified for the current output, an inherently high speed DAC operating mode. However, most DAC applications require a current-to-voltage conversion at some point in the signal path, although an unbuffered voltage level (not using an op amp) is suitable for use in a successive-approximation A/D converter (see next page), or in many display applications. With proper design this form of current-to-voltage conversion can give very fast operation. The fastest voltage conversion is achieved by connecting a low value resistor directly to the output, as shown in Figure 10. In this case, the settling time is primarily determined by the cell switching time and by the RC time constant of the AD566 output capacitance of 25 picofarads (plus stray capacitance) combined with the output resistor value. Settling to 0.01% of full scale (for a full scale transition) requires 9 time constants. This effect is important for an equivalent resistance over  $1\text{k}\Omega$ .

If an op amp is used to provide a low impedance output signal, some loss in settling time will be seen due to op amp dynamics. The normal current-to-voltage converter op amp circuits, based on the fast settling AD509 are shown in the applications circuits on Performance page. The unipolar or bipolar circuits shown settle to  $\pm 1/2\text{LSB}$  in  $1\mu\text{s}$ . The DAC output capacitance, which acts as a stray capacitance at the op amp inverting input, must be compensated by a feedback capacitor, as shown. The value should be chosen carefully for each application and each op amp type.

Fastest operation will be obtained by minimizing lead lengths, stray capacitance and impedance levels. The supply should be bypassed near the device;  $0.1\mu\text{F}$  will be sufficient since the AD566 runs at constant supply current regardless of input code. Output capacitance can be minimized by grounding pin 11 in 10V span applications.

## DIRECT UNBUFFERED VOLTAGE OUTPUT FOR CABLE DRIVING

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 10 shows a connection using the gain and bipolar output resistors to give a  $\pm 1.60$  volt bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors ( $R_X$ ) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to  $-2\text{mA}$  unipolar output current and using the 10.0 volt reference voltage for bipolar offset. For example, setting  $R_X = 2.67\text{k}\Omega$  gives a  $\pm 1$  volt range with a  $1\text{k}\Omega$  equivalent output impedance.

This connection is especially useful for directly driving a long cable at high speed. A  $50\Omega$   $R_X$  resistor drives a  $50\Omega$  cable with a  $\pm 50\text{mV}$  full scale swing; settling time is very fast as discussed in the section above.

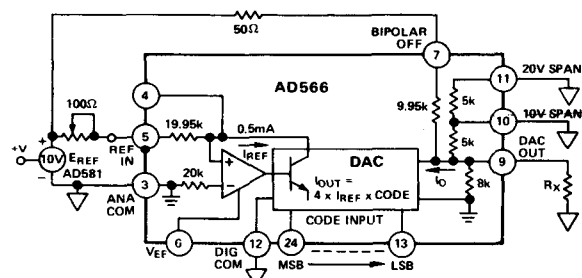


Figure 10. Unbuffered Bipolar Voltage Output

### MICROPROCESSOR CONTROL FOR A 12-BIT DAC

A common I/O interface is the Digital-to-Analog Converter output, which provides a voltage corresponding to a data word from a microprocessor.

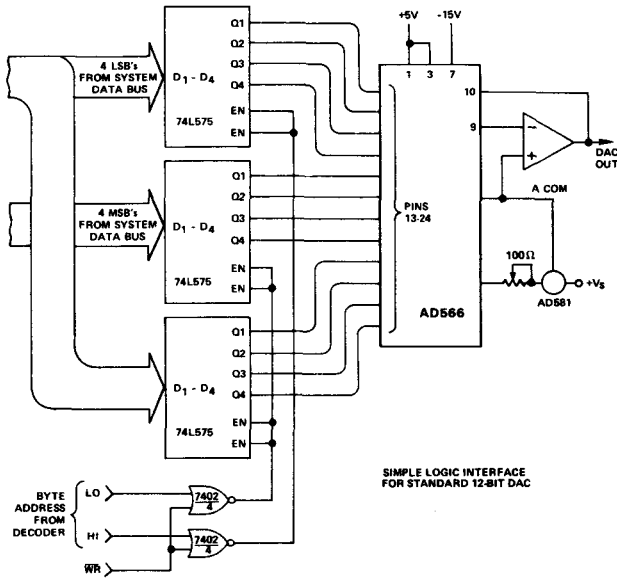


Figure 11.

A complex situation arises when the data for the DAC needs more bits of resolution than the system data bus can carry in 1 byte. For example, applications using an 8-bit microprocessor is often required to drive a 12-bit DAC. Several hardware formats are possible; the most convenient one depends on the desired data format. If the most significant 8 bits are in one byte of memory, they can be transferred into an 8-bit latch in one memory-or I/O-write cycle. An adjacent cycle can be used to transfer the 4 most-significant bits of another data word into a latch controlling the 4 least-significant bits of the DAC. The most-significant bits of the data bus drive two separately controlled 4-bit latches which are controlled by two separate addresses. The Hi Byte address allows the microprocessor to write in the 8 most significant data bits and the Lo Byte address allows the microprocessor to write in the 4 remaining bits. When all 12 bits are latched, the DAC output will assume its proper new value. An intermediate value will be momentarily present at the DAC terminals between Hi and Lo Byte write cycles. For applications such as CRT displays where this intermediate value cannot be tolerated, double buffering can be effectively employed. This could be implemented with a separately-controlled 12-bit latch at the DAC inputs.

### D/A CONVERTERS IN DISPLAYS

In Figure 12, a counter-driven AD566 is shown as a sawtooth sweep generator. When used for displays, this scheme provides a highly-repeatable, controllable linear sweep.

Raster displays are usually generated by a fast horizontal scan and a slower vertical scan which is derived from the horizontal scan. Intensity modulation during each horizontal scan provides the pictorial information. The picture resolution is expressed in terms of the number of discernible data points per line multiplied by the number of lines. The minimum frame period is the time allowed for the horizontal scan-plus-retrace multiplied by the number of lines, plus vertical retrace time.

A family of monolithic D/A converters is available from Analog Devices that are suitable for verticle sweeps. The line-spacing uniformity depends on linearity while maximum number of lines depends on DAC resolution. A display of 1024 lines would require 10 bits of resolution and 12 bits of linearity (0.012% of linearity provides less than 12% of spacing error). Switching transients created within the vertical sweep DAC are blanked because they occur during the horizontal retrace interval.

For horizontal sweeps, the DAC requirements are more severe. For example, to resolve 500 points per line, at 500 lines per frame, at a 30Hz frame rate, requires that each digital horizontal step settle within 100ns (typical full scale settling time is 200ns), and that there be no "glitches". Even if the display is blanked between horizontal steps, large glitches at major carriers can cause deflection-amplifier transients, which distort the pattern.

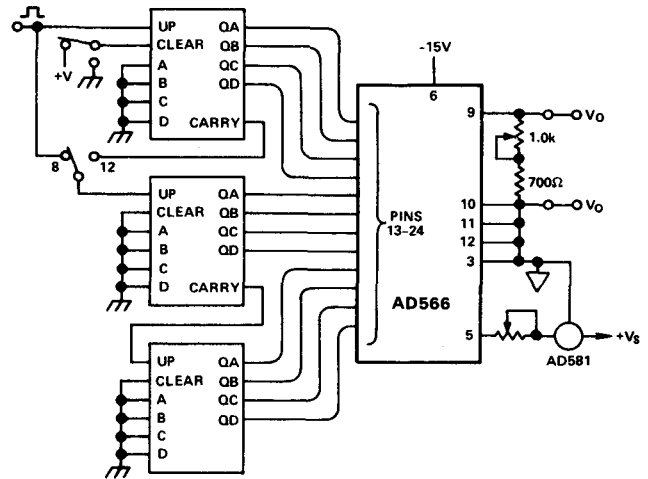


Figure 12.

The excellent high speed performance of the AD566 is demonstrated in the oscilloscope photograph of Figure 13. This measurement is made with the AD566 driving directly into an equivalent 50Ω load, amplified with a low capacitance MOS-input, UHF amplifier. The figure shows the worst case situation, which is full scale transition from switching all bits OFF to ON. The equipment and circuitry used to make the measurements adds about 50ns to the actual device performance.

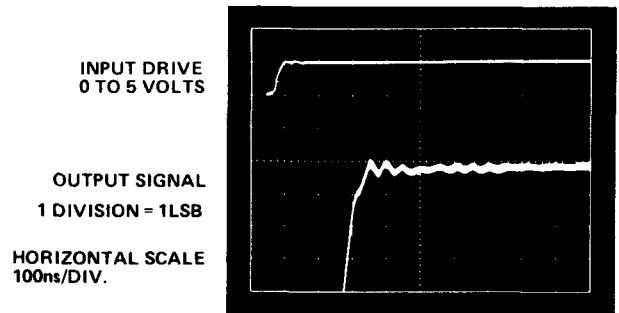


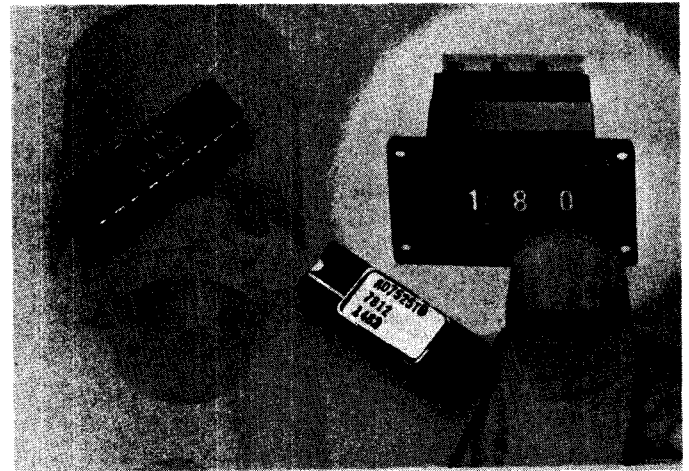
Figure 13. Settling Characteristic Detail

### FEATURES

Resolution: 3 1/2 Digit BCD (1999 Counts)  
Accuracy:  $\pm 0.2\%$   
Excellent Repeatability Accuracy  
Low Power Dissipation

### APPLICATIONS

Thumbwheel Switch Voltage Dividers  
Digitally Controlled Gain Circuits  
Digitally Controlled Attenuators  
BCD Multiplying DAC's  
Low Power Converters



### GENERAL DESCRIPTION

The AD7525 is a monolithic CMOS 3 1/2 digit BCD digitally controlled potentiometer designed for precision incremental voltage-divider applications.

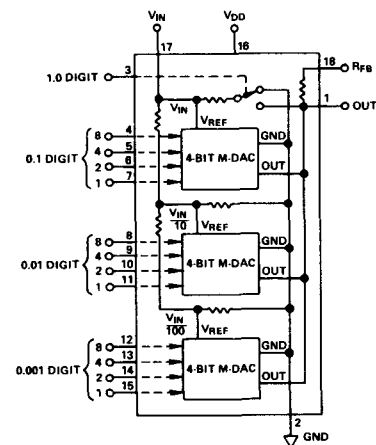
With the addition of an external op amp, the output can be digitally controlled from 0 to 19.99V in 10mV increments with a 10V input.

AC or DC voltage up to  $\pm 25V$  can be applied to the input providing high application flexibility in fields such as audio gain control, etc.

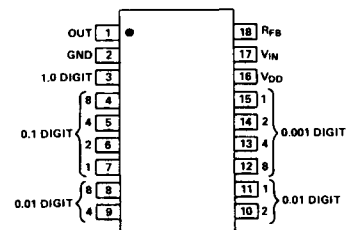
Digital control, excellent repeatability and 0.2% accuracy make the AD7525 an ideal replacement for 10-turn potentiometers or thumbwheel switch voltage dividers using discrete resistor networks.

Packaged in an 18-pin DIP, the AD7525 uses an advanced CMOS fabrication process combined with wafer laser trimming.

### FUNCTIONAL DIAGRAM



### PIN CONFIGURATION



### ORDERING INFORMATION

#### Temperature Range and Package

| Plastic<br>0 to +70°C | Ceramic<br>-25°C to +85°C | Ceramic<br>-55°C to +125°C |
|-----------------------|---------------------------|----------------------------|
| AD7525KN              | AD7525BD<br>AD7525BD/883B | AD7525TD<br>AD7525TD/883B  |

# SPECIFICATIONS

( $V_{DD} = +15V$ ;  $V_{PIN1} = 0V$ ;  $V_{IN} = +10V$  unless otherwise stated)

| PARAMETER  | $T_A = +25^\circ C$                                 | $T_A = \text{Operating Temperature Range}$          | CONDITION   |
|--|---|---|---|
| <b>ACCURACY</b>                                    |   |   |   |
| Resolution <sup>1</sup>                            | 1 part in 2000                                      | 1 part in 2000                                      |   |
| Absolute Accuracy Error <sup>2</sup>               | $\pm 0.2\%V_{IN}$ max                               | $\pm 0.3\%V_{IN}$ max                               | BCD 0000 to 1999  |
| <b>DYNAMIC PERFORMANCE</b>                         |   |   |   |
| Switching Time                                     | $1\mu s$ max <sup>3</sup>                           | $1\mu s$ max <sup>4</sup>                           | $V_{IN} = +5V$ , $R_{OUT}$ (pin 1) = $100\Omega$ , Digital Inputs = $V_{IL}$ to $V_{IH}$ or $V_{IH}$ to $V_{IL}$ . $V_{PINS}$ measured from 10% to 90%<br>$V_{IN} = \pm 10V$ , 20kHz sinewave |
| Feedthrough Error                                  | $\pm 0.05\%V_{IN}$ max <sup>4</sup>                 | $\pm 0.1\%V_{IN}$ max <sup>4</sup>                  |   |
| <b>ANALOG INPUT</b>                                |   |   |   |
| Input Resistance (pin 17) <sup>5</sup>             | $2k\Omega$ min/ $10k\Omega$ max                     | $2k\Omega$ min/ $10k\Omega$ max                     |   |
| $V_{IN}$ Range (max recommended)                   | $\pm 10V$ max                                       | $\pm 10V$ max                                       |   |
| <b>ANALOG OUTPUT</b>                               |   |   |   |
| Output Capacitance<br>$C_{OUT}$ (pin 1)            | $60pF$ max <sup>4</sup><br>$200pF$ max <sup>4</sup> | $60pF$ max <sup>4</sup><br>$200pF$ max <sup>4</sup> | Digital Inputs = BCD 0000<br>Digital Inputs = BCD 1999  |
| $R_{FB}$ Resistance (pin 18 to pin 1) <sup>5</sup> | $8k\Omega$ min/ $32k\Omega$ max                     | $8k\Omega$ min/ $32k\Omega$ max                     |   |
| <b>DIGITAL INPUTS</b>                              |   |   |   |
| Input HIGH Voltage<br>$V_{IH}$                     | +14.5V min  | +14.5V min  |   |
| Input LOW Voltage<br>$V_{IL}$                      | +0.5V max   | +0.5V max   |   |
| Input Leakage Current                              | $\pm 1\mu A$ max                                    | $\pm 10\mu A$ max                                   | Digital Input = 0V or $V_{DD}$  |
| Input Capacitance                                  | $5pF$ max <sup>4</sup>                              | $5pF$ max <sup>4</sup>                              |   |
| Input Coding                                       | $3\frac{1}{2}$ Digit BCD (1999 Counts)              | $3\frac{1}{2}$ Digit BCD (1999 Counts)              |   |
| <b>POWER SUPPLY</b>                                |   |   |   |
| $V_{DD}$ Range                                     | +5V to +17V   | +5V to +17V   | Functional with Degraded Performance  |
| $V_{DD}$   | +15V $\pm 5\%$                                      | +15V $\pm 5\%$                                      | Rated Accuracy  |
| $I_{DD}$   | 500 $\mu A$ max                                     | 1mA max   | Digital Inputs = $V_{IL}$ or $V_{IH}$   |

## NOTES:

<sup>1</sup> Commercial devices are sample tested over temperature.

<sup>2</sup> Absolute accuracy is measured using the AD7525 internal feedback resistor.

<sup>3</sup> AC parameter, sample tested at +25°C to ensure conformance to specification.

<sup>4</sup> Guaranteed, not tested.

<sup>5</sup> Thin film resistor temperature coefficient is approximately -300ppm/°C.

Specifications subject to change without notice.

## CAUTION

1. ESD (electro-static discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.
2. Do not apply voltages more negative than GND or more positive than  $V_{DD}$  to any pin except  $V_{IN}$  (pin 17) and  $R_{FB}$  (pin 18).
3. The inputs of some IC amplifiers (especially high speed types) present a low impedance to  $V-$  during power sequencing. To prevent the AD7525 OUT terminal (pin 1) from exceeding  $-300mV$  (which causes catastrophic substrate current), a Schottky diode, HP5082-2811 or equivalent, is recommended. While not required for most amplifier types, provision for the diode should be made during layout. The diode should be connected between OUT (pin 1) and GND (pin 2) as shown in Figure 4, page 141S.

## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ C$  unless otherwise noted)

|  |                     |
|--|---------------------|
| $V_{DD}$ (to GND) . . . . .              | $-0.3V, +17V$       |
| $V_{IN}$ (to GND) . . . . .              | $\pm 25V$           |
| $R_{FB}$ (to GND) . . . . .              | $\pm 25V$           |
| Digital Input Voltage (to GND) . . . . . | $-0.3V$ to $V_{DD}$ |
| $V_{PIN1}$ (to GND) . . . . .            | $-0.3V$ to $V_{DD}$ |
| Power Dissipation (Package)              |                     |

Plastic (Suffix N)

|  |                   |
|--|-------------------|
| To $+70^\circ C$ . . . . .               | 670mW             |
| Derates above $+70^\circ C$ by . . . . . | $.8.3mW/^\circ C$ |

Ceramic (Suffix D)

|  |                 |
|--|-----------------|
| To $+75^\circ C$ . . . . .               | 450mW           |
| Derates above $+75^\circ C$ by . . . . . | $.6mW/^\circ C$ |

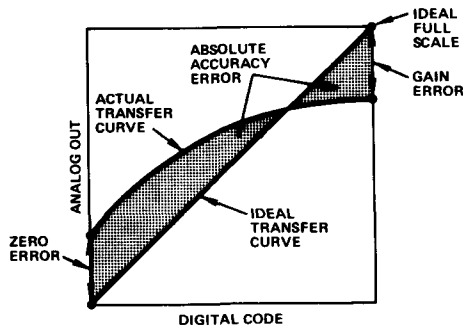
Operating Temperature

|   |                                 |
|---|---------------------------------|
| Commercial Plastic (KN Version) . . . . . | $0^\circ C$ to $+70^\circ C$    |
| Industrial Ceramic (BD Version) . . . . . | $-25^\circ C$ to $+85^\circ C$  |
| Military Ceramic (TD Version) . . . . .   | $-55^\circ C$ to $+125^\circ C$ |

## TERMINOLOGY

**SWITCHING TIME:** In a D/A converter, the switching time is the time taken for an analog switch to change to a new state from the previous one. It includes delay time, and rise time from 10% to 90%, but does not include settling time, which is a function of the output amplifier used.

**ABSOLUTE ACCURACY ERROR:** Deviation of the actual transfer curve (uncalibrated) from the ideal transfer curve. It is expressed as a percentage of the input voltage.



*Absolute Accuracy Error*

**OUTPUT CAPACITANCE:** Capacitance from OUT terminal (pin 1) to ground.

**FEEDTHROUGH ERROR:** Error caused by capacitive coupling from  $V_{IN}$  (pin 17) to OUT (pin 1) with all digital inputs LOW.

## PRINCIPLES OF OPERATION

### CIRCUIT DESCRIPTION

The AD7525, a  $3\frac{1}{2}$  digit BCD multiplying DAC, consists of a thin-film R/2R ladder, interquad voltage dividers and 13 N-channel MOS SPDT current steering switches. Most applications require the addition of only an external operational amplifier.

Referring to Figure 1, the "1.0 Digit" is a 1-bit multiplying DAC (composed of  $SW_1$  and  $R_1$ ) while the 0.1, 0.01, and 0.001 digits are 4-bit multiplying DAC's (DAC1, DAC2, and DAC3) connected by 10:1 dividers (composed of  $R_{IN2}, R_2, R_3$  and  $R_{IN3}, R_4, R_5$ ).

DAC1 is expanded to show the R/2R ladder and switch network. With input voltage  $V_{IN}$ , the currents in each shunt arm are (starting at the left)  $V_{IN}/2R, V_{IN}/4R, V_{IN}/8R$  and  $V_{IN}/16R$ . A logic ONE applied to a digital input steers that shunt arm's current to OUT, while a logic ZERO steers the current to GND.

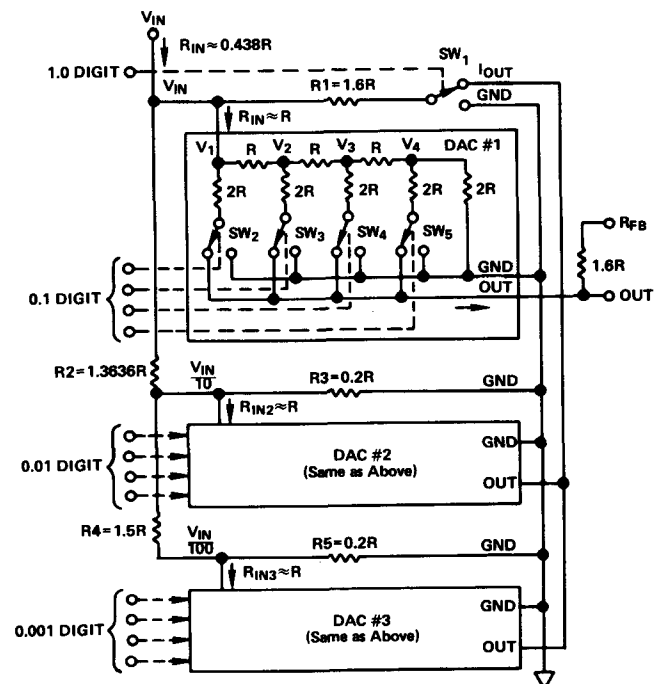


Figure 1. AD7525 Circuit Diagram



## EQUIVALENT CIRCUIT

As shown in Figure 2, the AD7525 is a digitally controlled  $\pi$ -network attenuator with signal input "VIN" (pin 17), signal output "OUT" (pin 1), signal common "GND" (pin 2) and digital control "BCD input" (pins 3-15).

With OUT (pin 1) terminated at op amp virtual ground and  $R_{FB}$  (pin 18) connected to the op amp output, the nominal transfer equation is:

$$V_{OUT} = -V_{IN} BCD$$

where  $0.000 \leq BCD \leq 1.999$

Table 1 shows the various circuit elements of Figure 2 as a function of the BCD input (where applicable). BCD code dependent elements are shown connected by dotted lines in Figure 2.

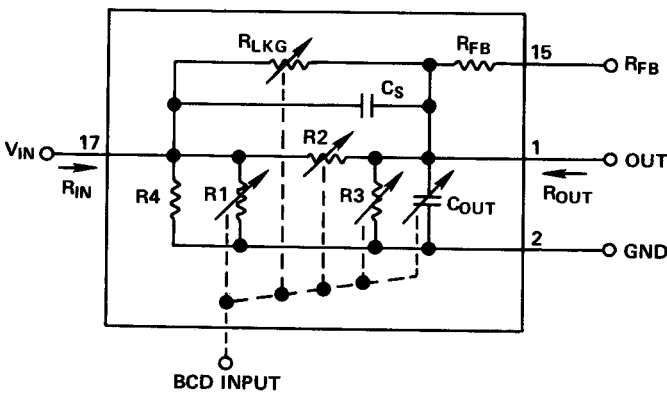


Figure 2. Functional Equivalent Circuit

It is important to realize that offset is caused by including the usual bias current compensation resistor in the amplifier noninverting terminal. This should not be included; rather, the amplifier should have a bias current which is low over the temperature range of interest. Bias current causes "output offset" of magnitude  $(I_B)R_{FB}$ .

## High Frequency Amplifiers

$R_{FB}$  and  $C_{OUT}$  create a phase lag in the output amplifier's feedback circuit. This phase lag, in conjunction with the amplifier's phase lag, may cause ringing or oscillation. When using a high speed amplifier, shunting the amplifier input to output with 5-20pF of feedback capacitance ensures stability.

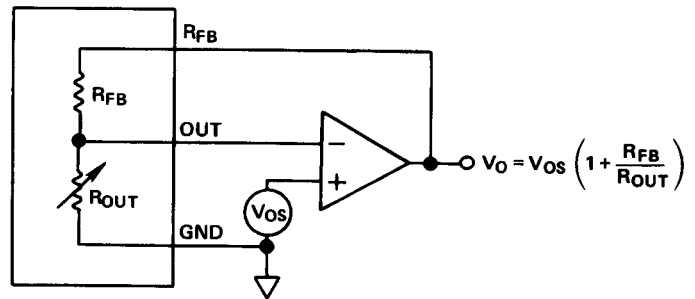


Figure 3. Noise Gain Equivalent Circuit

## OUTPUT AMPLIFIER CONSIDERATIONS

### Amplifier Offset

From Table 1, the output resistance at OUT (pin 1) is code dependent, varying between  $\infty$  to  $0.35 R_{LDR}$ . For a fixed feedback resistor of value  $1.6 R_{LDR}$  (Figure 3), the output error for a fixed amplifier offset ( $V_{OS}$ ) is:

$$V_{ERROR} = \left(1 + \frac{R_{FB}}{R_{OUT}}\right) V_{OS}$$

Case 1: ( $R_{OUT} = \infty$ )

$$V_{ERROR} = \left(1 + \frac{R_{FB}}{\infty}\right) V_{OS}$$

$$V_{ERROR} = V_{OS}$$

Case 2: ( $R_{OUT} = 0.35 R_{LDR}$ )

$$V_{ERROR} = \left(1 + \frac{1.6 R_{LDR}}{0.35 R_{LDR}}\right) V_{OS}$$

$$V_{ERROR} = (1 + 4.6)V_{OS} = 5.6 V_{OS}$$

Cases 1 and 2 show that amplifier offset in conjunction with a changing output resistance at OUT (pin 1) create nonlinearity error, in addition to a simple offset term.

It is therefore recommended that amplifier initial offset be adjusted to less than  $100\mu V$  (as measured between the amplifier input terminals). The offset voltage over the temperature range of interest should not exceed  $250\mu V$ .

| CIRCUIT ELEMENT   | VALUE  |
|-------------------|--|
| $R_{IN}$ (pin 17) | $R_{IN} = R_1 \parallel R_2 \parallel R_4 = 0.438 R_{LDR}$ (note 1)  |
| $R_4$             | $R_4 = 0.838 R_{LDR}$ (note 1)   |
| $R_1$             | $R_1 = R_{FB} \left(\frac{1}{BCD} - 0.5002\right)$<br>$0.000 \leq BCD \leq 1.999$                                  |
| $R_2$             | $R_2 = \frac{R_{FB}}{BCD}$<br>for $0.000 \leq BCD \leq 1.999$  |
| $R_{OUT}$ (pin 1) | Varies nonlinearly with input codes.<br>Range $\infty$ to $0.35 R_{LDR}$ (note 1)<br>$R_{OUT} = R_2 \parallel R_3$ |
| $R_{IN}$          | $R_{IN} = 0.438 R_{LDR}$ (note 1)  |
| $R_{LKG}$         | $R_{LKG} \approx 50M\Omega$ (note 2)   |
| $C_{OUT1}$        | $C_{OUT} \approx [(50pF)(BCD) + 30pF]$<br>$0.000 \leq BCD \leq 1.999$  |
| $C_S$             | $C_S \approx 0.2pF$ (package capacitance)  |

### NOTES:

- $R_{LDR}$  is R/2R ladder characteristic resistance, min  $5k\Omega$ , max  $20k\Omega$ , typically  $10k\Omega$ .
- $50M\Omega$  corresponds to an OUT (pin 1) leakage of  $200nA$  (as shown in specification table) and a  $V_{IN}$  of  $10V$ .

Table 1. Equivalent Circuit Element Values

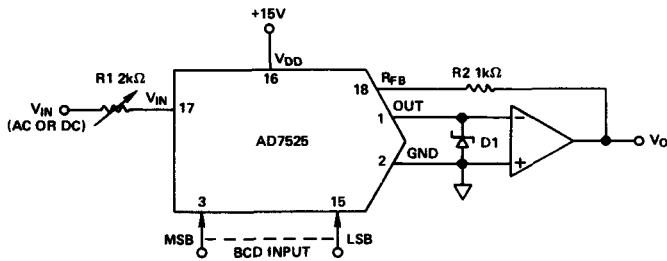


Figure 4. Digitally Controlled Attenuator Circuit

| BCD INPUT |      |      |       | Equivalent<br>Decimal<br>Input | ANALOG OUTPUT |                |
|-----------|------|------|-------|--------------------------------|---------------|----------------|
| 1.0       | 0.1  | 0.01 | 0.001 |                                | $V_O/V_{IN}$  | $V_O$          |
| 1         | 1001 | 1001 | 1001  | 1.999                          | -1.999        | $-1.999V_{IN}$ |
| 1         | 0000 | 0000 | 0001  | 1.001                          | -1.001        | $-1.001V_{IN}$ |
| 1         | 0000 | 0000 | 0000  | 1.000                          | -1.000        | $-1.000V_{IN}$ |
| 0         | 1001 | 1001 | 1001  | 0.999                          | -0.999        | $-0.999V_{IN}$ |
| 0         | 0101 | 0000 | 0000  | 0.500                          | -0.500        | $-0.500V_{IN}$ |
| 0         | 0000 | 0000 | 0000  | 0.000                          | 0             | 0              |

Note 1:

For proper BCD coding, the 0.1 digit, 0.01 digit or 0.001 digit must not exceed BCD "9" (1001).

Table 2. Analog Input/Output Relationship vs. Digital Input

## CALIBRATION PROCEDURE

### Offset Adjustment:

1. Apply BCD code 0.000 (0 0000 0000 0000) to the AD7525 digital inputs.
2. Connect a high resolution, high impedance voltmeter between pins 1 and 2 of the AD7525.
3. Adjust amplifier's trimpot for minimum reading on the voltmeter ( $<100\mu V$ ).

### Gain Adjustment:

1. Apply BCD code 1.000 (1 0000 0000 0000) to the AD7525 digital input.
2. Apply +10V to the  $V_{IN}$  input of Figure 1.
3. Connect the voltmeter between  $V_O$  (amplifier output) and pin 2 of the AD7525.
4. Adjust  $R_1$  until  $V_O = -10V$ .

## APPLICATION – THUMBWHEEL SWITCH ATTENUATOR

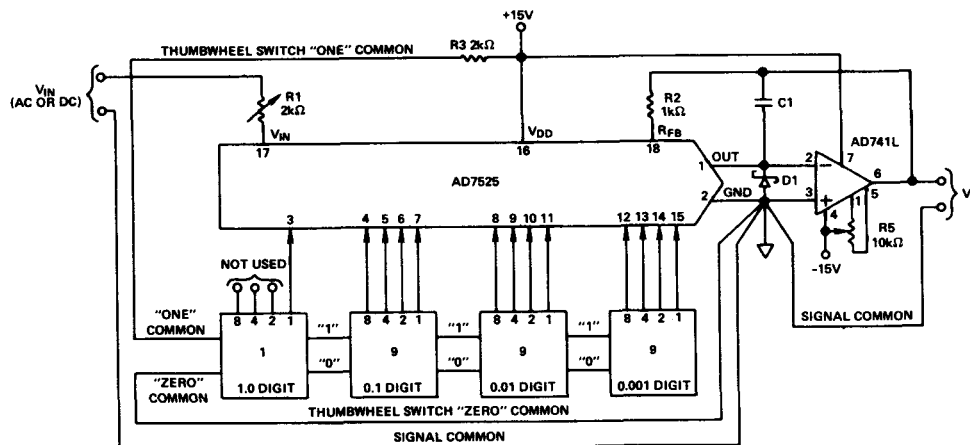


Figure 5. Thumbwheel Switch Attenuator

The circuit shown in Figure 5 is a precision voltage divider similar to 10-turn pots and thumbwheel switch incremental-voltage-divider assemblies. Advantages of the circuit are:

- Economy
- Low Output Impedance
- Resolution 0.1%  $V_{IN}$
- Excellent Repeatability Accuracy
- 1000 - Count Overrange

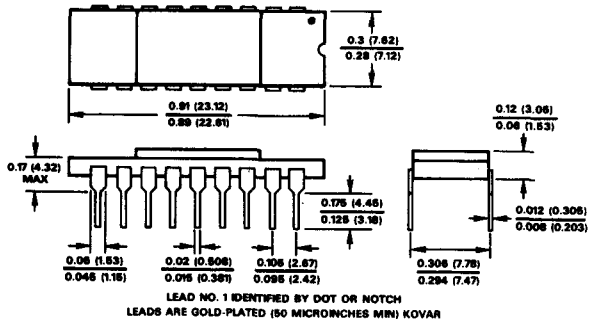
The BCD coded thumbwheel assembly applies BCD data to the AD7525 digital inputs. The switch assembly shown has single-pole-double-throw action, thus the BCD inputs are

pulled either to +15V or GND (available from AMP, Harrisburg, PA; CHERRY, Waukegan, Illinois; or SAE, Santa Clara, California). Resistor  $R_3$  limits current if make-before-break switches are used. SPST switch assemblies can be used, however appropriate pull-up or pull-down resistors must be used on each digital input, depending upon whether the switch coding is BCD or complementary BCD. This ensures each digital input has appropriate  $V_{IH}$  or  $V_{IL}$  levels applied.

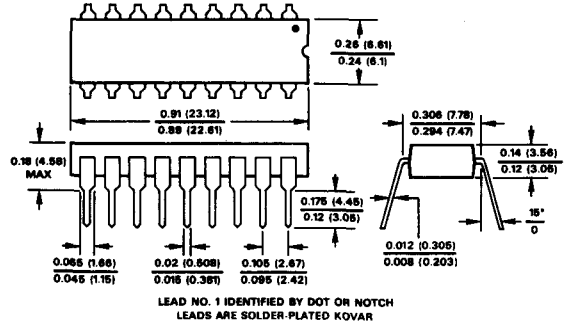
Resistors  $R_1$  and  $R_2$  provide gain adjustment capability.  $R_5$  is used to adjust the amplifier offset voltage (as measured between the amplifier input terminals) to less than  $100\mu V$ . Diode  $D_1$  (HP5082-2811) provides AD7525 output protection (see Caution note 3, page 139S).

**MECHANICAL INFORMATION**  
Dimensions shown in inches and (mm).

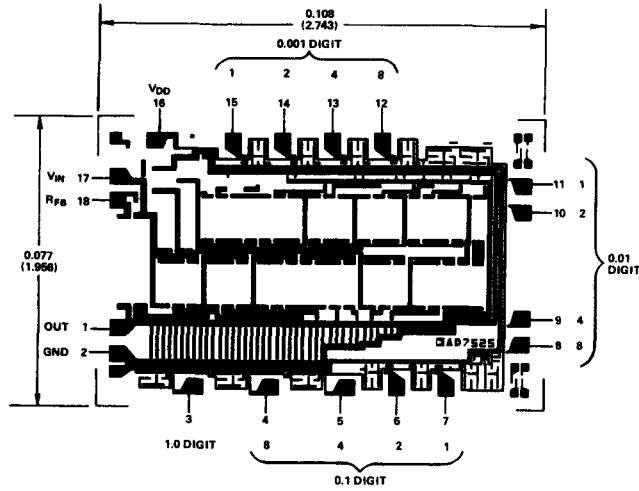
**18 PIN CERAMIC DIP**



**18 PIN PLASTIC DIP**



**BONDING DIAGRAM**



- NOTES:  
1. PAD NUMBERS CORRESPOND TO PIN NUMBERS SHOWN IN PIN CONFIGURATION.  
2. PAD 2 (GND) SHOULD BE BONDED FIRST TO MINIMIZE ESD HAZARDS.  
3. PADS ARE 0.004in X 0.004in (0.102mm X 0.102mm).



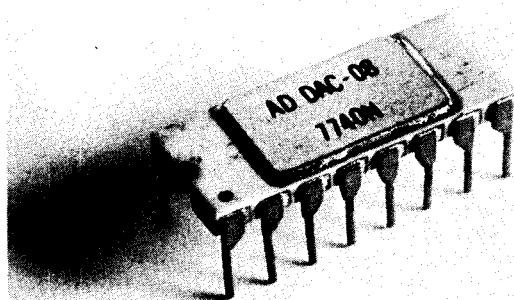
# 8-Bit Monolithic High Speed Multiplying D/A Converter

## AD DAC-08

### PRELIMINARY TECHNICAL DATA

#### FEATURES

- Exact Replacement for Industry Standard DAC-08
- Fast (85ns typical) Settling Time
- Linearity Error  $\pm 1/4$ LSB ( $\pm 0.1\%$ ) Guaranteed Over Full Temperature Range
- Wide Output Voltage Compliance:  $-10V$  to  $+18V$
- Single Chip Monolithic Construction
- 16-Pin Ceramic DIP Packaging
- Low Cost
- MIL-STD-883 Processing Available



#### PRODUCT DESCRIPTION

The AD DAC-08 is a low-cost, 8-bit monolithic multiplying digital-to-analog converter featuring typical settling times of 85ns. The chip contains 8 matched bipolar current steering switches, a precision resistor network, and high-speed control amplifier, thus integrating all important circuit functions on a single chip.

The AD DAC-08 provides matching of full-scale output current to within 1LSB of the reference current. Analog Devices' precision linear processing makes this matching possible without the use of laser trimming. Diffused resistors are used rather than thin-film resistors in an effort to provide specified performance at low cost.

The AD DAC-08 is recommended for use in applications requiring 8-bit accuracy and fast settling times coupled with ease of use. The AD DAC-08 also provides an alternate source for designs already using the standard DAC-08.

The AD DAC-08 is available in 5 performance grades: the AD DAC-08A and AD DAC-08 are rated for the full  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  military temperature range; and the AD DAC-08H, E, and C grades are specified for the  $0$  to  $+70^{\circ}\text{C}$  commercial temperature range. All models are guaranteed monotonic over their full temperature range, and all are packaged in a hermetically-sealed 16-pin ceramic dual-in-line package.

#### PRODUCT HIGHLIGHTS

1. The AD DAC-08 is a true second-source equivalent to the industry standard DAC-08.
2. The versatile current-in, current-out design, choice of fixed or variable reference, and CMOS or TTL compatible inputs offer the user greater flexibility in applying the device.
3. The fast settling time allows the AD DAC-08 to be used in applications such as CRT displays, waveform generators, and high-speed analog-to-digital converters.
4. The high impedance current output can drive a resistor directly, or be used with an external op amp to produce a low impedance output voltage.
5. The AD DAC-08 is available in chip form for use in hybrid microcircuits. Consult Analog Devices' chip catalog for available grades and application details.
6. The AD DAC-08 and AD DAC-08A are available fully screened to MIL-STD-883, Method 5004 Class B. A full list of tests is available upon request.

# SPECIFICATIONS

The AD DAC-08 and AD DAC-08A specifications apply for  $V_S = \pm 15V$ ,  $I_{REF} = 2.0mA$ ,  $T_A = -55^\circ C$  to  $+125^\circ C$  unless otherwise noted.

| MODEL CHARACTERISTIC      | SYMBOL             | CONDITIONS   | AD DAC-08  |             |            | AD DAC-08A |             |            | UNITS           |
|---------------------------|--------------------|--|------------|-------------|------------|------------|-------------|------------|-----------------|
|                           |                    |  | MIN        | TYP         | MAX        | MIN        | TYP         | MAX        |                 |
| RESOLUTION                |                    |  |            |             | 8          |            |             | 8          | Bits            |
| MONOTONICITY              |                    | $T_A = -55^\circ C$ to $+125^\circ C$                                      | GUARANTEED |             |            | GUARANTEED |             |            |                 |
| NONLINEARITY              |                    | $T_A = -55^\circ C$ to $+125^\circ C$                                      |            |             | $\pm 0.19$ |            |             | $\pm 0.1$  | % FS            |
| SETTLING TIME             | $t_s$              | Full Scale Step to $\pm 1/2LSB$  | 85         |             | 135        | 85         |             | 135        | ns              |
| PROPAGATION DELAY         | $t_{PLH}, t_{PHL}$ | All Bits Switched  | 35         |             | 60         | 35         |             | 60         | ns              |
| FULL SCALE TEMPCO         | $TC I_{FS}$        |  | $\pm 10$   |             | $\pm 50$   | $\pm 10$   |             | $\pm 50$   | ppm/ $^\circ C$ |
| OUTPUT VOLTAGE COMPLIANCE | $V_{OC}$           | $\Delta I_{FS} < 1/2LSB$ ;<br>$R_{OUT} > 20M\Omega$ typ                    | -10        |             | -18        | -10        |             | +18        | V dc            |
| FULL SCALE CURRENT        | $I_{FS4}$          | $V_{REF} = 10.000V$ ; $R_{14}, R_{15} = 5.000k\Omega$ ; $T_A = 25^\circ C$ | 1.94       | 1.99        | 2.04       | 1.984      | 1.992       | 2.000      | mA              |
| FULL SCALE SYMMETRY       | $I_{FSS}$          | $(I_{FS4} - I_{FS2})$  |            | $\pm 1.0$   | $\pm 8.0$  |            | $\pm 0.5$   | $\pm 4.0$  | $\mu A$         |
| ZERO SCALE CURRENT        | $I_{ZS}$           |  |            | 0.2         | 2.0        |            | 0.1         | 1.0        | $\mu A$         |
| OUTPUT CURRENT RANGE      | $I_{FSR}$          | $V_- = -5.0V$<br>$V_- = -7.0$ to $-18V$                                    | 0          | 2.0         | 2.1        | 0          | 2.0         | 2.1        | mA              |
| LOGIC INPUT LEVELS        |                    |  |            |             |            |            |             |            |                 |
| Logic "0"                 | $V_{IL}$           | $V_{LC} = 0V$  |            |             | 0.8        |            |             | 0.8        | V               |
| Logic "1"                 | $V_{IH}$           | $V_{LC} = 0V$  | 2.0        |             |            | 2.0        |             |            | V               |
| LOGIC INPUT CURRENTS      |                    |  |            |             |            |            |             |            |                 |
| Logic "0"                 | $I_{IL}$           | $V_{LC} = 0V$<br>$-10V < V_{IN} < +0.8V$                                   |            | -2.0        | -10        |            | -2.0        | -10        | $\mu A$         |
| Logic "1"                 | $I_{IH}$           | $2.0V < V_{IN} < 18V$  |            | 0.002       | 10         |            | 0.002       | 10         | $\mu A$         |
| LOGIC INPUT SWING         | $V_{IS}$           | $V_- = -15V$   | -10        |             | +18        | -10        |             | +18        | V               |
| LOGIC THRESHOLD RANGE     | $V_{IHR}$          | $V_S = \pm 15V$  | -10        |             | +13.5      | -10        |             | +13.5      | V               |
| REFERENCE BIAS CURRENT    | $I_{REF}$          |  | +0.1       | -1.0        | -3.0       | +0.1       | -1.0        | -3.0       | $\mu A$         |
| REFERENCE INPUT SLEW RATE | $di/dt$            |  | 4.0        |             | 8.0        | 4.0        |             | 8.0        | mA/ $\mu s$     |
| POWER SUPPLY SENSITIVITY  |                    |  |            |             |            |            |             |            |                 |
| $PSSI_{FS+}$              |                    | $V_+ = 4.5V$ to $18V$  |            | +0.0003     | $\pm 0.01$ |            | +0.0003     | $\pm 0.01$ | %/%             |
| $PSSI_{FS-}$              |                    | $V_- = 4.5V$ to $-18V$<br>$I_{REF} = 1.0mA$                                |            | $\pm 0.002$ | $\pm 0.01$ |            | $\pm 0.002$ | $\pm 0.01$ | %/%             |
| POWER SUPPLY CURRENT      |                    |  |            |             |            |            |             |            |                 |
| From $+V_S$               | $I_+$              |  | 0.4        | 2.3         | 3.8        | 0.4        | 2.3         | 3.8        | mA              |
| From $-V_S$               | $I_-$              |  | -0.8       | -6.4        | -7.8       | -0.8       | -6.4        | -7.8       | mA              |
| POWER DISSIPATION         |                    |  |            |             |            |            |             |            |                 |
|                           | $P_D$              | $\pm 5V, I_{REF} = 1.0mA$  |            | 33          | 48         |            | 33          | 48         | mW              |
|                           |                    | $+5V, -15V, I_{REF} = 2.0mA$   |            | 108         | 136        |            | 108         | 136        | mW              |
|                           |                    | $\pm 15V, I_{REF} = 2.0mA$   |            | 135         | 174        |            | 135         | 174        | mW              |

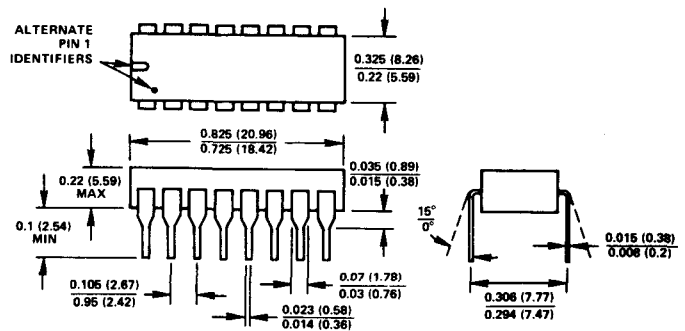
## ABSOLUTE MAXIMUM RATINGS

|                                       |                               |                                 |
|---------------------------------------|-------------------------------|---------------------------------|
| Operating Temperature                 | AD DAC-08, DAC-08A            | $-55^\circ C$ to $+125^\circ C$ |
|                                       | AD DAC-08E, C, H              | $0$ to $+70^\circ C$            |
| Storage Temperature                   |                               | $-65^\circ C$ to $+150^\circ C$ |
| Power Dissipation                     |                               | 500mW                           |
|                                       | Above $100^\circ C$ Derate by | 10mW/ $^\circ C$                |
| Lead Soldering Temperature            |                               | $300^\circ C$ (60sec)           |
| $-V_S$ Supply to $+V_S$ Supply        |                               | 36V                             |
| Logic Inputs                          |                               | $-V_S$ to $(-V_S + 36V)$        |
| $V_{LC}$                              |                               | $-V_S$ to $+V_S$                |
| Reference Inputs ( $V_{14}, V_{15}$ ) |                               | $-V_S$ to $+V_S$                |
| Reference Input Differential          |                               |                                 |
| Voltage ( $V_{14}$ to $V_{15}$ )      |                               | $\pm 18V$                       |
| Reference Input Current ( $I_{14}$ )  |                               | 5.0mA                           |

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

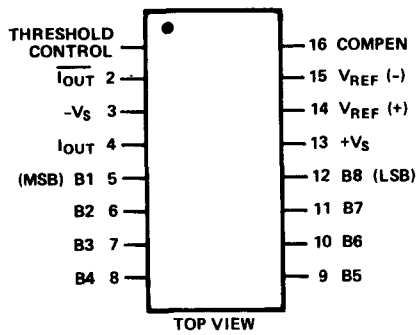
### 16-PIN DUAL-IN-LINE



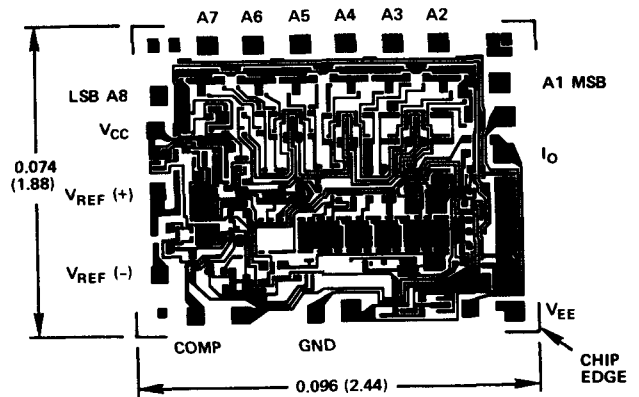
# SPECIFICATIONS

The AD DAC-08C, E, and H specifications apply for  $V_S = \pm 15V$ ,  $I_{REF} = 2.0mA$ ,  $T_A = 0$  to  $+70^\circ C$  unless otherwise noted.

| MODEL CHARACTERISTIC      | SYMBOL                         | CONDITIONS  | AD DAC-08C  |                             |                          | AD DAC-08E  |                             |                          | AD DAC-08H  |                             |                          | UNITS           |
|---------------------------|--------------------------------|---|-------------|-----------------------------|--------------------------|-------------|-----------------------------|--------------------------|-------------|-----------------------------|--------------------------|-----------------|
|                           |                                |   | MIN         | TYP                         | MAX                      | MIN         | TYP                         | MAX                      | MIN         | TYP                         | MAX                      |                 |
| RESOLUTION                |                                |   |             |                             | 8                        |             |                             | 8                        |             |                             | 8                        | Bits            |
| MONOTONICITY              |                                | $T_A = 0$ to $+70^\circ C$  | GUARANTEED  |                             |                          | GUARANTEED  |                             |                          | GUARANTEED  |                             |                          |                 |
| NONLINEARITY              |                                | $T_A = 0$ to $+70^\circ C$  |             |                             | $\pm 0.39$               |             |                             | $\pm 0.19$               |             |                             | $\pm 0.1$                | % FS            |
| SETTLING TIME             | $t_s$                          | Full Scale Step to $\pm 1/2LSB$   | 85          | 150                         |                          | 85          | 150                         |                          | 85          | 135                         |                          | ns              |
| PROPAGATION DELAY         | $t_{PLH}, t_{PHL}$             | All Bits Switched   | 35          | 60                          |                          | 35          | 60                          |                          | 35          | 60                          |                          | ns              |
| FULL SCALE TEMPCO         | $TC I_{FS}$                    |   | $\pm 10$    | $\pm 80$                    |                          | $\pm 10$    | $\pm 50$                    |                          | $\pm 10$    | $\pm 50$                    |                          | ppm/ $^\circ C$ |
| OUTPUT VOLTAGE COMPLIANCE | $V_{OC}$                       | $\Delta I_{FS} < 1/2LSB$ ;<br>$R_{OUT} > 20M\Omega$                                     | -10         |                             | +18                      | -10         |                             | +18                      | -10         |                             | +18                      | V dc            |
| FULL SCALE CURRENT        | $I_{FS4}$                      | $V_{REF} = 10.000V$ ; $R_{14}, R_{15} = 5.000k\Omega$ ; $T_A = 25^\circ C$              | 1.94        | 1.99                        | 2.04                     | 1.94        | 1.99                        | 2.04                     | 1.984       | 1.992                       | 2.000                    | mA              |
| FULL SCALE SYMMETRY       | $I_{FSS}$                      | $(I_{FS4} - I_{FS2})$   |             | $\pm 2.0$                   | $\pm 16$                 |             | $\pm 1.0$                   | $\pm 8.0$                |             | $\pm 0.5$                   | $\pm 4.0$                | $\mu A$         |
| ZERO SCALE CURRENT        | $I_{ZS}$                       |   |             | 0.2                         | 4.0                      |             | 0.2                         | 2.0                      |             | 0.1                         | 1.0                      | $\mu A$         |
| OUTPUT CURRENT RANGE      | $I_{FSR}$                      | $V = -5.0V$<br>$V = -7.0$ to $-18V$   | 0           | 2.0                         | 2.1                      | 0           | 2.0                         | 2.1                      | 0           | 2.0                         | 2.1                      | mA              |
|                           |                                |   | 0           | 2.0                         | 4.2                      | 0           | 2.0                         | 4.2                      | 0           | 2.0                         | 4.2                      | mA              |
| LOGIC INPUT LEVELS        |                                |   |             |                             |                          |             |                             |                          |             |                             |                          |                 |
| Logic "0"                 | $V_{IL}$                       | $V_{LC} = 0V$   |             |                             | 0.8                      |             |                             | 0.8                      |             |                             | 0.8                      | V               |
| Logic "1"                 | $V_{IH}$                       | $V_{LC} = 0V$   | 2.0         |                             |                          | 2.0         |                             |                          | 2.0         |                             |                          | V               |
| LOGIC INPUT CURRENTS      |                                |   |             |                             |                          |             |                             |                          |             |                             |                          |                 |
| Logic "0"                 | $I_{IL}$                       | $V_{LC} = 0V$<br>$-10V < V_{IN} < +0.8V$  |             | -2.0                        | -10                      |             | -2.0                        | -10                      |             | -2.0                        | -10                      | $\mu A$         |
| Logic "1"                 | $I_{IH}$                       | $2.0V < V_{IN} < 18V$   |             | 0.002                       | 10                       |             | 0.002                       | 10                       |             | 0.002                       | 10                       | $\mu A$         |
| LOGIC INPUT SWING         | $V_{IS}$                       | $V = -15V$  | -10         |                             | +18                      | -10         |                             | +18                      | -10         |                             | +18                      | V               |
| LOGIC THRESHOLD RANGE     | $V_{IHL}$                      | $V_S = \pm 15V$   | -10         |                             | +13.5                    | -10         |                             | +13.5                    | -10         |                             | +13.5                    | V               |
| REFERENCE BIAS CURRENT    | $I_{REF}$                      |   | +0.1        | -1.0                        | -3.0                     | +0.1        | -1.0                        | -3.0                     | +0.1        | -1.0                        | -3.0                     | $\mu A$         |
| REFERENCE INPUT SLEW RATE | $di/dt$                        |   | 4.0         | 8.0                         |                          | 4.0         | 8.0                         |                          | 4.0         | 8.0                         |                          | mA/ $\mu s$     |
| POWER SUPPLY SENSITIVITY  | $PSSI_{FS+}$ ,<br>$PSSI_{FS-}$ | $V = +4.5V$ to $18V$<br>$V = -4.5V$ to $-18V$<br>$I_{REF} = 1.0mA$                      |             | $\pm 0.0003$<br>$\pm 0.002$ | $\pm 0.01$<br>$\pm 0.01$ |             | $\pm 0.0003$<br>$\pm 0.002$ | $\pm 0.01$<br>$\pm 0.01$ |             | $\pm 0.0003$<br>$\pm 0.002$ | $\pm 0.01$<br>$\pm 0.01$ | %/%             |
| POWER SUPPLY CURRENT      | $I+$ ,<br>$I-$                 | From $+V_S$<br>From $-V_S$  | 0.4<br>-0.8 | 2.3<br>-6.4                 | 3.8<br>-7.8              | 0.4<br>-0.8 | 2.3<br>-6.4                 | 3.8<br>-7.8              | 0.4<br>-0.8 | 2.3<br>-6.4                 | 3.8<br>-7.8              | mA<br>mA        |
| POWER DISSIPATION         | $P_D$                          | $\pm 5V, I_{REF} = 1.0mA$<br>$+5V, -15V, I_{REF} = 2.0mA$<br>$\pm 15V, I_{REF} = 2.0mA$ |             | 33<br>108<br>135            | 48<br>136<br>174         |             | 33<br>108<br>135            | 48<br>136<br>174         |             | 33<br>108<br>135            | 48<br>136<br>174         | mW<br>mW<br>mW  |



Pin Connections



THE AD DAC-08 IS ALSO AVAILABLE IN CHIP FORM. CONSULT ANALOG DEVICES' CHIP CATALOG FOR SPECIFICATIONS AND APPLICATIONS INFORMATION.

Chip Dimensions and Pad Layout. Dimensions shown in inches and (mm).

## APPLYING THE AD DAC-08

### Reference Connections

Figure 1 shows the block diagram of the AD DAC-08 circuit. A reference current (equal to the desired full-scale output current) is applied to pin 14. The reference amplifier adjusts the base voltage of the NPN current source transistors. The collector currents are binarily weighted, and their sum is equal to 255/256 times the reference current. The binary weighting is accomplished by the diffused resistor R-2R ladder network. The individual collector currents are steered into either the  $I_{OUT}$  or  $\bar{I}_{OUT}$  lines by the current switches. These switches are driven by level shifters which can accept TTL or CMOS logic levels directly. The  $I_{OUT}$  and  $\bar{I}_{OUT}$  lines can drive an op amp summing junction or can drive resistive loads directly due to the wide range of output compliance voltage.

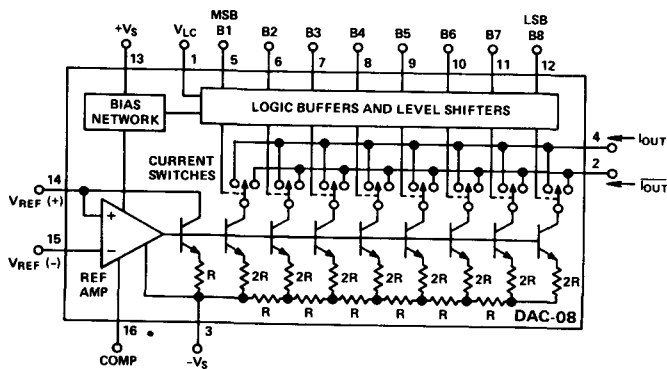


Figure 1. AD DAC-08 Block Diagram

Figure 2 illustrates the connections for positive and negative references. When a positive reference is used (Figure 2a), resistor R14 (equal to  $V_{REF}$  divided by the desired  $I_{FS}$ ) establishes the reference current into pin 14. Reference amplifier bias current errors are minimized by connecting R15 (equal to R14) from pin 15 to ground. Adjustment of the output scale can be done by trimming R14, although in most applications the tight initial matching between reference current and output current will be adequate.

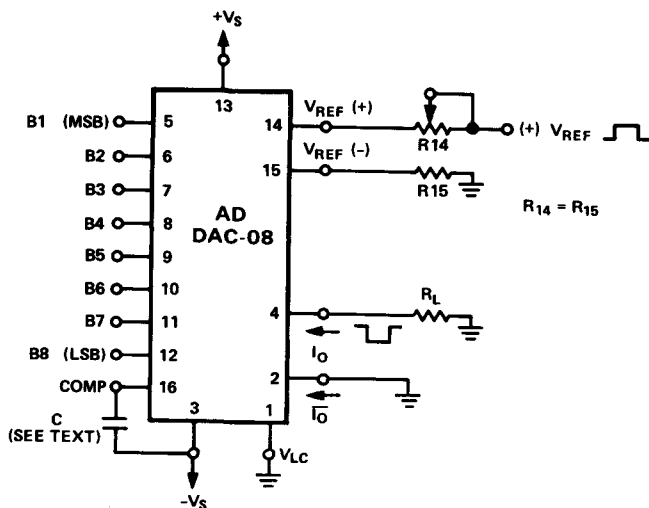


Figure 2a. Connections for Use with Positive Reference

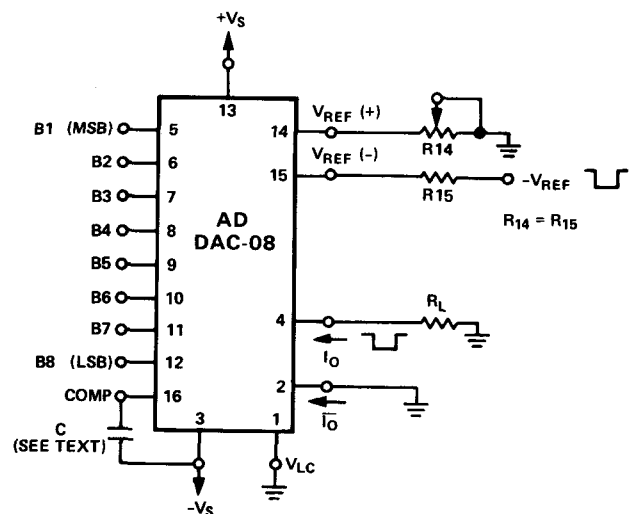


Figure 2b. Connections for Use with Negative Reference

Figure 2b shows the connections for a negative reference. Note that the reference current flows from ground into pin 14 through R14, which should be a low TC resistor as in the positive reference configuration. Resistor R15 serves the purpose of bias current cancellation only and need not be a precision resistor. Note that the input impedance for a negative reference is very high, while a positive reference sees an impedance equal to R14.

When a dc reference is used, a reference bypass capacitor is recommended. The reference should be a low-drift, well-regulated and filtered type, such as the AD581 10V reference IC. Other values of reference voltage may be used, provided that R14 is chosen for a reference current between 0.2mA and 4.0mA.

The reference amplifier requires an external compensation capacitor from pin 16 to  $-V_S$ . When a fixed dc reference is used, a 0.01 $\mu$ F capacitor is recommended.

### MULTIPLYING MODE PERFORMANCE

The AD DAC-08 can be used to perform two-quadrant digital-analog multiplication by applying an ac reference signal. When an ac reference is used, pin 15 must be offset to insure that pin 14 is always at a higher potential than pin 15.

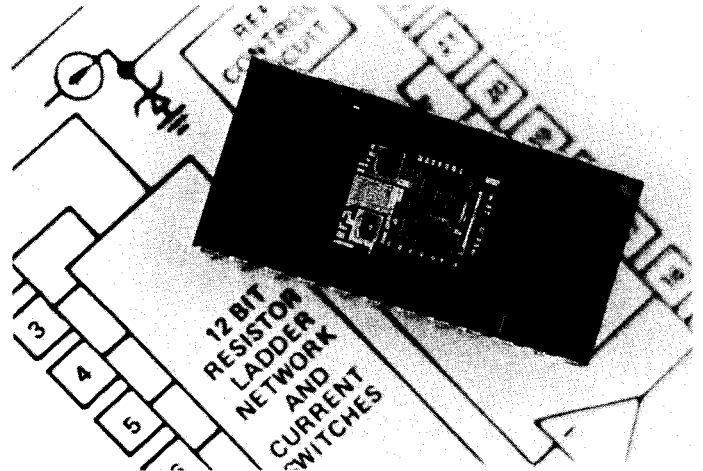
The reference amplifier must be properly compensated in ac applications to insure stability. The value of the capacitor from pin 16 to  $-V_S$  depends on the value of R14. Minimum values of compensation capacitor for R14 values of 1, 2 and 5k $\Omega$  are 15, 37 and 75pF respectively.

### LOGIC INPUT CIRCUIT

The AD DAC-08 digital inputs will accommodate all popular logic families. The switching threshold is adjustable by applying a voltage to the logic threshold control pin (pin 1). The threshold is nominally 1.4 volts above  $V_{LC}$  at room temperature. For TTL/DTL interface, pin 1 is simply grounded. The logic inputs will tolerate wide voltage swings; for example, for  $-V_S = -15V$ , the inputs may swing between  $-10V$  and  $+18V$ .

**FEATURES**

**Low Cost**  
**Improved Replacement for Standard DAC80**  
**3 Chip, High Reliability Construction**  
**Low Power Dissipation**  
**Laser-Trimmed to High Accuracy:**  
 **$\pm\frac{1}{2}$ LSB Max Nonlinearity, 0 to +70°C**  
**Guaranteed Monotonicity, 0 to +70°C**  
**High Stability, High Current Output**  
**Buried Zener Reference**  
**On-Board Output Amplifier (V Models)**  
**24 Lead Side Brazed Ceramic DIP**

**PRODUCT DESCRIPTION**

The AD DAC80 is a low cost 12-bit digital-to-analog converter, consisting of matched bipolar switches, a precision resistor network, a low-drift high-stability voltage reference and an optional output amplifier. Options include TTL compatible complementary 12-bit binary (CBI) or 3 digit BCD (CCD) input codes, as well as current or voltage output modes. The AD DAC80 offers output voltage ranges of  $\pm 2.5$ ,  $\pm 5$ ,  $\pm 10$ , 0 to +5, or 0 to +10 volts (V models); output current ranges (I models) are either  $\pm 1$ mA or 0 to -2mA.

Advanced circuit design and precision processing techniques result in significant performance advantages over conventional, larger, standard DAC80 devices. An innovative 3-chip construction improves reliability by a factor of two. The AD DAC80 incorporates a fully differential, non-saturating precision current switching cell structure<sup>1</sup> which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability, SiCr thin film resistors are trimmed with a fine resolution laser, resulting in lower differential nonlinearity errors. A low noise, high stability subsurface zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature cycle characteristics which challenge the best discrete zener references.

The AD DAC80 is recommended for all low cost 12-bit D/A converter applications where reliability and cost are of paramount importance. The AD DAC80 is also ideal for use in constructing A/D conversion systems and as a building block for higher resolution D/A systems.

<sup>1</sup> COVERED BY PATENT NUMBERS: 3,978,473; Re 28,633; 4,020,486; 3,747,088; 3,803,590; 3,961,326.

**PRODUCT HIGHLIGHTS**

1. The AD DAC80 directly replaces other devices of this type with significant increases in performance.
2. 3-Chip IC construction makes the AD DAC80 the optimum choice for applications where low cost and high reliability are major considerations.
3. System performance upgrading is possible without redesign.
4. The AD DAC80 offers a maximum nonlinearity error of  $\pm 0.012\%$ ,  $\pm 30$ ppm/ $^{\circ}$ C maximum gain drift, and a total accuracy drift in the bipolar configuration of  $\pm 20$ ppm/ $^{\circ}$ C maximum.
5. The low T.C. Binary ladder guarantees that all AD DAC80 units will be monotonic over the specified temperature range.
6. Reduced power consumption requirements result in improved stability and shorter warm-up time.
7. The precision buried zener reference can supply up to 2.5mA for use elsewhere in the application.
8. Voltage or current output modes are available in either of the BCD or binary input formats.



# SPECIFICATIONS (T<sub>A</sub> = +25°C, rated power supplies unless otherwise noted)

| MODEL  | DAC80-CBI                                   | DAC80-CCD                |
|--|---|--------------------------|
| <b>DIGITAL INPUT</b>   |   |                          |
| Resolution   | 12 Bits max                                 | 3 Digits max             |
| Logic Levels (TTL/Compatible)  |   |                          |
| Logical "1" (at +1μA)  | +2V dc min, +5.5V dc max                    | *                        |
| Logical "0" (at -100μA)  | 0V dc min, +0.8V dc max                     | *                        |
| <b>ACCURACY</b>  |   |                          |
| Linearity Error 0 to +70°C   | ±1/4LSB typ, ±1/2LSB <sup>1</sup> max       | ±1/8LSB typ, ±1/4LSB max |
| Differential Linearity Error 0 to +70°C  | ±1/2LSB typ, ±3/4LSB max                    | ±1/4LSB typ, ±1/2LSB max |
| Gain Error <sup>2</sup>  | ±0.1% typ, ±0.3% max                        | *                        |
| Offset Error <sup>2</sup>  | ±0.05% FSR typ, ±0.15% FSR <sup>3</sup> max | *                        |
| Monotonicity Temp. Range   | 0 to +70°C                                  | *                        |
| <b>DRIFT<sup>4</sup> (0 to +70°C)</b>  |   |                          |
| Total Bipolar Drift (Includes Gain, Offset, and Linearity Drifts) <sup>5</sup> | ±20ppm FSR/°C max                           | *                        |
| Total Error Over 0 to +70°C <sup>6</sup>                                       |   |                          |
| Unipolar   | ±0.08% FSR typ, ±0.15% FSR max              | *                        |
| Bipolar  | ±0.06% FSR typ, ±0.10% FSR max              | *                        |
| Gain   | ±15ppm/°C typ, ±30ppm/°C max                | *                        |
| Exclusive of Internal Reference  | ±5ppm/°C typ, ±7ppm/°C max                  | *                        |
| Unipolar Offset  | ±1ppm FSR/°C typ, ±3ppm FSR/°C max          | *                        |
| Bipolar Offset   | ±5ppm FSR/°C typ, ±10ppm FSR/°C max         | *                        |
| <b>CONVERSION SPEED/V Models</b>   |   |                          |
| Settling Time to ±0.01% of FSR   |   |                          |
| For FSR Change   |   |                          |
| with 10kΩ Feedback <sup>7</sup>  | 5μs typ                                     | *                        |
| with 5kΩ Feedback  | 3μs typ                                     | *                        |
| For 1LSB Change  | 1.5μs typ                                   | *                        |
| Slew Rate  | 10V/μs min, 15V/μs typ                      | *                        |
| <b>CONVERSION SPEED/I Models</b>   |   |                          |
| Settling Time to ±0.01% of FSR   |   |                          |
| For FSR Change   |   |                          |
| 10 to 100Ω Load  | 300ns typ                                   | *                        |
| 1kΩ Load   | 1μs typ                                     | *                        |
| <b>ANALOG OUTPUT/V Models</b>  |   |                          |
| Ranges <sup>7</sup>  | ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V       | 0 to +10V                |
| Output Current   | ±5mA min                                    | *                        |
| Output Impedance (dc)  | 0.05Ω typ                                   | *                        |
| Short Circuit Duration   | Indefinite to Common                        | *                        |
| <b>ANALOG OUTPUT/I Models</b>  |   |                          |
| Ranges   | ±1mA, 0 to -2mA typ                         | 0 to -2mA typ            |
| Output Impedance - Bipolar   | 3.2kΩ typ                                   | *                        |
| Output Impedance - Unipolar  | 6.6kΩ typ                                   | *                        |
| Compliance   | +10V, -1.5V                                 | *                        |
| <b>INTERNAL REFERENCE VOLTAGE</b>  |   |                          |
| Tempco of Drift  | +6.3V ±2% max                               | *                        |
| External - Use Current <sup>8</sup>  | ±10ppm/°C typ, ±20ppm/°C max                | *                        |
| Output Impedance   | +2.5mA max                                  | *                        |
|  | 1.5Ω typ                                    | *                        |
| <b>POWER SUPPLY SENSITIVITY</b>  |   |                          |
| +15V Supply  | ±0.002% FSR/% V <sub>S</sub> max            | *                        |
| -15V and +5V Supplies  | ±0.002% FSR/% V <sub>S</sub> max            | *                        |
| <b>POWER SUPPLY REQUIREMENTS</b>   |   |                          |
| DAC80  | ±14V dc, +4.75V dc min                      | *                        |
|  | ±15V dc, +5V dc typ                         | *                        |
|  | ±16V dc, +16V dc max                        | *                        |
| DAC80Z <sup>7</sup>  | ±11.4V dc, +4.75V dc min                    | *                        |
|  | ±12V dc, +5V dc typ                         | *                        |
|  | ±16V dc, +16V dc max                        | *                        |
| Supply Drain   |   |                          |
| +15/+12V (Including 5mA Load)  | 10mA typ, 20mA max                          | *                        |
| -15/-12V (Including 5mA Load)  | -20mA typ, -35mA max                        | *                        |
| +5V (Logic Supply)   | 8mA typ, 20mA max                           | *                        |
| <b>TEMPERATURE RANGE</b>   |   |                          |
| Specification  | 0 to +70°C max                              | *                        |
| Operating  | -25°C to +85°C max                          | *                        |
| Storage  | -55°C to +100°C                             | *                        |

## NOTES

<sup>1</sup>Least Significant Bit (LSB).

<sup>2</sup>Adjustable to zero with external trim potentiometer.

<sup>3</sup>FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.

<sup>4</sup>To maintain drift spec internal feedback resistors must be used for current output models.

<sup>5</sup>See discussion on page 151S.

<sup>6</sup>With gain and offset errors adjusted to zero at +25°C. See discussion on page 151S.

<sup>7</sup>DAC80Z supply range is ±12.0V min to ±16.0V max for ±5V and 0 to +5V outputs.

<sup>8</sup>Maximum with no degradation of specifications with constant load.

Specifications subject to change without notice.

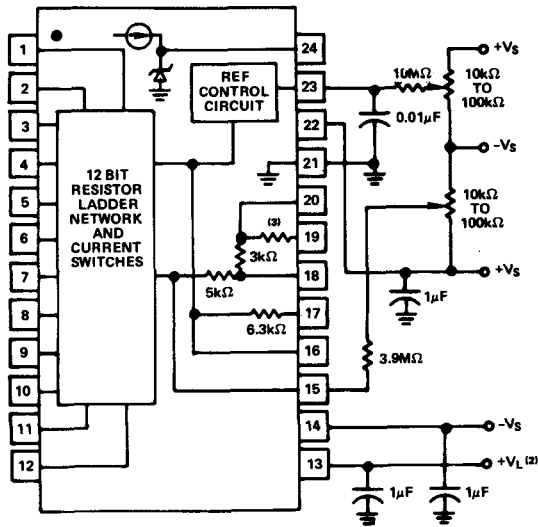


Figure 1. External Adjustment and Voltage Supply Connection Diagram, Current Model

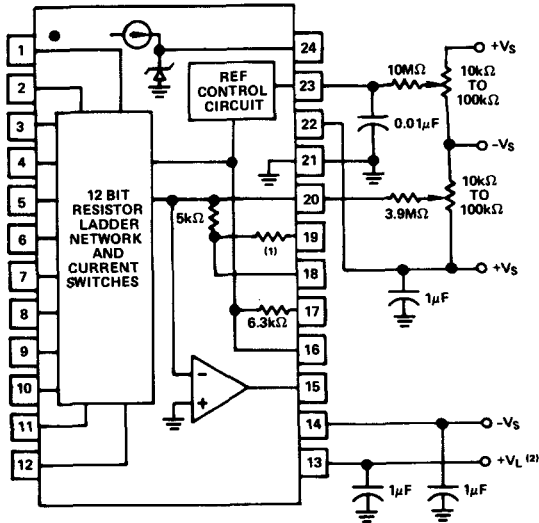


Figure 2. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

**NOTES:**

1.  $3k\Omega$  for CCD models.  $5k\Omega$  for CBI models.
2. If connected to  $+V_S$  which is permissible, power dissipation increases 200mW.
3. CBI model,  $2k\Omega$ ; CCD model,  $0\Omega$  and pin 20 has no internal connection.

**PIN CONFIGURATION**

24 LEAD DUAL IN-LINE PACKAGE

| I Models     | Pin # | V Models     |
|--------------|-------|--------------|
| (MSB) Bit 1  | 1     | Bit 1(MSB)   |
| Bit 2        | 2     | Bit 2        |
| Bit 3        | 3     | Bit 3        |
| Bit 4        | 4     | Bit 4        |
| Bit 5        | 5     | Bit 5        |
| Bit 6        | 6     | Bit 6        |
| Bit 7        | 7     | Bit 7        |
| Bit 8        | 8     | Bit 8        |
| Bit 9        | 9     | Bit 9        |
| Bit 10       | 10    | Bit 10       |
| Bit 11       | 11    | Bit 11       |
| (LSB) Bit 12 | 12    | Bit 12 (LSB) |

| I Models         | Pin # | V Models         |
|------------------|-------|------------------|
| Logic Supply     | 13    | Logic Supply     |
| $-V_S$           | 14    | $-V_S$           |
| $I_{OUT}$        | 15    | $V_{OUT}$        |
| Ref Input        | 16    | Ref Input        |
| Bipolar Offset   | 17    | Bipolar Offset   |
| Scaling Network  | 18    | 10V Range        |
| Scaling Network  | 19    | 20V Range        |
| Common           | 20    | Summing Junction |
| Common           | 21    | Common           |
| $+V_S$           | 22    | $+V_S$           |
| Gain Adjust      | 23    | Gain Adjust      |
| $6.3V_{REF}$ Out | 24    | $6.3V_{REF}$ Out |

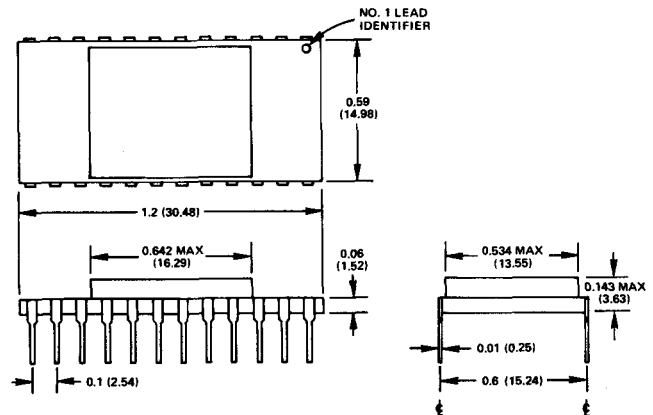


Figure 3. Outline Dimensions (Dimensions shown in inches and (mm))

**AD DAC80 ORDERING AND PRICING GUIDE**

| MODEL           | INPUT CODE           | OUTPUT MODE | SUPPLY RANGE |
|-----------------|----------------------|-------------|--------------|
| AD DAC80-CBI-V  | Binary               | Voltage     | Normal       |
| AD DAC80-CBI-I  | Binary               | Current     | Normal       |
| AD DAC80-CCD-V  | Binary Coded Decimal | Voltage     | Normal       |
| AD DAC80-CCD-I  | Binary Coded Decimal | Current     | Normal       |
| AD DAC80Z-CBI-V | Binary               | Voltage     | Extended     |
| AD DAC80Z-CBI-I | Binary               | Current     | Extended     |
| AD DAC80Z-CCD-V | Binary Coded Decimal | Voltage     | Extended     |
| AD DAC80Z-CCD-I | Binary Coded Decimal | Current     | Extended     |

## DIGITAL INPUT CODES

The AD DAC80 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB or CTC.

| DIGITAL INPUT |                | ANALOG OUTPUT |   |                             |                             |
|---------------|----------------|---------------|---|-----------------------------|-----------------------------|
| CBI Models    | MSB            | LSB           | CSB Compl.<br>Straight Binary                 | COB Compl.<br>Offset Binary | CTC* Compl.<br>Two's Compl. |
|               |                | 000000000000  |   | +Full Scale                 | +Full Scale                 |
|               | 011111111111   |               | +½ Full Scale                                 | Zero                        | -Full Scale                 |
|               | 100000000000   |               | Mid-scale -1LSB                               | -1 LSB                      | +Full Scale                 |
|               | 111111111111   |               | Zero  | -Full Scale                 | Zero                        |
| CCD Models    | MSB            | LSB           | CCD<br>Complementary Coded Decimal - 3 Digits |                             |                             |
|               | 0110 0110 0110 |               | +Full Scale                                   |                             |                             |
|               | 1111 1111 1111 |               | Zero  |                             |                             |

\*Invert the MSB of the COB code with an external inverter to obtain CTC code.

Table 1. Digital Input Codes

## ACCURACY

Accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Of these three specifications, the linearity error specification is the most important since it can not be corrected for. The linearity error of the AD DAC80 is specified over its entire temperature range. This means that the analog output will not vary by more than  $\pm 1/2$ LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0 to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of  $\pm 1/2$ LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next. Monotonicity over the 0 to +70°C range is guaranteed in the AD DAC80 to insure that the analog output will not decrease with increasing input digital codes.

## DRIFT

**Gain Drift** is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each AD DAC80 model at 0°C; +25°C and +70°C; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change.

**Offset Drift** is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, +25°C and +70°C. The maximum change in offset is referenced to the offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

## SETTLING TIME

Settling time for each AD DAC80 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 4).

**Voltage Output Models.** Three settling times are specified to  $\pm 0.01\%$  of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0 1 1 1 ... 1 1 to 1 0 0 0 ... 0 0), the point at which the worst case settling time occurs.

**Current Output Models.** Two settling times are specified to  $\pm 0.01\%$  of FSR. Each is given for current models connected with two different resistive loads: 10 to 100 ohms and 1000 to 1875 ohms. Internal resistors are provided for connecting nominal load resistances of approximately 1000 to 1800 ohms for output voltage range of  $\pm 1$ V and 0 to -2V. (See Table IV, Page 153S).

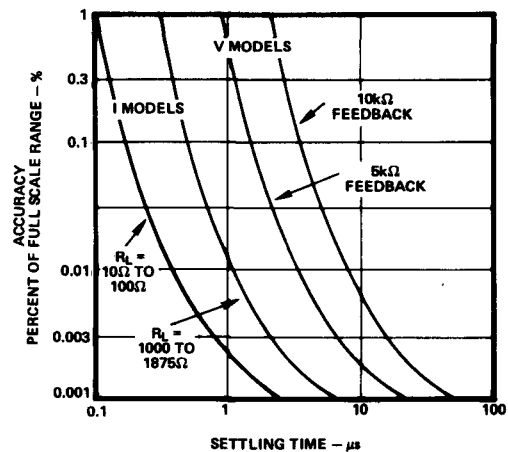


Figure 4. Full Scale Range Settling Time vs. Accuracy

## COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy.

## POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a per cent of FSR per cent of change in either the positive, negative, or logic supplies about the nominal power supply voltages.

## REFERENCE SUPPLY

All AD DAC80 models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) is accurate to  $\pm 2\%$  and must be connected to the Reference Input (pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven off of the reference will result in gain variations of the AD DAC80. All gain adjustments should be made under constant load conditions.

## ANALYZING DEVICE ACCURACY OVER THE TEMPERATURE RANGE

For the purposes of temperature drift analysis, the major device components are shown in Figure 5. The reference element and buffer amplifier drifts are combined to give the total reference temperature coefficient, which is specified as  $\pm 20\text{ppm}/^\circ\text{C}$  max. The input reference current to the DAC,  $I_{\text{REF}}$ , is developed from the internal reference and will show the same drift rate as the reference voltage. The DAC output current,  $I_{\text{REF}}$ , which is a function of the digital input code, is designed to track  $I_{\text{REF}}$ ; if there is a slight mismatch in these currents over temperature, it will contribute to the gain T.C. The bipolar offset resistor,  $R_{\text{BP}}$ , and gain setting resistor,  $R_{\text{GAIN}}$ , also have temperature coefficients which contribute to system drift errors. The input offset voltage drift of the output amplifier, OA, also contributes a small error.

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input which calls for zero output to a point which is defined as full scale. A specification for total error over temperature assumes that both the zero and full scale points have been trimmed for zero error at  $+25^\circ\text{C}$ . Total error is normally expressed a percentage of the full scale range. In the bipolar situation, this means the total range from  $-V_{\text{FS}}$  to  $+V_{\text{FS}}$ .

Several new design concepts not previously used in DAC80-type devices contribute to a reduction in all the error factors over temperature. The incorporation of low temperature coefficient silicon-chromium thin-film resistors deposited on a single chip, a patented, fully differential, emitter weighted, precision current steering cell structure, and a T.C. trimmed buried zener diode reference element results in superior wide temperature range performance. The full scale gain setting resistors and bipolar offset resistor are also fabricated on the chip with the same SiCr material as the ladder network, resulting in low gain and offset drift.

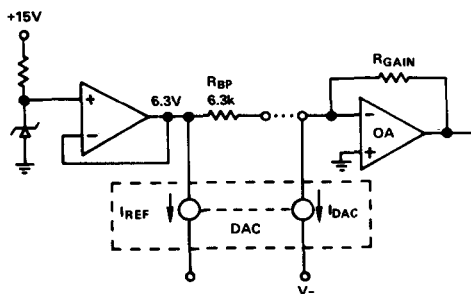


Figure 5. Bipolar Configuration

## MONOTONICITY AND LINEARITY

The initial linearity error of  $\pm 1/2\text{LSB}$  max and the differential linearity error of  $\pm 3/4\text{LSB}$  max guarantee monotonic performance over the range of 0 to  $+70^\circ\text{C}$ . It can therefore be assumed that linearity errors are insignificant in computation of total temperature errors.

## UNIPOLAR ERRORS

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift of  $3\text{ppm}/^\circ\text{C}$  max (which comes from leakage currents and drift in the output amplifier (OA)) causes a linear shift in the transfer curve as shown in Figure 6. The gain drift causes a change in the slope of the curve and results from reference drift, DAC drift, and drift in  $R_{\text{GAIN}}$  relative to the DAC resistors for a total of  $30\text{ppm}/^\circ\text{C}$  max. Total absolute error due to all of these effects is guaranteed to be less than  $\pm 0.15\%$  of full scale from 0 to  $+70^\circ\text{C}$ .

## BIPOLAR RANGE ERRORS

The analysis is slightly more complex in the bipolar mode. In this mode  $R_{\text{BP}}$  is connected to the summing node of the output amplifier (see Figure 5) to generate a current which, exactly balances the current of the MSB so that the output voltage is zero with only the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in  $I_{\text{REF}}$  and thus  $I_{\text{DAC}}$ , so that  $I_{\text{DAC}}$  will always be exactly balanced by  $I_{\text{BP}}$  with the MSB turned on. This effect is shown in Figure 6. The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts discussed before will have the same effect on the bipolar offset. A mismatch of  $R_{\text{BP}}$  to the DAC resistors is usually the largest component of bipolar drift, but in the AD DAC80 this error is held to  $10\text{ppm}/^\circ\text{C}$  max. Gain drift in the DAC also contributes to bipolar offset drift, as well as full scale drift, but again is held to  $7\text{ppm}/^\circ\text{C}$  max. The total of all these errors is held to  $\pm 0.1\%$  of full scale from 0 to  $+70^\circ\text{C}$ . Note that, in the bipolar ranges, full scale is defined as the total range from  $-V_{\text{FS}}$  to  $+V_{\text{FS}}$ .

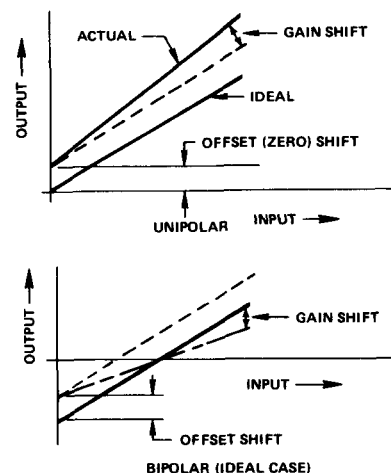


Figure 6. Unipolar and Bipolar Drifts

# Using the AD DAC80

## ±12 VOLT SUPPLY OPERATION

The Z models will operate with supply voltages as low as ±11.4V. It is recommended that output voltage ranges -10V to +10V and 0V to +10V not be used with the Z model if the supply voltages are ever less than the recommended ±12V. The output amplifier may saturate if  $|V_{SUPPLY}| - |V_{OUT}|_{max} < 2.0V$ . This applies to units with both CBI and CCD input codes. Except for operation at lower supply voltages, the AD DAC80Z and AD DAC80 operation is identical.

## POWER SUPPLY CONNECTIONS

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams (Figures 1 and 2). These capacitors (1μF electrolytic recommended) should be located close to the AD DAC80. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for optimum high frequency performance.

## EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. These potentiometers should be connected as shown in the block diagrams on Page 149S and adjusted as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the

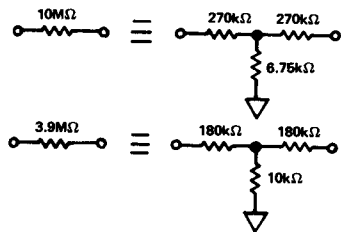


Figure 7. Equivalent Resistances

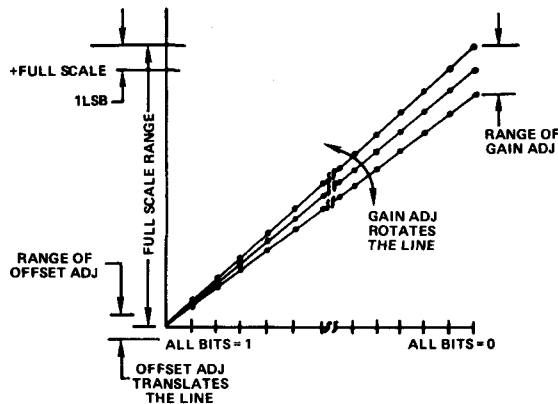


Figure 8. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter. (Input, Horizontal; Output, Vertical).

AD DAC80 to prevent noise pick-up. If it is not convenient to use these high-value resistors, a functionally equivalent "T" network, as shown in Figure 7 may be substituted in each case. The gain adjust (pin 23) is a high impedance point and a 0.01μF ceramic capacitor should be connected from this pin to common to prevent noise pick-up. Figures 8 and 9 show the relationship of the OFFSET and GAIN adjustments to the unipolar and bipolar D/A converters.

**Offset Adjustment.** For unipolar (CSB, CCD) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output. For bipolar (COD, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is -10V. See Table II for corresponding codes and the block diagrams on Page 149S for offset adjustment connections.

**Gain Adjustment.** For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the block diagrams for gain adjustment connections.

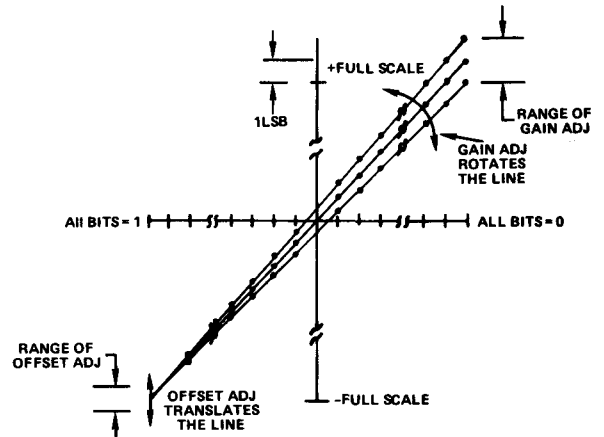


Figure 9. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A CONVERTER. (Input, Horizontal; Output, Vertical).

| DIGITAL INPUT        |           | ANALOG OUTPUT |           |           |           |
|----------------------|-----------|---------------|-----------|-----------|-----------|
| 12 Bit Resolution    |           | VOLTAGE*      |           | CURRENT   |           |
| MSB                  | LSB       | 0 to +10V     | ±10V      | 0 to -2mA | ±1mA      |
| 000000000000         |           | +9.9976V      | +9.9951V  | -1.9995mA | -0.9995mA |
| 011111111111         |           | +5.0000V      | 0.0000V   | -1.0000mA | 0.0000mA  |
| 100000000000         |           | +4.9976V      | -0.0049V  | -0.9995mA | +0.0005mA |
| 111111111111         |           | 0.0000V       | -10.0000V | 0.0000mA  | 0.488μV   |
|                      | 1LSB      | 2.44mV        | 4.88mV    | 0.488mA   | +1.000mA  |
| 3 Digital Resolution |           |               |           |           |           |
| MSB                  | LSB       |               |           |           |           |
| 0110                 | 0110 0110 | +9.990V**     | N/A       | -1.249mA  | N/A       |
| 0110                 | 0110 1111 | +9.900V       | N/A       | -1.238mA  | N/A       |
| 0110                 | 1111 1111 | +9.000V       | N/A       | -1.125mA  | N/A       |
| 1111                 | 1111 1111 | 0.000V        | N/A       | 0.000mA   | N/A       |
|                      | 1LSB      | 10.00mV       | N/A       | 1.25μA    | N/A       |

\*To obtain values for other binary (CBI) ranges: 0 to +5V range: divide 0 to +10V range values by 2; ±5V range: divide ±10V range values by 2; ±2.5V range: divide ±10V range values by 4.

\*\*Normal full scale range with correct codes; output can go higher if illegal codes are applied.

Table II. Digital Input/Analog Output

## VOLTAGE OUTPUT MODELS

Internal scaling resistors provided in the DAC80 may be connected to produce bipolar output voltage ranges of  $\pm 10$ ,  $\pm 5$  or  $\pm 2.5$ V or unipolar output voltage ranges of 0 to +5 or 0 to +10V (see Figure 10).

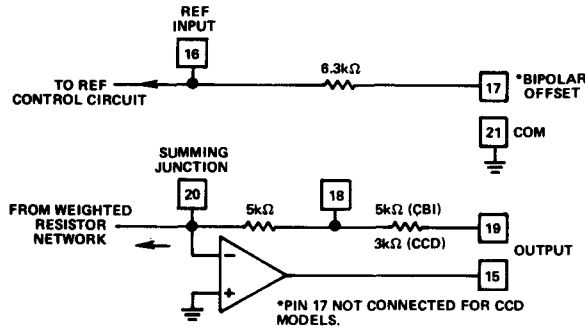


Figure 10. Output Amplifier Voltage Range Scaling Circuit

Gain and offset drift are minimized in the DAC80 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full scale range change: 5 microseconds for 8kΩ or 10kΩ feedback resistors; 3 microseconds for a 5kΩ feedback resistor.

| Output Range | Digital Input Codes | Connect Pin 15 to | Connect Pin 17 to | Connect Pin 19 to | Connect Pin 16 to |
|--------------|---------------------|-------------------|-------------------|-------------------|-------------------|
| $\pm 10$ V   | COB or CTC          | 19                | 20                | 15                | 24                |
| $\pm 5$ V    | COB or CTC          | 18                | 20                | N.C.              | 24                |
| $\pm 2.5$ V  | COB or CTC          | 18                | 20                | 20                | 24                |
| 0 to +10V    | CSB                 | 18                | 21                | N.C.              | 24                |
| 0 to +5V     | CSB                 | 18                | 21                | 20                | 24                |
| 0 to +10V    | CCD                 | 19                | N.C.              | 15                | 24                |

Table III. Output Voltage Range Connections-Voltage Model AD DAC80

The equivalent resistive scaling network and output circuit of the current model are shown in Figures 11 and 12. External  $R_{LS}$  or  $R_{LP}$  resistors are required to produce exactly 0 to -2V or  $\pm 1$ V output. TCR of these resistors should be  $\pm 100$ ppm/ $^{\circ}$ C or less to maintain the AD DAC80 output specifications. If exact output ranges are not required, the external resistors are not needed.

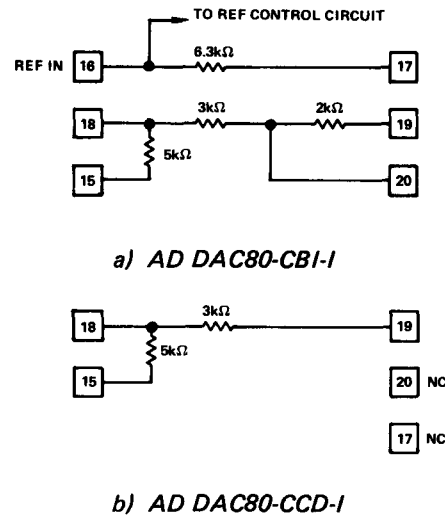


Figure 11. Internal Scaling Resistors

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of  $\pm 1$ V or 0 to -2V. These resistors ( $R_{LI}$ ) are an integral part of the AD DAC80 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external  $R_L$  (or  $R_F$ ) resistors should have a TCR of  $\pm 25$ ppm/ $^{\circ}$ C or less to minimize drift. This will typically add  $\pm 50$ ppm/ $^{\circ}$ C to the TCR of  $R_L$  (or  $R_F$ ) to the total drift.

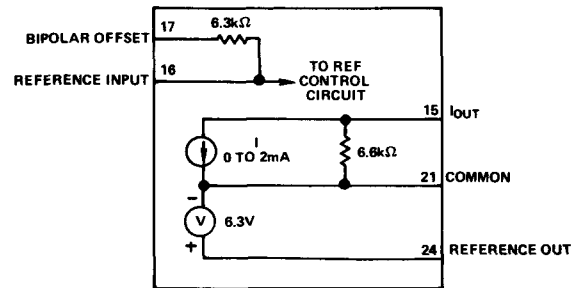


Figure 12. AD DAC80 Current Model Equivalent Output Circuit

| Digital Input Codes | Output Range | Internal Resistance $R_{LI}$ | 1% Metal Film External Resistance $R_{LS}$ $R_{LP}$ | $R_{LI}$ Connections |                   |                   | Reference<br>Connect Pin 16 to | Bipolar Offset    |                           |                     |
|---------------------|--------------|------------------------------|---|----------------------|-------------------|-------------------|--------------------------------|-------------------|---------------------------|---------------------|
|                     |              |                              |   | Connect Pin 15 to    | Connect Pin 18 to | Connect Pin 20 to |                                | Connect Pin 17 to | $R_{LS}$                  | $R_{LP}$            |
| CSB                 | 0 to -2V     | 0.968kΩ                      | 210Ω N/A  | 20                   | 19 & $R_{LS}$     | 15                | 24                             | Com (21)          | Between Pin 18 & Com (21) | N/A                 |
| CCD                 | 0 to -2V     | 3kΩ                          | N/A 3.57kΩ  | N.C.                 | Com (21)          | N.C.              | 24                             | N.C.              | N/A                       | Between Pin 15 & 21 |
| COB or CTC          | $\pm 1$ V    | 1.2kΩ                        | 249Ω N/A  | 18                   | 19                | $R_{LS}$          | 24                             | 15                | Between Pin 20 & Com (21) | N/A                 |

Table IV. Current Model/Resistive Load Connections

### DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance,  $R_L = R_{LI} + R_{LS}$ , connected as shown in Figure 13 will generate a voltage range,  $V_{OUT}$ , determined by:

$$V_{OUT} = -2\text{mA} \left( \frac{6.6\text{k} \times R_L}{6.6\text{k} + R_L} \right)$$

Where  $R_L \text{ max} = 1.54\text{k}\Omega$

and  $V_{OUT} \text{ max} = -2.5\text{V}$

To achieve specified drift, connect the internal scaling resistor ( $R_{LI}$ ) as shown in Table IV to an external metal film trim resistor ( $R_{LS}$ ) to provide full scale output voltage range of 0 to  $-2\text{V}$ . With  $R_{LS} = 0$ ,  $V_{OUT} = -1.69\text{V}$ .

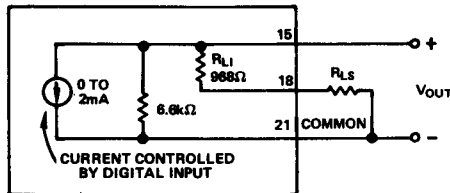


Figure 13. Equivalent Circuit AD DAC80-CBI-I Connected for Unipolar Voltage Output with Resistive Load

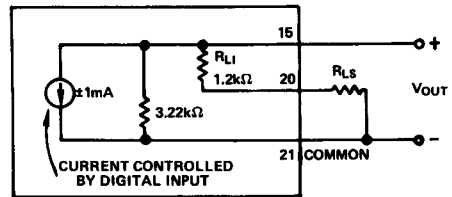


Figure 15. AD DAC80-CBI-I Connected for Bipolar Output Voltage with Resistive Load

where  $I_{OUT}$  is the AD DAC80 output current and  $R_F$  is the feedback resistor. Using the internal feedback resistors of the current model AD DAC80 provides output voltage ranges the same as the voltage model AD DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table V and Figure 16.

| Output Range       | Digital Input Codes | Connect A to | Connect Pin 17 to | Connect Pin 19 to | Connect Pin 16 to |
|--------------------|---------------------|--------------|-------------------|-------------------|-------------------|
| $\pm 10\text{V}$   | COB or CTC          | 19           | 15                | A                 | 24                |
| $\pm 5\text{V}$    | COB or CTC          | 18           | 15                | N.C.              | 24                |
| $\pm 2.5\text{V}$  | COB or CTC          | 18           | 15                | 15                | 24                |
| 0 to $+10\text{V}$ | CSB                 | 18           | 21                | N.C.              | 24                |
| 0 to $+5\text{V}$  | CSB                 | 18           | 21                | 15                | 24                |
| 0 to $+10\text{V}$ | CCD                 | 19           | N.C.              | A                 | 24                |

Table V. Voltage Range of Current Output AD DAC80

CCD Input Code: Connect the internal scaling resistors as shown in Table V and add an external metal film resistor ( $R_{LP}$ ) in parallel as shown in Figure 14 to obtain a 0 to  $-2\text{V}$  full scale output voltage range for CCD input codes.

$$\text{With } R_L = \frac{R_{LI} \times R_{LP}}{R_{LI} + R_{LP}}$$

$$V_{OUT} = -1.25\text{mA} \left( \frac{6.9\text{k} \times R_L}{6.9\text{k} + R_L} \right)$$

If  $R_{LP} = \infty$ ,  $V_{OUT} = -3.62\text{V}$

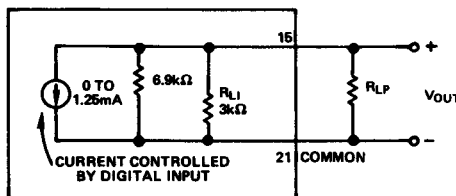
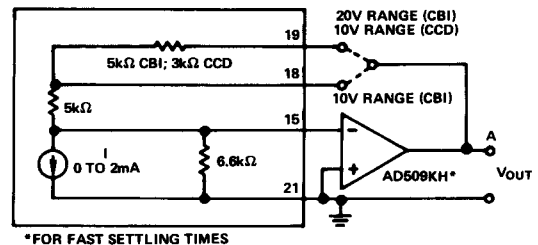


Figure 14. AD DAC80-CCD-I Connected for Voltage Output with Resistive Load



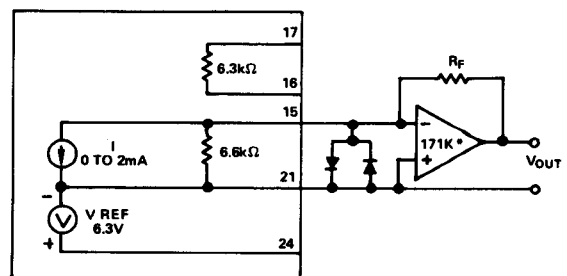
\*FOR FAST SETTLING TIMES

Figure 16. External Op Amp – Using Internal Feedback Resistors

### OUTPUT LARGER THAN 20V RANGE

For output voltage ranges larger than  $\pm 10\text{V}$ , a high voltage op amp may be employed with an external feedback resistor. Use  $I_{OUT}$  values of  $\pm 1\text{mA}$  for bipolar voltage ranges and  $-2\text{mA}$  for unipolar voltage ranges (see Figure 17). Use protection diodes when a high voltage op amp is used.

The feedback resistor,  $R_F$ , should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between  $R_F$  and the internal scaling resistor network. This will typically add  $50\text{ppm}/^\circ\text{C} + R_F$  drift to total drift.



\*FOR OUTPUT VOLTAGE SWINGS UP TO 140V p-p.

Figure 17. External Op Amp – Using External Feedback Resistors

### DRIVING A RESISTOR LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 15,  $R_L = R_{LI} + R_{LS}$ .  $V_{OUT}$  is determined by:

$$V_{OUT} = \pm 1\text{mA} \left( \frac{R_L \times 3.22\text{k}}{R_L + 3.22\text{k}} \right)$$

Where  $R_L \text{ max} = 11.18\text{k}\Omega$

$V_{OUT} \text{ max} = \pm 2.5\text{V}$

To achieve specified drift, connect the internal scaling resistors ( $R_{LI}$ ) as shown in Table IV for the COB or CTC codes and add an external metal film resistor ( $R_{LS}$ ) in series to obtain a full scale output range of  $\pm 1\text{V}$ . In this configuration, with  $R_{LS}$  equal to zero, the full scale range will be  $\pm 0.874\text{V}$ .

### DRIVING AN EXTERNAL OP AMP

The current model AD DAC80 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. As seen in Figure 16.

$$V_{OUT} = I_{OUT} \times R_F$$

### FEATURES

Improved Replacement for Standard DAC85

3 Chip, High Reliability Construction

Low Power Dissipation

Laser-Trimmed to High Accuracy:

$\pm 3/4$ LSB Max Nonlinearity,  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
(AD DAC85 MIL)

High Stability, High Current Output

Buried Zener Reference

On-Board Output Amplifier (V Models)

24 Lead Side Brazed Ceramic DIP

### PRODUCT DESCRIPTION

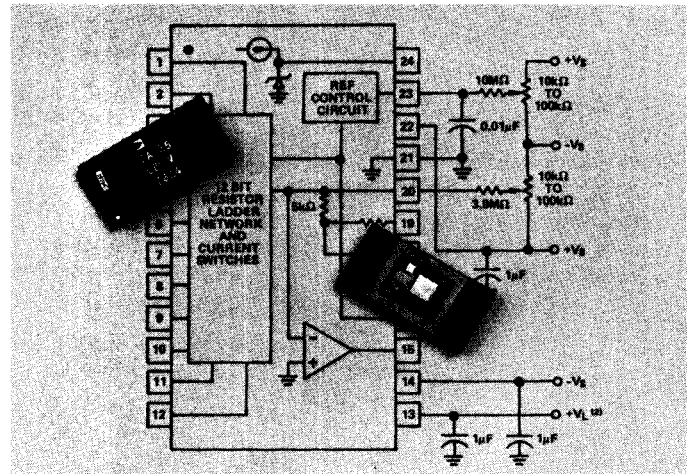
The AD DAC85 is a high performance 12-bit digital-to-analog converter, consisting of matched bipolar switches, a precision resistor network, a low-drift high-stability voltage reference and an optional output amplifier. Options include TTL compatible complementary 12-bit binary (CBI) or 3 digit BCD (CCD) input codes, as well as current or voltage output modes. The AD DAC85 offers output voltage ranges of  $\pm 2.5$ ,  $\pm 5$ ,  $\pm 10$ , 0 to +5, or 0 to +10 volts (V models); output current ranges (I models) are either  $\pm 1\text{mA}$  or 0 to  $-2\text{mA}$ .

Advanced circuit design and precision processing techniques result in significant performance advantages over conventional, larger, standard DAC85 devices. An innovative 3-chip construction improves reliability by a factor of five.<sup>1</sup> The AD DAC85 incorporates a fully differential, non-saturating precision current switching cell structure\* which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability, SiCr thin film resistors are trimmed with a fine resolution laser, resulting in low differential nonlinearity errors. A low noise, high stability subsurface zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature cycle characteristics which challenge the best discrete zener references.

The AD DAC85 is recommended for all 12-bit D/A converter applications where reliability and performance over temperature are of paramount importance.

\*COVERED BY PATENT NUMBERS: 3,978,473; RE 28,633; 4,020,486; 3,747,088; 3,803,590; 3,961,326.

<sup>1</sup>For details of calculations see Application Note, "AD DAC85 Reliability Predictions".



### PRODUCT HIGHLIGHTS

1. The AD DAC85 directly replaces other devices of this type with significant increases in performance.
2. 3-Chip IC construction makes the AD DAC85 the optimum choice for applications where performance and reliability are major considerations.
3. System performance upgrading is possible without redesign.
4. The AD DAC85 offers a maximum nonlinearity error of  $\pm 0.012\%$ ,  $\pm 20\text{ppm}/^{\circ}\text{C}$  maximum gain drift, and a total accuracy drift in the bipolar configuration of  $\pm 10\text{ppm}/^{\circ}\text{C}$  maximum.
5. The low T.C. Binary ladder guarantees that all AD DAC85 units will be monotonic over the specified temperature range.
6. Reduced power consumption requirements result in improved stability and shorter warm-up time.
7. The precision buried zener reference can supply up to 2.5mA for use elsewhere in the application.
8. Voltage or current output modes are available in either of the BCD or binary input formats.



# SPECIFICATIONS (Typical @ +25°C unless otherwise specified)

| MODEL  | AD DAC85C                         | AD DAC85C | AD DAC85    | AD DAC85    | AD DAC85LD  | AD DAC85MIL | UNITS                     |
|--|-----------------------------------|-----------|-------------|-------------|-------------|-------------|---------------------------|
|  | CBI                               | CCD       | CBI         | CCD         | CBI         | CBI         |                           |
| <b>DIGITAL INPUT</b>   |                                   |           |             |             |             |             |                           |
| Resolution   | 12                                | 3         | 12          | 3           | 12          | 12          | Bits<br>Digits            |
| Logic Levels (TTL Compatible)                                    |                                   |           |             |             |             |             |                           |
| Logic "1" (at +1μA)  | +2V dc min, +5.5V dc max          | *         | *           | *           | *           | *           | V                         |
| Logic "0" (at -100μA)  | 0V dc min, +0.8V dc max           | *         | *           | *           | *           | *           | V                         |
| <b>TRANSFER CHARACTERISTICS</b>                                  |                                   |           |             |             |             |             |                           |
| <b>ACCURACY</b>  |                                   |           |             |             |             |             |                           |
| Linearity Error @ 25°C (max)                                     | ±1/2                              | ±1/4      | ±1/2        | ±1/4        | ±1/2        | ±1/2        | LSB                       |
| 0 to +70°C (max)   | ±1/2                              | ±1/2      |             |             |             |             | LSB                       |
| -25°C to +85°C (max)   |                                   |           | ±1/2        | ±1/2        | ±1/2        | ±1/2        | LSB                       |
| -55°C to +125°C (max)  |                                   |           |             |             |             | ±3/4        | LSB                       |
| Differential Linearity Error                                     | ±1/2                              | *         | *           | *           | *           | *           | LSB                       |
| Gain Error <sup>1</sup>  | ±0.1                              | *         | *           | *           | *           | *           | %                         |
| Offset Error <sup>1</sup>  | ±0.05                             | *         | *           | *           | *           | *           | % of FSR <sup>2</sup>     |
| Minimum Temperature Range for<br>Guaranteed Monotonicity         | 0 to +70                          | 0 to +70  | -25 to +85  | -25 to +85  | -25 to +85  | -55 to +125 | °C                        |
| <b>DRIFT<sup>3</sup></b>   |                                   |           |             |             |             |             |                           |
| Gain 0 to +70°C (max)  | ±20                               | ±20       | ±20         | ±20         | ±10         | ±20         | ppm/°C                    |
| -25°C to +85°C (max)   | —                                 | —         | ±20         | ±20         | ±10         | ±20         | ppm/°C                    |
| -55°C to +125°C (max)  | —                                 | —         | —           | —           | —           | ±20         | ppm/°C                    |
| Offset   |                                   |           |             |             |             |             |                           |
| Unipolar 0 to +70°C  | +1                                | +1        |             |             |             |             | ppm of FSR/°C             |
| -25°C to +85°C   |                                   |           | ±1          | ±1          | ±1          | ±1          | ppm of FSR/°C             |
| -55°C to +125°C  |                                   |           |             |             |             |             | ppm of FSR/°C             |
| Bipolar 0 to +70°C (max)   | ±10                               |           |             |             |             | ±2          | ppm of FSR/°C             |
| -25°C to +85°C (max)   |                                   |           | ±10         |             | ±5          | ±10         | ppm of FSR/°C             |
| -55°C to +125°C (max)  |                                   |           |             |             |             | ±10         | ppm of FSR/°C             |
| <b>CONVERSION SPEED</b>  |                                   |           |             |             |             |             |                           |
| <b>Voltage Models</b>  |                                   |           |             |             |             |             |                           |
| Settling Time to ±0.01% of FSR<br>for FSR change                 |                                   |           |             |             |             |             |                           |
| with 10kΩ Feedback   | 5                                 | *         | *           | *           | *           | *           | μs                        |
| with 5kΩ Feedback  | 3                                 | *         | *           | *           | *           | *           | μs                        |
| for 1LSB change  | 1.5                               | *         | *           | *           | *           | *           | μs                        |
| Slew Rate  | 20                                | *         | *           | *           | *           | *           | V/μs                      |
| <b>Current Models</b>  |                                   |           |             |             |             |             |                           |
| Settling Time to ±0.01% of FSR<br>for FSR change 10 to 100Ω load | 300                               | *         | *           | *           | *           | *           | ns                        |
| 1kΩ load   | 1                                 | *         | *           | *           | *           | *           | μs                        |
| <b>ANALOG OUTPUT</b>   |                                   |           |             |             |             |             |                           |
| Voltage Models Ranges — CBI Units                                | ±2.5, ±5, ±10, +5, +10            | *         | *           | *           | *           | *           | V                         |
| CCD Units  | +10                               | *         | *           | *           | *           | *           | V                         |
| Output Current (min)   | ±5                                | *         | *           | *           | *           | *           | mA                        |
| Output Impedance (dc)  | 0.05                              | *         | *           | *           | *           | *           | Ω                         |
| <b>Current Models</b>  |                                   |           |             |             |             |             |                           |
| Ranges   | ±1, -2                            | *         | *           | *           | *           | *           | mA                        |
| Output Impedance - Bipolar                                       | 3.2                               | *         | *           | *           | *           | *           | kΩ                        |
| Unipolar   | 6.65                              | *         | *           | *           | *           | *           | kΩ                        |
| Compliance   | -2.5, +10.5                       | *         | *           | *           | *           | *           | V                         |
| Internal Reference Voltage (V <sub>r</sub> )                     | 6.3                               | *         | *           | *           | *           | *           | V                         |
| Output Impedance   | 1.5                               | *         | *           | *           | *           | *           | Ω                         |
| Max. External Current <sup>4</sup>                               | 2.5                               | *         | *           | *           | *           | *           | mA                        |
| Max Reference Error  | ±2                                | *         | *           | *           | *           | *           | %                         |
| Tempco of Drift  | ±10 typ, ±20 max                  | *         | *           | *           | *           | *           | ppm of V <sub>r</sub> /°C |
| <b>POWER SUPPLY SENSITIVITY</b>                                  |                                   |           |             |             |             |             |                           |
| +15V Supply  | ±0.002                            | *         | *           | *           | *           | *           | % of FSR/% V <sub>S</sub> |
| -15 and +5V Supplies   | ±0.002                            | *         | *           | *           | *           | *           | % of FSR/% V <sub>S</sub> |
| <b>POWER SUPPLY REQUIREMENTS</b>                                 |                                   |           |             |             |             |             |                           |
| Rated Voltage  | ±15 and +5                        | *         | *           | *           | *           | *           | V                         |
| Range  | ±14.5 to ±15.5 and +4.50 to +15.5 | *         | *           | *           | *           | *           | V                         |
| <b>Supply Drain</b>  |                                   |           |             |             |             |             |                           |
| +15V (including 5mA load)  | 15 typ, 20 max                    | *         | *           | *           | *           | *           | mA                        |
| +5V  | 15 typ, 20 max                    | *         | *           | *           | *           | *           | mA                        |
| -15V   | 25 typ, 30 max                    | *         | *           | *           | *           | *           | mA                        |
| <b>TEMPERATURE RANGE</b>   |                                   |           |             |             |             |             |                           |
| Specification  | 0 to +70                          | *         |             |             |             |             | °C                        |
| Operating  | -25 to +85                        | *         | -25 to +85  | -25 to +85  | -25 to +85  | -55 to +125 | °C                        |
| Storage  | -55 to +125                       | *         | -55 to +125 | -55 to +125 | -55 to +125 | -55 to +125 | °C                        |

## NOTES

\*Specifications same as AD DAC85C CBI.

<sup>1</sup> Adjustable to zero with external trim potentiometer.

<sup>2</sup> FSR means "full scale range" and is 20V for +10V range, 10V for +5V range, etc.

<sup>3</sup> To maintain drift spec internal feedback resistors must be used for current output models; the buried zener reference drift is a nonlinear function of temperature: all devices are tested to insure that actual drift at any temperature within the specified operating range is less than guaranteed maximum.

<sup>4</sup> With no degradation of specifications under constant load.

Prices and Specifications subject to change without notice.

**MIL-STD-883B**

The rigors of the military/aerospace environment (temperature extremes, humidity, mechanical stress, etc.), demand the utmost in electronic circuits. The AD DAC85 with the inherent reliability of integrated circuit construction, was designed with these applications in mind. To further insure reliability, the AD DAC85 is offered with 100% screening to MIL-STD-883B, method 5004.

Table I details the test procedures of MIL-STD-883B. All AD DAC85 models with an 883B suffix have been processed in accordance with these tests on a 100% basis: AD DAC85 MIL-CBI-V-883B is an example of 883B designation.

| TEST                         | METHOD  | PURPOSE   |
|------------------------------|---|---|
| 1) Internal Visual (Pre cap) | 2017  | Removes potentially defective parts with respect to bonding, metalization, etc.         |
| 2) Stabilization Bake        | Method 1008, Test Condition C, 24 hours @ +150°C                      | Stabilizes circuit elements, thin film resistors.                                       |
| 3) Temperature Cycling       | Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C             | Changes operating characteristics.  |
| 4) Constant Acceleration     | Method 2001, Test Condition B, Y1 plane, 10kg                         | Removes potential failures due to weak wire or chip bonding; insures package integrity. |
| 5) Seal, Fine and Gross      | Method 1014, Test Condition A or B and C, 5 x 10 <sup>-7</sup> cc/sec | Verifies hermetic sealing.  |
| 6) Burn-in Test              | Method 1015, Test Condition D, 168 hours @ +125°C                     | Removes potential electrical failures.  |
| 7) Final Electrical Tests    | Performed at +25°C, maximum and minimum operating temperatures        | Removes any failures from the above tests and verifies electrical specifications.       |
| 8) External Visual           | Method 2009   | Insures physical condition of package and branding.                                     |

**AD DAC85 ORDERING & PRICING GUIDE**

| MODEL             | INPUT CODE           | OUTPUT MODE | TEMPERATURE RANGE |
|-------------------|----------------------|-------------|-------------------|
| AD DAC85C-CBI-V   | Binary               | Voltage     | 0°C to +70°C      |
| AD DAC85C-CBI-I   | Binary               | Current     | 0°C to +70°C      |
| AD DAC85-CBI-V    | Binary               | Voltage     | -25°C to +85°C    |
| AD DAC85-CBI-I    | Binary               | Current     | -25°C to +85°C    |
| AD DAC85LD-CBI-V  | Binary               | Voltage     | -25°C to +85°C    |
| AD DAC85LD-CBI-I  | Binary               | Current     | -25°C to +85°C    |
| AD DAC85MIL-CBI-V | Binary               | Voltage     | -55°C to +125°C   |
| AD DAC85MIL-CBI-I | Binary               | Current     | -55°C to +125°C   |
| AD DAC85C-CCD-V   | Binary Coded Decimal | Voltage     | 0°C to +70°C      |
| AD DAC85C-CCD-I   | Binary Coded Decimal | Current     | 0°C to +70°C      |
| AD DAC85-CCD-V    | Binary Coded Decimal | Voltage     | -25°C to +85°C    |
| AD DAC85-CCD-I    | Binary Coded Decimal | Current     | -25°C to +85°C    |

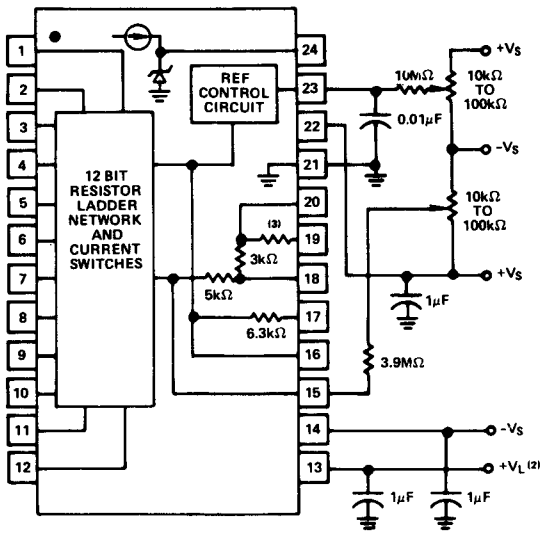


Figure 1. External Adjustment and Voltage Supply Connection Diagram, Current Model

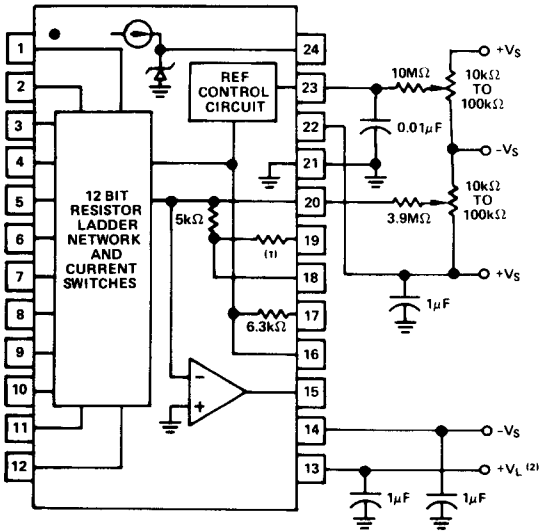


Figure 2. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

**NOTES:**

1. 3kΩ for CCD models. 5kΩ for CBI models.
2. If connected to +V<sub>S</sub> which is permissible, power dissipation increases 200mW.
3. CBI model, 2kΩ; CCD model, 0Ω and pin 20 has no internal connection.

**PIN CONFIGURATION**

**24 LEAD DUAL IN-LINE PACKAGE**

| I Models     | Pin # | V Models     |
|--------------|-------|--------------|
| (MSB) Bit 1  | 1     | Bit 1(MSB)   |
| Bit 2        | 2     | Bit 2        |
| Bit 3        | 3     | Bit 3        |
| Bit 4        | 4     | Bit 4        |
| Bit 5        | 5     | Bit 5        |
| Bit 6        | 6     | Bit 6        |
| Bit 7        | 7     | Bit 7        |
| Bit 8        | 8     | Bit 8        |
| Bit 9        | 9     | Bit 9        |
| Bit 10       | 10    | Bit 10       |
| Bit 11       | 11    | Bit 11       |
| (LSB) Bit 12 | 12    | Bit 12 (LSB) |

| I Models                | Pin # | V Models                |
|-------------------------|-------|-------------------------|
| Logic Supply            | 13    | Logic Supply            |
| -V <sub>S</sub>         | 14    | -V <sub>S</sub>         |
| V <sub>OUT</sub>        | 15    | V <sub>OUT</sub>        |
| Ref Input               | 16    | Ref Input               |
| Bipolar Offset          | 17    | Bipolar Offset          |
| Scaling Network         | 18    | 10V Range               |
| Scaling Network         | 19    | 20V Range               |
| Scaling Network         | 20    | Summing Junction        |
| Common                  | 21    | Common                  |
| +V <sub>S</sub>         | 22    | +V <sub>S</sub>         |
| Gain Adjust             | 23    | Gain Adjust             |
| 6.3V <sub>REF</sub> Out | 24    | 6.3V <sub>REF</sub> Out |

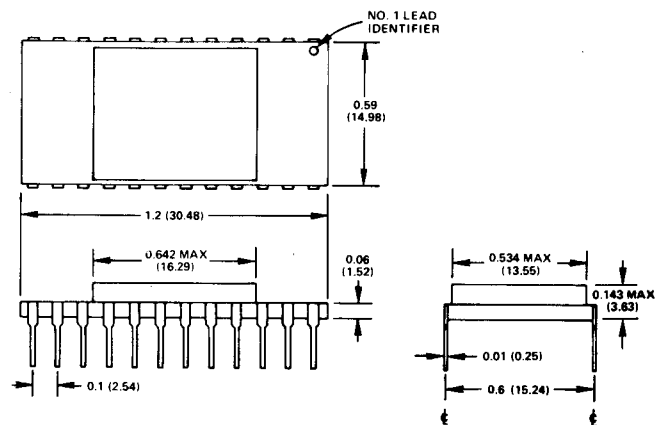


Figure 3. Outline Dimensions (Dimensions shown in inches and (mm))

## DIGITAL INPUT CODES

The AD DAC85 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB or CTC.

| DIGITAL INPUT |              | ANALOG OUTPUT |  |                          |                          |
|---------------|--------------|---------------|--|--------------------------|--------------------------|
| CBI Models    | MSB          | LSB           | CSB Compl. Straight Binary                 | COB Compl. Offset Binary | CTC* Compl. Two's Compl. |
|               | 000000000000 |               |  | +Full Scale              | +Full Scale              |
| 011111111111  |              |               | +½ Full Scale                              | Zero                     | -Full Scale              |
| 100000000000  |              |               | Mid-scale -1LSB                            | -1 LSB                   | +Full Scale              |
| 111111111111  |              |               | Zero                                       | -Full Scale              | Zero                     |
| CCD Models    | MSB          | LSB           | CCD Complementary Coded Decimal - 3 Digits |                          |                          |
|               | 0110         | 0110 0110     | +Full Scale                                |                          |                          |
|               | 1111         | 1111 1111     | Zero                                       |                          |                          |

\*Invert the MSB of the COB code with an external inverter to obtain CTC code.

Table 1. Digital Input Codes

## ACCURACY

Accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Of these three specifications, the linearity error specification is the most important since it can not be corrected for. The linearity error of the AD DAC85 is specified over its entire temperature range. This means that the analog output will not vary by more than  $\pm 1/2$ LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of  $\pm 1/2$ LSB means that the output voltage step sizes can range from  $1/2$ LSB to  $3/2$ LSB when the input changes from one adjacent input state to the next. Monotonicity over the  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  range is guaranteed in the AD DAC85 to insure that the analog output will not decrease with increasing input digital codes.

## DRIFT

**Gain Drift** is a measure of the change in the full scale range output over temperature expressed in parts per million per  $^{\circ}\text{C}$  (ppm/ $^{\circ}\text{C}$ ). Gain drift is established by: 1) testing the end point differences for each AD DAC85 model at the lowest operating temperature,  $+25^{\circ}\text{C}$  and the highest operating temperature; 2) calculating the gain error with respect to the  $+25^{\circ}\text{C}$  value and; 3) dividing by the temperature change.

**Offset Drift** is a measure of the actual change in output with all "1"s on the input over the specified temperature range. For example, the offset for the "C" version is measured at  $0^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$  and  $+70^{\circ}\text{C}$ . The maximum change in offset is referenced to the offset at  $25^{\circ}\text{C}$  and is divided by the temperature range. This drift is expressed in parts per million of full scale range per  $^{\circ}\text{C}$  (ppm of FSR/ $^{\circ}\text{C}$ ).

## SETTLING TIME

Settling time for each AD DAC85 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 4).

**Voltage Output Models.** Three settling times are specified to  $\pm 0.01\%$  of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0 1 1 1 ... 1 1 to 1 0 0 0 ... 0 0), the point at which the worst case settling time occurs.

**Current Output Models.** Two settling times are specified to  $\pm 0.01\%$  of FSR. Each is given for current models connected with two different resistive loads: 10 to 100 ohms and 1000 to 1875 ohms. Internal resistors are provided for connecting nominal load resistances of approximately 1000 to 1800 ohms for output voltage range of  $\pm 1\text{V}$  and 0 to  $-2\text{V}$  (see Table IV, Page 161S).

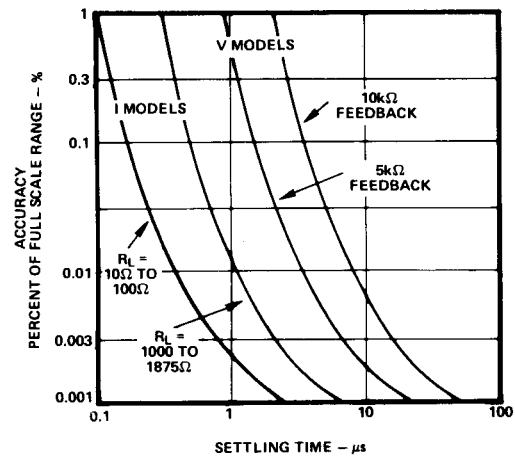


Figure 4. Full Scale Range Settling Time vs. Accuracy

## COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy.

## POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a per cent of FSR per per cent of change in either the positive, negative, or logic supplies about the nominal power supply voltages.

## REFERENCE SUPPLY

All AD DAC85 models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) is accurate to  $\pm 2\%$  and must be connected to the Reference Input (pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven off of the reference will result in gain variations of the AD DAC85. All gain adjustments should be made under constant load conditions.

# Using the AD DAC85

## POWER SUPPLY CONNECTIONS

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams (Figures 1 and 2). These capacitors (1 $\mu$ F electrolytic recommended) should be located close to the AD DAC85. Electrolytic capacitors, if used, should be paralleled with 0.01 $\mu$ F ceramic capacitors for optimum high frequency performance.

## EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. These potentiometers should be connected as shown in the block diagrams on Page 158S and adjusted as described below. TCR of the potentiometers should be 100ppm/ $^{\circ}$ C or less. The 3.9M $\Omega$  and 10M $\Omega$  resistors (20% carbon or better) should be located close to the AD DAC85 to prevent noise pick-up. If it is not convenient to use these high-value resistors, a functionally equivalent "T" network, as shown in Figure 7 may be substituted in each case. The gain adjust (pin 23) is a high impedance point and a 0.01 $\mu$ F ceramic capacitor should be connected from this pin

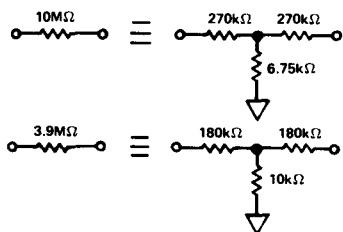


Figure 7. Equivalent Resistances

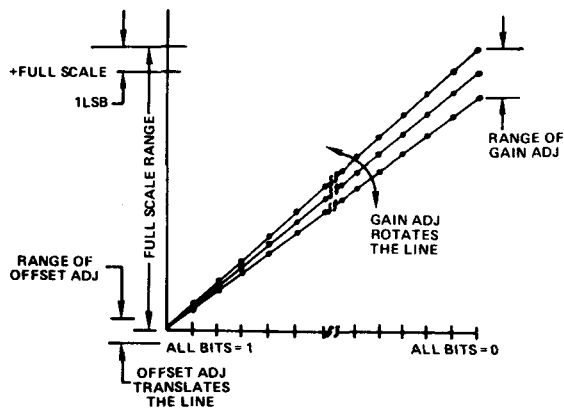


Figure 8. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter. (Input, Horizontal; Output, Vertical).

to common to prevent noise pick-up. Figures 8 and 9 show the relationship of the OFFSET and GAIN adjustments to the unipolar and bipolar D/A converters.

**Offset Adjustment.** For unipolar (CSB, CCD) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output. For bipolar (COD, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is -10V. See Table II for corresponding codes and the block diagrams on Page 158S for offset adjustment connections.

**Gain Adjustment.** For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the block diagrams for gain adjustment connections.

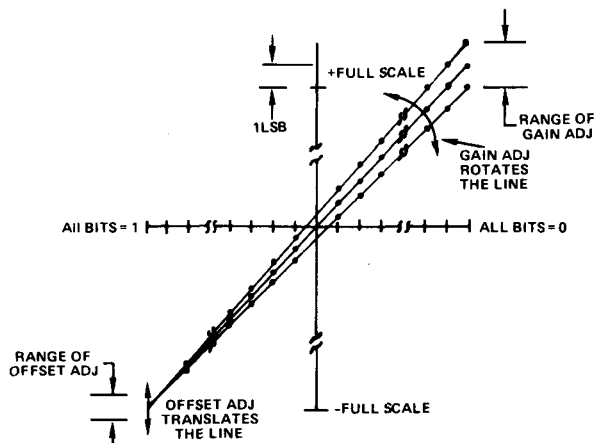


Figure 9. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A CONVERTER. (Input, Horizontal; Output, Vertical).

| DIGITAL INPUT        |     | ANALOG OUTPUT |           |              |           |               |
|----------------------|-----|---------------|-----------|--------------|-----------|---------------|
| 12 Bit Resolution    |     | VOLTAGE*      |           | CURRENT      |           |               |
| MSB                  | LSB | 0 to +10V     | $\pm 10V$ | 0 to -2mA    | $\pm 1mA$ |               |
| CBI Models           |     | 000000000000  | +9.9976V  | +9.9951V     | -1.9995mA | -0.9995mA     |
|                      |     | 011111111111  | -5.0000V  | 0.0000V      | -1.0000mA | 0.0000mA      |
|                      |     | 100000000000  | +4.9976V  | -0.0049V     | -0.9995mA | +0.0005mA     |
|                      |     | 111111111111  | 0.0000V   | -10.0000V    | 0.0000mA  | 0.488 $\mu$ V |
|                      |     | 1LSB          | 2.44mV    | 4.88mV       | 0.488mA   | +1.000mA      |
| 3 Digital Resolution |     |               |           |              |           |               |
| MSB                  |     |               |           |              |           |               |
| 0110 0110 0110       |     | +9.990V**     | N/A       | -1.249mA     | N/A       |               |
| 0110 0110 1111       |     | +9.900V       | N/A       | -1.238mA     | N/A       |               |
| 0110 1111 1111       |     | +9.000V       | N/A       | -1.125mA     | N/A       |               |
| 1111 1111 1111       |     | 0.000V        | N/A       | 0.000mA      | N/A       |               |
| 1LSB                 |     | 10.00mV       | N/A       | 1.25 $\mu$ A | N/A       |               |

\*To obtain values for other binary (CBI) ranges 0 to -5V range divide 0 to +10V range values by 2;  $\pm 5V$  range: divide  $\pm 10V$  range values by 2;  $\pm 2.5V$  range: divide  $\pm 10V$  range values by 4.  
\*\*Normal full scale range with correct codes; output can go higher if illegal codes are applied.

Table II. Digital Input/Analog Output

## VOLTAGE OUTPUT MODELS

Internal scaling resistors provided in the AD DAC85 may be connected to produce bipolar output voltage ranges of  $\pm 10$ ,  $\pm 5$  or  $\pm 2.5$ V or unipolar output voltage ranges of 0 to +5 or 0 to +10V (see Figure 10).

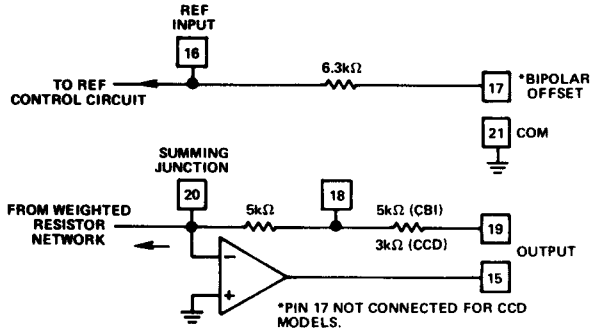


Figure 10. Output Amplifier Voltage Range Scaling Circuit

Gain and offset drift are minimized in the AD DAC85 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full scale range change: 5 microseconds for 8kΩ or 10kΩ feedback resistors; 3 microseconds for a 5kΩ feedback resistor.

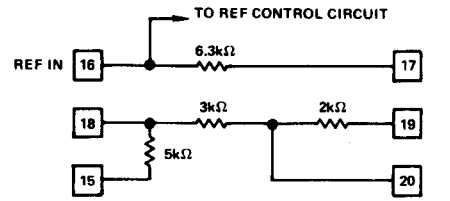
| Output Range | Digital Input Codes | Connect Pin 15 to | Connect Pin 17 to | Connect Pin 19 to | Connect Pin 16 to |
|--------------|---------------------|-------------------|-------------------|-------------------|-------------------|
| $\pm 10$ V   | COB or CTC          | 19                | 20                | 15                | 24                |
| $\pm 5$ V    | COB or CTC          | 18                | 20                | N.C.              | 24                |
| $\pm 2.5$ V  | COB or CTC          | 18                | 20                | 20                | 24                |
| 0 to +10V    | CSB                 | 18                | 21                | N.C.              | 24                |
| 0 to +5V     | CSB                 | 18                | 21                | 20                | 24                |
| 0 to +10V    | CCD                 | 19                | N.C.              | 15                | 24                |

Table III. Output Voltage Range Connections-Voltage Model AD DAC85

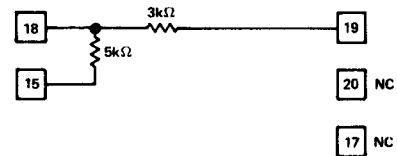
The equivalent resistive scaling network and output circuit of the current model are shown in Figures 11 and 12. External  $R_{LS}$  or  $R_{LP}$  resistors are required to produce exactly 0 to -2V or  $\pm 1$ V output. TCR of these resistors should be  $\pm 100$ ppm/ $^{\circ}$ C or less to maintain the AD DAC85 output specifications. If exact output ranges are not required, the external resistors are not needed.

| Digital Input Codes | Output Range | Internal Resistance $R_{LI}$ | 1% Metal Film External Resistance $R_{LS}$ $R_{LP}$ |        | $R_{LI}$ Connections |                   |                   | Reference         | Bipolar Offset    |                           |                     |
|---------------------|--------------|------------------------------|---|--------|----------------------|-------------------|-------------------|-------------------|-------------------|---------------------------|---------------------|
|                     |              |                              |   |        | Connect Pin 15 to    | Connect Pin 18 to | Connect Pin 20 to | Connect Pin 16 to | Connect Pin 17 to | $R_{LS}$                  | $R_{LP}$            |
| CSB                 | 0 to -2V     | 0.968kΩ                      | 210Ω  | N/A    | 20                   | 19 & $R_{LS}$     | 15                | 24                | Com (21)          | Between Pin 18 & Com (21) | N/A                 |
| CCD                 | 0 to -2V     | 3kΩ                          | N/A   | 3.57kΩ | N.C.                 | Com (21)          | N.C.              | 24                | N.C.              | N/A                       | Between Pin 15 & 21 |
| COB or CTC          | $\pm 1$ V    | 1.2kΩ                        | 249Ω  | N/A    | 18                   | 19                | $R_{LS}$          | 24                | 15                | Between Pin 20 & Com (21) | N/A                 |

Table IV. Current Model/Resistive Load Connections



a) AD DAC85-CBI-I



b) AD DAC85-CCD-I

Figure 11. Internal Scaling Resistors

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of  $\pm 1$ V or 0 to -2V. These resistors ( $R_{LI}$ ) are an integral part of the AD DAC85 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external  $R_L$  (or  $R_F$ ) resistors should have a TCR of  $\pm 25$ ppm/ $^{\circ}$ C or less to minimize drift. This will typically add  $\pm 50$ ppm/ $^{\circ}$ C + the TCR of  $R_L$  (or  $R_F$ ) to the total drift.

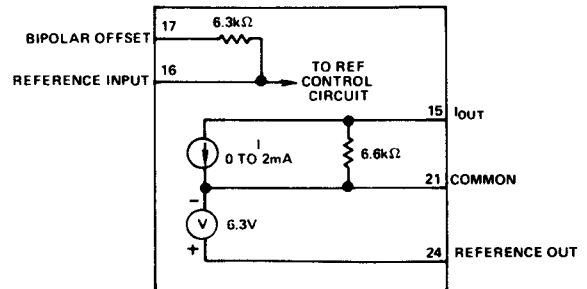


Figure 12. AD DAC85 Current Model Equivalent Output Circuit

### DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance,  $R_L = R_{LI} + R_{LS}$ , connected as shown in Figure 13 will generate a voltage range,  $V_{OUT}$ , determined by:

$$V_{OUT} = -2mA \left( \frac{6.6k \times R_L}{6.6k + R_L} \right)$$

Where  $R_L \text{ max} = 1.54k\Omega$

and  $V_{OUT \text{ max}} = -2.5V$

To achieve specified drift, connect the internal scaling resistor ( $R_{LI}$ ) as shown in Table IV to an external metal film trim resistor ( $R_{LS}$ ) to provide full scale output voltage range of 0 to -2V. With  $R_{LS} = 0$ ,  $V_{OUT} = -1.69V$ .

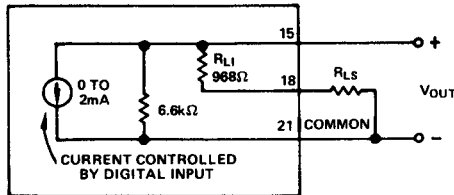


Figure 13. Equivalent Circuit AD DAC85-CBI-1 Connected for Unipolar Voltage Output with Resistive Load

CCD Input Code: Connect the internal scaling resistors as shown in Table V and add an external metal film resistor ( $R_{LP}$ ) in parallel as shown in Figure 14 to obtain a 0 to -2 volt full scale output voltage range for CCD input codes.

$$\text{With } R_L = \frac{R_{LI} \times R_{LP}}{R_{LI} + R_{LP}}$$

$$V_{OUT} = -1.25mA \left( \frac{6.9k \times R_L}{6.9k + R_L} \right)$$

If  $R_{LP} = \infty$ ,  $V_{OUT} = -3.62V$

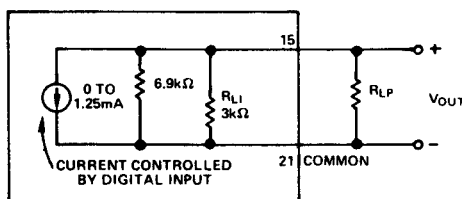


Figure 14. AD DAC85-CCD-1 Connected for Voltage Output with Resistive Load

### DRIVING A RESISTOR LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 15,  $R_L = R_{LI} + R_{LS}$ .  $V_{OUT}$  is determined by:

$$V_{OUT} = \pm 1mA \left( \frac{R_L \times 3.22k}{R_L + 3.22k} \right)$$

Where  $R_L \text{ max} = 11.18k\Omega$

$V_{OUT \text{ max}} = \pm 2.5V$

To achieve specified drift, connect the internal scaling resistors ( $R_{LI}$ ) as shown in Table IV for the COB or CTC codes and add an external metal film resistor ( $R_{LS}$ ) in series to obtain a full scale output range of  $\pm 1V$ . In this configuration, with  $R_{LS}$  equal to zero, the full scale range will be  $\pm 0.874V$ .

### DRIVING AN EXTERNAL OP AMP

The current model AD DAC85 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. As seen in Figure 16,

$$V_{OUT} = I_{OUT} \times R_F$$

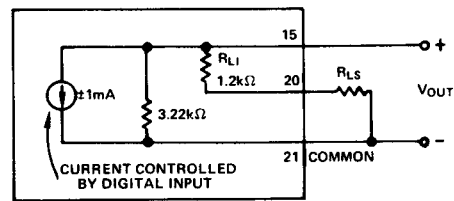
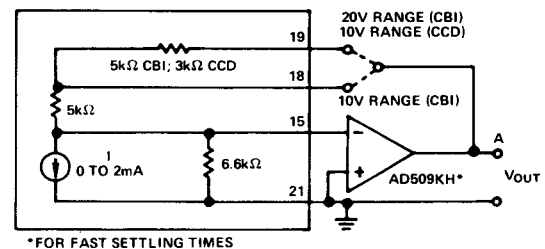


Figure 15. AD DAC85-CBI-1 Connected for Bipolar Output Voltage with Resistive Load

where  $I_{OUT}$  is the AD DAC85 output current and  $R_F$  is the feedback resistor. Using the internal feedback resistors of the current model AD DAC85 provides output voltage ranges the same as the voltage model AD DAC85. To obtain the desired output voltage range when connecting an external op amp, refer to Table V and Figure 16.

| Output Range | Digital Input Codes | Connect A to | Connect Pin 17 to | Connect Pin 19 to | Connect Pin 16 to |
|--------------|---------------------|--------------|-------------------|-------------------|-------------------|
| $\pm 10V$    | COB or CTC          | 19           | 15                | A                 | 24                |
| $\pm 5V$     | COB or CTC          | 18           | 15                | N.C.              | 24                |
| $\pm 2.5V$   | COB or CTC          | 18           | 15                | 15                | 24                |
| 0 to +10V    | CSB                 | 18           | 21                | N.C.              | 24                |
| 0 to +5V     | CSB                 | 18           | 21                | 15                | 24                |
| 0 to +10V    | CCD                 | 19           | N.C.              | A                 | 24                |

Table V. Voltage Range of Current Output AD DAC85



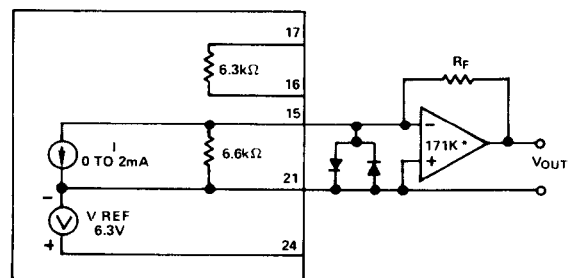
\*FOR FAST SETTLING TIMES

Figure 16. External Op Amp - Using Internal Feedback Resistors

### OUTPUT LARGER THAN 20V RANGE

For output voltage ranges larger than  $\pm 10$  volts, a high voltage op amp may be employed with an external feedback resistor. Use  $I_{OUT}$  values of  $\pm 1mA$  for bipolar voltage ranges and  $-2mA$  for unipolar voltage ranges (see Figure 17). Use protection diodes when a high voltage op amp is used.

The feedback resistor,  $R_F$ , should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between  $R_F$  and the internal scaling resistor network. This will typically add  $50ppm/^{\circ}C + R_F$  drift to total drift.



\*FOR OUTPUT VOLTAGE SWINGS UP TO 140V p-p.

Figure 17. External Op Amp - Using External Feedback Resistors

**PRELIMINARY TECHNICAL DATA****FEATURES**

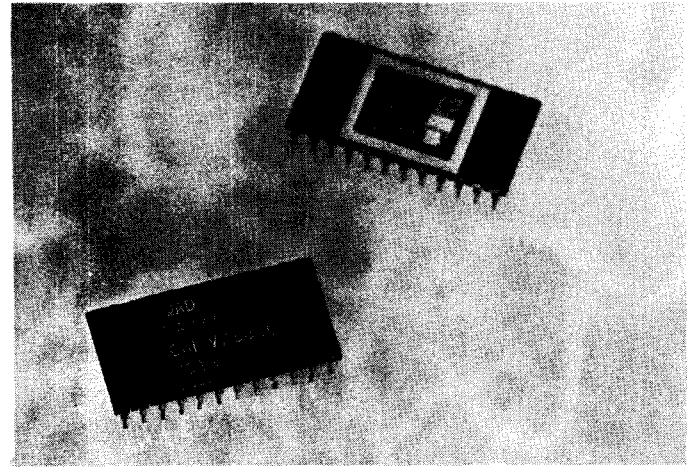
Pin-Compatible with AD DAC80 and AD DAC85  
3 Chip, High Reliability Construction  
Low Power Dissipation  
Laser-Trimmed to High Accuracy:  
 $\pm 3/4$ LSB Max Nonlinearity,  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
High Stability, High Current Output  
Buried Zener Reference  
On-Board Output Amplifier (V Models)  
24 Lead Side Brazed Ceramic DIP

**PRODUCT DESCRIPTION**

The AD DAC87 is a high performance 12-bit digital-to-analog converter, consisting of matched bipolar switches, a precision resistor network, a low-drift high-stability voltage reference and an optional output amplifier. The digital inputs are TTL compatible with complementary binary (CBI) input coding. The AD DAC87 offers output voltage ranges of  $\pm 2.5$ ,  $\pm 5$ ,  $\pm 10$ , 0 to +5, or 0 to +10 volts (V models); output current ranges (I models) are either  $\pm 1\text{mA}$  or 0 to  $-2\text{mA}$ .

Advanced circuit design and precision processing techniques result in significant performance advantages over conventional, larger, standard DAC87 devices. An innovative 3-chip construction improves reliability by a factor of five.<sup>1</sup> The AD DAC87 incorporates a fully differential, non-saturating precision current switching cell structure<sup>2</sup> which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability SiCr thin film resistors are trimmed with a fine resolution laser, resulting in low differential linearity errors. A low noise, high stability sub-surface zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature drift characteristics which challenge the best discrete zener references.

The AD DAC87 is recommended for all 12-bit D/A converter applications where reliability and performance over temperature are of paramount importance.

**PRODUCT HIGHLIGHTS**

1. The AD DAC87 directly replaces other devices of this type with significant increases in performance.
2. 3-Chip IC construction makes the AD DAC87 the optimum choice for applications where performance and reliability are major considerations.
3. System performance upgrading is possible without redesign.
4. The AD DAC87 offers a maximum nonlinearity of  $\pm 0.012\%$ ,  $\pm 25\text{ppm}/^{\circ}\text{C}$  maximum gain drift, and a total accuracy drift in the bipolar configuration of  $\pm 0.24\%$  of FSR maximum over the  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range.
5. The low T.C. Binary ladder guarantees that all AD DAC87 units will be monotonic over the specified temperature range.
6. Reduced power consumption requirements result in improved stability and shorter warm-up time.
7. The precision buried zener reference can supply up to  $2.5\text{mA}$  for use elsewhere in the application.
8. Voltage or current output models are available.
9. The solder-sealed ceramic package provides a reliable hermetic metal-to-metal seal.
10. All accuracy and drift parameters are 100% tested at  $-55^{\circ}\text{C}$  and  $+125^{\circ}\text{C}$  to insure high performance over the full temperature range.

<sup>1</sup> For details of calculations see Application Note, "AD DAC87 Reliability Predictions".

<sup>2</sup> COVERED BY PATENT NUMBERS: 3,978,473; RE 28,633; 4,020,486; 3,747,088; 3,803,590; 3,961,326.



# SPECIFICATIONS (T<sub>A</sub> = +25°C, rated power supplies unless otherwise noted)

| MODEL  | AD DAC87-CBI |                                  |              |                           |
|--|--------------|----------------------------------|--------------|---------------------------|
|  | MIN          | TYP                              | MAX          | UNITS                     |
| <b>DIGITAL INPUT</b>   |              |                                  |              |                           |
| Resolution   |              |                                  | 12           | Bits                      |
| Logic Levels (TTL Compatible)  |              |                                  |              |                           |
| Logic "1" (at +1μA)  | +2           |                                  | +5.5         | V                         |
| Logic "0" (at -100μA)  | 0            |                                  | +0.8         | V                         |
| <b>TRANSFER CHARACTERISTICS</b>  |              |                                  |              |                           |
| <b>ACCURACY</b>  |              |                                  |              |                           |
| Linearity Error @ +25°C  |              | ±1/4                             | ±1/2         | LSB                       |
| -55°C to +125°C  |              |                                  | ±3/4         | LSB                       |
| Differential Linearity Error at +25°C                                  |              | ±1/2                             | ±3/4         | LSB                       |
| -55°C to +125°C  |              |                                  | ±1           | LSB                       |
| Gain Error <sup>1</sup>  |              | ±0.1                             | ±0.2         | %                         |
| Offset Error <sup>1</sup>  |              | ±0.05                            | ±0.1         | %FSR <sup>2</sup>         |
| Temperature Range for Guaranteed Monotonicity                          | -55          |                                  | +125         | °C                        |
| <b>DRIFT<sup>3</sup> (-55°C to +125°C)</b>                             |              |                                  |              |                           |
| Total Bipolar Drift, max (includes gain, offset, and linearity drifts) |              | ±15                              | ±30          | ppm of FSR/°C             |
| Total Error (-55°C to +125°C) <sup>4</sup>                             |              |                                  |              |                           |
| Unipolar   |              | ±0.13                            | ±0.3         | % of FSR                  |
| Bipolar  |              | ±0.12                            | ±0.24        | % of FSR                  |
| Gain   |              |                                  |              |                           |
| Including Internal Reference   |              | ±10                              | ±25          | ppm/°C                    |
| Excluding Internal Reference   |              | ±5                               | ±10          | ppm/°C                    |
| Unipolar Offset  |              | ±1                               | ±3           | ppm of FSR/°C             |
| Bipolar Offset   |              | ±5                               | ±10          | ppm of FSR/°C             |
| <b>CONVERSION SPEED</b>  |              |                                  |              |                           |
| Voltage Model (AD DAC87-CBI-V)   |              |                                  |              |                           |
| Settling Time to ±0.01% of FSR for FSR change                          |              |                                  |              |                           |
| with 10kΩ Feedback   |              | 5                                |              | μs                        |
| with 5kΩ Feedback  |              | 3                                |              | μs                        |
| for 1LSB change  |              | 1.5                              |              | μs                        |
| Slew Rate  | 10           | 20                               |              | V/μs                      |
| Current Model (AD DAC87-CBI-V)   |              |                                  |              |                           |
| Settling Time to ±0.01% of FSR for FSR Change 10 to 100Ω Load          |              | 300                              |              | ns                        |
| 1kΩ Load   |              | 1                                |              | μs                        |
| <b>ANALOG OUTPUT</b>   |              |                                  |              |                           |
| Voltage Models   |              |                                  |              |                           |
| Ranges   |              | ±2.5, ±5, ±10, 0 to +5, 0 to +10 |              | V                         |
| Output Current   | ±5           |                                  |              | mA                        |
| Output Impedance (dc)  |              | 0.05                             |              | Ω                         |
| Short Circuit Duration   |              | INDEFINITE TO COMMON             |              |                           |
| Current Models   |              |                                  |              |                           |
| Ranges   |              | ±1, 0 to -2                      |              | mA                        |
| Output Impedance -- Bipolar  | 2.5          | 3.3                              | 4.1          | kΩ                        |
| -- Unipolar  | 5.0          | 6.6                              | 8.2          | kΩ                        |
| Compliance   | -1.5         |                                  | +10.5        | V                         |
| Internal Reference Voltage (V <sub>R</sub> )                           | +6.17        | +6.3                             | +6.43        | V                         |
| Output Impedance   |              | 1.5                              |              | Ω                         |
| Max. External Current <sup>5</sup>                                     |              |                                  | 2.5          | mA                        |
| Tempco of Drift  |              | ±5                               | ±10          | ppm of V <sub>R</sub> /°C |
| <b>POWER SUPPLY SENSITIVITY</b>  |              |                                  |              |                           |
| +15V Supply  |              | ±0.002                           | ±0.003       | % of FSR/%V <sub>S</sub>  |
| -15V and +5V Supplies  |              | ±0.002                           | ±0.003       | % of FSR/%V <sub>S</sub>  |
| <b>POWER SUPPLY REQUIREMENTS</b>                                       |              |                                  |              |                           |
| Rated Voltages   |              | ±15, +5                          |              | V                         |
| Range  | ±13.5, +4.5  |                                  | ±16.5, +16.5 | V                         |
| Supply Drain   |              |                                  |              |                           |
| +15V (Including 5mA Load)  |              | 10                               | 20           | mA                        |
| +5V  |              | 10                               | 20           | mA                        |
| -15V   |              | 20                               | 30           | mA                        |
| <b>TEMPERATURE RANGE</b>   |              |                                  |              |                           |
| Specification  | -55          |                                  | +125         | °C                        |
| Storage  | -65          |                                  | +150         | °C                        |

## NOTES:

<sup>1</sup> Adjustable to zero with external trim potentiometer.

<sup>2</sup> FSR means "full scale range" and is 20V for 10V range, 10V for 5V range, etc.

<sup>3</sup> To maintain drift spec internal feedback resistors must be used for current output models; the buried zener reference drift is a nonlinear function of temperature; all devices are tested to insure that actual drift at any temperature within the specified operating range is less than guaranteed maximum.

<sup>4</sup> With gain and offset errors adjusted to zero at +25°C.

<sup>5</sup> With no degradation of specifications under constant load.

Prices and specifications subject to change without notice.

## MIL-STD-883

The rigors of the military/aerospace environment (temperature extremes, humidity, mechanical stress, etc.), demand the utmost in electronic circuits. The AD DAC87, with the inherent

reliability of integrated circuit construction, was designed with these applications in mind. To further insure reliability, the AD DAC87 is available with 100% screening to MIL-STD-883, method 5008. Consult factory for pricing.

| TEST                         | METHOD  | PURPOSE   |
|------------------------------|---|---|
| 1) Internal Visual (Pre cap) | 2017  | Removes potentially defective parts with respect to bonding, metalization, etc.         |
| 2) Stabilization Bake        | Method 1008, Test Condition C, 24 hours @ +150°C                    | Stabilizes circuit elements, thin film resistors.                                       |
| 3) Temperature Cycling       | Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C           | Potential mechanical and electrical failures caused by thermal removes stresses.        |
| 4) Constant Acceleration     | Method 2001, Test Condition B, Y1 plane, 10,000g                    | Removes potential failures due to weak wire or chip bonding; insures package integrity. |
| 5) Seal, Fine and Gross      | Method 1014, Test Condition A or B and C, $5 \times 10^{-7}$ cc/sec | Verifies hermetic sealing.  |
| 6) Burn-in Test              | Method 1015, Test Condition D, 168 hours @ +125°C                   | Removes potential electrical failures   |
| 7) Final Electrical Tests    | Performed at +25°C, maximum and minimum operating temperatures      | Removes any failures from the above tests and verifies electrical specifications.       |
| 8) External Visual           | Method 2009   | Insures physical condition of package and branding.                                     |

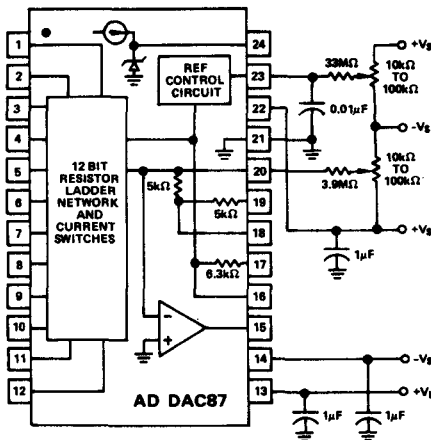


Figure 1. External Adjustment and Voltage Supply Connection Diagram, Current Model

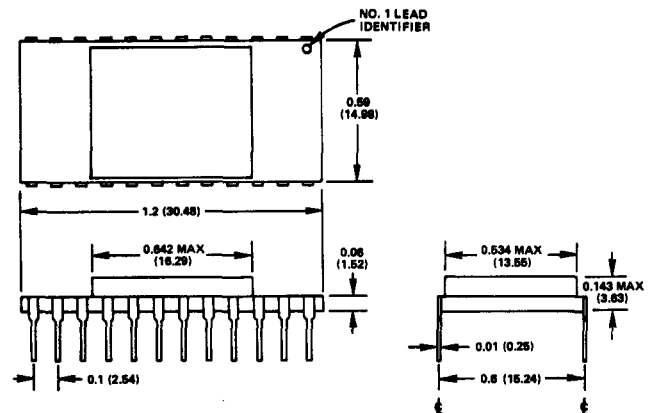


Figure 3. Outline Dimensions (Dimensions shown in inches and (mm))

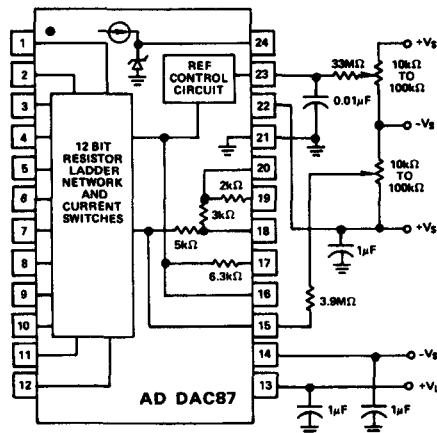


Figure 2. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

### PIN CONFIGURATION 24 LEAD DUAL IN-LINE PACKAGE

| I Models        | Pin # | V Models         |
|-----------------|-------|------------------|
| (MSB) Bit 1     | 1     | Bit 1 (MSB)      |
| Bit 2           | 2     | Bit 2            |
| Bit 3           | 3     | Bit 3            |
| Bit 4           | 4     | Bit 4            |
| Bit 5           | 5     | Bit 5            |
| Bit 6           | 6     | Bit 6            |
| Bit 7           | 7     | Bit 7            |
| Bit 8           | 8     | Bit 8            |
| Bit 9           | 9     | Bit 9            |
| Bit 10          | 10    | Bit 10           |
| Bit 11          | 11    | Bit 11           |
| (LSB) Bit 12    | 12    | Bit 12 (LSB)     |
| Logic Supply    | 13    | Logic Supply     |
| -Vs             | 14    | -Vs              |
| IOU             | 15    | VOU              |
| Ref Input       | 16    | Ref Input        |
| Bipolar Offset  | 17    | Bipolar Offset   |
| Scaling Network | 18    | 10V Range        |
| Scaling Network | 19    | 20V Range        |
| Scaling Network | 20    | Summing Junction |
| Common          | 21    | Common           |
| +Vs             | 22    | +Vs              |
| Gain Adjust     | 23    | Gain Adjust      |
| 6.3VREF Out     | 24    | 6.3VREF Out      |



## DAC1136/1137/1138

### FEATURES

**DAC1138**  
 18-Bit Resolution and Accuracy ( $38\mu\text{V}$ , 1 Part in 262,144)  
 Integral Nonlinearity 1/2LSB  
 Differential Nonlinearity 1/2LSB  
 Settling to 1/2LSB (0.0002%) in  $10\mu\text{s}$   
 Hermetically-Sealed Semiconductors

**DAC1137**  
 18-Bit Resolution, 16-Bit Accuracy  
 Lowest Cost 18-Bit DAC  
 Settling to 1/2LSB (0.0002%) in  $10\mu\text{s}$

**DAC1136**  
 16-Bit Resolution and Accuracy  
 Low Cost  
 Nonlinearity 1/2LSB  
 Settling to 1/2LSB (0.0008%) in  $6\mu\text{s}$

**DEGLITCHER IV**  
 Virtually Eliminates DAC Glitches  
 Available on DAC1136/1137/1138 Card-Mounted Assembly

### GENERAL DESCRIPTION

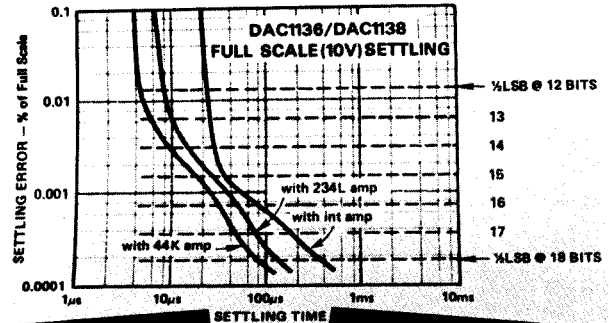
The DAC1136/1137/1138 are complete self-contained voltage or current output modular digital to analog converters with resolutions and accuracies of 16 and 18 bits. These modules are constructed in a compact  $2'' \times 4'' \times 0.4''$  package and share the same pin-out as the popular DAC-14QM and DAC-16QM.

The DAC1136/1137/1138 combine precision current sources with state-of-the-art steering switches to produce a very linear output. Inputs to these converters are compatible with TTL levels. The converters have a current output of 2mA full scale. A voltage output can be obtained by connecting the internal amplifier to the current output by means of jumpers. By using additional jumpers, the user can select any one of the following output ranges: 0 to +5V, 0 to +10V,  $\pm 5\text{V}$ , or  $\pm 10\text{V}$ .

The DAC1136/1137/1138 are available as card-mounted assemblies. In this configuration, selectable options include: input codes, output amplifiers, and a high speed transient-suppressing Deglitcher Module, Deglitcher IV.

### WHERE TO USE HIGH RESOLUTION DAC'S

The DAC1136/1137/1138 deliver exceptional accuracies for a broad range of display, test, and instrumentation applications. The DAC1136, with a resolution of 16 bits or 1 part in 65536, and the DAC1137/1138 with a resolution of 18 bits or 1 part in 262,144 are ideally suited for applications requiring wide dynamic range measurement and control. Applications include data distribution systems, high resolution CRT displays, automatic semiconductor testing, photo-type-setting, frequency synthesis and nuclear reactor control.



### CERTIFICATE OF CALIBRATION

Each DAC1138 has been calibrated with equipment and methods that are traceable to the National Bureau of Standards (NBS). A Certificate of Performance is sent with each unit, which includes 1000 hour stability data for the reference zener and linearity test data.

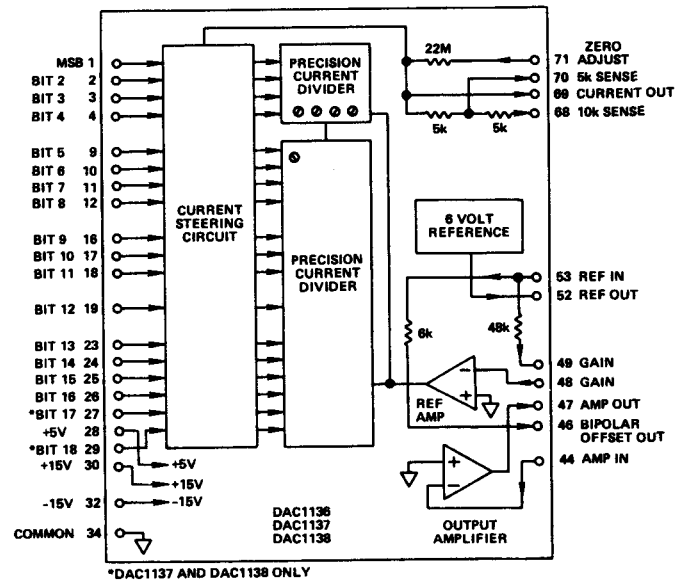


Figure 1. Block Diagram and Pin Designations

# SPECIFICATIONS (typical @ +25°C, and rated supply voltage, unless otherwise noted)

| Model   | DAC1136   |                         |                             | DAC1136 CARD-MOUNTED ASSY  |                     |
|---|---|-------------------------|-----------------------------|--|---------------------|
|   | J   | K                       | L                           | W/Internal Amp   | W/44K W/234L        |
| RESOLUTION<br>Magnitude of 1LSB (10V range)   | 16 Bits<br>152μV  |                         |                             | Specifications are the same as module unless otherwise noted       |                     |
| DIGITAL INPUTS<br>Input Codes<br>Unipolar<br>Bipolar<br>Strobe  | TTL/See Figure 2<br><br>Complementary Binary<br>Complementary Offset Binary<br>N.A.                   |                         |                             | See Ordering Guide<br>See Ordering Guide<br>See Note 1             |                     |
| ACCURACY<br>Integral and Differential Nonlinearity (max)<br>Zero Offset<br>Gain<br>Reference Voltage <sup>2</sup>   | 1LSB  | 0.5LSB                  | 0.5LSB                      | Adjustable to Zero<br>Adjustable to Full Scale<br>6.00V ± 0.4% max |                     |
| TEMPERATURE COEFFICIENTS (ppm/°C)<br>Integral Nonlinearity<br>Differential Nonlinearity<br>Offset<br>Unipolar<br>Bipolar<br>Gain <sup>3</sup><br>Reference Voltage  | 1<br>1  | 1<br>1<br>0.5<br>5<br>6 | 1.5 max<br>1.5 max<br>8 max | 2  | 0.5                 |
| STABILITY LONG TERM (ppm/10 <sup>3</sup> hr)<br>Offset<br>Gain <sup>3</sup><br>Reference Voltage  | 6<br>12<br>7  |                         |                             | 30   | 6                   |
| POWER SUPPLY REJ<br>Voltage<br>Offset <sup>4</sup><br>Gain  | 75dB<br>80dB  |                         |                             | 80dB   | 100dB               |
| DYNAMIC CHARACTERISTICS<br>Settling Time to ±1/2LSB<br>Voltage<br>Full Scale Step<br>Unipolar<br>Bipolar<br>LSB Step<br>Current<br>Full Scale Step<br>LSB Step<br>Noise (rms 10Hz - 100kHz)<br>Voltage<br>Current | 30μs<br>40μs<br>6μs<br>8μs<br>6μs<br>30μV<br>1nA  |                         |                             | 15μs<br>25μs<br>5μs  | 25μs<br>35μs<br>7μs |
| ANALOG OUTPUTS<br>Voltage<br>Output Range<br>Rated Output Current<br>Output Impedance<br>Current<br>Output Range<br>Unipolar<br>Bipolar   | 0 to +5V, 0 to +10V, ±5V, ±10V<br>4mA<br>See Characteristic Curves<br><br>-2mA to 0mA<br>-1mA to +1mA |                         |                             | See Ordering Guide<br>±20mA ±5mA<br>See Characteristic Curves      |                     |
| VOLTAGE COMPLIANCE<br>Rated Accuracy<br>Clamp Limits <sup>5</sup><br>Source Resistance<br>Unipolar<br>Bipolar<br>Source Capacitance   | ±2mV<br>±500mV<br><br>>33kΩ<br>>5kΩ<br>150pF  |                         |                             | VOLTAGE OUTPUT ONLY  |                     |
| POWER SUPPLY REQUIREMENTS <sup>6</sup><br>+5V dc ±5%<br>±15V dc ±5%   | 9mA<br>30mA   |                         |                             | See Note 7<br>40mA 37mA  |                     |
| TEMPERATURE RANGE<br>Operating Temperature <sup>8</sup><br>Storage Temperature  | 0 to +70°C<br>-55°C to +85°C  |                         |                             |  |                     |

## NOTES:

<sup>1</sup> Positive going transition (Logic "0" to Logic "1") will clock data into series 74LS, input, latching registers.

<sup>2</sup> The reference output is high impedance ( $Z_{OUT} \approx 200\Omega$ )

<sup>3</sup> Exclusive of reference.

<sup>4</sup> Unipolar and bipolar.

<sup>5</sup> Clamp limits are set by Schottky diodes.

<sup>6</sup> Recommended power supply: Analog Devices model 923.

<sup>7</sup> 95mA using mounting card with input latching registers, see ordering guide.

<sup>8</sup> 5% to 95% relative humidity noncondensing.

Specifications subject to change without notice.

| Model  | DAC1137  |  | DAC1138 |   | DAC1137/1138 Card-Mounted Assy<br>W/Internal Amp W/234L  |
|--|--|--|---------|---|--|
|  | J  | K  |         |   |  |
| <b>RESOLUTION</b><br>Magnitude of 1LSB (10V range)   | 18 Bits<br>38 $\mu$ V  |  |         |   | Specifications are the same as module unless otherwise noted   |
| <b>DIGITAL INPUTS</b><br>Input Codes<br>Unipolar<br>Bipolar<br>Strobe  | TTL/See Figure 2<br><br>Complementary Binary<br>Complementary Offset Binary<br>N.A.  |  |         |   | See Ordering Guide<br>See Ordering Guide<br>See Note 1   |
| <b>ACCURACY</b><br>Integral and Differential Nonlinearity (max)<br>Zero Offset Error<br>Gain Error<br>Reference Voltage <sup>3</sup> (max)   | $\pm 0.5\text{LSB}^2$ $\pm 1\text{LSB}$ $\pm 0.5\text{LSB}$<br>Adjustable to Zero<br>Adjustable to Full Scale<br>6.0V $\pm 0.25\%$ 6.0V $\pm 0.13\%$ * |  |         |   |  |
| <b>TEMPERATURE COEFFICIENTS (ppm/<math>^{\circ}</math>C)<sup>4</sup></b><br>Integral Nonlinearity<br>Differential Nonlinearity<br>Offset<br>Unipolar<br>Bipolar<br>Gain <sup>5</sup><br>Reference Voltage                            | $\pm 0.5$ max<br>$\pm 0.5$ max<br>$\pm 0.5$<br>$\pm 3$<br>$\pm 5$ max<br>$\pm 3$   | $\pm 0.3$<br>$\pm 0.4$<br>$\pm 0.5$<br>$\pm 1$<br>$\pm 0.8$<br>$\pm 2$ | *       | * |  |
| <b>STABILITY LONG TERM (ppm/<math>10^3</math> hr)</b><br>Offset<br>Gain <sup>5</sup><br>Reference Voltage  | $\pm 3$<br>$\pm 5$<br>$\pm 7$  | $\pm 2$<br>$\pm 2$<br>$\pm 10$ max                                     | *       | * | 6  |
| <b>POWER SUPPLY REJ</b><br>Voltage<br>Offset <sup>6</sup><br>Gain  | 75dB<br>80dB   |  |         |   | 100dB  |
| <b>DYNAMIC CHARACTERISTICS</b><br>Settling Time to $\pm 1/2\text{LSB}$<br>Voltage<br>Full Scale Step<br>Unipolar<br>Bipolar<br>LSB Step<br>Current<br>Full Scale Step<br>LSB Step<br>Noise (rms 10Hz - 100kHz)<br>Voltage<br>Current | 250 $\mu$ s<br>3ms<br>18 $\mu$ s<br>10 $\mu$ s<br>8 $\mu$ s<br>30 $\mu$ V<br>1nA   |  |         |   | 130 $\mu$ s<br>200 $\mu$ s<br>20 $\mu$ s<br><br>VOLTAGE OUTPUT ONLY<br><br>40 $\mu$ V<br>VOLTAGE OUTPUT ONLY |
| <b>ANALOG OUTPUTS</b><br>Voltage<br>Output Range<br>Rated Output Current<br>Output Impedance<br>Current<br>Output Range<br>Unipolar<br>Bipolar   | 0 to +5V, 0 to +10V, $\pm 5\text{V}$ , $\pm 10\text{V}$<br>4mA max<br>See Characteristic Curves<br><br>-2mA to 0mA<br>-1mA to +1mA                     |  |         |   | See Ordering Guide<br><br>$\pm 5\text{mA}$   |
| <b>VOLTAGE COMPLIANCE</b><br>Rated Accuracy<br>Clamp Limits <sup>7</sup><br>Source Resistance<br>Unipolar<br>Bipolar<br>Source Capacitance   | $\pm 200\mu\text{V}$<br>$\pm 500\text{mV}$<br>$> 33\text{k}\Omega$<br>$> 5\text{k}\Omega$<br>150pF   |  |         |   | VOLTAGE OUTPUT ONLY  |
| <b>POWER SUPPLY REQUIREMENTS<sup>8,9</sup></b><br>+5V dc $\pm 5\%$<br>$\pm 15\text{V}$ dc $\pm 5\%$  | 9mA<br>30mA  |  |         |   | See Note 10<br>37mA  |
| <b>TEMPERATURE RANGE</b><br>Operating Temperature <sup>11</sup><br>Storage Temperature   | 0 to +70 $^{\circ}$ C<br>-55 $^{\circ}$ C to +85 $^{\circ}$ C  |  |         |   |  |

**NOTES:**

<sup>1</sup> Positive going transition (Logic "0" to Logic "1") will clock data into logic series 74LS network.

<sup>2</sup> DAC1137 has 18-bit resolution and 16-bit accuracy, therefore LSB values are referred to 16 bits.

<sup>3</sup> The reference output is high impedance, maximum load 1 $\mu$ A,  $Z_{\text{out}} \approx 200\Omega$ .

<sup>4</sup> See characteristic curves for performance over temperature.

<sup>5</sup> Exclusive of reference.

<sup>6</sup> Unipolar and bipolar

<sup>7</sup> Clamp limits are set by Schottky diodes.

<sup>8</sup> Recommended power supply: Analog Devices model 923.

<sup>9</sup> Change in differential linearity from factory setting due to power supply voltage variation from nominal is  $\approx 3.5\text{ppm}/V\Delta V_S$ .

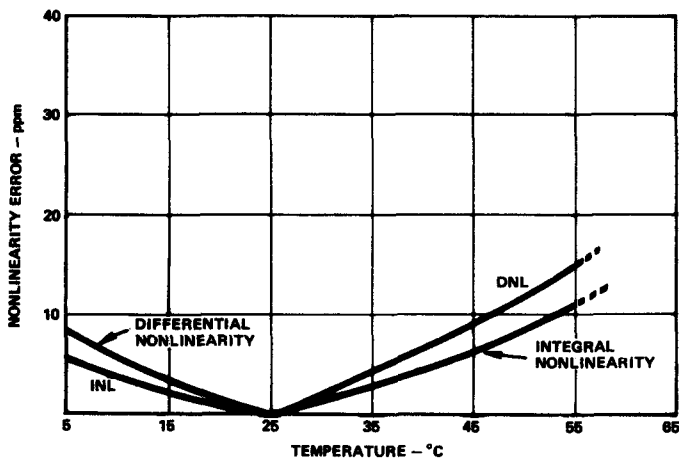
<sup>10</sup> 95mA using mounting card with input latching registers, see ordering guide.

<sup>11</sup> 5% to 95% relative humidity noncondensing.

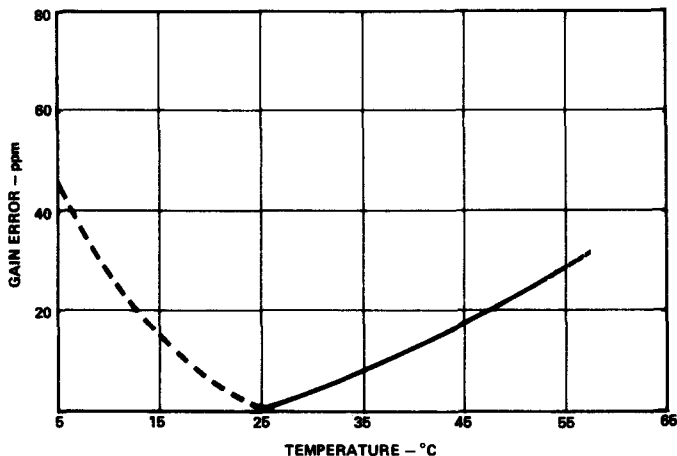
\* Specifications same as DAC1138J.

Specifications subject to change without notice.

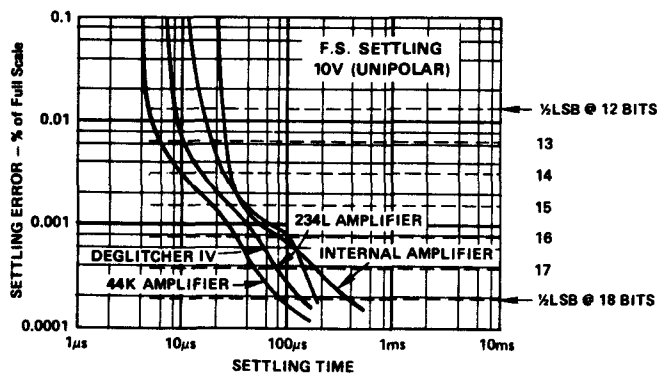
# Characteristic Curves\*



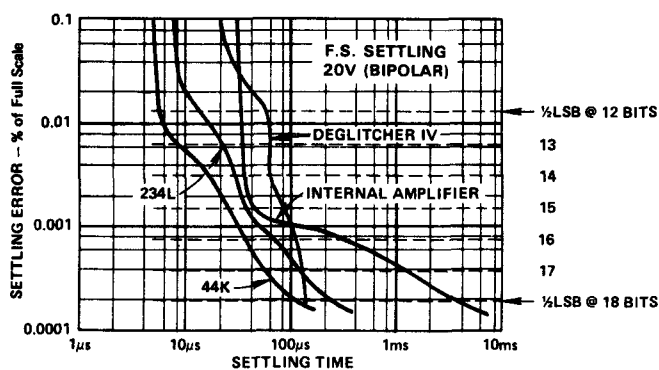
DAC1138 Nonlinearity vs. Temperature



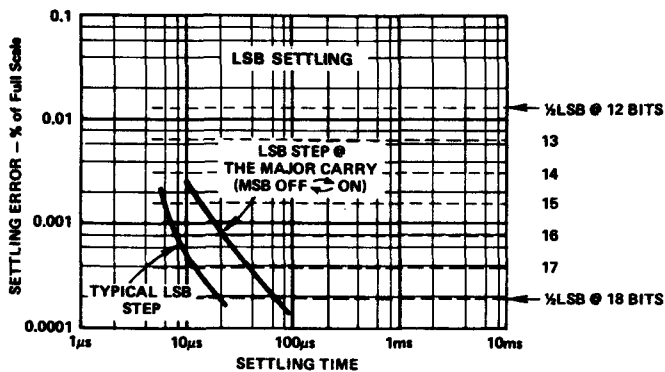
DAC1138 Gain Error vs. Temperature



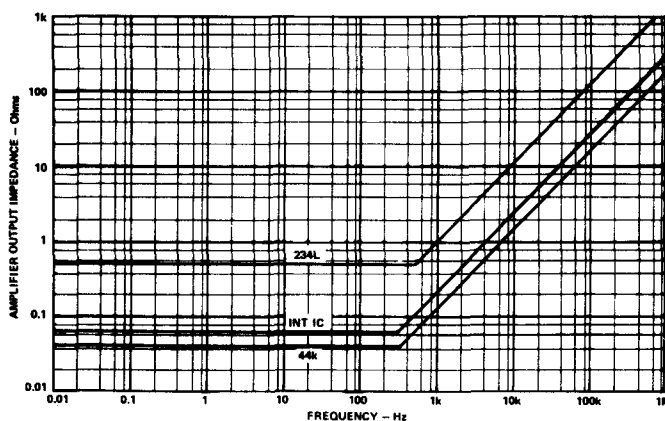
Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for 10V Output Step (0V ↔ +10V)



Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for 20V Output Step (+10V ↔ -10V)



Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for LSB Steps (Essentially Independent of Amplifier Used)

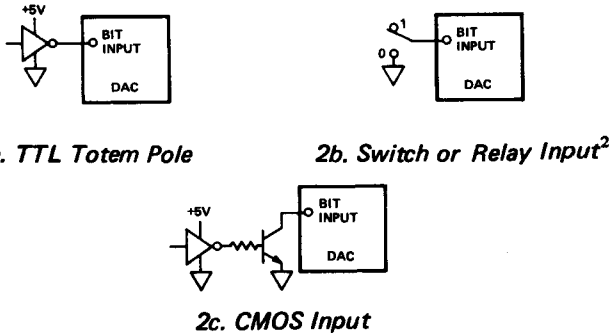


Amplifier Output Impedance vs. Frequency

\*NOTE: All curves typical at rated supply voltage.  
F.S. = Full Scale

## INPUT CONSIDERATIONS

The DAC1136/1137/1138 may be driven by TTL or CMOS as shown in Figure 2. Note that the TTL input is shown with inputs for both a direct "totem pole" TTL gate and open collector (or "pull-up") configurations.



1. FOR TTL WITH OPEN COLLECTOR, DO NOT USE EXTERNAL PULL-UP. CONVERTERS HAVE INTERNAL 10kΩ PULL-UP ON EACH INPUT TO 3.8V.
2. USE SPST SWITCH OR REPLY TO GROUND. WHEN SWITCH IS OPEN, INTERNAL 10kΩ WILL PULL INPUT UP TO 3.8V.

Figure 2. Input Connections

## OUTPUT CONNECTIONS AND GUARDING

The DAC1136/1137/1138 output connections for various voltage ranges are shown in Figure 3.

Since an LSB is only 38μV (at 10 volts full scale for the DAC1138), care must be exercised to properly guard the current output of the converter from leakage current. Any connection made to the DAC's current output (pin 69) should be guarded. Suggested printed circuit board guarding is shown in Figure 3. The optional card-mounted assemblies of the DAC1136/1137/1138 have been carefully designed for optimum guarding and performance.

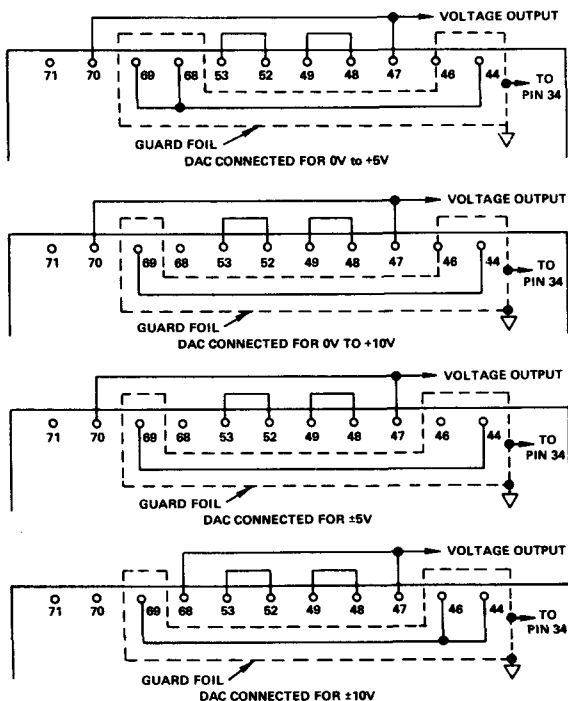
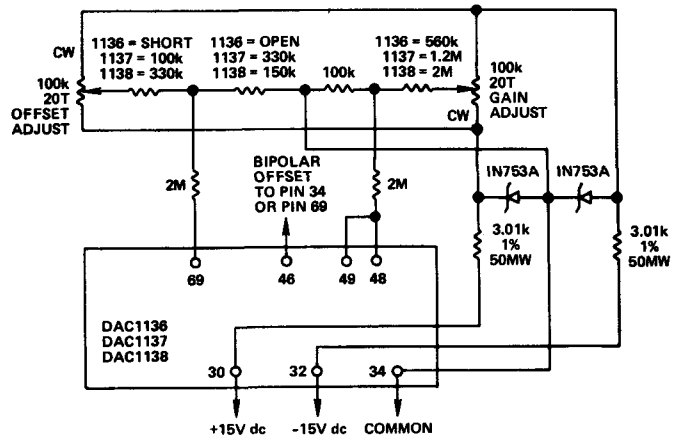


Figure 3. Output Voltage Connections and Suggested PCB Guarding (Unipolar and Bipolar)

## GAIN AND OFFSET ADJUSTMENTS

The gain and offset adjustments are made with external potentiometers which the user supplies. With the appropriate digital inputs applied, these potentiometers are adjusted until the desired output voltage is obtained. The proper connections for offset and gain are shown in Figure 4. The voltmeter used to measure the output should be capable of stable resolution of 1/4LSB in the region of zero and full scale. Because of the interaction between offset and gain adjustments, the adjustment procedure described below should be carefully followed. Offset adjustment affects gain, but gain adjustment does not affect offset.



- NOTES:
1. ALL FIXED RESISTORS ARE 5% CARBON COMP. UNLESS OTHERWISE NOTED.
  2. ALL POTENTIOMETERS ARE 20-TURN INFINITE RESOLUTION TYPE.

Figure 4. Gain and Offset Adjustments

For unipolar mode, apply a digital input of all "1's" (complementary binary code for zero output) and adjust the offset potentiometer until a 0.00000V output is obtained (see Table 1). Once the appropriate offset adjustment has been made, apply a digital input of all "0's". Adjust the gain potentiometer until the plus full scale output is obtained (see Table 1).

For bipolar mode, apply a digital input of all "1's" (complementary offset binary code for minus full scale) and adjust the offset potentiometer for the proper minus full scale output voltage (see Table 1). Once the appropriate minus full scale adjustment has been made, apply a digital input of all "0's". Adjust the gain potentiometer until the plus full scale output shown below is obtained.

| RANGE       | IDEAL OUTPUT     |                       |
|-------------|------------------|-----------------------|
|             | DAC1137/<br>1138 | DAC1136               |
| Unipolar:   | All 11...1       |                       |
| 0V → +10V   | 0.00000V         | +9.999962V +9.999848V |
| 0V → +5V    | 0.00000V         | +4.999981V +4.999924V |
| Bipolar:    | All 00...0       |                       |
| -10V → +10V | -10.00000V       | +9.999934V +9.999695V |
| -5V → +5V   | -5.00000V        | +4.999962V +9.999848V |
| To adjust:  | Adjust ZERO pot  | Adjust GAIN pot       |

Table 1. Full Scale Output



## DIFFERENTIAL LINEARITY ADJUSTMENT

Each DAC1136/1137/1138 has been factory calibrated and tested to achieve the performance indicated in the electrical specifications. Should it be necessary to readjust the linearity of these units, the user can do so. Before attempting this recalibration, it is imperative that the circuit be checked to confirm that all previously described precautions have been taken to insure proper application at the 16- or 18-bit level. Basically, the DAC is trimmed by comparing a bit to the sum of all lower bits, and adjusting, if necessary, for a one LSB positive difference. The top 4 major carries, i.e., MSB minus the sum of bits 2-through-the-LSB, down through bit 4 minus the sum of bits 5-through-the-LSB, can be trimmed using the procedure outlined below. The setup for this adjustment is shown in Figure 5. In this procedure, an LSB is referred to as  $38\mu\text{V}$ , implying that the DAC1137/1138 is being used on the 10V range. For the DAC1136 an LSB is  $152\mu\text{V}$  on the 10V range.

### 1. Bit 4 Trim

- Set bit inputs to 11110 . . . . 0.
- Read the output voltage by nulling the voltmeter.
- Set bit inputs to 11101 . . . . 1.
- Read voltage by nulling voltmeter. This reading should be equal to that of step 1b plus 1LSB. Adjust bit 4 if required (see B4, Figure 7).

### 2. Bit 3 Trim

- Set bit inputs to 1110 . . . . 0.
- Read output voltage by nulling the voltmeter.
- Set inputs to 1101 . . . . 1.
- Read voltage by nulling the voltmeter. This reading should be equal to that of step 2b plus 1LSB. Adjust bit 3 if required (see B3, Figure 7).

### 3. Bit 2 Trim

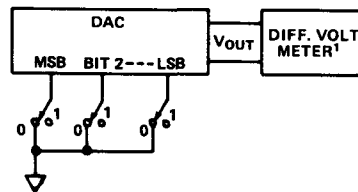
- Set bit inputs to 110 . . . . 0.
- Read output voltage by nulling the voltmeter.
- Set bit inputs to 101 . . . . 1.
- Read voltage by nulling voltmeter. This reading should be equal to that of step 3b plus 1LSB. Adjust bit 2 if required (see B2, Figure 7).

### 4. Bit 1 (MSB) Trim

- Set bit switches to 100 . . . . 0.
- Read output voltage by nulling the voltmeter.
- Set bit switches to 011 . . . . 1.
- Read voltage by nulling voltmeter. This reading should be equal to that of step 4b plus 1LSB. Adjust bit 1 (MSB) if required (see MSB, Figure 7).

If insufficient range exists on any adjustment, then a separate adjustment for the weight of bits 5-through-the-LSB (see

Sum B5 LSB, Figure 7) should be performed. This condition will probably not occur on bit 2, 3 and 4 but might occur on the MSB. If adjustment of the sum of bits 5-through-the-LSB is made, the trim procedure for all bits should be repeated. Obviously, since the procedure affects the weight of individual bits, it affects the overall gain of the DAC. The final step should be adjustment of gain (user supplied adjustment external to module or pot at edge of mounting card).



- A DIFFERENTIAL VOLTMETER CAPABLE OF  $100\mu\text{V}$  FULL SCALE SHOULD BE USED. THIS WILL RESOLVE AN LSB, WHICH AT 18 BITS IS  $38\mu\text{V}$  (10V RANGE). A FLUKE 895A, OR EQUIVALENT IS RECOMMENDED.

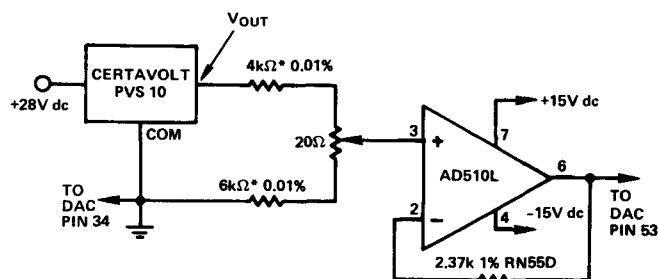
Figure 5. Differential Linearity Adjustment

## IMPROVING LONG TERM-STABILITY AND REFERENCE TEMPERATURE COEFFICIENT

The DAC1136/1137/1138 can be operated with an external reference connected to pin 53 of the module. The current drain on the external reference will be  $1.125\text{mA}$  in bipolar mode or  $0.125\text{mA}$  in unipolar mode (pin 46 should be left open and not grounded when using an external reference in the unipolar mode). When external reference is used, pin 52, the output of the internal reference is left open.

Codi Semiconductor manufactures a reference module called Certavolt<sup>1</sup> with a 10 volt output accurate to 0.001%. This output is temperature compensated to within  $1\text{ppm}/^\circ\text{C}$  from  $+15^\circ\text{C}$  to  $+55^\circ\text{C}$ . The Certavolt requires a power supply of  $+28\text{V dc}$  @  $20\text{mA}$ . To convert the  $+10$  volt output of the Certavolt to the  $+6$  volt required by the DAC, the circuit shown in Figure 6 is recommended.

<sup>1</sup> Certavolt is a registered trade name by Codi Semiconductor.

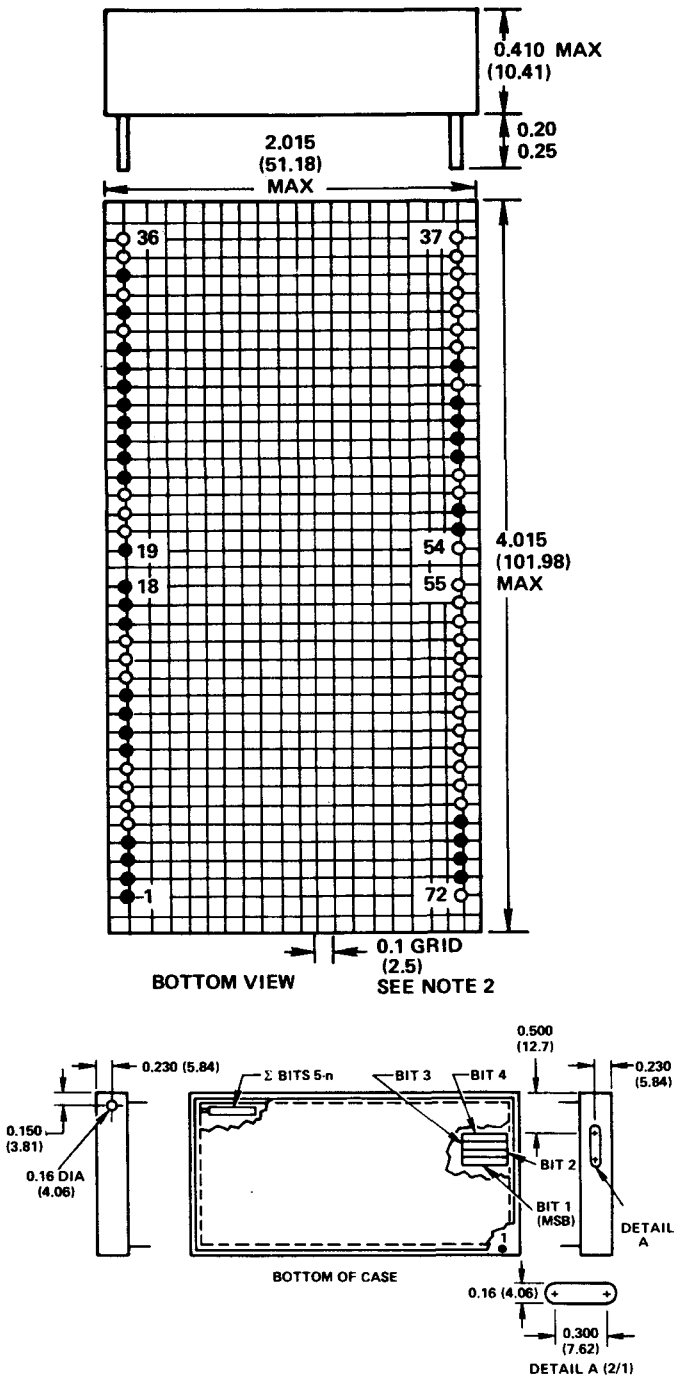


\* VISHAY S102

Figure 6. DAC1136/1137/1138 with External Precision Reference

## OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).



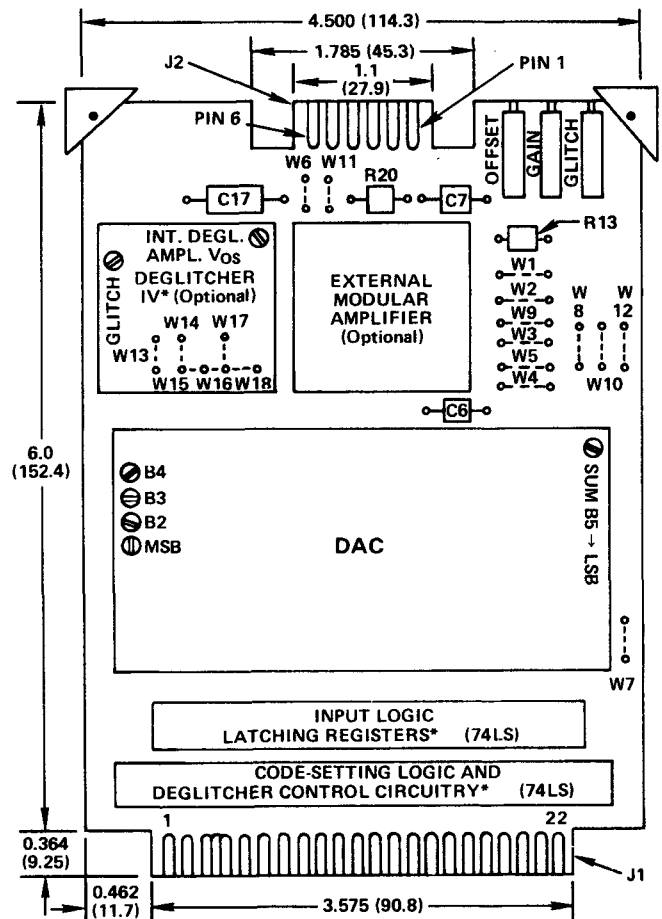
### NOTES:

1. PINS: 0.019 ±0.001 DIA HALF HARD BRASS, GOLD PLATED PER MIL-G-45204B CLASS I, TYPE II.
2. GRID AND MARKINGS NEXT TO PINS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON UNIT.
3. PINS 27 AND 29 ARE NOT PRESENT ON DAC1136.

## OPTIONAL CARD MOUNTED ASSEMBLY

The high resolution of the DAC1136/1137/1138 demands that considerable thought be given to the wiring connections to the module, even when simply evaluating the unit in a temporary laboratory bench set-up. Analog Devices offers an optional card mounted assembly designed to provide optimum performance at the 18-bit level. As shown in Figure 7, this 4 1/2" X 6" printed circuit card can be ordered with input and output options to suit most applications.

The card includes the appropriate DAC, gain and offset adjustment potentiometers, and power supply bypass capacitors. In addition, the card mounted assembly can be ordered with input registers and code-setting logic, external output amplifiers, and a deglitcher. For optimum performance, the card mounted assembly has been designed with a separate analog and digital connector, which are supplied with the unit.



\*THESE ITEMS ARE NOT AVAILABLE ON THE "DIRECT" CARD-MOUNTED ASSEMBLY (W'S INDICATE JUMPER POSITIONS).

Figure 7. Card Mounted Assembly

### CONNECTOR J1

| PIN | FUNCTION | PIN  | FUNCTION            |
|-----|----------|------|---------------------|
| A   | BIT 1    | U    | STROBE              |
| B   | BIT 2    | V    | BIT 18 <sup>1</sup> |
| C   | BIT 3    | W    | +5V                 |
| D   | BIT 4    | X    | +15V                |
| E   | BIT 5    | Y    | -15V                |
| F   | BIT 6    | Z    | DIGITAL GND         |
| H   | BIT 7    | 1-4  | NC                  |
| J   | BIT 8    | 5    | INTERLOCK           |
| K   | BIT 9    | 6    | INTERLOCK           |
| L   | BIT 10   | 7-16 | NC                  |
| M   | BIT 11   | 17   | BIT 17 <sup>1</sup> |
| N   | BIT 12   | 18   |                     |
| P   | BIT 13   | 19   |                     |
| R   | BIT 14   | 20   |                     |
| S   | BIT 15   | 21   |                     |
| T   | BIT 16   | 22   |                     |

J1 MATES WITH CINCH P.N. 251-22-30-160 (SUPPLIED).

<sup>1</sup> DAC 1137/1138 ONLY

### CONNECTOR J2

| PIN | FUNCTION           |
|-----|--------------------|
| 1   | ANALOG SENSE LOW   |
| 2   | ANALOG SOURCE LOW  |
| 3   | NC                 |
| 4   | ANALOG SOURCE HIGH |
| 5   | ANALOG SENSE HIGH  |
| 6   | ANALOG REF. IN/OUT |
| A   | ANALOG REF. IN/OUT |
| B   | ANALOG SENSE HIGH  |
| C   | ANALOG SOURCE HIGH |
| D   | NC                 |
| E   | ANALOG SOURCE LOW  |
| F   | ANALOG SENSE LOW   |


J2 MATES WITH CINCH P.N. 251-06-30-160 (SUPPLIED).

### Mounting Card Connector Designations

#### INPUT OPTIONS

The card-mounted assembly can be ordered with or without input registers. When the direct input option is chosen, the card-mounted assembly will be shipped without input registers. Input registers are mounted on the card when any other digital input code option is selected. The input code ordered by the user is set at the factory by means of various jumpers in the logic circuitry. See ordering guide for details.

When the card mounted assembly contains input registers the system utilizes a dynamic strobe circuit. Strobe characteristics of input registers are:

1.  Strobe Pulse: One Std. series 74LS load, Leading-Edge-Triggered. Positive pulse should remain HI for  $\geq 100\text{ns}$ .
2. The digital input code can be changed at any time up to and including that instant when the strobe command goes HI.
3. The actual transfer of the input code to the DAC will occur  $\approx 3\mu\text{s}$  after the strobe command; during this  $3\mu\text{s}$  the digital input code to the card assembly should not be changed, in order to prevent the possible coupling of logic noise into the DAC output.

#### OUTPUT OPTIONS

The card assembly for the DAC1136/1137/1138 allows for several user-selectable output configurations:

1. Internal IC Output Amplifier built into the DAC.
2. Analog Devices model 234L; for low noise, low drift applications ( $2\mu\text{V}$ ,  $\pm 0.1\mu\text{V}/^\circ\text{C}$ ).
3. Analog Devices model 44K; recommended only for high speed or high current applications ( $75\mu\text{s}$  settling to 0.0002%, 20mA).
4. Deglitcher IV with self-contained output amplifier.
5. Deglitcher IV with model 234L output amplifier.
6. Deglitcher IV with model 44K output amplifier.

#### DEGLITCHER IV

The Deglitcher IV is a precision high-speed, high-isolation sample-and-hold circuit which eliminates the glitches that occur whenever a DAC is dithered through a major carry. Such momentary transients can be of concern in applications such as high-resolution CRT beam positioning, where glitch-free code transitions are often required for optimum display quality and legibility. Oscilloscope photographs in Figures 8a and 8b below show the output of a DAC1136 being dithered up and down through the major carry, between codes 1000000000000000 and 0111111111111111. In Figure 8b, the Deglitcher IV is turned on, virtually eliminating the glitches and allowing the  $152\mu\text{V}$  LSB step to be clearly seen.

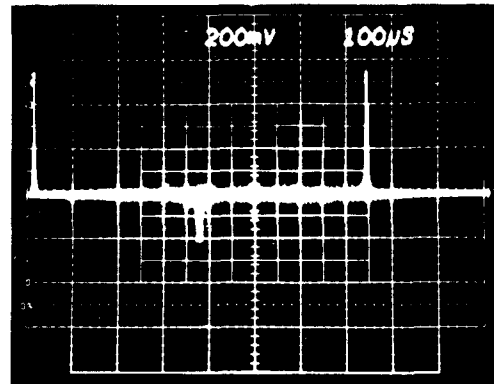


Figure 8a. DAC1136; Major-Carry Dither without Deglitcher IV (BW = 1MHz)

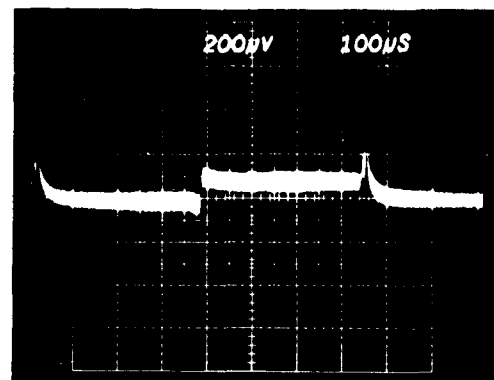


Figure 8b. Same Major-Carry Dither with Deglitcher IV (BW = 1MHz)

The Deglitcher IV utilizes a proprietary sampling technique which isolates the output amplifier during the critical 10 $\mu$ s period immediately following a code change. The only discernible difference in DAC performance when used with Deglitcher IV is a delay of approximately 13 $\mu$ s after the strobe goes HI before the (deglitched) DAC output voltages starts slewing toward the new value.

### GLITCH ADJUSTMENT

There are two glitch adjustment potentiometers on the mounting card assembly. With the DAC updating on the major carry, adjust the external glitch potentiometer for optimum glitch. If necessary, glitch adjustment can also be made with glitch potentiometer internal to Deglitcher IV.

### CARD-MOUNTED ASSEMBLY JUMPER DESIGNATIONS

The output voltage range, reference source, amplifier and deglitcher configuration can be programmed by the user, if necessary, by means of jumpers, resistors and capacitors, as shown below.

| <u>Output Voltage Range</u> | <u>Install Jumpers</u> |
|-----------------------------|------------------------|
| $\pm 10V$                   | W10, W5                |
| $\pm 5V$                    | W12, W5                |
| +10V                        | W12, W3                |

| <u>Reference</u> | <u>Install Jumpers</u> |
|------------------|------------------------|
| Internal         | W2                     |
| External         | W1                     |

| <u>Amplifier</u>                  | <u>Install Jumpers</u> |
|-----------------------------------|------------------------|
| Internal                          | W4, W9                 |
| External <sup>1</sup>             | W8, W13                |
| Deglitcher IV <sup>2</sup>        | W8, W15, W17, W18      |
| Deg. IV with Ext Amp <sup>3</sup> | W8, W14, W16           |

#### NOTES:

<sup>1</sup> With a 234L amplifier install C7 (0.01 $\mu$ F, 10%, ceramic capacitor). With a 44K amplifier use a variable resistor (typ value  $\approx$  499 $\Omega$ , 0.1W, 1%) to adjust the output voltage for a  $\pm 100\mu$ V reading as measured between pins 69 and 34 of the DAC (this step sets voltage compliance); install this value resistor (R13 position).

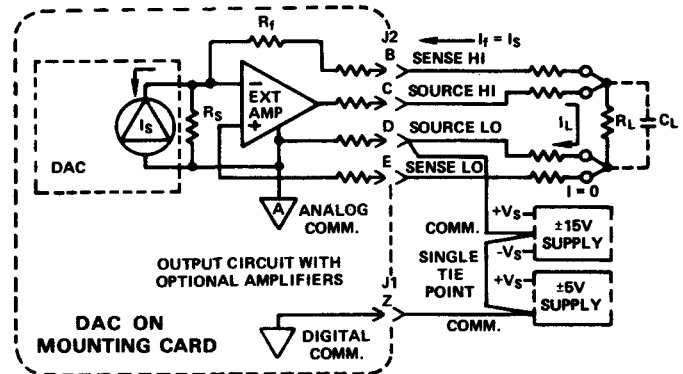
<sup>2</sup> With Deglitcher IV remove R20 (100 $\Omega$ ) and replace the resistor with a jumper.

<sup>3</sup> With Deglitcher IV and a 234L amplifier install: C7 (0.01 $\mu$ F, 10% ceramic capacitor), C6 (220pF, 10%, ceramic capacitor), C17 (1000pF, 10%, polystyrene capacitor) and replace R20 (100 $\Omega$ ) with a jumper. With Deglitcher IV and a 44K amplifier perform the operation described in note 1 and install: C6 (220pF, 10%, ceramic capacitor), C17 (1000pF, 10%, polystyrene capacitor) and replace R20 (100 $\Omega$ ) with a jumper.

To isolate analog and digital grounds, W7 is omitted (refer to Figure 7 for recommended ground tie point).

W6 and W11 are not installed on standard units; this allows 4-wire connection to J2 when either a 44K or 234L amplifier is used.

When using an external amplifier, a four terminal output connection can be utilized on the card assembly in order to allow for compensation of connector contact resistance. See Figure 9.



#### NOTE:

- VOLTAGE DROP BETWEEN SOURCE LO AND SENSE LO MUST OBSERVE CURRENT MODE COMPLIANCE LIMITS FOR RATED ACCURACY.
- THIS CONNECTION SCHEME CANNOT BE USED WITH INTERNAL AMPLIFIER OF THE DAC OR DEGLITCHER IV.

Figure 9. Output Circuit with Optional Amplifiers

## ORDERING GUIDE

### WHEN ORDERING THE DAC1136/1137/1138 WITHOUT THE CARD ASSEMBLY, ORDER EITHER

|          |         |          |
|----------|---------|----------|
| DAC1136J | DAC1137 | DAC1138J |
| DAC1136K |         | DAC1138K |
| DAC1136L |         |          |

When ordering the DAC1136/1137/1138 as a Card-Mounted Assembly, the part must be described with 6 suffixes as shown on next page.

DAC 113

| DAC MODULE |      |            |           |
|------------|------|------------|-----------|
| CODE       | CODE | RESOLUTION | LINEARITY |
| 6          | J    | 18 BITS    | 15 BITS   |
| 6          | K    | 16 BITS    | 16 BITS   |
| 6          | L    | 16 BITS    | 16 BITS   |
| 7          | -    | 18 BITS    | 18 BITS   |
| 8          | J    | 18 BITS    | 17 BITS   |
| 8          | K    | 18 BITS    | 18 BITS   |

| CODE | OUTPUT AMPLIFIER                   |
|------|------------------------------------|
| 1    | INTERNAL                           |
| 2    | 44K <sup>1</sup>                   |
| 3    | 234L                               |
| 4    | DEGLITCHER IV                      |
| 5    | DEGLITCHER IV <sup>1</sup> AND 44K |
| 6    | DEGLITCHER IV AND 234L             |

| CODE | INPUT LOGIC CODE <sup>2</sup> |
|------|-------------------------------|
| 0    | DIRECT (C-B) <sup>3</sup>     |
| 1    | BINARY                        |
| 2    | COMP BIN                      |
| 3    | 2'S COMP                      |
| 4    | COMP 2'S COMP                 |
| 5    | SIGN PLUS MAG BIN             |
| 6    | COMP SIGN MAG BIN             |
| 7    | OFFSET BINARY                 |
| 8    | COMP OFFSET BINARY            |

| CODE | OUTPUT VOLTAGE RANGE |
|------|----------------------|
| 1    | +10V                 |
| 2    | ±5V                  |
| 3    | ±10V                 |

| CODE | DAC VOLTAGE REFERENCE |
|------|-----------------------|
| 1    | INTERNAL              |
| 2    | EXTERNAL              |

NOTES:

1. ORDER WITH DAC1136 ONLY.
2. TWO MOUNTING CARDS ARE AVAILABLE: A DIRECT INPUT VERSION (OPTION CODE 0) WITHOUT INPUT LOGIC LATCHING REGISTERS AND A REGISTER VERSION CONTAINING INPUT LOGIC LATCHING REGISTERS. THE REGISTER VERSION IS SUPPLIED WHEN CODES 1 THRU 8 ARE ORDERED.
3. NOT AVAILABLE ON CARD ASSEMBLIES ORDERED WITH DEGLITCHER IV

### PRELIMINARY TECHNICAL DATA

#### FEATURES

- ISA S50.1 Type 3 Class U Output
- Guaranteed Monotonic 0 to +70°C
- Totally Powered From Loop Supply
- Wide Supply Range 10 to 36 Volts
- Self-Contained Data Latch
- Auxiliary Analog Input
- No Minimum Load Requirement

#### GENERAL DESCRIPTION

The DAC1422 is a low power 10-bit digital-to-analog converter with 4-20mA current output designed specifically for the process and industrial control industry. It is the first such product to be totally powered from the loop supply; no other power is required. The DAC1422 consists of CMOS input latching registers, CMOS digital-to-analog converter and a voltage-to-loop current converter. Should computer power fail, the DAC1422 can retain the last data word strobed into the latching registers. An additional voltage-to-loop current converter is included to provide an analog backup in the event of computer power failure. To simplify its use in process control applications, the DAC1422 features wide offset and span adjustments. The three-terminal output structure conforms to the ISAS50.1 type 3, Class U specification.



#### POWER/OUTPUT CONNECTIONS (Figure 2)

The DAC1422 output is a current source designed to drive a grounded load. The maximum value of  $R_L$  is dependent upon the loop supply and full scale output current according to the formula:

$$R_L (\text{max}) = \frac{V_{\text{LOOP}} - 6V}{I_{\text{OUT}} (\text{F.S.})}$$

For example, at 20mA,  $V_{\text{LOOP}} = 24$  Volts, the maximum  $R_L$  is 900Ω. There is no minimum  $R_L$  required; the DAC1422 maintains stated performance into a short circuit load.

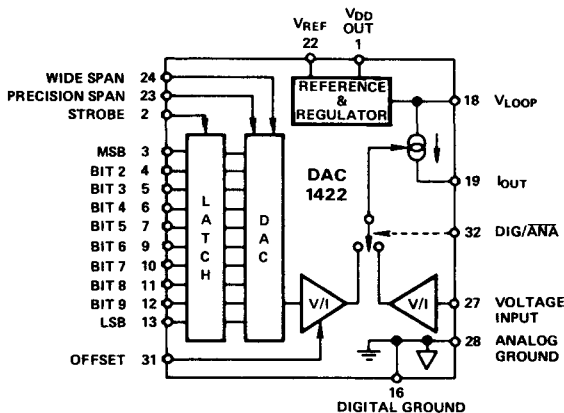


Figure 1. Block Diagram

| DIGITAL INPUT       | NOMINAL CURRENT OUTPUT |
|---------------------|------------------------|
| Binary Code         |                        |
| 1 1 1 1 1 1 1 1 1 1 | +19.984mA              |
| 0 0 0 0 0 0 0 0 0 1 | + 4.016mA              |
| 0 0 0 0 0 0 0 0 0 0 | + 4.000mA              |

Table 1.

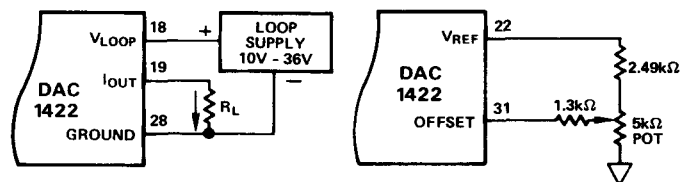


Figure 2. Output/Power Connections

Figure 3. Offset Adjustment Circuit

#### OFFSET ADJUSTMENT (Figure 3)

The DAC1422 is factory trimmed for offset to within ±0.2% FSR (2LSB's). For this performance, leave the offset pin (pin 31) unconnected. If potentiometer trimming is required, the circuit in Figure 2 will provide approximately ±10% offset adjustment. For greater adjustment resolution, increase the resistor in series with pin 31.

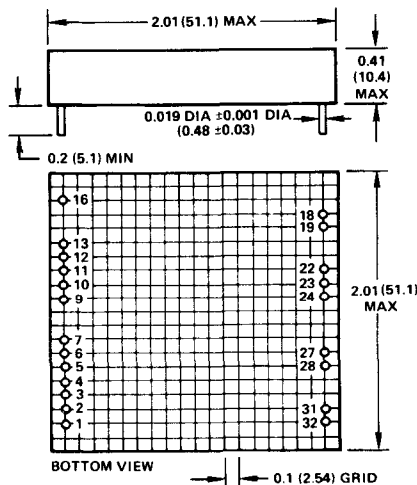
# SPECIFICATIONS

(typical @ +25°C, V<sub>LOOP</sub> = 24 volts unless otherwise specified)

| MODEL                         | DAC1422   |
|-------------------------------|---|
| <b>INPUTS</b>                 |   |
| Resolution                    | 10 Bits   |
| Levels<br>(Except "ANA/DIG")  | CMOS V <sub>DD</sub> = 5V<br>"1" = >3.3V @ 1μA<br>"0" = <1.7V @ 1μA |
| ANA/DIG Input                 |   |
| Impedance                     | 12K   |
| "1"                           | >2.4V @ 140μA   |
| "0"                           | <0.7V @ 0μA   |
| Latch Strobe                  | Rising Edge Sensitive   |
| T <sub>DH</sub> (Data Hold)   | 0ns (min)   |
| T <sub>DS</sub> (Data Set-Up) | 50ns (min)  |
| <b>OUTPUT</b>                 |   |
| Type                          | ISA S50.1 Type 3 Meets and Exceeds Class U                          |
| Nominal Range                 | 4-20mA  |
| Compliance                    | V <sub>LOOP</sub> - 6V  |
| Output Impedance              | >4MΩ @ dc   |
| Minimum Load                  | 0Ω  |
| <b>ANALOG</b>                 |   |
| Monotonicity                  | Guaranteed, 0 to +70°C  |
| Integral Linearity            | ±1/2LSB   |
| Differential Linearity        | ±1/2LSB   |
| Temperature Stability         |   |
| Offset                        | 25ppm/°C FSR  |
| Span                          | 50ppm/°C FSR  |
| Adjustability                 | ±10% minimum, each, Offset and Span                                 |
| Initial Trim Accuracy         | ±2LSB's each, offset and span                                       |
| Analog Input                  |   |
| Range                         | 1 - 5V  |
| Gain                          | 4mA/Volt (1-5V produces 4-20mA)                                     |
| Accuracy                      | ±3%   |
| Stability                     | ±100ppm/°C FSR  |
| Input Impedance               | 10 <sup>8</sup> Ω   |
| <b>POWER</b>                  |   |
| Loop Supply, minimum          | +10V  |
| maximum                       | +36V  |
| Power Supply Rejection        | 20ppm/V FSR   |
| Supply Current                | I <sub>OUT</sub> + 30mA   |
| <b>ENVIRONMENTAL</b>          |   |
| Operating Temperature         | 0 to +70°C  |
| Storage Temperature           | -25°C to +85°C  |
| Size                          | 2" X 2" X 0.4"  |

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET: AC1577

## SPAN ADJUSTMENT (Figures 4a & 4b)

If no span adjustment is desired, connect pin 22 (V<sub>REF</sub>) to pin 23 (Precision Span) for factory trimmed span accuracy of ±0.2% (2LSB's). If span adjust is required, the circuit in Figure 4b will allow ±10% minimum span adjustability. To increase the resolution of the adjustable span, use a resistor in series with the pot and reduce the value of the pot accordingly.



Figure 4a. Factory Trimmed Figure 4b. Adjustable Span

## ANALOG BACKUP INPUT (Figure 5)

An Analog Backup Input is provided for use in adjusting the output in the event that the source of digital inputs fails. This is a high impedance voltage input, scaled so that 1-5 volts input give 4-20mA output; it is unaffected by the offset and gain adjustments. To prevent induced errors, this input should not exceed +5.5 volts and should be grounded if not used. Switchover to the analog input is provided by pin 32, the digital/analog control input. When at Logic "1" the output is controlled by the DAC. When at Logic "0", the output is controlled by the analog input. Figure 4 shows one possible use of the analog input: to provide for potentiometer-variable control in the event of computer failure. The V<sub>DD</sub> OUT pin (pin 1) is used as a 5 volt reference for the potentiometer. If this feature is not used, connect pin 32 to pin 1 and pin 27 to ground.

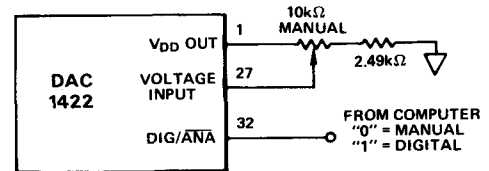


Figure 5. Potentiometer Backup Control

## STROBE INPUT (Figure 6)

The input latch in the DAC1422 is a CMOS rising edge sensitive device. The last loaded digital word remains latched during backup manual operation. The user is cautioned that the digital inputs remain active, even when the control is switched to analog.

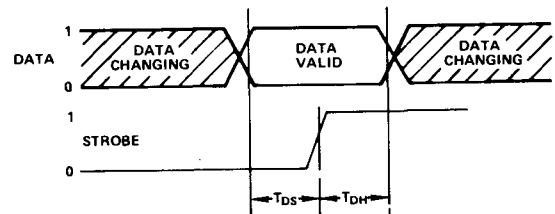


Figure 6. Input Timing

## V<sub>DD</sub> OUTPUT

The V<sub>DD</sub> output may be utilized as a supply for external CMOS circuitry such as tri state or buss transceivers, up to a limit of 1mA I<sub>DD</sub>. If used in this fashion, it is recommended that the user add a 0.1μF bypass capacitor to ground from this pin to keep externally injected "glitches" from disturbing the internal circuitry of the DAC1422.

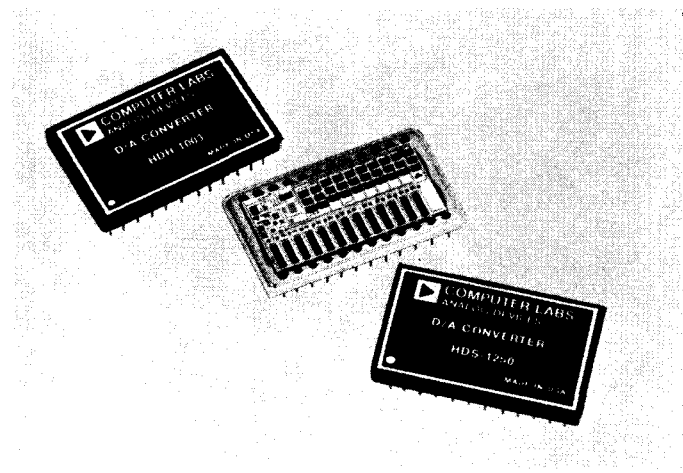
**HDS-0820, -1025, -1250/HDH-0802, -1003, -1205**

## FEATURES

- 25ns Current Settling to 0.1% (HDS)
- 200ns Voltage Settling to 0.1% (HDH)
- 10mA Current Out (HDS)
- Guaranteed Monotonicity Over Temperature
- No External Parts Required
- Reliable Hybrid Construction

## APPLICATIONS

- CRT Vector Displays
- TV Video Reconstruction
- Military Equipment (MIL-STD-883)
- Analytical and Medical Instruments



## GENERAL DESCRIPTION

The HDS/HDH series of digital to analog converters represent the fastest precision settling current and voltage DAC's available. Capable of processing to MIL-STD-883 and guaranteed monotonicity over their operating temperature range; their quiescent power is 1/2 that of competitive units. The current output models provide 10mA full scale allowing direct drive of capacitive loads and transmission lines. All versions have a precision reference and are active laser trimmed to specified accuracy, thus no external adjustment pots or other components are required.

With 6 available units engineering trade-offs can be made between resolution, speed, current or voltage output, and of course price. To facilitate this comparison major specifications are summarized in Table 1.

| Model                 | Resolution | Full Scale Step Settling Time |
|-----------------------|------------|-------------------------------|
| <b>Current Output</b> |            |                               |
| HDS-0820              | 8 Bits     | 10mA Step<br>20ns to 0.4%     |
| HDS-1025              | 10 Bits    | 25ns to 0.1%                  |
| HDS-1250              | 12 Bits    | 35ns to 0.025%                |
| <b>Voltage Output</b> |            |                               |
| HDH-0802              | 8 Bits     | 10V Step<br>200ns to 0.4%     |
| HDH-1003              | 10 Bits    | 300ns to 0.1%                 |
| HDH-1205              | 12 Bits    | 500ns to 0.125%               |

Table 1.

Other general specifications that apply to all devices include TTL logic; glass or hermetic metal package; unipolar or bipolar operation with internal offsetting reference.

The HDH voltage output devices provide access to the op amp summing point so that reduced full scale output voltage swing can be provided. Such operation with an external resistor shunting the internal 1k resistor will reduce the already low op amp offset drift.



# SPECIFICATIONS (typical @ +25°C with nominal power supply voltages unless otherwise noted)

| MODEL   | UNITS      | CURRENT OUT                                 |           |                   | VOLTAGE OUT          |            |              |
|---|------------|---|-----------|-------------------|----------------------|------------|--------------|
|   |            | HDS-0820                                    | HDS-1025  | HDS-1250          | HDH-0802             | HDH-1003   | HDH-1205     |
| RESOLUTION FS = Full Scale                                  | Bits       | 8   | 10        | 12                | 8                    | 10         | 12           |
| LSB WEIGHT  |            | 40μA  | 10μA      | 2.5μA             | 40mV                 | 10mV       | 2.5mV        |
| ACCURACY (Relative to FS Including Linearity)               | ±% FS      | 0.1   | 0.05      | 0.0125            | 0.1                  | 0.05       | 0.0125       |
| Linearity   |            | ±10μA                                       | ±5μA      | ±1.25μA           | ±10mV                | ±5mV       | ±1.25mV      |
|   | LSB        | ±1/4  | ±1/2      | ±1/2              | ±1/4                 | ±1/2       | ±1/2         |
| Monotonicity  |            | Guaranteed Over Operating Temperature Range |           |                   |                      |            |              |
| Zero Offset (Initial)                                       |            | 15nA max                                    | *         | *                 | 10mV typ<br>50mV max | *          | *            |
| TEMPERATURE COEFFICIENTS                                    |            |   |           |                   |                      |            |              |
| Linearity   | ppm/°C     | 3   | *         | *                 | *                    | *          | *            |
| Gain  | ppm/°C     | 30  | *         | *                 | *                    | *          | *            |
| Unipolar Offset   | ppm/°C     | 3   | *         | *                 | *                    | *          | *            |
| Bipolar Offset  | ppm/°C     | 15  | *         | *                 | *                    | *          | *            |
| DATA INPUTS   |            |   |           |                   |                      |            |              |
| Logic Compatibility   |            | TTL and 5V CMOS                             |           |                   |                      |            |              |
| Logic Voltage Levels Positive Logic "1" =                   | V          | +2 to +7                                    | *         | *                 | *                    | *          | *            |
| "0" =   | V          | 0 to +0.8                                   | *         | *                 | *                    | *          | *            |
| Logic Loading (Each Bit) "1" =                              | μA         | 40  | *         | *                 | *                    | *          | *            |
| "0" =   | mA         | -2.6  | *         | *                 | *                    | *          | *            |
| Codes   |            | BIN, OBN                                    |           |                   | BIN, OBN             |            |              |
| OUTPUT  |            |   |           |                   |                      |            |              |
| Current Range FS  |            |   |           |                   |                      |            |              |
| Unipolar  | mA         | +10.24                                      | *         | +10.24<br>±0.05%  | ±25 max              | **         | **           |
| Bipolar   | mA         | ±5.12                                       | *         | ±5.12<br>±0.025%  | ±25 max              | **         | **           |
| Voltage Out FS <sup>1, 2</sup>                              |            |   |           |                   |                      |            |              |
| Unipolar HDS with 200Ω<br>Internal Connected R <sub>L</sub> | V          | +1.024                                      | *         | +1.024<br>±0.05%  | -10.24 ±0.1%         | **         | **           |
| Bipolar   | V          | ±0.512                                      | *         | ±0.512<br>±0.025% | ±5.12 ±0.05%         | **         | **           |
| Compliance  | V          | +1.5, -2                                    | *         | *                 | N/A                  | **         | **           |
| Impedance, Internal (See Figure 1)                          | Ω          | 200   | *         | *                 | 0.1 max              | **         | **           |
| SETTLING TIME   |            |   |           |                   |                      |            |              |
| Current   | ns to % FS | 20 to 0.4                                   | 25 to 0.1 | 35 to 0.025       | N/A                  | N/A        | N/A          |
| Voltage <sup>2</sup>  |            |   |           |                   |                      |            |              |
| Unipolar or Bipolar Out, 75Ω Load,<br>0.56V p-p             | ns to % FS | 30 to 0.4                                   | 35 to 0.1 | 50 to 0.025       | N/A                  | N/A        | N/A          |
| Unipolar or Bipolar Out, Internal<br>200Ω Load, 1.024V p-p  | ns to % FS | 45 to 0.4                                   | 50 to 0.1 | 60 to 0.025       | N/A                  | N/A        | N/A          |
| 10V Output Step   | ns to % FS | N/A   | N/A       | N/A               | 200 to 0.4           | 300 to 0.1 | 500 to 0.025 |
| 5V Output Step  | ns to % FS | N/A   | N/A       | N/A               | 150 to 0.4           | 200 to 0.1 | 350 to 0.025 |
| POWER REQUIREMENTS  |            |   |           |                   |                      |            |              |
| +14.5V to +15.5V  | mA max     | 42  | *         | 50                | 70                   | **         | **           |
| -12V to -16V  | mA max     | 14  | *         | 15                | 40                   | **         | **           |
| Power Supply Rejection Ratio                                | %/V        | 0.2   | *         | *                 | *                    | *          | *            |
| TEMPERATURE RANGE   |            |   |           |                   |                      |            |              |
| Operating - Glass Package                                   | °C         | 0 to +70                                    | *         | *                 | *                    | *          | *            |
| Operating - "M" Metal Case <sup>3</sup>                     | °C         | -55 to +125                                 | *         | *                 | *                    | *          | *            |
| Storage   | °C         | -55 to +125                                 | *         | *                 | *                    | *          | *            |

## NOTES:

<sup>1</sup> Other voltages may be obtained with external resistor.

<sup>2</sup> For HDS series,  $V_{OUT} = I_{OUT} \times R_{equivalent}$  which is the value of the 200Ω internal impedance in parallel with the external load resistance. Thus, by correct selection of external R<sub>L</sub>  $V_{OUT}$  can be any magnitude up to the + or - compliance voltage. See Figures 1 and 2.

<sup>3</sup> Contact factory or local Analog Devices sales office for "M" Metal Case device specifications and prices.

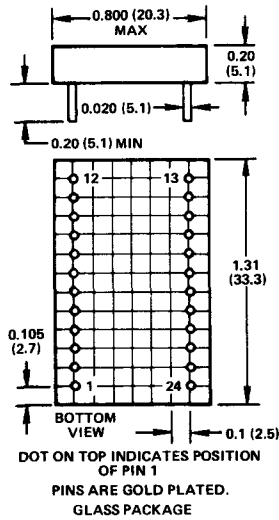
\*Specifications same as HDS-0820.

\*\*Specifications same as HDH-0802.

Specifications subject to change without notice.

### OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



### PIN DESIGNATIONS HDS-0820, HDS-1025

| PIN   | FUNCTION           |
|-------|--------------------|
| 1     | +15V               |
| 2, 3  | BIT 1 (MSB)        |
| 4     | BIT 2              |
| 5     | BIT 3              |
| 6     | BIT 4              |
| 7     | BIT 5              |
| 8     | BIT 6              |
| 9     | BIT 7              |
| 10    | BIT 8              |
| 11    | BIT 9 (HDS-1025)   |
| 12    | BIT 10             |
| 13-20 | GND                |
| 21    | OUTPUT             |
| 22    | $R_L$ 200 $\Omega$ |
| 23    | BIPOLAR OFFSET     |
| 24    | -15V               |

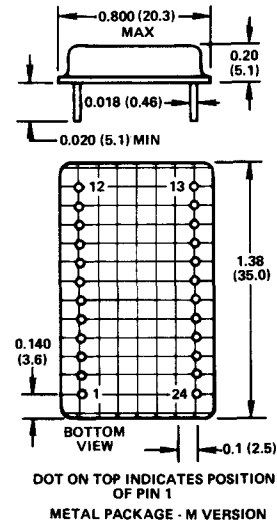
| Analog Output, $\pm 5.12$ mA | Offset Binary |
|------------------------------|---------------|
| +5.11mA (1LSB)               | 111.....1     |
| +2.56mA                      | 110.....0     |
| 0mA                          | 100.....0     |
| -2.56mA                      | 010.....0     |
| -5.12mA                      | 000.....0     |

| Analog Output, 0 to +10.24mA | Straight Binary |
|------------------------------|-----------------|
| +10.23mA                     | 111.....1       |
| +7.68mA                      | 110.....0       |
| +5.12mA                      | 100.....0       |
| +2.56mA                      | 010.....0       |
| 0mA                          | 000.....0       |

Table 2. Coding HDS Series

### OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



### PIN DESIGNATIONS HDH SERIES

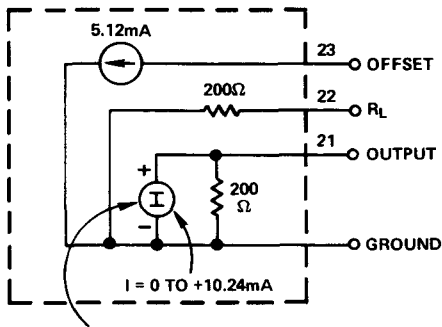
| PIN   | FUNCTION       |
|-------|----------------|
| 1     | BIT 1 (MSB)    |
| 2     | BIT 2          |
| 3     | BIT 3          |
| 4     | BIT 4          |
| 5     | BIT 5          |
| 6     | BIT 6          |
| 7     | BIT 7          |
| 8     | BIT 8          |
| 9     | BIT 9          |
| 10    | BIT 10         |
| 11    | BIT 11         |
| 12    | BIT 12         |
| 13-19 | GROUND         |
| 20    | SUM NODE       |
| 21    | OUTPUT         |
| 22    | BIPOLAR OFFSET |
| 23    | -15V           |
| 24    | +15V           |

ON HDH-0802 DEVICES, GROUND PINS 9, 10, 11 AND 12.  
ON HDH-1003 DEVICES, GROUND PINS 11 AND 12.

| Analog Output, $\pm 5.12$ V | Complement Offset Binary |
|-----------------------------|--------------------------|
| -5.1175V                    | 111.....1                |
| -2.56V                      | 110.....0                |
| 0V                          | 100.....0                |
| +2.56V                      | 010.....0                |
| +5.12V                      | 000.....0                |

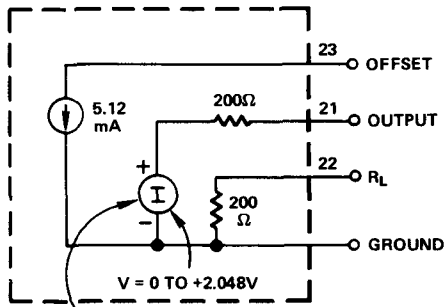
| Analog Output, 0 to +10.24V | Complement Binary |
|-----------------------------|-------------------|
| -10.2375V                   | 111.....1         |
| -7.68V                      | 110.....0         |
| -5.12V                      | 100.....0         |
| -2.56V                      | 010.....0         |
| 0V                          | 000.....0         |

Table 3. Coding HDH Series



CURRENT CONTROLLED BY DIGITAL INPUT CODE

Figure 1. HDS Current Equivalent Circuit



VOLTAGE CONTROLLED BY DIGITAL INPUT CODE

Figure 2. HDS Voltage Equivalent Circuit

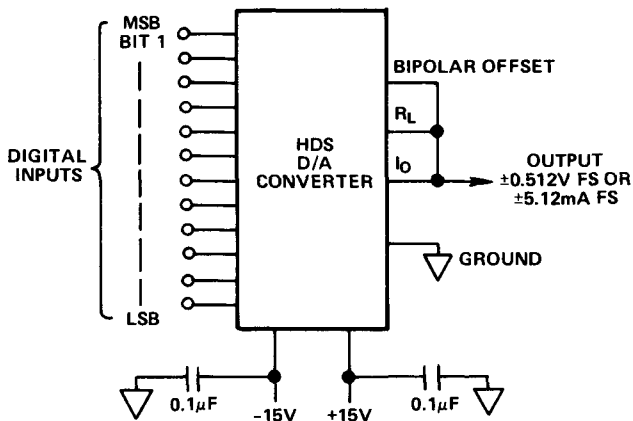


Figure 3. Bipolar Current Output

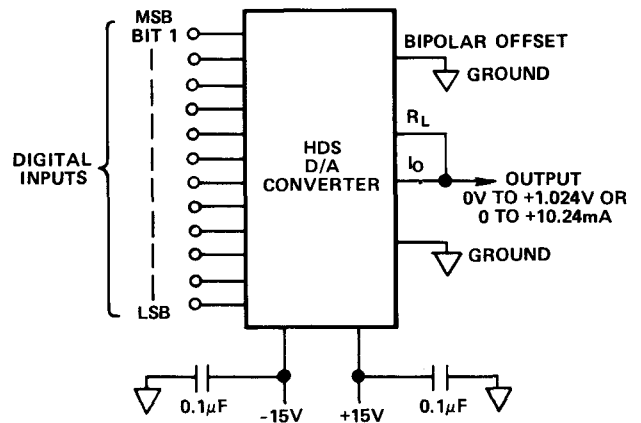
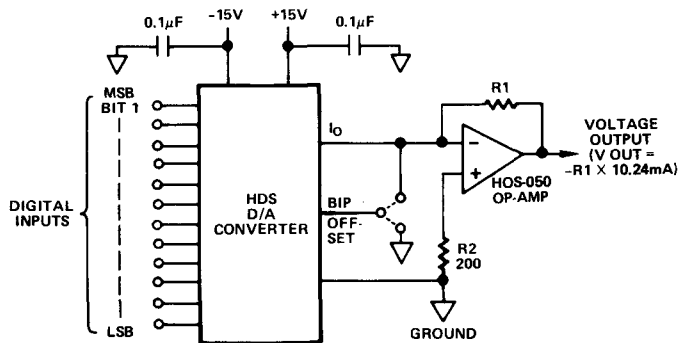


Figure 4. Unipolar Current Output

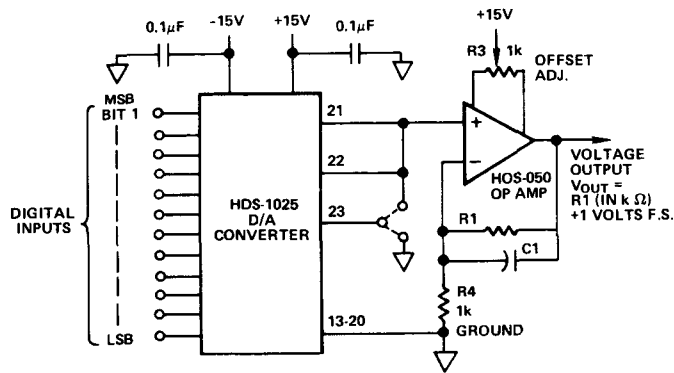


CIRCUIT PROVIDES UNIPOLAR NEGATIVE OUTPUT WITH COMPLEMENT BINARY CODING (BIPOLAR OFFSET GROUND) OR BIPOLAR OUTPUT WITH COMPLEMENTARY OFFSET BINARY CODING (BIPOLAR OFFSET TO  $i_o$ ).  
SETTLING TIME FOR 10.24V OUTPUT ( $R_1 = 1k$ ) IS APPROXIMATELY 150ns.

Figure 5. Inverting Unipolar or Bipolar Voltage Output

#### ORDERING INFORMATION

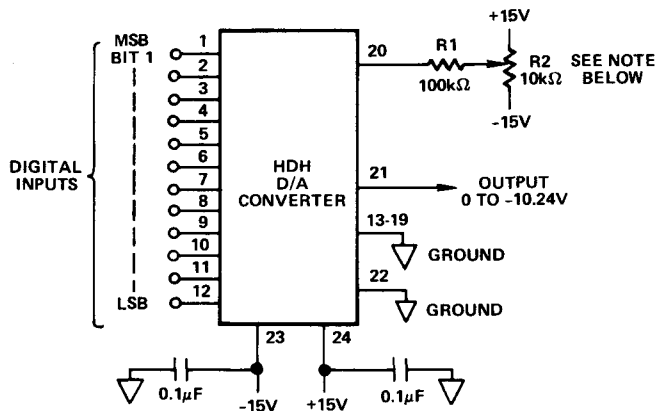
Order model number HDS-0820, HDS-1025, HDS-1250, HDH-0802, HDH-1003, HDH-1205. Models with extended operating temperature range, hermetically-sealed metal-case construction (M versions) and MIL-STD-883 processing are also available. Consult factor or local Analog Devices sales office for further information.



**NOTES:**

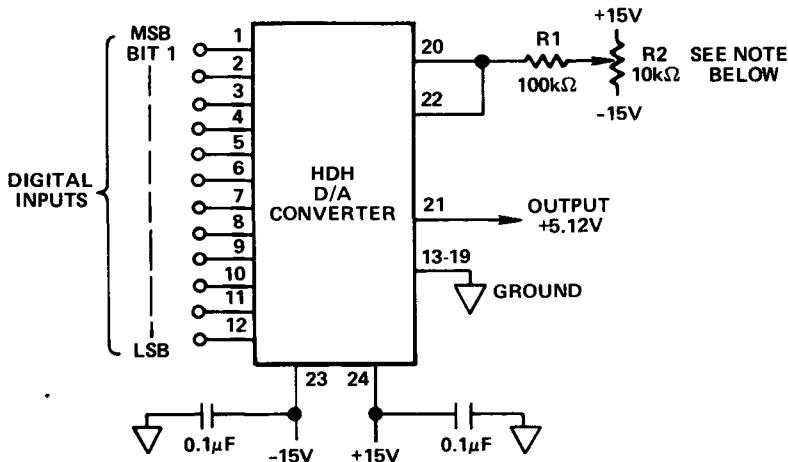
1. CIRCUIT SHOWN FOR UNIPOLAR POSITIVE OUTPUT. OUTPUT SETTING TIME IS APPROXIMATELY 150ns.
2. FOR 0 to +10V OUTPUT, R1 = 9k $\Omega$ .
3. R3 IS ADJUSTED TO COMPENSATE OP-AMP OFFSET.
4. FOR UNIPOLAR OUTPUT, GROUND PIN 23. FOR BIPOLAR OUTPUT, SHORT PIN 23 TO PIN 21 AND UNGROUND PIN 23.
5. C1 IS APPROXIMATELY 10pF AND MAY BE ADJUSTED FOR BEST TRANSIENT RESPONSE.

**Figure 6. Noninverting Unipolar or Bipolar Voltage Output – HDS-1025**



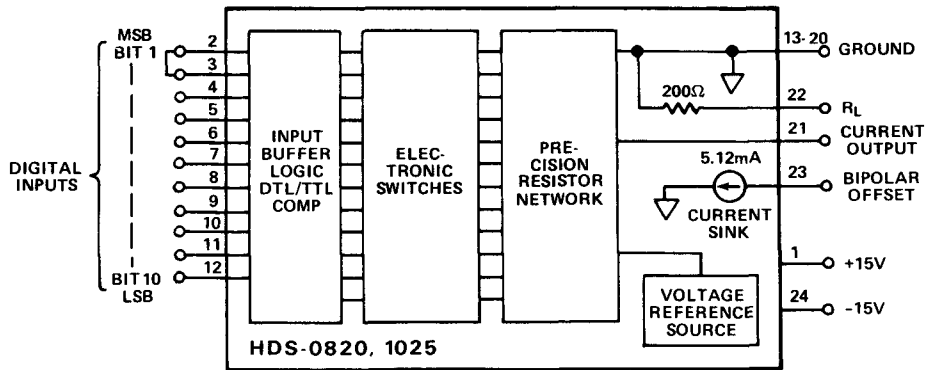
NOTE: R1 and R2 ARE OPTIONAL AND USED ONLY WHEN PRECISE ZEROING OF THE OUTPUT (<10mV) IS REQUIRED.

**Figure 7. Unipolar Negative Output**



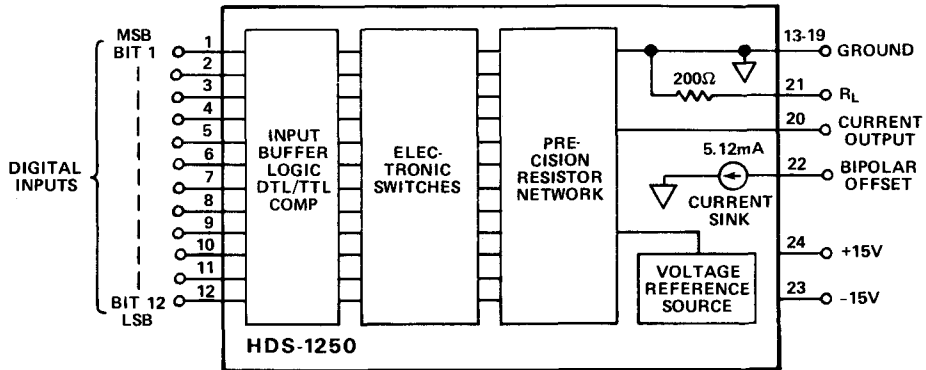
NOTE: R1 and R2 ARE OPTIONAL AND USED ONLY WHEN PRECISE ZEROING OF THE OUTPUT (<10mV) IS REQUIRED.

**Figure 8. Bipolar Output**

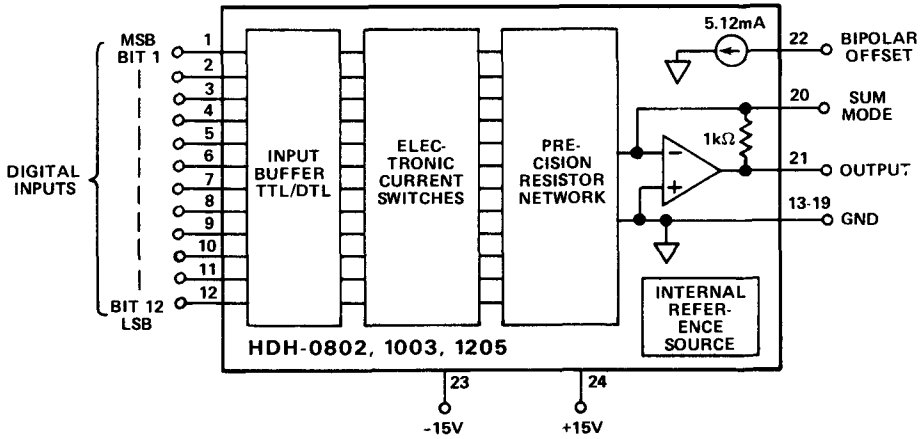


NOTE: ON 8-BIT VERSIONS, PINS 11 AND 12 ARE NOT CONNECTED INTERNALLY, AND PIN 10 IS LSB.

Block Diagram – HDS-0820 and HDS-1025



Block Diagram – HDS-1250



NOTE: ON HDH-0802 DEVICES, GROUND PINS 9, 10, 11 AND 12. ON HDH-1003 DEVICES, GROUND PINS 11 AND 12.

Block Diagram – HDH-0802, HDH-1003 and HDH-1205

### FEATURES

- Ultra-High Speed: 20MHz Word Rate
- 8- and 10-Bit Versions Available
- TTL Compatible
- Smallest Size Available: 3" X 4" X 0.5"
- Completely Self-Contained with Input Register, D/A, Deglitcher, Timing, Internal References, and Output Buffering

### APPLICATIONS

- Color-Television Video Reconstruction, Time-Base Correction and Frame Synchronization
- Graphic Displays
- Deflection Systems
- Character Generators
- High Speed D/A Systems

### GENERAL DESCRIPTION

The MDD Series is a subsystem module which contains an input digital register, ultra-high speed current output D/A converter, deglitcher, output buffer amplifier, precision references, and timing circuitry within a 3"X4"X0.5" case. The output of the device is an ultra-linear analog representation of the digital input. Requiring only external gain and offset potentiometers for final calibration, the MDD D/A solves the glitch problem associated with high-speed D/A converters. The incorporation of an internal register virtually eliminates the need for input bit time deskewing. While not totally eliminating the glitch per se, the remnant glitch is very small, and more importantly, constant (and therefore filterable) over the output range.

The MDD Series is available with 8- or 10-bit resolution and in two versions. The basic versions contain a unity gain output buffer and can deliver 2V p-p open circuit (or 1V p-p into a load) when the MDD output is both source and load terminated. The "A" versions contain a very high speed output gain amplifier to allow the MDD to deliver 4V p-p open circuit (or 2V p-p into a load) when the device is source and load terminated. Higher output voltages may be obtained—up to  $\pm 10V$  by external feedback resistor selection. However, settling time degradation must be expected.

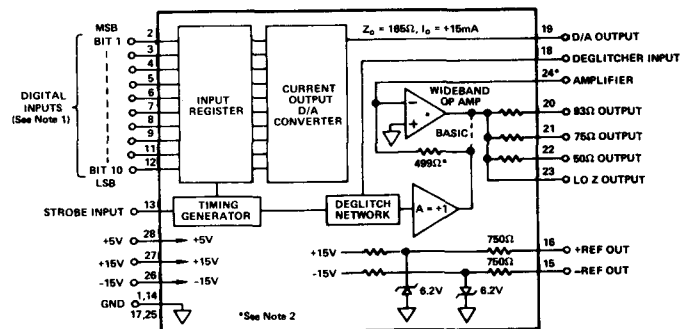
### TV APPLICATION

The "A" version of the MDD Series deglitched D/A is ideally suited for color television video reconstruction. Its output can directly drive the low impedances normally associated with video baseband transmission. Since the output impedance of



the internal operational amplifier is less than  $1\Omega$ , the transmission-line match obtained with the internal source terminating resistor is almost perfect. Other applications include waveform generation, automatic test equipment, and fast process control systems.

Designed primarily for PC board mounting, these D/A's may also be plugged into pin sockets. The pins are 0.04" diameter, gold plated, and are on 0.2" centers. For increased reliability, each module is burned-in for 96 hours at  $+25^\circ C$  before final test and shipment.



- NOTES:  
 1. INPUTS SHOWN FOR 10-BIT VERSIONS. FOR 8-BIT VERSIONS PINS 11 AND 12 ARE UNUSED.  
 2. THESE PARTS (\*) ARE OMITTED IN BASIC VERSIONS, BUT PRESENT IN "A" VERSIONS.

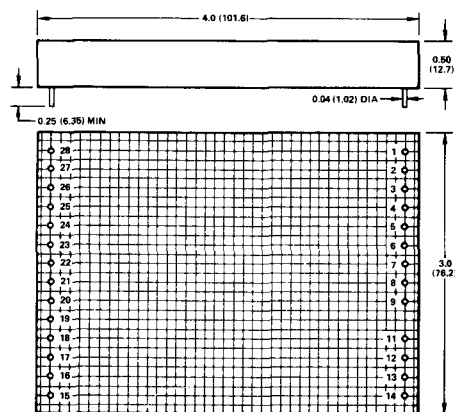
*MDD Series Block Diagram*

# SPECIFICATIONS (typical at +25°C and nominal supply voltages unless otherwise noted)

| MODEL   | MDD-0820<br>MDD-0820A  | MDD-1020<br>MDD-1020A   |
|---|--|---|
| <b>RESOLUTION</b>   | 8 Bits   | 10 Bits   |
| Accuracy (including linearity) at<br>Maximum Word Rate of 20MHz | ±0.2%  | ±0.05%  |
| Monotonicity  | Guaranteed 0 to +70°C  |   |
| <b>DIGITAL DATA BIT INPUTS</b>                                  | 1 Standard "S" TTL Load  |   |
| Logic Level/Load  | "1" = +2.4V to +5V   |   |
| Positive Logic-Binary (BIN)                                     | "0" = 0V to +0.4V  |   |
| <b>DIGITAL STROBE INPUT</b>                                     | 2 Standard "S" TTL Loads   |   |
| Logic Level/Load  | "1" = +2.4V to +5V   |   |
| Positive Logic  | "0" = 0V to +0.4V  |   |
| Risetime and Falltime   | 10ns max   |   |
| Width   | 15ns min   |   |
| Timing  | Negative-Going Trailing Edge to Occur a<br>Minimum of 20ns After Last Data Bit<br>Change |   |
| Frequency   | 20MHz max  |   |
| <b>OUTPUT</b>   | <b>MDD-0820</b><br><b>MDD-1020</b>   | <b>MDD-0820A</b><br><b>MDD-1020A</b>                                    |
| Voltage, No Load, Unipolar                                      | 0 to +2V   | Externally Programmable with<br>Gain and Offset Resistor to<br>±10V max |
| Bipolar   | +1V to -1V   |   |
| Impedance   |  |   |
| Pin 23, Low Z   | 10Ω max  | 1Ω max  |
| Pin 22, 50Ω   | 50Ω ±5%  | 50Ω ±1%   |
| Pin 21, 75Ω   | 75Ω ±5%  | 75Ω ±1%   |
| Pin 20, 93Ω   | 93Ω ±5%  | 93Ω ±1%   |
| Amplifier Current   | ±50mA for dc load = 100Ω min,<br>dc load = Z <sub>OUT</sub> + R <sub>LOAD</sub>          |   |
| DAC Current   | +15mA  |   |
| <b>SETTLING TIME</b>  | 15ns   |   |
| DAC Current Output (to 0.1%)                                    | 50ns to 0.1%   | 120ns to 0.1%   |
| Voltage Output (no load)  | 2V p-p   | 4V p-p  |
| <b>RESIDUAL GLITCH</b>  | 30mV for 2V p-p F.S. Output<br>or 1.5% of F.S.   |   |
| <b>PEDESTAL</b>   | 10mV for 2V p-p F.S. Output<br>or 0.5% of F.S.   |   |
| <b>OUTPUT ZERO OFFSET</b>                                       | Adjustable to Zero   |   |
| <b>OUTPUT ZERO OFFSET vs. TEMP</b>                              | 100ppm/°C  |   |
| <b>GAIN</b>   | Adjustable   |   |
| <b>REFERENCES AVAILABLE</b>                                     | ±6.2V  |   |
| <b>POWER REQUIREMENTS</b>                                       |  |   |
| +15V ±3%  | 120mA  |   |
| -15V ±3%  | 150mA  |   |
| +5V ±5%   | 250mA  |   |
| Power Supply Rejection Ratio                                    | 0.1%/V   |   |
| <b>CASE</b>   | Diallyl Phthalate (per MIL-M-14<br>type SDG-F)   |   |
| <b>TEMPERATURE RANGE</b>  |  |   |
| Operating   | 0 to +70°C   |   |
| Storage   | -55°C to +85°C   |   |

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



BOTTOM VIEW

WEIGHT: 5 oz., 143 G

0.12(3.0)

PINS ARE GOLD PLATED PER MIL-G-5204 TYPE II  
DOT ON TOP INDICATES POSITION OF PIN 1.

## PIN DESIGNATIONS

| PIN | FUNCTION           | PIN | FUNCTION         |
|-----|--------------------|-----|------------------|
| 1   | GROUND*            | 15  | -REF OUT         |
| 2   | BIT 1 INPUT (MSB)  | 16  | +REF OUT         |
| 3   | BIT 2 INPUT        | 17  | GROUND*          |
| 4   | BIT 3 INPUT        | 18  | DEGLITCHER INPUT |
| 5   | BIT 4 INPUT        | 19  | D/A OUTPUT       |
| 6   | BIT 5 INPUT        | 20  | 93Ω OUTPUT       |
| 7   | BIT 6 INPUT        | 21  | 75Ω OUTPUT       |
| 8   | BIT 7 INPUT        | 22  | 50Ω OUTPUT       |
| 9   | BIT 8 INPUT        | 23  | LO Z OUTPUT      |
| 10  | NC                 | 24  | AMP FEEDBACK     |
| 11  | BIT 9 INPUT        | 25  | GROUND*          |
| 12  | BIT 10 INPUT (LSB) | 26  | -15V POWER INPUT |
| 13  | STROBE INPUT       | 27  | +15V POWER INPUT |
| 14  | GROUND*            | 28  | +5V POWER INPUT  |

\*ALL GROUNDS INTERNALLY CORRECTED

Specifications subject to change without notice.

**NOTES ON "DEGLITCHING"**

An MDD Series D/A converter operating with a full-scale p-p analog output of 1V will typically have a glitch, or transient, in its output which is 15mV in amplitude and is 25ns wide, at the 50% points. These typical values are independent of whether the D/A converter is an 8-bit unit or a 10-bit unit.

This glitch remains constant, regardless of the transition points. In other words, it is the same for the transition from 0000000001 to 1000000000 as it is for the transition from 1000000000 to 1000000001 or any other two input words.

A constant glitch is the purpose of the deglitcher circuits. They are intended to hold the area under the curve at a constant value; they are not intended to get rid of all glitches per se.

When the area under the transient curve is held constant, the frequency spectrum of the glitch is a fine line; i.e., a single-line spectrum at the sample rate frequency, and harmonics of the sample frequency.

If the glitch is a function of signal dynamics, as it is in the case of a D/A converter output which is not deglitched, a multitude of intermodulation products are formed. Some of

these IM products appear in the video pass-band as spurious signals and increased noise level. The deglitcher circuits effectively eliminate these products. When they do, the S/N ratio approaches that of an ideally-quantized signal, where the rms noise is  $Q/\sqrt{12}$ , when frequencies above Nyquist are filtered out.

In summary then:

- The remnant glitch for an MDD Series D/A converter is typically 15mV for a full-scale 1V p-p output; this is 1.5% of F.S.
- The glitch width is typically 25ns at the 50% points.
- The amplitude and width of the glitch are constant, and independent of:
  - the magnitude of change in successive transitions
  - number of bits of digital output
  - input (update) data rates

D/A converters without deglitching circuits (such as the Analog Devices' MDS/MDP D/A units) have smaller, shorter glitches, on the average; but this type of converter has larger glitches at the major crossings, especially at the mid-scale transition.

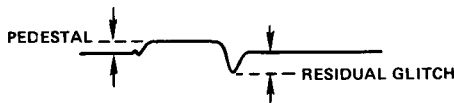


Figure 1. Pedestal/Glitch Relationship

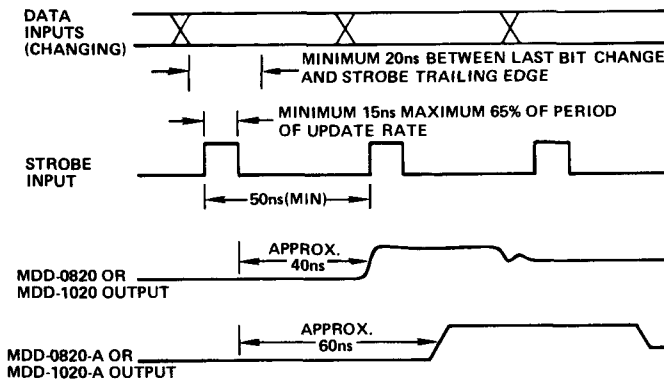


Figure 2. MDD Series Timing Diagram

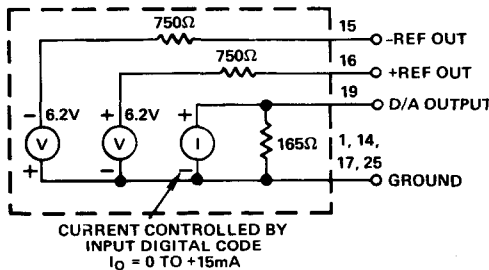


Figure 3. D/A Current Equivalent Circuit

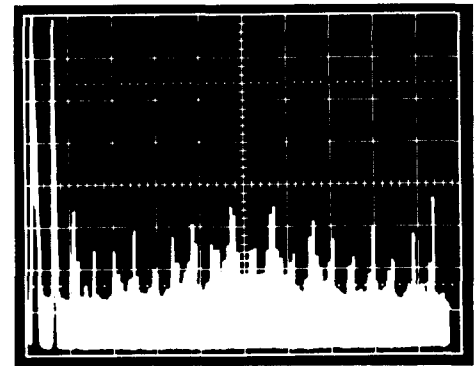


Figure 4. Spectrum of 10-bit D/A Operating at 11MHz Update Rate Without Deglitching - Unfiltered

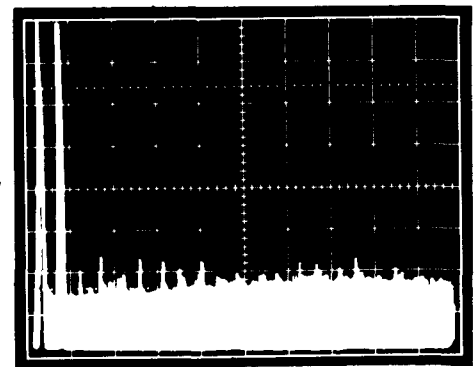


Figure 5. Spectrum of 10-bit D/A Operating at 11MHz Update Rate With Deglitching - Unfiltered



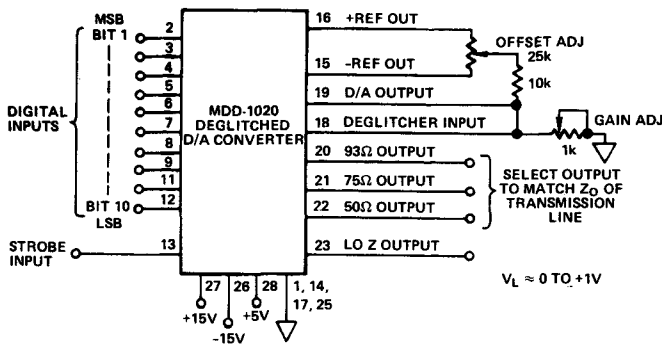


Figure 6. Unipolar Output Configuration Basic Versions

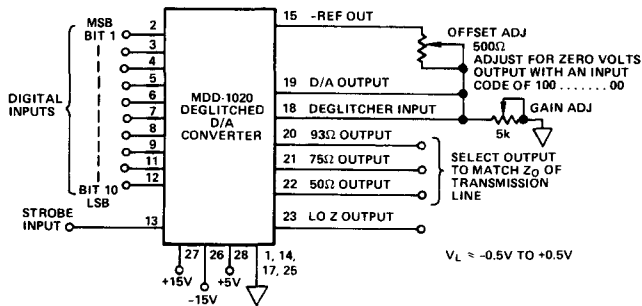


Figure 7. Bipolar Output Configuration Basic Versions

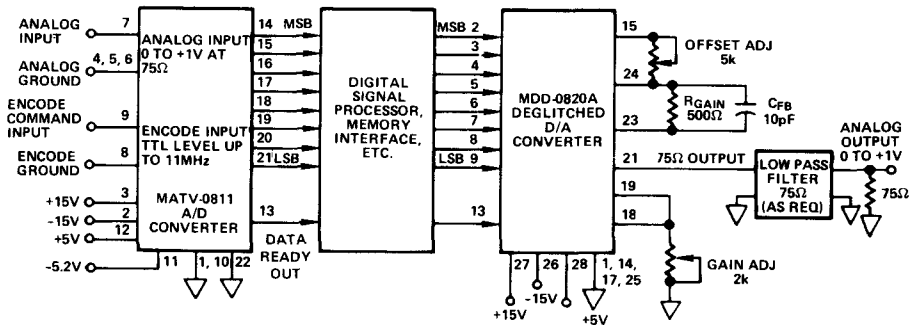
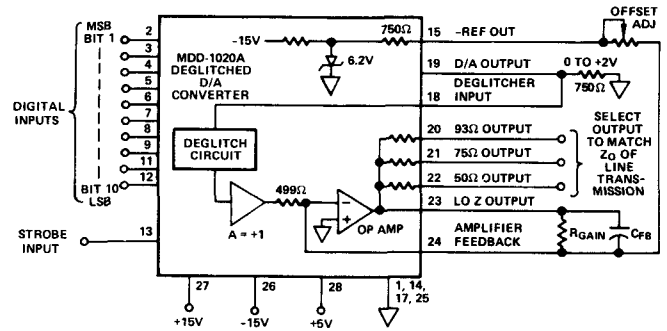


Figure 9. Typical A/D-D/A Back-to-Back Connections for Video Applications or Testing

The typical video differential phase and gain errors (disregarding quantization effects) for the configuration shown are  $3^\circ$  and 3%, respectively, using an encode command frequency of three times the NTSC color subcarrier (10.74MHz). For applications requiring digitization at frequencies of four times NTSC (14.32MHz) or three times PAL (13.29MHz) the MATV-0816 A/D Converter should be substituted. For applications requiring digitization at four times PAL (17.74MHz), the MATV-0820 A/D Converter should be substituted. Results are applicable for either NTSC or PAL test signals using the 20 IRE modulated ramp.

Due to the inherently stable characteristics of the output operational amplifier, the "A" versions are recommended for driving properly terminated video terminated lines.



- NOTES:
1. SELECT  $R_{GAIN}$  TO GIVE DESIRED OPEN CIRCUIT OUTPUT VOLTAGE. THE INPUT VOLTAGE TO THE OP AMP IS APPROXIMATELY 0 TO +2V. THE OUTPUT OF THE OP AMP IS THEREFORE  $(12 \times R_{GAIN}/500\Omega)$  VOLTS P-P.
  2. THE LOGIC IS INVERTED INTERNALLY FOR THE "A" VERSIONS SUCH THAT ALL "1'S" AT THE DIGITAL INPUTS YIELDS A FULL-SCALE POSITIVE VOLTAGE AT THE OP AMP OUTPUT.
  3. FOR POSITIVE UNIPOLAR OPERATION, THE NOMINAL OFFSET POTENTIOMETER RESISTANCE SHOULD BE SET FOR A VALUE OF APPROXIMATELY 800Ω, MAKING A 2000Ω POTENTIOMETER IDEAL.
  4. FOR BIPOLAR OPERATION, THE NOMINAL OFFSET POTENTIOMETER RESISTANCE SHOULD BE SET FOR A VALUE OF APPROXIMATELY 2300Ω, MAKING A 5000Ω POTENTIOMETER IDEAL. THE OUTPUT VOLTAGE SHOULD BE ADJUSTED FOR ZERO WITH AN INPUT CODE OF 10 . . . . . 00.
  5. MAKE  $C_{FB}$  NOMINALLY 10pF. SELECT FOR OPTIMUM SETTLING TIME IF DESIRED.
  6. IF ADJUSTABLE GAIN IS DESIRED, ADD A LOW-VALUE, LOW-INDUCTANCE CERMET TRIMMING POTENTIOMETER IN SERIES WITH  $R_{GAIN}$ . BY PUTTING THE GAIN ADJUSTMENT HERE, THE GAIN AND OFFSET ADJUSTMENTS ARE INDEPENDENT OF EACH OTHER.

Figure 8. Output Configuration - "A" Versions

#### ORDERING INFORMATION

- For 8-Bit Models,      MDD-0820    without output amplifier  
 Order:                    MDD-0820A with output amplifier
- For 10-Bit Models,    MDD-1020    without output amplifier  
 Order:                    MDD-1020A with output amplifier

Mating pin socket connectors for the MDD Series is model MSB-2. Prototyping socket is MSD-1.

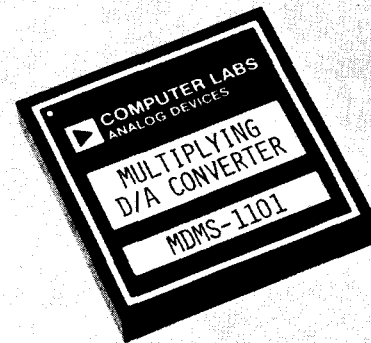
The MDD Series D/A's are normally burned-in at  $+25^\circ\text{C}$  for a minimum of 96 hours. For extended burn-in, consult the factory. All of Analog Devices' data acquisition products are covered by a one-year warranty.

### FEATURES

- Small Size: 2" X 2" X 0.4"
- Highest Speed Available
- High Multiplying Accuracy: Maintains Monotonicity and Linearity for any Analog Input within the Specified Range
- High Current Output: 10mA Full Scale
- High Reliability, Hybrid Microcircuit Construction
- Guaranteed Operation: -30°C to +85°C

### APPLICATIONS

- CRT Displays
- Waveform Generation
- Vector Generation
- Fast Digital Attenuator



### GENERAL DESCRIPTION

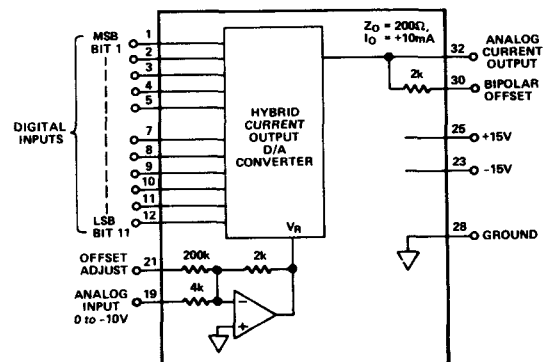
The MDMS series is an ultra-high speed, one or two-quadrant, multiplying D/A converter capable of 10MHz operation and 11-bit precision. The settling time for both analog and digital inputs is 100ns, and the large signal bandwidth of the analog input is in excess of 10MHz. The module is designed for the needs of the graphic display field and other applications requiring high-accuracy, high-speed multiplying operation.

The current output of the MDMS series D/A is precisely proportional to the analog input signal multiplied by the digital input code. The analog input signal may be any voltage between 0V and -10V, and can be a sine wave, triangle wave, sawtooth, or other waveform. The D/A output is an accurate scaled version of the input waveform, the scale factor being the digital input code. Alternatively, the analog input voltage may be used to scale a digitally generated signal. Various offsetting provisions are made so that the analog signal, digital signal, and output may be made bipolar or unipolar in order to accommodate various uses requiring one or two-quadrant operation.

The output impedance of the D/A is 200 ohms so that a two-volt output swing is possible with no load. Loading the output with 200 ohms results in a 1 volt p-p output. If an external operational amplifier such as the Analog Devices' HOS-050 Op Amp is connected to the output of the D/A, output voltages up to 20V p-p are obtainable at a small sacrifice in speed.

### ORDERING INFORMATION

Order Model Number MDMS-0801, MDMS-1001, or MDMS-1101. Ruggedized versions with extended burn-in are also available. Consult the factory.



BIPOlar OPERATION IS ACCOMPLISHED BY CONNECTING PIN 30 TO -15V, OR IF ADJUSTMENT IS REQUIRED, PIN 30 MAY BE CONNECTED THROUGH A 1.5k ADJUSTMENT POTENTIOMETER TO -15V.

MDMS Series - Block Diagram

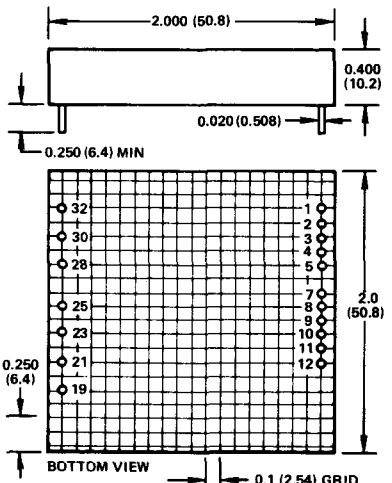
# SPECIFICATIONS (typical @ +25°C and nominal power supply voltages unless otherwise noted)

| MODEL                               | MDMS-0801  | MDMS-1001  | MDMS-1101           |
|-------------------------------------|--|--|---------------------|
| <b>RESOLUTION</b>                   | 8 Bits   | 10 Bits  | 11 Bits             |
| LSB Weight                          | 40µA   | 10µA   | 5µA                 |
| <b>ACCURACY (ADJUSTABLE TO)</b>     | ±0.2%  | ±0.05%   | ±0.025%             |
| Monotonicity                        | Guaranteed   | *  | *                   |
| Linearity                           | 20µA, ±1/2LSB  | 5µA, ±1/2LSB                                       | 2.5µA, ±1/2LSB      |
| <b>ANALOG INPUT</b>                 |  |  |                     |
| Voltage Range                       | 0 to -10V  | *  | *                   |
| Impedance                           | 4kΩ ±2%  | *  | *                   |
| Transfer Function (inverting)       | 0V input scales D/A output to minimum output;<br>-10V input scales D/A output to maximum output. |  |                     |
| <b>DIGITAL INPUT (TTL)</b>          |  |  |                     |
| Positive Logic, "1" =               | +2.4V to +5.0V   | *  | *                   |
| "0" =                               | 0V to 0.4V   | *  | *                   |
| Loading, 2 Std. TTL Loads           |  |  |                     |
| "0" =                               | -5mA   | *  | *                   |
| "1" =                               | 50µA   | *  | *                   |
| <b>CODING (PARALLEL INPUT DATA)</b> |  |  |                     |
| Unipolar                            | BIN  | *  | *                   |
| Bipolar                             | OBN  | *  | *                   |
| All "1's" Input                     |  | Maximum Positive Output                            |                     |
| All "0's" Input                     |  | Maximum Negative Output                            |                     |
| <b>OUTPUT (CURRENT)</b>             |  |  |                     |
| Unipolar                            | 0 to +10mA   | *  | *                   |
| Bipolar                             | ±5mA   | *  | *                   |
| Compliance Voltage                  | +1.5V, -2V   | *  | *                   |
| Impedance                           | 200Ω, ±1%  | *  | *                   |
| Loading                             |  | 200Ω for 0 to 1V p-p Out<br>0Ω for 0 to 2V p-p Out |                     |
| Zero Offset (max)                   | 50nA   | *  | *                   |
| <b>DYNAMIC CHARACTERISTICS</b>      |  |  |                     |
| Settling Time (digital & analog)    | 90ns to 0.2% F.S.  | 100ns to 0.1% F.S.                                 | 130ns to 0.05% F.S. |
| Bandwidth (analog in)               | 10MHz  | *  | *                   |
| <b>TEMPERATURE COEFFICIENTS</b>     |  |  |                     |
| Linearity                           | 2ppm/°C  | *  | *                   |
| Monotonicity                        |  | Guaranteed -30°C to +85°C                          |                     |
| <b>POWER REQUIREMENTS</b>           |  |  |                     |
| +15V ±10%                           | 60mA   | *  | *                   |
| -15V ±10%                           | 20mA   | *  | *                   |
| Power Supply Rejection Ratio        | 0.005%/V   | *  | *                   |
| <b>TEMPERATURE RANGE</b>            |  |  |                     |
| Operating                           |  | -30°C to +85°C                                     |                     |
| Storage                             |  | -55°C to +125°C                                    |                     |
| <b>PHYSICAL CHARACTERISTICS</b>     |  |  |                     |
| Case                                |  | Diallyl Phthalate per MIL-M-14 Type SDG-F          |                     |

\*Specifications same as MDMS-0801  
Specifications subject to change without notice.

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE: DOT ON TOP INDICATES POSITION OF PIN 1  
WEIGHT: 1.6 OZ, 45.3 G  
PINS ARE GOLD PLATED PER MIL-G-5204 TYPE II

## MATING SOCKET MSA-1

## PIN DESIGNATIONS

| PIN | FUNCTION          |
|-----|-------------------|
| 1   | BIT 1 INPUT (MSB) |
| 2   | BIT 2 INPUT       |
| 3   | BIT 3 INPUT       |
| 4   | BIT 4 INPUT       |
| 5   | BIT 5 INPUT       |
| 7   | BIT 6 INPUT       |
| 8   | BIT 7 INPUT       |
| 9   | BIT 8 INPUT       |
| 10  | BIT 9 INPUT       |
| 11  | BIT 10 INPUT      |
| 12  | BIT 11 INPUT LSB  |
| 19  | ANALOG INPUT      |
| 21  | OFFSET ADJ        |
| 23  | -15V POWER INPUT  |
| 25  | +15V POWER INPUT  |
| 28  | GROUND            |
| 30  | BIPOLAR OFFSET    |
| 32  | ANALOG OUTPUT     |

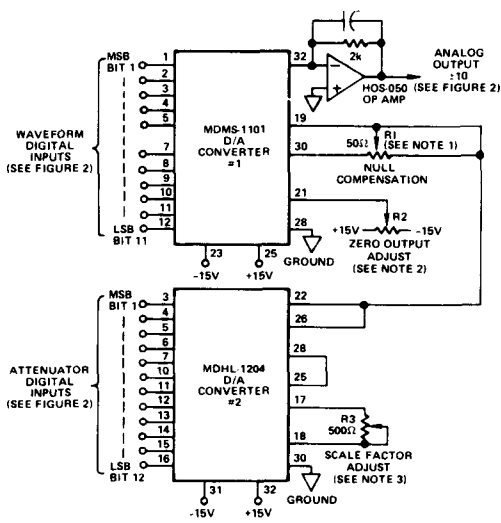
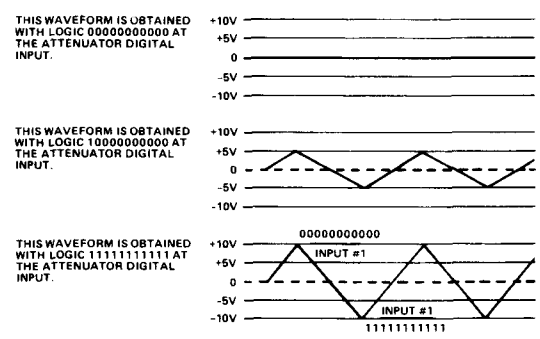


Figure 1. The MDMS-1101 Multiplying D/A Used as a Digital Waveform Generator with Digital Attenuator Control



NOTES  
1. R1 MAY BE OMITTED IF 0.5% DC SHIFT IS PERMISSIBLE BETWEEN MINIMUM & MAXIMUM ATTENUATION.  
2. ADJUST R2 FOR 0V OUTPUT WITH ATTENUATOR INPUT SET FOR 0000000000 AND WAVEFORM INPUT ACTIVE.  
3. ADJUST R3 TO OBTAIN ±10V OUTPUT WITH ATTENUATOR INPUT SET FOR 1111111111 AND WAVEFORM INPUT ACTIVE.

THE ABOVE WAVEFORMS DEPICT THE ANALOG OUTPUT FOR VARIOUS VALUES OF ATTENUATOR DIGITAL INPUTS TO D/A #2 WITH A DIGITAL TRIANGLE BEING APPLIED TO THE WAVEFORM DIGITAL INPUT OF D/A #1.  
PEAK POSITIVE LEVEL = 0000000000 DIGITAL INPUT  
PEAK NEGATIVE LEVEL = 1111111111 DIGITAL INPUT  
(THE OUTPUT OF AMP INVERTS THE SENSE OF THE INPUT BITS)

Figure 2. Operation of Multiplying D/A Circuit

### FEATURES

Current Settling Times to 15ns  
 $\pm 1.5V$  Compliance  
 Voltage Settling Times to 100ns (MDH)  
 Monotonicity Guaranteed Over Temperature  
 High Output Currents — 15mA  
 $-30^{\circ}C$  to  $+85^{\circ}C$  Operating Range  
 Industry Standard Pin Outs  
 20V, p-p Out (MDH)  
 TTL or ECL Logic

### APPLICATIONS

CRT Vector Displays  
 Digital Waveform Generation  
 Automatic Test Equipment  
 TV Picture Reconstruction

### GENERAL DESCRIPTION

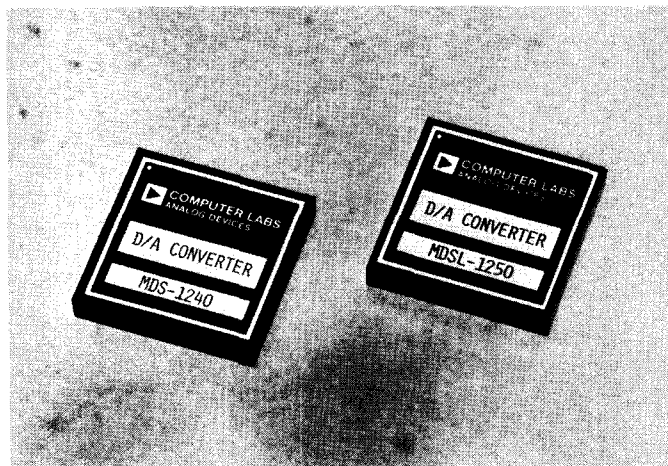
This broad family of digital-to-analog converters represents the "state of the art" in modular, high speed, voltage and current output devices. The family consists of a total of 11 devices in 4 series (MDS, MDSE, MDSL and MDH) that allow the user to make engineering trade-offs between resolution, speed, output and logic type. The first 3 are high compliance current output units which make possible linear output swings greater than  $\pm 1.5V$ . The voltage output MDH series contain a fast settling hybrid operational amplifier which provides  $\pm 10V$  output at  $\pm 50mA$ . To simplify selection these major specifications are summarized in Table 1.

| MODEL                               | BITS | FULL SCALE OUTPUT | FULL SCALE SETTLING TIME | INPUT LOGIC |
|-------------------------------------|------|-------------------|--------------------------|-------------|
| (Fastest Settling High Current Out) |      |                   |                          |             |
| MDS-0815                            | 8    | 15mA              | 15ns to 0.4% FS          | TTL         |
| MDS-1020                            | 10   | 15mA              | 20ns to 0.1% FS          | TTL         |
| MDS-1240                            | 12   | 15mA              | 40ns to 0.025% FS        | TTL         |
| (MDS with ECL Logic)                |      |                   |                          |             |
| MDS-0815E                           | 8    | 15mA              | 15ns to 0.4% FS          | ECL         |
| MDS-1020E                           | 10   | 15mA              | 20ns to 0.1% FS          | ECL         |
| (Low Current MDS)                   |      |                   |                          |             |
| MDSL-0825                           | 8    | 5mA               | 25ns to 0.1%             | TTL         |
| MDSL-1035                           | 10   | 5mA               | 25ns to 0.1%             | TTL         |
| MDSL-1250                           | 12   | 5mA               | 50ns to 0.025%           | TTL         |
| (Voltage Out MDSL)                  |      |                   |                          |             |
| MDH-0870                            | 8    | 10V/50mA          | 150ns to 0.4%            | TTL         |
| MDH-1001                            | 10   | 10V/50mA          | 200ns to 0.1%            | TTL         |
| MDH-1202                            | 12   | 10V/50mA          | 500ns to 0.025%          | TTL         |

Table 1.

### SPEED WITH PRECISION

Analog Devices' model MDS-1240 is the first D/A converter available with highly reliable, internal hybrid construction to



achieve ultra-high speed operation. In fact, it is the fastest 12-bit D/A available, settling to 0.025% in 40ns. Hybrid construction eliminates the thermal lag problem inherent in 12-bit D/A's constructed with discrete components. This in turn means that the accuracy is maintained over the total frequency range of operation, yielding superior results for frequency domain applications.

The MDS-1240 is particularly well suited for CRT display applications because of its unsurpassed speed and drive capabilities. The high output current (15mA) allows the use of low impedance loads so that settling times remain short — even with higher output voltage levels. The ability to drive load capacitance is at least 3 times that of other 12-bit D/A's thus providing capability to drive a terminated transmission line directly. The MDS-815 and MDS-1020 provide similar performance at 8 and 10 bits, while the MDS-E units provide it with ECL logic. MDSL-0825, MDSL-1035 and MDSL-1250 also utilize this reliable hybrid construction. The use of laser trimmed resistor networks within the D/A's not only eliminates thermal time lag errors but provide the linearity tempo of  $2ppm/^{\circ}C$ ; guaranteeing monotonic operation over the extended temperature range of  $-30^{\circ}C$  to  $+85^{\circ}C$ . The power dissipation of the MDSL series is one-half that of competitive D/A's, but a full 5mA output current is maintained. This allows driving transmission lines or other low impedance loads directly.

(continued on page 195S)

# SPECIFICATIONS (typical @ +25°C unless otherwise specified)

| MODEL  | UNITS                   | CURRENT OUTPUT<br>MDS   |            |                          | CURRENT OUTPUT<br>MDS-E (ECL) |            |
|--|-------------------------|---|------------|--------------------------|-------------------------------|------------|
|  |                         | 0815  | 1020       | 1240                     | 0815                          | 1020       |
| RESOLUTION   | Bits                    | 8   | 10         | 12                       | 8                             | 10         |
| LSB (Weight)   | $\mu\text{A}$           | 58.6  | 14.6       | 3.66                     | 58.6                          | 14.6       |
| ACCURACY   |                         |   |            |                          |                               |            |
| Initial (Adjust to 0)  | $\pm\%FS$               | 0.2   | 0.05       | 0.012                    | 0.2                           | 0.05       |
| Linearity (Integral)   | LSB max                 | $\pm 1/2$   | *          | *                        | *                             | *          |
| Monotonicity   |                         | Guaranteed Over Operating Temp Range                                    |            |                          | *                             | *          |
| Zero Offset (Adjust to 0)                                    |                         | 15nA max  | *          | *                        | *                             | *          |
| TEMPERATURE COEFFICIENTS                                     |                         |   |            |                          |                               |            |
| Linearity  | ppm/ $^{\circ}\text{C}$ | 5   | *          | 2                        | *                             | 2          |
| Gain   | ppm/ $^{\circ}\text{C}$ | 30  | *          | 20                       | *                             | *          |
| Offset (Bipolar)   | ppm/ $^{\circ}\text{C}$ | 15  | *          | *                        | *                             | *          |
| STABILITY WITH TIME  | $\pm\%/yr$ max          | 0.5   | *          | *                        | *                             | *          |
| DATA INPUTS  |                         |   |            |                          |                               |            |
| Logic Compatibility  |                         | TTL   | *          | *                        | ECL                           | ECL        |
| Logic Voltage Levels   |                         |   |            |                          |                               |            |
| Bit On Logic "1"   | V                       | +2 to +5.0  | *          | *                        | -0.9                          | -0.9       |
| Bit Off Logic "0"  | V                       | 0 to +0.4   | *          | *                        | -1.7                          | -1.7       |
| Logic Current (Each Bit)                                     |                         |   |            |                          |                               |            |
| Bit On Logic "1"   | $\mu\text{A}$           | $\leq 50$   | *          | *                        | *                             | *          |
| Bit Off Logic "0"  | mA                      | -8  | *          | -5 max                   | *                             | *          |
| MSB  | mA                      | N/A   | *          | -10 max                  | *                             | *          |
| Coding   |                         | All Units Binary (BIN) for Unipolar,<br>Offset Binary (OBN) for Bipolar |            |                          | *                             | *          |
| OUTPUT   |                         |   |            |                          |                               |            |
| Current Range  |                         |   |            |                          |                               |            |
| Unipolar   | mA                      | 0 to +15  | *          | *                        | 0 to -15                      | 0 to -15   |
| Bipolar  | mA                      | $\pm 7.5$   | *          | *                        | *                             | *          |
| Impedance (See Figure 3)                                     | $\Omega$                | 165   | *          | 200 $\pm 1\%$            | *                             | *          |
| Compliance (MDH $V_{OUT}$ )                                  | V                       | +1.5, -2  | *          | *                        | -1.5, +2                      | -1.5, +2   |
| Load Resistance for $V_{OUT}$ (See Figure 5)                 |                         |   |            |                          |                               |            |
| 0 to +1V   | $\Omega$                | 112   | *          | 100                      | *                             | *          |
| $\pm 1V$   | $\Omega$                | 4.32k   | *          | 750                      | *                             | *          |
| INTERNAL REFERENCE VOLTAGE OUT                               | V                       | N/A   | *          | -6.2 $\pm 5\%$           | *                             | *          |
| SETTLING TIME <sup>2</sup>                                   |                         |   |            |                          |                               |            |
| Current  | ns to %.                | 15 to 0.4   | 20 to 0.10 | 20 to 0.1<br>40 to 0.025 | *                             | 20 to 0.10 |
| Unipolar Voltage ( $R_L = 300\Omega \parallel 10\text{pF}$ ) | ns to %                 |   |            |                          |                               |            |
| Bipolar Voltage ( $R_L = 2325\Omega \parallel 10\text{pF}$ ) | ns to %                 |   |            |                          |                               |            |
| POWER REQUIREMENTS   |                         |   |            |                          |                               |            |
| Range  | V                       | $\pm 11$ to $\pm 16$  | *          | $\pm 14.5$ to $\pm 16.5$ | *                             | *          |
| Current at Nominal +V  | mA max                  | 105   | 120        | 55                       | *                             | 120        |
| Current at Nominal -V  | mA max                  | 15  | *          | 20                       | *                             | *          |
| POWER SUPPLY REJECTION RATIO                                 | %/V                     | 0.04  | *          |                          | *                             | *          |
| +15V   | %/V                     |   |            | -0.0001                  |                               |            |
| -15V (Bipolar)   | %/V                     |   |            | -0.002                   |                               |            |
| -15V (Unipolar)  | %/V                     |   |            | -0.2                     |                               |            |
| TEMPERATURE RANGE  |                         |   |            |                          |                               |            |
| Operating  | $^{\circ}\text{C}$      | -20 to +75  | *          | -30 to +85               | *                             | *          |
| Storage  | $^{\circ}\text{C}$      | -55 to +85  | *          | -55 to +125              | *                             | *          |
| CASE   |                         | Diallyl Phthalate per MIL-M-14 Type SDG-F                               |            |                          | *                             | *          |

\*Specifications same as MDS-0815.

## NOTES:

<sup>1</sup> 1ppm/ $^{\circ}\text{C}$  for current output. Op amp is  $50\mu\text{V}/^{\circ}\text{C}$ . (See tables in Figures 15, 16 and 17, for overall TC in various configurations.)

<sup>2</sup> For Full Scale Step.

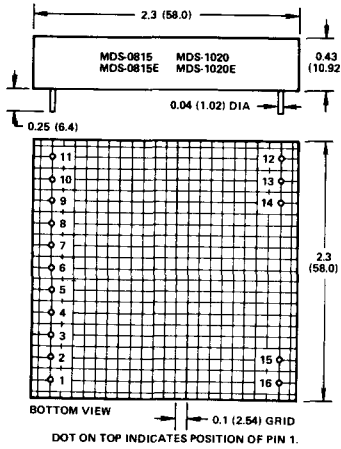
<sup>3</sup> 0 to +5V Out  
<sup>4</sup> 0 to +10V Out  
<sup>5</sup>  $\pm 5V$  Out } See Figures 15 and 16 for test circuits.

Specifications subject to change without notice.

| CURRENT OUTPUT |             |              | VOLTAGE OUT                 |                         |                           |
|----------------|-------------|--------------|-----------------------------|-------------------------|---------------------------|
| MDSL           |             |              | MDH                         |                         |                           |
| 0825           | 1035        | 1250         | 0870                        | 1001                    | 1202                      |
| 8              | 10          | 12           | 8                           | 10                      | 12                        |
| 19.6           | 4.88        | 1.22         | Depends on V <sub>OUT</sub> |                         |                           |
| 0.2            | 0.05        | 0.012        | 0.2                         | 0.05                    | 0.012                     |
| *              | *           | *            | *                           | *                       | *                         |
| *              | *           | *            | *                           | *                       | *                         |
| *              | *           | *            | 10mV                        | 10mV                    | 10mV                      |
| 2              | 2           | 2            | 2                           | 2                       | 2                         |
| 20             | 20          | 20           | 20                          | 20                      | 20                        |
| *              | *           | *            | See Note 1                  |                         |                           |
| *              | *           | *            | *                           | *                       | *                         |
| *              | *           | *            | *                           | *                       | *                         |
| *              | *           | *            | *                           | *                       | *                         |
| -1.6           | -1.6        | -1.6         | -1.6                        | -1.6                    | -1.6                      |
| *              | *           | *            | *                           | *                       | *                         |
| *              | *           | *            | *                           | *                       | *                         |
| *              | *           | *            | *                           | *                       | *                         |
| 0 to +5        | 0 to +5     | 0 to +5      | ±50 max                     | ±50 max                 | ±50 max                   |
| ±2.5           | ±2.5        | ±2.5         | ±50 max                     | ±50 max                 | ±50 max                   |
| 600±1%         | 600±1%      | 600±1%       | 0.1 max                     | 0.1 max                 | 0.1 max                   |
| *              | *           | *            | ±10                         | ±10                     | ±10                       |
| 300            | 300         | 300          | N/A                         | N/A                     | N/A                       |
| 2.325k         | 2.325k      | 2.325k       | N/A                         | N/A                     | N/A                       |
| -6.2±5%        | -6.2±5%     | -6.2±5%      | -6.2±5%                     | -6.2±5%                 | -6.2±5%                   |
| 25 to 0.1      | 25 to 0.1   | 50 to 0.25   | 15 to 0.2                   | 25 to 0.10              | 50 to 0.25                |
| 45 to 0.4      | 70 to 0.1   | 70 to 0.1    | 70 to 0.4 <sup>3</sup>      | 100 to 0.1 <sup>3</sup> | 200 to 0.025 <sup>3</sup> |
| 70 to 0.1      | 80 to 0.05  | 90 to 0.025  | 150 to 0.4 <sup>4</sup>     | 200 to 0.1 <sup>4</sup> | 400 to 0.025 <sup>4</sup> |
| 75 to 0.4      | 100 to 0.1  | 100 to 0.1   | 100 to 0.4 <sup>5</sup>     | 130 to 0.1 <sup>5</sup> | 250 to 0.025 <sup>5</sup> |
| 100 to 0.1     | 110 to 0.05 | 125 to 0.025 |                             |                         |                           |
| ±12 to ±15     | ±12 to ±15  | ±12 to ±15   | ±14.5 to ±16.5              | ±14.5 to ±16.5          | ±14.5 to ±16.5            |
| 26             | 26          | 26           | 50                          | 50                      | 50                        |
| 16             | 16          | 16           | 35                          | 35                      | 35                        |
| 0.0001         | 0.0001      | 0.0001       | 0.003                       | 0.003                   | 0.003                     |
| 0.001          | 0.001       | 0.001        | 0.01                        | 0.01                    | 0.01                      |
| 0.2            | 0.15        | 0.15         | 0.15                        | 0.15                    | 0.15                      |
| -30 to +85     | -30 to +85  | -30 to +85   | -30 to +85                  | -30 to +85              | -30 to +85                |
| -55 to +125    | -55 to +125 | -55 to +125  | -55 to +125                 | -55 to +125             | -55 to +125               |
| *              | *           | *            | *                           | *                       | *                         |

**MDS-0815, 0815E, 1020, 1020E**  
**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



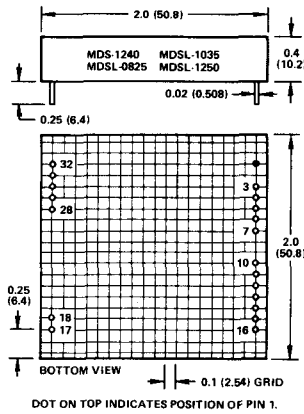
**MATING SOCKET MSB-1 1713**

**PIN DESIGNATIONS**  
**MDS-0815E, 1020E**

| PIN | FUNCTION    | PIN | FUNCTION |
|-----|-------------|-----|----------|
| 1   | BIT 1 (MSB) | 9   | BIT 9    |
| 2   | BIT 2       | 10  | BIT 10   |
| 3   | BIT 3       | 11  | +15V     |
| 4   | BIT 4       | 12  | OFFSET   |
| 5   | BIT 5       | 13  | COMMON   |
| 6   | BIT 6       | 14  | OUTPUT   |
| 7   | BIT 7       | 15  | COMMON   |
| 8   | BIT 8       | 16  | -15V     |

**MDS-1240, MDL-0825, 1035, 1250**  
**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



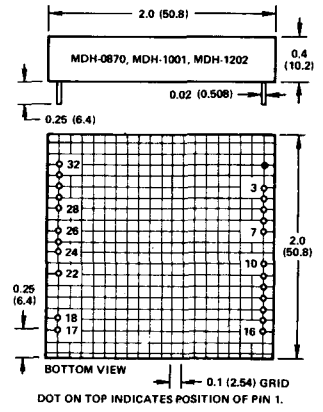
**MATING SOCKET MSA-1**

**PIN DESIGNATIONS**  
**MDS-0815, MDS-1020**

| PIN | FUNCTION    | PIN | FUNCTION |
|-----|-------------|-----|----------|
| 1   | BIT 1 (MSB) | 9   | BIT 9    |
| 2   | BIT 2       | 10  | BIT 10   |
| 3   | BIT 3       | 11  | -15V     |
| 4   | BIT 4       | 12  | OFFSET   |
| 5   | BIT 5       | 13  | COMMON   |
| 6   | BIT 6       | 14  | OUTPUT   |
| 7   | BIT 7       | 15  | COMMON   |
| 8   | BIT 8       | 16  | +15V     |

**MDH-0870, 1001, 1202**  
**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



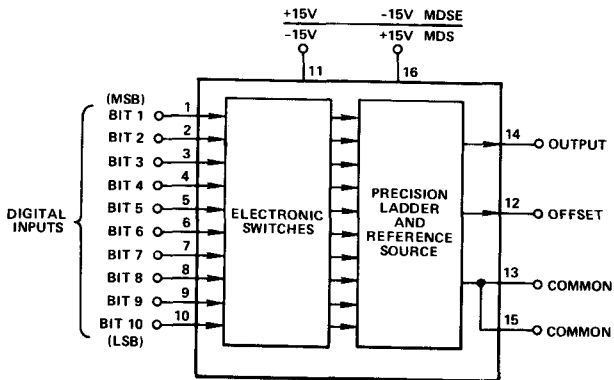
**MATING SOCKET MSA-1**

**PIN DESIGNATIONS**  
**MDS-1240, MDL-0825, 1035, 1250**

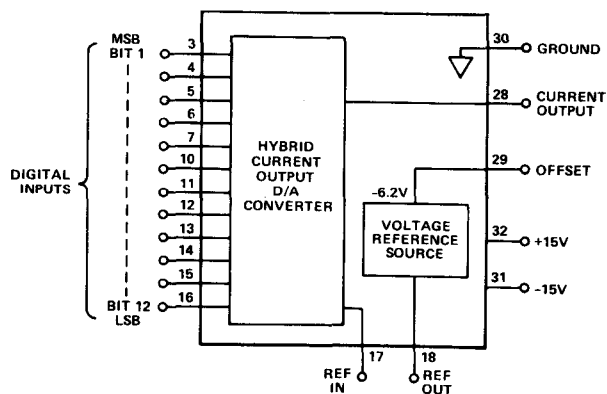
| PIN | FUNCTION          | PIN | FUNCTION         |
|-----|-------------------|-----|------------------|
| 3   | BIT 1 INPUT (MSB) | 15  | BIT 11 INPUT     |
| 4   | BIT 2 INPUT       | 16  | BIT 12 INPUT     |
| 5   | BIT 3 INPUT       | 17  | REFERENCE INPUT  |
| 6   | BIT 4 INPUT       | 18  | REFERENCE OUTPUT |
| 7   | BIT 5 INPUT       | 28  | ANALOG OUTPUT    |
| 10  | BIT 6 INPUT       | 29  | OFFSET           |
| 11  | BIT 7 INPUT       | 30  | GROUND           |
| 12  | BIT 8 INPUT       | 31  | -15V POWER INPUT |
| 13  | BIT 9 INPUT       | 32  | +15V POWER INPUT |
| 14  | BIT 10 INPUT      |     |                  |

**PIN DESIGNATIONS**  
**MDH-0870, 1001, 1202**

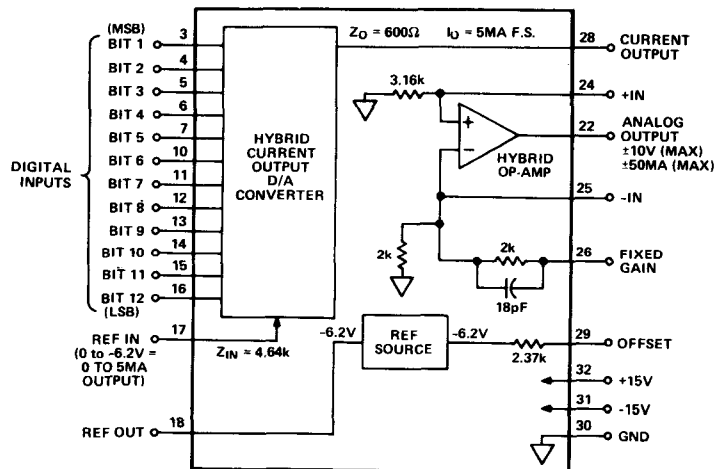
| PIN | FUNCTION          | PIN | FUNCTION         |
|-----|-------------------|-----|------------------|
| 3   | BIT 1 INPUT (MSB) | 17  | REFERENCE INPUT  |
| 4   | BIT 2 INPUT       | 18  | REFERENCE OUTPUT |
| 5   | BIT 3 INPUT       | 22  | ANALOG OUTPUT    |
| 6   | BIT 4 INPUT       | 24  | +INPUT           |
| 7   | BIT 5 INPUT       | 25  | -INPUT           |
| 10  | BIT 6 INPUT       | 26  | FIXED GAIN       |
| 11  | BIT 7 INPUT       | 28  | CURRENT OUTPUT   |
| 12  | BIT 8 INPUT       | 29  | OFFSET           |
| 13  | BIT 9 INPUT       | 30  | GROUND           |
| 14  | BIT 10 INPUT      | 31  | -15V POWER INPUT |
| 15  | BIT 11 INPUT      | 32  | +15V POWER INPUT |
| 16  | BIT 12 INPUT      |     |                  |



**MDS and MDSE Block Diagram**



**MDS-1240 and MDL Series Block Diagram**



**MDH Series Block Diagram**

(continued from page 191S)

Each D/A is housed in industry standard size cases, and each has an internal precision reference. Bipolar operation is achieved by external pin interconnection. In normal circumstances, no external components are required for operation into low impedance loads. Designed primarily for PCB mounting, these D/A's may also be plugged into standard DIL sockets mounted on 1.8" centers (MDS series 2" centers).

For ultra-high reliability, this D/A series is optionally available with burn-in extended beyond the Analog Devices standard of 96 hours at +25°C.

#### NOTES ON FAST-SETTLING D/A CONVERTERS

Invariably, fast-settling D/A converters use current rather than voltage switching.

There are inherent advantages to current-switching converters, since it eliminates an output amplifier. If there is no output amplifier, there is no slew rate limitation which slows settling. The absence of an output amplifier also means there are no overshoot and ringing problems often associated with feedback amplifiers.

The settling time of a current-switching D/A converter, then, is based on:

1. The RC time constant of the converter output.
2. The settling time of the output current change.

If the settling time of the D/A converter under consideration is determined by the RC time constant, the output capacitance and output impedance become very important.

As a typical example in the Analog Devices' D/A converters, output capacitance is 5pF, and nominal output impedance is 165Ω.

For test purposes, the output of these D/A converters are loaded with approximately 150Ω. (There is no "trick" or "gimmick" in loading the output of the converter; it is done to provide an output voltage of approximately 1.0V to 1.2V.) This loading means  $RC = 80 \times 5 \times 10^{-12} = 0.4\text{ns}$ . Since settling time is approximately 7 RC, the overall settling time, if determined by the RC time constant, would be 2.8ns.

Based on this, it becomes obvious the RC time constant of such converters outputs is not the limiting factor in establishing settling time. Instead, the settling time of the converters is based primarily on the settling time of the overall (output) current change, since the effect of the RC time constant is "swamped." Expressed in another way, this means settling time for the MDS series converters is relatively independent of load resistance, unless substantial load capacitance is present. The settling time of the output current, in turn, is based on:

1. The settling time of each switch within the converter.
2. The time skew among the digital inputs which cause the switching action.

Some manufacturers of fast-settling D/A converters spec settling time under the conditions of all digital inputs changing from "0" to "1", or vice versa. At first glance, it would appear this is the "worst case" condition for measuring settling time, since maximum current is being switched.

Unfortunately, this method of specifying neglects an important characteristic of saturated logic... the propagation delay for negative-going inputs is different from the delay for positive-

going inputs on all forms of saturated logic. The TTL or DTL driving logic, and the D/A input circuits for current-switching D/A's are subject to this same characteristic.

Thus, the time skew of the individual current switches within the converter is worse when one or more input bits are out of phase with the others. This is true even for ideal inputs in which the digital inputs arrive simultaneously; if there is time skew among the bit inputs, of course, the problem becomes more pronounced.

Note, settling times even better than those specified for the MDS series become possible if digital input bit arrivals are deskewed.

These differences among the switches cause a discontinuity or "glitch" in the output. The true "worst case" glitch always occurs at the switching point of the Most Significant Bit or the center point of the output range, because nearly equal and opposite currents are being switched within the converter.

In addition, all "0" to all "1" switching overlooks the practical aspects involved. There are relatively few times when all of the input bits will be changing from one state to the other on successive input changes; however, the MSB will switch out of phase with all other bits each time the analog output of the converter crosses the midpoint.

In considering the choice of a "fast-settling" D/A converter, then, the user should look for the following points in the data sheet:

1. If the settling time spec has all bits changing state identically, it neglects the phenomenon associated with saturated logic discussed earlier.
2. Is the settling time specified with an impractically-low-impedance load?

If the RC time constant of the converter output is the major factor in establishing settling time (because of high output capacitance and/or resistance), a low impedance load helps make settling time look better.

A low impedance load means the voltage being developed at the output is oftentimes too small to be useful.

A higher-impedance load which can develop a useable output of 1.0V or more sometimes negates the fast settling time of the spec sheet.

A test setup for this worst-case measurement is shown in Figure 1. Two pulse generators are used to generate the required out-of-phase pulses, and the delays are adjusted for minimum skew. Figure 2 is an unretouched photo of the oscilloscope trace of an MDS-815 under test.

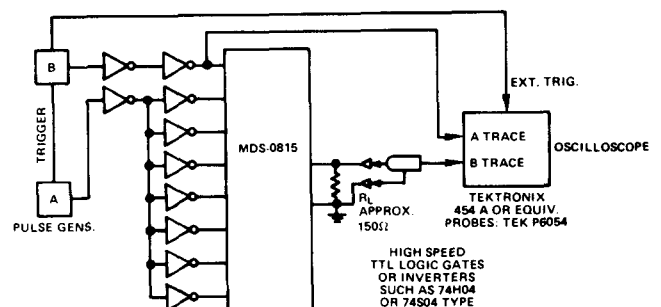


Figure 1.



| ANALOG OUTPUT<br>BIPOLAR, NONINVERTING | OFFSET BINARY     |
|--|-------------------|
| +FS, -1LSB                             | 1 1 1 . . . . . 1 |
| +1/2 FS                                | 1 1 0 . . . . . 0 |
| 0                                      | 1 0 0 . . . . . 0 |
| -1/2 FS                                | 0 1 0 . . . . . 0 |
| -FS                                    | 0 0 0 . . . . . 0 |

| ANALOG OUTPUT<br>UNIPOLAR, NONINVERTING | STRAIGHT BINARY   |
|---|-------------------|
| +FS, -1LSB                              | 1 1 1 . . . . . 1 |
| +3/4 FS                                 | 1 1 0 . . . . . 0 |
| +1/2 FS                                 | 1 0 0 . . . . . 0 |
| +1/4 FS                                 | 0 1 0 . . . . . 0 |
| 0                                       | 0 0 0 . . . . . 0 |

Table 2. Input Coding

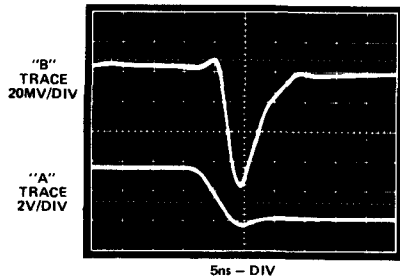


Figure 2.

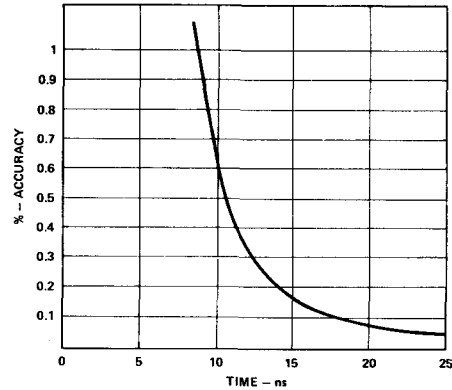


Figure 6. Accuracy vs. Time – MDS and MDSE

INTERNAL CURRENT DAC CHARACTERISTICS

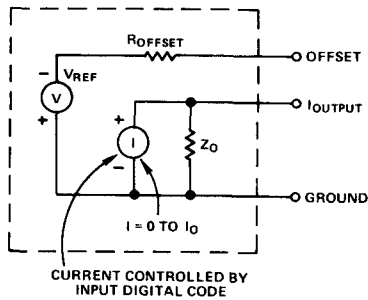


Figure 3. Current Equivalent Circuit

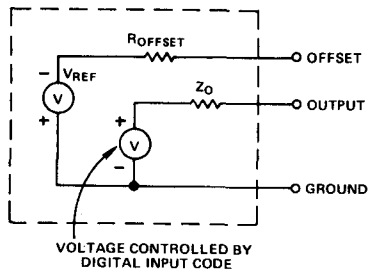


Figure 4. Voltage Equivalent Circuit

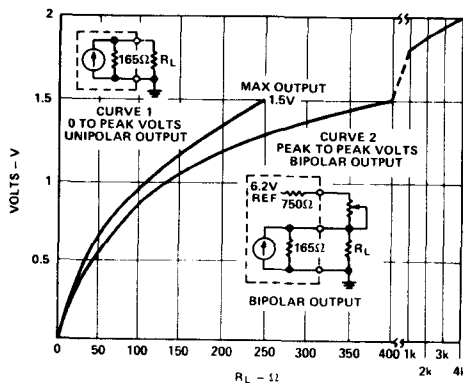


Figure 5.  $V_{OUT}$  vs. Load Resistance  
MDS-0815, -1020

BASIC CONNECTIONS AND CALIBRATIONS  
MDS/MDSE-0815, 1020

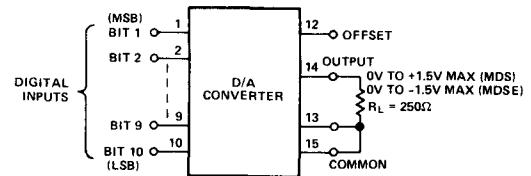


Figure 7. Unipolar Output Current

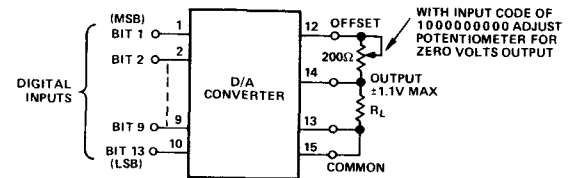
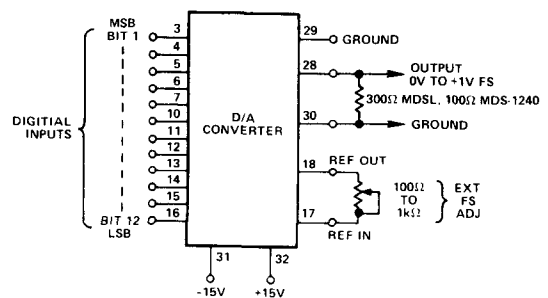


Figure 8. Bipolar Output Current

MDS-1240, MDSL-0825, 1035, 1250

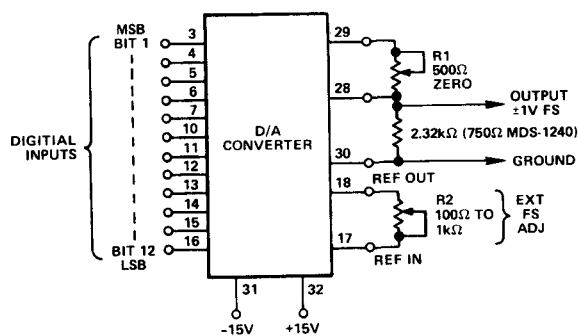


The 100Ω POTENTIOMETER MAY BE OMITTED IF ABSOLUTE ACCURACY OF FULL SCALE IS NOT REQUIRED. IN THIS CASE PINS 17 AND 18 SHOULD BE SHORTED AND THE FULL SCALE CURRENT WILL BE 5.1mA ±5% (MDS-1240, 10.2mA ±5%)

Figure 9. Unipolar Current Output

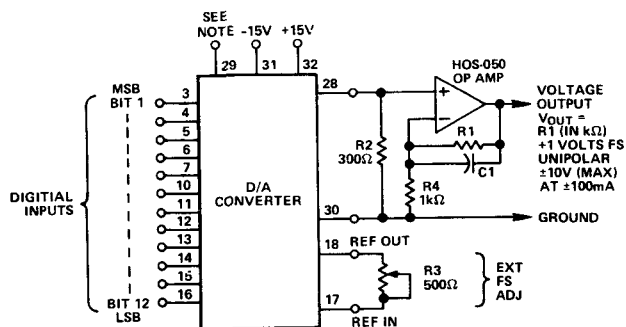
(MDS-1240, MDSL-0825, 1035, 1250 continued)

MDSL



**CALIBRATION PROCEDURE**  
 WITH INPUT CODE 000000000000  
 ADJUST THE 500Ω (R1) POTENTIOMETER  
 FOR -1.0000 VOLTS OUTPUT. WITH  
 INPUT CODE 111111111111 ADJUST  
 THE 100Ω (R2) POTENTIOMETER FOR  
 +0.99976 VOLTS OUTPUT.

Figure 10. Bipolar Current Output



**NOTES:**  
 1. CIRCUIT SHOWN FOR UNIPOLAR POSITIVE OUTPUT. OUTPUT SETTLING TIME IS APPROXIMATELY 150ns.  
 2. FOR 0 TO +10V OUTPUT R2 = 300Ω, R1 = 9kΩ.  
 3. R3 IS ADJUSTED FOR DESIRED OUTPUT. RANGE IS APPROXIMATELY +5%.  
 4. FOR BIPOLAR OUTPUT CONNECT 500Ω POTENTIOMETER BETWEEN PINS 29 AND 28 AND UNGROUND PIN 29. R2 IS SET TO 2.32kΩ, AND Vout (p-p) = 2 (R1 (IN kΩ) + 1).  
 5. C1 IS APPROXIMATELY 10pF AND MAY BE ADJUSTED FOR BEST TRANSIENT RESPONSE.

Figure 13. Noninverting Unipolar or Bipolar Voltage Output

VOLTAGE OUTPUT  
 MDS/MDSE-815, 1040

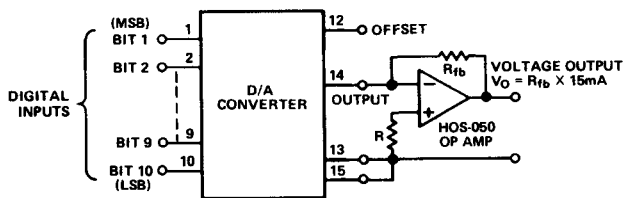
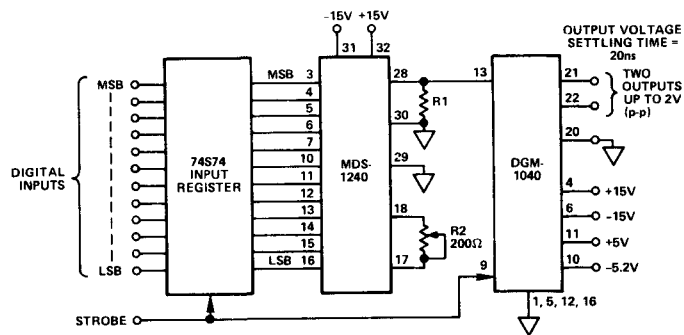


Figure 11. Voltage Output

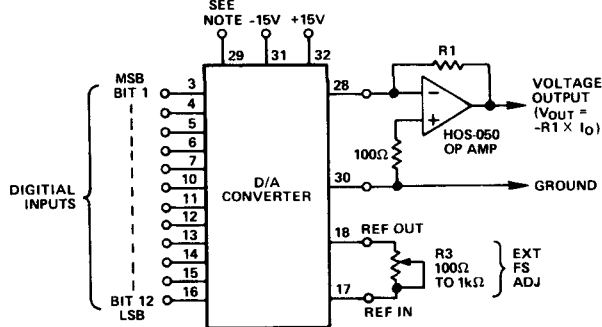
APPLICATIONS



**NOTES ON DEGLITCHED D/A:**  
 1. CONSULT DGM DATA SHEET FOR DEGLITCH CIRCUIT DETAILS.  
 2. R1 IS VARIED TO OBTAIN DESIRED OUTPUT LEVEL: FOR 0 TO +1V OUTPUT, R1 = 100Ω.

Figure 14. Ultra High-Speed Deglitched D/A

MDS-1240, MDSL (all)

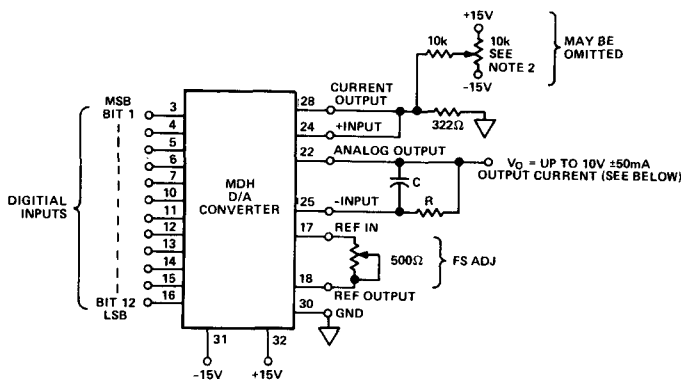


**NOTE:**  
 FOR UNIPOLAR VOLTAGE OUTPUT CONNECT JUMPER BETWEEN PINS 29 AND 30. FOR BIPOLAR VOLTAGE OUTPUT CONNECT A 500Ω POTENTIOMETER BETWEEN PINS 28 AND 29 AND ADJUST FOR ZERO OUTPUT WITH 100000000000 INPUT.

Figure 12. Inverting Unipolar or Bipolar Voltage Output

## MDH SERIES APPLICATIONS

By using external feedback resistor and capacitor as shown in Figures 15 and 16, other full scale output ranges from 2V to 10V may be obtained.

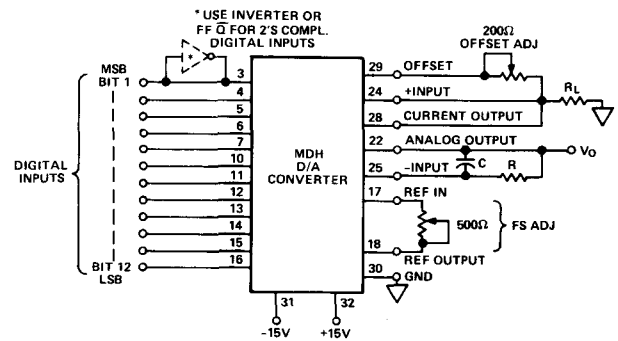


**NOTES:**

1. VALUE OF C IS APPROXIMATE. A FIXED CAPACITOR WITH TOLERANCE OF  $\pm 1\text{pF}$  MAY BE USED IF 50% DEGRADATION OF SETTLING TIME IS PERMITTED. IF SETTLING TIME IS TO BE OPTIMIZED, AN ADJUSTABLE CAPACITOR SHOULD BE USED FOR C AND ADJUSTED FOR MINIMUM SETTLING TIME.
2. OFFSET NULLING MAY BE ACCOMPLISHED BY CONNECTING A 10k POTENTIOMETER BETWEEN +15V AND -15V, AND CONNECTING ITS ADJUSTABLE TAP TO A 10k RESISTOR, THE OTHER END OF THE RESISTOR IS CONNECTED TO PIN 28. TYPICAL UNCOMPENSATED OFFSET IS 1% OF FULL SCALE.

| VOLTAGE OUTPUT | SETTLING TIME | OFFSET TEMPCO                   | R   | C     |
|----------------|---------------|---------------------------------|-----|-------|
| 0 to +2V       | 70ns          | $100\mu\text{V}/^\circ\text{C}$ | 2k  | 10pF  |
| 0 to +5V       | 100ns         | $250\mu\text{V}/^\circ\text{C}$ | 8k  | 2pF   |
| 0 to +10V      | 200ns         | $500\mu\text{V}/^\circ\text{C}$ | 18k | 0.5pF |

Figure 15. Binary Coding Unipolar Output Configuration



**NOTES:**

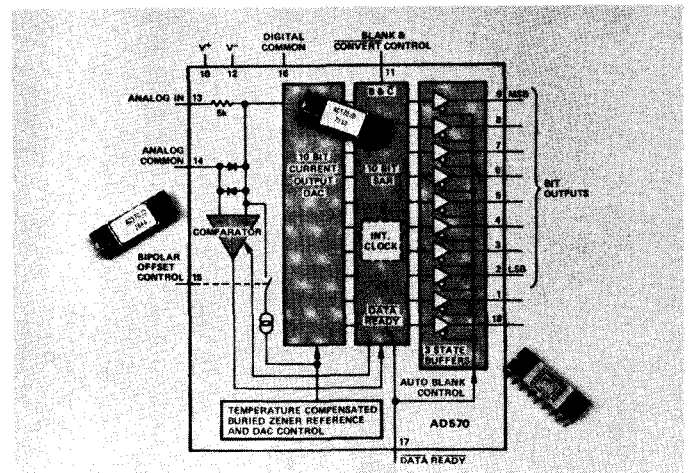
1. THE 200Ω POTENTIOMETER IS ADJUSTED FOR AN OUTPUT OF -FS WITH ALL ZEROES IN THE DIGITAL INPUT.
2. THE 500Ω POTENTIOMETER IS ADJUSTED FOR AN OUTPUT OF +FS-1LSB WITH ALL ONE'S IN THE DIGITAL INPUT.
3. FOR TWO'S COMPLEMENT (2SC) OPERATION, AN EXTERNAL INVERTER MUST BE USED TO COMPLEMENT BIT 1 (MSB).
4. AN ADJUSTABLE CAPACITOR MAY BE USED FOR C AND ADJUSTED TO OPTIMIZE SETTLING TIME.

| VOLTAGE OUTPUT   | SETTLING TIME | OFFSET TEMPCO                   | R <sub>L</sub> | C     | R   |
|------------------|---------------|---------------------------------|----------------|-------|-----|
| $\pm 1\text{V}$  | 70ns          | $100\mu\text{V}/^\circ\text{C}$ | 383            | 10pF  | 2k  |
| $\pm 2\text{V}$  | 100ns         | $200\mu\text{V}/^\circ\text{C}$ | 383            | 2pF   | 6k  |
| $\pm 5\text{V}$  | 100ns         | $250\mu\text{V}/^\circ\text{C}$ | 9.1k           | 2pF   | 8k  |
| $\pm 10\text{V}$ | 200ns         | $500\mu\text{V}/^\circ\text{C}$ | 9.1k           | 0.5pF | 18k |

Figure 16. Offset Binary Coding or 2's Comp Coding Bipolar Output Configuration

### FEATURES

Complete A/D Converter with Reference and Clock  
Fast Successive Approximation Conversion –  $25\mu\text{s}$   
No Missing Codes Over Temperature  
0 to  $+70^\circ\text{C}$  – AD570J  
 $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  – AD570S  
Digital Multiplexing – 3 State Outputs  
18 Pin Ceramic DIP  
Low Cost Monolithic Construction



### PRODUCT DESCRIPTION

The AD570 is an 8-bit successive approximation A/D converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers – all fabricated on a single chip. No external components are required to perform a full accuracy 8-bit conversion in  $25\mu\text{s}$ .

The AD570 incorporates the most advanced integrated circuit design and processing technology available today.  $I^2L$  (integrated injection logic) processing in the fabrication of the SAR function along with laser trimming of the high stability SiCr thin film resistor ladder network at the wafer stage (LWT) and a temperature compensated, subsurface Zener reference insures full 8-bit accuracy at low cost.

Operating on supplies of  $+5\text{V}$  and  $-15\text{V}$ , the AD570 will accept analog inputs of 0 to  $+10\text{V}$  unipolar or  $\pm 5\text{V}$  bipolar, externally selectable. As the BLANK and CONVERT input is driven low, the three state outputs will be open and a conversion will commence. Upon completion of the conversion, the  $\overline{\text{DATA READY}}$  line will go low and the data will appear at the output. Pulling the BLANK and CONVERT input high blanks the outputs and readies the device for the next conversion. The AD570 executes a true 8-bit conversion with no missing codes in approximately  $25\mu\text{s}$ .

The AD570 is available in two versions; the AD570J is specified for the 0 to  $70^\circ\text{C}$  temperature range, the AD570S for  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ . Both guarantee full 8-bit accuracy and no missing codes over their respective temperature ranges and are packaged in 18-pin hermetically-sealed ceramic DIP's.

### PRODUCT HIGHLIGHTS

1. The AD570 is a complete 8-bit A/D converter. No external components are required to perform a conversion. Full scale calibration accuracy of  $\pm 0.8\%$  (2LSB of 8 bits) is achieved without external trims.
2. The AD570 is a single chip device employing the most advanced IC processing techniques. Thus, the user has at his disposal a truly precision component with the reliability and low cost inherent in monolithic construction.
3. The AD570 accepts either unipolar (0 to  $+10\text{V}$ ) or bipolar ( $-5\text{V}$  to  $+5\text{V}$ ) analog inputs by simply grounding or opening a single pin.
4. The device offers true 8-bit accuracy and exhibits no missing codes over its entire operating temperature range.
5. Operation is guaranteed with  $-15\text{V}$  and  $+5\text{V}$  supplies. The device will also operate with a  $-12\text{V}$  supply.
6. The AD570S is also available with full processing to MIL-STD-883B, Class B. The single chip construction and functional completeness make the AD570 especially attractive for high reliability applications.
7. Every AD570 is subjected to long-term stabilization bakes, given a powered burn-in at  $+125^\circ\text{C}$ , and temperature cycled ten times from  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$  prior to final test to insure reliability and long-term stability. In addition, all units are tested 100% at the extremes of their respective temperature ranges for all parameters to guarantee full performance.

\*Covered by Patent No. 3,940,760, other patents pending.

# SPECIFICATIONS

(typical @ +25°C with V+ = +5V, V- = -15V, all voltages measured with respect to digital common, unless otherwise indicated)

| MODEL  | AD570JD                          | AD570SD/AD570SD-883B <sup>1</sup> |
|--|----------------------------------|-----------------------------------|
| RESOLUTION <sup>2</sup>  | 8 Bits                           | *                                 |
| RELATIVE ACCURACY @ 25°C <sup>2,3,4</sup>  | ±1/2LSB max                      | *                                 |
| T <sub>min</sub> to T <sub>max</sub>   | ±1/2LSB max                      | *                                 |
| FULL SCALE CALIBRATION <sup>4,5</sup><br>(With 15Ω Resistor In Series With<br>Analog Input)                              | ±2LSB (typ)                      | *                                 |
| UNIPOLAR OFFSET (max) <sup>4</sup>   | ±1/2LSB                          | *                                 |
| BIPOLAR OFFSET (max) <sup>4</sup>  | ±1/2LSB                          | *                                 |
| DIFFERENTIAL NONLINEARITY<br>(Resolution for Which no Missing<br>Codes are Guaranteed)                                   |                                  |                                   |
| +25°C  | 8 Bits                           | *                                 |
| T <sub>min</sub> to T <sub>max</sub>   | 8 Bits                           | *                                 |
| TEMPERATURE RANGE  | 0 to +70°C                       | -55°C to +125°C                   |
| TEMPERATURE COEFFICIENTS <sup>4</sup><br>Guaranteed max Change   |                                  |                                   |
| T <sub>min</sub> to T <sub>max</sub>   |                                  |                                   |
| Unipolar Offset  | ±1LSB (88ppm/°C)                 | ±1LSB (40ppm/°C)                  |
| Bipolar Offset   | ±1LSB (88ppm/°C)                 | ±1LSB (40ppm/°C)                  |
| Full Scale Calibration <sup>6</sup><br>(With 15Ω Fixed Resistor or<br>200Ω Trimmer)                                      | ±2LSB (176ppm/°C)                | ±2LSB (80ppm/°C)                  |
| POWER SUPPLY REJECTION <sup>4</sup><br>Max Change In Full Scale Calibration  |                                  |                                   |
| TTL Positive Supply<br>+4.5V ≤ V+ ≤ +5.5V  | ±2LSB max                        | *                                 |
| Negative Supply<br>-16.5V ≤ V- ≤ -13.5V  | ±2LSB max                        | *                                 |
| ANALOG INPUT RESISTANCE  | 3kΩ min<br>5kΩ typ<br>7kΩ max    | *<br>*<br>*                       |
| ANALOG INPUT RANGES<br>(Analog Input to Analog Common)   |                                  |                                   |
| Unipolar   | 0 to +10V                        | *                                 |
| Bipolar  | -5V to +5V                       | *                                 |
| OUTPUT CODING  |                                  |                                   |
| Unipolar   | Positive True Binary             | *                                 |
| Bipolar  | Positive True Offset Binary      | *                                 |
| LOGIC OUTPUT   |                                  |                                   |
| Bit Outputs and Data Ready   |                                  |                                   |
| Output Sink Current<br>(V <sub>OUT</sub> = 0.4V max, T <sub>min</sub> to T <sub>max</sub> )                              | 3.2mA min<br>(2TTL Loads)        | *<br>*                            |
| Output Source Current (Bit Outputs) <sup>7</sup><br>(V <sub>OUT</sub> = 2.4V min, T <sub>min</sub> to T <sub>max</sub> ) | 0.5mA min                        | *                                 |
| Output Leakage When Blanked  | ±40μA max                        | *                                 |
| LOGIC INPUT  |                                  |                                   |
| Blank and Convert Input<br>0 ≤ V <sub>in</sub> ≤ V+  | ±40μA max                        | *                                 |
| Blank – Logic “1”  | 2.0V min                         | *                                 |
| Convert – Logic “0”  | 0.8V max                         | *                                 |
| CONVERSION TIME  | 15μs min<br>25μs typ<br>40μs max | *<br>*<br>*                       |

| MODEL                                   | AD570JD            | AD570SD/AD570SD-883B <sup>1</sup> |
|---|--------------------|-----------------------------------|
| <b>POWER SUPPLY</b>                     |                    |                                   |
| Absolute Maximum                        |                    |                                   |
| V+                                      | +7V                | *                                 |
| V-                                      | -16.5V             | *                                 |
| Specified Operating — Rated Performance |                    |                                   |
| V+                                      | +5V                | *                                 |
| V-                                      | -15V               | *                                 |
| Operating Range                         |                    |                                   |
| V+                                      | +4.5V to +5.5V     | *                                 |
| V-                                      | -12.0V to -16.5V   | *                                 |
| Operating Current                       |                    |                                   |
| Blank Mode                              |                    |                                   |
| V+ = +5V                                | 2mA typ (10mA max) | *                                 |
| V- = -15V                               | 9mA typ (15mA max) | *                                 |
| Convert Mode                            |                    |                                   |
| V+ = +5V                                | 5mA                | *                                 |
| V- = -15V                               | 10mA               | *                                 |

\*Specifications same as AD570J

Specifications subject to change without notice.

**NOTES:**

<sup>1</sup> The AD570S is available fully processed and screened to the requirements of MIL-STD-883B, Class B. A complete list of tests is given on page 204S. When ordering, specify the AD570SD/883B.

<sup>2</sup> The AD570 is a selected version of the AD571 10-bit A to D converter. As such, some devices may exhibit 9 or 10 bits of relative accuracy or resolution, but that is neither tested nor guaranteed. Only TTL logic inputs should be connected to pins 1 and 18 (or no connection made) or damage may result.

<sup>3</sup> Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

<sup>4</sup> Specifications given in LSB's refer to the weight of a least significant bit at the 8-bit level, which is 0.39% of full-scale.

<sup>5</sup> Full scale calibration is guaranteed trimmable to zero with an external 200Ω potentiometer in place of the 15Ω fixed resistor. Full scale is defined as 10 volts minus 1 LSB, or 9.961 volts.

<sup>6</sup> Full Scale Calibration Temperature Coefficient includes effects of unipolar offset drift as well as gain drift.

<sup>7</sup> The Data output lines have active pull-ups to source 0.5mA. The DATA READY line is open collector with a nominal 6kΩ internal pull-up resistor.

**ABSOLUTE MAXIMUM RATINGS**

|                                 |              |
|---------------------------------|--------------|
| V+ to Digital Common            | .0 to +7V    |
| V- to Digital Common            | .0 to -16.5V |
| Analog Common to Digital Common | ±1V          |
| Analog Input to Analog Common   | ±15V         |
| Control Inputs                  | 0 to V+      |
| Digital Outputs (Blank Mode)    | 0 to V+      |
| Power Dissipation               | 800mW        |

**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

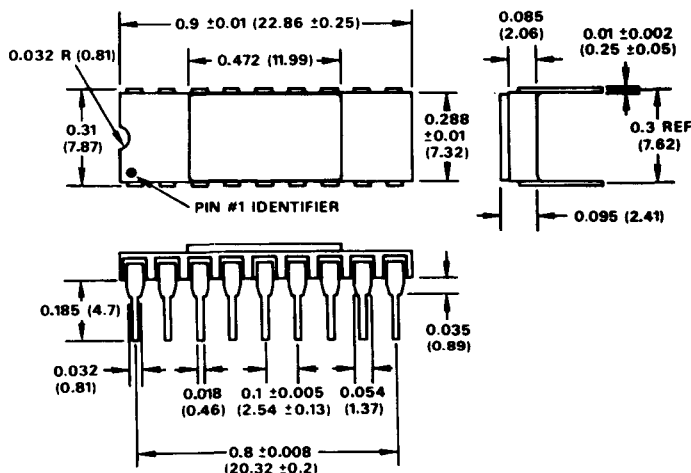
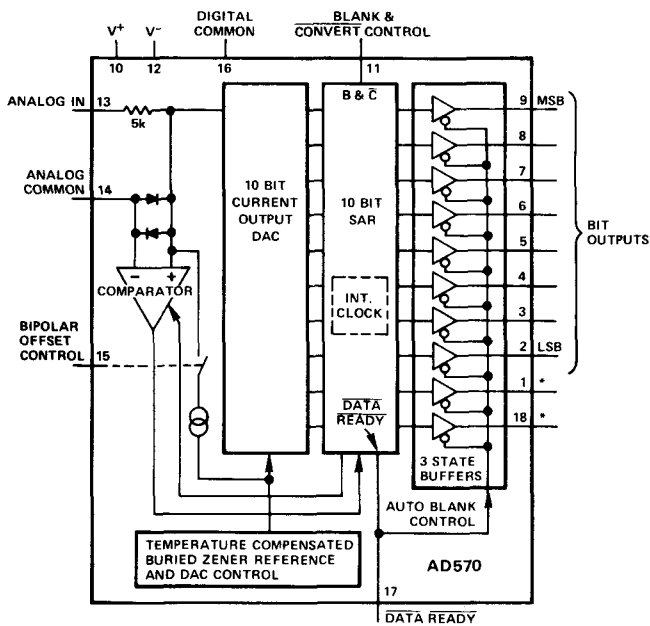


Figure 1. 18-Lead Ceramic Dual-In-Line Package

## CIRCUIT DESCRIPTION

The AD570 is a complete 8-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD570 is shown in Figure 2. Upon receipt of the CONVERT command, the internal 8-bit current output DAC is sequenced by the  $I^2L$  successive-approximation register (SAR) from its most-significant bit (MSB) to least-significant bit (LSB) to provide an output current which accurately balances the input signal current through the  $5k\Omega$  input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less the bit is left on, if more, the bit is turned off. After testing all the bits, the SAR contains a 8-bit binary code which accurately represents the input signal to within  $\pm 1/2LSB$  (0.20%).

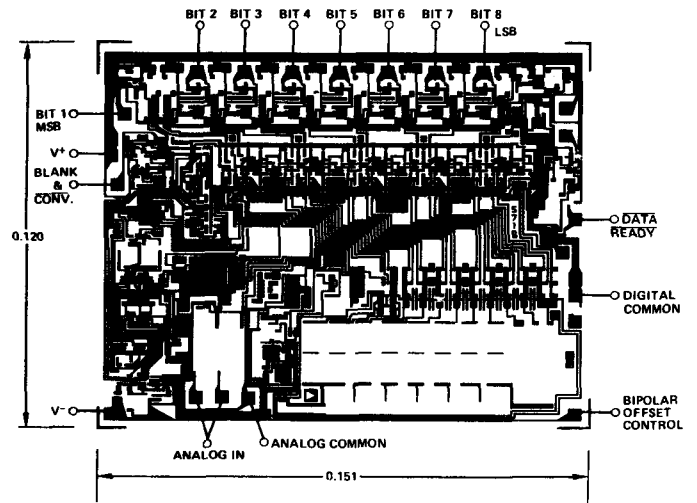


\*SEE NOTE 2, PAGE 3

Figure 2. AD570 Functional Block Diagram

Upon completion of the sequence, the SAR sends out a DATA READY signal (active low), which also brings the three-state buffers out of their "open" state, making the bit output lines become active high or low, depending on the code in the SAR. When the BLANK and CONVERT line is brought high, the output buffers again go "open", and the SAR is prepared for another conversion cycle. Details of the timing are given on page 205S.

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of



THE AD570 IS ALSO AVAILABLE IN A LASER-TRIMMED PASSIVATED CHIP FORM. CONSULT FACTORY FOR PRICING AND APPLICATION PARTICULARS. FIGURE 3 SHOWS THE CHIP METALLIZATION LAYOUT AND BONDING PADS.

Figure 3. Chip Bonding Diagram

the MSB less  $\frac{1}{2}LSB$ ) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 to +10V unipolar input range becomes a -5V to +5V range. The  $5k\Omega$  thin film input resistor is trimmed so that with a full scale input signal, an input current will be generated which exactly matches the DAC output with all bits on. (The input resistor is trimmed slightly low to facilitate user trimming, as discussed on the next page.)

## POWER SUPPLY SELECTION

The AD570 is designed and specified for optimum performance using a +5V and -15V supply. The supply current drawn by the device is a function of the operating mode (BLANK or CONVERT), as given on the specification page. The supply currents change only moderately over temperature as shown in Figure 4, and do not change significantly with changes in  $V^-$  from -10.8 volts to -16 volts.

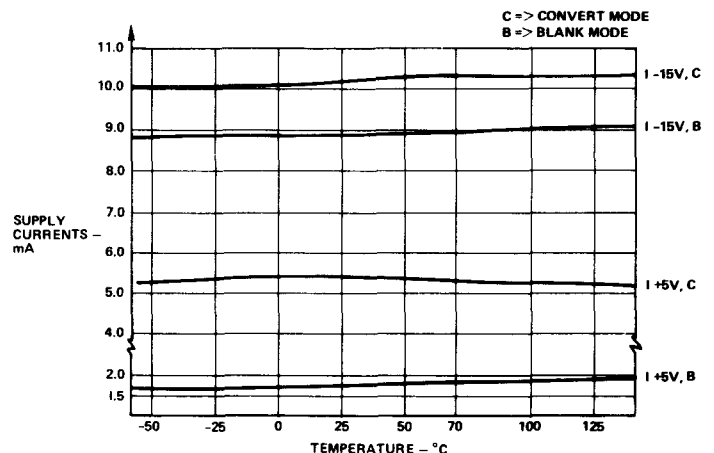


Figure 4. AD570 Power Supply Current vs. Temperature

## CONNECTING THE AD570 FOR STANDARD OPERATION

The AD570 contains all the active components required to perform a complete A/D conversion. Thus, for most situations, all that is necessary is connection of the power supply (+5 and -15), the analog input, and the conversion start pulse. But, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 5.

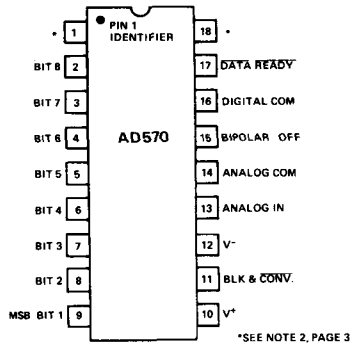


Figure 5. AD570 Pin Connections

## FULL SCALE CALIBRATION

The 5kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC—plus about 0.3%—when a full scale analog input voltage of 9.961 volts (10 volts - 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.961 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 13. Typical full scale calibration error will then be about ±2LSB or ±0.8%. If a more precise calibration is desired, a 200Ω trimmer should be used instead. Set the analog input at 9.961 volts, and set the trimmer so that the output code is just at the transition between 11111110 and 11111111. Each LSB will then have a weight of 39.06mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have weight of exactly 40.00mV), a 50Ω resistor in series with a 200Ω trimmer (or a 500Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ.

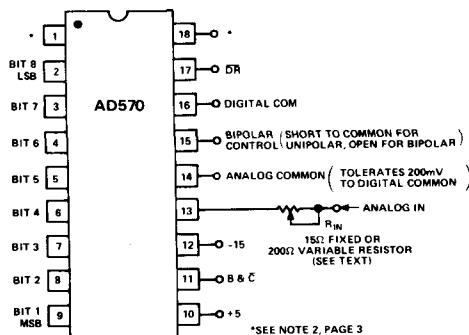


Figure 6. Standard AD570 Connections

## BIPOLAR OPERATION

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin to digital common. If the pin is left open, the bipolar offset current will be switched into the comparator summing node, giving a -5V to +5V range with an offset binary output code. (-5.00 volts in will give a 8-bit code of 00000000; an input of 0.00 volts results in an output code of 10000000 and 4.96 volts at the input yields the 11111111 code.) The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 7.

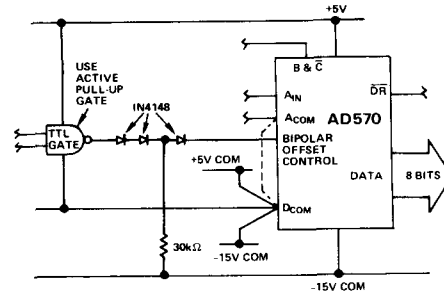


Figure 7. Bipolar Offset Controlled by Logic Gate

Gate Output = 1 Unipolar 0 - 10V Input Range  
Gate Output = 0 Bipolar ±5V Input Range

## COMMON MODE RANGE

The AD570 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common mode range between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition, a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. An additional 1mA will flow in during a blank interval with zero analog input. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum differential voltage rating between the two commons is ±1 volt. We recommend the connection of a parallel pair of back-to-back protection diodes as shown in Figure 8 between the commons if they are not connected locally.

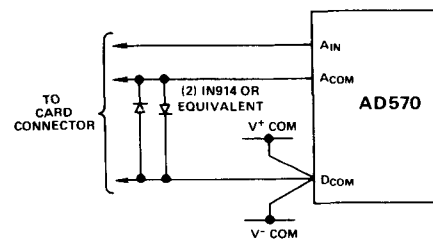


Figure 8. Differential Common Voltage Protection



## ZERO OFFSET

The apparent zero point of the AD570 can be adjusted by inserting an offset voltage between the Analog Common of the device and the actual signal return or signal common. Figure 9 illustrates two methods of providing this offset. Figure 9A shows how the converter zero may be offset by up to  $\pm 3$  bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.

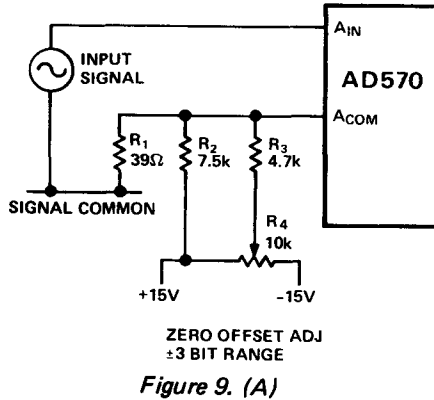


Figure 9. (A)

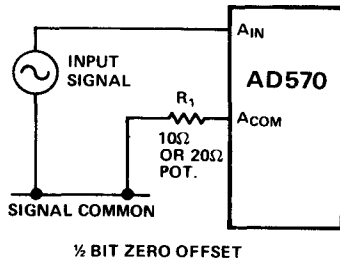
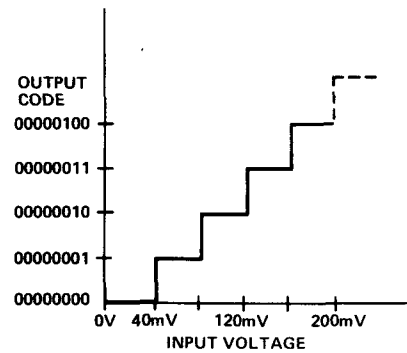


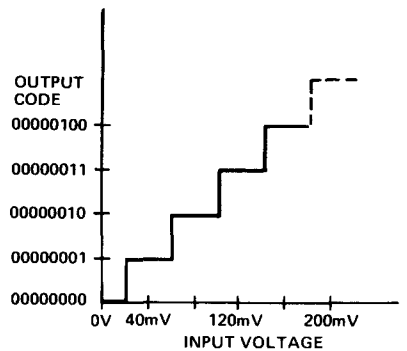
Figure 9. (B)

Figure 10 shows the nominal transfer curve near zero for an AD570 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics. This offset can easily be accomplished as shown in Figure 9B. At balance (after a conversion) approximately 2mA flows into the Analog Common terminal. A  $10\Omega$  resistor in series with this terminal will result in approximately the desired  $\frac{1}{2}$  bit offset of the transfer characteristics. The nominal 2mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a  $20\Omega$  potentiometer (connected as a rheostat) can be used as R2. Additional negative offset range may be obtained by using larger values of R2. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of  $\frac{1}{2}$  LSB is introduced, full scale trimming as described on previous page should be done with an analog input of 9.941 volts.

**NOTE:** During a conversion transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle as appropriate during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling which returns to analog signal common should go to the signal input side of the resistive offset network.



NOMINAL CHARACTERISTICS REFERRED TO ANALOG COMMON



OFFSET CHARACTERISTICS WITH  $10\Omega$  IN SERIES WITH ANALOG COMMON

Figure 10. AD570 Transfer Curve - Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights  $\sim 36.1mV$ )

## MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD570, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further insure reliability, the AD570 is offered with 100% screening to MIL-STD-883B, method 5004.

Table I details the test procedures of MIL-STD-883. Analog Devices subjects each part ordered with 883B screening to these tests on a 100% basis.

TABLE I

| TEST                         | METHOD  |
|------------------------------|---|
| 1) Internal Visual (Pre cap) | 2010, Test Condition B  |
| 2) Stabilization Bake        | Method 1008, 24 hours @ $+150^{\circ}C$                                     |
| 3) Temperature Cycling       | Method 1010, Test Condition C, 10 Cycles, $-65^{\circ}C$ to $+150^{\circ}C$ |
| 4) Constant Acceleration     | Method 2001, Test Condition E, Y1 plane, 30kg                               |
| 5) Seal, Fine and Gross      | Method 1014, Test Condition B and C   |
| 6) Burn-in Test              | Method 1015, Test Condition B, 160 hours @ $+125^{\circ}C$ min              |
| 7) Final Electrical Tests    | Performed 100% to all min and max specifications on data pages.             |
| 8) External Visual           | Method 2009   |

## CONTROL AND TIMING OF THE AD570

There are several important timing and control features on the AD570 which must be understood precisely to allow optimal interfacing to microprocessor or other types of control systems. All of these features are shown in the timing diagram in Figure 11.

The normal stand-by situation is shown at the left end of the drawing. The  $\overline{\text{BLANK}}$  and  $\overline{\text{CONVERT}}$  (B &  $\overline{\text{C}}$ ) line is held high, the output lines will be "open", and the  $\overline{\text{DATA READY}}$  ( $\overline{\text{DR}}$ ) line will be high. This mode is the lowest power state of the device (typically 150mW). When the (B &  $\overline{\text{C}}$ ) line is brought low, the conversion cycle is initiated; but the  $\overline{\text{DR}}$  and Data lines do not change state. When the conversion cycle is complete (typically 25 $\mu\text{s}$ ), the  $\overline{\text{DR}}$  line goes low, and within 500ns, the Data lines become active with the new data.

About 1.5 $\mu\text{s}$  after the B &  $\overline{\text{C}}$  line is again brought high, the  $\overline{\text{DR}}$  line will go high and the Data lines will go open. When the B &  $\overline{\text{C}}$  line is again brought low, a new conversion will begin. The minimum pulse width for the B &  $\overline{\text{C}}$  line to blank previous data and start a new conversion is 2 $\mu\text{s}$ . If the B &  $\overline{\text{C}}$  line is brought high during a conversion, the conversion will stop, and the  $\overline{\text{DR}}$  and Data lines will not change. If a 2 $\mu\text{s}$  or longer pulse is applied to the B &  $\overline{\text{C}}$  line during a conversion, the converter will clear and start a new conversion cycle.

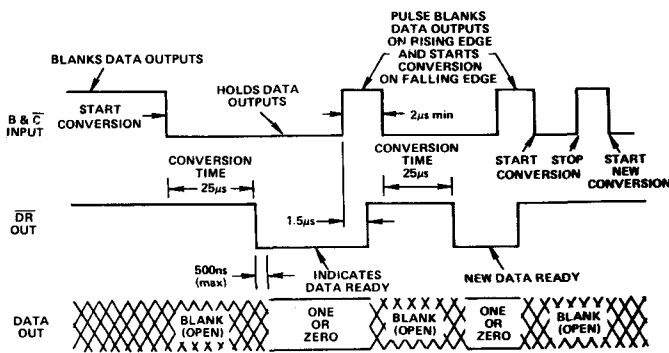


Figure 11. AD570 Timing and Control Sequence

## CONTROL MODES WITH $\overline{\text{BLANK}}$ AND $\overline{\text{CONVERT}}$

The timing sequence of the AD570 discussed above allows the device to be easily operated in a variety of systems with differing control modes. The two most common control modes, the Convert Pulse Mode, and the Multiplex Mode, are illustrated here.

**Convert Pulse Mode** — In this mode, data is present at the output of the converter at all times except when conversion is taking place. Figure 12 illustrates the timing of this mode. The  $\overline{\text{BLANK}}$  and  $\overline{\text{CONVERT}}$  line is normally low and conversions are triggered by a positive pulse. A typical application for this timing mode is shown in Figure 15, in which  $\mu\text{P}$  bus interfacing is easily accomplished with three-state buffers.

**Multiplex Mode** — In this mode the outputs are blanked except when the device is selected for conversion and readout; this timing shown in Figure 13. A typical AD570 multiplexing application is shown in Figure 16.

This operating mode allows multiple AD570 devices to drive common data lines. All  $\overline{\text{BLANK}}$  and  $\overline{\text{CONVERT}}$  lines are held high to keep the outputs blanked. A single AD570 is selected, its  $\overline{\text{BLANK}}$  and  $\overline{\text{CONVERT}}$  line is driven low and at the end of

conversion, which is indicated by  $\overline{\text{DATA READY}}$  going low, the conversion result will be present at the outputs. When this data has been read from the 8-bit bus,  $\overline{\text{BLANK}}$  and  $\overline{\text{CONVERT}}$  is restored to the blank mode to clear the data bus for other converters. When several AD570's are multiplexed in sequence, a new conversion may be started in one AD570 while data is being read from another. As long as the data is read and the first AD570 is cleared within 15 $\mu\text{s}$  after the start of conversion of the second AD570, no data overlap will occur.

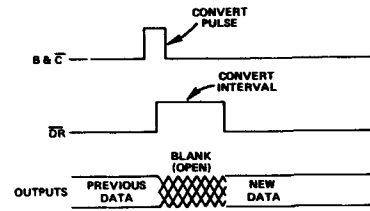


Figure 12. Convert Pulse Mode

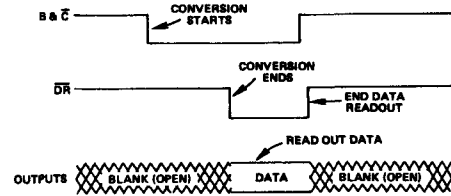


Figure 13. Multiplex Mode

## SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD570

Many situations in high-speed acquisition systems or digitizing of rapidly changing signals require a sample-and-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD570, a SHA can also serve as a high input impedance buffer.

Figure 14 shows the AD570 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10 $\mu\text{s}$  with a droop rate less than 100 $\mu\text{V}/\text{ms}$ . The control signals are arranged so that when the control line goes low, the AD582 is put into the "hold" mode, and the AD570 will begin its conversion cycle. (The AD582 settles to final value well in advance of the

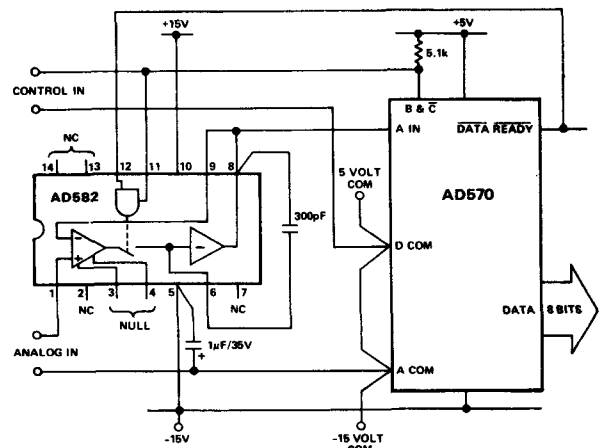


Figure 14. Sample-Hold Interface to the AD570





# SPECIFICATIONS

(typical @ +25°C with V+ = +5V, V- = -15V, all voltages measured with respect to digital common, unless otherwise indicated)

| MODEL  | AD571JD                          | AD571KD                    | AD571SD/AD571SD-883B <sup>5</sup> |
|--|----------------------------------|----------------------------|-----------------------------------|
| RESOLUTION   | 10 Bits                          | *                          | *                                 |
| RELATIVE ACCURACY @ 25°C <sup>1</sup><br>T <sub>min</sub> to T <sub>max</sub>  | ±1LSB max<br>±1LSB max           | ±1/2LSB max<br>±1/2LSB max | ±1LSB max<br>±1LSB max            |
| FULL SCALE CALIBRATION <sup>2</sup><br>(With 15Ω Resistor In Series With<br>Analog Input)                                | ±2LSB (typ)                      | *                          | *                                 |
| UNIPOLAR OFFSET (max)  | ±1LSB                            | ±1/2LSB                    | *                                 |
| BIPOLAR OFFSET (max)   | ±1LSB                            | ±1/2LSB                    | *                                 |
| DIFFERENTIAL NONLINEARITY<br>(Resolution for Which no Missing<br>Codes are Guaranteed)                                   |                                  |                            |                                   |
| +25°C  | 10 Bits                          | *                          | *                                 |
| T <sub>min</sub> to T <sub>max</sub>   | 9 Bits                           | 10 Bits                    | 10 Bits                           |
| TEMPERATURE RANGE  | 0 to +70°C                       | *                          | -55°C to +125°C                   |
| TEMPERATURE COEFFICIENTS<br>Guaranteed max Change<br>T <sub>min</sub> to T <sub>max</sub>                                |                                  |                            |                                   |
| Unipolar Offset  | ±2LSB (44ppm/°C)                 | ±1LSB (22ppm/°C)           | ±2LSB (20ppm/°C)                  |
| Bipolar Offset   | ±2LSB (44ppm/°C)                 | ±1LSB (22ppm/°C)           | ±2LSB (20ppm/°C)                  |
| Full Scale Calibration<br>(With 15Ω Fixed Resistor or<br>50Ω Trimmer)  | ±4LSB (88ppm/°C)                 | ±2LSB (44ppm/°C)           | ±5LSB (50ppm/°C)                  |
| POWER SUPPLY REJECTION<br>Max Change In Full Scale Calibration   |                                  |                            |                                   |
| CMOS Positive Supply (K only)<br>+13.5V ≤ V+ ≤ +16.5V  | N.A.                             | ±1LSB max                  | N.A.                              |
| TTL Positive Supply<br>+4.5V ≤ V+ ≤ +5.5V  | ±2LSB max                        | ±1LSB max                  | *                                 |
| Negative Supply<br>-16.5V ≤ V+ ≤ -13.5V  | ±2LSB max                        | ±1LSB max                  | *                                 |
| ANALOG INPUT RESISTANCE  | 3kΩ min<br>5kΩ typ<br>7kΩ max    | *                          | *                                 |
| ANALOG INPUT RANGES<br>(Analog Input to Analog Common)   |                                  |                            |                                   |
| Unipolar   | 0 to +10V                        | *                          | *                                 |
| Bipolar  | -5V to +5V                       | *                          | *                                 |
| OUTPUT CODING  |                                  |                            |                                   |
| Unipolar   | Positive True Binary             | *                          | *                                 |
| Bipolar  | Positive True Offset Binary      | *                          | *                                 |
| LOGIC OUTPUT <sup>3</sup><br>Bit Outputs and $\overline{\text{Data Ready}}$  |                                  |                            |                                   |
| Output Sink Current<br>(V <sub>OUT</sub> = 0.4V max, T <sub>min</sub> to T <sub>max</sub> ) <sup>4</sup>                 | 3.2mA min<br>(2TTL Loads)        | *                          | *                                 |
| Output Source Current (Bit Outputs) <sup>4</sup><br>(V <sub>OUT</sub> = 2.4V min, T <sub>min</sub> to T <sub>max</sub> ) | 0.5mA min                        | *                          | *                                 |
| Output Leakage When Blanked  | ±40μA max                        | *                          | *                                 |
| LOGIC INPUT  |                                  |                            |                                   |
| Blank and Convert Input<br>0 ≤ V <sub>in</sub> ≤ V+  | ±40μA max                        | *                          | *                                 |
| Blank – Logic “1”  | 2.0V min                         | *                          | *                                 |
| Convert – Logic “0”  | 0.8V max                         | *                          | *                                 |
| CONVERSION TIME  | 15μs min<br>25μs typ<br>30μs max | *                          | *                                 |

| MODEL                                   | AD571JD            | AD571KD         | AD571SD/AD571SD-883B <sup>5</sup> |
|---|--------------------|-----------------|-----------------------------------|
| <b>POWER SUPPLY</b>                     |                    |                 |                                   |
| Absolute Maximum                        |                    |                 |                                   |
| V+                                      | +7V                | +16.5V          | *                                 |
| V-                                      | -16.5V             | *               | *                                 |
| Specified Operating – Rated Performance |                    |                 |                                   |
| V+                                      | +5V                | +5V to +15V     | *                                 |
| V-                                      | -15V               | *               | *                                 |
| Operating Range                         |                    |                 |                                   |
| V+                                      | +4.5V to +5.5V     | +4.5V to +16.5V | *                                 |
| V-                                      | -12V to -16.5V     | *               | *                                 |
| Operating Current                       |                    |                 |                                   |
| Blank Mode                              |                    |                 |                                   |
| V+ = +5V                                | 2mA typ (10mA max) | *               | *                                 |
| V+ = +15V                               | 5mA typ (10mA max) | *               | *                                 |
| V- = -15V                               | 9mA typ (15mA max) | *               | *                                 |
| Convert Mode                            |                    |                 |                                   |
| V+ = +5V                                | 5mA                | *               | *                                 |
| V+ = +15V                               | 10mA               | *               | *                                 |
| V- = -15V                               | 10mA               | *               | *                                 |

\*Specifications same as AD571J

\*\*Specifications same as AD571K

Specifications subject to change without notice.

**NOTES:**

<sup>1</sup> Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

<sup>2</sup> Full scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω fixed resistor. Full scale is defined as 10 volts minus 1LSB, or 9.990 volts.

<sup>3</sup> Logic Input and Output Thresholds and Levels are a function of V+. They are guaranteed TTL compatible at V+ = +5V, CMOS compatible at V+ = 15V for the AD571K.

<sup>4</sup> The Data output lines have active pull-ups to source 0.5mA. The DATA READY line is open collector with a nominal 6kΩ internal pull-up resistor.

<sup>5</sup> The AD571S is available fully processed and screened to the requirements of MIL-STD-883A, Class B. A complete list of tests is given further. When ordering, specify the AD571SD-883B.

**ABSOLUTE MAXIMUM RATINGS**

|                                 |           |             |
|---------------------------------|-----------|-------------|
| V+ to Digital Common            | AD571J, S | 0 to +7V    |
|                                 | AD571K    | 0 to +16.5V |
| V- to Digital Common            |           | 0 to -16.5V |
| Analog Common to Digital Common |           | ±1V         |
| Analog Input to Analog Common   |           | ±15V        |
| Control Inputs                  |           | 0 to V+     |
| Digital Outputs (Blank Mode)    |           | 0 to V+     |
| Power Dissipation               |           | 800mW       |

**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

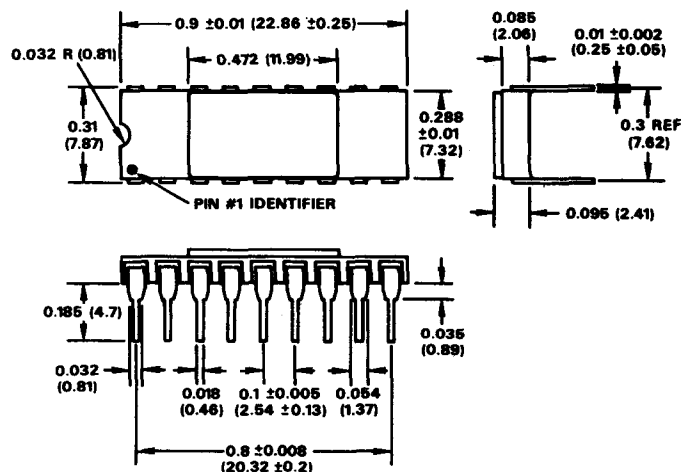


Figure 1. 18-Lead Ceramic Dual-In-Line Package

## CIRCUIT DESCRIPTION

The AD571 is a complete 10-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD571 is shown in Figure 2. Upon receipt of the CONVERT command, the internal 10-bit current output DAC is sequenced by the I<sup>2</sup>L successive-approximation register (SAR) from its most-significant bit (MSB) to least-significant bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less the bit is left on, if more, the bit is turned off. After testing all the bits, the SAR contains a 10-bit binary code which accurately represents the input signal to within  $\pm\frac{1}{2}$ LSB (0.05%).

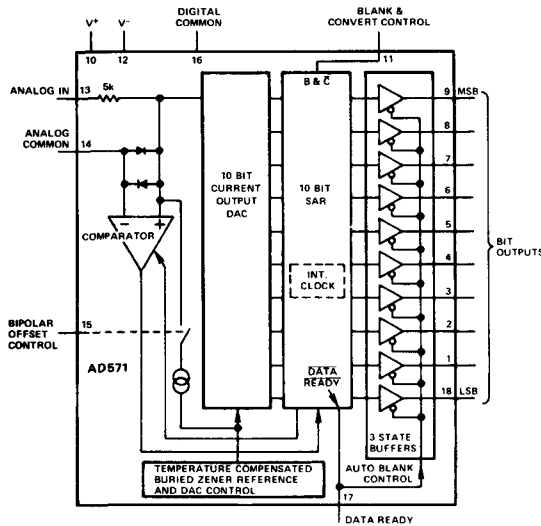


Figure 2. AD571 Functional Block Diagram

Upon completion of the sequence, the SAR sends out a DATA READY signal (active low), which also brings the three-state buffers out of their "open" state, making the bit output lines become active high or low, depending on the code in the SAR. When the BLANK and CONVERT line is brought high, the output buffers again go "open", and the

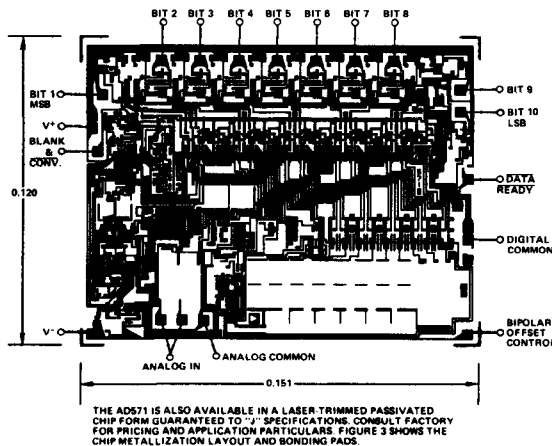


Figure 3. Chip Bonding Diagram

SAR is prepared for another conversion cycle. Details of the timing are given further.

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less  $\frac{1}{2}$ LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 to +10V unipolar input range becomes a -5V to +5V range. The 5kΩ thin film input resistor is trimmed so that with a full scale input signal, an input current will be generated which exactly matches the DAC output with all bits on. (The input resistor is trimmed slightly low to facilitate user trimming, as discussed on the next page.)

## POWER SUPPLY SELECTION

The AD571 is designed for optimum performance using a +5V and -15V supply, for which the AD571J and AD571S are specified. AD571K will also operate with up to a +15V supply, which allows direct interface to CMOS logic. The input logic threshold is a function of V<sub>+</sub> as shown in Figure 4. The supply current drawn by the device is a function of both V<sub>+</sub> and the operating mode (BLANK or CONVERT). These supply current variations are shown in Figure 5. The supply currents change only moderately over temperature as shown in Figure 9.

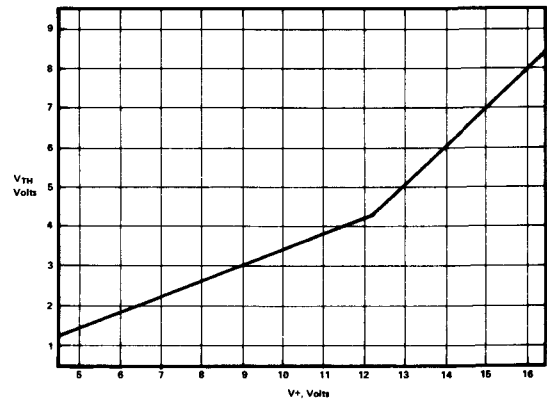


Figure 4. Logic Threshold (AD571K Only)

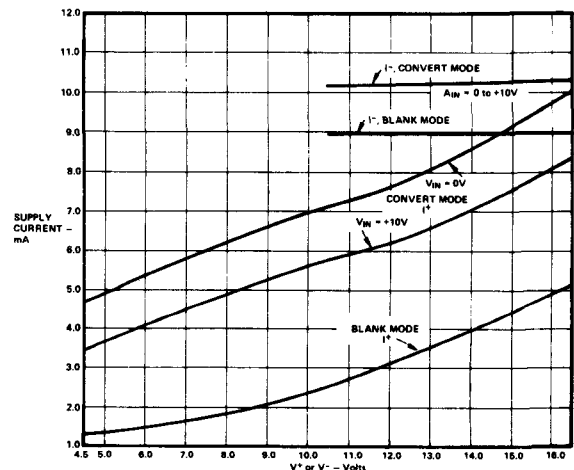


Figure 5. Supply Currents vs Supply Levels and Operating Modes

## CONNECTING THE AD571 FOR STANDARD OPERATION

The AD571 contains all the active components required to perform a complete A/D conversion. Thus, for most situations, all that is necessary is connection of the power supply (+5 and -15), the analog input, and the conversion start pulse. But, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 6.

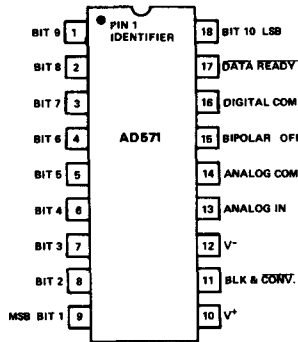


Figure 6. AD571 Pin Connections

## FULL SCALE CALIBRATION

The 5kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC—plus about 0.3%—when a full scale analog input voltage of 9.990 volts (10 volts - 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.99 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 13. Typical full scale calibration error will then be about ±2LSB or ±0.2%. If the more precise calibration is desired, a 50Ω trimmer should be used instead. Set the analog input at 9.990 volts, and set the trimmer so that the output code is just at the transition between 111111110 and 111111111. Each LSB will then have a weight of 9.766mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have weight of exactly 10.00mV), a 100Ω resistor in series with a 100Ω trimmer (or a 200Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ.

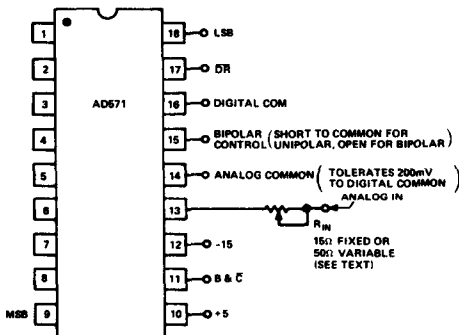


Figure 7. Standard AD571 Connections

## BIPOLAR OPERATION

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin to digital common. If the pin is left open, the bipolar offset current will be switched into the comparator summing node, giving a -5V to +5V range with an offset binary output code. (-5.00 volts in will give a 10-bit code of 000000000; an input of 0.00 volts results in an output code of 100000000 and 4.99 volts at the input yields the 111111111 code). The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 8.

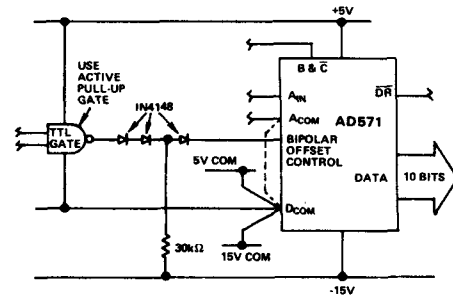


Figure 8. Bipolar Offset Controlled by Logic Gate

Gate Output = 1 Unipolar 0 - 10V Input Range  
Gate Output = 0 Bipolar ±5V Input Range

## COMMON MODE RANGE

The AD571 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common mode range between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition, a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. An additional 1mA will flow in during a blank interval with zero analog input. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. We recommend the connection of a parallel pair of back-to-back protection diodes between the commons if they are not connected locally.

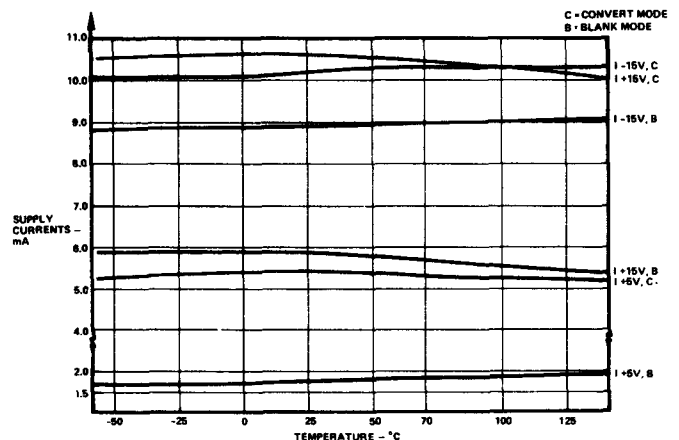


Figure 9. AD571 Power Supply Current vs Temperature



## ZERO OFFSET

The apparent zero point of the AD571 can be adjusted by inserting an offset voltage between the Analog Common of the device and the actual signal return or signal common. Figure 10 illustrates two methods of providing this offset. Figure 10A shows how the converter zero may be offset by up to  $\pm 3$  bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.

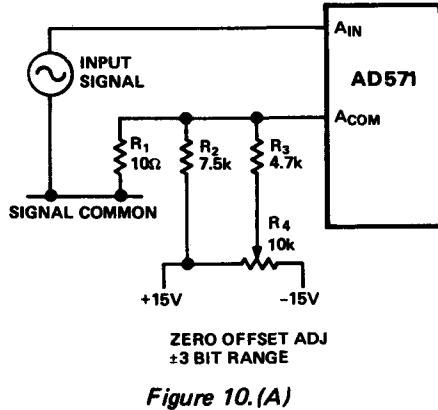


Figure 10.(A)

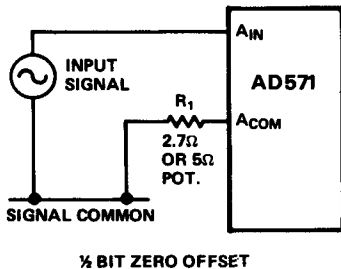
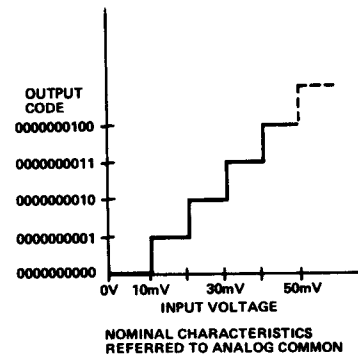


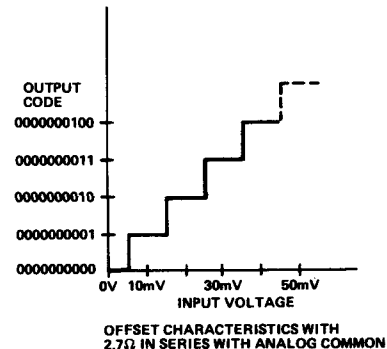
Figure 10.(B)

Figure 11 shows the nominal transfer curve near zero for an AD571 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics. This offset can easily be accomplished as shown in Figure 10B. At balance (after a conversion) approximately 2mA flows into the Analog Common terminal. A 2.7Ω resistor in series with this terminal will result in approximately the desired 1/2 bit offset of the transfer characteristics. The nominal 2mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 5Ω potentiometer (connected as a rheostat) can be used as R2. Additional negative offset range may be obtained by using larger values of R2. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of 1/2LSB is introduced, full scale trimming as described on previous page should be done with an analog input of 9.985 volts.

**NOTE:** During a conversion transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle as appropriate during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling which returns to analog signal common, should go to the signal input side of the resistive offset network.



NOMINAL CHARACTERISTICS REFERRED TO ANALOG COMMON



OFFSET CHARACTERISTICS WITH 2.7Ω IN SERIES WITH ANALOG COMMON

Figure 11. AD571 Transfer Curve - Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights  $\sim 9.766\text{mV}$ )

## MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD571, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further insure reliability, the AD571 is offered with 100% screening to MIL-STD-883B, method 5004.

Table I details the test procedures of MIL-STD-883. Analog Devices subjects each part ordered with 883B screening to these tests on a 100% basis.

TABLE I

| TEST                         | METHOD   |
|------------------------------|--|
| 1) Internal Visual (Pre cap) | 2010, Test Condition B   |
| 2) Stabilization Bake        | Method 1008, 24 hours @ +150°C                                 |
| 3) Temperature Cycling       | Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C      |
| 4) Constant Acceleration     | Method 2001, Test Condition E, Y1 plane, 30kg                  |
| 5) Seal, Fine and Gross      | Method 1014, Test Condition A and C                            |
| 6) Burn-in Test              | Method 1015, Test Condition B, 168 hours @ +125°C              |
| 7) Final Electrical Tests    | Performed 100% to all min and max specifications on data pages |
| 8) External Visual           | Method 2009  |

## CONTROL AND TIMING OF THE AD571

There are several important timing and control features on the AD571 which must be understood precisely to allow optimal interfacing to microprocessor or other types of control systems. All of these features are shown in the timing diagram in Figure 12.

The normal stand-by situation is shown at the left end of the drawing. The  $\overline{\text{BLANK}}$  and  $\overline{\text{CONVERT}}$  (B & C) line is held high, the output lines will be "open", and the  $\overline{\text{DATA READY}}$  ( $\overline{\text{DR}}$ ) line will be high. This mode is the lowest power state of the device (typically 150mW). When the (B & C) line is brought low, the conversion cycle is initiated; but the  $\overline{\text{DR}}$  and Data lines do not change state. When the conversion cycle is complete (typically 25 $\mu$ s), the  $\overline{\text{DR}}$  line goes low, and within 500ns, the Data lines become active with the new data.

About 1.5 $\mu$ s after the B & C line is again brought high, the  $\overline{\text{DR}}$  line will go high and the Data lines will go open. When the B & C line is again brought low, a new conversion will begin. The minimum pulse width for the B & C line to blank previous data and start a new conversion is 2 $\mu$ s. If the B & C line is brought high during a conversion, the conversion will stop, and the  $\overline{\text{DR}}$  and Data lines will not change. If a 2 $\mu$ s or longer pulse is applied to the B & C line during a conversion, the converter will clear and start a new conversion cycle.

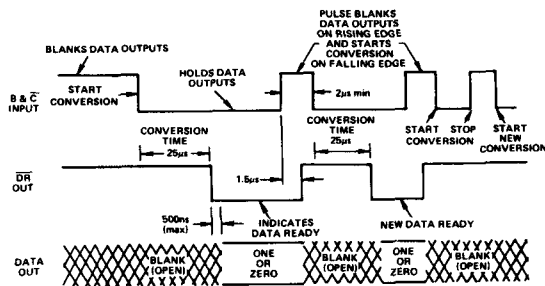


Figure 12. AD571 Timing and Control Sequence

## CONTROL MODES WITH $\overline{\text{BLANK}}$ AND $\overline{\text{CONVERT}}$

The timing sequence of the AD571 discussed above allows the device to be easily operated in a variety of systems with differing control modes. The two most common control modes, the Convert Pulse Mode, and the Multiplex Mode, are illustrated here.

**Convert Pulse Mode** — In this mode, data is present at the output of the converter at all times except when conversion is taking place. Figure 13 illustrates the timing of this mode. The  $\overline{\text{BLANK}}$  and  $\overline{\text{CONVERT}}$  line is normally low and conversions are triggered by a positive pulse. A typical application for this timing mode is shown in Figure 16, in which  $\mu$ P bus interfacing is easily accomplished with three-state buffers.

**Multiplex Mode** — In this mode the outputs are blanked except when the device is selected for conversion and readout; this timing shown in Figure 14. A typical AD571 multiplexing application is shown in Figure 17.

This operating mode allows multiple AD571 devices to drive common data lines. All  $\overline{\text{BLANK}}$  and  $\overline{\text{CONVERT}}$  lines are held high to keep the outputs blanked. A single AD571 is selected, its  $\overline{\text{BLANK}}$  and  $\overline{\text{CONVERT}}$  line is driven low and at the end of

conversion, which is indicated by  $\overline{\text{DATA READY}}$  going low, the conversion result will be present at the outputs. When this data has been read from the 10-bit bus,  $\overline{\text{BLANK}}$  and  $\overline{\text{CONVERT}}$  is restored to the blank mode to clear the data bus for other converters. When several AD571's are multiplexed in sequence, a new conversion may be started in one AD571 while data is being read from another. As long as the data is read and the first AD571 is cleared within 15 $\mu$ s after the start of conversion of the second AD571, no data overlap will occur.

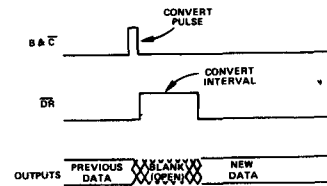


Figure 13. Convert Pulse Mode

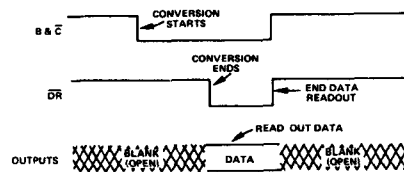


Figure 14. Multiplex Mode

## SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD571

Many situations in high-speed acquisition systems or digitizing of rapidly changing signals require a sample-and-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD571, a SHA can also serve as a high input impedance buffer.

Figure 15 shows the AD571 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10 $\mu$ s with a droop rate less than 100 $\mu$ V/ms. The control signals are arranged so that when the control line goes low, the AD582 is put into the "hold" mode, and the AD571 will begin its conversion cycle. (The AD582 settles to final value well in advance of the

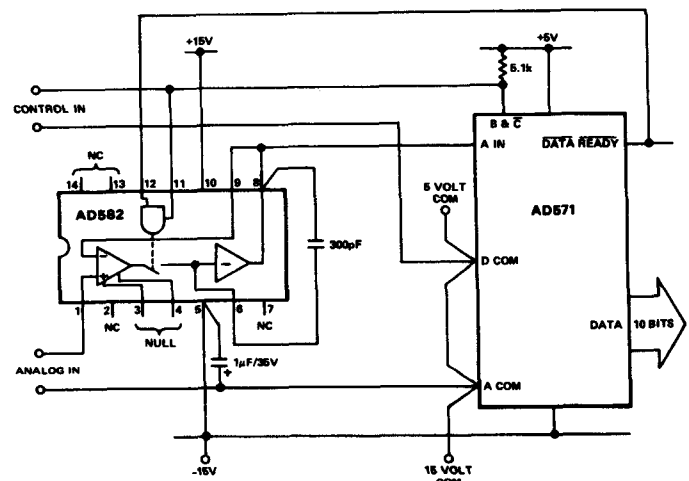


Figure 15. Sample-Hold Interface to the AD571

first comparator decision inside the AD571). The  $\overline{\text{DATA READY}}$  line is fed back to the other side of the differential input control gate so that the AD582 cannot come out of the "hold" mode during the conversion cycle. At the end of the conversion cycle, the  $\overline{\text{DATA READY}}$  line goes low, automatically placing the AD582 back into the sample mode. This feature allows simple control of both the SHA and the A-D converter with a single line. Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle to give the most accurate measurements.

### INTERFACING THE AD571 TO A MICROPROCESSOR

The AD571 can easily be arranged to be driven from standard microprocessor control lines and to present data to any standard microprocessor bus (4-, 8-, 12- or 16-bit) with a minimum of additional control components. The configuration shown in Figure 16 is designed to operate with an 8-bit bus and standard 8080 control signals.

The input control circuitry shown is required to insure that the AD571 receives a sufficiently long B & C input pulse. When the converter is ready to start a new conversion, the B & C line is low, and  $\overline{\text{DR}}$  is low. To command a conversion, the start address decode line goes low, followed by  $\overline{\text{WR}}$ . The B & C line will now go high, followed about 1.5  $\mu\text{s}$  later by  $\overline{\text{DR}}$ . This resets the external flip-flop and brings B & C back to low, which initiates the conversion cycle. At the end of the conversion cycle, the  $\overline{\text{DR}}$  line goes low, the data outputs will become active with the new data and the control lines will return to the stand-by state. The new data will remain active until a new conversion is commanded. The self-pulsing nature of this circuit guarantees a sufficient convert pulse width.

This new data can now be presented to the data bus by enabling the three-state buffers when desired. A data word (8-bit or 2-bit) is loaded onto the bus when its decoded address goes low and the  $\overline{\text{RD}}$  line goes low. This arrangement presents data to the bus "left-justified," with highest bits in the 8-bit word; a "right-justified" data arrangement can be set

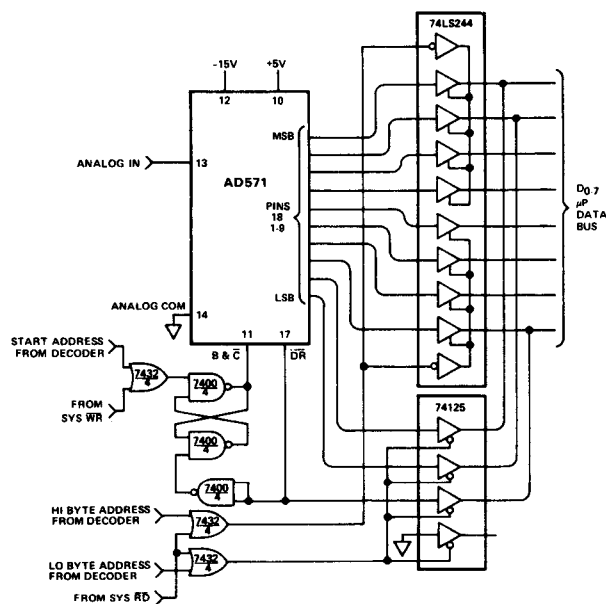


Figure 16. Interfacing AD571 to an 8-Bit Bus (8080 Control Structure)

up by a simple re-wiring. Polling the converter to determine if conversion is complete can be done by addressing the gate which buffers the  $\overline{\text{DR}}$  line, as shown. In this configuration, there is no need for additional buffer register storage since the data can be held indefinitely in the AD571, since the B & C line is continually held low.

### BUS INTERFACING WITH A PERIPHERAL INTERFACE CIRCUIT

An improved technique for interfacing to a  $\mu\text{P}$  bus involves the use of special peripheral interfacing circuits (or I/O devices), such as the MC6820 Peripheral Interface Adapter (PIA). Shown in Figure 17 is a straightforward application of a PIA to multiplex up to 8 AD571 circuits. The AD571 has 3-state outputs, hence the data bit outputs can be paralleled, provided that only one converter at a time is permitted to be the active state. The  $\overline{\text{DATA READY}}$  output of the AD571 is an open collector with resistor pull-up, thus several  $\overline{\text{DR}}$  lines can be wire-ored to allow indication of the status of the selected device. One of the 8-bit ports of the PIA is combined with 2-bits from the other port and programmed as a 10-bit input port. The remaining 6-bits of the second port are programmed as outputs and along with the 2 control bits (which act as outputs), are used to control the 8 AD571's. When a control line is in the "1" or high state, the ADC will be automatically blanked. That is, its outputs will be in the inactive open state. If a single control line is switched low, its ADC will convert and the outputs will automatically go active when the conversion is complete. The result can be read from the two peripheral ports; when the next conversion is desired, a different control line can be switched to zero, blanking the previously active port at the same time. Subsequently, this second device can be read by the microprocessor, and so-forth. The status lines are wire-ored in 2 groups and connected to the two remaining control pins. This allows a conversion status check to be made after a convert command, if necessary. The ADC's are divided into two groups to minimize the loading effect of the internal pull-up resistors on the  $\overline{\text{DATA READY}}$  buffers. See the MC6820 data sheet for more application detail.

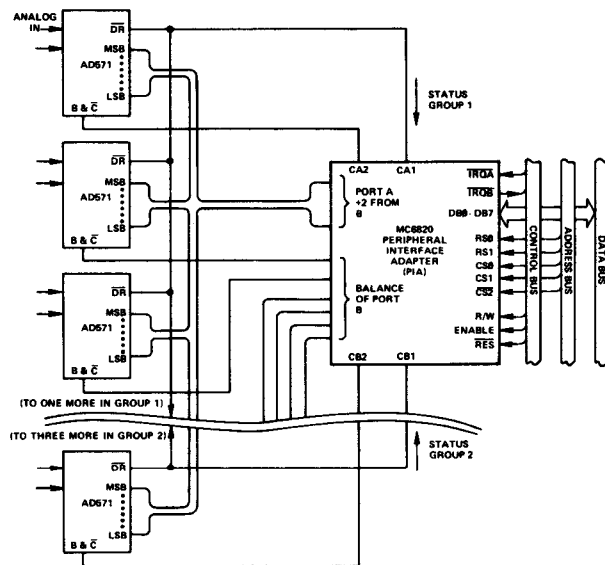


Figure 17. Multiplexing 8 AD571's Using Single PIA for  $\mu\text{P}$  Interface. No Other Logic Required (6800 Control Structure)

## PRELIMINARY TECHNICAL DATA

### FEATURES

Complete 12-Bit A/D Converter with Reference and Clock

Full 8 or 16-Bit Microprocessor Bus Interface

Guaranteed Linearity Over Temperature

0 to 70°C – AD574J, K, L

-55°C to +125°C – AD574S, T, U

No Missing Codes Over Temperature

Fast Successive Approximation Conversion - 25 $\mu$ s

Buried Zener Reference for Long-Term Stability

and Low Gain T.C. 10ppm/°C max AD574L  
12.5ppm/°C max AD574U

Low Profile 28-Pin Ceramic DIP

Low Power: 455mW

Low Cost

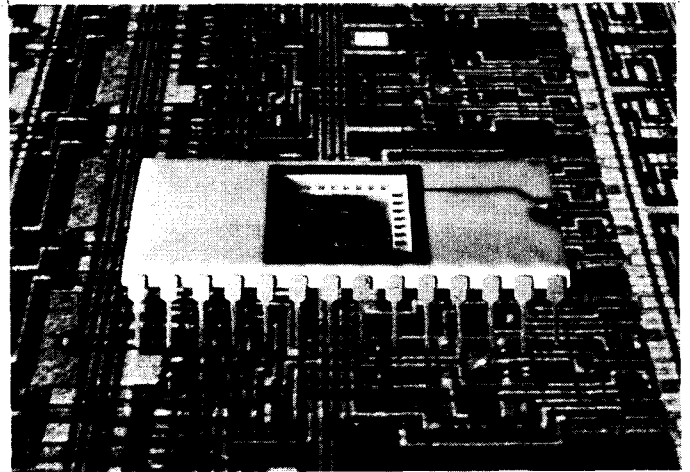
### PRODUCT DESCRIPTION

The AD574 is a complete 12-bit successive-approximation analog-to-digital converter with 3-state output buffer circuitry for direct interface to an 8-12- or 16-bit microprocessor bus. The AD574 design is implemented with two LSI chips each containing both analog and digital circuitry, resulting in the maximum performance and flexibility at the lowest cost.

One chip is the high performance AD565 12-bit DAC and voltage reference. It contains the high speed current output switching circuitry, laser-trimmed thin film resistor network, low T.C. buried zener reference and the precision input scaling and bipolar offset resistors. This chip is laser-trimmed at the wafer stage (LWT) to adjust ladder network linearity, voltage reference tolerance and temperature coefficient, and the calibration accuracy of input scaling and bipolar offset resistors.

The second chip uses the newly-developed LCI (linear-compatible integrated injection logic) process to provide the low-power I<sup>2</sup>L successive-approximation register, converter control circuitry, clock, bus interface, and the high performance latching comparator. The precision, low-drift comparator is adjusted for initial input offset error at the wafer stage by the "zener-zap" technique which trims the comparator input stage to 1/10 LSB typical error. This form of trimming, while cumbersome for complex ladder networks, is an attractive alternative to thin film resistor trimming for a simple offset adjustment and eliminates the need for thin film processing for this portion of the circuitry.

The AD574 is available in six different grades. The AD574J, K, and L grades are specified for operation over the 0 to +70°C temperature range. The AD574S, T, and U are specified for the -55°C to +125°C range. All grades are packaged in a low-profile, 0.600 inch wide, 28-pin hermetically-sealed ceramic DIP.



### PRODUCT HIGHLIGHTS

1. The AD574 interfaces to most popular microprocessors with an 8-, 12-, or 16-bit bus without external buffers or peripheral interface controllers. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12-bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros.)
2. The AD574 will also operate equally well in a self-cycling, stand alone mode and can perform conversions and latch data into an external latch at a 40kHz sample rate.
3. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges, 0 to +10 and 0 to +20 volts unipolar, or -5 to +5 and -10 to +10 volts bipolar. Typical bipolar offset and full scale calibration of  $\pm 0.05\%$  can be trimmed to zero with one external component each.
4. The internal buried zener reference is trimmed to 10.00 volts with a 1% maximum error and 15ppm/°C typical T.C. The reference is available externally and can drive up to 1.5mA beyond that required for the reference and bipolar offset resistors.
5. The two-chip construction renders the AD574 inherently more reliable than hybrid multi-chip designs. All three military grades have guaranteed linearity error over the full -55°C to +125°C and are especially recommended for high performance needs in harsh environments. These units are available fully processed to MIL-STD-883B, Level B.

# SPECIFICATIONS

(typical @ +25°C with  $V_{CC} = +15$ ,  $V_{LOGIC} = +5V$ ,  $V_{DD} = -15V$ , unless otherwise specified)

## DC AND TRANSFER ACCURACY SPECIFICATIONS

| MODEL  | AD574J                      | AD574K     | AD574L     | UNITS           |
|--|-----------------------------|------------|------------|-----------------|
| RESOLUTION (max)   | 12                          | 12         | 12         | Bits            |
| <b>NONLINEARITY ERROR</b>  |                             |            |            |                 |
| 25°C (max)   | ±1                          | ±1/2       | ±1/2       | LSB             |
| $T_{min}$ to $T_{max}$ (max)   | ±1                          | ±1/2       | ±1/2       | LSB             |
| <b>DIFFERENTIAL LINEARITY ERROR</b><br>(Minimum resolution for which no missing codes are guaranteed)                      |                             |            |            |                 |
| 25°C   | 11                          | 12         | 12         | Bits            |
| $T_{min}$ to $T_{max}$   | 11                          | 12         | 12         | Bits            |
| UNIPOLAR OFFSET (max) (Adjustable to zero)   | ±2                          | ±1         | ±1         | LSB             |
| BIPOLAR OFFSET (max) (Adjustable to zero)  | ±10                         | ±4         | ±4         | LSB             |
| <b>FULL SCALE CALIBRATION ERROR</b><br>(with fixed 50Ω resistor from REF OUT to REF IN)<br>(Adjustable to zero) 25°C (max) |                             |            |            |                 |
|  | 0.3                         | 0.2        | 0.2        | % of F.S.       |
| $T_{min}$ to $T_{max}$ (Without Initial Adjustment)  | 0.5                         | 0.3        | 0.2        | % of F.S.       |
| (With Initial Adjustment)  | 0.22                        | 0.12       | 0.05       | % of F.S.       |
| TEMPERATURE RANGE  | 0 to +70                    |            |            | °C              |
| <b>TEMPERATURE COEFFICIENTS (Using internal reference)</b><br>Guaranteed max change  |                             |            |            |                 |
| $T_{min}$ to $T_{max}$<br>Unipolar Offset  | ±2<br>(10)                  | ±1<br>(5)  | ±1<br>(5)  | LSB<br>(ppm/°C) |
| Bipolar Offset   | ±2<br>(10)                  | ±1<br>(5)  | ±1<br>(5)  | LSB<br>(ppm/°C) |
| Full Scale Gain  | ±9<br>(50)                  | ±5<br>(27) | ±2<br>(10) | LSB<br>(ppm/°C) |
| <b>POWER SUPPLY REJECTION</b><br>Max change in Full Scale Calibration  |                             |            |            |                 |
| +13.5V ≤ $V_{CC}$ ≤ +16.5V   | ±2                          | ±1         | ±1         | LSB             |
| +4.5V ≤ $V_{LOGIC}$ ≤ +5.5V  | ±1/2                        | ±1/2       | ±1/2       | LSB             |
| -16.5V ≤ $V_{DD}$ ≤ -13.5V   | ±2                          | ±1         | ±1         | LSB             |
| <b>ANALOG INPUTS</b>   |                             |            |            |                 |
| Input Ranges   |                             |            |            |                 |
| Bipolar  | -5 to +5<br>-10 to +10      |            |            | Volts<br>Volts  |
| Unipolar   | 0 to +10<br>0 to +20        |            |            | Volts<br>Volts  |
| Input Impedance  |                             |            |            |                 |
| 10 Volt Span   | 5k (3k min, 7k max)         |            |            | Ω               |
| 20 Volt Span   | 10k (6k min, 14k max)       |            |            | Ω               |
| <b>POWER SUPPLIES</b>  |                             |            |            |                 |
| Operating Range  |                             |            |            |                 |
| $V_{LOGIC}$  | +4.5 to +5.5                |            |            | Volts           |
| $V_{CC}$   | +13.5 to +16.5              |            |            | Volts           |
| $V_{DD}$   | -13.5 to -16.5              |            |            | Volts           |
| Operating Current  |                             |            |            |                 |
| $V_{LOGIC}$  | 25 typ., 35 max             |            |            | mA              |
| $V_{CC}$   | 2 typ., 6 max               |            |            | mA              |
| $V_{DD}$   | 20 typ., 35 max             |            |            | mA              |
| POWER DISSIPATION  | 455 typ., 780 max           |            |            | mW              |
| <b>INTERNAL REFERENCE VOLTAGE</b>  |                             |            |            |                 |
| Output Current (available for external loads)  | 10.00 ±0.1 (max)<br>1.5 min |            |            | Volts<br>mA     |

Specifications subject to change without notice.

**DC AND TRANSFER ACCURACY SPECIFICATIONS**

| MODEL   | AD574S      | AD574T                | AD574U       | UNITS           |
|---|-------------|-----------------------|--------------|-----------------|
| <b>RESOLUTION (max)</b>   | 12          | 12                    | 12           | Bits            |
| <b>NONLINEARITY ERROR</b>   |             |                       |              |                 |
| 25°C (max)  | ±1          | ±1/2                  | ±1/2         | LSB             |
| -25°C to +85°C (max)  | ±1          | ±1/2                  | ±1/2         | LSB             |
| -55°C to +125°C (max)   | ±1          | ±1                    | ±1           | LSB             |
| <b>DIFFERENTIAL LINEARITY ERROR</b><br>(Minimum resolution for which no missing codes are guaranteed) |             |                       |              |                 |
| 25°C  | 11          | 12                    | 12           | Bits            |
| T <sub>min</sub> to T <sub>max</sub>  | 11          | 12                    | 12           | Bits            |
| <b>UNIPOLAR OFFSET (max) (Adjustable to zero)</b>   | ±2          | ±1                    | ±1           | LSB             |
| <b>BIPOLAR OFFSET (max) (Adjustable to zero)</b>  | ±10         | ±4                    | ±4           | LSB             |
| <b>FULL SCALE CALIBRATION ERROR</b><br>(with fixed 50Ω resistor from REF IN to REF OUT)               |             |                       |              |                 |
| (Adjustable to zero) 25°C (max)   | 0.3         | 0.2                   | 0.2          | % of F.S.       |
| T <sub>min</sub> to T <sub>max</sub> (Without Initial Adjustment)                                     | 0.8         | 0.6                   | 0.3          | % of F.S.       |
| (With Initial Adjustment)   | 0.5         | 0.25                  | 0.12         | % of F.S.       |
| <b>TEMPERATURE RANGE</b>  | -55 to +125 |                       |              | °C              |
| <b>TEMPERATURE COEFFICIENTS (using internal reference)</b><br>Guaranteed max change                   |             |                       |              |                 |
| T <sub>min</sub> to T <sub>max</sub>  |             |                       |              |                 |
| Unipolar Offset   | ±2<br>(5)   | ±1<br>(2.5)           | ±1<br>(2.5)  | LSB<br>(ppm/°C) |
| Bipolar Offset  | ±4<br>(10)  | ±2<br>(5)             | ±1<br>(2.5)  | LSB<br>(ppm/°C) |
| Full Scale Calibration  | ±20<br>(50) | ±10<br>(25)           | ±5<br>(12.5) | LSB<br>(ppm/°C) |
| <b>POWER SUPPLY REJECTION</b>   |             |                       |              |                 |
| Max change in Full Scale Calibration  |             |                       |              |                 |
| +13.5V ≤ V <sub>CC</sub> ≤ +16.5V   | ±2          | ±1                    | ±1           | LSB             |
| +4.5V ≤ V <sub>LOGIC</sub> ≤ +5.5V  | ±1/2        | ±1/2                  | ±1/2         | LSB             |
| -16.5V ≤ V <sub>DD</sub> ≤ -13.5V   | ±2          | ±1                    | ±1           | LSB             |
| <b>ANALOG INPUTS</b>  |             |                       |              |                 |
| Input Ranges  |             |                       |              |                 |
| Bipolar   |             | -5 to +5              |              | Volts           |
|   |             | -10 to +10            |              | Volts           |
| Unipolar  |             | 0 to +10              |              | Volts           |
|   |             | 0 to +20              |              | Volts           |
| Input Impedance   |             |                       |              | Ω               |
| 10 Volt Span  |             | 5k (3k min, 7k max)   |              | Ω               |
| 20 Volt Span  |             | 10k (6k min, 14k max) |              | Ω               |
| <b>POWER SUPPLIES</b>   |             |                       |              |                 |
| Operating Range   |             |                       |              |                 |
| V <sub>LOGIC</sub>  |             | +4.5 to +5.5          |              | Volts           |
| V <sub>CC</sub>   |             | +13.5 to +16.5        |              | Volts           |
| V <sub>DD</sub>   |             | -13.5 to -16.5        |              | Volts           |
| Operating Current   |             |                       |              | mA              |
| V <sub>LOGIC</sub>  |             | 25 typ., 35 max       |              | mA              |
| V <sub>CC</sub>   |             | 2 typ., 6 max         |              | mA              |
| V <sub>DD</sub>   |             | 20 typ., 35 max       |              | mA              |
| <b>POWER DISSIPATION</b>  |             | 455 typ., 780 max     |              | mW              |
| <b>INTERNAL REFERENCE VOLTAGE</b>   |             |                       |              |                 |
| Output Current (available for external loads)   |             | 10.00 ±0.1 (max)      |              | Volts           |
|   |             | 1.5 min               |              | mA              |

Specifications subject to change without notice.

## DIGITAL CHARACTERISTICS

### ALL GRADES

(See Page 222S for Detailed Timing Specifications)

LOGIC INPUTS (Not including  $12/\bar{8}$ , which must be hard-wired high or low.)

$$4.5V \leq V_{\text{LOGIC}} \leq 5.5V$$

Input Threshold

$T_{\text{min}}$  to  $T_{\text{max}}$

Logic "1"

2.0 Volts min

Logic "0"

0.8 Volts max

Input Current

$T_{\text{min}}$  to  $T_{\text{max}}$

Logic "1"

10 $\mu$ A max

Logic "0"

10 $\mu$ A max

## LOGIC OUTPUTS

$T_{\text{min}}$  to  $T_{\text{max}}$

Bit Outputs and STS

Output Sink Current

1.6mA min

( $V_{\text{OUT}} = 0.4V$  max)

(1 TTL Load)

Output Source Current

0.5mA min

( $V_{\text{OUT}} = 2.4V$  min)

Output Leakage when Blanked

$\pm 40\mu$ A max

## OUTPUT CODING

Unipolar

Positive True Binary

Bipolar

Positive True Offset

Binary

## CONVERSION TIME

15 $\mu$ s min

25 $\mu$ s typ

35 $\mu$ s max

## MINIMUM START PULSE WIDTH

AT CE (Pin 6) (Positive)

300ns

AT  $\bar{CS}$  (Pin 3) (Negative)

400ns

AT R/ $\bar{C}$  (Pin 5) (Negative)

400ns

## ABSOLUTE MAXIMUM RATINGS

(Specifications apply to all grades, except where noted)

$V_{\text{CC}}$  to Digital Common . . . . . 0 to +16.5V

$V_{\text{DD}}$  to Digital Common . . . . . 0 to -16.5V

$V_{\text{LOGIC}}$  to Digital Common . . . . . 0 to +7V

Analog Common to Digital Common . . . . .  $\pm 1V$

Control Inputs (CE,  $\bar{CS}$ , A<sub>0</sub>,  $12/\bar{8}$ , R/ $\bar{C}$ ) to

Digital Common . . . . . 0 to  $V_{\text{LOGIC}}$

Analog Inputs (REF, IN, BIP OFF,  $10 V_{\text{IN}}$ ) to

Analog Common . . . . .  $\pm 12V$

$20 V_{\text{IN}}$  to Analog Common . . . . .  $\pm 24V$

REF OUT . . . . . Indefinite short to common

Momentary short to  $V_{\text{CC}}$

Chip Temperature (J, K, L grades) . . . . . 100°C

(S, T, U grades) . . . . . 150°C

Power Dissipation . . . . . 1000mW

Lead Temperature, Soldering . . . . . 300°C, 10 sec.

Storage Temperature . . . . . -65°C to +150°C

## MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD574, with the inherent reliability of integrated circuit construction, was designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protects the chip from hazardous environments. To further insure reliability, the AD574 is offered with 100% screening to MIL-STD-883B, method 5004.

Table I details the test procedures of MIL-STD-883. Analog Devices subjects each part ordered with 883B screening to these tests on a 100% basis.

TABLE I

| TEST                         | METHOD   |
|------------------------------|--|
| 1) Internal Visual (Pre cap) | 2010, Test Condition B   |
| 2) Stabilization Bake        | Method 1008, 24 hours @ +150°C                                 |
| 3) Temperature Cycling       | Method 1010, Test Condition C, 10 Cycles, -65°C to +150°C      |
| 4) Constant Acceleration     | Method 2001, Test Condition E, Y1 plane, 30kg                  |
| 5) Seal, Fine and Gross      | Method 1014, Test Condition A and C                            |
| 6) Burn-in Test              | Method 1015, Test Condition B, 168 hours @ +125°C              |
| 7) Final Electrical Tests    | Performed 100% to all min and max specifications on data pages |
| 8) External Visual           | Method 2009  |

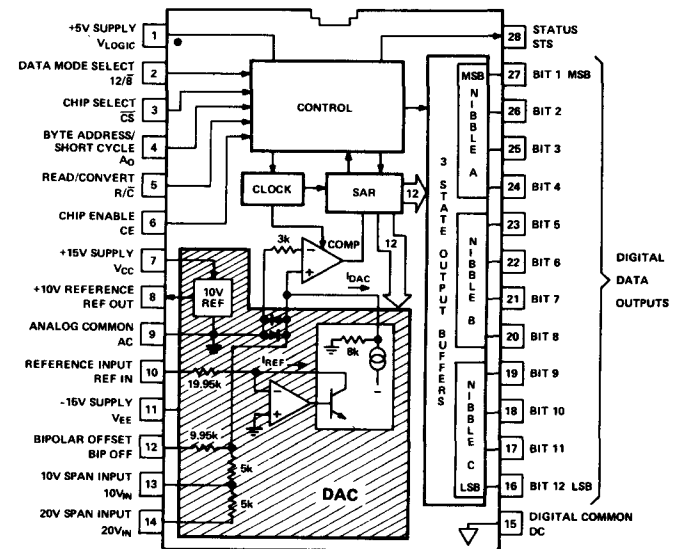


Figure 1. AD574 Block Diagram and Pin Configuration

## THE AD574 OFFERS GUARANTEED MAXIMUM LINEARITY OVER THE FULL OPERATING TEMPERATURE RANGE

### DEFINITIONS OF SPECIFICATIONS

#### NONLINEARITY ERROR

Nonlinearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs 1/2LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 1/2LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The AD574K, L, T, and U grades are guaranteed for maximum nonlinearity error of  $\pm 1/2$ LSB over their respective temperature ranges. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The AD574J and S grades are guaranteed to  $\pm 1$ LSB max error over their respective temperature ranges. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

#### DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. (In actual practice, our test systems limit minimum code width to 1/4LSB.) For the AD574K, L, T, and U grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The AD574J and S grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12 bit codes are missing.

#### UNIPOLAR OFFSET

The first transition should occur at a level 1/2LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following two pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

#### BIPOLAR OFFSET

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for

an analog value 1/2LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

#### FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for 10,000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figure 5. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

#### POWER SUPPLY REJECTION

The standard specifications for the AD574 assume use of +5.00 and  $\pm 15.00$  volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

#### CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

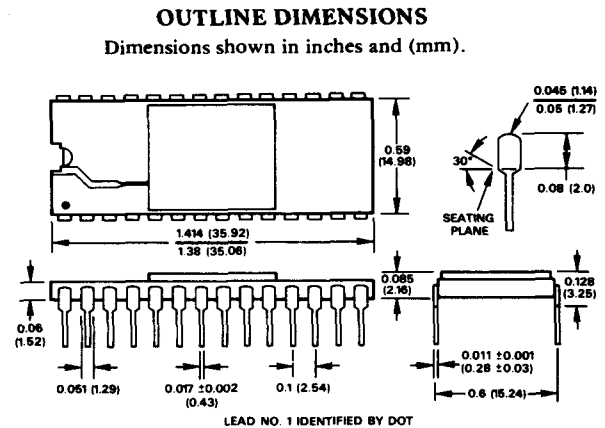


Figure 2. 28 Lead Dual-in-Line Package

#### AD574 ORDERING GUIDE

| MODEL   | TEMP RANGE                            | LINEARITY ERROR<br>MAX ( $T_{min}$ to $T_{max}$ ) | RESOLUTION<br>NO MISSING CODES<br>( $T_{min}$ to $T_{max}$ ) | FULL SCALE<br>T.C. (ppm/ $^{\circ}$ C) |
|---------|---------------------------------------|---|--|--|
| AD574JD | 0 to +70 $^{\circ}$ C                 | $\pm 1$ LSB                                       | 11 Bits  | 50.0                                   |
| AD574KD | 0 to +70 $^{\circ}$ C                 | $\pm 1/2$ LSB                                     | 12 Bits  | 27.0                                   |
| AD574LD | 0 to +70 $^{\circ}$ C                 | $\pm 1/2$ LSB                                     | 12 Bits  | 10.0                                   |
| AD574SD | -55 to +125 $^{\circ}$ C              | $\pm 1$ LSB                                       | 11 Bits  | 50.0                                   |
| AD574TD | -25 $^{\circ}$ C to +85 $^{\circ}$ C  | $\pm 1/2$ LSB                                     |  |  |
|         | -55 $^{\circ}$ C to +125 $^{\circ}$ C | $\pm 1$ LSB                                       | 12 Bits  | 25.0                                   |
| AD574UD | -25 $^{\circ}$ C to +85 $^{\circ}$ C  | $\pm 1/2$ LSB                                     |  |  |
|         | -55 $^{\circ}$ C to +125 $^{\circ}$ C | $\pm 1$ LSB                                       | 12 Bits  | 12.5                                   |



## CIRCUIT OPERATION

The AD574 is a complete 12-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD574 is shown in Figure 3. The device consists of two chips, one containing the precision 12-bit DAC with voltage reference, the other containing the comparator, successive-approximation register, clock, output buffers and control circuitry.

When the control section is commanded to initiate a conversion (as described later), it then enables the clock and resets the successive-approximation register (SAR) to all zeros. (Once a conversion cycle has begun, it cannot be stopped or re-started and data is not available from the output buffers). The SAR, timed by the clock, will then sequence through the conversion cycle and return an end-of-convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read functions by external command.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most-significant-bit (MSB) to least-significant-bit (LSB) to provide an output current which accurately balances the input signal current through the  $5k\Omega$  (or  $10k\Omega$ ) input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within  $\pm 1/2$ LSB.

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts  $\pm 1\%$ ; it is buffered and can supply up to 1.5mA to an external load in addition to that required to drive the reference input resistor ( $0.5mA$ ) and bipolar offset resistor ( $1mA$ ). The thin film application resistors are trimmed to match the full scale output current of the DAC. There are two  $5k\Omega$  input scaling resistors to allow either a 10 volt or 20 volt span. The  $10k\Omega$  bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation. (Details of full scale and offset trimming are given on next page.)

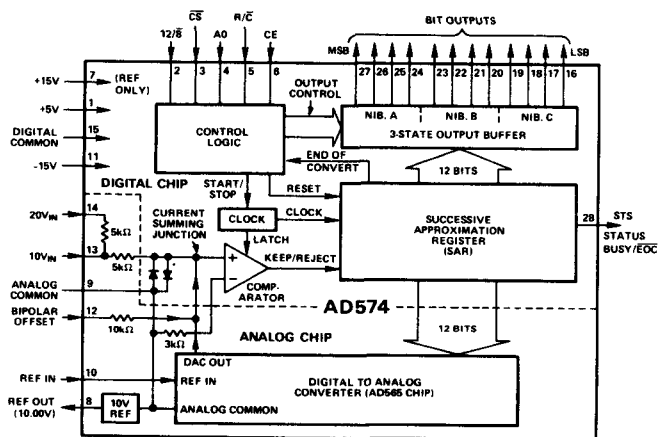


Figure 3. Block Diagram of AD574 12 bit A-to-D Converter

## CONTROL FUNCTIONS

There are two sets of control pins on the AD574, the general control inputs (CE,  $\overline{CS}$ , and  $R/\overline{C}$ ) and the internal register control inputs ( $12/\overline{8}$  and  $A_0$ ). The general control pins function similarly to those on most A/D converters, performing device timing, addressing, cycle initiation and read enable functions. The internal register control inputs, which are not found on most A/D converters, select output data format and conversion cycle length.

The two major control functions, convert start and read enable, are controlled by CE,  $\overline{CS}$ ,  $R/\overline{C}$ . Although all three inputs must be in the correct state to perform the function (for convert start, CE = 1,  $\overline{CS}$  = 0,  $R/\overline{C}$  = 0; for read enable, CE = 1,  $\overline{CS}$  = 0,  $R/\overline{C}$  = 1), the sequence does not matter. For large systems, typically microprocessor controlled, standard operation for convert start would be to first set  $R/\overline{C}$  = 0 (from  $R/\overline{W}$  line); address the chip with  $\overline{CS}$  = 0, then apply a positive start pulse to CE. A read would be done similarly but with  $R/\overline{C}$  = 1.

For a much simpler stand-alone operation, CE can be wired high,  $\overline{CS}$  wired low, and  $R/\overline{C}$  toggled as needed to initiate conversion. In this mode, a 200ns negative pulse will initiate conversion, and the data will automatically appear at the end of conversion. Alternatively, the  $R/\overline{C}$  input can be brought low to start conversion, then brought high at any time later (after completion of conversion) to enable the data output lines. Many combinations of the above can be implemented by proper manipulation of the three control lines. Exact timing of these functions is shown on page 222S.

The  $A_0$  (byte select) and  $12/\overline{8}$  (data format) inputs work together to control the output data and conversion cycle. In almost all situations  $12/\overline{8}$  is hard-wired high or low. If it is wired high, all 12 data lines will be enabled when the read function is called by the general control inputs. For an 8-bit bus interface,  $12/\overline{8}$  will be wired low. In this mode, only the 8 upper bits or the 4 lower bits can be enabled at once, as addressed by  $A_0$ . For these applications, the 4LSB's (pins 16–19) should be hard-wired to the 4MSB's (pins 24–27). Thus, during a read, when  $A_0$  is low the upper 8 bits are enabled and present data on pins 20 through 27. When  $A_0$  goes high, the upper 8 data bits are disabled, the 4LSB's then present data to pins 24 to 27, and the 4 middle bits are overridden so that zeros are presented to pins 20 to 23.

The  $A_0$  input performs an additional function of controlling conversion length. If  $A_0$  is held low prior to cycle initiation, a full 12-bit cycle in about  $25\mu s$  will result; if  $A_0$  is held high prior to cycle initiation a shortened 8-bit cycle in about  $16\mu s$  will result. The  $A_0$  line must be set prior to cycle initiation and held in the desired position at least until STS goes high. Thus, for microprocessor interface applications, the  $A_0$  line must be properly controlled during both the convert start and read functions.

The STS or status line goes high at the initiation of the conversion cycle and will go low when the cycle is complete.

## UNIPOLAR RANGE CONNECTIONS FOR THE AD574

The AD574 contains all the active components required to perform a complete 12-bit A/D conversion. Thus, for most situations, all that is necessary is connection of the power supplies (+5, +15, and -15 volts), the analog input, and the conversion initiation command, as discussed on next page. Analog input connections and calibration are easily accomplished; the unipolar operating mode is shown in Figure 4.

All of the thin film application resistors of the AD574 are trimmed for absolute calibration. Therefore, in many applications, no calibration trimming will be required. The absolute accuracy for each grade is given in the specification tables. For example, if no trims are used, the AD574K guarantees  $\pm 1$ LSB max zero offset error and  $\pm 0.2\%$  (8LSB) max full scale error. (Typical full scale error is  $\pm 2$ LSB.) If the offset trim is not required, pin 12 can be connected directly to pin 9; the two resistors and trimmer for pin 12 are then not needed. If the full scale trim is not needed, a  $50\Omega \pm 1\%$  resistor should be connected between pin 8 and pin 10.

The analog input is connected between pin 13 and pin 9 for a 0 to +10V input range, between 14 and pin 9 for a 0 to +20V input range. The AD574 easily accommodates an input signal beyond the +15V supply. For the 10 volt span input, the LSB has a nominal value of 2.44mV, for the 20 volt span, 4.88mV. If a 10.24V range is desired (nominal 2.5mV/bit), the gain trimmer (R2) should be replaced by a  $50\Omega$  resistor, and a  $200\Omega$  trimmer inserted in series with the analog input to pin 13 (for a full scale range of 20.48V (5mV/bit), use a  $500\Omega$  trimmer into pin 14.) The gain trim described below is now done with these trimmers. The nominal input impedance into pin 13 is  $5k\Omega$ , and  $10k\Omega$  into pin 14.

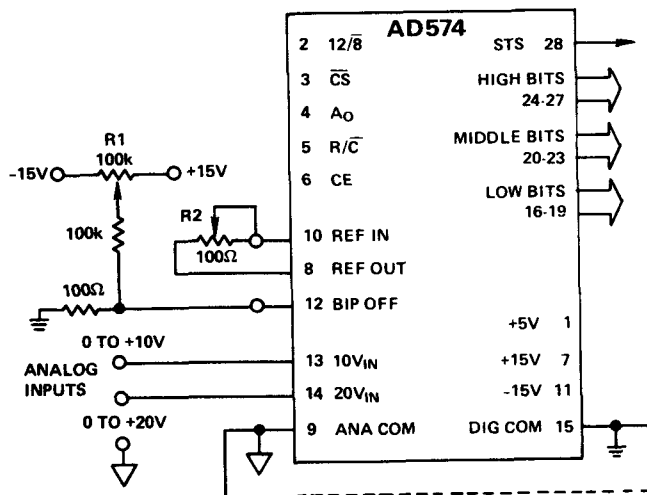


Figure 4. Unipolar Input Connections

## UNIPOLAR CALIBRATION

The AD574 is intended to have a nominal  $1/2$ LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes

above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of  $+1/2$ LSB (1.22mV for 10V range). If pin 12 is connected to pin 9, the unit typically will behave in this manner, within specifications. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately  $\pm 15$ mV of offset trim range.

The full scale trim is done by applying a signal  $1/2$ LSB below the nominal full scale (9.9963 for a 10V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

## BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 5. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, one or both of the trimmers shown can be replaced by a  $50\Omega \pm 1\%$  fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal  $1/2$ LSB above negative full scale ( $-4.9988$ V for the  $\pm 5$ V range) is applied, and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then, a signal is  $1/2$ LSB below positive full scale ( $+4.9963$ V for the  $\pm 5$ V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

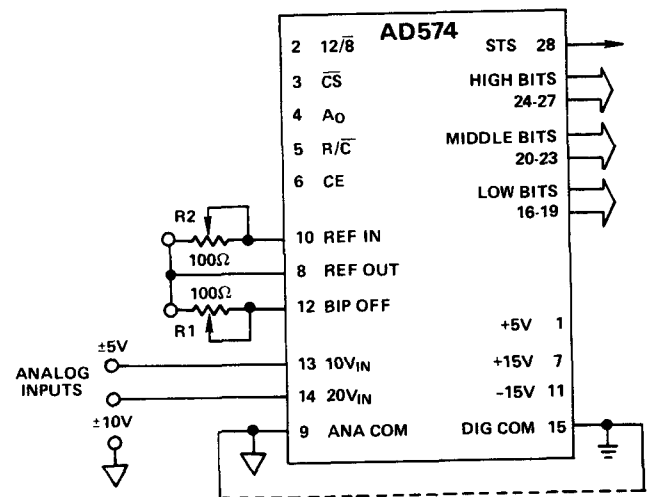


Figure 5. Bipolar Input Connections

The analog common at pin 9 is the ground reference point for the internal reference and is thus the "high quality" ground for the AD574; it should be connected directly to the analog reference point of the system. The digital common at pin 15 can be connected to the most convenient ground reference point; analog power return is preferred. If digital common contains high frequency noise beyond 200mV, this noise may feed through the converter, so that some caution will be required in applying these grounds.

## FULL CONTROL INTERFACE

The AD574 has a versatile set of control functions which will allow interface to a wide variety of microprocessor types as well as much simpler data acquisition systems, and even stand alone applications. It would be impossible to cover all of the potential AD574 control interface situations, but discussion of the two possible extreme situations and their timing will allow extension of the control concepts to most other applications.

### STANDARD FULL CONTROL INTERFACE

The timing for the standard full control interface is shown in Figure 6. In this operating mode,  $\overline{CS}$  is used as the address input which selects the particular device,  $R/\overline{C}$  selects between the read data and start conversion functions, and CE is used to time the actual functions.

The left side of the figure shows the conversion start control.  $\overline{CS}$  and  $R/\overline{C}$  are brought low (their sequence does not matter), then the start pulse is applied to CE. The timing diagram shows a time delay for  $\overline{CS}$  and  $R/\overline{C}$  prior to the start pulse at CE. If less time than this is allowed, the conversion will still be started, but an appropriately longer pulse will be needed at CE. However, if the hold times for  $\overline{CS}$  and  $R/\overline{C}$  after the rising edge of the start pulse at CE are not followed, the conversion may not be initiated.

The  $A_0$  line determines the conversion cycle length, and must be selected prior to conversion initiation. If  $A_0$  is low, a 12-bit cycle results; if  $A_0$  is high, an 8-bit short cycle results. Minimum set-up and hold times are shown. The status line goes high to indicate conversion in progress. The analog input signal is

allowed to vary until the STS goes high. It must then be held steady until STS again goes low at the end of conversion.

The data read function operates in a similar fashion except that  $R/\overline{C}$  is now held high. The data is stored in the output register and can be recalled at will until a new conversion cycle is commanded. In addition, if the converter is arranged in the 8-bit data mode, the  $A_0$  line now functions as the byte select address, with set-up and hold times as shown. The  $A_0$  line can be switched directly from one byte to the next without recycling the other three control lines. With  $A_0$  low, pins 20 to 27 (bits 8-1) come out of three-state and present data. With  $A_0$  high, pins 16-19 (bits 12-9) come out of three-state with data and pins 20-23 present active trailing zeros. In the 8-bit mode pins 16-19 will be hard-wired directly to pins 24-27 for direct two-byte loading onto an 8-bit bus. There are two delay times for the data lines after CE is brought low:  $t_{HD}$  is the delay until data is no longer valid;  $t_{HL}$  is the delay until the outputs are fully into the high impedance state.

### TIMING SPECIFICATIONS — FULL CONTROL MODE

|           |   |           |           |
|-----------|---|-----------|-----------|
| $t_{DSC}$ | 200ns max                                       | $t_{DD}$  | 350ns max |
| $t_{HEC}$ | 300ns min                                       | $t_{HD}$  | 100ns min |
| $t_{SSC}$ | 300ns min                                       | $t_{SSR}$ | 250ns min |
| $t_{HSC}$ | 200ns min                                       | $t_{SRR}$ | 0 min     |
| $t_{SRC}$ | 200ns min                                       | $t_{SAR}$ | 200ns min |
| $t_{HRC}$ | 200ns min                                       | $t_{HSR}$ | 100ns min |
| $t_{SAC}$ | 0 min   | $t_{HRR}$ | 0 min     |
| $t_{HAC}$ | 300ns min                                       | $t_{HAR}$ | 100ns min |
| $t_C$     | 15-35 $\mu$ s (12 bit)<br>10-20 $\mu$ s (8-bit) | $t_{HL}$  | 350ns max |

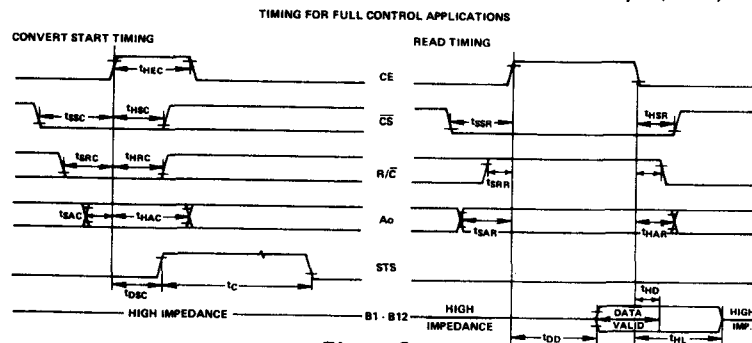


Figure 6.

remain valid for the time  $t_{HDR}$ . An alternative to the above is to toggle  $R/\overline{C}$  as needed to initiate a new cycle on read data. Data will appear when  $R/\overline{C}$  is brought high, a new cycle is initiated when  $R/\overline{C}$  goes low.

### TIMING SPECIFICATIONS — STAND ALONE MODE

|                        |                       |
|------------------------|-----------------------|
| $t_{HRL}$              | 400ns min             |
| $t_{DS}$               | 500ns max             |
| $t_{HDR}$              | 300ns min             |
| $t_{HS}$               | -100ns min +200ns max |
| $t_{HRH}$              | 150ns min             |
| $t_{DDR}$              | 350ns max             |
| $t_C$ (12 bit convert) | 15-35 $\mu$ s         |
| $t_C$ (8 bit convert)  | 10-20 $\mu$ s         |

## STAND ALONE OPERATION

For simpler control functions, the AD574 can be controlled with just  $R/\overline{C}$ . In this case, CE is wired high,  $\overline{CS}$  low,  $12/\overline{8}$  high, and  $A_0$  low. There are two ways of cycling the device with this simple hook-up. If a negative pulse is used to initiate conversion as in Figure 7, the converter will automatically bring the 12 data lines out of three-state at the end of conversion. The data will remain valid on the output lines until another pulse is applied.

If the conversion is initiated by a high pulse as shown in Figure 8, the data lines are held in three-state at the end of conversion until  $R/\overline{C}$  is brought high. The next conversion cycle is initiated when  $R/\overline{C}$  goes low, the data from the previous cycle will

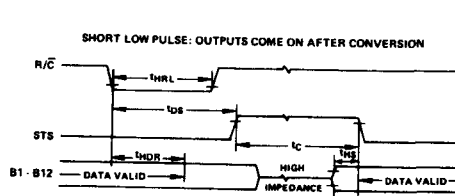


Figure 7.

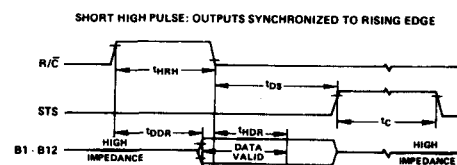


Figure 8.

## PRELIMINARY TECHNICAL DATA

### FEATURES

#### Performance

True 12-Bit Operation: Max Nonlinearity  $< \pm 0.012\%$

Low Gain T.C.:  $< \pm 30\text{ppm}/^\circ\text{C}$

Low Power: 800mW

Fast Conversion Time:  $< 22\mu\text{s}$

Precision 6.3V Reference for External Application

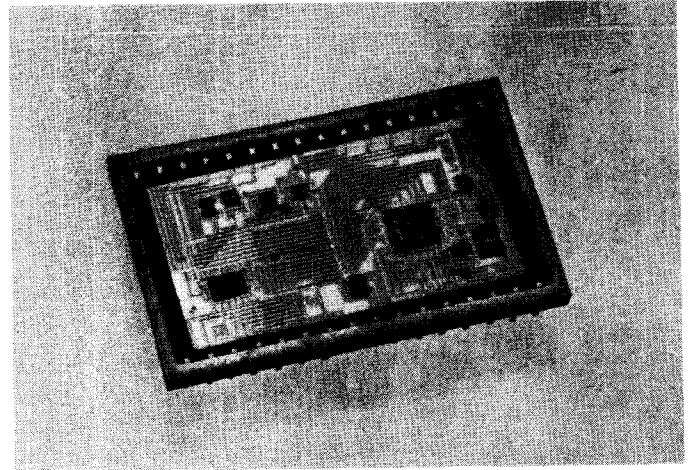
Short-Cycle Capability

Serial or Parallel Logic Outputs

Monolithic DAC with Scaling Resistors for Stability

Low Chip Count—High Reliability

Industry—Standard Pinout



## PRODUCT DESCRIPTION

The AD ADC80 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility of use combined with IC size, price and reliability.

Important performance characteristics of the AD ADC80 include a maximum linearity error at  $+25^\circ\text{C}$  of  $\pm 0.012\%$ , max gain T.C. of  $30\text{ppm}/^\circ\text{C}$ , typical power dissipation of 800mW and conversion time of  $22\mu\text{s}$ . Monotonic operation of the feedback D/A converter guarantees no missing codes over the temperature range of  $-25^\circ\text{C}$  to  $+85^\circ\text{C}$ .

The design of the AD ADC80 includes scaling resistors that provide analog signal ranges of  $\pm 2.5$ ,  $\pm 5.0$ ,  $\pm 10$ , 0 to  $+5$  or 0 to  $+10$  volts. The 6.3V precision reference may be used for external applications. All digital signals are fully DTL and TTL compatible; output data may be read in both serial and parallel form.

The AD ADC80 is available in two performance grades, the AD ADC80-12 (0.012% of FSR max) and the AD ADC80-10 (0.048% of FSR max). Both grades are specified for use over the  $-25^\circ\text{C}$  to  $+85^\circ\text{C}$  temperature range and both are available in a 32-pin hermetically sealed ceramic DIP.

## PRODUCT HIGHLIGHTS

1. The AD ADC80 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. Monolithic 12-bit feedback DAC for reduced chip count and higher reliability.
3. The internal buried zener reference is laser trimmed to 6.3 volts. The reference voltage is available externally and can supply up to 1.5mA beyond that required for the reference and bipolar offset current.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. Every AD ADC80 is subject to stabilization bakes and receives a powered burn-in at  $+125^\circ\text{C}$ .
6. The AD ADC80 directly replaces other devices of this type with significant increases in performance.
7. The fast conversion rate of the AD ADC80 makes it an excellent choice for applications requiring high system throughput rates.
8. The short cycle and external clock options are provided for applications requiring faster conversion speeds or lower resolutions.



Figure 2. Linearity Error vs. Conversion Time (Normalized)

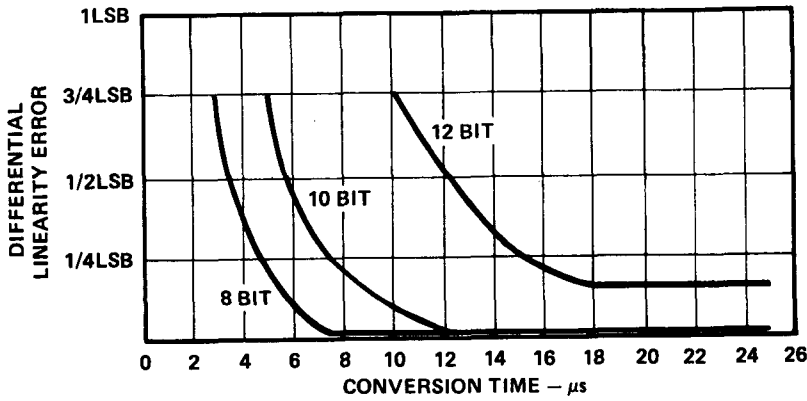
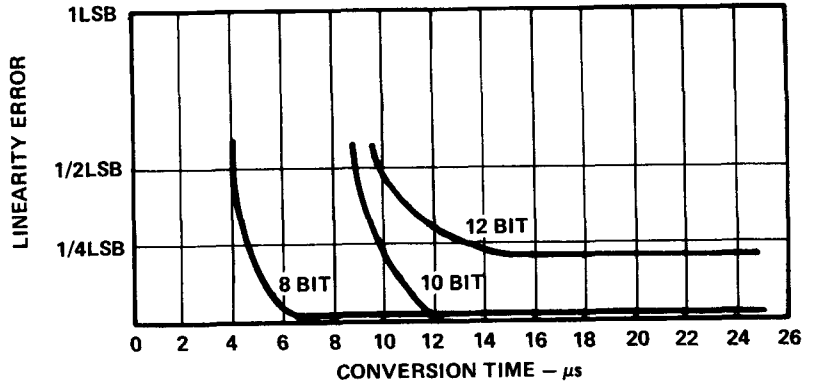


Figure 3. Differential Linearity Error vs. Conversion Time (Normalized)

Figure 4. Maximum Gain Drift Error – % of FSR vs. Temperature

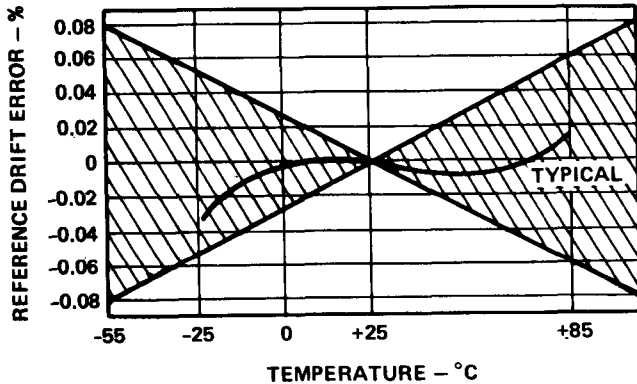
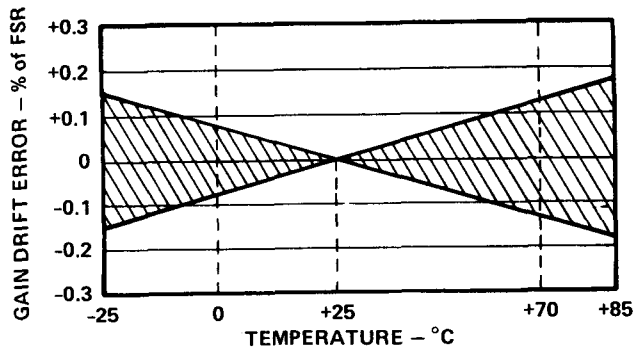


Figure 5. Reference Drift – % Error vs. Temperature

The analog continuum is partitioned into  $2^{12}$  discrete ranges for 12-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of  $\pm 1/2\text{LSB}$ , associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the AD ADC80 have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at  $\pm 0.1\%$  FSR for gain and  $\pm 0.05\%$  FSR for offset. These errors may be trimmed to zero by the use of the external trim circuits as shown in Figures 7 and 9. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in staircase step width between codes from the ideal least significant bit (Figure 6).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD ADC80 is specified as having no missing codes over the entire temperature range from  $-25^\circ\text{C}$  to  $+85^\circ\text{C}$ .

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$\text{RSS} = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

$\epsilon_G$  = Gain Drift Error (ppm/ $^\circ\text{C}$ )

$\epsilon_O$  = Offset Drift Error (ppm of FSR/ $^\circ\text{C}$ )

$\epsilon_L$  = Linearity Error (ppm of FSR/ $^\circ\text{C}$ )

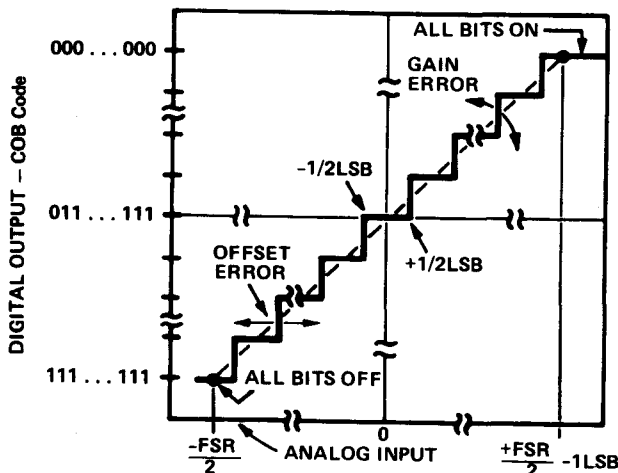


Figure 6. Transfer Characteristic for an Ideal Bipolar A/D

## OFFSET ADJUSTMENT

The zero adjust circuit consists of a potentiometer connected across  $\pm V_S$  with its slider connected through a  $1.8\text{M}\Omega$  resistor to Comparator Input pin 11 for all ranges. As shown in Figure 7 the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a  $-1200\text{ppm}/^\circ\text{C}$  tempco contributes a worst-case offset tempco of  $8 \times 244 \times 10^{-6} \times 1200\text{ppm}/^\circ\text{C} = 2.3\text{ppm}/^\circ\text{C}$  of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than  $\pm 4\text{LSB}$ , use of a carbon composition offset summing resistor typically contributes no more than  $1\text{ppm}/^\circ\text{C}$  of FSR offset tempco.

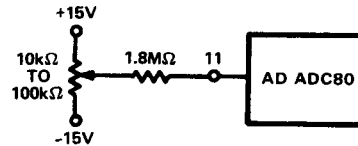


Figure 7. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco  $< 100\text{ppm}/^\circ\text{C}$ ) are used, is shown in Figure 8.

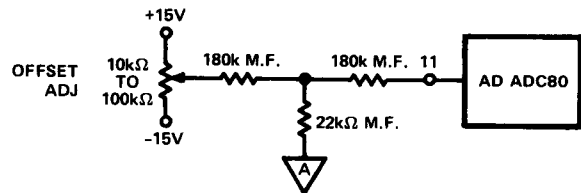


Figure 8. Low Tempco Zero Adjustment Circuit

In either zero adjust circuit, the fixed resistor connected to pin 11 should be located close to this pin to keep the pin 11 connection runs short (Comparator Input pin 11 is quite sensitive to external noise pick-up).

## GAIN ADJUSTMENT

The gain adjust circuit consists of a potentiometer connected across  $\pm V_S$  with its slider connected through a  $10\text{M}\Omega$  resistor to the gain adjust pin 16 as shown in Figure 9.

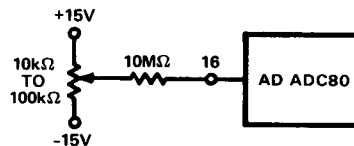


Figure 9. Gain Adjustment Circuit

An alternate gain adjust circuit which contributes negligible gain tempco if metal film resistors (Tempco  $< 100\text{ppm}/^\circ\text{C}$ ) are used is shown in Figure 10.

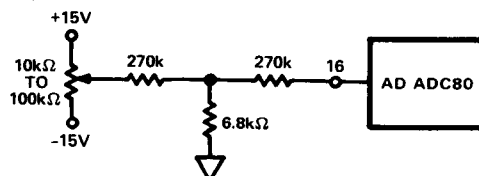


Figure 10. Low Tempco Gain Adjustment Circuit

## THEORY OF OPERATION

On receipt of a CONVERT START command, the AD ADC80 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

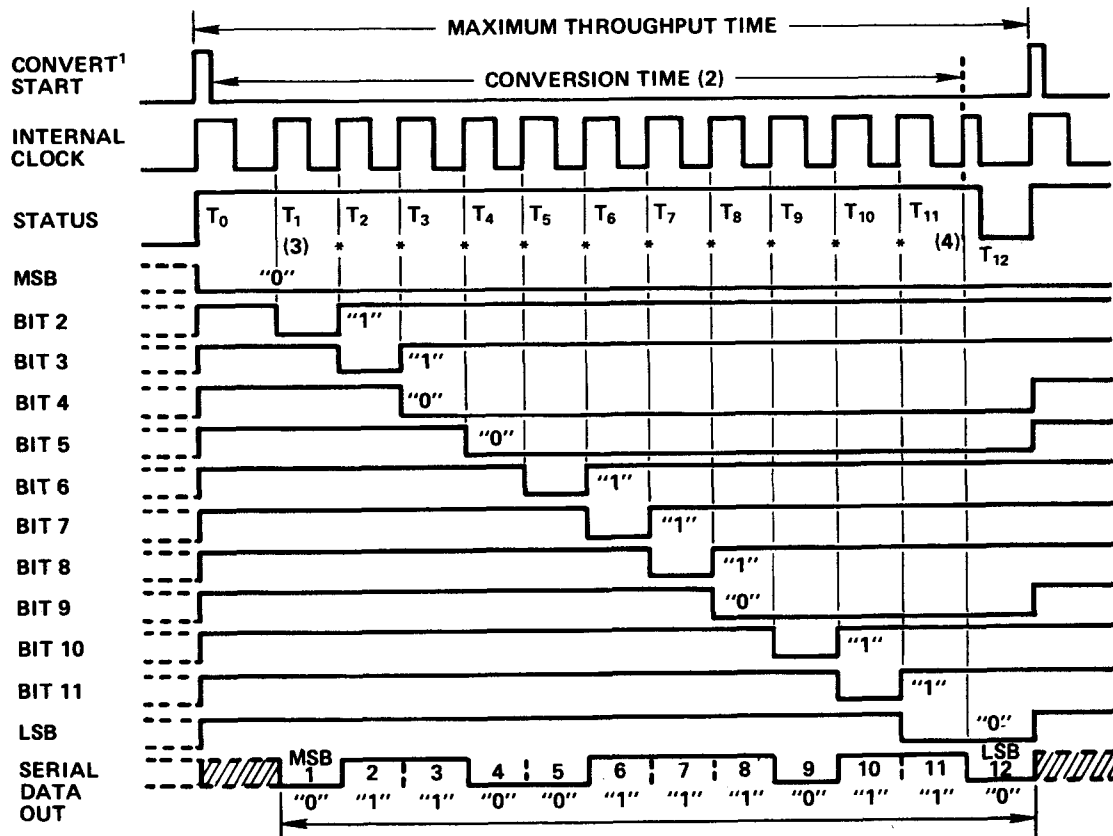
## TIMING

The timing diagram is shown in Figure 11. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time  $t_0$ ,

$B_1$  is reset and  $B_2 - B_{12}$  are set unconditionally. At  $t_1$  the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At  $t_2$ , the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at  $t_{12}$ . After a 40ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 11).

Incorporation of this 40ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.



### NOTES:

1. THE CONVERT START PULSE WIDTH IS 100ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "RISING EDGE" OF THE CONVERT COMMAND.
2. 25 $\mu$ s FOR 12 BITS AND 21 $\mu$ s FOR 10 BITS.
3. MSB DECISION
4. LSB DECISION 40ns PRIOR TO THE STATUS GOING LOW

\*BIT DECISIONS

Figure 11. Timing Diagram (Binary Code 011001110110)



## DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complemented two's complement binary, depending on whether BIT 1 (pin 6) or its logical inverse BIT 1 (pin 8) is used as the MSB. Parallel data becomes valid approximately 40ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in Figure 11. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 11. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

**Short Cycle Input:** A Short Cycle Input, pin 21, permits the timing cycle shown in Figure 11 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 21 is connected to +5V (pin 9). When 10-bit resolution is desired, pin 21 is connected to Bit 11 output pin 28. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision ( $t_{10} + 40ns$  in timing diagram of Figure 11). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table I.

| Connect Short Cycle Pin 21 to Pin: | Resolution Bits | Resolution (% FSR) | Maximum Conversion Time ( $\mu s$ ) | Status Flag Reset |
|------------------------------------|-----------------|--------------------|-------------------------------------|-------------------|
| 9                                  | 12              | 0.024              | 25                                  | $t_{12} + 40ns$   |
| 28                                 | 10              | 0.100              | 21                                  | $t_{10} + 40ns$   |
| 30                                 | 8               | 0.390              | 17                                  | $t_8 + 40ns$      |

Table I. Short Cycle Connections

## INPUT SCALING

The AD ADC80 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 12 for circuit details.

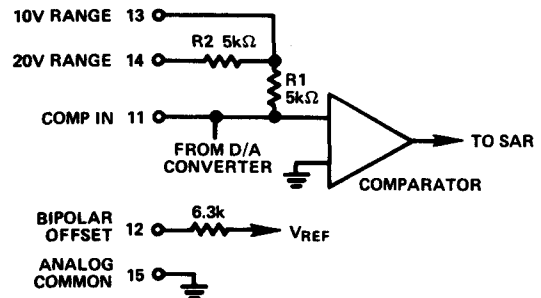


Figure 12. AD ADC80 Input Scaling Circuit

| Input Signal Range | Output Code | Connect Pin 12 To Pin | Connect Pin 14 To | Connect Input Signal To |
|--------------------|-------------|-----------------------|-------------------|-------------------------|
| $\pm 10V$          | COB or CTC  | 11                    | Input Signal      | 14                      |
| $\pm 5V$           | COB or CTC  | 11                    | Open              | 13                      |
| $\pm 2.5V$         | COB or CTC  | 11                    | Pin 11            | 13                      |
| 0V to +5V          | CSB         | 15                    | Pin 11            | 13                      |
| 0V to +10V         | CSB         | 15                    | Open              | 13                      |

Table II. AD ADC80 Input Scaling Connections

## Binary (BIN) Output

### Analog Input Voltage Range

### Code Designation

### One Least Significant Bit (LSB)

### Transition Values

### MSB

### LSB

### 000 ... 000\*\*\*\*

### 011 ... 111

### 111 ... 110

## INPUT VOLTAGE RANGE AND LSB VALUES

| Defined As:                     | $\pm 10V$         | $\pm 5V$          | $\pm 2.5V$       | 0V to +10V        | 0V to +5V        |
|---------------------------------|-------------------|-------------------|------------------|-------------------|------------------|
| Code                            | COB*              | COB*              | COB*             | CSB***            | CSB***           |
| Designation                     | or CTC**          | or CTC**          | or CTC**         |                   |                  |
| One Least Significant Bit (LSB) | $\frac{20V}{2^n}$ | $\frac{10V}{2^n}$ | $\frac{5V}{2^n}$ | $\frac{10V}{2^n}$ | $\frac{5V}{2^n}$ |
| Transition Values               |                   |                   |                  |                   |                  |
| MSB                             |                   |                   |                  |                   |                  |
| LSB                             |                   |                   |                  |                   |                  |
| 000 ... 000****                 | +Full Scale       | +10V -3/2LSB      | +5V -3/2LSB      | +2.5V -3/2LSB     | +10V -3/2LSB     |
| 011 ... 111                     | Mid Scale         | 0                 | 0                | 0                 | +5V              |
| 111 ... 110                     | -Full Scale       | -10V +1/2LSB      | -5V +1/2LSB      | -2.5V +1/2LSB     | 0 +1/2LSB        |

## NOTES:

\*COB = Complementary Offset Binary

\*\*CTC = Complementary Two's complement—obtained by using the complement of the most significant bit (MSB). MSB is available on pin 8.

\*\*\*CSB = Complementary Straight Binary.

\*\*\*\*Voltages given are the nominal value for transition to the code specified.

Table III. Input Voltages and Code Definitions

## GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD ADC80. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD ADC80's supply terminals should be capacitively decoupled as close to the AD ADC80 as possible. A large value capacitor such as  $1\mu\text{F}$  in parallel with a  $0.1\mu\text{F}$  capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

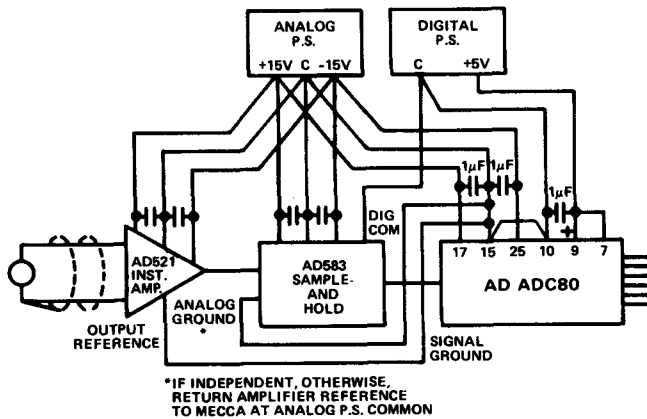


Figure 13. Basic Grounding Practice

## CONTROL MODES

The timing sequence of the AD ADC80 allows the device to be easily operated in a variety of systems with different control modes. The most common control modes are illustrated in Figures 14-17.

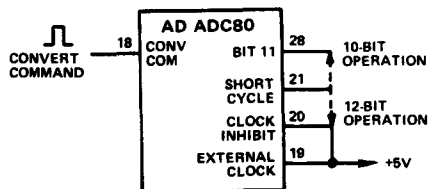


Figure 14. Internal Clock—Normal Operating Mode. Conversion Initiated by the Rising Edge of the Convert Command. The Internal Clock Runs Only During Conversion.

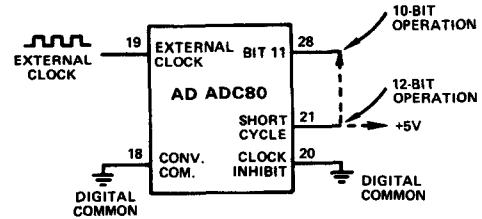


Figure 15. Continuous Conversion with External Clock. Conversion is Initiated by 14th Clock Pulse. Clock runs Continuously.

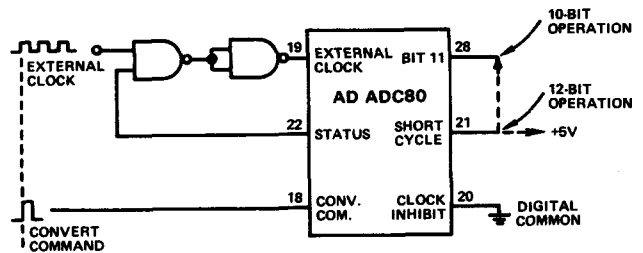


Figure 16. Continuous External Clock. Conversion Initiated by Rising Edge of Convert Command. The Convert Command must be Synchronized with Clock.

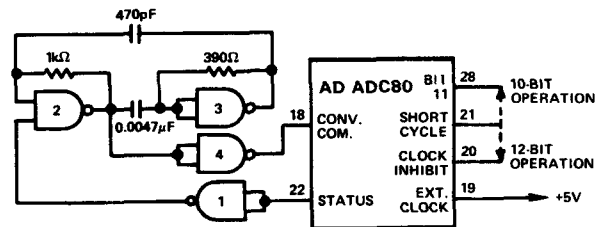


Figure 17. Continuous Conversion with Internal Clock. Conversion is Initiated by the 14th Clock Pulse. Clock Runs Continuously. The Oscillator Formed by Gates 2 and 3 Insures that the Conversion Process will Start When Logic Power is First Turned On.

## CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 18 and 19, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and  $-FS$  for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

**0 to +10V Range:** Set analog input to  $+1LSB = +0.0024V$ . Adjust Zero for digital output = 1111111110. Zero is now calibrated. Set analog input to  $+FSR -2LSB = +9.9952V$ . Adjust Gain for 0000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to  $+5.0000V$ ; digital output code should be 0111111111.

**-10V to +10V Range:** Set analog input to  $-9.9951V$ ; adjust Zero for 1111111110 digital output (complementary offset binary) code. Set analog input to  $+9.9902V$ ; adjust Gain for 0000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to  $0.0000V$ ; digital output (complementary offset binary) code should be 0111111111.

**Other Ranges:** Representative digital coding for 0 to +10V and -10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V,  $-2.5V$  to  $+2.5V$  and  $-5V$  to  $+5V$  ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately  $\pm 1/4LSB$  using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 3.

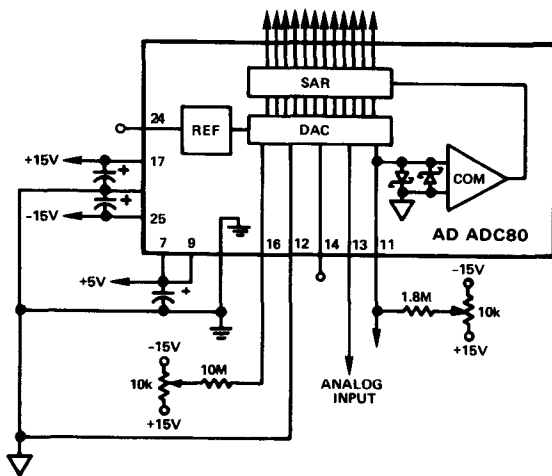


Figure 18. Analog and Power Connections for Unipolar 0-10V Input Range

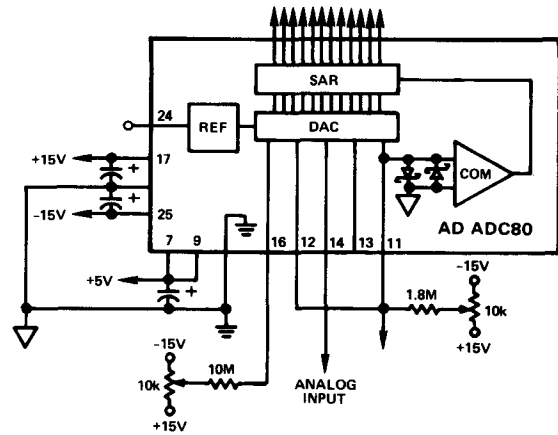


Figure 19. Analog and Power Connections for Bipolar  $\pm 10V$  Input Range

## MULTICHANNEL CONVERSION

In multichannel conversion systems, elements of the acquisition chain may be shared by two or more input sources. This sharing may occur in a number of ways, depending on the desired properties of the multiplexed system.

The data acquisition system shown in Figure 20 is a low cost solution to digitizing data from many analog channels. For most efficient use of time, the multiplexer is acquiring the next channel to be converted while the sample-hold is holding the previous output level for conversion. When conversion is complete, the status line from the converter causes the S/H to return to the sample mode and acquire the new data. After the acquisition time is completed, the sample hold can be switched to hold. A conversion can then begin and the multiplexer can be switched to the next channel.

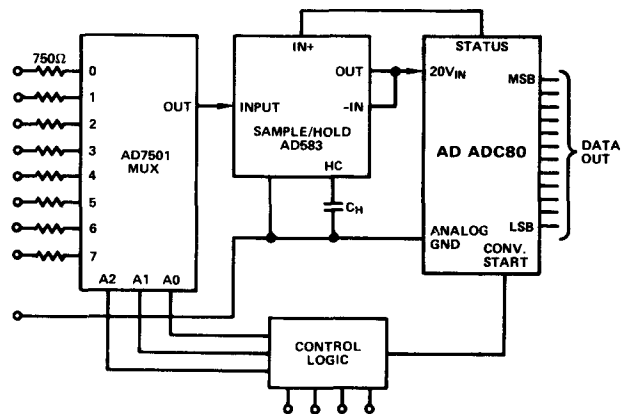


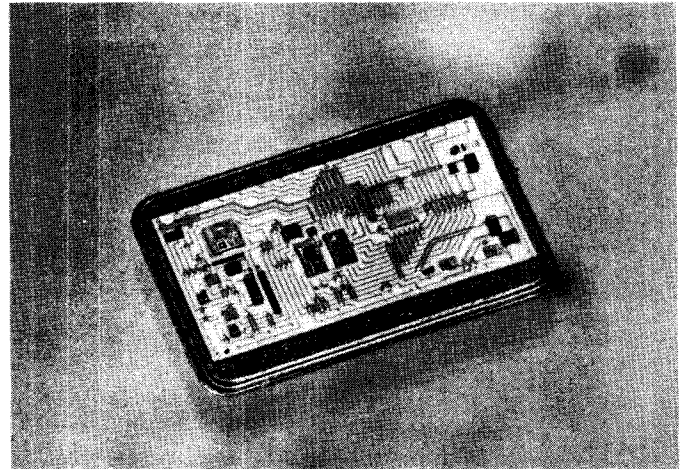
Figure 20. Data Acquisition System

### FEATURES

- Conversion Times as Low as  $1.2\mu\text{s}$
- Resolution: 8, 10 and 12 Bits
- Exceptional Accuracy, 0.012% of F.S.
- Low Power
- Contained in Glass or Metal 32-Pin DIP
- Adjustment-Free Operation

### APPLICATIONS

- Waveform Analysis
- Fast Fourier Transforms
- Radar



### GENERAL DESCRIPTION

With a typical conversion time of only  $2.2\mu\text{s}$  for complete 12-bit conversion, the Analog Devices' HAS series hybrid A/D converters are the fastest, smallest, most complete successive-approximation A/D's available. Housed in 32-pin DIP packages, these converters feature laser trimming for accuracy and linearity surpassing the best modular competitive A/D's. This series offers a unique combination of flexibility and simplicity which allows them to be used as stand-alone A/D converters requiring no additional external potentiometers and needing only an analog input signal and encode command for operation.

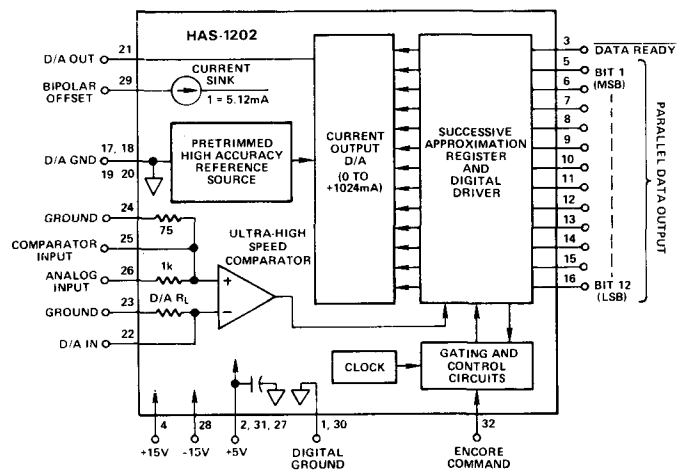
The HAS-1202 A/D features an accuracy of 0.012% and when combined with an HTC-0300 track-and-hold, forms an A/D conversion system capable of up to 350kHz sampling rates.

The HAS series A/D's are ideally suited for applications requiring excellent performance characteristics, small size, low power consumption and adjustment-free operation. Some of these applications include radar, PCM, data-acquisition, and digital-signal-processing systems where FFT's and other digital processing techniques are to be performed on analog input data.

For the ultra-high reliability requirements of military and aerospace applications these A/D's are optionally available with hermetically sealed metal cases and with MIL-STD-883 processing.

Extreme care in circuit layout should be exercised when using these hybrids in order to obtain rated performance. In particular, input and output runs should be as short as possible, a ground plane should be used to tie all ground pins together, and power supplies should be bypassed as close to the hybrid

circuit power supply pins as possible. Do not allow input or other analog signal lines to be in close proximity to or cross over any digital output line.



- NOTES:
1. FUNCTIONAL CONFIGURATION SHOWN IS FOR THE HAS-1202. FOR THE HAS-1002 PINS 15 AND 16 ARE NOT CONNECTED INTERNALLY. FOR HAS-0802 PINS 13, 14, 15 AND 16 ARE NOT CONNECTED INTERNALLY.
  2. FOR BIPOLAR OPERATION, CONNECT PIN 21 TO PIN 29. FOR UNIPOLAR OPERATION, LEAVE PIN 21 OPEN AND GROUND PIN 29.

*Block Diagram – HAS Series*

# SPECIFICATIONS (typical @ +25°C with nominal voltages unless otherwise noted)

| MODEL   | UNITS        | HAS-0802   | HAS-1002  | HAS-1202  |
|---|--------------|--|-----------|-----------|
| <b>RESOLUTION</b>                                   |              |  |           |           |
| LSB Weight  | BITS         | 8  | 10        | 12        |
|   | % Full Scale | 0.4  | 0.1       | 0.025     |
|   | mV           | 40   | 10        | 2.5       |
| <b>RELATIVE ACCURACY (INCLUDING LINEARITY)</b>      |              |  |           |           |
| Quantization Error                                  | % Full Scale | 0.05   | 0.025     | 0.012     |
|   | LSB          | ±1/2   | *         | *         |
| <b>LINEARITY VS. TEMPERATURE</b>                    |              |  |           |           |
|   | ppm/°C       | 3  | *         | *         |
|   |              | (No Missing Codes over Temperature Range)  |           |           |
| <b>INPUT OFFSET VOLTAGE</b>                         |              |  |           |           |
| Initial (Trimmable to Zero)                         | mV           | 10   | *         | *         |
| Zero Offset vs. Temperature                         | μV/°C        | 15   | *         | *         |
| Bipolar Offset vs. Temperature                      | μV/°C        | 100  | *         | *         |
| <b>GAIN ERROR</b>                                   |              |  |           |           |
| Initial (Trimmable to Zero)                         | % Full Scale | 0.1  | *         | *         |
| Gain vs. Temperature                                | ppm/°C       | 30   | *         | *         |
| <b>INPUT</b>  |              |  |           |           |
| Ranges (Full Scale)                                 |              |  |           |           |
| "Built-In" Standard Unipolar                        | V ±0.1%      | +10.24   | *         | *         |
| Bipolar   | V ±0.05%     | ±5.12  | *         | *         |
| Resistor Programmable (See Figure 3)                | V, 0 to:     | +5, +7.5, +15, +20, ±2.5, ±3.75, ±7.5, ±10   | *         | *         |
| Impedance   | Ω min        | 1000   | *         | *         |
| Overvoltage   | V            | Two Times Full Scale + or -  |           |           |
| <b>CONVERSION TIME (COMPLETE CYCLE TIME)</b>        |              |  |           |           |
|   | μs max (typ) | 1.5 (1.2)  | 1.7 (1.4) | 2.8 (2.2) |
| <b>CONVERSION RATE</b>                              |              |  |           |           |
|   | kHz max      | 667  | 558       | 357       |
| <b>ENCODE COMMAND – TTL LOGIC INPUT</b>             |              |  |           |           |
| Logic Levels (Positive Logic) Function <sup>1</sup> | V            | "0" = 0 to +0.4, "1" = +2 to +5<br>Logic "1" Resets Converter<br>Logic "0" Starts Conversion   |           |           |
| Loading   |              | 1 Standard TTL Load:<br>"0" = -1.6mA, max<br>"1" = 40μA, max   |           |           |
| Pulse Width   | ns min       | 100  | *         | *         |
| Repetition Rate                                     |              | 0 to Maximum Conversion Rate   |           |           |
| <b>LOGIC OUTPUTS</b>                                |              |  |           |           |
| Data Ready (DR) Function                            |              | Signals conversion is complete when low.<br>After DR goes low, data is valid. A new conversion may be initiated at this time. DR may be used to strobe data into external register if adequate register setup time is allowed.<br>See Figure 1 |           |           |
| Timing Loading Parallel Data Format                 |              | 5 Standard TTL Loads, max<br><br>8-, 10-, or 12-bits parallel data. Valid from time DR output goes low until 20ns after receipt of next encode command.  |           |           |
| Logic Levels  |              | TTL Compatible:<br>"0" = 0V to +0.4V<br>"1" = +2.4V to +5V   |           |           |
| Loading   |              | Will drive up to 5 Standard TTL Loads or 2 TTL "S" or "H" Loads.   |           |           |
| Coding <sup>2</sup>                                 |              | Offset Binary (BIN) for Unipolar Inputs:<br>+10.24V = 1 1 1 1 . . . . 1<br>0V = 0 0 0 0 . . . . 0<br>Offset Binary (OBN) for Bipolar Inputs:<br>+5.12V = 1 1 1 1 . . . . 1<br>0V = 0 1 1 1 . . . . 1<br>-5.12V = 0 0 0 0 . . . . 0             |           |           |
| <b>POWER REQUIREMENTS</b>                           |              |  |           |           |
| +14.5V to +15.5V (+18V Absolute Max)                | mA           | 40   | *         | *         |
| -14.5V to -15.5V (-18V Absolute Max)                | mA           | 15   | *         | *         |
| +4.75V to +5.25V (+7V Absolute Max)                 | mA           | 200  | *         | *         |
| <b>TEMPERATURE RANGE</b>                            |              |  |           |           |
| Operating   | °C           | 0 to +70   | *         | *         |
| Storage   | °C           | -55 to +125  | *         | *         |

## NOTES:

<sup>1</sup>After converter is reset, all other logic signals, including clock, are internally generated.

<sup>2</sup>When HAS series A/D's are used with HTC-0300 track/hold, output coding is complementary binary (CBN) for unipolar inputs and complementary offset binary (COB) for bipolar inputs (see Table 1).

\*Specifications same as model HAS-0802.

Specifications subject to change without notice.

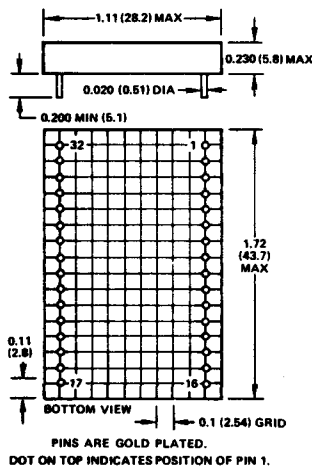
Table 1. Output Coding\*

| SCALE                     | INPUT OF HTC-0300 | INPUT OF HAS-1202 | DIGITAL OUTPUT |
|---------------------------|-------------------|-------------------|----------------|
| <b>UNIPOLAR OPERATION</b> |                   |                   |                |
| FS-1LSB                   | -10.2375V         | +10.2375V         | 111111111111   |
| 3/4 FS                    | - 7.6800V         | + 7.6800V         | 110000000000   |
| 1/2 FS                    | - 5.1200V         | + 5.1200V         | 100000000000   |
| 1/4 FS                    | - 2.5600V         | + 2.5600V         | 010000000000   |
| +1LSB                     | - 0.0025V         | + 0.0025V         | 000000000001   |
| 0                         | 0.0000V           | 0.0000V           | 000000000000   |
| <b>BIPOLAR OPERATION</b>  |                   |                   |                |
| +FS-1LSB                  | - 5.1175V         | + 5.1175V         | 111111111111   |
| 0                         | 0.0000V           | 0.0000V           | 100000000000   |
| -FS+1LSB                  | + 5.1175V         | - 5.1175V         | 000000000001   |
| -FS                       | + 5.1200V         | - 5.1200V         | 000000000000   |

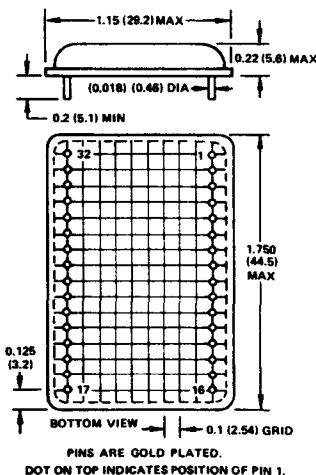
\*Coding and input levels shown are for HAS-1202. For 8- and 10-bit A/D's the input levels are less by the values of the LSB weight for each type, and the digital output will show only 8 or 10 bits, respectively.

**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).



**GLASS PACKAGE**



**METAL PACKAGE (M)  
(OPTIONAL)**

**PIN DESIGNATIONS**

**HAS-1202\***

| PIN        | FUNCTION            |
|------------|---------------------|
| 1, 30      | DIGITAL GROUND      |
| 2, 27, 31  | +5V                 |
| 3          | DATA READY          |
| 4          | +15V                |
| 5          | BIT 1 OUTPUT (MSB)  |
| 6          | BIT 2 OUTPUT        |
| 7          | BIT 3 OUTPUT        |
| 8          | BIT 4 OUTPUT        |
| 9          | BIT 5 OUTPUT        |
| 10         | BIT 6 OUTPUT        |
| 11         | BIT 7 OUTPUT        |
| 12         | BIT 8 OUTPUT        |
| 13         | BIT 9 OUTPUT        |
| 14         | BIT 10 OUTPUT       |
| 15         | BIT 11 OUTPUT       |
| 16         | BIT 12 OUTPUT (LSB) |
| 17, 18, 19 | ANALOG GROUND       |
| 20, 23, 24 | ANALOG GROUND       |
| 25         | COMP INPUT          |
| 26         | ANALOG INPUT        |
| 28         | -15V                |
| 29         | BIPOLAR OFFSET      |
| 32         | ENCODE COMMAND      |

\*HAS-1002, PINS 15 AND 16 ARE NOT CONNECTED INTERNALLY.  
HAS-0802, PINS 13, 14, 15 AND 16 ARE NOT CONNECTED INTERNALLY.

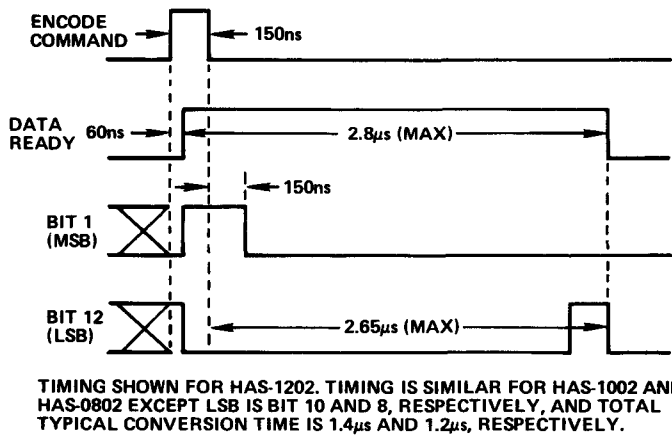


Figure 1. Timing Diagram (Typical)

Input Connections For Optional Input Ranges

| INPUT RANGE        | R1    | R2   | Z <sub>IN</sub> | ABSOLUTE MAXIMUM SIGNAL |
|--------------------|-------|------|-----------------|-------------------------|
| 0 to +5V, ±2.5V    | SHORT | 1000 | 500             | ±10V                    |
| 0 to +7.5V, ±3.75V | SHORT | 3000 | 750             | ±15V                    |
| 0 to +15V, ±7.5V   | 500   | OPEN | 1500            | ±30V                    |
| 0 to +20V, ±10V    | 1000  | OPEN | 2000            | ±40V                    |

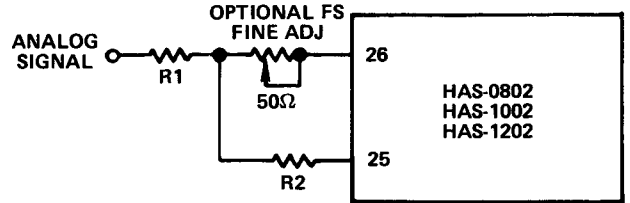


Figure 3. Full Scale Trim

APPLICATION CIRCUIT

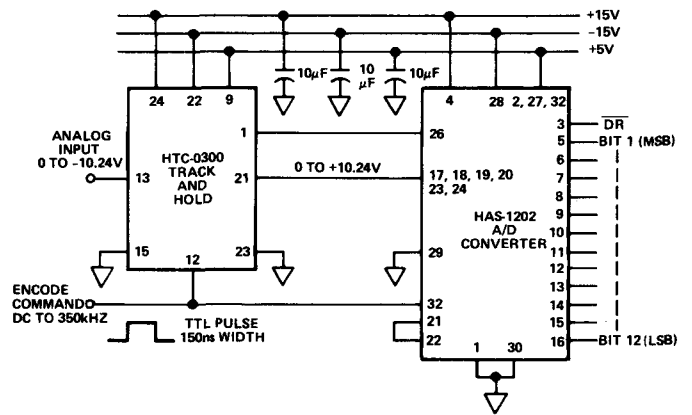
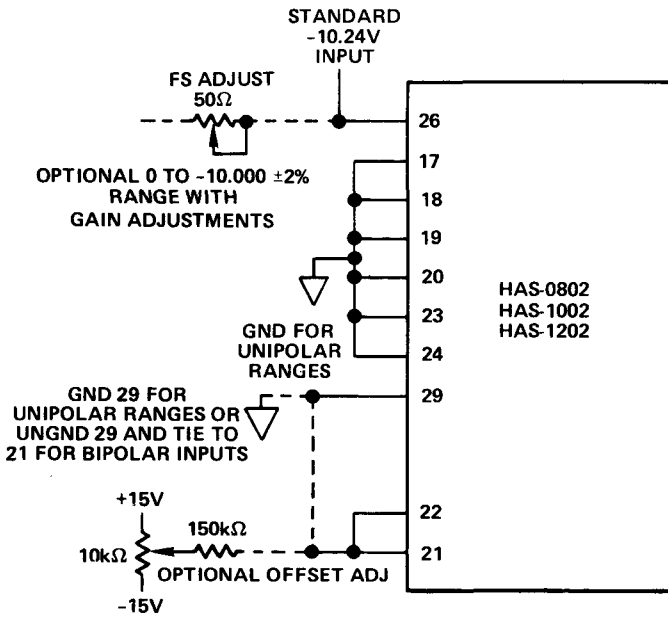


Figure 4. DC to 350kHz, 12-Bit, A/D Conversion System

ORDERING INFORMATION

Order model number HAS-0802, HAS-1002, or HAS-1202 for 8-, 10-, or 12-bit operation, respectively. Mating connector for the HAS series A/D's is model number HSA-2. Metal cased versions of this A/D with extended operating temperature range, and MIL-STD processing are also available. Consult the factory or nearest Analog Devices' sales office for further information.



NOTES:

- THIS CIRCUIT SHOWN FOR UNIPOLAR (0 TO -10.24V) INPUT. 0V INPUT = 000000000000; -10.24 INPUT = 111111111111.
- FOR BIPOLAR (±5.12V) INPUT, UNGROUND PIN 29 AND CONNECT PIN 29 TO PIN 21.
- FOR EXTRA-PRECISE GAIN (FULL-SCALE) ADJUSTMENT, CONNECT A 50Ω VARIABLE RESISTANCE IN SERIES WITH PIN 20 OF HAS-1202. THIS WILL RESULT IN 0 TO -10.000V INPUT WITH ADJUSTMENT RANGE OF ±2% OF FULL SCALE.
- FOR EXTRA-PRECISE ZERO OFFSET ADJUSTMENT, CONNECT 150k RESISTOR FROM PIN 21 TO THE TAP OF A 10k POTENTIOMETER. END TERMINATIONS OF POTENTIOMETER CONNECT TO +15V AND -15V. THIS ZERO OFFSET ADJUSTMENT WILL HAVE A RANGE OF APPROXIMATELY ±100mV.

Figure 2. Input Connections For Standard Input Ranges

### FEATURES

High Speed at Low Cost

8 Bits  $1\mu\text{s}$  max

10 Bits  $1.5\mu\text{s}$  max

12 Bits  $2\mu\text{s}$  max

No Missing Codes Over Temperature

Low Power

Industry Standard Pin Out

Parallel and Serial Outputs

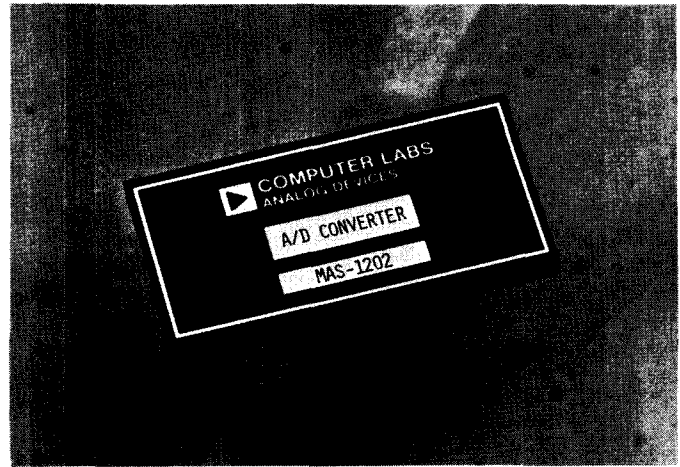
### APPLICATIONS

High Speed Data Acquisition

Real Time Waveform Analysis

Radar Signal Processing

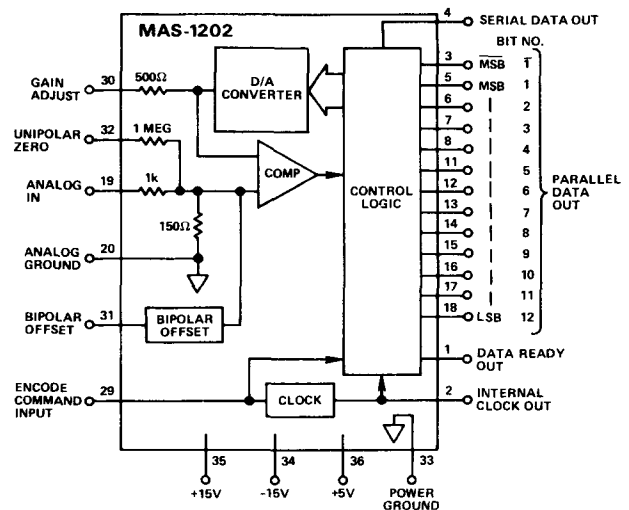
Analytical Instruments



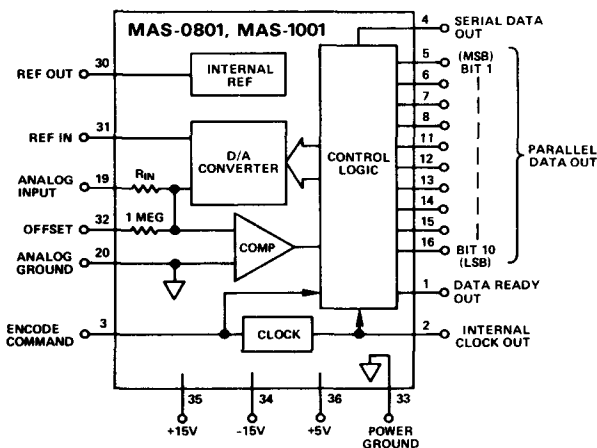
### GENERAL DESCRIPTION

The MAS series of high speed analog to digital converters represent the "state of the art" in application of the successive approximation conversion technique by providing highest speed at lowest cost. With monotonicity guaranteed over temperature these reliable modules are form, fit and function compatible with popular industry standards from Datal and Philbrick (for new designs consider the HAS series of hybrid converters).

In most applications these A/D's should be used with a fast sample hold such as the THS/THC series.



MAS-1202 Block Diagram



MAS-0801 and MAS-1001 Block Diagram



# SPECIFICATIONS (typical @ +25°C unless otherwise noted)

| Model   | Units     | MAS-0801   | MAS-1001 | MAS-1202    |
|---|-----------|--|----------|-------------|
| <b>RESOLUTION</b> FS = Full Scale                       | Bits      | 8  | 10       | 12          |
| <b>ACCURACY</b> (Relative to Full Scale)                | ±% FS     | 0.2  | 0.05     | 0.012       |
| Quantization Error                                      | LSB       | ±1/2   | *        | *           |
| Nonlinearity  | LSB (max) | ±1/2   | *        | *           |
| Differential Nonlinearity                               | LSB (max) | ±1/2   | *        | *           |
| Missing Codes   |           | No Missing Codes 0 to +70°C  |          |             |
| <b>TEMPERATURE COEFFICIENTS</b>                         |           |  |          |             |
| Differential Nonlinearity                               | ±ppm/°C   | 3  | *        | *           |
| Gain  | ±ppm/°C   | 20   | *        | 30          |
| Gain (Option-P)   | ±ppm/°C   | 5  | *        | NA          |
| Zero Offset (Unipolar)                                  | ±μV/°C    | 10   | *        | 100         |
| Zero Offset (Bipolar)                                   | ±ppm/°C   | 15   | *        | *           |
| Zero Offset (Option-P)                                  | ±ppm/°C   | 5  | *        | NA          |
| <b>INPUT</b>  |           |  |          |             |
| Ranges (Full Scale)                                     | Options   | MAS-0801 and MAS-1001 ONLY   |          | STANDARD    |
| MAS-XXXX-1  | V         | 0 to -5  | *        | 0 to +10/±5 |
| MAS-XXXX-2  | V         | 0 to -10   | *        | NA          |
| MAS-XXXX-3  | V         | ±5   | *        | NA          |
| MAS-XXXX-4  | V         | ±10  | *        | NA          |
| MAS-XXXX-5  | V         | ±1.024   | *        | NA          |
| Impedance (Function of Option)                          | Ω/V       | 100  | *        | 1150Ω       |
| <b>OVERVOLTAGE</b>                                      | V         | To Twice Peak Input FS Without Damage.   |          |             |
| <b>CONVERSION TIME</b> <sup>1</sup>                     | μs max    | 1  | 1.5      | 2           |
|   | μs typ    | 0.8  | 1.3      | 1.8         |
| <b>ENCODE COMMAND</b>                                   |           |  |          |             |
| Logic Levels (1 Standard TTL Load)<br>Function          | V         | "0" = 0 to +0.4, "1" = +2 to +5.5<br>Positive-going edge resets converter,<br>Trailing edge starts conversion for 8-<br>and 10-bit versions. |          |             |
| Duration (Width)  | ns min    | 50   | *        | 100         |
| Rise and Fall Times                                     | ns max    | 20   | *        | *           |
| Repetition Rate   | kHz max   | 1000   | 666      | 500         |
| <b>LOGIC OUTPUTS</b>                                    |           |  |          |             |
| Levels TTL (Same as Encode Command)<br>Drive Capability |           | Data and Data Ready – 4 Std TTL Loads,<br>Clock – 6TTL Loads   |          |             |
| Parallel Data   |           | 8, 10 or 12 lines of data held until next<br>Encode Command  |          |             |
| Coding (Unipolar)<br>(Bipolar)                          |           | CBN  | *        | BIN         |
|   |           | COB/2SC  | *        | OBN/2SC     |
| Serial Data   |           | MSB first, successive pulse output during<br>conversion, NRZ.  |          |             |
| Coding  |           | Same as parallel output except 2SC not<br>available.   |          |             |
| Clock   |           | Pulse train of 9, 11 or 13 internal clock<br>pulses, gated on during the conversion<br>period.   |          |             |
| <b>POWER REQUIREMENTS</b>                               |           |  |          |             |
| +14.5V to +15.5V  | mA        | 70   | *        | 80          |
| -14.5V to -15.5V  | mA        | 30   | *        | 20          |
| +5V ±5%   | mA        | 150  | *        | *           |
| <b>TEMPERATURE RANGE</b>                                |           |  |          |             |
| Operating   | °C        | 0 to +70   | *        | *           |
| Storage   | °C        | -55 to +85   | *        | *           |
| <b>PHYSICAL CHARACTERISTICS</b>                         |           |  |          |             |
| Case  |           | Diallyl Phthalate per MIL-M-14 Type SDC-F  |          |             |

**NOTE:**

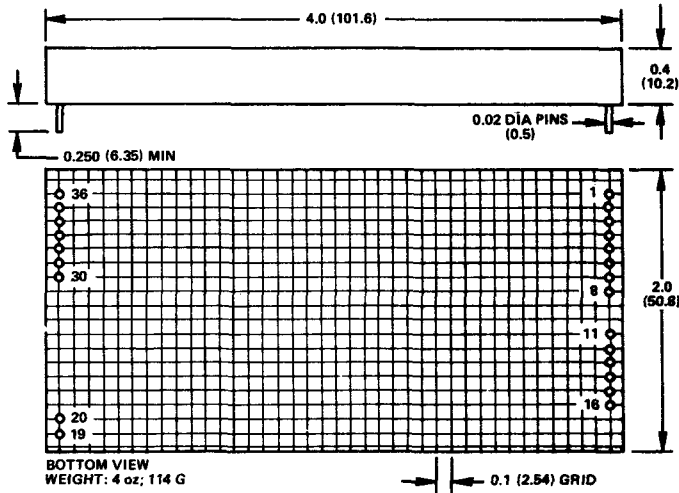
<sup>1</sup> Total conversion time from leading edge of encode command pulse to trailing edge of data ready pulse with 50ns wide encode command.

\*Specifications same as MAS-0801.

Specifications subject to change without notice.

### OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



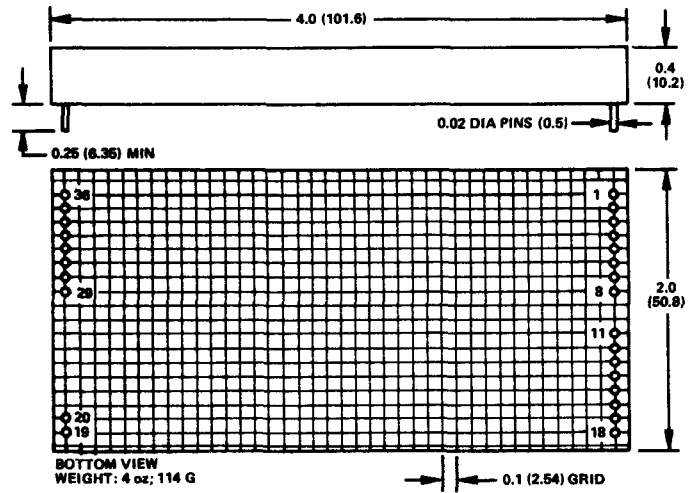
BOTTOM VIEW  
WEIGHT: 4 oz; 114 G

0.1 (2.54) GRID

NOTES:  
SOME MODELS DO NOT USE ALL PIN OUTS. IN THESE CASES, UNUSED PINS ARE DELETED.  
PINS ARE GOLD PLATED  
DOT ON TOP INDICATES POSITION OF PIN 1

### OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



BOTTOM VIEW  
WEIGHT: 4 oz; 114 G

0.1 (2.54) GRID

NOTES:  
PINS ARE GOLD PLATED  
DOT ON TOP INDICATES POSITION OF PIN 1

### PIN DESIGNATIONS MAS-0801, MAS-1001

| PIN | FUNCTION           | PIN | FUNCTION         |
|-----|--------------------|-----|------------------|
| 1   | DATA READY OUT     | 15  | BIT 9 OUT        |
| 2   | INTERNAL CLOCK OUT | 16  | BIT 10 OUT (LSB) |
| 3   | ENCODE COMMAND IN  | 19  | ANALOG INPUT     |
| 4   | SERIAL OUTPUT      | 20  | ANALOG GROUND    |
| 5   | BIT 1 OUT (MSB)    | 30  | REFERENCE OUT    |
| 6   | BIT 2 OUT          | 31  | REFERENCE INPUT  |
| 7   | BIT 3 OUT          | 32  | OFFSET           |
| 8   | BIT 4 OUT          | 33  | POWER GROUND     |
| 11  | BIT 5 OUT          | 34  | -15V POWER IN    |
| 12  | BIT 6 OUT          | 35  | +15V POWER IN    |
| 13  | BIT 7 OUT          | 36  | +5V POWER IN     |
| 14  | BIT 8 OUT          |     |                  |

### PIN DESIGNATIONS MAS-1202

| PIN | FUNCTION           | PIN | FUNCTION          |
|-----|--------------------|-----|-------------------|
| 1   | DATA READY         | 16  | BIT 10 OUT        |
| 2   | INTERNAL CLOCK OUT | 17  | BIT 11 OUT        |
| 3   | BIT 1 OUT (MSB)    | 18  | BIT 12 OUT (LSB)  |
| 4   | SERIAL DATA OUT    | 19  | ANALOG INPUT      |
| 5   | BIT 1 OUT (MSB)    | 20  | ANALOG GROUND     |
| 6   | BIT 2 OUT          | 29  | ENCODE COMMAND IN |
| 7   | BIT 3 OUT          | 30  | GAIN ADJUST       |
| 8   | BIT 4 OUT          | 31  | BIPOLAR OFFSET    |
| 11  | BIT 5 OUT          | 32  | UNIPOLAR ZERO     |
| 12  | BIT 6 OUT          | 33  | POWER GROUND      |
| 13  | BIT 7 OUT          | 34  | -15V POWER IN     |
| 14  | BIT 8 OUT          | 35  | +15V POWER IN     |
| 15  | BIT 9 OUT          | 36  | +5V POWER IN      |

### ORDERING INFORMATION

The 8- and 10-bit versions of the MAS series may be ordered with various options according to the chart below.

**MAS-0801**  
RESOLUTION  
AND ACCURACY

MAS-0801 = 8 Bits  
MAS-1001 = 10 Bits

**P**  
TEMPCO

For  $\pm 5\text{ppm}/^\circ\text{C}$   
tempco at slightly  
higher cost, add  
"P". For standard  
tempco, leave blank.

**-1**  
ANALOG INPUT  
RANGE

-1 0 to -5V FS  
-2 0 to -10V FS  
-3  $\pm 5\text{V}$  FS  
-4  $\pm 10\text{V}$  FS  
-5  $\pm 1.024\text{V}$  FS

**-CBN**  
LOGIC OUTPUT  
CODING  
(See Note 1)

CBN = Complementary  
Binary (Options  
1 and 2)  
COB = Complementary  
Offset Binary  
(Options 3, 4 and 5)  
C2SC = Complementary  
Two's Comple-  
ment (Options  
3, 4 and 5)

NOTES:  
For 12-bit performance order the MAS-1202 which has no options.  
The mating connector for the MAS series is the MSA-1.

## OUTPUT CODING

The logic output coding is shown true relative to the analog input to the A/D. If an inverting track and hold—such as the Analog Devices THC series—or an inverting op amp is used ahead of the A/D, the true logic coding is inverted relative to the system input. This yields the systemic coding as follows:

| Scale     | Input Voltage | Complementary Straight Binary |
|-----------|---------------|-------------------------------|
| -FS -1LSB | -9.9900V      | 1111 1111 11                  |
| -3/4 FS   | -7.5000V      | 1100 0000 00                  |
| -1/2 FS   | -5.0000V      | 1000 0000 00                  |
| -1/4 FS   | -2.5000V      | 0100 0000 00                  |
| -1LSB     | -0.0010V      | 0000 0000 01                  |
| 0         | 0.0000V       | 0000 0000 00                  |

### NOTE

(0 to -10V) for MAS-1001-2; LSB = 10mV for MAS-1001-1, apply input voltage factor of 1/2.

Table 1. MAS-0801 and MAS-1001 Unipolar Operation for Options 1 and 2

| Scale     | Input Voltage | Complementary Offset Binary | Complementary Two's Complement |
|-----------|---------------|-----------------------------|--------------------------------|
| -FS -1LSB | -1.022V       | 1111 1111 11                | 0111 1111 11                   |
| -1/2 FS   | -0.512V       | 1100 0000 00                | 0100 0000 00                   |
| 0         | -0.000V       | 1000 0000 00                | 0000 0000 00                   |
| +1/2 FS   | +0.512V       | 0100 0000 00                | 1100 0000 00                   |
| +FS       | +1.024V       | 0000 0000 00                | 1000 0000 00                   |

### NOTE

(-1.024V to +1.024V) for MAS-1001-5; LSB = 2mV.

Table 3. MAS-0801 and MAS-1001 Bipolar Operation for Option 5

| Scale     | Input Voltage | Straight Binary | Two's Complement |
|-----------|---------------|-----------------|------------------|
| +FS -1LSB | +4.9976V      | 1111 1111 1111  | 0111 1111 1111   |
| +3/4 FS   | +3.7500V      | 1110 0000 0000  | 0110 0000 0000   |
| +1/2 FS   | +2.5000V      | 1100 0000 0000  | 0100 0000 0000   |
| 0         | 0.0000V       | 1000 0000 0000  | 0000 0000 0000   |
| -1/2 FS   | -2.5000V      | 0100 0000 0000  | 1100 0000 0000   |
| -3/4 FS   | -3.7500V      | 0010 0000 0000  | 1010 0000 0000   |
| -FS +1LSB | -4.9976V      | 0000 0000 0001  | 1000 0000 0001   |
| -FS       | -5.0000V      | 0000 0000 0000  | 1000 0000 0000   |

### NOTE

In Table 5, TWO'S COMPLEMENT (2SC) is accomplished by using the MSB output for Bit 1.

Table 5. MAS-1202 Bipolar Operation (-5V to +5V)

Binary (BIN) in place of Complementary Binary (CBN) for options 1 and 2; Offset Binary (OBN) in place of Complementary Offset Binary (COB) for options 3, 4 and 5; Two's Complement (2SC) in place of Complementary Two's Complement (C2SC).

| Scale     | Input Voltage | Complementary Offset Binary | Complementary Two's Complement |
|-----------|---------------|-----------------------------|--------------------------------|
| -FS -1LSB | -4.9900V      | 1111 1111 11                | 0111 1111 11                   |
| -3/4 FS   | -3.7500V      | 1110 0000 00                | 0110 0000 00                   |
| -1/2 FS   | -2.5000V      | 1100 0000 00                | 0100 0000 00                   |
| 0         | 0.0000V       | 1000 0000 00                | 0000 0000 00                   |
| +1/2 FS   | +2.5000V      | 0100 0000 00                | 1100 0000 00                   |
| +3/4 FS   | +3.7500V      | 0010 0000 00                | 1010 0000 00                   |
| +FS -1LSB | +4.9900V      | 0000 0000 01                | 1000 0000 01                   |
| +FS       | +5.0000V      | 0000 0000 00                | 1000 0000 00                   |

### NOTES:

(-5V to +5V) for MAS-1001-3; LSB = 10mV for MAS-1001-4 apply input voltage factor of 2.

In Table 2, complementary 2SC is accomplished by factory option.

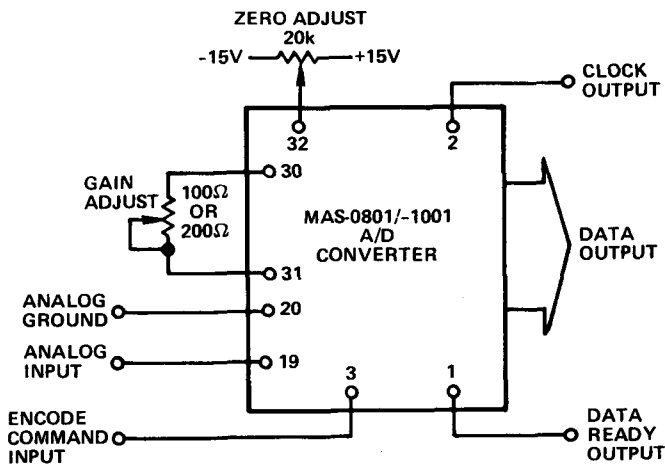
Table 2. MAS-0801 and MAS-1001 Bipolar Operation for Options 3 and 4

| Scale     | Input Voltage | Straight Binary |
|-----------|---------------|-----------------|
| +FS -1LSB | +9.9976V      | 1111 1111 1111  |
| +7/8 FS   | +8.7500V      | 1110 0000 0000  |
| +3/4 FS   | +7.5000V      | 1100 0000 0000  |
| +1/2 FS   | +5.0000V      | 1000 0000 0000  |
| +1/4 FS   | +2.5000V      | 0100 0000 0000  |
| +1LSB     | +0.0024V      | 0000 0000 0001  |
| 0         | 0.0000V       | 0000 0000 0000  |

### NOTE

Unipolar Operation (0 to +10V)

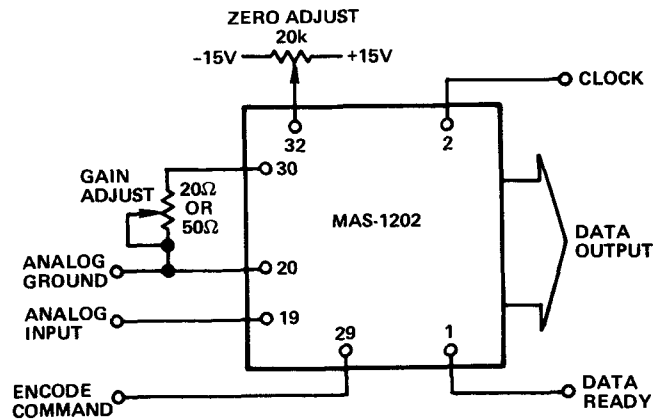
Table 4. MAS-1202 Unipolar Operation (0 to +10V)



**PROCEDURE:**

1. APPLY ENCODE COMMAND PULSE TO THE ENCODE COMMAND INPUT (PIN 3).
2. CONNECT A PRECISION VOLTAGE SOURCE TO THE ANALOG INPUT (PIN 19) AND ANALOG GROUND (PIN 20). ADJUST THIS SOURCE FOR  $+1/2\text{LSB}$  ( $+1.2\text{mV}$ ). VARY THE ZERO ADJUST POTENTIOMETER FOR AN LSB FLUTTER (THIS WILL APPEAR AS AN EQUAL UNCERTAINTY AT THE OUTPUT BETWEEN THE CODES 0000 0000 AND 0000 0001).
3. WITH THE PRECISION VOLTAGE SOURCE ADJUSTED TO  $-FS + 1/2\text{LSB}$ , ADJUST THE GAIN POTENTIOMETER FOR A FLUTTER BETWEEN CODES 1111 1110 AND 1111 1111.

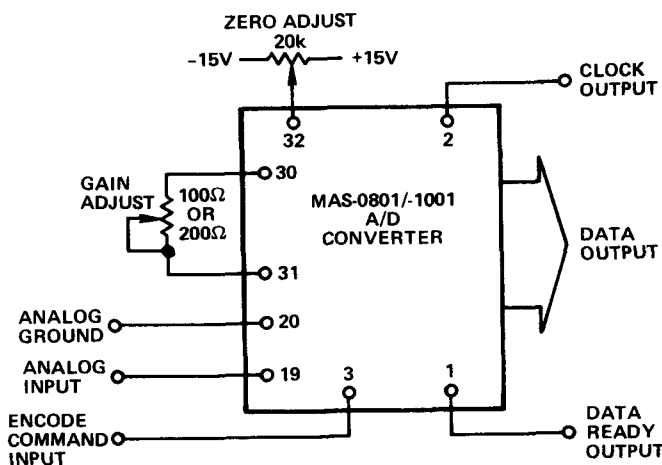
Figure 1. MAS-0801 and MAS-1001 Unipolar Operation



**PROCEDURE:**

1. APPLY ENCODE COMMAND PULSE TO THE ENCODE COMMAND INPUT (PIN 29).
2. CONNECT A PRECISION VOLTAGE SOURCE TO THE ANALOG INPUT (PIN 19) AND ANALOG GROUND (PIN 20). ADJUST THIS SOURCE FOR  $+1/2\text{LSB}$  ( $+1.2\text{mV}$ ). VARY THE ZERO ADJUST POTENTIOMETER FOR BIT 12 FLUTTER (THIS WILL APPEAR AS AN EQUAL UNCERTAINTY AT THE OUTPUT BETWEEN THE CODES 0000 0000 0000 AND 0000 0000 0001).
3. WITH THE PRECISION VOLTAGE SOURCE ADJUSTED TO  $+FS - 1/2\text{LSB}$  ( $+9.9964\text{V}$ ), ADJUST THE GAIN POTENTIOMETER FOR A FLUTTER BETWEEN CODES 1111 1111 1110 AND 1111 1111 1111.

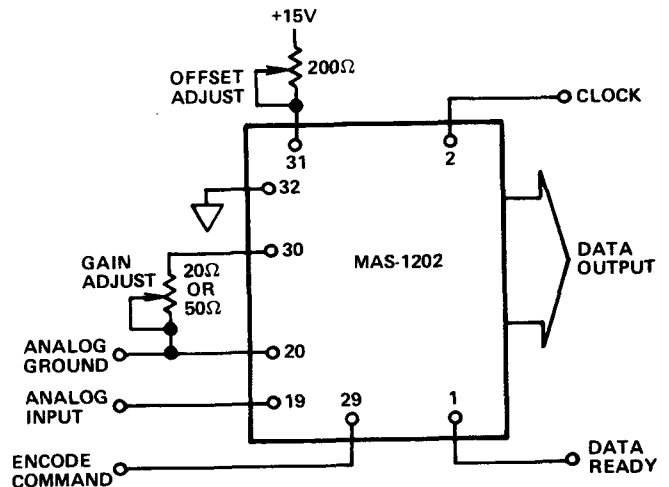
Figure 3. MAS-1202 Unipolar Operation



**PROCEDURE:**

1. APPLY AN ENCODE COMMAND TO THE ENCODE COMMAND INPUT (PIN 3).
2. CONNECT A PRECISION VOLTAGE SOURCE TO THE ANALOG INPUT (PIN 19) AND ANALOG GROUND (PIN 20). ADJUST THIS SOURCE TO  $+FS - 1/2\text{LSB}$ . THE ZERO ADJUST POTENTIOMETER FOR A FLUTTER BETWEEN VARY CODES 0000 0000 AND 0000 0001.
3. ADJUST THE VOLTAGE SOURCE TO  $-FS + 1/2\text{LSB}$ . ADJUST THE GAIN POTENTIOMETER FOR A FLUTTER BETWEEN THE CODES 1111 1110 AND 1111 1111.

Figure 2. MAS-0801 and MAS-1001 Bipolar Operation



**PROCEDURE:**

1. APPLY AN ENCODE COMMAND TO THE ENCODE COMMAND INPUT (PIN 29).
2. CONNECT A PRECISION VOLTAGE SOURCE TO THE ANALOG INPUT (PIN 19) AND ANALOG GROUND (PIN 20). ADJUST THIS SOURCE TO  $-FS + 1/2\text{LSB}$  ( $-4.9988\text{V}$ ). ADJUST THE OFFSET POTENTIOMETER FOR A FLUTTER BETWEEN CODES 0000 0000 0000 AND 0000 0000 0001.
3. ADJUST THE VOLTAGE SOURCE TO  $+FS - 1/2\text{LSB}$  ( $+4.9964\text{V}$ ). ADJUST THE GAIN POTENTIOMETER FOR A FLUTTER BETWEEN THE CODES 1111 1111 1110 AND 1111 1111 1111.

Figure 4. MAS-1202 Bipolar Operation

# APPLICATIONS

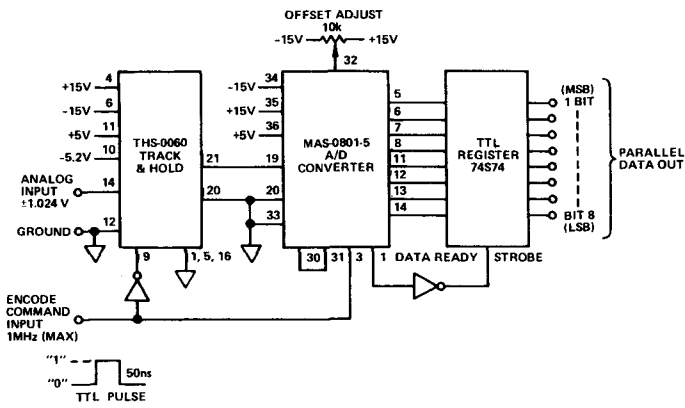


Figure 5. Depicts a Complete 8-Bit, 1MHz Conversion System Using the THS-0060 Track-and-Hold and the MAS-0801-5 Low-Voltage Input A/D Converter

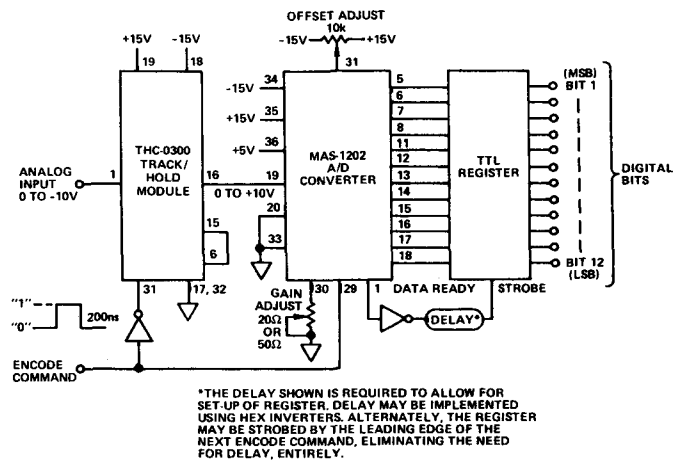


Figure 6. Depicts the MAS-1202 A/D Converter used with the THC-0300 Track-and-Hold

# TIMING DIAGRAMS

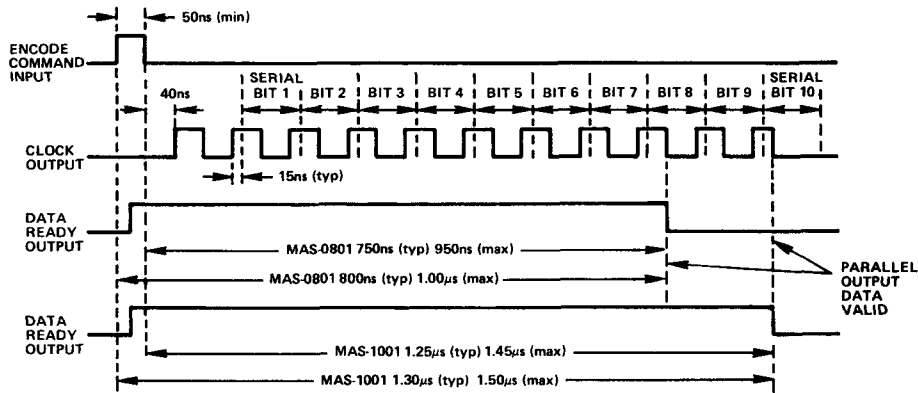


Figure 7. MAS-0801 and MAS-1001 Timing Diagram

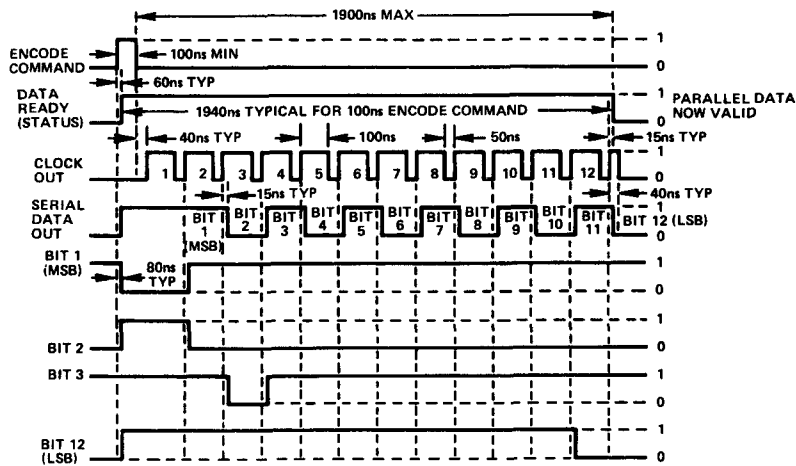


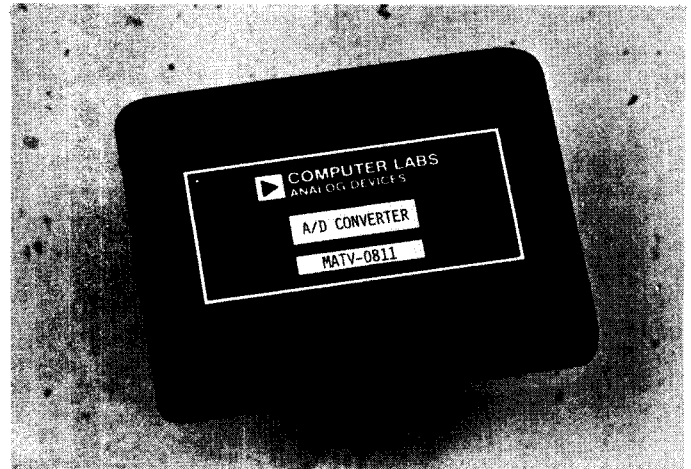
Figure 8. MAS-1202 Timing Diagram

### FEATURES

- 8-Bit Accuracy — Guaranteed Monotonic
- Ultra-High Speed — dc to 20MHz Word Rates
- Most Economical Video A/D
- Smallest Available Complete A/D — 5.5" X 4.38" X 0.85"
- Self Contained — Includes Input Buffer, Encoder, Reference, Timing, and Buffered Parallel Output

### APPLICATIONS

- Digitize Color Television at Up to Three or Four Times NTSC or PAL Color Subcarrier Frequencies
- Video Time Base Correction and Frame Synchronization
- Radar Signal Processing
- Real Time Transient and Continuous Spectrum Analysis

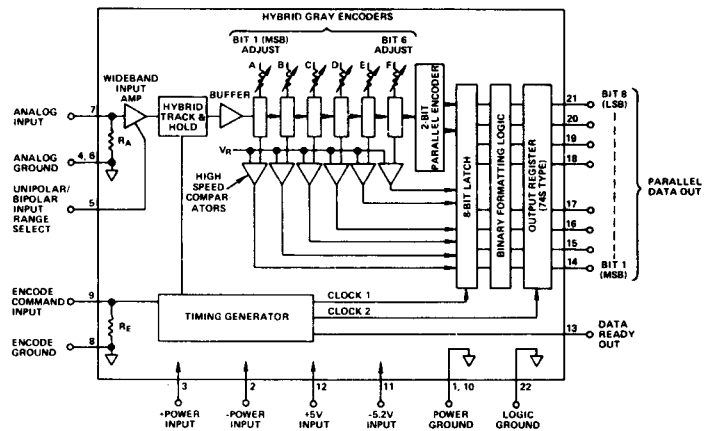


### GENERAL DESCRIPTION

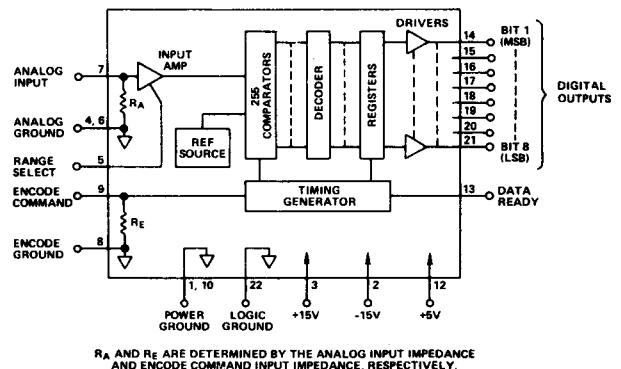
The Analog Devices' MATV series of A/D converters represent a major breakthrough in high-speed A/D technology. Providing conversion word rates from dc to 11MHz, 16MHz and 20MHz the MATV-0811, MATV-0816 and MATV-0820 are the lowest cost A/D converters in their performance class. As complete devices, they require only the addition of external power to accomplish precision video A/D conversion.

The use of internal hybrid microcircuit construction allows these modular A/D's to occupy a volume of only 21 cubic inches—about 1/5 the volume of available comparable devices. They are housed in metal cases which not only shield the circuits from external RF interference, but aid in efficient heat dissipation. A choice of analog input voltages is available, including the industry standard 0 to +1V at 75Ω. The encode command input, data ready output, and the digital bit outputs are all TTL compatible. Designed to operate from either ±12V or ±15V analog and +5V digital supplies (MATV-0811 and MATV-0816 also require -5.2V), the MATV series dissipate less than 8 watts. Their weight is < 10 ounces due to enclosure rather than encapsulation. This technique facilitates rapid, inexpensive factory repair and aids in reliable printed circuit board mounting by the customer without extensive mechanical constraints or system engineering.

Relative dc accuracy is 0.2% of full scale ±1/2LSB when operating over the frequency range of dc to 20MHz. The MATV series is designed to digitize color television signals at rates up to 20MHz and is also ideally suited for other analog to digital conversion requirements, such as radar signal processing, laser pulse analysis, transient analysis, and medical electronics applications where real-time analysis and display of large quantities of information are required.



MATV-0811, MATV-0816 Block Diagram



RA and RE ARE DETERMINED BY THE ANALOG INPUT IMPEDANCE AND ENCODE COMMAND INPUT IMPEDANCE, RESPECTIVELY.

MATV-0820 Block Diagram

# SPECIFICATIONS

(typical @ +25°C and nominal power supply voltages unless otherwise noted)

| MODEL   | UNITS                | MATV-0811          | MATV-0816                | MATV-0820              |
|---|----------------------|--------------------|--------------------------|------------------------|
| <b>RESOLUTION (FS = Full Scale)</b>                   | Bits/% FS            | 8/0.4              | *                        | *                      |
| <b>LSB Weight</b>                                     | % FS                 | 0.4                | *                        | *                      |
| <b>ACCURACY (relative) at dc</b>                      | typ                  | ±0.15% ±1/2LSB     | * <sup>1</sup>           | *                      |
|   | max                  | ±0.2% ±1/2LSB      | * <sup>1</sup>           | *                      |
|   |                      | GUARANTEED         | *                        | *                      |
| <b>Monotonicity</b>                                   |                      |                    | *                        | *                      |
| <b>Differential Nonlinearity vs Temperature</b>       | % FS/°C              | 0.01               | *                        | 0.005                  |
| <b>Linearity and Gain vs Temperature</b>              | % FS/°C              | 0.02               | *                        | 0.01                   |
| <b>DYNAMIC CHARACTERISTICS</b>                        |                      |                    |                          |                        |
| <b>AC Linearity @ Encode Rate<sup>2</sup></b>         | MHz                  | 11                 | 15                       | 20                     |
| <b>Analog Input Frequency</b>                         |                      |                    |                          |                        |
| DC to 3.6MHz  | Spurious Signals are |                    |                          |                        |
|   | > dB below FS        | 50                 | *                        | *                      |
|   |                      | 45                 | *                        | *                      |
| 3.6MHz to 5.5MHz                                      |                      |                    |                          |                        |
| <b>Conversion Rate (Encode Word Rate)</b>             | MHz max              | 11                 | 16 <sup>1</sup>          | 20                     |
| <b>Conversion Time<sup>3</sup></b>                    | ns                   | 150±20             | 120±20                   | 35 ±10 + 1/Encode Rate |
| <b>Aperture Uncertainty (Jitter)</b>                  | ps max               | ±30                | *                        | *                      |
| <b>Aperture Time</b>                                  | ns                   | 3                  | *                        | 12                     |
| <b>Signal to Noise Ratio</b>                          |                      |                    |                          |                        |
| (rms signal to rms noise)                             | dB min               | 48                 | *                        | *                      |
| (peak signal to rms noise)                            | dB min               | 58                 | *                        | *                      |
| <b>Noise Power Ratio<sup>4</sup></b>                  | dB min               | 37                 | *                        | *                      |
| <b>Transient Response<sup>5</sup></b>                 | ns                   | 50                 | *                        | *                      |
| <b>Overvoltage Recovery Time<sup>6</sup></b>          | ns                   | 60                 | *                        | *                      |
| <b>Differential Gain<sup>7</sup></b>                  | %                    | 3                  | *                        | *                      |
| <b>Differential Phase</b>                             | Degrees              | 1                  | *                        | *                      |
| <b>Bandwidth</b>                                      |                      |                    |                          |                        |
| Small Signal 3dB                                      | MHz                  | 20                 | *                        | *                      |
| Large Signal 3dB                                      | MHz                  | 15                 | *                        | *                      |
| Flat ±0.1dB, dc through                               | MHz                  | 5.5                | *                        | *                      |
| <b>INPUT<sup>8</sup></b>                              |                      |                    |                          |                        |
| <b>Voltage Range</b>                                  |                      |                    |                          |                        |
| Unipolar (Pin 5 Grounded)                             | V                    | 0 to 1             | *                        | *                      |
| Bipolar (Pin 5 open)                                  | V                    | ±0.5               | *                        | *                      |
| <b>Impedance (Terminated to Ground)</b>               | Ω                    | 75                 | *                        | *                      |
| <b>ENCODE COMMAND INPUT<sup>8</sup></b>               |                      |                    |                          |                        |
| <b>Logic Levels, TTL Compatible</b>                   |                      | "0" = 0 to +0.4V   | *                        | *                      |
|   |                      | "1" = +2.4V to +5V | *                        | *                      |
| <b>Impedance (terminated to ground)</b>               | Ω                    | 75 ±5%             | *                        | *                      |
| <b>Rise and Fall Times (10% to 90%) max</b>           | ns                   | 10                 | *                        | *                      |
| <b>Duration/Width 50% points (see timing diagram)</b> | ns min               | 10                 | *                        | 20                     |
|   | ns max               | 50% duty cycle     | 40                       | *                      |
| <b>Frequency (random or periodic)</b>                 | dc to MHz            | 11                 | 16                       | 20                     |
| <b>DIGITAL DATA OUTPUT<sup>8</sup></b>                |                      |                    |                          |                        |
| <b>Format</b>   |                      |                    | Eight Parallel Bits NRZ  |                        |
| <b>Logic Levels, TTL</b>                              |                      |                    | (Same as Encode Command) |                        |
| <b>Drive Capability (not short circuit protected)</b> | TTL Loads            | 10 Std             | 10 Schottky              |                        |
| <b>Time Skew</b>                                      | ns max               | 15                 | 10                       | 10                     |
| <b>Coding</b>   |                      |                    | Straight Binary (BIN)    |                        |
| <b>DATA READY OUTPUT</b>                              |                      |                    |                          |                        |
| <b>Format<sup>9</sup></b>                             |                      | RZ                 | *                        | *                      |
| <b>Logic Levels, TTL</b>                              |                      |                    | (Same as Encode Command) |                        |
| <b>Drive Capability</b>                               |                      | 10 Std             | 10 Schottky              |                        |
| <b>Width</b>  | ns                   | 40±10              | 35±5                     | 25±5                   |
| <b>POWER REQUIREMENTS<sup>10</sup></b>                |                      |                    |                          |                        |
| MATV-0811, MATV-0816/MATV-0820                        |                      |                    |                          |                        |
| +15V ±2%/+11.8V to +15.5V                             | mA max               | 210                | *                        | 70                     |
| -15V ±2%/-11.8V to -15.5V                             | mA max               | 180                | *                        | 400                    |
| +5V ±5%/+5V ±5%                                       | mA max               | 450                | 540                      | 200                    |
| -5.2V ±5%   | mA max               | 280                | *                        | N/A                    |
| <b>TEMPERATURE RANGE<sup>11</sup></b>                 |                      |                    |                          |                        |
| <b>Operating (case)</b>                               | °C                   | 0 to +70           | *                        | *                      |
| <b>Storage</b>  | °C                   | -55 to +85         | *                        | *                      |

\*Same as MATV-0811.

## NOTES:

<sup>1</sup> Applies to a customer specified operating frequency, ±10%. Outside this range, accuracy may degrade to ±0.3% ±1/2LSB.

<sup>2</sup> AC linearity expressed in terms of spurious in-band signals generated at specified encode rates.

<sup>3</sup> Pipeline delay not related to encode rate.

<sup>4</sup> DC to 5MHz while noise BW with slot frequency at 500kHz.

<sup>5</sup> Time to achieve 8-bit (0.2%) accuracy after F.S. step input.

<sup>6</sup> For signals not exceeding 10% overvoltage, the A/D will recover to 8-bit accuracy within 60ns after the signal returns to the specified range. Overvoltage inputs greater than 150% of F.S. may damage input circuits and should be avoided.

<sup>7</sup> At maximum encode rate, 20 IRF unit subcarrier, not including quantization effects.

<sup>8</sup> Consult factory for other voltage, impedance and logic level options.

<sup>9</sup> For MATV-0811, the leading edge of the Data Ready pulse occurs approximately 15ns before output data changes. The trailing edge is recommended for strobing data into external circuits.

For MATV-0816, the leading edge of the Data Ready pulse occurs approximately 10ns before output data changes. The trailing edge is recommended for strobing data into external circuits.

For MATV-0820, the leading edge of the Data Ready pulse occurs approximately simultaneously with output data changes. The trailing edge is recommended for strobing data into external circuits. This provides a minimum of 20ns set-up time for external registers.

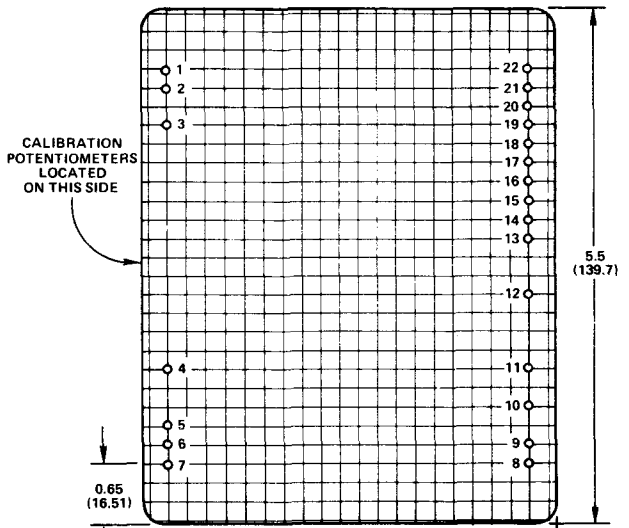
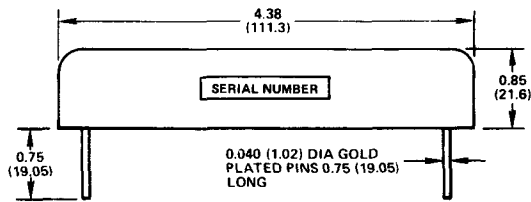
<sup>10</sup> The A/D's are calibrated at the factory at either ±12V or ±15V as a no-cost option. Other operating voltages within this range may be specified by the user at slight additional cost. See application section for more information.

<sup>11</sup> See Thermal Considerations page 244S for operating temperature considerations.

Specifications subject to change without notice.

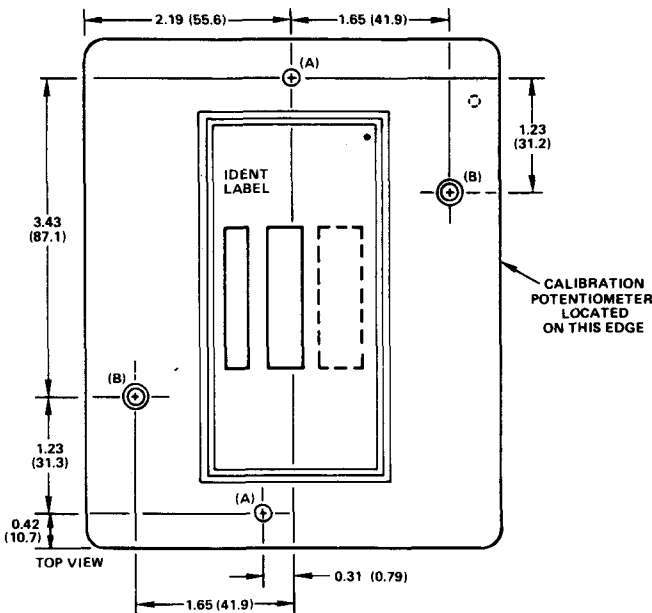
# MECHANICAL OUTLINE AND DIMENSIONS

Dimensions shown in inches and (mm)



PINS ARE GOLD PLATED PER MIL-G-5204, TYPE II

NOTES:  
DIMENSIONS AND LOCATION OF HOLD DOWN HOLES FOR MATV-0820 ARE SHOWN ON THE MECHANICAL OUTLINE FIGURE BELOW. NOT AVAILABLE ON MATV-0811 AND -0816.  
DOT ON TOP INDICATES POSITION OF PIN 1.



(A) LOCATIONS ARE HOLES (0.16" TO 0.18" DIA.) THRU THE A/D SUITABLE FOR SECURING THE UNIT TO A MOTHER BOARD, ETC.  
(B) LOCATIONS ARE EQUIPPED WITH #6X32 CLINCH NUTS (0.3" DEEP) SUITABLE FOR ATTACHING HEAT SINK, ETC.

DOT ON TOP INDICATES POSITION OF PIN 1.

# MATV SERIES PIN DESIGNATIONS

| PIN | FUNCTION  | COMMENTS                            |
|-----|---|-------------------------------------|
| 1   | POWER GROUND  | *                                   |
| 2   | - POWER INPUT   | -11.5V (MIN); -16.5V (MAX)          |
| 3   | + POWER INPUT   | +11.5V (MIN); +16.5V (MAX)          |
| 4   | ANALOG GROUND   | *                                   |
| 5   | RANGE SELECT  | UNIPOLAR = GROUND<br>BIPOLAR = OPEN |
| 6   | ANALOG GROUND   | *                                   |
| 7   | ANALOG INPUT  | OPTIONAL                            |
| 8   | ENCODE GROUND   | *                                   |
| 9   | ENCODE COMMAND  | TTL, +5V (MAX)                      |
| 10  | POWER GROUND  | *                                   |
| 11  | NO CONNECTION 0820<br>-5.2V POWER INPUT<br>0811, 0816 | -5V (MIN), -5.5V (MAX)              |
| 12  | +5V POWER INPUT                                       | +4.75V (MIN); +5.25V (MAX)          |
| 13  | DATA READY OUTPUT                                     | TTL LEVELS                          |
| 14  | BIT 1 OUTPUT (MSB)                                    | TTL LEVELS                          |
| 15  | BIT 2 OUTPUT  | TTL LEVELS                          |
| 16  | BIT 3 OUTPUT  | TTL LEVELS                          |
| 17  | BIT 4 OUTPUT  | TTL LEVELS                          |
| 18  | BIT 5 OUTPUT  | TTL LEVELS                          |
| 19  | BIT 6 OUTPUT  | TTL LEVELS                          |
| 20  | BIT 7 OUTPUT  | TTL LEVELS                          |
| 21  | BIT 8 OUTPUT (LSB)                                    | TTL LEVELS                          |
| 22  | DIGITAL LOGIC GND.                                    | *                                   |

\*ALL GROUNDS ARE INTERNALLY CONNECTED

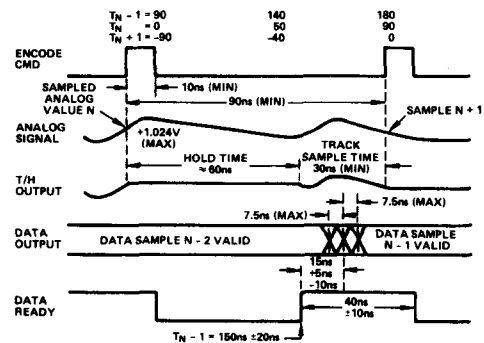


Figure 1. MATV-0811 Timing Diagram at Maximum Sample Rate of 11MHz

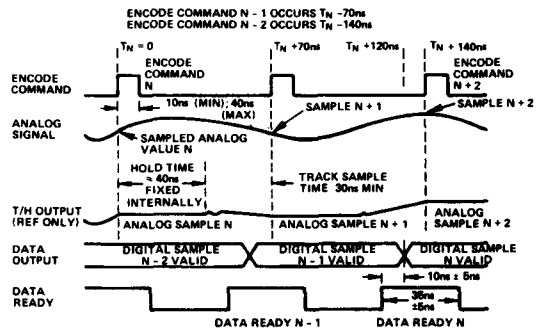
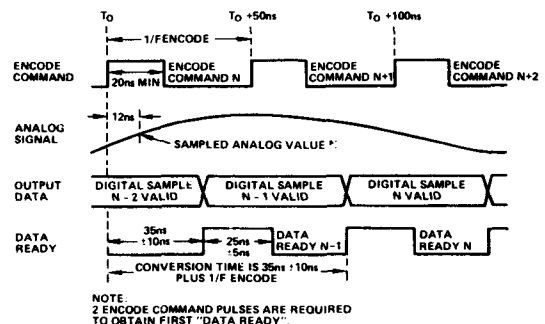


Figure 2. MATV-0816 Timing Diagram at Sample Rate of 14.3MHz



NOTE:  
2 ENCODE COMMAND PULSES ARE REQUIRED TO OBTAIN FIRST "DATA READY".

Figure 3. MATV-0820 Timing Diagram Shown at an Encode Frequency of 20MHz



# Applying the MATV-0811, -0816, -0820

## REMOTE INTERFACE CONSIDERATIONS

In many applications, the user may wish to build up an A/D converter assembly using the MATV modular converter as a building block. The assembly would typically consist of a printed circuit card in a card nest, housed within an equipment enclosure. It could also be a chassis with coaxial inputs and outputs, and power supplies incorporated into the chassis to permit operation from ac line voltages.

This type of assembly generally includes provisions for converting remotely generated signals and driving transmission lines to the remote digital loads. The design of such an assembly must take into account the wideband, low level sensitivity of the A/D converter input, and the use of terminated coaxial input lines is recommended for analog and encode command inputs. The use of 75Ω coaxial transmission line is recommended. It is particularly important to isolate the A/D's digital outputs from the signal input, since digital feedback can seriously affect the conversion accuracy.

In order to maintain specified A/D conversion parameters, the power supplies must be fully decoupled from sources of noise and other signals. Total line and load regulation should be better than 15mV at the MATV power supply terminals.

The output circuit of the MATV is a "74" register and is capable of driving up to 10 local TTL loads. When driving distant loads and terminations are required, line drivers should be used. For twisted pair lines, the 9614 driver is recommended. For coaxial lines, the 2614 is recommended.

Figure 4 shows the recommended circuit for the A/D assembly used in applications where the signal source and digital load are remote from the A/D converter.

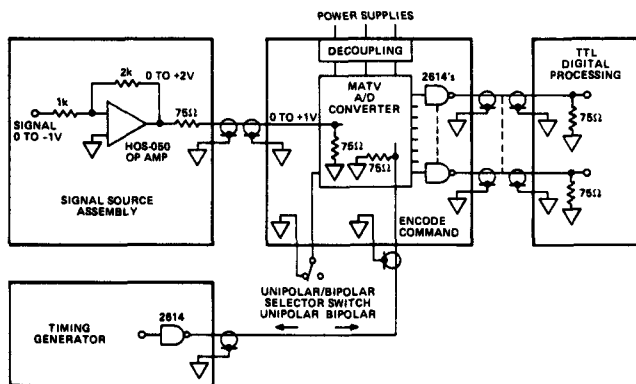


Figure 4. Typical System Application

## THERMAL CONSIDERATIONS

The MATV series A/D converters are specified to operate over a temperature range of 0 to +70°C. The temperature referred to is the module case temperature, and operation outside of this range can seriously damage the converter. The temperature limitations that Analog Devices has placed on this converter are necessitated by the published temperature limits of the commercially available components used within the device. Nowhere in the device are unreliable semiconductor junction temperature limits approached.

Generally, the A/D module must have forced air cooling when in operation. The only exceptions are when the unit is operated in free air ambients of <+40°C (as during bench test, for example), or if the case is in contact with a heat sink or cold plate which will maintain the temperature of the case at +70°C or less.

Whenever the A/D module is confined in a closed space or operated at ambient temperatures above +40°C, Analog Devices recommends an air flow of 500 linear feet per minute across the top of the case. Since the A/D is a metal encased device, this amount of air flow will keep the case temperature within 10°C of the air temperature, and thus permit operation at ambient temperatures of up to +60°C. This amount of air flow can be easily supplied by a 20 or 30 CFM fan if the air flow is directed across the top surface of the module.

## POWER SUPPLY CONSIDERATIONS

The MATV-0820 A/D is designed to operate from standard analog and digital power supplies. The digital supply is +5V ±5% the industry standard. The analog supplies may be any symmetrical voltages between ±11.8 and ±15.5 volts. Thus the modules may be operated on either of the two industry standard analog-supply voltages (±12V or ±15V).

The MATV-0811 and MATV-0816 also require -5.2V ±5%, and their calibration is affected somewhat by power supply changes. So the A/D must be readjusted whenever the analog supply voltages are changed by more than 300mV. The MATV-0811 and MATV-0816 units supplied by Analog Devices are normally calibrated and tested at ±15V ±0.1% power supply voltages. The customer may at time of purchase specify other power supply voltages between ±12V and ±15V, and the A/D's will be calibrated and tested at the specified power supply voltages.

## CALIBRATION INFORMATION — MATV-0811, MATV-0816

The MATV series A/D converters are calibrated at the factory at either ±12V or ±15V and do not normally require recalibration more often than every year (depending on severity of service). The following calibration procedures are provided to aid the user in long term maintenance. Recalibration should not be started unless it has been determined that the A/D is definitely out of calibration.

## DC CALIBRATION

Using appropriate power supply voltages and encode rates, adjust potentiometers A through F shown in Figure 5 as indicated below. Use a test set-up similar to that shown in Figure 6.

| Unipolar DC Input Voltage | Adjustment Point | Adjust for Flutter Zone of Bit Given | Correct Output "X" Denotes Flutter or Uncertainty |
|---------------------------|------------------|--------------------------------------|---|
| +1/2 FS                   | A                | 1                                    | XXXXXXXXX   |
| +1/4 FS                   | B                | 2                                    | 0XXXXXXXX   |
| +3/8 FS                   | C                | 3                                    | 01XXXXXXXX  |
| +7/16 FS                  | D                | 4                                    | 011XXXXXX   |
| +15/32 FS                 | E                | 5                                    | 0111XXXXX   |
| +31/64 FS                 | F                | 6                                    | 01111XXXX   |

Table 1.

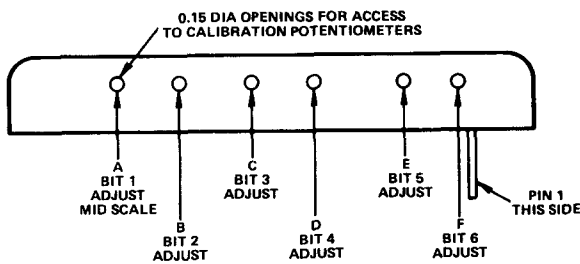
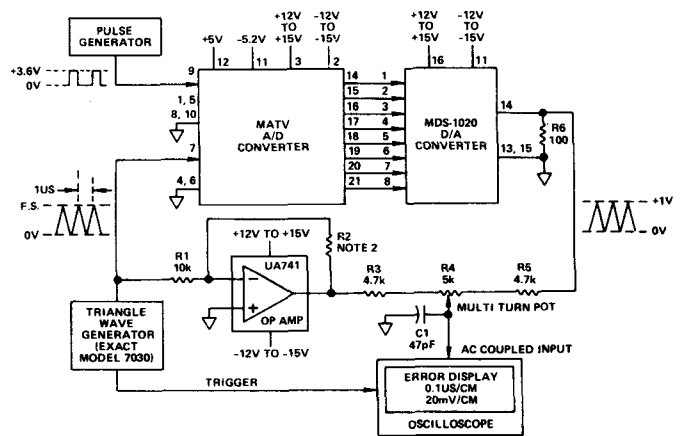


Figure 5. Location of Calibration Potentiometers



- NOTES:
1. ENCODE COMMAND FREQUENCY IS SET TO CUSTOMER-SPECIFIED RATE, DC THRU 10MHz.
  2. R2 VALUES ARE AS FOLLOWS: FOR 1V INPUT VERSIONS, R2 EQUALS 10k. FOR 2V INPUT VERSIONS, R2 EQUALS 4.7k. FOR 5V INPUT VERSIONS, R2 EQUALS 2k. FOR 10V INPUT VERSIONS, R2 EQUALS 1k.
  3. R4 IS ADJUSTED FOR MINIMUM SLOPE ON ERROR PATTERN.

Figure 7. Dynamic Linearity Adjustment Set-Up

### CALIBRATION INFORMATION – MATV-0820

Two internal calibration potentiometers are provided for the adjustment of offset and gain of the MATV-0820. These potentiometers are accessible from the exterior of the MATV-0820, and Figure 8 shows the location of these potentiometers.

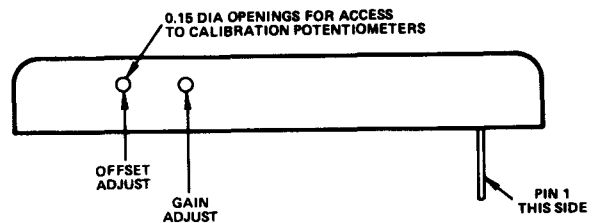


Figure 8. Location of Calibration Potentiometers

### DYNAMIC LINEARITY ADJUSTMENT

If the need arises for recalibration of an MATV series A/D, the simple dc procedure just described may be used, or the following dynamic adjustment may be performed. In general, the dc procedure gives satisfactory results for most applications, but by its nature, is an approximation. When the best possible linearity is required, the following dynamic linearity adjustment may be used. In this procedure, the output of the A/D is converted back into an analog signal by a D/A converter and then subtracted from the input. The result is an error display, and the A/D calibration potentiometers are used to reduce the error pattern to the minimum possible error.

The equipment is set-up and adjusted as shown in Figure 7. The A/D adjustments F through B (see Figure 5) are adjusted in that order to obtain minimum error, which is indicated by the least vertical deflection on the oscilloscope error display.

Adjustment B controls the linearity at mid-scale of the A/D. Mid-scale (1/2 scale) is approximately in the horizontal center of the display. Adjustment C controls the linearity at 1/4 scale, 1/2 scale and 3/4 scale. Adjustment D controls the linearity at 1/8 scale, 1/4 scale, 3/8 scale . . . 7/8 scale. Adjustment E controls linearity in 1/16 scale segments across the range, and adjustment F controls linearity in 1/32 scale segments across the range.

Note that adjustment F interacts with B, C, D and E. Adjustment E interacts with adjustments B, C and D, etc. Therefore the highest letter adjustment pot requiring adjustment must be varied first. For example, if nonlinearities are observed at 1/4, 1/2 and 3/4 scale, adjustment C is first varied to correct the errors at 1/4 and 3/4 scale. Then adjustment B is used to correct the error at mid-scale.

After adjustment, the error display should be less than 4mV p-p.

### OFFSET ADJUSTMENT

The OFFSET ADJUST control shifts the range of the A/D without affecting gain or linearity. It is normally adjusted for an output of 0000000X (X signifies an uncertainty or flutter zone for the indicated bit) with an input analog dc voltage of +1/2LSB for the unipolar input option, and -FS +1/2LSB for the bipolar input option. The user, however, may set this potentiometer to any point in its range to obtain a different offset. The range of the offset potentiometer is approximately  $\pm 10\%$  of FS.

### GAIN ADJUSTMENT

The GAIN ADJUST control affects the full scale range of the A/D by varying the gain of the A/D front end. It is normally adjusted to give an output of 1111111X for an input dc analog voltage of +FS -1/2LSB. The user may adjust this potentiometer anywhere in its range to provide for different input full scale requirements. The range of this potentiometer is approximately  $\pm 5\%$  of the nominal input FS range.

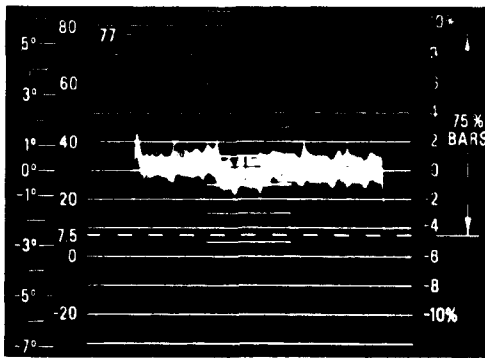


Figure 9. Typical Differential Gain of MATV-0816 Operating at 15MHz Word Rates

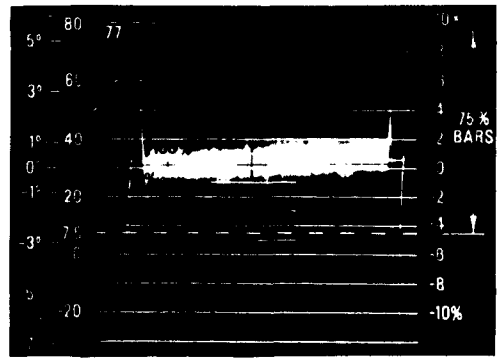


Figure 10. Typical Differential Phase of MATV-0816 Operating at 15MHz Word Rates

#### ORDERING INFORMATION

Each MATV series A/D converter will be calibrated at  $\pm 15V$  as a standard. Order by model number either MATV-0811, MATV-0816 or MATV-0820.

#### Optional Versions

The MATV series A/D's are available with a variety of options, including analog input range and impedance, encode command input impedance, encode word rate, power supply voltage calibration, etc. Any option other than what is shown on the data sheet will have higher price and longer delivery, since each non-standard device is built on a per order basis.

A complete listing of optional designators is available from either the factory or your local Analog Devices' sales office.

#### Device Marking

The MATV series A/D that you order will be marked with a series of alphanumeric characters which specifically designate the options built into the device. These will be as follows:

MATV-0811 will be marked MATV-0811-1-BIN

MATV-0816 will be marked MATV-0816-0175BIN75143150

MATV-0820 will be marked MATV-0820-0175BIN75

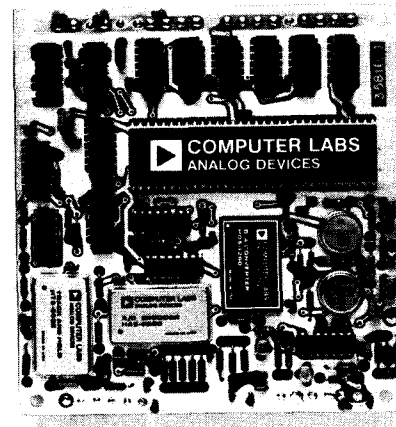
This information is provided so that there will be no confusion as to why information other than the basic model number appears on the device identification label, which might cause problems at a customer's incoming inspection.

### FEATURES

- 10 Bits @ 5MHz Word Rate
- One-27 Sq. In. PC Board
- Built-In Track-and-Hold — 25ps Aperture Uncertainty
- 20MHz Analog Input Bandwidth
- TTL Compatible
- Low (10-Watt) Power Dissipation
- Signal-To-Noise Ratio Greater Than 58dB
- Noise Power Ratio Greater Than 49dB
- Completely Repairable

### APPLICATIONS

- Radar Digitizing
- Digital Communications
- Real Time Spectrum Analysis
- High Resolution TV



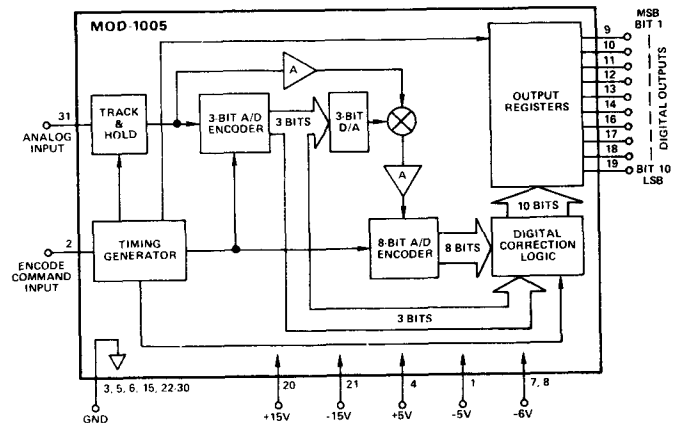
### GENERAL DESCRIPTION

Analog Devices' model MOD-1005 is a very high-speed A/D converter capable of digitizing video input signals to 10-bit accuracy at random or periodic word rates of dc through 5MHz. The MOD-1005 is truly a breakthrough in high-speed A/D technology. It is the most cost effective A/D in this speed category, combining small size and low power dissipation with low cost.

The MOD-1005 is constructed on a single printed circuit card which is intended for mounting on a system mother-board, and occupies only 27 square inches. Within this A/D is the required sample/track and hold amplifier, encoder, timing circuits and output latches for a true simultaneous, all-parallel digital output.

The encode command input and digital outputs are TTL compatible. The A/D requires only an external encode command pulse and external power supplies for operation. **NO** external parts are required. Gain and offset potentiometers are provided on the card. The A/D is fully repairable either at the factory or in the field.

The MOD-1005 is ideally suited for systems requiring the ultimate in conversion speed and accuracy. Such applications include radar digitizing, digital communications, spectrum analysis, and many others. Each MOD-1005 is backed by Analog Devices' limited one year warranty.



*Block Diagram*

# SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

|   |  |
|---|--|
| <b>MODEL</b>                                    | <b>MOD-1005</b>                                  |
| <b>RESOLUTION (FS = FULL SCALE)</b>             | 10 Bits (0.1% FS)                                |
| <b>LSB WEIGHT</b>                               | 4mV  |
| <b>ACCURACY (INCLUDING LINEARITY) @ DC</b>      | ±0.05% Full Scale ±1/2LSB                        |
| Monotonicity                                    | Guaranteed                                       |
| Differential Nonlinearity vs. Temperature       | 0.0005% of FS/°C                                 |
| Gain vs. Temperature                            | 0.01% of FS/°C                                   |
| <b>DYNAMIC CHARACTERISTICS</b>                  |  |
| AC Linearity <sup>1</sup>                       | Spurious Signals >59dB below FS                  |
| Conversion Time                                 | See Text   |
| Conversion Rate (Word Rate)                     | dc to 5MHz                                       |
| Aperture Uncertainty (Jitter)                   | ±25ps max  |
| Aperture Time                                   | 45ns (±10ns from unit to unit)                   |
| Signal to Noise Ratio (rms signal to rms noise) | 58dB min at 500kHz analog input                  |
| Noise Power Ratio <sup>2</sup>                  | 49dB min   |
| Transient Response (Full Scale Step Input)      | 10-Bit (0.05%) Accuracy within 50ns              |
| Overvoltage Recovery Time                       |  |
| Recovers to 10-bit accuracy after               |  |
| 2 X FS input overvoltage in                     | 200ns  |
| Input Bandwidth (small signal, 3dB)             | 20MHz min  |
| Input Bandwidth (large signal, 3dB)             | 15MHz min flat within ±0.1dB,<br>dc through 5MHz |
| <b>INPUT</b>                                    |  |
| Voltage Range                                   | ±2.048V FS<br>±4V Absolute max                   |
| Impedance                                       | 50Ω  |
| Offset Voltage                                  | Adjust to 0 with On Board Potentiometer          |
| Offset vs. Temperature                          | 0.01% Full Scale/°C                              |
| Bias Current                                    | 1nA max  |
| <b>ENCODE COMMAND INPUT</b>                     |  |
| Logic Levels, TTL Compatible                    | "0" = 0 to +0.4V<br>"1" = +2.4V to +5V           |
| Logic Loading                                   | 2 Standard TTL Gates                             |
| Rise and Fall Times                             | 10ns max   |
| Duration Min/Max                                | 20ns/60% of Duty Cycle                           |
| Frequency (Random or Periodic)                  | dc to 5MHz                                       |
| Sample Delay                                    | 45ns (unit to unit tolerance is ±10ns)           |
| <b>DIGITAL DATA OUTPUT</b>                      |  |
| Format  | 10 Parallel Bits, NRZ                            |
| Logic Levels, TTL Compatible                    | "0" = 0 to +0.4V<br>"1" = +2.4V to +5V           |
| Drive (Not Short Circuit Protected)             | Up to 1 Schottky TTL or<br>2 Standard TTL Loads  |
| Time Skew                                       | 10ns max   |
| Coding  | 2's Complement (2SC)                             |
| Conversion Time                                 | See Text (page 249S)                             |
| <b>POWER REQUIREMENTS</b>                       | typ/max  |
| +15V ±5%  | 150/170mA  |
| -15V ±5%  | 150/170mA  |
| -6V ±4%   | 300/350mA  |
| +5V ±5%   | 350/400mA  |
| -5V ±5%   | 500/550mA  |
| Power Consumption                               | 10 Watts   |
| <b>TEMPERATURE RANGE</b>                        |  |
| Operating                                       | 0 to +70°C                                       |
| Storage   | -55°C to +85°C                                   |
| Cooling Requirements                            | 100 Linear Feet Per Min (LFPM)                   |
| <b>PHYSICAL CHARACTERISTICS</b>                 |  |
| Construction                                    | Single Printed Circuit Card                      |

## NOTES:

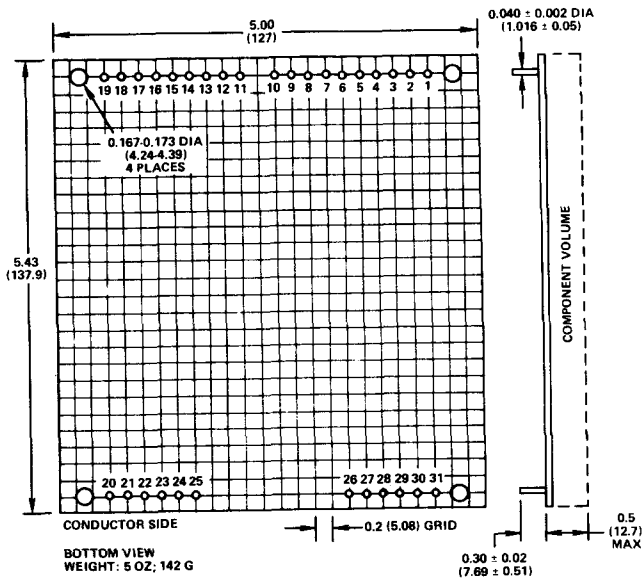
<sup>1</sup> AC linearity expressed in terms of spurious in-band signals generated as specified encode rates, with dc to 2.5MHz analog input.

<sup>2</sup> DC to 2.4MHz white noise BW with Slot frequency of 512kHz.

Specifications subject to change without notice.

## OUTLINE DIMENSIONS

Dimensions shown in inches (mm).



## PIN DESIGNATIONS

| PIN | FUNCTION       | PIN | FUNCTION     |
|-----|----------------|-----|--------------|
| 1   | -5V            | 16  | BIT 7        |
| 2   | ENCODE COMMAND | 17  | BIT 8        |
| 3   | GND*           | 18  | BIT 9        |
| 4   | +5V            | 19  | BIT 10 LSB   |
| 5   | GND*           | 20  | +15V         |
| 6   | GND*           | 21  | -15V         |
| 7   | -6V            | 22  | GND*         |
| 8   | -6V            | 23  | GND*         |
| 9   | BIT 1 MSB      | 24  | GND*         |
| 10  | BIT 2          | 25  | GND*         |
| 11  | BIT 3          | 26  | GND*         |
| 12  | BIT 4          | 27  | GND*         |
| 13  | BIT 5          | 28  | GND*         |
| 14  | BIT 6          | 29  | GND*         |
| 15  | GND*           | 30  | GND*         |
|     |                | 31  | ANALOG INPUT |

\*ALL GROUND PINS ARE CONNECTED TOGETHER WITHIN THE MOD-1005

## ORDERING INFORMATION

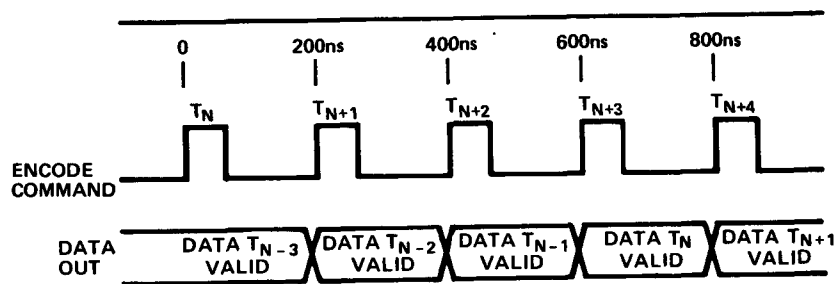
Order model number MOD-1005 A/D converter. Mating pin sockets for the MOD-1005 are model number MSB-2 (31 required per A/D).

## CONVERSION TIME

Output data is valid two encode command clock periods plus 200ns after application of an initial encode command pulse. Due to the pipeline delay effect of the A/D, a total of three encode command pulses are required to shift the data to the output of the A/D. For example, with a 5MHz encode rate, data is valid 600ns after the application of the first encode

command pulse – assuming that two pulses occur after the first.

Use of the trailing edge of the encode command is recommended for strobing output data into external register (see Figure 1).



DATA  $T_N$  (THE RESULT OF ENCODE COMAND  $T_N$ ) OCCURS TWO CONVERSION PERIODS PLUS 200ns AFTER ENCODE COMMAND  $T_N$ . FOR A 5MHz WORD RATE AS SHOWN, DATA IS VALID 200ns AFTER THE THIRD ENCODE COMMAND PULSE OR  $T_N + 600$ ns. IN ALL CASES, THREE ENCODE COMMAND PULSES ARE REQUIRED FOR TRANSFER OF DATA TO THE OUTPUT, DUE TO THE PIPELINE DELAY EFFECT THROUGH THE A/D. NO DATA READY PULSE IS SUPPLIED.

Figure 1. MOD-1005 Timing Diagram

## GROUND CONNECTIONS

It should be noted that the MOD-1005 PC board has 13 ground pins. These are all connected to the ground plane on the board. For best results it is recommended that ALL of these pins be connected to a massive system or "mother board" ground plane.

## CALIBRATION PROCEDURE (MOD-1005)

The MOD-1005 A/D is precisely calibrated at the factory before shipment, and should need no further calibration. However, if slight readjustments of the A/D are required in the system, the following procedure should be followed. It should be remembered that the output coding of this A/D is 2SC.

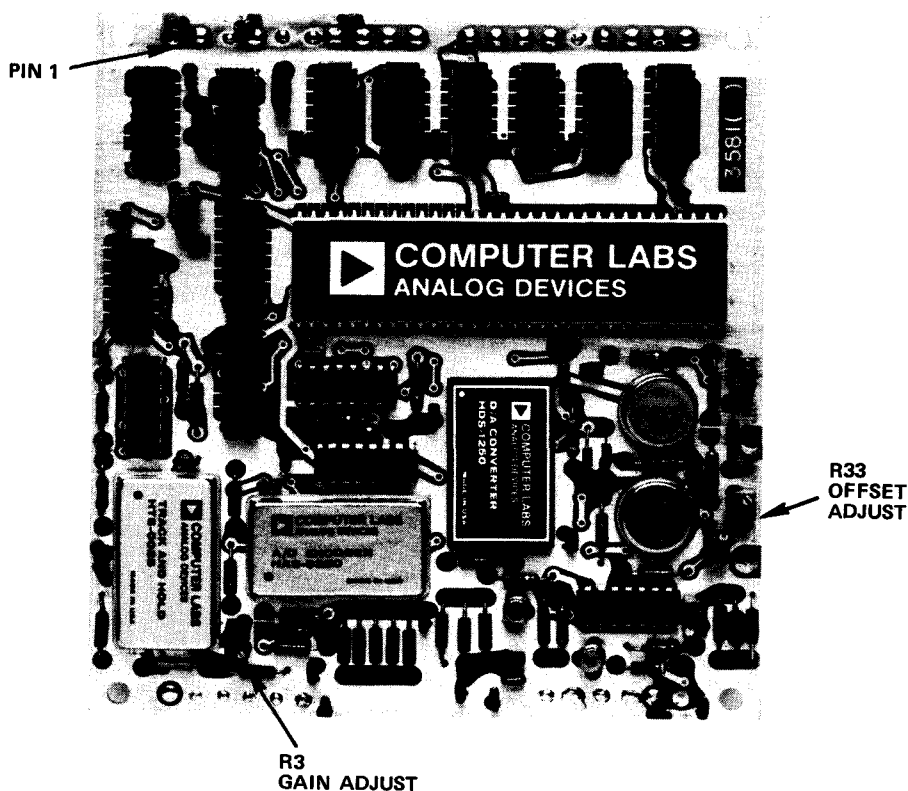
### Offset Adjustment

The offset is adjusted by varying potentiometer R33 with 0 volts applied to the analog input. To obtain the proper output

code, observe that the digital output is changing between 11111111 and 00000000 at this adjustment level. When properly adjusted a digital code of 00000000 will represent analog input 1LSB above zero volts, and a digital code of 11111111 will represent an analog input of 1LSB below zero volts.

### Gain Adjustment

The gain is adjusted by varying potentiometer R3. This adjustment is made by applying +2.042V (FS -1 1/2LSB) to the analog input and while monitoring the digital output, adjust R3 for the output code varying between 01111110 and 01111111 (FS). If the user needs to offset the entire range of the A/D, this can be accomplished by readjusting R33 as required. However, in this procedure, the offset should always be adjusted first.



*A/D Converter Assembly*

## FEATURES

- Low Cost A-D Conversion
- Versatile Input Amplifier
  - Positive or Negative Voltage Modes
  - Negative Current Mode
  - High Input Impedance, Low Drift
- Single Supply, 5 to 36 Volts
- Linearity:  $\pm 0.05\%$  FS
- Low Power: 1.2mA Quiescent Current
- Full Scale Frequency up to 100kHz
- 1.00 Volt Reference
- Thermometer Output ( $1\text{mV}/^\circ\text{K}$ )
- F-V Applications

## PRODUCT DESCRIPTION

The AD537 is a monolithic V-F converter consisting of an input amplifier, a precision oscillator system, an accurate internal reference generator and a high current output stage. Only a single external RC network is required to set up any full scale (F.S.) frequency up to 100kHz and any F.S. input voltage up to  $\pm 30\text{V}$ . Linearity error is as low as  $\pm 0.05\%$  for 10kHz F.S., and operation is guaranteed over an 80dB dynamic range. The overall temperature coefficient (excluding the effects of external components) is typically  $\pm 30\text{ppm}/^\circ\text{C}$ . The AD537 operates from a single supply of 5 to 36V and consumes only 1.2mA quiescent current.

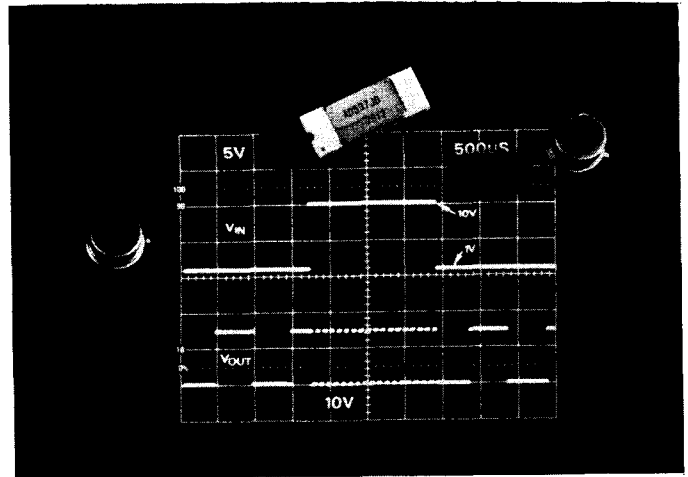
A temperature-proportional output, scaled to  $1.00\text{mV}/^\circ\text{K}$ , enables the circuit to be used as a reliable temperature-to-frequency converter; in combination with the fixed reference output of 1.00V, offset scales such as  $0^\circ\text{C}$  or  $0^\circ\text{F}$  can be generated.

The low drift ( $1\mu\text{V}/^\circ\text{C}$  typ) input amplifier allows operation directly from small signals (e.g., thermocouples or strain gages) while offering a high ( $250\text{M}\Omega$ ) input resistance. Unlike most V-F converters, the AD537 provides a square-wave output, and can drive up to 12 TTL loads, LEDs, very long cables, etc.

The excellent temperature characteristics and long-term stability of the AD537 are guaranteed by the primary band-gap reference generator and the low T.C. silicon chromium thin film resistors used throughout.

The device is available in either a TO-116 ceramic DIP or a TO-100 metal can; both are hermetically sealed packages.

The AD537 is available in three performance/temperature grades; the J and K grades are specified for operation over the 0 to  $70^\circ\text{C}$  range while the AD537S is specified for operation over the full military temperature range,  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ . MIL-STD-883, Level B processing is available.



## PRODUCT HIGHLIGHTS

1. The AD537 is a complete V-F converter requiring only an external RC timing network to set the desired full scale frequency and a selectable pull-up resistor for the open-collector output stage. Any full-scale input voltage range from 100mV to 10 volts (or greater, depending on  $+V_S$ ) can be accommodated by proper selection of timing resistor. The full scale frequency is then set by the timing capacitor from the simple relationship,  $f = V/10RC$ .
2. The power supply requirements are minimal, only 1.2mA quiescent current is drawn from a single positive supply from 4.5 to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to  $(+V_S - 4)$  volts. Negative inputs can easily be connected for below ground operation.
3. F-V converters with excellent characteristics are also easy to build by connecting the AD537 in a phase-locked loop. Application particulars are shown in Figure 10.
4. The versatile open-collector NPN output stage can sink up to 20mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or  $-V_S$ ) and 4 volts below  $+V_S$ . This allows easy direct interface to any logic family with either positive or negative logic levels.
5. Every AD537 is subjected to long term stabilization bakes and temperature cycled 10 times from  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$  prior to final test to insure reliability and long-term stability.



# SPECIFICATIONS (typical @ +25°C with V<sub>S</sub> (total) = 5 to 36V, unless otherwise noted)

| MODEL  | AD537JH  | AD537JD     | AD537KD<br>AD537KH                    | AD537SD<br>AD537SH |
|--|--|-------------|---------------------------------------|--------------------|
| <b>CURRENT-TO-FREQUENCY CONVERTER</b>  |  |             |                                       |                    |
| Frequency Range  | 0 to 150kHz  | *           | *                                     | *                  |
| Nonlinearity <sup>1</sup>  |  |             |                                       |                    |
| f <sub>max</sub> = 10kHz   | 0.15% max (0.1% typ)                                 | *           | 0.07% max                             | **                 |
| f <sub>max</sub> = 100kHz  | 0.25% max (0.15% typ)                                | *           | 0.1% max                              | **                 |
| Full Scale Calibration Error   |  |             |                                       |                    |
| C = 0.01μF, I <sub>IN</sub> = 1.000mA  | ±10% max   | ±7% max     | ±5% max                               | **                 |
| vs. Supply (f <sub>max</sub> < 100kHz)                                       | ±0.1%/V max (0.01% typ)                              | *           | *                                     | *                  |
| vs. Temp. (T <sub>min</sub> to T <sub>max</sub> )                            | ±150ppm/°C max (50ppm typ)                           | *           | 50ppm/°C max (30ppm typ) <sup>2</sup> | 150ppm/°C max      |
| <b>ANALOG INPUT AMPLIFIER</b><br>(Voltage-to-Current Converter)              |  |             |                                       |                    |
| Voltage Input Range  |  |             |                                       |                    |
| Single Supply  | 0 to (+V <sub>S</sub> - 4) Volts (min)               | *           | *                                     | *                  |
| Dual Supply  | -V <sub>S</sub> to (+V <sub>S</sub> - 4) Volts (min) | *           | *                                     | *                  |
| Input Bias Current   |  |             |                                       |                    |
| (Either Input)   | 100nA  | *           | *                                     | *                  |
| Input Resistance (Non-Inverting)   | 250MΩ  | *           | *                                     | *                  |
| Input Offset Voltage   |  |             |                                       |                    |
| (Trimable in "D" Package Only)   | 5mV max  | *           | 2mV max                               | **                 |
| vs. Supply   | 200μV/V max  | 100μV/V max | 100μV/V max                           | **                 |
| vs. Temp. (T <sub>min</sub> to T <sub>max</sub> )                            | 5μV/°C   | *           | 1μV/°C                                | 10μV/°C max        |
| Safe Input Voltage <sup>3</sup>  | ±V <sub>S</sub>                                      | *           | *                                     | *                  |
| <b>REFERENCE OUTPUTS</b>   |  |             |                                       |                    |
| Voltage Reference  |  |             |                                       |                    |
| Absolute Value   | 1.00 Volt ±5% max                                    | *           | *                                     | *                  |
| vs. Temp. (T <sub>min</sub> to T <sub>max</sub> )                            | 50ppm/°C   | *           | 100ppm/°C max <sup>2</sup>            | **                 |
| vs. Supply   | ±0.03%/V max   | *           | *                                     | *                  |
| Output Resistance <sup>4</sup>   | 380Ω   | *           | *                                     | *                  |
| Absolute Temperature Reference <sup>5</sup>                                  |  |             |                                       |                    |
| Nominal Output Level   | 1.00mV/°K  | *           | *                                     | *                  |
| Initial Calibration @ +25°C  | 298mV (±5mV)   | *           | 298mV (±5mV max)                      | **                 |
| Slope Error from 1.00mV/°K   | ±0.02mV/°K   | *           | *                                     | *                  |
| Slope Nonlinearity   | ±0.1°K   | *           | *                                     | *                  |
| Output Resistance <sup>4</sup>   | 900Ω   | *           | *                                     | *                  |
| <b>OUTPUT INTERFACE (Open Collector Output)</b><br>(Symmetrical Square Wave) |  |             |                                       |                    |
| Output Sink Current in Logic "0"   |  |             |                                       |                    |
| V <sub>OUT</sub> = 0.4V max, T <sub>min</sub> to T <sub>max</sub> )          | 10mA min   | 20mA min    | 20mA min                              | 10mA min           |
| Output Leakage Current in Logic "1"  |  |             |                                       |                    |
| (T <sub>min</sub> to T <sub>max</sub> )                                      | 200nA max  | *           | *                                     | 2μA max            |
| Logic Common Level Range   | -V <sub>S</sub> to (+V <sub>S</sub> - 4) Volts       | *           | *                                     | *                  |
| Rise/Fall Times (C <sub>T</sub> = 0.01μF)                                    |  |             |                                       |                    |
| I <sub>IN</sub> = 1mA  | 0.2μs  | *           | *                                     | *                  |
| I <sub>IN</sub> = 1μA  | 1μs  | *           | *                                     | *                  |
| <b>POWER SUPPLY</b>  |  |             |                                       |                    |
| Voltage, Rated Performance   |  |             |                                       |                    |
| Single Supply  | 4.5V to 36V  | *           | *                                     | *                  |
| Dual Supply  | ±5 to ±18V   | *           | *                                     | *                  |
| Quiescent Current  | 1.2mA (2.5mA max)                                    | *           | *                                     | *                  |
| <b>TEMPERATURE RANGE</b>   |  |             |                                       |                    |
| Rated Performance  | 0 to +70°C   | *           | *                                     | -55°C to +125°C    |
| Storage  | -65°C to +150°C                                      | *           | *                                     | *                  |

\*Specifications same as AD537JH.

\*\*Specifications same as AD537K.

†Insert letter grade.

Specifications subject to change without notice.

<sup>1</sup> Nonlinearity is specified for a current input level (I<sub>IN</sub>) to the converter from 0.1 to 1000μA. Converter has 100% overrange capability up to I<sub>IN</sub> = 2000μA with slightly reduced linearity. Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.

<sup>2</sup> Guaranteed not tested.

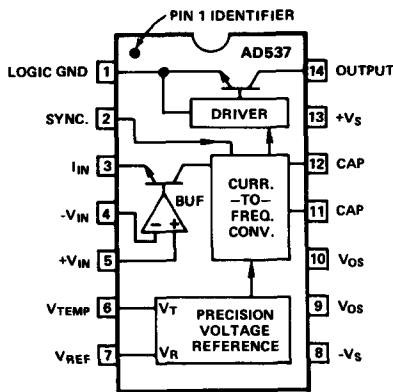
<sup>3</sup> Maximum voltage input level is equal to the supply on either input terminal. However, large negative voltage levels can be applied to the negative terminal if the input is scaled to a nominal 1mA full scale through an appropriate value resistor (see Figure 4).

<sup>4</sup> Loading the 1.0 volt or 1mV/°K outputs can cause a significant change in overall circuit performance, as indicated in the applications section. To maintain normal operation, these outputs should be operated into the internal buffer or an external amplifier.

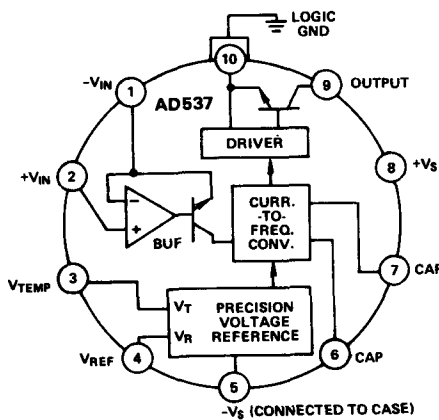
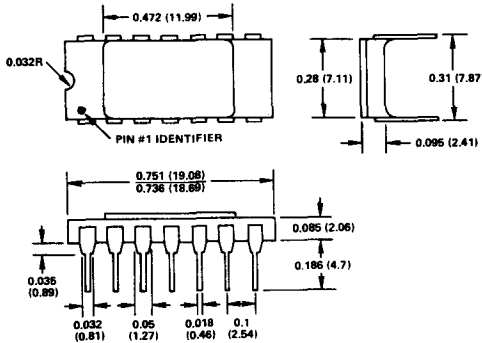
<sup>5</sup> Temperature reference output performance is specified from 0 to +70°C for "J" and "K" devices, -55°C to +125°C for "S" model.

## PIN CONFIGURATION & DIMENSIONS

Dimensions shown in inches and (mm).



### "D" PACKAGE - TO-116



### "H" PACKAGE - TO-100

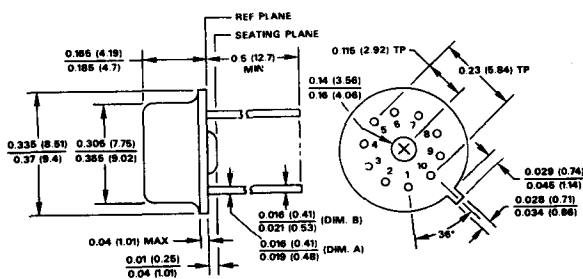


Figure 1. Block Diagram and Pin Connections

## AD537 CHIPS

The AD537 is also available in passivated chip form guaranteed to "J" specifications. Consult factory for pricing and application particulars. Figure 2 shows the chip metallization layout and bonding pads.

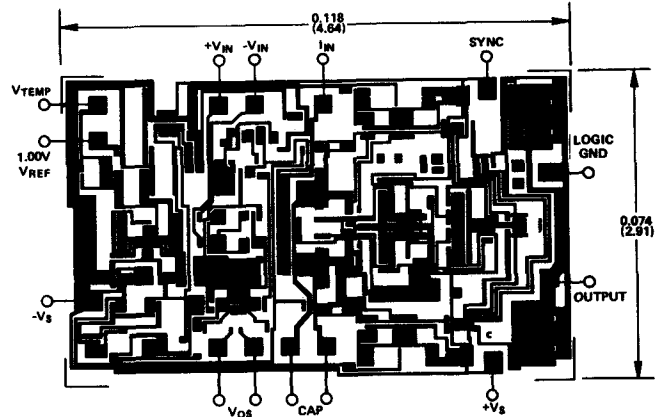


Figure 2. Chip Bonding Diagram

## CIRCUIT OPERATION

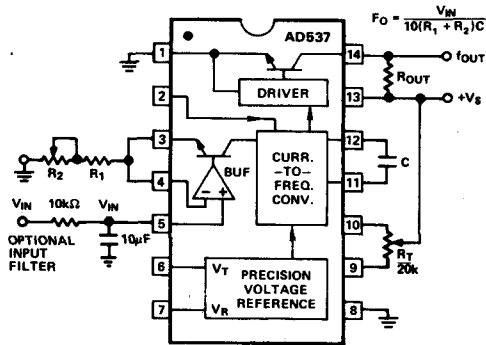
A block diagram of the AD537 is shown in Figure 1. A versatile operational amplifier (BUF) serves as the input stage; its purpose is to convert and scale the input voltage signal to a drive current in the NPN follower. Optimum performance is achieved when, at the full scale input voltage, a 1mA drive current is delivered to the current-to-frequency converter. The drive current to the current-to-frequency converter (an astable multivibrator) provides both the bias levels and the charging current to the externally connected timing capacitor. This "adaptive" bias scheme allows the oscillator to provide low nonlinearity over the entire current input range of 0.1 to 2000 $\mu$ A. The square wave oscillator output goes to the output driver which provides a floating base drive to the NPN power transistor. This floating drive allows the logic interface to be referenced to a different level than  $-V_S$ . The "SYNC" input ("D" package only) allows the oscillator to be slaved to an external master oscillator; this input can also be used to shut off the oscillator.

The reference generator uses a band-gap circuit (this allows single-supply operation to 4.5 volts which is not possible with low T.C. zeners) to provide the reference and bias levels for the amplifier and oscillator stages. The reference generator also provides the precision, low T.C. 1.00 volt output and the  $V_{TEMP}$  output which tracks absolute temperature at  $1mV/^{\circ}K$ .

## V-F CONNECTION FOR POSITIVE INPUT VOLTAGES

The positive voltage input range is from  $-V_S$  (ground in single supply operation) to 4 volts below the positive supply. The connection shown in Figure 3 provides a very high (250M $\Omega$ ) input impedance. The input voltage is converted to the proper drive current at pin 3 by selecting a scaling resistor. The full scale current is 1mA, so, for example a 10 volt range would require a nominal 10k $\Omega$  resistor. The trim range required will depend on capacitor tolerance. Full scale currents other than 1mA can be chosen, but linearity will be reduced; 2mA is the maximum allowable drive.

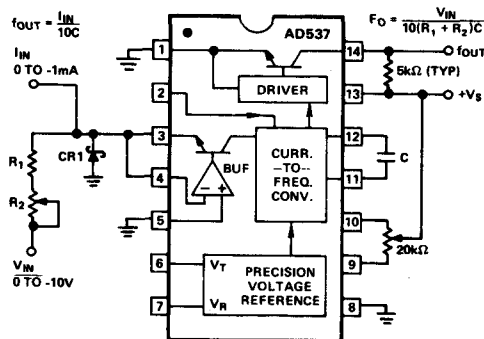
As indicated by the scaling relationship in Figure 3, a  $0.01\mu\text{F}$  timing capacitor will give a 10kHz full scale frequency, and  $0.001\mu\text{F}$  will give 100kHz with a 1mA drive current. The maximum frequency is 150kHz. Polystyrene or NPO ceramic capacitors are preferred for T.C. and dielectric absorption; polycarbonate or mica are acceptable; other types will degrade linearity. The capacitor should be wired very close to the AD537.



**Figure 3. Standard V-F Connection for Positive Input Voltages**  
**V-F CONNECTIONS FOR NEGATIVE INPUT VOLTAGE OR CURRENT**

A wide range of negative input voltages can be accommodated with proper selection of the scaling resistor, as indicated in Figure 4. This connection, unlike the buffered positive connection, is not high impedance since the 1mA F.S. drive current must be supplied by the signal source. However, very large negative voltages beyond the supply can be handled easily; just modify the scaling resistors appropriately. Diode CR1 (HP5082-2811) is necessary for overload and latchup protection for current or voltage inputs.

If the input signal is a true current source,  $R_1$  and  $R_2$  are not used. Full scale calibration can be accomplished by connecting a  $200\text{k}\Omega$  pot in series with a fixed  $27\text{k}\Omega$  from pin 7 to  $-V_S$  (see calibration section, below).



**Figure 4. V-F Connections for Negative Input Voltage or Current**

### CALIBRATION

There are two independent adjustments: scale and offset. The first is trimmed by adjustment of the scaling resistor  $R$  and the second by the (optional) potentiometer connected to  $+V_S$  and the  $V_{OS}$  pins ("D" package only). Precise calibration requires the use of an accurate voltage standard set to the desired FS value and a frequency meter; a scope is useful for monitoring

output waveshape. Verification of linearity requires the availability of a switchable voltage source (or a DAC) having a linearity error below  $\pm 0.005\%$ , and the use of long measurement intervals to minimize count uncertainties. *Every AD537 is automatically tested for linearity*, and it will not usually be necessary to perform this verification, which is both tedious and time-consuming.

Although drifts are small it is good practice to allow the operating environment to attain stable temperature and to ensure that the supply, source and load conditions are proper. Begin by setting the input voltage to 1/10,000 of full scale. Adjust the offset pot until the output frequency is 1/10,000 of full scale (for example 1Hz for FS of 10kHz). This is most easily accomplished using a frequency meter connected to the output. Then apply the FS input voltage and adjust the gain pot until the desired FS frequency is indicated. In applications where the FS input is small, this adjustment will very slightly affect the offset voltage, due to the input bias current of the buffer amplifier. A change of  $1\text{k}\Omega$  in  $R$  will affect the input by approximately  $100\mu\text{V}$ , which is as much as 0.1% of a 100mV FS range. Therefore, it may be necessary to repeat the offset and scale adjustments for the highest accuracy. The design of the input amplifier is such that the input voltage drift after offset nulling is typically below  $1\mu\text{V}/^\circ\text{C}$ .

In some cases the signal may be in the form of a negative current source. This can be handled in a similar way to a negative input voltage. However, the scaling resistor is no longer required, eliminating the capability of trimming full scale in this fashion. Since it will usually be impractical to vary the capacitance, an alternative calibration scheme is needed. This is shown in Figure 5. A resistor-potentiometer connected from the  $V_R$  output to  $-V_S$  will alter the internal operating conditions in a predictable way, providing the necessary adjustment range. With the values shown, a range of  $\pm 4\%$  is available; a larger range can be attained by reducing  $R_1$ . This technique does not degrade the temperature-coefficient of the converter, and the linearity will be as for negative input voltages. The minimum supply voltage may be used.

Unless it is required to set the input node at exactly ground potential, no offset adjustment is needed. The capacitor  $C$  is selected to be 5% below the nominal value; with  $R_2$  in its mid-position the output frequency is given by

$$f = \frac{I}{10.5 \times C}$$

where  $f$  is in kHz,  $I$  is in mA and  $C$  is in  $\mu\text{F}$ . For example, for a FS frequency of 10kHz at a FS input of 1mA,  $C = 9500\text{pF}$ . Calibration is effected by applying the full-scale input and adjusting  $R_2$  for the correct reading.

This alternative adjustment scheme may also be used when it is desired to present an exact input resistance in the negative-voltage mode. The scaling relationship is then

$$f = \frac{V}{R_{\text{exact}}} \cdot \frac{1}{10.5 C}$$

The calibration procedure is then similar to that used for positive input voltages, except that the scale adjustment is by means of  $R_2$ .

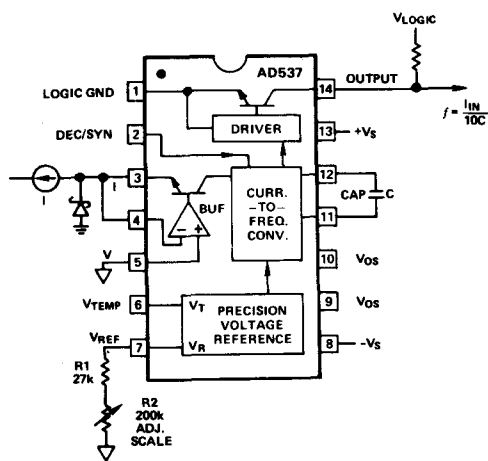


Figure 5. Scale Adjustment for Current Inputs

### INPUT PROTECTION

The AD537 was designed to be used with a minimum of additional hardware. However, the successful application of a precision IC involves a good understanding of possible pitfalls and the use of suitable precautions.

The  $-V_{IN}$ ,  $+V_{IN}$  and  $I_{IN}$  pins should not be driven more than 300mV below  $-V_S$ . This would cause internal junctions to conduct, possibly damaging the IC. The AD537 can be protected from "below  $-V_S$ " inputs by a Schottky diode, CR1 (HP5082-2811) as shown in Figure 4. It is also desirable not to drive  $+V_{IN}$ ,  $-V_{IN}$  and  $I_{IN}$  above  $+V_S$ . In operation, the converter will become very nonlinear for inputs above  $(+V_S - 3.5V)$ . Control currents above 2mA will also cause nonlinearity.

The 80dB dynamic range of the AD537 guarantees operation from a control current of 1mA (nominal FS) down to 100nA (equivalent to 1mV to 10V FS). Below 100nA improper operation of the oscillator may result, causing a false indication of input amplitude. In many cases this might be due to short-lived noise spikes which become added to the input. For example, when scaled to accept a FS input of 1V, the  $-80$ dB level is only 100 $\mu$ V, so when the mean input is only 60dB below FS (1mV), noise spikes of 0.9mV are sufficient to cause momentary malfunction.

This effect can be minimized by using a simple low-pass filter ahead of the converter. For a FS of 10kHz a single-pole filter with a time-constant of 100ms (Figure 3) will be suitable, but the optimum configuration will depend on the application and type of signal processing. Noise spikes are only likely to be a cause of error when the input current remains near its minimum value for long periods of time; above 100nA (1mV) full integration of additive input noise occurs.

The AD537 is somewhat susceptible to interference from other signals. The most sensitive nodes (besides the inputs) are the capacitor terminals and the SYNC pin. The timing capacitor should be located as close as possible to the AD537 to minimize signal pickup in the leads. In some cases, guard rings or shielding may be required. The SYNC pin should be decoupled through a 0.005 $\mu$ F (or larger) capacitor to pin 13 ( $+V_S$ ). This minimizes the possibility that

the AD537 will attempt to synchronize to a spurious signal. This precaution is unnecessary on the metal can package since the SYNC function is not brought out to a package pin and is thus not susceptible to pickup.

### DECOUPLING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100 $\Omega$ ) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1 $\mu$ F to 1.0 $\mu$ F should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD537.

A decoupling capacitor may also be useful from  $+V_S$  to SYNC in those applications where very low cycle-to-cycle period variation (jitter) is demanded. By placing a capacitor across  $+V_S$  and SYNC this noise is reduced. On the 10kHz FS range, a 6.8 $\mu$ F capacitor reduces the jitter to one in 20,000 which is adequate for most applications. A tantalum capacitor should be used to avoid errors due to dc leakage.

### OPERATION WITH NON-ZERO TC

The good temperature stability of the AD537 can only be realized using stable timing components. However, compensation for capacitors having a negative TC (such as polystyrene,  $-150 \pm 80$ ppm/ $^{\circ}$ C) can be easily introduced by adding a resistor between the  $+1$ mV/ $^{\circ}$ K output and  $-V_S$ . The value should be selected from the curve given in Figure 6. Over this range of compensation the scale factor is only slightly affected; the error is about  $+0.03\%$ /ppm/ $^{\circ}$ K in frequency (e.g., 150ppm shift would change the scale factor 4.5%).

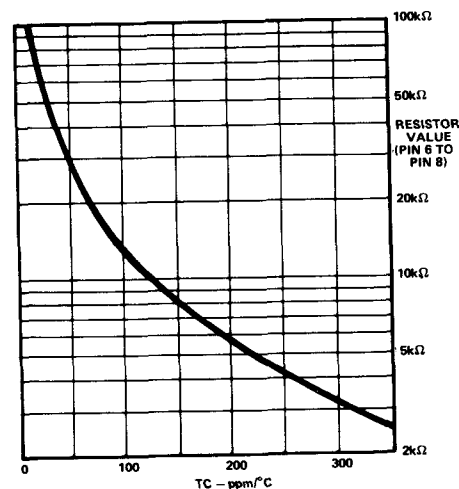


Figure 6. Positive T.C. Induced Versus Correction Resistance

### NONLINEARITY SPECIFICATION

The preferred method for specifying linearity error is in terms of the maximum deviation from the ideal relationship after calibrating the converter at full scale and "zero". This error will vary with the full scale frequency and the mode of operation. The AD537 operates best at a 10kHz full scale frequency with a negative voltage input; the linearity is typically within  $\pm 0.05\%$ . Operating at higher frequencies or with positive inputs will degrade the linearity as indicated in the specifications. The shape of a typical linearity plot is given in Figure 7.

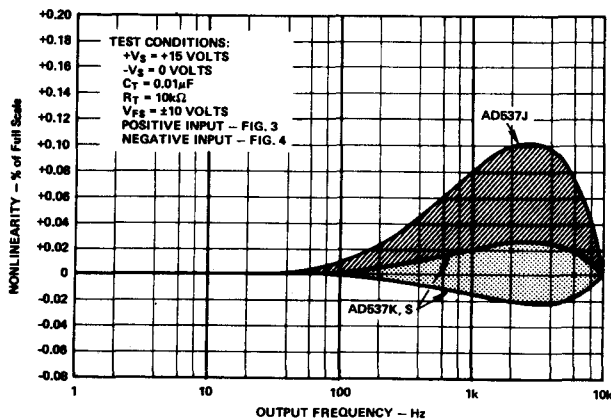


Figure 7a. Typical Nonlinearity Error Envelopes with 10kHz F.S. Output

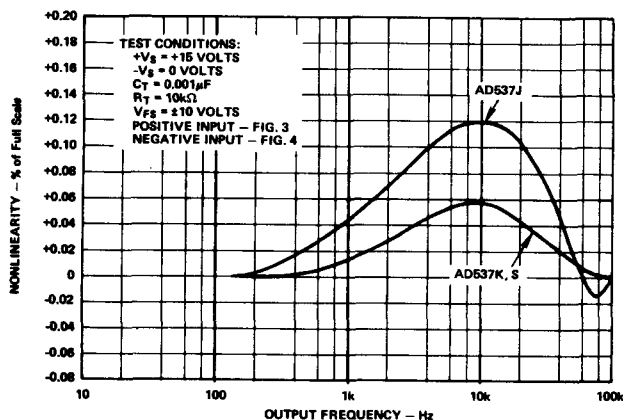


Figure 7b. Typical Nonlinearity Error with 100kHz F.S. Output

### OUTPUT INTERFACING CONSIDERATIONS

The design of the output stage allows easy interfacing to all digital logic families. The collector and emitter of the output NPN transistor are both uncommitted; the emitter can be tied to any voltage between  $-V_S$  and 4 volts below  $+V_S$ . The open collector can be pulled up to a voltage 36 volts above the emitter regardless of  $+V_S$ . The high power output stage can supply up to 20mA (10mA for "H" package) at a maximum saturation voltage of 0.4 volts. The stage limits the output current at 25mA; it can handle this limit indefinitely without damaging the device.

Figure 8 shows the AD537 with a standard 0 to +10 volt input connection and the output stage connections. The values for the logic common voltage, pull-up resistor, positive logic level, and  $-V_S$  supply are given in the accompanying chart for several logic forms.

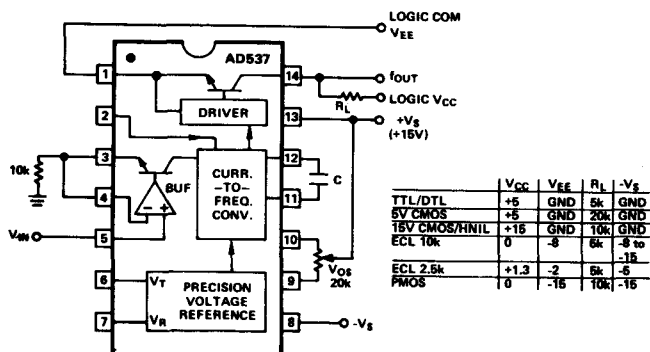


Figure 8. Interfacing Standard Logic Families

### APPLICATIONS

The diagrams and descriptions of the following applications are provided to stimulate the discerning engineer with alternative circuit design ideas. "Applications of the AD537 IC Voltage-to-Frequency Converter", available from Analog Devices on request, covers a wider range of topics and concepts in data conversion and data transmission using voltage-to-frequency converters.

### TRUE TWO-WIRE DATA TRANSMISSION

Figure 9 shows the AD537 in a true two-wire data transmission scheme. The twisted-pair transmission line serves the dual purpose of supplying power to the device and also carrying frequency data in the form of current modulation. The PNP circuit at the receiving end represents a fairly simple way for converting the current modulation back into a voltage square wave which will drive digital logic directly. The 0.6 volt square wave which will appear on the supply line at the device terminals does not affect the performance of the AD537 because of its excellent supply rejection. Also, note that the circuit operates at nearly constant average power regardless of frequency.

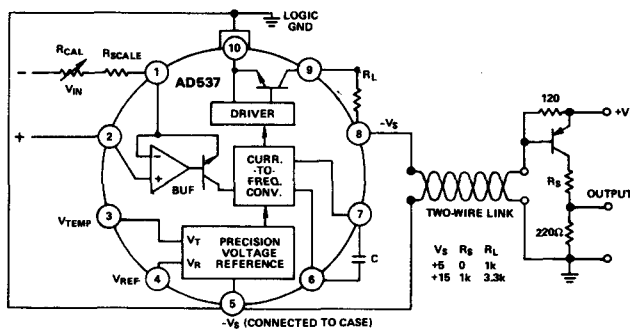


Figure 9. True Two-Wire Operation

### F-V CONVERTERS

The AD537 can be used as a high linearity VCO in a phase-locked loop to accomplish frequency-to-voltage conversion. By operating the loop without a low-pass filter in the feedback path (first-order system), it can lock to any frequency from zero to an upper limit determined by the design, responding in three or four cycles to a step change of input frequency. In practice, the overall response time is determined by the characteristics of the averaging filter which follows the PLL.

Figure 10 shows a connection using a low-power TTL quad open-collector nand gate which serves as the phase comparator. The input signal should be a pulse train or square wave with characteristics similar to TTL or 5-volt CMOS outputs. Any duty cycle is acceptable, but the minimum pulse width is 40µs. The output voltage is one volt for a 10kHz input frequency. The output as shown here is at a fairly high impedance level; for many situations an additional buffer may be required.

Trimming is similar to V-F application trimming. First set the  $V_{OS}$  trimmer to mid-scale. Apply a 10kHz input frequency and trim the 2kΩ potentiometer for 1.00 volts out. Then apply a 10Hz waveform and trim the  $V_{OS}$  for 1mV out. Finally, retrim the full scale output at 10kHz. Other frequency scales can be obtained by appropriate scaling of timing components.

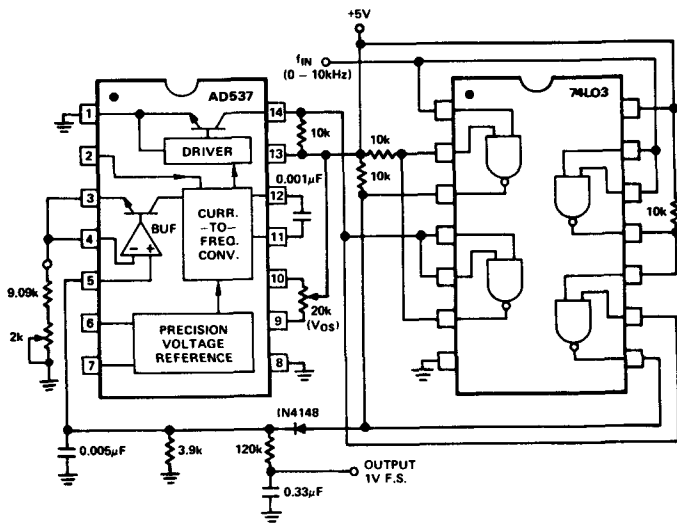


Figure 10. 10kHz F-V Converter

### TEMPERATURE-TO-FREQUENCY CONVERSION

The linear temperature-proportional output of the AD537 can be used as shown in these applications to perform various direct temperature-to-frequency conversion functions; it can also be used with other external connections in a temperature sensing or compensation scheme. If the sensor output is used externally, it should be buffered through an op amp since loading that point will cause significant error in the sensor output as well as in the main V-F converter circuitry.

An absolute temperature ( $^{\circ}$  Kelvin) -to-frequency converter is very easily accomplished, as shown in Figure 11. The 1mV per  $^{\circ}$  K output serves as the input to the buffer amplifier, which then scales the oscillator drive current to a nominal 298 $\mu$ A at +25 $^{\circ}$  C (298 $^{\circ}$  K). Use of a 1000pF capacitor results in a corresponding frequency of 2.98kHz. Setting the single 2k $\Omega$  trimmer for the correct frequency at a well-defined temperature near +25 $^{\circ}$  C will normally result in an accuracy of  $\pm 2^{\circ}$  C from -55 $^{\circ}$  C to +125 $^{\circ}$  C (using an AD537S). An NPO ceramic capacitor is recommended to minimize nonlinearity due to capacitance drift.

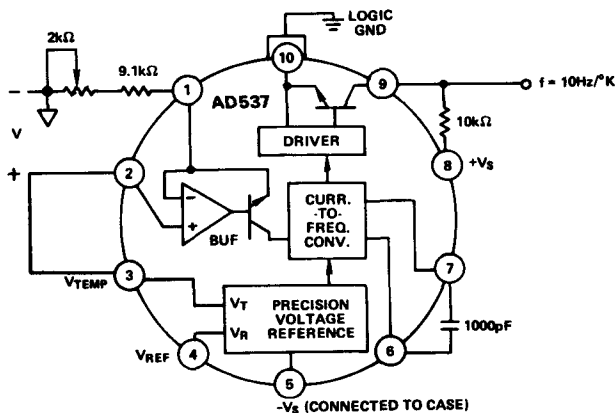


Figure 11. Absolute Temperature to Frequency Converter

### OFFSET TEMPERATURE SCALES

Many other temperature scales can be set up by offsetting the temperature output with the voltage reference output. Such a

scheme is shown by the Celsius-to-frequency converter in Figure 12. Corresponding component values for a Fahrenheit-to-frequency converter which give 10Hz/ $^{\circ}$  F are given in parentheses.

A simple calibration procedure which will provide  $\pm 2^{\circ}$  C accuracy requires substitution of a 7.27k resistor for the series combination of the 6.04k with the 2k trimmer; then simply set the 500 $\Omega$  trimmer to give 250Hz at +25 $^{\circ}$  C.

High accuracy calibration procedure:

1. Measure room temperature in  $^{\circ}$  K.
2. Measure temperature output at pin 6 at that temperature.
3. Calculate offset adjustment as follows:

$$\text{Offset Voltage (mV)} = \frac{V_{\text{TEMP}} (\text{pin 6}) (\text{mV})}{\text{Room temp } (^{\circ}\text{K})} \times 273.2$$

4. Temporarily disconnect 49 $\Omega$  resistor (or 500 $\Omega$  pot) and trim 2k $\Omega$  pot to give the offset voltage at the indicated node. Reconnect 49 $\Omega$  resistor.
5. Adjust slope trimmer to give proper frequency at room temperature (+25 $^{\circ}$  C = 250Hz).

Adjustment for  $^{\circ}$  F or any other scale is analogous.

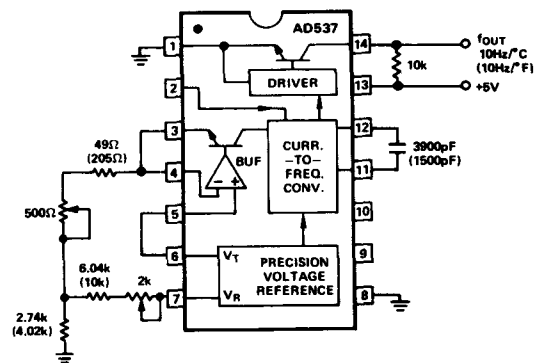


Figure 12. Offset Temperature Scale Converters-Centigrade and (Fahrenheit) to Frequency

### SYNCHRONOUS OPERATION

The SYNC terminal at pin 2 of the DIP package can be used to synchronize a free running AD537 to a master oscillator, either at a multiple or a sub-multiple of the primary frequency. The preferred connection is shown in Figure 13. The diodes are used to produce the proper drive magnitude from high level signals. The SYNC terminal can also be used to shut off the oscillator. Shorting the terminal to +V<sub>S</sub> will stop the oscillator, and the output will go high (output NPN off).

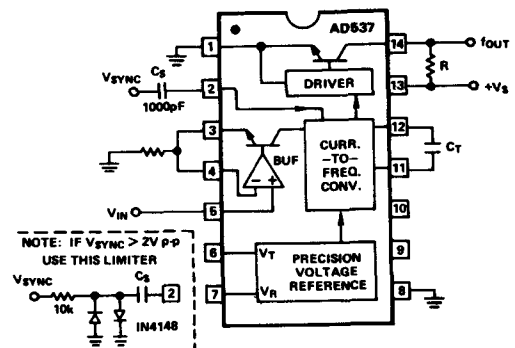


Figure 13. Connection for Synchronous Operation

Figure 14 shows the maximum pull-in range available at a given signal level; the optimum signal is a 0.8 to 1.0 volt square wave; signals below 0.1 volt will have no effect; signals above 2 volts p-p will disable the oscillator. The AD537 can normally be synchronized to a signal which forces it to a higher frequency up to 30% above the nominal free-running frequency, it can only be brought down about 1-2%.

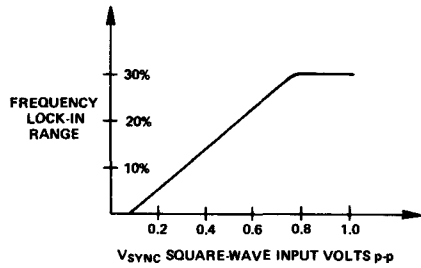


Figure 14. Maximum Frequency Lock-In Range Versus Sync. Signal

### LINEAR PHASE LOCKED LOOP

The phase-locked-loop F/V circuit described earlier operates from an essentially noise-free binary input. PLL's are also used to extract frequency information from a noisy analog signal. To do this, the digital phase-comparator must be replaced by a linear multiplier. In the implementation shown in Figure 15, the triangular waveform appearing across the timing capacitor is used as one of the multiplier inputs; the signal provides the other input. It can be shown that the mean value of the multiplier output is zero when the two signals are in quadrature. In this condition, the ripple in the error signal is also quite small. Thus, the voltage at pin 5 is essentially zero, and the frequency is determined primarily by the current in the timing resistor, controlled either manually or by a control voltage.

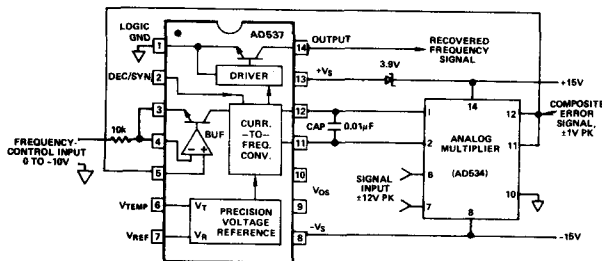


Figure 15. Linear Phase-Locked Loop

Noise on the input signal affects the loop operation only slightly; it appears as noise in the timing current, but this is averaged out by the timing capacitor. On the other hand, if the input frequency changes there is a net error voltage at pin 5 which acts to bring the oscillator back into quadrature. Thus, the output at pin 14 is a noise-free square-wave having exactly the same frequency as the input signal. The effectiveness of this circuit can be judged from Figure 16 which shows the response to an input of 1V rms 1kHz sinusoid plus 1V rms Gaussian noise. The positive supply to the AD537 is reduced by about 4V in order to keep the voltages at pins 11 and 12 within the common-mode range of the AD534.

Since this is also a first-order loop the circuit possesses a very wide capture range. However, even better noise-integrating properties can be achieved by adding a filter between the multiplier output and the VCO input. Details of suitable filter characteristics can be found in the standard texts on the subject.

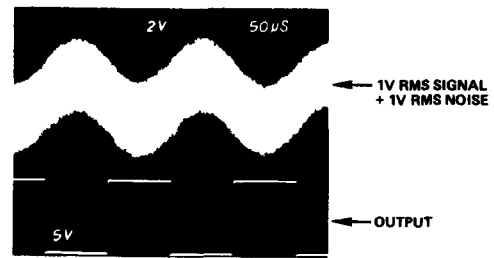


Figure 16. Performance of AD537 Linear Phase-Locked Loop

By connecting the multiplier output to the lower end of the timing resistor and moving the control input to pin 5, a high-resistance frequency-control input is made available. However, due to the reduced supply voltage, this input cannot exceed +6V.

### TRANSDUCER INTERFACE

The AD537 was specifically designed to accept a broad range of input signals, particularly small voltage signals, which may be converted directly (unlike many V-F converters which require signal pre-conditioning). The 1.00V stable reference output is also useful in interfacing situations, and the high input resistance allows non-loading interfacing from a source of varying resistance, such as the slider of a potentiometer.

### THERMOCOUPLE INPUT

The output of a Chromel-Constantan (Type E) thermocouple, using a reference junction at 0°C, varies from 0 to 53.14mV over the temperature range 0 to +700°C with a slope of 80.678µV/degree over most of its range and some nonlinearity over the range 0 to +200°C. For this example, we assume that it is desired to indicate temperature in Degrees Celsius using a counter/display with a 100ms gate width. Thus, the V-F converter must deliver an output of 7kHz for an input of 53.14mV. If very precise operation down to 0°C is imperative, some sort of linearizing is necessary (see, for example, Analog Devices' Nonlinear Circuits Handbook, pp92-97) but in many cases operation is only needed over part of the range.

The circuit shown in Figure 17 provides good accuracy from +300°C to +700°C. The extrapolation of the temperature-voltage curve back to 0°C shows that an offset of -3.34mV is required to fit the curve most exactly. This small amount of voltage can be introduced without an additional calibration step using the +1.00V output of the AD537. To adjust the scale, the thermocouple should be raised to a known reference temperature near 500°C and the frequency adjusted to value using R1. The error should be within ±0.2% over the range 400°C to 700°C.

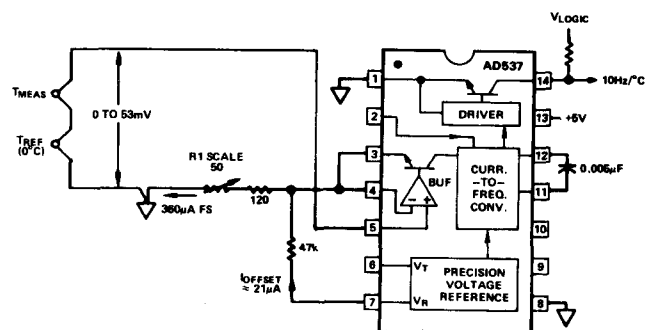
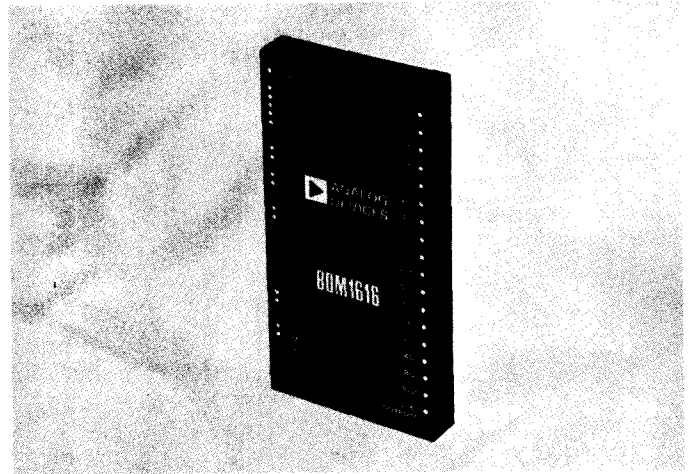


Figure 17. Thermocouple Interface with First-Order Linearization

**FEATURES**

- Binary Angle to Modulo 360° BCD Output
- Rounding Errors <math><0.005^\circ</math>
- All TTL Levels
- Fast Parallel Operation



**DESCRIPTION**

The BDM 1615/1616/1617 converters are solid state converters which take as inputs angular data in binary form and give out angular data in Binary Coded Decimal form—modulo 360°. The code converters are available in two versions. The first is scaled in degrees and decimal fractions of degrees and the second version is scaled in degrees and minutes.

The BDM 1615 and 1616 accept 14 bit binary inputs and give data in degrees and decimal fractions of a degree, and degrees and minutes respectively.

The BDM 1617 accepts a 16 bit binary input and gives out data in degrees and decimal fractions of a degree.

Rounding errors are <math><0.02^\circ</math> for the BDM 1615 and <math><0.005^\circ</math> for the BDM 1617.

All the converters take in parallel data and give out parallel data; the time of operation is <math><0.5\mu s</math>.

With most synchro/resolver to digital converters the output digital angle is given in natural binary form with the bit weighting being 180°, 90°, 45° etc. While this natural binary form of angular information is suited for digital computer interfacing and direct angular transmission in serial form, it is not suited for direct conversion to visual digital displays or for use in computers using BCD coding. The BDMs (Binary Decimal Modules) 1615/1616/1617 have been designed to meet this interface requirement.

Two of the main applications for the BDMs are depicted in Figures 1 and 2. Figure 1 shows the BDM being used to convert the binary angular information from a synchro to digital converter into a suitable form for driving the visual display decoder and Figure 2 shows the BDM connected to the binary output from a computer to give a digital display.

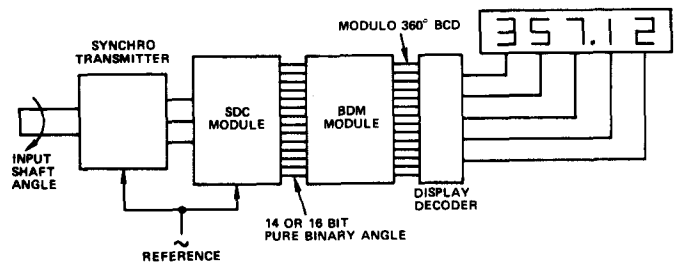


Figure 1.

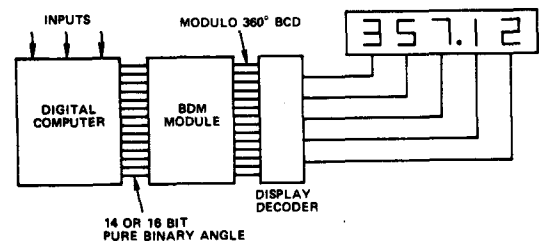


Figure 2.



# SPECIFICATIONS (typical @ +25°C unless otherwise noted)

| MODEL                 | BDM 1615   | BDM 1616  | BDM 1617                                      |
|-----------------------|--|---|---|
| Input                 | 14 Bits Natural Binary at TTL Levels   | *   | 16 Bits Natural Binary at TTL Levels          |
| Fan In                | 5 TTL Loads  | *   | *   |
| Output                | Modulo 360° and BCD<br>Fraction—0.01, 0.02, 0.04, 0.08, 0.1, 0.2, 0.4, 0.8°. | Modulo 360° and<br>Minutes Coded—40', 20', 10', 8', 4', 2', 1'. | *   |
| Fan Out               | 2 TTL Loads  | *   | *   |
| Mode of Operation     | Parallel In, Parallel Out  | *   | *   |
| Speed of Operation    | < 0.5μs  | *   | *   |
| Rounding Errors       | 0.02°  | 1 arc minute  | 0.005°  |
| Supply Voltage        | 5.0V ±5%   | *   | *   |
| Supply Current        | 350mA  | *   | 700mA   |
| Power                 | 1.75 Watts   | *   | 2.25 Watts                                    |
| Operating Temperature | 0 to +70°C<br>-50°C to +105°C  | *   | *   |
| Storage Temperature   | -55°C to +125°C  | *   | *   |
| Size                  | 4" x 2" x 0.4"<br>102mm x 51mm x 10mm  | *   | 3.125" x 2.625" x 0.8"<br>79mm x 67mm x 20mm  |
| Enable                | —  | —   | @ "0" = Normal Operation<br>@ "1" = LED Check |

\*Same specification as BDM 1615

Specifications subject to change without notice.

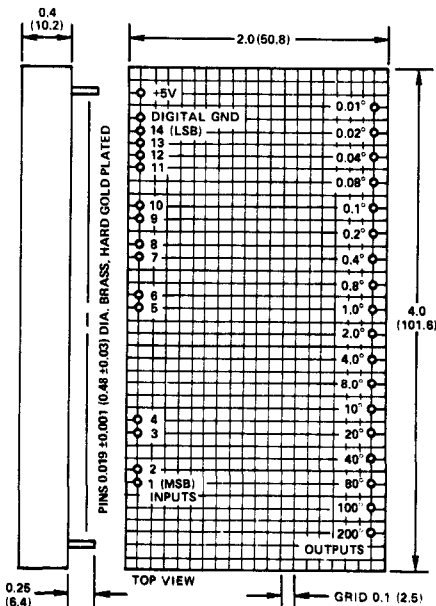
## ORDERING INFORMATION

Each of the BDMs is available in either of two versions according to the required operating temperature range. The type number must be followed by a code defining the required temperature range; the code is 500 for 0 to +70°C and 600 for -55°C to +105°C.

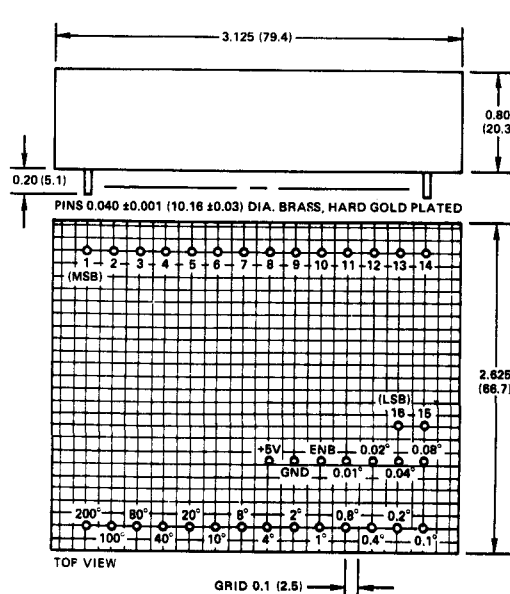
e.g., BDM 1616/600 is for a temperature range of -55°C to +105°C.

## PIN CONNECTIONS AND OUTLINE DIMENSIONS

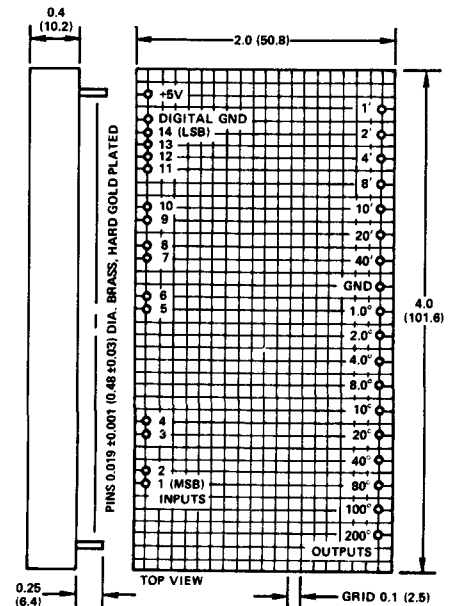
Dimensions shown in inches and (mm).



BDM1615



BDM1617



BDM1616

### FEATURES

- Very Low Radius Vector Variation (Transformation Ratio) ( $\pm 0.1\%$ )
- High Accuracy ( $\pm 2$  arc-mins at  $+25^\circ\text{C}$ )
- 12 or 14 Bit Resolution
- No 5 Volt Power Supply Required
- MIL Spec/Hi Rel Versions Available
- Internal 1.3VA Amplifiers
- Internal Transformers (400Hz Option)
- No Trims or Adjustments Necessary

### APPLICATIONS

- Driving Control Transformers
- Driving Torque Receivers (with External Amplifiers)
- Servo Mechanisms
- Retransmission Systems
- Positional Control

### GENERAL DESCRIPTION

The DSC1705 and DSC1706 are Digital to Synchro and Digital to Resolver converters capable of driving electromechanical loads of up to 1.3VA.

They accept a 14 or 12 bit digital input representing angle and a reference voltage of either 60Hz or 400Hz, and produce a 3 wire or 4 wire output suitable for driving Synchros or Resolvers.

The 400Hz converters contain internal 1.3VA amplifiers as well as output and reference transformers.

The 60Hz versions contain internal 1.3VA amplifiers but require external output and reference transformers.

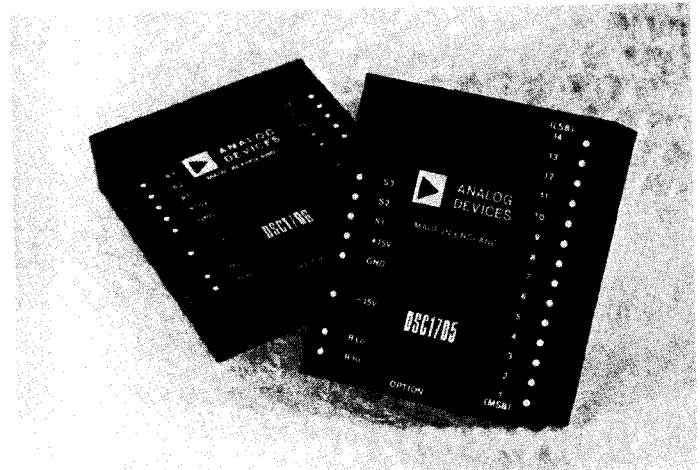
If it is necessary to drive a load requiring more than 1.3VA, options for both the 400Hz and 60Hz converters are available allowing the use of external amplifiers and transformers.

### RADIUS VECTOR

One of the outstanding features of these converters is the almost negligible Radius Vector variation (Transformation Ratio).

On many Digital to Synchro Converters presently available, the individual sine and cosine outputs produced do not follow the exact sine and cosine laws, and depending upon angle can vary up to  $\pm 7\%$ . This is not always important as the ratio of the sine to the cosine, i.e., the tangent, is always correct to the specified accuracy of the converter. There are cases however, when driving torque receivers and certain servo control loops when this variation is unacceptable.

*The design of the DSC1705 and DSC1706 has reduced this variation to less than  $\pm 0.1\%$ . This means that when the converters are used in closed loop servo systems, the gain of the closed loop is independent of the digital input angle, thus making reference correction unnecessary.*



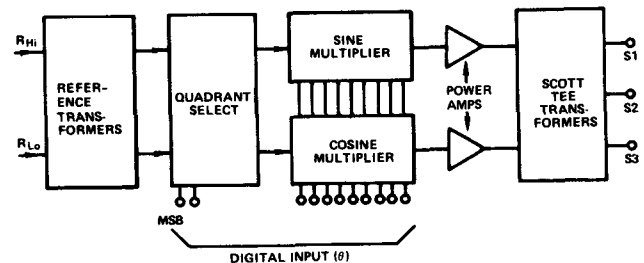
### MODELS AVAILABLE

The two Digital to Synchro/Resolver converters described in this data sheet differ primarily in the areas of resolution and accuracy as follows:-

Model DSC1705XYZ is a 14 bit converter with an overall accuracy of  $\pm 4$  arc-minutes.

Model DSC1706XYZ is a 12 bit converter with an overall accuracy of  $\pm 8$  arc-minutes.

The XYZ option code defines the option thus: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the output and the reference voltages, whether the output is in Synchro or Resolver format and whether external transformers are required.



*Principle of Operation*

### FUNCTIONAL DIAGRAM, DSC1705 and DSC1706

The principle of operation of the converters described in this data sheet is shown in the diagram above.

# SPECIFICATIONS (typical @ +25°C unless otherwise noted)

| Model   | DSC1705  | DSC1706   |
|---|--|---|
| ACCURACY <sup>1</sup>                                     | ±4 arc-minutes                                       | ±8 arc-minutes                                  |
| RESOLUTION  | 14 Bits (1LSB = 1.3 arc-minutes)                     | 12 Bits (1LSB = 5.3 arc-minutes)                |
| INPUT CODE  | 14 Bits Natural Parallel Binary with MSB = 180°      | 12 Bits Natural Parallel Binary with MSB = 180° |
| REFERENCE VOLTAGE INPUT                                   |  |   |
| With Internal Transformers                                |  |   |
| Low Level   | 26V rms  | *   |
| High Level  | 115V rms   | *   |
| External Transformer Options <sup>2</sup>                 | 4V rms   | *   |
| REFERENCE FREQUENCY                                       | 60Hz or 400Hz  | *   |
| REFERENCE INPUT IMPEDANCE                                 |  |   |
| With Internal Transformers                                |  |   |
| Low Level   | 20kΩ   | *   |
| High Level  | 200kΩ  | *   |
| External Transformer Options <sup>2</sup>                 | 10kΩ   | *   |
| DIGITAL INPUT (TTL COMPATIBLE)                            | 1TTL Load  | *   |
| OUTPUT VOLTAGE AND FORMAT                                 |  |   |
| With Internal Transformers                                |  |   |
| Low Level   | 11.8V rms Line-to-Line Synchro or Resolver           | *   |
| High Level  | 90V rms Line-to-Line Synchro or Resolver             | *   |
| External Transformer Options <sup>3</sup>                 | 7V rms Sine and Cosine                               | *   |
| LOAD CAPABILITY   | 1.3VA  | *   |
| SHORT CIRCUIT PROTECTION                                  | Continuous for 5 minutes                             | *   |
| OUTPUT SETTLING TIME <sup>4</sup>                         | 50μs for 180° Step                                   | *   |
| RADIUS VECTOR VARIATION (Transformation Ratio)            | ±0.1% max Sine and Cosine                            | *   |
| INTERNAL TRANSFORMER ISOLATION                            | 500V dc  | *   |
| POWER SUPPLIES  |  |   |
| Voltage   | ±15V dc ±5%  | *   |
| Current   |  |   |
| (a) No Load   | 95mA per Line  | *   |
| (b) Full Load Mean  | 225mA per Line                                       | *   |
| WARM-UP TIME  | 1sec to Full Accuracy                                | *   |
| OPERATING TEMPERATURE RANGE                               | 0 to +70°C Standard<br>-55°C to +105°C Extended      | *   |
| STORAGE TEMPERATURE RANGE                                 | -55°C to +125°C                                      | *   |
| SIZE  | 3.125" x 2.625" x 0.8"<br>(79.4mm x 66.7mm x 20.3mm) | *   |
| WEIGHT  | 8 ounces (224 grams) max                             | *   |
| MEAN TIME BETWEEN FAILURES (MTBF) CALCULATED <sup>5</sup> | 150,000 Hours  | *   |

## NOTES

<sup>1</sup> Accuracy applies over the full operating temperature range of the option and for:

- (a) ±10% reference frequency and amplitude variation.
- (b) 10% harmonic distortion on the reference.
- (c) ±5% power supply variation.
- (d) Any balanced load from no load to full load.

<sup>2</sup> Refers to input to converter and not to external transformers.

<sup>3</sup> Refers to output from internal converter amplifiers and not from external transformers.

<sup>4</sup> Dependent upon option and load conditions.

<sup>5</sup> With MIL-STD-883B components.

Specifications subject to change without notice.

## CONNECTING THE CONVERTER

**400Hz options.** All these converters contain internal output and reference transformers.

The digital input should be connected to pins "1" through "12" on the DSC1706 and pins "1" through "14" on the DSC1705, noting that pin "1" is the Most Significant Bit (MSB).

"S1", "S2" and "S3" should be connected to the appropriate inputs on the synchro being driven. ("S4" is used also when connection is made to a resolver).

The reference should be connected to "R<sub>Hi</sub>" and "R<sub>Lo</sub>" ensuring that the phase is correct.

"GND" is the common for both power supplies and digital inputs.

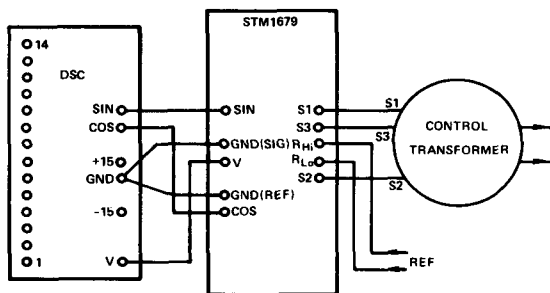
**60Hz Options.** For 60Hz operation, an external transformer, STM1679 is required.

The power supplies and digital input should be connected as for the 400Hz version.

The STM1679 transformer should have its pins "SIN", "COS" and "V" connected to the equivalent pins on the converter. The "GND(SIG)" and "GND(REF)" should both be connected to "GND" on the converter.

The outputs to the load should be taken from "S1", "S2" and "S3" on the STM1679 transformer ("S4" also in the case of a resolver).

The reference input should be made to "R<sub>Hi</sub>" and "R<sub>Lo</sub>" on the STM1679.



*60Hz Connection to a Control Transformer  
(Diagram Shows Bottom View of Modules)*

## OPERATION WITH EXTERNAL AMPLIFIERS OR TRANSFORMER OTHER THAN STM1679

For certain applications, the power output required by the load will be greater than the 1.3VA supplied by the internal amplifiers. Thus external amplifiers and transformers will be needed. Products offered to fulfill this requirement are:

SPA1695 – Dual 5VA Amplifier

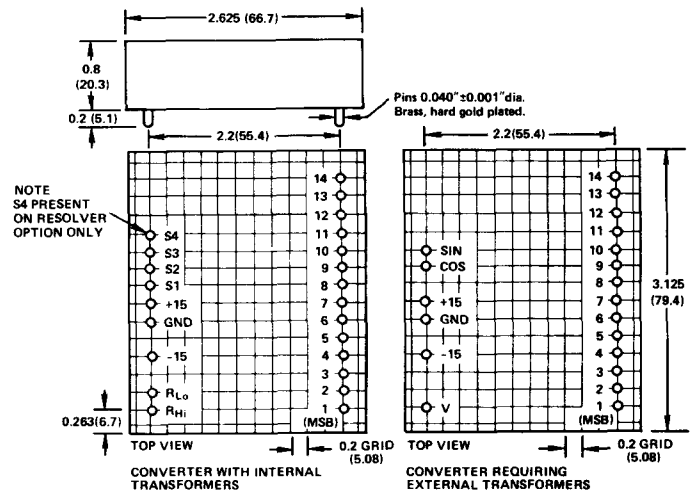
STM1696 – 5VA output and reference transformers (400Hz)

STM1697 – 5VA output and reference transformers (60Hz)

If you have a requirement for such products please request the data sheet.

## CONVERTER OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

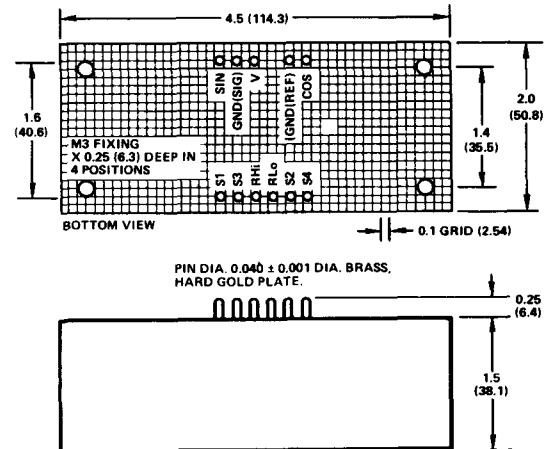
Dimensions shown in inches and (mm).



NOTE  
DIAGRAMS ABOVE SHOW DSC1705.  
DSC1706 DOES NOT HAVE PINS "13" AND "14".

## TRANSFORMER (STM1679) OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).



\*S4 PIN PRESENT FOR RESOLVER OPTION ONLY

## BIT WEIGHT TABLE

| Bit Number           | Weight in Degrees |
|----------------------|-------------------|
| 1 (MSB)              | 180.0000          |
| 2                    | 90.0000           |
| 3                    | 45.0000           |
| 4                    | 22.5000           |
| 5                    | 11.2500           |
| 6                    | 5.6250            |
| 7                    | 2.8125            |
| 8                    | 1.4063            |
| 9                    | 0.7031            |
| 10                   | 0.3516            |
| 11                   | 0.1758            |
| 12 (LSB for DSC1706) | 0.0879            |
| 13                   | 0.0439            |
| 14 (LSB for DSC1705) | 0.0220            |

## LOADING THE DSC's WITH CONTROL TRANSFORMERS (CT's)

The most common device to be driven by Digital to Synchro converters is the control transformer (CT)

The minimum power required to drive a CT can be expressed as:

$$(VA) = \frac{V^2}{|Z_{so}|} \cdot \frac{3}{4}$$

where V is the line to line voltage and  $Z_{so}$  is the impedance between one input terminal and the other two shorted together with the rotor open circuit. ( $Z_{so} = R_{so} + j X_{so}$ )

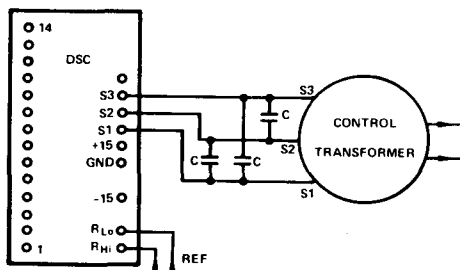
For example, if a CT has a  $Z_{so}$  of  $700 + j 4900$  and a line to line voltage of 90 volts, then:

$$|Z_{so}| = \sqrt{700^2 + 4900^2} = 4950 \text{ Ohms}$$

$$\text{and } (VA) = \frac{90^2}{4950} \cdot \frac{3}{4} = 1.23VA$$

## TUNING CT LOADS

The load can be reduced by tuning the output with 3 capacitors as shown below.



Capacitor Connection for Tuning CT's

C should be equal to:

$$\frac{X_{so}}{2\omega (R_{so}^2 + X_{so}^2)}$$

The power required after tuning will be:

$$(VA)_{\text{untuned}} \times \frac{R_{so}}{Z_{so}}$$

Therefore in the above example the capacitor value should be:

$$\frac{4900}{2 \times 2\pi \times 400 (245 \times 10^5)} = 40nF$$

and the power required after tuning will be:

$$1.23 \times \frac{700}{4950} = 0.17VA$$

Note allowance should always be made for tolerances in the CT windings, capacitors and frequency.

## PRACTICAL CONSIDERATIONS OF TUNING CT LOADS

1. The capacitors used need not be of high tolerance, 20% is sufficient.
2. Three capacitors must be used, one across S1 and S2, one across S1 and S3 and one across S2 and S3.
3. Voltage working and type of capacitors should be as follows:

### 11.8V Line-to-Line options:

15 Volt ac working or greater, non-polarized tantalum type.

### 90V Line-to-Line options:

100 Volt ac working or greater, for example, low K ceramic types.

4. For tuning Resolver loads, two capacitors only are required, one connected between S1 and S3 and the other connected between S2 and S4.

## CONTROL DIFFERENTIAL TRANSMITTERS (CDX's)

The loading on a DSC of these devices can be considered in a similar way to that of CT's. However because a CT normally follows a CDX, the effective Z will need to be calculated. This value will normally be between 66% and 80% of the  $Z_{so}$  quoted for the CDX.

## TORQUE RECEIVERS (TR's)

Torque receivers are more difficult devices to drive than CT's and CDX's, and in general external amplifiers and transformers will be necessary. However, because of the lack of radius vector variation, the DSC1705 and DSC1706 are far more suited to driving TR's than converters with a variation of  $\pm 7\%$ .

For a deviation of an angle  $\theta$ , the drive current required will be:

$$\frac{2 \cdot V \cdot \sin \frac{\theta}{2}}{|Z_{ss}|}$$

Points to be observed are:

- (a) The TR should not be allowed to lock up.
- (b) A phase lead equal to that specified for the TR should be introduced into the reference input to the DSC.
- (c) The reference should always be present on the TR and the converter.
- (d) The DSC output voltage should be matched exactly to the voltage requirements of the TR.

## CAUTIONS

- (a) Do not connect a 115V reference to a 26V converter.
- (b) Do not reverse the power supplies.
- (c) Do not connect the reference to any other pins except "R<sub>Hi</sub>" and "R<sub>Lo</sub>"

## ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by an option code in order to fully define the item. All standard options and their appropriate option codes are listed below.

| Part Number <sup>1</sup>  | Resolution | Operating Temp. Range | Line-to-Line Output Voltage and Format | Reference Voltage | Reference Frequency |
|---------------------------|------------|-----------------------|--|-------------------|---------------------|
| DSC1705511                | 14 Bits    | 0 to +70°C            | 11.8V Synchro                          | 26V               | 400Hz               |
| DSC1705512                | 14 Bits    | 0 to +70°C            | 90.0V Synchro                          | 115V              | 400Hz               |
| DSC1705611                | 14 Bits    | -55°C to +105°C       | 11.8V Synchro                          | 26V               | 400Hz               |
| DSC1705612                | 14 Bits    | -55°C to +105°C       | 90.0V Synchro                          | 115V              | 400Hz               |
| DSC1705518                | 14 Bits    | 0 to +70°C            | 11.8V Resolver                         | 26V               | 400Hz               |
| DSC1705618                | 14 Bits    | -55°C to +105°C       | 11.8V Resolver                         | 26V               | 400Hz               |
| DSC1705507 and STM1679522 | 14 Bits    | 0 to +70°C            | 90.0V Synchro                          | 115V              | 60Hz                |
| DSC1705607 and STM1679622 | 14 Bits    | -55°C to +105°C       | 90.0V Synchro                          | 115V              | 60Hz                |

Note: 1. For 12 bit resolution, substitute DSC1706 in place of DSC1705 in the above.  
2. For options not shown above, consult the factory.

### FEATURES

- Accurate Sine, Cosine Multiplication
- 14 Bit Resolution
- 3 Arc mins Accuracy
- 0.1% Radius Accuracy
- Low Profile (0.4")
- Maximum Frequency to Full Accuracy 2.5kHz
- Low Feedthrough

### APPLICATIONS

- Digital to Synchro Conversion
- Displays
- Axis Rotation
- Simulators
- Numerical Control
- Prediction
- Vector Resolution
- Spectrum Analysis
- Ultra Low Frequency Oscillators



### GENERAL DESCRIPTION

The DTM1716 and DTM1717 are computing converters which have a digital angle input in natural binary form and a bipolar analog input  $V_i(t)$ . There are two analog outputs  $V_{01}(t)$  and  $V_{02}(t)$ , the outputs are related to the inputs by;

$$V_{01}(t) = V_i(t) \sin \phi(t) \quad V_{02}(t) = V_i(t) \cos \phi(t)$$

where  $\phi$  is the digital angular input.  $\phi$  ranges from 0 to 360°. The analog input has a range of  $\pm 10V$ ; the analog output has a range of  $\pm 10V$ .

The digital input has a resolution of 14 bits for the DTM1716 and 12 bits for the DTM1717. The modules are powered from  $\pm 15V$  supply lines.

If the output voltages are regarded as the components of a vector, the radius accuracy is better than 0.1% and the angular inaccuracy is less than 3 arc minutes for the DTM1716.

A block diagram of the DTM1716 is shown in Figure 1.

Particular attention has been paid in the design to achieve high accuracy in the sine and cosine generation so that they may be used separately as accurate functions.

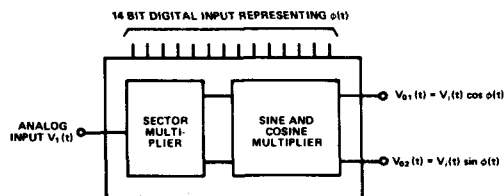


Figure 1. Diagram of DTM1716

Two models are available each with two options as shown below.

DTM1716500 has 14 bit digital input resolution and a 0 to +70°C operating temperature range.

DTM1716600 has 14 bit digital input resolution and a -55°C to +105°C operating temperature range.

DTM1717500 has a 12 bit digital input resolution and a 0 to +70°C operating temperature range.

DTM1717600 has a 12 bit digital input resolution and -55°C to +105°C operating temperature range.

### OPERATION

The operation of the DTM1716 is straightforward, being powered from  $\pm 15V$  lines relative to the common pin. No damage is caused by either the +15V or -15V being disconnected but they must not be reversed. The analog input is protected against a short circuit to either power line. The output is short circuit proof and can be connected to either power line without damage. The digital inputs are standard TTL levels. The module dimensions and pin out are shown in Figure 2.

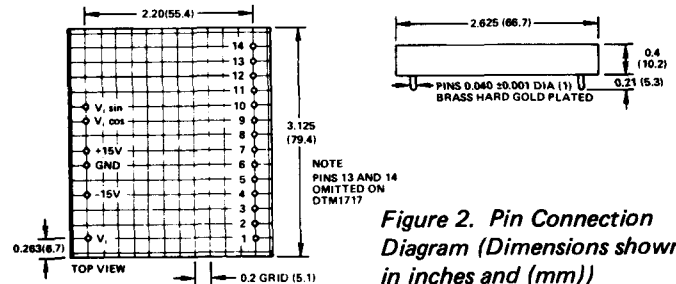


Figure 2. Pin Connection Diagram (Dimensions shown in inches and (mm))

# SPECIFICATIONS (typical @ +25°C unless otherwise noted)

| MODELS  | DTM1716  | DTM1717  |
|---|--|--|
| DIGITAL ANGULAR RESOLUTION                          | 14 bits (1 LSB = 1.3 arc-mins)                     | 12 bits (1 LSB = 5.3 arc-mins)                 |
| FULL SCALE OUTPUT                                   | ±10V   | *  |
| SCALING ACCURACY                                    | 0.1% FSR   | *  |
| FULL SCALE INPUT                                    | ±10V   | *  |
| SCALE TEMPCO  | 25ppm/°C of FSR                                    | *  |
| ZERO OFFSET   | 2.5mV  | *  |
| OFFSET DRIFT  | 50µV/°C  | *  |
| AC ACCURACY   |  |  |
| Analog Step Response<br>(10V Step)                  | 40µs<br>(to 0.1%)                                  | *  |
| MAX SLEW RATE                                       | 0.5V/µs  | *  |
| FULL POWER OUTPUT                                   | 8kHz   | *  |
| FEEDTHROUGH   | <1mV at 400Hz                                      | *  |
| ANALOG INPUT IMPEDANCE                              | 10kΩ   | *  |
| ANALOG OUTPUT IMPEDANCE                             | 100mΩ  | *  |
| OUTPUT LOAD   | 2kΩ  | *  |
| OUTPUT PROTECTION                                   | Short circuit proof                                | *  |
| DIGITAL INPUT                                       | 14 bit natural parallel binary,<br>1 TTL Load      | 12 bits natural parallel binary,<br>1 TTL Load |
| RESPONSE TO DIGITAL STEP<br>(90°) (FS Analog Input) | 40µs to 0.1% of final value                        | *  |
| VECTOR ACCURACY <sup>1</sup>                        |  |  |
| Radius Error  | 0.1% FSR   | *  |
| Angular Error                                       | ±3 arc-mins  | *  |
| POWER SUPPLY REJECTION                              | 80dB   | *  |
| POWER SUPPLIES                                      | +15V @ 50mA max<br>-15V @ 40mA max                 | *<br>*   |
| TEMPERATURE RANGE                                   | 0 to +70°C Standard<br>or -55°C to +105°C extended | *<br>*   |
| Operating   |  | *  |
| Storage   | -55°C to +125°C                                    | *  |
| DIMENSIONS  | 3.125 x 2.625 x 0.4"<br>79.4 x 66.7 x 10.2mm       | *  |
| WEIGHT  | 3 oz (85 grams)                                    | *  |

## NOTES

\*Specification same as DTM1716.

<sup>1</sup> See Figure 4.

Specifications subject to change without notice.

## APPLICATIONS OF THE DTM1716

Figure 3 shows how the DTM1716 can be used in radars and radar simulators for modulating display sawtooth generators using signals derived from a synchro transmitter on the antenna and a Synchro to Digital converter. The synchro signal representing the antenna angle is converted to a 14 bit natural binary representation by the Synchro to Digital converter SDC1704. The digital angle is applied to the digital input of the DTM1716. A dc voltage is applied to the DTM1716 analog input which controls the radius of the displayed raster. The output voltages are used to provide the X and Y time base currents. The switches across the capacitors are opened on the leading edge of the transmission pulse and closed after a time interval determined by the range.

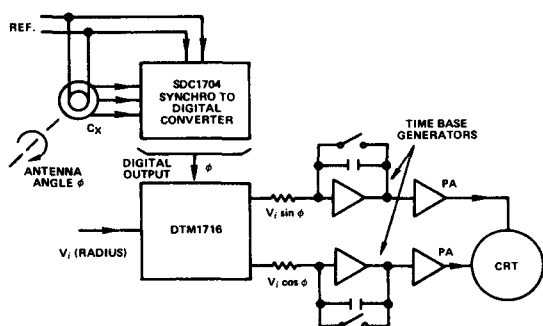


Figure 3. PPI Waveform Generation Using the DTM1716

## AXIS ROTATION

Figure 4 shows how two DTM1716's may be used to compute the new two dimensional coordinates of a point relative to a rotated set of axes. The input voltage  $X_1$  and  $Y_1$  are proportional to the coordinates of a point in the XY plane. If a digital angle  $\phi$  is applied to the DTM1716's, the output voltages  $X_2$  and  $Y_2$  correspond to the X and Y coordinates of the point relative to a set of axes rotated through the angle  $\phi$ . The systems can be extended to three dimensions.

The arrangement as shown in Figure 4 may also be used to obtain the new coordinates of a point which is rotated through the angle in the same coordinate set. This scheme provides a low cost, accurate and compact solution to transformation problems.

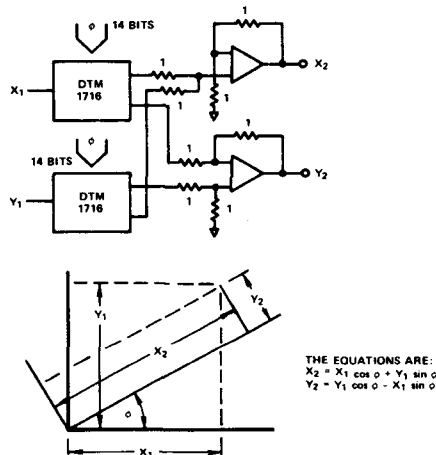


Figure 4. Axis Rotation in Two Dimensions Using the DTM1716

## SYNCHRO TO INVARIANT SINE/COSINE

In many engineering applications it is required to obtain voltages proportional to the sine and cosine of an angular movement and to be able to scale the voltages electrically. Figure 5 shows how a Synchro to Digital converter and the DTM1716 may be used for this purpose. The advantage of this scheme is that the coefficients of sine and cosine are electrically scalable by means of the bipolar voltage  $V_i$ , saving memory space, multipliers, power and space.

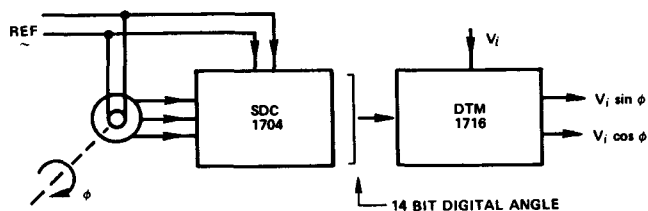


Figure 5. Synchro to Invariant Sine/Cosine Using the SDC1704 and DTM1716

## POWER SPECTRUM ANALYSIS

Figure 6 shows a less usual application of the DTM1716 in the spectrum analysis of low frequency signals. This has the advantage of providing almost infinite resolution at extremely low relative cost.

A simple method of obtaining the power in the frequency interval  $f \pm \Delta f$  is shown in Figure 6.

The input waveform from which the power spectrum is required is  $g(t)$ . Multiplication of this waveform by  $\sin 2\pi ft$  causes the energy in the waveform between  $f - \Delta f$  and  $f + \Delta f$  to be shifted to lie between  $-\Delta f$  and  $f + \Delta f$ . The low pass filter passes this voltage waveform to the square law devices to produce an output proportional to the power. Two channels, sine and cosine, are used for the case where  $g(t)$  may contain a periodic component. If for example there is a line in the power spectrum, without the use of the two channels the output at that frequency would depend upon its phase. The use of both sine and cosine multiplication avoids this problem.

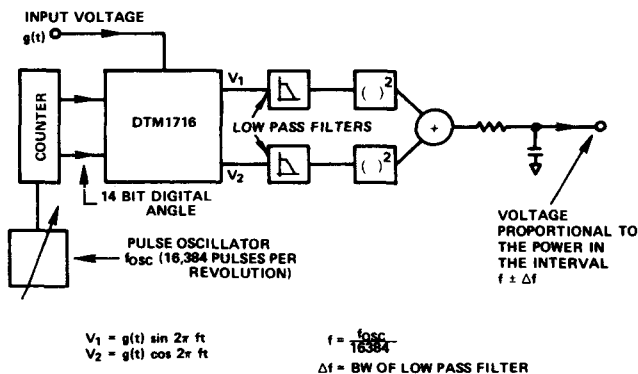


Figure 6. The Use of the DTM1716 to Obtain the Power Frequency Spectrum of  $g(t)$



## PHASE MODULATION

The DTM1717 can be used for low frequency phase modulation of subcarriers. Figure 7 shows the method which uses two DTM1717's and an ADC. Frequency modulation can be obtained if the amplitude of the signal is made to be inversely proportional to its frequency. This can be accomplished by inserting an integrator in series with the modulation input. Similar techniques can be used for very low frequency synthesis.

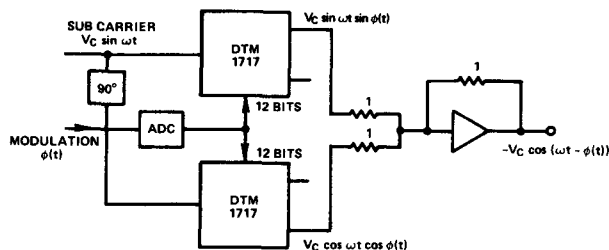


Figure 7. Phase Modulation Using 2 DTM1717's

## ORDERING INFORMATION

There are only two options for each of the DTM1716 and DTM1717. They are the commercial or extended temperature ranges. The appropriate designations are as follows:

DTM1716500 (14 bits) 0 to +70°C

DTM1716600 (14 bits) -55°C to +105°C

DTM1717500 (12 bits) 0 to +70°C

DTM1717600 (12 bits) -55°C to +105°C

## OTHER PRODUCTS

Many modules concerned with the conversion of synchro data

are manufactured by us, some of which are listed below. If you have any questions about our products or require advice about their use for a particular application, please contact our Applications Engineering Department.

## SYNCHRO TO DIGITAL CONVERTERS

The SDC1700 is a low profile (0.4") converter with a 12 bit natural binary output. Its overall accuracy is  $\pm 8.5$  arc-minutes, and the module contains internal transformers for all reference frequency options including 60Hz.

The SDC1702 is similar to the new SDC1700 but has a 10 bit natural binary output and an overall accuracy of +22 arc-minutes.

The SDC1704 is similar to the above two converters, but has a 14 bit natural binary output and an overall accuracy of  $\pm 2.0$  arc-minutes  $\pm 1$ LSB.

The SBCD1752/1753/1756 and 1757 are Synchro to Digital converters based on the SDC1700 which give an output in BCD format.

## DIGITAL TO SYNCHRO CONVERTERS

Resolutions of between 10 and 14 bits are available as well as the DSC1710 which is a one card, 1 channel, two speed DSC system containing its own 20VA power amplifiers.

## TWO SPEED PROCESSORS

The TSL1612 combines the digital outputs of the two Synchro to Digital converters in a two speed system in order to produce a single digital word representing the input angle. It is available for any ratio between 2:1 and 36:1.

### FEATURES

- High Dynamic Performance (13,000°/sec)
- Tracking Conversion Loop (Noise Immunity)
- Internal Micro Transformers (50Hz or 400Hz)
- 12 Bit Resolution  $\pm 11$  Arc Minutes Accuracy
- $\pm 10V$  Output at 5mA
- Low Output Ripple ( $< 5mV$  p-p)
- Analog Voltage Proportional to  $d\theta/dt$



### DESCRIPTION

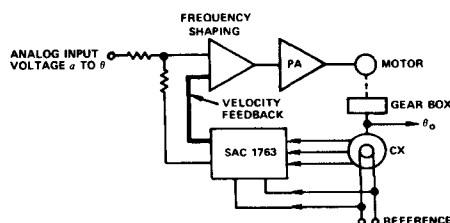
The SAC 1763 is a synchro to linear dc converter; it takes input angular information in synchro or resolver form voltages and gives an output voltage which is linearly proportional to the input angle. The output voltage of  $\pm 10V$  at  $\pm 5mA$  represents an input angular change of  $\pm 180^\circ$  of the synchro or resolver format signals applied to the converter input. An additional voltage proportional to  $d\theta/dt$  is provided for control loop applications.

Options are available for all the standard line to line voltages and frequencies for either synchro or resolver inputs. These options together with commercial or extended temperature ranges are determined by a code following the type number (see ordering information). An important feature of the SAC 1763 series converters is that no external transformer modules are required; the transformer isolation and conversion to resolver form is carried out by microtransformers which are inside the converter module *even for the 60Hz versions*.

The conversion is carried out by the use of a tracking synchro to digital converter followed by a precision DAC. The high dynamic performance of the internal tracking converter with an acceleration of  $10,000^\circ$  per second<sup>2</sup> (400Hz version) for only 5 arc minutes additional error makes the converter suitable for precision measurement and control applications.

The static overall accuracy of the SAC 1763 is  $\pm 11.0$  arc minutes with a temperature coefficient of  $< 0.2$  arc minutes per degree C.

Applications of the SAC 1763 are in measurement and control of angular movement usually but not necessarily where the total excursion of angle is  $\pm 180^\circ$  or less. In measurement the output may feed into an X-Y plotter or FM recorder, etc. The diagram shows the SAC 1763 being used inside an angular control loop where the input is a dc voltage representing the angle. The availability of the velocity voltage eliminates the need for a tachogenerator for stabilization.



Analog to Shaft Angle Using the SAC 1763

### CONNECTING PINS AND THEIR FUNCTIONS

The electrical connections to the SAC 1763 are by means of hard gold plated brass pins of length 0.2" (5.08mm) and  $0.040 \pm 0.001$  in diameter (1.016mm  $\pm 0.25$ mm). The electrical function and marking of the pins in the order in which they occur on the module are as below.

#### OUT

This pin provides the output voltage of  $\pm 10V$  representing  $\pm 180^\circ$ . The current available is  $\pm 5mA$ . The output common is the GND pin.

#### VEL

This pin provides the voltage output which is proportional to velocity. The scale of the differential velocity voltage is  $\pm 10.0V$  for  $d\theta/dt$  max of the option. The VEL pin increases in voltage, i.e., goes positive for a counter clockwise rotation of the synchro as viewed from the shaft end and reduces in voltage for a clockwise rotation. The output impedance of the pins is  $1\Omega$  and the max current which can be provided is 1mA from either pin.

#### S2, S4, S1, S3

These pins are for the synchro or resolver form input signals. Pin S4 is omitted for synchro versions. The input voltages will be either 90 or 11.8V line to line at frequencies of 60 or 400Hz according to the option. The connection data is given overleaf. The input impedance is resistive and is  $200k\Omega$  line to line for the 90V option, and  $26k\Omega$  line to line for the 11.8V options.

#### RLo, RHi

These pins are for the reference input voltages which will be at either 115V or 26V line to line at either 60 or 400Hz according to option. The input impedance is resistive and is  $200k\Omega$  line to line for the 115V option and  $45k\Omega$  line to line for the 26V option.

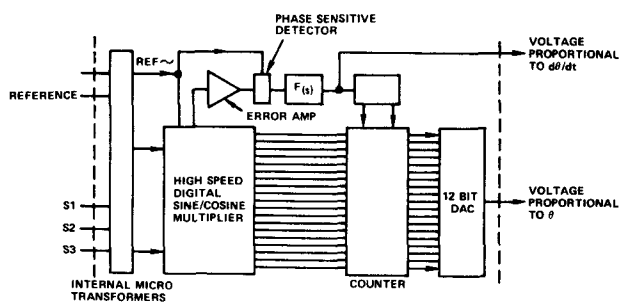
# SPECIFICATIONS (typical @ +25°C unless otherwise noted)

|   |  |
|---|--|
| Accuracy* (maximum error)   | ±11 Arc Minutes  |
| Resolution  | 1 Part in 4096   |
| Analog Output   | ±10V @ ±5mA  |
| Drift (maximum)   | 0.2 Arc Minutes per Degree C   |
| Ripple and Noise  | < 5mV p-p  |
| Signal and Reference Frequency                                      | 60Hz and 400Hz   |
| Signal Voltage  | 90V Line to Line or 11.8V Line to Line                                   |
| Signal Impedances   | 90V-200kΩ<br>11.8V-26kΩ  |
| Reference Voltages  | 115V (90V Signal)<br>26V (11.8V Signal)                                  |
| Reference Impedances  | 270kΩ High Level<br>56kΩ Low Level                                       |
| Transformer Isolation   | 500V dc  |
| Synchro Input Rates (For Full Accuracy)                             | 60Hz Version 5 Revolutions/Second<br>400Hz Version 36 Revolutions/Second |
| Acceleration (Minimum for Additional Error Less Than 6 Arc Minutes) | 60Hz Version 200°/Second/Second<br>400Hz Version 10,000°/Second/Second   |
| Velocity Voltage  | ±10V for ± Velocity Maximum of the Option                                |
| Power Supply Requirements   | +15V @ 100mA    Voltages ±5%<br>-15V @ 25mA                              |
| Power Dissipation   | 1.9W (Maximum)   |
| Operating Temperature Range   | 0 to +70°C Standard<br>-55°C to +105°C Extended                          |
| Storage Temperature   | -55°C to +125°C  |
| Dimensions  | 3.125" x 2.625" x 0.8"<br>(79.4mm x 66.7mm x 20.3mm)                     |
| Weight  | 7ozs (200 grams)   |

\*NOTE: Accuracy for:

- (a) ±10% signal and reference amplitude variation
- (b) 10% signal and reference harmonic distortion
- (c) ±5% power supply variation

Specifications subject to change without notice.



Functional Diagram of the SAC 1763, Synchro to dc Converter

## -15, GND +15V

These are the power line pins for the +15V, -15V power supplies; the voltage should be ±15V ±5%. The currents taken are 100mA on the +15V supply and 25mA on the -15V supply. The power lines must not be reversed. The GND pin is also the common pin for the output voltage.

## OPERATION

The electrical connections are straight forward; the power lines (which must not be reversed) are connected to the +15 and -15 lines with the common connection to the ground pin GND. The analog output voltage representing the digital

angle is between the pin OUT and GND. ±10V corresponding to ±180°, up to 5mA may be taken from the OUT pin. The analog voltage proportional to the rate of change of angle is provided between the pins VEL and GND. The variation is ±10.0V for the maximum velocity of the option.

Input connection is made to the pins S1, S2, S3, S4, R<sub>Hi</sub> and R<sub>Lo</sub> (S4 is not used for synchro inputs). The convention for the connections is as follows:

## Synchro Connection

$$E_{S1} - S3 = E_{RLo} - R_{Hi} \sin \omega t \sin \theta$$

$$E_{S3} - S2 = E_{RLo} - R_{Hi} \sin \omega t \sin (\theta + 120)$$

$$E_{S2} - S1 = E_{RLo} - R_{Hi} \sin \omega t \sin (\theta + 240)$$

## Resolver Connection

$$E_{S1} - S3 = E_{RLo} - R_{Hi} \sin \omega t \sin \theta$$

$$E_{S2} - S4 = E_{RHi} - R_{Lo} \sin \omega t \cos \theta$$

Since the SAC 1763 uses a tracking converter with a very fast response it will often be used inside control loops. For these applications it will be useful to know the transfer function connecting the output voltage representing angle to the input synchro angle. The transfer function for the 400Hz option is:

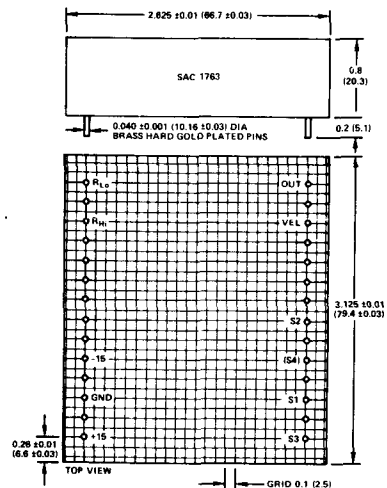
$$\frac{\bar{\theta}_0}{\bar{\theta}_1} = \frac{1655 (1 + 4.7 \times 10^{-3} S)}{1.03 \times 10^{-5} S^3 + 1.25 \times 10^{-2} S^2 + 7.78S + 1655}$$

and for the 60Hz version the transfer function is:

$$\frac{\bar{\theta}_0}{\bar{\theta}_1} = \frac{229 (1 + 3.0 \times 10^{-2} S)}{4.5 \times 10^{-4} S^3 + 8.3 \times 10^{-2} S^2 + 6.88S + 229}$$

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



## ORDERING CODE

The SAC 1763 type number is followed by a code defining the temperature range, frequency and voltage options, i.e., SAC 1763/XYZ

where X, Y and Z are replaced by numbers which define the variation. The permissible options for the SAC 1763 are:

- X = 5 signifying 0 to +70°C operation
  - X = 6 signifying -55°C to +105°C operation
  - Y = 1 signifying 400Hz operation
  - Y = 2 signifying 60Hz operation
  - Z = 1 signifies Synchro signal 11.8V, reference 26V
  - Z = 2 signifies Synchro signal 90V, reference 115V
  - Z = 8 signifies Resolver signal 11.8V, reference 26V
- For other than these options consult the factory.

### FEATURES

BCD (Binary Coded Decimal) Output Representing 0 to 359.9°  
or 0 to  $\pm 179.9^\circ$

-15V Power Supply Requirement Optional

High Tracking Rate (75 revs/sec)

Internal Microtransformers for 60Hz, 400Hz and 2.6kHz

#### Options

Voltage Scaling with External Resistors (Unique Feature)

Transformer Isolated Outputs

Low Cost

MIL Spec/Hi Rel Options Available

### APPLICATIONS

Visual Display of Angular Information

Valve Position Indication

Antenna Monitoring

Industrial Controls

### GENERAL DESCRIPTION

The SBCD1752, SBCD1753, SBCD1756 and the SBCD1757 are modular, continuous tracking Synchro/Resolver to Digital converters which employ a type 2 servo loop.

They are intended for use in both Industrial and Military applications either for displaying angular data directly, or for inputting BCD information directly into a data processing system.

The input signals can be either 3 wire synchro plus reference or 4 wire resolver plus reference, depending on the option. The outputs will be presented in parallel Binary Coded Decimal (BCD).

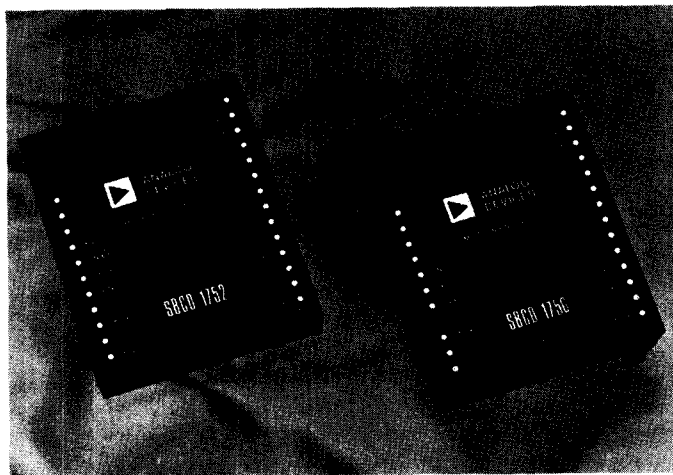
Particular attention has been paid in the design, to achieving the highest tracking rates and accelerations possible, compatible with the resolution and carrier frequency used, while at the same time obtaining a high overall accuracy.

One of the outstanding features of these converters is the use made of precision Scott T and reference microtransformers. *This has made it possible to include the transformers within the module, even for the 60Hz version as well as providing facilities for external voltage scaling.*

### MODELS AVAILABLE

The four Synchro to Digital converters described in this data sheet, differ primarily in the areas of output format and power supply requirements.

Model SBCD1752XYZ is a 13 bit plus sign, BCD output converter, giving  $-180.0^\circ$  to  $-0.1^\circ$  and  $+0.0$  to  $+179.9^\circ$  requiring  $\pm 15V$  and  $+5V$  power supplies, and having an overall accuracy of  $\pm 0.2$  Degrees.



Model SBCD1753XYZ is a 14 bit, BCD output converter, giving 0 to 359.9°, requiring  $\pm 15V$  and  $+5V$  power supplies, and having an overall accuracy of  $\pm 0.2$  Degrees.

Model SBCD1756XYZ is a 13 bit plus sign, BCD output converter, giving  $-180.0^\circ$  to  $-0.1^\circ$  and  $+0.0$  to  $+179.9^\circ$  requiring  $+15V$  and  $+5V$  power supplies, and having an overall accuracy of  $\pm 0.2$  Degrees.

Model SBCD1757XYZ is a 14 bit, BCD output converter, giving 0 to 359.9°, requiring  $+15V$  and  $+5V$  power supplies, and having an overall accuracy of  $\pm 0.2$  Degrees.

The XYZ code defines the option thus:

X signifies the operating temperature range.

Y signifies the reference frequency.

Z signifies the input voltage and range and whether it will accept Synchro or Resolver information.

More information about the option code is given under the heading "Ordering Information".

### DATA TRANSFER (ALL MODELS)

The readiness of the converters for data transfer is indicated by the state of the BUSY pin. The voltage appearing on the BUSY pin consists of a train of pulses, at TTL levels, of length according to the option (see Specifications table). The converter is busy when the BUSY pin is at TTL "High" level. The pulses occur for increasing and decreasing counts.

The most suitable time for transferring data is 400ns after the trailing edge of the BUSY pulse, and the times allowable for data transfer are shown in the specification. Even at the maximum speed of the option, these times will be sufficient to transfer data before the next BUSY pulse occurs.

(continued on page 273S)

# SPECIFICATIONS (typical at 25°C unless otherwise stated)

| MODELS   | SBCD1752   | SBCD1753                                | SBCD1756             | SBCD1757 |
|--|--|---|----------------------|----------|
| ACCURACY <sup>1</sup> (max Error)  |  |   |                      |          |
| All Frequency Options  | ±0.2 Degrees   | *                                       | *                    | *        |
| OUTPUT   | Parallel BCD, 8TTL Loads   | *                                       | *                    | *        |
| RESOLUTION   | 13 Bit + Sign Representing<br>-180.0° to -0.1° and<br>+0.0° to +179.9° | 14 bit repre-<br>senting 0 to<br>359.9° | *                    | **       |
| SIGNAL AND REFERENCE<br>FREQUENCY  | 60Hz, 400Hz and 2.6kHz   | *                                       | *                    | *        |
| SIGNAL VOLTAGE (Line to Line)  |  |   |                      |          |
| Low Level  | 11.8V rms  | *                                       | *                    | *        |
| High Level   | 90.0V rms  | *                                       | *                    | *        |
| SIGNAL IMPEDANCES  |  |   |                      |          |
| Low Level  | 26kΩ (Resistive)   | *                                       | *                    | *        |
| High Level   | 200kΩ (Resistive)  | *                                       | *                    | *        |
| REFERENCE VOLTAGE  |  |   |                      |          |
| Low Level  | 26V (11.8V Signal)   | *                                       | *                    | *        |
| High Level   | 115V (90V Signal)  | *                                       | *                    | *        |
| REFERENCE IMPEDANCE  |  |   |                      |          |
| Low Level  | 56kΩ (Resistive)   | *                                       | *                    | *        |
| High Level   | 270kΩ (Resistive)  | *                                       | *                    | *        |
| TRANSFORMER<br>ISOLATION   | 500V dc  | *                                       | *                    | *        |
| TRACKING RATE (min)  |  |   |                      |          |
| 60Hz   | 5 Revolutions Per Second   | *                                       | *                    | *        |
| 400Hz  | 36 Revolutions Per Second  | *                                       | *                    | *        |
| 2.6kHz   | 75 Revolutions Per Second  | *                                       | *                    | *        |
| Accel. <sup>1</sup> Constant K <sub>a</sub>  |  |   |                      |          |
| 60Hz   | 2000/sec <sup>2</sup>  | *                                       | *                    | *        |
| 400Hz  | 120,000/sec <sup>2</sup>   | *                                       | *                    | *        |
| 2.6kHz   | 600,000/sec <sup>2</sup>   | *                                       | *                    | *        |
| STEP RESPONSE (179° Step)<br>(For 0.1° Error)  |  |   |                      |          |
| 60Hz   | 1.5sec   | *                                       | *                    | *        |
| 400Hz  | 125ms  | *                                       | *                    | *        |
| 2.6kHz   | 50ms   | *                                       | *                    | *        |
| POWER LINES  | +15V @ 25mA  | *                                       | +15V @ 80mA          | ***      |
|  | -15V @ 25mA  | *                                       | +5V @ 500mA          | ***      |
|  | +5V @ 500mA  | *                                       |                      |          |
| POWER DISSIPATION  | 3.25 Watts   | *                                       | 3.7 Watts            | ***      |
| BUSY LOGIC OUTPUT, POSITIVE PULSE (1 TTL Load)   |  |   |                      |          |
| 60Hz   | 3.5 to 4.5μs   | *                                       | *                    | *        |
| 400Hz  | 0.5 to 1.25μs  | *                                       | *                    | *        |
| 2.6kHz   | 0.5 to 1.25μs  | *                                       | *                    | *        |
| MAX DATA TRANSFER<br>TIME (From 400ns After<br>Trailing Edge of BUSY<br>at max Velocity) |  |   |                      |          |
| 60Hz   | 40μs   | *                                       | *                    | *        |
| 400Hz  | 5.0μs  | *                                       | *                    | *        |
| 2.6kHz   | 1.8μs  | *                                       | *                    | *        |
| INHIBIT INPUT (To Inhibit)   | Logic "0" 1TTL Load  | *                                       | *                    | *        |
| TEMPERATURE RANGE  |  |   |                      |          |
| Operating  | 0 to +70°C Standard  | *                                       | *                    | *        |
|  | -55°C to +105°C Extended   | *                                       | *                    | *        |
| Storage  | -55°C to +125°C  | *                                       | *                    | *        |
| DIMENSIONS   | 3.125" x 2.625" x 0.8"<br>(79.4 x 66.7 x 20.4mm)                       | *                                       | *                    | *        |
| WEIGHT   | 6.4 ozs. (180 grams)   | *                                       | 6.5 ozs. (185 grams) | ***      |

<sup>1</sup> Specified over the appropriate operating temperature range and for

(a) ±10% signal and reference amplitude variation

(b) 10% signal and reference harmonic distortion

(c) ±5% power supply variation

(d) ±10% variation in reference frequency.

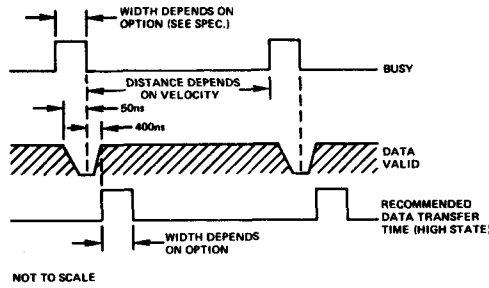
\* Specifications same as SBCD1752

\*\* Specifications same as SBCD1753

\*\*\* Specifications same as SBCD1756

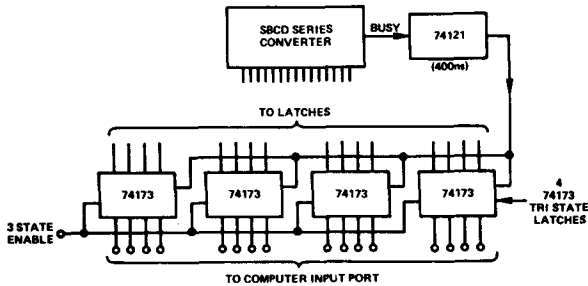
Specifications subject to change without notice.

(continued from page 271S)



**Data Transfer Diagram**

The function of the **INHIBIT** pin is to enable the user to inhibit the update of the converter's output counter. This is achieved by taking the **INHIBIT** pin to a TTL Logic zero. If used, the **INHIBIT** should be applied 400ns after the trailing edge of the **BUSY** pulse. This will ensure that the data on the output pins is valid. The data should then be transferred and the **INHIBIT** released before the next **BUSY** pulse occurs. The worst case times allowable for data transfer in this case are shown in the Specifications under the heading of "MAX DATA TRANSFER TIME (from 400ns After Trailing Edge of **BUSY** at Max Velocity)". It should be noted that the application of the **INHIBIT** will not prevent the **BUSY** pulses appearing on the **BUSY** pin, and thus if the **INHIBIT** is not released by the time that the next **BUSY** pulse occurs, the **BUSY** pulse will still appear, although the internal converter loop will have been opened. Under this condition, a worst case recovery time, equivalent to that of a step of 179 degrees may be encountered (see Spec.). To avoid this and to ensure valid data transfer, the system shown in the diagram is recommended.



**Suggested External Interface Circuitry**

In cases where the converter is connected to a data bus or used as a peripheral, the method outlined in the above diagram is recommended. The **INHIBIT** is not necessary in this case, and the external "Enable" has control of the converter output.

The AC1755 mounting card described later in this data sheet contains the external components shown in the diagram.

### CONNECTING THE CONVERTER

The power lines, which should not be reversed, should be connected to "+15V", "-15V" and "+5V" in the case of the SBCD1752 and SBCD1753, and to "+15V" and "+5V" in the case of the SBCD1756 and SBCD1757, with the common connection to "GND" in all cases.

It is suggested that 0.1μF and 6.8μF capacitors be placed in parallel from +15V to GND, from -15V to GND and from +5V to GND.

The digital output connections in the case of the SBCD1753 and SBCD1757 should be taken from the pins marked "0.1" through to "200"; these values being represented in degrees.

In the case of the SBCD1752 and SBCD1756, the data should be taken from the pins marked "0.1" through to "100", these values also being represented in degrees. In the case of these latter units the "SIGN" pin will indicate the polarity of the output, Logic "0" representing positive angles and Logic "1" representing negative angles.

In the case of a synchro, the signals are connected to S<sub>1</sub>, S<sub>2</sub> and S<sub>3</sub> according to the following convention:

### Synchro connection

$$E_{S1 - S3} = E_{RLO} - R_{HI} \sin \omega t \sin \theta$$

$$E_{S3 - S2} = E_{RLO} - R_{HI} \sin \omega t \sin (\theta + 120^\circ)$$

$$E_{S2 - S1} = E_{RLO} - R_{HI} \sin \omega t \sin (\theta + 240^\circ)$$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

### Resolver Connection

$$E_{S1 - S3} = E_{RLO} - R_{HI} \sin \omega t \sin \theta$$

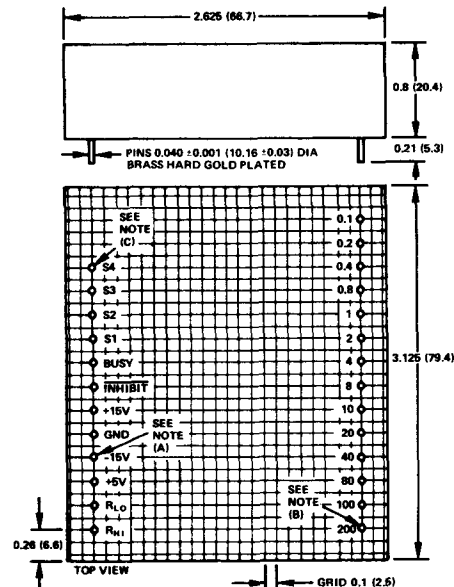
$$E_{S2 - S4} = E_{RHI} - R_{LO} \sin \omega t \cos \theta$$

The **BUSY** and **INHIBIT** pin (is used), should be connected as described under the heading "DATA TRANSFER".

The reference connections are made to pins R<sub>HI</sub> and R<sub>LO</sub>.

### PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).



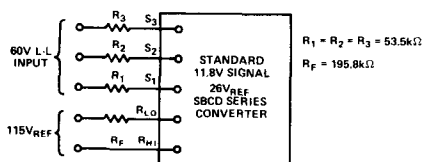
- NOTES
- (A) NOT PRESENT ON SBCD1756 AND SBCD1757
- (B) ON SBCD1752 AND SBCD1756 MARKED AS SIGN
- (C) PRESENT ON RESOLVER TO DIGITAL CONVERTER (RBCD) ONLY.

### RESISTIVE SCALING OF INPUTS

A unique feature of the SBCD1752/1753/1756/1757 converters is that the inputs can be resistively scaled to accommodate any value of input signal and reference voltage.

In order to calculate the values of the external scaling resistors necessary, add 1.1kΩ in series with the input per extra volt in the case of the signal, and 2.2kΩ per extra volt in the case of the reference.

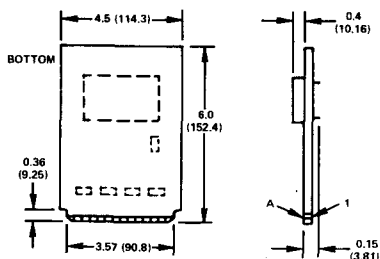
For example, assume that it is required to use a standard 11.8V line to line signal, 26V reference converter with 60V line to line signal and a 115V reference. The resistors should be arranged as in the diagram.



**Note:** In the case of  $R_1$ ,  $R_2$ , and  $R_3$ , the ratio error between the resistances is more critical than the absolute value. In general a 1% ratio error will give rise to an extra inaccuracy of 0.28 Degrees, while a ratio accuracy of 0.1% will give rise to an extra inaccuracy of 0.028 Degrees. The absolute value of  $R_F$  is not critical.

### CARD MOUNTING

All the converters can be mounted on an AC1755 mounting card. This card contains the latches and monostable, described under the "DATA TRANSFER" heading, which are necessary to transfer the data on to a computer bus system, as well as sockets for the converter. The latches have a tri-state output to facilitate ease of use. The AC1755 also contains facilities for the inclusion of input signal scaling and reference resistors as described under the heading "RESISTIVE SCALING OF INPUTS". The card uses a 22/22 0.156" pitch edge connector. The pin-out is shown below. If it is not required to use the external latches, they can be jumpered on the board.



**AC1755 Mounting Card (First Angle Projection).**  
Dimensions Shown in Inches and (mm).

| Edge Pin Number | Function       | Edge-Pin Letter | Function         |
|-----------------|----------------|-----------------|------------------|
| 1               | R (Lo)         | A               | Tri-State Enable |
| 2               | R (Hi)         | F               | +15 Volts        |
| 3               | S <sub>3</sub> | H               | +15 Volts        |
| 4               | S <sub>2</sub> | J               | -15 Volts (3)    |
| 5               | S <sub>1</sub> | K               | -15 Volts (3)    |
| 6               | S <sub>4</sub> | L               | GND              |
|                 |                | M               | GND              |
| 13              | BUSY           | N               | +5 Volts         |
| 15              | INHIBIT        | P               | +5 Volts         |
| 16              | 0.1            | T               | 8                |
| 17              | 0.2            | U               | 10               |
| 18              | 0.4            | V               | 20               |
| 19              | 0.8            | W               | 40               |
| 20              | 1              | X               | 80               |
| 21              | 2              | Y               | 100              |
| 22              | 4              | Z               | 200 (1) SIGN (2) |

### NOTES

- (1) SBCD1753 and SBCD1757 only
- (2) SBCD1752 and SBCD1756 only
- (3) SBCD1752 and SBCD1753 only

### AC1755 Mounting Card Edge Connections

### ORDERING INFORMATION

Converters should be ordered by the appropriate part number (i.e., SBCD1752, SBCD1753, SBCD1756 or SBCD1757) followed by the appropriate option code.

If the unit is to be a Resolver to Digital converter, the SBCD should be replaced by RBCD in the part number.

The XYZ options are as follows:

X signifies the operating temperature range thus;  
 $X = 5$  0 to +70°C (Commercial Temp.)  
 $X = 6$  -55°C to +105°C (Extended Temp.)

Y signifies the reference frequency thus;  
 $Y = 1$  signifies 400Hz  
 $Y = 2$  signifies 60Hz\*  
 $Y = 4$  signifies 2.6kHz

Z signifies the input signal and reference voltages and whether the converter is a Synchro to Digital or a Resolver to Digital converter. The options for Z are:

$Z = 1$  signifies Synchro, signal 11.8 Volts  
reference 26 Volts  
 $Z = 2$  signifies Synchro, signal 90 Volts  
reference 115 Volts  
 $Z = 8$  signifies Resolver, signal 11.8 Volts  
reference 26 Volts

Thus an SBCD1753 with a commercial (0 to +70°C) operating range, using a 400Hz, 26 volt reference with an 11.8 volt signal would be ordered as an SBCD1753511.

\*For 50Hz operation, a 60Hz converter can be used with no reduction in accuracy.

In addition a 400Hz unit will work with a 2.6kHz reference and a 60Hz unit will work with a 400Hz reference; however they will have the velocity and acceleration characteristics of the lower frequency rated unit.

### OTHER PRODUCTS

The SBCD series of Synchro to Digital converters are just a few of the modules and instruments concerned with Synchro conversion manufactured by us. Some of our other products are listed below and technical data is available. If you have any questions about our products or require advice about the use of them for a particular application, please contact our Applications Engineering Department.

### SYNCHRO TO DIGITAL CONVERTERS

The SDC1700 is a low profile (0.4") converter with a 12 bit natural binary output. Its overall accuracy is  $\pm 8.5$  arc-minutes, and the module contains internal transformers for all reference frequency options including 60Hz. The SDC1702 is similar to the SDC1700 but has a 10 bit natural binary output and an overall accuracy of  $\pm 22$  arc-minutes.

The SDC1704 is similar to the above two converters, but has a 14 bit natural binary output and an overall accuracy of  $\pm 2.0$  arc-minutes  $\pm 1$  LSB.

### TWO SPEED PROCESSORS

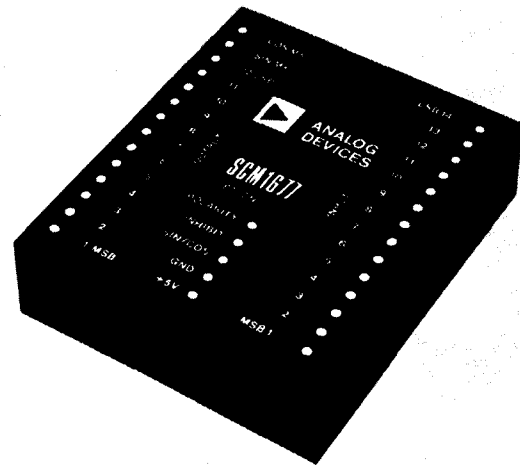
The TSL1612 and the TSL1729 both produce one digital output word up to 20 bits in length from the outputs of 2 Synchro to Digital converters in a coarse/fine system. The TSL1612 is used for ratios of 9:1, 18:1 and 36:1, while the TSL1729 is programmable for all ratios from 1:1 to 63:1.

### DIGITAL TO SYNCHRO CONVERTERS

Resolutions of between 10 and 16 bits are available as well as the DSC1710, a one card, 2 channel, 40VA, DSC system including power amps for use with 2 speed coarse/fine ratios of 9:1, 18:1, 36:1.

### FEATURES

- 14 Bit Angular Resolution
- 12 Bit Ordinate Resolution
- Programmable Sine or Cosine Sequencing
- Internal Sequence Oscillator
- TTL Compatible



### DESCRIPTION

The SCM 1677 takes as its input a natural binary digital angle 0 to 360° with resolution up to 14 bits (for low resolution operation unused inputs are connected to Logic "0").

The digital output represents either the sine or cosine of the input digital angle. The magnitude of the output is determined by 12 bits natural binary and the sign of the output is determined by the logic level of the "polarity" output pin. Logic "0" corresponds to a positive output and Logic "1" corresponds to a negative output.

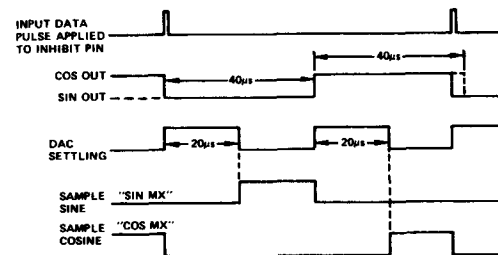
The SCM can be operated in 4 modes; they are:—

- 1) Using the internal oscillator which works at 12.5kHz the output will provide alternatively the sine and cosine of the input angle. This mode of operation is obtained with the "inhibit" pin at Logic "0" and the "sin/cos" pin at Logic "0".
- 2) To provide outputs which are always equal to the sine of the input angle. This mode is obtained by connecting the "inhibit" pin to Logic "1" and the "sin/cos" pin to Logic "0".
- 3) To provide outputs which are always equal to the cosine of the input angle. This mode is obtained by connecting the "inhibit" pin to Logic "1" and the "sin/cos" pin to Logic "1".
- 4) Fast switching between sine and cosine outputs under external control. This mode is obtained by connecting the "inhibit" pin to Logic "1" and switching the "sin/cos" pin between "1" and "0", "1" giving cosine, the "0" giving sine. It takes up to a maximum of 2μs for the output to be valid after the change on the "sin/cos" pin.

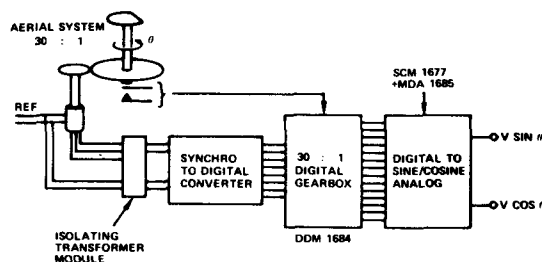
To facilitate the synchronization of the multiplex mode of operation [mode (1)] additional outputs have been provided on pins marked "Sin MX" and "Cos MX".

In this mode of operation the output is changing from giving the sine of the input to giving the cosine of the input at 12.5kHz i.e., it gives the sine for 40μs and the cosine for 40μs. 20μs after the change from sine to cosine the waveform on the pin "Sin MX" changes from a Logic "0" to Logic "1" for 20μs then returns to "0". Also 20μs after the change from cosine to sine the "Cos MX" pin changes from a Logic "0" to Logic "1" for 20μs then returns to "0".

The object of providing these delayed waveforms is to allow for any settling that is necessary in the multiplexed DAC which is connected to the output.



"COS MX" and "SIN MX" Outputs



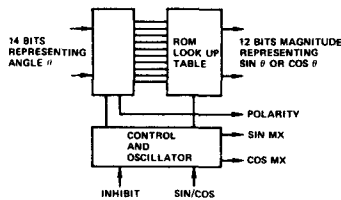
The Application of the SCM 1677 in Producing Invariant Sine/Cosine Voltages



# SPECIFICATIONS (typical @ +15V unless otherwise noted)

|                             |  |
|-----------------------------|--|
| Input Form                  | Angle in Natural Binary  |
| Input Angular Resolution    | 14 Bits for 360°   |
| Input Levels                | TTL Positive Logic   |
| Input Loading               | 2TTL Loads   |
| Outputs                     | Multiplexed Digital Sine and Cosine of the Input Angle in Natural Binary Form  |
| Multiplexing Rate           | Alternating Sine and Cosine at 12.5kHz But Can Be Overridden to Produce Static Sine or Cosine, Or High Speed Switching Between Sine and Cosine Under External Command. |
| Output Resolution           | 13 Bits Sign-Magnitude   |
| Rounding Error              | ±0.024% of Peak  |
| Output Levels               | TTL Positive Logic   |
| Output Loading              | CMOS Loads   |
| Size                        | 3.125" x 2.62" x 0.8" (79.4mm x 66.6mm x 20.3mm)   |
| Power Supply                | +5V @ 600mA  |
| Operating Temperature Range | 0 to +70°C or -55°C to +105°C  |
| Storage                     | -55°C to +125°C  |

Specifications subject to change without notice.



SCM 1677 Functional Diagram

## SYNCHRONIZING THE SCM 1677 TO AN EXTERNAL CLOCK

If the input angle to the SCM is being updated by an asynchronous clock the internal oscillator can still be used to give the alternation between sine and cosine. For this method of operation the external clock pulse (250ns or more positive pulse) must not be repetitive with a period shorter than 80μs. Application of the external clock pulse to the "inhibit" pin will switch the SCM into sine output state after which it will sequence sine and cosine every 40μs until the next clock pulse which will again put the SCM 1677 into its sine state and start the period of operation from this time. If the SCM 1677 is already in its sine state at the time of the occurrence of the subsequent clock pulse the output will stay at sine with the cycle of operation again restarted from the time of application of the pulse.

If the clock pulses are spaced by < 80μs the cosine period will be shortened. If pulses are closer than 40μs, only the sine output will be given (see timing diagram).

## ELECTRICAL CONNECTING PINS AND THEIR FUNCTION

Electrical connection to the SCM 1677 is made by means of 0.040 ±0.001" dia. brass hard gold plated pins of length 0.20" (1.02 ±0.025mm dia. 5mm in length). The module is usually plugged into sockets in the printed circuit board. For environmental conditions of high vibration the pins may be soldered directly to the printed circuit board. The pin designations and their function in the order of their occurrence is given below.

### COS MX

This pin is an output pin; in the absence of an inhibit voltage the waveform on this pin will be 20μs long pulse every cycle of operation i.e., every 80μs. The leading edge of the 20μs pulse occurs 20μs after the output has been providing the cosine of the input angle. The usual function of this waveform is for the leading (positive going) edge to be used to act as convert command in the DAC system following the SCM 1677; it gives 20μs for the sample and holds, etc. to settle.

### SIN MX

This pin is an output pin; in the absence of an inhibit voltage the waveform on this pin will be a 20μs long pulse every cycle of operation i.e., every 80μs. The leading edge of the 20μs pulse occurs 20μs after the output has been providing the sine of the input angle. Its purpose is as for Cos MX.

### DIGITAL OUTPUT PINS

These are the pins 12, 11 . . . . . 1; they provide a binary digital representation of the modulus of the output. Pin 12 is the least significant digit and pin 1 the most significant digit. The outputs are designed for driving into CMOS loads. Logic "1" is 5 volts and Logic "0" is 0 volts. The output current "1" state is 0.3mA. No damage will occur if the pins are accidentally connected to either ground (0 volts) or +5 volts.

### POLARITY

The pin marked "polarity" provides the output sign information. The levels are 0 and +5 volts. The output is positive when the "polarity" is at Logic "0" and negative when the polarity is at Logic "1". The output is designed for driving CMOS loads. 0.3mA is available.

### INHIBIT

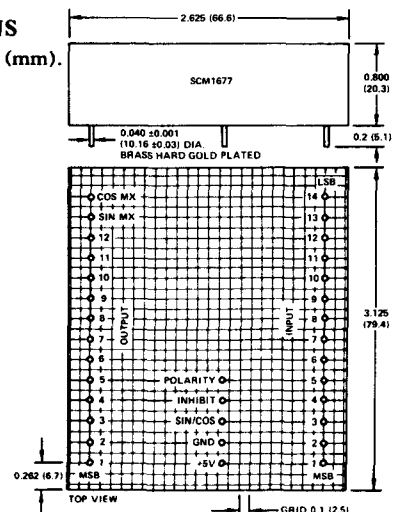
This pin facilitates the inhibiting of the internal oscillator. It is an input pin. The pin represents two TTL loads and is operated by voltages at TTL levels. A Logic "1" on this pin stops the internal oscillator and puts the converter into its sine conversion state for as long as the Logic "1" state is held (or longer if a pulse is applied). If a short positive pulse, 250ns or longer is applied to the inhibit pin two things are caused to happen. First, if the SCM 1677 is in its cosine state it will immediately change to give out sine (2μs ripple through delay); if the converter is giving sine it will continue to do so. Second, in either of the above contingencies the phasing of the sequence of waveforms in the timing diagram will be restarted from the time of application of the pulse, i.e., it will have a sine output for 40μs and then switch to giving out cosine for 40μs repeating this alternation until the receipt of a further pulse.

### SIN/COS

This pin is provided to permit external determination of the conversion to be either sine or cosine. The levels required are TTL, and the input loading is 2 TTL loads. To use this pin the Inhibit pin must be put in the Logic "1" state. Having put the Inhibit pin permanently in the Logic "1" state the output may be caused to give either the sine or cosine of the input angle by switching the "sin/cos" pin between Logic "0" and Logic "1". Logic "0" causes the sine conversion. It will take up to a maximum of 2μs for the output data to be valid after a change.

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



### SCM 1677

#### Ordering information

The only options for the SCM 1677 are in temperature range; the correct order number will therefore be:—

#### SCM 1677/X00

X = 5 for 0 to +70°C

X = 6 for -55°C to +105°C

## SDC1700/1702/1704 Series

### FEATURES

Internal Microtransformers for 60Hz, 400Hz and 2.6kHz References  
 Low Profile (0.4")  
 10, 12 or 14 Bit Resolution for 360°  
 High Tracking Rates (75 revs/sec)  
 Voltage Scaling with External Resistors (Unique Feature)  
 DC Voltage Output Proportional to Angular Velocity  
 Low Cost  
 Lightweight 3oz. (85 grams)  
 MIL Spec/Hi Rel Options Available

### APPLICATIONS

Servo Mechanisms  
 Retransmission Systems  
 Coordinate Conversion  
 Antenna Monitoring  
 Simulation  
 Industrial Controls  
 Fire Control Systems  
 Machine Tool Control Systems

### GENERAL DESCRIPTION

The SDC1700, SDC1702 and SDC1704 are modular, continuous tracking Synchro/Resolver to Digital Converters which employ a type 2 servo loop.

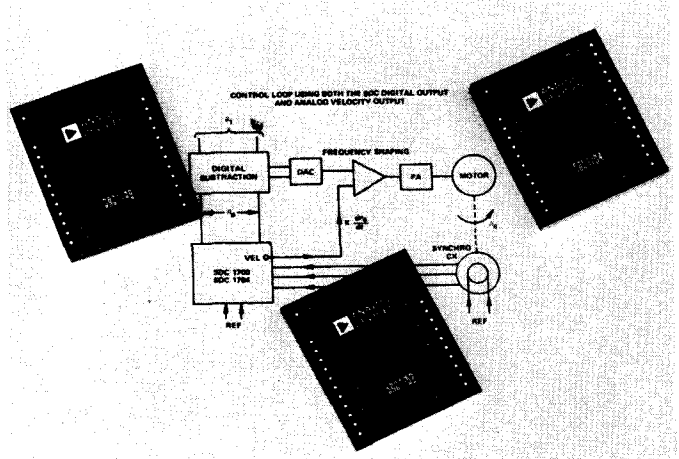
They are intended for use in both Industrial and Military applications.

The input signals can be either 3 wire synchro plus reference or 4 wire resolver plus reference, depending on the option. The outputs will be presented in TTL compatible, parallel natural binary.

One of the outstanding features of the converters is the use of precision Scott T and reference microtransformers. *This has made it possible to include the transformers within the module, even on the 60Hz option, and yet still maintain the profile height of 0.4".*

Particular attention has been paid in the design, to achieving the highest tracking rates and accelerations possible, compatible with the resolution and carrier frequency used, while at the same time obtaining a high overall accuracy.

When SDCs are used in control loops, it is often useful to have a voltage which is proportional to angular velocity. This voltage is available and has been brought out on all the SDC1700 converters.



Extended temperature range versions of all the converters are available.

### MODELS AVAILABLE

The three Synchro to Digital Converters described in this data sheet differ primarily in the areas of resolution, accuracy and dynamic performance as follows:

Model SDC1702XYZ is a 10 bit converter which has an overall accuracy of  $\pm 22$  arc-minutes and a resolution of 21 arc-minutes.

Model SDC1700XYZ is a 12 bit converter with an overall accuracy of  $\pm 8.5$  arc-minutes and a resolution of 5.3 arc-minutes.

Model SDC1704XYZ is a 14 bit converter with an overall accuracy of  $\pm 2$  arc-minutes  $\pm 1$ LSB and a resolution of 1.3 arc-minutes.

The XYZ code defines the option thus: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the input voltage and range, and whether it will accept synchro or resolver format.

More information about the option code is given under the heading of "Ordering Information".

### NOTE

For all the standard options, no external transformers are needed with these converters.

# SPECIFICATIONS (typical @ +25°C unless otherwise noted)

| MODELS   | SDC1702  | SDC1700  | SDC1704                            |
|--|--|--|------------------------------------|
| ACCURACY <sup>1</sup> (max error)  |  |  |                                    |
| 60Hz   | ±22 arc-minutes  | ±8.5 arc-minutes                                 | ±2.6 arc-minutes ±1LSB             |
| 400Hz  | ±22 arc-minutes  | ±8.5 arc-minutes                                 | ±2.0 arc-minutes ±1LSB             |
| 2.6kHz   | ±22 arc-minutes  | ±8.5 arc-minutes                                 | ±2.6 arc-minutes ±1LSB             |
| RESOLUTION   | 10 Bits (1LSB = 21 arc. mins.)   | 12 Bits (1LSB = 5.3 arc. mins.)                  | 14 Bits (1LSB = 1.3 arc. mins.)    |
| OUTPUT (In Parallel)   | 10 Bits (Natural Binary)   | 12 Bits (Natural Binary)                         | 14 Bits (Natural Binary)           |
| SIGNAL AND REFERENCE FREQUENCY   | 60Hz, 400Hz, 2.6kHz  | *  | *                                  |
| SIGNAL VOLTAGE (Line-to-Line)  |  |  |                                    |
| Low Level  | 11.8V rms  | *  | *                                  |
| High Level   | 90V rms  | *  | *                                  |
| SIGNAL IMPEDANCES  |  |  |                                    |
| Low Level  | 26kΩ (Resistive)   | *  | *                                  |
| High Level   | 200kΩ (Resistive)  | *  | *                                  |
| REFERENCE VOLTAGE  |  |  |                                    |
| Low Level  | 26V (11.8V Signal)   | *  | *                                  |
| High Level   | 115V (90V Signal)  | *  | *                                  |
| REFERENCE IMPEDANCE  | 270kΩ (115V Reference)<br>56kΩ (26V Reference)<br>(Impedance is Resistive) | *  | *                                  |
| TRANSFORMER ISOLATION  | 500V dc  | *  | *                                  |
| TRACKING RATE (min)  |  |  |                                    |
| 60Hz   | 5 Revolutions Per Second   | *  | 500°/sec                           |
| 400Hz  | 36 Revolutions Per Second  | *  | 12 Revolutions Per Second          |
| 2.6kHz   | 75 Revolutions Per Second  | *  | 25 Revolutions Per Second          |
| Accel. <sup>1</sup>  |  |  |                                    |
| Constant K <sub>a</sub>  |  |  |                                    |
| 60Hz   | 2000/sec <sup>2</sup>  | *  | 1100/sec <sup>2</sup>              |
| 400Hz  | 120,000/sec <sup>2</sup>   | *  | 80,000/sec <sup>2</sup>            |
| 2.6kHz   | 600,000/sec <sup>2</sup>   | *  | 300,000/sec <sup>2</sup>           |
| STEP RESPONSE (179° Step)<br>(For 1LSB Error)  |  |  |                                    |
| 60Hz   | 1.5sec   | *  | *                                  |
| 400Hz  | 125ms  | *  | *                                  |
| 2.6kHz   | 50ms   | *  | *                                  |
| POWER LINES  | ±15V @ 25mA } ±5%<br>+5V @ 70mA }  | *  | ±15V @ 45mA } ±5%<br>+5V @ 110mA } |
| POWER DISSIPATION  | 1.1 Watts  | *  | 1.9 Watts                          |
| DATA LOGIC OUTPUT <sup>2</sup><br>(TTL Compatible)   | 2 TTL Loads SDC17026YZ<br>4 TTL Loads SDC17025YZ                           | 2 TTL Loads SDC17006YZ<br>4 TTL Loads SDC17005YZ | 2 TTL Loads on<br>All Options      |
| BUSY LOGIC OUTPUT, POSITIVE PULSE (1 TTL Load)   |  |  |                                    |
| 60Hz   | 2.5μs to 4.5μs   | *  | 1.5μs to 3.5μs                     |
| 400Hz  | 0.5μs to 1.25μs  | *  | 0.5μs to 1.5μs                     |
| 2.6kHz   | 0.5μs to 1.25μs  | *  | 0.5μs to 1.5μs                     |
| MAX DATA TRANSFER TIME<br>(From 70ns After Trailing Edge of<br>BUSY Pulse at max Velocity) |  |  |                                    |
| 60Hz   | 40μs   | *  | 35μs                               |
| 400Hz  | 5.0μs  | *  | 3.0μs                              |
| 2.6kHz   | 1.8μs  | *  | 0.8μs                              |
| INHIBIT INPUT (To Inhibit)   | Logic "0" 1 TTL Load   | *  | Logic "0" 2 TTL Loads              |
| WARM UP TIME   | 1 sec to Rated Accuracy  | *  | *                                  |
| TEMPERATURE RANGE  |  |  |                                    |
| Operating  | 0 to +70°C Standard<br>-55°C to +105°C Extended                            | *  | *                                  |
| Storage  | -55°C to +125°C  | *  | *                                  |
| DIMENSIONS   | 3.125" x 2.625" x 0.4"<br>(79.4 x 66.7 x 10.2mm)                           | *  | *                                  |
| WEIGHT   | 3 ozs. (85 grams)  | *  | *                                  |

\*Specification same as SDC1702

<sup>1</sup>Specified over the appropriate operating temperature range of the option and for:  
(a) ±10% signal and reference amplitude variation (b) 10% signal and reference  
Harmonic Distortion (c) ±5% power supply variation (d) ±10% variation in reference  
frequency.

<sup>2</sup>It is recommended that buffers should be used if the SDC1704 digital output is  
required to drive over a distance greater than 6".

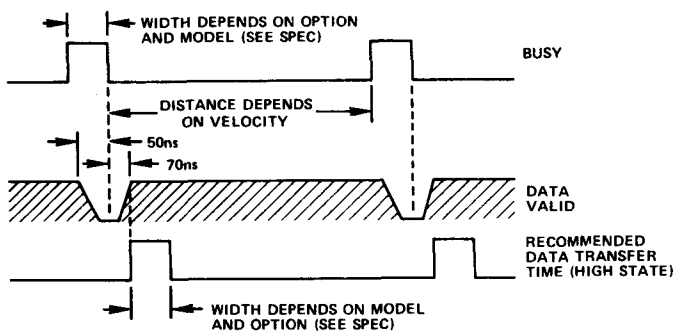
Specifications subject to change without notice.

## DATA TRANSFER (All Models)

The readiness of the converters for data transfer is indicated by the state of the BUSY pin.

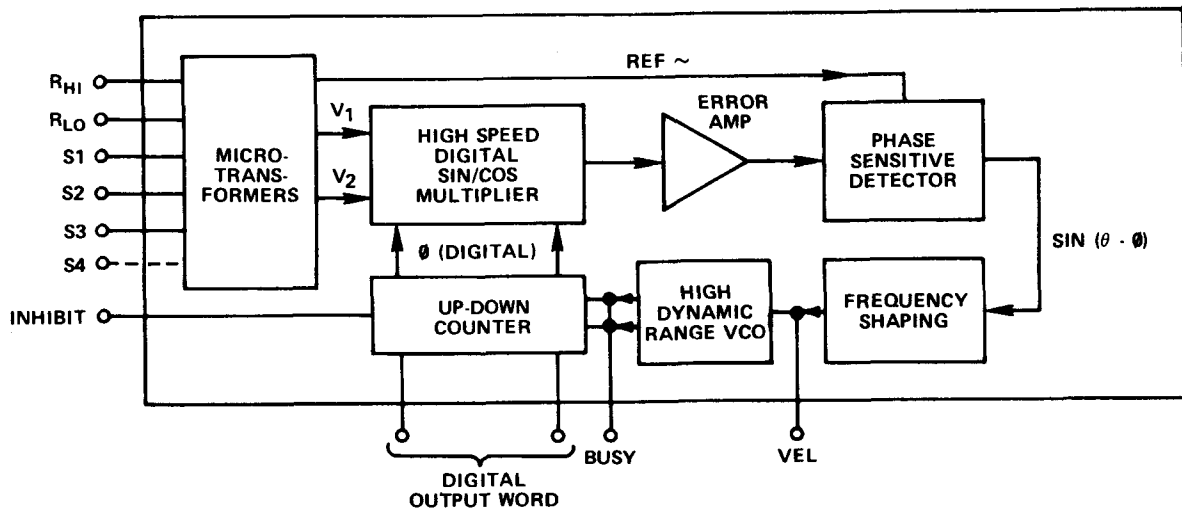
The voltage appearing on the BUSY pin consists of a train of pulses, at TTL levels, of length according to the model and option (see specification table). The converter is busy when the BUSY pin is at a TTL "High" level. These pulses correspond to those delivered by the VCO to increment or decrement the up-down counter (see schematic diagram). Thus the pulses will occur for increasing and decreasing counts.

The most suitable time for transferring data is 70ns after the trailing edge of the BUSY pulse, and the times allowable for data transfer are shown in the specification. Even at the maximum speed of the option, these times will be sufficient to transfer data before the next BUSY pulse occurs.



Data Transfer Diagram

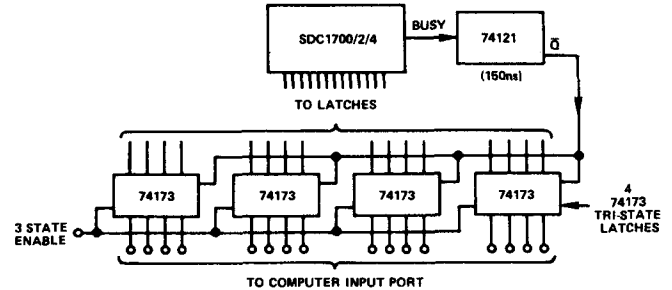
The function of the INHIBIT pin is to enable the user to inhibit the counter update. When this pin is driven to 0 Volts, the VCO pulses are prevented from updating the counter and thus the internal converter loop is opened. If used, the INHIBIT should be applied at the trailing edge of the BUSY signal, however the BUSY pulses will still occur on the BUSY pin when the INHIBIT is present. Note that if the converter loop is opened for any length of time, the converter may take an appreciable time to recover to full accuracy when the loop is restored.



Functional Diagram of the SDC1700/2/4 Converters

## INTERFACING WITH A COMPUTER

It is recommended that external latches and a monostable are used to enable data to be transferred onto a computer data bus. One method is shown in the diagram. Using this method will mean that the latches are constantly updated by the BUSY signal, while at the same time enabling inputs to be made to the computer by means of normal data transfer procedures. The AC1755 mounting card contains these external components.



Suggested External Computer Interface Circuitry

## THEORY OF OPERATION

If the unit is a Synchro to Digital Converter, then the 3 wire synchro output will be connected to S1, S2 and S3 on the module and the Scott T transformer pair will convert these signals into resolver format.

$$\text{i.e., } \begin{aligned} V_1 &= K E_0 \sin \omega t \sin \theta \\ V_2 &= K E_0 \sin \omega t \cos \theta \end{aligned}$$

Where  $\theta$  is the angle of the Synchro Shaft.

If the unit is a Resolver to Digital Converter, then the 4 wire resolver output will be connected to S1, S2, S3 and S4 on the module and the microtransformer will act purely as an isolator.

To understand the conversion process, then assume that the current word state of the up-down counter is  $\phi$ .

The  $V_1$  is multiplied by  $\cos \phi$  and  $V_2$  is multiplied by  $\sin \phi$  to give

$$\begin{aligned} &K E_0 \sin \omega t \sin \theta \cos \phi \\ \text{and } &K E_0 \sin \omega t \cos \theta \sin \phi \end{aligned}$$

These signals are subtracted by the error amplifier to give:

$$K E_O \sin \omega t (\sin \theta \cos \phi - \cos \theta \sin \phi)$$

$$\text{or } K E_O \sin \omega t \sin (\theta - \phi)$$

A phase sensitive detector, integrator and Voltage Controlled Oscillator (VCO) form a closed loop system which seeks to null  $\sin (\theta - \phi)$ .

When this is accomplished, the word state of the up-down counter ( $\phi$ ), equals within the rated accuracy of the converter, the synchro shaft angle  $\theta$ .

### CONNECTING THE CONVERTER

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, are  $\pm 15V$  and  $5V$ . They must be connected to the " $\pm 15V$ " and " $5V$ " pins with the common connection to the ground pin GND.

It is suggested that  $0.1\mu F$  and  $6.8\mu F$  capacitors be placed in parallel from  $+15V$  to GND, from  $-15V$  to GND and from  $+5V$  to GND.

The digital output is taken from pins:

- 1 through to 10 for the SDC1702
- 1 through to 12 for the SDC1700
- 1 through to 14 for the SDC1704

Pin 1 represents the MSB in each case. The reference connections are made to pins " $R_{HI}$ " and " $R_{LO}$ ".

In the case of a Synchro, the signals are connected to " $S1$ ", " $S2$ " and " $S3$ " according to the following convention:

$$E_{S1} - S3 = E_{RLO} - R_{HI} \sin \omega t \sin \theta$$

$$E_{S3} - S2 = E_{RLO} - R_{HI} \sin \omega t \sin (\theta + 120^\circ)$$

$$E_{S2} - S1 = E_{RLO} - R_{HI} \sin \omega t \sin (\theta + 240^\circ)$$

For a resolver, the signals are connected to " $S1$ ", " $S2$ ", " $S3$ " and " $S4$ " according to the following convention:

$$E_{S1} - S3 = E_{RLO} - R_{HI} \sin \omega t \sin \theta$$

$$E_{S2} - S4 = E_{RHI} - R_{LO} \sin \omega t \cos \theta$$

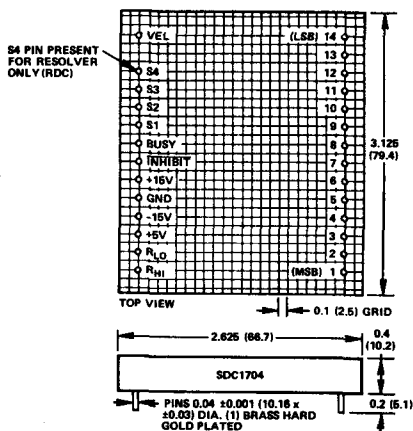
The analog voltage representing velocity is available between " $VEL$ " and " $GND$ ".

The " $BUSY$ " and " $INHIBIT$ " pin (if used), should be connected as described under the heading " $Data Transfer$ ".

NOTE: If the INHIBIT pin is used (i.e., driven to 0 volts), the control loop will be opened and a finite time will be required (see spec) for the converter to recover.

### OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions are shown in inches and (mm).



NOTE: ABOVE DIAGRAM ILLUSTRATES CONNECTIONS FOR SDC1704. FOR SDC1700, PINS 13 AND 14 ARE OMITTED. PIN 12 IS LSB. FOR SDC1702, PINS 11, 12, 13, 14 ARE OMITTED. PIN 10 IS LSB.

### RESISTIVE SCALING OF INPUTS

A unique feature of the SDC1700 series of converters is that the inputs can be resistively scaled to accommodate any range of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered. In addition it should be noted that a 400Hz unit will operate from a 2.6kHz reference. It will however have the velocity and acceleration characteristics as specified for the 400Hz converter. A 60Hz converter will operate from a 400Hz reference and will have the velocity and acceleration characteristics as specified for the 60Hz converter.

To calculate the values of the external scaling resistors, add  $1.11k\Omega$  in series with the input per extra volt in the case of the signal, and  $2.2k\Omega$  in the case of the reference.

For example, assume that we have an 11.8 volt line to line signal/26.0 volt reference converter, and we wish to use a 60 volt line to line signal with a 115 volt reference.

Thus in each signal input line, the extra voltage capability required is:

$$60 - 11.8 = 48.2 \text{ volts}$$

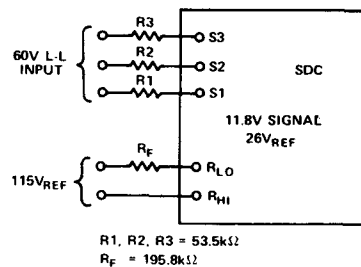
Therefore each resistor needs to have a value of  $48.2 \times 1.11 = 53.5k\Omega$ . In the case of the reference, the extra voltage capability required is:

$$115 - 26.0 = 89 \text{ volts}$$

Therefore the resistor needs to have a value of:

$$89.0 \times 2.2 = 195.8k\Omega$$

Thus the inputs can be scaled as in the diagram below.



$R1, R2, R3 = 53.5k\Omega$   
 $R_F = 195.8k\Omega$

NOTE: IN THE CASE OF  $R1, R2$  AND  $R3$ , THE RATIO ERRORS BETWEEN THE RESISTANCES IS MORE IMPORTANT THAN THE ABSOLUTE RESISTANCE VALUES.

IN GENERAL A 1% RATIO ERROR WILL GIVE RISE TO AN EXTRA INACCURACY OF 17 ARC-MINUTES WHILE A RATIO ERROR OF 0.1% WILL GIVE RISE TO AN EXTRA INACCURACY OF 1.7 ARC-MINUTES.

THE ABSOLUTE VALUE OF  $R_F$  IS NOT CRITICAL.

### BIT WEIGHT TABLE

| Bit Number           | Weight in Degrees |
|----------------------|-------------------|
| 1 (MSB)              | 180.0000          |
| 2                    | 90.0000           |
| 3                    | 45.0000           |
| 4                    | 22.5000           |
| 5                    | 11.2500           |
| 6                    | 5.6250            |
| 7                    | 2.8125            |
| 8                    | 1.4063            |
| 9                    | 0.7031            |
| 10 (LSB for SDC1702) | 0.3516            |
| 11                   | 0.1758            |
| 12 (LSB for SDC1700) | 0.0879            |
| 13                   | 0.0439            |
| 14 (LSB for SDC1704) | 0.0220            |

## VELOCITY PIN

This pin provides a voltage output which is proportional to the angular velocity of the input. The voltage goes negative for an increasing digital angle and goes positive for a decreasing digital angle.

The characteristics of the velocity pin output are given in the table below.

|  |  |
|--|--|
| Scaling of Output Voltage for One Fifth max Velocity | 2Volts (Nominal)   |
| Output Voltage Temp. Coeff.                          | 0.05%/°C of Output   |
| Output Voltage Drift (All Models)                    | 0 to +70°C<br>±50µV/°C<br>-55°C to +105°C<br>±100µV/°C   |
| Linearity:   | 0/sec to 800°/sec SDC1704<br>400Hz 1%<br>0/sec to 100°/sec SDC1704<br>60Hz 1%<br>0/sec to 800°/sec SDC1700/2<br>400Hz 2%<br>0/sec to 100°/sec SDC1700/2<br>60Hz 1.5% |
| Noise: (0 to 20Hz)                                   | @ 800°/sec SDC1700/2/4<br>400Hz 1mV rms<br>@ 100°/sec SDC1700/2/4<br>60Hz 1mV rms  |
| Impedance (Output)                                   | 1Ω   |
| max Current Available                                | 1mA  |

The velocity voltage can be used in closed loop servo systems for stabilization instead of a tachometer.

The SDC1700/2/4 velocity outputs do not have the disadvantages of being inefficient at low speeds and do not need gearing required by tachometers. In addition, the output is available at no extra cost.

For other velocity output scaling and linearity consult the factory.

Two examples of the use of the velocity pin are shown in the diagram below.

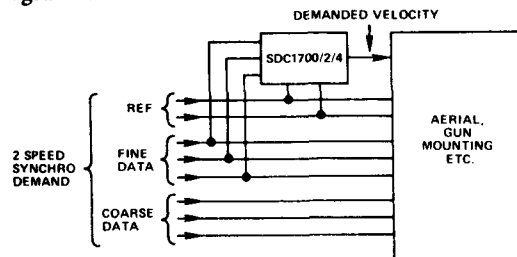


Diagram showing a velocity feed forward application. The SDC is used to produce the demanded velocity from Synchro form inputs.

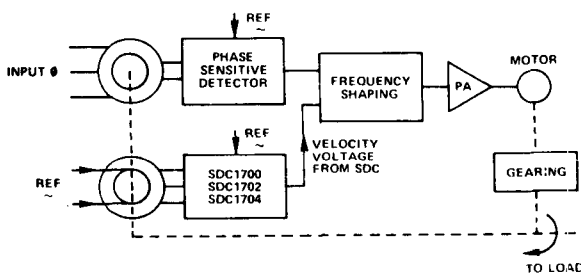
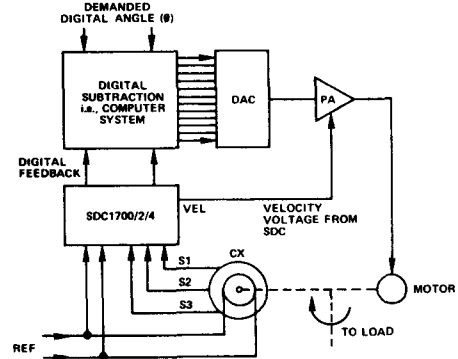


Diagram showing the velocity voltage being used to stabilize an electro-mechanical control loop

## APPLICATIONS OF SYNCHRO TO DIGITAL CONVERTERS

SDCs can be used in a variety of ways in control loops as well as for the conversion of angular data into a form which is readily acceptable to digital displays or computers.

The diagram below shows an SDC being used in a digitally controlled feedback loop.



An SDC Being Used in a Digitally Controlled Feedback Loop

Such loops as shown in the diagram above require the high dynamic performance of the SDC1700 series converters. It should be noted that in this application, the SDC1700 series will replace conventional tachometers and phase sensitive detectors while at the same time provide digital position feedback.

Many synchro systems employ a two speed, geared arrangement utilizing one synchro for the fine shaft and one for the coarse. An example of this type is shown below.

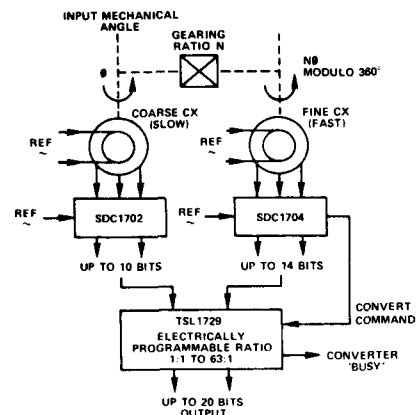


Diagram Showing Coarse/Fine Synchro Processor System

In the above example, two tracking SDC's are being used to provide data for coarse/fine (two speed) data transmission systems.

The TSL1729 is a processor which combines the outputs of two SDC's to provide one output word of up to 20 bits in length.

The TSL1729 is programmable for any ratio between 1:1 and 63:1 and provides automatic compensation for misalignment of the coarse synchro relative to its shaft. It also corrects for any overlap between the digits of the coarse and fine shafts.

## MEAN TIME BETWEEN FAILURES (M.T.B.F.)

The estimated mean time between failures is given as follows:

|           |               |
|-----------|---------------|
| SDC1700/2 | 180,000 Hours |
| SDC1704   | 160,000 Hours |

Further information relating to M.T.B.F. and to the quality control and test procedures employed by us can be obtained from the factory on request.

## TRANSFER FUNCTION

The transfer function of the SDC1700/2 and SDC1704, 400Hz versions, is given below.

For the transfer functions of the other models or for a detailed analysis of those given here, please contact us.

SDC1700/2 400Hz

$$\frac{\theta_0}{\theta_1} = \frac{160.7 \times 10^6 (1 + 4.7 \times 10^{-3} S)}{S^3 + 1214 S^2 + 755.3 \times 10^3 S + 160.7 \times 10^6}$$

SDC1704 400Hz

$$\frac{\theta_0}{\theta_1} = \frac{2.546 \times 10^6 (1 + 20 \times 10^{-3} S)}{S^3 + 275 S^2 + 50.94 \times 10^3 S + 2.546 \times 10^6}$$

## CARD MOUNTING

All the converters can be mounted on an AC1755 mounting card. This card contains the latches and the monostable, described under the "Data Transfer" heading, which are necessary to transfer the data on to a computer bus system, and sockets for the converter.

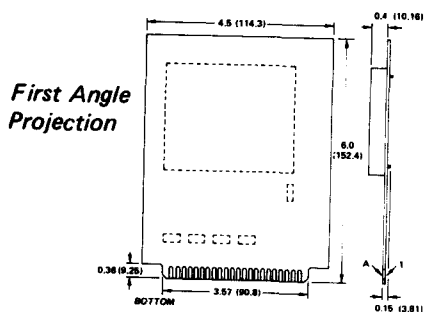
The latches have a tri-state output to facilitate ease of use.

The AC1755 also contains facilities for the inclusion of input signal and reference scaling resistors as described under the heading "Resistive Scaling of Inputs".

The card uses a 22/22 0.156" pitch edge connector. The pin out is shown below. If it is not required to use the external latches and monostable, they can be jumpered on the board.

### AC1755 MOUNTING CARD

Dimensions shown in inches and (mm).



### EDGE CONNECTIONS AC1755

| Edge Pin Number | Function | Edge Pin Letter | Function         |
|-----------------|----------|-----------------|------------------|
| 1               | R (Lo)   | A               | Tri-State Enable |
| 2               | R (Hi)   | F               | +15V             |
| 3               | S3       | H               | +15V             |
| 4               | S2       | J               | -15V             |
| 5               | S1       | K               | -15V             |
| 6               | S4       | L               | GND              |
| 8               | VEL      | M               | GND              |
| 13              | BUSY     | N               | +5V              |
| 15              | INHIBIT  | P               | +5V              |
| 16              | BIT 14   | T               | BIT 7            |
| 17              | BIT 13   | U               | BIT 6            |
| 18              | BIT 12   | V               | BIT 5            |
| 19              | BIT 11   | W               | BIT 4            |
| 20              | BIT 10   | X               | BIT 3            |
| 21              | BIT 9    | Y               | BIT 2            |
| 22              | BIT 8    | Z               | BIT 1            |

NOTE: SDC1702 does not use pins 16, 17, 18 or 19. SDC1700 does not use pins 16 and 17.

## ORDERING INFORMATION

Parts should be ordered by the appropriate part number (i.e., SDC1700, SDC1702, SDC1704) followed by the appropriate XYZ option code.

If the unit is to be a Resolver to Digital Converter, the SDC should be replaced by RDC in the part number.

The XYZ options are as follows:

X signifies the operating temperature range and the options are:

X = 5 signifies 0 to +70°C (commercial) temperature.

X = 6 signifies -55°C to +105°C (extended) temperature.

Y signifies the reference frequency and the options are:

Y = 1 signifies 400Hz

Y = 2 signifies 60Hz\*

Y = 4 signifies 2.6kHz

Z signifies the input signal and reference voltages and whether the converter is an SDC or an RDC. The options are:

Z = 1 signifies Synchro, signal 11.8V, reference 26V.

Z = 2 signifies Synchro, signal 90.0V, reference 115V.

Z = 8 signifies Resolver, signal 11.8V, reference 26V.

Thus, for example, an SDC1704 with a commercial (0 to +70°C) operating range, using a 400Hz, 26V reference with an 11.8V signal would be ordered as an SDC1704511.

For other than these options, consult the factory.

## CAUTIONS

Do not reverse the power supplies.

Do not connect signal and/or reference inputs to other than S1, S2, S3, S4, R<sub>HI</sub> or R<sub>LO</sub>.

Do not connect signals and/or references to a lower voltage rated converter. (Such as a 115V Synchro into a 26V Converter).

Misconnections as per the above will damage the units and void the warranty.

## OTHER PRODUCTS

The SDC1700/2/4 converters are just a few of the modules and instruments concerned with Synchro conversion products manufactured by us.

Other products are listed below and technical data is available. If you have any questions about our products or require advice about the use of them for a particular application, please contact our Applications Engineering Department.

## TWO SPEED PROCESSORS

Which utilize the digital outputs of two SDCs in a 2 speed coarse/fine system to produce one combined digital word of up to 20 bits in length. The TSL1729 in particular can be used with any ratio between 1:1 and 63:1.

## DIGITAL TO SYNCHRO CONVERTERS

Resolutions of between 10 and 16 bits available as well as the DSC1710, a one card, 2 channel 40VA DSC system including power amps for use with 2 speed coarse/fine ratios of 9:1, 18:1 and 36:1.

## BCD OUTPUT SYNCHRO TO DIGITAL CONVERTERS

The SBCD1752 and SBCD1753 are converters with a BCD instead of a binary output based upon the SDC1700. They have outputs of ±180.0 degrees and 0 to 360.0 degrees respectively.

### \*50Hz Operation

For 50Hz operation, a 60Hz converter can be used with no reduction in accuracy.



# Ultra-Low Profile (0.35") Three-State Latched Output Synchro to Digital Converters

## SDC1725/1726

### FEATURES

- Three-State Latched Output
- Continuous Tracking Even During Data Transfer
- Simple Data Transfer Facility
- Low Profile 0.35" (8.9mm)
- Internal Transformers for 60Hz, 400Hz and 2.6kHz References
- Signal and Reference Voltage Scaling with External Resistors
- High Tracking Rates (50 revs/sec)
- Lightweight 3.3 oz. (93 gms)
- MIL Spec/Hi Rel Options Available

### APPLICATIONS

- Servo Mechanisms
- Retransmission Systems
- Coordinate Conversion
- Antenna Monitoring
- Simulators
- Industrial Controls
- Artillery Fire Control Systems
- Machine Tool Control Systems

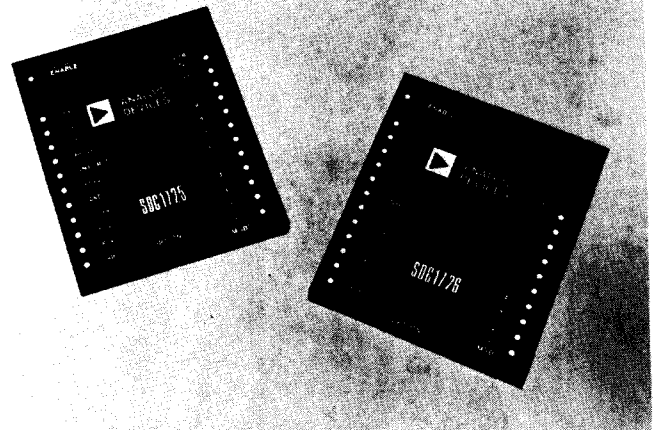
### GENERAL DESCRIPTION

The SDC1725 and SDC1726 are modular, continuous tracking Synchro/Resolver to Digital Converters which employ a type 2 servo loop and contain three-state latches on the digital outputs.

The input signals can be either 3 wire synchro plus reference or 4 wire resolver plus reference depending on the option. The outputs will be presented in TTL compatible parallel natural binary, buffered by three-state latches.

*The three-state output facility not only simplifies multiplexing of more than one device onto a single data bus but also enables the "INHIBIT" to be used without opening the internal converter loop.*

Another outstanding feature of these converters is the use of precision Scott T and reference microtransformers. This has made it possible to include internal transformers, even on the 60Hz options, and yet obtain a profile height lower than any other modular Synchro/Resolver to Digital converter currently available.



### MODELS AVAILABLE

The two Synchro/Resolver to Digital Converters described in this data sheet differ primarily in the areas of resolution and accuracy as follows:

Model SDC1725XYZ is a 12-bit converter with an overall accuracy of  $\pm 3.2$  arc-minutes  $\pm 1$ LSB and a resolution of 5.3 arc-minutes.

Model SDC1726XYZ is a 10-bit converter with an overall accuracy of  $\pm 22$  arc-minutes and a resolution of 21 arc-minutes.

The XYZ code defines the option as follows: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the signal and reference voltage and whether it will accept synchro or resolver format.

More information about the option code is given under the heading of "Ordering Information".

### NOTE

No external transformers are required with these converters.



# SPECIFICATIONS (typical at +25°C unless otherwise stated)

| Models  | SDC1725  | SDC1726                         |
|---|--|---------------------------------|
| <b>ACCURACY<sup>1</sup></b><br>(max Error all Options)    | ±3.2 arc-minutes ±1LSB                             | ±22 arc-minutes                 |
| <b>RESOLUTION</b>   | 12 Bits  | 10 Bits                         |
| <b>OUTPUT</b>   | 12-Bits Parallel Natural Binary                    | 10-Bits Parallel Natural Binary |
| <b>SIGNAL AND REFERENCE</b>                               |  |                                 |
| <b>FREQUENCY</b>  | 60Hz, 400Hz, 2.6kHz                                | *                               |
| <b>SIGNAL VOLTAGE (Line to Line)</b>                      |  |                                 |
| Low Level   | 11.8V rms  | *                               |
| High Level  | 90.0V rms  | *                               |
| <b>SIGNAL IMPEDANCES</b>                                  |  |                                 |
| Low Level   | 26kΩ Resistive                                     | *                               |
| High Level  | 200kΩ Resistive                                    | *                               |
| <b>REFERENCE VOLTAGE</b>                                  |  |                                 |
| Low Level   | 26V rms (11.8V Signal)                             | *                               |
| High Level  | 115V rms (90.0V Signal)                            | *                               |
| <b>REFERENCE IMPEDANCE</b>                                |  |                                 |
| Low Level   | 56kΩ (26V Reference)                               | *                               |
| High Level  | 270kΩ (115V Reference)<br>(Impedance is Resistive) | *                               |
| <b>TRANSFORMER ISOLATION</b>                              | 500V dc  | *                               |
| <b>TRACKING RATE (Minimum)</b>                            |  |                                 |
| 60Hz Options  | 5 Revolutions Per Second                           | *                               |
| 400Hz Options   | 36 Revolutions Per Second                          | *                               |
| 2.6kHz Options  | 50 Revolutions Per Second                          | *                               |
| <b>ACCELERATION</b>                                       |  |                                 |
| Constant K <sub>a</sub>                                   |  |                                 |
| 60Hz Options  | 2000/sec <sup>2</sup>                              | *                               |
| 400Hz Options   | 120,000/sec <sup>2</sup>                           | *                               |
| 2.6kHz Options  | 600,000/sec <sup>2</sup>                           | *                               |
| <b>STEP RESPONSE (179° Step)</b><br>(For 1LSB Error)      |  |                                 |
| 60Hz Options  | 1.5sec   | *                               |
| 400Hz Options   | 125ms  | *                               |
| 2.6kHz Options  | 50ms   | *                               |
| <b>POWER LINES</b>  | +15V @ 25mA<br>-15V @ 25mA<br>+5V @ 120mA          | *<br>*<br>*                     |
| <b>POWER DISSIPATION</b>                                  | 1.35 Watts   | *                               |
| <b>DATA LOGIC OUTPUTS<sup>2</sup></b><br>(TTL Compatible) | 6TTL Loads All Options                             | *                               |
| <b>BUSY LOGIC OUTPUT LOADING<sup>2</sup></b>              | 2TTL Loads   | *                               |
| <b>BUSY LOGIC OUTPUT WIDTH<sup>2</sup></b>                | 330ns max  | *                               |
| <b>INHIBIT INPUT (TO INHIBIT)</b>                         | Logic "0" 1 TTL Load                               | *                               |
| <b>ENABLE INPUT (TO ENABLE)</b>                           | Logic "0" 1 TTL Load                               | *                               |
| <b>WARM UP TIME</b>                                       | 1sec to Rated Accuracy                             | *                               |
| <b>TEMPERATURE RANGE</b>                                  |  |                                 |
| Operating   | 0 to +70°C Standard<br>-55°C to +105°C Extended    | *<br>*                          |
| Storage   | -55°C to +125°C                                    | *                               |
| <b>DIMENSIONS</b>   | 3.125" X 2.625" X 0.35"<br>(79.4 X 66.7 X 8.9mm)   | *<br>*                          |
| <b>WEIGHT</b>   | 3.3 ozs (93 gms)                                   | *                               |

\*Specifications the same as for SDC1725.

## NOTES

<sup>1</sup> Specified over the appropriate operating temperature range and for: (a) ±10% signal and reference amplitude variation; (b) 10% signal and reference harmonic distortion; (c) ±5% power supply variation; and (d) ±10% variation in reference frequency.

<sup>2</sup> Schottky logic loading rules apply.

Specifications subject to change without notice.

## THEORY OF OPERATION

If the unit is a Synchro to Digital Converter the 3 wire synchro output will be connected to S1, S2 and S3 on the module and the Scott T transformer pair will convert these signals into resolver format.

$$\text{i.e., } V_1 = K E_0 \sin \omega t \sin \theta$$

$$V_2 = K E_0 \sin \omega t \cos \theta$$

Where  $\theta$  is the angle of the synchro shaft.

If the unit is a Resolver to Digital Converter, the 4 wire resolver output will be connected to S1, S2, S3 and S4 on the module and the microtransformers will act purely as isolators.

To understand the conversion process, assume that the current word state of the up-down counter is  $\phi$ .

Then  $V_1$  is multiplied by  $\cos \phi$  and  $V_2$  is multiplied by  $\sin \phi$  to give:

$$K E_0 \sin \omega t \sin \theta \cos \phi$$

and

$$K E_0 \sin \omega t \cos \theta \sin \phi$$

These signals are subtracted by the error amplifier to give:

$$K E_0 \sin \omega t (\sin \theta \cos \phi - \cos \theta \sin \phi)$$

or

$$K E_0 \sin \omega t \sin (\theta - \phi)$$

A phase sensitive detector, integrator and voltage controlled oscillator (VCO) form a closed loop system which seeks to null  $\sin (\theta - \phi)$ .

When this is accomplished, the word state of the up-down counter ( $\phi$ ) equals, within the rated accuracy of the converter, the synchro shaft angle  $\theta$ .

Assuming that the "INHIBIT" is at a logic high state, then the digital word  $\phi$  will be strobed into the latches 150ns after the up-down counter has been updated. If the three state "ENABLE" is at a logic low, then the digital output word will be presented to the output pins of the module.

## DATA TRANSFER

Data transfer from the SDC1725 and SDC1726 is very straightforward.

Consider the timing sequence shown in the timing diagram which assumes that the input to the converter is changing.

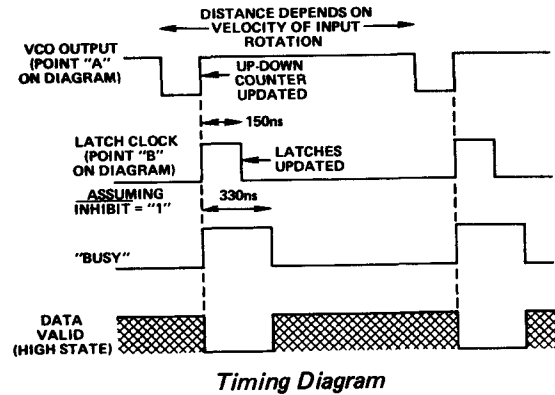
From this diagram, it can be seen that there are two ways to transfer data.

One method is to detect the state of the BUSY signal, which is high for 330ns while the up-down counters and latches are settling, and transfer data when it is in a low state.

However, a much more satisfactory method is to use the "INHIBIT" input. As can be seen from the functional diagram application of the "INHIBIT" prevents the two monostables being triggered and consequently the latches being updated. Therefore, it follows that data will always be valid from 330ns after the INHIBIT has been taken to a logic low state. It can also be seen that this method of data transfer is valid regardless of when the INHIBIT is applied.

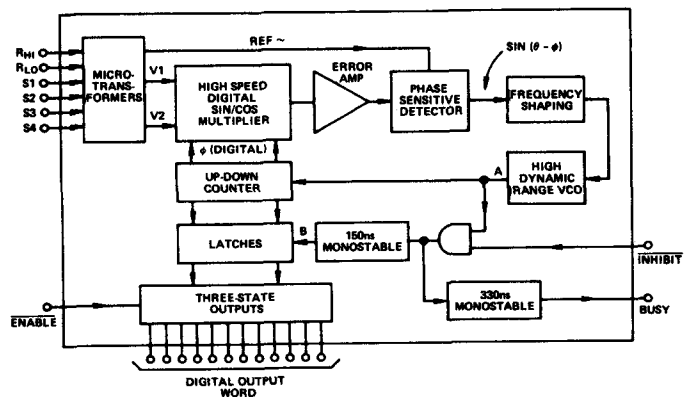
The three-state ENABLE can be used at any time in order to present the data in the latches to the output pins. A logic low on this pin will cause the data to be presented to the outputs.

Note that the operation of the internal converter loop cannot be affected in any way by the logic state present on the INHIBIT and ENABLE pins.



| Bit Number         | Weight in Degrees |
|--------------------|-------------------|
| 1                  | 180.0000          |
| 2                  | 90.0000           |
| 3                  | 45.0000           |
| 4                  | 22.5000           |
| 5                  | 11.2500           |
| 6                  | 5.6250            |
| 7                  | 2.8125            |
| 8                  | 1.4063            |
| 9                  | 0.7031            |
| 10 (LSB - SDC1726) | 0.3516            |
| 11                 | 0.1758            |
| 12 (LSB - SDC1725) | 0.0879            |

**Bit Weight Table**



## CONNECTING THE CONVERTER

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, should be connected to the "+15V", "-15V" and "+5V" pins with the common connection to the ground pin "GND". It is suggested that a parallel combination of a 0.1μF and a 6.8μF capacitor is placed in each of the three positions from "+15V" to "GND", from "-15V" to "GND" and from "+5V" to "GND".

The digital output is taken from pins:

"1" through to "10" for the SDC1726

"1" through to "12" for the SDC1725

Pin "1" represents the MSB in each case.

The reference connections are made to "R<sub>HI</sub>" and "R<sub>LO</sub>".  
 In the case of a Synchro the signals are connected to "S1", "S2" and "S3" according to the following convention:

$$E_{S1} - S3 = E_{RLO} - R_{HI} \sin \omega t \sin \theta$$

$$E_{S3} - S2 = E_{RLO} - R_{HI} \sin \omega t \sin (\theta + 120^\circ)$$

$$E_{S2} - S1 = E_{RLO} - R_{HI} \sin \omega t \sin (\theta + 240^\circ)$$

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

$$E_{S1} - S3 = E_{RLO} - R_{HI} \sin \omega t \sin \theta$$

$$E_{S2} - S4 = E_{RHI} - R_{LO} \sin \omega t \cos \theta$$

The "BUSY", "INHIBIT" and "ENABLE" pins should be connected as described under the heading "Data Transfer".

### RESISTIVE SCALING OF INPUTS

A feature of this range of converters is that the signal and reference inputs can be resistively scaled to accommodate any range of input signal and reference voltages.

This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered.

To calculate the values of the external scaling resistors in the case of a Synchro Converter, add 1.11kΩ per extra volt of signal in series with "S1", "S2" and "S3", and 2.2kΩ per extra volt of reference in series with "R<sub>HI</sub>".

In the case of a Resolver to Digital Converter, add 2.22kΩ in series with "S1" and "S2" per extra volt of signal and 2.2kΩ per extra volt of reference in series with "R<sub>HI</sub>".

For example, assume that we have an 11.8V line to line, 26V reference Synchro Converter, and we wish to use it with a 60V line to line signal with a 115V reference.

In each signal input line, the extra voltage capability required is:

$$60 - 11.8 = 48.2V$$

Therefore each one of the three resistors needs to have a value of:

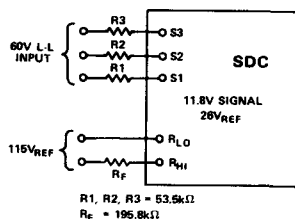
$$48.2 \times 1.11 = 53.5k\Omega$$

Similarly the single resistor needed in series with "R<sub>HI</sub>" can be calculated as being 195.8kΩ.

The inputs of the converter can therefore be scaled as in the diagram below.

### USING THE CONVERTERS WITH OTHER THAN THE SPECIFIED REFERENCE FREQUENCY

A 60Hz converter can be used from 50Hz to 400Hz, and a 400Hz converter can be used from 400Hz up to 2.6kHz, but they will have the dynamic characteristics specified for the unit concerned.



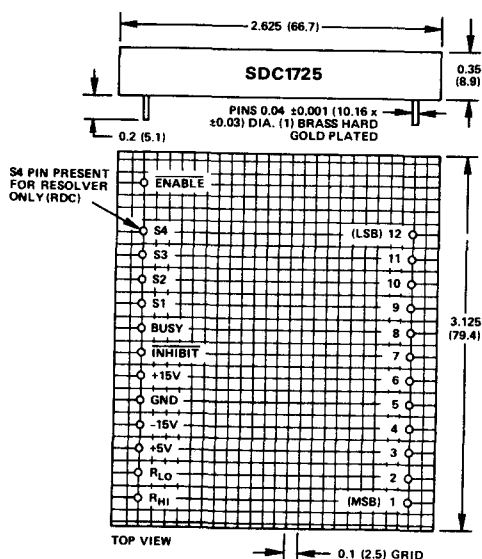
NOTE  
 IN THE CASE OF THE SIGNAL RESISTORS THE RATIO ERRORS BETWEEN THE RESISTANCES IS MORE IMPORTANT THAN THE ABSOLUTE RESISTANCE VALUES.

IN GENERAL A 1% RATIO ERROR WILL GIVE RISE TO AN EXTRA INACCURACY OF 17 ARC-MINUTES WHILE A RATIO ERROR OF 0.1% WILL GIVE RISE TO AN EXTRA INACCURACY OF 1.7 ARC-MINUTES. THE ABSOLUTE VALUE OF R<sub>f</sub> IS NOT CRITICAL.

R1, R2, R3 = 53.5kΩ  
 R<sub>f</sub> = 195.8kΩ

### OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).



NOTE  
 THE ABOVE DIAGRAM SHOWS THE CONNECTIONS FOR THE SDC1725. ON THE SDC1726, PINS 11 AND 12 ARE OMITTED AND PIN 10 IS THE LSB.

### ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by an option code in order to fully define them. All the standard options and their option codes are shown below. For options not shown, please consult the factory.

| Part Number | Resolution | Operating Temp. Range | L to L Voltage/Format | Ref. Voltage | Ref. Freq. |
|-------------|------------|-----------------------|-----------------------|--------------|------------|
| SDC1725511  | 12 Bits    | 0 to +70°C            | 11.8V Synchro         | 26 Volts     | 400Hz      |
| SDC1725611  | 12 Bits    | -55°C to +105°C       | 11.8V Synchro         | 26 Volts     | 400Hz      |
| SDC1725512  | 12 Bits    | 0 to +70°C            | 90.0V Synchro         | 115 Volts    | 400Hz      |
| SDC1725612  | 12 Bits    | -55°C to +105°C       | 90.0V Synchro         | 115 Volts    | 400Hz      |
| RDC1725518  | 12 Bits    | 0 to +70°C            | 11.8V Resolver        | 26 Volts     | 400Hz      |
| RDC1725618  | 12 Bits    | -55°C to +105°C       | 11.8V Resolver        | 26 Volts     | 400Hz      |
| SDC1725522  | 12 Bits    | 0 to +70°C            | 90.0V Synchro         | 115 Volts    | 60Hz       |
| SDC1725622  | 12 Bits    | -55°C to +105°C       | 90.0V Synchro         | 115 Volts    | 60Hz       |
| SDC1725541  | 12 Bits    | 0 to +70°C            | 11.8V Synchro         | 26 Volts     | 2.6kHz     |
| SDC1725641  | 12 Bits    | -55°C to +105°C       | 11.8V Synchro         | 26 Volts     | 2.6kHz     |
| RDC1725548  | 12 Bits    | 0 to +70°C            | 11.8V Resolver        | 26 Volts     | 2.6kHz     |
| RDC1725648  | 12 Bits    | -55°C to +105°C       | 11.8V Resolver        | 26 Volts     | 2.6kHz     |

Note

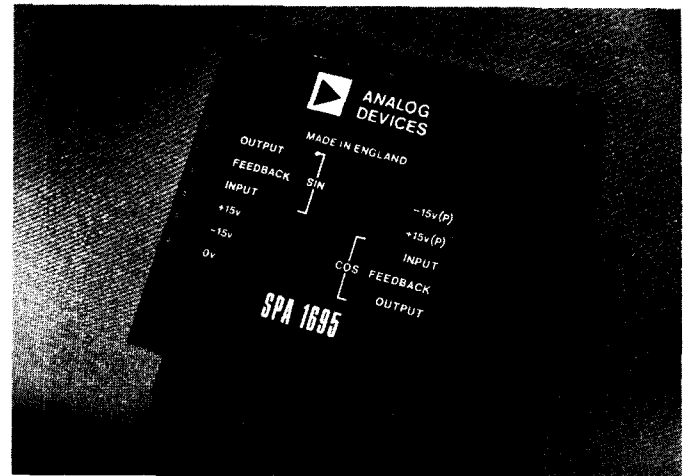
For 10-bit resolution, substitute 1726 in place of 1725 in the part number above.

### FEATURES

5VA Output – Capable of Driving 4 Size CT's  
 Indefinite Short Circuit Protection  
 Metal Case Acts as Heatsink  
 Easily Mounted  
 Voltage Sensing Facility  
 Operation with No Derating Up to +105°C  
 Suitable for 50 to 400Hz Operation

### APPLICATIONS

Can Be Used With the Digital Vector Generators (DTM1716 and DTM1717) to Drive Control Transformers (CT's)



### GENERAL DESCRIPTION

The SPA1695 is a two channel amplifier intended for use in conjunction with the DTM1716 and DTM1717 Digital Vector Generators for driving Control Transformers (CT's).

The unit is capable of supplying 5VA to the load and therefore can be used in cases where the internal amplifiers of a Digital to Synchro Converter are not sufficient (i.e., in general when the load exceeds 1.3VA).

The SPA1695 is contained in an aluminium case which has pre-drilled flanges for mounting purposes and excellent heatsinking properties.

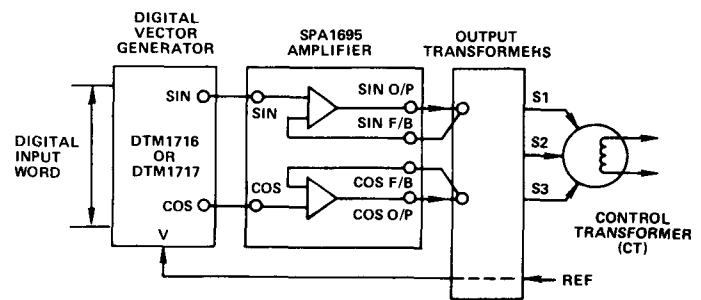
The amplifier has no derating up to +105°C and is indefinitely short circuit protected at 25°C ambient.

The unit accepts resolver format inputs (Sine and Cosine) at 7 volts rms max. The output of the amplifier is in resolver format at 7 volts rms max and should be fed into suitable transformers (see ordering information).

Voltage sensing pins are provided to compensate for any voltage drop which may occur between the output of the amplifier and the output transformer.

### MODELS AVAILABLE

The SPA1695 does not require any option numbers in order to fully specify it. The standard unit operates over the frequency range 50 to 400Hz and over the temperature range of -55°C to +105°C.



*Implementation of the SPA 1695 Amplifier*

### SCHEMATIC DIAGRAM OF AN SPA1695 AMPLIFIER BEING USED TO DRIVE A CONTROL TRANSFORMER (CT)

The above diagram shows a Digital Vector Generator being used in conjunction with the SPA1695 amplifier and external transformers to drive a Control Transformer.

The diagram illustrates the use of the Sine and Cosine feedback pins ("Sin F/B" and "Cos F/B").

## SPECIFICATIONS (typical at 25°C unless otherwise noted)

|  |   |
|--|---|
| POWER OUTPUT <sup>1</sup>                | 5VA   |
| ACCURACY <sup>2</sup> (between channels) | 2 arc-minutes                                 |
| GAIN ACCURACY <sup>2</sup> (matching)    | 0.1%  |
| INPUT VOLTAGE (per channel)              | 7V rms  |
| OPERATING FREQUENCY                      | 50 to 400Hz                                   |
| INPUT IMPEDANCE                          | Greater than 50kΩ                             |
| INPUT BIAS CURRENT                       | Less than 1μA                                 |
| GAIN (per channel)                       | Unity   |
| INPUT DRIFT                              | 50μV/°C                                       |
| INITIAL OUTPUT OFFSET                    | 3mV max at 25°C                               |
| CROSS OVER DISTORTION                    | 0.01% max                                     |
| DERATING OF AMPLIFIER                    | None up to +105°C                             |
| POWER SUPPLY REQUIREMENTS:               |   |
| ±15V(P) No Load                          | 115mA Unregulated                             |
| ±15V(P) Average Full Load                | 630mA Unregulated                             |
| ±15V                                     | 15mA Regulated                                |
| WEIGHT                                   | 275 Grams (9.7 ozs)                           |
| SIZE                                     | 3.46" x 2.68" x 0.98"<br>(88mm x 68mm x 25mm) |
| OPERATING TEMPERATURE RANGE              | -55°C to +105°C                               |
| STORAGE TEMPERATURE RANGE                | -55°C to +125°C                               |

### NOTES:

- Power output is sufficient to drive four 400Hz 90 volts line to line control transformers.
- Valid over full temperature range of -55°C to +105°C.

Specifications subject to change without notice.

## CONNECTING THE SPA1695

The diagram shows the connection of the SPA1695 to the DTM1716 or DTM1717 Digital Vector Generator, and STM1686 output and reference transformers.

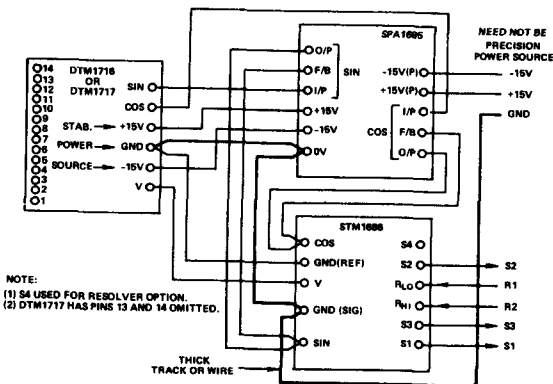


Diagram Showing Connection of the SPA1695 to a DTM1716 or DTM1717 and STM1686

### NOTES:

- The "Sin F/B" and the "Cos F/B" pins of the SPA1695 should be connected directly to the "Sin" and "Cos" terminals on the output transformer at the transformer. This is to compensate for any drop in voltage along the connections between the "Sin O/P" and "Cos O/P" pins of the amplifier and the transformer.
- The "+15V" and "-15V" pins of the SPA1695 should be connected to a regulated power supply in order to drive the internal operational amplifiers. The "+15V(P)" and "-15V(P)" are used for the output stage and these supplies need not be a precision source. The minimum voltage when considering all tolerances including ripple, should be between 14.75 and 20 volts.
- The part of the 0 volt system local to the amplifier and converter should be tapped from the "GND(SIG)" pin on the transformer and should not interconnect with any other part of the 0 volt system by any other method (see above diagram).
- In the above diagram, connection is also shown between the reference transformers, contained in the STM1686 and the Digital Vector Generator.

## USING TWO SPA1695 AMPLIFIERS IN PUSH-PULL CONFIGURATION

Twice the output power may be achieved by connecting the outputs from two SPA1695 amplifiers in push-pull configuration, the two devices being fed with out of phase signals.

For more information consult the factory.

## ADDITIONAL HEATSINKING

Although the SPA1695 case will provide the necessary heatsink properties to allow the amplifier to provide the 5VA power output over the full temperature range, it is recommended that additional heatsinking be provided where possible.

## ORDERING INFORMATION AND TRANSFORMER TYPE

Part number SPA1695 is sufficient to specify the amplifier – no option codes are needed.

The transformers should be ordered according to the following:

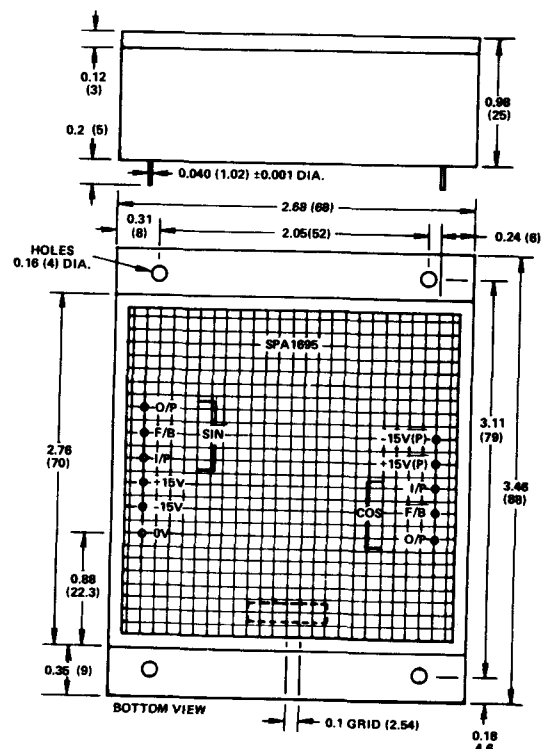
|            |  |
|------------|--|
| STM1686611 | 400Hz, Synchro output, 11.8 volt signal, 26 volt reference.  |
| STM1686612 | 400Hz, Synchro output, 90 volt signal, 115 volt reference.   |
| STM1686618 | 400Hz, Resolver output, 11.8 volt signal, 26 volt reference. |
| STM1687622 | 50/60Hz, Synchro output, 90 volt signal, 115 volt reference. |

### NOTES:

- Above transformers are suitable for use over the temperature range -55°C to +105°C.
- If it is required to use the SPA1695 with Digital to Resolver converters, then use:
  - STM1736 for 400HZ and STM1737 for 50/60Hz systems in the case of the DRC1605 and DRC1606 converters.
  - STM1696 for 400Hz and STM1697 for 50/60Hz systems in the case of the DRC1705 and DRC1706 converters.

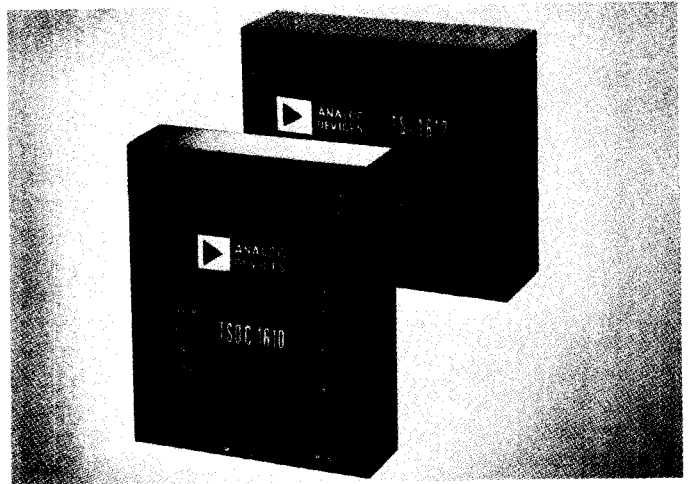
## AMPLIFIER OUTLINE DIMENSIONS AND PIN CONNECTION DIAGRAM

Dimensions shown in inches and (mm).



**FEATURES**

- Both Binary and Non-Binary Ratios
- Digital Non-Binary Ratio Two Speed Processors
- Binary Two Speed Converters
- All Units Modular Construction
- Military Versions Available



**DESCRIPTION**

This data sheet describes two products both concerned with two speed (sometimes called coarse/fine) synchro data transmission; they are, the TSL 1612 and the TSDC 1608 thru TSDC 1611. The TSL 1612 is a two speed data processor i.e., it takes as inputs two sets of digital information representing the angles from the coarse and fine synchros and combines these to produce a single 19-bit word representing the angle of the coarse shaft. The TSL 1612 deals with the non-binary ratios 36:1, 18:1 and 9:1. Its inputs will be derived from synchro to digital converters contained in separate modules.

Figures 1 and 2 show the difference between the Two Speed Digital Converters and the Two Speed Digital Processor modules.

The TSDC 1608 thru TSDC 1611 are for the gear ratios of 8:1, 16:1, 32:1 and 64:1. The TSDC 1608 thru TSDC 1611 take as inputs angular information in synchro form from the coarse two speed shaft together with digital information from the two coarse digits from a separate synchro to digital converter on the fine shaft. The digital output is a combination of the fine synchro to digital converter digits and the digits from the TSD 1608. Two speed digital converter systems contain "synchronizing" logic for avoiding ambiguous codes and generally require more explanation than other converters. See the following pages for information on some of the general questions that may arise with these systems.

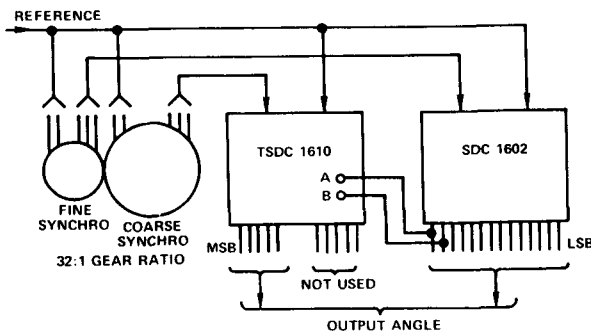


Figure 1. Coarse/Fine Synchro Converter System

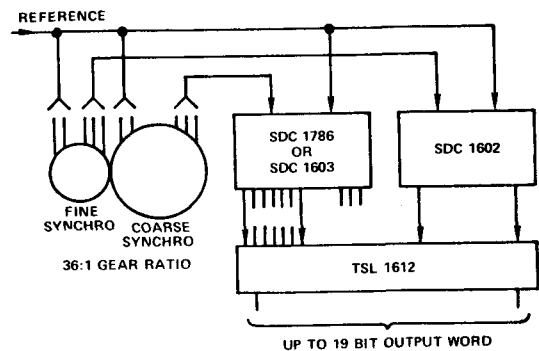


Figure 2. Coarse/Fine Synchro Processor System

# Two Speed Synchro To Digital Binary Ratios TSDC 1608 thru 1611

## FEATURES

- Contains 10 Bit Synchro to Digital Converter
- Contains Two Speed Processor
- Works With Any Fine Synchro to Digital Converter
- Military Version Available
- 400Hz or 60Hz Operation

## DESCRIPTION

Models TSDC 1608 thru 1611 are 10 bit tracking synchro to digital converters with electrical characteristics the same as the SDC 1603 except that the TSDCs include two speed processing logic for binary coarse/fine systems. The difference between the models is in the positioning of the CD connections, see Figure 6. Modules 1608, 1609, 1610 and 1611 are suitable for gear ratios of 8:1, 16:1, 32:1 and 64:1 respectively. The 400Hz versions have all the transformers inside the module; 60Hz versions have an external transformer module. The model number e.g., TSDC 1608 must be followed by an XYZ code defining the temperature range, frequency and voltages; for details see the ordering information which gives the coding.

The synchronizing data is taken from the two MSBs of the fine synchro converter to the inputs A and B (see Figure 4). The number of digits used from the TSDC is  $\log_2 N$  where N is the binary ratio. The full range of digits are brought out of the TSDCs so that they can be also used as normal synchro to digital converters; for this use, the inputs A and B must be set logically at A≠B.

## SPECIFICATIONS (typical @ +25°C unless otherwise noted)

|  |   |
|--|---|
| Accuracy* (max)                          | ±30 Arc Minutes   |
| Resolution                               | 10 Bits (1LSB = 21 Arc Minutes)                           |
| Output (TTL Levels)                      | 10 Bits Natural Parallel Binary                           |
| Fan Out                                  | 4 TTL Loads   |
| Transformer Isolation                    | 500V dc   |
| Tracking Rate                            | 2880°/Second  |
| Step Response (179°)                     | 200ms for 1LSB  |
| Signal and Reference Voltages            | All Standard Synchro or Resolver Voltages and Frequencies |
| Signal Impedance and Reference Impedance | 200kΩ High Level<br>20kΩ Low Level                        |
| Power Supplies                           | ±15V @ 35mA<br>+5V @ 190mA                                |
| Operating Temperature Range              | 0 to +70°C<br>or -55°C to +105°C                          |
| Dimensions                               | 3.125" x 2.625" x 0.8"<br>79.4mm x 66.6mm x 20.5mm        |
| Weight                                   | 7ozs (200 grams)  |

- \*Accuracy applies over the operating temperature range and for:—
- ±10% signal and reference amplitude variation
  - ±10% reference and signal frequency variation
  - 10% signal and reference harmonic distortion
  - ±5% power supply variation
  - ±20° phase shaft between reference and signal waveforms

Specifications subject to change without notice.

290S S/D AND D/S CONVERTERS

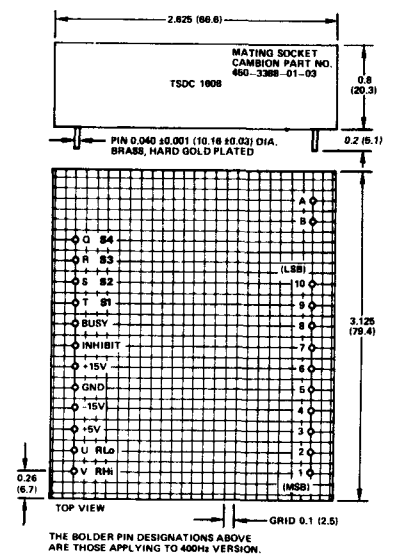
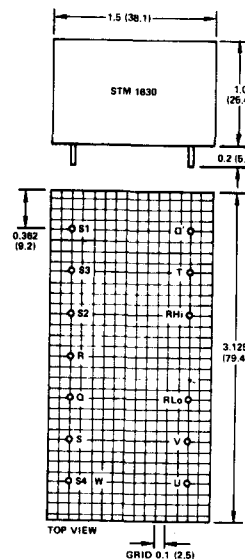
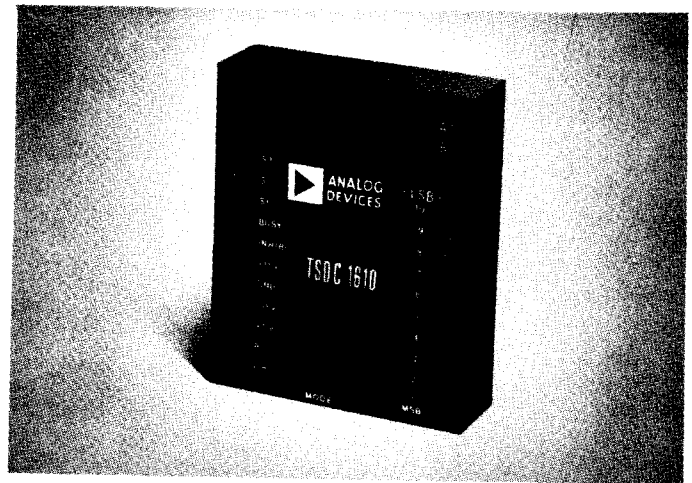


Figure 3.

Figure 4.

Dimensions shown in inches and (mm).

## CONNECTIONS

**400Hz operation** - The 400Hz versions of the TSDC modules have both the input signal and reference transformer contained inside the module. The signal inputs are connected by means of the pins shown S1, S2, S3 and S4, see Figure 4. In the case of synchro input S1, S2 and S3 are used. For resolver inputs the sine input is applied to S1 and S3, and the cosine input to S2 and S4. The reference inputs are applied to the pins marked RH<sub>i</sub> and RLo. The polarities of the connections are such that if S1, S2 and RLo are common the voltages on S3, S4 and RH<sub>i</sub> are in time phase in the first quadrant.

**60Hz operation** - The 60Hz versions of the TSDC modules do not contain either the signal or the reference transformers. An external transformer module STM 1630/XYZ contains the signal and reference transformers. The pins QRST, U and V on the TSDC module connect to the pins QRST, U and V on the transformer module. The signal and reference inputs connect to the pins marked S1, S2, S3, W and RLo, RH<sub>i</sub> on the transformer module with the same meaning for these pins as in the 400Hz case where W replaces S4. The pin marked Q' is not used (see Figure 3).

# Two Speed Processor TSL 1612

## FEATURES

- 36:1, 18:1 or 9:1 Ratios With Same Module
- No False Output Readings
- Fast (500ns) Parallel Operation
- Easy to Use
- Up to 19 Bits Electronic Accuracy

## DESCRIPTION

Model TSL 1612 is for use with synchro to digital converters in either electrically or mechanically geared coarse/fine two speed synchro systems. It is specifically designed for 36:1, 18:1 and 9:1 gear ratios.

The digital inputs to the TSL 1612 are up to 14 bits from the fine converter and up to 7 bits from the coarse converter according to the gear ratio required. The output is up to 19 bits parallel binary angle data. The module may be used with any synchro converters which produce parallel binary output.

The connections of the coarse inputs and the TSL 1612 outputs change according to the ratio to be obtained. For all ratios the fine SDC outputs connect directly to the fine TSL 1612 inputs i.e., Bit (1) out to Bit (1) in thru to Bit 14 out to Bit 14 in. For 36:1 ratio Bits 1 to 7 out of the coarse SDC connect to Bit 1 to 7 coarse inputs of the TSL 1612, and the outputs are taken from Bits 1 to 19. For 18:1 ratio Bits 1 to 6 out of the SDC connect to Bits 2 to 7 inputs of the TSL 1612. The outputs from the TSL are taken from Bits 2 to 19. For 9:1 operation the coarse inputs Bits 1 to 5 from the SDC are connected to Bits 3 to 7 on the coarse TSL inputs. The outputs are taken from Bits 3 thru to 19.

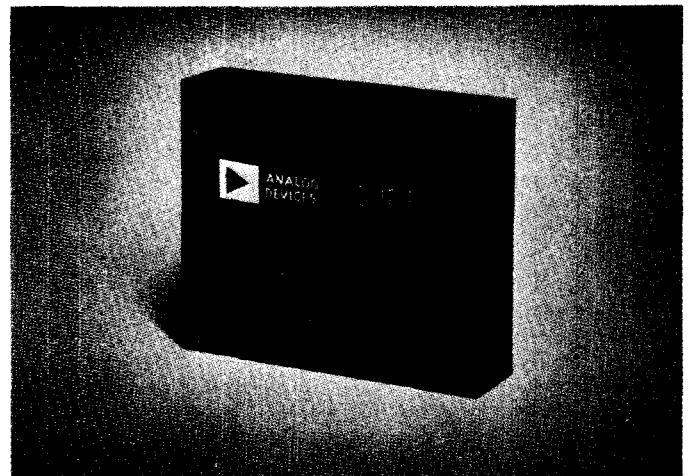
Unused inputs to the TSL are connected to ground. Unused outputs are left open circuit. If a synchro to digital converter with <14 bits output is used, the unused LSB inputs to the TSL 1612 must be grounded.

The TSL 1612 can be used with both tracking and sampling synchro to digital converters; in particular, it can be used with the multiplexed synchro to digital converter SSD 1625. Two channels of the multiplex system are used; one for the coarse synchro and one for the fine. Multiplexed sampling converters permit operation at higher speeds than are possible with tracking type systems. The SSD 1625 multiplex system consists of three basic units i.e., sample and hold, peak detector and SSD converter module; additional latches

## SPECIFICATION

|                      |   |
|----------------------|---|
| Ratios:              | 36:1, 18:1, 9:1                                   |
| Fine Synchro Input   | Up to 14 Bits Parallel Binary Angle               |
| Coarse Synchro Input | Up to 7 Bits Parallel Binary Angle                |
| Logic Levels         | DTL/TTL Compatible                                |
| Input Loading        | 2TTL Loads  |
| Output Fan Out       | 5TTL Loads  |
| Digital Output       | Up to 19 Bits Parallel Binary Angle               |
| Conversion Time      | 500ns   |
| Temperature Range    | 0 to +70°C<br>-55°C to +105°C                     |
| Power Supplies       | +5V ±5% @ 600mA                                   |
| Size                 | 3.125" x 2.625" x 0.4"<br>79.4mm x 66.6mm x 102mm |
| Weight               | 3.5ozs. 100 grams                                 |

Specifications subject to change without notice.



must be used between the SDD and the TSL 1612 to hold over the information for simultaneous use in the TSL 1612.

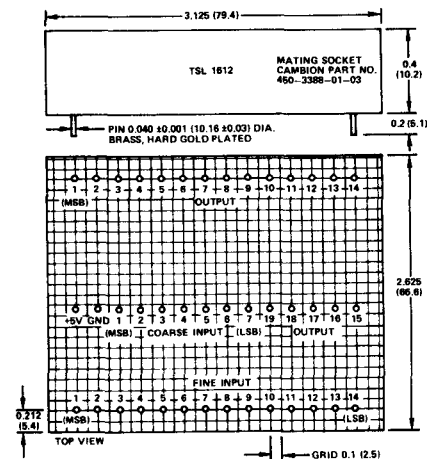


Figure 5.

Dimensions shown in inches and (mm).

## GENERAL INFORMATION ON COARSE/FINE SYNCHRO SYSTEMS

Coarse/fine synchro systems are used when it is required to set or transmit the angle of a shaft to an accuracy which is higher than that which could be obtained by the use of a single synchro transmitter. The angular accuracy of measurement by a single synchro is limited by the technology concerned with producing accurate sine law output magnitudes as a function of the shaft angle. (A good synchro will have an accuracy of about 3 arc minutes.) This limitation can be overcome by the use of either an additional multipole synchro on the same shaft or by the use of gearing to an additional synchro on another shaft. The two synchros used are referred to as the coarse and fine synchros. Two speed systems using gearing will have an accuracy which is limited by the backlash in the gears. To obtain an improvement in accuracy with a two speed system, the errors due to backlash must be less than the inaccuracy of the single coarse synchro. With two speed systems, the accuracy requirements on the synchros are far less stringent; the coarse synchro must be capable of determining the angle to better than 90° on the fine shaft, and the fine synchro must be capable of determining the angle to better than the backlash angle on the fine shaft. The most common ratios for two speed systems are 1:8, 1:9, 1:32 and 1:36.



In following the logic concerned with the operation of the two speed digital converters and processors it is important to understand that the reading of the fine synchro dominates in the determination of the coarse shaft angle despite the backlash in the gears. The reason for this is implied in the earlier paragraph. If the error in determining the coarse shaft angle from the coarse synchro electrical signals is  $E_1$ , if the backlash angle on the coarse shaft (by holding fine shaft fixed) is  $E_2$ , and if the error in determining the fine shaft angle from the fine synchro electrical signals is  $E_3$ , then

$$\frac{E_3}{R} < E_2 < E_1 \text{ where } R \text{ is the gear ratio.}$$

This means that we cannot do better than to assure that the fine shaft angle is the best indication of the coarse shaft position.

In the two speed digital converters which receive inputs from both the coarse and fine synchros, circumstances will occur when the coarse angle determined by the most significant digits of fine synchro will conflict with the overlapping least significant digits of the coarse synchro. (This is due to the backlash in the gearing causing different readings at the major transition points.) Digital logic circuits for resolving this conflict are included in the converters. The digital reading from the fine synchro is made to dominate in the overlapping region and a correction is made bringing the coarse reading into line to provide an unambiguous digital representation of the angle of the coarse shaft.

To see that the coarse angle cannot be determined to a greater accuracy than the backlash angle, the fine synchro can be held fixed; a rotation of the coarse synchro through the backlash angle will not change the output digital reading.

#### LOGIC FOR REMOVING BACKLASH AMBIGUITY (SYNCHRONIZING LOGIC)

Figure 6 shows two shafts coupled by gears which have the coarse and fine synchros coupled to synchro to digital converters which give out angular information in natural binary form with the MSB of each converter corresponding to 180° rotation of the appropriate shaft. For the purpose of this point the gear ratio is taken to be a binary number of 32:1, for non-binary gear ratios the digital outputs are modified to have similar bit weights and the same type of synchronizing logic is used.

In Figure 6 the unit inside the TSDC 1610 shown as the synchronizing logic unit compares the inputs A and B and according to the result either adds or subtracts "1" from DC which may result in a carry into the adder/subtractor unit. The logic of the comparison is: if  $A=B=0$  add 1 to C. If  $A=B=1$  subtract 1 from C. If  $A \neq B$  do not change C. The backlash is assumed to be less than the angle represented by C. All the possible states of the logic levels A, B, C and D that may occur as outputs of the SDCs together with the carry output are shown in Table 1.

|    |    | AB - 2 MSBs OF THE FINE SDC |   |    |   |    |   |    |   |   |   |   |   |
|----|----|-----------------------------|---|----|---|----|---|----|---|---|---|---|---|
| DC | AB | 00                          |   | 01 |   | 10 |   | 11 |   |   |   |   |   |
|    |    | K                           | D | C  | K | D  | C | K  | D | C |   |   |   |
| 00 | 00 | 0                           | 0 | 1  | 0 | 0  | 0 | 0  | 0 | 0 | 1 | 1 | 1 |
| 01 | 01 | 0                           | 1 | 0  | 0 | 0  | 1 | 0  | 0 | 1 | 0 | 0 | 0 |
| 10 | 10 | 0                           | 1 | 1  | 0 | 1  | 0 | 0  | 1 | 0 | 0 | 0 | 0 |
| 11 | 11 | 1                           | 1 | 0  | 0 | 1  | 1 | 0  | 1 | 1 | 0 | 1 | 0 |

DIGITS 0, 1 AND 0, 2 WHERE RATIO 1/2 AND DIGITS 1, 0, 1 ARE MODIFIED BY THE CARRY K

IF A = 0, B = 0 ADD 1 TO C  
 IF A = 1, B = 1 SUBTRACT 1 FROM C  
 IF A ≠ B NO ACTION  
 RESULT K, D, C ONLY K IS USED TO ADD OR SUBTRACT FROM COARSE DIGITS

Table 1. Diagram Showing the Logic of the Synchronizing Unit Inside the TSDC 1610

#### NON-BINARY RATIOS

In the non-binary digital two speed coarse/fine digital processor an exactly analogous arrangement is used except that it is necessary to multiply the coarse digits by the gear ratio using a digital shift and add multiplier to make the overlapping digits have the same bit weight. Having obtained a uniform bit weight by multiplying by 36 in the case of a 36:1 gear ratio the two MSBs of the fine digits are compared and the same logical operations are performed as in the binary gear ratio case. The resulting outputs are then converted back by a digital shift and add multiplier into weights corresponding to the coarse angle.

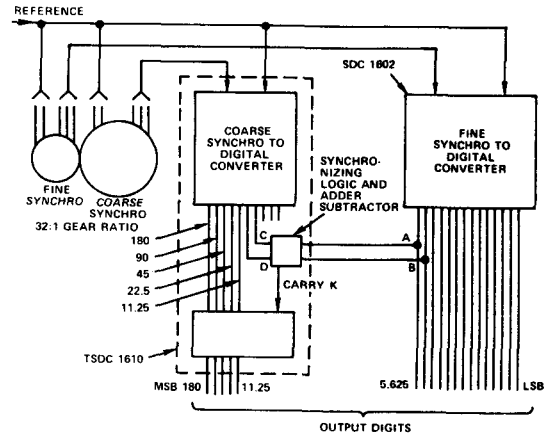


Figure 6. Diagram Showing the Arrangement of the Two SDCs Together With Synchronizing Logic

#### ORDERING INFORMATION

The TSL 1612 and TSDC 1608 - 1611 are available in two temperature ranges. The TSDC 1608 - 1611 also have frequency and voltage variations. To define these variations the type number must be followed by X, Y or Z where:—

- X = 5 signifies temperature 0 to +70°C
- X = 6 signifies temperature -55°C to +105°C
- Y = 1 signifies reference frequency of 400Hz
- Y = 2 signifies reference frequency of 60Hz
- Y = 0 Not applicable to that device
- Z = 1 signifies synchro signal voltage 11.8V reference 26.0V (Y must equal 1)
- Z = 2 signifies synchro signal voltage 90.0V reference 115.0V (Y equals 1 or 2)
- Z = 3 signifies resolver signal voltage 11.8V reference 11.8V (Y must equal 1)
- Z = 4 signifies resolver signal voltage 26.0V reference 26.0V (Y must equal 1)
- Z = 5 signifies resolver signal voltage 90.0V reference 90.0V (Y equals 1 or 2)
- Z = 6 signifies resolver signal voltage 115.0V reference 115.0V (Y equals 1 or 2)
- Z = 8 signifies resolver signal voltage 11.8V reference 26.0V (Y must equal 1)
- Z = 0 Not applicable to that device

Transformers for 400Hz use are encapsulated in the module.

Transformers for 60Hz use are external to the module and must be ordered separately.

The transformer module for 60Hz operation of the TSDC 1608 - 1611 is type No. STM 1630/X2Y.

### FEATURES

Aperture Times to 20ps  
 Acquisition Times to 20ns  
 Linearity 0.01%  
 $10^{10} \Omega$  Input Z (HTS-0025)  
 $\pm 50\text{mA}$  Output Current

### APPLICATIONS

Data Acquisition Systems  
 Data Distribution Systems  
 Peak Measurement Systems  
 Simultaneous Sample & Hold  
 Analog Delay & Storage

### GENERAL DESCRIPTION

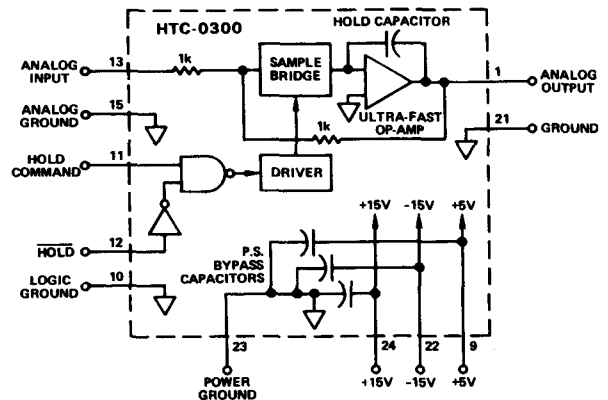
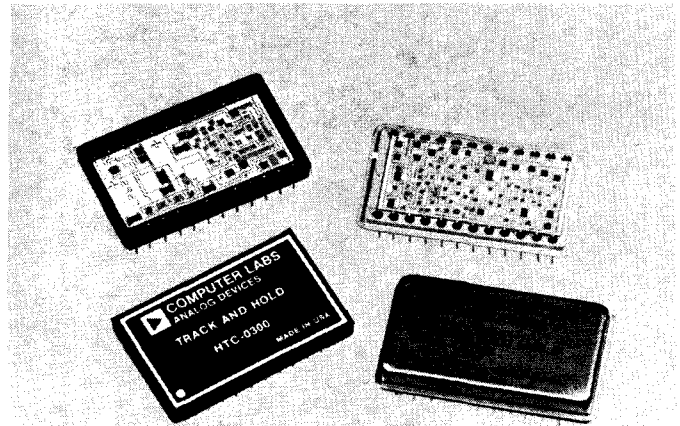
The HTS-0025 and HTC-0300 represent "state of the art" in the ability of an analog device to capture and hold rapidly changing transient or continuous waveforms. The user can choose between them by making engineering trade-offs between maximum speed/bandwidth capability, precision gain, feedthrough rejection, input impedance, hold time, harmonic distortion, output swing, logic type, power requirements and price. With an aperture uncertainty of only 20ps and an acquisition/settling time of 20ns, the HTS-0025 is the fastest hybrid sample/track-and-hold amplifier available.

It achieves this performance with a dc coupled Schottky diode sampling bridge driven by a  $10^{10} \Omega$  input impedance FET amplifier and followed by a low impedance  $-10 \Omega$  max - output amplifier.

The HTC-0300 provides 100ps aperture uncertainty and 100ns acquisition/settling time to 0.1% for a 10 volt input-output swing (less than 150ns for 12-bit settling). It achieves this speed and precision gain ( $-1.00 \pm 0.1\%$ ) with high speed op amps and diode switches. These techniques also improve feedthrough rejection, output swing, linearity, harmonic distortion and droop rate.

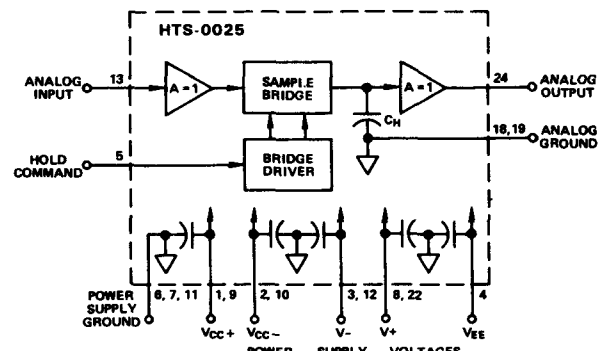
### APPLICATIONS

The most common use for a sample/track-and-hold is to place it ahead of an A/D converter to allow digitizing of signals with bandwidths higher than the digitizer alone can handle. The use of the HTS-0025 can allow a reduction of system aperture to 20ps. These sample/track-and-hold amplifiers are also used for peak holding functions, simultaneous sampling A/D's (with appropriate analog multiplexing), and other high-speed analog signal processing applications. These hybrids have been used to construct A/D converters of up to 12 bits of resolution with word rates as high as 20MHz. The HTC-0300 is designed to be used with Analog Devices' HAS Series hybrid A/D converters.



NOTE: PIN 12 SHOULD BE GROUNDIED IF NOT USED.

Block Diagram - HTC-0300



NOTE: PIN 12 SHOULD BE GROUNDIED IF NOT USED.

Block Diagram - HTS-0025

# SPECIFICATIONS (typical at +25°C and nominal power supply voltages unless noted otherwise)

| MODEL  | UNITS              | HTS-0025                            | HTS-0025M                           | HTC-0300             | HTC-0300M          |
|--|--------------------|-------------------------------------|-------------------------------------|----------------------|--------------------|
| <b>DYNAMIC CHARACTERISTICS</b>   |                    |                                     |                                     |                      |                    |
| Acquisition Time (See Figure 1)<br>to 1% for 1V Output Step<br>to 0.1% for 10V Output Step | ns typ (max)       | 20 (30)                             | *                                   | N/A                  | **                 |
| Sample Rate <sup>1</sup>   | ns typ (max)       | N/A                                 | *                                   | 100 (170)            | 100 (200)          |
| Aperture Time  | MHz max            | 30                                  | *                                   | 5                    | **                 |
| Settling Time  | ns min (typ) (max) | 6 (10) (20)                         | *                                   | *                    | *                  |
| Bandwidth (3dB 2V p-p Input)<br>(3dB Small Signal Input)                                   | ns typ (max)       | 20 (30)                             | *                                   | 100 (120)            | **                 |
| Slew Rate  | MHz min            | 30                                  | 20                                  | N/A                  | **                 |
| Aperture Uncertainty   | MHz min            | N/A                                 | *                                   | 8                    | **                 |
| Harmonic Distortion (See Figure 6 and<br>Output Loading)                                   | V/μs typ (min)     | 400 (200)                           | *                                   | 250 (120)            | 250 (100)          |
| Feedthrough Rejection (2V p-p, 10MHz Input)<br>(dc to 2.5MHz)                              | ps (rms) max       | 20                                  | *                                   | 100                  | **                 |
| Droop Rate   | dB typ (max)       | 65 (60)                             | *                                   | 75 (62)              | **                 |
| Pedestal During Hold (See Figure 1)  | dB min             | 70                                  | *                                   | N/A                  | **                 |
| Transients (See Figure 1)  | dB min             | N/A                                 | *                                   | 70                   | **                 |
|  | mV/μs typ (max)    | 0.2 (4) <sup>2</sup>                | 0.2 (30)                            | 0.005 (0.007)        | 0.005 (0.1)        |
|  | mV typ (max)       | 2 (20)                              | *                                   | 5 (50)               | **                 |
|  | mV typ (max)       | 30 (100)                            | *                                   | N/A                  | **                 |
| <b>ACCURACY/STABILITY DC</b>   |                    |                                     |                                     |                      |                    |
| Gain   | V/V                | +0.92 min                           | *                                   | -1.00 ±0.1%          | **                 |
| Gain vs. Temperature   | ppm/°C typ (max)   | 20 (40)                             | *                                   | 10 (50)              | **                 |
| Zero Offset Voltage  | mV typ (max)       | 2 (20)                              | *                                   | 2 (20)               | **                 |
| Offset vs. Temperature   | typ (max)          | 50 (150)μV/°C                       | *                                   | 10 (15)ppm/°C        | **                 |
| Linearity  | % max              | 0.01                                | *                                   | *                    | *                  |
| <b>INPUT</b>   |                    |                                     |                                     |                      |                    |
| Voltage Range  | V max              | ±2                                  | *                                   | ±10                  | **                 |
| 60dB Feedthrough Rejection   | V p-p max          | 3                                   | *                                   | N/A                  | **                 |
| Impedance  | Ω typ (min)        | 10 <sup>10</sup> (10 <sup>9</sup> ) | 10 <sup>10</sup> (10 <sup>8</sup> ) | 1000                 | **                 |
| Bias Current   | nA max             | 15                                  | 100                                 | 2                    | **                 |
| <b>OUTPUT</b>  |                    |                                     |                                     |                      |                    |
| Voltage  | V max              | ±2                                  | *                                   | ±10                  | **                 |
| Current (not short circuit protected)  | mA max             | ±50                                 | *                                   | *                    | *                  |
| Impedance  | Ω typ (max)        | 3 (10)                              | *                                   | 0.1 (dc)             | **                 |
| Loading — Harmonic   |                    |                                     |                                     |                      |                    |
| Distortion for 2V p-p  | 50dB               | Ω min                               | 50                                  | *                    | **                 |
| Signal and Specified R <sub>L</sub>  | 60dB               | Ω min                               | 100                                 | *                    | **                 |
|  | 65dB               | Ω min                               | 200                                 | *                    | **                 |
| Noise <sup>3</sup>   | mV rms             | 0.1 (max)                           | 0.2 (max)                           | 0.1                  | **                 |
| <b>HOLD COMMAND (DIGITAL INPUT)</b>  |                    |                                     |                                     |                      |                    |
| Logic Compatible   |                    | ECL                                 | *                                   | TTL                  | **                 |
| "0" = Track/"1" = Hold <sup>4</sup>  | V                  | -1.5 to -1.4/-0.7 to -1.05          | *                                   | N/A                  | **                 |
| "Hold" Input, "0" = Track/"1" = Hold   | V                  | N/A                                 | *                                   | 0 to +0.4/+2.4 to +5 | **                 |
| "Hold" Input, "0" = Hold/"1" = Track   | V                  | N/A                                 | *                                   | 0 to +0.4/+2.4 to +5 | **                 |
| <b>POWER REQUIREMENTS — HTS</b>  |                    |                                     |                                     |                      |                    |
| V <sup>+</sup> = +15V ±0.5V (Pins 8 and 22)  | mA max             | 40                                  | *                                   | N/A                  | **                 |
| V <sup>-</sup> = -15V ±0.5V (Pins 3 and 12)  | mA max             | 40                                  | *                                   | N/A                  | **                 |
| V <sub>CC+</sub> = +4.4V to +15.5V (Pins 1 and 9) <sup>5</sup>                             | mA max             | 15                                  | *                                   | N/A                  | **                 |
| V <sub>CC-</sub> = -4.95V to -15.5V (Pins 2 and 10) <sup>5</sup>                           | mA max             | 15                                  | *                                   | N/A                  | **                 |
| V <sub>EE</sub> = -5.2V to ±0.25V (Pin 4)  | mA max             | 40                                  | *                                   | N/A                  | **                 |
| <b>POWER REQUIREMENTS — HTC</b>  |                    |                                     |                                     |                      |                    |
| ±12V to ±18V   | mA max             | N/A                                 | *                                   | 25                   | **                 |
| +5V to ±0.25V  | mA max             | N/A                                 | *                                   | 25                   | **                 |
| Power Supply Rejection Ratio   | mV/V               | N/A                                 | *                                   | 10                   | **                 |
| <b>TEMPERATURE RANGE</b>   |                    |                                     |                                     |                      |                    |
| Operating  | °C                 | 0 to +70                            | -55 to +100 (case)                  | 0 to +70             | -55 to +100 (case) |
| Storage  | °C                 | -55 to +125                         | *                                   | *                    | *                  |

## NOTES:

<sup>1</sup> Sample rates shown are a guide only, and are based on system acquisition times — not logic speed. These rates can be exceeded with acquisition time trade-offs.

<sup>2</sup> Droop rate for case temperatures up to 50°C is 1mV/μs max.

<sup>3</sup> Noise level measured in track mode is 5MHz bandwidth. Noise level increases when high duty cycle repetitive hold command is applied. A 50% duty cycle hold command results in approximately 0.3mV(rms) total noise output.

<sup>4</sup> One ECL-10k Gate, no pulldown resistor.

<sup>5</sup> V<sub>CC+</sub> may be tied to V<sup>+</sup>. V<sub>CC-</sub> may be tied to V<sup>-</sup> or V<sub>EE</sub>.

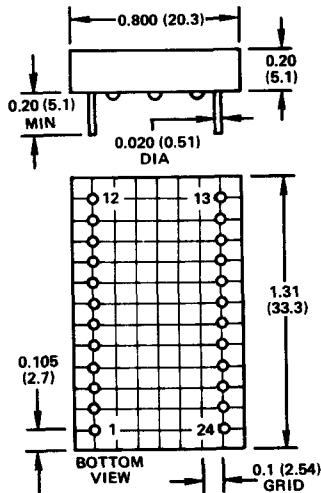
\* Specifications same as model HTS-0025.

\*\* Specifications same as model HTC-0300.

Specifications subject to change without notice.

**HTC-0300 (Only)  
GLASS PACKAGE**

Dimensions shown in inches and (mm)



DOT ON TOP INDICATES POSITION OF PIN 1.

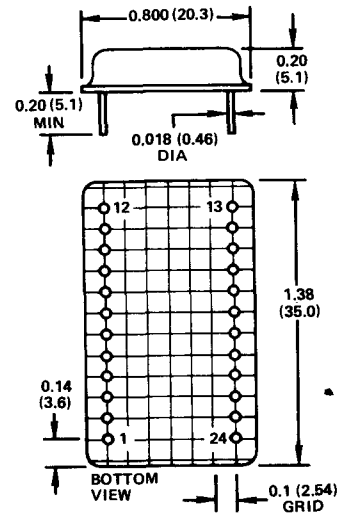
**OUTLINE DIMENSIONS**

**PIN DESIGNATIONS**

| PIN | FUNCTION (HTC-0300) | FUNCTION (HTS-0025)      |
|-----|---------------------|--------------------------|
| 1   | ANALOG OUTPUT       | $V^+$ [+5V to +15.5V]    |
| 2   | N/A                 | $V_{CC}$ [-5V to -15.5V] |
| 3   | N/A                 | $V^-$ [-15V]             |
| 4   | N/A                 | $V_{EE}$ [-5.2V]         |
| 5   | N/A                 | HOLD COMMAND             |
| 6   | N/A                 | GROUND                   |
| 7   | N/A                 | GROUND                   |
| 8   | N/A                 | $V^+$ [+15V]             |
| 9   | +5V                 | $V_{CC}$ [+5V to +15.5V] |
| 10  | GROUND              | $V_{CC}$ [-5V to -15.5V] |
| 11  | HOLD                | GROUND                   |
| 12  | HOLD                | $V^-$ [-15V]             |
| 13  | ANALOG INPUT        | ANALOG INPUT             |
| 15  | INPUT GROUND        | N/A                      |
| 18  | N/A                 | ANALOG GROUND            |
| 19  | N/A                 | ANALOG GROUND            |
| 21  | GROUND              | N/A                      |
| 22  | -15V                | $V^-$ [+15V]             |
| 23  | GROUND              | N/A                      |
| 24  | +15V                | ANALOG OUTPUT            |

**HTS-0025, HTS-0025M, HTC-0300M  
METAL PACKAGE**

Dimensions shown in inches and (mm)



DOT ON TOP INDICATES POSITION OF PIN 1.

**OUTLINE DIMENSIONS**

**TRACK-AND-HOLD (T/H) MODE**

When operated in the T/H mode, these devices are allowed to "track" the input signal for a period of time prior to initiating a "hold command". During the track period, the output follows the input, and the devices function as operational amplifiers. The HTS-0025 operates as a precision follower with a gain of +1, the HTC-0300, -1.

When a Logic "1" is applied to the "hold command" input of the unit, its output is frozen. This output level is held until the track mode is reestablished by a Logic "0" at the hold command input. This operation is shown graphically in Figure 1. The held output level is the voltage value at the input at the instant (plus the aperture time) the hold command is applied.

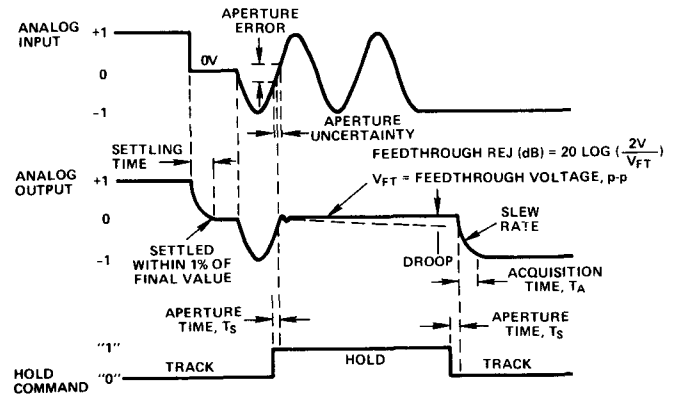


Figure 1b. Track/Hold Waveforms - HTS-0025

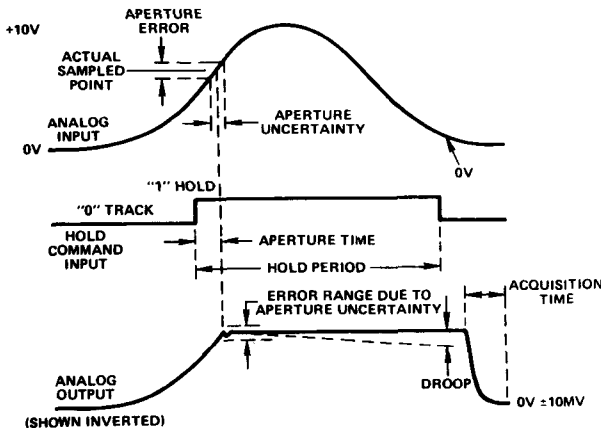


Figure 1a. Track/Hold Waveforms - HTC-0300

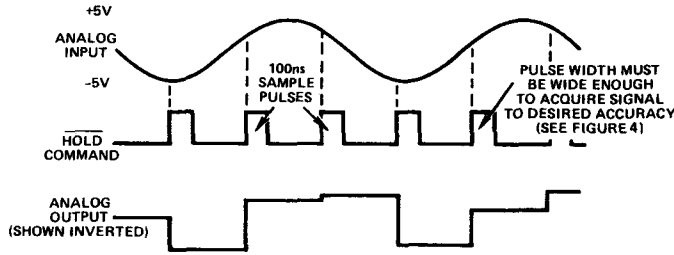
The HTC-0300 provides a hold input for use if the hold command is inverted, that is if the user wishes to use a "0" for the hold condition and a "1" for the track mode. Performance of the unit is identical with either type of input.

Variations in the instants of sampling are called aperture uncertainty. It appears as jitter in the sampling point and can cause significant errors when very high dV/dt inputs are sampled. During the hold period, feedthrough and droop rate can introduce errors at the output. It is important that a track-and-hold have high feedthrough rejection to prevent input-to-output leakage during the hold period. The droop rate is the amount the output changes during the hold period as a result of loading on the internal hold capacitor.

When the hold command input returns to the track condition, the amount of time required for the track-and-hold output to reestablish accurate tracking of the input signal is called the acquisition time.

### SAMPLE-AND-HOLD (S/H) MODE

In the S/H mode of operation, the devices are normally left in the hold condition. A very short sample pulse is applied to the hold command input when a new sample needs to be obtained at the output. The sample pulse width is dictated by the acquisition time. For small sample-to-sample variations, a pulse width as narrow as 20 to 80ns may be used. In general, however, the pulse width should be 100 to 300ns (see Figure 4).



• Figure 2. Sample/Hold Operation – HTC-0300

The HTC-0300 hybrid track-and-hold amplifier has been designed to operate without external trimming potentiometers and “compensation” devices required in most modular units. Active laser trimming is used on the HTC-0300 to “null” the pedestal (the offset during “HOLD” times), set the dc offset to zero, and adjust the gain of the device to unity. Internal frequency compensating elements are incorporated to make the HTC-0300 unconditionally stable and to optimize the frequency response of the internal operational amplifier for this application. Unlike other microcircuit T/H amplifiers, the HTC has a high drive capability ( $\pm 50\text{mA}$ ) and a very low output impedance which allows it to drive directly virtually all types of A/D converters (even the “current-bucking” input types which will produce a degraded A/D conversion without sufficient T/H output drive) and those with low input impedance.

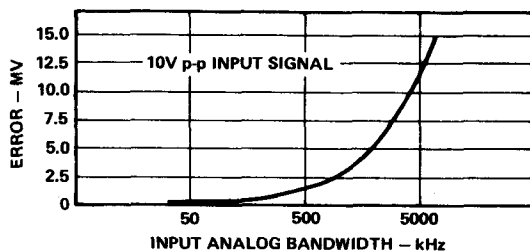


Figure 3. HTC-0300 Error Due to Aperture Uncertainty

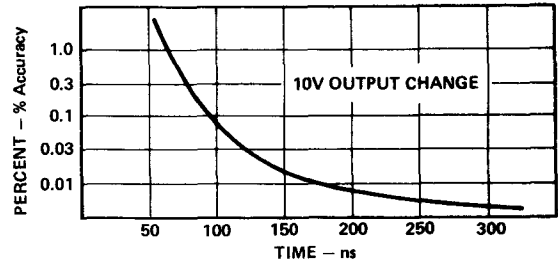


Figure 4a. Settling Accuracy vs. Acquisition Time – HTC-0300

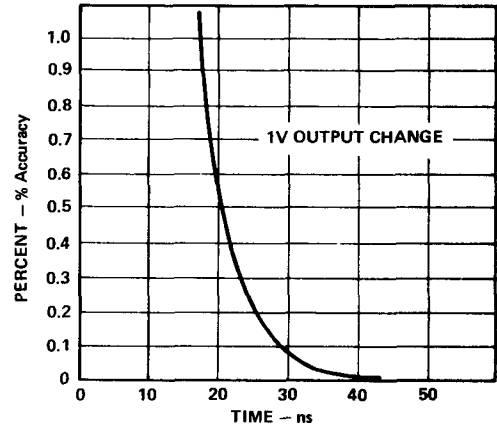


Figure 4b. Settling Accuracy vs. Acquisition Time – HTS-0025

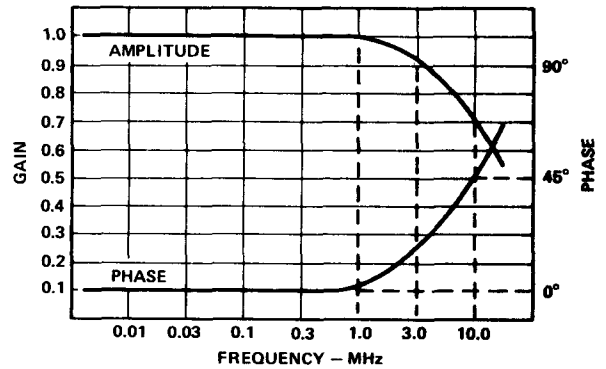


Figure 5. Amplitude and Phase Response – HTC-0300

# Typical HTS-0025 Operation

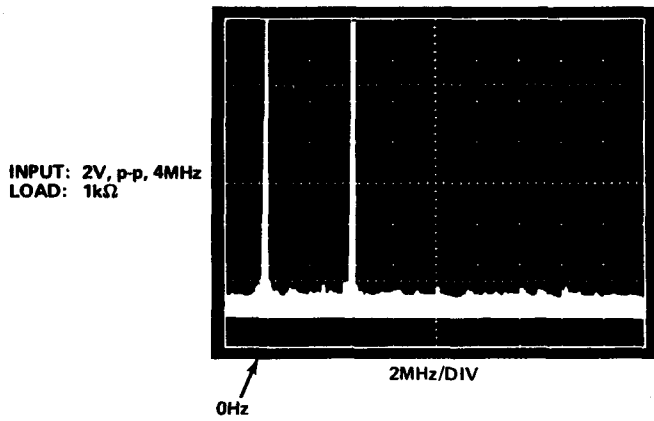


Figure 6a. Harmonic Distortion — Track Mode

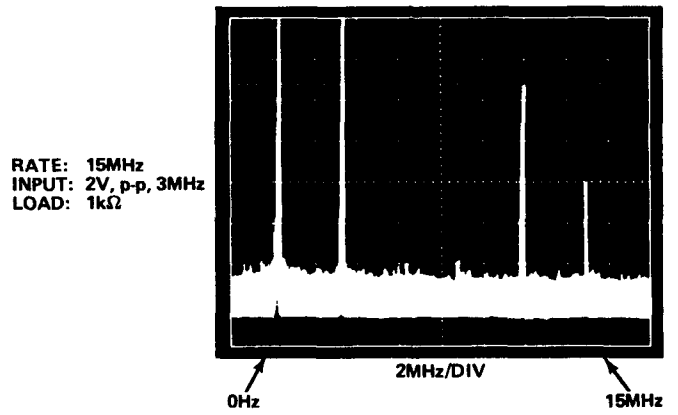


Figure 6b. Frequency Domain Outputs

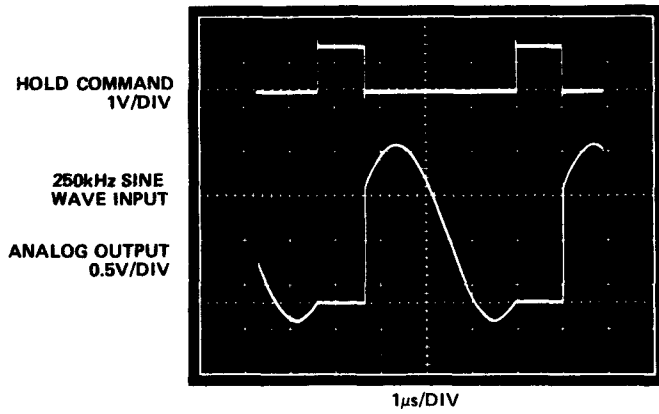


Figure 7a. Track/Hold Operation

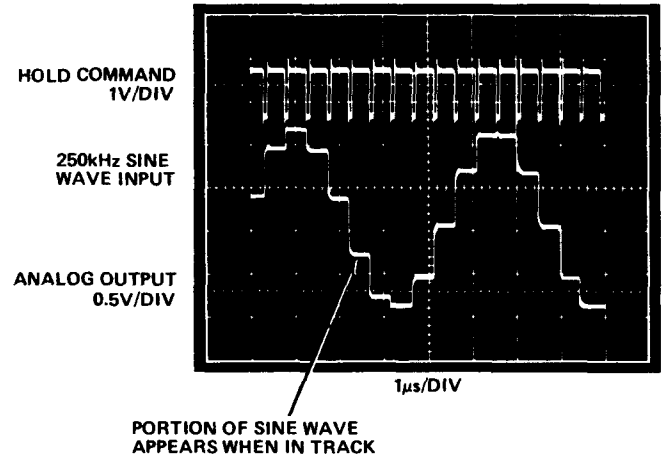


Figure 7b. Sample/Hold Operation

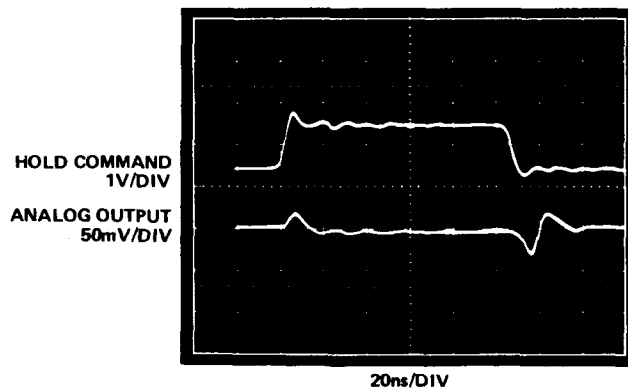


Figure 7c. Expanded View of Output Signal Showing Switching Transients and Pedestal with DC Input

## A/D CONVERSION SYSTEM WITH 300kHz CONTINUOUS SAMPLING RATE AND 12-BIT BINARY OUTPUT

The circuit below illustrates a typical application of the HTC-0300 as a sample/hold amplifier preceding a successive-approximation type of A/D converter. During the conversion interval, the input voltage to the A/D must be held constant. To the extent that this input signal is not absolutely constant, an error results in the digitized output of the A/D. However, with the excellent feedthrough-rejection and droop-rate specifications of the HTC-0300, very little error in the A/D conversion process will be due to the T/H circuit. In addition, the very fast acquisition time of this hybrid microcircuit means that the A/D can be operated at very near its maximum sample rate since very little of the conversion cycle time is required for the T/H to acquire each successive signal sample.

### HTC-0300

|   |                      |
|---|----------------------|
| Sample Rate                             | Approximately 300kHz |
| Encode Command Rate (f clock)           | 3.9MHz               |
| Pulse Width of Monostable Multivibrator | 150ns                |
| Analog Input                            | Digital Output       |
| 0V                                      | 000000000000         |
| +10V                                    | 111111111111         |

Table 1. Performance Parameters For This A/D System

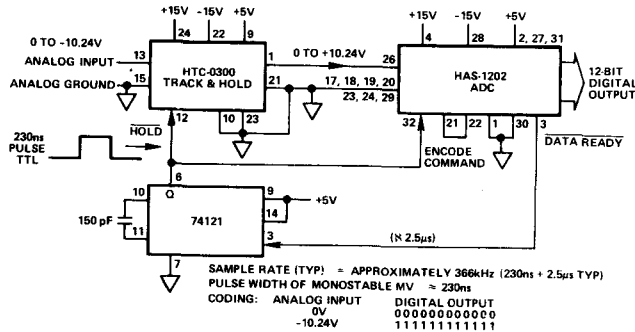


Figure 8. A/D Conversion System

### ORDERING INFORMATION

Order Model Number HTS-0025 or Model Number HTC-0300 for 0 to +70°C operation. For operation from -55°C to +100°C order Model HTS-0025M or HTC-0300M in metal cases. For units processed to MIL-STD-883, consult the factory or the nearest Analog Devices' sales office.

### PRELIMINARY TECHNICAL DATA

#### FEATURES

- ±10V min Input/Output Range
- 50ns Aperture Delay
- 0.5ns Aperture Jitter
- 6μs Settling Time
- 0.01% Max Gain Linearity Error
- Complete with Input Buffer

#### APPLICATIONS

- Track and Hold
- Peak Measurement Systems
- Data Acquisition Systems
- Simultaneous Sample-and-Hold

#### GENERAL DESCRIPTION

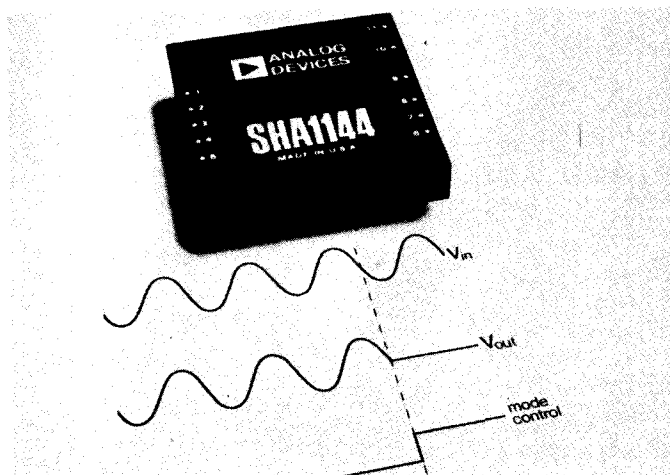
The SHA1144 is a fast sample-and-hold amplifier module with accuracy and dynamic performance appropriate for application with fast 14-bit A/D converters. In the "sample" mode, it acts as a fast amplifier, tracking the input signal. When switched to the "hold" mode, the output is held at a level corresponding to the input signal voltage at the instant of switching. The droop rate in "hold" is appropriate to allow accurate conversion by 14-bit A/D converters having conversion times of up to 150μs.

#### DYNAMIC PERFORMANCE

The SHA1144 was designed to be compatible with fast 14-bit A/D converters such as the Analog Devices' ADC1130 and ADC1131 series, which convert 14 bits in 25μs and 12μs, respectively. Maximum acquisition time of 8μs for the SHA1144 permits high sampling rates for 14-bit conversions. The SHA1144 is guaranteed to have a gain nonlinearity of ±0.001% of full scale to insure 1/2LSB accuracy in 14-bit systems. When in the "hold" mode, the droop rate is 1μV/μs, so the SHA1144 will hold an input signal to ±0.003% of full scale (20V p-p) for over 600μs.

#### PRINCIPLE OF OPERATION

The SHA1144 consists basically of two high speed operational amplifiers, a storage capacitor, and a digitally controlled switch. It differs from typical sample-and-hold modules in one important respect; application versatility. The user completes the SHA1144 feedback circuit external to the module. Therefore, the module may be used in inverting or noninverting configurations and can easily be arranged to provide circuit gain of more than unity, to simplify signal conditioning in a subsystem.



#### FEEDBACK CONNECTIONS

A block diagram of the SHA1144 is shown in Figure 1. The input section acts as a voltage-to-current converter, providing the current needed to charge the "hold" capacitor. The output amplifier isolates the "hold" capacitor and provides low output impedance for driving the load. Since feedback is not hard-wired in the module, both inverting and noninverting input terminals are available, and the SHA1144 can be connected as a follower with unity gain or potentiometric gain, as well as inverter or even a differential amplifier. Since the unity gain follower mode will be the most frequent application, performance data listed in the specification table is based on this operating mode.

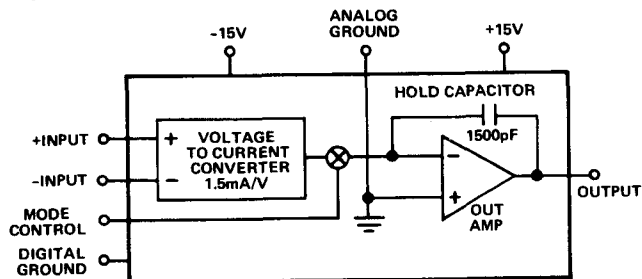
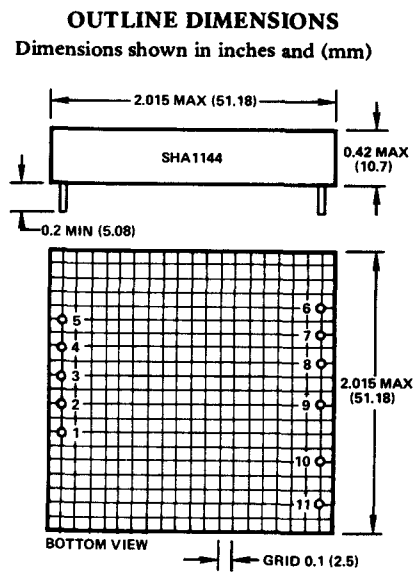


Figure 1. Block Diagram



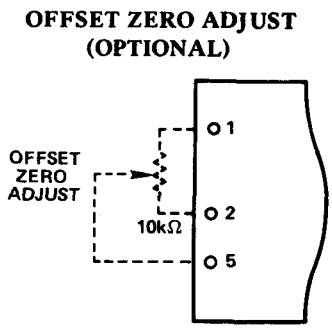
# SPECIFICATIONS (typical @ +25°C gain = 1V/V, and nominal supply voltages unless otherwise noted)

|   |  |               |
|---|--|---------------|
| <b>MODEL</b>                              | <b>SHA1144</b>                             |               |
| <b>ACCURACY</b>                           |  |               |
| Gain                                      | +1V/V                                      |               |
| Gain Error                                | ±0.005%                                    |               |
| Gain Nonlinearity                         | ±0.0005% (±0.001% max)                     |               |
| Gain Temperature Coefficient (0 to +70°C) | ±1ppm/°C (±2ppm/°C max)                    |               |
| <b>INPUT CHARACTERISTICS</b>              |  |               |
| Input Voltage Range                       | ±10V                                       |               |
| Impedance                                 | 10 <sup>11</sup> Ω    10pF                 |               |
| Bias Current                              | 0.5nA max                                  |               |
| Initial Offset Voltage                    | Adjustable to Zero                         |               |
| Offset vs. Temperature (0 to +70°C)       | ±30μV/°C max                               |               |
| <b>OUTPUT CHARACTERISTICS</b>             |  |               |
| Voltage                                   | ±10V min                                   |               |
| Current                                   | ±5mA min                                   |               |
| Resistance                                | <1Ω  |               |
| Capacitive load                           | 350pF                                      |               |
| Noise @ 100kHz Bandwidth                  | 70μV p-p                                   |               |
| @ 1MHz Bandwidth                          | 175μV p-p                                  |               |
| <b>SAMPLE MODE DYNAMICS</b>               |  |               |
| Frequency Response                        |  |               |
| Small Signal (-3dB)                       | 1MHz                                       |               |
| Full Power                                | 50kHz                                      |               |
| Slew Rate                                 | 3V/μs                                      |               |
| <b>SAMPLE-TO-HOLD SWITCHING</b>           |  |               |
| Aperture Delay Time                       | 50ns                                       |               |
| Aperture Uncertainty                      | 0.5ns                                      |               |
| Offset Step                               | 1mV  |               |
| Offset Nonlinearity                       | 160μV                                      |               |
| Switching Transient                       |  |               |
| Amplitude                                 | 50mV                                       |               |
| Settling Time to ±0.003%                  | 1μs  |               |
| <b>HOLD MODE DYNAMICS</b>                 |  |               |
| Droop Rate                                | 1μV/μs (2μV/μs max)                        |               |
| Variation with Temperature                | double every 10°C                          |               |
| Feedthrough (for 20V p-p Input @ 1kHz)    | -80dB                                      |               |
| <b>HOLD-TO-SAMPLE SWITCHING</b>           |  |               |
| Acquisition Time to ±0.003%               | (20V Step)                                 | 6μs (8μs max) |
|   | (10V Step)                                 | 5μs           |
| ±0.01%                                    | (20V Step)                                 | 5μs           |
|   | (10V Step)                                 | 4μs           |
| <b>DIGITAL INPUT</b>                      |  |               |
| Sample Mode (Logic "1")                   | +2V < Logic "1" < +5.5V<br>@ 15nA max      |               |
| Hold Mode (Logic "0")                     | 0V < Logic "0" < +0.8V<br>@ 5μA (20μA max) |               |
| <b>POWER REQUIRED</b>                     |  |               |
|   | +15V ±3% @ 60mA                            |               |
|   | -15V ±3% @ 45mA                            |               |
| <b>TEMPERATURE RANGE</b>                  |  |               |
| Operating                                 | 0 to +70°C                                 |               |
| Storage                                   | -55 to +85°C                               |               |



- NOTES:**
1. Pins: 0.019 ±0.001 (0.48mm ±0.02mm) dia. half-hard brass, gold plated per MIL-G-45204B, Class 1, Type II.

- PIN DESIGNATIONS**
- |           |                    |
|-----------|--------------------|
| 1. TRIM   | 7. ANALOG GROUND   |
| 2. TRIM   | 8. -15V            |
| 3. +INPUT | 9. ANALOG OUTPUT   |
| 4. -INPUT | 10. MODE CONTROL   |
| 5. TRIM   | 11. DIGITAL GROUND |
| 6. +15V   |                    |



Specifications subject to change without notice.

Figure 2 shows feedback connections to the SHA1144 for the unity gain follower mode. Output (pin 9) is connected to input (pin 4). Input signal is applied to pin 3.

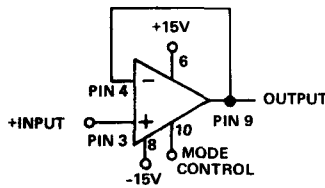


Figure 2. Unity Gain Follower

Figure 3 shows feedback connections for noninverting operation with potentiometric gain. When the indicated values are installed, gain will be +5. As in all operational amplifiers, gain-bandwidth product is a constant for a given sample-and-hold. Effective 3dB bandwidth will be inversely proportional to gain.

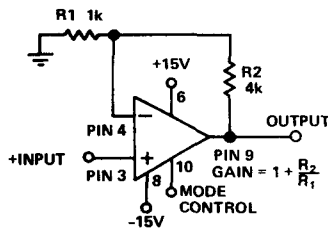


Figure 3. Noninverting Operation

By using conventional operational amplifier feedback connections, the SHA1144 can be connected for use as an inverter, with various gains (as determined by the  $R_F/R_1$  ratio), or as a differential amplifier.

### DATA ACQUISITION APPLICATION

Successive-approximation A/D converters can generate substantial linearity errors if the analog input varies during the period of conversion; even the fast 14-bit models available cannot tolerate input signal frequencies of greater than a few Hz. For this reason, sample-and-hold amplifiers like the SHA1144 are connected between the A/D and its signal source to hold the analog input constant during conversion.

When the SHA1144 is connected to an A/D, its aperture time uncertainty, rather than the A/D's conversion time, is the factor which limits the allowable input signal frequency. The SHA1144, with a typical aperture delay time of 50ns and an uncertainty of 0.5ns, will change from the sample mode to the hold mode 50 to 50.5ns after the "1" to "0" transition of the mode control input. If the system timing is so arranged as to initiate the mode control signal 50ns early, then switching will actually occur within 0.5ns of the desired time as shown below.

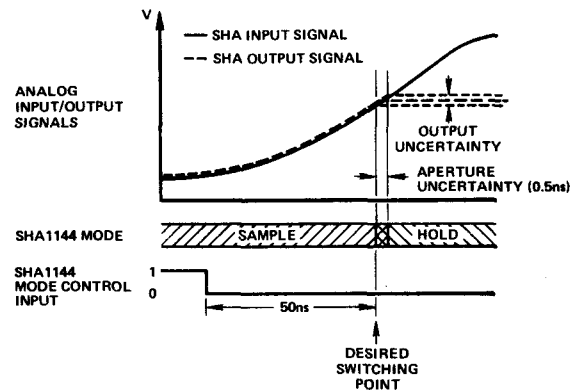


Figure 4. Aperture Uncertainty

The maximum allowable slew rate will thus equal the quotient of the maximum allowable voltage uncertainty and the 0.5ns aperture uncertainty. For sinewave inputs, the corresponding maximum frequency is expressed by:

$$f_{\max} = \left( \frac{\Delta E}{E_{FS}} \right) \left( \frac{1}{2\pi\Delta t} \right) \cong 3.18 \times 10^8 \left( \frac{\Delta E}{E_{FS}} \right)$$

where:  $\Delta E$  = the allowable voltage uncertainty  
 $E_{FS}$  = the sinewave magnitude

For a system containing a SHA1144 and a 14-bit A/D with  $\pm 10V$  input signals and an allowable input uncertainty of  $\pm 1/2LSB$  ( $\pm 620\mu V$ ), the maximum allowable signal frequency will be 19.7kHz.

### POWER SUPPLY AND GROUNDING CONNECTIONS

The proper power supply and grounding connections are shown below in Figure 5.

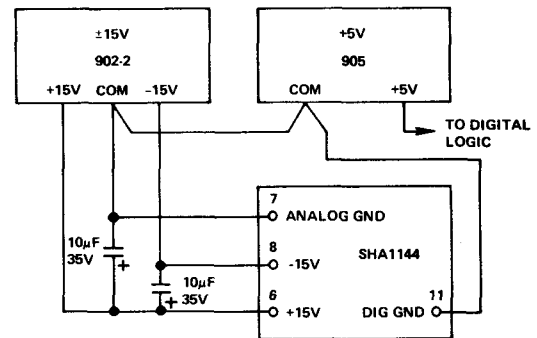


Figure 5. Power Supply and Grounding Connections

The  $\pm 15V$  power supplies must be externally bypassed as shown. The capacitors should be tantalum types and should be installed as close to the module pins as possible. The analog and digital ground lines should be run separately to their respective power supply commons to prevent coupling of digital switching noise to the sensitive analog circuit section.

## OPERATION WITH AN A/D CONVERTER

Figure 6 below shows the appropriate connections between the SHA1144 and a successive approximation A/D converter in block diagram form.

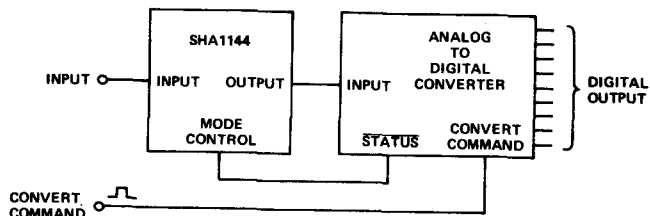


Figure 6. SHA1144 and A/D Connections

The resulting timing sequence at the start of conversion is illustrated in Figure 7.

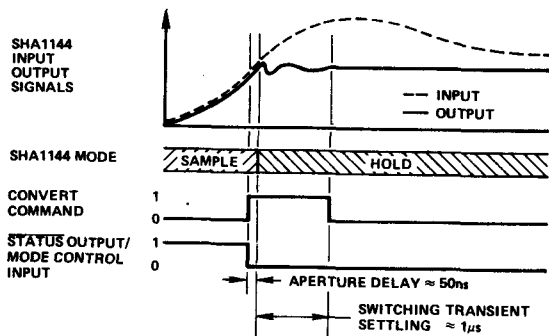


Figure 7. A/D and SHA Timing at Start of Conversion

Note that the leading edge of the convert command pulse causes the converter's STATUS output to go to Logic "0" which in turn switches the SHA1144 from sample to hold. As discussed previously, the typical SHA1144 actually changes modes 50 to 50.5ns after the "1" to "0" transition of the mode control input. This mode switching causes a transient on the output terminal which decays to within 0.003% of the final value in approximately 1µs. Once the transient has settled, the convert command input is returned to Logic "0" and the conversion proceeds. As shown in Figure 8, the STATUS signal returns to Logic "1" and the SHA1144 returns to the sample mode at the end of conversion. Within 6µs, it will have acquired the input signal to 0.003% accuracy and a new conversion cycle may be started.

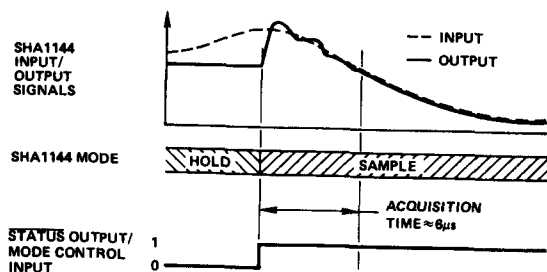


Figure 8. A/D and SHA Timing at End of Conversion

## OPERATION WITH AN A/D AND MULTIPLEXER

The subsystem of Figure 9 may also be connected to a multiplexer like the Harris HI508A as shown below.

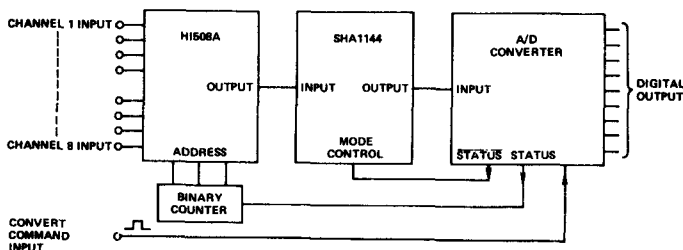


Figure 9. A/D, SHA, and MPX Connections

The leading edge of the convert command pulse sets the STATUS output to Logic "0" thereby switching the SHA1144 to "hold"; the corresponding change to Logic "1" of the STATUS output increments the binary counter and changes the multiplexer address. Since the SHA1144's aperture time is small with respect to the multiplexer switching time, it will have switched to the hold mode before the multiplexer actually changes channels. The multiplexer switching transients will settle out long before the SHA returns to "sample" at the end of conversion. The timing sequence described above is illustrated in Figure 10.

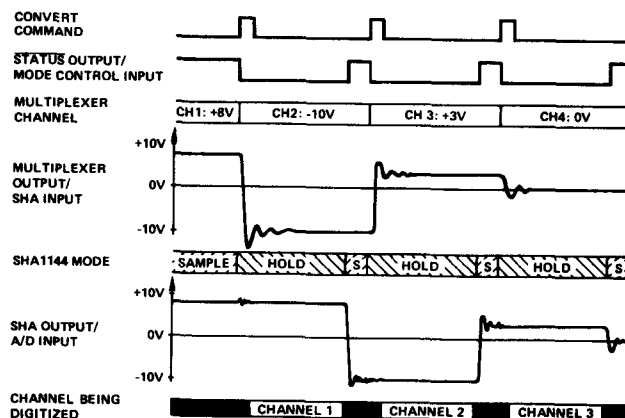


Figure 10. A/D, SHA, and MPX Timing

This method of sequencing the multiplexer may be altered to permit random addressing or addressing in a preset pattern. The timing of the multiplexer address changes may also be altered but consideration should be given to the effects of feedthrough in the SHA1144. Feedthrough is the coupling of analog input signals to the output terminal while the SHA is in "hold". Large multiplexer switching transients occurring during A/D conversion may introduce an error.

## GENERAL DESCRIPTION

High resolution, high speed data acquisition demands that considerable thought be given to wiring connections, even when simply evaluating the unit in a temporary laboratory bench set-up. To assist with such evaluations, an AC1580 is available. This 4 1/2" X 6" printed circuit card has sockets that allow a SHA1144 and ADC1130 or ADC1131 to be plugged directly onto it. It also has provisions for two optional Harris HI508A multiplexers. This card includes gain and offset adjustment potentiometers and power supply bypass capacitors. It mates with a Cinch 251-22-30-160 (or equivalent) edge connector (P1) and Cinch 251-06-30-160 (or equivalent) edge connector (P2) which are supplied with every card.

To use the AC1580, program as shown in the wiring chart of Table 1, by installing the appropriate jumpers. An outline drawing and schematic are provided for reference.

### Calibration Procedure

Set up the SHA1144 for the desired gain per the wiring chart of Table 1. Short W9 which drives the SHA MODE CONTROL with the STATUS of the ADC. Calibrate offset and gain in the manner described below. When calibration is completed W9

may be removed and the SHA MODE CONTROL may be driven in accordance with the option chart.

### Offset Calibration

For the 0 to +10V unipolar range set the input voltage precisely to +0.0003V. Adjust the zero potentiometer until the converter is just on the verge of switching from 00 . . . . 0 to 00 . . . . 1.

For the +5V bipolar range, set the input voltage precisely to -4.9997V; for ±10V units set it to -9.9994V. Adjust the zero potentiometer until offset binary coded units are just on the verge of switching from 00 . . . . 0 to 00 . . . . 1 and two's complement coded units are just on the verge of switching from 100 . . . 0 to 100 . . . . 1.

### Gain Calibration

Set the input voltage precisely to +9.9991V for 0 to +10V units, +4.9991V for ±5V units or +9.9982V for ±10V units. Note that these values are 1 1/2LSB's less than the nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11 . . . 0 to 11 . . . 1 and two's complement coded units are just on the verge of switching from 011 . . . 10 to 011 . . . 11.

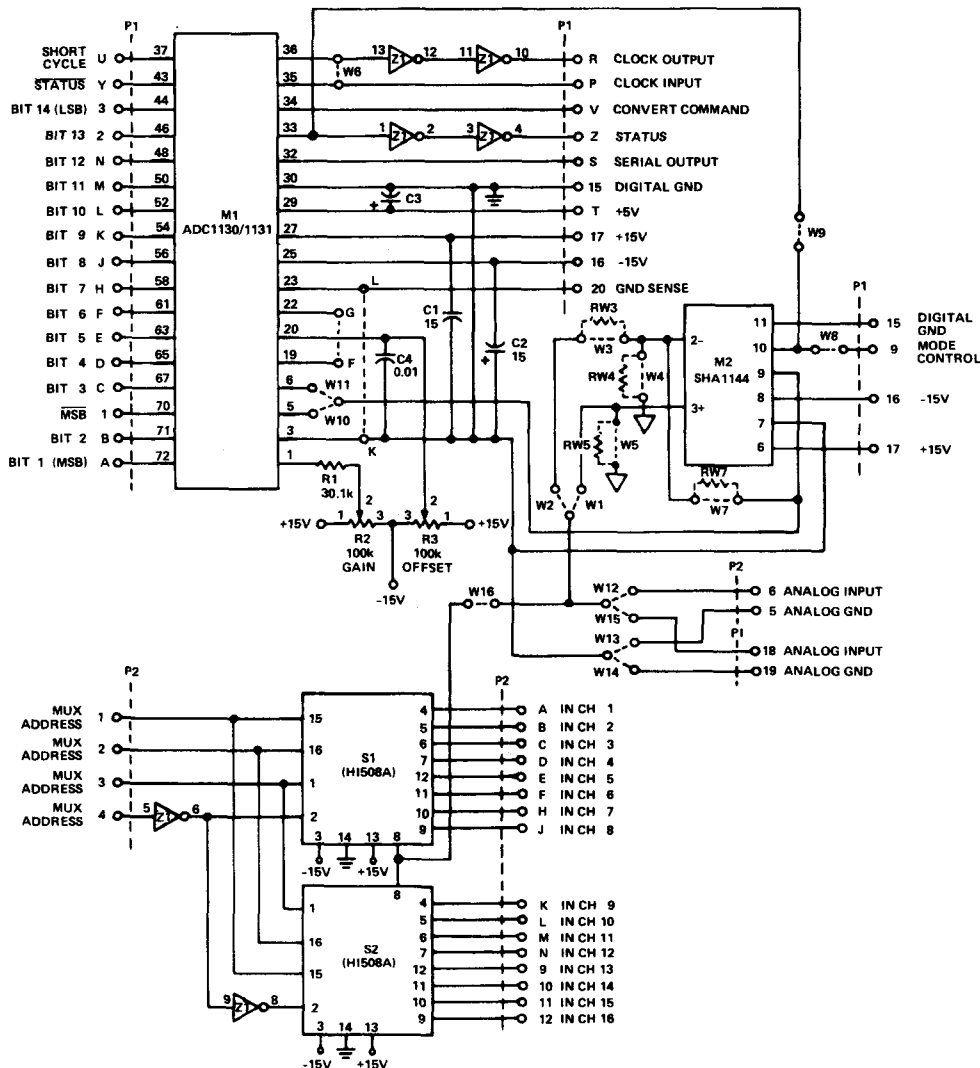
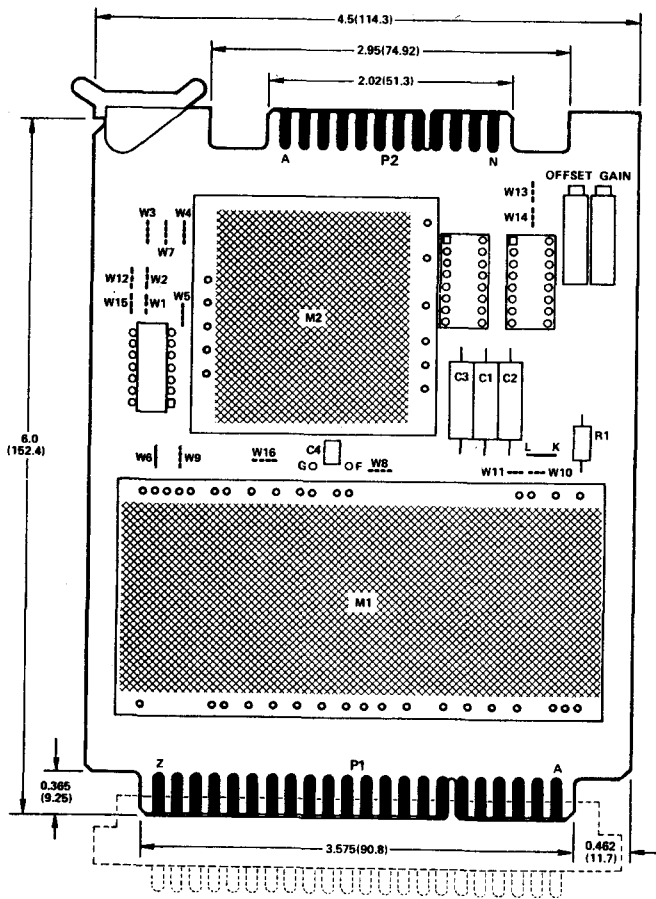


Figure 11. Schematic and Pin Designations

**OUTLINE DIMENSIONS**  
Dimensions shown in inches and (mm).



NOTES  
1. P1 IS CINCH CONNECTOR TYPE 251-22-30-180.  
2. P2 IS CINCH CONNECTOR TYPE 251-06-30-180.

Figure 12. AC1580 Mounting Board

**A to D Converter Options**

| Range     | Jumpers                               |
|-----------|---------------------------------------|
| 0V to 10V | Jumper W11                            |
| ±5V       | Jumper W11 and Jumper G to F on Board |
| ±10V      | Jumper W10 and Jumper G to F on Board |

**SHA Options**

|                                   |   |
|-----------------------------------|---|
| SHA Unity Gain (+1)               | Jumper W1 and Jumper W7   |
| SHA with Gain <sup>1,3</sup>      | Jumper W1 and Install RW4 and RW7 in W4 and W7 Locations <sup>3</sup>               |
| SHA as an Inverter <sup>2,3</sup> | Jumper W2 and Jumper W5 and Install RW3 and RW7 in W3 and W7 Locations <sup>3</sup> |

**SHA Mode Control**

|  |           |
|--|-----------|
| Internal<br>(Driven from Status of the ADC)                  | Jumper W9 |
| External<br>(Apply External Signal to Pin 9 of Connector P1) | Jumper W8 |

**Multiplexer Option**

When Using Multiplexers Jumper W16

**INPUT OPTIONS**

| Inputs        | From Connector P1 | From Connector P2 |
|---------------|-------------------|-------------------|
| Analog Input  | Jumper W15        | Jumper W12        |
| Analog Ground | Jumper W14        | Jumper W13        |

**NOTES**

$${}^1G = 1 + \frac{RW7}{RW4} \quad {}^2G = -\frac{RW7}{RW3}$$

<sup>3</sup> See Figure 11 for appropriate gain setting resistor locations (RW3, RW4, RW7)

Table 1. Option Chart

| "ON" Channel | 1 | 2 | 3 | 4 |  |
|--------------|---|---|---|---|--|
| 1            | L | L | L | L | L = TTL Logic "0"<br>(0V ≤ "0" ≤ +0.8V)  |
| 2            | L | L | H | L |  |
| 3            | L | H | L | L | H = TTL Logic "1"<br>(+2V ≤ "1" ≤ +5.5V) |
| 4            | L | H | H | L |  |
| 5            | H | L | L | L |  |
| 6            | H | L | H | L |  |
| 7            | H | H | L | L |  |
| 8            | H | H | H | L |  |
| 9            | L | L | L | H |  |
| 10           | L | L | H | H |  |
| 11           | L | H | L | H |  |
| 12           | L | H | H | H |  |
| 13           | H | L | L | H |  |
| 14           | H | L | H | H |  |
| 15           | H | H | L | H |  |
| 16           | H | H | H | H |  |

Table 2. Multiplexer Address

### FEATURES

20ps Aperture Uncertainty (THS)  
15 to 1000ns Acquisition Times  
0.01% Linearity  
DC Coupled High Input Z Buffer

### APPLICATIONS

Data Acquisition Systems  
Data Distribution Systems  
Peak Measurement Systems  
Simultaneous Sample & Hold  
Analog Delay & Storage



### GENERAL DESCRIPTION

The THS/THC series' modules include the fastest sample/track-and-hold amplifier (SHA) available (THS-0025), as well as general purpose high speed low droop rate, low feedthrough devices such as the THC-1500. The six devices in the series allow a wide range of trade-offs between speed, price, droop rate, output noise levels, gain precision and offset drift. All devices feature high input impedance buffer amplifiers and high output current amplifiers (50mA). The THS units achieve their speed through the use of a dc-coupled Schottky diode sampling bridge while the THC series use MOS FET switches. TTL, or ECL logic can be used on any THC device, and either is available as a no cost option on THS units.

### APPLICATIONS

The most common use for a track and hold is to place it ahead of an A/D converter to allow the digitizing of signals with bandwidths higher than the digitizer alone can handle. The use of the THS series track and holds can allow a reduction of system aperture to 20ps while THC units provide 100ps. These track and holds may also be used for peak holding functions, simultaneous sampling A/D's (with appropriate analog multiplexing), and other high speed analog signal processing applications. These modules have been used to construct 13-bit A/D converters with word rates as high as 10MHz. The THS/THC series is designed to operate in either the track-and-hold or sample-and-hold modes. They perform well with the MAS series' A/D converters.

### TRACK-AND-HOLD (T/H) MODE

When a THS/THC unit is operated in the T/H mode, it is allowed to "track" the input signal for a period of time prior to initiating a "hold command". During the track period, the output follows the input, and the device functions like an amplifier. In the THC units a resistor gain programmable op amp provides this function.

When a Logic "1" is input to the "hold command" input of the T/H, its output is frozen. This output level is held until the track mode is reestablished by a Logic "0" at the "hold command" input. This operation is shown graphically in Figure 1. The held output level is the voltage value at the input at the instant the hold command is applied, plus the aperture time.

Variations in the instants of sampling are called aperture uncertainty. It appears as jitter in the sampling point and can cause significant errors when very high dV/dt inputs are sampled.

During the hold period, feedthrough and droop rate can introduce errors at the output. It is important that a track and hold have high feedthrough rejection to prevent input to output leakage during the hold period. The droop rate is the amount the output changes during the hold period, as a result of loading on the internal hold capacitor.

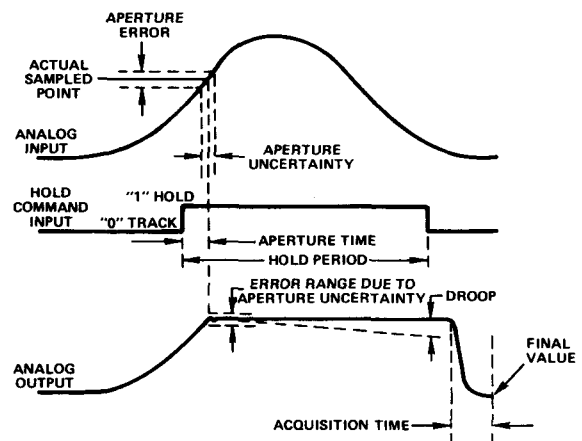


Figure 1. Track-and-Hold Operation

# SPECIFICATIONS (typical at 25°C and nominal supply voltages)

| MODEL   | UNITS    | FAST THS SERIES                           |          |          | ULTRA FAST THS SERIES                           |          |          |
|---|----------|---|----------|----------|---|----------|----------|
|   |          | THC-0300                                  | THC-0750 | THC-1500 | THS-0025  | THS-0060 | THS-0225 |
| <b>DYNAMIC CHARACTERISTICS</b>                                      |          |   |          |          |   |          |          |
| Acquisition Time (to 0.1%)  | ns       | 100                                       | 300      | 1000     | 25  | 75       | 300      |
| Sample Rate (max) <sup>1</sup>                                      | MHz      | 5   | 2.5      | 1        | 30  | 15       | 3.5      |
| Aperture Time TTL   | ns       | 18  | *        | *        | 10  | **       | **       |
| ECL   | ns       | 8   | *        | *        | 6   | **       | **       |
| Settling Time THC to 0.1%, THS to 1%<br>(See Figure 2)              | ns       | 80  | 250      | 900      | 15  | 50       | 200      |
| Bandwidth (Small Signal 3dB)  | MHz      | 12  | 4        | 1.2      | 60  | 20       | 5        |
| Slew Rate   | V/μs     | 300                                       | 100      | 30       | 300   | 100      | 25       |
| Aperture Uncertainty  | ps max   | 100                                       | *        | *        | 20  | **       | **       |
| Harmonic Distortion, 500kHz THC, 5MHz THS                           | dB       | 68  | *        | *        | *   | *        | *        |
| Feedthrough Rejection (dc to max Sample Rate/2)<br>(dc to 5MHz THS) | dB       | 63  | 70       | 80       | 65  | 75       | 80       |
| Droop Rate  | μV/μs    | 12  | 5        | 2        | 5000  | 500      | 100      |
| <b>ACCURACY/STABILITY DC</b>  |          |   |          |          |   |          |          |
| Gain  | V/V      | -1 ±2% (Pin 6 to Pin 15)                  |          |          | 0.975   | **       | **       |
| Gain vs. Temperature  | ppm/°C   | 10  | *        | *        | 5   | **       | **       |
| Zero Offset Voltage   |          | Adjustable to Zero                        |          |          | Adjustable to Zero                              |          |          |
| Offset vs. Temperature  | ppm/°C   | 10  | *        | *        | 30  | **       | **       |
| Linearity   | %        | ±0.01                                     | *        | *        | *   | *        | *        |
| <b>INPUT</b>  |          |   |          |          |   |          |          |
| Voltage   | V max    | ±10                                       | *        | *        | ±2  | **       | **       |
| Impedance   | Ω        | 1000                                      | *        | *        | 1M  | **       | **       |
| Bias Current  | nA       | 0.05                                      | *        | *        | *   | *        | *        |
| <b>OUTPUT</b>   |          |   |          |          |   |          |          |
| Voltage   | V max    | ±10                                       | *        | *        | ±2 (No Load)                                    | **       | **       |
| Current   | mA       | ±50                                       | *        | *        | *   | *        | *        |
| Impedance   |          | Less than 0.01Ω @ dc                      |          |          | 5Ω (Output 1, Pin 21)<br>75Ω (Output 2, Pin 22) |          |          |
| Noise (dc to 15MHz THS) (dc to 2.5MHz THC)                          | μV rms   | 100                                       | 50       | 50       | 200   | 100      | 50       |
| <b>HOLD COMMAND (DIGITAL INPUTS)</b>                                |          |   |          |          |   |          |          |
| TTL Single Line Input (2 Std. TTL Loads)                            |          |   |          |          | (TTL or ECL Purchased as no cost Options)       |          |          |
| "0" = Sample/Track  |          | 0 to +0.4V                                | *        | *        | *   | *        | *        |
| "1" = Hold  |          | +2.4 to +5V                               | *        | *        | *   | *        | *        |
| ECL   |          | Single Line Input <sup>2</sup>            |          |          | Two Line Complementary <sup>3</sup>             |          |          |
| "0" = Sample/Track  | V        | -1.7                                      | *        | *        | *   | *        | *        |
| "1" = Hold  | V        | -0.8                                      | *        | *        | *   | *        | *        |
| <b>POWER REQUIREMENTS</b>   |          |   |          |          |   |          |          |
| +15V ±5% (THC) +12V to +15V (THS)                                   | mA max   | 90  | *        | *        | 100   | **       | **       |
| -15V ±5% (THC) -12V to -15V (THS)                                   | mA max   | 80  | *        | *        | 100   | **       | **       |
| +5V ±5% (THS) TTL Option  | mA max   | N/A                                       | *        | *        | 20  | **       | **       |
| -5.2V ±5% (THS) ECL Option  | mA max   | N/A                                       | *        | *        | 80  | **       | **       |
| -5.2V ±5% (THS) ECL Option  | mA max   | N/A                                       | *        | *        | 24  | **       | **       |
| Power Supply Rejection Ratio ±15V                                   | mV/V max | 10  | *        | *        | 20  | **       | **       |
| <b>TEMPERATURE RANGE</b>  |          |   |          |          |   |          |          |
| Operating   | °C       | 0 to +70                                  | *        | *        | *   | *        | *        |
| Storage   | °C       | -55 to +125                               | *        | *        | *   | *        | *        |
| <b>PHYSICAL CHARACTERISTICS</b>                                     |          |   |          |          |   |          |          |
| Case  |          | diallyl phthalate per MIL-M-14 type SDG-F |          |          | diallyl phthalate per MIL-M-14 type SDG-F       |          |          |

**NOTES:**

<sup>1</sup> Sample rates shown are a guide only and are based on system acquisition times—not logic speed. These rates can be exceeded with acquisition time trade-offs.

<sup>2</sup> These inputs are unterminated. An external pull down resistor should be used when driven by ECL 10k logic source.

<sup>3</sup> These inputs are each terminated with a 330Ω pull down resistor to -5.2V.

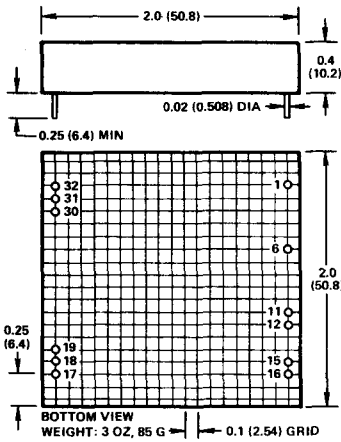
\* Specifications same as THC-0300.

\*\* Specifications same as THS-0025.

Specifications subject to change without notice.

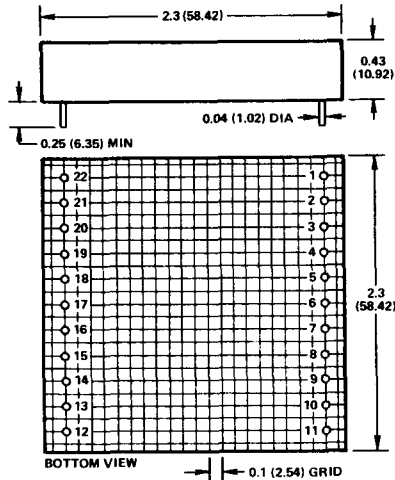
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES: SOME MODELS DO NOT USE ALL PIN OUTS. IN THESE CASES, UNUSED PINS ARE DELETED. PINS ARE GOLD PLATED. DOT ON TOP INDICATES POSITION OF PIN 1.

**THC Series**



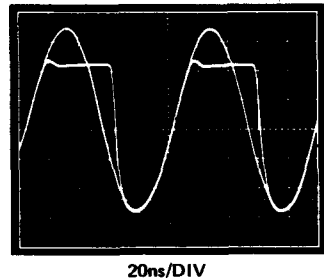
NOTES: SOME MODELS DO NOT USE ALL PIN OUTS. IN THESE CASES, UNUSED PINS ARE DELETED. PINS ARE GOLD PLATED. DOT ON TOP INDICATES POSITION OF PIN 1.

**THS Series**

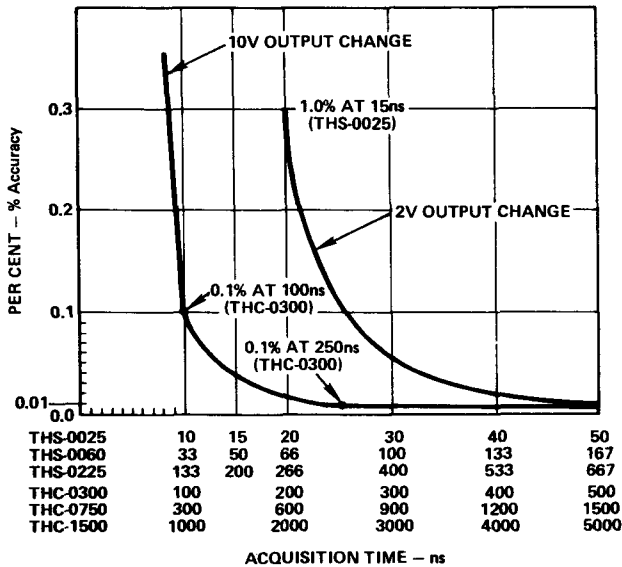
## PIN DESIGNATIONS

| PIN | THC SERIES' FUNCTION | THS SERIES' FUNCTION |
|-----|----------------------|----------------------|
| 1   | ANALOG INPUT         | GROUND               |
| 4   | N/A                  | +15V                 |
| 5   | N/A                  | GROUND               |
| 6   | FEEDBACK             | -15V                 |
| 7   | N/A                  | HOLD COMMAND (ECL)   |
| 8   | N/A                  | HOLD COMMAND (ECL)   |
| 9   | N/A                  | HOLD COMMAND (TTL)   |
| 10  | N/A                  | -5.2V                |
| 11  | OFFSET ADJUST        | +5V                  |
| 12  | OFFSET ADJUST        | GROUND               |
| 13  | N/A                  | OFFSET ADJUST        |
| 14  | N/A                  | ANALOG INPUT 1       |
| 15  | UNITY GAIN           | N/A                  |
| 16  | ANALOG OUTPUT        | GROUND               |
| 17  | GROUND               | N/A                  |
| 18  | -15V                 | N/A                  |
| 19  | +15V                 | N/A                  |
| 20  | N/A                  | GROUND               |
| 21  | N/A                  | ANALOG OUTPUT 1      |
| 22  | N/A                  | ANALOG OUTPUT 2      |
| 30  | HOLD COMMAND (ECL)   | N/A                  |
| 31  | HOLD COMMAND (TTL)   | N/A                  |
| 32  | GROUND               | N/A                  |

When the hold command input returns to the track condition, the amount of time required for the T/H output to reestablish accurate tracking of the input signal is called the acquisition time. Figure 2 shows settling accuracy versus acquisition time for the THS/THC series. Figure 3 shows superimposed photographs of the input and output waveforms of a THS-0025 operated as a track-and-hold amplifier. Note that the output reacquires the input just 12ns after the end of the hold time.



**Figure 3. Track-and-Hold Operation (THS-0025)**

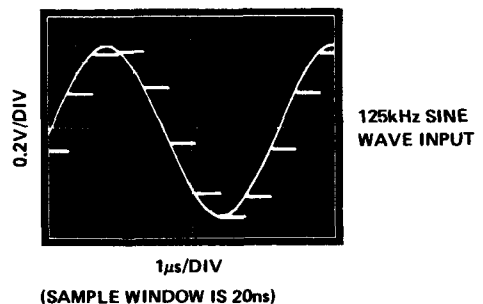


**Figure 2. Acquisition Time vs. Settling Accuracy**

### SAMPLE AND HOLD (S/H) MODE

In the S/H mode of operation, devices are normally left in the hold condition. A very short sample pulse is applied to the hold command input when a new sample needs to be obtained at the output. The sample pulse width is dictated by the acquisition time. For small sample-to-sample variations, a pulse width as narrow as 12ns may be used for THS units and 80ns for THC units. If possible for greater accuracy, sample pulses should be wider (see Figure 2).

In general, however, the pulse width should be 15ns to 50ns, depending on required accuracy. Figure 4 shows the input and output waveforms of a THS-0025 used in the S/H mode.



**Figure 4. Sample-and-Hold Operation (THS-0025)**



**APPLICATION NOTES**

Figure 5 shows a slope sensitive circuit which is capable of finding the peaks of positive excursions of an input waveform and digitizing the result. The circuit may be implemented without the A/D converter, in which case the output is an analog level held by the T/H module that may be observed or measured in some other manner.

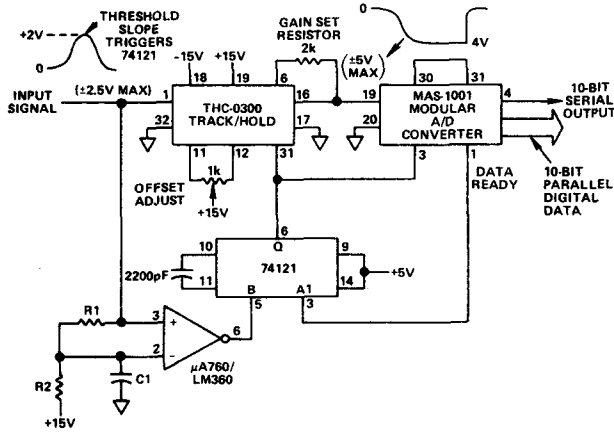


Figure 5. Peak Detector (THC-0300)

The comparator triggers the T/H module when the positive slope of the input signal drops below a threshold slope equal to  $15V/R2C1$ . A minimum positive slope of  $15V/R1C1$  is required to arm the detector. Resistors R1 and R2 are used to provide a guard band to prevent noise from triggering the circuit. The guardband voltage is equal to  $15V \times R1/R2$  and is generally set to approximately 5 to 20mV.

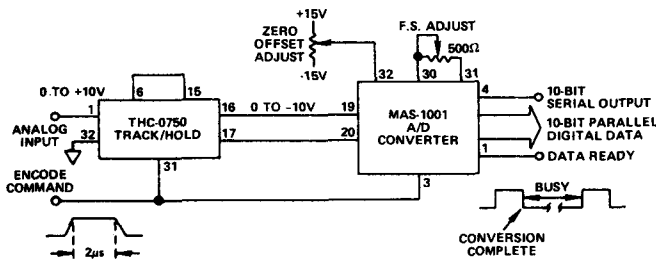


Figure 6. A/D Conversion System (THC)

|                      |                           |
|----------------------|---------------------------|
| Throughput Rate      | Greater than 400kHz       |
| Overall Accuracy     | 0.05%                     |
| Resolution           | One Part in 1024 (10 Bit) |
| Aperture Uncertainty | 100ps                     |

**Analog Input                      Digital Output**

|         |                     |
|---------|---------------------|
| 0V      | 0 0 0 0 0 0 0 0 0 0 |
| +5.000V | 1 0 0 0 0 0 0 0 0 0 |
| +9.990V | 1 1 1 1 1 1 1 1 1 1 |

Table 1. Capsule Performance for the A/D System

Analog Devices' THC series track-and-holds are designed to interface directly with the MAS series A/D converters as well as other commercially available modular A/D's. In the above application, the THC module is used to acquire the analog signal to be converted and hold the sampled output over a much longer time period to permit the A/D module to accurately encode the analog data sample. In this way, the system aperture time is reduced to less than 100ps, and analog bandwidths up to the Nyquist limit may be accurately digitized.

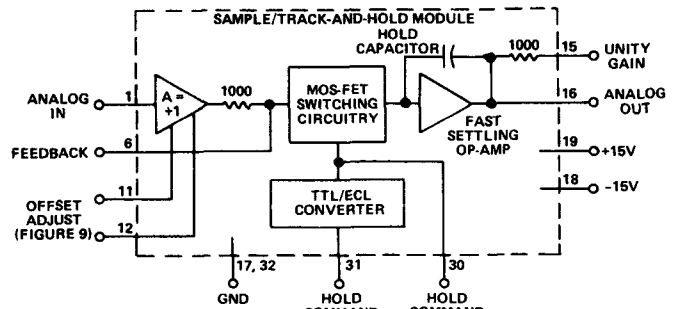
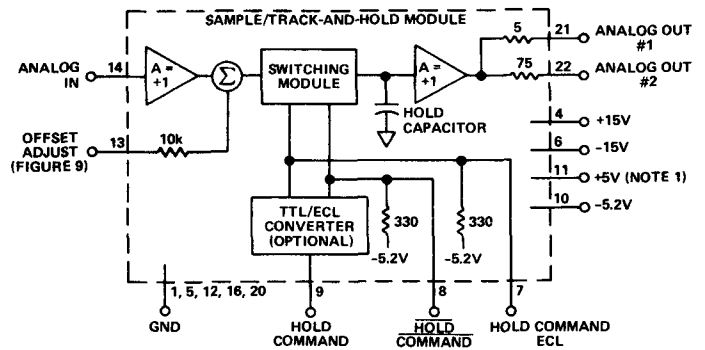


Figure 7. Sample/Track-and-Hold THC Series Block Diagram



NOTE: 1. THESE PINS UNUSED IF ECL INPUT OPTION IS SELECTED

Figure 8. Sample/Track-and-Hold THS Series Block Diagram

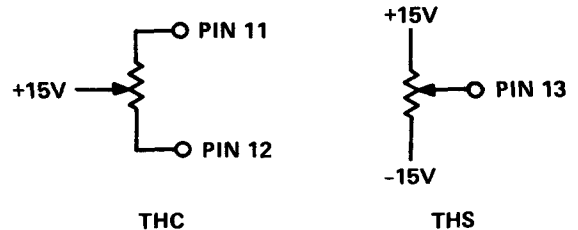


Figure 9. Optional Offset Adjustments

**ORDERING INFORMATION**

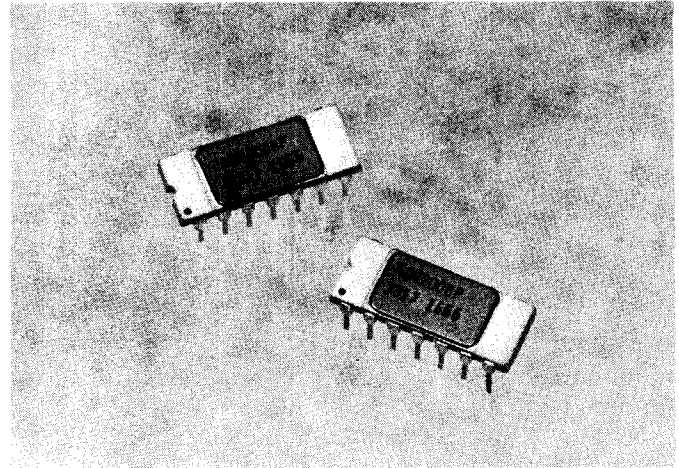
Order THS-0025 TTL, THS-0060 TTL, or THS-0225 TTL for TTL Hold Command Option.

Order THS-0025 ECL, THS-0060 ECL, or THS-0225 ECL for Balanced ECL Hold Command Input.

Order THC-0300, THC-0750, THC-1500 as required. All have available TTL and ECL Logic Inputs.

### FEATURES

**Latch-Proof DI CMOS**  
**Overvoltage-Proof:  $V_{SUPPLY} \pm 25V$**   
**Superior DG-200 Replacement**  
**Break-Before-Make Switching Action**  
 **$R_{ON}$ :  $100\Omega$  max over Full Temperature Range**  
**Direct TTL/CMOS Interface**

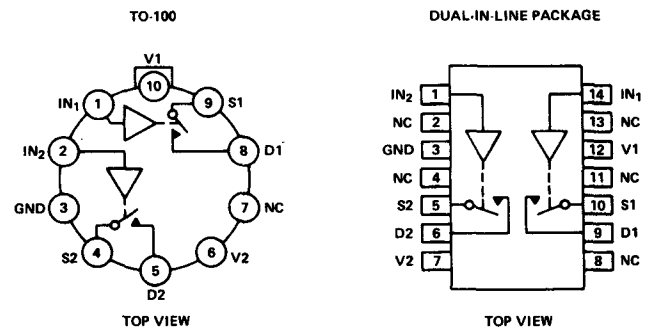


### GENERAL DESCRIPTION

The ADG200 is a dual single-pole-single-throw analog switch. In the ON condition, the switch conducts current in either direction, maintaining nearly constant ON resistance over the entire analog signal range. In the OFF condition, the switch blocks voltages of peak values equal to the switch  $V+$  and  $V-$  supplies. Switch action is break-before-make. The digital inputs interface directly to TTL or CMOS logic over the full operating temperature range.

Fabricated using an advanced monolithic dielectrically-isolated CMOS process, the ADG200 is a superior plug-in replacement for the DG200. The ADG200 provides additional advantages (over the DG200) of: overvoltage protection to  $\pm 25V$  beyond the power supplies, total latch-free operation, much lower power dissipation (30mW max) and faster switching time.

### PIN CONFIGURATION



SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

### ORDERING INFORMATION

| Commercial<br>0 to +70°C | Industrial<br>-25°C to +85°C |          | Military<br>-55°C to +125°C |                          |
|--------------------------|------------------------------|----------|-----------------------------|--------------------------|
|                          | Ceramic                      | TO-100   | Ceramic                     | TO-100                   |
| ADG200CJ                 | ADG200BP                     | ADG200BA | ADG200AP                    | ADG200AA<br>ADG200AA/883 |

Note: "/883" version is 100% screened to MIL-STD-883, class B as per note 7, page 310S.

# SPECIFICATIONS

| CHARACTERISTIC  | TYP <sup>1</sup><br>+25°C | MAX LIMITS                  |                   |             |                      |                   |                       | UNITS | TEST CONDITIONS <sup>8</sup><br>Unless Noted V <sub>1</sub> = +15V<br>V <sub>2</sub> = -15V, GND = 0V                |   |
|---|---------------------------|-----------------------------|-------------------|-------------|----------------------|-------------------|-----------------------|-------|--|---|
|   |                           | AA, AP Suffix               |                   |             | BA, BP/CJ Suffix     |                   |                       |       |  |   |
|   |                           | -55°C <sup>2</sup>          | +25°C             | +125°C      | -25/0°C <sup>2</sup> | +25°C             | +85/70°C <sup>2</sup> |       |  |   |
| <b>SWITCH</b>   |                           |                             |                   |             |                      |                   |                       |       |  |   |
| <b>I<sub>DS(ON)</sub></b> Drain-Source ON Resistance                                | 60<br>40                  | 70<br>70                    | 70<br>70          | 100<br>100  | 80<br>80             | 80<br>80          | 100<br>100            | Ω     | V <sub>D</sub> = 10V<br>V <sub>D</sub> = -10V  | V <sub>IN</sub> = 0.8V<br>I <sub>S</sub> = 0.1mA                    |
| <b>I<sub>S(OFF)</sub></b> Source OFF Leakage Current                                | 0.2<br>-0.2               | 500<br>-500                 | 2<br>-2           | 500<br>-500 | 500<br>-500          | 5<br>-5           | 500<br>-500           | nA    | V <sub>S</sub> = 10V, V <sub>D</sub> = -10V<br>V <sub>S</sub> = -10V, V <sub>D</sub> = 10V                           | V <sub>IN</sub> = 2.4V  |
| <b>I<sub>D(OFF)</sub></b> Drain OFF Leakage Current                                 | 0.3<br>-0.3               | 500<br>-500                 | 2<br>-2           | 500<br>-500 | 500<br>-500          | 5<br>-5           | 500<br>-500           |       | V <sub>D</sub> = 10V, V <sub>S</sub> = -10V<br>V <sub>D</sub> = -10V, V <sub>S</sub> = 10V                           |   |
| <b>I<sub>D(ON)</sub></b> <sup>3</sup> Channel ON Leakage Current                    | 0.1<br>-0.1               | 500<br>-500                 | 2<br>-2           | 500<br>-500 | 500<br>-500          | 2<br>-2           | 500<br>-500           |       | V <sub>D</sub> = V <sub>S</sub> = 10V<br>V <sub>D</sub> = V <sub>S</sub> = -10V                                      | V <sub>IN</sub> = 0.8V  |
| <b>INPUT</b>  |                           |                             |                   |             |                      |                   |                       |       |  |   |
| <b>I<sub>INH</sub></b> Input Current<br>Input Voltage High                          |                           | -10<br>10                   | -1<br>1           | -10<br>10   | -10<br>10            | -1<br>1           | -10<br>10             | μA    | V <sub>IN</sub> = 2.4V<br>V <sub>IN</sub> = 15V  |   |
| <b>I<sub>IN(PEAK)</sub></b> <sup>4</sup> Peak Input Current Required for Transition |                           | NOT APPLICABLE <sup>4</sup> |                   |             |                      |                   |                       |       |  |   |
| <b>I<sub>INL</sub></b> Input Current<br>Input Voltage Low                           |                           | -10                         | -1                | -10         | -10                  | -1                | -10                   | μA    | V <sub>IN</sub> = 0V   |   |
| <b>DYNAMIC</b>  |                           |                             |                   |             |                      |                   |                       |       |  |   |
| <b>t<sub>ON</sub></b> Turn-ON Time <sup>5</sup>                                     | 300                       |                             | 1000 <sup>2</sup> |             |                      | 1000 <sup>2</sup> |                       | ns    | V <sub>IN</sub> = 3.5V to 0V<br>V <sub>IN</sub> = 0V to 3.5V   | R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 35pF<br>V <sub>S</sub> = ±5V |
| <b>t<sub>OFF</sub></b> Turn-OFF Time <sup>5</sup>                                   | 120                       |                             | 500 <sup>2</sup>  |             |                      | 500 <sup>2</sup>  |                       |       |  |   |
| <b>C<sub>S(OFF)</sub></b> Source OFF Capacitance                                    | 11                        |                             |                   |             |                      |                   |                       | pF    | V <sub>S</sub> = 0V, V <sub>IN</sub> = 5V  |   |
| <b>C<sub>D(OFF)</sub></b> Drain OFF Capacitance                                     | 11                        |                             |                   |             |                      |                   |                       | pF    | V <sub>D</sub> = 0V, V <sub>IN</sub> = 5V  | f = 140kHz  |
| <b>C<sub>D(ON)</sub> + C<sub>S(ON)</sub></b> Channel ON Capacitance                 | 28                        |                             |                   |             |                      |                   |                       | pF    | V <sub>D</sub> = V <sub>S</sub> = 0V<br>V <sub>IN</sub> = 0V   |   |
| <b>OFF Isolation</b> <sup>6</sup>   | 64                        |                             |                   |             |                      |                   |                       | dB    | V <sub>IN</sub> = 5V, R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 15pF<br>V <sub>S</sub> = 7V <sub>rms</sub> , f = 500kHz |   |
| <b>SUPPLY</b>   |                           |                             |                   |             |                      |                   |                       |       |  |   |
| <b>I<sub>1</sub></b> Positive Supply Current  | 0.02                      | 2                           | 1                 | 2           | 2                    | 1                 | 2                     | mA    | Both Channels ON; V <sub>IN</sub> = 0V   |   |
| <b>I<sub>2</sub></b> Negative Supply Current  | -0.02                     | -2                          | -1                | -2          | -2                   | -1                | -2                    | mA    |  |   |
| <b>I<sub>1</sub></b> Positive Supply Current  | 0.1                       | 2                           | 1                 | 2           | 2                    | 1                 | 2                     | mA    | Both Channels OFF; V <sub>IN</sub> = 5V  |   |
| <b>I<sub>2</sub></b> Negative Supply Current  | -0.02                     | -2                          | -1                | -2          | -2                   | -1                | -2                    | mA    |  |   |

**NOTES:**

- <sup>1</sup> Typical values for information only, not guaranteed or production tested.
- <sup>2</sup> Guaranteed, not subject to 100% production test.
- <sup>3</sup> I<sub>D(ON)</sub> is leakage from driver gate into ON switch.
- <sup>4</sup> Digital inputs are MOS gates. Typical leakage (+25°C) is less than 1 nanoamp. This is in contrast to other designs which require typically 150μA to switch.
- <sup>5</sup> Switch action is guaranteed break-before-make.
- <sup>6</sup> OFF isolation (dB) = 20 log V<sub>S</sub>/V<sub>D</sub> where V<sub>S</sub> = input to OFF switch and V<sub>D</sub> = output.

<sup>8</sup> Functional operation is possible for supply voltages less than ±15V, but the input logic switching threshold will shift (see page 312S).  
Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS

|  |                        |
|--|------------------------|
| V <sub>IN</sub> (Digital Input) to Ground                              | -.0.3V, V <sub>1</sub> |
| V <sub>S</sub> or V <sub>D</sub> to V <sub>1</sub><br>(1 second surge) | +25V, -40V             |
| (continuous)   | +20V, -35V             |
| V <sub>S</sub> or V <sub>D</sub> to V <sub>2</sub><br>(1 second surge) | -25V, +40V             |
| (continuous)   | -20V, +35V             |
| V <sub>1</sub> to Ground   | -.0.3V, +17V           |
| V <sub>2</sub> to Ground   | +0.3V, -17V            |
| Current, Any Terminal Except S or D                                    | 30mA                   |
| Current, S or D  | 50mA                   |
| Current, S or D Pulsed<br>(1ms, 10% duty cycle max)                    | 150mA                  |

## Operating Temperature

|               |                 |
|---------------|-----------------|
| AA, AP Suffix | -55°C to +125°C |
| BA, BP Suffix | -25°C to +85°C  |
| CJ Suffix     | 0°C to +70°C    |

## Storage Temperature

|            |                 |
|------------|-----------------|
| CJ Suffix  | -65°C to +125°C |
| All Others | -65°C to +150°C |

## Power Dissipation (Package)\*

|                        |       |
|------------------------|-------|
| Metal Can**            | 450mW |
| 14 Pin Ceramic DIP***  | 825mW |
| 14 Pin Plastic DIP**** | 470mW |

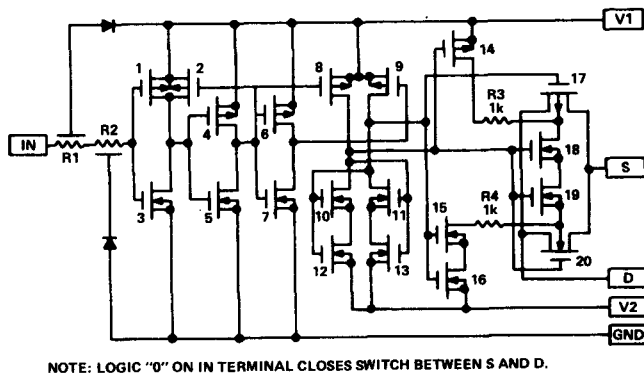
- \* Devices with all leads welded or soldered to printed circuit board
- \*\* Derate 6mW/°C above +75°C
- \*\*\* Derate 11mW/°C above +75°C
- \*\*\*\* Derate 6.5mW/°C above +25°C

### CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



### CIRCUIT DESCRIPTION



NOTE: LOGIC "0" ON IN TERMINAL CLOSES SWITCH BETWEEN S AND D.

Figure 1. Schematic Diagram (1 of 2 channels)

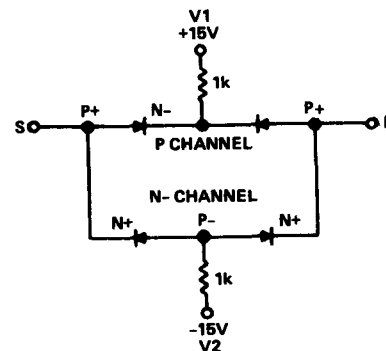


Figure 2. ADG200 Output Switch Diode Equivalent Circuit

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenon necessitate protection circuitry. However, these protection circuits either cause degradation of important switch parameters such as  $R_{ON}$  or leakage, or provide only limited protection in the event of overvoltage.

The ADG200 switch utilizes a dielectrically-isolated CMOS fabrication process to eliminate the four-layer structure found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 1. The output switching element consists of device numbers 17 and 20. Operation is as follows: for an "ON" switch, the gate of device 20 is  $V_1$  and the gate of device 17 is  $V_2$  from the driver circuits. Device numbers 14, 15, and 16 are "OFF" and numbers 18 and 19 are "ON". Hence, the back-gates of the P- and N-channel output devices (numbers 17 and 20) are tied together and floating. Floating the output switch back-gates with the signal input provides a flatter  $R_{ON}$  versus  $V_S$  response.

For an "OFF" switch, device numbers 18 and 19 are "OFF", and the back-gates of devices 17 and 20 are tied through  $1k\Omega$  resistors  $R_3$  and  $R_4$  to the respective supply voltages through the "ON" devices 14, 15, and 16.

If a voltage is applied to the S or D terminals which exceeds  $V_1$  or  $V_2$ , the S- or D-to-back-gate diode is forward biased; however,  $R_3$  and  $R_4$  provide current limiting action (Fig. 2).

Consequently, without external current limiting resistance (or increased  $R_{ON}$ ), the ADG200 series switches provide:

1. Latch-proof operation.
2. Overvoltage protection 25V beyond the  $V_1$  or  $V_2$  supply voltage.

An equivalent circuit of the output switch element in Figure 2 shows that, indeed, the  $1k\Omega$  limiting resistors are in series with the back-gates of the P- and N-channel output devices — *not* in series with the signal path between the S & D terminals.

In some applications it is possible to run on a parasitic NPN (drain to back-gate to source of the N-channel) transistor which causes device destruction under certain conditions. This case will only manifest itself when a negative overvoltage (and not a positive overvoltage) exists with another voltage source on the other side of the switch. Current limitation through external resistors ( $200\Omega$ ) or the output of op amps will prevent damage to the device.

## TYPICAL PERFORMANCE CHARACTERISTICS

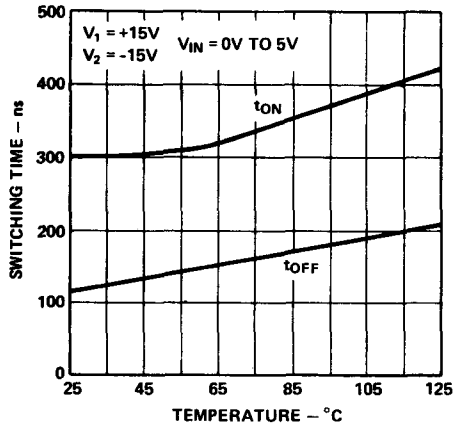


Figure 3. Switching Time vs. Temperature

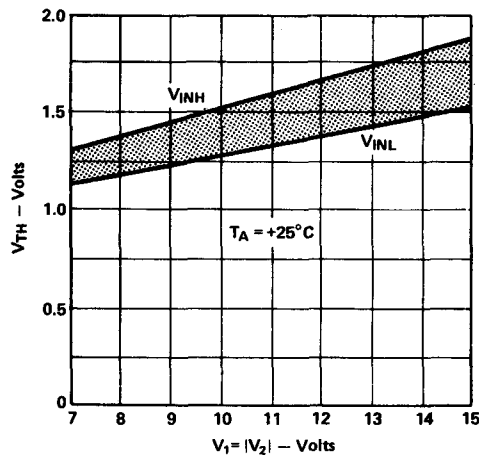
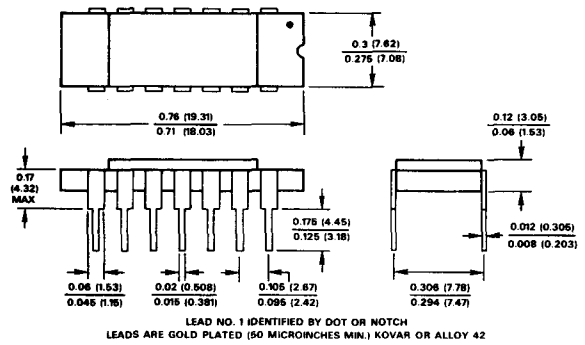


Figure 4. Input Logic Threshold vs. Power Supply Voltage

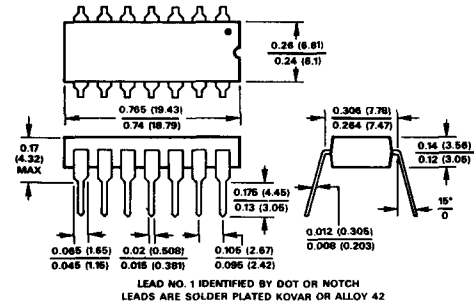
## MECHANICAL INFORMATION

Dimensions shown in inches and (mm).

### 14-PIN CERAMIC DIP

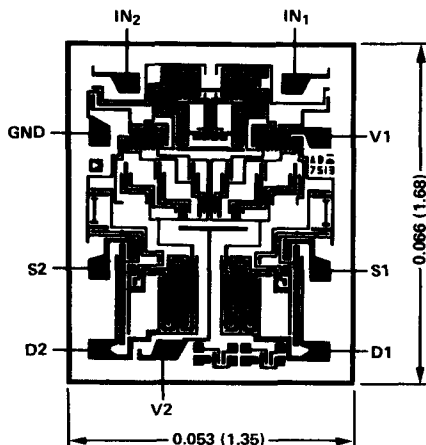


### 14-PIN PLASTIC DIP



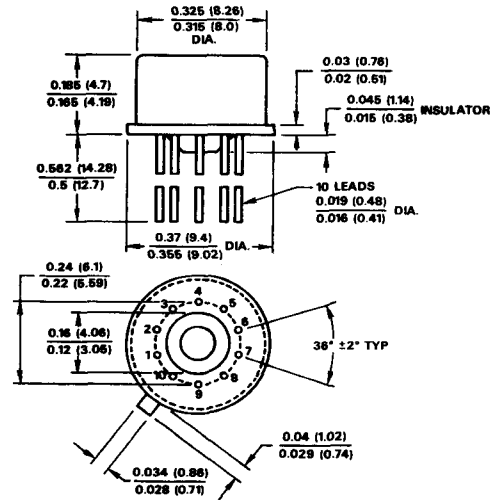
### BONDING DIAGRAM

Dimensions shown in inches and (mm).



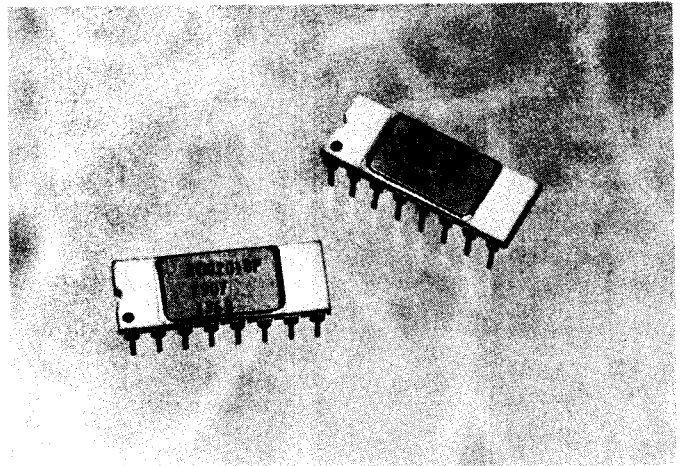
- NOTES:  
 1. BOND GND PIN FIRST TO MINIMIZE ESD HAZARD.  
 2. BONDING PADS ARE 0.004 × 0.004 INCHES (0.102 × 0.102mm).

### TO-100



### FEATURES

- Latch-Proof DI CMOS
- Overtoltage Proof to 25V Beyond Supplies
- Superior DG201 Replacement
- Break-Before-Make Switching Action
- Low  $R_{ON}$ : 80 $\Omega$
- Low Power Dissipation: 30mW max
- Direct TTL or CMOS Interfacing



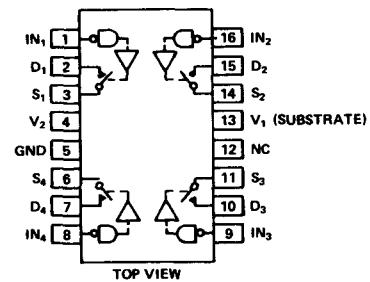
### GENERAL DESCRIPTION

The ADG201 is a quad SPST analog switch. In the ON state, the switch conducts current in either direction, maintaining nearly constant ON resistance over its signal handling range. In the OFF state, it blocks voltages equal to the switch V+ and V- supplies. Switch action is break-before-make.

The digital inputs interface directly to TTL or CMOS logic over the full operating temperature range.

Fabricated with an advanced monolithic dielectrically-isolated CMOS process, the ADG201 is a superior plug in replacement for the DG201. ADG201 advantages over other designs include: lower  $R_{ON}$ , lower power dissipation, faster switching time, overvoltage protection (25V beyond power supplies), and latch-free operation.

### PIN CONFIGURATION



SWITCH IS OPEN FOR LOGIC "1" (POSITIVE TRUE) INPUT

### ORDERING INFORMATION

| Commercial<br>0 to +70°C | Industrial<br>-25°C to +85°C | Military<br>-55°C to +125°            |
|--------------------------|------------------------------|---------------------------------------|
| Plastic                  | Ceramic                      | Ceramic                               |
| ADG201CJ                 | ADG201BP                     | ADG201AP<br>ADG201AP/883 <sup>1</sup> |

NOTE: "/883" version is 100% screened to MIL-STD-883, class B as per note 7, page 314S.

# SPECIFICATIONS

| CHARACTERISTIC  | TYP <sup>1</sup><br>+25°C | MAX LIMITS                  |          |             |                      |            |                       | UNITS | TEST CONDITIONS <sup>8</sup><br>Unless Noted V <sub>1</sub> = +15V<br>V <sub>2</sub> = -15V, GND = 0V                |   |
|---|---------------------------|-----------------------------|----------|-------------|----------------------|------------|-----------------------|-------|--|---|
|   |                           | AP SUFFIX                   |          |             | BP, CJ SUFFIX        |            |                       |       |  |   |
|   |                           | -55°C <sup>2</sup>          | +25°C    | +125°C      | -25/0°C <sup>2</sup> | +25°C      | +85/70°C <sup>2</sup> |       |  |   |
| <b>SWITCH</b>   |                           |                             |          |             |                      |            |                       |       |  |   |
| <b>I<sub>D(ON)</sub></b> Drain-Source ON Resistance                                 | 60<br>40                  | 80<br>80                    | 80<br>80 | 125<br>125  | 100<br>100           | 100<br>100 | 125<br>125            | Ω     | V <sub>D</sub> = 10V<br>V <sub>D</sub> = -10V  | V <sub>IN</sub> = 0.8V<br>I <sub>S</sub> = -1mA                     |
| <b>I<sub>S(OFF)</sub></b> Source OFF Leakage Current                                | 0.2<br>-0.2               | 500<br>-500                 | 1<br>-1  | 500<br>-500 | 250<br>-250          | 5<br>-5    | 250<br>-250           |       | V <sub>S</sub> = 10V, V <sub>D</sub> = -10V<br>V <sub>S</sub> = -10V, V <sub>D</sub> = 10V                           | V <sub>IN</sub> = 2.4V  |
| <b>I<sub>D(OFF)</sub></b> Drain OFF Leakage Current                                 | 0.3<br>-0.3               | 500<br>-500                 | 1<br>-1  | 500<br>-500 | 250<br>-250          | 5<br>-5    | 250<br>-250           | nA    | V <sub>D</sub> = 10V, V <sub>S</sub> = -10V<br>V <sub>D</sub> = -10V, V <sub>S</sub> = 10V                           | V <sub>IN</sub> = 2.4V  |
| <b>I<sub>D(ON)</sub></b> <sup>3</sup> Drain ON Leakage Current                      | 0.1<br>-0.1               | 500<br>-500                 | 1<br>-1  | 500<br>-500 | 250<br>-250          | 5<br>-5    | 250<br>-250           | nA    | V <sub>D</sub> = V <sub>S</sub> = 10V<br>V <sub>D</sub> = V <sub>S</sub> = -10V                                      | V <sub>IN</sub> = 0.8V  |
| <b>INPUT</b>  |                           |                             |          |             |                      |            |                       |       |  |   |
| <b>I<sub>INH</sub></b> Input Current<br>Input Voltage High                          |                           | -10<br>10                   | -1<br>1  | -10<br>10   | -10<br>10            | -1<br>1    | -10<br>10             | μA    | V <sub>IN</sub> = 2.4V<br>V <sub>IN</sub> = 15V  |   |
| <b>I<sub>IN(PEAK)</sub></b> <sup>4</sup> Peak Input Current Required for Transition |                           | NOT APPLICABLE <sup>4</sup> |          |             |                      |            |                       |       |  |   |
| <b>I<sub>INL</sub></b> Input Current<br>Input Voltage Low                           |                           | -10                         | -1       | -10         | -10                  | -1         | -10                   | μA    | V <sub>IN</sub> = 0V   |   |
| <b>DYNAMIC</b>  |                           |                             |          |             |                      |            |                       |       |  |   |
| <b>t<sub>ON</sub></b> Turn-ON Time <sup>2,5</sup>                                   | 260                       | 1000                        |          |             | 1000                 |            |                       | ns    | V <sub>IN</sub> = 3.5V to 0V<br>V <sub>IN</sub> = 0V to 3.5V   | R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 35pF<br>V <sub>S</sub> = ±5V |
| <b>t<sub>OFF</sub></b> Turn-OFF Time <sup>2,5</sup>                                 | 130                       | 500                         |          |             | 500                  |            |                       |       |  |   |
| <b>C<sub>S(OFF)</sub></b> Source OFF Capacitance                                    | 9                         |                             |          |             |                      |            |                       | pF    | V <sub>S</sub> = 0V, V <sub>IN</sub> = 5V  |   |
| <b>C<sub>D(OFF)</sub></b> Drain OFF Capacitance                                     | 9                         |                             |          |             |                      |            |                       | pF    | V <sub>D</sub> = 0V, V <sub>IN</sub> = 5V  |   |
| <b>C<sub>D(ON)</sub> + C<sub>S(ON)</sub></b> Channel ON Capacitance                 | 21                        |                             |          |             |                      |            |                       | pF    | V <sub>D</sub> = V <sub>S</sub> = 0V<br>V <sub>IN</sub> = 0V   |   |
| <b>OFF Isolation</b> <sup>6</sup>   | 65                        |                             |          |             |                      |            |                       | dB    | V <sub>IN</sub> = 5V, R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 15pF<br>V <sub>S</sub> = 7V <sub>rms</sub> , f = 500kHz |   |
| <b>SUPPLY</b>   |                           |                             |          |             |                      |            |                       |       |  |   |
| <b>I<sub>1</sub></b> Positive Supply Current  | 0.015                     | 2                           | 1        | 2           | 2                    | 1          | 2                     | mA    | One Channel ON, V <sub>IN</sub> = 0V   |   |
| <b>I<sub>2</sub></b> Negative Supply Current  | -0.015                    | -2                          | -1       | -2          | -2                   | -1         | -2                    | mA    |  |   |
| <b>I<sub>1</sub></b> Positive Supply Current  | 0.2                       | 2                           | 1        | 2           | 2                    | 1          | 2                     | mA    | All Channels OFF, V <sub>IN</sub> = 5V   |   |
| <b>I<sub>2</sub></b> Negative Supply Current  | -0.015                    | -2                          | -1       | -2          | -2                   | -1         | -2                    | mA    |  |   |

## NOTES:

- <sup>1</sup>Typical values for information only, not guaranteed or production tested.
- <sup>2</sup>Guaranteed, not subject to 100% production test.
- <sup>3</sup>I<sub>D(ON)</sub> is leakage from driver gate into ON switch.
- <sup>4</sup>Digital inputs are MOS gates. Typical leakage (+25°C) is less than 1 nanoamp. This is in contrast to other designs which require typically 150μA to switch.
- <sup>5</sup>Switch action is guaranteed break-before-make.
- <sup>6</sup>OFF isolation (dB) = 20 log V<sub>S</sub>/V<sub>D</sub> where V<sub>S</sub> = input to OFF switch and V<sub>D</sub> = output.

<sup>8</sup>Functional operation is possible for supply voltages less than ±15V, but the input switching threshold will shift (see page 316S).  
Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS

|  |                       |
|--|-----------------------|
| V <sub>IN</sub> (Digital Input) to Ground                              | -0.3V, V <sub>1</sub> |
| V <sub>S</sub> or V <sub>D</sub> to V <sub>1</sub><br>(1 second surge) | +25V, -40V            |
| (continuous)   | +20V, -35V            |
| V <sub>S</sub> or V <sub>D</sub> to V <sub>2</sub><br>(1 second surge) | -25V, +40V            |
| (continuous)   | -20V, +35V            |
| V <sub>1</sub> to Ground   | -0.3V, +17V           |
| V <sub>2</sub> to Ground   | +0.3V, -17V           |
| Current, any terminal except S or D                                    | 30mA                  |
| Continuous Current, S or D   | 50mA                  |
| Peak Current, S or D<br>(pulsed at 1ms, 10% duty cycle max)            | 150mA                 |

## Operating Temperature

|             |                 |
|-------------|-----------------|
| (AP Suffix) | -55°C to +125°C |
| (BP Suffix) | -25°C to +85°C  |
| (CJ Suffix) | 0°C to +70°C    |

## Storage Temperature

|                 |                 |
|-----------------|-----------------|
| (AP, BP Suffix) | -65°C to +150°C |
| (CJ Suffix)     | -65°C to +125°C |

## Power Dissipation (Package)\*

|                       |       |
|-----------------------|-------|
| 16 Pin Ceramic DIP**  | 900mW |
| 16 Pin Plastic DIP*** | 470mW |

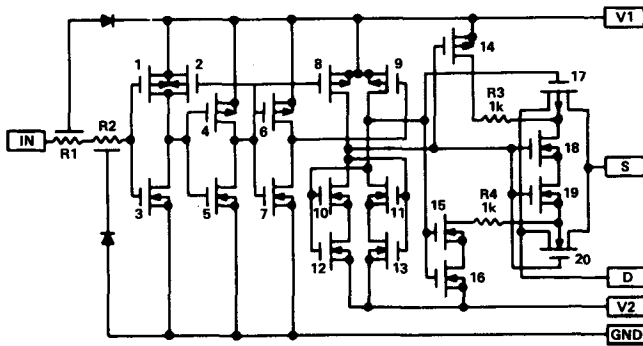
- \* Device mounted with all leads soldered or welded to PC board
- \*\* Derate 12mW/°C above +75°C
- \*\*\* Derate 6.5mW/°C above +25°C

### CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed for insertion.



### CIRCUIT DESCRIPTION



NOTE: LOGIC "0" ON IN TERMINAL CLOSES SWITCH BETWEEN S AND D.

Figure 1. Schematic Diagram, 1 of 4 Channels

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenon necessitate protection circuitry. However, these protection circuits either cause degradation of important switch parameters such as  $R_{ON}$  or leakage, or provide only limited protection in the event of overvoltage.

The ADG201 switch utilizes a dielectrically-isolated CMOS fabrication process to eliminate the four-layer structure found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 1. The output switching element consists of device numbers 17 and 20. Operation is as follows: for an "ON" switch, the gate of device 20 is  $V_1$  and the gate of device 17 is  $V_2$  from the driver circuits. Device numbers 14, 15, and 16 are "OFF" and numbers 18 and 19 are "ON". Hence, the back-gates of the P- and N-channel output devices (numbers 17 and 20) are tied together and floating. Floating the output switch back-gates with the signal input provides a flatter  $R_{ON}$  versus  $V_S$  response.

For an "OFF" switch, device numbers 18 and 19 are "OFF", and the back-gates of devices 17 and 20 are tied through  $1k\Omega$  resistors  $R_3$  and  $R_4$  to the respective supply voltages through the "ON" devices 14, 15 and 16.

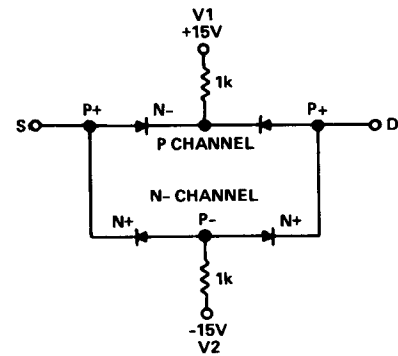


Figure 2. ADG201 Output Switch Diode Equivalent Circuit

If a voltage is applied to the S or D terminals which exceeds  $V_1$  or  $V_2$ , the S- or D-to-back-gate diode is forward biased; however,  $R_3$  and  $R_4$  provide current limiting action (Fig. 2).

Consequently, without external current limiting resistance (or increased  $R_{ON}$ ), the ADG201 series switches provide:

1. Latch-proof operation.
2. Overvoltage protection 25V beyond the  $V_1$  or  $V_2$  supply voltage.

An equivalent circuit of the output switch element in Figure 2 shows that, indeed, the  $1k\Omega$  limiting resistors are in series with the back-gates of the P- and N-channel output devices—not in series with the signal path between the S & D terminals.

In some applications it is possible to turn on a parasitic NPN (drain to back-gate to source of the N-channel) transistor which causes device destruction under certain conditions. This case will only manifest itself when a negative overvoltage (and not a positive overvoltage) exists with another voltage source on the other side of the switch. Current limitation through external resistors ( $200\Omega$ ) or the output of op amps will prevent damage to the device.



## TYPICAL PERFORMANCE CHARACTERISTICS

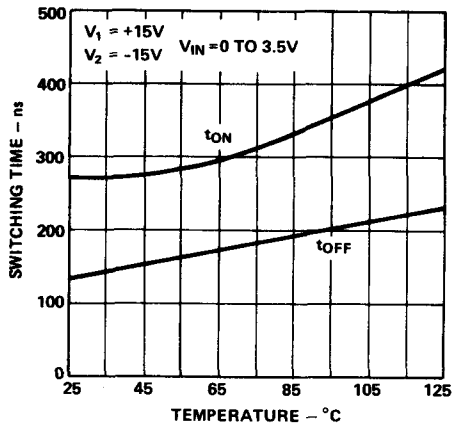


Figure 3. Switching Time vs. Temperature

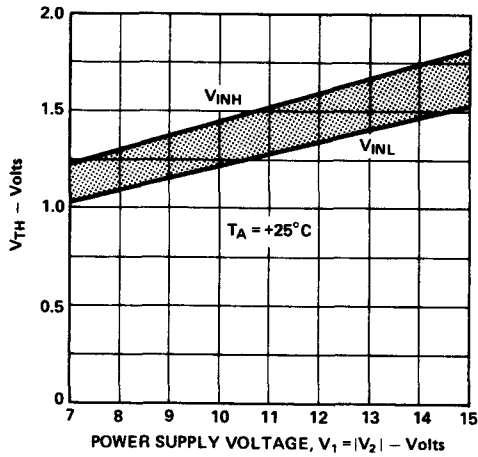
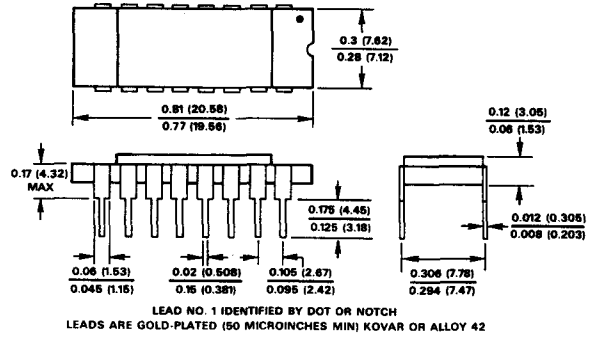


Figure 4. Input Logic Threshold vs. Power Supply Voltage

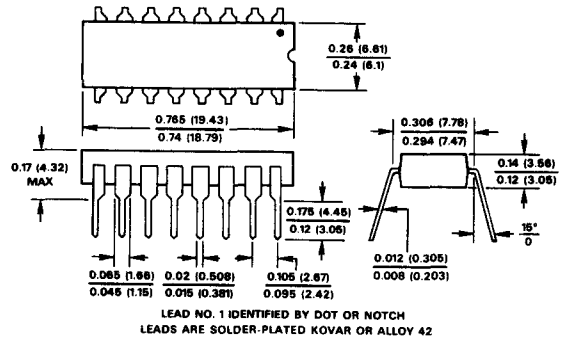
## MECHANICAL INFORMATION

Dimensions shown in inches and (mm).

### 16 PIN CERAMIC DIP

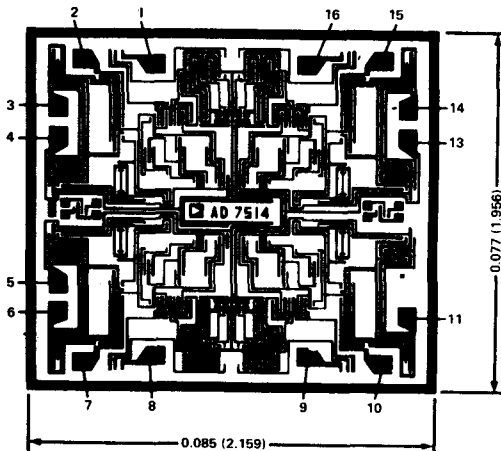


### 16 PIN PLASTIC DIP



## BONDING DIAGRAM

Dimensions shown in inches and (mm).



### NOTES:

1. PADS ARE 0.004 X 0.004 INCHES (0.102 X 0.102mm) MIN.
2. TO MINIMIZE ESD HAZARD, BOND PIN 5 FIRST.
3. PAD NUMBERS CORRESPOND TO PIN NUMBERS SHOWN ON PIN CONFIGURATION.

## FEATURES

### Versatility

- Complete System in Reliable IC Form
- Small Size: Two 32 Pin Metal DIP's
- 16 Single-Ended or 8 Differential Channels with Switchable Mode Control
- Military/Aerospace Temperature Range:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  (AD363S) MIL-STD-883B Processing Available
- Versatile Input/Output/Control Format
- Short-Cycle Capability

### Performance

- True 12 Bit Operation: Nonlinearity  $\leq \pm 0.012\%$
- Guaranteed No Missing Codes Over Temperature Range
- High Throughput Rate: 30kHz
- Low Power: 1.7W
- Hermetically-Sealed, Electrostatically-Shielded Metal DIP's

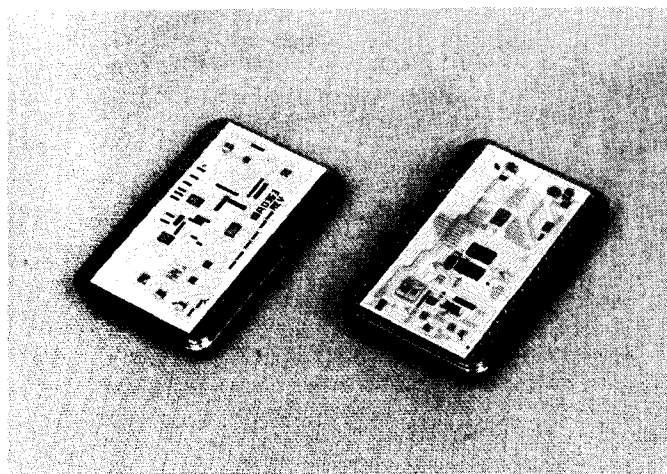
### Value

- Complete: No Additional Parts Required
- Reliable: Hybrid IC Construction, Hermetically Sealed by Welding. All Inputs Fully Protected.
- Precision  $\pm 10.0 \pm 0.005$  Volt Reference for External Application
- Fast Precision Buffer Amplifier for External Application
- Low Cost

## PRODUCT DESCRIPTION

The AD363 is a complete 16 channel, 12 bit data acquisition system in integrated circuit form. By applying large-scale linear and digital integrated circuitry, thick and thin film hybrid technology and active laser trimming, the AD363 equals or exceeds the performance and versatility of previous modular designs.

The AD363 consists of two separate functional blocks, each hermetically-sealed in an electrostatically-shielded 32 pin metal dual-in-line package. The analog input section contains two eight-channel multiplexers, a differential amplifier, a sample-and-hold, a channel address register and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD363 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced to an AD363 by dynamically switching the input mode control.



The Analog-to-Digital Converter Section contains a complete 12-bit successive approximation analog-to-digital converter, including internal clock, precision 10 volt reference, comparator, buffer amplifier and a proprietary-design 12 bit D/A converter. Active laser trimming of the reference and D/A converter results in maximum linearity errors of  $\pm 0.012\%$  while performing a 12 bit conversion in 25 microseconds.

Analog input voltage ranges of  $\pm 2.5$ ,  $\pm 5.0$ ,  $\pm 10$ , 0 to  $+5$  and 0 to  $+10$  volts are user-selectable. Adding flexibility and value are the precision 10 volt reference (active-trimmed to a tolerance of  $\pm 5\text{mV}$ ) and the internal buffer amplifier, both of which may be used for external applications. All digital signals are TTL/DTL compatible and output data is positive-true in parallel and serial form.

System throughput rate is as high as 30kHz at full rated accuracy. The AD363K is specified for operation over a 0 to  $+70^{\circ}\text{C}$  temperature range while the AD363S operates to specification from  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Processing to MIL-STD-883B is available for the AD363S. Both device grades are guaranteed to have no missing codes over their specified temperature ranges.

# SPECIFICATIONS (typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

| MODEL  | AD363K  | AD363S                        |
|--|---|-------------------------------|
| <b>ANALOG INPUTS</b>   |   |                               |
| Number of Inputs   | 16 Single-Ended or 8 Differential<br>(Electronically Selectable)  | *                             |
| Input Voltage Ranges   |   |                               |
| Bipolar  | ±2.5V, ±5.0V, ±10.0V  | *                             |
| Unipolar   | 0 to +5V, 0 to +10V   | *                             |
| Input (Bias) Current, Per Channel                                  | ±50nA max   | *                             |
| Input Impedance  |   |                               |
| On Channel   | 10 <sup>10</sup> Ω, 100pF   | *                             |
| Off Channel  | 10 <sup>10</sup> Ω, 10pF  | *                             |
| Input Fault Current (Power Off or On)                              | 20mA, max, Internally Limited   | *                             |
| Common Mode Rejection  |   |                               |
| Differential Mode  | 70dB min (80dB typ) @ 1kHz, 20V p-p   | *                             |
| Mux Crosstalk (Interchannel,<br>Any Off Channel to Any On Channel) | -80dB max (-90dB typ) @ 1kHz, 20V p-p   | *                             |
| <b>RESOLUTION</b>  |   |                               |
|  | 12 BITS   | *                             |
| <b>ACCURACY</b>  |   |                               |
| Gain Error <sup>1</sup>  | ±0.05% FSR (Adj. to Zero)   | *                             |
| Unipolar Offset Error  | ±10mV (Adj to Zero)   | *                             |
| Bipolar Offset Error   | ±20mV (Adj to Zero)   | *                             |
| Linearity Error  | ±½LSB max   | *                             |
| Differential Linearity Error                                       | ±1LSB max (±½LSB typ)   | *                             |
| Relative Accuracy  | ±0.025% FSR   | *                             |
| Noise Error  | 1mV p-p, 0 to 1MHz  | *                             |
| <b>TEMPERATURE COEFFICIENTS</b>                                    |   |                               |
| Gain   | ±30ppm/°C max (±10ppm/°C typ)   | ±25ppm/°C max (±15ppm/°C typ) |
| Offset, ±10V Range   | ±10ppm/°C max (±5ppm/°C typ)  | ±8ppm/°C max (±5ppm/°C typ)   |
| Differential Linearity   | No Missing Codes Over Temperature<br>Range  | *                             |
| <b>SIGNAL DYNAMICS</b>   |   |                               |
| Conversion Time <sup>2</sup>                                       | 25μs max (22μs typ)   | *                             |
| Throughput Rate, Full Rated Accuracy                               | 25kHz min (30kHz typ)   | *                             |
| Sample and Hold  |   |                               |
| Aperture Delay   | 100ns max (50ns typ)  | *                             |
| Aperture Uncertainty   | 500ps max (100ps typ)   | *                             |
| Acquisition Time   |   |                               |
| To ±0.01% of Final Value<br>for Full Scale Step                    | 18μs max (10μs, typ)  | *                             |
| Feedthrough  | -70dB max (-80dB typ) @ 1kHz  | *                             |
| Droop Rate   | 2mV/ms max (1mV/ms typ)   | *                             |
| <b>DIGITAL INPUT SIGNALS<sup>4</sup></b>                           |   |                               |
| Convert Command (to ADC Section,<br>Pin 21)                        | Positive Pulse, 200ns min Width. Leading<br>Edge ("0" to "1") Resets Register,<br>Trailing Edge ("1" to "0") Starts Con-<br>version.<br>1TTL Load | *<br>*                        |
| Input Channel Select (To Analog<br>Input Section, Pins 28-31)      | 4 Bit Binary, Channel Address.<br>1LS TTL Load  | *<br>*                        |
| Channel Select Latch (To Analog<br>Input Section, Pin 32)          | "1" Latch Transparent<br>"0" Latched<br>4LS TTL Loads   | *<br>*<br>*                   |

| MODEL   | AD363K   | AD363S          |
|---|--|-----------------|
| <b>DIGITAL INPUT SIGNALS, cont.</b>   |  |                 |
| Sample-Hold Command (To Analog Input Section Pin 13 Normally Connected To ADC "Status", Pin 20) | "0" Sample Mode<br>"1" Hold Mode<br>2LS TTL Loads  | *<br>*<br>*     |
| Short Cycle (To ADC Section Pin 14)   | Connect to +5V for 12 Bits Resolution.<br>Connect to Output Bit n + 1 For n Bits Resolution.<br>1TTL Load    | *<br>*<br>*     |
| Single Ended/Differential Mode Select (To Analog Input Section, Pin 1)                          | "0": Single-Ended Mode<br>"1": Differential Mode<br>3TTL Loads   | *<br>*<br>*     |
| <b>DIGITAL OUTPUT SIGNALS<sup>4</sup></b><br>(All Codes Positive True)                          |  |                 |
| Parallel Data   |  |                 |
| Unipolar Code   | Binary   | *               |
| Bipolar Code  | Offset Binary/Two's Complement   | *               |
| Output Drive  | 2TTL Loads   | *               |
| Serial Data (NRZ Format)  |  |                 |
| Unipolar Code   | Binary   | *               |
| Bipolar Code  | Offset Binary  | *               |
| Output Drive  | 2TTL Loads   | *               |
| Status (Status)   | Logic "1" ("0") During Conversion  | *               |
| Output Drive  | 2TTL Loads   | *               |
| Internal Clock  |  |                 |
| Output Drive  | 2TTL Loads   | *               |
| Frequency   | 500kHz   | *               |
| INTERNAL REFERENCE VOLTAGE  | +10.00V, ±5mV  | *               |
| Max External Current  | ±4mA   | *               |
| Voltage Temp. Coefficient   | ±20ppm/°C, max   | ±10ppm/°C, max  |
| <b>POWER REQUIREMENTS</b>   |  |                 |
| Supply Voltages/Currents  | +15V, ±5% @ +45mA max (+38mA typ)<br>-15V, ±5% @ -45mA max (-38mA typ)<br>+5V, ±5% @ +136mA max (+113mA typ) | *<br>*<br>*     |
| Total Power Dissipation   | 2 watts max (1.7 watts typ)  | *               |
| <b>TEMPERATURE RANGE</b>  |  |                 |
| Specification   | 0 to +70°C   | -55°C to +125°C |
| Storage   | -55°C to +85°C <sup>3</sup>  | -55°C to +150°C |

**NOTES:**

<sup>1</sup> With 50Ω, 1% fixed resistor in place of Gain Adjust pot; see Figures 7 and 8.

<sup>2</sup> Conversion time of ADC Section.

<sup>3</sup> AD363K External Hold Capacitor is limited to +85°C; Analog Input Section and ADC Section may be stored at up to +150°C.


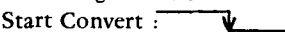
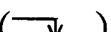
<sup>4</sup> One TTL Load is defined as I<sub>IL</sub> = -1.6mA max @ V<sub>IL</sub> = 0.4V, I<sub>IH</sub> = 40μA max @ V<sub>IH</sub> = 2.4V.

One LS TTL Load is defined as I<sub>IL</sub> = -0.36mA max @ V<sub>IL</sub> = 0.4V, I<sub>IH</sub> = 20μA max @ V<sub>IH</sub> = 2.7V.

Specifications subject to change without notice.

| <b>ABSOLUTE MAXIMUM RATINGS</b>      |                         |
|--------------------------------------|-------------------------|
| <b>(ALL MODELS)</b>                  |                         |
| +V, Digital Supply                   | +5.5V                   |
| +V, Analog Supply                    | +16V                    |
| -V, Digital Supply                   | -16V                    |
| V <sub>IN</sub> , Signal             | ±V, Analog Supply       |
| V <sub>IN</sub> , Digital            | 0 to +V, Digital Supply |
| A <sub>GND</sub> to D <sub>GND</sub> | ±1V                     |

**PIN FUNCTION DESCRIPTION**

| ANALOG INPUT SECTION |   | ANALOG TO DIGITAL CONVERTER SECTION |  |
|----------------------|---|-------------------------------------|--|
| Pin Number           | Function  | Pin Number                          | Function   |
| 1                    | Single-End/Differential Mode Select<br>"0": Single-Ended Mode<br>"1": Differential Mode       | 1                                   | Data Bit 12 (Least Significant Bit) Out  |
| 2                    | Digital Ground  | 2                                   | Data Bit 11 Out  |
| 3                    | Positive Digital Power Supply, +5V  | 3                                   | Data Bit 10 Out  |
| 4                    | "High" Analog Input, Channel 7  | 4                                   | Data Bit 9 Out   |
| 5                    | "High" Analog Input, Channel 6  | 5                                   | Data Bit 8 Out   |
| 6                    | "High" Analog Input, Channel 5  | 6                                   | Data Bit 7 Out   |
| 7                    | "High" Analog Input, Channel 4  | 7                                   | Data Bit 6 Out   |
| 8                    | "High" Analog Input, Channel 3  | 8                                   | Data Bit 5 Out   |
| 9                    | "High" Analog Input, Channel 2  | 9                                   | Data Bit 4 Out   |
| 10                   | "High" Analog Input, Channel 1  | 10                                  | Data Bit 3 Out   |
| 11                   | "High" Analog Input, Channel 0  | 11                                  | Data Bit 2 Out   |
| 12                   | Hold Capacitor (Provided, See Figure 1)   | 12                                  | Data Bit 1 (Most Significant Bit) Out  |
| 13                   | Sample-Hold Command<br>"0": Sample Mode<br>"1": Hold Mode<br>Normally Connected to ADC Pin 20 | 13                                  | Data Bit 1 (MSB) Out   |
| 14                   | Offset Adjust (See Figure 6)  | 14                                  | Short Cycle Control<br>Connect to +5V for 12 Bits<br>Connect to Bit (n+1) Out for n Bits   |
| 15                   | Offset Adjust (See Figure 6)  | 15                                  | Digital Ground   |
| 16                   | Analog Output<br>Normally Connected to ADC<br>"Analog In" (See Figure 1)                      | 16                                  | Positive Digital Power Supply, +5V   |
| 17                   | Analog Ground   | 17                                  | Status Out<br>"0": Conversion in Progress<br>(Parallel Data Not Valid)<br>"1": Conversion Complete<br>(Parallel Data Valid)  |
| 18                   | "High" ("Low") Analog Input, Channel 15 (7)   | 18                                  | +10Volt Reference Out (See Figures 3, 7, 8, 11)  |
| 19                   | "High" ("Low") Analog Input, Channel 14 (6)   | 19                                  | Clock Out (Runs During Conversion)   |
| 20                   | Negative Analog Power Supply, -15V  | 20                                  | Status Out<br>"0": Conversion Complete<br>(Parallel Data Valid)<br>"1": Conversion in Progress<br>(Parallel Data Not Valid)  |
| 21                   | Positive Analog Power Supply, +15V  | 21                                  | Convert Start In<br>Reset Logic : <br>Start Convert :  |
| 22                   | "High" ("Low") Analog Input, Channel 13 (5)   | 22                                  | Comparator In (See Figures 3, 7, 8)  |
| 23                   | "High" ("Low") Analog Input, Channel 12 (4)   | 23                                  | Bipolar Offset<br>Open for Unipolar Inputs<br>Connect to ADC Pin 22 for<br>Bipolar Inputs<br>(See Figure 8)  |
| 24                   | "High" ("Low") Analog Input, Channel 11 (3)   | 24                                  | 10V Span R In (See Figure 7)   |
| 25                   | "High" ("Low") Analog Input, Channel 10 (2)   | 25                                  | 20V Span R In (See Figure 8)   |
| 26                   | "High" ("Low") Analog Input, Channel 9 (1)  | 26                                  | Analog Ground  |
| 27                   | "High" ("Low") Analog Input, Channel 8 (0)  | 27                                  | Gain Adjust (See Figures 7 and 8)  |
| 28                   | Input Channel Select, Address Bit AE  | 28                                  | Positive Analog Power Supply, +15V   |
| 29                   | Input Channel Select, Address Bit AO  | 29                                  | Buffer Out (For External Use)  |
| 30                   | Input Channel Select, Address Bit A1  | 30                                  | Buffer In (For External Use)   |
| 31                   | Input Channel Select, Address Bit A2  | 31                                  | Negative Analog Power Supply, -15V   |
| 32                   | Input Channel Select Latch<br>"0": Latched<br>"1": Latch "Transparent"                        | 32                                  | Serial Data Out<br>Each Bit Valid On Trailing (  )<br>Edge Clock Out, ADC Pin 19  |

## AD363 DESIGN

### Concept

The AD363 consists of two separate functional blocks as shown in Figure 1; each is packaged in a hermetically-sealed 32 pin metal DIP.

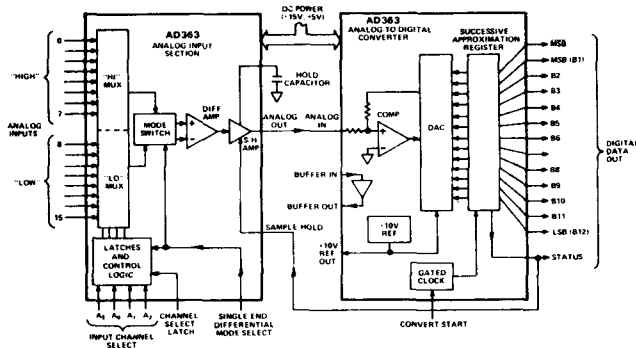


Figure 1. AD363 Functional Block Diagram

The Analog Input Section contains multiplexers, a differential amplifier, a sample-and-hold, a channel address register and control logic. Analog-to-digital conversion is provided by a 12 bit, 25 microsecond "ADC" which is also available separately as the AD572.

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration 32 pin packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

### Analog Input Section Design

Figure 2 is a block diagram of the AD363 Analog Input Section (AIS).

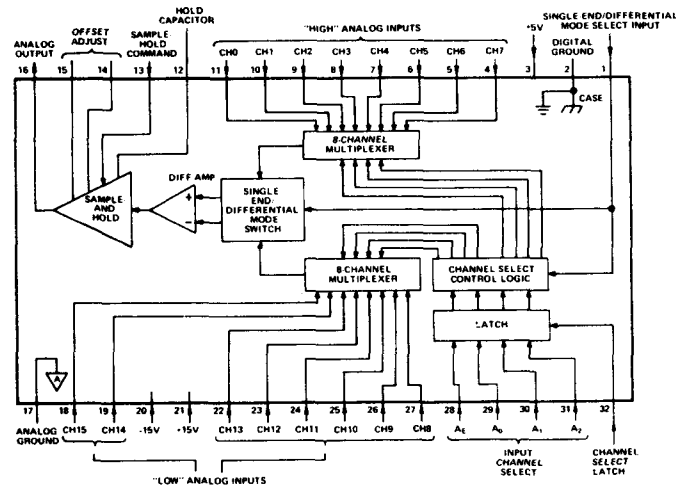


Figure 2. AD363 Analog Input Section Functional Block Diagram and Pinout

The AIS consists of two 8-channel multiplexers, a differential amplifier, a sample-and-hold, channel address latches and control logic. The multiplexers can be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD363 is an internal analog switch controlled by a digital input that performs switching between single-ended and differential modes. This feature allows a single product to perform in either mode without external hard-wire interconnections. Of more significance is the ability to serve a mixture of both single-ended and differential sources with a single AD363 by dynamically switching the input mode control.

Multiplexer channel address inputs are interfaced through a level-triggered ("transparent") input register. With a Logic "1" at the Channel Select Latch input, the address signals feed through the register to directly select the appropriate input channel. This address information can be held in the register by placing a Logic "0" on the Channel Select Latch input. Internal logic monitors the status of the Single-Ended/Differential Mode input and addresses the multiplexers accordingly.

A differential amplifier buffers the multiplexer outputs while providing high input impedance in both differential and single-ended modes. Amplifier gain and common mode rejection are actively laser-trimmed.

The sample-and-hold is a high speed monolithic device that can also function as a gated operational amplifier. Its uncommitted differential inputs allow it to serve a second role as the output subtractor in the differential amplifier. This eliminates one amplifier and decreases drift, settling time and power consumption. A Logic "1" on the Sample-and-Hold Command input will cause the sample-and-hold to "freeze" the analog signal while the ADC performs the conversion. Normally the Sample-and-Hold Command is connected to the ADC Status output which is at Logic "1" during conversion and Logic "0" between conversions. For slowly-changing inputs, throughput speed may be increased by grounding the Sample-and-Hold Command input instead of connecting it to the ADC status.

A Polystyrene hold capacitor is provided with each commercial temperature range system (AD363K) while a Teflon capacitor is provided with units intended for operation at temperatures up to 125°C (AD363S). Use of an external capacitor allows the user to make his own speed/accuracy tradeoff; a smaller capacitor will allow faster sample-and-hold response but will decrease accuracy while a larger capacitor will increase accuracy at slower conversion rates.

The Analog Input Section is constructed on a substrate that includes thick-film resistors for non-critical applications such as input protection and biasing. A separately-mounted laser-trimmed thin-film resistor network is used to establish accurate gain and high common-mode rejection. The metal package affords electromagnetic and electrostatic shielding and is hermetically welded at low temperatures. Welding eliminates the possibility of contamination from solder particles or flux while low temperature sealing maintains the accuracy of the laser-trimmed thin-film resistors.

## Analog-to-Digital Converter Design

Figure 3 is a block diagram of the Analog-to-Digital Converter Section (ADC) of the AD363.

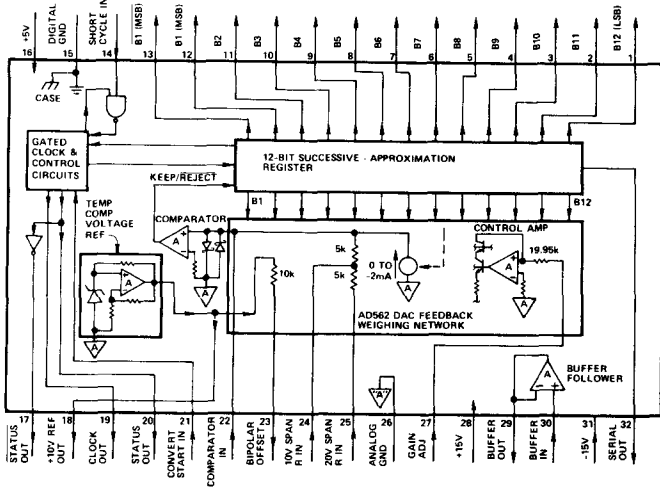


Figure 3. AD363 ADC Section (AD572) Functional Diagram and Pinout

Available separately as the AD572, the ADC is a 12 bit, 25 microsecond device that includes an internal clock, reference, comparator and buffer amplifier.

The +10V reference is derived from a low T.C. zener reference diode which has its zener voltage amplified and buffered by an op amp. The reference voltage is calibrated to +10V,  $\pm 5\text{mV}$  by active laser-trimming of the thin-film resistors which determine the closed-loop gain of the op amp. 4mA of current is available for external use. The reference circuit is constructed on its own thin-film substrate which is, in turn, mounted on the thick-film ADC main substrate.

The DAC feedback weighting network is comprised of a proprietary 12 bit analog current switch chip and silicon-chromium thin-film ladder network. (Packaged separately, this DAC is available as the AD562.) This ladder network is active laser-trimmed to calibrate all bit ratio scale factors to a precision of 0.005% of FSR (full-scale range) to guarantee no missing codes over the operating temperature range. The design of the ADC includes scaling resistors that provide user-selectable analog input signal ranges of  $\pm 2.5$ ,  $\pm 5$ ,  $\pm 10$ , 0 to +5, or 0 to +10 volts.

Other useful features include true binary output for unipolar inputs, offset binary and two's complement output for bipolar inputs, serial output, short-cycle capability for lower resolution, higher speed measurements, and an available high input impedance buffer amplifier which may be used elsewhere in the system.

As in the Analog Input Section, the ADC main substrate includes thick-film resistors in non-critical areas. Thin-film substrates are separately mounted to assure accurate and stable

reference and DAC performance. Packaging considerations are the same as for the AIS.

## THEORY OF OPERATION

### System Timing

Figure 4 is a timing diagram for the AD363 connected as shown in Figure 1 and operating at maximum conversion rate.

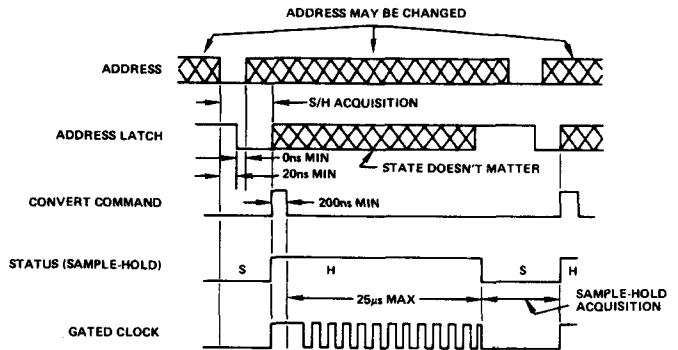


Figure 4. AD363 Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which indicates that it is "busy" by placing a Logic "1" on its Status line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy" the sample-and-hold is in the hold mode.
4. The ADC goes into its 25 microsecond conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not effect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0". The sample-and-hold returns to the sample mode.
6. If the input signal has changed full-scale (different channels may have widely-varying data) the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12 bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

### ADC Operation

On receipt of a Convert Start command, the analog-to-digital converter converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows:

The 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the respective device bit output pins and to the corresponding bit inputs of the feedback DAC.

The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

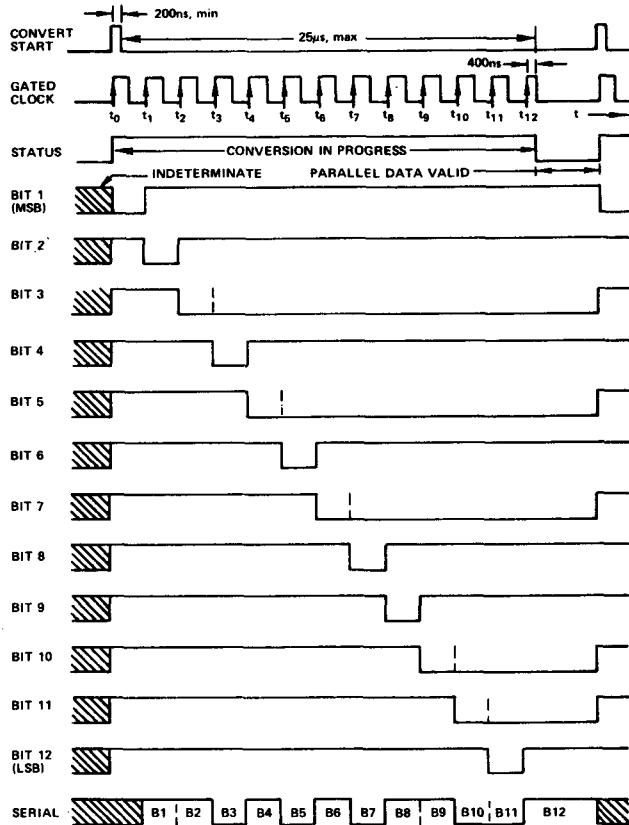


Figure 5. ADC Timing Diagram (Binary Code 110101011001)

The timing diagram is shown in Figure 5. Receipt of a Convert Start signal sets the Status flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All SAR parallel bit and Status flip-flops are initialized on the leading edge, and the gated clock inhibit signal removed on the trailing edge of the Convert Start signal. At time  $t_0$ , B1 is reset and B2-B12 are set unconditionally. At  $t_1$  the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At  $t_2$ , the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at  $t_{12}$ . After 400ns delay period, the Status flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the Status flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges.

Incorporation of this 400ns delay period guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the Status flag, permitting parallel data transfer to be initiated by the trailing edge of the Status signal.

The versatility and completeness of the AD363 concept results in a large number of user-selectable configurations. This allows optimization of most systems applications.

### Single-Ended/Differential Mode Control

The 363 features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a TTL logic input applied to pin 1 of the Analog Input Section:

- "0": Single-Ended (16 channels)
- "1": Differential (8 channels)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. Figure 11 illustrates an example of a "mixed" application. In this case, four microseconds must be allowed for the output of the Analog Input Section to settle to within  $\pm 0.01\%$  of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "hold mode"). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

### Input Channel Addressing

Table 1 is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding digital number to the four Input Channel Select address bits, AE, A0, A1, A2 (Analog Input Section, pins 28-31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1 and A2; AE must be enabled with a Logic "1". Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexers singly or in pairs as required.

| ADDRESS |    |    |    | ON CHANNEL (Pin Number) |                        |        |
|---------|----|----|----|-------------------------|------------------------|--------|
| AE      | A2 | A1 | A0 | Single Ended            | Differential "Hi" "Lo" |        |
| 0       | 0  | 0  | 0  | 0 (11)                  | None                   |        |
| 0       | 0  | 0  | 1  | 1 (10)                  | None                   |        |
| 0       | 0  | 1  | 0  | 2 (9)                   | None                   |        |
| 0       | 0  | 1  | 1  | 3 (8)                   | None                   |        |
| 0       | 1  | 0  | 0  | 4 (7)                   | None                   |        |
| 0       | 1  | 0  | 1  | 5 (6)                   | None                   |        |
| 0       | 1  | 1  | 0  | 6 (5)                   | None                   |        |
| 0       | 1  | 1  | 1  | 7 (4)                   | None                   |        |
| 1       | 0  | 0  | 0  | 8 (27)                  | 0 (11)                 | 0 (27) |
| 1       | 0  | 0  | 1  | 9 (26)                  | 1 (10)                 | 1 (26) |
| 1       | 0  | 1  | 0  | 10 (25)                 | 2 (9)                  | 2 (25) |
| 1       | 0  | 1  | 1  | 11 (24)                 | 3 (8)                  | 3 (24) |
| 1       | 1  | 0  | 0  | 12 (23)                 | 4 (7)                  | 5 (23) |
| 1       | 1  | 0  | 1  | 13 (22)                 | 5 (6)                  | 5 (22) |
| 1       | 1  | 1  | 0  | 14 (19)                 | 6 (5)                  | 6 (19) |
| 1       | 1  | 1  | 1  | 15 (18)                 | 7 (4)                  | 7 (18) |

Table 1. Input Channel Addressing Truth Table



When the channel address is changed, six microseconds must be allowed for the Analog Input Section to settle to within  $\pm 0.01\%$  of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "hold" mode).

#### Input Channel Address Latch

The AD363 is equipped with a latch for the Input Channel Select address bits. If the Latch Control pin (pin 32 of the Analog Input Section) is at Logic "1", input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the time of the "1" to "0" transition.

This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

#### Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input (Analog Input Section, pin 13) is normally connected to the Status output (pin 20) from the ADC section. When a conversion is initiated by applying a Convert Start command to the ADC (pin 21), Status goes to Logic "1", putting the sample-and-hold into the "hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the sample mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within  $\pm 0.01\%$  of the final value before a new Convert Start command is issued.

The purpose of a sample-and-hold is to "stop" fast changing input signals long enough to be converted. In this application, it also allows the user to change channels and/or SE/ DIFF mode while a conversion is in progress thus eliminating the effects of multiplexer, analog switch and differential amplifier settling times. If maximum throughput rate is required for slowly changing signals, the Sample-and-Hold Mode Control may be wired to ground (Logic "0") rather than to ADC Status thus leaving the sample-and-hold in a continuous sample mode.

#### Hold Capacitor

A 2000pF capacitor is provided with each AD363. One side of this capacitor is wired to the Analog Input Section pin 12, the other to analog ground as close to pin 17 as possible. The capacitor provided with the AD363K is Polystyrene while the wider operating temperature range of the AD363S demands a Teflon capacitor (supplied).

Larger capacitors may be substituted to minimize noise, but acquisition time of the sample-and-hold will be extended. If less than 12 bits of accuracy is required, a smaller capacitor may be used. This will shorten the S/H acquisition time. In all cases, the proper capacitor dielectric must be used; i.e., Polystyrene (AD363K only) or Teflon (AD363K or S). Other types of capacitors may have higher dielectric absorption (memory) and will cause errors. **CAUTION:** Polystyrene capacitors will be destroyed if subjected to temperatures above  $+85^{\circ}\text{C}$ . No capacitor is required if the sample-and-hold is not used.

#### Short Cycle Control

A Short Cycle Control (ADC Section, pin 14) permits the

timing cycle shown in Figure 5 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 14 is connected to +5V (ADC Section, pin 10). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the Status flag resets after the Bit 10 decision ( $t_{10} + 400\text{ns}$  in timing diagram of Figure 2). Short Cycle pin connections and associated maximum 12, 10 and 8-bit conversion times are summarized in Table 2.

| Connect Short Cycle Pin 14 to Pin: | Bits | Resolution (% FSR) | Maximum Conversion Time ( $\mu\text{s}$ ) | Status Flag Reset at: (Figure 5) |
|------------------------------------|------|--------------------|---|----------------------------------|
| 16                                 | 12   | 0.024              | 25  | $t_{12} + 400\text{ns}$          |
| 2                                  | 10   | 0.10               | 21  | $t_{10} + 400\text{ns}$          |
| 4                                  | 8    | 0.39               | 17  | $t_8 + 400\text{ns}$             |

Table 2. Short Cycle Connections

One should note that the calibration voltages listed in Table 4 are for 12-bit resolution only, and are not those corresponding to the center of each discrete quantization interval at reduced bit resolution.

#### Digital Output Data Format

Both parallel and serial data are in positive-true form and outputted from TTL storage registers. Parallel data output coding is binary for unipolar ranges and either offset binary or two's complement binary, depending on whether Bit 1 (ADC Section pin 12) or its logical inverse  $\bar{\text{Bit 1}}$  (pin 13) is used as the MSB. Parallel data becomes valid approximately 200ns before the Status flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the Status flag.

Serial data coding is binary for unipolar input ranges and offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid on all negative-going clock edges, permitting serial data to be clocked directly into a receiving register on these edges. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 5. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred at the completion of the conversion period.

#### Analog Input Voltage Range Format

The AD363 may be configured for any of 3 bipolar or 2 unipolar input voltage ranges as shown in Table 3.

| Range          | Connect Analog Input To ADC Pin: | Connect ADC Span Pin: | Connect Bipolar ADC Pin 23 To: |
|----------------|----------------------------------|-----------------------|--------------------------------|
| 0 to +5V       | 24                               | 25 to 22              | —                              |
| 0 to +10V      | 24                               | —                     |                                |
| -2.5V to +2.5V | 24                               | 25 to 22              | 22                             |
| -5V to +5V     | 24                               | —                     |                                |
| -10V to +10V   | 25                               | —                     |                                |

Table 3. Analog Input Voltage Range Pin Connections

| Analog Input - Volts<br>(Center of Quantization Interval) |                     |                       | Input Normalized<br>to FSR |                   | Digital Output Code<br>(Binary for Unipolar Ranges;<br>Offset Binary for Bipolar Ranges) |              |
|---|---------------------|-----------------------|----------------------------|-------------------|--|--------------|
| 0 to +10V<br>Range  | -5V to +5V<br>Range | -10V to +10V<br>Range | Unipolar<br>Ranges         | Bipolar<br>Ranges | B1<br>(MSB)  | B12<br>(LSB) |
| +9.9976   | +4.9976             | +9.9951               | +FSR-1 LSB                 | +½FSR-1 LSB       | 1  | 1            |
| +9.9952   | +4.9952             | +9.9902               | +FSR-2 LSB                 | +½FSR-2 LSB       | 1  | 1            |
| ⋮   | ⋮                   | ⋮                     | ⋮                          | ⋮                 | ⋮  | ⋮            |
| +5.0024   | +0.0024             | +0.0049               | +½FSR+1 LSB                | +1 LSB            | 1  | 0            |
| +5.0000   | +0.0000             | +0.0000               | +½FSR                      | ZERO              | 1  | 0            |
| ⋮   | ⋮                   | ⋮                     | ⋮                          | ⋮                 | ⋮  | ⋮            |
| +0.0024   | -4.9976             | -9.9951               | +1 LSB                     | -½FSR+1 LSB       | 0  | 0            |
| +0.0000   | -5.0000             | -10.0000              | ZERO                       | -½FSR             | 0  | 0            |

Table 4. Digital Output Codes vs Analog Input For Unipolar and Bipolar Ranges

The resulting input-output transfer functions are given by Table 4.

### Analog Input Section Offset Adjust Circuit

The offset voltage of the AD363 may be adjusted at either the Analog Input Section or the ADC Section. Normally the adjustment is performed at the ADC but in some special applications, it may be helpful to adjust the offset of the Analog Input Section. An example of such a case would be if the input signals were small (<10mV) relative to Analog Input Section voltage offset and gain was inserted between the Analog Input Section and the ADC. To adjust the offset of the Analog Input Section, the circuit shown in Figure 6 is recommended.

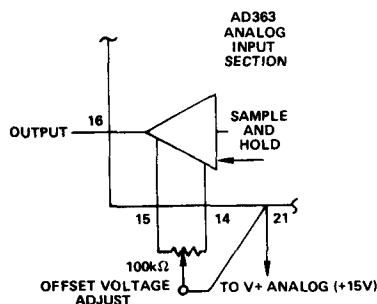


Figure 6. Analog Input Section Offset Voltage Adjustment

Under normal conditions, all calibration is performed at the ADC Section.

### ADC Offset Adjust Circuit

Analog and power connections for 0 to +10V unipolar and -10V to +10V bipolar input ranges are shown in Figures 7 and 8, respectively. The Bipolar Offset, ADC pin 23 is open-circuited for all unipolar input ranges, and connected to Comparator input (ADC pin 22) for all bipolar input ranges. The zero adjust circuit consists of a potentiometer connected across  $\pm V_S$  with its slider connected through a 3.9MΩ resistor to Comparator input (ADC pin 22) for all ranges. The tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a  $-1200\text{ppm}/^\circ\text{C}$  tempco contributes a worst-case offset tempco of  $8 \times 244 \times 10^{-6} \times 1200\text{ppm}/^\circ\text{C} = 2.3\text{ppm}/^\circ\text{C}$  of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than  $\pm 4\text{LSB}$ , use of a carbon composition offset summing resistor normally contributes no more than  $1\text{ppm}/^\circ\text{C}$  of FSR offset tempco.

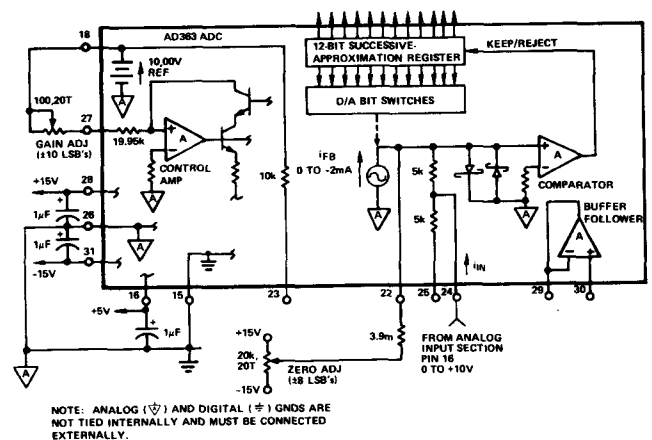


Figure 7. ADC Analog and Power Connections for Unipolar 0 to +10V Input Range

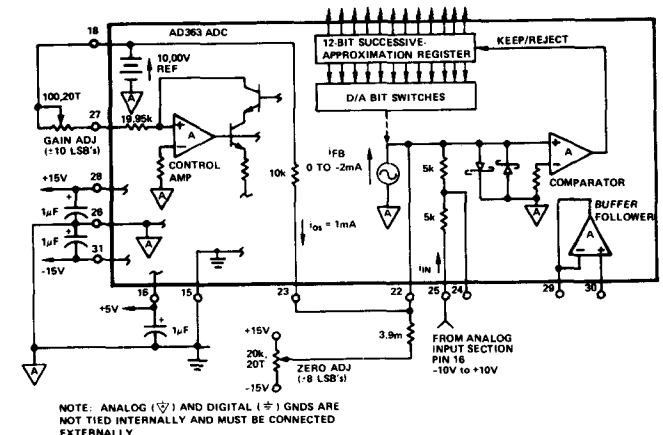


Figure 8. ADC Analog and Power Connections for Bipolar -10V to +10V Input Range

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco < 100 ppm/°C) are used, is shown in Figure 9.

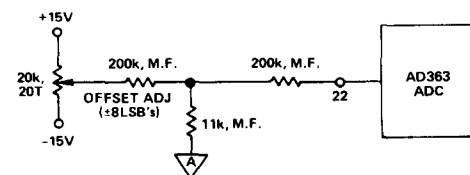


Figure 9. Low Tempco Zero Adj Circuit

In either zero adjust circuit, the fixed resistor connected to ADC pin 22 should be located close to this pin to keep the connection runs short, since the Comparator input (ADC pin 22) is quite sensitive to external noise pick-up.

### Gain Adjust

The gain adjust circuit consists of a  $100\Omega$  potentiometer connected between +10V Reference Output pin 18 and Gain Adjust Input (ADC pin 27) for all ranges. Both GAIN and ZERO ADJ potentiometers should be multi-turn, low tempco types; 20T cermet (tempco =  $100\text{ppm}/^\circ\text{C max}$ ) types are recommended. If the  $100\Omega$  GAIN ADJ potentiometer is replaced by a fixed  $50\Omega$  resistor, absolute gain calibration to  $\pm 0.1\%$  of FSR is guaranteed.

### Calibration

Calibration of the AD363 consists of adjusting offset and gain. Relative accuracy (linearity) is not affected by these adjustments, so if absolute zero and gain error is not important in a given application, or if system intelligence can correct for such errors, calibration may be unnecessary.

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 7, 8, and 9, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and  $-\frac{1}{2}\text{FSR}$  for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

**0 to +10V Range:** Set analog input to  $+1\text{LSB} = +0.0024\text{V}$ . Adjust Zero for digital output = 00000000001; Zero is now calibrated. Set analog input to  $+\text{FSR} - 2\text{LSB} = +9.9952\text{V}$ . Adjust Gain for 11111111110 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to  $+5.0000\text{V}$ ; digital output code should be 10000000000.

**-10V to +10V Range:** Set analog input to  $-9.9951\text{V}$ ; adjust Zero for 00000000001 digital output (offset binary) code. Set analog input to  $+9.9902\text{V}$ ; adjust Gain for 11111111110 digital output (offset binary) code. Half-scale calibration check: set analog input to  $0.0000\text{V}$ ; digital output (offset binary) code should be 10000000000.

**Other Ranges:** Representative digital coding for 0 to +10V, -5V to +5V, and -10V to +10V ranges is shown in Table 4. Coding relationships are calibration points for 0 to +5V and -2.5V to +2.5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -5V to +5V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately  $\pm\frac{1}{4}\text{LSB}$  using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter II-4.

### Other Considerations

**Grounding:** Analog and digital signal grounds should be kept

separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground (Analog Input Section pin 17, ADC Section pin 26) and Digital Ground (Analog Input Section pin 2 and ADC Section pin 15) are not connected internally; these pins must be connected externally for the system to operate properly. Preferably, this connection is made at only one point, as close to the system as possible. The cases are connected internally to Digital Ground to provide good electrostatic shielding. If the grounds are not tied common on the same card with both system packages, the digital and analog grounds should be connected locally with back-to-back general-purpose diodes as shown in Figure 10. This will protect the AD363 from possible damage caused by voltages in excess of  $\pm 1$  volt between the ground systems which could occur if the key grounding card should be removed from the overall system. The system will operate properly with as much as  $\pm 200\text{mV}$  between grounds, however this difference will be reflected directly as an input offset voltage.

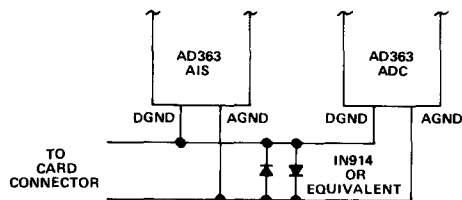


Figure 10. Ground-Fault Protection Diodes

**Power Supply Bypassing:** The  $\pm 15\text{V}$  and  $+5\text{V}$  power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance.  $1\mu\text{F}$  tantalum types are recommended; these capacitors should be located close to the system. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling since each power lead is bypassed internally with a  $0.039\mu\text{F}$  ceramic capacitor.

### Applications

The AD363 contains several unique features that contribute to its application versatility. The more significant features include a precision +10V reference, an uncommitted buffer amplifier, the dynamic single-ended/differential mode switch and simple, uncommitted digital interfaces.

### Transducer Interfacing

The precision +10V reference, buffer amplifier and mode switch can simplify transducer interfacing. Figure 11 illustrates how these features may be used to advantage.

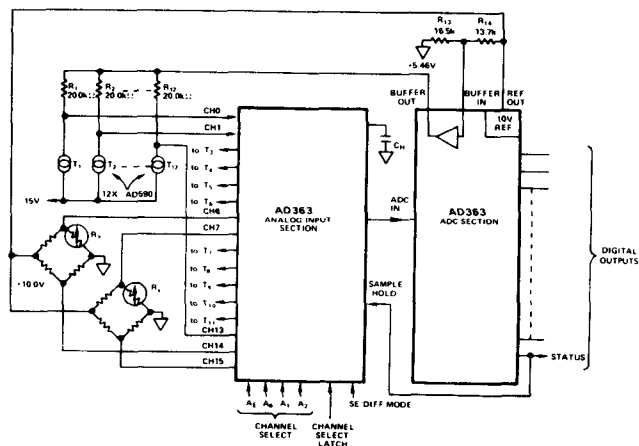


Figure 11. AD363 Transducer Interface Application

The AD590 is a temperature transducer that can be considered an ideal two-terminal current source with an output of one microamp per degree Kelvin ( $1\mu\text{A}/^\circ\text{K}$ ). With an offsetting current of  $273\mu\text{A}$  sourced from the  $+5.46$  volt buffered reference through  $20\text{k}\Omega$  resistors (R1-R12) each of the 12 AD590 circuits develop  $-20\text{mV}/^\circ\text{C}$ . The outputs are monitored with the AD363 front-end in the single-ended mode (Logic "0" on the Mode Control input). The  $+5.46$  volt reference is derived from the ADC  $+10$  volt precision reference and voltage divider R13, R14. Low output impedance for this  $+5.46$  volt reference is provided by the ADC internal buffer amplifier. (The  $10\mu\text{V}/^\circ\text{C}$  offset voltage drift of the buffer amplifier contributes negligible errors.) At  $0^\circ\text{C}$ , each temperature transducer circuit delivers a 0 volt output. At  $125^\circ\text{C}$ , the output is  $-2.5\text{V}$ ; at  $-55^\circ\text{C}$ , the output is  $+1.10\text{V}$ . By using the two's complement ADC output (complemented MSB or sign bit), the negative voltage versus temperature function is inverted and digital reading proportional to temperature in degrees centigrade is provided. Resolution is  $0.061^\circ\text{C}$  per least significant bit.

The precision  $+10$  volt reference is also used to power several bridge circuits that require differential read-out. When addressing these bridge transducers, a Logic "1" at the mode control input will switch the AD363 to the differential mode. In many cases, this feature will eliminate the requirement for a differential amplifier for each bridge transducer.

#### Microprocessor Interfacing

Digital interfacing to the AD363 has been deliberately left uncommitted; every processor system and application has different interface requirements and designing for one specific processor could complicate other applications.

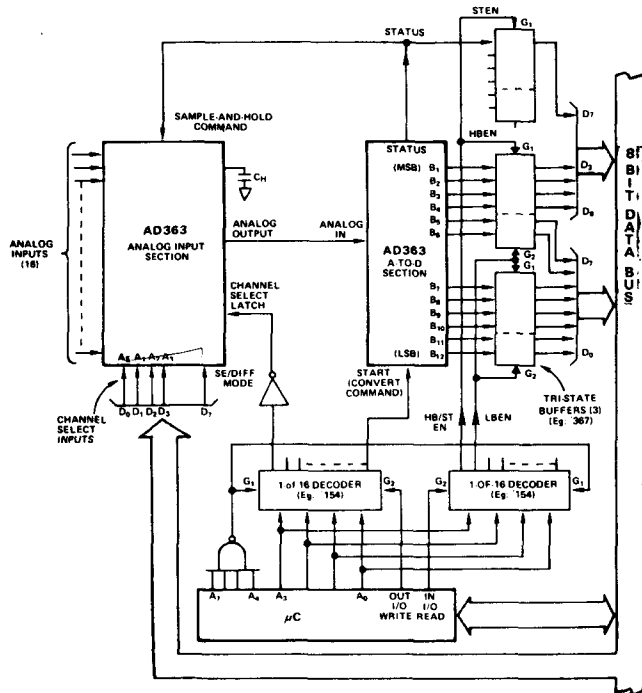


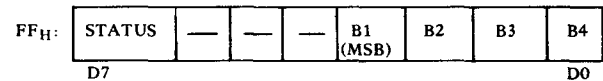
Figure 12. AD363 Microprocessor Interface Application

The addition of a small amount of hardware will satisfy most interface requirements; an example based on 8080-type architecture is shown in Figure 12.

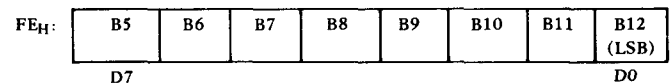
In this system the data bus is used to transmit multiplexer channel selection and convert and read commands to the AD363. It is also possible to address the AD363 as memory using the address bus to perform channel selection, convert and read operations.

The address lines can be decoded to provide channel selection, ADC convert start, status and ADC data (2 bytes) locations. These are accessed with I/O read/write instructions.

The ADC outputs are buffered with tri-state drivers. Figure 12 shows the 4 most significant ADC data bits and status as one byte



and the 8 least significant ADC data bits as the second byte.



Internal tri-state buffering is not provided because in many applications it would be better to have the first byte contain the 8 most significant bits. To accommodate both left and right justified formats would require more package pins and increase complexity.

The operating sequence for this system is as follows:

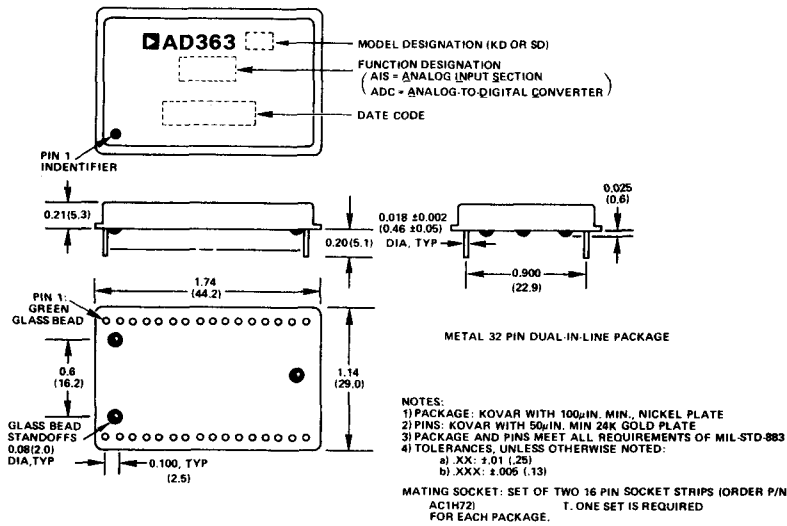
|   |     |     |   |
|---|-----|-----|---|
| 1 | MVI | 80H | puts the address for channel 0 (including SE/DIFF mode) into accumulator  |
| 2 | OUT | FFH | puts 80H on data bus and FFH on address bus. Pulses I/O WRITE. OUT FFH is decoded as a "LOAD ADDRESS" command to the channel select latches.                            |
| 3 | OUT | FOH | puts FOH on address bus and pulses I/O WRITE. This is decoded to issue a "CONVERSION START" to the ADC. Accumulator contents are of no significance.                    |
| 4 | IN  | FFH | puts FFH on address bus and pulses I/O READ. This is decoded to enable the appropriate tri-states, thus putting status and the 4 most significant bits on the data bus. |
| 5 | IN  | FEH | puts FEH on address bus and pulses I/O READ. This is decoded to enable the appropriate tri-states, thus putting the 8 least significant bits on the data bus.           |

The status may be examined for "0" (conversion complete). In that case, the 4 MSB's would be read.

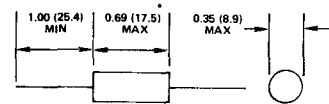
At this point, the multiplexer channel selection may be changed and another channel processed with the same instruction set (steps 2 through 5).

**OUTLINE DIMENSIONS  
PACKAGE SPECIFICATIONS**  
Dimensions shown in inches and (mm).

**ANALOG INPUT SECTION  
AND  
ANALOG-TO-DIGITAL CONVERTER**



**HOLD CAPACITOR**



\*THIS DIMENSION IS FOR POLYSTYRENE CAPACITOR SUPPLIED WITH K GRADE.  
MAX BODY LENGTH OF TEFLON CAPACITOR SUPPLIED WITH S GRADE IS 1.00"

**PROCESSING FOR HIGH RELIABILITY**

**STANDARD PROCESSING**

**PROCESSING TO MIL-STD-883**

As part of the standard manufacturing procedure, all models of the AD363 receive the following processing:

All models of AD363 ordered to the requirements of MIL-STD-883B, Method 5008 are identified with a /883B suffix and receive the following processing:

| PROCESS                           | CONDITIONS                   |
|-----------------------------------|------------------------------|
| 1) 100% pre-cap Visual Inspection | In-house Criteria            |
| 2) Stabilization Bake             | 24 hours @ +150°C            |
| 3) Seal Test, Gross Leak          | Method 1014 Test Condition C |
| 4) Operating Burn-In              | 48 hours @ +125°C            |

| PROCESS                               | CONDITIONS   |
|---------------------------------------|--|
| 1) 100% pre-cap Visual Inspection     | 2017.1   |
| 2) Stabilization Bake                 | 1008, 24 hours @ +150°C  |
| 3) Temperature Cycle                  | 1010, Test Condition C, 10 cycles, -65°C to +150°C                           |
| 4) Constant Acceleration              | 2001, Y1 Plane, 1000G  |
| 5) Visual Inspection                  | Visible Damage   |
| 6) Operating Burn-In                  | 1015, Test Condition B 160 hours @ +125°C                                    |
| 7) Seal Test: Fine Leak<br>Gross Leak | 1014, Test Condition A, 5 x 10 <sup>-7</sup> std cc/sec<br>1014, Condition C |
| 8) Final Electrical Test              | Per Data Sheet   |
| 9) External Visual Inspection         | 2009   |

**AD363 ORDERING GUIDE**

| Model            | Specification Temp Range  | Max Gain T.C. | Max Reference T.C. | Guaranteed Temp Range No Missing Codes |
|------------------|---|---------------|--------------------|--|
| AD363KD          | 0 to +70°C  | ±30ppm/°C     | ±20ppm/°C          | 0 to +70°C                             |
| AD363SD          | -55°C to +125°C   | ±25ppm/°C     | ±10ppm/°C          | -55°C to +125°C                        |
| AD363SD/<br>883B | Meets all AD363SD specifications after processing to the requirements of MIL-STD-883B, Method 5008. |               |                    |  |

NOTE: D Suffix = Dual-In-Line package designator.

### PRELIMINARY TECHNICAL DATA

#### FEATURES

##### DAS1150

- Resistor-Programmable Gain (1 = 1000V/V)
- High Accuracy with Low Level Input Signals
- Low Cost
- High Throughput Rate and High Gain

##### DAS1151

- Software-Programmable Gain (1, 2, 4, 8V/V)
- Provides Gain for Signal Conditioning and High Throughput Rate
- Gain Ratio Error:  $\pm 0.02\%$  FS max

### GENERAL DESCRIPTION

The DAS1150 and DAS1151 are two data acquisition modules designed, built and tested to meet system data acquisition requirements. The designs are comprised of an instrumentation amplifier, sample-hold amplifier and 12-bit successive approximation A/D converter. These products are used on Analog Devices Real Time Interface boards as data acquisition systems to interface with microcomputer boards.

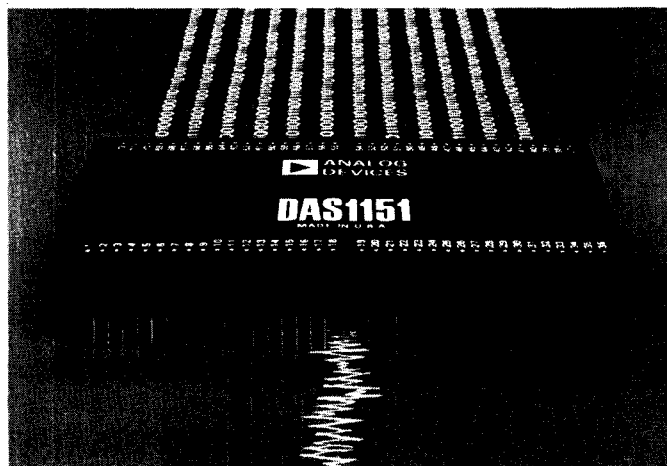
With the DAS1150 and DAS1151, users can apply gain to the instrumentation amplifier for signal conditioning and still achieve high speed data conversion. The difference between models is how the gain is controlled. With the DAS1150, the designer sets the gain from 1 to 1000 V/V with a resistor,  $R_G$ . The DAS1151 has gains of 1-2-4-8 that are software-programmable.

### DESIGN FEATURES AND USER BENEFITS

The DAS1150 and DAS1151 offer true high-speed 12-bit performance with maximum overall error at unity gain of  $\pm 1$  least significant bit (LSB). This performance is guaranteed at a 25kHz throughput rate. There is very little performance lost at high gains. For example, at gain of 1000, the DAS1150 has a throughput of 13kHz and an overall accuracy of  $\pm 2$ LSB. The DAS1151 with its software-programmable gain provides dynamic range expansion through subranging as well as the flexibility of using different gain settings to accommodate different input signal levels. The resistor-programmable-gain DAS1150 may be used for input ranges from 10mV full scale to  $\pm 10$ V full scale with very little loss of speed and no degradation of linearity at high gains.

### THEORY OF OPERATION

Block diagrams of the DAS1150 and DAS1151 are shown in Figures 1 and 2. Analog input signals are applied to the input of the instrumentation amplifier. The instrumentation amplifier is gain-programmable by the user via a resistor (DAS1150) or TTL/CMOS logic (DAS1151). This feature permits the user



to operate the module on any input voltage range from  $\pm 10$ mV to  $\pm 10$ V with the DAS1150 or any of 4 input voltage ranges with the DAS1151. The instrumentation amplifier drives a sample-hold amplifier, whose function is to hold the selected analog input signal at a constant level while the A/D converter is making a conversion.

The A/D converter is a high speed 12-bit successive approximation device that has been designed using Analog Devices AD562 integrated circuit D/A converter with a precision reference source, a high speed comparator and successive approximation logic; the laser trimmed AD562 which contains precision current switches and a very stable thin film resistor network provides excellent performance over temperature.

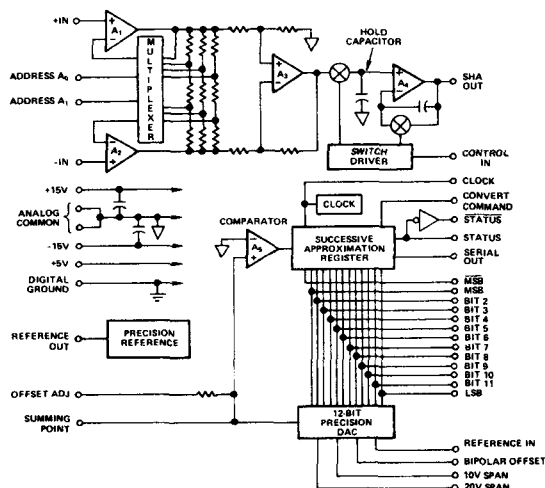


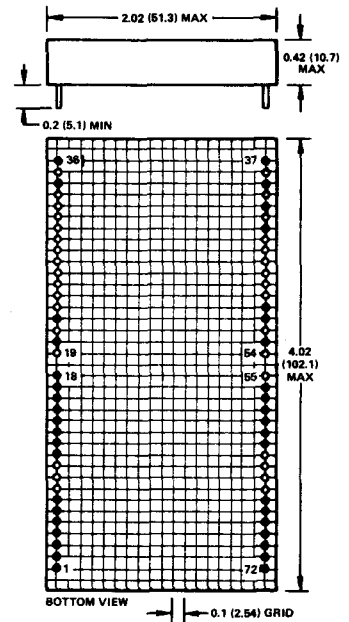
Figure 1. DAS1151 Block Diagram and Pin Designations

# SPECIFICATIONS (typical @ +25°C and rated supplies unless otherwise noted)

| MODELS  | DAS1150  | DAS1151                       |
|---|--|-------------------------------|
| RESOLUTION  | 12 Bits  | *                             |
| <b>DYNAMIC CHARACTERISTICS</b>                          |  |                               |
| ADC Conversion Time                                     | 25μs max   | *                             |
| IA Settling Time, 20V Input Step                        |  |                               |
| to 0.01% @ G = 1  | 15μs max   | (G = 1-8) 10μs max            |
| to 0.01% @ G = 10                                       | 15μs   | N.A.                          |
| to 0.05% @ G = 1000                                     | 50μs   | N.A.                          |
| Throughput Rate G = 1                                   | 25kHz  | (G = 1-8) 28.5kHz             |
| G = 10  | 25kHz  | N.A.                          |
| G = 1000  | 13.3kHz  | N.A.                          |
| Sample-Hold   |  |                               |
| Aperture Delay Time                                     | 90ns   | *                             |
| Aperture Time   | 20ns   | *                             |
| Aperture Uncertainty Time                               | 5ns  | *                             |
| Droop Rate  | 2mV/s  | *                             |
| <b>ACCURACY</b>   |  |                               |
| Overall Error @ G = 1                                   | ±1LSB max  | *                             |
| @ G = 1000  | ±2LSB max  | (G = 8) ±2LSB max             |
| Nonlinearity Error                                      | ±1/2LSB (±1LSB max)  | *                             |
| Offset Error  | Adjust to Zero   | *                             |
| Gain Error  | Adjust to Zero   | *                             |
| <b>TEMPERATURE COEFFICIENTS</b>                         |  |                               |
| Offset (RTI)  | $\pm \left(1 + \frac{50}{G}\right) \mu V/^{\circ}C$                                | ±30μV/°C                      |
| Gain (RTI)  | ±20ppm of Reading/°C   | *                             |
| Differential Nonlinearity                               | 2ppm/°C  | *                             |
| <b>ANALOG INPUTS</b>                                    |  |                               |
| Voltage Input Range $\left(\frac{ADC\ FS}{GAIN}\right)$ | 10mV to ±10V   | 0.625V to ±10V                |
| ADC Input Ranges  | 0 to +5V   | *                             |
|   | 0 to +10V  | *                             |
|   | ±2.5V  | *                             |
|   | ±5V  | *                             |
|   | ±10V   | *                             |
| Instrumentation Amplifier                               |  |                               |
| Gain  | Resistor-Programmable  | Software-Programmable         |
| Gain Range  | 1 to 1000  | 1, 2, 4, 8                    |
| Gain Equation   | $G = 1 + \left(\frac{20k\Omega}{R_G}\right)$                                       | See Table 4                   |
| Gain Ratio Error  | N.A.   | ±0.02% FS max                 |
| Input Impedance   | 10 <sup>8</sup> Ω  | *                             |
| Bias Current  | 20nA   | 2nA                           |
| Offset Current  | 2nA  | 500pA                         |
| Offset Voltage (RTI)                                    | ±50μV  | ±200μV                        |
| <b>DIGITAL INPUTS</b>                                   |  |                               |
| ADC Convert Command                                     | Positive Pulse, TTL Compatible, 100ns min Width                                    | *                             |
| SHA Mode Control  | Positive Pulse TTL Compatible Logic  | *                             |
|   | "1" = Hold, Logic "0" = Sample   | *                             |
| PGA Gain Control  | N.A.   | TTL Compatible, Positive True |
| <b>DIGITAL OUTPUT</b>                                   |  |                               |
| Parallel Data Output                                    | 6TTL Loads/Bit   | *                             |
| Unipolar  | Positive True Binary   | *                             |
| Bipolar   | Positive True Offset Binary or Two's Complement                                    | *                             |
| Serial Data Output                                      | 6 TTL Loads  | *                             |
| Unipolar  | Positive True Binary NRZ Format, MSB First   | *                             |
| Bipolar   | Positive True Offset Binary, NRZ Format, MSB First                                 | *                             |
| Status Output   | Logic "1" During Conversion, TTL Compatible, 4TTL Loads, Complement also Available | *                             |
| Clock Output  | 480kHz, TTL Compatible, 6TTL Loads   | *                             |
| <b>POWER REQUIREMENTS</b>                               |  |                               |
|   | +5V dc ±5% @ 130mA (170mA max)   | *                             |
|   | ±15V dc ±3% @ 30mA (40mA max)  | *                             |
|   | ±15V dc ±3% @ 30mA (40mA max)  | *                             |
| <b>TEMPERATURE RANGE</b>                                |  |                               |
| Operating   | 0 to +70°C   | *                             |
| Storage   | -55°C to +85°C   | *                             |

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES:  
TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.

SEE TABLE BELOW FOR PIN DELETIONS.

MODULE WEIGHT: 3.5 OUNCES (99.3 GRAMS).  
ALL PINS ARE GOLD PLATED HALF-HARD BRASS (MIL-G-45204), 0.019" ±0.001" (0.48 ±0.02mm) DIA.

| MODEL   | DELETED PINS |
|---------|--------------|
| DAS1150 | PINS 50, 51  |
| DAS1151 | PINS 41, 43  |

MATING SOCKET: AC1577

Specifications subject to change without notice.

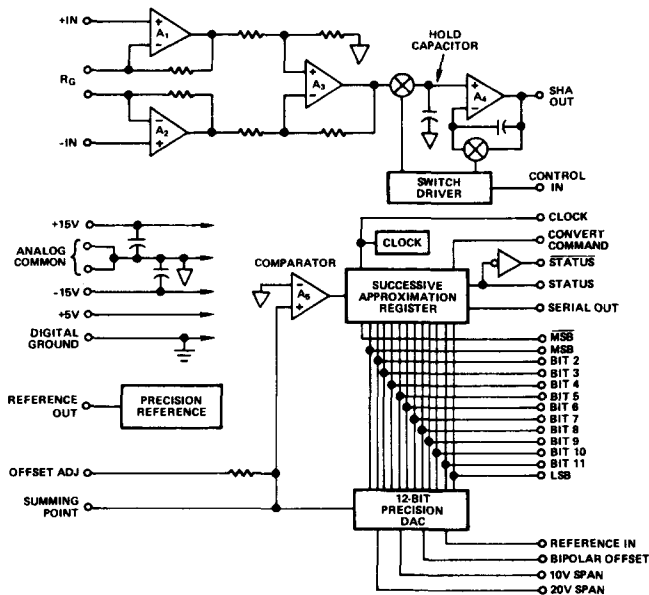
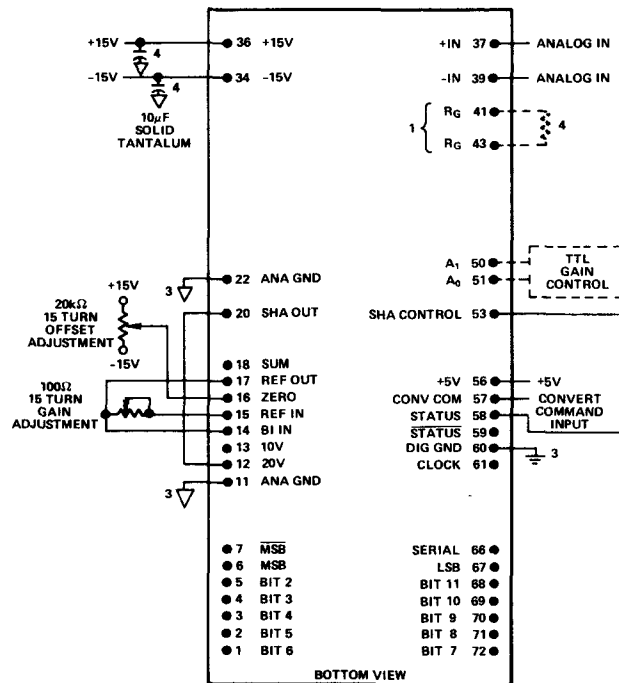


Figure 2. DAS1150 Block Diagram and Pin Designations

### GROUNDING PRACTICE

Attention should be given to the methods of connection for electrical returns and voltage reference points. Analog ground and digital ground are provided. These data acquisition systems do not have an internal connection between analog ground and digital ground and, thus, a connection must be provided in the external circuitry. The choice of an optimum "star" point for these grounds is an important consideration in the performance of the system. No strict rules can be given, only the general guidelines that the grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops between the high current carrying logic supply ground and the sensitive analog circuit sections.

1. If the  $\pm 15V$  power supply is floating (for optimum analog accuracy), connect its common to analog ground. If the  $\pm 15V$  power supply is not floating, connect its common to digital ground.
2. Connect the  $+5V$  supply common to digital ground. If this supply also powers additional equipment, run separate, parallel returns to the equipment ground and to digital ground.
3. Single-ended input signals should only be returned to analog ground. If this is not possible, then connect the input signals in the differential configuration.
4. Connect computer ground to digital ground. Use heavy wire or ground planes.
5. The computer chassis should be connected to the computer and power supply grounds at only one point.
6. Connect the third wire ground from main ac power input to the computer power supply return.
7. Bias return path should always be provided.



NOTES:  
<sup>1</sup> THESE PINS APPEAR ON DAS1150 ONLY.  
<sup>2</sup> THESE PINS APPEAR ON DAS1151 ONLY.  
<sup>3</sup> ANALOG AND DIGITAL GROUNDS SHOULD BE TIED TOGETHER AT ONE POINT AS CLOSE TO THE MODULE AS POSSIBLE.  
<sup>4</sup> SHOULD BE LOCATED WITHIN 1" FROM MODULE.

Figure 3. Module Connections for  $\pm 10V$  Range

Figure 3 shows the connections required to operate the DAS1150 or DAS1151 with a  $\pm 10V$  input range. Table 1 shows connections for ADC input ranges.

| Input Range | Jumper                     |
|-------------|----------------------------|
| 0 to $+5V$  | Pin 17 to 15, Pin 20 to 18 |
| $\pm 2.5V$  | Pin 17 to 14, Pin 20 to 18 |
| 0 to $+10V$ | Pin 17 to 15, Pin 20 to 13 |
| $\pm 5V$    | Pin 17 to 14, Pin 20 to 13 |
| $\pm 10V$   | Pin 17 to 14, Pin 20 to 12 |

Table 1. ADC Input Range Connections

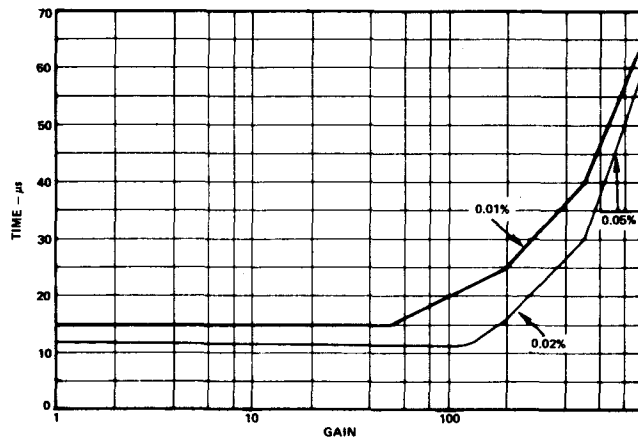


Figure 4. Typical Settling Time Curves for DAS1150



## GAIN AND OFFSET ADJUSTMENT PROCEDURE

| ADC ANALOG INPUT |            |  | DIGITAL OUTPUT |
|------------------|------------|--|----------------|
| +5V RANGE        | +10V RANGE |  | BINARY CODE    |
| +4.9988V         | +9.9976V   |  | 1111111111     |
| +2.5000V         | +5.0000V   |  | 1000000000     |
| +0.6250V         | +1.2500V   |  | 0010000000     |
| +0.0012V         | +0.0024V   |  | 0000000001     |
| +0.0000V         | +0.0000V   |  | 0000000000     |

Table 2. Nominal Unipolar Input-Output Relationships

| ADC ANALOG INPUT |           |            | DIGITAL OUTPUT     |                       |
|------------------|-----------|------------|--------------------|-----------------------|
| ±2.5V RANGE      | ±5V RANGE | ±10V RANGE | OFFSET BINARY CODE | TWO'S COMPLEMENT CODE |
| +2.4988V         | +4.9976V  | +9.9951V   | 1111111111         | 0111111111            |
| +1.2500V         | +2.5000V  | +5.0000V   | 1100000000         | 0100000000            |
| +0.0012V         | +0.0024V  | +0.0049V   | 1000000001         | 0000000001            |
| +0.0000V         | +0.0000V  | +0.0000V   | 1000000000         | 0000000000            |
| -2.5000V         | -5.0000V  | -10.0000V  | 0000000000         | 1000000000            |

Table 3. Nominal Bipolar Input-Output Relationships

### OFFSET CALIBRATION

For unipolar mode set the input voltage precisely to the value of 1 LSB (see Table 2) and adjust the offset potentiometer until the converter is just on the verge of switching from 0000000000 to 0000000001.

For bipolar mode set the input voltage precisely to zero volts. Adjust the offset potentiometer until the offset binary coded units are just on the verge of switching from 0111111111 to 1000000000 and two's complement coded units are just on the verge of switching 1111111111 to 0000000000.

### GAIN CALIBRATION

The analog input values given in Tables 2 and 3 are values that should be present at the input to the internal ADC. The value of the analog input will be affected by the gain of the

$$\text{module, i.e., ANALOG IN} = \left( \frac{\text{ADC FULL SCALE}}{\text{GAIN}} \right)$$

Set the ADC input voltage precisely to plus full scale minus 1 1/2 LSB's: +4.9982V for 5V units, +9.9963V for ±10V units, +2.4982V for ±2.5V units, +4.9963V for ±5V units, or +9.9926V for ±10V units. Adjust the 100Ω variable gain resistor until binary and offset binary coded units are just on the verge of switching from 1111111110 to 1111111111 and two's complement coded units are just on the verge of switching from 0111111110 to 0111111111.

### TIMING

The "0" to "1" transition of the CONVERT COMMAND input resets the MSB output to Logic "0" and the CLOCK STATUS, MSB, and BIT 2 through BIT 12 outputs to Logic "1". Nothing further happens until the CONVERT COMMAND returns to Logic "0", at which time the conversion proceeds.

With the MSB in the Logic "0" state, the internal digital-to-analog converter's (D/A) output is compared with the analog input (SHA OUT). If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB Logic "1". If the D/A output is greater than the analog input, the MSB remains at Logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to Logic "0" and another comparison is made. This process continues through each successive bit until the BIT 12 (LSB) comparison is completed. At this time the STATUS output returns to Logic "0" and the conversion cycle ends.

The SERIAL DATA output is of the non-return-to-zero (NRZ) type. The data is available, MSB first, 40ns after each of the twelve "0" to "1" clock transitions.

### AMPLIFIER GAIN

The DAS1150 instrumentation amplifier gain may be set to any any value between 1 and 1000 by connecting an external gain resistor between pins 41 and 43. The resistance is determined by the formula  $G = 1 + \left( \frac{20k\Omega}{R_G} \right)$ .  $R_G$  should be located as close as possible to the module pins. It must be noted that the TC of  $R_G$  directly affects the gain temperature coefficient of the DAS1150. A high quality metal film resistor 0.1% is recommended.

The gain of the DAS1151 is programmed by loading the proper code into the gain address, as shown in Table 4.

| ADDRESS INPUTS |                | DAS1151 GAIN |
|----------------|----------------|--------------|
| A <sub>1</sub> | A <sub>0</sub> |              |
| 0              | 0              | 1            |
| 0              | 1              | 2            |
| 1              | 0              | 4            |
| 1              | 1              | 8            |

Table 4. DAS1151 Gain State Truth Table

# Power Supplies : AC/DC & DC/DC

## Modular AC/DC Power Supplies

Analog Devices ac/dc Power Supplies are designed to provide OEM's and circuit designers with a broad line of high reliability, regulated and short circuit protected power supplies at low overall cost. These modules are available with 5 volt to 12 volt outputs (single, dual and triple) and current ratings from 25mA to 2 amps. Most Analog Devices' Power Supplies are available from stock in both large and small quantities. Substantial discounts apply on quantity orders.

### ADVANTAGES

Packaged circuit modules have found wide acceptance. Engineers have discovered the convenience and economy of plug-in building blocks . . . op amps, logic cards, miniature A/D and D/A converters are now available in wide varieties. Now a complete line of modular power supplies is available from Analog Devices. These encapsulated units are shipped ready to use, at prices below the internal manufacturing cost of most OEM users.

### TRIPLE OUTPUT SUPPLIES — NEW

Analog Devices offers two new triple output ac/dc designs which are particularly useful in A/D, D/A and signal conditioning applications. Using a triple output supply is often less expensive than purchasing two separate supplies and also saves on space.

Model 923 is designed to provide power to data acquisition systems as well as A/D and D/A converters. The  $\pm 15V$  @  $\pm 100mA$  outputs can drive linear circuits such as op amps, while the  $+5V$  @  $500mA$  output can power the digital logic.

Model 2B35 is designed to provide regulated excitation to transducers such as strain gages, pressure transducers or load cells, as well as  $\pm 15V$  power for amplifiers and other analog circuits. The single-resistor programmable transducer excitation output may be operated in two modes: constant voltage, providing a  $+1V$  to  $+15V$  output or a constant current, adjustable from  $100\mu A$  to  $10mA$ .

### AC/DC POWER SUPPLIES FEATURES

- Current limited short circuit protection
- PC mounted and chassis mount designs
- Single, dual and triple output designs
- Current outputs of 25mA to 500mA for dual output supplies, 250mA to 2A for single output supplies
- Free-air convection cooling—no external heat sink required

### GENERAL SPECIFICATIONS FOR ALL MODELS

Input Voltage: 105V ac to 125V ac, 50 to 400Hz

Temperature Coefficient:  $0.02\%/^{\circ}C$

Input Isolation: 50 megohms

Breakdown Voltage: 500V rms, minimum

Operating Temperature:  $-25^{\circ}C$  to  $+71^{\circ}C$

Operating at elevated temperatures may require derating.

Consult factory.

Storage Temperature:  $-25^{\circ}C$  to  $+85^{\circ}C$

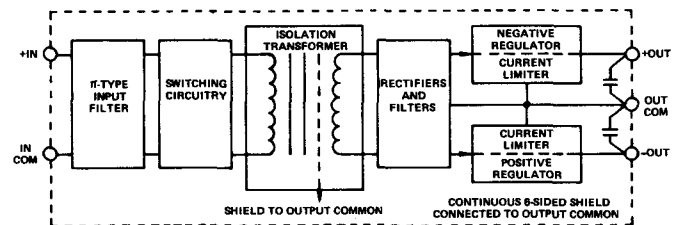
Short Circuit Protection: All of the ac/dc Power Supplies employ current limiting. They can withstand substantial overload including direct shorts. Prolonged operation should be avoided since excessive temperature rises will occur.

## Modular DC/DC Converters

Analog Devices' compact dc-dc converters satisfy a wide variety of floating power requirements in analog (Computational Circuits, Op Amps, Instrumentation Amps) and digital (a-d/d-a) applications. Available in three power levels of 1.8 watt (models 949), 4.5 watt (models 940, 941, 943, 945 and 953) and 12 watt (model 951), these designs offer accurate ( $\pm 0.05\%$  max error), regulated outputs with very low noise. Most models are high efficiency (typically over 60% at full load) that feature complete 6-sided continuous shielding for EMI/RFI protection.

### DUAL OUTPUT MODELS

Logic to analog power conversion is available with models 940, 941, 949 and 951. These modules deliver floating power ( $\pm 12V$  and  $\pm 15V$ ) from logic power sources ( $+5V$ ). This permits analog networks to be separated from digital systems in order to avoid intersystem grounding problems. Model 945 derives regulated  $\pm 15V$  outputs from any combination of inputs between 23 and 31 volts. The 945 can be powered from dual 12 volt, dual 15 volt,  $+24$  volt or  $+28$  volt power supplies.



Block Diagram — Models 940, 941, 945, 951 and 953

### DC/DC CONVERTERS FEATURES

- Inaudible ( $>20kHz$ ) converter switching frequency
- Continuous, Six-Sided EMI/RFI shielding except on model 949
- Free air convection cooling—no external heat sink or specification derating is required over operating temperature range
- Output short circuit protection (either output to common) for at least 8 hrs. at  $T_A = +71^{\circ}C$
- Automatic restart after short condition removed
- Automatic starting with reverse current injected into outputs

### GENERAL SPECIFICATIONS FOR ALL MODELS

Line Regulation—full range:  $\pm 0.05\%$  max ( $\pm 1\%$  max, 949)

Load Regulation—no load to full load:  $\pm 0.05\%$  max ( $\pm 0.5\%$  max, 949)

Output Noise and Ripple: 1mV rms max (2mV rms max, 949)

Breakdown Voltage: 500V dc minimum

Input Filter Type:  $\pi$  (except model 949)

Operating Temperature Range:  $-25^{\circ}C$  to  $+71^{\circ}C$

Storage Temperature Range:  $-40^{\circ}C$  to  $+100^{\circ}C$

# Power Supply Specifications

## MODULAR AC/DC POWER SUPPLIES

SPECIFICATIONS (typical @ +25°C and 115V ac 60Hz unless otherwise noted)

| Type             | Model         | Output Voltage Volts | Output Current mA | Line Reg. Max % | Load Reg. Max % | Output Voltage Error Max | Ripple and Noise mV rms Max | Inches Dimensions |               |
|------------------|---------------|----------------------|-------------------|-----------------|-----------------|--------------------------|-----------------------------|-------------------|---------------|
| PC Board Mounted | Dual Output   | 915                  | ±15               | ±25             | 0.2             | 0.2                      | ±1%                         | 1                 | 3.5X2.5X0.875 |
|                  |               | 904                  | ±15               | ±50             | 0.02            | 0.02                     | +200mV<br>-0mV              | 0.5               | 3.5X2.5X0.875 |
|                  |               | 902                  | ±15               | ±100            | 0.02            | 0.02                     | +300mV<br>-0mV              | 0.5               | 3.5X2.5X1.25  |
|                  |               | 902-2                | ±15               | ±100            | 0.02            | 0.02                     | +300mV<br>-0mV              | 0.5               | 3.5X2.5X0.875 |
|                  |               | 920                  | ±15               | ±200            | 0.02            | 0.02                     | +300mV<br>-0mV              | 0.5               | 3.5X2.5X1.25  |
|                  |               | 925                  | ±15               | ±350            | 0.02            | 0.02                     | ±1%                         | 0.5               | 3.5X2.5X1.62  |
|                  |               | 921                  | ±12               | ±240            | 0.02            | 0.02                     | +300mV<br>-0mV              | 0.5               | 3.5X2.5X1.25  |
|                  | Single Output | 906                  | 5                 | 250             | 0.02            | 0.04                     | ±1                          | 1                 | 3.5X2.5X0.875 |
|                  |               | 903                  | 5                 | 500             | 0.02            | 0.04                     | ±1                          | 1                 | 3.5X2.5X1.25  |
|                  |               | 905                  | 5                 | 1000            | 0.02            | 0.05                     | ±1                          | 1                 | 3.5X2.5X1.25  |
|                  |               | 922                  | 5                 | 2000            | 0.02            | 0.05                     | ±1                          | 1                 | 3.5X2.5X1.62  |
|                  | Triple Output | 923                  | ±15               | ±100            | 0.02            | 0.02                     | ±1                          | 0.5               | 3.5X2.5X1.25  |
|                  |               |                      | +5                | 500             | 0.02            | 0.05                     | ±1                          | 0.5               |               |
| 2B35J            |               | ±15                  | ±65               | 0.08            | 0.1             | (-0, +300mV)             | 0.5                         | 3.5X2.5X1.25      |               |
|                  |               | +1 to +15*           | 125               | 0.08            | 0.1             | *                        | 0.25                        |                   |               |
| 2B35K            |               | ±15                  | ±65               | 0.01            | 0.02            | (-0, +300mV)             | 0.5                         | 3.5X2.5X1.25      |               |
|                  | +1 to +15*    | 125                  | 0.01              | 0.02            | *               | 0.25                     |                             |                   |               |
| Chassis Mounted  | 952           | ±15                  | ±100              | 0.05            | 0.05            | ±2                       | 1                           | 4.4X2.7X1.44      |               |
|                  | 970           | ±15                  | ±200              | 0.05            | 0.05            | ±2                       | 1                           | 4.4X2.7X1.44      |               |
|                  | 973           | ±15                  | ±350              | 0.05            | 0.05            | ±2                       | 1                           | 4.4X2.7X2.00      |               |
|                  | 975           | ±15                  | ±500              | 0.05            | 0.05            | ±2                       | 1                           | 4.4X2.7X2.00      |               |
|                  | 955           | 5                    | 1000              | 0.05            | 0.15            | ±2                       | 2                           | 4.4X2.7X1.44      |               |

\*Resistor Programmable

## MODULAR DC/DC CONVERTERS

SPECIFICATIONS (typical @ +25°C over the full range of input voltages unless otherwise noted)

| Model | Output Voltage Volts | Output Current mA | Input Voltage Volts | Input Voltage Range Volts | Input Current Full Load | Output Voltage Error Max | Temperature Coefficient /°C Max | Efficiency Full Load Min | Dimensions Inches |
|-------|----------------------|-------------------|---------------------|---------------------------|-------------------------|--------------------------|---------------------------------|--------------------------|-------------------|
| 943   | 5                    | 1000              | 5                   | 4.65/5.5                  | 152A                    | ±1%                      | ±0.02%                          | 62%                      | 2.0 X 2.0 X 0.375 |
| 941   | ±12                  | ±150              | 5                   | 4.65/5.5                  | 1.17A                   | ±0.5%                    | ±0.01%                          | 58%                      | 2.0 X 2.0 X 0.375 |
| 949   | ±15                  | ±60*              | 5                   | 4.65/5.5                  | 0.6A                    | ±2%                      | ±0.03%                          | 58%                      | 2.0 X 1.0 X 0.375 |
| 940   | ±15                  | ±150              | 5                   | 4.65/5.5                  | 1.35A                   | ±0.5%                    | ±0.01%                          | 62%                      | 2.0 X 2.0 X 0.375 |
| 953   | ±15                  | ±150              | 12                  | 11/13                     | 0.6A                    | ±0.5%                    | ±0.01%                          | 62%                      | 2.0 X 2.0 X 0.375 |
| 945   | ±15                  | ±150              | 28                  | 23/31                     | 250mA                   | ±0.5%                    | ±0.01%                          | 61%                      | 2.0 X 2.0 X 0.375 |
| 951   | ±15                  | ±410              | 5                   | 4.65/5.5                  | 3.7A                    | ±0.5%                    | ±0.01%                          | 62%                      | 3.5 X 2.5 X 0.88  |

\*Single-ended or unbalanced operation is permissible such that total output current load does not exceed a total of 120mA.

# Products Still Available

The specifications published in this catalog are intended to assist the user in choosing components for the design of *new* equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are no longer likely to be the most economic choice for your new designs. Nevertheless, we recognize that it is often a wise choice to refrain from redesigning proven equipment, and we are continuing to make these products available for use in existing designs. Naturally, data sheets on these products are available upon request.

|               |       |                  |             |
|---------------|-------|------------------|-------------|
| 2N5900 Series | 280   | 956              | ADC-14I/17I |
| 40            | 280-1 | 971              | DAC-10H     |
| 41            | 282   | 973              | DAC1112     |
| 42            | 283   | AD108/208/308    | DAC1122     |
| 45            | 350   | AD108A/208A/308A | DSC Series  |
| 46            | 424   | AD111/211/311    | IDC Series  |
| 47            | 427   | AD351            | MDA-8H      |
| 105           | 428   | AD502            | MDA-10H     |
| 111           | 432   | AD511            | MDA-LB      |
| 118           | 440   | AD512            | MDA-LD      |
| 119           | 441   | AD514            | MDA-UB      |
| 141           | 603   | AD520            | MDA-UD      |
| 146           | 605   | AD523            | SERDEX      |
| 148           | 751   | AD530            | SMC1007     |
| 153           | 752   | AD550            | SMX1004     |
| 163           | 756   | AD553            | SMX2607     |
| 165           | 901   | AD555            | SRX1005     |
| 170           | 907   | AD801            | SRX2605     |
| 183           | 908   | AD810 Series     | STX1003     |
| 230           | 909   | AD814 Series     | STX2603     |
| 231           | 931   | AD818            |             |
| 232           | 932   | AD820 Series     |             |
| 233           | 933   | AD830 Series     |             |
| 272           | 934   | AD835 Series     |             |
| 273           | 935   | AD840 Series     |             |
| 274           | 942   | AD3900 Series    |             |
| 276           | 944   | ADC-8S           |             |
| 279           | 946   | ADC1121          |             |

# Substitution Guide for Products No Longer Available

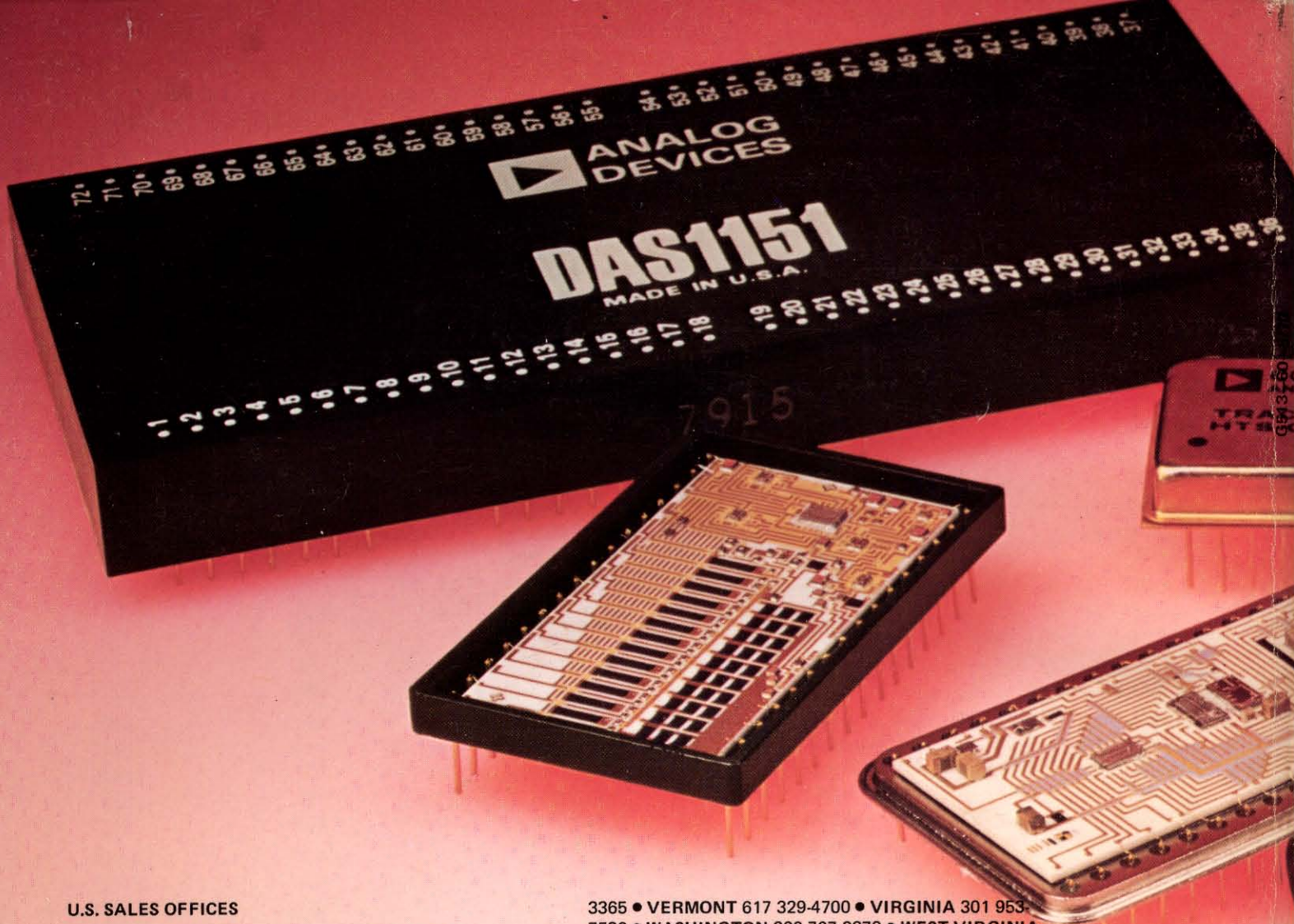
The products listed in the left-hand column below are no longer available. In many cases, comparable functions and performance may be obtained with newer models, but — as a rule — they are not directly interchangeable. The closest recommended equivalent, physically and electrically, is listed in the right-hand column.

| Model | Closest Recommended Equivalent | Model   | Closest Recommended Equivalent |
|-------|--------------------------------|---------|--------------------------------|
| 101   | 45                             | 161     | 165                            |
| 102   | 48                             | 220     | 234                            |
| 106   | 118                            | 301     | 52                             |
| 107   | 118                            | 302     | 310                            |
| 108   | 52                             | 602J10  | 610                            |
| 110   | 48                             | 602J100 | 610                            |
| 114   | 119                            | 602K100 | 610                            |
| 115   | 43                             | AD505   | AD509                          |
| 120   | 50                             | AD508   | AD517                          |
| 142   | 48                             | AD513   | AD503                          |
| 143   | 52                             | AD516   | AD506                          |
| 149   | 50                             | AD551   | AD553                          |
|       |                                | ADM501  | ADM501/506                     |

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| Model #       | Page   | Model #               | Page   | Model #                           | Page   | Model #     | Page   |
|---------------|--------|-----------------------|--------|-----------------------------------|--------|-------------|--------|
| AC2626        | 83S    | AD7520/21             | 299(C) | MDD Series                        | 185S   | 285         | 143(C) |
| AD101/201/301 |        | AD7522                | 307(C) | MDMS Series                       | 189S   | 286/281     | 147(C) |
| 301AL         | 17(C)  | AD7523                | 313(C) | MDS, MDSE, MDSL,                  |        | 288/947/948 | 53S    |
| AD363         | 317S   | AD7524                | 317(C) | MDH Series                        | 191S   | 310/311     | 97(C)  |
| AD503/506     | 21(C)  | AD7525                | 137S   | MOD1005                           | 247S   | 429         | 187(C) |
| AD504         | 25(C)  | AD7530/31             | 323(C) | MPX-8A                            | 561(C) | 433         | 191(C) |
| AD507         | 29(C)  | AD7533                | 327(C) | RTI-1200                          | 573(C) | 434         | 195(C) |
| AD509         | 33(C)  | AD7541                | 333(C) | RTI-1201                          | 577(C) | 435         | 199(C) |
| AD510         | 37(C)  | AD7550                | 411(C) | RTI-1220/1221                     | 581(C) | 436         | 203(C) |
| AD515         | 21S    | AD7570                | 419(C) | RTI-1240/41/42/<br>43             | 585(C) | 442         | 235(C) |
| AD517         | 27S    | AD ADC80              | 223S   | SAC1763                           | 269S   | 450/54/56   | 481(C) |
| AD518         | 53(C)  | ADC1100               | 431(C) | SBCD1752/1753/<br>1756/1757       | 271S   | 451/53      | 485(C) |
| AD521         | 47S    | ADC1102               | 435(C) | SCDX Series                       | 504(C) | 452         | 491(C) |
| AD522         | 113(C) | ADC1103               | 437(C) | SCM1677                           | 275S   | 458/60      | 495(C) |
| AD528         | 57(C)  | ADC1105               | 441(C) | SDC1700/1702/<br>1704             | 277S   | 606         | 117(C) |
| AD531         | 161(C) | ADC1109               | 447(C) | SDC1725/1726                      | 283S   | 610         | 121(C) |
| AD532         | 169(C) | ADC1121               | 449(C) | SHA-1A                            | 517(C) | 610         | 121(C) |
| AD533         | 175(C) | ADC1130/1131          | 453(C) | SHA-2A                            | 519(C) | 902-2       | 333S   |
| AD534         | 179(C) | ADC1133               | 457(C) | SHA-3/4/5                         | 523(C) | 903         | 333S   |
| AD535         | 59S    | ADC-141/171           | 459(C) | SHA-6                             | 525(C) | 904         | 333S   |
| AD536A        | 65S    | ADC-16Q               | 463(C) | SHA1134                           | 529(C) | 905         | 333S   |
| AD537         | 251S   | ADC-12QZ              | 467(C) | SHA1144                           | 299S   | 906         | 333S   |
| AD540         | 61(C)  | AD DAC-08             | 143S   | SMC1007                           | 564(C) | 907         | 594(C) |
| AD542         | 33S    | AD DAC80              | 147S   | SMX1004                           | 564(C) | 908         | 594(C) |
| AD544         | 37S    | AD DAC85              | 155S   | SMX2607                           | 564(C) | 915         | 333S   |
| AD545         | 41S    | AD DAC87              | 163S   | SPA1695                           | 287S   | 920         | 333S   |
| AD559         | 277(C) | ADG200                | 309S   | SRX1005                           | 564(C) | 921         | 333S   |
| AD561         | 113S   | ADG201                | 313S   | SRX2605                           | 564(C) | 922         | 333S   |
| AD562/563     | 289(C) | BDM1615/1616/<br>1617 | 259S   | SSCT Series                       | 504(C) | 923         | 333S   |
| AD565         | 121S   | DAC1009               | 339(C) | STX1003                           | 564(C) | 925         | 333S   |
| AD566         | 129S   | DAC1106/08            | 343(C) | STX2603                           | 564(C) | 934         | 594(C) |
| AD570         | 199S   | DAC1118               | 347(C) | THS, THC Series                   | 305S   | 940         | 333S   |
| AD571         | 207S   | DAC1125               | 349(C) | TSL1612/TSDC1608<br>thru TSDC1611 | 289S   | 941         | 333S   |
| AD572         | 395(C) | DAC1132               | 353(C) | 48                                | 69(C)  | 942         | 596(C) |
| AD574         | 215S   | DAC1136/1137/<br>1138 | 167S   | 50/51                             | 71(C)  | 943         | 333S   |
| AD580         | 241(C) | DAC1422               | 179S   | 52                                | 75(C)  | 944         | 596(C) |
| AD581         | 71S    | DAC-10DF              | 365(C) | 171                               | 77(C)  | 945         | 333S   |
| AD582         | 509(C) | DAC-QM/QG             | 367(C) | 2B20                              | 93S    | 946         | 596(C) |
| AD583         | 513(C) | DAC-QM/QS             | 373(C) | 2B22                              | 97S    | 949         | 333S   |
| AD584         | 77S    | DAC-12QZ              | 375(C) | 2B30/31                           | 101S   | 951         | 333S   |
| AD590         | 85S    | DAC-10Z/<br>MDA-10Z   | 377(C) | 2B35                              | 107S   | 952         | 333S   |
| AD741         | 65(C)  | DAS1128               | 565(C) | 234                               | 81(C)  | 953         | 333S   |
| AD1408/1508   | 295(C) | DAS1150/1151          | 329S   | 235                               | 85(C)  | 955         | 333S   |
| AD2020        | 403(C) | DSC1705/1706          | 261S   | 260                               | 89(C)  | 956         | 595(C) |
| AD2023        | 407(C) | DTM1716/1717          | 265S   | 261                               | 91(C)  | 970         | 333S   |
| AD2036        | 259(C) | HAS Series            | 231S   | 275                               | 129(C) | 973         | 333S   |
| AD2037/AD2038 | 109S   | HDS, HDH Series       | 179S   | 277                               | 133(C) | 975         | 333S   |
| AD2040        | 111S   | HOS Series            | 45S    | 284                               | 137(C) |             |        |
| AD2700/01/02  | 265(C) | HTS, HTC Series       | 293S   |                                   |        |             |        |
| AD7501/02/03  | 537(C) | IDC Series            | 504(C) |                                   |        |             |        |
| AD7506/07     | 541(C) | MAS Series            | 235S   |                                   |        |             |        |
| AD7510DI      | 545(C) | MATV Series           | 241S   |                                   |        |             |        |
| AD7513        | 553(C) |                       |        |                                   |        |             |        |
| AD7516        | 557(C) |                       |        |                                   |        |             |        |
| AD7519        | 559(C) |                       |        |                                   |        |             |        |





**U.S. SALES OFFICES**

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