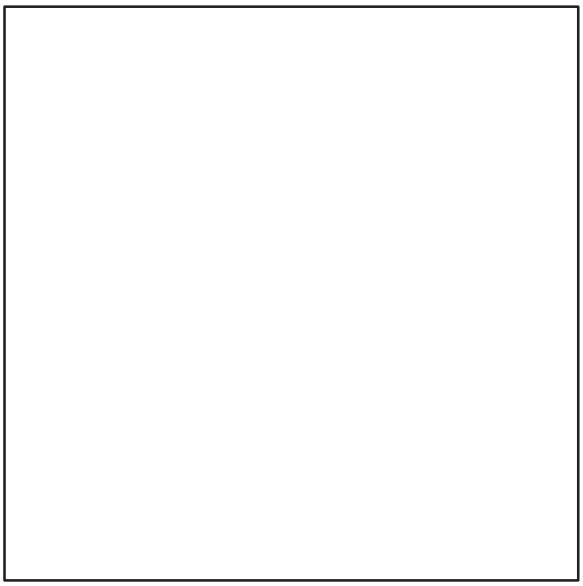
MOTOROLA

DL111/D
REV 7

Bipolar Power

Transistor Data



MOTOROLA

Bipolar Power Device Data

This book presents technical data for Motorola's broad line of silicon power transistors. Complete specifications are provided in the form of data sheets and accompanying selection guides which provide a quick comparison of characteristics to simplify the task of choosing the best device for a circuit.

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. Please consult your nearest Motorola Semiconductor sales office for further assistance regarding any aspect of Motorola Bipolar Power Transistor products.

Printed in U.S.A.

Data Sheet Fax via Touch–Tone Phone

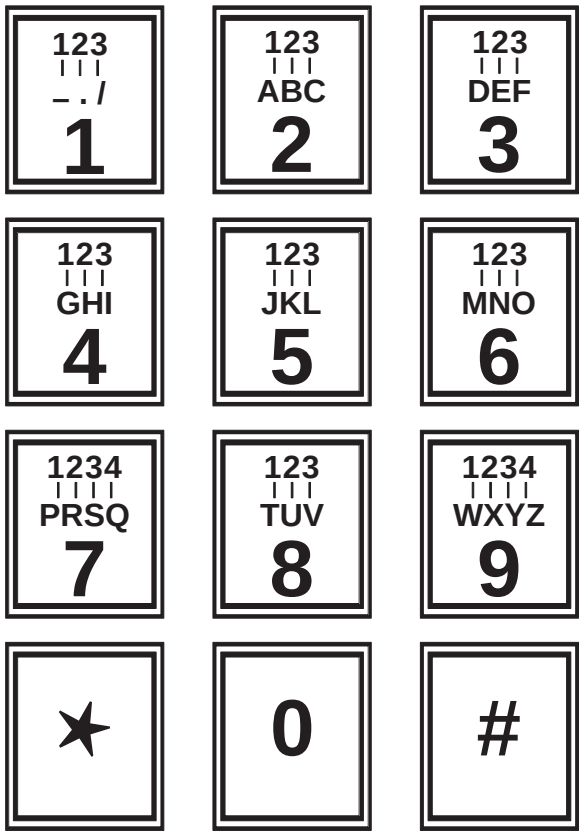
Motorola's **M*fax***SM system is as easy to use as dialing your touch–tone telephone. Your touch–tone phone becomes your link to ordering over 30,000 documents available for faxing. A fax of complete, easy–to–use instructions can be obtained with a first–time phone call into the system.

The combination of letters and numbers on the keypad will deliver faxes to your machine.

Number or letter strings entered for requests are ended with the use of the # sign.

Use 2–digit combinations when numbers entered are part of a part number.
EXAMPLE:
981 is entered:
09 08 01#
9 = 09
8 = 08
1 = 01

While keying 2–digit strings, the system will repeat back the entered letter or number.



Letters are entered with 2–digit combinations.
EXAMPLE:
DBL is entered:
31 22 53#
D = 31
B = 22
L = 53

The position of the letters on the keys determines the numbers entered. For instance MNO would be:
61 62 63#
M = 61–key 6 position 1
N = 62–key 6 position 2
O = 63–key 6 position 3

EXAMPLE:
A requested document, MC6530 is entered:
61 23 06 05 03 00#
M = 61
C = 23
6 = 06
5 = 05
3 = 03
0 = 00

Motorola's **M*fax*** system repeats letter and number combinations as they are entered so changes for keys touched in error can be corrected. Complete help is available throughout the instructions when you dial into the system at **602–244–6609**. A Personal Identification Number (PIN) is assigned to you to speed up ordering of faxes.

MOTOROLA
POWER TRANSISTORS
IN BRIEF

Wide Range of Transistor Specifications

Motorola offers more than 700 standard (off–the–shelf) power transistors to cover the widest range of applications at the lowest cost.

Current Range — 0.1 to 80 Amperes
Voltage Range — 25 to 1800 Volts
Power Dissipation Range — 5 to 250 Watts.

Darlingtons

Darlington transistors represent the integral high gain circuits of the power field. Consisting of two transistors, two resistors, and (up to) two diodes, they achieve gain figures up to 20,000 in a single package. Widespread implementation of Motorola Darlingtons can be highly cost–effective in a fast growing number of applications.

Specials

Implementation of six sigma quality, statistical process control, and overall customer satisfaction programs at Motorola are producing tighter electrical distributions and specifications on all standard devices. Future standard device introductions will have tighter specifications and offer high volume economy, thereby reducing or eliminating the need for specifically selected devices.

Specials will continue to be reviewed, but will require minimum order quantities and minimum yearly run rates. Check with your Motorola Sales Representative for more information on special devices.

Portfolio Management

Six Sigma Program implementation is also allowing the portfolio to be condensed by elimination of devices which are no longer actually produced because of the tighter parametric distributions. Low voltage and unpopular gain devices are now being deleted and others, categorized as non–preferred, may eventually be eliminated as well. **Preferred types** are shown in the selector guide section in **bold type**. Replacements, most of them direct, for the eliminated and non–preferred types are indicated in the Alphanumeric Index/Cross–reference included in this selector guide.

What's Different

Additions:

MJE15032
MJE15033
MJE18002D2
MJE18004D2
MJE18009
MJF18009
MJE18204
MJF18204
MJE18206
MJF18206
MJE18604D2
BUD43B
BUD44D2
BUH50
BUH51
BUH100
BUH150
BUL43B
BUL44D2
BUL45D2

Deletions:

2N3054
2N3054A
2N3441
2N3447
2N3584
2N3585
2N3719
2N3720
2N3738
2N3739
2N3740
2N3741
2N3741A
2N3766
2N3767
2N3867
2N3868
2N4233A
2N4240
2N4347
2N4912
2N5428
2N5430
2N5683
2N5875
2N5876
2N6053
2N6054
2N6190
2N6191
2N6193
2N6211
2N6212
2N6213
2N6294
2N6295
2N6296
2N6297
2N6298
2N6299
2N6300
2N6301
2N6303
2N6317
2N6318
2N6377
2N6378
2N6421
2N6678
2N6833
2N6837
2SA1302
2SA1306B
2SC3281
2SC3298B
BD235
BD236
BD239A
BD239B
BD239C
BD240A
BD240B
BD240C
BD241A
BD242A
BD243A
BD244A
BD779
BD797
BD798
BD799
BD800
BD807
BD809
BD897
BD897A
BD898
BD898A
BD899
BD899A
BD900
BD900A
BD901
BD902
BDW40
BDW41
BDW45
BDX33A
BDX34A
BDX53A
BDX54A
BU223Z
BU406D
BU407D
BU508A
BU522
BU522A
BU807
BUS51
BUT13
BUT50P
BUT51P
BUV24
BUX39
BUX40
BUX41N
D44C12
D44E3
MJ900
MJ901
MJ3041
MJ10001
MJ10004
MJ10006
MJ10008
MJ10014
MJ10024
MJ10025
MJ11011
MJ11019
MJ11020
MJ13014
MJ13015
MJ13335
MJ14000
MJ16002A
MJH16002A
MJ16006
MJH16006
MJ16008
MJH16008
MJ16006A
MJ16010A
MJ16014
MJ16016
MJ4646
MJ4647
MJ6308
MJ6503
MJD148
MJD44E3
MJD5731
MJD13003
MJE240
MJE241
MJE250
MJE251
MJE252
MJE5420Z
MJF10012
MJF16002
MJF16006A
MJF16010A
MJF16204
MJF16206
MJF16210
MJF16212
MJH16002
MJH16004
MJH16106
MJW16210
MJW6678
MPSU01
MPSU01A
MPSU02
MPSU03
MPSU04
MPSU05
MPSU06
MPSU07
MPSU10
MPSU45
MPSU51
MPSU51A
MPSU52
MPSU55
MPSU56
MPSU57
MPSU60
MPSU95

Index and Cross Reference

The table on the subsequent pages contains an Alphanumeric index of Silicon power transistors currently manufactured and available to the industry. The column headed “Similar” lists units with characteristics that might represent suitable replacements. In cases where such a replacement is contemplated, the Motorola device data sheet should be carefully compared with one for the device being replaced to determine any variations that could affect circuit performance.

INDEX AND CROSS REFERENCE

The following table represents an index and cross–reference guide for all low–frequency power transistors which are either manufactured directly by Motorola or for which Motorola manufactures a suitable equivalent. Where the Motorola part number differs from the industry part number, the Motorola device is a “form, fit and function” replacement for the industry type number — however, subtle differences in characteristics and/or specifications may exist. Where multiple replacement parts appear for a given industry part number, the page number represents the first replacement device listed.

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement	Page Number
40251		2N3055	3–2
40325		2N3055	3–2
40363		2N5878	3–74
40369		2N5878	3–74
40411		MJ802	3–421
40513		MJE3055T	3–628
40514		MJE3055T	3–628
40542		MJE3055T	3–628
40543		MJE3055T	3–628
40613		TIP31B	3–873
40618		TIP31B	3–873
40621		TIP31B	3–873
40622		TIP31B	3–873
40624		TIP41B	3–883
40627		TIP41B	3–883
40629		TIP31B	3–873
40630		TIP31B	3–873
40631		TIP31B	3–873
40632		TIP41B	3–883
40636		2N5878	3–74
40853		2N6547	3–140
40854		2N6547	3–140
40871		TIP41C	3–883
40872		TIP42C	3–883
40873		TIP41B	3–883
40874		TIP41B	3–883
40875		TIP41C	3–883
40876		TIP41B	3–883
40887		MJE340	3–602
41012		2N5038	3–42
41013		2N6339	3–117
41500		TIP31B	3–873
41501		TIP32B	3–873
41504		TIP31B	3–873
43104		2N5631	3–59
1SI10A–100		MJ16018	3–520
2N1487		2N5878	3–74
2N1488		2N5878	3–74
2N1489		2N5878	3–74
2N1490		2N5878	3–74
2N1702		2N5878	3–74
2N3021		2N3792	3–25
2N3022		2N3792	3–25
2N3023		2N3792	3–25
2N3024		2N3792	3–25
2N3025		2N3792	3–25
2N3026		2N3792	3–25
2N3055	2N3055		3–2
2N3055A	2N3055A		3–5

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement	Page Number
2N3055H		2N3055A	3–5
2N3055SD		2N3055A	3–5
2N3055UB		2N3055A	3–5
2N3076		BUV23	3–388
2N3171		2N3792	3–25
2N3172		2N3792	3–25
2N3173		2N3792	3–25
2N3174		MJ15016	3–5
2N3183		2N3792	3–25
2N3184		2N3792	3–25
2N3185		2N3792	3–25
2N3186		MJ15016	3–5
2N3195		2N3792	3–25
2N3196		2N3792	3–25
2N3198		MJ15016	3–5
2N3232		2N5878	3–74
2N3233		2N5882	3–77
2N3234		2N3442	3–9
2N3235		2N3055	3–2
2N3236		2N5882	3–77
2N3237		2N5302	3–54
2N3238		2N5882	3–77
2N3239		2N5882	3–77
2N3240		2N5882	3–77
2N3441	2N3442		3–9
2N3442	2N3442		3–9
2N3445		2N3716	3–12
2N3446		2N3716	3–12
2N3447		2N3716	3–12
2N3448		2N3716	3–12
2N3667		2N5882	3–77
2N3713		2N5882	3–77
2N3714	2N3716		3–12
2N3715	2N3716		3–12
2N3716	2N3716		3–12
2N3771	2N3771		3–17
2N3772	2N3772		3–17
2N3773	2N3773		3–21
2N3789	2N3792		3–25
2N3790	2N3792		3–25
2N3791	2N3792		3–25
2N3792	2N3792		3–25
2N3863		2N3716	3–12
2N3864		2N5882	3–77
2N3865		MJ15001	3–497
2N3902		BUX48A	3–401
2N4002		2N6274	3–108
2N4032		2N6274	3–108
2N4111		2N3716	3–12

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Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement	Page Number
2N4113		2N3716	3–12
2N4347		2N3055A	3–5
2N4348		2N5631	3–59
2N4398	2N4399		3–29
2N4399	2N4399		3–29
2N4901		MJ15016	3–5
2N4902		MJ15016	3–5
2N4903		MJ15016	3–5
2N4904		MJ15016	3–5
2N4905		MJ15016	3–5
2N4906		MJ15016	3–5
2N4907		2N3792	3–25
2N4908		2N3792	3–25
2N4909		2N3792	3–25
2N4918	2N4918		3–34
2N4919	2N4919		3–34
2N4920	2N4920		3–34
2N4921	2N4921		3–38
2N4922	2N4922		3–38
2N4923	2N4923		3–38
2N5034		2N3055	3–2
2N5035		2N3055	3–2
2N5036		2N3055	3–2
2N5037		2N3055	3–2
2N5038	2N5038		3–42
2N5039	2N5038		3–42
2N5157		BUX48A	3–401
2N5190	2N5191		3–44
2N5191	2N5191		3–44
2N5192	2N5192		3–44
2N5193	2N5194		3–49
2N5194	2N5194		3–49
2N5195	2N5195		3–49
2N5240		BUX48A	3–401
2N5241		BUX48A	3–401
2N5264		BUV23	3–388
2N5293		TIP31B	3–873
2N5294		TIP31B	3–873
2N5295		TIP31B	3–873
2N5296		TIP31B	3–873
2N5297		TIP31B	3–873
2N5298		TIP31B	3–873
2N5301	2N5302		3–54
2N5302	2N5302		3–54
2N5303	2N5303		3–54
2N5386		2N5038	3–42
2N5387		2N6547	3–140
2N5388		2N6547	3–140
2N5389		2N6547	3–140
2N5466		BUX48A	3–401
2N5467		BUX48A	3–401
2N5490		MJE3055T	3–628
2N5491		MJE3055T	3–628
2N5492		2N6292	3–101
2N5493		2N6292	3–101
2N5494		MJE3055T	3–628
2N5495		MJE3055T	3–628
2N5496		2N6292	3–101
2N5497		2N6292	3–101
2N5559		MJ15001	3–497
2N5575		2N5685	3–66
2N5578		2N5685	3–66
2N5614		2N3716	3–12

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement	Page Number
2N5616		2N3716	3–12
2N5618		2N3716	3–12
2N5629		2N5631	3–59
2N5630	2N5631		3–59
2N5631	2N5631		3–59
2N5632		2N5882	3–77
2N5633		MJ15001	3–497
2N5634		MJ15001	3–497
2N5655	2N5657		3–63
2N5656	2N5657		3–63
2N5657	2N5657		3–63
2N5659		2N5631	3–59
2N5683	2N5684		3–66
2N5684	2N5684		3–66
2N5685	2N5685		3–66
2N5686	2N5686		3–66
2N5733		2N6274	3–108
2N5734		2N6338	3–117
2N5737		2N5878	3–74
2N5738		2N5880	3–77
2N5739		2N5878	3–74
2N5740		2N5880	3–77
2N5741		2N5884	3–81
2N5742		2N6031	3–59
2N5743		2N5884	3–81
2N5744		MJ4502	3–431
2N5745	2N5745		3–29
2N5758	2N5758		3–70
2N5759		2N3055A	3–5
2N5760		2N3442	3–9
2N5867		2N3792	3–25
2N5868		2N3792	3–25
2N5869		2N3716	3–12
2N5870		2N3716	3–12
2N5871		2N3792	3–25
2N5872		2N3792	3–25
2N5873		2N3716	3–12
2N5874		2N3716	3–12
2N5877	2N5878		3–74
2N5878	2N5878		3–74
2N5879	2N5880		3–77
2N5880	2N5880		3–77
2N5881	2N5882		3–77
2N5882	2N5882		3–77
2N5883	2N5884		3–81
2N5884	2N5884		3–81
2N5885	2N5886		3–81
2N5886	2N5886		3–81
2N5929		2N6338	3–117
2N5930		2N6338	3–117
2N5931		2N6341	3–117
2N5932		2N6338	3–117
2N5933		2N6338	3–117
2N5935		2N6341	3–117
2N5936		2N6338	3–117
2N5937		2N6341	3–117
2N5970		2N5882	3–77
2N5971		2N5882	3–77
2N5972		MJ15003	3–500
2N5973		2N5886	3–81
2N5974		MJE2955T	3–628
2N5975		MJE2955T	3–628
2N5976		MJE2955T	3–628

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Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement	Page Number
2N5977		MJE3055T	3–628
2N5978		MJE3055T	3–628
2N5979		MJE3055T	3–628
2N5980		MJE2955T	3–628
2N5981		MJE2955T	3–628
2N5982		2N6490	3–132
2N5983		MJE3055T	3–628
2N5984		MJE3055T	3–628
2N5985		2N6488	3–132
2N5986		2N6490	3–132
2N5987		2N6490	3–132
2N5988		2N6490	3–132
2N5989		2N6486	—
2N5990		2N6488	3–132
2N5991		2N6488	3–132
2N6021		TIP32C	3–873
2N6022		TIP32C	3–873
2N6023		TIP32B	3–873
2N6024		TIP32B	3–873
2N6025		TIP32B	3–873
2N6026		TIP32B	3–873
2N6029		2N6031	3–59
2N6030	2N6031		3–59
2N6031	2N6031		3–59
2N6032		2N6275	3–108
2N6033		2N6277	3–108
2N6034	2N6035		3–85
2N6035	2N6035		3–85
2N6036	2N6036		3–85
2N6037	2N6038		3–85
2N6038	2N6038		3–85
2N6039	2N6039		3–85
2N6040	2N6041		3–89
2N6041	2N6041		3–89
2N6042	2N6042		3–89
2N6043	2N6044		3–89
2N6044	2N6044		3–89
2N6045	2N6045		3–89
2N6049	2N6049		—
2N6050	2N6052		3–93
2N6051	2N6052		3–93
2N6052	2N6052		3–93
2N6055	2N6056		3–97
2N6056	2N6056		3–97
2N6057	2N6059		3–93
2N6058	2N6059		3–93
2N6059	2N6059		3–93
2N6098		2N6487	3–132
2N6099		2N6487	3–132
2N6100		2N6487	3–132
2N6101		2N6488	3–132
2N6102		2N6488	3–132
2N6103		2N6487	3–132
2N6106		2N6107	3–101
2N6107	2N6107		3–101
2N6108		2N6109	3–101
2N6109	2N6109		3–101
2N6110		2N6107	3–101
2N6111	2N6107		3–101
2N6121		TIP31B	3–873
2N6122		TIP31B	3–873
2N6123		TIP31B	3–873
2N6124		TIP32B	3–873

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement	Page Number
2N6125		TIP32B	3–873
2N6126		TIP32C	3–873
2N6127		2N6437	3–128
2N6128		2N6338	3–117
2N6129		TIP41B	3–883
2N6130		TIP41B	3–883
2N6131		TIP41B	3–883
2N6132		TIP42C	3–883
2N6133		TIP42C	3–883
2N6134		TIP42C	3–883
2N6177		MJE340	3–602
2N6226		MJ15016	3–5
2N6227		MJ15016	3–5
2N6228		MJ15016	3–5
2N6229		2N5880	3–77
2N6230		MJ15002	3–497
2N6231		MJ15002	3–497
2N6246		2N5880	3–77
2N6247		2N5880	3–77
2N6248		MJ15016	3–5
2N6249		BUV23	3–388
2N6250		BUV23	3–388
2N6253		2N5878	3–74
2N6254		2N5878	3–74
2N6257		2N5886	3–81
2N6258		2N5686	3–66
2N6259		2N5631	3–59
2N6262		2N3442	3–9
2N6270		2N6338	3–117
2N6271		2N6338	3–117
2N6272		2N6338	3–117
2N6273		2N6338	3–117
2N6274	2N6274		3–108
2N6275	2N6275		3–108
2N6276		2N6275	3–108
2N6277	2N6277		3–108
2N6278		2N6274	3–108
2N6279		2N6275	3–108
2N6280		2N6275	3–108
2N6281		2N6277	3–108
2N6282	2N6283		3–112
2N6283	2N6283		3–112
2N6284	2N6284		3–112
2N6285	2N6286		3–112
2N6286	2N6286		3–112
2N6287	2N6287		3–112
2N6288	2N6292		3–101
2N6289		2N6292	3–101
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SVT7551		MJ16010	3–512
SVT7552		MJ16010	3–512
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SVT7554		MJ16010	3–512
SVT7555		MJ16010	3–512
SVT7560		MJ16010	3–512
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SVT7563		MJ16110	3–529
SVT7564		MJ16110	3–529
SVT7565		MJ16110	3–529
SVT7570		MJ16010	3–512
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SVT7573		MJ16110	3–529
SVT7574		MJ16110	3–529
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TIP30	TIP30C		3–871
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TIP30A	TIP30C		3–871
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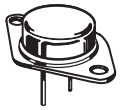
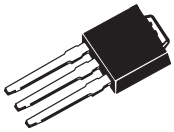
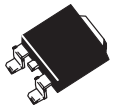
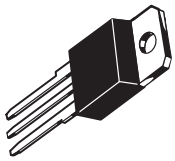
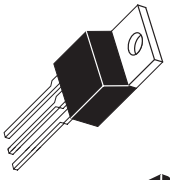
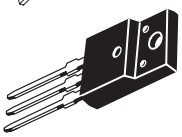
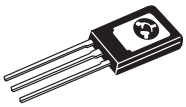
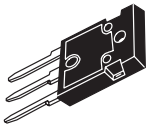
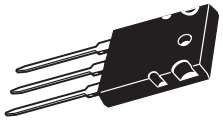
Selector Guide

The selector guides on the subsequent pages offer a quick “first–selection” capability for devices that fit specific applications categories.

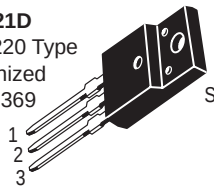
1. by package
2. by major product category
3. by major applications

In each case, pertinent electrical characteristics are supplied to permit rapid comparison of potentially suitable devices.

Bipolar Power Transistors
Selection by Package

Package		I_C Range (Amps)	V_{CE} Range (Volts)	P_D (Watts)	Page #
	**TO–204AA (TO–3) CASE 1–07**	4–30	40–1500	90–250	5.5–12
	**TO–204AE CASE 197A**	50–80	60–1000	150–300	5.5–12
	**DPAK CASE 369**	0.5–10	40–400	12.5–20	5.5–11
	**DPAK CASE 369A**	0.5–10	40–400	12.5–20	5.5–11
	**TO–218 TYPE CASE 340D**	5.0–25	60–1500	80–150	5.5–7
	**TO–220AB CASE 221A–06**	0.5–15	30–1800	30–125	5.5–4
	**ISOLATED TO–220 TYPE CASE 221D**	1–12	80–450	20–45	5.5–3
	**TO–225AA (TO–126 TYPE) CASE 77**	0.3–5.0	25–400	12.5–40	5.5–9
	**TO–247 TYPE CASE 340F**	10–30	400–1500	125–180	5.5–8
	**TO–264 CASE 340G**	15–16	200–650	250	5.5–9

CASE 221D
Isolated TO–220 Type
UL Recognized
File #E69369



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

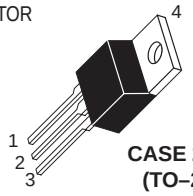
Table 1. Plastic (Isolated TO–220 Type)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
			NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
1	250		***MJF47***		30/150	0.3	2 typ	0.17 typ	0.3	10	28
2	400	700	***BUL44F***		14/34	0.2	2.75(3)	0.2(3)	1	13 typ	25
		1000	***MJF18002***		14/34	0.2	2.75(3)	0.175(3)	1	13 typ	25
3	100		***MJF31C***	***MJF32C***	10 min	1	0.6	0.3	1	3	28
5	100		***MJF122***(2)	***MJF127***(2)	2000 min	3	1.5 typ	1.5 typ	3	4(1)	28
	400	700	***BUL45F***		14/34	0.3	1.7(3)	0.15(3)	1	12 typ	35
	450	1000	***BUT11AF***		10 min	.005	4	0.8	2.5		40
		1000	***MJF18004***		14/34	0.3	1.7(3)	0.15(3)	1	13 typ	35
	550	1200	***MJF18204***		18/35	0.5	2.75(3)	0.2(3)	2	12	35
6	400	700	***BUL146F***		14/34	0.5	2.5(3)	0.15(3)	3	14 typ	40
	450	1000	***MJF18006***		14/34	0.5	3.2(3)	0.15(3)	3	14 typ	40
8	80			***MJF6107***	30/90	2	0.5 typ	0.13 typ	2	4	35
	150		***MJF15030***	***MJF15031***	40 min	3	1 typ	0.15 typ	3	30	35
	400	700	***MJF13007***		5/30	5	3	0.7	5	4	40
			BUL147F		14/34	1	2.5(3)	0.18(3)	2	14 typ	45
	450	1000	***MJF18008***		16/34	1	2.75(3)	0.18(3)	2	13 typ	45
10	60		***MJF3055***	***MJF2955***	20/100	4	—	—	—	2	40
	80		***MJF44H11***	***MJF45H11***	40/100	4	0.5 typ	0.14 typ	5	40	35
	100		***MJF6388***(2)	***MJF6668***(2)	3k/20k	3	1.5 typ	1.5 typ		20(1)	40
	450	1000	***MJF18009***		14/34	1.5	2.75(3)	0.2(3)	3	12	50
12	400	700	***MJF13009***		6/30	8	3	0.7	8	8	40

(1)$|h_{FE}|$ @ 1 MHz
(2)Darlington
(3)Switching tests performed w/special application simulator circuit. See data sheet for details.

Devices listed in bold, italic are Motorola preferred devices.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



CASE 221A–06
(TO–220AB)

Table 2. Plastic TO–220AB

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min(8)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
0.5	350	MJE2360T		15 min	0.1				10 typ	30
		MJE2361T		40 min	0.1				10 typ	30
1	100	TIP29C	TIP30C	15/75	1	0.6 typ	0.3 typ	1	3	30
	250	TIP47		30/150	0.3	2 typ	0.18 typ	0.3	10	40
	300	TIP48	MJE5730	30/150	0.3	2 typ	0.18 typ	0.3	10	40
	350	***TIP49***	***MJE5731***	30/150	0.3	2 typ	0.18 typ	0.3	10	40
	400	***TIP50***	***MJE5731A***(7)	30/150	0.3	2 typ	0.18 typ	0.3	10	40
2	100	***TIP112***(2)	***TIP117***(2)	500 min	2	1.7 typ	1.3 typ	2	25(1)	50
	400/700	***BUL44***		14/36	0.4	2.75(3)	0.175(3)	1	13 typ	50
	450/1000	***BUX85***		30	0.1	3.5	1.4	1	4	50
	450/1000	***MJE18002***		14/34	0.2	3(3)	0.17(3)	1	12 typ	40
	900/1800	***MJE1320***		3 min	1	4 typ	0.8 typ	1		80
3	80	BD241B	BD242B	25 min	1				3	40
	100	BD241C	BD242C	25 min	1				3	40
		TIP31C	***TIP32C***	25 min	1	0.6 typ	0.3 typ	1	3	40
	150		***MJE9780***	50/200	0.5				5 typ	40

(1)$|h_{FE}|$ @ 1 MHz
(2)Darlington
(3)Switching tests performed w/special application simulator circuit. See data sheet for details.
(7)V_{CEO} = 375 V
(8)When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

Devices listed in bold, italic are Motorola preferred devices.

Table 2. Plastic TO–220AB (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min(8)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
4	40		***MJE1123***	45/100	4				5	75
	60	***MJE800***(2)	***MJE700***(2)	750 min	1.5				1(1)	40
	80	***D44C12***	***D45C12***	40/120	0.2			1	40 typ	30
	400/700	***MJE13005***		6/30	3	3	0.7	3	4	60
5	100	***TIP122***(2)	***TIP127***(2)	1k min	3	1.5 typ	1.5 typ	4	4(1)	75
	250	2N6497		10/75	2.5	1.8	0.8	2.5	5	80
	300	***2N6498***		10/75	2.5	1.8	0.8	2.5	5	80
	400/700	***BUL45***		14/34	0.3	1.7(3)	0.15(3)	1	12 typ	75
	450/1000	MJE16002		5 min	5	3	0.3	3		80
	450/850	***MJE16004***		7 min	5	2.7	0.35	3		80
	450/1000	***MJE18004***		14/34	0.3	1.7	0.15	1.0	13	75
	550/1200	***MJE18204***		18/35	0.5	2.75(3)	0.2(3)	2	12	75
6	80	***BD243B***	***BD244B***	15 min	3	0.4 typ	0.15 typ	3	3	65
	100	***BD243C***	***BD244C***	15 min	3	0.4 typ	0.15 typ	3	3	65
		TIP41C	***TIP42C***	15/75	3	0.4 typ	0.15 typ	3	3	65
	250/550	***MJE16204***		5 min	6	1.5(2)	0.15(2)	1	10	80
	400/700	***BUL146***		14/34	0.5	1.75(3)	0.15(3)	3	14 typ	100
	450/1000	***MJE18006***		14/34	0.5	3.2(3)	0.13(3)	3	14 typ	100
7	30	2N6288	2N6111	30/150	3	0.4 typ	0.15 typ	3	4	40
	50		2N6109	30/150	2.5	0.4 typ	0.15 typ	3	4	40
	70	***2N6292***	***2N6107***	30/150	2	0.4 typ	0.15 typ	3	4	40
	100	***BD801***	***BD802***	15 min	3				3	65
	150	BU407		30 min	1.5		0.75	5	10	60
	200	***BU406***		30 min	1.5		0.75	5	10	60
	450	***BU522B***(2)		250 min	2.5				7.5	75

(1)$|h_{FE}|$ @ 1 MHz
(2)Darlington
(3)Switching tests performed w/special application simulator circuit. See data sheet for details.
(7)V_{CEO} = 375 V
(8)When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

Devices listed in bold, italic are Motorola preferred devices.

Table 2. Plastic TO–220AB (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min(8)	Device Type NPN	Device Type PNP	h_{FE} Min/Max	@ I_C Amp	Resistive Switching t_s µs Max	Resistive Switching t_f µs Max	Resistive Switching @ I_C Amp	f_T MHz Min	P_D (Case) Watts @ 25°C
8	60	2N6043(2)	2N6040(2)	1k/10k	4	1.5 typ	1.5 typ	3	4(1)	75
	80	***2N6044***(2)	***2N6041***(2)	1k/10k	4	1.5 typ	1.5 typ	3	4(1)	75
		BDX53B(2)	***BDX54B***(2)	750 min	3				4(1)	60
	100	***2N6045***(2)	***2N6042***(2)	1k/10k	3	1.5 typ	1.5 typ	3	4(1)	75
		BDX53C(2)	***BDX54C***(2)	750 min	3					
		TIP102(2)	***TIP107***(2)	1k/20k	3	1.5 typ	1.5 typ	3	4(1)	80
	120	MJE15028	MJE15029	20 min	4				30	50
	150	***MJE15030***	***MJE15031***	20 min	4				30	50
	200	***BU806***(2)		100 min	5	0.55 typ	0.2 typ	5		60
	300/600	MJE5740(2)		200 min	4	8 typ	2 typ	6	4	80
			MJE5850	15 min	2	2	0.5	4		80
	350	***MJE5741***(2)		200 min	4	8 typ	2 typ	6		80
			MJE5851	15 min	2	2	0.5	4		80
		MJE5742(2)		200 min	4	8 typ	2 typ	6		80
		MJE13007		5/30	5	3	0.7	5		80
			MJE5852	15 min	2	2	0.5	4		80
	400/650	***MJE16106***		6/22	8	2 typ	0.1 typ	5		100
	400/700	***BUL147***		14/34	1	2.5(3)	0.18(3)	2	14 typ	125
	450/1000	***MJE18008***		16/34	1	2.75(3)	0.18(3)	2	13 typ	125
10	20		***BD808***	15 min	4				1.5	90
	60	D44H8	D45H8	40 min	4					50
		MJE3055T	***MJE2955T***	20/70	4					75
		2N6387(2)	***2N6667***(2)	1k/20k	5				20(1)	65
	80	***BDX33B***(2)	***BDX34B***(2)	750 min	3				3	70
		BD809	***BD810***	15 min	4				1.5	90
		2N6388(2)	***2N6668***(2)	1k/20k	5				20(1)	65
		D44H10	D45H10	20 min	4	0.5 typ	0.14 typ	5	50 typ	50
		D44H11	***D45H11***	40 min	4	0.5 typ	0.14 typ	5	50 typ	50

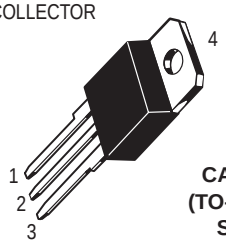
(1)$|h_{FE}|$ @ 1 MHz
(2)Darlington
(3)Switching tests performed w/special application simulator circuit. See data sheet for details.
(7)V_{CEO} = 375 V
(8)When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.
(9)Self protected Darlington

Devices listed in bold, italic are Motorola preferred devices.

Table 2. Plastic TO–220AB (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min(8)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
10	100	***BDX33C***(2)	***BDX34C***(2)	750 min	3				3	70
	450/1000	***MJE18009***		14/34	1.5	2.75(3)	0.2(3)	3	12	150
12	400/700	***MJE13009***		6/30	8	3	0.7	8	4	100
15	80	***2N6488***	***2N6491***	20/150	5	0.6 typ	0.3 typ	5	5	75
		D44VH10	***D45VH10***	20 min	4	0.5	0.09	8	50 typ	83
	100	***BDW42***(2)	***BDW47***(2)	1k min	5	1 typ	1.5 typ	5	4	85

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



CASE 340D
(TO–218 Type,
SOT–93)

Table 3. Plastic TO–218 Type

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min(8)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
8	500/1000	***MJH16006A***		5 min	8	2.5	0.25	5		125
10	60	TIP140(2)	TIP145(2)	500 min	10	2.5 typ	2.5 typ	5	4(1)	125
		TIP141(2)	TIP146(2)	500 min	10	2.5 typ	2.5 typ	5	4(1)	125
	100	***BDV65B***(2)	***BDV64B***(2)	1k min	5					125
		TIP33C	TIP34C	20/100	3				3	80
		TIP142(2)	***TIP147***(2)	500 min	10	2.5 typ	2.5 typ	5	4(1)	125
	400	***BU323AP***(2)		150/100	6	15	15	6		125
		MJH10012(2)		100/2k	6	15	15	6		118

(1)$|h_{FE}|$ @ 1 MHz
(2)Darlington
(8)When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

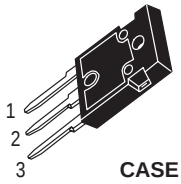
Devices listed in bold, italic are Motorola preferred devices.

Table 3. Plastic TO–218 Type (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min(8)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
15	60	***TIP3055***	***TIP2955***	5 min	10				2.5	80
	150	MJH11018(2)	MJH11017(2)	400/15k	10				3	150
	200	MJH11020(2)	MJH11019(2)	400/15k	10				3	150
	250	***MJH11022***(2)	***MJH11021***(2)	400/15k	10				3	150
	400	BUV48		8 min	10	2	0.4	10		150
	450	***BUV48A***		8 min	8	2	0.4	10		150
16	140	MJE4342	MJE4352	15 min	8	1.2 typ	1.2 typ	8	1	125
	160	***MJE4343***	***MJE4353***	15 min	8	1.2 typ	1.2 typ	8	1	125
20	60	MJH6282(2)	MJH6285(2)	750/18k	10				4	125
	100	***MJH6284***(2)	***MJH6287***(2)	750/18k	10				4	125
25	80	TIP35A	TIP36A	15/75	15	0.6 typ	0.3 typ	10	3	125
	100	***BD249C***	***BD250C***	10 min	15				3	125
		TIP35C	***TIP36C***	15/75	15	0.6 typ	0.3 typ	10	3	125

(2)Darlington
(8)When 2 voltages are given, the format is $V_{CEO(sus)}$ / V_{CES}.

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER



CASE 340F
(TO–247 Type)

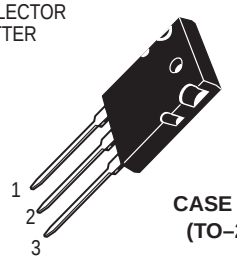
Table 4. Isolated Mounting Hole — Plastic TO–247 Type

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
			NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
10	650	1500	***MJW16212***		4/10	10	4(3)	0.5(3)	5.5		150
	800	1500	***MJW16018***		4 min	5	4.5 typ	0.2 typ	5	3 typ	150
12	500	1200	***MJW16206***		5/13	10	2.25	0.25	6.5	3 typ	150
15	450	850	***MJW16010***		5 min	15	1.2 typ	0.2 typ	10		150
		850	***MJW16012***		7 min	15	0.9 typ	0.15 typ	10		150
	500	1000	***MJW16010A***		5 min	15	3	0.4	10		150

(3)Switching tests performed w/special application simulator circuit. See data sheet for details.
(10)Tested in Applications simulator: see Data Sheet.

Devices listed in bold, italic are Motorola preferred devices.

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER



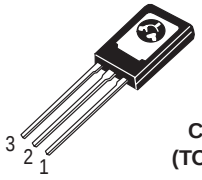
CASE 340G
(TO–264)

Table 5. Large Plastic TO–264

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		hFE Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
15	200	***MJL3281A***	***MJL1302A***	60/175	0.1				30 typ	200
	650/1500	***MJL16218***		4/11	12				2.5 typ	170
16	250	***MJL21194***	***MJL21193***	25/75	8				4	200

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER



CASE 77
(TO–225AA)

Table 6. Plastic TO–225AA Type (Formerly TO–126 Type)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
0.3	350	***MJE3439***		40/160	0.02				15	15
0.5	150	MJE341		25/200	0.05				15	20.8
	200	***MJE344***		30/300	0.05				15	20.8
	250	2N5655		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20
		BD157		30/240	0.05					20
	300	***BD158***		30/240	0.05					20
		MJE340	***MJE350***	30/240	0.05					20.8
		2N5656		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20

Devices listed in bold, italic are Motorola preferred devices.

Table 6. Plastic TO–225AA Type (Formerly TO–126 Type) (continued)

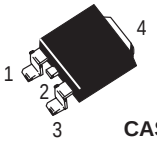
I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
0.5	350	***2N5657***		30/250	0.1	3.5 typ	0.24 typ	0.1	10	20
		BD159		30/240	0.05					20
1	40	2N4921	2N4918	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30
	60	2N4922	2N4919	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30
	80	***2N4923***	***2N4920***	20/100	0.5	0.6 typ	0.3 typ	0.5	3	30
1.5	45	***BD165***	***BD166***	15 min	0.5				6	20
		BD135	BD136	40/250	0.15					12.5
	60	BD137	BD138	40/250	0.15					12.5
	80	***BD169***		15 min	0.5				6	20
		BD139	***BD140***	40/250	0.15					12.5
			BD140–10	63/160	0.15					12.5
	300	MJE13002(11)		5/25	1	4	0.7	1	5	40
	400	***MJE13003***(11)		5/25	1	4	0.7	1	5	40
2	80	***BD237***	***BD238***	25 min	1				3	25
	100	***MJE270***(2)(11)	***MJE271***(2)(11)	1.5k min	0.12				6	15
3	60	MJE181	MJE171	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
	80	***BD179***	***BD180***	40/250	0.15				3	30
		MJE182	***MJE172***	50/250	0.1	0.6 typ	0.12 typ	0.1	50	12.5
	200	***BUY49P***		30 min	0.5				25	20
4	40	***MJE521***	***MJE371***	40 min	1					40
	45	***BD437***	***BD438***	40 min	2				3	36
			BD776(2)	750 min	2				20	15
	60		***BD440***	25 min	2				3	36
		BD677(2)	***BD678***(2)	750 min	1.5					40
		BD677A(2)	***BD678A***(2)	750 min	2					40
		BD787	***BD788***	20 min	2				50	15
		BD777(2)	***BD778***(2)	750 min	2				20	15
		2N5191	***2N5194***	25/100	1.5	0.4 typ	0.4 typ	1.5	2	40
		MJE800(2)	***MJE700***(2)	750 min	1.5				1(1)	40
		2N6038(2)	***2N6035***(2)	750/18k	2	1.7 typ	1.2 typ	2	25	40
	80	***2N5192***	***2N5195***	25/100	1.5	0.4 typ	0.4 typ	1.5	2	40
		BD441	***BD442***	15 min	2				3	36
		BD679(2)	***BD680***(2)	750 min	1.5					40
		BD679A(2)	***BD680A***(2)	750 min	2					40
		BD789	***BD790***	10 min	2				40	15

(1) $|h_{FE}|$ @ 1 MHz
(2) Darlington
(11) Case 77, Style 3

Devices listed in bold, italic are Motorola preferred devices.

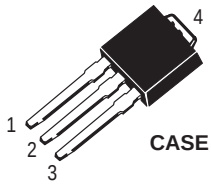
Table 6. Plastic TO–225AA Type (Formerly TO–126 Type) (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
4	80	***BD779***(2)	***BD780***(2)	750 min	2				20	15
		MJE802(2)	MJE702(2)	750 min	1.5				1(1)	40
		MJE803(2)	***MJE703***(2)	750 min	2				1(1)	40
		2N6039(2)	***2N6036***(2)	750/18k	2	1.7 typ	1.2 typ	2	25	40
	100	***BD681***(2)	***BD682***(2)	750 min	1.5					40
		BD791	***BD792***	10 min	2				40	15
		MJE243	***MJE253***	40/120	0.2	0.15 typ	0.07 typ	2	40	15
5	25	***MJE200***	***MJE210***	45/180	2	0.13 typ	0.035 typ	2	65	15



CASE 369A(13)

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



CASE 369(12)

Table 7. DPAK – Surface Mount Power Packages

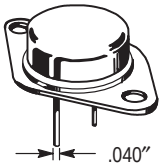
I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s µs Max	t_f µs Max	@ I_C Amp		
0.5	300	***MJD340***	***MJD350***	30/240	0.05					15
1	250	MJD47		30/150	0.3	2	0.2	0.3	10	15
	375		***MJD5731***	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	400	***MJD50***		30/150	0.3	2	0.2	0.3	10	15
1.5	400	***MJD13003***		5/25	1	4	0.7	1	4	15

(1)$|h_{FE}|$ @ 1 MHz
(2)Darlington
(12)Case 369–07 may be ordered by adding –1 suffix to part number.
(13)Case 369A–13 may be ordered as tape and reel by adding a "T4" suffix; 2500 units/reel.

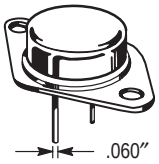
Devices listed in bold, italic are Motorola preferred devices.

Table 7. DPAK – Surface Mount Power Packages (continued)

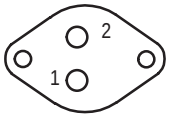
I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
2	100	***MJD112***(2)	***MJD117***(2)	1000 min	2	1.7	1.3	2	25(1)	20
3	40	MJD31	MJD32	10 min	1	0.6	0.3	1	3	15
	100	***MJD31C***	***MJD32C***	10 min	1	0.6	0.3	1	3	15
4	80	***MJD6039***(2)	***MJD6036***(2)	1k/12k	2	1.7	1.2	2	25	20
	100	***MJD243***	***MJD253***	40/180	0.2	0.16	0.04	1	40	12.5
5	25	***MJD200***	***MJD210***	45/180	2	0.15	0.04	2	65	12.5
6	100	***MJD41C***	***MJD42C***	15/75	3	0.4	0.15	3	3	20
8	80	***MJD44H11***	***MJD45H11***	40 min	4	0.5	0.14	5	50 typ	20
	100	***MJD122***(2)	***MJD127***(2)	1k/12k	4	1.5	2	4	4(1)	20
10	60	***MJD3055***	***MJD2955***	20/100	4	1.5	1.5	3	2	20
	80	***MJD44E3***(2)		1k min	5	2	0.5	10		20



CASE 1–07
TO–204AA



CASE 197A TO–204AE
(Used for high current types at end of table. See types w/footnote(16).)



STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

Table 8. Metal TO–204AA (Formerly TO–3), TO–204AE

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min(8)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
4	200	MJ15018		30 min	1				20	150
	250	***MJ15020***	***MJ15021***	30 min	1				20	150
5	700/1500	***BU208A***		2.5 min	4.5	8 typ	0.4 typ	4.5	4 typ	90
8	60	MJ1000(2)		1k min	3					90
		2N6055(2)		750/18k	4	1.5 typ	1.5 typ	4	4(1)	100
	80	***MJ1001***(2)		1k min	3					90
		2N6056(2)		750/18k	4	1.5 typ	1.5 typ	4	4(1)	100

(1)$|h_{FE}|$ @ 1 MHz
(2)Darlington
(8)When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.
(12)Case 369 may be ordered by adding –1 suffix to part number.
(13)Case 369A may be ordered as tape and reel by adding a "T4" suffix; 2500 units/reel.

Devices listed in bold, italic are Motorola preferred devices.

Table 8. Metal TO–204AA (Formerly TO–3), TO–204AE (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min(8)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
10	60	2N3715	2N3791	30 min	3	0.3 typ	0.4 typ	5	4	150
		MJ3000(2)	MJ2500(2)	1k min	5					150
	80	2N3716	2N3792	30 min	3	0.3 typ	0.4 typ	5	4	150
		2N5878		20/100	4	1	0.8	4	4	150
		MJ3001(2)	***MJ2501***(2)	1k min	5					150
	140	2N3442		20/70	4					117
	250	***MJ15011***	***MJ15012***	20/100	2					200
	325	***MJ413***		20/80	0.5				2.5	125
		MJ423		30/90	1				2.5	125
	400	***BU323A***(2)		150 min	6	7.5 typ	5.2 typ	6		175
		MJ10007(2)		30/300	5	1.5	0.5	5	10(1)	150
		MJ10012(2)		100/2k	6	15	15	6		175
12	60	2N6057(2)	2N6050(2)	750/18k	6	1.6 typ	1.5 typ	6	4(1)	150
	80	2N6058(2)	2N6051(2)	750/18k	6	1.6 typ	1.5 typ	6	4(1)	150
	100	***2N6059***(2)	***2N6052***(2)	750/18k	6	1.6 typ	1.5 typ	6	4(1)	150
15	60	***2N3055***	***MJ2955***	20/70	4	0.7 typ	0.3 typ	4	2.5	115
		2N3055A	***MJ2955A***	20/70	4				0.8	115
		2N6576(2)		2k/20k	4	2	7	10	10–200(1)	120
		2N5881	2N5879	20/100	6	1	0.8	6	4	160
	80	***2N5882***	***2N5880***	20/100	6	1	0.8	6	4	160
	90	2N6577(2)		2k/20k	4	2	7	10	10–200(1)	120
	120	***MJ15015***	***MJ15016***	20/70	4	0.7 typ	0.3 typ	4	1	180
		2N6578(2)		2k/20k	4	2	7	10	10–200(1)	120
	140	MJ15001	MJ15002	25/150	4				2	200
	150	MJ11018(2)	MJ11017(2)	100 min	15				3(1)	175
	200	MJ11020(2)		100 min	15				3(1)	175
		MJ3281A	***MJ1302A***	60/175	0.1				30 typ	250
	250	***MJ11022***(2)	MJ11019(2)	100 min	15				3(1)	175
			MJ11021(2)	6/30	10	4	0.7	10	6 to 24	175
	400/850	***BUX48***		8 min	10	2	0.4	10		175
		2N6547		6/30	10	4	0.7	10	6 to 24	175
	400/650	***MJ16110***		6/20	15	0.8 typ	0.1 typ	10		175
	450/1000	***BUX48A***		8 min	8	2	0.4	10		175

(1)$|h_{FE}|$ @ 1 MHz
(2)Darlington
(8)When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

Devices listed in bold, italic are Motorola preferred devices.

Table 8. Metal TO–204AA (Formerly TO–3), TO–204AE (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min(8)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
15	450/850	MJ16010		5 min	15	1.2 typ	0.2 typ	10		175
		MJ16012		7 min	15	0.9 typ	0.15 typ	10		175
16	140	***2N3773***	2N6609	15/60	8	1.1 typ	1.5 typ	8	4	150
		2N5631	2N6031	15/60	8	1.2 typ	1.2 typ	8	1	200
	200	MJ15022	MJ15023	15/60	8				5	250
	250	***MJ15024***	***MJ15025***	15/60	8				5	250
		MJ21194	***MJ21193***	25/75	8				4	250
20	60	***2N3772***		15/60	10				2	150
		2N6282(2)	2N6285(2)	750/18k	10	2.5 typ	2.5 typ	10	4(1)	160
	75	2N5039		20/100	10	1.5	0.5	10	60	140
	80	***2N6283***(2)	2N6286(2)	750/18k	10	2.5 typ	2.5 typ	10	4(1)	160
	90	2N5038		20/100	12	1.5	0.5	12	60	140
	100	***2N6284***(2)	***2N6287***(2)	750/18k	10	2.5 typ	2.5 typ	10	4(1)	160
	140	***MJ15003***	***MJ15004***	25/150	5				2	250
	200	***BUV11***		10 min	12	1.8	0.4	12	8	150
	350	***MJ10000***(2)		40/400	10	3	1.8	10	10(1)	175
	400	***MJ10005***(2)		40/400	10	1.5	0.5	10	10(1)	175
		MJ13333		10/60	5	4	0.7	10		175
	500	***MJ10009***(2)		30/300	10	2	0.6	10	8(1)	175
25	60	2N5885	2N5883	20/100	10	1	0.8	10	4	200
	80	***2N5886***	***2N5884***	20/100	10	1	0.8	10	4	200
			2N6436	30/120	10	1	0.25	10	40	200
	100	2N6338	2N6437	30/120	10	1	0.25	10	40	200
	120	2N6339	***2N6438***	30/120	10	1	0.25	10	40	200
	140	2N6340		30/120	10	1	0.25	10	40	200
	150	***2N6341***		30/120	10	1	0.25	10	40	200
30	40	***2N3771***		15/60	15				2	150
		2N5301	2N4398	15/60	15	2	1	10	2	200
	60	2N5302	2N4399	15/60	15	2	1	10	2	200
		MJ11012(2)	MJ11011(2)	1k min	20				4(1)	200
	90	***MJ11014***(2)	***MJ11013***(2)	1k min	20				4(1)	200
	100	2N6328		6/30	30				3	200
		MJ802	***MJ4502***	25/100	7.5				2	200
	120	***MJ11016***(2)	***MJ11015***(2)	1k min	20				4(1)	200

(1)$|h_{FE}|$ @ 1 MHz
(2)Darlington
(8)When 2 voltages are given, the format is $V_{CEO(sus)}/V_{CES}$.

Devices listed in bold, italic are Motorola preferred devices.

Table 8. Metal TO–204AA (Formerly TO–3), TO–204AE (continued)

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min(8)	Device Type		h_{FE} Min/Max	@ I_C Amp	Resistive Switching			f_T MHz Min	P_D (Case) Watts @ 25°C
		NPN	PNP			t_s μs Max	t_f μs Max	@ I_C Amp		
30	325	***BUV23***		8 min	16	1.8	0.4	16	8	250
	400/1000	***BUS98***		8 min	20	2.3	0.4	20		250
		BUX98		8 min	20	3	0.8	20		250
	450/850	MJ16020(16)		5 min	30	1.8	0.2	20		250
		MJ16022(16)		7 min	30	1.5	0.15	20		250
	450/1000	***BUS98A***		8 min	16	2.3	0.4	16		250
		BUX98A		8 min	16	3	0.8	16		250
40	200	BUV21(16)		10 min	25	1.8	0.4	25	8	150
	250	***BUV22***(16)		10 min	20	1.1	0.35	20	8	250
	350	MJ10022(2)(16)		50/600	10	2.5	0.9	20		250
	400	***MJ10023***(2)(16)		50/600	10	2.5	0.9	20		250
50	60	2N5685(16)		15/60	25	0.5 typ	0.3 typ	25	2	300
	80	***2N5686***(16)	***2N5684***(16)	15/60	25	0.5 typ	0.3 typ	25	2	300
	90	***MJ11030***(2)(16)	***MJ11031***(2)(16)	400 min	50					300
	100	2N6274(16)		30/120	20	0.8	0.25	20	30	250
	120	2N6275(16)	***2N6379***(16)	30/120	20	0.8	0.25	20	30	250
		MJ11032(2)(16)	***MJ11033***(2)(16)	400 min	50					300
	125	***BUV20***(16)		10 min	50	1.2	0.25	50	8	250
		BUV60(16)		10 min	80	1.1	0.25	80		250
	150	***2N6277***(16)		30/120	20	0.8	0.25	20	30	250
	400	***MJ10015***(2)(16)		10 min	40	2.5	1	20		250
	500	***BUT34***(2)(16)		15 min	32	3	1.5	32		250
		MJ10016(2)(16)		10 min	40	2.5	1	20		250
56	400	***BUT33***(2)(16)		20 min	36	3.3	1.6	36		250
60	60		MJ14001(16)	15/100	50					300
	80	***MJ14002***(16)	***MJ14003***(16)	15/100	50					300
	200	MJ10020(2)(16)		75 min	15	3.5	0.5	30		250
	250	***MJ10021***(2)(16)		75 min	15	3.5	0.5	30		250
70	125	***BUS50***(16)		15 min	50	1.5	0.3	70		350
80	100	***BUV18A***(16)		10 min	80	1.1	0.25	80		250

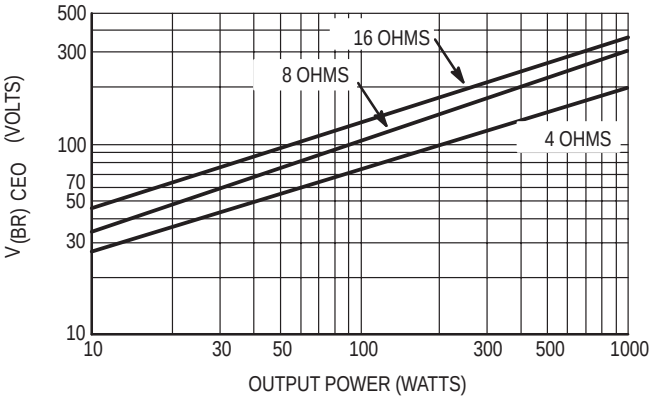
(1)$|h_{FE}|$ @ 1 MHz
(2)Darlington
(8)When 2 voltages are given, the format is $V_{CEO(sus)}$ / V_{CES}.
(16)Case 197A–03 (TO–204AE)

Devices listed in bold, italic are Motorola preferred devices.

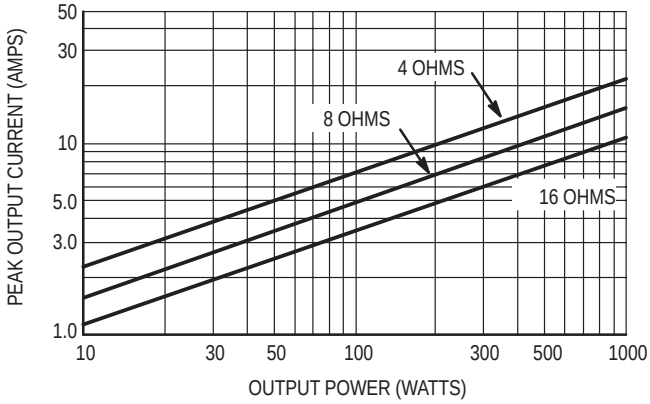
Audio

GENERAL DESIGN CURVES FOR POWER AUDIO OUTPUT STAGES

$V_{(BR)CEO}$ Required on Output and Driver Transistor versus Output Power for 4, 8 and 18 Ohm Loads



Output Transistor Peak Collector Current versus Output Power for 4, 8 and 16 Ohm Loads



Another important parameter that must be considered before selecting the output transistors is the safe–operating area these devices must withstand. For a complete discussion see Application Note AN485.

Table 9. Recommended Power Transistors for Audio/Servo Loads

RMS Power Output	NPN	PNP	Case	P_D Watts @ 25°C	V_{CEO}	h_{FE} @ Min/Max	I_C Amps	f_T MHz Typ	ISB Volts/Amps
To 25W	MJE15030	MJE15031	TO–220	50	150	20 min	4	30	14/3.6
	MJE15032	MJE15033	TO–220	50	250	50 min	1	40	50/1
25 to 50W	2N3055A	MJ2955A	TO–204	120	120	20/70	4	3	60/2
	MJ15001	MJ15002	TO–204	200	140	25/150	4	3	40/5
50 to 100W	MJ15015	MJ15016	TO–204	180	120	20/70	4	3	60/3
	MJ15003	MJ15004	TO–204	250	140	25/150	5	3	100/1
	MJ15020	MJ15021	TO–204	150	250	30 min	1	20	50/3
Over 100W	MJ15024	MJ15025	TO–204	250	250	15/60	8	8	80/2.2
	MJ3281A	MJ1302A	TO–204	250	200	60/175	7	30	50/4
	MJL3281A	MJL1302A	340G–01	150	200	60/175	7	30	40/4
	MJ21194	MJ21193	TO–204	250	250	25/75	8	7	100/2
	MJL21194	MJL21193	340G–01	200	200	25/75	8	7	100/2

The Power Transistors shown are provided for reference only and show device capability. The final choice of the Power Transistors used is left to the circuit designer and depends upon the particular safe–operating area required and the mounting and heat sinking configuration used.

Electronic Lamp Ballasts

As in many other areas of its semiconductor activity, Motorola is an industry leader in the fast growing market of Electronic Ballast Semiconductors. We introduced the first dedicated devices for this market in 1988. Today, devices based on advanced technologies such as H2BIP (High Gain, High Frequency Bipolar) and ZPCMOS (Zero Power Control MOS) are leading the way in providing benefits for ballast manufacturers, consumers and the environment.

Two factors make the Electronic Lamp Ballast market grow at an ever increasing rate — Economics and the Environment.

Lamps based on Electronic Ballasts have long lifetimes and very low power consumption, so contributing to the efficient use of energy and to preservation of the environment. Motorola designs silicon solutions specifically for these applications.

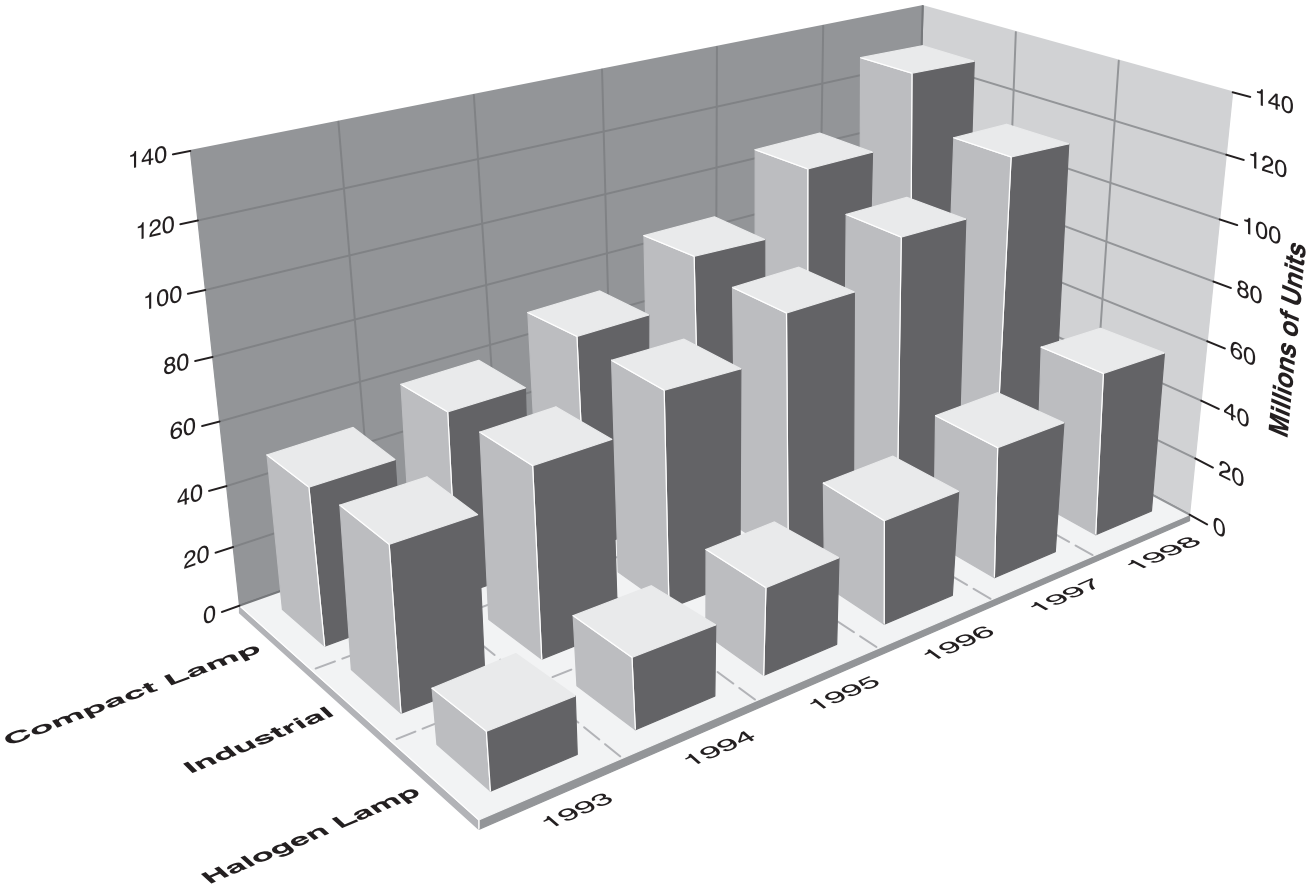
For this growing ballast market Motorola offers optimized devices such as Power MOSFETs, Bipolar Transistors, Linear drive ICs, custom Start–Stop ICs, Diodes and Silicon Bilateral Switches.

Even more important are our efforts to develop the technology for tomorrow in close cooperation with the world's leading manufacturers of Electronic Transformers and Lamp Ballasts, as well as assisting them today in their choice of technology.

This capability is driven from our centre of competence based in Toulouse, France. An important team of Applications, Design, Product, Manufacturing and Marketing Engineers drives our worldwide dedication to this market.

The intention of this section is to provide you with a 'snapshot' of our bipolar transistor products and capabilities. It is a document showing Motorola's professionalism in this area, and illustrating some of the expertise available to *you* — the Electronic Lamp Ballast manufacturer.

World Lamp Ballast Market



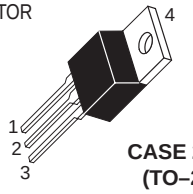
Cross Reference Transistors for Electronic Lamp Ballasts

Industry Part Number	Motorola Direct Replacement	Motorola Nearest Replacement
2SC4053		MJE18004
2SC4546		BUL146F
2SC4630		MJF18004
2SC4820		MJF18002
BU1706A		MJE18604D2
BU1708A		MJE18604D2
BUD43B–1	BUD43B–1	
BUF610		MJE18004D2
BUF654		BUL146
BUH100	BUH100	
BUH150	BUH150	
BUH50	BUH50	
BUH51	BUH51	
BUL146	BUL146	
BUL146F	BUL146F	
BUL147	BUL147	
BUL147F	BUL147F	
BUL213		MJE18204
BUL216		MJE18206
BUL381		BUL45
BUL38D		BUL45D2
BUL410		MJE18006
BUL416		MJE18604D2
BUL43B	BUL43B	
BUL44	BUL44	
BUL44D2	BUL44D2	
BUL44F	BUL44F	
BUL45	BUL45	
BUL45D2	BUL45D2	
BUL45F	BUL45F	
BUL48		MJE18004D2
BUL510		MJE18004D2
BUL57		BUL147
BUL67		BUL147
BUL810		BUV48A
BUL87		BUL147
BULD215		BUL45D2

Industry Part Number	Motorola Direct Replacement	Motorola Nearest Replacement
BULD50		BUL44D2
BULD85		BUL45D2
BUT11AF		MJF18004
BUT18		BUH100
BUT93		BUL45
BUT93D		BUL44D2
BUV46		MJE18006
KSC5021F		MJE18004
KSC5027F		MJE18604D2
MJD13003–1	MJE13003–1	
MJE13003	MJE13003	
MJE13005	MJE13005	
MJE13007	MJE13007	
MJE13009	MJE13009	
MJE18002	MJE18002	
MJE18004	MJE18004	
MJE18004D2	MJE18004D2	
MJE18006	MJE18006	
MJE18008	MJE18008	
MJE18009	MJE18009	
MJE18204	MJE18204	
MJE18206	MJE18206	
MJE18604D2	MJE18604D2	
MJF18002	MJF18002	
MJF18004	MJF18004	
MJF18006	MJF18006	
MJF18008	MJF18008	
MJF18009	MJF18009	
MJF18204	MJF18204	
MJF18206	MJF18206	
TD13003		MJD13003–1
TD13004		BUF43B–1
TEO13005D		BUL44D2–1
TEO13007	MJE13007	
TEO13003	MJE13003	
TEO13005	MJE13005	
TEO13009	MJE13009	

Cross Reference Transistors for Electronic Lamp Ballasts

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



CASE 221A–06
(TO–220AB)

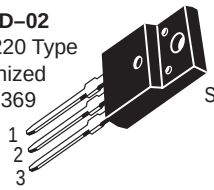
Table 10. TO–220AB Bipolar Transistors

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type	I_C Operating Amps	h_{FE} min @ I_C Operating V_{CE} = 1 V	Inductive Switching @ I_C Operating T_{si} Min/Max (μs)	P_D (Case) Watts @ 25°C
2	350	650	BUL43B	0.8	9	1.8 / 3.3	40
	400	700	BUL44	0.8	10	2.6 / 3.8	50
	400	700	BUL44D2*	0.8	20	2.05 / 2.35	50
	450	1000	MJE18002	1	6	/ 2.75	50
4	500	800	BUH50	2	8 typ	/ 2.5	50
5	400	700	BUL45	2	7	2.6 / 3.8	75
	400	700	BUL45D2*	2	10	1.95 / 2.25	75
	450	1000	MJE18004	2	6	/ 2.5	75
	450	1000	MJE18004D2*	2	6	2.1 / 2.4	75
	550	1200	MJE18204	2	5	/ 2.75	75
	600	1600	MJE18604D2*	0.5	15	/ 1.0	75
6	400	700	BUL146	3	8	2.6 / 3.8	100
	450	1000	MJE18006	3	6	/ 3.2	100
8	400	700	BUL147	4.5	8	2.6 / 3.8	125
	450	1000	MJE18008	4.5	6	/ 3.2	125
	550	1200	MJE18206	3	5	/ 2.75	100
10	400	700	BUH100	5	10 typ	/ 3.0	100
	450	1000	MJE18009	7	8	/ 2.75	150
15	400	700	BUH150	10	8 typ	/ 2.75	150

BUHXXX Series are specified for Halogen applications.
* D2 suffix indicates transistor with built in C–E freewheeling diode and antisaturation network.

Cross Reference Transistors for Electronic Lamp Ballasts

CASE 221D–02
Isolated TO–220 Type
UL Recognized
File #E69369

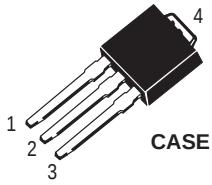


STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

Table 11. Isolated TO–220 Bipolar Transistors

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type	I_C Operating Amps	h_{FE} min @ I_C Operating V_{CE} = 1 V	Inductive Switching @ I_C Operating T_{si} Min/Max (μs)	P_D (Case) Watts @ 25°C
2	400	700	BUL44F	0.8	10	2.6 / 3.8	25
	450	1000	MJF18002	1	6	/ 2.75	25
5	400	700	BUL45F	2	7	2.6 / 3.8	35
	450	1000	MJF18004	2	6	/ 2.5	35
	550	1200	MJF18204	2	5	/ 2.75	40
6	400	700	BUL146F	3	8	2.6 / 3.8	40
	450	1000	MJF18006	3	6	/ 3.2	40
8	400	700	BUL147F	4.5	8	2.6 / 3.8	45
	450	1000	MJF18008	4.5	6	/ 3.2	45
	550	1200	MJF18206	5	6	/ 2.75	45
10	450	1000	MJF18009	7	8	/ 2.75	50

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



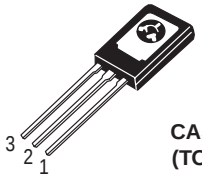
CASE 369–07

Table 12. DPAK Bipolar Transistors

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type	I_C Operating Amps	h_{FE} min @ I_C Operating V_{CE} = 1 V	Inductive Switching @ I_C Operating T_{si} Min/Max (μs)	P_D (Case) Watts @ 25°C
2	350	650	BUD43B–1	0.8	9 typ	1.8 / 3.3	25
	400	700	BUD44D2–1*	0.8	20 typ	2.05 / 2.35	25

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

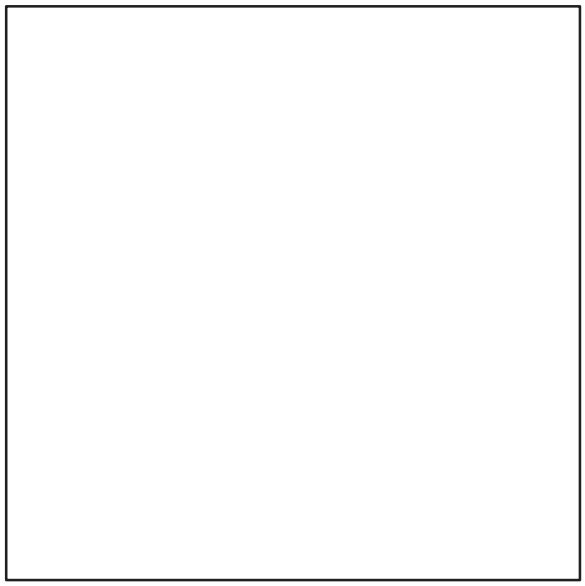


CASE 77–08
(TO–225AA)

Table 13. Case 77 (TO–225) Bipolar Transistors

I_C Cont Amps Max	$V_{CEO(sus)}$ Volts Min	V_{CES} Volts Min	Device Type	I_C Operating Amps	h_{FE} min @ I_C Operating V_{CE} = 1 V	Inductive Switching @ I_C Operating T_{si} Min/Max (μs)	P_D (Case) Watts @ 25°C
1.5	400	700	MJE13003	1	6 typ	/ 3.0	40
4	400	700	BUH51	1	8	/ 3.75	50

BUHXXX Series are specified for Halogen applications.
* D2 suffix indicates transistor with built in C–E freewheeling diode and antisaturation network.



The following power transistor data sheets are arranged in alphanumeric sequence, some data sheets may contain information applying to more than one transistor—e.g.2N4398, 2N4399, 2N5745. To determine if a particular device type is covered by a data sheet in this section, either refer to the alphanumeric listing of the Index and Cross Reference on page 1–2 or simply turn to the proper sequence for indication of where the Data Sheet can be found.

Data Sheets

Complementary Silicon Power Transistors

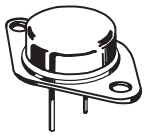
. . . designed for general–purpose switching and amplifier applications.

- DC Current Gain — h_{FE} = 20–70 @ I_C = 4 Adc
- Collector–Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C = 4 Adc
- Excellent Safe Operating Area

NPN
2N3055*
PNP
MJ2955*

***Motorola Preferred Device**

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60 VOLTS
115 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	60	Vdc
Collector–Emitter Voltage	V_{CER}	70	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	7	Vdc
Collector Current — Continuous	I_C	15	Adc
Base Current	I_B	7	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.657	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

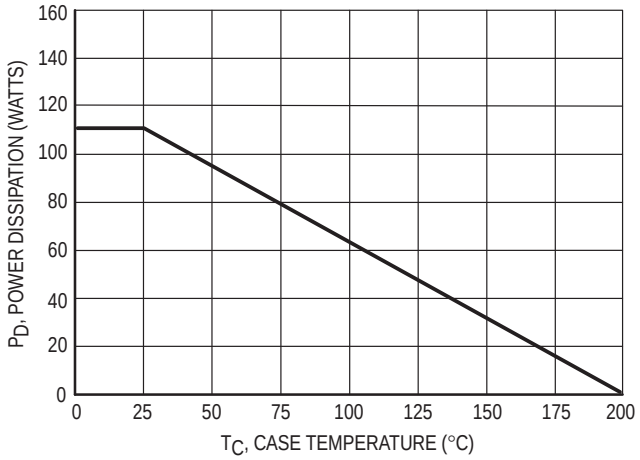


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	—	Vdc
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	$V_{CER(sus)}$	70	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 — —	 1.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
***ON CHARACTERISTICS (1)**				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	 20 5.0	 70 —	—
Collector–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	 —	 1.1 3.0	Vdc
Base–Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1.0 s, Nonrepetitive)	$I_{s/b}$	2.87	—	Adc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	—	MHz
*Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	15	120	—
*Small–Signal Current Gain Cutoff Frequency (V_{CE} = 4.0 Vdc, I_C = 1.0 Adc, f = 1.0 kHz)	f_{hfe}	10	—	kHz

* Indicates Within JEDEC Registration. (2N3055)

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

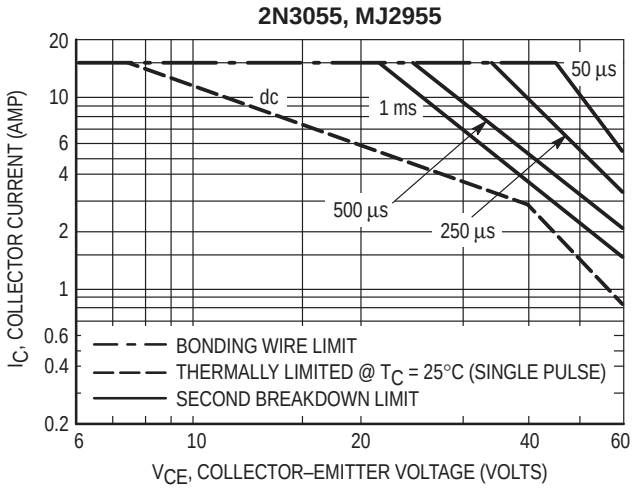


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

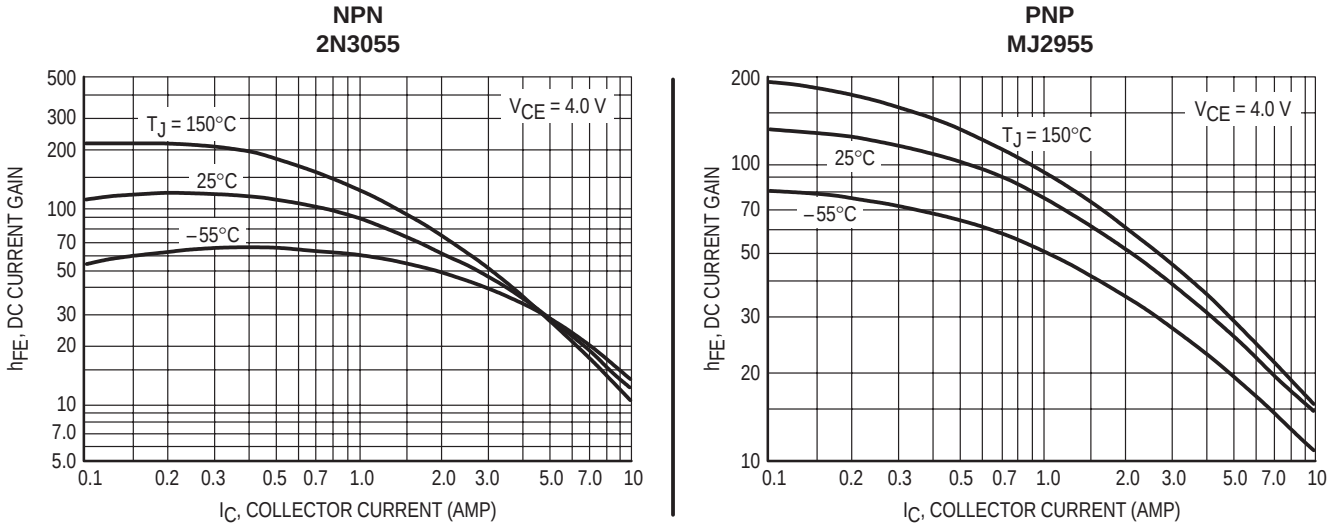


Figure 3. DC Current Gain

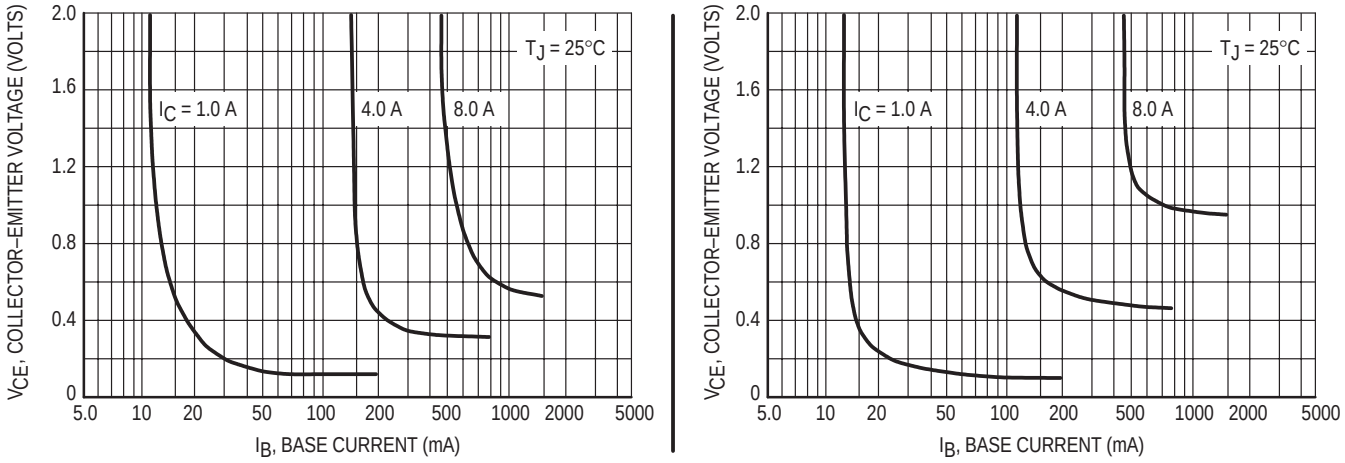


Figure 4. Collector Saturation Region

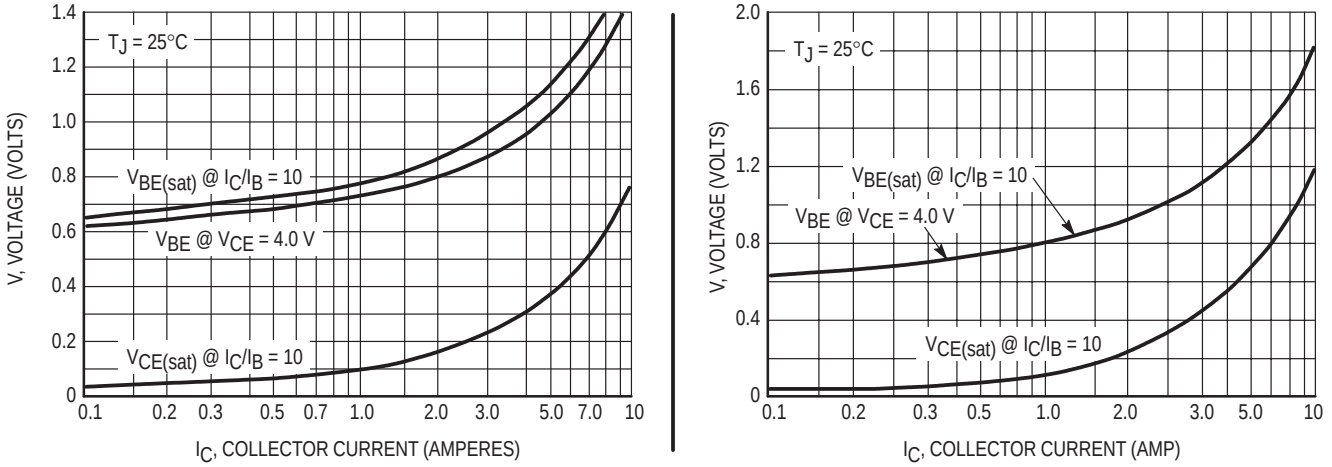


Figure 5. “On” Voltages

Complementary Silicon High-Power Transistors

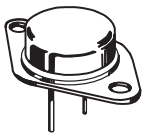
. . . PowerBase complementary transistors designed for high power audio, stepping motor and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc–to–dc converters, inverters, or for inductive loads requiring higher safe operating area than the 2N3055 and MJ2955.

- Current–Gain — Bandwidth–Product @ I_C = 1.0 Adc
  f_T = 0.8 MHz (Min) – NPN
  = 2.2 MHz (Min) – PNP
- Safe Operating Area — Rated to 60 V and 120 V, Respectively

NPN
2N3055A
MJ15015*
MJ2955A
PNP
MJ15016*

*Motorola Preferred Device

15 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60, 120 VOLTS 115, 180 WATTS



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	2N3055A MJ2955A	MJ15015 MJ15016	Unit
Collector–Emitter Voltage	V_{CEO}	60	120	Vdc
Collector–Base Voltage	V_{CBO}	100	200	Vdc
Collector–Emitter Voltage Base Reversed Biased	V_{CEV}	100	200	Vdc
Emitter–Base Voltage	V_{EBO}	7.0		Vdc
Collector Current — Continuous	I_C	15		Adc
Base Current	I_B	7.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.65	180 1.03	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	0.98	°C/W

* Indicates JEDEC Registered Data. (2N3055A)

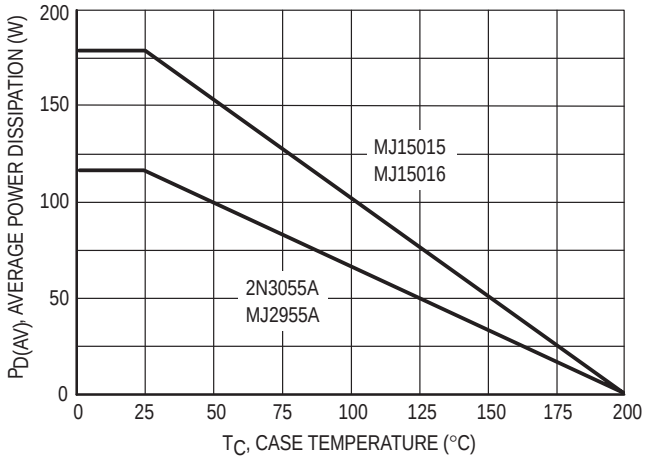


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
*Collector–Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	2N3055A, MJ2955A MJ15015, MJ15016	$V_{CEO(sus)}$	60 120	— —	Vdc
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, $V_{BE(off)}$ = 0 Vdc)	2N3055A, MJ2955A		—	0.7	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 0 Vdc)	MJ15015, MJ15016		—	0.1	
*Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	2N3055A, MJ2955A MJ15015, MJ15016	I_{CEV}	— —	5.0 1.0	mAdc
Collector Cutoff Current		I_{CEV}			mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3055A, MJ2955A MJ15015, MJ15016		— —	30 6.0	
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)	2N3055A, MJ2955A MJ15015, MJ15016	I_{EBO}	— —	5.0 0.2	mAdc
***SECOND BREAKDOWN**					
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$			Adc
(t = 0.5 s non–repetitive)	2N3055A, MJ2955A		1.95	—	
(V_{CE} = 60 Vdc)	MJ15015, MJ15016		3.0	—	
***ON CHARACTERISTICS (1)**					
DC Current Gain		h_{FE}			—
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)			10	70	
(I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)			20	70	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)			5.0	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 4.0 Adc, I_B = 400 mAdc)			—	1.1	
(I_C = 10 Adc, I_B = 3.3 Adc)			—	3.0	
(I_C = 15 Adc, I_B = 7.0 Adc)			—	5.0	
Base–Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	0.7	1.8	Vdc
***DYNAMIC CHARACTERISTICS**					
Current–Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)	2N3055A, MJ15015 MJ2955A, MJ15016	f_T	0.8 2.2	6.0 18	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	60	600	pF
***SWITCHING CHARACTERISTICS (2N3055A only)**					
RESISTIVE LOAD					
Delay Time	(V_{CC} = 30 Vdc, I_C = 4.0 Adc, I_{B1} = I_{B2} = 0.4 Adc, t_p = 25 μs Duty Cycle ≤ 2%)	t_d	—	0.5	μs
Rise Time		t_r	—	4.0	μs
Storage Time		t_s	—	3.0	μs
Fall Time		t_f	—	6.0	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.
* Indicates JEDEC Registered Data. (2N3055A)

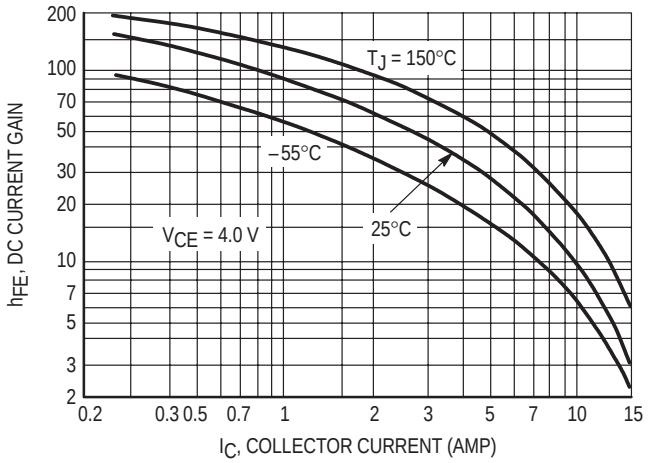


Figure 2. DC Current Gain

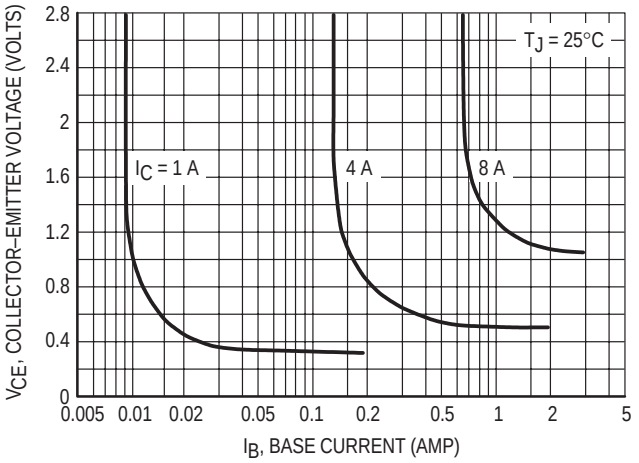


Figure 3. Collector Saturation Region

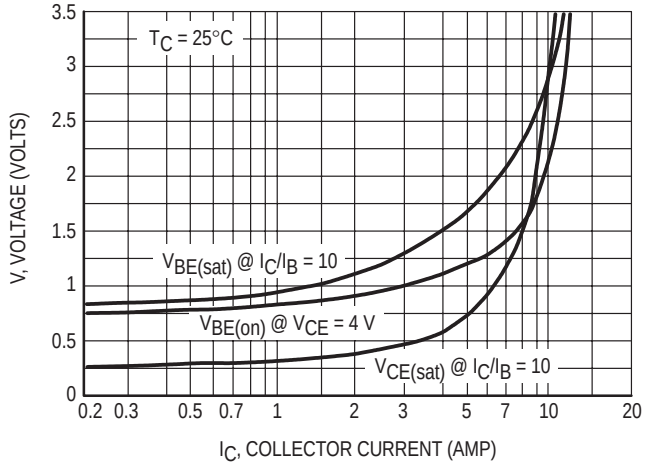


Figure 4. “On” Voltages

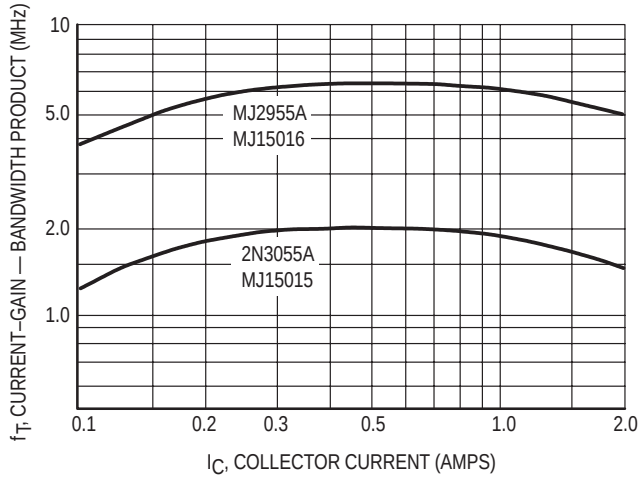


Figure 5. Current–Gain — Bandwidth Product

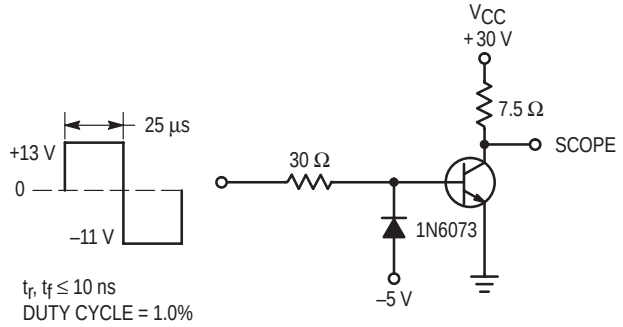


Figure 6. Switching Times Test Circuit (Circuit shown is for NPN)

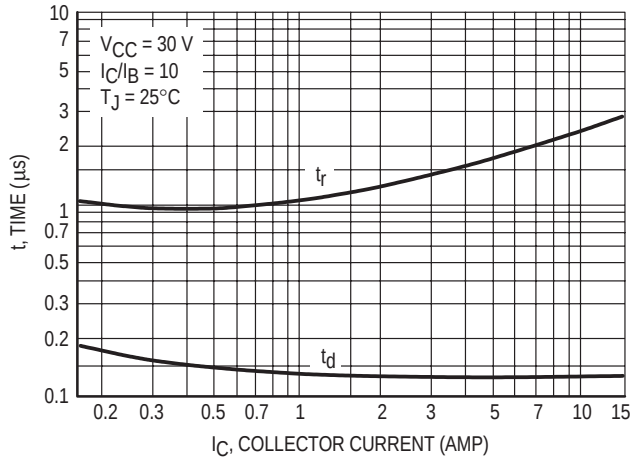


Figure 7. Turn–On Time

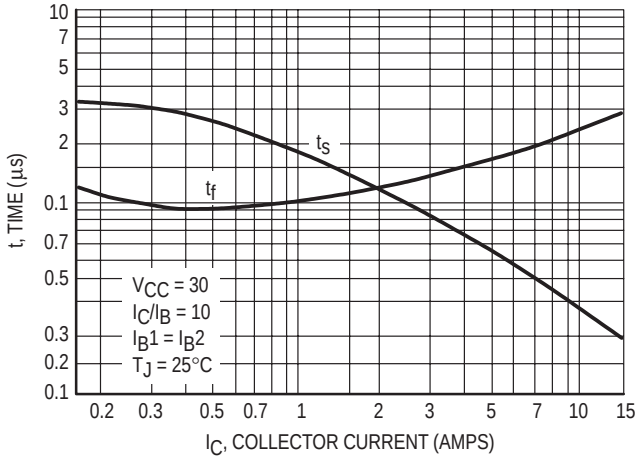


Figure 8. Turn–Off Times

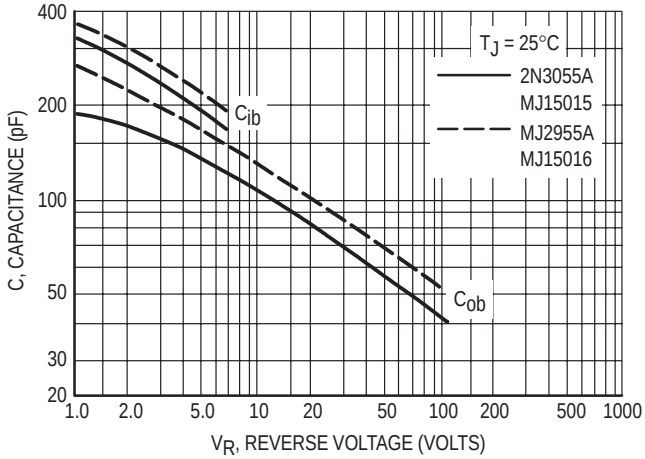


Figure 9. Capacitances

COLLECTOR CUT–OFF REGION

NPN

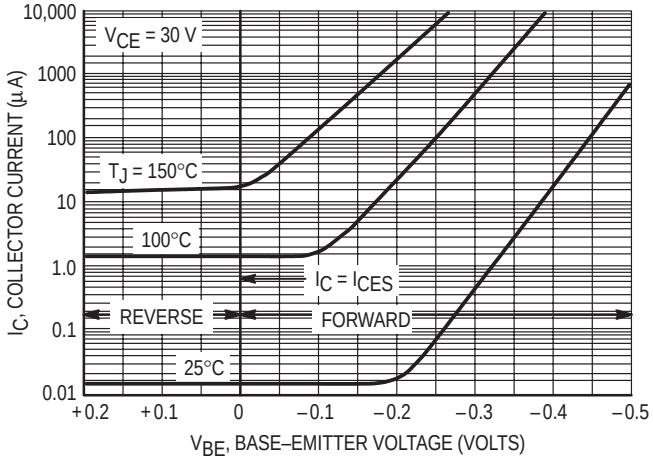


Figure 10. 2N3055A, MJ15015

PNP

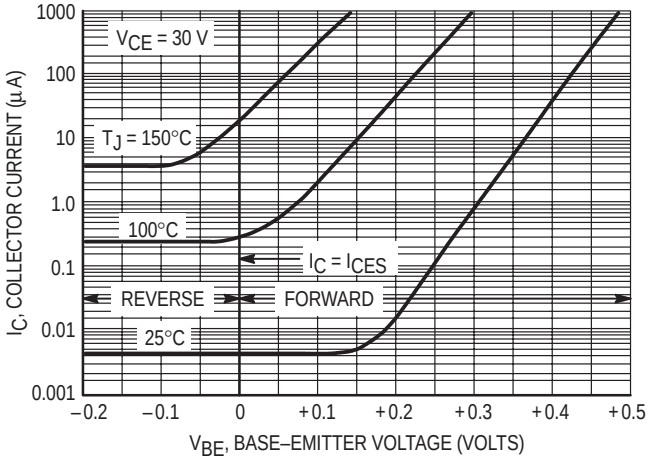


Figure 11. MJ2955A, MJ15016

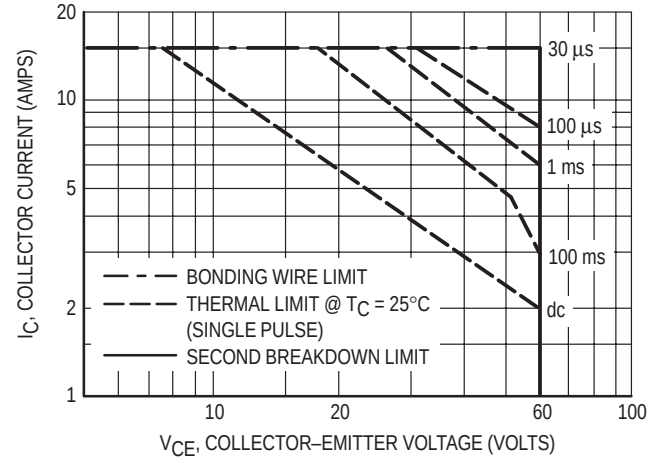


Figure 12. Forward Bias Safe Operating Area 2N3055A, MJ2955A

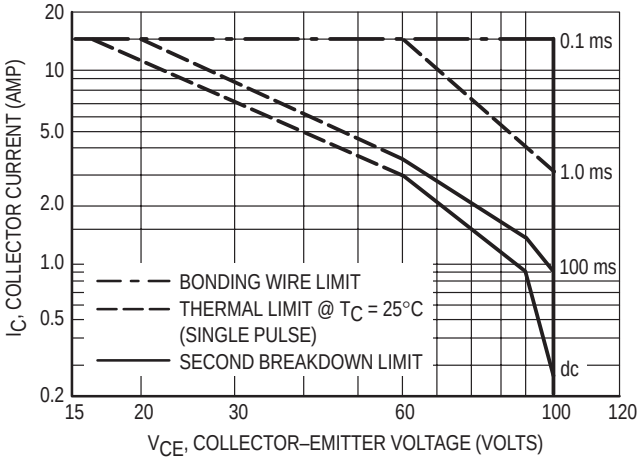


Figure 13. Forward Bias Safe Operating Area MJ15015, MJ15016

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe Operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 12 and 13 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

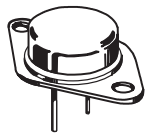
2N3442

High-Power Industrial Transistors

NPN silicon power transistor designed for applications in industrial and commercial equipment including high fidelity audio amplifiers, series and shunt regulators and power switches.

- Collector –Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 140 Vdc (Min)
- Excellent Second Breakdown Capability

10 AMPERE
POWER TRANSISTOR
NPN SILICON
140 VOLTS
117 WATTS



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	140	Vdc
Collector–Base Voltage	V_{CB}	160	Vdc
Emitter–Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous Peak	I_C	10 15**	Adc
Base Current — Continuous Peak	I_B	7.0 —	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	117 0.67	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W

* Indicates JEDEC Registered Data.
** This data guaranteed in addition to JEDEC registered data.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	—	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}	—	200	mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	— —	5.0 30	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 7.5	70 —	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	—	5.0	Vdc
Base–Emitter On Voltage (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	5.7	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (2) (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 40 kHz)	f_T	80	—	kHz
Small–Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	12	72	—

* Indicates JEDEC Registered Data.

NOTES:

4. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.
5. $f_T = |h_{fe}| \bullet f_{test}$

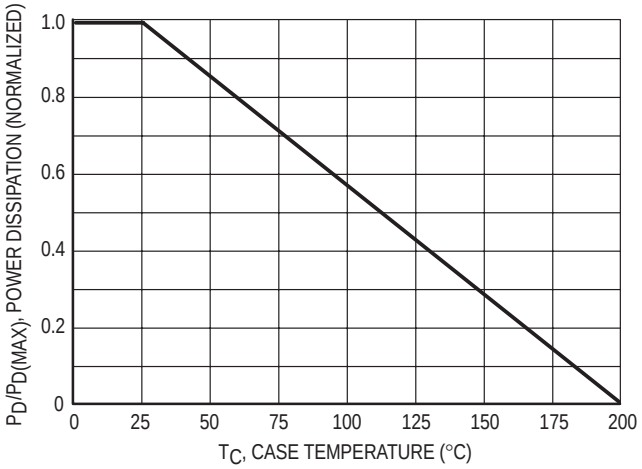


Figure 1. Power Derating

ACTIVE REGION SAFE OPERATING AREA INFORMATION

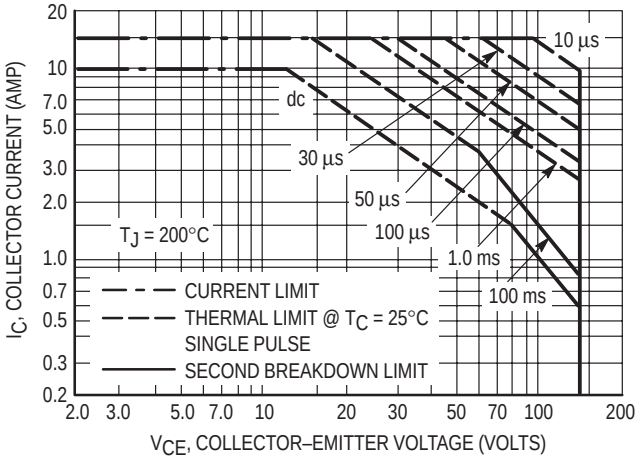


Figure 2. 2N3442

There are two limitations on the power–handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

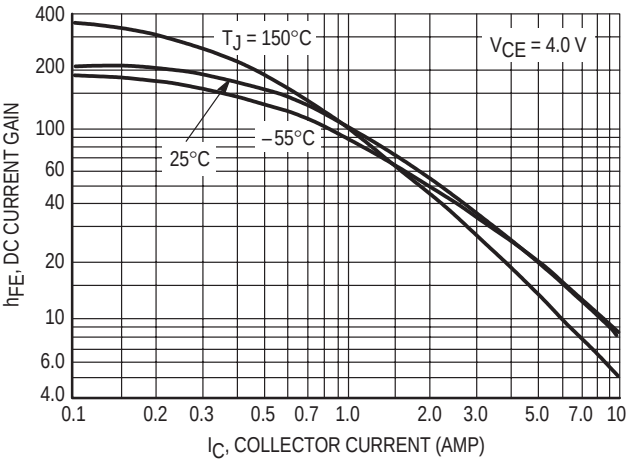


Figure 3. DC Current Gain

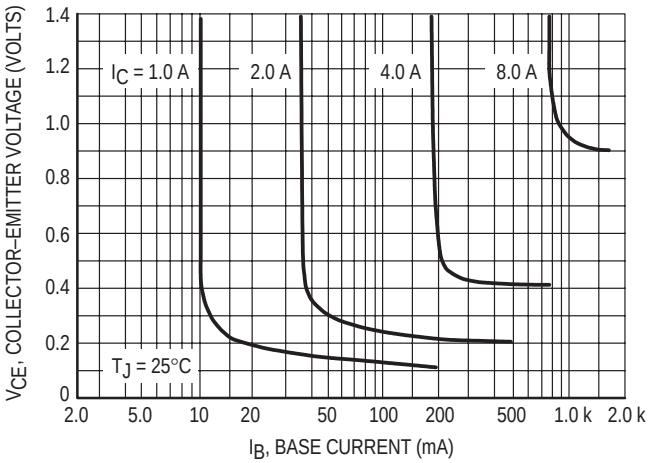


Figure 4. Collector–Saturation Region

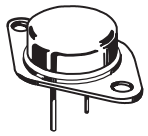
Silicon NPN Power Transistors

. . . designed for medium–speed switching and amplifier applications. These devices feature:

- Total Switching Time at 3 A typically 1.15 μs
- Gain Ranges Specified at 1 A and 3 A
- Low $V_{CE(sat)}$: typically 0.5 V at I_C = 5 A and I_B = 0.5 A
- Excellent Safe Operating Areas
- Complement to 2N3791–92

NPN
2N3715
2N3716

10 AMPERE
POWER TRANSISTORS
SILICON NPN
60–80 VOLTS
150 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	2N3715	2N3716	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Volts
Collector–Base Voltage	V_{CB}	80	100	Volts
Emitter–Base Voltage	V_{EB}	7.0	7.0	Volts
Collector Current	I_C	10	10	Amps
Base Current	I_B	4.0	4.0	Amps
Power Dissipation	P_D	150	150	Watts
Thermal Resistance	θ_{JC}	1.17	1.17	°C/W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	–65 to +200		°C

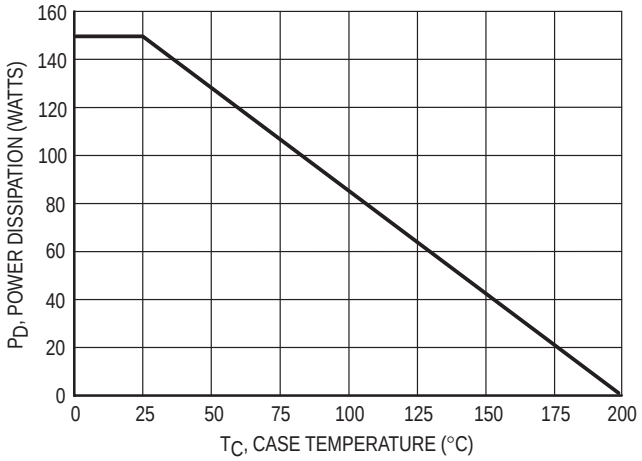


Figure 1. Power–Temperature Derating Curve

Safe Area Limits are indicated by Figures 12, 13. Both limits are applicable and must be observed.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Emitter–Base Cutoff Current (V_{EB} = 7.0 Vdc)	All Types	I_{EBO}	—	5.0	mAdc
Collector–Emitter Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 80 Vdc, V_{BE} = –1.5 Vdc)	2N3715		—	1.0	
(V_{CE} = 100 Vdc, V_{BE} = –1.5 Vdc)	2N3716		—	1.0	
(V_{CE} = 60 Vdc, V_{BE} = –1.5 Vdc, T_C = 150°C)	2N3715		—	10	
(V_{CE} = 80 Vdc, V_{BE} = –1.5 Vdc, T_C = 150°C)	2N3716		—	10	
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$*			Vdc
(I_C = 200 mAdc, I_B = 0)	2N3715		60	—	
	2N3716		80	—	
DC Current Gain (1)		h_{FE}*			—
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	2N3715, 2N3716		50	150	
(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	2N3715, 2N3716		30	—	
Collector–Emitter Saturation Voltage (1) (I_C = 5.0 Adc, I_B = 0.5 Adc)	2N3715, 2N3716	$V_{CE(sat)}$*	—	0.8	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 5.0 Adc, I_B = 0.5 Adc)	2N3715, 2N3716	$V_{BE(sat)}$*	—	1.5	Vdc
Base–Emitter Voltage (1) (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	All Types	V_{BE}*	—	1.5	Vdc
Small Signal Current Gain (V_{CE} = 10 Vdc, I_C = 0.5 Adc, f = 1.0 MHz)	All Types	h_{fe}	4.0	—	—
Switching Times (Figure 2)			**Typ**		µs
(I_C = 5.0 A, I_{B1} = I_{B2} = 0.5 Adc)					
Rise Time		t_r	0.45		
Storage Time		t_s	0.3		
Fall Time		t_f	0.4		

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

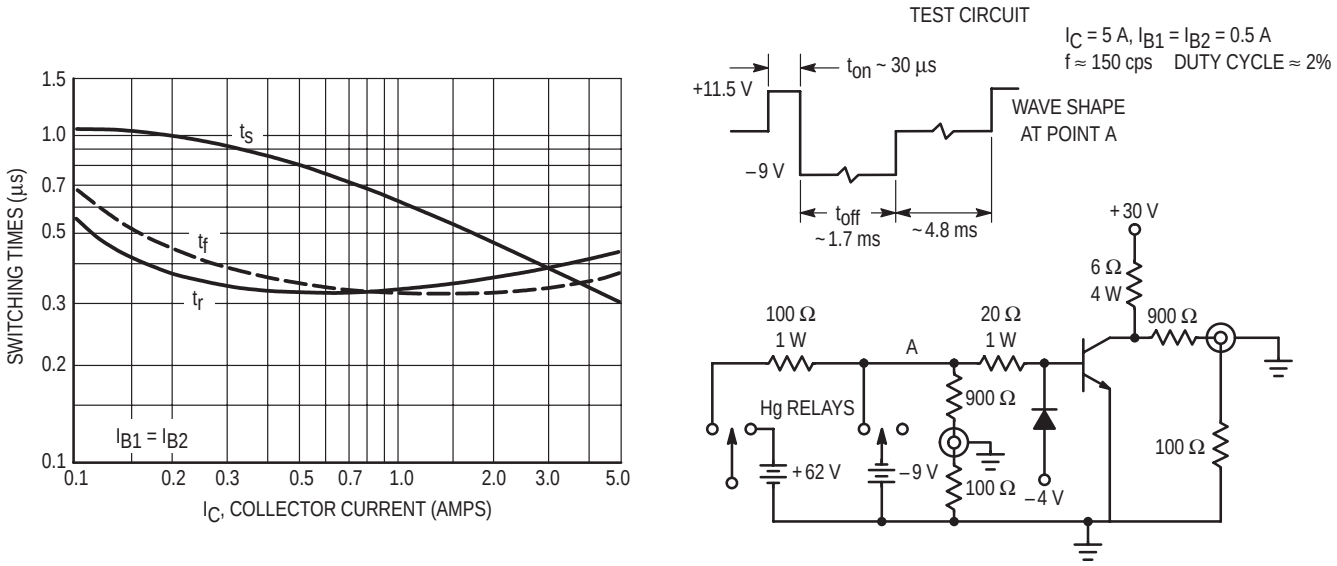


Figure 2. Typical Switching Times

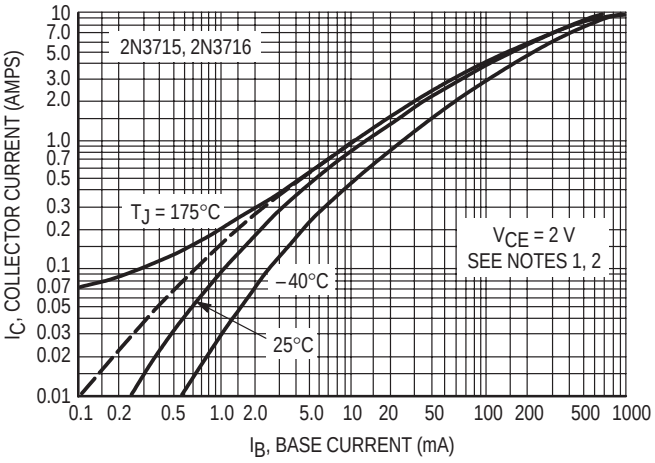


Figure 3. Collector Current versus Base Current

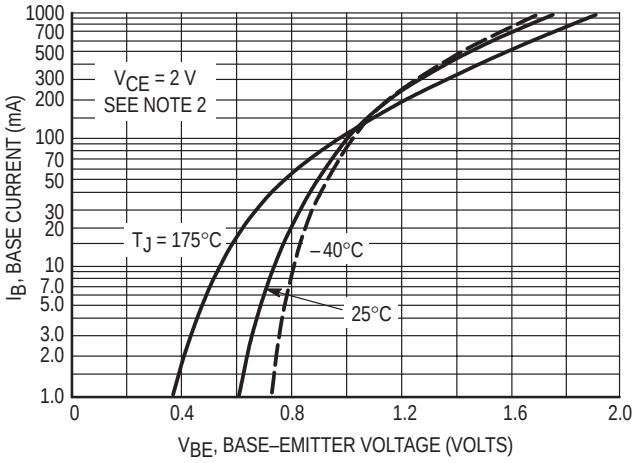


Figure 4. Base Current–Voltage Variations

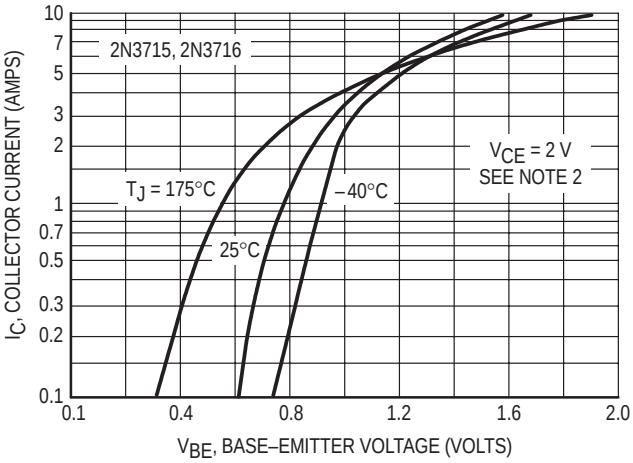


Figure 5. Collector Current–Voltage Variations

NOTE 1. Dotted line indicates metered base current plus the I_{CBO} of the transistor at 175°C.
NOTE 2. Pulse test: pulse width ≈ 200 μsec, duty cycle ≈ 1.5%.

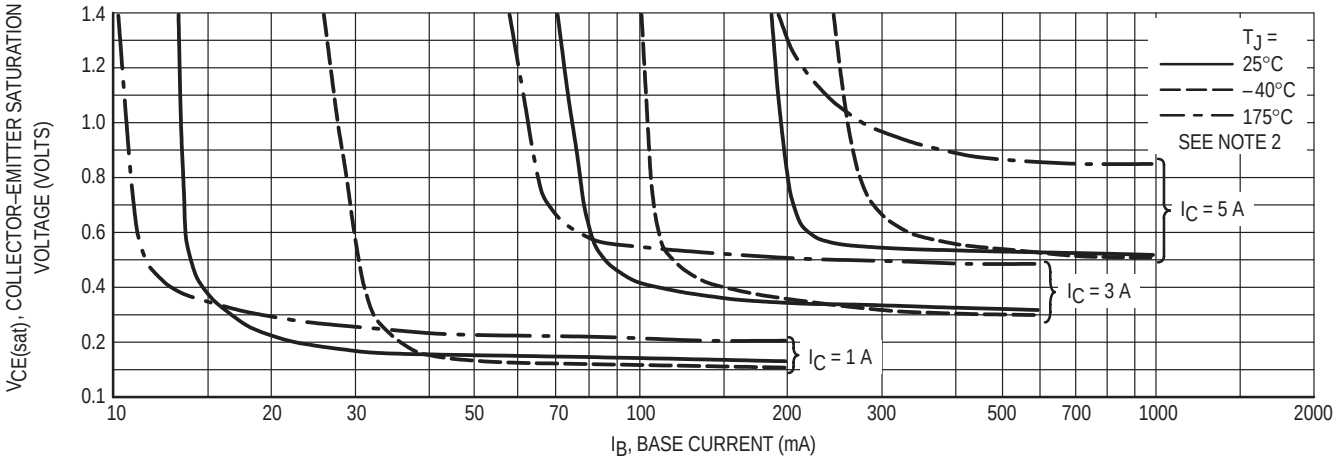


Figure 6. Collector–Emitter Saturation Voltage Variations

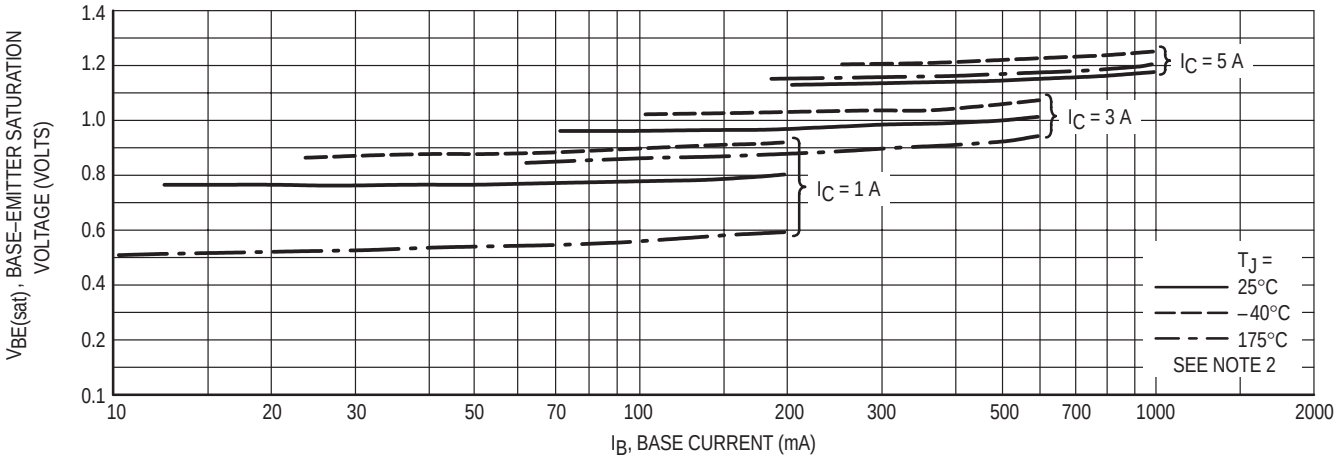


Figure 7. Base–Emitter Saturation Voltage Variations

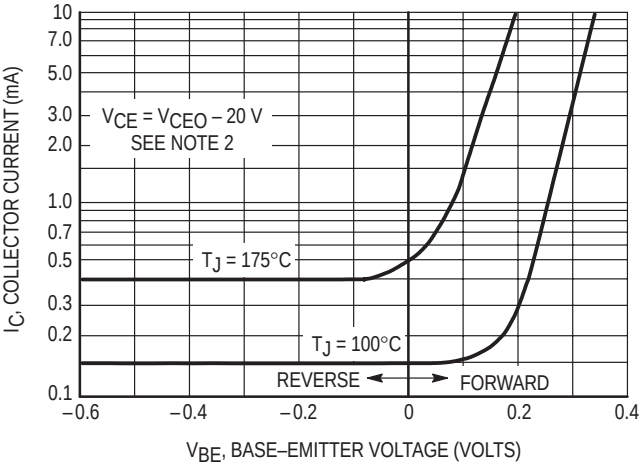


Figure 8. Collector Current versus Base–Emitter Voltage

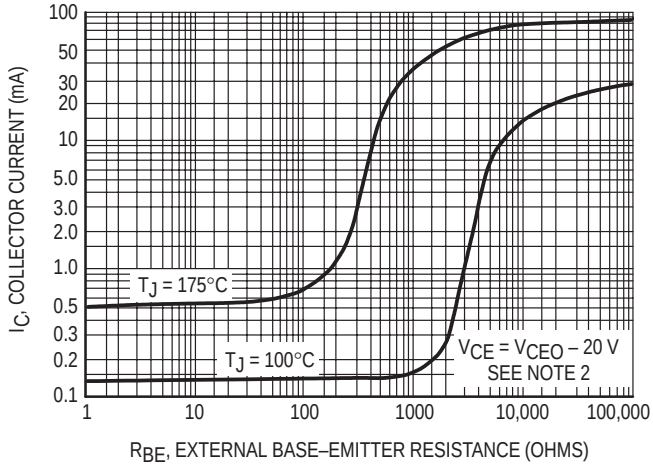


Figure 9. Collector Current versus Base–Emitter Resistance

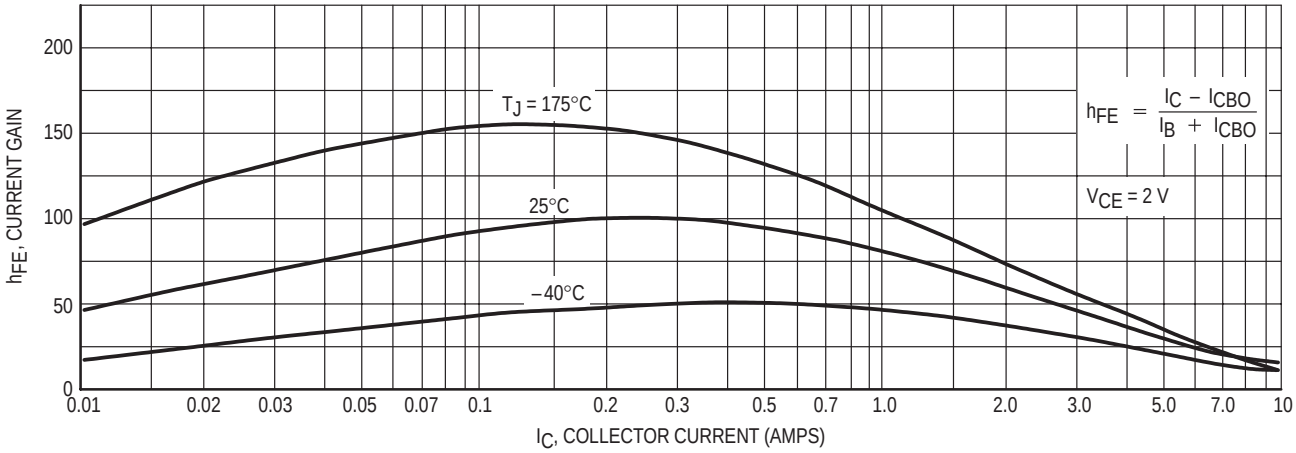


Figure 10. Current Gain Variations

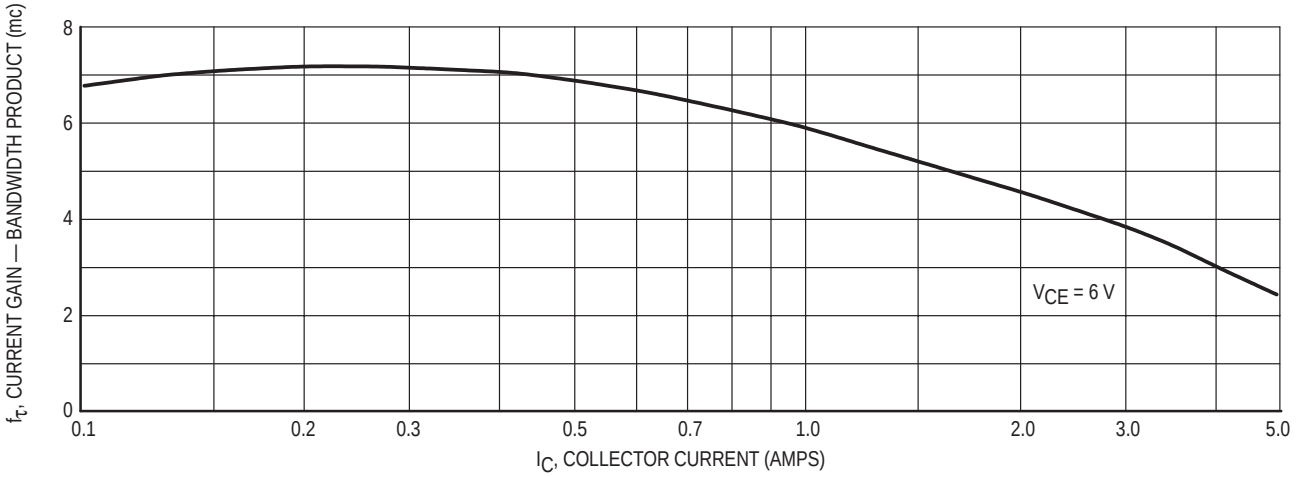


Figure 11. Current Gain — Bandwidth Product versus Collector Current

SAFE OPERATING AREAS

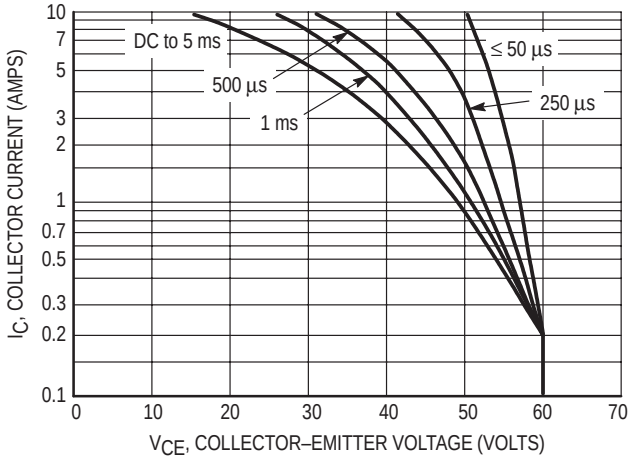


Figure 12. 2N3715

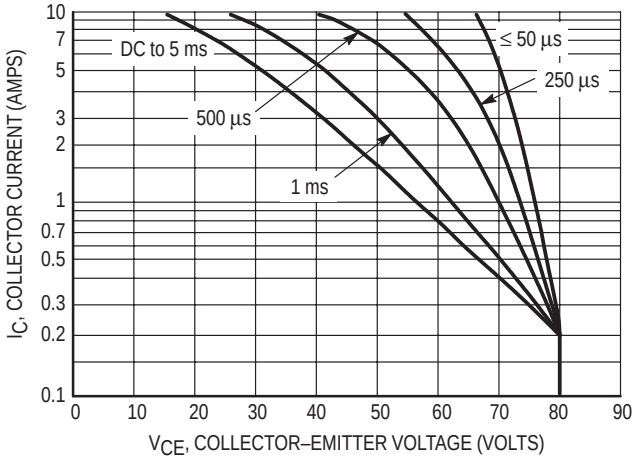


Figure 13. 2N3716

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector–emitter short. (Duty cycle of the excursions make no significant change in these safe areas.) To insure operation below the maximum T_J, the power–temperature derating curve must be observed for both steady state and pulse power conditions.

High Power NPN Silicon Power Transistors

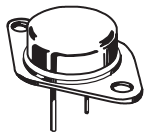
2N3771*
2N3772

*Motorola Preferred Device

. . . designed for linear amplifiers, series pass regulators, and inductive switching applications.

- Forward Biased Second Breakdown Current Capability
  $I_{S/b}$ = 3.75 Adc @ V_{CE} = 40 Vdc — 2N3771
  = 2.5 Adc @ V_{CE} = 60 Vdc — 2N3772

20 and 30 AMPERE POWER TRANSISTORS NPN SILICON 40 and 60 VOLTS 150 WATTS



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	2N3771	2N3772	Unit
Collector–Emitter Voltage	V_{CEO}	40	60	Vdc
Collector–Emitter Voltage	V_{CEX}	50	80	Vdc
Collector–Base Voltage	V_{CB}	50	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0	7.0	Vdc
Collector Current — Continuous Peak	I_C	30 30	20 30	Adc
Base Current — Continuous Peak	I_B	7.5 15	5.0 15	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.855		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	2N3771, 2N3772	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

* Indicates JEDEC Registered Data.

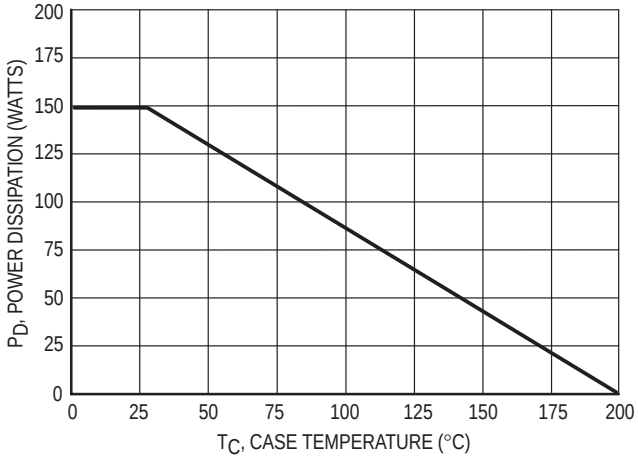


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
*Collector–Emitter Sustaining Voltage (1) (I_C = 0.2 Adc, I_B = 0)	2N3771 2N3772	$V_{CEO(sus)}$	40 60	— —	Vdc
Collector–Emitter Sustaining Voltage (I_C = 0.2 Adc, $V_{EB(off)}$ = 1.5 Vdc, R_{BE} = 100 Ohms)	2N3771 2N3772	$V_{CEX(sus)}$	50 80	— —	Vdc
Collector–Emitter Sustaining Voltage (I_C = 0.2 Adc, R_{BE} = 100 Ohms)	2N3771 2N3772	$V_{CER(sus)}$	45 70	— —	Vdc
*Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 25 Vdc, I_B = 0)	 2N3771 2N3772	I_{CEO}	 — —	 10 10	mAdc
*Collector Cutoff Current (V_{CE} = 50 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 45 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	 2N3771 2N3772 2N6257 2N3771 2N3772	I_{CEV}	 — — — — —	 2.0 5.0 4.0 10 10	mAdc
*Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	 2N3771 2N3772	I_{CBO}	 — —	 2.0 5.0	mAdc
*Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0) (V_{BE} = 7.0 Vdc, I_C = 0)	 2N3771 2N3772	I_{EBO}	 — —	 5.0 5.0	mAdc
***ON CHARACTERISTICS**					
DC Current Gain (1) (I_C = 15 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 30 Adc, V_{CE} = 4.0 Vdc) (I_C = 20 Adc, V_{CE} = 4.0 Vdc)	 2N3771 2N3772 2N3771 2N3772	h_{FE}	 15 15 5.0 5.0	 60 60 — —	—
Collector–Emitter Saturation Voltage (I_C = 15 Adc, I_B = 1.5 Adc) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 30 Adc, I_B = 6.0 Adc) (I_C = 20 Adc, I_B = 4.0 Adc)	 2N3771 2N3772 2N3771 2N3772	$V_{CE(sat)}$	 — — — —	 2.0 1.4 4.0 4.0	Vdc
Base–Emitter On Voltage (I_C = 15 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	 2N3771 2N3772	$V_{BE(on)}$	 — —	 2.7 2.2	Vdc
***DYNAMIC CHARACTERISTICS**					
Current–Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 50 kHz)		f_T	0.2	—	MHz
Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	40	—	—
SECOND BREAKDOWN					
Second Breakdown Energy with Base Forward Biased, t = 1.0 s (non–repetitive) (V_{CE} = 40 Vdc) (V_{CE} = 60 Vdc)	 2N3771 2N3772	$I_{S/b}$	 3.75 2.5	 — —	Adc

* Indicates JEDEC Registered Data.
(1) Pulse Test: 300 μs, Rep. Rate 60 cps.

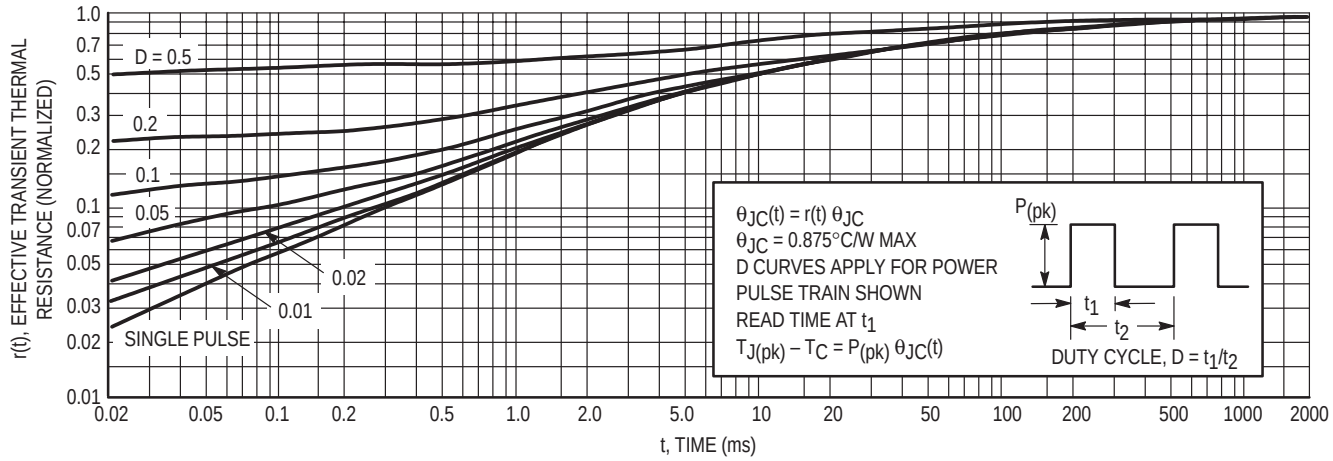


Figure 2. Thermal Response — 2N3771, 2N3772

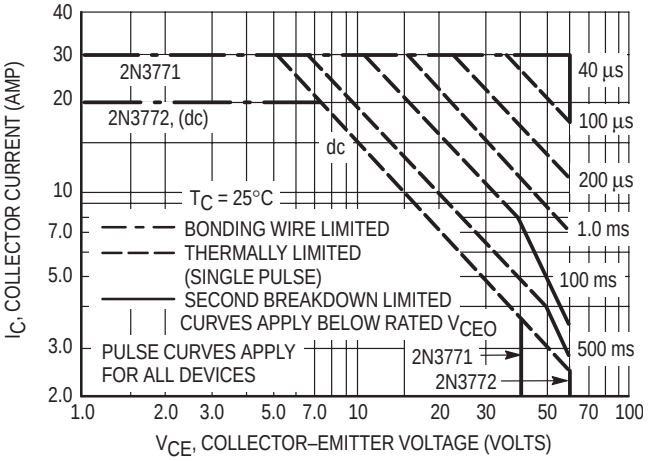


Figure 3. Active–Region Safe Operating Area — 2N3771, 2N3772

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Figure 3 is based on JEDEC registered Data. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data of Figure 2. Using data of Figure 2 and the pulse power limits of Figure 3, $T_{J(pk)}$ will be found to be less than $T_{J(max)}$ for pulse widths of 1 ms and less. When using Motorola transistors, it is permissible to increase the pulse power limits until limited by $T_{J(max)}$.

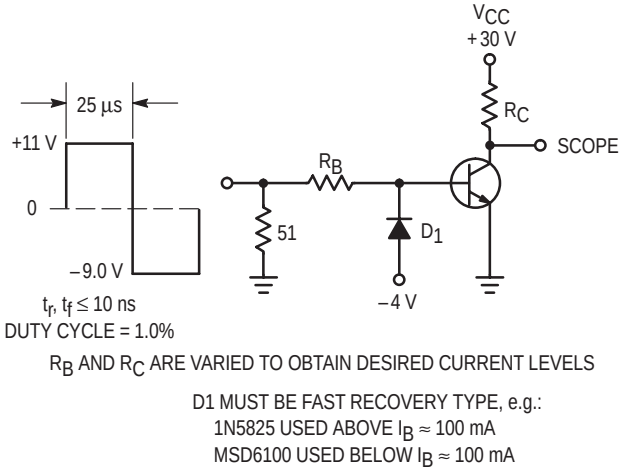


Figure 4. Switching Time Test Circuit

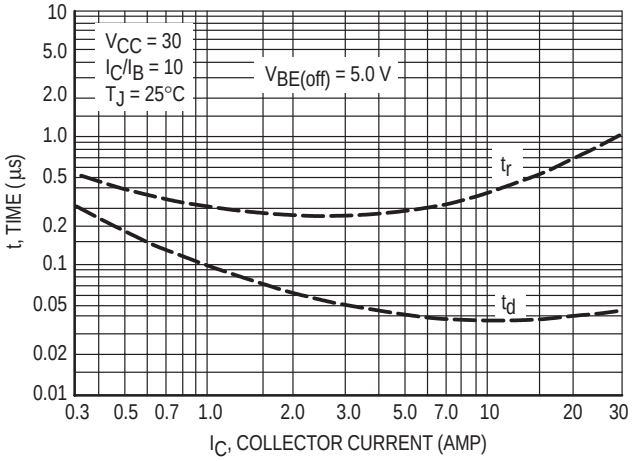


Figure 5. Turn–On Time

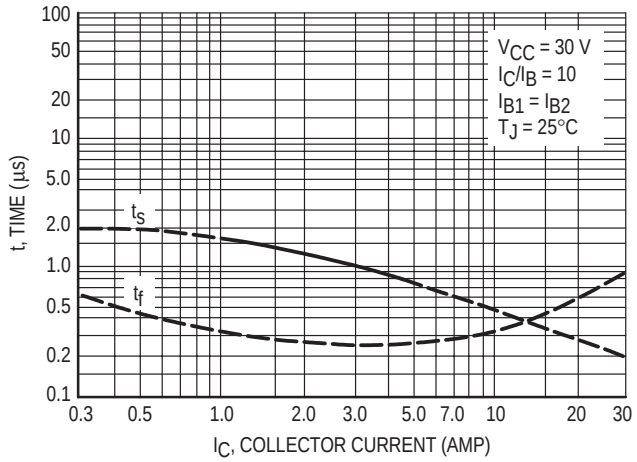


Figure 6. Turn–Off Time

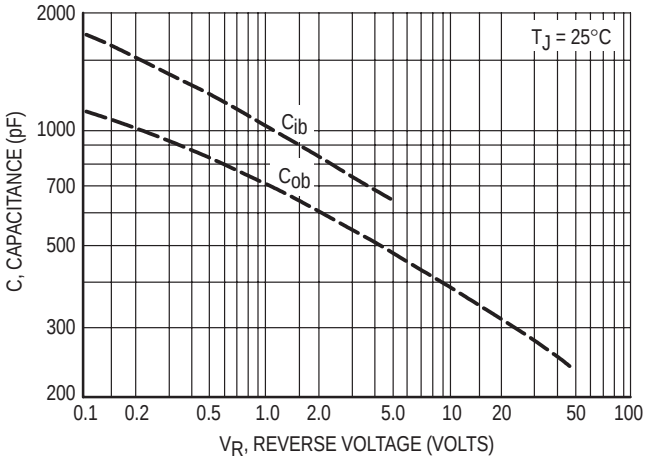


Figure 7. Capacitance

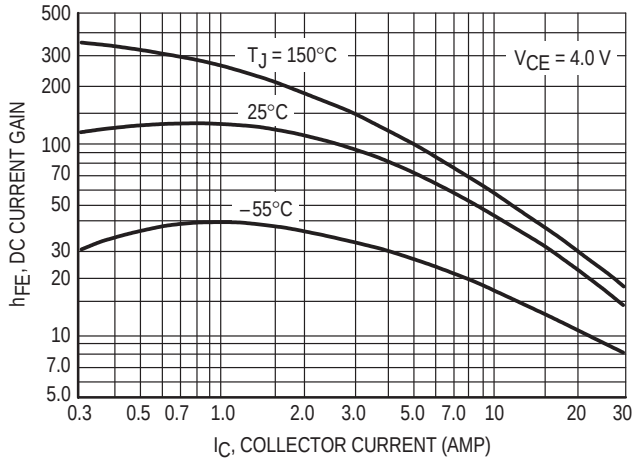


Figure 8. DC Current Gain

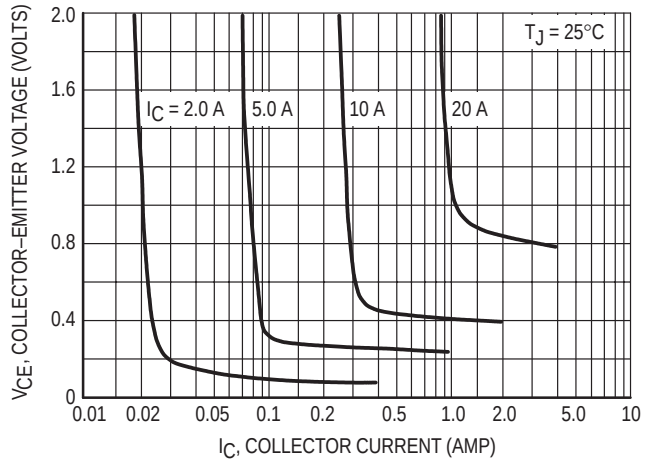


Figure 9. Collector Saturation Region

Complementary Silicon Power Transistors

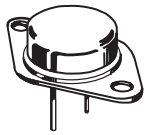
NPN
2N3773*
PNP
2N6609

*Motorola Preferred Device

16 AMPERE
COMPLEMENTARY
POWER TRANSISTORS
140 VOLTS
150 WATTS

The 2N3773 and 2N6609 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc to dc converters or inverters.

- High Safe Operating Area (100% Tested) 150 W @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
  h_{FE} = 15 (Min) @ 8 A, 4 V
  $V_{CE(sat)}$ = 1.4 V (Max) @ I_C = 8 A, I_B = 0.8 A
- For Low Distortion Complementary Designs



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector Emitter Voltage	V_{CEO}	140	Vdc
Collector–Emitter Voltage	V_{CEX}	160	Vdc
Collector–Base Voltage	V_{CBO}	160	Vdc
Emitter–Base Voltage	V_{EBO}	7	Vdc
Collector Current — Continuous — Peak (1)	I_C	16 30	Adc
Base Current — Continuous — Peak (1)	I_B	4 15	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.855	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

* Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
*Collector–Emitter Breakdown Voltage (I_C = 0.2 Adc, I_B = 0)	$V_{CEO(sus)}$	140	—	Vdc
*Collector–Emitter Sustaining Voltage (I_C = 0.1 Adc, $V_{BE(off)}$ = 1.5 Vdc, R_{BE} = 100 Ohms)	$V_{CEX(sus)}$	160	—	Vdc
Collector–Emitter Sustaining Voltage (I_C = 0.2 Adc, R_{BE} = 100 Ohms)	$V_{CER(sus)}$	150	—	Vdc
*Collector Cutoff Current (V_{CE} = 120 Vdc, I_B = 0)	I_{CEO}	—	10	mAdc
*Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 — —	 2 10	mAdc
Collector Cutoff Current (V_{CB} = 140 Vdc, I_E = 0)	I_{CBO}	—	2	mAdc
*Emitter Cutoff Current (V_{BE} = 7 Vdc, I_C = 0)	I_{EBO}	—	5	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain *(I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)	h_{FE}	 15 5	 60 —	—
Collector–Emitter Saturation Voltage *(I_C = 8 Adc, I_B = 800 mAdc) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	 — —	 1.4 4	Vdc
*Base–Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	2.2	Vdc
DYNAMIC CHARACTERISTICS				
Magnitude of Common–Emitter Small–Signal, Short–Circuit, Forward Current Transfer Ratio (I_C = 1 A, f = 50 kHz)	$\|h_{fe}\|$	4	—	—
*Small–Signal Current Gain (I_C = 1 Adc, V_{CE} = 4 Vdc, f = 1 kHz)	h_{fe}	40	—	—
SECOND BREAKDOWN CHARACTERISTICS				
Second Breakdown Collector Current with Base Forward Biased t = 1 s (non–repetitive), V_{CE} = 100 V, See Figure 12	$I_{S/b}$	1.5	—	Adc

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.
* Indicates JEDEC Registered Data.

NPN

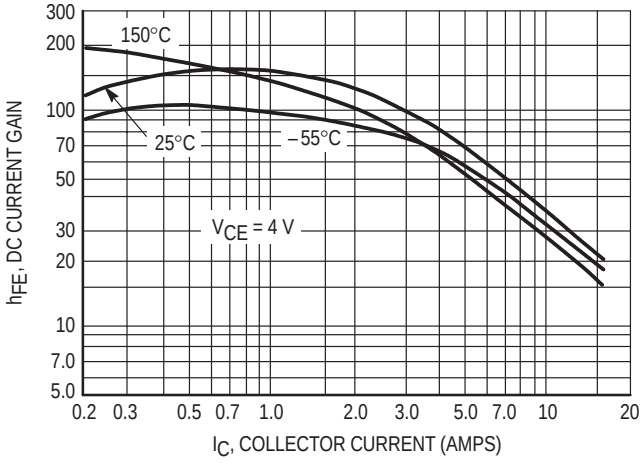


Figure 1. DC Current Gain

PNP

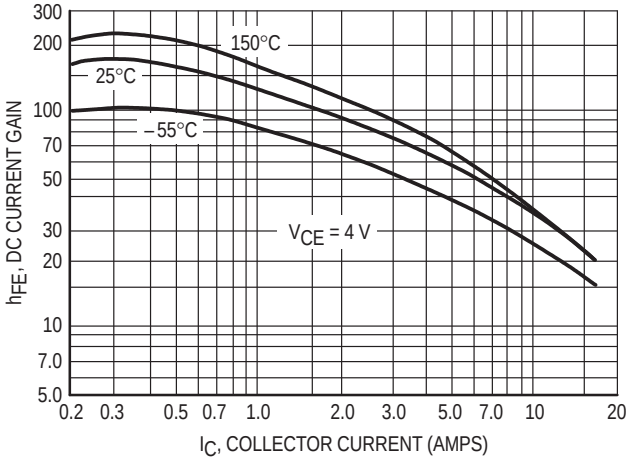


Figure 2. DC Current Gain

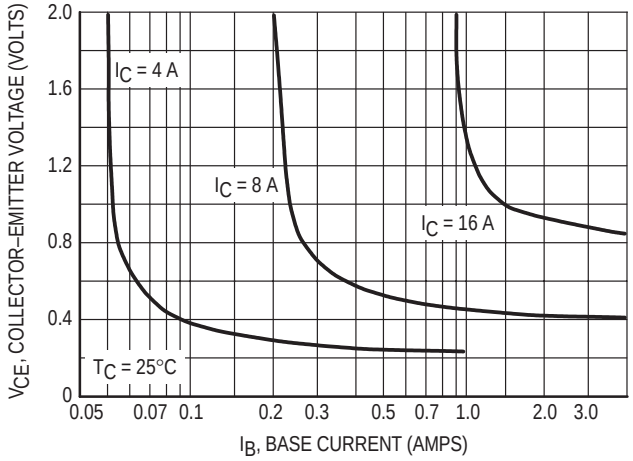


Figure 3. Collector Saturation Region

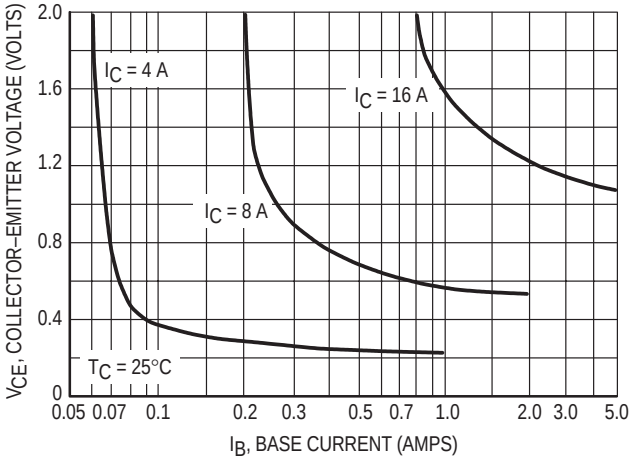


Figure 4. Collector Saturation Region

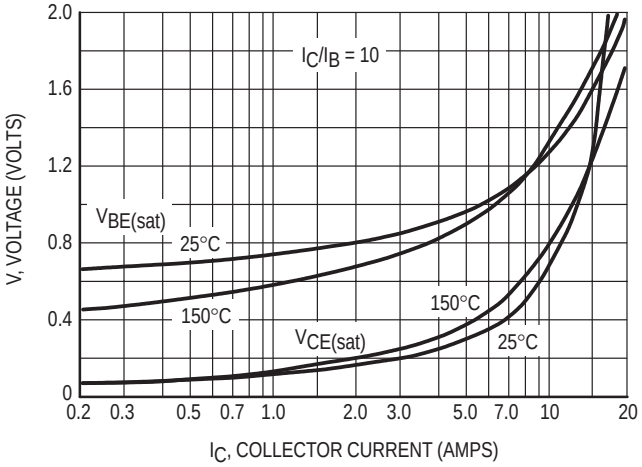


Figure 5. “On” Voltage

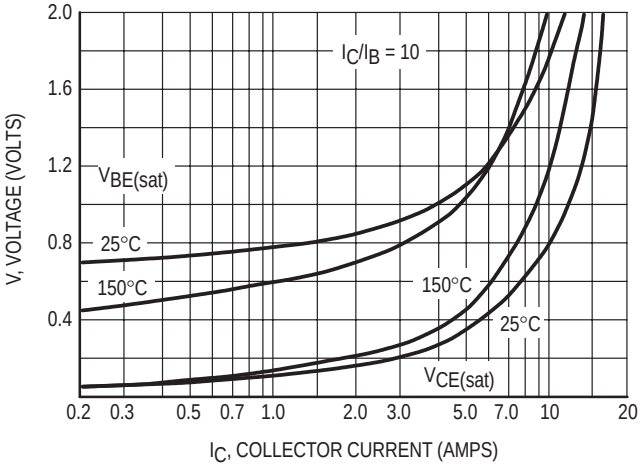


Figure 6. “On” Voltage

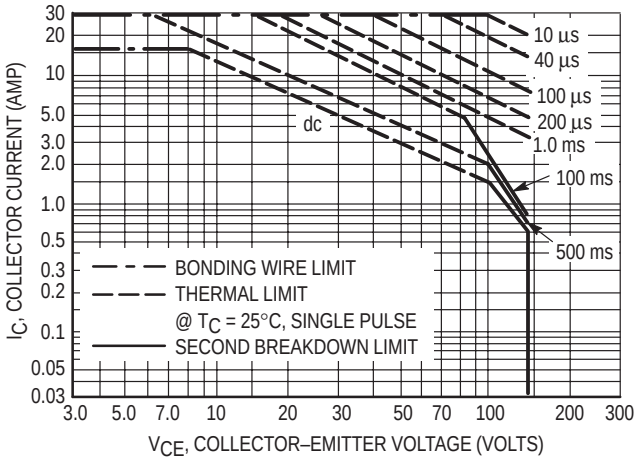


Figure 7. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 200°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

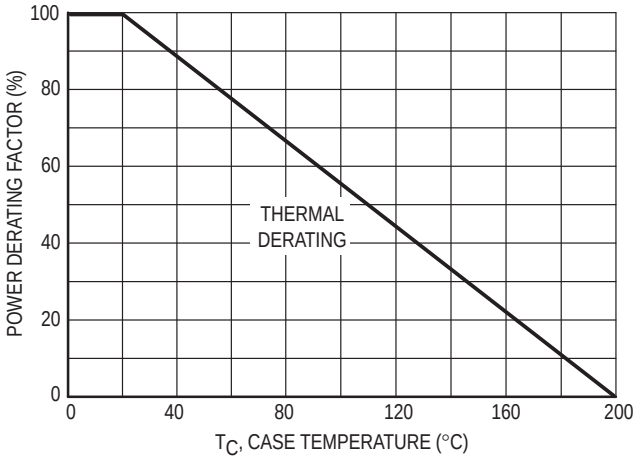


Figure 8. Power Derating

Silicon PNP Power Transistors

2N3791
2N3792

. . . designed for medium–speed switching and amplifier applications. These devices feature:

- Total Switching Time @ 3.0 A ≈1.0 μs (typ)
- h_{FE} (min) = 50 @ 1.0 A
- Low $V_{CE(sat)}$ = 0.5 V (typ) @ I_C = 5.0 A, I_B = 0.5 A
- Excellent Safe Area Limits
- Complementary NPN available — 2N3716

10 AMPERE
POWER TRANSISTORS
PNP SILICON
60–80 VOLTS
150 WATTS

CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	2N3791	2N3792	Unit
Collector–Base Voltage	V_{CB}	60	80	Volts
Collector–Emitter Voltage	V_{CEO}	60	80	Volts
Emitter–Base Voltage	V_{EB}	7.0	7.0	Volts
Collector Current (Continuous)	I_C	10	10	Amps
Base Current (Continuous)	I_B	4.0	4.0	Amps
Power Dissipation	P_D	150	150	Watts
Thermal Resistance	θ_{JC}	1.17	1.17	°C/W
Junction Operating and Storage Temperature Range	T_J, T_{stg}	–65 to +200		°C

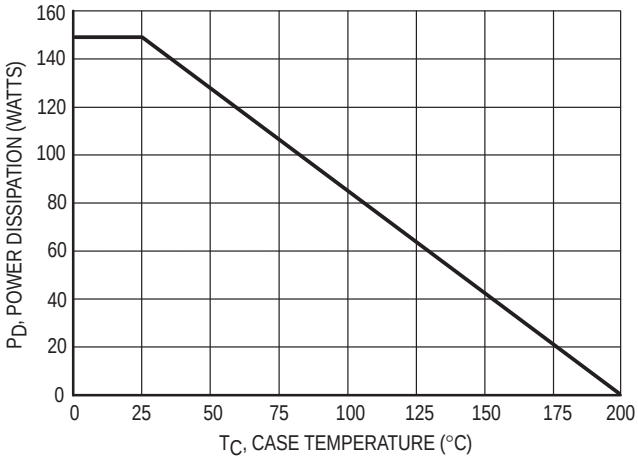


Figure 1. Power–Temperature Derating Curve

Safe Area Limits are indicated by Figures 15, 16. Both limits are applicable and must be observed.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N3791		60	—	
	2N3792		80	—	
Collector–Emitter Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, V_{BE} = – 1.5 Vdc)	2N3791		—	1.0	
(V_{CE} = 80 Vdc, V_{BE} = – 1.5 Vdc)	2N3792		—	1.0	
(V_{CE} = 60 Vdc, V_{BE} = – 1.5 Vdc, T_C = 150°C)	2N3791		—	5.0	
(V_{CE} = 80 Vdc, V_{BE} = – 1.5 Vdc, T_C = 150°C)	2N3792		—	5.0	
Emitter–Base Cutoff Current		I_{EBO}	—	5.0	mAdc
(V_{EB} = 7.0 Vdc)	All Types				
DC Current Gain (1)		h_{FE}			—
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)			50	180	
(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)			30	—	
Collector–Emitter Saturation Voltage (1)		$V_{CE(sat)}$	—	1.0	Vdc
(I_C = 5.0 Adc, I_B = 0.5 Adc)					
Base–Emitter On Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 5.0 A, V_{CE} = 2.0 Vdc)			—	1.8	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)			—	4.0	
Current–Gain — Bandwidth Product		f_T	4.0	—	MHz
(V_{CE} = 10 Vdc, I_C = 0.5 Adc, f = 1.0 MHz)					

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

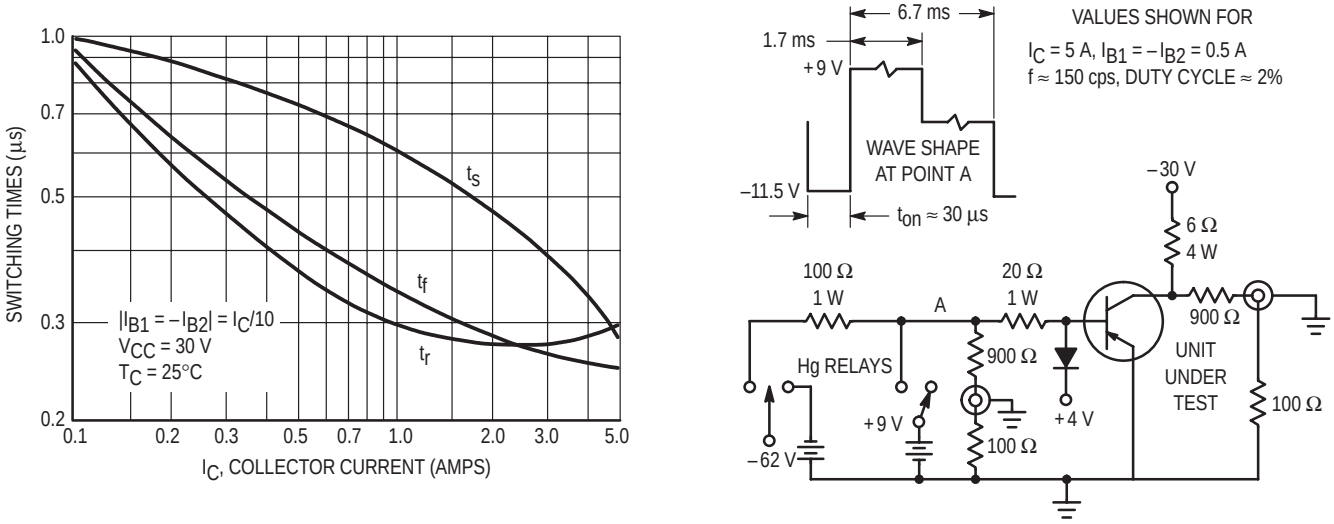


Figure 2. Typical Switching Times and Test Circuit

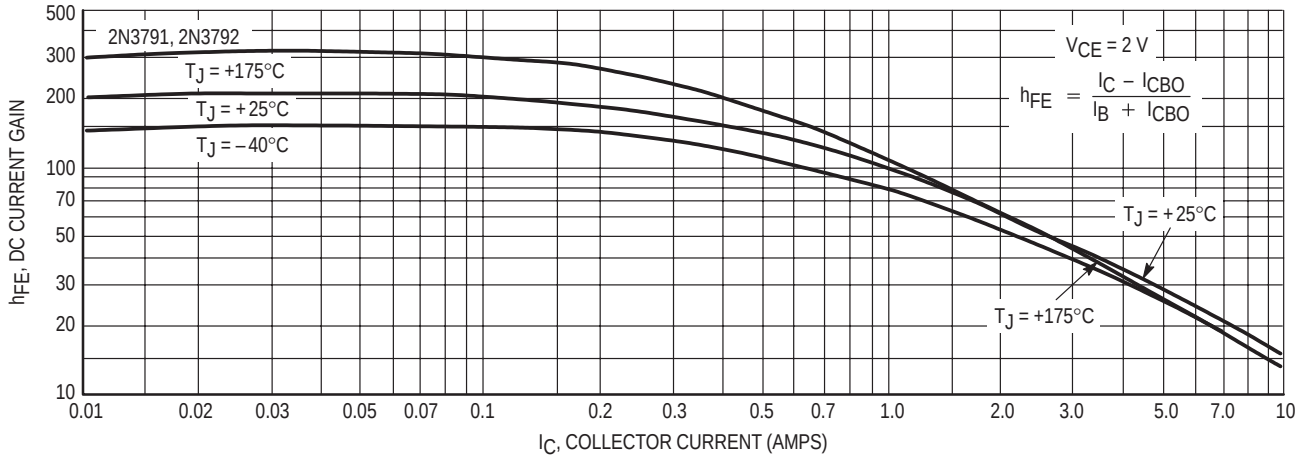


Figure 3. Current Gain Variations

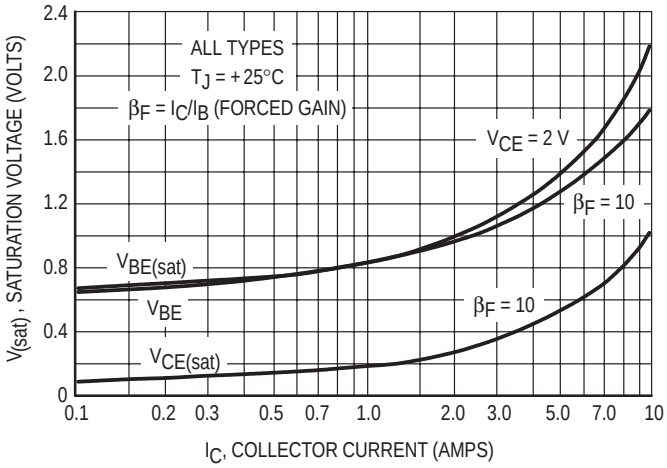


Figure 4. Saturation Voltages

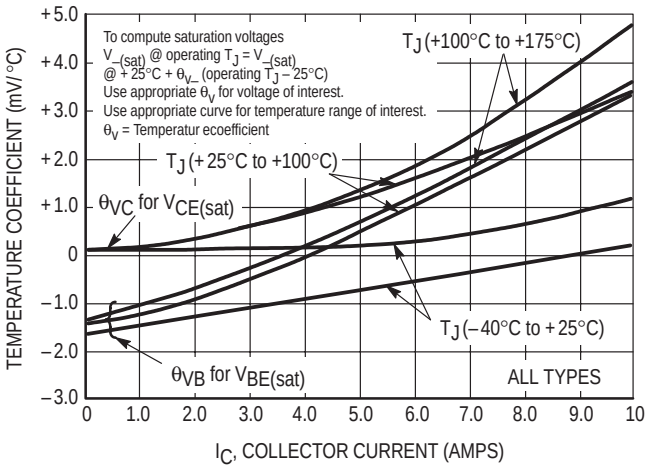


Figure 5. Temperature Coefficients

SAFE OPERATING AREAS

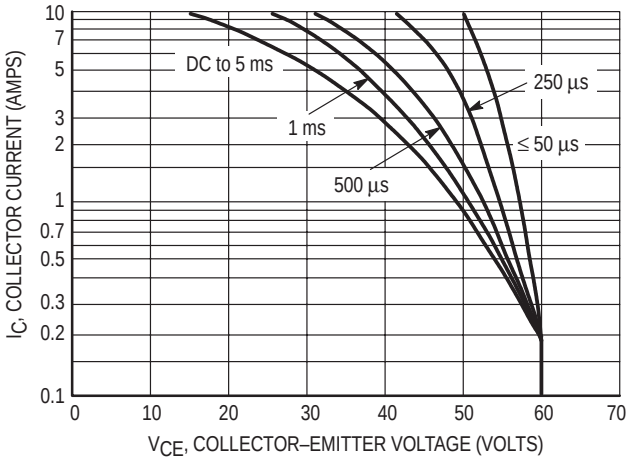


Figure 6. 2N3789, 2N3791

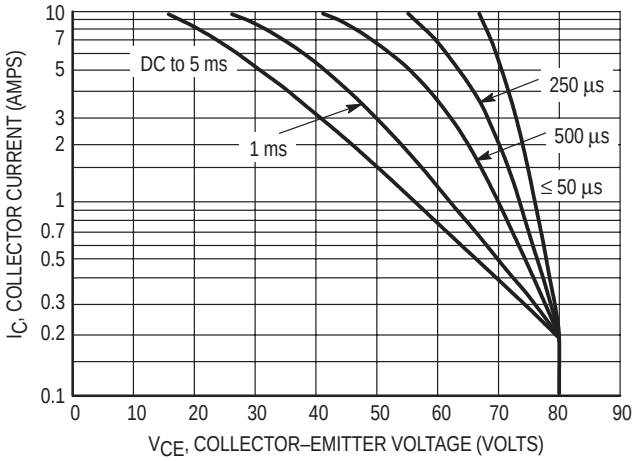


Figure 7. 2N3790, 2N3792

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not go into secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a collector–emitter short. (Duty cycle of the excursions make no significant change in these safe areas.) To insure operation below the maximum T_J, the power–temperature derating curve must be observed for both steady state and pulse power conditions.

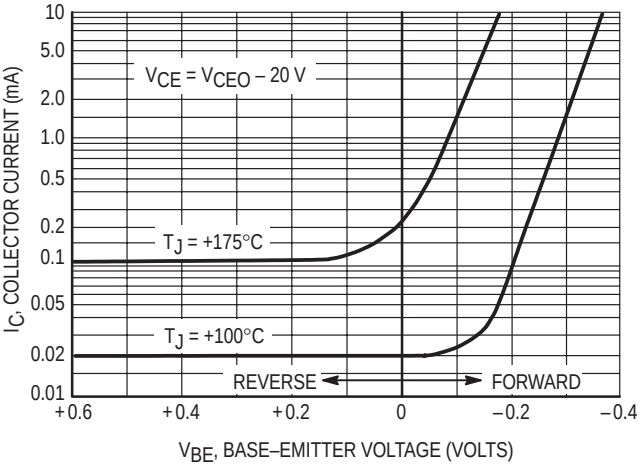


Figure 8. Cut–Off Region Transconductance

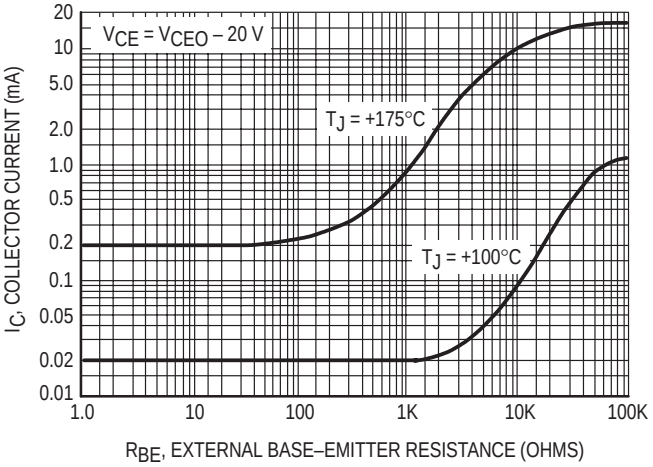


Figure 9. Collector Cut–Off Current versus Base–Emitter Resistance

2N4347
(See 2N3442)

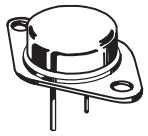
PNP Silicon High-Power Transistors

2N4398
2N4399
2N5745

. . . designed for use in power amplifier and switching circuits.

- Low Collector–Emitter Saturation Voltage —
  I_C = 15 Adc, $V_{CE(sat)}$ = 1.0 Vdc (Max) 2N4398,99
  = 1.5 Vdc (Max) 2N5745
- DC Current Gain Specified — 1.0 to 30 Adc
- Complements to NPN 2N5301, 2N5302, 2N5303

20, 30 AMPERE
POWER TRANSISTORS
PNP SILICON
40 – 60 – 180 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	2N4398	2N4399	2N5745	Unit
Collector–Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector–Base Voltage	V_{CB}	40	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	30 50	30 50	20 50	Adc
Base Current — Continuous Peak	I_B	7.5 15			Adc
Total Device Dissipation @ T_A = 25°C** Derate above 25°C	P_D	5.0 28.6			Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.15			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	35	°C/W

* Indicates JEDEC Registered Data.
** Motorola guarantees this data in addition to JEDEC Registered Data.

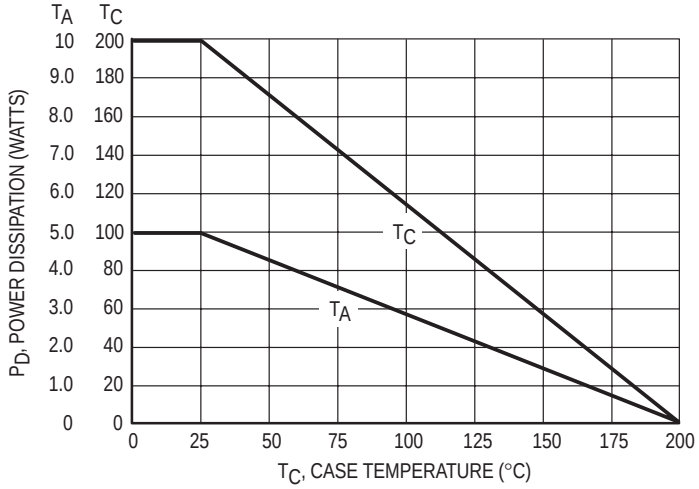


Figure 1. Power–Temperature Derating Curve

Safe Area Curves are indicated by Figure 13. All limits are applicable and must be observed.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N4398		40	—	
	2N4399		60	—	
	2N5745		80	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N4398		—	5.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N4399		—	5.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N5745		—	5.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4398		—	5.0	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N4399		—	5.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5745		—	5.0	
(V_{CE} = 30 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N4398, 2N4399		—	10	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5745		—	10	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N4398		—	1.0	
(V_{CB} = 60 Vdc, I_E = 0)	2N4399		—	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5745		—	1.0	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			—
(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	All Types		40	—	
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5745		15	60	
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N4398, 2N4399		15	60	
(I_C = 20 Adc, V_{CE} = 2.0 Vdc)	2N5745		5.0	—	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N4398, 2N4399		5.0	—	
Collector–Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)	2N4398, 2N4399		—	0.75	
	2N5745		—	1.0	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N4398, 2N4399		—	1.0	
	2N5745		—	1.5	
(I_C = 20 Adc, I_B = 2.0 Adc)	2N4398, 2N4399		—	2.0	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5745		—	2.0	
(I_C = 30 Adc, I_B = 6.0 Adc)	2N4398, 2N4399		—	4.0	
Base–Emitter Saturation Voltage (1)		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)**	2N4398, 2N4399		—	1.6	
	2N5745		—	1.7	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N4398, 2N4399		—	1.85	
	2N5745		—	2.0	
(I_C = 20 Adc, I_B = 2.0 Adc)**	2N4398, 2N4399		—	2.5	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5745		—	2.5	
Base–Emitter On Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5745		—	1.5	
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N4398, 2N4399		—	1.7	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N5745		—	2.5	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N4398, 2N4399		—	3.0	

* Indicates JEDEC Registered Data. (continued)

** Motorola Guarantees this Data in Addition to JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

ELECTRICAL CHARACTERISTICS — continued

Characteristic		Symbol	Min	Max	Unit
DYNAMIC CHARACTERISTICS					
Current–Gain Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	2N4398, 2N4399 2N5745	f_T	 4.0 2.0	 — —	MHz
Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	40	—	—
SWITCHING CHARACTERSTICS					
Rise Time	2N4398, 2N4399 2N5745	t_r	— —	0.4 1.0	μs
Storage Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc) 2N4396, 2N4399 2N5745	t_s	— —	1.5 2.0	μs
Fall Time	2N4398, 2N4399 2N5746	t_f	— —	0.6 1.0	μs

(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

SWITCHING TIME EQUIVALENT TEST CIRCUITS

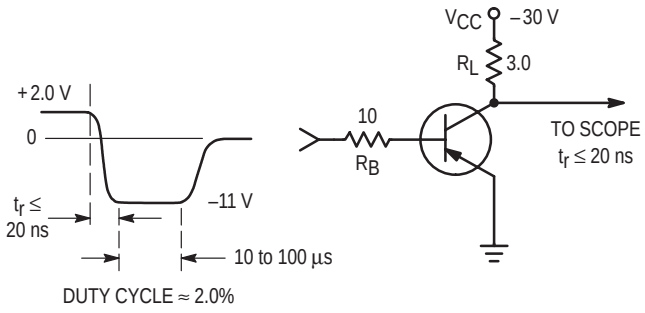


Figure 2. Turn–On Time

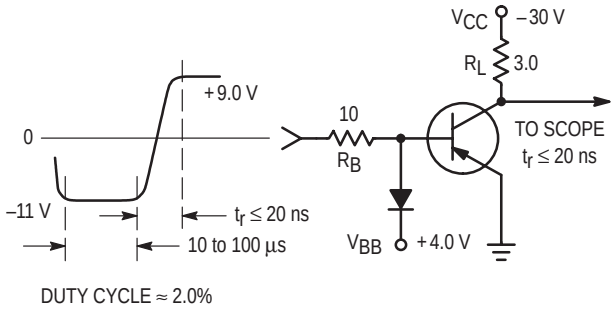


Figure 3. Turn–Off Time

TYPICAL “ON” REGION CHARACTERISTICS

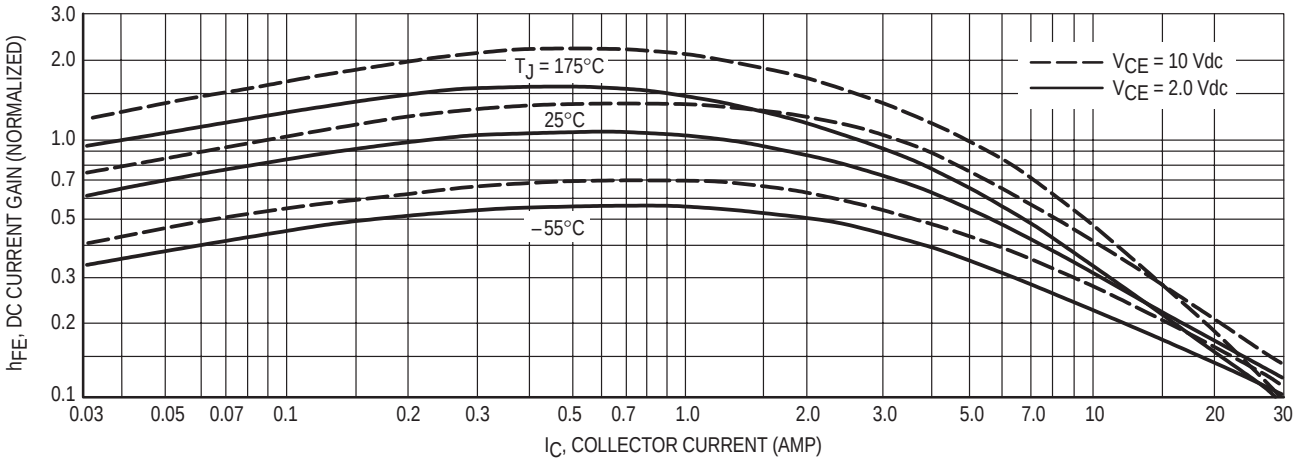


Figure 4. DC Current Gain

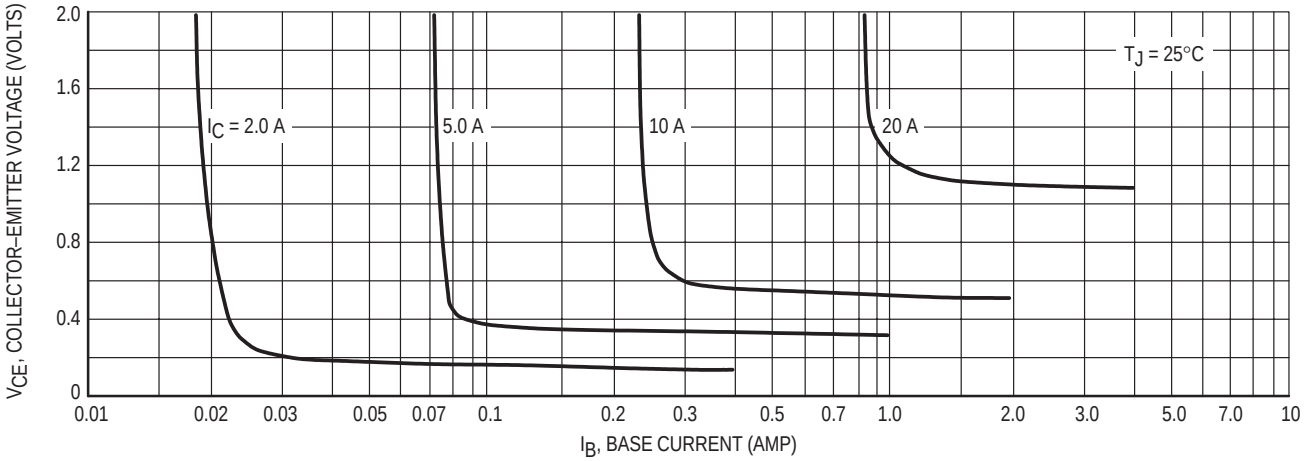


Figure 5. Collector Saturation Region

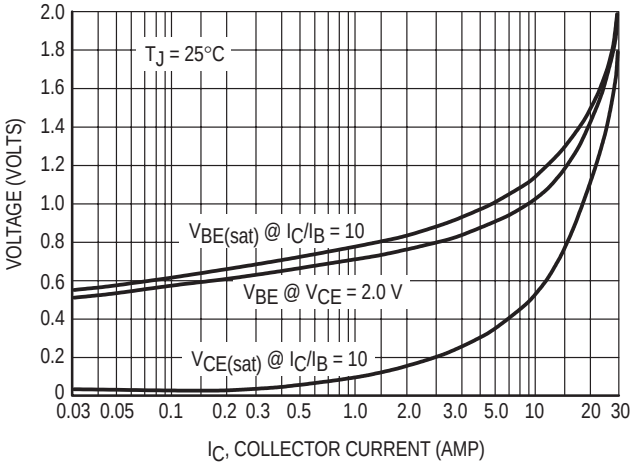


Figure 6. “On” Voltages

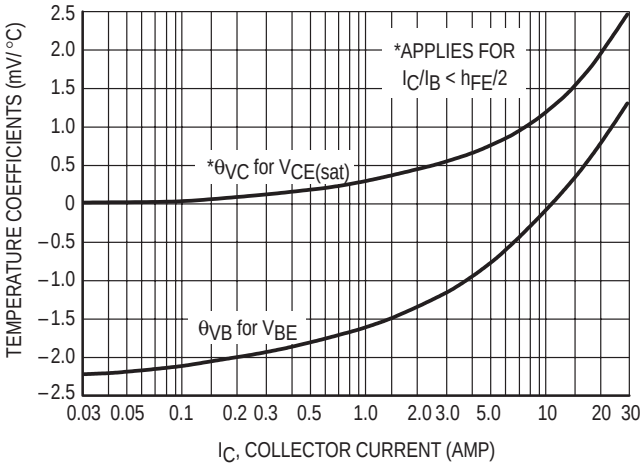


Figure 7. Temperature Coefficients

RATINGS AND THERMAL DATA

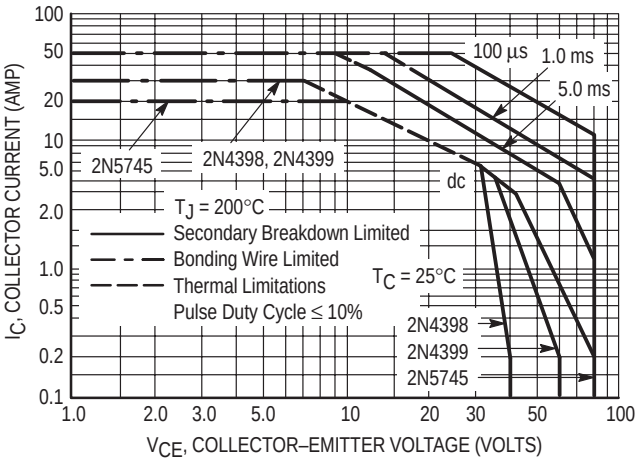


Figure 8. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 8 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

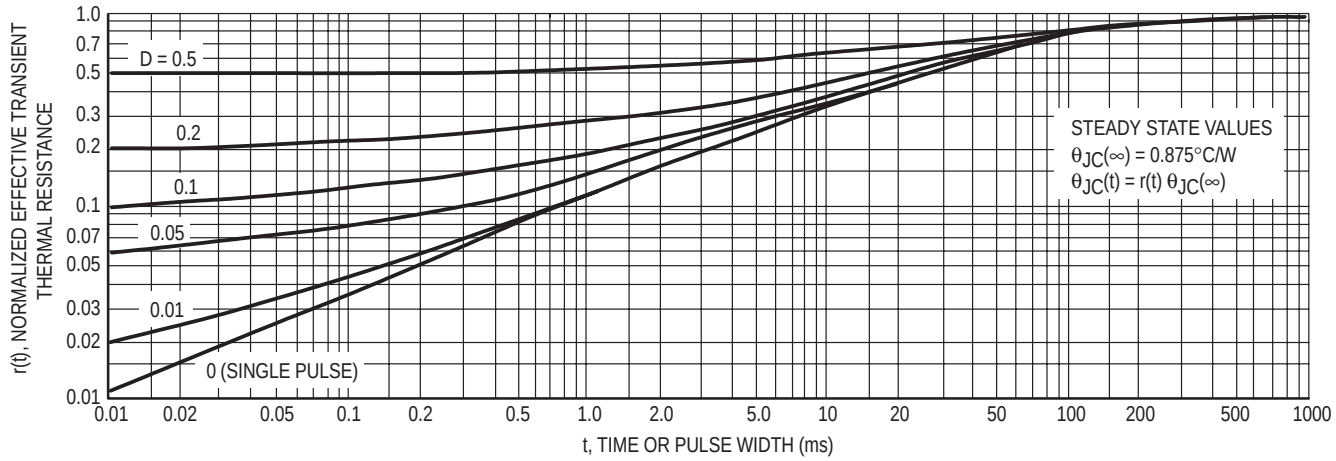
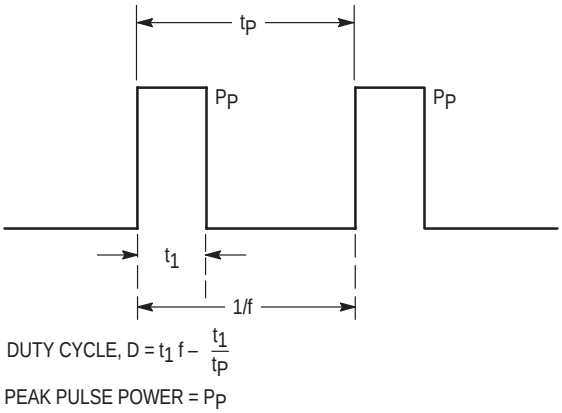


Figure 9. Thermal Response

DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA



A train of periodical power pulses can be represented by the model as shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 9 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 9 by the steady state value $\theta_{JC}(\infty)$.

Example:

The 2N4398 is dissipating 100 watts under the following conditions: t_1 = 1.0 ms, t_P = 5.0 ms. (D = 0.2)

Using Figure 9, at a pulse width of 1.0 ms and D = 0.2, the reading of r (t) is 0.28.

The peak rise in junction temperature is therefore

$T = r(t) \times P_P \times \theta_{JC}(\infty) = 0.28 \times 100 \times 0.875 = 24.5°C$

Medium-Power Plastic PNP Silicon Transistors

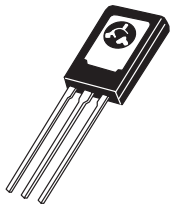
2N4918 thru 2N4920*

*Motorola Preferred Device

. . . designed for driver circuits, switching, and amplifier applications. These high–performance plastic devices feature:

- Low Saturation Voltage — $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 1.0 Amp
- Excellent Power Dissipation Due to Thermopad Construction — P_D = 30 W @ T_C = 25°C
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Amp
- Complement to NPN 2N4921, 2N4922, 2N4923

3 AMPERE GENERAL–PURPOSE POWER TRANSISTORS 40–80 VOLTS 30 WATTS



CASE 77–08 TO–225AA TYPE

***MAXIMUM RATINGS**

Ratings	Symbol	2N4918	2N4919	2N4920	Unit
Collector–Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector–Base Voltage	V_{CB}	40	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous (1)	I_C*	1.0 3.0			Adc
Base Current	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.24			Watts W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS (2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

* Indicates JEDEC Registered Data for 2N4918 Series.

(1) The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements. The 3.0 Amp maximum value is based upon actual current–handling capability of the device (See Figure 5).

(2) Recommend use of thermal compound for lowest thermal resistance.

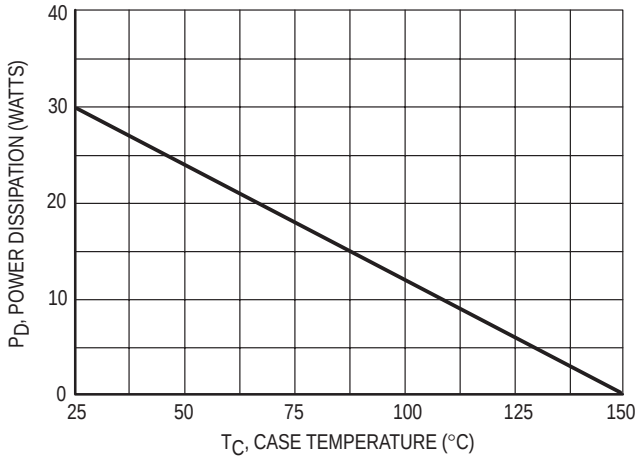


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	2N4918 2N4919 2N4920	$V_{CEO(sus)}$	 40 60 80	 — — —	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	2N4918 2N4919 2N4920	I_{CEO}	 — — —	 0.5 0.5 0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)		I_{CEX}	 — —	 0.1 0.5	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		h_{FE}	 40 30 10	 — 150 —	—
Collector–Emitter Saturation Voltage (1) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	—	0.6	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$	—	1.3	Vdc
Base–Emitter On Voltage (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	—	1.3	Vdc
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	3.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	100	pF
Small–Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	—	—

* Indicates JEDEC Registered Data.

(1) Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%

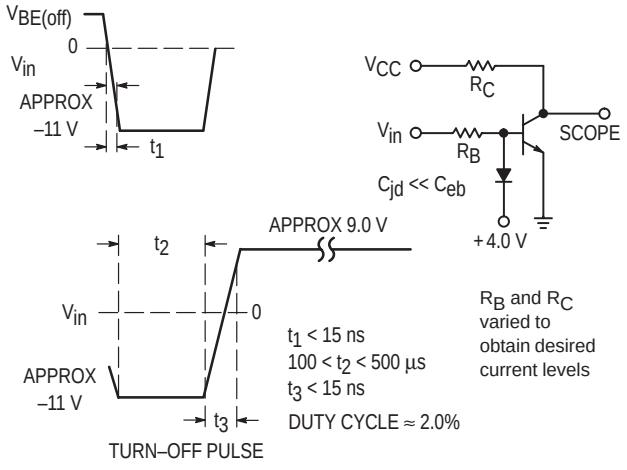


Figure 2. Switching Time Equivalent Test Circuit

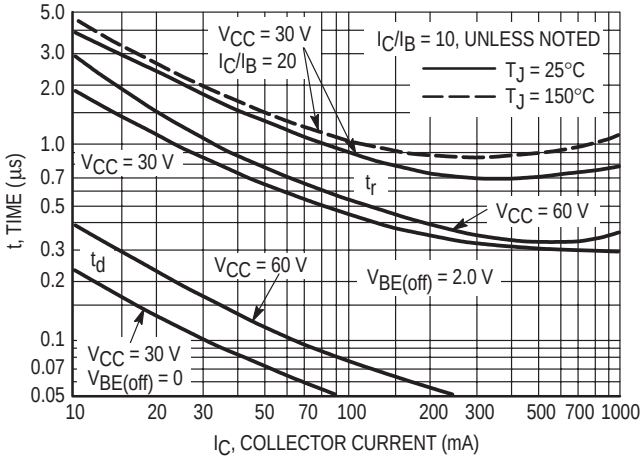


Figure 3. Turn–On Time

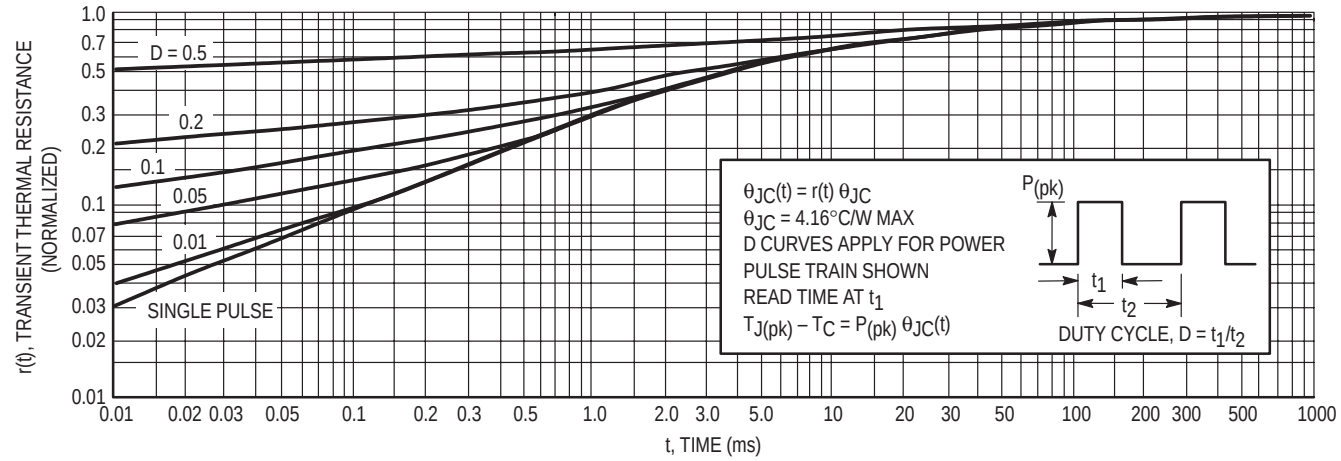


Figure 4. Thermal Response

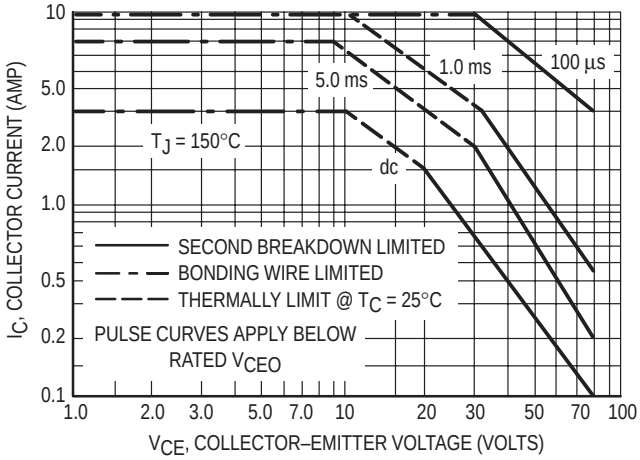


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

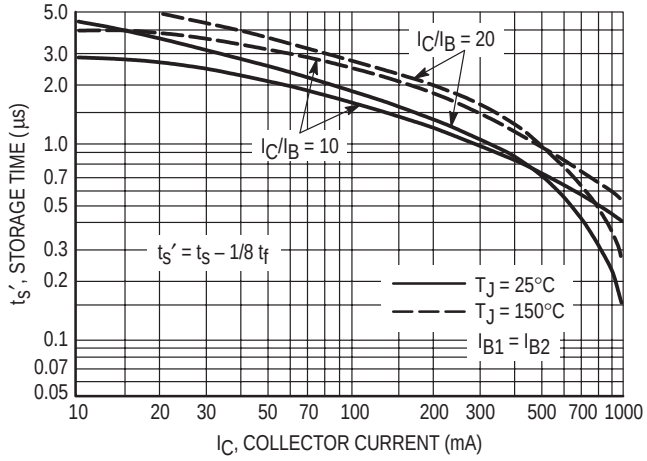


Figure 6. Storage Time

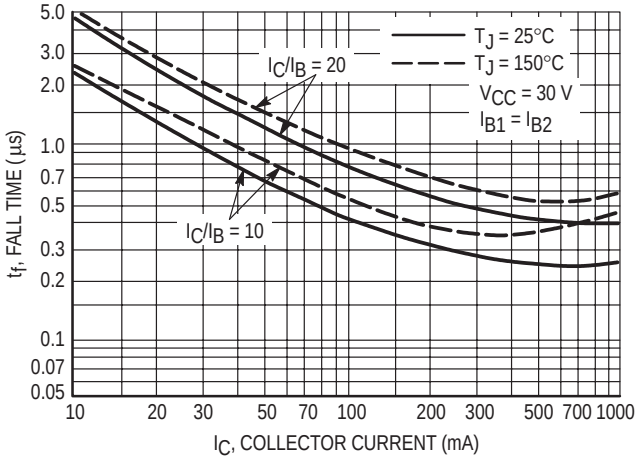


Figure 7. Fall Time

TYPICAL DC CHARACTERISTICS

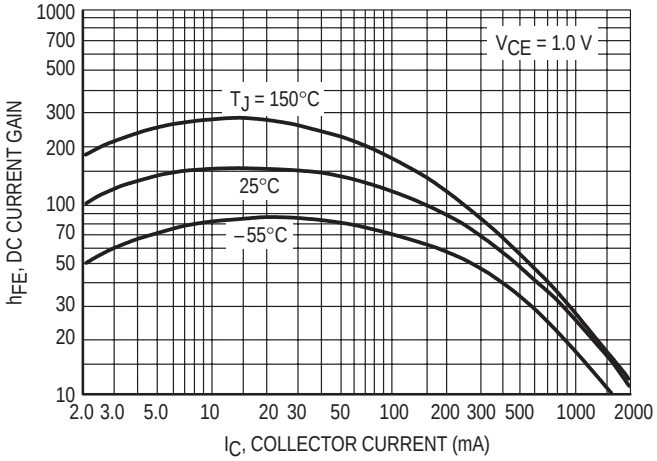


Figure 8. Current Gain

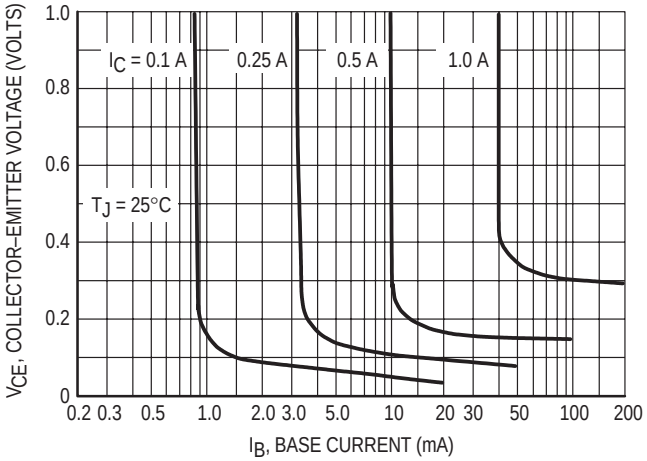


Figure 9. Collector Saturation Region

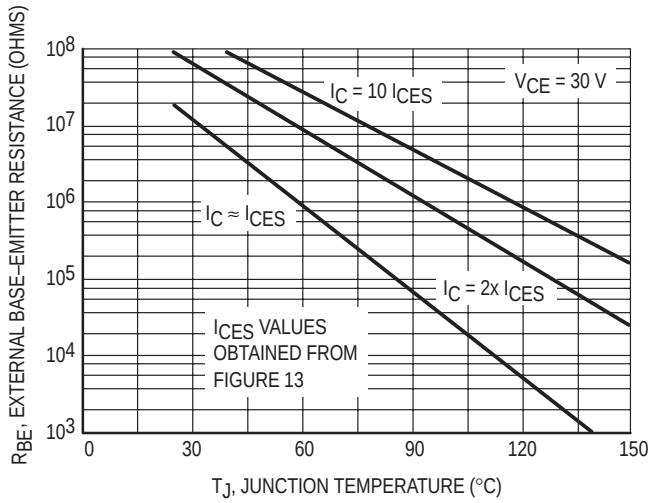


Figure 10. Effects of Base–Emitter Resistance

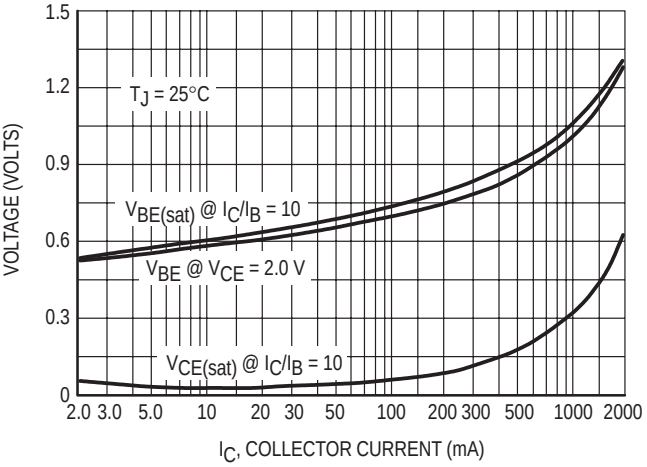


Figure 11. "On" Voltage

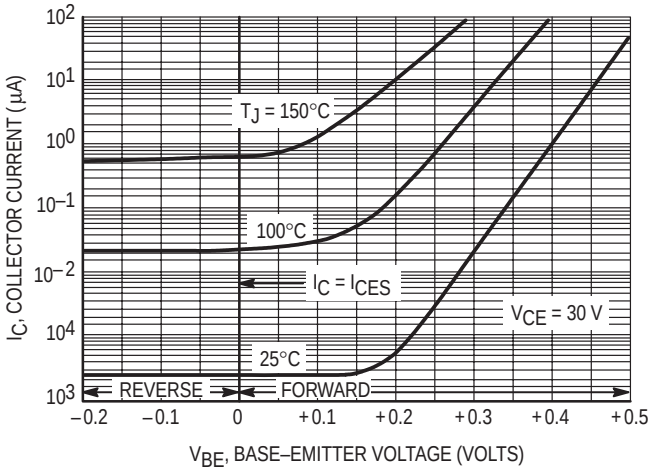


Figure 12. Collector Cut–Off Region

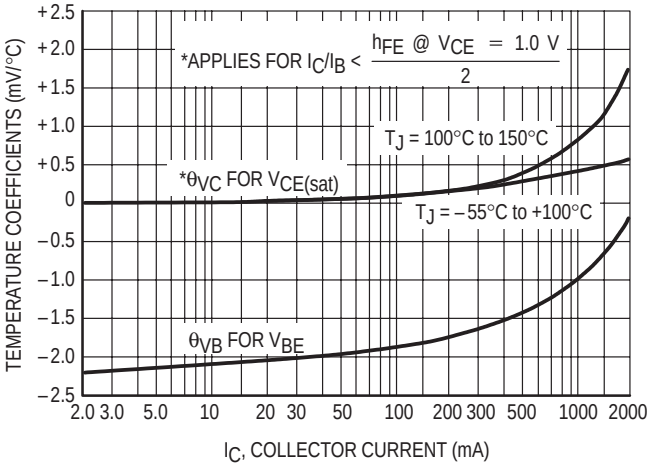


Figure 13. Temperature Coefficients

Medium-Power Plastic NPN Silicon Transistors

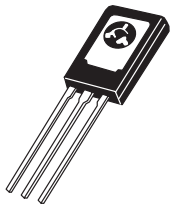
2N4921 thru 2N4923*

*Motorola Preferred Device

. . . designed for driver circuits, switching, and amplifier applications. These high–performance plastic devices feature:

- Low Saturation Voltage — $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 1.0 Amp
- Excellent Power Dissipation Due to Thermopad Construction — P_D = 30 W @ T_C = 25°C
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Amp
- Complement to PNP 2N4918, 2N4919, 2N4920

1 AMPERE GENERAL–PURPOSE POWER TRANSISTORS 40–80 VOLTS 30 WATTS



CASE 77–08 TO–225AA TYPE

***MAXIMUM RATINGS**

Rating	Symbol	2N4921	2N4922	2N4923	Unit
Collector–Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector–Base Voltage	V_{CB}	40	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous (1)	I_C	1.0 3.0			Adc
Base Current — Continuous	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.24			Watts W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS (2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

(1) The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements. The 3.0 Amp maximum value is based upon actual current handling capability of the device (see Figures 5 and 6)

(2) Recommend use of thermal compound for lowest thermal resistance.

* Indicates JEDEC Registered Data.

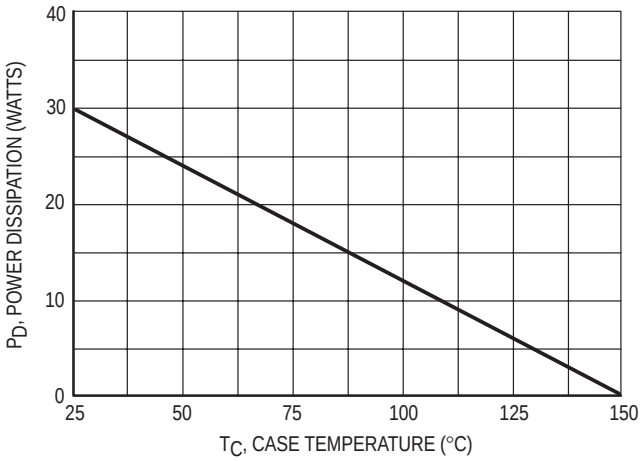


Figure 1. Power Derating

Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	2N4921	$V_{CEO(sus)}$	40	—	Vdc
	2N4922		60	—	
	2N4923		80	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N4921		—	0.5	
(V_{CE} = 30 Vdc, I_B = 0)	2N4922		—	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	2N4923		—	0.5	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc)			—	0.1	
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)			—	0.5	
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			—
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)			40	—	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			30	150	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)			10	—	
Collector–Emitter Saturation Voltage (1) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	—	0.6	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$	—	1.3	Vdc
Base–Emitter On Voltage (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	—	1.3	Vdc
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	3.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	100	pF
Small–Signal Current Gain (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	—	—

(1) Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%.
* Indicates JEDEC Registered Data.

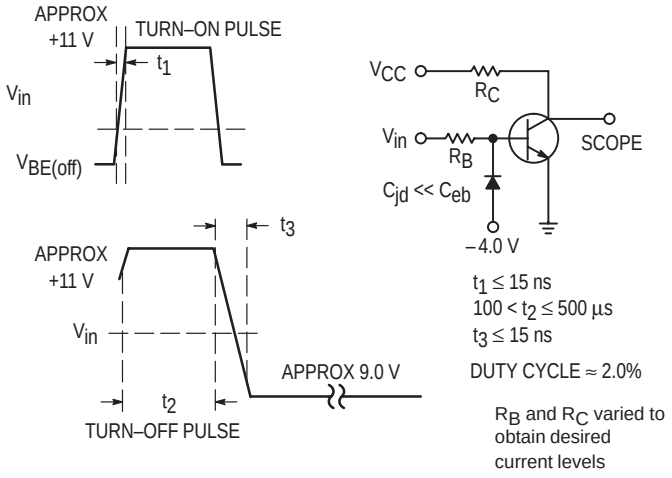


Figure 2. Switching Time Equivalent Circuit

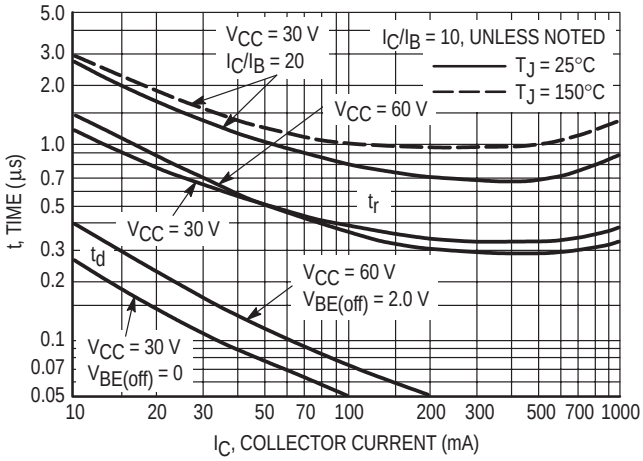


Figure 3. Turn–On Time

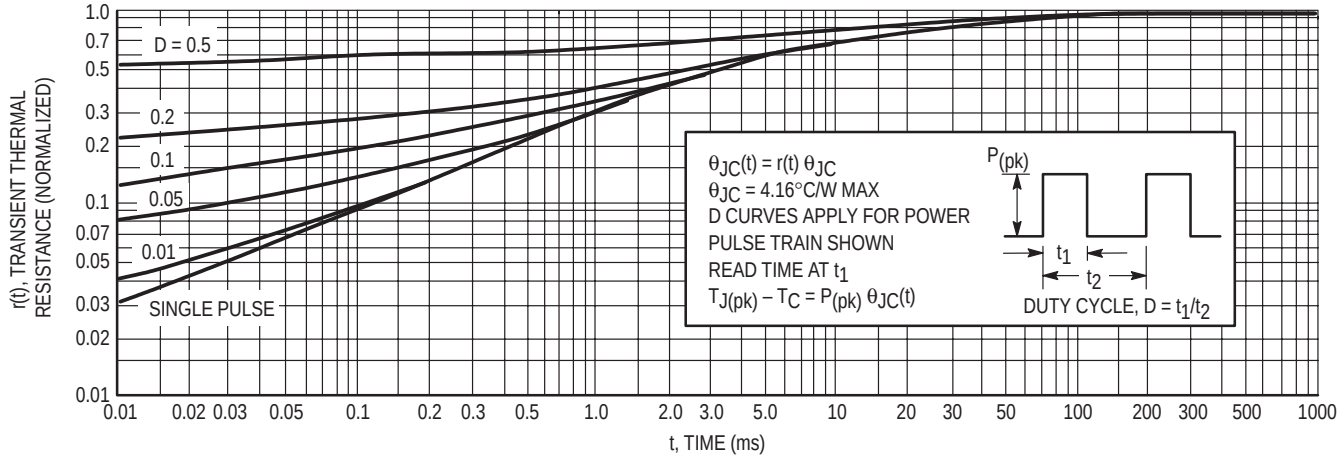


Figure 4. Thermal Response

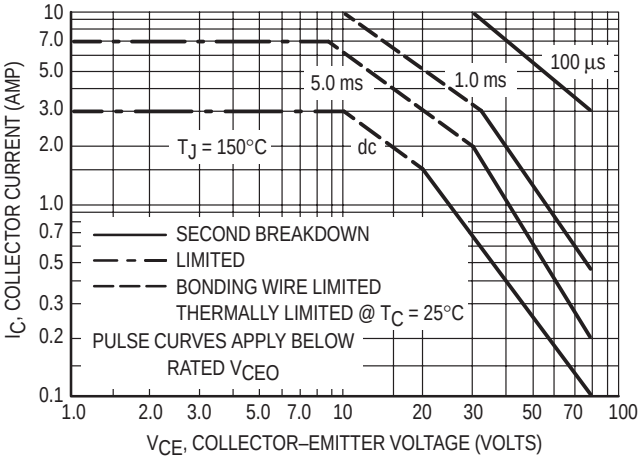


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

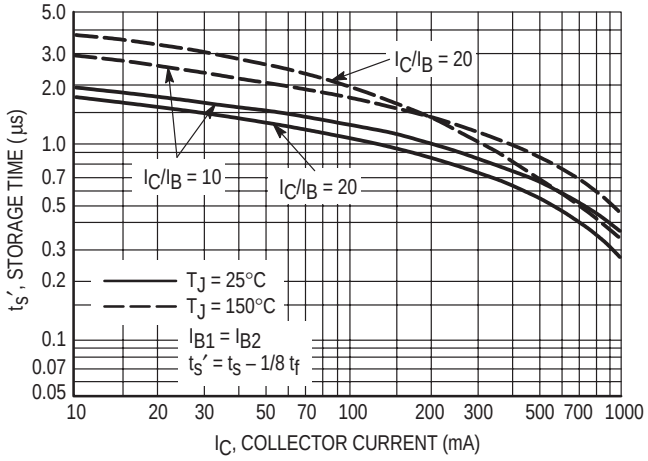


Figure 6. Storage Time

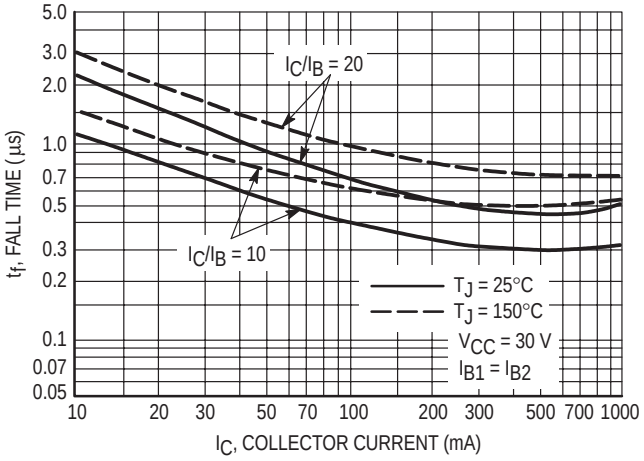


Figure 7. Fall Time

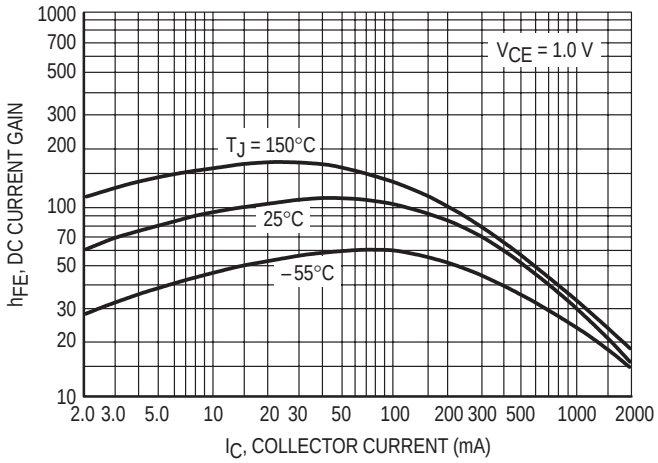


Figure 8. Current Gain

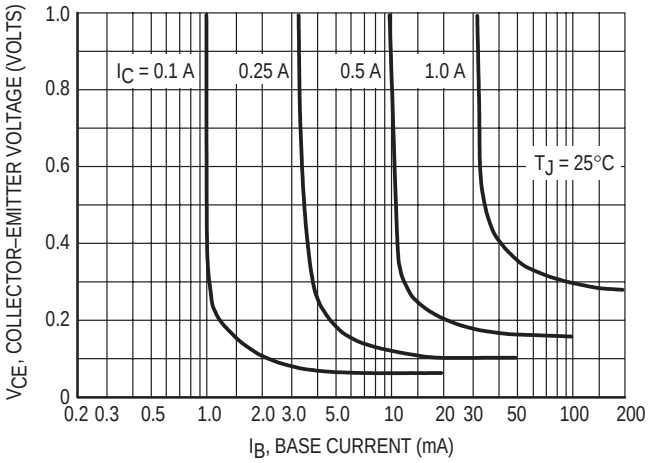


Figure 9. Collector Saturation Region

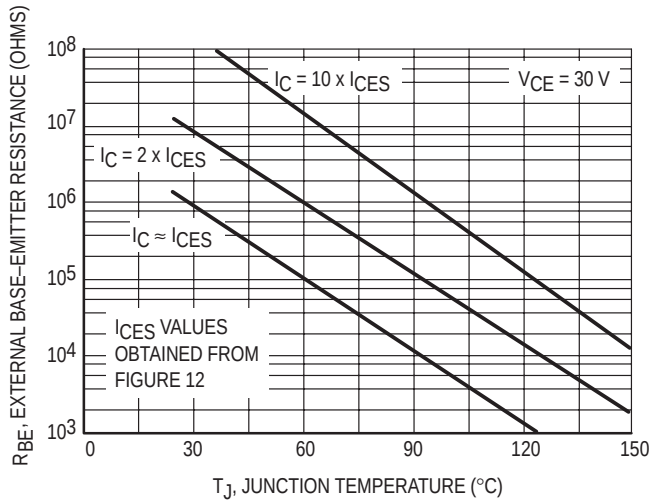


Figure 10. Effects of Base–Emitter Resistance

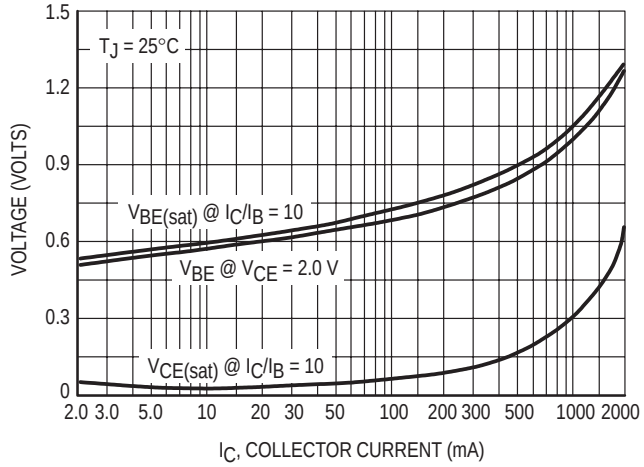


Figure 11. “On” Voltage

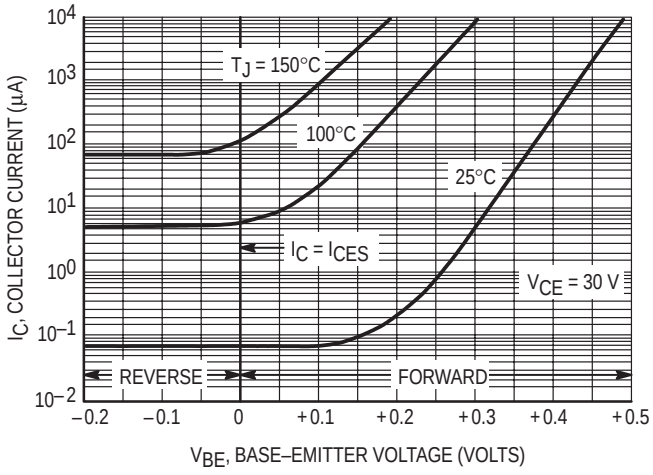


Figure 12. Collector Cut–Off Region

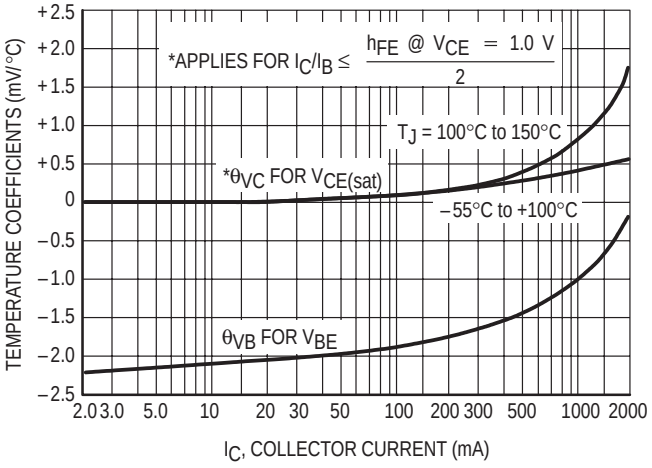


Figure 13. Temperature Coefficients

2N5038*
2N5039

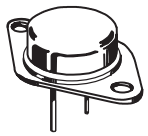
*Motorola Preferred Device

NPN Silicon Transistors

. . . fast switching speeds and high current capacity ideally suit these parts for use in switching regulators, inverters, wide–band amplifiers and power oscillators in industrial and commercial applications.

- High Speed — t_f = 0.5 μs (Max)
- High Current — $I_{C(max)}$ = 30 Amps
- Low Saturation — $V_{CE(sat)}$ = 2.5 V (Max) @ I_C = 20 Amps

20 AMPERE
NPN SILICON
POWER TRANSISTORS
75 and 90 VOLTS
140 WATTS



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	2N5038	2N5039	Unit
Collector–Base Voltage	V_{CBO}	150	120	Vdc
Collector–Emitter Voltage	V_{CEV}	150	120	Vdc
Emitter–Base Voltage	V_{EBO}	7		Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	20 30		Adc
Base Current — Continuous	I_B	5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	140 0.8		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W

* Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 10 ms, Duty Cycle ≤ 50%.

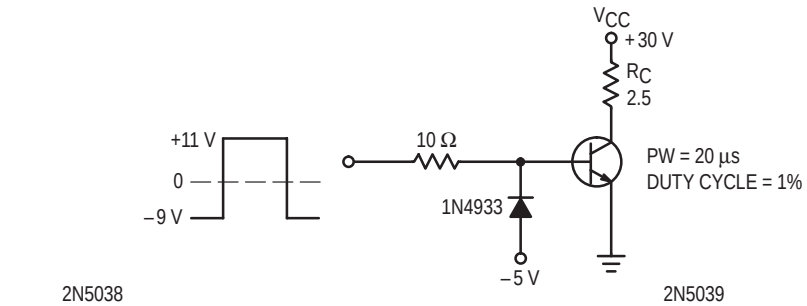


Figure 1. Switching Time Test Circuit

Preferred devices are Motorola recommended choices for future use and best overall value.
REV 7

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5038		90	—	
	2N5039		75	—	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 V)	2N5038		—	50	
(V_{CE} = 110 Vdc, $V_{BE(off)}$ = 1.5 V)	2N5039		—	50	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5038		—	10	
(V_{CE} = 85 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5039		—	10	
Emitter Cutoff Current		I_{EBO}			mAdc
(V_{EB} = 5 Vdc, I_C = 0)	2N5038		—	5	
	2N5039		—	15	
(V_{EB} = 7 Vdc, I_C = 0)	Both		—	50	
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 12 Adc, V_{CE} = 5 Vdc)	2N5038		20	100	
(I_C = 10 Adc, V_{CE} = 5 Vdc)	2N5039		20	100	
Collector–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 5 Adc)		$V_{CE(sat)}$	—	2.5	Vdc
Base–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 5 Adc)		$V_{BE(sat)}$	—	3.3	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common–Emitter Small–Signal Short–Circuit Forward Current Transfer Ratio (I_C = 2 Adc, V_{CE} = 10 Vdc, f = 5 MHz)		$\|h_{fe}\|$	12	—	—
SWITCHING CHARACTERISTICS					
RESISTIVE LOAD					
Rise Time	(V_{CC} = 30 Vdc)	t_r	—	0.5	μs
Storage Time	(I_C = 12 Adc, I_{B1} = I_{B2} = 1.2 Adc) 2N5038	t_s	—	1.5	μs
Fall Time	(I_C = 10 Adc, I_{B1} = I_{B2} = 1 Adc) 2N5039	t_f	—	0.5	μs

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300, μs, Duty Cycle ≤ 2%.

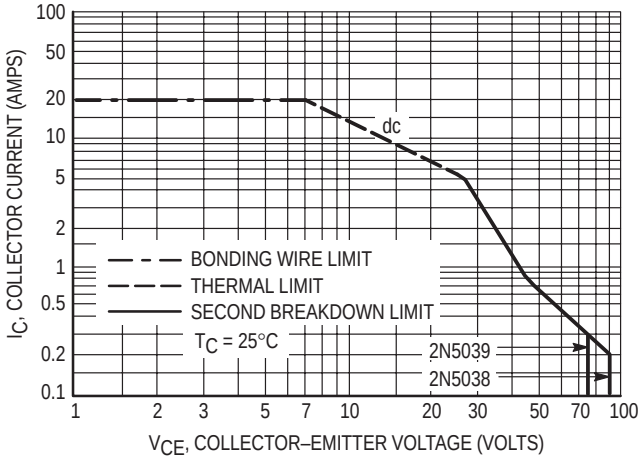


Figure 2. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Second breakdown pulse limits are valid for duty cycles to 10%. At high case temperatures, thermal limitations may reduce the power that can be handled to values less than the limitations imposed by second breakdown.

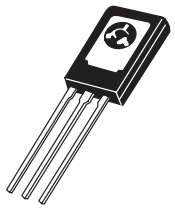
2N5191
2N5192*

*Motorola Preferred Device

Silicon NPN Power Transistors

. . . for use in power amplifier and switching circuits, — excellent safe area limits. Complement to PNP 2N5194, 2N5195.

4 AMPERE
POWER TRANSISTORS
SILICON NPN
60–80 VOLTS
40 WATTS



CASE 77–08
TO–225AA TYPE

***MAXIMUM RATINGS**

Rating	Symbol	2N5191	2N5192	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	 2N5191 2N5192	$V_{CEO(sus)}$	 60 80	 — —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	 2N5191 2N5192	I_{CEO}	 — —	 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	 2N5191 2N5192 2N5191 2N5192	I_{CEX}	 — — — —	 0.1 0.1 2.0 2.0	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	 2N5191 2N5192	I_{CBO}	 — —	 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc

(continued)

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

***ELECTRICAL CHARACTERISTICS — continued** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			—
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	2N5191		25	100	
	2N5192		20	80	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	2N5191		10	—	
	2N5192		7.0	—	
Collector–Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)			—	0.6	
(I_C = 4.0 Adc, I_B = 1.0 Adc)			—	1.4	
Base–Emitter On Voltage (1)		$V_{BE(on)}$	—	1.2	Vdc
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product		f_T	2.0	—	MHz
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)					

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
* Indicates JEDEC Registered Data.

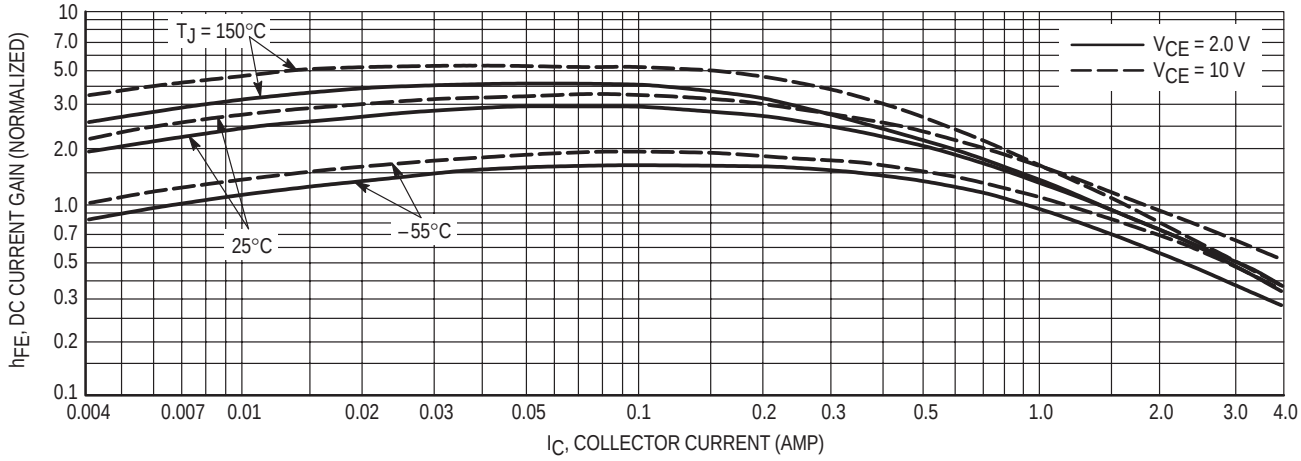


Figure 1. DC Current Gain

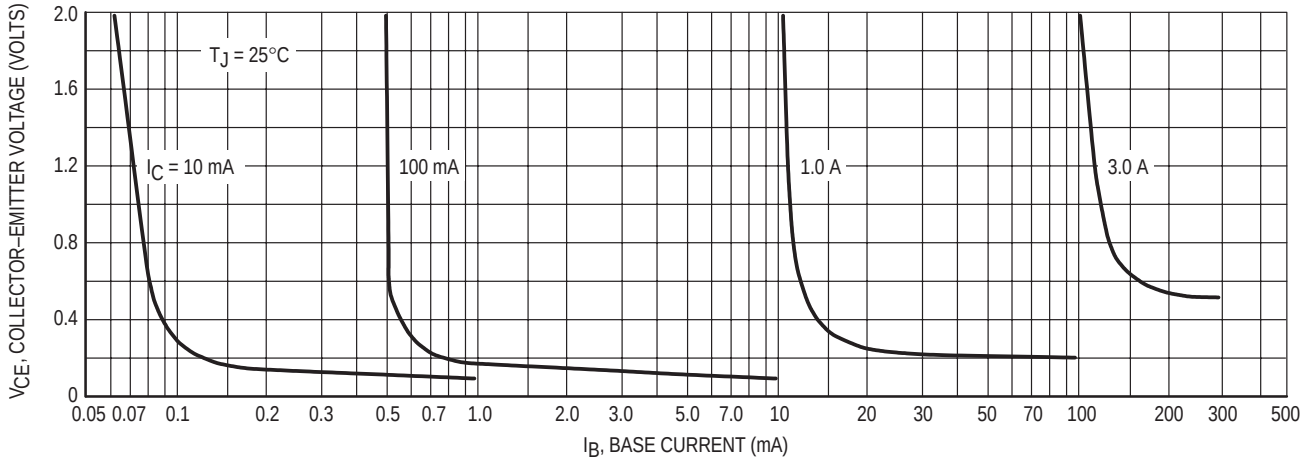


Figure 2. Collector Saturation Region

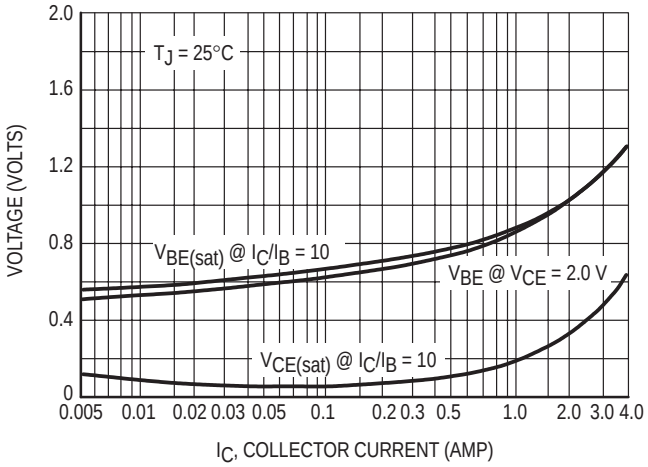


Figure 3. "On" Voltages

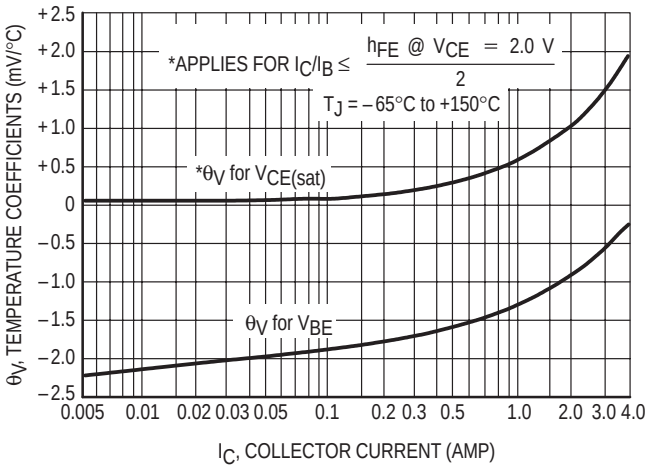


Figure 4. Temperature Coefficients

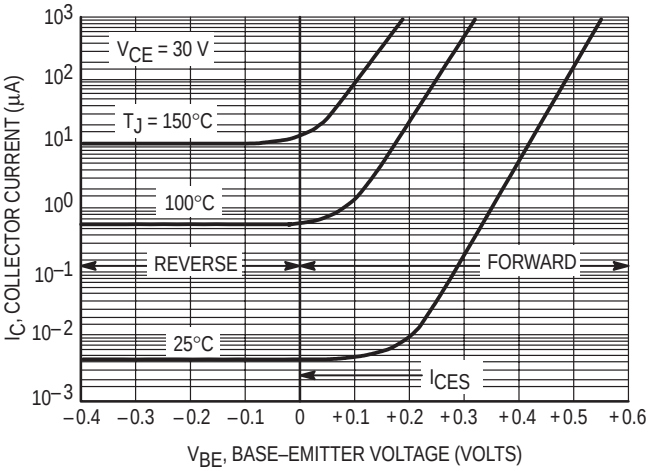


Figure 5. Collector Cut–Off Region

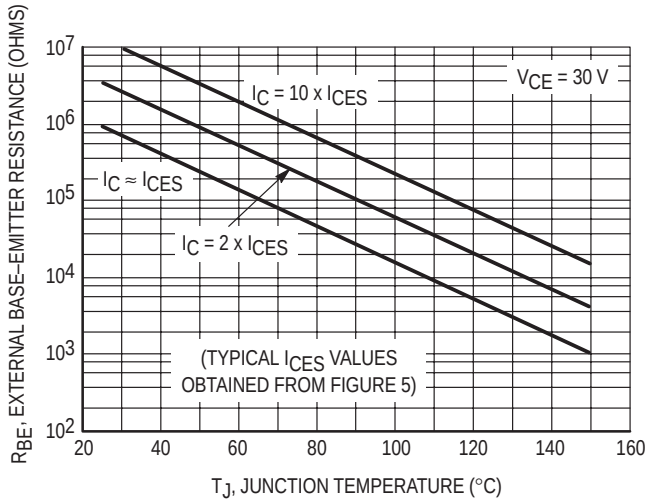


Figure 6. Effects of Base–Emitter Resistance

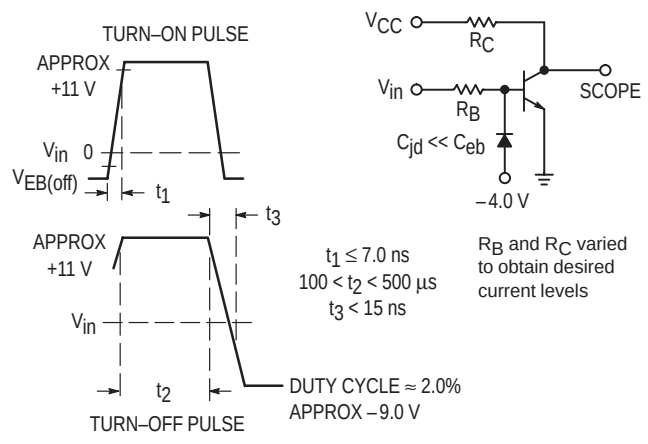


Figure 7. Switching Time Equivalent Test Circuit

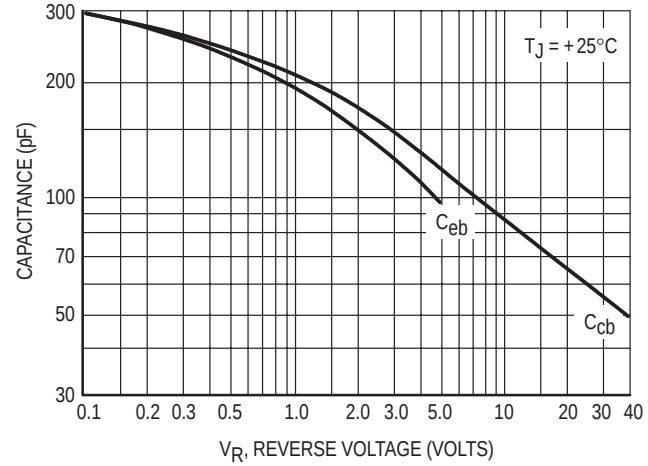


Figure 8. Capacitance

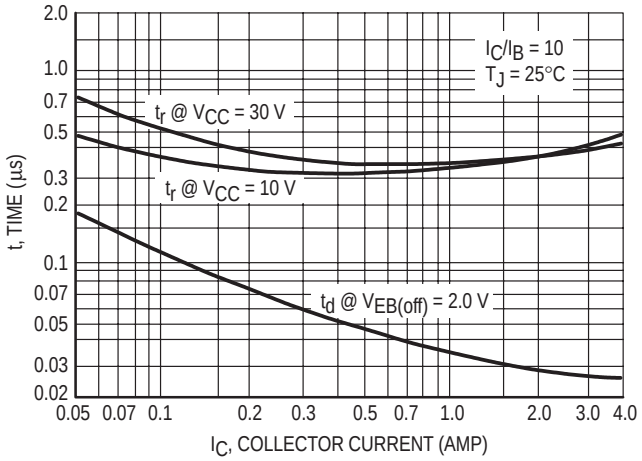


Figure 9. Turn–On Time

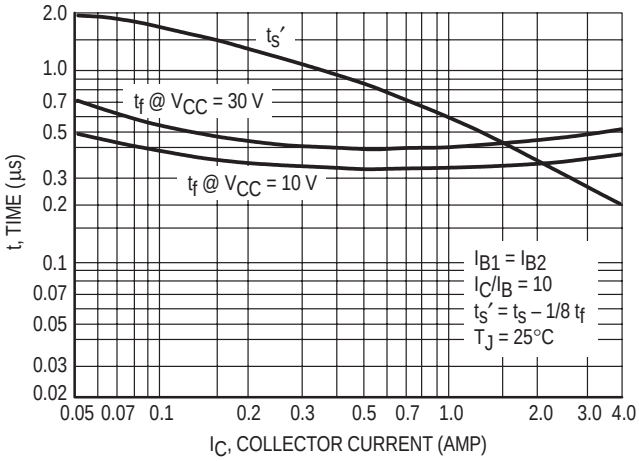


Figure 10. Turn–Off Time

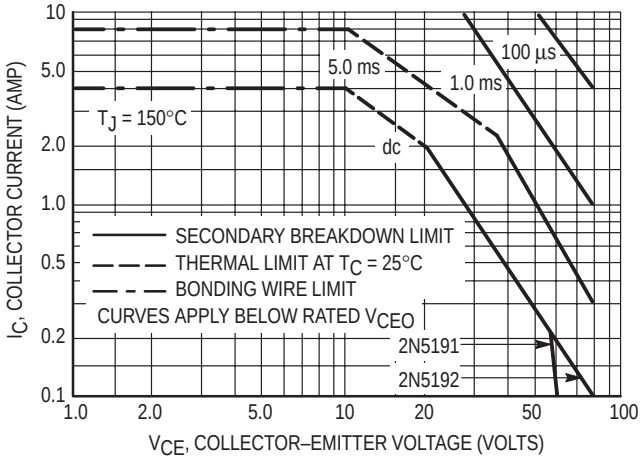


Figure 11. Rating and Thermal Data
Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

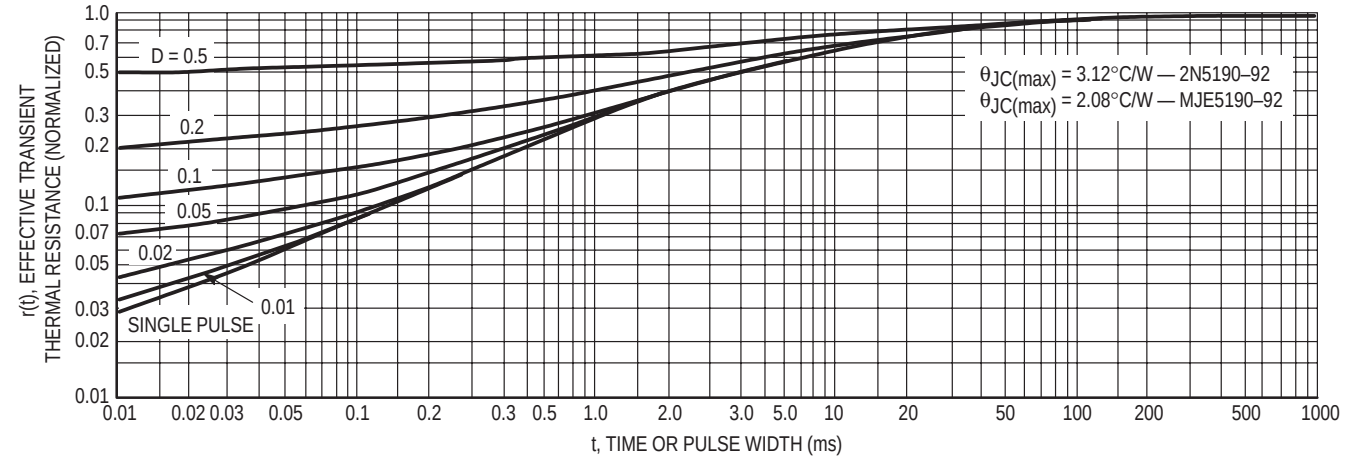
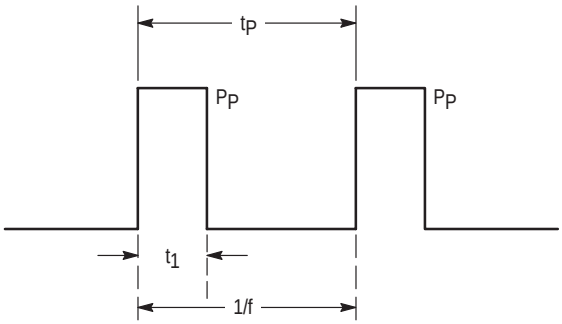


Figure 12. Thermal Response

DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA



DUTY CYCLE, D = $t_1 f = \frac{t_1}{t_P}$

PEAK PULSE POWER = P_P

Figure A

A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:
The 2N5190 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, t_p = 0.5 ms. (D = 0.2).

Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of $r(t_1, D)$ is 0.27.

The peak rise in function temperature is therefore:

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ C$$

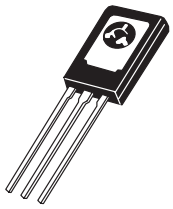
2N5194
2N5195*

*Motorola Preferred Device

Silicon PNP Power Transistors

. . . for use in power amplifier and switching circuits, — excellent safe area limits. Complement to NPN 2N5191, 2N5192

4 AMPERE
POWER TRANSISTORS
SILICON PNP
60–80 VOLTS



CASE 77–08
TO–225AA TYPE

***MAXIMUM RATINGS**

Rating	Symbol	2N5194	2N5195	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C/W

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	 2N5194 2N5195	$V_{CEO(sus)}$	 60 80	 — —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	 2N5194 2N5195	I_{CEO}	 — —	 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	 2N5194 2N5195 2N5194 2N5195	I_{CEX}	 — — — —	 0.1 0.1 2.0 2.0	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	 2N5194 2N5195	I_{CBO}	 — —	 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc

(continued)

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

***ELECTRICAL CHARACTERISTICS — continued** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			—
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)	2N5194		25	100	
	2N5195		20	80	
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	2N5194		10	—	
	2N5195		7.0	—	
Collector–Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 0.15 Adc)			—	0.6	
(I_C = 4.0 Adc, I_B = 1.0 Adc)			—	1.4	
Base–Emitter On Voltage (1)		$V_{BE(on)}$	—	1.2	Vdc
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product		f_T	2.0	—	MHz
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)					

* Indicates JEDEC Registered Data.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

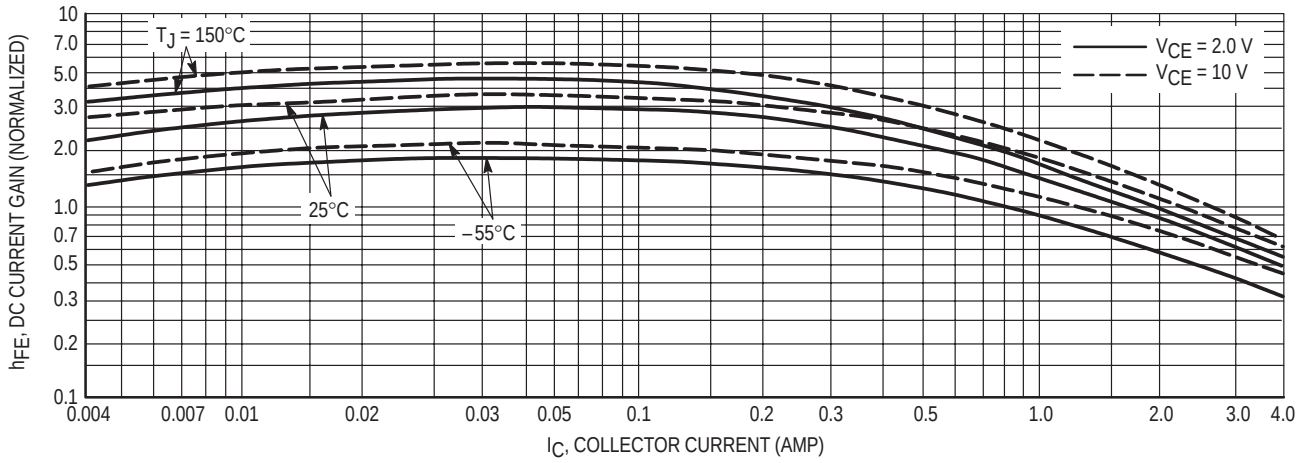


Figure 1. DC Current Gain

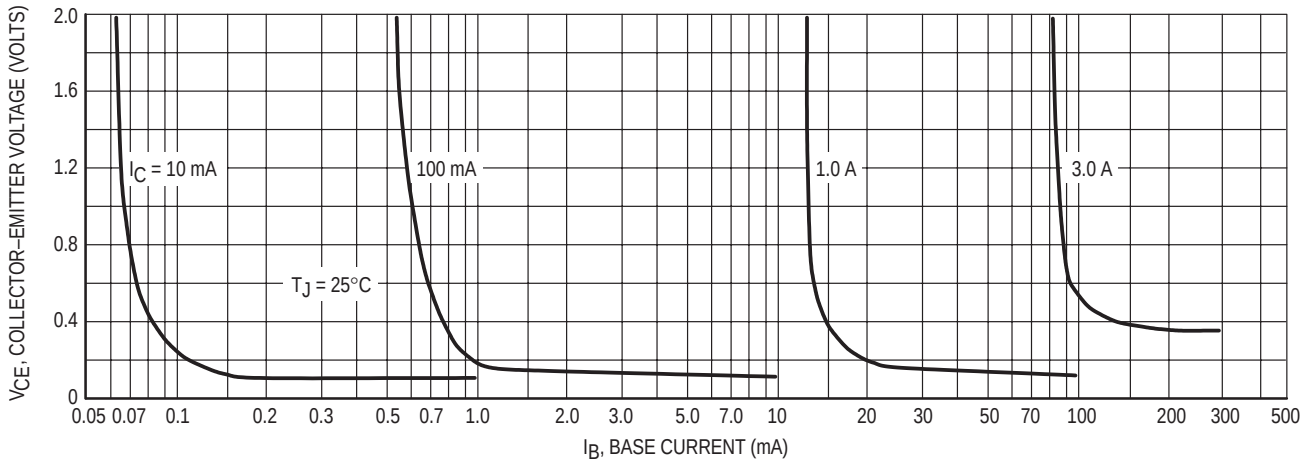


Figure 2. Collector Saturation Region

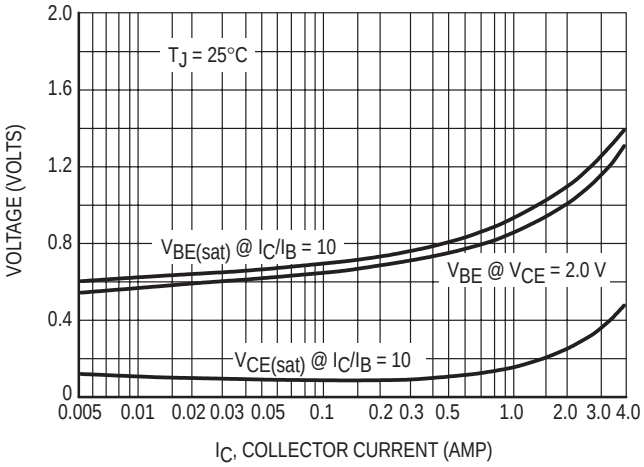


Figure 3. "On" Voltage

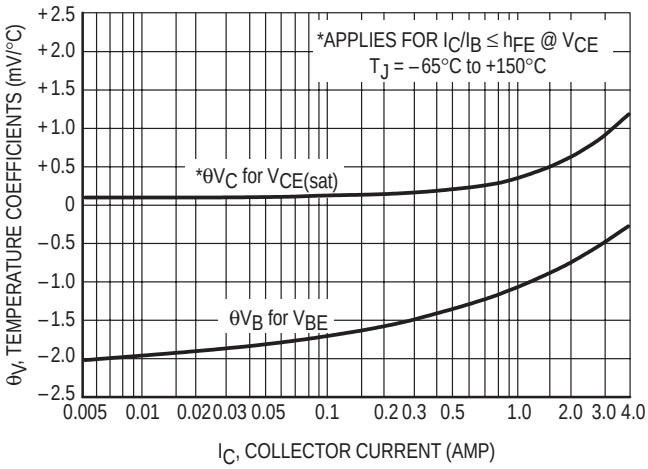


Figure 4. Temperature Coefficients

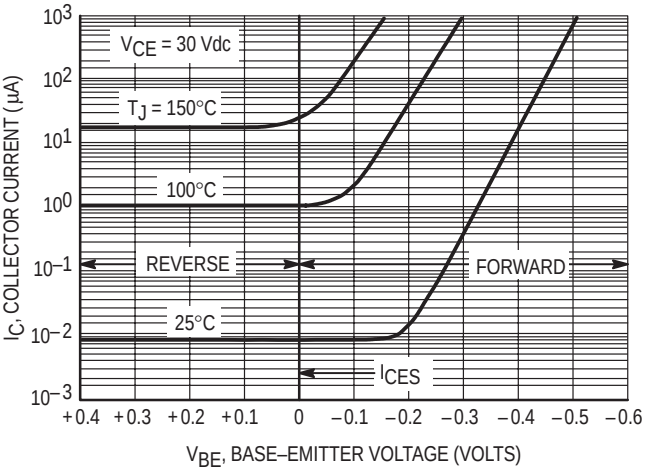


Figure 5. Collector Cut–Off Region

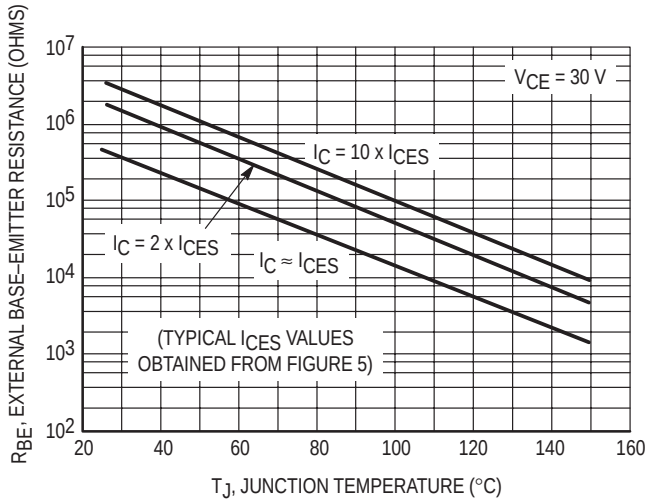


Figure 6. Effects of Base–Emitter Resistance

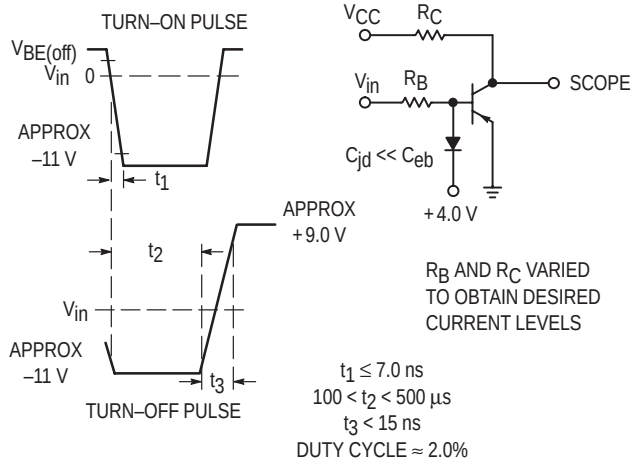


Figure 7. Switching Time Equivalent Test Circuit

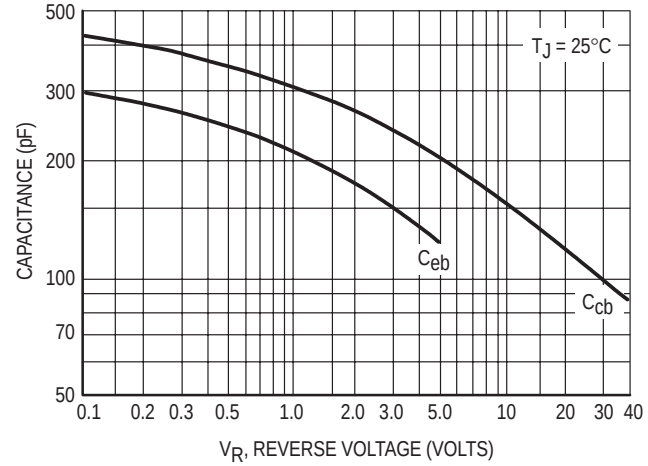


Figure 8. Capacitance

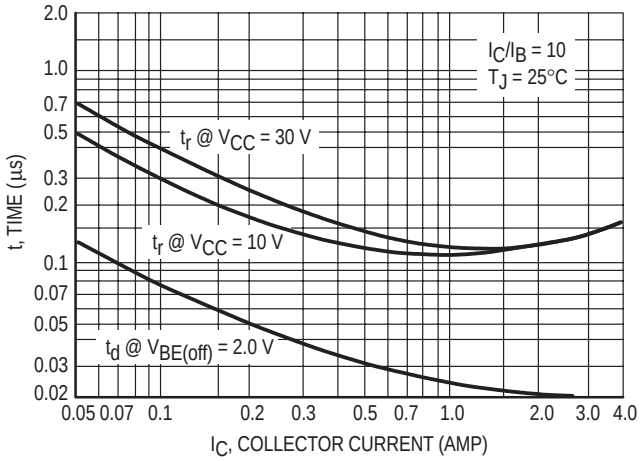


Figure 9. Turn–On Time

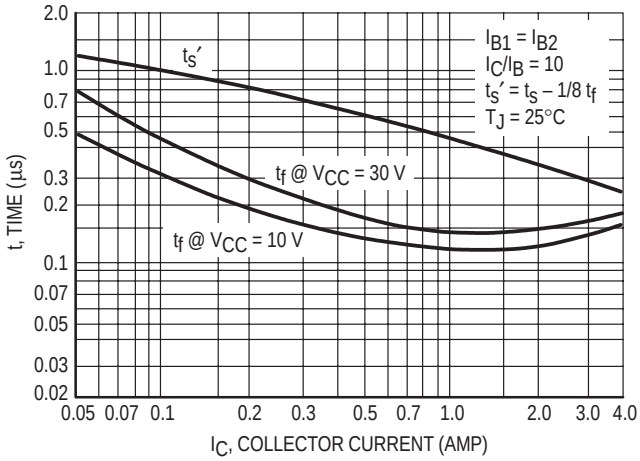


Figure 10. Turn–Off Time

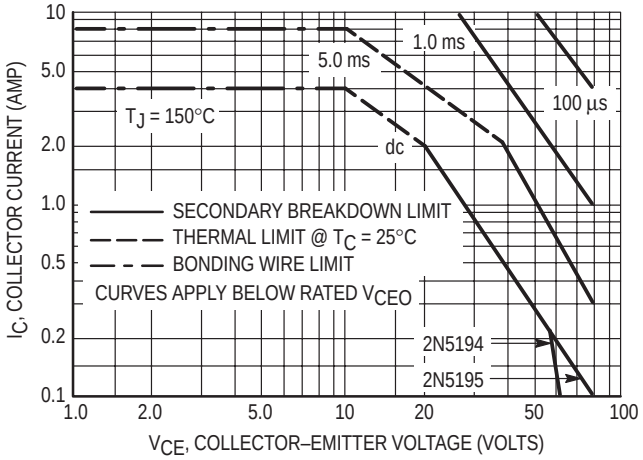


Figure 11. Rating and Thermal Data
Active–Region Safe Operating Area

Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_{J(pk)}$ = 150°C. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high–case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

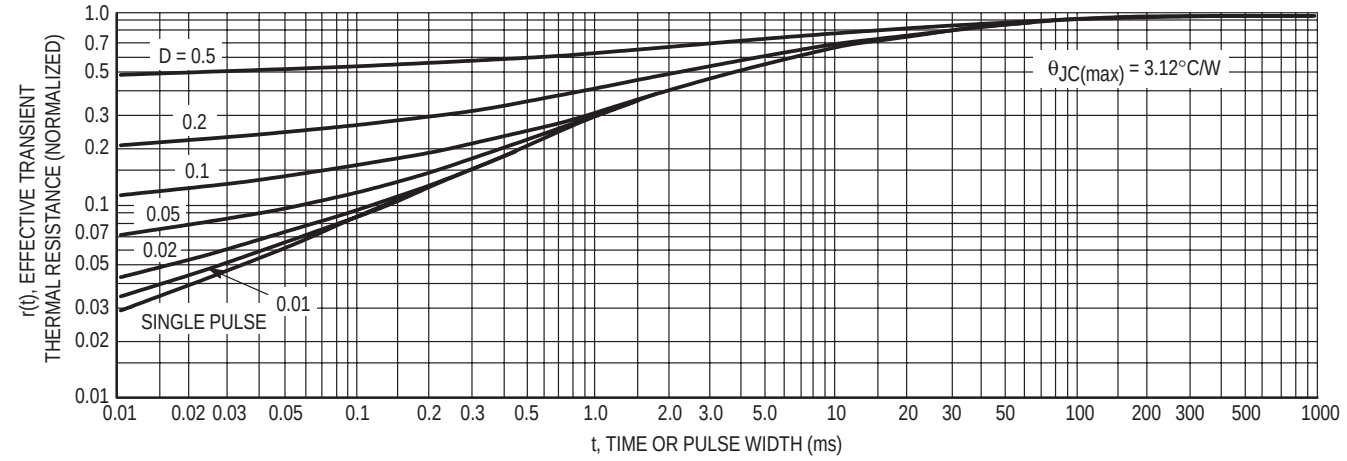
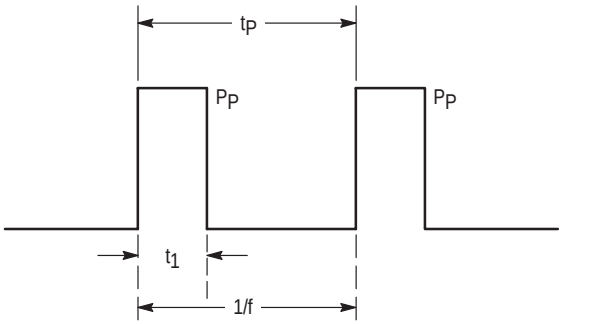


Figure 12. Thermal Response

DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA



DUTY CYCLE, D = $t_1 f = \frac{t_1}{t_P}$

PEAK PULSE POWER = P_P

Figure A

A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find $\theta_{JC}(t)$, multiply the value obtained from Figure 12 by the steady state value θ_{JC}.

Example:
The 2N5193 is dissipating 50 watts under the following conditions: t_1 = 0.1 ms, t_p = 0.5 ms. (D = 0.2).

Using Figure 12, at a pulse width of 0.1 ms and D = 0.2, the reading of $r(t_1, D)$ is 0.27.

The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_P \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ C$$

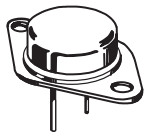
2N5301
2N5302
2N5303

High-Power NPN Silicon Transistors

20 AND 30 AMPERE
POWER TRANSISTORS
NPN SILICON
40–60–80 VOLTS
200 WATTS

. . . for use in power amplifier and switching circuits applications.

- High Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 80 Vdc (Min) @ I_C = 200 mAdc (2N5303)
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.75 Vdc (Max) @ I_C = 10 Adc (2N5301, 2N5302)
  1.0 Vdc (Max) @ I_C = 10 Adc (2N5303)
- Excellent Safe Operating Area —
  200 Watt dc Power Rating to 30 Vdc (2N5303)
- Complements to PNP 2N4398, 2N4399 and 2N5745



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	2N5301	2N5302	2N5303	Unit
Collector–Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector–Base Voltage	V_{CB}	40	60	80	Vdc
Collector Current — Continuous	I_C	30	30	20	Adc
Base Current	I_B	7.5			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W
Thermal Resistance, Case to Ambient	θ_{CA}	34	°C/W

* Indicates JEDEC Registered Data.

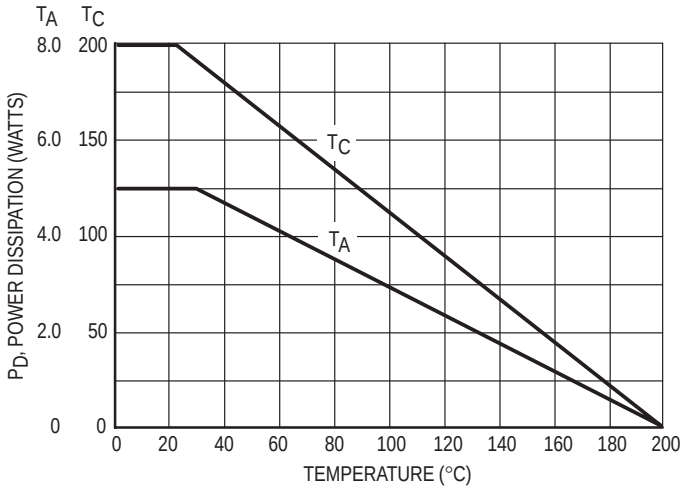


Figure 1. Power Temperature Derating Curve

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**					
Collector–Emitter Sustaining Voltage (Note 1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N5301		40	—	
	2N5302		60	—	
	2N5303		80	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N5301		—	5.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N5302		—	5.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N5303		—	5.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5301		—	1.0	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5302		—	1.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5303		—	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5301		—	10	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5302		—	10	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5303		—	10	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N5301		—	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5302		—	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5303		—	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 1)		h_{FE}			—
*(I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	ALL TYPES		40	—	
*(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5303		15	60	
*(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N5301, 2N5302		15	60	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N5303		5.0	—	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N5301, 2N5302		5.0	—	
*Collector–Emitter Saturation Voltage (Note 1)		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)	2N5301, 2N5302		—	0.75	
(I_C = 10 Adc, I_B = 1.0 Adc)	2N5303		—	1.0	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N5303		—	1.5	
(I_C = 20 Adc, I_B = 2.0 Adc)	2N5301, 2N5302		—	2.0	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5303		—	2.0	
(I_C = 30 Adc, I_B = 6.0 Adc)	2N5301, 2N5302		—	3.0	
*Base Emitter Saturation Voltage (Note 1)		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)	ALL TYPES		—	1.7	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N5301, 2N5302		—	1.8	
(I_C = 15 Adc, I_B = 1.5 Adc)	2N5303		—	2.0	
(I_C = 20 Adc, I_B = 2.0 Adc)	2N5301, 2N5302		—	2.5	
(I_C = 20 Adc, I_B = 4.0 Adc)	2N5303		—	2.5	
*Base–Emitter On Voltage (Note 1)		$V_{BE(on)}$			Vdc
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)	2N5303		—	1.5	
(I_C = 15 Adc, V_{CE} = 2.0 Vdc)	2N5301, 2N5302		—	1.7	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)	2N5303		—	25	
(I_C = 30 Adc, V_{CE} = 4.0 Vdc)	2N5301, 2N5302		—	3.0	
***DYNAMIC CHARACTERISTICS**					
Current–Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	2.0	—	MHz
Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	40	—	—
***SWITCHING CHARACTERISTICS**					
Rise Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_r	—	1.0	μs
Storage Time		t_s	—	2.0	μs
Fall Time		t_f	—	1.0	μs

* Indicates JEDEC Registered Data.

Note 1: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

SWITCHING TIME EQUIVALENT TEST CIRCUITS

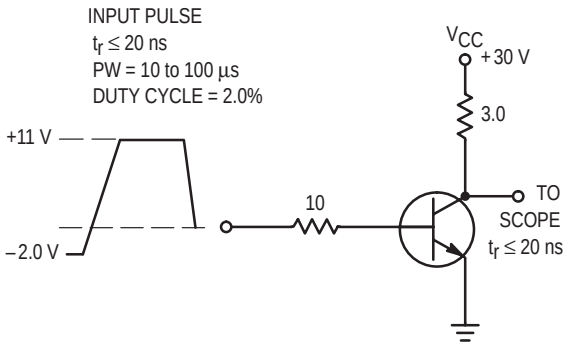


Figure 2. Turn–On time

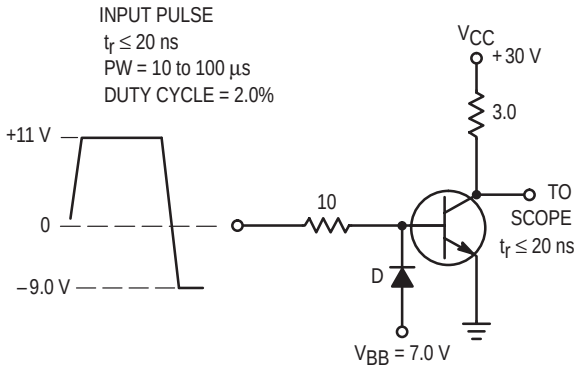


Figure 3. Turn–Off time

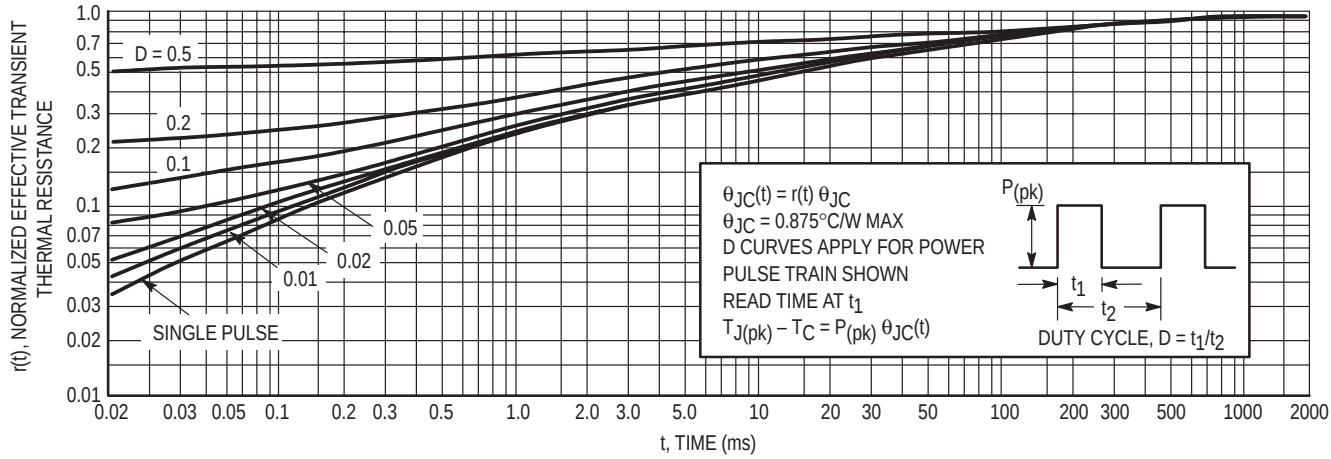


Figure 4. Thermal Response

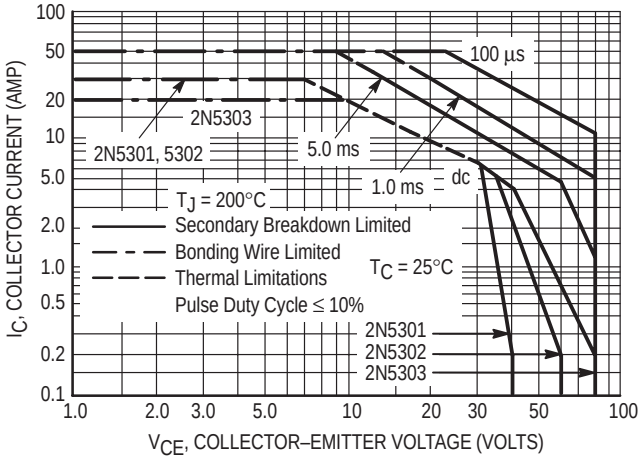


Figure 5. Active–Region Safe Operating Area

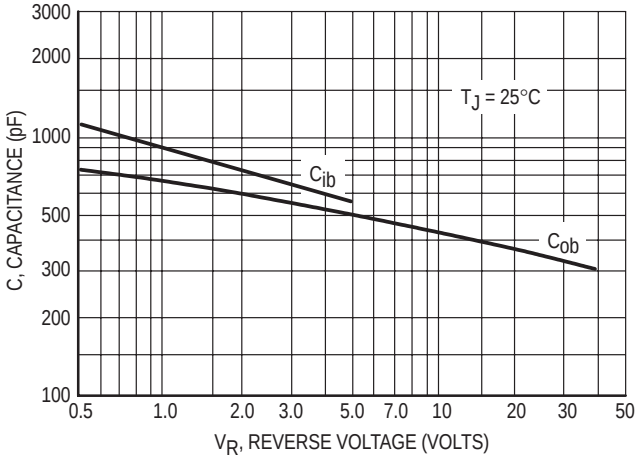


Figure 6. Capacitance versus Voltage

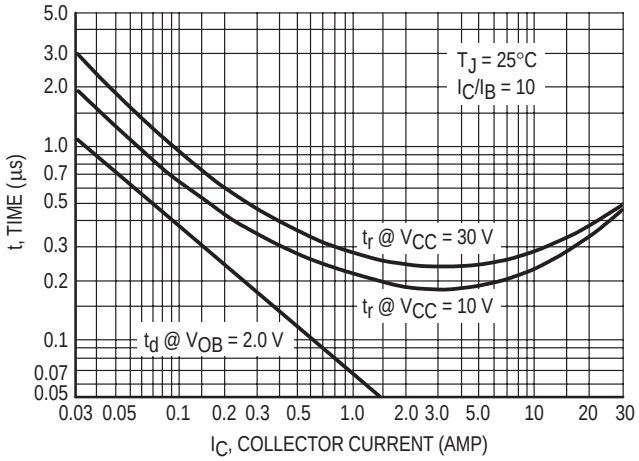


Figure 7. Turn–On Time

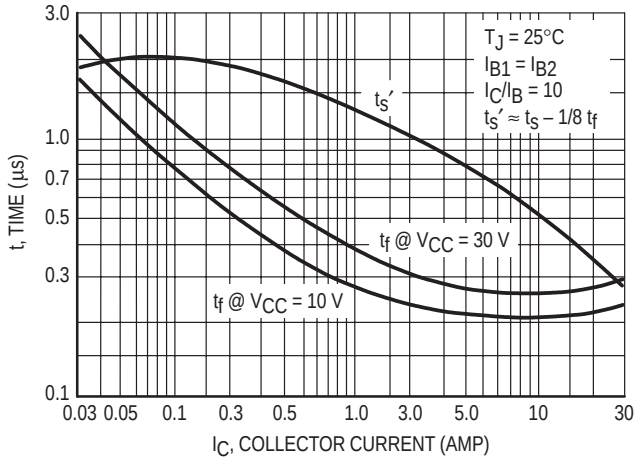


Figure 8. Turn–Off Time

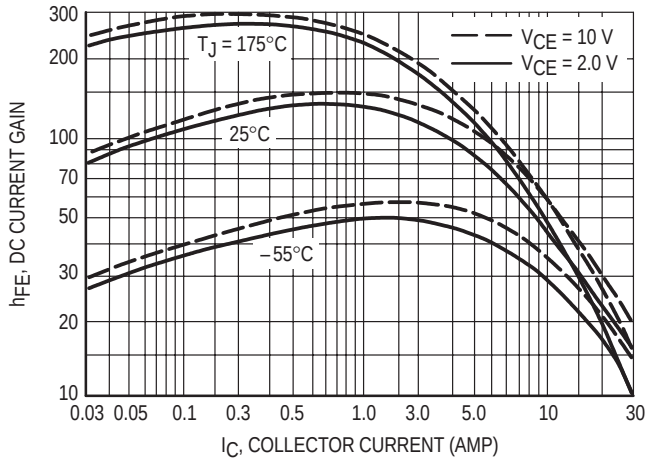


Figure 9. DC Current Gain

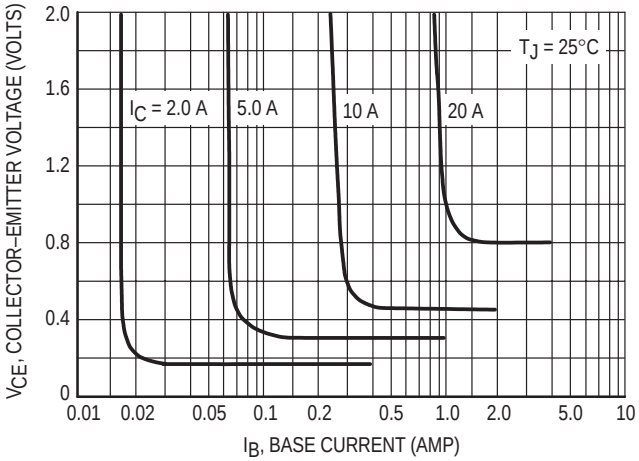


Figure 10. Collector Saturation Region

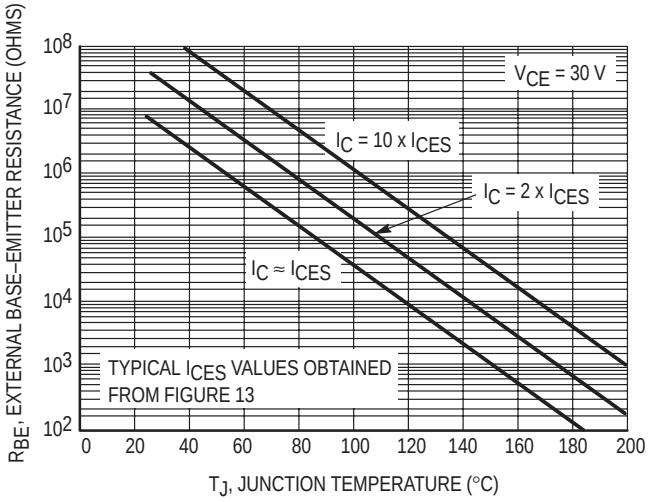


Figure 11. Effects of Base–Emitter Resistance

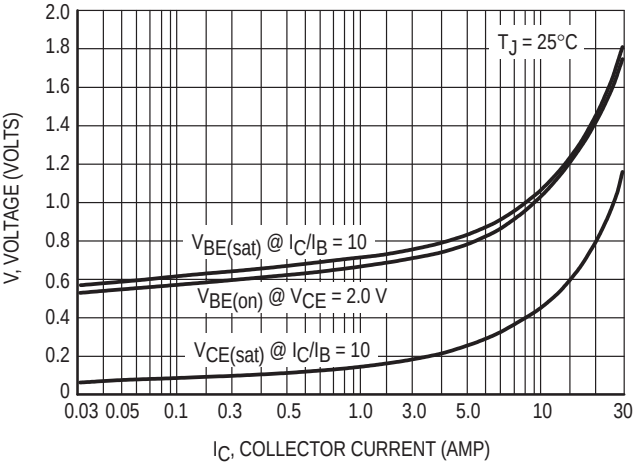


Figure 12. “On” Voltages

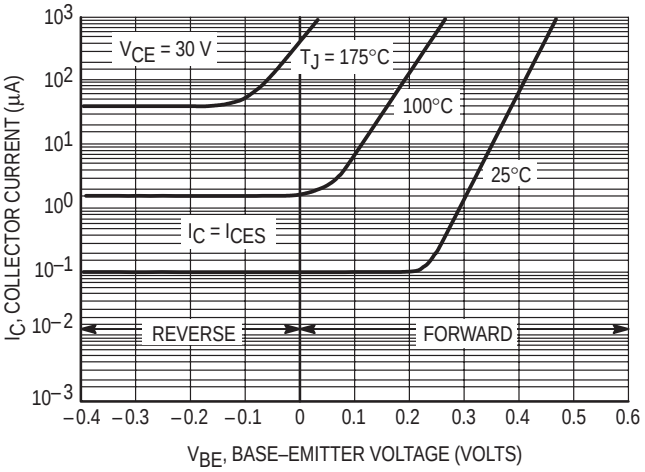


Figure 13. Collector Cut–Off Region

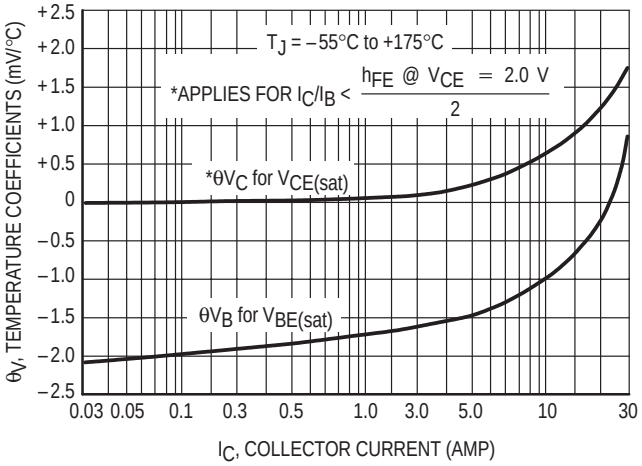


Figure 14. Temperature Coefficients

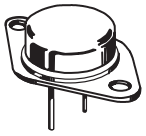
High-Voltage — High Power Transistors

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 120 Vdc — 2N5630, 2N6030
  = 140 Vdc — 2N5631, 2N6031
- High DC Current Gain — @ I_C = 8.0 Adc
  h_{FE} = 20 (Min) — 2N5630, 2N6030
  = 15 (Min) — 2N5631, 2N6031
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc

NPN
2N5630
2N5631
PNP
2N6030
2N6031

16 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
100 –120 –140 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (1)

Rating	Symbol	2N5630 2N6030	2N5631 2N6031	Unit
Collector–Emitter Voltage	V_{CEO}	120	140	Vdc
Collector–Base Voltage	V_{CB}	120	140	Vdc
Emitter–Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak	I_C	16 20		Adc
Base Current — Continuous	I_B	5.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS (1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

(1) Indicates JEDEC Registered Data.

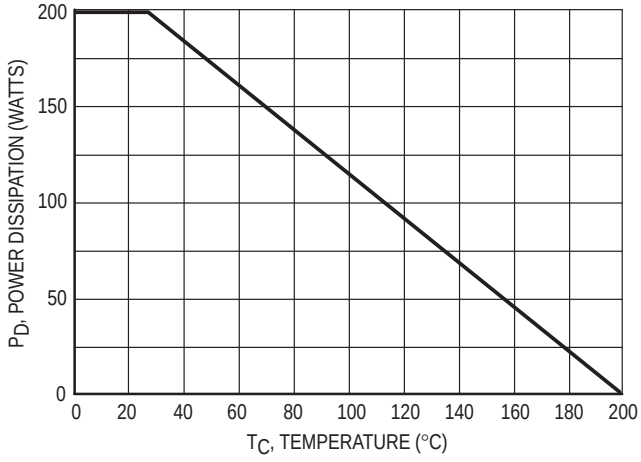


Figure 1. Power Derating

Safe Area Curves are indicated by Figure 5. All Limits are applicable and must be observed.

REV 7

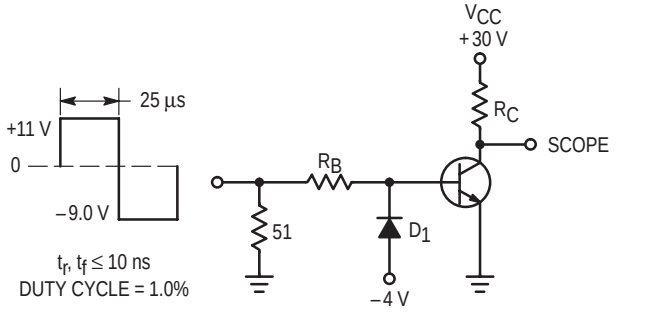
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N5630, 2N6030 2N5631, 2N6031	$V_{CEO(sus)}$	 120 140	 —	Vdc
Collector–Emitter Cutoff Current (V_{CE} = 50 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 70 Vdc, I_B = 0)	 2N5630, 2N6030 2N5631, 2N6031	I_{CEO}	 — —	 2.0 2.0	mAdc
Collector–Emitter Cutoff Current (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	 — —	 2.0 7.0	mAdc
Collector–Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	2.0	mAdc
Emitter–Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 16 Adc, V_{CE} = 2.0 Vdc)	 2N5630, 2N6030 2N5631, 2N6031 All Types	h_{FE}	 20 15 4.0	 80 60 —	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 16 Adc, I_B = 4.0 Adc)	 All Types	$V_{CE(sat)}$	 — —	 1.0 2.0	Vdc
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	—	1.8	Vdc
Base–Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N5630, 31 2N6030, 31	C_{ob}	— —	500 1000	pF
Small–Signal Current Gain (I_C = 4.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	15	—	—

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≥ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

For PNP test circuit, reverse all polarities and D1.

Figure 2. Switching Times Test Circuit

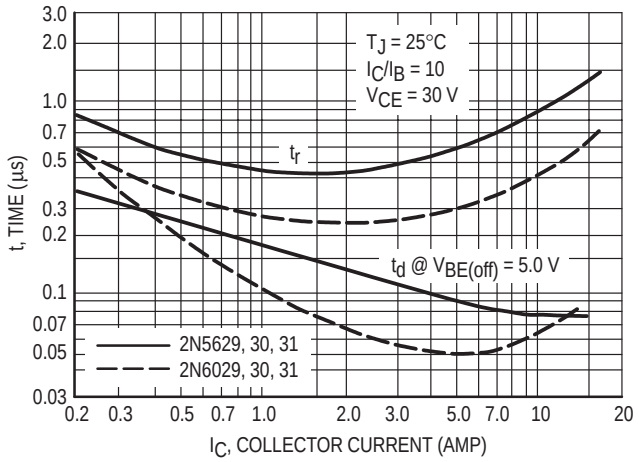


Figure 3. Turn–On Time

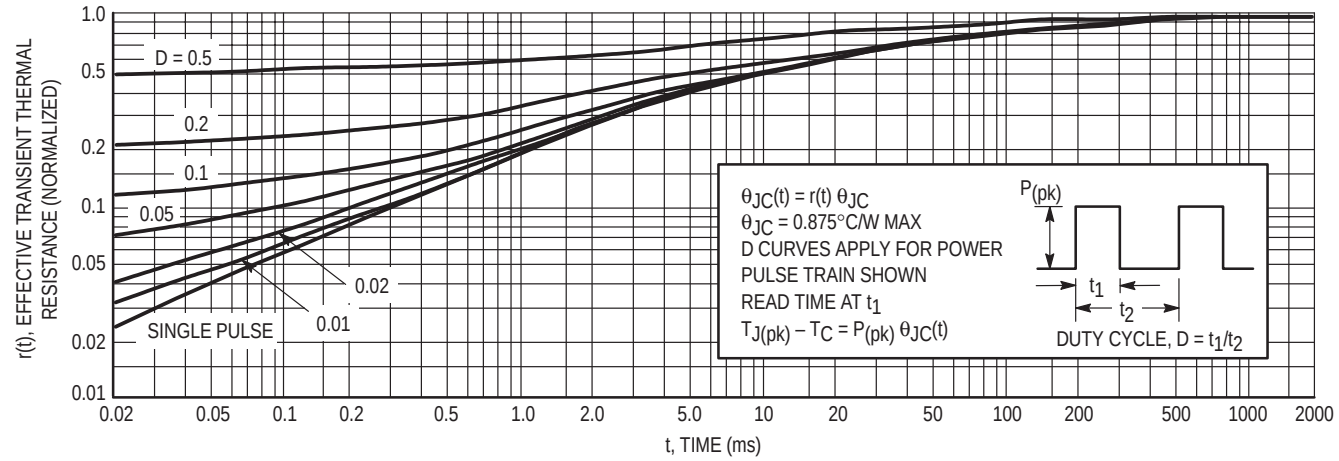


Figure 4. Thermal Response

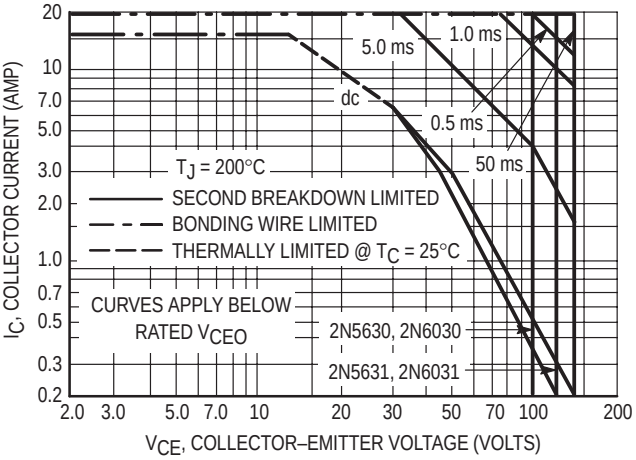
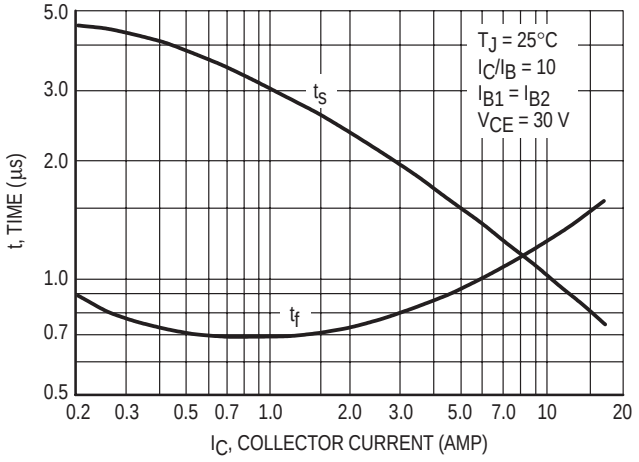


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN
2N5630, 2N5631



PNP
2N6030, 2N6031

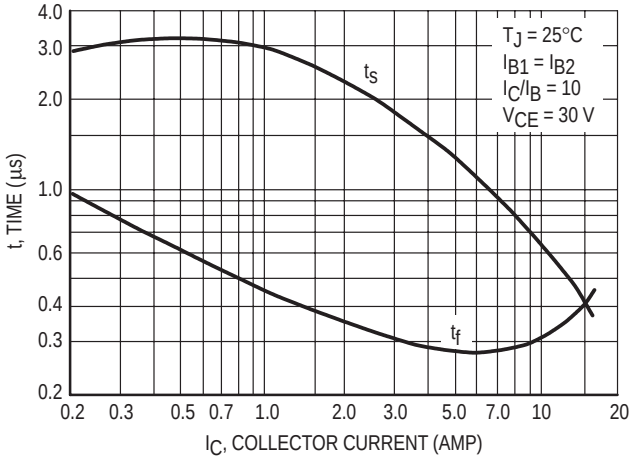
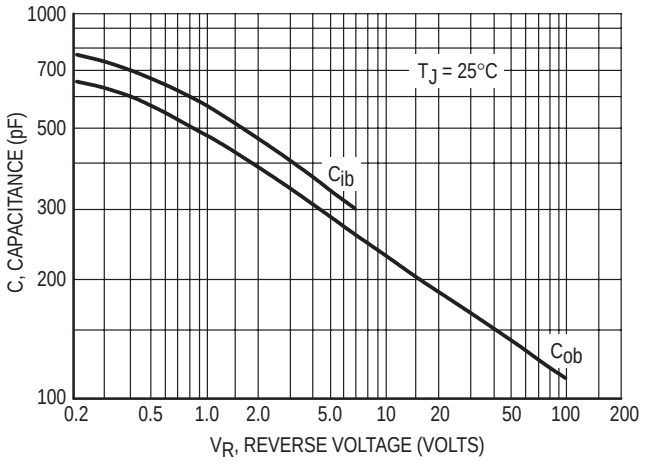


Figure 6. Turn–Off Time

NPN
2N5630, 2N5631



NPN
2N5630, 2N5631

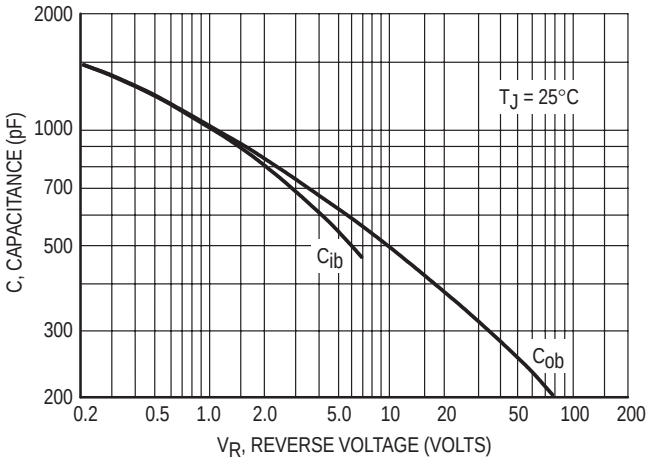
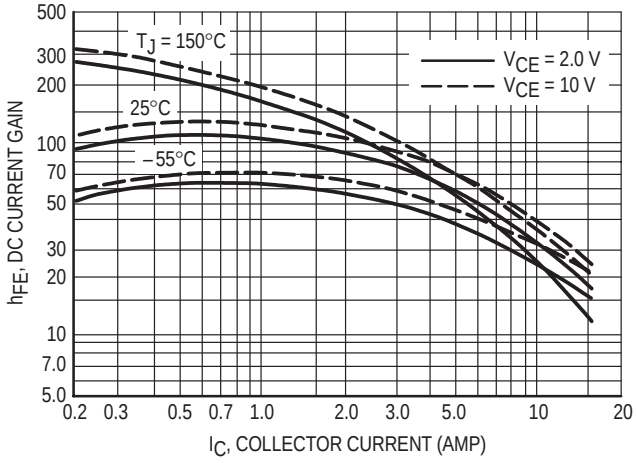


Figure 7. Capacitance



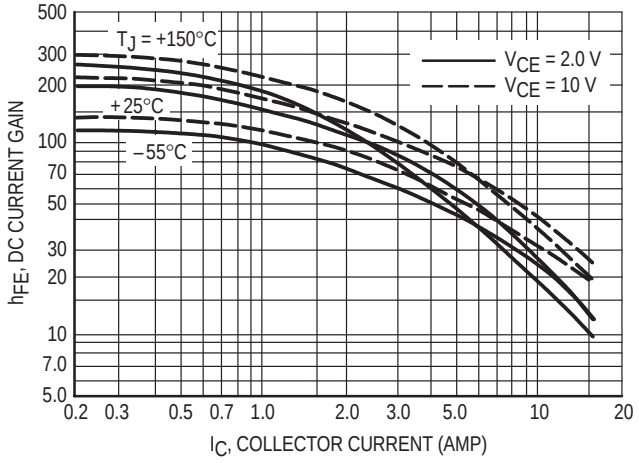
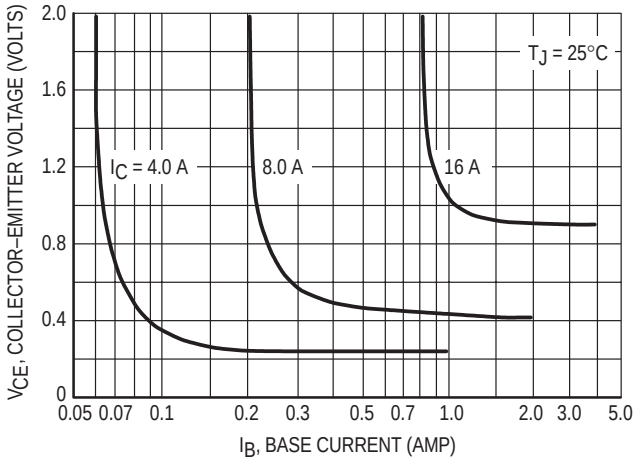


Figure 8. DC Current Gain



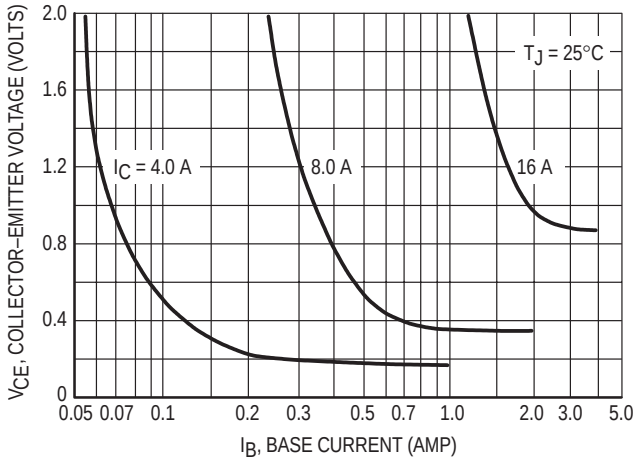


Figure 9. Collector Saturation Region

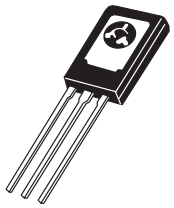
2N5655
2N5656
2N5657

Plastic NPN Silicon High-Voltage Power Transistor

. . . designed for use in line–operated equipment such as audio output amplifiers; low–current, high–voltage converters; and AC line relays.

- Excellent DC Current Gain — h_{FE} = 30–250 @ I_C = 100 mAdc
- Current–Gain — Bandwidth Product — f_T = 10 MHz (Min) @ I_C = 50 mAdc

0.5 AMPERE
POWER TRANSISTORS
NPN SILICON
250–300–350 VOLTS
20 WATTS



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS (1)

Rating	Symbol	2N5655	2N5656	2N5657	Unit
Collector–Emitter Voltage	V_{CEO}	250	300	350	Vdc
Collector–Base Voltage	V_{CB}	275	325	375	Vdc
Emitter–Base Voltage	V_{EB}	6.0			Vdc
Collector Current — Continuous Peak	I_C	0.5 1.0			Adc
Base Current	I_B	0.25			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

(1) Indicates JEDEC Registered Data.

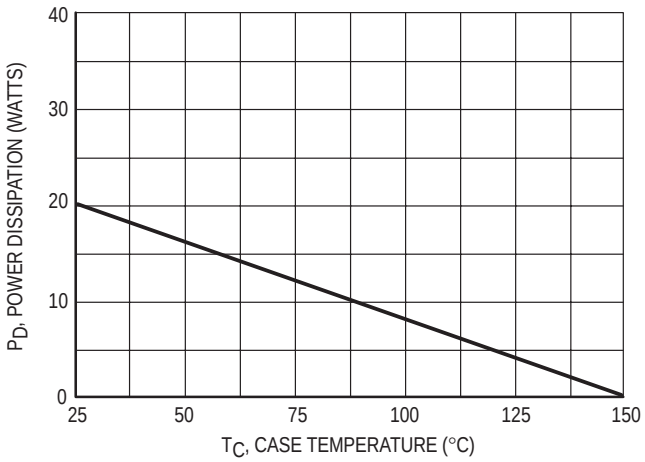


Figure 1. Power Derating

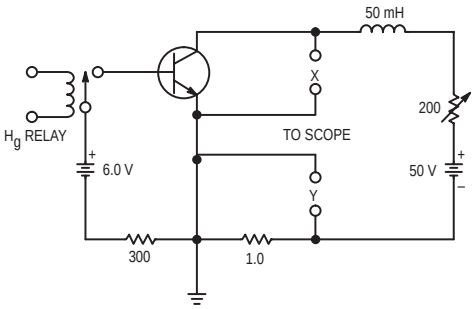


Figure 2. Sustaining Voltage Test Circuit

Safe Area Limits are indicated by Figures 3 and 4. Both limits are applicable and must be observed.

REV 3

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc (inductive), L = 50 mH)	2N5655	$V_{CEO(sus)}$	250	—	Vdc
	2N5656		300	—	
	2N5657		350	—	
Collector–Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	2N5655	$V_{(BR)CEO}$	250	—	Vdc
	2N5656		300	—	
	2N5657		350	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 150 Vdc, I_B = 0)	2N5655		—	0.1	
(V_{CE} = 200 Vdc, I_B = 0)	2N5656		—	0.1	
(V_{CE} = 250 Vdc, I_B = 0)	2N5657		—	0.1	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5655		—	0.1	
(V_{CE} = 300 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5656		—	0.1	
(V_{CE} = 350 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5657		—	0.1	
(V_{CE} = 150 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5655		—	1.0	
(V_{CE} = 200 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5656		—	1.0	
(V_{CE} = 250 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 100°C)	2N5657		—	1.0	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 275 Vdc, I_E = 0)	2N5655		—	10	
(V_{CB} = 325 Vdc, I_E = 0)	2N5656		—	10	
(V_{CB} = 375 Vdc, I_E = 0)	2N5657		—	10	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	10	μAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			—
(I_C = 50 mAdc, V_{CE} = 10 Vdc)			25	—	
(I_C = 100 mAdc, V_{CE} = 10 Vdc)			30	250	
(I_C = 250 mAdc, V_{CE} = 10 Vdc)			15	—	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)			5.0	—	
Collector–Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 100 mAdc, I_B = 10 mAdc)			—	1.0	
(I_C = 250 mAdc, I_B = 25 mAdc)			—	2.5	
(I_C = 500 mAdc, I_B = 100 mAdc)			—	10	
Base–Emitter Voltage (1) (I_C = 100 mAdc, V_{CE} = 10 Vdc)		V_{BE}	—	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	10	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	25	pF
Small–Signal Current Gain (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	—	—

* Indicates JEDEC Registered Data for 2N5655 Series.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

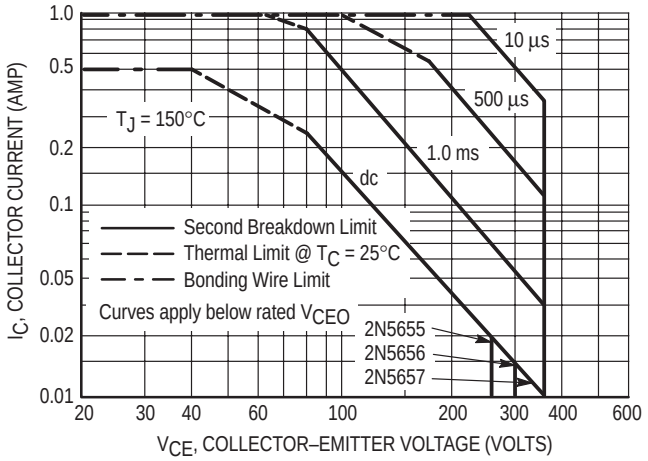


Figure 3. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

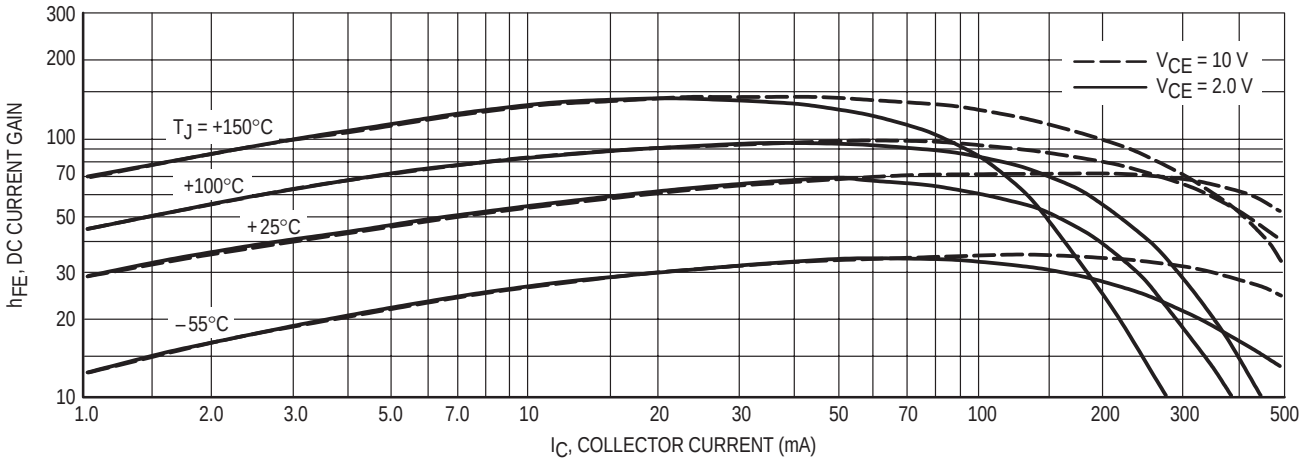


Figure 4. Current Gain

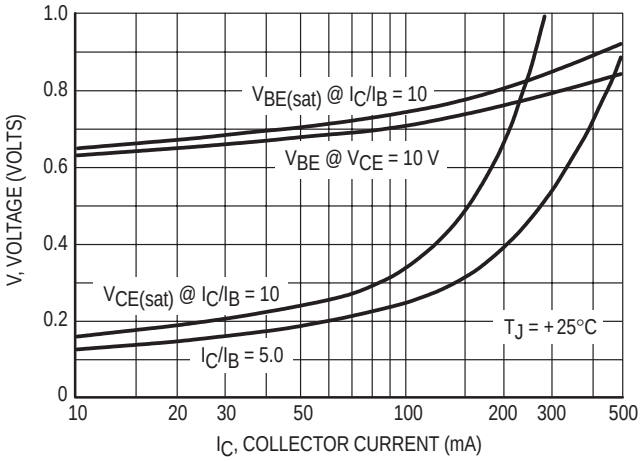


Figure 5. “On” Voltages

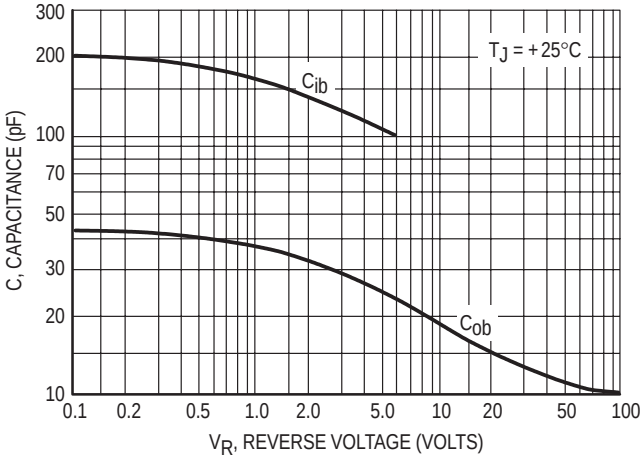


Figure 6. Capacitance

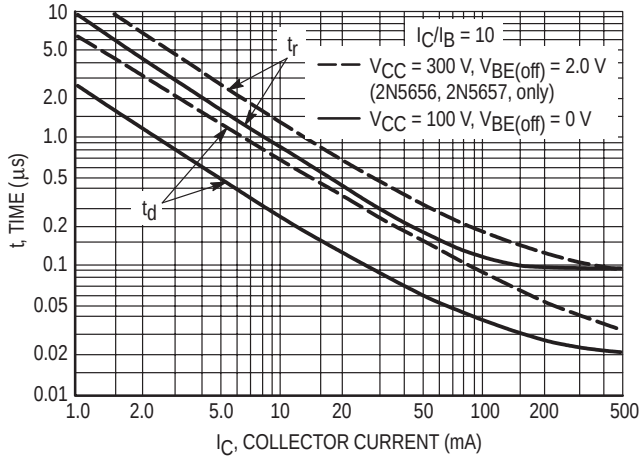


Figure 7. Turn–On Time

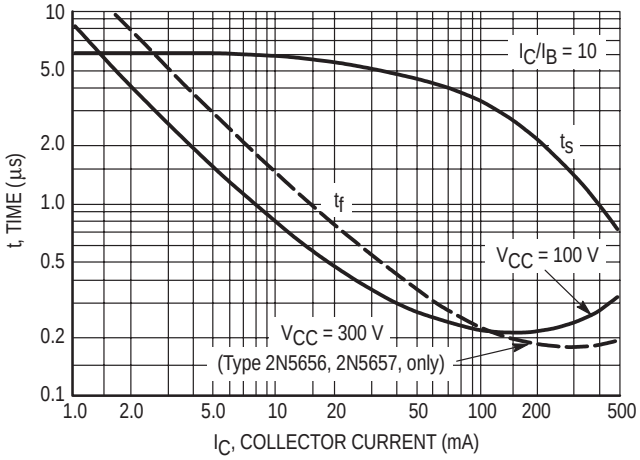


Figure 8. Turn–Off Time

High-Current Complementary Silicon Power Transistors

. . . designed for use in high–power amplifier and switching circuit applications.

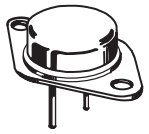
- High Current Capability — I_C Continuous = 50 Amperes.
- DC Current Gain —
  h_{FE} = 15–60 @ I_C = 25 Adc
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 25 Adc

PNP
2N5684
NPN
2N5685

2N5686*

***Motorola Preferred Device**

50 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60–80 VOLTS
300 WATTS



CASE 197A–05
TO–204AE

MAXIMUM RATINGS (1)

Rating	Symbol	2N5685	2N5684 2N5686	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	50		Adc
Base Current	I_B	15		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 1.715		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS (1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.584	°C/W

(1) Indicates JEDEC Registered Data.

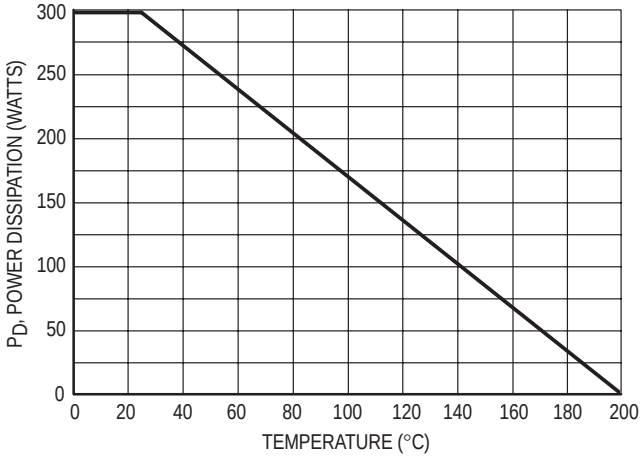


Figure 1. Power Derating

Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

Preferred devices are Motorola recommended choices for future use and best overall value.

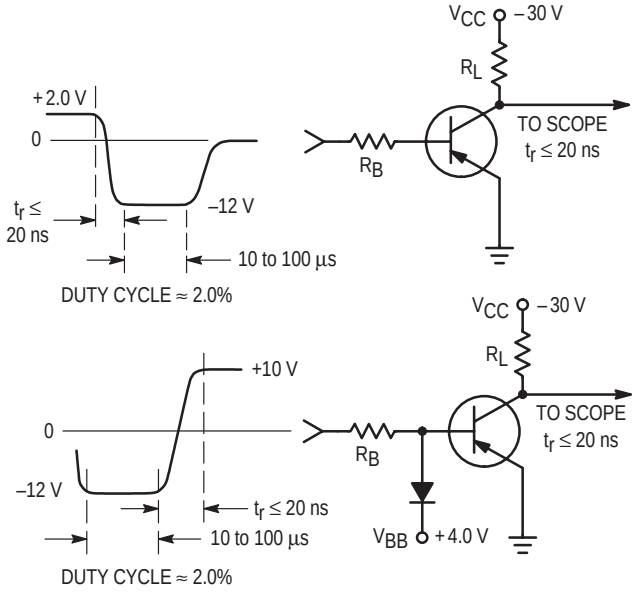
REV 7

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Note 1)	2N5685	$V_{CEO(sus)}$	60	—	Vdc
(I_C = 0.2 Adc, I_B = 0)	2N5684, 2N5686		80	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N5685		—	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5684, 2N5686		—	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5685		—	2.0	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N5684, 2N5686		—	2.0	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5685		—	10	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5684, 2N5686		—	10	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5685		—	2.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5684, 2N5686		—	2.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 1)		h_{FE}			—
(I_C = 25 Adc, V_{CE} = 2.0 Vdc)			15	60	
(I_C = 50 Adc, V_{CE} = 5.0 Vdc)			5.0	—	
Collector–Emitter Saturation Voltage (Note 1)		$V_{CE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.5 Adc)			—	1.0	
(I_C = 50 Adc, I_B = 10 Adc)			—	5.0	
Base–Emitter Saturation Voltage (Note 1) (I_C = 25 Adc, I_B = 2.5 Adc)		$V_{BE(sat)}$	—	2.0	Vdc
Base–Emitter On Voltage (Note 1) (I_C = 25 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 5.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	2.0	—	MHz
Output Capacitance	2N5684	C_{ob}	—	2000	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N5685, 2N5686		—	1200	
Small–Signal Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{fe}	15	—	

* Indicates JEDEC Registered Data.

Note 1: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

Figure 2. Switching Time Test Circuit

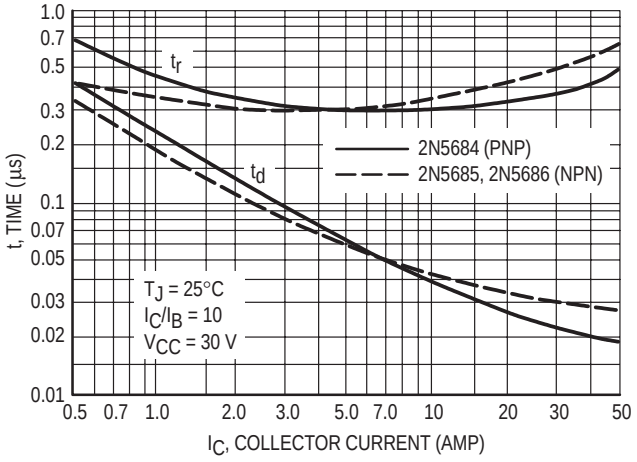


Figure 3. Turn–On Time

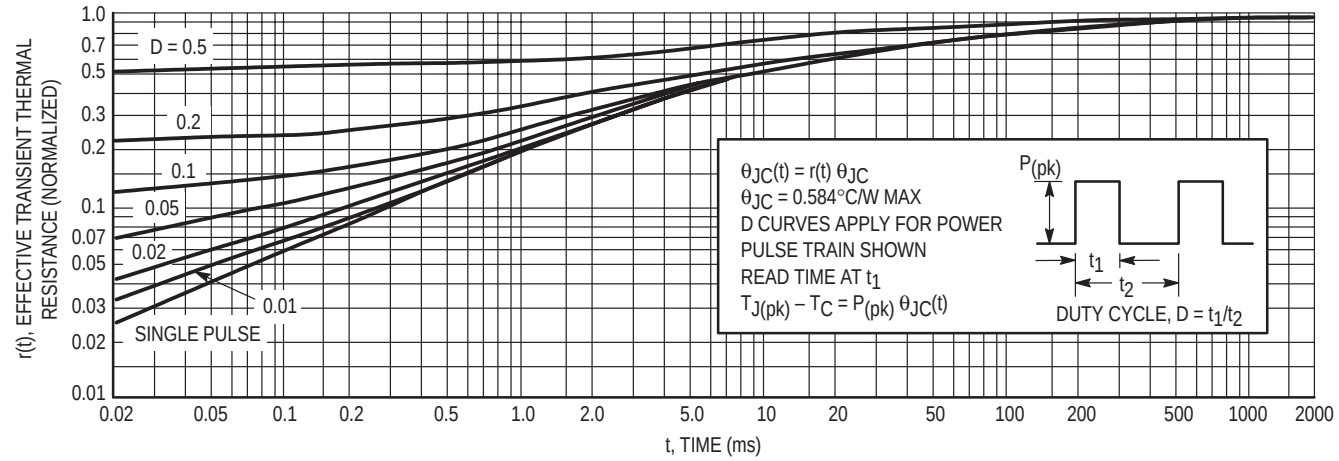


Figure 4. Thermal Response

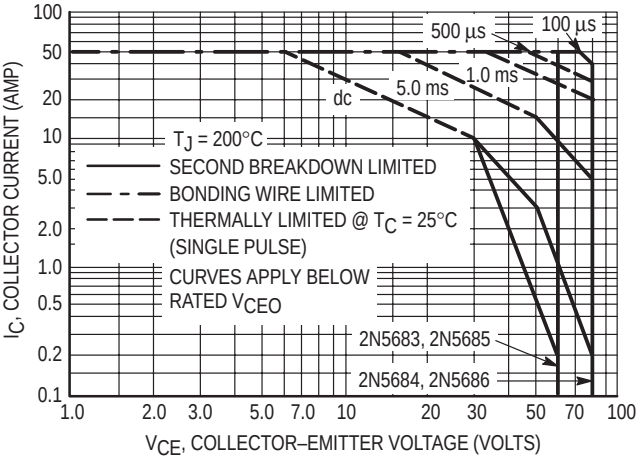


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

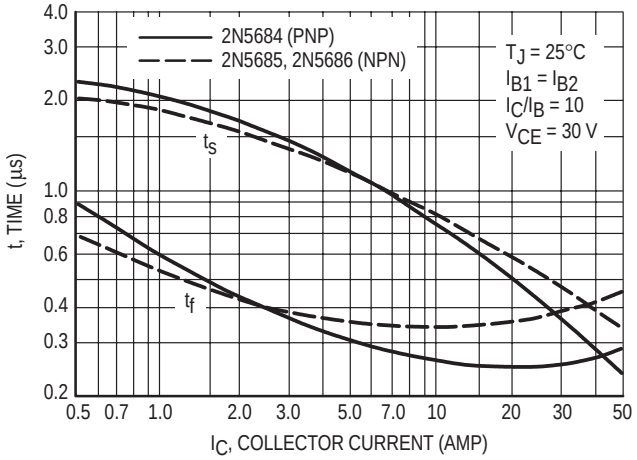


Figure 6. Turn–Off Time

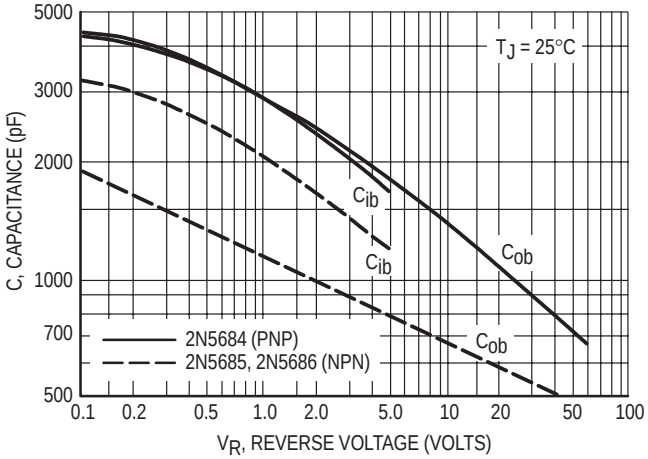
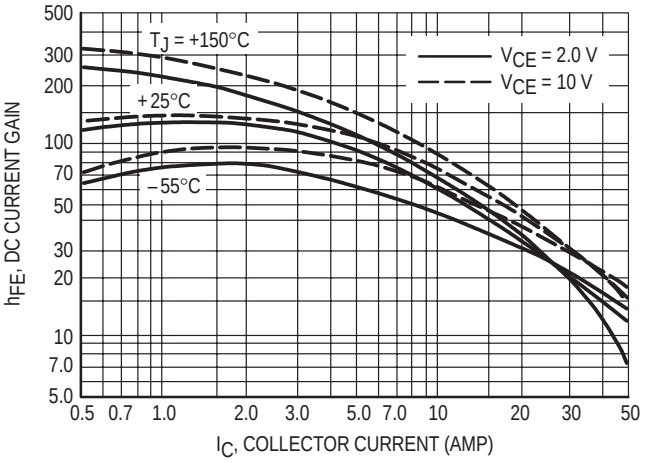


Figure 7. Capacitance

PNP
2N5684



NPN
2N5685, 2N5686

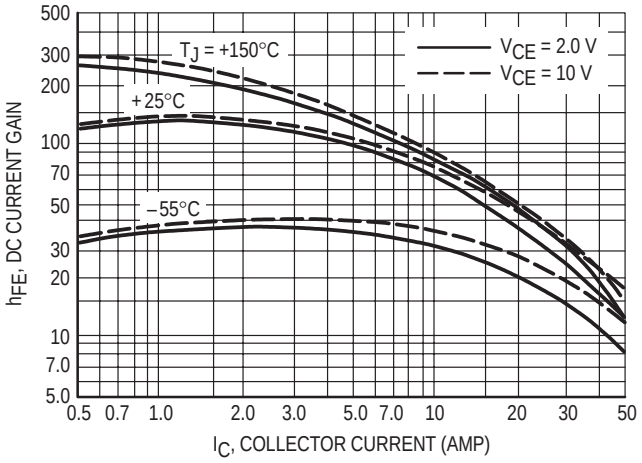
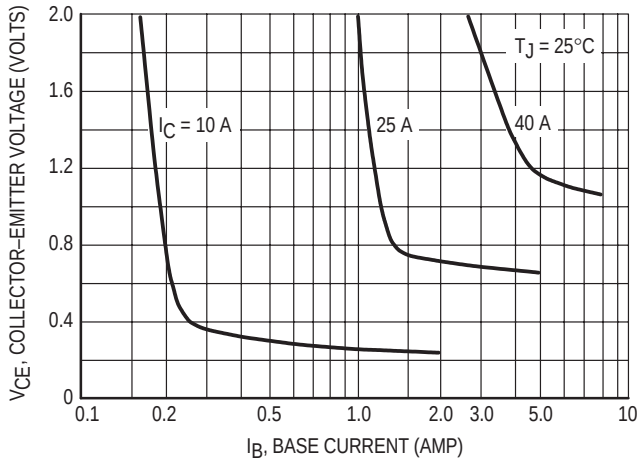


Figure 8. DC Current Gain



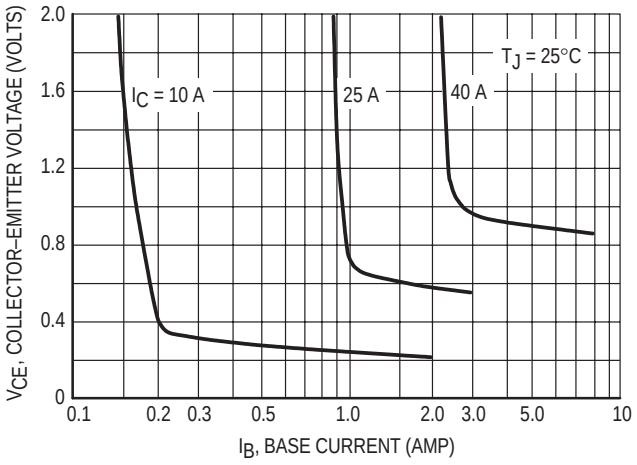
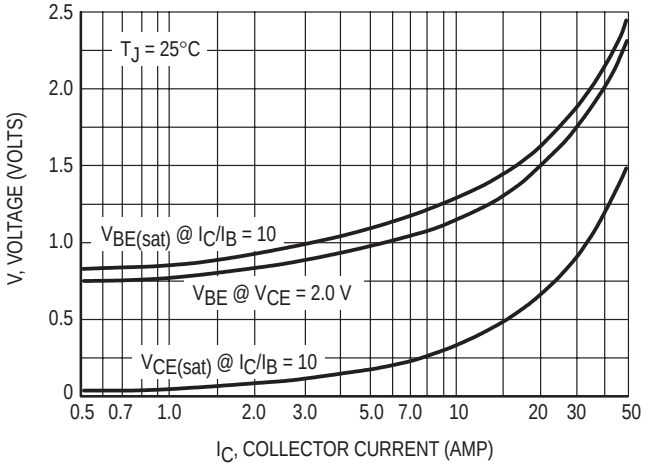


Figure 9. Collector Saturation Region



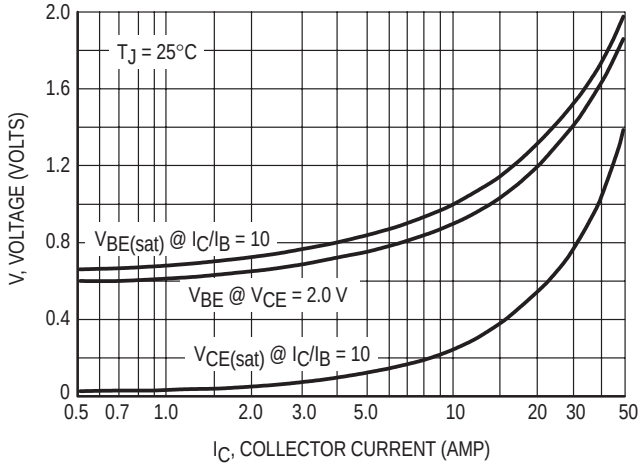


Figure 10. “On” Voltages

2N5745
(See 2N4398)

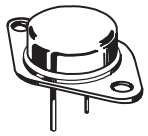
2N5758

High-Voltage High-Power Silicon Transistors

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 100 Vdc (Min)
- DC Current Gain @ I_C = 3.0 Adc —
  h_{FE} = 25 (Min)
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 3.0 Adc

6 AMPERE
POWER TRANSISTOR
NPN SILICON
100 – 140 VOLTS
150 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (1)

Rating	Symbol	2N5758	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous Peak	I_C	6.0 10	Adc
Base Current	I_B	4.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857	Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS (1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

(1) Indicates JEDEC Registered Data.

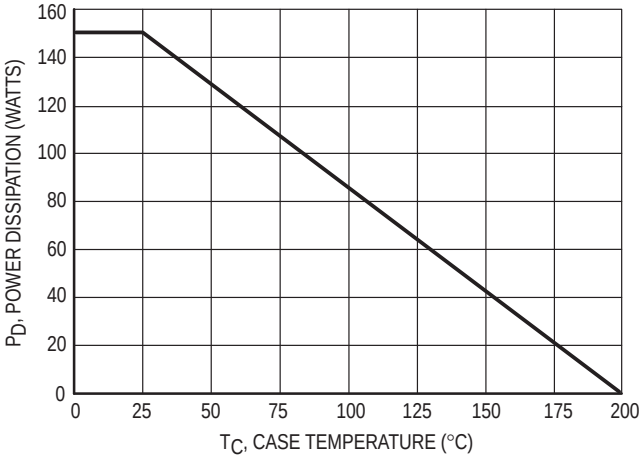


Figure 1. Power Derating

Safe area limits are indicated by Figure 5. Both limits are applicable and must be observed.

REV 7

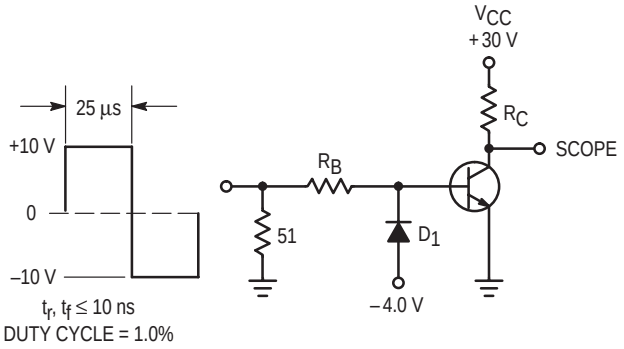
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 — —	 1.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	I_{CBO}	—	1.0	mAdc
Emitter–Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 6.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	 25 5.0	 100 —	—
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.3 Adc) (I_C = 6.0 Adc, I_B = 1.2 Adc)	$V_{CE(sat)}$	 — —	 1.0 2.0	Vdc
Base–Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)	f_T	1.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	300	pF
Small–Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	15	—	—

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

(2) $f_T = |h_{fe}| \bullet f_{test}$.



*For PNP test circuit, reverse all polarities and D1.

Figure 2. Switching Time Test Circuit

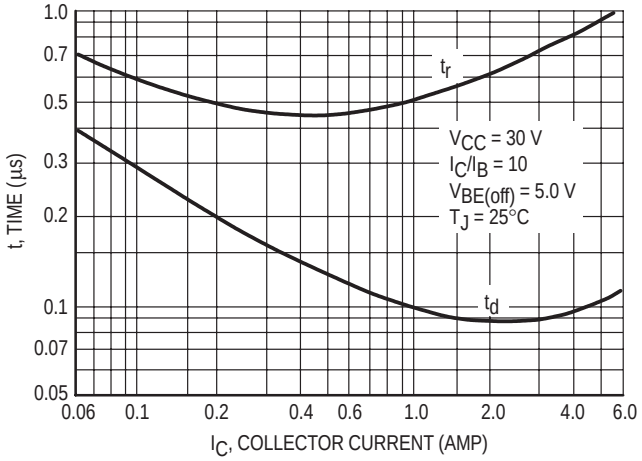


Figure 3. Turn–On Time

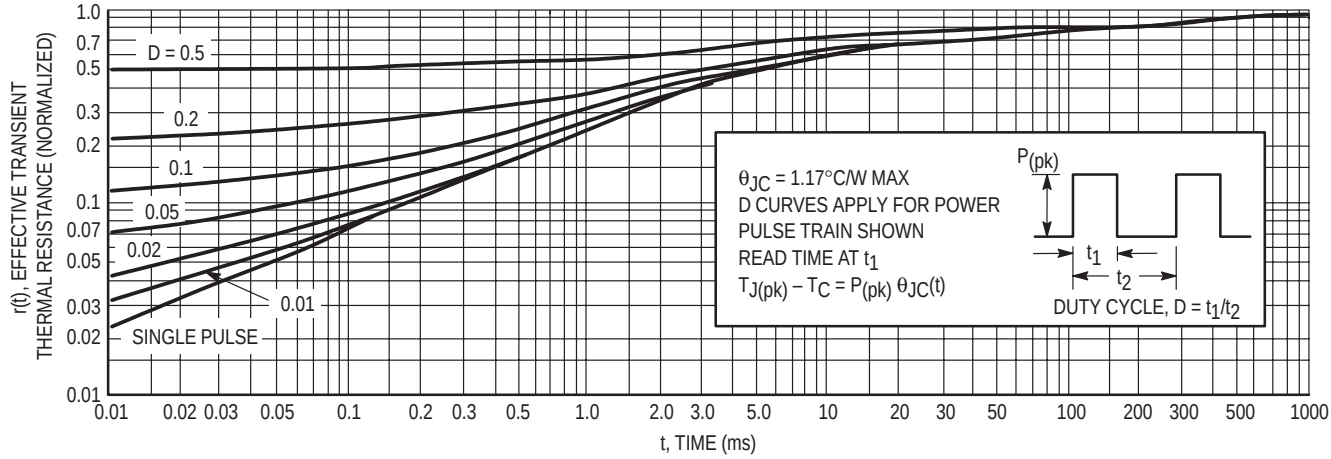


Figure 4. Thermal Response

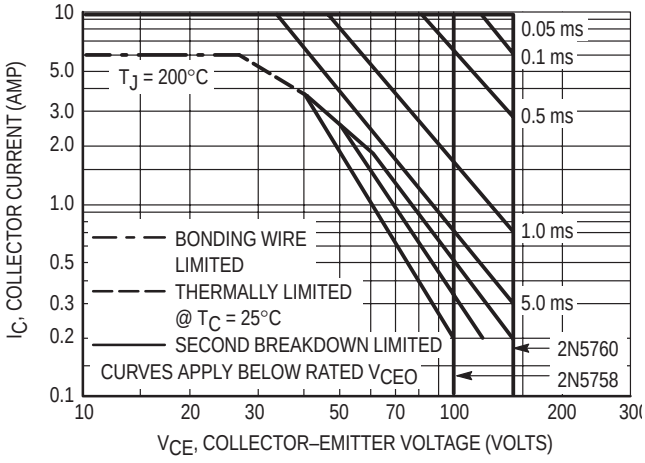


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

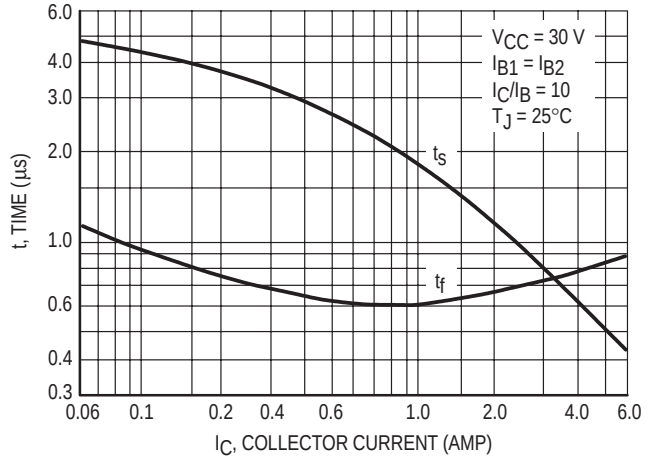


Figure 6. Turn–Off Time

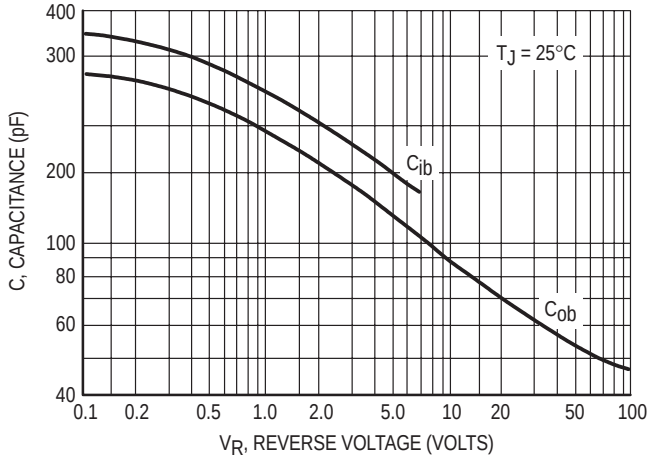


Figure 7. Capacitance

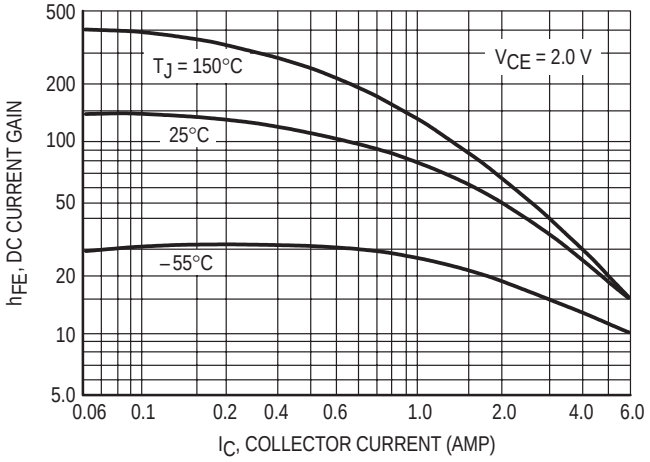


Figure 8. DC Current Gain

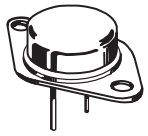
NPN
2N5877
2N5878

Complementary Silicon High-Power Transistors

. . . designed for general–purpose power amplifier and switching applications.

- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 5.0 Adc
- Low Leakage Current —
  I_{CEX} = 0.5 mAdc (Max) @ Rated Voltage
- Excellent DC Current Gain —
  h_{FE} = 20 (Min) @ I_C = 4.0 Adc
- High Current Gain — Bandwidth Product —
  f_T = 4.0 MHz (Min) @ I_C = 0.5 A

10 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60 – 80 VOLTS
150 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (1)

Rating	Symbol	2N5877	2N5878	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	10 20		Adc
Base Current	I_B	4.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

(1) Indicates JEDEC Registered Data.

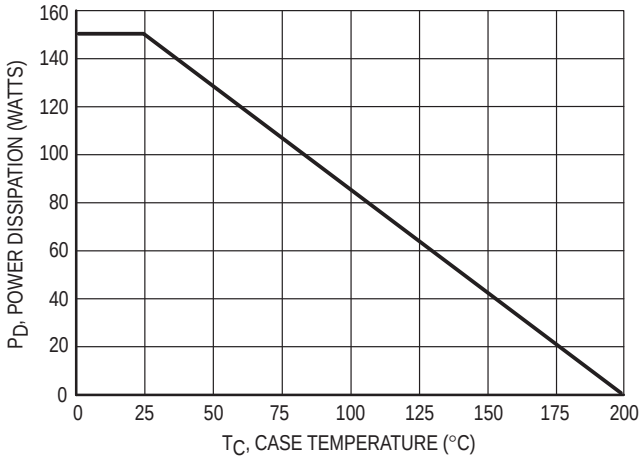


Figure 1. Power Derating

REV 7

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N5877 2N5878	$V_{CEO(sus)}$	60 80	— —	Vdc
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N5877		—	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5878		—	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5877		—	0.5	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5878		—	0.5	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5877		—	5.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5878		—	5.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5877		—	0.5	
(V_{CB} = 80 Vdc, I_E = 0)	2N5878		—	0.5	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_E = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			—
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			35	—	
(I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)			20	100	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)			4.0	—	
Collector–Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 0.5 Adc)			—	1.0	
(I_C = 10 Adc, I_B = 2.5 Adc)			—	3.0	
Base–Emitter Saturation Voltage (1) (I_C = 10 Adc, I_B = 2.5 Adc)		$V_{BE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5877, 2N5878	C_{ob}	—	300	pF
Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	—	—
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 4.0 Adc, I_{B1} = I_{B2} = 0.4 Adc, See Figure 2)	t_r	—	0.7	μs
Storage Time		t_s	—	1.0	μs
Fall Time		t_f	—	0.8	μs

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.

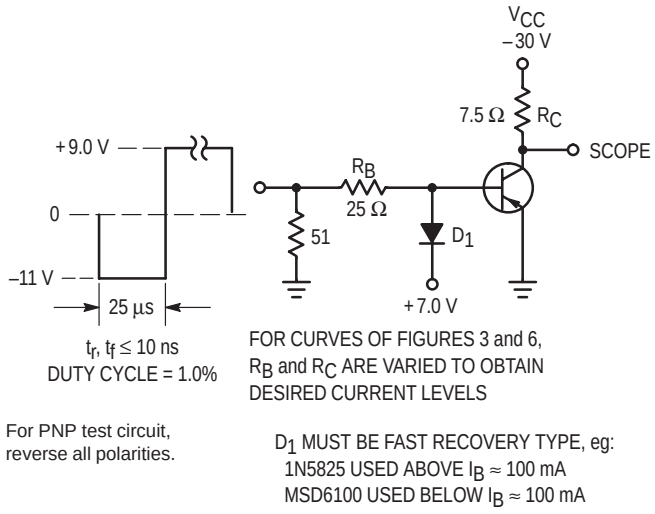


Figure 2. Switching Time Test Circuit

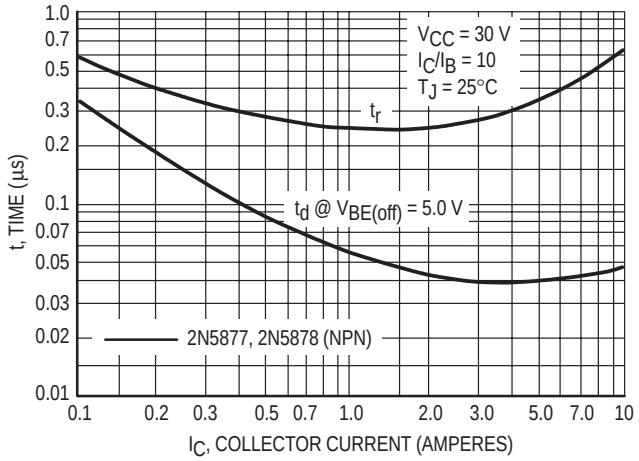


Figure 3. Turn–On Time

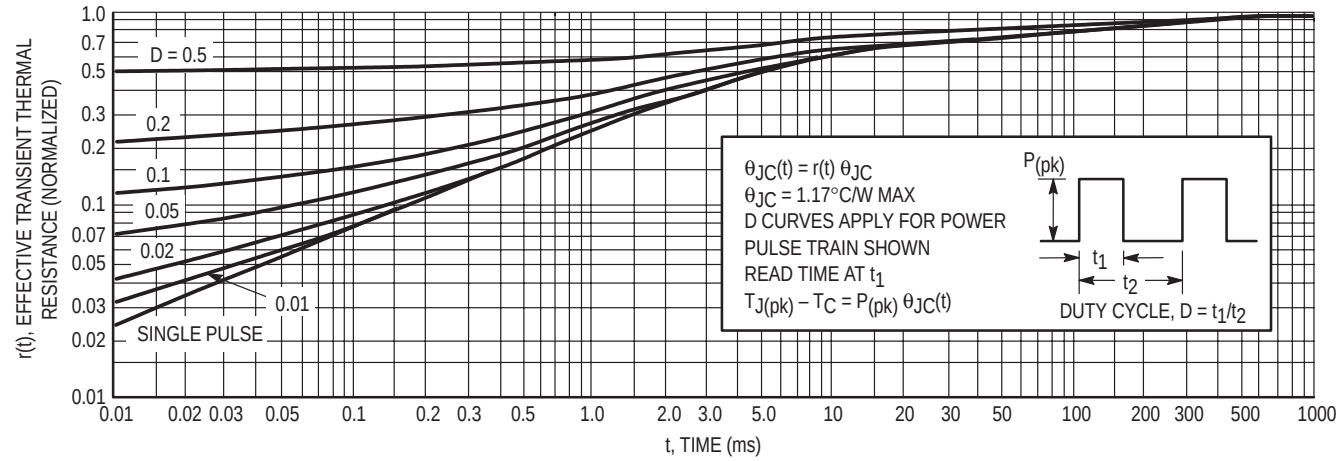


Figure 4. Thermal Response

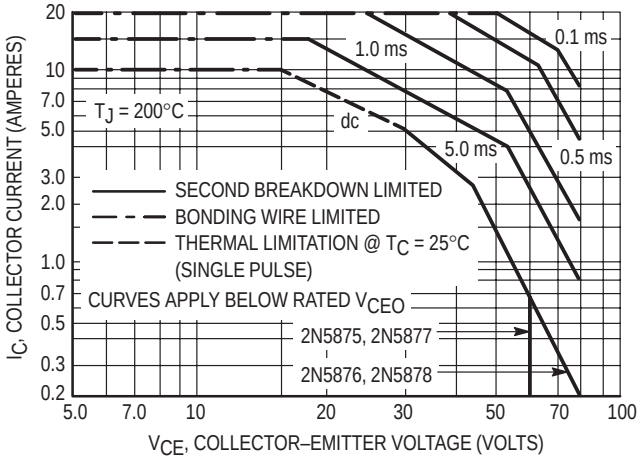


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

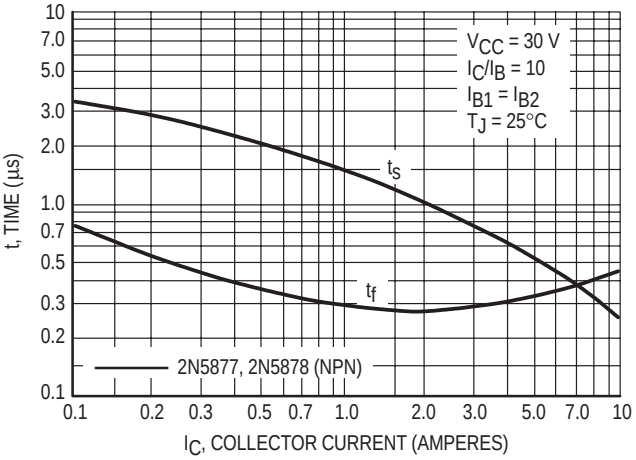


Figure 6. Turn–Off Time

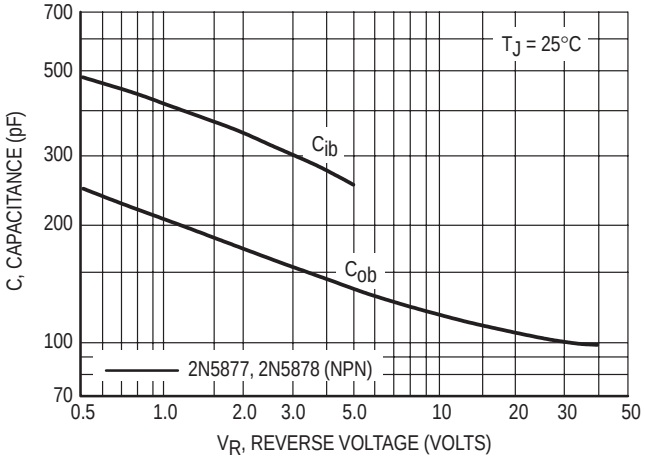


Figure 7. Capacitance

Complementary Silicon High-Power Transistors

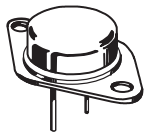
. . . designed for general–purpose power amplifier and switching applications.

- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N5879, 2N5881
  = 80 Vdc (Min) — 2N5880, 2N5882
- DC Current Gain —
  h_{FE} = 20 (Min) @ I_C = 6.0 Adc
- Low Collector — Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 7.0 Adc
- High Current — Gain–Bandwidth Product —
  f_T = 4.0 MHz (Min) @ I_C = 1.0 Adc

PNP
2N5879
2N5880*
NPN
2N5881
2N5882*

***Motorola Preferred Device**

15 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60 – 80 VOLTS
160 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (1)

Rating	Symbol	2N5879 2N5881	2N5880 2N5882	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	15 30		Adc
Base Current	I_B	5.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	160 0.915		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.1	°C/W

(1) Indicates JEDEC registered data. Units and conditions differ on some parameters and re–registration reflecting these changes has been requested. All above values meet or exceed present JEDEC registered data.

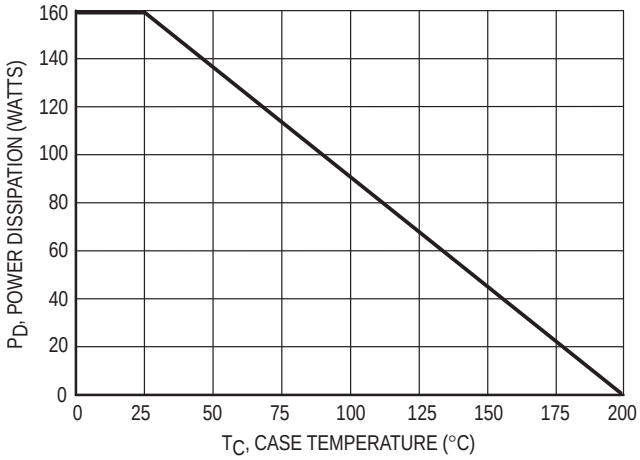


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)	2N5879, 2N5881	$V_{CEO(sus)}$	60	—	Vdc
(I_C = 200 mAdc, I_B = 0)	2N5880, 2N5882		80	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	2N5879, 2N5881		—	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N5880, 2N5882		—	1.0	
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5879, 2N5881		—	0.5	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5880, 2N5882		—	0.5	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5879, 2N5881		—	5.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5880, 2N5882		—	5.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5879, 2N5881		—	0.5	
(V_{CB} = 80 Vdc, I_E = 0)	2N5880, 2N5882		—	0.5	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			—
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)			35	—	
(I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)			20	100	
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			4.0	—	
Collector–Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 7.0 Adc, I_B = 0.7 Adc)			—	1.0	
(I_C = 15 Adc, I_B = 3.75 Adc)			—	4.0	
Base–Emitter Saturation Voltage (1) (I_C = 15 Adc, I_B = 3.75 Adc)		$V_{BE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (1) (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2)		f_T	4.0	—	MHz
(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)					
Output Capacitance	2N5879, 2N5880	C_{ob}	—	600	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)	2N5881, 2N5882		—	400	
Small–Signal Current Gain (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	20	—	—
SWITCHING CHARACTERISTICS					
Rise Time	(V_{CC} = 30 Vdc, I_C = 6.0 Adc, I_{B1} = I_{B2} = 0.6 Adc See Figure 2)	t_r	—	0.7	µs
Storage Time		t_s	—	1.0	µs
Fall Time		t_f	—	0.8	µs

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%

(2) $f_T = |h_{fe}| \bullet f_{test}$.

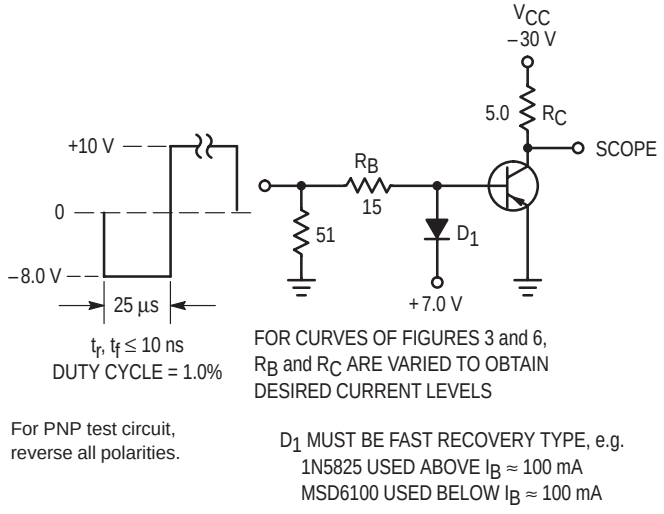


Figure 2. Switching Times Test Circuit

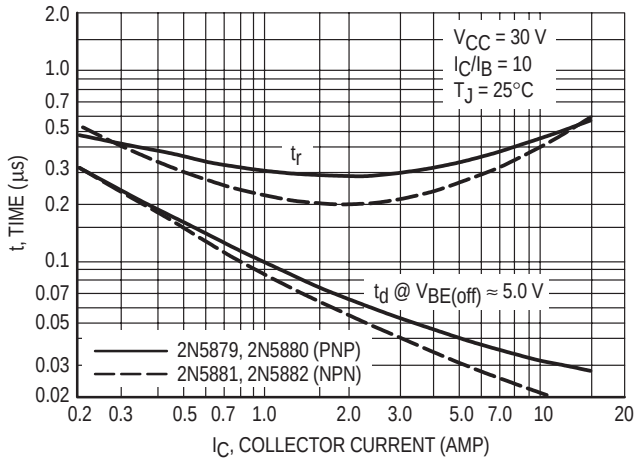


Figure 3. Turn–On Time

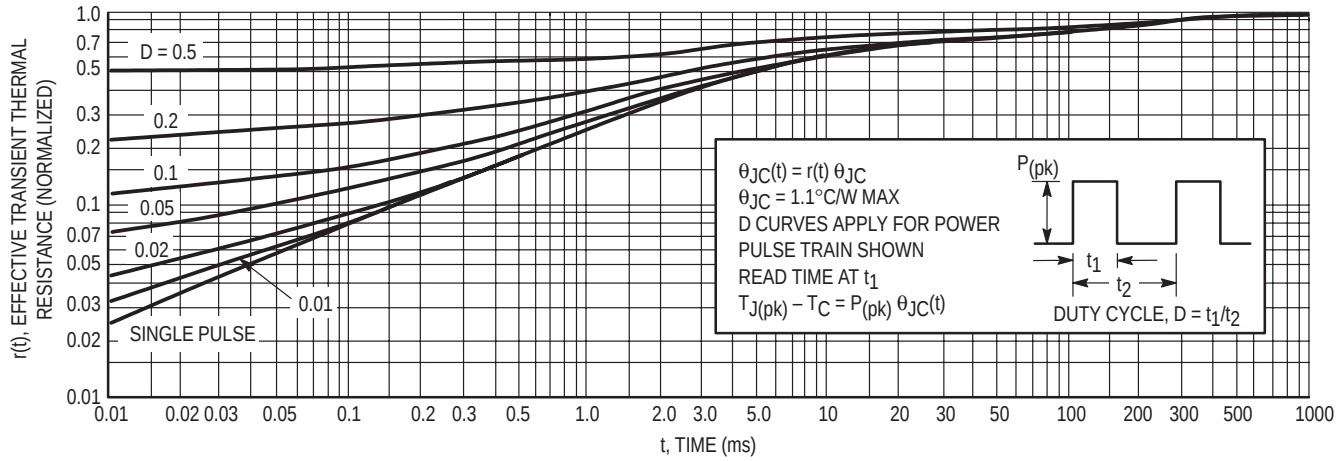


Figure 4. Thermal Response

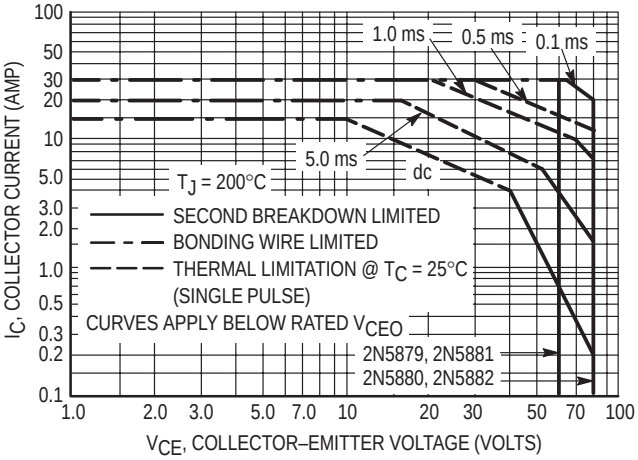


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

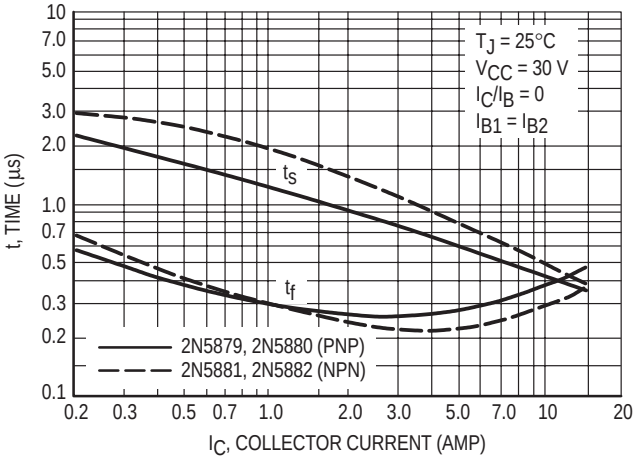


Figure 6. Turn–Off Time

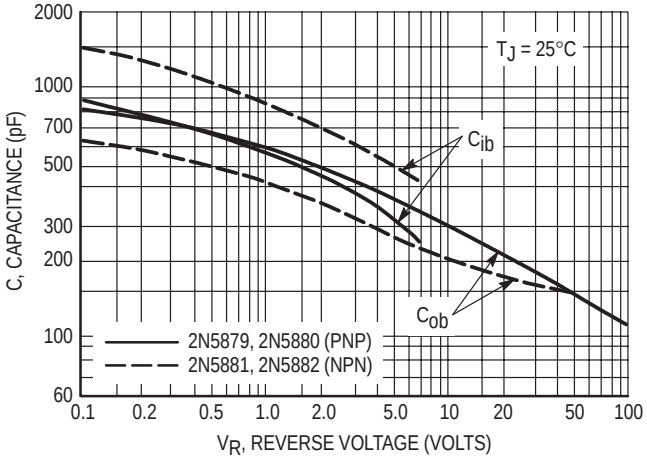
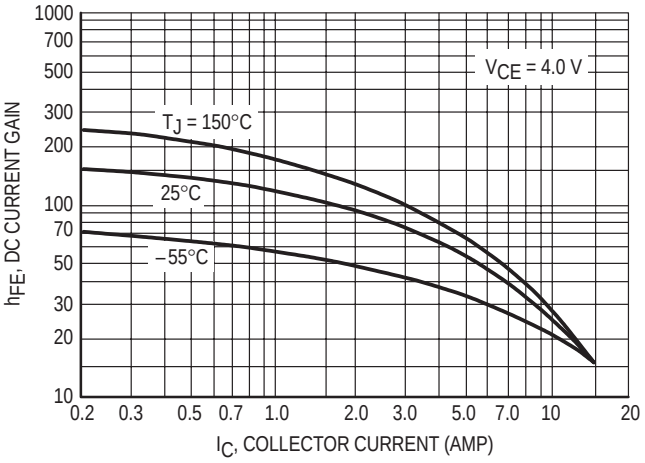


Figure 7. Capacitance

PNP
2N5879, 2N5880



NPN
2N5881, 2N5882

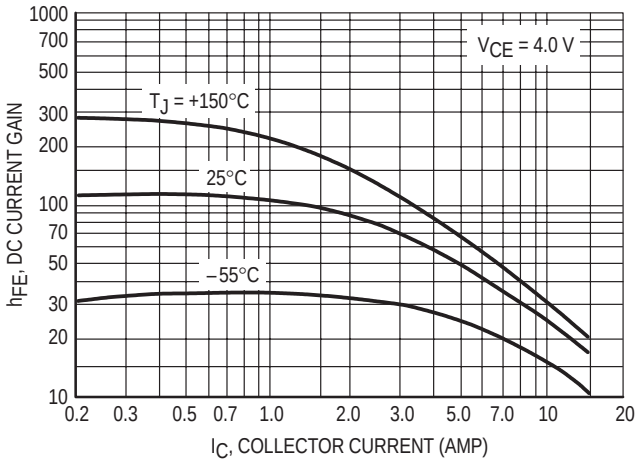
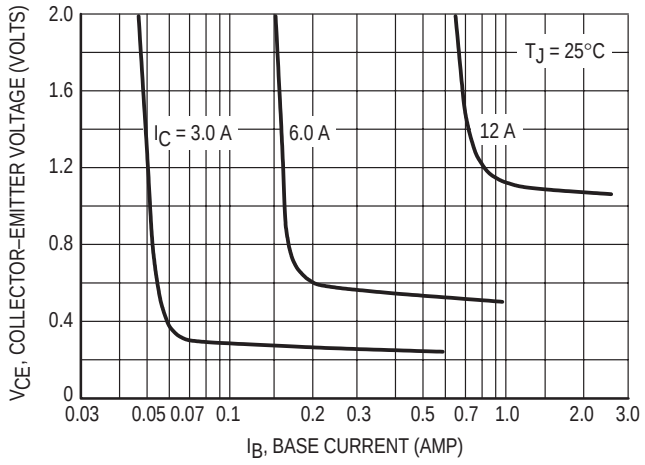


Figure 8. DC Current Gain



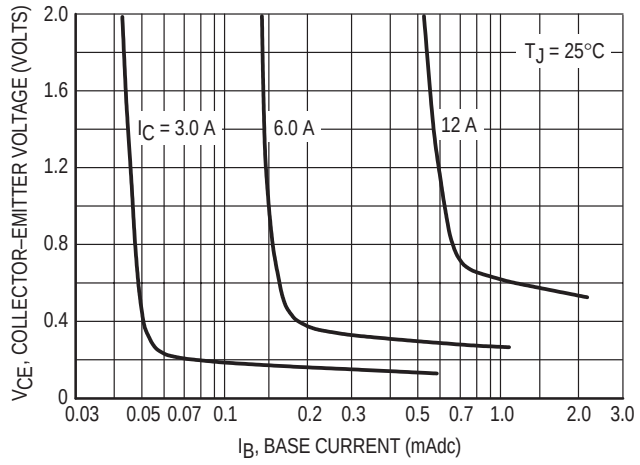
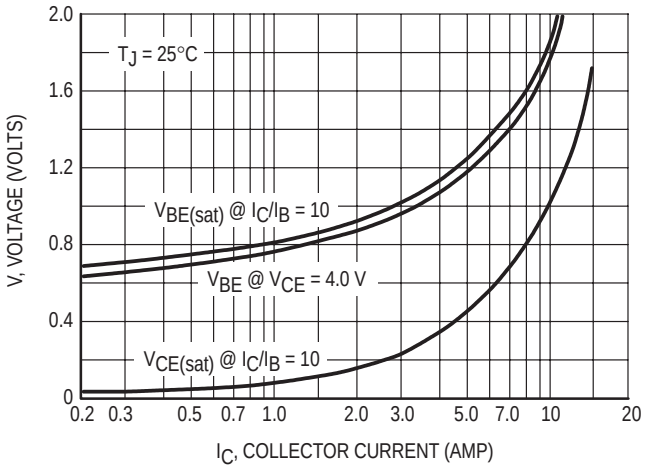


Figure 9. Collector Saturation Region



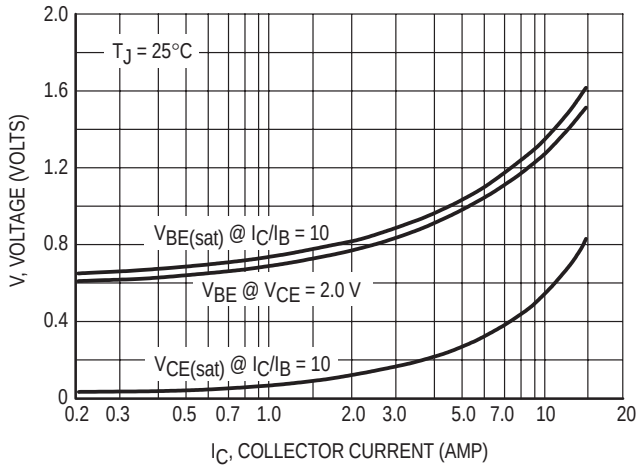


Figure 10. “On” Voltages

Complementary Silicon High-Power Transistors

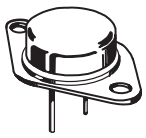
. . . designed for general–purpose power amplifier and switching applications.

- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc, (max) at I_C = 15 Adc
- Low Leakage Current
  I_{CEX} = 1.0 mAdc (max) at Rated Voltage
- Excellent DC Current Gain —
  h_{FE} = 20 (min) at I_C = 10 Adc
- High Current Gain Bandwidth Product —
  f_τ = 4.0 MHz (min) at I_C = 1.0 Adc

PNP
2N5883
2N5884*
NPN
2N5885
2N5886*

***Motorola Preferred Device**

25 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60 – 80 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (1)

Rating	Symbol	2N5883 2N5885	2N5884 2N5886	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	25 50		Adc
Base Current	I_B	7.5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.15		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

(1) Indicates JEDEC registered data. Units and conditions differ on some parameters and re–registration reflecting these changes has been requested. All above values most or exceed present JEDEC registered data.

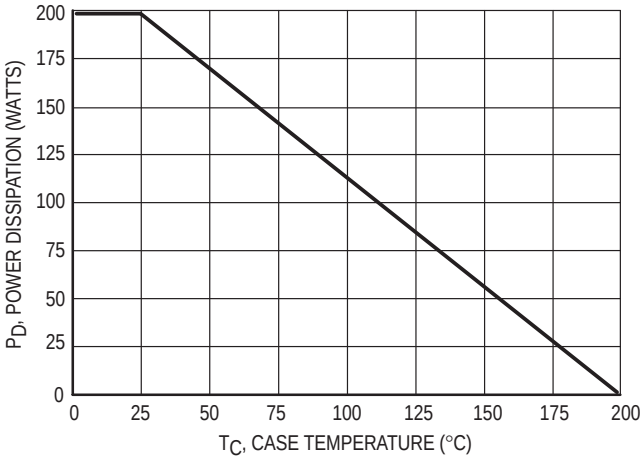


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N5883, 2N5885 2N5884, 2N5886	$V_{CEO(sus)}$	60 80	— —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	2N5883, 2N5885 2N5984, 2N5886	I_{CEO}	— —	2.0 2.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	 2N5883, 2N5885 2N5884, 2N5886 2N5883, 2N5885 2N5884, 2N5886	I_{CEX}	 — — —	 1.0 1.0 10 10	mAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	 2N5883, 2N5885 2N5884, 2N5886	I_{CBO}	 — —	 1.0 1.0	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc

ON CHARACTERISTICS

DC Current Gain (1) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc) (I_C = 25 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	35 20 4.0	— 100	—
Collector–Emitter Saturation Voltage (1) (I_C = 15 Adc, I_B = 1.5 Adc) (I_C = 25 Adc, I_B = 6.25 Adc)	$V_{CE(sat)}$	— —	1.0 4.0	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 25 Adc, I_B = 6.25 Adc)	$V_{BE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (1) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	1.5	Vdc

DYNAMIC CHARACTERISTICS

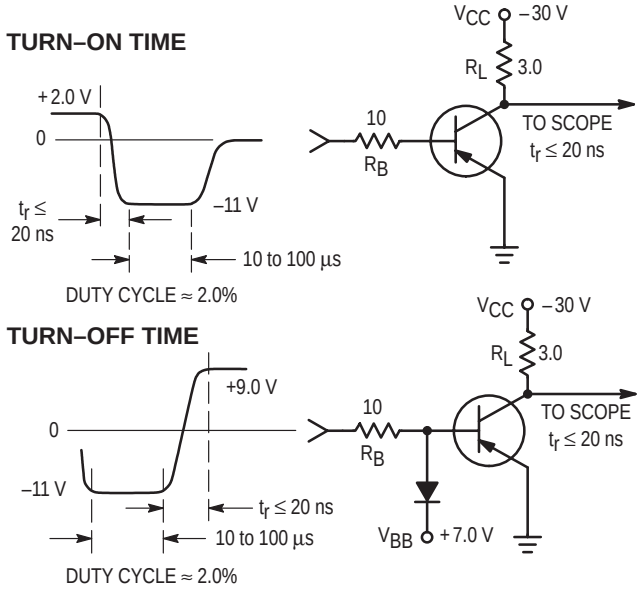
Current–Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5883, 2N5884 2N5885, 2N5886	C_{ob}	— —	1000 500	pF
Small–Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 kHz)	h_{fe}	20	—	—

SWITCHING CHARACTERISTICS

Rise Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_r	—	0.7	μs
Storage Time		t_s	—	1.0	μs
Fall Time		t_f	—	0.8	μs

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%. (2) $f_T = |h_{fe}| \bullet f_{test}$.



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN, REVERSE ALL POLARITIES.

Figure 2. Switching Time Equivalent Test Circuits

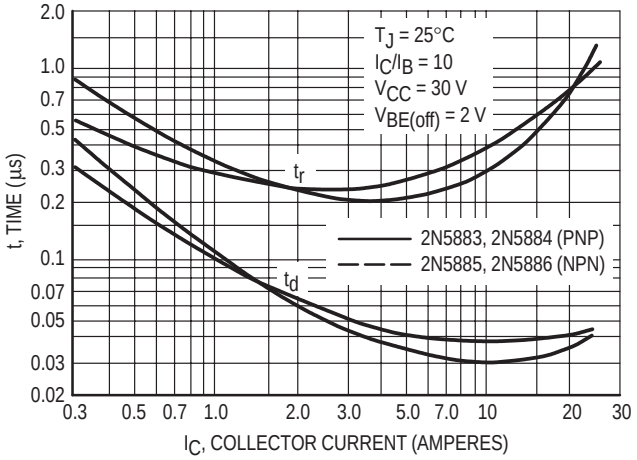


Figure 3. Turn–On Time

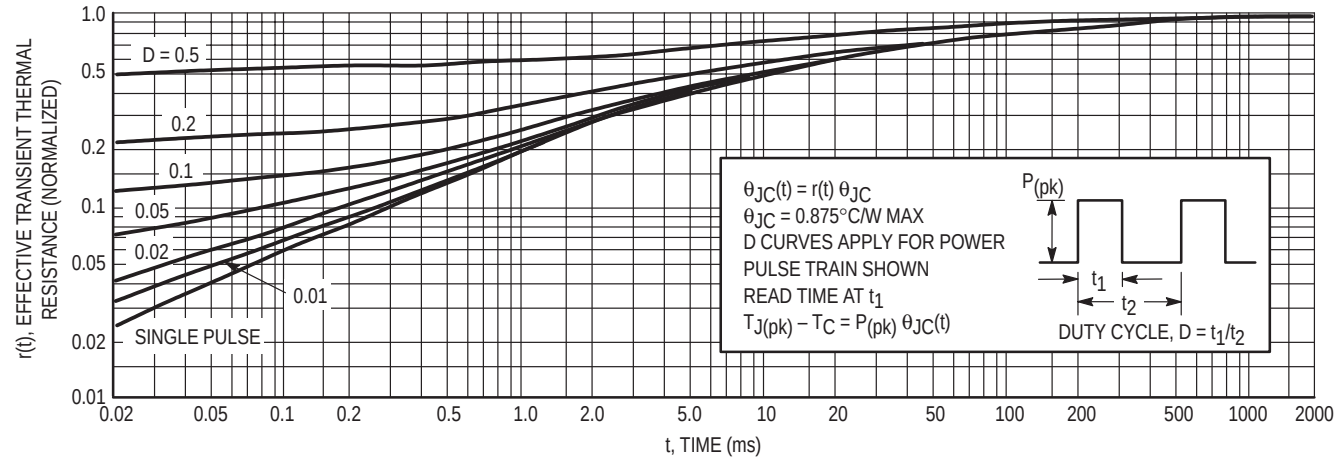


Figure 4. Thermal Response

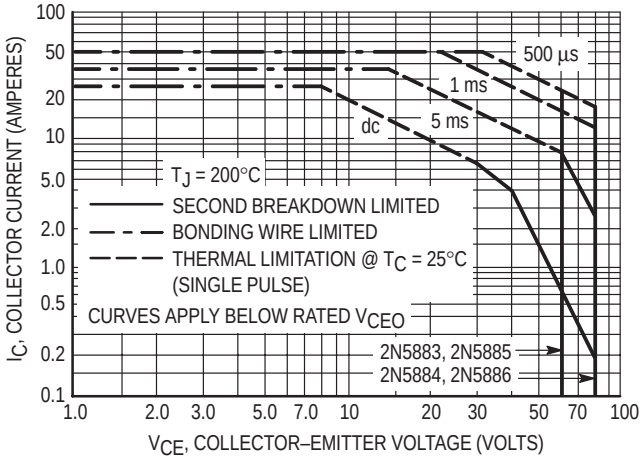


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

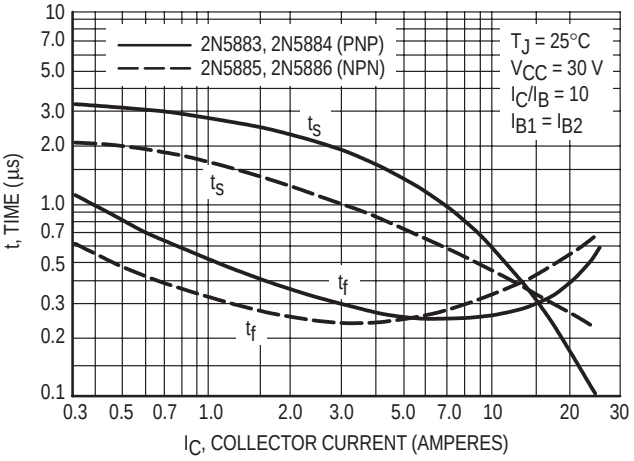


Figure 6. Turn–Off Time

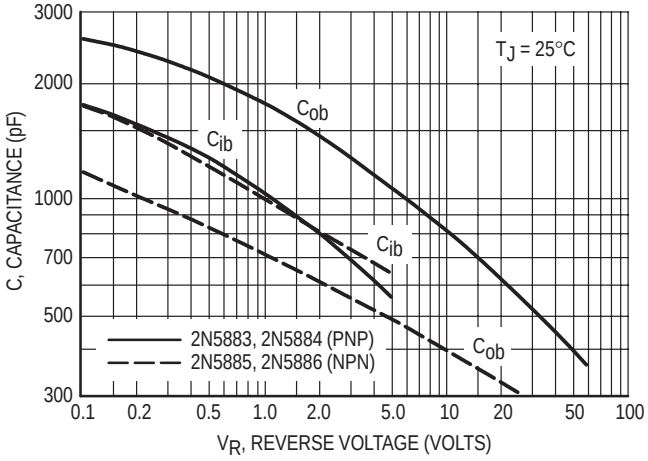
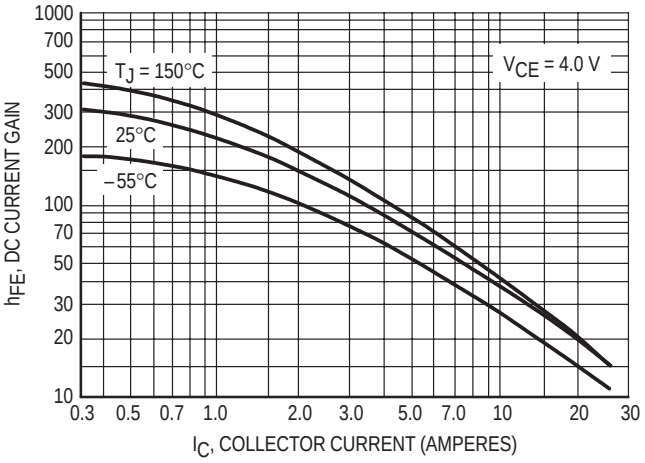


Figure 7. Capacitance

PNP DEVICES
2N5883 and 2N5884



NPN DEVICES
2N5885 and 2N5886

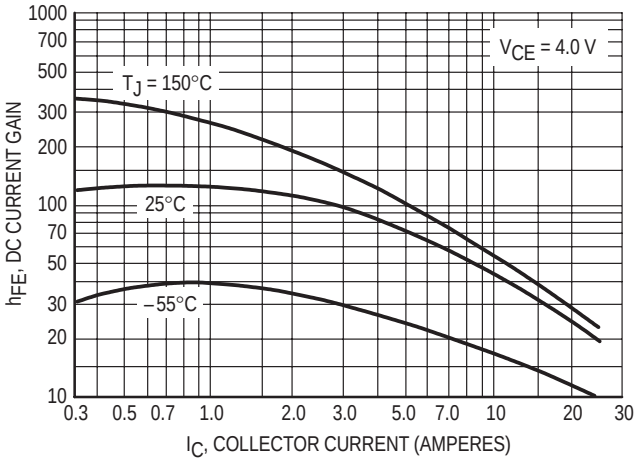
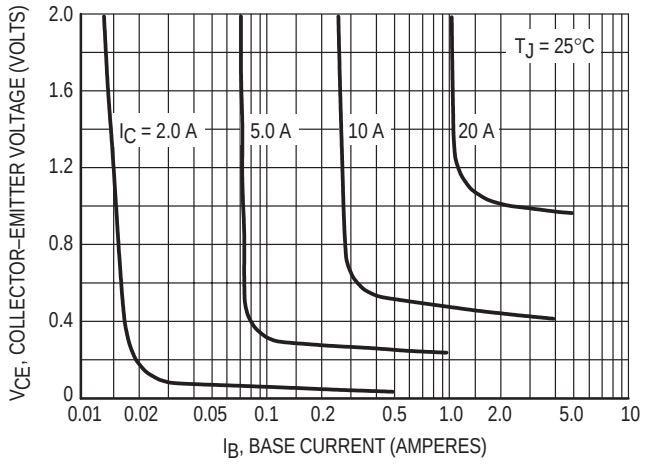


Figure 8. DC Current Gain



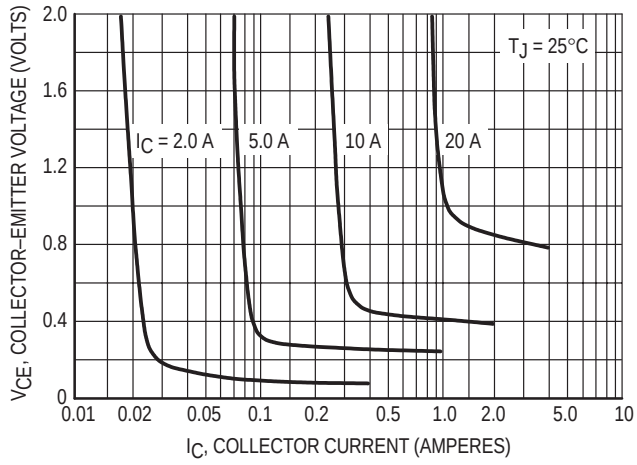
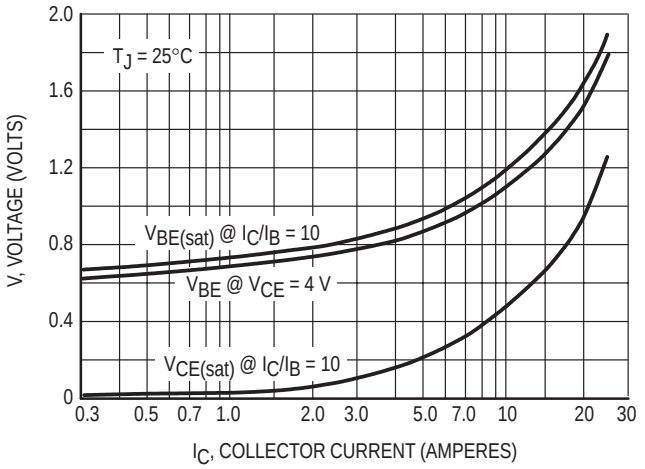


Figure 9. Collector Saturation Region



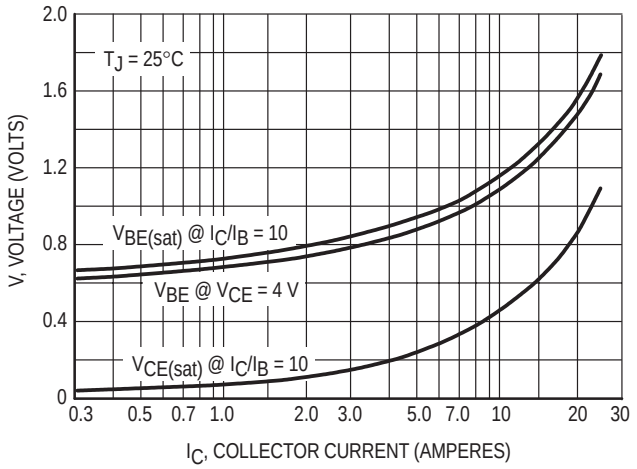


Figure 10. “On” Voltages

2N6030 thru 2N6031
(See 2N5630)

Plastic Darlington Complementary Silicon Power Transistors

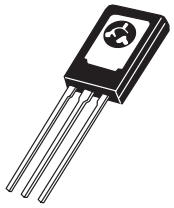
PNP
2N6035
2N6036*
NPN
2N6038
2N6039*

*Motorola Preferred Device

. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain —
  h_{FE} = 2000 (Typ) @ I_C = 2.0 Adc
- Collector–Emitter Sustaining Voltage — @ 100 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6035, 2N6038
  = 80 Vdc (Min) — 2N6036, 2N6039
- Forward Biased Second Breakdown Current Capability
  $I_{S/b}$ = 1.5 Adc @ 25 Vdc
- Monolithic Construction with Built–In Base–Emitter Resistors to Limit Leakage Multiplication
- Space–Saving High Performance–to–Cost Ratio TO–225AA Plastic Package

DARLINGTON
4–AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60, 80 VOLTS
40 WATTS



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS (1)

Rating	Symbol	2N6035 2N6038	2N6036 2N6039	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	4.0 8.0		Adc
Base Current	I_B	100		mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012		Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.3	°C/W

(1) Indicates JEDEC Registered Data.

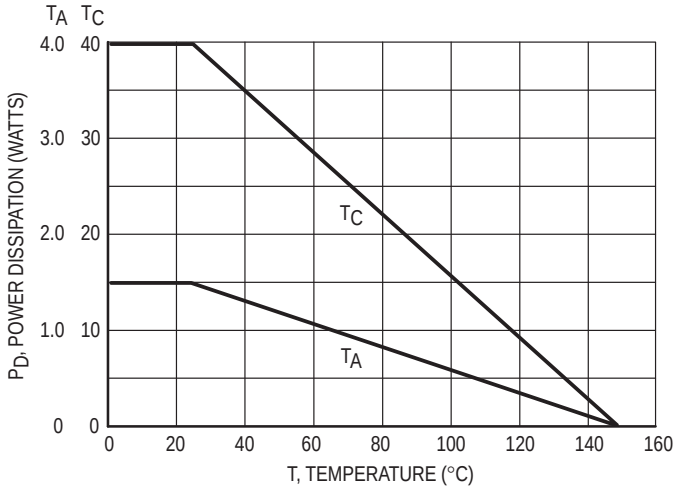


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	2N6035, 2N6038 2N6036, 2N6039	$V_{CEO(sus)}$	 60 80	 — —	Vdc
Collector–Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	 2N6035, 2N6038 2N6036, 2N6039	I_{CEO}	 — —	 100 100	μA
Collector–Cutoff Current (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	 2N6035, 2N6038 2N6036, 2N6039 2N6035, 2N6038 2N6036, 2N6039	I_{CEX}	 — — — —	 100 100 500 500	μA
Collector–Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	 2N6035, 2N6038 2N6036, 2N6039	I_{CBO}	 — —	 0.5 0.5	mAdc
Emitter–Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	 500 750 100	 — 15,000 —	—
Collector–Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 8.0 mAdc) (I_C = 4.0 Adc, I_B = 40 mAdc)		$V_{CE(sat)}$	 — —	 2.0 3.0	Vdc
Base–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 40 mAdc)		$V_{BE(sat)}$	—	4.0	Vdc
Base–Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small–Signal Current–Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	25	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	 2N6035, 2N6036 2N6038, 2N6039	C_{ob}	 — —	 200 100	pF

* Indicates JEDEC Registered Data.

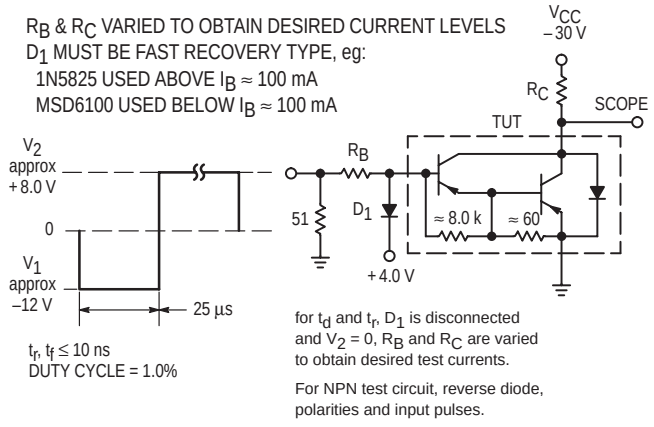


Figure 2. Switching Times Test Circuit

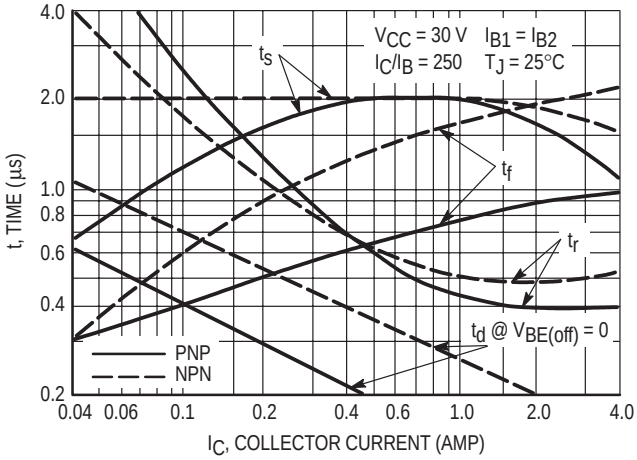


Figure 3. Switching Times

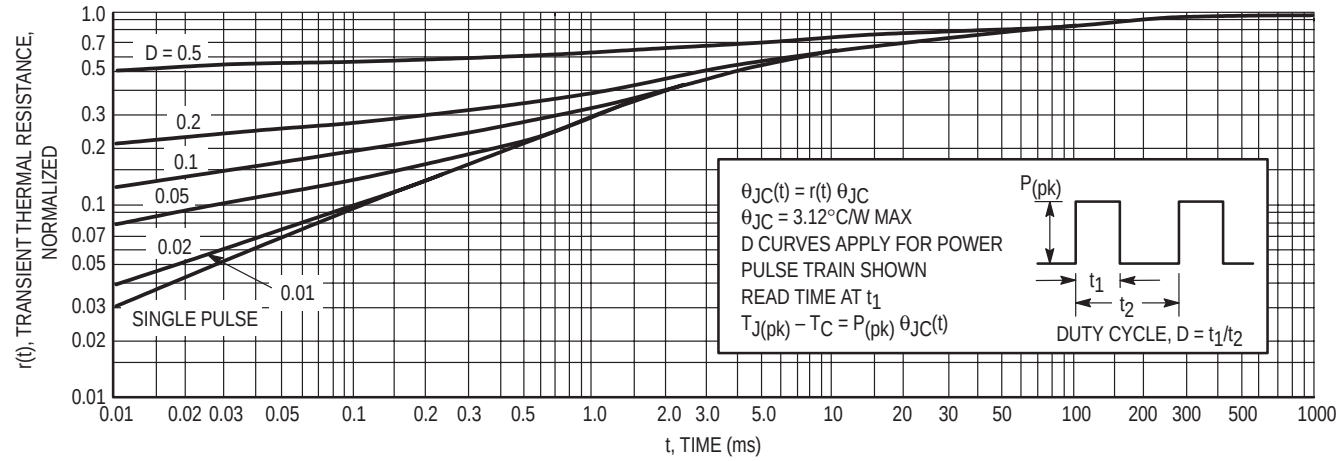


Figure 4. Thermal Response

ACTIVE–REGION SAFE–OPERATING AREA

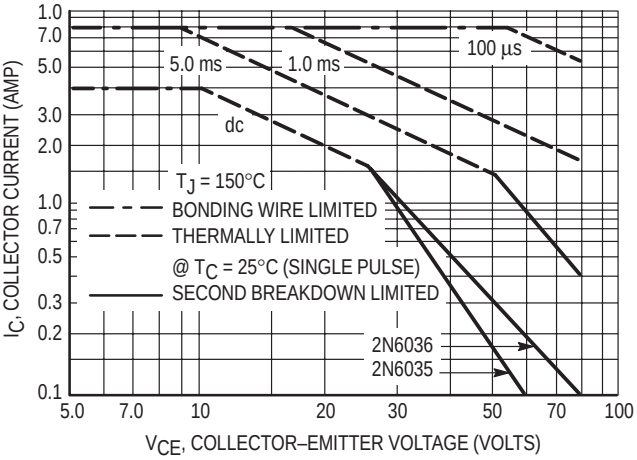


Figure 5. 2N6035, 2N6036

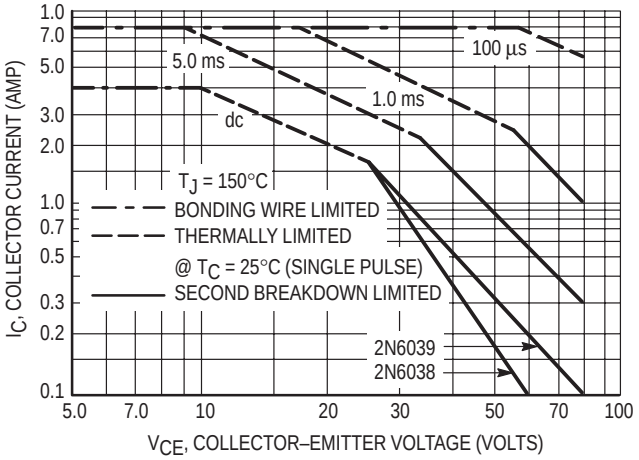


Figure 6. 2N6038, 2N6039

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

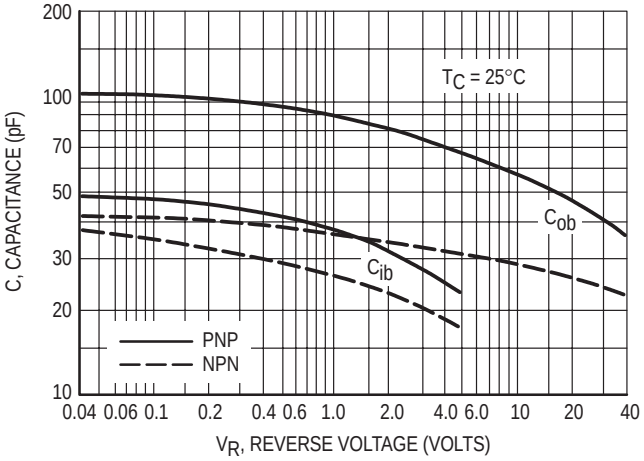
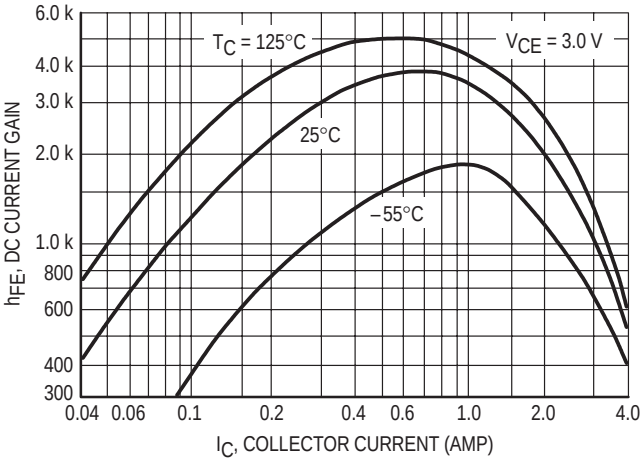


Figure 7. Capacitance

PNP
2N6035, 2N6036



NPN
2N6038, 2N6039

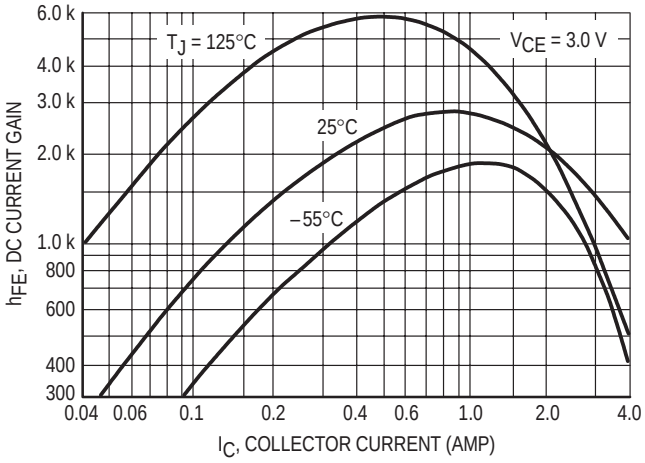
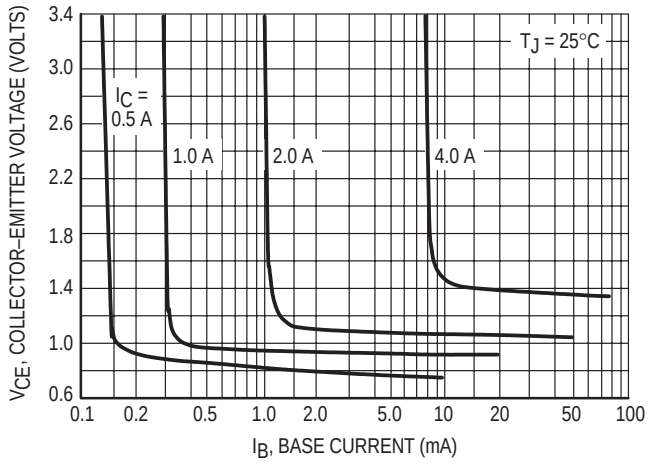


Figure 8. DC Current Gain



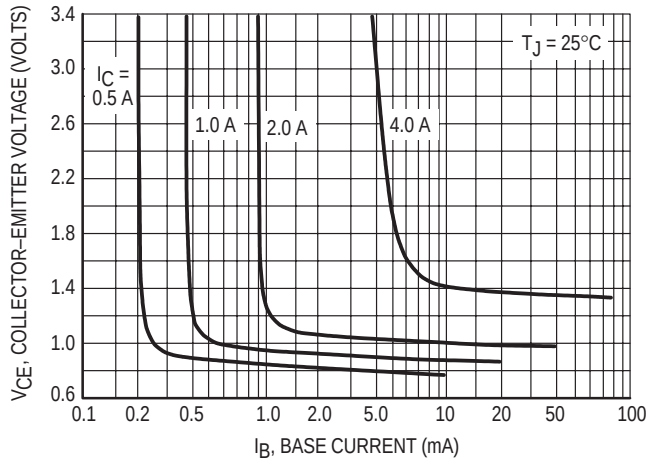
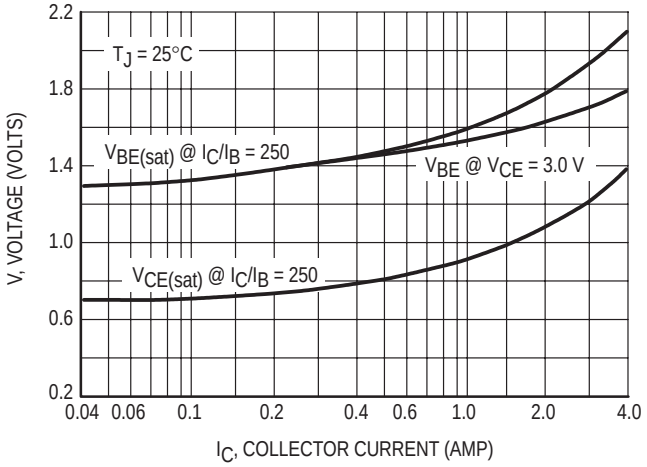


Figure 9. Collector Saturation Region



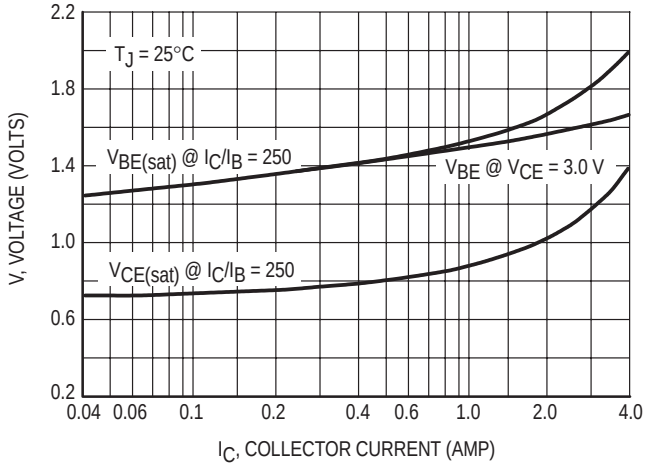


Figure 10. “On” Voltages

Plastic Medium-Power Complementary Silicon Transistors

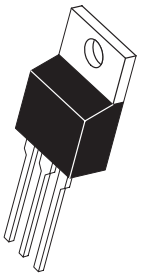
. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector–Emitter Sustaining Voltage — @ 100 mAdc —
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6040, 2N6043
  = 80 Vdc (Min) — 2N6041, 2N6044
  = 100 Vdc (Min) — 2N6042, 2N6045
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 4.0 Adc — 2N6040,41, 2N6043,44
  = 2.0 Vdc (Max) @ I_C = 3.0 Adc — 2N6042, 2N6045
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors

PNP
2N6040
thru
2N6042*
NPN
2N6043
thru
2N6045*

***Motorola Preferred Device**

DARLINGTON
8 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60 – 80 – 100 VOLTS
75 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS (1)

Rating	Symbol	2N6040 2N6043	2N6041 2N6044	2N6042 2N6045	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	8.0 16			Adc
Base Current	I_B	120			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.60			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.2 0.0175			Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	57	°C/W

(1) Indicates JEDEC Registered Data.

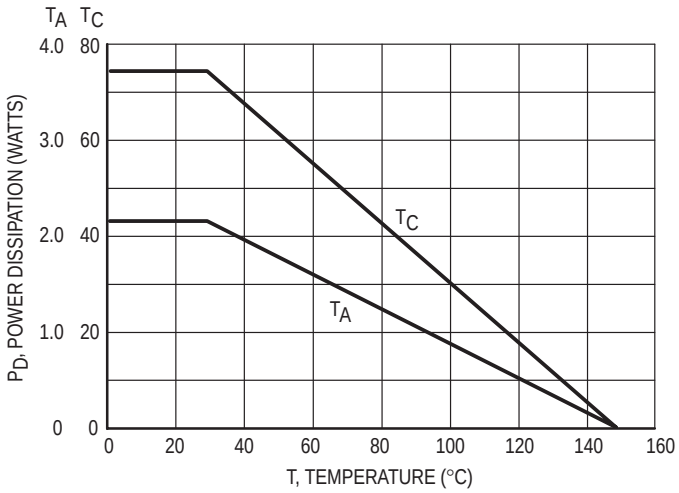


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	2N6040, 2N6043	$V_{CEO(sus)}$	60	—	Vdc
	2N6041, 2N6044		80	—	
	2N6042, 2N6045		100	—	
Collector Cutoff Current		I_{CEO}			μA
(V_{CE} = 60 Vdc, I_B = 0)	2N6040, 2N6043		—	20	
(V_{CE} = 80 Vdc, I_B = 0)	2N6041, 2N6044		—	20	
(V_{CE} = 100 Vdc, I_B = 0)	2N6042, 2N6045		—	20	
Collector Cutoff Current		I_{CEX}			μA
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6040, 2N6043		—	20	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6041, 2N6044		—	20	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6042, 2N6045		—	20	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6040, 2N6043		—	200	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6041, 2N6044		—	200	
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6042, 2N6045		—	200	
Collector Cutoff Current		I_{CBO}			μA
(V_{CB} = 60 Vdc, I_E = 0)	2N6040, 2N6043		—	20	
(V_{CB} = 80 Vdc, I_E = 0)	2N6041, 2N6044		—	20	
(V_{CB} = 100 Vdc, I_E = 0)	2N6042, 2N6045		—	20	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			—
(I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	2N6040, 41, 2N6043, 44		1000	20.000	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	2N6042, 2N6045		1000	20,000	
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	All Types		100	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 4.0 Adc, I_B = 16 mAdc)	2N6040, 41, 2N6043, 44		—	2.0	
(I_C = 3.0 Adc, I_B = 12 mAdc)	2N6042, 2N6045		—	2.0	
(I_C = 8.0 Adc, I_B = 80 Adc)	All Types		—	4.0	
Base–Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 80 mAdc)		$V_{BE(sat)}$	—	4.5	Vdc
Base–Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	—	
Output Capacitance	2N6040/2N6042	C_{ob}	—	300	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6043/2N6045		—	200	
Small–Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	300	—	—

* Indicates JEDEC Registered Data.

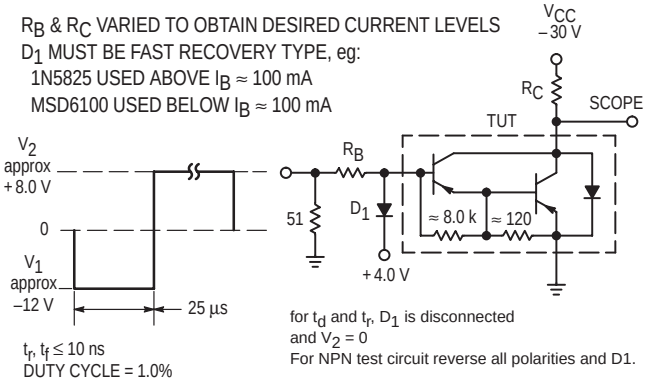


Figure 2. Switching Times Equivalent Circuit

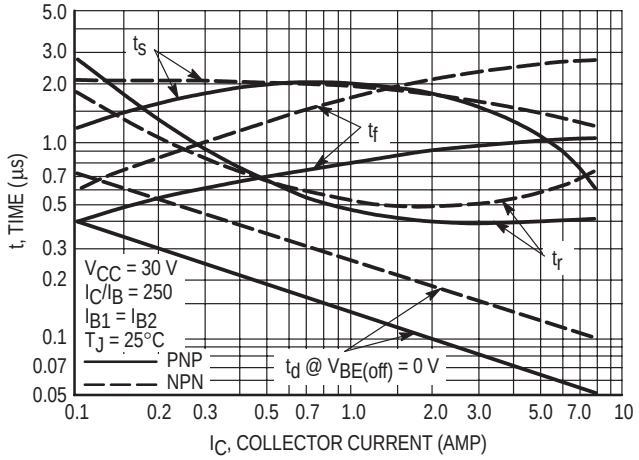


Figure 3. Switching Times

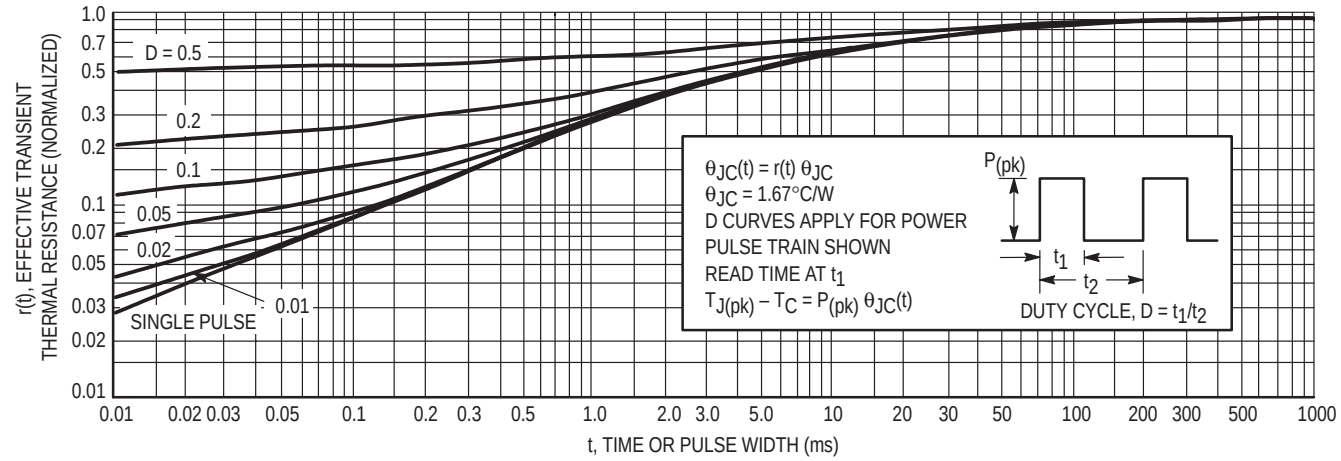


Figure 4. Thermal Response

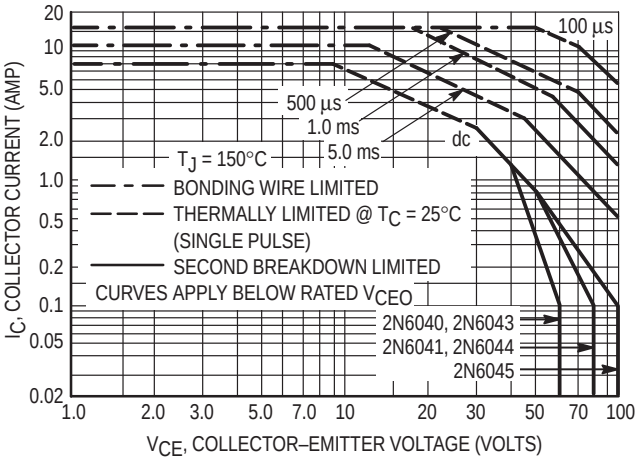


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

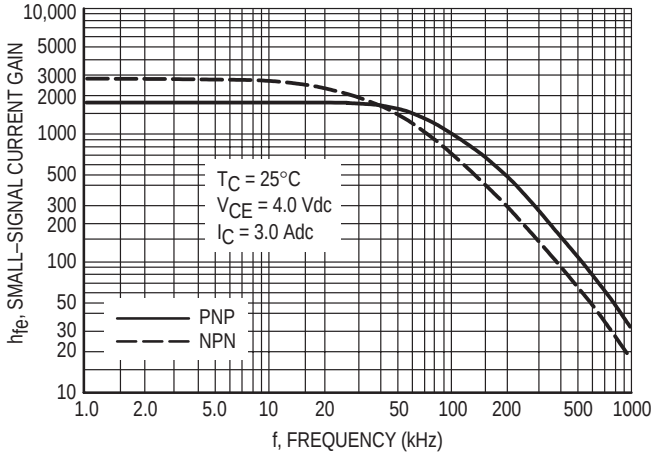


Figure 6. Small–Signal Current Gain

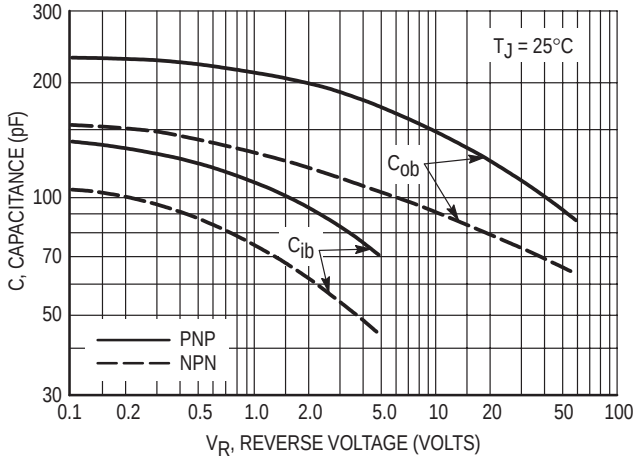
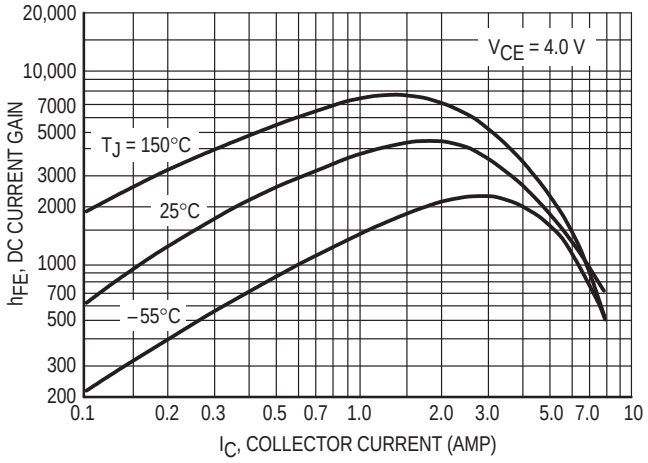


Figure 7. Capacitance

PNP
2N6040, 2N6041, 2N6042



NPN
2N6043, 2N6044, 2N6045

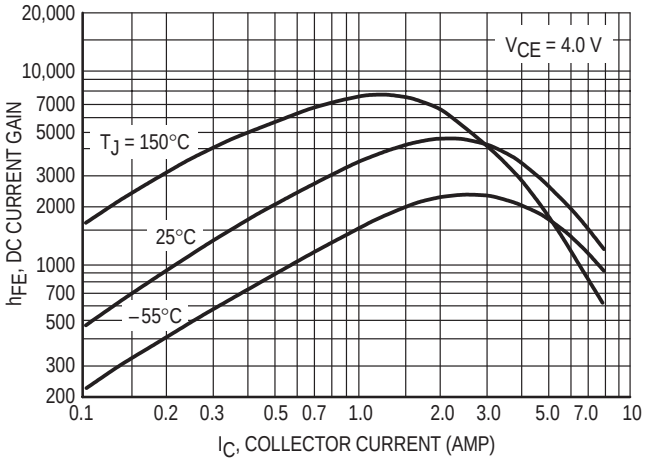
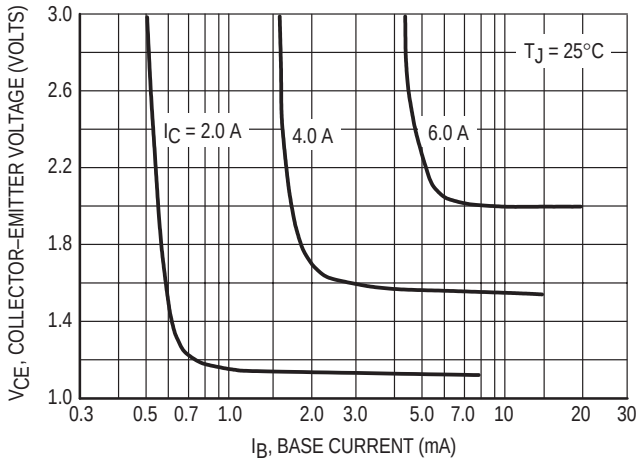


Figure 8. DC Current Gain



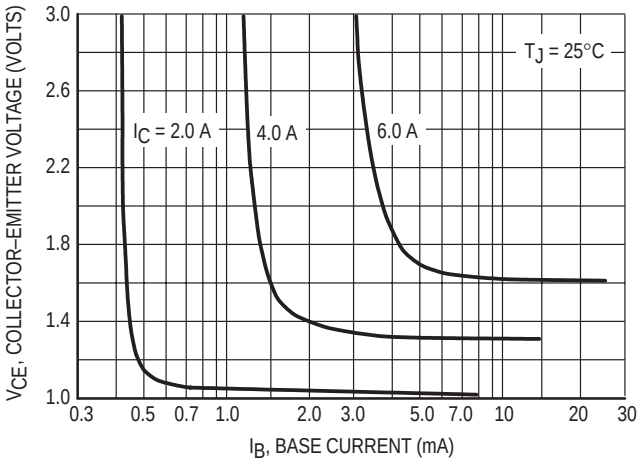
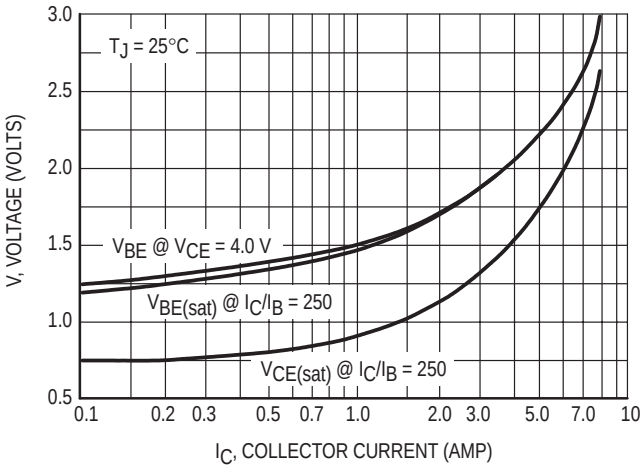


Figure 9. Collector Saturation Region



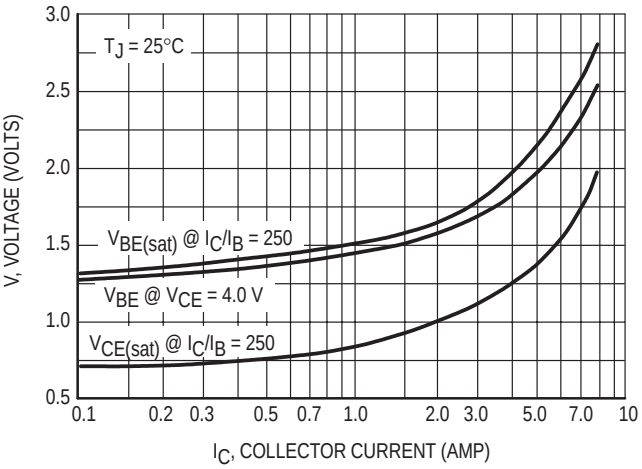


Figure 10. “On” Voltages

Darlington Complementary Silicon Power Transistors

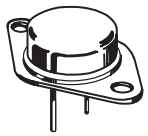
. . . designed for general–purpose amplifier and low frequency switching applications.

- High DC Current Gain —
  h_{FE} = 3500 (Typ) @ I_C = 5.0 Adc
- Collector–Emitter Sustaining Voltage — @ 100 mA
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6050, 2N6057
  80 Vdc (Min) — 2N6051, 2N6058
  100 Vdc (Min) — 2N6052, 2N6059
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors

PNP
2N6050
thru
2N6052*
NPN
2N6057
thru
2N6059*

***Motorola Preferred Device**

DARLINGTON
12 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60 – 80 – 100 VOLTS
150 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (1)

Rating	Symbol	2N6050 2N6057	2N6051 2N6058	2N6052 2N6059	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	12 20			Adc
Base Current	I_B	0.2			Adc
Total Device Dissipation @T_C = 25°C Derate above 25°C	P_D	150 0.857			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200°C			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Rating	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

(1) Indicates JEDEC Registered Data.

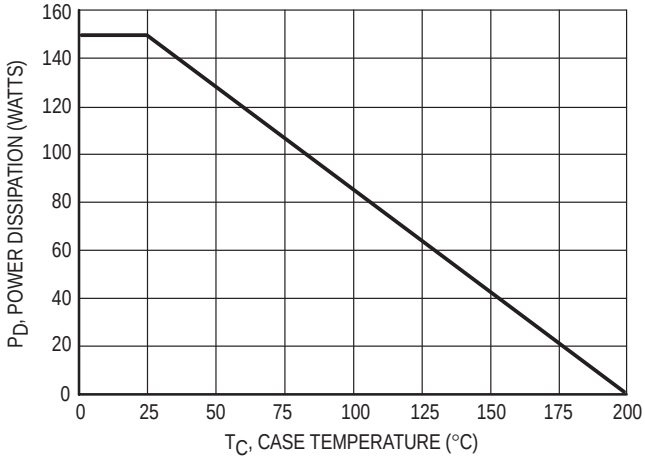


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

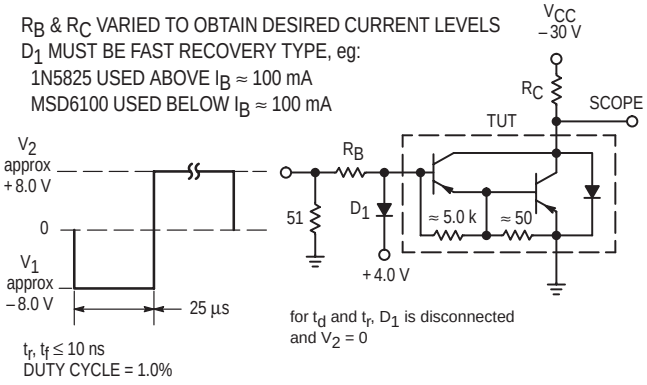
REV 1

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	2N6050, 2N6057 2N6051, 2N6058 2N6052, 2N6059	$V_{CEO(sus)}$	 60 80 100	 — — —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	 2N6050, 2N6057 2N6051, 2N6058 2N6052, 2N6059	I_{CEO}	 — — —	 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	 —	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 6.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 12 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	 750 100	 18,000 —	—
Collector–Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 24 mAdc) (I_C = 12 Adc, I_B = 120 mAdc)		$V_{CE(sat)}$	 — —	 2.0 3.0	Vdc
Base–Emitter Saturation Voltage (I_C = 12 Adc, I_B = 120 mAdc)		$V_{BE(sat)}$	—	4.0	Vdc
Base–Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small–Signal Short Circuit Forward Current Transfer Ratio (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6050/2N6052 2N6057/2N6059	C_{ob}	 —	500 300	pF
Small–Signal Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	—	—

* Indicates JEDEC Registered Data.

(1) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2.0%.



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

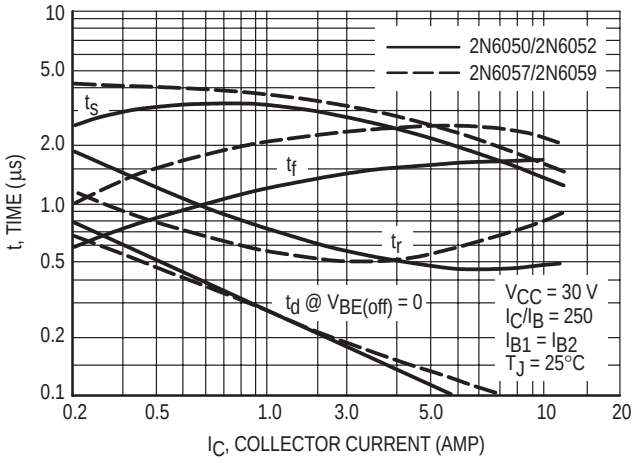


Figure 3. Switching Times

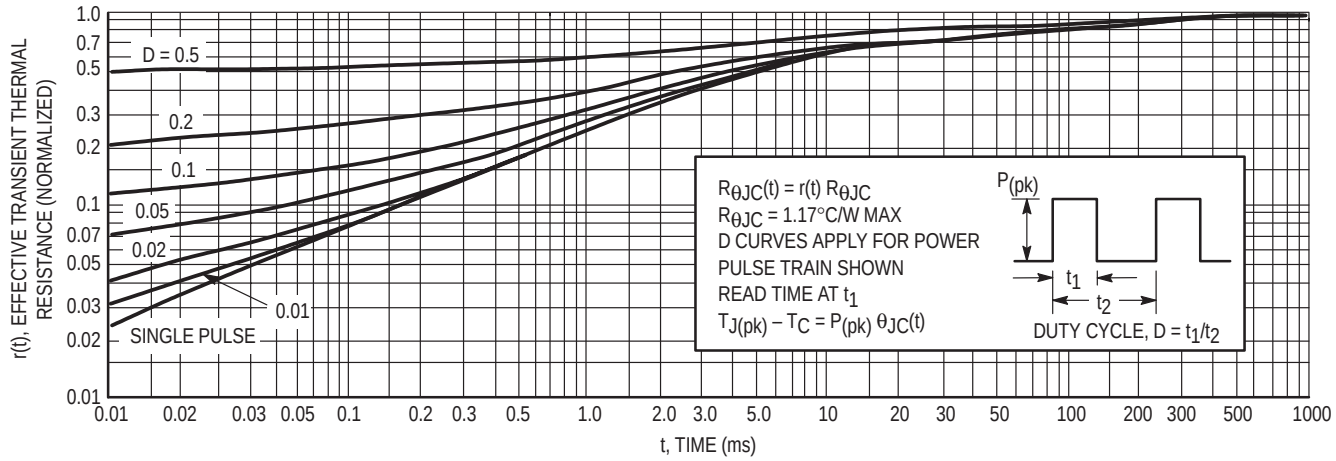


Figure 4. Thermal Response

ACTIVE–REGION SAFE OPERATING AREA

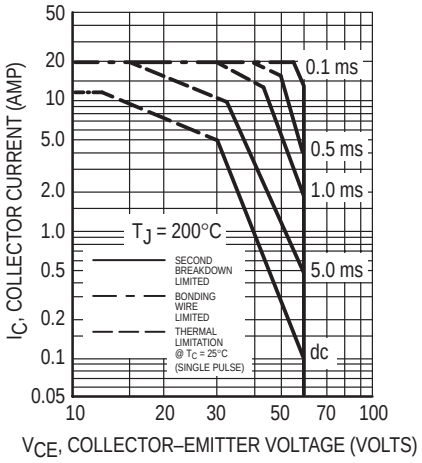


Figure 5. 2N6050, 2N6057

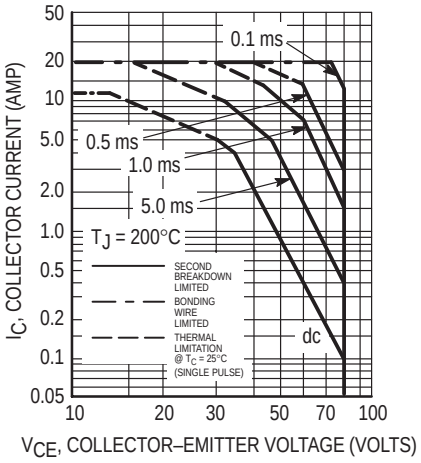


Figure 6. 2N6051, 2N6058

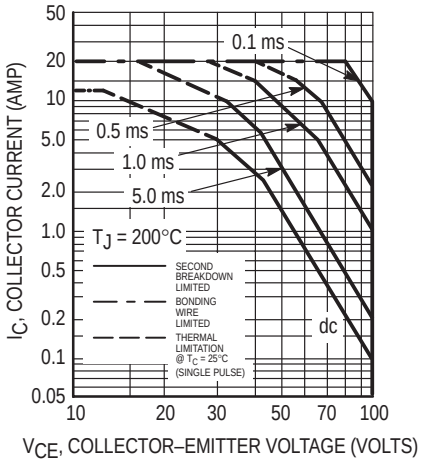


Figure 7. 2N6052, 2N6059

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6 and 7 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$; $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

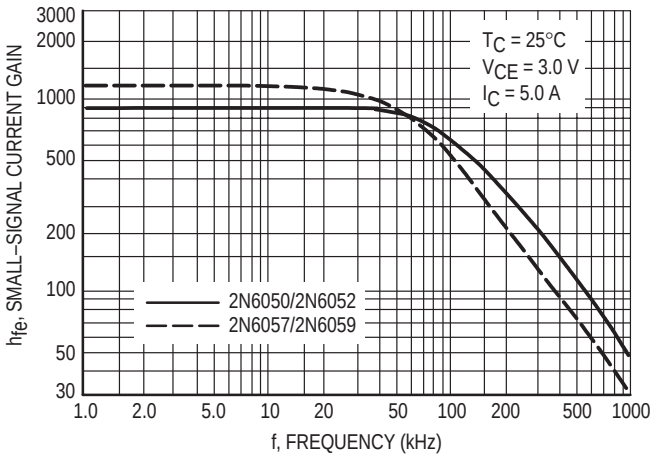


Figure 8. Small–Signal Current Gain

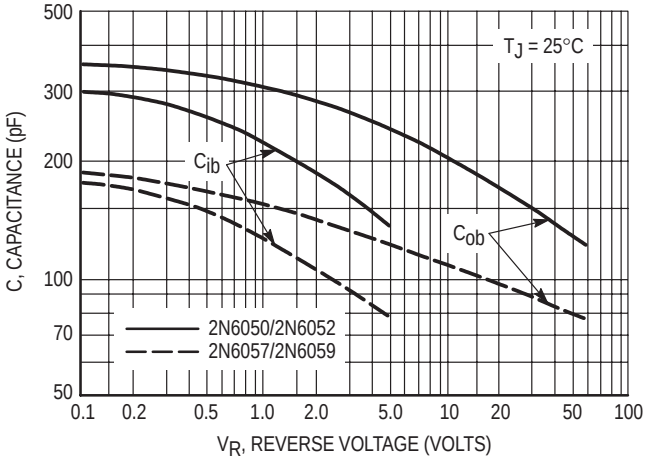
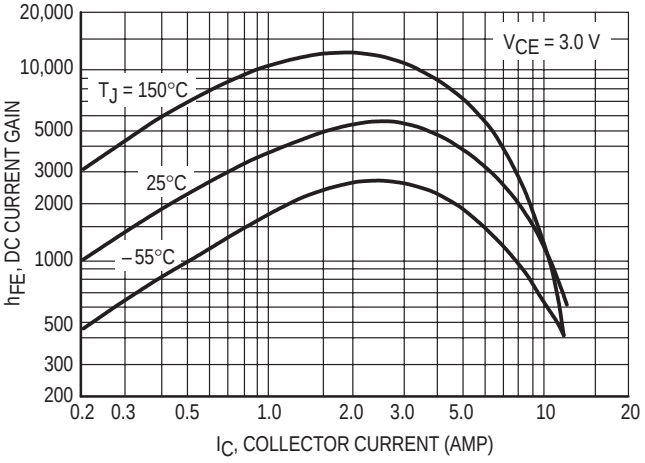


Figure 9. Capacitance

PNP
2N6050, 2N6051, 2N6052



NPN
2N6057, 2N6058, 2N6059

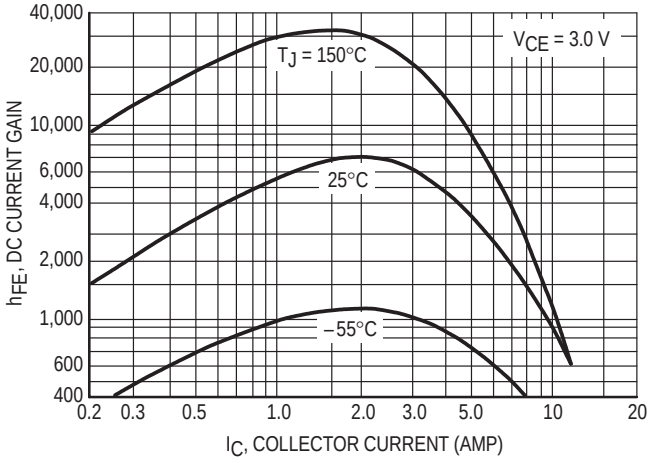
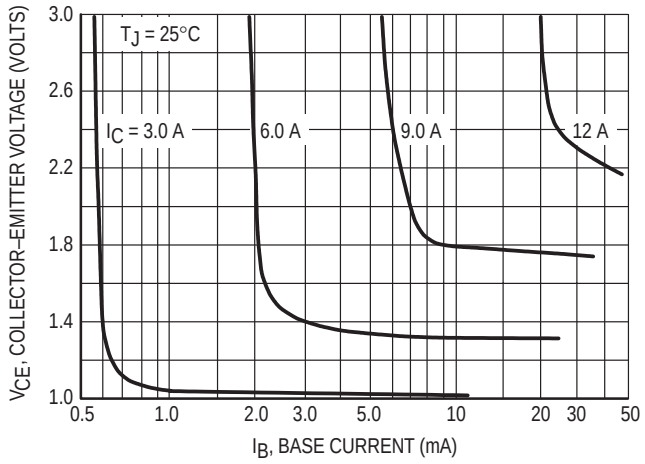


Figure 10. DC Current Gain



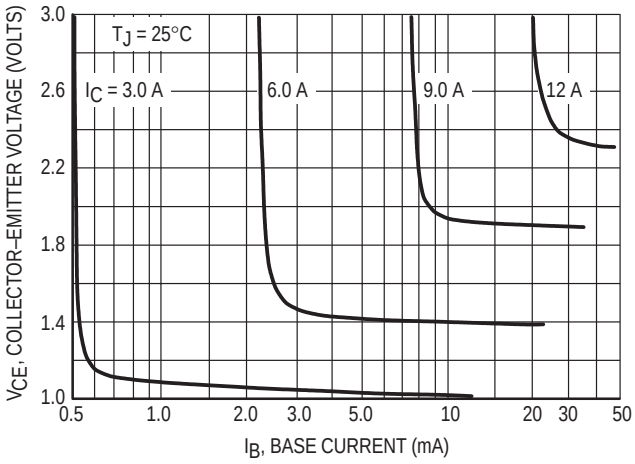
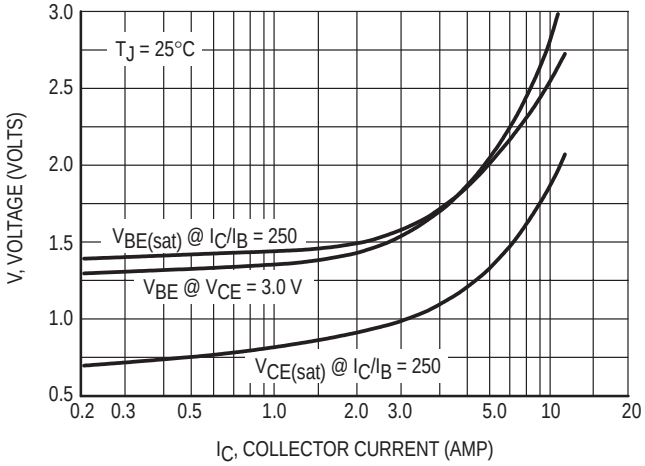


Figure 11. Collector Saturation Region



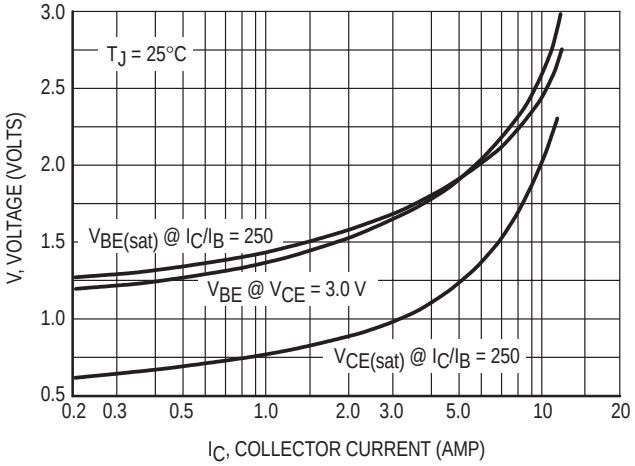


Figure 12. “On” Voltages

Darlington Complementary Silicon Power Transistors

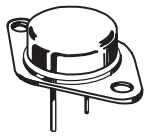
NPN
2N6055
2N6056*

*Motorola Preferred Device

. . . designed for general–purpose amplifier and low frequency switching applications.

- High DC Current Gain —
  h_{FE} = 3000 (Typ) @ I_C = 4.0 Adc
- Collector–Emitter Sustaining Voltage — @ 100 mA
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6055
  = 80 Vdc (Min) — 2N6056
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 4.0 Adc
  = 3.0 Vdc (Max) @ I_C = 8.0 Adc
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors

DARLINGTON
8 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60 – 80 VOLTS
100 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (1)

Rating	Symbol	2N6055	2N6056	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	8.0 16		Adc
Base Current	I_B	120		mAdc
		2N6055 **2N6056**		
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.571		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	2N6055 2N6056	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	°C/W

(1) Indicates JEDEC Registered Data

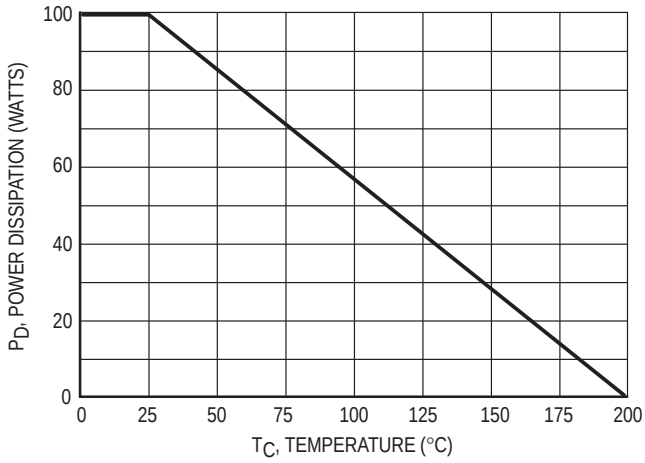


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

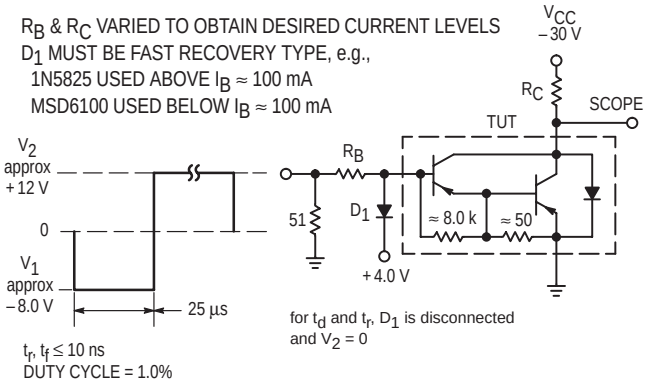
REV 1

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	2N6055 2N6056	$V_{CEO(sus)}$	 60 80	 — —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	 2N6055 2N6056	I_{CEO}	 — —	 0.5 0.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	 — —	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	 750 100	 18000 —	—
Collector–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 16 mAdc) (I_C = 8.0 Adc, I_B = 80 mAdc)		$V_{CE(sat)}$	 — —	 2.0 3.0	Vdc
Base–Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 80 mAdc)		$V_{BE(sat)}$	—	4.0	Vdc
Base–Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small–Signal Short Circuit Current Transfer Ratio (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6055, 2N6056	C_{ob}	—	200	pF
Small–Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	—	—

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%



For NPN test circuit reverse diode, polarities and input pulses.

Figure 2. Switching Times Test Circuit

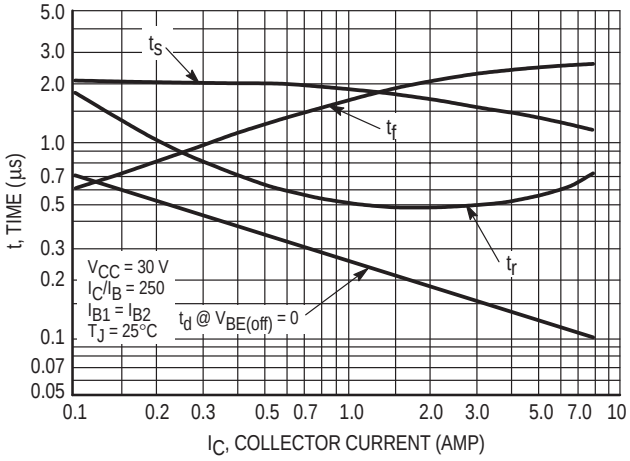


Figure 3. Switching Times

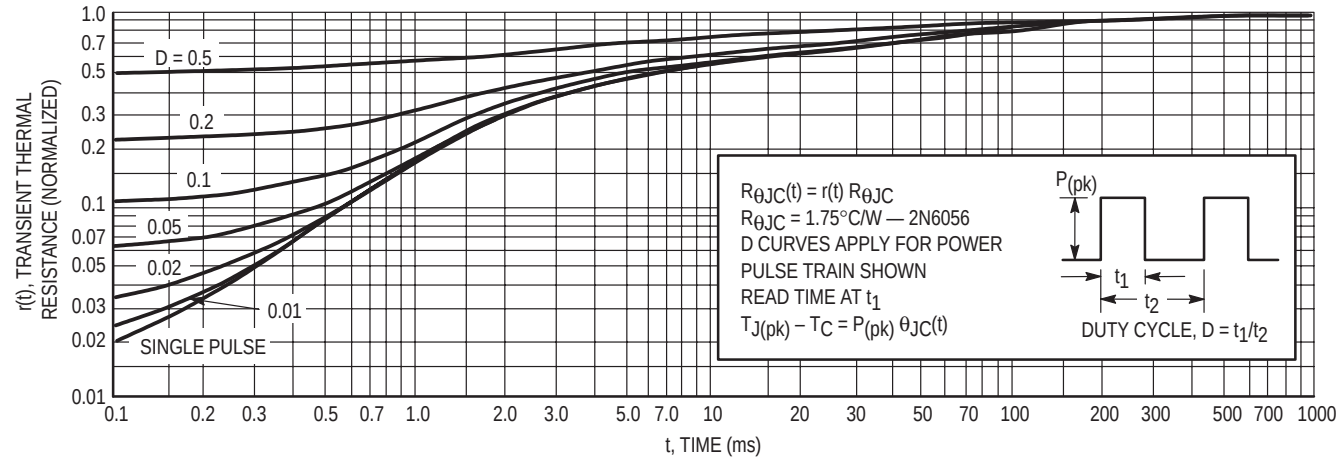


Figure 4. Thermal Response

ACTIVE–REGION SAFE OPERATING AREA

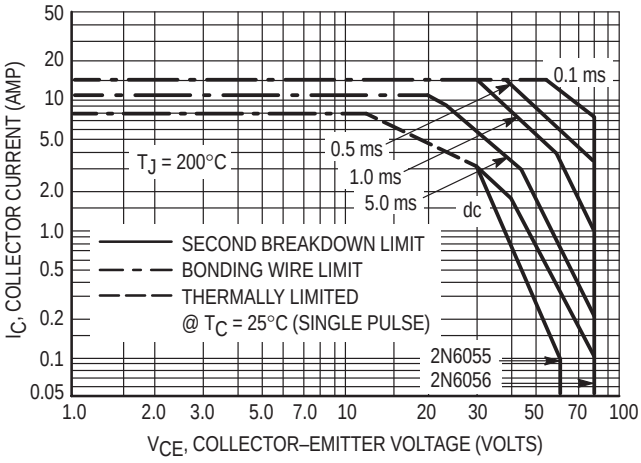


Figure 5. 2N6055 and 2N6056

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200 °C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

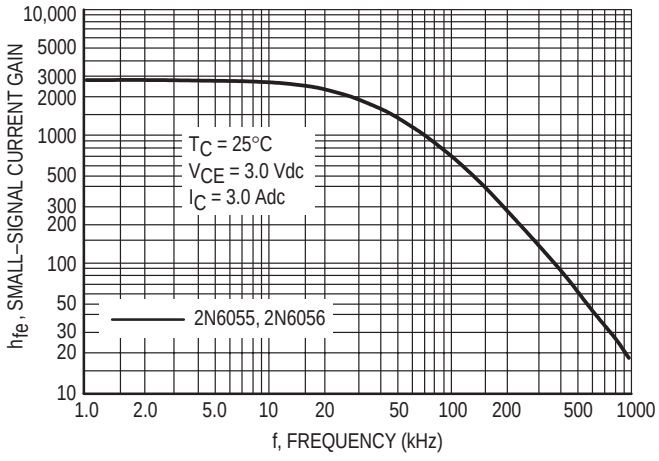


Figure 6. Small–Signal Current Gain

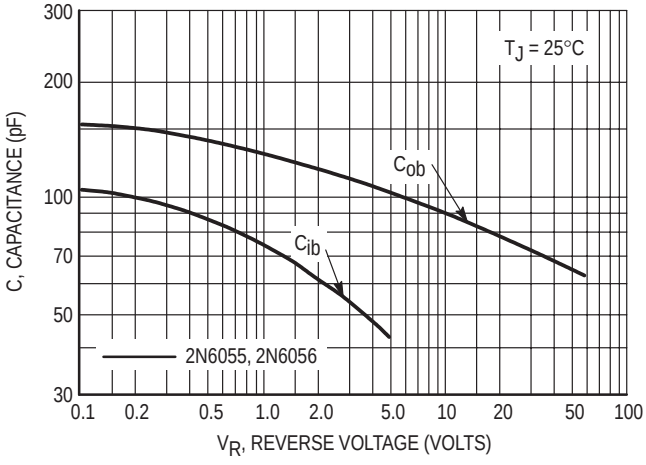


Figure 7. Capacitance

NPN
2N6055, 2N6056

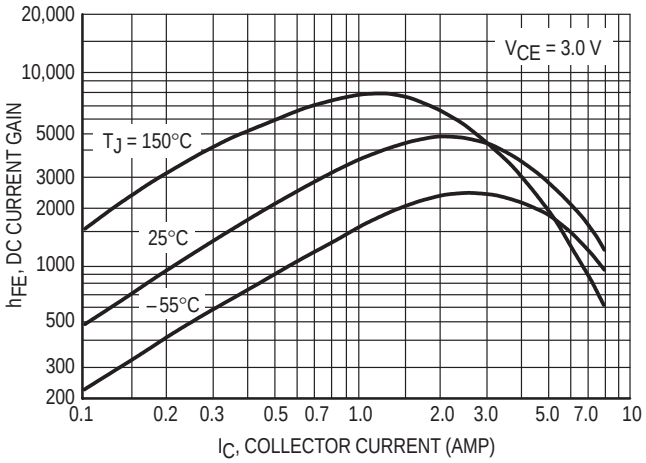


Figure 8. DC Current Gain

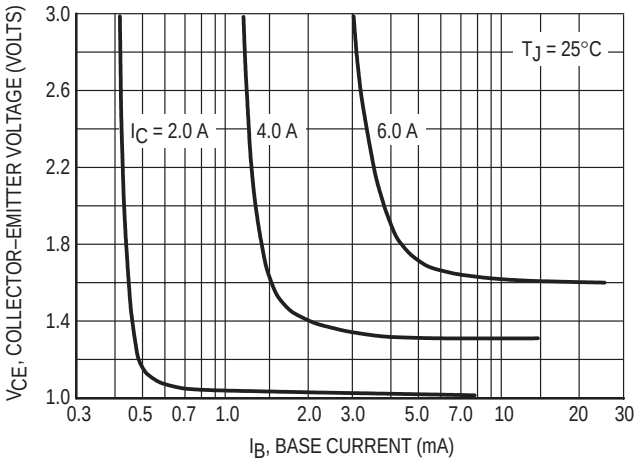


Figure 9. Collector Saturation Region

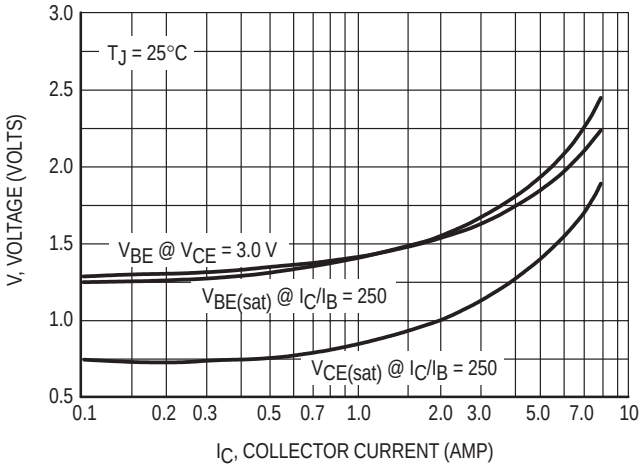


Figure 10. “On” Voltages

2N6057 thru 2N6059
(See 2N6050)

Complementary Silicon Plastic Power Transistors

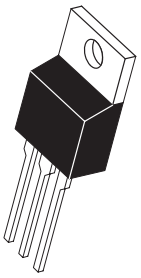
. . . designed for use in general–purpose amplifier and switching applications.

- DC Current Gain Specified to 7.0 Amperes
  h_{FE} = 30–150 @ I_C = 3.0 Adc — 2N6111, 2N6288
  = 2.3 (Min) @ I_C = 7.0 Adc — All Devices
- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 30 Vdc (Min) — 2N6111, 2N6288
  = 50 Vdc (Min) — 2N6109
  = 70 Vdc (Min) — 2N6107, 2N6292
- High Current Gain — Bandwidth Product
  f_T = 4.0 MHz (Min) @ I_C = 500 mAdc — 2N6288, 90, 92
  = 10 MHz (Min) @ I_C = 500 mAdc — 2N6107, 09, 11
- TO–220AB Compact Package

PNP
2N6107
2N6109*
2N6111
NPN
2N6288
2N6292*

***Motorola Preferred Device**

7 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
30 – 50 – 70 VOLTS
40 WATTS



CASE 221A–06
TO–220AB

***MAXIMUM RATINGS**

Rating	Symbol	2N6111 2N6288	2N6109	2N6107 2N6292	Unit
Collector–Emitter Voltage	V_{CEO}	30	50	70	Vdc
Collector–Base Voltage	V_{CB}	40	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	7.0 10			Adc
Base Current	I_B	3.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W

* Indicates JEDEC Registered Data.

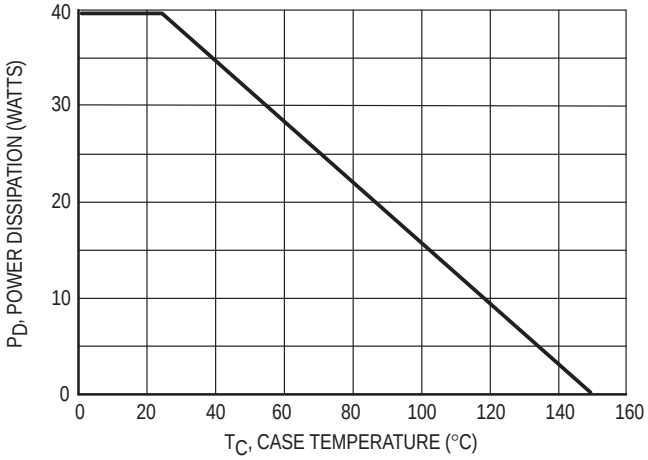


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N6111, 2N6288		30	—	
	2N6109		50	—	
	2N6107, 2N6292		70	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N6111, 2N6288		—	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	2N6109		—	1.0	
(V_{CE} = 60 Vdc, I_B = 0)	2N6107, 2N6292		—	1.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 40 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6111, 2N6288		—	100	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6109		—	100	
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6107, 2N6292		—	100	
(V_{CE} = 30 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6111, 2N6288		—	2.0	mAdc
(V_{CE} = 50 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6109		—	2.0	
(V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	2N6107, 2N6292		—	2.0	
Emitter Cutoff Current		I_{EBO}	—	1.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)	2N6107, 2N6292		30	150	
(I_C = 2.5 Adc, V_{CE} = 4.0 Vdc)	2N6109		30	150	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)	2N6111, 2N6288		30	150	
(I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)	All Devices		2.3	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$	—	3.5	Vdc
(I_C = 7.0 Adc, I_B = 3.0 Adc)					
Base–Emitter On Voltage		$V_{BE(on)}$	—	3.0	Vdc
(I_C = 7.0 Adc, V_{CE} = 4.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2)		f_T			MHz
(I_C = 500 mAdc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 MHz)	2N6288, 92		4.0	—	
	2N6107, 09, 11		10	—	
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	—	250	pF
Small–Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4.0 Vdc, f = 50 kHz)		h_{fe}	20	—	—

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.

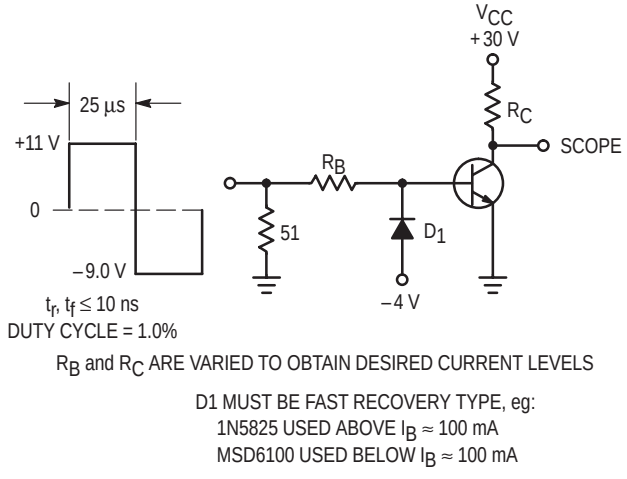


Figure 2. Switching Time Test Circuit

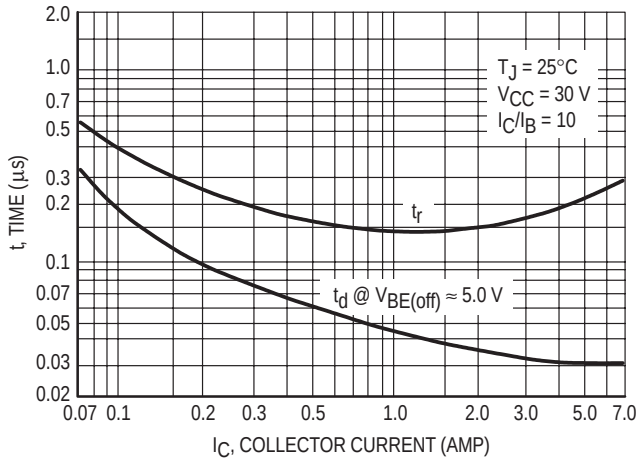


Figure 3. Turn–On Time

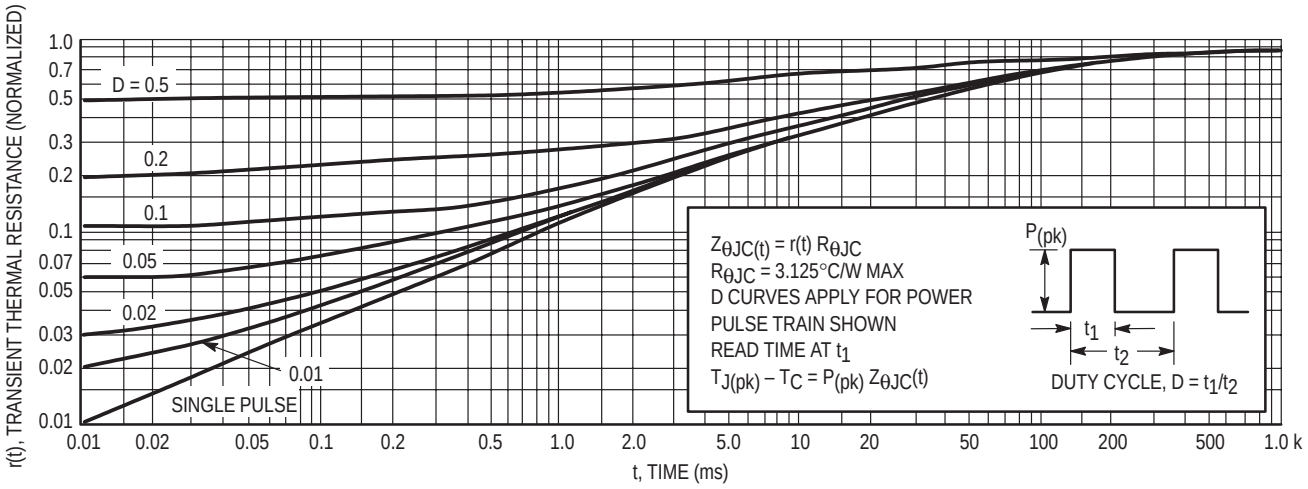


Figure 4. Thermal Response

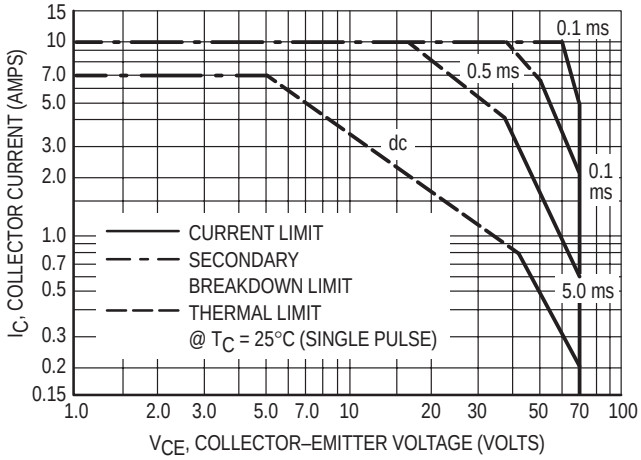


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

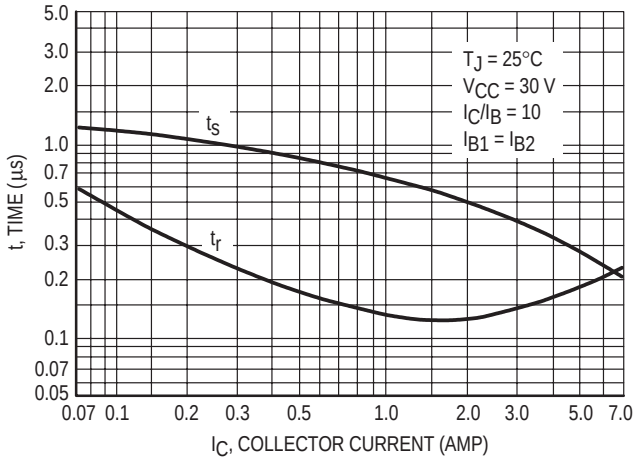


Figure 6. Turn–Off Time

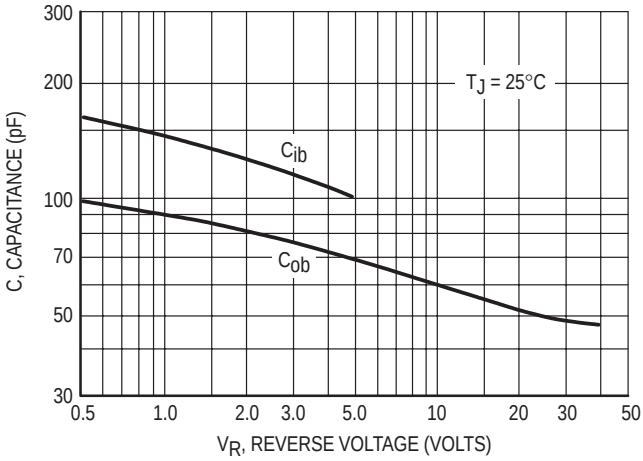


Figure 7. Capacitance

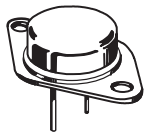
2N6251

High Voltage NPN Silicon Power Transistors

15 AMPERE
POWER TRANSISTOR
NPN SILICON
350 VOLTS
175 WATTS

. . . designed for high voltage inverters, switching regulators and line operated amplifier applications. Especially well suited for switching power supply applications.

- High Voltage Breakdown Rating
- Low Saturation Voltages
- Fast Switching Capability
- High $E_{S/b}$ Energy Handling Capability



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage (1)	$V_{CEO(sus)}$	350	Vdc
Collector–Emitter Voltage (1)	$V_{CER(sus)}$	375	Vdc
Collector–Base Voltage (1)	V_{CB}	450	Vdc
Emitter–Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous** — Peak	I_C I_{CM}	15 30	Adc
Base Current — Continuous (1) — Peak	I_B I_{BM}	10 20	Adc
Emitter Current — Continuous — Peak	I_E I_{EM}	25 50	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C*	P_D	175 100 1.0	Watts W/°C
Operating and Storage Junction (1) Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8” from Case for 5 Seconds	T_L	275	°C

(1) Indicates JEDEC Registered Data.
** JEDEC Registered Value is 10 A, Motorola Guaranteed Value is 15 A.

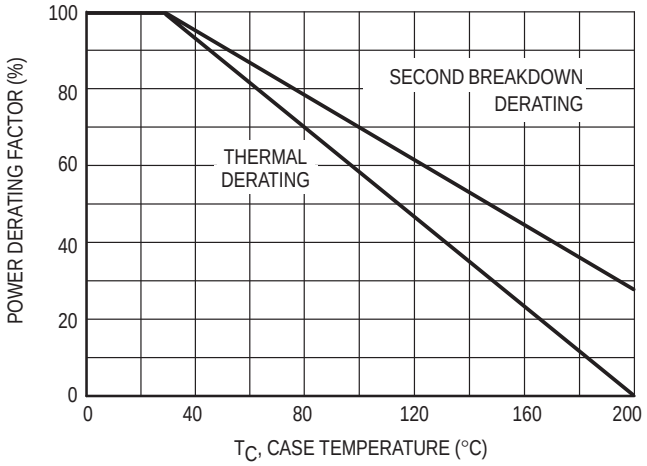


Figure 1. Power Derating

REV 1

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 200 mA, I_B = 0)		$V_{CEO(sus)}$	350	—	Vdc
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 200 mA)		$V_{CER(sus)}$	375	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CER}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CER}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)		I_{CEV}	 — —	 5.0 10	mAdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 225 Vdc, I_B = 0) (V_{CE} = 300 Vdc, I_B = 0)		I_{CEO}	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased t = 1.0s (non–repetitive)	(V_{CE} = 30 V) (V_{CE} = 100 V)	$I_{S/b}$	5.8 0.3	— —	Vdc
Second Breakdown Energy with base reverse biased (Table 1) (I_C = 10 A, $V_{BE(off)}$ = 4.0 Vdc, L = 50 μH)		$E_{S/b}$	2.5	—	mJ
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	6.0	50	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.67 Adc)		$V_{CE(sat)}$	—	1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 1.25 Adc) (I_C = 10 Adc, I_B = 1.67 Adc)		$V_{BE(sat)}$	—	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	2.5	—	MHz
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Rise Time	(V_{CC} = 200 Vdc, I_C = 10 A, Duty Cycle ≤ 2.0%, t_p = 100 μs) (I_{B1} = I_{B2} = 1.67 Adc)	t_r	—	2.0	μs
Storage Time		t_s	—	3.5	μs
Fall Time		t_f	—	1.0	μs

* Indicates JEDEC Registered Data.

(1) Measured on a curve tracer (60 Hz full–wave rectified sine wave).

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	$V_{CER(sus)}$	$E_{S/b}$	RESISTIVE SWITCHING
INPUT CONDITIONS	+6.0 V, 0, 39, 1, 2	+6.0 V, 0, 39, 51, 1, 2	I_{B1} = 2.0 A, +10 V, 0, 50, 1, 50, 4 V, 2	+ 15 V, 50 µF, TIP41B, 51, 51, 4.7, 0.02 µF, 1, 2
CIRCUIT VALUES	L_{coil} = 42 mH R_{coil} = 0.7 Ω, f_o = 60 Hz V_{CC} = 0 to 50 V	L_{coil} = 14 mH R_{coil} = 0.05 Ω V_{CC} = 0 to 50 V f_o = 60 Hz	L_{coil} = 50 µH, V_{CC} = 11.5 V R_{coil} = 0.2 Ω	I_C = 10 A PW ≈ 100 µs $t_r \le$ 5 ns $t_f \le$ 50 ns DUTY CYCLE ≤ 2% V_{CC} = 200 V R_L = 20 Ω
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT: TUT, 1, 2, 1N4937, R_{coil}, L_{coil}, V_{CL}, R_S, 0.1, V_{CC} OUTPUT WAVEFORMS: I_C, $I_{C(pk)}$, t, t_1, t_f, V_{CE}, t t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$			RESISTIVE TEST CIRCUIT: + 200 V, 20, DC CURRENT PROBE, 1, TUT, 3, 2, 25, – 6.0 V

NOTE: SET $I_{C(pk)}$ TO OBTAIN I_C = 200 mA AT $V_{CEO(sus)}$ EQUAL TO RATED VALUE.
ADJUST V_{Clamp} VOLTAGE FOR $V_{CEO(sus)}$ RATED VALUE.

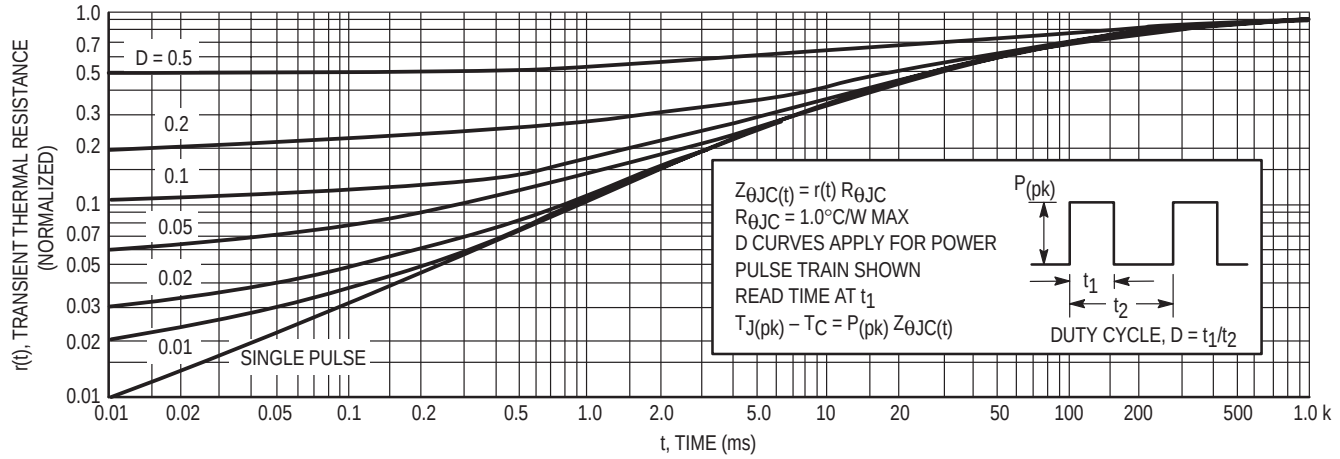


Figure 2. Thermal Response

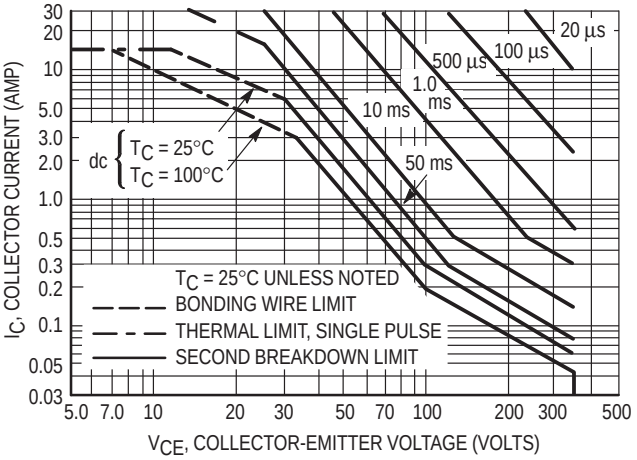


Figure 3. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on T_C = 25°C. $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltage shown on Figure 3 may be found at any case temperature by using the appropriate curve on Figure 1.

$T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

DC CHARACTERISTICS

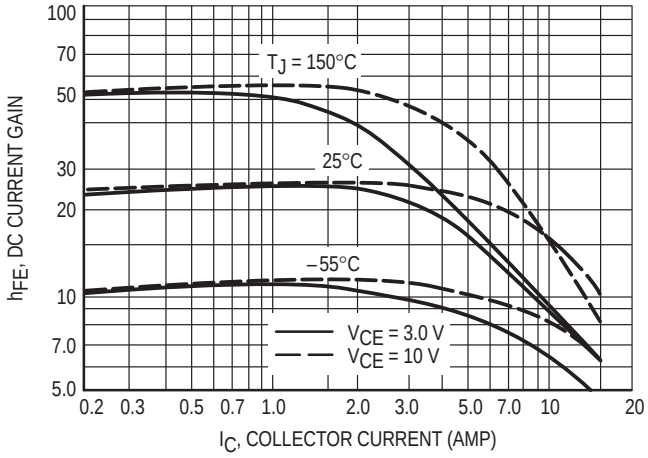


Figure 4. DC Current Gain

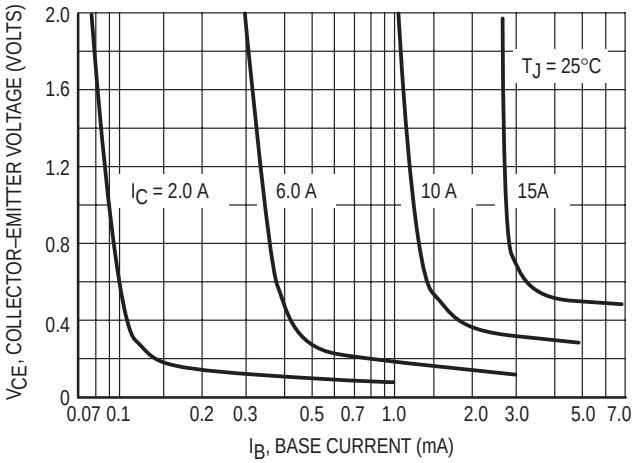


Figure 5. Collector Saturation Region

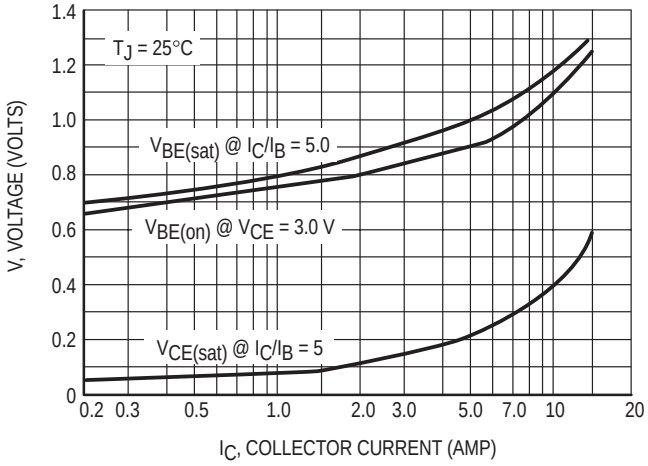


Figure 6. "On" Voltagae

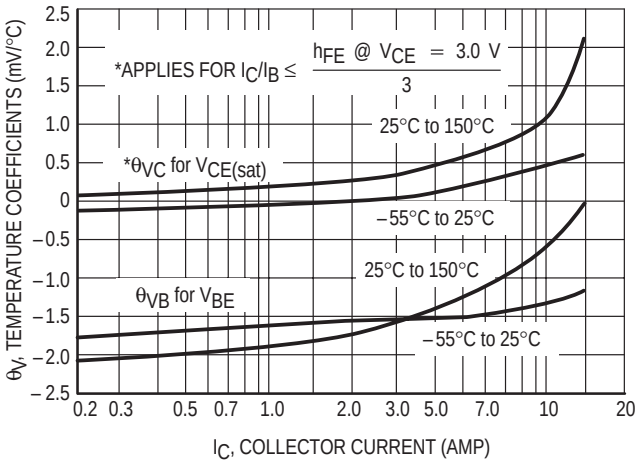


Figure 7. Temperature Coefficients

RESISTIVE SWITCHING PERFORMANCE

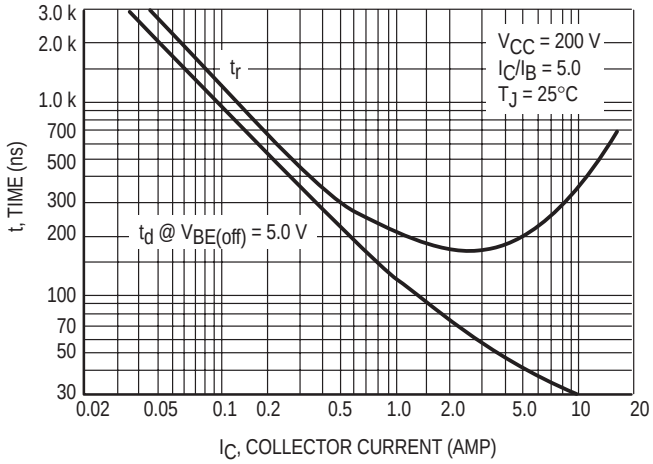


Figure 8. Turn-on Time

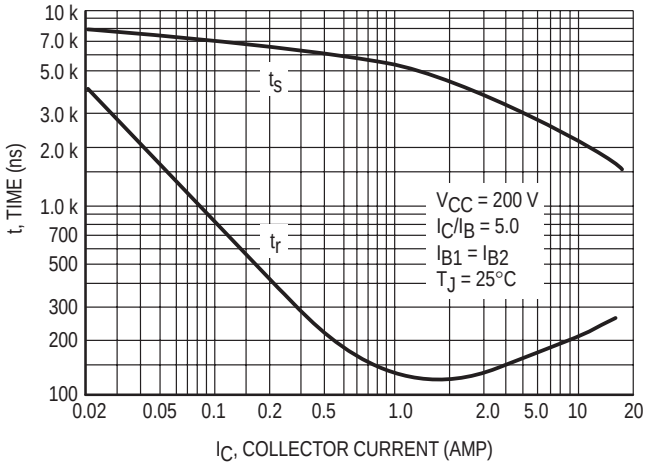


Figure 9. Turn-off Time

High-Power NPN Silicon Transistors

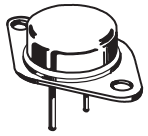
2N6274
2N6275
2N6277*

*Motorola Preferred Device

. . . designed for use in industrial–military power amplifer and switching circuit applications.

- High Collector Emitter Sustaining —
  $V_{CEO(sus)}$ = 100 Vdc (Min) — 2N6274
  = 120 Vdc (Min) — 2N6275
  = 150 Vdc (Min) — 2N6277
- High DC Current Gain —
  h_{FE} = 30–120 @ I_C = 20 Adc
  = 10 (Min) @ I_C = 50 Adc
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 20 Adc
- Fast Switching Times @ I_C 20 Adc
  t_r = 0.35 µs (Max)
  t_S = 0.8 µs (Max)
  t_f = 0.25 µs (Max)
- Complement to 2N6377–79

50 AMPERE
POWER TRANSISTORS
NPN SILICON
100, 120, 140, 150 VOLTS
250 WATTS



CASE 197A–05
TO–204AE
(TO–3)

MAXIMUM RATINGS(1)

Rating	Symbol	2N6274	2N6275	2N6277	Unit
Collector–Base Voltage	V_{CB}	120	140	180	Vdc
Collector–Emitter Voltage	V_{CEO}	100	120	150	Vdc
Emitter–Base Voltage	V_{EB}	6.0			Vdc
Collector Current — Continuous Peak	I_C	50 100			Adc
Base Current	I_B	20			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200			°C

THERMAL CHARACTERISTIC

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

(1) Indicates JEDEC Registered Data.

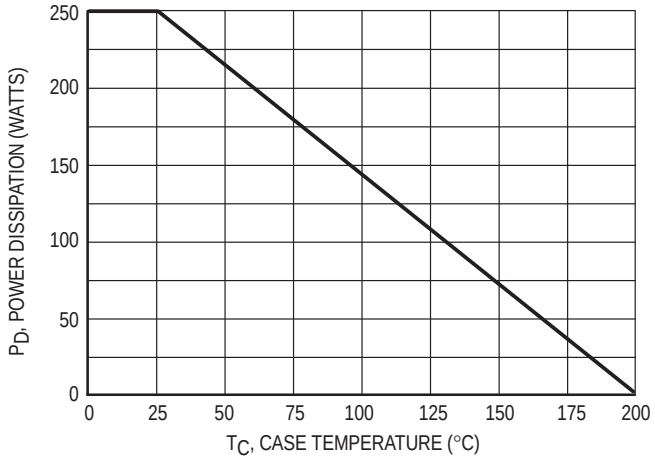


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

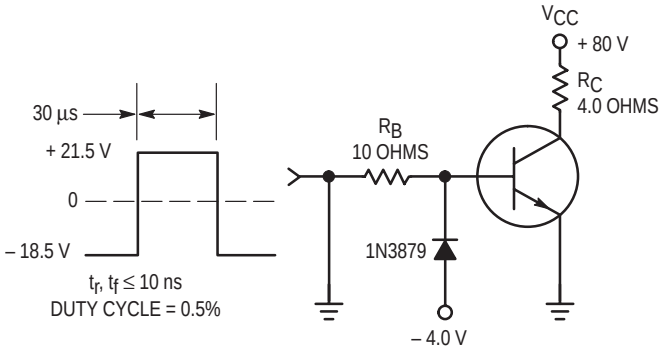
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
I_C = 50 mAdc, I_B = 0)	2N6274		100	—	
	2N6275		120	—	
	2N6277		150	—	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N6274		—	50	
(V_{CE} = 60 Vdc, I_B = 0)	2N6275		—	50	
(V_{CE} = 75 Vdc, I_B = 0)	2N6277		—	50	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc)			—	10	μAdc
(V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)			—	1.0	mAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	100	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			50	—	
I_C = 20 Adc, V_{CE} = 4.0 Vdc)			30	120	
I_C = 50 Adc, V_{CE} = 4.0 Vdc)			10	—	
Coliector–Emitter Saturation Voltage		V_{CE} (sat)			Vdc
I_C = 20 Adc, I_B = 2.0 Adc)			—	1.0	
I_C = 50 Adc, I_B = 10 Adc)			—	3.0	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
I_C = 20 Adc, I_B = 2.0 Adc)			—	1.8	
I_C = 50 Adc, I_B = 10 Adc)			—	3.5	
Base–Emitter On Voltage (I_C = 20 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	30	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	600	pF
SWITCHING CHARACTERISTICS					
Rise Time		t_r	—	0.35	μs
(V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = 2.0 Adc, $V_{BE(off)}$ = 5.0 Vdc)					
Storage Time		t_s	—	0.80	μs
(V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)					
Fall Time		t_f	—	0.25	μs
(V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)					

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$



NOTE: For information of Figures 3 and 6 , R_B and R_C were varied to obtain desired test conditions.

Figure 2. Switching Time Test Circuit

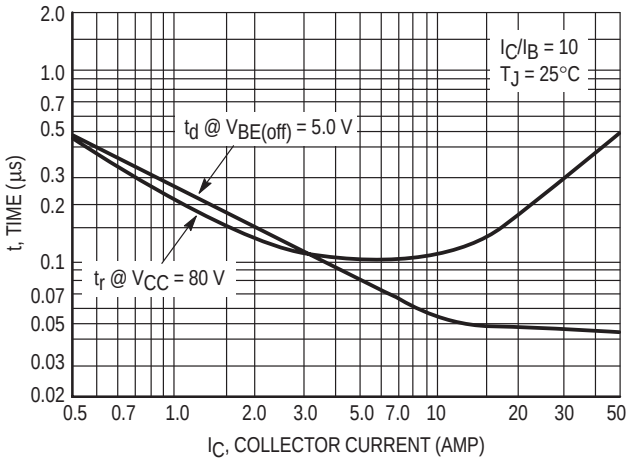


Figure 3. Turn–On Time

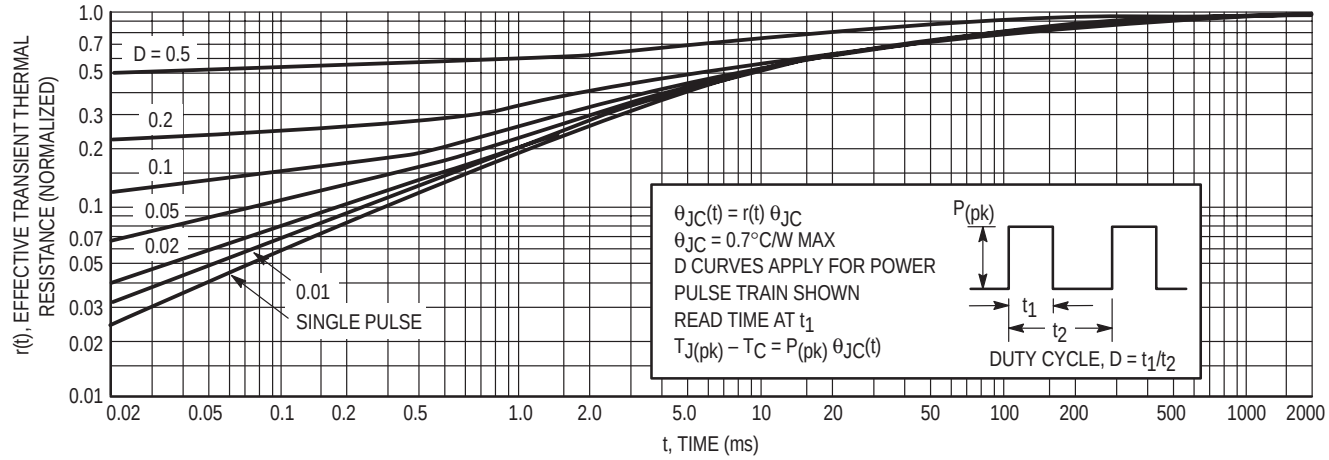


Figure 4. Thermal Response

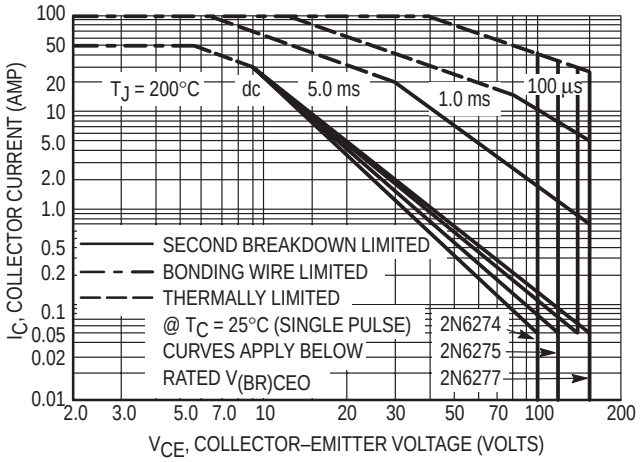


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

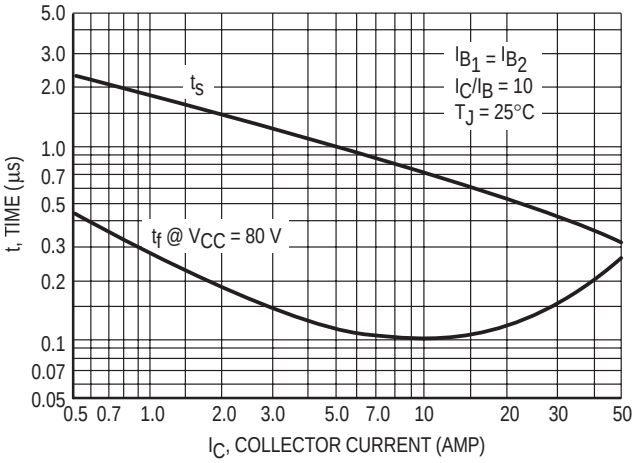


Figure 6. Turn–Off Time

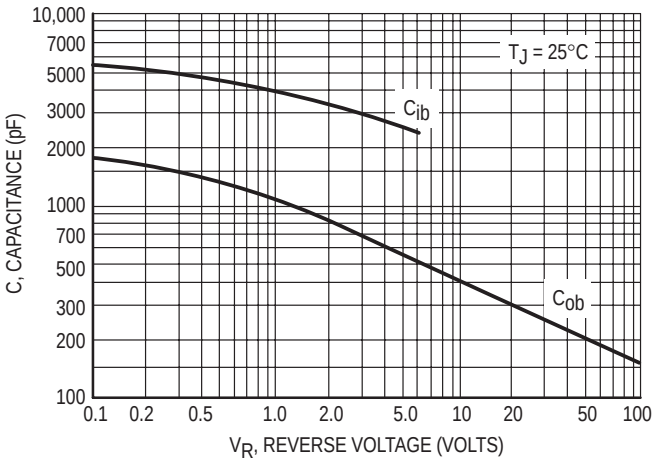


Figure 7. Capacitance

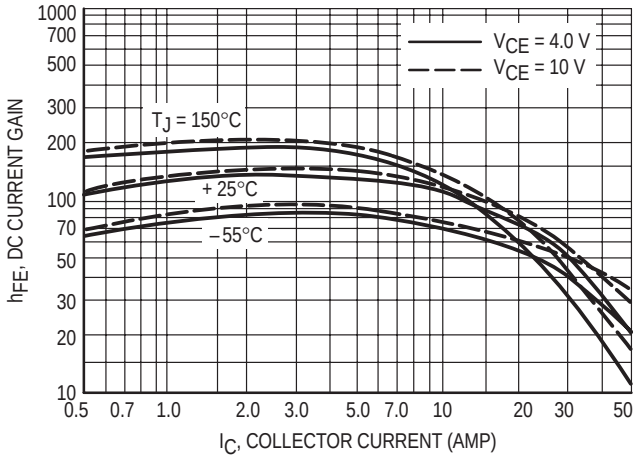


Figure 8. DC Current Gain

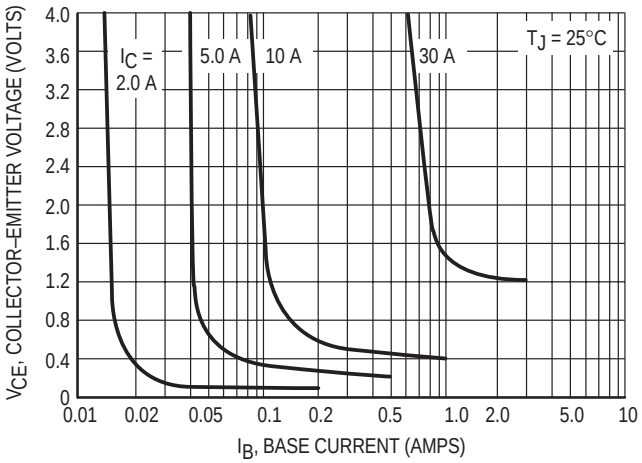


Figure 9. Collector Saturation Region

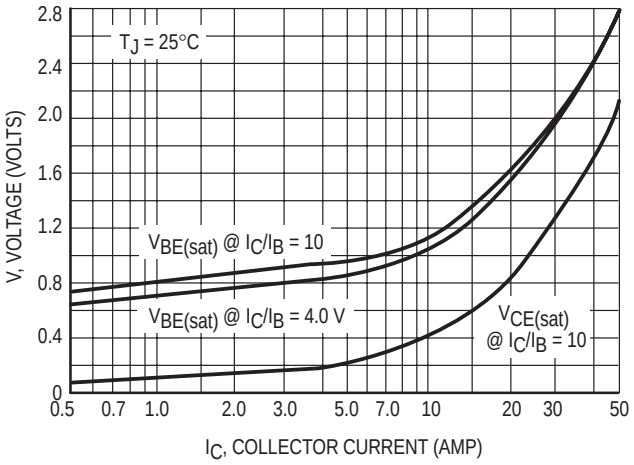


Figure 10. “On” Voltages

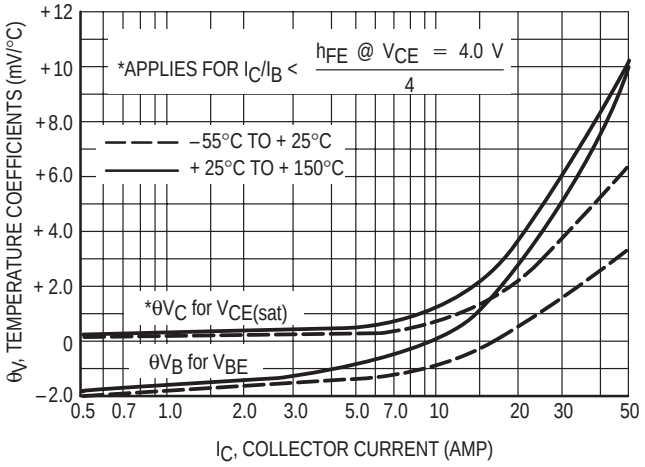


Figure 11. Temperature Coefficients

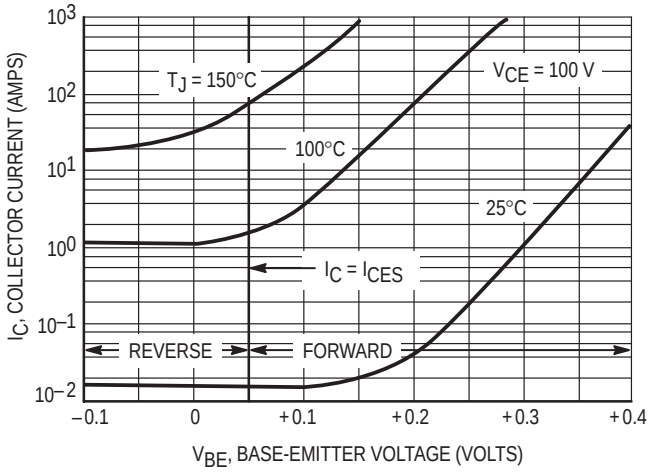


Figure 12. Collector Cut–Off Region

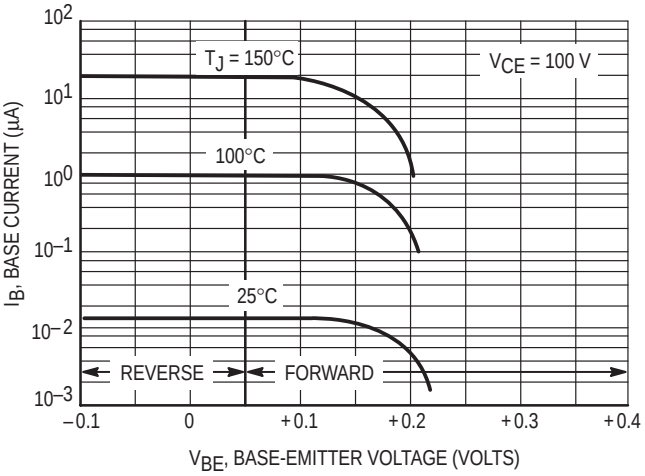


Figure 13. Base Cut–off Region

Darlington Complementary Silicon Power Transistors

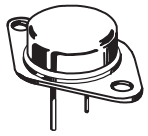
. . . designed for general–purpose amplifier and low–frequency switching applications.

- High DC Current Gain @ I_C = 10 Adc —
  h_{FE} = 2400 (Typ) — 2N6282, 2N6283, 2N6284
  = 4000 (Typ) — 2N6285, 2N6286, 2N6287
- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6282, 2N6285
  = 80 Vdc (Min) — 2N6283, 2N6286
  = 100 Vdc (Min) — 2N6284, 2N6287
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors

NPN
2N6282
thru
2N6284*
PNP
2N6285
thru
2N6287*

***Motorola Preferred Device**

DARLINGTON
20 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60, 80, 100 VOLTS
160 WATTS



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	2N6282 2N6285	2N6283 2N6286	2N6284 2N6287	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	20 40			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	160 0.915			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	–65 to +200			°C

***THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.09	°C/W

* Indicates JEDEC Registered Data.

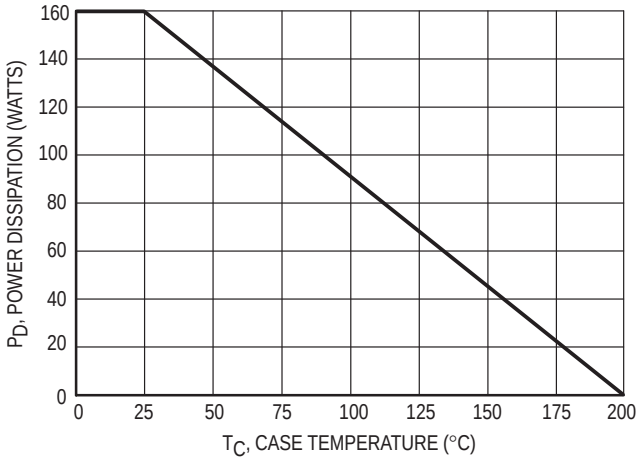


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 0.1 Adc, I_B = 0)	2N6282, 2N6285 2N6283, 2N6286 2N6284, 2N6287	$V_{CEO(sus)}$	 60 80 100	 — — —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	 2N6282, 2N6285 2N6283, 2N6286 2N6284, 2N6287	I_{CEO}	 — — —	 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	 — —	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc) (I_C = 20 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	 750 100	 18,000 —	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 40 mAdc) (I_C = 20 Adc, I_B = 200 mAdc)		$V_{CE(sat)}$	 — —	 2.0 3.0	Vdc
Base–Emitter On Voltage (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
Base–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	—	4.0	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small–Signal Short–Circuit Forward Current Transfer Ratio (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	 2N6282,83,84 2N6285,86,87	C_{ob}	 — —	 400 600	pF
Small–Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	—	—

* Indicates JEDEC Registered Data.

(1) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2%

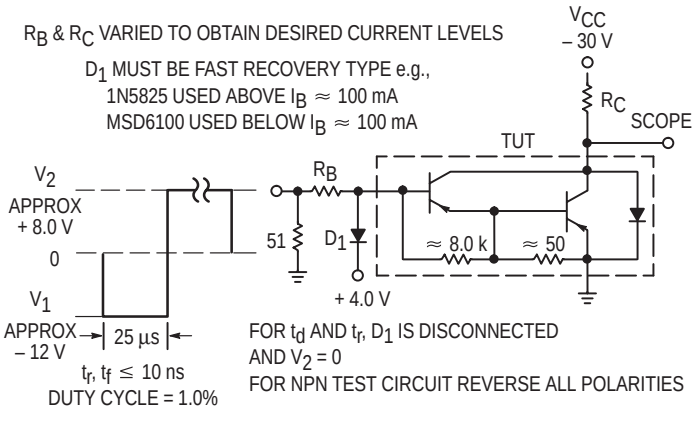


Figure 2. Switching Times Test Circuit

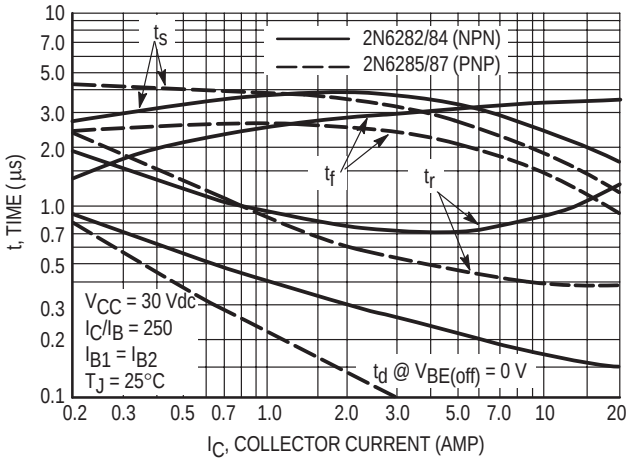


Figure 3. Switching Times

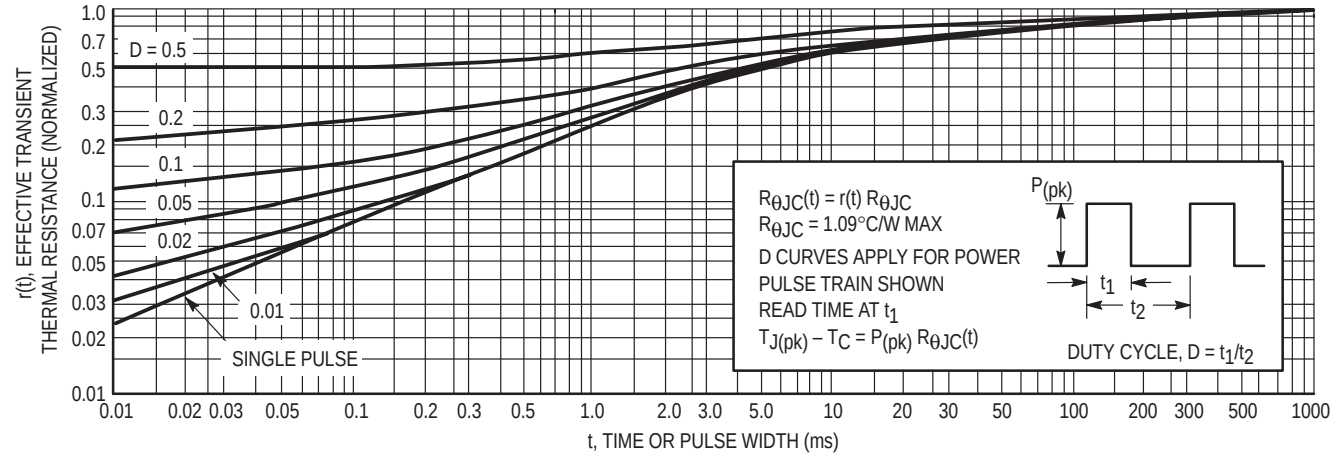


Figure 4. Thermal Response

ACTIVE–REGION SAFE OPERATING AREA

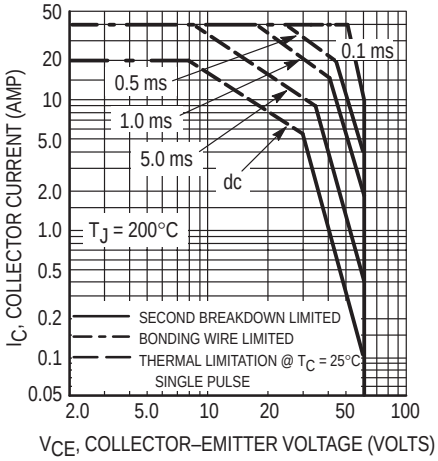


Figure 5. 2N6282, 2N6285

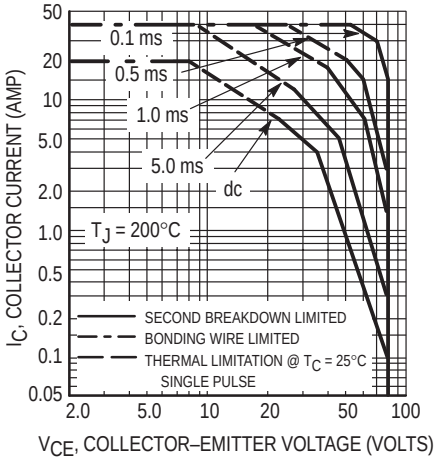


Figure 6. 2N6283, 2N6286

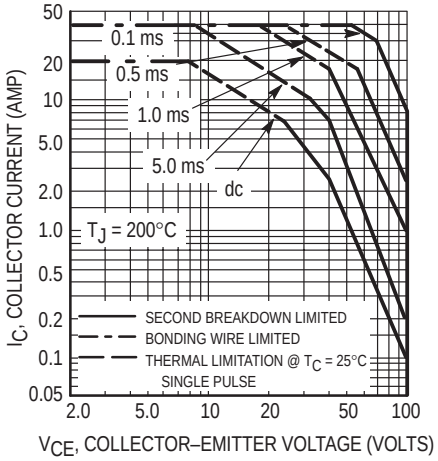


Figure 7. 2N6284, 2N6287

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e. the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6 and 7 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

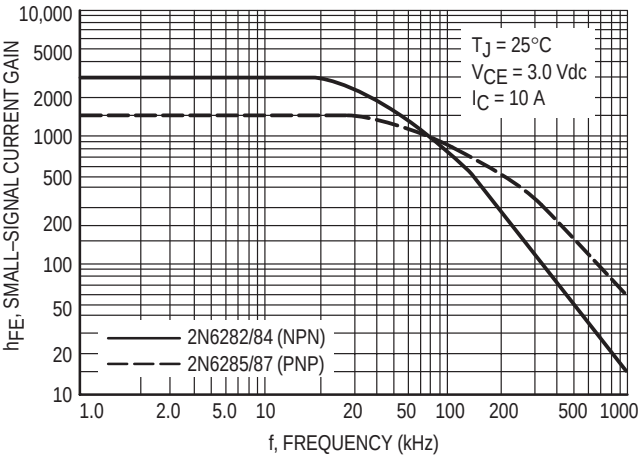


Figure 8. Small–Signal Current Gain

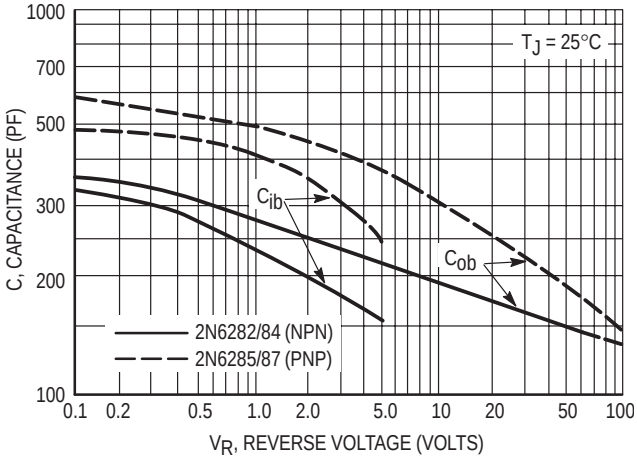
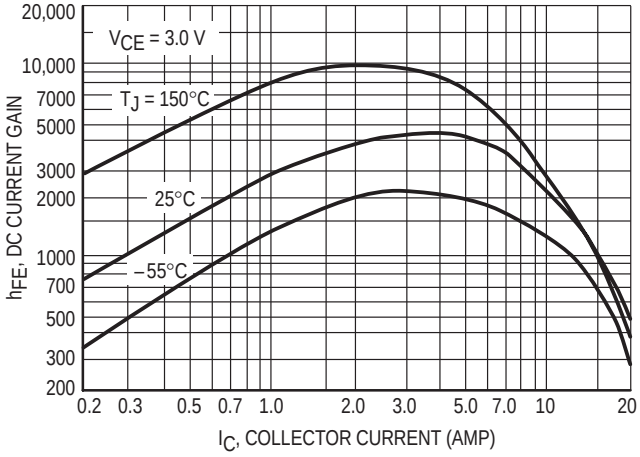


Figure 9. Capacitance

NPN
2N6282, 2N6283, 2N6284



PNP
2N6285, 2N6286, 2N6287

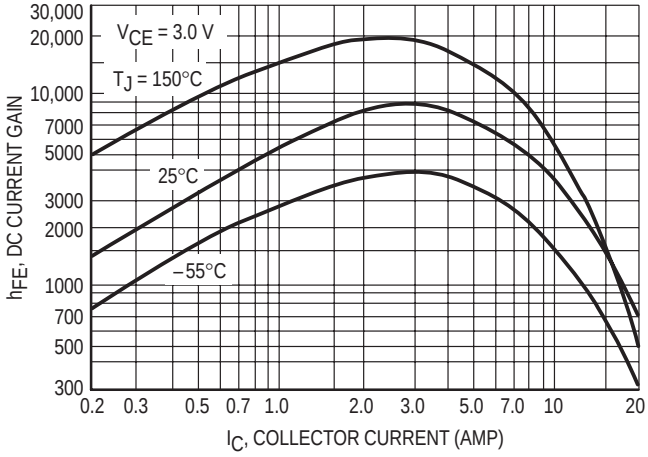
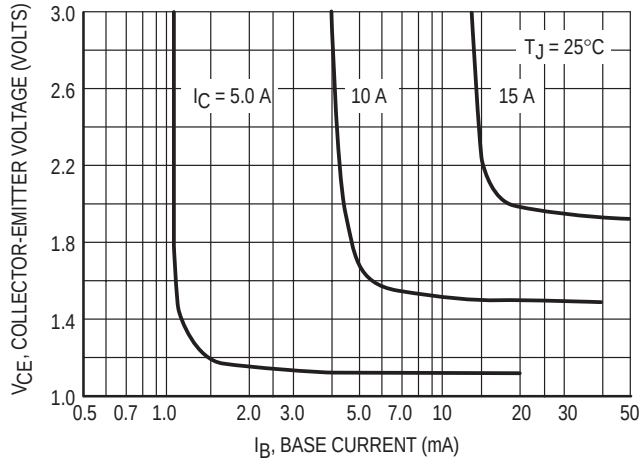


Figure 10. DC Current Gain



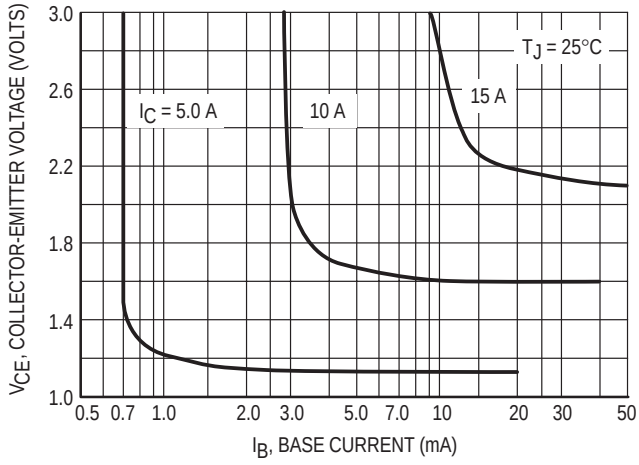
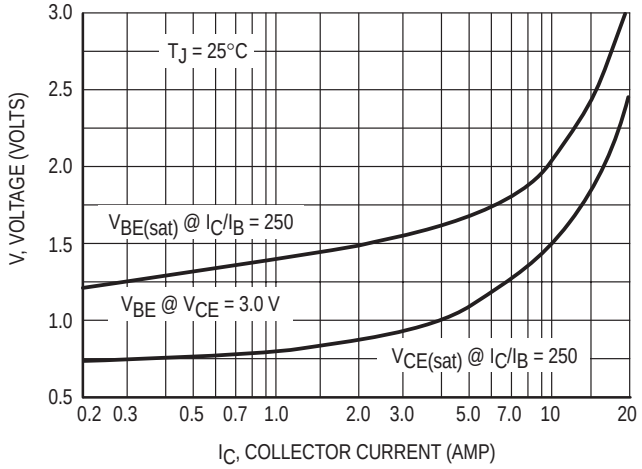


Figure 11. Collector Saturation Region



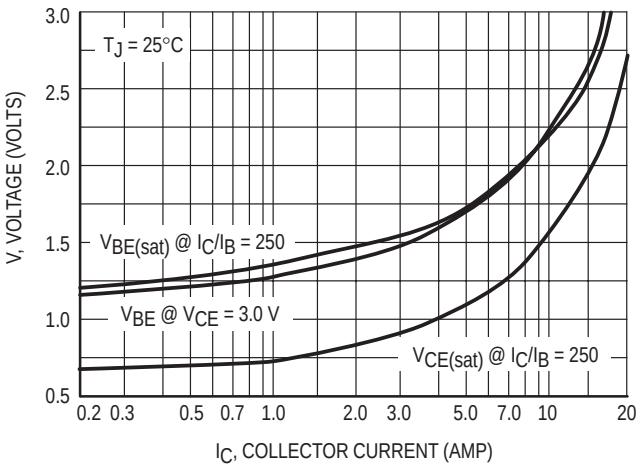
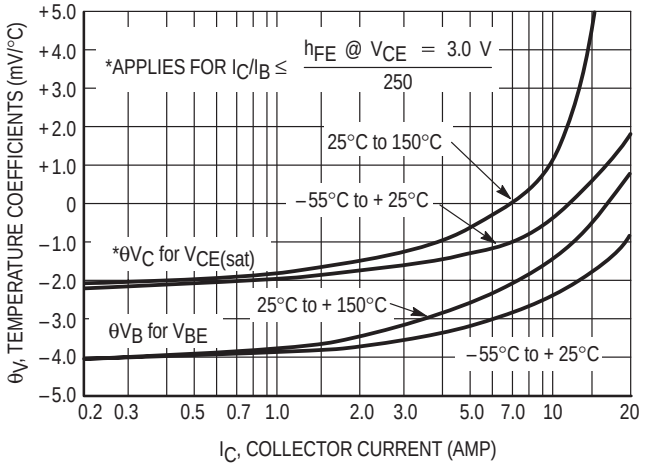


Figure 12. “On” Voltages

NPN
2N6282, 2N6283, 2N6284



PNP
2N6285, 2N6286, 2N6287

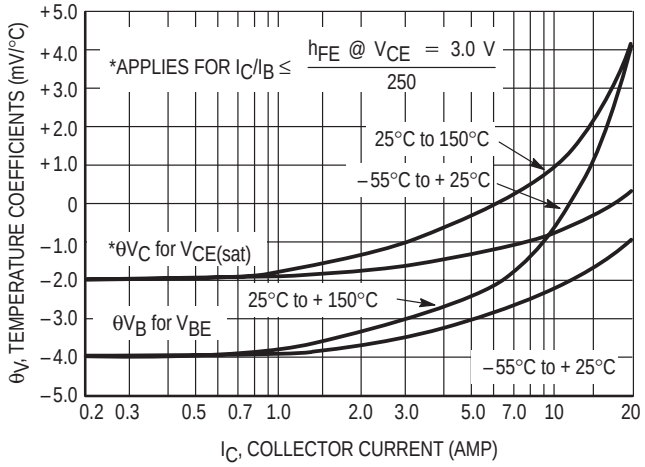
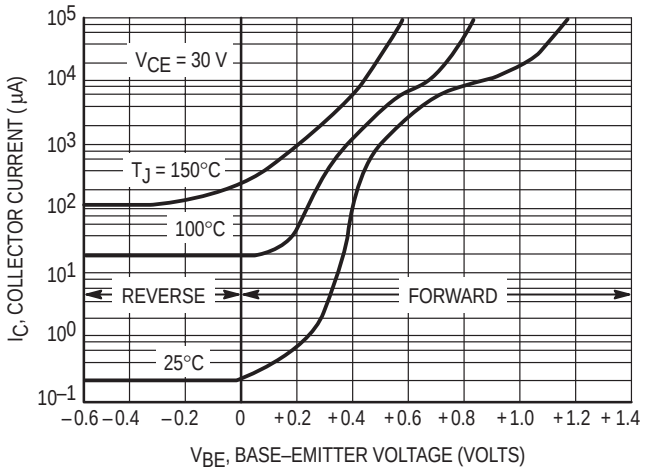


Figure 13. Temperature Coefficients



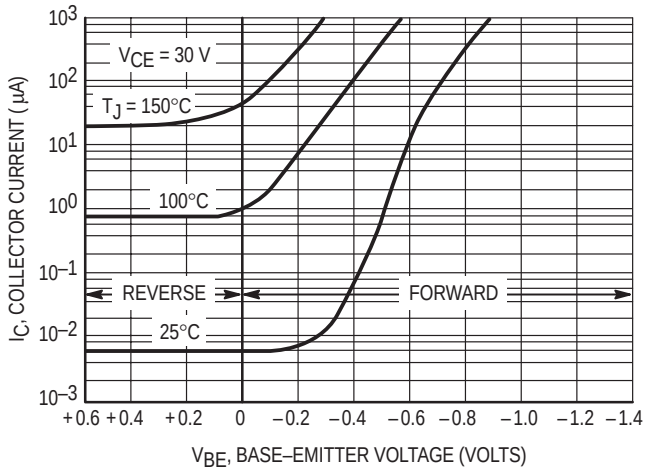
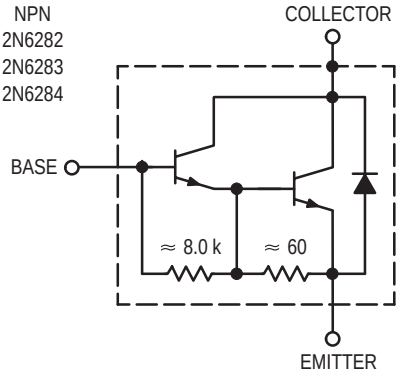


Figure 14. Collector Cut–Off Region



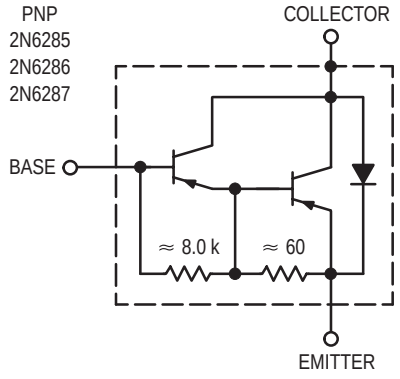


Figure 15. Darlington Schematic

High-Power NPN Silicon Transistors

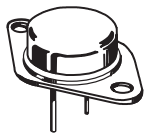
. . . designed for use in industrial–military power amplifier and switching circuit applications.

- High Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 100 Vdc (Min) — 2N6338
  = 120 Vdc (Min) — 2N6339
  = 140 Vdc (Min) — 2N6340
  = 150 Vdc (Min) — 2N6341
- High DC Current Gain —
  h_{FE} = 30 – 120 @ I_C = 10 Adc
  = 12 (Min) @ I_C = 25 Adc
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Fast Switching Times @ I_C = 10 Adc
  t_r = 0.3 μs (Max)
  t_s = 1.0 μs (Max)
  t_f = 0.25 μs (Max)
- Complement to 2N6436–38

2N6338
2N6339
2N6340
2N6341*

***Motorola Preferred Device**

25 AMPERE
POWER TRANSISTORS
NPN SILICON
100, 120, 140, 150 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	2N6338	2N6339	2N6340	2N6341	Unit
Collector–Base Voltage	V_{CB}	120	140	160	180	Vdc
Collector–Emitter Voltage	V_{CEO}	100	120	140	150	Vdc
Emitter–Base Voltage	V_{EB}	6.0				Vdc
Collector Current Continuous Peak	I_C	 25 50				Adc
Base Current	I_B	10				Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 200 1.14				 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

* Indicates JEDEC Registered Data.

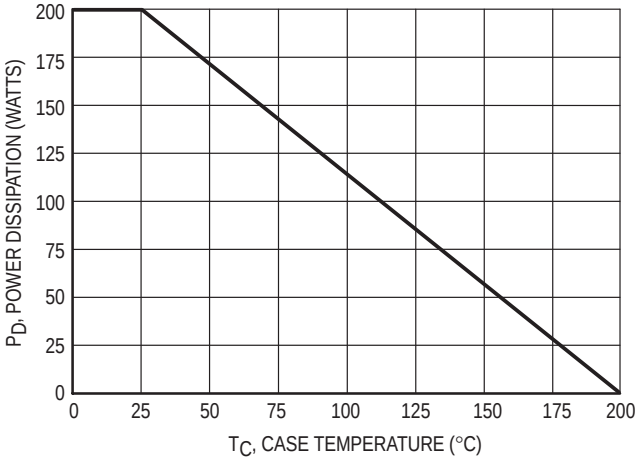


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

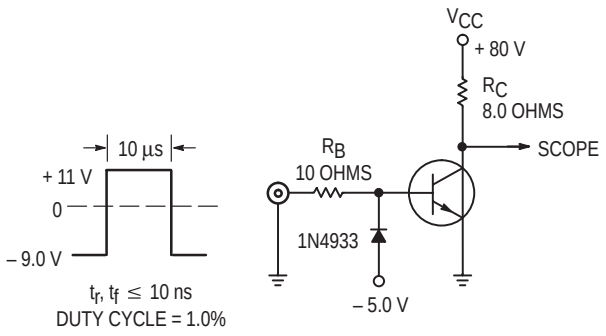
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0)	2N6338	$V_{CEO(sus)}$	100	—	Vdc
	2N6339		120	—	
	2N6340		140	—	
	2N6341		150	—	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 50 Vdc, I_B = 0)	2N6338		—	50	
(V_{CE} = 60 Vdc, I_B = 0)	2N6339		—	50	
(V_{CE} = 70 Vdc, I_B = 0)	2N6340		—	50	
(V_{CE} = 75 Vdc, I_B = 0)	2N6341		—	50	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc)			—	10	μAdc
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)			—	1.0	mAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	100	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain)		h_{FE}			—
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)			50	—	
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)			30	120	
(I_C = 25 Adc, V_{CE} = 2.0 Vdc)			12	—	
Collector Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)			—	1.0	
(I_C = 25 Adc, I_B = 2.5 Adc)			—	1.8	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)			—	1.8	
(I_C = 25 Adc, I_B = 2.5 Adc)			—	2.5	
Base–Emitter On Voltage (I_C = 10 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	40	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	300	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} ≈ 80 Vdc, I_C = 10Adc, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 6.0 Vdc)		t_r	—	0.3	μs
Storage Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)		t_s	—	1.0	μs
Fall Time (V_{CC} ≈ 80 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)		t_f	—	0.25	μs

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.



NOTE: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

Figure 2. Switching Time Test Circuit

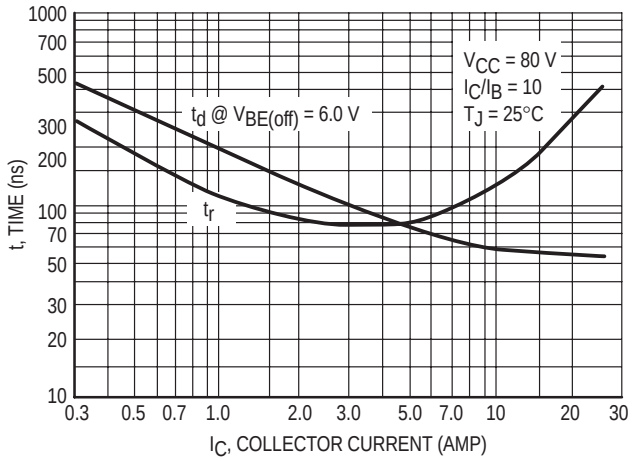


Figure 3. Turn–On Time

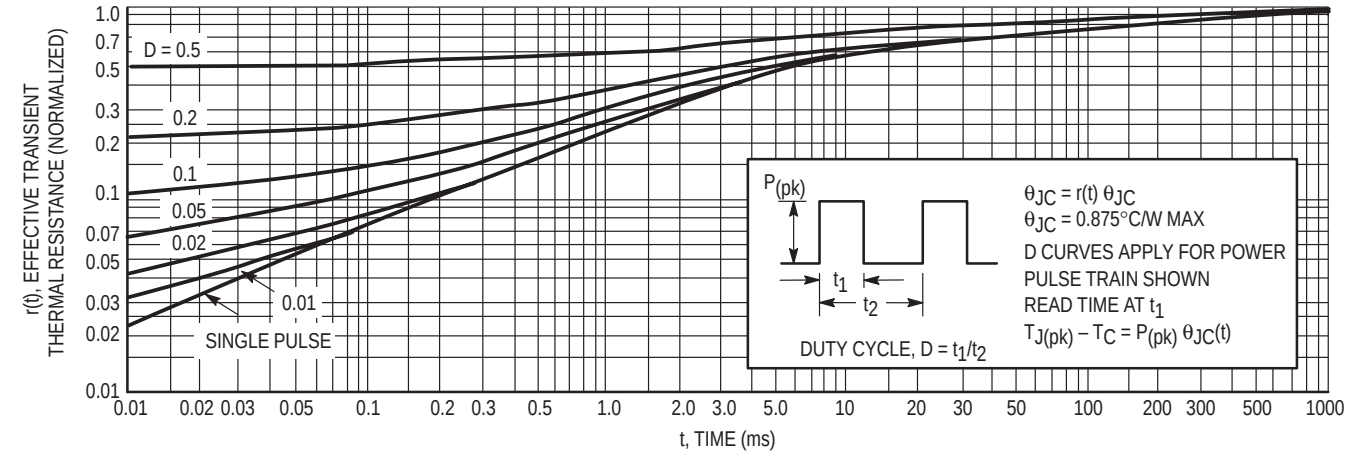


Figure 4. Thermal Response

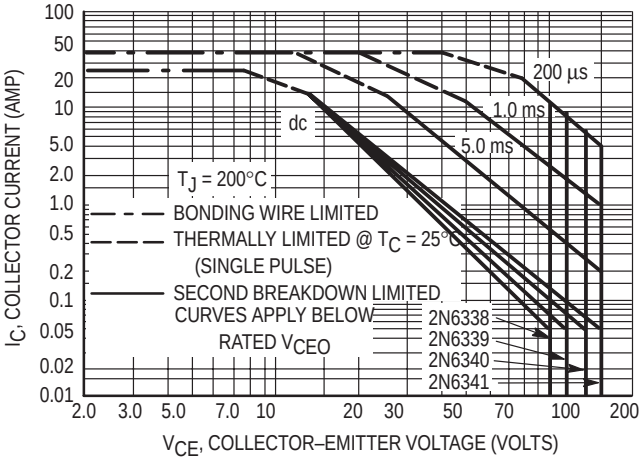


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

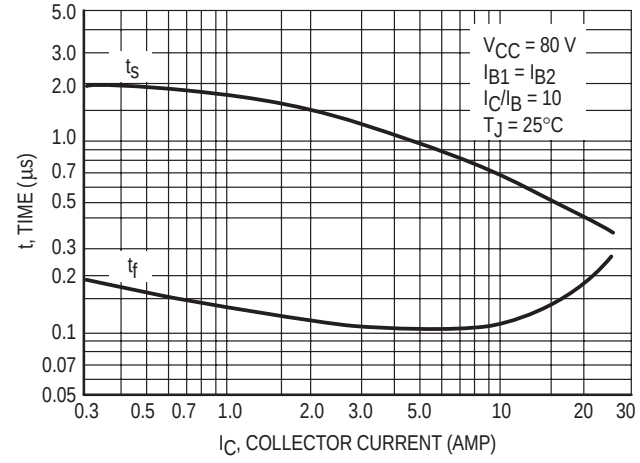


Figure 6. Turn–Off Time

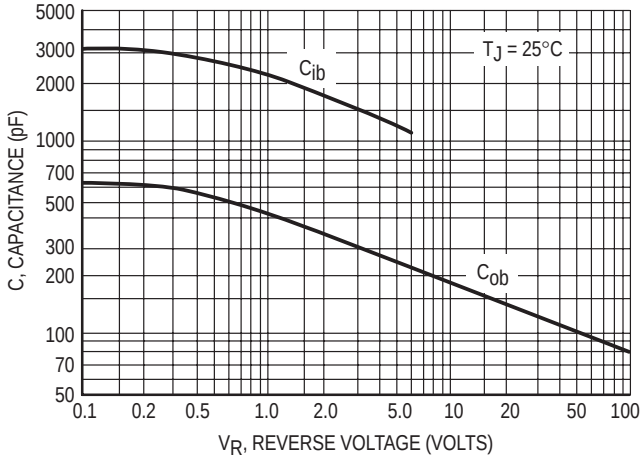


Figure 7. Capacitance

2N6379*

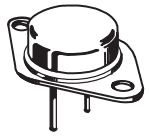
*Motorola Preferred Device

High-Power PNP Silicon Transistors

50 AMPERE
POWER TRANSISTORS
PNP SILICON
80, 100, 120 VOLTS
250 WATTS

. . . designed for use in industrial–military power amplifier and switching circuit applications.

- High Collector Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 120 Vdc (Min) — 2N6379
- High DC Current Gain —
  h_{FE} = 30–120 @ I_C = 20 Adc
  = 10 (Min) @ I_C = 50 Adc
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 20 Adc
- Fast Switching Times @ I_C = 20 Adc
  t_r = 0.35μs (Max)
  t_s = 0.8 μs (Max)
  t_f = 0.25 μs (Max)
- Complement to 2N6274–77



CASE 197A–05
TO–204AE
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CB}	140	Vdc
Collector–Emitter Voltage	V_{CEO}	120	Vdc
Emitter–Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous Peak	I_C	50 100	Adc
Base Current	I_B	20	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

* Indicates JEDEC Registered Data.

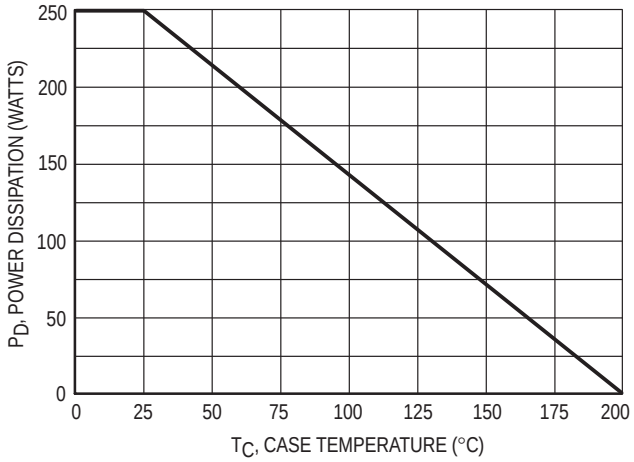


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

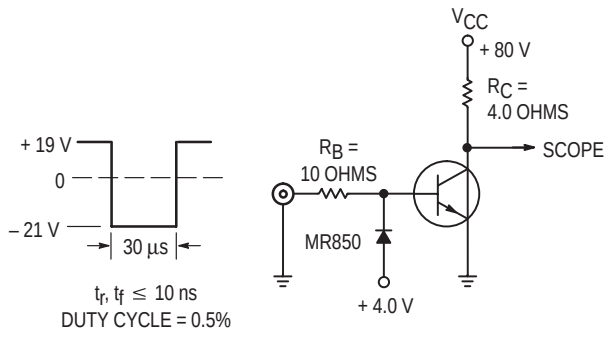
REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
***OFF CHARACTERISTICS**				
Collector–Emitter Sustaining Voltage(1) (I_C = 50 mAdc, I_B = 0)	$V_{CEO(sus)}$	120	—	Vdc
Collector Cutoff Current (V_{CE} = 70 Vdc, I_B = 0)	I_{CEO}	—	50	µAdc
Collector Cutoff Current (V_{CE} = 90% Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	—	10	µAdc
(V_{CE} = 90% Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		—	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	100	µAdc
***ON CHARACTERISTICS(1)**				
DC Current Gain	h_{FE}			—
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		50	—	
(I_C = 20 Adc, V_{CE} = 4.0 Vdc)		30	120	
(I_C = 50 Adc, V_{CE} = 4.0 Vdc)		10	—	
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)		—	1.2	
(I_C = 50 Adc, I_B = 10 Adc)		—	3.0	
Base–Emitter Saturation Voltage	$V_{BE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 2.0 Adc)		—	1.8	
(I_C = 50 Adc, I_B = 10 Adc)		—	3.5	
DYNAMIC CHARACTERISTICS				
*Current–Gain — Bandwidth Product(2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	30	—	MHz
*Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	1500	pF
***SWITCHING CHARACTERISTICS (Figure 2)**				
Rise Time	t_r	—	0.35	µs
Storage Time (V_{CC} = 80 Vdc, I_C = 20 Adc, I_{B1} = I_{B2} = 2.0 Adc)	t_s	—	0.80	µs
Fall Time	t_f	—	0.25	µs

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2.0%. (2) $f_T = |h_{fe}| \bullet f_{test}$



NOTE: For information on Figures 3 & 6, R_B and R_C were varied to obtain desired test conditions.

Figure 2. Switching Time Test Circuit

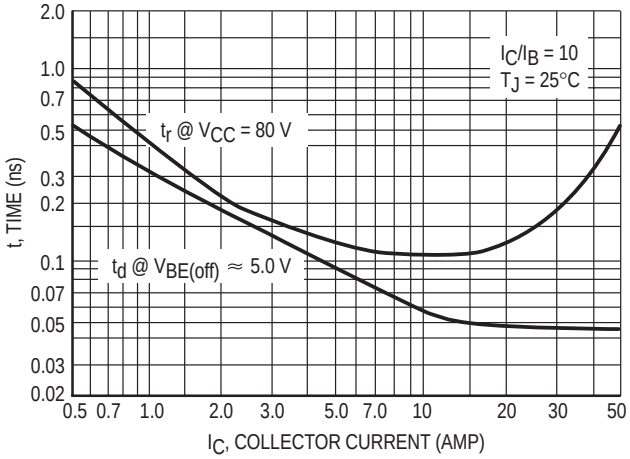


Figure 3. Turn–On Time

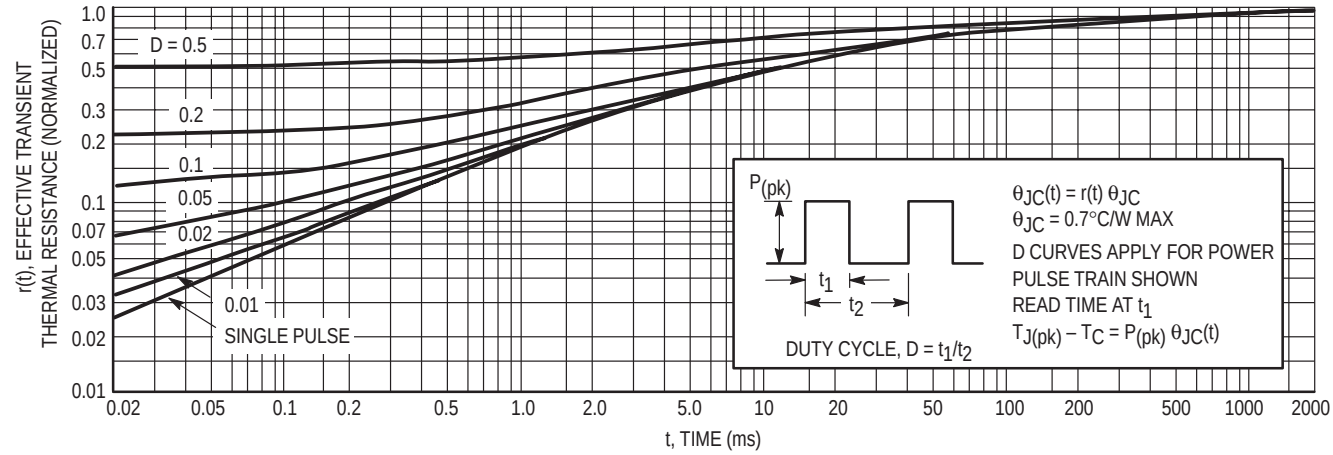


Figure 4. Thermal Response

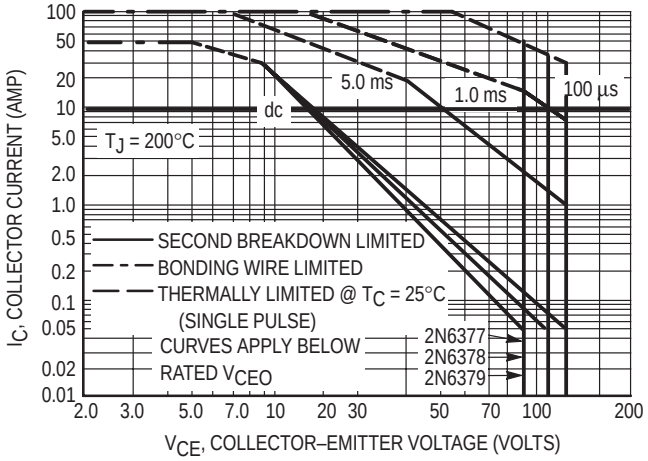


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

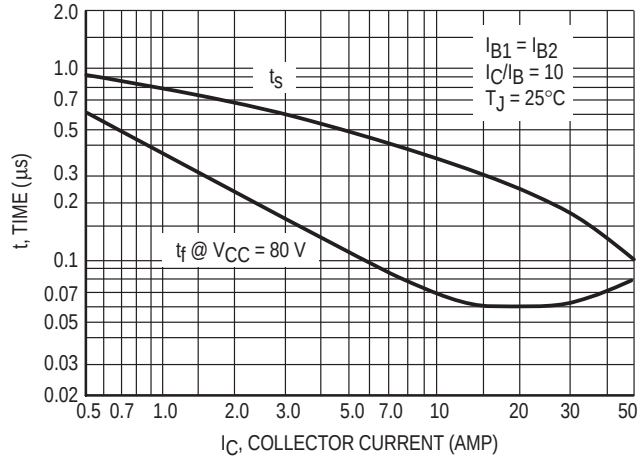


Figure 6. Turn–Off Time

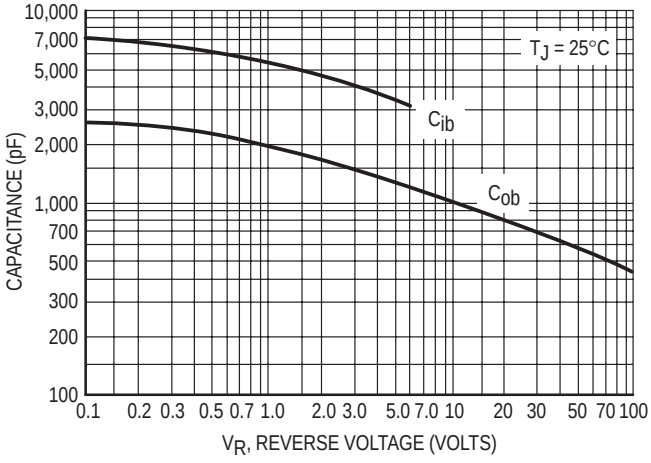


Figure 7. Capacitance

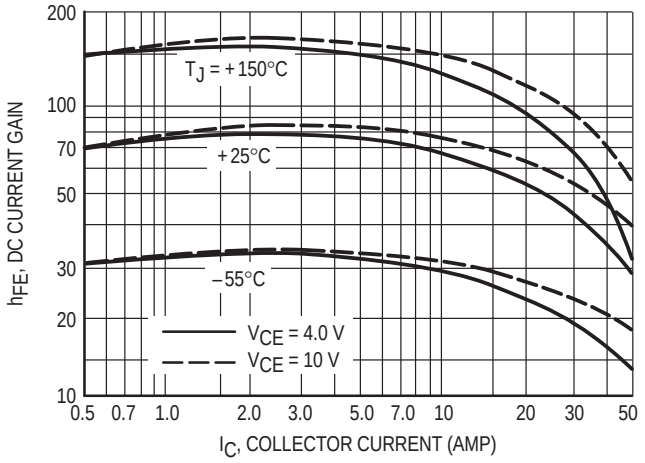


Figure 8. DC Current Gain

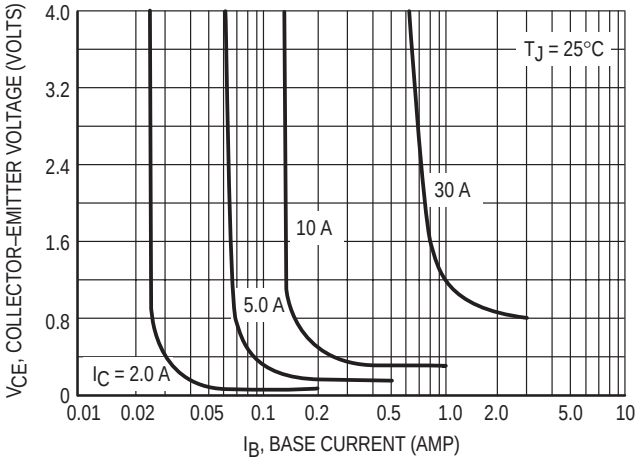


Figure 9. Collector Saturation Region

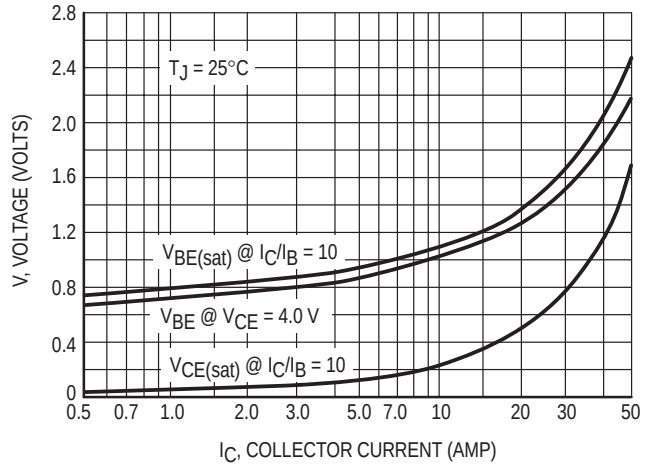


Figure 10. “On” Voltages

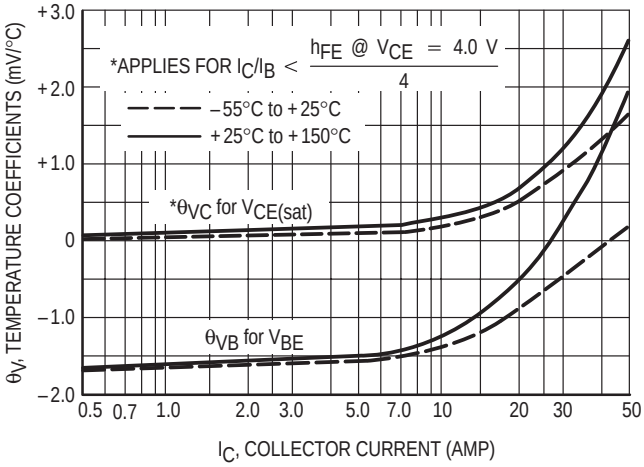


Figure 11. Temperature Coefficients

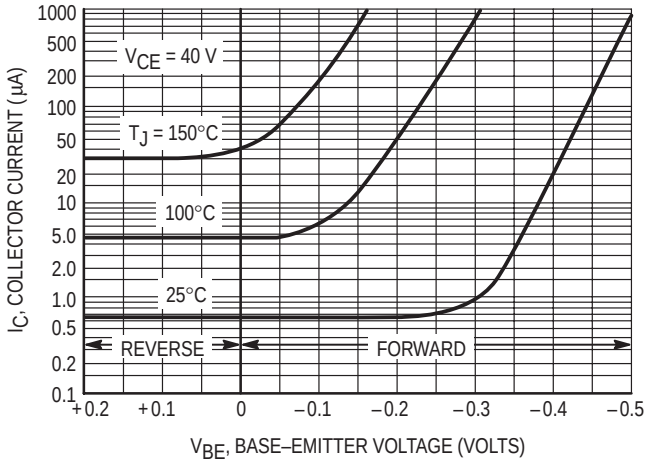


Figure 12. Collector Cut–Off Region

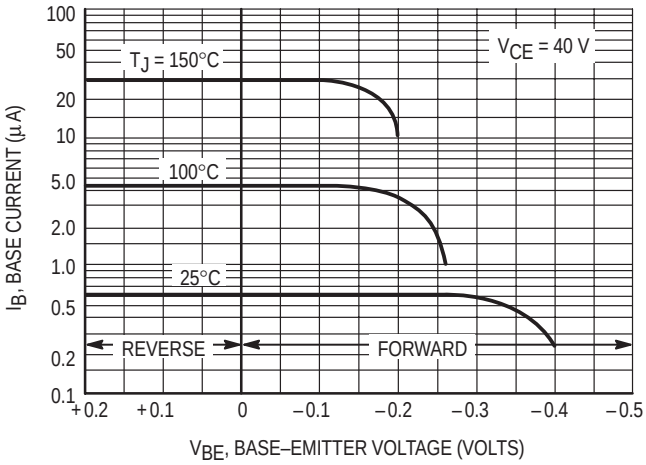


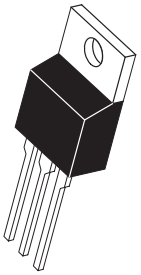
Figure 13. Base Cutoff Region

Plastic Medium-Power Silicon Transistors

2N6387
2N6388*

*Motorola Preferred Device

DARLINGTON
8 AND 10 AMPERE
NPN SILICON
POWER TRANSISTORS
60–80 VOLTS
65 WATTS



CASE 221A–06
TO–220AB

. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector–Emitter Sustaining Voltage – @ 100 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6387
  = 80 Vdc (Min) — 2N6388
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 5.0 Adc — 2N6387, 2N6388
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors
- TO–220AB Compact Package

***MAXIMUM RATINGS**

Rating	Symbol	2N6387	2N6388	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	10 15	10 15	Adc
Base Current	I_B	250		mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 65 0.52		 Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2.0 0.016		 Watts W/°C
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

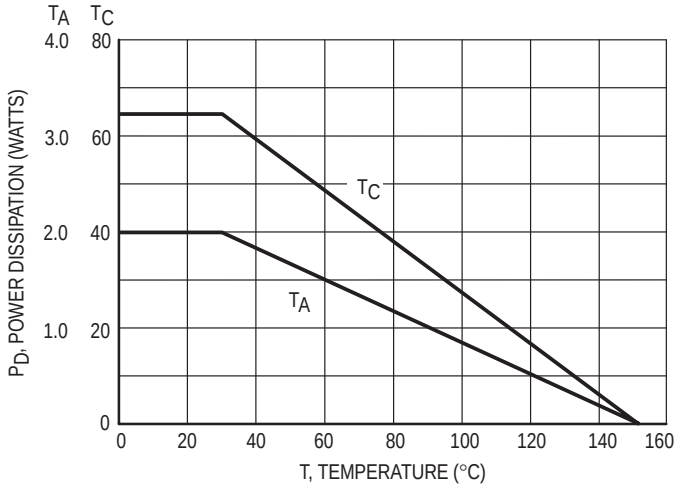


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N6387		60	—	
	2N6388		80	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 60 Vdc, I_B = 0)	2N6387		—	1.0	
(V_{CE} = 80 Vdc, I_B = 0)	2N6388		—	1.0	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6387		—	300	
(V_{CE} – 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	2N6388		—	300	
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6387		—	3.0	mAdc
(V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6388		—	3.0	
Emitter Cutoff Current		I_{EBO}	—	5.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		1000	20,000	
(I_C = 1 0 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		100	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 0.01 Adc)	2N6387, 2N6388		—	2.0	
(I_C = 10 Adc, I_B = 0.1 Adc)	2N6387, 2N6388		—	3.0	
Base–Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		—	2.8	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)	2N6387, 2N6388		—	4.5	
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain		$\|h_{fe}\|$	20	—	
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)					
Output Capacitance		C_{ob}	—	200	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)					
Small–Signal Current Gain		h_{fe}	1000	—	—
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)					

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

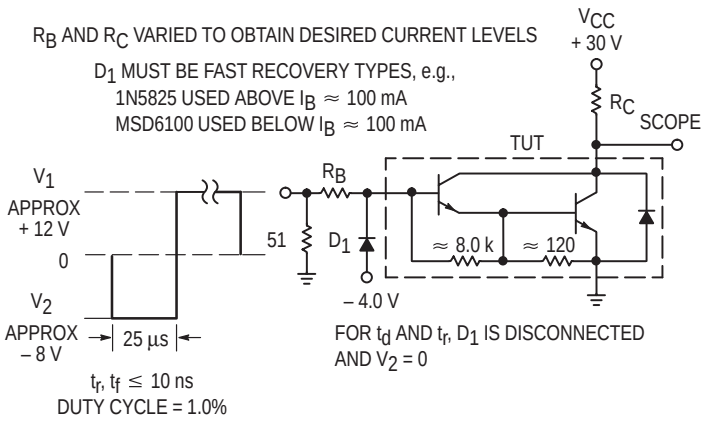


Figure 2. Switching Times Test Circuit

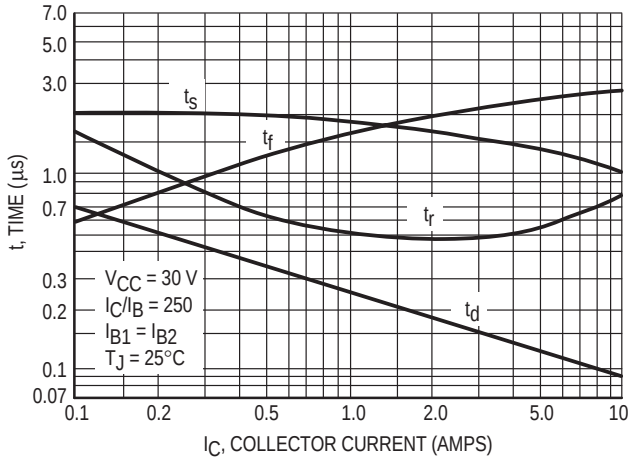


Figure 3. Switching Times

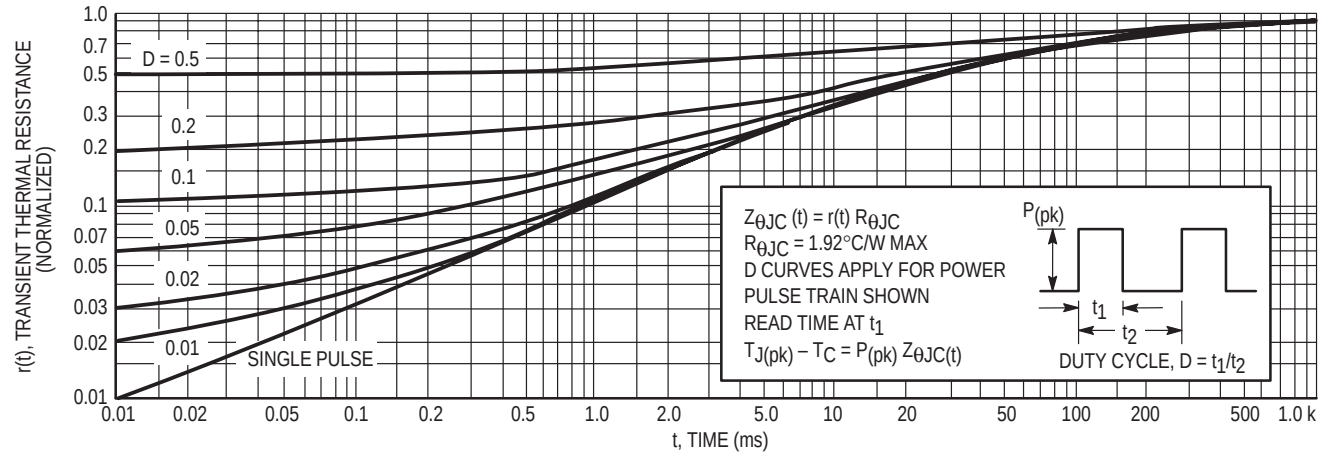


Figure 4. Thermal Response

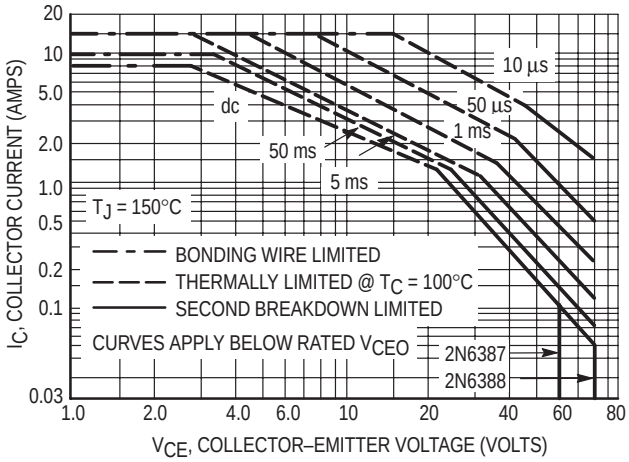


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

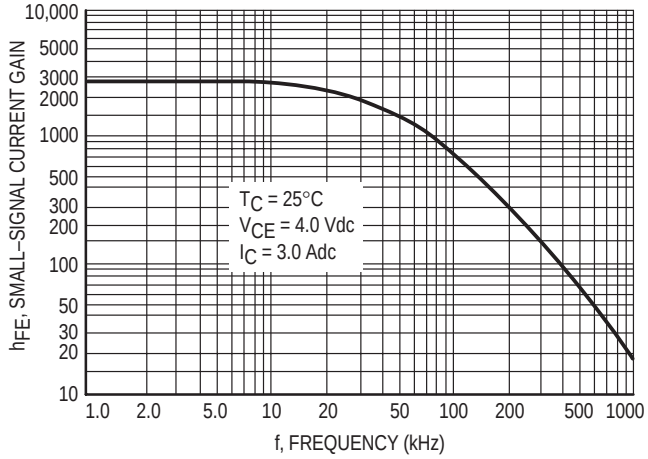


Figure 6. Small–Signal Current Gain

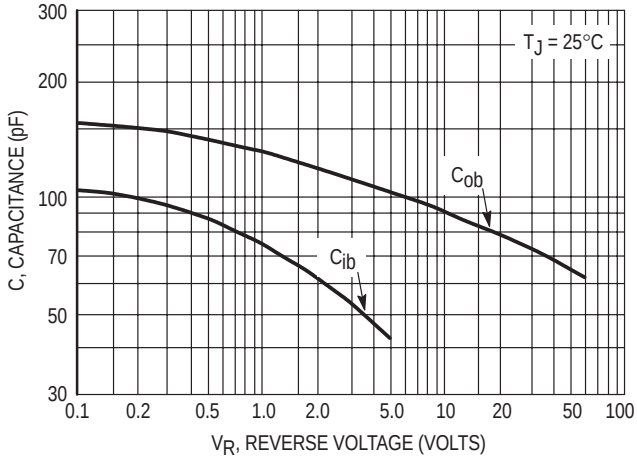


Figure 7. Capacitance

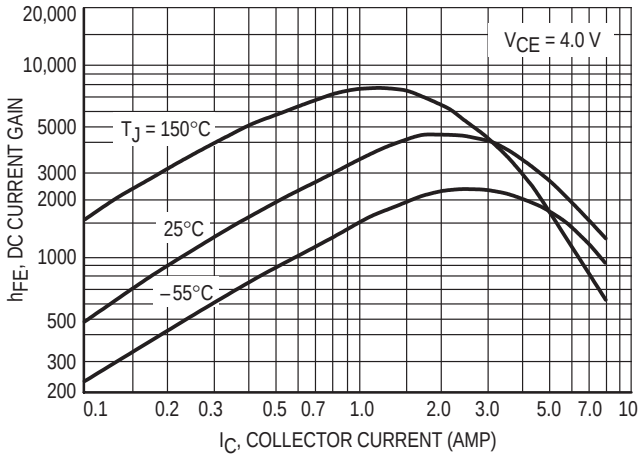


Figure 8. DC Current Gain

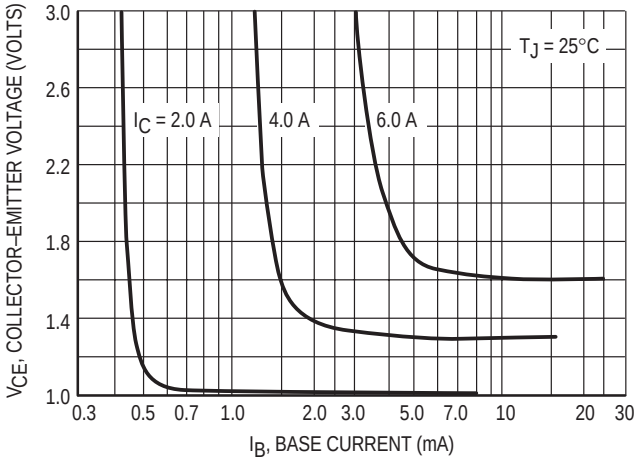


Figure 9. Collector Saturation Region

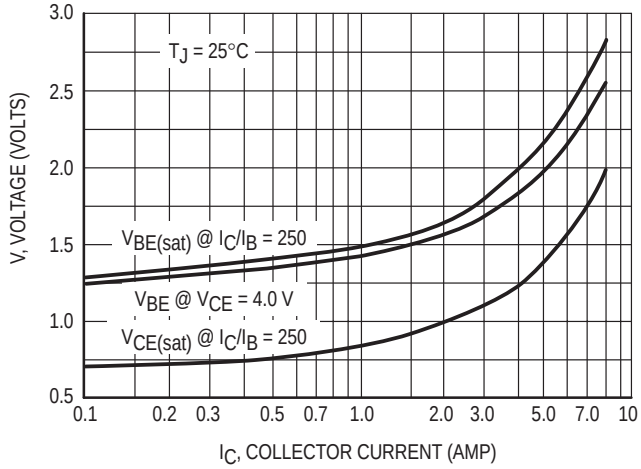


Figure 10. “On” Voltages

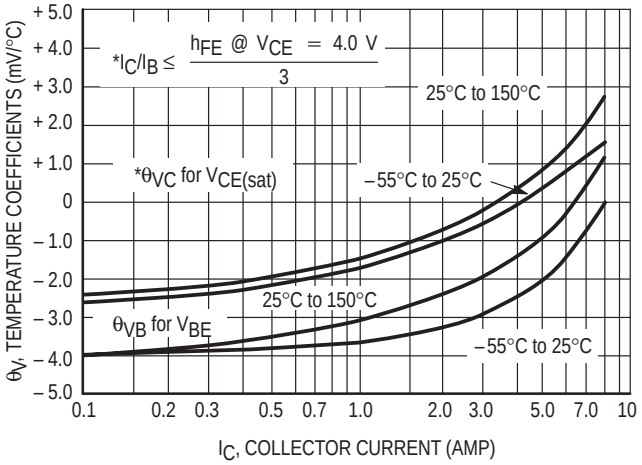


Figure 11. Temperature Coefficients

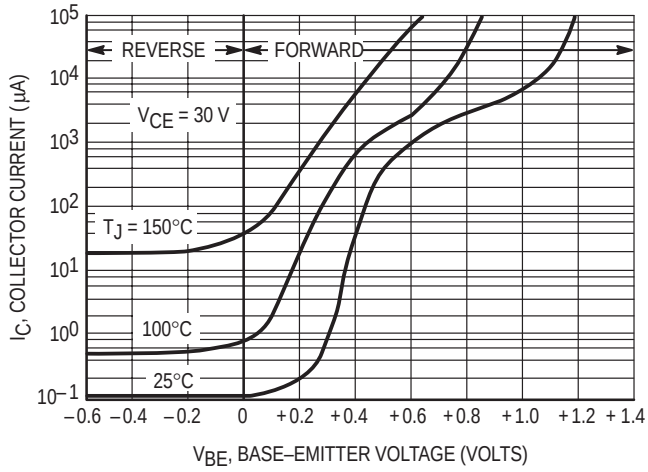


Figure 12. Collector Cut–Off Region

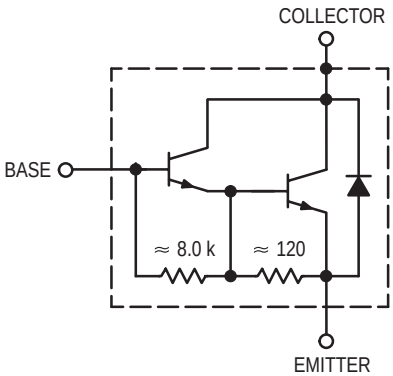


Figure 13. Darlington Schematic

High-Power PNP Silicon Transistors

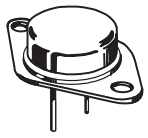
. . . designed for use in industrial–military power amplifier and switching circuit applications.

- High Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 80 Vdc (Min) — 2N6436
  = 100 Vdc (Min) — 2N6437
  = 120 Vdc (Min) — 2N6438
- High DC Current Gain —
  h_{FE} = 20–80 @ I_C = 10 Adc
  = 12 (Min) @ I_C = 25 Adc
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) @ I_C = 10 Adc
- Fast Switching Times @ I_C = 10 Adc
  t_r = 0.3 µs (Max)
  t_s = 1.0 µs (Max)
  t_f = 0.25 µs (Max)
- Complement to NPN 2N6338 thru 2N6341

2N6436
2N6437
2N6438*

***Motorola Preferred Device**

25 AMPERE
POWER TRANSISTORS
PNP SILICON
80, 100, 120 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (1)

Rating	Symbol	2N6436	2N6437	2N6438	Unit
Collector–Base Voltage	V_{CB}	100	120	140	Vdc
Collector–Emitter Voltage	V_{CEO}	80	100	120	Vdc
Emitter–Base Voltage	V_{EB}	6.0			Vdc
Collector Current — Continuous Peak	I_C	25 50			Adc
Base Current	I_B	10			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14			Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	–65 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	°C/W

(1) Indicates JEDEC Registered Data.

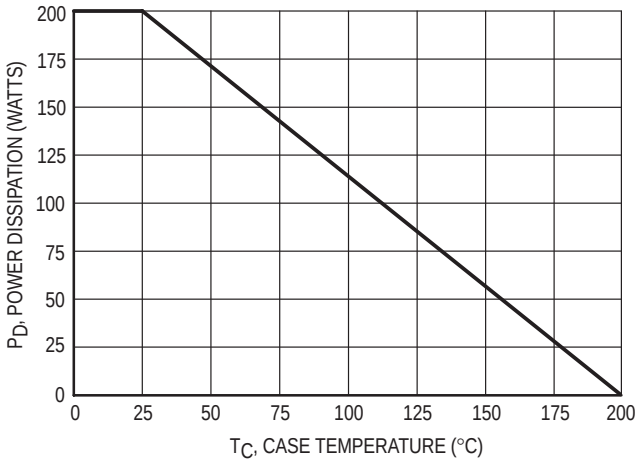


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

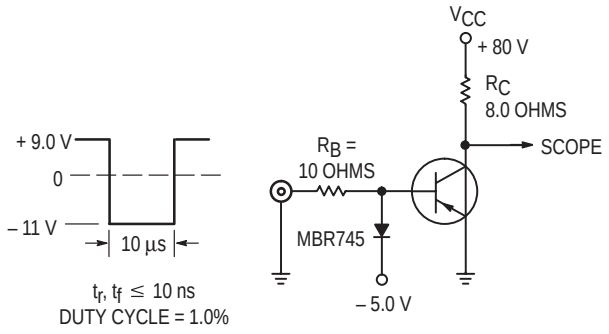
REV 7

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 50 mAdc, I_B = 0)	2N6436	$V_{CEO(sus)}$	80	—	Vdc
	2N6437		100	—	
	2N6438		120	—	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 40 Vdc, I_B = 0)	2N6436		—	50	
(V_{CE} = 50 Vdc, I_B = 0)	2N6437		—	50	
(V_{CE} = 60 Vdc, I_B = 0)	2N6438		—	50	
Collector Cutoff Current		I_{CEX}			μAdc
(V_{CE} = 90 Vdc, $V_{BE(off)}$ = –1.5 Vdc)	2N6436		—	10	
(V_{CE} = 110 Vdc, $V_{BE(off)}$ = –1.5 Vdc)	2N6437		—	10	
(V_{CE} = 130 Vdc, $V_{BE(off)}$ = –1.5 Vdc)	2N6438		—	10	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = –1.5 Vdc, T_C = 150°C)	2N6436		—	1.0	mAdc
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = –1.5 Vdc, T_C = 150°C)	2N6437		—	1.0	
(V_{CE} = 120 Vdc, $V_{BE(off)}$ = –1.5 Vdc, T_C = 150°C)	2N6438		—	1.0	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 100 Vdc, I_E = 0)	2N6436		—	10	
(V_{CB} = 120 Vdc, I_E = 0)	2N6437		—	10	
(V_{CB} = 140 Vdc, I_E = 0)	2N6438		—	10	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	100	μAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			—
(I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)			30	—	
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)			20	120	
(I_C = 25 Adc, V_{CE} = 2.0 Vdc)			12	—	
Collector–Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)			—	1.0	
(I_C = 25 Adc, I_B = 2.5 Adc)			—	1.8	
Base–Emitter Saturation Voltage (1)		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 1.0 Adc)			—	1.8	
(I_C = 25 Adc, I_B = 2.5 Adc)			—	2.5	
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	40	—	MHz
Output Capacitance (V_{CE} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	700	pF
SWITCHING CHARACTERISTICS					
Rise Time (V_{CC} = 80 Vdc, I_C = 10 A, $V_{BE(off)}$ = 6.0 Vdc, I_{B1} = 1.0 Adc)		t_r	—	0.3	μs
Storage (V_{CC} = 80 Vdc, I_C = 10 A, $V_{BE(off)}$ = 6.0 Vdc, I_{B1} = I_{B2} = 1.0 Adc)		t_s	—	1.0	μs
Fall Time (V_{CC} = 80 Vdc, I_C = 10 A, $V_{BE(off)}$ = 6.0 Vdc, I_{B1} = I_{B2} = 1.0 Adc)		t_f	—	0.25	μs

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.



NOTE: For information on Figures 3 and 6, R_B and R_C were varied to obtain desired test conditions.

Figure 2. Switching Time Test Circuit

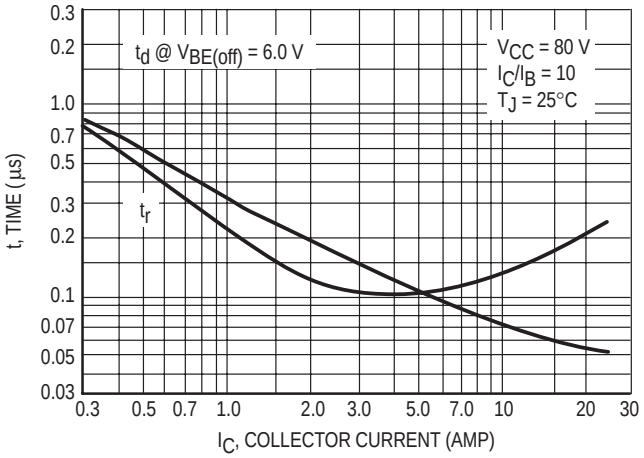


Figure 3. Turn–On Time

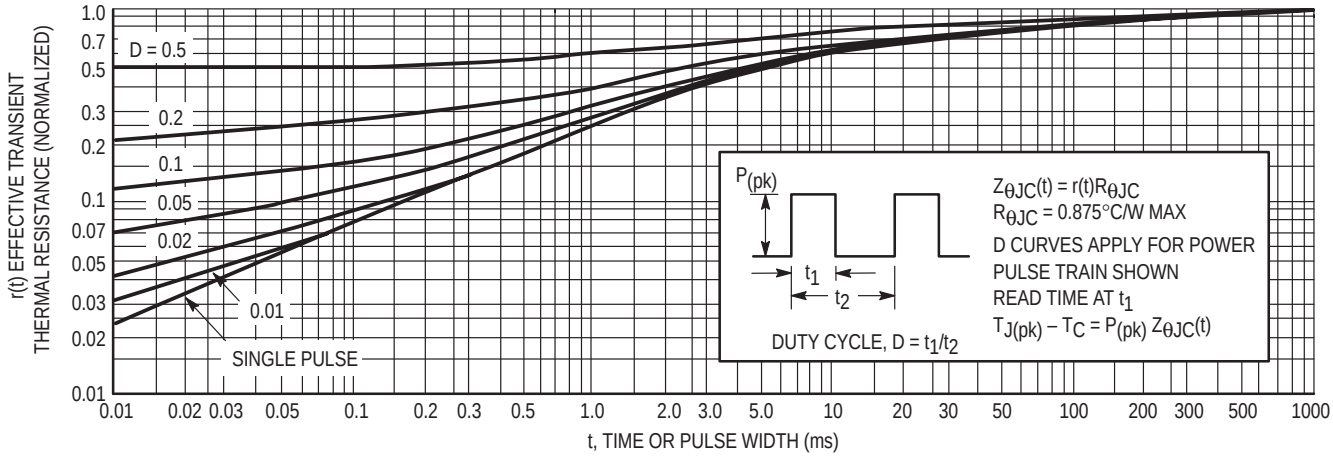


Figure 4. Thermal Response

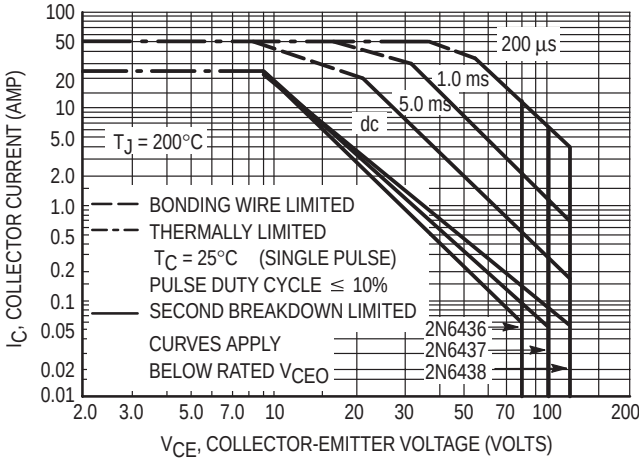


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

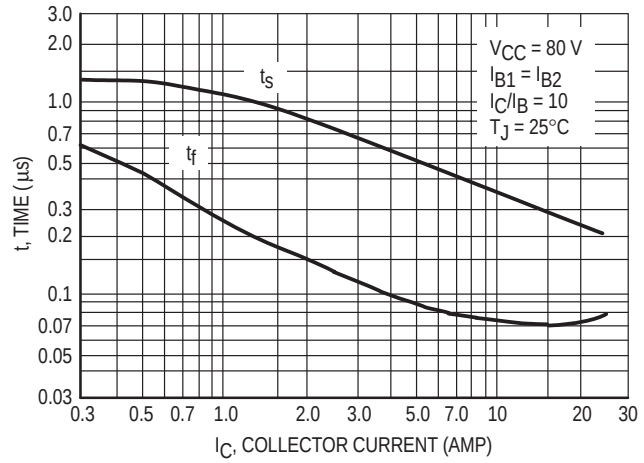


Figure 6. Turn-Off Time

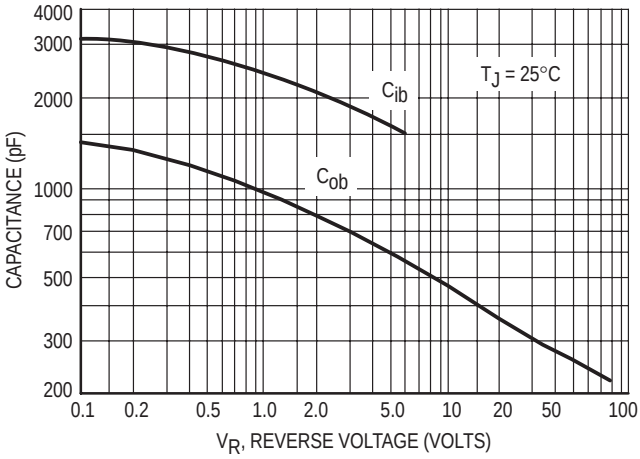


Figure 7. Capacitance

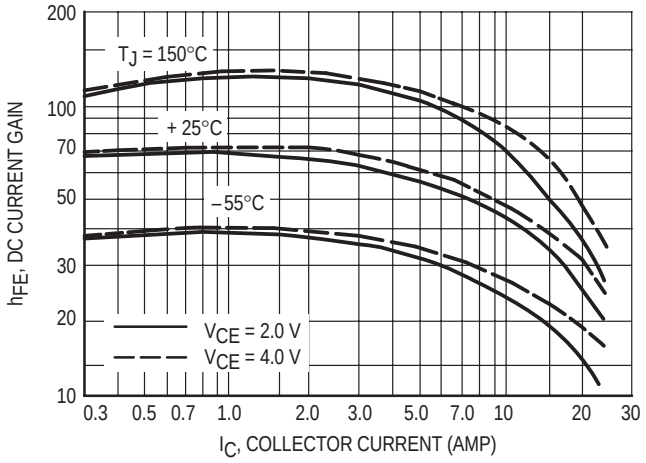


Figure 8. DC Current Gain

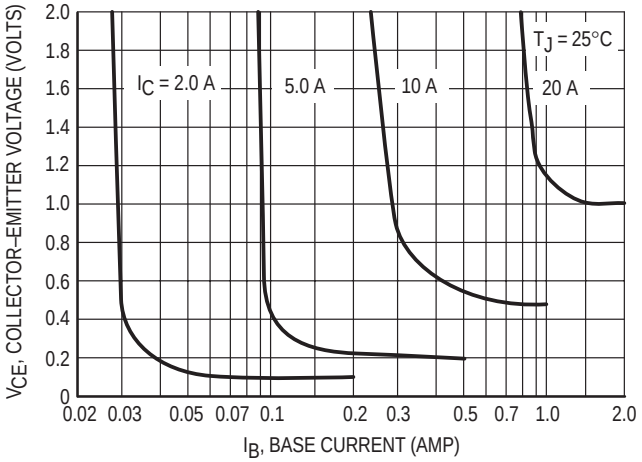


Figure 9. Collector Saturation Region

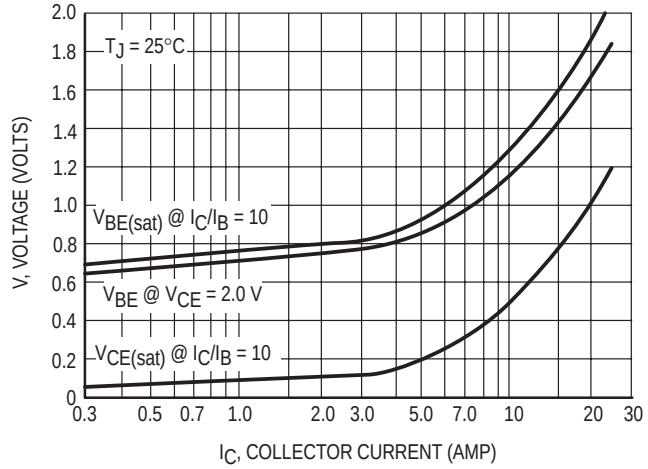


Figure 10. “On” Voltages

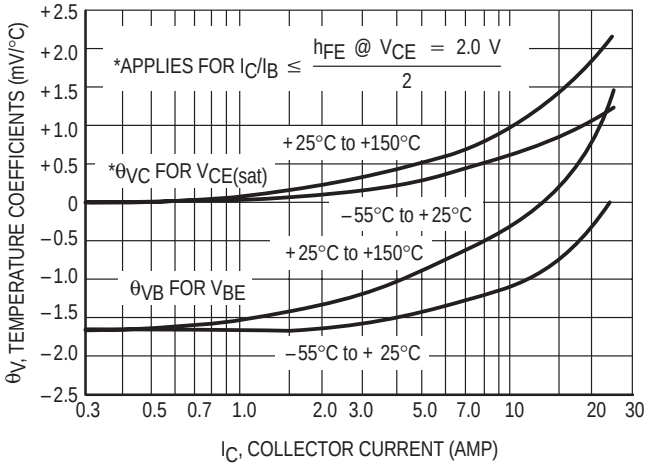


Figure 11. Temperature Coefficients

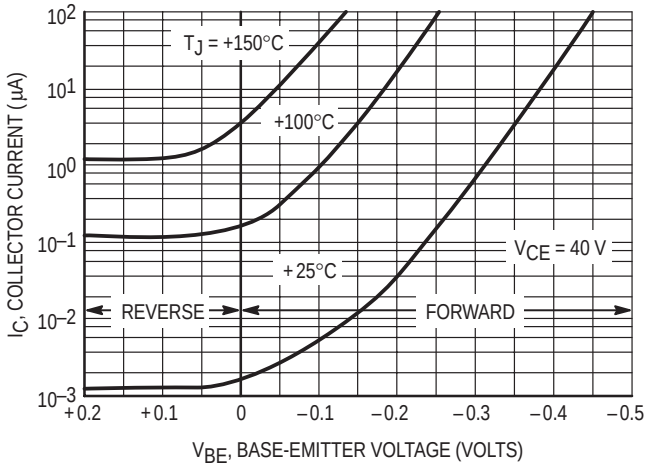


Figure 12. Collector Cut-Off Region

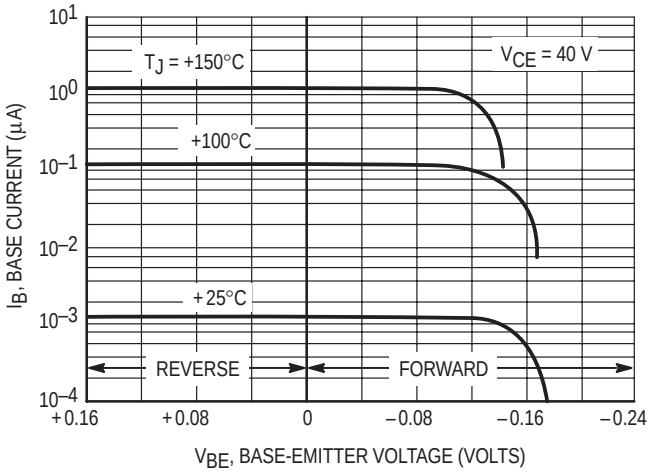


Figure 13. Base Cutoff Region

Complementary Silicon Plastic Power Transistors

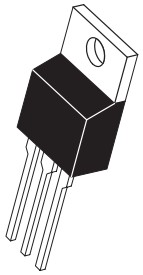
. . . designed for use in general–purpose amplifier and switching applications.

- DC Current Gain Specified to 15 Amperes —
  h_{FE} = 20–150 @ I_C = 5.0 Adc
  = 5.0 (Min) @ I_C = 15 Adc
- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc (Min) – 2N6487, 2N6490
  = 80 Vdc (Min) – 2N6488, 2N6491
- High Current Gain — Bandwidth Product
  f_T = 5.0 MHz (Min) @ I_C = 1.0 Adc
- TO–220AB Compact Package

NPN
2N6487
2N6488*
PNP
2N6490
2N6491*

***Motorola Preferred Device**

15 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60–80 VOLTS
75 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS (1)

Rating	Symbol	2N6487 2N6490	2N6488 2N6491	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	70	90	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	15		Adc
Base Current	I_B	5.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.8 0.014		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W

(1) Indicates JEDEC Registered Data.

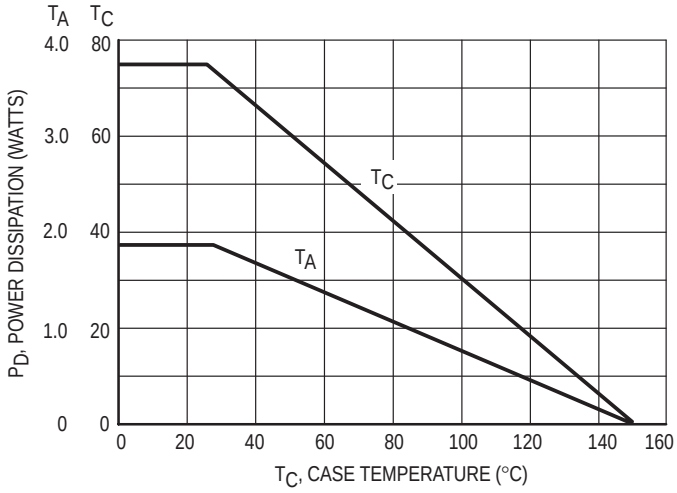


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

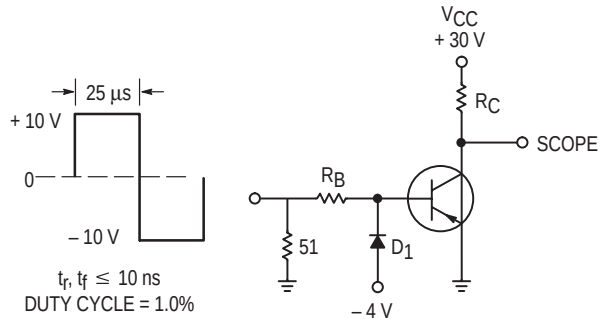
***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N6487, 2N6490 2N6488, 2N6491	$V_{CEO(sus)}$	 60 80	 — —	Vdc
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, V_{BE} = 1.5 Vdc)	2N6487, 2N6490 2N6488, 2N6491	VCEX	 70 90	 — —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	 2N6487, 2N6490 2N6488, 2N6491	I_{CEO}	 — —	 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 65 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 85 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	 2N6487, 2N6490 2N6488, 2N6491 2N6487, 2N6490 2N6488, 2N6491	I_{CEX}	 — — — —	 500 500 5.0 5.0	µAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 15 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	 20 5.0	 150 —	—
Collector–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.5 Adc) (I_C = 15 Adc, I_B = 5.0 Adc)		$V_{CE(sat)}$	 — —	 1.3 3.5	Vdc
Base–Emitter On Voltage (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 15 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	 — —	 1.3 3.5	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 MHz)		f_T	5.0	—	MHz
Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)		h_{fe}	25	—	—

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.



R_B AND R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS.
FOR PNP, REVERSE ALL POLARITIES.

D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

Figure 2. Switching Time Test Circuit

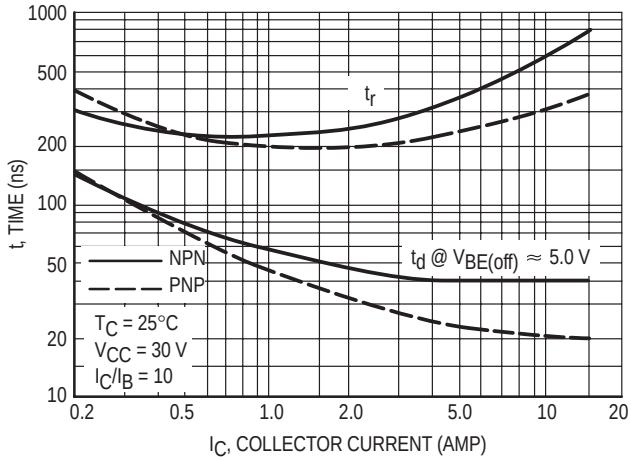


Figure 3. Turn–On Time

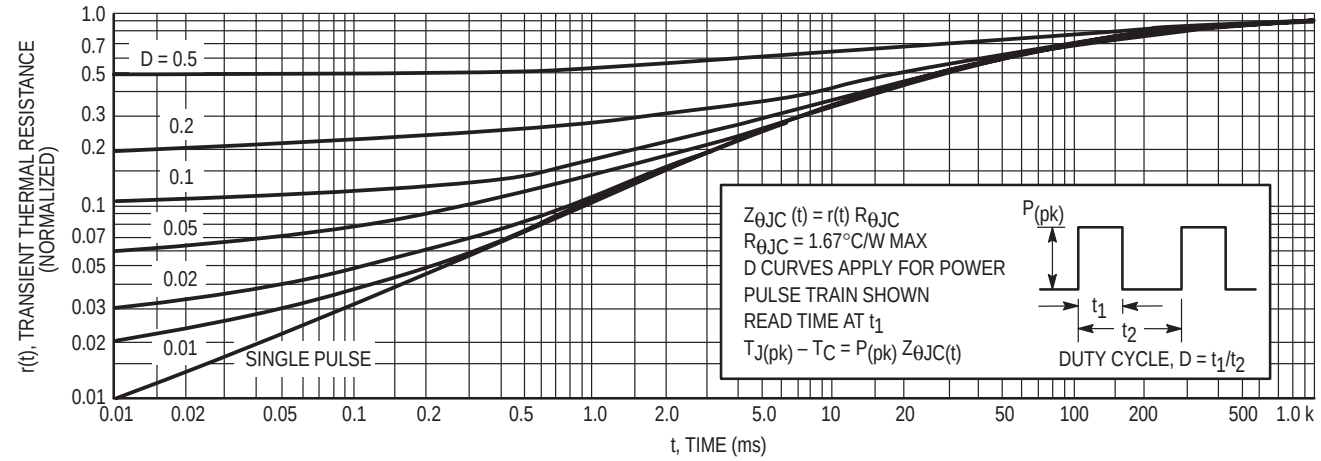


Figure 4. Thermal Response

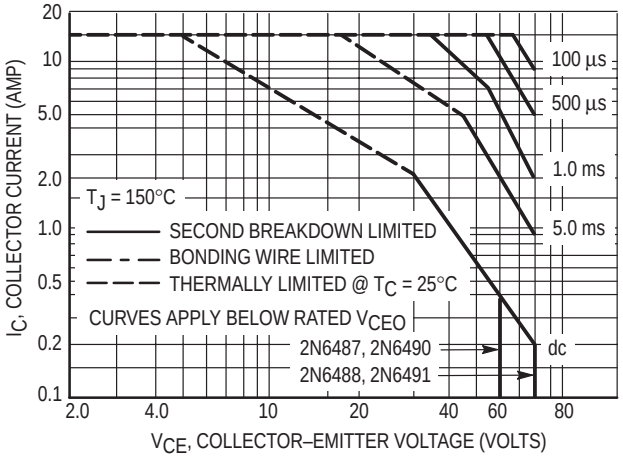


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistors average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

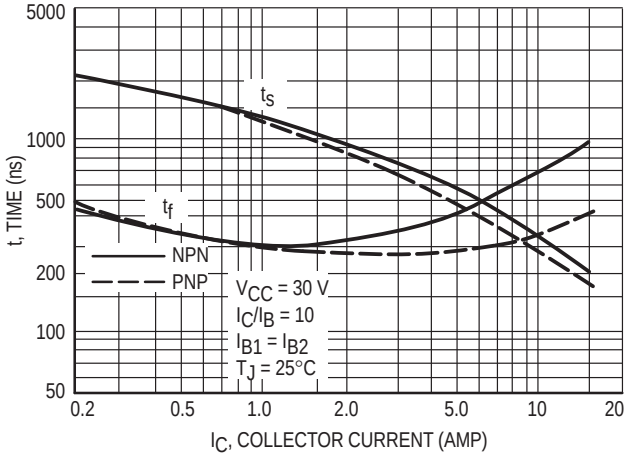


Figure 6. Turn–Off Time

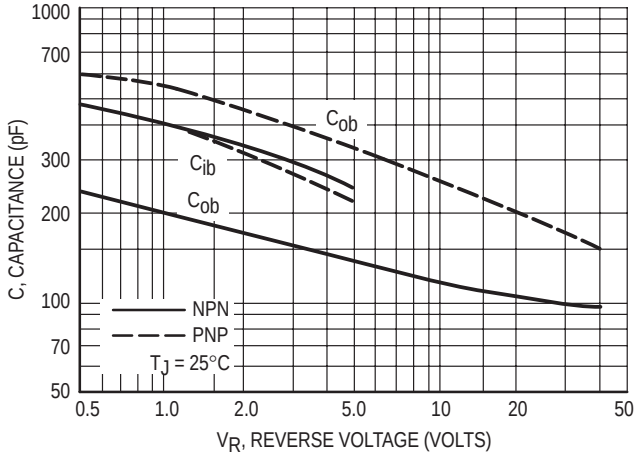
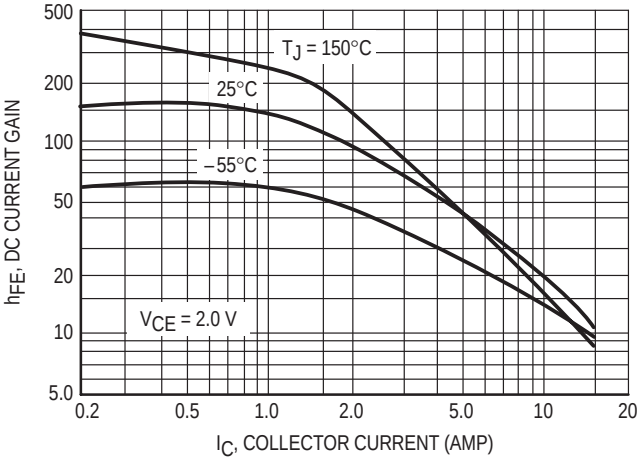


Figure 7. Capacitances

NPN
2N6487, 2N6488



PNP
2N6490, 2N6491

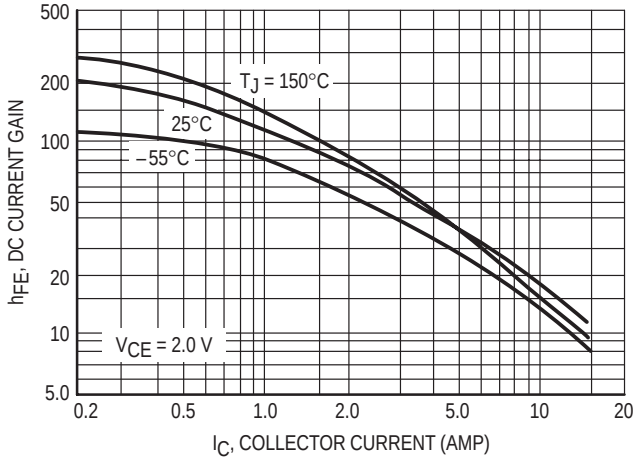
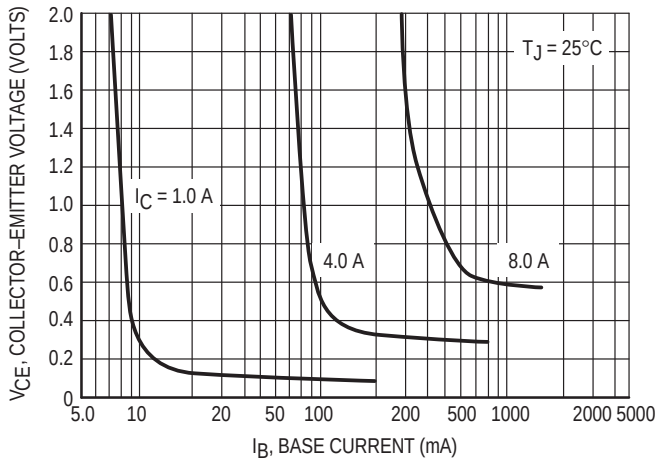


Figure 8. DC Current Gain



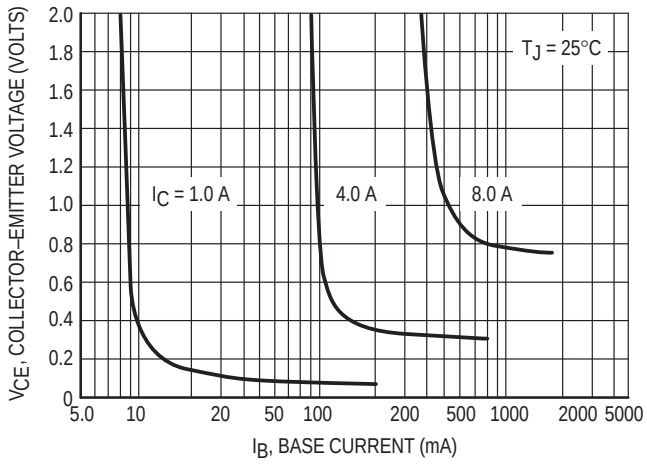
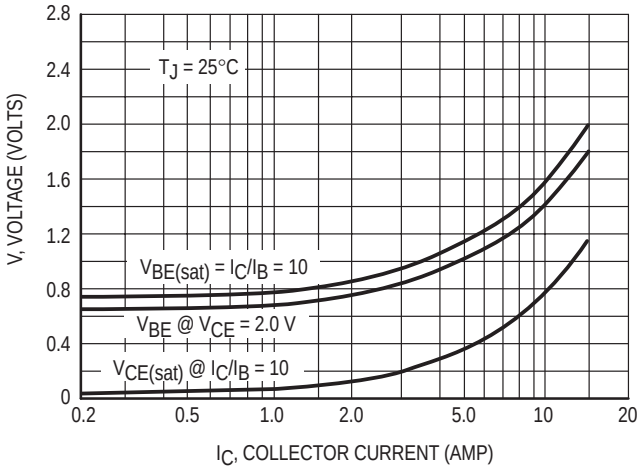


Figure 9. Collector Saturation Region



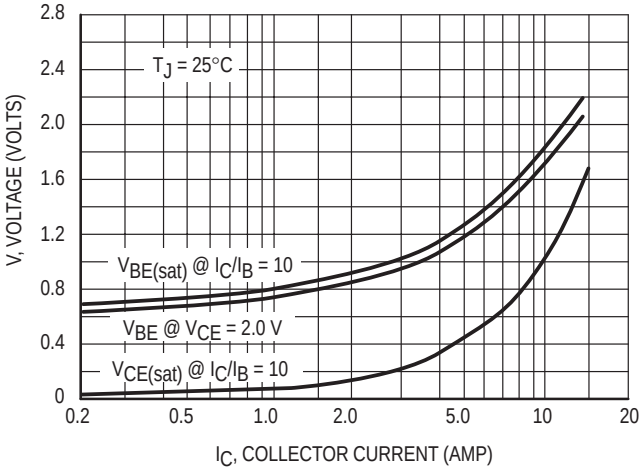


Figure 10. “On” Voltages

2N6497
2N6498*

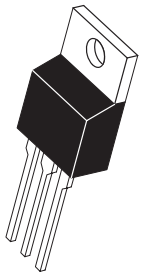
*Motorola Preferred Device

High Voltage NPN Silicon Power Transistors

. . . designed for high voltage inverters, switching regulators and line–operated amplifier applications. Especially well suited for switching power supply applications.

- High Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 250 Vdc (Min) — 2N6497
  = 300 Vdc (Min) — 2N6498
- Excellent DC Current Gain
  h_{FE} = 10–75 @ I_C = 2.5 Adc
- Low Collector–Emitter Saturation Voltage @ I_C = 2.5 Adc —
  $V_{CE(sat)}$ = 1.0 Vdc (Max) — 2N6497
  = 1.25 Vdc (Max) — 2N6498

5 AMPERE
POWER TRANSISTORS
NPN SILICON
250 & 300 VOLTS
80 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS (1)

Rating	Symbol	2N6497	2N6498	Unit
Collector–Emitter Voltage	V_{CEO}	250	300	Vdc
Collector–Base Voltage	V_{CB}	350	400	Vdc
Emitter–Base Voltage	V_{EB}	6.0	6.0	Vdc
Collector Current — Continuous — Peak	I_C	5.0 10	5.0 10	Adc
Base Current	I_B	2.0	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.64	80 0.64	Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	–65 to +150	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W

(1) Indicates JEDEC Registered Data.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$				Vdc
(I_C = 25 mAdc, I_B = 0)	2N6497		250	—	—	
	2N6498		300	—	—	
Collector Cutoff Current		I_{CEX}				mAdc
(V_{CE} = 350 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6497		—	—	1.0	
(V_{CE} = 400 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6498		—	—	1.0	
(V_{CE} = 175 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	2N6497		—	—	10	
(V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	2N6498		—	—	10	
Emitter Cutoff Current		I_{EBO}	—	—	1.0	mAdc
(V_{BE} = 6.0 Vdc, I_C = 0)						
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				—
(I_C = 2.5 Adc, V_{CE} = 10 Vdc)			10	—	75	
(I_C = 5.0 Adc, V_{CE} = 10 Vdc)			3.0	—	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 2.5 Adc, I_B = 500 mAdc)	2N6497		—	—	1.0	
	2N6498		—	—	1.25	
(I_C = 5.0 Adc, I_B = 2.0 Adc)	All Devices		—	—	5.0	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 2.5 Adc, I_B = 500 mAdc)			—	—	1.5	
(I_C = 5.0 Adc, I_B = 2.0 Adc)			—	—	2.5	
DYNAMIC CHARACTERISTICS						
Current–Gain — Bandwidth Product		f_T	5.0	—	—	MHz
(I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)						
Output Capacitance		C_{ob}	—	—	150	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)						
SWITCHING CHARACTERISTICS						
Rise Time		t_r	—	0.4	1.0	μs
(V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = 0.5 Adc)						
Storage Time		t_s	—	1.4	2.5	μs
(V_{CC} = 125 Vdc, I_C = 2.5 Adc, V_{BE} = 5.0 Vdc, I_{B1} = I_{B2} = 0.5 Adc)						
Fall Time		t_f	—	0.45	1.0	μs
(V_{CC} = 125 Vdc, I_C = 2.5 Adc, I_{B1} = I_{B2} = 0.5 Adc)						

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

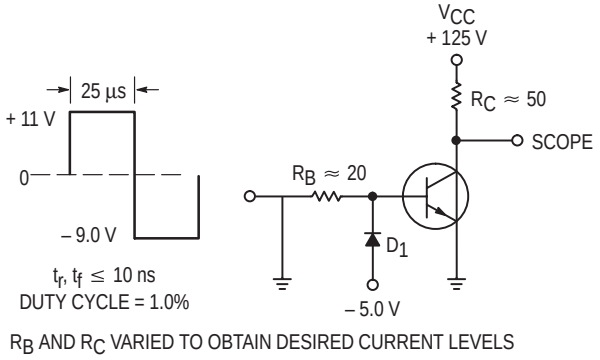


Figure 1. Switching Time Test Circuit

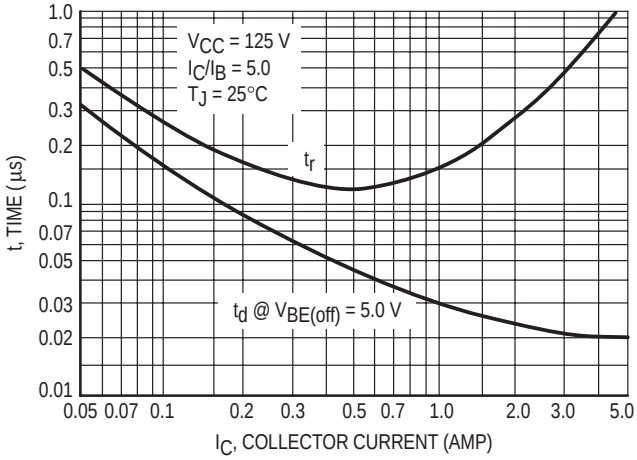


Figure 2. Turn–On Time

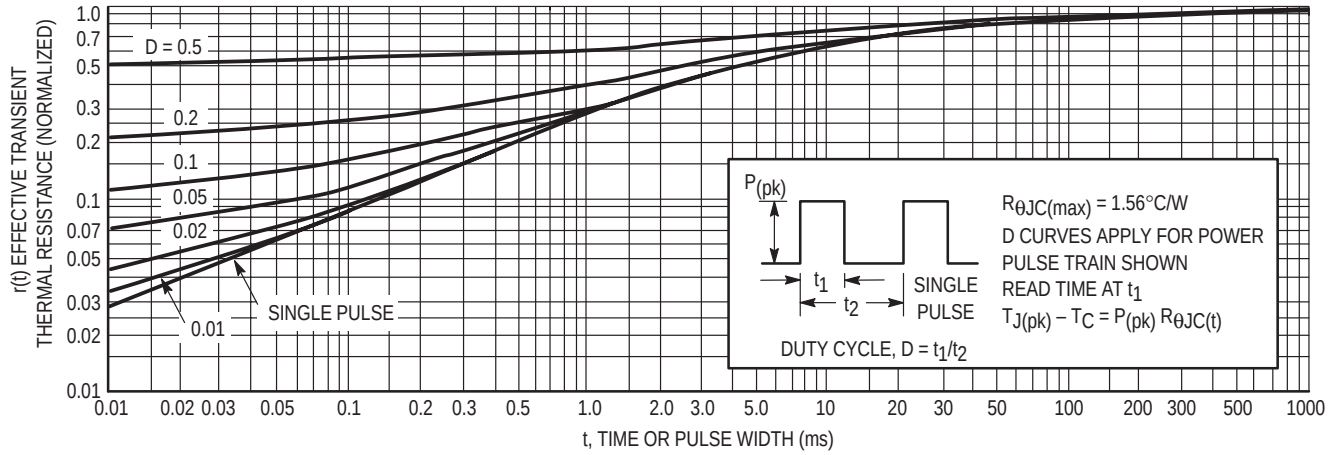


Figure 3. Thermal Response

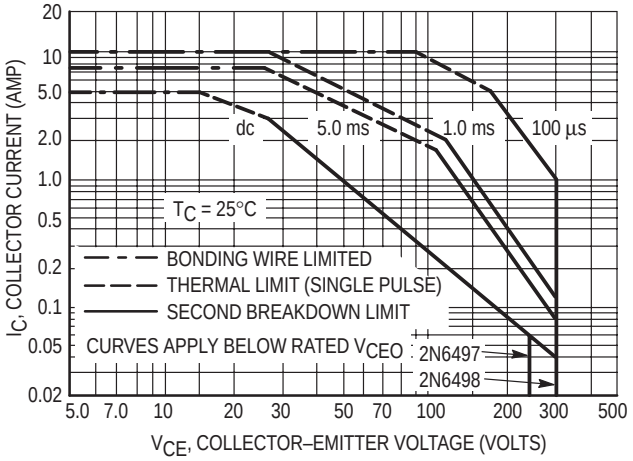


Figure 4. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltage shown on Figure 4 may be found at any case temperature by using the appropriate curve on Figure 6.

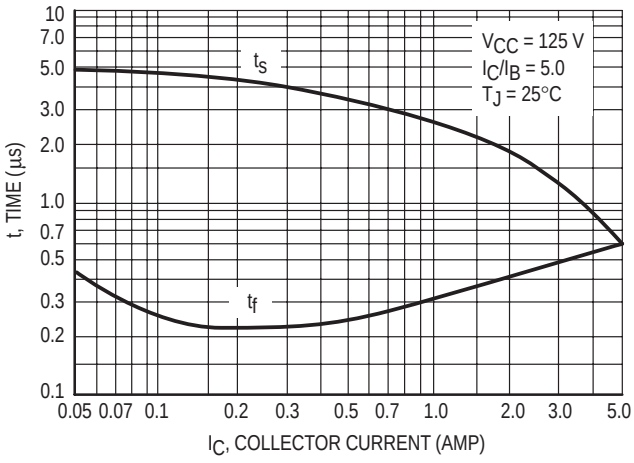


Figure 5. Turn–Off Time

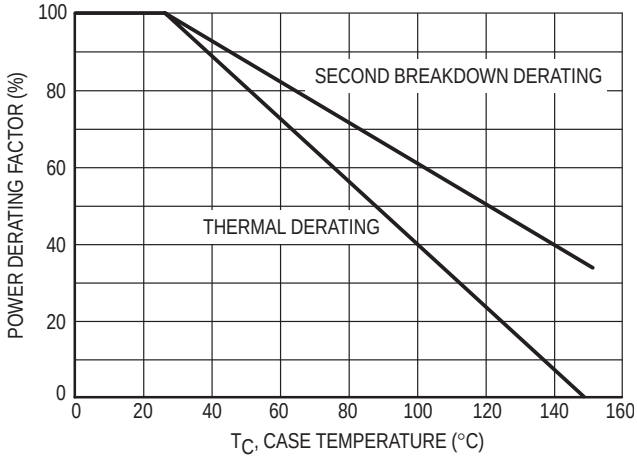


Figure 6. Power Derating

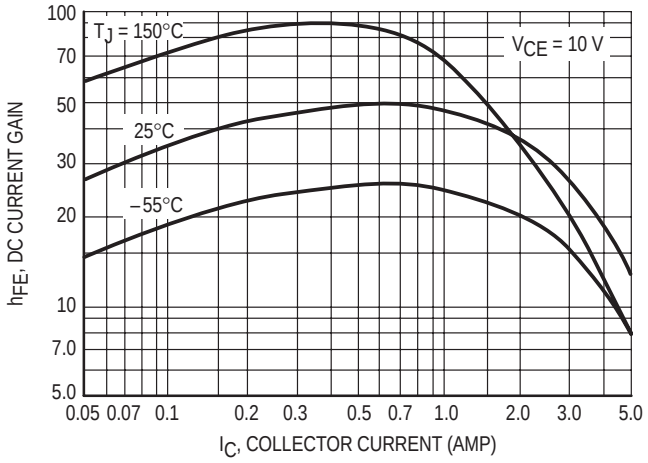


Figure 7. DC Current Gain

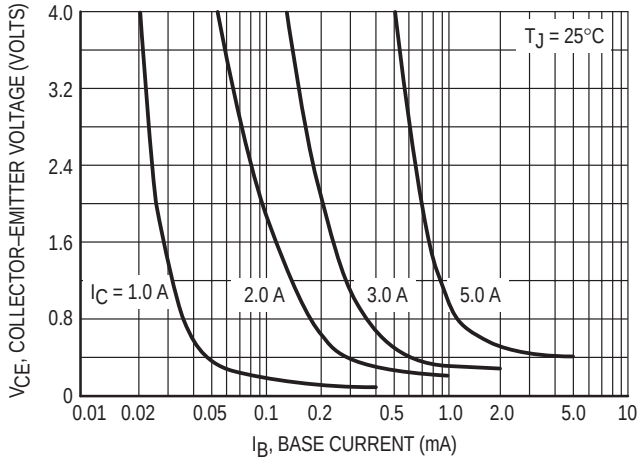


Figure 8. Collector Saturation Region

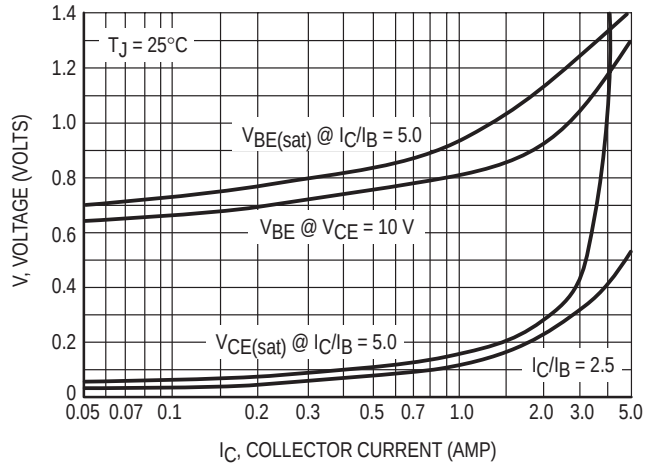


Figure 9. “On” Voltages

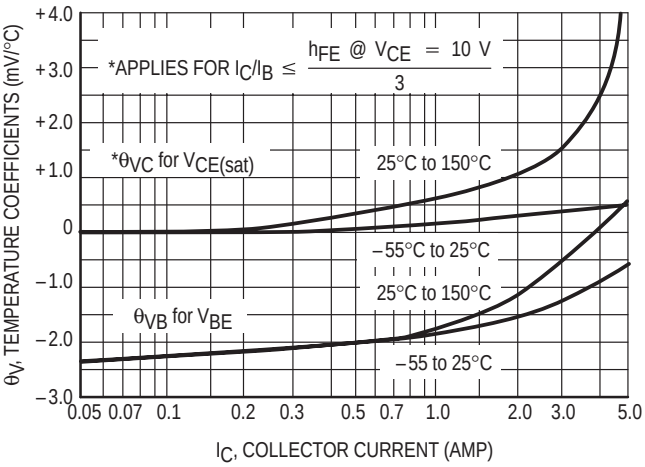


Figure 10. Temperature Coefficients

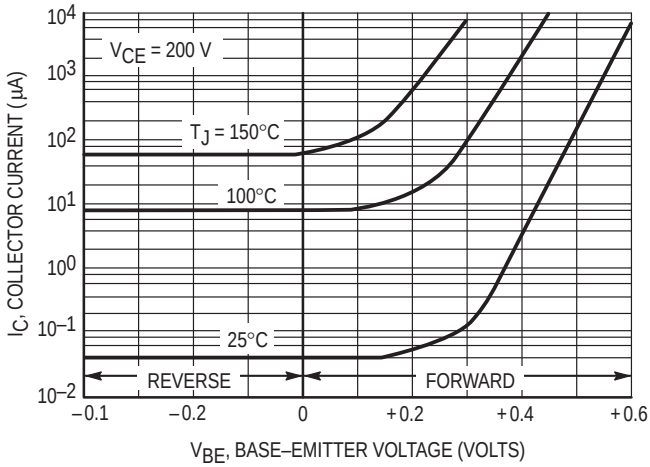


Figure 11. Collector Cutoff Region

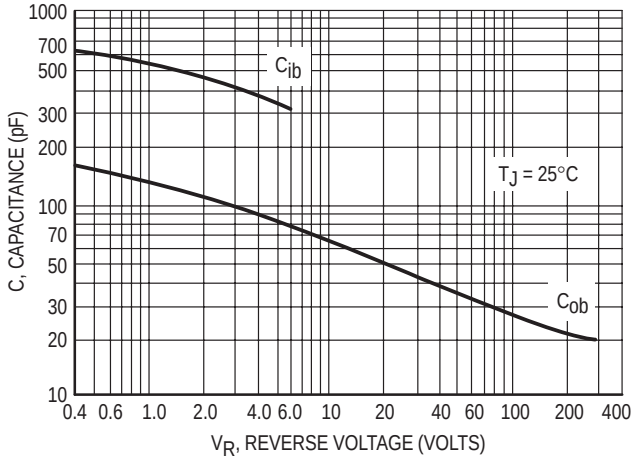


Figure 12. Capacitance

2N6547

Designer's™ Data Sheet

Switchmode Series NPN Silicon Power Transistors

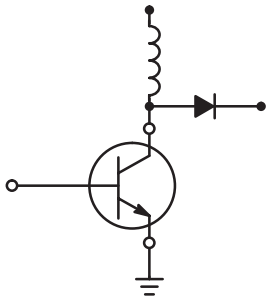
15 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
175 WATTS

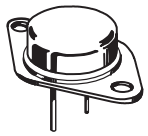
The 2N6547 transistor is designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for 115 and 220 volt line operated switch–mode applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

Specification Features —

High Temperature Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents





CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (1)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector–Emitter Voltage	$V_{CEX(sus)}$	450	Vdc
Collector–Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	9.0	Vdc
Collector Current — Continuous — Peak (2)	I_C I_{CM}	15 30	Adc
Base Current — Continuous — Peak (2)	I_B I_{BM}	10 20	Adc
Emitter Current — Continuous — Peak (2)	I_E I_{EM}	25 35	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	 175 100 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 4

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, I_B = 0)	2N6546 2N6547	$V_{CEO(sus)}$	 300 400	 — —	Vdc
Collector–Emitter Sustaining Voltage (I_C = 8.0 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) (I_C = 15 A, V_{clamp} = Rated V_{CEO} = 100 V, T_C = 100°C)	2N6546 2N6547 2N6546 2N6547	$V_{CEX(sus)}$	 350 450 200 300	 — — — —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	 — —	 1.0 4.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased t = 1.0 s (non–repetitive) (V_{CE} = 100 Vdc)		$I_{S/b}$	0.2	—	Adc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 10 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	 1 2 6.0	 60 30	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc) (I_C = 15 Adc, I_B = 3.0 Adc) (I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)		$V_{CE(sat)}$	 — — —	 1.5 5.0 2.5	Vdc
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc) (I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C		$V_{BE(sat)}$	 — —	 1.6 1.6	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	6.0	28	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)		C_{ob}	125	500	pF
SWITCHING CHARACTERISTICS					
Resistive Load					
Delay Time	(V_{CC} = 250 V, I_C = 10 A, I_{B1} = I_{B2} = 2.0 A, t_p = 100 µs, Duty Cycle ≤ 2.0%)	t_d	—	0.05	µs
Rise Time		t_r	—	1.0	µs
Storage Time		t_s	—	4.0	µs
Fall Time		t_f	—	0.7	µs
Inductive Load, Clamped					
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_s	—	5.0	µs
Fall Time		t_f	—	1.5	µs
			Typical		
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_s	2.0		µs
Fall Time		t_f	0.09		µs

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

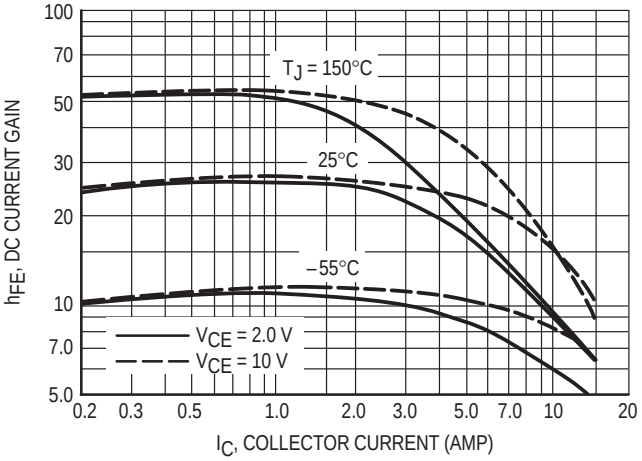


Figure 1. DC Current Gain

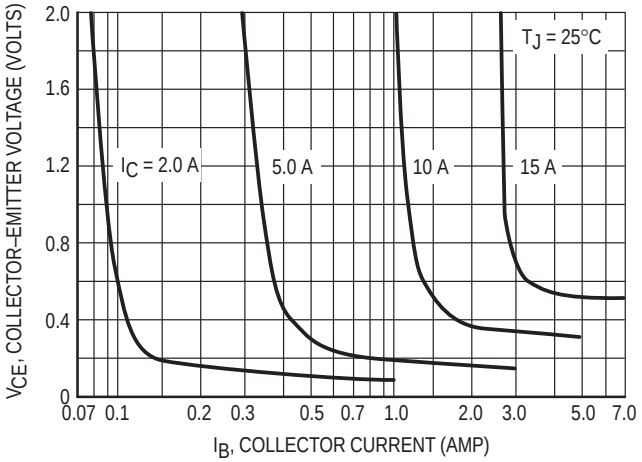


Figure 2. Collector Saturation Region

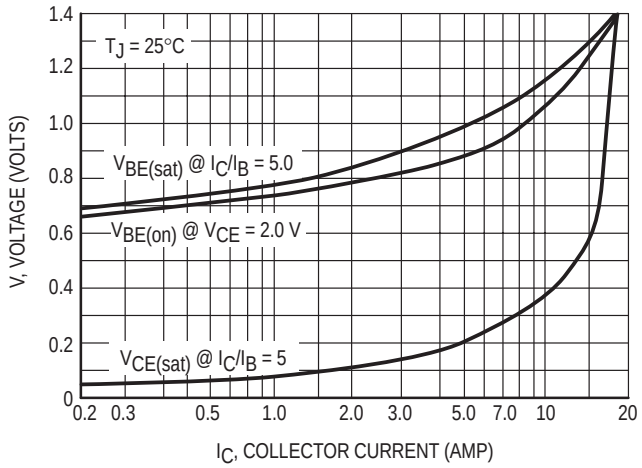


Figure 3. “On” Voltages

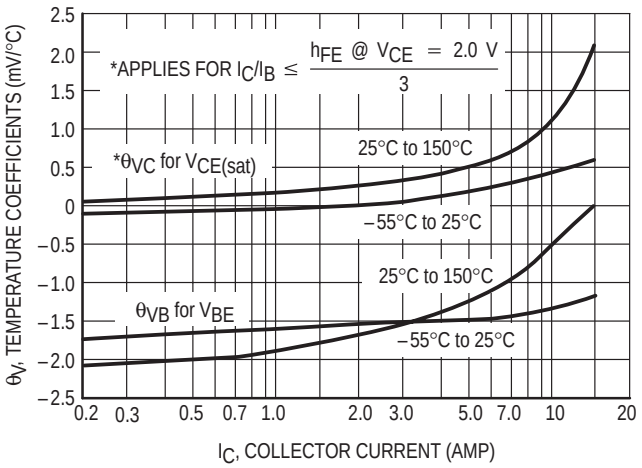


Figure 4. Temperature Coefficients

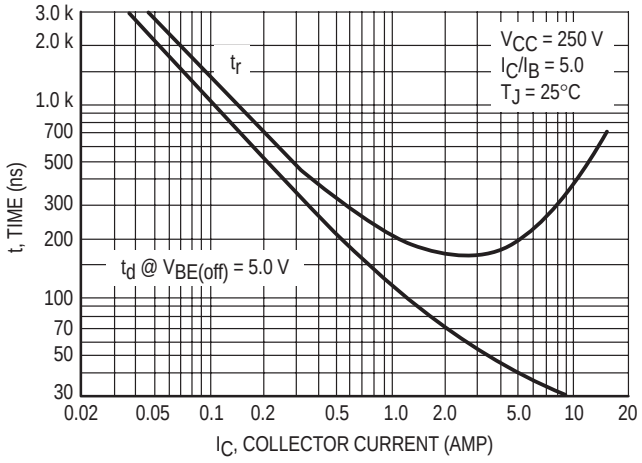


Figure 5. Turn–On Time

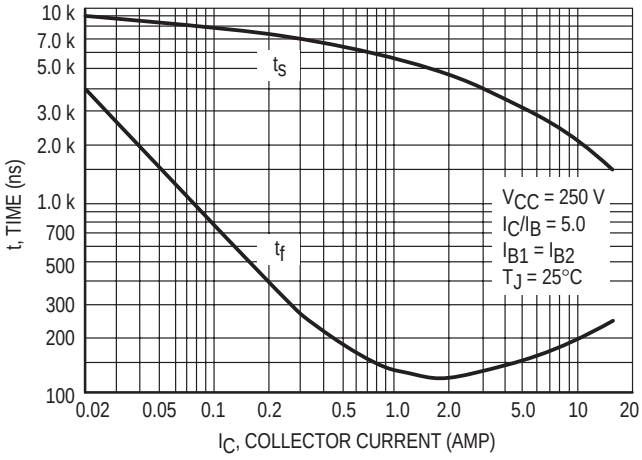


Figure 6. Turn–Off Time

MAXIMUM RATED SAFE OPERATING AREAS

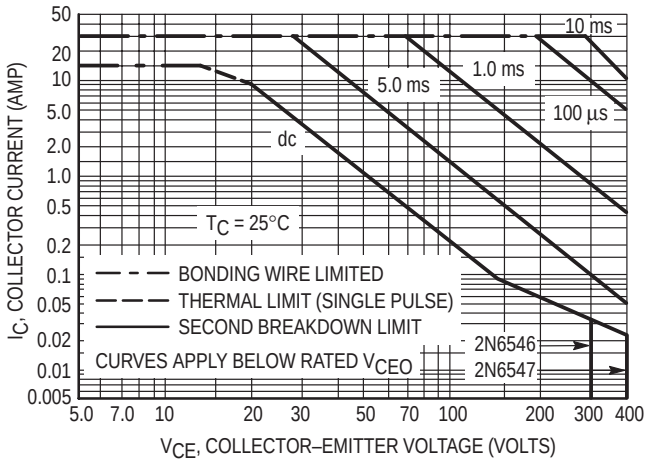


Figure 7. Forward Bias Safe Operating Area

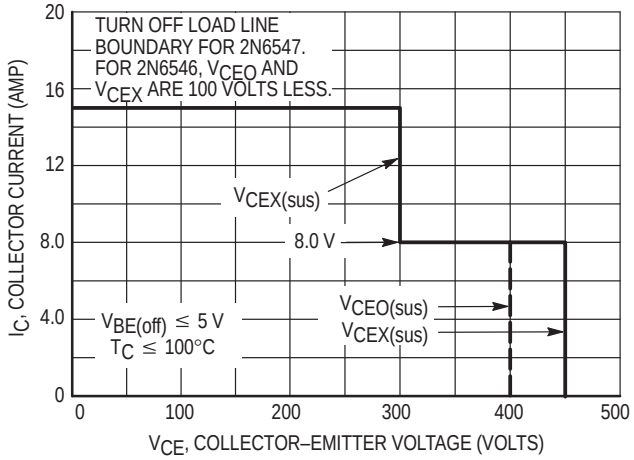


Figure 8. Reverse Bias Safe Operating Area

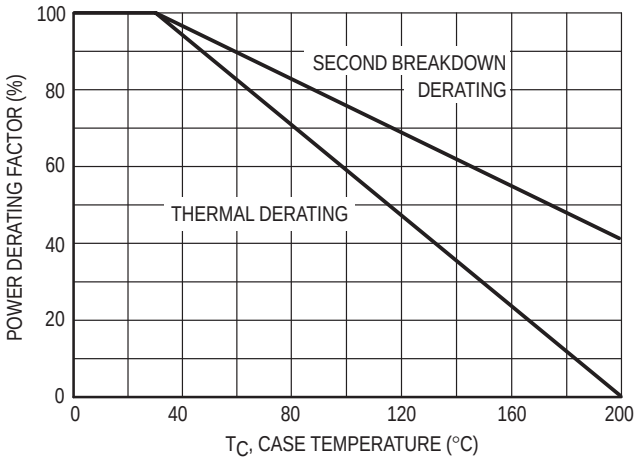


Figure 9. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

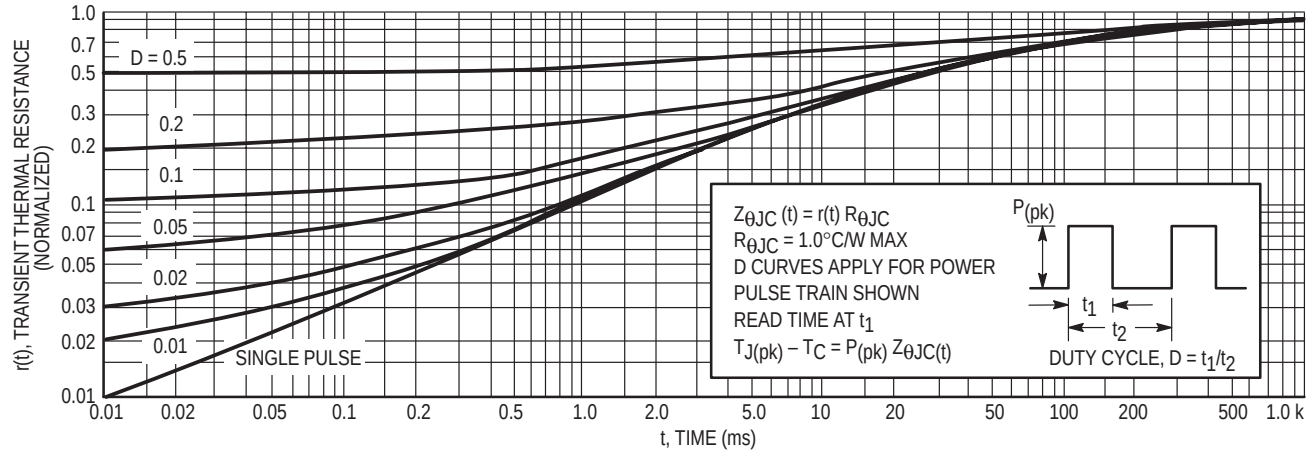


Figure 10. Thermal Response

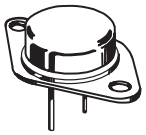
2N6576
2N6577
2N6578

NPN Silicon Power Darlington Transistors

15 AMPERE
POWER TRANSISTORS
NPN SILICON
DARLINGTON
60, 90, 120 VOLTS
120 WATTS

General–purpose EpiBase power Darlington transistors, suitable for linear and switching applications.

- Replacement for 2N3055 and Driver
- High Gain Darlington Performance
- Built–in Diode Protection for Reverse Polarity Protection
- Can Be Driven from Low–Level Logic
- Popular Voltage Range
- Operating Range — –65 to +200°C



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (1)

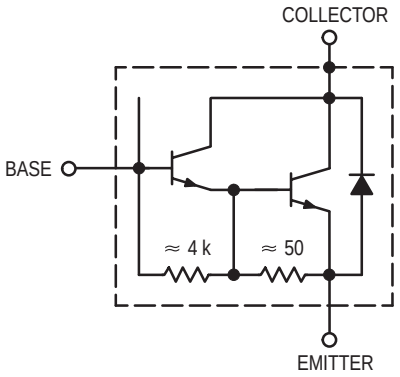
Rating	Symbol	2N6576	2N6577	2N6578	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	60	90	120	Vdc
Collector–Base Voltage	V_{CB}	60	90	120	Vdc
Emitter–Base Voltage	V_{EB}	7.0			Vdc
Collector Current — Continuous — Peak	I_C	15 30			Adc
Base Current — Continuous — Peak	I_B	0.25 0.50			Adc
Emitter Current — Continuous — Peak	I_E	15.25 30.5			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 120 0.685			 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.46	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16″ from Case for 10s.	T_L	265	°C

(1) Indicates JEDEC Registered Data.

DARLINGTON SCHEMATIC



REV 7

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	2N6576		60	—	
	2N6577		90	—	
	2N6578		120	—	
Collector Cutoff Current (V_{CE} = Rated Value)		I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CER} = Rated $V_{CEO(sus)}$ Value, R_{BE} = 10 kΩ, T_C = 150°C)		I_{CER}	—	5.0	mAdc
Collector Cutoff Current V_{CEX} = Rated $V_{CEO(sus)}$ Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	—	5.0	mAdc
Collector Cutoff Current (V_{CB} = Rated Value)		I_{CBO}	—	0.5	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			—
(I_C = 15 Adc, V_{CE} = 4.0 Vdc)			100	—	
(I_C = 10 Adc, V_{CE} = 3.0 Vdc)			500	5,000	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			2000	20,000	
(I_C = 0.4 Adc, V_{CE} = 3.0 Vdc)			200	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 15 Adc, I_B = 0.15 Adc)			—	4.0	
(I_C = 10 Adc, I_B = 0.1 Adc)			—	2.8	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 15 Adc, I_B = 0.15 Adc)			—	4.5	
(I_C = 10 Adc, I_B = 0.1 Adc)			—	3.5	
Collector–Emitter Diode Voltage Drop (I_{EC} = 15 Adc)		VF	—	4.5	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common–Emitter Small–Signal Short–Circuit Current Transfer Ratio (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	10	200	—

SWITCHING CHARACTERISTICS
RESISTIVE LOAD (Figure 2)

Delay Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = 0.1 Adc, t_p = 300 μs, Duty Cycle ≤ 2.0%)	t_d	—	0.15	μs
Rise Time		t_r	—	1.0	μs
Storage Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 0.1 Adc, t_p = 300 μs, Duty Cycle ≤ 2.0%)	t_s	—	2.0	μs
Fall Time		t_f	—	7.0	μs

* Indicates JEDEC Registered Data
(1) Pulse test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

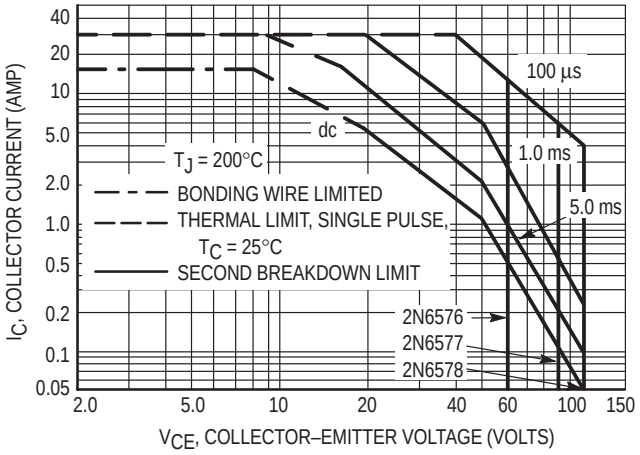


Figure 1. Rated Forward Biased Safe–Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%.

$T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

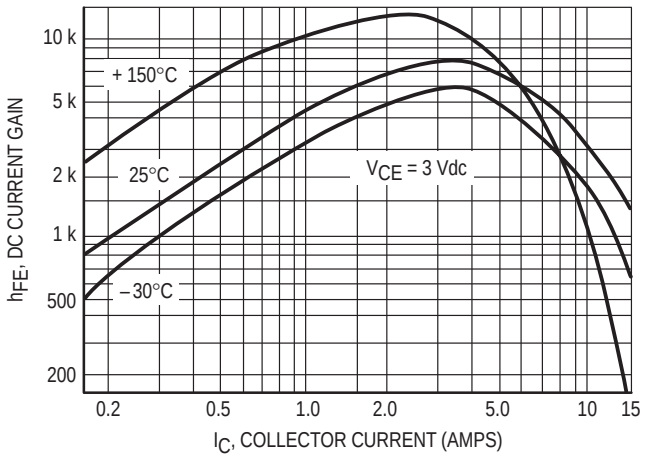


Figure 2. DC Current Gain

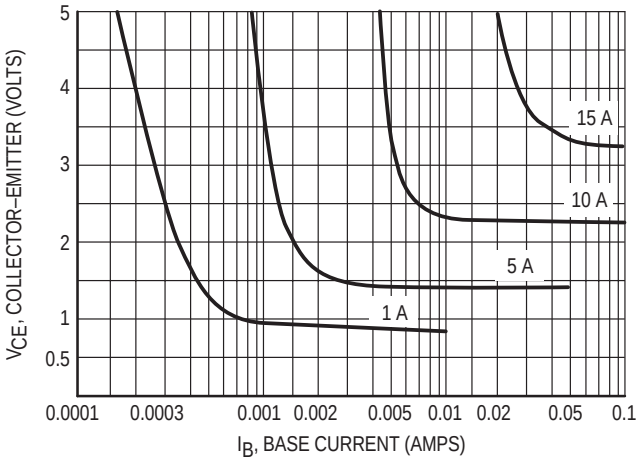


Figure 3. Collector Saturation Region

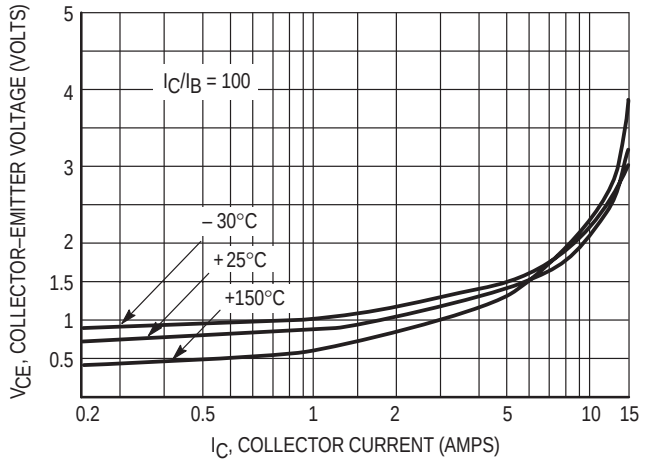


Figure 4. Collector Saturation Voltage

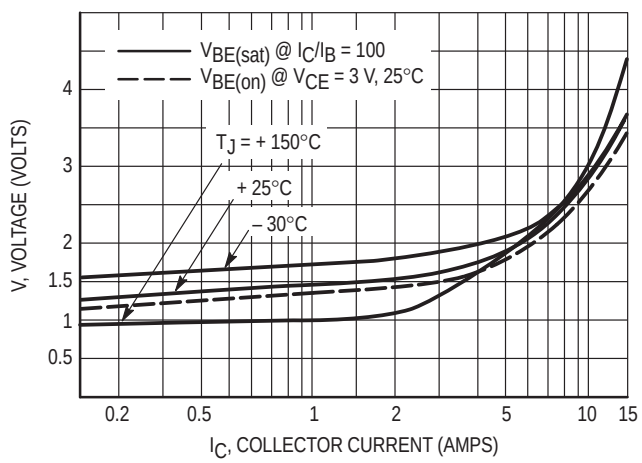


Figure 5. Base–Emitter Voltage

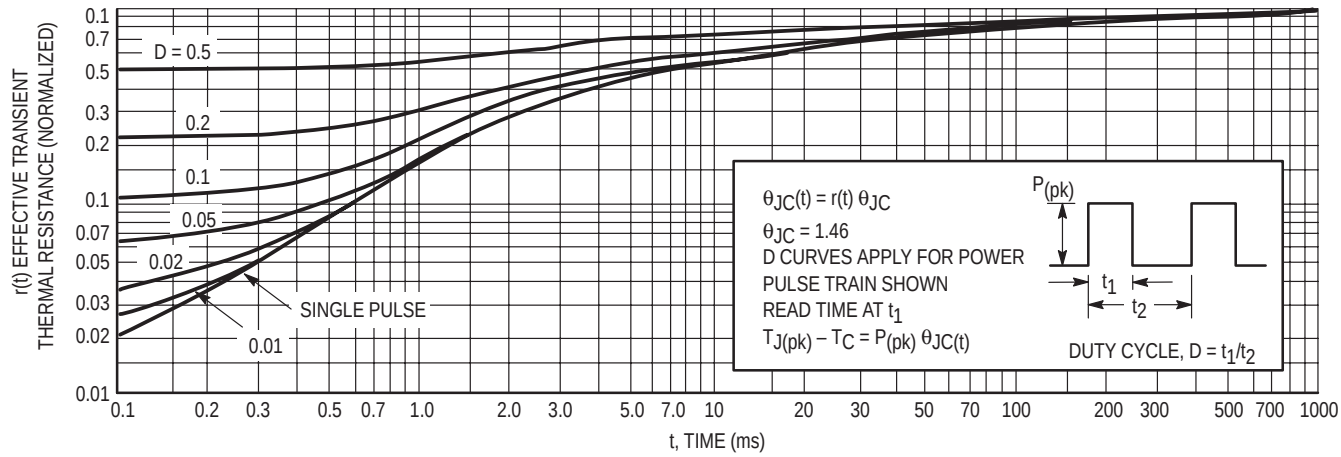


Figure 6. Thermal Response

2N6609
(See 2N3773)

Darlington Silicon Power Transistors

2N6667
2N6668

. . . designed for general–purpose amplifier and low speed switching applications.

- High DC Current Gain — h_{FE} = 3500 (Typ) @ I_C = 4 Adc
- Collector–Emitter Sustaining Voltage — @ 200 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — 2N6667
  = 80 Vdc (Min) — 2N6668
- Low Collector–Emitter Saturation Voltage — $V_{CE(sat)}$ = 2 Vdc (Max) @ I_C = 5 Adc
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors
- TO–220AB Compact Package
- Complementary to 2N6387, 2N6388

PNP SILICON
DARLINGTON
POWER TRANSISTORS
10 AMPERES
60–80 VOLTS
65 WATTS

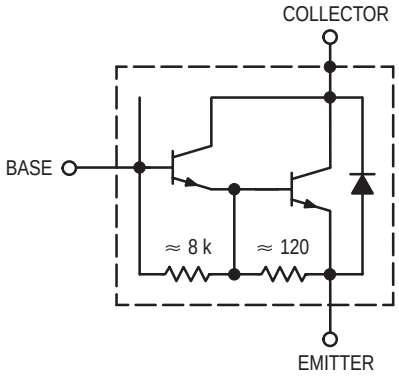
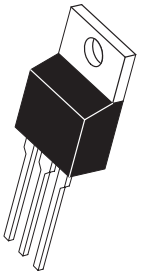


Figure 1. Darlington Schematic



CASE 221A–06
TO–220AB

MAXIMUM RATINGS (1)

Rating	Symbol	2N6667	2N6668	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous — Peak	I_C	10 15		Adc
Base Current	I_B	250		mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	65 0.52		watts W/°C
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 0.016		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) Indicates JEDEC Registered Data.

REV 1

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	2N6667 2N6668	$V_{CEO(sus)}$	60 80	— —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	2N6667 2N6668	I_{CEO}	— —	1 1	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	 2N6667 2N6668 2N6667 2N6668	I_{CEX}	 — — — —	 300 300 3 3	 µAdc mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	5	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5 Adc, V_{CE} = 3 Vdc) (I_C = 10 Adc, V_{CE} = 3 Vdc)		h_{FE}	1000 100	20000 —	—
Collector–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.01 Adc) (I_C = 10 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	— —	2 3	Vdc
Base–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.01 Adc) (I_C = 10 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$	— —	2.8 4.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)		$\|h_{fe}\|$	20	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}	—	200	pF
Small–Signal Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc, f = 1 kHz)		h_{fe}	1000	—	—

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

R_B & R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1, MUST BE FAST RECOVERY TYPES e.g.,
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

FOR t_d AND t_r, D_1 IS DISCONNECTED AND V_2 = 0

t_r, $t_f \leq$ 10 ns
DUTY CYCLE = 1.0%

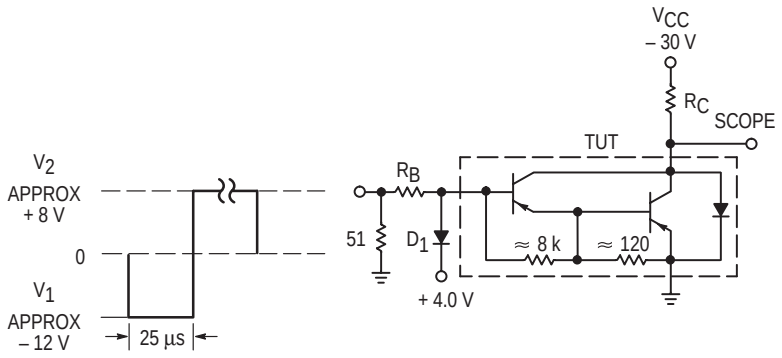


Figure 2. Switching Times Test Circuit

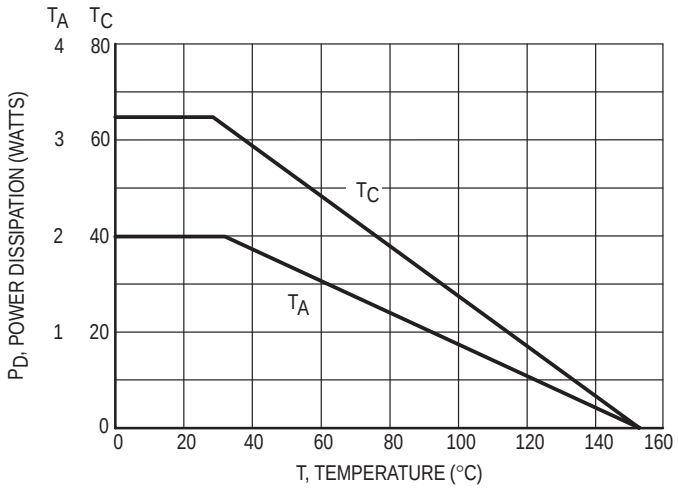


Figure 3. Power Derating

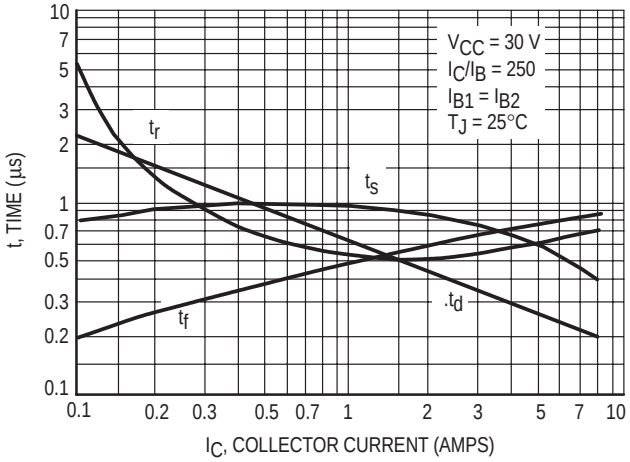


Figure 4. Typical Switching Times

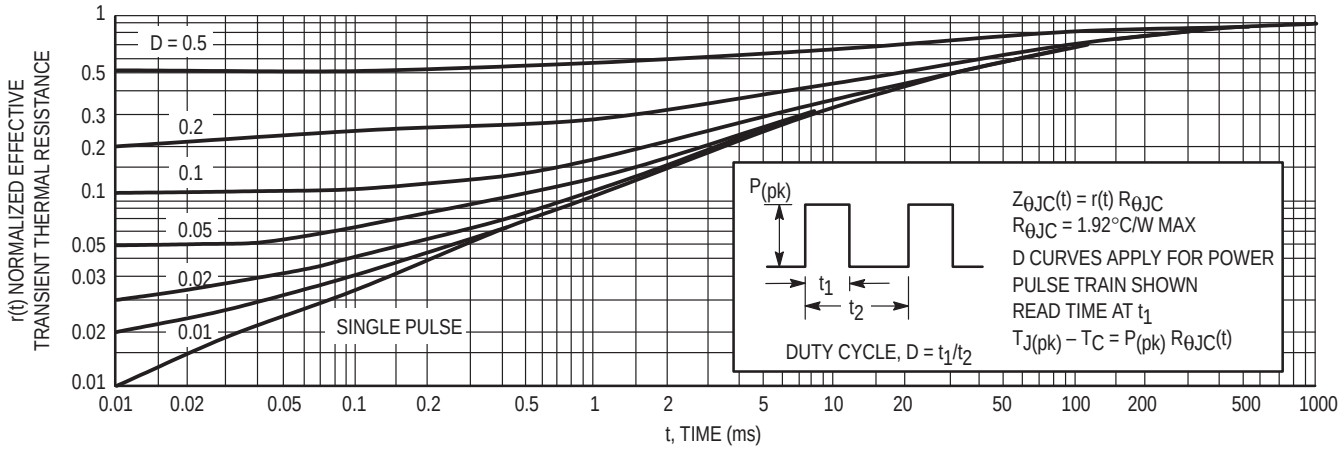


Figure 5. Thermal Response

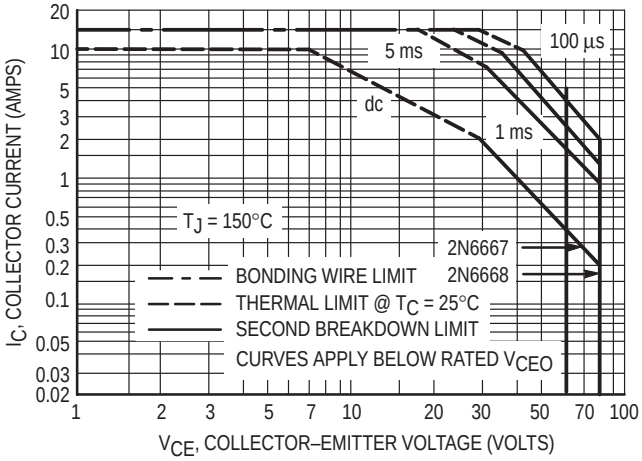


Figure 6. Maximum Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

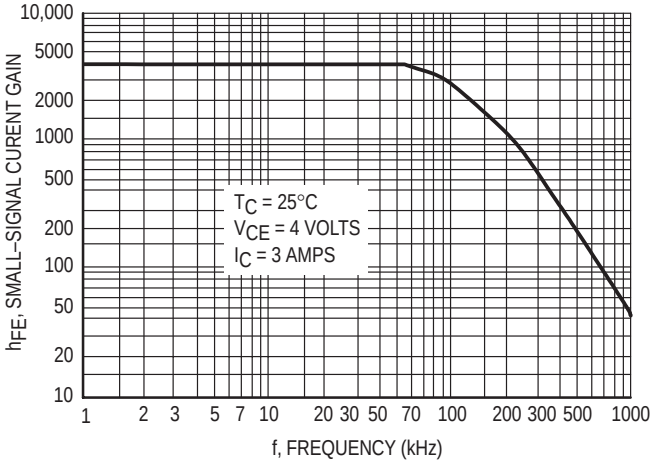


Figure 7. Typical Small–Signal Current Gain

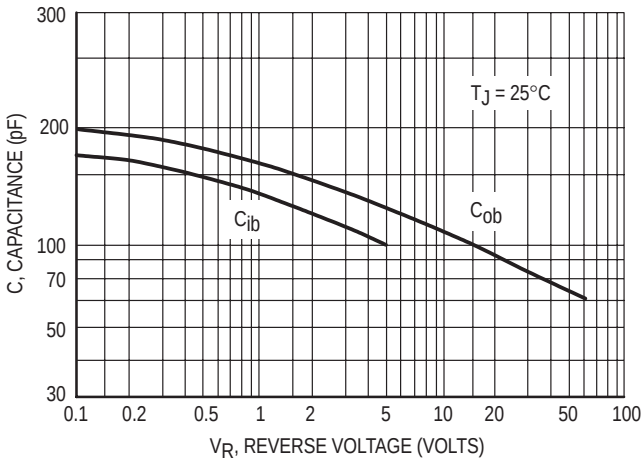


Figure 8. Typical Capacitance

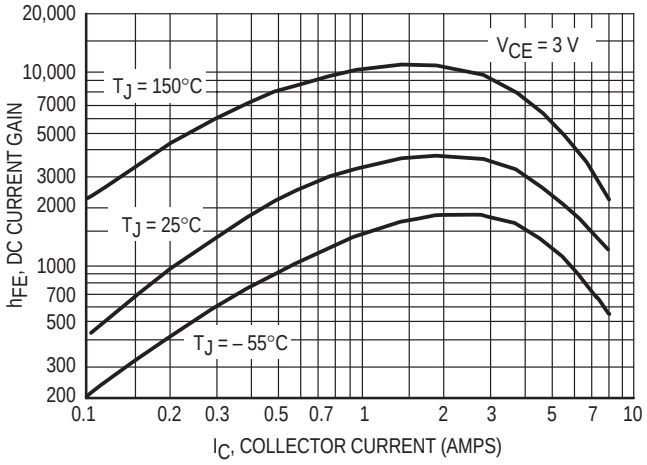


Figure 9. Typical DC Current Gain

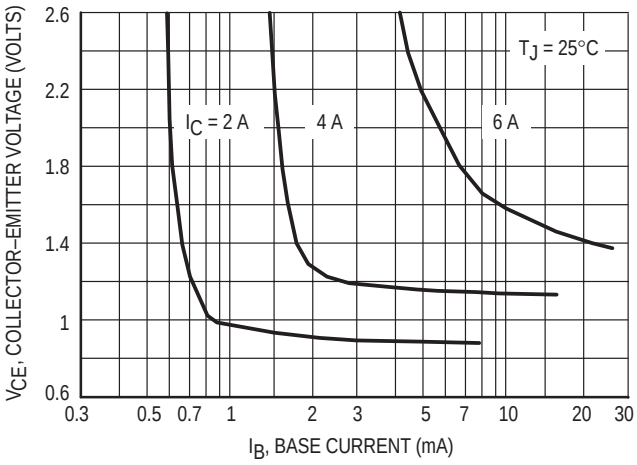


Figure 10. Typical Collector Saturation Region

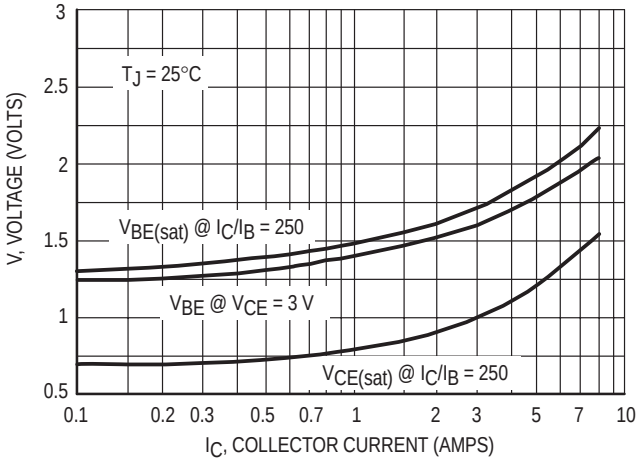


Figure 11. Typical “On” Voltages

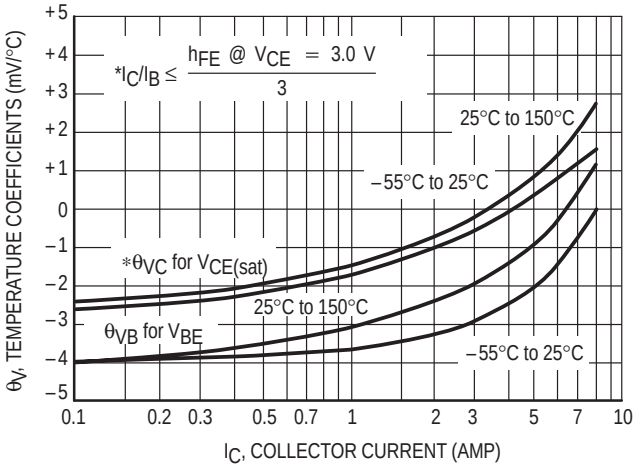


Figure 12. Typical Temperature Coefficients

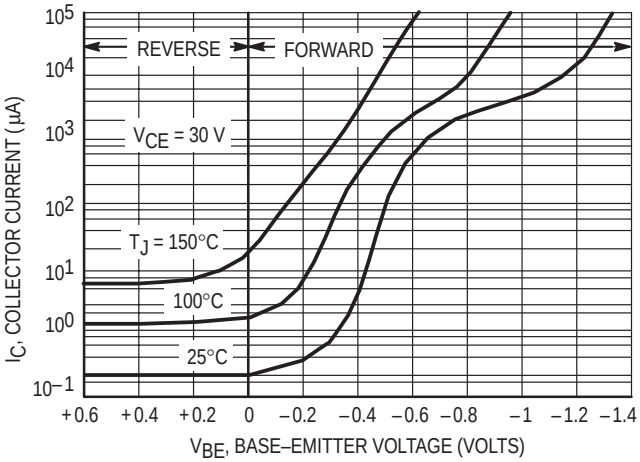


Figure 13. Typical Collector Cut–Off Region

2N6836

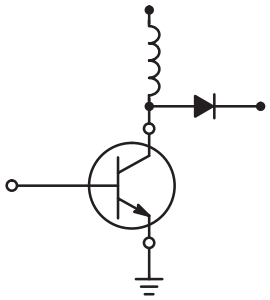
Designer's™ Data Sheet

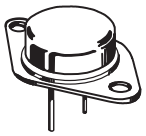
Switchmode Series Ultra-Fast NPN Silicon Power Transistors

15 AMPERE
NPN SILICON
POWER TRANSISTOR
450 VOLTS
175 WATTS

These transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated switchmode applications.

- Switching Regulators
- Inverters
- Motor Controls
- Deflection Circuits
- Fast Turn–Off Times
  - 30 ns Inductive Fall Time — 75°C (Typ)
  - 50 ns Inductive Crossover Time — 75°C (Typ)
  - 600 ns Inductive Storage Time — 75°C (Typ)
- Operating Temperature Range –65 to +200°C
- 100°C Performance Specified for:
  - Reverse–Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents





CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (2)

Rating	Symbol	Max	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector–Emitter Voltage	V_{CEV}	850	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 20	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 15	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS (2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5.0 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Indicate JEDEC Registered Data.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)							
Collector–Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)			$V_{CEO(sus)}$	450*	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			I_{CEV}	 — —	 — —	 0.25* 1.5*	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)			I_{EBO}	—	—	1.0*	mAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$	See Figure 15*			
Clamped Inductive SOA with Base Reverse Biased			RBSOA	See Figure 16			
ON CHARACTERISTICS (1)							
Collector–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.7 Adc) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 1.0 Adc, T_C = 100°C)			$V_{CE(sat)}$	 — — —	 — — —	 1.2 2.5* 3.0*	Vdc
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 1.0 Adc, T_C = 100°C)			$V_{BE(sat)}$	 — —	 — —	 1.5* 1.5	Vdc
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc) (I_C = 15 Adc, V_{CE} = 5.0 Vdc)			h_{FE}	 8.0* 5.0	 — —	 30* —	—
DYNAMIC CHARACTERISTICS (2)							
Current Gain — Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.25 Adc, f_{test} = 10 MHz)			f_T	10*	—	75*	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)			C_{ob}	50*	—	400*	pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	(I_C = 10 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.0 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%)	(I_{B2} = 2.6 Adc, R_{B2} = 1.6 Ω)	t_d	—	20	100*	ns
Rise Time			t_r	—	200	500*	
Storage Time			t_s	—	1200	3000*	
Fall Time			t_f	—	200	250*	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	650	—	
Fall Time			t_f	—	80	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 10 Adc, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	800	1500*	ns
Fall Time			t_{fi}	—	50	150*	
Crossover Time			t_c	—	90	200*	
Storage Time		(T_C = 150°C)	t_{sv}	—	1050	—	
Fall Time			t_{fi}	—	70	—	
Crossover Time			t_c	—	120	—	

(1) Pulse Test: PW ± 300 μs, Duty Cycle ≤ 2%.
(2) $f_T = |h_{fe}| f_{test}$.
* Indicates JEDEC Registered Limit.

TYPICAL STATIC CHARACTERISTICS

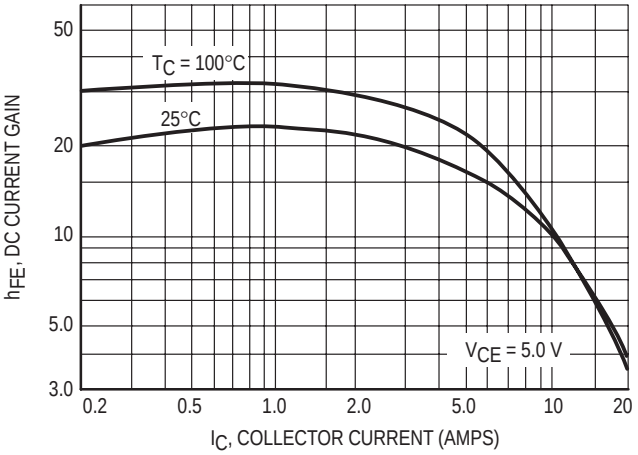


Figure 1. DC Current Gain

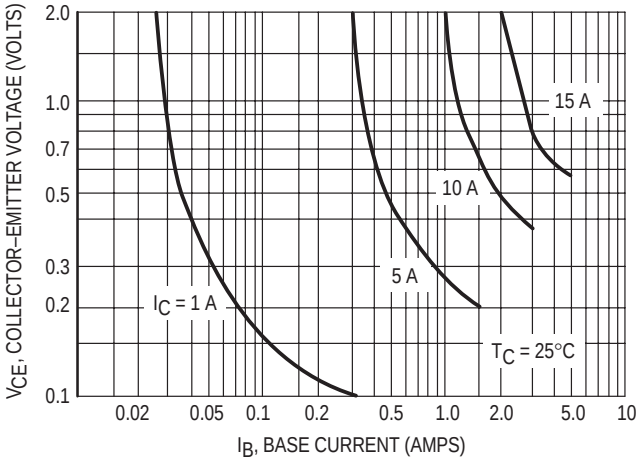


Figure 2. Collector Saturation Region

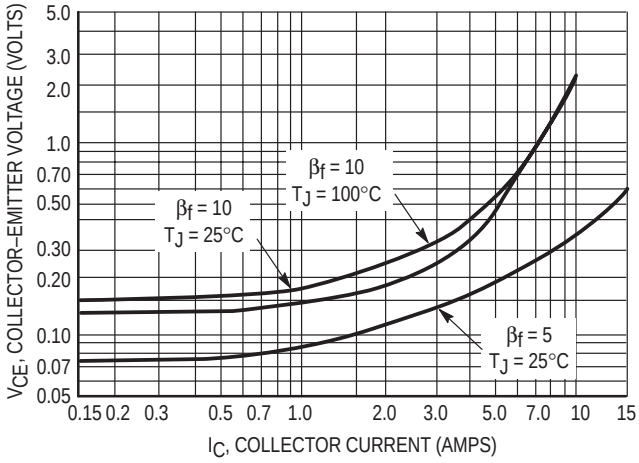


Figure 3. Collector–Emitter Saturation Voltage

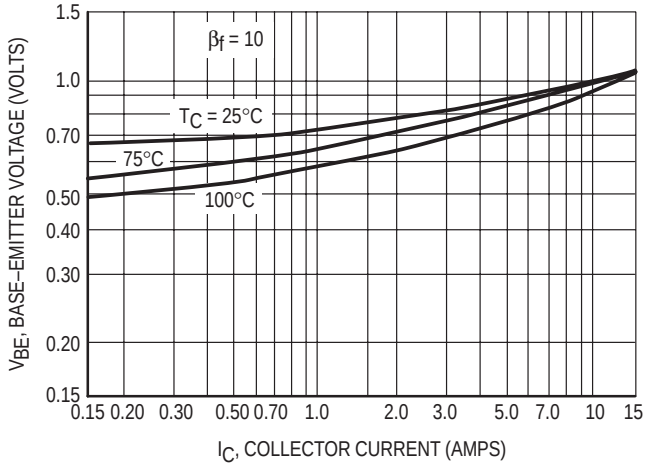


Figure 4. Base–Emitter Voltage

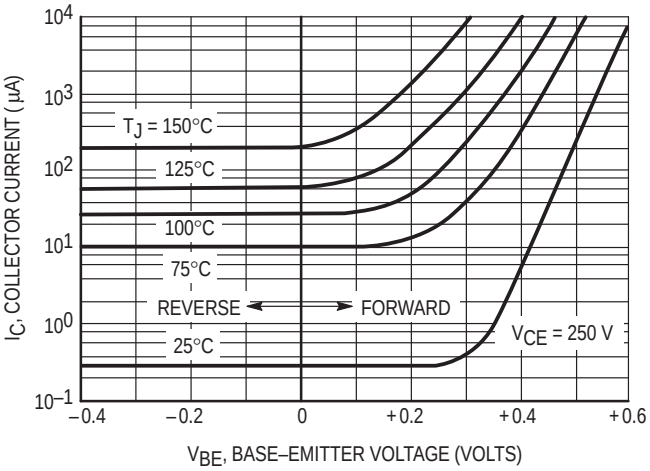


Figure 5. Collector Cutoff Region

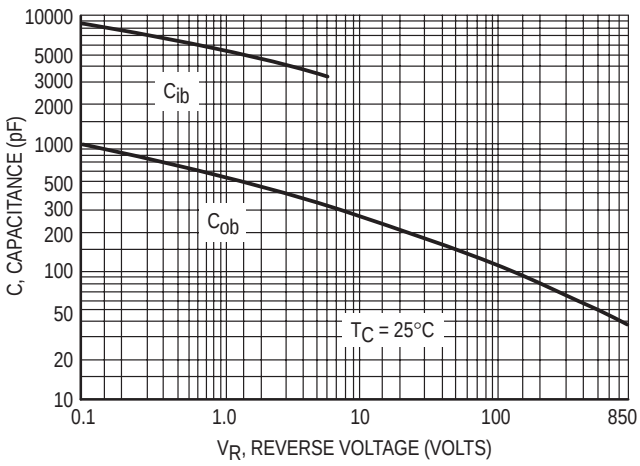


Figure 6. Capacitance

TYPICAL DYNAMIC CHARACTERISTICS

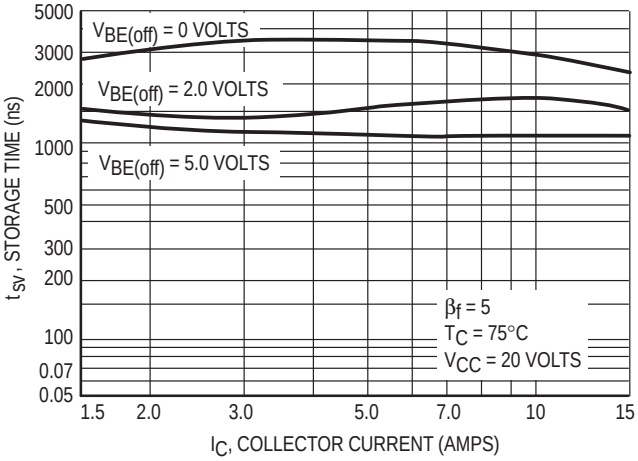


Figure 7. Storage Time

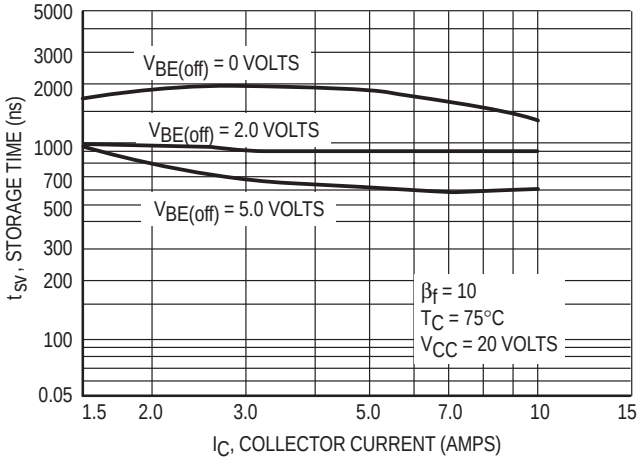


Figure 8. Storage Time

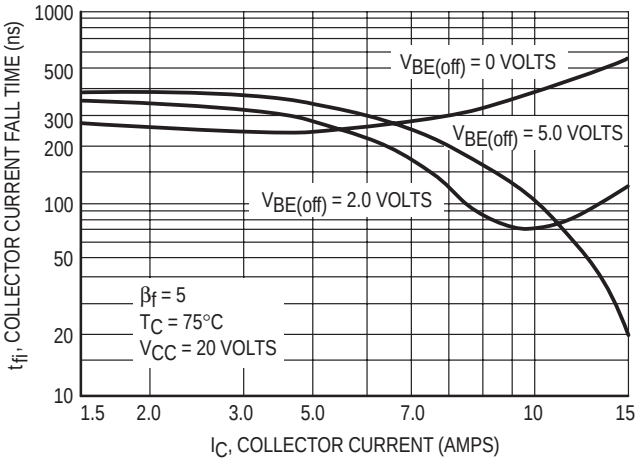


Figure 9. Collector Current Fall Time

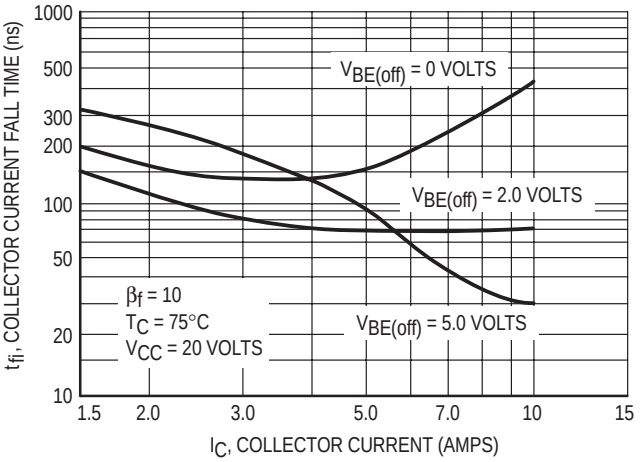


Figure 10. Collector Current Fall Time

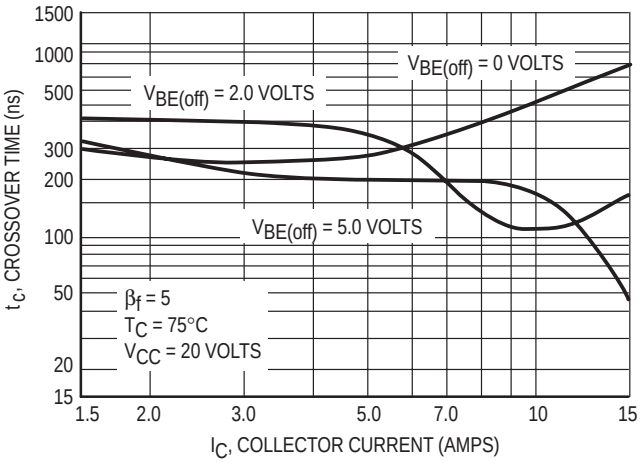


Figure 11. Crossover Time

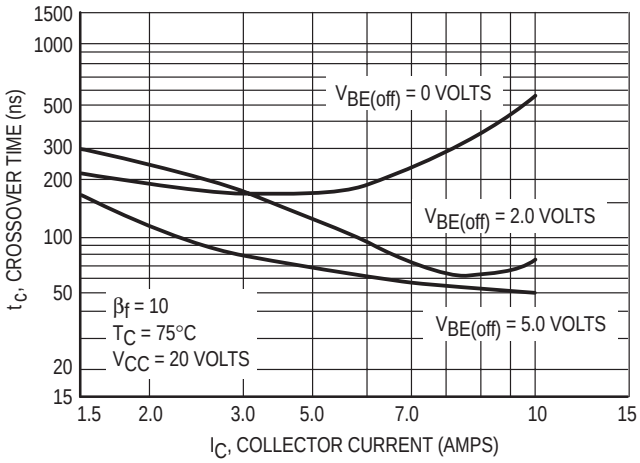


Figure 12. Crossover Time

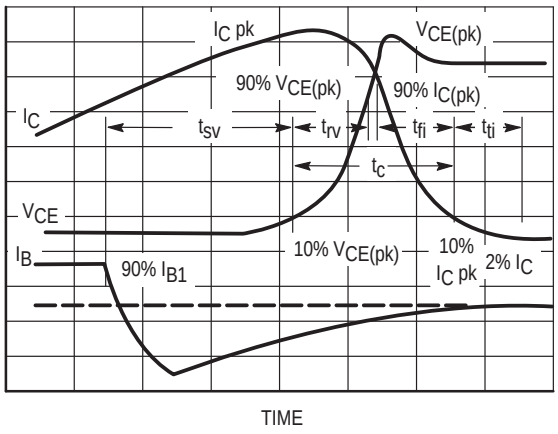


Figure 13. Inductive Switching Measurements

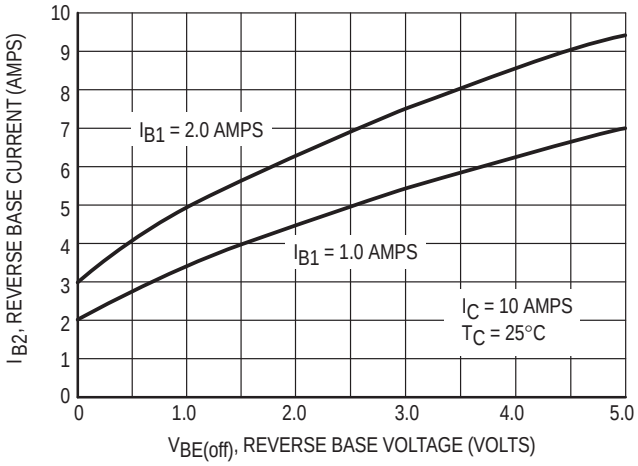


Figure 14. Peak Reverse Base Current

GUARANTEED SAFE OPERATING AREA LIMITS

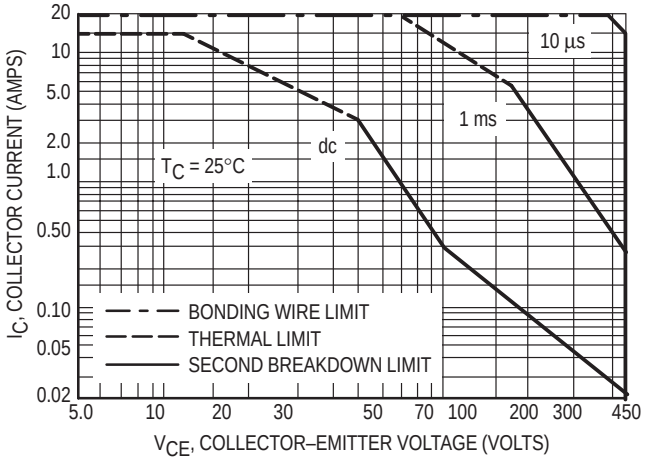


Figure 15. Maximum Forward Bias Safe Operating Area

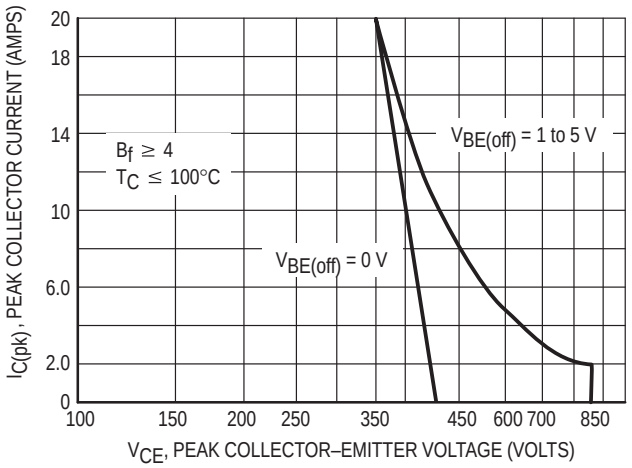


Figure 16. Maximum Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, R_C snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

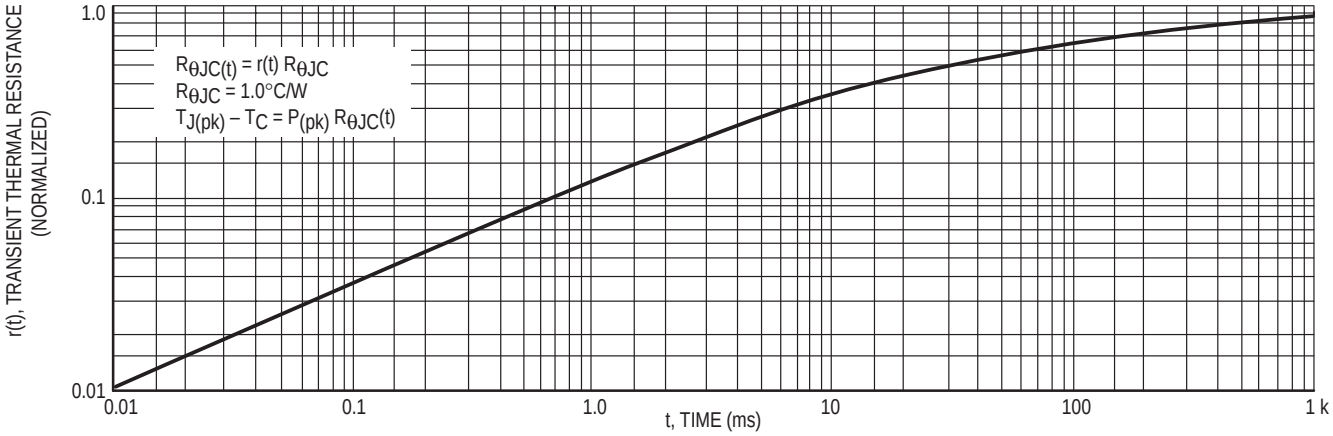


Figure 17. Thermal Response

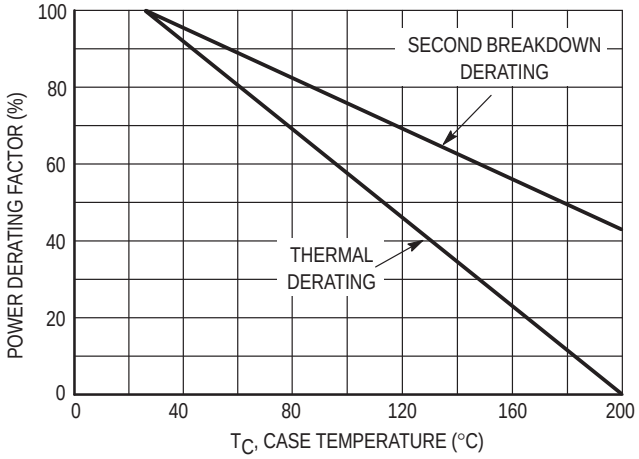
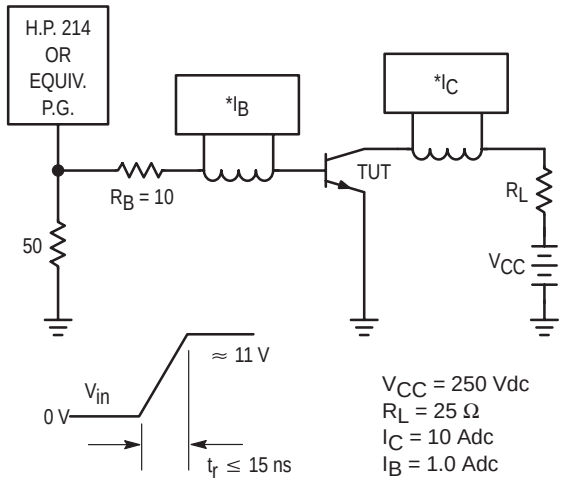


Figure 18. Power Derating

Table 1. Resistive Load Switching

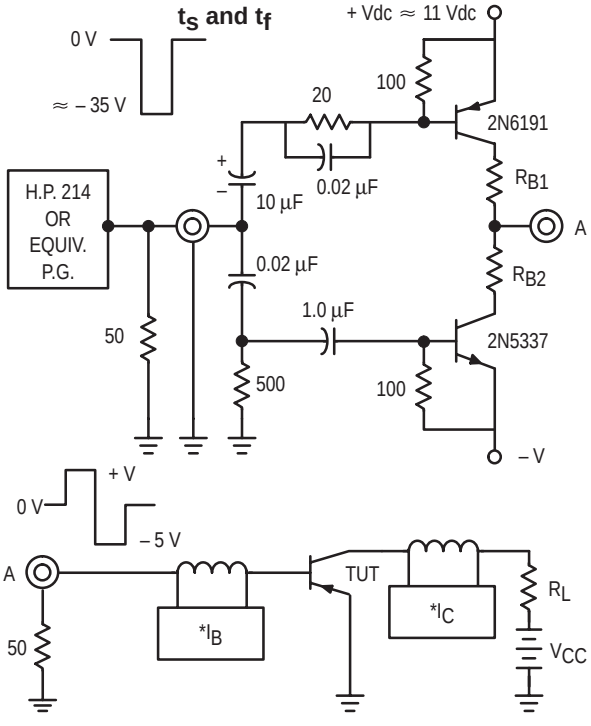
t_d and t_r



V_{CC} = 250 Vdc
R_L = 25 Ω
I_C = 10 Adc
I_B = 1.0 Adc

*Tektronix P–6042 or equivalent.

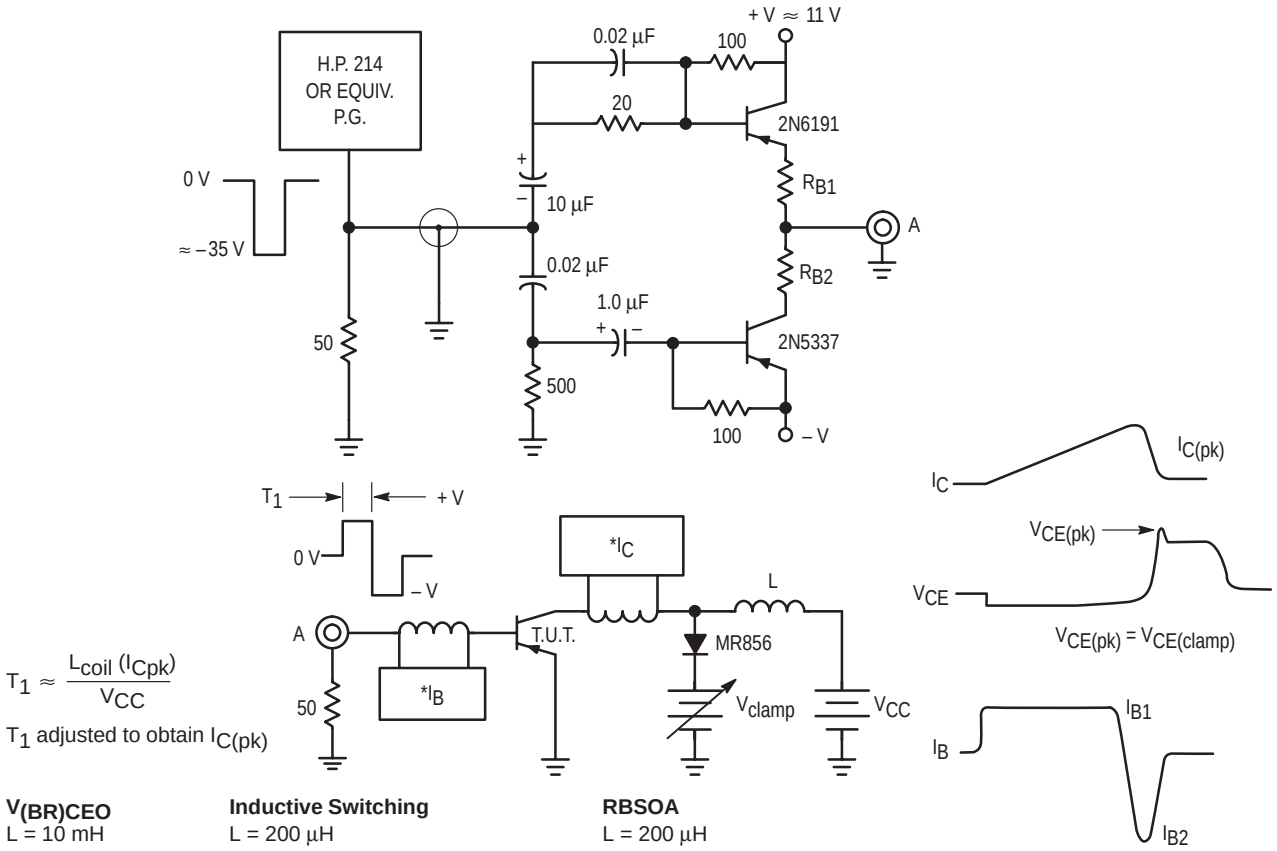
t_s and t_f



V_{CC} = 250 Vdc
R_L = 25 Ω
I_C = 10 Adc
I_{B1} = 1.0 Adc
I_{B2} = 2.6 Adc
For $V_{BE(off)}$ = 5.0 V
R_{B1} = 10 Ω
R_{B2} = 1.6 Ω
R_{B2} = 0 Ω

*NOTE: Adjust – V to obtain desired $V_{BE(off)}$ at Point A.

Table 2. Inductive Load Switching



$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$	**Inductive Switching**	**RBSOA**
L = 10 mH	L = 200 μH	L = 200 μH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 20 Volts	V_{CC} = 20 Volts
	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

*Tektronix P–6042 or Equivalent

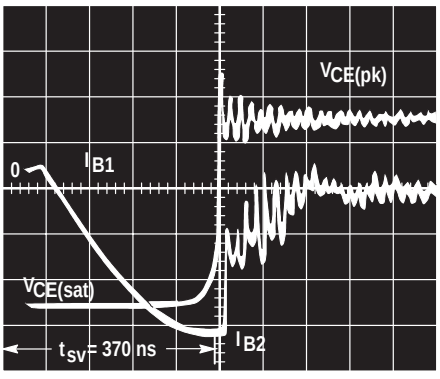
Scope — Tektronix 7403 or Equivalent

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

TYPICAL INDUCTIVE SWITCHING WAVEFORMS

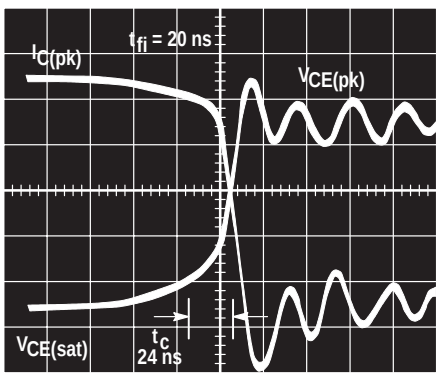
t_{sv}

$I_{C(pk)}$ = 10 Amps
I_{B1} = 1.0 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 400 Volts
T_C = 25°C
Time Base = 100 ns/cm



t_{fi}, t_c

$I_{C(pk)}$ = 10 Amps
I_{B1} = 1.0 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 400 Volts
T_C = 25°C
Time Base = 20 ns/cm



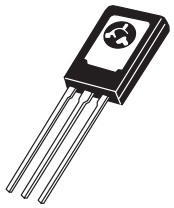
BD135
BD137
BD139

Plastic Medium Power Silicon NPN Transistor

. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 135, 137, 139 are complementary with BD 136, 138, 140

1.5 AMPERE
POWER TRANSISTORS
NPN SILICON
45, 60, 80 VOLTS
10 WATTS



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector–Emitter Voltage	V_{CEO}	BD 135 BD 137 BD 139	45 60 80	Vdc
Collector–Base Voltage	V_{CBO}	BD 135 BD 137 BD 139	45 60 100	Vdc
Emitter–Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		12.5 100	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unlt
Collector–Emitter Sustaining Voltage* (I_C = 0.03 Adc, I_B = 0)	BV_{CEO}*	BD 135 BD 137 BD 139	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_C = 125°C)	I_{CBO}		— —	0.1 10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	10	μAdc
DC Current Gain (I_C = 0.005 A, V_{CE} = 2 V) (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A V_{CE} = 2 V)	h_{FE}*		25 40 25	— 250 —	—
Collector–Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*		—	0.5	Vdc
Base–Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1	Vdc

* Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

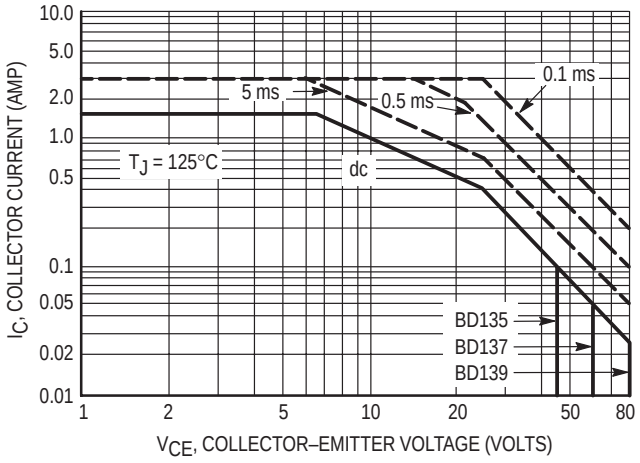


Figure 1. Active–Region Safe Operating Area

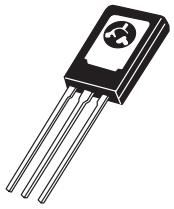
BD136
BD138
BD140
BD140-10

Plastic Medium Power Silicon PNP Transistor

. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 136, 138, 140 are complementary with BD 135, 137, 139

1.5 AMPERE
POWER TRANSISTORS
PNP SILICON
45, 60, 80 VOLTS
10 WATTS



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector–Emitter Voltage	V_{CEO}	BD 136 BD 138 BD 140	45 60 80	Vdc
Collector–Base Voltage	V_{CBO}	BD 136 BD 138 BD 140	45 60 100	Vdc
Emitter–Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation@ T_A = 25°C Derate above 25°C	P_D		1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		12.5 100	Watt mW/°C
Operating and Storage Junction Temperarture Range	T_J, T_{stg}		–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Type	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.03 Adc, I_B = 0)		BV_{CEO}	BD 136 BD 138 BD 140	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_C = 125 °C)		I_{CBO}		— —	0.1 10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}		—	10	μAdc
DC Current Gain (I_C = 0.005 A, V_{CE} = 2 V) (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A, V_{CE} = 2 V)	 ALL ALL BD140–10	h_{FE}*		 25 40 63 25	 — 250 160 —	—
Collector–Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)		$V_{CE(sat)}$*		—	0.5	Vdc
Base–Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$*		—	1	Vdc

* Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

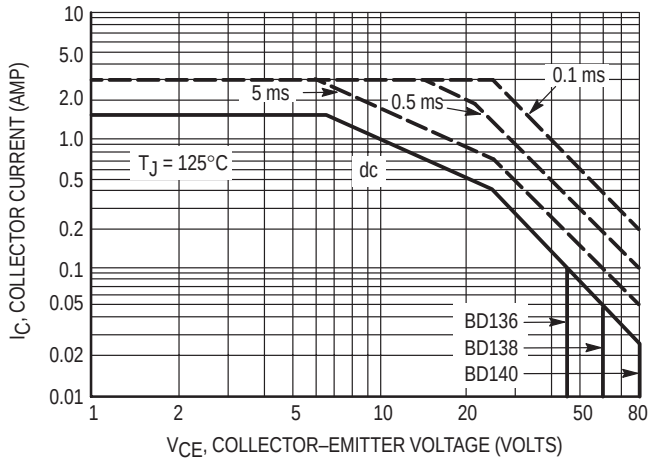


Figure 1. Active–Region Safe Operating Area

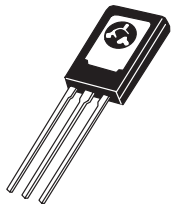
BD157
BD158
BD159

Plastic Medium Power NPN Silicon Transistor

. . . designed for power output stages for television, radio, phonograph and other consumer product applications.

- Suitable for Transformerless, Line–Operated Equipment
- Thermopad† Construction Provides High Power Dissipation Rating for High Reliability

0.5 AMPERE
POWER TRANSISTORS
NPN SILICON
250 – 300 – 350 VOLTS
20 WATTS



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	BD 157	BD 158	BD 159	Unit
Collector–Emitter Voltage	V_{CEO}	250	300	350	Vdc
Collector–Base Voltage	V_{CB}	275	325	375	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	0.5 1.0			Adc
Base Current	I_B	0.25			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	BV_{CEO}	BD 157 BD 158 BD 159	250 300 350	—	Vdc
Collector Cutoff Current (At rated voltage)	I_{CBO}		—	100	μAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	100	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}		30	240	—

REV 7

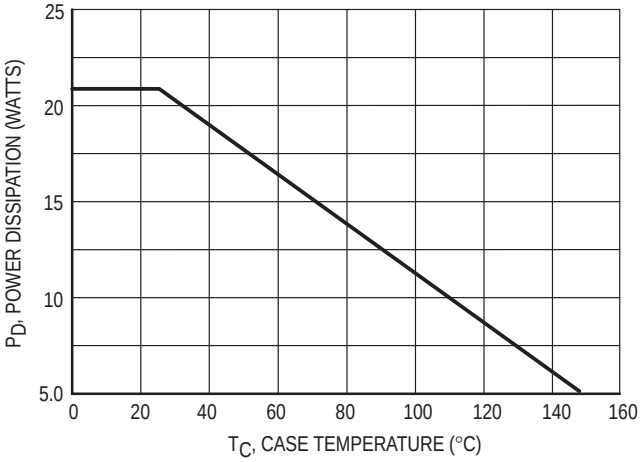


Figure 1. Power–Temperature Derating Curve

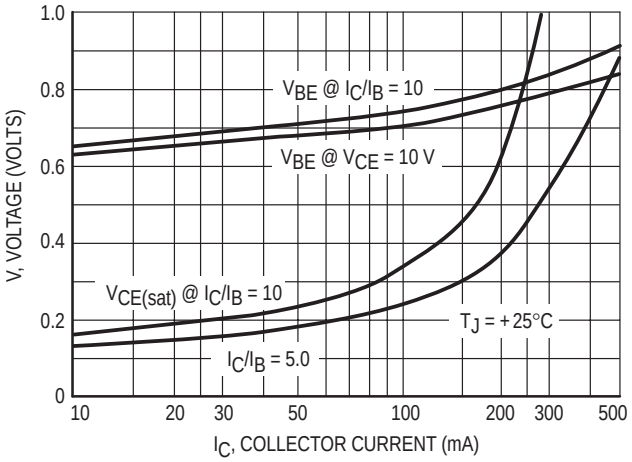


Figure 2. "On" Voltages

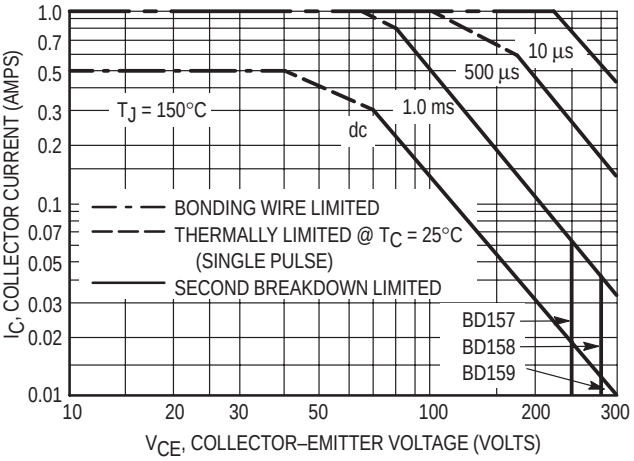


Figure 3. DC Safe Operating Area

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below, the maximum T_J, power–temperature derating must be observed for both steady state and pulse power conditions.

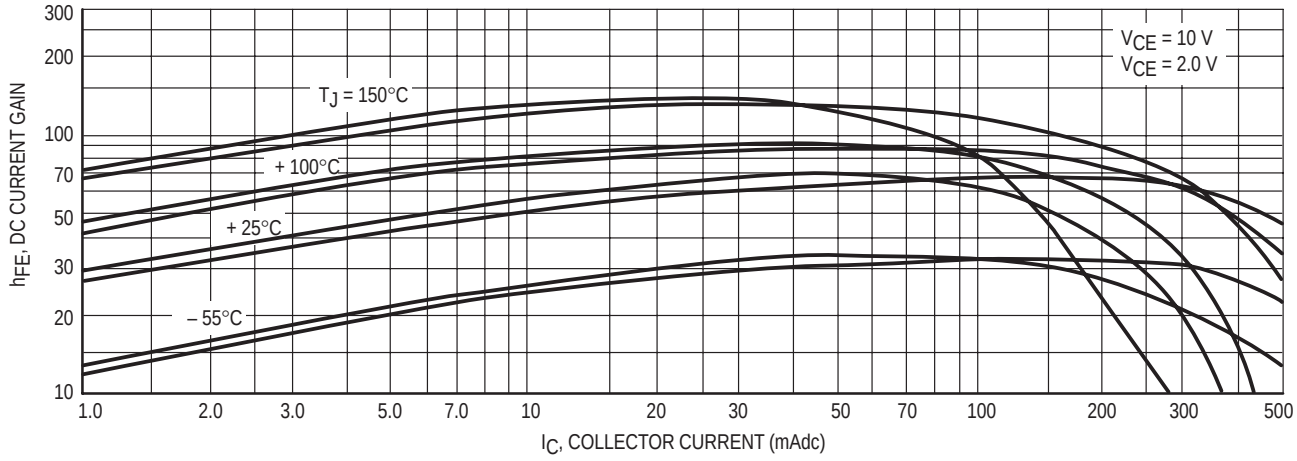


Figure 4. Current Gain

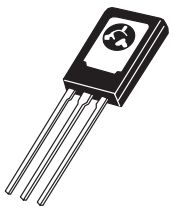
BD165
BD169

Plastic Medium Power Silicon NPN Transistor

. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 165, 169 are complementary with BD 166, 168, 170

1.5 AMPERE
POWER TRANSISTORS
NPN SILICON
45, 60, 80 VOLTS
20 WATTS



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector–Emitter Voltage	V_{CEO}	BD 165 BD 169	45 80	
Collector–Base Voltage	V_{CBO}	BD 165 BD 169	45 80	Vdc
Emitter–Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.25 8	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		20 160	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}	BD 165 BD 169	45 80	— —	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	 BD 165 BD 169	 — —	 0.1 0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	1.0	mAdc
DC current Gain (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A, V_{CE} = 2 V)	h_{FE}*		 40 15	 — —	
Collector–Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*		—	0.5	Vdc
Base–Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	0.95	Vdc
Current Gain–Bandwidth Product (I_C = 500 mAdc, V_{CE} = 2 Vdc, f = 1.0 MHz)	f_T		6.0	—	MHz

* Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

REV 7

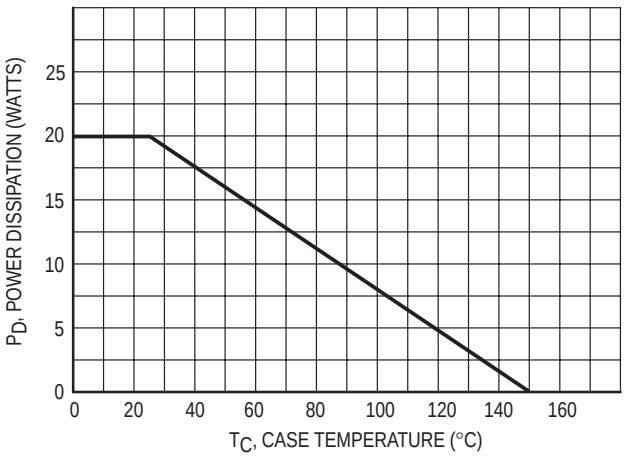


Figure 1. P_D – T_C Derating Curve

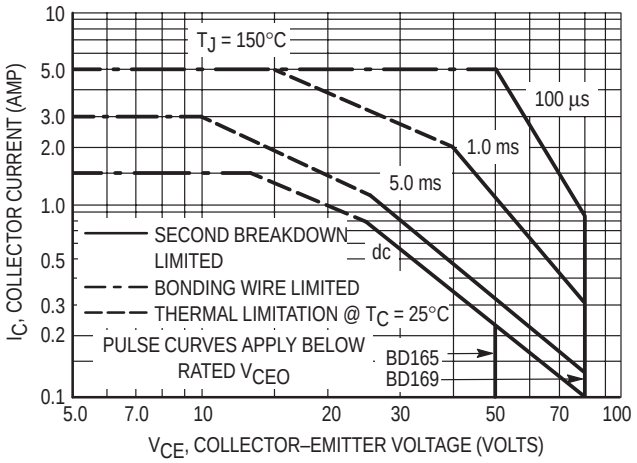


Figure 2. Safe Operating Area (see Note 1)

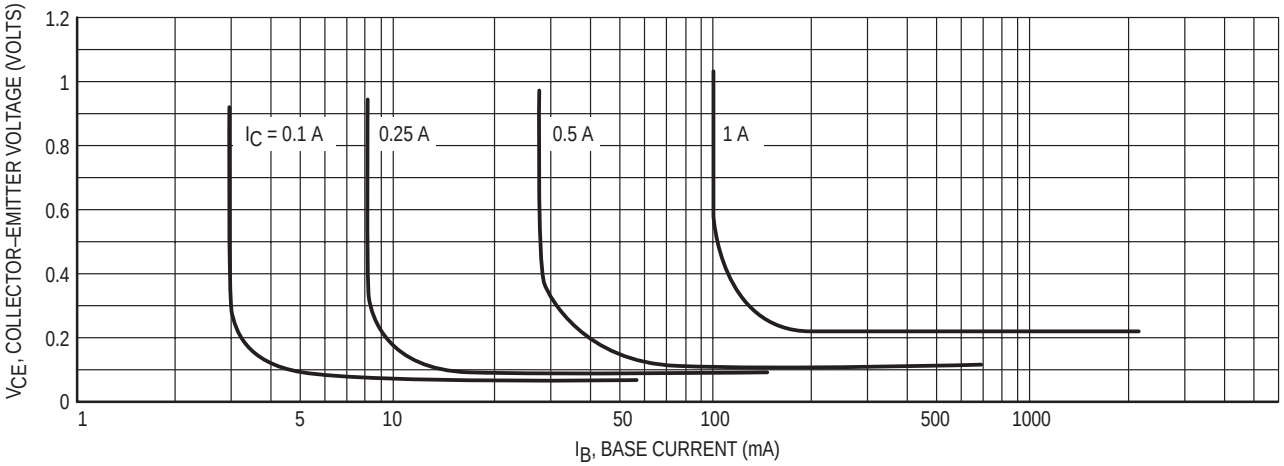


Figure 3. Collector Saturation Region

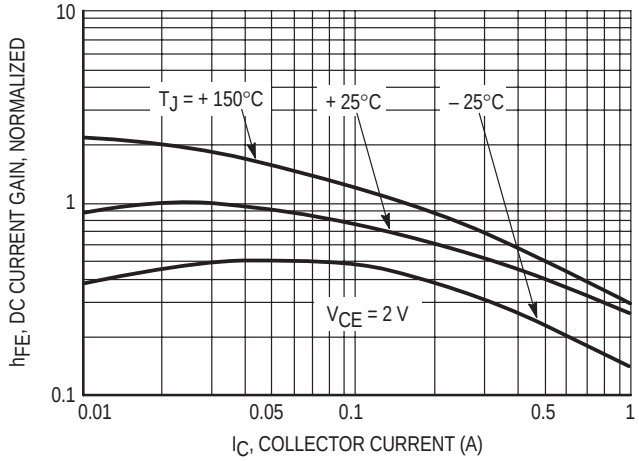


Figure 4. Current Gain

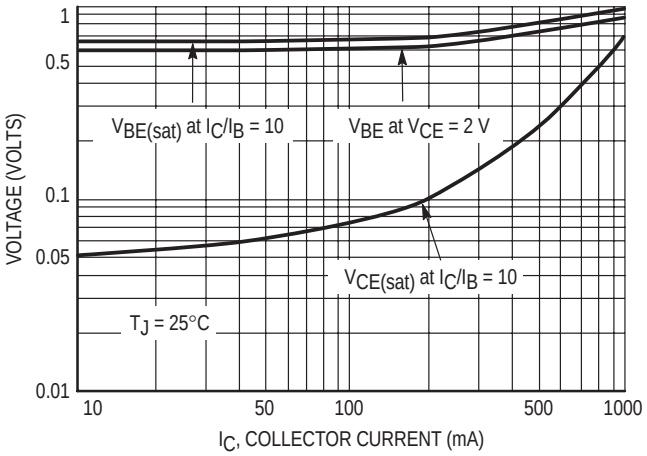


Figure 5. "On" Voltage

Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

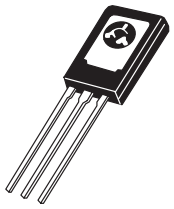
BD166

Plastic Medium Power Silicon PNP Transistor

1.5 AMPERE
POWER TRANSISTOR
PNP SILICON
45 VOLTS
20 WATTS

. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD166 is complementary with BD165



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	45	Vdc
Collector–Base Voltage	V_{CBO}	45	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	1.5	Adc
Base Current	I_B	0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 160	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	$V_{(BR)CEO}$	45	—	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
DC Current Gain (I_C = 0. 15 A, V_{CE} = 2.0 V) (I_C = 0.5 A, V_{CE} = 2.0 V)	h_{FE}	 40 15	 — —	
Collector–Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$	—	0.5	Vdc
Base–Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	0.95	Vdc
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 2.0 Vdc, f = 1.0 MHz)	f_T	6.0	—	MHz

* Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

REV 7

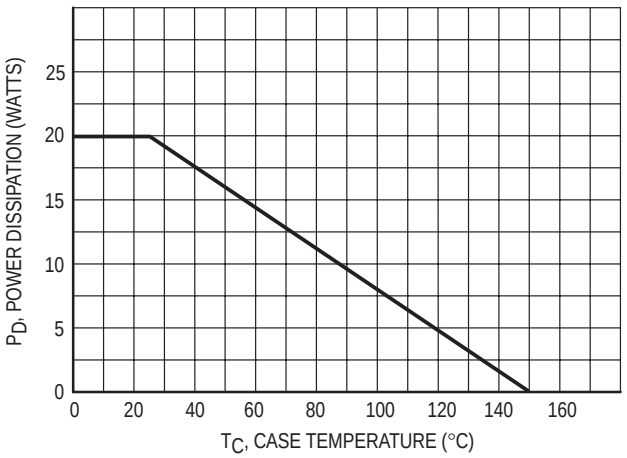


Figure 1. P_D – T_C Derating Curve

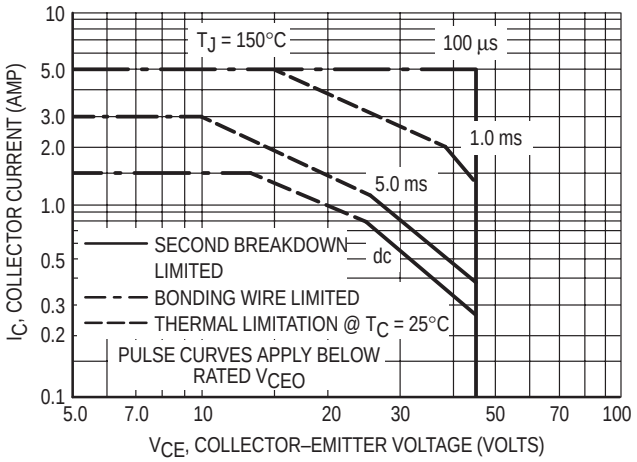


Figure 2. Safe Operating Area (see Note 1)

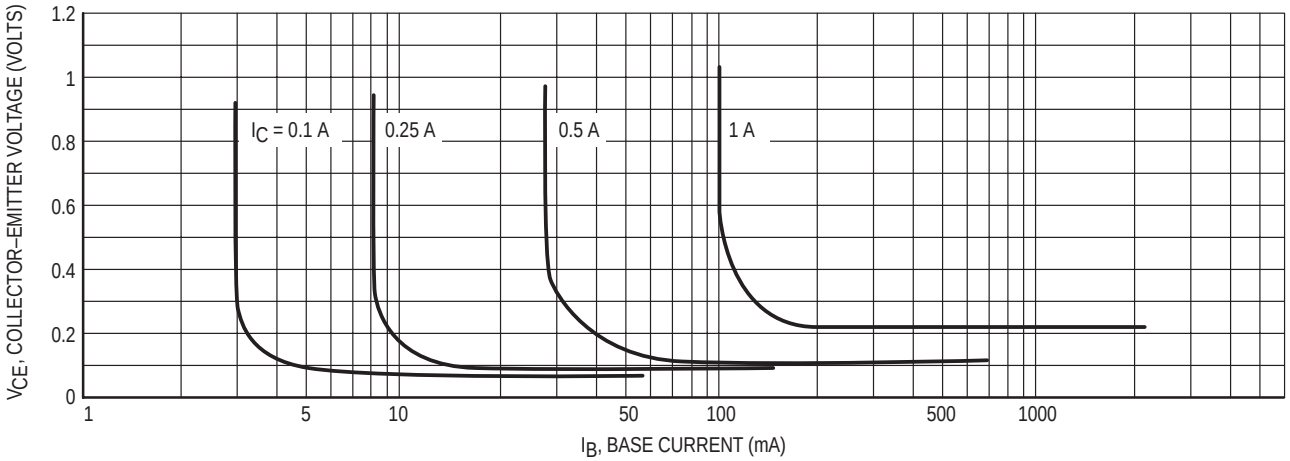


Figure 3. Collector Saturation Region

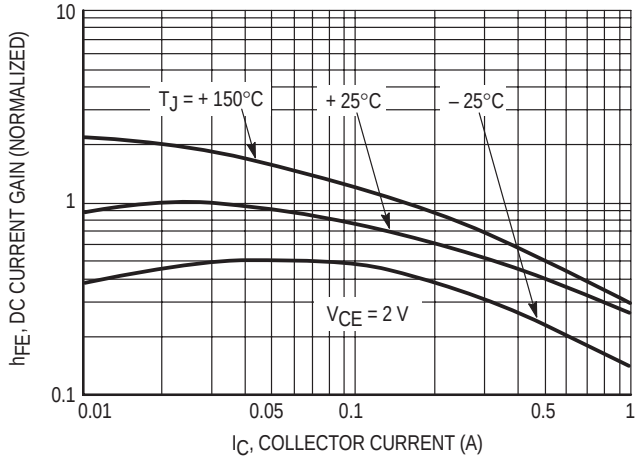


Figure 4. Current Gain

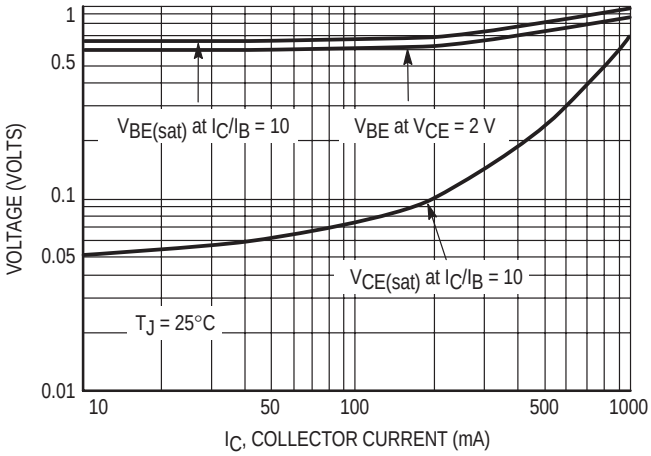


Figure 5. "On" Voltage

Note 1:

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

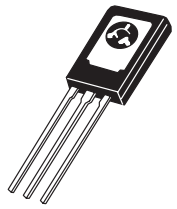
BD179
BD179-10

Plastic Medium Power Silicon NPN Transistor

. . . designed for use in 5.0 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD179 is complementary with BD180

3.0 AMPERES
POWER TRANSISTORS
NPN SILICON
80 VOLTS
30 WATTS



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Base Voltage	V_{CBO}	80	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	3.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 240	Watts mw/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	$V_{(BR)CEO}$	80	—	Vdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
DC Current Gain (I_C = 0.15 A, V_{CE} = 2.0 V) BD179–10 (I_C = 1.0 A, V_{CE} = 2.0 V) ALL	h_{FE}	 63 15	 160 —	
Collector–Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	0.8	Vdc
Base–Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.3	Vdc
Current–Gain – Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	3.0	—	MHz

* Pulse Test: Pulse Width ≦ 300 As, Duty Cycle ≦ 2.0%.

REV 7

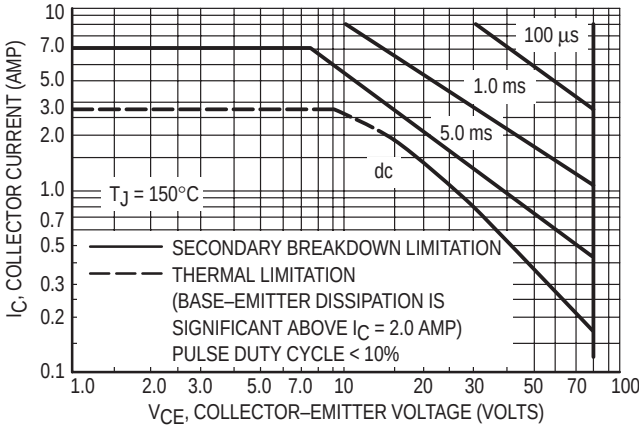


Figure 1. Active Region Safe Operating Area

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power–temperature derating must be observed for both steady state and pulse power conditions.

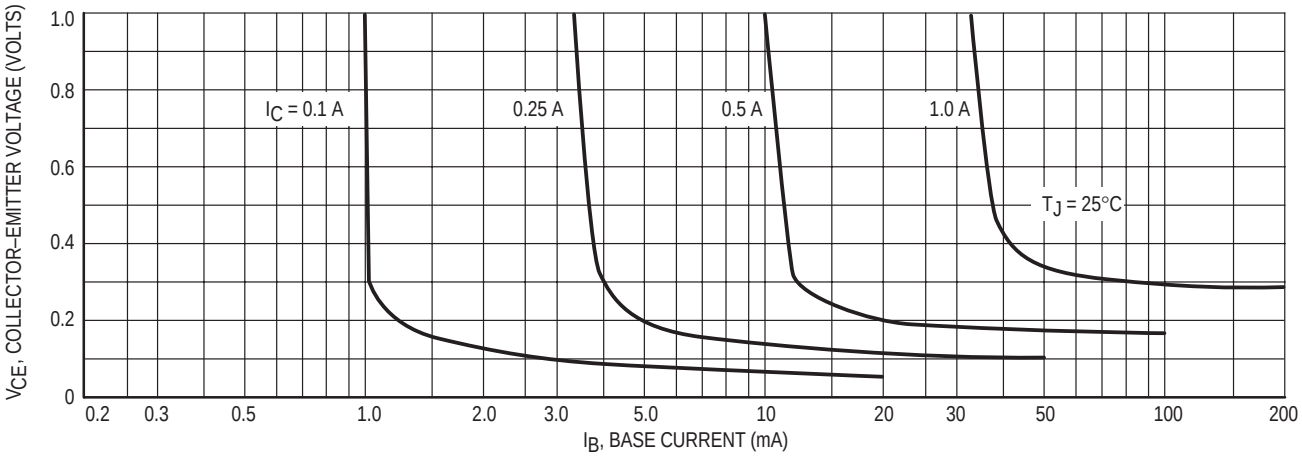


Figure 2. Collector Saturation Region

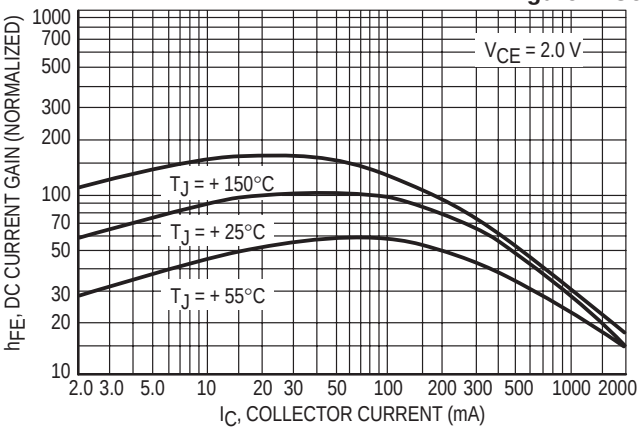


Figure 3. Current Gain

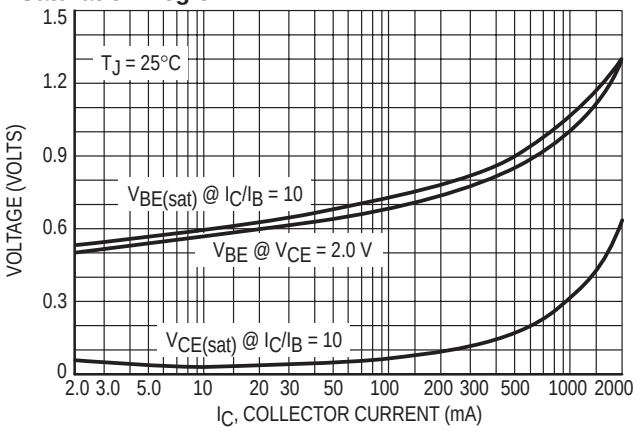


Figure 4. "On" Voltages

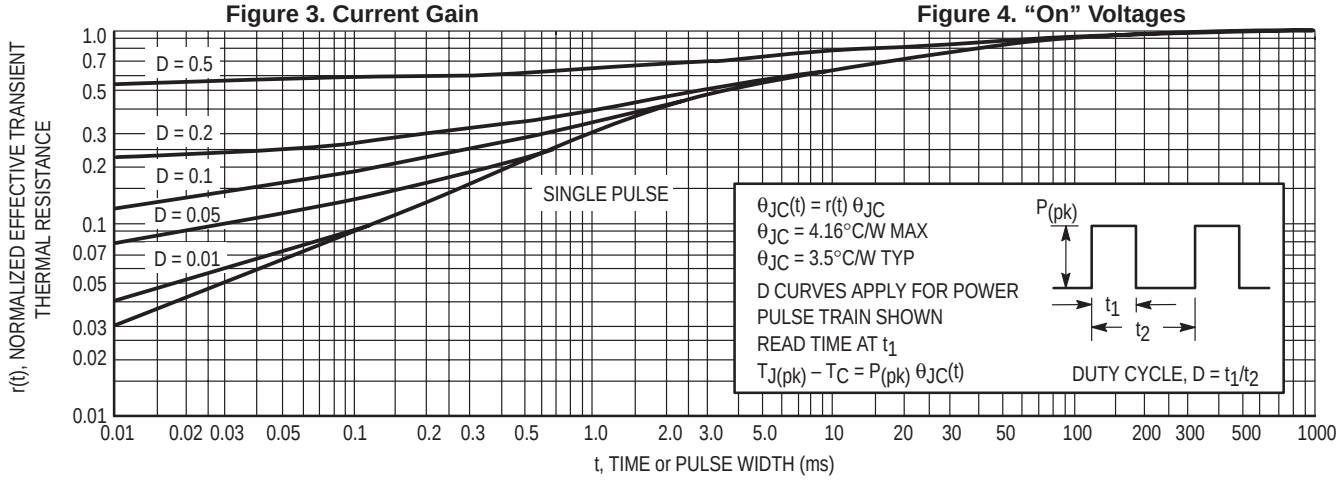


Figure 5. Thermal Response

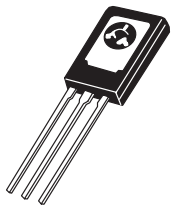
BD180

Plastic Medium Power Silicon PNP Transistor

3.0 AMPERES
POWER TRANSISTOR
PNP SILICON
80 VOLTS
30 WATTS

. . . designed for use in 5.0 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD180 is complementary with BD179



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Base Voltage	V_{CBO}	80	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	3.0	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 240	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)		$V_{(BR)CEO}$	80	—	Vdc
Collector Cutoff Current (V_{CB} = 45 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	 BD180	I_{CBO}	 — —	 — 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
DC Current Gain (I_C = 0.15 A, V_{CE} = 2.0 V) (I_C = 1.0 A, V_{CE} = 2.0 V)		h_{FE}	 40 15	 250 —	—
Collector–Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	—	0.8	Vdc
Base–Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	1.3	Vdc
Current–Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	3.0	—	MHz

* Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

REV 7

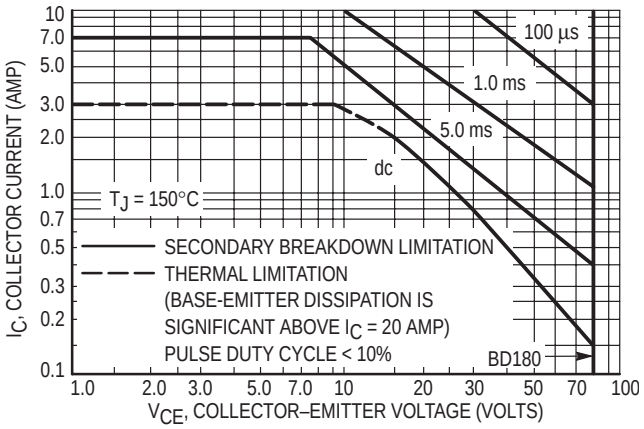


Figure 1. Active Region Safe Operating Area

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power–temperature derating must be observed for both steady state and pulse power conditions.

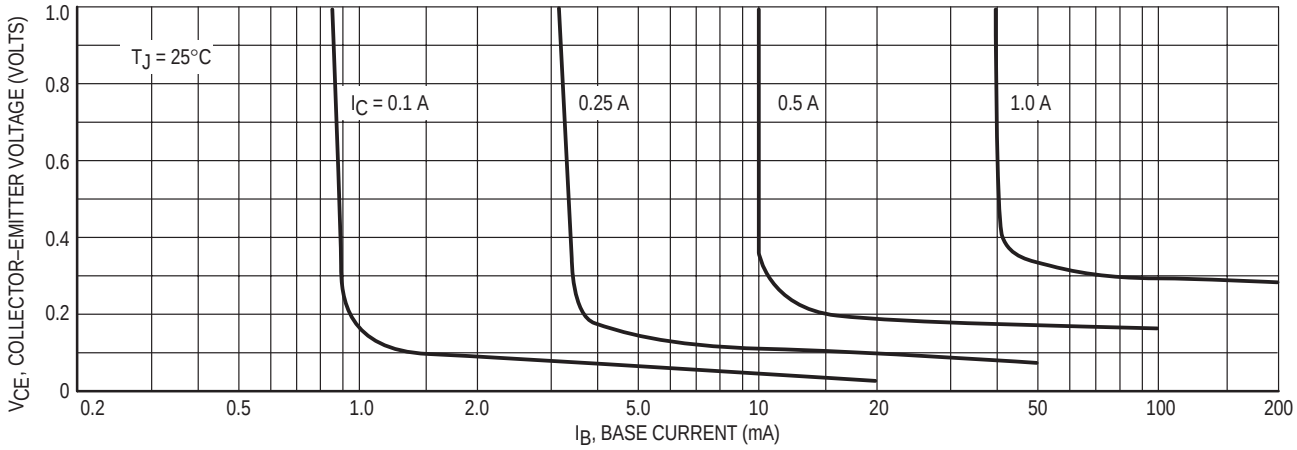


Figure 2. Collector Saturation Region

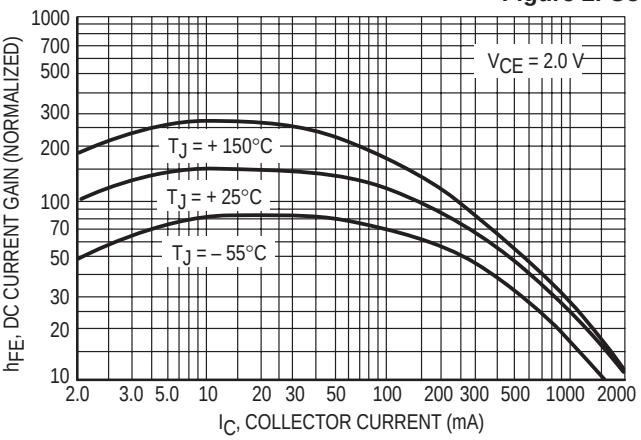


Figure 3. Current Gain

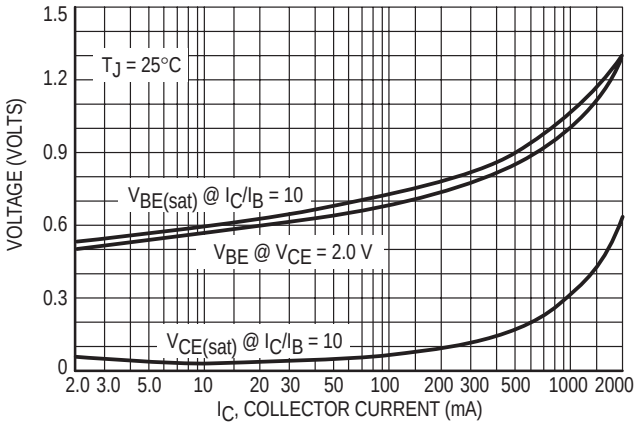


Figure 4. "On" Voltages

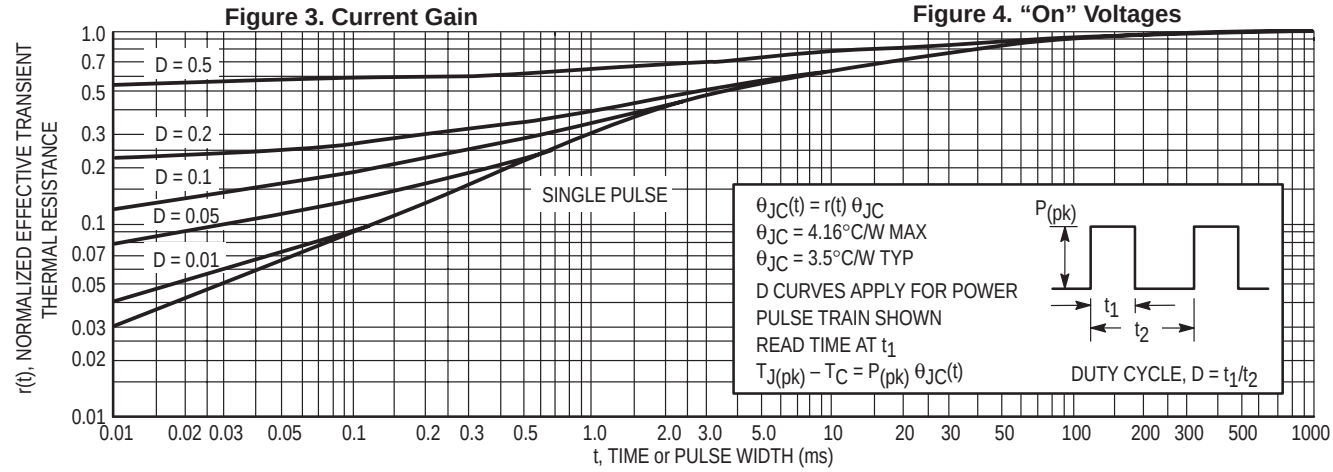


Figure 5. Thermal Response

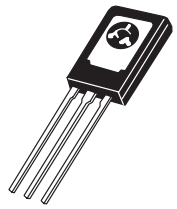
BD237

Plastic Medium Power Silicon NPN Transistor

. . . designed for use in 5.0 to 10 Watt audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 0.15 Adc

2.0 AMPERES
POWER TRANSISTORS
NPN SILICON
80 VOLTS
25 WATTS



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Base Voltage	V_{CBO}	100	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	2.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C	P_D	25	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	$V_{(BR)CEO}$	80	—	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
DC Current Gain (I_C = 0.15 A, V_{CE} = 2.0 V) (I_C = 1.0 A, V_{CE} = 2.0 V)	h_{FE1} h_{FE2}	40 25	— —	
Collector–Emitter Saturation Voltage* (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	0.6	Vdc
Base–Emitter On Voltage* (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.3	Vdc
Current–Gain — Bandwidth Product (I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	3.0	—	MHz

* Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

REV 7

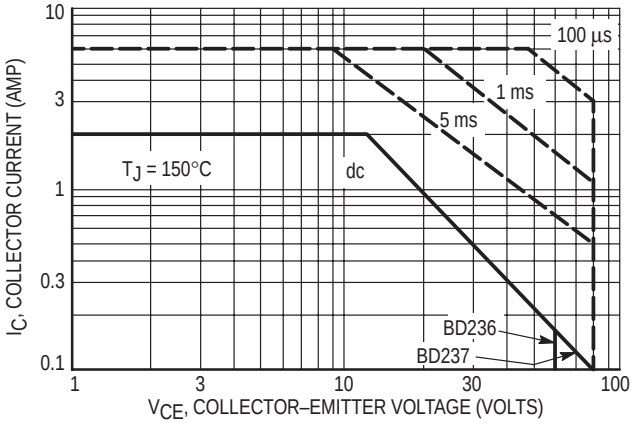


Figure 1. Active Region Safe Operating Area

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power–temperature derating must be observed for both steady state and pulse power conditions.

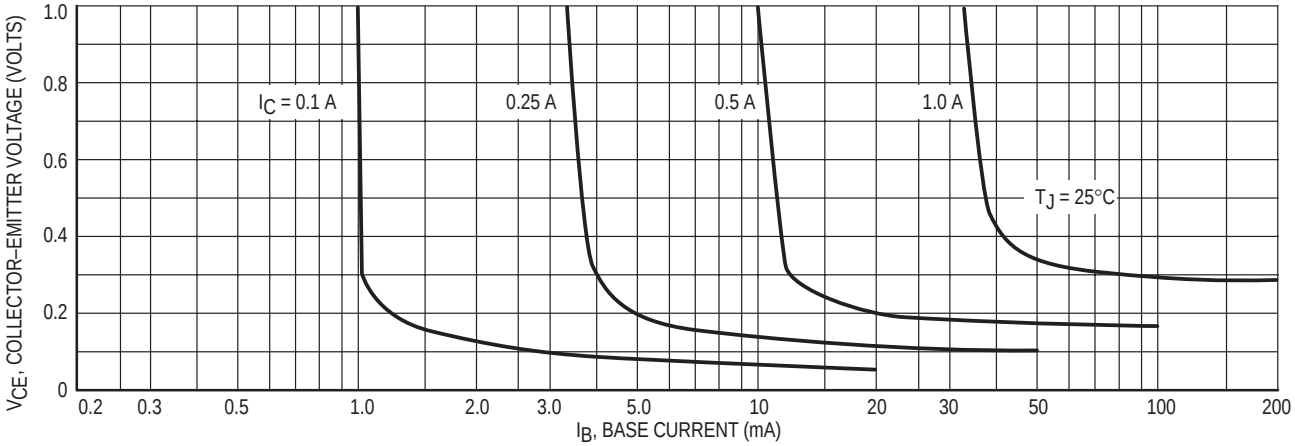


Figure 2. Collector Saturation Region

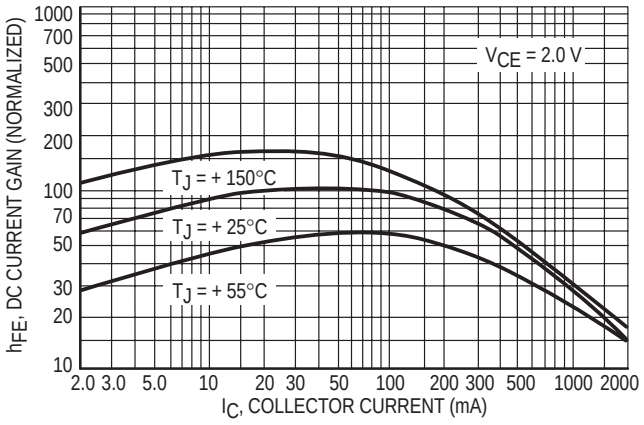


Figure 3. Current Gain

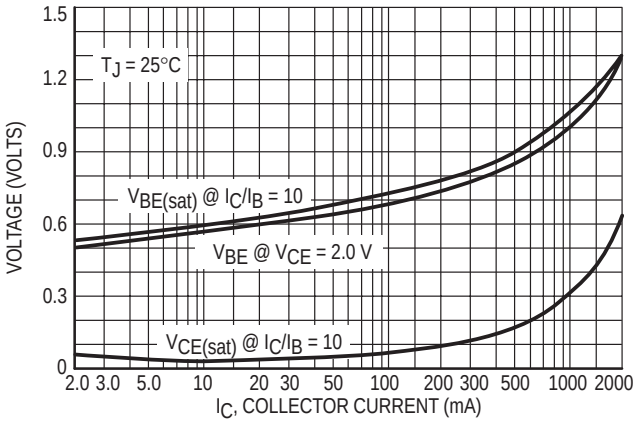


Figure 4. "On" Voltages

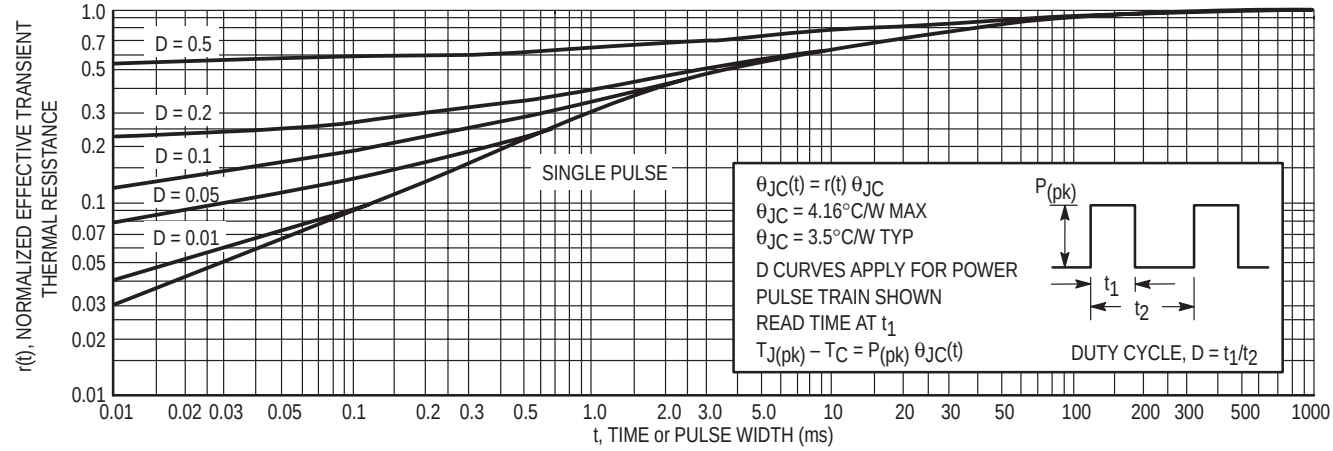


Figure 5. Thermal Response

Complementary Silicon Plastic Power Transistors

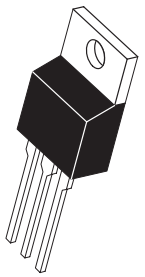
. . . designed for use in general purpose amplifier and switching applications.

- Collector–Emitter Saturation Voltage —
  V_{CE} = 1.2 Vdc (Max) @ I_C = 3.0 Adc
- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 80 Vdc (Min.) BD241B, BD242B
  = 100 Vdc (Min.) BD241C, BD242C
- High Current Gain — Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO–220 AB Package

NPN
BD241B
BD241C*
PNP
BD242B
BD242C*

***Motorola Preferred Device**

3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
80, 100 VOLTS
40 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BD241B BD242B	BD241C BD242C	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Emitter Voltage	V_{CES}	90	115	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	3.0 5.0		Adc Adc
Base Current	I_B	1.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W

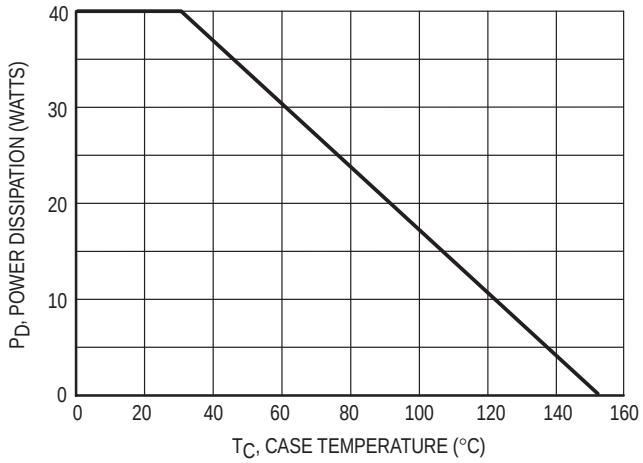


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage[1] (I_C = 30 mAdc, I_B = 0)	BD241B, BD242B BD241C, BD242C	V_{CEO}	80 100		Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)	BD241B, BD241C, BD242B, BD242C	I_{CEO}		0.3	mAdc
Collector Cutoff Current (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	BD241B, BD242B BD241C, BD242C	I_{CES}		200 200	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}		1.0	mAdc
ON CHARACTERISTICS[1]					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	25 10		
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 600 Adc)		$V_{CE(sat)}$		1.2	Vdc
Base–Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$		1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain – Bandwidth Product[2] (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	3.0		MHz
Small–Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	20		

1 Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
2 $f_T = |h_{fe}| \bullet f_{test}$.

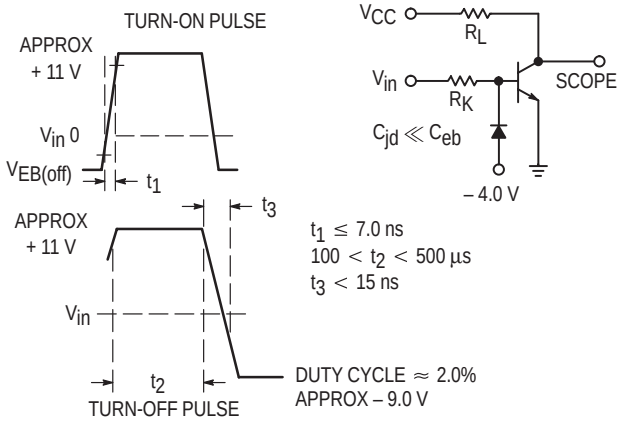


Figure 2. Switching Time Equivalent Circuit

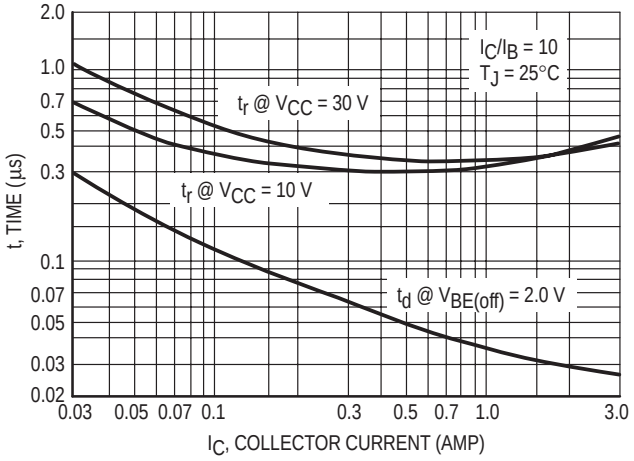


Figure 3. Turn–On Time

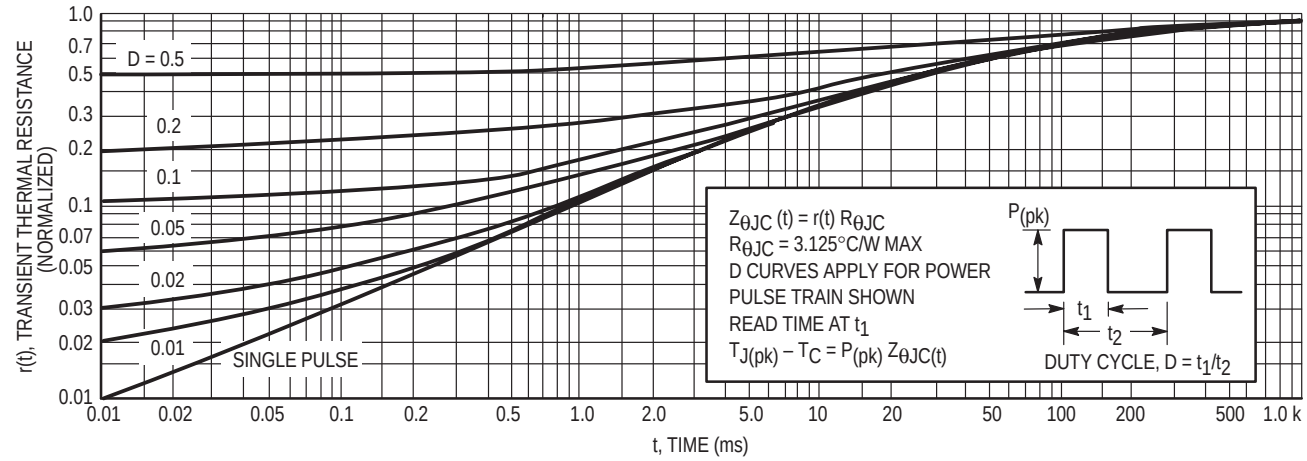


Figure 4. Thermal Response

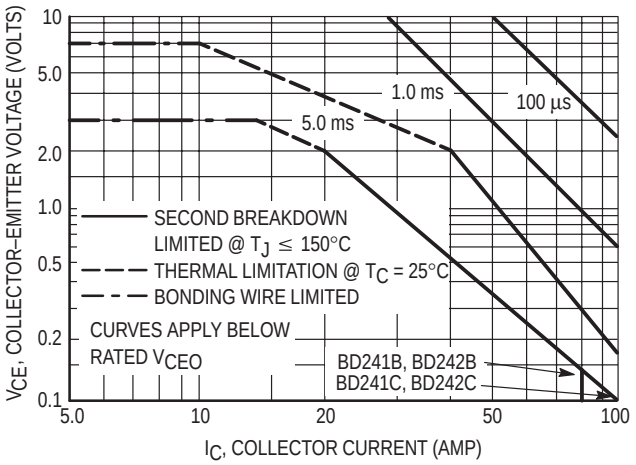


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C, $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

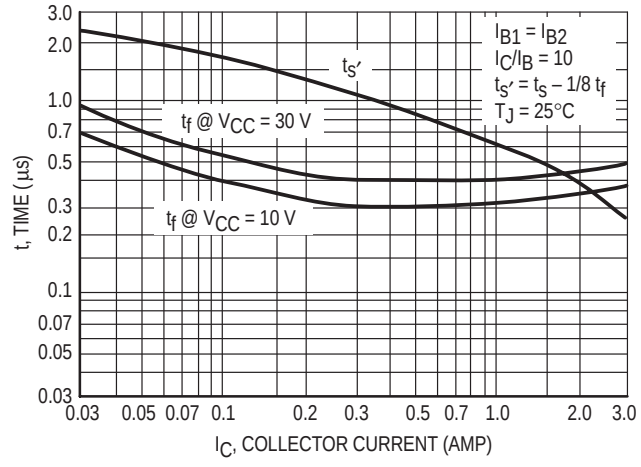


Figure 6. Turn–Off Time

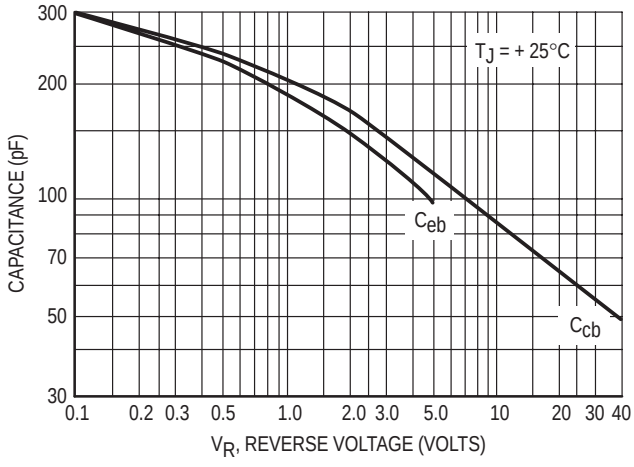


Figure 7. Capacitance

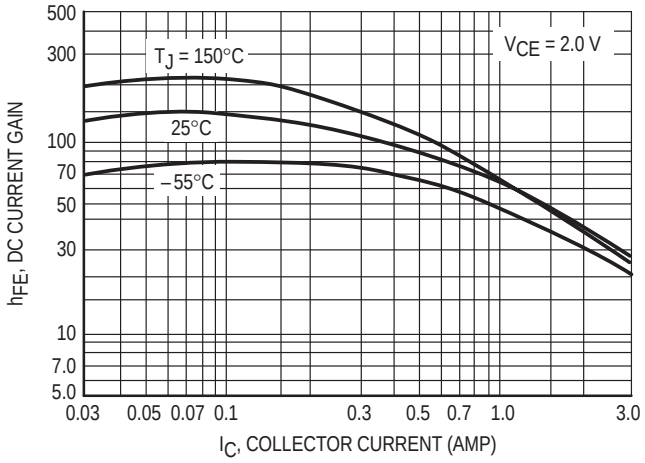


Figure 8. DC Current Gain

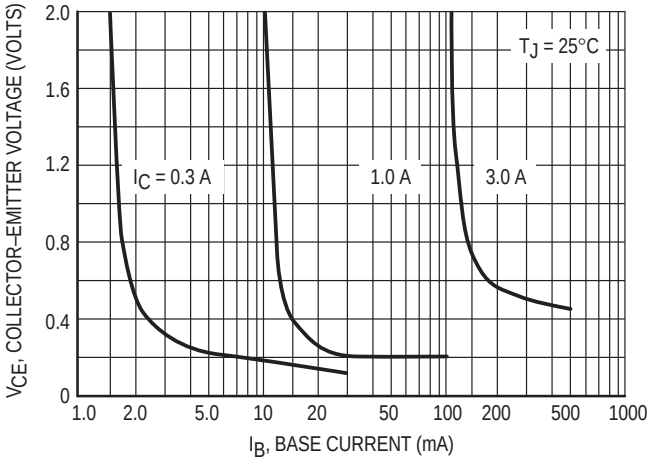


Figure 9. Collector Saturation Region

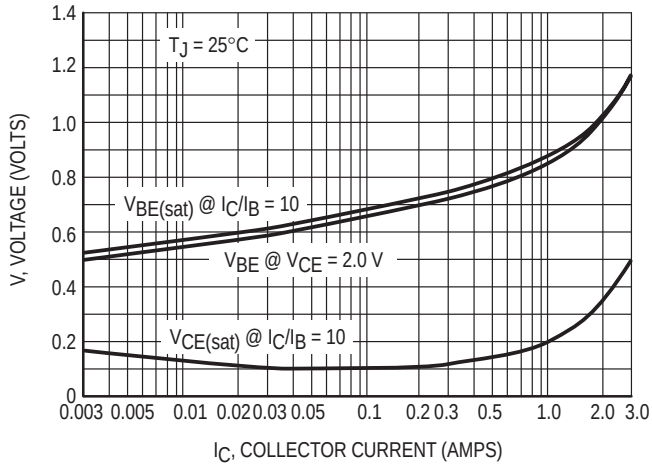


Figure 10. “On” Voltages

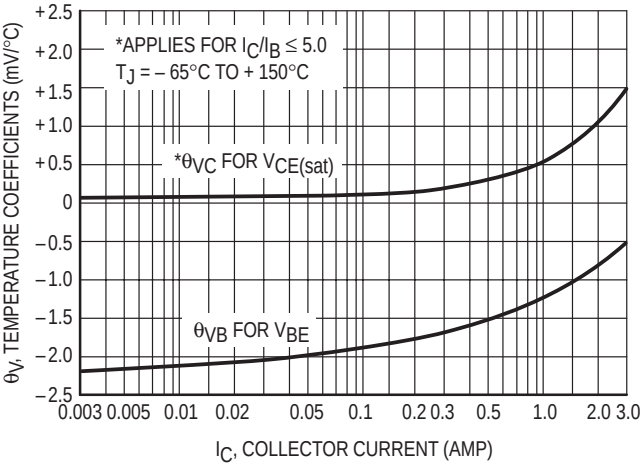


Figure 11. Temperature Coefficients

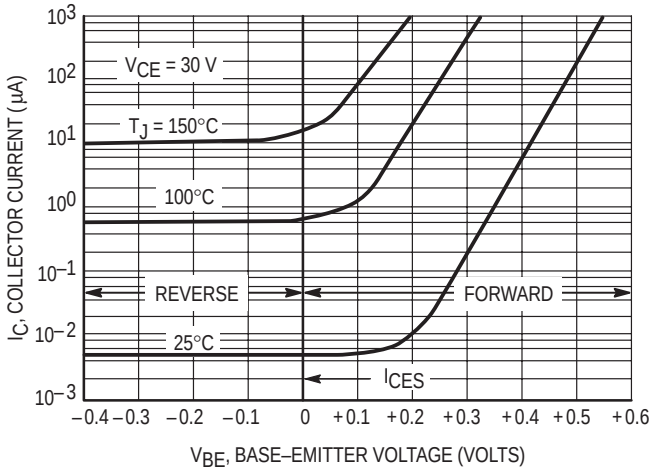


Figure 12. Collector Cut–Off Region

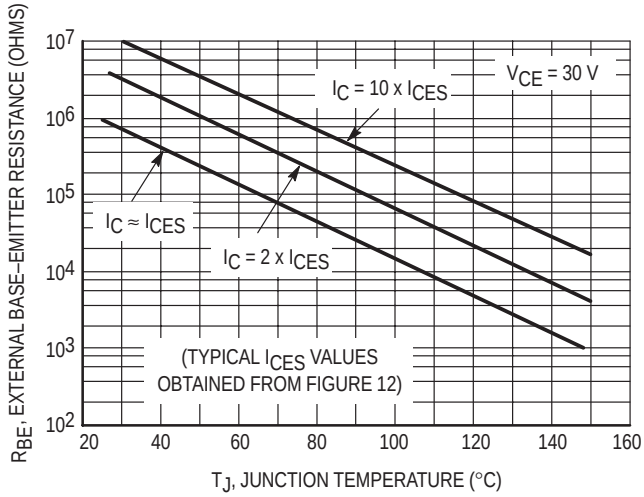


Figure 13. Effects of Base–Emitter Resistance

Complementary Silicon Plastic Power Transistors

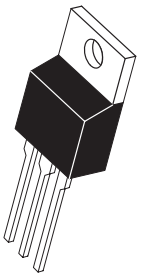
. . . designed for use in general purpose amplifier and switching applications.

- Collector – Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 6.0 Adc
- Collector Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 80 Vdc (Min) — BD243B, BD244B
  = 100 Vdc (Min) — BD243C, BD244C
- High Current Gain Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO–220 AB Package

NPN
BD243B
BD243C*
PNP
BD244B
BD244C*

***Motorola Preferred Device**

6 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
80 – 100 VOLTS
65 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BD243B BD244B	BD243C BD244C	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	6 10		Adc
Base Current	I_B	2.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 65 0.52		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W

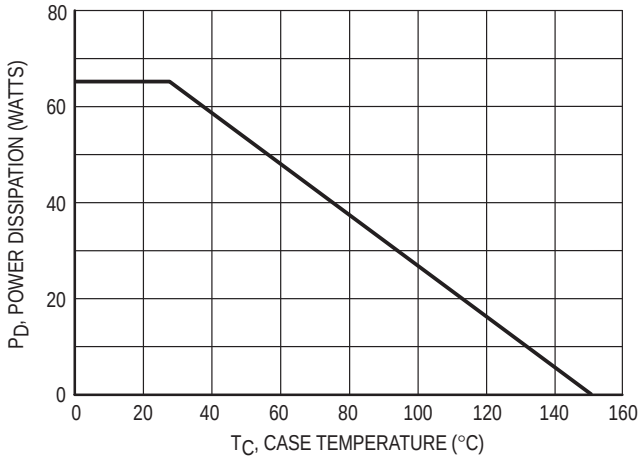


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	BD243B, BD244B BD243C, BD244C	$V_{CEO(sus)}$	 80 100	 — —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)	BD243B, BD243C, BD244B, BD244C	I_{CEO}	—	0.7	mAdc
Collector Cutoff Current (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	BD243B, BD244B BD243C, BD244C	I_{CES}	 — —	 400 400	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	 30 15	 — —	—
Collector–Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$	—	1.5	Vdc
Base–Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	3.0	—	MHz
Small–Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	—	—

(1) Pulse Test: Pulsewidth ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = h_{fe} \bullet f_{test}$

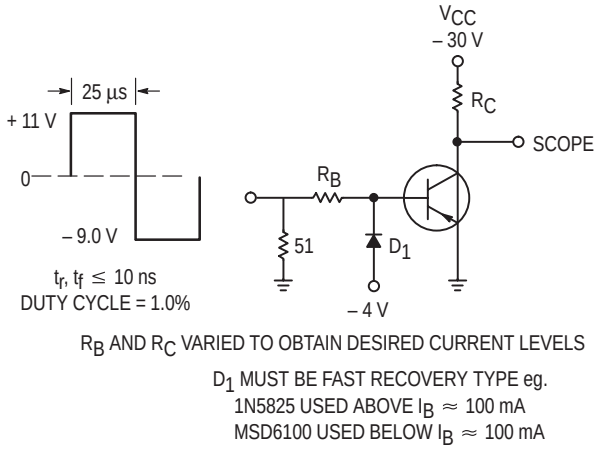


Figure 2. Switching Time Test Circuit

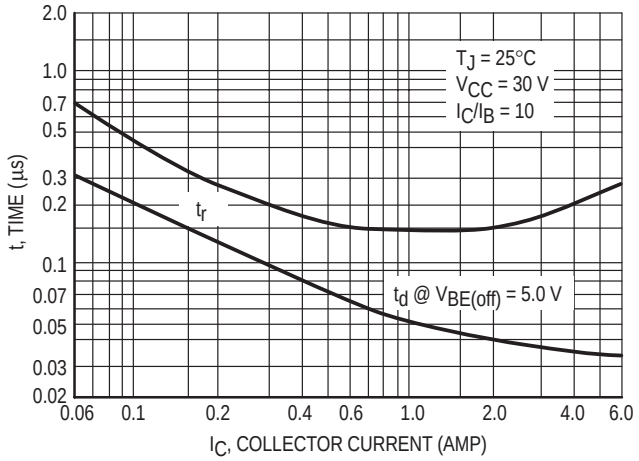


Figure 3. Turn–On Time

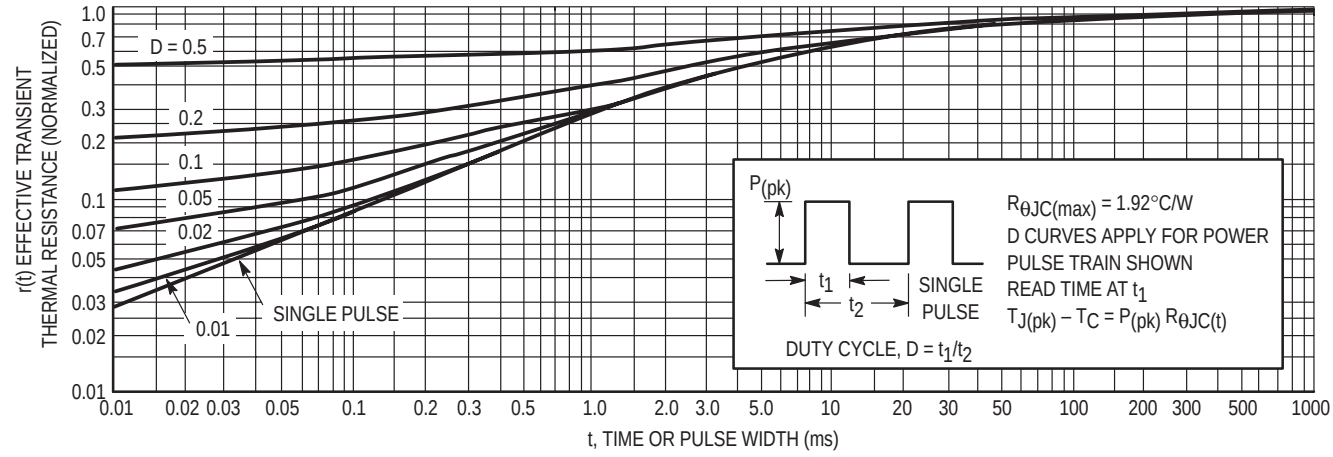


Figure 4. Thermal Response

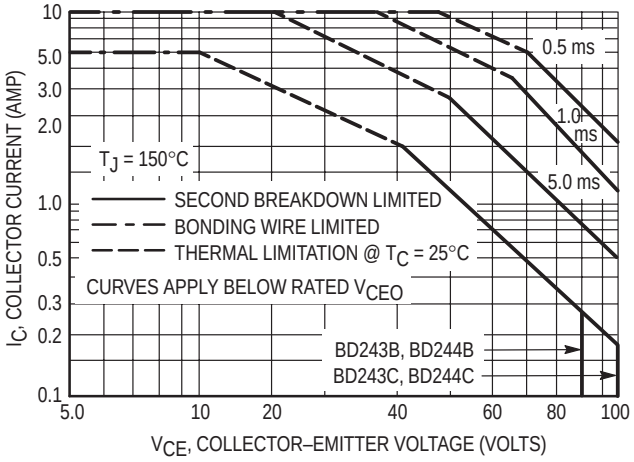


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C: T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$, $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

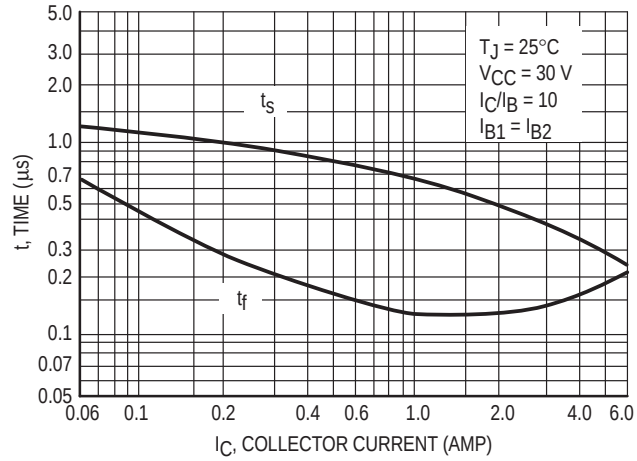


Figure 6. Turn-Off Time

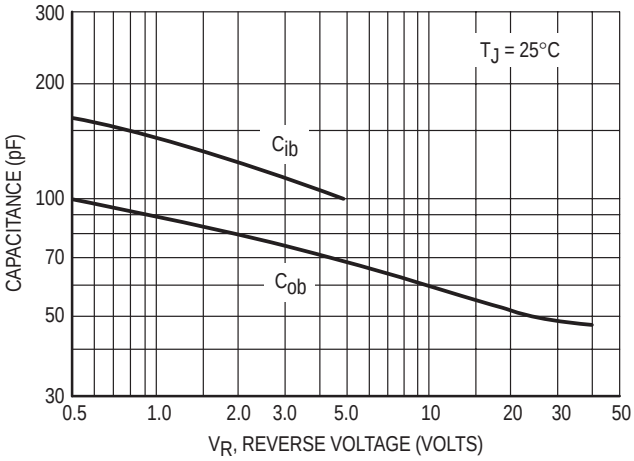


Figure 7. Capacitance

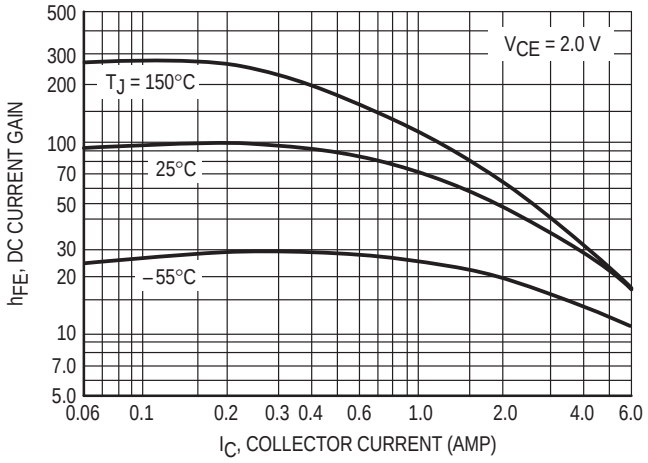


Figure 8. DC Current Gain

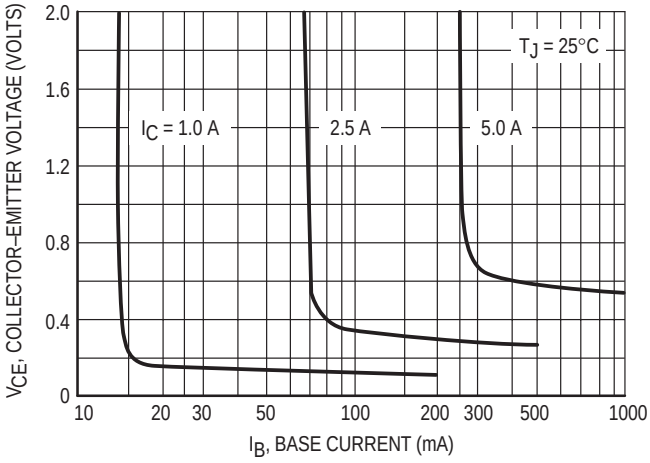


Figure 9. Collector Saturation Region

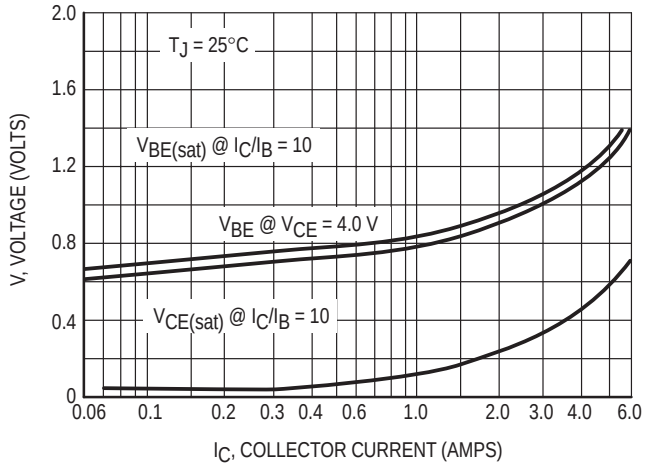


Figure 10. “On” Voltages

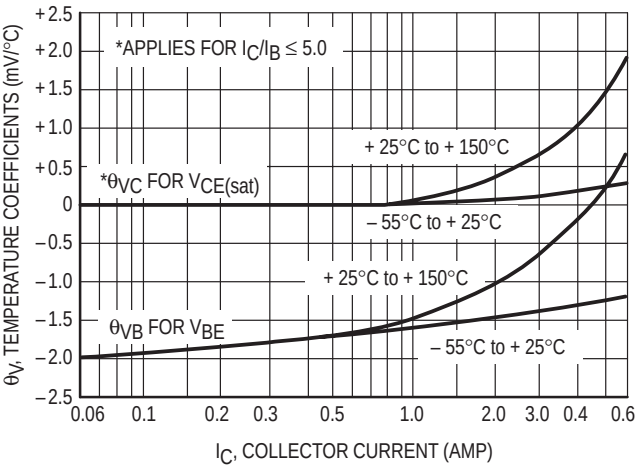


Figure 11. Temperature Coefficients

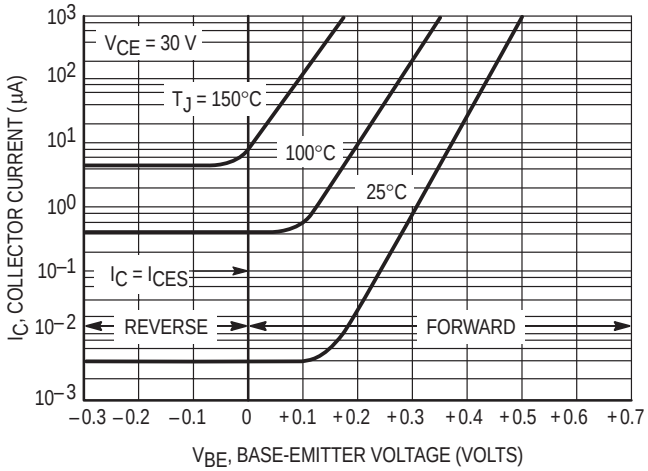


Figure 12. Collector Cut-Off Region

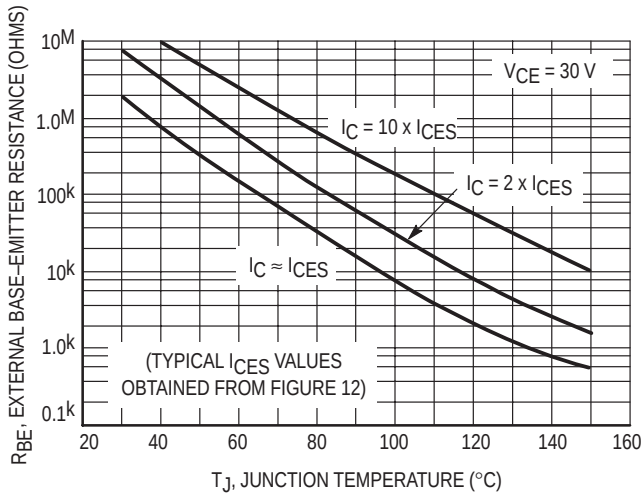


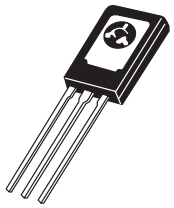
Figure 13. Effects of Base–Emitter Resistance

BD437
BD441

Plastic Medium Power Silicon NPN Transistor

. . . for amplifier and switching applications. Complementary types are BD438 and BD442.

4.0 AMPERES
POWER TRANSISTORS
NPN SILICON



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector–Emitter Voltage	BD437 BD441	V_{CEO}	45 80	Vdc
Collector–Base Voltage	BD437 BD441	V_{CBO}	45 80	Vdc
Emitter–Base Voltage		V_{EBO}	5.0	Vdc
Collector Current		I_C	4.0	Adc
Base Current		I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	36 288	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.5	°C/W

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Collector–Emitter Breakdown Voltage (I_C = 100 mA, I_B = 0)	BD437 BD441	$V_{(BR)CEO}$	 45 80	 — —	 — —	Vdc
Collector–Base Breakdown Voltage (I_C = 100 μA, I_B = 0)	BD437 BD441	$V_{(BR)CBO}$	 45 80	 — —	 — —	Vdc
Emitter–Base Breakdown Voltage (I_E = 100 μA, I_C = 0)		$V_{(BR)EBO}$	5.0	—	—	Vdc
Collector Cutoff Current (V_{CB} = 45 V, I_E = 0) (V_{CB} = 80 V, I_E = 0)	 BD437 BD441	I_{CBO}	 — —	 — —	 0.1 0.1	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 V)		I_{EBO}	—	—	1.0	mAdc
DC Current Gain (I_C = 10 mA, V_{CE} = 5.0 V)	BD437 BD441	h_{FE}	 30 15	 — —	 — —	
DC Current Gain (I_C = 500 mA, V_{CE} = 1.0 V)	BD437 BD441	h_{FE}	 85 40	 — —	 375 475	
DC Current Gain (I_C = 2.0 A, V_{CE} = 1.0 V)	BD437 BD441	h_{FE}	 40 15	 — —	 — —	
Collector Saturation Voltage (I_C = 2.0 A, I_B = 0.2 A) (I_C = 3.0 A, I_B = 0.3 A)	 BD437 BD441	$V_{CE(sat)}$	 — —	 — —	 0.7 0.8	Vdc
Base–Emitter On Voltage (I_C = 2.0 A, V_{CE} = 1.0 V)		$V_{BE(on)}$	—	—	1.1	Vdc
Current–Gain — Bandwidth Product (V_{CE} = 1.0 V, I_C = 250 mA, f = 1.0 MHz)		f_T	3.0	—	—	MHz

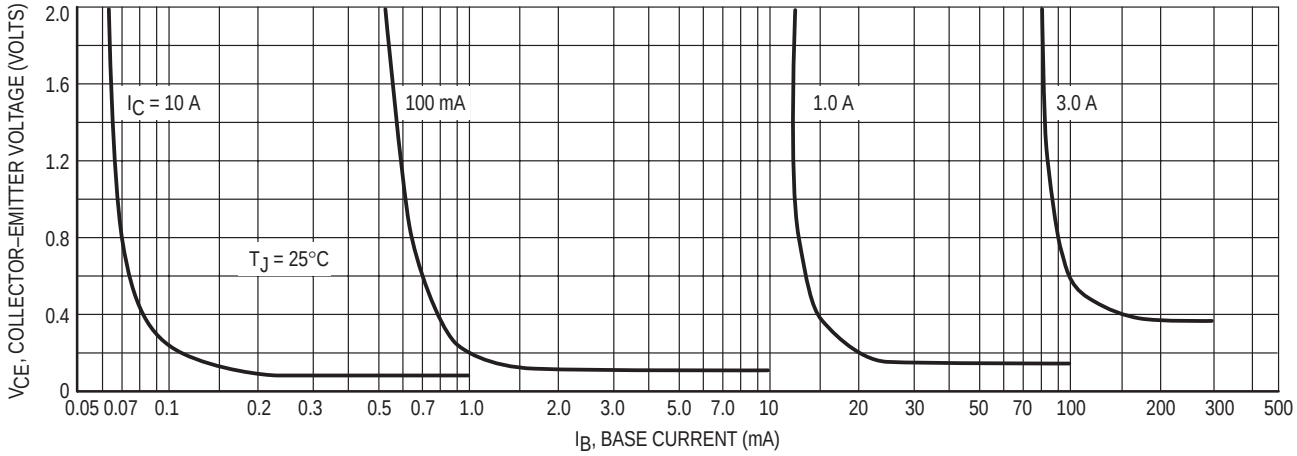


Figure 1. Collector Saturation Region

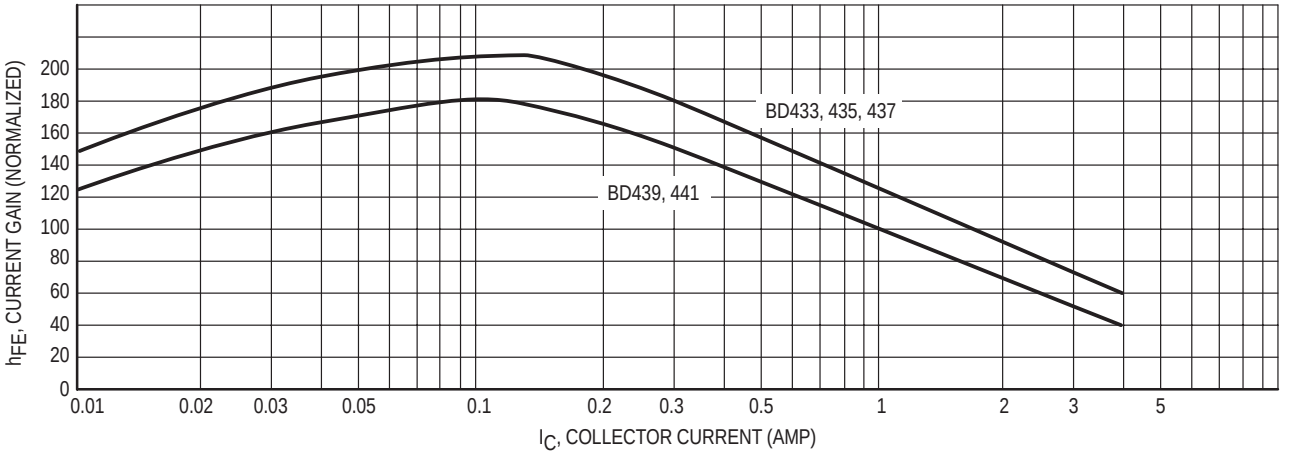


Figure 2. Current Gain

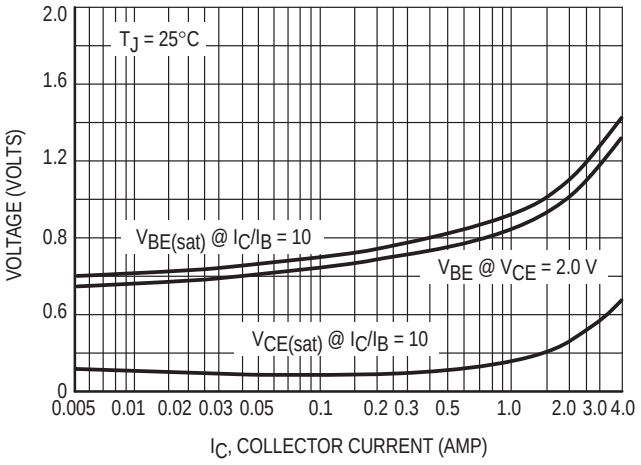


Figure 3. “On” Voltage

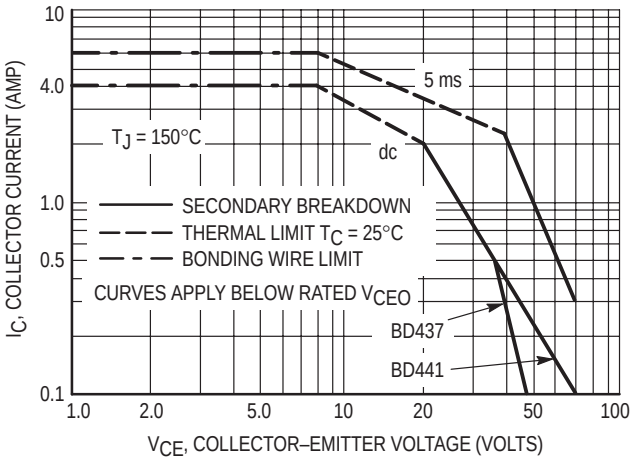


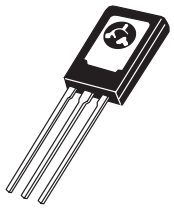
Figure 4. Active Region Safe Operating Area

BD438
BD440
BD442

Plastic Medium Power Silicon PNP Transistor

. . . for amplifier and switching applications. Complementary types are BD437 and BD441.

4.0 AMPERES
POWER TRANSISTORS
PNP SILICON



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector–Emitter Voltage	BD438 BD440 BD442	V_{CEO}	45 60 80	Vdc
Collector–Base Voltage	BD438 BD440 BD442	V_{CBO}	45 60 80	Vdc
Emitter–Base Voltage		V_{EBO}	5.0	Vdc
Collector Current		I_C	4.0	Adc
Base Current		I_B	1.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	36 288	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.5	°C/W

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Collector–Emitter Breakdown Voltage		$V_{(BR)CEO}$				Vdc
(I_C = 100 mA, I_B = 0)	BD438		45	—	—	
	BD440		60	—	—	
	BD442		80	—	—	
Collector–Base Breakdown Voltage		$V_{(BR)CBO}$				Vdc
(I_C = 100 μA, I_B = 0)	BD438		45	—	—	
	BD440		60	—	—	
	BD442		80	—	—	
Emitter–Base Breakdown Voltage		$V_{(BR)EBO}$	5.0	—	—	Vdc
(I_E = 100 μA, I_C = 0)						
Collector Cutoff Current		I_{CBO}				mAdc
(V_{CB} = 45 V, I_E = 0)	BD438		—	—	0.1	
(V_{CB} = 60 V, I_E = 0)	BD440		—	—	0.1	
(V_{CB} = 80 V, I_E = 0)	BD442		—	—	0.1	
Emitter Cutoff Current		I_{EBO}	—	—	1.0	mAdc
(V_{EB} = 5.0 V)						
DC Current Gain		h_{FE}				
(I_C = 10 mA, V_{CE} = 5.0 V)	BD438		30	—	—	
	BD440		20	—	—	
	BD442		15	—	—	
DC Current Gain		h_{FE}				
(I_C = 500 mA, V_{CE} = 1.0 V)	BD438		85	—	375	
	BD440		40	—	475	
	BD442		40	—	475	
DC Current Gain		h_{FE}				
(I_C = 2.0 A, V_{CE} = 1.0 V)	BD438		40	—	—	
	BD440		25	—	—	
	BD442		15	—	—	
Collector Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 3.0 A, I_B = 0.3 A)	BD438		—	—	0.7	
	BD440		—	—	0.8	
	BD442		—	—	0.8	
Base–Emitter On Voltage	BD438	$V_{BE(ON)}$	—	—	1.1	Vdc
(I_C = 2.0 A, V_{CE} = 1.0 V)	BD440/442		—	—	1.5	
Current–Gain — Bandwidth Product		f_T	3.0	—	—	MHz
(V_{CE} = 1.0 V, I_C = 250 mA, f = 1.0 MHz)						

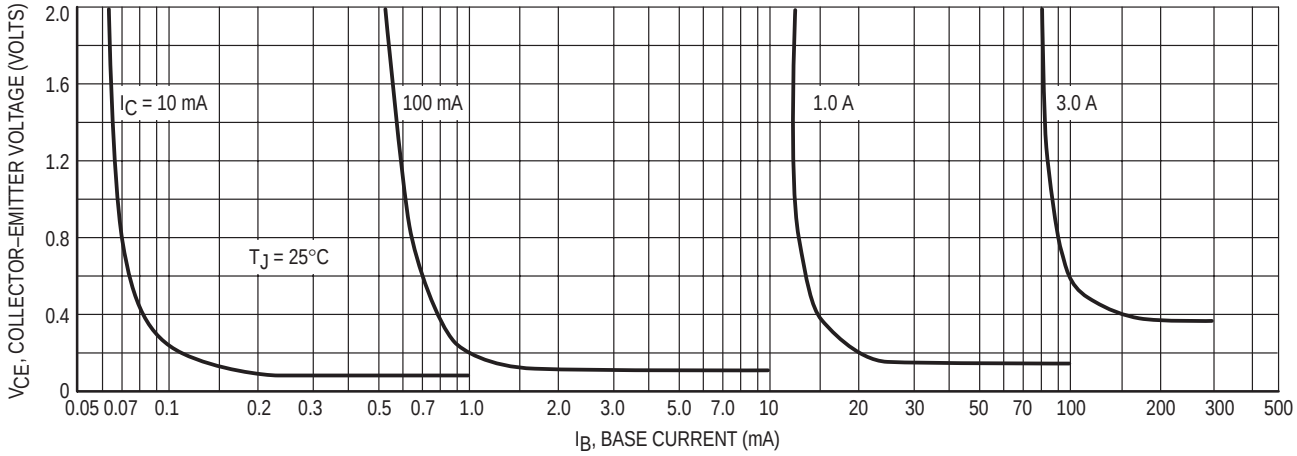


Figure 1. Collector Saturation Region

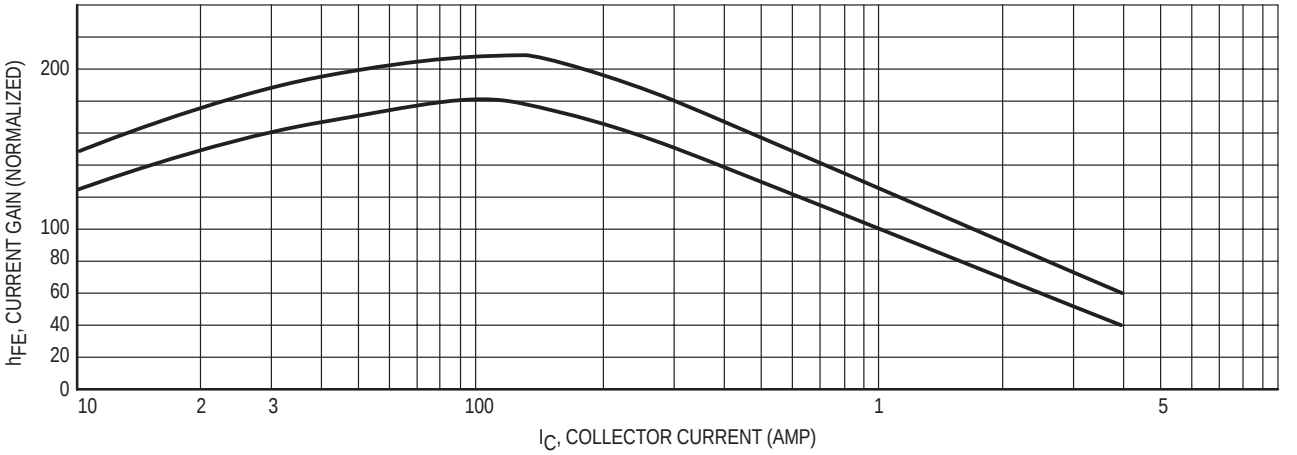


Figure 2. Current Gain

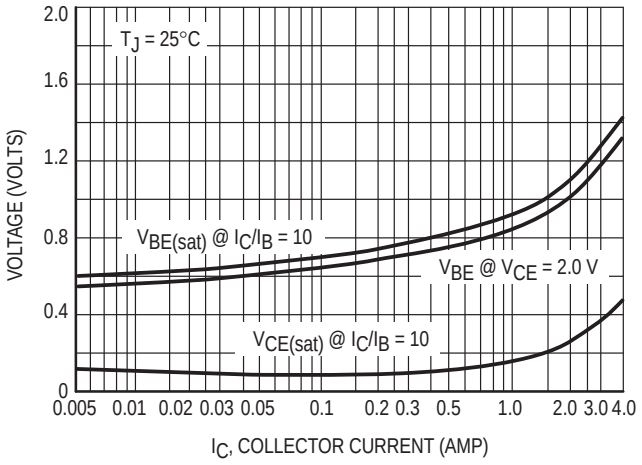


Figure 3. “On” Voltage

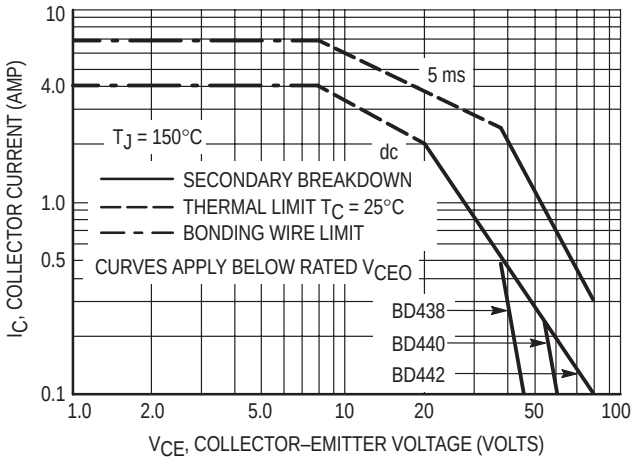


Figure 4. Active Region Safe Operating Area

Plastic Medium-Power Silicon NPN Darlingtons

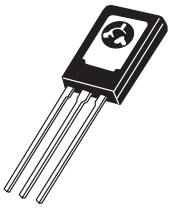
. . . for use as output devices in complementary general–purpose amplifier applications.

- High DC Current Gain —
  h_{FE} = 750 (Min) @ I_C = 1.5 and 2.0 Adc
- Monolithic Construction
- BD675, 675A, 677, 677A, 679, 679A, 681 are complementary with BD676, 676A, 678, 678A, 680, 680A, 682
- BD 677, 677A, 679, 679A are equivalent to MJE 800, 801, 802, 803

BD675
BD675A
BD677
BD677A
BD679
BD679A
BD681*

***Motorola Preferred Device**

4.0 AMPERE
DARLINGTON
POWER TRANSISTORS
NPN SILICON
60, 80, 100 VOLTS
40 WATTS



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	BD675 BD675A	BD677 BD677A	BD679 BD679A	BD681	Unit
Collector–Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	4.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @T_C = 25°C Derate above 25°C	P_D	40 0.32				Watts W/°C
Operating and Storage Junction Temperating Range	T_J, T_{stg}	–55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.13	°C/W

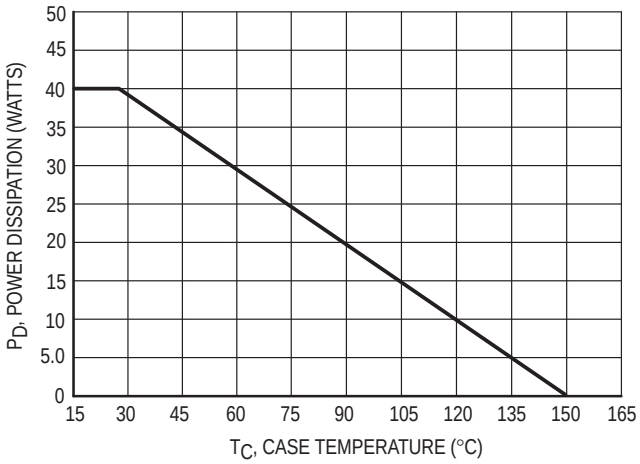


Figure 1. Power Temperature Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage(1) (I_C = 50 mAdc, I_B = 0)	BD675, 675A BD677, 677A BD679, 679A BD681	BV_{CEO}	45 60 80 100	— — — —	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	—	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100'C)		I_{CBO}	 — —	 0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS					
DC Currert Gain(1) (I_C = 1.5 Adc,V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	 BD675, 677, 679, 681 BD675A, 677A, 679A	h_{FE}	 750 750	 — —	—
Collector–Emitter Saturation Voltage(1) (I_C = 1.5 Adc, I_B = 30 mAdc) (I_C = 2.0 Adc, I_B = 40 mAdc)	 BD677, 679, 681 BD675A, 677A, 679A	$V_{CE(sat)}$	 — —	 2.5 2.8	Vdc
Base–Emitter On Voltage(1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3 0 Vdc)	 BD677, 679, 681 BD675A, 677A, 679A	$V_{BE(on)}$	 — —	 2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

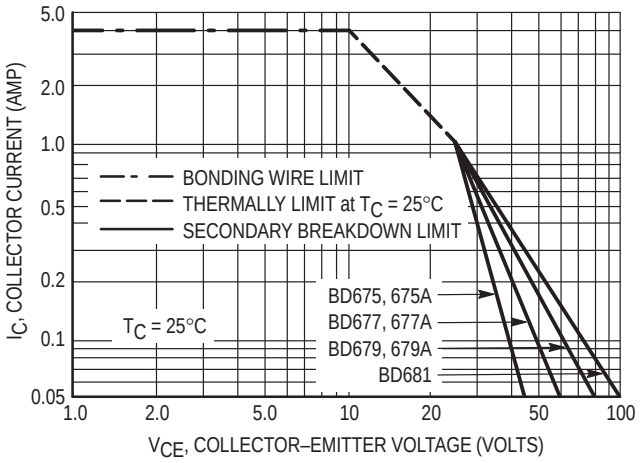


Figure 2. DC Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

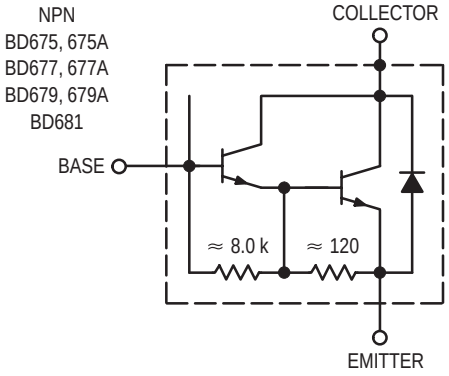


Figure 3. Darlington Circuit Schematic

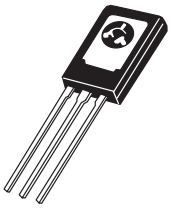
Plastic Medium-Power Silicon PNP Darlingtons

. . . for use as output devices in complementary general–purpose amplifier applications.

- High DC Current Gain —
  h_{FE} = 750 (Min) @ I_C = 1.5 and 2.0 Adc
- Monolithic Construction
- BD676, 676A, 678, 678A, 680, 680A, 682 are complementary with BD675, 675A, 677, 677A, 679, 679A, 681
- BD 678, 678A, 680, 680A are equivalent to MJE 700, 701, 702, 703

BD676
BD676A
BD678
BD678A
BD680
BD680A
BD682

4.0 AMPERE
DARLINGTON
POWER TRANSISTORS
PNP SILICON
45, 60, 80, 100 VOLTS
40 WATTS



CASE 77–08
TO–225AA TYPE

MAXIMUM RATING

Rating	Symbol	BD676 BD676A	BD678 BD678A	BD680 BD680A	BD682	Unit
Collector–Emitter Voltage	V_{CEO}	45	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	45	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0				Vdc
Collector Current	I_C	4.0				Adc
Base Current	I_B	0.1				Adc
Total Device Dissipation @ T_C = 25 °C Derate above 25 °C	P_D	40 0.32				Watts W/°C
Operating and Storage Junction Temperating Range	T_J, T_{stg}	–55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.13	°C/W

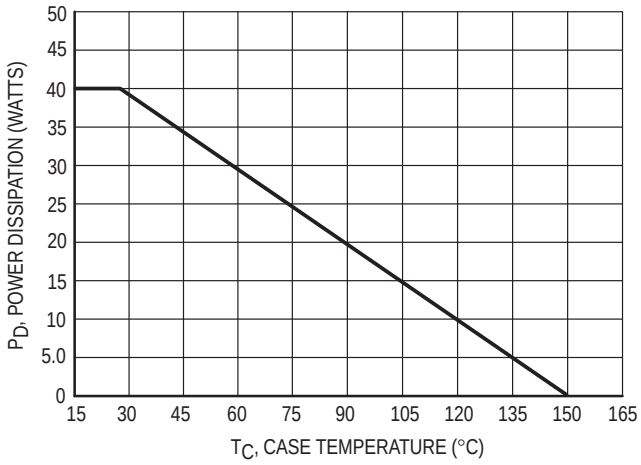


Figure 1. Power Temperature Derating

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage(1) (I_C = 50 mAdc, I_B = 0)	BD676, 676A BD678, 678A BD680, 680A BD682	BV_{CEO}	45 60 80 100	— — — —	Vdc
Collector Cutoff Current (V_{CE} = Half Rated V_{CEO}, I_B = 0)		I_{CEO}	—	500	μAdc
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0) (V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)		I_{CBO}	 — —	 0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	 BD676, 678, 680, 682 BD676A, 678A, 680A	h_{FE}	 750 750	 — —	
Collector–Emitter Saturation Voltage(1) (I_C = 1.5 Adc, I_B = 30 mAdc) (I_C = 2.0 Adc, I_B = 40 mAdc)	 BD678, 680, 682 BD676A, 678A, 680A	$V_{CE(sat)}$	 — —	 2.5 2.8	Vdc
Base–Emitter On Voltage(1) (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	 BD678, 680, 682 BD676A, 678A, 680A	$V_{BE(on)}$	 — —	 2.5 2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

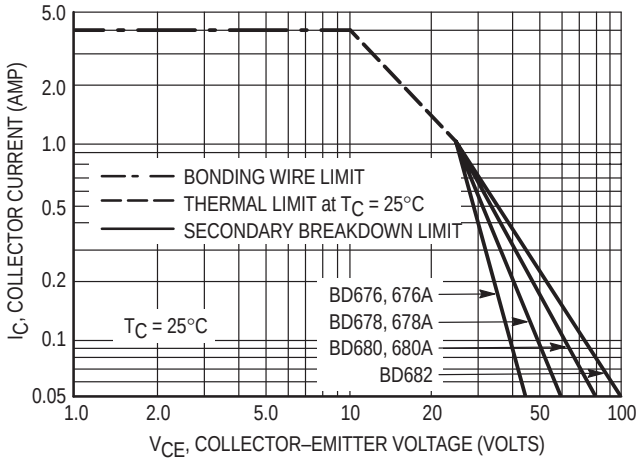


Figure 2. DC Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

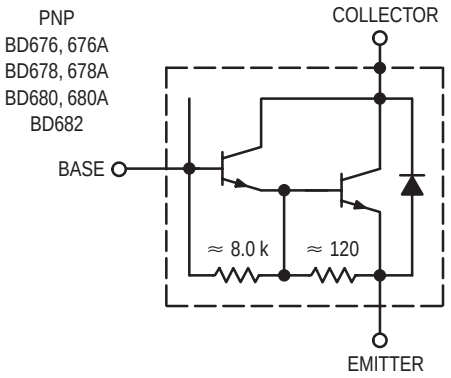


Figure 3. Darlington Circuit Schematic

Plastic Darlington Complementary Silicon Power Transistors

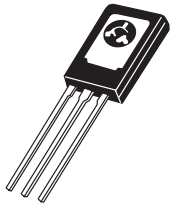
. . . designed for general purpose amplifier and high–speed switching applications.

- High DC Current Gain
  h_{FE} = 1400 (Typ) @ I_C = 2.0 Adc
- Collector–Emitter Sustaining Voltage — @ 10 mAdc
  $V_{CEO(sus)}$ = 45 Vdc (Min) — BD776
  = 60 Vdc (Min) — BD777, 778
  = 80 Vdc (Min) — BD780
- Reverse Voltage Protection Diode
- Monolithic Construction with Built–in Base–Emitter output Resistor

NPN
BD777
PNP
BD776
BD778
BD780*

***Motorola Preferred Device**

DARLINGTON
4–AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
45, 60, 80 VOLTS
15 WATTS



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	BD776	BD777 BD778	BD780	Unit
Collector–Emitter Voltage	V_{CEO}	45	60	80	Vdc
Collector–Base Voltage	V_{CB}	45	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	4.0 6.0			Adc
Base Current	I_B	100			mAdc
Total Device Dissipation T_C = 25°C – Derate above 25°C	P_D	15 0.12			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	83.3	°C/W

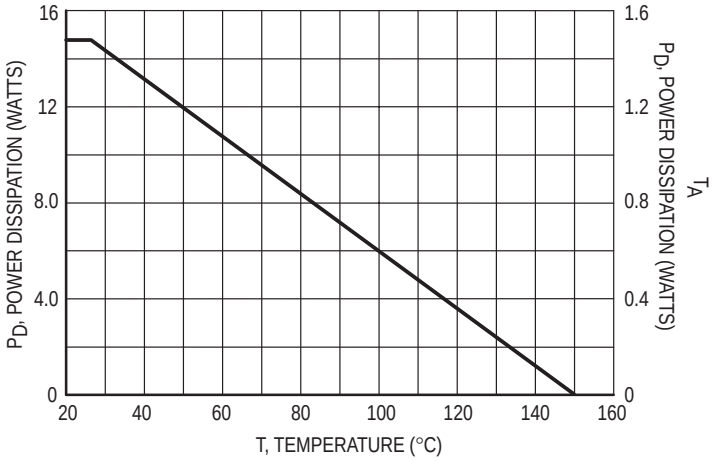


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_O = 10 mAdc, I_B = 0)	BD776 BD777, BD778 BD780	$V_{CEO(sus)}$	45 60 80	— — —	Vdc
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 20 Vdc, I_B = 0)	BD776		—	100	
(V_{CE} = 30 Vdc, I_B = 0)	BD777, BD778		—	100	
(V_{CE} = 40 Vdc, I_B = 0)	BD780		—	100	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = Rated, $V_{CEO(sus)}$, I_E = 0)			—	1.0	
(V_{CB} = Rated, $V_{CEO(sus)}$, I_E = 0, I_C = 100°C)			—	100	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		H_{FE}	750	—	
Collector–Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 6 mAdc)		$V_{CE(Sat)}$	—	1.5	Vdc
Base Emitter Saturation Voltage (I_C = 1.5 Adc, I_B = 6 mAdc)		$V_{BE(Sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (I_C = 1.5 Adc,V_{CE} = 3 Vdc)		$V_{BE(On)}$	—	2.3	Vdc
Output Diode Voltage Drop (I_{EC} = 2.0 Adc)		V_{EC}	—	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)		f_T	20	—	MHz
		Symbol	**Min**	**Typ**	**Unit**
Turn–On Time (I_C = 250 mA/V_{CE} = 2 V)	BD775–777 BD776–778–780	t_{on}	— —	250 150	ns
Turn–Off Time (I_C = 250 mA, V_{CE} = 2 V)	BD775–777 BD776–778–780	t_{off}	— —	600 400	ns

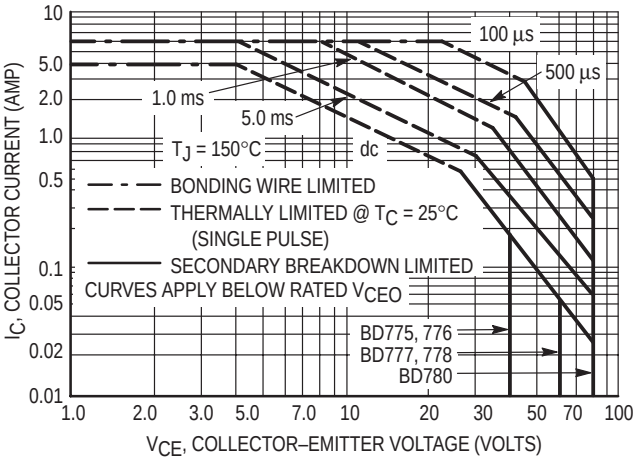


Figure 2. Active Region Safe Operating Area

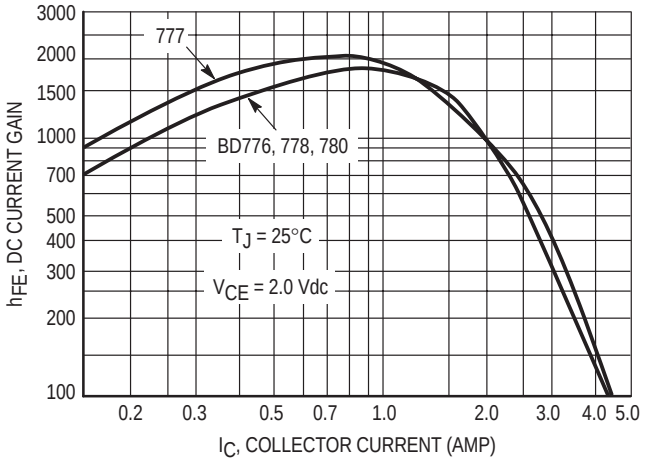


Figure 3. Typical DC Current Gain

Figure 4. Darlington Circuit Schematic

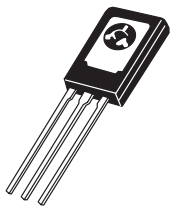
NPN
BD787
PNP
BD788

Complementary Plastic Silicon Power Transistors

. . . designed for lower power audio amplifier and low current, high–speed switching applications.

- Low Collector–Emitter Sustaining Voltage — $V_{CEO(sus)}$ 60 Vdc (Min) — BD787, BD788
- High Current–Gain — Bandwidth Product — f_T = 50 MHz (Min) @ I_C = 100 mAdc
- Collector–Emitter Saturation Voltage Specified at 0.5, 1.0, 2.0 and 4.0 Adc

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60 VOLTS
15 WATTS



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	BD787 BD788	Unit
Collector–Emitter Voltage	V_{CEO}	60	Vdc
Collector–Base Voltage	V_{CBO}	80	Vdc
Emitter–Base Voltage	V_{EBO}	6.0	Vdc
Collector Current — Continous — Peak	I_C	4.0 8.0	Adc Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	15 0.12	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W

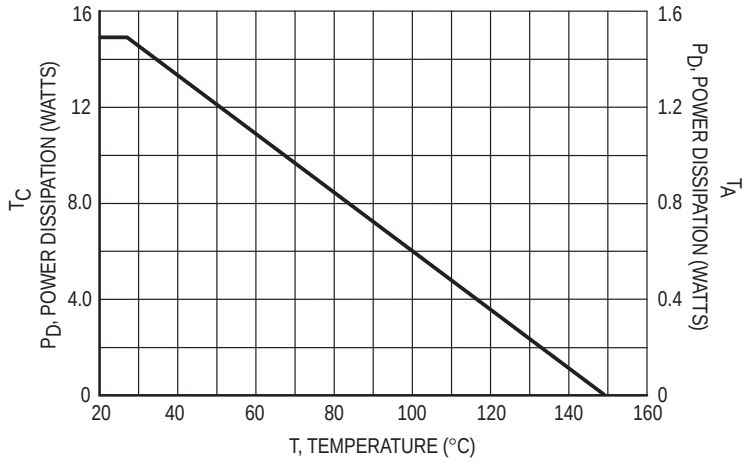


Figure 1. Power Derating

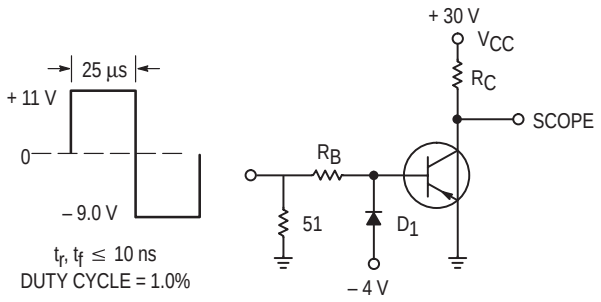
REV 7

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)		$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current (V_{CE} = 20 Vdc, I_B = 0) (V_{CE} = 30 Vdc, I_B = 0)		I_{CEO}	— —	100 —	μAdc —
Collector Cutoff Current (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)		I_{CEX}	— —	1.0 0.1	μAdc mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 200 mAdc, V_{CE} = 3.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	 40 25 20 5.0	 250 — — —	—
Collector–Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 1.0 Adc, I_B = 100 mAdc) (I_C = 2.0 Adc, I_B = 200 mAdc) (I_C = 4.0 Adc, I_B = 800 mAdc)		$V_{CE(sat)}$	 — — — —	 0.4 0.6 0.8 2.5	Vdc
Base–Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	—	2.0	Vdc
Base–Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		f_T	50	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_C = 0) (f = 0.1 MHz)	 BD787 BD788	C_{ob}	 — —	 50 70	pF
Small–Signal Current Gain (I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	10	—	—

* Indicates JEDEC Registered Data

(1) Pulse Test; Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



R_B AND R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, e.g.:

1N5825 USED ABOVE $I_B \approx$ 100 mA

MSD6100 USED BELOW $I_B \approx$ 100 mA

FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES.

Figure 2. Switching Time Test Circuit

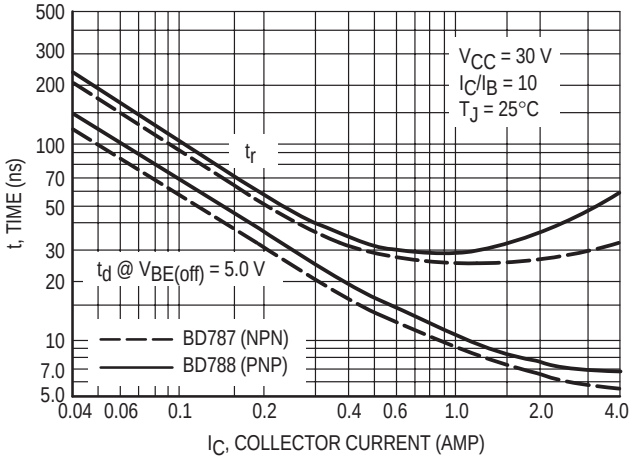


Figure 3. Turn–On Time

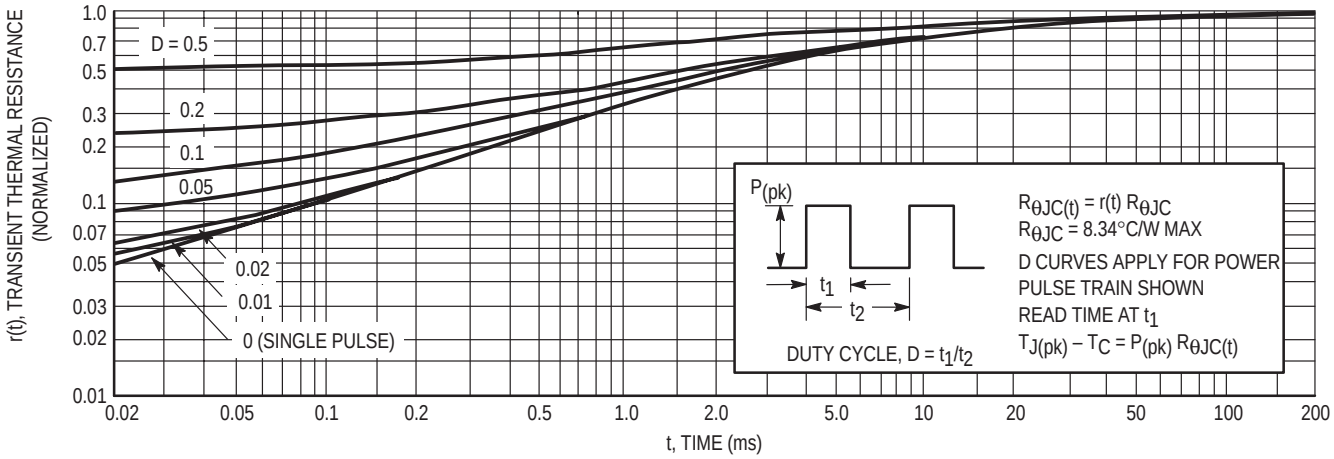


Figure 4. Thermal Response

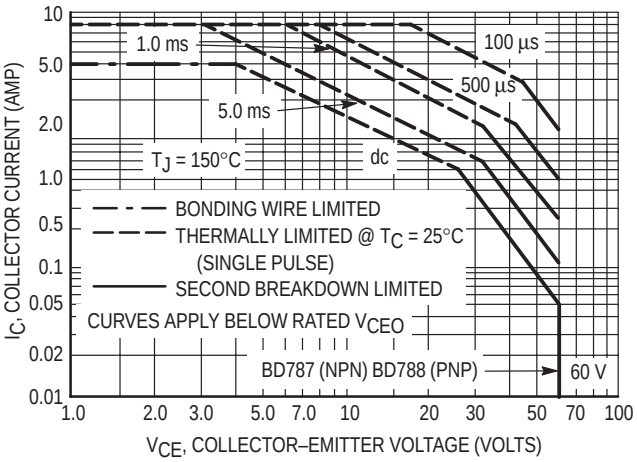


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C: T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$, $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

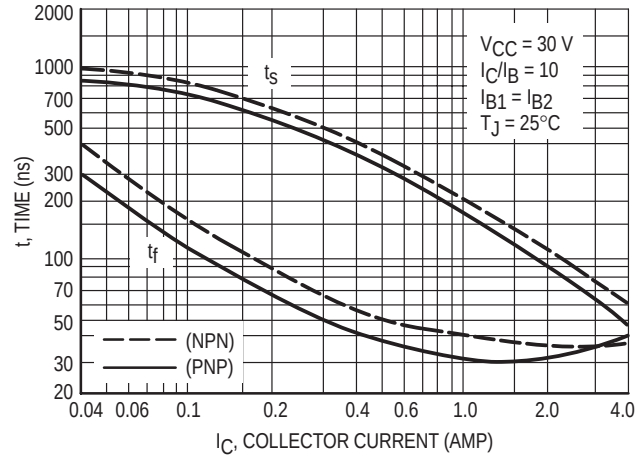


Figure 6. Turn–Off Time

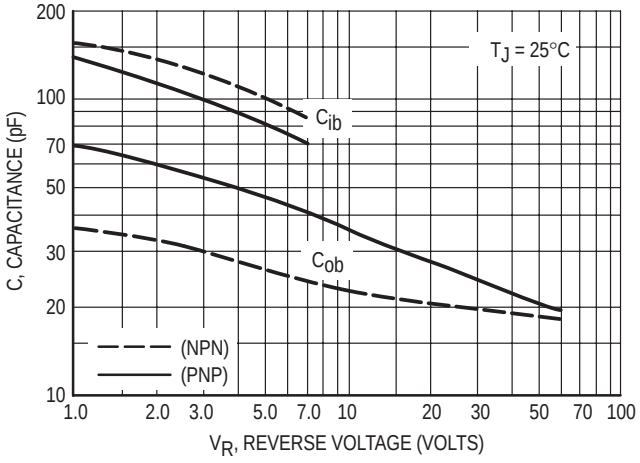
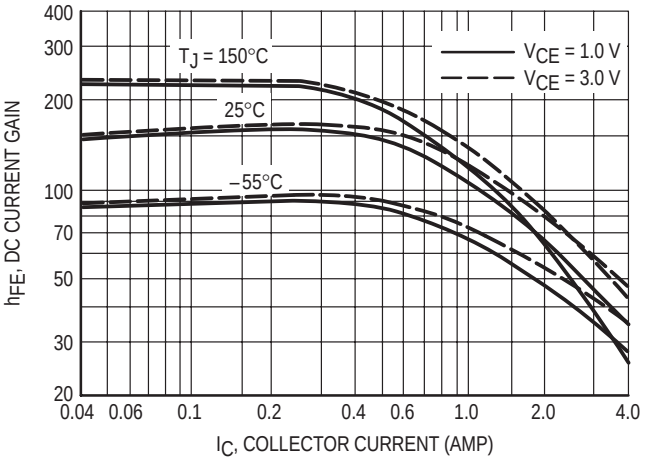


Figure 7. Capacitance

NPN
BD787



NPN
BD788

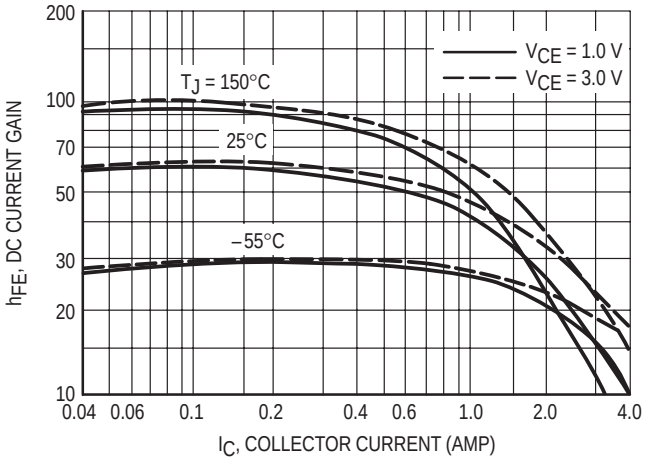
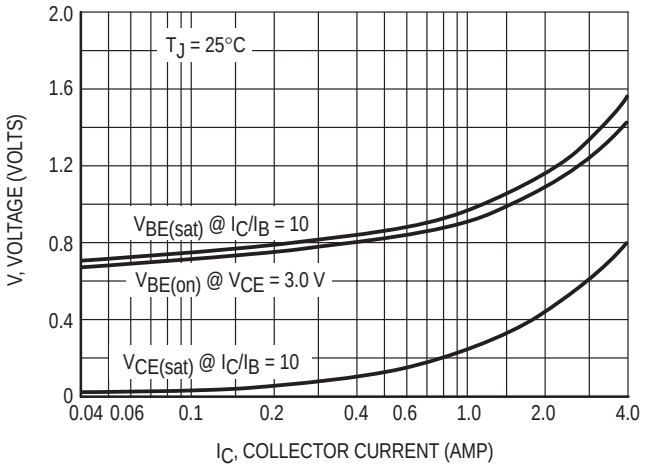


Figure 8. DC Current Gain



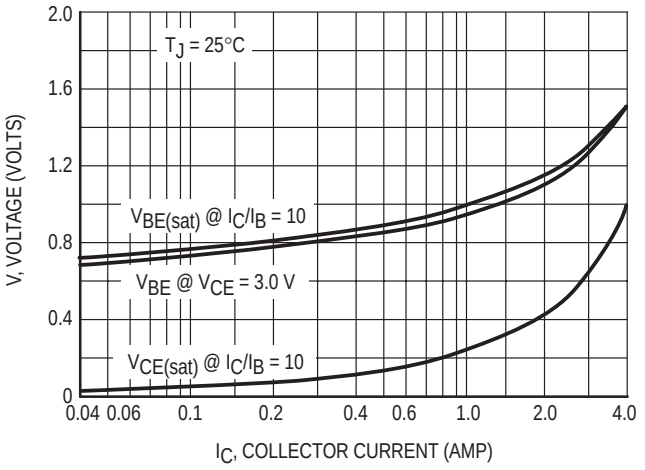
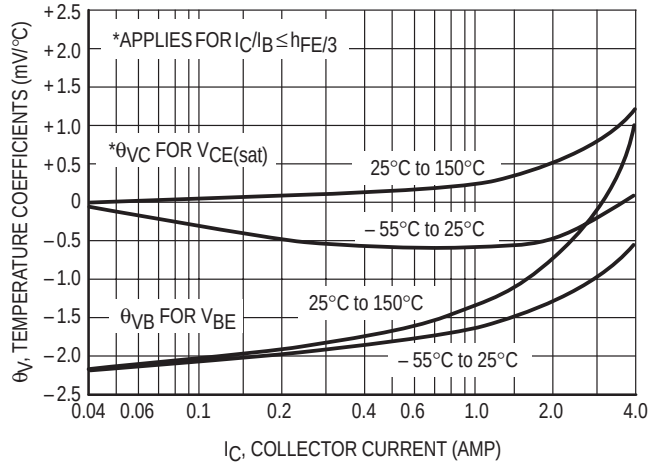


Figure 9. “On” Voltages



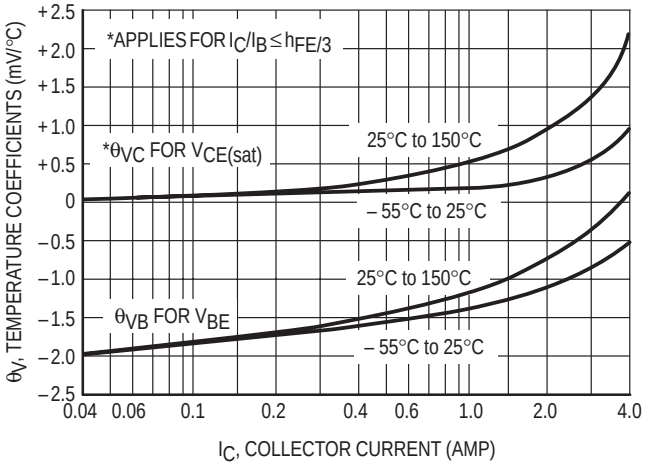


Figure 10. Temperature Coefficients

Complementary Plastic Silicon Power Transistors

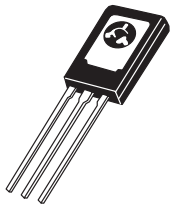
. . . designed for low power audio amplifier and low–current, high speed switching applications.

- High Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 80 Vdc (Min) — BD789, BD790
  = 100 Vdc (Min) — BD791, BD792
- High DC Current Gain @ I_C = 200 mAdc
  h_{FE} = 40–250
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.5 Vdc (Max) @ I_C = 500 mAdc
- High Current Gain — Bandwidth Product —
  f_T = 40 MHz (Min) @ I_C = 100 mAdc)

NPN
BD789
BD791*
PNP
BD790
BD792*

*Motorola Preferred Device

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
80, 100 VOLTS
15 WATTS



CASE 77–08
TO–225AA TYPE

***MAXIMUM RATINGS**

Rating	Symbol	BD789 BD790	BD791 BD792	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base Voltage	V_{EBO}	6.0		Vdc
Collector Current — Continuous — Peak	I_C	4.0 8.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.34	°C/W

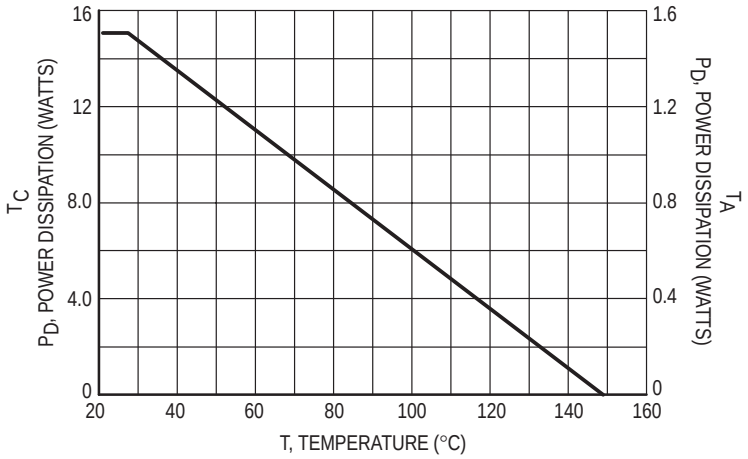


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

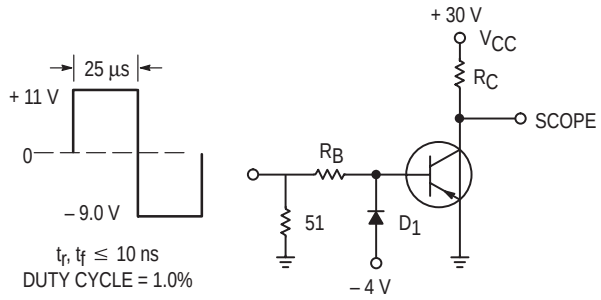
REV 7

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 10 mAdc, I_B = 0)	BD789, BD790		80	—	
	BD791, BD792		100	—	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 40 Vdc, I_B = 0)	BD789, BD790		—	100	
(V_{CE} = 50 Vdc, I_B = 0)	BD791, BD792		—	100	
Collector Cutoff Current		I_{CEX}			
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	BD789, BD790		—	1.0	μAdc
(V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	BD791, BD792		—	1.0	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1 5 Vdc, T_C = 125°C)	BD789, BD790		—	0.1	mAdc
(V_{CE} = 50 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	BD791, BD792		—	0.1	
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 200 mAdc, V_{CE} = 3 0 Vdc)			40	250	
(I_C = 1.0 Adc, V_{CE} = 3.0 Vdc)			20	—	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			10	—	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			5.0	—	
Collector Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			—	0.5	
(I_C = 1.0 Adc, I_B = 100 mAdc)			—	1.0	
(I_C = 2.0 Adc, I_B = 200 mAdc)			—	2.5	
(I_C = 4.0 Adc, I_B = 800 mAdc)			—	3.0	
Base–Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	—	1.8	Vdc
Base–Emitter On Voltage (I_C = 200 mAdc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product		f_T	40	—	MHz
(I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)					
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_C = 0, f = 0.1 MHz)	BD789, BD791		—	50	
	BD790, BD792		—	70	
Small–Signal Current Gain		h_{fe}	10	—	—
(I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)					

* Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



R_B AND R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, eg
MBR340 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA
FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES.

Figure 2. Switching Time Test Circuit

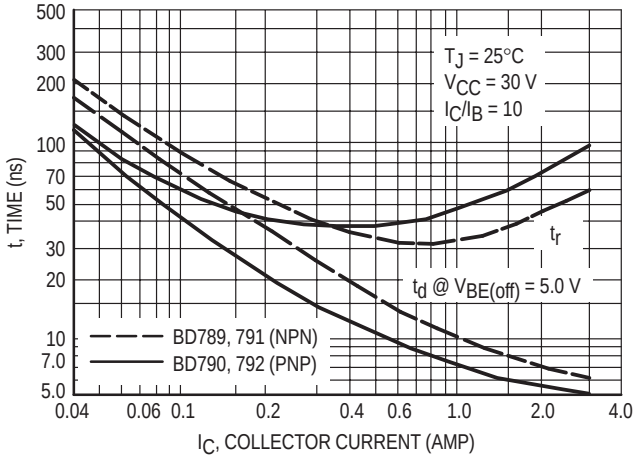


Figure 3. Turn–On Time

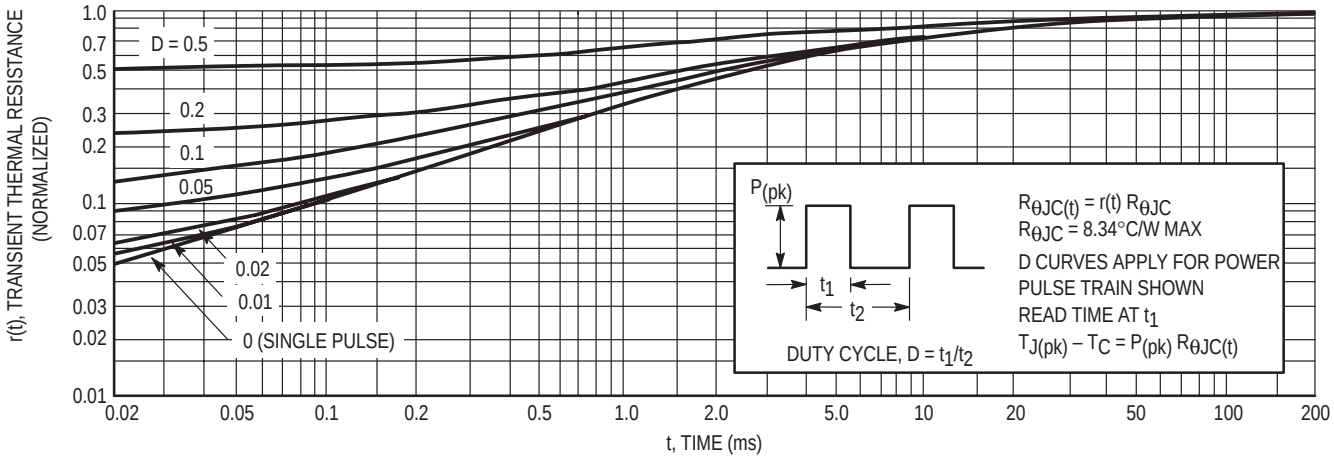


Figure 4. Thermal Response

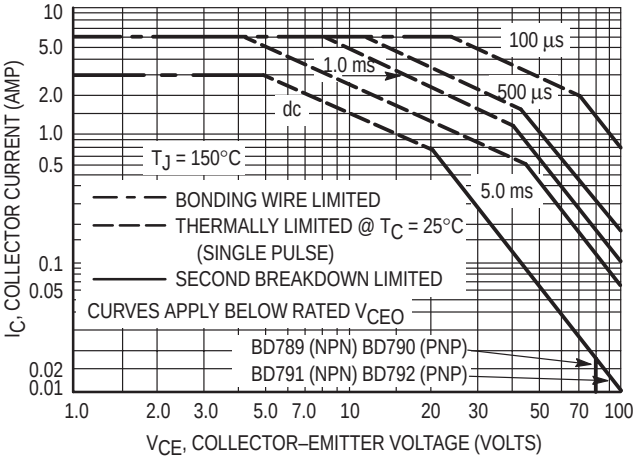


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C: T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C, $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

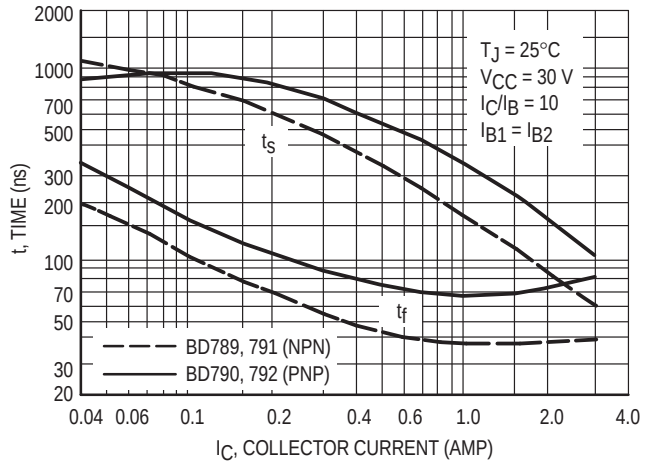


Figure 6. Turn–Off Time

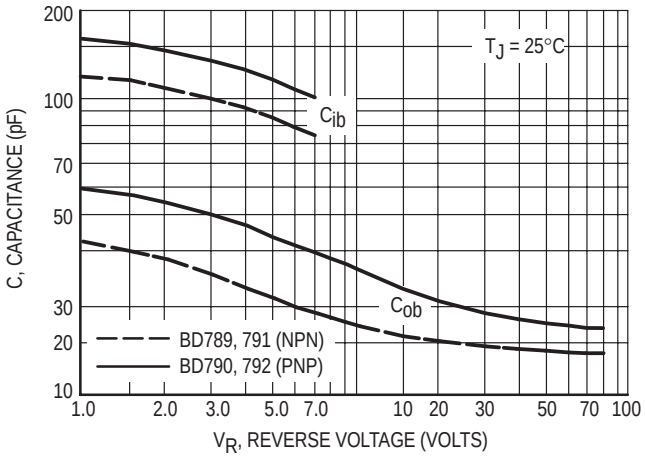
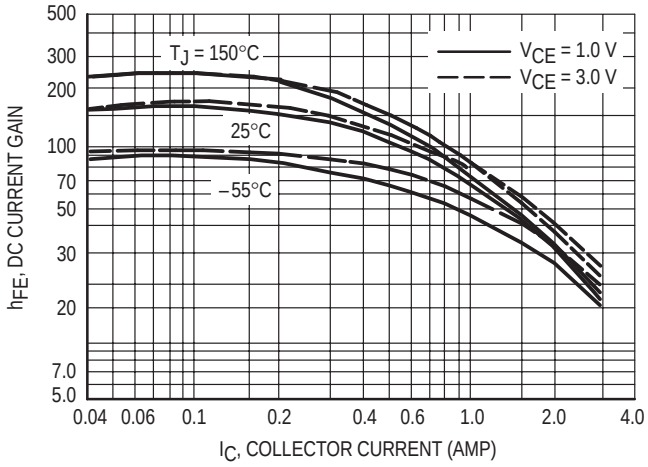


Figure 7. Capacitance

NPN
BD789, BD791



NPN
BD790, BD792

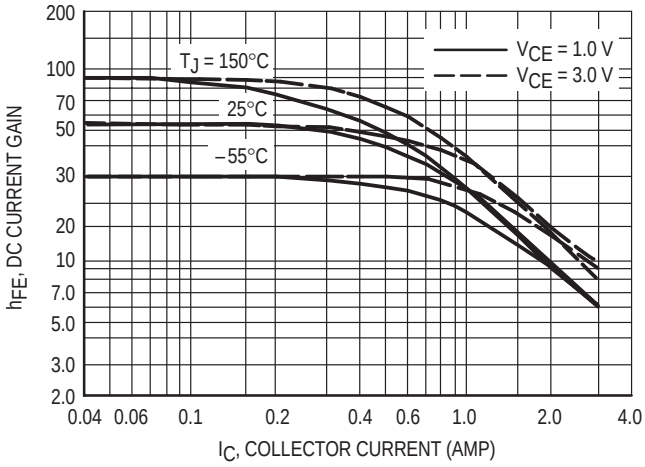
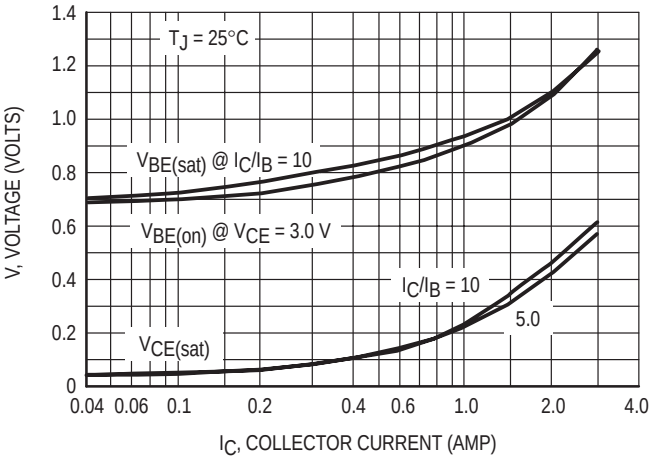


Figure 8. DC Current Gain



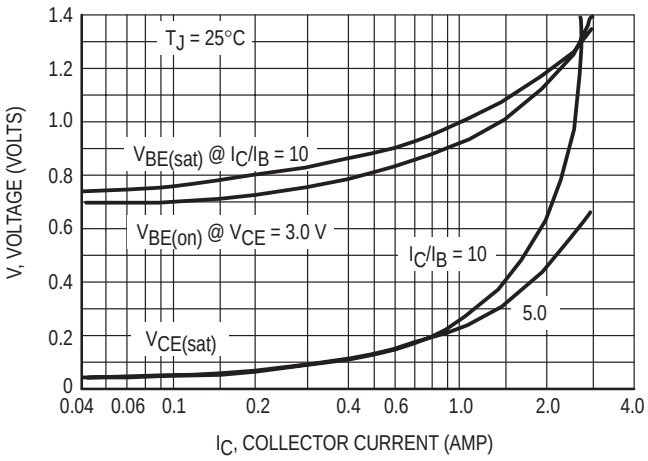
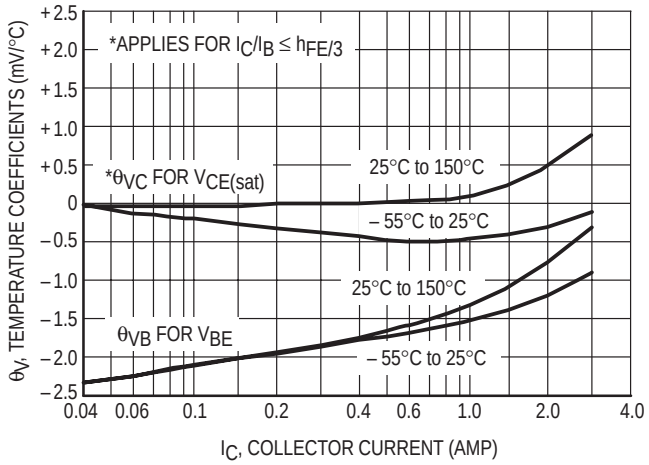


Figure 9. “On” Voltages



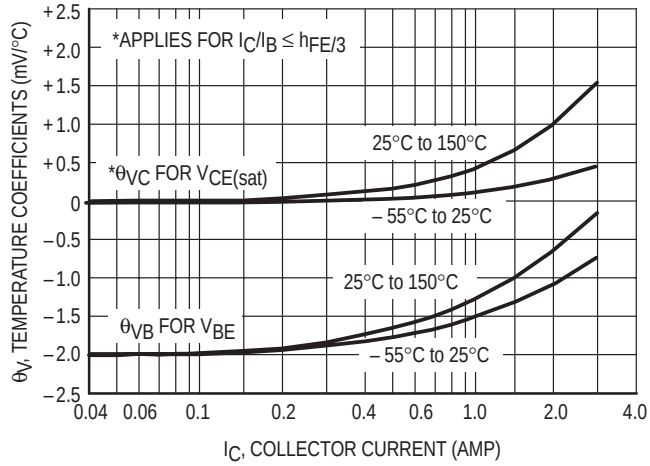


Figure 10. Temperature Coefficients

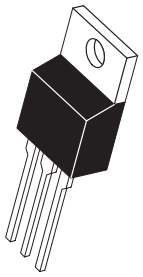
BD801

Plastic High Power Silicon NPN Transistor

8 AMPERE
POWER TRANSISTORS
NPN SILICON
100 VOLTS
65 WATTS

. . . designed for use up to 30 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 1.0 Adc
- BD801 is complementary with BD 798, 800, 802



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CBO}	100	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	8.0	Adc
Base Current	I_B	3.0	Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	65 522	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.92	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0) (I_C = 0.05 Adc, I_B = 0)	BV_{CEO}	100	—	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	0.1	—	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
DC Current Gain (I_C = 1.0 A, V_{CE} = 2.0 V) (I_C = 3.0 A, V_{CE} = 2.0 V)	h_{FE}	 30 15	 — —	
Collector–Emitter Saturation Voltage* (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$	—	1.0	Vdc
Base–Emitter On Voltage* (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.6	Vdc
Current–Gain Bandwidth Product (I_C = 0.25 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	3.0	—	MHz

* Pulse Test: Pulse Width ≤ 300 μs. Duty Cycle ≤ 2.0%.

REV 7

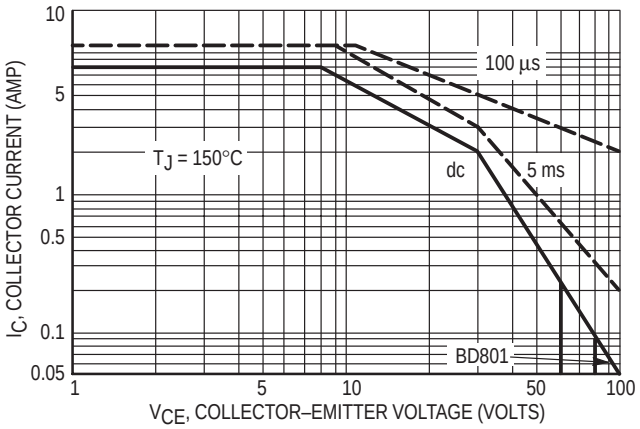


Figure 1. Active Region Safe Operating Area

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power–temperature derating must be observed for both steady state and pulse power conditions.

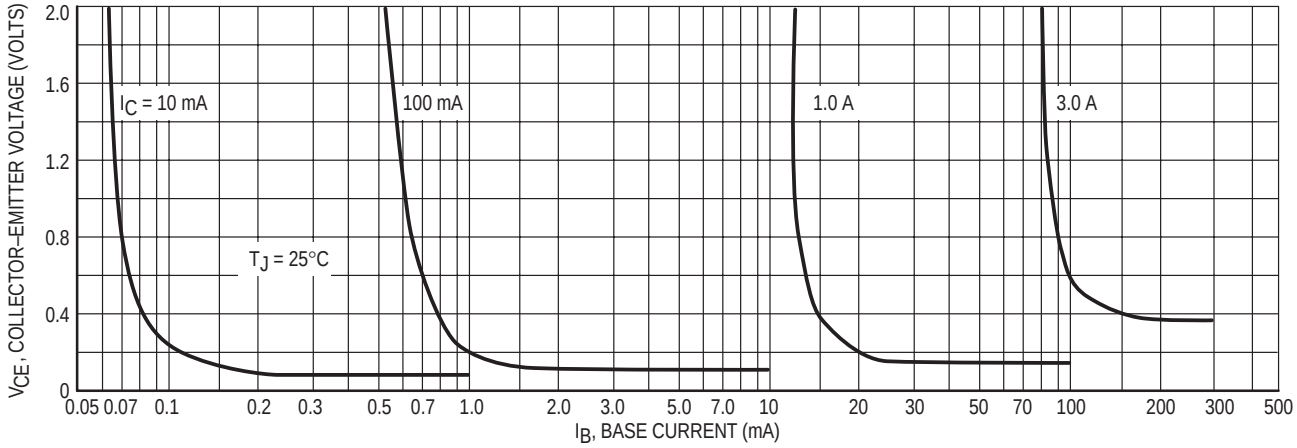


Figure 2. Collector Saturation Region

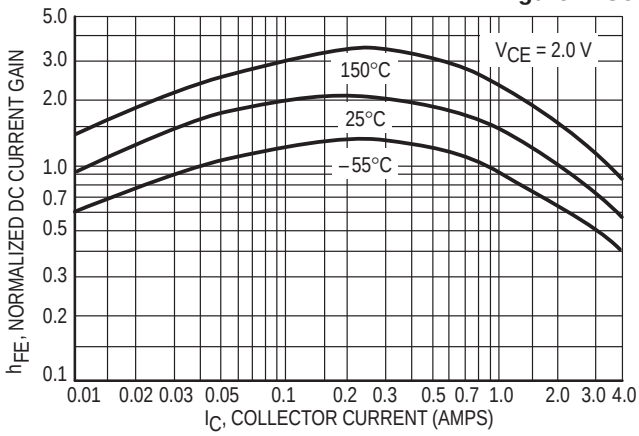


Figure 3. Normalized DC Current Gain

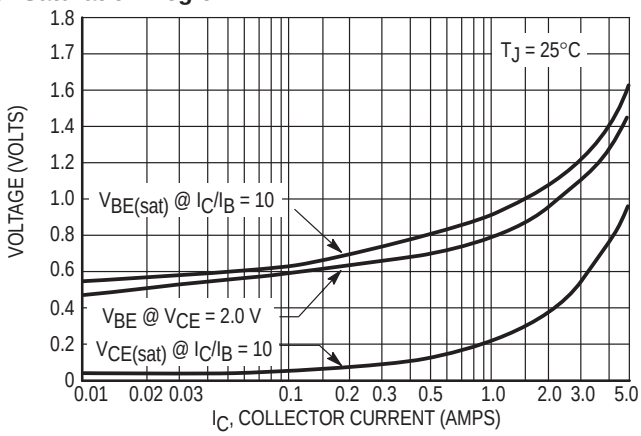


Figure 4. "On" Voltage

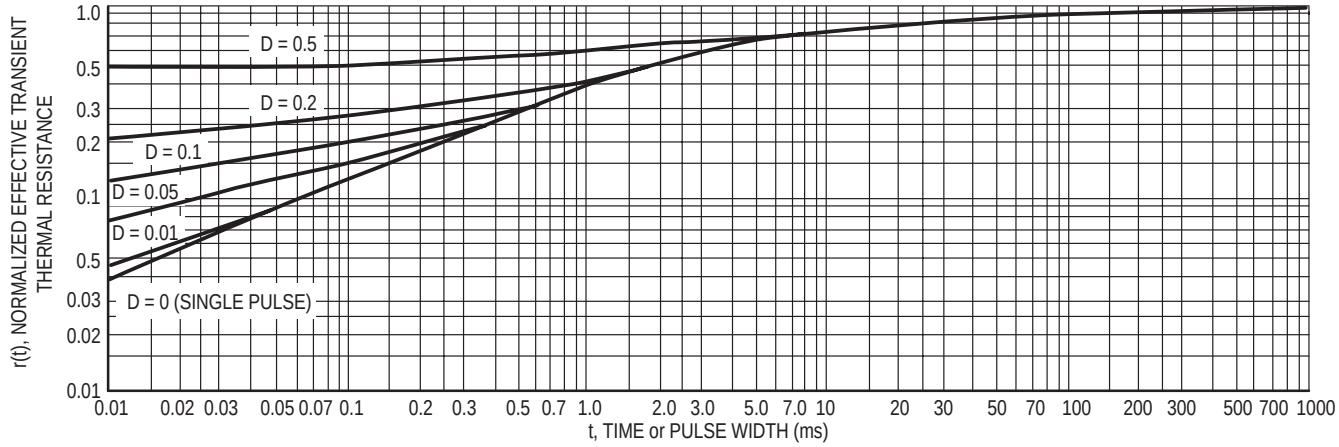


Figure 5. Thermal Response

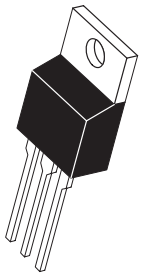
BD802

Plastic High Power Silicon PNP Transistor

8 AMPERE
POWER TRANSISTORS
PNP SILICON
100 VOLTS
65 WATTS

. . . designed for use up to 30 Watt audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 1.0 Adc
- BD802 is complementary with BD 795, 797, 799, 801



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CBO}	100	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	8.0	Adc
Base Current	I_B	3.0	Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D	65 522	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.92	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.05 Adc, I_B = 0)	BV_{CEO}	100	—	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
DC Current Gain (I_C = 1.0 A, V_{CE} = 2.0 V) (I_C = 3.0 A, V_{CE} = 2.0 V)	h_{FE}	 30 15	 — —	
Collector–Emitter Saturation Voltage* (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$	—	1.0	Vdc
Base–Emitter On Voltage* (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.6	Vdc
Current–Gain — Bandwidth Product (I_C = 0.25 Adc, V_{CE} = 10 Vdc, f = MHz)	f_T	3.0	—	MHz

* Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0.

REV 7

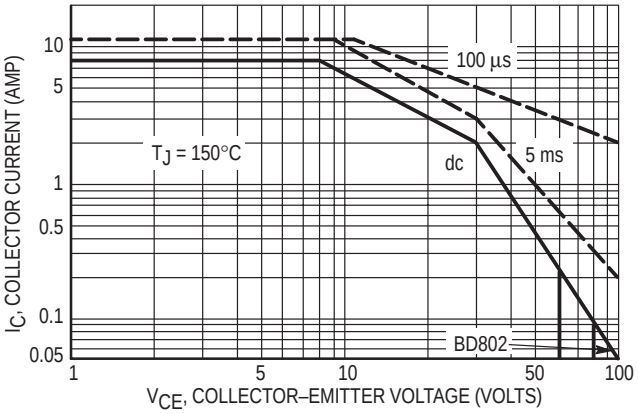


Figure 1. Active Region Safe Operating Area

The Safe Operating Area Curves indicate $I_C - V_{CE}$ limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power–temperature derating must be observed for both steady state and pulse power conditions.

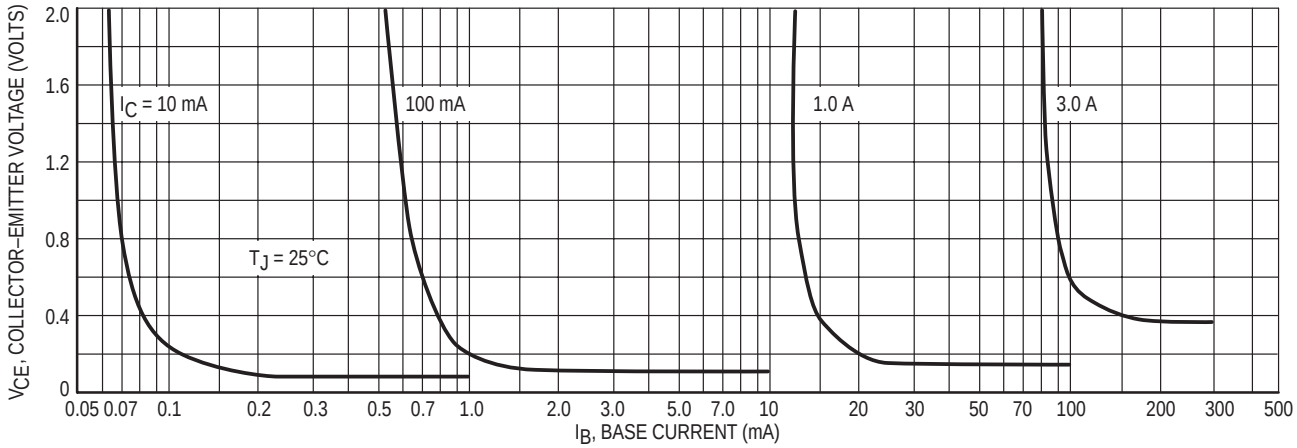


Figure 2. Collector Saturation Region

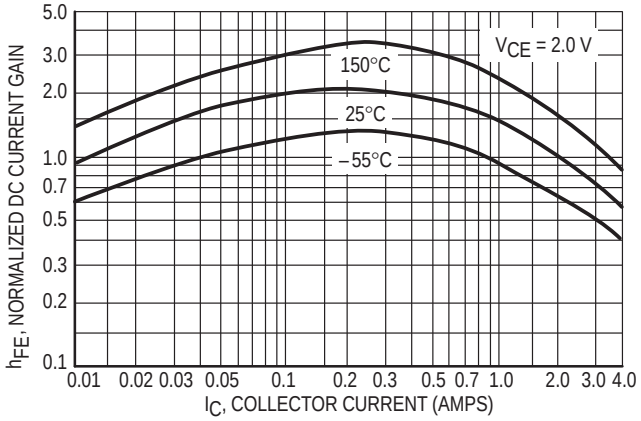


Figure 3. Normalized DC Current Gain

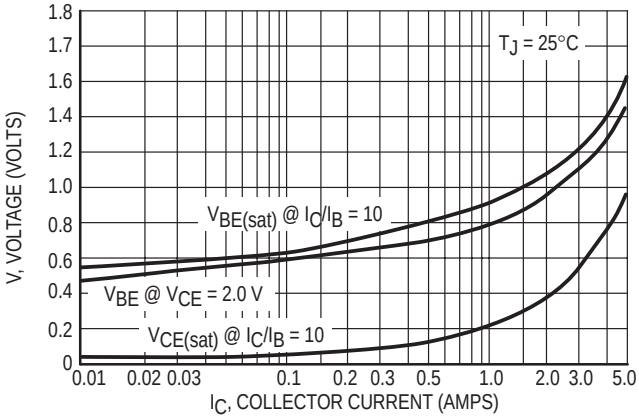


Figure 4. "On" Voltage

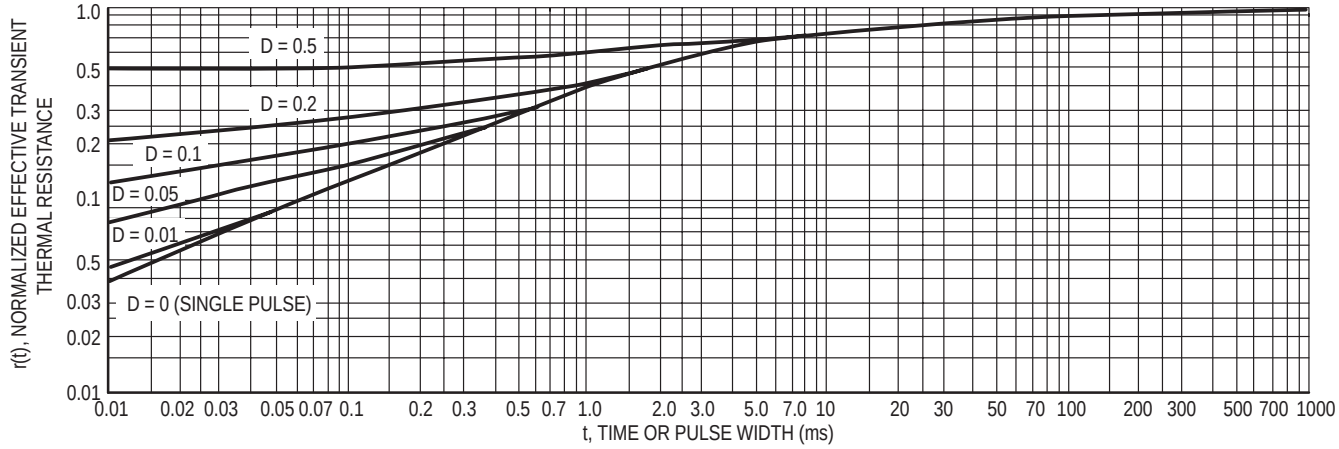


Figure 5. Thermal Response

BD808
BD810*

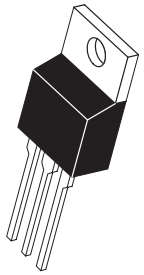
*Motorola Preferred Device

Plastic High Power Silicon PNP Transistor

. . . designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 30 (Min) @ I_C = 2.0 Adc
- BD 808, 810 are complementary with BD 807, 890

10 AMPERE
POWER TRANSISTORS
PNP SILICON
60, 80 VOLTS
90 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector–Emitter Voltage	V_{CEO}	BD808 BD810	60 80	Vdc
Collector–Base Voltage	V_{CBO}	BD808 BD810	70 80	Vdc
Emitter–Base Voltage	V_{EBO}		5.0	Vdc
Collector Current	I_C		10	Adc
Base Current	I_B		6.0	Adc
Total Device Dissipation T_C = 25°C Derate above 25°C	P_D		90 720	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.39	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.1 Adc, I_B = 0)	BV_{CEO}	BD808 BD810	60 80	— —	Vdc
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	 BD808 BD810	 — —	 1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	2.0	mAdc
DC Current Gain (I_C = 2.0 A, V_{CE} = 2.0 V) (I_C = 4.0 A, V_{CE} = 2.0 V)	h_{FE}		 30 15	 — —	
Collector–Emitter Saturation Voltage* (I_C = 3.0 Adc, I_B = 0.3 Adc)	$V_{CE(sat)}$		—	1.1	Vdc
Base–Emitter On Voltage* (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$		—	1.6	Vdc
Current–Gain Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T		1.5	—	MHz

* Pulse Test: Pulse Width ≦ 300 μs, Duty Cycle ≦ 2.0%.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

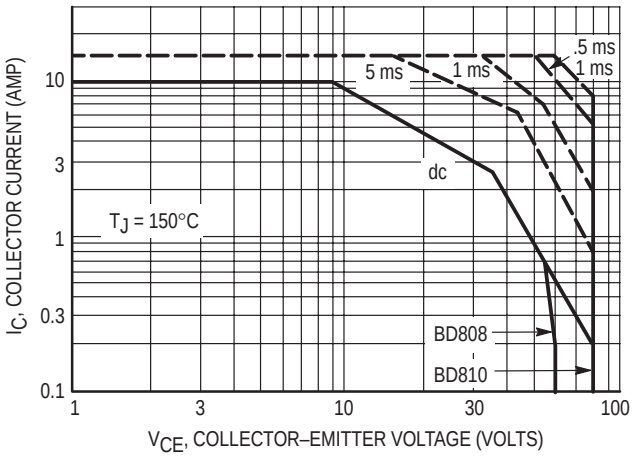


Figure 1. Active Region DC Safe Operating Area (see Note 1)

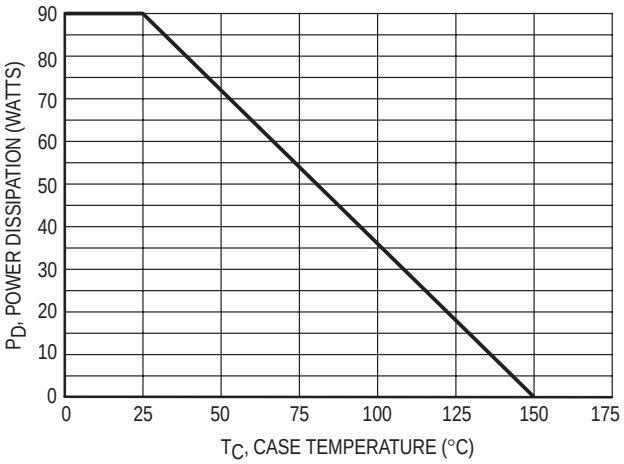


Figure 2. Power–Temperature Derating Curve

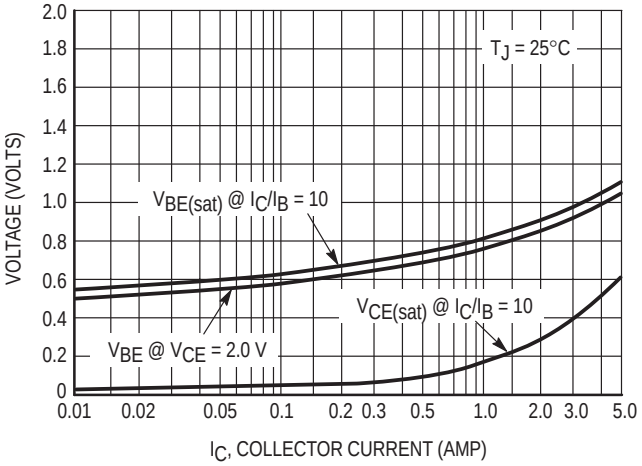


Figure 3. "On" Voltages

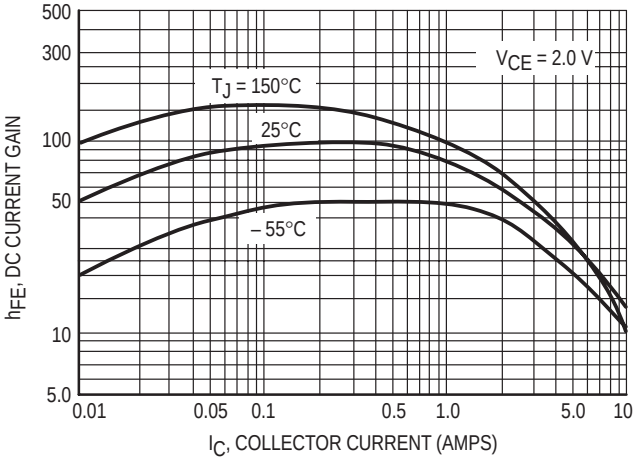


Figure 4. Current Gain

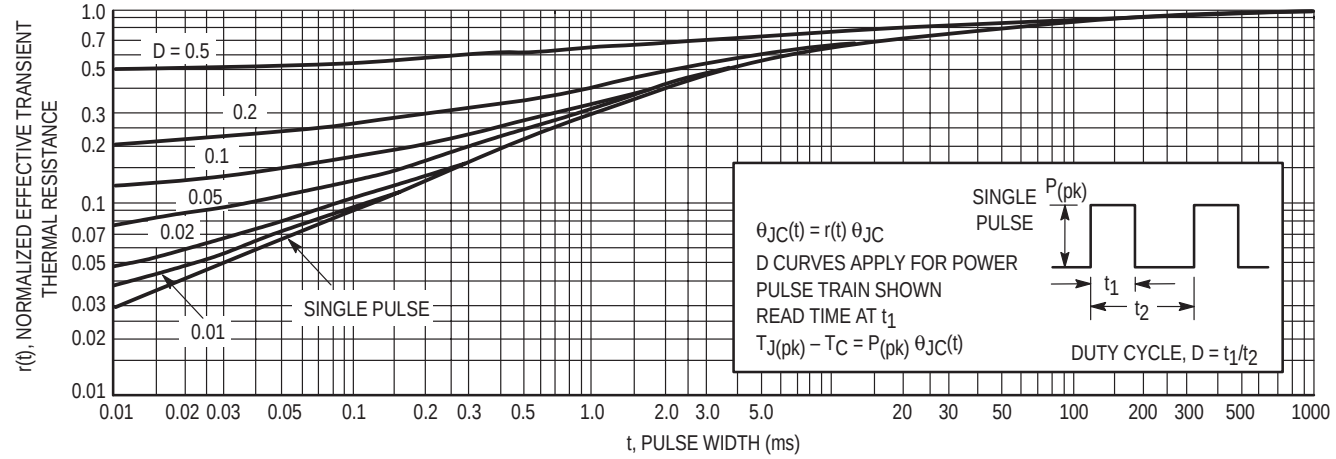


Figure 5. Thermal Response

Note 1:

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

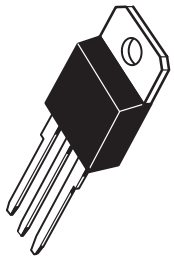
Complementary Silicon Plastic Power Darlingtons

. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain
  HFE = 1000 (min.) @ 5 Adc
- Monolithic Construction with Built–in Base Emitter Shunt Resistors

NPN
BDV65B
PNP
BDV64B

DARLINGTONS
10 AMPERES
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60 – 80 – 100 – 120 VOLTS
125 WATTS



CASE 340D–01
SOT 93, TO–218 TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C	10 20	Adc
Base Current	I_B	0.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 125 1.0	 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	°C/W

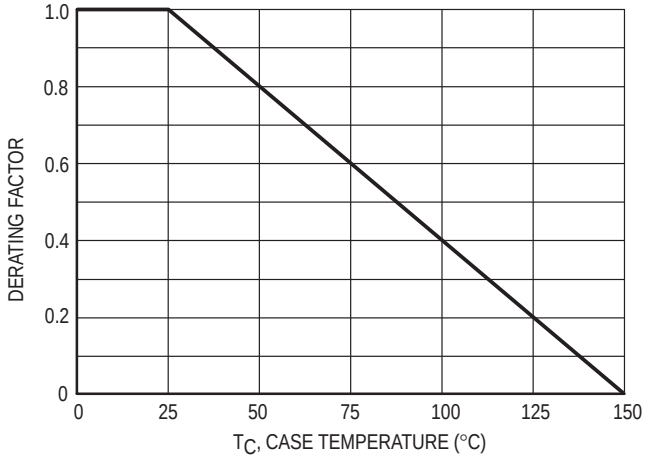


Figure 1. Power Derating

REV 7

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	0.4	mAdc
Collector Cutoff Current (V_{CB} = 50 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	—	2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	1000	—	—
Collector–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.02 Adc)	$V_{CE(sat)}$	—	2.0	Vdc
Base–Emitter Saturation Voltage (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	2.5	Vdc

NPN

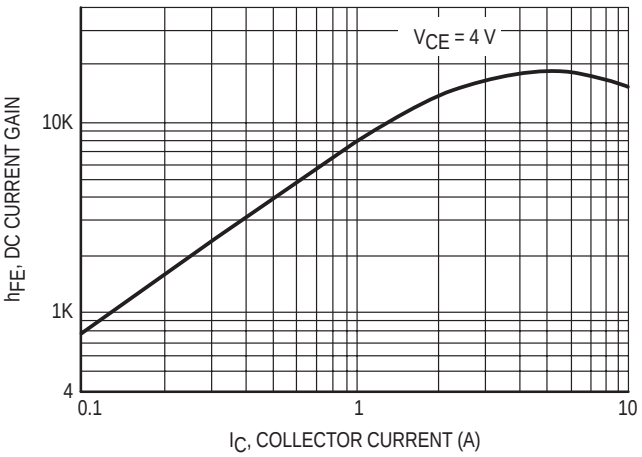


Figure 2. DC Current Gain

PNP

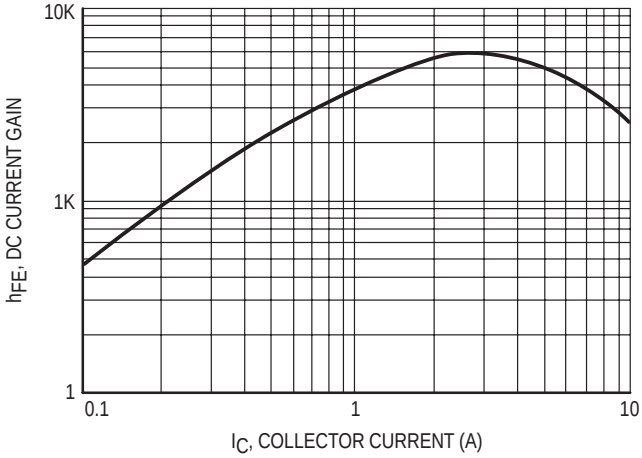


Figure 3. DC Current Gain

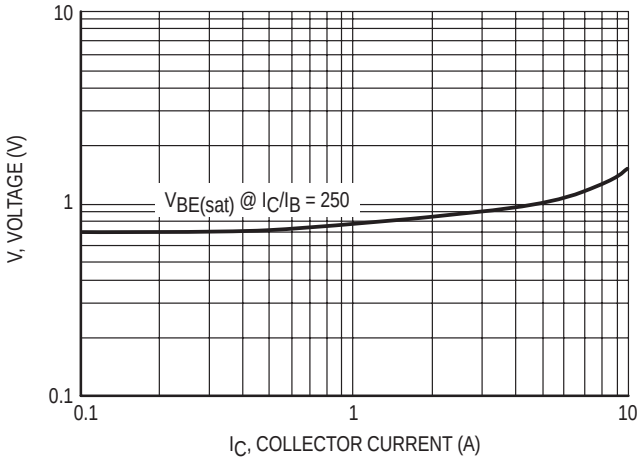


Figure 4. “On” Voltages

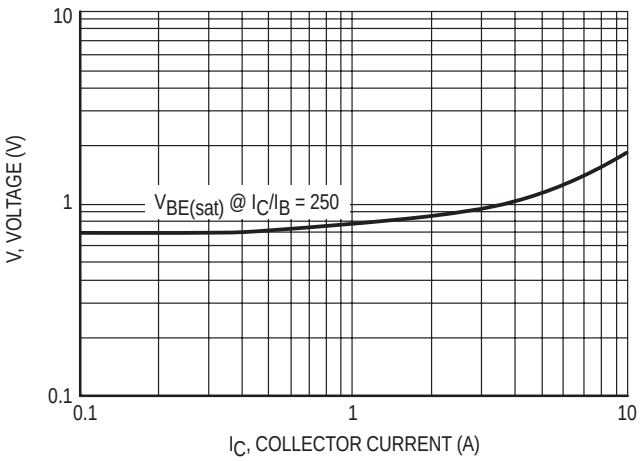


Figure 5. “On” Voltages

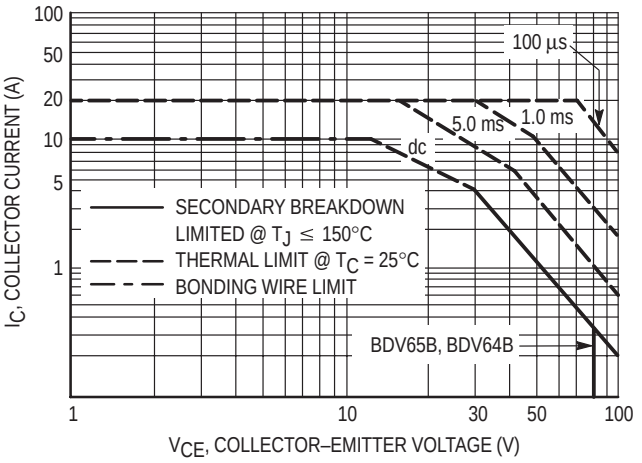


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)}$ = 150°C, T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 7. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

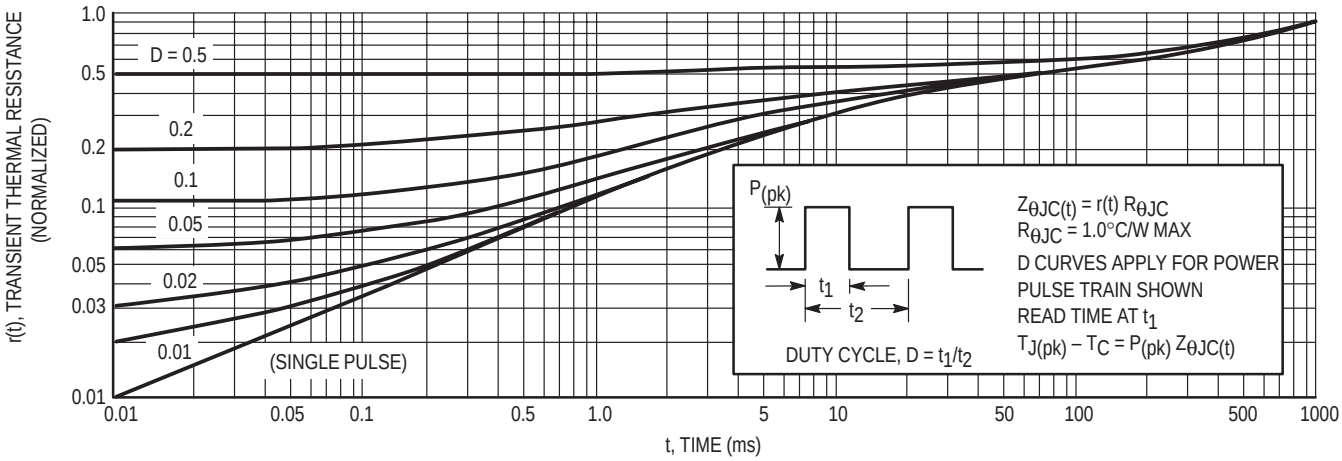


Figure 7. Thermal Response

Darlington Complementary Silicon Power Transistors

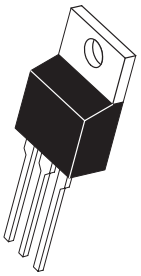
. . . designed for general purpose and low speed switching applications.

- High DC Current Gain – h_{FE} = 2500 (typ.) @ I_C = 5.0 Adc.
- Collector Emitter Sustaining Voltage @ 30 mAdc:
  $V_{CEO(sus)}$ = 80 Vdc (min.) — BDW46
  100 Vdc (min.) — BDW42/BDW47
- Low Collector Emitter Saturation Voltage
  $V_{CE(sat)}$ = 2.0 Vdc (max.) @ I_C = 5.0 Adc
  3.0 Vdc (max.) @ I_C = 10.0 Adc
- Monolithic Construction with Built–In Base Emitter Shunt resistors
- TO–220AB Compact Package

NPN
BDW42*
PNP
BDW46
BDW47*

***Motorola Preferred Device**

DARLINGTON
15 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80 – 100 VOLTS
85 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BDW46	BDW42 BDW47	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	15		Adc
Base Current	I_B	0.5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	85 0.68		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.47	°C/W

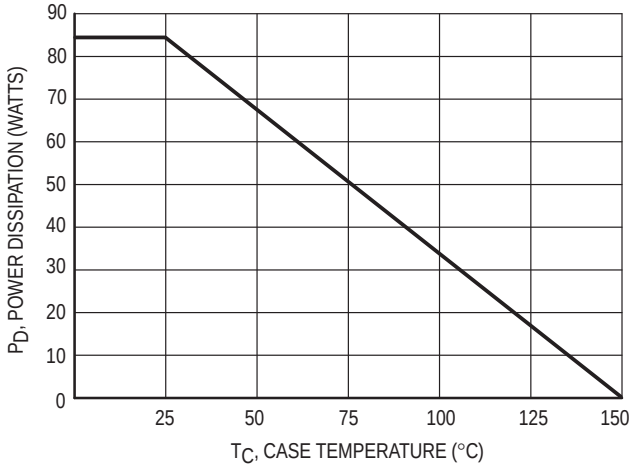


Figure 1. Power Temperature Derating Curve

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	BDW46		80	—	
	BDW42/BDW47		100	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 40 Vdc, I_B = 0)	BDW46		—	2.0	
(V_{CE} = 50 Vdc, I_B = 0)	BDW42/BDW47		—	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 80 Vdc, I_E = 0)	BDW41/BDW46		—	1.0	
(V_{CB} = 100 Vdc, I_E = 0)	BDW42/BDW47		—	1.0	
Emitter Cutoff Current		I_{EBO}	—	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			
(I_C = 5.0 Adc, V_{CE} = 4.0 Vdc)			1000	—	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)			250	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 10 mAdc)			—	2.0	
(I_C = 10 Adc, I_B = 50 mAdc)			—	3.0	
Base–Emitter On Voltage		$V_{BE(on)}$	—	3.0	Vdc
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)					
SECOND BREAKDOWN (2)					
Second Breakdown Collector		$I_{S/b}$			Adc
Current with Base Forward Biased					
BDW42	V_{CE} = 28.4 Vdc		3.0	—	
	V_{CE} = 40 Vdc		1.2	—	
BDW46/BDW47	V_{CE} = 22.5 Vdc		3.8	—	
	V_{CE} = 36 Vdc		1.2	—	
DYNAMIC CHARACTERISTICS					
Magnitude of common emitter small signal short circuit current transfer ratio		f_T	4.0	—	MHz
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)					
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	BDW42		—	200	
	BDW46/BDW47		—	300	
Small–Signal Current Gain		h_{fe}	300	—	
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)					

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.
(2) Pulse Test non repetitive: Pulse Width = 250 ms.

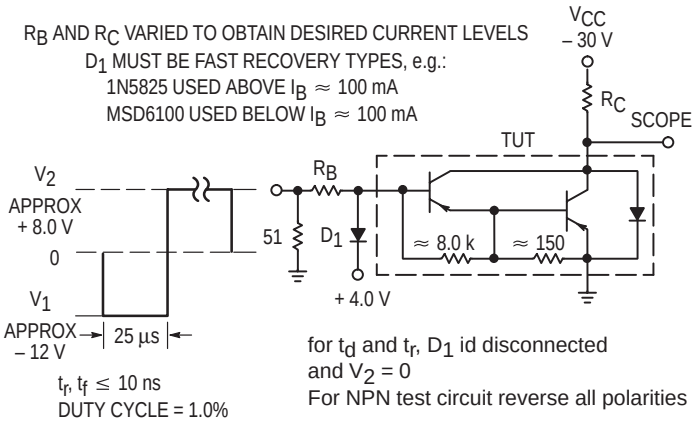


Figure 2. Switching Times Test Circuit

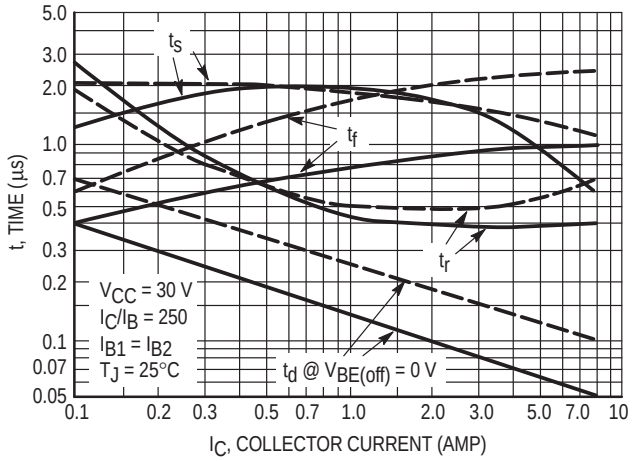


Figure 3. Switching Times

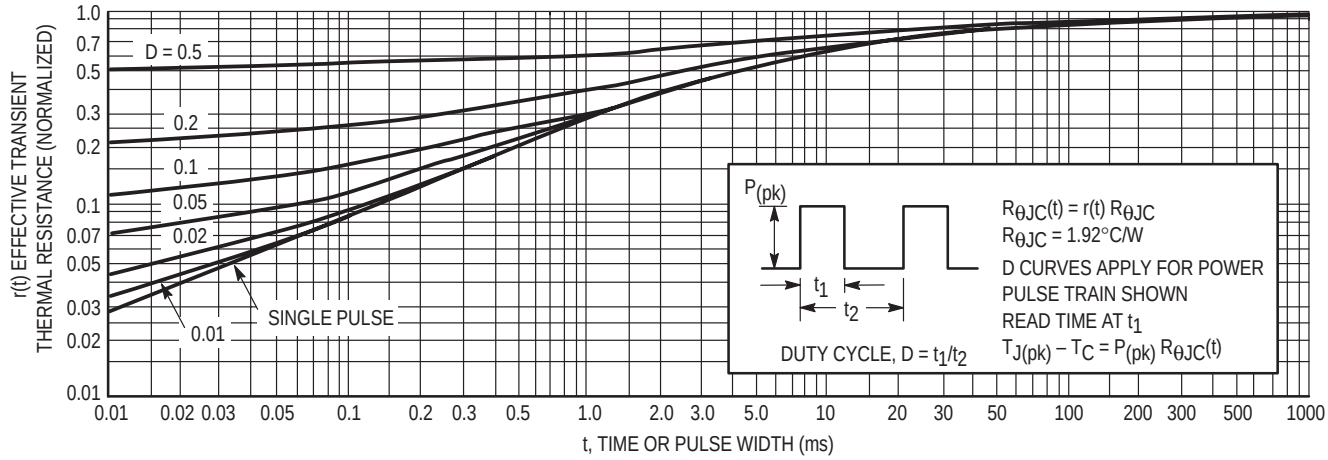


Figure 4. Thermal Response

ACTIVE–REGION SAFE OPERATING AREA

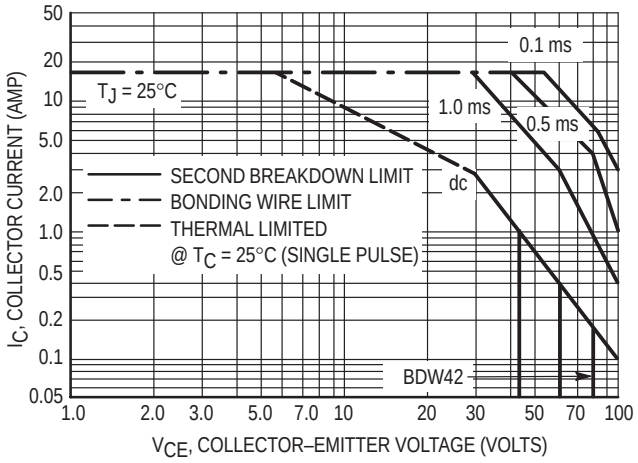


Figure 5. BDW42

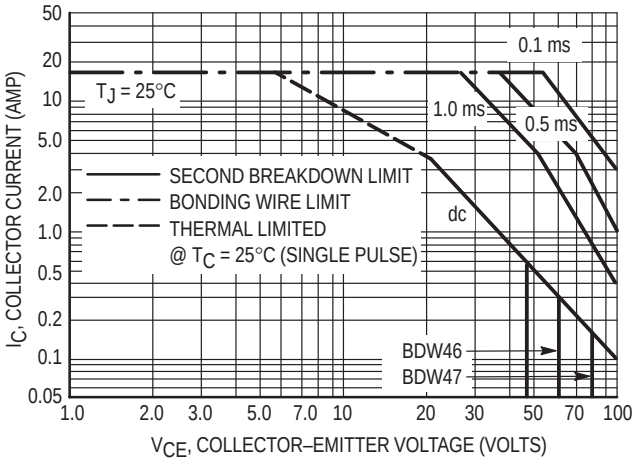


Figure 6. BDW46 and BDW47

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Fig. 5 and 6 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Fig. 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

* Linear extrapolation

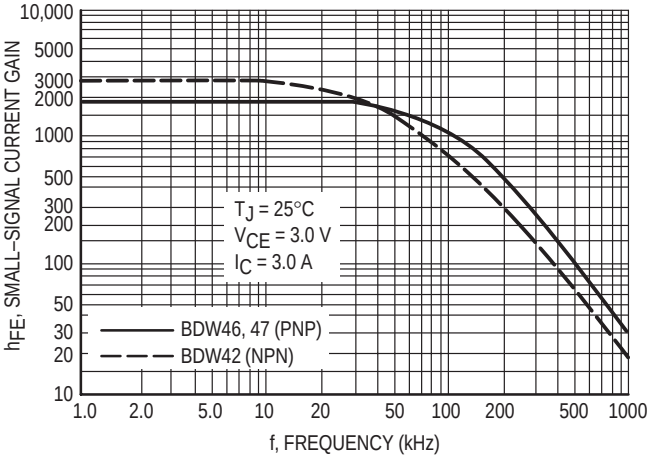


Figure 7. Small–Signal Current Gain

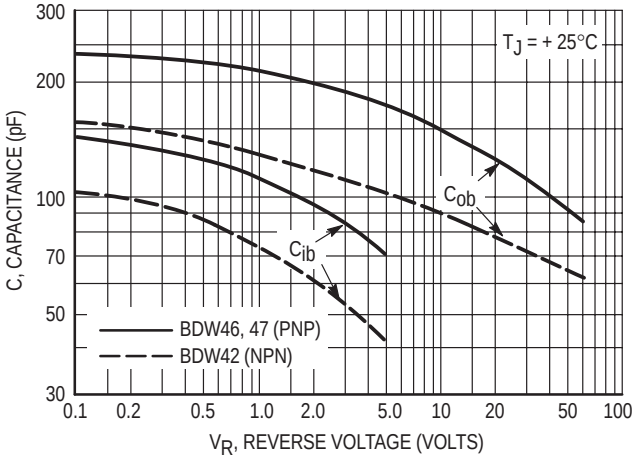


Figure 8. Capacitance

BDW40, 41, 42 (NPN) **BDW45, 46, 47 (PNP)**

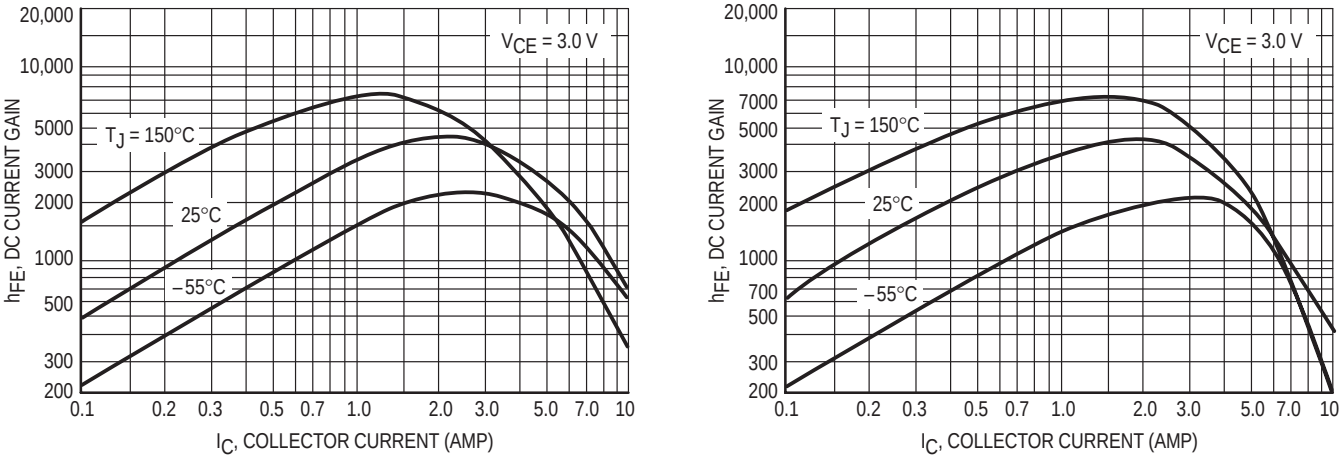


Figure 9. DC Current Gain

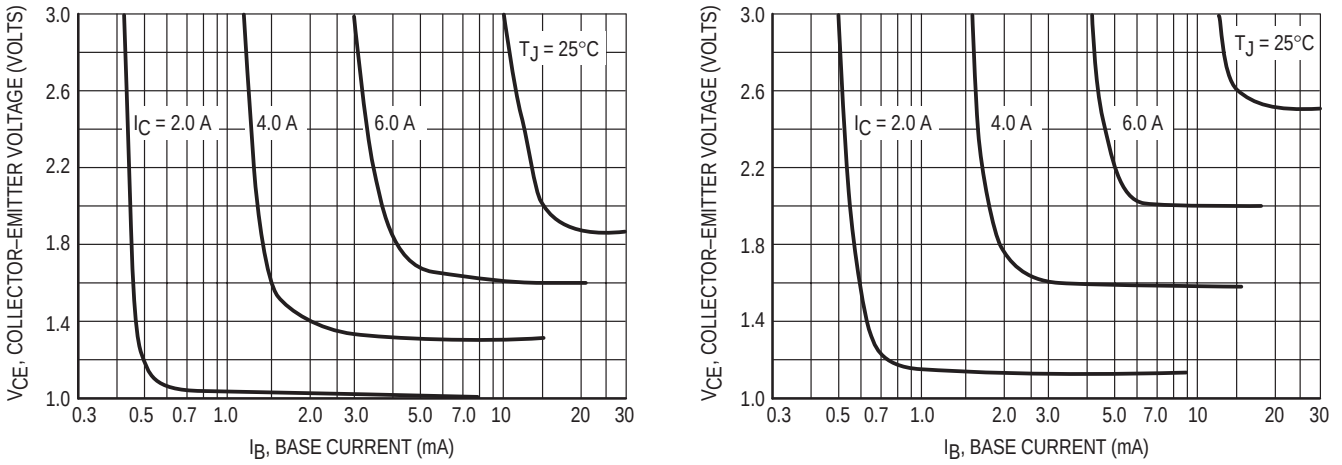


Figure 10. Collector Saturation Region

BDW40, 41, 42 (NPN) **BDW45, 46, 47 (PNP)**

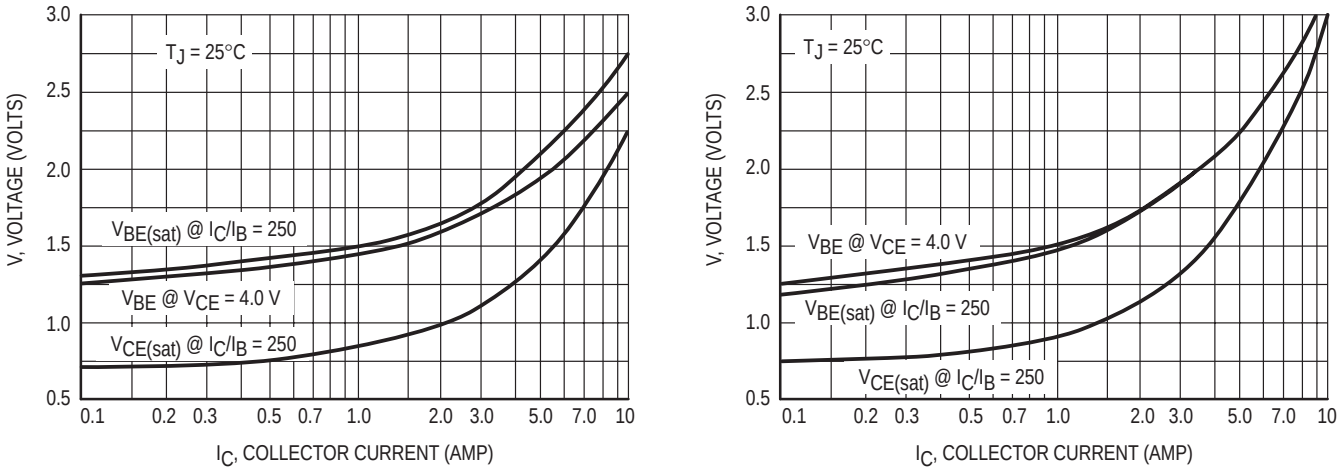


Figure 11. “On” Voltages

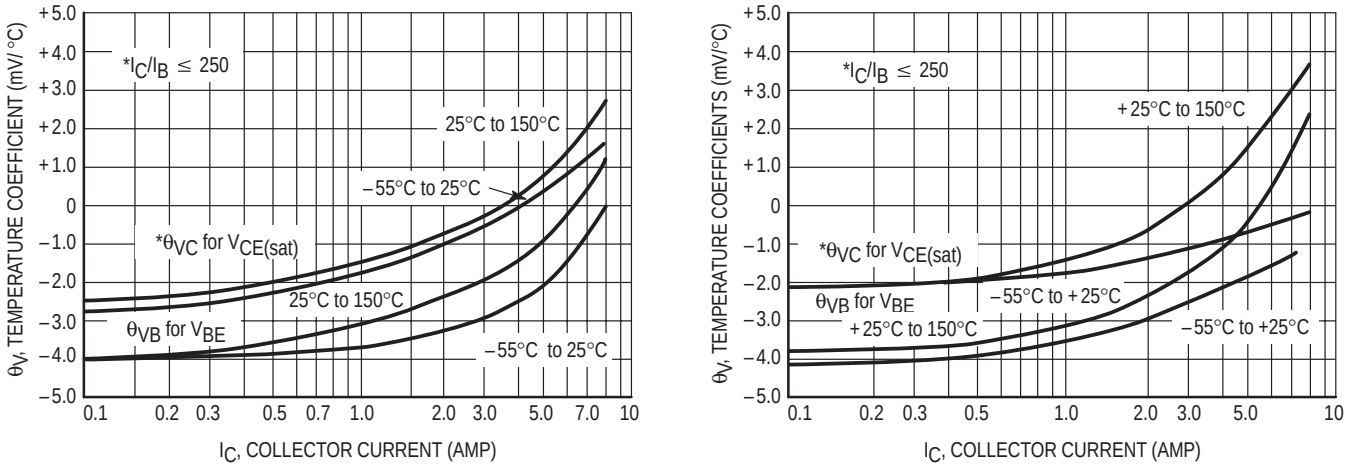


Figure 12. Temperature Coefficients

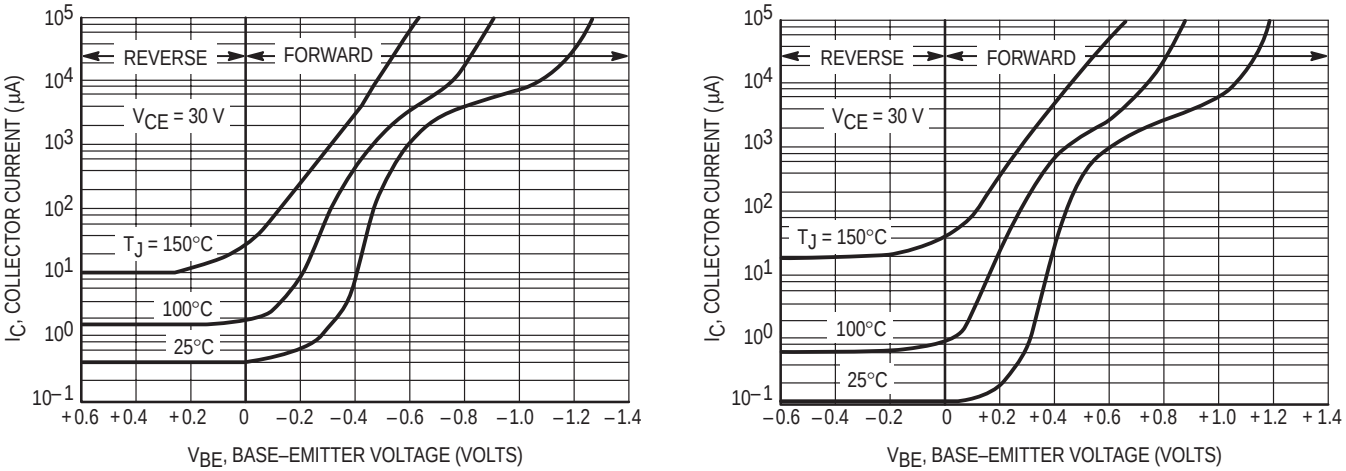


Figure 13. Collector Cut–Off Region

Figure 14. Darlington Schematic

Darlington Complementary Silicon Power Transistors

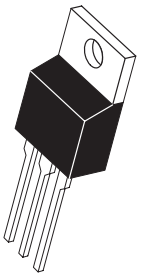
. . . designed for general purpose and low speed switching applications.

- High DC Current Gain — h_{FE} = 2500 (typ.) at I_C = 4.0
- Collector–Emitter Sustaining Voltage at 100 mAdc
  $V_{CEO(sus)}$ = 80 Vdc (min.) — BDX33B, 34B
  100 Vdc (min.) — BDX33C, 34C
- Low Collector–Emitter Saturation Voltage
  $V_{CE(sat)}$ = 2.5 Vdc (max.) at I_C = 3.0 Adc — BDX33B, 33C/34B, 34C
- Monolithic Construction with Build–In Base–Emitter Shunt resistors
- TO–220AB Compact Package

NPN
BDX33B
BDX33C*
PNP
BDX34B
BDX34C*

***Motorola Preferred Device**

DARLINGTON
10 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80 – 100 VOLTS
70 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BDX33B BDX34B	BDX33C BDX34C	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	10 15		Adc
Base Current	I_B	0.25		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	 70 0.56		 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.78	°C/W

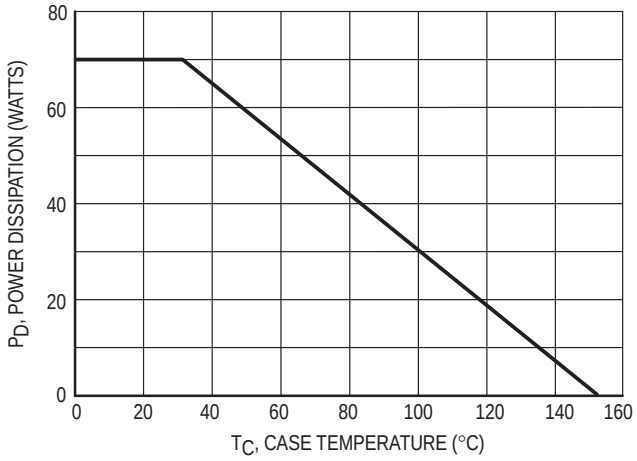


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0)	BDX33B/BDX34B BDX33C/BDX34C	$V_{CEO(sus)}$	 80 100	 — —	Vdc
Collector–Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0, R_{BE} = 100)	BDX33B/BDX34B BDX33C/BDX33C	$V_{CER(sus)}$	 80 100	 — —	Vdc
Collector–Emitter Sustaining Voltage[1] (I_C = 100 mAdc, I_B = 0, V_{BE} = 1.5 Vdc)	BDX33B/BDX34B BDX33C/BDX34C	$V_{CEX(sus)}$	 80 100	 — —	Vdc
Collector Cutoff Current (V_{CE} = 1/2 rated V_{CEO}, I_B = 0)	T_C = 25°C T_C = 100°C	I_{CEO}	 — —	 0.5 10	mAdc
Collector Cutoff Current (V_{CB} = rated V_{CBO}, I_E = 0)	T_C = 25°C T_C = 100°C	I_{CBO}	 — —	 1.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	10	mAdc
ON CHARACTERISTICS					
DC Current Gain[1] (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	BDX33B, 33C/34B, 34C	h_{FE}	750	—	—
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 6.0 mAdc)	BDX33B, 33C/34B, 34C	$V_{CE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	BDX33B, 33C/34B, 34C	$V_{BE(on)}$	—	2.5	Vdc
Diode Forward Voltage (I_C = 8.0 Adc)		V_F	—	4.0	Vdc

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
[2] Pulse Test non repetitive: Pulse Width = 0.25 s.

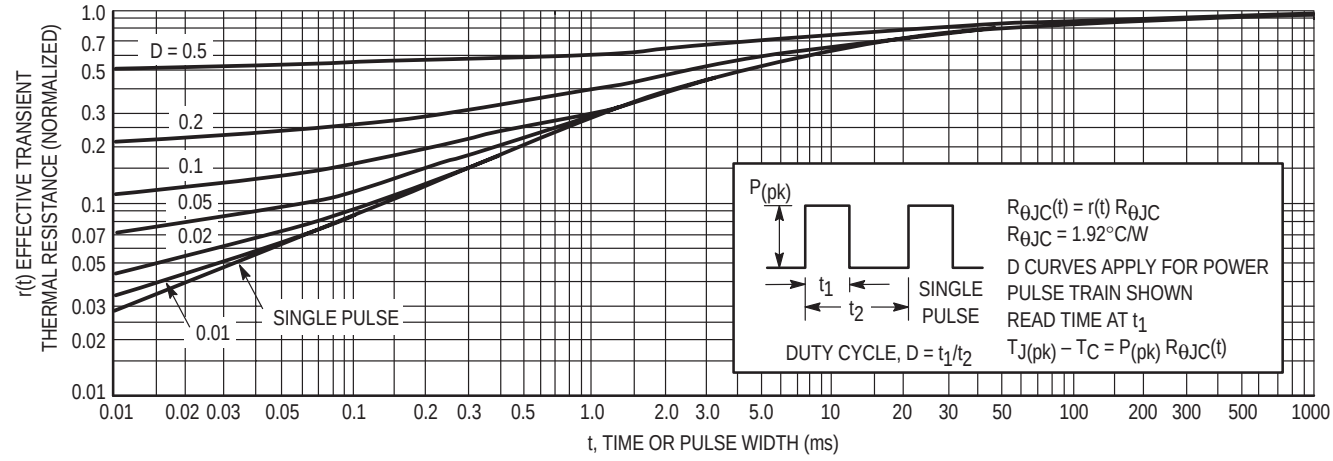


Figure 1. Thermal Response

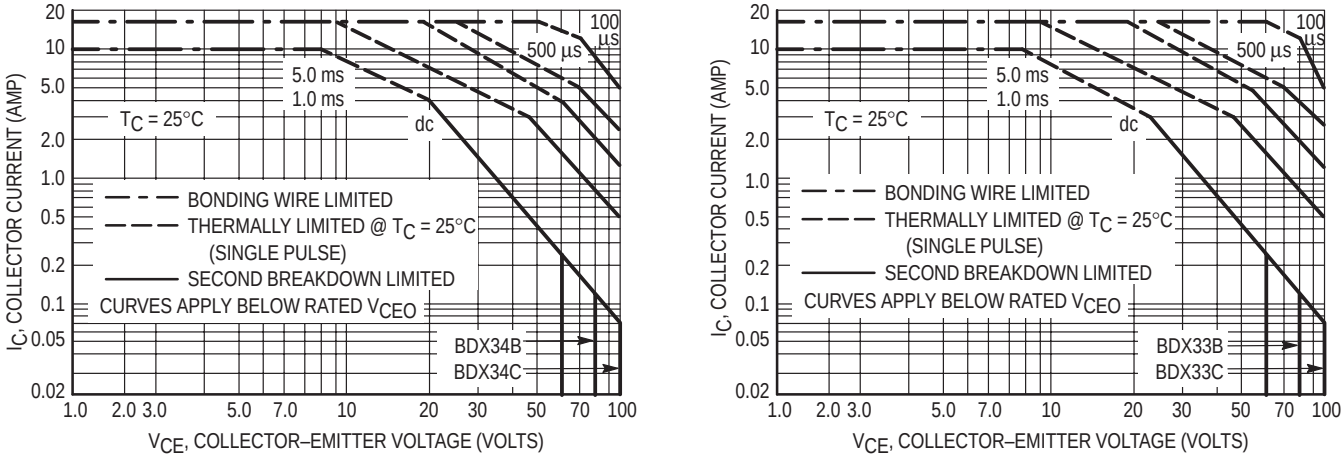


Figure 2. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Fig. 3 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} = 150°C$. $T_{J(pk)}$ may be calculated from the data in Fig. . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

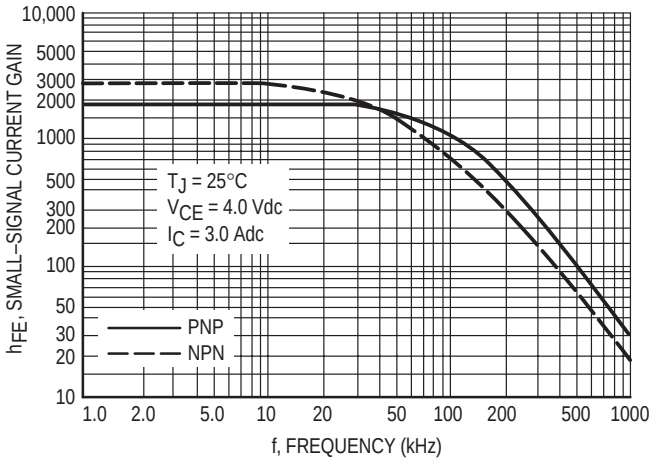


Figure 3. Small–Signal Current Gain

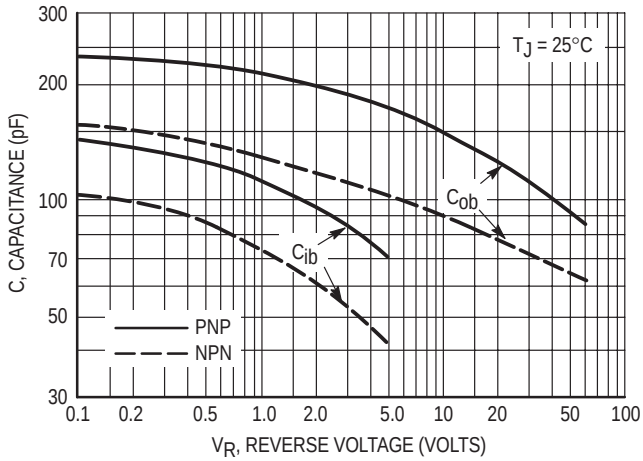
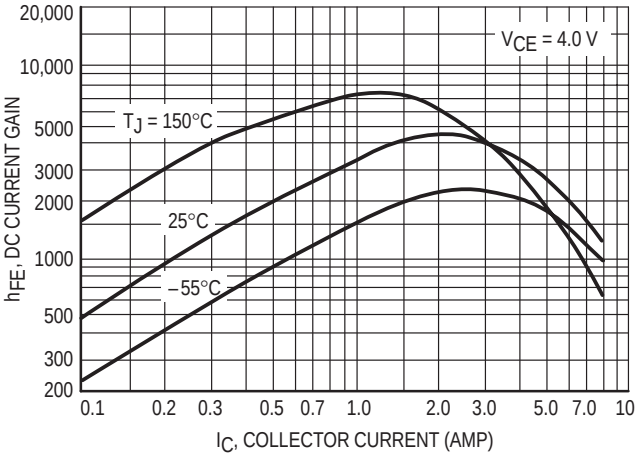


Figure 4. Capacitance

NPN
BDX33B, 33C



PNP
BDX34B, 34C

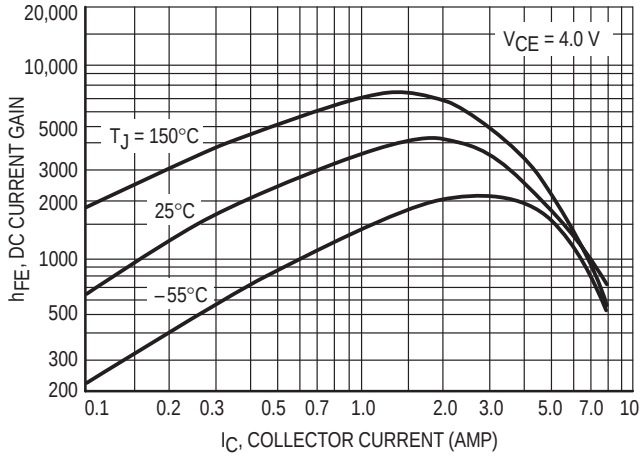
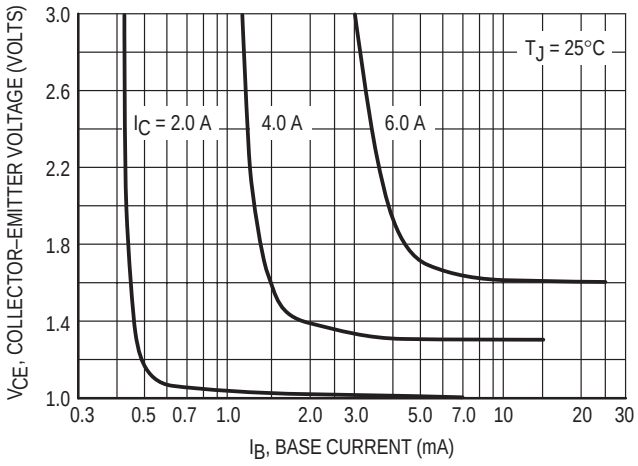


Figure 5. DC Current Gain



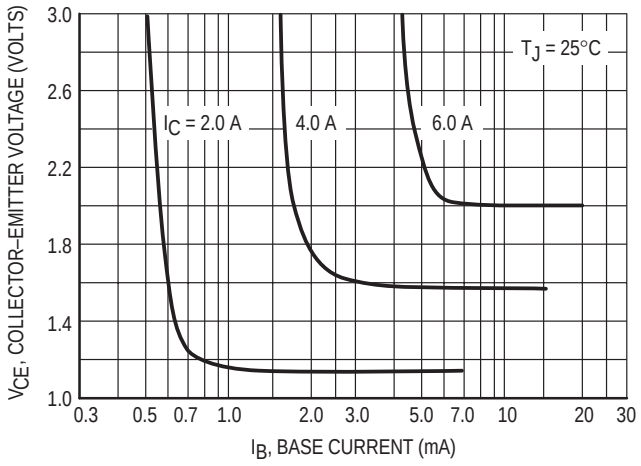
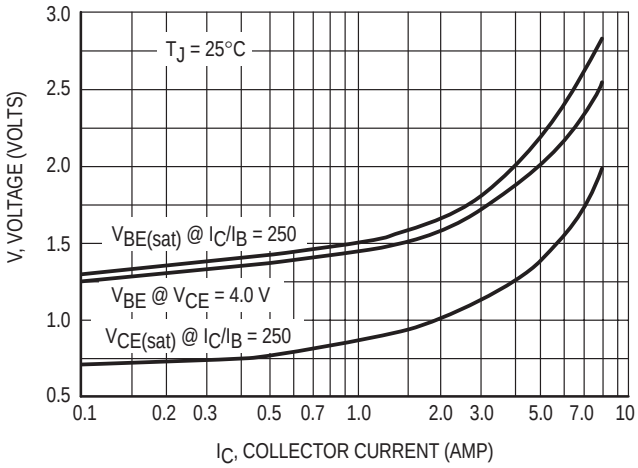


Figure 6. Collector Saturation Region



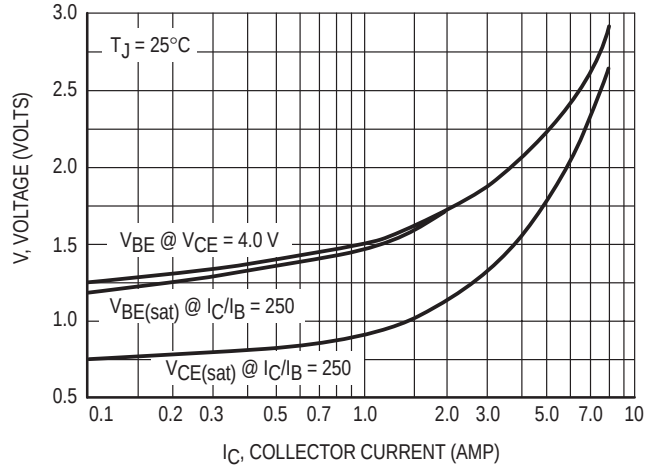


Figure 7. “On” Voltages

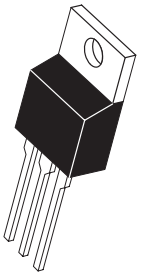
Plastic Medium-Power Complementary Silicon Transistors

. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector Emitter Sustaining Voltage — @ 100 mAdc
  $V_{CEO(sus)}$ = 80 Vdc (Min) — BDX53B, 54B
  = 100 Vdc (Min) — BDX53C, 54C
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors
- TO–220AB Compact Package

NPN
BDX53B
BDX53C
PNP
BDX54B
BDX54C

DARLINGTON
8 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80 – 100 VOLTS
65 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BDX53B BDX54B	BDX53C BDX54C	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	8.0 12		Adc
Base Current	I_B	0.2		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 0.48		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	70	°C/W

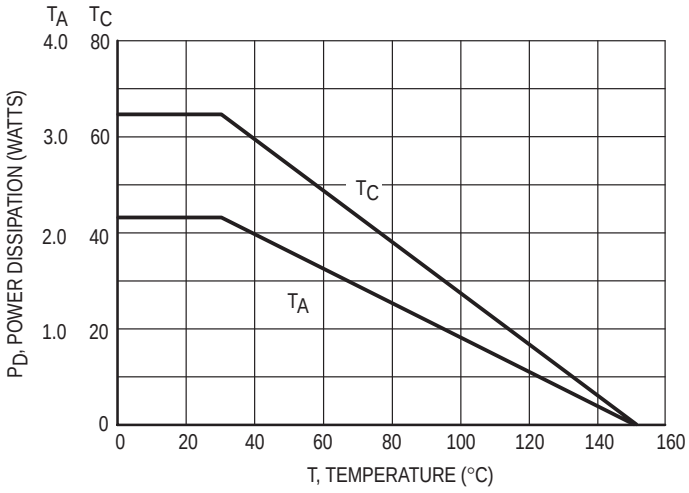


Figure 1. Power Derating

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	BDX53B, BDX54B BDX53C, BDX54C	$V_{CEO(sus)}$	80 100	— —	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	BDX53B, BDX54B BDX53C, BDX54C	I_{CEO}	— —	0.5 0.5	mAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	BDX53B, BDX54B BDX53C, BDX54C	I_{CBO}	— —	0.2 0.2	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	750	—	—
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 12 mAdc)		$V_{CE(sat)}$	— —	2.0 4.0	Vdc
Base–Emitter Saturation Voltage (I_C = 3.0 Adc, I_C = 12 mA)		$V_{BE(sat)}$	—	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		h_{fe}	4.0	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	BDX53B, 53C BDX54B, 54C	C_{ob}	— —	300 200	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

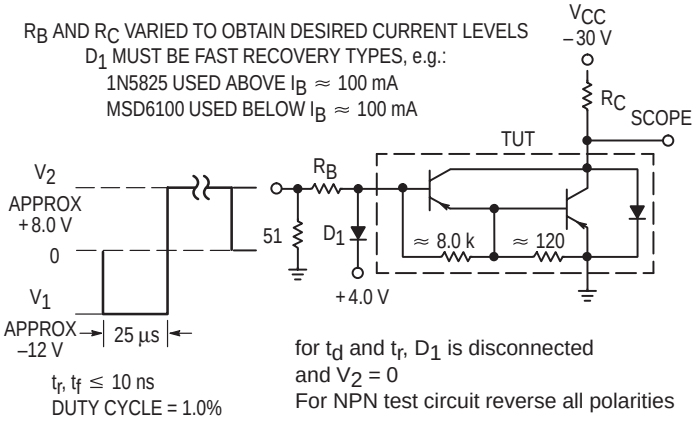


Figure 2. Switching Time Test Circuit

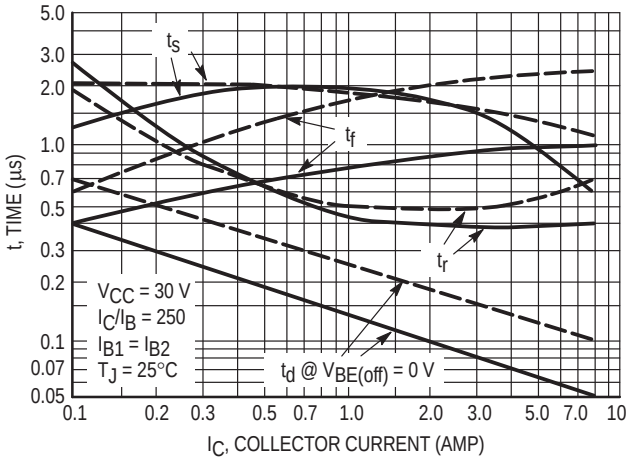


Figure 3. Switching Times

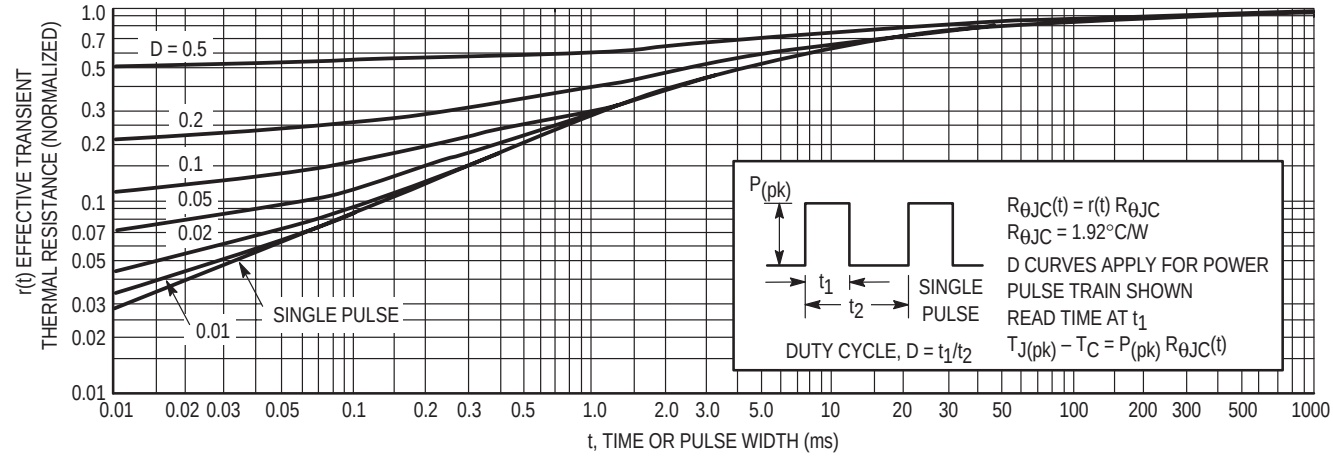


Figure 4. Thermal Response

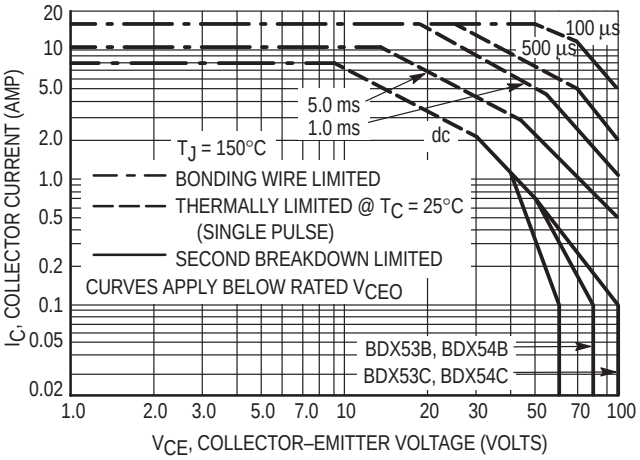


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate I_C –V_{CE} limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

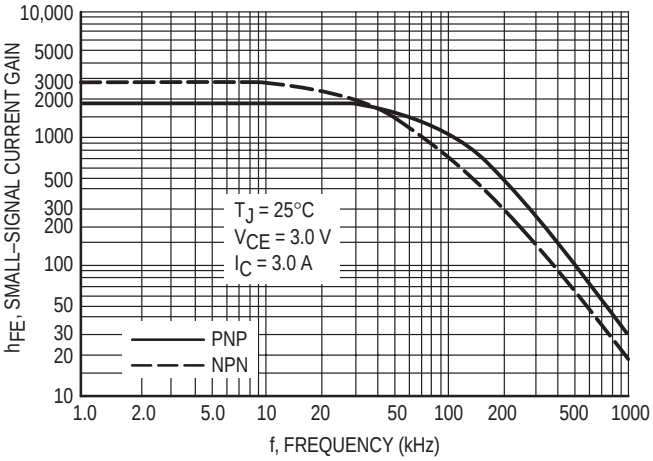


Figure 6. Small-Signal Current Gain

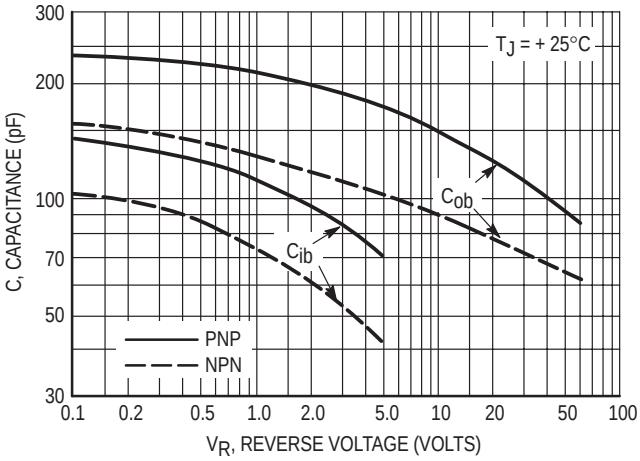
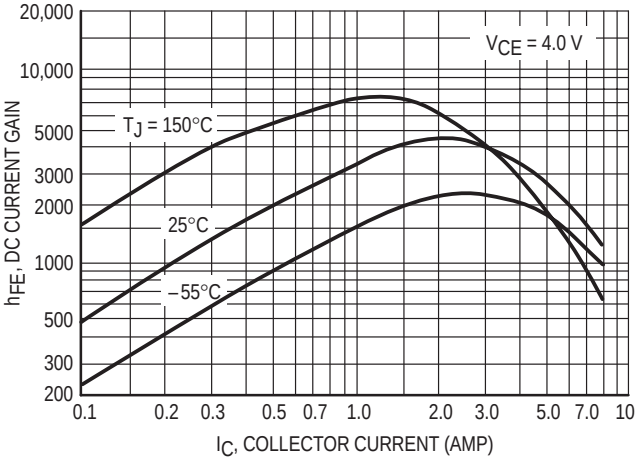


Figure 7. Capacitance

NPN
BDX53B, 53C



PNP
BDX54B, 54C

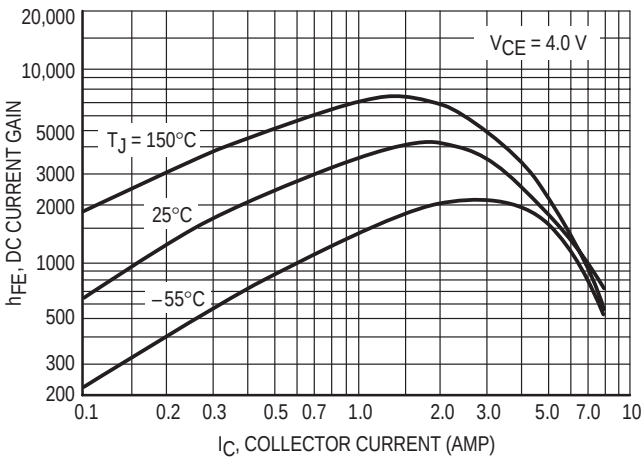
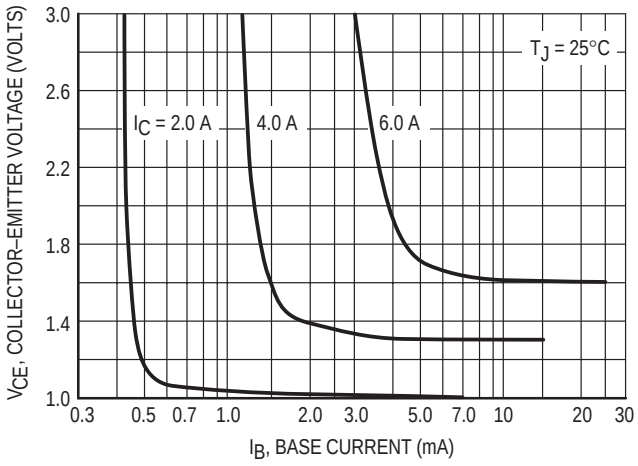


Figure 8. DC Current Gain



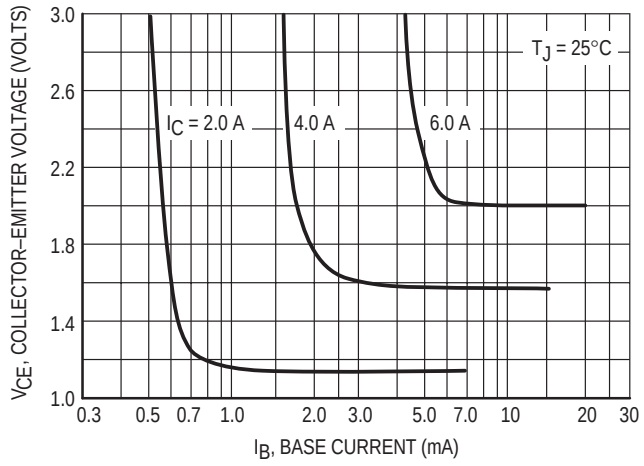
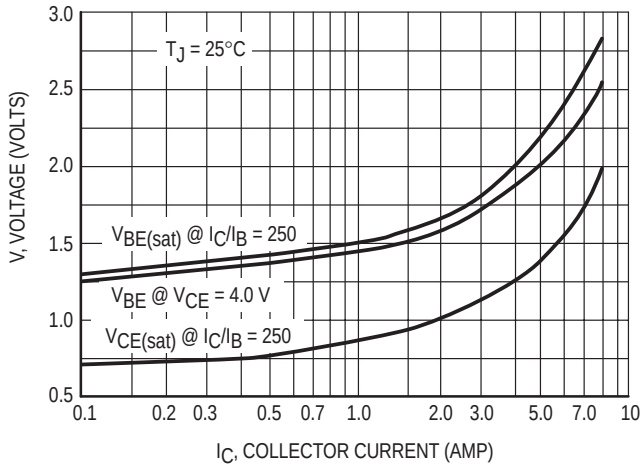


Figure 9. Collector Saturation Region



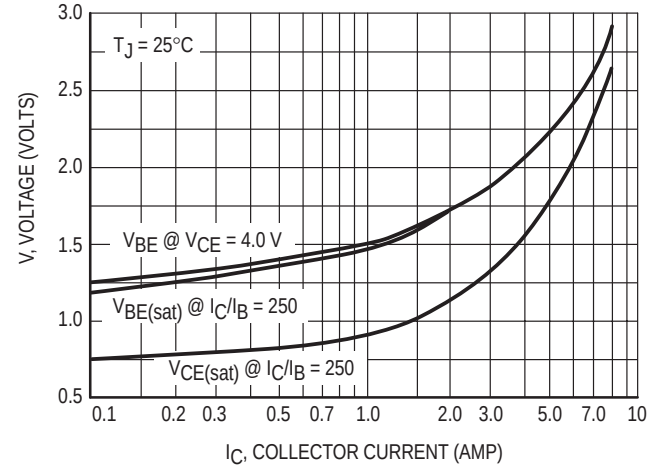


Figure 10. “On” Voltages

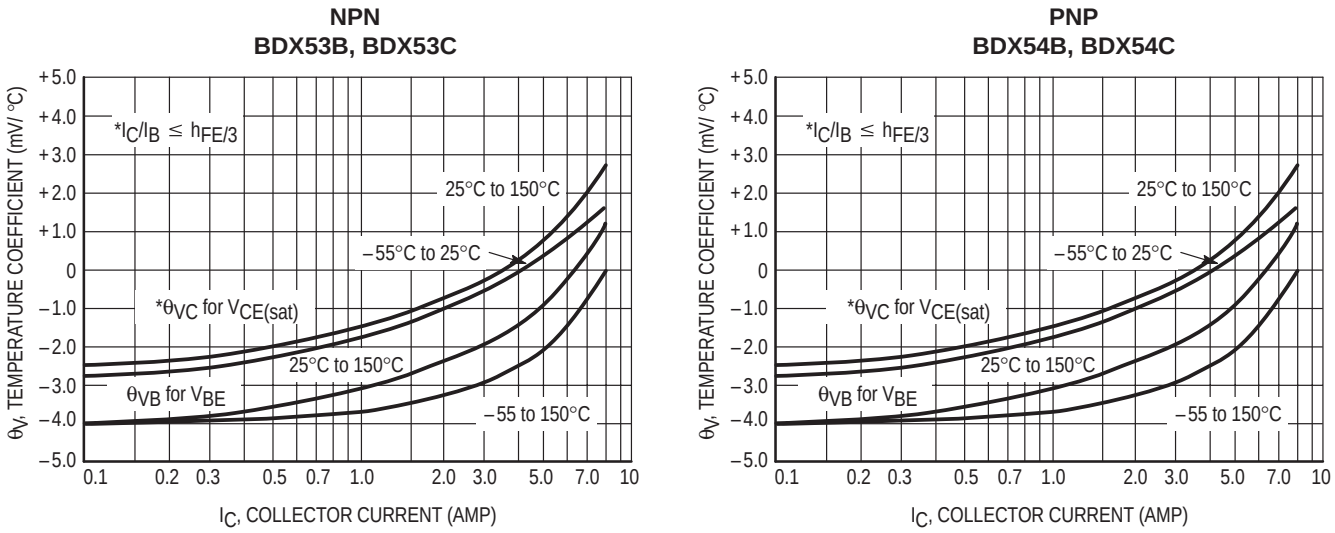


Figure 11. Temperature Coefficients

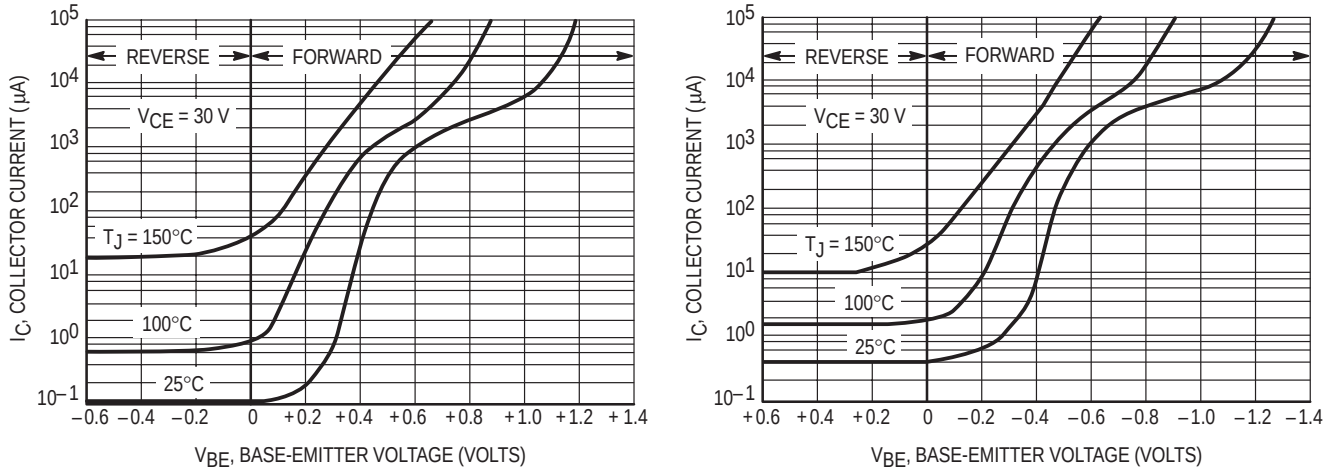


Figure 12. Collector Cut–Off Region

Figure 13. Darlington Schematic

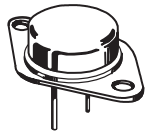
BU208A

Horizontal Deflection Transistor

. . . designed for use in televisions.

- Collector–Emitter Voltages V_{CES} 1500 Volts
- Fast Switching — 400 ns Typical Fall Time
- Low Thermal Resistance 1°C/W Increased Reliability
- Glass Passivated (Patented Photoglass). Triple Diffused Mesa Technology for Long Term Stability

5.0 AMPERES
NPN SILICON
POWER TRANSISTOR
700 VOLTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	BU208A	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	700	Vdc
Collector–Emitter Voltage	V_{CES}	1500	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C I_{CM}	5.0 7.5	Vdc
Base Current — Continuous — Peak (Negative)	I_B I_{BM}	4.0 3.5	Adc
Total Power Dissipation @ T_C = 95°C Derate above 95°C	P_D	12.5 0.625	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +115	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.6	°C/W
Maximum Lead Temperature for Soldering Purpose, 1/8″ from Case for 5 Seconds	T_L	275	°C

NOTES:
1. Pulsed 5.0 ms, Duty Cycle ≤ 10%.
2. See page 3 for Additional Ratings on A Type.
3. Figures in ( ) are Standard Ratings Motorola Guarantees are Superior.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, L = 25 mH)	$V_{CEO(sus)}$	700	—	—	Vdc
Collector Cutoff Current[1] ALL TYPES (V_{CE} = rated V_{CES}, V_{BE} = 0)	I_{CES}	—	—	1.0	mAdc
Emitter Base Voltage[1]	V_{EBO}				Vdc
(I_C = 0, I_E = 10 mAdc)		5	—	—	
(I_C = 0, I_E = 100 mAdc)		—	7	—	
ON CHARACTERISTICS[1]					
DC Current Gain (I_C = 4.5 Adc, V_{CE} = 5 Vdc)	h_{FE}	2.25	—	—	
Collector–Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2 Adc)	$V_{CE(sat)}$	—	—	1	Vdc
Base–Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2 Adc)	$V_{BE(sat)}$	—	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)	f_T	—	4	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	125	—	pF
SWITCHING CHARACTERISTICS					
Storage Time (see test circuit fig. 1) (I_C = 4.5 Adc, I_{B1} = 1.8 Adc, L_B = 10 μH)	t_s	—	8	—	μs
Fall time (see test circuit fig. 1) (I_C = 4.5 Adc, I_{B1} = 1.8 Adc, L_B = 10 μH)	t_f	—	0.4	—	μs

[1]Pulse test: PW = 300 μs; Duty cycle ≤ 2%.

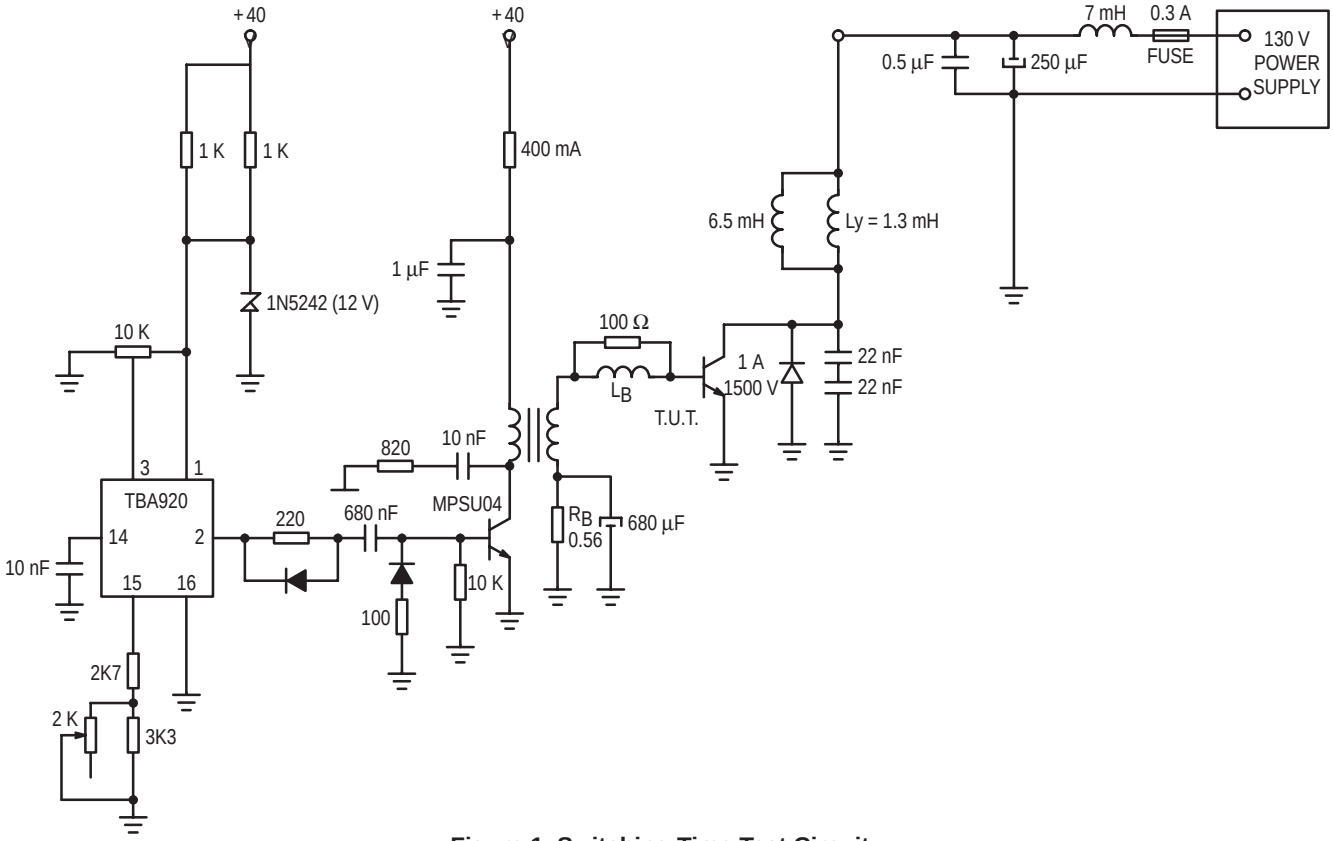


Figure 1. Switching Time Test Circuit

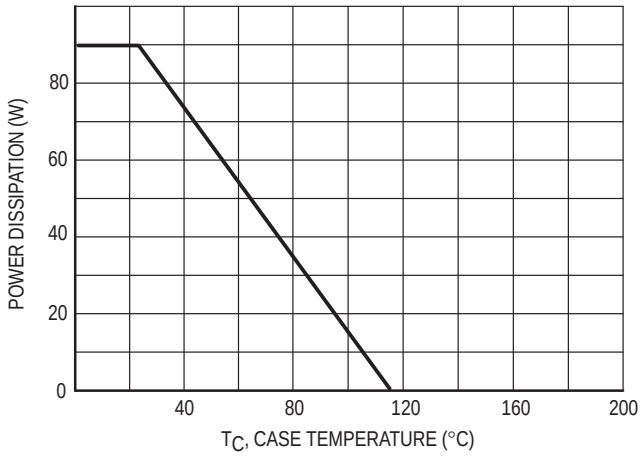


Figure 2. Power Derating

BASE DRIVE
The Key to Performance

By now, the concept of controlling the shape of the turn–off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn–off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst–case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn–off base current will reverse very quickly as shown in Fig. 3. This results in rapid, but only partial collector turn–off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Fig. 4, thus allowing access carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B Is usually done empirically since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B.

This shows the parameter that really matters, dissipation, whether caused by switching or by saturation. For very low L_B a very narrow optimum is obtained. This occurs when I_{B1} $h_{FE} \cong I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the I_{B1}. $h_{FE} = I_{CM}$ point as the turn off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor initiation of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left, or right according to the relation I_{B1} h_{FE} = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Neither L_B nor I_{B1} are absolutely critical. Due to the high gain of Motorola devices it is suggested that in general a low value of I_{B1} be used to obtain optimum efficiency — eg. for BU208A with I_{CM} = 4.5 A use $I_{B1} \approx$ 1.5 A, at I_{CM} = 4 A use $I_{B1} \approx$ 1.2 A. These values are lower than for most competition devices but practical tests have showed comparable efficiency for Motorola devices even at the higher level of I_{B1}.

An L_B of 10 μH to 12 μH should give satisfactory operation of BU208A with I_{CM} of 4 to 4.5 A and I_{B1} between 1.2 and 2 A.

TEST CIRCUIT WAVEFORMS

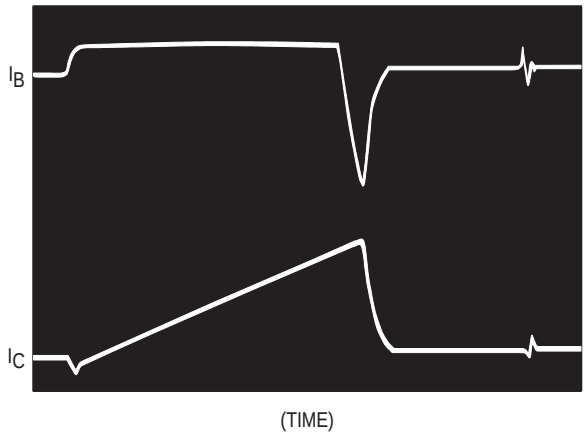


Figure 3

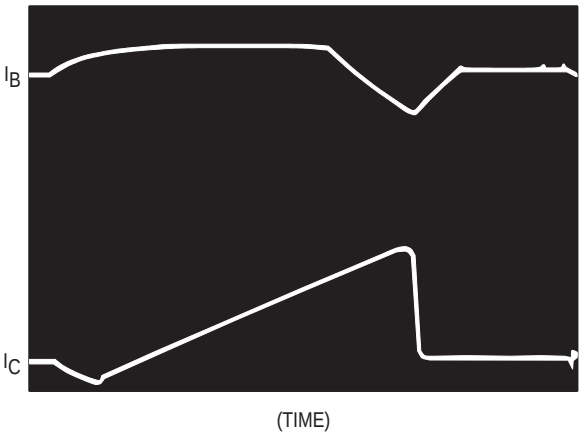


Figure 4

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance. Once the required transistor operating current is determined, fixed circuit values may be selected.

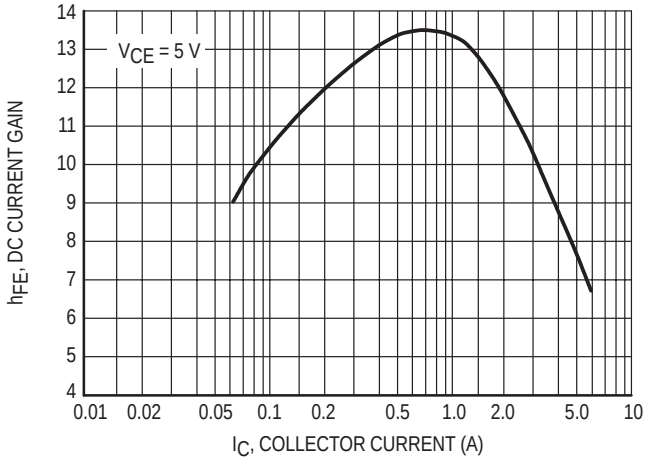


Figure 5. DC Current Gain

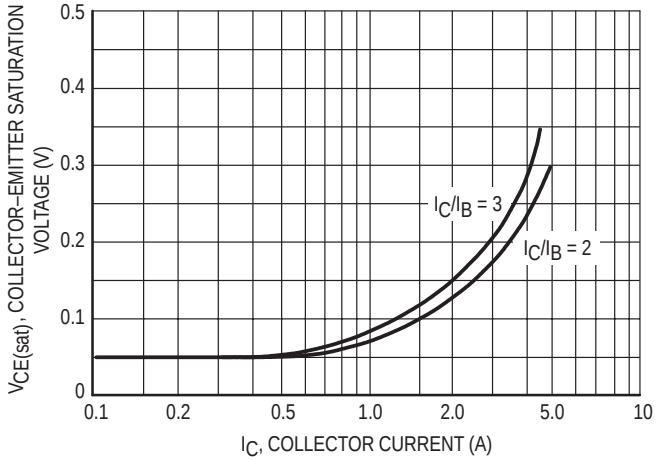


Figure 6. Collector–Emitter Saturation Voltage

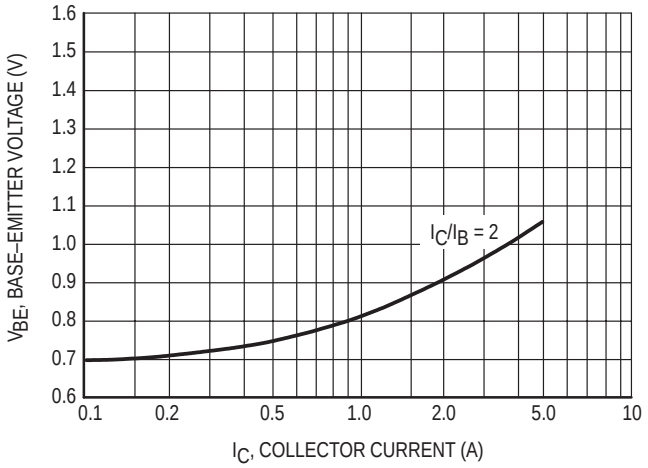


Figure 7. Base–Emitter Saturation Voltage

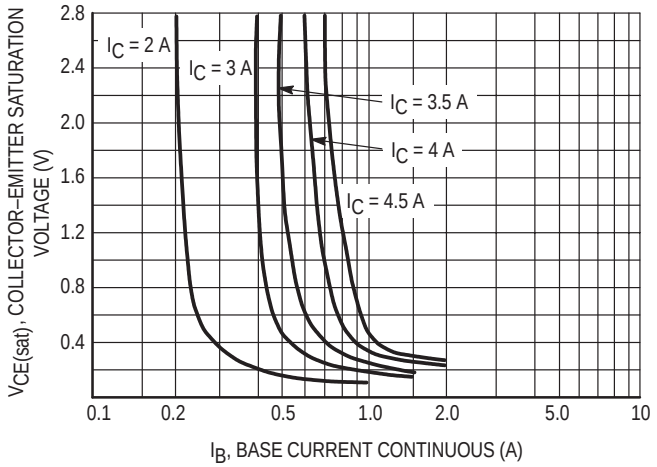


Figure 8. Collector Saturation Region

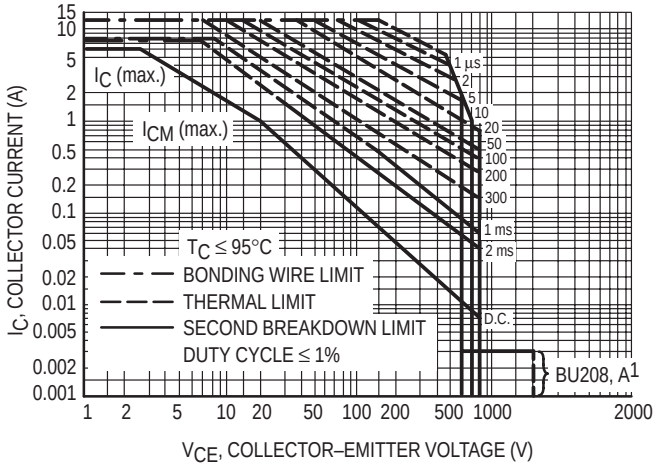


Figure 9. Maximum Forward Bias Safe Operating Area

[1]Pulse width ≤ 20 µs. Duty cycle ≤ 0.25. R_{BE} ≤ 100 Ohms.

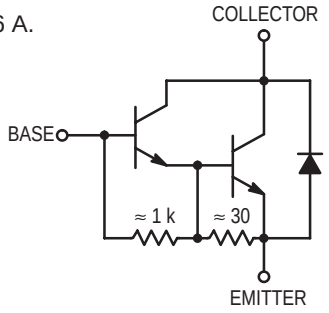
BU323A

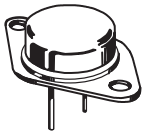
NPN Silicon Power Darlington Transistor

16 AMPERE PEAK POWER TRANSISTOR DARLINGTON NPN SILICON 400 VOLTS 175 WATTS

The BU323A is a monolithic darlington transistor designed for automotive ignition, switching regulator and motor control applications.

- V_{CE} Sat Specified at –40°C = 2.0 V Max. at I_C = 6 A.
- Photoglass Passivation for Reliability and Stability.





CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector–Base Voltage	V_{CBO}	600	Vdc
Emitter–Base Voltage	V_{EBO}	8.0	Vdc
Collector Current — Continuous Peak (1)	I_C	10 16	Adc
Base Current — Continuous	I_B	3.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1.0	Watts Watts W/°C
Operating and Storage Junction	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS[1]					
Collector–Emitter Sustaining Voltage (Figure 1) L = 10 mH (I_C = 200 mAdc, I_B = 0, V_{clamp} = Rated V_{CEO})	$V_{CEO(sus)}$	400			Vdc
Collector–Emitter sustaining Voltage (Figure 1) (I_C = 3 A, R_{BE} = 100 Ohms, L = 500 μH) Unclamped	$V_{CER(sus)}$	475			Vdc
Collector Cutoff Current (Rated V_{CER}, R_{BE} = 100 Ohms)	I_{CER}			1	mAdc
Collector Cutoff Current (Rated V_{CBO}, I_E = 0)	I_{CBO}			1	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)	I_{EBO}			40	mAdc
ON CHARACTERISTICS[1]					
DC Current Gain (I_C = 3 Adc, V_{CE} = 6 Vdc) (I_C = 6 Adc, V_{CE} = 6 Vdc) (I_C = 10 Adc, V_{CE} = 6 Vdc)	h_{FE}	300 150 50	550 350 150	2000	
Collector–Emitter Saturation Voltage (I_C = 3 Adc, I_B = 60 mAdc) (I_C = 6 Adc, I_B = 120 mAdc) (I_C = 10 Adc, I_B = 300 mAdc) (I_C = 6 Adc, I_B = 120 mAdc, T_C = –40°C)	$V_{CE(sat)}$			1.5 1.7 2.7 2.0	Vdc
Base–Emitter Saturation Voltage (I_C = 6 Adc, I_B = 120 mAdc) (I_C = 10 Adc, I_B = 300 mAdc) (I_C = 6 Adc, I_B = 120 mAdc, T_C = –40°C)	$V_{BE(sat)}$			2.2 3 2.4	Vdc
Base–Emitter On Voltage (I_C = 10 Adc, V_{CE} = 6 Vdc)	$V_{BE(on)}$			2.5	Vdc
Diode Forward Voltage (I_F = 10 Adc)	V_f		2	3.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}		165	350	pF
SWITCHING CHARACTERISTICS					
Storage Time	(V_{CC} – 12 Vdc, I_C = 6 Adc, I_{B1} = I_{B2} = 0.3 Adc) Fig. 2	t_s		7.5	15	μs
Fall Time		t_f		5.2	15	μs
FUNCTIONAL TESTS					
Second Breakdown Collector Current with Base–Forward Biased	$I_{S/B}$		See Figure10		
Pulsed Energy Test (See Figure 12)	$I_C^2L/2$	550			mJ

1 Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

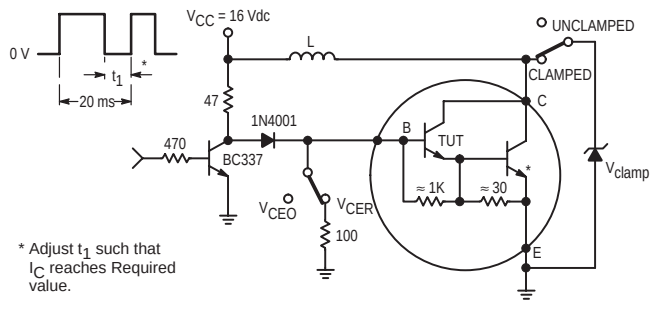


Figure 1. Sustaining Voltage Test Circuit

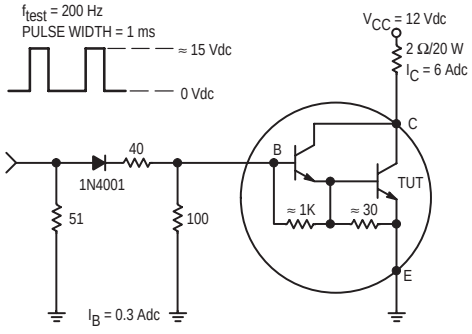


Figure 2. Switching Times Test Circuit

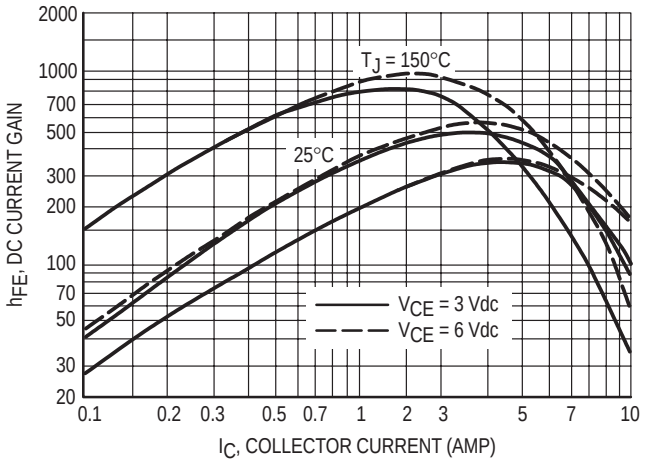


Figure 3. DC Current Gain

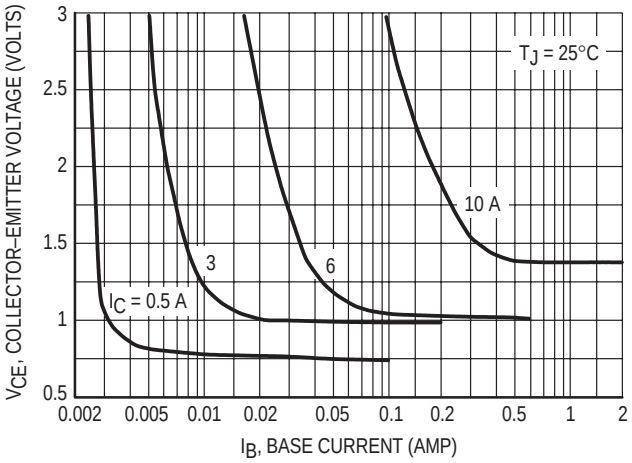


Figure 4. Collector Saturation Region

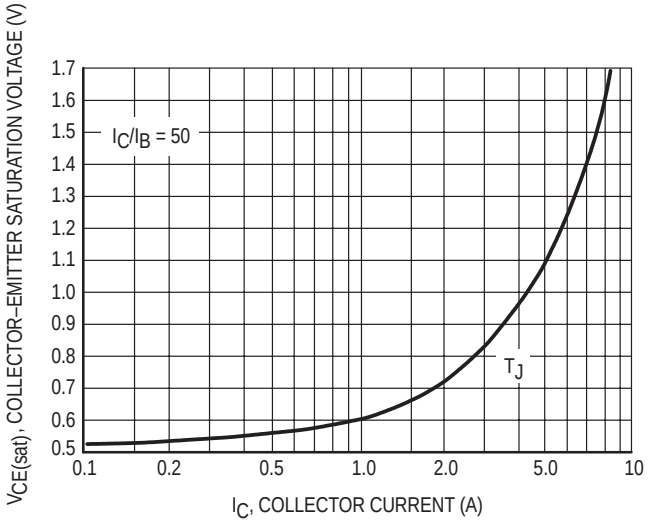


Figure 5. Collector–Emitter Saturation Voltage

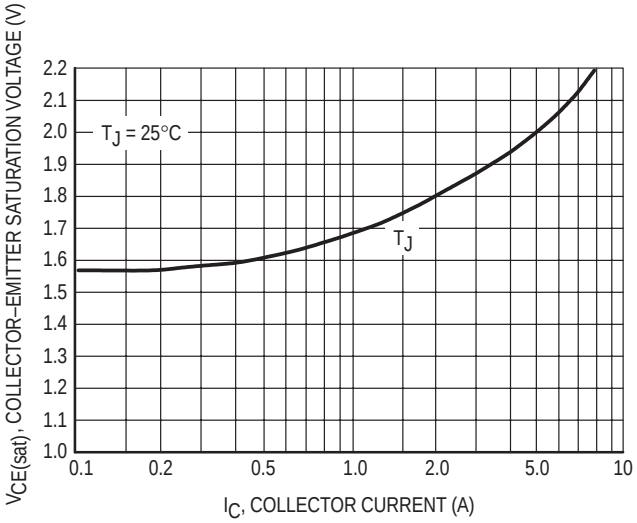


Figure 6. Base–Emitter Voltage

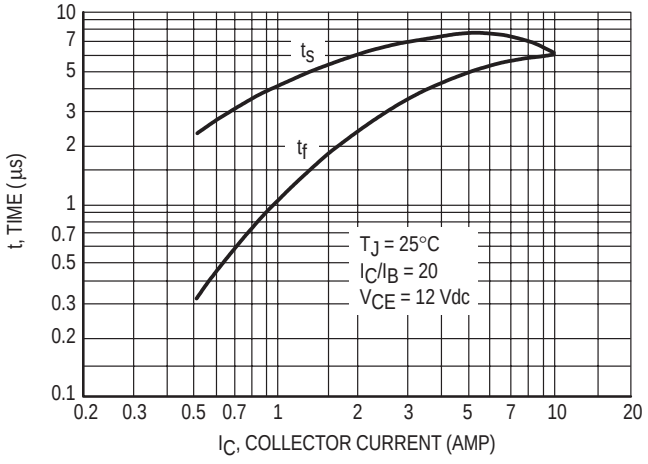


Figure 7. Turn–Off Switching Time

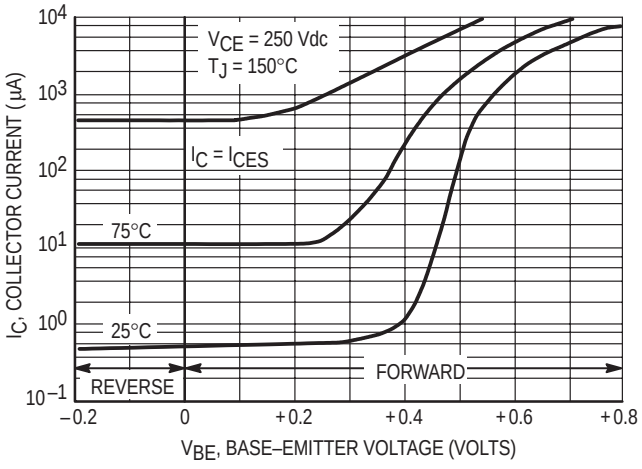


Figure 8. Collector Cutoff Region

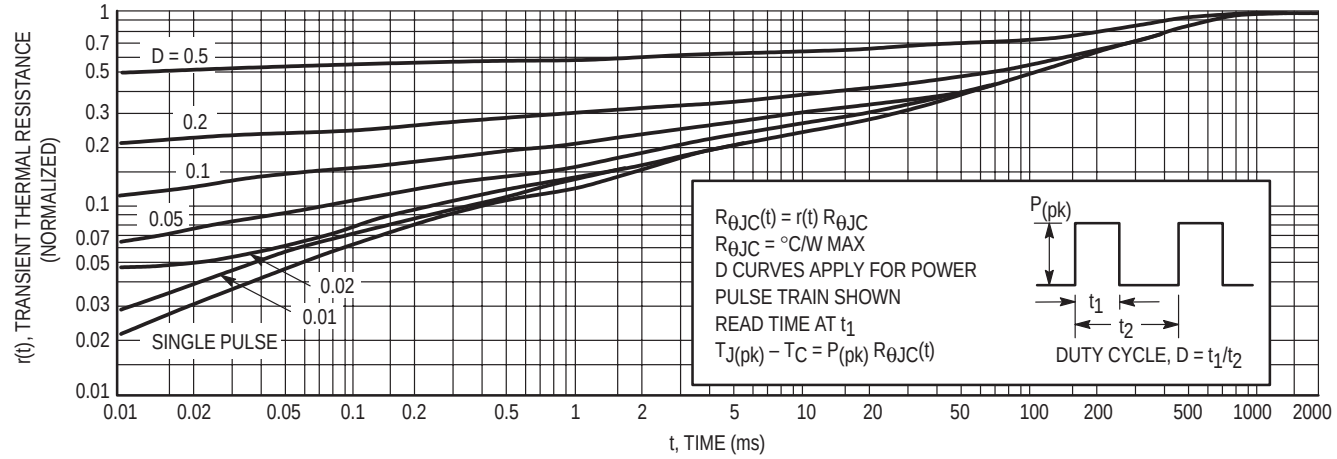


Figure 9. Thermal Response

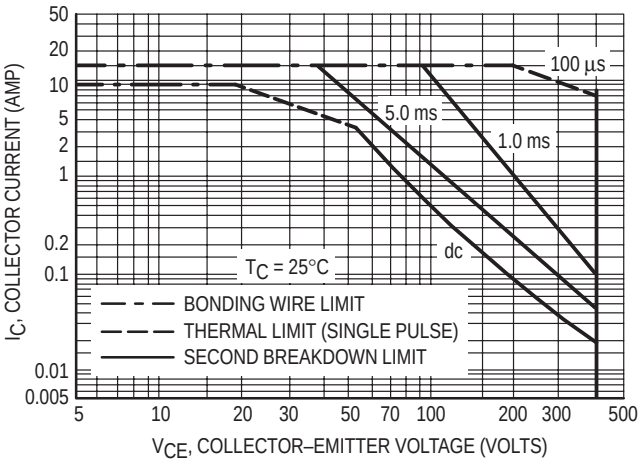


Figure 10. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

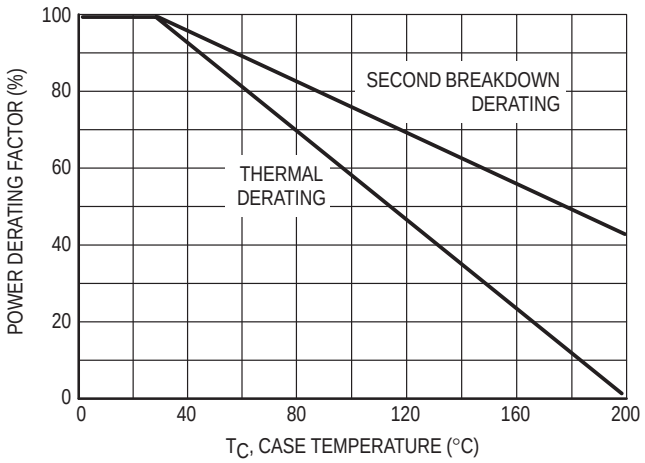
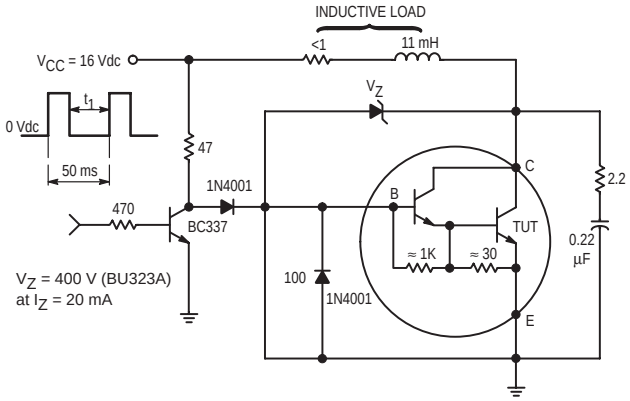


Figure 11. Power Derating



t_1 to be selected such that I_C reaches 10 Adc before switch–off.

NOTE: Figure 12 specifies energy handling capabilities in an automotive ignition circuit.

Figure 12. Ignition Test Circuit

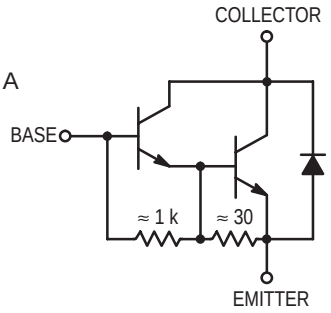
BU323AP

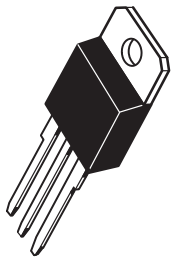
NPN Silicon Darlington Power Transistor

DARLINGTON
NPN SILICON
POWER TRANSISTOR
400 VOLTS
125 WATTS

The BU323AP is a monolithic darlington transistor designed for automotive ignition, switching regulator and motor control applications.

- Collector–Emitter Sustaining Voltage — $V_{CER(sus)}$ = 475 Vdc
- 125 Watts Capability at 50 Volts
- V_{CE} Sat Specified at –40°C = 2.0 V Max. at I_C = 6.0 A
- Photoglass Passivation for Reliability and Stability





CASE 340D–01
TO–218 TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector–Emitter Voltage	V_{CEV}	475	Vdc
Emitter–Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 16	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	3.0	Adc
Total Power Dissipation — T_C = 25°C — T_C = 100°C Derate above 25°C	P_D	125 100 1.0	Watts Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≦ 10%.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS[1]					
Collector–Emitter Sustaining Voltage (Figure 1) L = 10 mH (I_C = 200 mAdc, I_B = 0, V_{clamp} = Rated V_{CEO})	$V_{CEO(sus)}$	400			Vdc
Collector–Emitter Sustaining Voltage (Figure 1) (I_C = 3 A, R_{BE} = 100 Ohms, L = 500 μH) Unclamped	$V_{CER(sus)}$	475			Vdc
Collector Cutoff Current (Rated V_{CER}, R_{BE} = 100 Ohms)	I_{CER}			1	mAdc
Collector Cutoff Current (Rated V_{CBO}, I_E = 0)	I_{CBO}			1	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)	I_{EBO}			40	mAdc
ON CHARACTERISTICS[1]					
DC Current Gain (I_C = 3 Adc, V_{CE} = 6 Vdc) (I_C = 6 Adc, V_{CE} = 6 Vdc) (I_C = 10 Adc, V_{CE} = 6 Vdc)	h_{FE}	300 150 50	550 350 150	2000	
Collector–Emitter Saturation Voltage (I_C = 3 Adc, I_B = 60 mAdc) (I_C = 6 Adc, I_B = 120 mAdc) (I_C = 10 Adc, I_B = 300 mAdc (I_C = 6 Adc, I_B = 120 mAdc, T_C = –40°C)	$V_{CE(sat)}$			1.5 1.7 2.7 2.0	Vdc
Base–Emitter Saturation Voltage (I_C = 6 Adc, I_B = 120 mAdc) (I_C = 10 Adc, I_B = 300 mAdc) (I_C = 6 Adc, I_B = 120 mAdc, T_C = –40°C)	$V_{BE(sat)}$			2.2 3 2.4	Vdc
Base–Emitter On Voltage (I_C = 10 Adc, V_{CE} = 6 Vdc)	$V_{BE(on)}$			2.5	Vdc
Diode Forward Voltage (I_F = 10 Adc)	V_f		2	3.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}		165	350	pF
SWITCHING CHARACTERISTICS					
Storage Time	(V_{CC} = 12 Vdc, I_C = 6 Adc, I_{B1} = I_{B2} = 0.3 Adc) Fig. 2	t_s		7.5	15	μs
Fall Time		t_f		5.2	15	μs
FUNCTIONAL TESTS					
Second Breakdown Collector Current with Base–Forward Biased	$I_{S/B}$		See Figure 10		
Pulsed Energy Test (See Figure 12)	$I_C^2L/2$	550			mJ

[1]Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

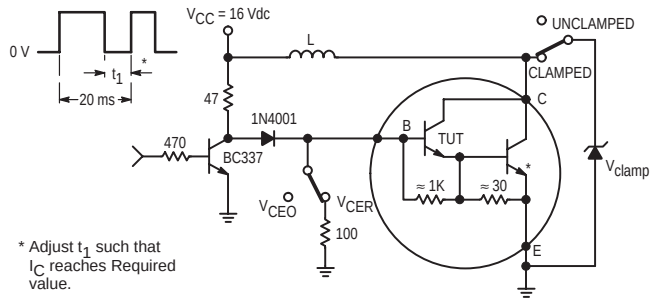


Figure 1. Sustaining Voltage Test Circuit

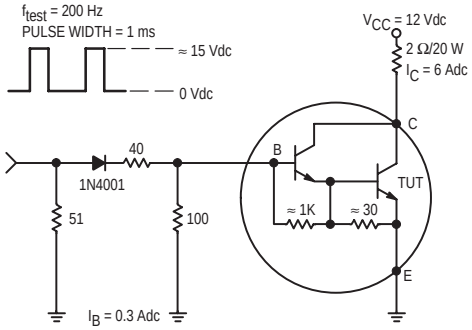


Figure 2. Switching Times Test Circuit

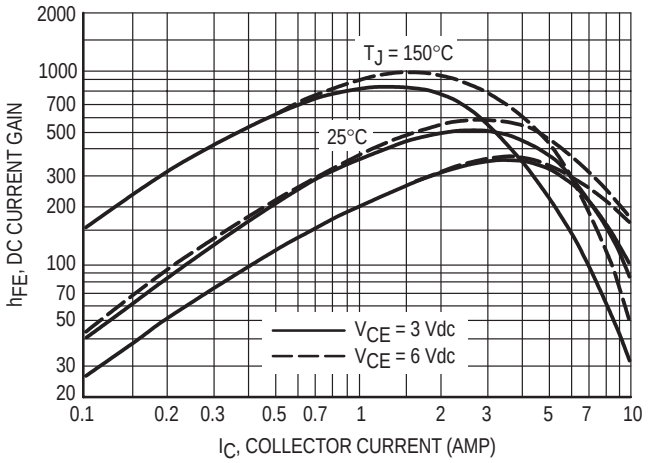


Figure 3. DC Current Gain

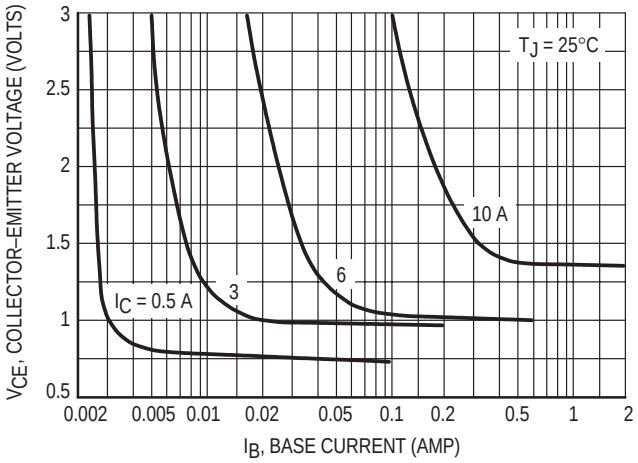


Figure 4. Collector Saturation Region

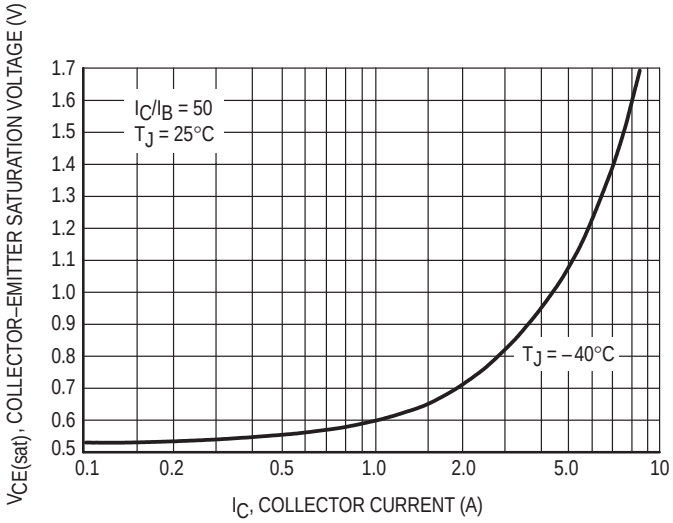


Figure 5. Collector–Emitter Saturation Voltage

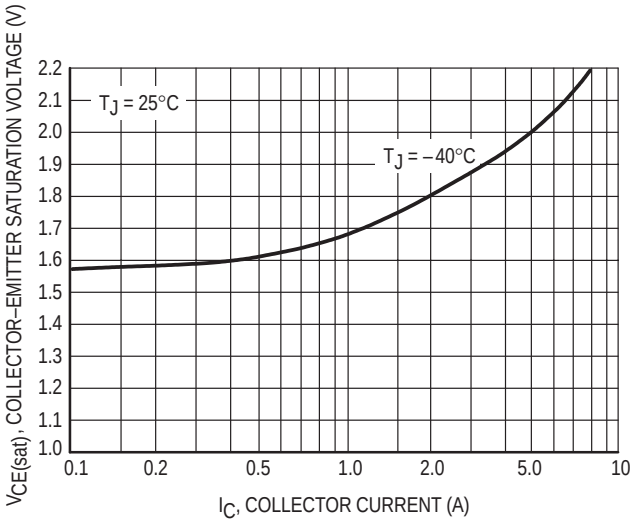


Figure 6. Base–Emitter Voltage

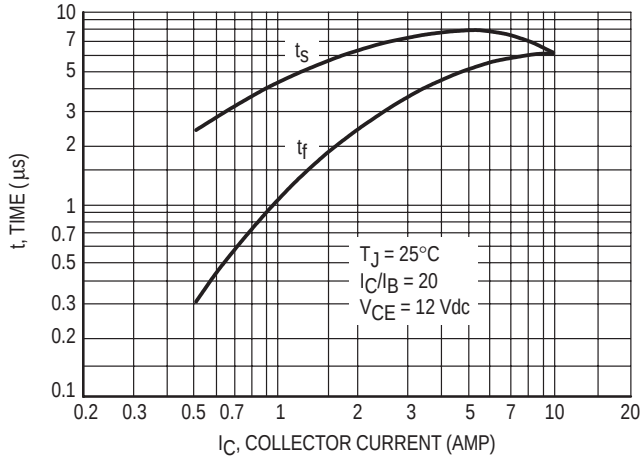


Figure 7. Turn–Off Switching Time

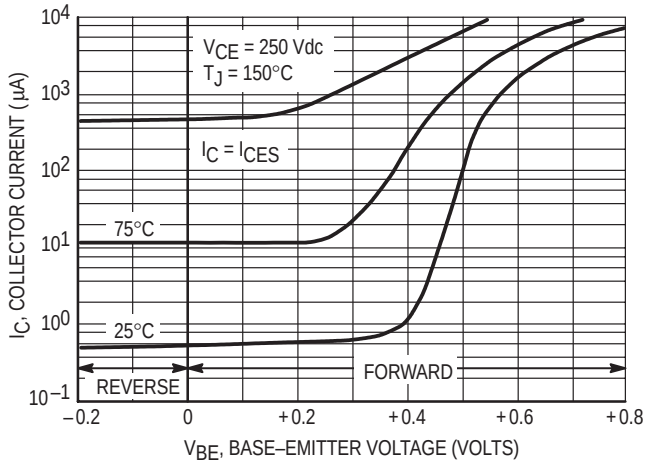


Figure 8. Collector Cutoff Region

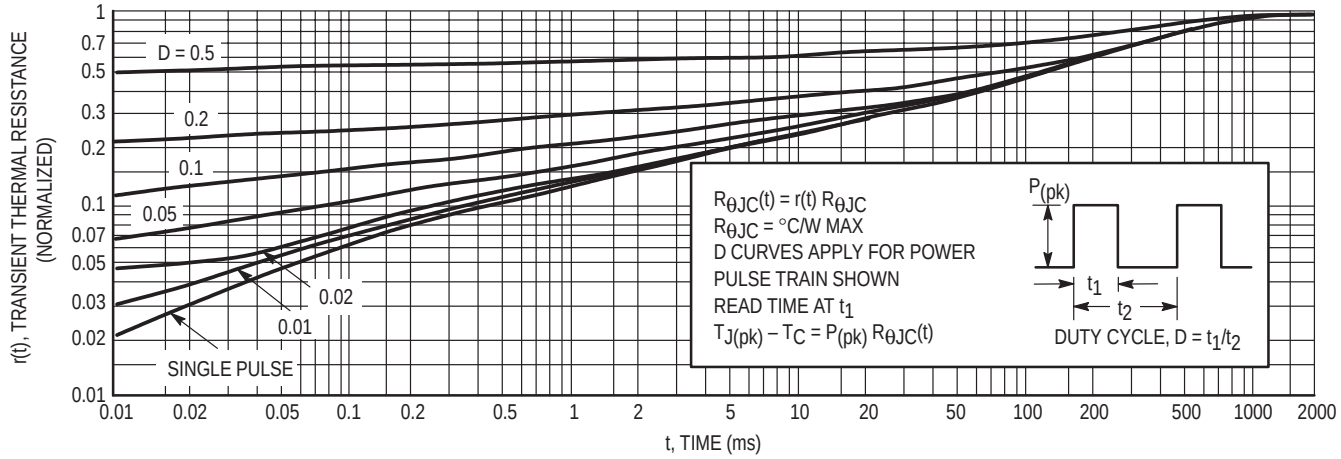


Figure 9. Thermal Response

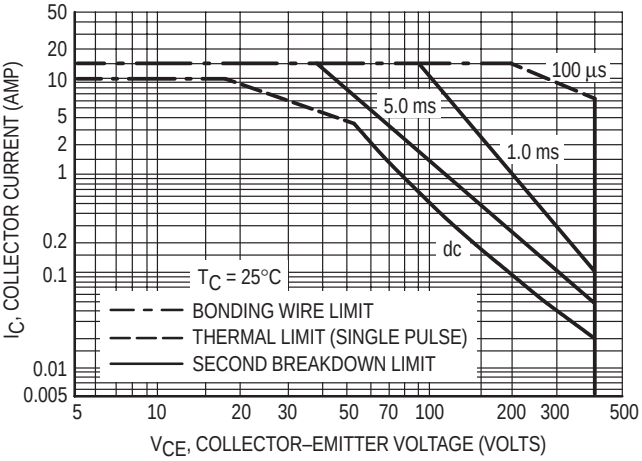


Figure 10. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

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$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

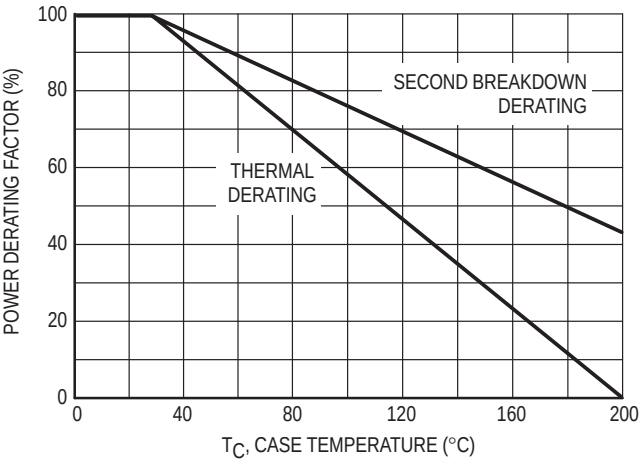
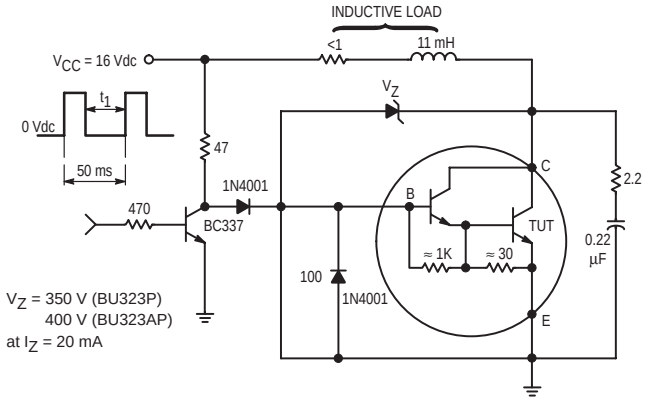


Figure 11. Power Derating



t_1 to be selected such that I_C reaches 10 Adc before switch–off.

NOTE: Figure 12 specifies energy handling capabilities in an automotive ignition circuit.

Figure 12. Ignition Test Circuit

BU323Z

Advance Information

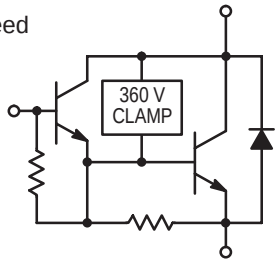
NPN Silicon Power Darlington

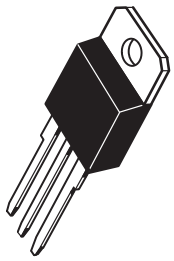
High Voltage Autoprotected

AUTOPROTECTED DARLINGTON
10 AMPERES
360 – 450 VOLTS CLAMP
150 WATTS

The BU323Z is a planar, monolithic, high–voltage power Darlington with a built–in active zener clamping circuit. This device is specifically designed for unclamped, inductive applications such as Electronic Ignition, Switching Regulators and Motor Control, and exhibit the following main features:

- Integrated High–Voltage Active Clamp
- Tight Clamping Voltage Window (350 V to 450 V) Guaranteed Over the –40°C to +125°C Temperature Range
- Clamping Energy Capability 100% Tested in a Live Ignition Circuit
- High DC Current Gain/Low Saturation Voltages Specified Over Full Temperature Range
- Design Guarantees Operation in SOA at All Times
- Offered in Plastic SOT–93/TO–218 Type or TO–220 Packages





CASE 340D–01
SOT–93/TO–218 TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	350	Vdc
Collector–Emitter Voltage	V_{EBO}	6.0	Vdc
Collector Current — Continuous — Peak	I_C I_{CM}	10 20	Adc
Base Current — Continuous — Peak	I_B I_{BM}	3.0 6.0	Adc
Total Power Dissipation (T_C = 25°C) Derate above 25°C	P_D	150 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +175	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector–Emitter Clamping Voltage (I_C = 7.0 A) (T_C = –40°C to +125°C)	V_{CLAMP}	350	—	450	Vdc
Collector–Emitter Cutoff Current (V_{CE} = 200 V, I_B = 0)	I_{CEO}	—	—	100	μAdc
Emitter–Base Leakage Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	50	mAdc
ON CHARACTERISTICS (1)					
Base–Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 8.0 Adc, I_B = 100 mAdc)		—	—	2.2	
(I_C = 10 Adc, I_B = 0.25 Adc)		—	—	2.5	
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 7.0 Adc, I_B = 70 mAdc)		—	—	1.6	
(T_C = 125°C)		—	—	1.8	
(I_C = 8.0 Adc, I_B = 0.1 Adc)		—	—	1.8	
(T_C = 125°C)		—	—	2.1	
(I_C = 10 Adc, I_B = 0.25 Adc)		—	—	1.7	
Base–Emitter On Voltage	$V_{BE(on)}$				Vdc
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc) (T_C = –40°C to +125°C)		1.1	—	2.1	
(I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)		1.3	—	2.3	
Diode Forward Voltage Drop (I_F = 10 Adc)	V_F	—	—	2.5	Vdc
DC Current Gain	h_{FE}				—
(I_C = 6.5 Adc, V_{CE} = 1.5 Vdc) (T_C = –40°C to +125°C)		150	—	—	
(I_C = 5.0 Adc, V_{CE} = 4.6 Vdc)		500	—	3400	
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	—	—	2.0	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	—	200	pF
Input Capacitance (V_{EB} = 6.0 V)	C_{ib}	—	—	550	pF
CLAMPING ENERGY (see notes)					
Repetitive Non–Destructive Energy Dissipated at turn–off: (I_C = 7.0 A, L = 8.0 mH, R_{BE} = 100 Ω) (see Figures 2 and 4)	W_{CLAMP}	200	—	—	mJ

SWITCHING CHARACTERISTICS: Inductive Load (L = 10 mH)

Fall Time	(I_C = 6.5 A, I_{B1} = 45 mA, $V_{BE(off)}$ = 0, $R_{BE(off)}$ = 0, V_{CC} = 14 V, V_Z = 300 V)	t_{fi}	—	625	—	ns
Storage Time		t_{si}	—	10	30	μs
Cross–over Time		t_c	—	1.7	—	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%.

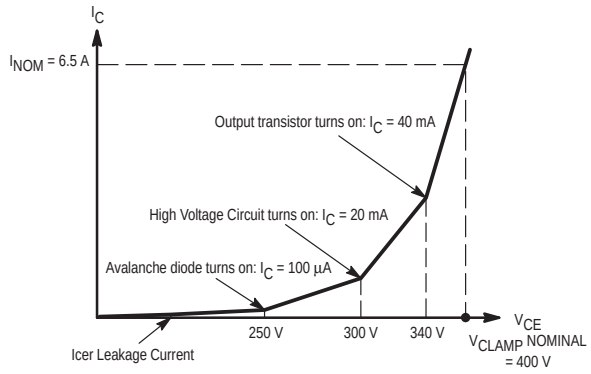


Figure 1. $I_C = f(V_{CE})$ Curve Shape

By design, the BU323Z has a built–in avalanche diode and a special high voltage driving circuit. During an auto–protect cycle, the transistor is turned on again as soon as a voltage, determined by the zener threshold and the network, is reached. This prevents the transistor from going into a Reverse Bias Operating limit condition. Therefore, the device will have an extended safe operating area and will always appear to be in “FBSOA.” Because of the built–in zener and associated network, the $I_C = f(V_{CE})$ curve exhibits an unfamiliar shape compared to standard products as shown in Figure 1.

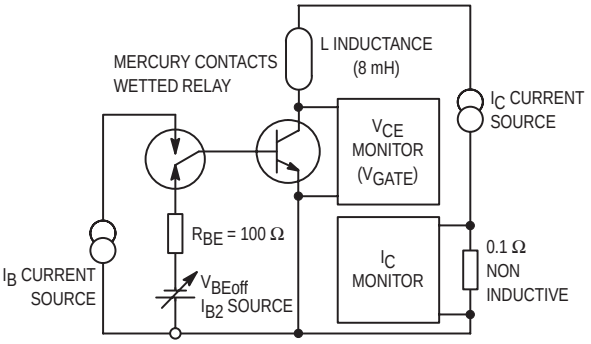


Figure 2. Basic Energy Test Circuit

The bias parameters, V_{CLAMP}, I_{B1}, $V_{BE(off)}$, I_{B2}, I_C, and the inductance, are applied according to the Device Under Test (DUT) specifications. V_{CE} and I_C are monitored by the test system while making sure the load line remains within the limits as described in Figure 4.

Note: All BU323Z ignition devices are 100% energy tested, per the test circuit and criteria described in Figures 2 and 4, to the minimum guaranteed repetitive energy, as specified in the device parameter section. The device can sustain this energy on a repetitive basis without degrading any of the specified electrical characteristics of the devices. The units under test are kept functional during the complete test sequence for the test conditions described:
$I_{C(peak)}$ = 7.0 A, I_CH = 5.0 A, I_CL = 100 mA, I_B = 100 mA, R_{BE} = 100 Ω, V_{gate} = 280 V, L = 8.0 mH

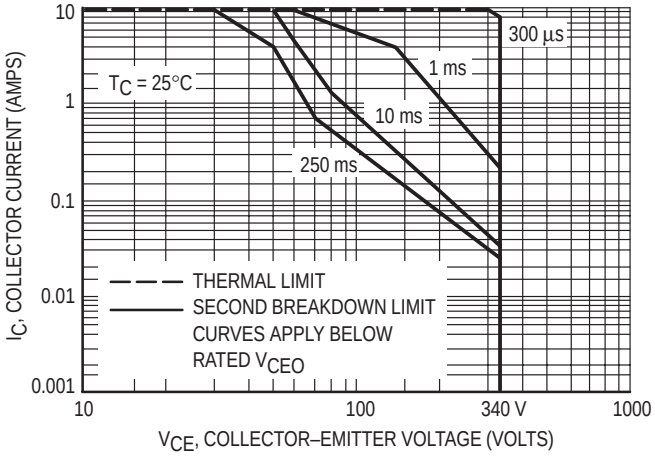


Figure 3. Forward Bias Safe Operating Area

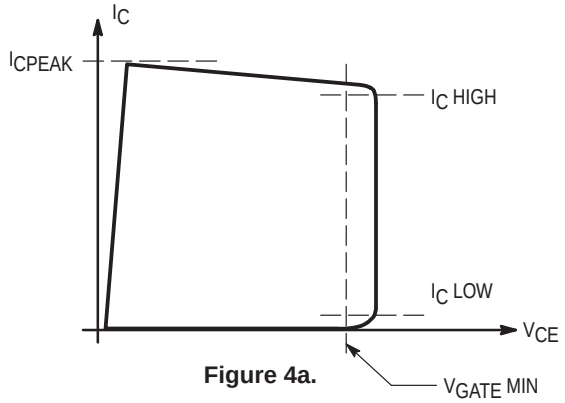


Figure 4a.

The shaded area represents the amount of energy the device can sustain, under given DC biases ($I_C/I_B/V_{BE(off)}/R_{BE}$), without an external clamp; see the test schematic diagram, Figure 2.

The transistor PASSES the Energy test if, for the inductive load and $I_{CPEAK}/I_B/V_{BE(off)}$ biases, the V_{CE} remains outside the shaded area and greater than the V_{GATE} minimum limit, Figure 4a.

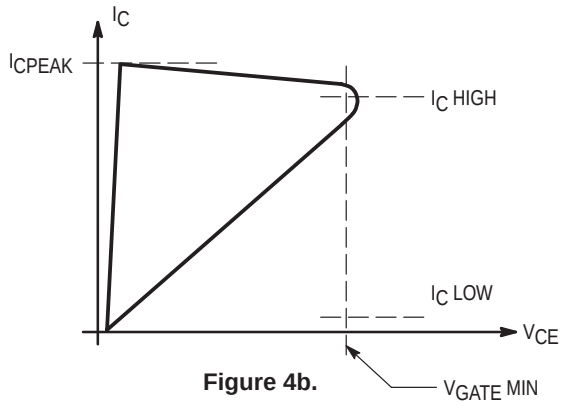


Figure 4b.

The transistor FAILS if the V_{CE} is less than the V_{GATE} (minimum limit) at any point along the V_{CE}/I_C curve as shown on Figures 4b, and 4c. This assures that hot spots and uncontrolled avalanche are not being generated in the die, and the transistor is not damaged, thus enabling the sustained energy level required.

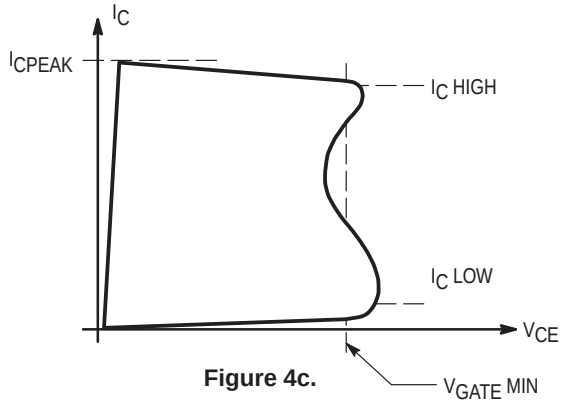


Figure 4c.

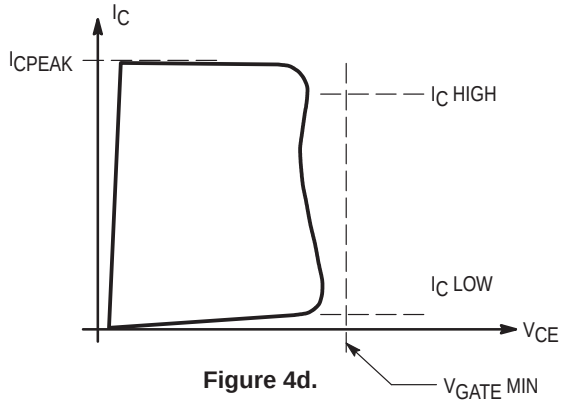


Figure 4d.

The transistor FAILS if its Collector/Emitter breakdown voltage is less than the V_{GATE} value, Figure 4d.

Figure 4. Energy Test Criteria for BU323Z

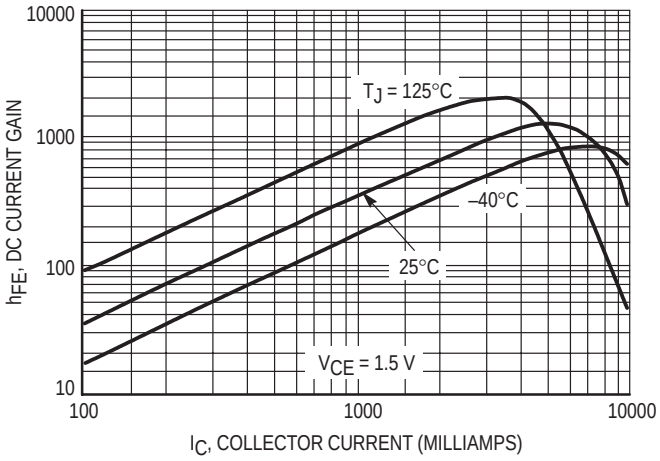


Figure 5. DC Current Gain

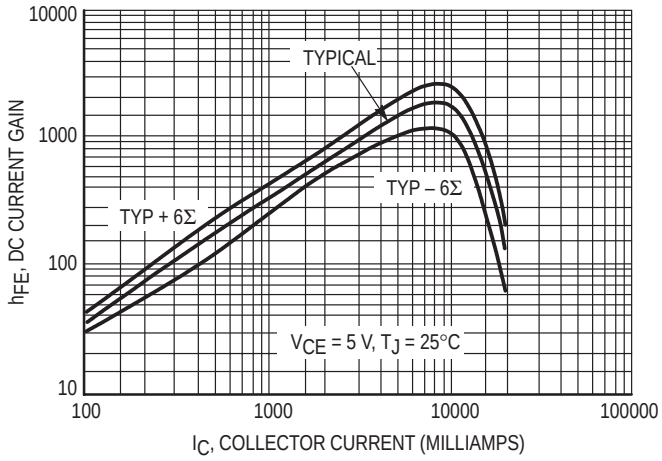


Figure 6. DC Current Gain

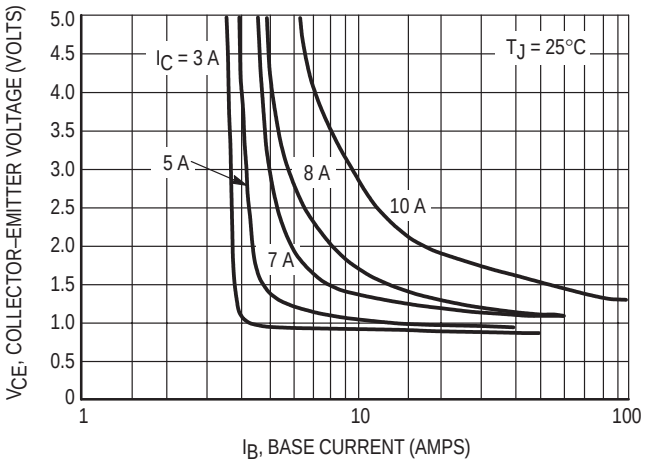


Figure 7. Collector Saturation Region

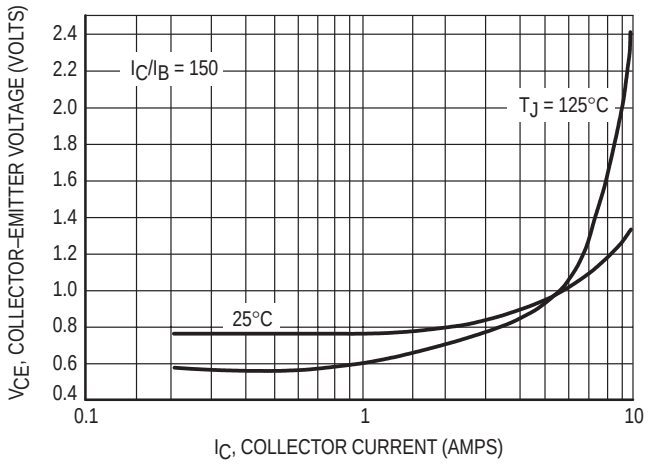


Figure 8. Collector–Emitter Saturation Voltage

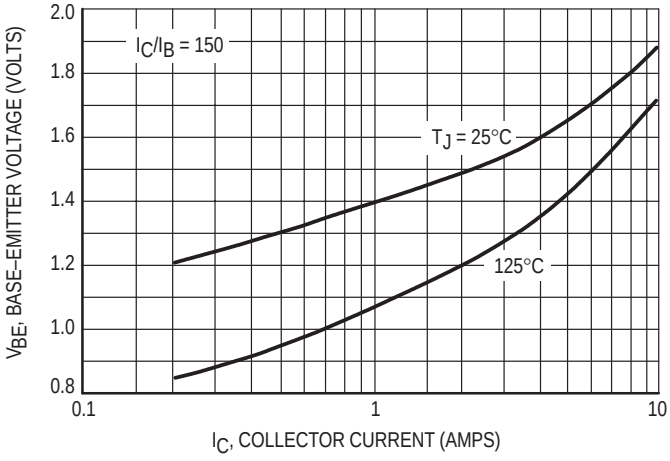


Figure 9. Base–Emitter Saturation Voltage

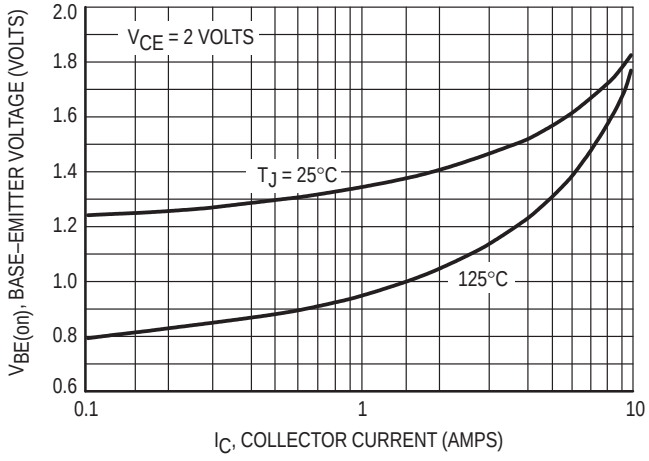


Figure 10. Base–Emitter “ON” Voltages

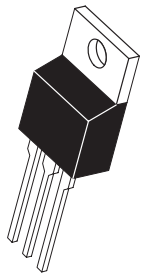
BU406
BU407

NPN Power Transistors

7 AMPERES
NPN SILICON
POWER TRANSISTORS
60 WATTS
150 and 200 VOLTS

These devices are high voltage, high speed transistors for horizontal deflection output stages of TV's and CRT's.

- High Voltage: V_{CEV} = 330 or 400 V
- Fast Switching Speed: t_f = 750 ns (max)
- Low Saturation Voltage: $V_{CE(sat)}$ = 1 V (max) @ 5 A
- Packaged in Compact JEDEC TO–220AB



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BU406	BU407	Unit
Collector–Emitter Voltage	V_{CEO}	200	150	Vdc
Collector–Emitter Voltage	V_{CEV}	400	330	Vdc
Collector–Base Voltage	V_{CBO}	400	330	Vdc
Emitter Base Voltage	V_{EBO}	6		Vdc
Collector Current — Continuous Peak Repetitive Peak (10 ms)	I_C	7 10 15		Adc
Base Current	I_B	4		Adc
Total Device Dissipation, T_C = 25°C Derate above T_C = 25°C	P_D	60 0.48		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage(1) (I_C = 100 mAdc, I_B = 0)	BU406 BU407	$V_{CEO(sus)}$	200 150	— —	— —	Vdc
Collector Cutoff Current		I_{CES}				mAdc
(V_{CE} = Rated V_{CEV}, V_{BE} = 0)			—	—	5	
(V_{CE} = Rated V_{CEO} + 50 Vdc, V_{BE} = 0)			—	—	0.1	
(V_{CE} = Rated V_{CEO} + 50 Vdc, V_{BE} = 0, T_C = 150°C)			—	—	1	
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)	BU406, BU407	I_{EBO}	—	—	1	mAdc
ON CHARACTERISTICS (1)						
Collector–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)		$V_{CE(sat)}$	—	—	1	Vdc
Base–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)		$V_{BE(sat)}$	—	—	1.2	Vdc
Forward Diode Voltage (I_{EC} = 5 Adc) "D" only		V_{EC}	—	—	2	Volts

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 1%.

(continued)

REV 2

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 20 MHz)	f_T	10	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	80	—	pF
SWITCHING CHARACTERISTICS					
Inductive Load Crossover Time (V_{CC} = 40 Vdc, I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc, L = 150 μH)	t_c	—	—	0.75	μs

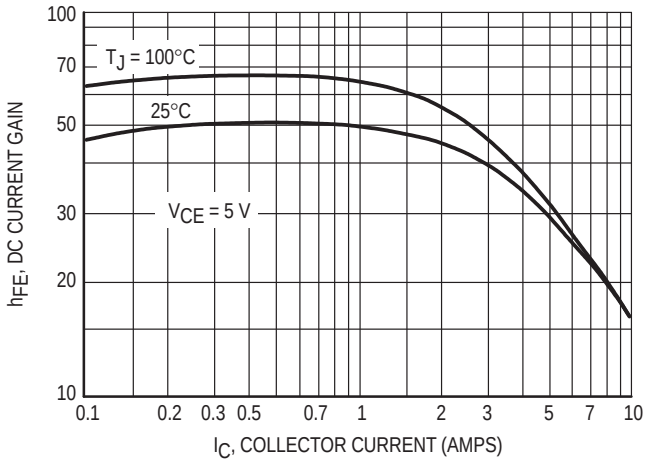


Figure 1. DC Current Gain

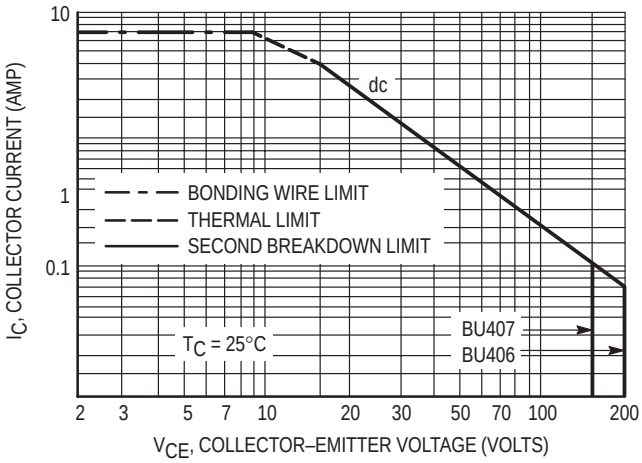


Figure 2. Maximum Rated Forward Bias Safe Operating Area

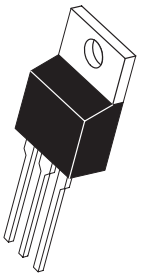
BU522B

High Voltage Silicon Power Darlingtons

7 AMPERES
DARLINGTON
POWER TRANSISTORS
NPN SILICON
450 VOLTS
75 WATTS

Power Transistor mainly intended for use as ignition circuit output transistor.

- Specified minimum sustaining voltage:
  $V_{CER(sus)}$ = 425 V at I_C = 1 A
- High S.O.A. capability:
  V_{CE} = 400 V
- Low $V_{CE(sat)}$ = 2.0 V max. at I_C = 4 A



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BU522B	Unit
Collector–Emitter Voltage Sust.	$V_{CER(sus)}$	425	Vdc
Collector–Emitter Voltage	V_{CER}	450	Vdc
Collector–Base Voltage	V_{CBO}	475	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current Continuous	I_C	7.0	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.60	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max.	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W

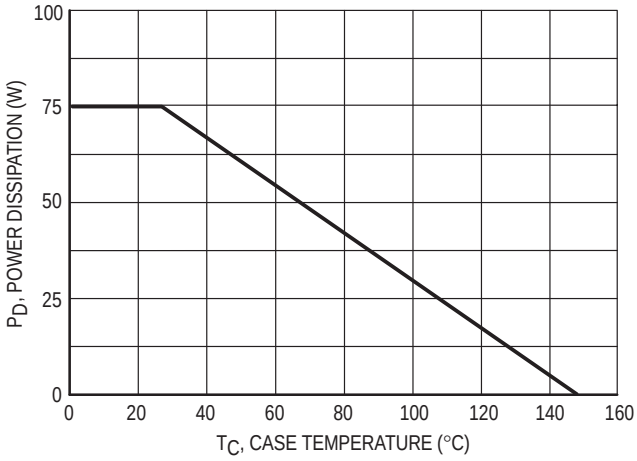
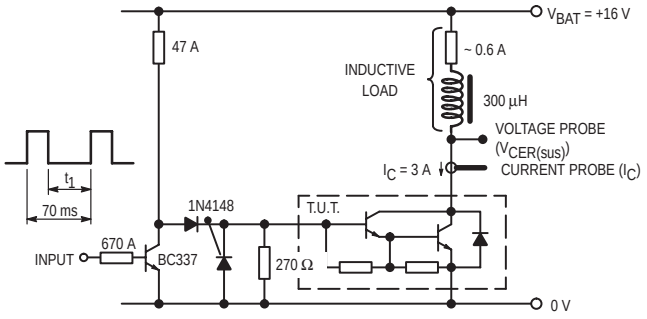


Figure 1. Power Derating

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (See Figure 2) (I_C = 1.0 A) See Figure 2	$V_{CER(sus)}$	425			Vdc
Collector Cutoff Current (Rated V_{CER}, R_{BE} = 270 Ω)	I_{CER}			1.0	mAdc
Collector Cutoff Current (Rated V_{CBO}, I_E = 0)	I_{CBO}			1.0	mAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}			40	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 5 Vdc)	h_{FE}	250			—
Collector–Emitter Saturation Voltage (I_C = 4 Adc, I_B = 80 mAdc)	$V_{CE(sat)}$			2	Vdc
Base–Emitter Saturation Voltage (I_C = 4 Adc, I_B = 80 mAdc)	$V_{BE(sat)}$			2.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (I_C = 0.3 mAdc, V_{CE} = 5.0 Vdc, f_{test} = 10 MHz)	f_T		7.5		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}		150		pF



t_1 to be selected that I_C reaches 3 Adc before switch–off
Case temperature of the power transistor T_C = 25°C

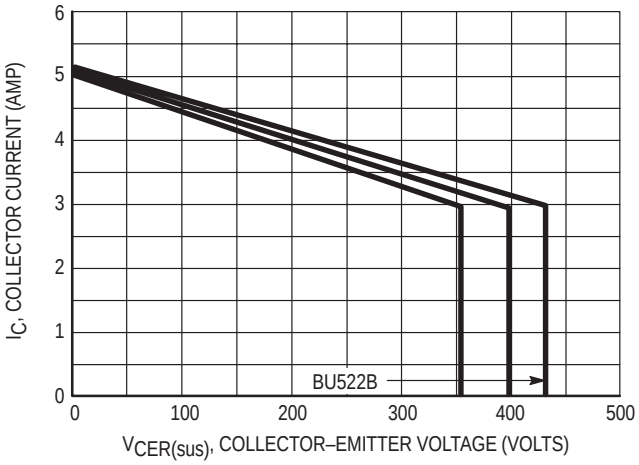
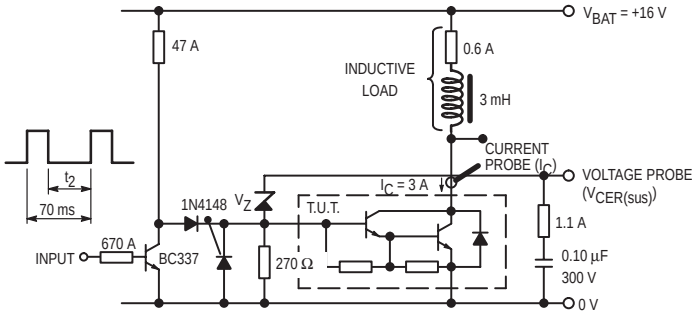


Figure 2. Sustaining Voltage Test $V_{CER(sus)}$

Test conditions of the Collector–Base Clamping Circuit:



Clamping device characteristics:

V_Z = 400 V ± 1% at I_Z = 20 mA

Clamping duration is around 40 µsec

t_2 to be selected that I_L reaches 5 Adc before switch–off

Case temperature of the power transistor: T_C = 25°C.

Figure 3. S.O.A. Test

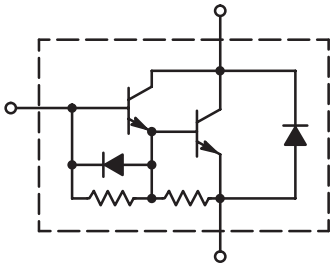
BU806

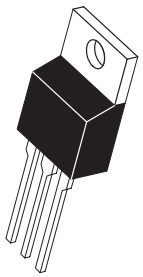
NPN Darlington Power Transistor

8.0 AMPERE DARLINGTON NPN POWER TRANSISTORS 60 WATTS 200 VOLTS

This Darlington transistor is a high voltage, high speed device for use in horizontal deflection circuits in TV's and CRT's.

- High Voltage: V_{CEV} = 330 or 400 V
- Fast Switching Speed:
  t_c = 1.0 µs (max)
- Low Saturation Voltage:
  $V_{CE(sat)}$ = 1.5 V (max)
- Packaged in JEDEC TO–220AB
- Damper Diode V_F is specified.
  V_F = 2.0 V (max)





CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BU806	Unit
Collector–Emitter Voltage	V_{CEO}	200	Vdc
Collector–Emitter Voltage	V_{CEV}	400	Vdc
Collector–Base Voltage	V_{CBO}	400	Vdc
Emitter–Base Voltage	V_{EBO}	6.0	Vdc
Collector Current — Continuous — Peak	I_C	8.0 15	Adc
Emitter–Collector Diode Current	I_F	10	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation, T_C = 25°C Derate above T_C = 25°C	P_D	60 0.48	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.08	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W
Lead Temperature for Soldering Purposes, 1/8″ from Case for 5.0 Seconds	T_L	275	°C

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)		$V_{CEO(sus)}$	200	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CBO}, V_{BE} = 0)		I_{CES}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 6.0 Vdc)		I_{CEV}	—	—	100	μAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	—	3.0	mAdc
ON CHARACTERISTICS (1)						
Collector–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 50 mAdc)		$V_{CE(sat)}$	—	—	1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 50 mAdc)		$V_{BE(sat)}$	—	—	2.4	Vdc
Emitter–Collector Diode Forward Voltage (I_F = 4.0 Adc)		V_F	—	—	2.0	Vdc
SWITCHING CHARACTERISTICS						
Turn–On Time	(Resistive Load, V_{CC} = 100 Vdc, I_C = 5.0 Adc, I_{B1} = 50 mAdc, I_{B2} = 500 mAdc)	t_{on}	—	0.35	—	μs
Storage Time		t_s	—	0.55	—	μs
Fall Time		t_f	—	0.20	—	μs
Crossover Time (I_C = 5.0 Adc, I_{B1} = 50 mAdc, $V_{BE(off)}$ = 4.0 Vdc, V_{clamp} = 200 Vdc, L = 500 μH)		t_c	—	0.40	1.0	μs

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 1%.

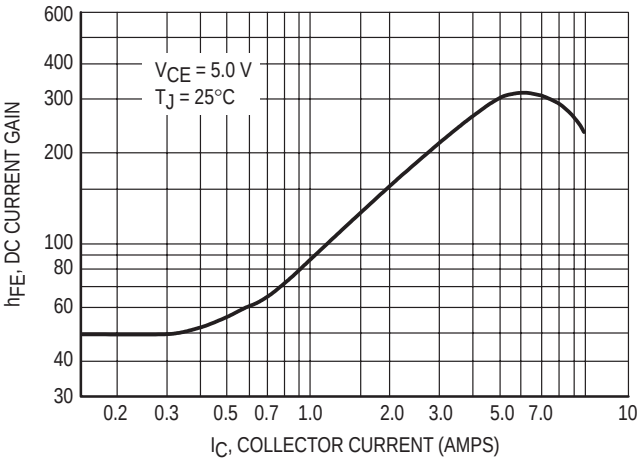


Figure 1. DC Current Gain

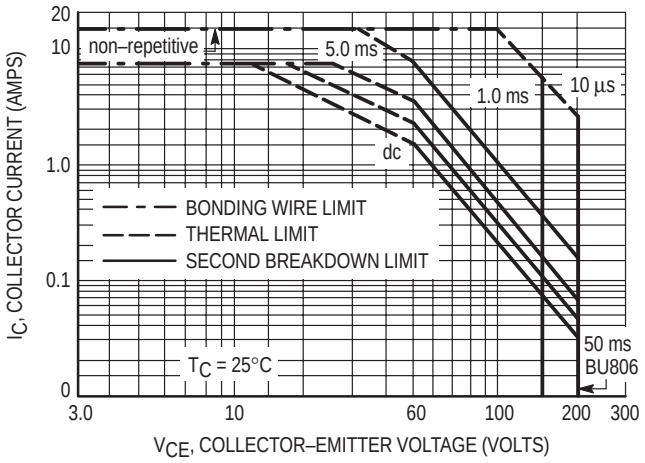


Figure 2. Safe Operating Area (FBSOA)

BUD43B

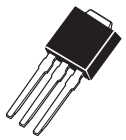
Product Preview

SWITCHMODE NPN Silicon Planar Power Transistor

POWER TRANSISTORS
2 AMPERES
700 VOLTS
25 WATTS

The BUD43B has an application specific state–of–the–art die designed for use in 220 V line operated Switchmode Power supplies and electronic ballast (“light ballast”). The main advantages brought by this new transistor are:

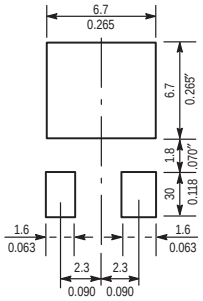
- Improved Efficiency Due to Low Base Drive Requirements:
  - — High and Flat DC Current Gain h_{FE}
  - — Fast and Tightened Switching Distributions
  - — No Coil Required in Base Circuit for Fast Turn–off (no current tail)



CASE 369–07

CASE 369A–13

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	350	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	650	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	650	Vdc
Emitter–Base Voltage	V_{EBO}	9	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	2 4	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	1 2	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	25 0.2	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 5 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	350			Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{BE} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			10 200	μAdc
Emitter–Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.5 Adc)		$V_{BE(sat)}$			125	Vdc
Collector–Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.5 Adc)	@ T_C = 25°C	$V_{CE(sat)}$			1	Vdc
DC Current Gain (I_C = 1 Adc, V_{CE} = 2 Vdc) (I_C = 2 Adc, V_{CE} = 5 Vdc)	 @ T_C = 25°C @ T_C = 25°C	h_{FE}	 8 6			
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}		40		pF
Input Capacitance (V_{EB} = 8 V)		C_{ib}		400		pF

SWITCHING CHARACTERISTICS (Resistive Load) (D.C. ≤ 10%, Pulse Width = 20 μs)

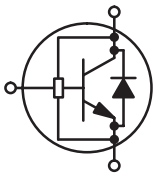
Turn–on Time	(I_C = 1.2 Adc, I_{B1} = 0.4 Adc, I_{B2} = 0.1 Adc, V_{CC} = 300 V)	@ T_C = 25°C	t_{off}	4.7		5.8	μs
Fall Time	(I_C = 2.5 Adc, I_{B1} = 0.5 Adc, I_{B2} = 0.5 Adc, V_{CC} = 150 V)	@ T_C = 25°C	t_f			800	ns

BUD44D2

POWER TRANSISTORS
2 AMPERES
700 VOLTS
25 WATTS

Advance Information

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

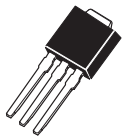


The BUD44D2 is state–of–art High Speed High gain BIPolar transistor (H2BIP). High dynamic characteristics and lot to lot minimum spread (±150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an h_{FE} window.

Main features:

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ I_C = 100 mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector–Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic $V_{CE(sat)}$
- "6 Sigma" Process Providing Tight and Reproductible Parameter Spreads

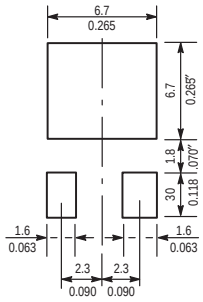
It's characteristics make it also suitable for PFC application.



CASE 369–07

CASE 369A–13

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter–Base Voltage	V_{EBO}	12	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	2 5	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	1 2	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	25 0.2	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 5 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	400	470		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	700	920		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	12	14.5		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CEO}			50 500	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0) (V_{CE} = 500 V, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C @ T_C = 125°C	I_{CES}			50 500 100	μAdc
Emitter–Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 0.4 Adc, I_B = 40 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{BE(sat)}$		0.78 0.65	0.9 0.8	Vdc
(I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C			0.87 0.76	1 0.9	
Collector–Emitter Saturation Voltage (I_C = 0.4 Adc, I_B = 20 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.45 0.67	0.65 1	Vdc
(I_C = 0.4 Adc, I_B = 40 mAdc)	@ T_C = 25°C @ T_C = 125°C			0.25 0.27	0.4 0.5	
(I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C			0.28 0.35	0.5 0.6	
DC Current Gain (I_C = 0.4 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	20 18	32 26		—
(I_C = 1 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		10 7	14 9.5		
(I_C = 2 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C		8	11		
DIODE CHARACTERISTICS						
Forward Diode Voltage (I_{EC} = 0.2 Adc)	@ T_C = 25°C	V_{EC}		0.8	1	V
(I_{EC} = 0.2 Adc)	@ T_C = 125°C			0.6		
(I_{EC} = 0.4 Adc)	@ T_C = 25°C			0.9	1.2	
(I_{EC} = 1 Adc)	@ T_C = 25°C			1.1	1.5	
Forward Recovery Time (see Figure 22 bis) (I_F = 0.2 Adc, di/dt = 10 A/μs)	@ T_C = 25°C	T_{fr}		415		ns
(I_F = 0.4 Adc, di/dt = 10 A/μs)	@ T_C = 25°C			390		
(I_F = 1 Adc, di/dt = 10 A/μs)	@ T_C = 25°C			340		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
DYNAMIC SATURATION VOLTAGE								
Dynamic Saturation Voltage: Determined 1 µs and 3 µs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 0.4 A, I_{B1} = 40 mA, V_{CC} = 300 V	@ 1 µs	@ T_C = 25°C	$V_{CE(dsat)}$		3.3		V
			@ T_C = 125°C			6.8		
		@ 3 µs	@ T_C = 25°C			0.5		
			@ T_C = 125°C			1.3		
	I_C = 1 A, I_{B1} = 0.2 A, V_{CC} = 300 V	@ 1 µs	@ T_C = 25°C			4.4		
			@ T_C = 125°C			12.8		
		@ 3 µs	@ T_C = 25°C			0.5		
			@ T_C = 125°C			1.8		
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)				f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)				C_{ob}		50	75	pF
Input Capacitance (V_{EB} = 8 Vdc)				C_{ib}		240	500	pF
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 µs)								
Turn–on Time	I_C = 1 Adc, I_{B1} = 0.2 Adc, I_{B2} = 0.5 Adc, V_{CC} = 300 Vdc		@ T_C = 25°C	t_{on}		90	150	ns
			@ T_C = 125°C			105		
Turn–off Time			@ T_C = 25°C	t_{off}		1.1	1.25	µs
			@ T_C = 125°C			1.5		
Turn–on Time	I_C = 0.5 Adc, I_{B1} = 50 mAdc, I_{B2} = 250 mAdc, V_{CC} = 300 Vdc		@ T_C = 25°C	t_{on}	400		600	ns
			@ T_C = 125°C			600		
Turn–off Time			@ T_C = 25°C	t_{off}	750		1000	ns
			@ T_C = 125°C			1300		
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 µH)								
Fall Time	I_C = 0.4 Adc, I_{B1} = 40 mAdc, I_{B2} = 0.2 Adc		@ T_C = 25°C	t_f		110	150	ns
			@ T_C = 125°C			105		
Storage Time			@ T_C = 25°C	t_s		0.55	0.75	µs
			@ T_C = 125°C			0.7		
Crossover Time			@ T_C = 25°C	t_c		85	150	ns
			@ T_C = 125°C			80		
Fall Time	I_C = 1 Adc, I_{B1} = 0.2 Adc, I_{B2} = 0.5 Adc		@ T_C = 25°C	t_f		100	150	ns
			@ T_C = 125°C			90		
Storage Time			@ T_C = 25°C	t_s		1.05	1.5	µs
			@ T_C = 125°C			1.45		
Crossover Time			@ T_C = 25°C	t_c		100	175	ns
			@ T_C = 125°C			100		
Fall Time	I_C = 0.8 Adc, I_{B1} = 160 mAdc, I_{B2} = 160 mAdc		@ T_C = 25°C	t_f		110	150	ns
			@ T_C = 125°C			180		
Storage Time			@ T_C = 25°C	t_s	2.05		2.35	µs
			@ T_C = 125°C			2.8		
Crossover Time			@ T_C = 25°C	t_c		180	300	ns
			@ T_C = 125°C			400		
Fall Time	I_C = 0.4 Adc, I_{B1} = 40 mAdc, I_{B2} = 40 mAdc		@ T_C = 25°C	t_f		150	225	ns
			@ T_C = 125°C			175		
Storage Time			@ T_C = 25°C	t_s	1.65		1.95	µs
			@ T_C = 125°C			2.2		
Crossover Time			@ T_C = 25°C	t_c		150	250	ns
			@ T_C = 125°C			330		

TYPICAL STATIC CHARACTERISTICS

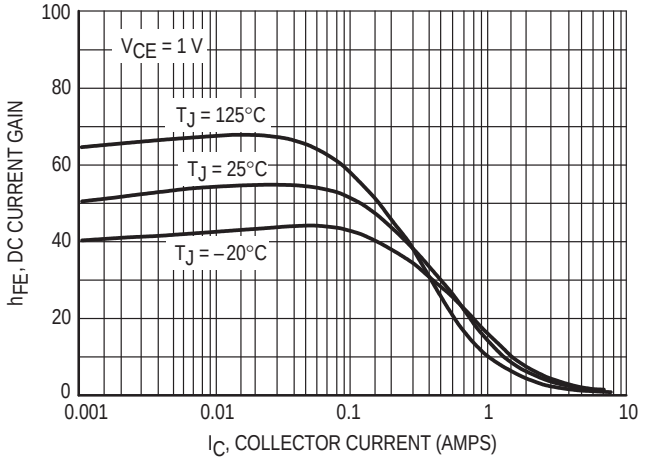


Figure 1. DC Current Gain @ 1 Volt

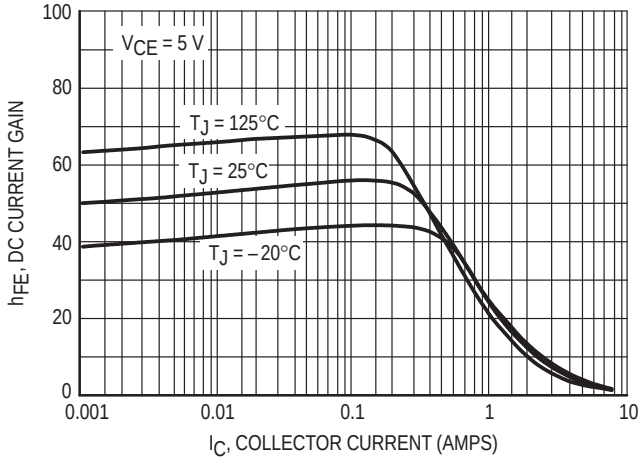


Figure 2. DC Current Gain @ 5 Volt

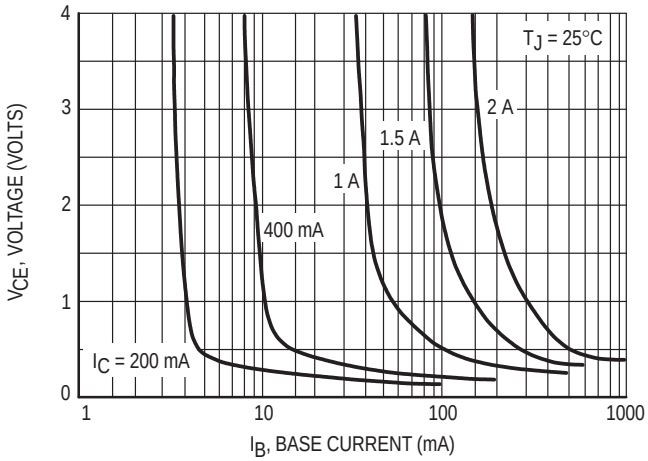


Figure 3. Collector Saturation Region

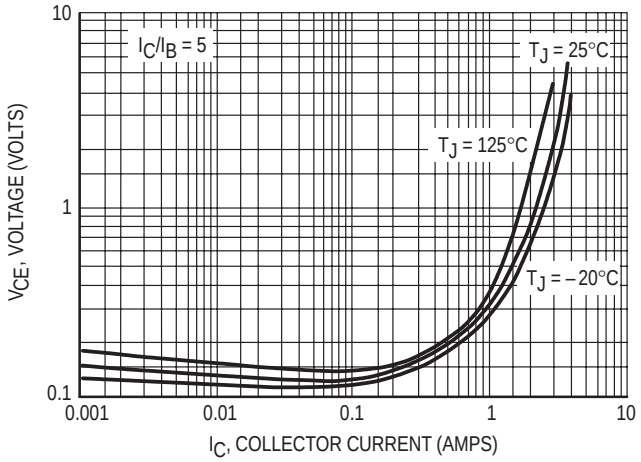


Figure 4. Collector–Emitter Saturation Voltage

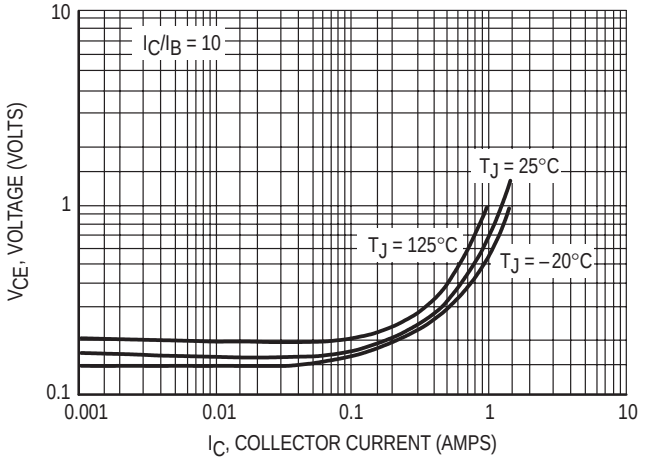


Figure 5. Collector–Emitter Saturation Voltage

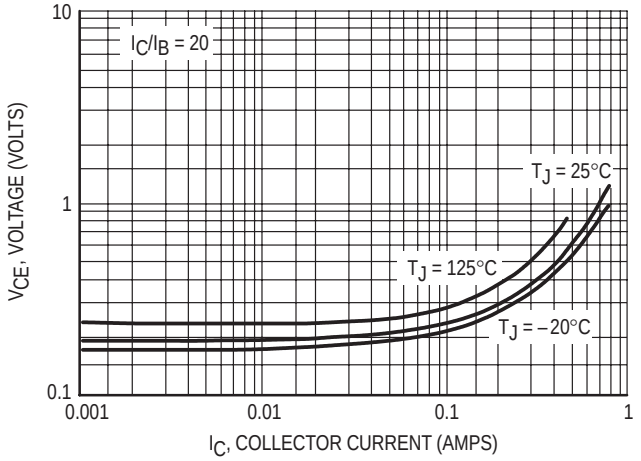


Figure 6. Collector–Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

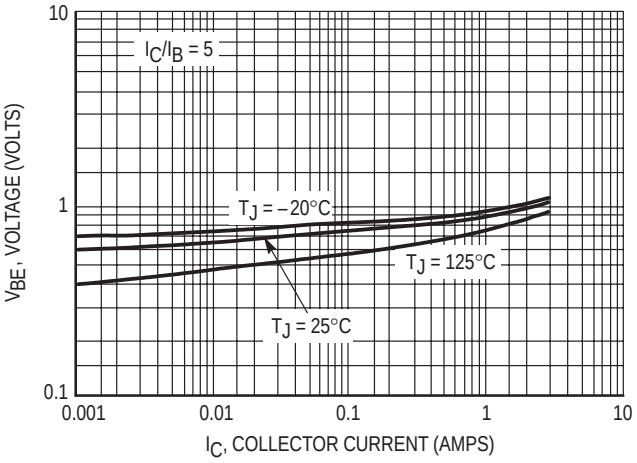


Figure 7A. Base–Emitter Saturation Region

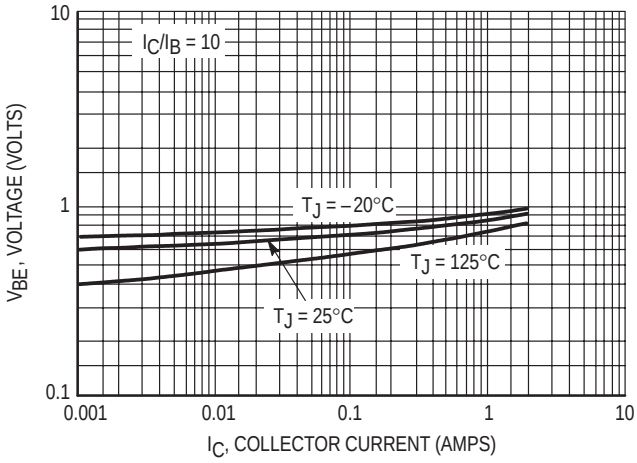


Figure 7B. Base–Emitter Saturation Region

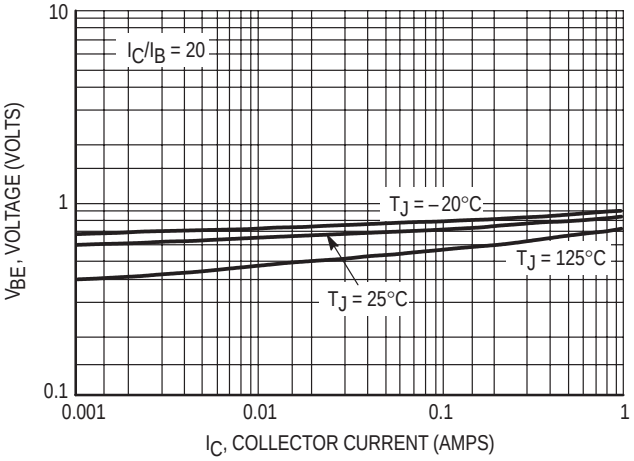


Figure 7C. Base–Emitter Saturation Region

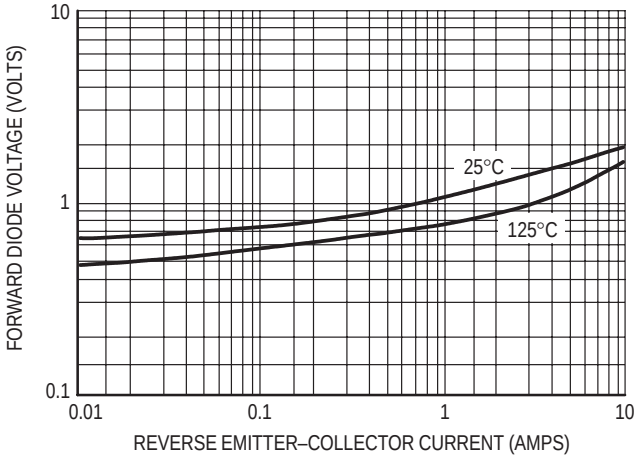


Figure 8. Forward Diode Voltage

TYPICAL SWITCHING CHARACTERISTICS

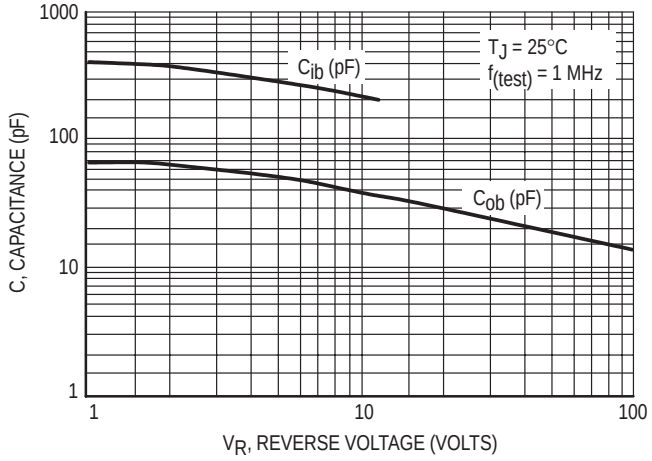


Figure 9. Capacitance

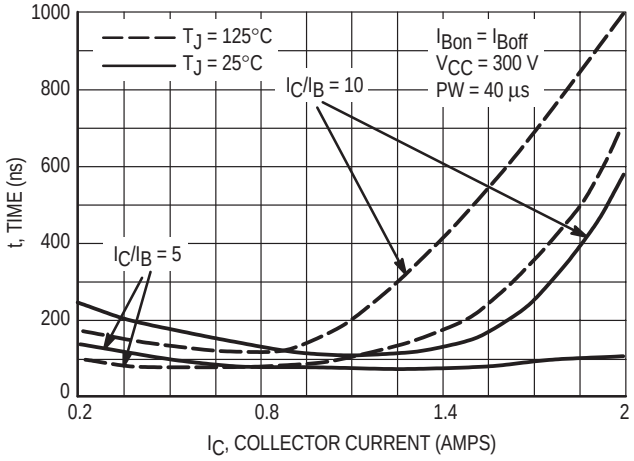


Figure 10. Resistive Switch Time, t_{on}

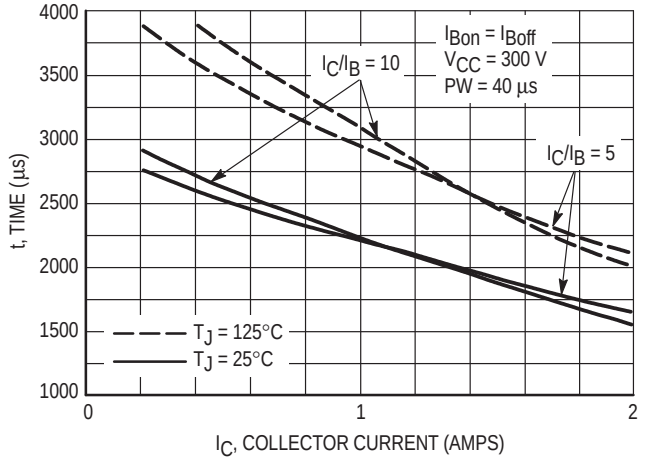


Figure 11. Resistive Switch Time, t_{off}

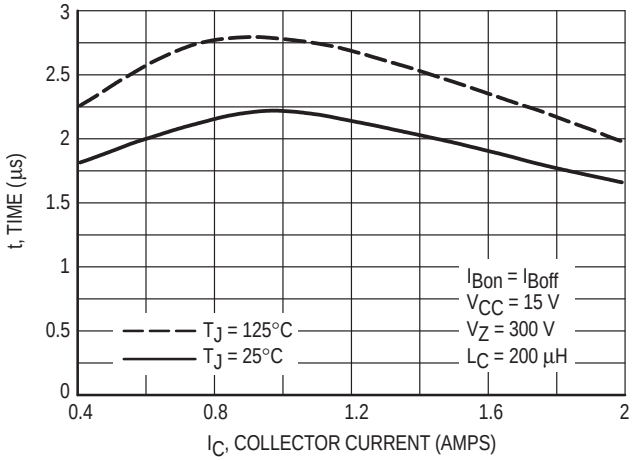


Figure 12. Inductive Storage Time, t_{si} @ I_C/I_B = 5

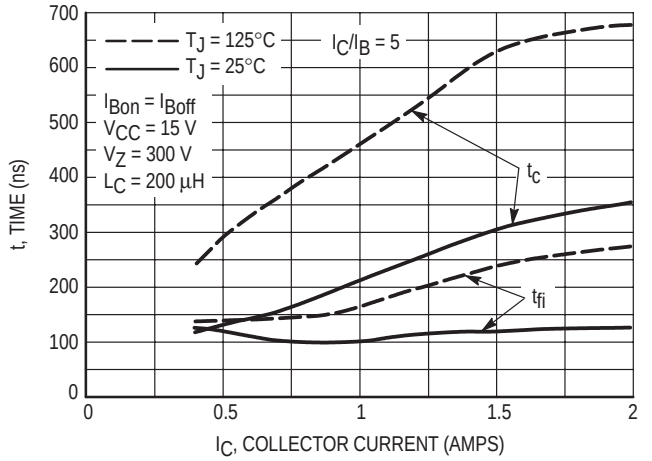


Figure 13. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 5

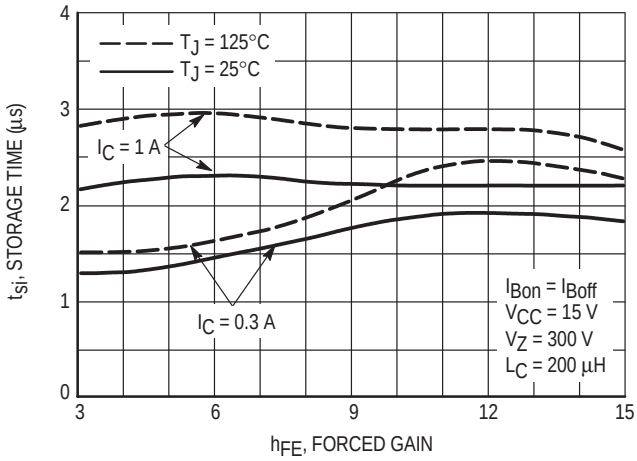


Figure 14. Inductive Storage Time

TYPICAL SWITCHING CHARACTERISTICS

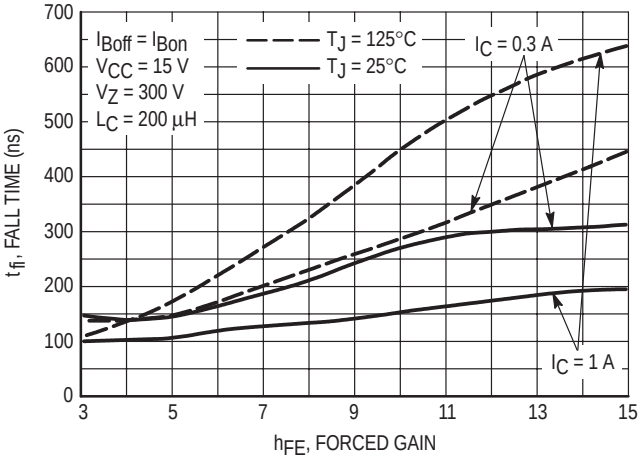


Figure 15. Inductive Fall Time

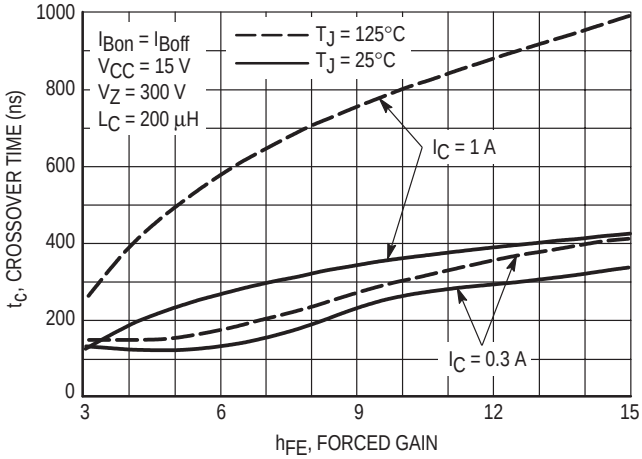


Figure 16. Inductive Crossover Time

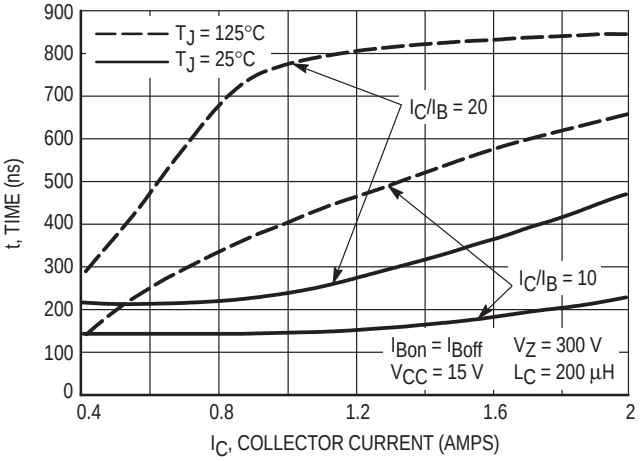


Figure 17. Inductive Switching, t_{fi}

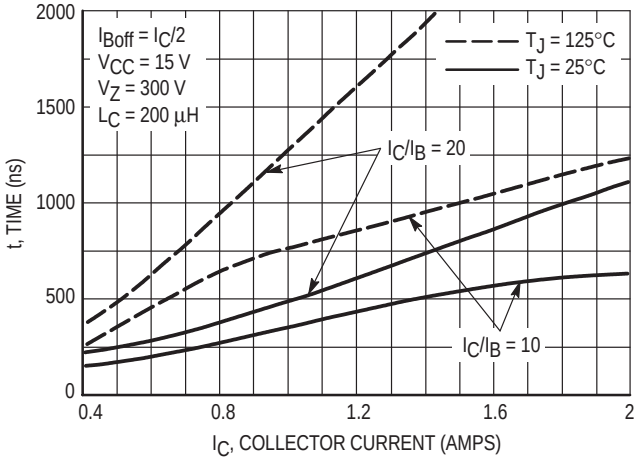


Figure 18. Inductive Switching, t_c

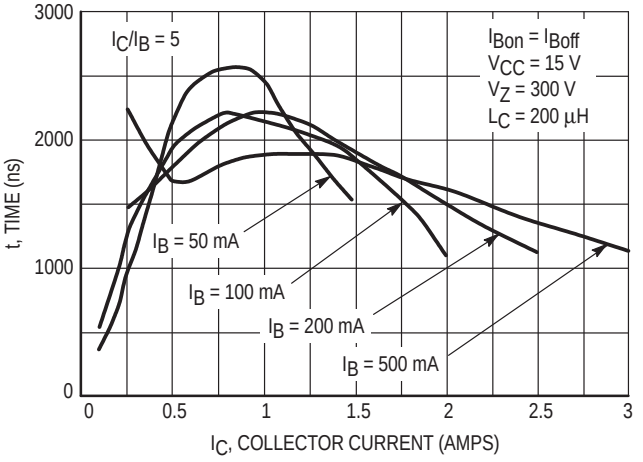


Figure 19. Inductive Storage Time, t_{si}

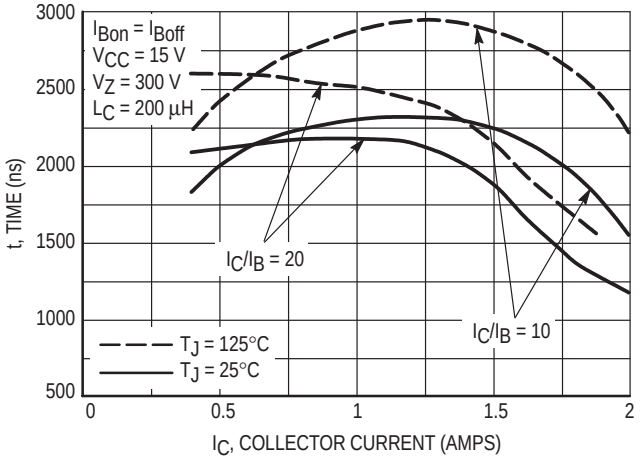


Figure 20. Inductive Storage Time, t_{si}

TYPICAL SWITCHING CHARACTERISTICS

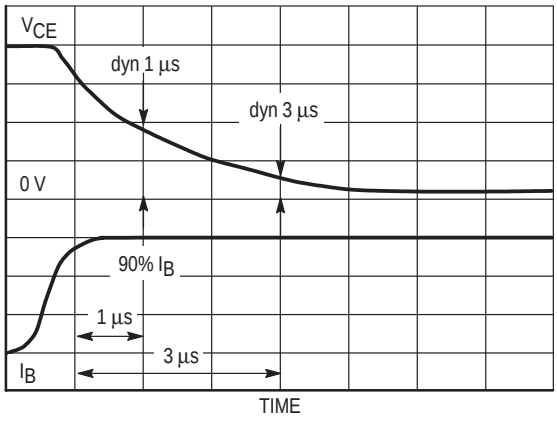


Figure 21. Dynamic Saturation Voltage Measurements

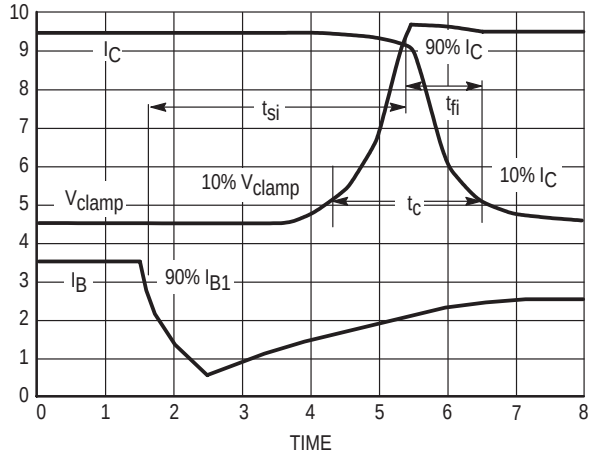


Figure 22. Inductive Switching Measurements

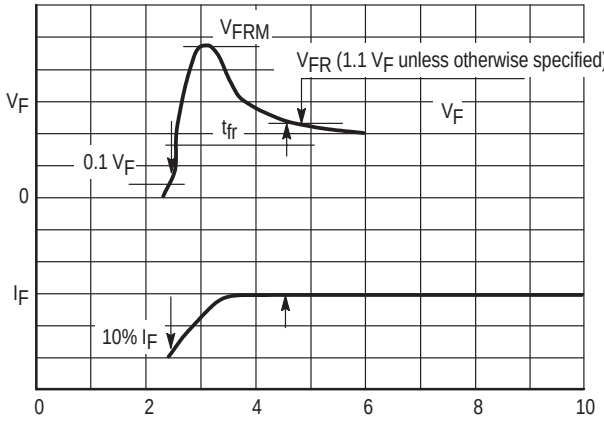
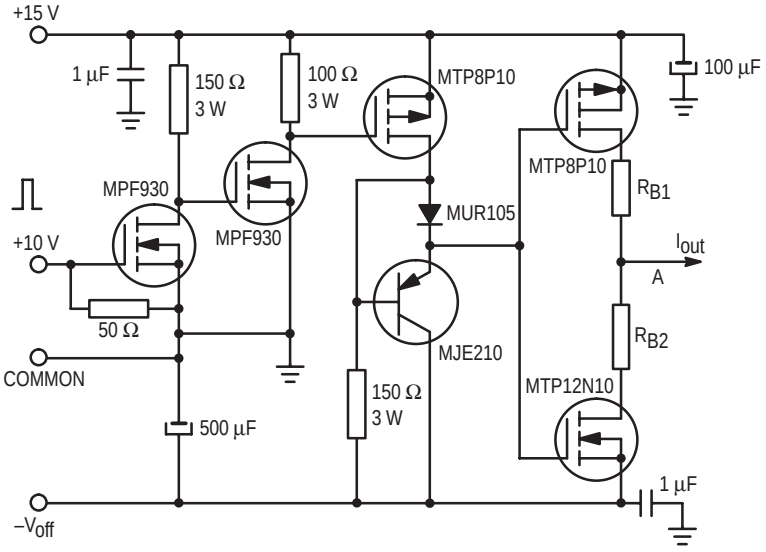
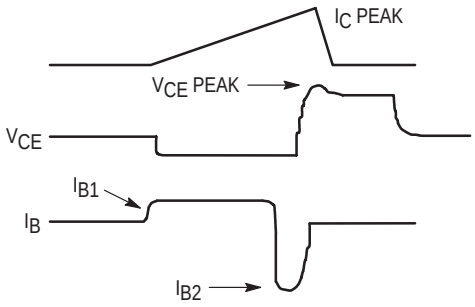


Figure 22 bis. t_{fr} Measurements

TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL STATIC CHARACTERISTICS

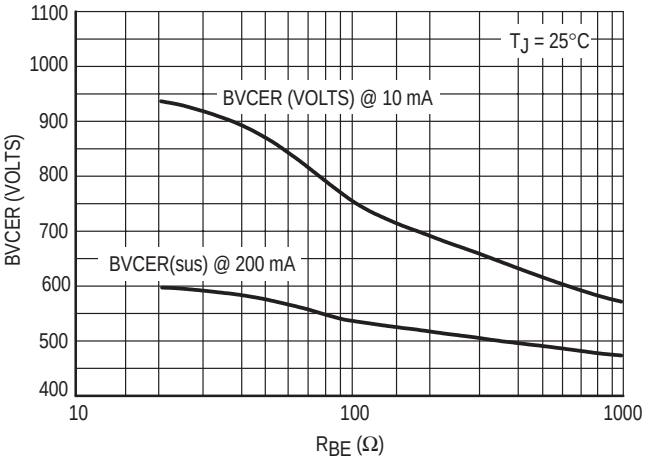


Figure 23. BVCER

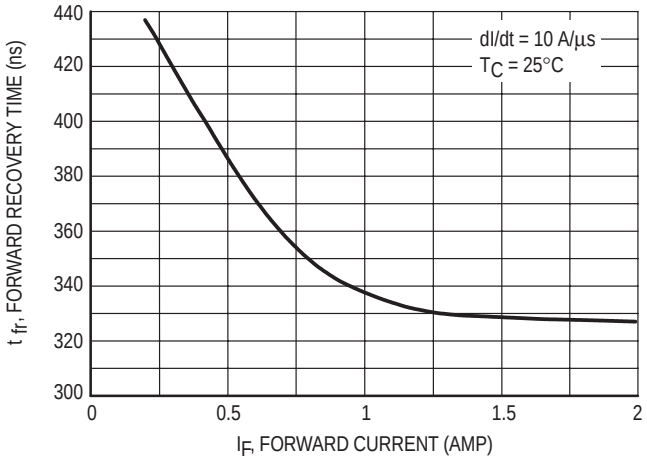


Figure 24. Forward Recovery Time t_{fr}

BUH50

Designer's™ Data Sheet

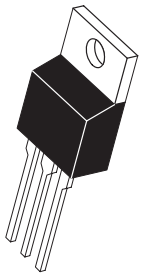
SWITCHMODE NPN Silicon Planar Power Transistor

POWER TRANSISTOR
4 AMPERES
800 VOLTS
50 WATTS

The BUH50 has an application specific state–of–art die designed for use in 50 Watts HALOGEN electronic transformers and switchmode applications.

This high voltage/high speed transistor exhibits the following main feature:

- Improved Efficiency Due to Low Base Drive Requirements:
  — High and Flat DC Current Gain h_{FE}
  — Fast Switching
- Motorola "6SIGMA" Philosophy Provides Tight and Reproductible Parametric Distributions
- Specified Dynamic Saturation Data
- Full Characterization at 125°C



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	500	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	800	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	800	Vdc
Emitter–Base Voltage	V_{EBO}	9	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	4 8	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	50 0.4	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)			$V_{CEO(sus)}$	500			Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)			I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C		I_{CES}			100 1000	μAdc
Emitter–Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)			I_{EBO}			100	μAdc
ON CHARACTERISTICS							
Base–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.33 Adc) (I_C = 2 Adc, I_B = 0.66 Adc) 25°C (I_C = 2 Adc, I_B = 0.66 Adc) 100°C			$V_{BE(sat)}$		 0.86 0.94 0.85	 1.2 1.6 1.5	Vdc
Collector–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.33 Adc)	@ T_C = 25°C		$V_{CE(sat)}$		0.2	0.5	Vdc
(I_C = 2 Adc, I_B = 0.66 Adc)	@ T_C = 25°C @ T_C = 125°C				0.32 0.29	0.6 0.7	
(I_C = 3 Adc, I_B = 1 Adc)	@ T_C = 25°C				0.5	1	
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C		h_{FE}	7	13		—
(I_C = 2 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C			5	10		—
DYNAMIC CHARACTERISTICS							
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)			f_T	4			MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)			C_{ob}		50	100	pF
Input Capacitance (V_{EB} = 8 Vdc)			C_{ib}		850	1200	pF
DYNAMIC SATURATION VOLTAGE							
Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1 A I_{B1} = 0.33 A V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$		1.75 5		V
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C			0.3 0.5		V
	I_C = 2 A I_{B1} = 0.66 A V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C			6 14		V
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C			0.75 4		V

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)							
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc V_{CC} = 125 Vdc	@ T_C = 25°C	t_{on}		95	250	ns
Turn–off Time		@ T_C = 25°C	t_{off}		2.5	3.5	μs
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 1 Adc V_{CC} = 125 Vdc	@ T_C = 25°C	t_{on}		110	250	ns
Turn–off Time		@ T_C = 25°C	t_{off}		0.95	2	μs
Turn–on Time	I_C = 1 Adc, I_{B1} = 0.3 Adc I_{B2} = 0.3 Adc V_{CC} = 125 Vdc	@ T_C = 25°C	t_{on}		100	200	ns
Turn–off Time		@ T_C = 25°C	t_{off}		2.9	3.5	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 2 Adc I_{B1} = 0.4 Adc I_{B2} = 1 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		80 95	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		1.2 1.7	2.5	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		150 180	300	ns
Fall Time	I_C = 2 Adc I_{B1} = 0.66 Adc I_{B2} = 1 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		90 100	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		1.7 2.5	2.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		190 220	350	ns

TYPICAL STATIC CHARACTERISTICS

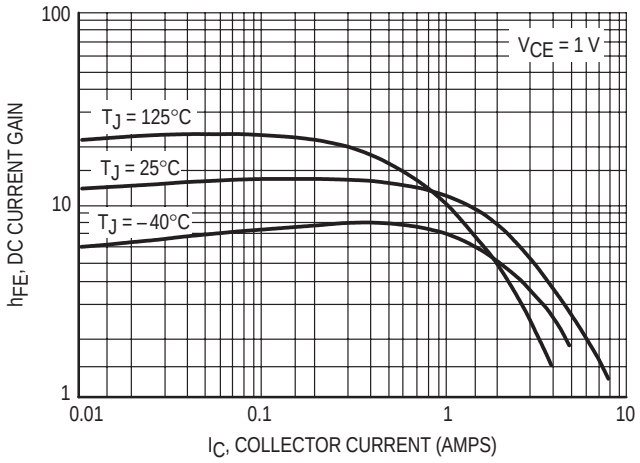


Figure 1. DC Current Gain @ 1 Volt

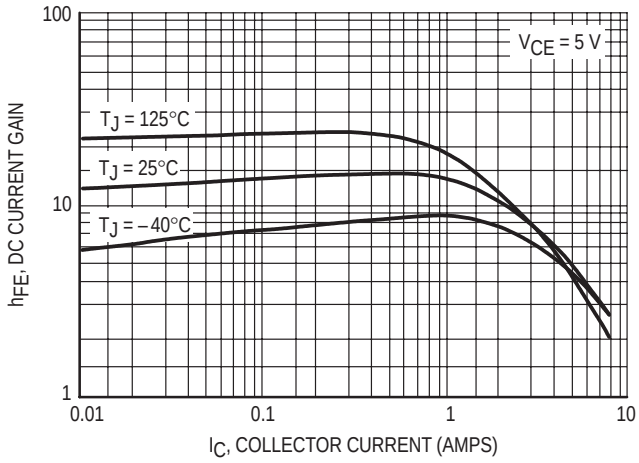


Figure 2. DC Current Gain @ 5 Volt

TYPICAL STATIC CHARACTERISTICS

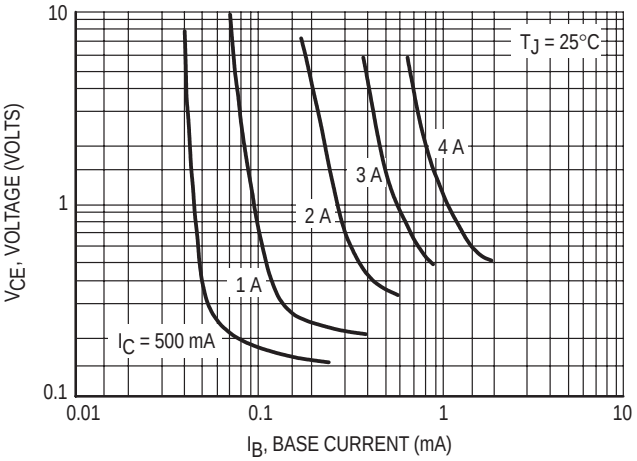


Figure 3. Collector Saturation Region

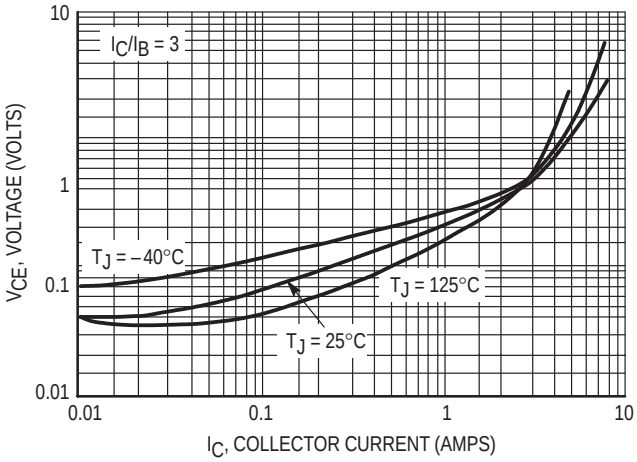


Figure 4. Collector–Emitter Saturation Voltage

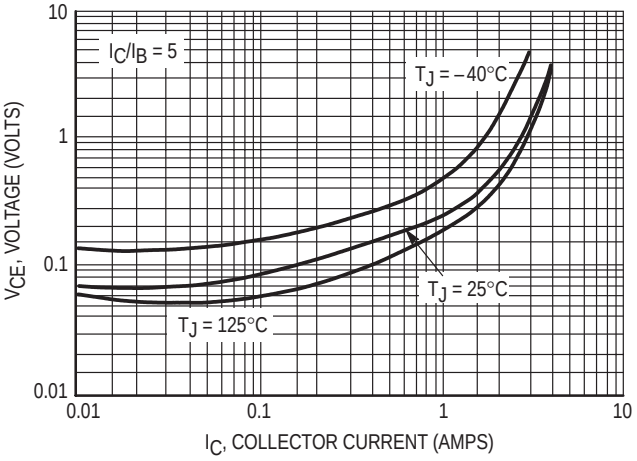


Figure 5. Collector–Emitter Saturation Voltage

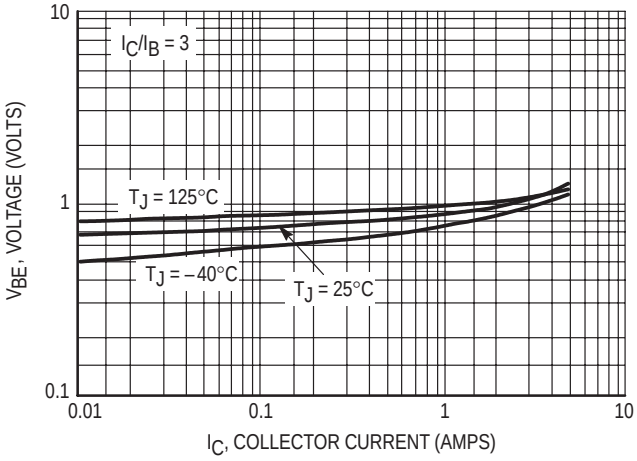


Figure 6. Base–Emitter Saturation Region

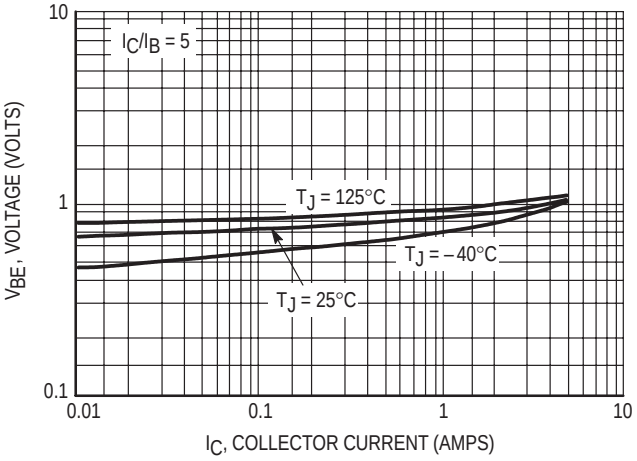


Figure 7. Base–Emitter Saturation Region

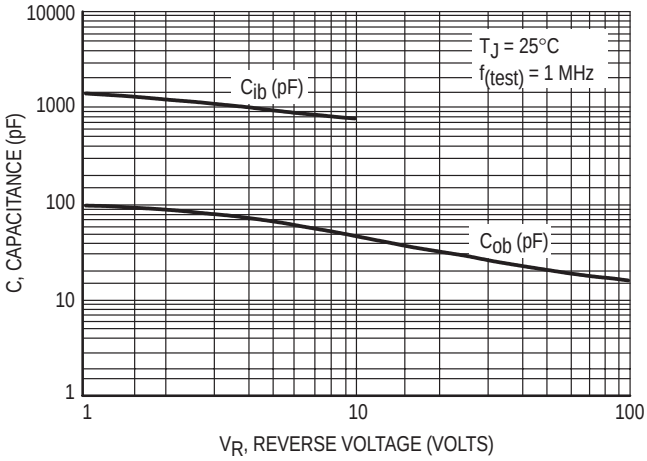


Figure 8. Capacitance

TYPICAL SWITCHING CHARACTERISTICS

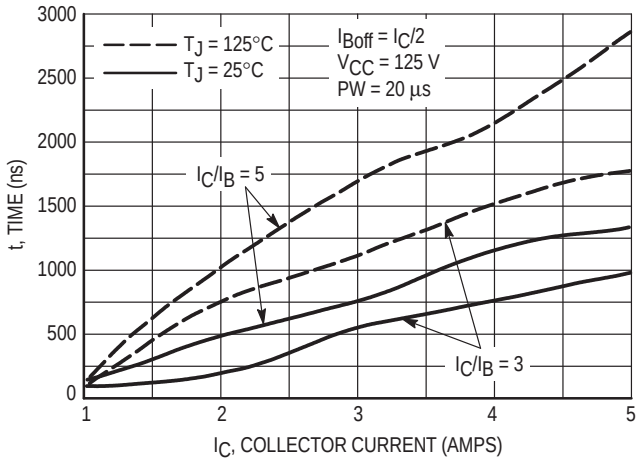


Figure 9. Resistive Switching, t_{on}

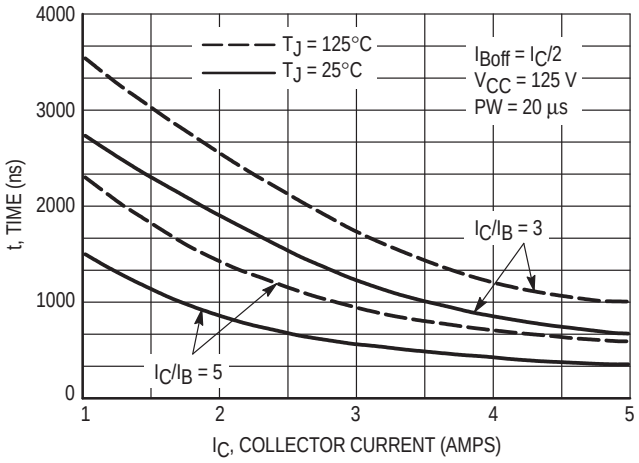


Figure 10. Resistive Switch Time, t_{off}

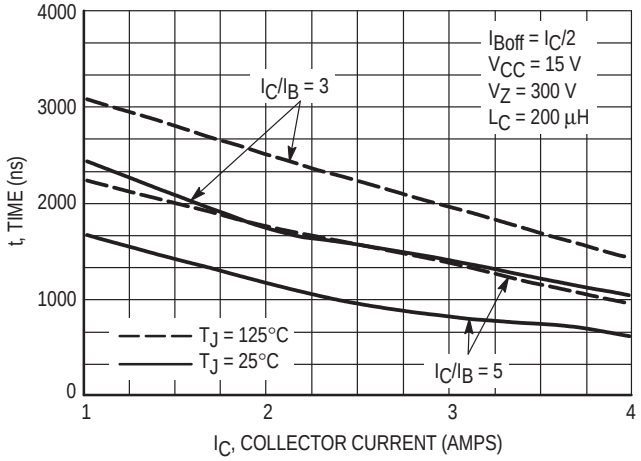


Figure 11. Inductive Storage Time, t_{si}

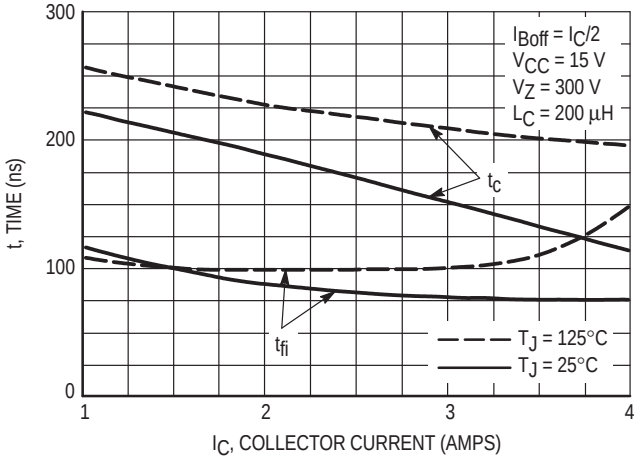


Figure 12. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 3

TYPICAL CHARACTERISTICS

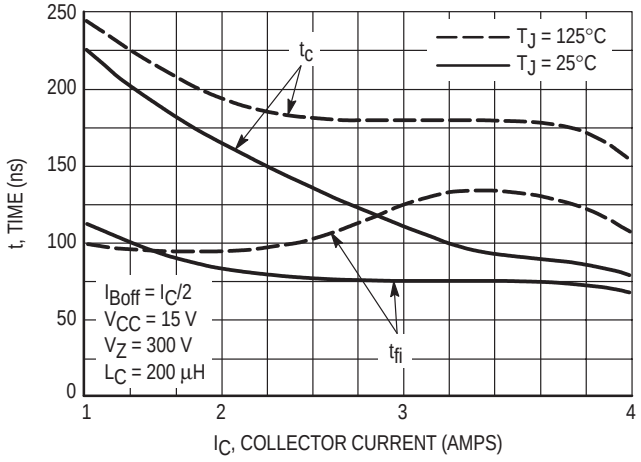


Figure 13. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 5

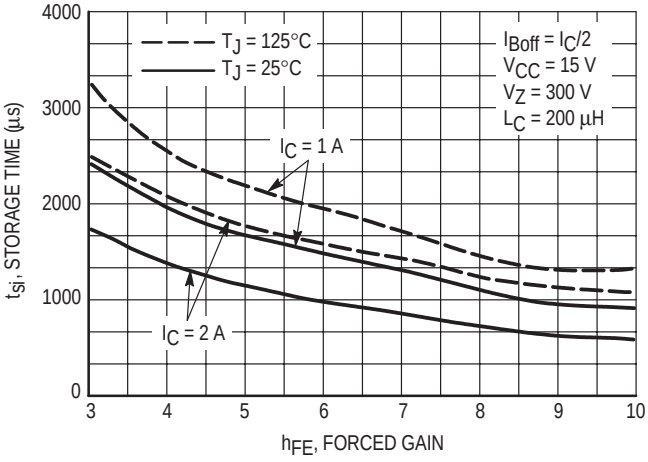


Figure 14. Inductive Storage Time

TYPICAL CHARACTERISTICS

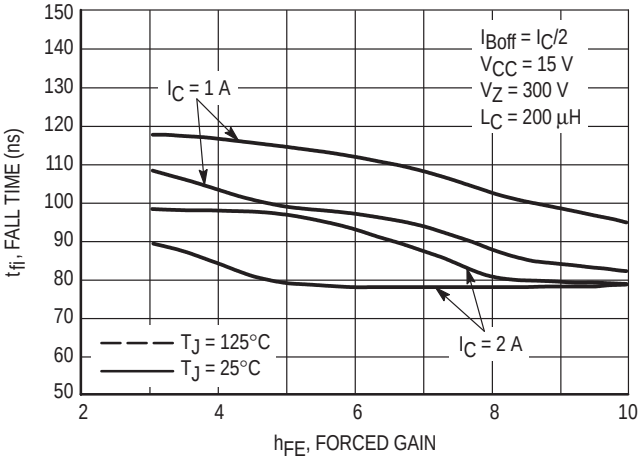


Figure 15. Inductive Fall Time

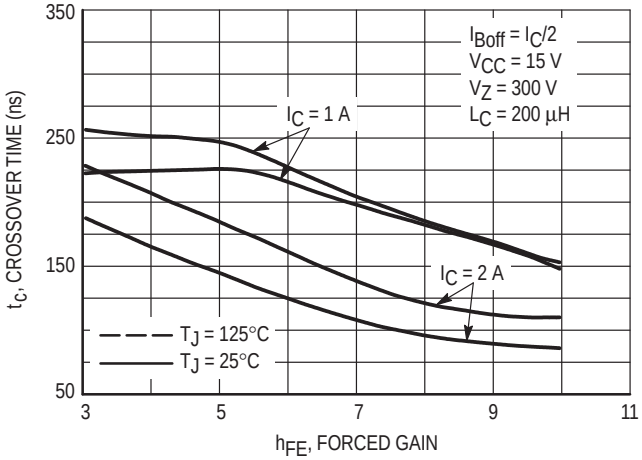


Figure 16. Inductive Crossover Time

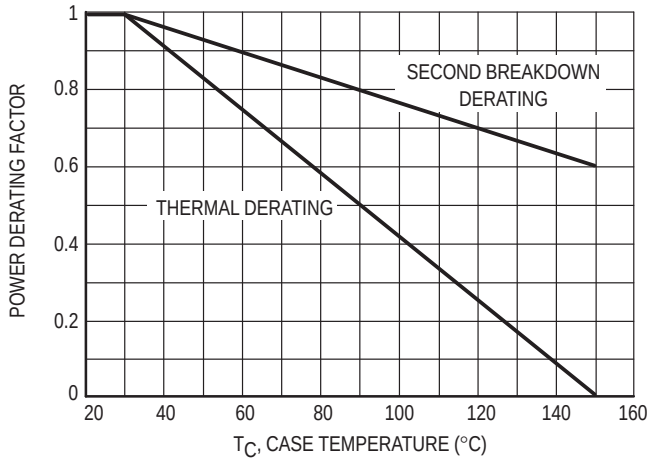


Figure 17. Forward Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 20 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 20 may be found at any case temperature by using the appropriate curve on Figure 17.

$T_{J(pk)}$ may be calculated from the data in Figure 22. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 21). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL CHARACTERISTICS

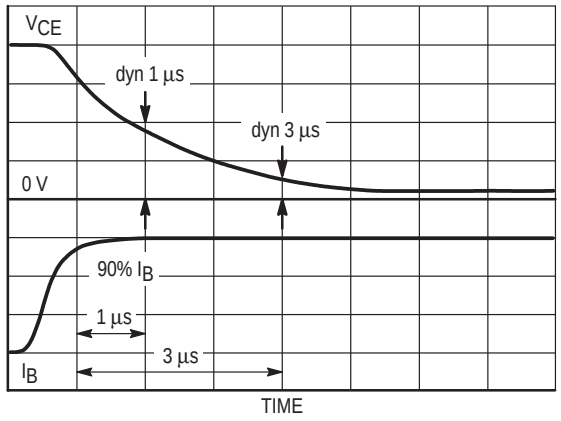


Figure 18. Dynamic Saturation Voltage

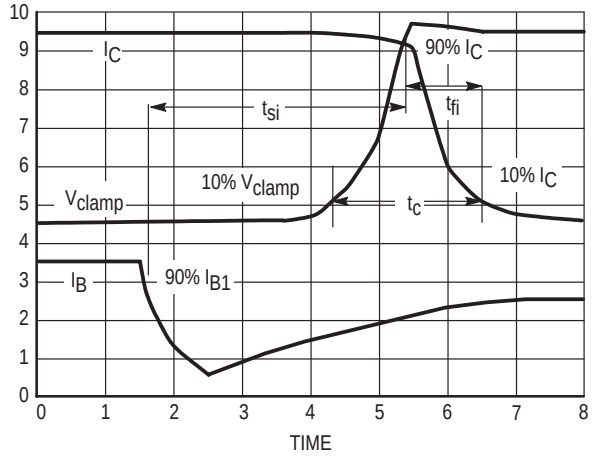


Figure 19. Inductive Switching Measurements

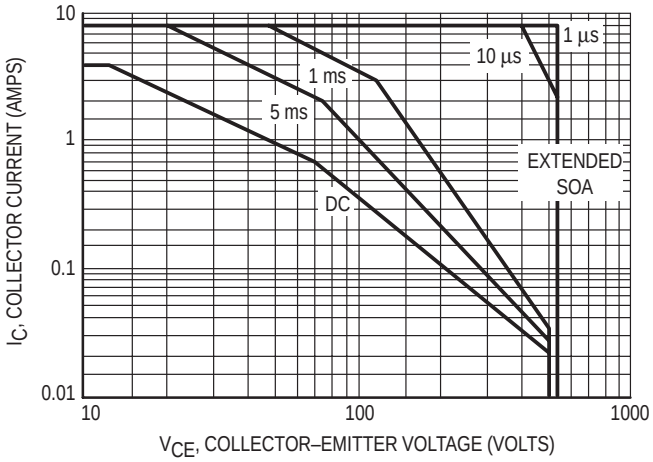


Figure 20. Forward Bias Safe Operating Area

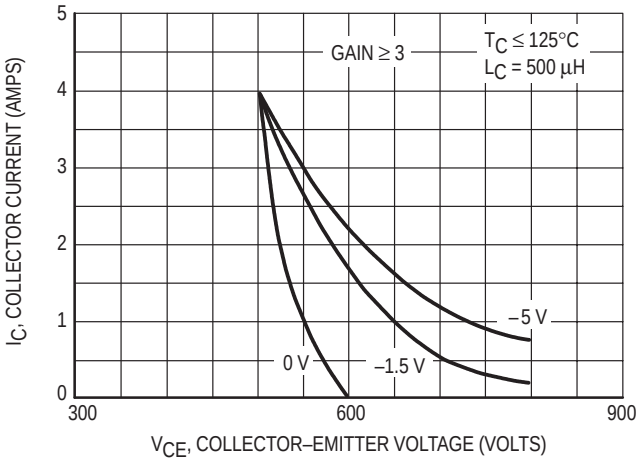
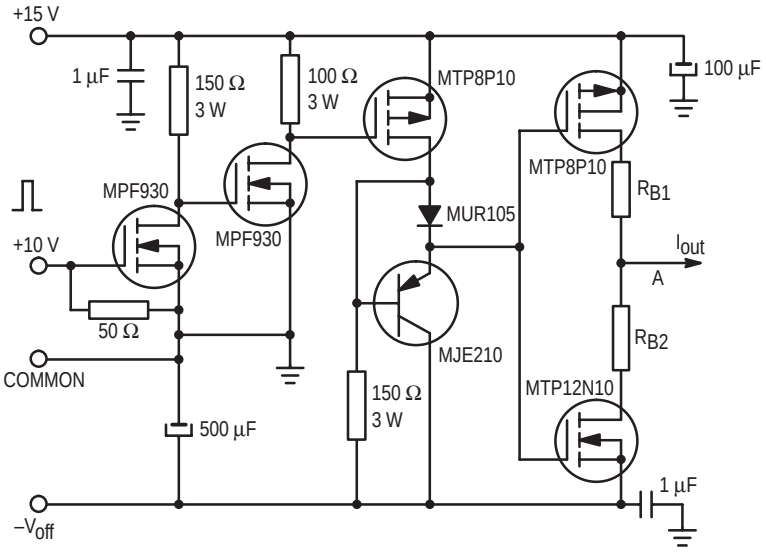
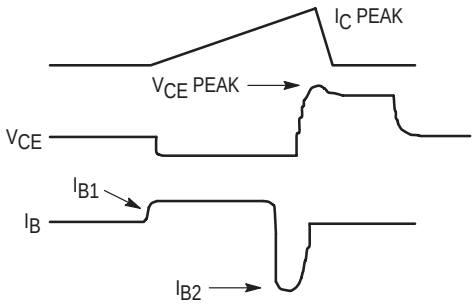


Figure 21. Reverse Bias Safe Operating Area

TYPICAL CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit





V(BR)CEO(sus)
L = 10 mH
R_{B2} = ∞
V_{CC} = 20 Volts
$I_{C(pk)}$ = 100 mA

Inductive Switching
L = 200 μH
R_{B2} = 0
V_{CC} = 15 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 500 μH
R_{B2} = 0
V_{CC} = 15 Volts
R_{B1} selected for desired I_{B1}

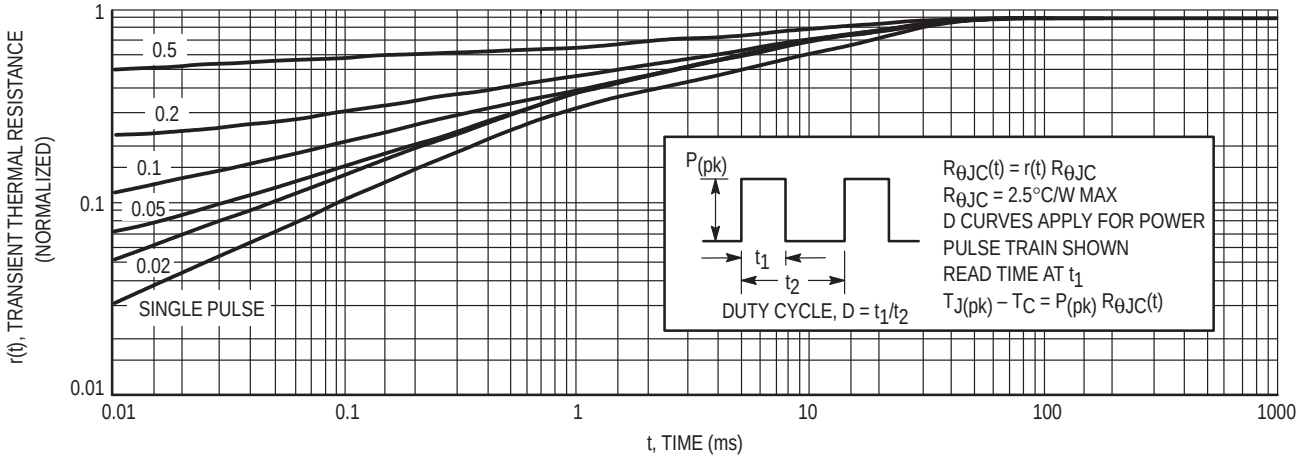


Figure 22. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUH50

BUH51

Advance Information

SWITCHMODE NPN Silicon Planar Power Transistor

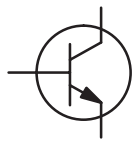
POWER TRANSISTOR
3 AMPERES
800 VOLTS
50 WATTS

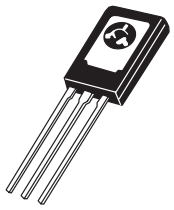
The BUH51 has an application specific state–of–art die designed for use in 50 Watts Halogen electronic transformers.

This power transistor is specifically designed to sustain the large inrush current during either the start–up conditions or under a short circuit across the load.

This High voltage/High speed product exhibits the following main features:

- Improved Efficiency Due to the Low Base Drive Requirements:
  — High and Flat DC Current Gain h_{FE}
  — Fast Switching
- Robustness Thanks to the Technology Developed to Manufacture this Device
- Motorola "6 SIGMA" Philosophy Providing Tight and Reproducible Parametric Distributions





CASE 77–07
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	500	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	800	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	800	Vdc
Emitter–Base Voltage	V_{EBO}	10	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	3 8	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	50 0.4	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 2.5 100	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	500	550		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	800	950		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	10	12.5		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 1000	μAdc
Collector Base Current (V_{CB} = Rated V_{CBO}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CBO}			100 1000	μAdc
Emitter–Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C	$V_{BE(sat)}$		0.92 0.8	1.1	Vdc
Collector–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.3 0.32	0.5 0.6	Vdc
DC Current Gain (I_C = 1 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	8 6	10 8		—
(I_C = 2 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		5 4	7.5 6.2		—
(I_C = 0.8 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		10 8	14 13		—
(I_C = 10 mAdc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		14 18	20 25		—
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 3 μs after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1 Adc, I_{B1} = 0.2 Adc, V_{CC} = 300 V; @ T_C = 25°C	$V_{CE(dsat)}$		1.7		V
	I_C = 1 Adc, I_{B1} = 0.2 Adc, V_{CC} = 300 V; @ T_C = 125°C			6		V
	I_C = 2 Adc, I_{B1} = 0.4 Adc, V_{CC} = 300 V; @ T_C = 25°C			5.1		V
	I_C = 2 Adc, I_{B1} = 0.4 Adc, V_{CC} = 300 V; @ T_C = 125°C			15		V
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 1 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T		23		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}		34	100	pF
Input Capacitance (V_{EB} = 8 Vdc, f = 1 MHz)		C_{ib}		200	500	pF

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Turn–on Time	I_C = 1 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		110 125	150	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		3.5 4.1	4	μs
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		700 1250	1000	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		1.75 2.1	2	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 1 Adc I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		200 320	300	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		3.4 4	3.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		350 640	500	ns
Fall Time	I_C = 2 Adc I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		140 300	200	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		2.3 2.8	2.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		400 725	600	ns

TYPICAL STATIC CHARACTERISTICS

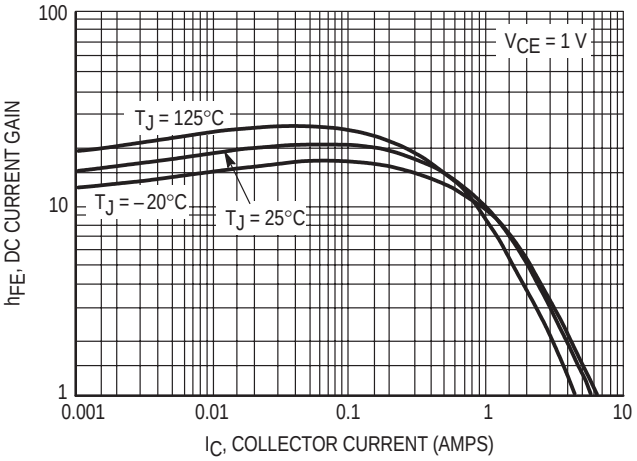


Figure 1. DC Current Gain @ 1 Volt

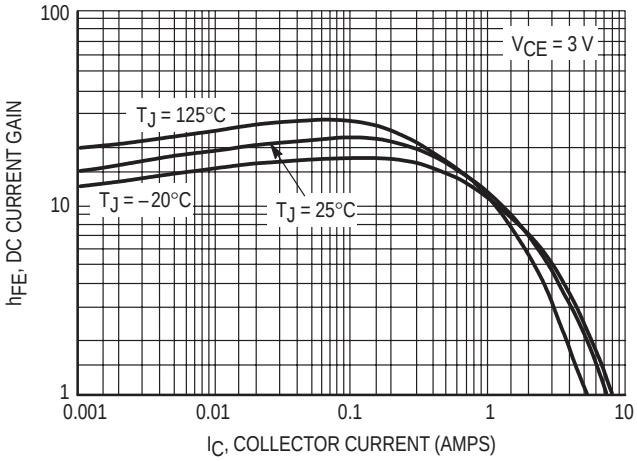


Figure 2. DC Current Gain @ 3 Volt

TYPICAL STATIC CHARACTERISTICS

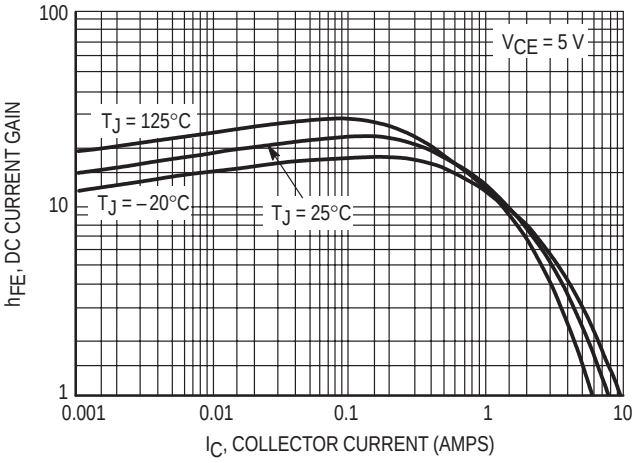


Figure 3. DC Current Gain @ 5 Volt

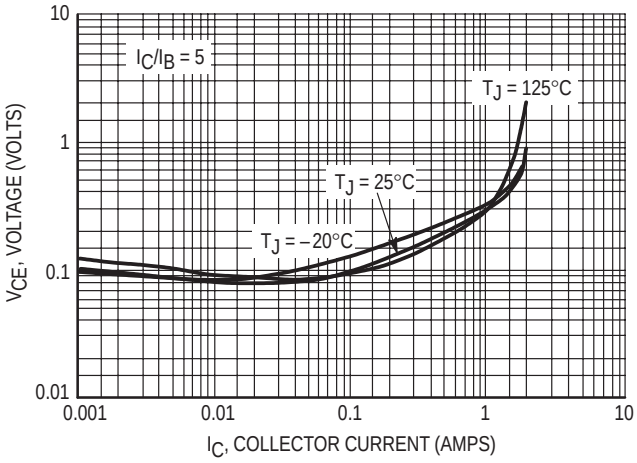


Figure 4. Collector–Emitter Saturation Voltage

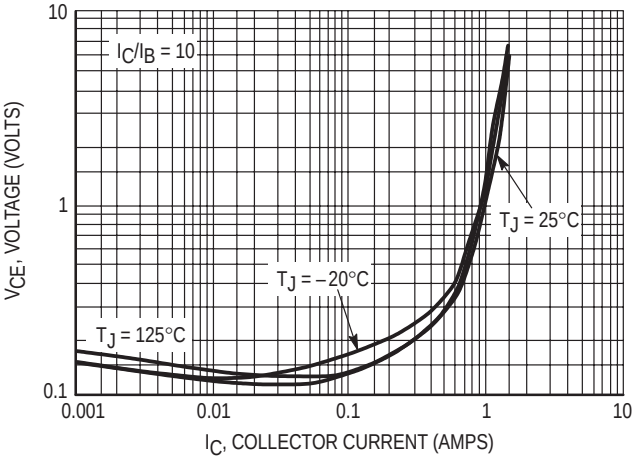


Figure 5. Collector–Emitter Saturation Voltage

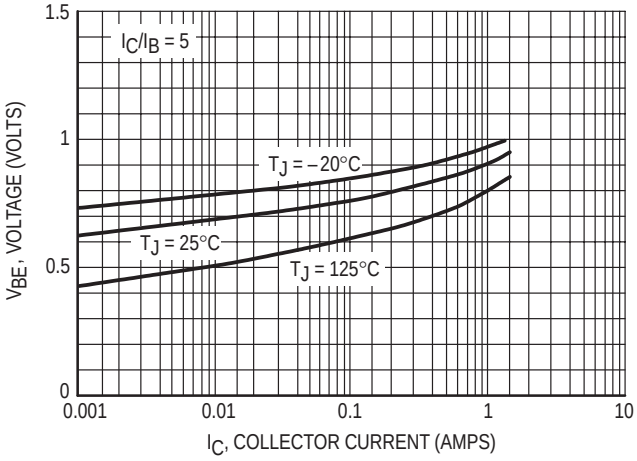


Figure 6. Base–Emitter Saturation Region

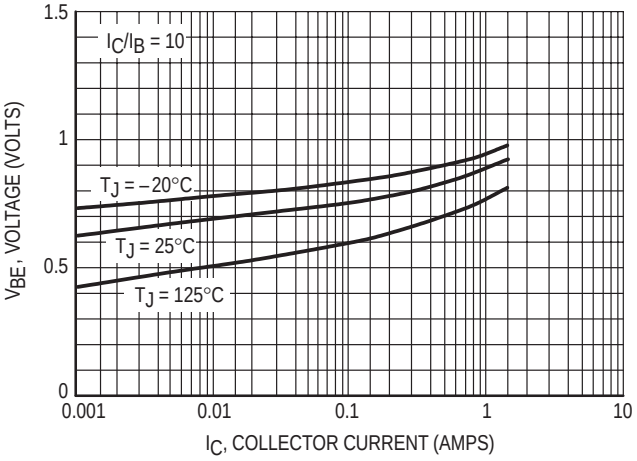


Figure 7. Base–Emitter Saturation Region

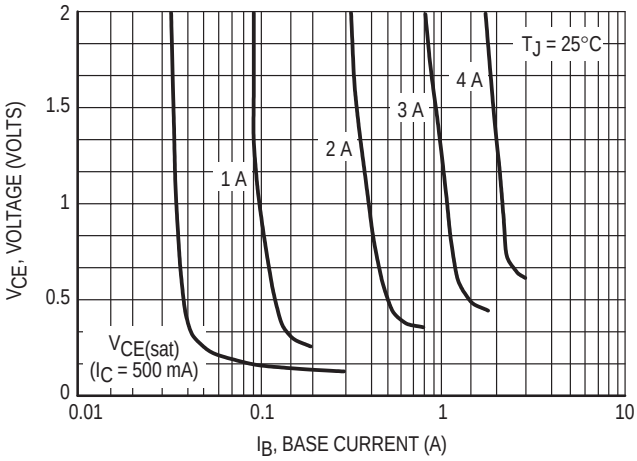


Figure 8. Collector Saturation Region

TYPICAL STATIC CHARACTERISTICS

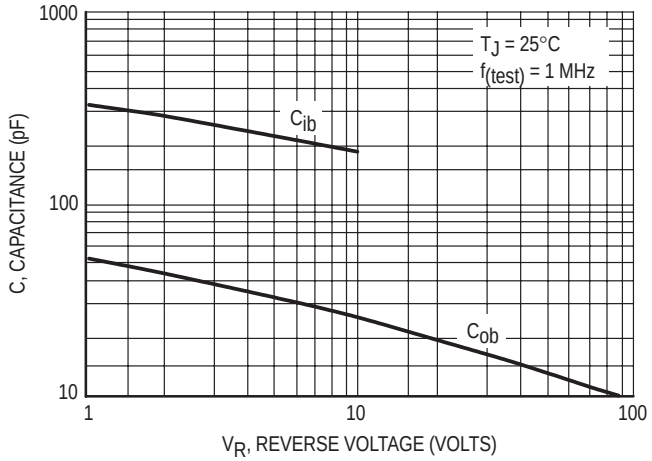


Figure 9. Capacitance

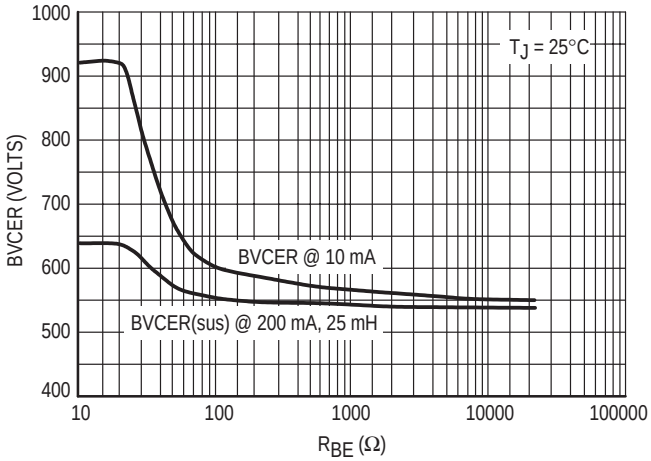


Figure 10. Resistive Breakdown

TYPICAL SWITCHING CHARACTERISTICS

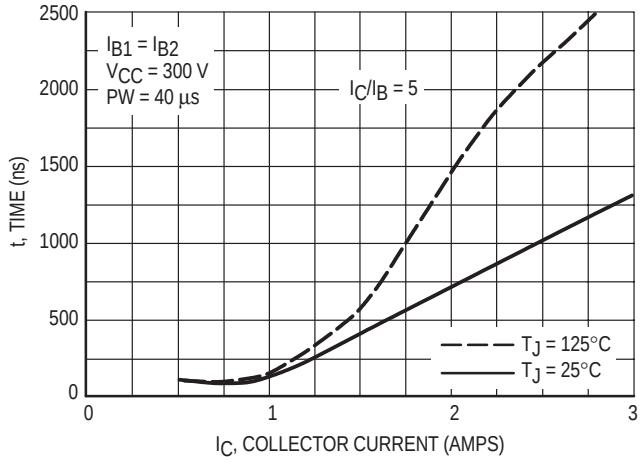


Figure 11. Resistive Switching, t_{on}

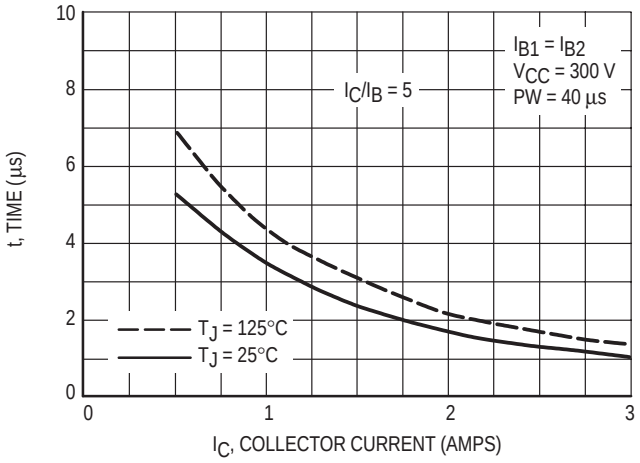


Figure 12. Resistive Switch Time, t_{off}

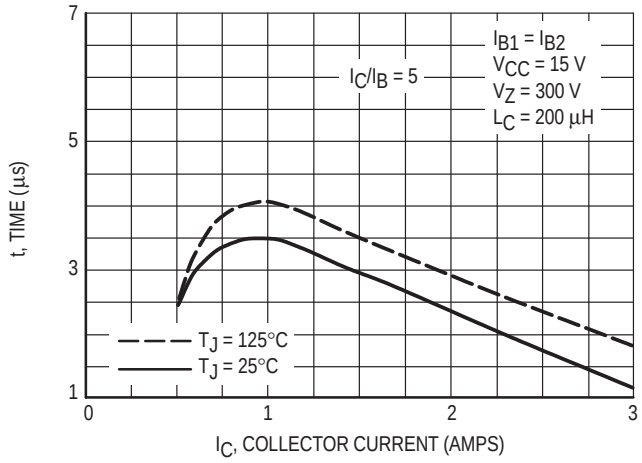


Figure 13. Inductive Storage Time, t_{si}

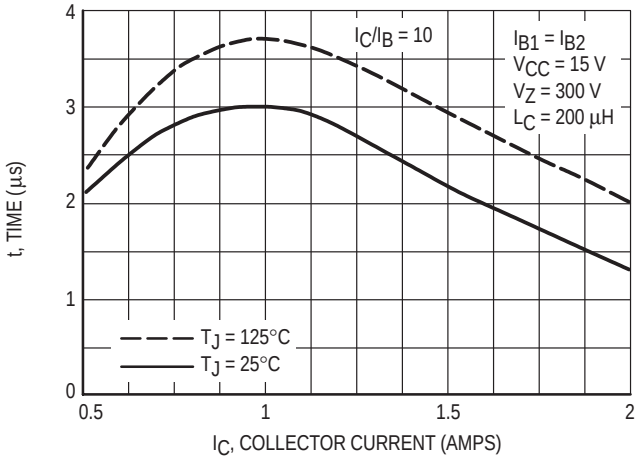


Figure 13 Bis. Inductive Storage Time, t_{si}

TYPICAL SWITCHING CHARACTERISTICS

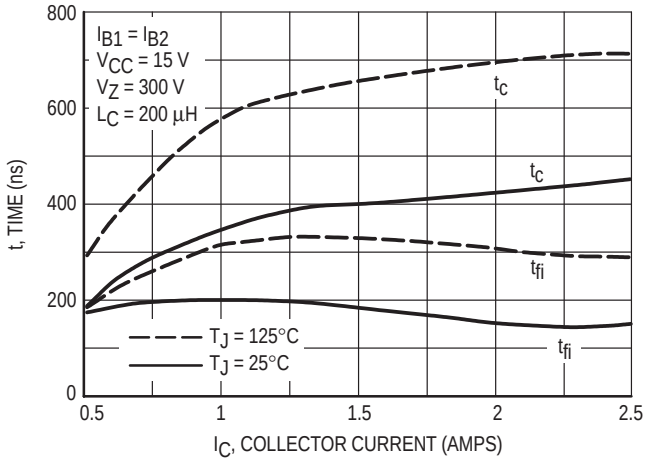


Figure 14. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 5

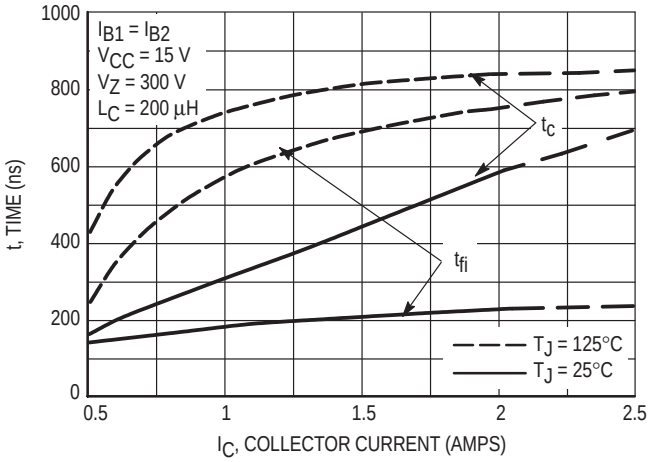


Figure 15. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 10

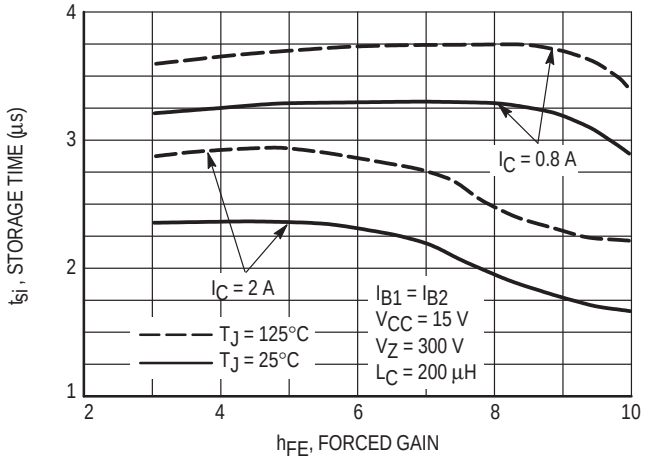


Figure 16. Inductive Storage Time

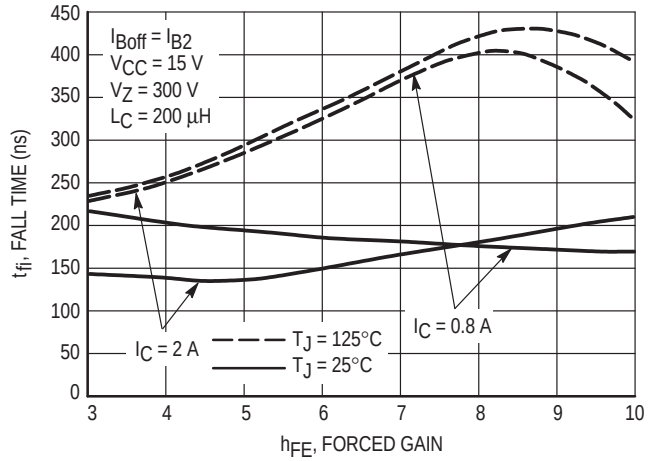


Figure 17. Inductive Fall Time

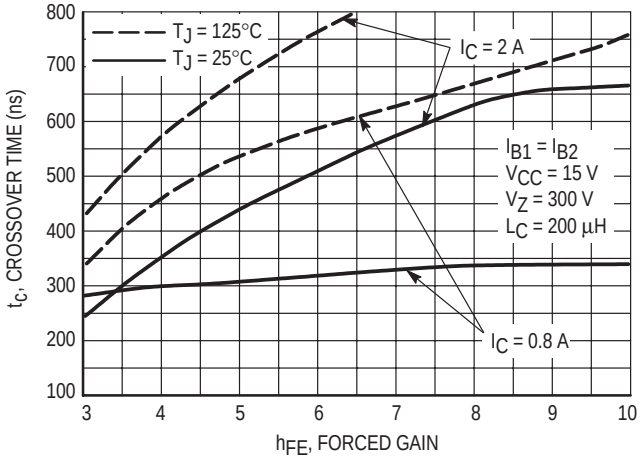


Figure 18. Inductive Crossover Time

TYPICAL SWITCHING CHARACTERISTICS

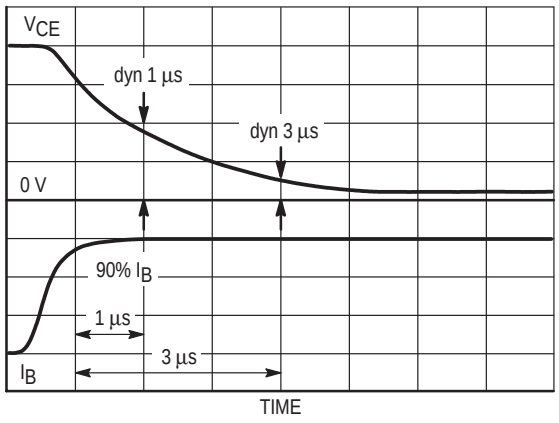


Figure 19. Dynamic Saturation Voltage Measurements

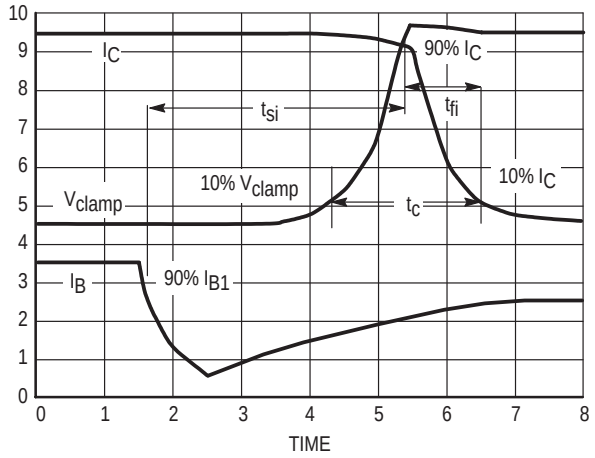
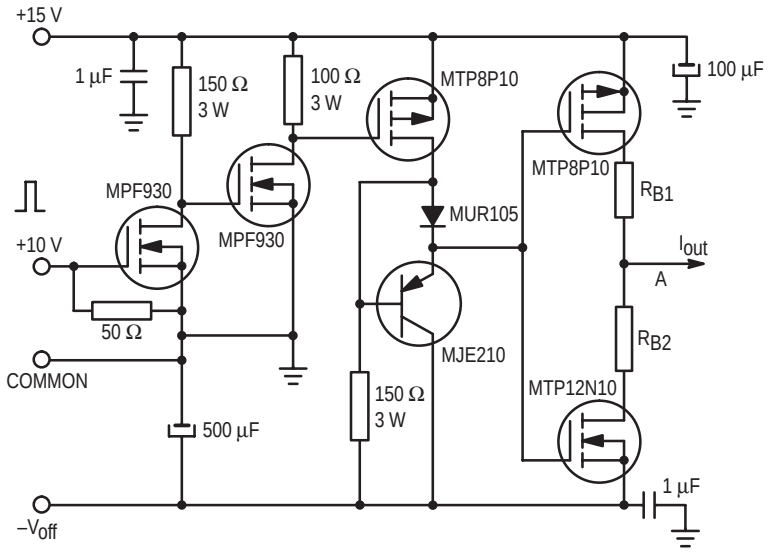
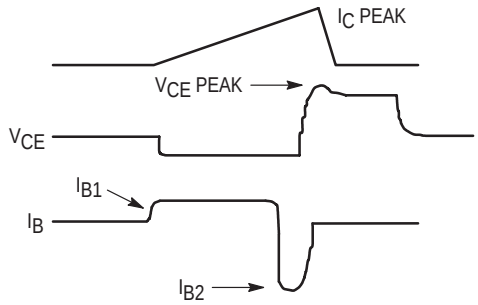


Figure 20. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL THERMAL RESPONSE

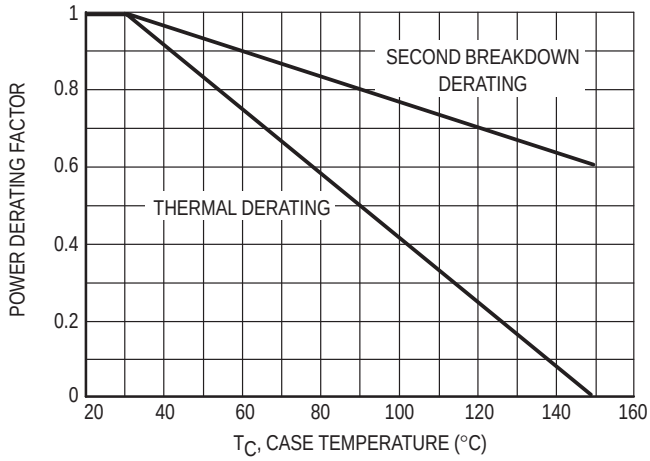


Figure 21. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 22 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 22 may be found at any case temperature by using the appropriate curve on Figure 21.

$T_{J(pk)}$ may be calculated from the data in Figure 24. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 23). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

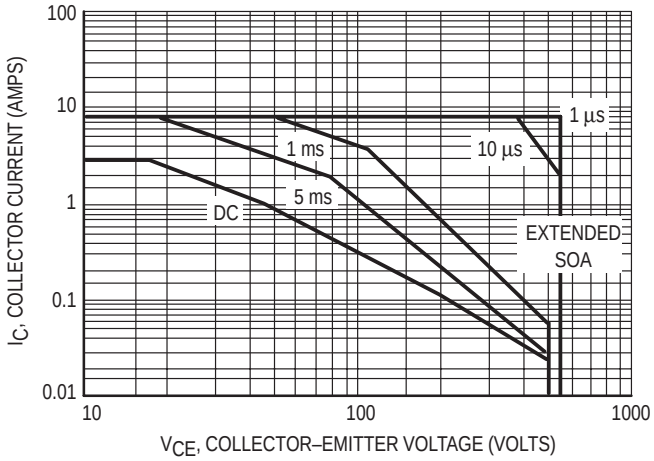


Figure 22. Forward Bias Safe Operating Area

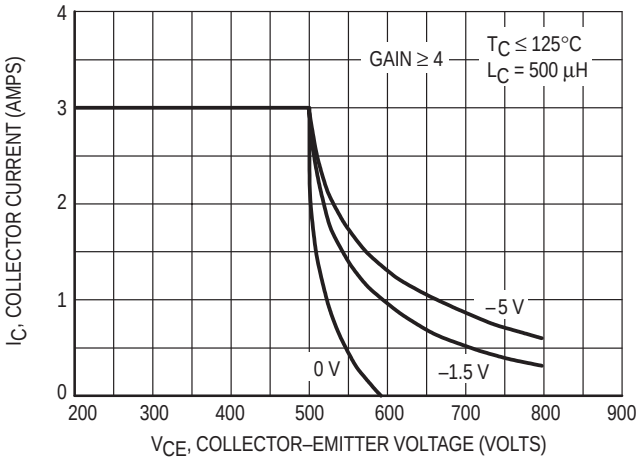


Figure 23. Reverse Bias Safe Operating Area

TYPICAL THERMAL RESPONSE

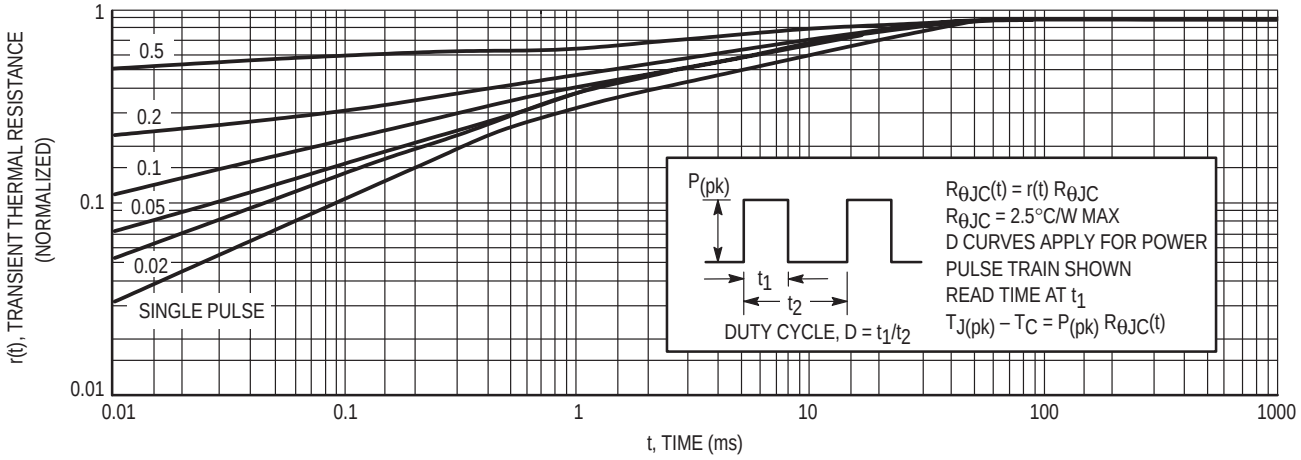


Figure 24. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUH51

BUH100

Designer's™ Data Sheet

SWITCHMODE NPN Silicon Planar Power Transistor

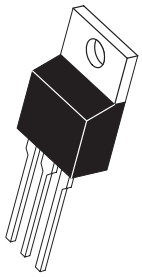
POWER TRANSISTOR
10 AMPERES
700 VOLTS
100 WATTS

The BUH100 has an application specific state–of–art die designed for use in 100 Watts Halogen electronic transformers.

This power transistor is specifically designed to sustain the large inrush current during either the start–up conditions or under a short circuit across the load.

This High voltage/High speed product exhibits the following main features:

- Improved Efficiency Due to the Low Base Drive Requirements:
  — High and Flat DC Current Gain h_{FE}
  — Fast Switching
- Robustness Thanks to the Technology Developed to Manufacture this Device
- Motorola "6 SIGMA" Philosophy Provides Tight and Reproducible Parametric Distributions



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter–Base Voltage	V_{EBO}	10	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 20	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4 10	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	100 0.8	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.25 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	400	460		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	700	860		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	10	12.5		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 1000	μAdc
Collector Base Current (V_{CB} = Rated V_{CBO}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CBO}			100 1000	μAdc
Emitter–Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc)	@ T_C = 25°C	$V_{BE(sat)}$		1	1.1	Vdc
Collector–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.37 0.37	0.6 0.6	Vdc
(I_C = 7 Adc, I_B = 1.5 Adc)	@ T_C = 25°C @ T_C = 125°C			0.5 0.6	0.75 1.5	Vdc
DC Current Gain (I_C = 1 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	15 16	24 28		—
(I_C = 5 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		10 10	15 14.5		—
(I_C = 7 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		8 7	12 10.5		—
(I_C = 10 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		6 4	9.5 8		—
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 3 μs after rising I_{B1} reaches 90% of final I_{B1} (See Figure 19)	I_C = 5 Adc, I_{B1} = 1 Adc, V_{CC} = 300 V	@ T_C = 25°C	$V_{CE(dsat)}$		1.1		V
		@ T_C = 125°C			2.1		V
	I_C = 7.5 Adc, I_{B1} = 1.5 Adc, V_{CC} = 300 V	@ T_C = 25°C			1.7		V
		@ T_C = 125°C			5		V
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 1 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T		23		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}		100	150	pF
Input Capacitance (V_{EB} = 8 Vdc, f = 1 MHz)		C_{ib}		1300	1750	pF

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Turn–on Time	I_C = 1 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		130 140	200	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		6.8 8.5	8	μs
Turn–on Time	I_C = 1 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.4 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		140 150	200	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		3.4 4.3	4	μs
Turn–on Time	I_C = 5 Adc, I_{B1} = 1 Adc I_{B2} = 1 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		250 800	500	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		2.9 3.6	3.5	μs
Turn–on Time	I_C = 7.5 Adc, I_{B1} = 1.5 Adc I_{B2} = 1.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		500 900	700	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		2.1 2.5	2.5	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 1 Adc I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		150 180	250	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		5.1 5.8	6	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		230 300	325	ns
Fall Time	I_C = 1 Adc I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		150 170	250	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		2.5 2.8	3	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		260 300	350	ns
Fall Time	I_C = 5 Adc I_{B1} = 1 Adc I_{B2} = 1 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		100 140	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		2.9 4.6	3.5	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		220 450	300	ns
Fall Time	I_C = 7.5 Adc I_{B1} = 1.5 Adc I_{B2} = 1.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		100 150	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		2 2.5	2.5	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		250 475	350	ns

TYPICAL STATIC CHARACTERISTICS

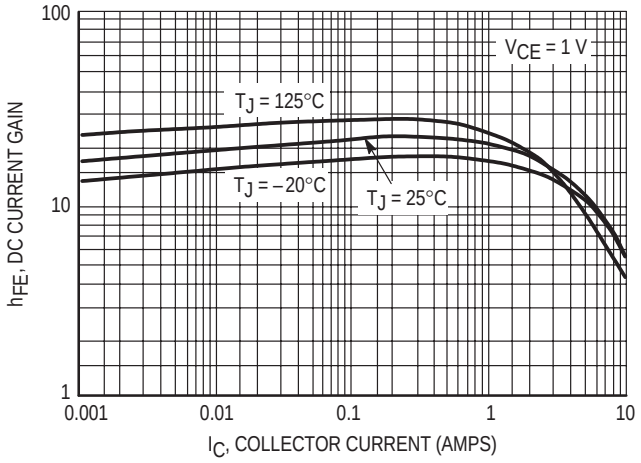


Figure 1. DC Current Gain @ 1 Volt

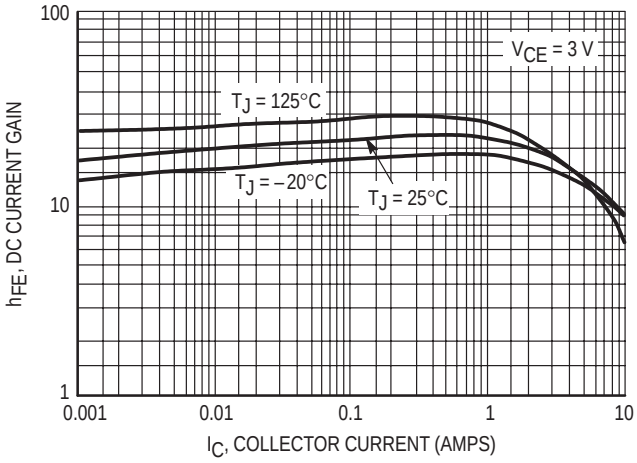


Figure 2. DC Current Gain @ 3 Volt

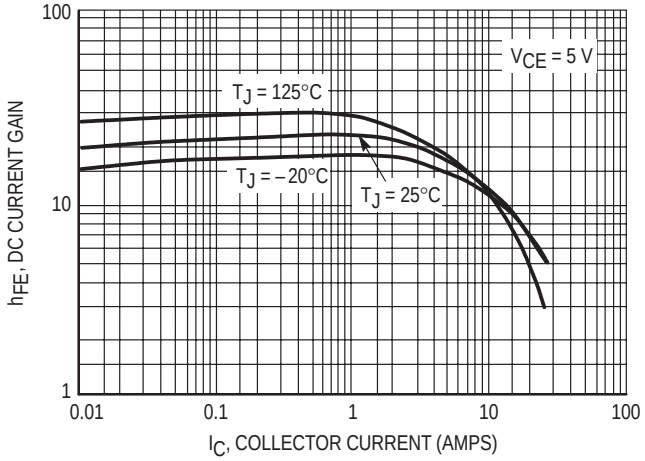


Figure 3. DC Current Gain @ 5 Volt

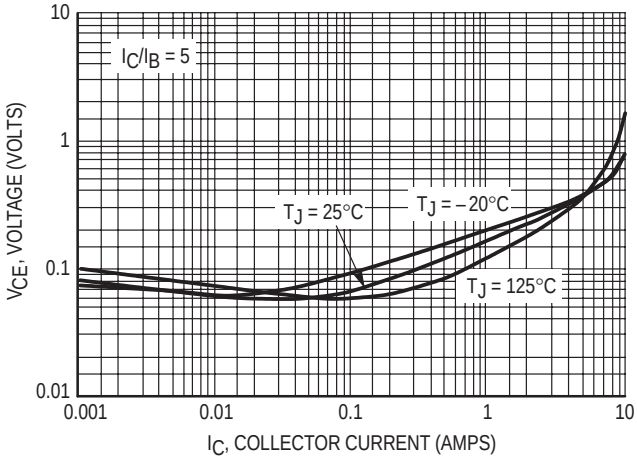


Figure 4. Collector–Emitter Saturation Voltage

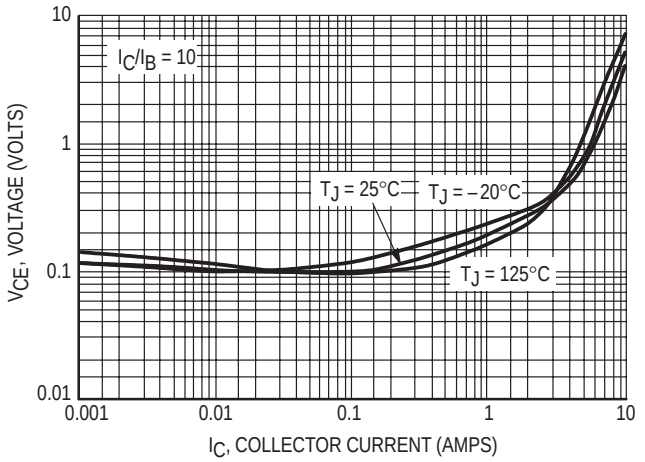


Figure 5. Collector–Emitter Saturation Voltage

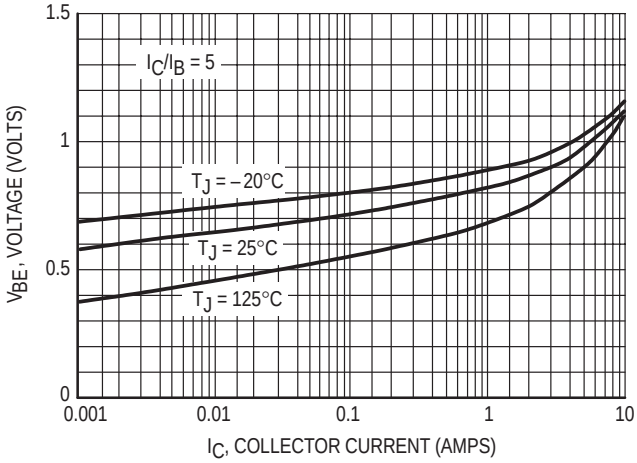


Figure 6. Base–Emitter Saturation Region

TYPICAL STATIC CHARACTERISTICS

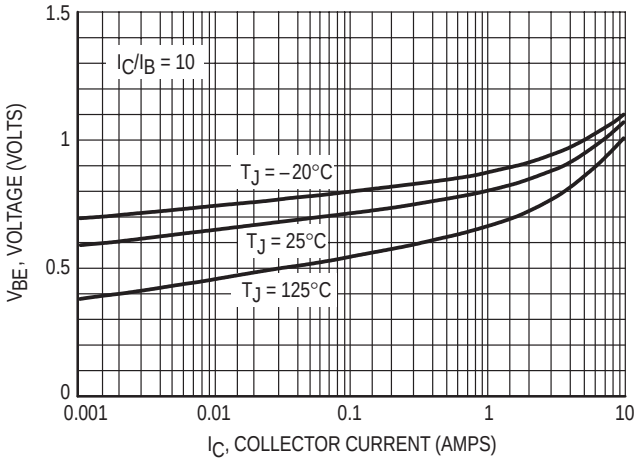


Figure 7. Base–Emitter Saturation Region

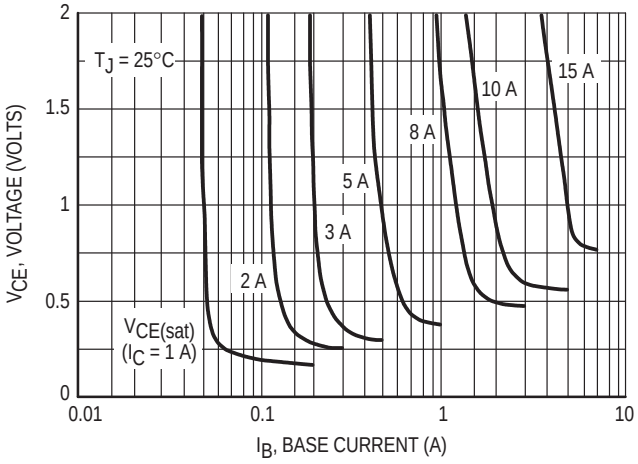


Figure 8. Collector Saturation Region

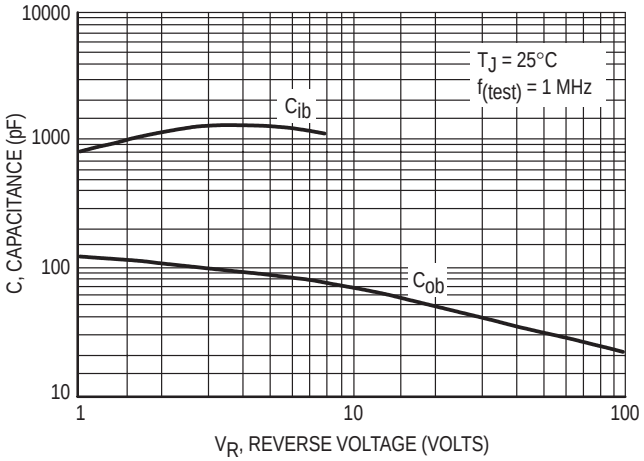


Figure 9. Capacitance

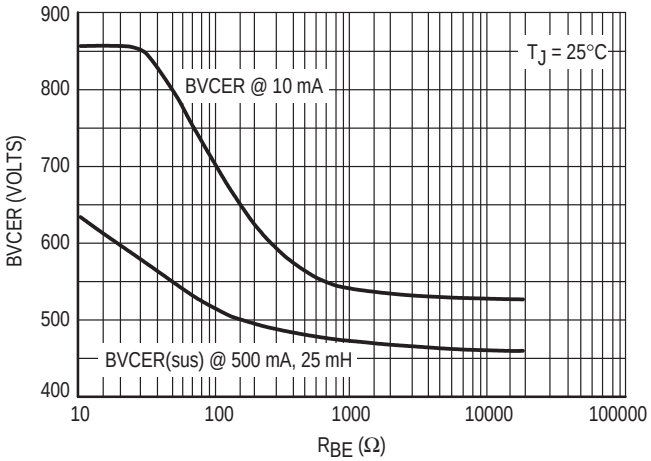


Figure 10. Resistive Breakdown

TYPICAL SWITCHING CHARACTERISTICS

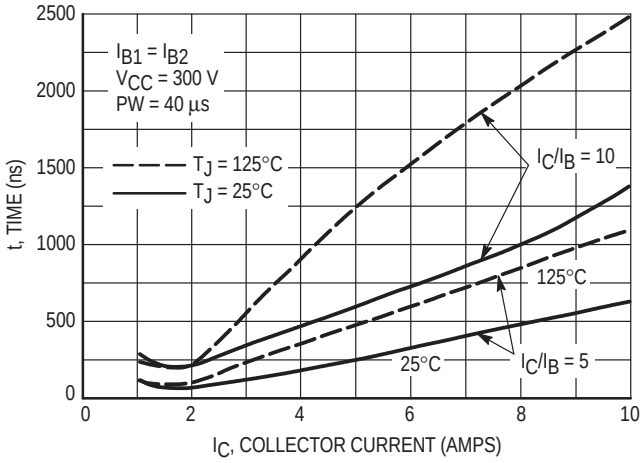


Figure 11. Resistive Switching Time, t_{on}

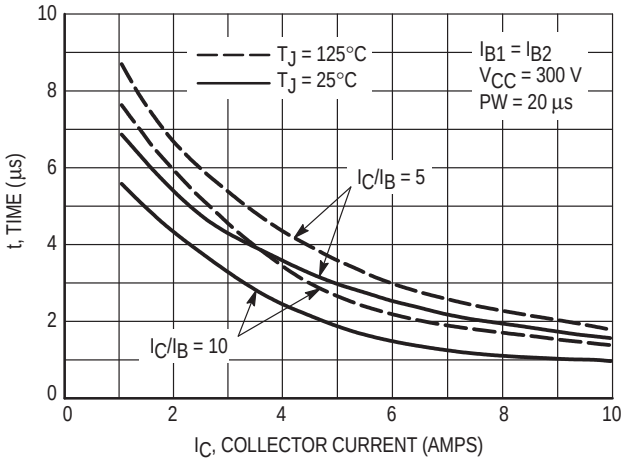


Figure 12. Resistive Switch Time, t_{off}

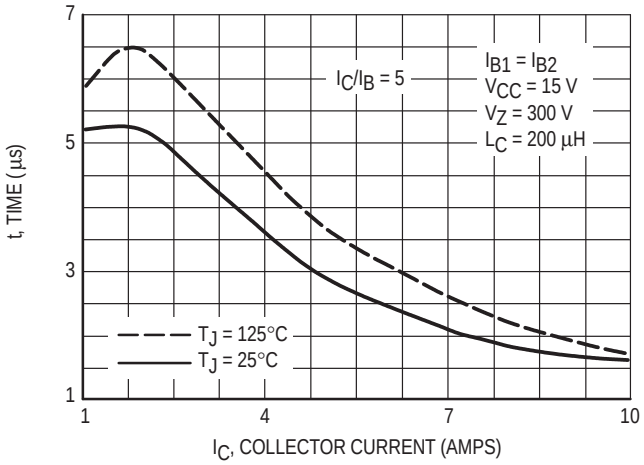


Figure 13. Inductive Storage Time, t_{si}

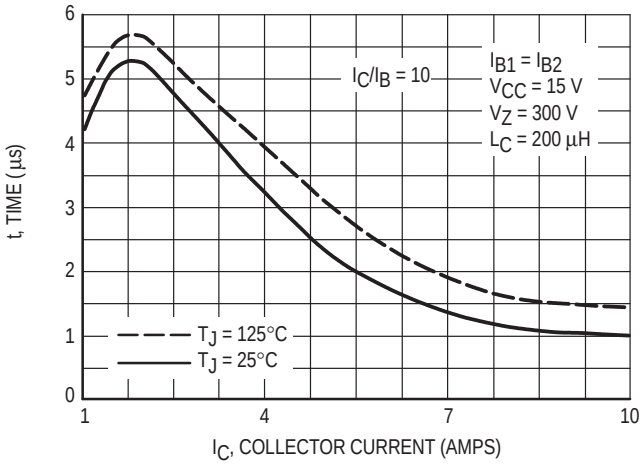


Figure 13 Bis. Inductive Storage Time, t_{si}

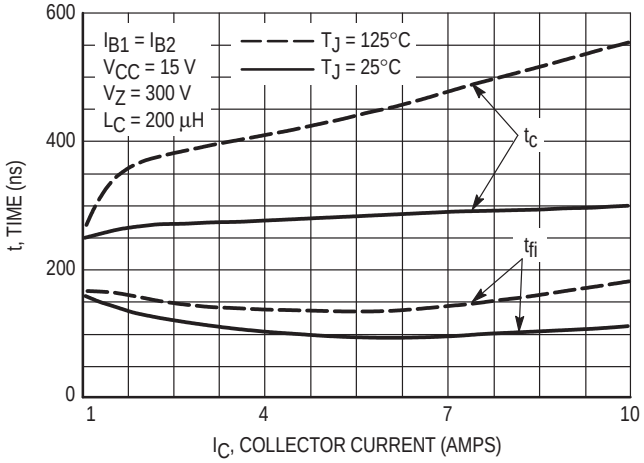


Figure 14. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 5

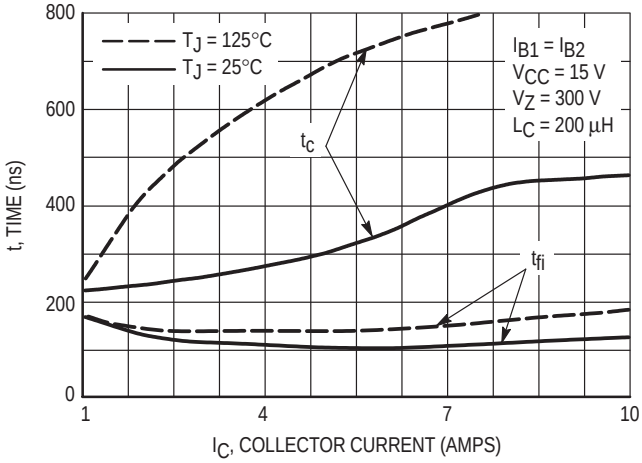


Figure 15. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS

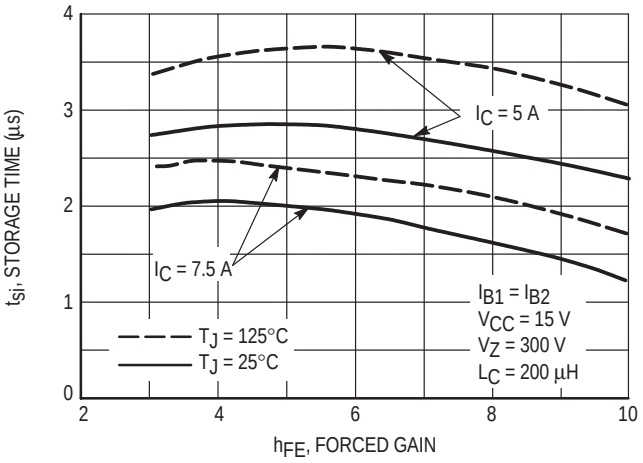


Figure 16. Inductive Storage Time

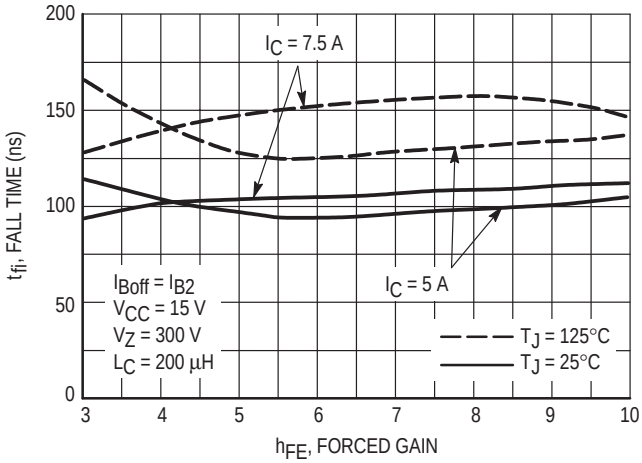


Figure 17. Inductive Fall Time

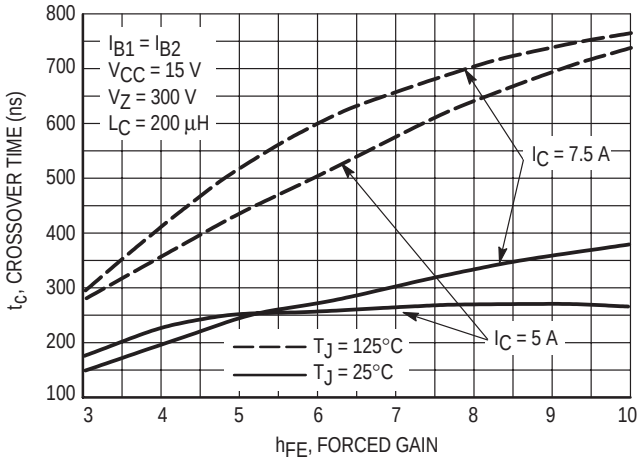


Figure 18. Inductive Crossover Time, t_c

TYPICAL SWITCHING CHARACTERISTICS

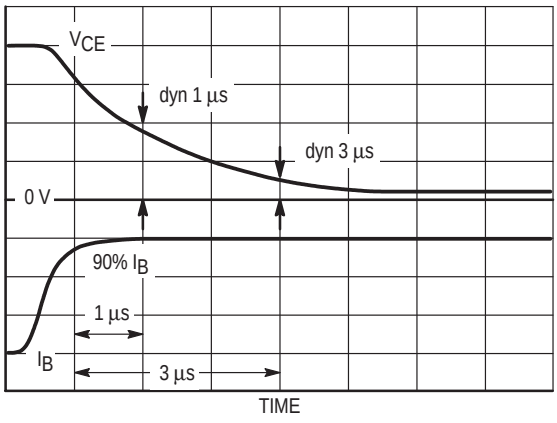


Figure 19. Dynamic Saturation Voltage Measurements

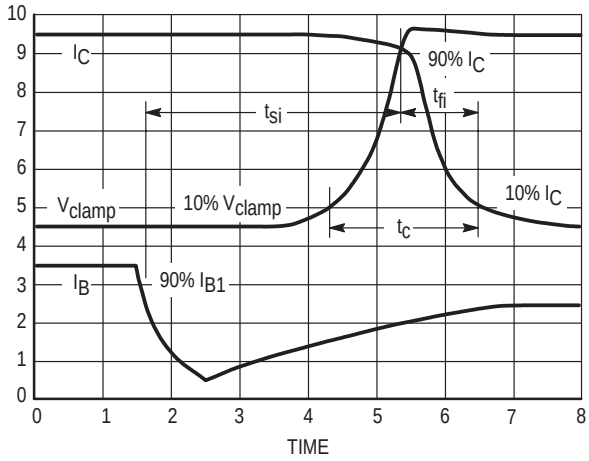
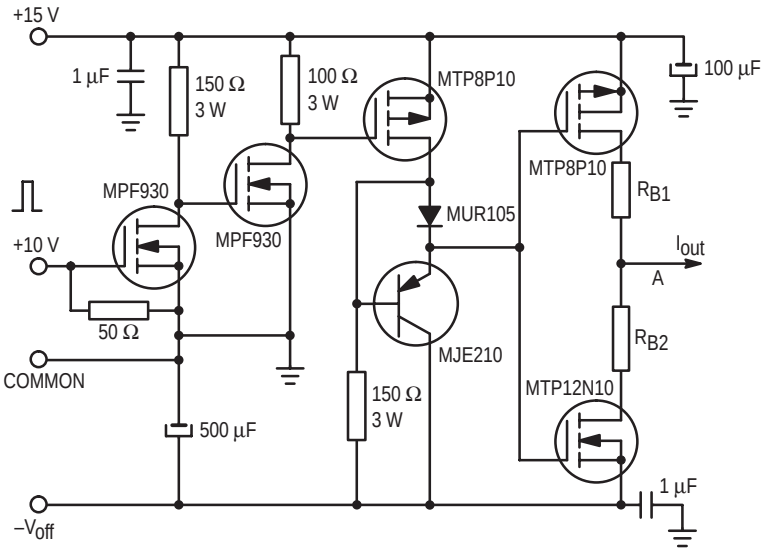
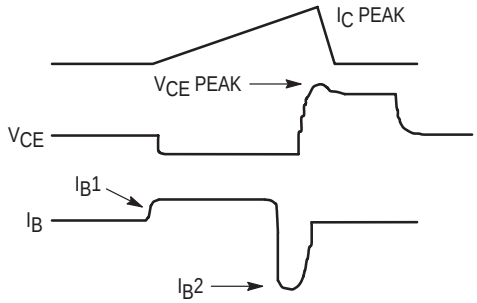


Figure 20. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit





V(BR)CEO(sus)
L = 10 mH
R_{B2} = ∞
V_{CC} = 20 Volts
$I_{C(pk)}$ = 100 mA

Inductive Switching
L = 200 μH
R_{B2} = 0
V_{CC} = 15 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 500 μH
R_{B2} = 0
V_{CC} = 15 Volts
R_{B1} selected for desired I_{B1}

TYPICAL THERMAL RESPONSE

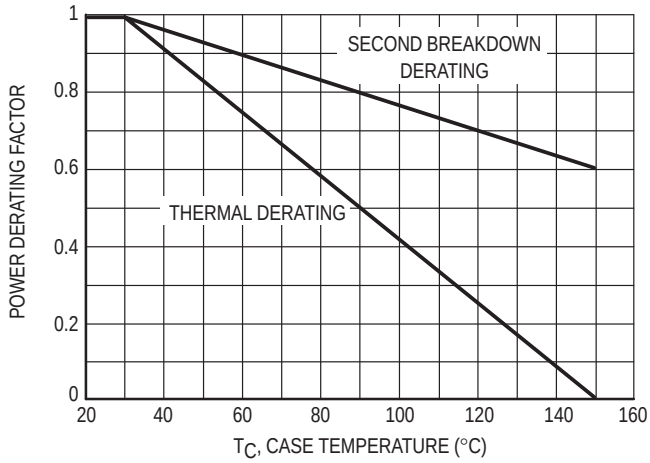


Figure 21. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 22 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 22 may be found at any case temperature by using the appropriate curve on Figure 21.

$T_{J(pk)}$ may be calculated from the data in Figure 24. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 23). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

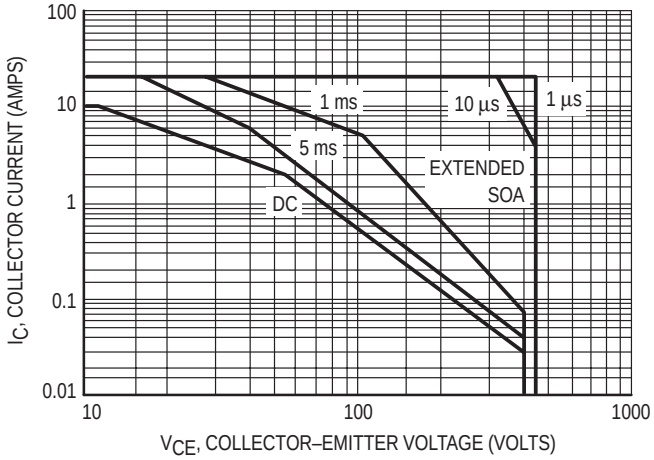


Figure 22. Forward Bias Safe Operating Area

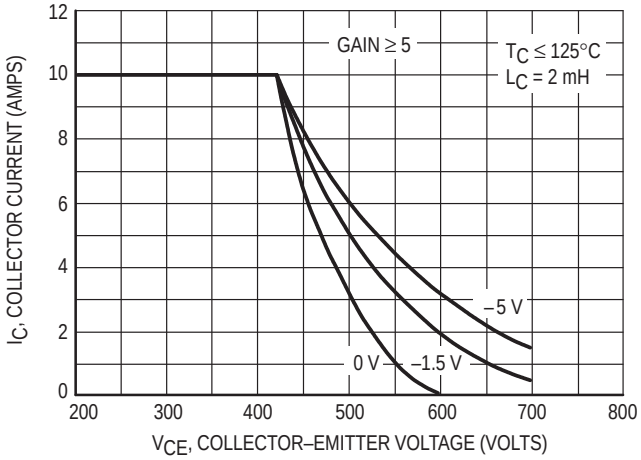


Figure 23. Reverse Bias Safe Operating Area

TYPICAL THERMAL RESPONSE

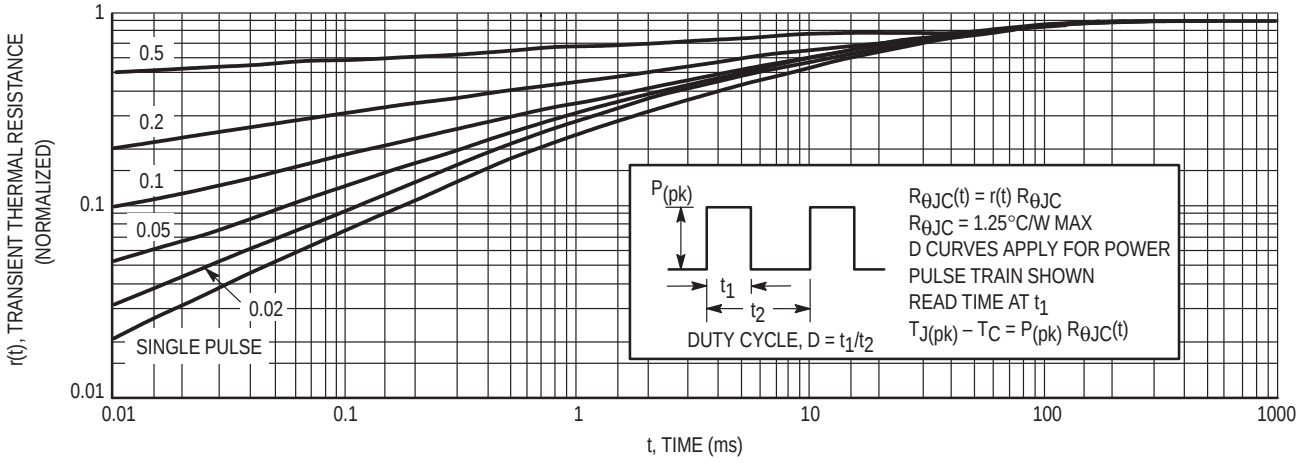


Figure 24. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUH100

BUH150

Designer's™ Data Sheet

SWITCHMODE NPN Silicon Planar Power Transistor

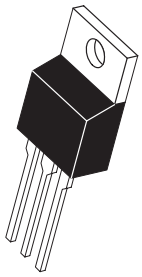
POWER TRANSISTOR
15 AMPERES
700 VOLTS
150 WATTS

The BUH150 has an application specific state–of–art die designed for use in 150 Watts Halogen electronic transformers.

This power transistor is specifically designed to sustain the large inrush current during either the start–up conditions or under a short circuit across the load.

This High voltage/High speed product exhibits the following main features:

- Improved Efficiency Due to the Low Base Drive Requirements:
  — High and Flat DC Current Gain h_{FE}
  — Fast Switching
- Robustness Thanks to the Technology Developed to Manufacture this Device
- Motorola "6 SIGMA" Philosophy Provides Tight and Reproducible Parametric Distributions



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter–Base Voltage	V_{EBO}	10	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 25	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	6 12	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	150 1.2	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 0.85 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	400	460		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	700	860		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	10	12.3		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 1000	μAdc
Collector Base Current (V_{CB} = Rated V_{CBO}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CBO}			100 1000	μAdc
Emitter–Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2 Adc)		$V_{BE(sat)}$		1	1.25	Vdc
Collector–Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.16 0.15	0.4 0.4	Vdc
(I_C = 10 Adc, I_B = 2 Adc)	@ T_C = 25°C			0.45	1	Vdc
(I_C = 20 Adc, I_B = 4 Adc)	@ T_C = 25°C			2	5	Vdc
DC Current Gain (I_C = 20 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	4 2.5	7 4.5		—
(I_C = 10 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		8 6	12 10		—
(I_C = 2 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		12 14	20 22		—
(I_C = 100 mAdc, V_{CE} = 5 Vdc)	@ T_C = 25°C		10	20		—
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 3 μs after rising I_{B1} reaches 90% of final I_{B1} (see Figure 19)	I_C = 5 Adc, I_{B1} = 1 Adc, V_{CC} = 300 V	@ T_C = 25°C	$V_{CE(dsat)}$		1.5		V
		@ T_C = 125°C			2.8		V
	I_C = 10 Adc, I_{B1} = 2 Adc, V_{CC} = 300 V	@ T_C = 25°C			2.4		V
		@ T_C = 125°C			5		V
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 1 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T		23		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}		100	150	pF
Input Capacitance (V_{EB} = 8 Vdc, f = 1 MHz)		C_{ib}		1300	1750	pF

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc V_{CC} = 300 Vdc	@ T_C = 25°C	t_{on}		200	300	ns
Storage Time		@ T_C = 25°C	t_s		5.3	6.5	μs
Fall Time		@ T_C = 25°C	t_f		240	350	ns
Turn–off Time		@ T_C = 25°C	t_{off}		5.6	7	μs
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc V_{CC} = 300 Vdc	@ T_C = 25°C	t_{on}		100	200	ns
Storage Time		@ T_C = 25°C	t_s		6.1	7.5	μs
Fall Time		@ T_C = 25°C	t_f		320	500	ns
Turn–off Time		@ T_C = 25°C	t_{off}		6.5	8	μs
Turn–on Time	I_C = 5 Adc, I_{B1} = 0.5 Adc I_{B2} = 0.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		450 800	650	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		2.5 3.9	3	μs
Turn–on Time	I_C = 10 Adc, I_{B1} = 2 Adc I_{B2} = 2 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		500 900	700	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		2.25 2.75	2.75	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 2 Adc I_{B1} = 0.2 Adc I_{B2} = 0.2 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		110 160	250	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		6.5 8	8	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		235 240	350	ns
Fall Time	I_C = 2 Adc I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		110 170	250	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		6 7.8	7.5	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		250 270	350	ns
Fall Time	I_C = 5 Adc I_{B1} = 0.5 Adc I_{B2} = 0.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		110 140	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		3.25 4.6	3.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		275 450	350	ns
Fall Time	I_C = 10 Adc I_{B1} = 2 Adc I_{B2} = 2 Adc	@ T_C = 25°C @ T_C = 125°C	t_{fi}		110 160	175	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_{si}		2.3 2.8	2.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		250 475	350	ns

TYPICAL STATIC CHARACTERISTICS

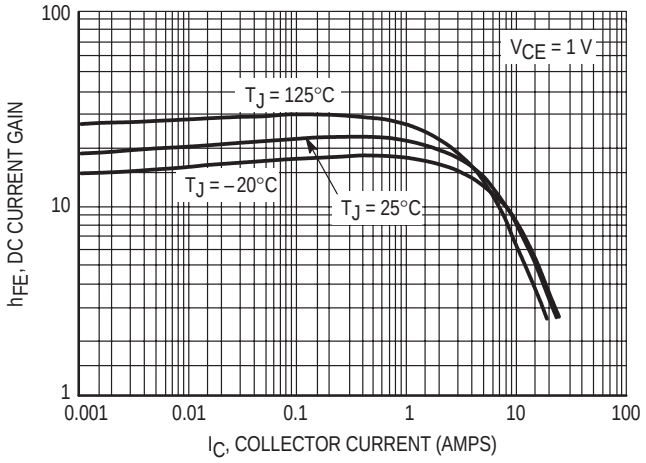


Figure 1. DC Current Gain @ 1 Volt

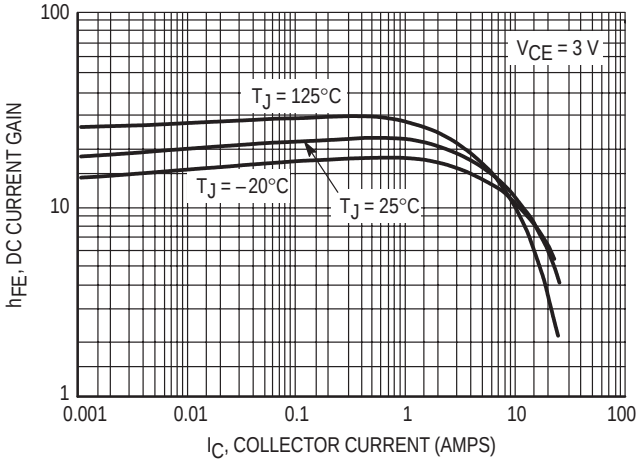


Figure 2. DC Current Gain @ 3 Volt

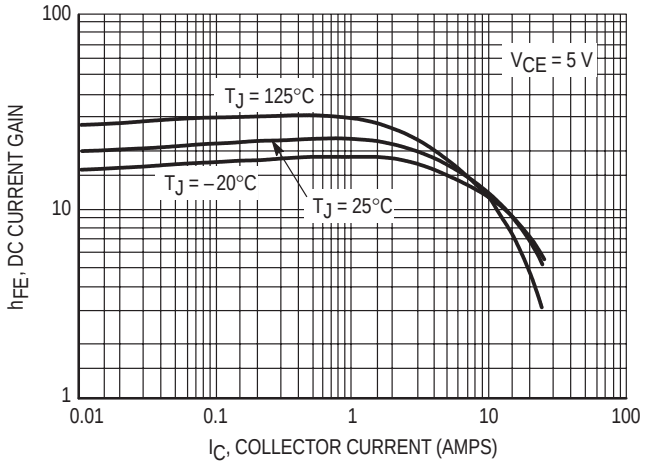


Figure 3. DC Current Gain @ 5 Volt

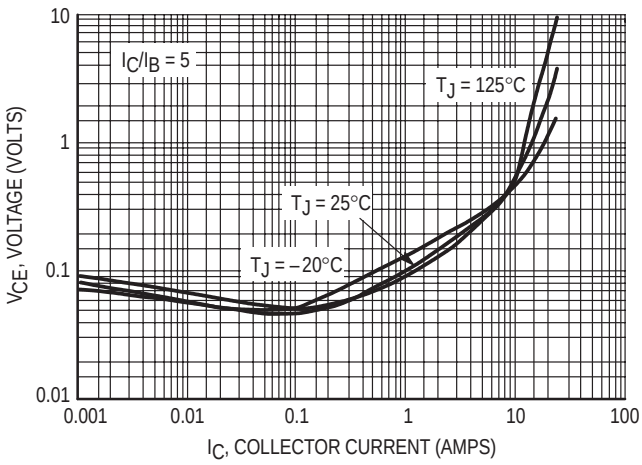


Figure 4. Collector–Emitter Saturation Voltage

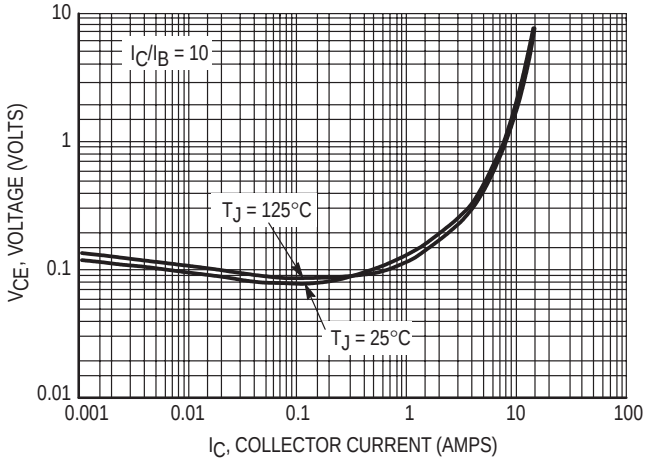


Figure 5. Collector–Emitter Saturation Voltage

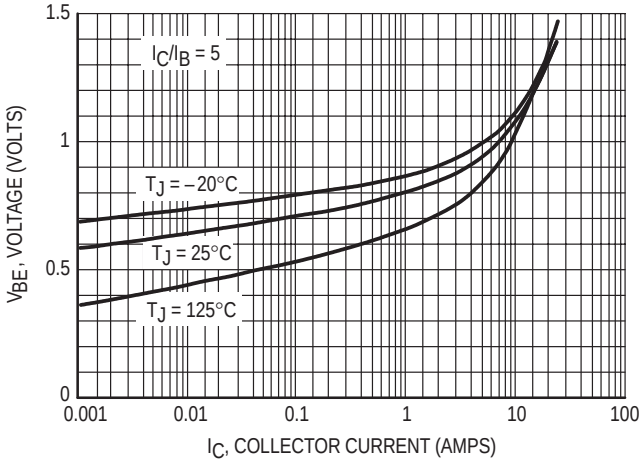


Figure 6. Base–Emitter Saturation Region

TYPICAL STATIC CHARACTERISTICS

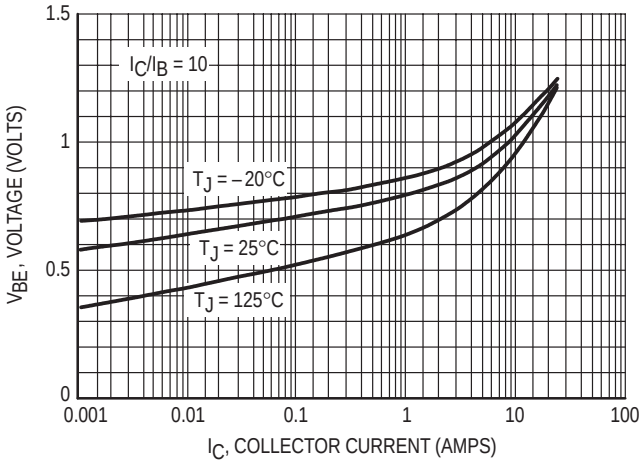


Figure 7. Base–Emitter Saturation Region

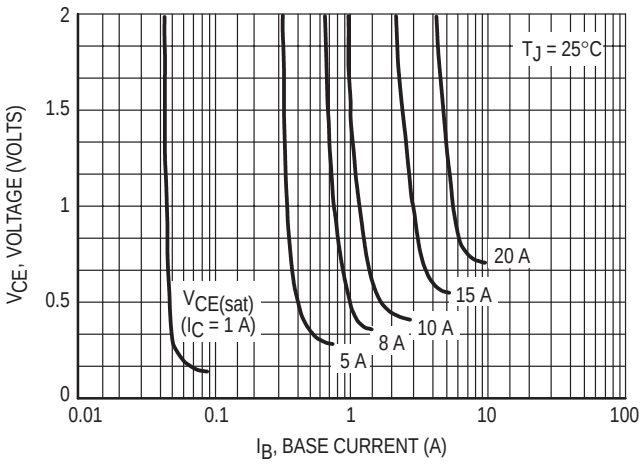


Figure 8. Collector Saturation Region

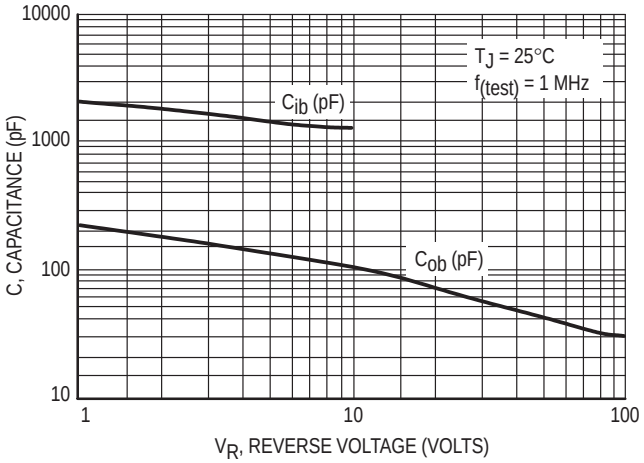


Figure 9. Capacitance

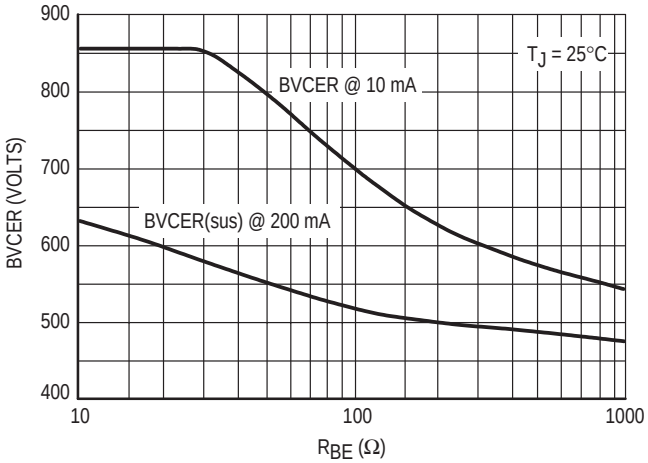


Figure 10. Resistive Breakdown

TYPICAL SWITCHING CHARACTERISTICS

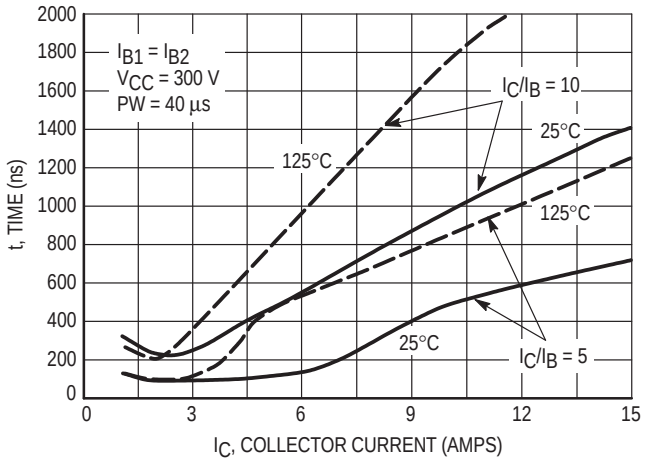


Figure 11. Resistive Switching, t_{on}

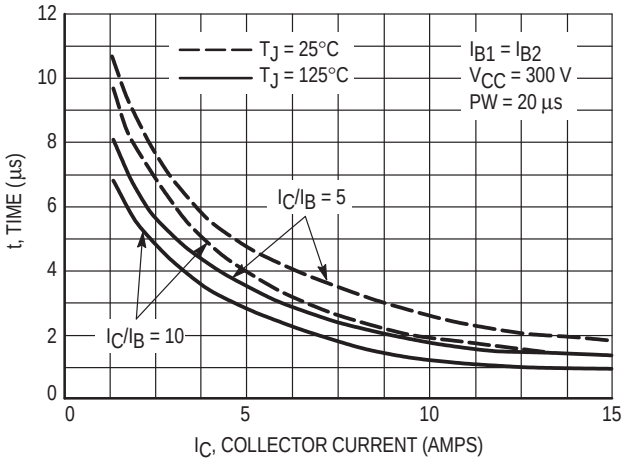


Figure 12. Resistive Switch Time, t_{off}

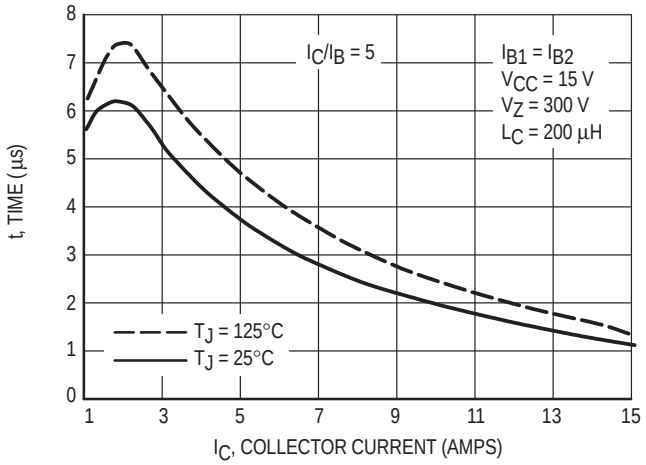


Figure 13. Inductive Storage Time, t_{si}

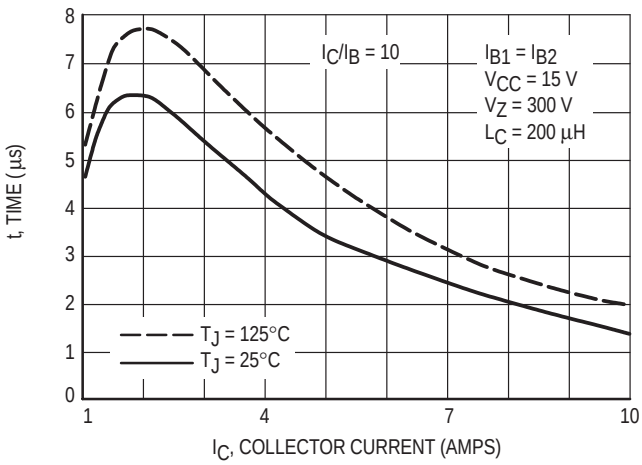


Figure 13 Bis. Inductive Storage Time, t_{si}

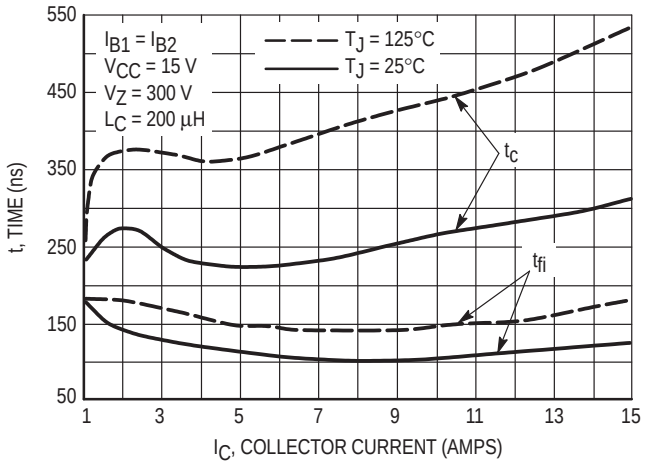


Figure 14. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 5

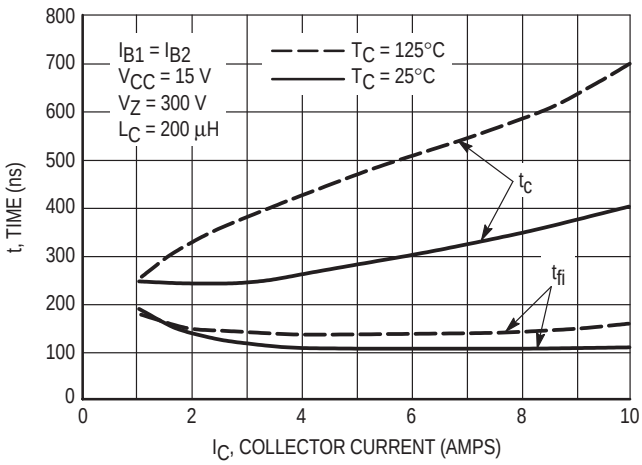


Figure 15. Inductive Storage Time, t_c & t_{fi} @ I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS

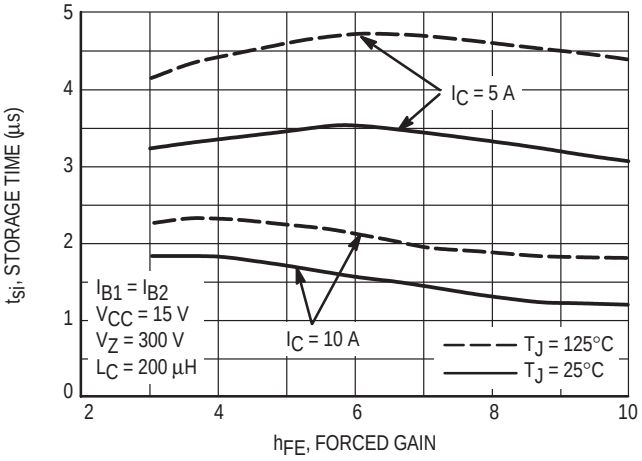


Figure 16. Inductive Storage Time

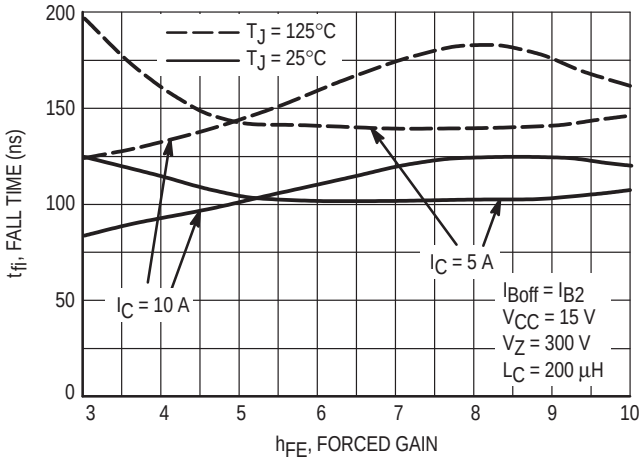


Figure 17. Inductive Fall Time

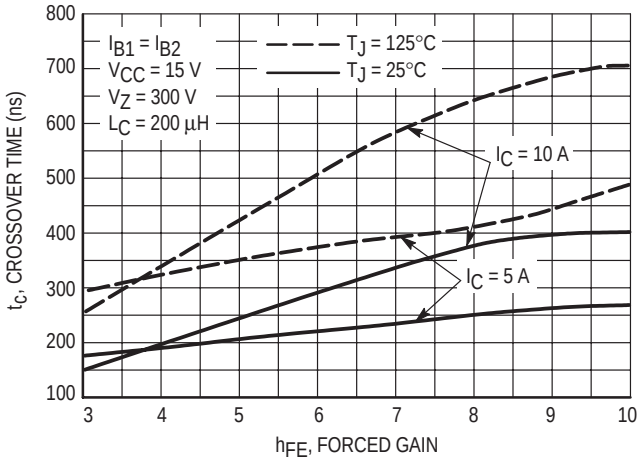


Figure 18. Inductive Crossover Time

TYPICAL SWITCHING CHARACTERISTICS

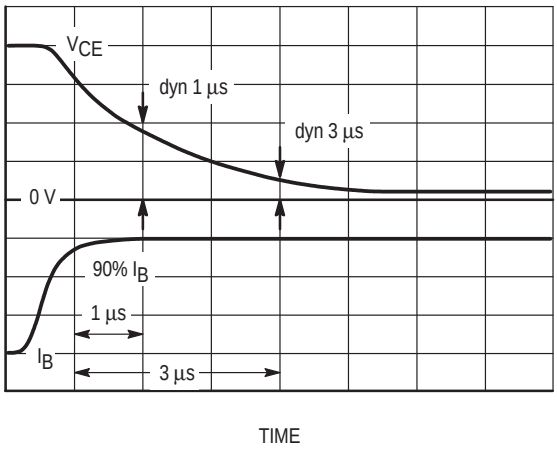


Figure 19. Dynamic Saturation Voltage Measurements

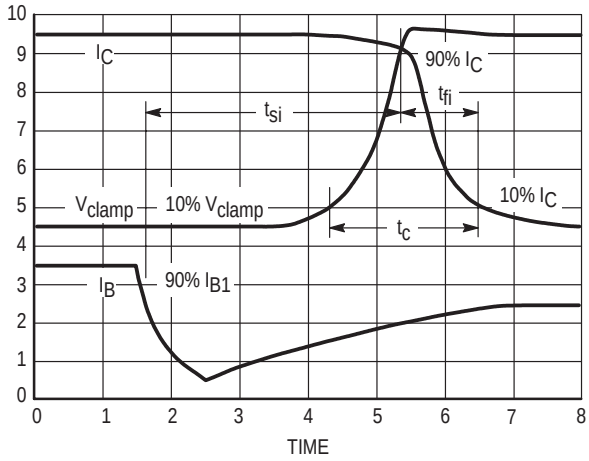
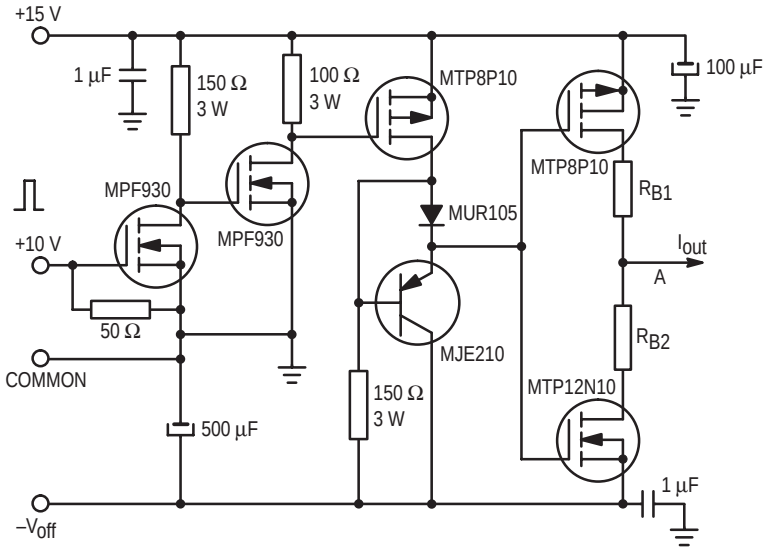
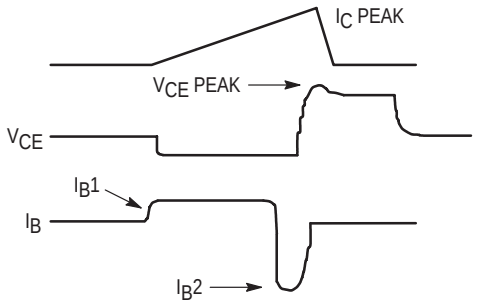


Figure 20. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL THERMAL RESPONSE

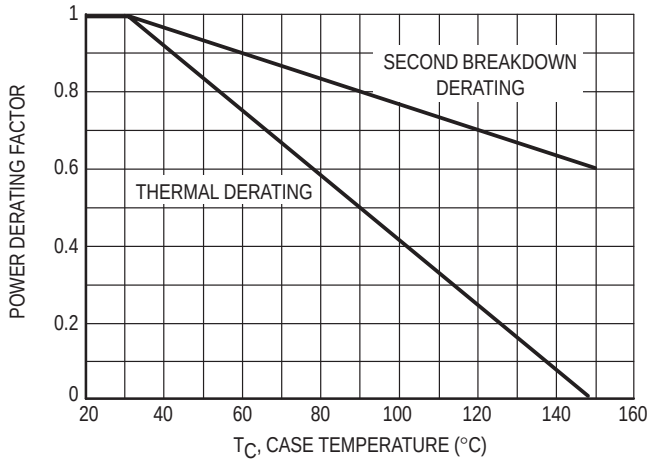


Figure 21. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 22 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 22 may be found at any case temperature by using the appropriate curve on Figure 21.

$T_{J(pk)}$ may be calculated from the data in Figure 24. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 23). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

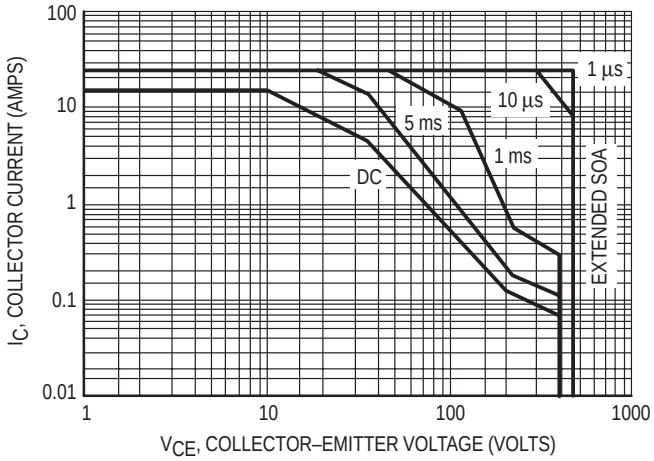


Figure 22. Forward Bias Safe Operating Area

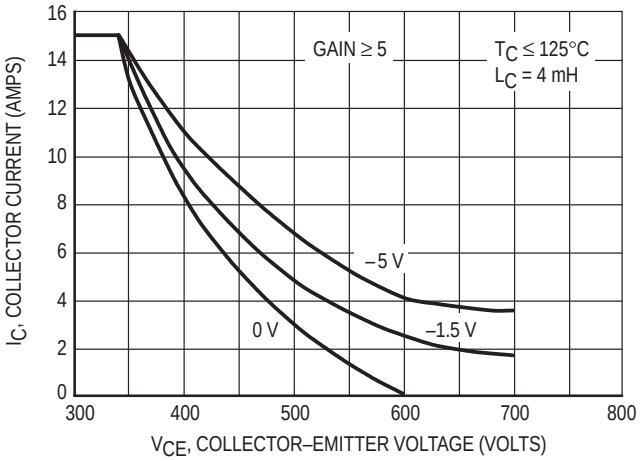


Figure 23. Reverse Bias Safe Operating Area

TYPICAL THERMAL RESPONSE

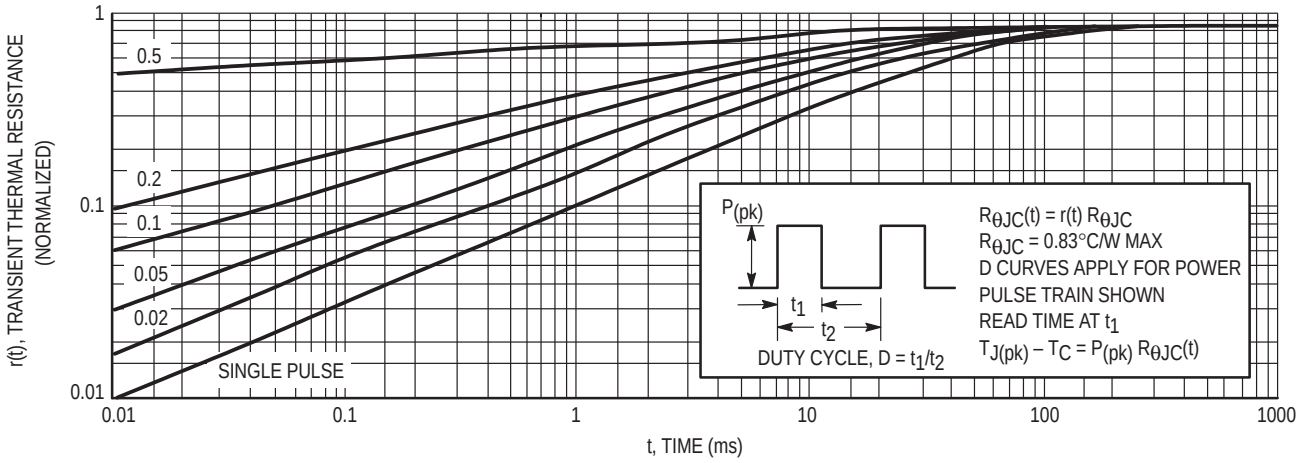


Figure 24. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUH150

Designer's™ Data Sheet
SWITCHMODE™
NPN Bipolar Power Transistor
For Switching Power Supply Applications

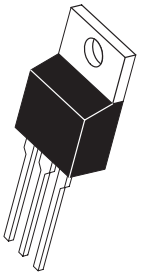
BUL44*
BUL44F*

*Motorola Preferred Device

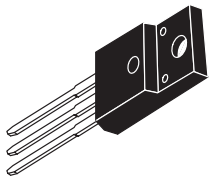
POWER TRANSISTOR
2.0 AMPERES
700 VOLTS
40 and 100 WATTS

The BUL44/BUL44F have an applications specific state–of–the–art die designed for use in 220 V line operated Switchmode Power supplies and electronic light ballasts. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  — High and Flat DC Current Gain h_{FE}
  — Fast Switching
  — No Coil Required in Base Circuit for Turn–Off (No Current Tail)
- Full Characterization at 125°C
- Tight Parametric Distributions are Consistent Lot–to–Lot
- Two Package Choices: Standard TO–220 or Isolated TO–220
- BUL44F, Case 221D, is UL Recognized to 3500 V_{RMS}: File #E69369



BUL44
CASE 221A–06
TO–220AB



BUL44F
CASE 221D–02
ISOLATED TO–220 TYPE
UL RECOGNIZED

MAXIMUM RATINGS

Rating	Symbol	BUL44	BUL44F	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700		Vdc
Emitter–Base Voltage	V_{EBO}	9.0		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	2.0 5.0		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	1.0 2.0		Adc
RMS Isolated Voltage(2) Test No. 1 Per Fig. 22a (for 1 sec, R.H. < 30%, Test No. 2 Per Fig. 22b T_C = 25°C) Test No. 3 Per Fig. 22c	V_{ISOL}	— — —	4500 3500 1500	Volts
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	50 0.4	25 0.2	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	– 65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	BUL44	BUL44F	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	5.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	—	—	100	μAdc
(T_C = 125°C)		—	—	500	
(V_{CE} = 500 V, V_{EB} = 0) (T_C = 125°C)		—	—	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS								
Base–Emitter Saturation Voltage (I_C = 0.4 Adc, I_B = 40 mAdc) (I_C = 1.0 Adc, I_B = 0.2 Adc)				$V_{BE(sat)}$	— —	0.85 0.92	1.1 1.25	Vdc
Collector–Emitter Saturation Voltage (I_C = 0.4 Adc, I_B = 40 mAdc) (I_C = 1.0 Adc, I_B = 0.2 Adc)				$V_{CE(sat)}$	 — — — —	 0.20 0.20 0.25 0.25	 0.5 0.5 0.6 0.6	Vdc
DC Current Gain (I_C = 0.2 Adc, V_{CE} = 5.0 Vdc) (I_C = 0.4 Adc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)				h_{FE}	 14 — 12 12 8.0 7.0 10	 — 32 20 20 14 13 22	 34 — — — — — —	—
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)				f_T	—	13	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)				C_{OB}	—	38	60	pF
Input Capacitance (V_{EB} = 8.0 V)				C_{IB}	—	380	600	pF
Dynamic Saturation Voltage: Determined 1.0 µs and 3.0 µs respectively after rising I_{B1} reaches 90% of final I_{B1}	(I_C = 0.4 Adc I_{B1} = 40 mAdc V_{CC} = 300 V)	1.0 µs	(T_C = 125°C)	$V_{CE(dsat)}$	— —	2.5 2.7	— —	Vdc
		3.0 µs	(T_C = 125°C)		— —	1.3 1.15	— —	
	(I_C = 1.0 Adc I_{B1} = 0.2 Adc V_{CC} = 300 V)	1.0 µs	(T_C = 125°C)		— —	3.2 7.5	— —	
		3.0 µs	(T_C = 125°C)		— —	1.25 1.6	— —	
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 µs)								
Turn–On Time	(I_C = 0.4 Adc, I_{B1} = 40 mAdc I_{B2} = 0.2 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	— —	40 40	100 —	ns
Turn–Off Time	(I_C = 0.4 Adc, I_{B1} = 40 mAdc I_{B2} = 0.2 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{off}	— —	1.5 2.0	2.5 —	µs
Turn–On Time	(I_C = 1.0 Adc, I_{B1} = 0.2 Adc I_{B1} = 0.5 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	— —	85 85	150 —	ns
Turn–Off Time	(I_C = 1.0 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{off}	— —	1.75 2.10	2.5 —	µs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 µH)								
Fall Time	(I_C = 0.4 Adc, I_{B1} = 40 mAdc I_{B2} = 0.2 Adc)		(T_C = 125°C)	t_{fi}	— —	125 120	200 —	ns
Storage Time			(T_C = 125°C)	t_{si}	— —	0.7 0.8	1.25 —	µs
Crossover Time			(T_C = 125°C)	t_c	— —	110 110	200 —	ns
Fall Time	(I_C = 1.0 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc)		(T_C = 125°C)	t_{fi}	— —	110 120	175 —	ns
Storage Time			(T_C = 125°C)	t_{si}	— —	1.7 2.25	2.75 —	µs
Crossover Time			(T_C = 125°C)	t_c	— —	180 210	300 —	ns
Fall Time	(I_C = 0.8 Adc, I_{B1} = 160 mAdc I_{B2} = 160 mAdc)		(T_C = 125°C)	t_{fi}	70 —	— 180	170 —	ns
Storage Time			(T_C = 125°C)	t_{si}	2.6 —	— 4.2	3.8 —	µs
Crossover Time			(T_C = 125°C)	t_c	— —	190 350	300 —	ns

r

TYPICAL STATIC CHARACTERISTICS

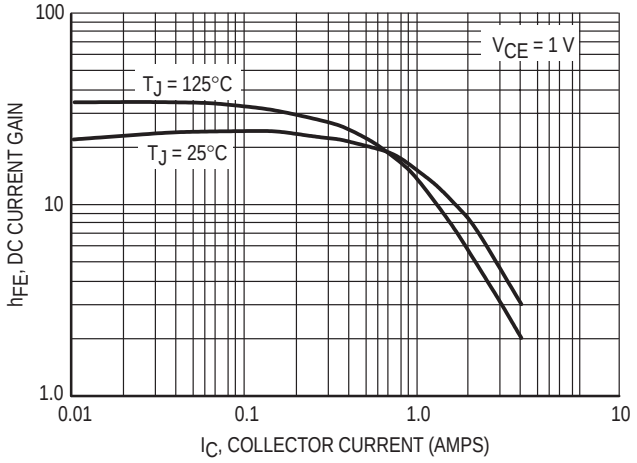


Figure 1. DC Current Gain at 1 Volt

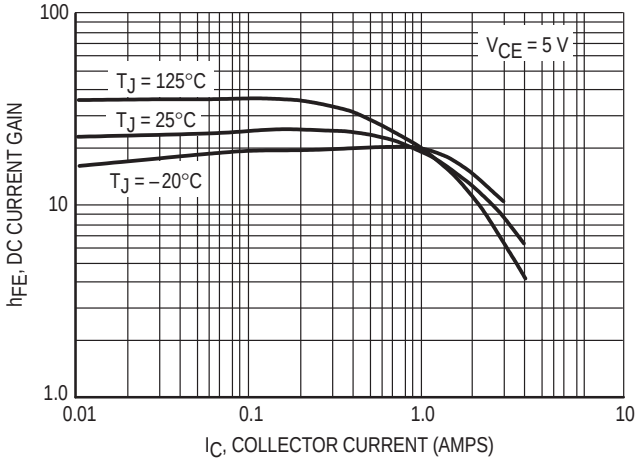


Figure 2. DC Current Gain at 5 Volts

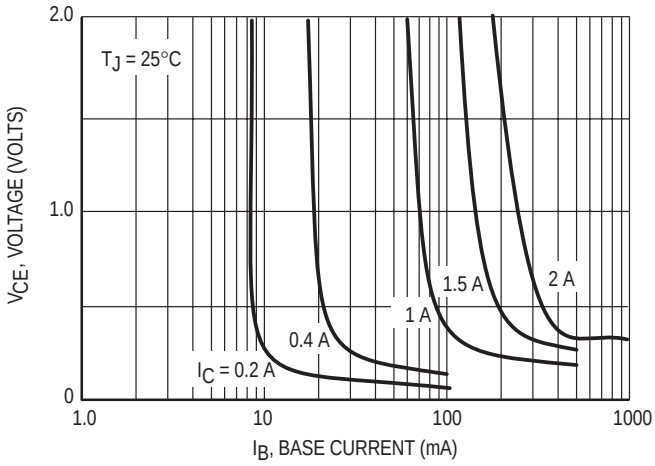


Figure 3. Collector Saturation Region

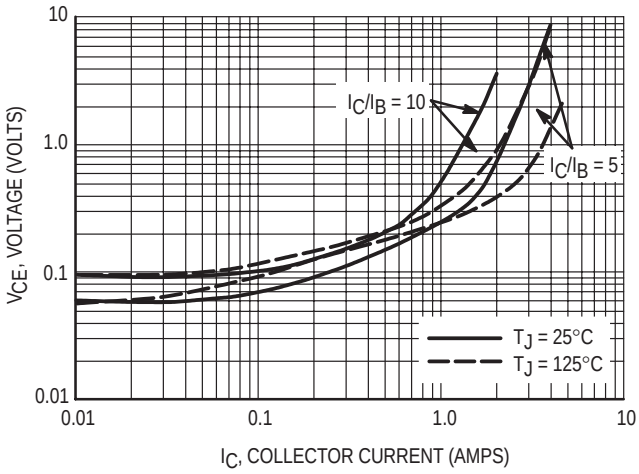


Figure 4. Collector–Emitter Saturation Voltage

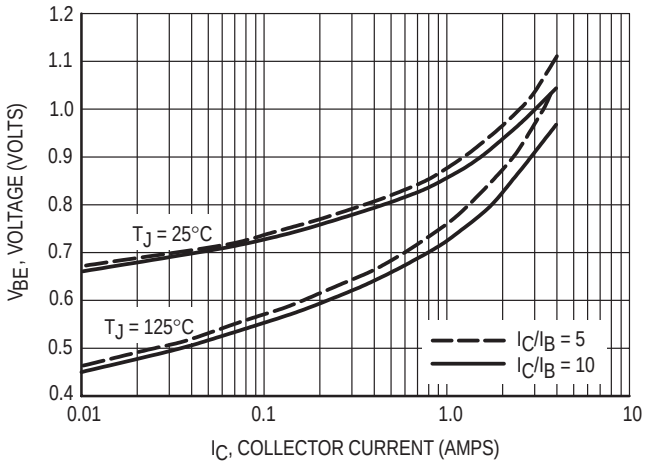


Figure 5. Base–Emitter Saturation Region

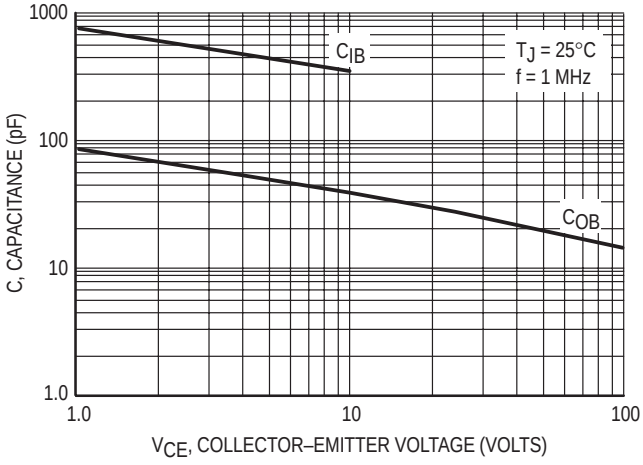


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

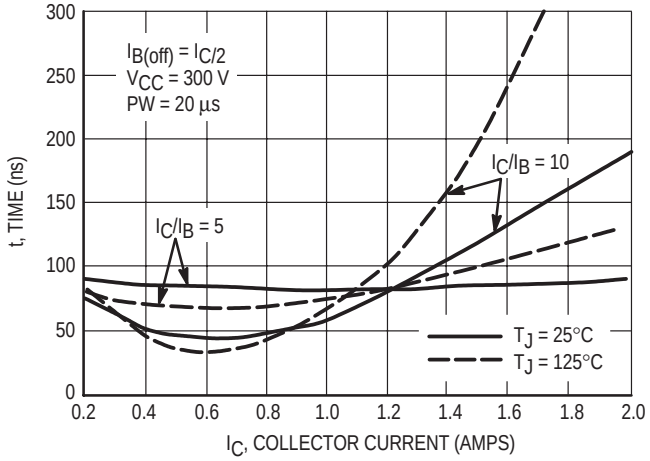


Figure 7. Resistive Switching, t_{on}

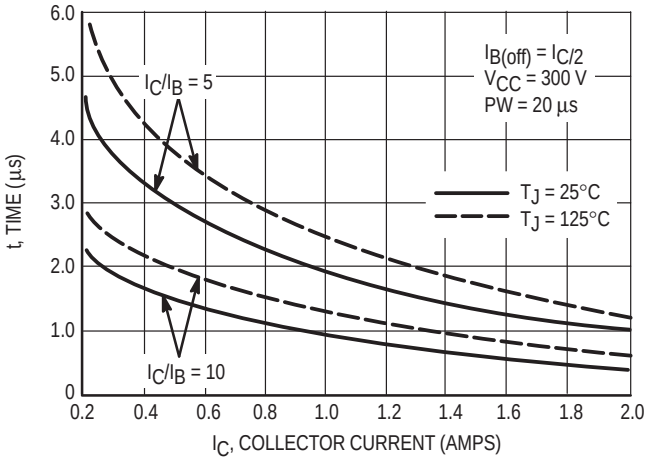


Figure 8. Resistive Switching, t_{off}

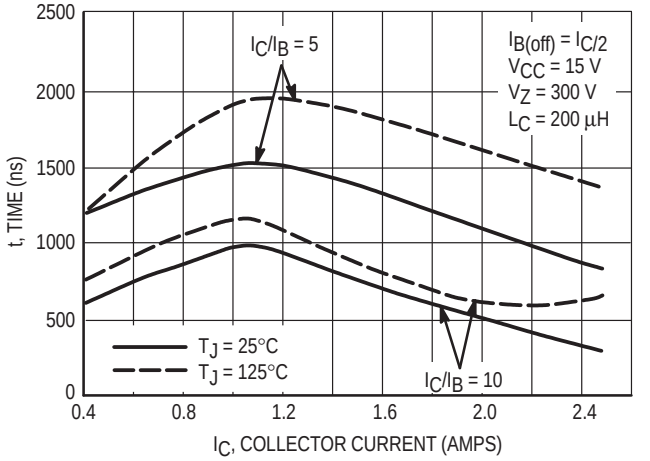


Figure 9. Inductive Storage Time, t_{si}

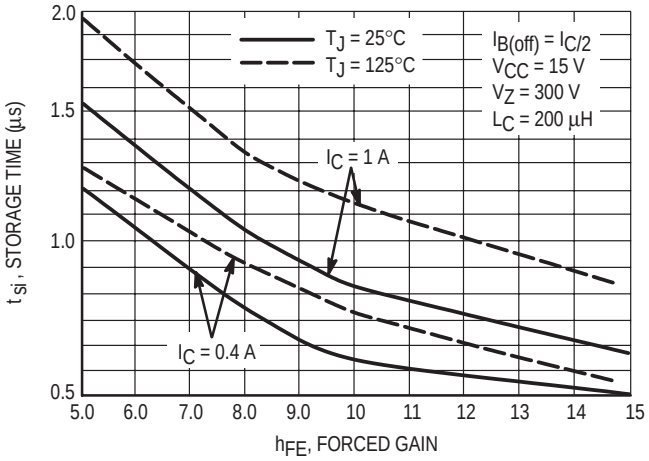


Figure 10. Inductive Storage Time

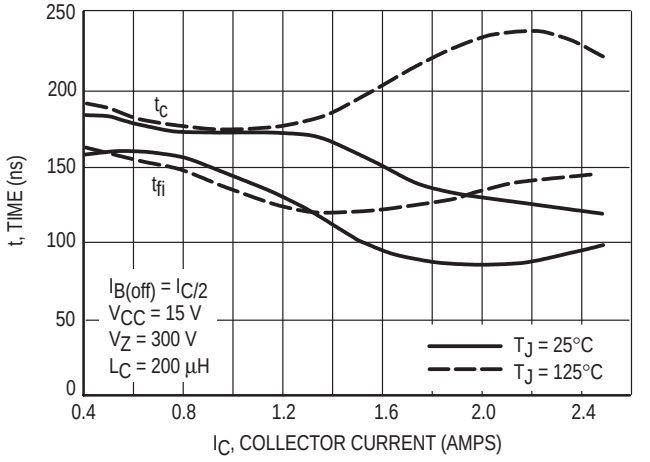


Figure 11. Inductive Switching, t_c and t_{fi} I_C/I_B = 5

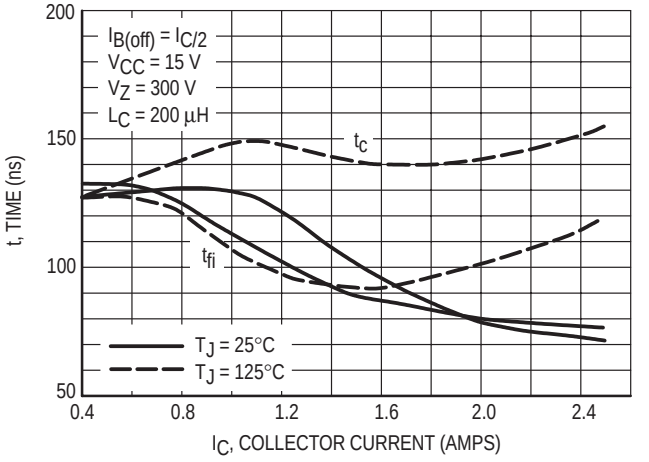


Figure 12. Inductive Switching, t_c and t_{fi} I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

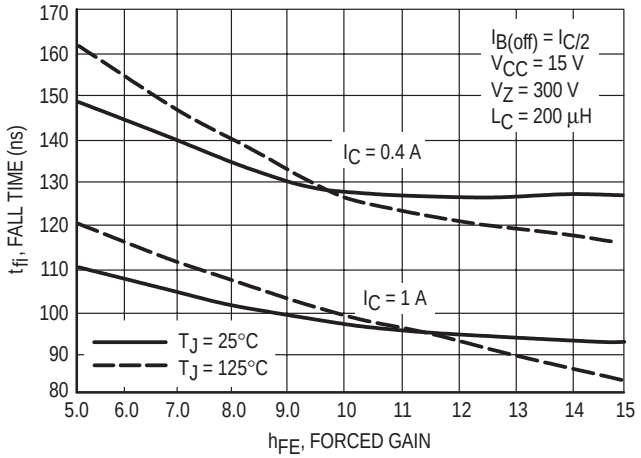


Figure 13. Inductive Fall Time

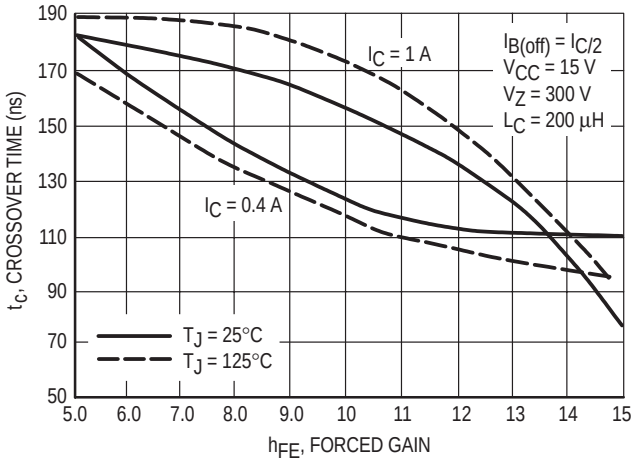


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

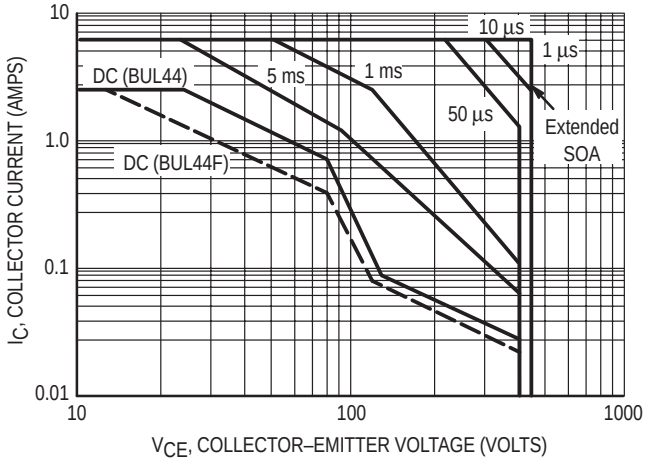


Figure 15. Forward Bias Safe Operating Area

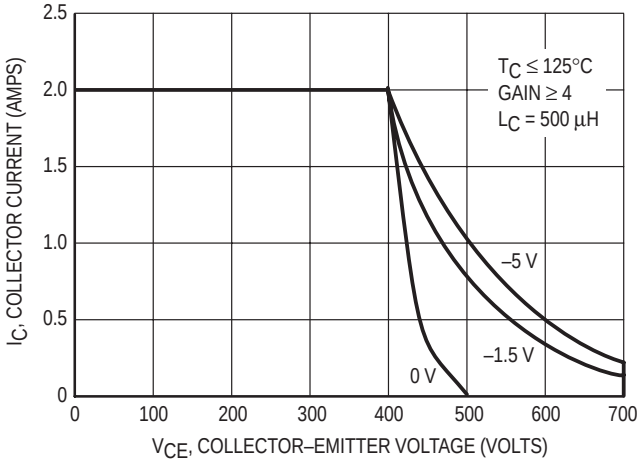


Figure 16. Reverse Bias Switching Safe Operating Area

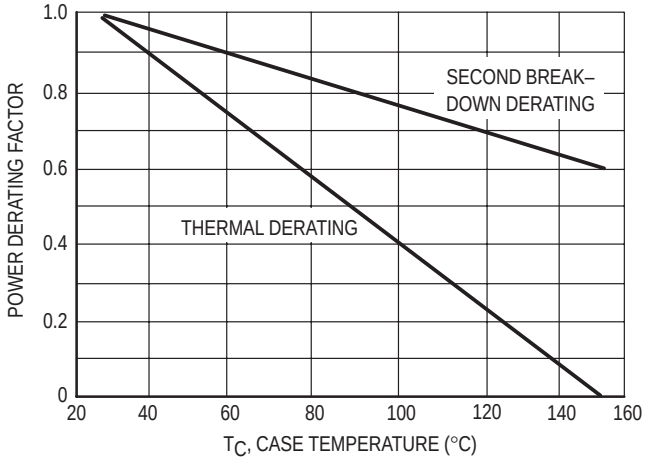


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of figure 15 is based on T_C = 25°C; $T_{J(PK)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on figure 15 may be found at any case temperature by using the appropriate curve on figure 17. $T_{J(PK)}$ may be calculated from the data in figure 20 and 21. At any case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse–biased. The safe level is specified as a reverse–biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

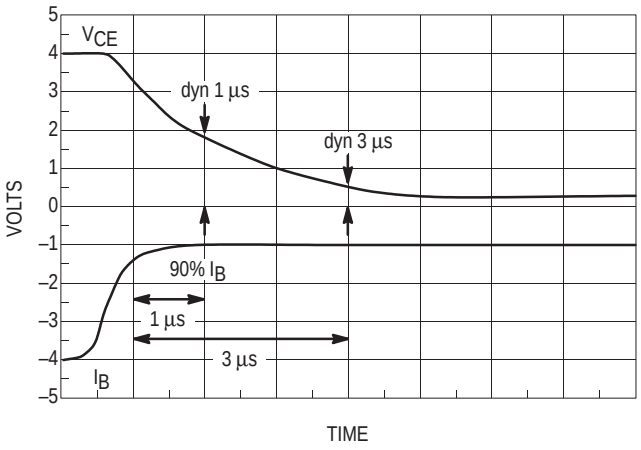


Figure 18. Dynamic Saturation Voltage Measurements

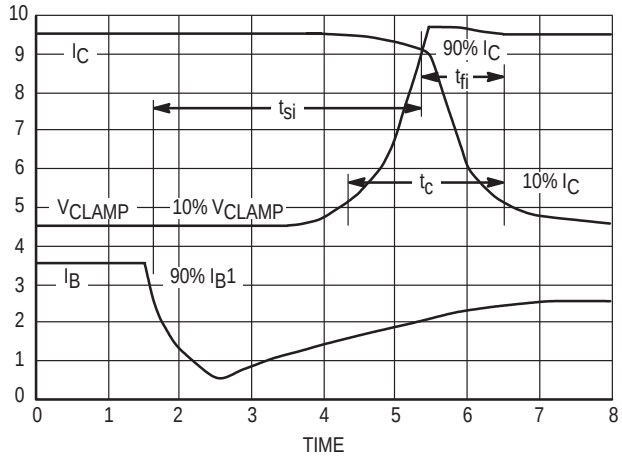
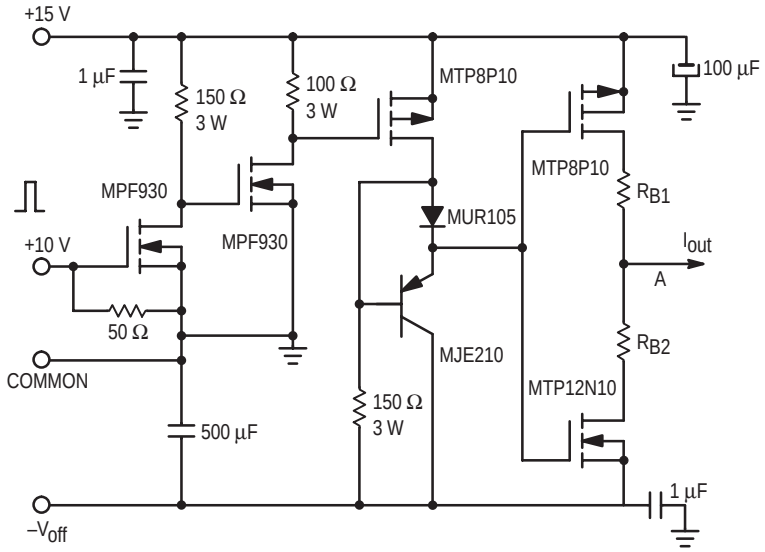
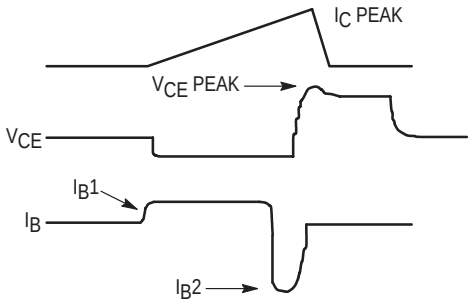


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_{B1}	RB1 SELECTED FOR DESIRED I_{B1}

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

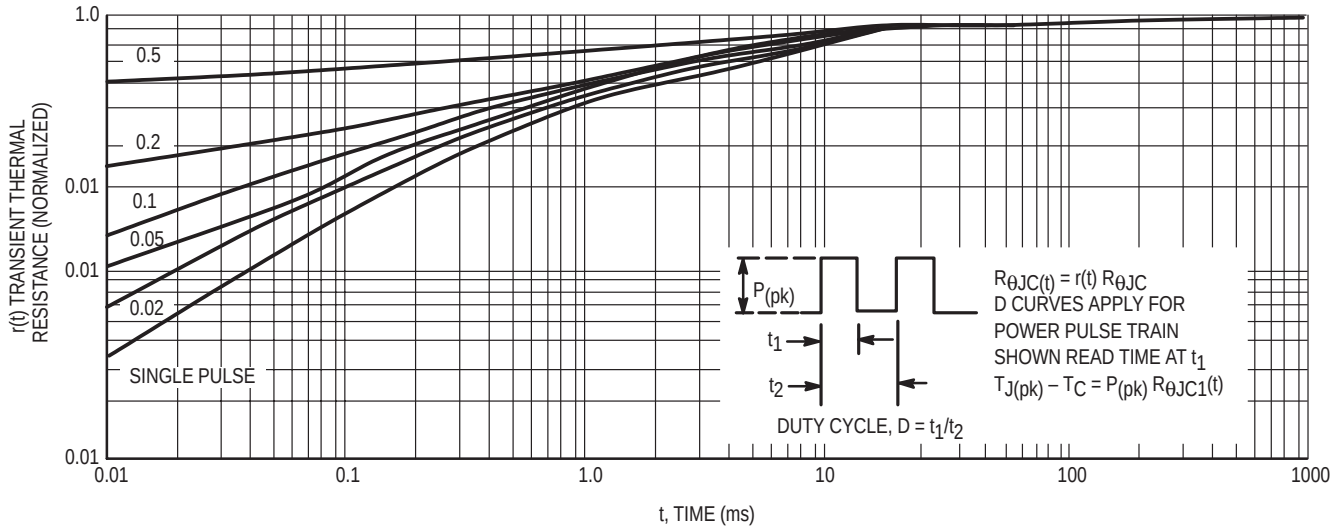


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL44

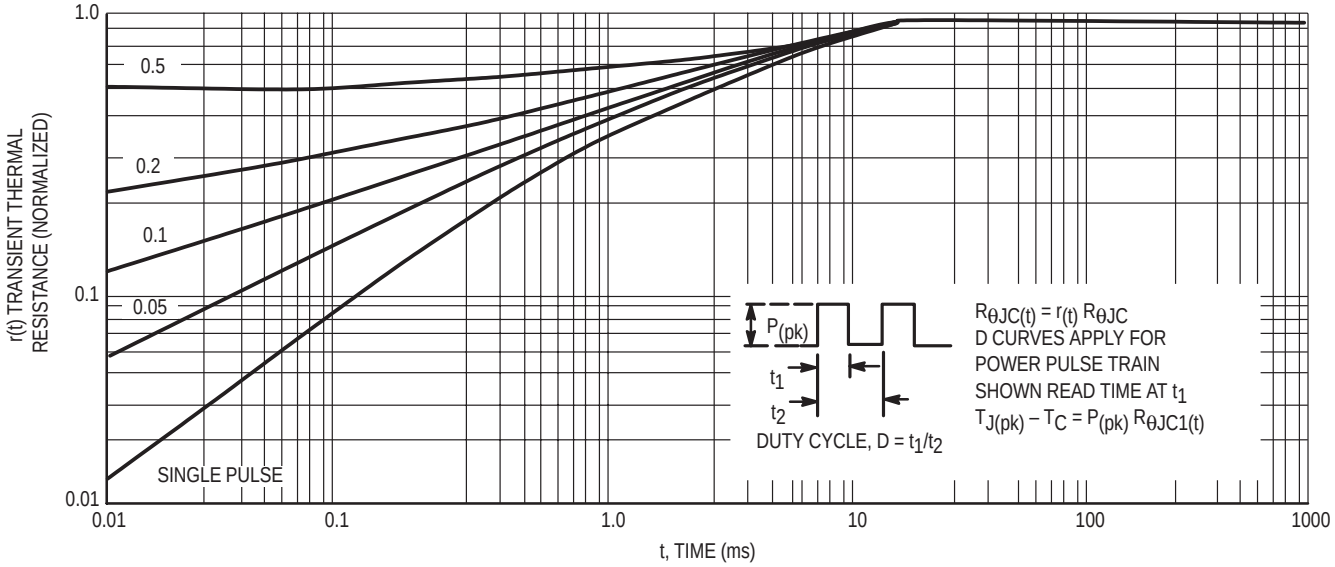


Figure 21. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL44F

TEST CONDITIONS FOR ISOLATION TESTS*

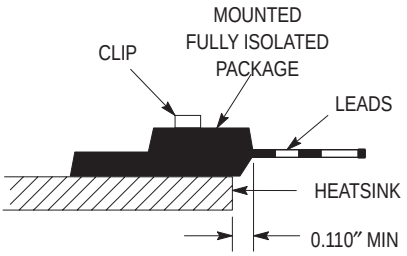


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

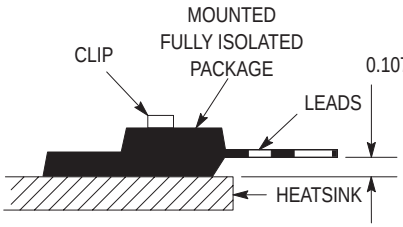


Figure 22b. Clip Mounting Position for Isolation Test Number 2

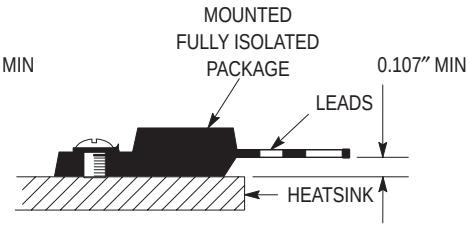


Figure 22c. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together.

MOUNTING INFORMATION**

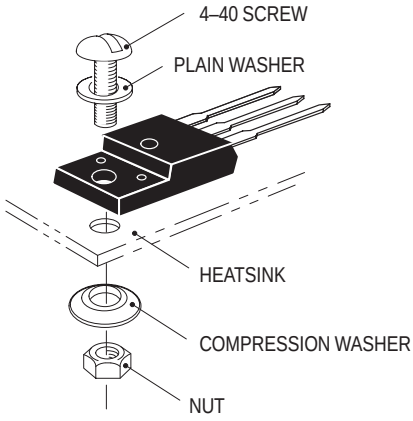


Figure 23a. Screw–Mounted

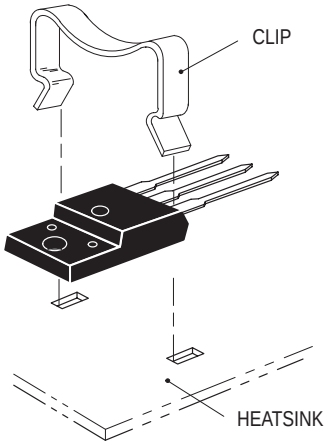


Figure 23b. Clip–Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

BUL43B

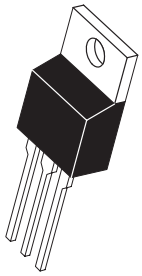
Product Preview

SWITCHMODE NPN Silicon Planar Power Transistor

POWER TRANSISTORS
2 AMPERES
700 VOLTS
40 WATTS

The BUL43B has an application specific state–of–the–art die designed for use in 220 V line operated Switchmode Power supplies and electronic ballast (“light ballast”). The main advantages brought by this new transistor are:

- Improved Efficiency Due to Low Base Drive Requirements:
  — High and Flat DC Current Gain h_{FE}
  — Fast and Tightened Switching Distributions
  — No Coil Required in Base Circuit for Fast Turn–Off (no current tail)



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	350	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	650	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	650	Vdc
Emitter–Base Voltage	V_{EBO}	9	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	2 4	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	1 2	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	40 0.32	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 3.125 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

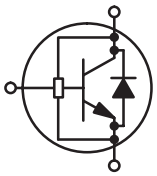
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	350			Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			10 200	μAdc
Emitter–Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.5 Adc)		$V_{BE(sat)}$			1.25	Vdc
Collector–Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.5 Adc)	@ T_C = 25°C	$V_{CE(sat)}$			1	Vdc
DC Current Gain (I_C = 1 Adc, V_{CE} = 2 Vdc)	@ T_C = 25°C	h_{FE}	8			—
(I_C = 2 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C		6			—
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}		40		pF
Input Capacitance (V_{EB} = 8 V)		C_{ib}		400		pF
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)						
Turn–off Time	I_C = 1.2 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.1 Adc V_{CC} = 300 Vdc	@ T_C = 25°C	t_{off}	4.7		5.8	μs
Fall Time	I_C = 2.5 Adc, I_{B1} = 0.5 Adc I_{B2} = 0.5 Adc V_{CC} = 150 Vdc	@ T_C = 25°C	t_f			800	ns

BUL44D2

Designer's™ Data Sheet

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

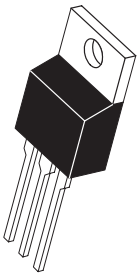
POWER TRANSISTORS
2 AMPERES
700 VOLTS
50 WATTS



The BUL44D2 is state–of–art High Speed High gain BIPolar transistor (H2BIP). High dynamic characteristics and lot to lot minimum spread (±150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an h_{FE} window.
Main features:

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ I_C = 100 mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector–Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic $V_{CE(sat)}$
- "6 Sigma" Process Providing Tight and Reproductible Parameter Spreads

It's characteristics make it also suitable for PFC application.



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter–Base Voltage	V_{EBO}	12	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	2 5	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	1 2	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	50 0.4	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	400	470		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	700	920		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	12	14.5		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CEO}			50 500	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0) (V_{CE} = 500 V, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C @ T_C = 125°C	I_{CES}			50 500 100	μAdc
Emitter–Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 0.4 Adc, I_B = 40 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{BE(sat)}$		0.78 0.65	0.9 0.8	Vdc
(I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C			0.87 0.76	1 0.9	
Collector–Emitter Saturation Voltage (I_C = 0.4 Adc, I_B = 40 mAdc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.25 0.27	0.4 0.5	Vdc
(I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C			0.28 0.35	0.5 0.6	
(I_C = 0.4 Adc, I_B = 20 mAdc)	@ T_C = 25°C @ T_C = 125°C			0.45 0.67	0.65 1	
DC Current Gain (I_C = 0.4 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	20 18	32 26		—
(I_C = 1 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		10 7	14 9.5		
DIODE CHARACTERISTICS						
Forward Diode Voltage (I_{EC} = 1 Adc)	@ T_C = 25°C	V_{EC}		1.1	1.5	V
(I_{EC} = 0.4 Adc)	@ T_C = 25°C			0.9	1.2	
(I_{EC} = 0.2 Adc)	@ T_C = 25°C			0.8	1	
(I_{EC} = 0.2 Adc)	@ T_C = 125°C			0.6		
Forward Recovery Time (see Figure 22 bis) (I_F = 0.2 Adc, di/dt = 10 A/μs)	@ T_C = 25°C	T_{fr}		415		ns
(I_F = 0.4 Adc, di/dt = 10 A/μs)	@ T_C = 25°C			390		
(I_F = 1 Adc, di/dt = 10 A/μs)	@ T_C = 25°C			340		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
DYNAMIC SATURATION VOLTAGE								
Dynamic Saturation Voltage: Determined 1 µs and 3 µs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 0.4 A, I_{B1} = 40 mA, V_{CC} = 300 V	@ 1 µs	@ T_C = 25°C	$V_{CE(dsat)}$		3.3		V
			@ T_C = 125°C			6.8		
		@ 3 µs	@ T_C = 25°C			0.5		V
			@ T_C = 125°C			1.3		
	I_C = 1 A, I_{B1} = 0.2 A, V_{CC} = 300 V	@ 1 µs	@ T_C = 25°C			4.4		V
			@ T_C = 125°C			12.8		
		@ 3 µs	@ T_C = 25°C			0.5		V
			@ T_C = 125°C			1.8		
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)				f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)				C_{ob}		50	75	pF
Input Capacitance (V_{EB} = 8 Vdc)				C_{ib}		240	500	pF
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 µs)								
Turn–on Time	I_C = 0.5 Adc, I_{B1} = 50 mAdc, I_{B2} = 250 mAdc, V_{CC} = 300 Vdc		@ T_C = 25°C	t_{on}		450	600	ns
			@ T_C = 125°C			600		
Turn–off Time			@ T_C = 25°C	t_{off}	700		1000	ns
			@ T_C = 125°C			1300		
Turn–on Time	I_C = 1 Adc, I_{B1} = 0.2 Adc, I_{B2} = 0.5 Adc, V_{CC} = 300 Vdc		@ T_C = 25°C	t_{on}		90	150	ns
			@ T_C = 125°C			105		
Turn–off Time			@ T_C = 25°C	t_{off}		1.1	1.25	µs
			@ T_C = 125°C			1.5		
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 µH)								
Fall Time	I_C = 0.4 Adc, I_{B1} = 40 mAdc, I_{B2} = 0.2 Adc		@ T_C = 25°C	t_f		110	150	ns
			@ T_C = 125°C			105		
Storage Time			@ T_C = 25°C	t_s		0.55	0.75	µs
			@ T_C = 125°C			0.70		
Crossover Time			@ T_C = 25°C	t_c		85	150	ns
			@ T_C = 125°C			80		
Fall Time	I_C = 1 Adc, I_{B1} = 0.2 Adc, I_{B2} = 0.5 Adc		@ T_C = 25°C	t_f		100	150	ns
			@ T_C = 125°C			90		
Storage Time			@ T_C = 25°C	t_s		1.05	1.5	µs
			@ T_C = 125°C			1.45		
Crossover Time			@ T_C = 25°C	t_c		100	175	ns
			@ T_C = 125°C			100		
Fall Time	I_C = 0.8 Adc, I_{B1} = 160 mAdc, I_{B2} = 160 mAdc		@ T_C = 25°C	t_f		110	150	ns
			@ T_C = 125°C			180		
Storage Time			@ T_C = 25°C	t_s	2.05		2.35	µs
			@ T_C = 125°C			2.8		
Crossover Time			@ T_C = 25°C	t_c		180	300	ns
			@ T_C = 125°C			400		
Fall Time	I_C = 0.4 Adc, I_{B1} = 40 mAdc, I_{B2} = 40 mAdc		@ T_C = 25°C	t_f		150	225	ns
			@ T_C = 125°C			175		
Storage Time			@ T_C = 25°C	t_s	1.65		1.95	µs
			@ T_C = 125°C			2.2		
Crossover Time			@ T_C = 25°C	t_c		150	250	ns
			@ T_C = 125°C			330		

TYPICAL STATIC CHARACTERISTICS

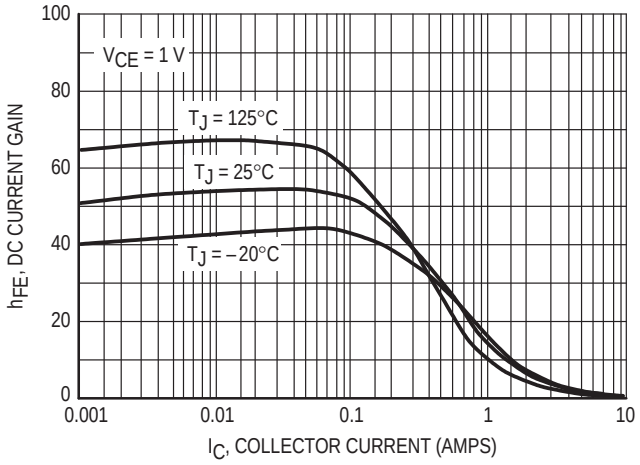


Figure 1. DC Current Gain @ 1 Volt

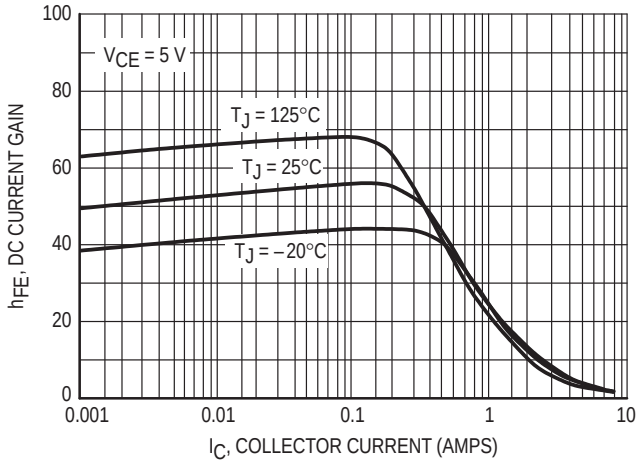


Figure 2. DC Current Gain @ 5 Volt

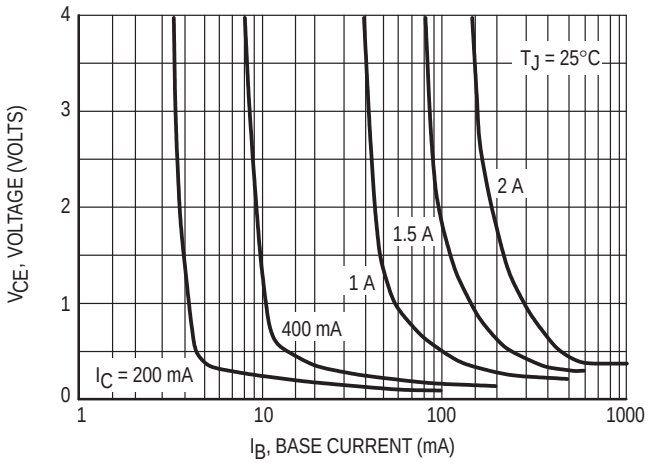


Figure 3. Collector Saturation Region

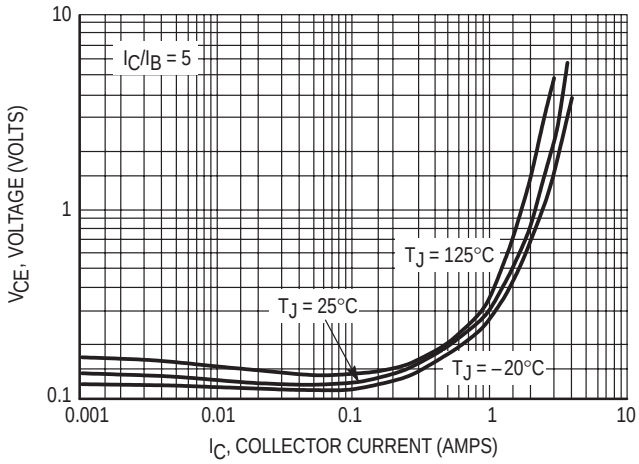


Figure 4. Collector–Emitter Saturation Voltage

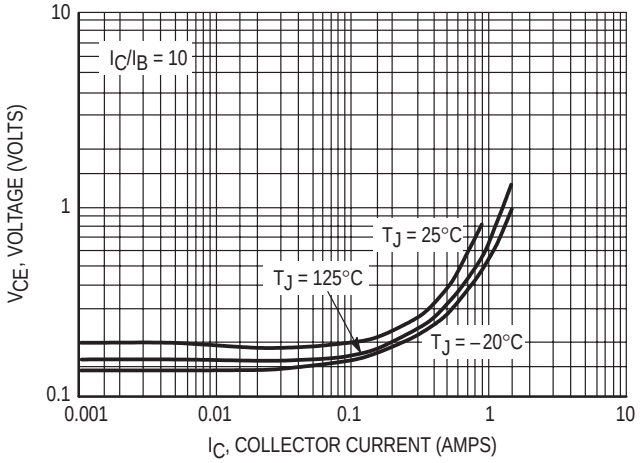


Figure 5. Collector–Emitter Saturation Voltage

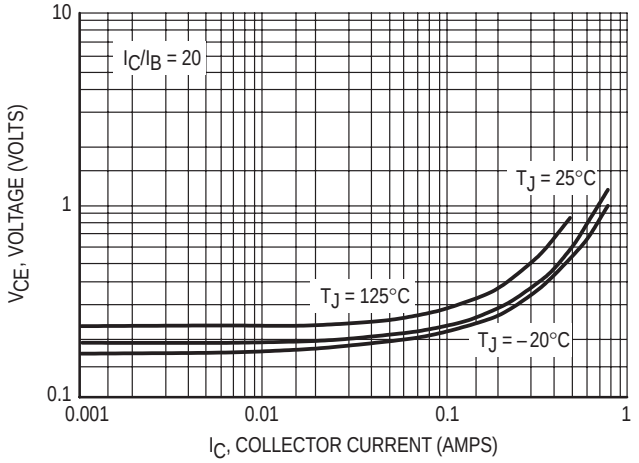


Figure 6. Collector–Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

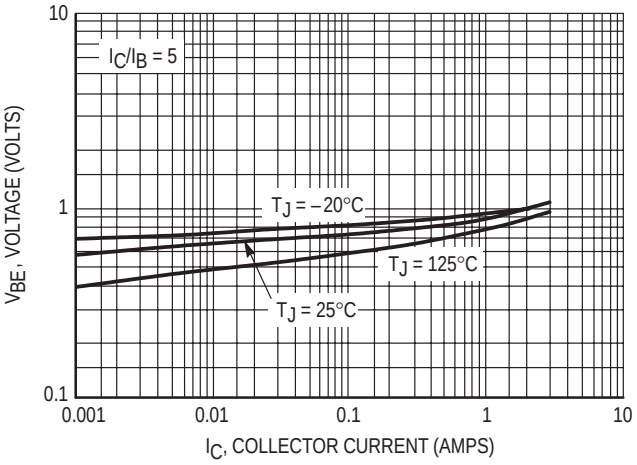


Figure 7A. Base–Emitter Saturation Region

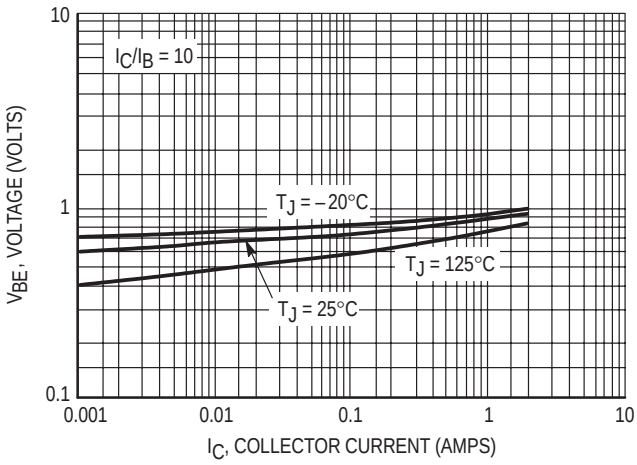


Figure 7B. Base–Emitter Saturation Region

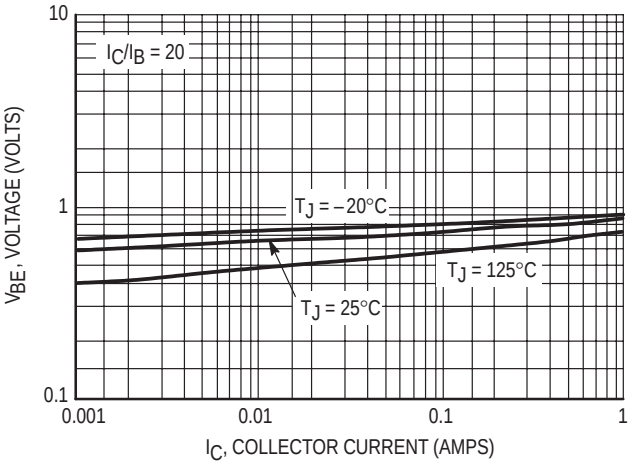


Figure 7C. Base–Emitter Saturation Region

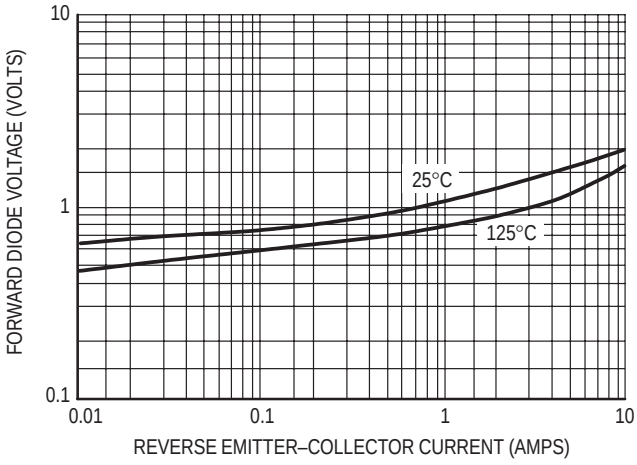


Figure 8. Forward Diode Voltage

TYPICAL SWITCHING CHARACTERISTICS

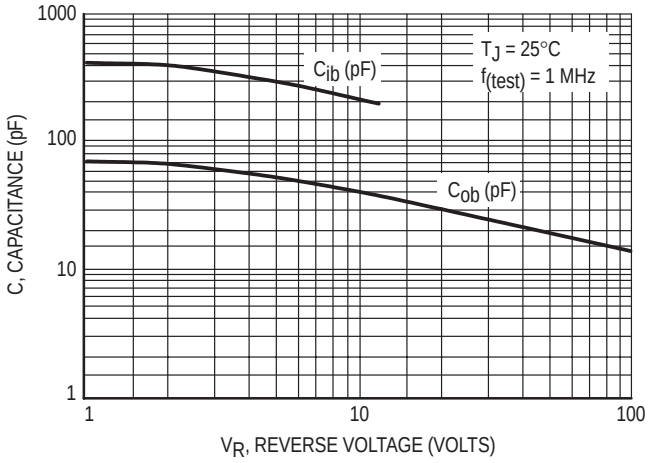


Figure 9. Capacitance

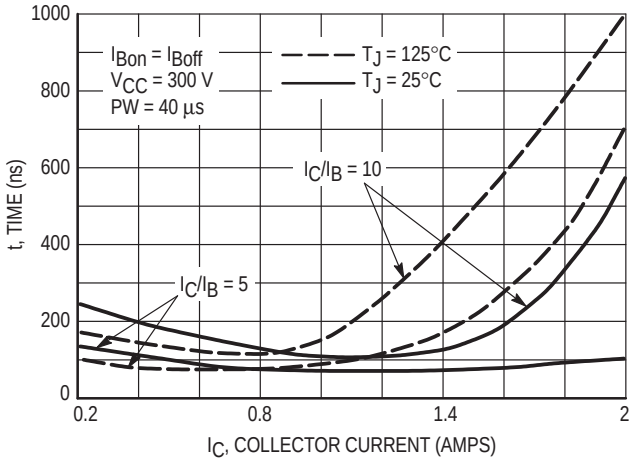


Figure 10. Resistive Switch Time, t_{on}

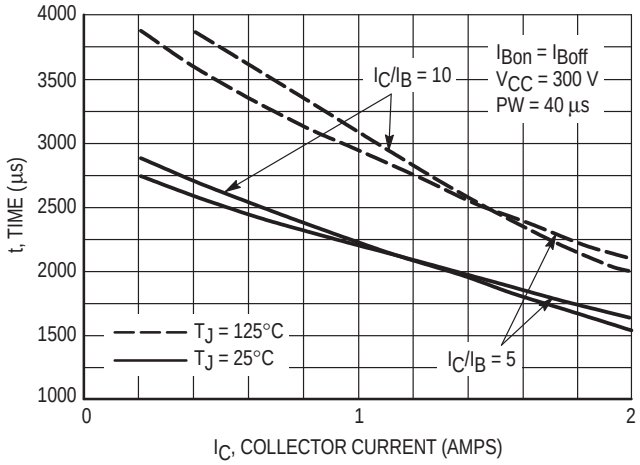


Figure 11. Resistive Switch Time, t_{off}

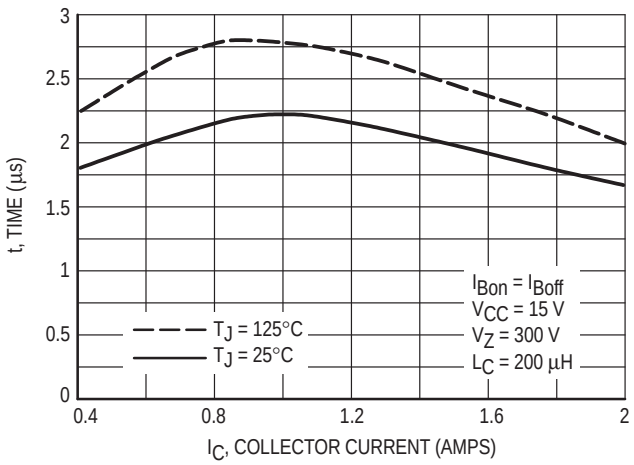


Figure 12. Inductive Storage Time, t_{si} @ I_C/I_B = 5

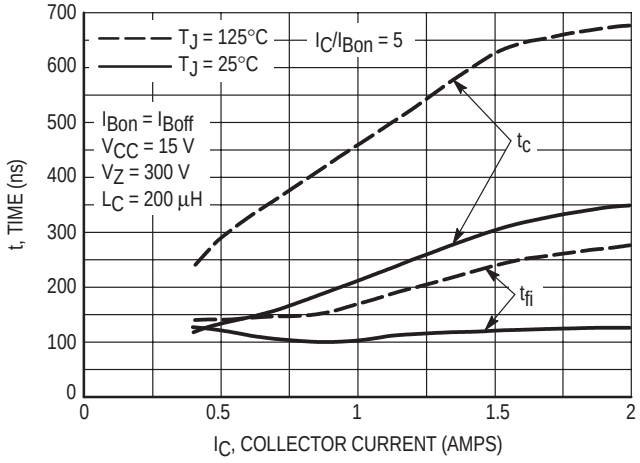


Figure 13. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 5

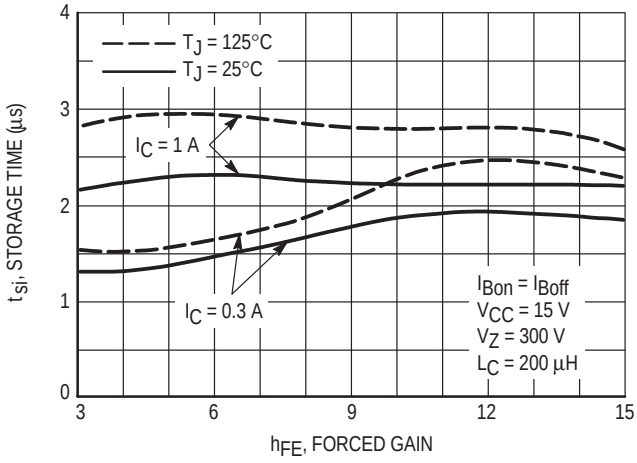


Figure 14. Inductive Storage Time

TYPICAL SWITCHING CHARACTERISTICS

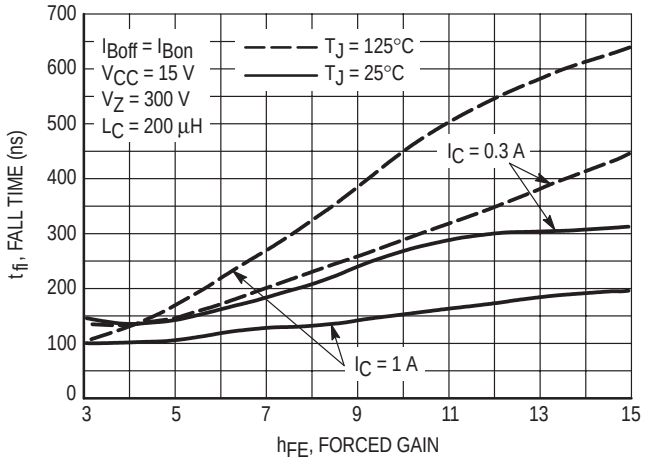


Figure 15. Inductive Fall Time

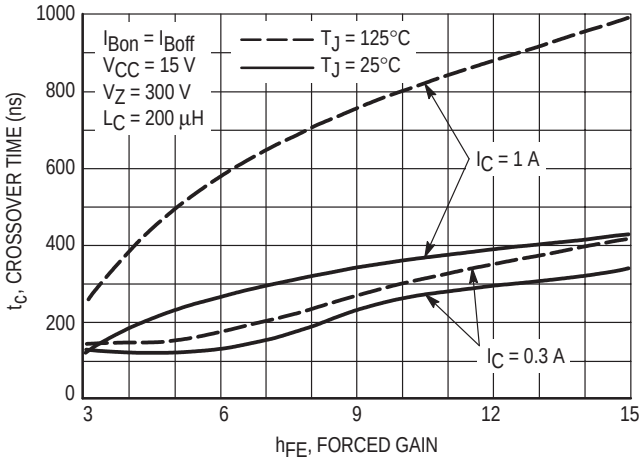


Figure 16. Inductive Crossover Time

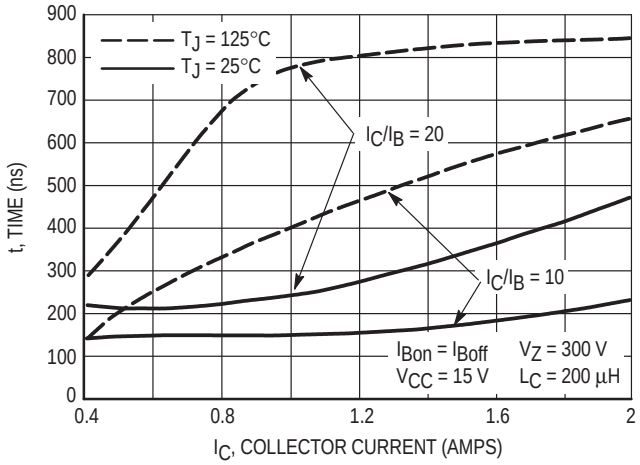


Figure 17. Inductive Switching, t_{fi}

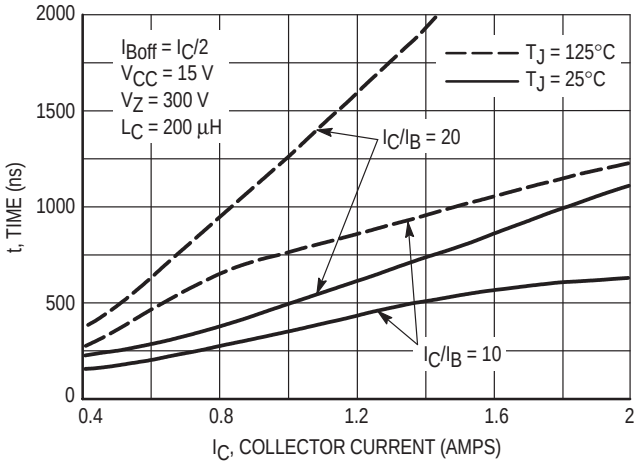


Figure 18. Inductive Switching, t_c

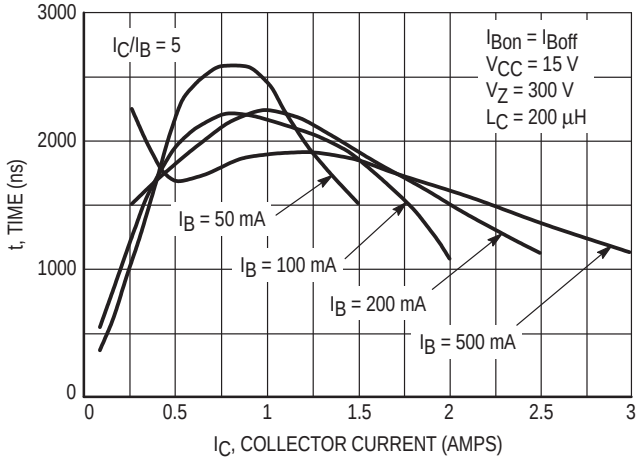


Figure 19. Inductive Storage Time, t_{si}

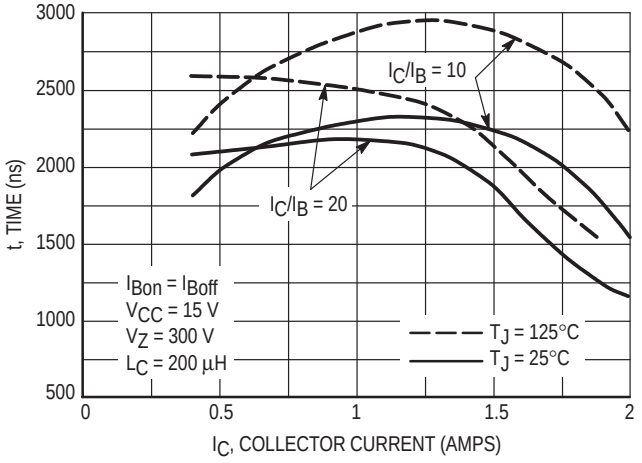


Figure 20. Inductive Storage Time, t_{si}

TYPICAL SWITCHING CHARACTERISTICS

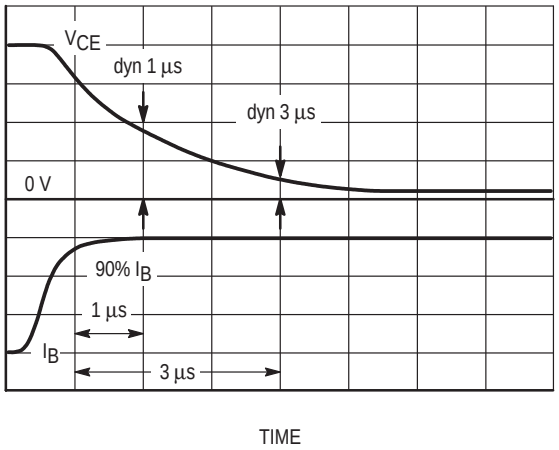


Figure 21. Dynamic Saturation Voltage Measurements

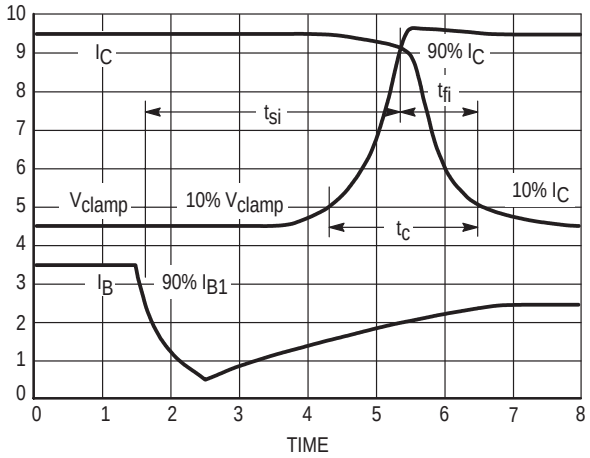


Figure 22. Inductive Switching Measurements

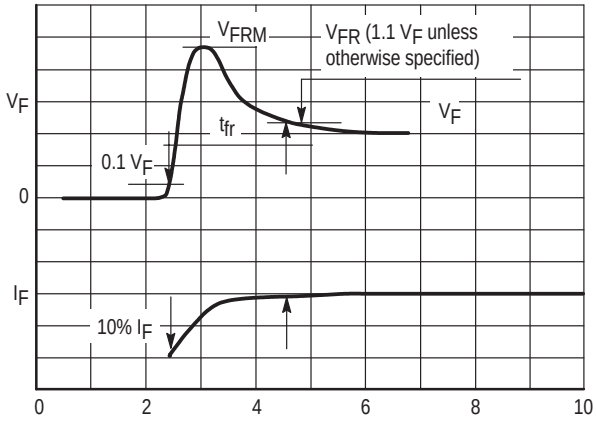
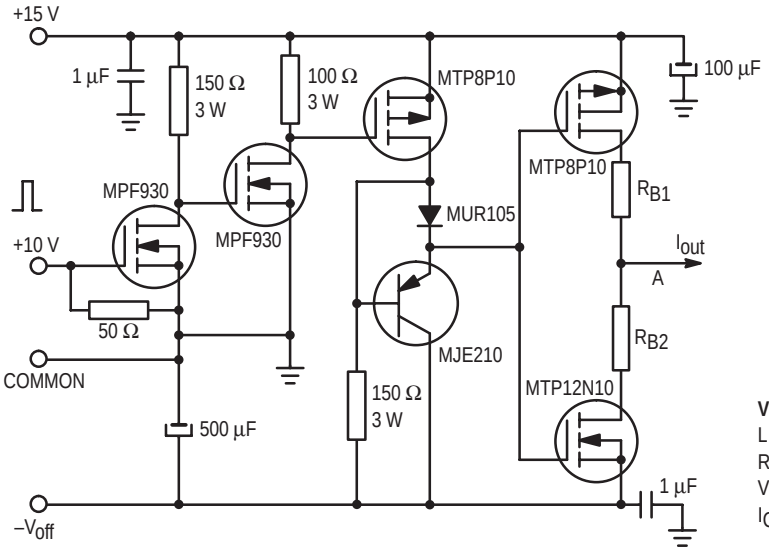
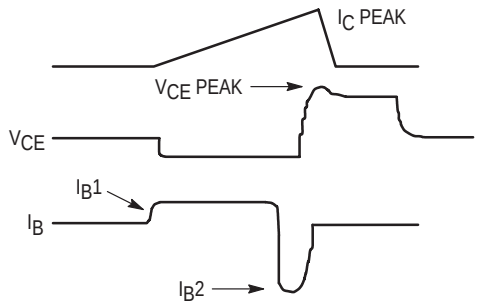


Figure 22 bis. t_{fr} Measurements

Table 1. Inductive Load Switching Drive Circuit





V(BR)CEO(sus)	**Inductive Switching**	**RBSOA**
L = 10 mH	L = 200 μH	L = 500 μH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL CHARACTERISTICS

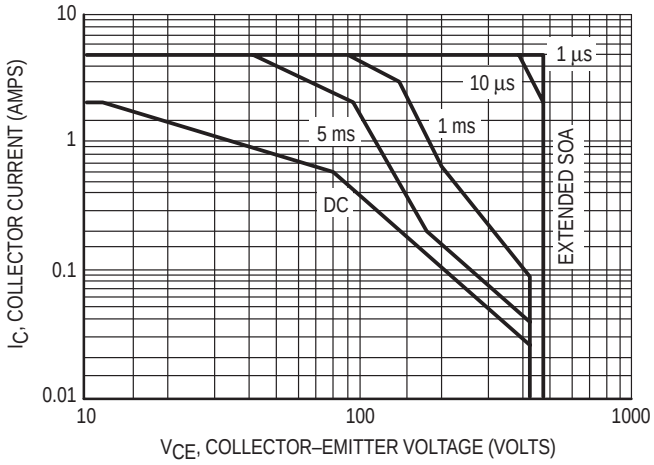


Figure 23. Forward Bias Safe Operating Area

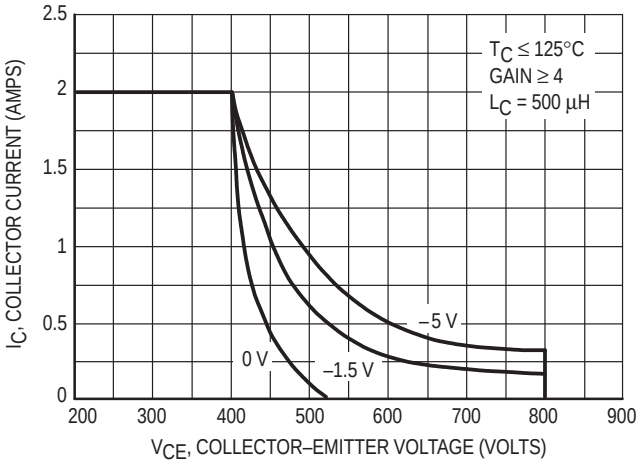


Figure 24. Reverse Bias Safe Operating Area

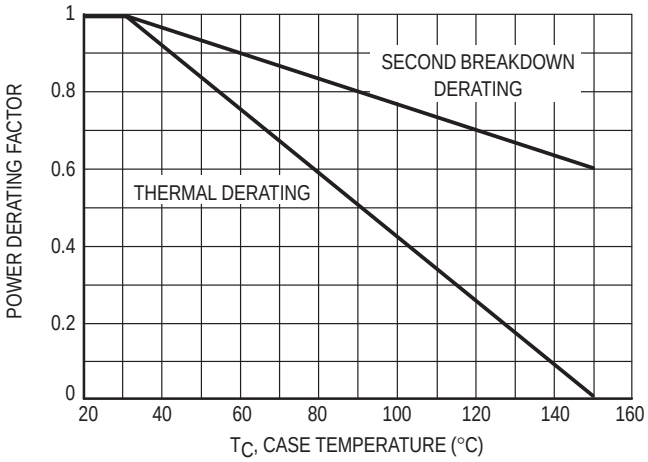


Figure 25. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 23 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 23 may be found at any case temperature by using the appropriate curve on Figure 25.

$T_{J(pk)}$ may be calculated from the data in Figure 26. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 24). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL THERMAL RESPONSE

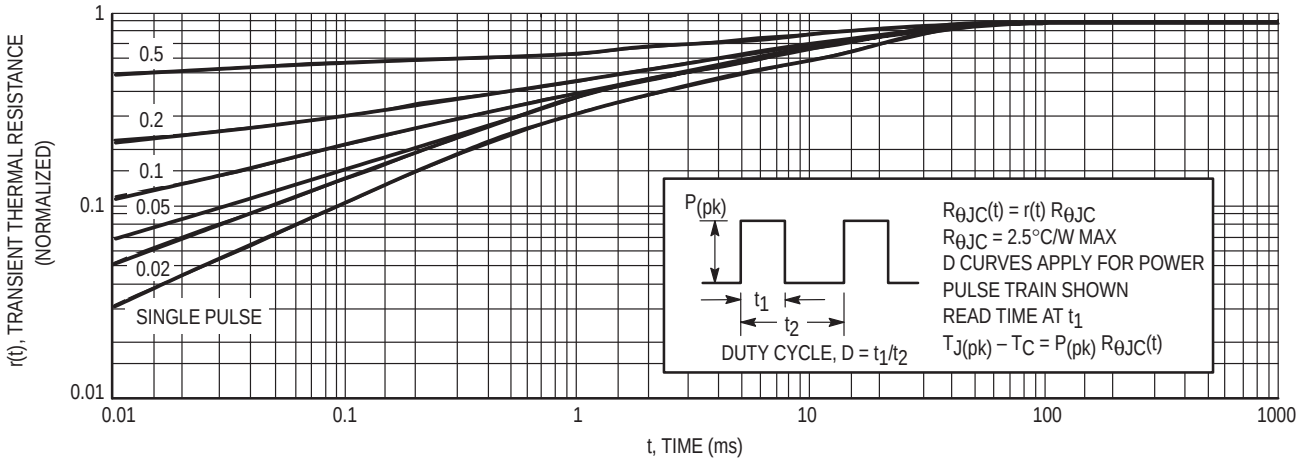


Figure 26. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL44D2

TYPICAL STATIC CHARACTERISTICS

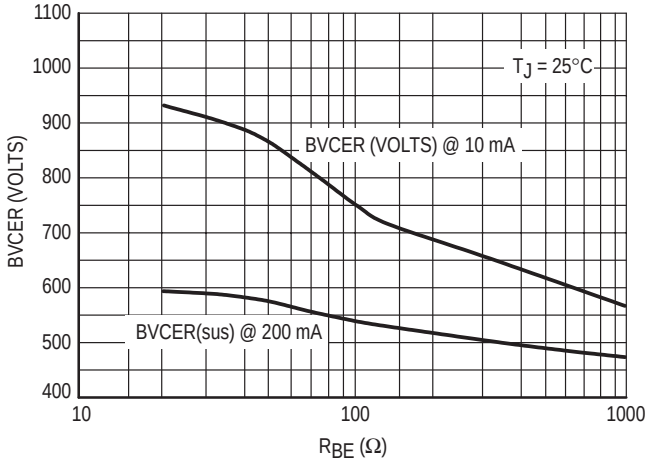


Figure 27. BVCER

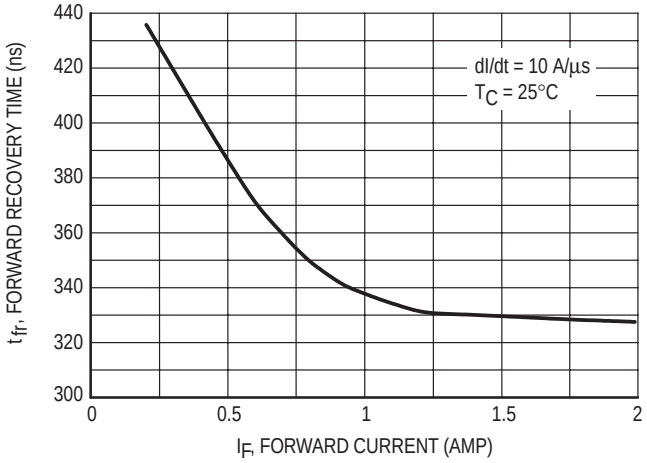


Figure 28. Forward Recovery Time t_{fr}

BUL45*
BUL45F*

*Motorola Preferred Device

Designer's™ Data Sheet

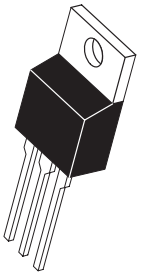
NPN Silicon Power Transistor

High Voltage SWITCHMODE™ Series

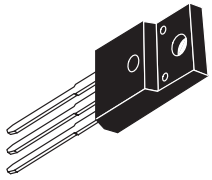
POWER TRANSISTOR
5.0 AMPERES
700 VOLTS
35 and 75 WATTS

Designed for use in electronic ballast (light ballast) and in Switchmode Power supplies up to 50 Watts. Main features include:

- Improved Efficiency Due to:
  - — Low Base Drive Requirements (High and Flat DC Current Gain h_{FE})
  - — Low Power Losses (On–State and Switching Operations)
  - — Fast Switching: t_{fi} = 100 ns (typ) and t_{si} = 3.2 µs (typ) @ I_C = 2.0 A, I_{B1} = I_{B2} = 0.4 A
- Full Characterization at 125°C
- Tight Parametric Distributions Consistent Lot–to–Lot
- BUL45F, Case 221D, is UL Recognized at 3500 V_{RMS}: File #E69369



BUL45
CASE 221A–06
TO–220AB



BUL45F
CASE 221D–02
ISOLATED TO–220 TYPE
UL RECOGNIZED

MAXIMUM RATINGS

Rating	Symbol	BUL45	BUL45F	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700		Vdc
Emitter–Base Voltage	V_{EBO}	9.0		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	5.0 10		Adc
Base Current	I_B	2.0		Adc
RMS Isolated Voltage(2) Test No. 1 Per Fig. 22a (for 1 sec, R.H. < 30%, Test No. 2 Per Fig. 22b T_C = 25°C) Test No. 3 Per Fig. 22c	V_{ISOL}	— — —	4500 3500 1500	Volts
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	75 0.6	35 0.28	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	– 65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18006	MJF18006	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	3.55 62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	µAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0) (T_C = 125°C)	I_{CES}	— —	— —	10 100	µAdc
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	µAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

(continued)

(2) Proper strike and creepage distance must be provided.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS								
Base–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc) (I_C = 2.0 Adc, I_B = 0.4 Adc)				$V_{BE(sat)}$	— —	0.84 0.89	1.2 1.25	Vdc
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc) (T_C = 125°C)				$V_{CE(sat)}$	— —	0.175 0.150	0.25 —	Vdc
Collector–Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.4 Adc) (T_C = 125°C)				$V_{CE(sat)}$	— —	0.25 0.275	0.4 —	Vdc
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 5.0 Vdc) (T_C = 125°C) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc) (T_C = 125°C) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)				h_{FE}	14 — 7.0 5.0 10	— 32 14 12 22	34 — — — —	—
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)				f_T	—	12	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)				C_{ob}	—	50	75	pF
Input Capacitance (V_{EB} = 8.0 Vdc)				C_{ib}	—	920	1200	pF
Dynamic Saturation Voltage: Determined 1.0 µs and 3.0 µs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18)	(I_C = 1.0 Adc I_{B1} = 100 mAdc V_{CC} = 300 V)	1.0 µs	(T_C = 125°C)	V_{CE} (Dyn sat)	— —	1.75 4.4	— —	Vdc
		3.0 µs	(T_C = 125°C)		— —	0.5 1.0	— —	
	(I_C = 2.0 Adc I_{B1} = 400 mAdc V_{CC} = 300 V)	1.0 µs	(T_C = 125°C)		— —	1.85 6.0	— —	
		3.0 µs	(T_C = 125°C)		— —	0.5 1.0	— —	
SWITCHING CHARACTERISTICS: Resistive Load								
Turn–On Time	(I_C = 2.0 Adc, I_{B1} = I_{B2} = 0.4 Adc Pulse Width = 20 µs, Duty Cycle < 20% V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	— —	75 120	110 —	ns
Turn–Off Time			(T_C = 125°C)	t_{off}	— —	2.8 3.5	3.5 —	µs
SWITCHING CHARACTERISTICS: Inductive Load (V_{CC} = 15 Vdc, L_C = 200 µH, V_{clamp} = 300 Vdc)								
Fall Time	(I_C = 2.0 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc)		(T_C = 125°C)	t_{fi}	70 —	— 200	170 —	ns
Storage Time			(T_C = 125°C)	t_{si}	2.6 —	— 4.2	3.8 —	µs
Crossover Time			(T_C = 125°C)	t_c	— —	230 400	350 —	ns
Fall Time	(I_C = 1.0 Adc, I_{B1} = 100 mAdc I_{B2} = 0.5 Adc)		(T_C = 125°C)	t_{fi}	— —	110 100	150 —	ns
Storage Time			(T_C = 125°C)	t_{si}	— —	1.1 1.5	1.7 —	µs
Crossover Time			(T_C = 125°C)	t_c	— —	170 170	250 —	ns
Fall Time	(I_C = 2.0 Adc, I_{B1} = 250 mAdc I_{B2} = 2.0 Adc)		(T_C = 125°C)	t_{fi}	—	80	120	ns
Storage Time			(T_C = 125°C)	t_{si}	—	0.6	0.9	µs
Crossover Time			(T_C = 125°C)	t_c	—	175	300	ns

TYPICAL STATIC CHARACTERISTICS

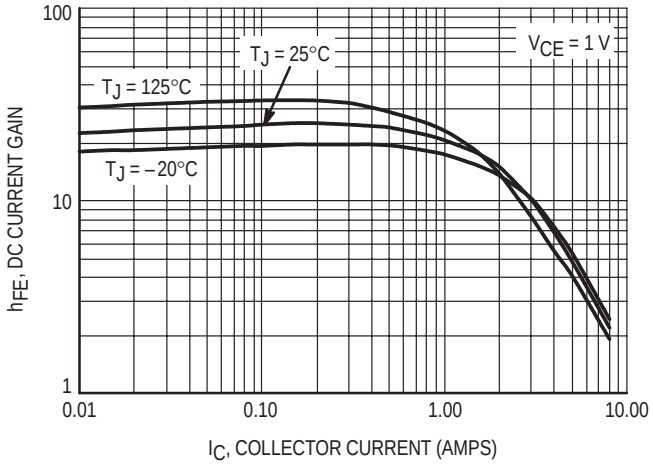


Figure 1. DC Current Gain @ 1 Volt

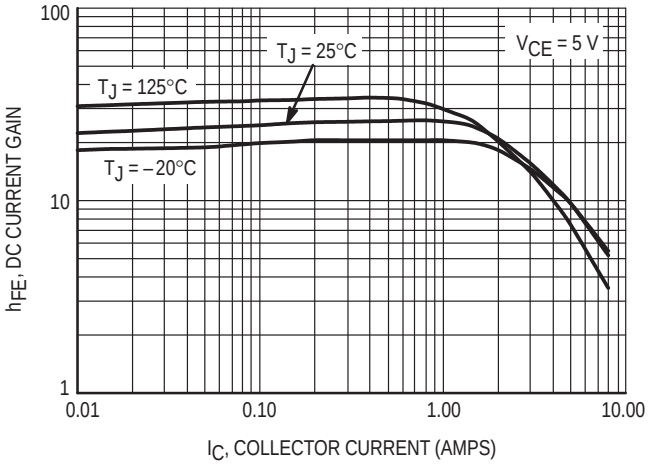


Figure 2. DC Current Gain at @ 5 Volts

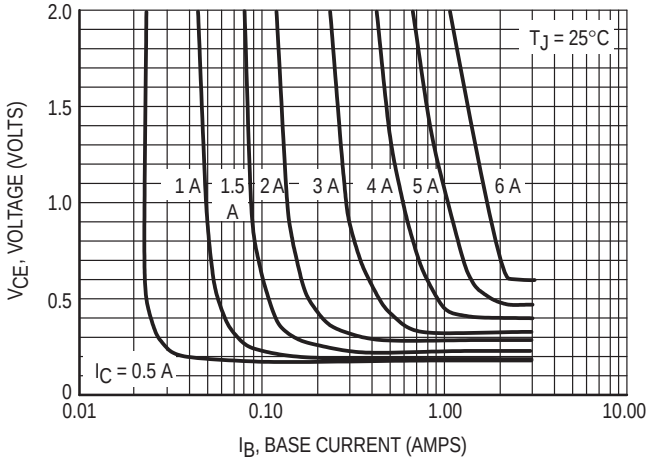


Figure 3. Collector–Emitter Saturation Region

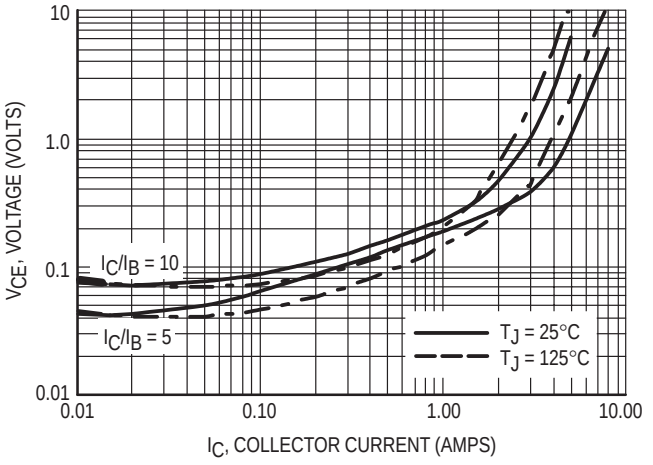


Figure 4. Collector–Emitter Saturation Voltage

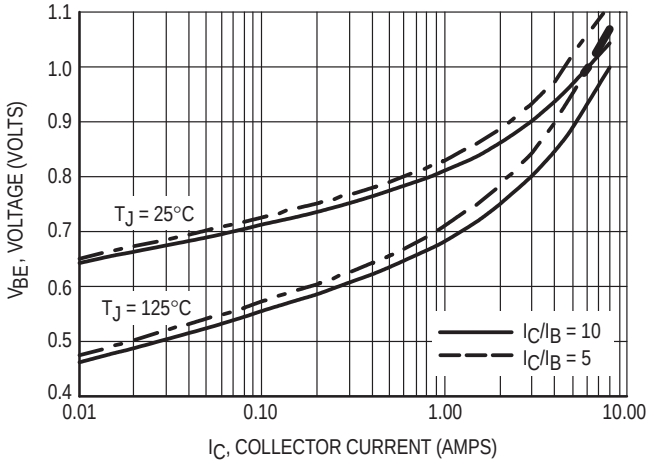


Figure 5. Base–Emitter Saturation Region

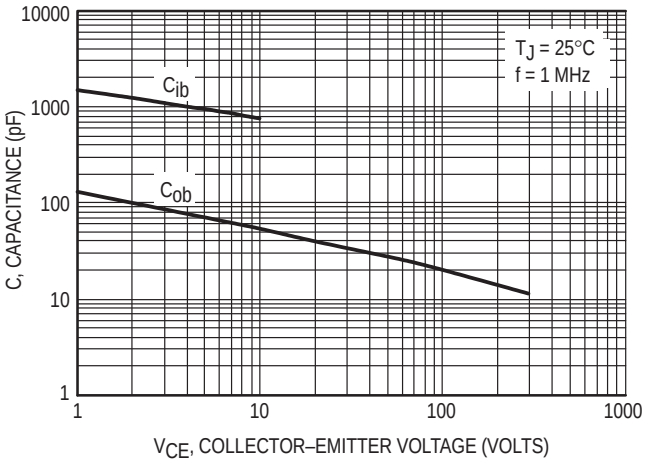


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

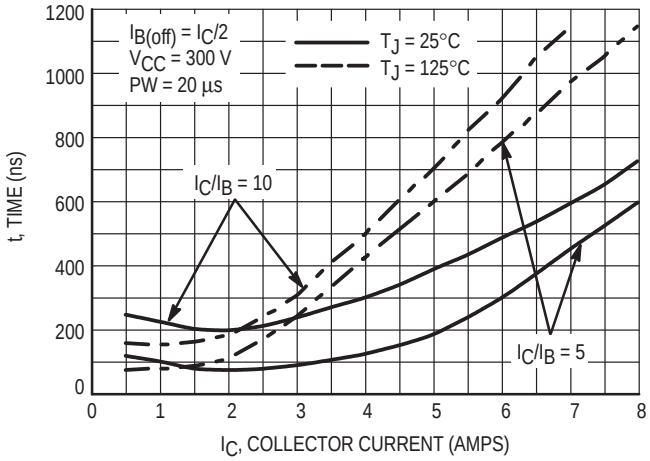


Figure 7. Resistive Switching, t_{on}

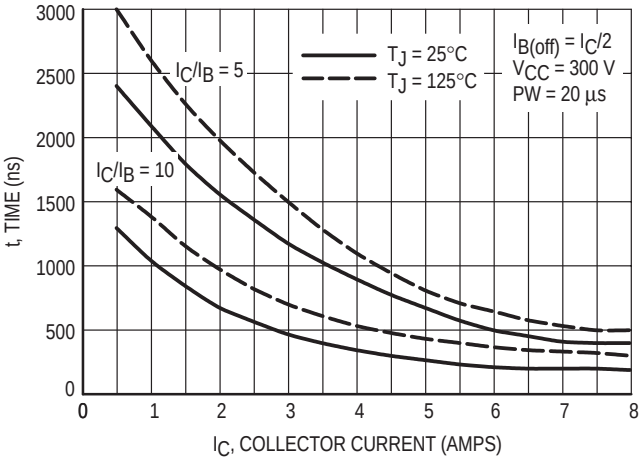


Figure 8. Resistive Switching, t_{off}

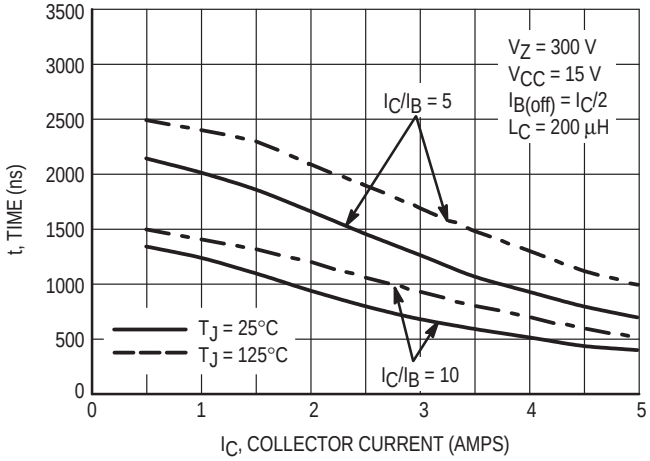


Figure 9. Inductive Storage Time, t_{si}

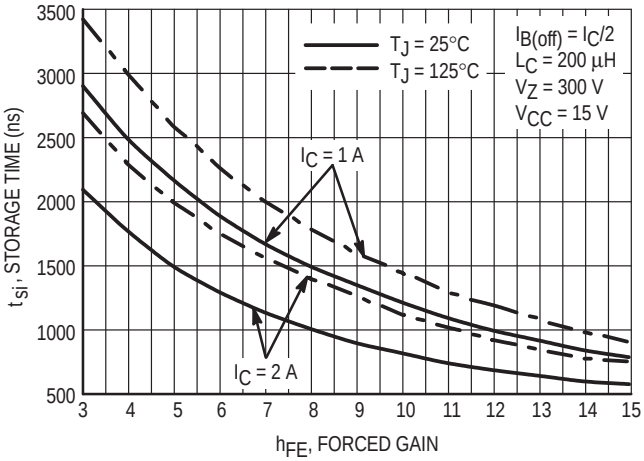


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

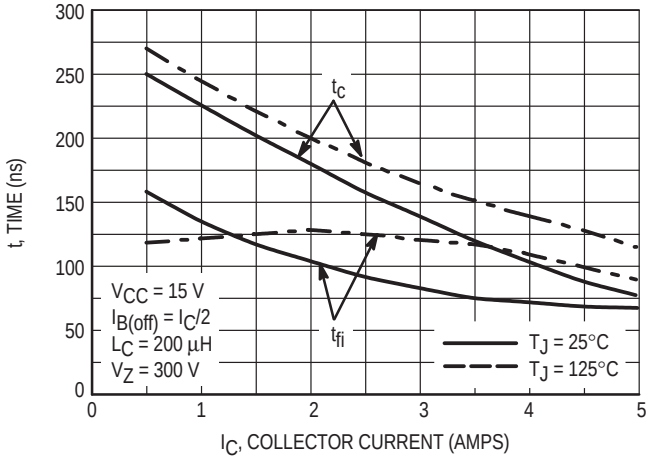


Figure 11. Inductive Switching, t_c & t_{fi}, $I_C/I_B = 5$

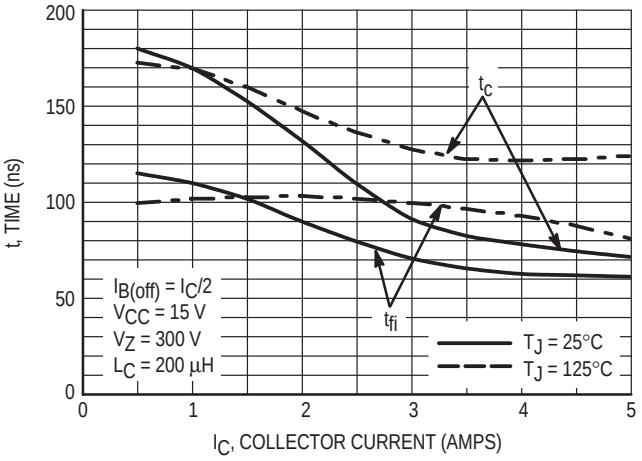


Figure 12. Inductive Switching, t_c & t_{fi}, $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

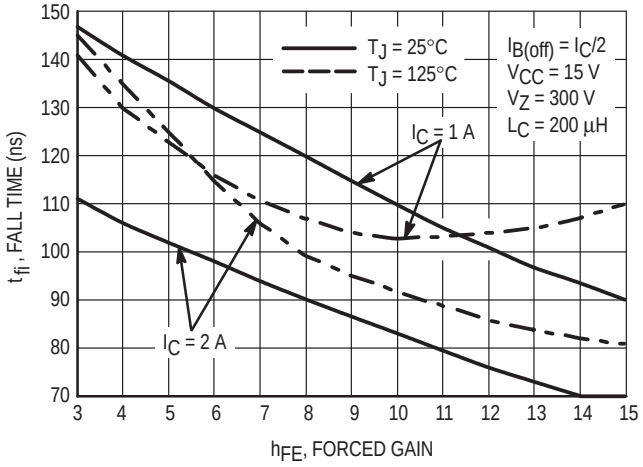


Figure 13. Inductive Fall Time, $t_{fi}(h_{FE})$

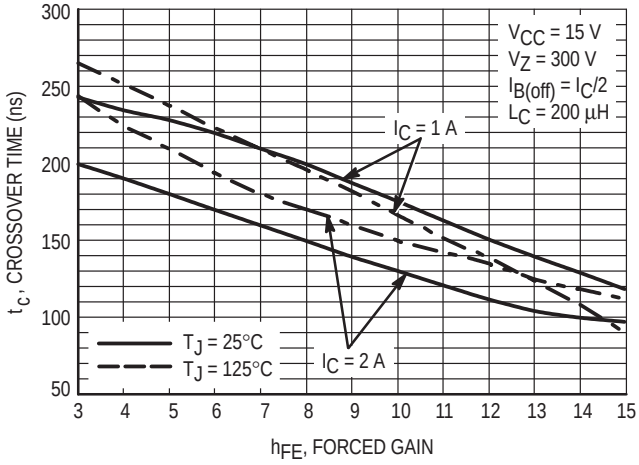


Figure 14. Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

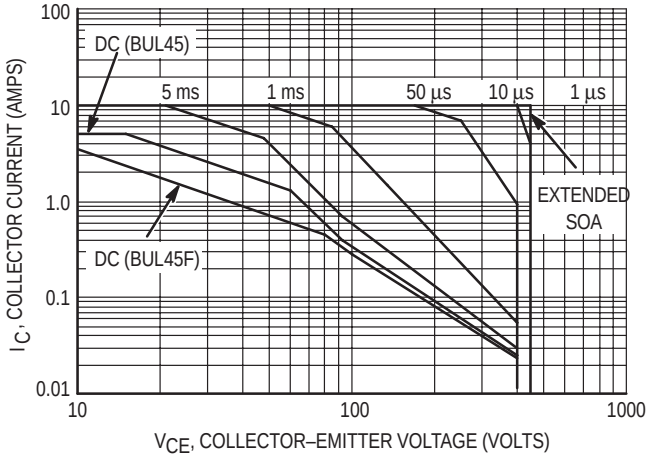


Figure 15. Forward Bias Safe Operating Area

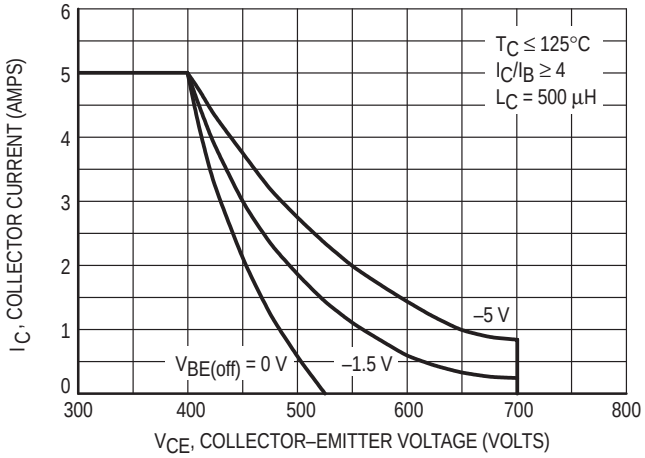


Figure 16. Reverse Bias Switching Safe Operating Area

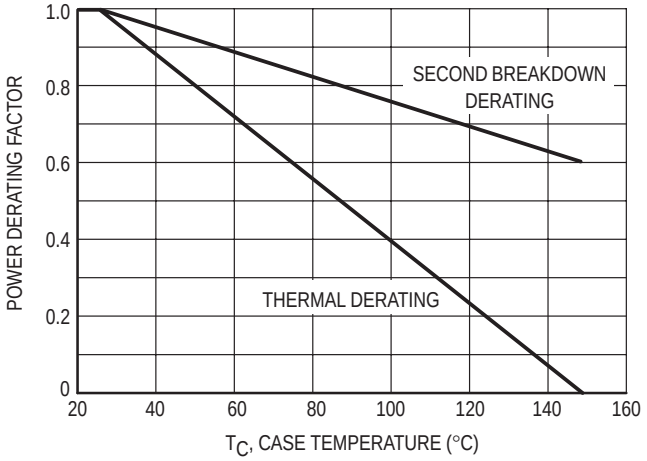


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figures 20 and 21. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse–biased. The safe level is specified as a reverse–biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

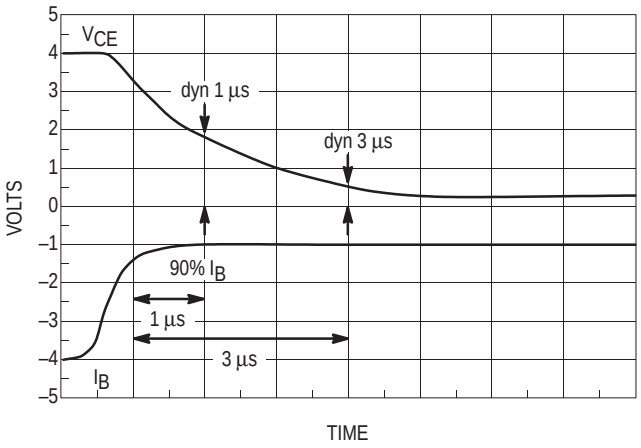


Figure 18. Dynamic Saturation Voltage Measurements

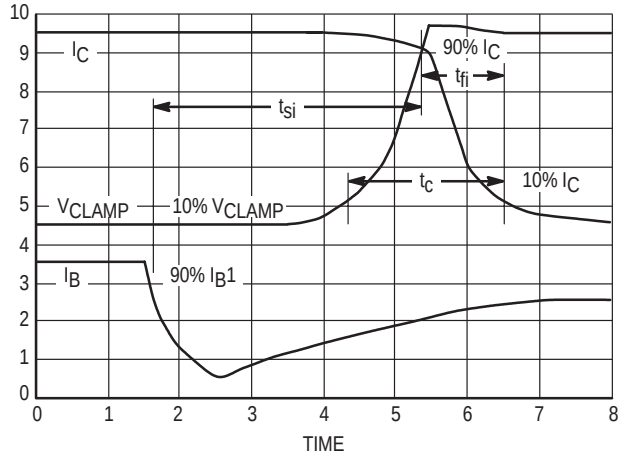
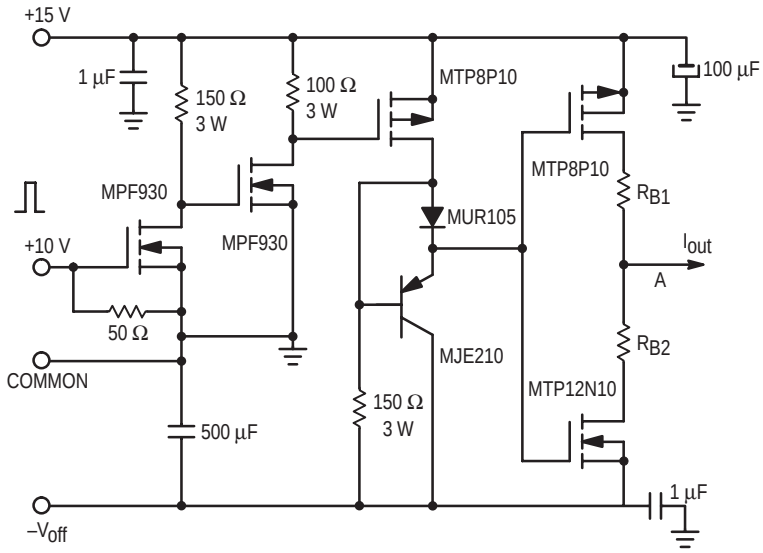
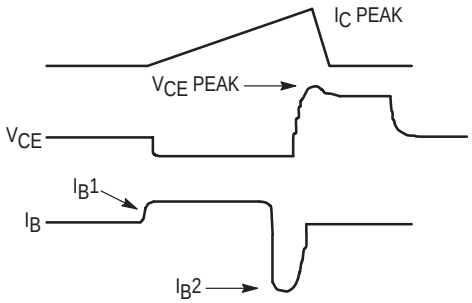


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 µH	L = 500 µH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_B1	RB1 SELECTED FOR DESIRED I_B1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

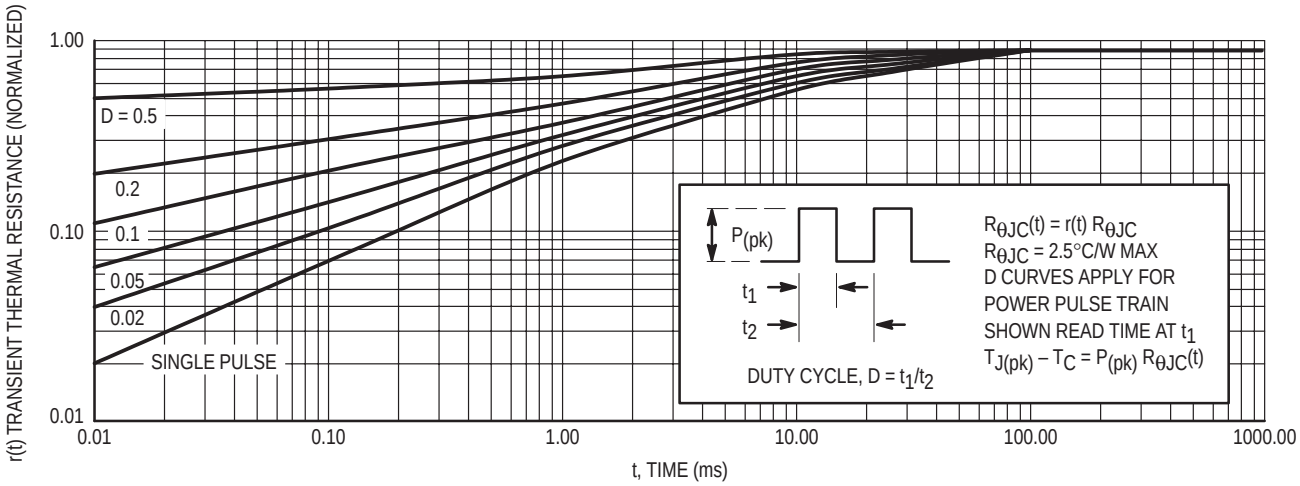


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL45

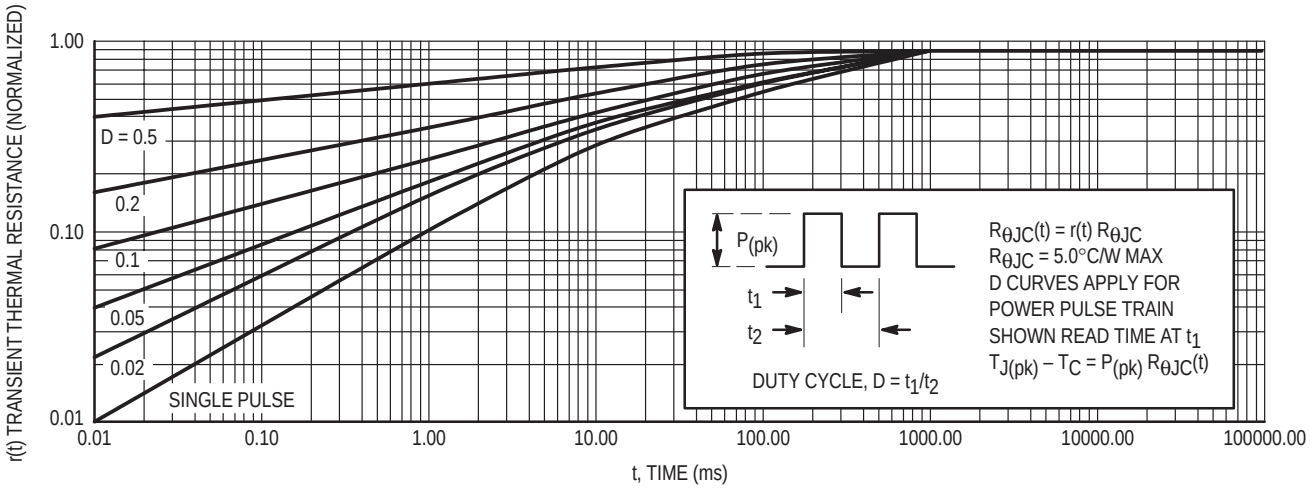
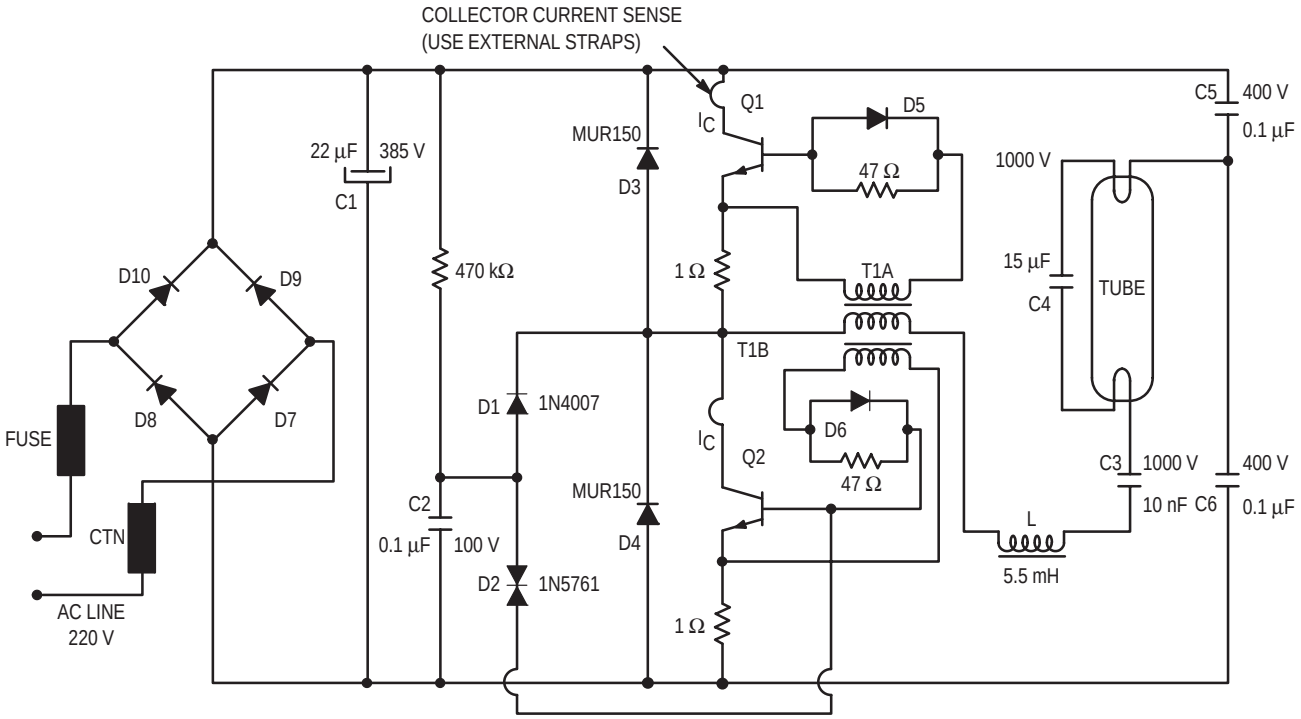


Figure 21. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL45F

The BUL45/BUL45F Bipolar Power Transistors were specially designed for use in electronic lamp ballasts. A circuit designed by Motorola applications was built to demonstrate how well these devices operate. The circuit and detailed component list are provided below.



Components Lists

Q1 = Q2 = BUL45 Transistor
D1 = 1N4007 Rectifier
D2 = 1N5761 Rectifier
D3 = D4 = MUR150
D5 = D6 = MUR105
D7 = D8 = D9 = D10 = 1N400
CTN = 47 Ω @ 25°C
L = RM10 core, A1 = 400, B51 (LCC) 75 turns, wire ∅ = 0.6 mm
T1 = FT10 toroid, T4A (LCC)
Primary: 4 turns
Secondaries: T1A: 4 turns
T1B: 4 turns

All resistors are 1/4 Watt, ±5%
R1 = 470 kΩ
R2 = R3 = 47 Ω
R4 = R5 = 1 Ω (these resistors are optional, and might be replaced by a short circuit)
C1 = 22 μF/385 V
C2 = 0.1 μF
C3 = 10 nF/1000 V
C4 = 15 nF/1000 V
C5 = C6 = 0.1 μF/400 V

NOTES:
1. Since this design does not include the line input filter, it cannot be used “as–is” in a practical industrial circuit.
2. The windings are given for a 55 Watt load. For proper operation they must be re–calculated with any other loads.

Figure 22. Application Example

TEST CONDITIONS FOR ISOLATION TESTS*

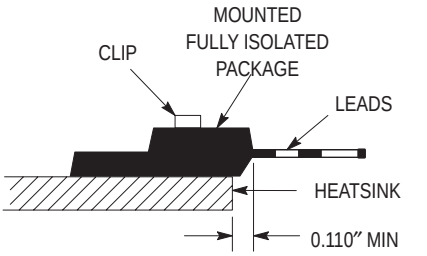


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

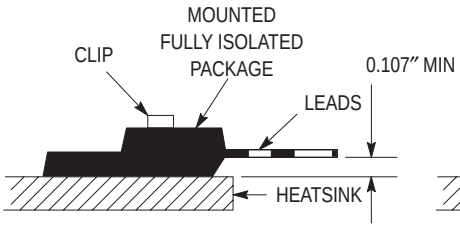


Figure 22b. Clip Mounting Position for Isolation Test Number 2

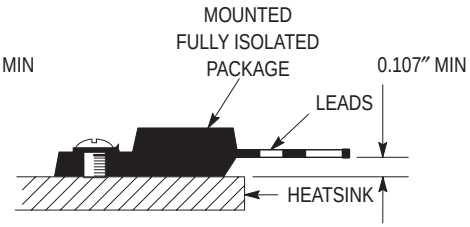


Figure 22c. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together.

MOUNTING INFORMATION**

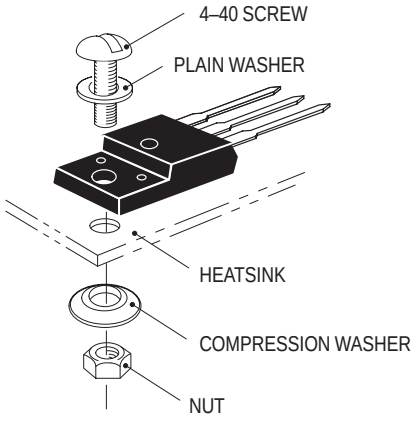


Figure 23a. Screw–Mounted

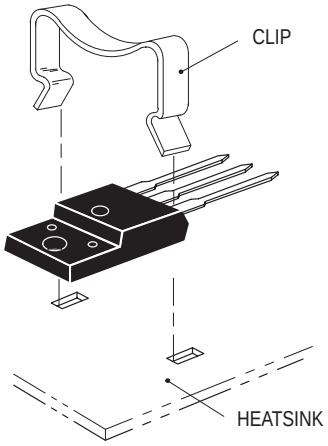


Figure 23b. Clip–Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

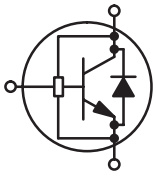
** For more information about mounting power semiconductors see Application Note AN1040.

BUL45D2

Designer's™ Data Sheet

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

POWER TRANSISTORS
5 AMPERES
700 VOLTS
75 WATTS

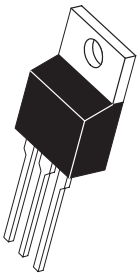


The BUL45D2 is state–of–art High Speed High gain BIPolar transistor (H2BIP). High dynamic characteristics and lot to lot minimum spread (±150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an h_{FE} window.

Main features:

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ I_C = 100 mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector–Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic $V_{CE(sat)}$
- "6 Sigma" Process Providing Tight and Reproductible Parameter Spreads

It's characteristics make it also suitable for PFC application.



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter–Base Voltage	V_{EBO}	12	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5 10	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	75 0.6	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.65 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	400	450		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)		V_{CBO}	700	910		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)		V_{EBO}	12	14.1		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C	I_{CES}			100	μAdc
	@ T_C = 125°C				500	
(V_{CE} = 500 V, V_{EB} = 0)	@ T_C = 125°C				100	
Emitter–Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)	@ T_C = 25°C	$V_{BE(sat)}$		0.8	1	Vdc
	@ T_C = 125°C			0.7	0.9	
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C			0.89	1	
	@ T_C = 125°C			0.79	0.9	
Collector–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)	@ T_C = 25°C	$V_{CE(sat)}$		0.28	0.4	Vdc
	@ T_C = 125°C			0.32	0.5	
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C			0.32	0.5	
	@ T_C = 125°C			0.38	0.6	
(I_C = 0.8 Adc, I_B = 40 mAdc)	@ T_C = 25°C			0.46	0.75	
	@ T_C = 125°C			0.62	1	
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C	h_{FE}	22	34		—
	@ T_C = 125°C		20	29		
(I_C = 2 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C		10	14		
	@ T_C = 125°C		7	9.5		
DIODE CHARACTERISTICS						
Forward Diode Voltage (I_{EC} = 1 Adc)	@ T_C = 25°C	V_{EC}		1.04	1.5	V
	@ T_C = 125°C			0.7		
(I_{EC} = 2 Adc)	@ T_C = 25°C			1.2	1.6	
	@ T_C = 125°C					
(I_{EC} = 0.4 Adc)	@ T_C = 25°C			0.85	1.2	
	@ T_C = 125°C			0.62		
Forward Recovery Time (see Figure 27) (I_F = 1 Adc, di/dt = 10 A/μs)	@ T_C = 25°C	T_{fr}		330		ns
(I_F = 2 Adc, di/dt = 10 A/μs)	@ T_C = 25°C			360		
(I_F = 0.4 Adc, di/dt = 10 A/μs)	@ T_C = 25°C			320		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)				f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)				C_{ob}		50	75	pF
Input Capacitance (V_{EB} = 8 Vdc)				C_{ib}		340	500	pF
DYNAMIC SATURATION VOLTAGE								
Dynamic Saturation Voltage: Determined 1 µs and 3 µs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1 A, I_{B1} = 100 mA, V_{CC} = 300 V	@ 1 µs	@ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$		3.7 9.4		V
		@ 3 µs	@ T_C = 25°C @ T_C = 125°C			0.35 2.7		V
	I_C = 2 A, I_{B1} = 0.8 A, V_{CC} = 300 V	@ 1 µs	@ T_C = 25°C @ T_C = 125°C			3.9 12		V
		@ 3 µs	@ T_C = 25°C @ T_C = 125°C			0.4 1.5		V
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 µs)								
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc, I_{B2} = 1 Adc, V_{CC} = 300 Vdc		@ T_C = 25°C @ T_C = 125°C	t_{on}		90 105	150	ns
Turn–off Time			@ T_C = 25°C @ T_C = 125°C	t_{off}		1.15 1.5	1.3	µs
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc, I_{B2} = 0.4 Adc, V_{CC} = 300 Vdc		@ T_C = 25°C @ T_C = 125°C	t_{on}		90 110	150	ns
Turn–off Time			@ T_C = 25°C @ T_C = 125°C	t_{off}	2.1	 3.1	2.4	µs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 µH)								
Fall Time	I_C = 1 Adc, I_{B1} = 100 mAdc, I_{B2} = 500 mAdc		@ T_C = 25°C @ T_C = 125°C	t_f		90 93	150	ns
Storage Time			@ T_C = 25°C @ T_C = 125°C	t_s		0.72 1.05	0.9	µs
Crossover Time			@ T_C = 25°C @ T_C = 125°C	t_c		95 95	150	ns
Fall Time	I_C = 2 Adc, I_{B1} = 0.4 Adc, I_{B2} = 0.4 Adc		@ T_C = 25°C @ T_C = 125°C	t_f		80 105	150	ns
Storage Time			@ T_C = 25°C @ T_C = 125°C	t_s	1.95	 2.9	2.25	µs
Crossover Time			@ T_C = 25°C @ T_C = 125°C	t_c		225 450	300	ns

TYPICAL STATIC CHARACTERISTICS

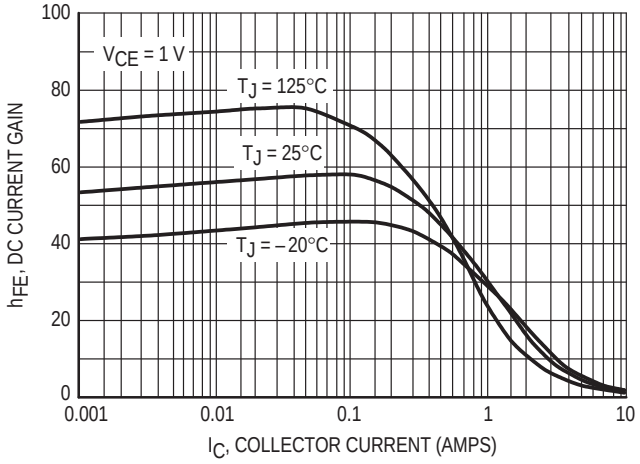


Figure 1. DC Current Gain @ 1 Volt

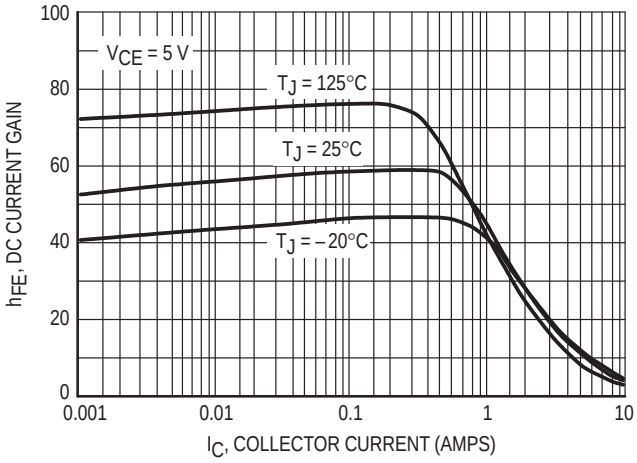


Figure 2. DC Current Gain @ 5 Volt

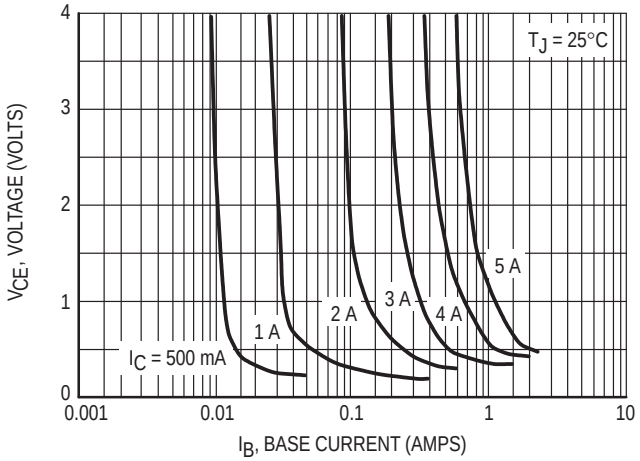


Figure 3. Collector Saturation Region

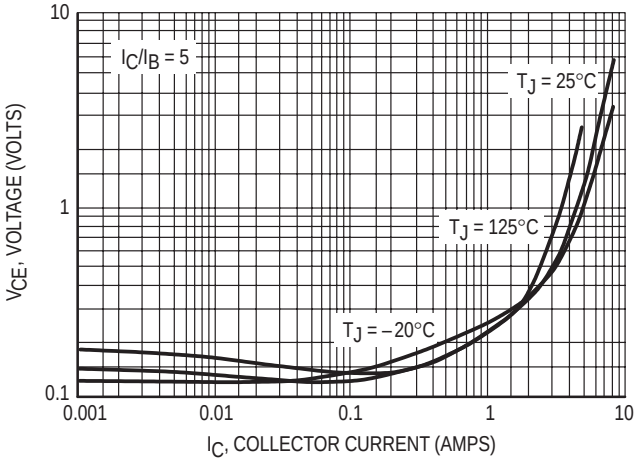


Figure 4. Collector–Emitter Saturation Voltage

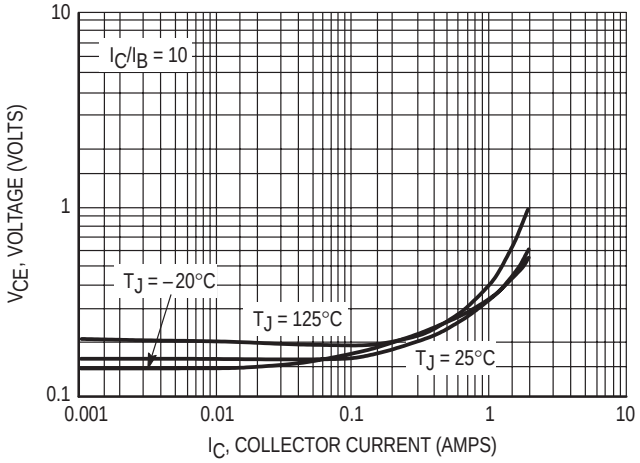


Figure 5. Collector–Emitter Saturation Voltage

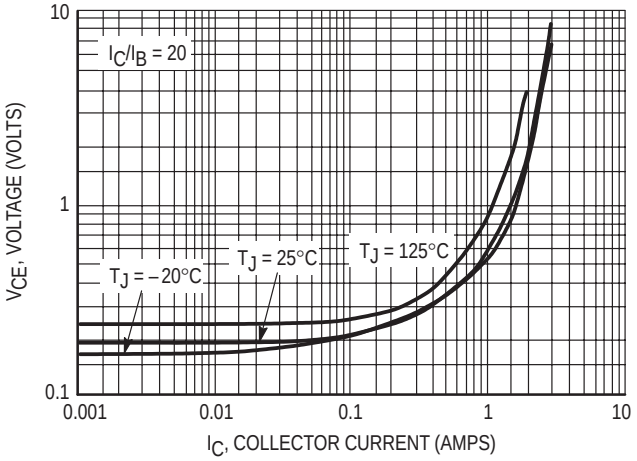


Figure 6. Collector–Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

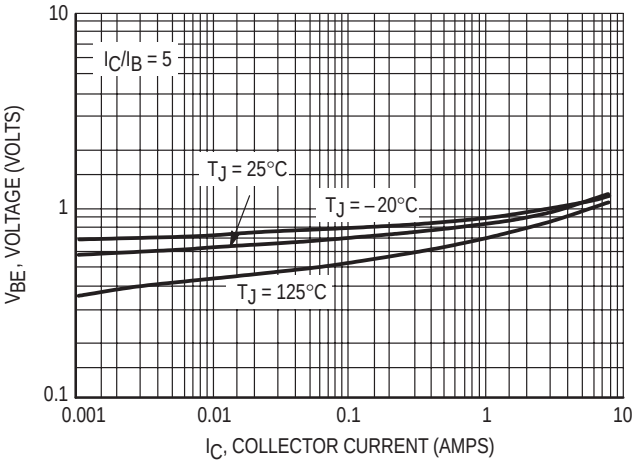


Figure 7. Base–Emitter Saturation Region

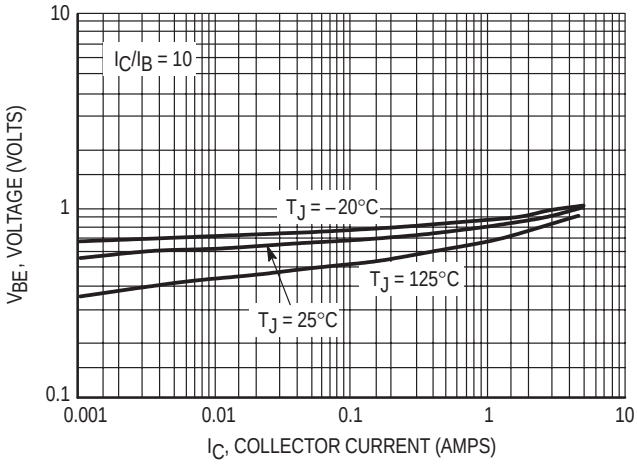


Figure 8. Base–Emitter Saturation Region

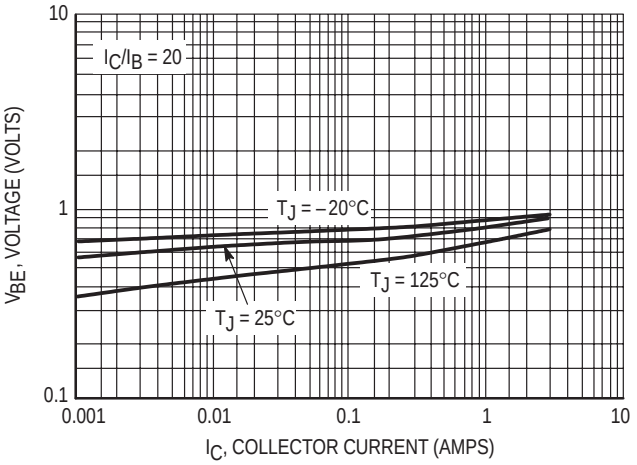


Figure 9. Base–Emitter Saturation Region

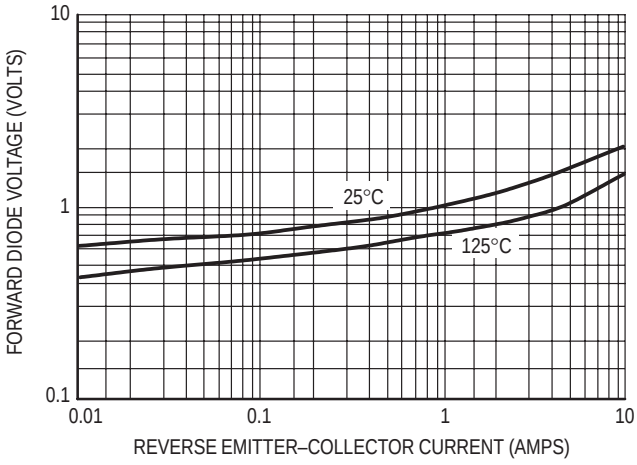


Figure 10. Forward Diode Voltage

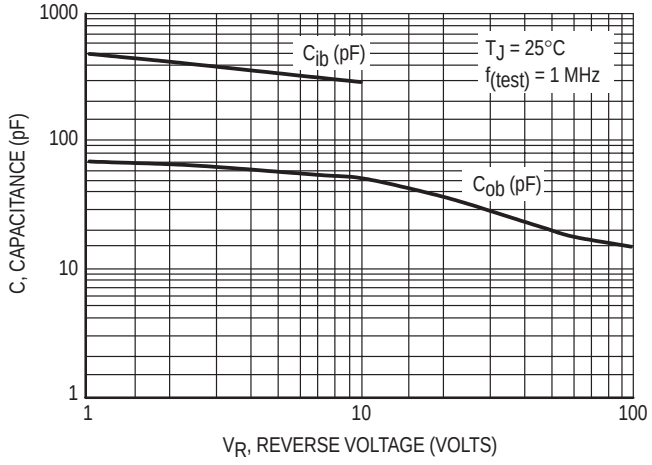


Figure 11. Capacitance

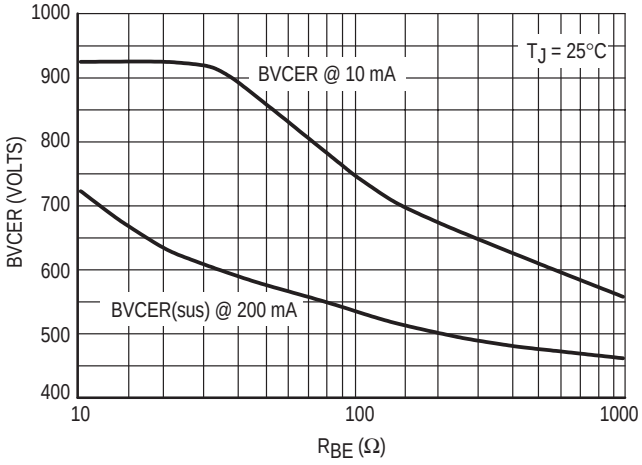


Figure 12. BVCER = f(ICER)

TYPICAL SWITCHING CHARACTERISTICS

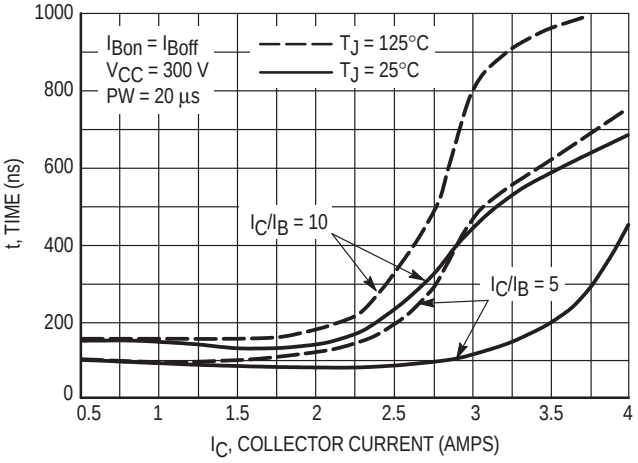


Figure 13. Resistive Switch Time, t_{on}

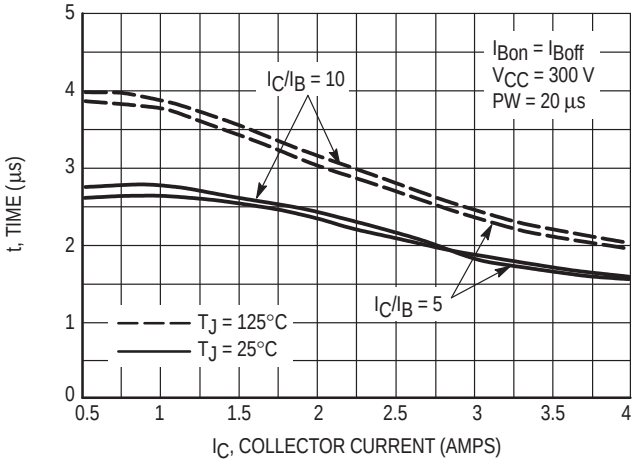


Figure 14. Resistive Switch Time, t_{off}

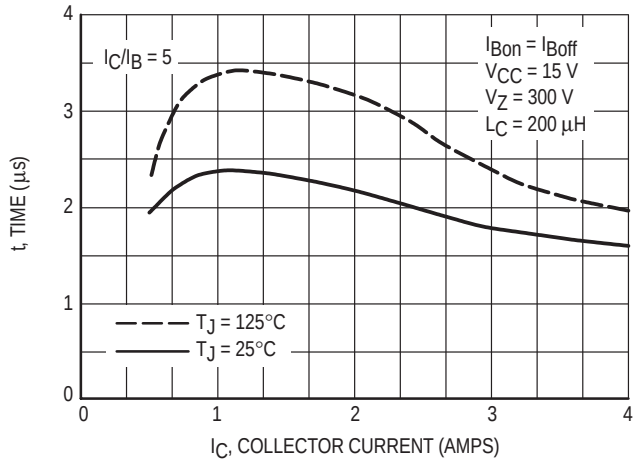


Figure 15. Inductive Storage Time, t_{si} @ I_C/I_B = 5

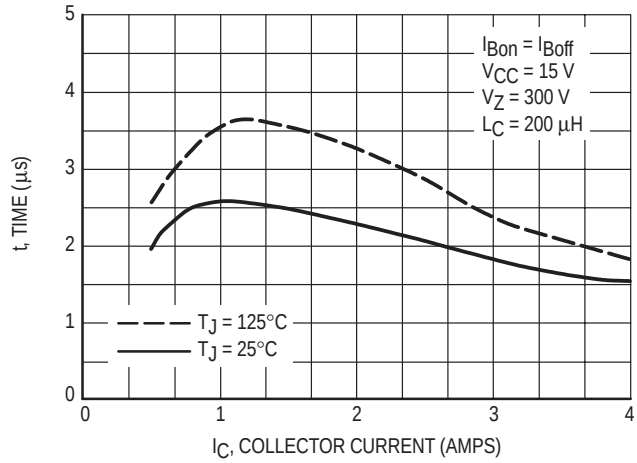


Figure 16. Inductive Storage Time, t_{si} @ I_C/I_B = 10

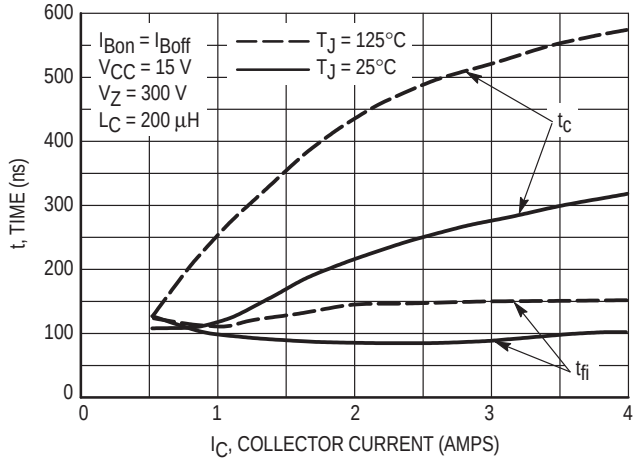


Figure 17. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 5

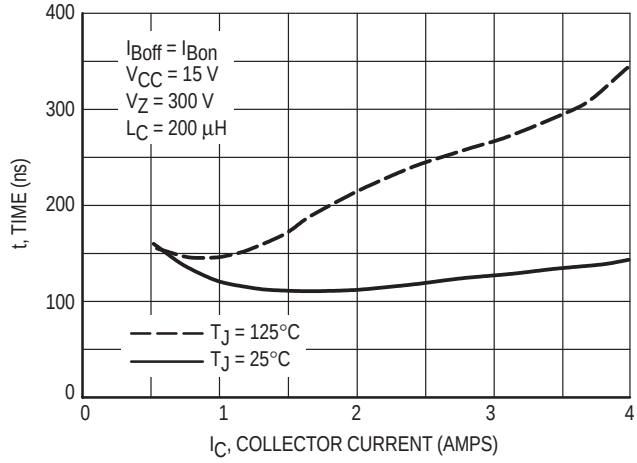


Figure 18. Inductive Switching, t_{fi} @ I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS

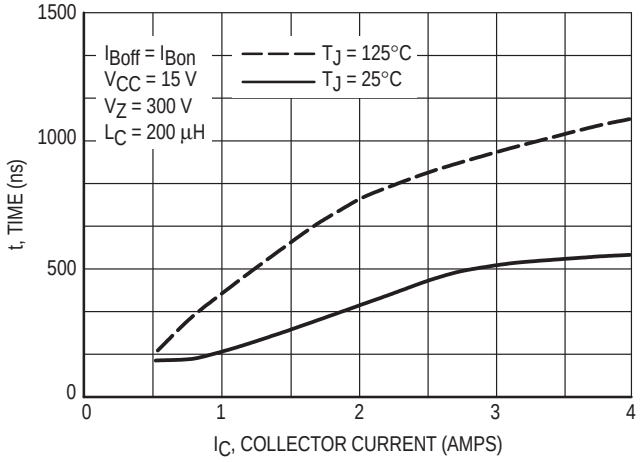


Figure 19. Inductive Switching, t_c @ $I_C/I_B = 10$

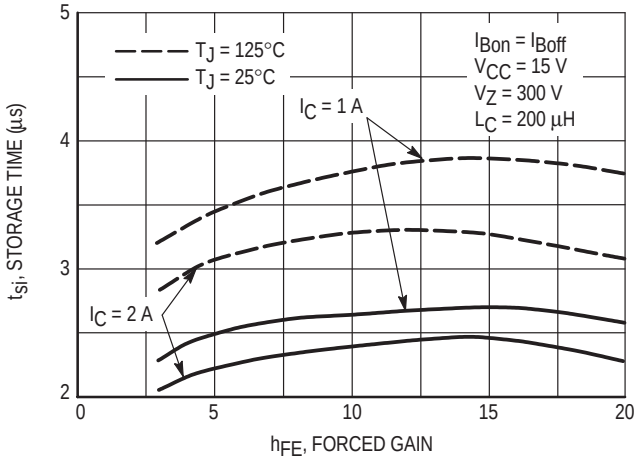


Figure 20. Inductive Storage Time

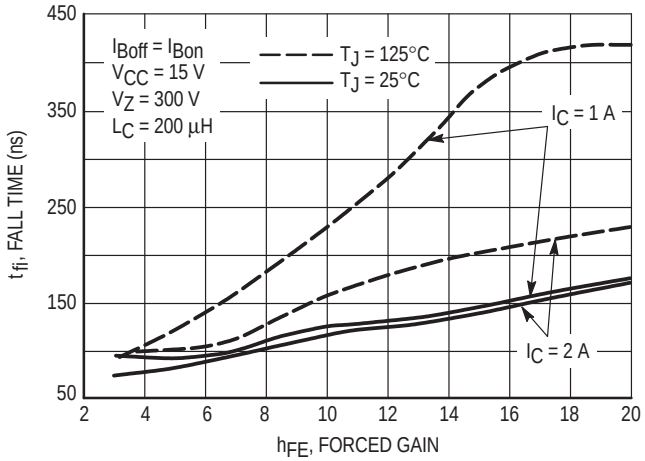


Figure 21. Inductive Fall Time

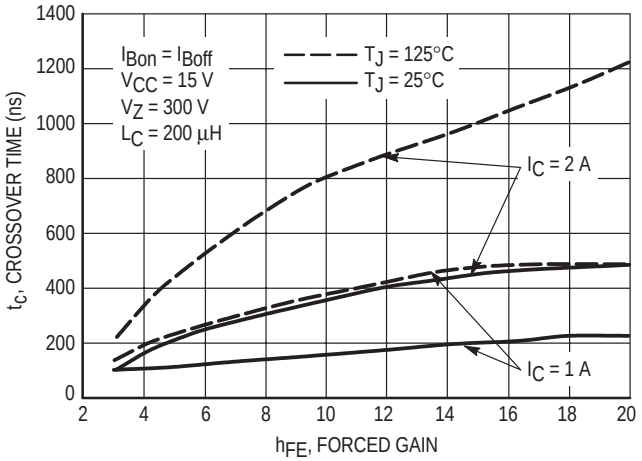


Figure 22. Inductive Crossover Time

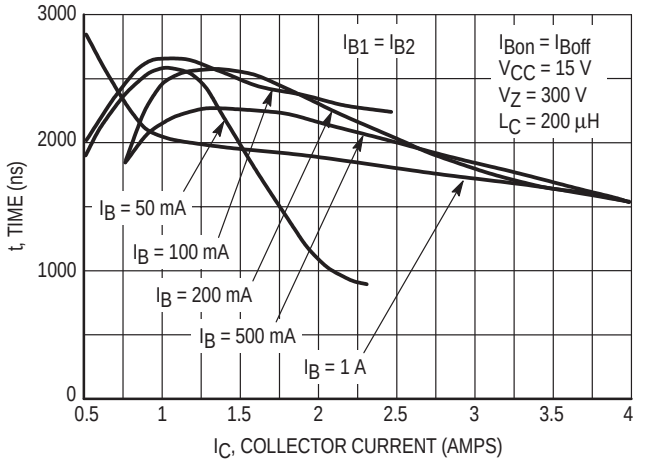


Figure 23. Inductive Storage Time, t_{si}

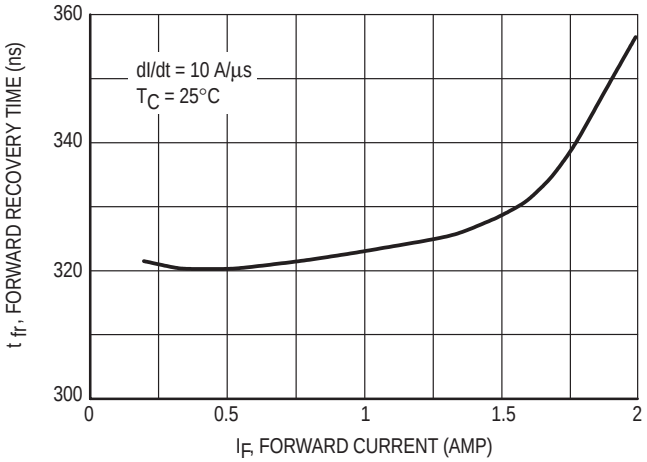


Figure 24. Forward Recovery Time t_{fr}

TYPICAL SWITCHING CHARACTERISTICS

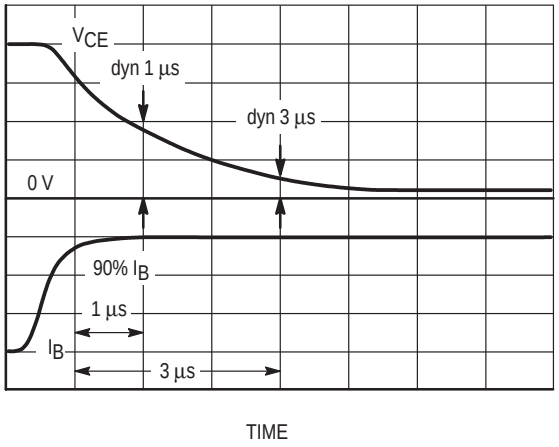


Figure 25. Dynamic Saturation Voltage Measurements

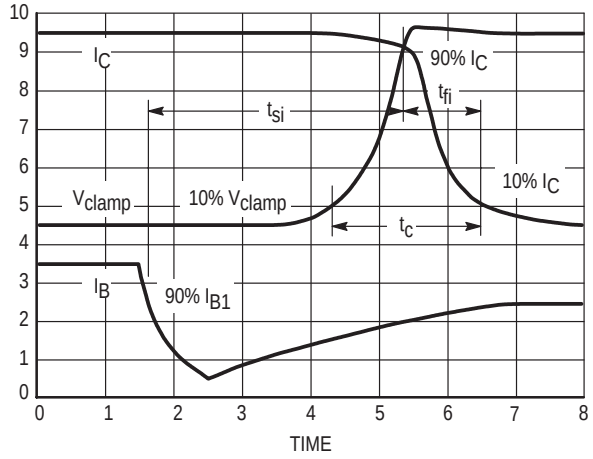


Figure 26. Inductive Switching Measurements

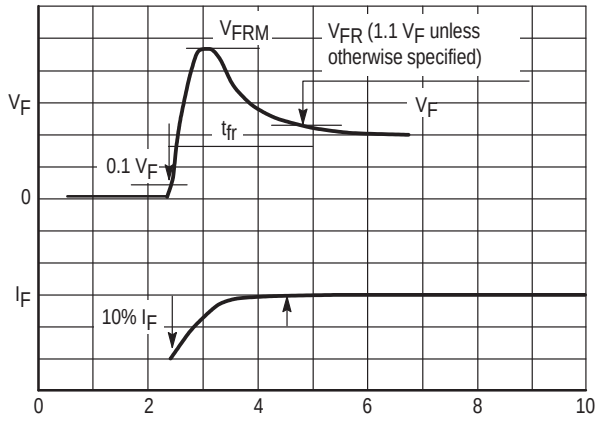
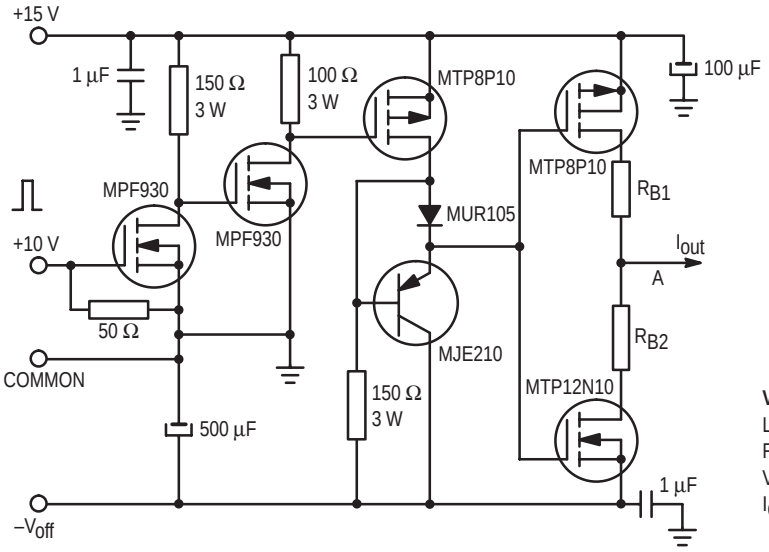
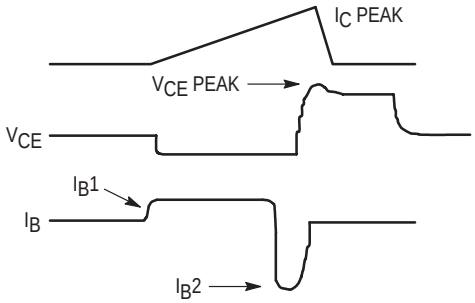


Figure 27. t_{fr} Measurements

TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL CHARACTERISTICS

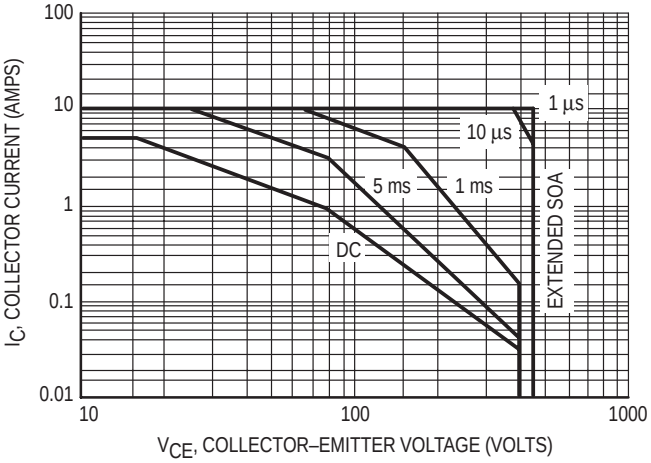


Figure 28. Forward Bias Safe Operating Area

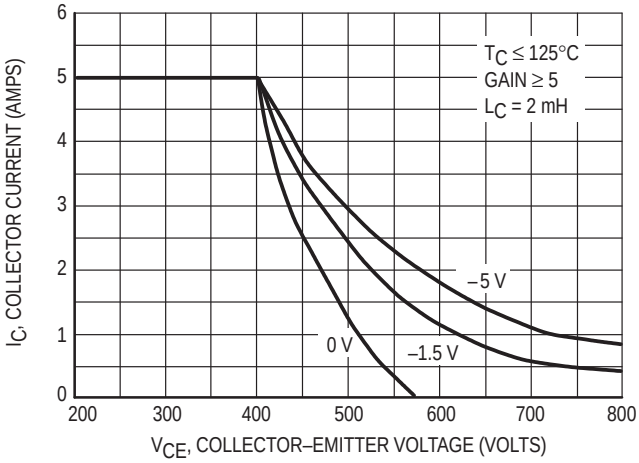


Figure 29. Reverse Bias Safe Operating Area

TYPICAL CHARACTERISTICS

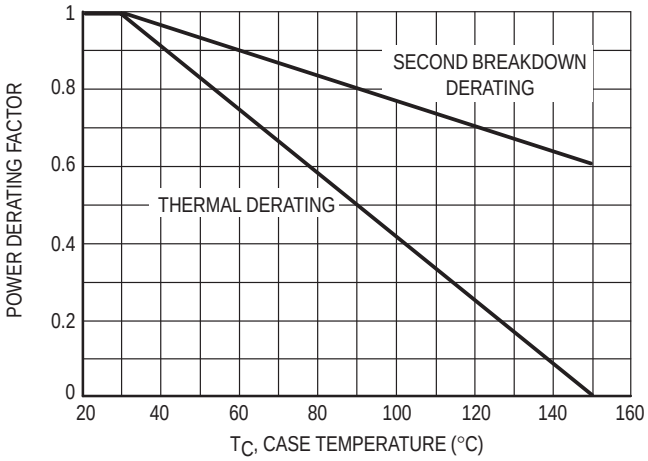


Figure 30. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

$T_{J(pk)}$ may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL THERMAL RESPONSE

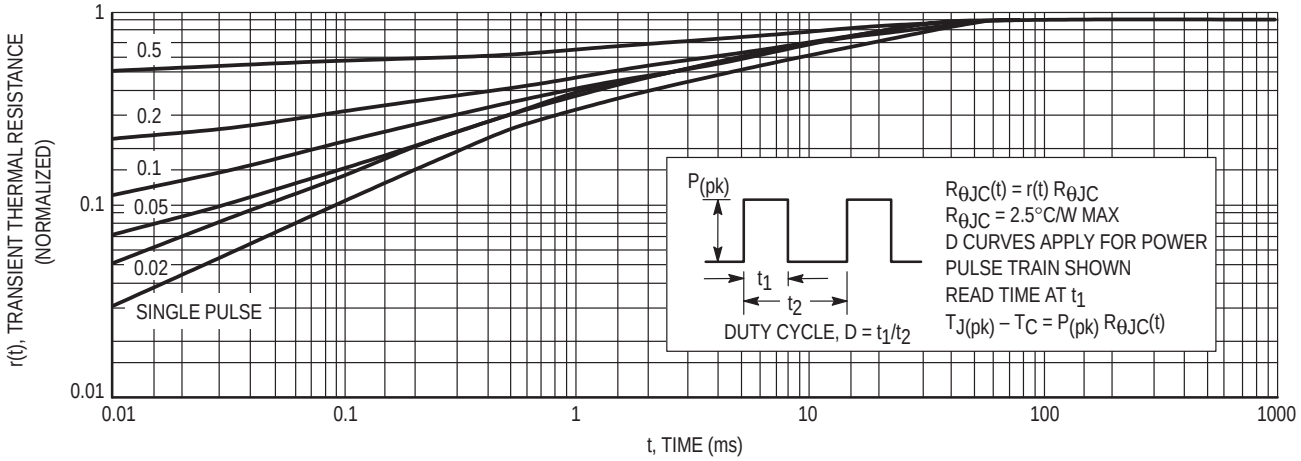


Figure 31. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL45D2

Designer's™ Data Sheet
SWITCHMODE™
NPN Bipolar Power Transistor
For Switching Power Supply Applications

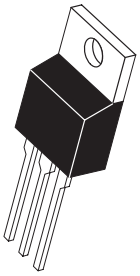
BUL146*
BUL146F*

*Motorola Preferred Device

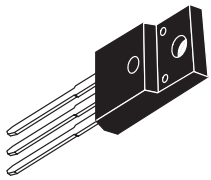
POWER TRANSISTOR
6.0 AMPERES
700 VOLTS
40 and 100 WATTS

The BUL146/BUL146F have an applications specific state–of–the–art die designed for use in fluorescent electric lamp ballasts to 130 Watts and in Switchmode Power supplies for all types of electronic equipment. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - — High and Flat DC Current Gain
  - — Fast Switching
  - — No Coil Required in Base Circuit for Turn–Off (No Current Tail)
- Full Characterization at 125°C
- Parametric Distributions are Tight and Consistent Lot–to–Lot
- Two Package Choices: Standard TO–220 or Isolated TO–220
- BUL146F, Isolated Case 221D, is UL Recognized to 3500 V_{RMS}: File #E69369



BUL146
CASE 221A–06
TO–220AB



BUL146F
CASE 221D–02
ISOLATED TO–220 TYPE
UL RECOGNIZED

MAXIMUM RATINGS

Rating	Symbol	BUL146	BUL146F	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700		Vdc
Emitter–Base Voltage	V_{EBO}	9.0		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	6.0 15		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	4.0 8.0		Adc
RMS Isolated Voltage(2) Test No. 1 Per Fig. 22a (for 1 sec, R.H. < 30%, Test No. 2 Per Fig. 22b T_C = 25°C) Test No. 3 Per Fig. 22c	V_{ISOL}	— — —	4500 3500 1500	V
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	100 0.8	40 0.32	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	– 65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	BUL44	BUL44F	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.25 62.5	3.125 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	—	—	100	μAdc
(T_C = 125°C)		—	—	500	
(V_{CE} = 500 V, V_{EB} = 0) (T_C = 125°C)		—	—	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS								
Base–Emitter Saturation Voltage	(I_C = 1.3 Adc, I_B = 0.13 Adc)			$V_{BE(sat)}$	—	0.82	1.1	Vdc
	(I_C = 3.0 Adc, I_B = 0.6 Adc)				—	0.93	1.25	
Collector–Emitter Saturation Voltage	(I_C = 1.3 Adc, I_B = 0.13 Adc)			$V_{CE(sat)}$	—	0.22	0.5	Vdc
			(T_C = 125°C)		—	0.20	0.5	
	(I_C = 3.0 Adc, I_B = 0.6 Adc)				—	0.30	0.7	
			(T_C = 125°C)		—	0.30	0.7	
DC Current Gain	(I_C = 0.5 Adc, V_{CE} = 5.0 Vdc)			h_{FE}	14	—	34	—
			(T_C = 125°C)		—	30	—	
	(I_C = 1.3 Adc, V_{CE} = 1.0 Vdc)				12	20	—	
			(T_C = 125°C)		12	20	—	
	(I_C = 3.0 Adc, V_{CE} = 1.0 Vdc)				8.0	13	—	
			(T_C = 125°C)		7.0	12	—	
	(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)				10	20	—	
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)				f_T	—	14	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)				C_{OB}	—	95	150	pF
Input Capacitance (V_{EB} = 8.0 V)				C_{IB}	—	1000	1500	pF
Dynamic Saturation Voltage: Determined 1.0 µs and 3.0 µs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18)	(I_C = 1.3 Adc I_{B1} = 300 mAdc V_{CC} = 300 V)	1.0 µs	(T_C = 125°C)	$V_{CE(dsat)}$	—	2.5	—	V
					—	6.5	—	
		3.0 µs			—	0.6	—	
			(T_C = 125°C)		—	2.5	—	
	(I_C = 3.0 Adc I_{B1} = 0.6 Adc V_{CC} = 300 V)	1.0 µs			—	3.0	—	
			(T_C = 125°C)		—	7.0	—	
		3.0 µs			—	0.75	—	
			(T_C = 125°C)		—	1.4	—	
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 µs)								
Turn–On Time	(I_C = 1.3 Adc, I_{B1} = 0.13 Adc I_{B2} = 0.65 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	—	100	200	ns
					—	90	—	
Turn–Off Time				t_{off}	—	1.35	2.5	µs
			(T_C = 125°C)		—	1.90	—	
Turn–On Time	(I_C = 3.0 Adc, I_{B1} = 0.6 Adc I_{B1} = 1.5 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	—	90	150	ns
					—	100	—	
Turn–Off Time				t_{off}	—	1.7	2.5	µs
			(T_C = 125°C)		—	2.1	—	
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 µH)								
Fall Time	(I_C = 1.3 Adc, I_{B1} = 0.13 Adc I_{B2} = 0.65 Adc)		(T_C = 125°C)	t_{fi}	—	115	200	ns
					—	120	—	
Storage Time				t_{si}	—	1.35	2.5	µs
			(T_C = 125°C)		—	1.75	—	
Crossover Time				t_c	—	200	350	ns
			(T_C = 125°C)		—	210	—	
Fall Time	(I_C = 3.0 Adc, I_{B1} = 0.6 Adc I_{B2} = 1.5 Adc)		(T_C = 125°C)	t_{fi}	—	85	150	ns
					—	100	—	
Storage Time				t_{si}	—	1.75	2.5	µs
			(T_C = 125°C)		—	2.25	—	
Crossover Time				t_c	—	175	300	ns
			(T_C = 125°C)		—	200	—	
Fall Time	(I_C = 3.0 Adc, I_{B1} = 0.6 Adc I_{B2} = 0.6 Adc)		(T_C = 125°C)	t_{fi}	80	—	180	ns
					—	210	—	
Storage Time				t_{si}	2.6	—	3.8	µs
			(T_C = 125°C)		—	4.5	—	
Crossover Time				t_c	—	230	350	ns
			(T_C = 125°C)		—	400	—	

TYPICAL STATIC CHARACTERISTICS

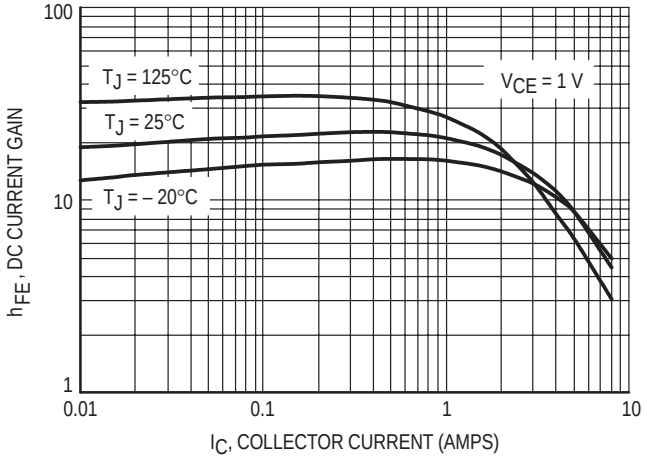


Figure 1. DC Current Gain @ 1 Volt

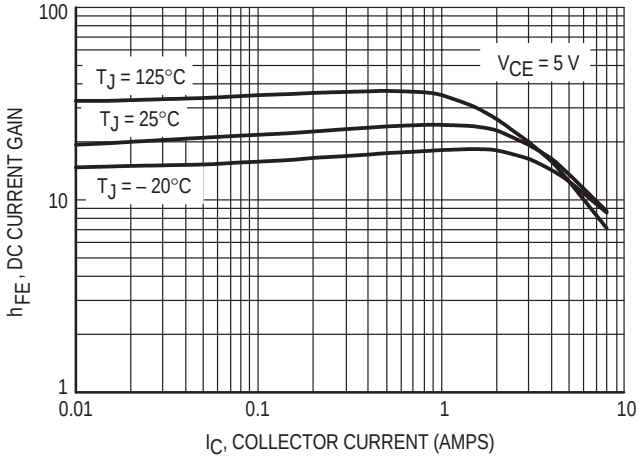


Figure 2. DC Current Gain @ 5 Volts

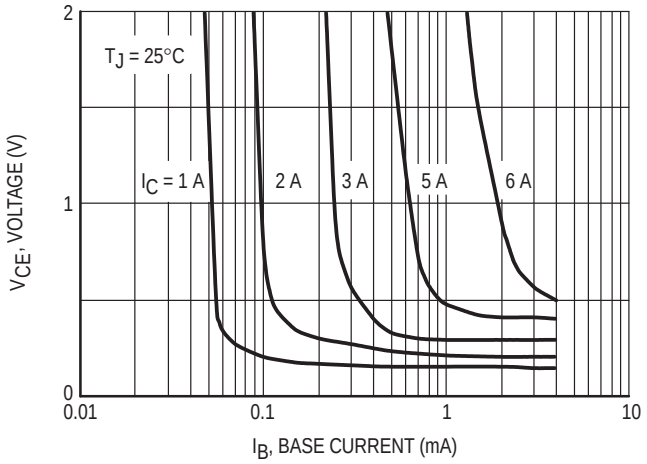


Figure 3. Collector Saturation Region

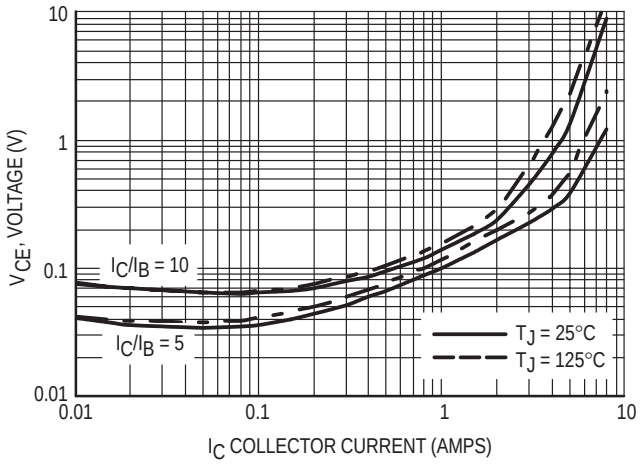


Figure 4. Collector–Emitter Saturation Voltage

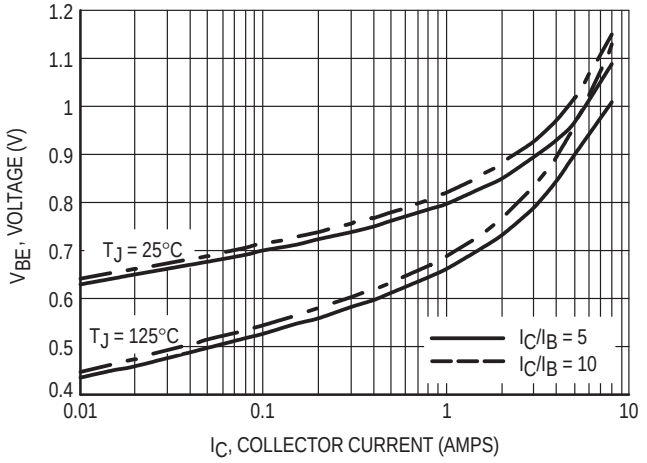


Figure 5. Base–Emitter Saturation Region

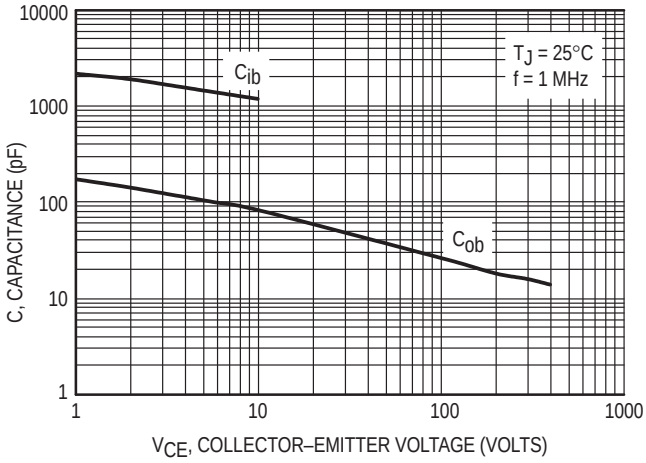


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

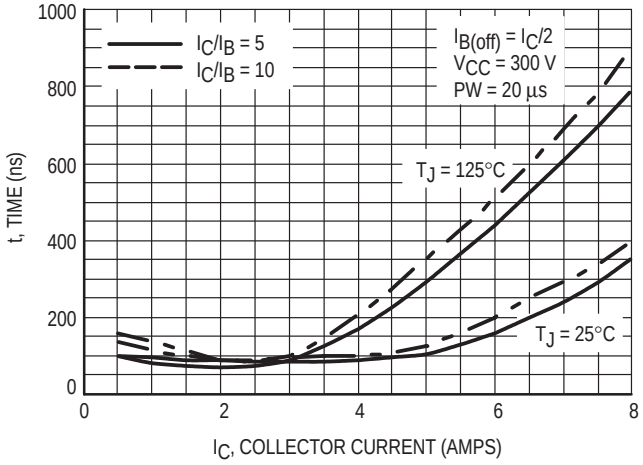


Figure 7. Resistive Switching, t_{on}

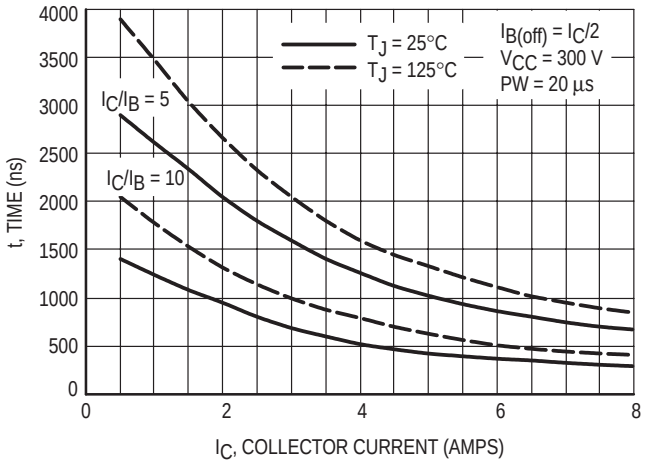


Figure 8. Resistive Switching, t_{off}

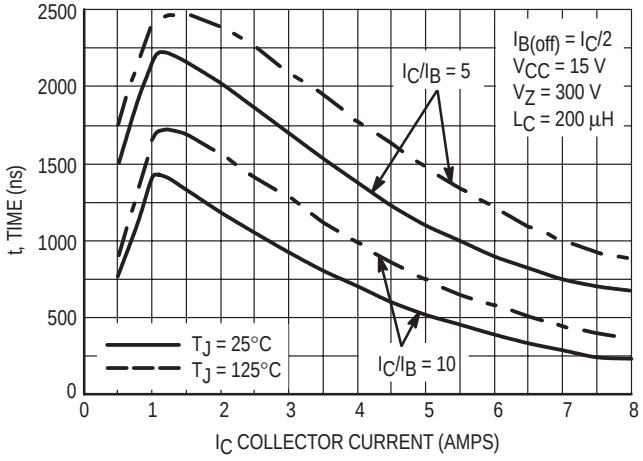


Figure 9. Inductive Storage Time, t_{si}

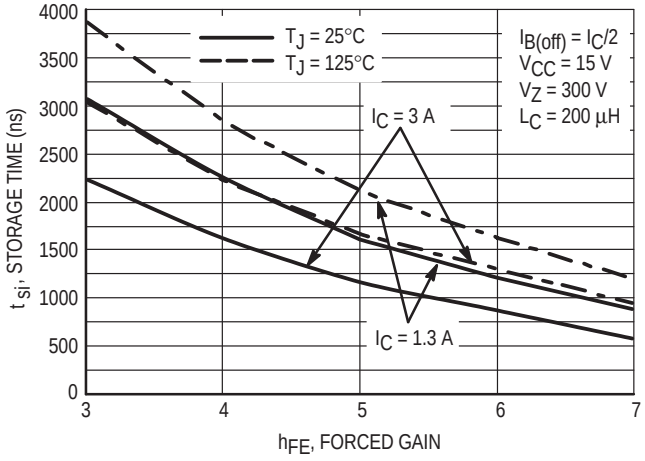


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

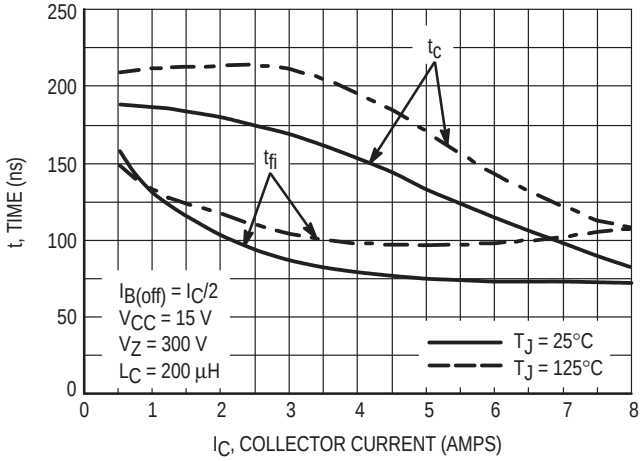


Figure 11. Inductive Switching, t_c and t_{fi}
$I_C/I_B = 5$

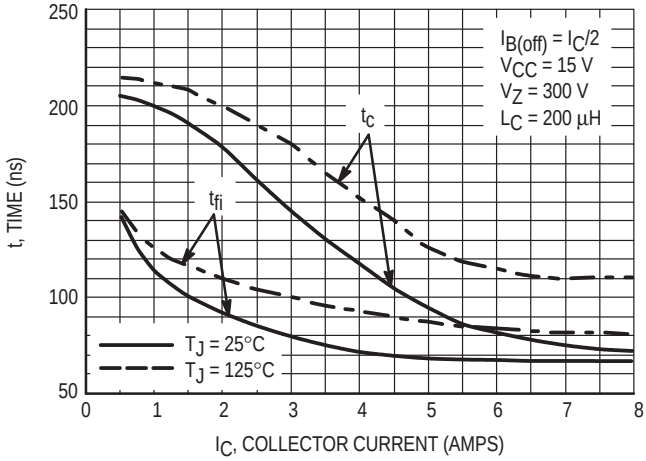


Figure 12. Inductive Switching, t_c and t_{fi}
$I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

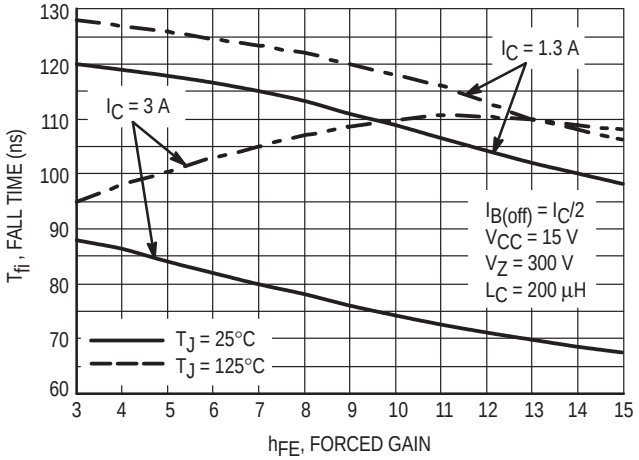


Figure 13. Inductive Fall Time

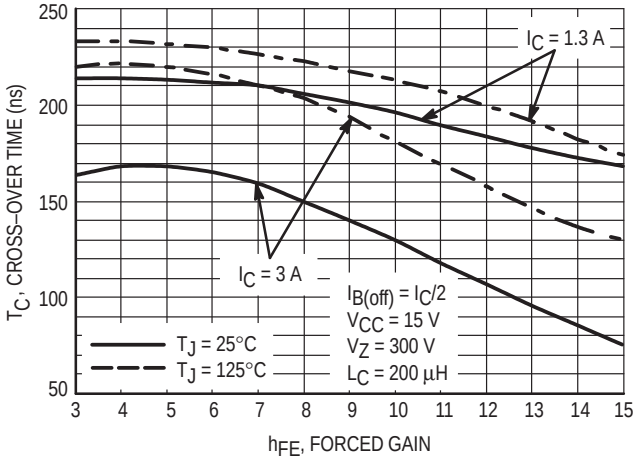


Figure 14. Inductive Cross–Over Time

GUARANTEED SAFE OPERATING AREA INFORMATION

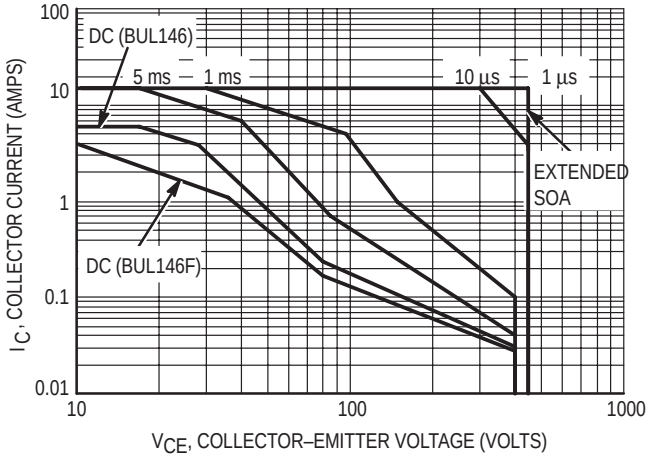


Figure 15. Forward Bias Safe Operating Area

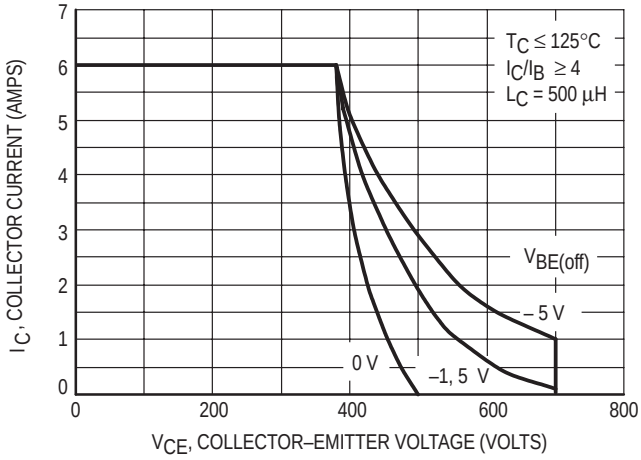


Figure 16. Reverse Bias Switching Safe Operating Area

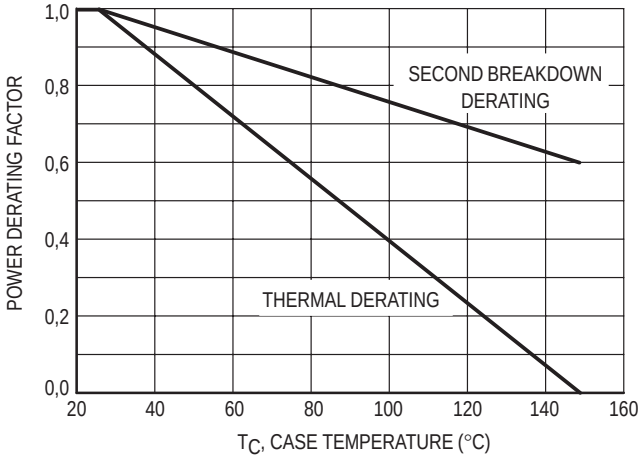


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figure 20 and 21. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse–biased. The safe level is specified as a reverse–biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

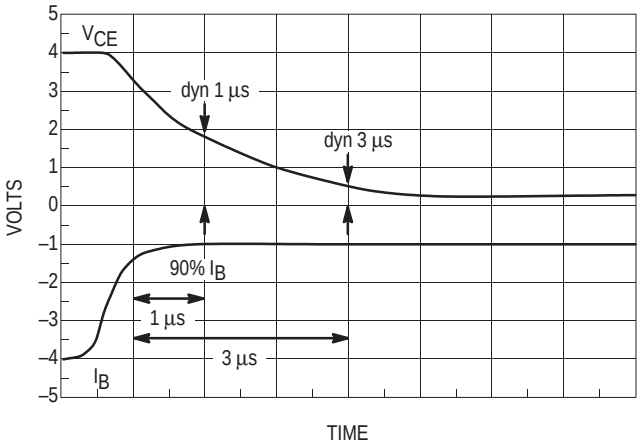


Figure 18. Dynamic Saturation Voltage Measurements

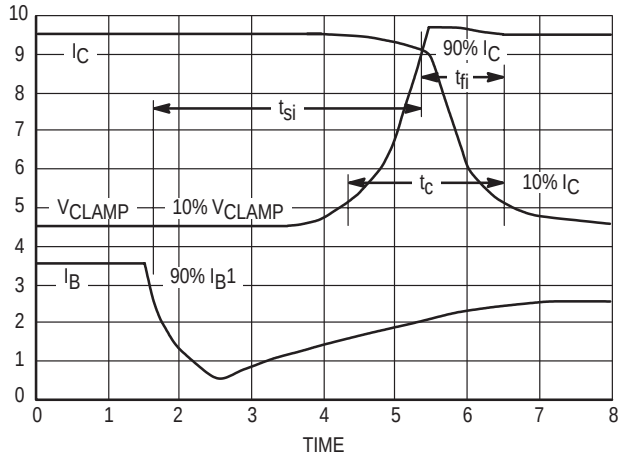
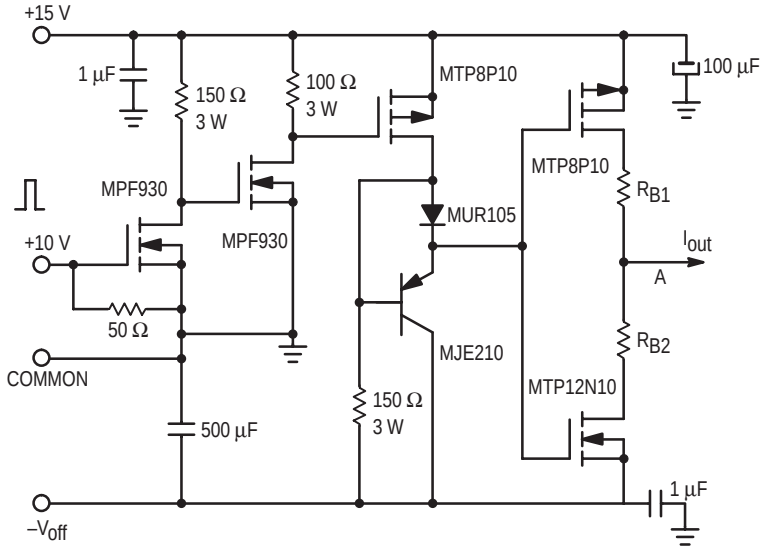
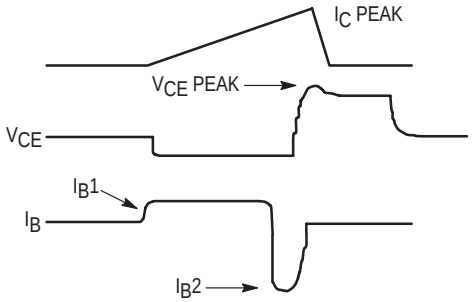


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 µH	L = 500 µH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_{B1}	RB1 SELECTED FOR DESIRED I_{B1}

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

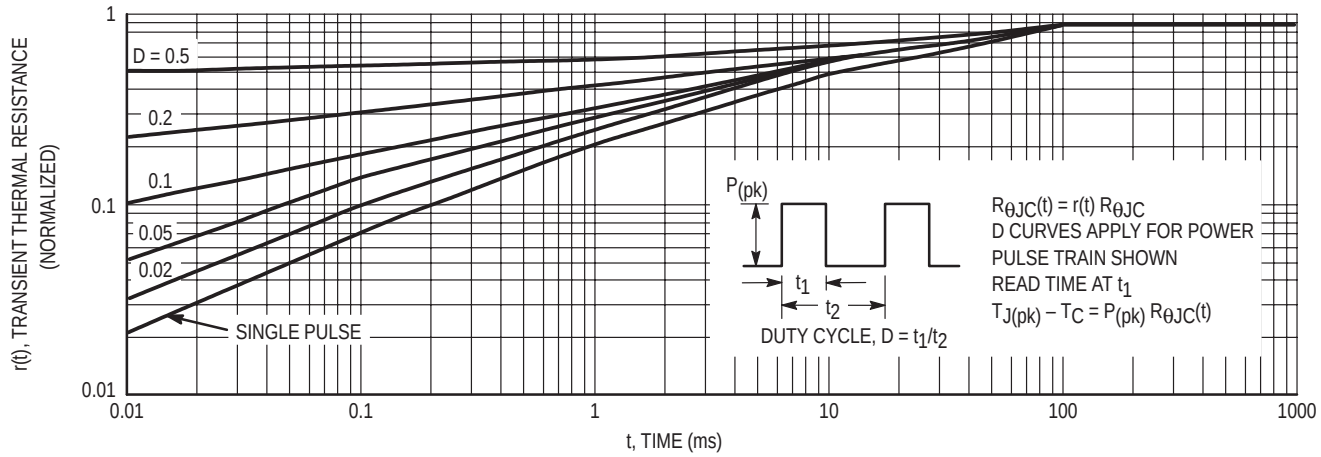


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL146

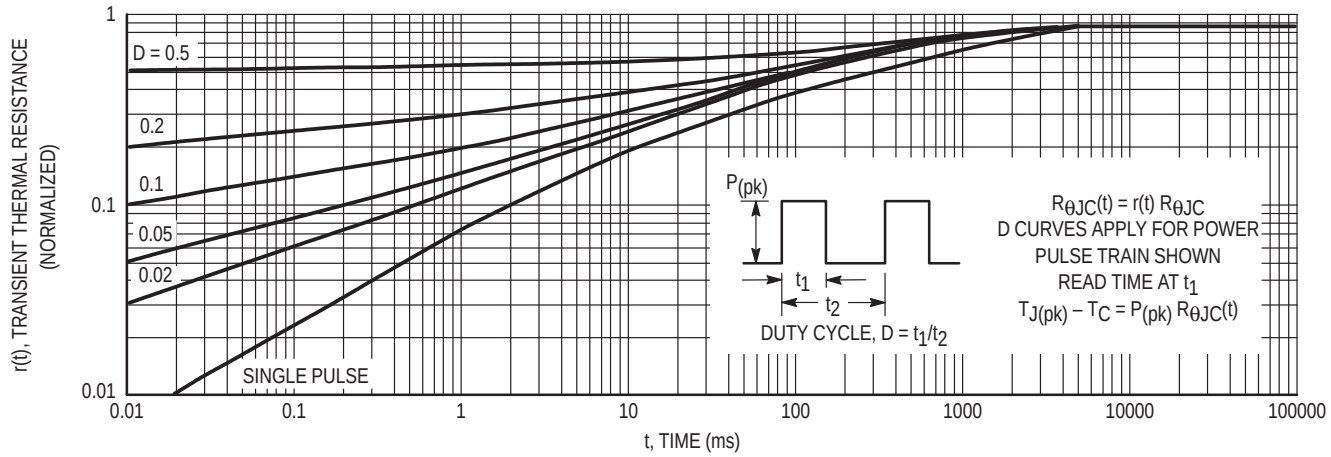


Figure 21. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL146F

TEST CONDITIONS FOR ISOLATION TESTS*

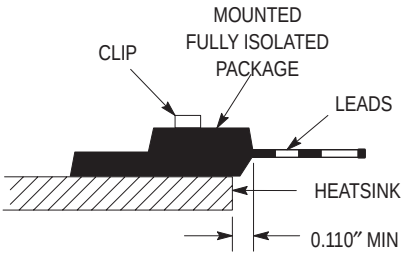


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

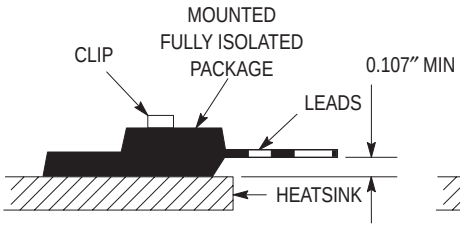


Figure 22b. Clip Mounting Position for Isolation Test Number 2

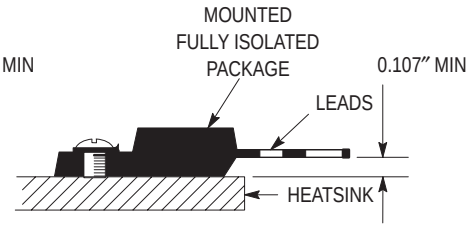


Figure 22c. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together.

MOUNTING INFORMATION**

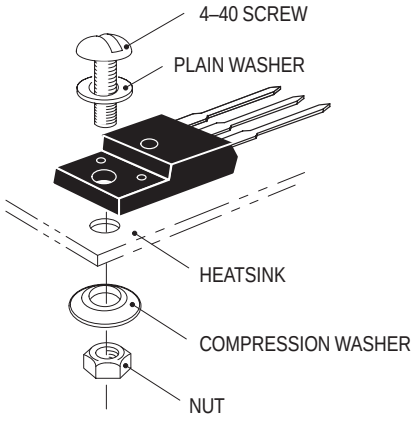


Figure 23a. Screw–Mounted

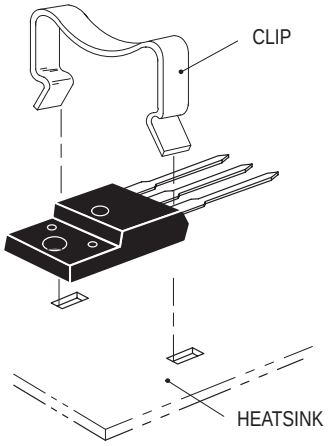


Figure 23b. Clip–Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

Designer's™ Data Sheet
SWITCHMODE™
NPN Bipolar Power Transistor
For Switching Power Supply Applications

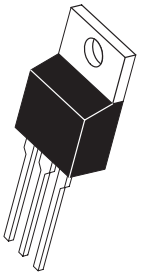
BUL147*
BUL147F*

*Motorola Preferred Device

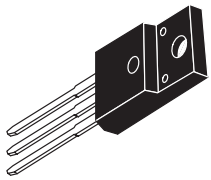
POWER TRANSISTOR
8.0 AMPERES
700 VOLTS
45 and 125 WATTS

The BUL147/BUL147F have an applications specific state–of–the–art die designed for use in electric fluorescent lamp ballasts to 180 Watts and in Switchmode Power supplies for all types of electronic equipment. These high–voltage/high–speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - — High and Flat DC Current Gain
  - — Fast Switching
  - — No Coil Required in Base Circuit for Turn–Off (No Current Tail)
- Parametric Distributions are Tight and Consistent Lot–to–Lot
- Two Package Choices: Standard TO–220 or Isolated TO–220
- BUL147F, Isolated Case 221D, is UL Recognized to 3500 V_{RMS}: File #E69369



BUL147
CASE 221A–06
TO–220AB



BUL147F
CASE 221D–02
ISOLATED TO–220 TYPE
UL RECOGNIZED

MAXIMUM RATINGS

Rating	Symbol	BUL147	BUL147F	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700		Vdc
Emitter–Base Voltage	V_{EBO}	9.0		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	8.0 16		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	4.0 8.0		Adc
RMS Isolated Voltage(2) Test No. 1 Per Fig. 22a (for 1 sec, R.H. < 30%, Test No. 2 Per Fig. 22b T_C = 25°C) Test No. 3 Per Fig. 22c	V_{ISOL}	— — —	4500 3500 1500	Volts
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	125 1.0	45 0.36	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	– 65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	BUL44	BUL44F	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	2.78 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	—	—	100	μAdc
(T_C = 125°C)		—	—	500	
(V_{CE} = 500 V, V_{EB} = 0) (T_C = 125°C)		—	—	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS								
Base–Emitter Saturation Voltage	(I_C = 2.0 Adc, I_B = 0.2 Adc)			$V_{BE(sat)}$	—	0.82	1.1	Vdc
	(I_C = 4.5 Adc, I_B = 0.9 Adc)				—	0.92	1.25	
Collector–Emitter Saturation Voltage				$V_{CE(sat)}$				Vdc
(I_C = 2.0 Adc, I_B = 0.2 Adc)					—	0.25	0.5	
	(T_C = 125°C)				—	0.3	0.5	
(I_C = 4.5 Adc, I_B = 0.9 Adc)					—	0.35	0.7	
	(T_C = 125°C)				—	0.35	0.8	
DC Current Gain	(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)			h_{FE}	14	—	34	—
	(T_C = 125°C)				—	30	—	
	(I_C = 4.5 Adc, V_{CE} = 1.0 Vdc)				8.0	12	—	
	(T_C = 125°C)				7.0	11	—	
	(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)	(T_C = 25°C to 125°C)			10	18	—	
	(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)				10	20	—	
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)				f_T	—	14	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)				C_{ob}	—	100	175	pF
Input Capacitance (V_{EB} = 8.0 V)				C_{ib}	—	1750	2500	pF
Dynamic Saturation Voltage: Determined 1.0 µs and 3.0 µs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18)	(I_C = 2.0 Adc I_{B1} = 200 mAdc V_{CC} = 300 V)	1.0 µs	(T_C = 125°C)	$V_{CE(dsat)}$	—	3.0	—	Volts
					—	5.5	—	
		3.0 µs	(T_C = 125°C)		—	0.8	—	
					—	1.4	—	
	(I_C = 5.0 Adc I_{B1} = 0.9 Adc V_{CC} = 300 V)	1.0 µs	(T_C = 125°C)		—	3.3	—	
					—	8.5	—	
		3.0 µs	(T_C = 125°C)		—	0.4	—	
					—	1.0	—	
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 µs)								
Turn–On Time	(I_C = 2.0 Adc, I_{B1} = 0.2 Adc I_{B2} = 1.0 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	—	200	350	ns
					—	190	—	
Turn–Off Time				t_{off}	—	1.0	2.5	µs
			(T_C = 125°C)		—	1.6	—	
Turn–On Time	(I_C = 4.5 Adc, I_{B1} = 0.9 Adc I_{B1} = 2.25 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	—	85	150	ns
					—	100	—	
Turn–Off Time				t_{off}	—	1.5	2.5	µs
			(T_C = 125°C)		—	2.0	—	
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 µH)								
Fall Time	(I_C = 2.0 Adc, I_{B1} = 0.2 Adc I_{B2} = 1.0 Adc)		(T_C = 125°C)	t_{fi}	—	100	180	ns
					—	120	—	
Storage Time				t_{si}	—	1.3	2.5	µs
			(T_C = 125°C)		—	1.9	—	
Crossover Time				t_c	—	210	350	ns
			(T_C = 125°C)		—	230	—	
Fall Time	(I_C = 4.5 Adc, I_{B1} = 0.9 Adc I_{B2} = 2.25 Adc)		(T_C = 125°C)	t_{fi}	—	80	150	ns
					—	100	—	
Storage Time				t_{si}	—	1.6	3.2	µs
			(T_C = 125°C)		—	2.1	—	
Crossover Time				t_c	—	170	300	ns
			(T_C = 125°C)		—	200	—	
Fall Time	(I_C = 4.5 Adc, I_{B1} = 0.9 Adc I_{B2} = 0.9 Adc)		(T_C = 125°C)	t_{fi}	60	—	180	ns
					—	150	—	
Storage Time				t_{si}	2.6	—	3.8	µs
			(T_C = 125°C)		—	4.3	—	
Crossover Time				t_c	—	200	350	ns
			(T_C = 125°C)		—	330	—	

TYPICAL STATIC CHARACTERISTICS

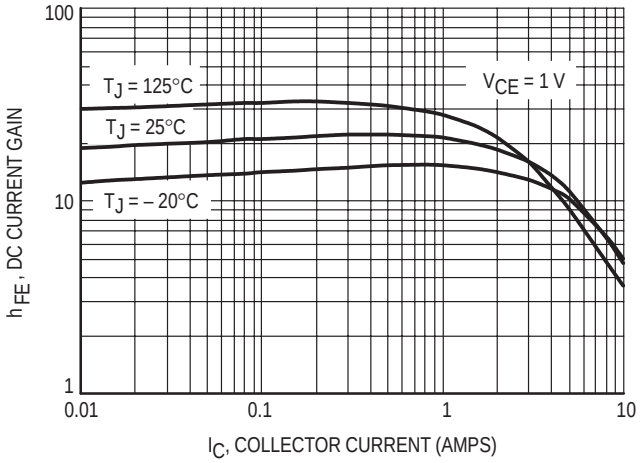


Figure 1. DC Current Gain @ 1 Volt

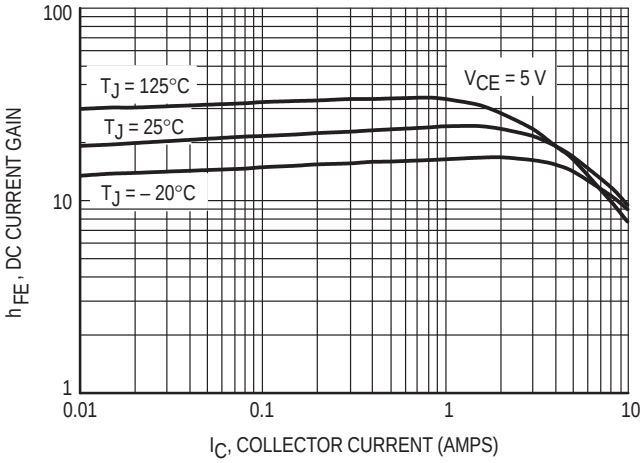


Figure 2. DC Current Gain @ 5 Volts

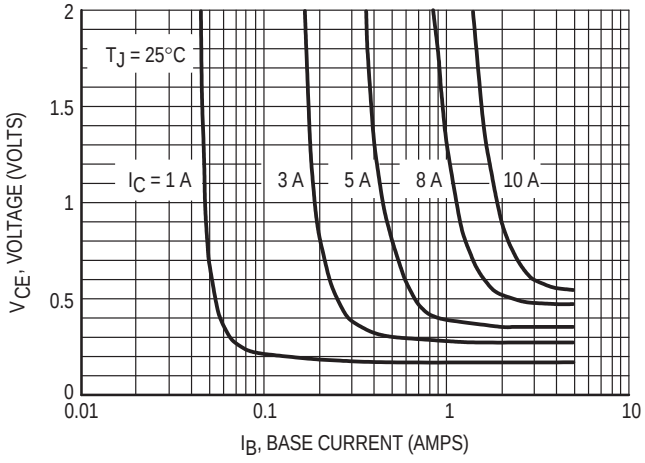


Figure 3. Collector Saturation Region

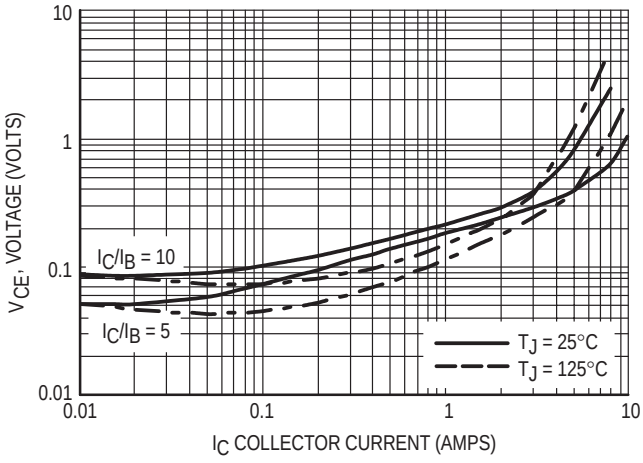


Figure 4. Collector–Emitter Saturation Voltage

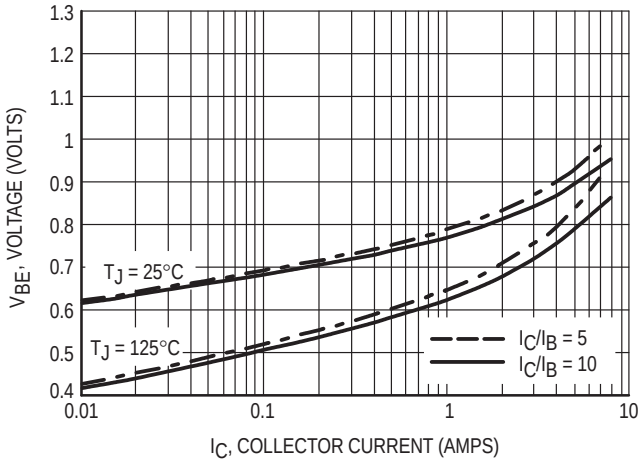


Figure 5. Base–Emitter Saturation Region

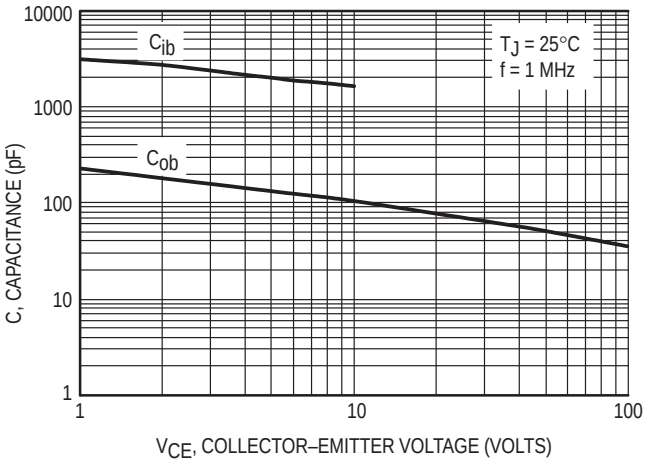


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

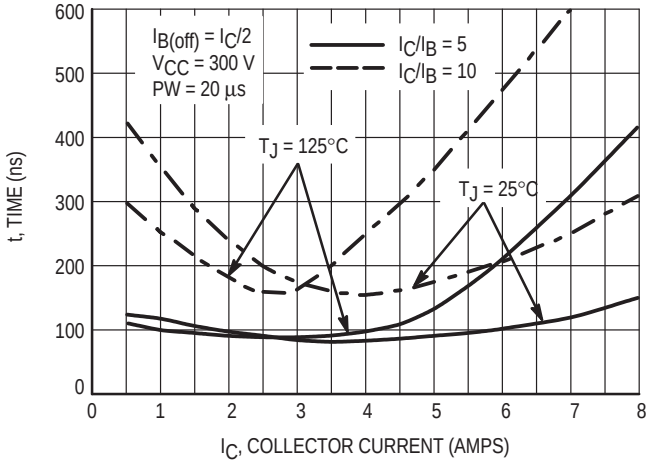


Figure 7. Resistive Switching, t_{on}

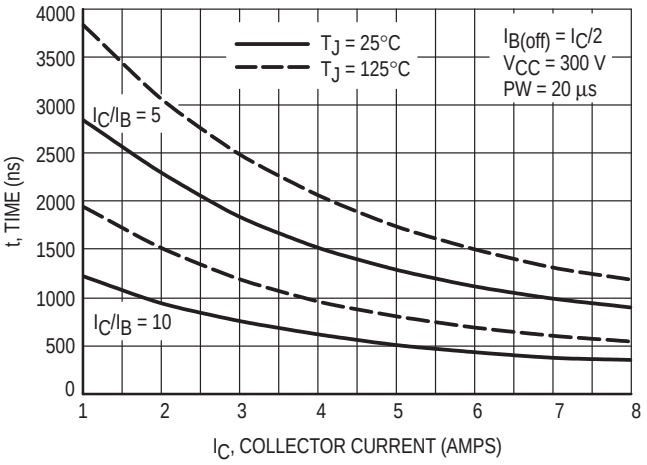


Figure 8. Resistive Switching, t_{off}

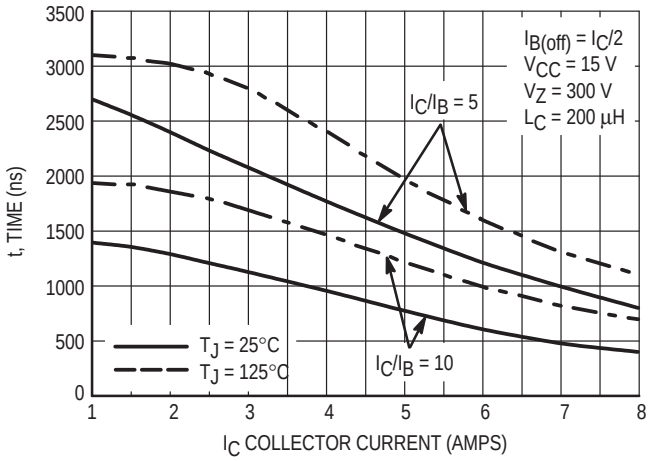


Figure 9. Inductive Storage Time, t_{si}

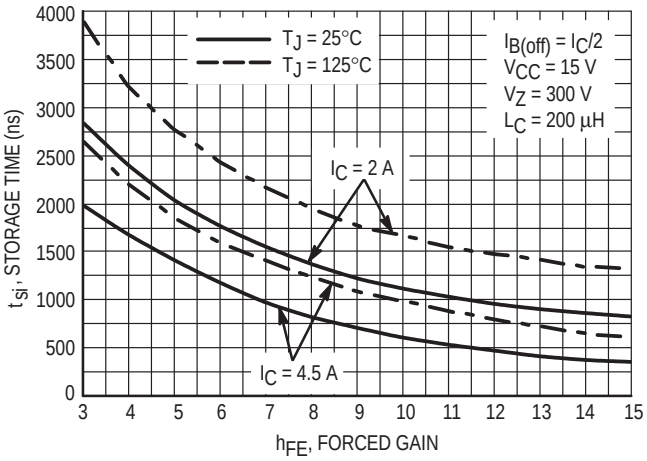


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

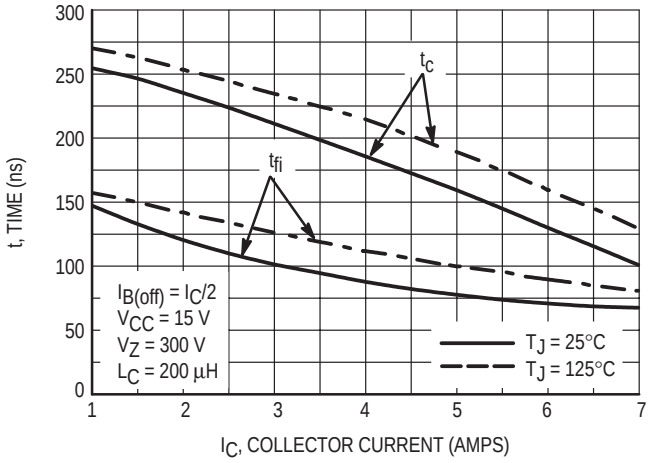


Figure 11. Inductive Switching, t_c and t_{fi}
$I_C/I_B = 5$

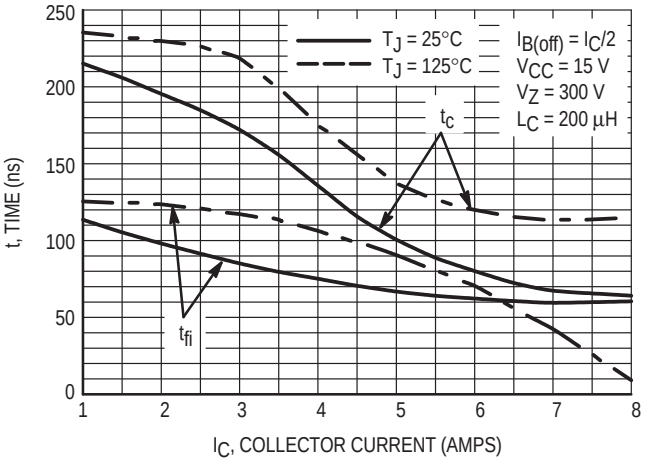


Figure 12. Inductive Switching, t_c and t_{fi}
$I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

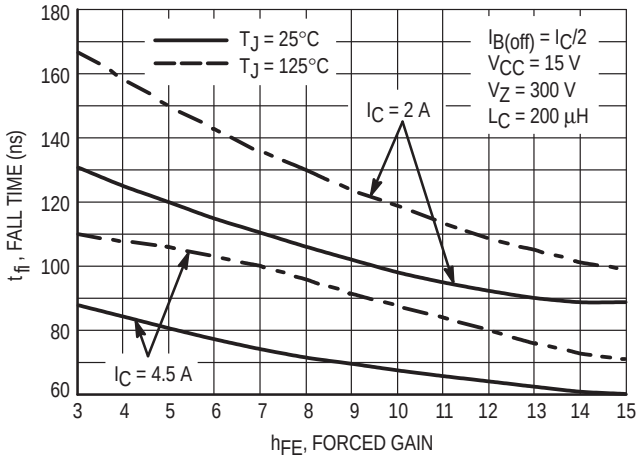


Figure 13. Inductive Fall Time

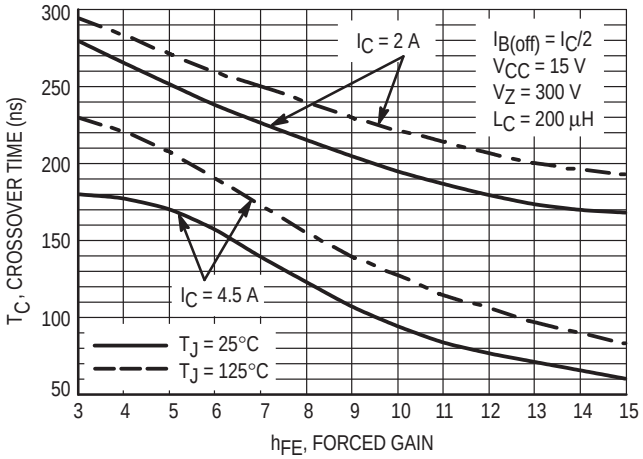


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

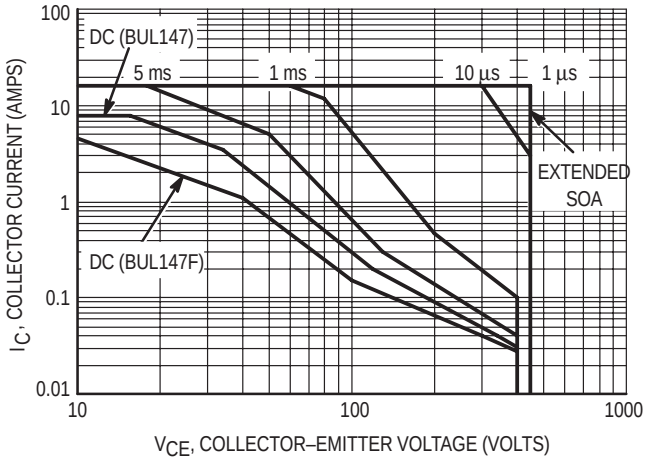


Figure 15. Forward Bias Safe Operating Area

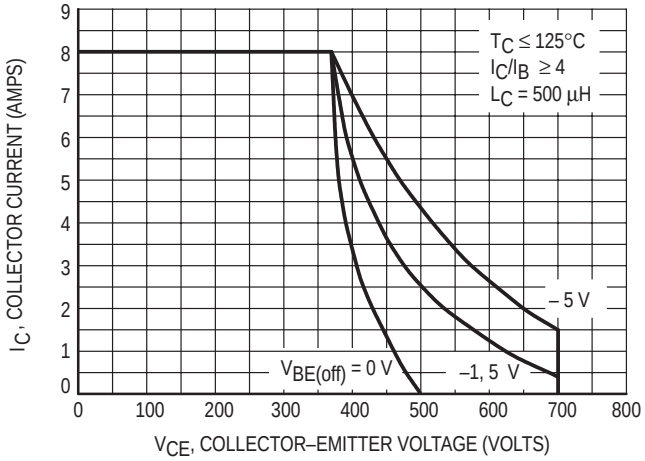


Figure 16. Reverse Bias Switching Safe Operating Area

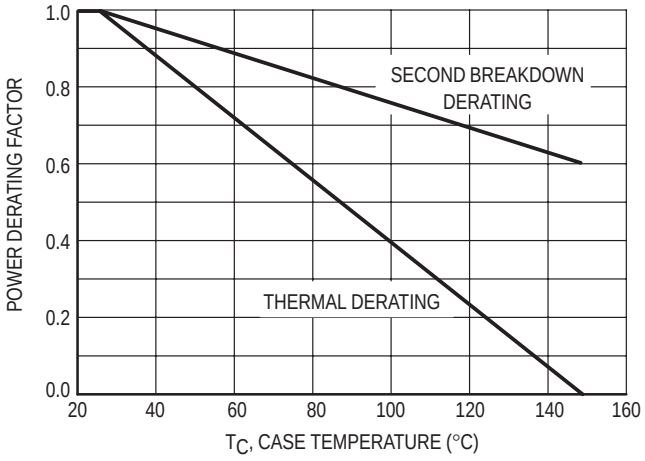


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figure 20 and 21. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse–biased. The safe level is specified as a reverse–biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

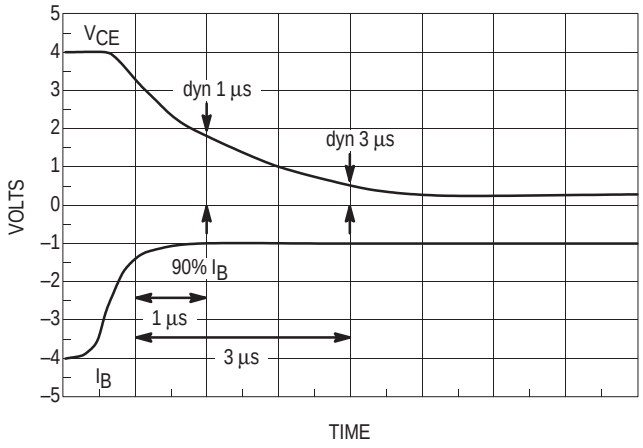


Figure 18. Dynamic Saturation Voltage Measurements

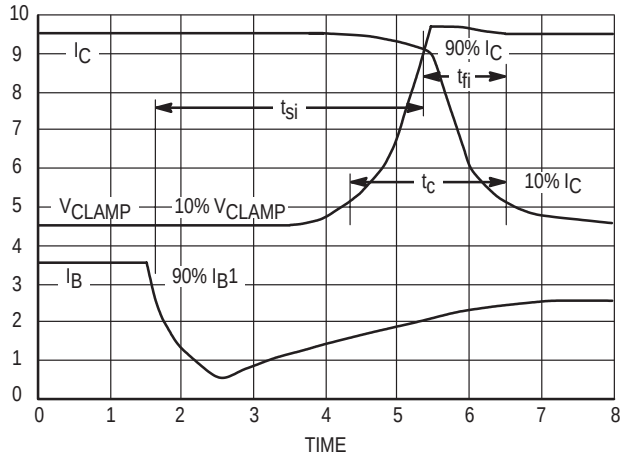
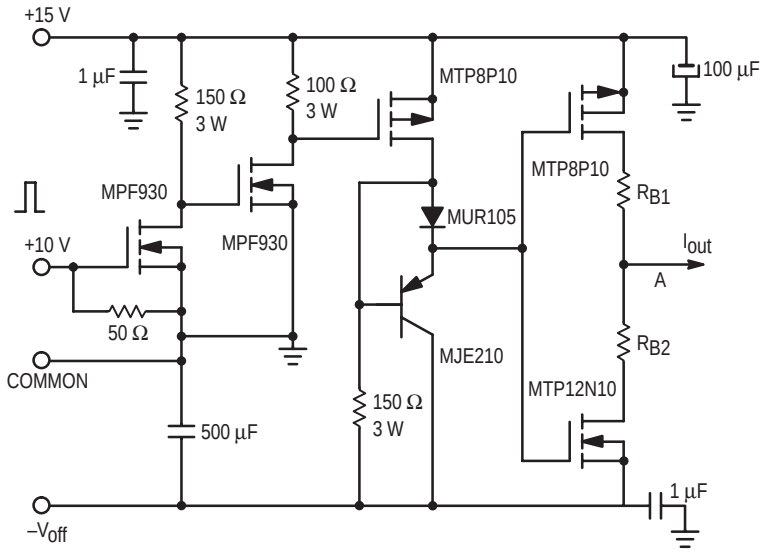
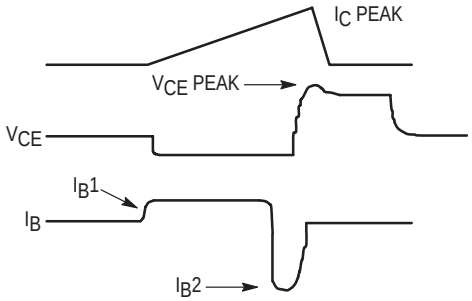


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 µH	L = 500 µH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_B1	RB1 SELECTED FOR DESIRED I_B1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

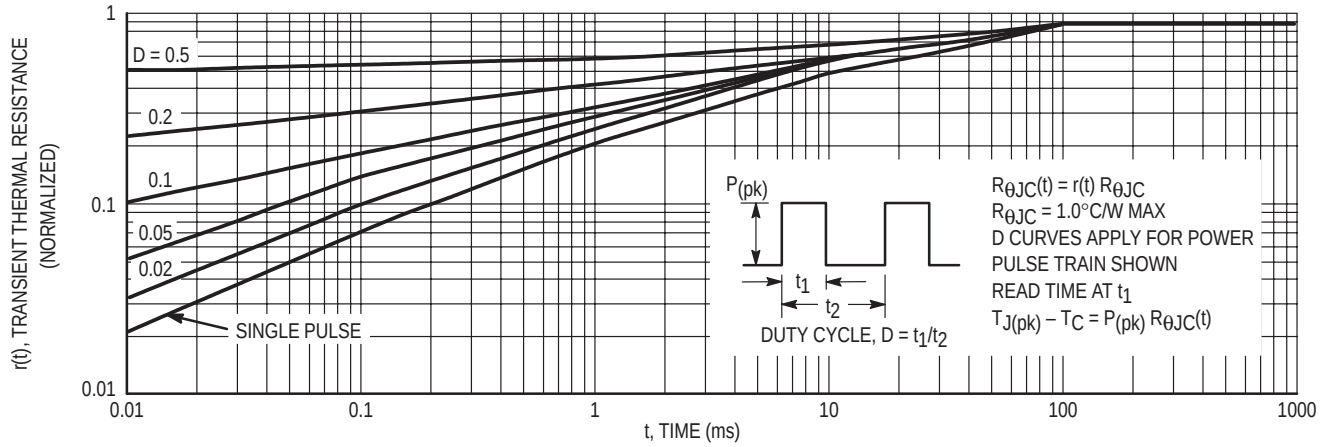


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL147

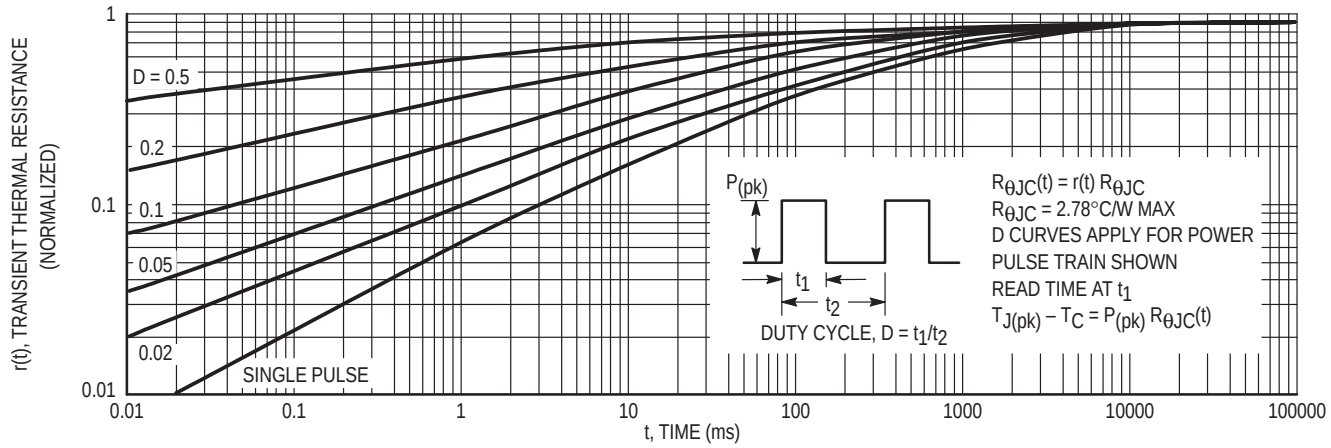


Figure 21. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL147F

TEST CONDITIONS FOR ISOLATION TESTS*

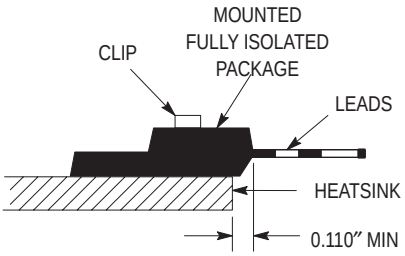


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

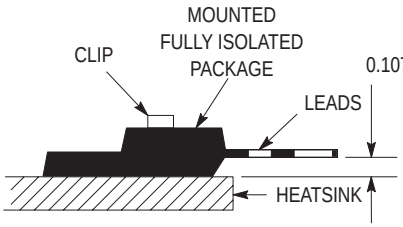


Figure 22b. Clip Mounting Position for Isolation Test Number 2

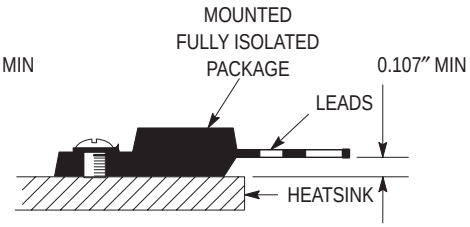


Figure 22c. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together.

MOUNTING INFORMATION**

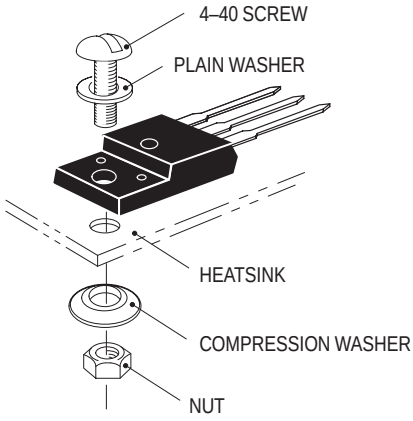


Figure 23a. Screw–Mounted

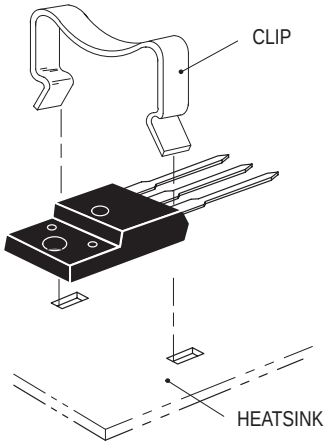


Figure 23b. Clip–Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

BUS50

SWITCHMODE Series NPN Silicon Power Transistors

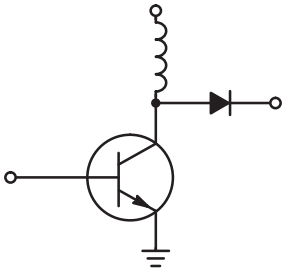
70 AMPERES
NPN SILICON
POWER TRANSISTOR
125 VOLTS (BVCEO)
350 WATTS
200 V (BVCES)

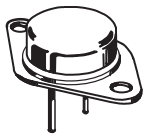
The BUS50 transistor is designed for low voltage, high–speed, power switching in inductive circuits where fall time is critical. It is particularly suited for battery switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls

Fast Turn–Off Times
300 ns Inductive Fall Time – 25°C (Typ)

Operating Temperature Range – 65 to + 200°C





CASE 197A–05
TO–204AE

MAXIMUM RATINGS

Rating	Symbol	BUS50	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	125	Vdc
Collector–Emitter Voltage	V_{CEV}	200	Vdc
Emitter Base Voltage	V_{EB}	7	Vdc
Collector Current — Continuous — Peak (1) — Overload	I_C I_{CM} I_{OI}	70 140	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	20	Adc
Total Power Dissipation — T_C = 25°C — T_C = 100°C Derate above 25°C	P_D	350 200 2	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	– 65 to + 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≦10%.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS[1]				
Collector–Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	125		Vdc
Collector Cutoff Current at Reverse Bias (V_{CE} = 200 V, V_{BE} = –1.5 V) (V_{CE} = 200 V, V_{BE} = –1.5 V, T_C = 125°C)	I_{CEX}		0.2 2	mAdc
Collector–Emitter Cutoff Current (V_{CE} = 125 V)	I_{CEO}		1	mAdc
Emitter Cutoff Current (V_{EB} = 7 V)	I_{EBO}		0.2	mAdc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 5 A, V_{CE} = 4 V) (I_C = 50 A, V_{CE} = 4 V)	h_{FE}	20 15		
Collector–Emitter Saturation Voltage (I_C = 35 A, I_B = 2 A) (I_C = 70 A, I_B = 7 A)	$V_{CE(sat)}$		1 1.2	Vdc
Base–Emitter Saturation Voltage (I_C = 35 A, I_B = 2 A) (I_C = 70 A, I_B = 7 A)	$V_{BE(sat)}$		1.8 2	Vdc

SWITCHING CHARACTERISTICS (Resistive Load) t_{on} and (Inductive Load) t_{sv}, t_{fi}

Turn–On Time	I_C = 70 A, I_{B1} = 7 A $V_{BE(off)}$ = −5 V (V_{CC} = 125 V)	t_{on}		1.2	μs
Storage Time		t_{sv}		1.5	
Fall Time		t_{fi}		0.3	

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

BUS98
BUS98A

Designer's™ Data Sheet

SWITCHMODE Series
NPN Silicon Power Transistors

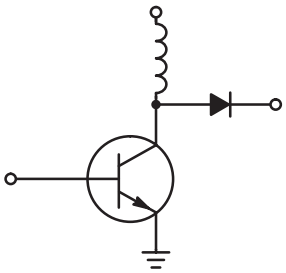
30 AMPERES
NPN SILICON
POWER TRANSISTORS
400 AND 450 VOLTS
(BVCEO)
250 WATTS
850 – 1000 V (BVCES)

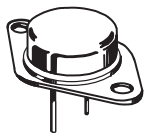
The BUS98 and BUS98A transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn–Off Times
60 ns Inductive Fall Time – 25°C (Typ)
120 ns Inductive Crossover Time – 25°C (Typ)
Operating Temperature Range – 65 to + 200°C

100°C Performance Specified for:
Reverse–Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents (125°C)





CASE 1–07
TO–204AA

MAXIMUM RATINGS

Rating	Symbol	BUS98	BUS98A	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector–Emitter Voltage	V_{CEV}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current — Continuous — Peak (1) — Overload	I_C I_{CM} I_{OI}	30 60 120		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 30		Adc
Total Power Dissipation — T_C = 25°C — T_C = 100°C Derate above 25°C	P_D	250 142 1.42		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	– 65 to + 200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≦10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector–Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$				Vdc
(I_C = 200 mA, I_B = 0) L = 25 mH	BUS98		400	—	—	
	BUS98A		450	—	—	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			—	—	0.4	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)			—	—	4.0	
Collector Cutoff Current		I_{CER}				mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 10 Ω)	T_C = 25 °C		—	—	1.0	
	T_C = 125 °C		—	—	6.0	
Emitter Cutoff Current		I_{EBO}	—	—	0.2	mAdc
(V_{EB} = 7 Vdc, I_C = 0)						
Emitter–Base Breakdown Voltage		V_{EBO}	7.0	—	—	Vdc
(I_E = 100 mA – I_C = 0)						
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$		See Figure 12		
Clamped Inductive SOA with Base Reverse Biased		RBSOA		See Figure 13		
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}	8	—	—	—
(I_C = 20 Adc, V_{CE} = 5 Vdc)	BUS98					
(I_C = 16 Adc, V_{CE} = 5 V)	BUS98A					
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 20 Adc, I_B = 4 Adc)	BUS98		—	—	1.5	
(I_C = 30 Adc, I_B = 8 Adc)			—	—	3.5	
(I_C = 20 Adc, I_B = 4 Adc, T_C = 100°C)			—	—	2.0	
(I_C = 16 Adc, I_B = 3.2 Adc)	BUS98A		—	—	1.5	
(I_C = 24 Adc, I_B = 5 Adc)			—	—	5.0	
(I_C = 16 Adc, I_B = 3.2 Adc, T_C = 100°C)			—	—	2.0	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 20 Adc, I_B = 4 Adc)	BUS98		—	—	1.6	
(I_C = 20 Adc, I_B = 4 Adc, T_C = 100°C)			—	—	1.6	
(I_C = 16 Adc, I_B = 3.2 Adc)	BUS98A		—	—	1.6	
(I_C = 16 Adc, I_B = 3.2 Adc, T_C = 100°C)			—	—	1.6	
DYNAMIC CHARACTERISTICS						
Output Capacitance		C_{ob}	—	—	700	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)						

SWITCHING CHARACTERISTICS

Restive Load (Table 1)

Delay Time	(V_{CC} = 250 Vdc, I_C = 20 A, I_{B1} = 4.0 A, t_p = 30 μs, Duty Cycle ≤ 2%, $V_{BE(off)}$ = 5 V) (for BUS98A: I_C = 16 A, Ib_1 = 3.2 A)	t_d	—	0.1	0.2	μs
Rise Time		t_r	—	0.4	0.7	
Storage Time		t_s	—	1.55	2.3	
Fall Time		t_f	—	0.2	0.4	

Inductive Load, Clamped (Table 1)

Storage Time	$I_{C(pk)}$ = 20 A, I_{b1} = 4 A, $V_{BE(off)}$ = 5 V, $V_{CE(c1)}$ = 250 V, $I_{C(pk)}$ = 16 A, IB_1 = 3.2 A) (BUS98)	(T_C = 25°C)	t_{sv}	—	1.55	—	μs
Fall Time			t_{fi}	—	0.06	—	
Storage Time		(T_C = 100°C)	t_{sv}	—	1.8	2.8	
Crossover Time	(BUS98A)		t_c	—	0.3	0.6	
Fall Time			t_{fi}	—	0.17	0.35	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

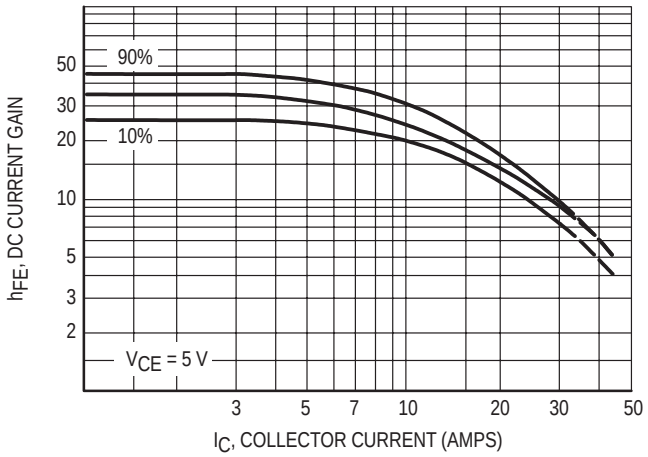


Figure 1. DC Current Gain

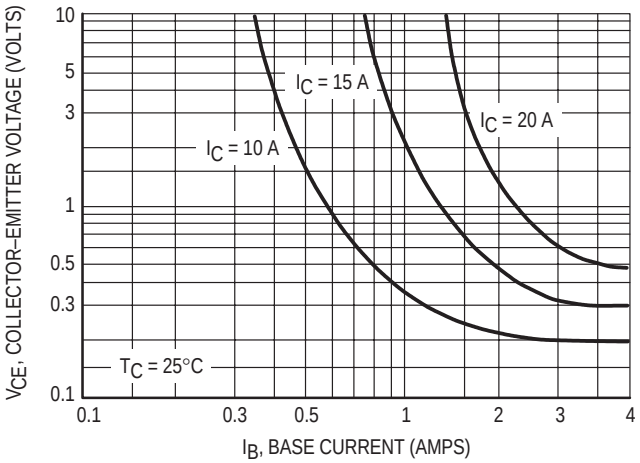


Figure 2. Collector Saturation Region

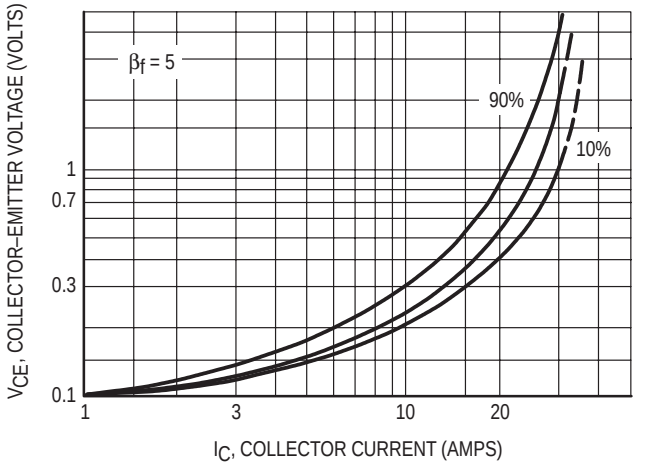


Figure 3. Collector–Emitter Saturation Voltage

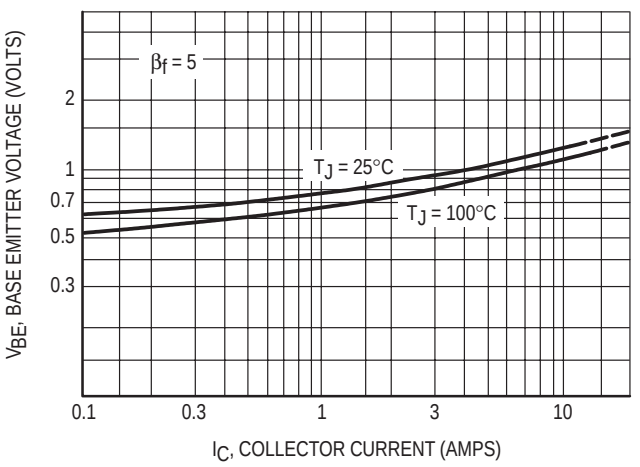


Figure 4. Base–Emitter Voltage

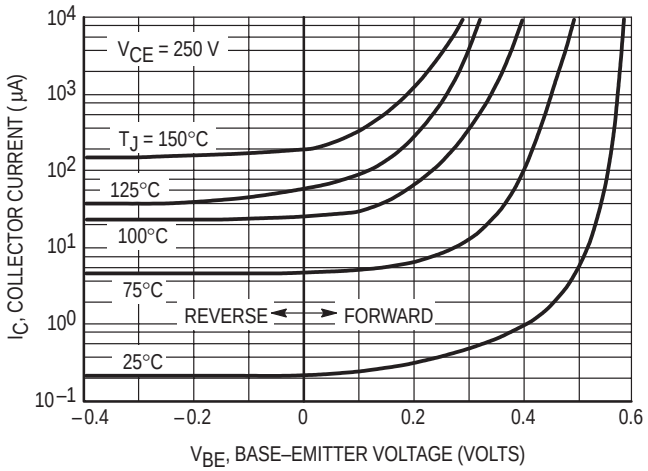


Figure 5. Collector Cutoff Region

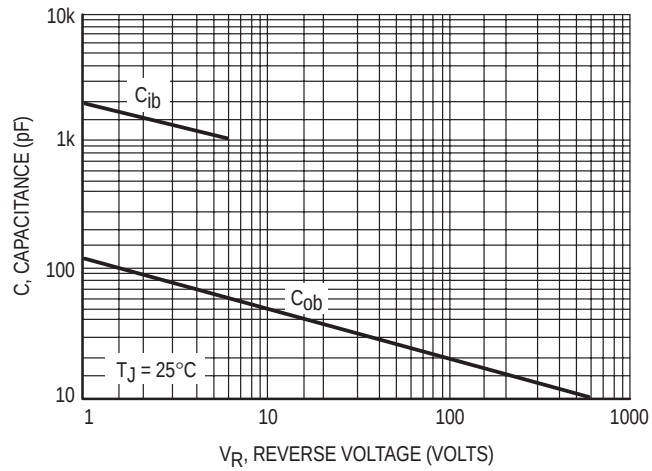


Figure 6. Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20, 1, 0, 2 PW Varied to Attain I_C = 100 mA	+10 V, –10 V, MJE200, BUV20, MJE210, BUV20, 0.1 µF, 50 µF, 1 µF, 50 µF, $-V_{C1}$ ADJUST V_{C1} TO OBTAIN DESIRED I_{B1}, ADJUST V_{C2} TO OBTAIN DESIRED I_{B2}	**TURN–ON TIME** I_{B1} adjusted to obtain the forced h_{FE} desired **TURN–OFF TIME** Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 25 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V	V_{CC} = 250 V Pulse Width = 10 µs
TEST CIRCUITS	**INDUCTIVE TEST CIRCUIT** TUT, 1, INPUT, SEE ABOVE FOR DETAILED CONDITIONS, 2, 1N4937 OR EQUIVALENT, R_{coil}, L_{coil}, V_{clamp}, V_{CC} **OUTPUT WAVEFORMS** I_C, $I_{C(pk)}$, t_f Clamped, t_1, t_f, t, V_{CE}, V_{CE} or V_{clamp}, TIME, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}\ (I_{C(pk)})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}\ (I_{C(pk)})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	**RESISTIVE TEST CIRCUIT** TUT, 1, 2, R_L, V_{CC}

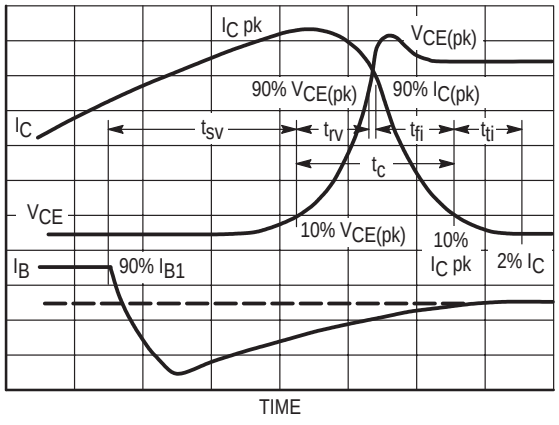


Figure 7. Inductive Switching Measurements

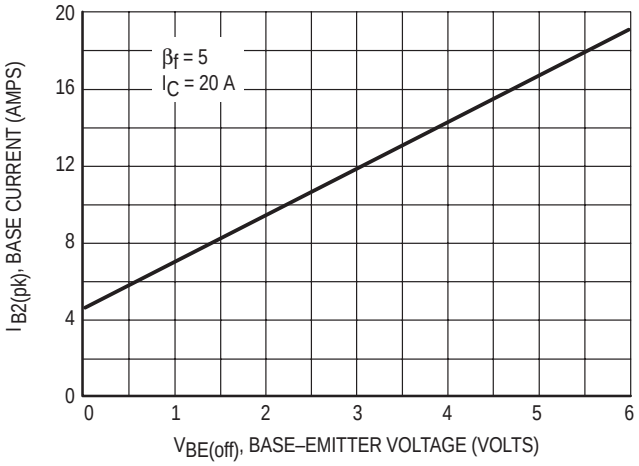


Figure 8. Peak–Reverse Current

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

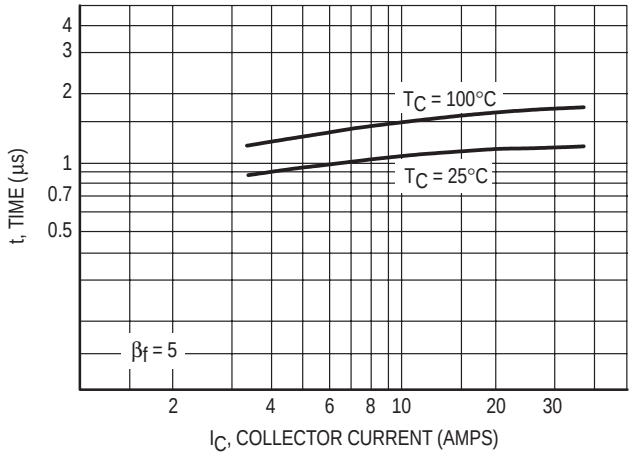


Figure 9. Storage Time, t_{sv}

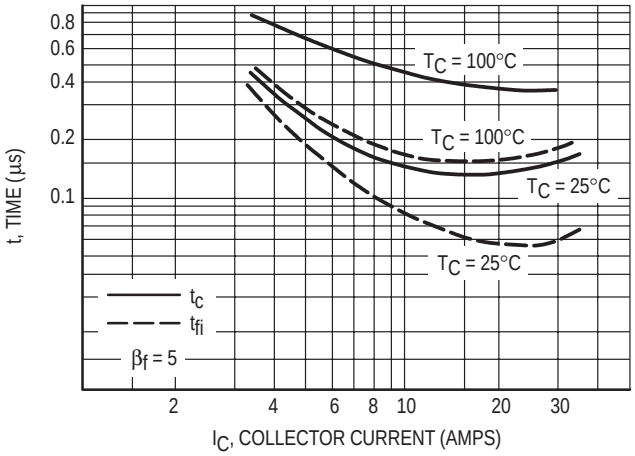


Figure 10. Crossover and Fall Times

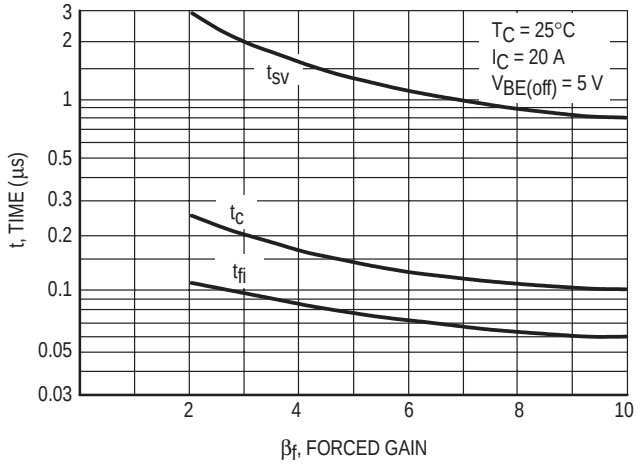


Figure 11a. Turn–Off Times versus Forced Gain

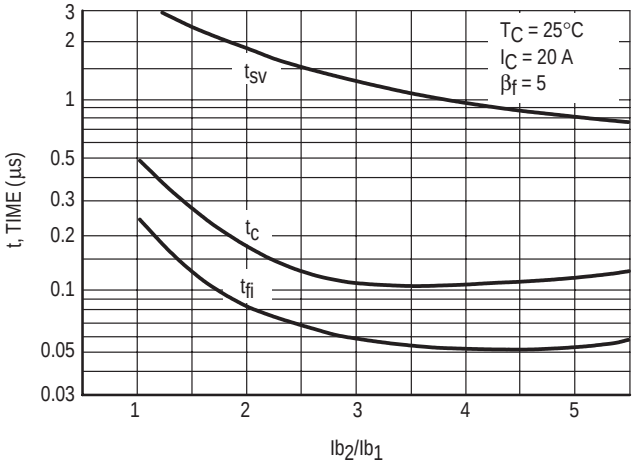


Figure 11b. Turn–Off TM Times versus Ib_2/Ib_1

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

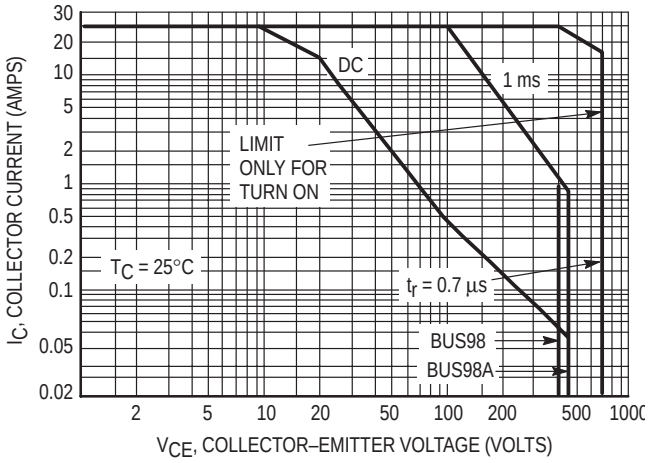


Figure 12. Forward Bias Safe Operating Area

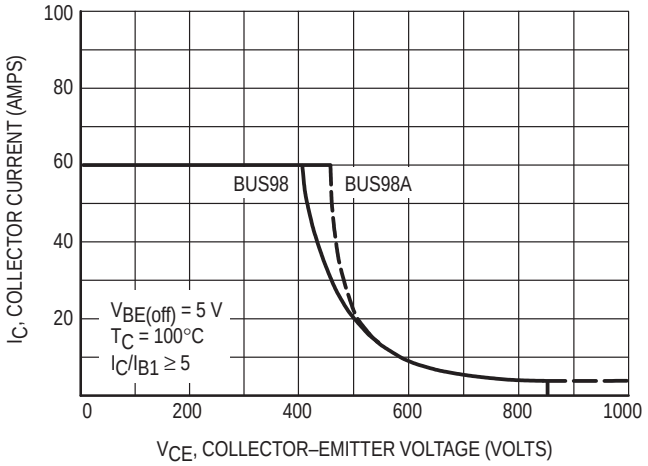


Figure 13. Reverse Bias Safe Operating Area

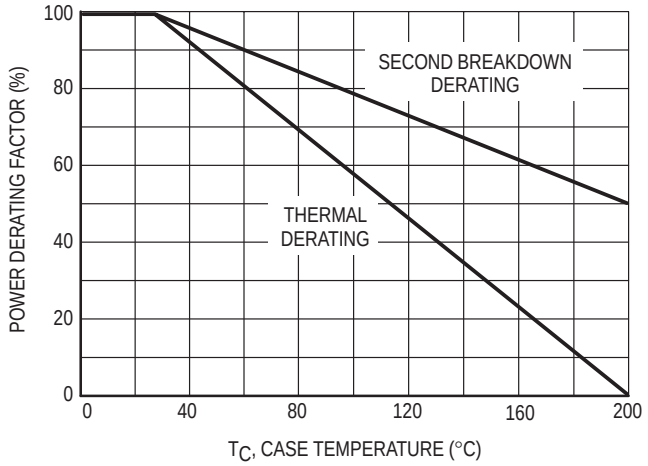


Figure 14. Power Derating

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

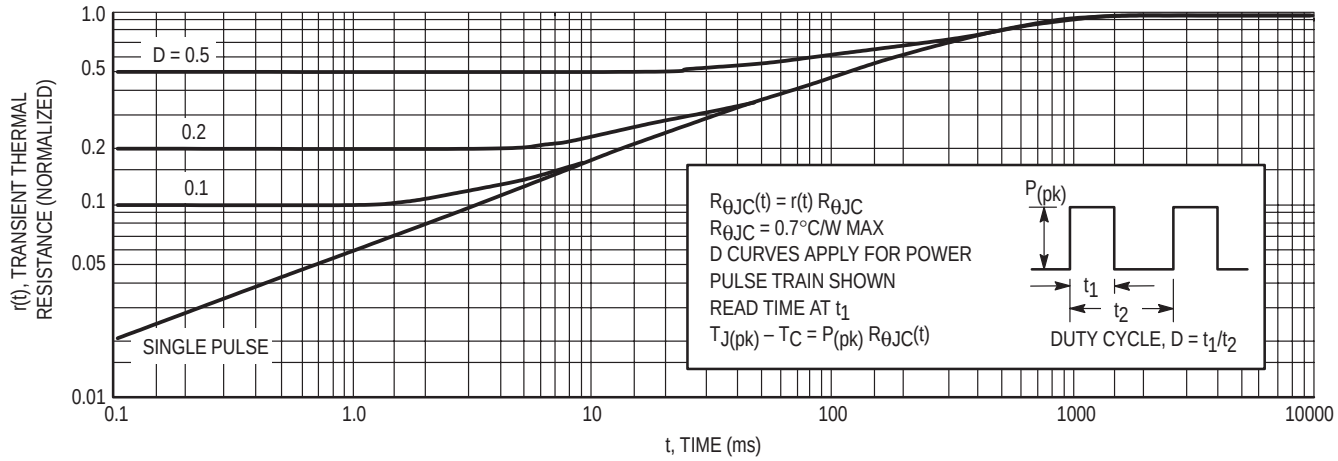


Figure 15. Thermal Response

OVERLOAD CHARACTERISTICS

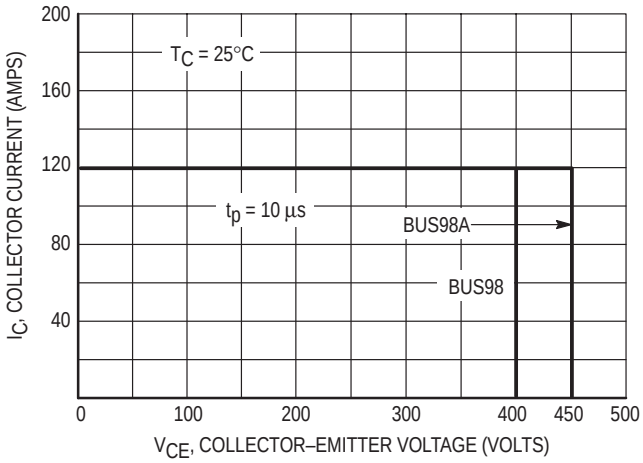


Figure 16. Rated Overload Safe Operating Area (OLSOA)

OLSOA

OLSOA applies when maximum collector current is limited and known. A good example Is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

Maximum allowable collector–emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common–base circuit (Figure 18) which allows precise definition of collector–emitter voltage and collector current. This is the same circuit that is used to measure forward–bias safe operating area.

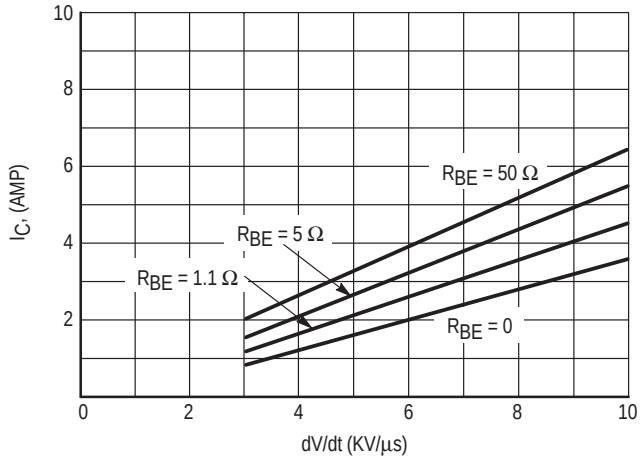
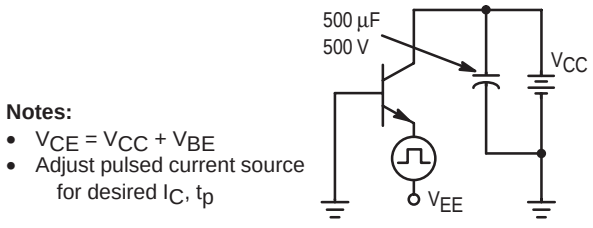


Figure 17. I_C = f (dV/dt)



Notes:
- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

Figure 18. Overload SOA Test Circuit

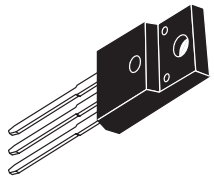
BUT11AF

Full Pak
High Voltage NPN Power Transistor
For Isolated Package Applications

POWER TRANSISTOR
5.0 AMPERES
450 VOLTS
40 WATTS

The BUT11AF was designed for use in line operated switching power supplies in a wide range of end use applications. This device combines the latest state of the art bipolar fabrication techniques to provide excellent switching, high voltage capability and low saturation voltage.

- 1000 Volt V_{CES} Rating
- Low Base Drive Requirements
- Isolated Overmold Package
- Improved System Efficiency
- No Isolating Washers Required
- Reduced System Cost
- High Isolation Voltage Capability (4500 V_{RMS})



CASE 221D–02
TO–220 TYPE

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector–Emitter Sustaining Voltage		$V_{CEO(sus)}$	450	Vdc
Collector–Emitter Breakdown Voltage		V_{CES}	1000	Vdc
Emitter–Base Voltage		V_{EBO}	9.0	Vdc
RMS Isolation Voltage (For 1 sec,	Per Figure 7	V_{ISOL1}	4500	V
T_A = 25°C, Rel. Humidity < 30%)	Per Figure 8	V_{ISOL2}	3500	
	Per Figure 9	V_{ISOL3}	2500	
Collector Current — Continuous — Pulsed (1)		I_C I_{CM}	5.0 10	Adc
Base Current — Continuous — Pulsed (1)		I_B I_{BM}	2.0 4.0	Adc
Total Power Dissipation @ T_C = 25°C* Derated above 25°C		P_D	40 0.32	Watts W/°C
Operating and Storage Temperature Range		T_J, T_{stg}	– 65 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case*	$R_{\theta JC}$	3.125	°C/W
Maximum Lead Temperature for soldering purposes 1/8″ from case for 5 sec.	T_L	260	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

* Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink, thermal grease applied, and a mounting torque of 6 to 8 in · lbs.

Full Pak is a registered trademark of Motorola Inc.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)							
Collector-Emitter Sustaining Voltage (Figures 1 & 2) (I_C = 100 mAdc, I_B = 0, L = 25 μH)			$V_{CEO(sus)}$	450	–	–	Vdc
Collector Cutoff Current (V_{CE} = 1000 Vdc, V_{BE} = 0) (V_{CE} = 1000 Vdc, V_{BE} = 0, T_J = 125°C)			I_{CES}	 – –	 – –	 1.0 2.0	mAdc
Emitter-Base Leakage (V_{EB} = 9.0 Vdc, I_C = 0)			I_{EBO}	–	–	10	mAdc
ON CHARACTERISTICS (1)							
Collector-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 0.5 Adc)			$V_{CE(sat)}$	–	–	1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 0.5 Adc)			$V_{BE(sat)}$	–	–	1.5	Vdc
DC Current Gain (I_C = 5.0 mAdc, V_{CE} = 5.0 Vdc)			h_{FE}	10	– –	– –	–
DYNAMIC CHARACTERISTICS							
Insulation Capacitance (Collector to External Heatsink)			Cc-hs	–	15	–	pF
SWITCHING CHARACTERISTICS							
Inductive Load (Figures 3 & 4)							
Storage	I_C = 2.5 Adc, I_{B1} = 0.5 Adc	T_J = 25°C	t_s	–	1100	1400	ns
Fall Time			t_{fi}	–	80	150	
Storage		T_J = 100°C	t_s	–	1200	1500	
Fall Time			t_{fi}	–	140	300	
Resistive Load (Figures 5 & 6)							
Turn-On Time	I_C = 2.5 Adc, I_{B1} = I_{B2} = 0.5 Adc		t_{on}	–	–	1000	ns
Storage Time			t_s	–	–	4000	
Fall Time			t_f	–	–	800	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

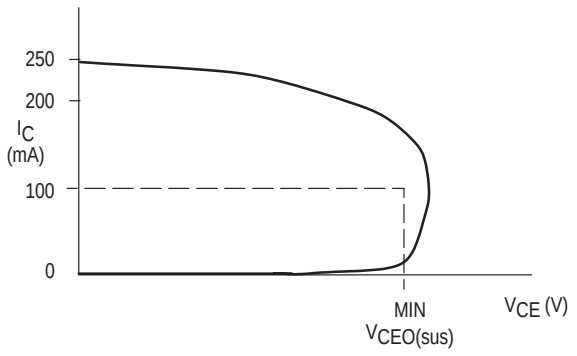


Figure 1. Oscilloscope Display for Sustaining Voltage

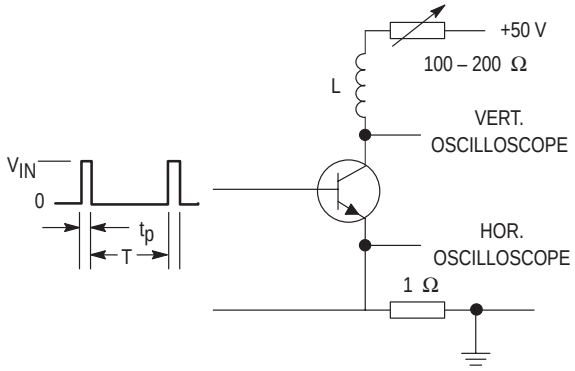
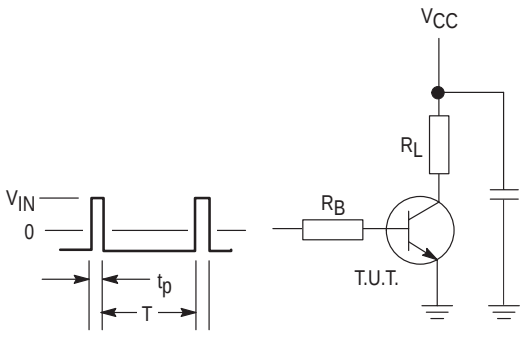


Figure 2. Test Circuit for $V_{CEO(sus)}$



V_{CC} = 250 V
V_{IN} = –6 to +8 V
t_p = 20 µs
$\frac{t_p}{T}$ = 0.01

Figure 3. Test Circuit Resistive Load

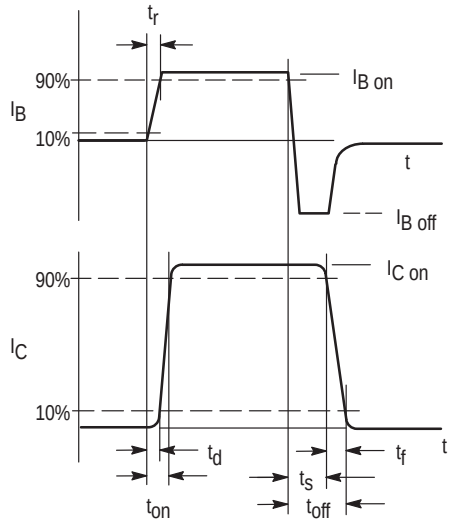
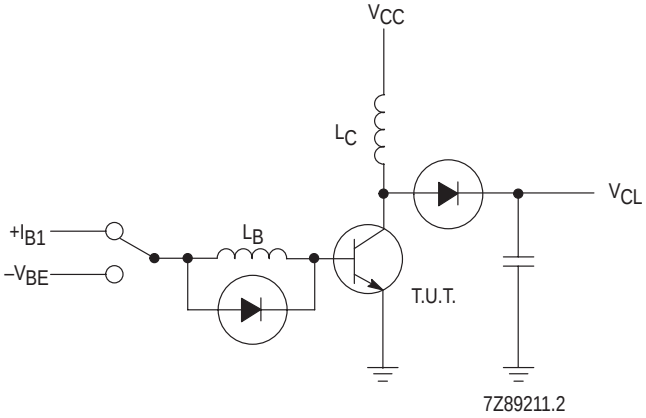


Figure 4. Switching Times Waveforms with Resistive Load



V_{CL} = 300 V
V_{CC} = 30 V
V_{EB} = 5 V
L_B = 1 µH
V_{CL} = 200 µH

Figure 5. Test Circuit Inductive Load

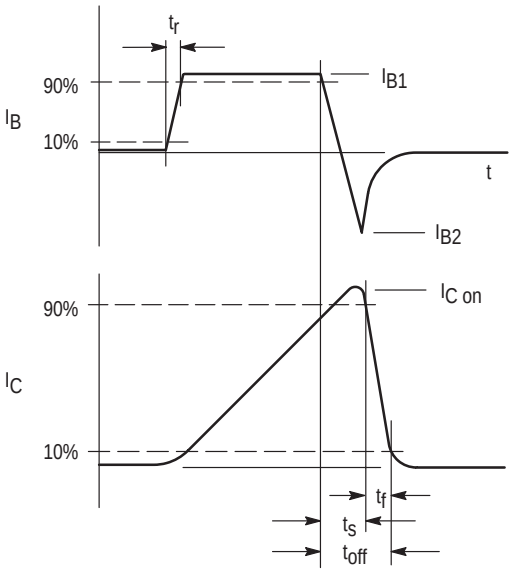


Figure 6. Switching Times Waveforms with Inductive Load

TEST CONDITIONS FOR ISOLATION TESTS*

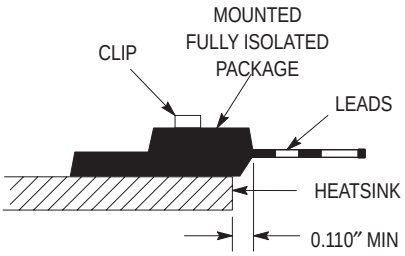


Figure 7. Screw or Clip Mounting Position for Isolation Test Number 1

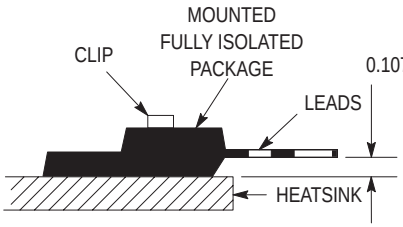


Figure 8. Clip Mounting Position for Isolation Test Number 2

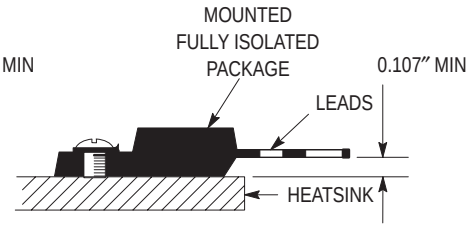


Figure 9. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together.

MOUNTING INFORMATION

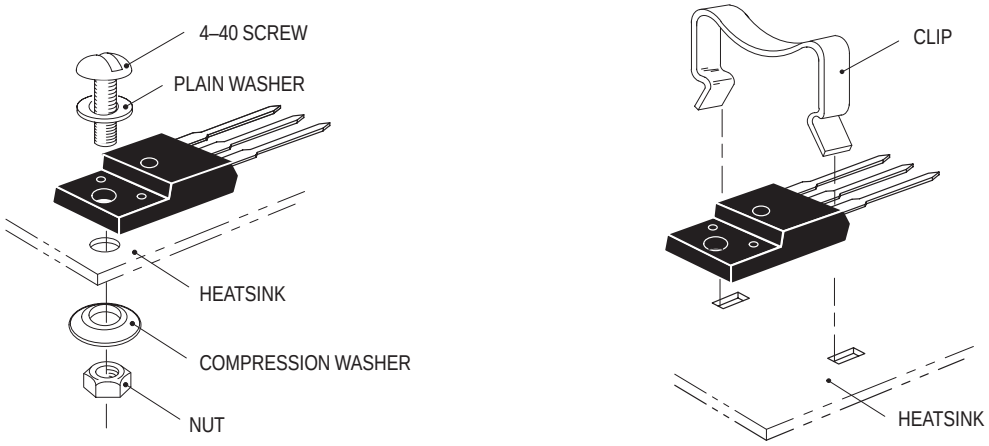


Figure 10. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

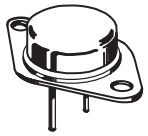
Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

BUT33

Designer's™ Data Sheet

SWITCHMODE Series NPN Silicon Power Darlington Transistors with Base-Emitter Speedup Diode

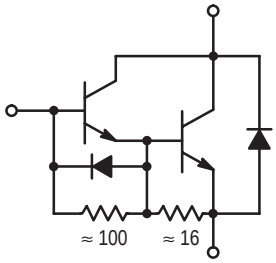
56 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTOR
600 VOLTS
250 WATTS



CASE 197A–05
TO–204AE
(TO–3)

The BUT33 Darlington transistor is designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated SWITCHMODE applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn Off Times
  - 800 ns Inductive Fall Time at 25°C (Typ)
  - 2.0 μs Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range –65 to 200°C



MAXIMUM RATINGS

Rating	Symbol	BUT33	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector–Emitter Voltage	V_{CEV}	600	Vdc
Emitter Base Voltage	V_{EB}	10	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	56 75	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	12 15	Adc
Free Wheel Diode Forward Current — Continuous — Peak	I_F I_{FM}	56 75	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 140	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purpose 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≦10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	 — —	 — —	 0.2 4.0	mAdc
Emitter Cutoff Current (V_{EB} = 20 V, I_C = 0)	I_{EBO}	—	—	350	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 20 A, V_{CE} = 5 V) (I_C = 36 A, V_{CE} = 5 V)	h_{FE}	 30 20	 — —	 — —	
Collector–Emitter Saturation Voltage (I_C = 20 A, I_B = 1 A) (I_C = 36 A, I_B = 3.6 A) (I_C = 44 A, I_B = 4.4 A) (I_C = 56 A, I_B = 11.2 A)	$V_{CE(sat)}$	 — — — —	 — — — —	 2.0 2.5 3.0 5.0	Vdc
Base–Emitter Saturation Voltage (I_C = 20 A, I_B = 1 A) (I_C = 36 A, I_B = 3.6 A) (I_C = 44 A, I_B = 4.4 A)	$V_{BE(sat)}$	 — — —	 — — —	 2.5 2.9 3.3	Vdc
Diode Forward Voltage (I_F = 44 A)	V_f	—	—	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load Clamped (Table 1)

Storage Time	T_C = 25°C	I_C = 36 A	t_s	—	2.0	3.3	μs
Fall Time		I_B = 3.6 A	t_f	—	0.8	1.6	μs
Storage Time	See Table 1		t_s	—	2.2	—	μs
Fall Time	T_C = 100°C	$V_{BE(off)}$ = 5 V	t_f	—	0.8	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≦ 2%.

TYPICAL CHARACTERISTICS

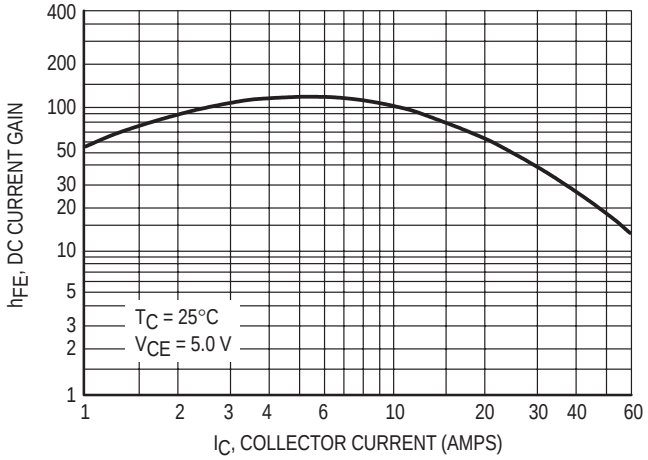


Figure 1. DC Current Gain

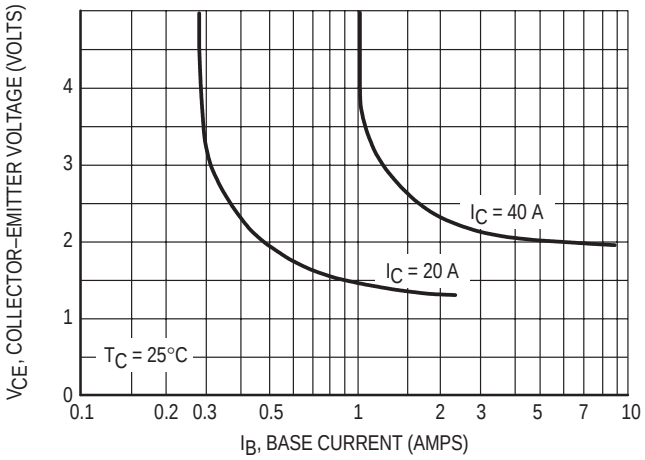


Figure 2. Collector Saturation Region

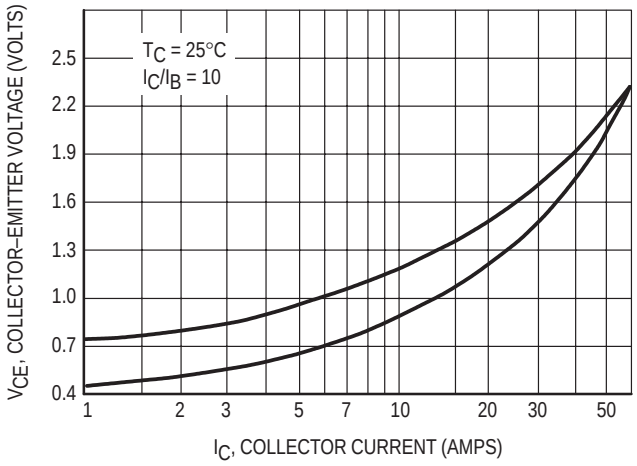


Figure 3. Collector–Emitter Saturation Voltage

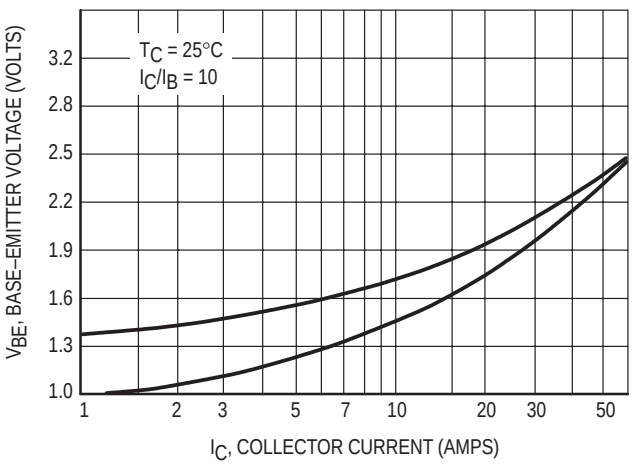


Figure 4. Base–Emitter Voltage

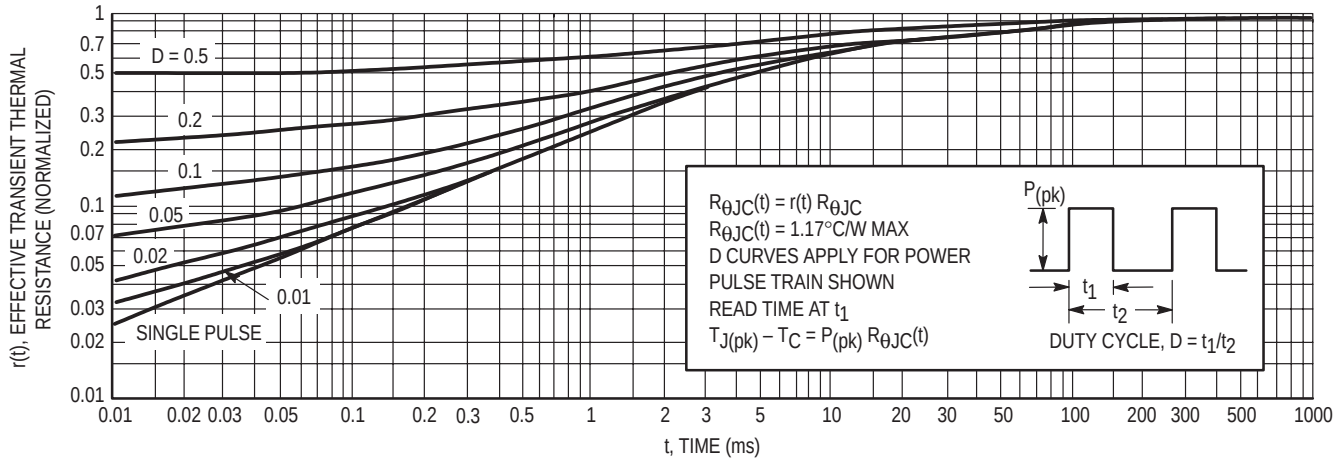


Figure 5. Thermal Response

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	TEST CIRCUIT for FREE–WHEEL DIODE
INPUT CONDITIONS	PW Varied to Attain I_C = 100 mA	PULSES δ = 3%	
CIRCUIT VALUES	L_{coil} = 10 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 10 V	
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT OUTPUT WAVEFORMS t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent		

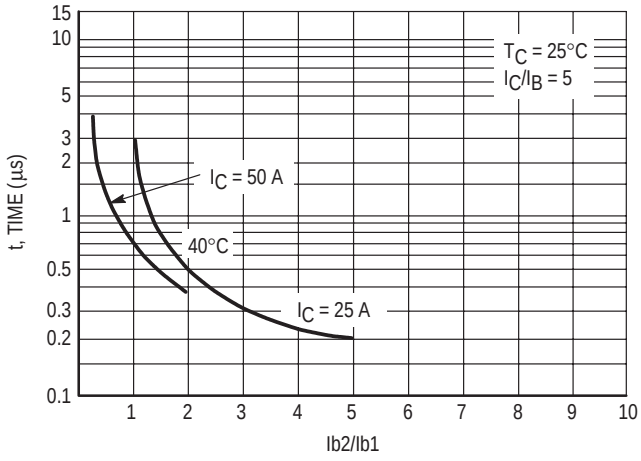


Figure 6. Fall Time versus IB2/IB1

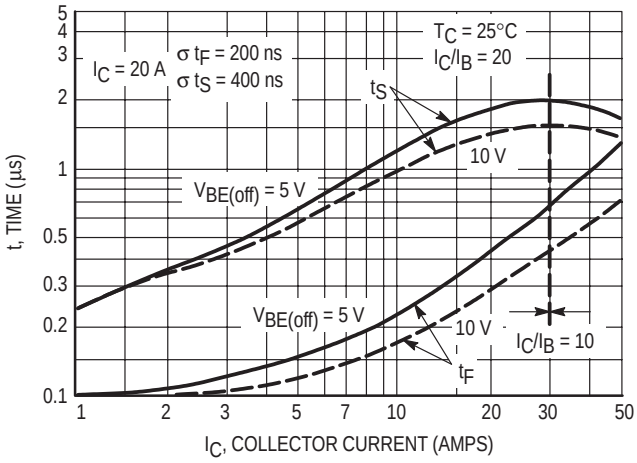


Figure 7. Turn–Off Time versus I_C

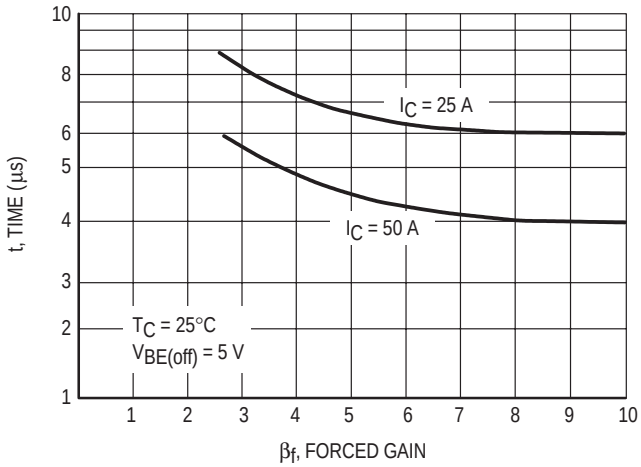


Figure 8. Storage Time versus Forced Gain

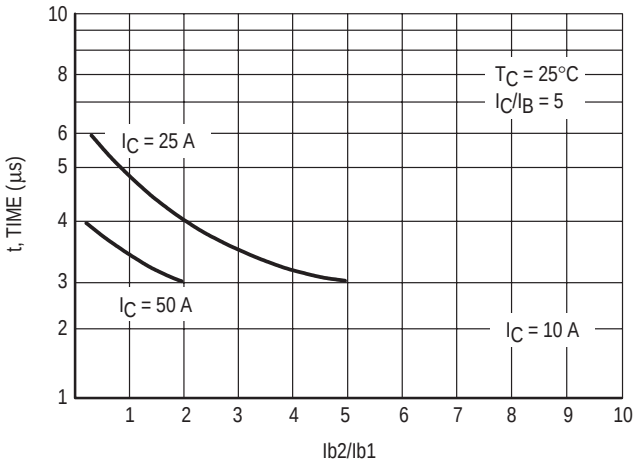


Figure 9. Storage Time versus Ib2/Ib1

FREE–WHEEL DIODE CHARACTERISTICS

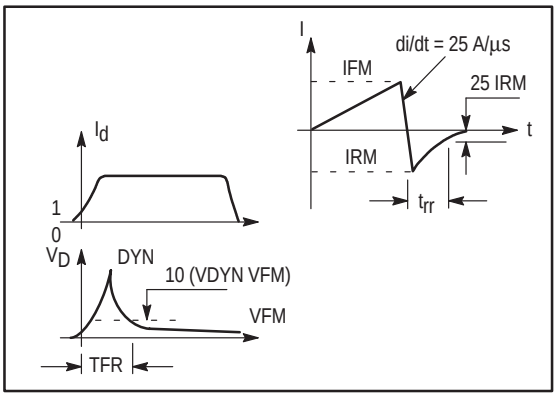


Figure 10. Free Wheel Diode Measurements

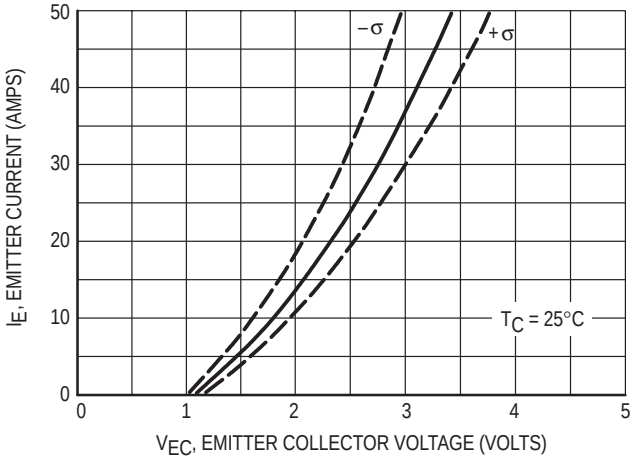


Figure 11. Forward Voltage

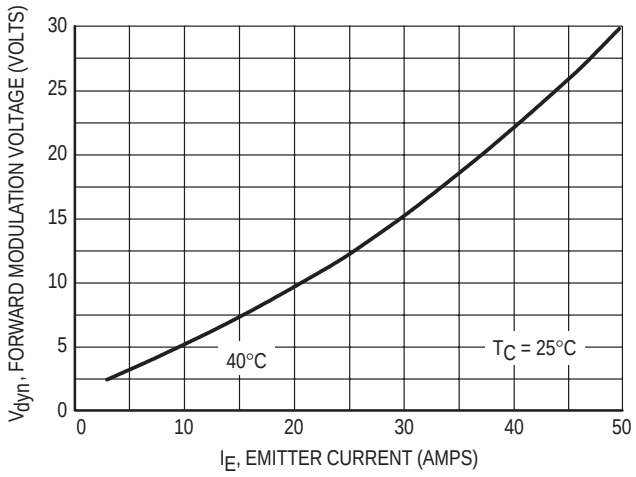


Figure 12. Forward Modulation Voltage

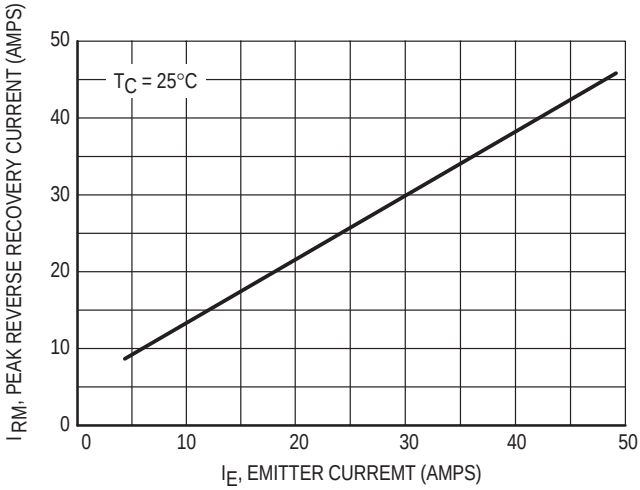


Figure 13. Peak Reverse Recovery Current

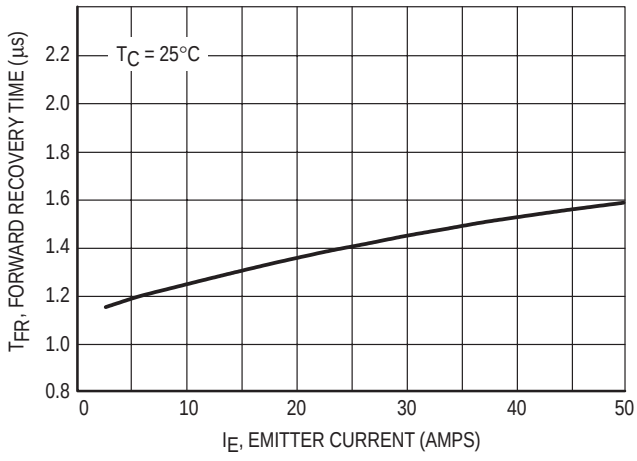


Figure 14. Forward Recovery Time

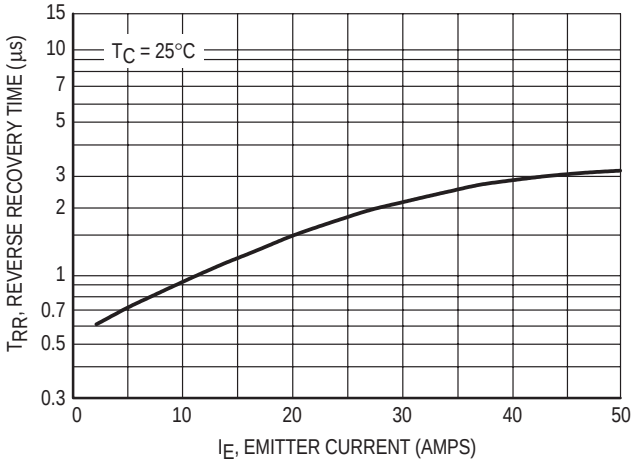


Figure 15. Reverse Recovery Time

The Safe Operating Area figures shown in Figures 16 and 17 are specified for the devices under the test conditiond shown.

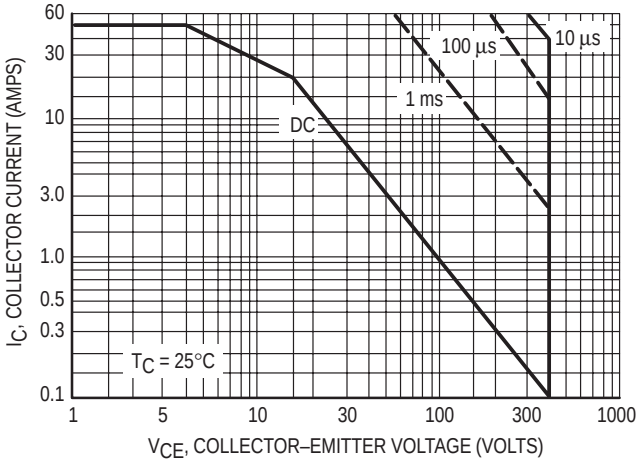


Figure 16. Safe Operating Area

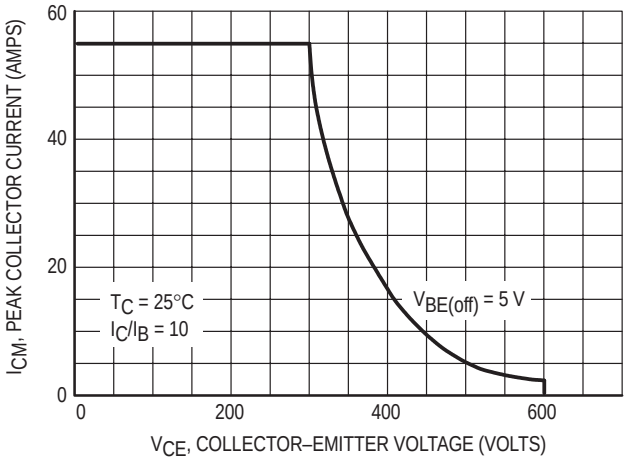


Figure 17. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

The data of Figure 16 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode Figure 17 gives the RBSOA characteristics.

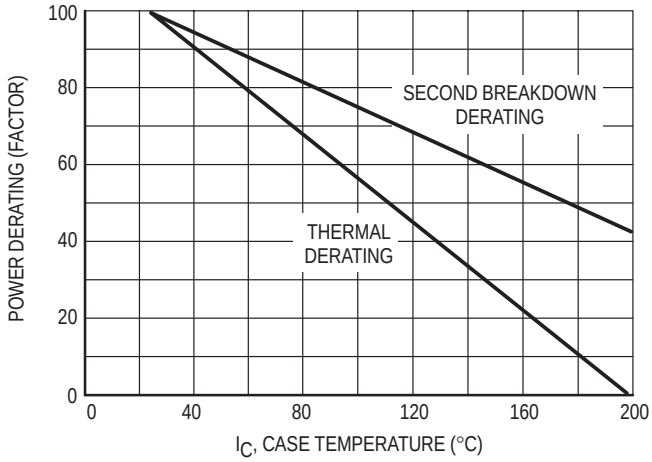


Figure 18. Power Derating

BUT34

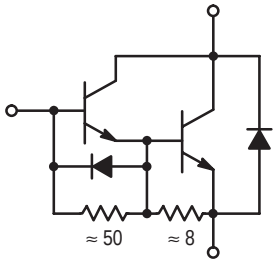
Designer's™ Data Sheet

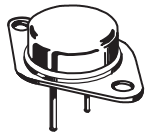
SWITCHMODE Series NPN Silicon Power Darlington Transistors with Base-Emitter Speedup Diode

50 AMPERES
NPN SILICON
POWER DARLINGTON
TRANSISTOR
850 VOLTS
250 WATTS

The BUT34 Darlington transistor is designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated SWITCHMODE applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn–Off Times
  - 0.7 μs Inductive Fall Time at 25°C (Typ)
  - 1.8 μs Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range –65 to 200°C





CASE 197A–05
TO–204AE
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	BUT34	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	500	Vdc
Collector–Emitter Voltage	V_{CEV}	850	Vdc
Emitter–Base Voltage	V_{EB}	10	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	50 75	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 15	Adc
Free Wheel Diode Forward Current — Continuous — Peak	I_F I_{FM}	50 75	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 140	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≦10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	500	—	—	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	 — —	 — —	 0.2 4.0	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)	I_{EBO}	—	—	350	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$		See Figure 16		
Clamped Inductive SOA with Base Reverse Biased	RBSOA		See Figure 17		
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 16 A, V_{CE} = 5 V) (I_C = 32 A, V_{CE} = 5 V)	h_{FE}	 30 15	 — —	 — —	
Collector–Emitter Saturation Voltage (I_C = 16 A, I_B = 0.8 A) (I_C = 32 A, I_B = 3.2 A) (I_C = 40 A, I_B = 4 A) (I_C = 50 A, I_B = 10 A)	$V_{CE(sat)}$	 — — — —	 — — — —	 2.0 3.0 3.5 5.0	Vdc
Base–Emitter Saturation Voltage (I_C = 16 A, I_B = 0.8 A) (I_C = 32 A, I_B = 3.2 A) (I_C = 40 A, I_B = 4 A)	$V_{BE(sat)}$	 — — —	 — — —	 2.5 2.9 3.3	Vdc
Diode Forward Voltage (I_F = 40 A)	V_f	—	—	4.0	Vdc

SWITCHING CHARACTERISTICS

Inductive Load, Clamped (Table 1)

Storage Time	T_C = 25°C	See Table 1	t_s	—	1.8	3.0	μs
Fall Time		I_C = 32 A	t_f	—	0.7	1.5	μs
Storage Time	T_C = 100°C	I_{B1} = 3.2 A	t_s	—	2.2	—	μs
Fall Time		$V_{BE(off)}$ = 5 V	t_f	—	0.8	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≦ 2%.

TYPICAL CHARACTERISTICS

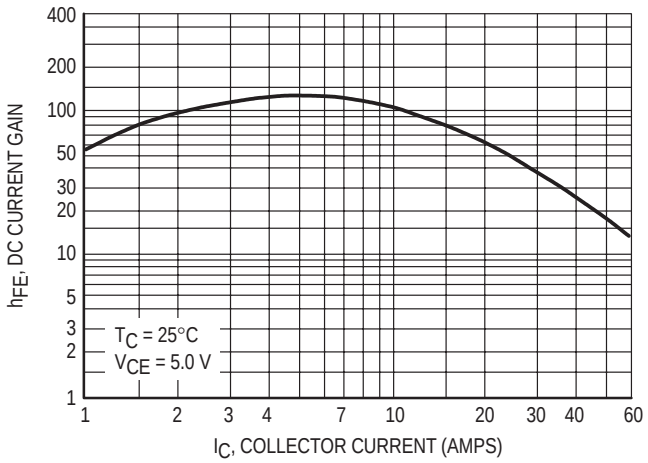


Figure 1. DC Current Gain

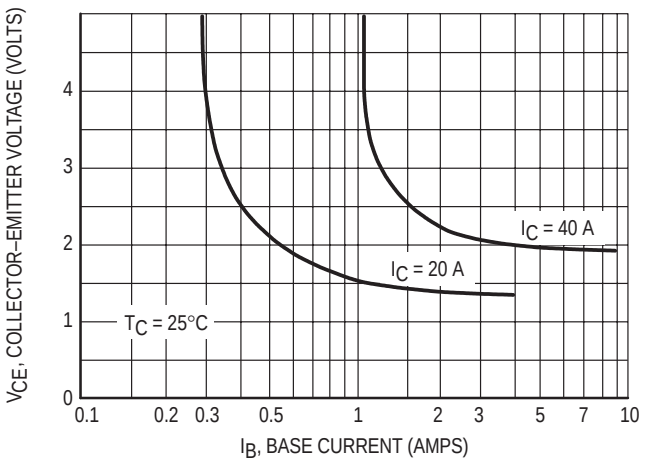


Figure 2. Collector Saturation Region

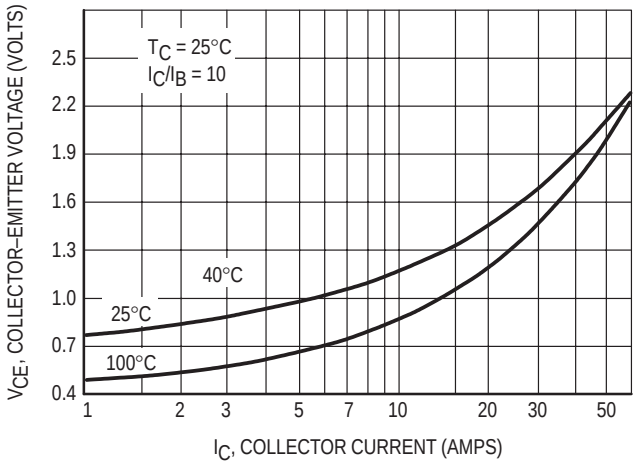


Figure 3. Collector–Emitter Saturation Voltage

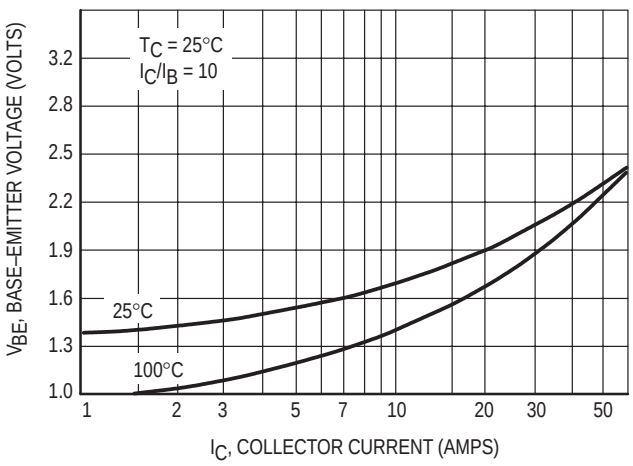


Figure 4. Base–Emitter Voltage

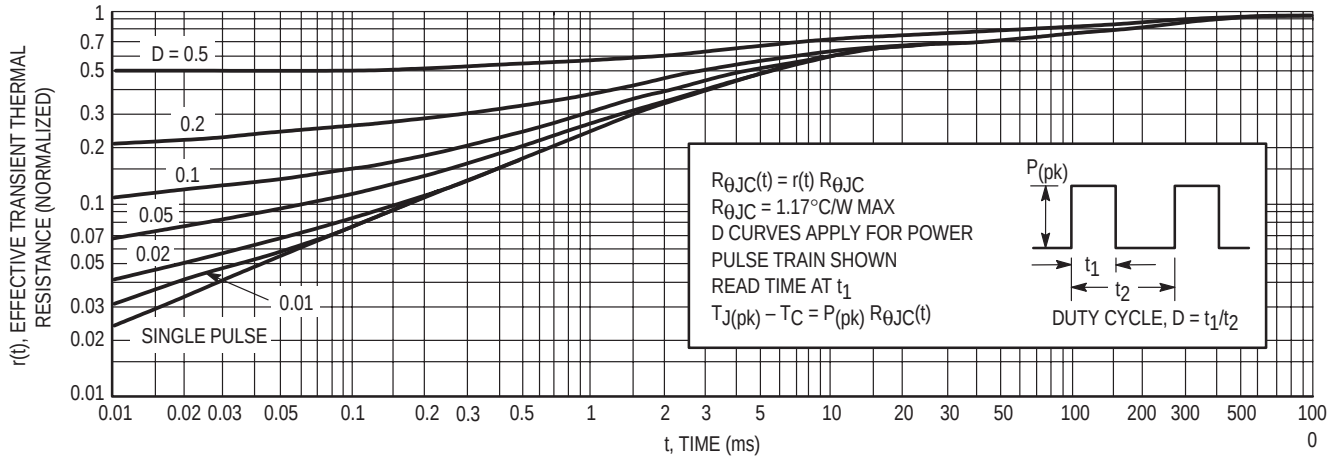


Figure 5. Thermal Response

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	TEST CIRCUIT for FREE–WHEEL DIODE
INPUT CONDITIONS	20 Ω, 5 V, 0, 1, 2 PW Varied to Attain I_C = 100 mA	+10 V, 33 2 W, D1, 22 µF, 2N6438, MR854, 160, 680 pF, MM3735, 220, 100, D1 D2 D3 D4 1N4934, PULSES δ = 3%, 2N3763, 680 pF, 100, 1 µF, I_{b1} ADJUST, I_{b2} ADJUST, dT_b ADJUST, dT, D3, D4, 22, 33 2 W, 2N6339, V_{CC}	DRIVER, V_D, I_D
CIRCUIT VALUES	L_{coil} = 10 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 10 V	
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT: TUT, 1, INPUT, SEE ABOVE FOR DETAILED CONDITIONS, 1N4937 OR EQUIVALENT, R_{coil}, L_{coil}, V_{clamp}, V_{CC}, 2, RS = 0.1 Ω OUTPUT WAVEFORMS: I_C, I_{CM}, t_f Clamped, t_1, t_f, t, V_{CE}, V_{CEM}, V_{clamp}, TIME, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	AV up to 50 V, CRONETICS PG130 up to 50 V, 510, 5 µs 1%, V_D, I_D

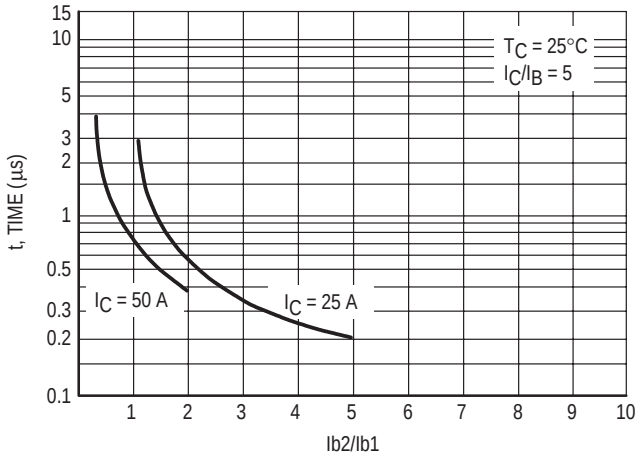


Figure 6. Fall Time versus IB2/IB1

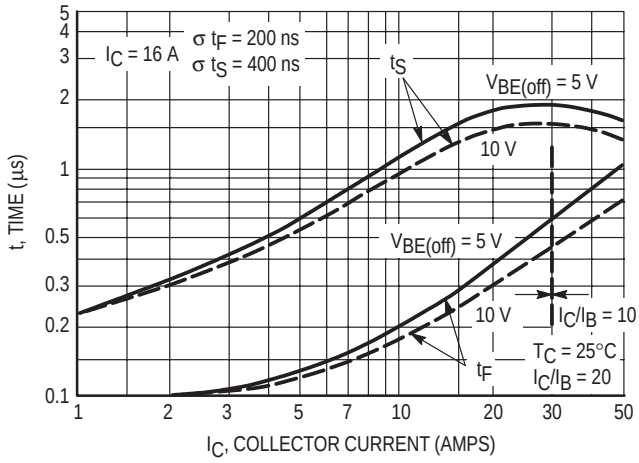


Figure 7. Turn–Off Time versus I_C

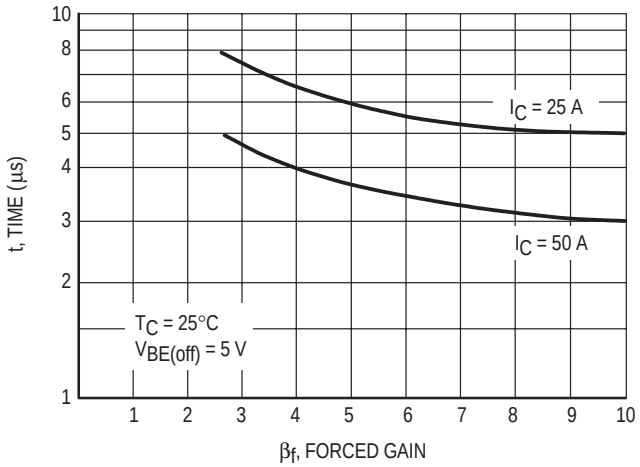


Figure 8. Storage Time versus Forced Gain

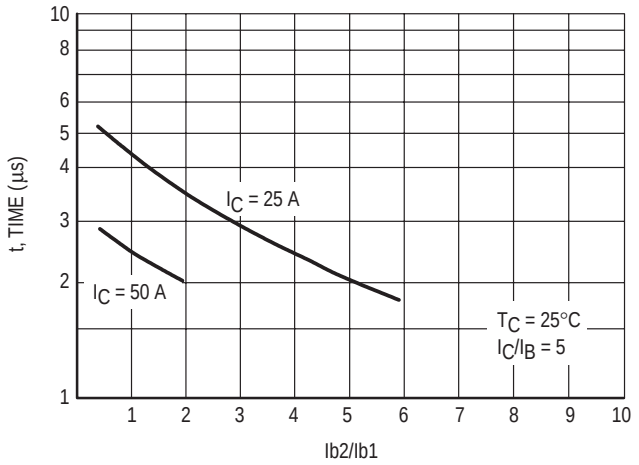


Figure 9. Storage Time versus Ib2/Ib1

FREE–WHEEL DIODE CHARACTERISTICS

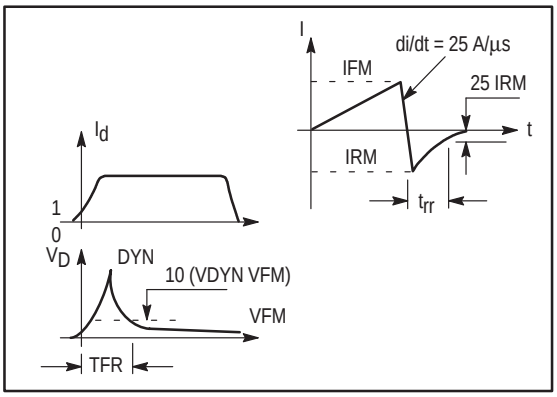


Figure 10. Free Wheel Diode Measurements

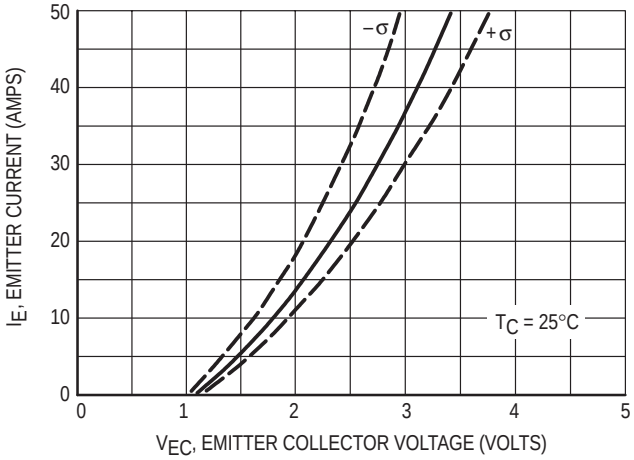


Figure 11. Forward Voltage

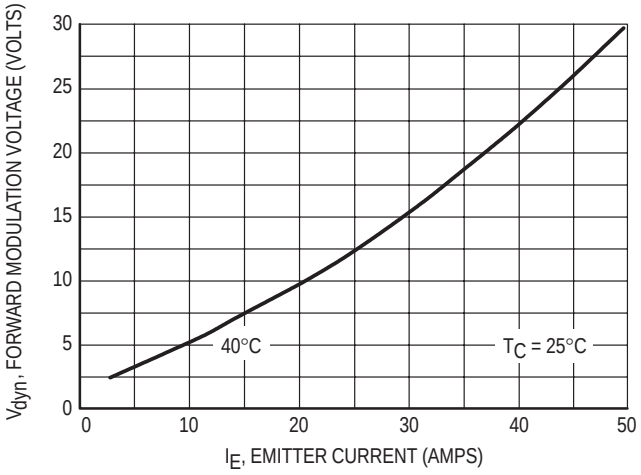


Figure 12. Forward Modulation Voltage

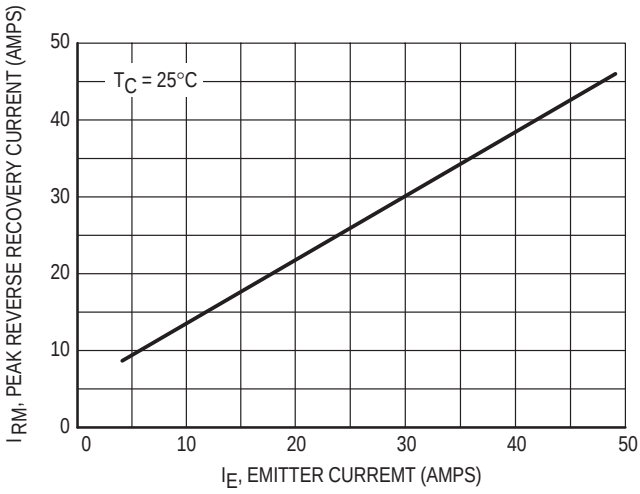


Figure 13. Peak Reverse Recovery Current

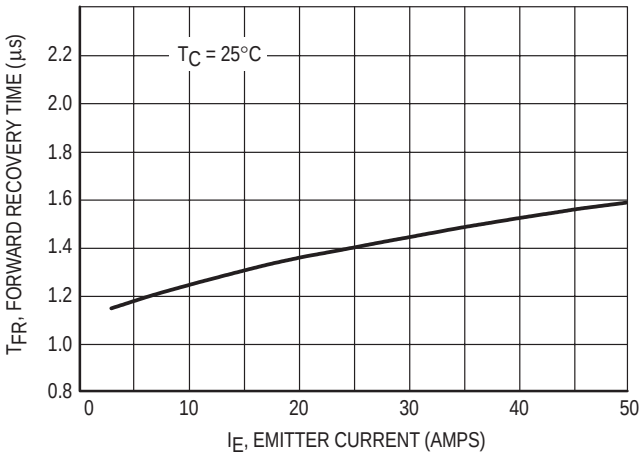


Figure 14. Forward Recovery Time

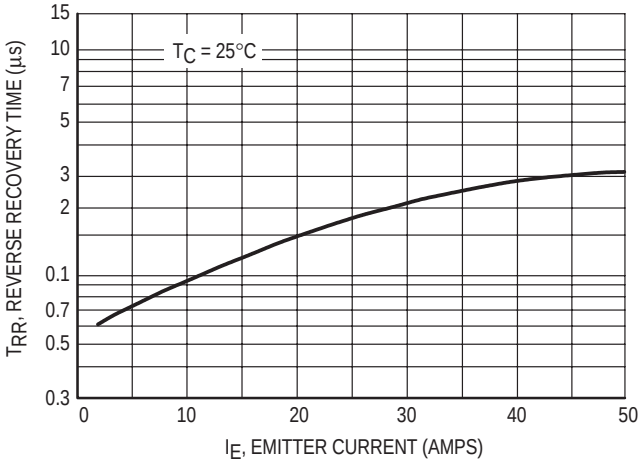


Figure 15. Reverse Recovery Time

The Safe Operating Area figures shown in Figures 16 and 17 are specifed for these devices under the test conditions shown.

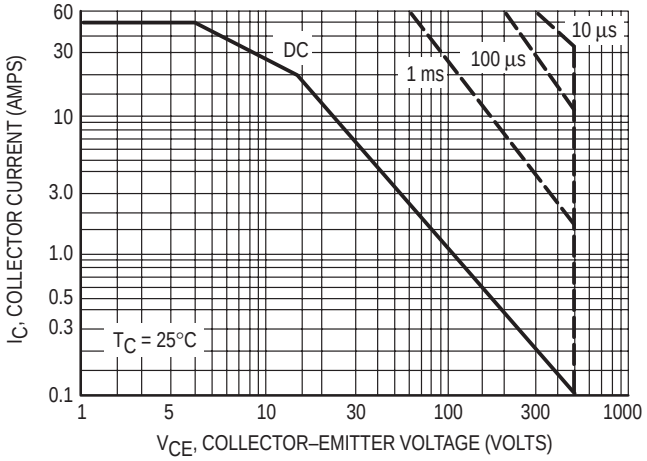


Figure 16. Safe Operating Area

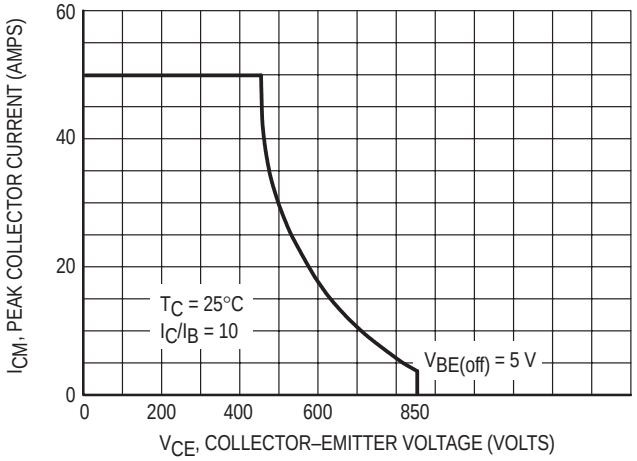


Figure 17. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subject to greater dissipation than the curves indicate.

The data of Figure 16 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

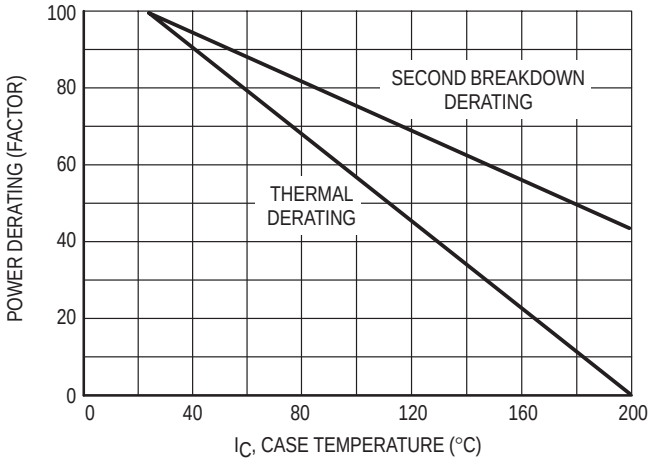


Figure 18. Power Derating

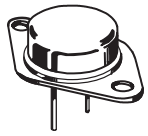
BUV11

SWITCHMODE Series NPN Silicon Power Transistor

. . . designed for high current, high speed, high power applications.

- High DC current gain; h_{FE} min. = 20 at I_C = 6 A
- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 0.6 V at I_C = 6 A
- Very fast switching times:
  T_F max. = 0.8 μs at I_C = 12 A

20 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
200 VOLTS
150 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	200	Vdc
Collector–Base Voltage	V_{CBO}	250	Vdc
Emitter–Base Voltage	V_{EBO}	7	Vdc
Collector–Emitter Voltage (V_{BE} = –1.5 V)	V_{CEX}	250	Vdc
Collector–Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	240	Vdc
Collector–Current— Continuous — Peak (pw ≤ 10 ms)	I_C I_{CM}	20 25	Adc Apk
Base–Current continuous	I_B	4	Adc
Total Power Dissipation @ T_C = 25°C	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

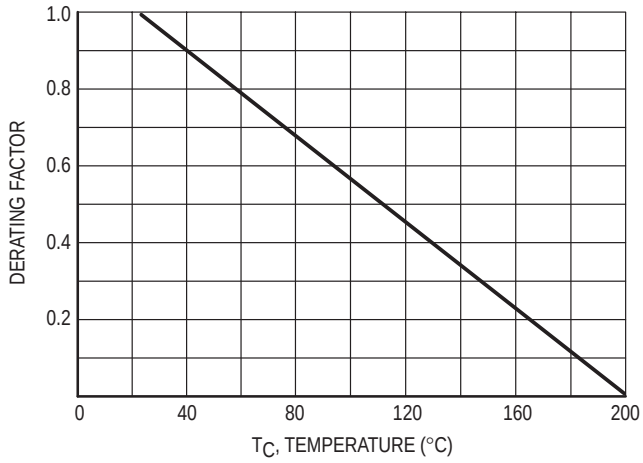


Figure 1. Power Derating

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Bias (V_{CE} = 250 V, V_{BE} = –1.5 V) (V_{CE} = 250 V, V_{BE} = –1.5 V, T_C = 125°C)	I_{CEX}		1.5 6	mAdc
Collector–Emitter Cutoff Current (V_{CE} = 160 V)	I_{CEO}		1.5	mAdc
Emitter–Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter–Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 30 V, t = 1 s) (V_{CE} = 140 V, t = 1 s)	$I_{S/b}$	5.0 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 6 A, V_{CE} = 2 V) (I_C = 12 A, V_{CE} = 4 V)	h_{FE}	20 10	60	
Collector–Emitter Saturation Voltage (I_C = 6 A, I_B = 0.6 A) (I_C = 12 A, I_B = 1.5 A)	$V_{CE(sat)}$		0.6 1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 12 A, I_B = 1.5 A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 1 A, f = 4 MHz)	f_T	8.0		MHz
SWITCHING CHARACTERISTICS (Resistive Load)				
Turn–on Time	(I_C = 12 A, I_{B1} = I_{B2} = 1.5 A, V_{CC} = 150 V, T_C = 12.5 Ω)	t_{on}	0.8	µs
Storage Time		t_s	1.8	
Fall Time		t_f	0.4	

[1] Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

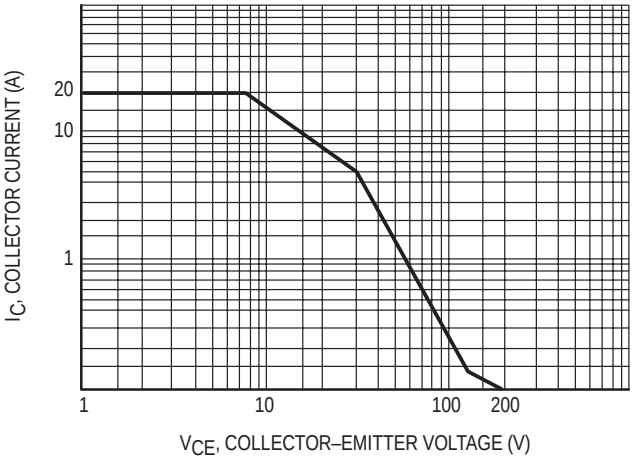


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown.

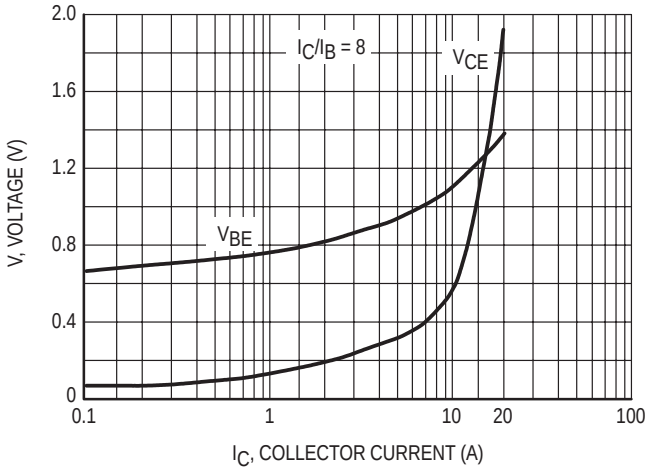


Figure 3. "On" Voltages

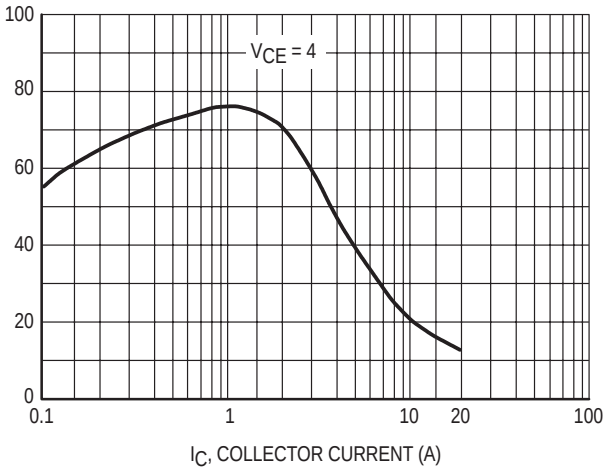


Figure 4. DC Current Gain

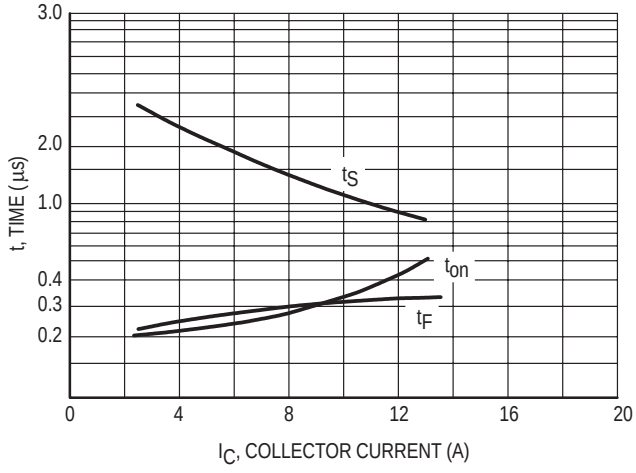
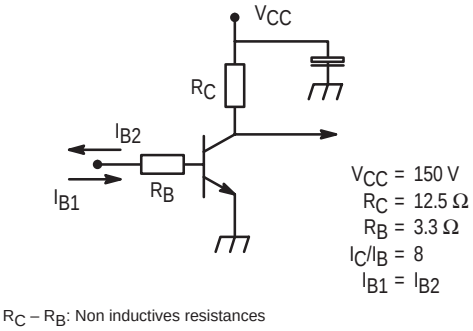


Figure 5. Switching Times versus Collector Current



$R_C - R_B$: Non inductives resistances

Figure 6. Switching Times Test Circuit

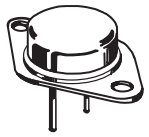
BUV20

SWITCHMODE Series
NPN Silicon Power Transistor

50 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
125 VOLTS
250 WATTS

. . . designed for high speed, high current, high power applications.

- High DC current gain:
  h_{FE} min = 20 at I_C = 25 A
  = 10 at I_C = 50 A
- Low $V_{CE(sat)}$:
  $V_{CE(sat)}$ max. = 0.6 V at I_C = 25 A
  = 1.2 V at I_C = 50 A
- Very fast switching times:
  T_F = 0.25 µs at I_C = 50 A



CASE 197A–05
TO–204AE
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emititer Voltage	$V_{CEO(sus)}$	125	Vdc
Collector–Base Voltage	V_{CBO}	160	Vdc
Emitter–Base Voltage	V_{EBO}	7	Vdc
Collector–Emitter Voltage (V_{BE} = –1.5 V)	V_{CEX}	160	Vdc
Collector–Emitter voltage (R_{BE} = 100 Ω)	V_{CER}	150	Vdc
Collector–Current — Continuous — Peak (pw ≤ 10 ms)	I_C I_{CM}	50 60	Adc Apk
Base–Current continuous	I_B	10	Adc
Total Power Dissipation @ T_C = 25°C	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

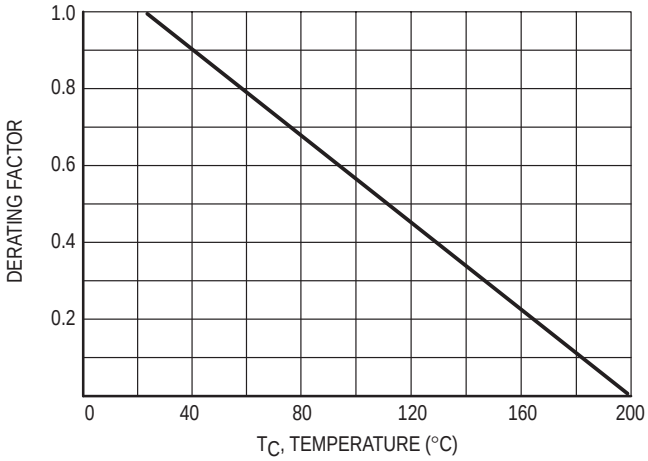


Figure 1. Power Derating

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS[1]				
Collector–Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	125		Vdc
Collector Cutoff Current at Reverse Bias (V_{CE} = 140 V, V_{BE} = – 1.5 V) (V_{CE} = 140 V, V_{BE} = – 1.5 V, T_C = 125°C)	I_{CEX}		3.0 12	mAdc
Collector–Emitter Cutoff Current (V_{CE} = 100 V)	I_{CEO}		3.0	mAdc
Emitter–Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter–Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 20 V, t = 1 s) (V_{CE} = 40 V, t = 1 s)	$I_{S/b}$	12 1.5		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 25 A, V_{CE} = 2 V) (I_C = 50 A, V_{CE} = 4 V)	h_{FE}	20 10	60	
Collector–Emitter Saturation Voltage (I_C = 25 A, I_B = 2.5 A) (I_C = 50 A, I_B = 5 A)	$V_{CE(sat)}$		0.6 1.2	Vdc
Base–Emitter Saturation Voltage (I_C = 50 A, I_B = 5 A)	$V_{BE(sat)}$		2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 2 A, f = 4 MHz)	f_T	8.0		MHz
SWITCHING CHARACTERISTICS (Resistive Load)				
Turn–on Time	(I_C = 50 A, I_{B1} = I_{B2} = 5 A, V_{CC} = 30 V, R_C = 0.6 Ω)	t_{on}		1.5 μs
Storage Time		t_s		1.2
Fall Time		t_f		0.25

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

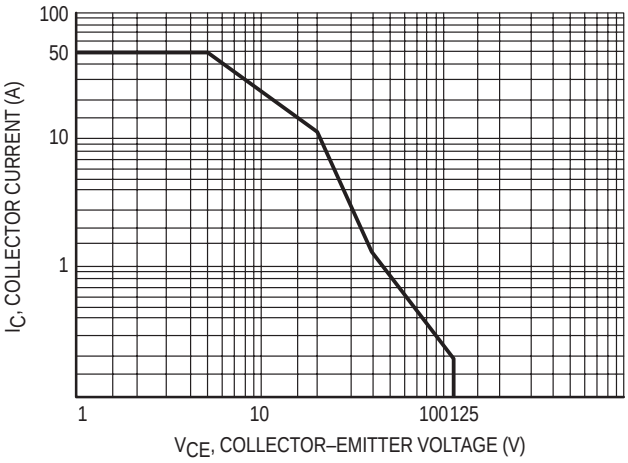


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C. $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

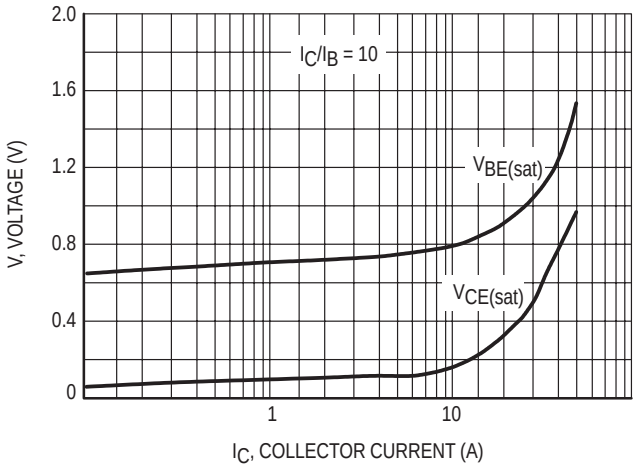


Figure 3. “On” Voltages

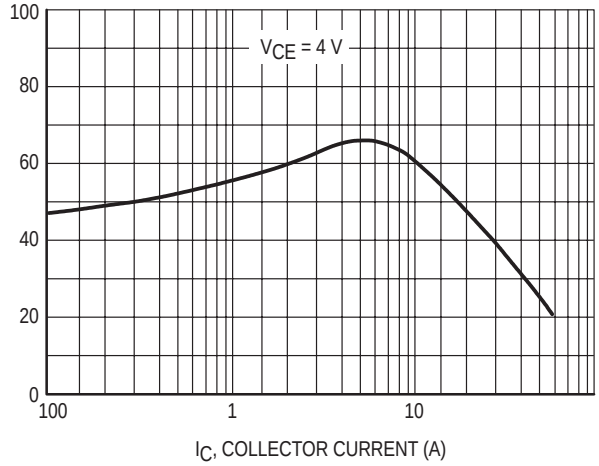


Figure 4. DC Current Gain

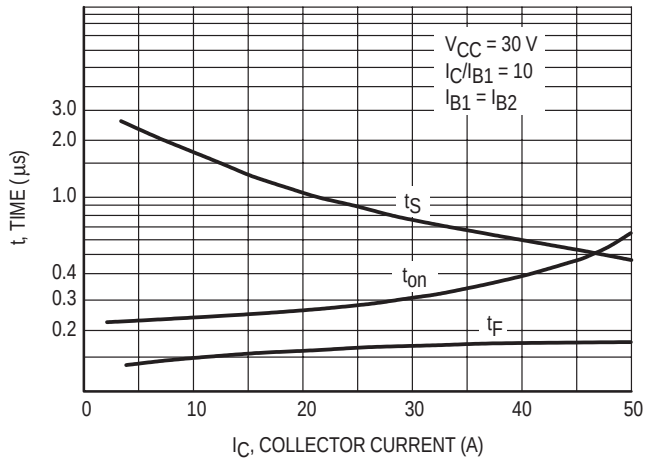
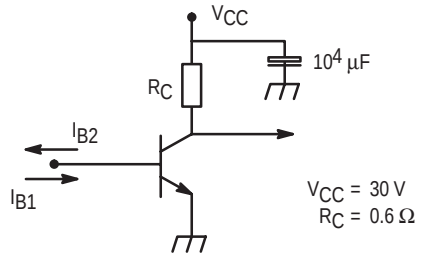


Figure 5. Resistive Switching Performance



R_C — Non inductive resistance

Figure 6. Switching Times Test Circuit

BUV21

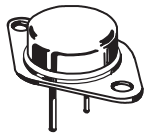
SWITCHMODE Series
NPN Silicon Power Transistor

40 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
200 VOLTS
250 WATTS

. . . designed for high speed, high current, high power applications.

- High DC current gain:
  h_{FE} min. = 20 at I_C = 12 A
- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 0.6 V at I_C = 8 A

Very fast switching times:
TF max. = 0.4 μs at I_C = 25 A



CASE 197A–05
TO–204AE
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	200	Vdc
Collector–Base Voltage	V_{CBO}	250	Vdc
Emitter–Base Voltage	V_{EBO}	7	Vdc
Collector–Emitter Voltage (V_{BE} = –1.5 V)	V_{CEX}	250	Vdc
Collector–Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	240	Vdc
Collector–Current — Continuous — Peak (pw ≤ 10 ms)	I_C I_{CM}	40 50	Adc Apk
Base–Current continuous	I_B	8	Adc
Total Power Dissipation @ T_C = 25°C	P_D	150	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

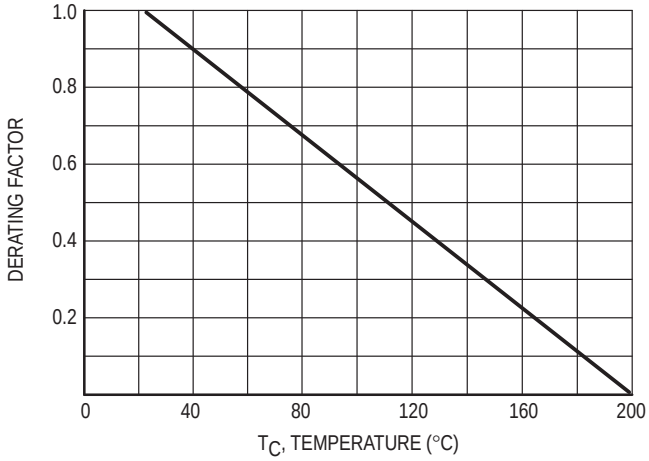


Figure 1. Power Derating

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS[1]				
Collector–Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Bias: (V_{CE} = 250 V, V_{BE} = –1.5 V) (V_{CE} = 250 V, V_{BE} = –1.5 V, T_C = 125°C)	I_{CEX}		3.0 12.0	mAdc
Collector–Emitter Cutoff Current (V_{CE} = 160 V)	I_{CEO}		3.0	mAdc
Emitter–Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter–Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 20 V, t = 1 s) (V_{CE} = 140 V, t = 1 s)	$I_{S/b}$	12 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 12 A, V_{CE} = 2 V) (I_C = 25 A, V_{CE} = 4 V)	h_{FE}	20 10	60	
Collector–Emitter Saturation Voltage (I_C = 12 A, I_B = 1.2 A) (I_C = 25 A, I_B = 3 A)	$V_{CE(sat)}$		0.6 1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 25 A, I_B = 3 A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (V_{CE} = 15 V, I_C = 2 A, f = 4 MHz)	f_T	8.0		MHz
SWITCHING CHARACTERISTICS (Resistive Load)				
Turn-on Time	t_{on}		1.0	μs
Storage Time (I_C = 25 A, I_{B1} = I_{B2} = 3 A, V_{CC} = 100 V, R_C = 4 Ω)	t_s		1.8	
Fall Time	t_f		0.4	

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

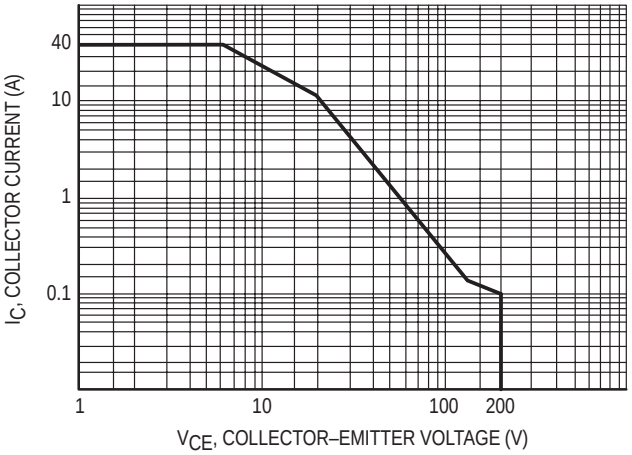


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C, $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

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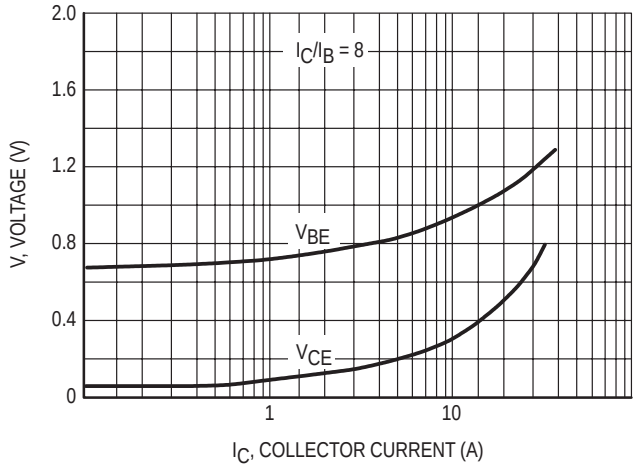


Figure 3. "On" Voltages

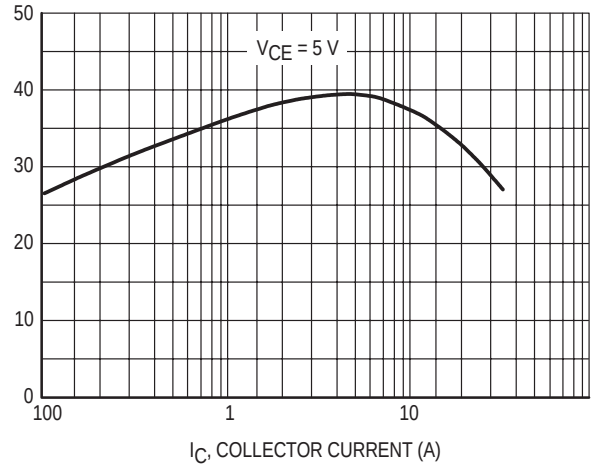


Figure 4. DC Current Gain

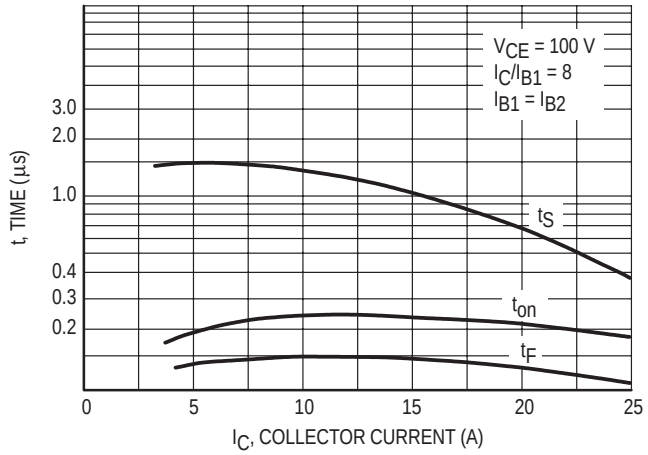
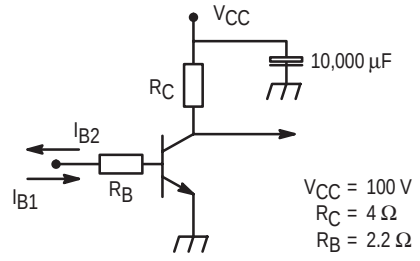


Figure 5. Resistive Switching Performance



$R_C - R_B$: Non inductive resistances

Figure 6. Switching Times Test Circuit

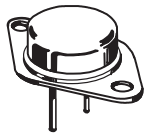
BUV22

SWITCHMODE Series
NPN Silicon Power Transistor

. . . designed for high current, high speed, high power applications.

- High DC current gain: HFE min. = 20 at I_C = 10 A
- Low $V_{CE(sat)}$: $V_{CE(sat)}$ max. = 1.0 V at I_C = 10 A
- Very fast switching times:
  T_F max. = 0.35 μs at I_C = 20 A

40 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
250 VOLTS
250 WATTS



CASE 197A–05
TO–204AE
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	250	Vdc
Collector–Base Voltage	V_{CBO}	300	Vdc
Emitter–Base Voltage	V_{EBO}	7	Vdc
Collector–Emitter Voltage (V_{BE} = –1.5 V)	V_{CEX}	300	Vdc
Collector–Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	290	Vdc
Collector–Current — Continuous — Peak (pw ≤ 10 ms)	I_C I_{CM}	40 50	Adc Apk
Base–Current continuous	I_B	8	Adc
Total Power Dissipation @ T_C = 25°C	P_D	250	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

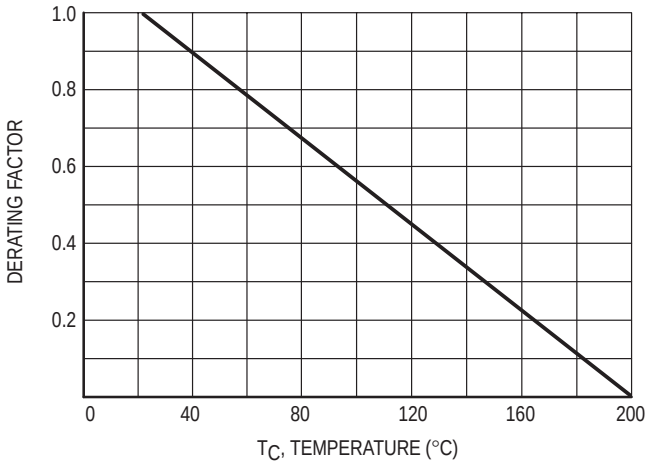


Figure 1. Power Derating

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS[1]				
Collector–Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	250		Vdc
Collector Cutoff Current at Reverse Bias (V_{CE} = 300 V, V_{BE} = –1.5 V) (V_{CE} = 300 V, V_{BE} = –1.5 V, T_C = 125°C)	I_{CEX}		3.0 12.0	mAdc
Collector–Emitter Cutoff Current (V_{CE} = 200 V)	I_{CEO}		3.0	mAdc
Emitter–Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter–Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 20 V, t = 1 s) (V_{CE} = 140 V, t = 1 s)	$I_{S/b}$	12 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 10 A, V_{CE} = 4 V) (I_C = 20 A, V_{CE} = 4 V)	h_{FE}	20 10	60	
Collector–Emitter Saturation Voltage (I_C = 10 A, I_B = 1 A) (I_C = 20 A, I_B = 2.5 A)	$V_{CE(sat)}$		1.0 1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 40 A, I_B = 4 A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 2 A, f = 4 MHz)	f_T	8.0		MHz
SWITCHING CHARACTERISTICS (Resistive Load)				
Turn–on Time	(I_C = 20 A, I_{B1} = I_{B2} = 2.5 A, V_{CC} = 100 V, R_C = 5 Ω)	t_{on}	0.8	μs
Storage Time		t_s	2.0	
Fall Time		t_f	0.35	

[1]Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

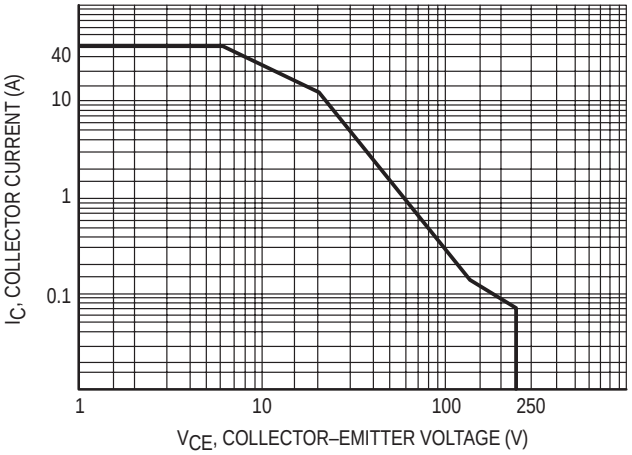


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown.

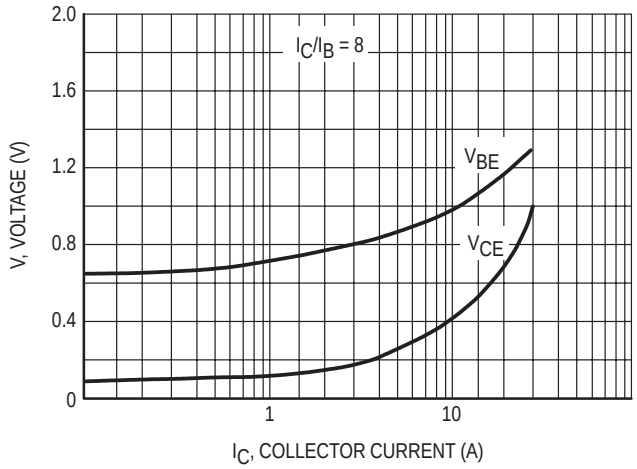


Figure 3. "On" Voltages

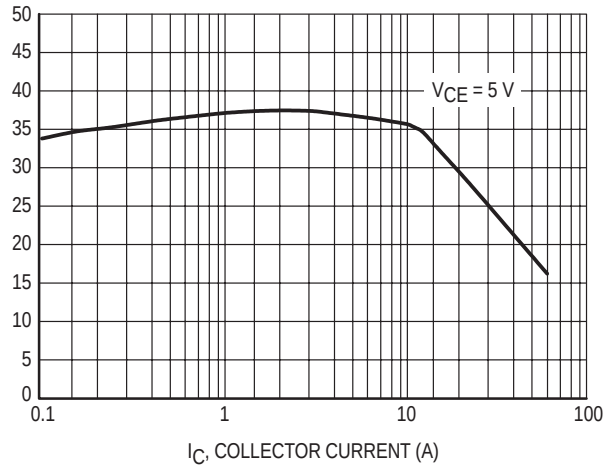


Figure 4. DC Current Gain

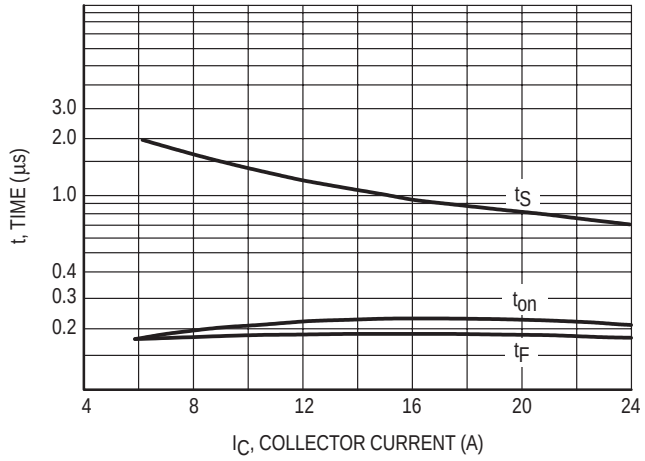
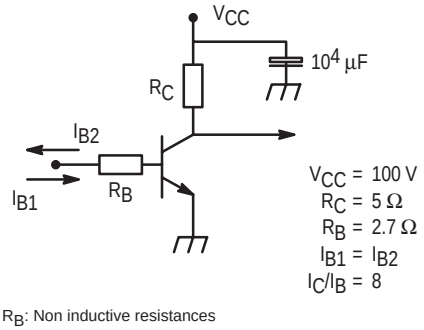


Figure 5. Resistive Switching Performance



$R_C - R_B$: Non inductive resistances

Figure 6. Switching Times Test Circuit

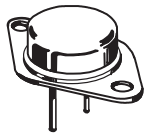
BUV23

SWITCHMODE Series
NPN Silicon Power Transistor

. . . designed for high current, high speed, high power applications.

- High DC current gain: HFE min. = 15 at I_C = 8 A
- Low $V_{CE(sat)}$, $V_{CE(sat)}$ max. = 0.8 V at I_C = 8 A
- Very fast switching times:
  T_F = 0.4 μs at I_C = 16 A

30 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
325 VOLTS
250 WATTS



CASE 197A–05
TO–204AE
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	325	Vdc
Collector–Base Voltage	V_{CBO}	400	Vdc
Emitter–Base Voltage	V_{EBO}	7	Vdc
Collector–Emitter Voltage (V_{BE} = –1.5 V)	V_{CEX}	400	Vdc
Collector–Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	390	Vdc
Collector–Current— Continuous — Peak (pw ≤ 10 ms)	I_C I_{CM}	30 40	Adc Apk
Base–Current continuous	I_B	6	Adc
Total Power Dissipation @ T_C = 25°C	P_D	250	Watts
Operating and Storage JunctionTemperature Range	T_J,T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.7	°C/W

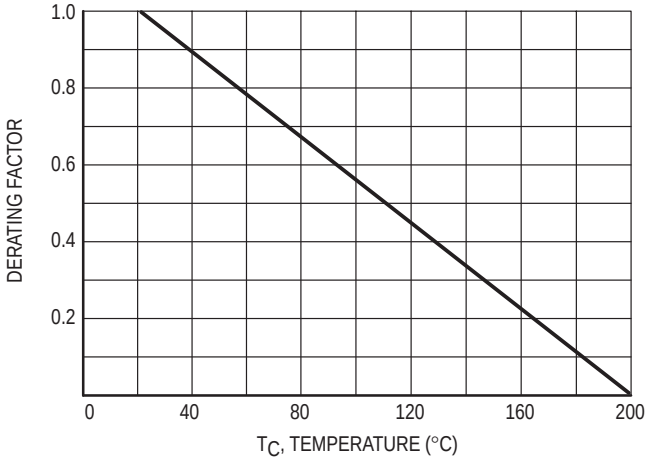


Figure 1. Power Derating

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS[1]				
Collector–Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	325		Vdc
Collector Cutoff Current at Reverse Bias (V_{CE} = 400 V, V_{BE} = –1.5 V) (V_{CE} = 400 V, V_{BE} = –1.5 V, T_C = 125°C)	I_{CEX}		 3.0 12	mAdc
Collector–Emitter Cutoff Current (V_{CE} = 260 V)	I_{CEO}		3.0	mAdc
Emitter–Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter–Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 20 V, t = 1 s) (V_{CE} = 140 V, t = 1 s)	$I_{S/b}$	 12 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 8 A, V_{CE} = 4 V) (I_C = 16 A, V_{CE} = 4 V)	h_{FE}	 15 8	 60	
Collector–Emitter Saturation Voltage (I_C = 8 A, I_B = 1.6 A) (I_C = 16 A, I_B = 3.2 A)	$V_{CE(sat)}$		 0.8 1.0	Vdc
Base–Emitter Saturation Voltage (I_C = 16 A, I_B = 3.2 A)	$V_{BE(sat)}$		1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 2 A, f = 4 MHz)	f_T	8.0		MHz
SWITCHING CHARACTERISTICS (Resistive Load)				
Turn–on Time	(I_C = 16 A, I_{B1} = I_{B2} = 3.2 A, V_{CC} = 100 V, R_C = 6.25 Ω)	t_{on}	0.8	μs
Storage Time		t_s	2.5	
Fall Time		t_f	0.4	

[1]Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

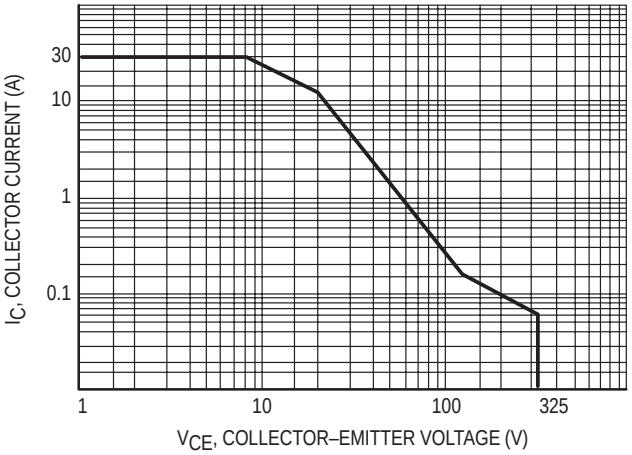


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures. thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown.

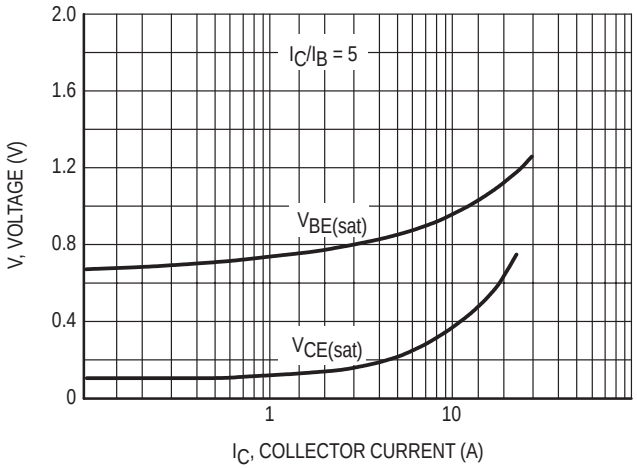


Figure 3. "On" Voltages

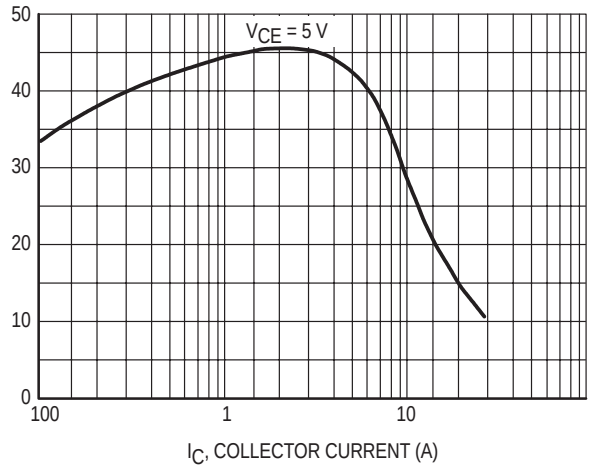


Figure 4. DC Current Gain

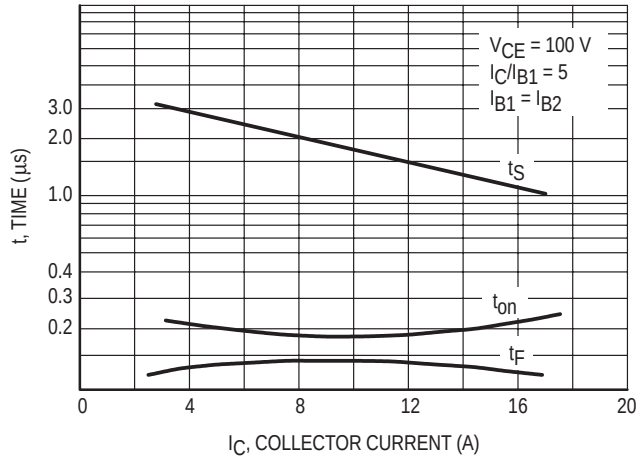
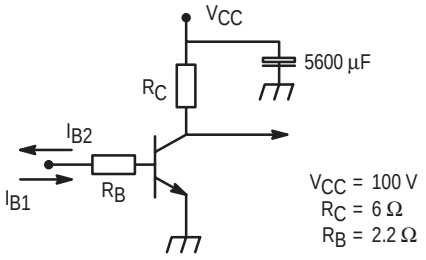


Figure 5. Resistive Switching Performance



$R_C - R_B$: Non inductive resistances

Figure 6. Switching Times Test Circuit

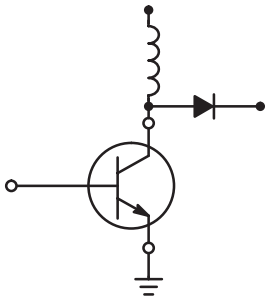
BUV48
BUV48A

SWITCHMODE II Series
NPN Silicon Power Transistors

15 AMPERES
NPN SILICON
POWER TRANSISTORS
400 AND 450 VOLTS
$V_{(BR)CEO}$
850 – 1000 VOLTS
$V_{(BR)CEX}$
150 WATTS

The BUV48/BUV48A transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated switchmode applications such as:

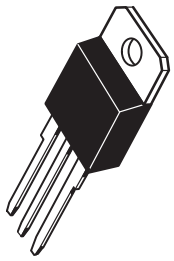
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn–Off Times
60 ns Inductive Fall Time — 25°C (Typ)
120 ns Inductive Crossover Time — 25°C (Typ)

Operating Temperature Range –65 to +175°C

100°C Performance Specified for:
Reverse–Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltage
Leakage Currents (125°C)



CASE 340D–01
TO–218 TYPE

MAXIMUM RATINGS

Rating	Symbol	BUV48	BUV48A	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector–Emitter Voltage (V_{BE} = –1.5 V)	V_{CEX}	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current — Continuous — Peak (1) — Overload	I_C I_{CM} I_{OI}	15 30 60		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	5 20		Adc
Total Power Dissipation — T_C = 25°C — T_C = 100°C Derate above 25°C	P_D	150 75 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +175		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector–Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$				Vdc
(I_C = 200 mA, I_B = 0) L = 25 mH	BUV48		400	—	—	
	BUV48A		450	—	—	
Collector Cutoff Current		I_{CEX}				mAdc
(V_{CEX} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			—	—	0.2	
(V_{CEX} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)			—	—	2	
Collector Cutoff Current		I_{CER}				mAdc
(V_{CE} = Rated V_{CEX}, R_{BE} = 10 Ω)	T_C = 25°C		—	—	0.5	
	T_C = 125°C		—	—	3	
Emitter Cutoff Current		I_{EBO}	—	—	0.1	mAdc
(V_{EB} = 5 Vdc, I_C = 0)						
Emitter–Base Breakdown Voltage		$V_{(BR)EBO}$	7	—	—	Vdc
(I_E = 50 mA – I_C = 0)						
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				
(I_C = 10 Adc, V_{CE} = 5 Vdc)	BUV48		8	—	—	
(I_C = 8 Adc, V_{CE} = 5 Vdc)	BUV48A		8	—	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 2 Adc)			—	—	1.5	
(I_C = 15 Adc, I_B = 3 Adc)	BUV48		—	—	5	
(I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)			—	—	2	
(I_C = 8 Adc, I_B = 1.6 Adc)			—	—	1.5	
(I_C = 12 Adc, I_B = 2.4 Adc)	BUV48A		—	—	5	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)			—	—	2	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 2 Adc)	BUV48		—	—	1.6	
(I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)			—	—	1.6	
(I_C = 8 Adc, I_B = 1.6 Adc)	BUV48A		—	—	1.6	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)			—	—	1.6	
DYNAMIC CHARACTERISTICS						
Output Capacitance		C_{ob}	—	—	350	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)						

SWITCHING CHARACTERISTICS

Resistive Load (Table 1)

Delay Time	I_C = 10 A, I_B, = 2 A	BUV48	t_d	—	0.1	0.2	μs
Rise Time	I_C = 8 A, I_B, = 1.6 A	BUV48A	t_r	—	0.4	0.7	
Storage Time	Duty Cycle ≤ 2%, $V_{BE(off)}$ = 5 V		t_s	—	1.3	2	
Fall Time	T_p = 30 μs, V_{CC} = 300 V		t_f	—	0.2	0.4	

Inductive Load, Clamped (Table 1)

Storage Time	I_C = 10 A, I_{B1} = 2 A	BUV48	(T_C = 25°C)	t_{sv}	—	1.3	—	μs
Fall Time				t_{fi}	—	0.06	—	
Storage Time	I_C = 8 A, I_{B1} = 1.6 A	BUV48A	(T_C = 100°C)	t_{sv}	—	1.5	2.5	
Crossover Time				t_c	—	0.3	0.6	
Fall Time				t_{fi}	—	0.17	0.35	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

Vcl = 300 V, $V_{BE(off)}$ = 5 V, Lc = 180 μH

DC CHARACTERISTICS

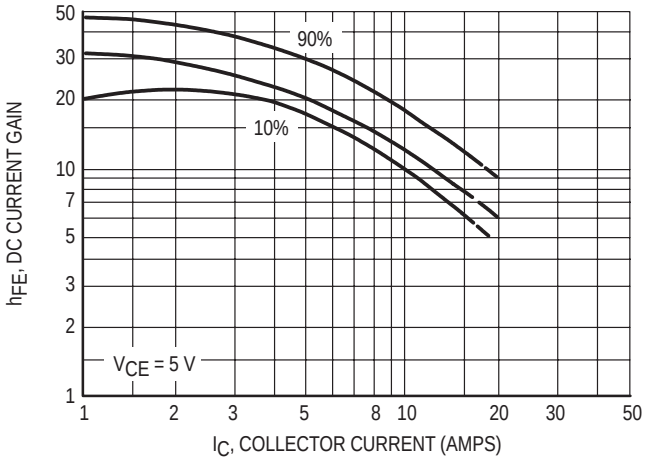


Figure 1. DC Current Gain

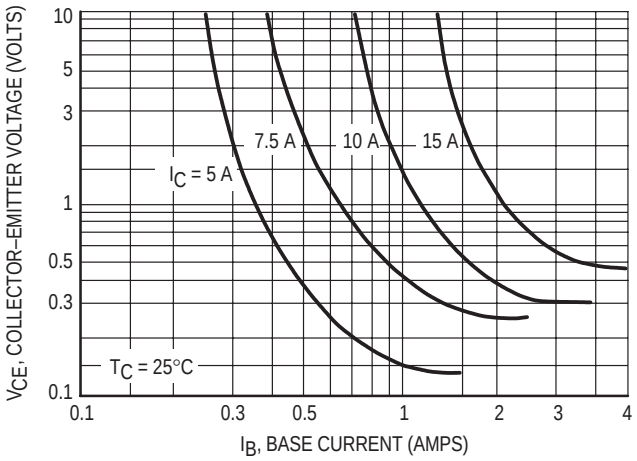


Figure 2. Collector Saturation Region

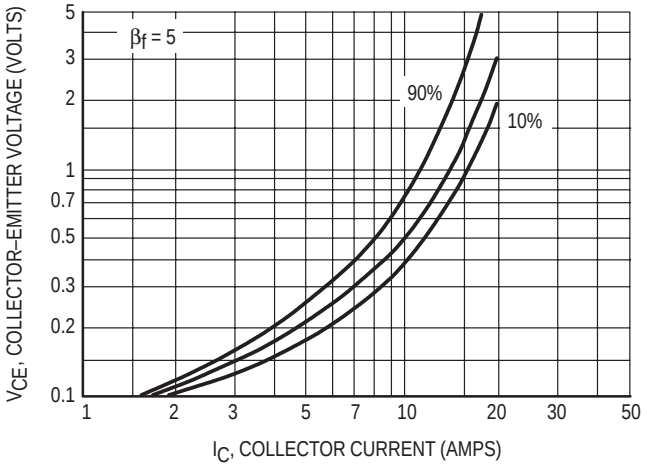


Figure 3. Collector–Emitter Saturation Voltage

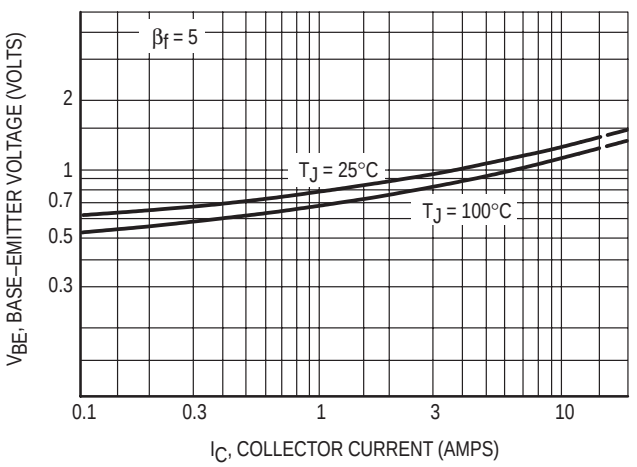


Figure 4. Base–Emitter Voltage

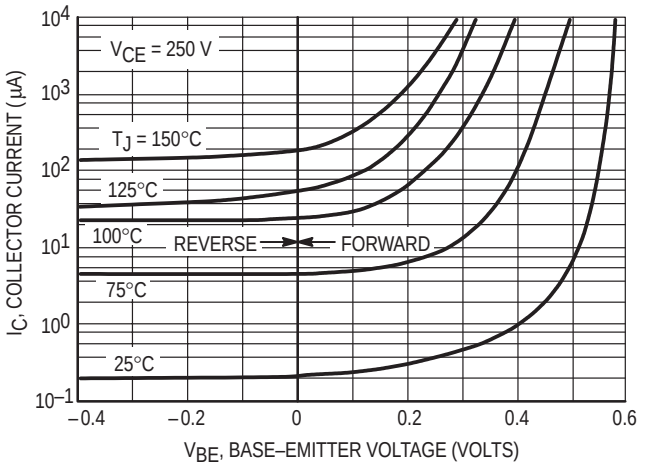


Figure 5. Collector Cutoff Region

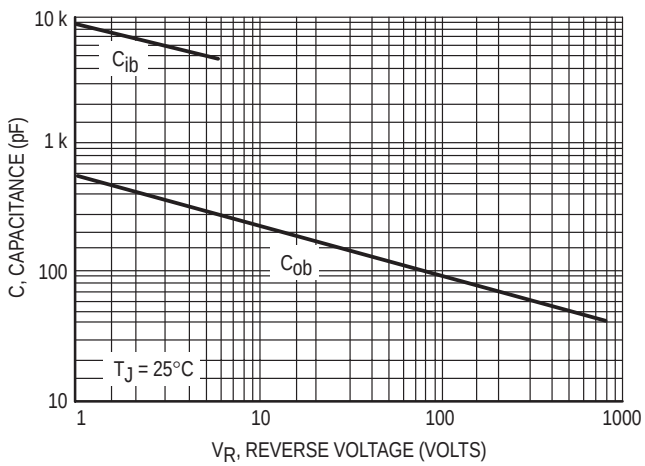


Figure 6. Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20, 1, 0, 2 PW Varied to Attain I_C = 200 mA	33 2 W, D1, 22 µF, 2N6438, +10 V, 160, D3, MR854, 220, 100, MM3735, 680 pF, 22, I_{b1} ADJUST, D1 D2 D3 D4 1N4934, 0.1 µF, I_{b2} ADJUST, dT_b ADJUST, PULSES δ = 3%, 2N3763, 680 pF, 22, dT, MR854, 160, 33 2 W, D3, 0.22 µF, 2N6339, V_{CC}	**TURN–ON TIME** I_{B1} I_{B1} adjusted to obtain the forced h_{FE} desired **TURN–OFF TIME** Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 25 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 300 V R_B ADJUSTED TO ATTAIN DESIRED I_{B1}	V_{CC} = 300 V R_L = 83 Ω Pulse Width = 10 µs
TEST CIRCUITS	**INDUCTIVE TEST CIRCUIT** TUT, 1, INPUT, 1N4937 OR EQUIVALENT, R_{coil}, L_{coil}, SEE ABOVE FOR DETAILED CONDITIONS, V_{clamp}, V_{CC}, 2, RS = 0.1 Ω **OUTPUT WAVEFORMS** I_C, $I_{C(pk)}$, t_f Clamped, t, t_1, t_f, V_{CE}, V_{CE} or V_{clamp}, TIME, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	**RESISTIVE TEST CIRCUIT** TUT, 1, 2, R_L, V_{CC}

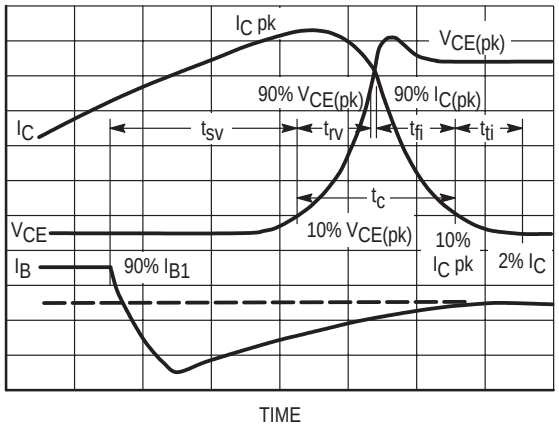


Figure 7. Inductive Switching Measurements

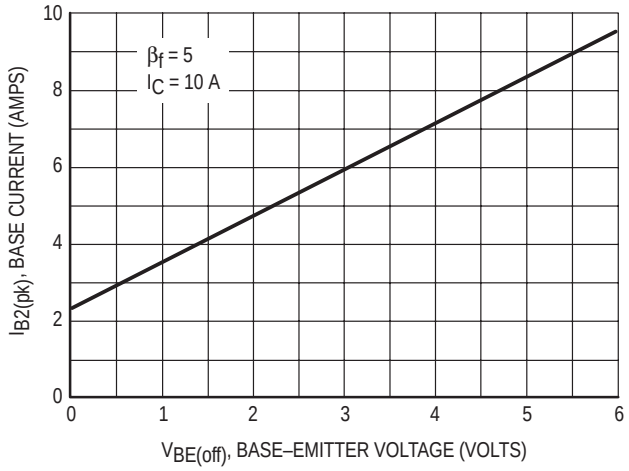


Figure 8. Peak–Reverse Current

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2\ V_{CC} I_C(t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

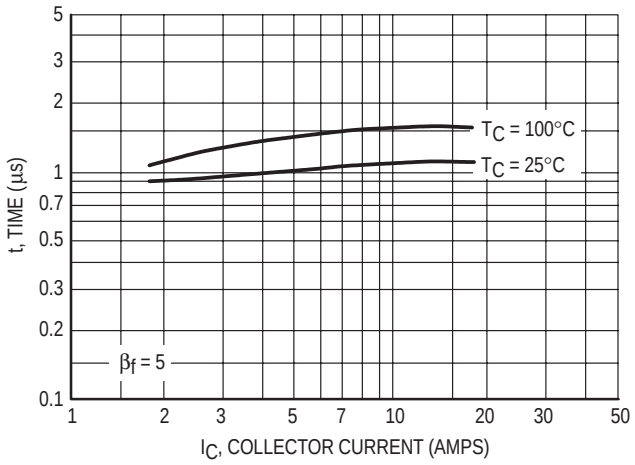


Figure 9. Storage Time, t_{sv}

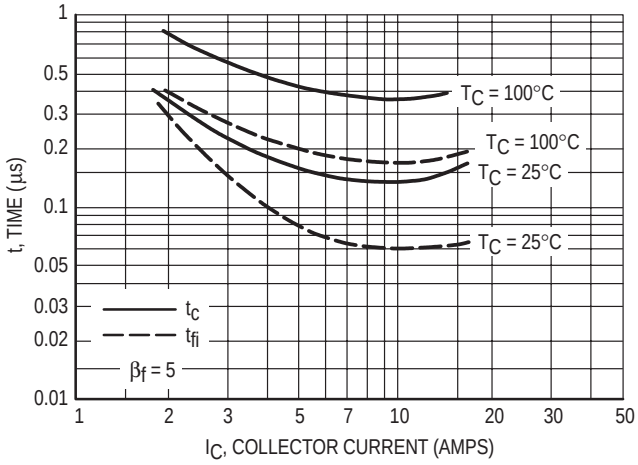


Figure 10. Crossover and Fall Times

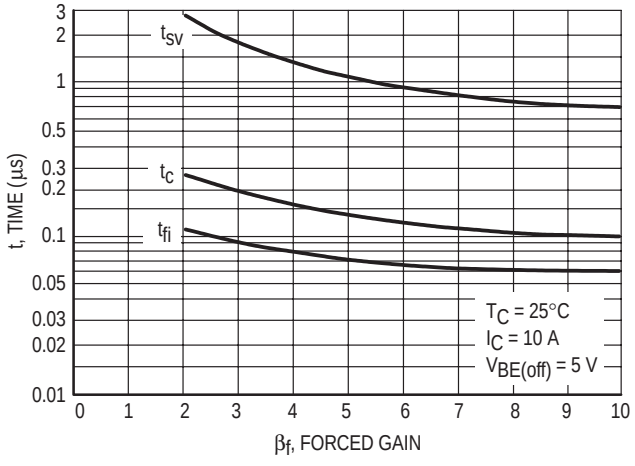


Figure 11a. Turn–Off Times versus Forced Gain

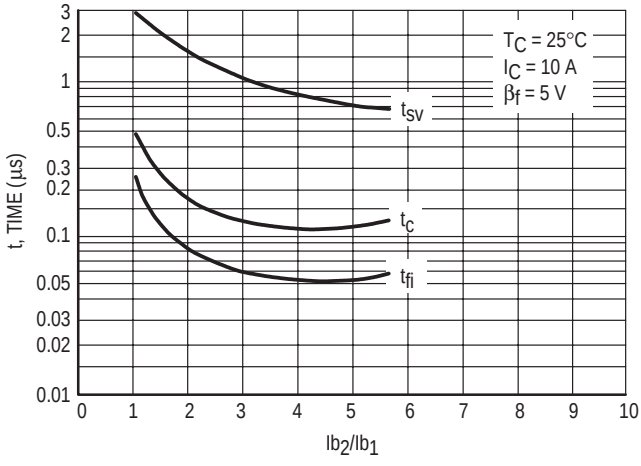


Figure 11b. Turn–Off Times versus Ib_2/Ib_1

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

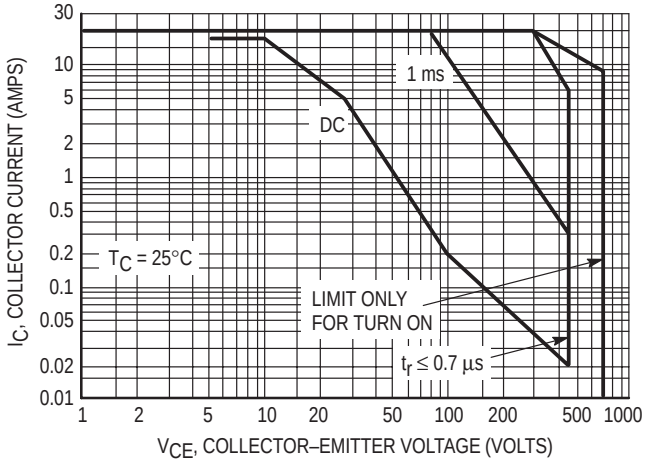


Figure 12. Forward Bias Safe Operating Area

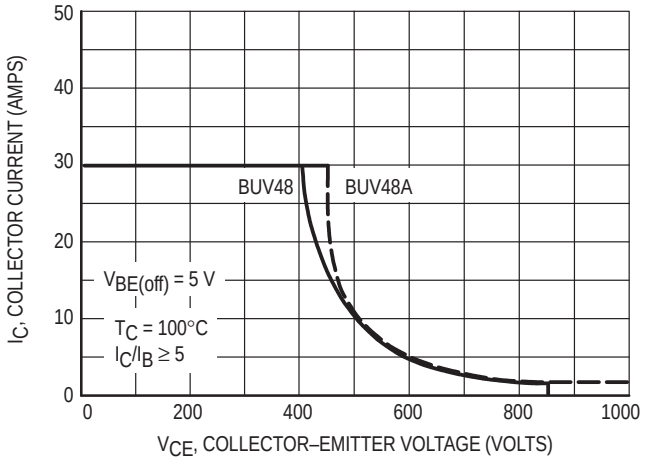


FIgure 13. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \leq$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

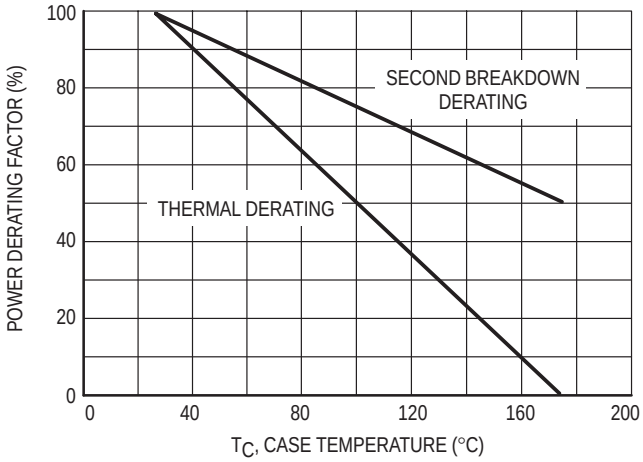


Figure 14. Power Derating

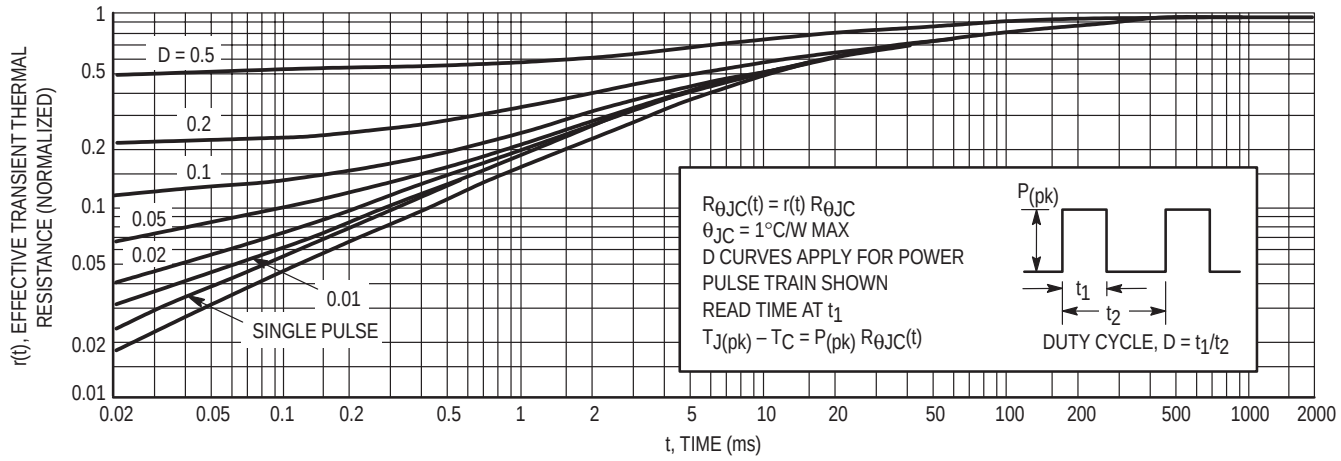


Figure 15. Thermal Response

OVERLOAD CHARACTERISTICS

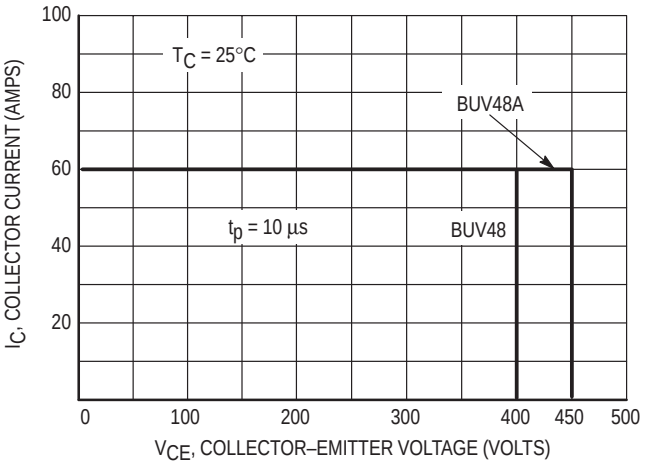


Figure 16. Rated Overload Safe Operating Area (OLSOA)

OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

Maximum allowable collector–emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common–base circuit (Figure 18) which allows precise definition of collector–emitter voltage and collector current. This is the same circuit that is used to measure forward–bias safe operating area.

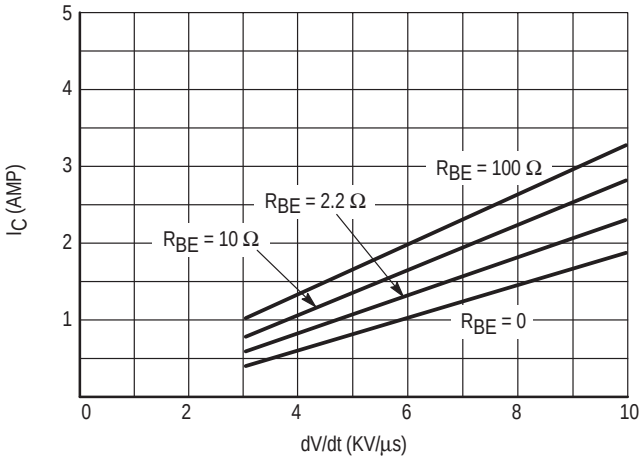


Figure 17. I_C = f(dV/dt)

Notes:
- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

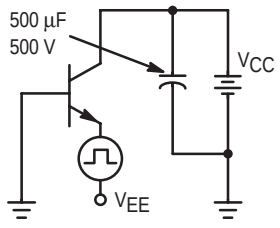


Figure 18. Overload SOA Test Circuit

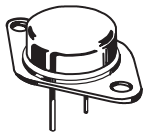
BUX41

SWITCHMODE Series
NPN Silicon Power Transistor

15 AMPERES
NPN SILICON
POWER
METAL TRANSISTOR
200 VOLTS
120 WATTS

. . . designed for high speed, high current, high power applications.

- Very fast switching times:
  T_F max. = 0.4 μs at I_C = 8 A



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	200	Vdc
Collector–Base Voltage	V_{CBO}	250	Vdc
Emitter–Base Voltage	V_{EBO}	7	Vdc
Collector–Emitter Voltage (V_{BE} = –2.5 V)	V_{CEX}	250	Vdc
Collector–Emitter Voltage (R_{BE} = 100 Ω)	V_{CER}	240	Vdc
Collector–Current — Continuous — Peak (pw ≤ 10 ms)	I_C I_{CM}	15 20	Adc Apk
Base–Current continuous	I_B	3	Adc
Total Power Dissipation @ T_C = 25°C	P_D	120	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.46	°C/W

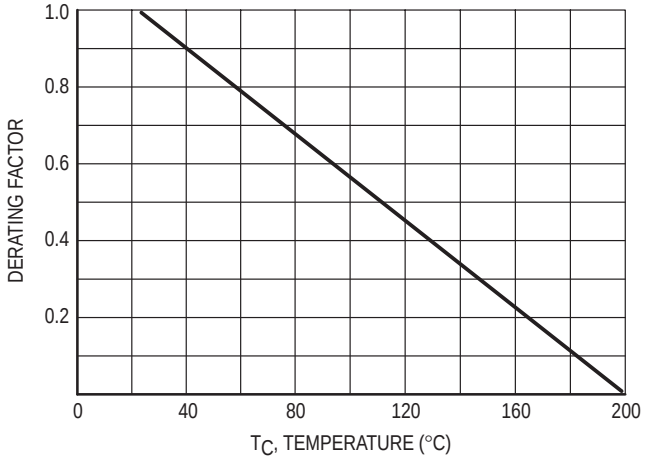


Figure 1. Power Derating

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS[1]				
Collector–Emitter Sustaining Voltage (I_C = 200 mA, I_B = 0, L = 25 mH)	$V_{CEO(sus)}$	200		Vdc
Collector Cutoff Current at Reverse Bias: (V_{CE} = 250 V, V_{BE} = –1.5 V) (V_{CE} = 250 V, V_{BE} = –1.5 V, T_C = 125°C)	I_{CEX}		1.0 5.0	mAdc
Collector–Emitter Cutoff Current (V_{CE} = 160 V)	I_{CEO}		1.0	mAdc
Emitter–Base Reverse Voltage (I_E = 50 mA)	V_{EBO}	7		V
Emitter–Cutoff Current (V_{EB} = 5 V)	I_{EBO}		1.0	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with base forward biased (V_{CE} = 30 V, t = 1 s) (V_{CE} = 135 V, t = 1 s)	$I_{S/b}$	4.0 0.15		Adc
ON CHARACTERISTICS[1]				
DC Current Gain (I_C = 5 A, V_{CE} = 4 V) (I_C = 8 A. V_{CE} = 4 V)	h_{FE}	15 8	45	
Collector–Emitter Saturation Voltage (I_C = 5 A, I_B = 0.5 A) (I_C = 8 A, I_B = 1 A)	$V_{CE(sat)}$		1.2 1.6	Vdc
Base–Emitter Saturation Voltage (I_C = 8 A, I_B = 1 A)	$V_{BE(sat)}$		2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (V_{CE} = 15 V, I_C = 1 A, f = 4 MHz)	f_T	8.0		MHz
SWITCHING CHARACTERISTICS (Resistive Load)				
Turn–on Time	(I_C = 8 A, I_{B1} = I_{B2} = 1 A, V_{CC} = 150 V, R_C = 18.75 Ω)	t_{on}	0.6	μs
Storage Time		t_s	1.5	
Fall Time		t_f	0.4	

[1] Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

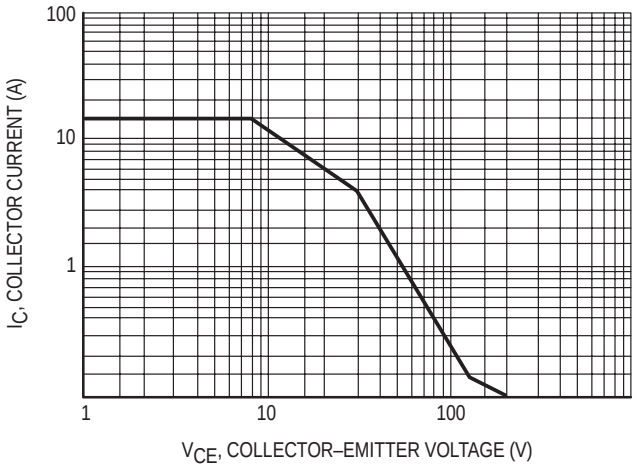


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_C = 25°C$, $T_{J(pk)}$ is variable depending on power level. Second breakdown limitations do not derate the same as thermal limitations.

At high case temperatures, thermal limitations will reduce the power that can handled to values less than the limitations imposed by second breakdown.

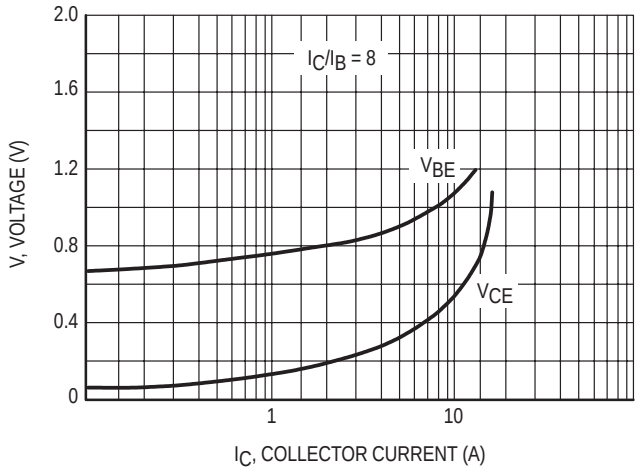


Figure 3. "On" Voltages

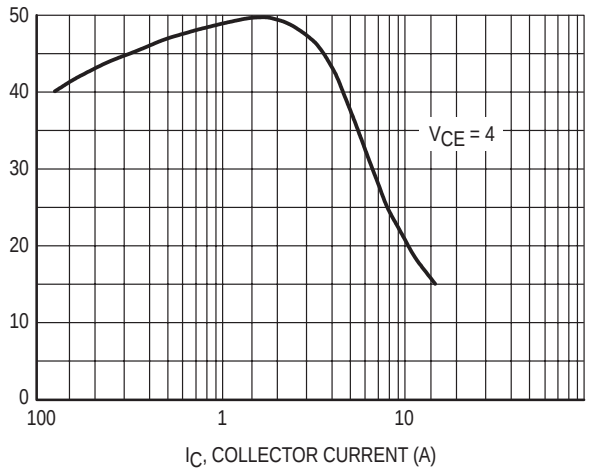


Figure 4. DC Current Gain

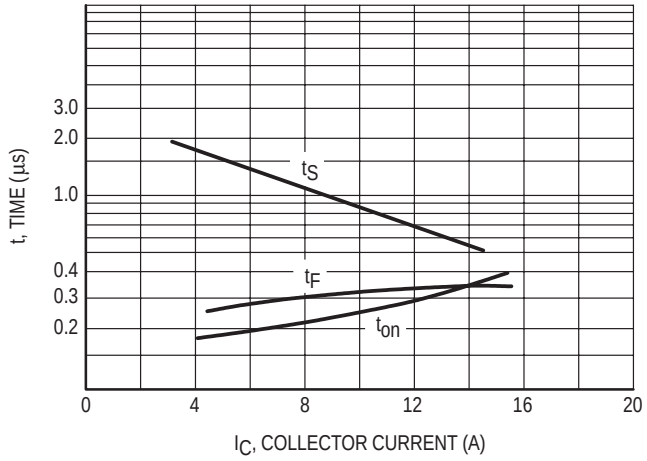
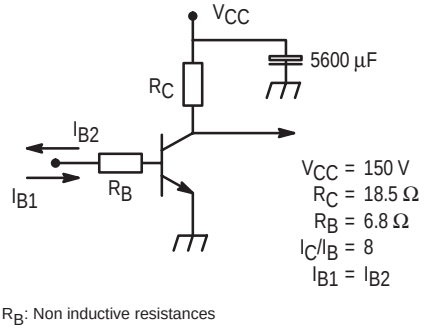


Figure 5. Resistive Switching Performance



$R_C - R_B$: Non inductive resistances

Figure 6. Switching Times Test Circuit

BUX48
BUX48A

SWITCHMODE II Series
NPN Silicon Power Transistors

The BUX 48/BUX 48A transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated SWITCHMODE applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

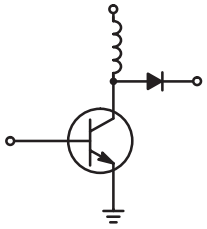
Fast Turn–Off Times

60 ns Inductive Fall Time — 25°C (Typ)
120 ns Inductive Crossover Time — 25°C (Typ)

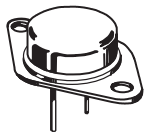
Operating Temperature Range –65 to +200°C

100°C Performance Specified for:

Reverse–Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltage
Leakage Currents (125°C)



15 AMPERES
NPN SILICON
POWER TRANSISTORS
400 AND 450 VOLTS
$V_{(BR)CEO}$
850 – 1000 VOLTS
$V_{(BR)CEX}$
175 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	BUX48	BUX48A	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector–Emitter Voltage (V_{BE} = – 1.5 V)	VCEX	850	1000	Vdc
Emitter Base Voltage	V_{EB}	7		Vdc
Collector Current — Continuous — Peak (1) — Overload	I_C I_{CM} I_{OI}	15 30 60		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	5 20		Adc
Total Power Dissipation — T_C = 25°C — T_C = 100°C Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector–Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$				Vdc
(I_C = 200 mA, I_B = 0) L = 25 mH	BUX48		400	—	—	
	BUX48A		450	—	—	
Collector Cutoff Current		I_{CEX}				mAdc
(V_{CEX} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			—	—	0.2	
(V_{CEX} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)			—	—	2	
Collector Cutoff Current		I_{CER}				mAdc
(V_{CE} = Rated V_{CEX}, R_{BE} = 10 Ω)	T_C = 25°C		—	—	0.5	
	T_C = 125°C		—	—	3	
Emitter Cutoff Current		I_{EBO}	—	—	0.1	mAdc
(V_{EB} = 5 Vdc, I_C = 0)						
Emitter–Base Breakdown Voltage		$V_{(BR)EBO}$	7	—	—	Vdc
(I_E = 50 mA – I_C = 0)						
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 13			
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				
(I_C = 10 Adc, V_{CE} = 5 Vdc)	BUX48		8	—	—	
(I_C = 8 Adc, V_{CE} = 5 Vdc)	BUX48A		8	—	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 2 Adc)			—	—	1.5	
(I_C = 15 Adc, I_B = 3 Adc)	BUX48		—	—	5	
(I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)			—	—	2	
(I_C = 8 Adc, I_B = 1.6 Adc)			—	—	1.5	
(I_C = 12 Adc, I_B = 2.4 Adc)	BUX48A		—	—	5	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)			—	—	2	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 2 Adc)	BUX48		—	—	1.6	
(I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)			—	—	1.6	
(I_C = 8 Adc, I_B = 1.6 Adc)			—	—	1.6	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)	BUX48A		—	—	1.6	
DYNAMIC CHARACTERISTICS						
Output Capacitance		C_{ob}	—	—	350	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)						
SWITCHING CHARACTERISTICS Resistive Load (Table 1)						
Delay Time	I_C = 10 A, I_B = 2 A	BUX48	t_d	—	0.1	0.2	µs
Rise Time	I_C = 8 A, I_B = 1.6 A	BUX48A	t_r	—	0.4	0.7	
Storage Time	Duty Cycle = 2%, $V_{BE(off)}$ = 5 V		t_s	—	1.3	2	
Fall Time	T_p = 30 µs, V_{CC} = 300 V		t_f	—	0.2	0.4	
Inductive Load, Clamped (Table 1)							
Storage Time	I_C = 10 A	BUX48 (T_C = 25°C)	t_{sv}	—	1.3	—	µs
Fall Time	I_{B1} = 2 A		t_{fi}	—	0.06	—	
Storage Time	I_C = 8 A	BUX48A (T_C = 100°C)	t_{sv}	—	1.5	2.5	
Crossover Time	I_{B1} = 1.6 A		t_c	—	0.3	0.6	
Fall Time			t_{fi}	—	0.17	0.35	

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤ 2%.
Vcl = 300 V, $V_{BE(off)}$ = 5 V, Lc = 180µH

DC CHARACTERISTICS

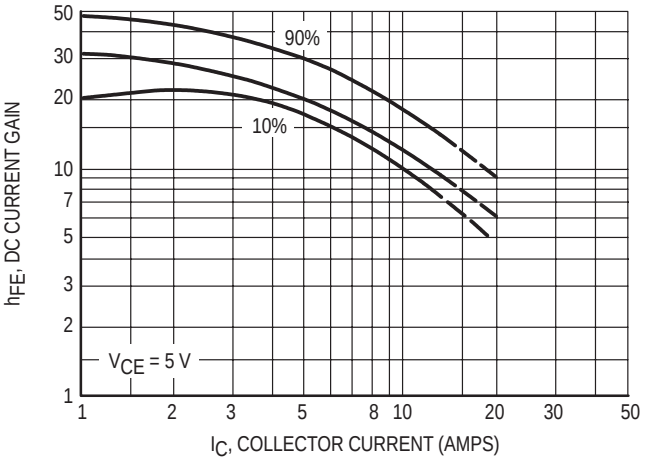


Figure 1. DC Current Gain

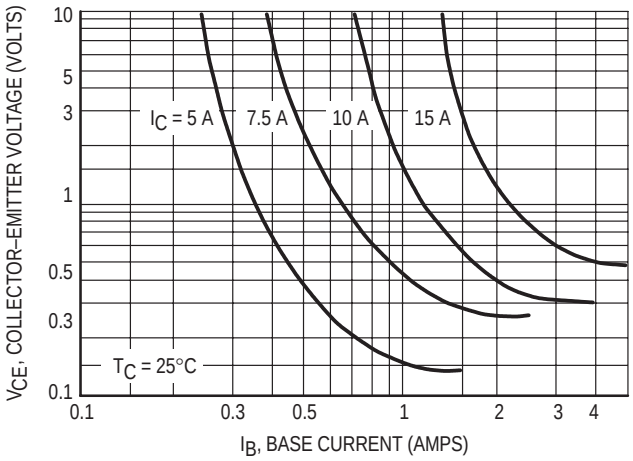


Figure 2. Collector Saturation Region

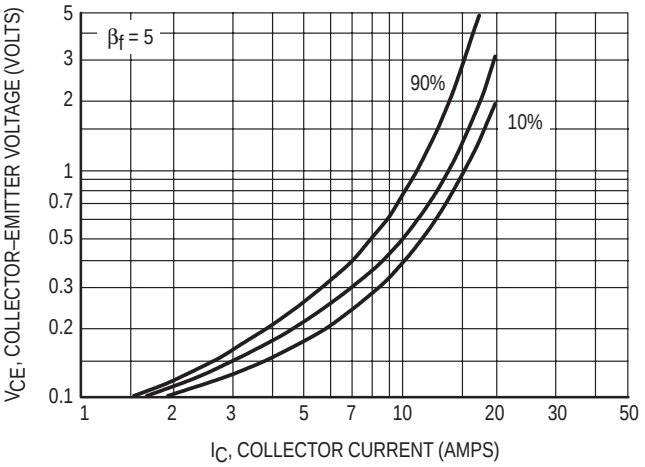


Figure 3. Collector–Emitter Saturation Voltage

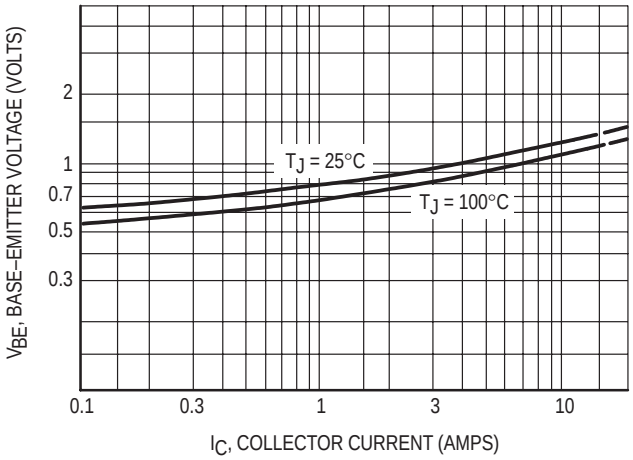


Figure 4. Base–Emitter Voltage

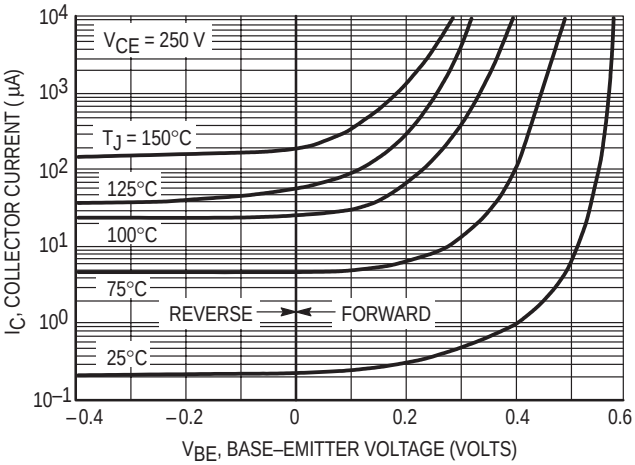


Figure 5. Collector Cutoff Region

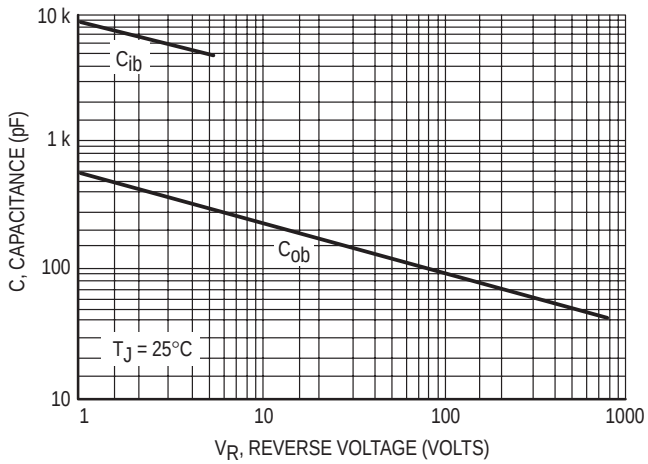


Figure 6. Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20, 0, 1, 2 PW Varied to Attain I_C = 200 mA	33 2 W, D1, 22 µF, 2N6438, +10 V, 160, D3, MR854, 220, 100, MM3735, 680 pF, 22, I_{b1} ADJUST, D1 D2 D3 D4 1N4934, 0.1 µF, I_{b2} ADJUST, dT_b ADJUST, PULSES δ = 3%, 680 pF, 2N3763, 680 pF, 22, D4, MR854, 100, 160, 33 2 W, D3, 0.22 µF, 2N6339, V_{CC}	**TURN–ON TIME** I_{B1} adjusted to obtain the forced h_{FE} desired **TURN–OFF TIME** Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 25 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 300 V R_B ADJUSTED TO ATTAIN DESIRED I_{B1}	V_{CC} = 300 V R_L = 83 Ω Pulse Width = 10 µs
TEST CIRCUITS	**INDUCTIVE TEST CIRCUIT** TUT, 1, INPUT, 1N4937 OR EQUIVALENT, R_{coil}, L_{coil}, SEE ABOVE FOR DETAILED CONDITIONS, V_{clamp}, V_{CC}, 2, RS = 0.1 Ω **OUTPUT WAVEFORMS** I_C, $I_{C(pk)}$, t_f Clamped, t, t_1, t_f, V_{CE}, V_{CE} or V_{clamp}, TIME, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	**RESISTIVE TEST CIRCUIT** TUT, 1, 2, R_L, V_{CC}

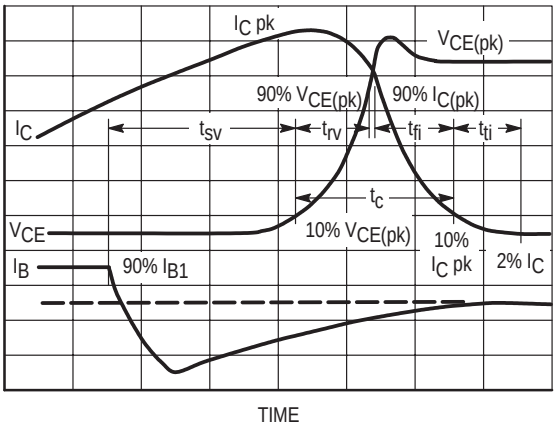


Figure 7. Inductive Switching Measurements

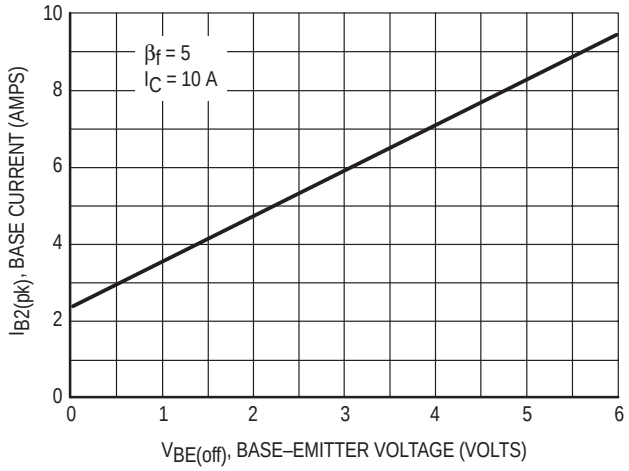


Figure 8. Peak–Reverse Current

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

INDUCTIVE SWITCHING

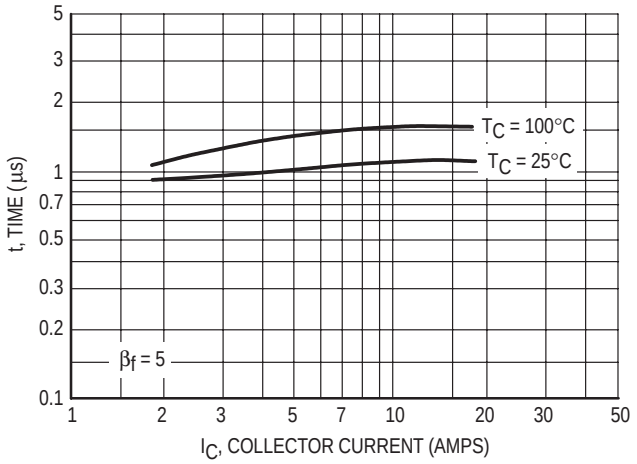


Figure 9. Storage Time, t_{sv}

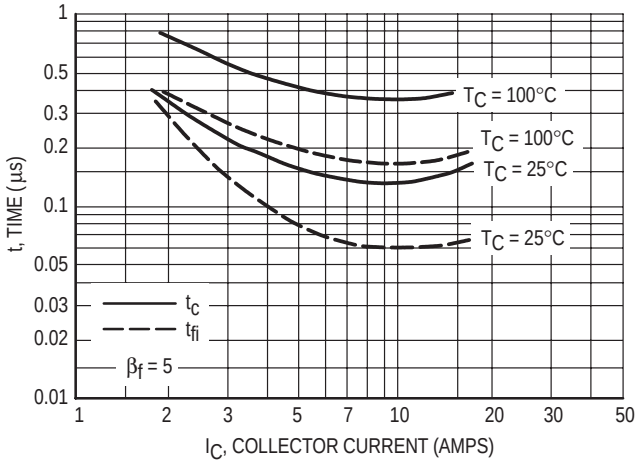


Figure 10. Crossover and Fall Times

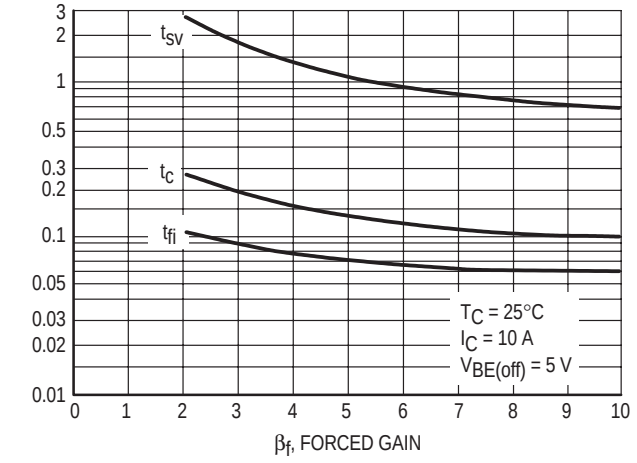


Figure 11a. Turn–Off Times versus Forced Gain

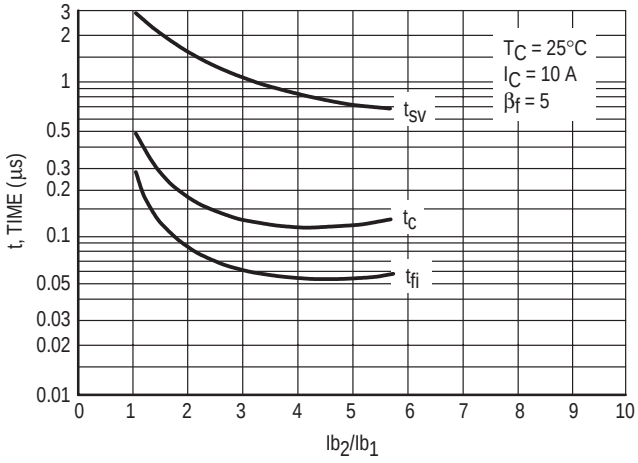


Figure 11b. Turn–Off Times versus Ib_2/Ib_1

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

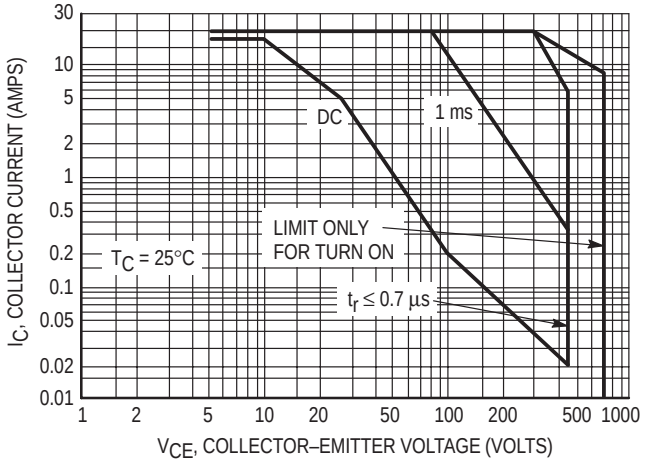


Figure 12. Forward Bias Safe Operating Area

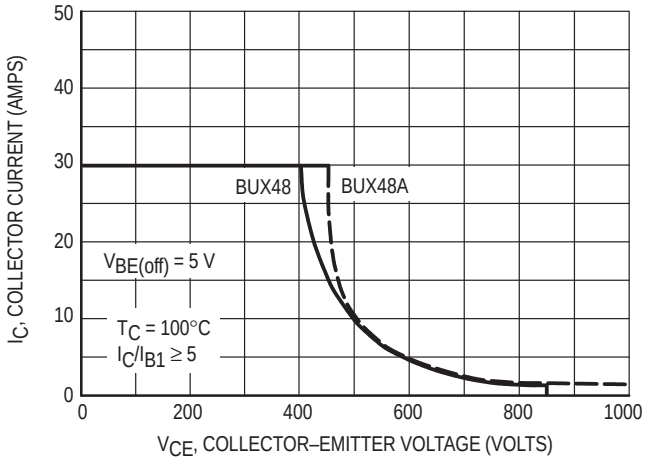


FIgure 13. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives RBSOA characteristics.

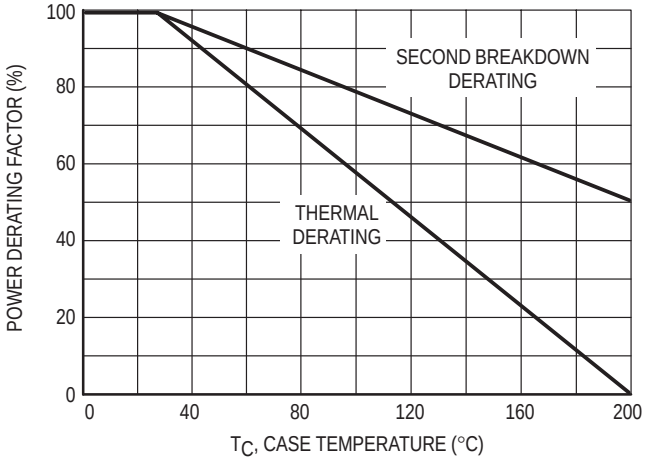


Figure 14. Power Derating

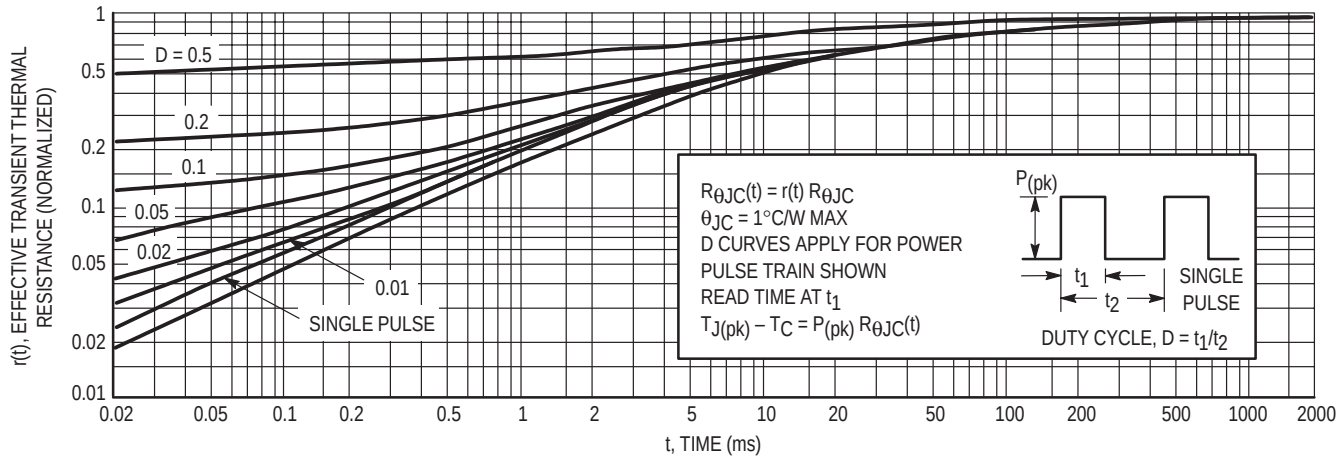


Figure 15. Thermal Response

OVERLOAD CHARACTERISTICS

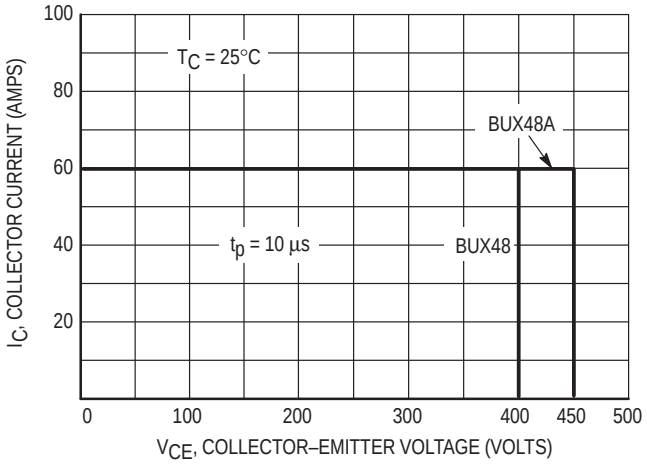


Figure 16. Rated Overload Safe Operating Area (OLSOA)

OLSOA

OLSOA applies when maximum collector current is limited and known. A good example is a circuit where an inductor is inserted between the transistor and the bus, which limits the rate of rise of collector current to a known value. If the transistor is then turned off within a specified amount of time, the magnitude of collector current is also known.

Maximum allowable collector–emitter voltage versus collector current is plotted for several pulse widths. (Pulse width is defined as the time lag between the fault condition and the removal of base drive.) Storage time of the transistor has been factored into the curve. Therefore, with bus voltage and maximum collector current known, Figure 16 defines the maximum time which can be allowed for fault detection and shutdown of base drive.

OLSOA is measured in a common–base circuit (Figure 18) which allows precise definition of collector–emitter voltage and collector current. This is the same circuit that is used to measure forward–bias safe operating area.

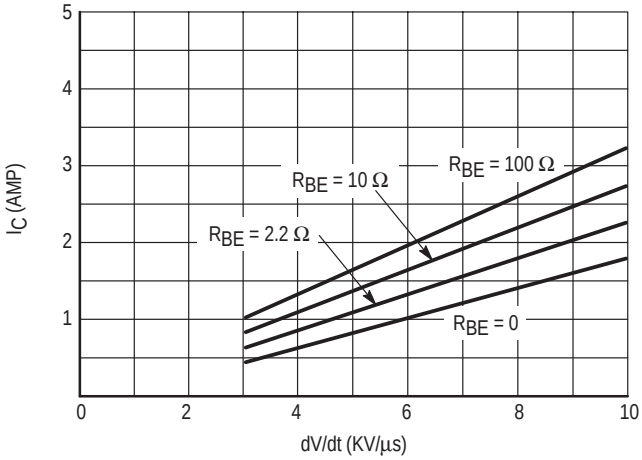


Figure 17. I_C = f(dV/dt)

Notes:
- $V_{CE} = V_{CC} + V_{BE}$
- Adjust pulsed current source for desired I_C, t_p

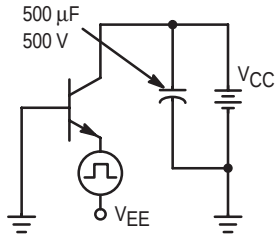


Figure 18. Overload SOA Test Circuit

BUX85

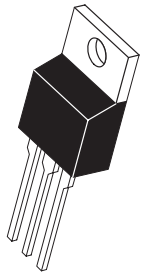
SWITCHMODE
NPN Silicon Power Transistors

2 AMPERES
POWER TRANSISTOR
NPN SILICON
450 VOLTS
50 WATTS

The BUX85 is designed for high voltage, high speed power switching applications like converters, inverters, switching regulators, motor control systems.

SPECIFICATIONS FEATURES:

- $V_{CEO(sus)}$ 450 V
- $V_{CES(sus)}$ 1000 V
- Fall time = 0.3 μs (typ) at I_C = 1.0 A
- $V_{CE(sat)}$ = 1.0 V (max) at I_C = 1.0 A, I_B = 0.2 A



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BUX84	BUX85	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	450	Vdc
Collector–Emitter Voltage	V_{CES}	800	1000	Vdc
Emitter Base Voltage	V_{EBO}	5		Vdc
Collector Current — Continuous — Peak (1)	 I_C I_{CM}	 2 3.0		Adc
Base Current — Continuous — Peak (1)	 I_B I_{BM}	 0.75 1.0		Adc
Reverse Base Current — Peak	I_{BM}	1		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 400		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purpose: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≦10%.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, (L = 25 mH) See fig. 1		$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current		I_{CES}				mAdc
(V_{CES} = Rated Value)			—	—	0.2	
(V_{CES} = Rated Value, T_C = 125°C)			—	—	1.5	
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)		I_{EBO}	—	—	1	mAdc
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 5 V)		h_{FE}	30	50	—	—
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 0.3 Adc, I_B = 30 mAdc)			—	—	0.8	
(I_C = 1 Adc, I_B = 200 mAdc)			—	—	1	
Base–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)		$V_{BE(sat)}$	—	—	1.1	Vdc
DYNAMIC CHARACTERISTICS						
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 1 0 Vdc, f = 1 MHz)		f_T	4	—	—	MHz
SWITCHING CHARACTERISTICS						
Turn–on Time	V_{CC} = 250 Vdc, I_C = 1 A I_{B1} = 0.2 A, I_{B2} = 0.4 A See fig. 2	t_{on}	—	0.3	0.5	µs
Storage Time		t_s	—	2	3.5	µs
Fall Time		t_f	—	0.3	—	µs
Fall Time	Same above cond. at T_C = 95°C	t_f	—	—	1.4	µs

(1) Pulse Test: PW = 300 µs, Duty Cycle ≦2%.

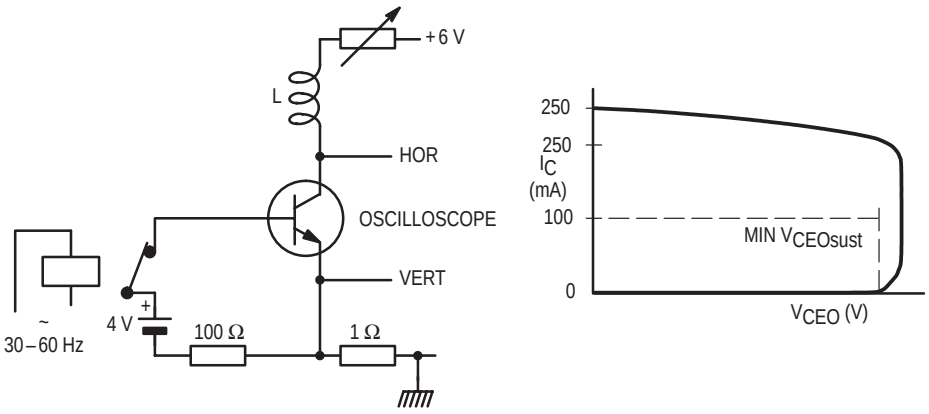


Figure 1. Test Circuit for $V_{CEOsust}$

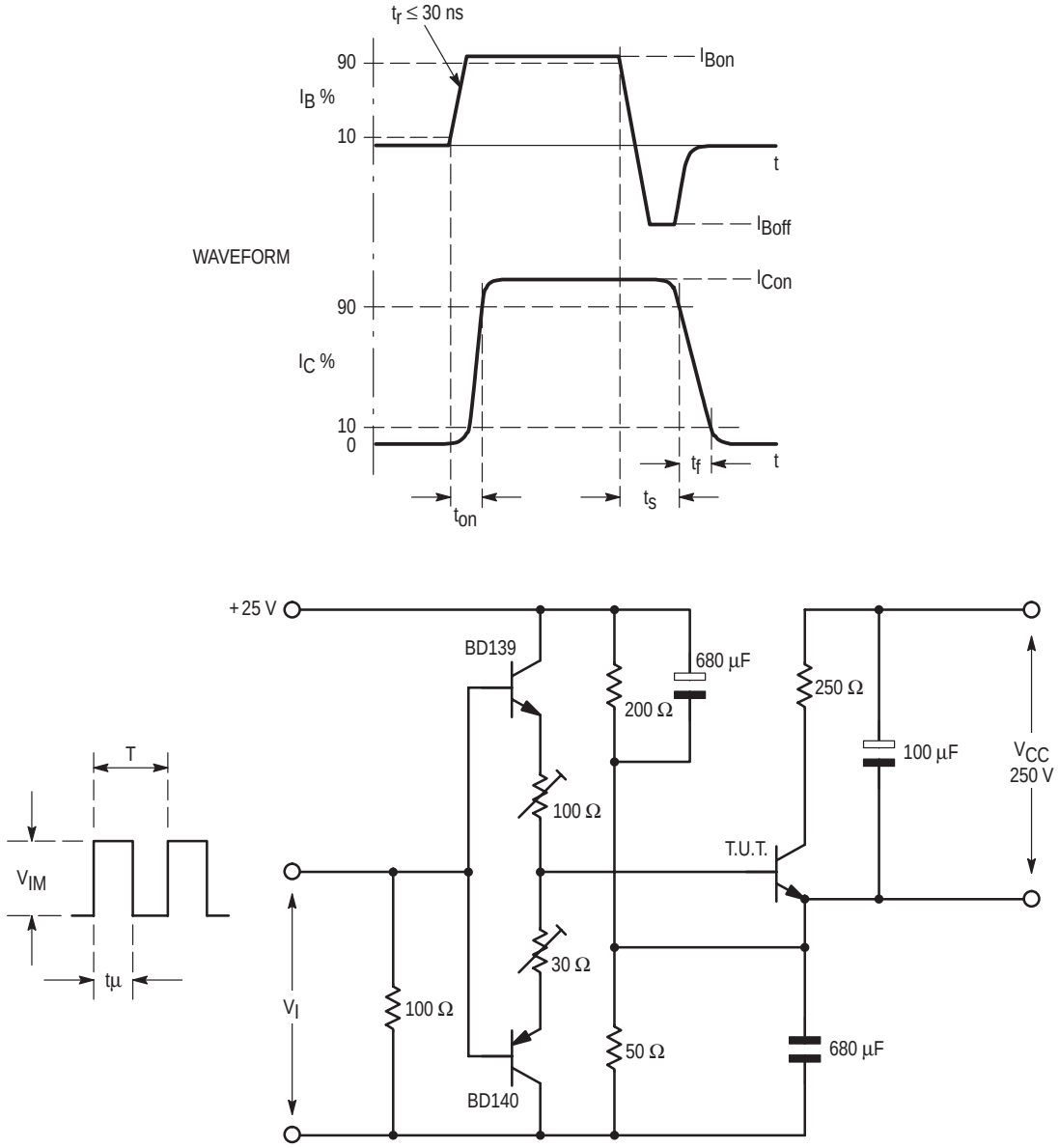


Figure 2. Switching Times/Test Circuit

Complementary Silicon Power Transistors

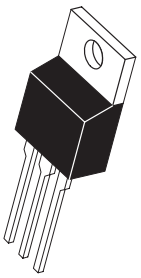
. . . for general purpose power amplification and switching such as output or driver stages in applications such as switching regulators, converters and power amplifiers.

- Low Collector–Emitter Saturation Voltage
  $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

NPN
D44H Series*
PNP
D45H Series*

*Motorola Preferred Device

10 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60, 80 VOLTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	D44H or D45H		Unit
		8	10, 11	
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Emitter Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous — Peak (1)	I_C	10 20		Adc
Total Power Dissipation @ T_C = 25°C @ T_A = 25°C	P_D	 50 1.67		Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
DC Current Gain (V_{CE} = 1.0 Vdc, I_C = 2.0 Adc)	D44H10 D45H10	h_{FE}	35	—	—
	D44H8,11 D44H8,11		60	—	
(V_{CE} = 1.0 Vdc, I_C = 4.0 Adc)	D44H10 D45H10		20	—	
	D44H8,11 D45H8,11		40	—	

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)		I_{CES}	—	—	10	μA
Emitter Cutoff Current (V_{EB} = 5.0 Vdc)		I_{EBO}	—	—	100	μA
ON CHARACTERISTICS						
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 8.0 Adc, I_B = 0.4 Adc)	D44H/D45H8,11		—	—	1.0	
(I_C = 8.0 Adc, I_B = 0.8 Adc)	D44H/D45H10		—	—	1.0	
Base–Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 0.8 Adc)		$V_{BE(sat)}$	—	—	1.5	Vdc
DYNAMIC CHARACTERISTICS						
Collector Capacitance		C_{cb}				pF
(V_{CB} = 10 Vdc, f_{test} = 1.0 MHz)	D44H Series		—	130	—	
	D45H Series		—	230	—	
Gain Bandwidth Product		f_T				MHz
(I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	D44H Series		—	50	—	
	D45H Series		—	40	—	
SWITCHING TIMES						
Delay and Rise Times		$t_d + t_r$				ns
(I_C = 5.0 Adc, I_{B1} = 0.5 Adc)	D44H Series		—	300	—	
	D45H Series		—	135	—	
Storage Time		t_s				ns
(I_C = 5.0 Adc, I_{B1} = I_{B2} = 0.5 Adc)	D44H Series		—	500	—	
	D45H Series		—	500	—	
Fall Time		t_f				ns
(I_C = 5.0 Adc, I_{B1} = 102 = 0.5 Adc)	D44H Series		—	140	—	
	D45H Series		—	100	—	

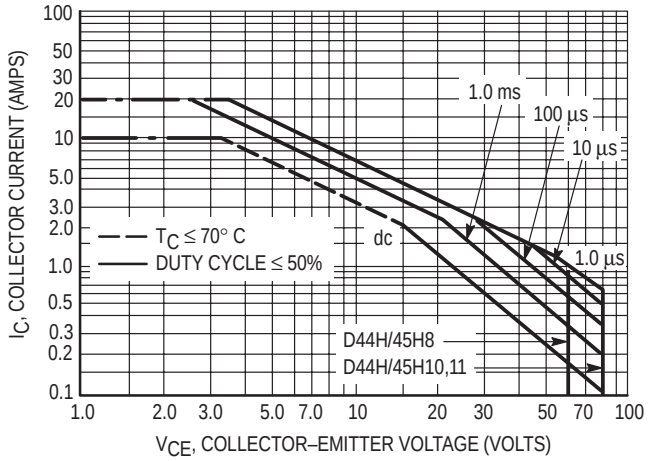


Figure 1. Maximum Rated Forward Bias Safe Operating Area

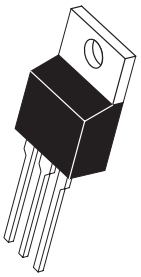
Complementary Silicon Power Transistors

NPN
D44VH
PNP
D45VH

These complementary silicon power transistors are designed for high–speed switching applications, such as switching regulators and high frequency inverters. The devices are also well–suited for drivers for high power switching circuits.

- Fast Switching — t_f = 90 ns (Max)
- Key Parameters Specified @ 100°C
- Low Collector–Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 V (Max) @ 8.0 A
- Complementary Pairs Simplify Circuit Designs

15 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80 VOLTS
83 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Emitter Voltage	V_{CEV}	100	Vdc
Emitter Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	83 0.67	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.

NOTE: All polarities are shown for NPN transistors. For PNP transistors, reverse polarities.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (1) (I_C = 25 mAdc, I_B = 0)		$V_{CEO(sus)}$	80	—	—	Vdc
Collector–Emitter Cutoff Current		I_{CEV}				μAdc
(V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 4.0 Vdc)			—	—	10	
(V_{CE} = Rated V_{CEV}, $V_{BE(off)}$ = 4.0 Vdc, T_C = 100°C)			—	—	100	
Emitter Base Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	—	10	μAdc
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				—
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)			35	—	—	
(I_C = 4.0 Adc, V_{CE} = 1.0 Vdc)			20	—	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 8.0 Adc, I_B = 0.4 Adc)	D44VH10		—	—	0.4	
(I_C = 8.0 Adc, I_B = 0.8 Adc)	D45VH10		—	—	1.0	
(I_C = 15 Adc, I_B = 3.0 Adc, T_C = 100°C)	D44VH10		—	—	0.8	
	D45VH10		—	—	1.5	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 8.0 Adc, I_B = 0.4 Adc)	D44VH10		—	—	1.2	
(I_C = 8.0 Adc, I_B = 0.8 Adc)	D45VH10		—	—	1.0	
(I_C = 8.0 Adc, I_B = 0.4 Adc, T_C = 100°C)	D44VH10		—	—	1.1	
(I_C = 8.0 Adc, I_B = 0.8 Adc, T_C = 100°C)	D45VH10		—	—	1.5	
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 10 Vdc, f = 20 MHz)		f_T	—	50	—	MHz
Output Capacitance		C_{ob}				pF
(V_{CB} = 10 Vdc, I_C = 0, f_{test} = 1.0 MHz)	D44VH10		—	120	—	
	D45VH10		—	275	—	
SWITCHING CHARACTERISTICS						
Delay Time	(V_{CC} = 20 Vdc, I_C = 8.0 Adc, I_{B1} = I_{B2} = 0.8 Adc)	t_d	—	—	50	ns
Rise Time		t_r	—	—	250	
Storage Time		t_s	—	—	700	
Fall Time		t_f	—	—	90	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

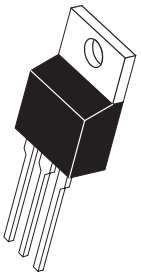
PNP
D45C

Complementary Silicon Power Transistor

. . . for general purpose driver or medium power output stages in CW or switching applications.

- Low Collector–Emitter Saturation Voltage — 0.5 V (Max)
- High f_t for Good Frequency Response
- Low Leakage Current

4.0 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80 VOLTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Emitter Voltage	VCES	90	Vdc
Emitter Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous Peak (1)	I_C	4.0 6.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_A = 25°C	P_D	30 1.67	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Width ≤ 6.0 ms, Duty Cycle ≤ 50%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
DC Current Gain (V_{CE} = 1.0 Vdc, I_C = 0.2 Adc) (V_{CE} = 1.0 Vdc, I_C = 1.0 Adc) (V_{CE} = 1.0 Vdc, I_C = 2.0 Adc)	h_{FE}	 40 20 20	 120 — —	—

(REPLACES D44C)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{BE} = 0)	I_{CES}	—	—	0.1	μA
Emitter Cutoff Current (V_{EB} = 5.0 Vdc)	I_{EBO}	—	—	10	μA
ON CHARACTERISTICS					
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 50 mAdc)	$V_{CE(sat)}$	—	0.135	0.5	Vdc
Base–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 100 mAdc)	$V_{BE(sat)}$	—	0.85	1.3	Vdc
DYNAMIC CHARACTERISTICS					
Collector Capacitance (V_{CB} = 10 Vdc, f = 1.0 MHz)	C_{cb}	—	125	—	pF
Gain Bandwidth Product (I_C = 20 mA, V_{CE} = 4.0 Vdc, f = 20 MHz)	f_T	—	40	—	MHz
SWITCHING TIMES					
Delay and Rise Times (I_C = 1.0 Adc, I_{B1} = 0.1 Adc)	$t_d + t_r$	—	50	75	ns
Storage Time (I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)	t_s	—	350	550	ns
Fall Time (I_C = 1.0 Adc, I_{B1} = I_{B2} = 0.1 Adc)	t_f	—	50	75	ns

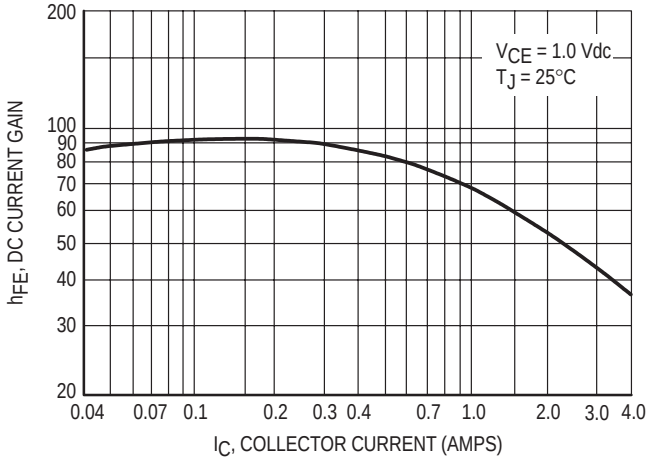


Figure 1. Typical DC Current Gain

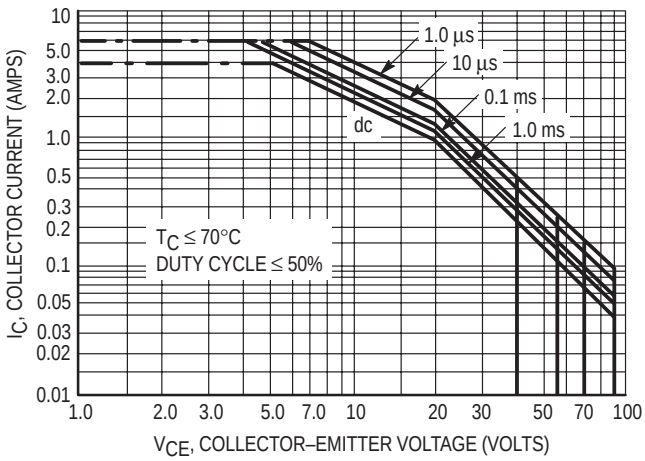


Figure 2. Maximum Rated Forward Bias Safe Operating Area

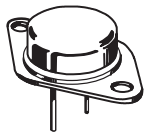
MJ410

High Voltage NPN Silicon Transistors

5 AMPERE
POWER TRANSISTOR
NPN SILICON
200 VOLTS
100 WATTS

. . . designed for medium to high voltage inverters, converters, regulators and switching circuits.

- High Collector–Emitter Voltage — V_{CEO} = 200 Volts
- DC Current Gain Specified @ 1.0 and 2.5 Adc
- Low Collector–Emitter Saturation Voltage — $V_{CE(sat)}$ = 0.8 Vdc @ I_C = 1.0 Adc



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	200	Vdc
Collector–Base Voltage	V_{CB}	200	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C	5.0 10	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation @ T_C = 75°C Derate above 75°C	P_D	100 1.33	Watts W/°C
Operating Junction Temperature Range	T_J	–65 to +150	°C
Storage Temperature Range	T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.75	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	200	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	—	0.25	mAdc
Collector Cutoff Current (V_{CB} = 200 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	I_{CEX}	—	0.5	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	 30 10	 90 —	—
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	0.8	Vdc
Base–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)	$V_{BE(sat)}$	—	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	—	MHz

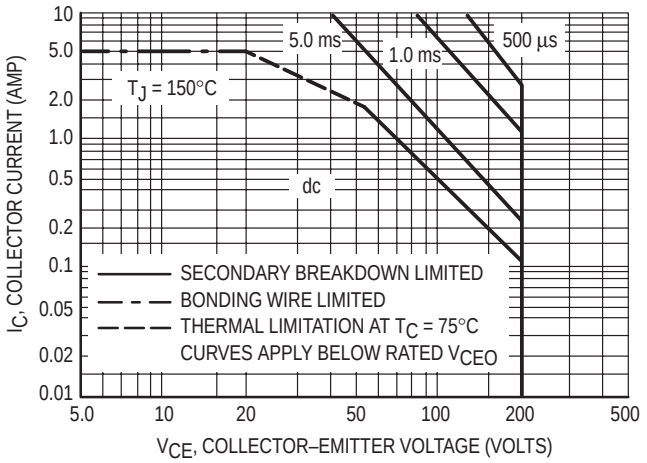


Figure 1. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values than the limitations imposed by second breakdown.

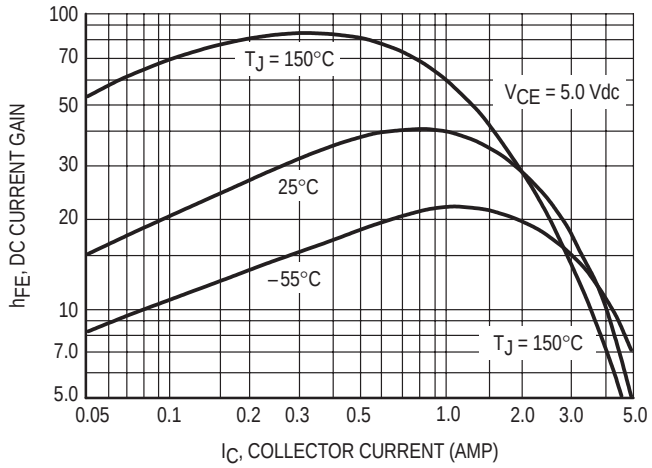


Figure 2. DC Current Gain

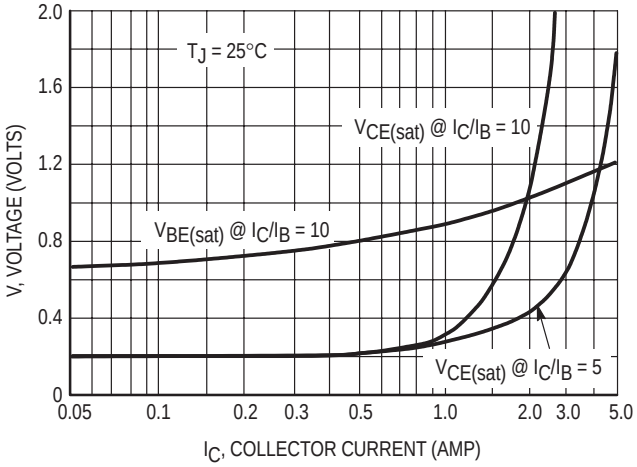


Figure 3. "On" Voltages

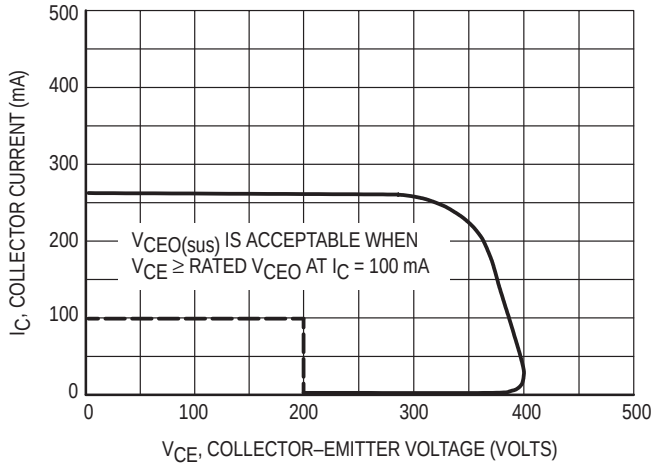


Figure 4. Sustaining Voltage Test Load Line

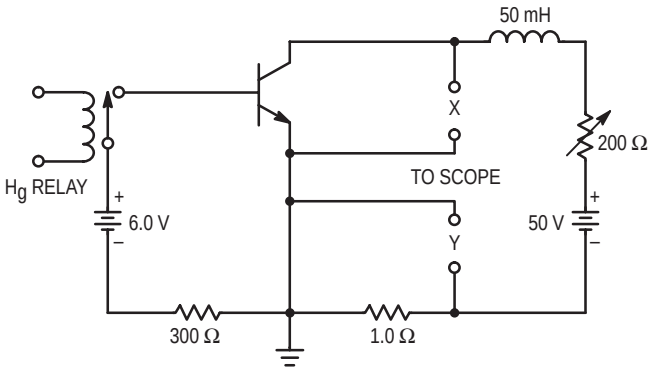


Figure 5. Sustaining Voltage Test Circuit

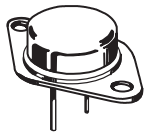
MJ413
MJ423

High-Voltage NPN Silicon Transistors

. . . designed for medium–to–high voltage inverters, converters, regulators and switching circuits.

- High Voltage — V_{CEX} = 400 Vdc
- Gain Specified to 3.5 Amp
- High Frequency Response to 2.5 MHz

10 AMPERE
POWER TRANSISTORS
NPN SILICON
400 VOLTS
125 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ413	MJ423	Unit
Collector–Emitter Voltage	V_{CEX}	400	400	Vdc
Collector–Base Voltage	V_{CB}	400	400	Vdc
Emitter–Base Voltage	V_{EB}	5.0	5.0	Vdc
Collector Current — Continuous	I_C	10	10	Adc
Base Current	I_B	2.0	2.0	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1.0		Watts W/°C
Operating Junction Temperature Range	T_J	–65 to +150		°C
Storage Temperature Range	T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.0	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage* (1) (I_C = 100 mAdc, I_B = 0)		$V_{(BR)CEO(sus)}$	325	—	Vdc
Collector Cutoff Current (V_{CE} = 400 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 400 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)		I_{CEX}	 — —	 0.25 0.5	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc)	 MJ413 MJ423 	h_{FE}	 20 15 30 10	 80 — 90 —	—
Collector–Emitter Saturation Voltage (1) (I_C = 0.5 Adc, I_B = 0.05 Adc) (I_C = 1.0 Adc, I_B – 0.10 Adc)	 MJ413 MJ423	$V_{CE(sat)}$	 — —	 0.8 0.8	Vdc
Base–Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 0.05 Adc) (I_C = 1.0 Adc, I_B = 0.1 Adc)	 MJ413 MJ423	$V_{BE(sat)}$	 — —	 1.25 1.25	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 200 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	2.5	—	MHz

(1) PW ≤ 300 μs Duty Cycle ≤ 2.0%.

REV 7

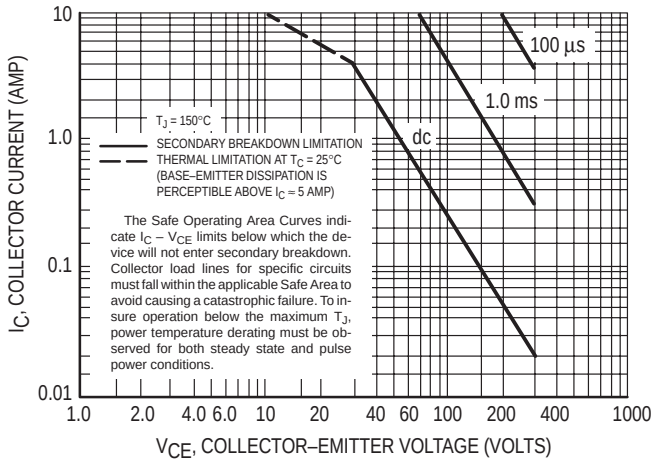


Figure 1. Active–Region Safe–Operating Area

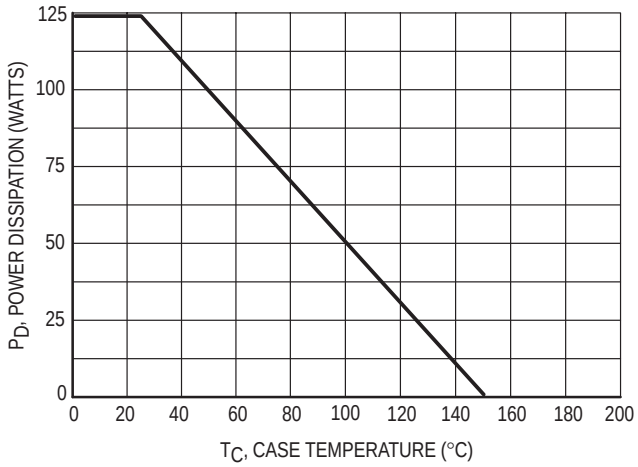


Figure 2. Power–Temperature Derating Curve

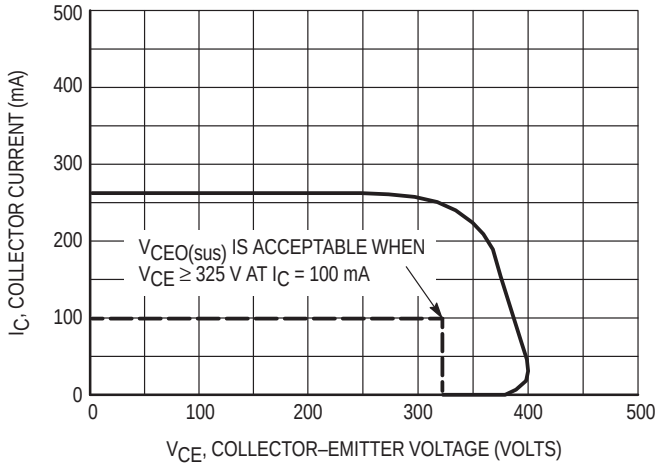


Figure 3. Sustaining Voltage Test Load Line

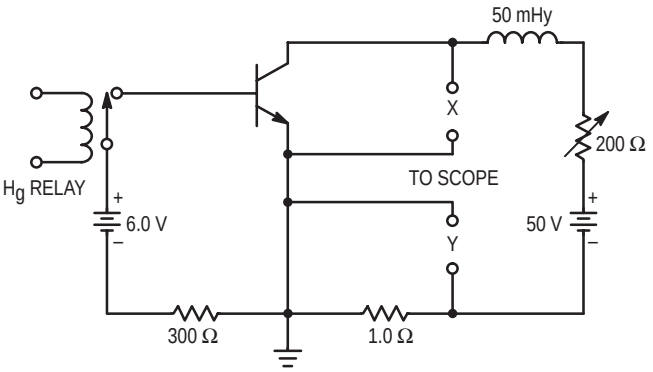


Figure 4. Sustaining Voltage Test Circuit

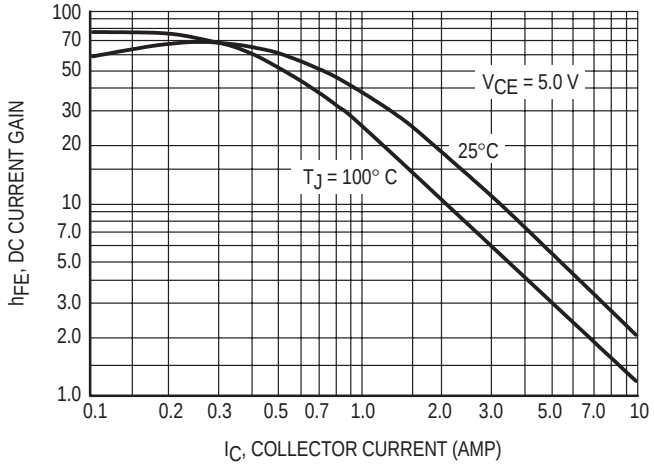


Figure 5. Current Gain

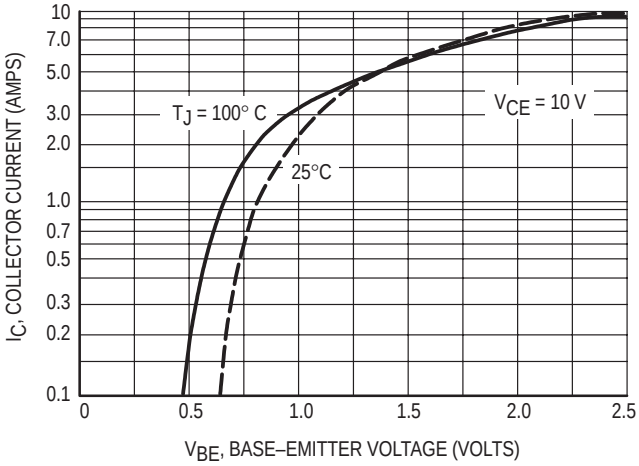


Figure 6. Transconductance

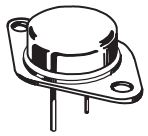
MJ802

High-Power NPN Silicon Transistor

30 AMPERE
POWER TRANSISTOR
NPN SILICON
100 VOLTS
200 WATTS

. . . for use as an output device in complementary audio amplifiers to 100–Watts music power per channel.

- High DC Current Gain — h_{FE} = 25–100 @ I_C = 7.5 A
- Excellent Safe Operating Area
- Complement to the PNP MJ4502



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CER}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Collector–Emitter Voltage	V_{CEO}	90	Vdc
Emitter–Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

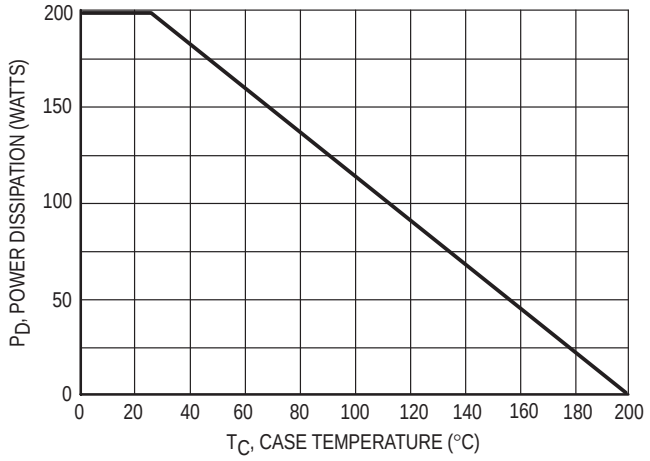


Figure 1. Power–Temperature Derating Curve

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage(1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	BV_{CER}	100	—	Vdc
Collector–Emitter Sustaining Voltage(1) (I_C = 200 mAdc)	$V_{CEO(sus)}$	90	—	Vdc
Collector–Base Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 — —	 1.0 5.0	mAdc
Emitter–Base Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS(1)				
DC Current Gain(1) (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	—
Base–Emitter "On" Voltage (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.3	Vdc
Collector–Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{CE(sat)}$	—	0.8	Vdc
Base–Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{BE(sat)}$	—	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	—	MHz

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

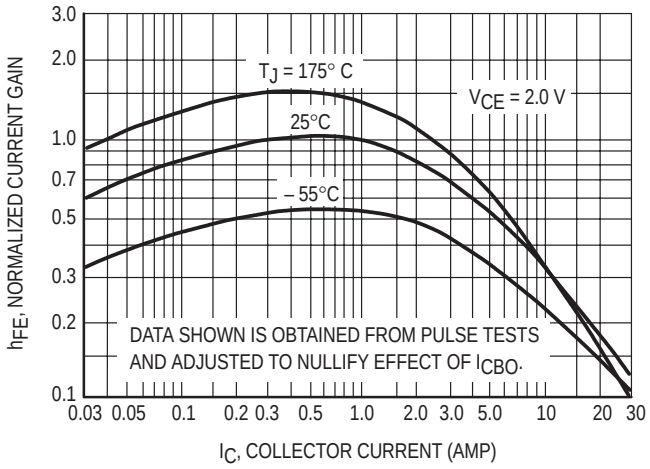


Figure 2. DC Current Gain

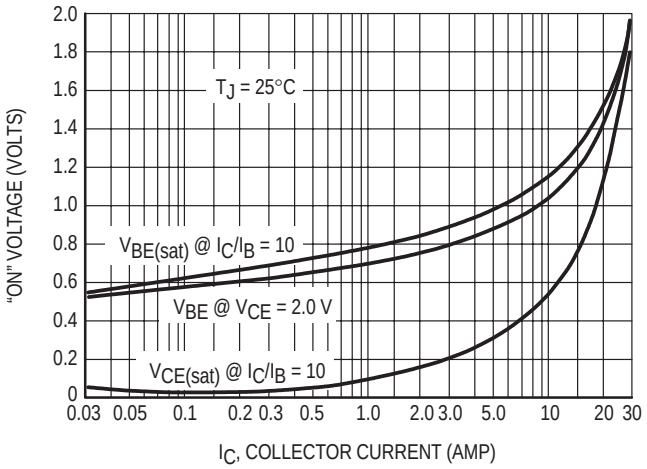


Figure 3. "On" Voltages

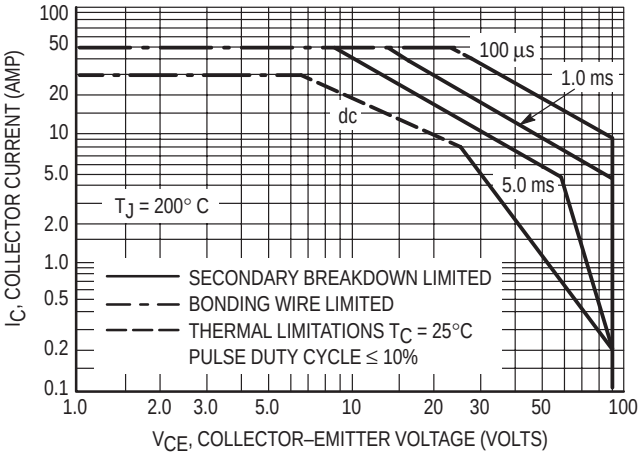


Figure 4. Active Region Safe Operating Area

The Safe Operating Area Curves indicate I_C – V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power temperature derating must be observed for both steady state and pulse power conditions.

Medium-Power Complementary Silicon Transistors

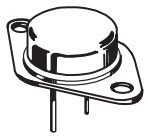
. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain — h_{FE} = 6000 (Typ) @ I_C = 3.0 Adc
- Monolithic Construction with Built–in Base–Emitter Shunt Resistors

NPN
MJ1000
MJ1001*

***Motorola Preferred Device**

10 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60 – 80 VOLTS
90 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ1000	MJ1001	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	10		Adc
Base Current	I_B	0.1		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	90 0.515		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.94	°C/W

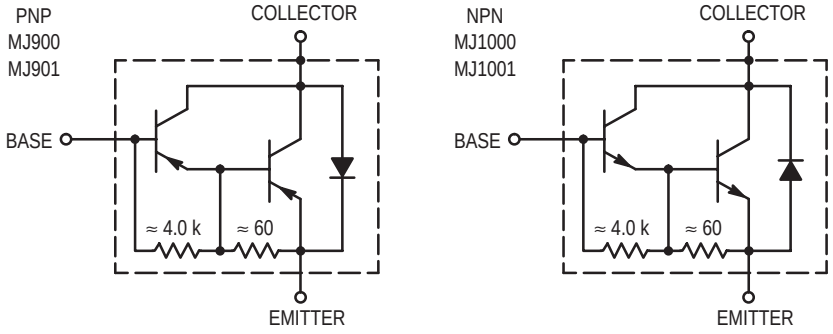


Figure 1. Darlington Circuit Schematic

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	MJ1000 MJ1001	$V_{(BR)CEO}$	60 80	— —	Vdc
Collector Emitter Leakage Current		I_{CER}			mAdc
(V_{CB} = 60 Vdc, R_{BE} = 1.0k ohm)	MJ1000		—	1.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0k ohm)	MJ1001		—	1.0	
(V_{CB} = 60 Vdc, R_{BE} = 1.0k ohm, T_C = 150°C)	MJ1000		—	5.0	
(V_{CB} = 80 Vdc, R_{BE} = 1.0k ohm, T_C = 150°C)	MJ1001		—	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
Collector Emitter Leakage Current (V_{CE} = 30 Vdc, I_B = 0)	MJ1000	I_{CEO}	—	500	μAdc
(V_{CE} = 40 Vdc, I_B = 0)	MJ1001		—	500	
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000	—	—
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			750	—	
Collector Emitter Saturation Voltage(1) (I_C = 30 Adc, I_B = 12 mAdc)		$V_{CE(sat)}$	—	2.0	Vdc
(I_C = 8.0 Adc, I_B = 40 mAdc)			—	4.0	
Base Emitter Voltage(1) (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	2.5	Vdc

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

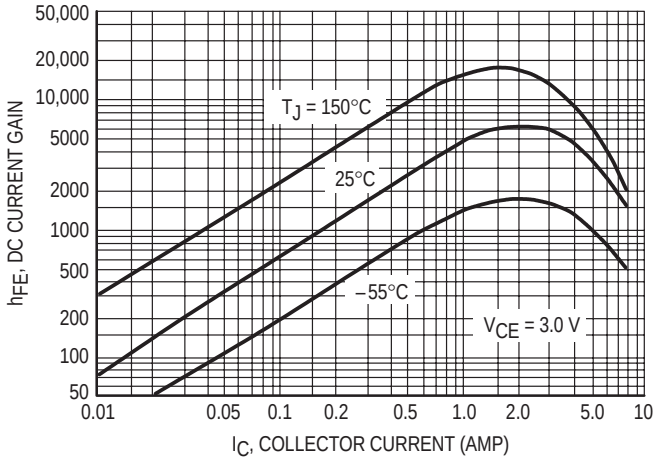


Figure 2. DC Current Gain

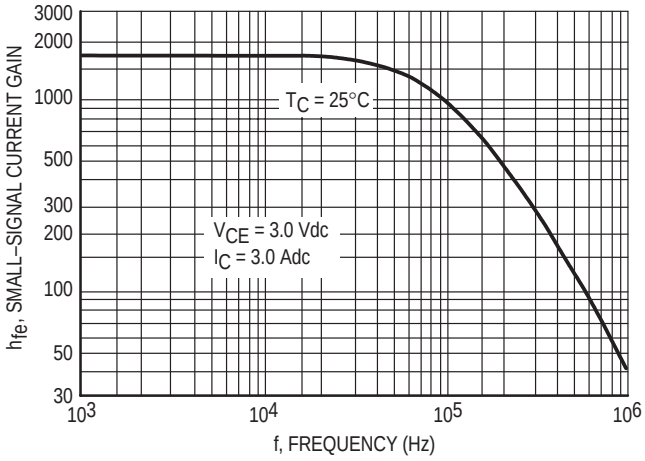


Figure 3. Small–Signal Current Gain

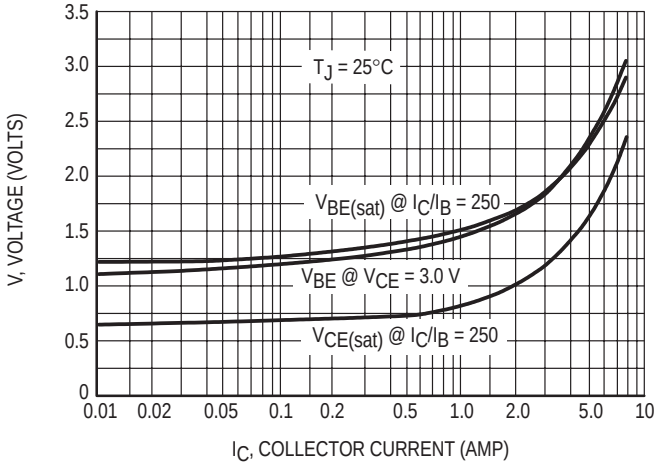


Figure 4. "On" Voltages

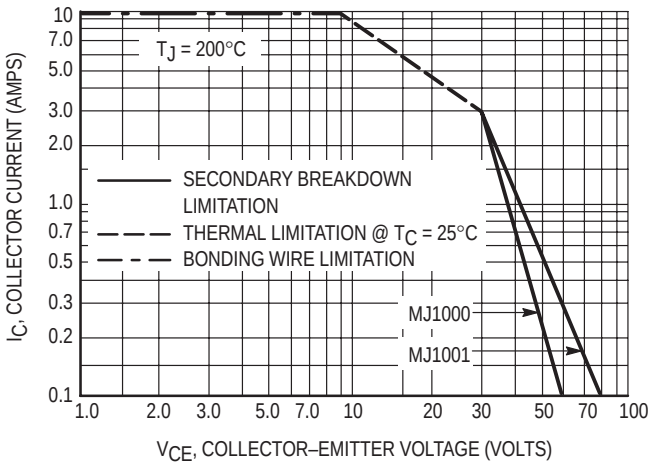


Figure 5. DC Safe Operating Area

There we two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

MJ2955 (See 2N3055)
MJ2955A
(See 2N3055A)

Medium-Power Complementary Silicon Transistors

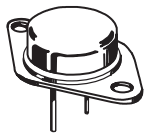
. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain — h_{FE} = 4000 (Typ) @ I_C = 5.0 Adc
- Monolithic Construction with Built–in Base–Emitter Shunt Resistors

PNP
MJ2500
MJ2501*
NPN
MJ3000
MJ3001*

***Motorola Preferred Device**

10 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60–80 VOLTS
150 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ2500 MJ3000	MJ2501 MJ3001	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	10		Adc
Base Current	I_B	0.2		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.857		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	°C/W

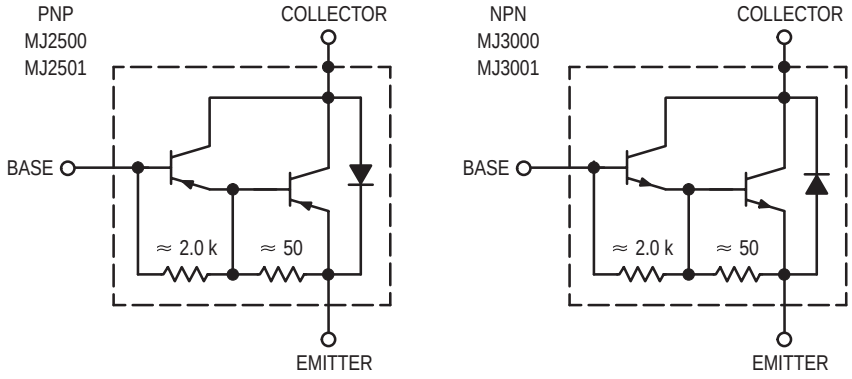


Figure 1. Darlington Circuit Schematic

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector Emitter Breakdown Voltage(1) (I_C = 100 mAdc, I_B = 0)	MJ2500, MJ3000 MJ2501, MJ3001	$V_{(BR)CEO}$	60 80	— —	Vdc
Collector–Emitter Leakage Current		I_{CER}			mAdc
(V_{EB} = 60 Vdc, R_{BE} = 1.0 k ohm)	MJ2500, MJ3000		—	1.0	
(V_{EB} = 80 Vdc, R_{BE} = 1.0 k ohm)	MJ2501, MJ3001		—	1.0	
(V_{EB} = 60 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ2500, MJ3000		—	5.0	
(V_{EB} = 80 Vdc, R_{BE} = 1.0 k ohm, T_C = 150°C)	MJ2501, MJ3001		—	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
Collector Emitter Leakage Current (V_{CE} = 30 Vdc, I_B = 0)	MJ2500, MJ3000	I_{CEO}	—	1.0	mAdc
(V_{CE} = 40 Vdc, I_B = 0)	MJ2501, MJ3001		—	1.0	
ON CHARACTERISTICS(1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000	—	—
Collector–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 20 mAdc)		$V_{CE(sat)}$	—	2.0	Vdc
(I_C = 10 Adc, I_B = 50 mAdc)			—	4.0	
Base Emitter Voltage (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	3.0	Vdc

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

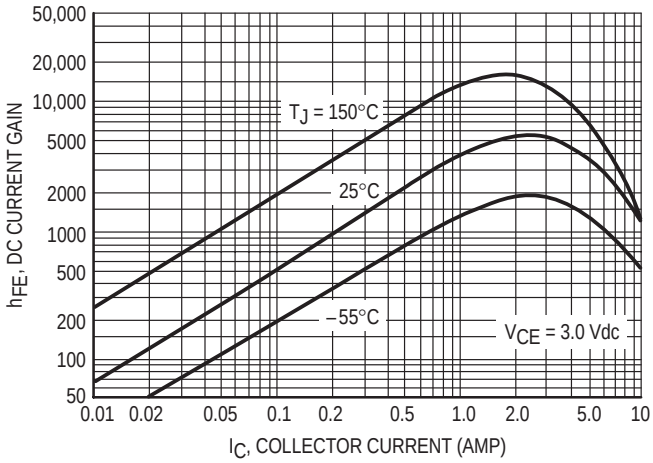


Figure 2. DC Current Gain

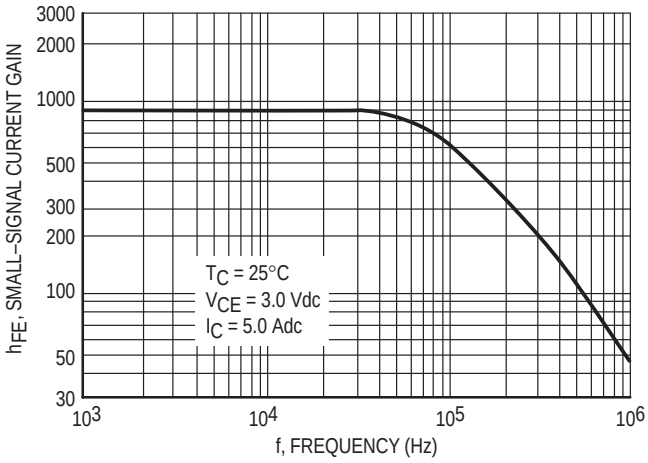


Figure 3. Small–Signal Current Gain

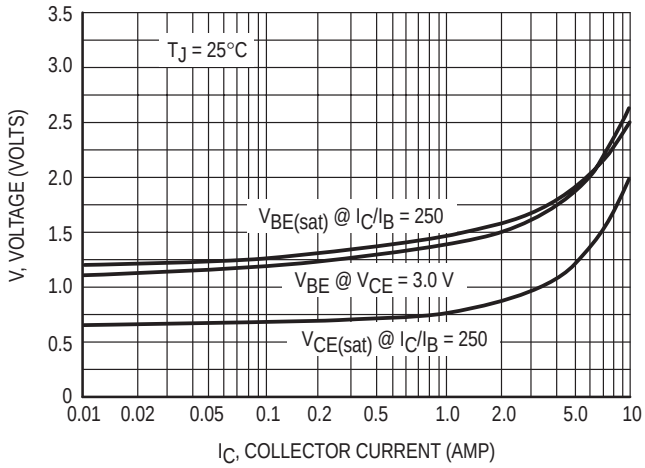


Figure 4. "On" Voltages

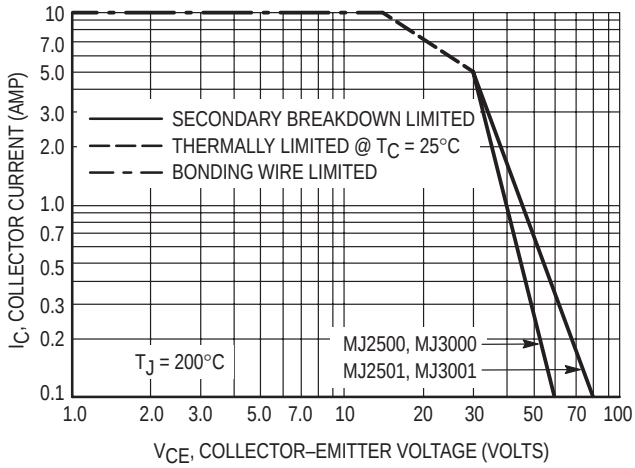


Figure 5. DC Safe Operating Area

There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

NPN
MJ3281A*
PNP
MJ1302A*

*Motorola Preferred Device

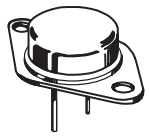
Designer's™ Data Sheet

Complementary NPN-PNP Silicon Power Bipolar Transistor

The MJ3281A and MJ1302A are PowerBase power transistors for high power audio, disk head positioners and other linear applications.

- Designed for 100 W Audio Frequency
- Gain Complementary:
  - — Gain Linearity from 100 mA to 7 A
  - — High Gain — 60 to 175
  - — h_{FE} = 45 (Min) @ I_C = 8 A
- Low Harmonic Distortion
- High Safe Operation Area — 1 A/100 V @ 1 sec
- High f_T — 30 MHz Typical

15 AMPERE
COMPLEMENTARY
SILICON POWER
TRANSISTORS
200 VOLTS
250 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	200	Vdc
Collector–Base Voltage	V_{CBO}	200	Vdc
Emitter–Base Voltage	V_{EBO}	7	Vdc
Collector–Emitter Voltage — 1.5 V	V_{CEX}	200	Vdc
Collector Current — Continuous — Peak (1)	I_C	15 25	Adc
Base Current — Continuous	I_B	1.5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	250 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	200	—	—	Vdc
Emitter–Base Voltage (I_E = 100 μAdc, I_C = 0)	V_{EBO}	7	—	—	Vdc
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0)	I_{CBO}	—	—	50	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	—	—	5	μAdc
Emitter Cutoff Current (V_{EB} = 7 Vdc, I_C = 0)	I_{EBO}	—	—	25	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector with Base Forward Biased	$I_{S/b}$				Adc
(V_{CE} = 50 Vdc, t = 1 s (non–repetitive)		4	—	—	
(V_{CE} = 100 Vdc, t = 1 s (non–repetitive)		1	—	—	
ON CHARACTERISTICS					
DC Current Gain	h_{FE}				
(I_C = 100 mAdc, V_{CE} = 5 Vdc)		60	125	175	
(I_C = 1 Adc, V_{CE} = 5 Vdc)		60	—	175	
(I_C = 3 Adc, V_{CE} = 5 Vdc)		60	—	175	
(I_C = 5 Adc, V_{CE} = 5 Vdc)		60	—	175	
(I_C = 7 Adc, V_{CE} = 5 Vdc)		60	115	175	
(I_C = 8 Adc, V_{CE} = 5 Vdc)		45	—	—	
(I_C = 15 Adc, V_{CE} = 5 Vdc)		12	35	—	
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1 Adc)	$V_{CE(sat)}$	—	—	3	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)	f_T	—	30	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	—	600	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

PNP MJ1302A

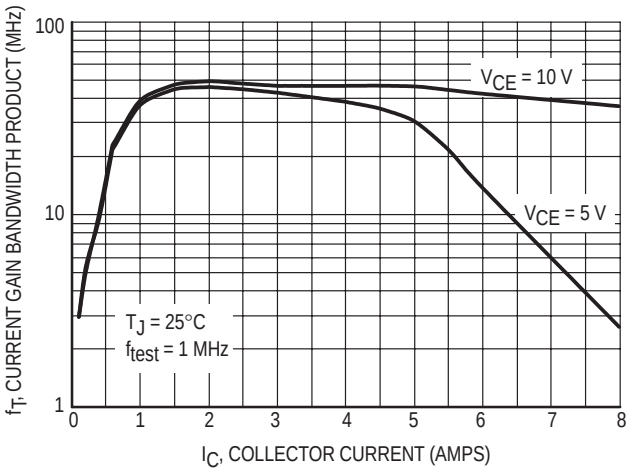


Figure 1. Current–Gain — Bandwidth Product

NPN MJ3281A

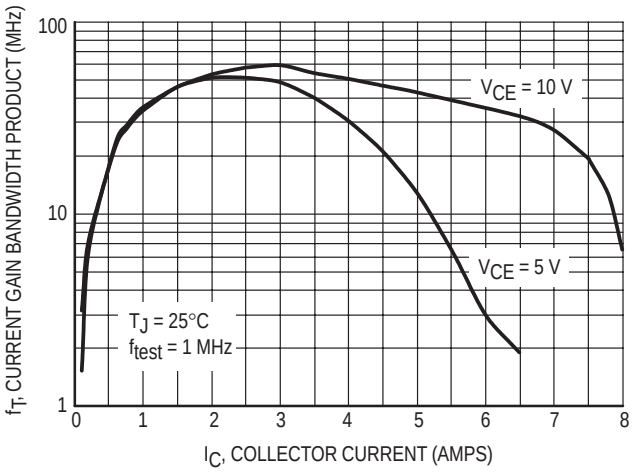


Figure 2. Current–Gain — Bandwidth Product

PNP MJ1302A

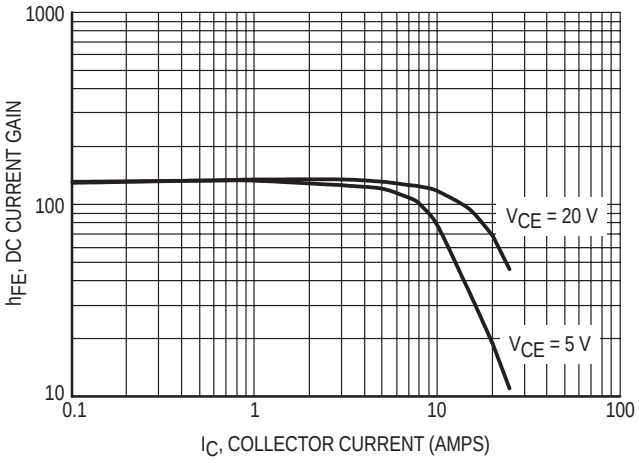


Figure 3. DC Current Gain

NPN MJ3281A

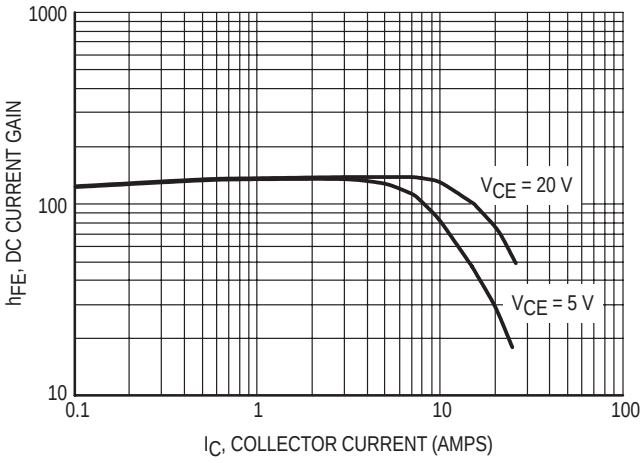


Figure 4. DC Current Gain

PNP MJ1302A

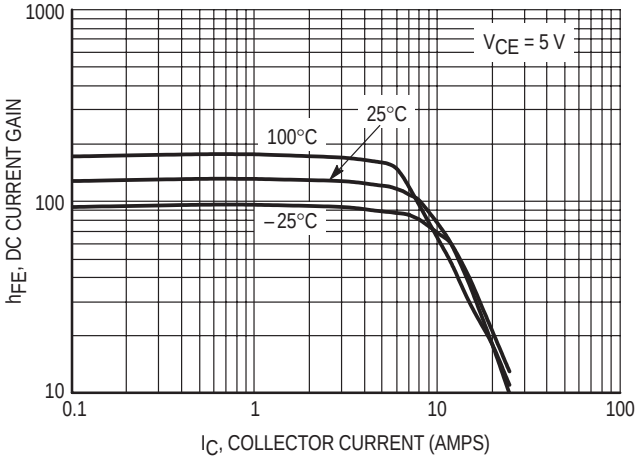


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJ3281A

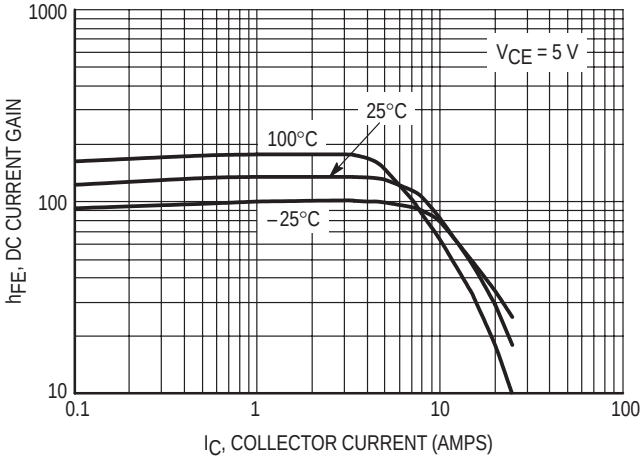


Figure 6. DC Current Gain, V_{CE} = 5 V

TYPICAL CHARACTERISTICS

PNP MJ1302A

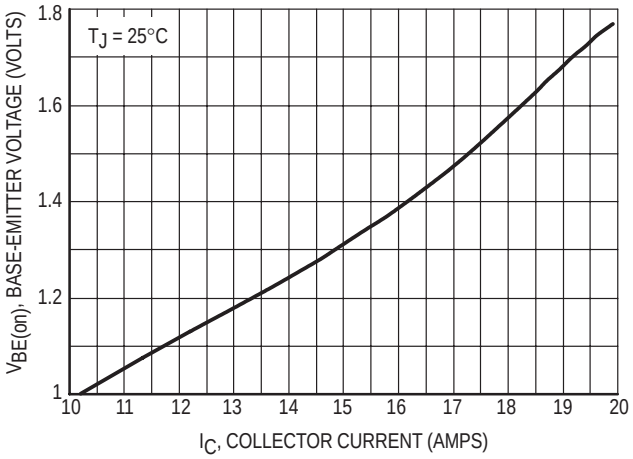


Figure 7. Typical Base–Emitter Voltage

NPN MJ3281A

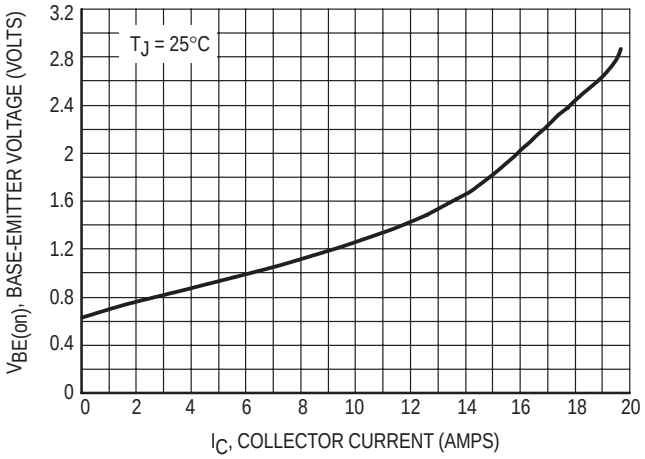


Figure 8. Typical Base–Emitter Voltage

PNP MJ1302A

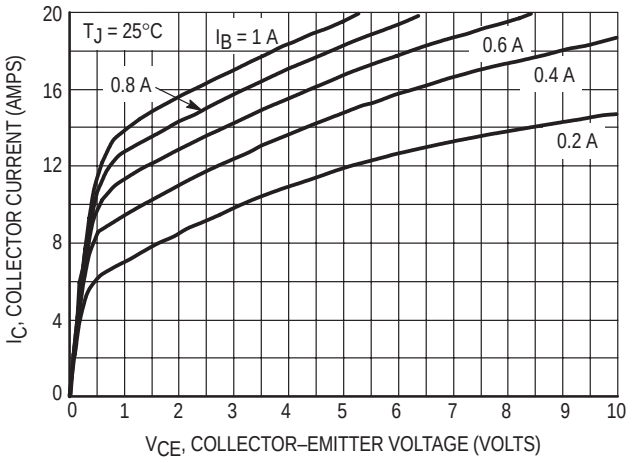


Figure 9. Typical Output Characteristics

NPN MJ3281A

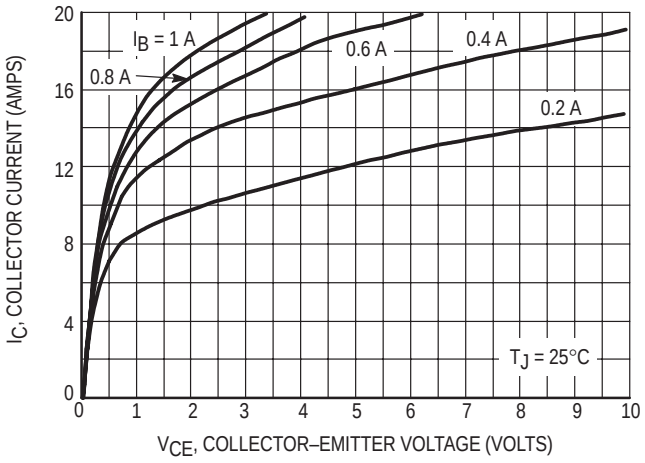


Figure 10. Typical Output Characteristics

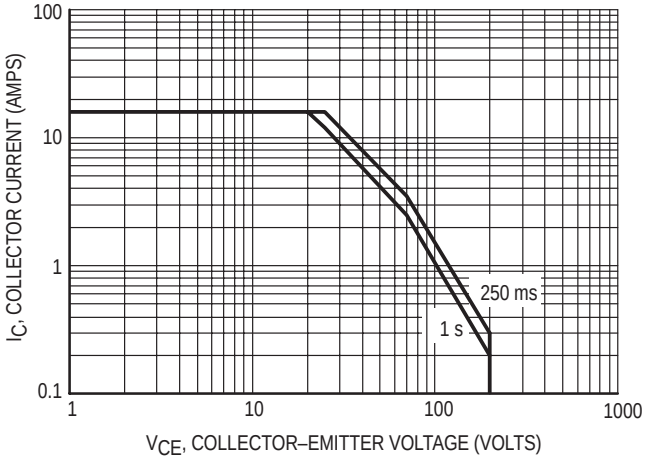


Figure 11. Forward Bias Safe Operating Area (FBSOA)

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

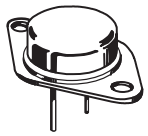
MJ4502

High-Power PNP Silicon Transistor

30 AMPERE
POWER TRANSISTOR
PNP SILICON
100 VOLTS
200 WATTS

. . . for use as an output device in complementary audio amplifiers to 100–Watts music power per channel.

- High DC Current Gain — h_{FE} = 25–100 @ I_C = 7.5 A
- Excellent Safe Operating Area
- Complement to the NPN MJ802



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CER}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Collector–Emitter Voltage	V_{CEO}	90	Vdc
Emitter–Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	30	Adc
Base Current	I_B	7.5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

MAXIMUM RATINGS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

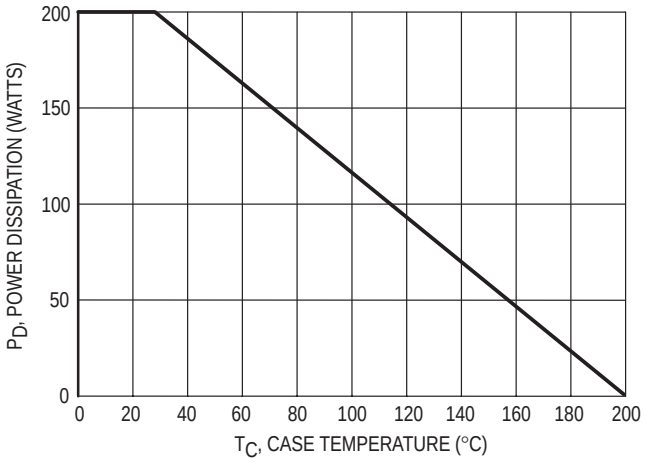


Figure 1. Power–Temperature Derating Curve

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage(1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	$V_{(BR)CER}$	100	—	Vdc
Collector–Emitter Sustaining Voltage(1) (I_C = 200 mAdc)	$V_{CEO(sus)}$	90	—	Vdc
Collector–Base Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 — —	 1.0 5.0	mAdc
Emitter–Base Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	25	100	—
Base–Emitter “On” Voltage (I_C = 7.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	—	1.3	Vdc
Collector–Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{CE(sat)}$	—	0.8	Vdc
Base–Emitter Saturation Voltage (I_C = 7.5 Adc, I_B = 0.75 Adc)	$V_{BE(sat)}$	—	1.3	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.0	—	MHz

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

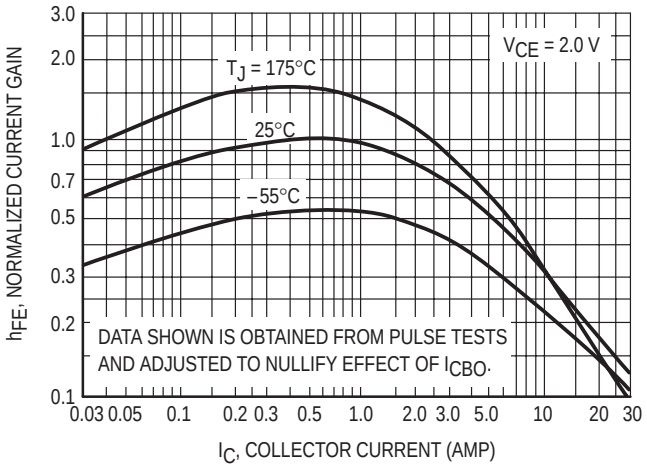


Figure 2. DC Current Gain

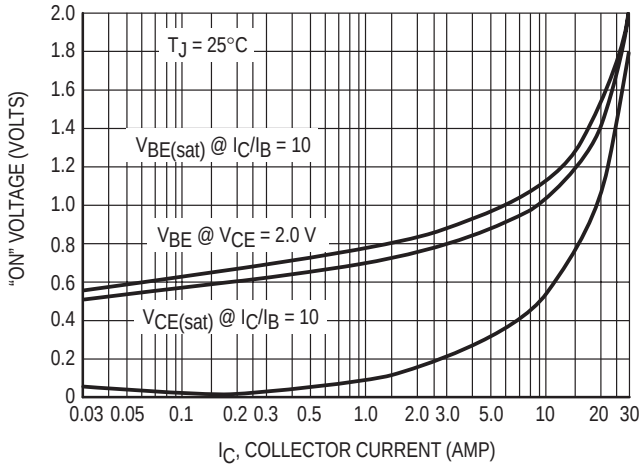


Figure 3. “On” Voltages

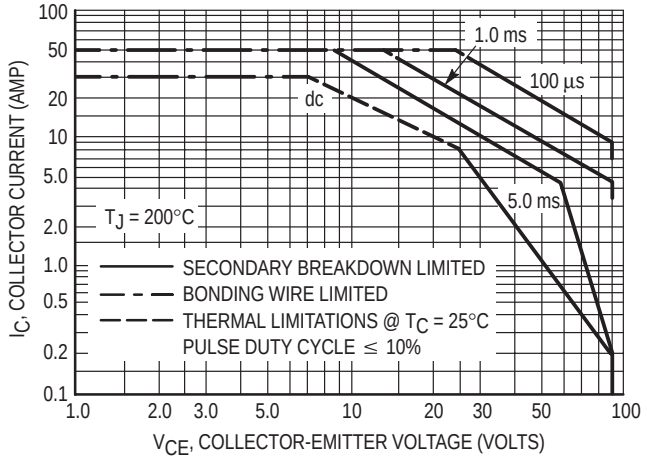


Figure 4. Active Region Safe Operating Area

The Safe Operating Area Curves indicate I_C – V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power–temperature derating must be observed for both steady state and pulse power conditions.

MJ10000

Designer's™ Data Sheet

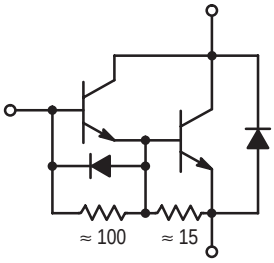
SWITCHMODE Series NPN Silicon Power Darlington Transistor

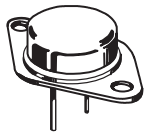
20 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS
350 VOLTS
175 WATTS

The MJ10000 Darlington transistor is designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times With Inductive Loads —
210 ns Inductive Fall Time (Typ)
Saturation Voltages
Leakage Currents





CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	350	Vdc
Collector–Emitter Voltage	V_{CEX}	400	Vdc
Collector–Emitter Voltage	V_{CEV}	450	Vdc
Emitter Base Voltage	V_{EB}	8	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 30	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5	Adc
Total Power Dissipation @ T_C = 25°C @ T_C =100°C Derate above 25°C	P_D	175 100 1	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 4

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)						
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	MJ10000	$V_{CEO(sus)}$	 350	 —	 —	Vdc
Collector–Emitter Sustaining Voltage (Table 1, Figure 12) I_C = 2 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C I_C = 10 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C	 MJ10000 MJ10000	$V_{CEX(sus)}$	 400 275	 — —	 — —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEV}	 — —	 — —	 0.25 5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	5	mAdc
Emitter Cutoff Current (V_{EB} = 8 Vdc, I_C = 0)		I_{EBO}	—	—	150	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 11			Adc
ON CHARACTERISTICS (2)						
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc) (I_C = 10 Adc, V_{CE} = 5 Vdc)		h_{FE}	 50 40	 — —	 600 400	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 400 mAdc) (I_C = 20 Adc, I_B = 1 Adc) (I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)		$V_{CE(sat)}$	 — — —	 — — —	 1.9 3 2	Vdc
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)		$V_{BE(sat)}$	 — —	 — —	 2.5 2.5	Vdc
Diode Forward Voltage (1) (I_F = 10 Adc)		V_f	—	3	5	Vdc
DYNAMIC CHARACTERISTICS						
Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		h_{fe}	10		—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}	100		325	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time Rise Time Storage Time Fall Time	(V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%)	t_d t_r t_s t_f	 — — —	 0.12 0.20 1.5 1.1	 0.2 0.6 3.5 2.4	 μs μs μs μs
Inductive Load, Clamped (Table 1)						
Storage Time Crossover Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv} t_c	— —	3.5 1.5	5.5 3.7	μs μs
Storage Time Crossover Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv} t_c	— —	1.0 0.7	— —	μs μs

(1) The internal Collector–to–Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode Is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

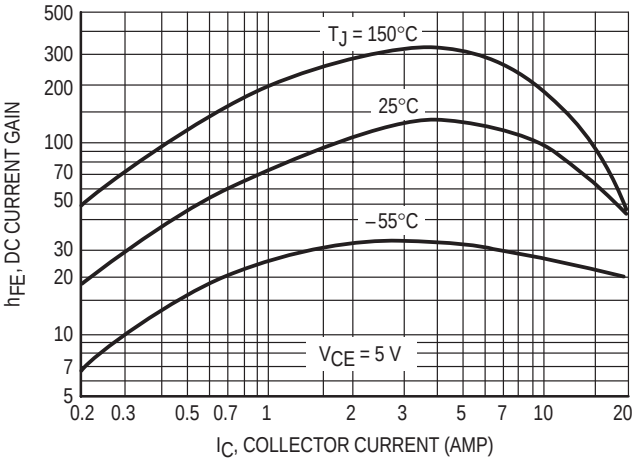


Figure 1. DC Current Gain

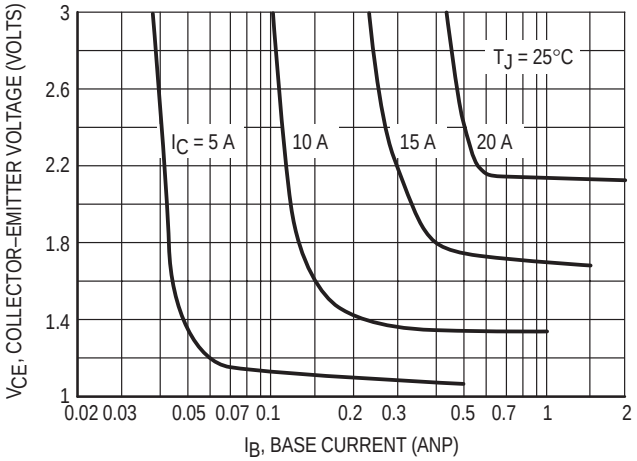


Figure 2. Collector Saturation Region

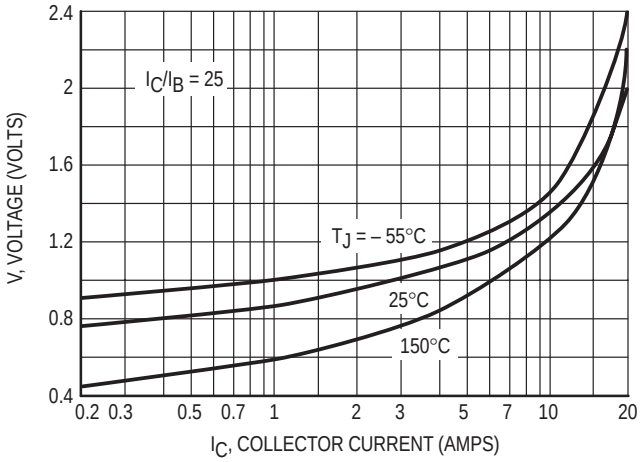


Figure 3. Collector Emitter Saturation Voltages

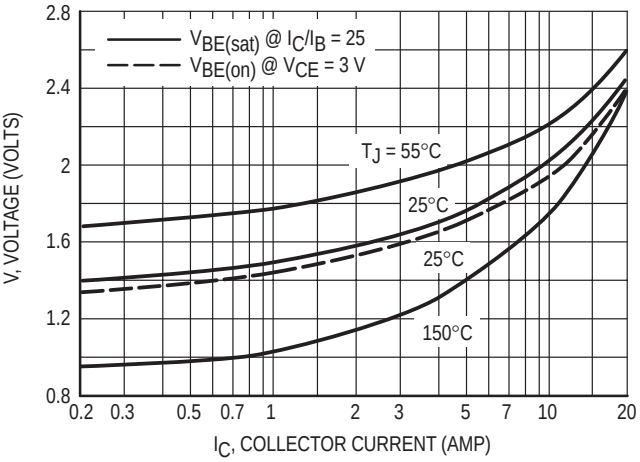


Figure 4. Base-Emitter Voltage

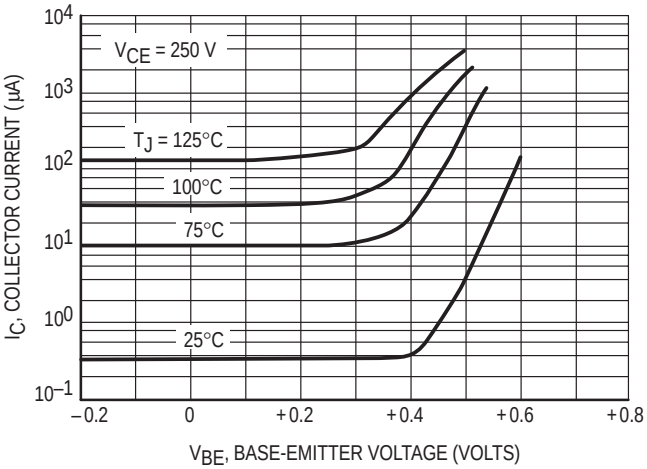


Figure 5. Collector Cutoff Region

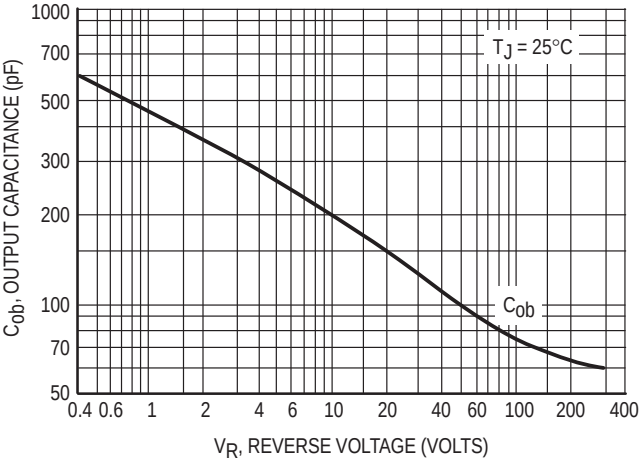
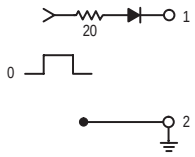
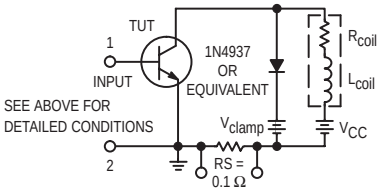
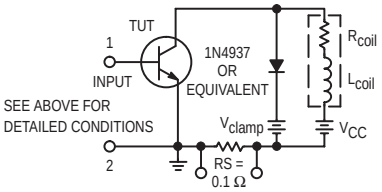
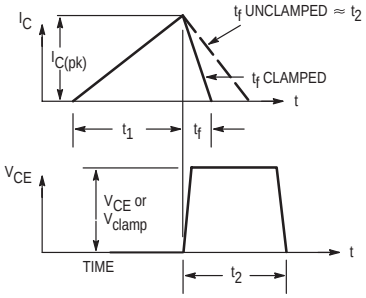
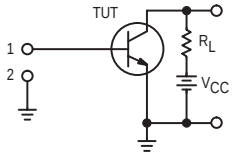


Figure 6. Output Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 250 mA	INDUCTIVE TEST CIRCUIT 	
CIRCUIT VALUES	L_{coil} = 10 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 25 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

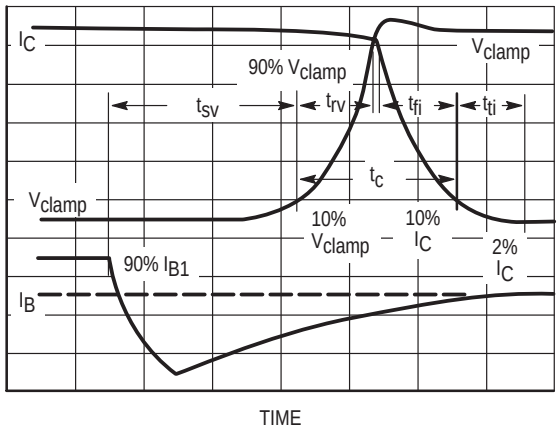


Figure 7. Inductive Switching Measurements

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn–off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2\ VCCIC(t_c)f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

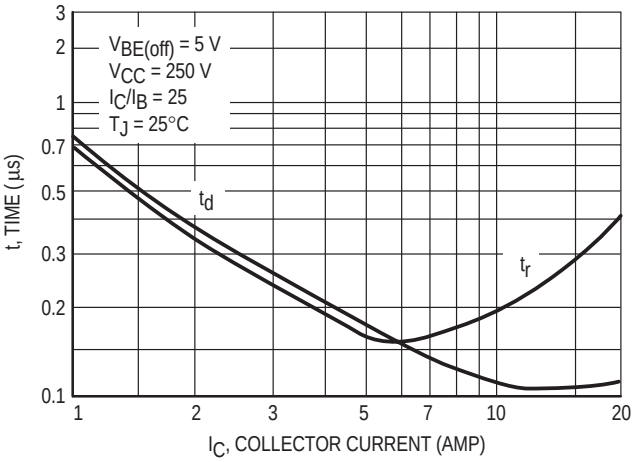


Figure 8. Turn–On Time

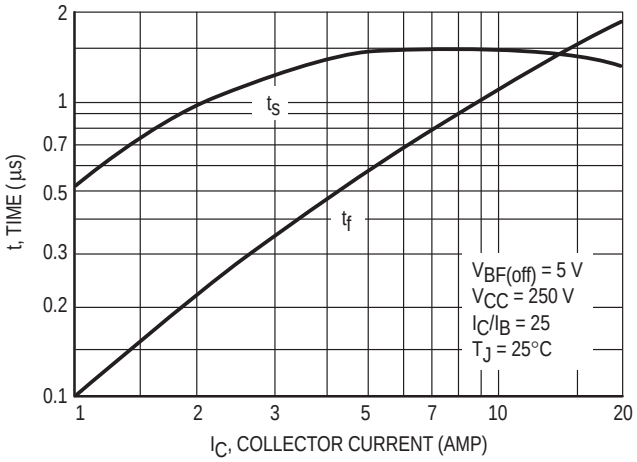


Figure 9. Turn–Off Time

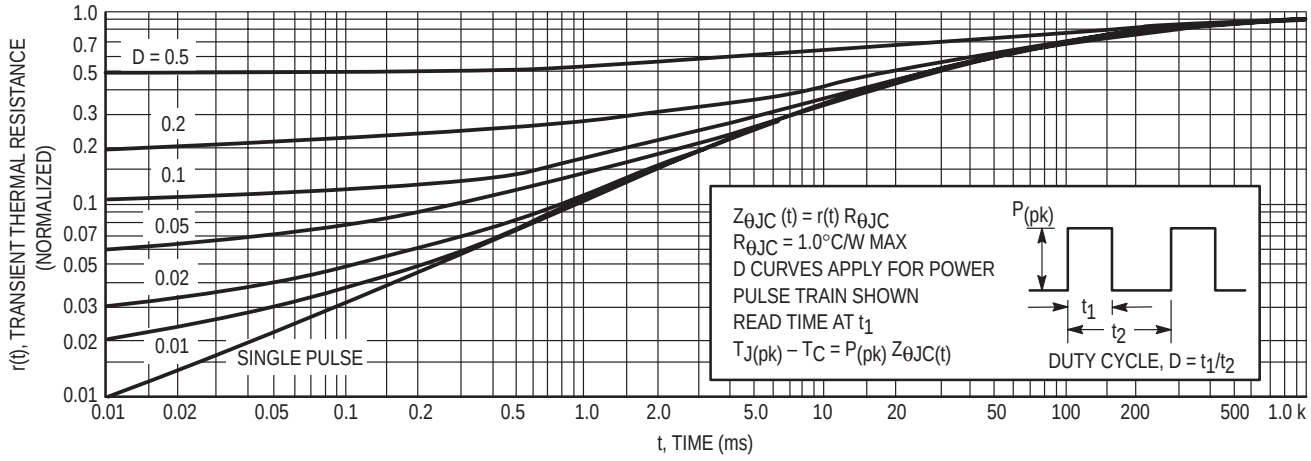


Figure 10. Thermal Response

The Safe Operating Area figures shown in Figures 11 and 12 are specified for these devices under the test conditions shown.

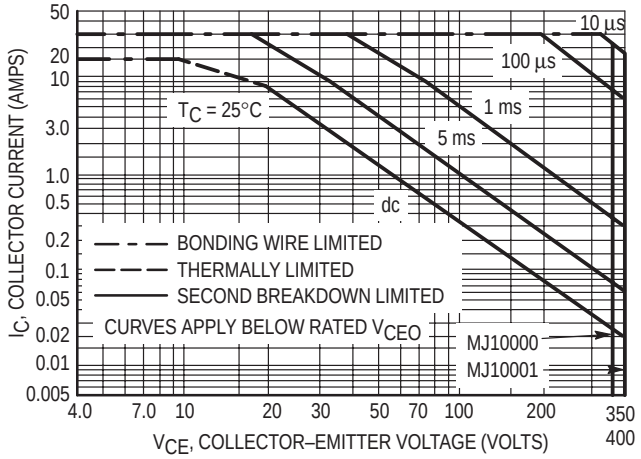


Figure 11. Forward Bias Safe Operating Area

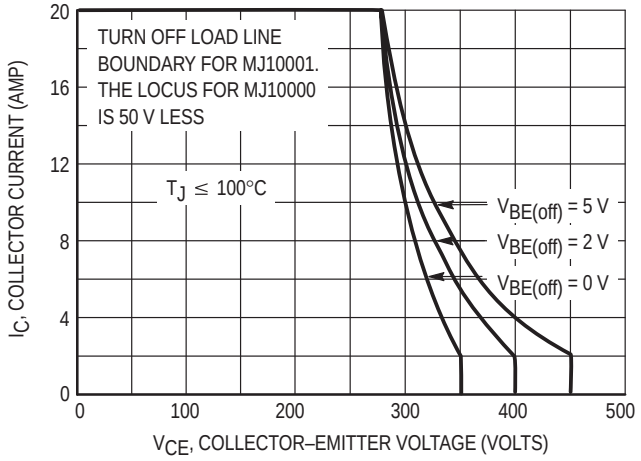


Figure 12. Reverse Bias Switching Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage–current condition that can be sustained during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

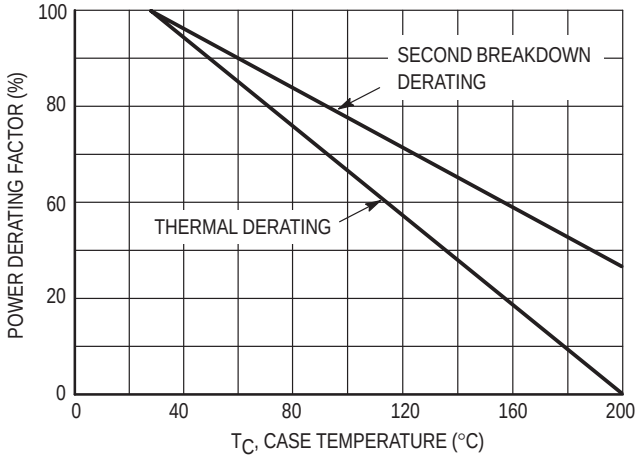


Figure 13. Power Derating

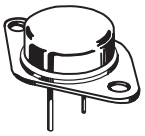
MJ10005*

*Motorola Preferred Device

Designer's™ Data Sheet

SWITCHMODE Series NPN Silicon Power Darlington Transistor with Base-Emitter Speedup Diode

20 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS
400 VOLTS
175 WATTS



CASE 1–07
TO–204AA
(TO–3)

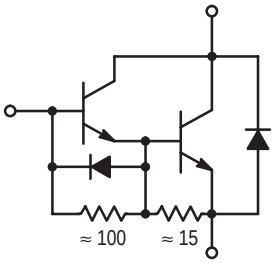
The MJ10005 Darlington transistor is designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Fast Turn–Off Times
- 40 ns Inductive Fall Time — 25°C (Typ)
- 650 ns Inductive Storage Time — 25°C (Typ)

Operating Temperature Range –65 to +200°C

100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	400	Vdc
Collector–Emitter Voltage	V_{CEX}	450	Vdc
Collector–Emitter Voltage	V_{CEV}	500	Vdc
Emitter Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 30	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Emitter Sustaining Voltage (Table 1, Figure 12) (I_C = 2.0 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) (I_C = 10 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	$V_{CEX(sus)}$	 450 325	 — —	 — —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	 — —	 — —	 0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)	I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 10 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	 50 40	 — —	 600 400	—
Collector Emitter Saturation Voltage (I_C = 10 Adc, I_B = 400 mAdc) (I_C = 20 Adc, I_B = 2.0 Adc) (I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 — — —	 1.9 3.0 2.0	Vdc
Base Emitter Saturation Voltage (I_C = 10 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 — —	 2.5 2.5	Vdc
Diode Forward Voltage (1) (I_F = 10 Adc)	V_f	—	3.0	5.0	Vdc
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	h_{fe}	10	—	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	100	—	325	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	(V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 400 mA, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%).	t_d	—	0.12	0.2	μs
Rise Time		t_r	—	0.2	0.6	μs
Storage Time		t_s	—	0.6	1.5	μs
Fall Time		t_f	—	0.15	0.5	μs
Inductive Load Clamped (Table 1)					
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_{sv}	—	1.0	2.5	μs
Crossover Time		t_c	—	0.4	1.5	μs
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_{sv}	—	0.65	—	μs
Crossover Time		t_c	—	0.2	—	μs

(1) The internal Collector–to–Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

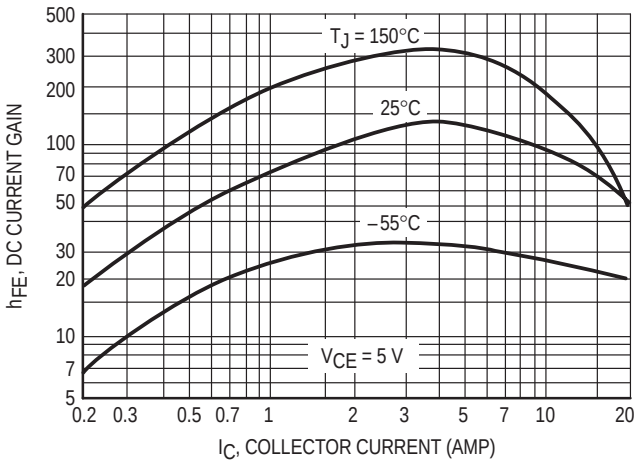


Figure 1. DC Current Gain

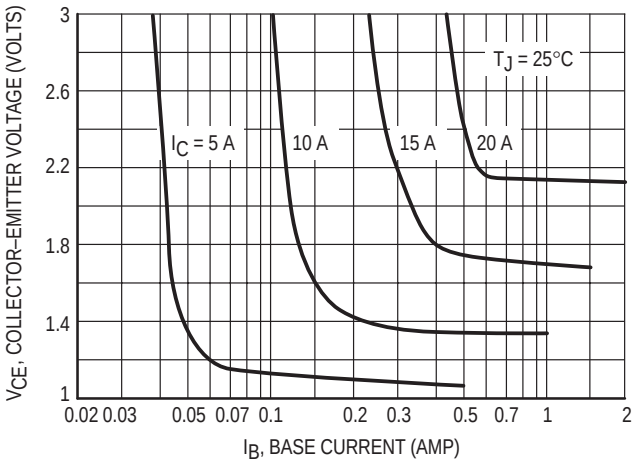


Figure 2. Collector Saturation Region

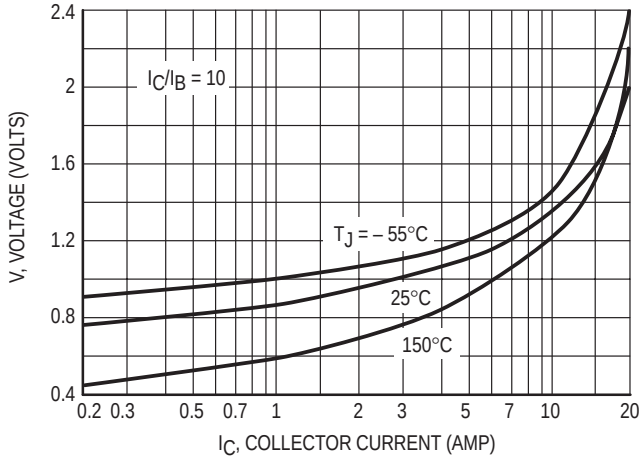


Figure 3. Collector–Emitter Saturation Voltage

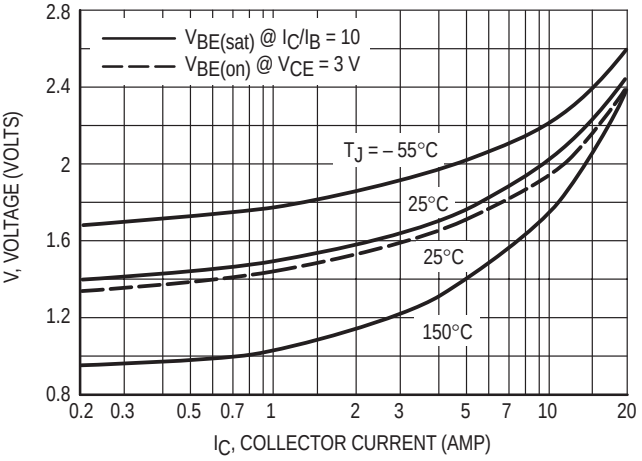


Figure 4. Base–Emitter Voltage

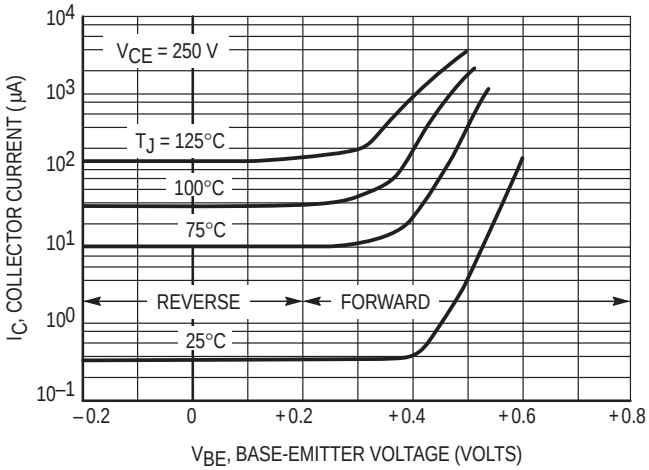


Figure 5. Collector Cutoff Region

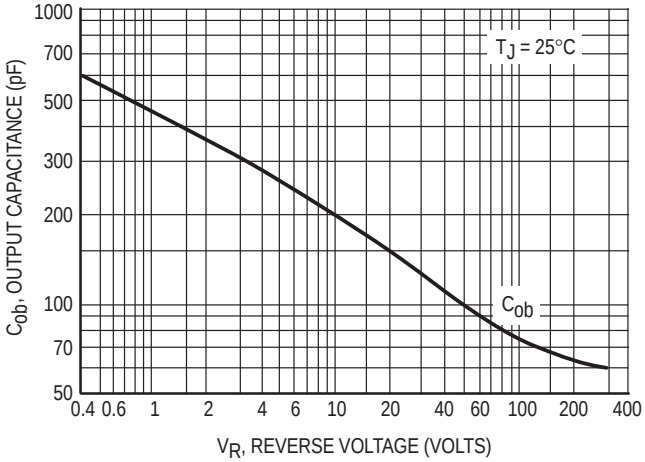
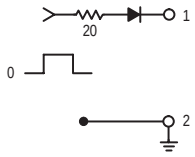
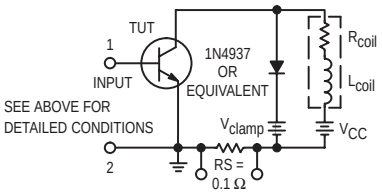
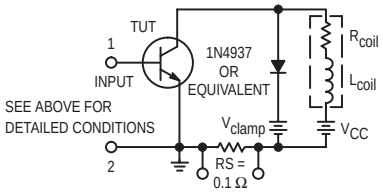
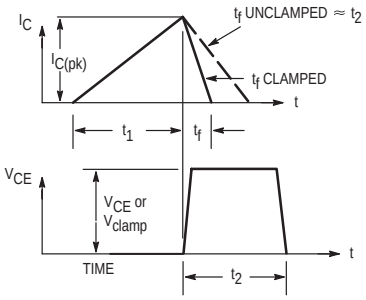
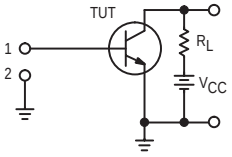


Figure 6. Output Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 250 mA	INDUCTIVE TEST CIRCUIT 	
CIRCUIT VALUES	L_{coil} = 10 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 25 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

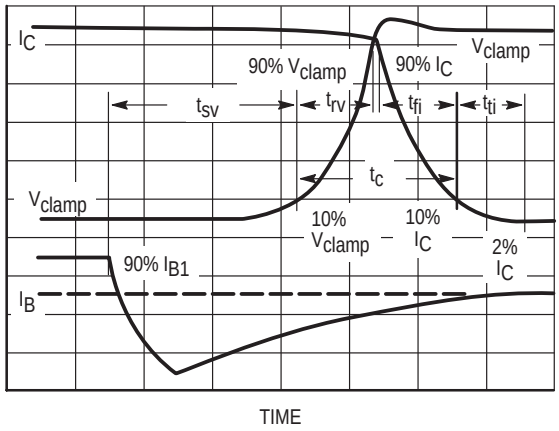


Figure 7. Inductive Switching Measurements

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn–off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222.

$$P_{SWT} = l/2\ V_{CC}\ I_C\ (t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

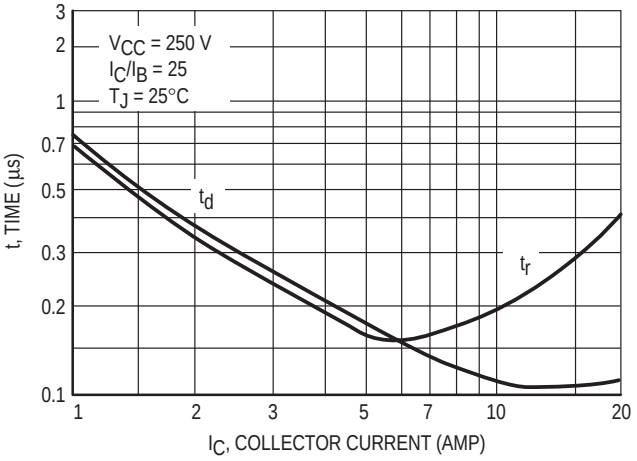


Figure 8. Turn–On Time

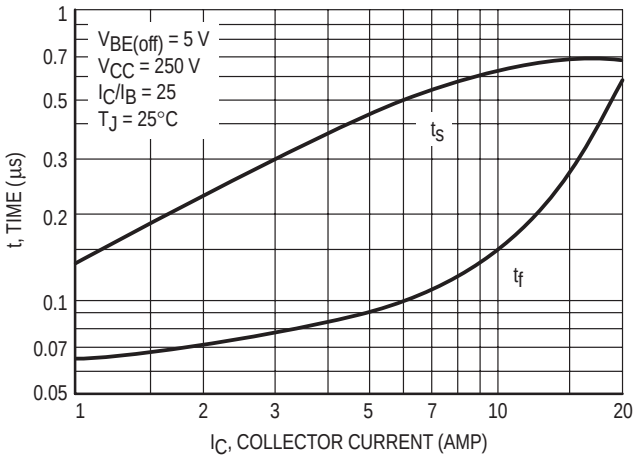


Figure 9. Turn–Off Time

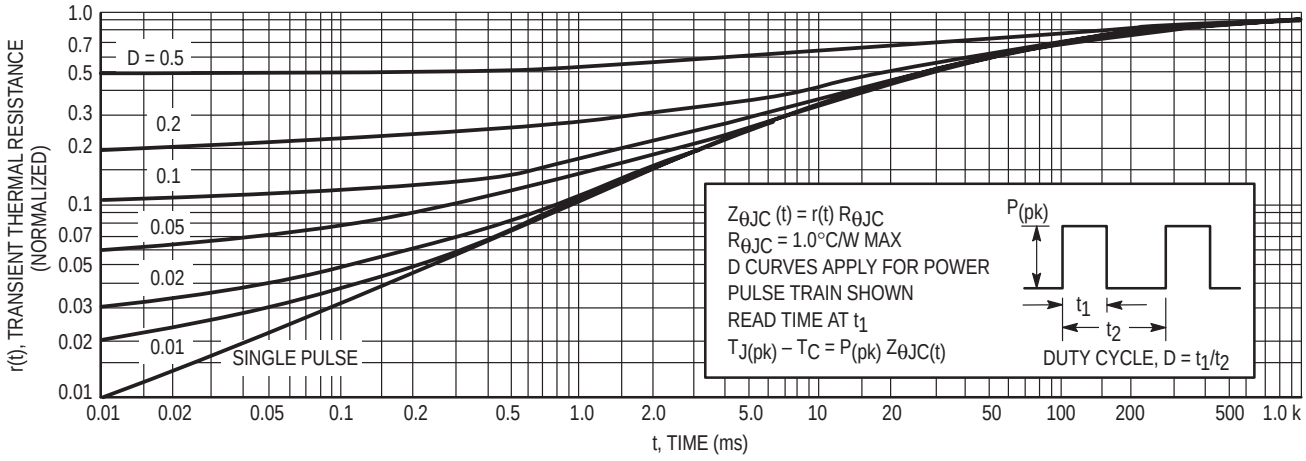


Figure 10. Thermal Response

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

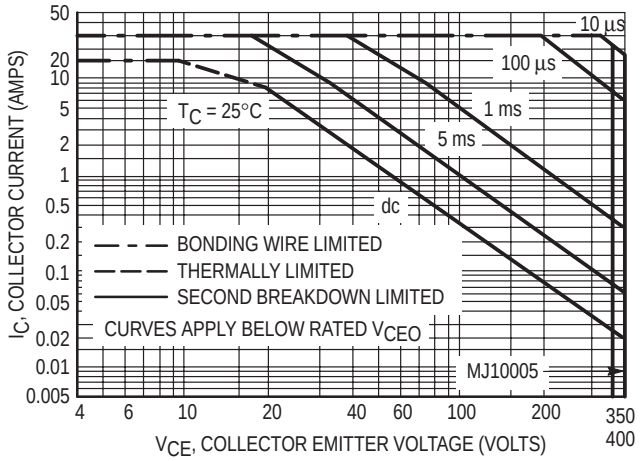


Figure 11. Forward Bias Safe Operating Area

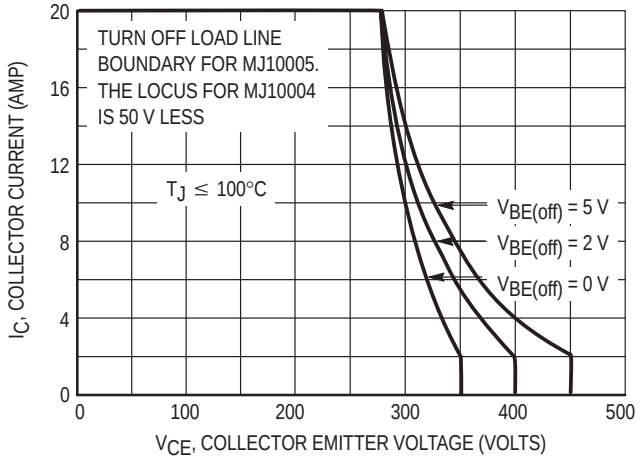


Figure 12. Reverse Bias Switching Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage–current condition that can be sustained during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

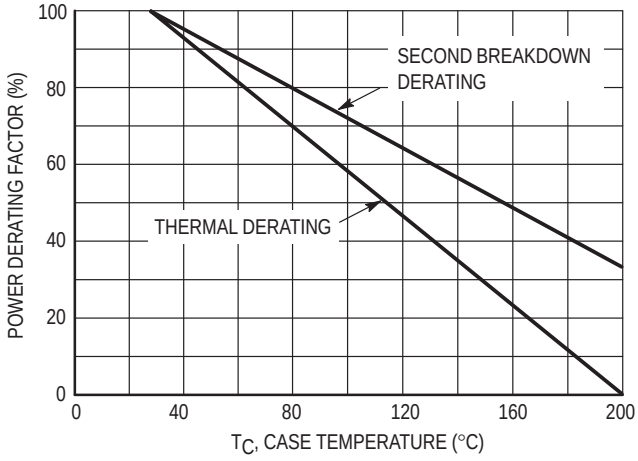


Figure 13. Power Derating

MJ10007*

*Motorola Preferred Device

Designer's™ Data Sheet

SWITCHMODE Series NPN Silicon Power Darlington Transistors with Base-Emitter Speedup Diode

10 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS
400 VOLTS
150 WATTS

The MJ10007 Darlington transistor is designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

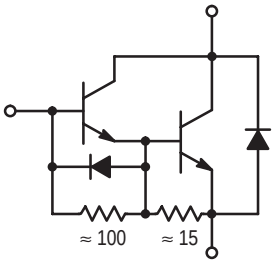
Fast Turn–Off Times

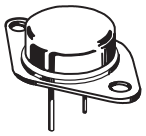
30 ns Inductive Fall Time — 25°C (Typ)
500 ns Inductive Storage Time — 25°C (Typ)

Operating Temperature Range –65 to +200°C

100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents





CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	400	Vdc
Collector–Emitter Voltage	V_{CEX}	450	Vdc
Collector–Emitter Voltage	V_{CEV}	500	Vdc
Emitter Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 20	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	150 100 0.86	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	$V_{CEO(sus)}$	400	—	—	Vdc
Collector–Emitter Sustaining Voltage (Table 1, Figure 12) (I_C = 1 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C) (I_C = 5 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	$V_{CEX(sus)}$	 450 325	 — —	 — —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1 5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	 — —	 — —	 0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 2 Vdc, I_C = 0)	I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 2.5 Adc, V_{CE} = 5.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	 40 30	 — —	 500 300	—
Collector Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 250 mAdc) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 5.0 Adc, I_B = 250 mAdc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 — — —	 1.9 2.9 2.0	Vdc
Base–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 250 mAdc) (I_C = 5.0 Adc, I_B = 250 mAdc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 — —	 2.5 2.5	Vdc
Diode Forward Voltage (1) (I_F = 5.0 Adc)	V_f	—	3.0	5	Vdc
DYNAMIC CHARACTERISTICS					
Small Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	h_{fe}	10	—	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	60	—	275	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	(V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	—	0.05	0.2	μs
Rise Time		t_r	—	0.25	0.6	μs
Storage Time		t_s	—	0.5	1.5	μs
Fall Time		t_f	—	0.06	0.5	μs
Inductive Load Clamped (Table 1)					
Storage Time	(I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_{sv}	—	0.8	2.0	μs
Crossover Time		t_c	—	0.6	1.5	μs
Storage Time	(I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_{sv}	—	0.5	—	μs
Crossover Time		t_c	—	0.3	—	μs

(1) The internal Collector–to–Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

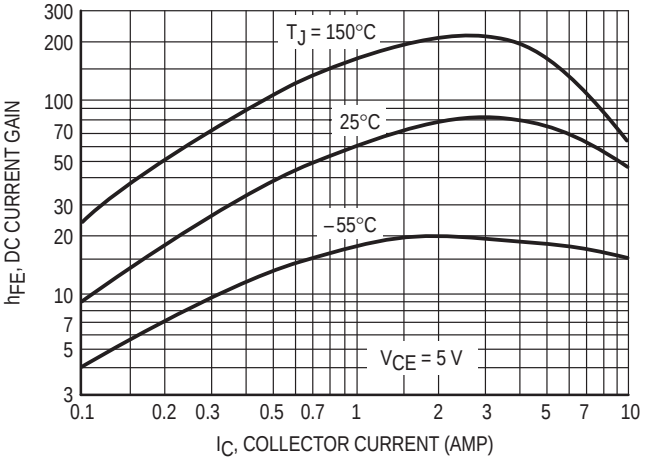


Figure 1. DC Current Gain

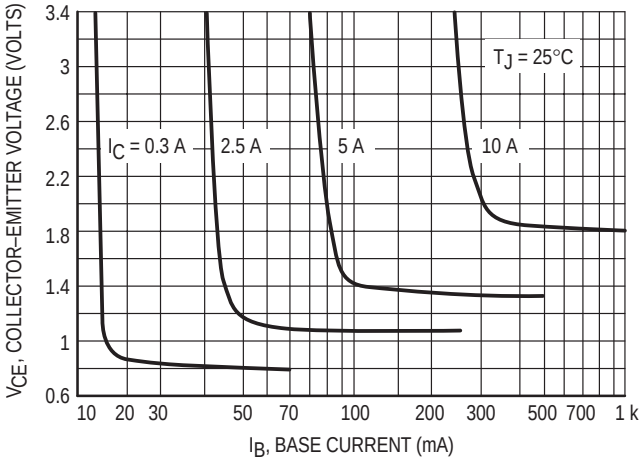


Figure 2. Collector Saturation Region

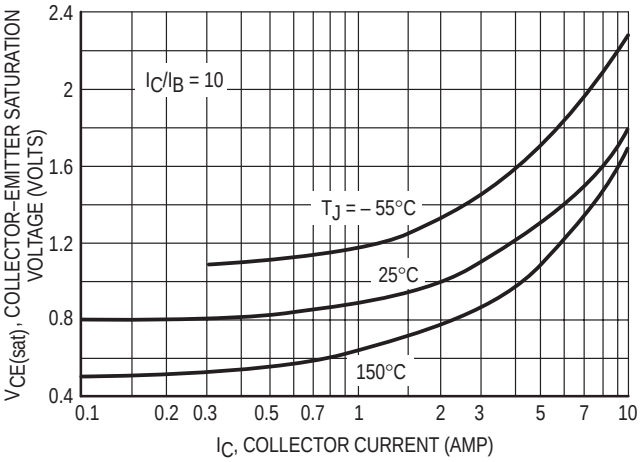


Figure 3. Collector-Emitter Saturation Voltage

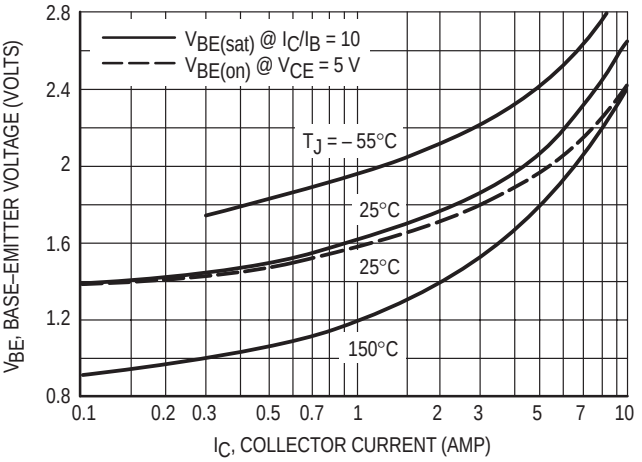


Figure 4. Base-Emitter Voltage

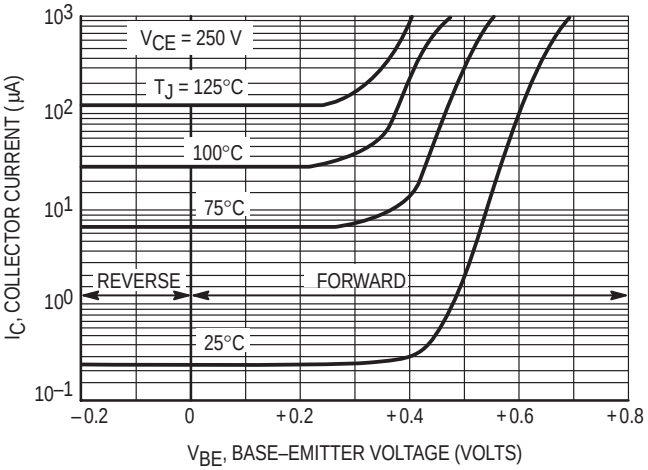


Figure 5. Collector Cutoff Region

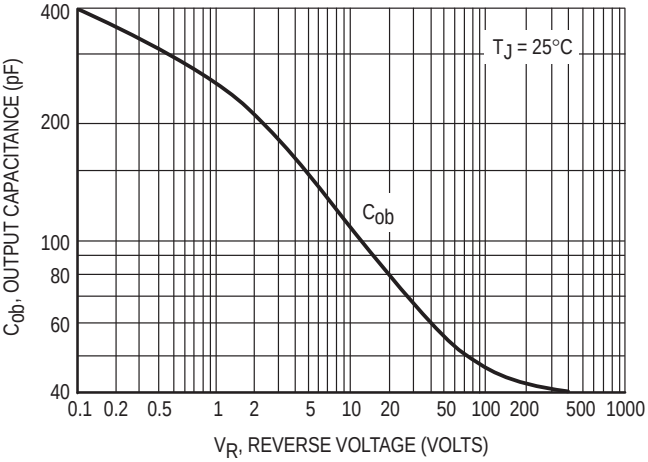
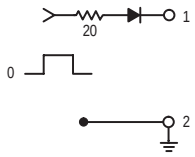
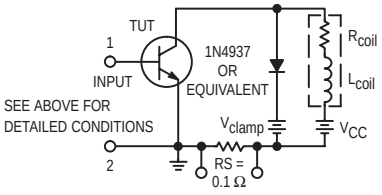
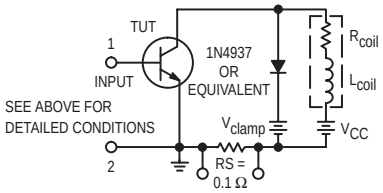
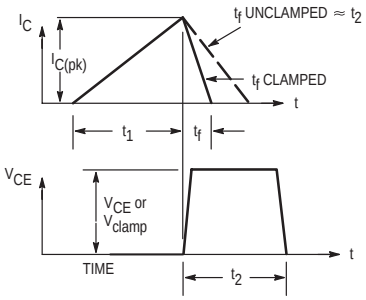
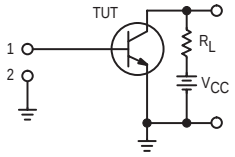


Figure 6. Output Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 250 mA	INDUCTIVE TEST CIRCUIT 	
CIRCUIT VALUES	L_{coil} = 10 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V f_o = 500 kHz V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT  OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

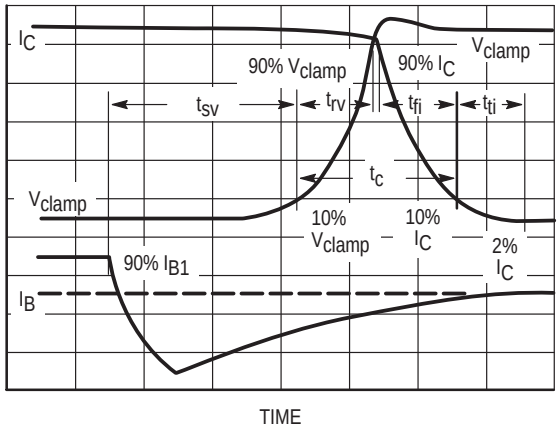


Figure 7. Inductive Switching Measurements

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn–off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222.

$$P_{SWT} = 1/2\ V_{CC}\ I_C\ (t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

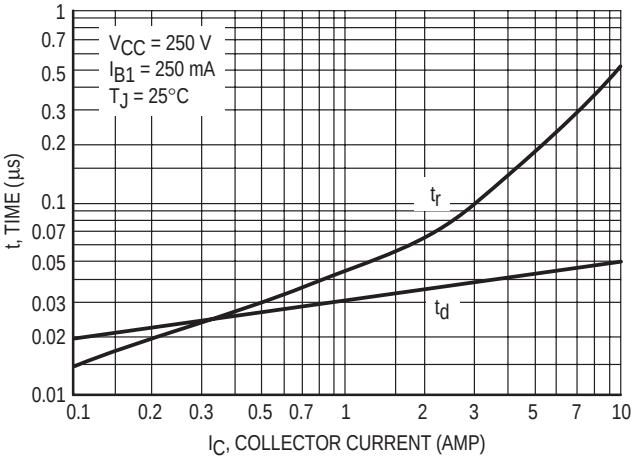


Figure 8. Turn–On Time

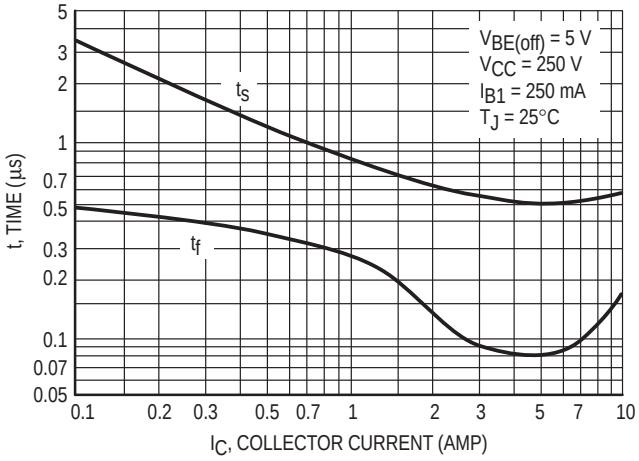


Figure 9. Turn–Off Time

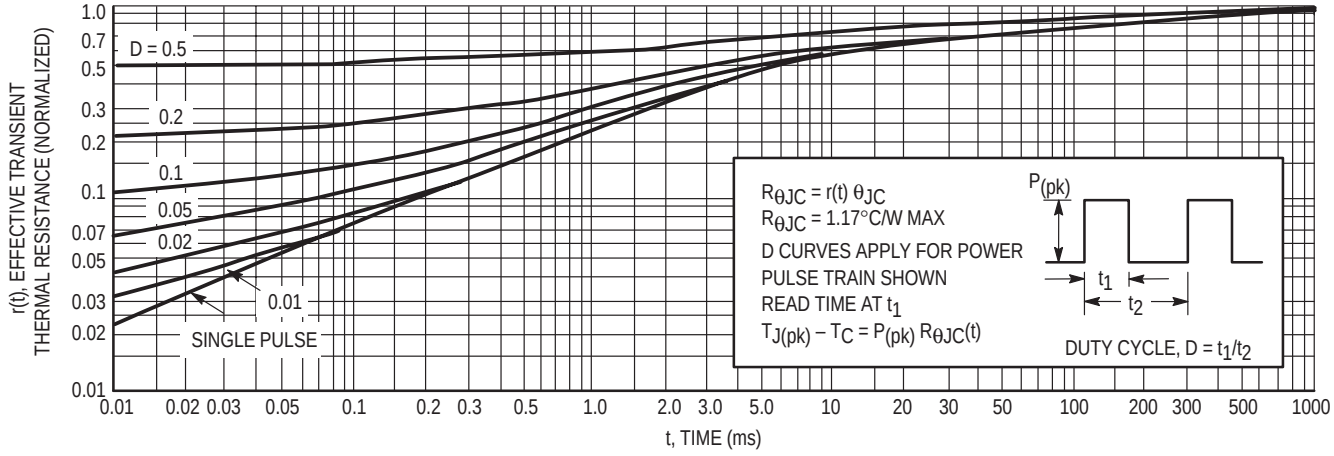


Figure 10. Thermal Response

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

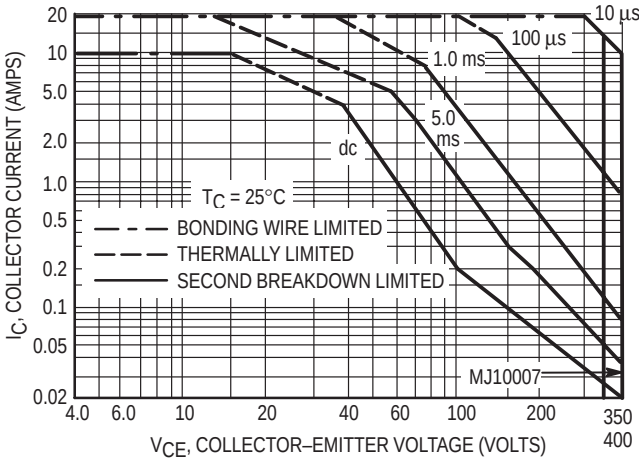


Figure 11. Forward Bias Safe Operating Area

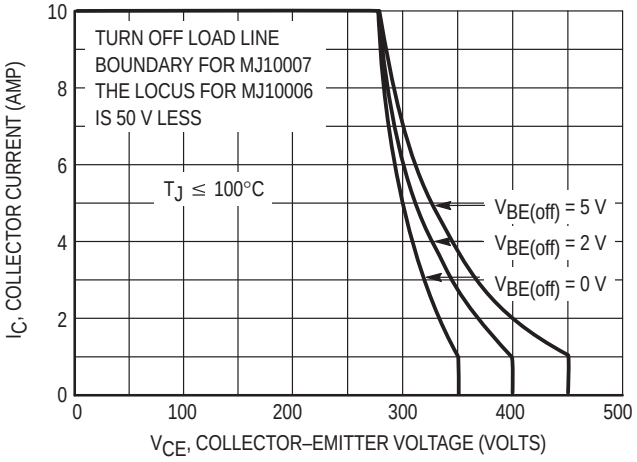


Figure 12. Reverse Bias Switching Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage–current condition that can be sustained during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

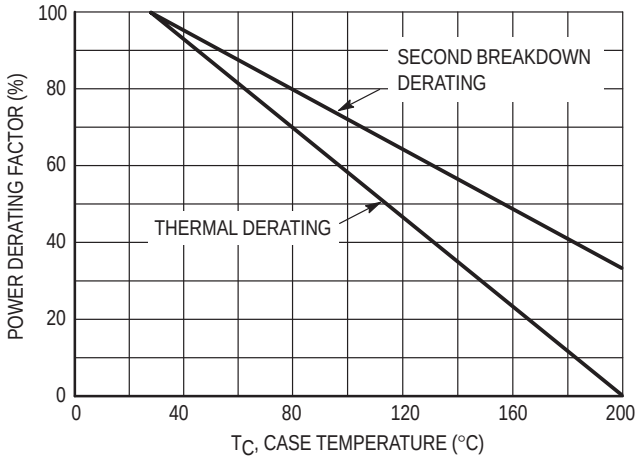


Figure 13. Power Derating

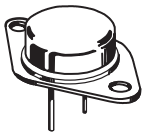
MJ10009*

*Motorola Preferred Device

Designer's™ Data Sheet

SWITCHMODE Series NPN Silicon Power Darlington Transistor with Base-Emitter Speedup Diode

20 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS
450 and 500 VOLTS
175 WATTS



CASE 1–07
TO–204AA
(TO–3)

The MJ10009 Darlington transistor is designed for high–voltage, high–speed, power switching in Inductive circuits where fall time is critical. It is particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

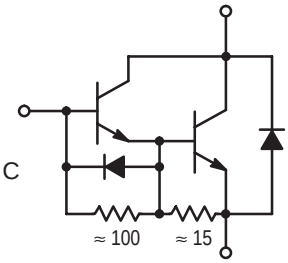
Fast Turn–Off Times

1.6 µs (max) Inductive Crossover Time – 10 A, 100°C
3.5 µs (max) Inductive Storage Time – 10 A, 100°C

Operating Temperature Range –65 to +200°C

100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	500	Vdc
Collector–Emitter Voltage	VCEX	500	Vdc
Collector–Emitter Voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EB}	8	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 30	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	$V_{CEO(sus)}$	500	—	—	Vdc
Collector Emitter Sustaining Voltage (Table 1, Figure 12) (I_C = 2 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C, $V_{BE(off)}$ = 5 V) (I_C = 10 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C, $V_{BE(off)}$ = 5 V)	$V_{CEX(sus)}$	 500 375	 — —	 — —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	 — —	 — —	 0.25 5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	5	mAdc
Emitter Cutoff Current (V_{EB} = 2 Vdc, I_C = 0)	I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc) (I_C = 10 Adc, V_{CE} = 5 Vdc)	h_{FE}	 40 30	 — —	 400 300	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 500 mAdc) (I_C = 20 Adc, I_B = 2 Adc) (I_C = 10 Adc, I_B = 500 mAdc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 — — —	 2 3.5 2.5	Vdc
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 500 mAdc) (I_C = 10 Adc, I_B = 500 mAdc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 — —	 2.5 2.5	Vdc
Diode Forward Voltage (1) (I_F = 10 Adc)	V_f	—	3	5	Vdc
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	h_{fe}	8	—	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	100	—	325	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	(V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 500 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 25 μs Duty Cycle ≤ 2%).	t_d	—	0.12	0.25	μs
Rise Time		t_r	—	0.5	1.5	μs
Storage Time		t_s	—	0.8	2.0	μs
Fall Time		t_f	—	0.2	0.6	μs
Inductive Load, Clamped (Table 1)					
Storage Time	(I_C = 10 A(pk), V_{clamp} = 250 V, I_{B1} = 500 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	1.5	3.5	μs
Crossover Time		t_c	—	0.36	1.6	μs
Storage Time	(I_C = 10 A(pk), V_{clamp} = 250 V, I_{B1} = 500 mA, $V_{BE(off)}$ = 5 Vdc)	t_{sv}	—	0.8	—	μs
Crossover Time		t_c	—	0.18	—	μs

(1) The internal Collector–to–Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

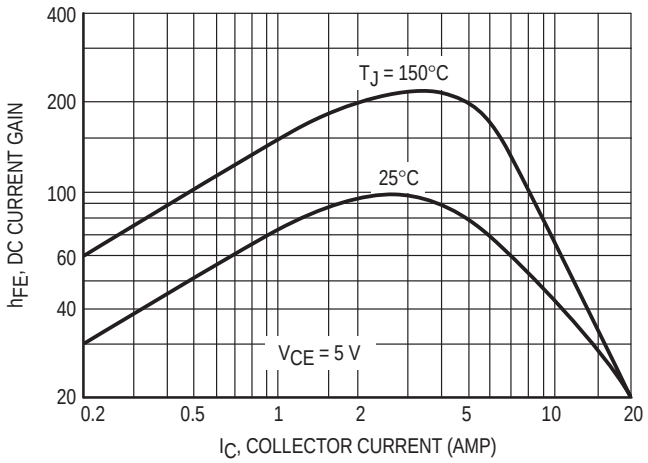


Figure 1. DC Current Gain

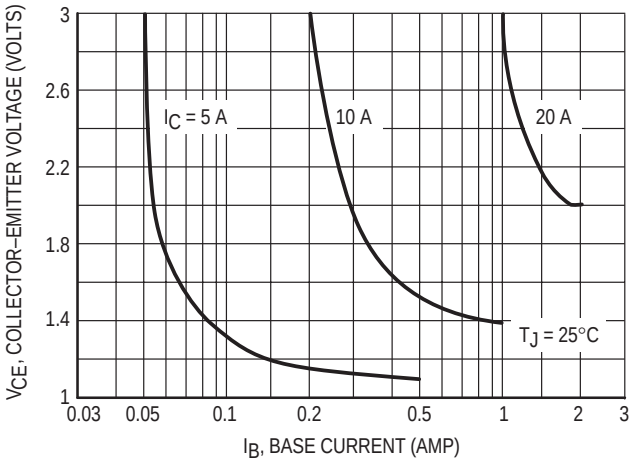


Figure 2. Collector Saturation Region

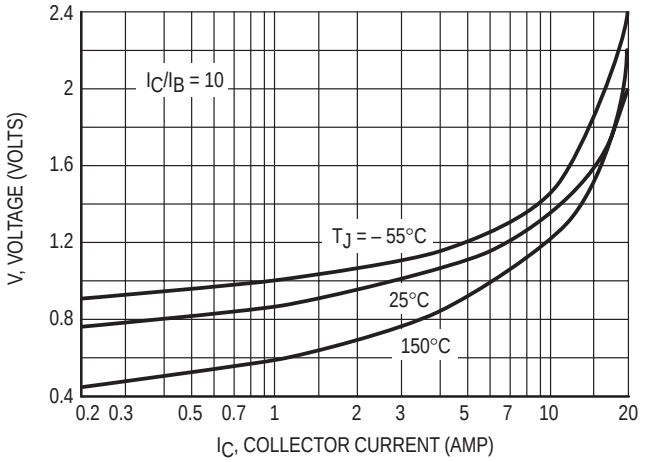


Figure 3. Collector–Emitter Saturation Voltage

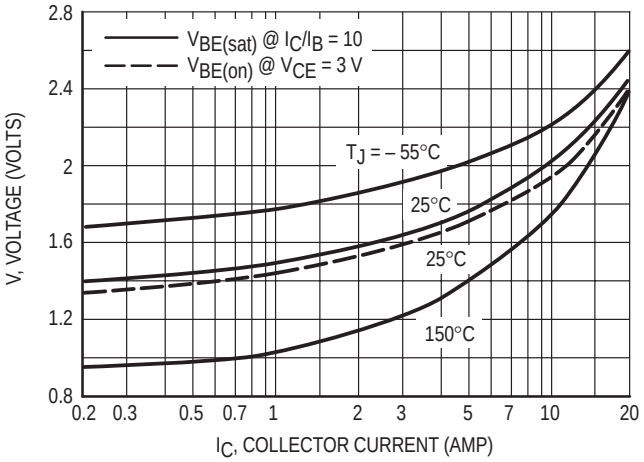


Figure 4. Base-Emitter Voltage

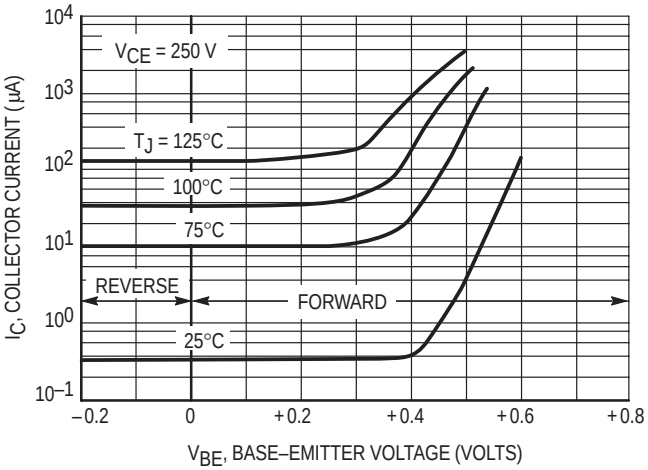


Figure 5. Collector Cutoff Region

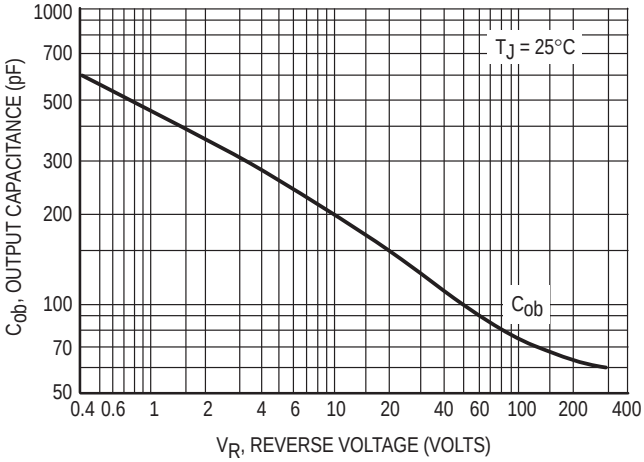
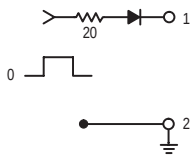
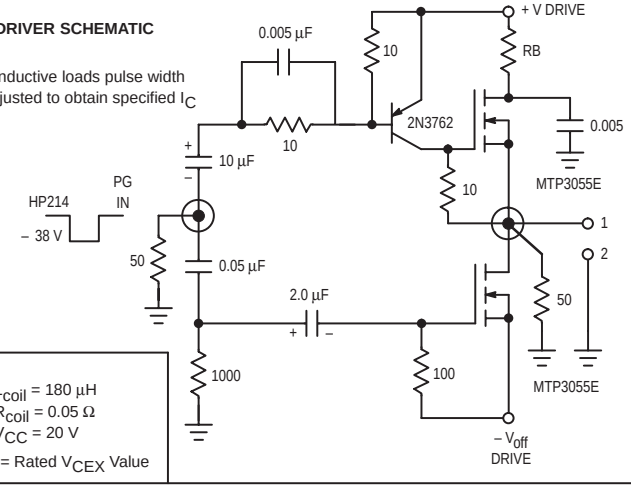
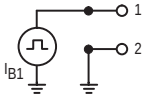
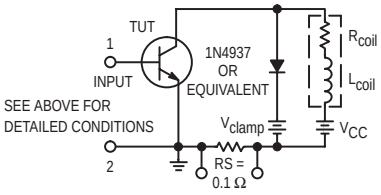
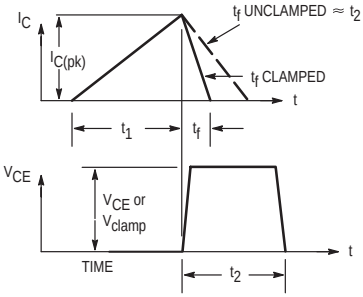
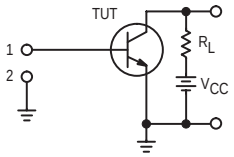


Figure 6. Output Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	**DRIVER SCHEMATIC** For inductive loads pulse width is adjusted to obtain specified I_C 	 I_{B1} adjusted to obtain the forced h_{FE} desired **TURN–OFF TIME** Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 10 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 25 Ω Pulse Width = 25 µs
TEST CIRCUITS	**INDUCTIVE TEST CIRCUIT** 	**OUTPUT WAVEFORMS**  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	**RESISTIVE TEST CIRCUIT** 

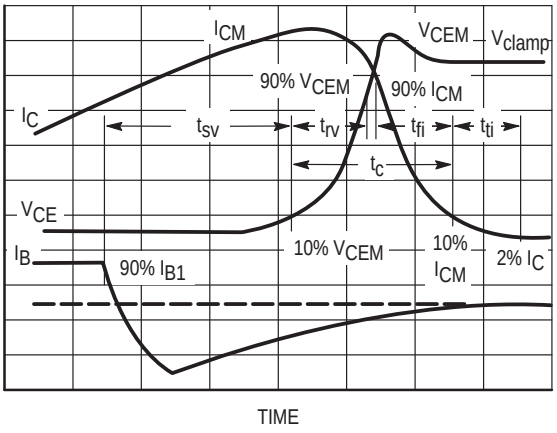


Figure 7. Inductive Switching Measurements

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

TYPICAL CHARACTERISTICS

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222.

$$P_{SWT} = 1/2\ V_{CC}\ I_C\ (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 7. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

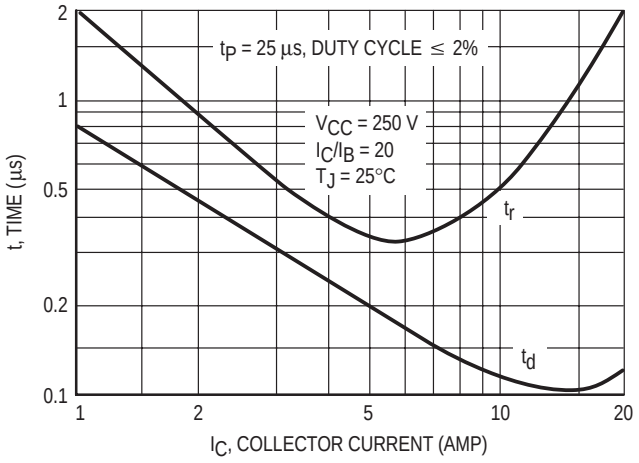


Figure 8. Turn-On Time

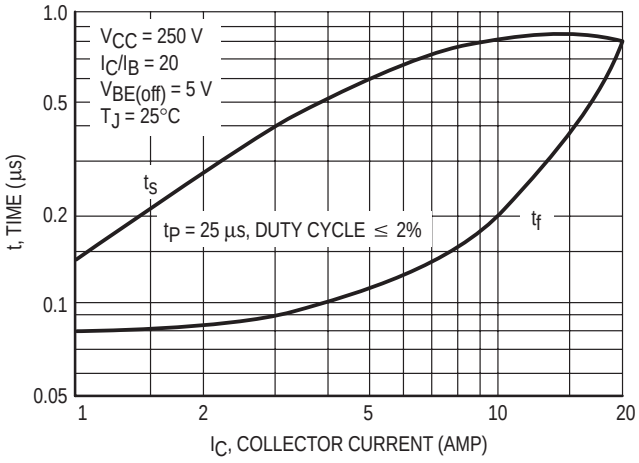


Figure 9. Turn-Off Time

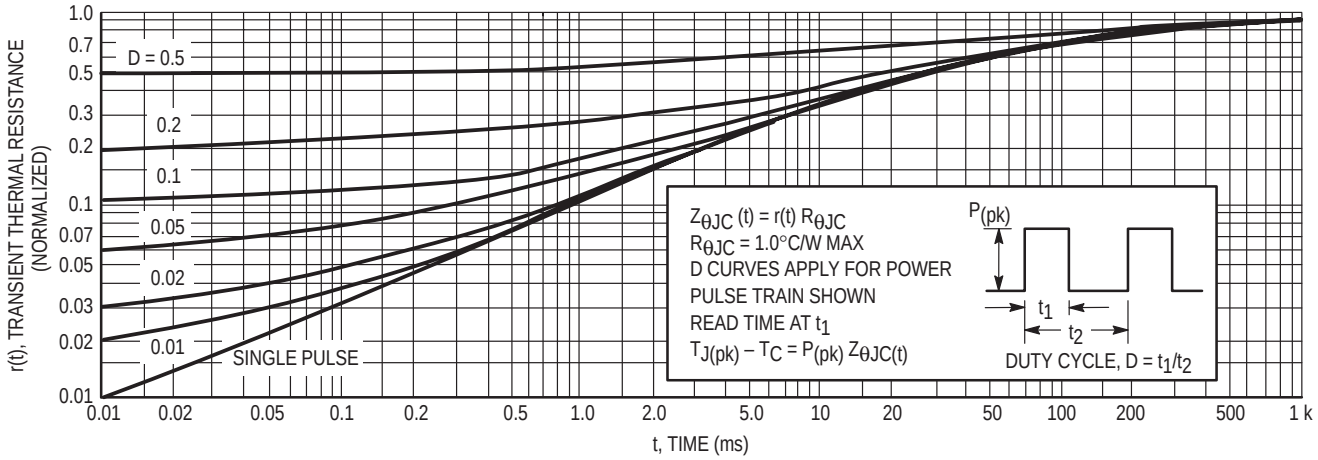


Figure 10. Thermal Response

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

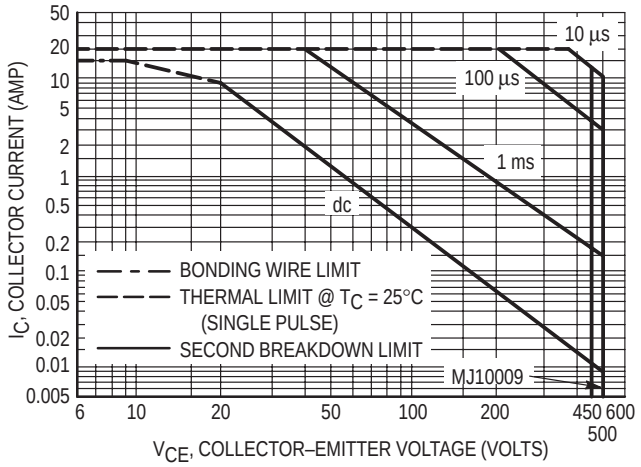


Figure 11. Forward Bias Safe Operating Area

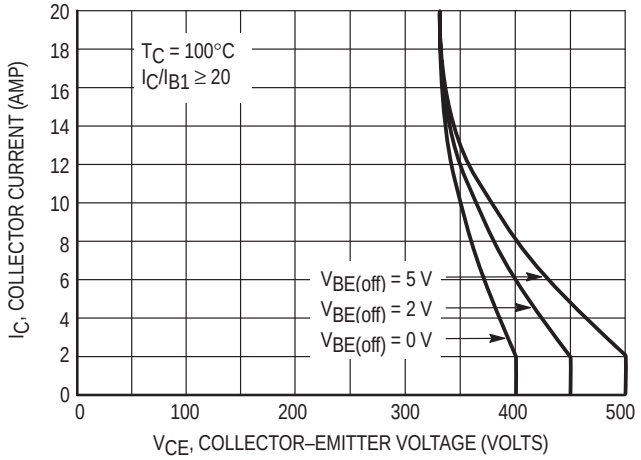


Figure 12. Reverse Bias Switching Safe Operating Area (MJ10009)

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage–current condition that can be sustained during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics. See Table 1 for circuit conditions.

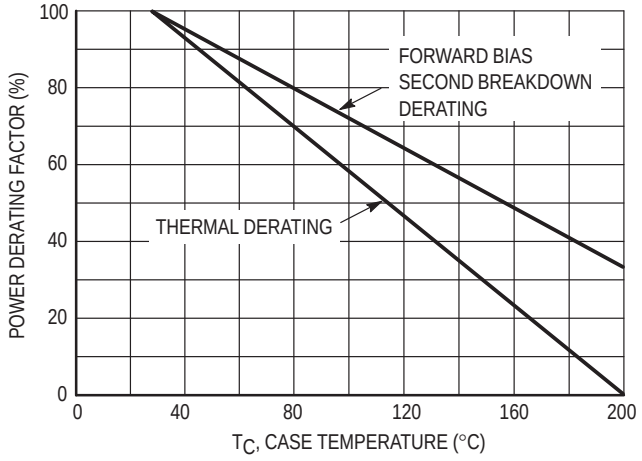


Figure 13. Power Derating

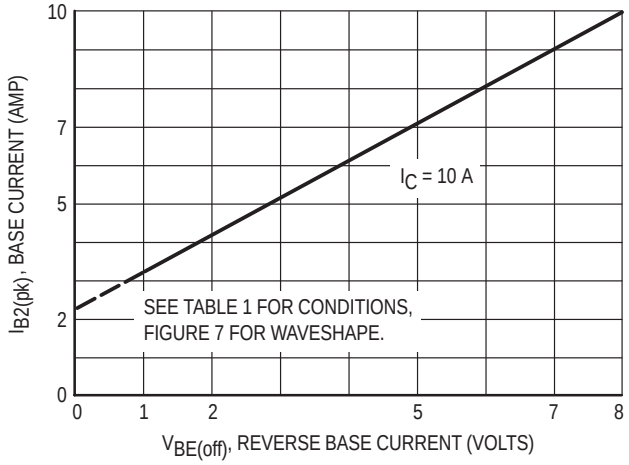


Figure 14. Reverse Base Current versus $V_{BE(off)}$ with No External Base Resistance

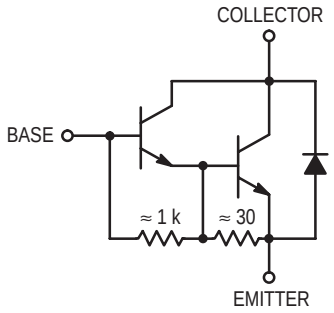
MJ10012
MJH10012

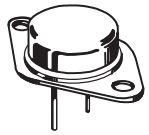
NPN Silicon Power Darlington Transistor

10 AMPERE
POWER TRANSISTORS
DARLINGTON NPN
SILICON
400 VOLTS
175 AND 118 WATTS

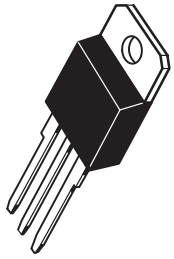
The MJ10012 and MJH10012 are high–voltage, high–current Darlington transistors designed for automotive ignition, switching regulator and motor control applications.

- Collector–Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 400 Vdc (Min)
- 175 Watts Capability at 50 Volts
- Automotive Functional Tests





CASE 1–07
TO–204AA
(TO–3)
MJ10012



CASE 340D–01
TO–218 TYPE
MJH10012

MAXIMUM RATINGS

Rating	Symbol	MJ10012	MJH10012	Unit
Collector–Emitter Voltage	V_{CEO}	400		Vdc
Collector–Emitter Voltage (R_{BE} = 27 Ω)	V_{CER}	550		Vdc
Collector–Base Voltage	V_{CBO}	600		Vdc
Emitter–Base Voltage	V_{EBO}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C	10 15		Adc
Base Current	I_B	2.0		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	 175 100 1.0	 118 47.5 1.05	 Watts Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	0.95	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	275	°C

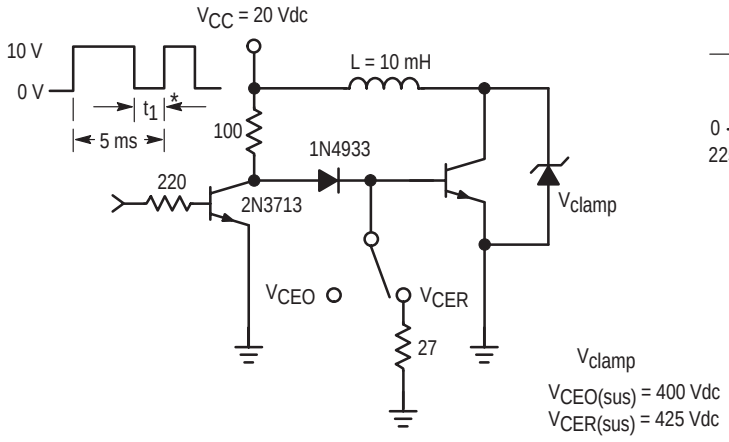
(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector–Emitter Sustaining Voltage (Figure 1) (I_C = 200 mAdc, I_B = 0, V_{clamp} = Rated V_{CEO})	$V_{CEO(sus)}$	400	—	—	Vdc
Collector–Emitter Sustaining Voltage (Figure 1) (I_C = 200 mAdc, R_{BE} = 27 Ohms, V_{clamp} = Rated V_{CER})	$V_{CER(sus)}$	425	—	—	Vdc
Collector Cutoff Current (Rated V_{CER}, R_{BE} = 27 Ohms)	I_{CER}	—	—	1.0	mAdc
Collector Cutoff Current (Rated V_{CBO}, I_E = 0)	I_{CBO}	—	—	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	40	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 6 0 Vdc) (I_C = 6.0 Adc, V_{CE} = 6.0 Vdc) (I_C = 10 Adc, V_{CE} = 6.0 Vdc)	h_{FE}	 300 100 20	 550 350 150	 — 2000 —	—
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 0.6 Adc) (I_C = 6.0 Adc, I_B = 0.6 Adc) (I_C = 10 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	 — — —	 — — —	 1 5 2.0 2.5	Vdc
Base Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 0.6 Adc) (I_C = 10 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	 — —	 — —	 2.5 3.0	Vdc
Base Emitter On Voltage (I_C = 10 Adc, V_{CE} = 6.0 Vdc)	$V_{BE(on)}$	—	—	2.8	Vdc
Diode Forward Voltage (I_F = 10 Adc)	V_f	—	2.0	3.5	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	—	165	350	pF
SWITCHING CHARACTERISTICS					
Storage Time	(V_{CC} = 12 Vdc, I_C = 6.0 Adc, I_{B1} = I_{B2} = 0.3 Adc) Figure 2	t_s	—	7 5	15	µs
Fall Time		t_f	—	5.2	15	µs
FUNCTIONAL TESTS					
Second Breakdown Collector Current with Base–Forward Biased	$I_{S/B}$	See Figure 10			—
Pulsed Energy Test (See Figure 12)	$I_C2L/2$	—	—	180	mJ

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2%.



* Adjust t_1 such that I_C reaches 200 mA at V_{CE} = V_{clamp}

Figure 1. Sustaining Voltage Test Circuit

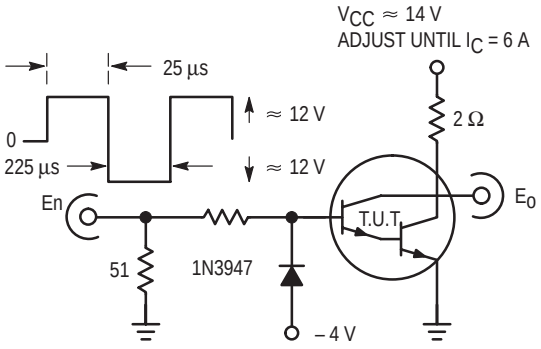


Figure 2. Switching Times Test Circuit

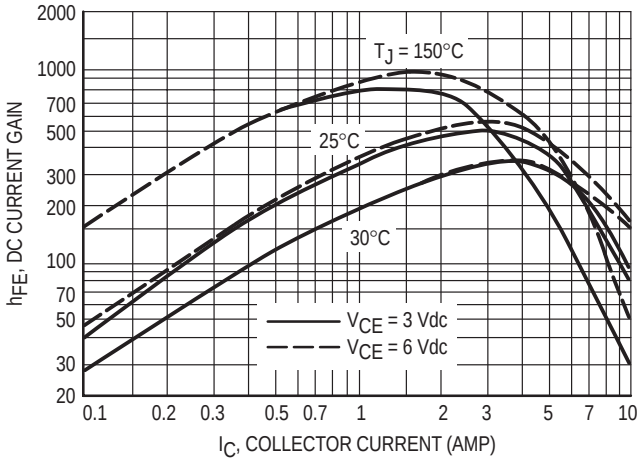


Figure 3. DC Current Gain

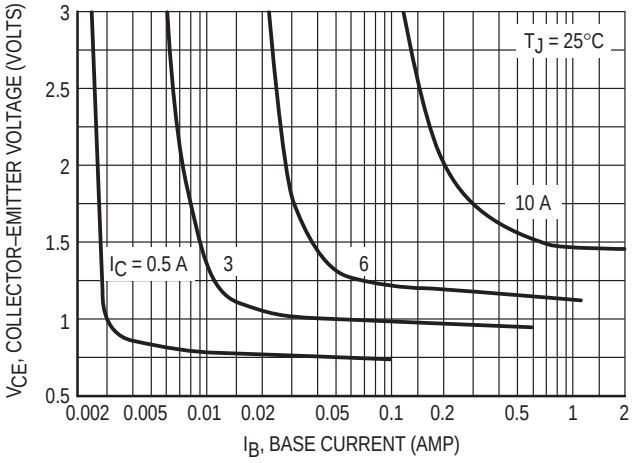


Figure 4. Collector Saturation Region

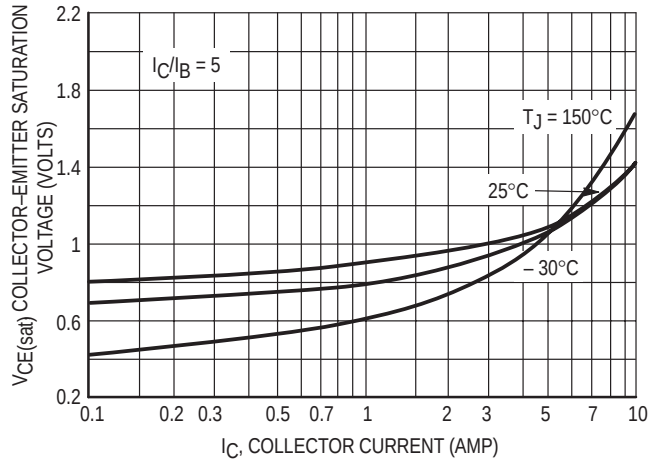


Figure 5. Collector–Emitter Saturation Voltage

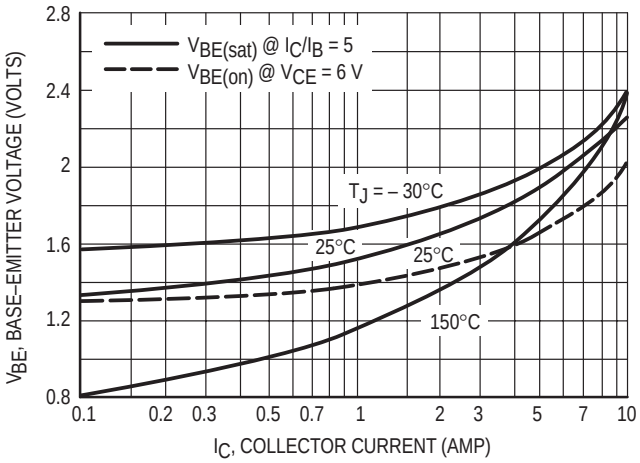


Figure 6. Base–Emitter Voltage

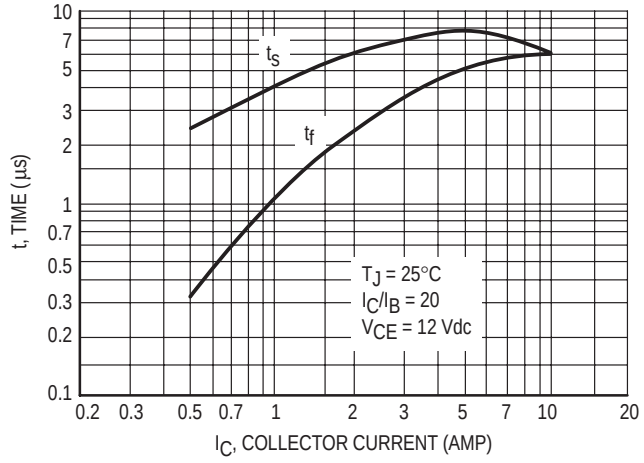


Figure 7. Turn–Off Switching Time

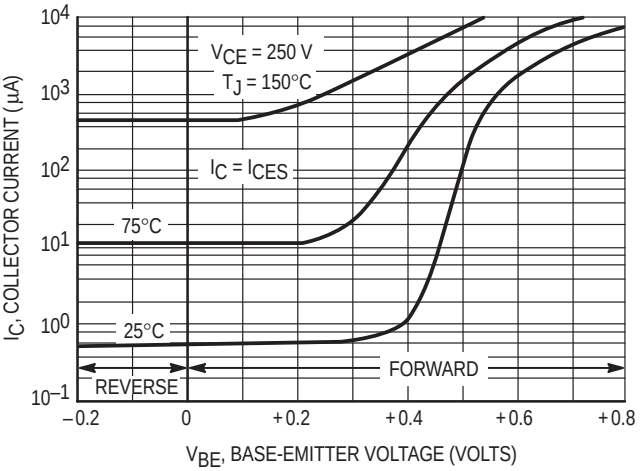


Figure 8. Collector Cutoff Region

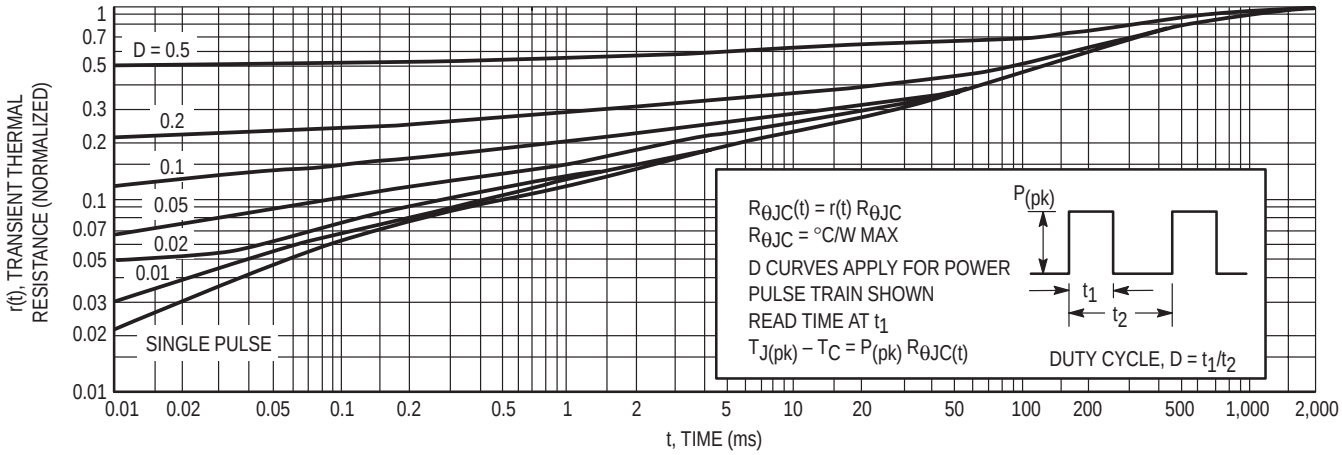


Figure 9. Thermal Response

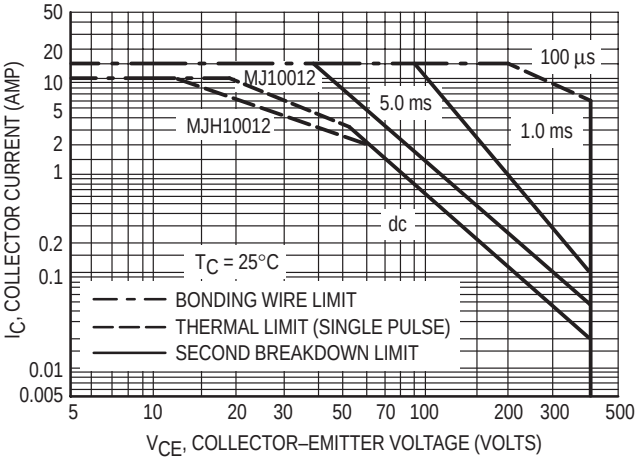


Figure 10. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25°C$, $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

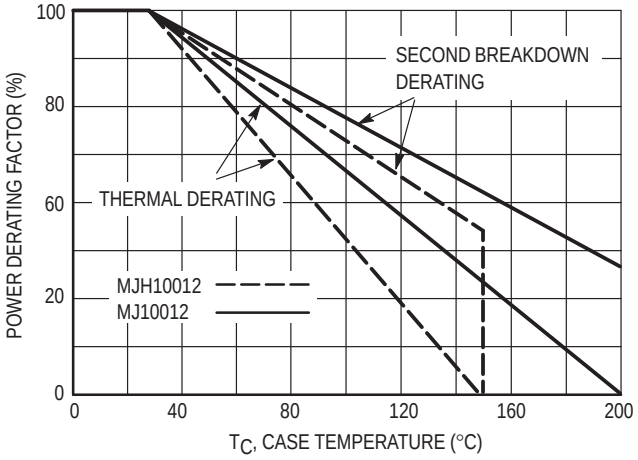
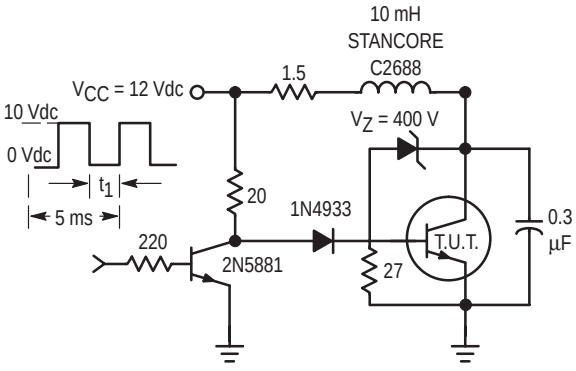


Figure 11. Power Derating



t_1 to be selected such that I_C reaches 6 Adc before switch-off.

NOTE: "Usage Test," Figure 12 specifies energy handling capabilities in an automotive ignition circuit.

Figure 12. Usage Test Circuit

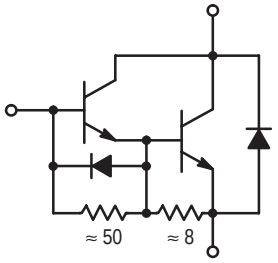
MJ10015
MJ10016

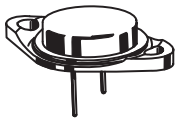
SWITCHMODE Series NPN Silicon Power Darlington Transistors with Base-Emitter Speedup Diode

50 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS
400 AND 500 VOLTS
250 WATTS

The MJ10015 and MJ10016 Darlington transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated switchmode applications such as:

- Switching Regulators
- Motor Controls
- Inverters
- Solenoid and Relay Drivers
- Fast Turn–Off Times
  - 1.0 µs (max) Inductive Crossover Time — 20 Amps
  - 2.5 µs (max) inductive Storage Time — 20 Amps
- Operating Temperature Range –65 to +200°C
- Performance Specified for
  - Reversed Biased SOA with Inductive Load
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents





CASE 197–05
TO–204AE TYPE
(TO–3 TYPE)

MAXIMUM RATINGS

Rating	Symbol	MJ10015	MJ10016	Unit
Collector–Emitter Voltage	V_{CEO}	400	500	Vdc
Collector–Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	50 75		Adc
Base Current — Continous — Peak (1)	I_B I_{BM}	10 15		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	MJ10015 MJ10016	$V_{CEO(sus)}$	 400 500	 — —	 — —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	—	—	0.25	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)		I_{EBO}	—	—	350	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 7			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 8			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 20 Adc, V_{CE} = 5.0 Vdc) (I_C = 40 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	 25 10	 — —	 — —	—
Collector–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc) (I_C = 50 Adc, I_B = 10 Adc)		$V_{CE(sat)}$	 — —	 — —	 2.2 5.0	Vdc
Base–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	—	—	2.75	Vdc
Diode Forward Voltage (2) (I_F = 20 Adc)		V_f	—	2.5	5.0	Vdc
DYNAMIC CHARACTERISTIC						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}	—	—	750	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 20 A, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5 Vdc, t_p = 25 µs Duty Cycle ≤ 2%).	t_d	—	0.14	0.3	µs
Rise Time		t_r	—	0.3	1.0	µs
Storage Time		t_s	—	0.8	2.5	µs
Fall Time		t_f	—	0.3	1.0	µs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 20 A(pk), V_{clamp} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc)	t_{sv}	—	1.0	2.5	µs
Crossover Time		t_c	—	0.36	1.0	µs

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤ 2%.

(2) The internal Collector–to–Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

TYPICAL CHARACTERISTICS

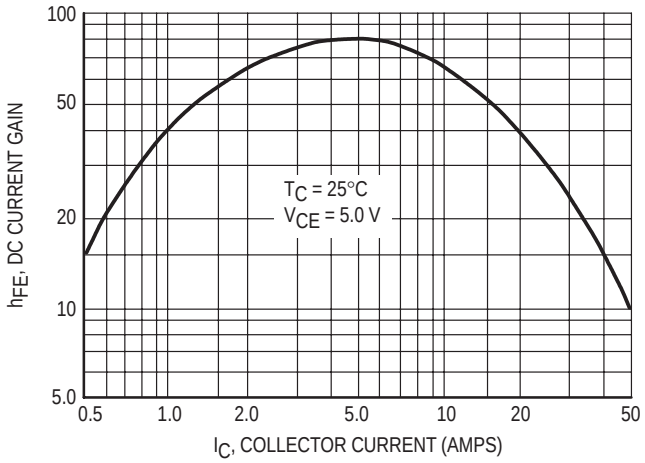


Figure 1. DC Current Gain

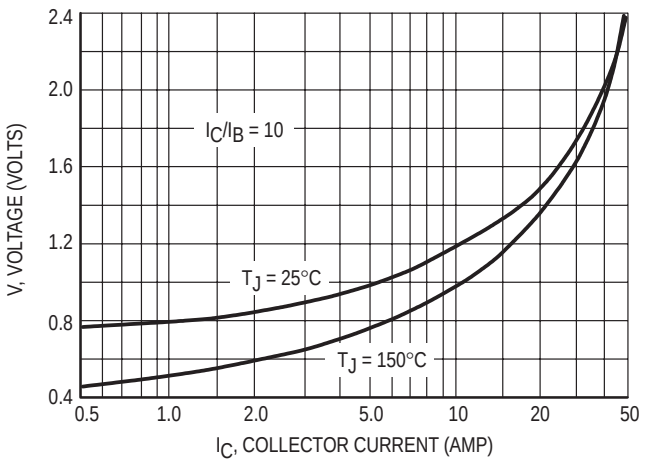


Figure 2. Collector–Emitter Saturation Voltage

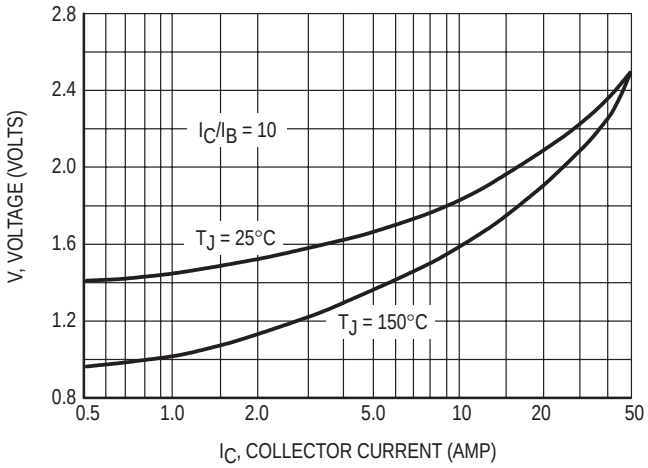


Figure 3. Base–Emitter Saturation Voltage

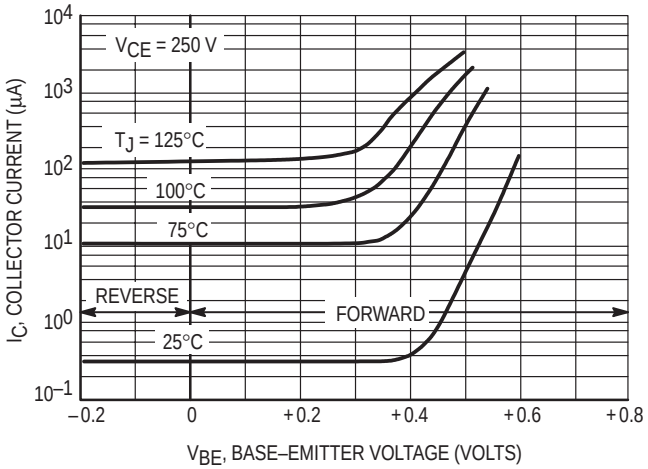


Figure 4. Collector Cutoff Region

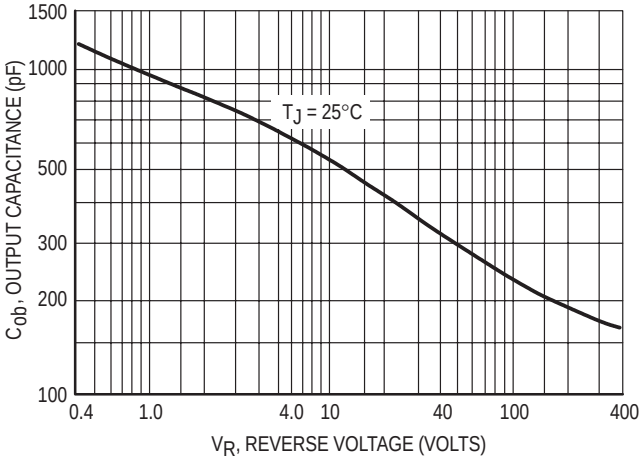
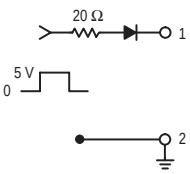
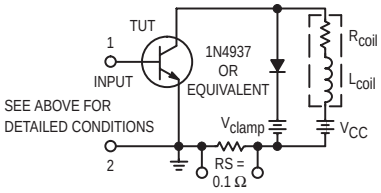
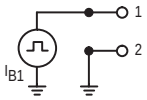
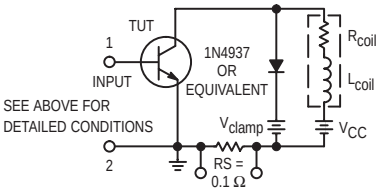
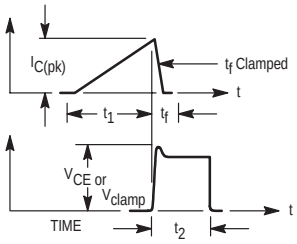
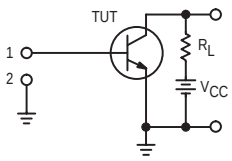


Figure 5. Output Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	V_{CEX} AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	INDUCTIVE TEST CIRCUIT 	TURN–ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN–OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 10 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V	V_{CC} = 250 V R_L = 12.5 Ω Pulse Width = 25 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT 	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

* Adjust –V such that $V_{BE(off)}$ = 5 V except as required for RBSOA (Figure 8).

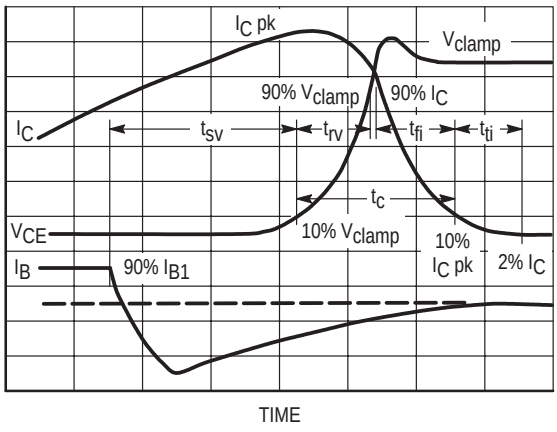


Figure 6. Inductive Switching Measurements

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2\ V_{CC}\ I_C\ (t_c)\ f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed.

The Safe Operating Area figures shown in Figures 7 and 8 are specified ratings for these devices under the test conditions shown.

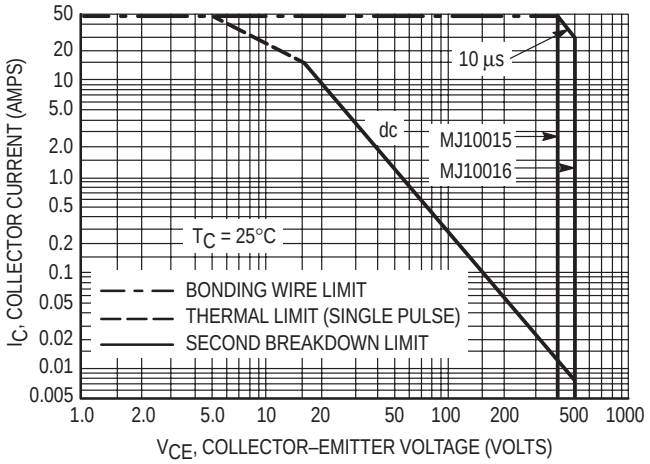


Figure 7. Forward Bias Safe Operating Area

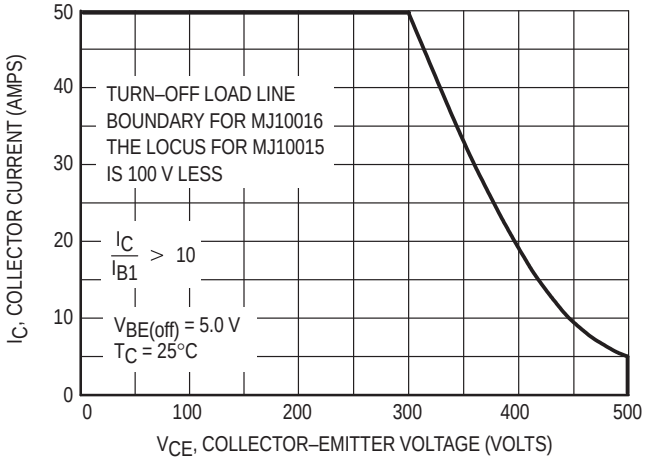


Figure 8. Reverse Bias Switching Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 8 gives the complete RBSOA characteristics.

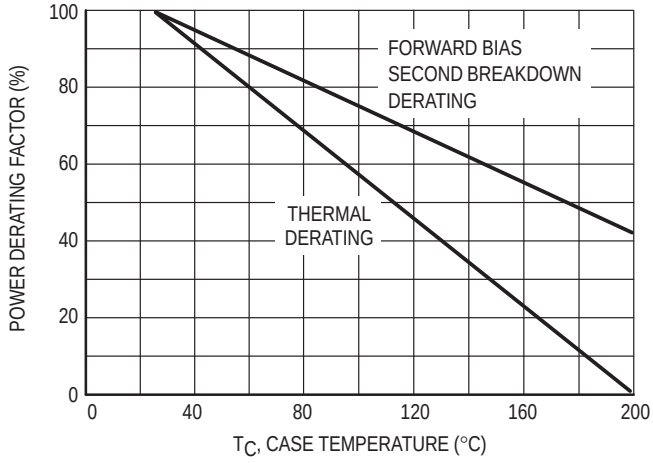


Figure 9. Power Derating

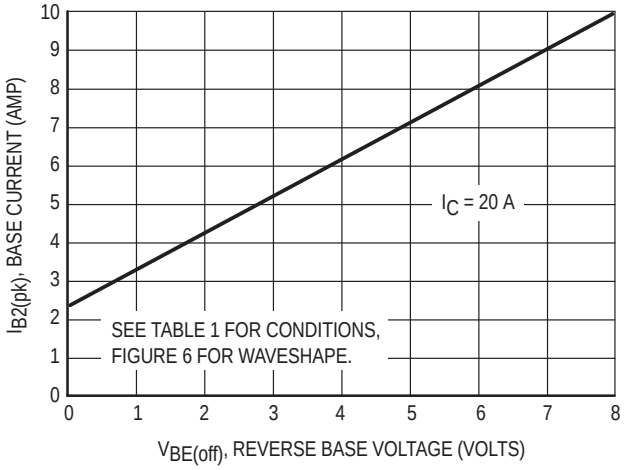


Figure 10. Typical Reverse Base Current versus $V_{BE(off)}$ With No External Base Resistance

MJ10020
MJ10021

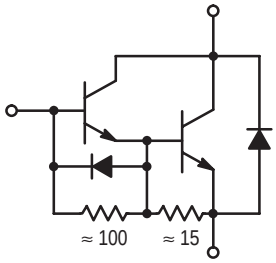
Designer's™ Data Sheet

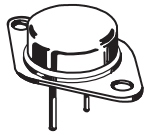
SWITCHMODE Series NPN Silicon Power Darlington Transistors with Base-Emitter Speedup Diode

60 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS
200 AND 250 VOLTS
250 WATTS

The MJ10020 and MJ10021 Darlington transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn–Off Times
  - 150 ns Inductive Fall Time at 25°C (Typ)
  - 750 ns Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range –65 to +200°C
- 100°C Performance Specified for:
  - Reversed Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents





CASE 197A–05
TO–204AE (TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ10020	MJ10021	Unit
Collector–Emitter Voltage	V_{CEO}	200	250	Vdc
Collector–Emitter Voltage	V_{CEV}	300	350	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	60 100		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	20 30		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	MJ10020 MJ10021	$V_{CEO(sus)}$	200 250	— —	— —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEV}	 — —	 — —	 0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = 0)		I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$		See Figure 13		
Clamped Inductive SOA with Base Reverse Biased		RBSOA		See Figure 14		
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 15 Adc, V_{CE} = 5.0 V)		h_{FE}	75	—	1000	—
Collector–Emitter Saturation Voltage (I_C = 30 Adc, I_B = 1.2 Adc) (I_C = 60 Adc, I_B = 4.0 Adc) (I_C = 30 Adc, I_B = 1.2 Adc, T_C = 100°C)		$V_{CE(sat)}$	 — — —	 — — —	 2.2 4.0 2.4	Vdc
Base–Emitter Saturation Voltage (I_C = 30 Adc, I_B = 1.2 Adc) (I_C = 30 Adc, I_B = 1.2 Adc, T_C = 100°C)		$V_{BE(sat)}$	 — —	 — —	 3.0 3.5	Vdc
Diode Forward Voltage (I_F = 30 Adc)		V_f	—	2.5	5.0	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	175	—	700	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 175 Vdc, I_C = 30 A, I_{B1} = Adc, $V_{BE(off)}$ = 5.0 V, t_p = 25 µs Duty Cycle ≤ 2.0%).	t_d	—	0.02	0.2	µs
Rise Time		t_r	—	0.30	1.0	µs
Storage Time		t_s	—	1.0	3.5	µs
Fall Time		t_f	—	0.07	0.5	µs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_{CM} = 30 A(pk), V_{CEM} = 200 V, I_{B1} = 1.2 A, $V_{BE(off)}$ = 5 V, T_C = 100°C)	t_{sv}	—	1.2	3.5	µs
Crossover Time		t_c	—	0.45	2.0	µs
Storage Time	(I_{CM} = 30 A(pk), V_{CEM} = 200 V, I_{B1} = 1.2 A, $V_{BE(off)}$ = 5 V, T_C = 25°C)	t_{sv}	—	0.75	—	µs
Crossover Time		t_c	—	0.25	—	µs
Fall Time		t_{fi}	—	0.15	—	µs

(1) Pulse Test: PW = 300 µs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

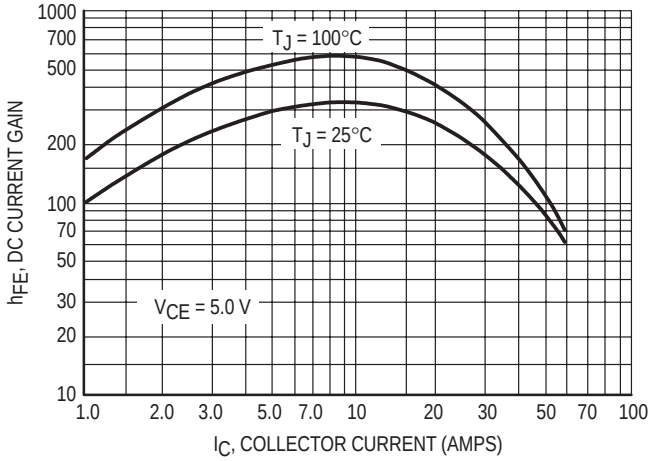


Figure 1. DC Current Gain

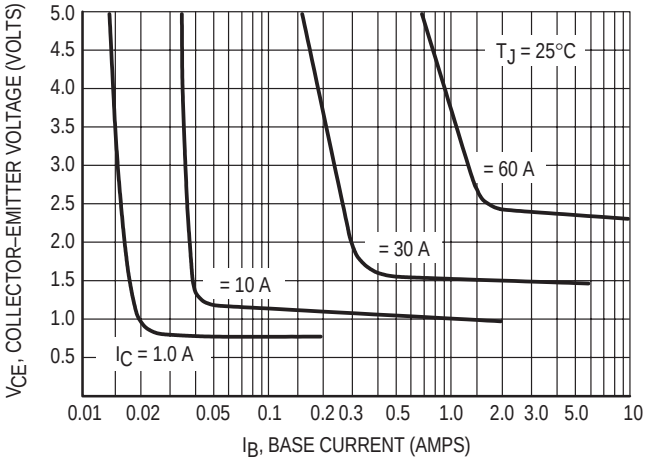


Figure 2. Collector Saturation Region

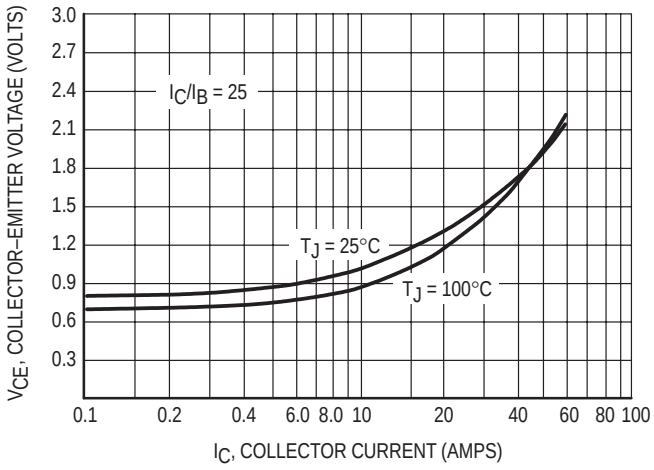


Figure 3. Collector–Emitter Saturation Voltage

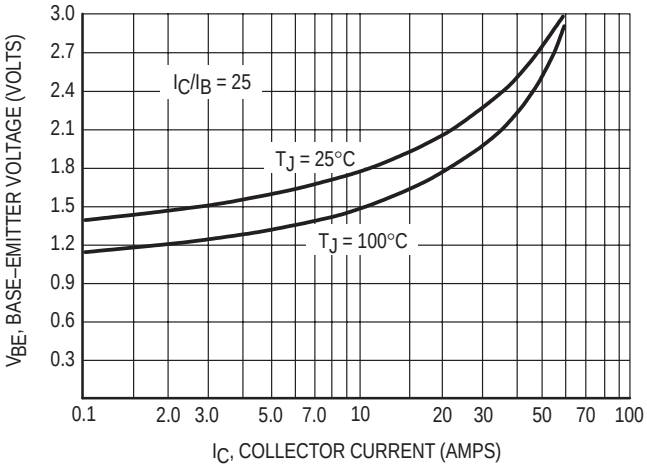


Figure 4. Base–Emitter Voltage

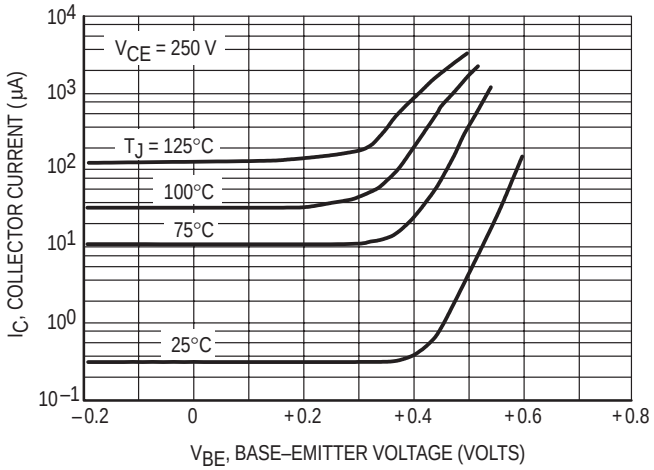


Figure 5. Collector Cutoff Region

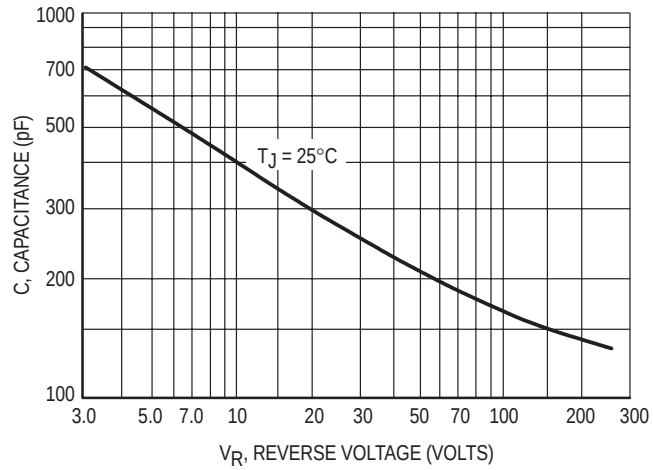
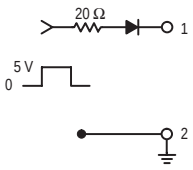
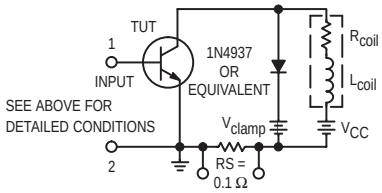
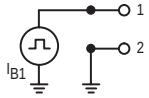
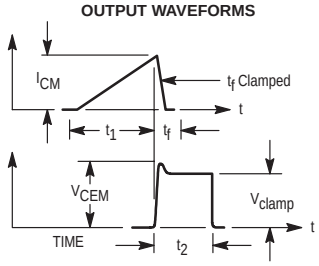
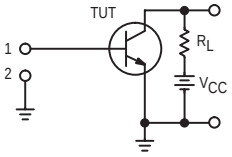


Figure 6. Output Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 PW Varied to Attain I_C = 100 mA	INDUCTIVE TEST CIRCUIT 	TURN–ON TIME  I_{B1} adjusted to obtain the forced h_{FE} desired TURN–OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 10 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω $V_{clamp} = V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V	V_{CC} = 175 V R_L = 5.6 Ω Pulse Width = 25 μs
TEST CIRCUITS	OUTPUT WAVEFORMS 	t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT 

* Adjust –V such that $V_{BE(off)}$ = 5 V except as required for RBSOA (Figure 14).

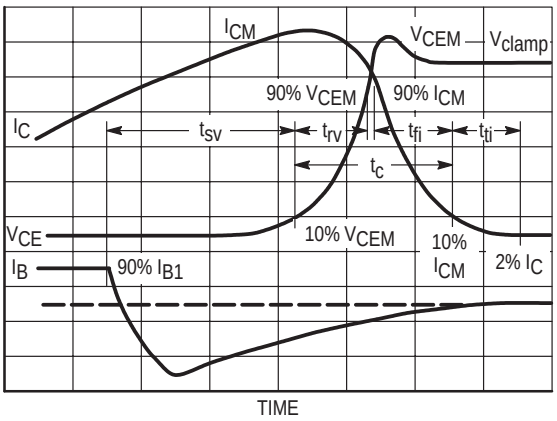


Figure 7. Inductive Switching Measurements

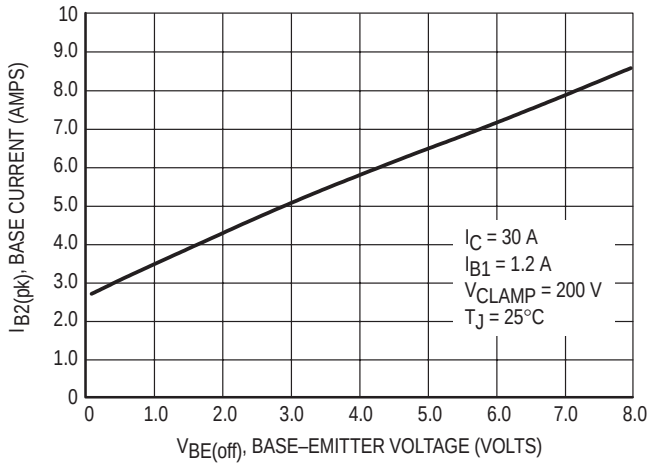


Figure 8. Typical Peak Reverse Base Current

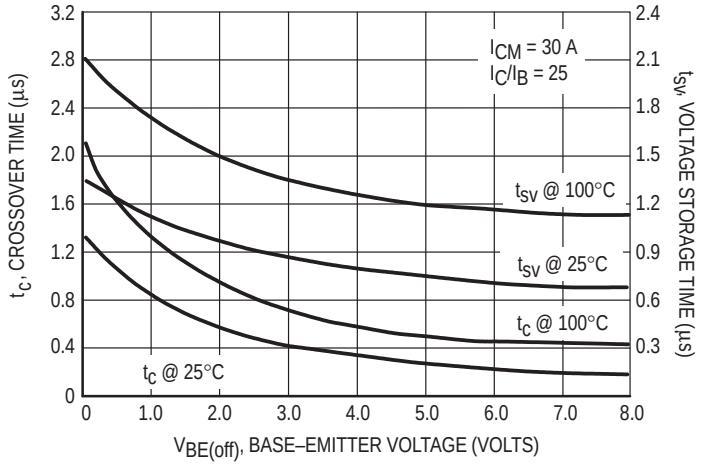


Figure 9. Typical Inductive Switching Times

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
t_{rv} = Voltage Rise Time, 10–90% V_{CEM}
t_{fi} = Current Fall Time, 90–10% I_{CM}
t_{ti} = Current Tail, 10–2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222A:

$$P_{SWT} = 1/2\ V_{CC}\ I_C\ (t_c)\ f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING

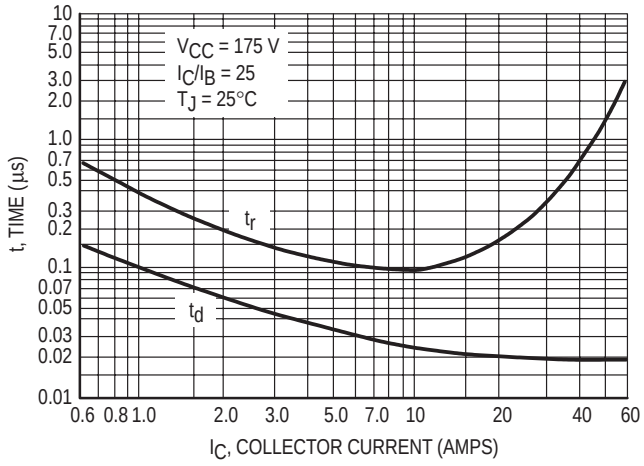


Figure 10. Typical Turn–On Switching Times

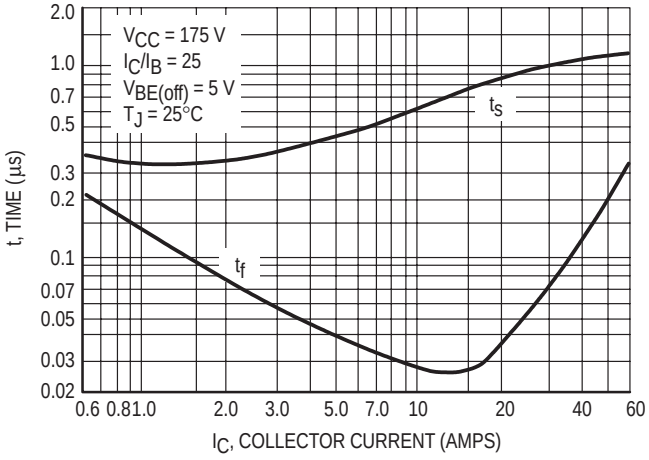


Figure 11. Typical Turn–Off Switching Times

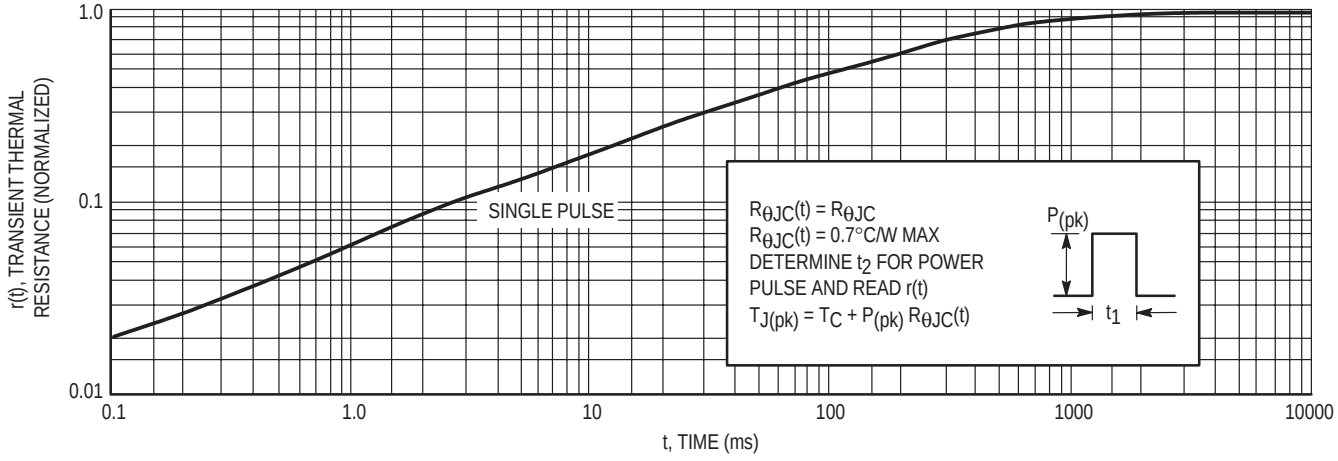


Figure 12. Thermal Response

The Safe Operating Area figures shown in Figures 13 and are specified for these devices under the test conditions shown.

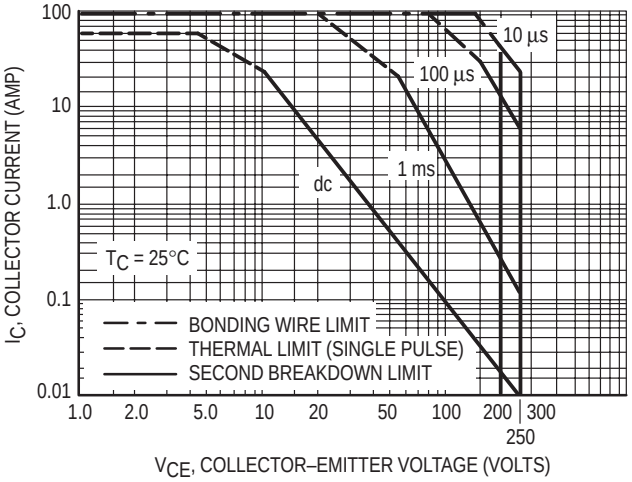


Figure 13. Maximum Forward Bias Safe Operating Area

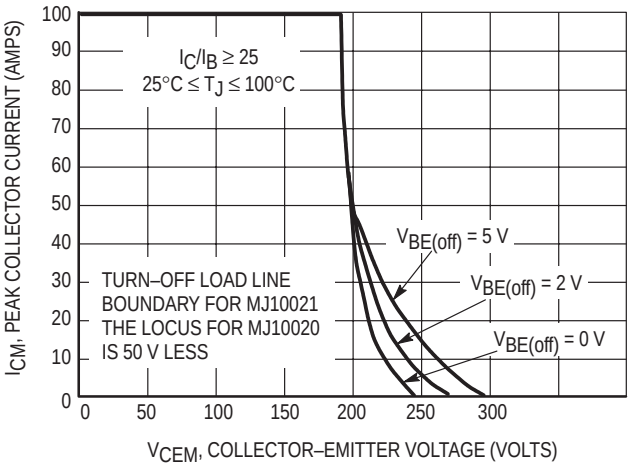


Figure 14. Maximum RBSOA, Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For Inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

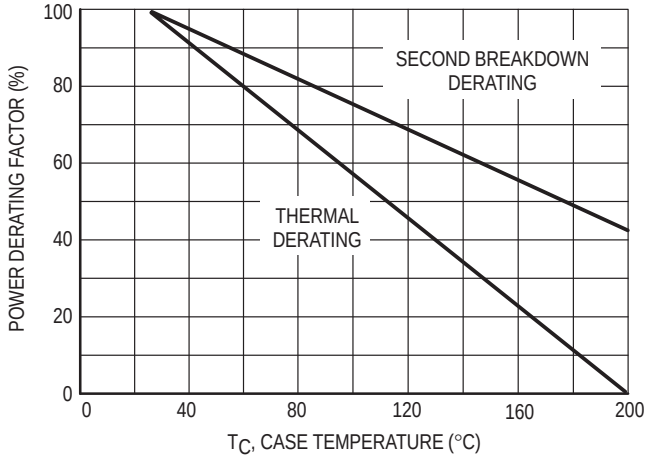


Figure 15. Power Derating

MJ10022
MJ10023

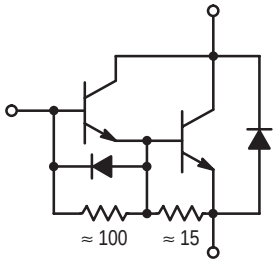
Designer's™ Data Sheet

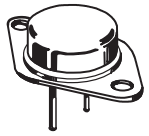
SWITCHMODE Series NPN Silicon Power Darlington Transistors with Base-Emitter Speedup Diode

40 AMPERE
NPN SILICON
POWER DARLINGTON
TRANSISTORS
350 AND 400 VOLTS
250 WATTS

The MJ10022 and MJ10023 Darlington transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn–Off Times
  - 150 ns Inductive Fall Time @ 25°C (Typ)
  - 300 ns Inductive Storage Time @ 25°C (Typ)
- Operating Temperature Range – 65 to + 200°C
- 100°C Performance Specified for:
  - Reversed Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents





CASE 197A–05
TO–204AE (TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ10022	MJ10023	Unit
Collector–Emitter Voltage	V_{CEO}	350	400	Vdc
Collector–Emitter Voltage	V_{CEV}	450	600	Vdc
Emitter Base Voltage	V_{EB}	80		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	40 80		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	20 40		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	MJ10022 MJ10023	$V_{CEO(sus)}$	350 400	— —	— —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEV}	 — —	 — —	 0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 V, I_C = O)		I_{EBO}	—	—	175	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$		See Figure 13		
Clamped Inductive SOA with Base Reverse Biased		RBSOA		See Figure 14		
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 V)		h_{FE}	50	—	600	—
Collector–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc) (I_C = 40 Adc, I_B = 5.0 Adc) (I_C = 20 Adc, I_B = 10 Adc, T_C = 100°C)		$V_{CE(sat)}$	 — — —	 — — —	 2.2 5.0 2.5	Vdc
Base–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.2 Adc) (I_C = 20 Adc, I_B = 1.2 Adc, T_C = 100°C)		$V_{BE(sat)}$	 — —	 — —	 2.5 2.5	Vdc
Diode Forward Voltage (I_F = 20 Adc)		V_f	—	2.5	5.0	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	150	—	600	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 20 A, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5.0 V, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	—	0.03	0.2	μs
Rise Time		t_r	—	0.4	1.2	μs
Storage Time		t_s	—	0.9	2.5	μs
Fall Time		t_f	—	0.3	0.9	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_{CM} = 20 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 V, T_C = 100°C)	t_{sv}	—	1.9	4.4	μs
Crossover Time		t_c	—	0.6	2.0	μs
Fall Time		t_{fi}	—	0.3	—	μs
Storage Time	(I_{CM} = 20 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 V, T_C = 25°C)	t_{sv}	—	1.0	—	μs
Crossover Time		t_c	—	0.3	—	μs
Fall Time		t_{fi}	—	0.15	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

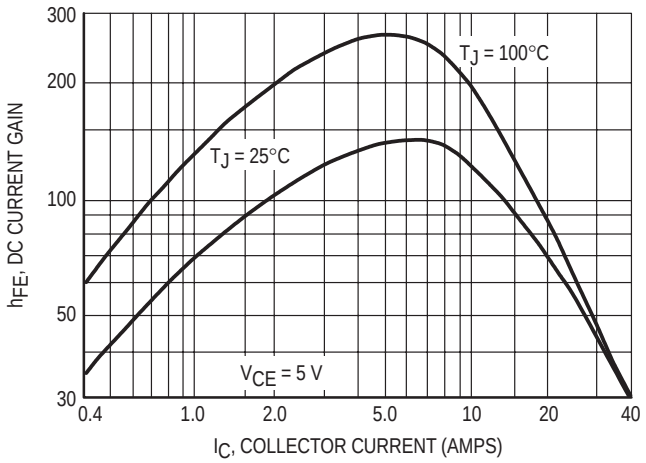


Figure 1. DC Current Gain

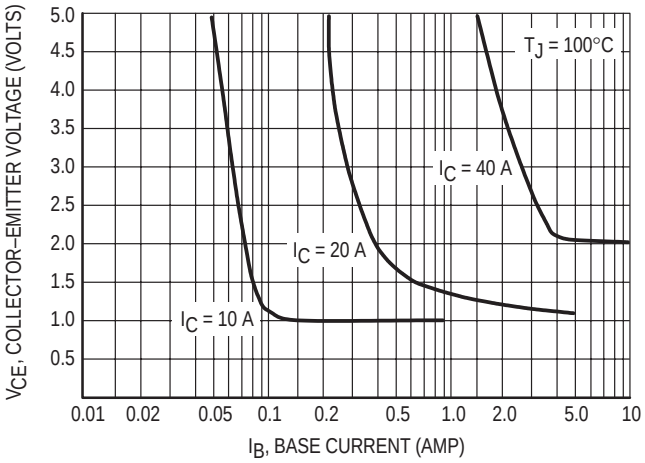


Figure 2. Collector Saturation Region

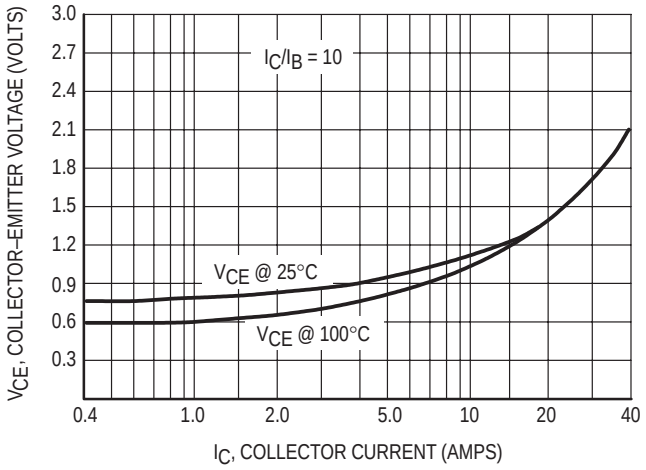


Figure 3. Collector–Emitter Saturation Voltage

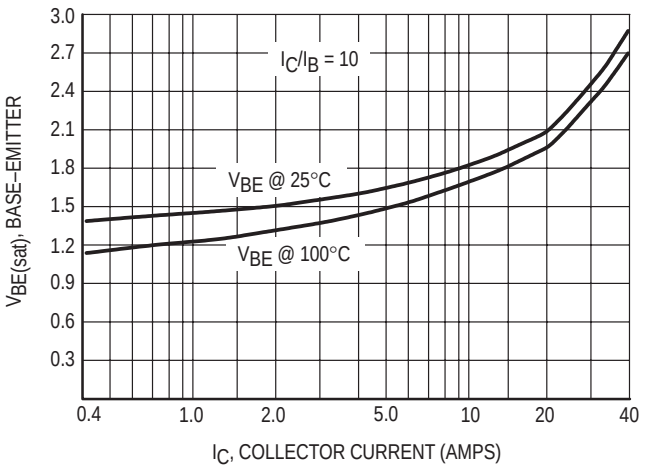


Figure 4. Base–Emitter Saturation Voltage

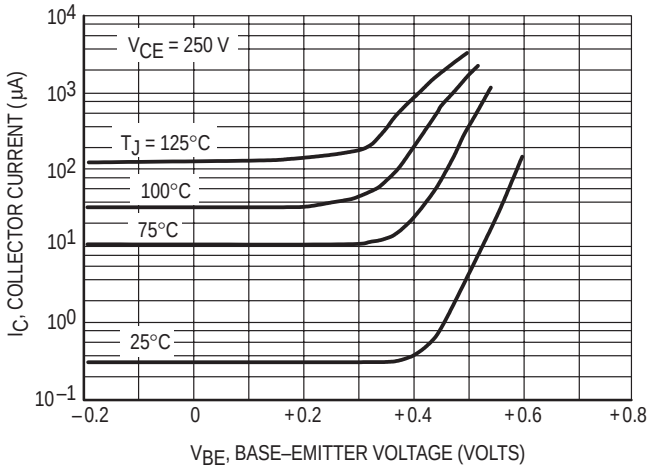


Figure 5. Collector Cutoff Region

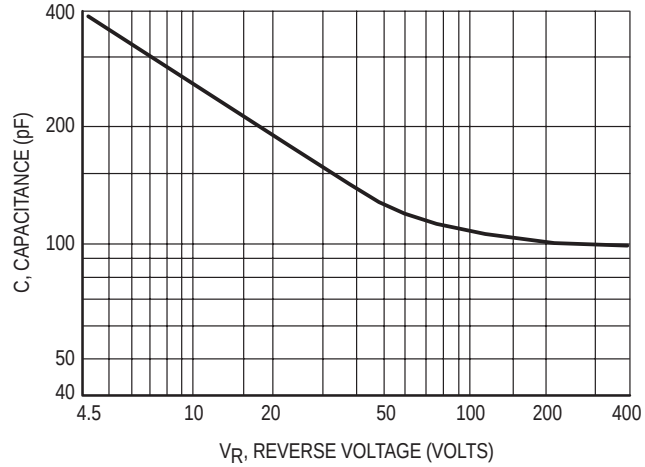


Figure 6. C_{ob}, Output Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	20 Ω, 5 V, 0, 1, 2 PW Varied to Attain I_C = 100 mA	INDUCTIVE TEST CIRCUIT TUT, 1N4937 OR EQUIVALENT, R_{coil}, L_{coil}, V_{clamp}, V_{CC}, RS = 0.1 Ω INPUT SEE ABOVE FOR DETAILED CONDITIONS	TURN–ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN–OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 10 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V	V_{CC} = 250 V R_L = 12.5 Ω Pulse Width = 25 μs
TEST CIRCUITS	OUTPUT WAVEFORMS I_{CM}, t_f Clamped, t, t_1, t_f, V_{CEM}, V_{clamp}, TIME, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent		RESISTIVE TEST CIRCUIT TUT, R_L, V_{CC}, 1, 2

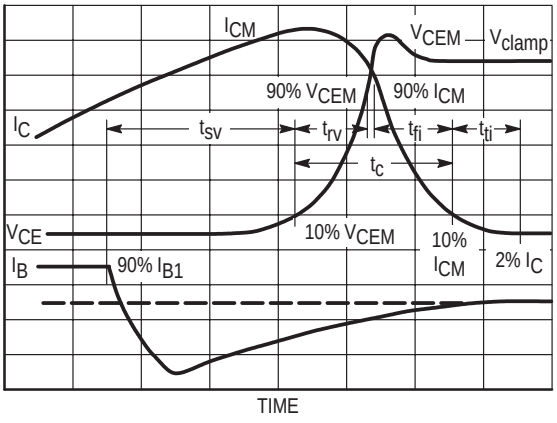


Figure 7. Inductive Switching Measurements

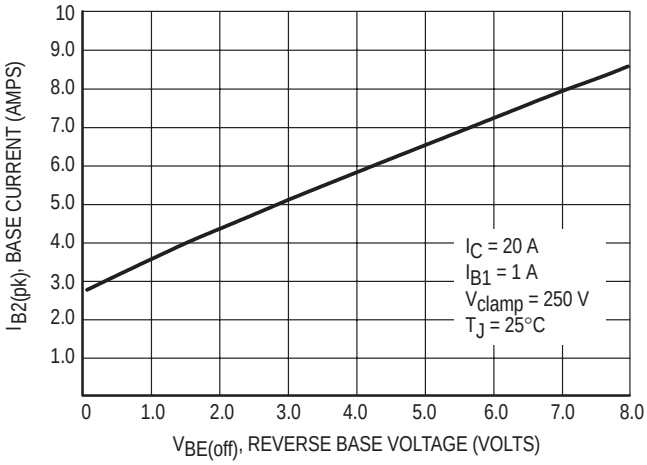


Figure 8. Typical Peak Reverse Base Current

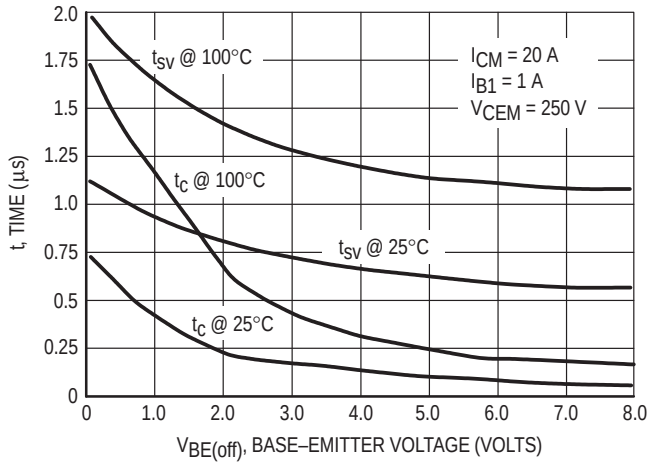


Figure 9. Typical Inductive Switching Times

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
t_{rv} = Voltage Rise Time, 10–90% V_{CEM}
t_{fi} = Current Fall Time, 90–10% I_{CM}
t_{ti} = Current Tail, 10–2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222A:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user orinented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING

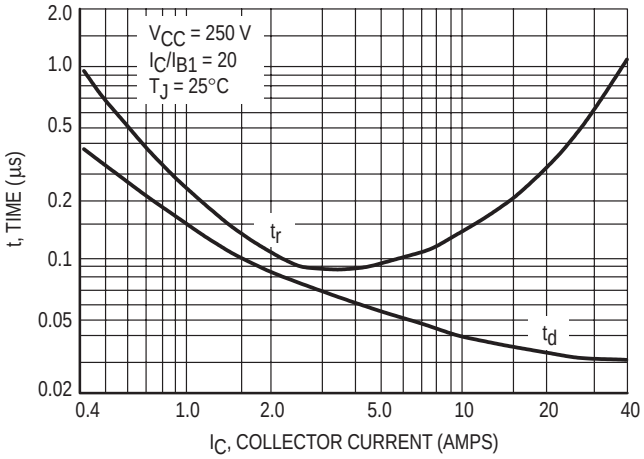


Figure 10. Typical Turn–On Switching Times

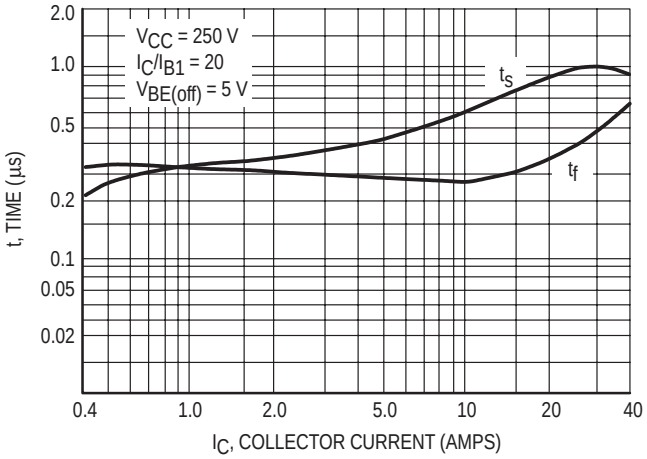


Figure 11. Typical Turn–Off Switching Times

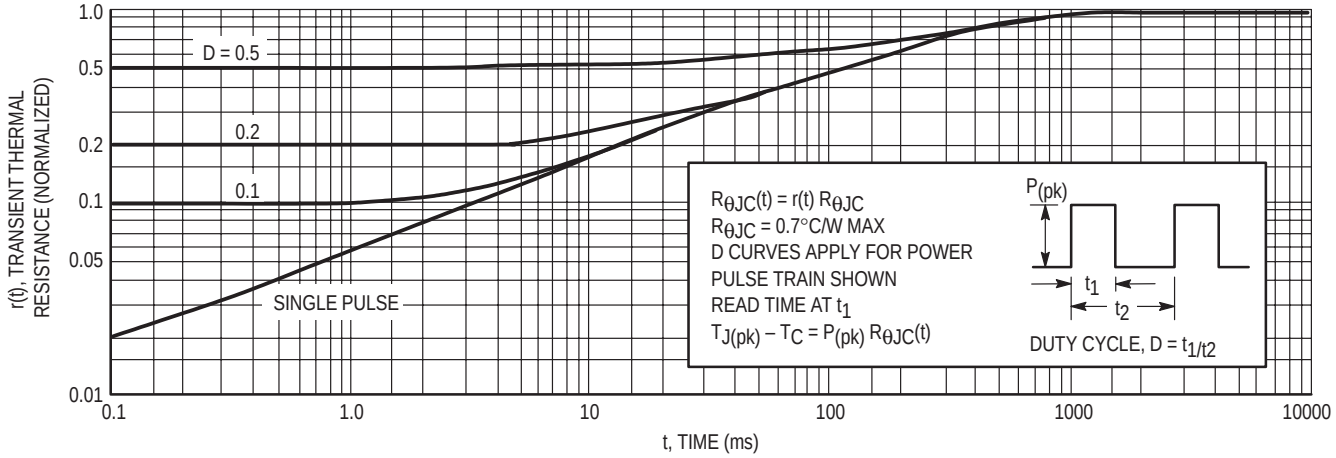


Figure 12. Thermal Response

The Safe Operating Area figures shown in Figures 13 and 14 are specified for these devices under the test conditions shown.

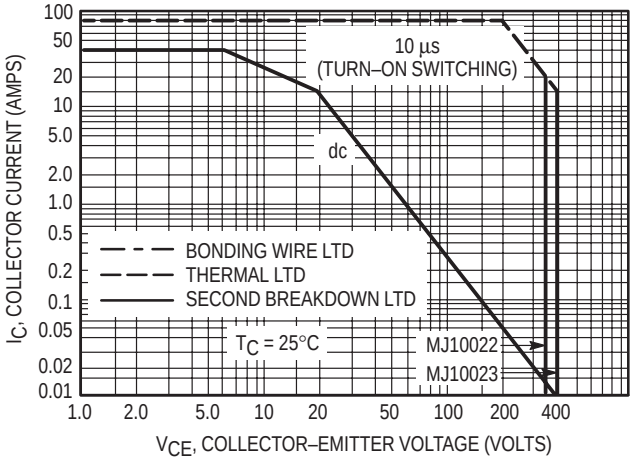


Figure 13. Maximum Forward Bias Safe Operating Area

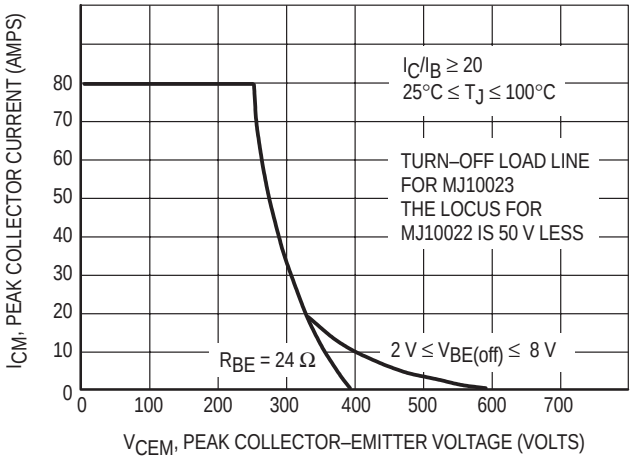


Figure 14. Maximum RBSOA, Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

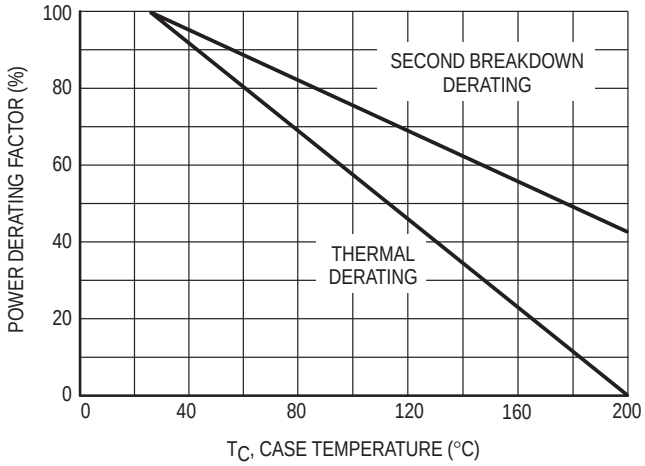


Figure 15. Power Derating

High-Current Complementary Silicon Transistors

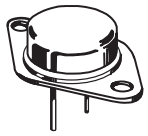
. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain — h_{FE} = 1000 (Min) @ I_C – 20 Adc
- Monolithic Construction with Built–in Base Emitter Shunt Resistor
- Junction Temperature to +200°C

PNP
MJ11013
MJ11015
NPN
MJ11012
MJ11014
MJ11016*

***Motorola Preferred Device**

30 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60–120 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ11012	MJ11013 MJ11014	MJ11015 MJ11016	Unit
Collector–Emitter Voltage	V_{CEO}	60	90	120	Vdc
Collector–Base Voltage	V_{CB}	60	90	120	Vdc
Emitter–Base Voltage	V_{EB}	5			Vdc
Collector Current	I_C	30			Adc
Base Current	I_B	1			Adc
Total Device Dissipation @T_C = 25°C Derate above 25°C @ T_C = 100°C	P_D	200 1.15			Watts W/°C
Operating Storage Junction Temperature Range	T_J, T_{stg}	–55 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.87	°C/W
Maximum Lead Temperature for Soldering Purposes for ≤ 10 Seconds.	T_L	275	°C

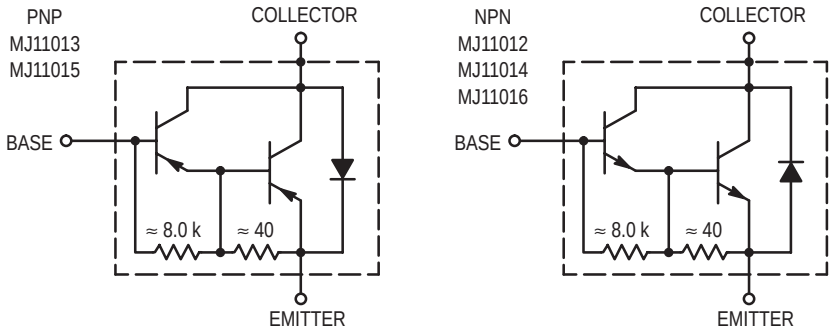


Figure 1. Darlington Circuit Schematic

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristics		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage(1)		$V_{(BR)CEO}$			Vdc
(I_C = 100 mAdc, I_B = 0)	MJ11012		60	—	
	MJ11013, MJ11014		90	—	
	MJ11015, MJ11016		120	—	
Collector–Emitter Leakage Current		I_{CER}			mAdc
(V_{CE} = 60 Vdc, R_{BE} = 1k ohm)	MJ11012		—	1	
(V_{CE} = 90 Vdc, R_{BE} = 1k ohm)	MJ11013, MJ11014		—	1	
(V_{CE} = 120 Vdc, R_{BE} = 1k ohm)	MJ11015, MJ11016		—	1	
(V_{CE} = 60 Vdc, R_{BE} = 1k ohm, T_C = 150°C)	MJ11012		—	5	
(V_{CE} = 90 Vdc, R_{BE} = 1k ohm, T_C = 150°C)	MJ11013, MJ11014		—	5	
(V_{CE} = 120 Vdc, R_{BE} = 1k ohm, T_C = 150°C)	MJ11015, MJ11016		—	5	
Emitter Cutoff Current		I_{EBO}	—	5	mAdc
(V_{BE} = 5 Vdc, I_C = 0)					
Collector–Emitter Leakage Current		I_{CEO}	—	1	mAdc
(V_{CE} = 50 Vdc, I_B = 0)					
ON CHARACTERISTICS(1)					
DC Current Gain		h_{FE}			—
(I_C = 20 Adc,V_{CE} = 5 Vdc)			1000	—	
(I_C = 30 Adc, V_{CE} = 5 Vdc)			200	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 20 Adc, I_B = 200 mAdc)			—	3	
(I_C = 30 Adc, I_B = 300 mAdc)			—	4	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 20 A, I_B = 200 mAdc)			—	3.5	
(I_C = 30 A, I_B = 300 mAdc)			—	5	
DYNAMIC CHARACTERISTICS					
Current–Gain Bandwidth Product		h_{fe}	4	—	MHz
(I_C = 10 A, V_{CE} = 3 Vdc, f = 1 MHz)					

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

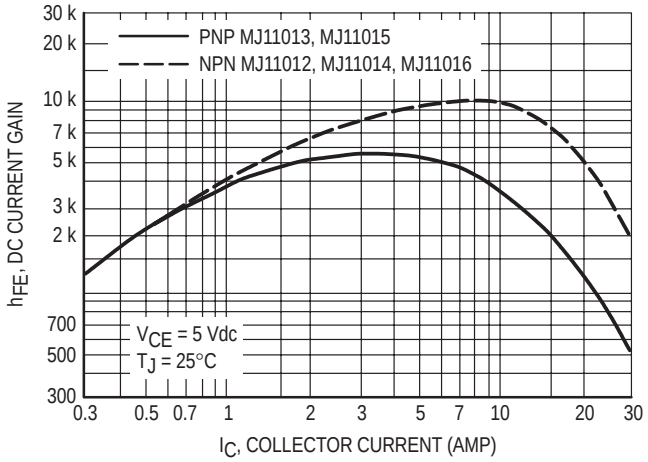


Figure 2. DC Current Gain (1)

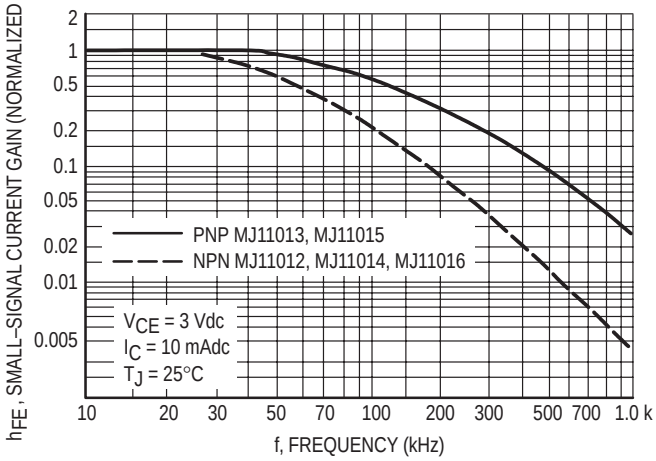


Figure 3. Small–Signal Current Gain

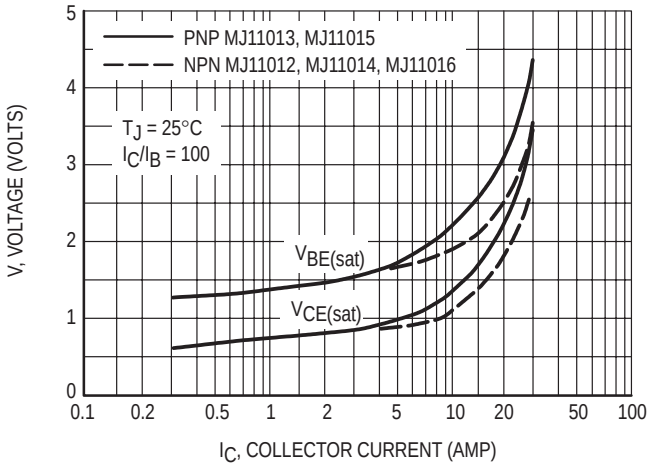


Figure 4. “On” Voltages (1)

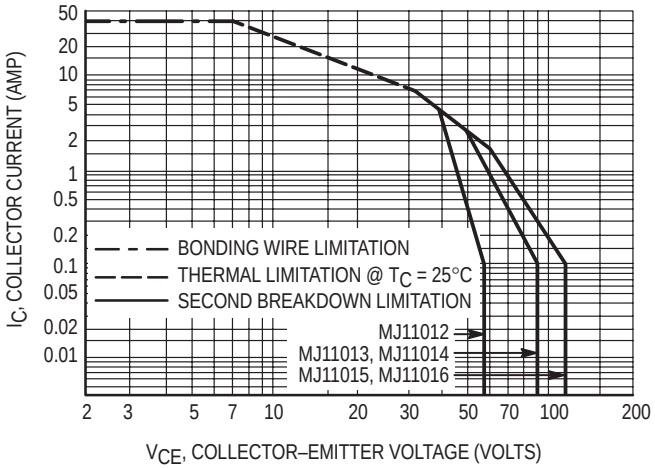


Figure 5. Active Region DC Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operations e.g., the transistor must not be subjected to greater dissipation than the curves indicate.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

Complementary Darlington Silicon Power Transistors

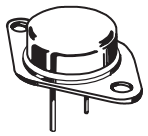
PNP
MJ11017
MJ11021*
NPN
MJ11018*
MJ11022

*Motorola Preferred Device

. . . designed for use as general purpose amplifiers, low frequency switching and motor control applications.

- High dc Current Gain @ 10 Adc — h_{FE} = 400 Min (All Types)
- Collector–Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 150 Vdc (Min) – MJ11018, 17
  = 250 Vdc (Min) – MJ11022, 21
- Low Collector–Emitter Saturation
  $V_{CE(sat)}$ = 1.0 V (Typ) @ I_C = 5.0 A
  = 1.8 V (Typ) @ I_C = 10 A
- Monolithic Construction
- 100% SOA Tested @ V_{CE} = 44 V, I_C = 4.0 A, t = 250 ms.

30 AMPERE DARLINGTON POWER TRANSISTORS COMPLEMENTARY SILICON 60–120 VOLTS 200 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ11018 MJ11017	MJ11022 MJ11021	Unit
Collector–Emitter Voltage	V_{CEO}	150	250	Vdc
Collector–Base Voltage	V_{CB}	150	250	Vdc
Emitter–Base Voltage	V_{EB}	50		Vdc
Collector Current — Continuous Peak	I_C	15 30		Adc
Base Current	I_B	0.5		Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	175 1.16		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +175 –65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.86	°C/W

(1) Pulse Test: Pulse Width 5.0 ms, Duty Cycle ≤ 10%.

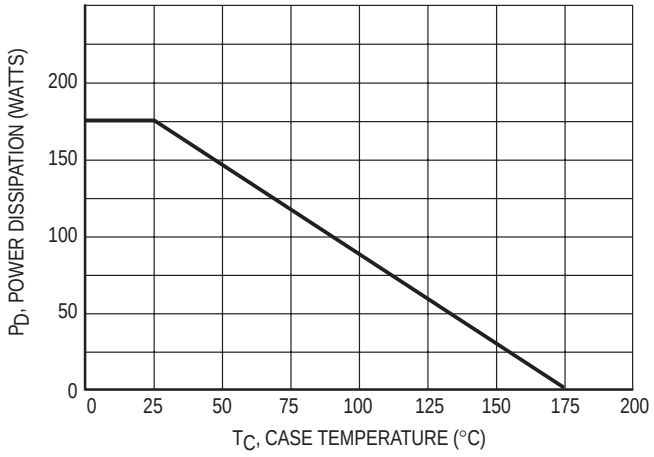


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

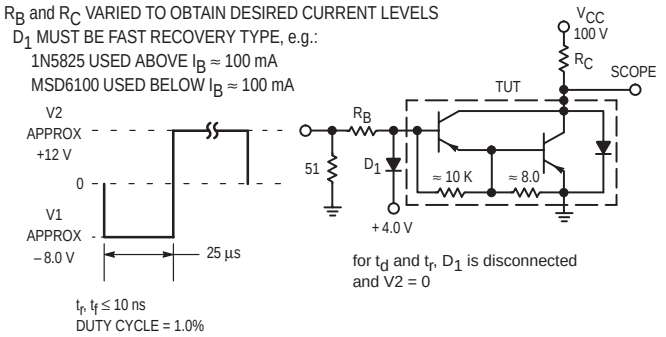
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 0. 1 Adc, I_B = 0)	MJ11017, MJ11018 MJ11021, MJ11022	$V_{CEO(sus)}$	 150 250	 — —	Vdc
Collector Cutoff Current (V_{CE} = 75, I_B = 0) (V_{CE} = 125, I_B = 0)	 MJ11017, MJ11018 MJ11021, MJ11022	I_{CEO}	 — —	 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_J = 150°C)		I_{CEV}	 — —	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc) (I_C = 15 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	 400 100	 15,000 —	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 100 mA) (I_C = 15 Adc, I_B = 150 mA)		$V_{CE(sat)}$	 — —	 2.0 3.4	Vdc
Base–Emitter On Voltage I_C = 10 A, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
Base–Emitter Saturation Voltage (I_C = 15 Adc, I_B = 150 mA)		$V_{BE(sat)}$	—	3.8	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain Bandwidth Product (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$[h_{fe}]$	3.0	—	Mhz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	 MJ11018, MJ11022 MJ11017, MJ11021	C_{ob}	 — —	 400 600	pF
Small–Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	75	—	—

SWITCHING CHARACTERISTICS

Characteristic		Symbol	Typical NPN	Typical PNP	Unit
Delay Time	(V_{CC} = 100 V, I_C = 10 A, I_B = 100 mA $V_{BE(off)}$ = 50 V) (See Figure 2.)	t_d	150	75	ns
Rise Time		t_r	1.2	0.5	µs
Storage Time		t_s	4.4	2.7	µs
Fall Time		t_f	10.0	2.5	µs

(1) Pulsed Test: Pulse Width = 300 µs, Duty Cycle ≤ 2%.



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

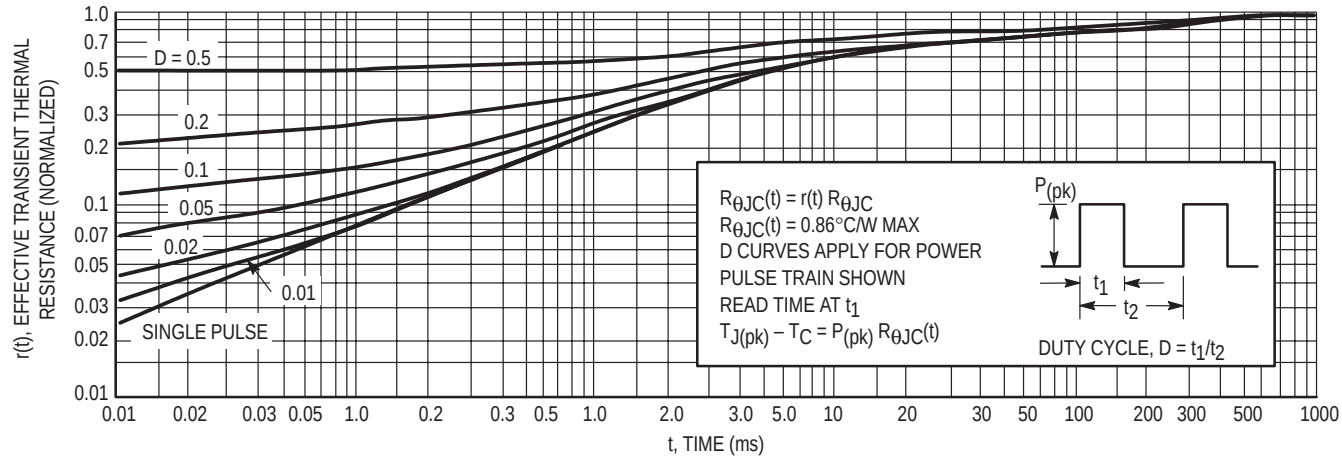


Figure 3. Thermal Response

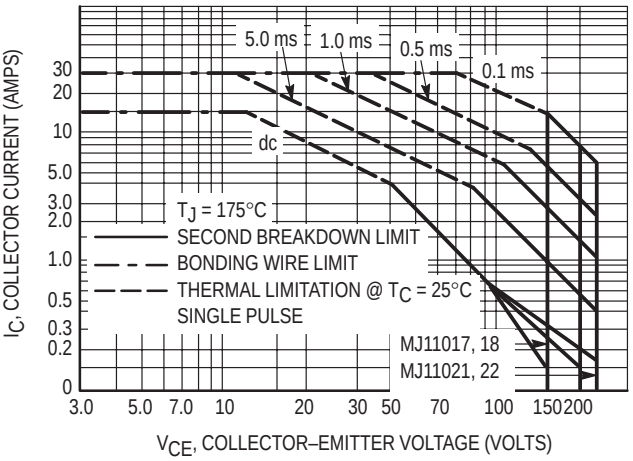


Figure 4. Maximum Rated Forward Bias Safe Operating Area (FBSOA)

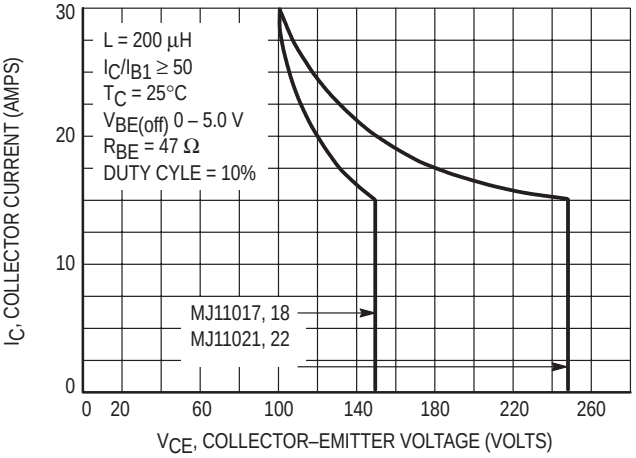


Figure 5. Maximum RBSOA, Reverse Bias Safe Operating Area

FORWARD BIAS

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 175°C$, T_C is variable dependIng on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 175°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be hold to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives ROSOA characteristics.

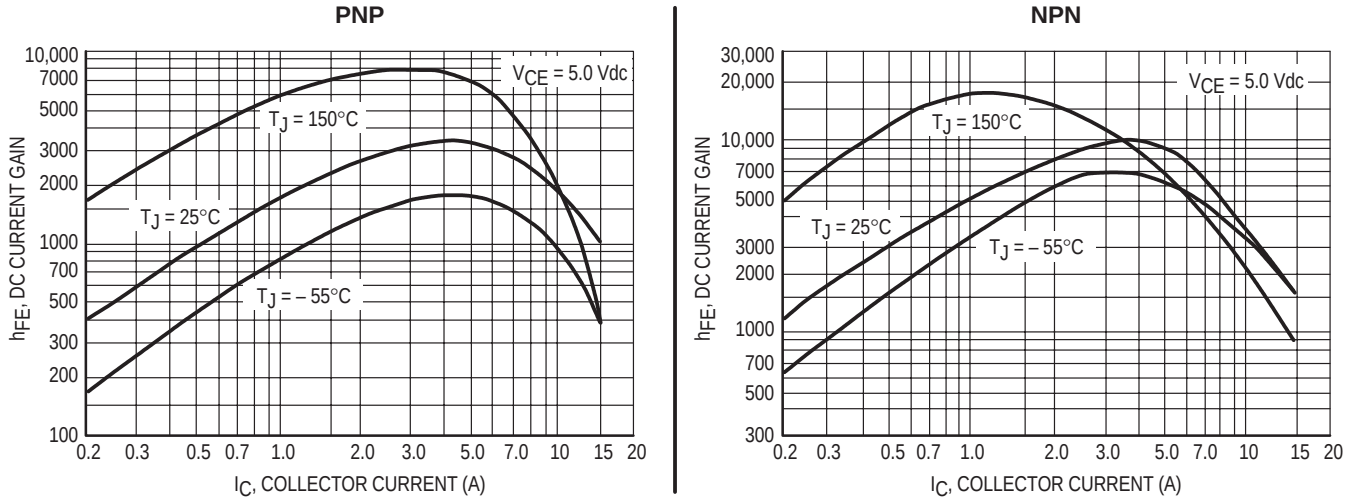


Figure 6. DC Current Gain

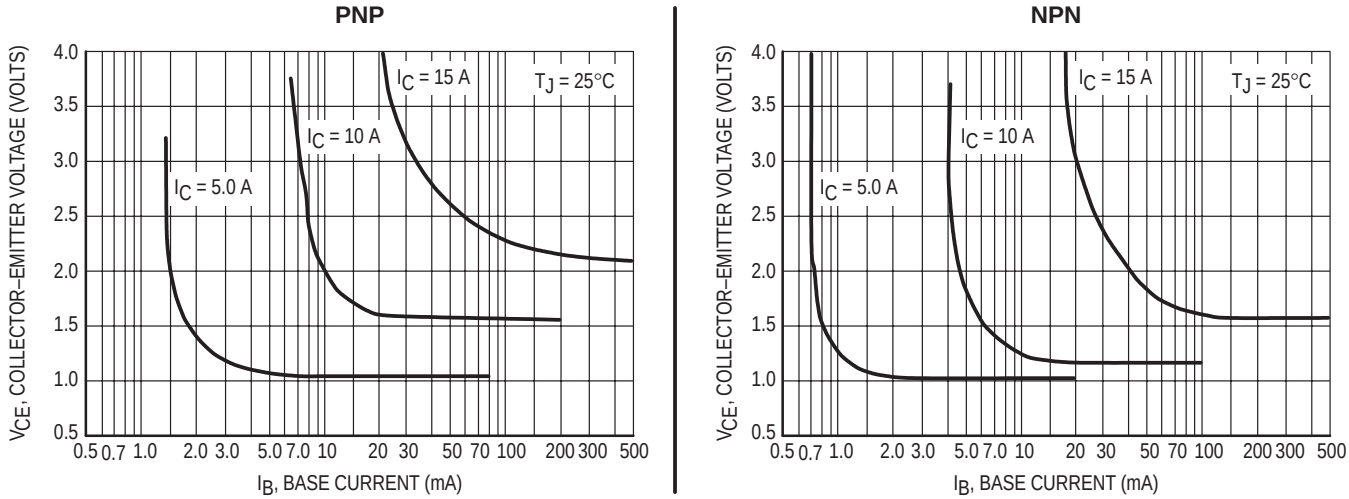


Figure 7. Collector Saturation Region

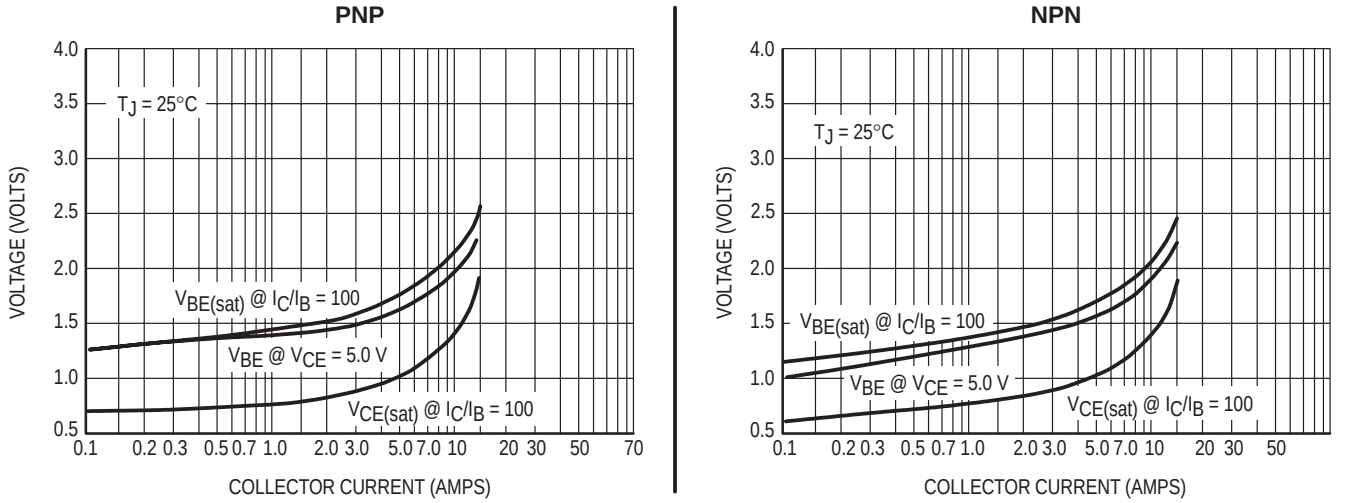


Figure 8. “On” Voltages

High-Current Complementary Silicon Transistors

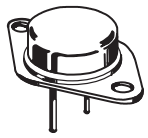
. . . for use as output devices in complementary general purpose amplifier applications.

- High DC Current Gain — h_{FE} = 1000 (Min) @ I_C = 25 Adc
  h_{FE} = 400 (Min) @ I_C = 50 Adc
- Curves to 100 A (Pulsed)
- Diode Protection to Rated I_C
- Monolithic Construction with Built–In Base–Emitter Shunt Resistor
- Junction Temperature to +200°C

NPN
MJ11028
MJ11030
MJ11032*
PNP
MJ11029
MJ11031
MJ11033*

*Motorola Preferred Device

50 AMPERE COMPLEMENTARY SILICON DARLINGTON POWER TRANSISTORS 60–120 VOLTS 300 WATTS



CASE 197A–05
TO–204AE (TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ11028 MJ11029	MJ11030 MJ11031	MJ11032 MJ11033	Unit
Collector–Emitter Voltage	V_{CEO}	60	90	120	Vdc
Collector–Base Voltage	V_{CB}	60	90	120	Vdc
Emitter–Base Voltage	V_{EB}	5			Vdc
Collector Current — Continuous Peak	I_C I_{CM}	50 100			Adc
Base Current — Continuous	I_B	2			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C @ T_C = 100°C	P_D	300 1.71			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Maximum Lead Temperature for Soldering Purposes for ≤ 10 seconds	T_L	275	°C
Thermal Resistance Junction to Case	$R_{\theta JC}$	0.584	°C

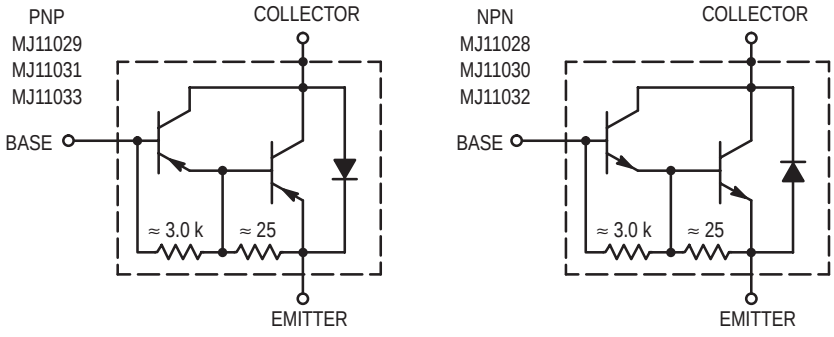


Figure 1. Darlington Circuit Schematic

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (1)	MJ11028, MJ11029	$V_{(BR)CEO}$	60	—	Vdc
(I_C = 1 00 mAdc, I_B = 0)	MJ11030, MJ11031		90	—	
	MJ11032, MJ11033		120	—	
Collector–Emitter Leakage Current		I_{CER}			mAdc
(V_{CE} = 60 Vdc, R_{BE} = 1 k ohm)	MJ11028, MJ11029		—	2	
(V_{CE} = 90 Vdc, R_{BE} = 1 k ohm)	MJ11030, MJ11031		—	2	
(V_{CE} = 120 Vdc, R_{BE} = 1 k ohm)	MJ11032, MJ11033		—	2	
(V_{CE} = 60 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11028, MJ11029		—	10	
(V_{CE} = 90 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11030, MJ11031		—	10	
(V_{CE} = 120 Vdc, R_{BE} = 1 k ohm, T_C = 150°C)	MJ11032, MJ11033		—	10	
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	5	mAdc
Collector–Emitter Leakage Current (V_{CE} = 50 Vdc, I_B = 0)		I_{CEO}	—	2	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 25 Adc, V_{CE} = 5 Vdc)			1 k	18 k	
(I_C = 50 Adc, V_{CE} = 5 Vdc)			400	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 250 mAdc)			—	2.5	
(I_C = 50 Adc, I_B = 500 mAdc)			—	3.5	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 200 mAdc)			—	3.0	
(I_C = 50 Adc, I_B = 300 mAdc)			—	4.5	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

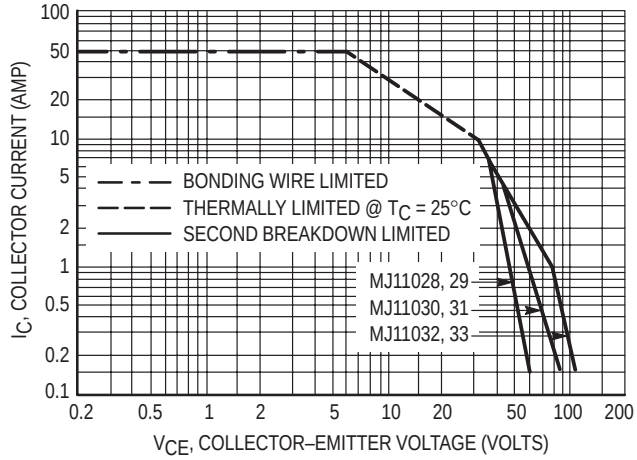


Figure 2. DC Safe Operating Area

There are two limitations on the power–handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

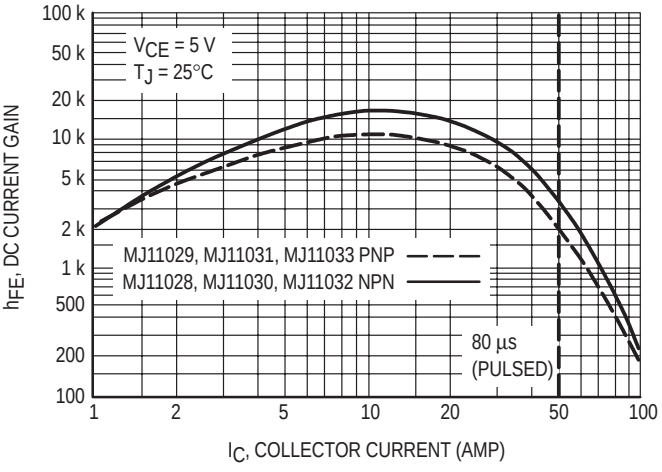


Figure 3. DC Current Gain

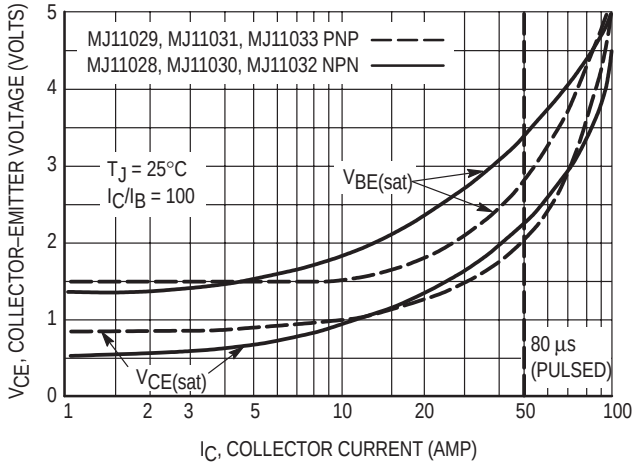


Figure 4. "On" Voltage

MJ13333

Designer's™ Data Sheet

SWITCHMODE Series NPN Silicon Power Transistor

20 AMPERE NPN SILICON POWER TRANSISTORS 400–500 VOLTS 175 WATTS

The MJ13333 transistor is designed for high voltage, high–speed, power switching in inductive circuits where fall time is critical. It is particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

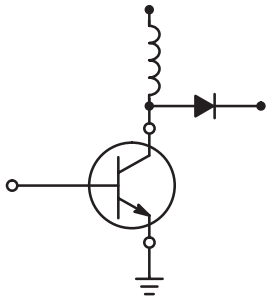
Fast Turn Off Times

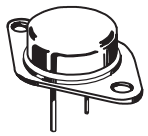
200 ns Inductive Fall Time — 25°C (Typ)
1.8 µs Inductive Storage Time — 25°C (Typ)

Operating Temperature Range –65 to +200°C

100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents





CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	400	Vdc
Collector–Emitter voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	20 30	Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	10 15	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤10%.
Similar device types available with lower V_{CEO} ratings, see the MJ13330 (200 V) and MJ13331 (250 V).

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEV}	 — —	 — —	 0.25 5.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 13			
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	10	—	60	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc) (I_C = 20 Adc, I_B = 6.7 Adc) (I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 — — —	 1.8 5.0 2.4	Vdc
Base Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc) (I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 — —	 1.8 1.8	Vdc
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	125	—	500	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	(V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5.0 Vdc, t_p = 10 μs, Duty Cycle ≤ 2.0%)	t_d	—	0.02	0.1	μs
Rise Time		t_r	—	0.3	0.7	μs
Storage Time		t_s	—	1.6	4.0	μs
Fall Time		t_f	—	0.3	0.7	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	2.5	5.0	μs
Crossover Time		t_c	—	0.8	2.0	μs
Storage Time	(I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	—	1.8	—	μs
Crossover Time		t_c	—	0.4	—	μs
Fall Time		t_{fi}	—	0.2	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

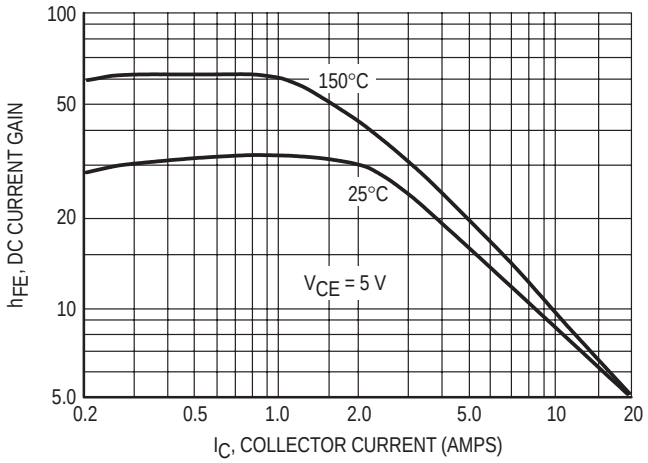


Figure 1. DC Current Gain

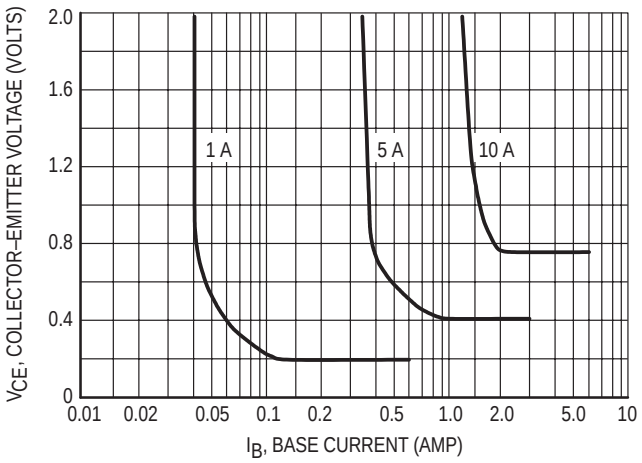


Figure 2. Collector Saturation Region

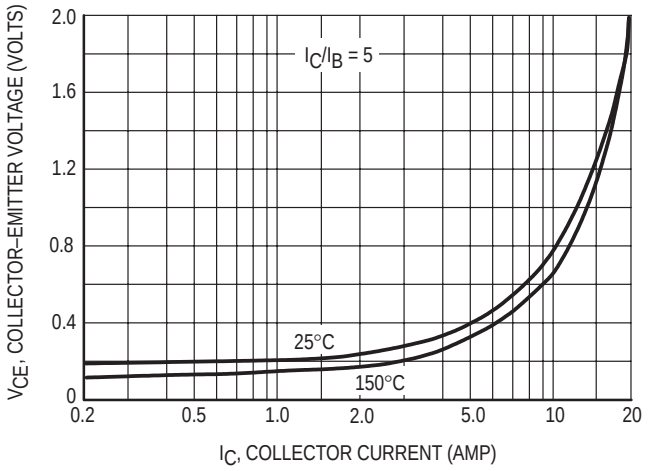


Figure 3. Collector–Emitter Saturation Region

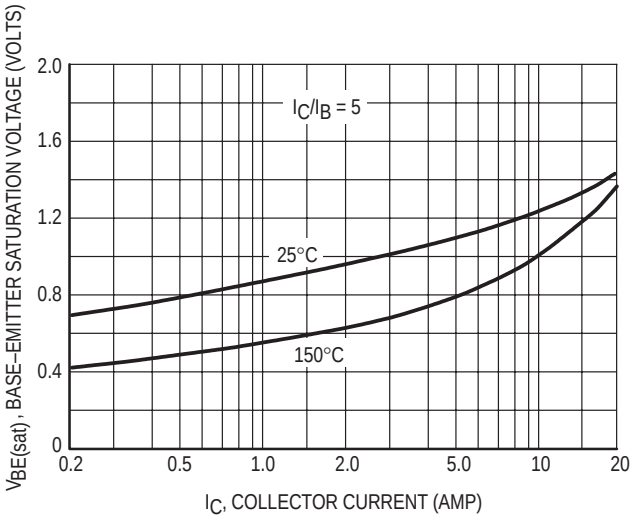


Figure 4. Base–Emitter Voltage

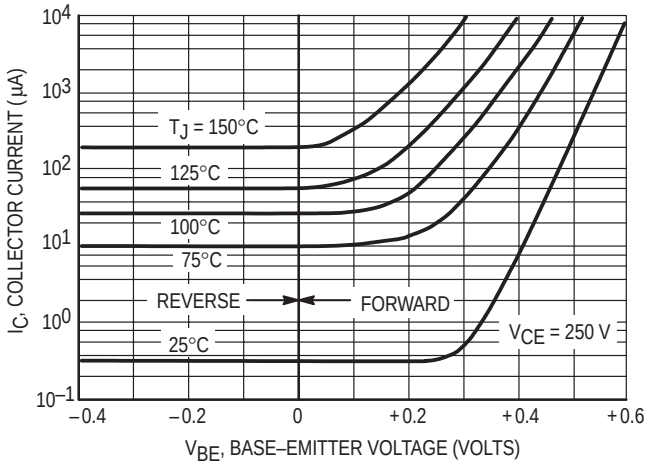


Figure 5. Collector Cutoff Region

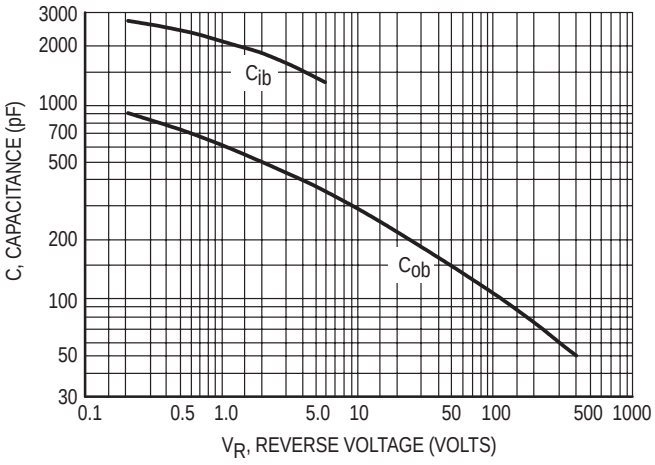


Figure 6. Capacitance

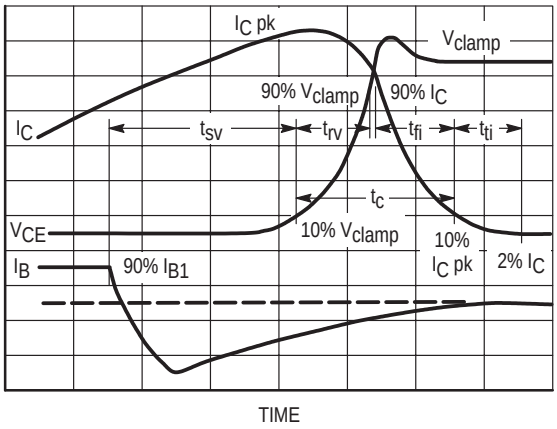


Figure 7. Inductive Switching Measurements

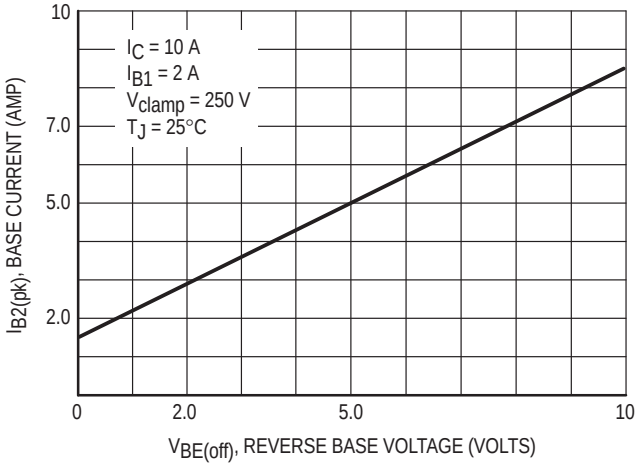


Figure 8. Reverse Base Current versus $V_{BE(off)}$ With No External Base Resistance

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10 – 90% V_{clamp}
t_{fi} = Current Fall Time, 90 – 10% I_C
t_{ti} = Current Tail, 10 – 2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers, However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

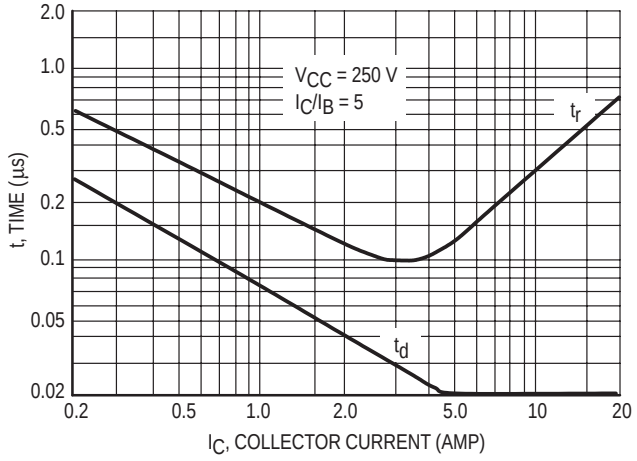


Figure 9. Turn–On Switching Times

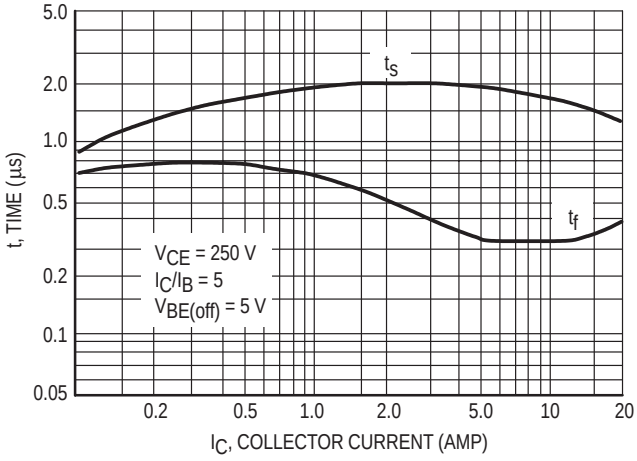


Figure 10. Turn–Off Switching Times

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20, 1, 0, 2 PW Varied to Attain I_C = 100 mA	250 µF, 470 Ω 2 W, 47 Ω, R1, +15 V, 15 V, 0, 330 Ω, 5.1 Ω 5 W, R2, 1, 2, 50 Ω, 100 Ω, 430 Ω, 39 Ω, –5.2, 250 µF All Diodes — 1N4934 All NPN — MJE200 All PNP — MJE210 Adjust R1 to obtain I_{B1} For switching and RBSOA, R2 = 0 For $V_{CEO(sus)}$, R2 = ∞	**TURN–ON TIME** 1, 2, I_{B1} I_{B1} adjusted to obtain the forced h_{FE} desired **TURN–OFF TIME** Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 10 µs
TEST CIRCUITS	**INDUCTIVE TEST CIRCUIT** TUT, 1, INPUT, SEE ABOVE FOR DETAILED CONDITIONS, 1N4937 OR EQUIVALENT, R_{coil}, L_{coil}, V_{clamp}, V_{CC}, 2, RS = 0.1 Ω **OUTPUT WAVEFORMS** I_C, $I_{C(pk)}$, t_f Clamped, t, t_1, t_f, V_{CE}, V_{CE} or V_{clamp}, TIME, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	**RESISTIVE TEST CIRCUIT** TUT, 1, 2, R_L, V_{CC}

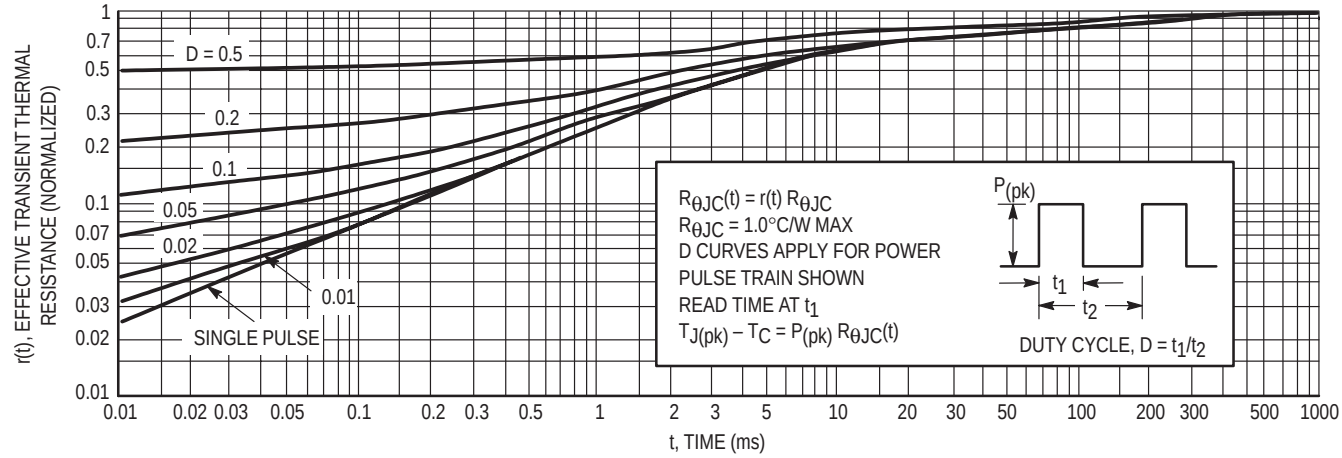


Figure 11. Thermal Response

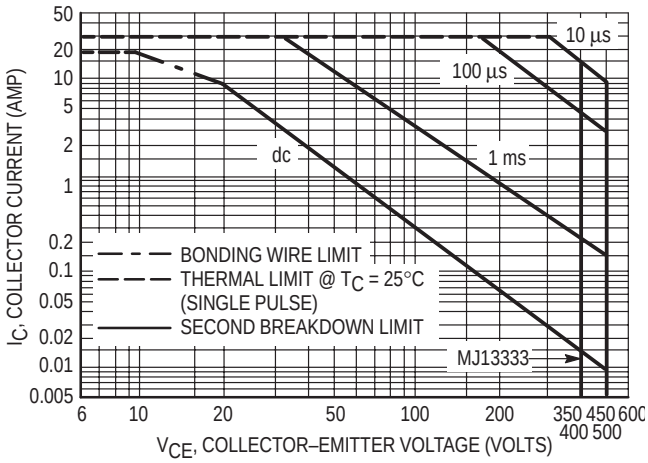


Figure 12. Forward Bias Safe Operating Area

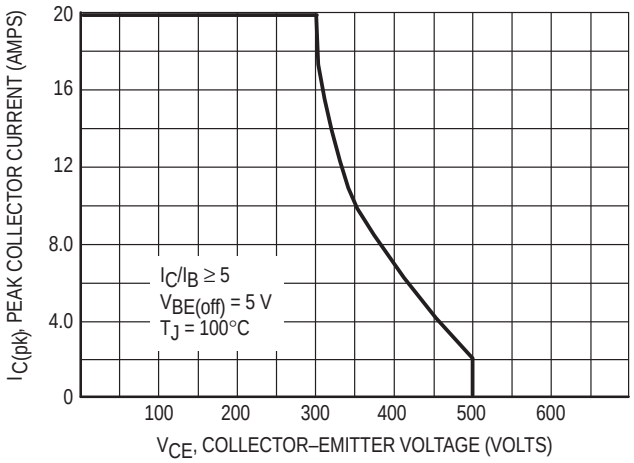


Figure 13. RBSOA, Reverse Bias Switching Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on T_C = 25°C. $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

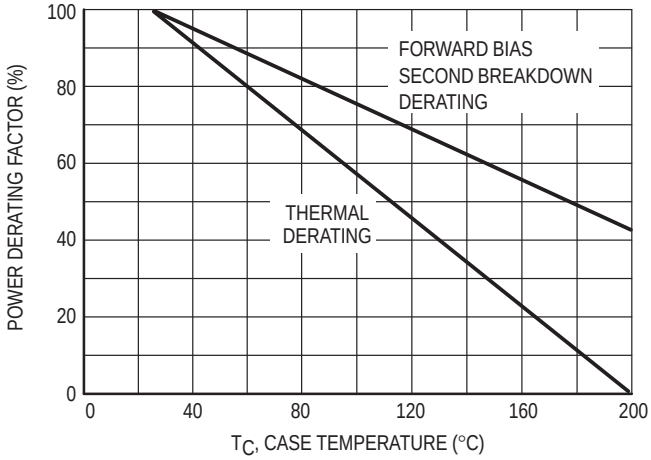


Figure 14. Power Derating

High-Current Complementary Silicon Power Transistors

. . . designed for use in high–power amplifier and switching circuit applications,

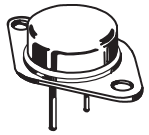
- High Current Capability — I_C Continuous = 60 Amperes
- DC Current Gain — h_{FE} = 15–100 @ I_C = 50 Adc
- Low Collector–Emitter Saturation Voltage — $V_{CE(sat)}$ = 2.5 Vdc (Max) @ I_C = 50 Adc

NPN
MJ14002*
PNP
MJ14001

MJ14003*

***Motorola Preferred Device**

60 AMPERES
COMPLEMENTARY
SILICON
POWER TRANSITORS
60–80 VOLTS
300 WATTS



CASE 197A–05
TO–204AE (TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ14001	MJ14002 MJ14003	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector Base Voltage	V_{CBO}	60	80	Vdc
Emitter–Base Voltage	V_{EBO}	5		Vdc
Collector Current — Continuous	I_C	60		Adc
Base Current — Continuous	I_B	15		Adc
Emitter Current — Continuous	I_E	75		
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 17		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.584	°C/W

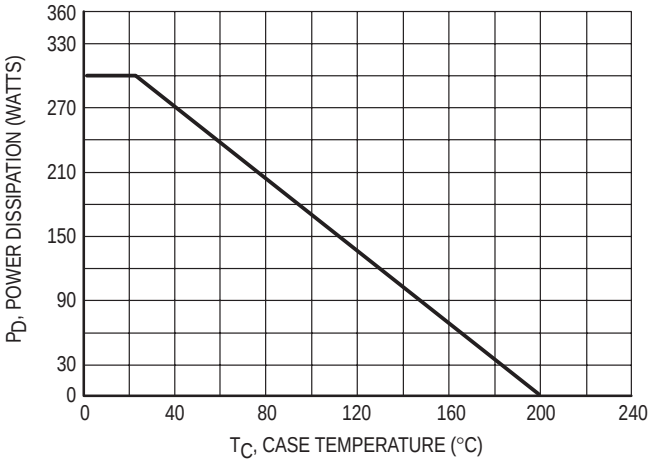


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 200 mAdc, I_B = 0)	MJ14001		60	—	
	MJ14002, MJ14003		80	—	
Collector Cutoff Current		I_{CEO}			mA
(V_{CE} = 30 Vdc, I_B = 0)	MJ14001		—	1.0	
(V_{CE} = 40 Vdc, I_B = 0)	MJ14402, MJ14003		—	1.0	
Collector Cutoff Current		I_{CEX}			mA
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 V)	MJ14001		—	1.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 V)	MJ14002, MJ14003		—	1.0	
Collector Cutoff Current		I_{CBO}			mA
(V_{CB} = 60 Vdc, I_E = 0)	MJ14001		—	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	MJ14002, MJ14003		—	1.0	
Emitter Cutoff Current		I_{EBO}	—	1.0	mA
(V_{BE} = 5 Vdc, I_C = 0)					
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			—
(I_C = 25 Adc, V_{CE} = 3.0 V)			30	—	
(I_C = 50 Adc, V_{CE} = 3.0 V)			15	100	
(I_C = 60 Adc, V_{CE} = 3.0 V)			5	—	
Collector–Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.5 Adc)			—	1	
(I_C = 50 Adc, I_B = 5.0 Adc)			—	2.5	
(I_C = 60 Adc, I_B = 12 Adc)			—	3	
Base–Emitter Saturation Voltage (1)		$V_{BE(sat)}$			Vdc
(I_C = 25 Adc, I_B = 2.5 Adc)			—	2	
(I_C = 50 Adc, I_B = 5.0 Adc)			—	3	
(I_C = 60 Adc, I_B = 12 Adc)			—	4	
DYNAMIC CHARACTERISTICS					
Output Capacitance		C_{ob}	—	2000	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)					

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

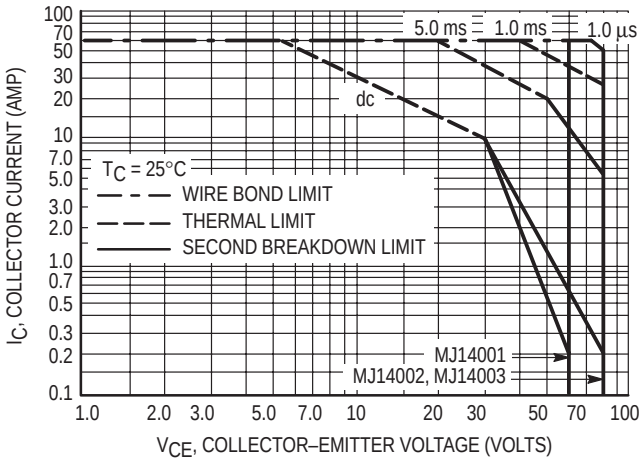


Figure 2. Maximum Rated Forward Biased Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ ≤ 200°C. $T_{J(pk)}$ may be calculated from the data in Figure 13. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL ELECTRICAL CHARACTERISTICS

NPN
MJ14002

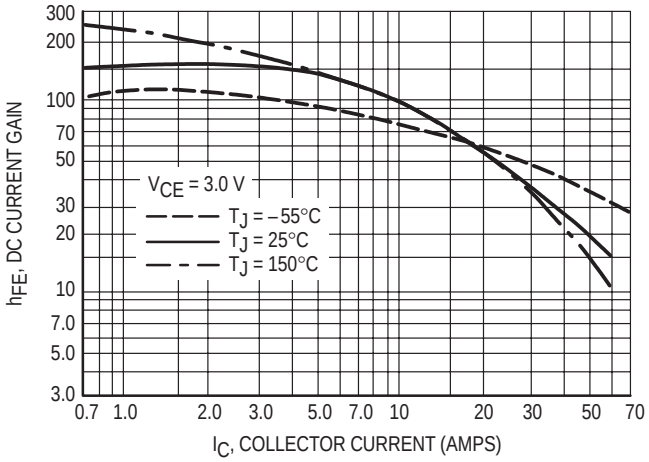


Figure 3. DC Current Gain

PNP
MJ14001, MJ14003

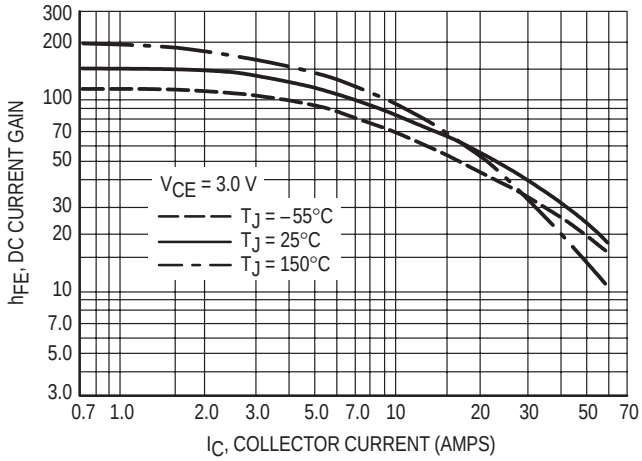


Figure 4. DC Current Gain

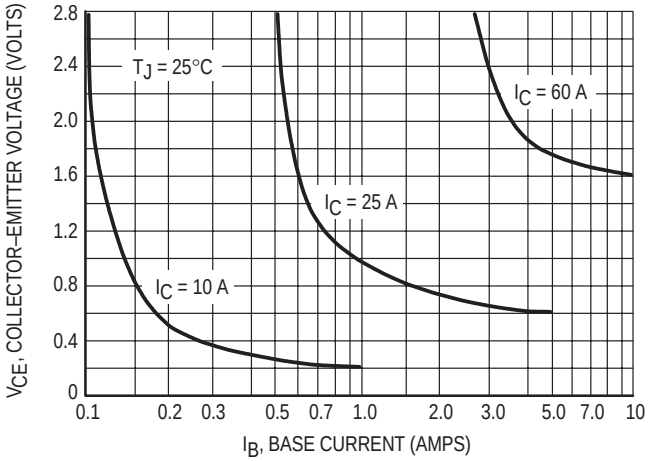


Figure 5. Collector Saturation Region

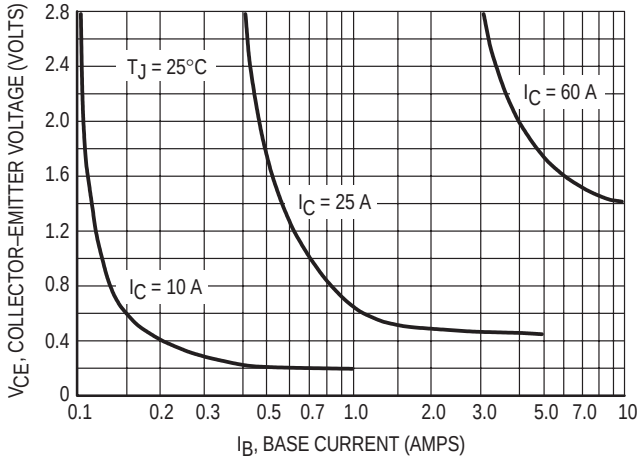


Figure 6. Collector Saturation Region

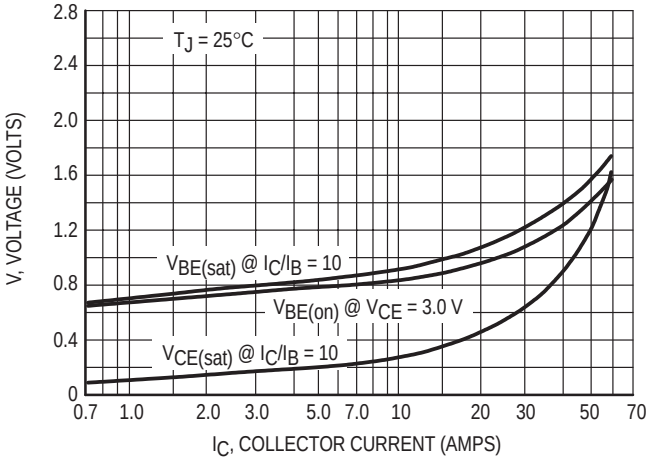


Figure 7. “On” Voltages

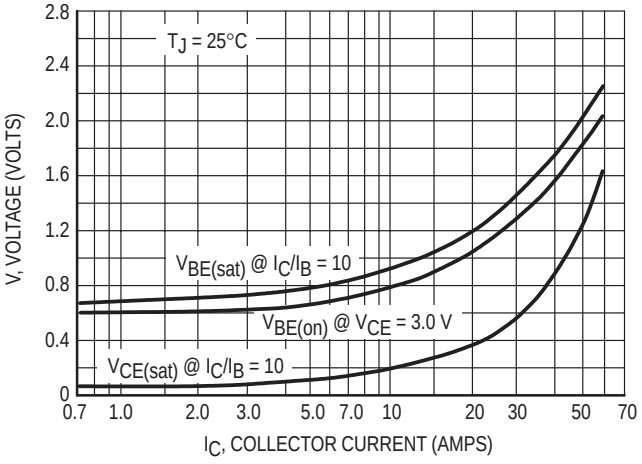


Figure 8. “On” Voltages

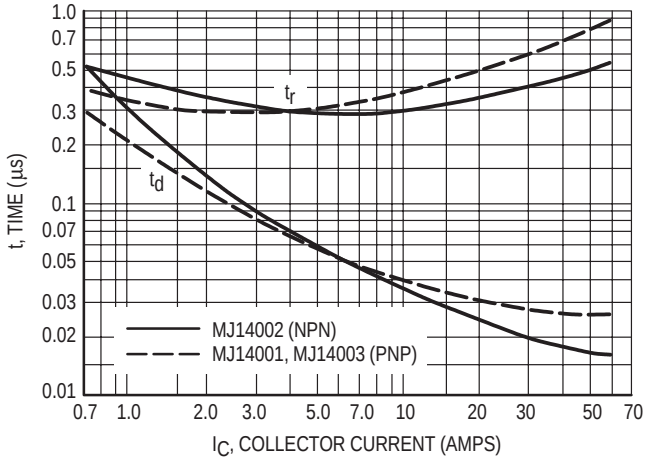


Figure 9. Turn–On Switching Times

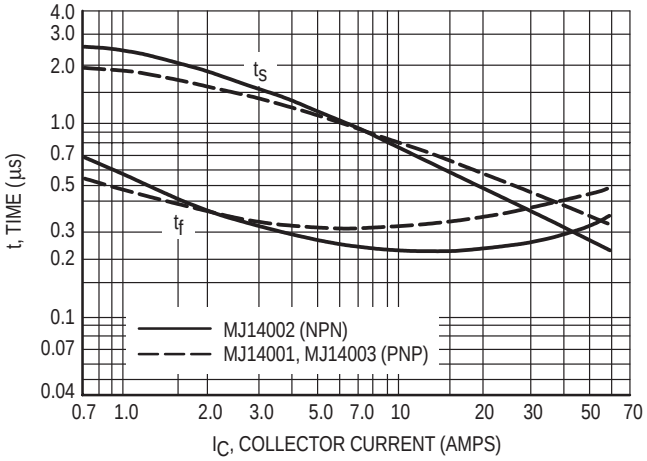


Figure 10. Turn–Off Switching Times

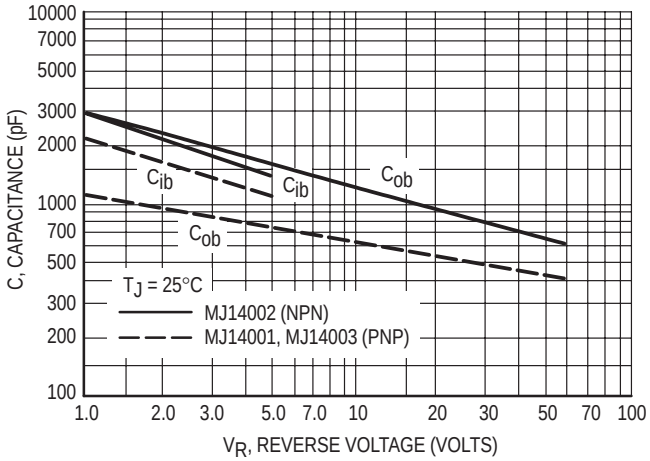
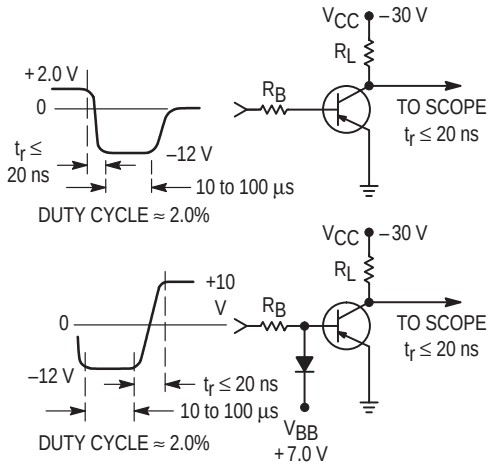


Figure 11. Capacitance Variation



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

Figure 12. Switching Test Circuit

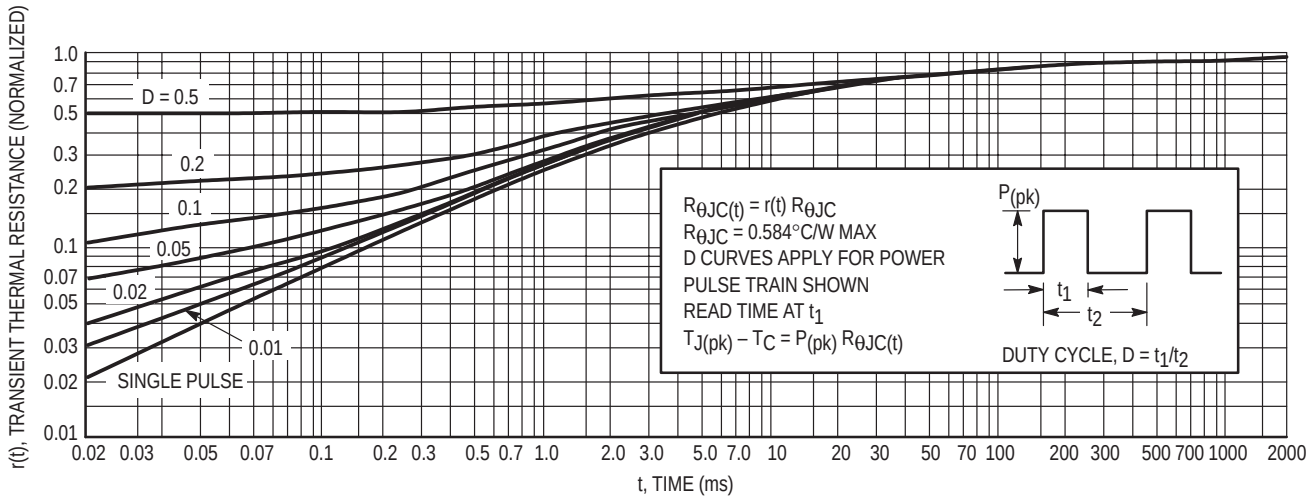


Figure 13. Thermal Response

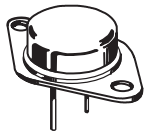
Complementary Silicon Power Transistors

NPN
MJ15001
PNP
MJ15002

The MJ15001 and MJ15002 are EpiBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) —
  200 W @ 40 V
  50 W @ 100 V
- For Low Distortion Complementary Designs
- High DC Current Gain —
  h_{FE} = 25 (Min) @ I_C = 4 Adc

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
140 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	140	Vdc
Collector–Base Voltage	V_{CBO}	140	Vdc
Emitter–Base Voltage	V_{EBO}	5	Vdc
Collector Current — Continuous	I_C	15	Adc
Base Current — Continuous	I_B	5	Adc
Emitter Current — Continuous	I_E	20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16″ from Case for ≤ 10 seconds	T_L	265	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C, = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	—	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 — —	 100 2	 μAdc mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}	—	250	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1 s (non–repetitive)) (V_{CE} = 100 Vdc, t = 1 s (non–repetitive))	$I_{S/b}$	 5 0.5	 — —	Adc
ON CHARACTERISTICS				
DC Current Gain (I_C = 4 Adc, V_{CE} = 2 Vdc)	h_{FE}	25	150	—
Collector–Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	—	1	Vdc
Base–Emitter On Voltage (I_C = 4 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	—	2	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 0.5 MHz)	f_T	2	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	1000	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

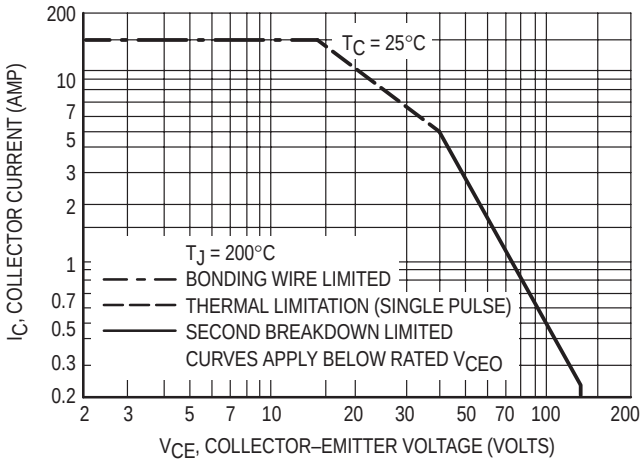


Figure 1. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J\ (pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

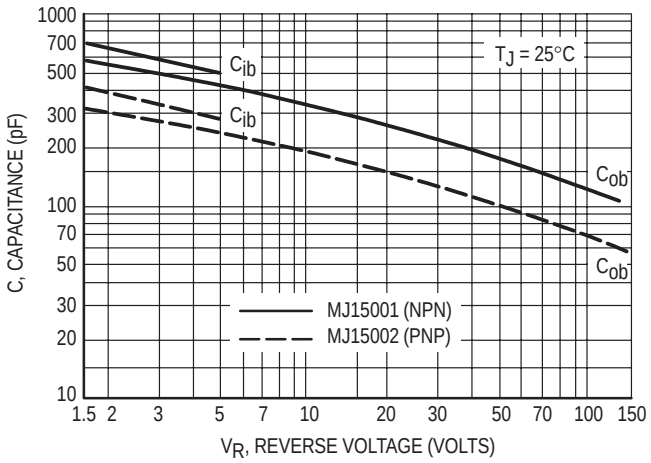


Figure 2. Capacitances

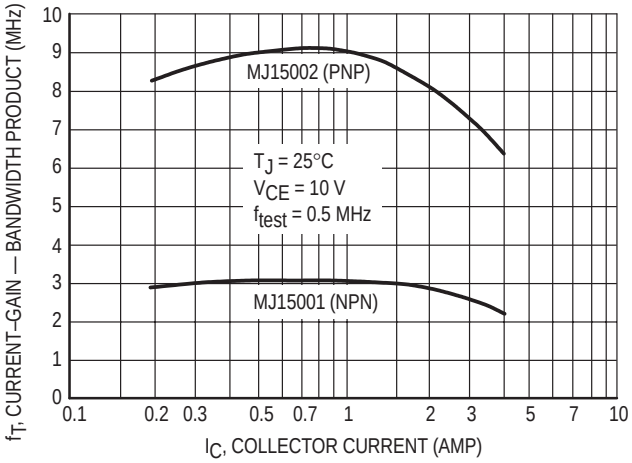


Figure 3. Current–Gain — Bandwidth Product

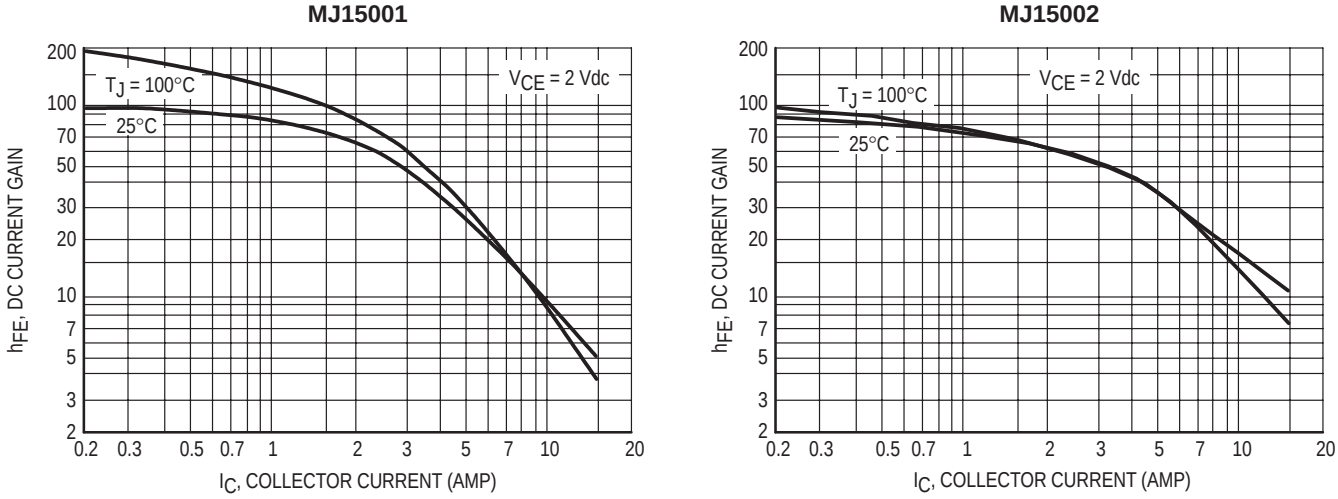


Figure 4. DC Current Gain

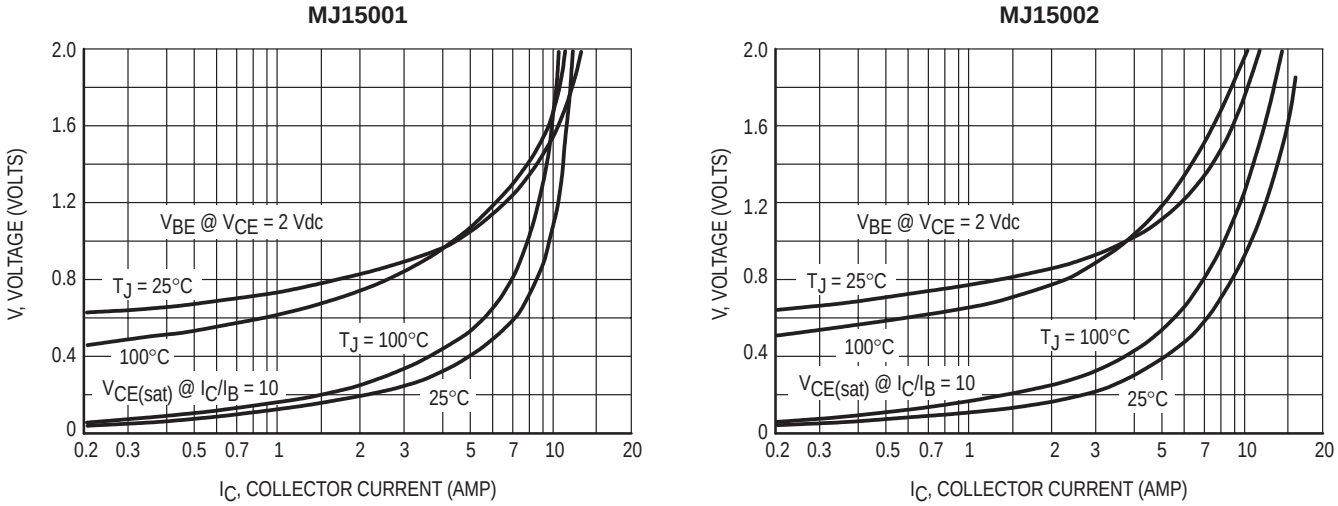


Figure 5. “On” Voltages

Complementary Silicon Power Transistors

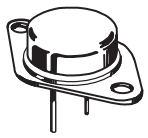
NPN
MJ15003*
PNP
MJ15004*

*Motorola Preferred Device

The MJ15003 and MJ15004 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) —
  250 W @ 50 V
- For Low Distortion Complementary Designs
- High DC Current Gain —
  h_{FE} = 25 (Min) @ I_C = 5 Adc

20 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
140 VOLTS
250 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	140	Vdc
Collector–Base Voltage	V_{CBO}	140	Vdc
Emitter–Base Voltage	V_{EBO}	5	Vdc
Collector Current — Continuous	I_C	20	Adc
Base Current — Continuous	I_B	5	Adc
Emitter Current — Continuous	I_E	25	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/16″ from Case for ≤ 10 seconds	T_L	265	°C

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	140	—	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	— —	100 2	μAdc mAdc
Collector Cutoff Current (V_{CE} = 140 Vdc, I_B = 0)	I_{CEO}	—	250	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Baised (V_{CE} = 50 Vdc, t = 1 s (non repetitive)) (V_{CE} = 100 Vdc, t = 1 s (non repetitive))	$I_{S/b}$	 5 1	 — —	Adc
ON CHARACTERISTICS				
DC Current Gain (I_C = 5 Adc, V_{CE} = 2 Vdc)	h_{FE}	25	150	
Collector Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc)	$V_{CE(sat)}$	—	1	Vdc
Base Emitter On Voltage (I_C = 5 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	—	2	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 0.5 MHz)	f_T	2	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	c_{ob}	—	1000	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

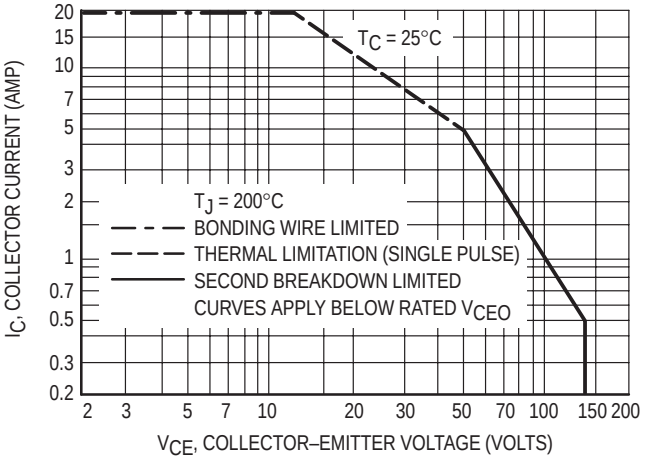


Figure 1. Active–Region Safe Operating Area

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Advance Information

Complementary Silicon Power Transistors

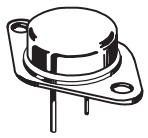
NPN
MJ15011*
PNP
MJ15012*

*Motorola Preferred Device

The MJ15011 and MJ15012 are PowerBase power transistors designed for high–power audio, disk head positioners, and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc–to–dc converters or inverters.

- High Safe Operating Area (100% Tested)
  1.2 A @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage
  h_{FE} = 20 (Min) @ 2 A, 2 V
  $V_{CE(sat)}$ = 2.5 V (Max) @ I_C = 4 A, I_B = 0.4 A
- For Low Distortion Complementary Designs

10 AMPERE
COMPLEMENTARY
POWER TRANSISTORS
250 VOLTS
200 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Emitter Voltage	V_{CEX}	250	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 15	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 5	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	12 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.875	°C/W
Maximum Lead Temperature for Soldering Purposes	T_L	265	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (1) (I_C = 100 mA)	$V_{(BR)CEO}$	250	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc)	I_{CEO}	—	1	mAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 15 Vdc)	I_{CEX}	—	500	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc)	I_{EBO}	—	500	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 2 Adc, V_{CE} = 2 Vdc) (I_C = 4 Adc, V_{CE} = 2 Vdc)	h_{FE}	 20 5	 100 —	—
Collector–Emitter Saturation Voltage (I_C = 2 Adc, I_B = 0.2 Adc) (I_C = 4 Adc, I_B = 0.4 Adc)	$V_{CE(sat)}$	 — —	 0.8 2 5	Vdc
Base–Emitter On Voltage (I_C = 4 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	—	2	Vdc
DYNAMIC CHARACTERISTICS				
Output Capacitance (V_{CB} = 10 Vdc, f = 1 MHz)	C_{ob}	—	750	pF
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 0.5 s) (V_{CE} = 100 Vdc, t = 0.5 s)	$I_{S/b}$	 5 1.4	 — —	Adc

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

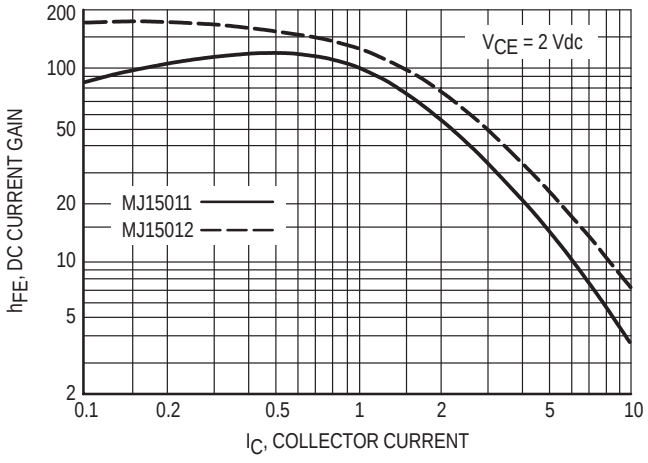


Figure 1. DC Current Gain

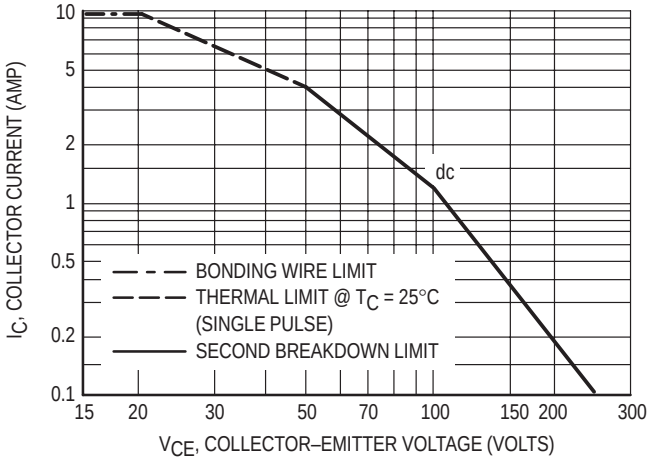


Figure 2. Active Region Safe Operating Area

MJ15015, MJ15016
(See 2N3055A)

Advance Information

Complementary Silicon Power Transistors

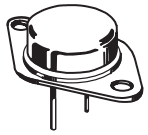
NPN
MJ15018
MJ15020*
PNP
MJ15019
MJ15021*

*Motorola Preferred Device

. . . designed for use as high frequency drivers in Audio Amplifiers.

- High Gain Complementary Silicon Power Transistors
- Safe Operating Area 100% Tested
  50 V, 3.0 A, 1.0 Sec.
- Excellent Frequency Response — f_T = 20 MHz min.

4.0 AMPERES
COMPLEMENTARY
SILICON
POWER TRANSISTORS
200 AND 250 VOLTS
150 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ15018 MJ15019	MJ15020 MJ15021	Unit
Collector–Emitter Voltage	V_{CEO}	200	250	Vdc
Collector–Base Voltage	V_{CBO}	200	250	Vdc
Emitter–Base Voltage	V_{EBO}	7.0		Vdc
Collector Current — Continuous	I_C	4.0		Adc
Base Current — Continuous	I_B	2.0		Adc
Emitter Current — Continuous	I_E	6.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

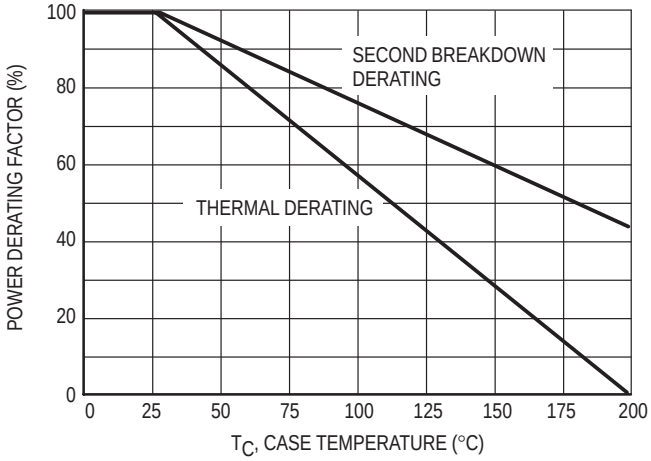


Figure 1. Power Derating

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	MJ15018, MJ15019 MJ15020, MJ15021	$V_{CEO(sus)}$	 200 250	 — —	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 Vdc, I_B = 0)	 MJ15018, MJ15019 MJ15020, MJ15021	I_{CEO}	 — —	 500 500	μAdc
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	500	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward–Biased (V_{CE} = 50 Vdc, t = 0.5 s (non–repetitive)		$I_{S/b}$	3.0	—	Adc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 V) (I_C = 3.0 Adc, V_{CE} = 4.0 V)		h_{FE}	 30 10	 — —	
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	—	1.0	Vdc
Base–Emitter on Voltage (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	20	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, F_{test} = 1.0 MHz)		C_{ob}	—	500	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

TYPICAL DYNAMIC CHARACTERISTICS

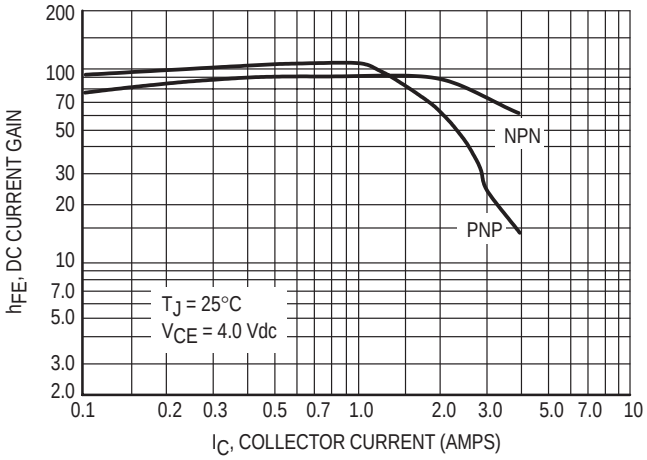


Figure 2. DC Current Gain

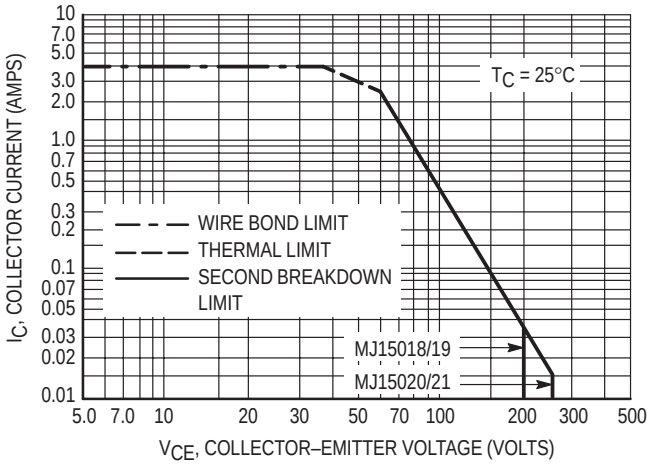


Figure 3. Maximum Rated Forward Biased Safe Operating Area

NPN
MJ15022
MJ15024*

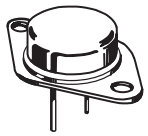
*Motorola Preferred Device

Silicon Power Transistors

The MJ15022 and MJ15024 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) —
  2 A @ 80 V
- High DC Current Gain —
  h_{FE} = 15 (Min) @ I_C = 8 Adc

16 AMPERE
SILICON
POWER TRANSISTORS
200 AND 250 VOLTS
250 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ15022	MJ15024	Unit
Collector–Emitter Voltage	V_{CEO}	200	250	Vdc
Collector–Base Voltage	V_{CBO}	350	400	Vdc
Emitter–Base Voltage	V_{EBO}	5		Vdc
Collector–Emitter Voltage	V_{CEX}	400		Vdc
Collector Current — Continuous Peak (1)	I_C	16 30		Adc
Base Current — Continuous	I_B	5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	MJ15022 MJ15024	$V_{CEO(sus)}$	 200 250	 — —	
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	 MJ15022 MJ15024	I_{CEX}	 — —	 250 250	µAdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 vdc, I_B = 0)	 MJ15022 MJ15024	I_{CEO}	 — —	 500 500	µAdc
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_B = 0)		I_{EBO}	—	500	µAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 0.5 s (non–repetitive)) (V_{CE} = 80 Vdc, t = 0.5 s (non–repetitive))		$I_{S/b}$	 5 2	 — —	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)		h_{FE}	 15 5	 60 —	—
Collector–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)		$V_{CE(sat)}$	 — —	 1.4 4.0	Vdc
Base–Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)		$V_{BE(on)}$	—	2.2	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	4	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)		C_{ob}	—	500	pF

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤ 2%.

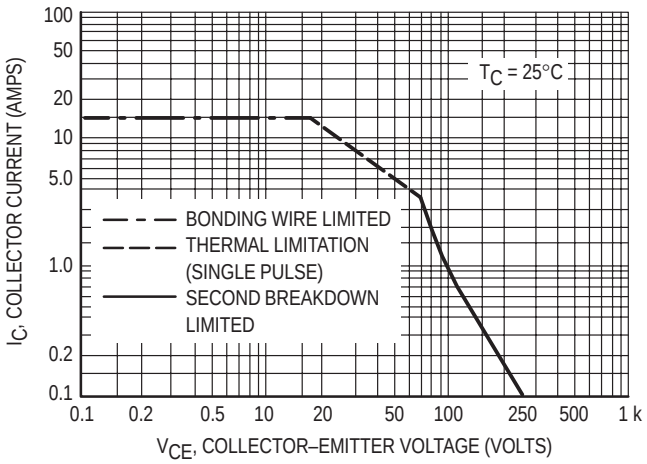


Figure 1. Active–Region Safe Operating Area

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values Ion than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

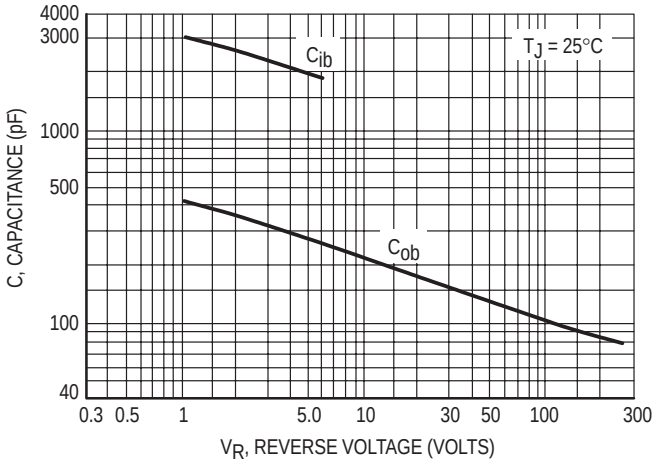


Figure 2. Capacitances

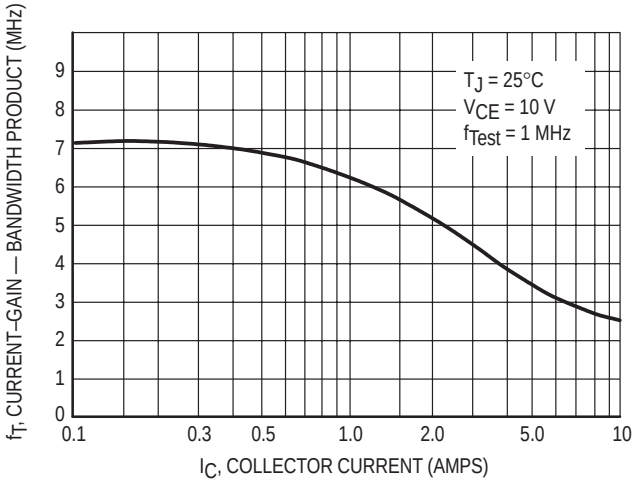


Figure 3. Current–Gain — Bandwidth Product

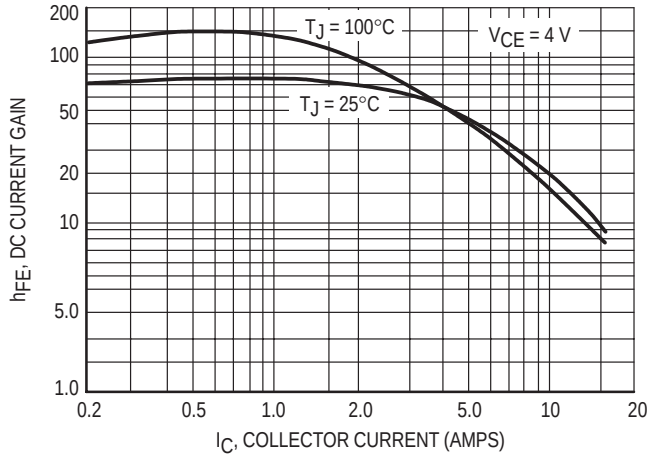


Figure 4. DC Current Gain

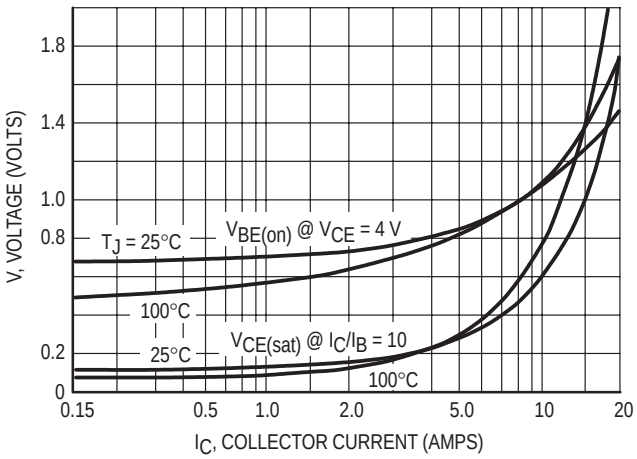


Figure 5. “On” Voltage

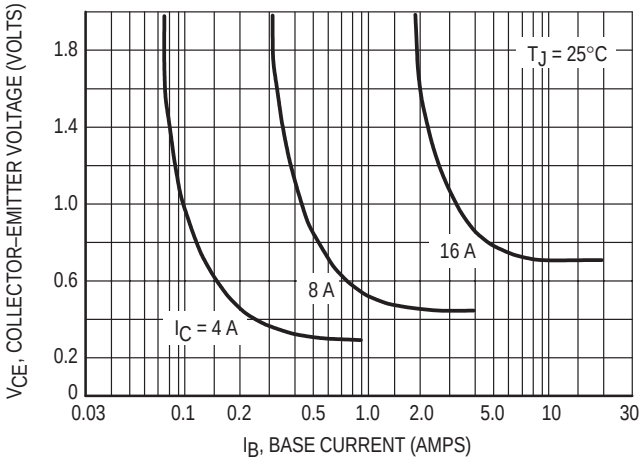


Figure 6. Collector Saturation Region

PNP
MJ15023
MJ15025*

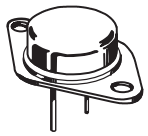
*Motorola Preferred Device

Silicon Power Transistors

The MJ15023 and MJ15025 are PowerBase power transistors designed for high power audio, disk head positioners and other linear applications.

- High Safe Operating Area (100% Tested) —
  2 A @ 80 V
- High DC Current Gain —
  h_{FE} = 15 (Min) @ I_C = 8 Adc

16 AMPERE
SILICON
POWER TRANSISTORS
200 AND 250 VOLTS
250 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	MJ15023	MJ15025	Unit
Collector–Emitter Voltage	V_{CEO}	200	250	Vdc
Collector–Base Voltage	V_{CBO}	350	400	Vdc
Emitter–Base Voltage	V_{EBO}	5		Vdc
Collector–Emitter Voltage	V_{CEX}	400		Vdc
Collector Current — Continuous Peak (1)	I_C	16 30		Adc
Base Current — Continuous	I_B	5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.70	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	MJ15023 MJ15025	$V_{CEO(sus)}$	 200 250	 — —	
Collector Cutoff Current (V_{CE} = 200 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	MJ15023 MJ15025	I_{CEX}	 — —	 250 250	μAdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 Vdc, I_B = 0)	MJ15023 MJ15025	I_{CEO}	 — —	 500 500	μAdc
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_B = 0)	Both	I_{EBO}	—	500	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 0.5 s (non–repetitive)) (V_{CE} = 80 Vdc, t = 0.5 s (non–repetitive))		$I_{S/b}$	 5 2	 — —	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 4 Vdc) (I_C = 16 Adc, V_{CE} = 4 Vdc)		h_{FE}	 15 5	 60 —	—
Collector–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)		$V_{CE(sat)}$	 —	 1.4 4.0	Vdc
Base–Emitter On Voltage (I_C = 8 Adc, V_{CE} = 4 Vdc)		$V_{BE(on)}$	—	2.2	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		f_T	4	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)		C_{ob}	—	600	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

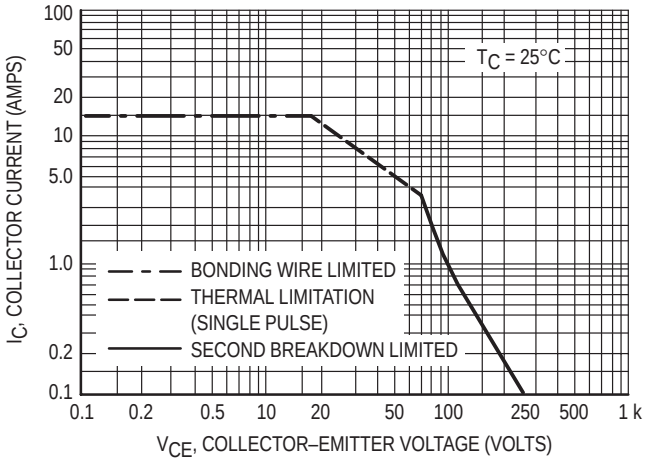


Figure 1. Active–Region Safe Operating Area

There are two limitations on the powerhandling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

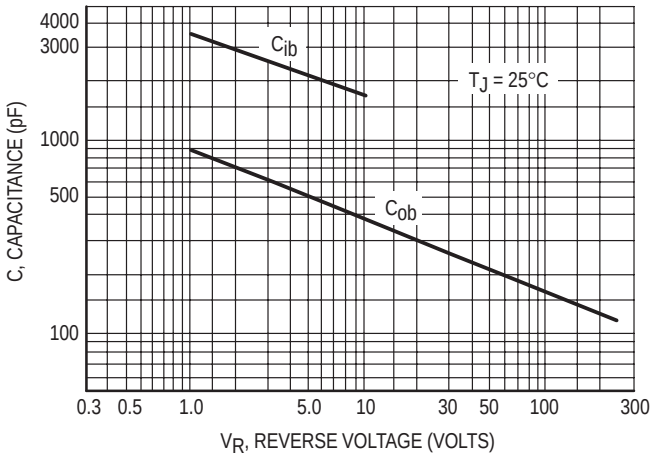


Figure 2. Capacitances

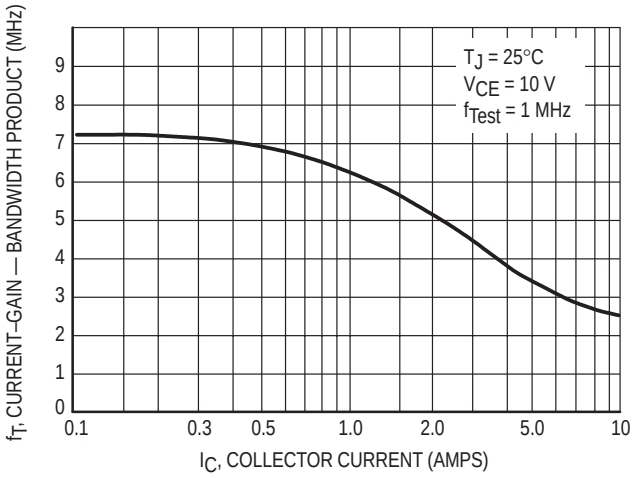


Figure 3. Current–Gain — Bandwidth Product

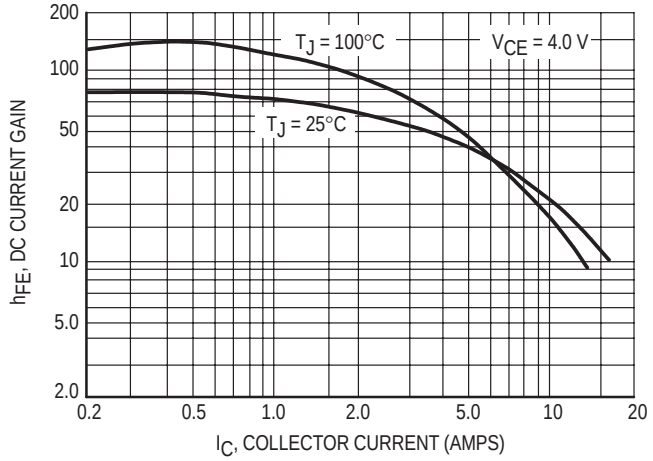


Figure 4. DC Current Gain

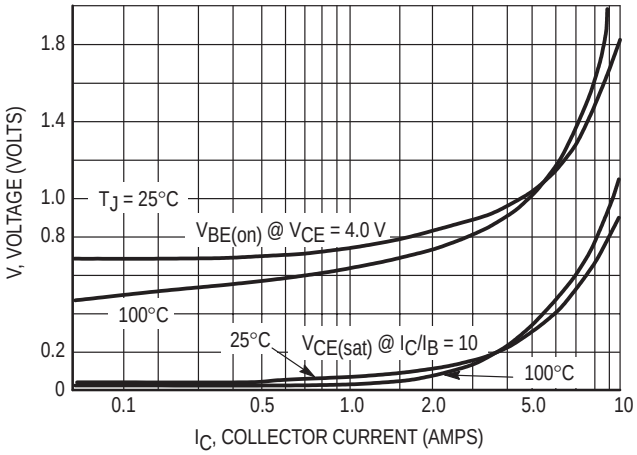


Figure 5. “On” Voltages

MJ16010
MJW16010
MJ16012*
MJW16012*

*Motorola Preferred Device

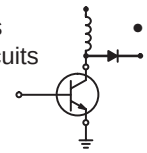
15 AMPERE
NPN SILICON
POWER TRANSISTORS
450 VOLTS
135 AND 175 WATTS

Designer's™ Data Sheet

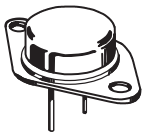
SWITCHMODE Series
NPN Silicon Power Transistors

These transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated switchmode applications. The MJ16012 and MJW16012 are selected high gain versions of the MJ16010 and MJW16010 for applications where drive current is limited.

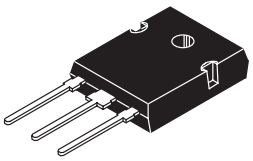
- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits



- Fast Turn–Off Times — T_C = 100°C
  50 ns Inductive Fall Time (Typ)
  90 ns Inductive Crossover Time (Typ)
  800 ns Inductive Storage Time (Typ)
- 100°C Performance Specified for:
  Reverse–Biased SOA with Inductive Loads
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents



CASE 1–07
TO–204AA
(TO–3)
MJ16010
MJ16012



CASE 340F–03
TO–247AE
MJW16010
MJW16012

MAXIMUM RATINGS

Rating	Symbol	MJ16010 MJ16012	MJW16010 MJW16012	Unit
Collector–Emitter Voltage	V_{CEO}	450		Vdc
Collector–Emitter Voltage	V_{CEV}	850		Vdc
Emitter–Base Voltage	V_{EB}	6.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	15 20		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	10 15		Adc
Total Device Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	 1 75 100 1.0	 135 53 8 1.11	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	0.93	°C/W
Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width ≤ 50 μs, Duty Cycle ≥ 10%

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	 — —	 — —	 0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)	I_{EBO}	—	—	10	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 16			
ON CHARACTERISTICS (1)					
Collector–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.7 Adc) (I_C = 10 Adc, I_B = 1.3 Adc) (I_C = 10 Adc, I_B = 1.3 Adc, T_C = 100°C)	$V_{CE(sat)}$	 — — —	 — — —	 2.5 3.0 3.0	Vdc
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.3 Adc) (I_C = 10 Adc, I_B = 1.3 Adc, T_C = 100°C)	$V_{BE(sat)}$	 — —	 — —	 1.5 1.5	Vdc
DC Current Gain (I_C = 15 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	5.0	—	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)	C_{ob}	—	—	400	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	(I_C = 10 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.3 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%)	(I_{B2} = 2.6 Adc, R_{B2} = 1.6 Ω)	t_d	—	20	—	ns
Rose Time			t_r	—	200	—	
Storage Time			t_s	—	1200	—	
Fall Time			t_f	—	200	—	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	650	—	
Fall Time			t_f	—	80	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 10 Adc, I_{B1} = 1.3 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	800	1800	ns
Fall Time			t_{fi}	—	50	200	
Crossover Time			t_c	—	90	250	
Storage Time		(T_C = 150°C)	t_{sv}	—	1050	—	
Fall Time			t_{fi}	—	70	—	
Crossover Time			t_c	—	120	—	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector–Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)			$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc. T_C = 100°C)			I_{CEV}	 — —	 — —	 0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)			I_{EBO}	—	—	10	mAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$	See Figure 15			
Clamped Inductive SOA with Base Reverse Biased			RBSOA	See Figure 16			
ON CHARACTERISTICS (1)							
Collector–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.7 Adc) (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 1.0 Adc, T_C = 100°C)			$V_{CE(sat)}$	 — — —	 — — —	 2.5 3.0 3.0	Vdc
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1.0 Adc) (I_C = 10 Adc, I_B = 1.0 Adc, T_C = 100°C)			$V_{BE(sat)}$	 — —	 — —	 1.5 1.5	Vdc
DC Current Gain (I_C = 15 Adc, V_{CE} = 5.0 Vdc)			h_{FE}	7.0	—	—	—
DYNAMIC CHARACTERISTICS							
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)			C_{ob}	—	—	400	pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	(I_C = 10 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.0 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%)	(I_{B2} = 2.0 Adc, R_{B2} = 1.6 Ω)	t_d	—	20	—	ns
Rose Time			t_r	—	200	—	
Storage Time			t_s	—	900	—	
Fall Time			t_f	—	150	—	
Storage Time		($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	500	—	
Fall Time			t_f	—	40	—	
Inductive Load (Table 2)							
Storage Time	(I_C = 10 Adc, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_C = 100°C)	t_{sv}	—	650	1500	ns
Fall Time			t_{fi}	—	30	150	
Crossover Time			t_c	—	50	200	
Storage Time		(T_C = 150°C)	t_{sv}	—	850	—	
Fall Time			t_{fi}	—	30	—	
Crossover Time			t_c	—	70	—	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%

TYPICAL STATIC CHARACTERISTICS

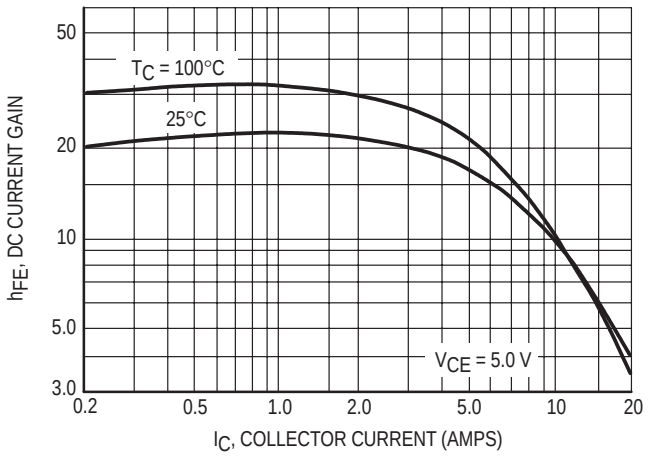


Figure 1. DC Current Gain

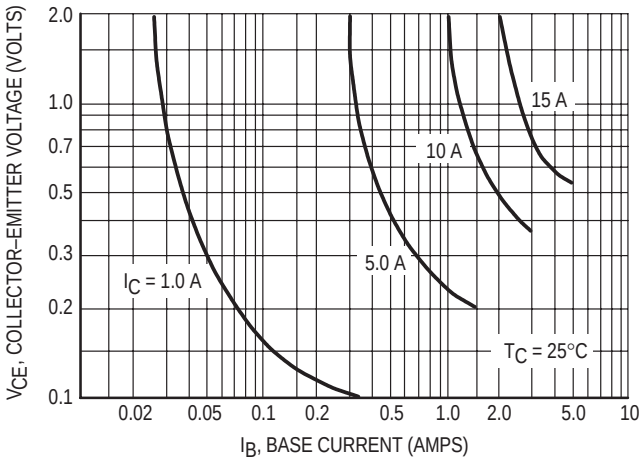


Figure 2. Collector Saturation Region

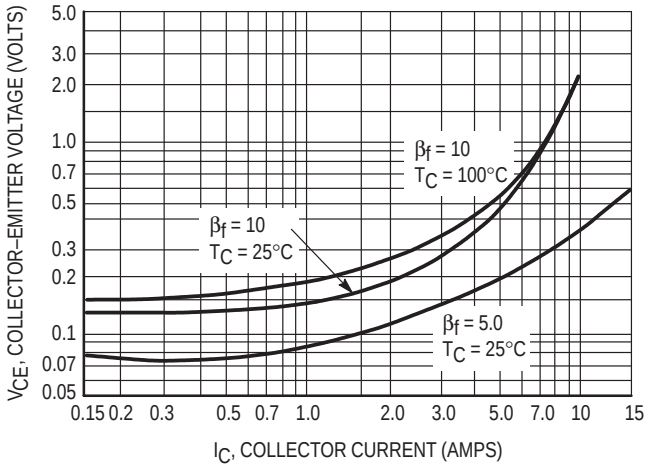


Figure 3. Collector–Emitter Saturation Voltage

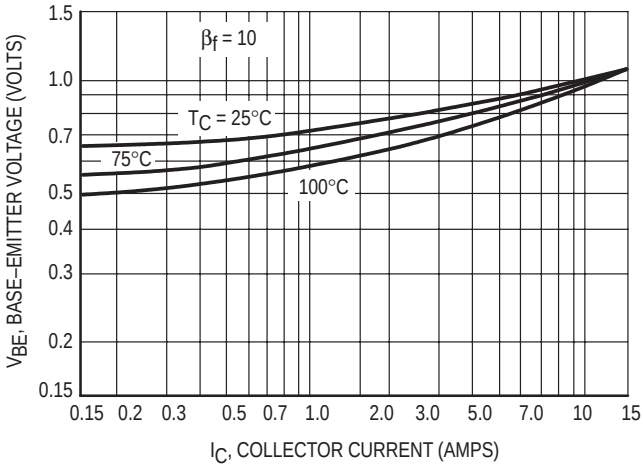


Figure 4. Base–Emitter Voltage

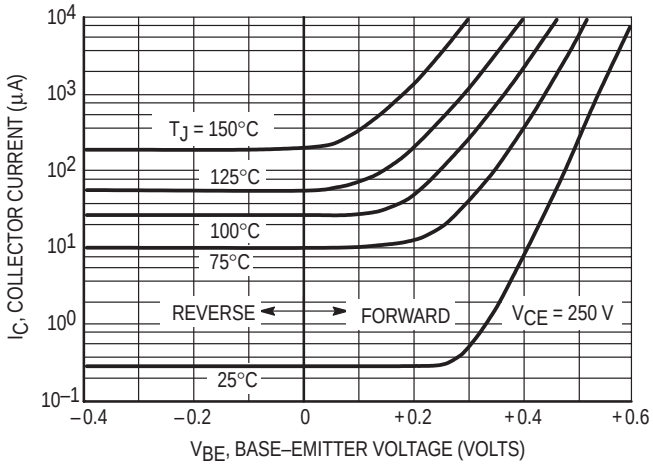


Figure 5. Collector Cutoff Region

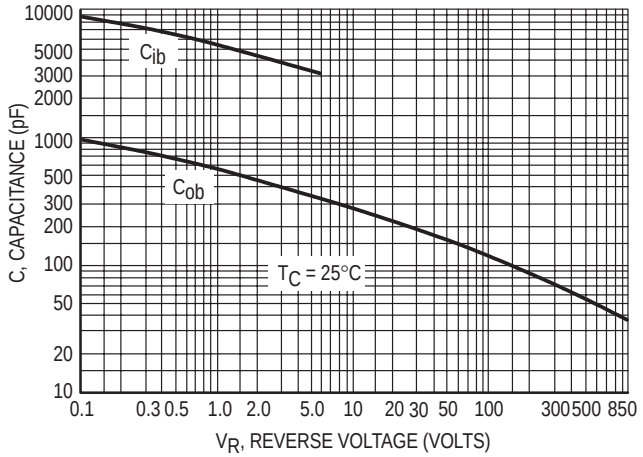


Figure 6. Capacitance

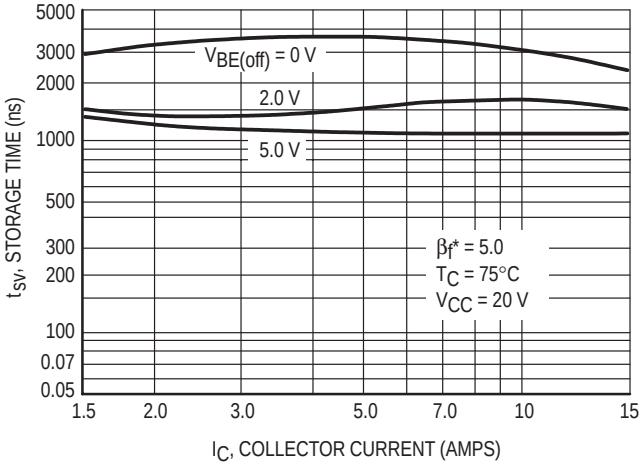


Figure 7. Storage Time

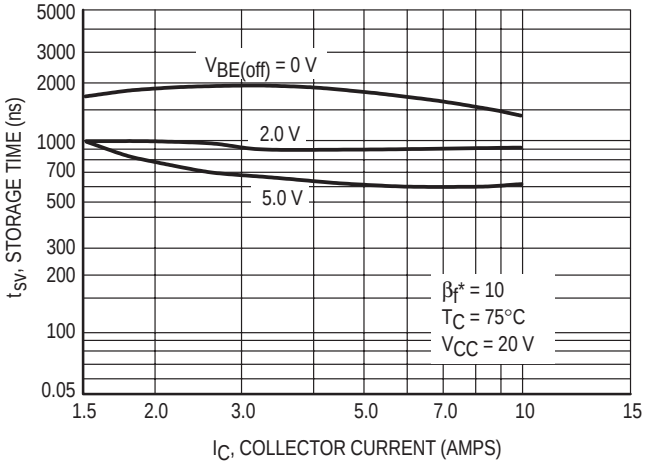


Figure 8. Storage Time

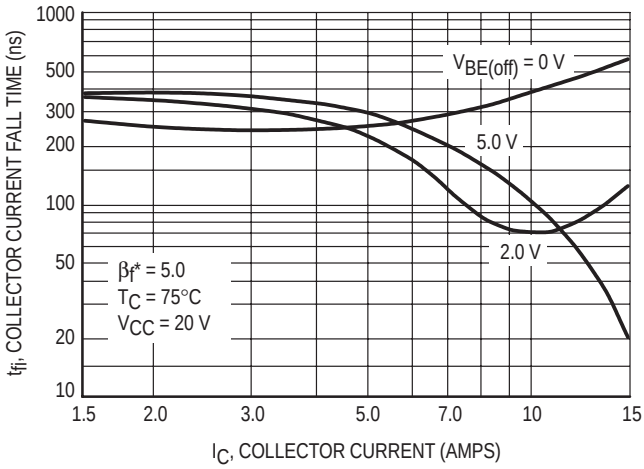


Figure 9. Collector Current Fall Time

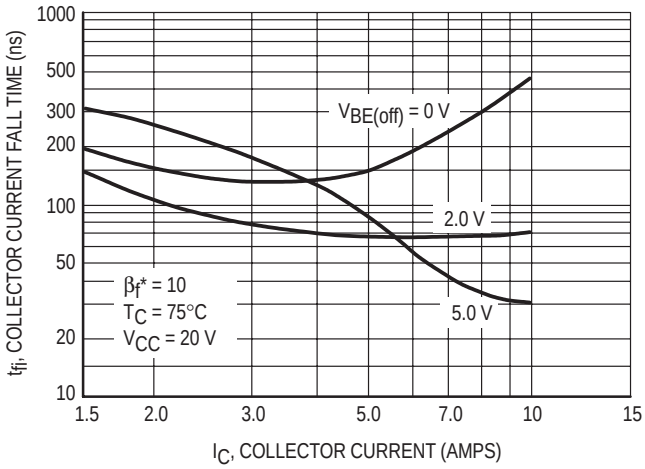


Figure 10. Collector Current Fall Time

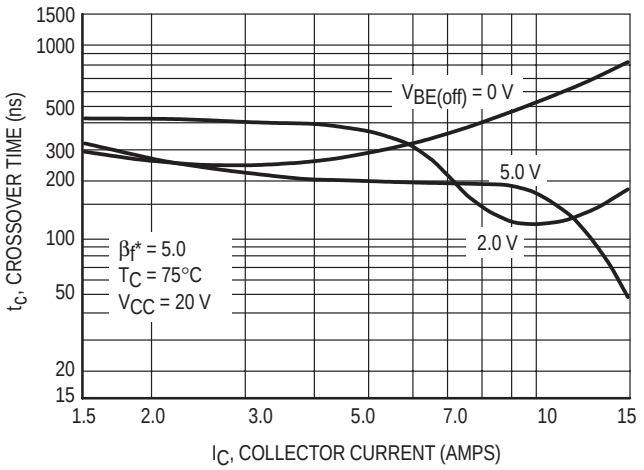


Figure 11. Crossover Time

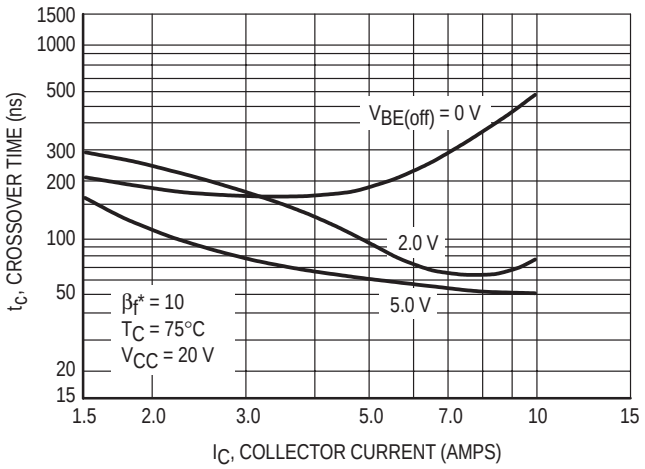


Figure 12. Crossover Time

$$*\beta_f = \frac{I_C}{I_{B1}}$$

GUARANTEED SAFE OPERATING AREA LIMITS

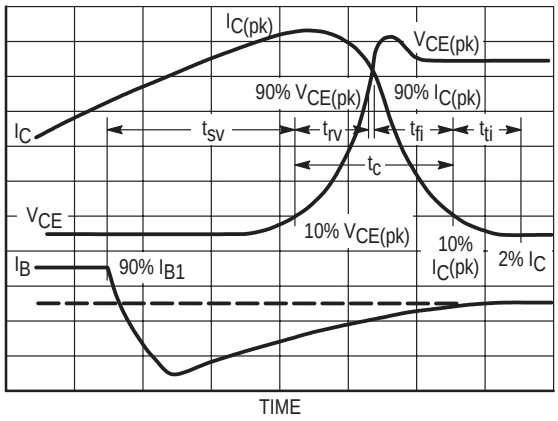


Figure 13. Inductive Switching Measurements

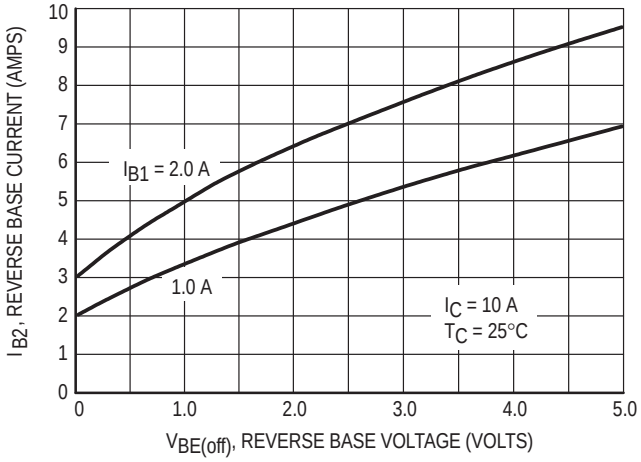


Figure 14. Peak Reverse Base Current

SAFE OPERATING AREA INFORMATION

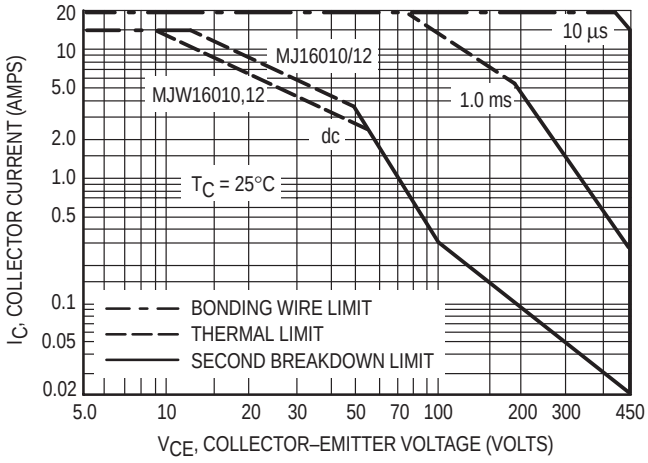


Figure 15. Maximum Forward Bias Safe Operating Area

$^*\beta_f = \frac{I_C}{I_{B1}}$

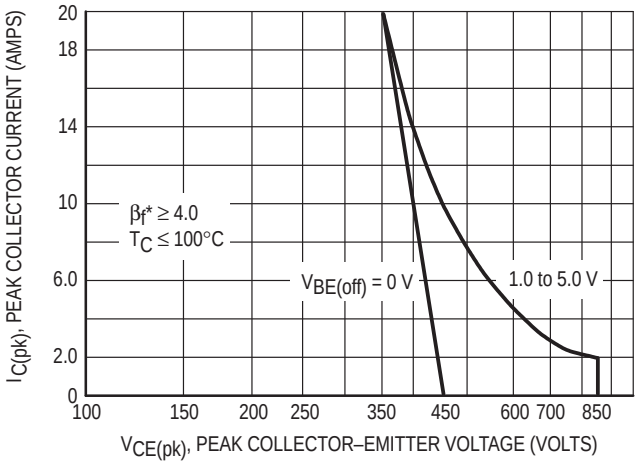


Figure 16. Maximum Reverse Bias Safe Operating Area

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 18.

$T_{J(pk)}$ may be calculated from the data in Figure 17. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 16 gives the RBSOA characteristics.

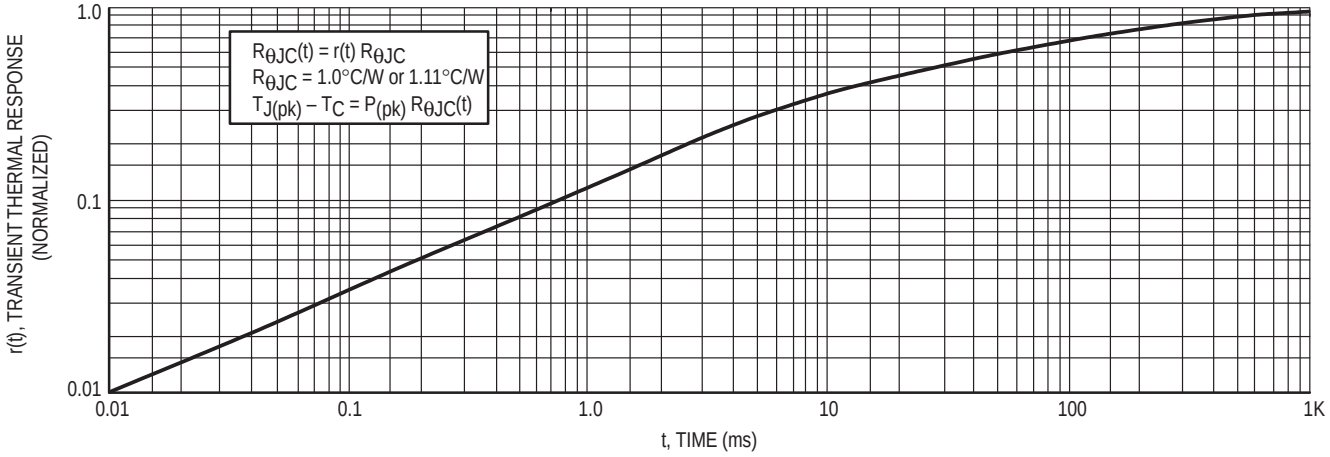


Figure 17. Thermal Response

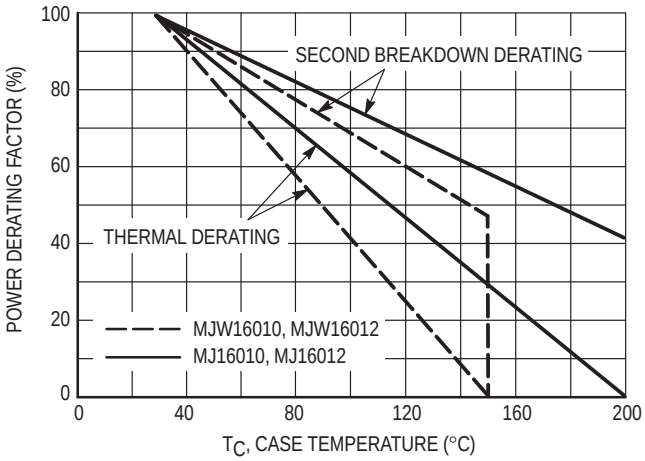
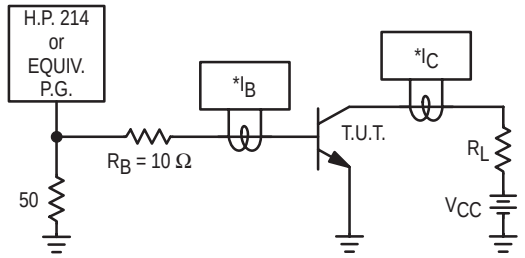


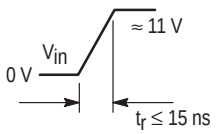
Figure 18. Power Derating

Table 1. Resistive Load Switching

t_d and t_r

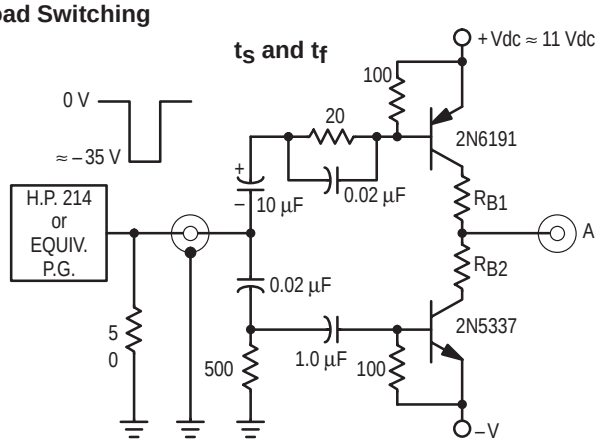


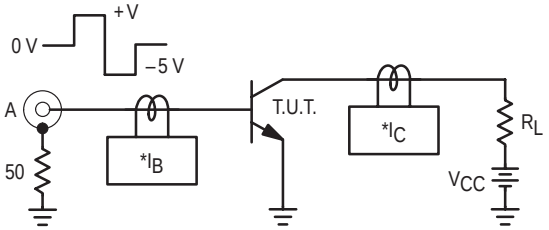
V_{CC} = 250 Vdc
R_L = 25 Ω
I_C = 10 Adc
I_B = 1.0 Adc



*Tektronix AM503
P6302 or Equivalent

t_s and t_f

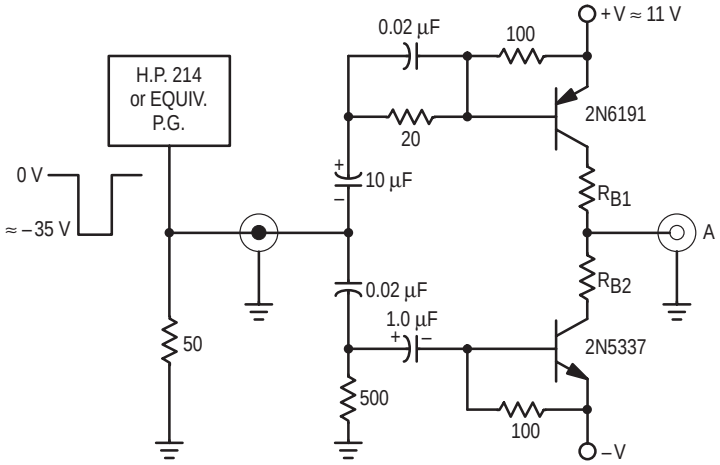


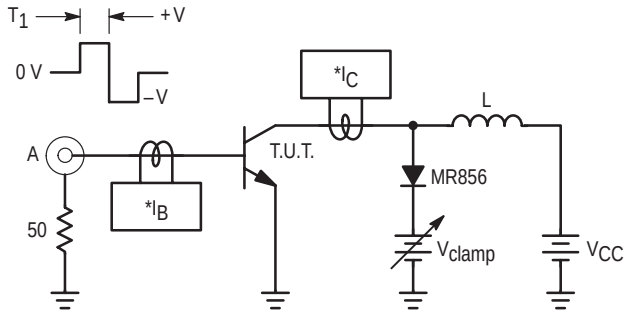


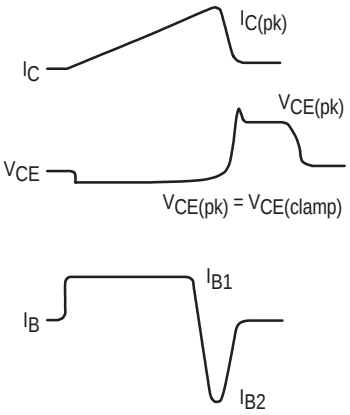
V_{CC} = 250 Vdc	I_{B1} = 1.0 Adc	R_{B1} = 10 Ω
R_L = 25 Ω	I_{B2} = 2.0 Adc	R_{B2} = 1.6 Ω
I_C = 10 Adc	For $V_{BE(off)}$ = 5.0 V, R_{B2} = 0 Ω	

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

Table 2. Inductive Load Switching







$t_1 \approx \frac{L_{coil}\ (I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{CEO(sus)}$
L = 10 mH
R_{B2} = ∞
V_{CC} = 20 V Its

*Tektronix AM503
P6302 or Equivalent

Inductive Switching
L = 200 µH
R_{B2} = 0
V_{CC} = 20 V
R_{B1} selected for desired I_{B1}

Scope — Tektronix
7403 or Equivalent

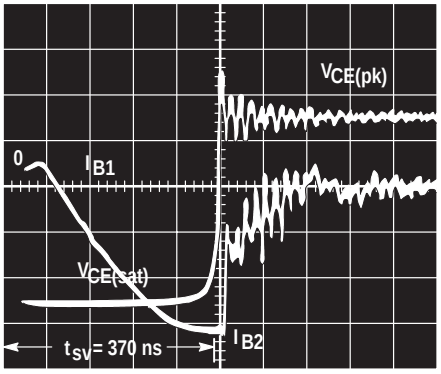
RBSOA
L = 200 µH
R_{B2} = 0
V_{CC} = 20 V
R_{B1} selected for desired I_{B1}

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

TYPICAL INDUCTIVE SWITCHING WAVEFORMS

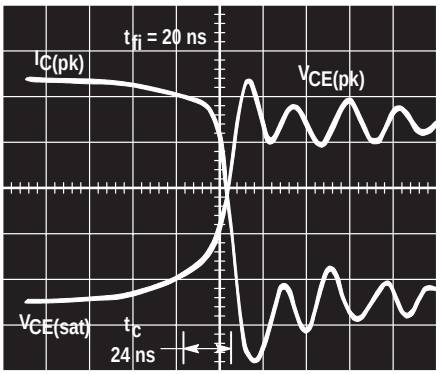
t_{sv}

$I_{C(pk)}$ = 10 A
I_{B1} = 1.0 A
$V_{BE(off)}$ = 5.0 V
$V_{CE(pk)}$ = 400 V
T_C = 25°C
Time Base =
100 ns/cm



t_{fi}, t_c

$I_{C(pk)}$ = 10 A
I_{B1} = 1.0 A
$V_{BE(off)}$ = 5.0 V
$V_{CE(pk)}$ = 400 V
T_C = 25°C
Time Base =
20 ns/cm



MJ16018*
MJW16018*

*Motorola Preferred Device

POWER TRANSISTORS
10 AMPERES
800 VOLTS
125 AND 175 WATTS

Designer's™ Data Sheet

NPN Silicon Power Transistors

1.5 kV SWITCHMODE Series

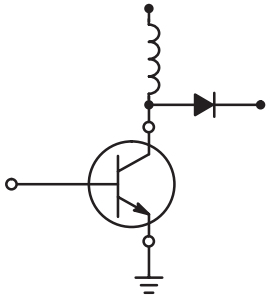
These transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated switchmode applications.

Typical Applications:

- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

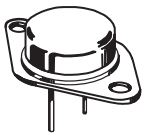
Features:

- Collector–Emitter Voltage — V_{CEV} = 1500 Vdc
- Fast Turn–Off Times
  - 80 ns Inductive Fall Time — 100°C (Typ)
  - 110 ns Inductive Crossover Time — 100°C (Typ)
  - 4.5 μs Inductive Storage Time — 100°C (Typ)
- 100°C Performance Specified for:
  - Reverse–Biased SOA with Inductive Load
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents

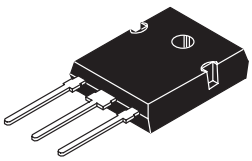


MAXIMUM RATINGS

Rating	Symbol	MJ16018	MJW16018	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	800		Vdc
Collector–Emitter Voltage	V_{CEV}	1500		Vdc
Emitter–Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	10 15		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	8 12		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above T_C = 25°C	P_D	 175 100 1	 125 50 1	 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 200	–55 to 150	°C



CASE 1–07
TO–204AA
MJ16018



CASE 340F–03
TO–247AE
MJW16018

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	1	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS(1)							
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 50 mA, I_B = 0)			$V_{CEO(sus)}$	800	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 1500 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 1500 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			I_{CEV}	 — —	 — —	 0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)			I_{EBO}	—	—	0.1	mAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$	See Figure 13			
Clamped Inductive SOA with Base Reverse Biased			RBSOA	See Figure 14			
ON CHARACTERISTICS(1)							
Collector–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 2 Adc) (I_C = 10 Adc, I_B = 5 Adc) (I_C = 5 Adc, I_B = 2 Adc, T_C = 100°C)			$V_{CE(sat)}$	 — — —	 — — —	 1 5 1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 2 Adc) (I_C = 5 Adc, I_B = 2 Adc, T_C = 100°C)			$V_{BE(sat)}$	— —	— —	1.5 1.5	Vdc
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc)			h_{FE}	4	—	—	—
DYNAMIC CHARACTERISTICS							
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 kHz)			C_{ob}	—	—	450	pF
SWITCHING CHARACTERISTICS							
Inductive Load (Table 1)							
Storage Time	Baker Clamped (I_C = 5 Adc, I_{B1} = 2 Adc, $V_{BE(off)}$ = 2 Vdc, $V_{CE(pk)}$ = 400 Vdc) PW = 25 µs	(T_J = 25°C)	t_{sv}	—	4000	8000	ns
Fall Time			t_{fi}	—	60	200	
Crossover Time			t_c	—	90	300	
Storage Time		(T_J = 100°C)	t_{sv}	—	4500	9000	
Fall Time			t_{fi}	—	80	250	
Crossover Time			t_c	—	110	375	
Resistive Load (Table 1)							
Delay Time	Baker Clamped (I_C = 5 Adc, V_{CC} = 250 Vdc, I_{B1} = 2 Adc, I_{B2} = 2 Adc, R_{B2} = 3 Ω, PW = 25 µs, Duty Cycle ≤ 2%)		t_d	—	85	200	ns
Rise Time			t_r	—	900	2000	
Storage Time			t_s	—	4500	9000	
Fall Time			t_f	—	200	400	

(1) Pulse Test: PW = 300 µs, Duty Cycle ≤ 2%.

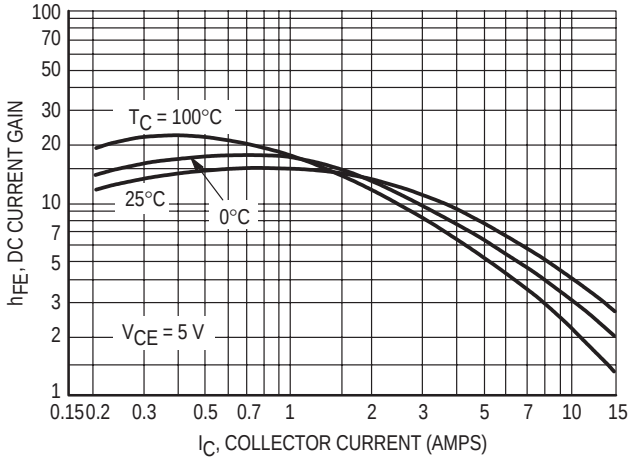


Figure 1. DC Current Gain

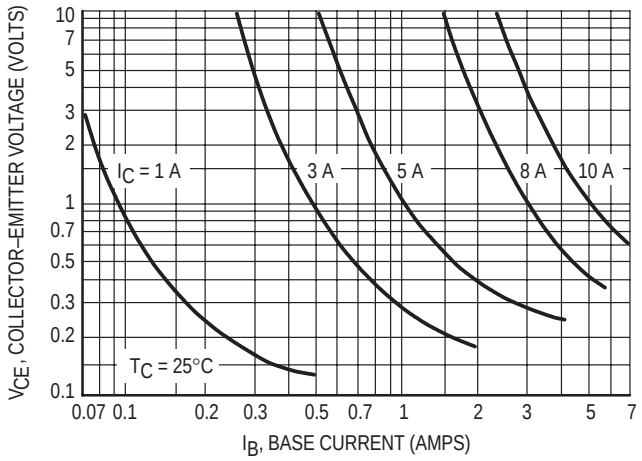


Figure 2. Collector Saturation Region

TYPICAL STATIC CHARACTERISTICS

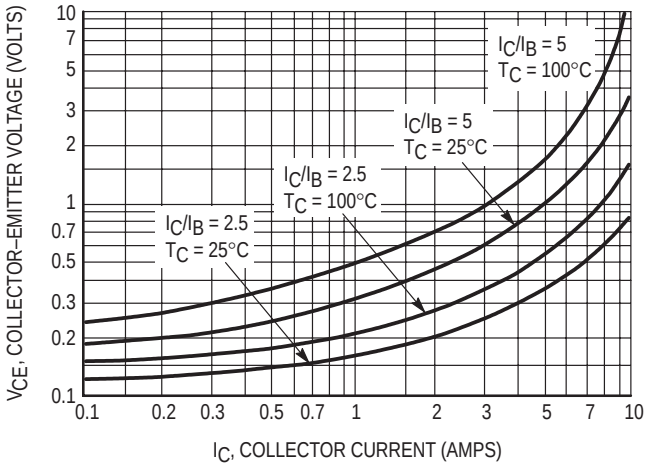


Figure 3. Collector–Emitter Saturation Region

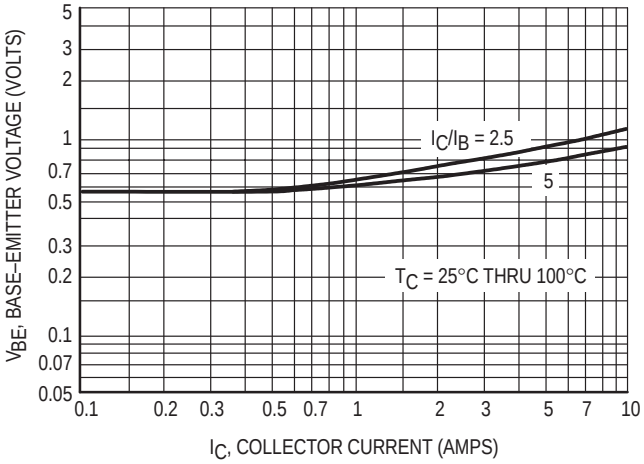


Figure 4. Base–Emitter Saturation Region

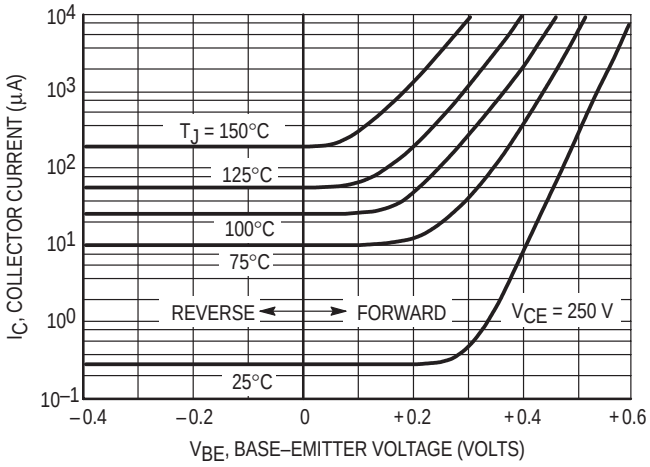


Figure 5. Collector Cutoff Region

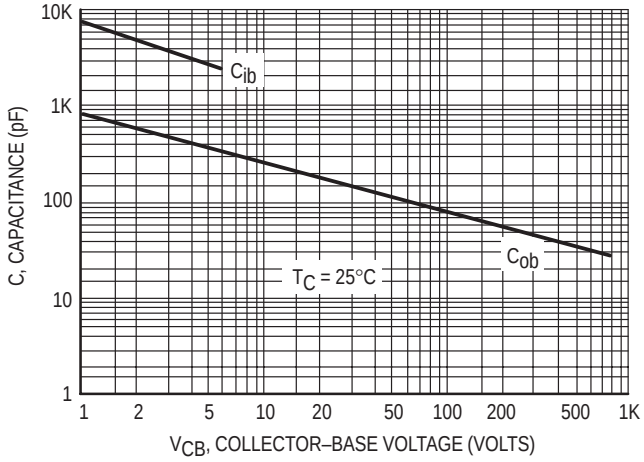


Figure 6. Typical Capacitance

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

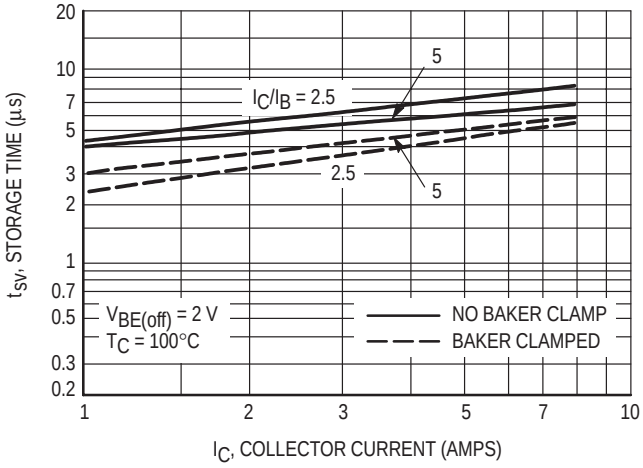


Figure 7. Storage Time

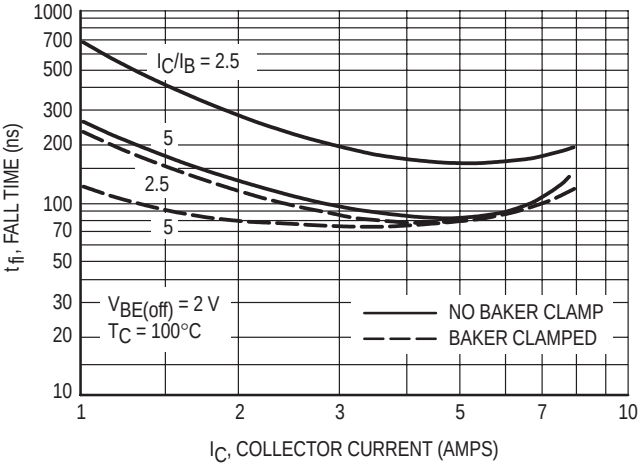


Figure 8. Inductive Switching Fall Time

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

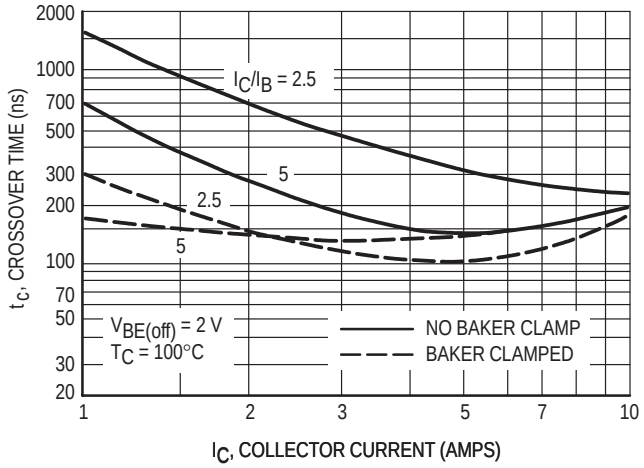


Figure 9. Inductive Switching Crossover Time

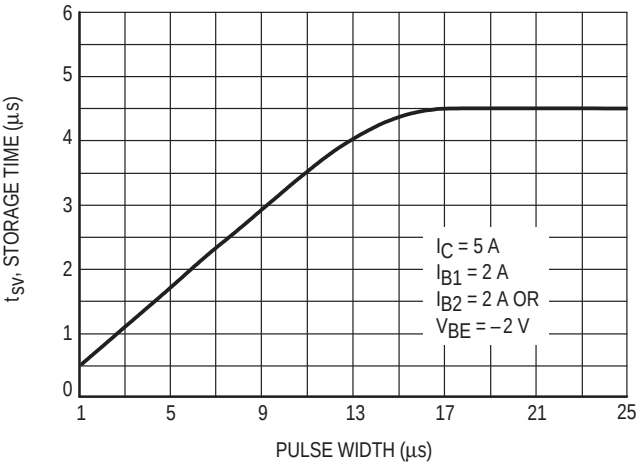


Figure 10. (t_{sv}) Storage Time versus I_{B1} Pulse Width

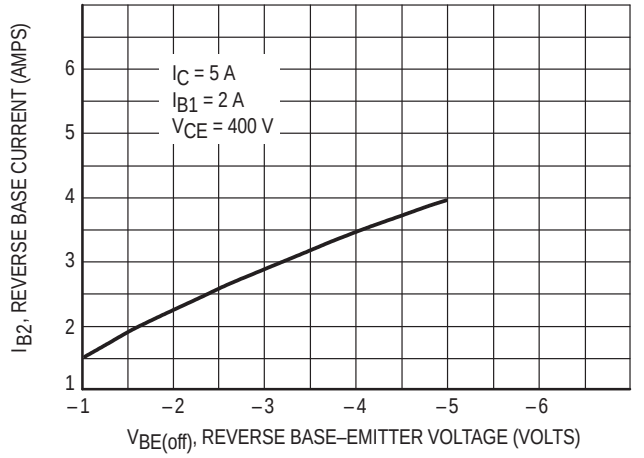


Figure 11. Reverse Base Current versus Off Voltage

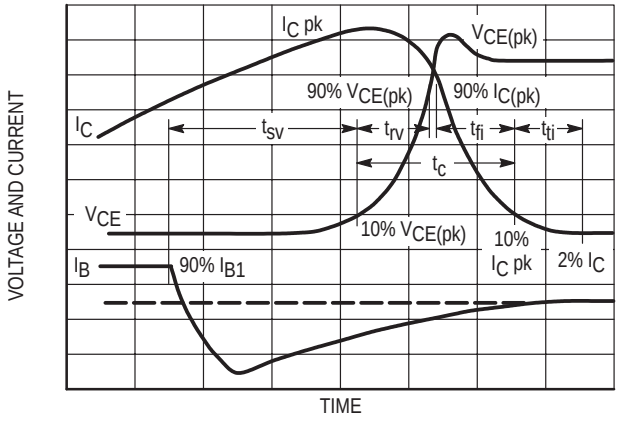


Figure 12. Inductive Switching Measurements

GUARANTEED SAFE OPERATING AREA LIMITS

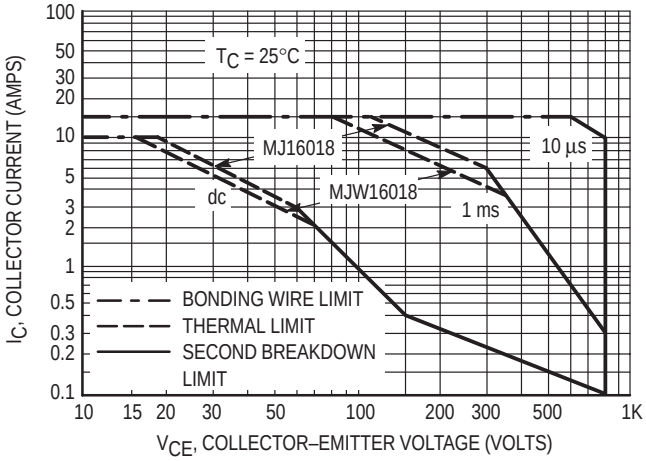


Figure 13. Maximum Forward Bias Safe Operating Area

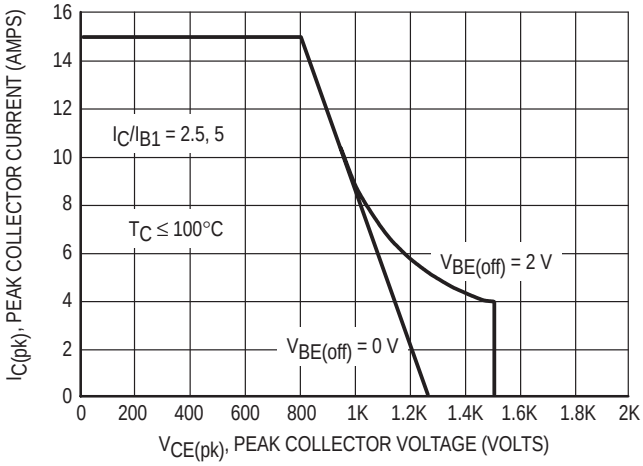


Figure 14. Maximum Reverse Bias Safe Operating Area

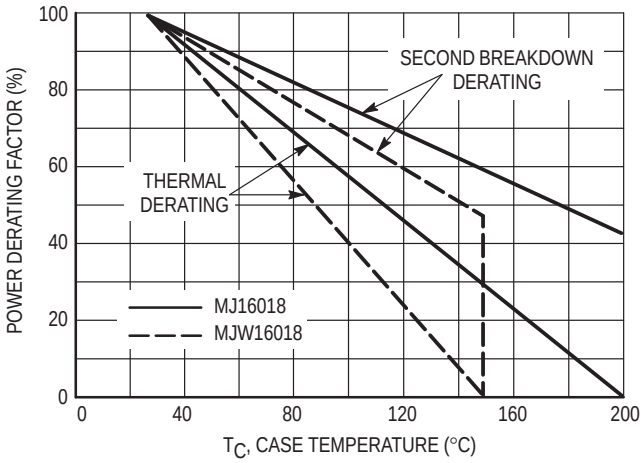


Figure 15. Power Derating

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 16. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

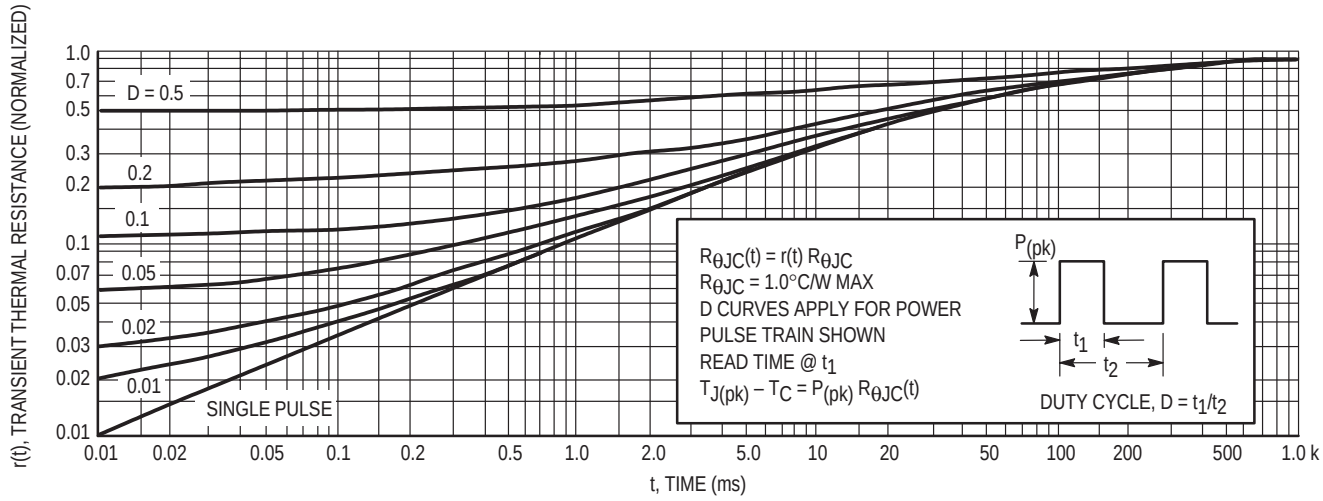
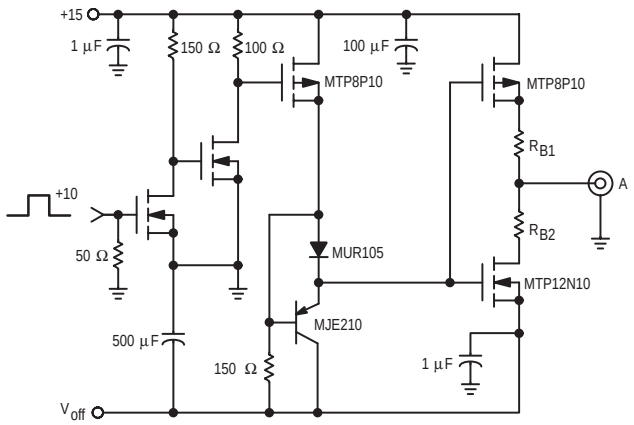
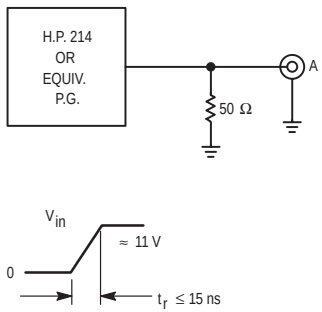
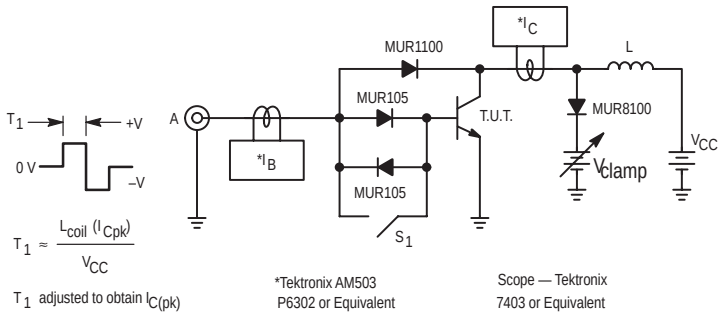
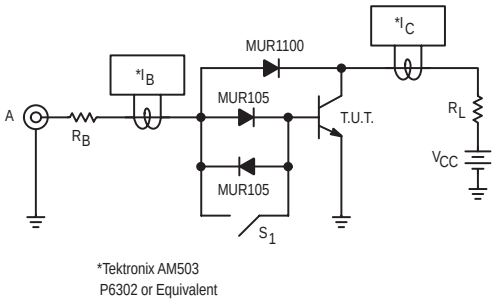


Figure 16. Thermal Response

Table 1. Test Conditions for Dynamic Performance

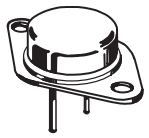
	$V_{CEO(sus)}$	RBSOA	Inductive Switching	Resistive Switching
Input Conditions	**Drive Circuit**  Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A			**For t_d and t_f :**  **For t_s and t_f :** Inductive Switching Drive Circuit
Circuit Values	L = 10 mH R_{B2} = ∞ V_{CC} = 20 Volts $I_{(pk)}$ = 50 mA S_1 Closed	L = 200 µH R_{B2} = 0 V_{CC} = 20 Volts R_{B1} selected for desired I_{B1} S_1 Closed	L = 200 µH R_{B2} = 0 when $V_{BE(off)}$ is specified or selected for desired I_{B2} V_{CC} ≈ 20 Volts, Adjusted to obtain desired IC R_{B1} selected for desired I_{B1} S_1 = Open for baker clamp condition	**for t_d and t_r** V_{CC} = 250 Volts R_B selected for desired I_{B1} R_L selected for desired I_C **for t_s and t_f** V_{CC} = 250 Volts R_B = 0 R_{B1} & R_{B2} selected for I_{B1} & I_{B2} R_L selected for desired I_C
Test Circuit	 			

MJ16020
MJ16022

Advance Information

SWITCHMODE Series
NPN Silicon Power Transistors

NPN SILICON POWER TRANSISTOR
30 AMPERES
450 VOLTS



CASE 197A–05
TO–204AE

These transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated switchmode applications. The MJ16022 is a selected high–gain version of the MJ16020 for applications where drive current is limited.

Features:

- Fast Switching Times:
  - 30 ns (Typ) Inductive Fall Time
  - 50 ns (Typ) Inductive Crossover Time
  - 800 ns (Typ) Inductive Storage Time
- 100°C Performance Specified for:
  - Reverse–Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages

Typical Applications:

- Switching Regulators
- Inverters
- Solenoids and Relay Drivers
- Motor Controls
- Deflection Circuits

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Max	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector–Emitter Breakdown Voltage	V_{CEV}	850	Vdc
Emitter–Base Voltage	V_{EB}	6	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	30 40	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	20 30	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.42	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS*						
Collector–Emitter Sustaining Voltage (I_C = 1 mA, I = 0)		$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ohms, T_C = 100°C)		I_{CER}	—	—	—	mAdc
Collector Cutoff Current		I_{CES}				nAdc
(V_{CE} = 850 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	@ T_C = 25°C		—	—	0.5	
(V_{CE} = 850 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	@ T_C = 100°C		—	—	5	
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)		I_{EBO}	—	—	2	nAdc
ON CHARACTERISTICS*						
Base–Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 20 Adc, I_B = 2 Adc)			—	—	1.5	
(I_C = 20 Adc, I_B = 2 Adc)	@ T_C = 100°C		—	—	1.5	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 20 Adc, I_B = 1.4 Adc)	@ T_C = 25°C		—	—	2.5	
(I_C = 20 Adc, I_B = 2.6 Adc)	@ T_C = 25°C		—	—	3	
(I_C = 20 Adc, I_B = 2.6 Adc)	@ T_C = 100°C		—	—	3	
DC Current Gain		h_{FE}				—
(I_C = 30 Adc, V_{CE} = 5 Vdc)	MJ16020		5	—	—	
	MJ16022		7	—	—	
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)		C_{ob}	—	—	800	pF

* Indicates Pulse Test: Pulse Width = 300 μs Max, Duty Cycle = 2%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: MJ16020							
Resistive Load							
Delay Time	(V_{CC} = 250 Vdc, I_C = 20 Adc, I_{B1} = 2.6 Adc, t_p = 30 μs, Duty Cycle < 2%)	I_{B2} = 5.2 Adc, R_B = 1.6 Ohm	t_d	—	20	—	ns
Rise Time			t_r	—	200	—	
Storage Time			t_s	—	1200	—	
Fall Time			t_f	—	200	—	
Storage Time		($V_{BE(off)}$ = 5 Vdc)	t_s	—	650	—	
Fall Time			t_f	—	80	—	
Inductive Load							
Storage Time	(I_C = 20 A, I_{B1} = 2.6 Adc, $V_{CE(pk)}$ = 400 V, $V_{BE(off)}$ = 5 Vdc)	(T_C = 100°C)	t_{sv}	—	800	2000	ns
Crossover Time			t_{fi}	—	50	200	
Fall Time			t_c	—	90	250	
Storage Time	(I_C = 20 A, I_{B1} = 2.6 Adc, $V_{CE(pk)}$ = 400 V, $V_{BE(off)}$ = 5 Vdc)	(T_C = 150°C)	t_{sv}	—	1050	—	
Crossover Time			t_{fi}	—	70	—	
Fall Time			t_c	—	120	—	
SWITCHING CHARACTERISTICS: MJ16022							
Resistive Load							
Delay Time	(V_{CC} = 250 Vdc, I_C = 20 Adc, I_{B1} = 2.6 Adc, t_p = 30 μs, Duty Cycle < 2%)	I_{B2} = 5.2 Adc, R_B = 1.6 Ohm	t_d	—	20	—	ns
Rise Time			t_r	—	200	—	
Storage Time			t_s	—	900	—	
Fall Time			t_f	—	150	—	
Storage Time		($V_{BE(off)}$ = 5 Vdc)	t_s	—	500	—	
Fall Time			t_f	—	40	—	
Inductive Load							
Storage Time	(I_C = 20 A, I_{B1} = 2.6 Adc, $V_{CE(pk)}$ = 400 V, $V_{BE(off)}$ = 5 Vdc)	(T_C = 100°C)	t_{sv}	—	650	1700	ns
Crossover Time			t_{fi}	—	30	150	
Fall Time			t_c	—	50	200	
Storage Time	(I_C = 20 A, I_{B1} = 2.6 Adc, $V_{CE(pk)}$ = 400 V, $V_{BE(off)}$ = 5 Vdc)	(T_C = 150°C)	t_{sv}	—	850	—	
Crossover Time			t_{fi}	—	30	—	
Fall Time			t_c	—	70	—	

MJ16110*
MJW16110*

*Motorola Preferred Device

POWER TRANSISTORS
15 AMPERES
400 VOLTS
175 AND 135 WATTS

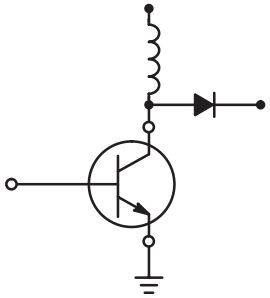
Designer's™ Data Sheet

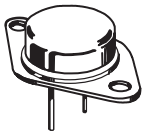
NPN Silicon Power Transistors

SWITCHMODE Bridge Series

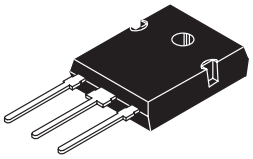
. . . specifically designed for use in half bridge and full bridge off line converters.

- Excellent Dynamic Saturation Characteristics
- Rugged RBSOA Capability
- Collector–Emitter Sustaining Voltage — $V_{CEO(sus)}$ — 400 V
- Collector–Emitter Breakdown — $V_{(BR)CES}$ — 650 V
- State–of–Art Bipolar Power Transistor Design
- Fast Inductive Switching:
  - t_{fi} = 25 ns (Typ) @ 100°C
  - t_c = 50 ns (Typ) @ 100°C
  - t_{sv} = 1 μs (Typ) @ 100°C
- Ultrafast FBSOA Specified
- 100°C Performance Specified for:
  - RBSOA
  - Inductive Load Switching
  - Saturation Voltages
  - Leakages





CASE 1–07
TO–204AA
(FORMERLY TO–3)
MJ16110



CASE 340F–03
TO–247AE
MJW16110

MAXIMUM RATINGS

Rating	Symbol	MJ16110	MJW16110	Unit
Collector–Emitter Sustaining Voltage	$V_{CEO(sus)}$	400		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	650		Vdc
Emitter–Base Voltage	V_{EBO}	6		Vdc
Collector Current — Continuous — Pulsed (1)	I_C I_{CM}	15 20		Adc
Base Current — Continuous — Pulsed (1)	I_B I_{BM}	10 15		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derated above 25°C	P_D	 175 100 1	 135 54 1.09	 Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 200	–55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	1	0.92	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)							
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 20 mAdc, I_B = 0)			$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CE} = 650 Vdc, $V_{BE(off)}$ = 1.5 V) (V_{CE} = 650 Vdc, $V_{BE(off)}$ = 1.5 V, T_C = 100°C)			I_{CEV}	 — —	 — —	 100 1000	μAdc
Collector Cutoff Current (V_{CE} = 650 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	—	1000	μAdc
Emitter–Base Leakage (V_{EB} = 6 Vdc, I_C = 0)			I_{EBO}	—	—	10	μAdc
ON CHARACTERISTICS (1)							
Collector–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 0.5 Adc) (I_C = 10 Adc, I_B = 1.2 Adc) (I_C = 10 Adc, I_B = 2 Adc) (I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)			$V_{CE(sat)}$	 — — — —	 0.3 0.7 0.3 0.4	 0.9 2.0 1.0 1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2 Adc) (I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)			$V_{BE(sat)}$	 — —	 1.2 1.2	 1.5 1.5	Vdc
DC Current Gain (I_C = 15 Adc, V_{CE} = 5 Vdc)			h_{FE}	6	12	20	—
DYNAMIC CHARACTERISTICS							
Dynamic Saturation			$V_{CE(dsat)}$	See Figures 11, 12, and 13			V
Output Capacitance (V_{CE} = 10 Vdc, I_E = 0, f_{test} = 1 kHz)			C_{ob}	—	—	400	pF
SWITCHING CHARACTERISTICS							
Inductive Load (Table 1)							
Storage	I_C = 10 A, I_{B1}= 1 A, $V_{BE(off)}$ = 5 V, $V_{CE(pk)}$ = 250 V	T_J = 25°C	t_{sv}	—	700	1500	ns
Crossover			t_c	—	45	150	
Fall Time			t_{fi}	—	20	75	
Storage		T_J = 100°C	t_{sv}	—	1000	2000	
Crossover			t_c	—	50	200	
Fall Time			t_{fi}	—	25	125	
Resistive Load (Table 2)							
Delay Time	I_C = 10 A, I_{B1} = 1 A, V_{CC} = 250 V, PW = 30 μs, Duty Cycle = ≤ 2%	I_{B2} = 2 A, R_{B2} = 4 Ω	t_d	—	15	—	ns
Rise Time			t_r	—	330	—	
Storage Time			t_s	—	800	—	
Fall Time			t_f	—	110	—	
Storage Time		$V_{BE(off)}$ = 5 V	t_s	—	500	—	
Fall Time			t_f	—	250	—	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

TYPICAL STATIC CHARACTERISTICS

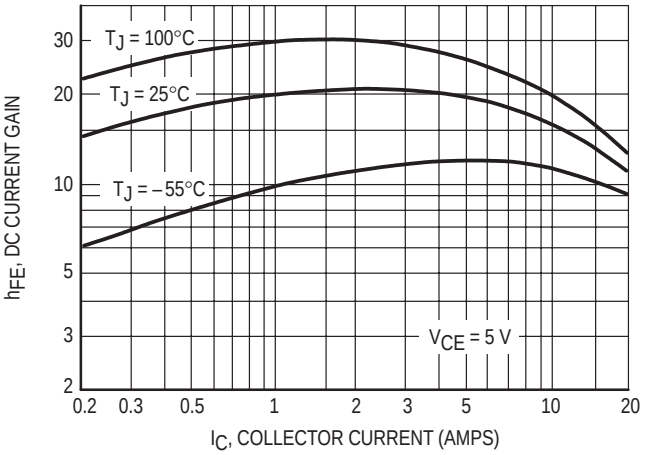


Figure 1. DC Current Gain

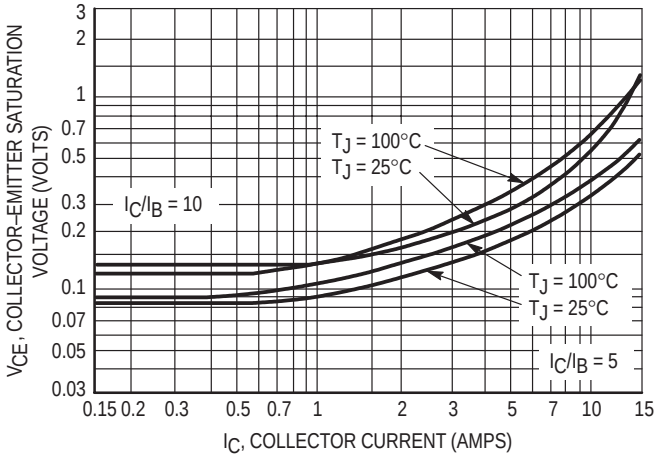


Figure 2. Collector–Emitter Saturation Voltage

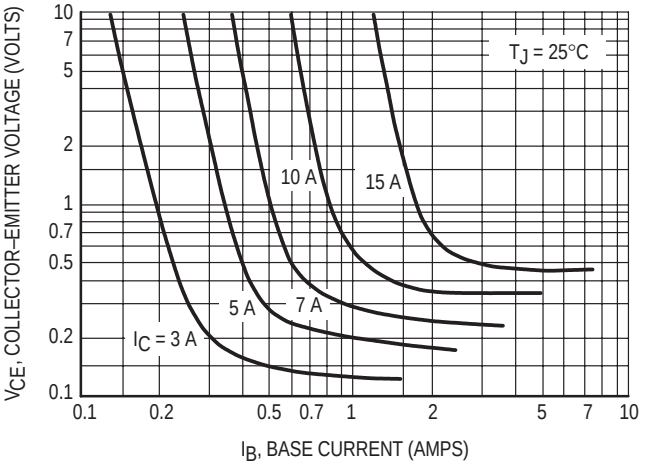


Figure 3. Collector–Emitter Saturation Region

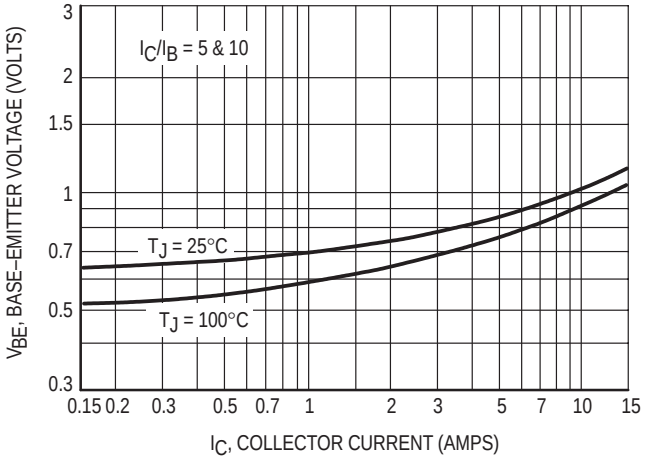


Figure 4. Base–Emitter Saturation Region

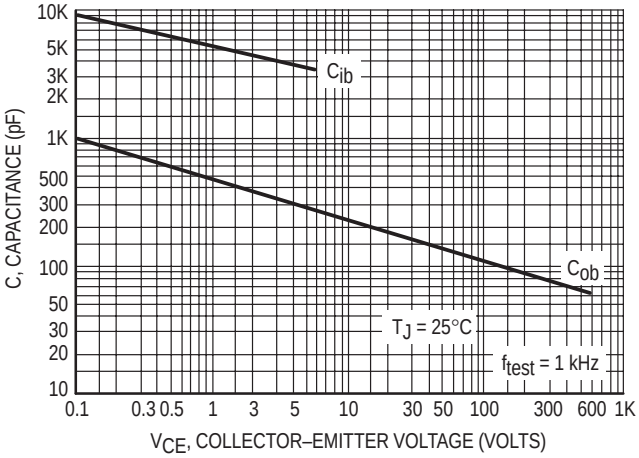


Figure 5. Capacitance

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

I_C/I_B = 10, T_C = 100°C, $V_{CE(pk)}$ = 250 V

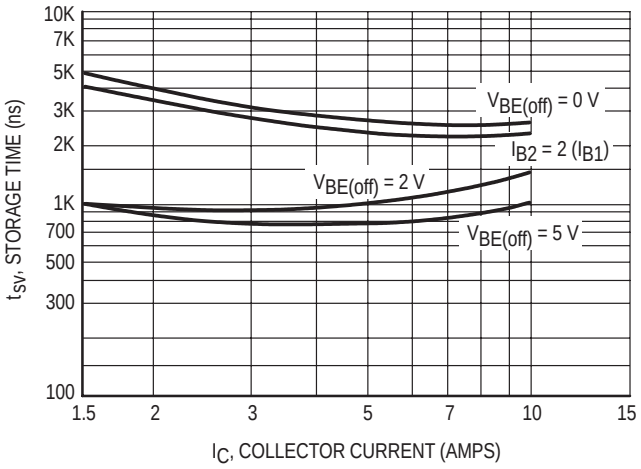


Figure 6. Storage Time

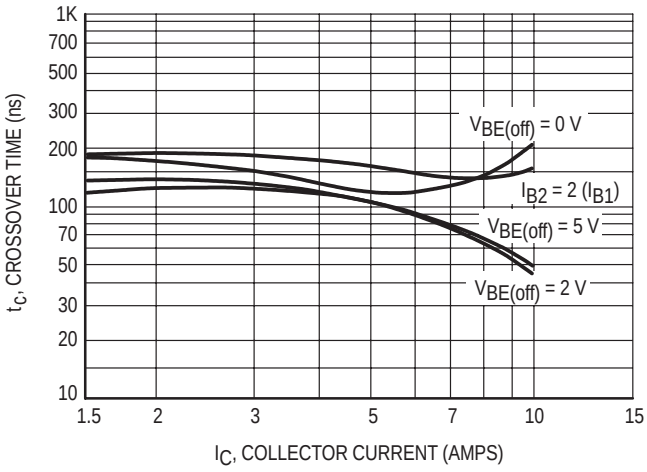


Figure 7. Crossover Time

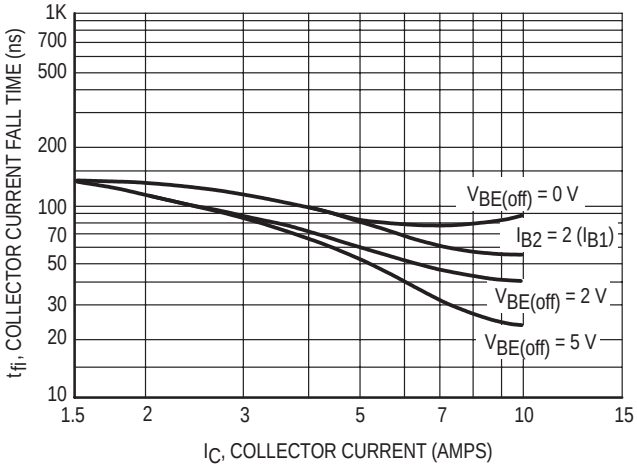


Figure 8. Fall Time

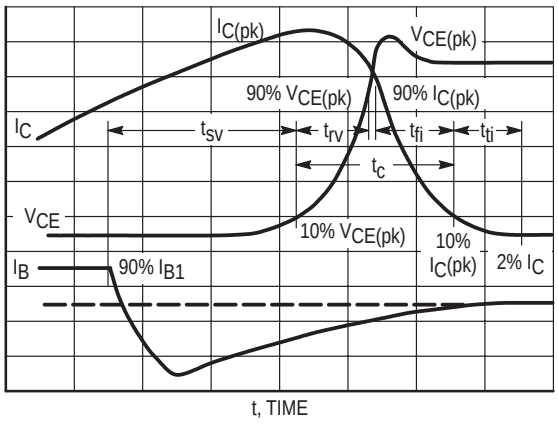


Figure 9. Inductive Switching Measurements

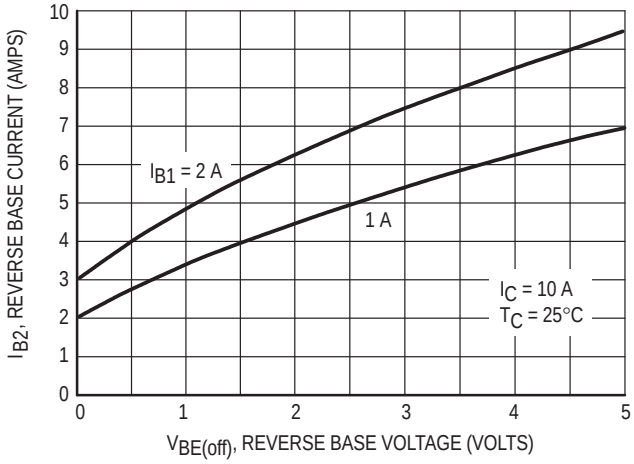
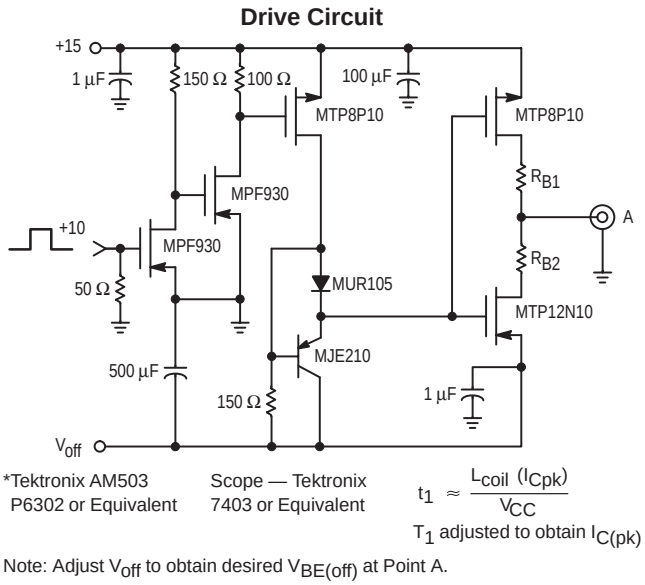


Figure 10. Peak Reverse Base Current

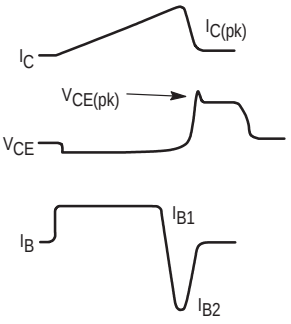
Table 1. Inductive Load Switching

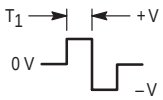


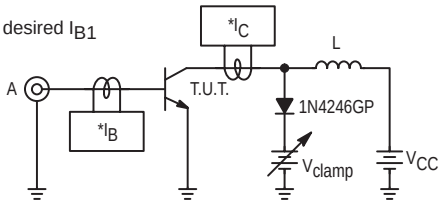
$V_{CEO(sus)}$
L = 10 mH
R_{B2} = ∞
V_{CC} = 20 Volts
$I_{C(pk)}$ = 20 mA

Inductive Switching
L = 200 µH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 200 µH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}



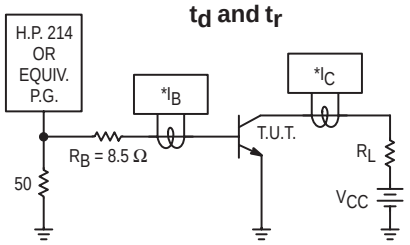


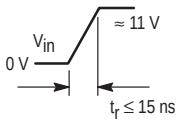


Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A.

Table 2. Resistive Load Switching

t_d and t_r



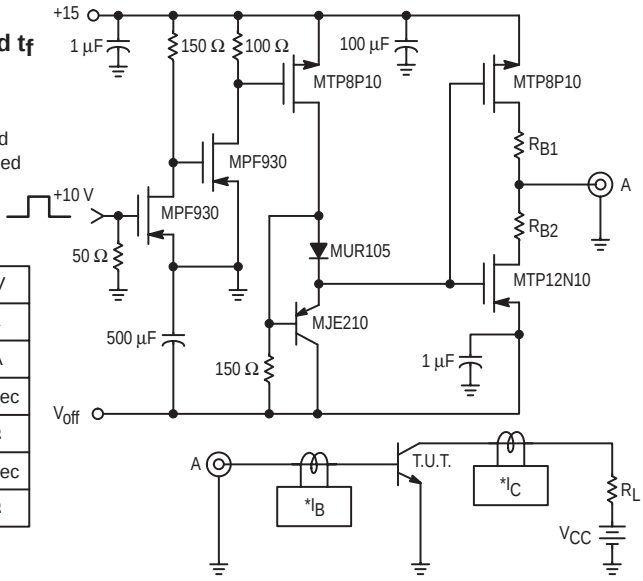


V_{CC}	250 Vdc
R_L	25 Ω
I_C	10 A
I_B	1 A

*Tektronix AM503
P6302 or Equivalent

t_s and t_f

$V_{(off)}$ adjusted to give specified off drive



V_{CC}	250 V
I_C	10 A
I_{B1}	1.0 A
I_{B2}	Per Spec
R_{B1}	15 Ω
R_{B2}	Per Spec
R_L	25 Ω

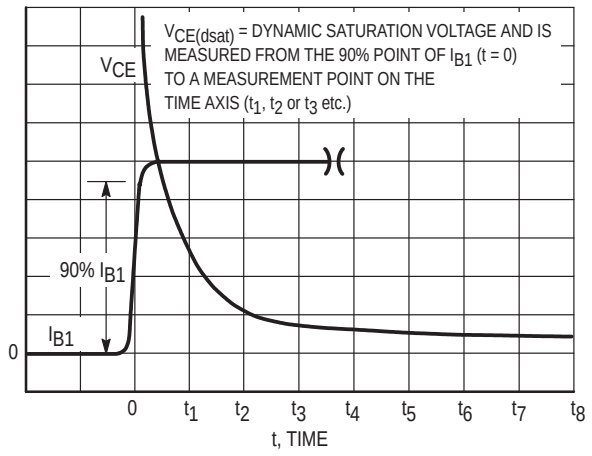


Figure 11. Definition of Dynamic Saturation Measurement

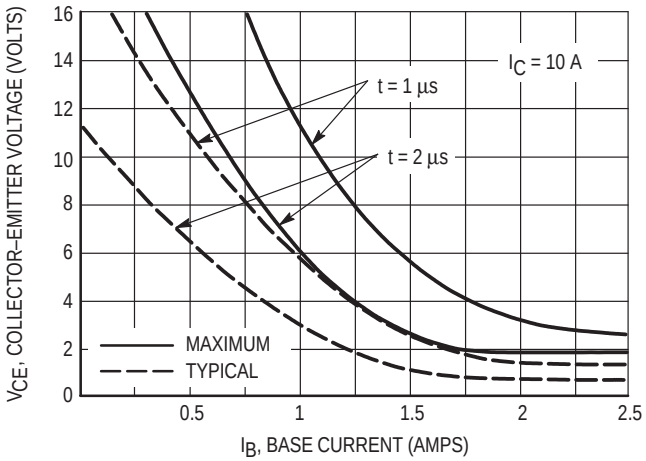


Figure 12. Dynamic Saturation Voltage

DYNAMIC SATURATION VOLTAGE

For bipolar power transistors low DC saturation voltages are achieved by conductivity modulating the collector region. Since conductivity modulation takes a finite amount of time, DC saturation voltages are not achieved instantly at turn–on. In bridge circuits, two transistor forward converters, and two transistor flyback converters dynamic saturation characteristics are responsible for the bulk of dynamic losses. The MJ16110 has been designed specifically to minimize these losses. Performance is roughly four times better than the original version of MJ16010.

From a measurement point of view, dynamic saturation voltage is defined as collector–emitter voltage at a specific point in time after I_{B1} has been applied, where t = 0 is the 90% point on the I_{B1} rise time waveform, This definition is illustrated in Figure 11. Performance data was taken in the circuit that is shown in Figure 13. The 24 volt rail allows a Tektronix 2445 or equivalent scope to operate at 1 volt per division without input amplifier saturation.

Dynamic saturation performance is illustrated in Figure 12. The MJ16110 reaches DC saturation levels in approximately 2 μs, provided that sufficient base drive is provided. The dependence of dynamic saturation voltage upon base drive suggests a spike of I_{B1} at turn–on to minimize dynamic saturation losses, and also avoid overdrive at turn–off. However, in order to simulate worst case conditions the guaranteed dynamic saturation limits in this data sheet are specified with a constant level of I_{B1}.

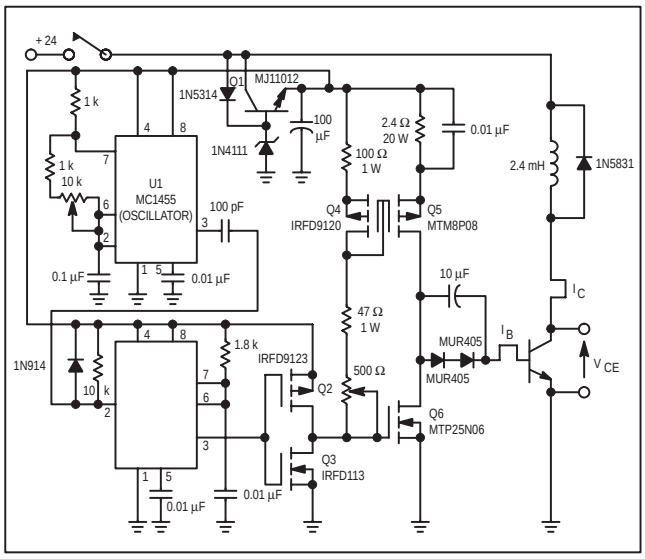


Figure 13. Dynamic Saturation Test Circuit

GUARANTEED SAFE OPERATING AREA INFORMATION

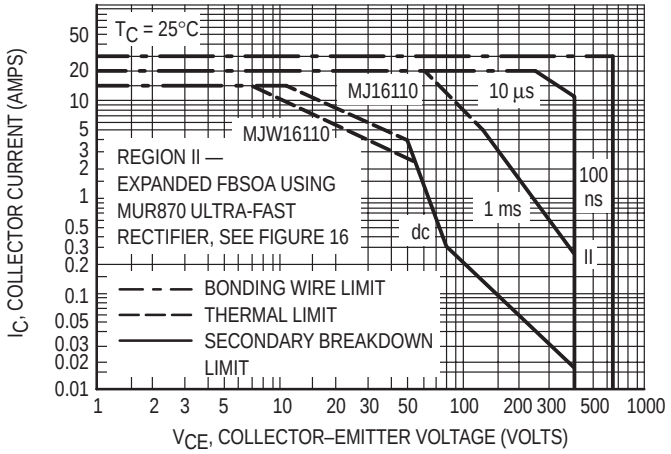


Figure 14. Forward Bias Safe Operating Area

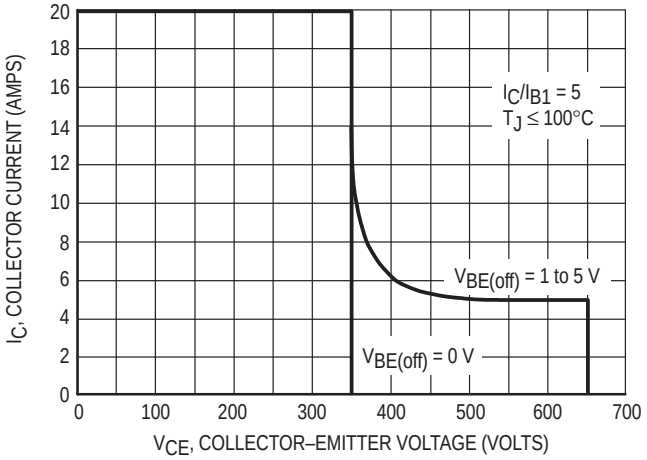


Figure 15. Reverse Bias Safe Operating Area

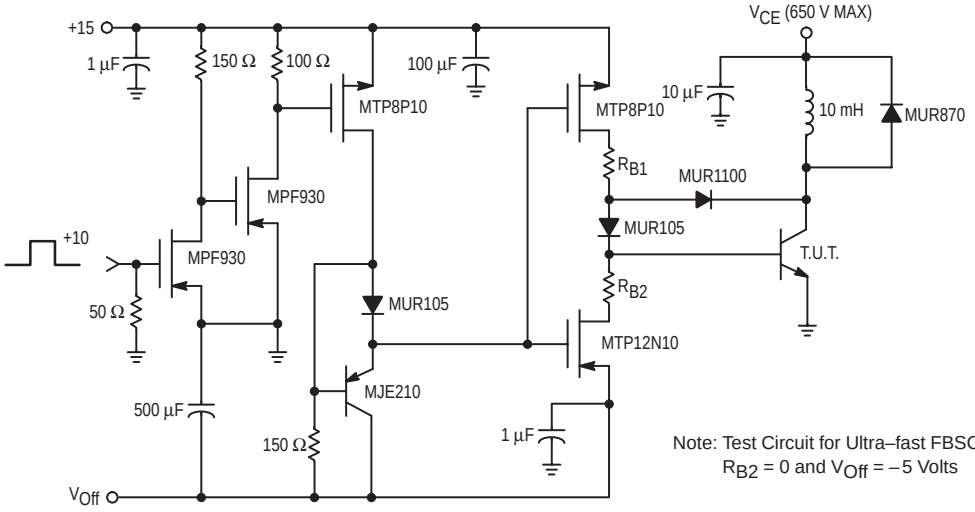


Figure 16. Switching Safe Operating Area

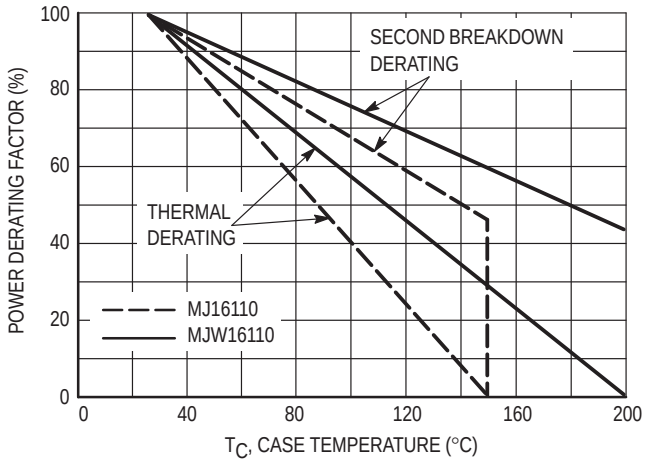


Figure 17. Power Derating

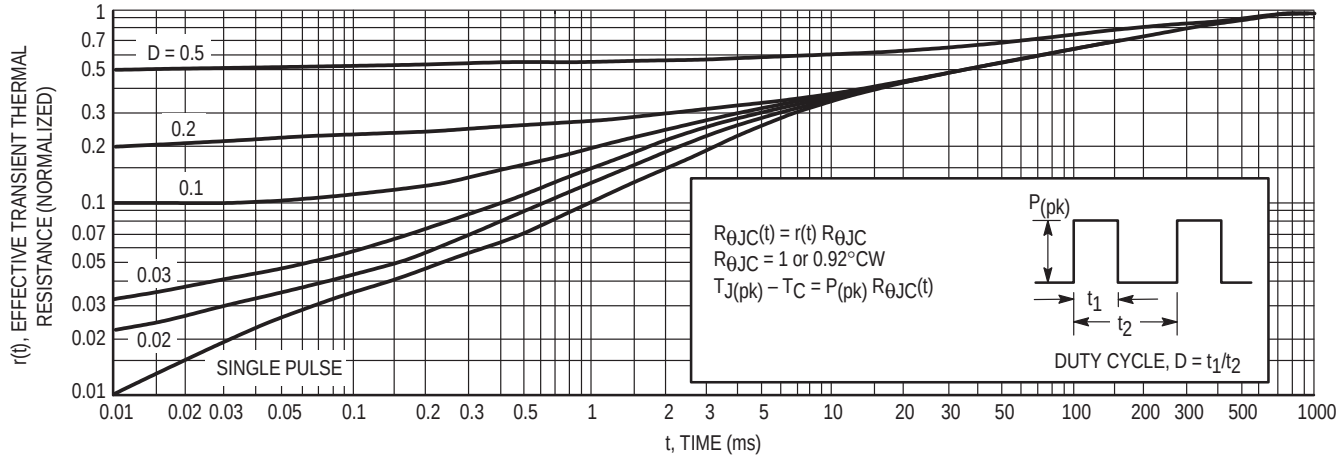


Figure 18. Thermal Response

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data in Figure 14 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 14 may be found at any case temperature by using the appropriate curve on Figure 17.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

SWITCHMODE DESIGN CONSIDERATIONS

FBSOA

Allowable dc power dissipation in bipolar power transistors decreases dramatically with increasing collector–emitter voltage. A transistor which safely dissipates 100 watts at 10 volts will typically dissipate less than 10 watts at its rated $V_{(BR)CEO(sus)}$. From a power handling point of view, current and voltage are not interchangeable (see Application Note AN875).

TURN–ON

Safe turn–on load line excursions are bounded by pulsed FBSOA curves. The 10 μs curve applies for resistive loads, most capacitive loads, and inductive loads that are clamped by standard or fast recovery rectifiers. Similarly, the 100 ns curve applies to inductive loads which are clamped by ultra–fast recovery rectifiers, and are valid for turn–on crossover times less than 100 ns (AN952).

SWITCHMODE DESIGN CONSIDERATIONS (Cont.)

At voltages above 75% of $V_{(BR)CEO(sus)}$, it is essential to provide the transistor with an adequate amount of base drive VERY RAPIDLY at turn–on. More specifically, safe operation according to the curves is dependent upon base current rise time being less than collector current rise time. As a general rule, a base drive compliance voltage in excess of 10 volts is required to meet this condition (see Application Note AN875).

TURN–OFF

A bipolar transistor's ability to withstand turn–off stress is dependent upon its forward base drive. Gross overdrive violates the RBSOA curve and risks transistor failure. For this reason, circuits which use fixed base drive are more likely to fail at light loads due to heavy overdrive (see Application Note AN875).

OPERATION ABOVE $V_{(BR)CEO(sus)}$

When bipolars are operated above collector–emitter breakdown, base drive is crucial. A rapid application of adequate forward base current is needed for safe turn–on, as is a stiff negative bias needed for safe turn–off. Any hiccup in the base–drive circuitry that even momentarily violates either of these conditions will likely cause the transistor to fail. Therefore, it is important to design the driver so that its output is negative in the absence of anything but a clean crisp input signal (see Application Note AN952).

RBSOA

Reversed Biased Safe Operating Area has a first order dependency on circuit configuration and drive parameters. The RBSOA curves in this data sheet are valid only for the conditions specified. For a comparison of RBSOA results in several types of circuits (see Application Note AN951).

DESIGN SAMPLES

Transistor parameters tend to vary much more from wafer lot to wafer lot, over long periods of time, than from one device to the next in the same wafer lot. For design evaluation it is advisable to use transistors from several different date codes.

BAKER CLAMPS

Many unanticipated pitfalls can be avoided by using Baker Clamps. MUR105 and MUR170 diodes are recommended for base drives less than 1 amp. Similarly, MUR405 and MUR470 types are well–suited for higher drive requirements (see Article Reprint AR131).

Silicon Power Transistors

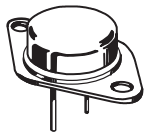
PNP
MJ21193*
NPN
MJ21194*

*Motorola Preferred Device

The MJ21193 and MJ21194 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain – h_{FE} = 25 Min @ I_C = 8 Adc
- Excellent Gain Linearity
- High SOA: 2.5 A, 80 V, 1 Second

16 AMPERE
COMPLEMENTARY
SILICON POWER
TRANSISTORS
250 VOLTS
250 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CBO}	400	Vdc
Emitter–Base Voltage	V_{EBO}	5	Vdc
Collector–Emitter Voltage – 1.5 V	V_{CEX}	400	Vdc
Collector Current — Continuous Peak (1)	I_C	16 30	Adc
Base Current — Continuous	I_B	5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	250 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	– 65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤10%.

(continued)

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	—	—	100	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non–repetitive)) (V_{CE} = 80 Vdc, t = 1 s (non–repetitive))	$I_{S/b}$	 5 2.5	 — —	 — —	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 8 Adc, V_{CE} = 5 Vdc) (I_C = 16 Adc, I_B = 5 Adc)	h_{FE}	 25 8	 — —	75	
Base–Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	—	—	2.2	Vdc
Collector–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc) (I_C = 16 Adc, I_B = 3.2 Adc)	$V_{CE(sat)}$	 — —	 — —	 1.4 4	Vdc
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS} h_{FE} unmatched (Matched pair h_{FE} = 50 @ 5 A/5 V) h_{FE} matched	T_{HD}	 — —	 0.8 0.08	 — —	%
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	4	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	—	500	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

PNP MJ21193

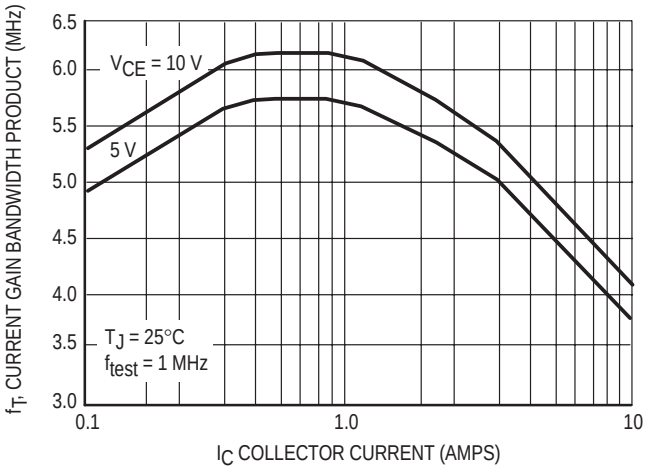


Figure 1. Typical Current Gain Bandwidth Product

NPN MJ21194

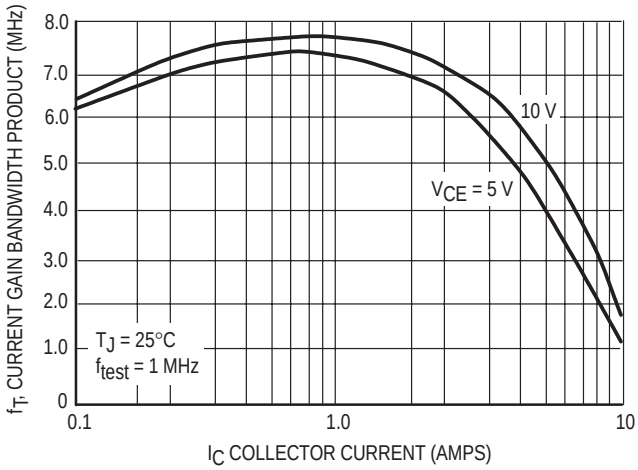


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJ21193

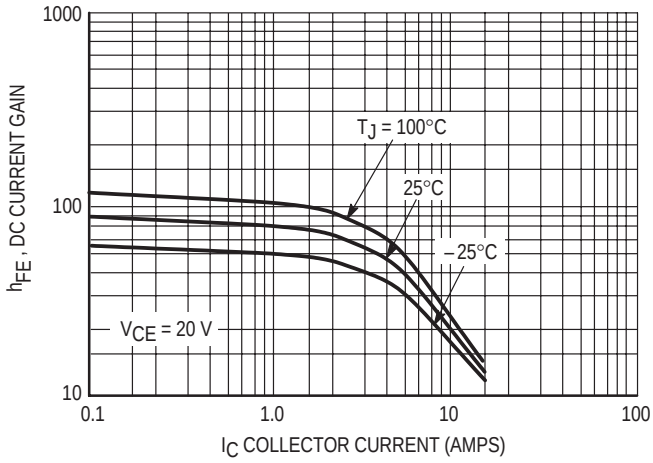


Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJ21194

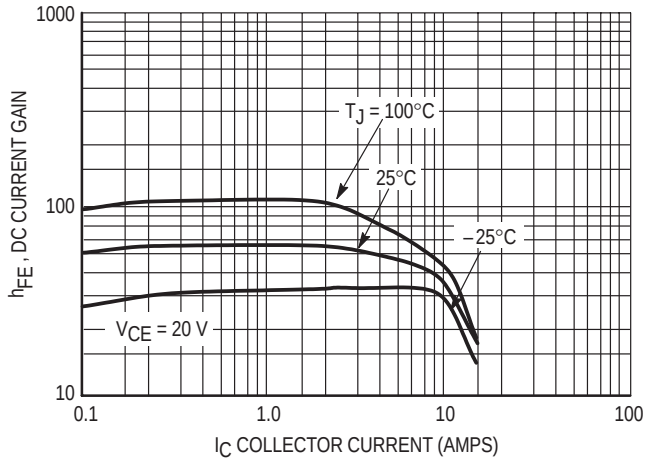


Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJ21193

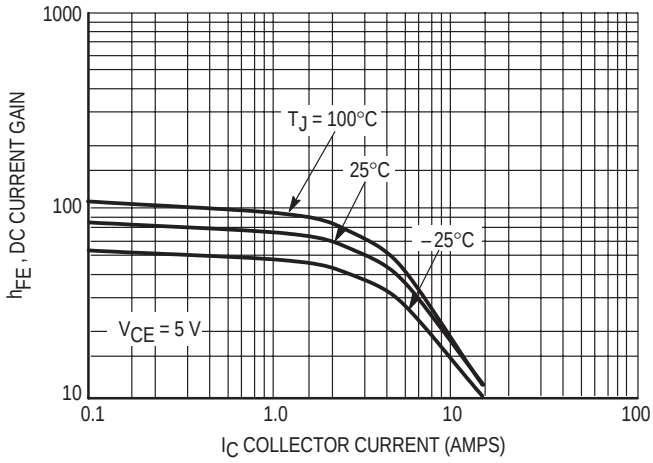


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJ21194

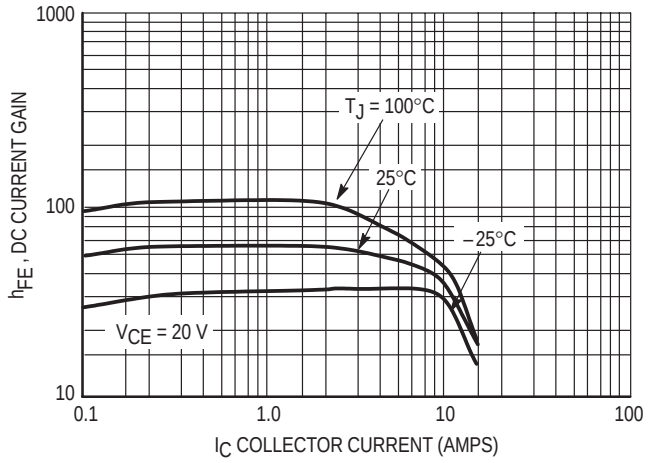


Figure 6. DC Current Gain, V_{CE} = 5 V

PNP MJ21193

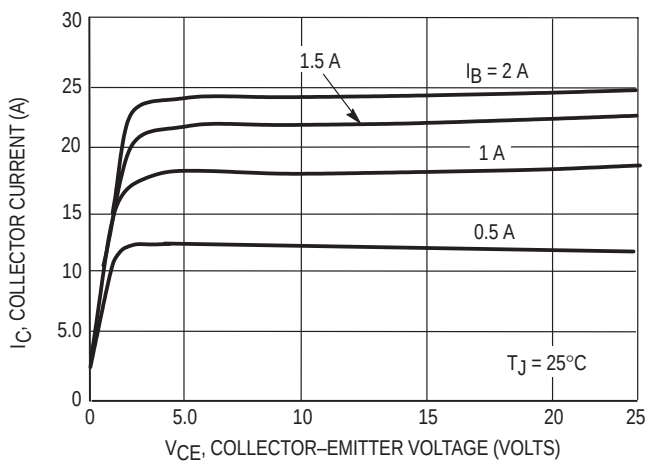


Figure 7. Typical Output Characteristics

NPN MJ21194

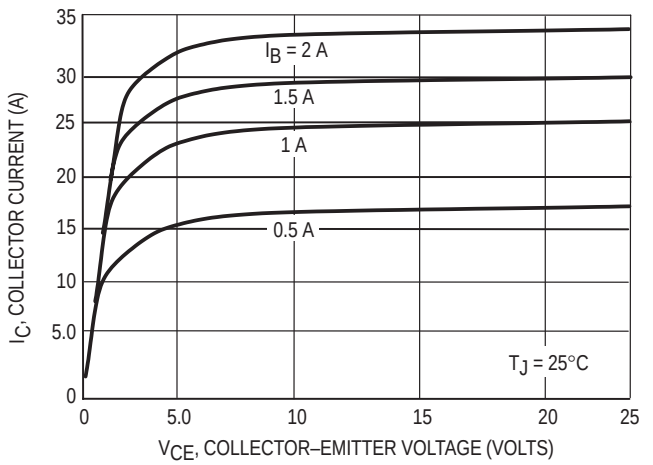


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJ21193

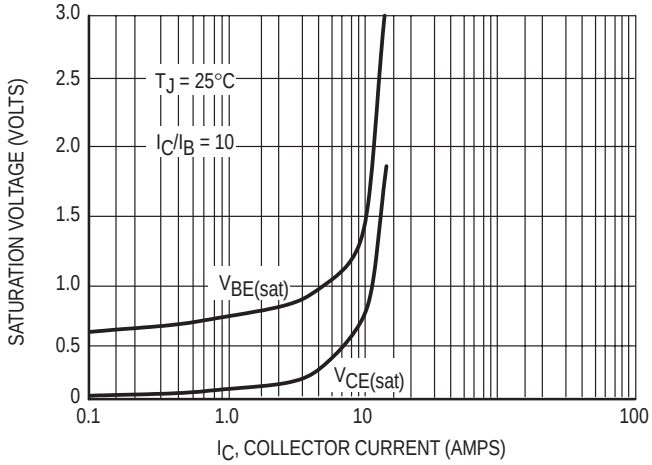


Figure 9. Typical Saturation Voltages

NPN MJ21194

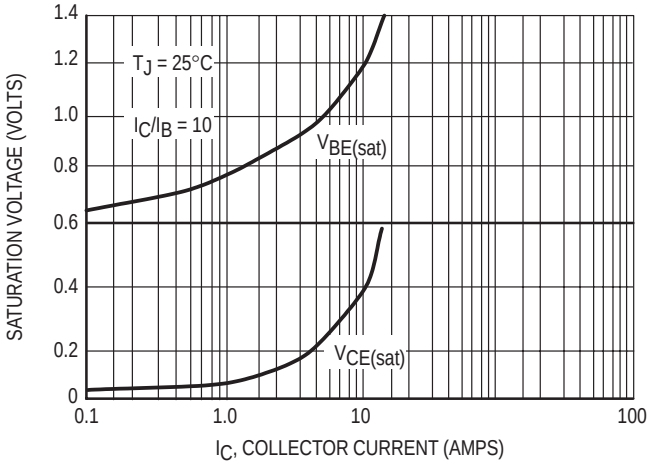


Figure 10. Typical Saturation Voltages

PNP MJ21193

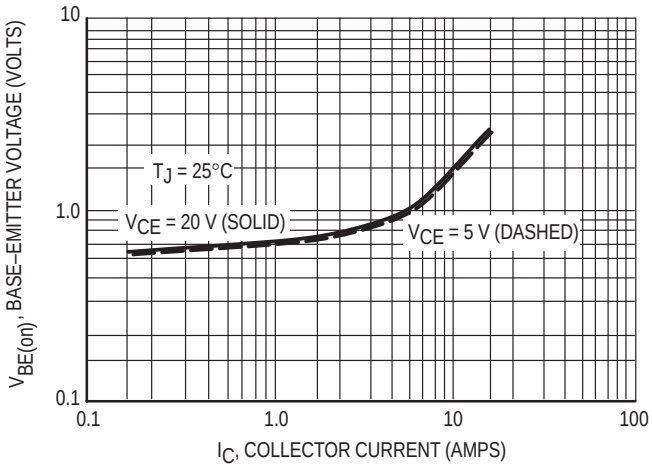


Figure 11. Typical Base–Emitter Voltage

NPN MJ21194

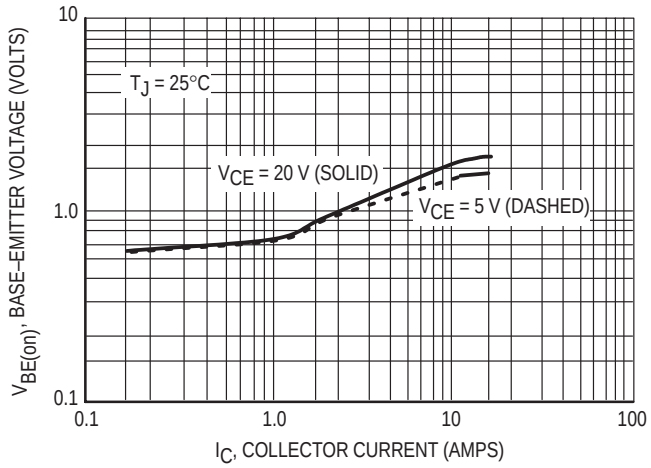


Figure 12. Typical Base–Emitter Voltage

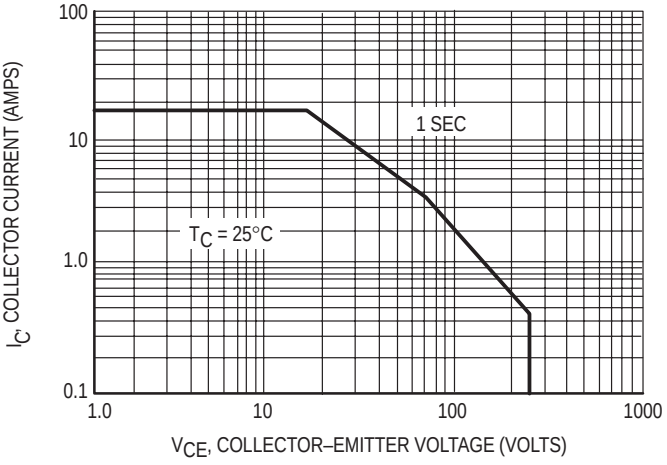


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

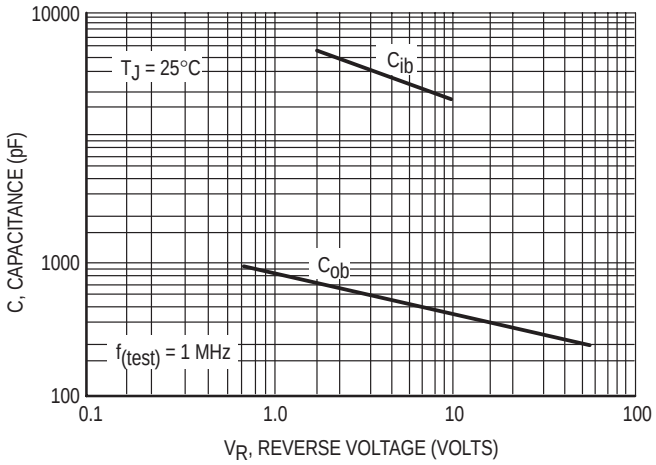


Figure 14. MJ21193 Typical Capacitance

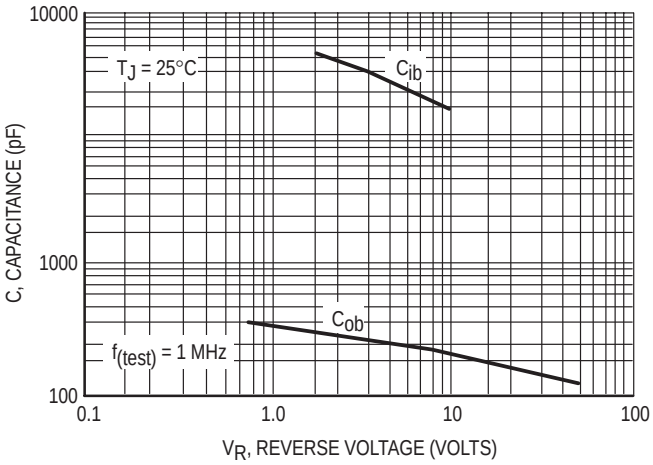


Figure 15. MJ21194 Typical Capacitance

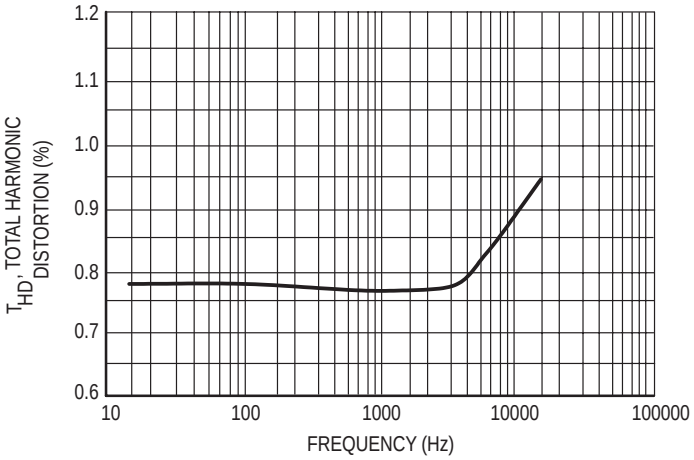


Figure 16. Typical Total Harmonic Distortion

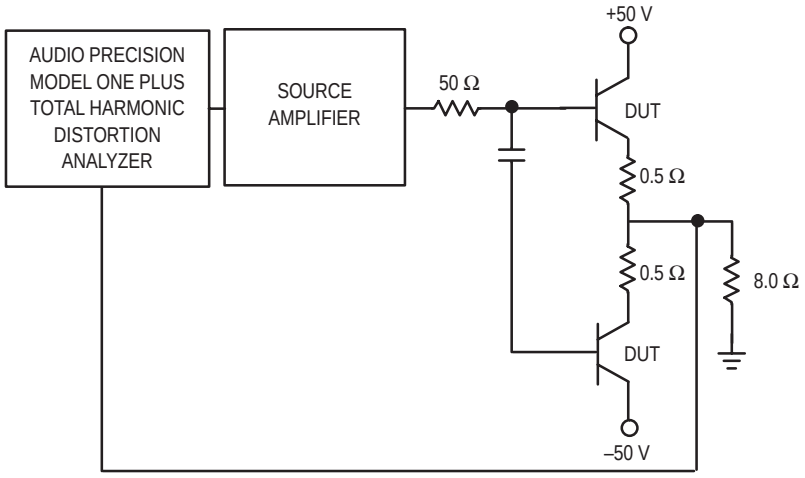


Figure 17. Total Harmonic Distortion Test Circuit

Complementary Power Transistors

DPAK For Surface Mount Applications

NPN
MJD31,C*
PNP
MJD32,C*

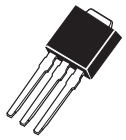
*Motorola Preferred Device

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("T4" Suffix)
- Electrically Similar to Popular TIP31 and TIP32 Series

SILICON
POWER TRANSISTORS
3 AMPERES
40 AND 100 VOLTS
15 WATTS

CASE 369A–13



CASE 369–07

MAXIMUM RATINGS

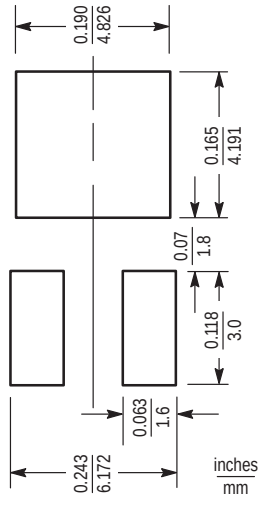
Rating	Symbol	MJD31 MJD32	MJD31C MJD32C	Unit
Collector–Emitter Voltage	V_{CEO}	40	100	Vdc
Collector–Base Voltage	V_{CB}	40	100	Vdc
Emitter–Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous Peak	I_C	3 5		Adc
Base Current	I_B	1		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12		Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.56 0.012		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.3	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	80	°C/W
Lead Temperature for Soldering Purposes	T_L	260	°C

* These ratings are applicable when surface mounted on the minimum pad size recommended.

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	MJD31, MJD32		40	—	
	MJD31C, MJD32C		100	—	
Collector Cutoff Current		I_{CEO}	—	50	μAdc
(V_{CE} = 40 Vdc, I_B = 0)	MJD31, MJD32				
(V_{CE} = 60 Vdc, I_B = 0)	MJD31C, MJD32C				
Collector Cutoff Current		ICES	—	20	μAdc
(V_{CE} = Rated V_{CEO}, V_{EB} = 0)					
Emitter Cutoff Current		I_{EBO}	—	1	mAdc
(V_{BE} = 5 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 1 Adc, V_{CE} = 4 Vdc)			25	—	
(I_C = 3 Adc, V_{CE} = 4 Vdc)			10	50	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$	—	1.2	Vdc
(I_C = 3 Adc, I_B = 375 mAdc)					
Base–Emitter On Voltage		$V_{BE(on)}$	—	1.8	Vdc
(I_C = 3 Adc, V_{CE} = 4 Vdc)					
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2)		f_T	3	—	MHz
(I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)					
Small–Signal Current Gain		h_{fe}	20	—	—
(I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)					

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) $f_T = |h_{fe}| \bullet f_{test}$.

TYPICAL CHARACTERISTICS

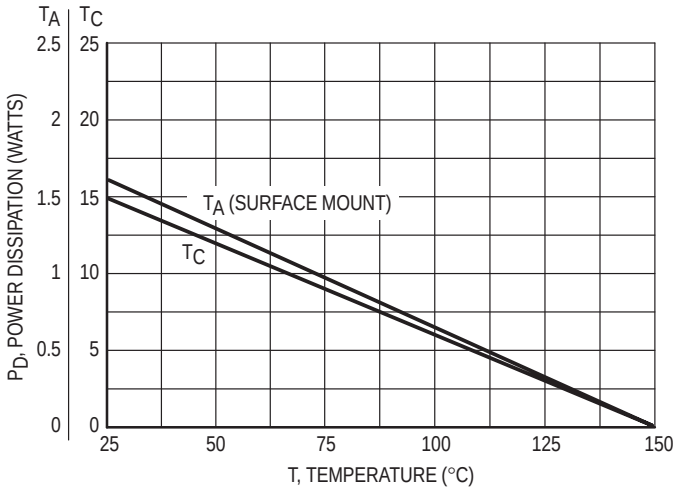
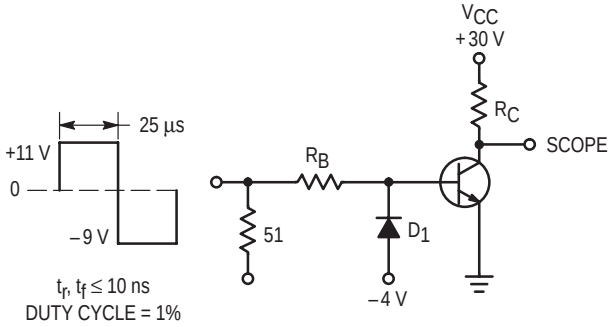


Figure 1. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA
REVERSE ALL POLARITIES FOR PNP.

Figure 2. Switching Time Test Circuit

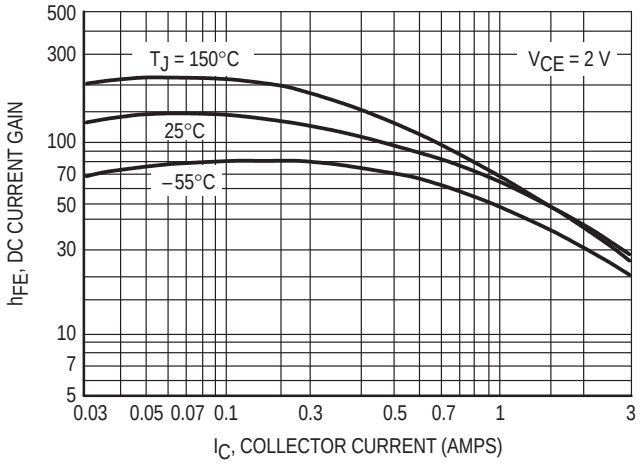


Figure 3. DC Current Gain

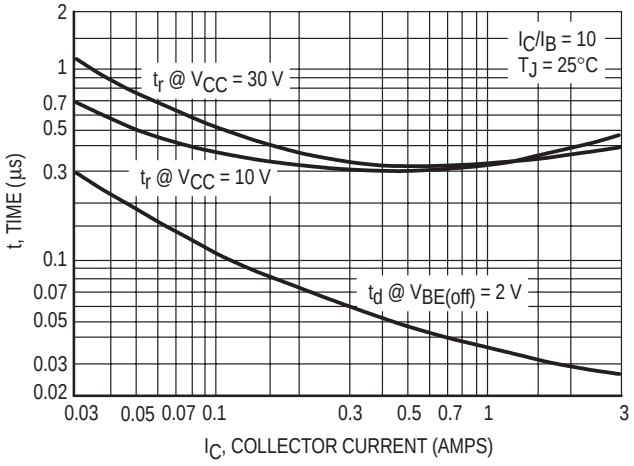


Figure 4. Turn–On Time

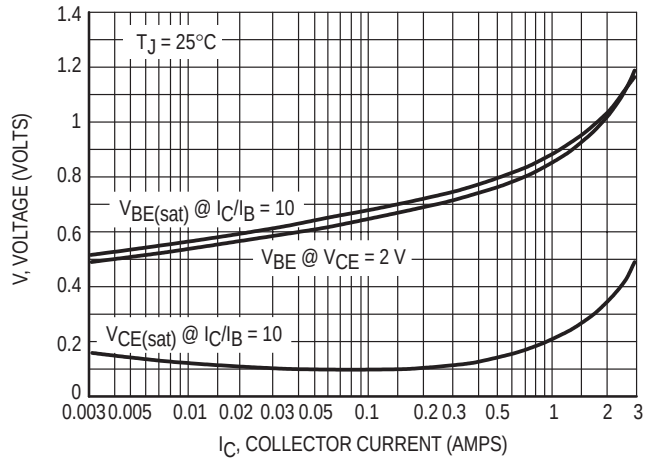


Figure 5. “On” Voltages

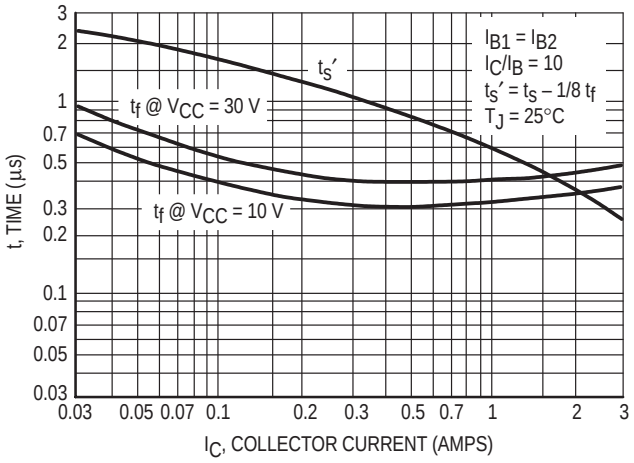


Figure 6. Turn–Off Time

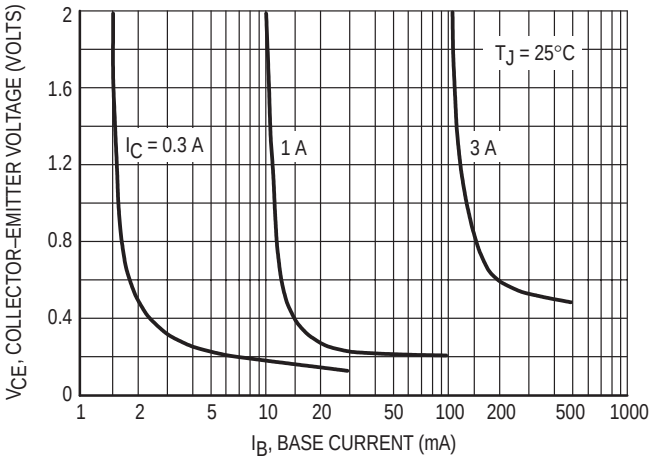


Figure 7. Collector Saturation Region

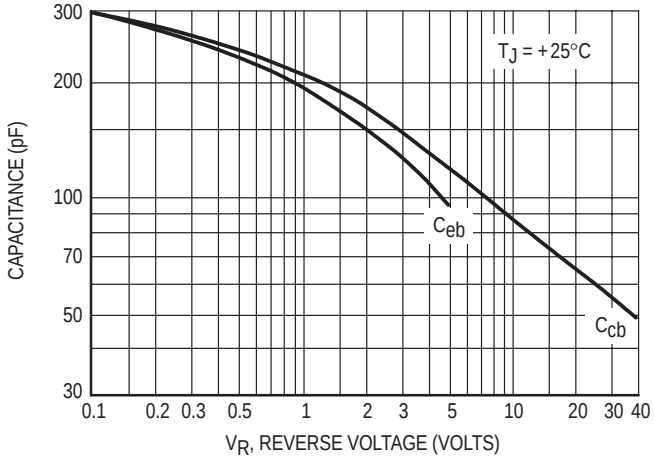


Figure 8. Capacitance

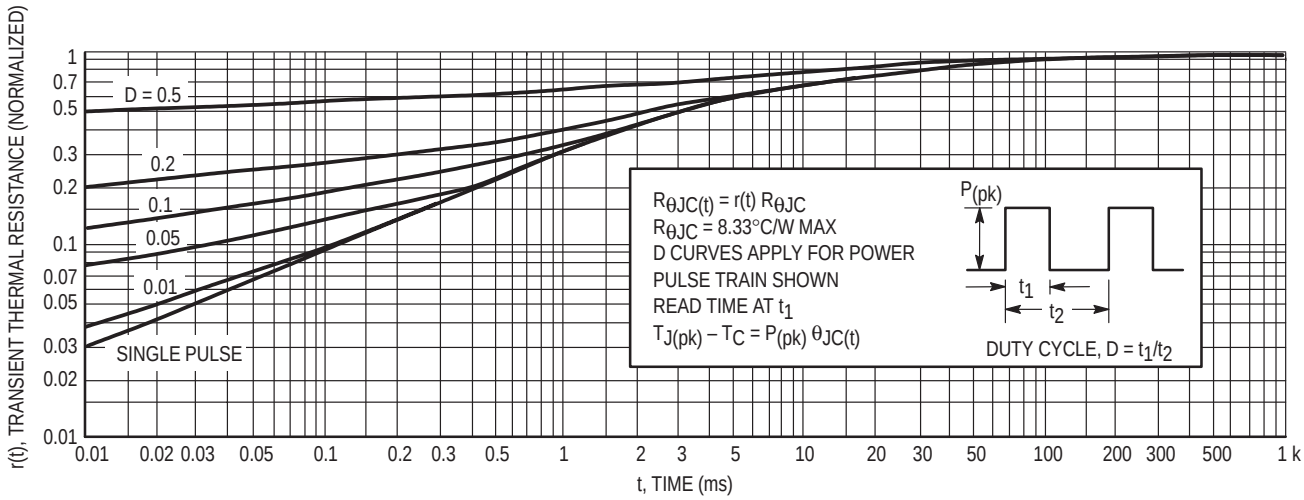


Figure 9. Thermal Response

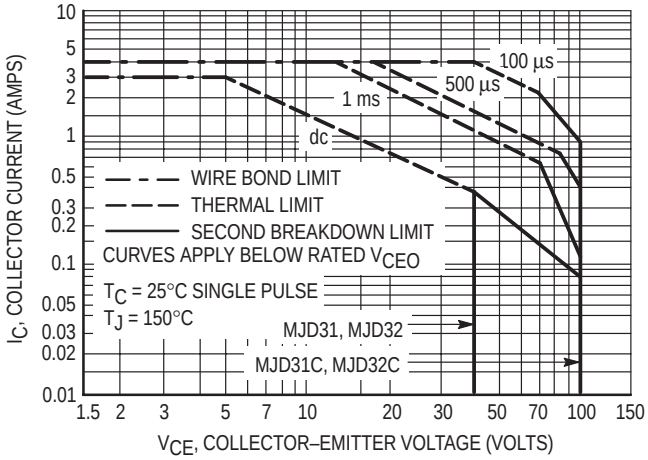


Figure 10. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Complementary Power Transistors

DPAK For Surface Mount Applications

NPN
MJD41C*
PNP
MJD42C*

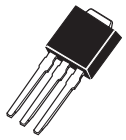
*Motorola Preferred Device

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("T4" Suffix)
- Electrically Similar to Popular TIP41 and TIP42 Series
- Monolithic Construction With Built–in Base–Emitter Resistors

SILICON
POWER TRANSISTORS
6 AMPERES
100 VOLTS
20 WATTS

CASE 369A–13



CASE 369–07

MAXIMUM RATINGS

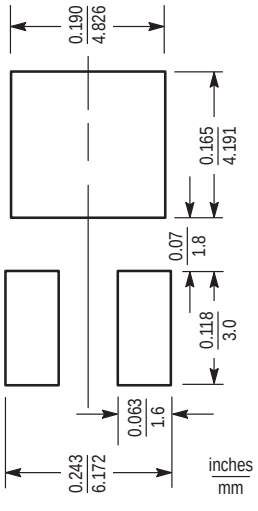
Rating	Symbol	MJD41C MJD42C	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	6 10	Adc
Base Current	I_B	2	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	°C/W

* These ratings are applicable when surface mounted on the minimum pad size recommended.

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)	I_{CEO}	—	50	μAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, V_{EB} = 0)	I_{CES}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	0.5	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4 Vdc) (I_C = 3 Adc, V_{CE} = 4 Vdc)	h_{FE}	 30 15	 — 75	—
Collector–Emitter Saturation Voltage (I_C = 6 Adc, I_B = 600 mAdc)	$V_{CE(sat)}$	—	1.5	Vdc
Base–Emitter On Voltage (I_C = 6 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	2	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	3	—	MHz
Small–Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 kHz)	h_{fe}	20	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

TYPICAL CHARACTERISTICS

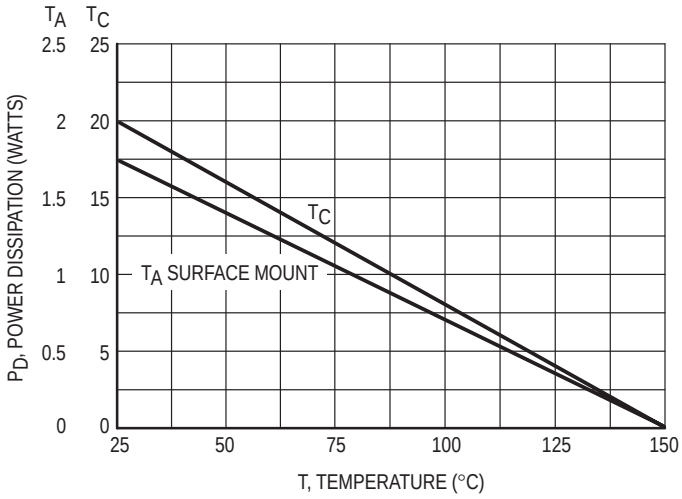
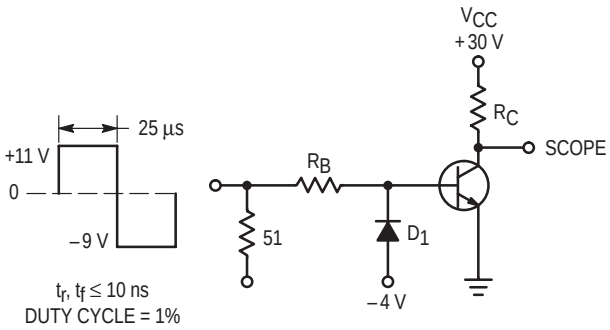


Figure 1. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
MSB5300 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA
REVERSE ALL POLARITIES FOR PNP.

Figure 2. Switching Time Test Circuit

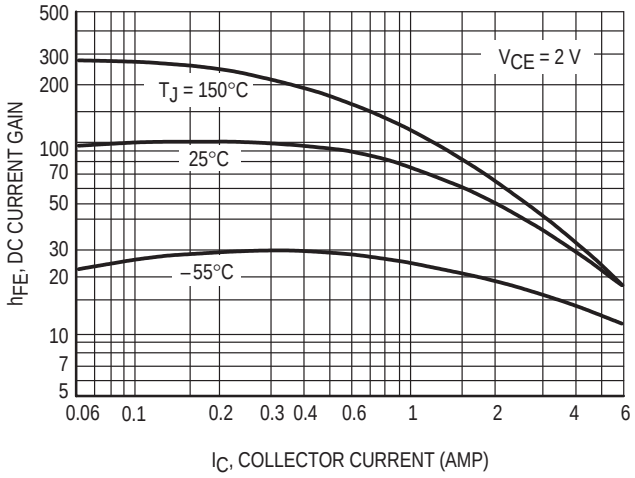


Figure 3. DC Current Gain

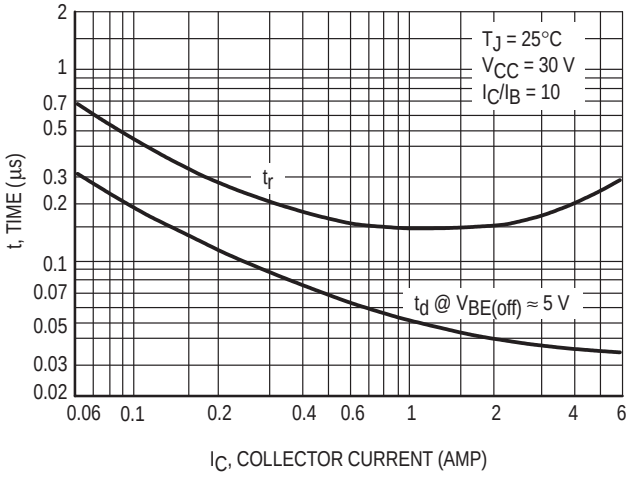


Figure 4. Turn–On Time

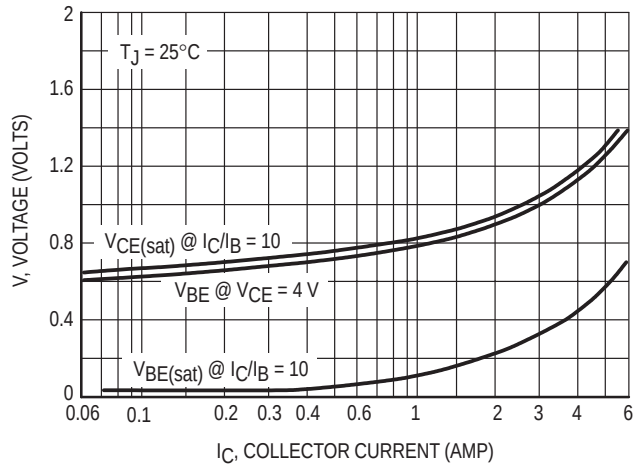


Figure 5. “On” Voltages

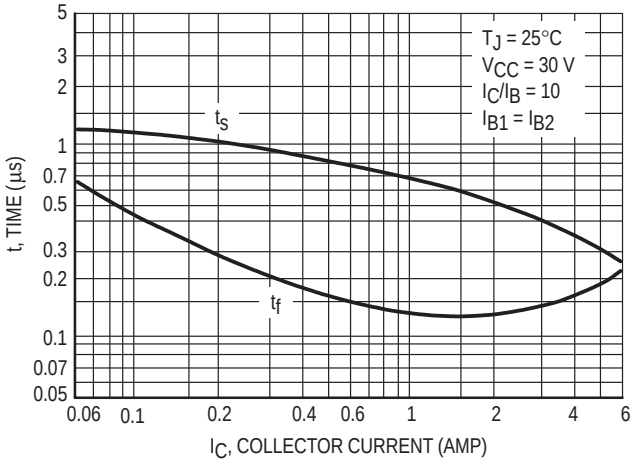


Figure 6. Turn–Off Time

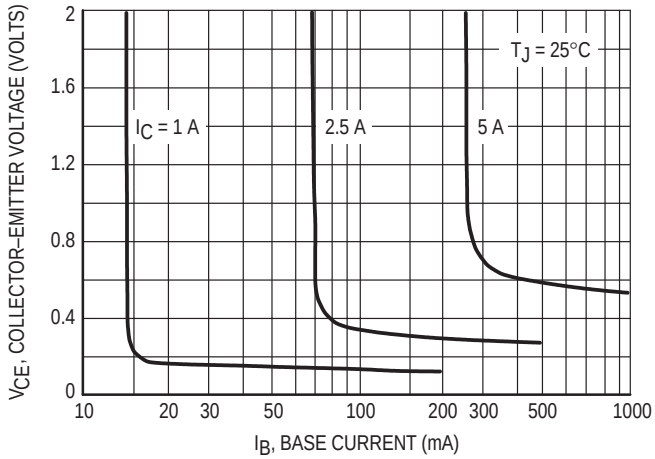


Figure 7. Collector Saturation Region

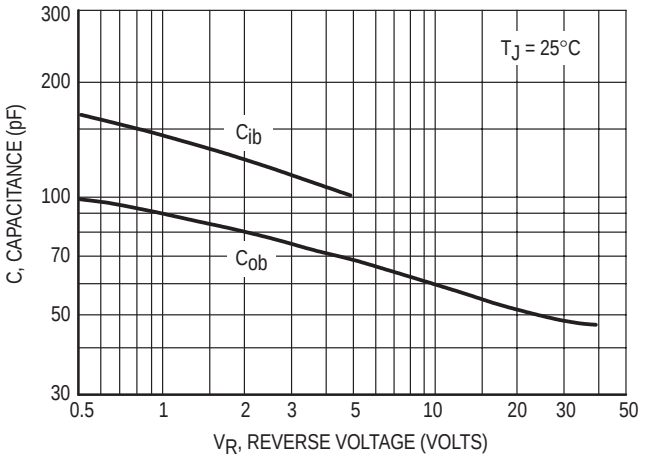


Figure 8. Capacitance

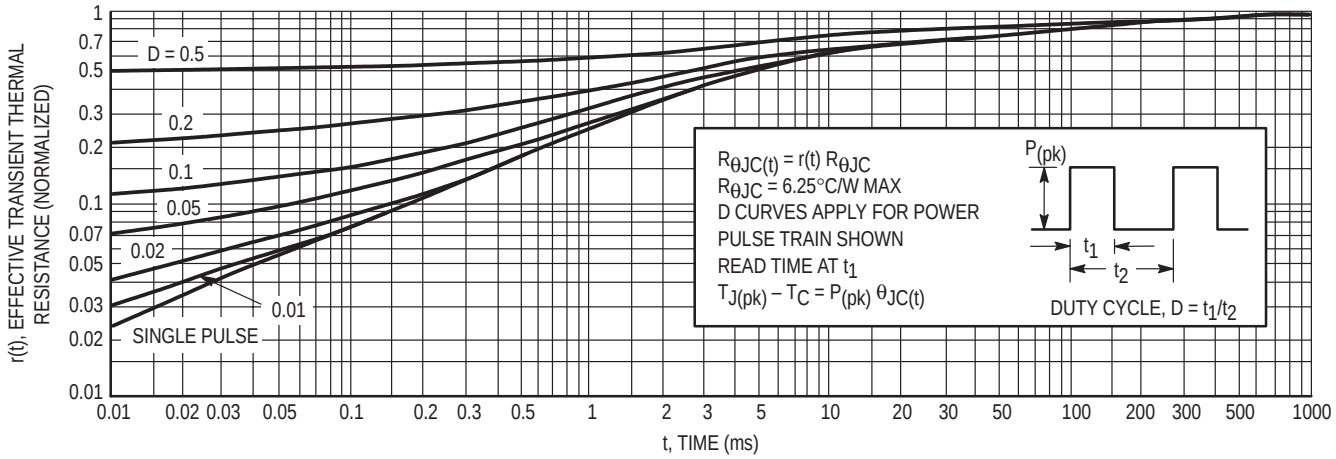


Figure 9. Thermal Response

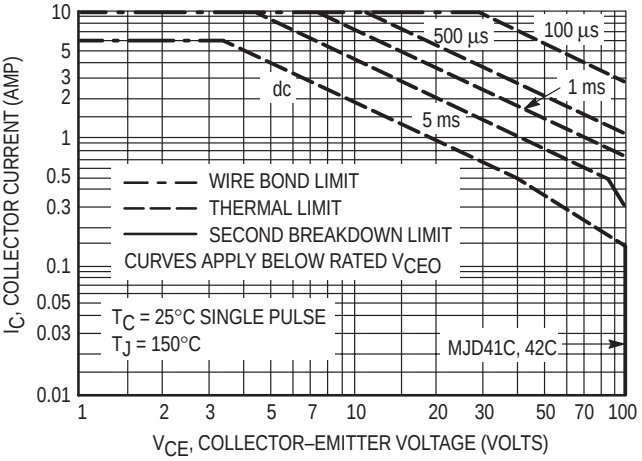


Figure 10. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Complementary Power Transistors

DPAK For Surface Mount Applications

. . . for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

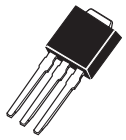
- Lead Formed for Surface Mount Application in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel for Surface Mount ("T4" Suffix)
- Electrically Similar to Popular D44H/D45H Series
- Low Collector Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.0 Volt Max @ 8.0 Amperes
- Fast Switching Speeds
- Complementary Pairs Simplifies Designs

NPN
MJD44H11*
PNP
MJD45H11*

***Motorola Preferred Device**

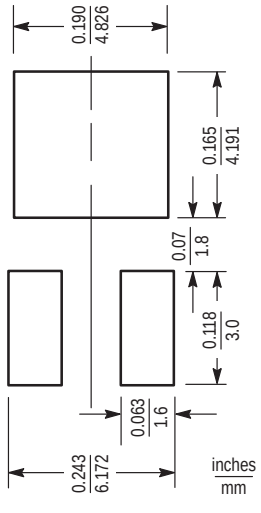
SILICON
POWER TRANSISTORS
8 AMPERES
80 VOLTS
20 WATTS

CASE 369A–13



CASE 369–07

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	D44H11 or D45H11	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	8 16	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 20 0.16	 Watts W/°C
Total Power Dissipation (1) @ T_A = 25°C Derate above 25°C	P_D	 1.75 0.014	 Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	°C/W
Lead Temperature for Soldering	T_L	260	°C

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 30 mA, I_B = 0)		$V_{CEO(sus)}$	80	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, V_{BE} = 0)		I_{CES}	—	—	10	μA
Emitter Cutoff Current (V_{EB} = 5 Vdc)		I_{EBO}	—	—	50	μA
ON CHARACTERISTICS						
Collector–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.4 Adc)		$V_{CE(sat)}$	—	—	1	Vdc
Base–Emitter Saturation Voltage (I_C = 8 Adc, I_B = 0.8 Adc)		$V_{BE(sat)}$	—	—	1.5	Vdc
DC Current Gain (V_{CE} = 1 Vdc, I_C = 2 Adc)		h_{FE}	60	—	—	—
DC Current Gain (V_{CE} = 1 Vdc, I_C = 4 Adc)			40	—	—	
DYNAMIC CHARACTERISTICS						
Collector Capacitance (V_{CB} = 10 Vdc, f_{test} = 1 MHz)	MJD44H11 MJD45H11	C_{cb}	— —	130 230	— —	pF
Gain Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 20 MHz)	MJD44H11 MJD45H11	f_T	— —	50 40	— —	MHz
SWITCHING TIMES						
Delay and Rise Times (I_C = 5 Adc, I_{B1} = 0.5 Adc)	MJD44H11 MJD45H11	$t_d + t_r$	— —	300 135	— —	ns
Storage Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJD44H11 MJD45H11	t_s	— —	500 500	— —	ns
Fall Time (I_C = 5 Adc, I_{B1} = I_{B2} = 0.5 Adc)	MJD44H11 MJD45H11	t_f	— —	140 100	— —	ns

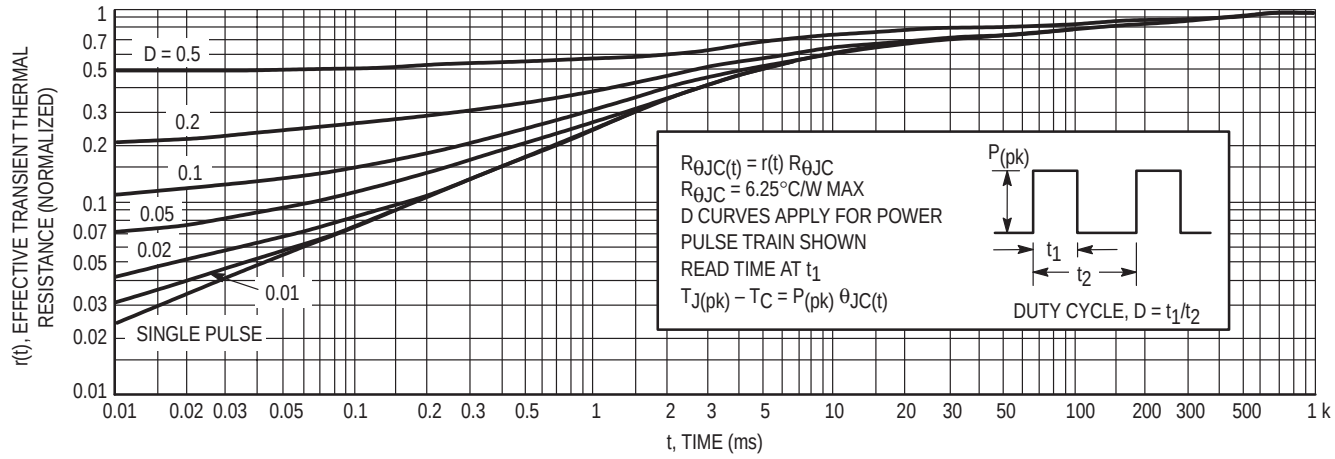


Figure 1. Thermal Response

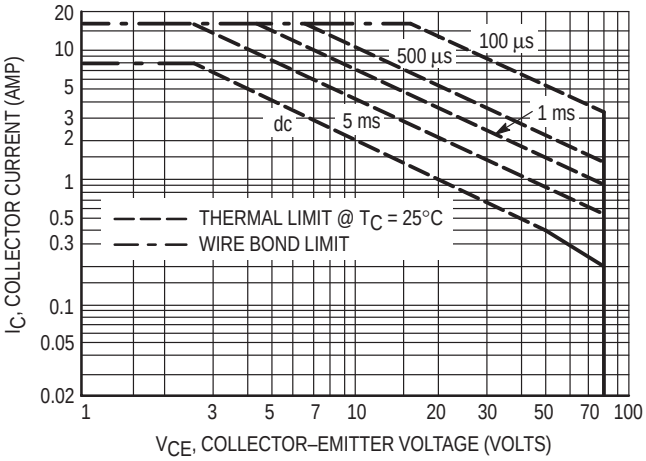


Figure 2. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

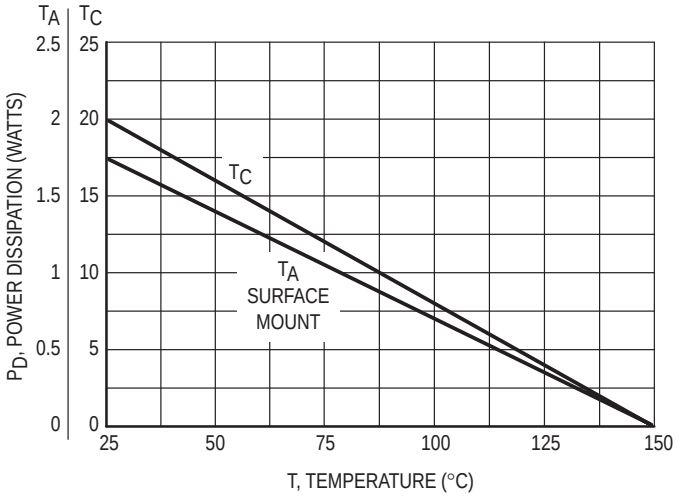


Figure 3. Power Derating

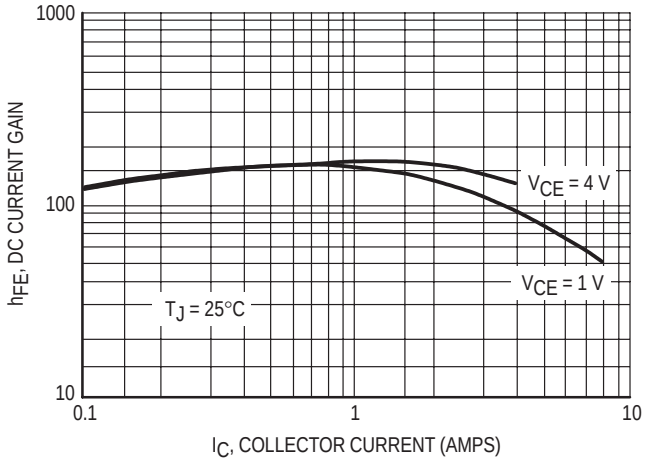


Figure 4. MJD44H11 DC Current Gain

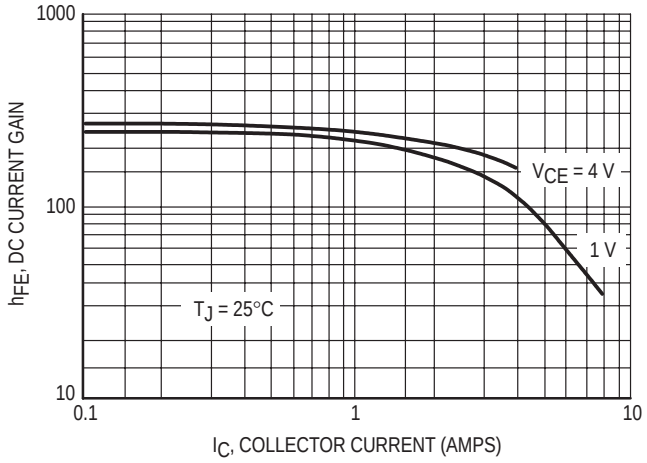


Figure 5. MJD45H11 DC Current Gain

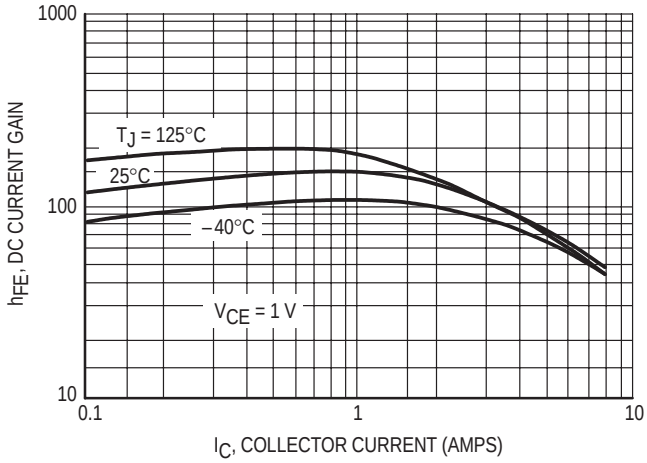


Figure 6. MJD44H11 Current Gain versus Temperature

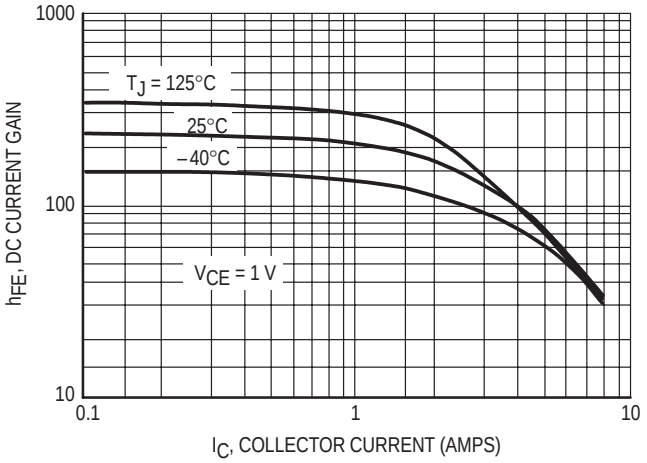


Figure 7. MJD45H11 Current Gain versus Temperature

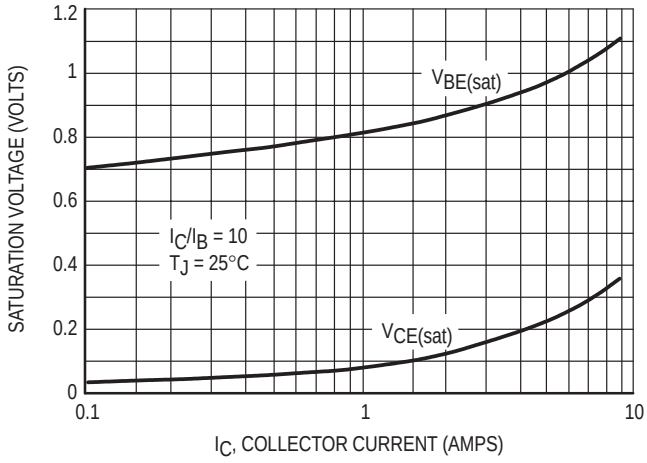


Figure 8. MJD44H11 On–Voltages

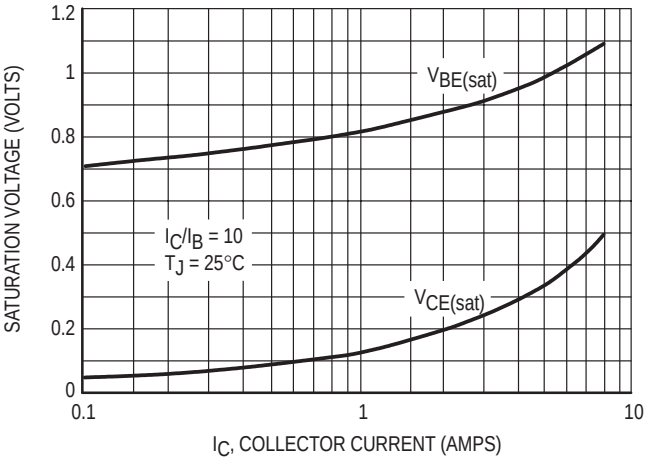


Figure 9. MJD45H11 On–Voltages

MJD47*
MJD50*

*Motorola Preferred Device

NPN SILICON
POWER TRANSISTORS
1 AMPERE
250, 400 VOLTS
15 WATTS

High Voltage Power Transistors
DPAK For Surface Mount Applications

Designed for line operated audio output amplifier, switchmode power supply drivers and other switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("T4" Suffix)
- Electrically Similar to Popular TIP47, and TIP50
- 250 and 400 V (Min) — $V_{CEO(sus)}$
- 1 A Rated Collector Current

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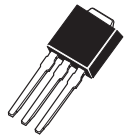


CASE 369–07

MAXIMUM RATINGS

Rating	Symbol	MJD47	MJD50	Unit
Collector–Emitter Voltage	V_{CEO}	250	400	Vdc
Collector–Base Voltage	V_{CB}	350	500	Vdc
Emitter–Base Voltage	V_{EB}	5		Vdc
Collector Current — Continuous Peak	I_C	1 2		Adc
Base Current	I_B	0.6		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12		Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.56 0.0125		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	80	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

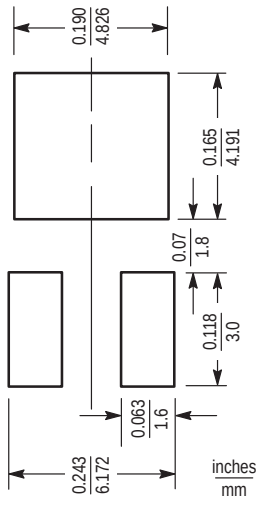
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	MJD47 MJD50	$V_{CEO(sus)}$	250 400	— —	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 300 Vdc, I_B = 0)	 MJD47 MJD50	I_{CEO}	 — —	 0.2 0.2	mAdc

* When surface mounted on minimum pad sizes recommended. (continued)

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS – continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued					
Collector Cutoff Current		I_{CES}			mAdc
(V_{CE} = 350 Vdc, V_{BE} = 0)	MJD47		—	0.1	
(V_{CE} = 500 Vdc, V_{BE} = 0)	MJD50		—	0.1	
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	1	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 0.3 Adc, V_{CE} = 10 Vdc)			30	150	
(I_C = 1 Adc, V_{CE} = 10 Vdc)			10	—	
Collector–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)		$V_{CE(sat)}$	—	1	Vdc
Base–Emitter On Voltage (I_C = 1 Adc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 2 MHz)		f_T	10	—	MHz
Small–Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1 kHz)		h_{fe}	25	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

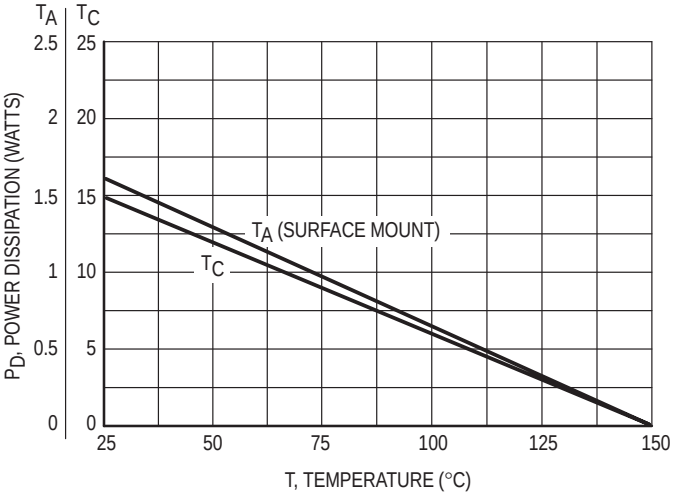


Figure 1. Power Derating

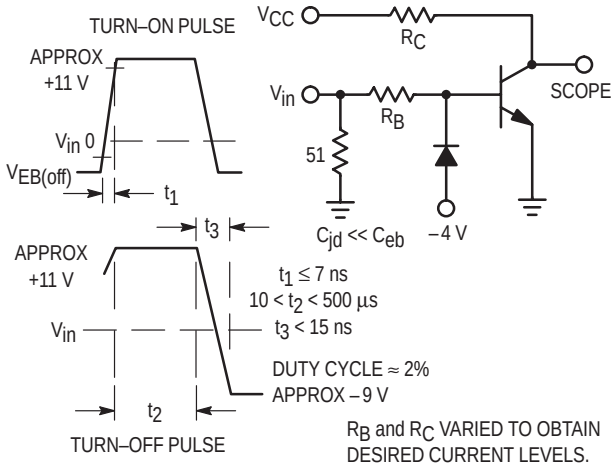


Figure 2. Switching Time Equivalent Circuit

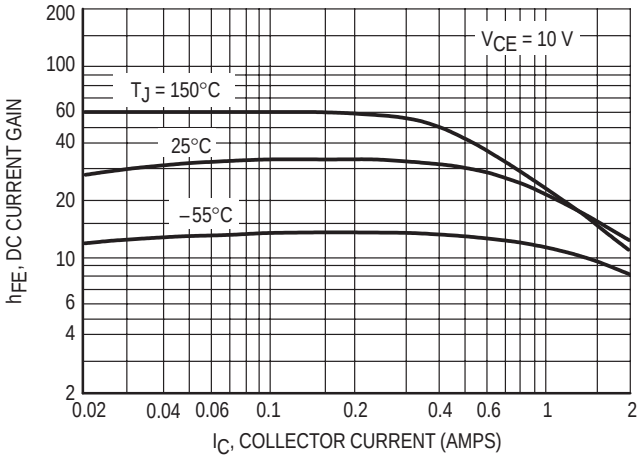


Figure 3. DC Current Gain

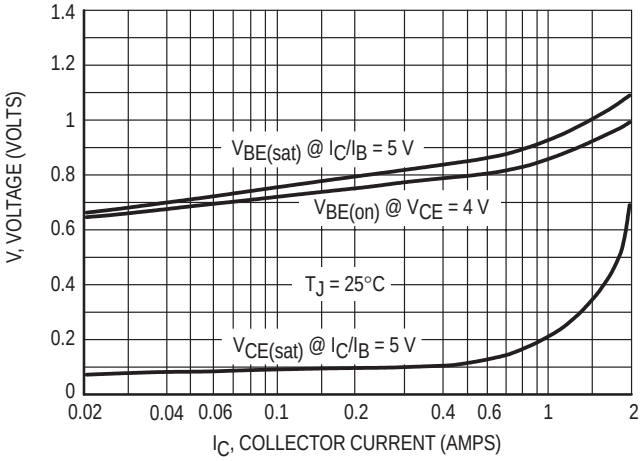


Figure 4. "On" Voltages

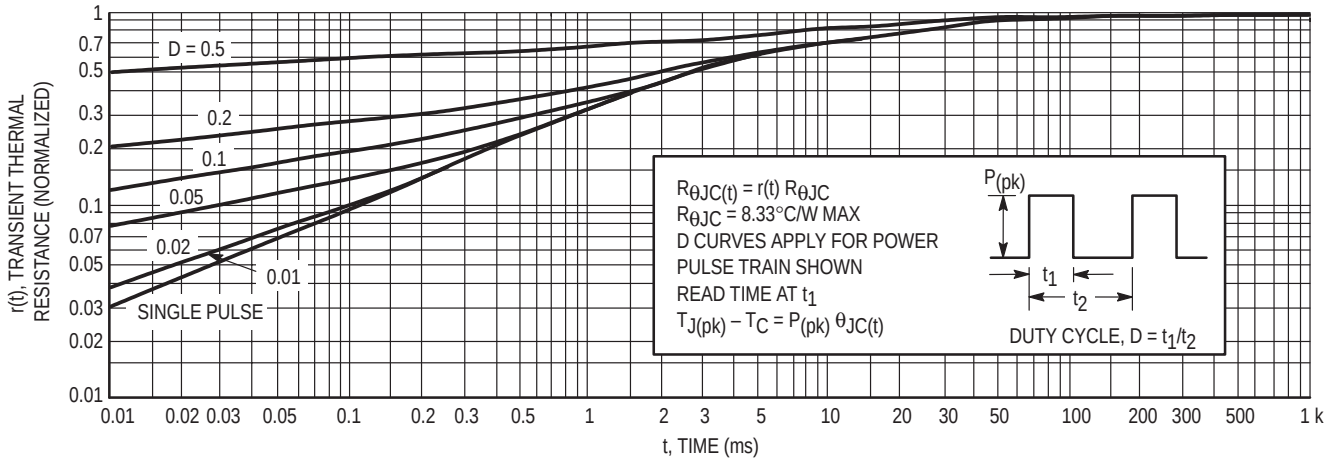


Figure 5. Thermal Response

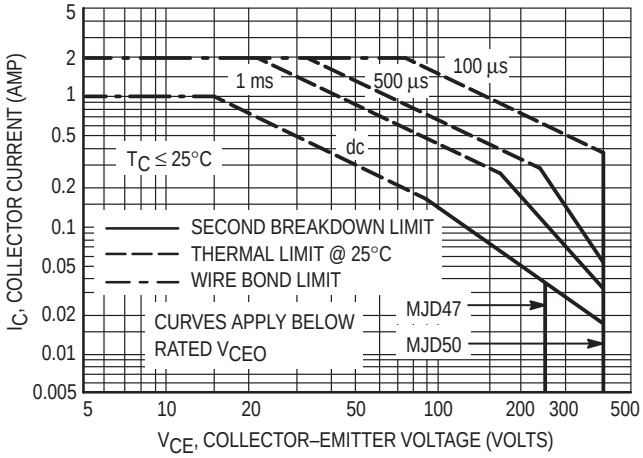


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

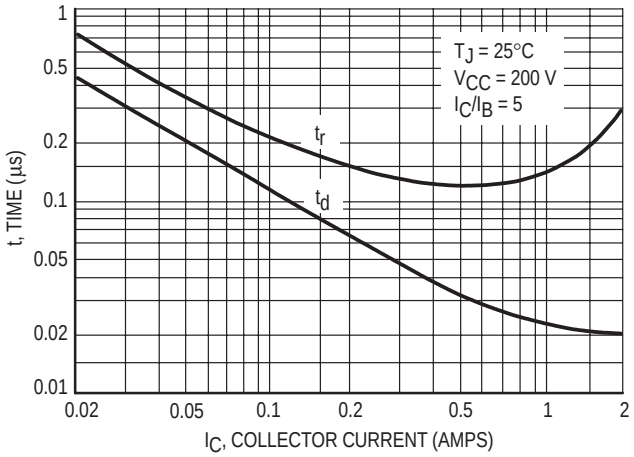


Figure 7. Turn–On Time

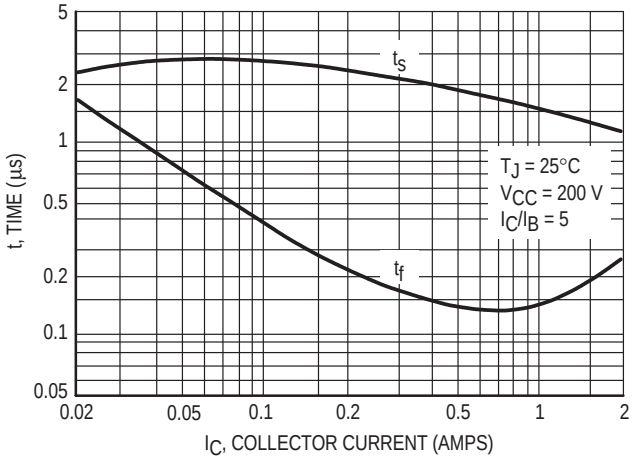


Figure 8. Turn-Off Time

Complementary Darlington Power Transistors

DPAK For Surface Mount Applications

NPN
MJD112*
PNP
MJD117*

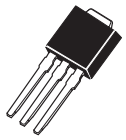
*Motorola Preferred Device

SILICON
POWER TRANSISTORS
2 AMPERES
100 VOLTS
20 WATTS

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("T4" Suffix)
- Surface Mount Replacements for TIP110–TIP117 Series
- Monolithic Construction With Built–in Base–Emitter Shunt Resistors
- High DC Current Gain — h_{FE} = 2500 (Typ) @ I_C = 2.0 Adc
- Complementary Pairs Simplifies Designs

CASE 369A–13



CASE 369–07

MAXIMUM RATINGS

Rating	Symbol	MJD112 MJD117	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	2 4	Adc
Base Current	I_B	50	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	°C/W

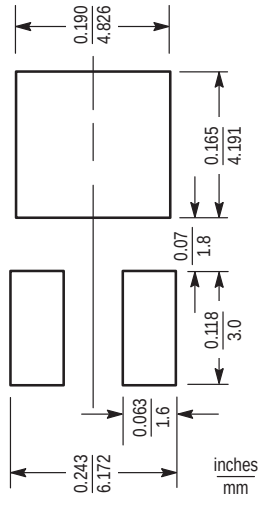
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	20	μAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	20	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	2	mAdc

* These ratings are applicable when surface mounted on the minimum pad sizes recommended.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

***ELECTRICAL CHARACTERISTICS — continued** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS – continued				
Collector–Cutoff Current (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	I_{CEX}	 — —	 10 500	μAdc
Collector–Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	—	10	μAdc
Emitter–Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	2	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3 Vdc) (I_C = 2 Adc, V_{CE} = 3 Vdc) (I_C = 4 Adc, V_{CE} = 3 Vdc)	h_{FE}	 500 1000 200	 — 12,000 —	—
Collector–Emitter Saturation Voltage (I_C = 2 Adc, I_B = 8 mAdc) (I_C = 4 Adc, I_B = 40 mAdc)	$V_{CE(sat)}$	 — —	 2 3	Vdc
Base–Emitter Saturation Voltage (I_C = 4 Adc, I_B = 40 mAdc)	$V_{BE(sat)}$	—	4	Vdc
Base–Emitter On Voltage (I_C = 2 Adc, V_{CE} = 3 Vdc)	$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	25	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJD117 MJD112	C_{ob}	 — —	 200 100	pF

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

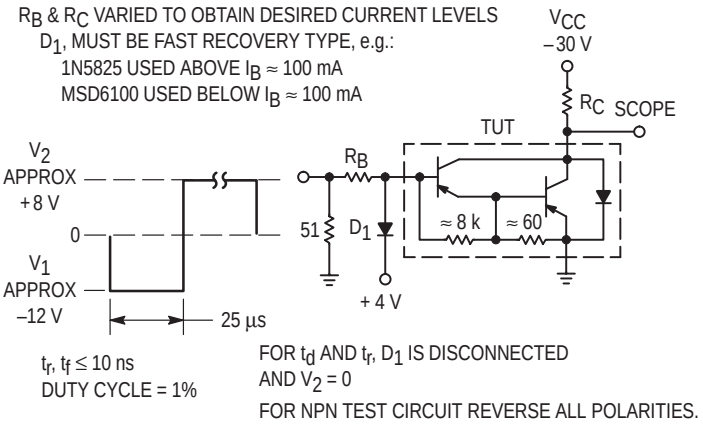


Figure 1. Switching Times Test Circuit

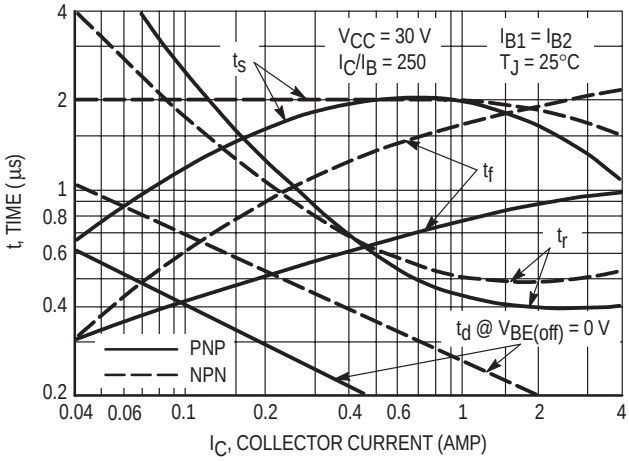


Figure 2. Switching Times

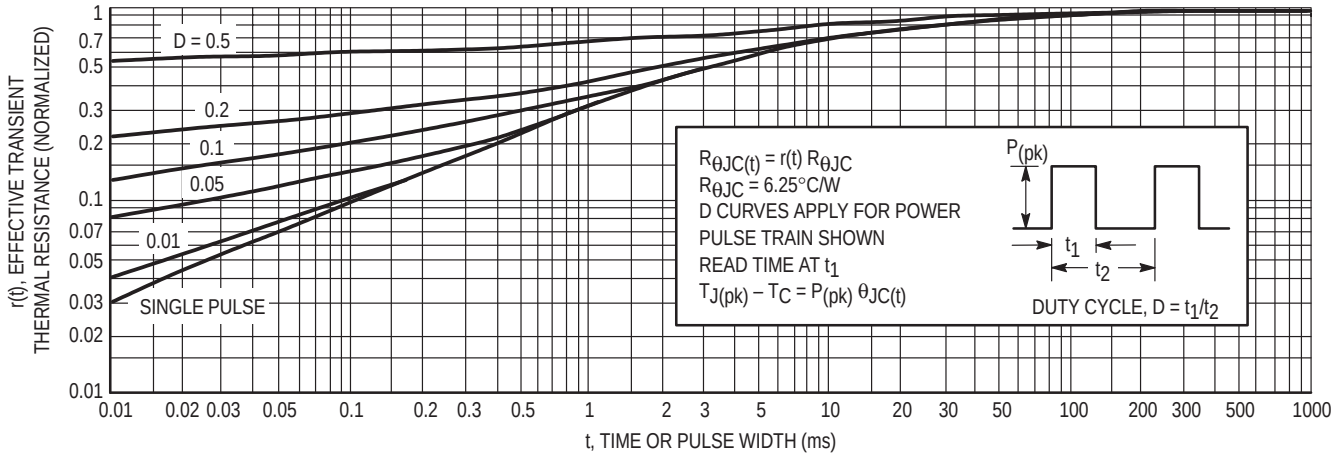


Figure 3. Thermal Response

ACTIVE–REGION SAFE–OPERATING AREA

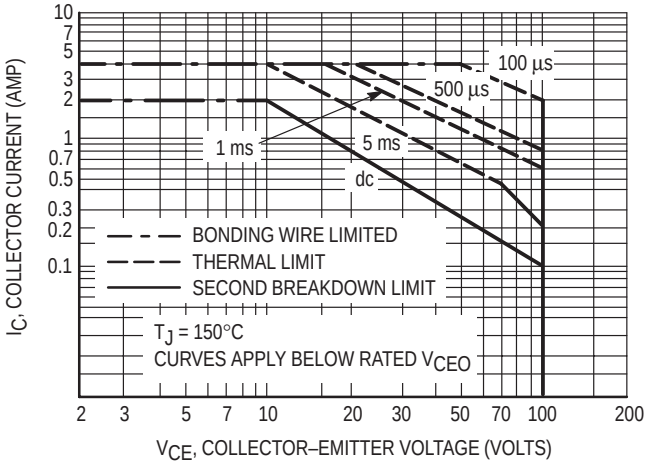


Figure 4. Maximum Rated Forward Biased Safe Operating Area

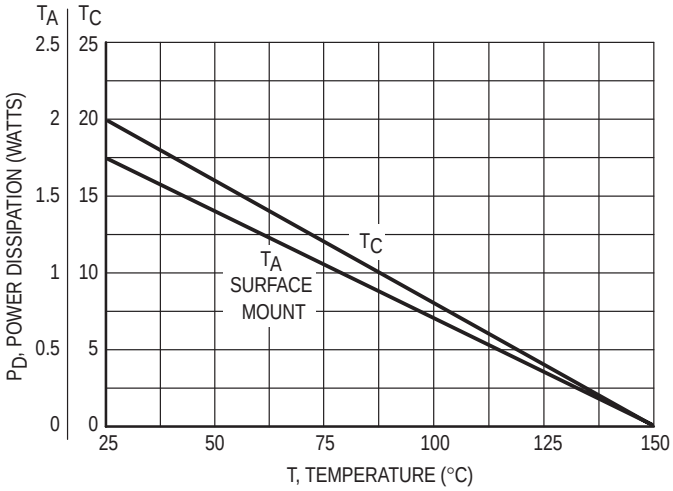


Figure 5. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

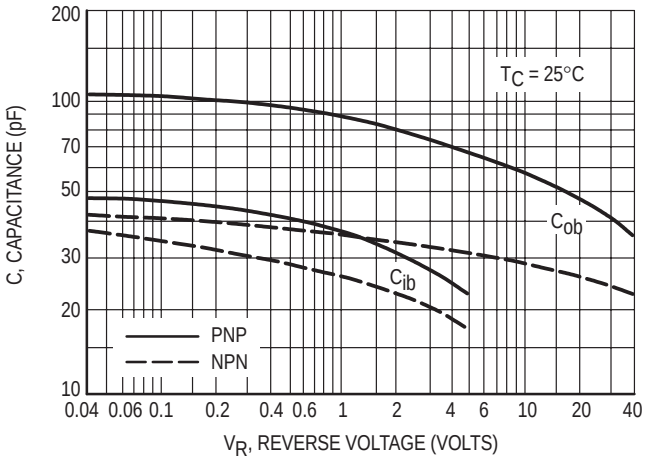
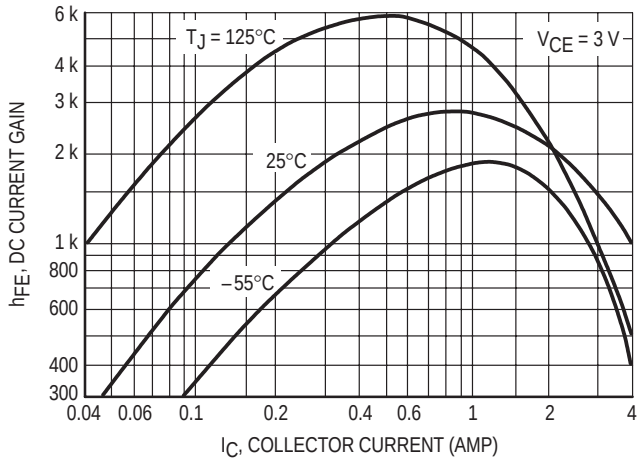


Figure 6. Capacitance

TYPICAL ELECTRICAL CHARACTERISTICS

NPN MJD112



PNP MJD117

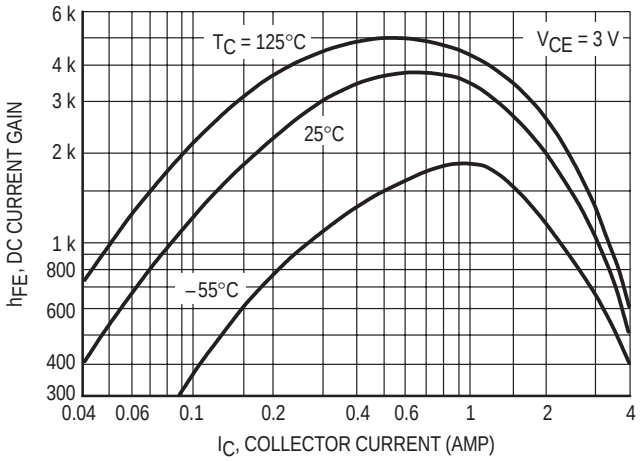
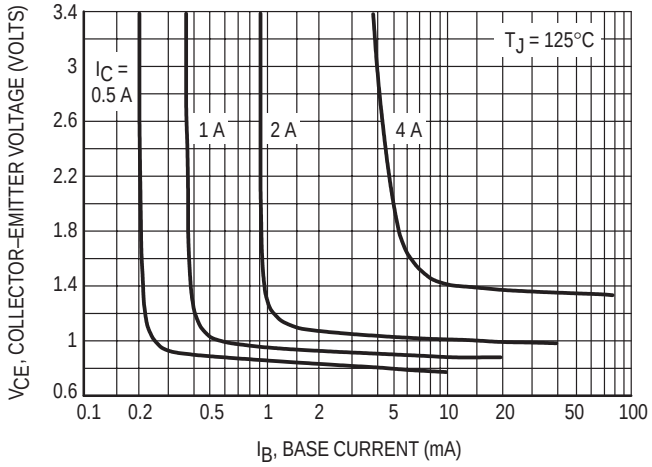


Figure 7. DC Current Gain



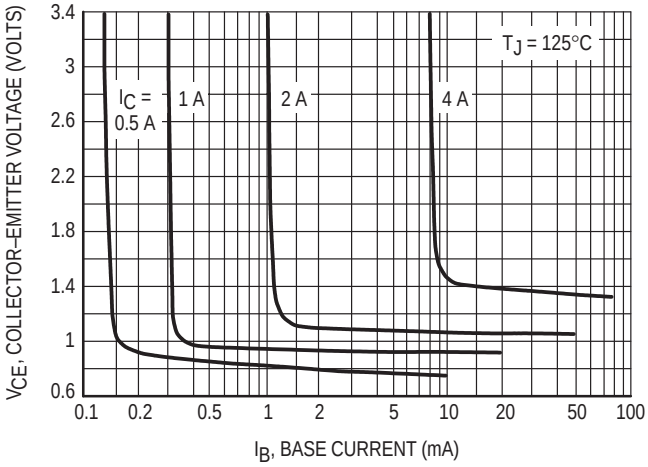
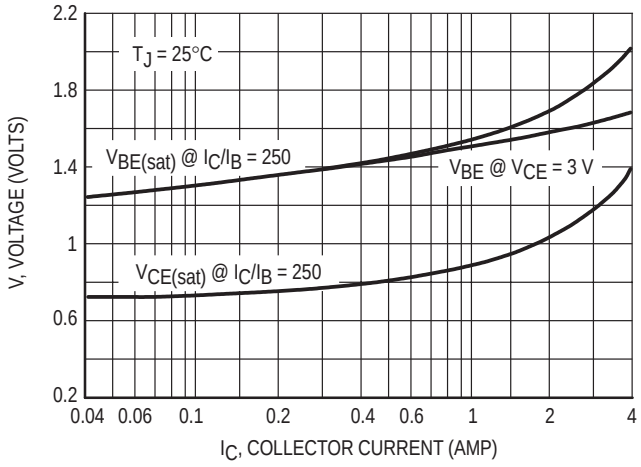


Figure 8. Collector Saturation Region



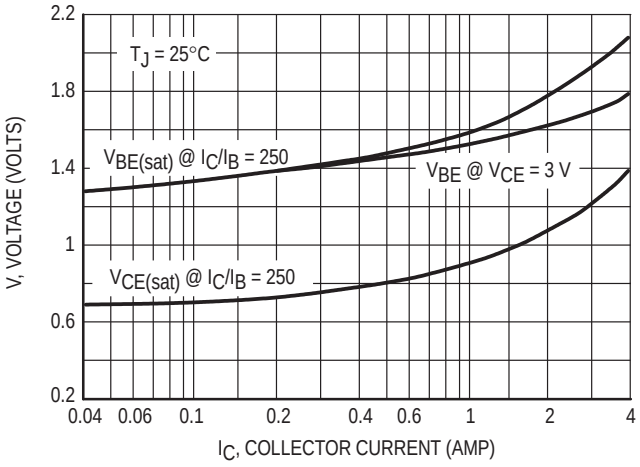
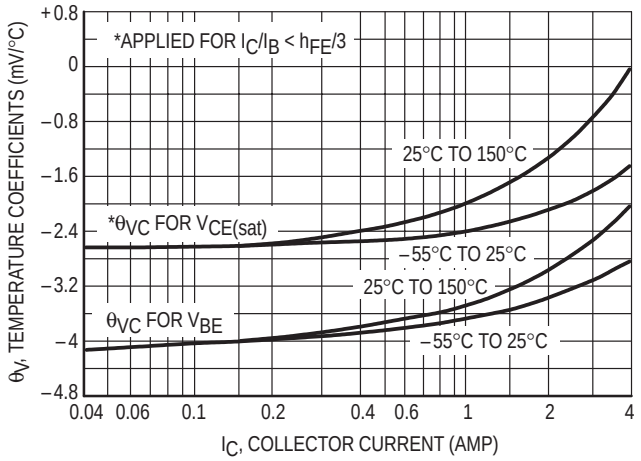


Figure 9. “On Voltages

NPN MJD112



PNP MJD117

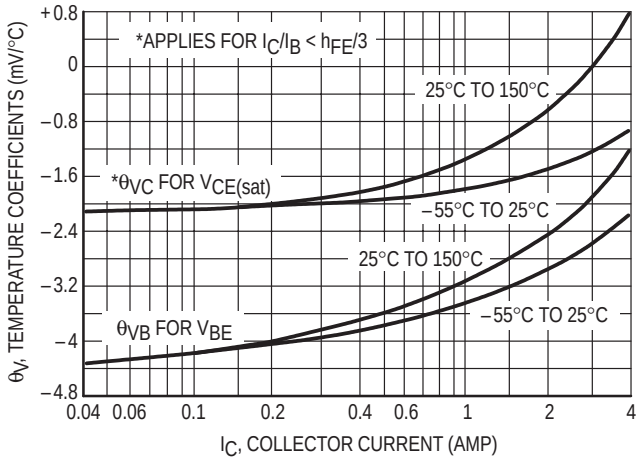
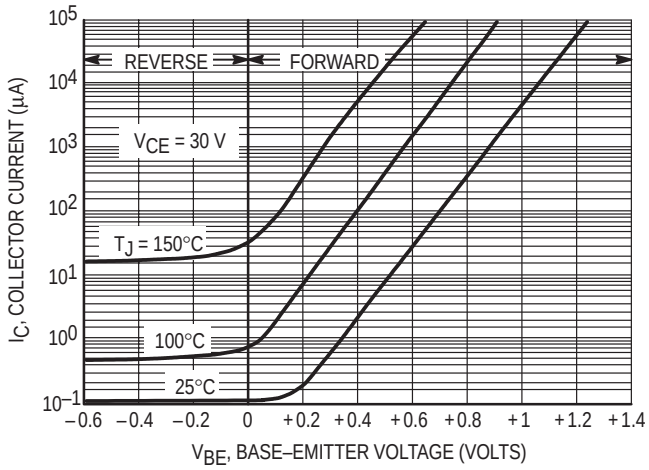


Figure 10. Temperature Coefficients



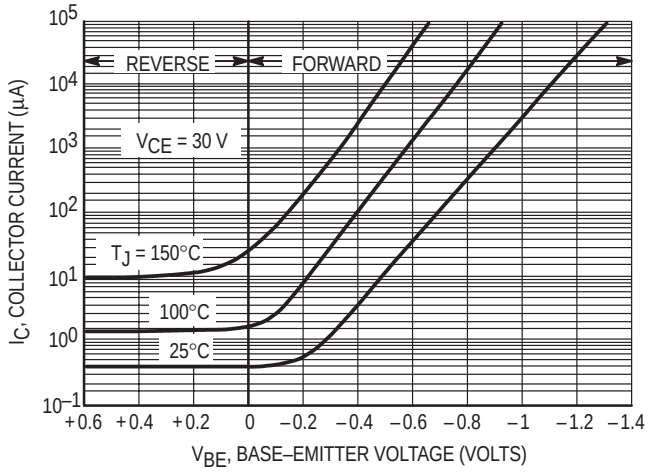


Figure 11. Collector Cut–Off Region

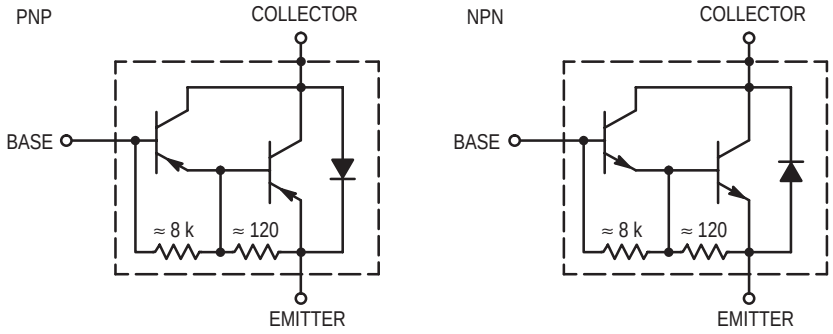


Figure 12. Darlington Schematic

Complementary Darlington Power Transistors

DPAK For Surface Mount Applications

NPN
MJD122*
PNP
MJD127*

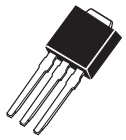
*Motorola Preferred Device

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version Available in 16 mm Tape and Reel ("T4" Suffix)
- Surface Mount Replacements for 2N6040–2N6045 Series, TIP120–TIP122 Series, and TIP125–TIP127 Series
- Monolithic Construction With Built–in Base–Emitter Shunt Resistors
- High DC Current Gain — h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Complementary Pairs Simplifies Designs

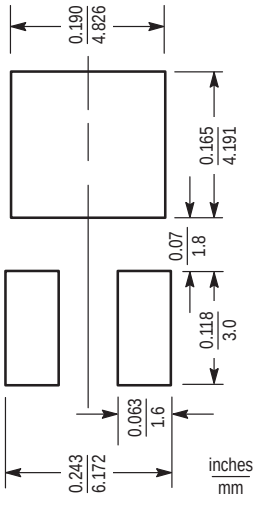
SILICON
POWER TRANSISTORS
8 AMPERES
100 VOLTS
20 WATTS

CASE 369A–13



CASE 369–07

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	MJD122 MJD127	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	8 16	Adc
Base Current	I_B	120	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	10	μAdc

* These ratings are applicable when surface mounted on the minimum pad sizes recommended.

(continued)

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued				
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	I_{CEX}	 — —	 10 500	μAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	2	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 4 Adc, V_{CE} = 4 Vdc) (I_C = 8 Adc, V_{CE} = 4 Vdc)	h_{FE}	 1000 100	 12,000 —	—
Collector–Emitter Saturation Voltage (I_C = 4 Adc, I_B = 16 mAdc) (I_C = 8 Adc, I_B = 80 mAdc)	$V_{CE(sat)}$	 — —	 2 4	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 8 Adc, I_B = 80 mAdc)	$V_{BE(sat)}$	—	4.5	Vdc
Base–Emitter On Voltage (I_C = 4 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain–Bandwidth Product (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 MHz)	$\|h_{fe}\|$	4	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJD127 MJD122	C_{ob}	 — —	 300 200	pF
Small–Signal Current Gain (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 kHz)	h_{fe}	300	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

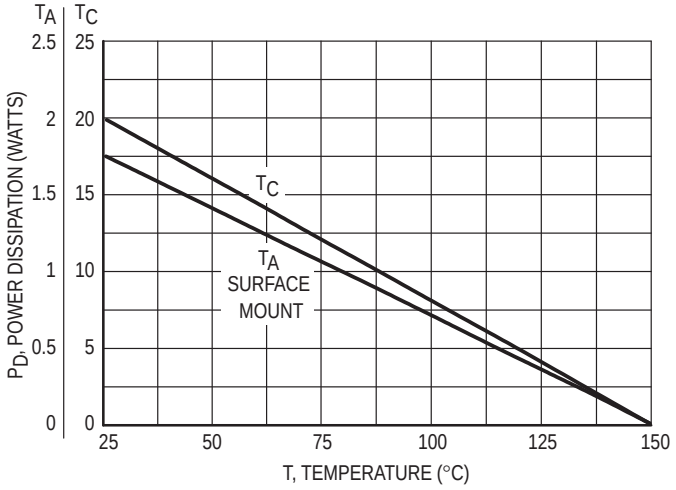
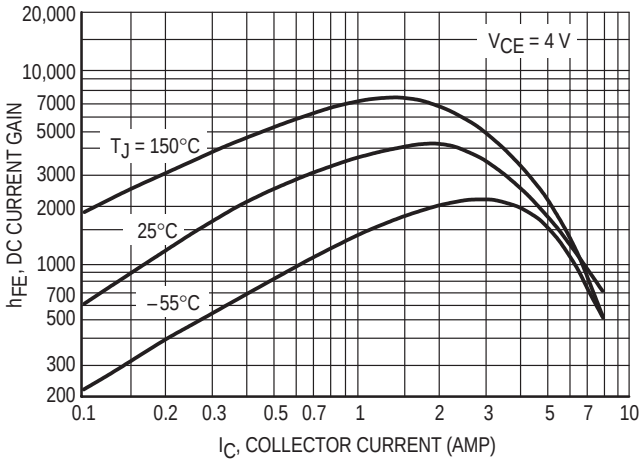


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

PNP MJD127



NPN MJD122

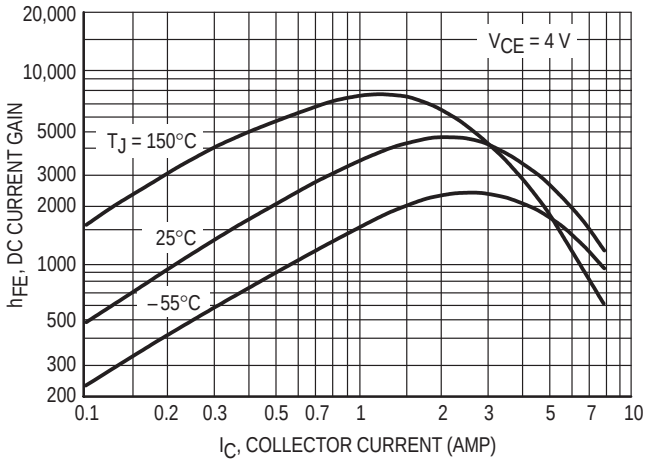
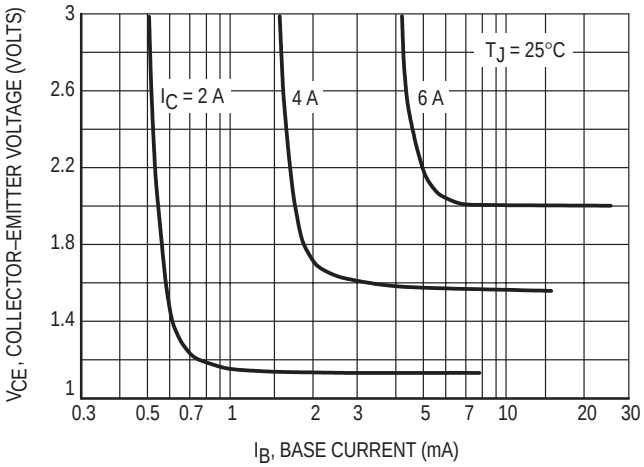


Figure 2. DC Current Gain



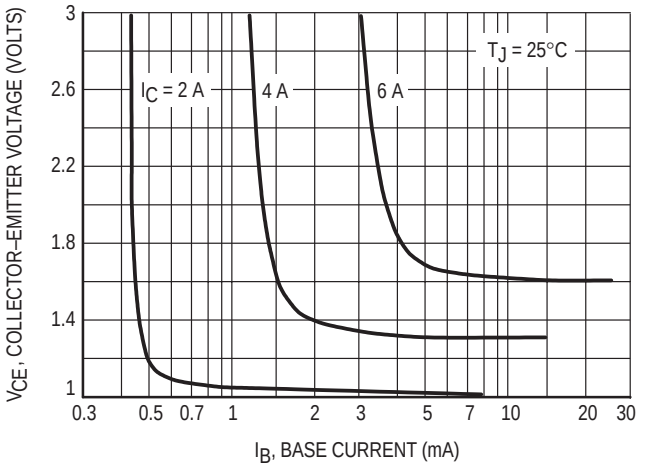
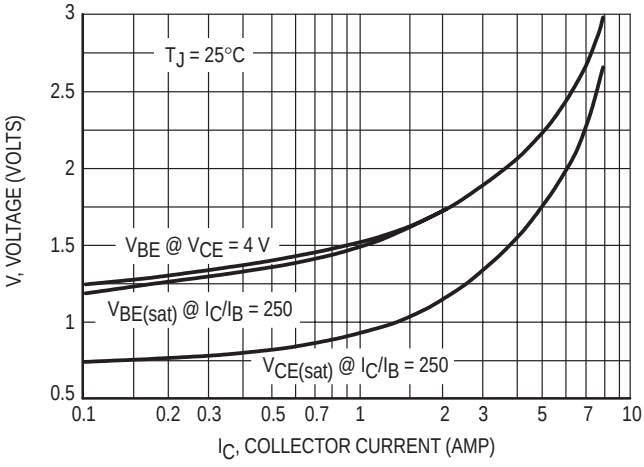


Figure 3. Collector Saturation Region



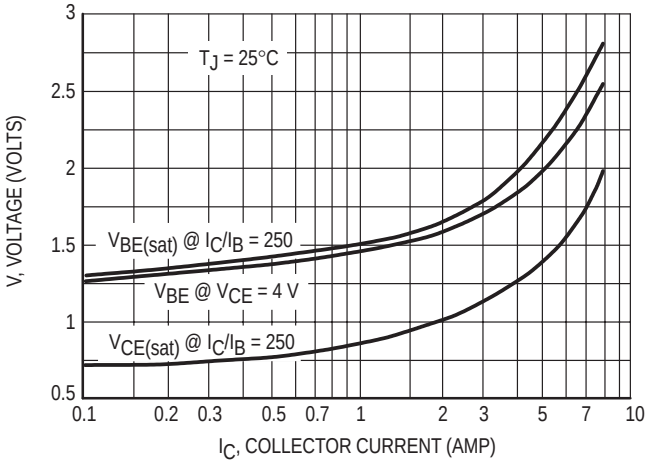
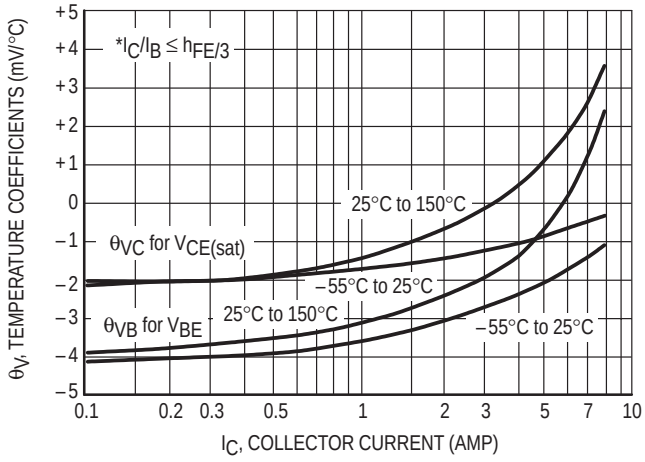


Figure 4. “On” Voltages

TYPICAL ELECTRICAL CHARACTERISTICS

PNP MJD127



NPN MJD122

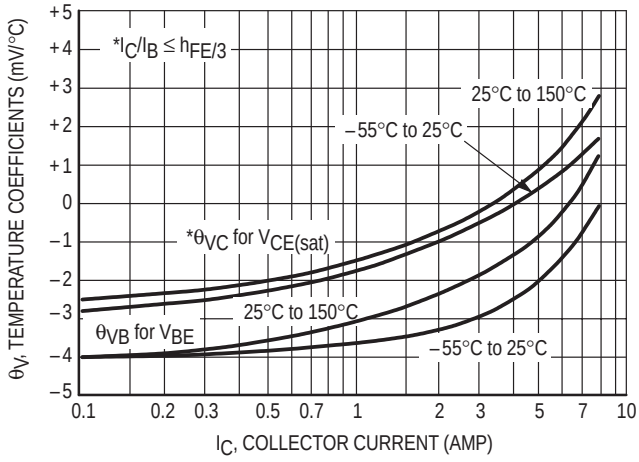
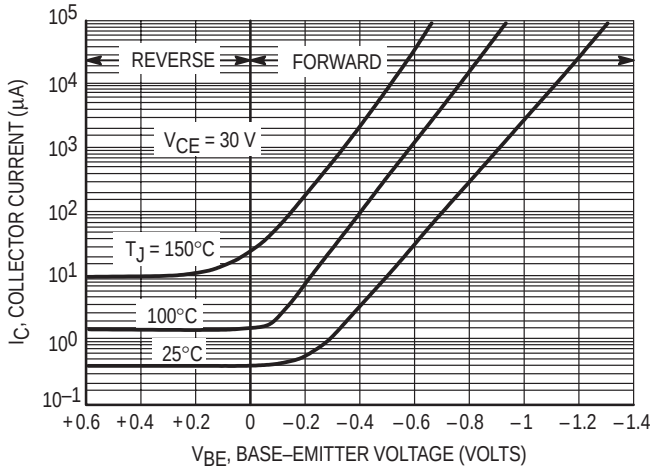


Figure 5. Temperature Coefficients



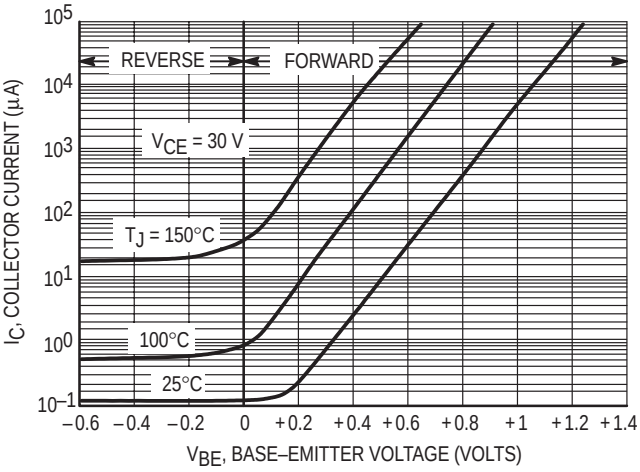


Figure 6. Collector Cut–Off Region

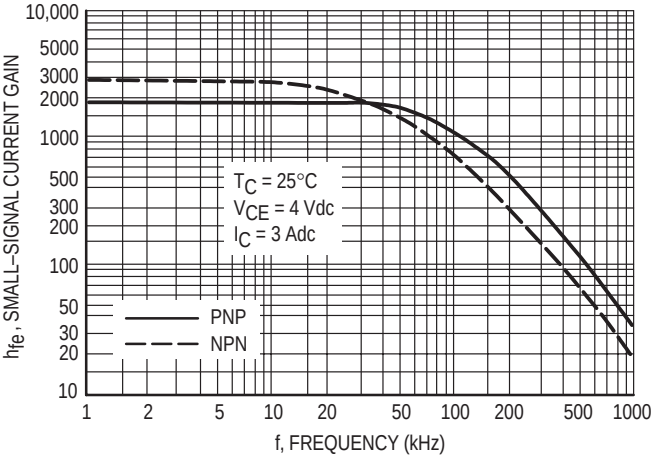


Figure 7. Small–Signal Current Gain

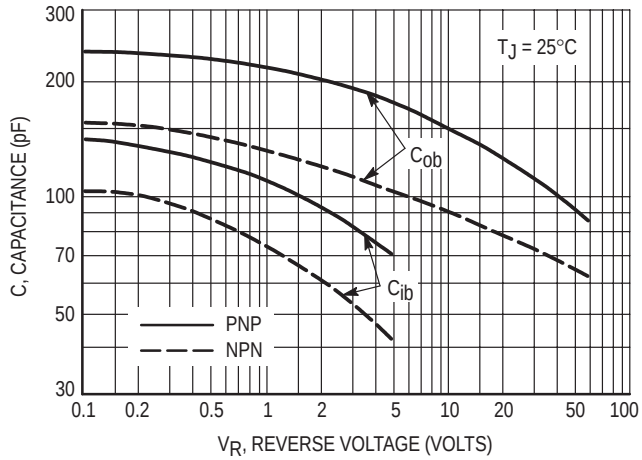


Figure 8. Capacitance

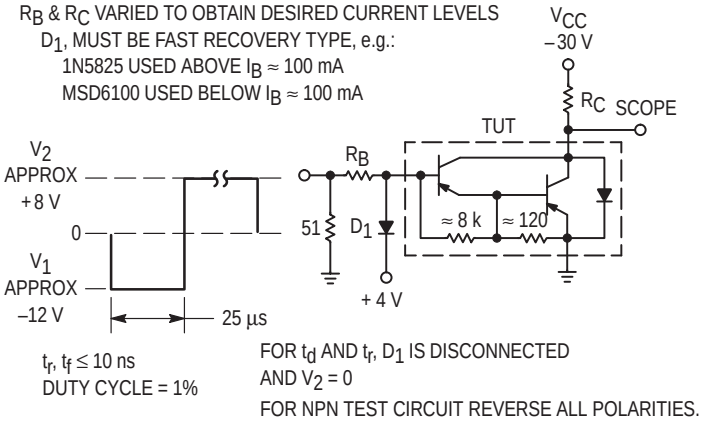


Figure 9. Switching Times Test Circuit

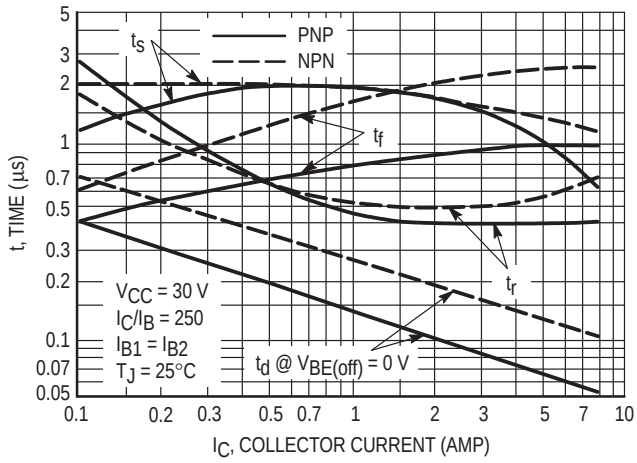


Figure 10. Switching Times

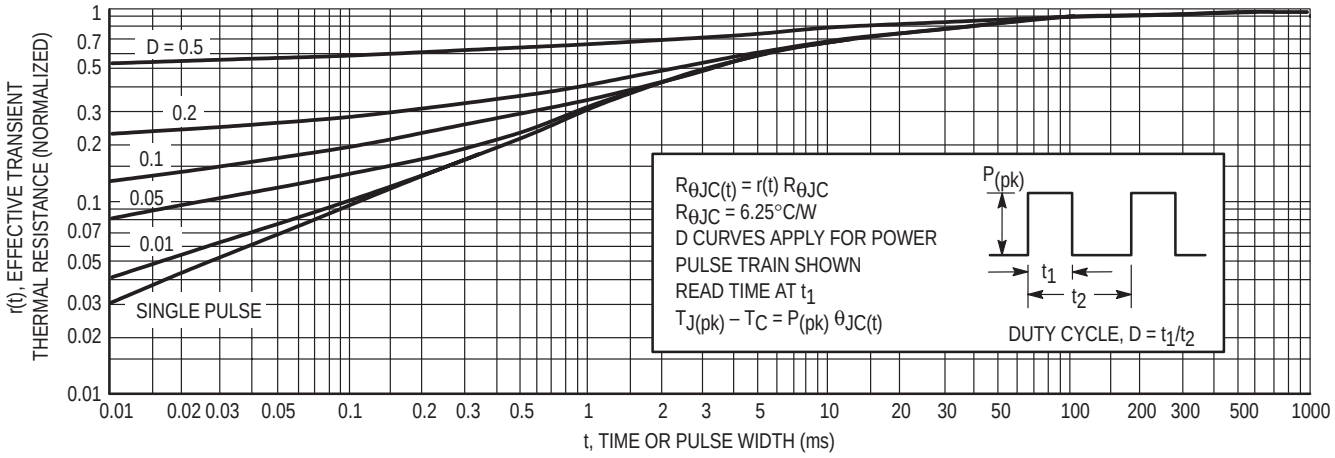


Figure 11. Thermal Response

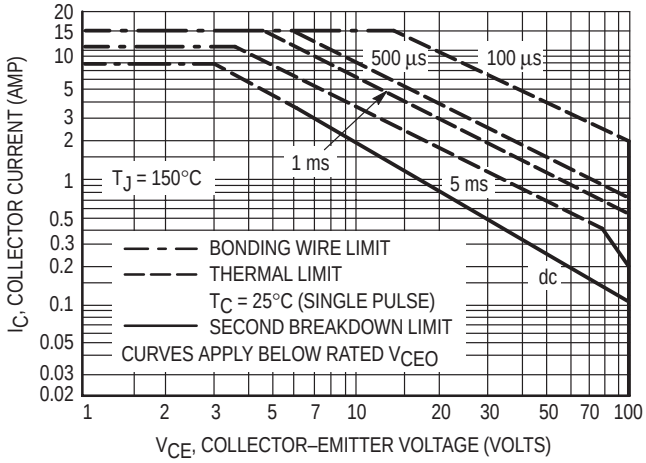


Figure 12. Maximum Forward Bias Safe Operating rea

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

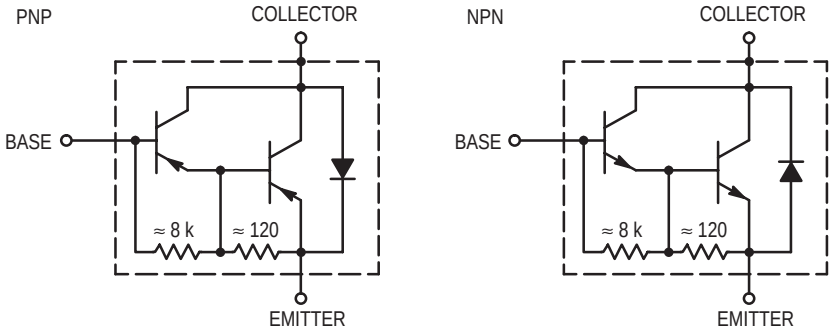


Figure 13. Darlington Schematic

Complementary Plastic Power Transistors

NPN/PNP Silicon DPAK For Surface Mount Applications

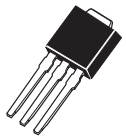
. . . designed for low voltage, low–power, high–gain audio amplifier applications.

- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 25 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain — h_{FE} = 70 (Min) @ I_C = 500 mAdc
  = 45 (Min) @ I_C = 2 Adc
  = 10 (Min) @ I_C = 5 Adc
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("T4" Suffix)
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.75 Vdc (Max) @ I_C = 2.0 Adc
- High Current–Gain — Bandwidth Product — f_T = 65 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakage — I_{CBO} = 100 nAdc @ Rated V_{CB}

NPN
MJD200
PNP
MJD210

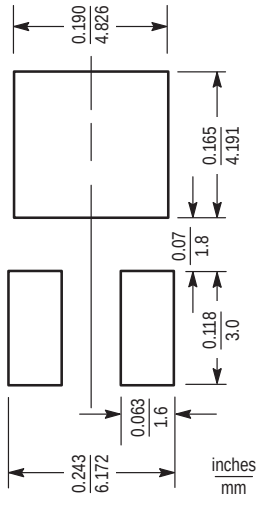
SILICON
POWER TRANSISTORS
5 AMPERES
25 VOLTS
12.5 WATTS

CASE 369A–13



CASE 369–07

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CB}	40	Vdc
Collector–Emitter Voltage	V_{CEO}	25	Vdc
Emitter–Base Voltage	V_{EB}	8	Vdc
Collector Current — Continuous Peak	I_C	5 10	Adc
Base Current	I_B	1	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.1	Watts W/°C
Total Device Dissipation @ T_A = 25°C* Derate above 25°C	P_D	1.4 0.011	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Junction to Ambient*	$R_{\theta JC}$ $R_{\theta JA}$	10 89.3	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	25	—	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}	 — —	 100 100	nAdc
Emitter Cutoff Current (V_{BE} = 8 Vdc, I_C = 0)	I_{EBO}	—	100	nAdc

* When surface mounted on minimum pad sizes recommended. (continued)

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.

REV 1

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 500 mAdc, V_{CE} = 1 Vdc) (I_C = 2 Adc, V_{CE} = 1 Vdc) (I_C = 5 Adc, V_{CE} = 2 Vdc)		h_{FE}	 70 45 10	 — 180 —	—
Collector–Emitter Saturation Voltage (1) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 2 Adc, I_B = 200 mAdc) (I_C = 5 Adc, I_B = 1 Adc)		$V_{CE(sat)}$	 — — —	 0.3 0.75 1.8	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 5 Adc, I_B = 1 Adc)		$V_{BE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (1) (I_C = 2 Adc, V_{CE} = 1 Vdc)		$V_{BE(on)}$	—	1.6	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	65	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJD200 MJD210	C_{ob}	— —	80 120	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

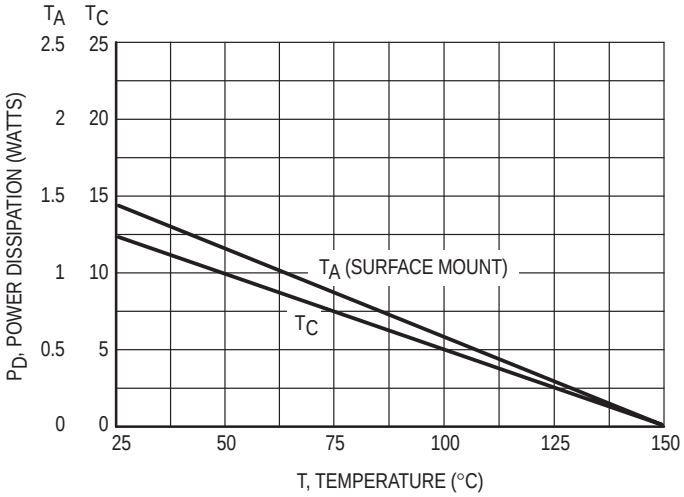


Figure 1. Power Derating

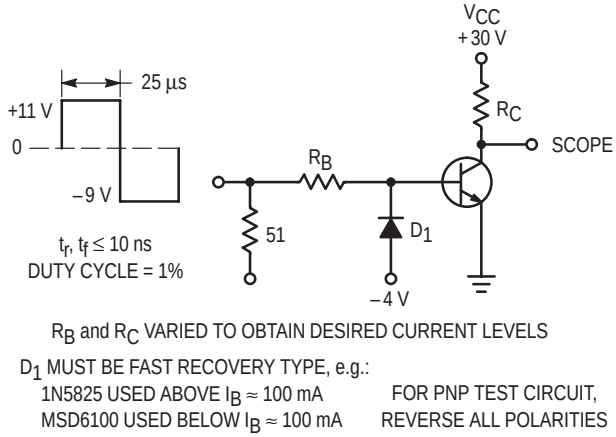


Figure 2. Switching Time Test Circuit

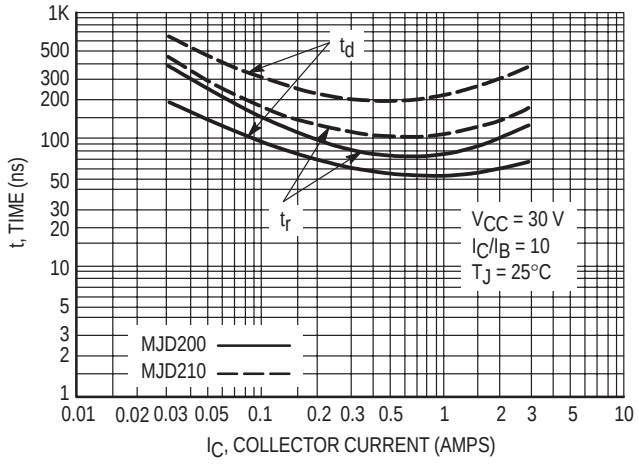


Figure 3. Turn–On Time

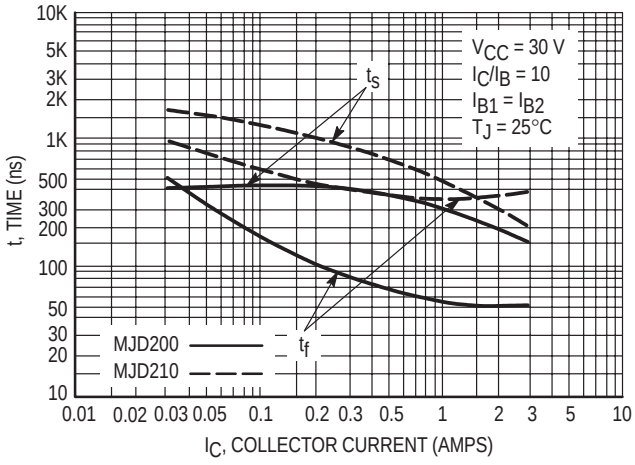
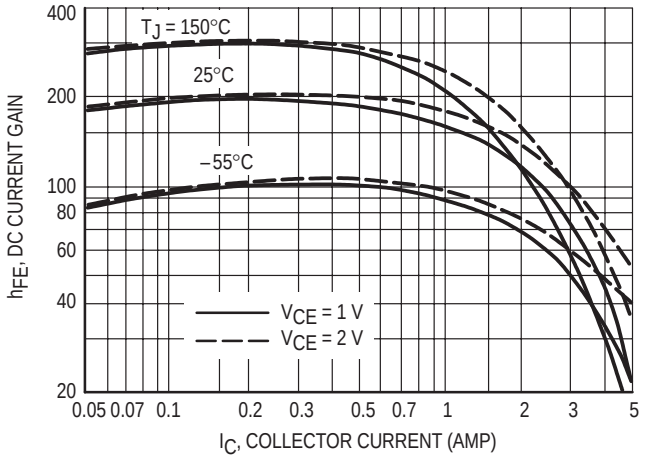


Figure 4. Turn–Off Time

NPN
MJD200



PNP
MJD210

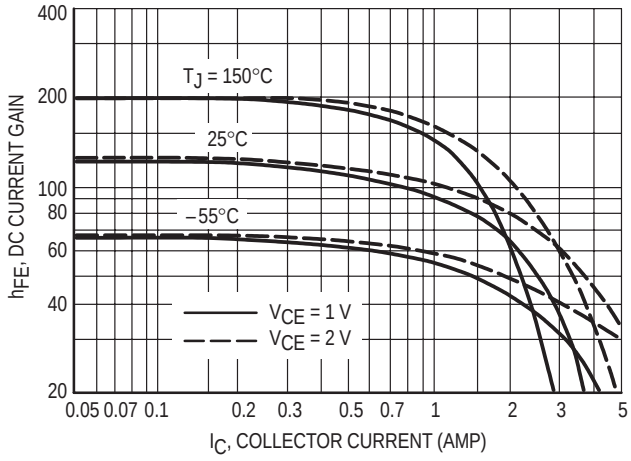
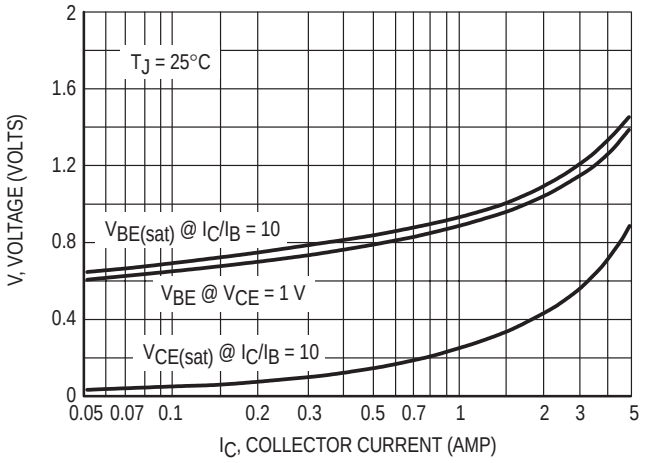


Figure 5. DC Current Gain



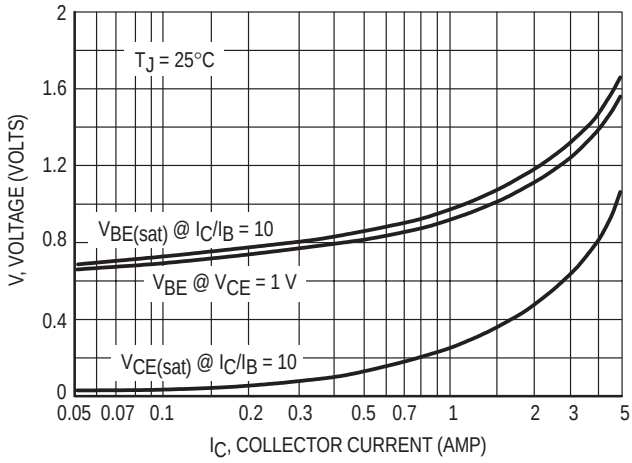
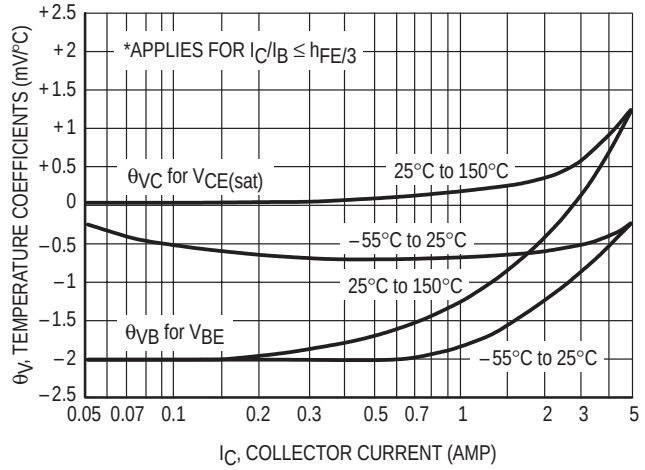


Figure 6. “On” Voltage



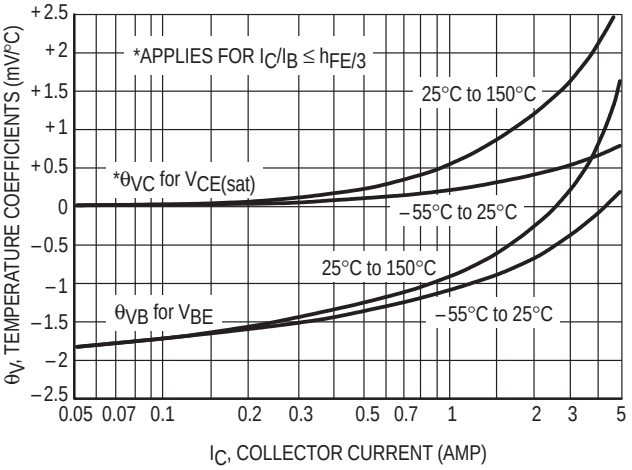


Figure 7. Temperature Coefficients

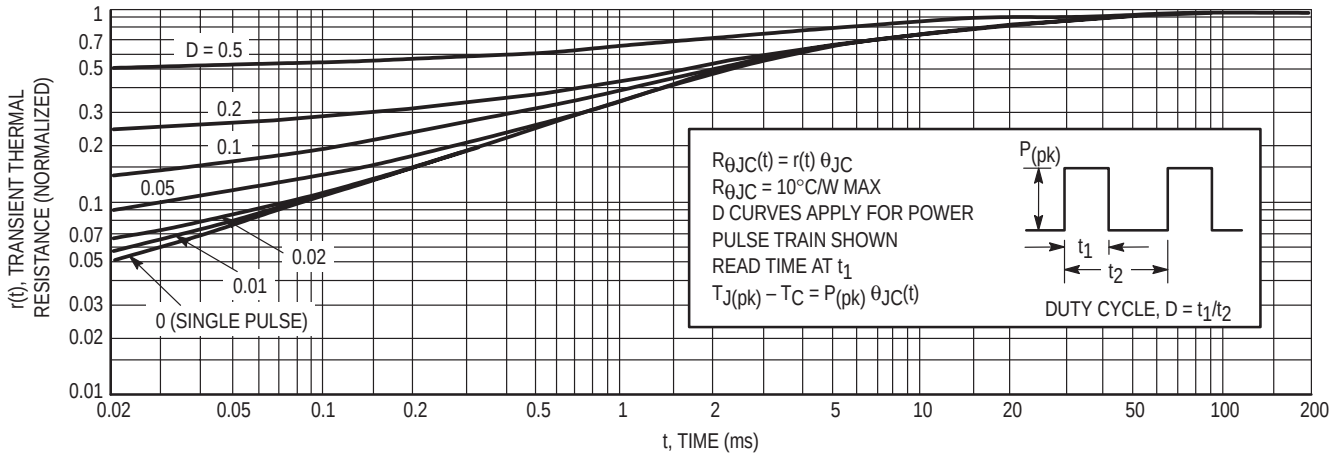


Figure 8. Thermal Response

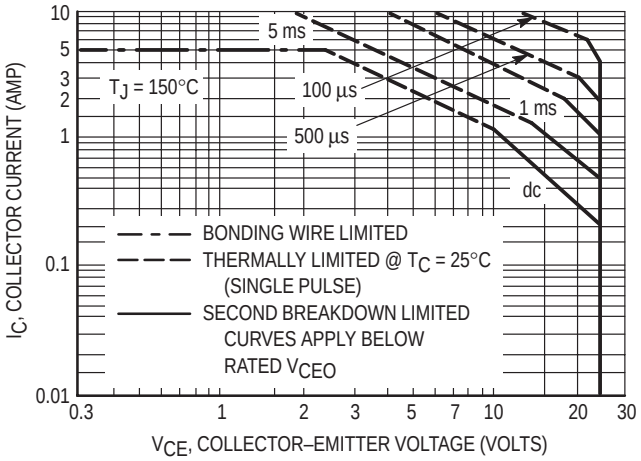


Figure 9. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Case 369–05 may be ordered by adding a "–1" suffix to the device title (i.e. MJD200–1)

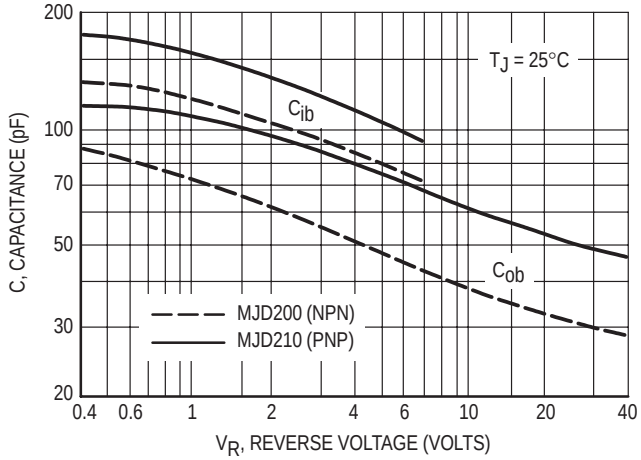


Figure 10. Capacitance

Plastic Power Transistor

DPAK For Surface Mount Applications

. . . designed for low voltage, low–power, high–gain audio amplifier applications.

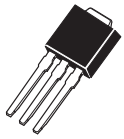
- Collector–Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 100 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain — h_{FE} = 40 (Min) @ I_C = 200 mAdc
  = 15 (Min) @ I_C = 1.0 Adc
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“–1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.6 Vdc (Max) @ I_C = 1.0 Adc
- High Current–Gain — Bandwidth Product — f_T = 40 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakage — I_{CBO} = 100 nAdc @ Rated V_{CB}

MJD243*

*Motorola Preferred Device

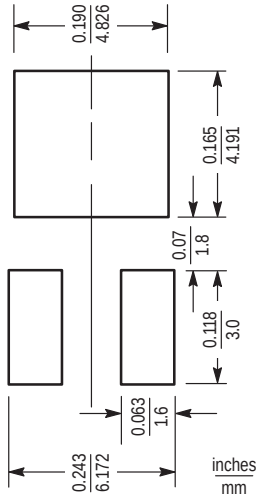
NPN SILICON
POWER TRANSISTOR
4 AMPERES
100 VOLTS
12.5 WATTS

CASE 369A–13



CASE 369–07

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CB}	100	Vdc
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Emitter–Base Voltage	V_{EB}	7	Vdc
Collector Current — Continuous Peak	I_C	4 8	Adc
Base Current	I_B	1	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.1	Watts W/°C
Total Device Dissipation @ T_A = 25°C* Derate above 25°C	P_D	1.4 0.011	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Junction to Ambient*	$R_{\theta JC}$ $R_{\theta JA}$	10 89.3	°C/W

* When surface mounted on minimum pad sizes recommended.

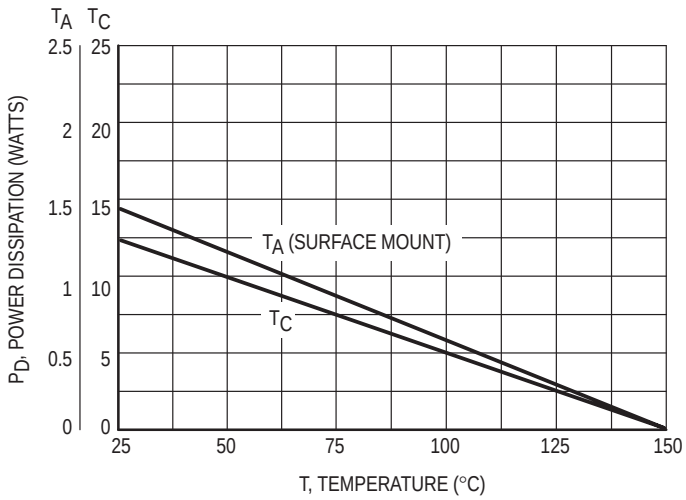


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0, T_J = 125°C)	I_{CBO}	— —	100 100	nAdc μAdc
Emitter Cutoff Current (V_{BE} = 7 Vdc, I_C = 0)	I_{EBO}	—	100	nAdc
DC Current Gain (1) (I_C = 200 mAdc, V_{CE} = 1 Vdc) (I_C = 1 Adc, V_{CE} = 1 Vdc)	h_{FE}	40 15	180 —	—
Collector–Emitter Saturation Voltage (1) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 1 Adc, I_B = 100 mAdc)	$V_{CE(sat)}$	 — —	 0.3 0.6	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 2 Adc, I_B = 200 mAdc)	$V_{BE(sat)}$	—	1.8	Vdc
Base–Emitter On Voltage (1) (I_C = 500 mAdc, V_{CE} = 1 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	40	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	50	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≈ 2%.
(2) $f_T = |h_{FE}| \bullet f_{test}$.

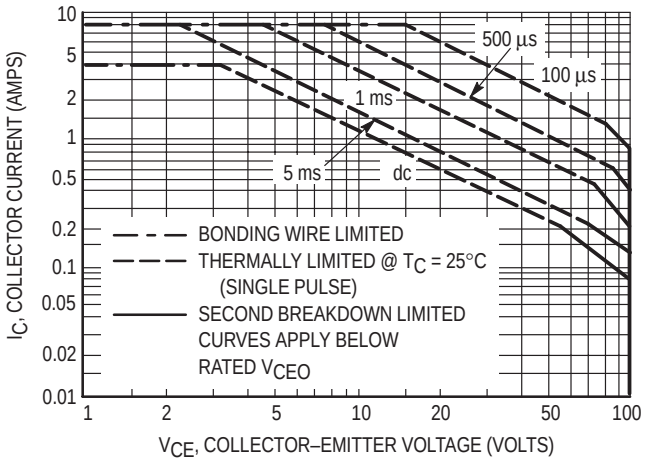


Figure 2. Active Region Maximum Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

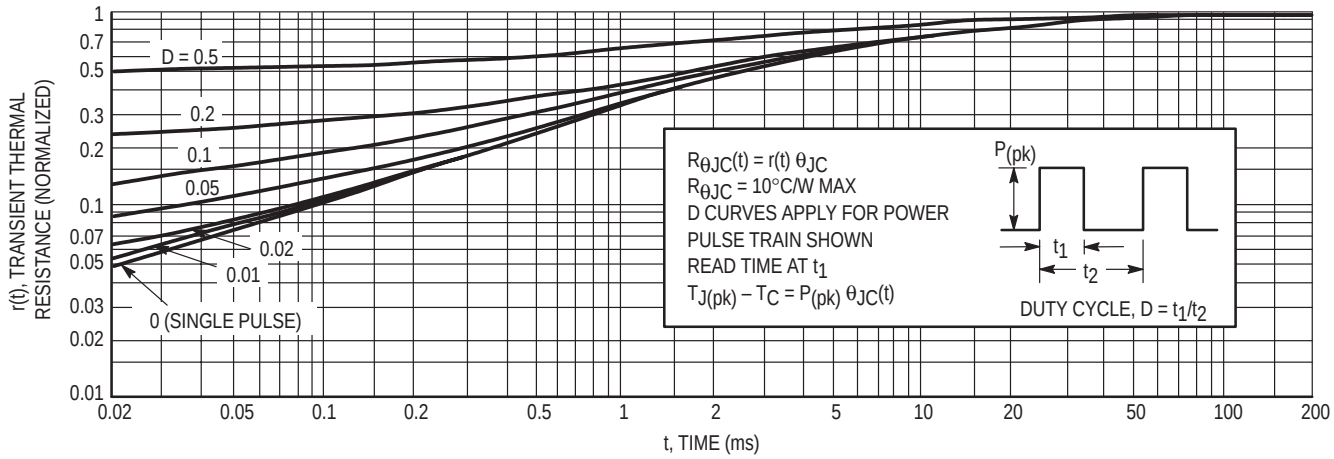


Figure 3. Thermal Response

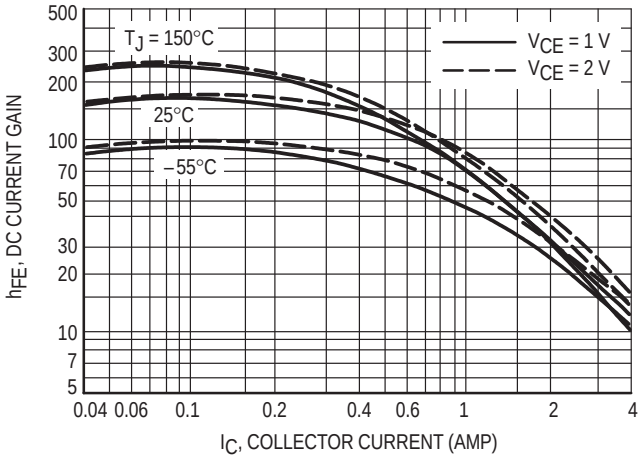


Figure 4. DC Current Gain

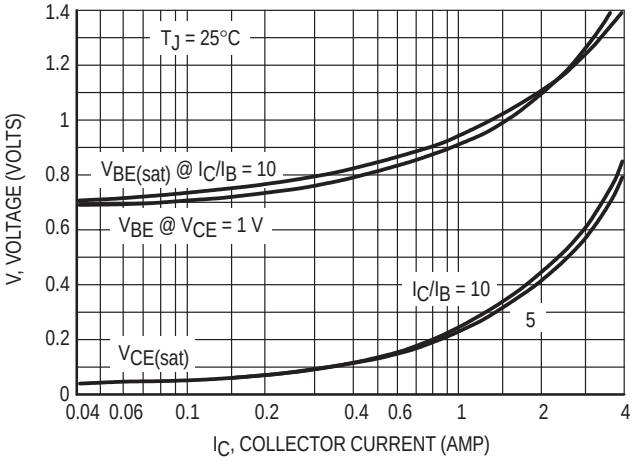


Figure 5. “On” Voltages

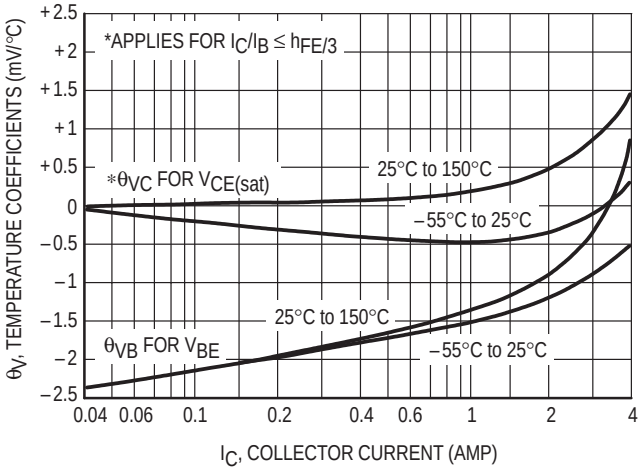


Figure 6. Temperature Coefficients

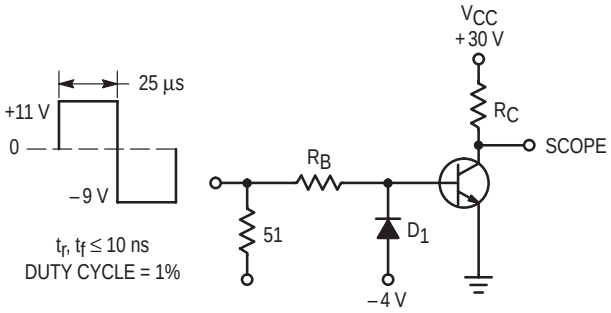


Figure 7. Switching Time Test Circuit

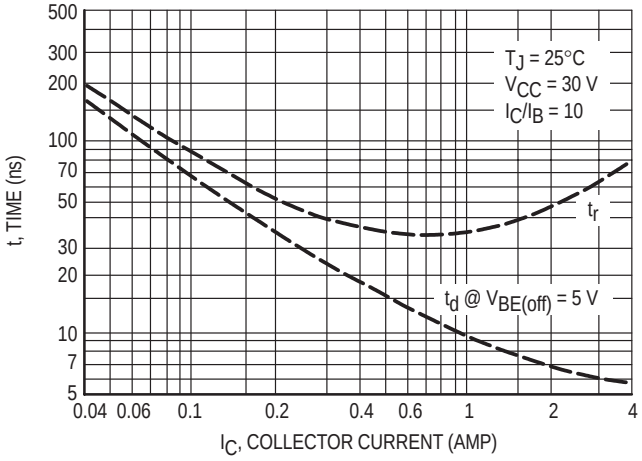


Figure 8. Turn–On Time

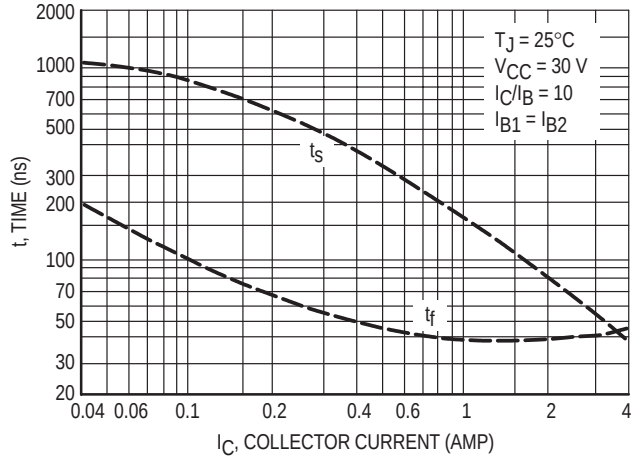


Figure 9. Turn–Off Time

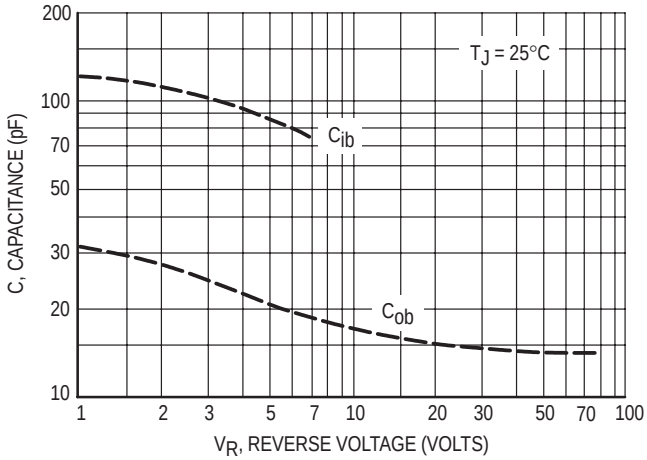


Figure 10. Capacitance

High Voltage Power Transistors
DPAK For Surface Mount Applications

Designed for line operated audio output amplifier, switchmode power supply drivers and other switching applications.

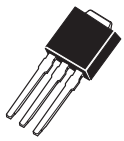
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("T4" Suffix)
- Electrically Similar to Popular MJE340 and MJE350
- 300 V (Min) — $V_{CEO(sus)}$
- 0.5 A Rated Collector Current

NPN
MJD340*
PNP
MJD350*

*Motorola Preferred Device

SILICON
POWER TRANSISTORS
0.5 AMPERE
300 VOLTS
15 WATTS

CASE 369A–13



CASE 369–07

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	300	Vdc
Collector–Base Voltage	V_{CB}	300	Vdc
Emitter–Base Voltage	V_{EB}	3	Vdc
Collector Current — Continuous — Peak	I_C	0.5 0.75	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.56 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

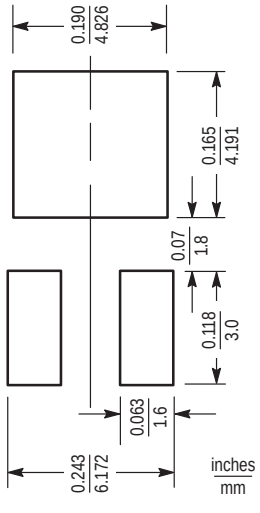
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	80	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 1 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	—	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 3 Vdc, I_C = 0)	I_{EBO}	—	0.1	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	—

* When surface mounted on minimum pad sizes recommended.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are Motorola recommended choices for future use and best overall value.

TYPICAL CHARACTERISTICS

MJD340

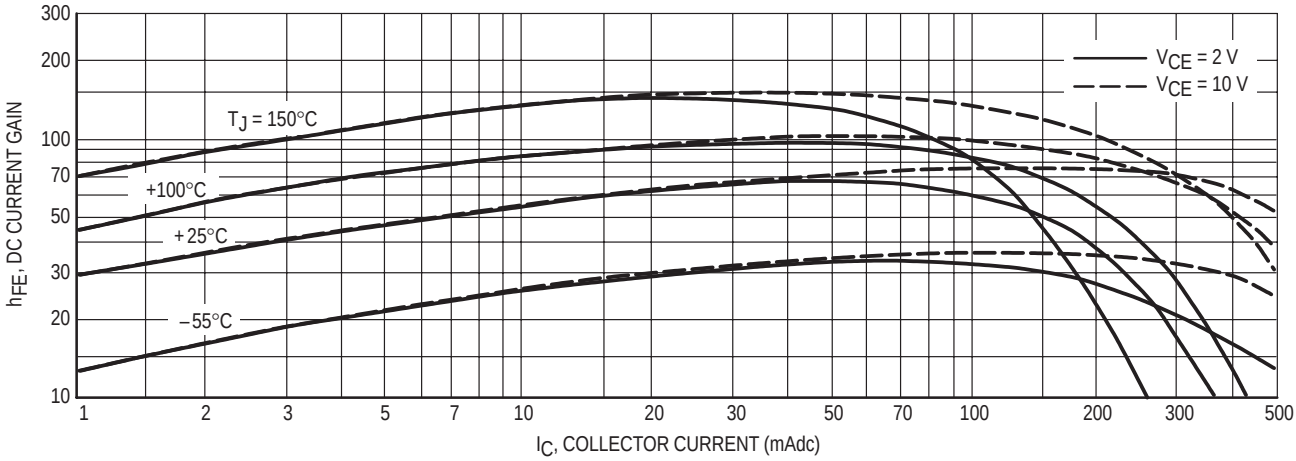


Figure 1. DC Current Gain

MJD340

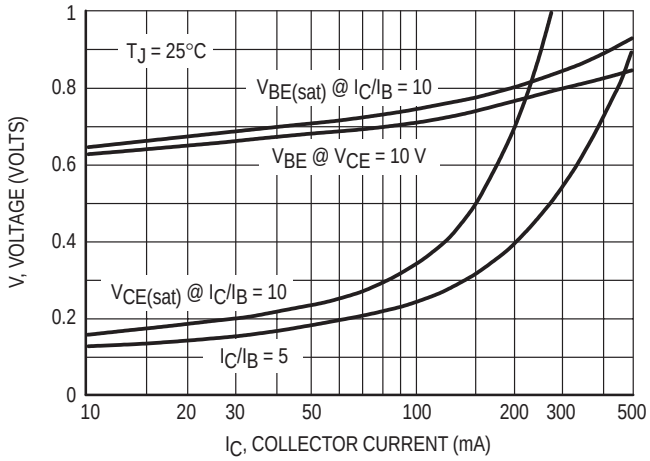


Figure 2. “On” Voltages

MJD350

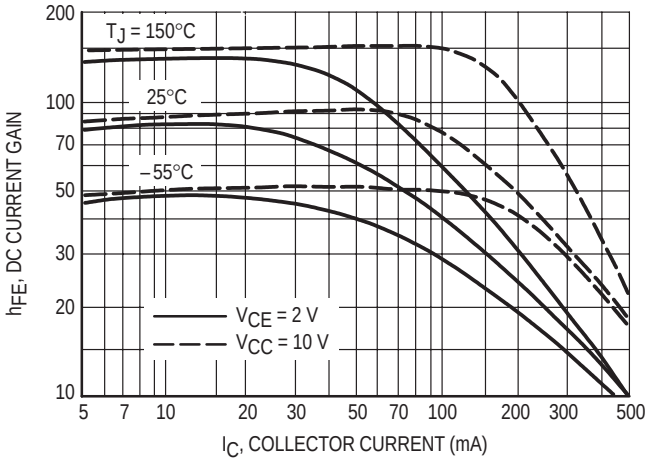


Figure 3. DC Current Gain

MJD350

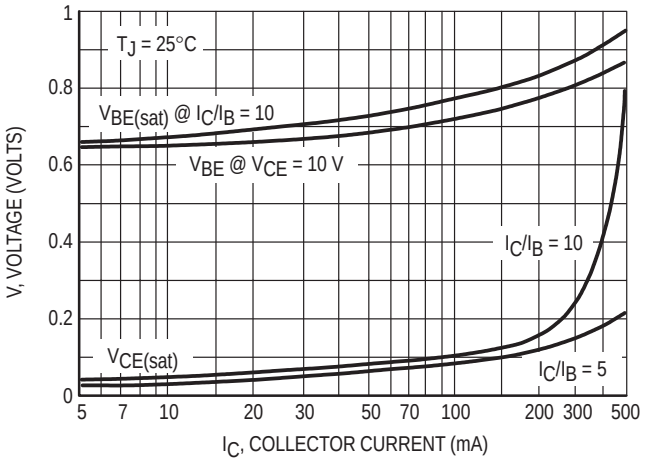


Figure 4. “On” Voltages

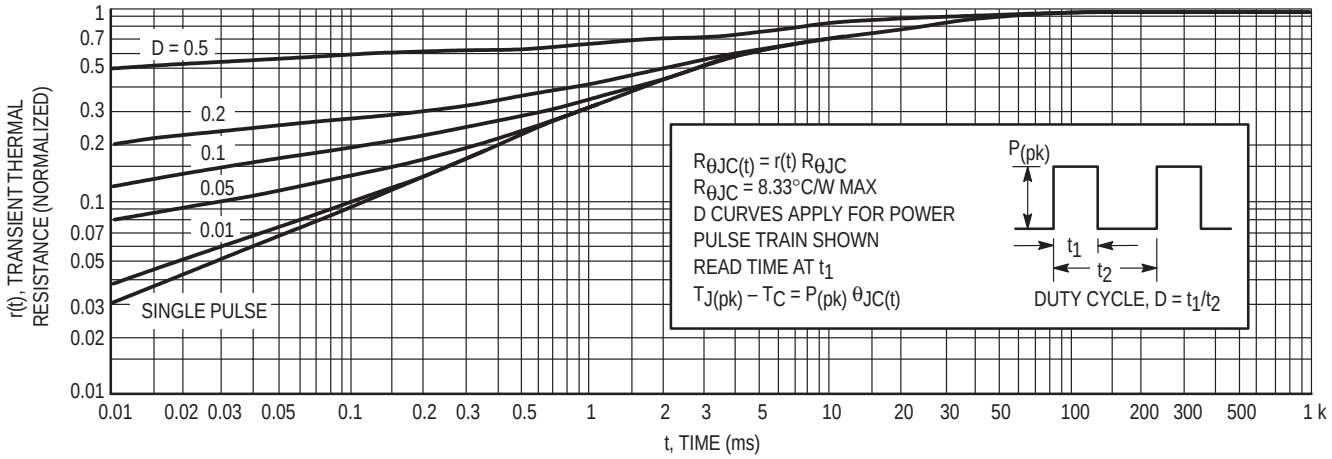


Figure 5. Thermal Response

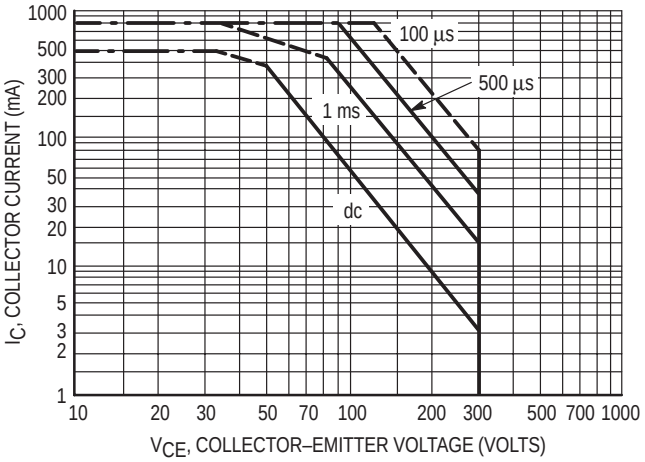


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

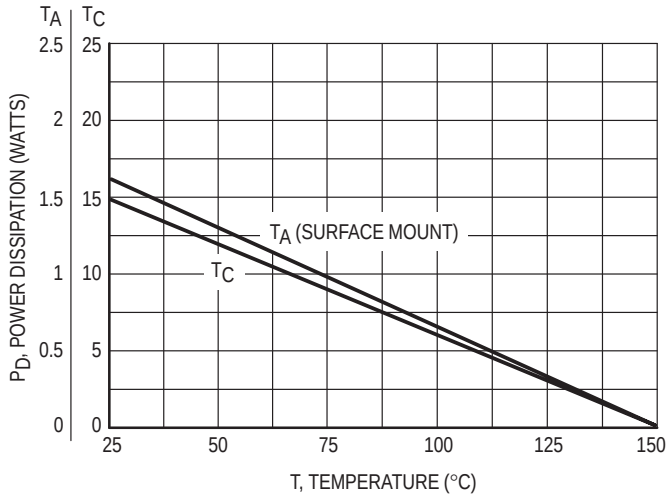


Figure 7. Power Derating

Complementary Power Transistors

DPAK For Surface Mount Applications

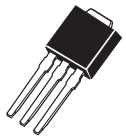
NPN
MJD2955
PNP
MJD3055

Designed for general purpose amplifier and low speed switching applications.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version Available in 16 mm Tape and Reel ("T4" Suffix)
- Electrically Similar to MJE2955 and MJE3055
- DC Current Gain Specified to 10 Amperes
- High Current Gain–Bandwidth Product — f_T = 2.0 MHz (Min) @ I_C = 500 mAdc

SILICON
POWER TRANSISTORS
10 AMPERES
60 VOLTS
20 WATTS

CASE 369A–13



CASE 369–07

MAXIMUM RATINGS

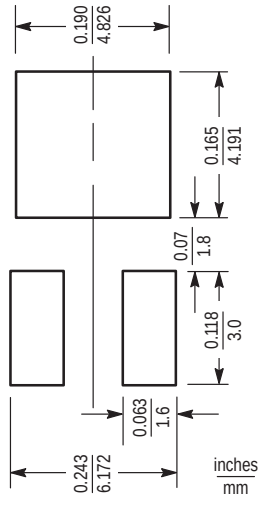
Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	60	Vdc
Collector–Base Voltage	V_{CB}	70	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	6	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D†	20 0.16	Watts W/°C
Total Power Dissipation (1) @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	°C/W

(1) These ratings are applicable when surface mounted on the minimum pad sizes recommended.
†Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	50	μAdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	— —	0.02 2	mAdc
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	— —	0.02 2	mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	0.5	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 4 Adc, V_{CE} = 4 Vdc) (I_C = 10 Adc, V_{CE} = 4 Vdc)	h_{FE}	20 5	100 —	—
Collector–Emitter Saturation Voltage (1) (I_C = 4 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	— —	1.1 8	Vdc
Base–Emitter On Voltage (1) (I_C = 4 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 500 kHz)	f_T	2	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

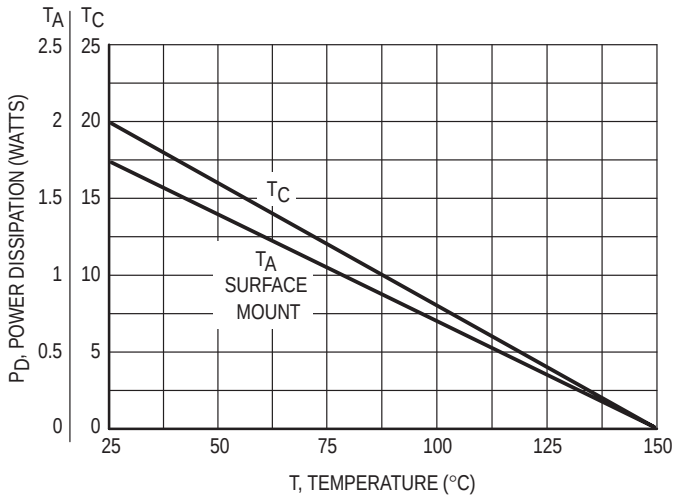


Figure 1. Power Derating

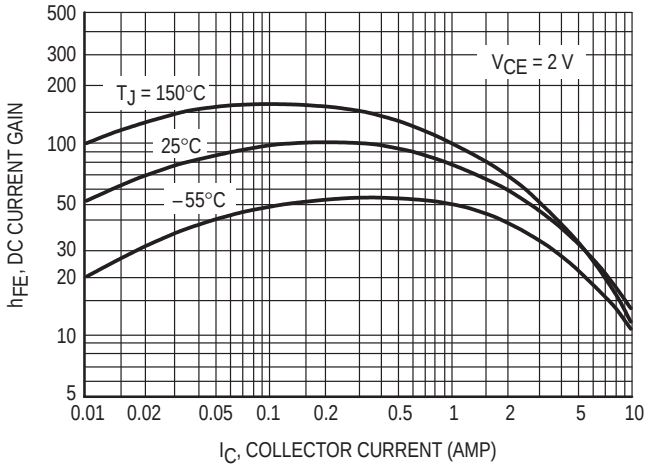


Figure 2. DC Current Gain

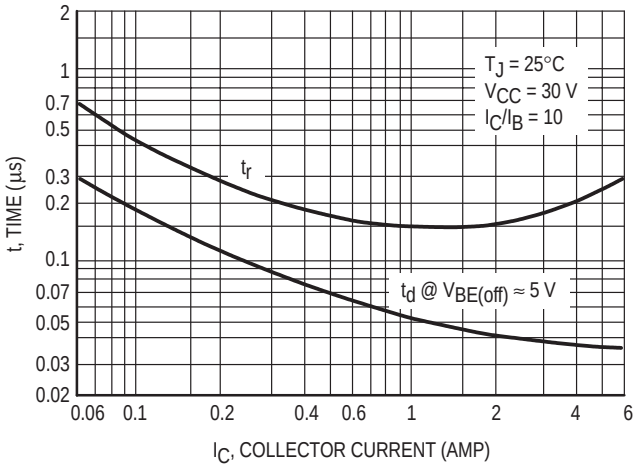


Figure 3. Turn–On Time

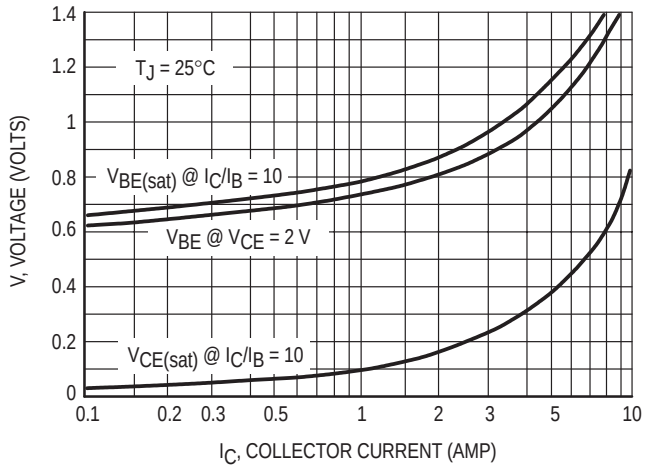


Figure 4. “On” Voltages, MJD3055

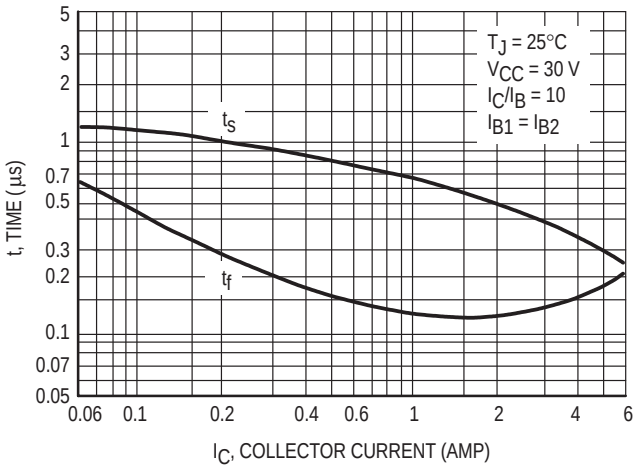


Figure 5. Turn–Off Time

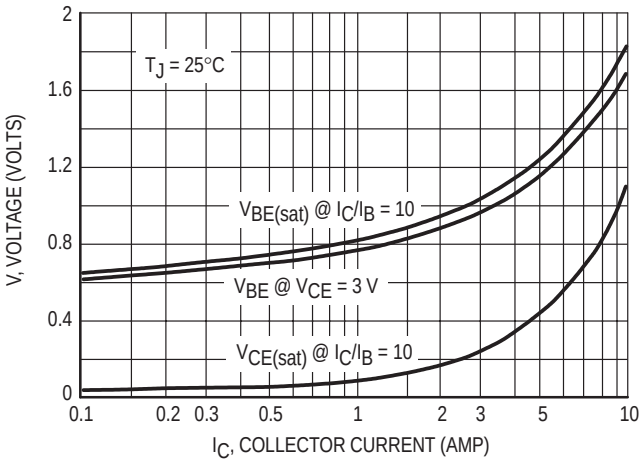


Figure 6. "On" Voltages, MJD2955

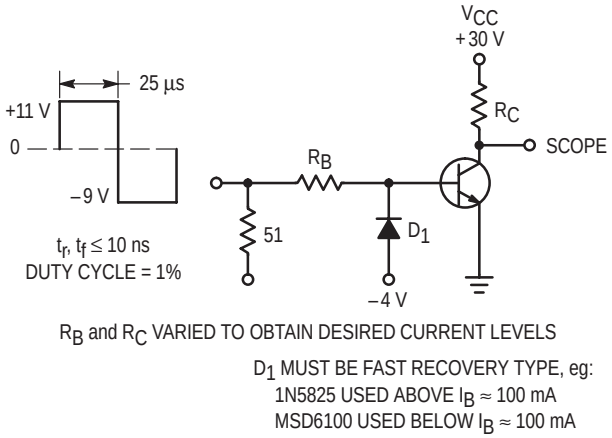


Figure 7. Switching Time Test Ciruit

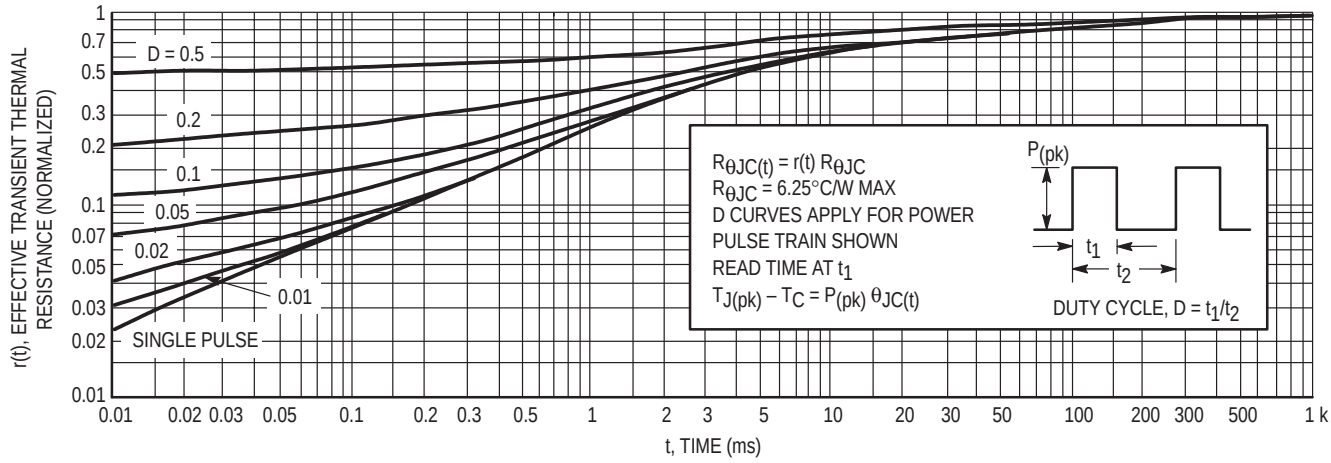


Figure 8. Thermal Response

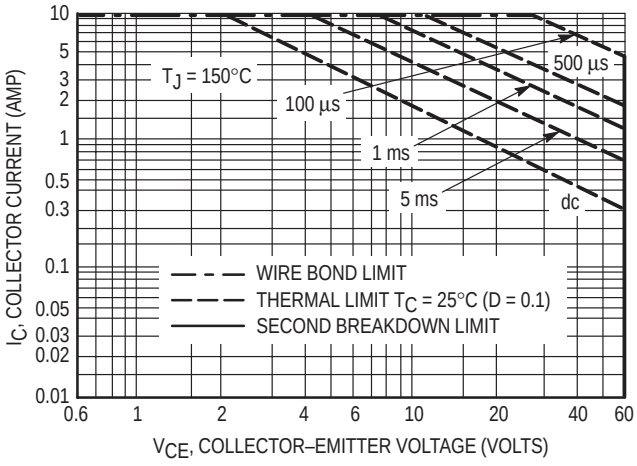


Figure 9. Maximum Forward Bias Safe Operating Area

FORWARD BIAS SAFE OPERATING AREA INFORMATION

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Complementary Darlington Power Transistors

DPAK For Surface Mount Applications

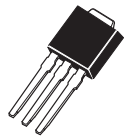
NPN
MJD6036
PNP
MJD6039

SILICON
POWER TRANSISTORS
4 AMPERES
80 VOLTS
20 WATTS

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, convertors, and power amplifiers.

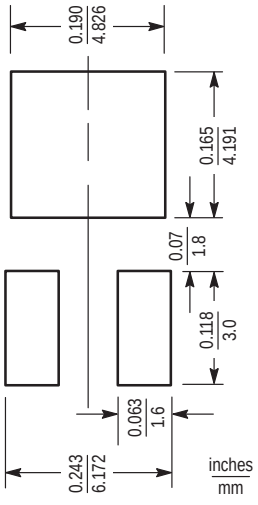
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Available on 16 mm Tape and Reel for Automatic Handling ("T4" Suffix)
- Surface Mount Replacements for 2N6034–2N6039 Series
- Monolithic Construction With Built–in Base–Emitter Shunt Resistors
- High DC Current Gain — h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Complementary Pairs Simplifies Designs

CASE 369A–13



CASE 369–07

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	MJD6036 MJD6039	Unit
Collector–Emitter Voltage	V_{CEO}	80	Vdc
Collector–Base Voltage	V_{CB}	80	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	4 8	Adc
Base Current	I_B	100	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation (1) @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	71.4	°C/W

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	80	—	Vdc
Collector–Cutoff Current (V_{CE} = 40 Vdc, I_B = 0)	I_{CEO}	—	10	µAdc

(1) These ratings are applicable when surface mounted on the minimum pad sizes recommended.
* Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%. (continued)

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS (1)				
DC Current Gain	h_{FE}			—
(I_C = 1 Adc, V_{CE} = 4 Vdc)		1000	—	
(I_C = 2 Adc, V_{CE} = 4 Vdc)		500	—	
Collector–Emitter Saturation Voltage (I_C = 2 Adc, I_B = 8 mAdc)	$V_{CE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (I_C = 2 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Small–Signal Current Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1 kHz)	h_{fe}	25	—	—
Output Capacitance	C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJD6036		—	200	
MJD6039		—	100	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

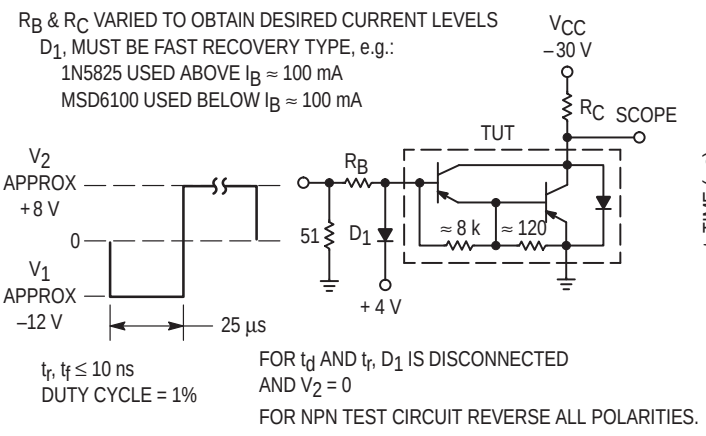


Figure 1. Switching Times Test Circuit

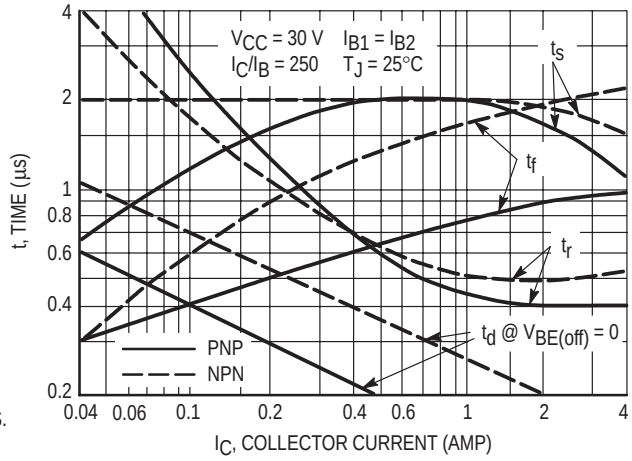


Figure 2. Switching Times

TYPICAL ELECTRICAL CHARACTERISTICS

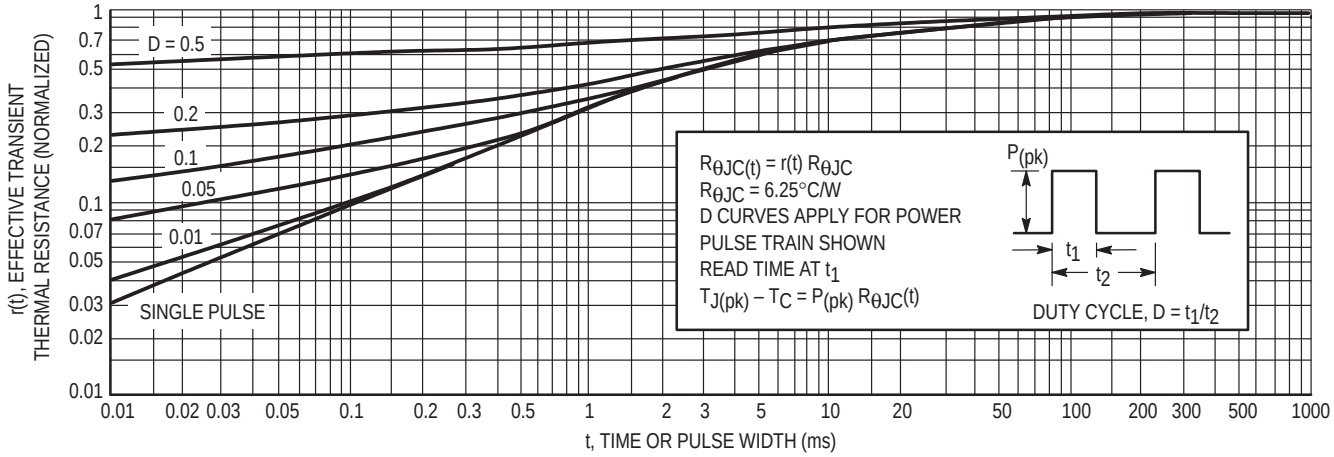


Figure 3. Thermal Response

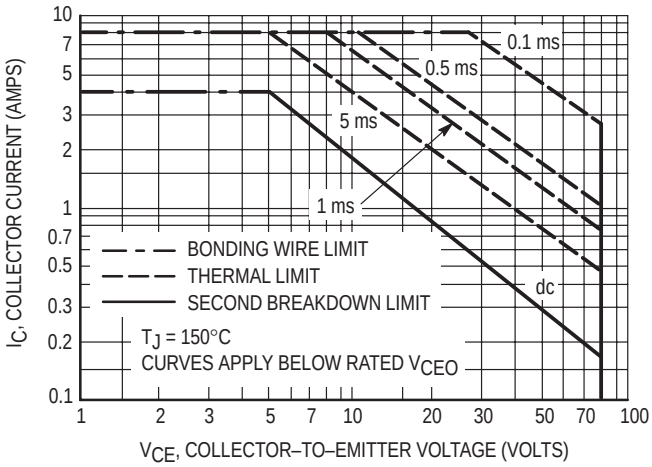


Figure 4. Maximum Rated Forward Biased Safe Operating Area

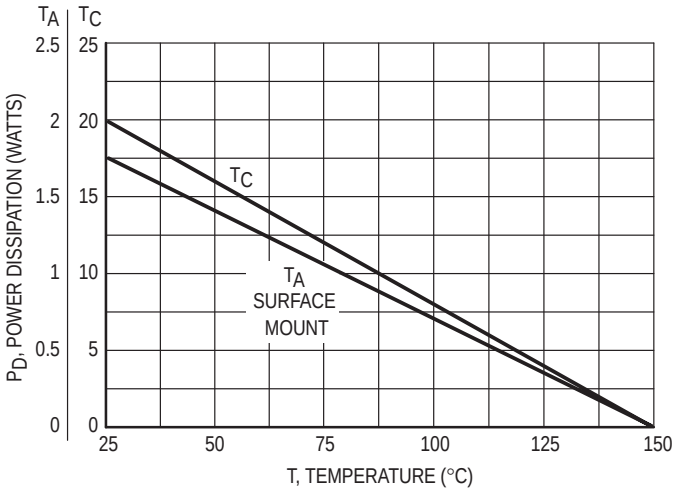


Figure 5. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 6 and 7 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

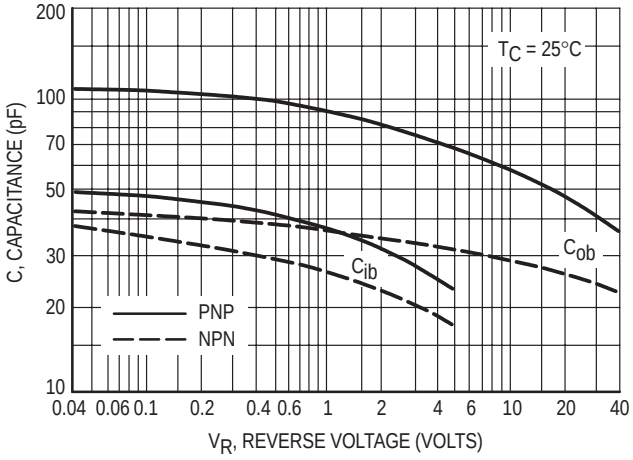
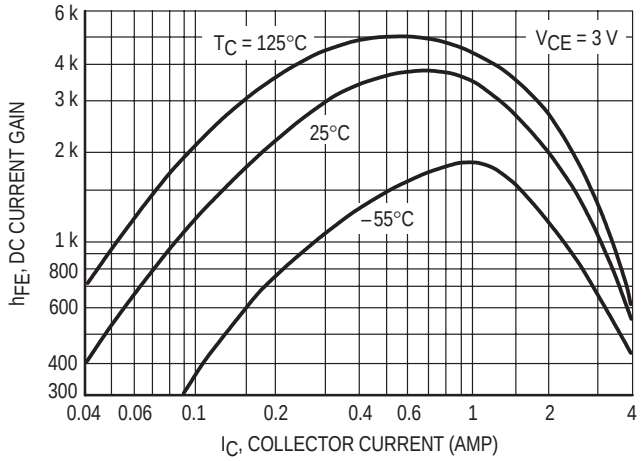


Figure 6. Capacitance

TYPICAL ELECTRICAL CHARACTERISTICS

PNP MJD6036



NPN MJD6039

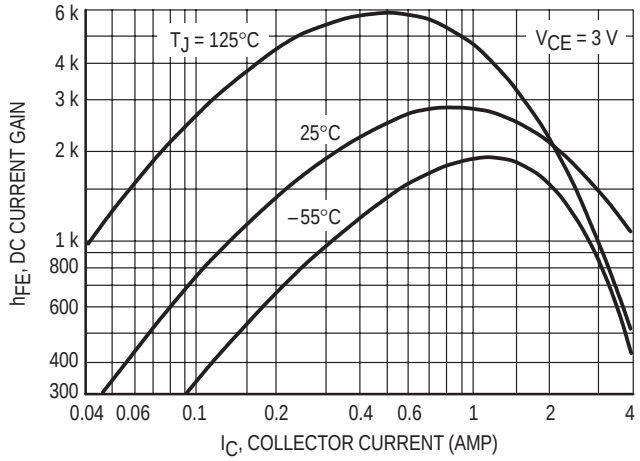
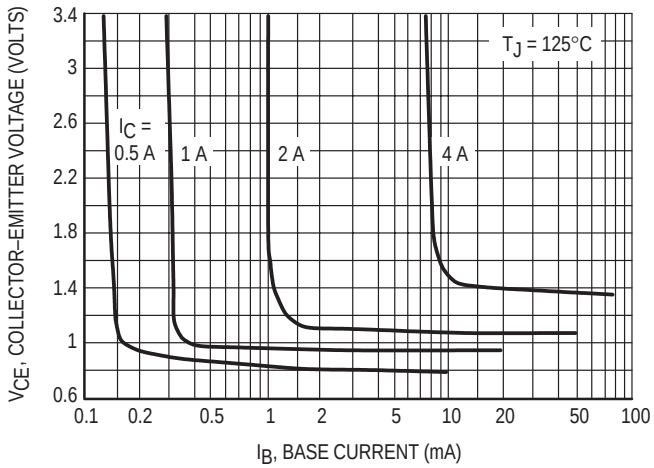


Figure 7. DC Current Gain



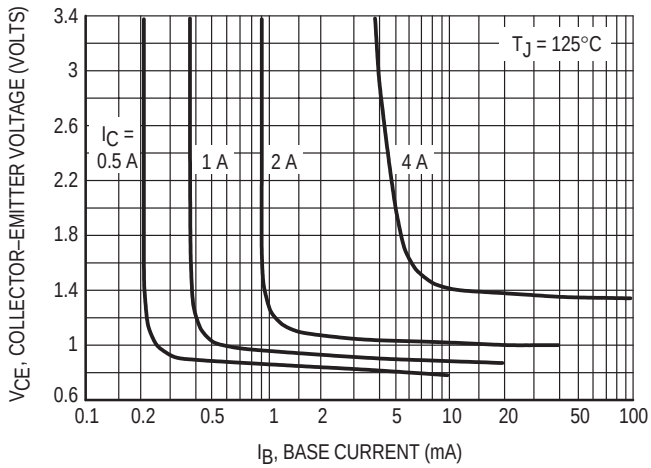
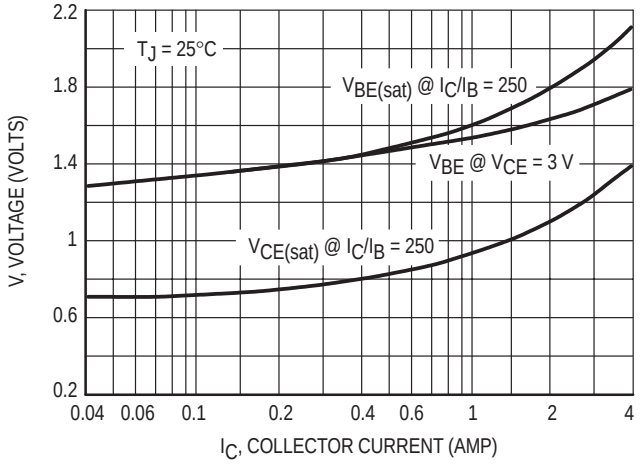


Figure 8. Collector Saturation Region



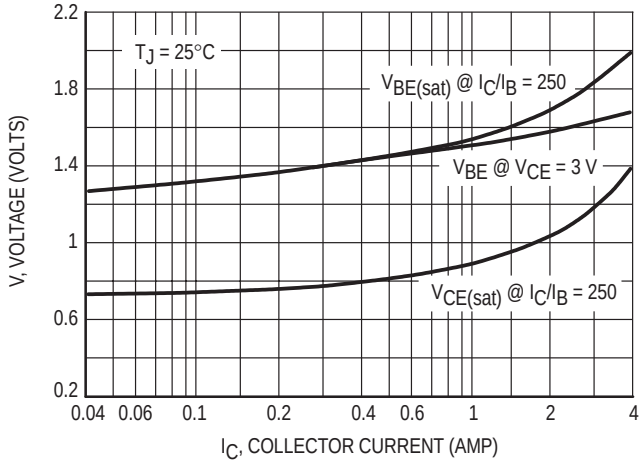


Figure 9. “On” Voltages

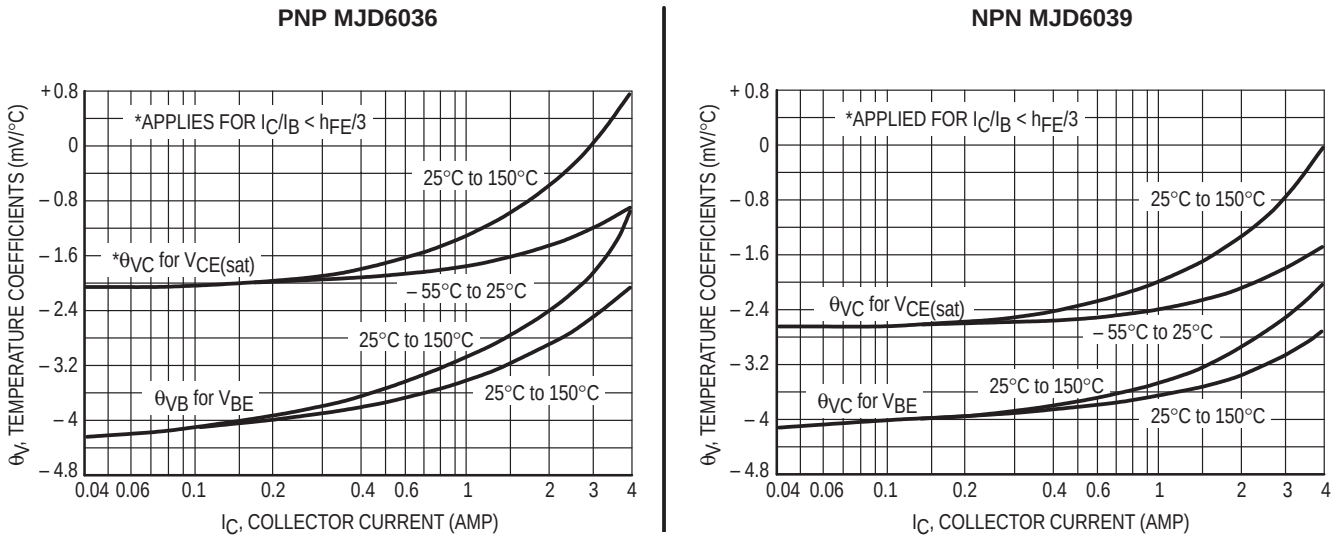


Figure 10. Temperature Coefficients

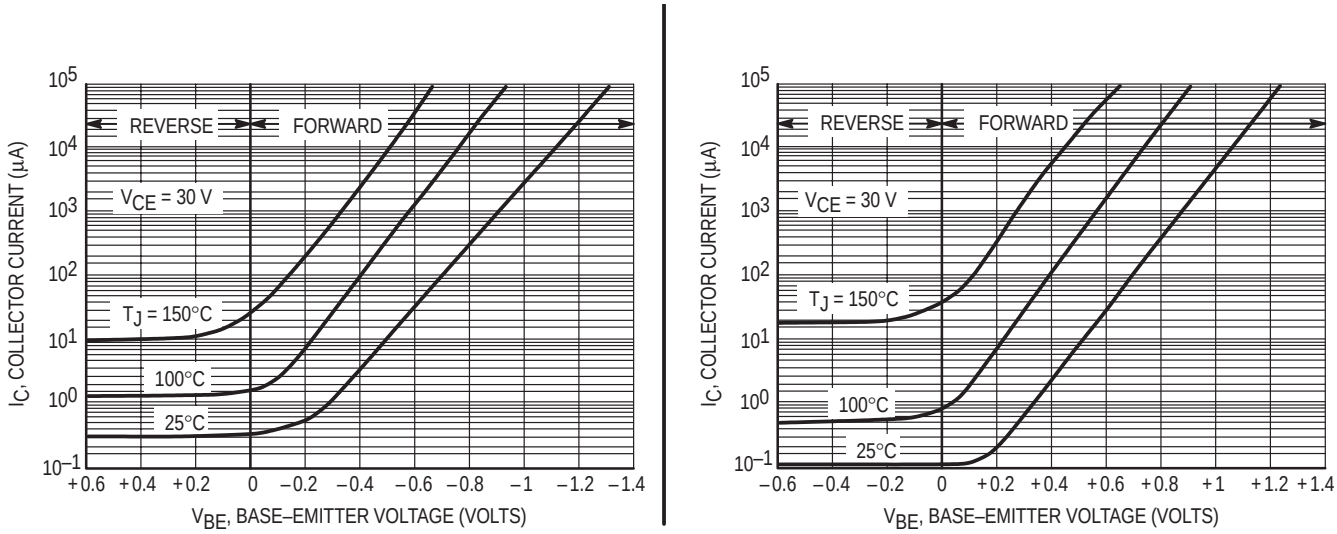


Figure 11. Collector Cut–Off Region

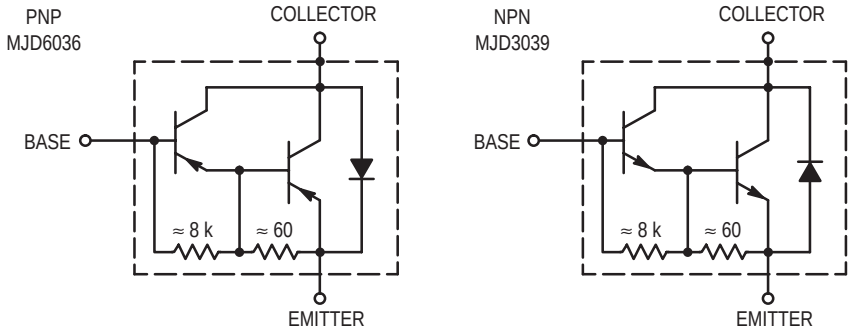


Figure 12. Darlington Schematic

Complementary Plastic Silicon Power Transistors

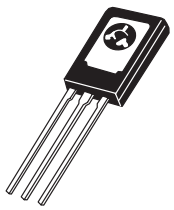
. . . designed for low power audio amplifier and low current, high speed switching applications.

- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc — MJE171, MJE181
  = 80 Vdc — MJE172, MJE182
- DC Current Gain —
  h_{FE} = 30 (Min) @ I_C = 0.5 Adc
  = 12 (Min) @ I_C = 1.5 Adc
- Current–Gain — Bandwidth Product —
  f_T = 50 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakages —
  I_{CBO} = 100 nA (Max) @ Rated V_{CB}

PNP
MJE171*
MJE172*
NPN
MJE181*
MJE182*

***Motorola Preferred Device**

3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60–80 VOLTS
12.5 WATTS



CASE 77–08
TO–225AA

MAXIMUM RATINGS

Rating	Symbol	MJE171 MJE181	MJE172 MJE182	Unit
Collector–Base Voltage	V_{CB}	80	100	Vdc
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak	I_C	3.0 6.0		Adc
Base Current	I_B	1.0		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012		Watts W/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

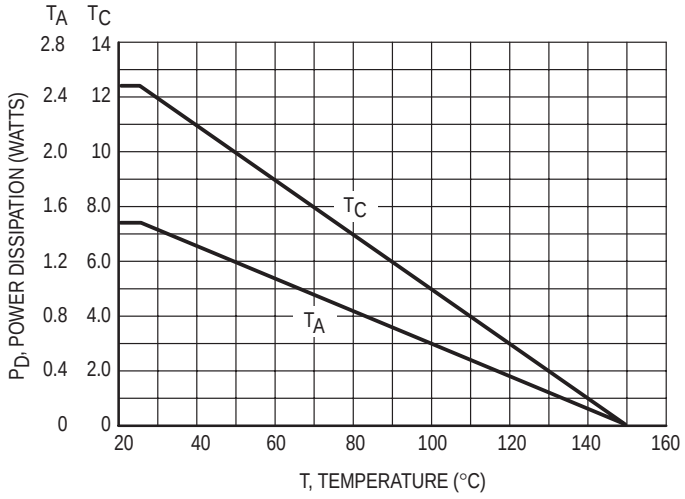


Figure 1. Power Derating

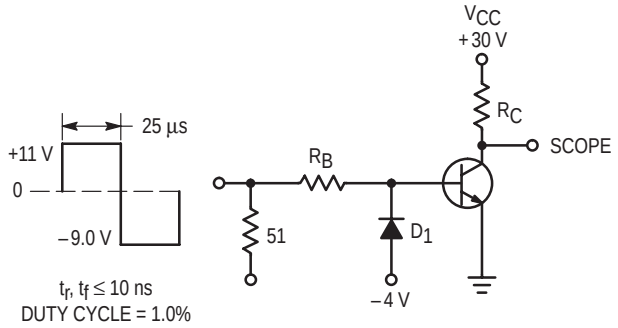
Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0)	MJE171, MJE181	$V_{CEO(sus)}$	60	—	Vdc
	MJE172, MJE182		80	—	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 80 Vdc, I_E = 0)	MJE171, MJE181		—	0.1	
(V_{CB} = 100 Vdc, I_E = 0)	MJE172, MJE182		—	0.1	
(V_{CB} = 80 Vdc, I_E = 0, T_C = 150°C)	MJE171, MJE181		—	0.1	mAdc
(V_{CB} = 100 Vdc, I_E = 0, T_C = 150°C)	MJE172, MJE182		—	0.1	
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			—
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)			50	250	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)			30	—	
(I_C = 1.5 Adc, V_{CE} = 1.0 Vdc)			12	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)			—	0.3	
(I_C = 1.5 Adc, I_B = 150 mAdc)			—	0.9	
(I_C = 3.0 Adc, I_B = 600 mAdc)			—	1.7	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 150 mAdc)			—	1.5	
(I_C = 3.0 Adc, I_B = 600 mAdc)			—	2.0	
Base–Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	—	1.2	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (1) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	50	—	MHz
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJE171/MJE172		—	60	
	MJE181/MJE182		—	40	

(1) $f_T = |h_{fe}| \bullet f_{test}$.



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA
FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES.

Figure 2. Switching Time Test Circuit

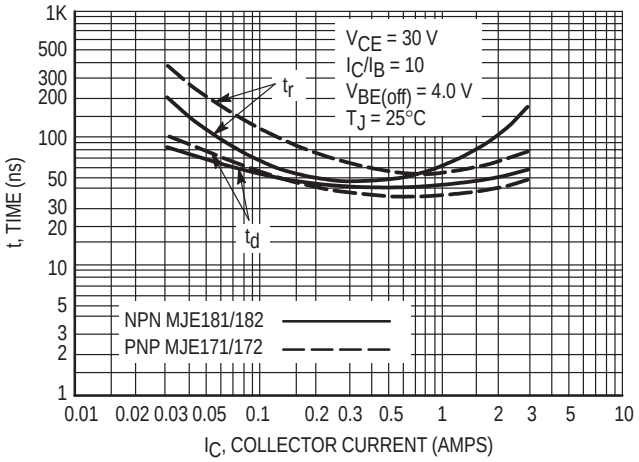


Figure 3. Turn–On Time

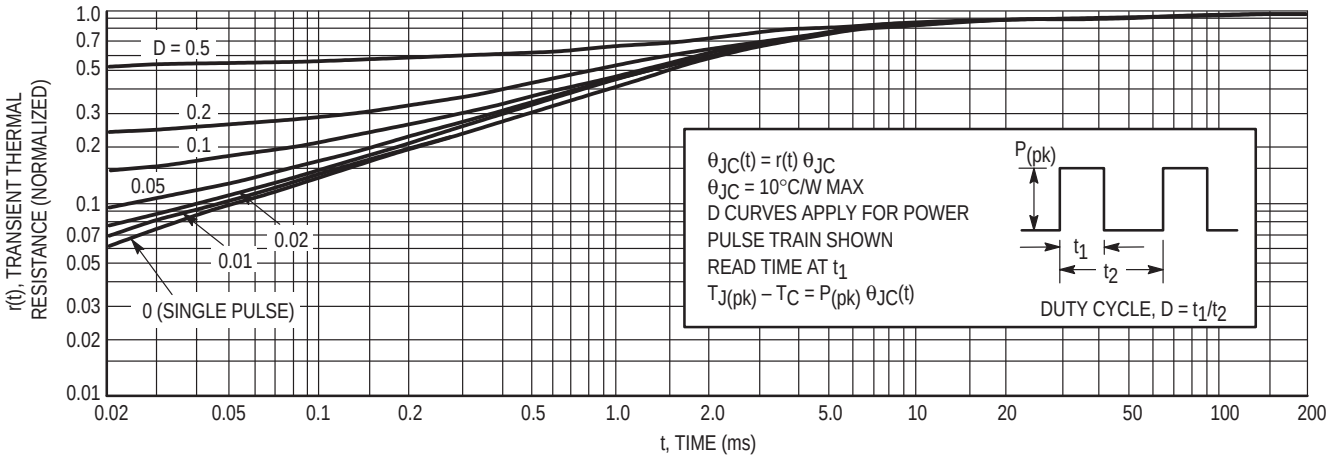


Figure 4. Thermal Response

ACTIVE–REGION SAFE OPERATING AREA

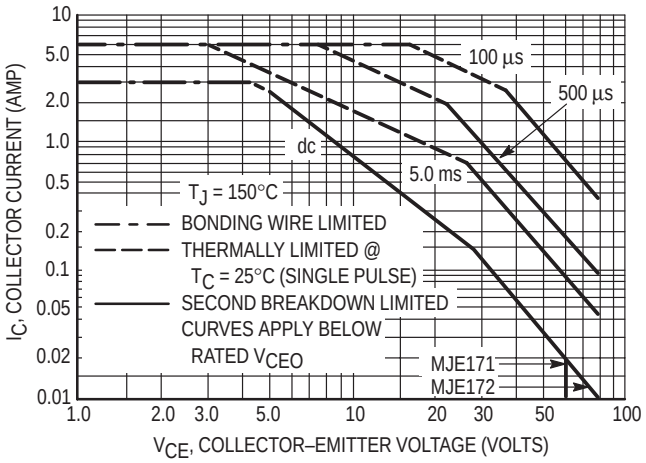


Figure 5. MJE171, MJE172

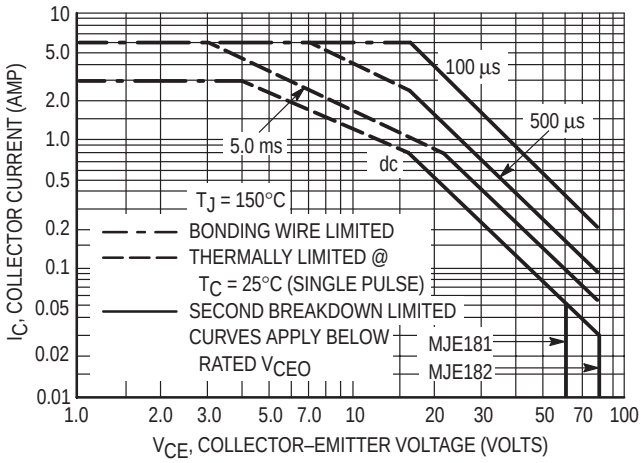


Figure 6. MJE181, MJE182

There are two limitations on the power handling ability of a transistor — average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperature, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

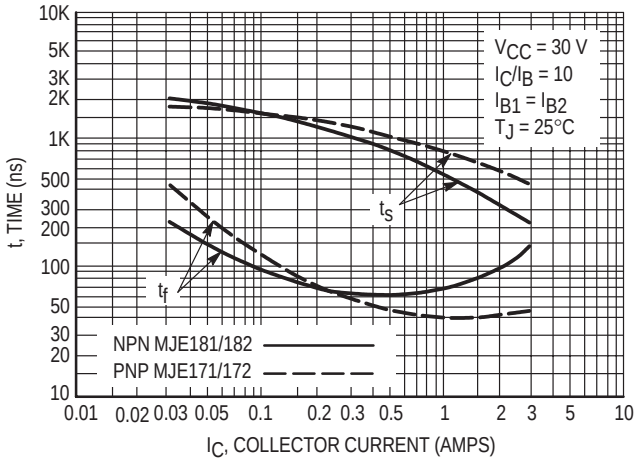


Figure 7. Turn–Off Time

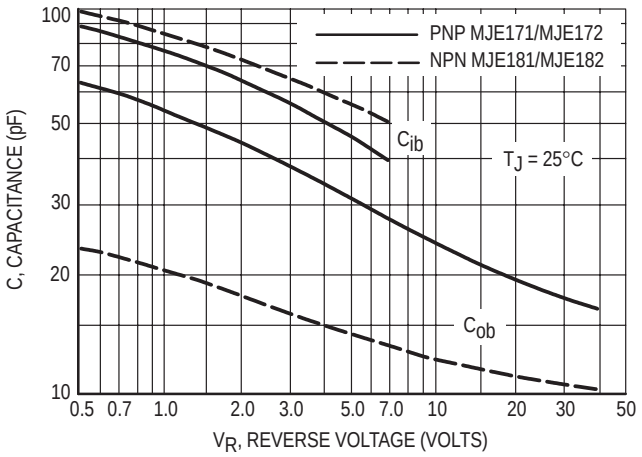


Figure 8. Capacitance

Complementary Silicon Power Plastic Transistors

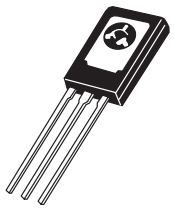
. . . designed for low voltage, low–power, high–gain audio amplifier applications.

- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 25 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain — h_{FE} = 70 (Min) @ I_C = 500 mAdc
  = 45 (Min) @ I_C = 2.0 Adc
  = 10 (Min) @ I_C = 5.0 Adc
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.75 Vdc (Max) @ I_C = 2.0 Adc
- High Current–Gain — Bandwidth Product —
  f_T = 65 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakage —
  I_{CBO} = 100 nAdc @ Rated V_{CB}

NPN
MJE200*
PNP
MJE210*

*Motorola Preferred Device

5 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
25 VOLTS
15 WATTS



CASE 77–08
TO–225AA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CB}	40	Vdc
Collector–Emitter Voltage	V_{CEO}	25	Vdc
Emitter–Base Voltage	V_{EB}	8.0	Vdc
Collector Current — Continuous Peak	I_C	5.0 10	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.34	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

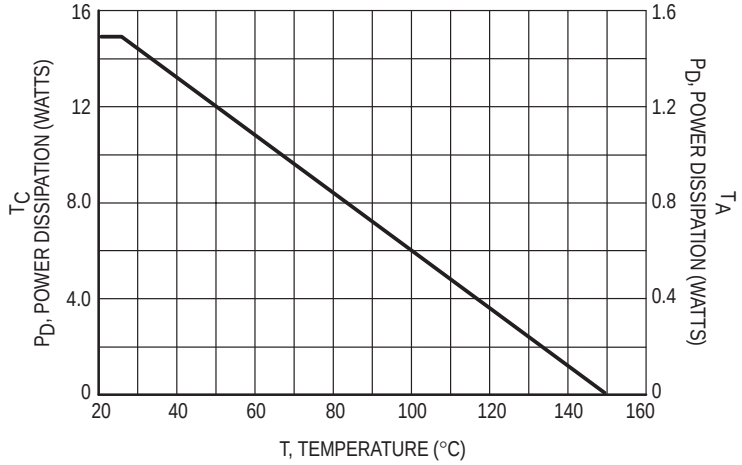


Figure 1. Power Derating

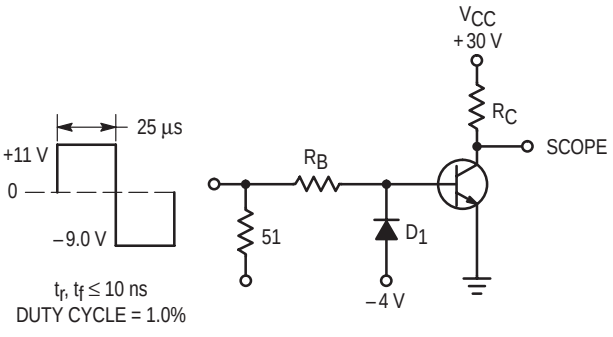
Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)		$V_{CEO(sus)}$	25	—	Vdc
Collector Cutoff Current (V_{CB} = 40 Vdc, I_E = 0) (V_{CB} = 40 Vdc, I_E = 0, T_J = 125°C)		I_{CBO}	 — —	 100 100	 nAdc µAdc
Emitter Cutoff Current (V_{BE} = 8.0 Vdc, I_C = 0)		I_{EBO}	 —	 100	nAdc
ON CHARACTERISTICS					
DC Current Gain (1) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	 70 45 10	 — 180 —	—
Collector–Emitter Saturation Voltage (1) (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 2.0 Adc, I_B = 200 mAdc) (I_C = 5.0 Adc, I_B = 1.0 Adc)		$V_{CE(sat)}$	 — — —	 0.3 0.75 1.8	Vdc
Base–Emitter Saturation Voltage (1) (I_C = 5.0 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (1) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)		$V_{BE(on)}$	—	1.6	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	65	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	 MJE200 MJE210	C_{ob}	 — —	 80 120	pF

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle ≈ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

Figure 2. Switching Time Test Circuit

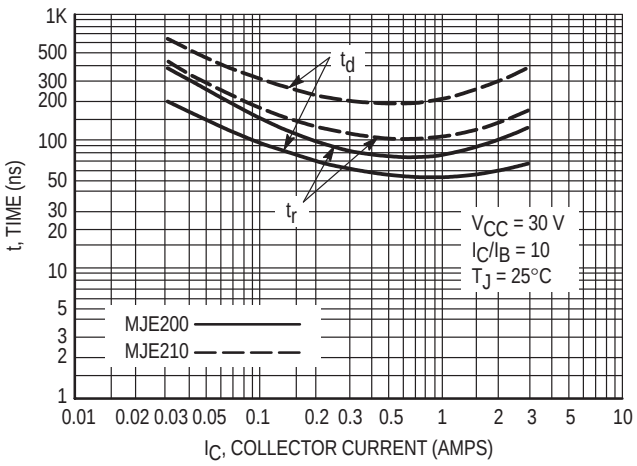


Figure 3. Turn–On Time

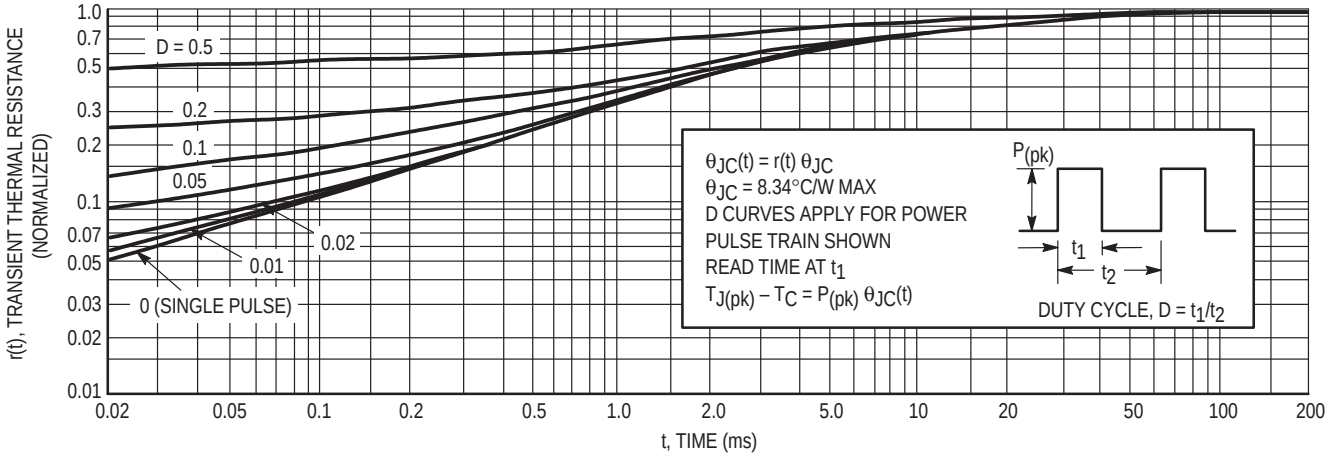


Figure 4. Thermal Response

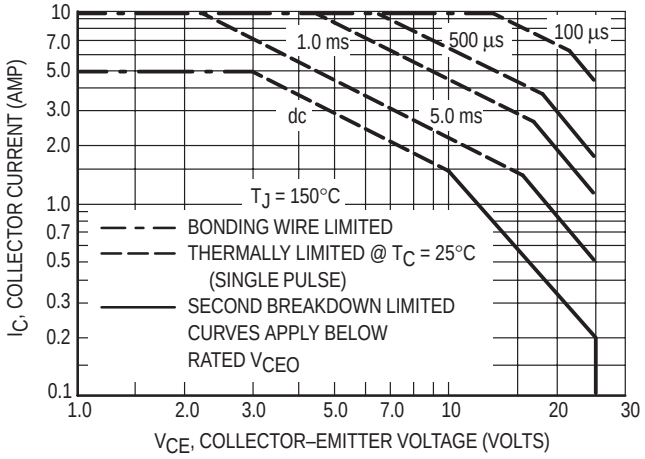


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

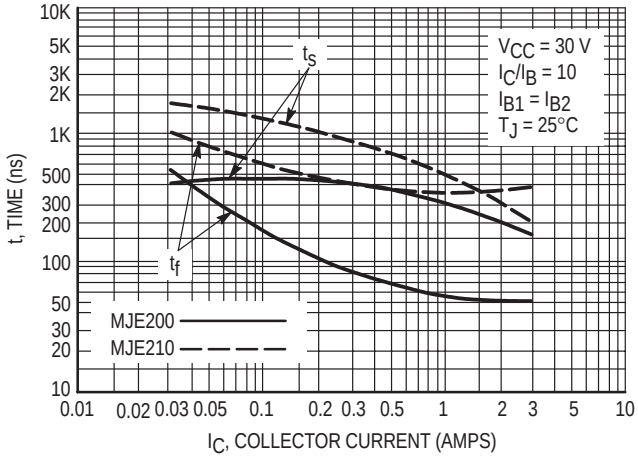


Figure 6. Turn–Off Time

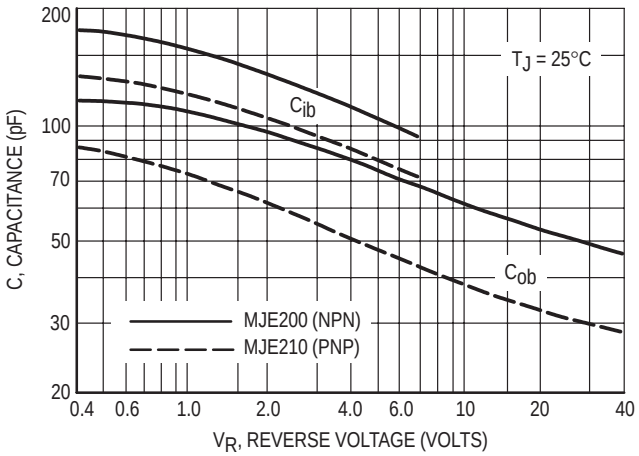
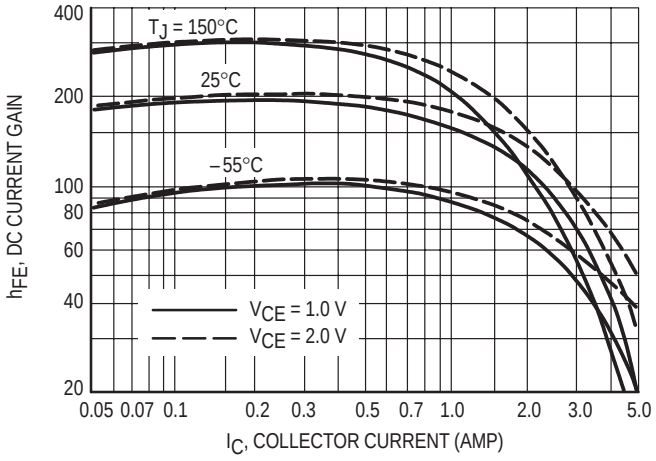


Figure 7. Capacitance

NPN
MJE200



PNP
MJE210

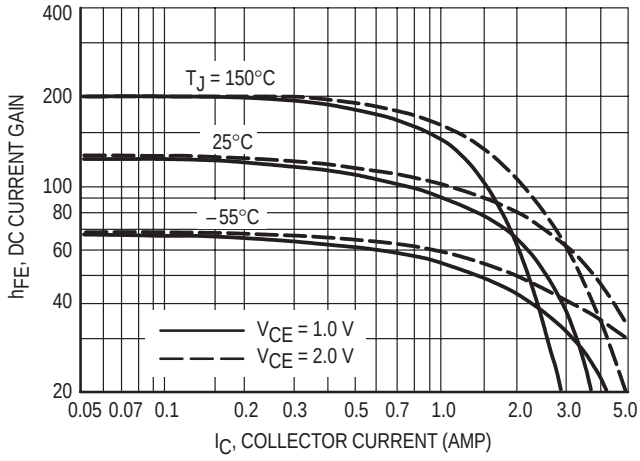
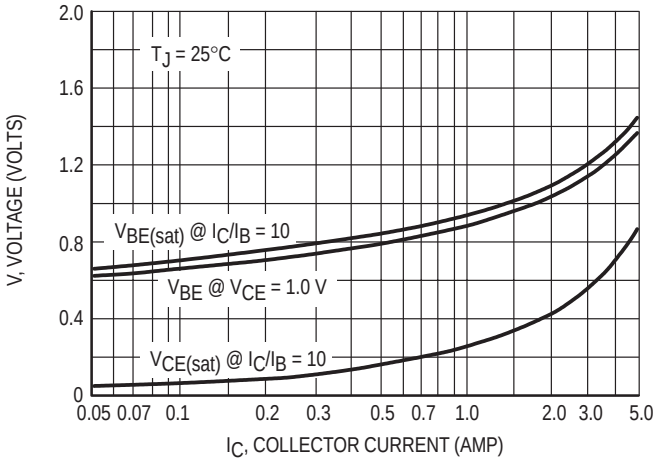


Figure 8. DC Current Gain



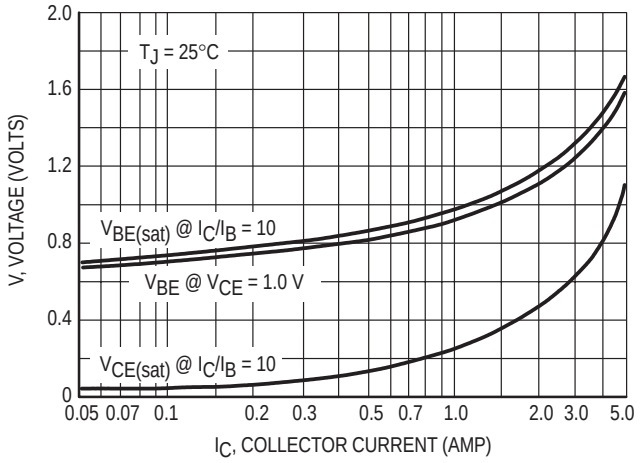
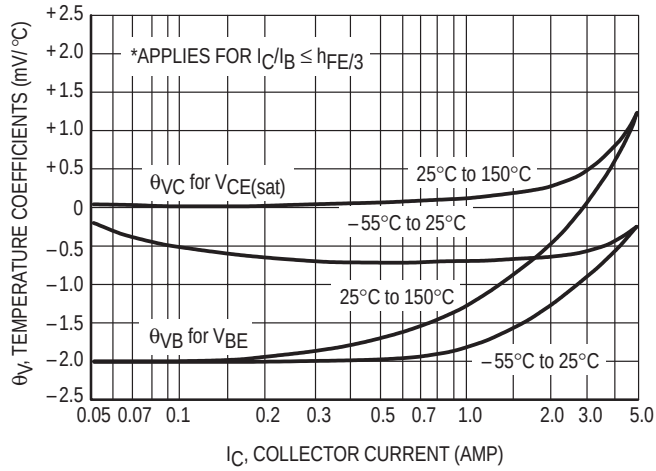


Figure 9. “On” Voltage



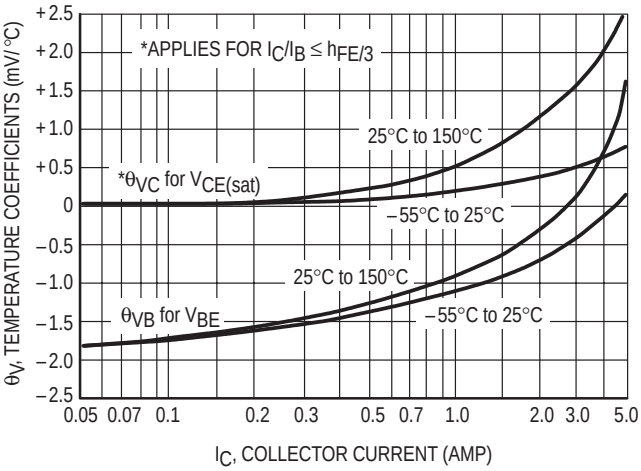


Figure 10. Temperature Coefficients

Complementary Silicon Power Plastic Transistors

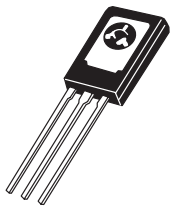
. . . designed for low power audio amplifier and low–current, high–speed switching applications.

- High Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 100 Vdc (Min) — MJE243, MJE253
- High DC Current Gain @ I_C = 200 mAdc
  h_{FE} = 40–200
  = 40–120 — MJE243, MJE253
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
- High Current Gain Bandwidth Product —
  f_T = 40 MHz (Min) @ I_C = 100 mAdc
- Annular Construction for Low Leakages
  I_{CBO} = 100 nAdc (Max) @ Rated V_{CB}

NPN
MJE243*
PNP
MJE253*

*Motorola Preferred Device

4 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
100 VOLTS
15 WATTS



CASE 77–08
TO–225AA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous Peak	I_C	4.0 8.0	Adc
Base Current	I_B	10	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/ac
Total Power Dissipation @ T_A = 25°C Derate @ 25°C	P_D	1.5 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.34	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	83.4	°C/W

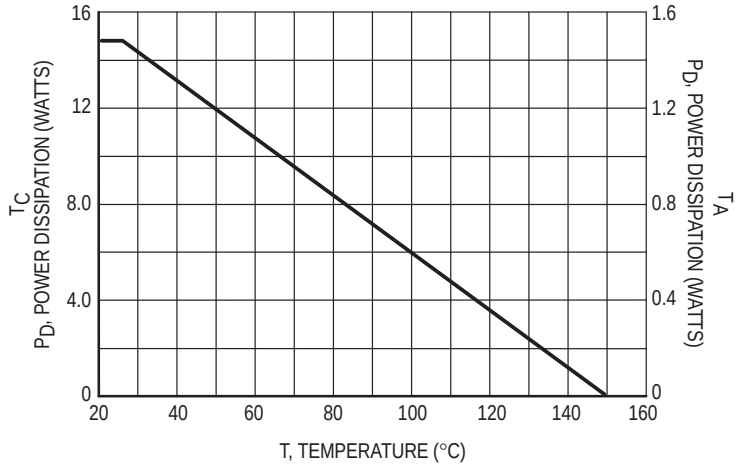


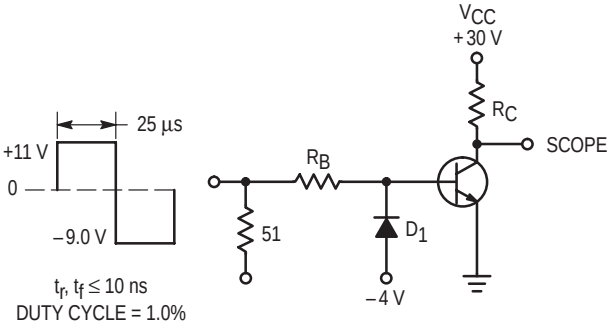
Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0) (V_{CE} = 100 Vdc, I_E = 0, T_C = 125°C)	I_{CBO}	— —	0.1 0.1	μAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 200 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	40 15	180 —	—
Collector–Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc) (I_C = 1.0 Adc, I_B = 100 mAdc)	$V_{CE(sat)}$	— —	0.3 0.6	Vdc
Base–Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 200 mAdc)	$V_{BE(sat)}$	—	1.8	Vdc
Base–Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 1.0 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	40	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	50	pF



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA
FOR PNP TEST CIRCUIT, REVERSE ALL POLARITIES

Figure 2. Switching Time Test Circuit

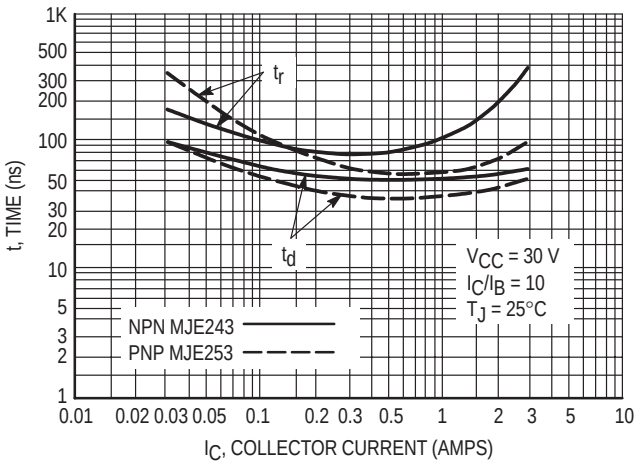


Figure 3. Turn–On Time

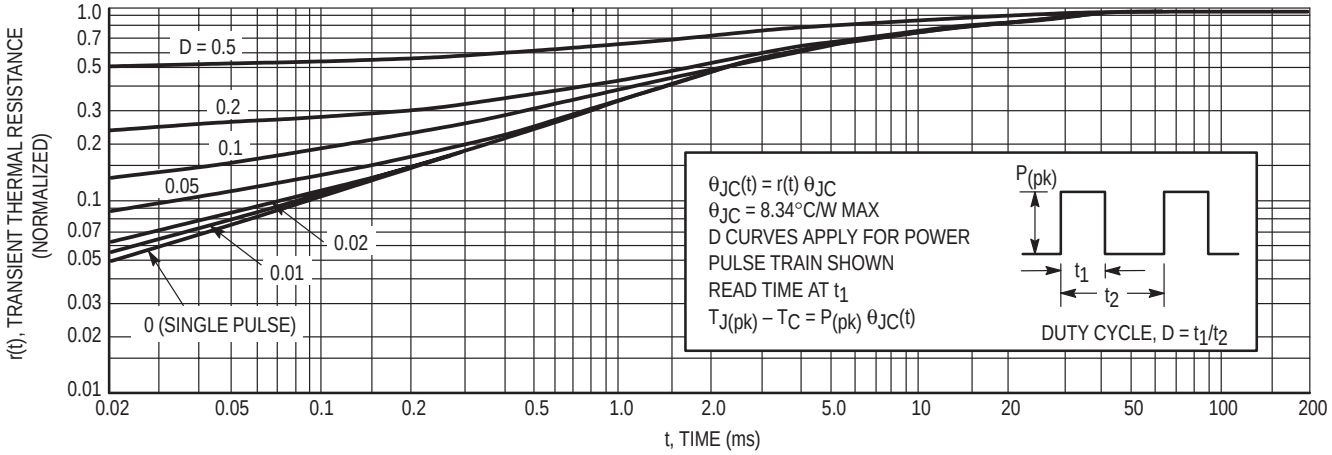


Figure 4. Thermal Response

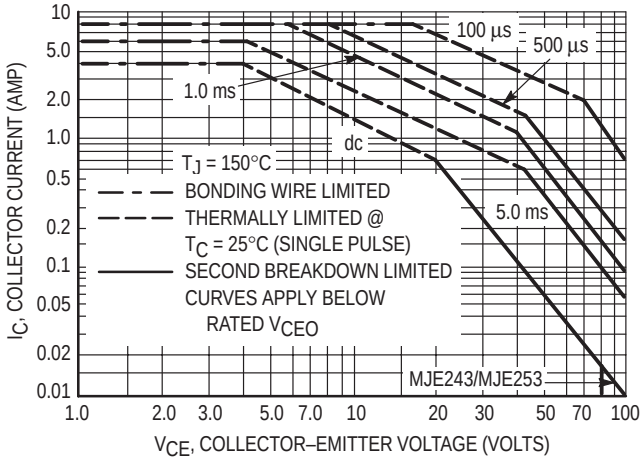


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

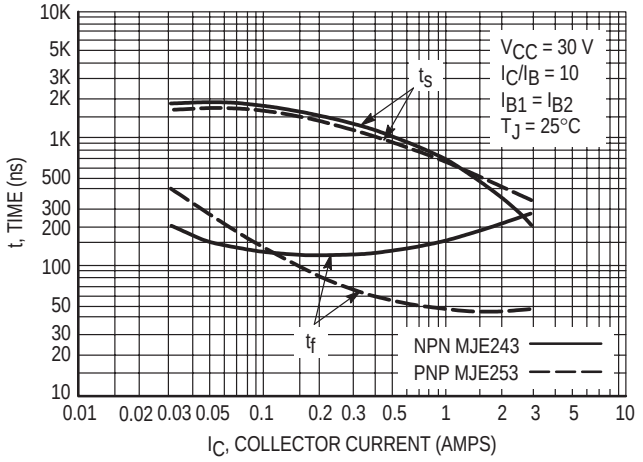


Figure 6. Turn–Off Time

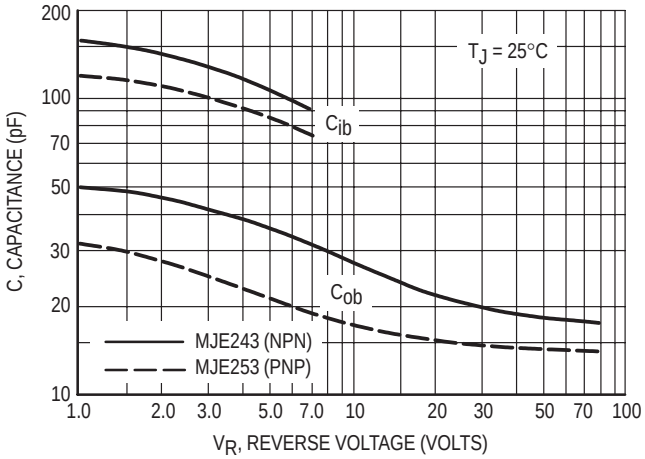
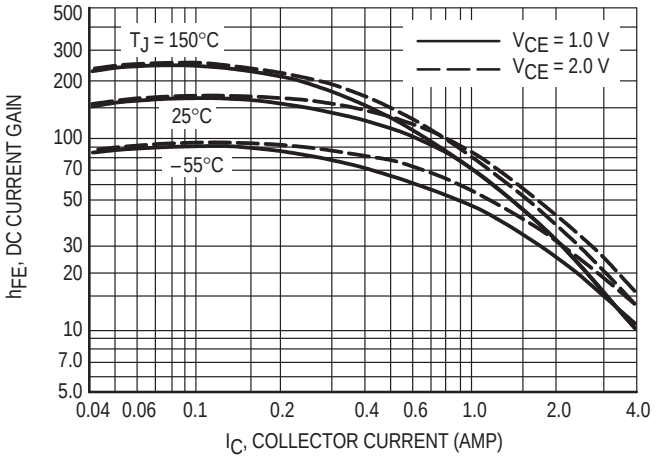


Figure 7. Capacitance

NPN
MJE243



PNP
MJE253

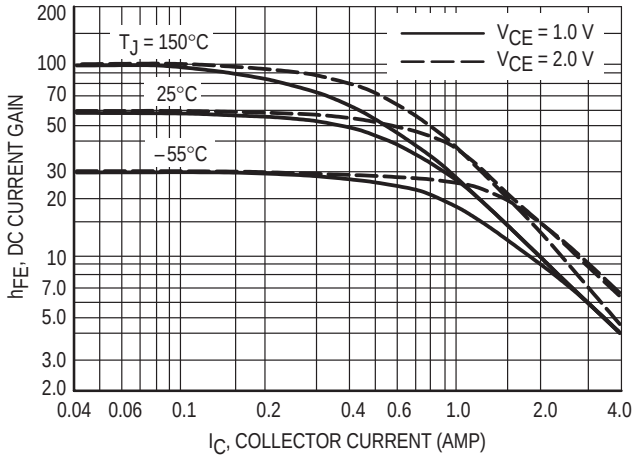
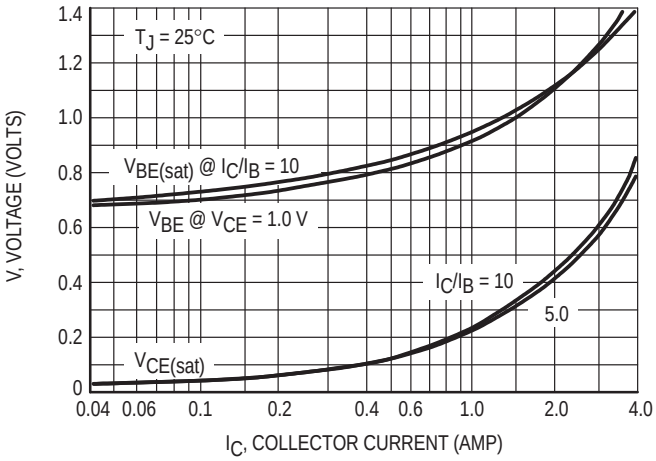


Figure 8. DC Current Gain



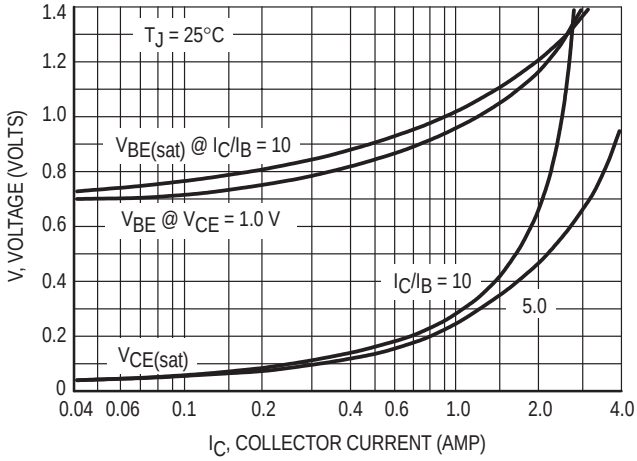
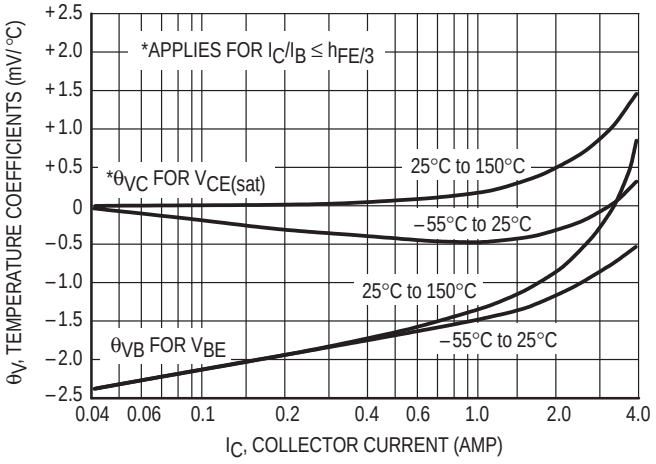


Figure 9. “On” Voltages



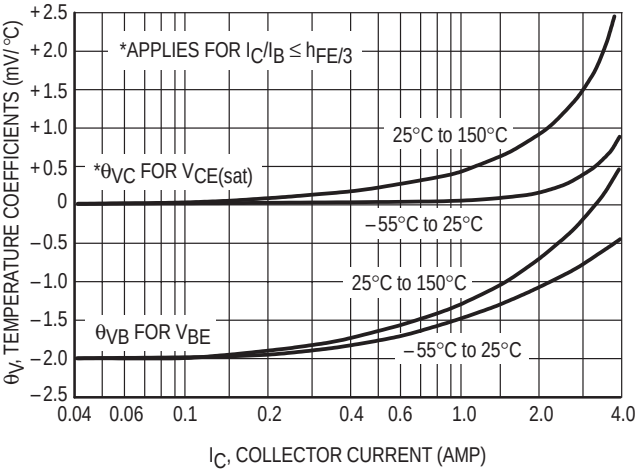


Figure 10. Temperature Coefficients

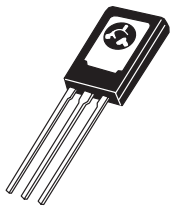
Complementary Silicon Power Transistors

. . . designed specifically for use with the MC3419 Solid–State Subscriber Loop Interface Circuit (SLIC).

- High Safe Operating Area
  $I_{S/B}$ @ 40 V, 1.0 s = 0.375 A — TO–126
- Collector–Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 100 Vdc (Min)
- High DC Current Gain
  h_{FE} @ 120 mA, 10 V = 1500 (Min)

NPN
MJE270
PNP
MJE271

2.0 AMPERE
COMPLEMENTARY
POWER DARLINGTON
TRANSISTORS
100 VOLTS
15 WATTS



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C	2.0 4.0	Adc
Base Current	I_B	0.1	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	83.3	°C/W

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 100 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	0.3	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	0.1	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1.0 s, non–repetitive)	$I_{S/b}$	375	—	Adc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 20 mAdc, V_{CE} = 3.0 Vdc) (I_C = 120 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 500 1500	 — —	—
Collector–Emitter Saturation Voltage (I_C = 20 mAdc, I_B = 0.2 mAdc) (I_C = 120 mAdc, I_B = 1.2 mAdc)	$V_{CE(sat)}$	 — —	 2.0 3.0	Vdc
Base–Emitter On Voltage (I_C = 120 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I_C = 0.05 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	6.0	—	MHz

NOTES:
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

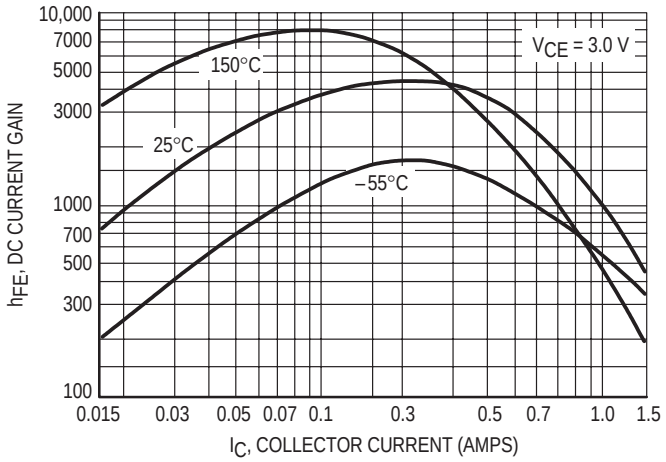


Figure 1. DC Current Gain

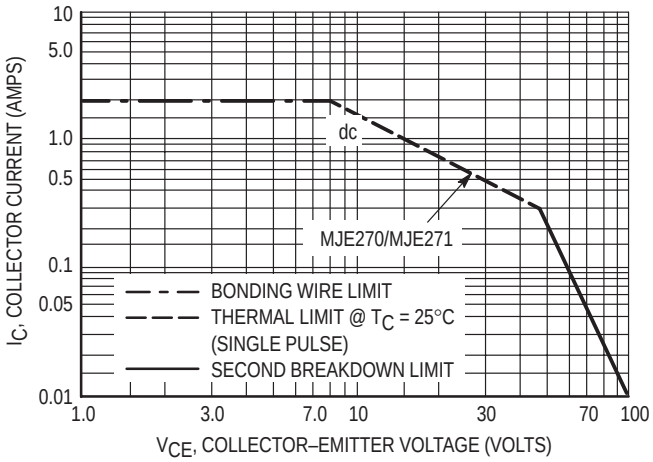


Figure 2. Safe Operating Area

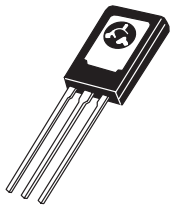
MJE340

Plastic Medium Power NPN Silicon Transistor

0.5 AMPERE
POWER TRANSISTOR
NPN SILICON
300 VOLTS
20 WATTS

. . . useful for high–voltage general purpose applications.

- Suitable for Transformerless, Line–Operated Equipment
- Thermopad Construction Provides High Power Dissipation Rating for High Reliability



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	300	Vdc
Emitter–Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	—	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	—

REV 7

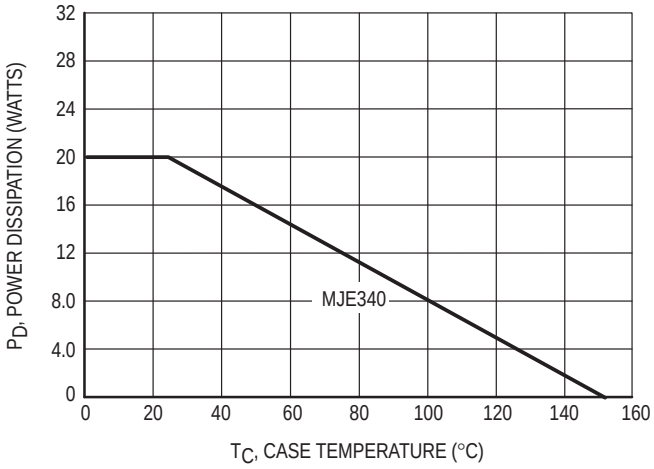


Figure 1. Power Temperature Derating

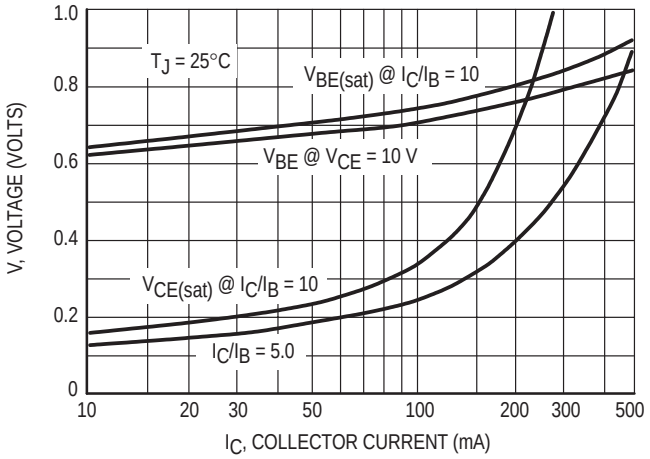


Figure 2. "On" Voltages

ACTIVE–REGION SAFE OPERATING AREA

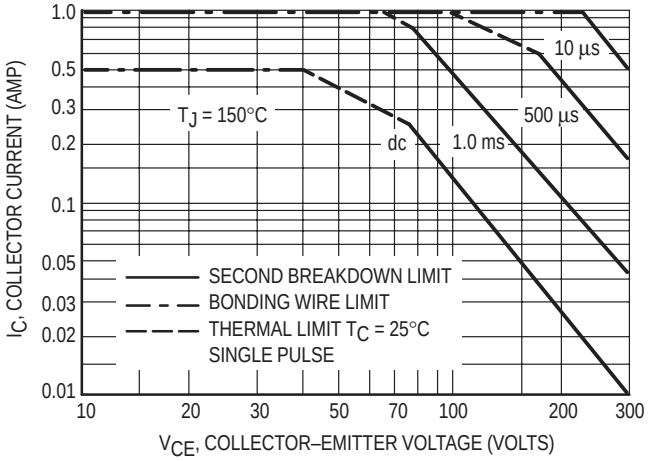


Figure 3. MJE340

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

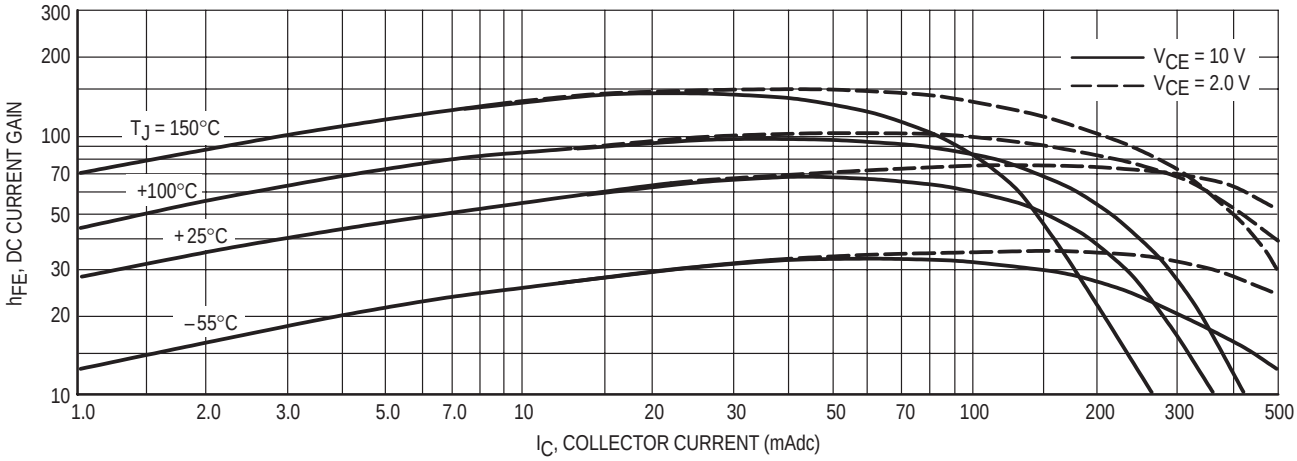


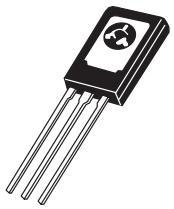
Figure 4. DC Current Gain

MJE341
MJE344

Plastic NPN Silicon Medium-Power Transistors

. . . useful for medium voltage applications requiring high f_T such as converters and extended range amplifiers.

0.5 AMPERE
POWER TRANSISTORS
NPN SILICON
150–200 VOLTS
20 WATTS



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	MJE341	MJE344	Unit
Collector–Emitter Voltage	V_{CEO}	150	200	Vdc
Collector–Base Voltage	V_{CB}	175	200	Vdc
Emitter–Base Voltage	V_{EB}	3.0	5.0	Vdc
Collector Current — Continuous	I_C	500		mAdc
Base Current	I_B	250		mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

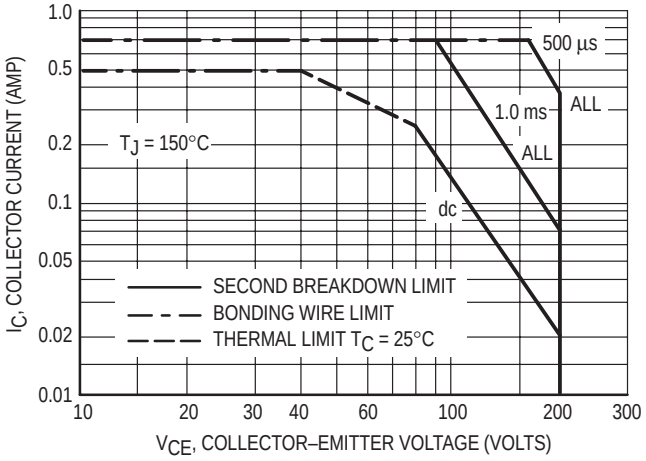


Figure 1. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less then the limitations imposed by second breakdown.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	MJE341 MJE344	$V_{CEO(sus)}$	 150 200	 — —	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0) (V_{CE} = 200 Vdc, I_B = 0)	 MJE341 MJE344	I_{CEO}	 — —	 1.0 1.0	mAdc
Collector Cutoff Current (V_{CB} = 175 Vdc, I_E = 0) (V_{CB} = 200 Vdc, I_E = 0)	 MJE341 MJE344	I_{CBO}	 — —	 0.3 0.1	mAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0) (V_{EB} = 5.0 Vdc, I_C = 0)	 MJE341 MJE344	I_{EBO}	 — —	 0.1 0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 50 mAdc, V_{CE} = 10 Vdc) (I_C = 150 mAdc, V_{CE} = 10 Vdc)	 MJE341 MJE341 MJE344 MJE341	h_{FE}	 20 25 30 20	 — 200 300 —	—
Collector–Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 5.0 mAdc) (I_C = 150 mAdc, I_B = 15 mAdc)	 MJE344 MJE341	$V_{CE(sat)}$	 — —	 1.0 2.3	Vdc
Base–Emitter On Voltage (I_C = 50 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	—	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 50 mAdc, V_{CE} = 25 Vdc, f = 10 MHz)		f_T	15	—	MHz
Output Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	15	pF
Small–Signal Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	—	—

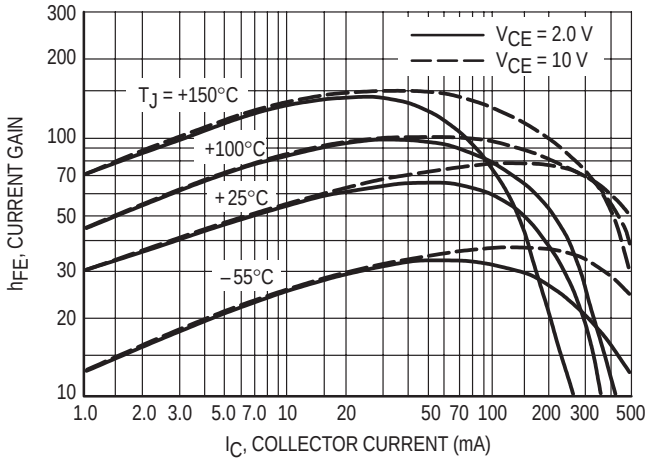


Figure 2. DC Current Gain

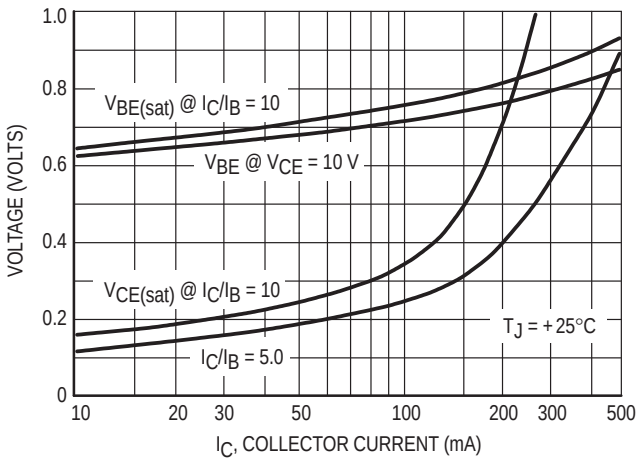


Figure 3. “On” Voltages

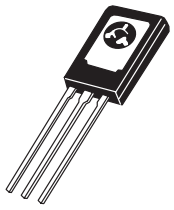
MJE350

Plastic Medium Power PNP Silicon Transistor

0.5 AMPERE
POWER TRANSISTOR
PNP SILICON
300 VOLTS
20 WATTS

. . . designed for use in line–operated applications such as low power, line–operated series pass and switching regulators requiring PNP capability.

- High Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 300 Vdc @ I_C = 1.0 mAdc
- Excellent DC Current Gain —
  h_{FE} = 30–240 @ I_C = 50 mAdc
- Plastic Thermopad Package



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	300	Vdc
Emitter–Base Voltage	V_{EB}	3.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	6.25	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	300	—	Vdc
Collector Cutoff Current (V_{CB} = 300 Vdc, I_E = 0)	I_{CBO}	—	100	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)	I_{EBO}	—	100	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30	240	—

REV 7

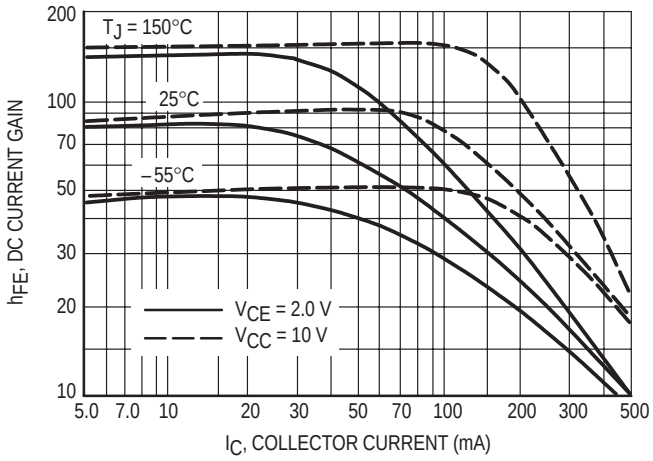


Figure 1. DC Current Gain

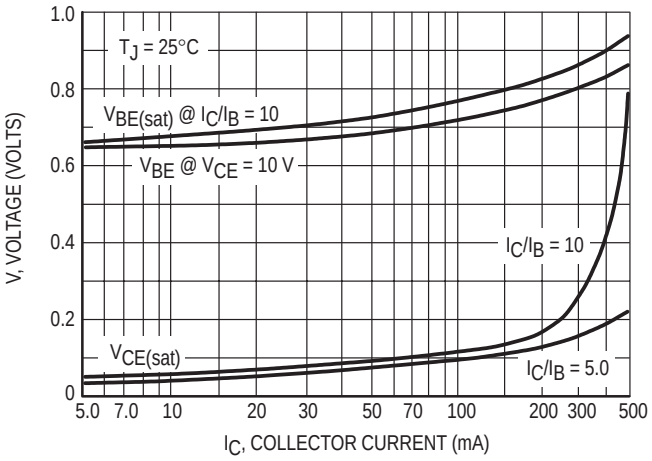


Figure 2. "On" Voltages

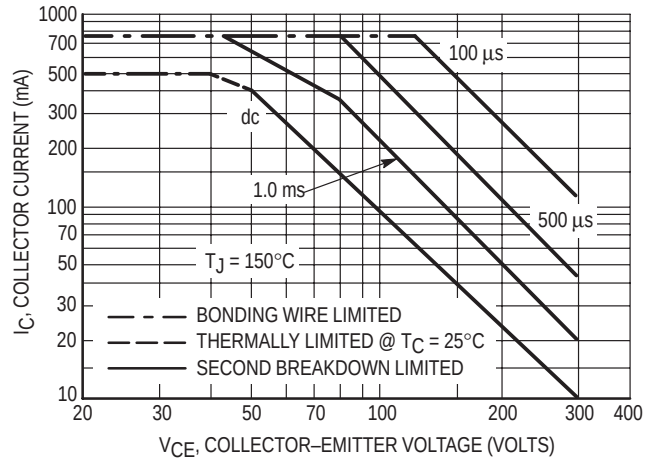


Figure 3. Active–Region Safe Operating Area

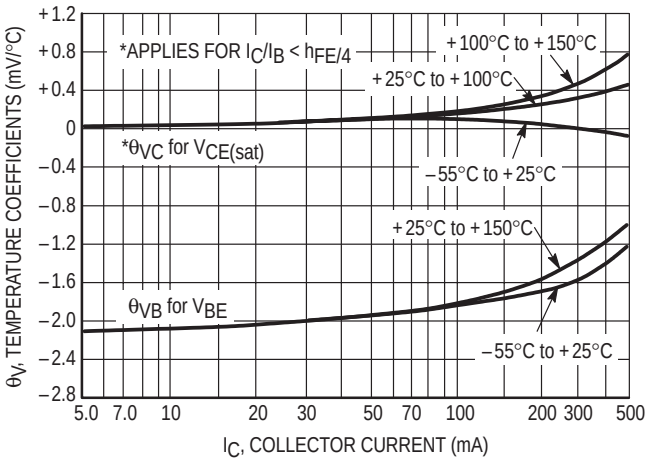


Figure 4. Temperature Coefficients

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

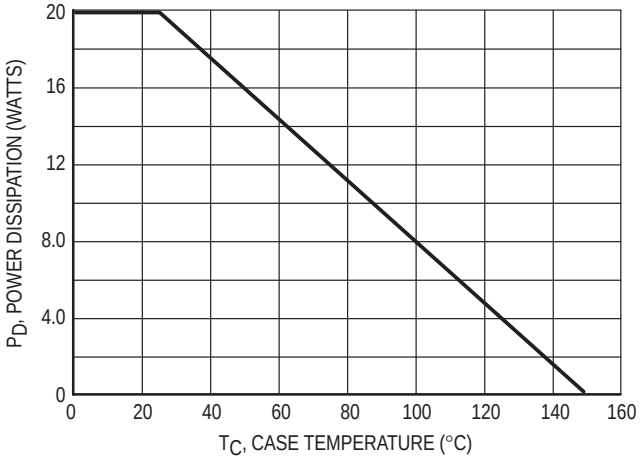


Figure 5. Power Derating

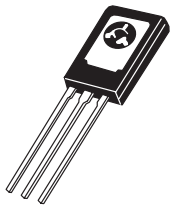
MJE371

Plastic Medium-Power PNP Silicon Transistors

4 AMPERE
POWER TRANSISTOR
PNP SILICON
40 VOLTS
40 WATTS

. . . designed for use in general–purpose amplifier and switching circuits. Recommended for use in 5 to 20 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 1.0 Adc
- MJE371 is Complementary to NPN MJE521



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	40	Vdc
Collector–Base Voltage	V_{CB}	40	Vdc
Emitter–Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	4.0 8.0	Adc
Base Current — Continuous	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	40	—	Vdc
Collector–Base Cutoff Current (V_{CB} = 40 Vdc, I_E = 0)	I_{CBO}	—	100	µAdc
Emitter–Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	100	µAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	40	—	—

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

REV 2

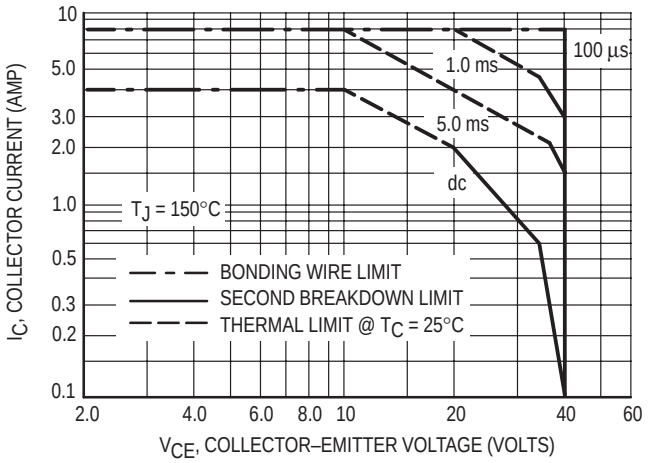


Figure 1. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less then the limitations imposed by second breakdown.

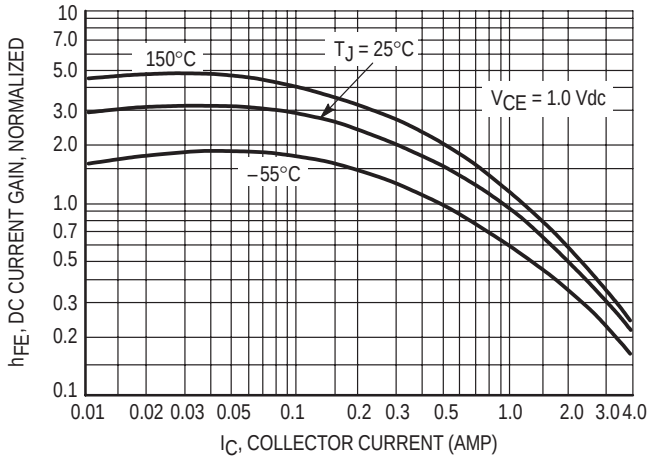


Figure 2. DC Current Gain

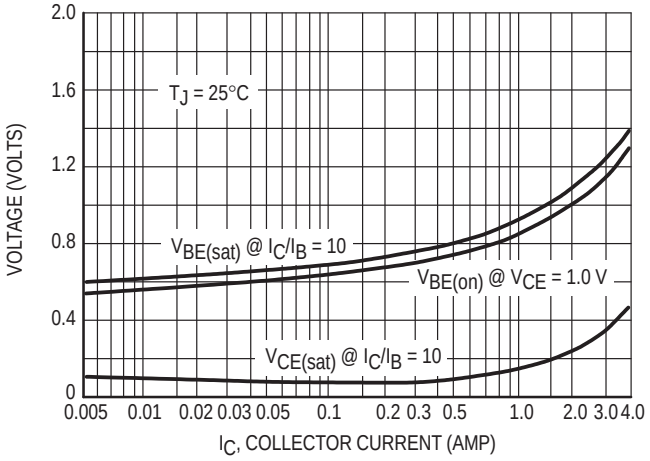


Figure 3. "On" Voltage

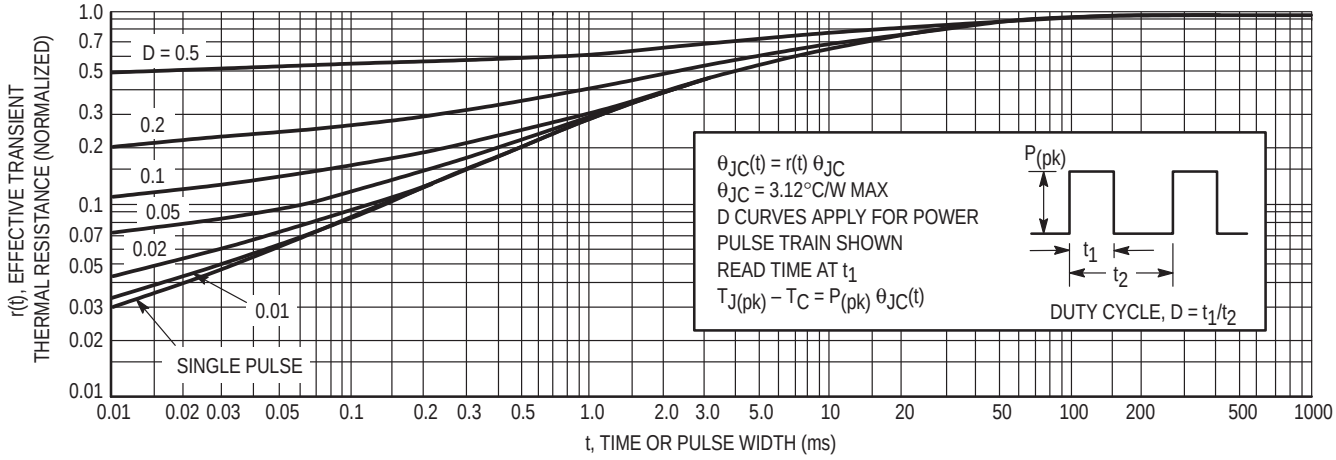


Figure 4. Thermal Response

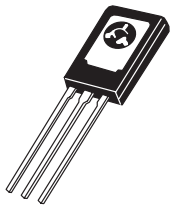
MJE521

Plastic Medium-Power NPN Silicon Transistor

. . . designed for use in general–purpose amplifier and switching circuits. Recommended for use in 5 to 10 Watt audio amplifiers utilizing complementary symmetry circuitry.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 1.0 Adc
- Complementary to PNP MJE371

4 AMPERE
POWER TRANSISTOR
NPN SILICON
40 VOLTS
40 WATTS



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	40	Vdc
Collector–Base Voltage	V_{CB}	40	Vdc
Emitter–Base Voltage	V_{EB}	4.0	Vdc
Collector Current — Continuous — Peak	I_C	4.0 8.0	Adc
Base Current — Continuous	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	3.12	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	40	—	Vdc
Collector–Base Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	—	100	µAdc
Emitter–Base Cutoff Current (V_{EB} = 4.0 Vdc, I_C = 0)	I_{EBO}	—	100	µAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	40	—	—

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

REV 1

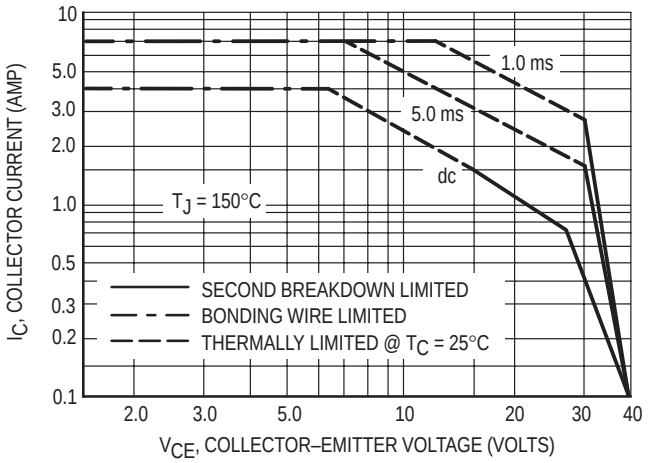


Figure 1. Active–Region Safe Operating Area

The data of Figure 1 based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided (T_{Jpk}) ≤ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

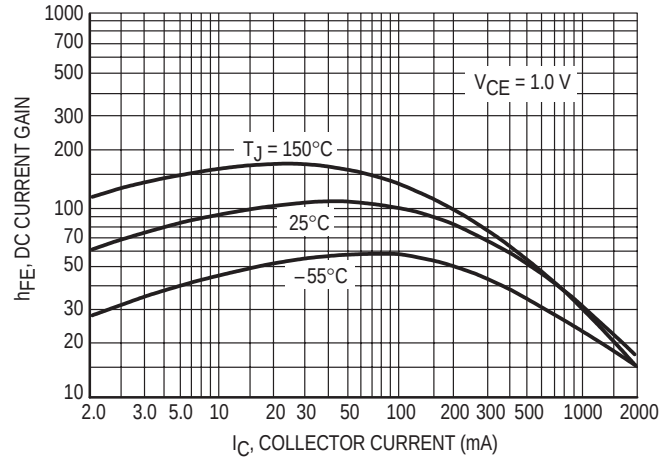


Figure 2. DC Current Gain

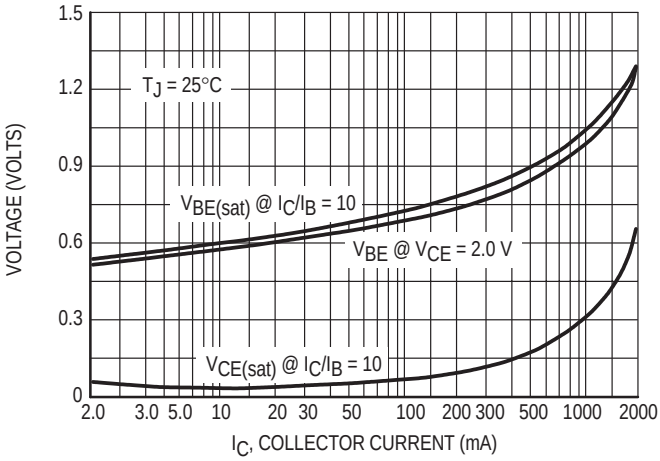


Figure 3. "On" Voltage

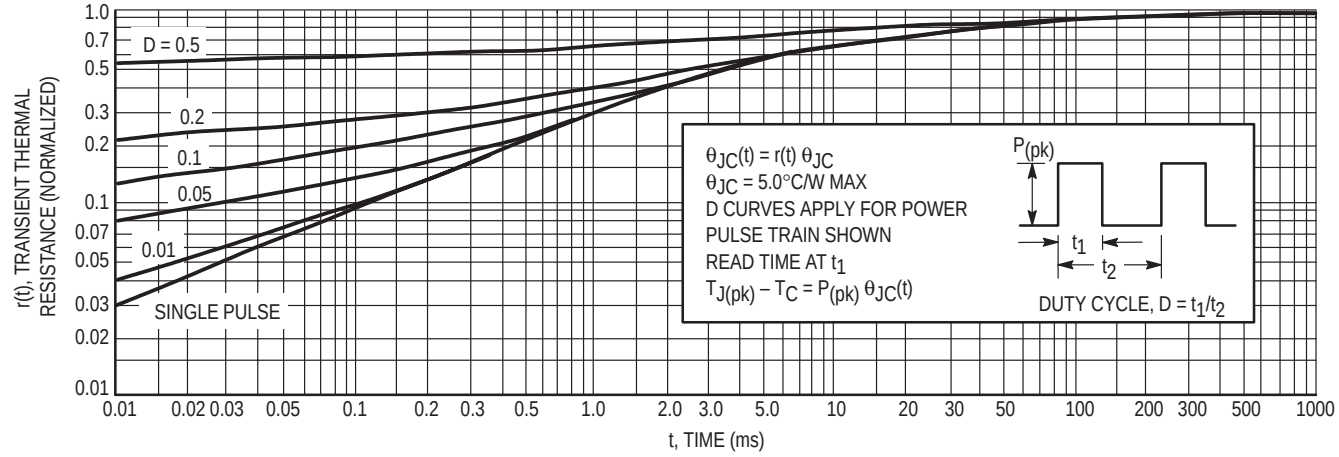


Figure 4. Thermal Response

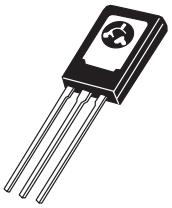
Plastic Darlington Complementary Silicon Power Transistors

. . . designed for general–purpose amplifier and low–speed switching applications.

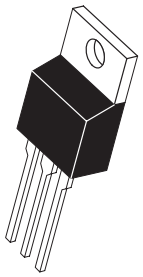
- High DC Current Gain —
  h_{FE} = 2000 (Typ) @ I_C = 2.0 Adc
- Monolithic Construction with Built–in Base–Emitter Resistors to Limit Leakage Multiplication
- Choice of Packages —
  MJE700 and MJE800 series
  T0220AB, MJE700T and MJE800T

PNP
MJE700,T
MJE702
MJE703
NPN
MJE800,T
MJE802
MJE803

4.0 AMPERE
DARLINGTON
POWER TRANSISTORS
COMPLEMENTARY
SILICON
40 WATT
50 WATT



CASE 77–08
TO–225AA TYPE
MJE700–703
MJE800–803



CASE 221A–06
TO–220AB
MJE700T
MJE800T

MAXIMUM RATINGS

Rating	Symbol	MJE700,T MJE800,T	MJE702 MJE703 MJE802 MJE803	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current	I_C	4.0		Adc
Base Current	I_B	0.1		Adc
		CASE 77	**TO–220**	
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	50 0.40	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case CASE 77 TO–220	$R_{\theta JC}$	 3.13 2.50	°C/W

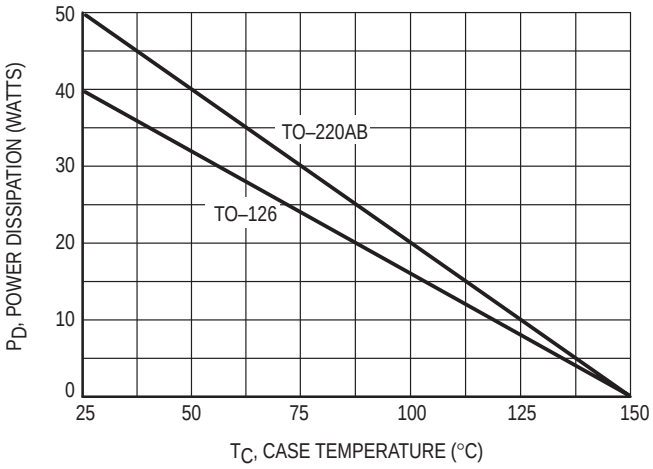


Figure 1. Power Derating

REV 3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (1) (I_C = 50 mAdc, I_B = 0)	MJE700,T, MJE800,T	$V_{(BR)CEO}$	60	—	Vdc
	MJE702, MJE703, MJE802, MJE803		80	—	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 60 Vdc, I_B = 0)	MJE700,T, MJE800,T		—	100	
(V_{CE} = 80 Vdc, I_B = 0)	MJE702, MJE703, MJE802, MJE803		—	100	
Collector Cutoff Current (V_{CB} = Rated BV_{CEO}, I_E = 0)		I_{CBO}	—	100	μAdc
(V_{CB} = Rated BV_{CEO}, I_E = 0, T_C = 100°C)			—	500	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (1)		h_{FE}			—
(I_C = 1.5 Adc, V_{CE} = 3.0 Vdc)	MJE700,T, MJE702, MJE800,T, MJE802		750	—	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	MJE703, MJE803		750	—	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	All devices		100	—	
Collector–Emitter Saturation Voltage (1)		$V_{CE(sat)}$			Vdc
(I_C = 1.5 Adc, I_B = 30 mAdc)	MJE700,T, MJE702, MJE800,T, MJE802		—	2.5	
(I_C = 2.0 Adc, I_B = 40 mAdc)	MJE703, MJE803		—	2.8	
(I_C = 4.0 Adc, I_B = 40 mAdc)	All devices		—	3.0	
Base–Emitter On Voltage (1)		$V_{BE(on)}$			Vdc
(I_C = 1.5 Adc, V_{CE} = 3.0 Vdc)	MJE700,T, MJE702, MJE800,T, MJE802		—	2.5	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)	MJE703, MJE803		—	2.5	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)	All devices		—	3.0	
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 1.5 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		h_{fe}	1.0	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

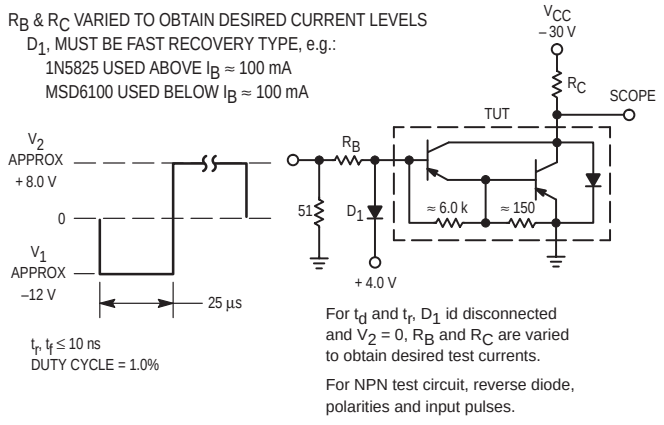


Figure 2. Switching Times Test Circuit

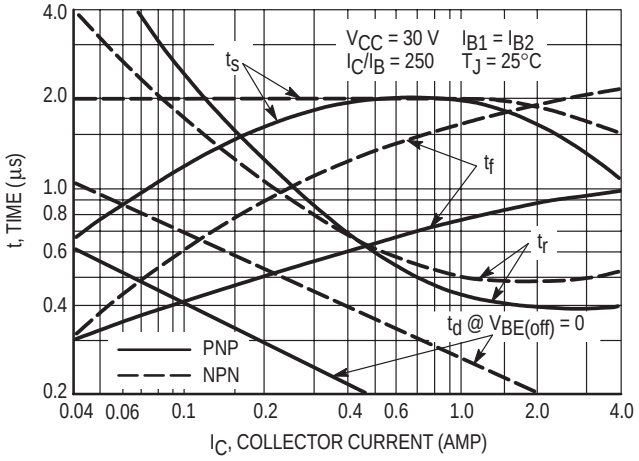


Figure 3. Switching Times

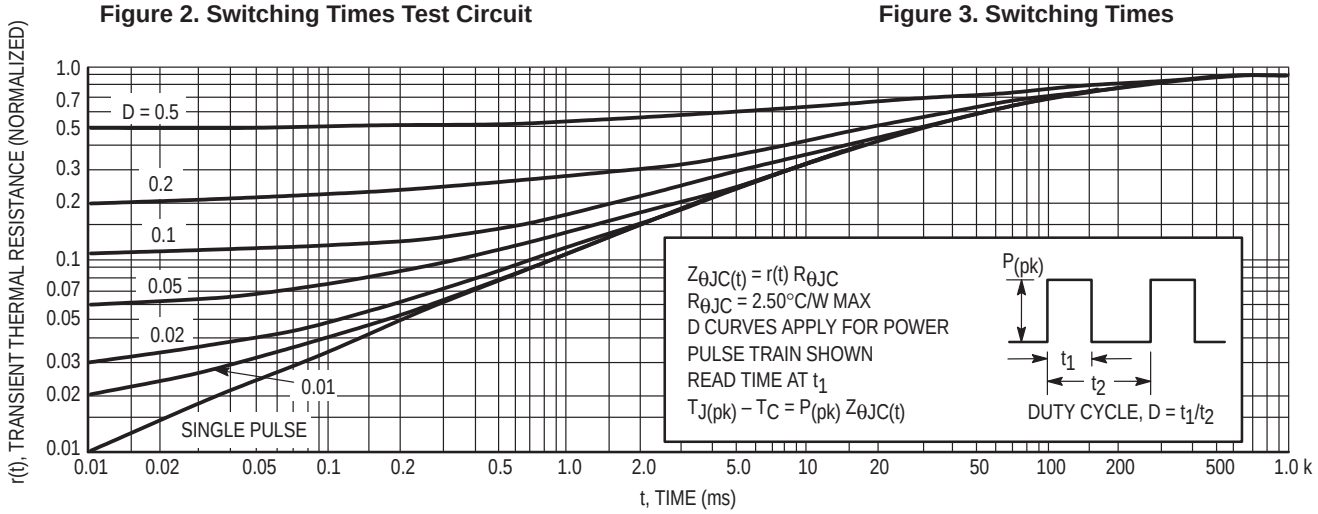


Figure 4. Thermal Response (MJE700T, 800T Series)

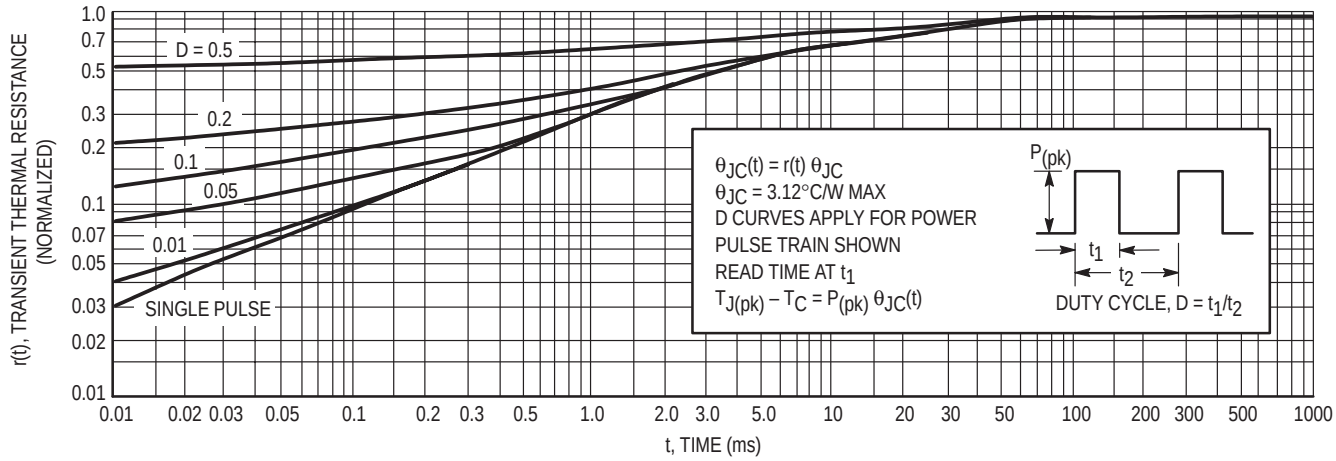


Figure 5. Thermal Response (MJE700, 800 Series)

ACTIVE–REGION SAFE–OPERATING AREA

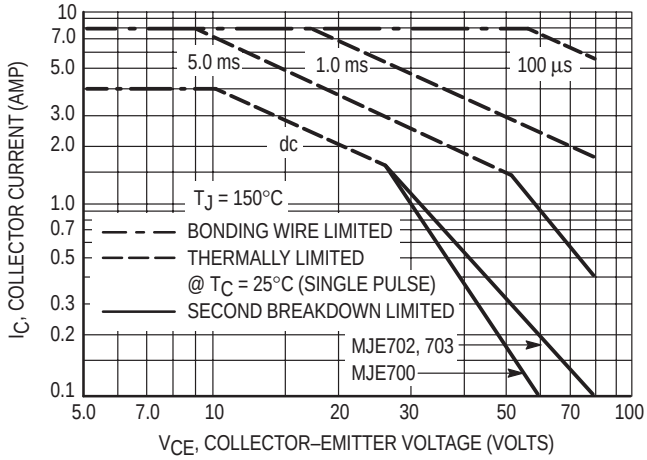


Figure 6. MJE700 Series

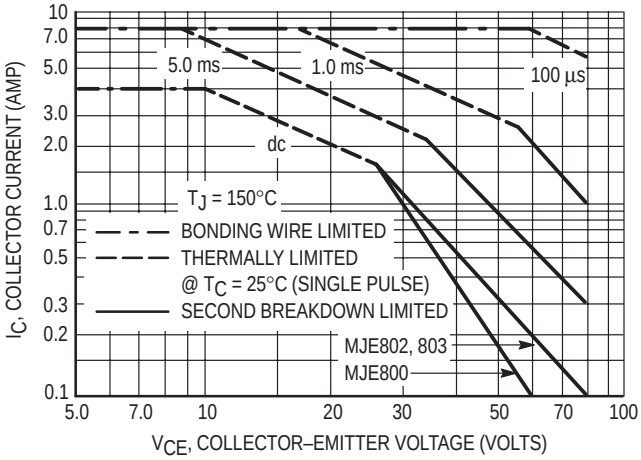


Figure 7. MJE800 Series

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 6 and 7 are based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4 or 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

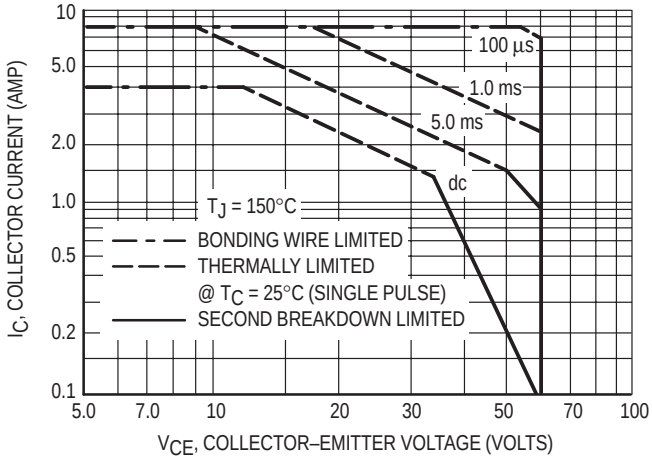


Figure 8. MJE700T

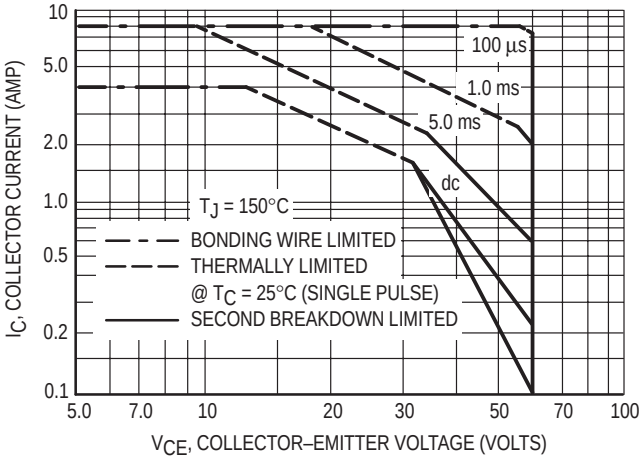
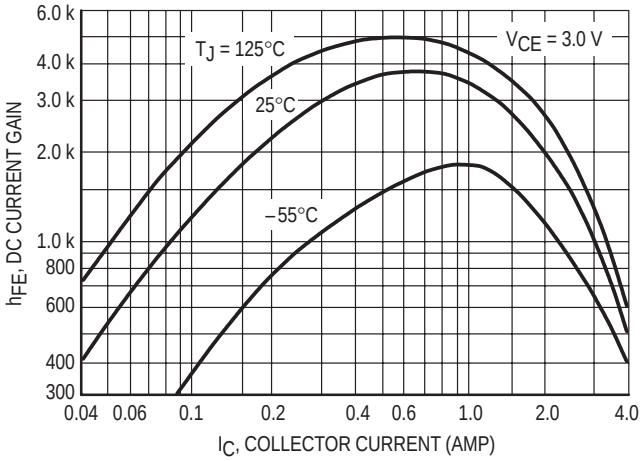


Figure 9. MJE800T

PNP
MJE700, T Series



NPN
MJE800, T Series

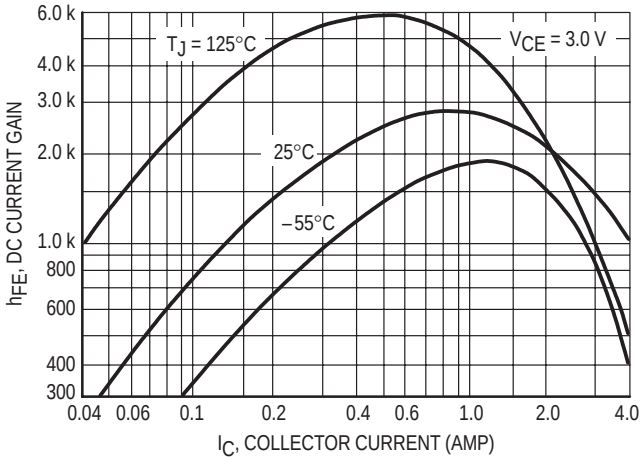
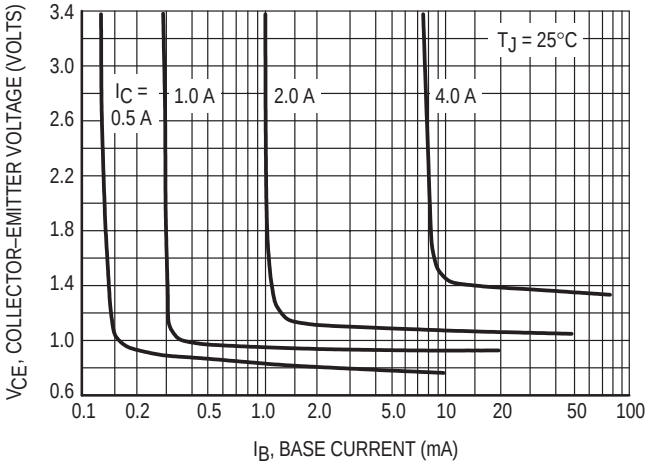


Figure 10. DC Current Gain



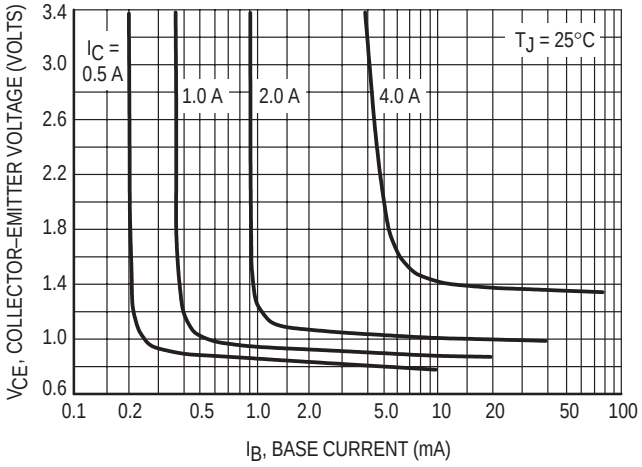
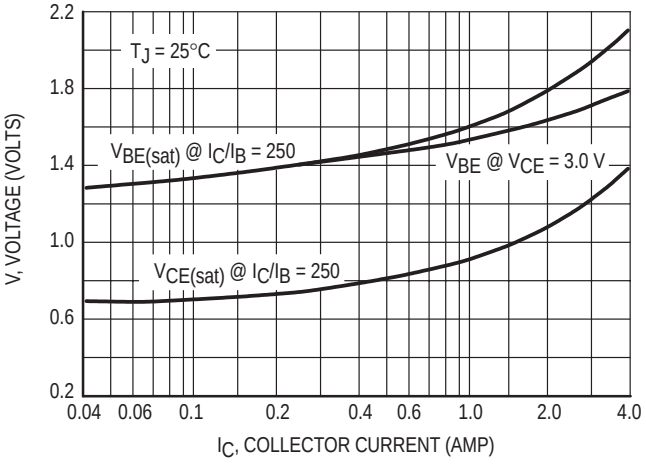


Figure 11. Collector Saturation Region



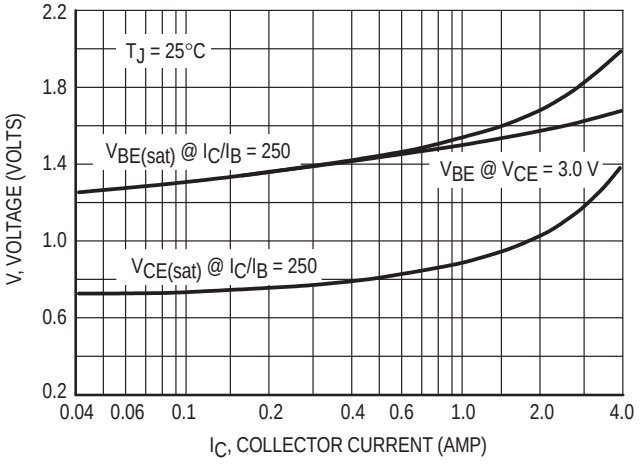


Figure 12. “On” Voltages

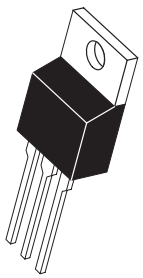
MJE1123

Bipolar Power PNP Low Dropout Regulator Transistor

PNP LOW DROPOUT TRANSISTOR 4.0 AMPERES 40 VOLTS

The MJE1123 is an applications specific device designed to provide low–dropout linear regulation for switching–regulator post regulators, battery powered systems and other applications. The MJE1123 is fully specified in the saturation region and exhibits the following main features:

- High Gain Limits Base–Drive Losses to only 1–2% of Circuit Output Current
- Gain is 100 Minimum at I_C = 1.0 Amp, V_{CE} = 7.0 Volts
- Excellent Saturation Voltage Characteristic, 0.2 Volts Maximum at 1.0 Amp



CASE 221A–06
TO–220AB

MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted.)

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	40	Vdc
Collector–Base Voltage	V_{CB}	50	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C I_{CM}	4.0 8.0	Adc
Base Current — Continuous	I_B	4.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	– 65 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 70	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS*					
Collector–Emitter Sustaining Voltage (I_C = 1.0 mA, I = 0)	$V_{CEO(sus)}$	40	65	—	Vdc
Emitter–Base Voltage (I_E = 100 μA)	V_{EBO}	7.0	11	—	Vdc
Collector Cutoff Current	I_{CEO}				μAdc
(V_{CE} = 7.0 Vdc, I_B = 0)		—	—	100	
(V_{CE} = 20 Vdc, I_B = 0)		—	—	250	
ON CHARACTERISTICS*					
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 1.0 Adc, I_B = 20 mAdc)		—	0.16	0.30	
(I_C = 1.0 Adc, I_B = 50 mAdc)		—	0.13	0.25	
(I_C = 1.0 Adc, I_B = 120 mAdc)		—	0.10	0.20	
(I_C = 2.0 Adc, I_B = 50 mAdc)		—	0.25	0.40	
(I_C = 2.0 Adc, I_B = 120 mAdc)		—	0.20	0.35	
(I_C = 4.0 Adc, I_B = 120 mAdc)		—	0.45	0.75	

* Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS* (continued)					
Base–Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 1.0 Adc, I_B = 20 mAdc)		—	0.77	0.95	
(I_C = 2.0 Adc, I_B = 50 mAdc)		—	0.87	1.20	
(I_C = 4.0 Adc, I_B = 120 mAdc)		—	1.00	1.40	
DC Current Gain	h_{FE}				—
(I_C = 1.0 Adc, V_{CE} = 7.0 Vdc)		100	170	225	
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)		100	180	225	
(I_C = 2.0 Adc, V_{CE} = 7.0 Vdc)		75	120	170	
(I_C = 2.0 Adc, V_{CE} = 10 Vdc)		80	140	180	
(I_C = 4.0 Adc, V_{CE} = 7.0 Vdc)		45	75	100	
(I_C = 4.0 Adc, V_{CE} = 10 Vdc)		45	79	100	
Base–Emitter On Voltage	$V_{BE(on)}$				Vdc
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)		—	0.75	0.90	
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)		—	0.84	1.00	
(I_C = 4.0 Adc, V_{CE} = 1.0 Vdc)		—	0.90	1.20	
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)	f_T	5.0	11.5	—	MHz

* Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.

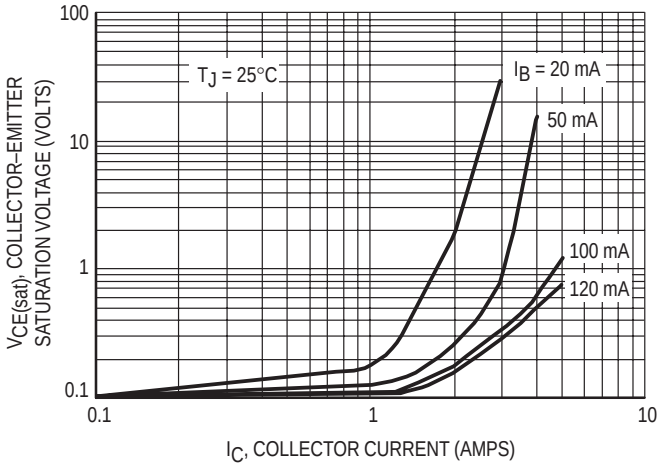


Figure 1. Saturation Voltage versus Collector Current as a Function of Base Drive

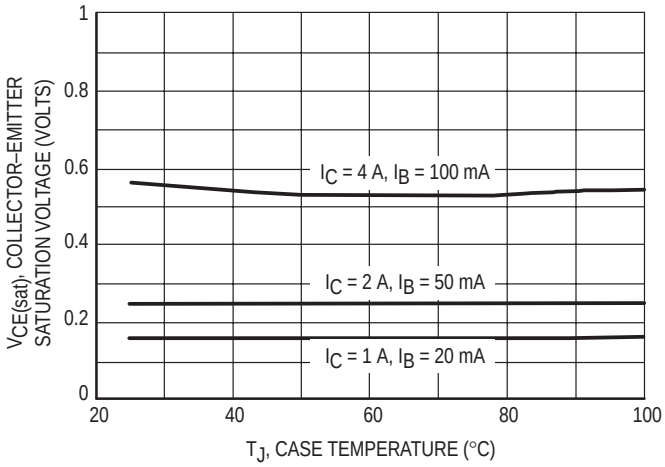


Figure 2. Saturation Voltage versus Temperature

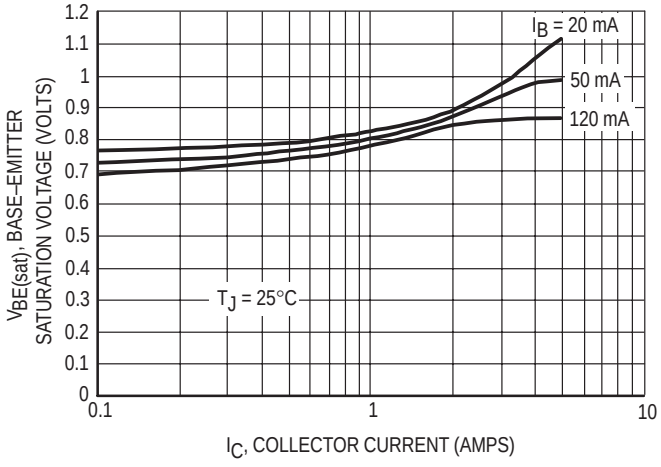


Figure 3. Base–Emitter Saturation Voltage

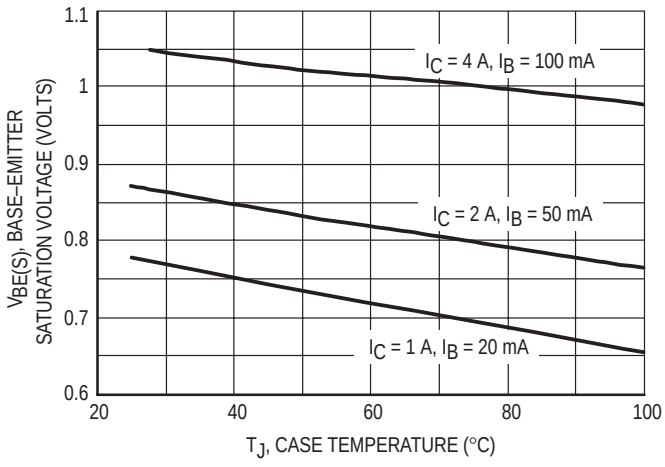


Figure 4. Base–Emitter Saturation Voltage versus Temperature

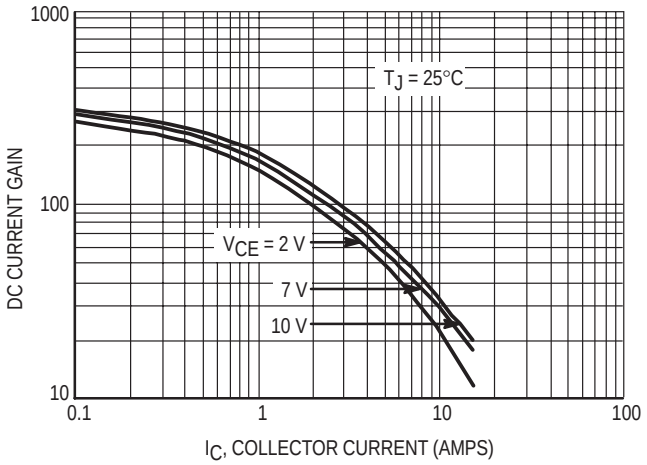


Figure 5. DC Current Gain

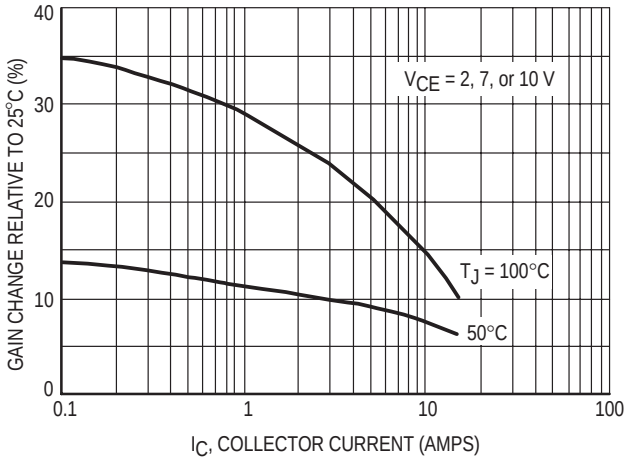
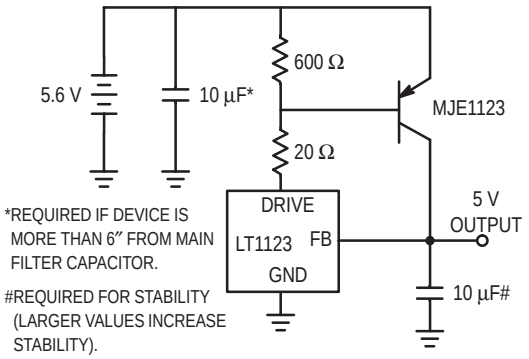


Figure 6. DC Current Gain Variation

TYPICAL LOW PASS TRANSISTOR APPLICATION

The MJE1123 was designed to operate as a low pass transistor in conjunction with the LT1123 offered by Linear Technology Corporation. Together they provide several excellent advantages:

- A dropout voltage below 50 mV at 1.0 amp, increasing to only 225 mV at 4.0 amps, typically.
- Line and load regulation are within 5.0 mV.
- Initial output accuracy is better than 1 percent.
- Full short circuit protection is included.
- Base drive loss is less than 2% of output current . . . even at 4.0 full amps output.
- The high gain and excellent collector–emitter saturation voltage make the combination better than monolithic devices.



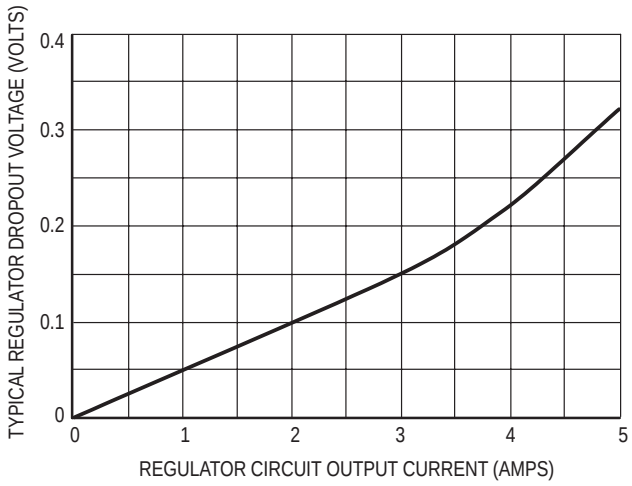


Figure 7. Typical Dropout Voltage of a MJE1123 and LT1123 Circuit

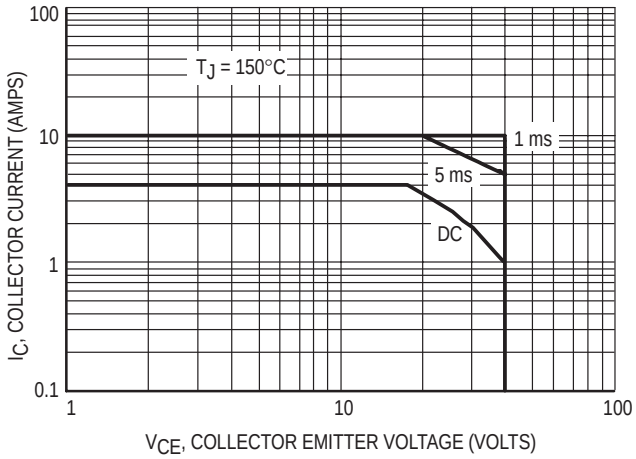


Figure 8. Maximum Forward Bias Safe Operating Area

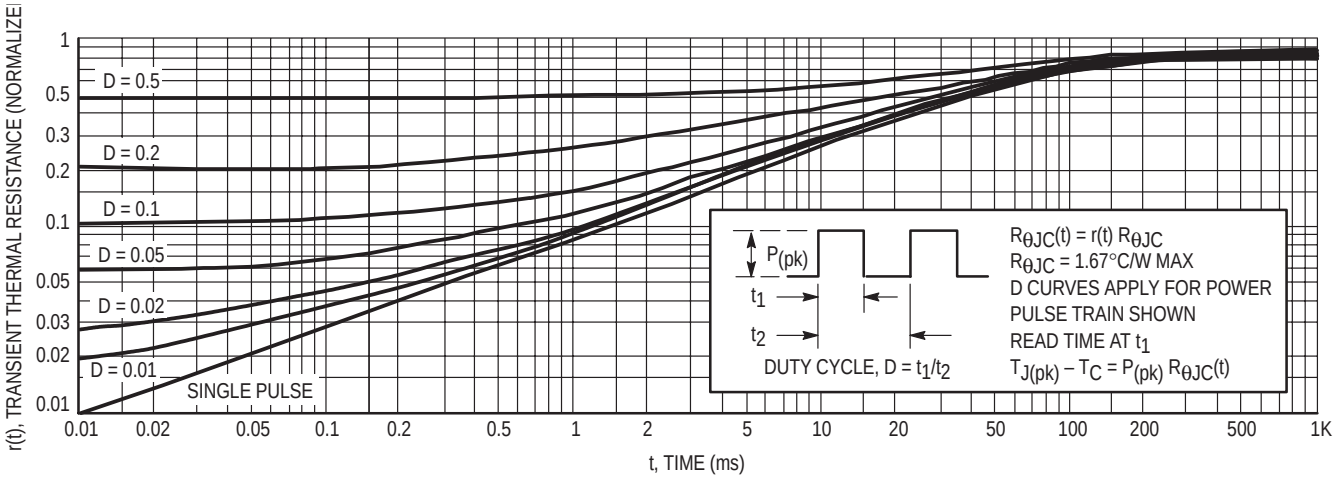


Figure 9. Typical Thermal Response

MJE1320

Designer's™ Data Sheet

NPN Silicon Power Transistor

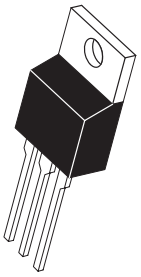
Switchmode Series

POWER TRANSISTOR
2 AMPERES
900 VOLTS
80 WATTS

This transistor is designed for high–voltage, power switching in inductive circuits where RBSOA and breakdown voltage are critical. They are particularly suited for line–operated switchmode applications.

Typical Applications:
- Fluorescent Lamp Ballasts
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Features:
- High V_{CEV} Capability (1800 Volts)
- Low Saturation Voltage
- 100°C Performance Specified for:
  - Reverse–Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	900	Vdc
Collector–Emitter Voltage	V_{CEV}	1800	Vdc
Emitter Base Voltage	V_{EB}	9	Vdc
Collector Current — Continuous Peak(1)	I_C I_{CM}	2 5	Adc
Base Current — Continuous Peak(1)	I_B I_{BM}	1.5 2.5	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	80 32 0.64	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector–Emitter Sustaining Voltage (I_C = 50 mA, I_B = 0)			$V_{CEO(sus)}$	900	—	—	Vdc
Collector Cutoff Current			I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)				—	—	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)				—	—	2.5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)			I_{EBO}	—	—	0.25	mAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with base forward biased			$I_{S/b}$	See Figure 13			
Clamped Inductive SOA with Base Reverse Biased			RBSOA	See Figure 14			
ON CHARACTERISTICS(1)							
DC Current Gain (V_{CE} = 5 Vdc)	I_C = 2 Adc		h_{FE}	2.5	4.5	—	—
	I_C = 1 Adc			3	7	—	—
Collector–Emitter Saturation Voltage			$V_{CE(sat)}$				Vdc
(I_C = 1 Adc, I_B = 0.5 Adc)				—	0.18	1	
(I_C = 2 Adc, I_B = 1 Adc)				—	0.3	2.5	
(I_C = 1 Adc, I_B = 0.5 Adc, T_C = 100°C)				—	0.3	1.5	
Base–Emitter Saturation Voltage			$V_{BE(sat)}$				Vdc
(I_C = 1 Adc, I_B = 0.5 Adc)				—	0.2	1.5	
(I_C = 2 Adc, I_B = 1 Adc)				—	0.9	2.8	
(I_C = 1 Adc, I_B = 0.5 Adc, T_C = 100°C)				—	0.15	1.5	
DYNAMIC CHARACTERISTICS							
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)			C_{ob}	—	80	—	pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	V_{CC} = 250 Vdc, I_C = 1 A I_{B1} = I_{B2} = 0.5 Adc t_p = 25 μs, Duty Cycle ≤ 2%		t_d	—	0.1	—	μs
Rise Time			t_r	—	0.8	—	μs
Storage Time			t_s	—	4	—	μs
Fall Time			t_f	—	0.8	—	μs
Inductive Load, Clamped (Table 2)							
Storage Time	I_C = 1 A, V_{clamp} = 400 Vdc, $V_{BE(off)}$ = 2 Vdc, I_{B1} = 0.5 Adc	T_C = 25°C	t_{sv}	—	2.8	—	μs
Crossover Time			t_c	—	2.2	—	μs
Storage Time		T_C = 100°C	t_{sv}	—	3.7	10.5	μs
Crossover Time			t_c	—	3.5	10	μs
Fall Time							

(1) Pulse Test: Pulse Width = 300 μs. Duty Cycle ≤ 2%.

TYPICAL STATIC CHARACTERISTICS

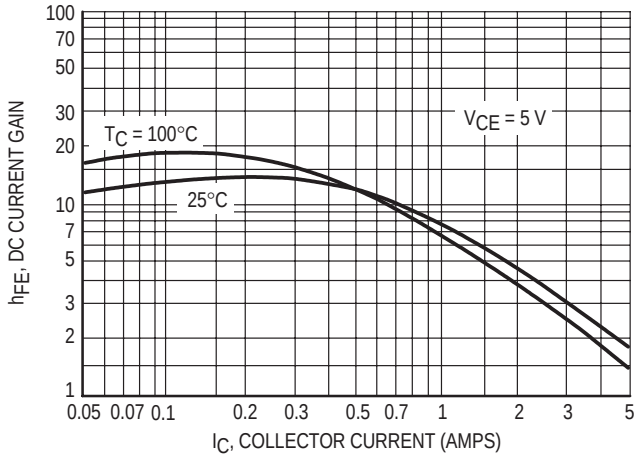


Figure 1. DC Current Gain

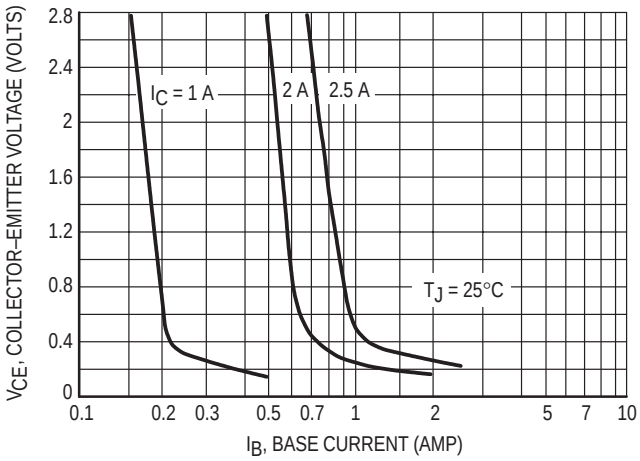


Figure 2. Collector Saturation Region

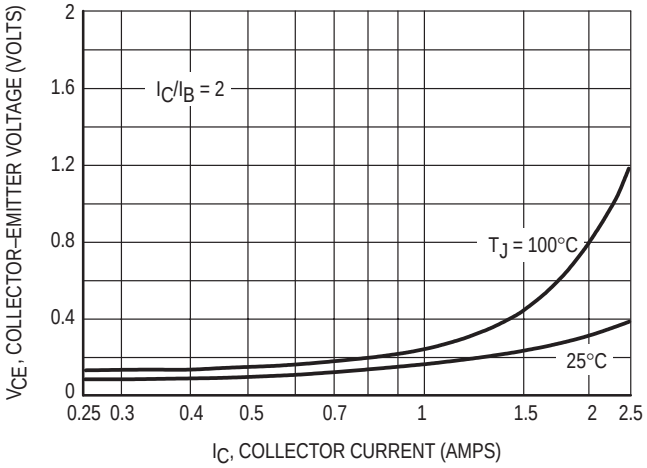


Figure 3. Collector–Emitter Saturation Voltage

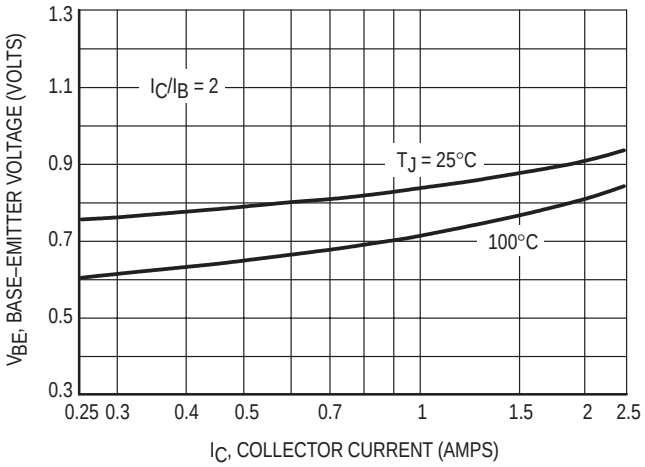


Figure 4. Base–Emitter Saturation Voltage

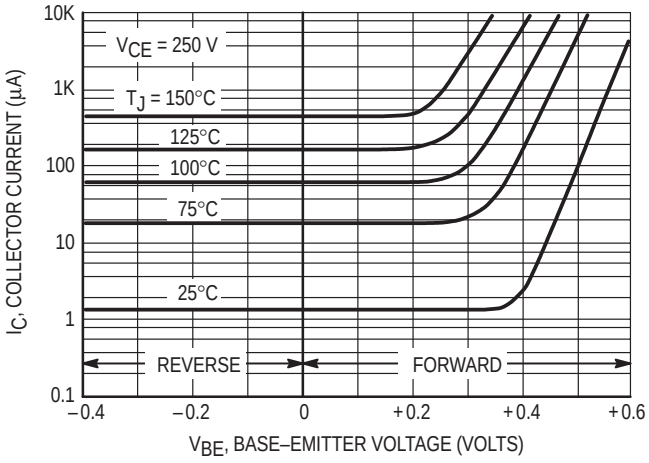


Figure 5. Collector Cutoff Region

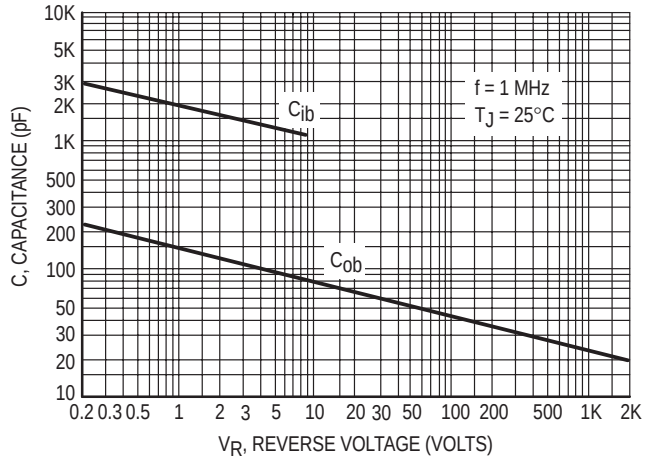


Figure 6. Capacitance Variation

TYPICAL DYNAMIC CHARACTERISTICS

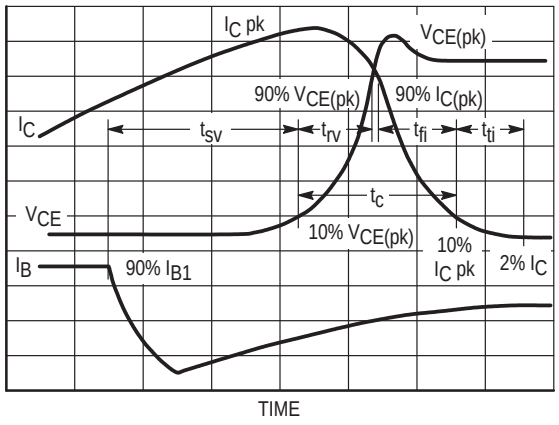


Figure 7. Inductive Switching Measurements

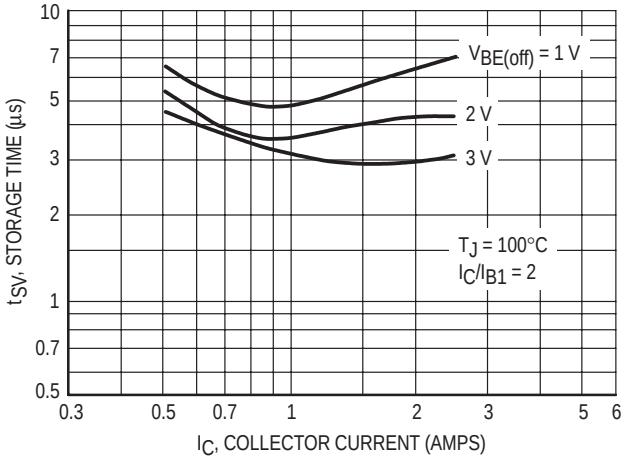


Figure 8. Inductive Storage Time

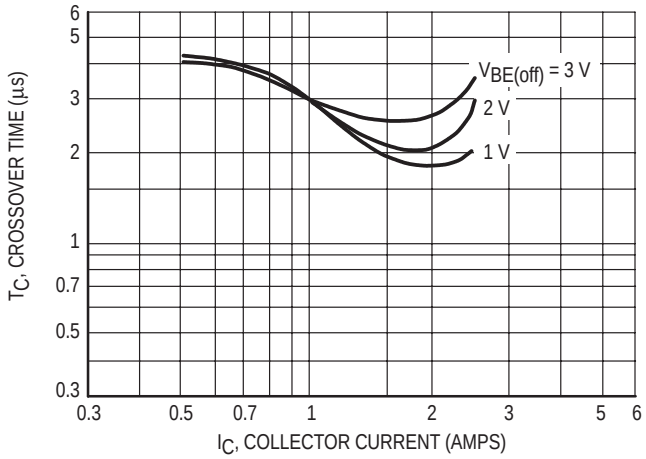


Figure 9. Inductive Crossover Time

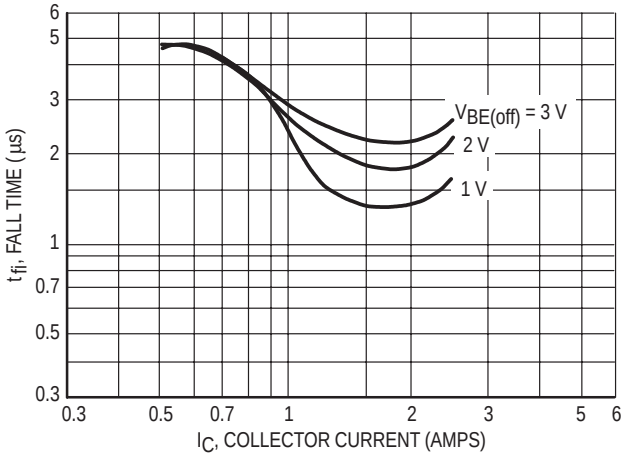
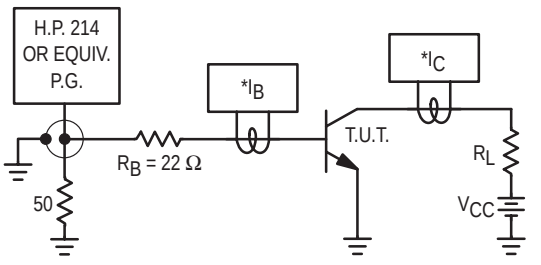
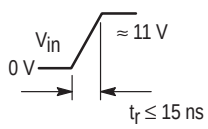


Figure 10. Inductive Fall Time

Table 1. Resistive Load Switching

t_d and t_r

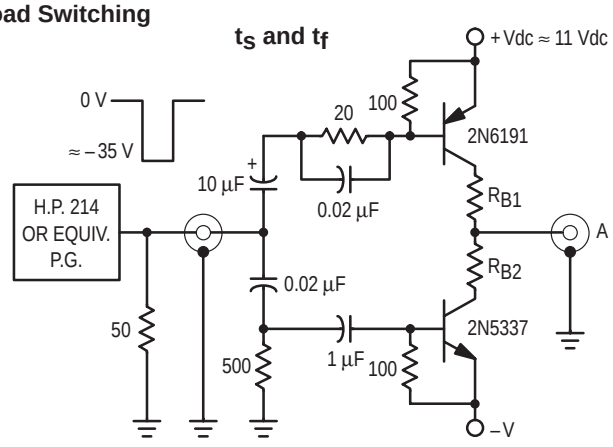


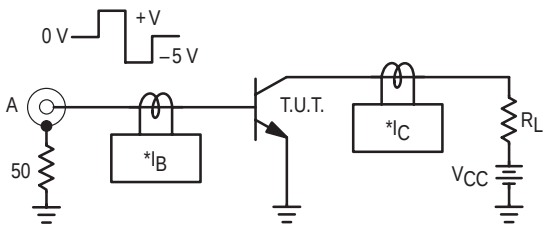


V_{CC} = 250 Vdc
R_L = 250 Ω
I_C = 1 Adc
I_B = 0.5 Adc

*Tektronix AM503
P6302 or Equivalent

t_s and t_f

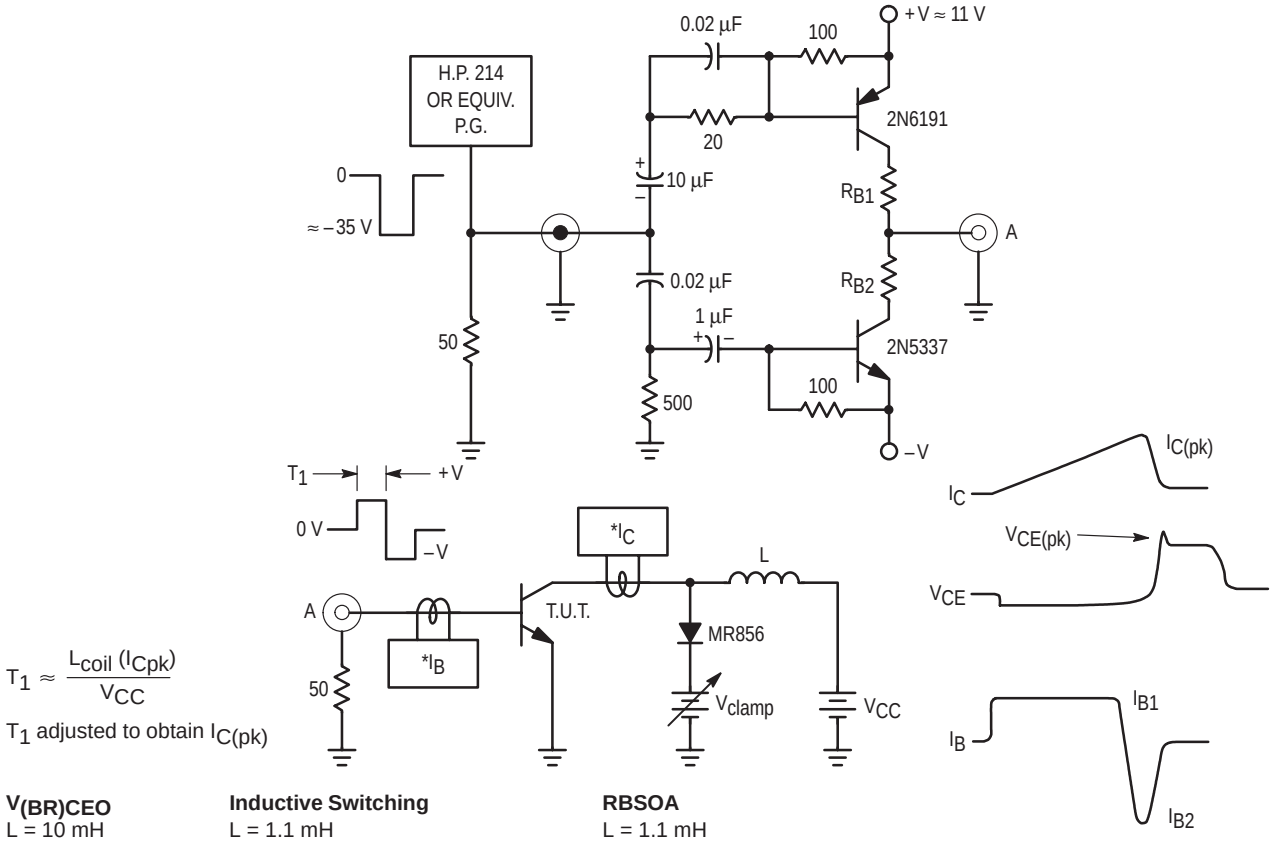




V_{CC} = 250 Vdc
R_L = 250 Ω
I_C = 1 Adc
I_{B1} = 0.5 Adc
I_{B2} = 0.5 Adc
For $V_{BE(off)}$ = 5 V
R_{B1} = 22 Ω
R_{B2} = 10 Ω
R_{B2} = 0 Ω

Note: Adjust – V to obtain desired $V_{BE(off)}$ at Point A.

Table 2. Inductive Load Switching



$T_1 \approx \frac{L_{coil}\,(I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$	Inductive Switching	RBSOA
L = 10 mH	L = 1.1 mH	L = 1.1 mH
$R_{B2} = \infty$	$R_{B2} = 0$	$R_{B2} = 0$
V_{CC} = 20 Volts	V_{CC} = 20 Volts	V_{CC} = 20 Volts
	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

*Tektronix P–6042 or Equivalent

Scope — Tektronix 7403 or Equivalent

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 14. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

GUARANTEED SAFE OPERATING AREA

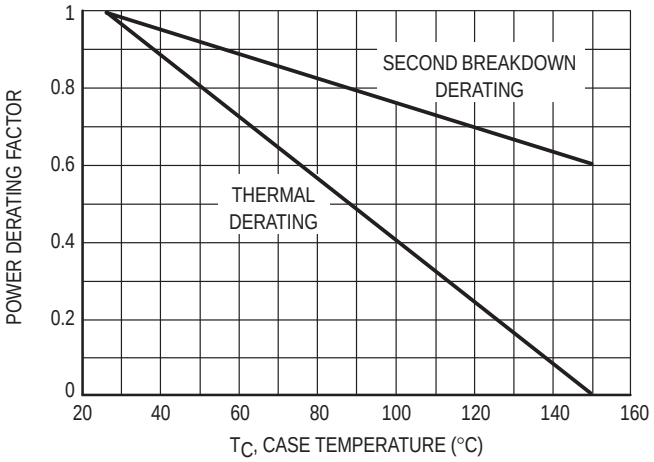


Figure 11. Power Derating

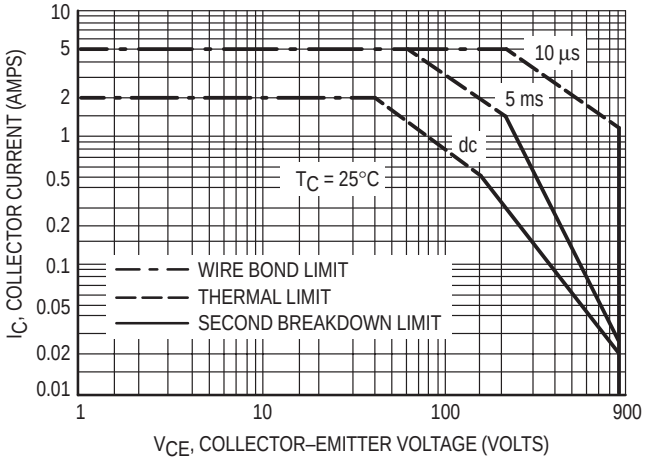


Figure 12. Maximum Rated Forward Bias Safe Operating Area

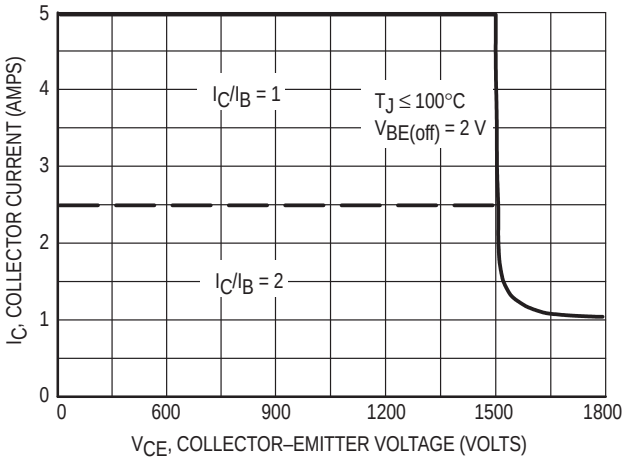


Figure 13. Maximum Rated Reverse Bias Safe Operating Area

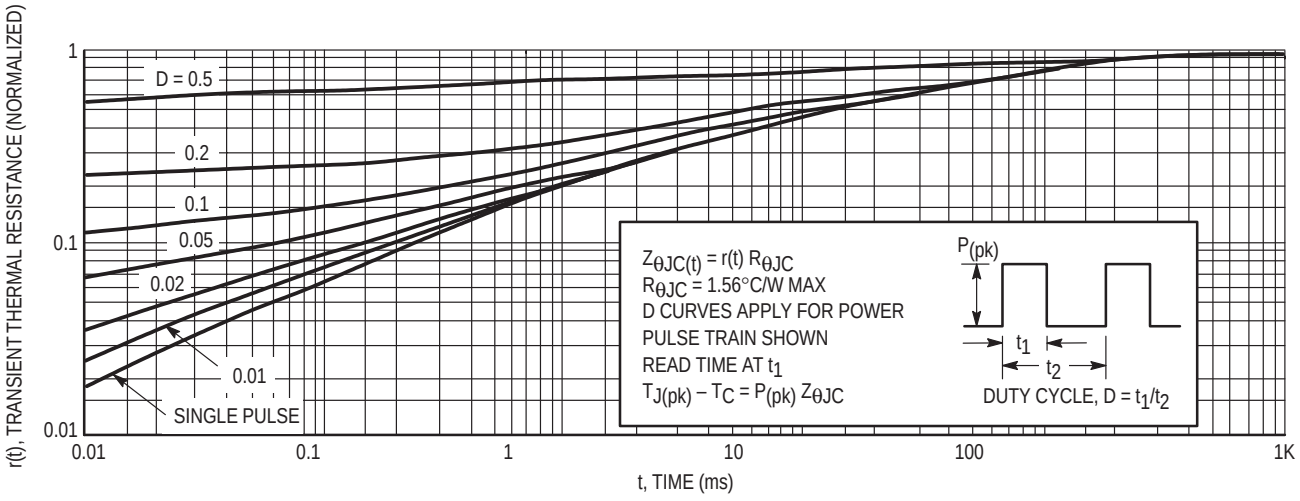


Figure 14. Thermal Response

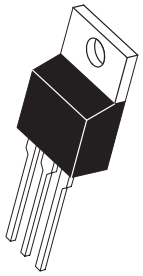
MJE2360T
MJE2361T

NPN Silicon High-Voltage Transistor

. . . useful for general–purpose, high voltage applications requiring high f_T.

- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 350 Vdc (Min) @ I_C = 2.5 mAdc
- DC Current Gain —
  h_{FE} = 40 (Min) @ I_C = 100 mAdc — MJE2361T
- Current–Gain–Bandwidth Product —
  f_T = 10 MHz (Typ) @ I_C = 50 mAdc

0.5 AMPERE
POWER TRANSISTORS
NPN SILICON
350 VOLTS
30 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	350	Vdc
Collector–Base Voltage	V_{CB}	375	Vdc
Emitter–Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous	I_C	0.5	Adc
Base Current	I_B	0.25	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.24	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.167	°C/W

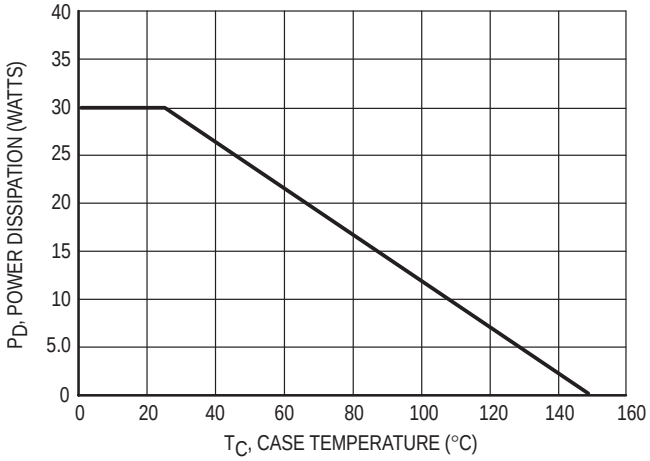


Figure 1. Power–Temperature Derating Curve

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage(1) (I_C = 2.5 mAdc, I_B = 0)		$V_{CEO(sus)}$	350	—	—	Vdc
Collector Cutoff Current (V_{CE} = 250 Vdc, I_B = 0)		I_{CEO}	—	—	0.25	mAdc
Collector Cutoff Current (V_{CE} = 375 Vdc, $V_{EB(off)}$ = 1.5 Vdc)		I_{CEX}	—	—	0.5	mAdc
Collector Cutoff Current (V_{CB} = 375 Vdc, I_E = 0)		I_{CBO}	—	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	—	0.1	mAdc
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				—
(I_C = 50 mAdc, V_{CE} = 10 Vdc)	MJE2360T		25	—	200	
	MJE2361T		50	—	250	
(I_C = 100 mAdc, V_{CE} = 10 Vdc)	MJE2360T		15	—	—	
	MJE2361T		40	—	—	
Collector–Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 10 mAdc)		$V_{CE(sat)}$	—	—	1.5	Vdc
Base–Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	—	—	1.0	Vdc
DYNAMIC CHARACTERISTICS						
Current–Gain — Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)		f_T	—	10	—	MHz
Output Capacitance (V_{CB} = 100 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	—	20	—	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

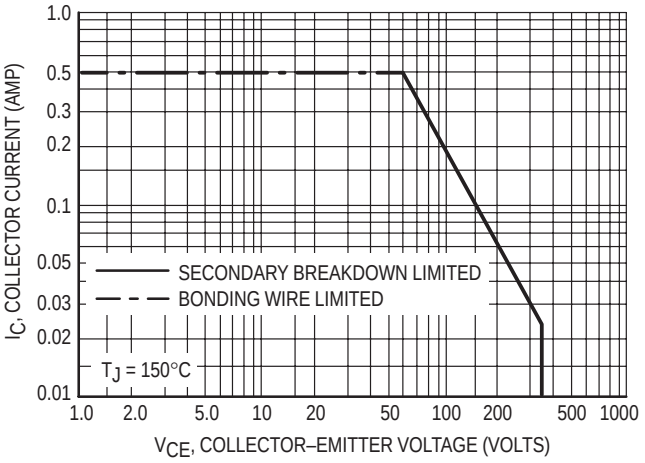


Figure 2. DC Safe Operating Area

The Safe Operating Area Curves indicate I_C – V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power–temperature derating must be observed for both steady state and pulse power conditions.

Complementary Silicon Plastic Power Transistors

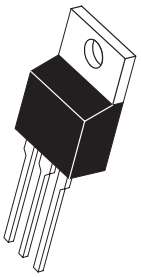
. . . designed for use in general–purpose amplifier and switching applications.

- DC Current Gain Specified to 10 Amperes
- High Current Gain — Bandwidth Product — f_T = 2.0 MHz (Min) @ I_C = 500 mAdc

PNP
MJE2955T*
NPN
MJE3055T*

*Motorola Preferred Device

10 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
60 VOLTS
75 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	60	Vdc
Collector–Base Voltage	V_{CB}	70	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	10	Adc
Base Current	I_B	6.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C MJE3055T, MJE2955T	P_D†	75 0.6	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.67	°C/W

†Safe Area Curves are indicated by Figure 1. Both limits are applicable and must be observed.

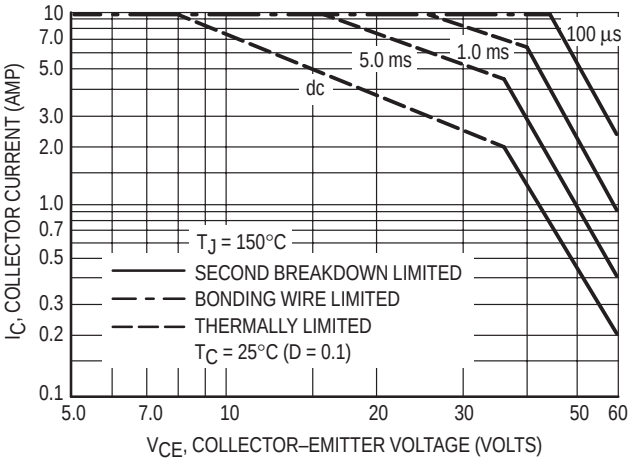


Figure 1. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_{J(pk)}$ = 150°C. T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN415A)

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	700	μAdc
Collector Cutoff Current (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 70 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	 — —	 1.0 5.0	mAdc
Collector Cutoff Current (V_{CB} = 70 Vdc, I_E = 0) (V_{CB} = 70 Vdc, I_E = 0, T_C = 150°C)	I_{CBO}	 — —	 1.0 10	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS				
DC Current Gain (1) (I_C = 4.0 Adc, V_{CE} = 4 0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	 20 5.0	 100 —	—
Collector–Emitter Saturation Voltage (1) (I_C = 4.0 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	 — —	 1.1 8.0	Vdc
Base–Emitter On Voltage (1) (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain–Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 500 kHz)	f_T	2.0	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 20%.

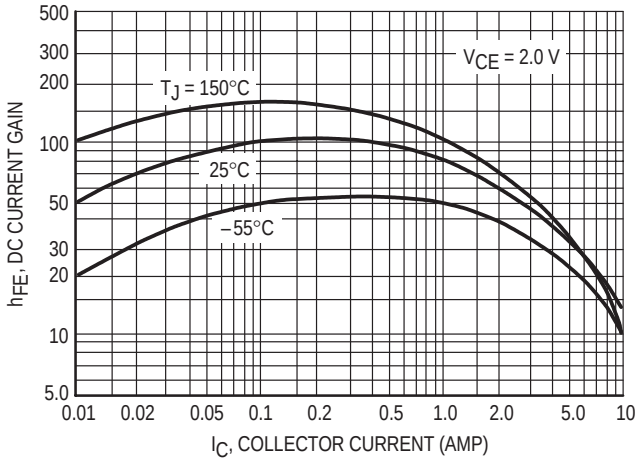


Figure 2. DC Current Gain

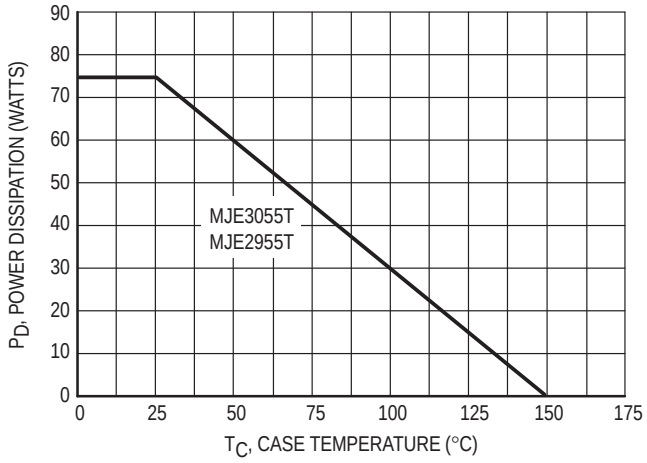
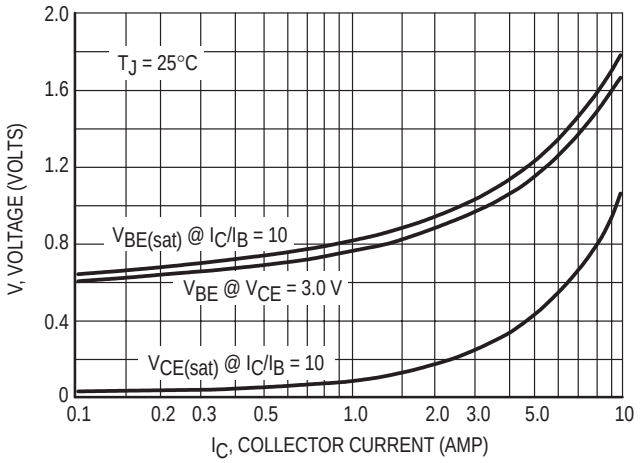


Figure 3. Power Derating

MJE2955T



MJE3055T

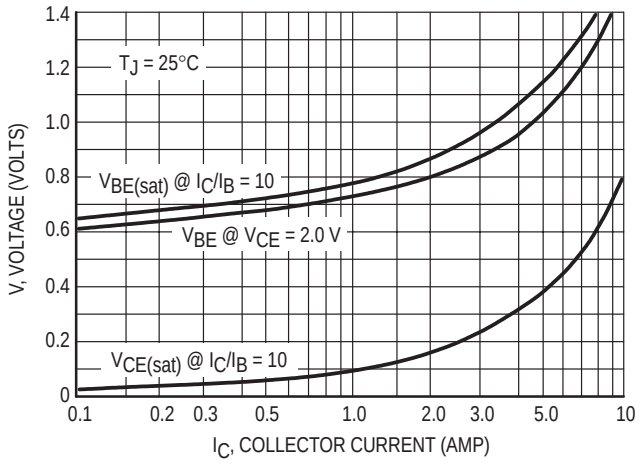


Figure 4. "On" Voltages

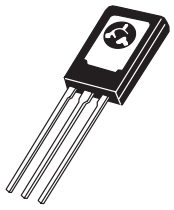
MJE3439

NPN Silicon High-Voltage Power Transistors

0.3 AMPERE
POWER TRANSISTOR
NPN SILICON
350 VOLTS
15 WATTS

. . . designed for use in line–operated equipment requiring high f_T.

- High DC Current Gain
  h_{FE} = 40–160 @ I_C = 20 mAdc
- Current Gain Bandwidth Product —
  f_T = 15 MHz (Min) @ I_C = 10 mAdc
- Low Output Capacitance
  C_{ob} = 10 pF (Max) @ f = 1.0 MHz



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	350	Vdc
Collector–Base Voltage	V_{CB}	450	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous	I_C	0.3	Adc
Base Current	I_B	150	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	8.33	°C/W

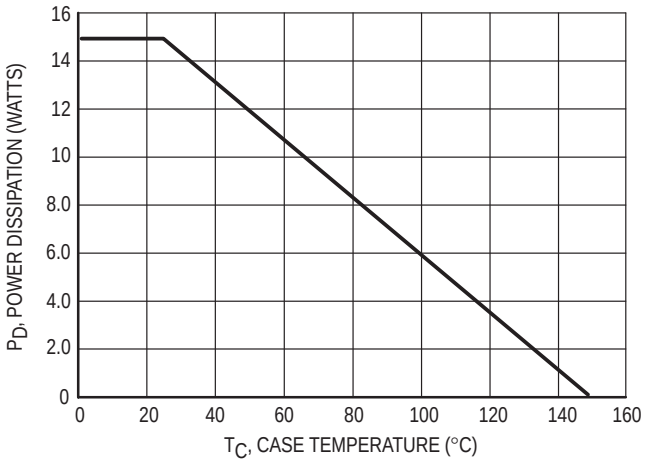


Figure 1. Power–Temperature Derating Curve

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (I_C = 5.0 mAdc, I_B = 0)	$V_{CEO(sus)}$	350	—	Vdc
Collector Cutoff Current (V_{CE} = 300 Vdc, I_B = 0)	I_{CEO}	—	20	μAdc
Collector Cutoff Current (V_{CE} = 450 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	I_{CEX}	—	500	μAdc
Collector Cutoff Current (V_{CB} = 350 Vdc, I_E = 0)	I_{CBO}	—	20	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	20	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 2.0 mAdc, V_{CE} = 10 Vdc) (I_C = 20 mAdc, V_{CE} = 10 Vdc)	h_{FE}	30 15	— 200	—
Collector–Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 4.0 mAdc)	$V_{CE(sat)}$	—	0.5	Vdc
Base–Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 4.0 mAdc)	$V_{BE(sat)}$	—	1.3	Vdc
Base–Emitter On Voltage (I_C = 50 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	—	0.8	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 5.0 MHz)	f_T	15	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}	—	10	pF
Small–Signal Current Gain (I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	h_{fe}	25	—	—

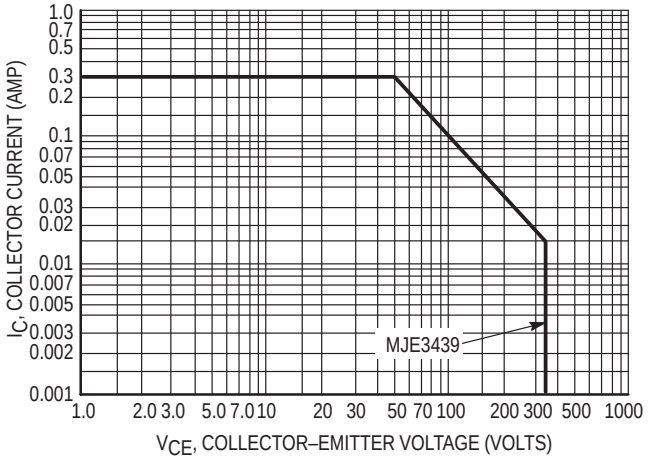


Figure 2. Active–Region Safe Operating Area

The Safe Operating Area Curves indicate I_C – V_{CE} limits below which the device will not enter secondary breakdown. Collector load lines for specific circuits must fall within the applicable Safe Area to avoid causing a catastrophic failure. To insure operation below the maximum T_J, power–temperature derating must be observed for both steady state and pulse power conditions.

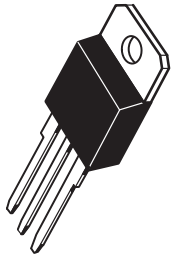
NPN
MJE4342
MJE4343
PNP
MJE4352
MJE4353

16 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
140–160 VOLTS

High-Voltage — High Power Transistors

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector–Emitter Sustaining Voltage —
  NPN PNP
  $V_{CEO(sus)}$ = 140 Vdc — MJE4342 MJE4352
  = 160 Vdc — MJE4343 MJE4353
- High DC Current Gain — @ I_C = 8.0 Adc
  h_{FE} = 35 (Typ)
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 8.0 Adc



CASE 340D–01
TO–218 TYPE

MAXIMUM RATINGS

Rating	Symbol	MJE4342 MJE4352	MJE4343 MJE4353	Unit
Collector–Emitter Voltage	V_{CEO}	140	160	Vdc
Collector–Base Voltage	V_{CB}	140	160	Vdc
Emitter–Base Voltage	V_{EB}	7.0		Vdc
Collector Current — Continuous Peak (1)	I_C	16 20		Adc
Base Current — Continuous	I_B	5.0		Adc
Total Power Dissipation @ T_C = 25°C	P_D	125		Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

(1) Pulse Test: Pulse Width ≤ 5.0 μs, Duty Cycle ≥ 10%.

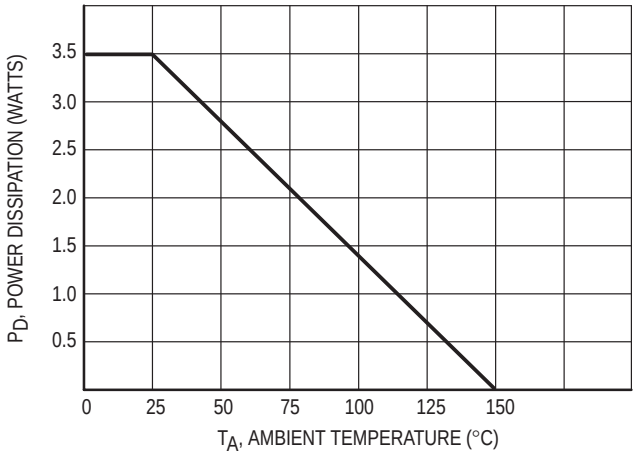


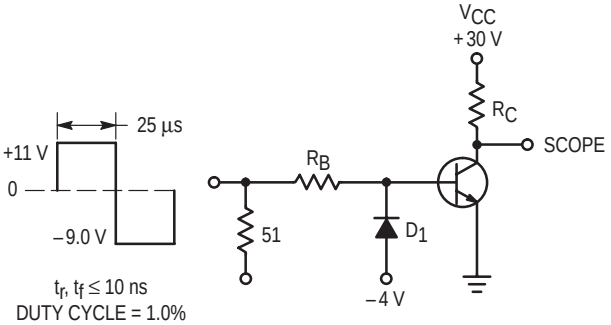
Figure 1. Power Derating
Reference: Ambient Temperature

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	MJE4342, MJE4352 MJE4343, MJE4353	$V_{CEO(sus)}$	140 160	— —	Vdc
Collector–Emitter Cutoff Current (V_{CE} = 70 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0	 MJE4342, MJE4352 MJE4343, MJE4353	I_{CEO}	— —	750 750	μAdc
Collector–Emitter Cutoff Current (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	— —	1.0 5.0	mAdc
Collector–Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}	—	750	μAdc
Emitter–Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 16 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	 15 8.0	 35 (Typ) 15 (Typ)	—
Collector–Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 800 mA) (I_C = 16 Adc, I_B = 2.0 Adc)		$V_{CE(sat)}$	 — —	 2.0 3.5	Vdc
Base–Emitter Saturation Voltage (I_C = 16 Adc, I_B = 2.0 Adc)		$V_{BE(sat)}$	—	3.9	Vdc
Base–Emitter On Voltage (I_C = 16 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	3.9	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)		f_T	1.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	800	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≥ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

Note: Reverse polarities to test PNP devices.

Figure 2. Switching Times Test Circuit

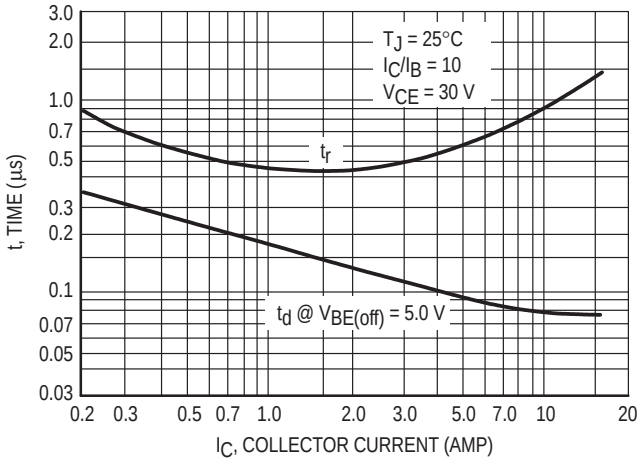


Figure 3. Typical Turn–On Time

TYPICAL CHARACTERISTICS

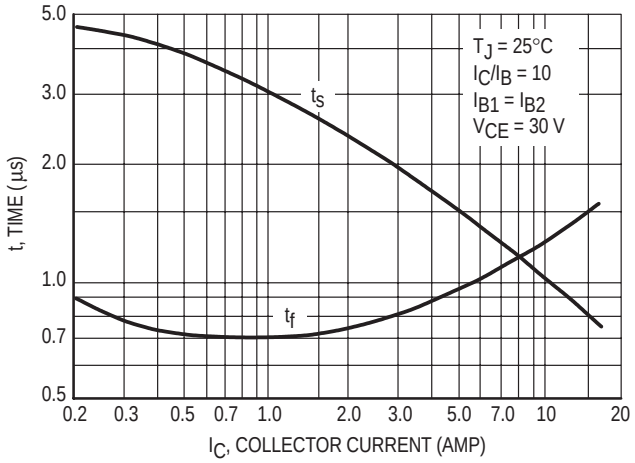


Figure 4. Turn–Off Time

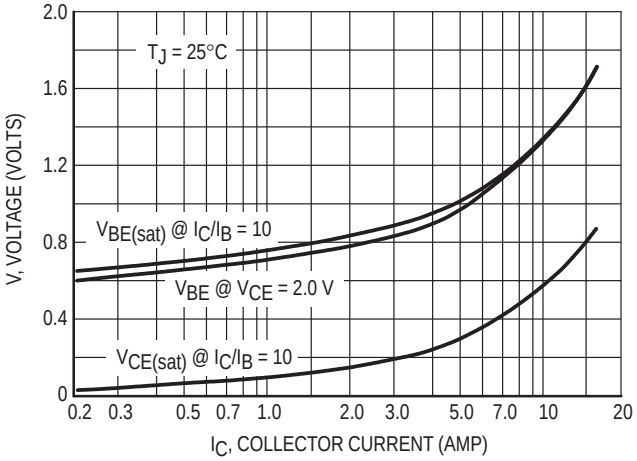


Figure 5. On Voltages

DC CURRENT GAIN

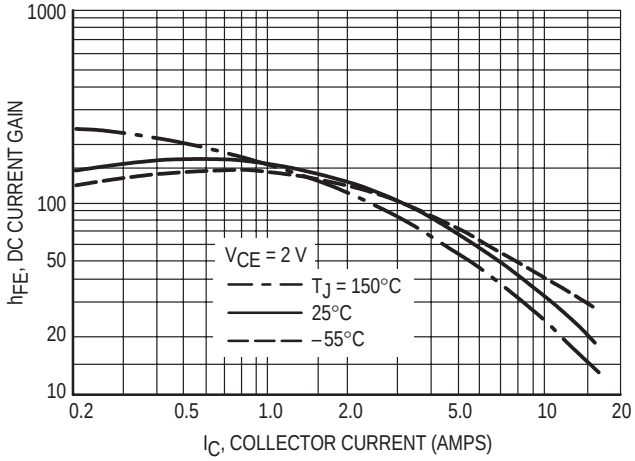


Figure 6. MJE4340 Series (NPN)

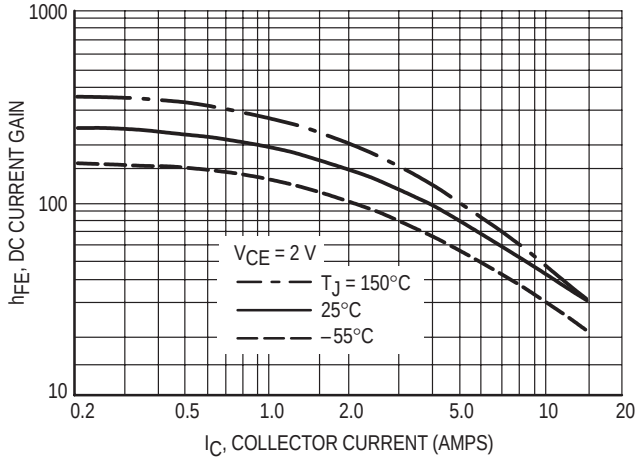


Figure 7. MJE4350 Series (PNP)

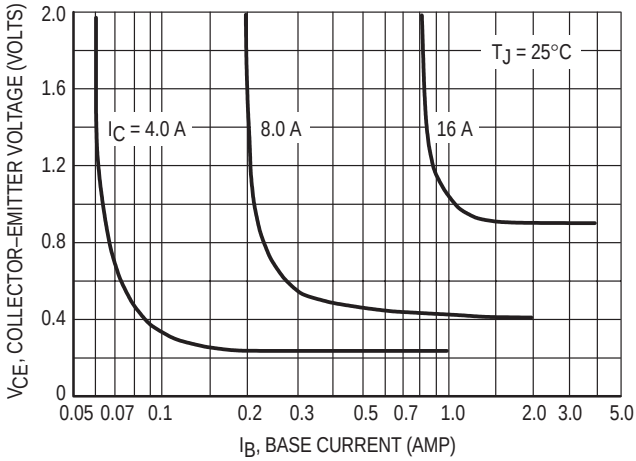


Figure 8. Collector Saturation Region

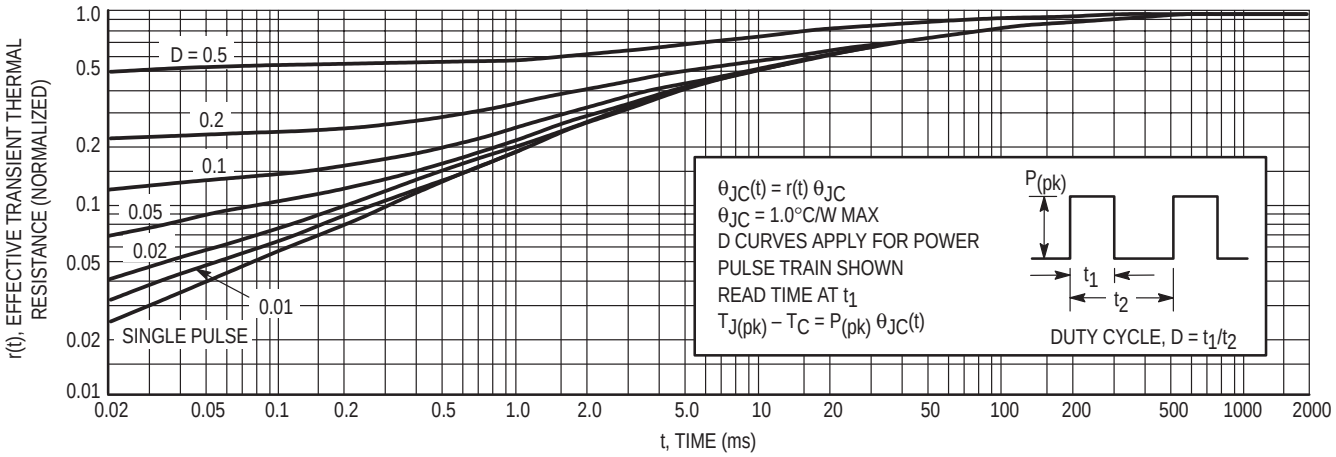


Figure 9. Thermal Response

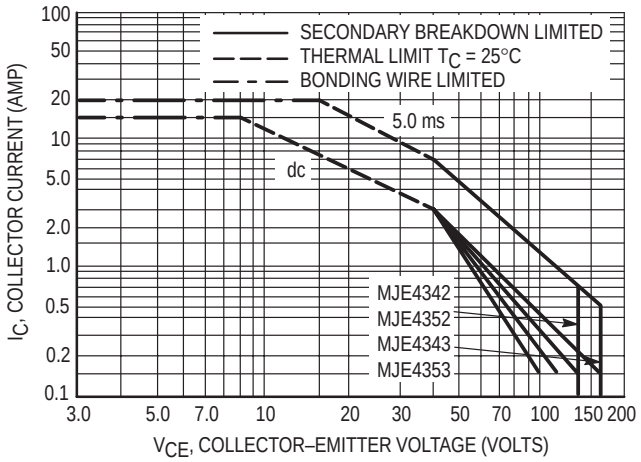


Figure 10. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 9.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 11 gives RBSOA characteristics.

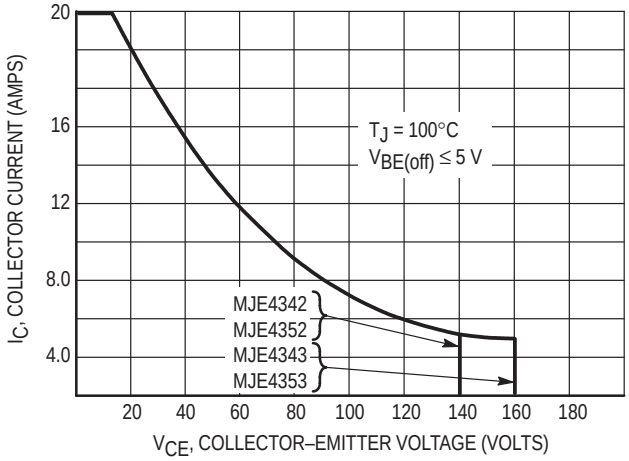


Figure 11. Maximum Reverse Bias Safe Operating Area

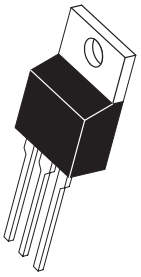
MJE5730
MJE5731
MJE5731A

High Voltage PNP Silicon Power Transistors

. . . designed for line operated audio output amplifier, SWITCHMODE power supply drivers and other switching applications.

- 300 V to 400 V (Min) — $V_{CEO(sus)}$
- 1.0 A Rated Collector Current
- Popular TO–220 Plastic Package
- PNP Complements to the TIP47 thru TIP50 Series

1.0 AMPERE
POWER TRANSISTORS
PNP SILICON
300 – 350 – 400 VOLTS
40 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	MJE5730	MJE5731	MJE5731A	Unit
Collector–Emitter Voltage	V_{CEO}	300	350	400	Vdc
Collector–Base Voltage	V_{CB}	300	350	400	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	1.0 3.0			Adc
Base Current	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 40 0.32			 Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	 2.0 0.016			 Watts W/°C
Unclamped Inducting Load Energy (See Figure 10)	E	20			mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	MJE5730 MJE5731 MJE5732	$V_{CEO(sus)}$	 300 350 400	 — — —	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0) (V_{CE} = 250 Vdc, I_B = 0) (V_{CE} = 300 Vdc, I_B = 0)	 MJE5730 MJE5731 MJE5732	I_{CEO}	 — — —	 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 300 Vdc, V_{BE} = 0) (V_{CE} = 350 Vdc, V_{BE} = 0) (V_{CE} = 400 Vdc, V_{BE} = 0)	 MJE5730 MJE5731 MJE5732	I_{CES}	 — — —	 1.0 1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc) (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		h_{FE}	 30 10	 150 —	—
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.2 Adc)		$V_{CE(sat)}$	—	1.0	Vdc
Base–Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 10 Vdc)		$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 2.0 MHz)		f_T	10	—	MHz
Small–Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	25	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

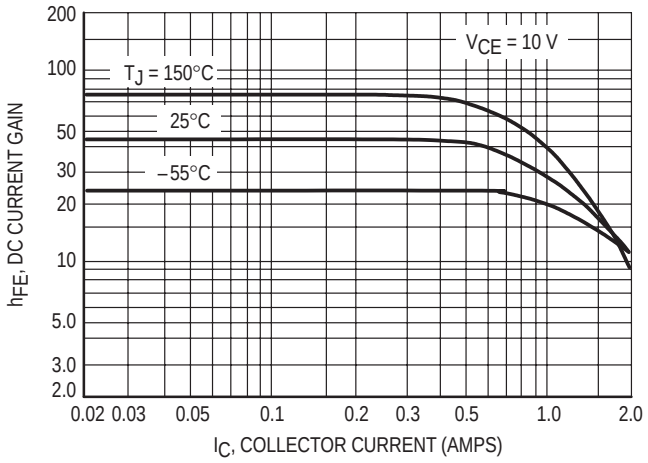


Figure 1. DC Current Gain

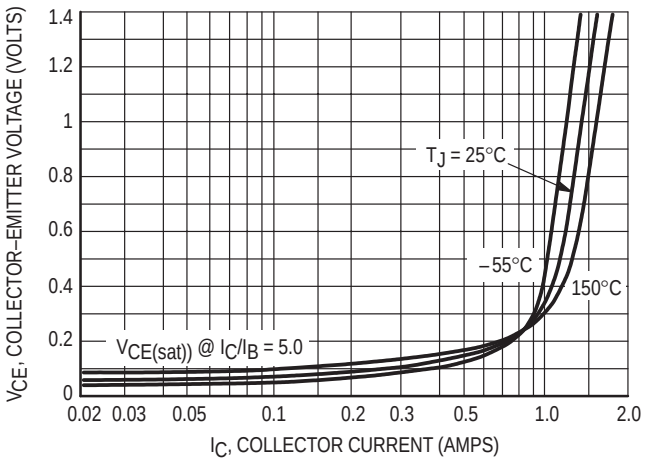


Figure 2. Collector–Emitter Saturation Voltage

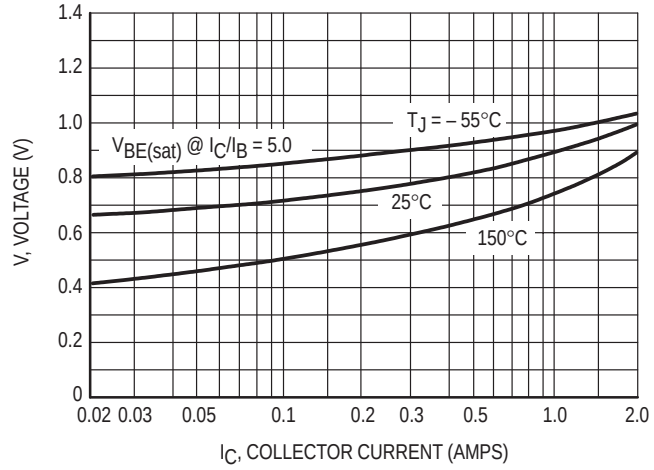


Figure 3. Base–Emitter Voltage

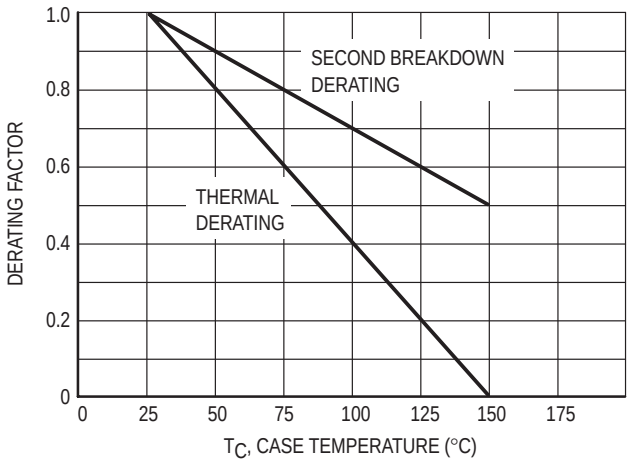


Figure 4. Normalized Power Derating

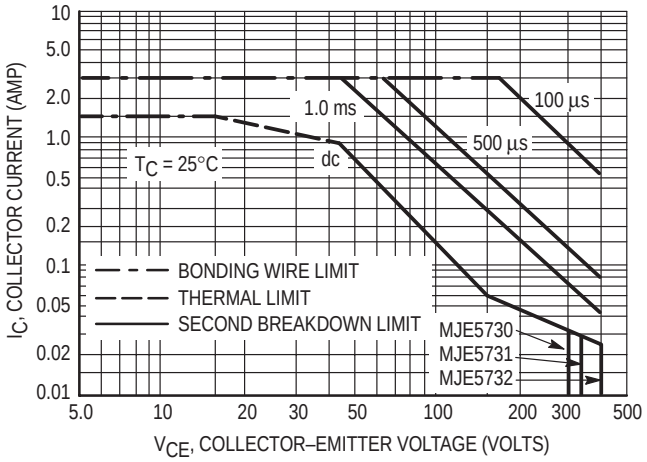


Figure 5. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

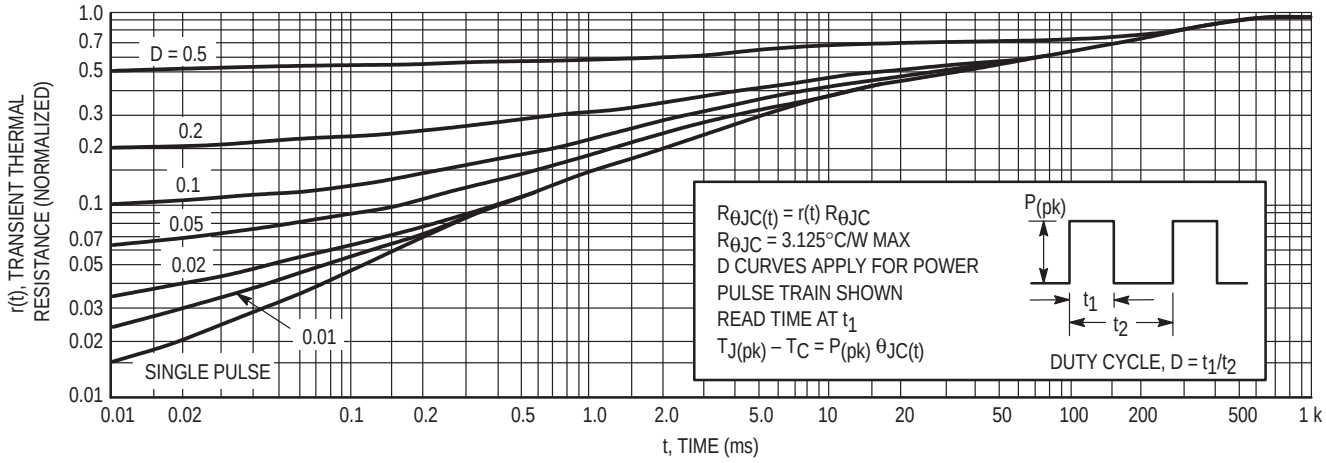


Figure 6. Thermal Response

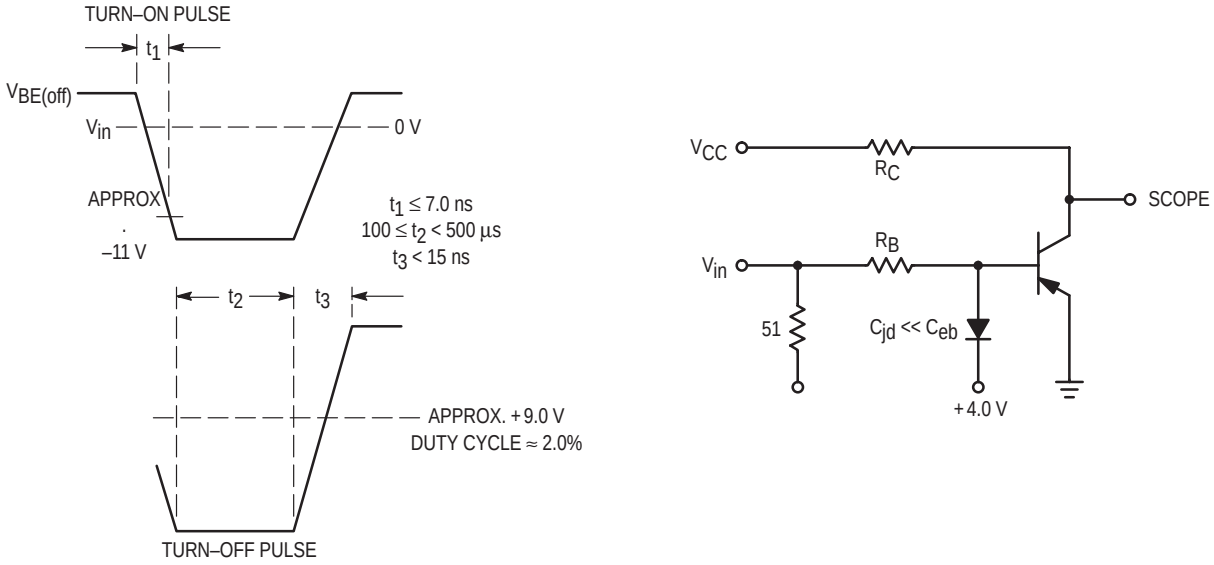


Figure 7. Switching Time Equivalent Circuit

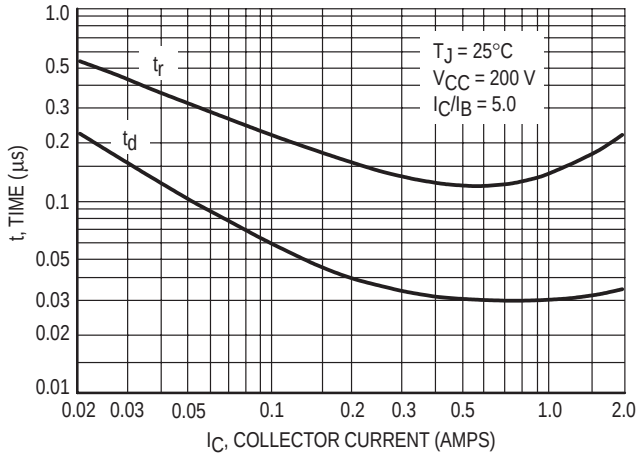


Figure 8. Turn–On Resistive Switching Times

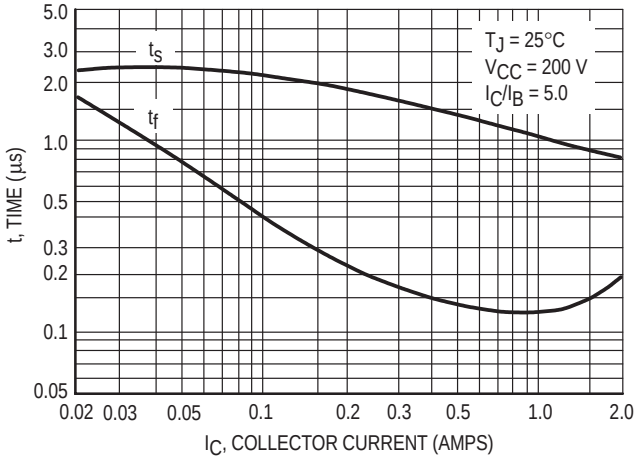
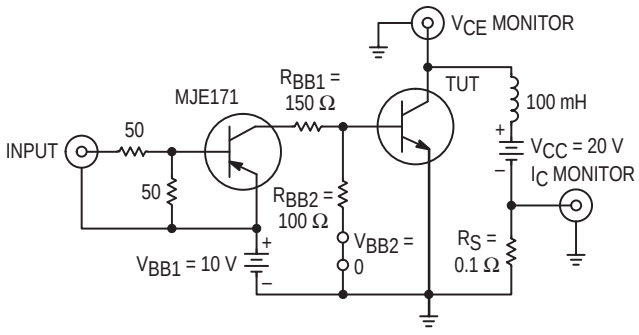


Figure 9. Resistive Turn–Off Switching Times

Test Circuit



Voltage and Current Waveforms

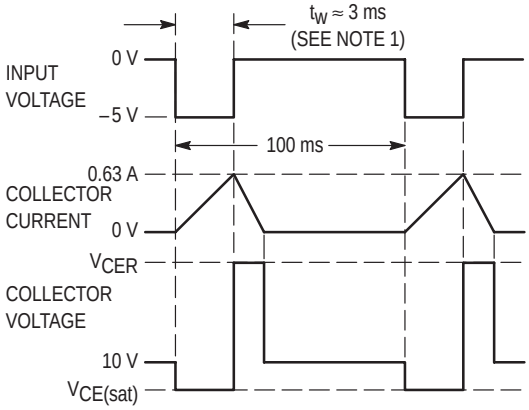


Figure 10. Inductive Load Switching

NPN Silicon Power Darlington Transistors

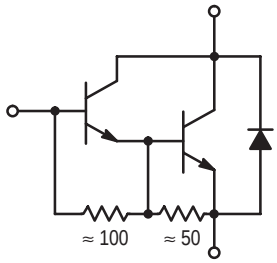
MJE5740
MJE5741*
MJE5742*

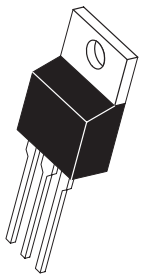
*Motorola Preferred Device

The MJE5740, 41, 42 Darlington transistors are designed for high–voltage power switching in inductive circuits. They are particularly suited for operation in applications such as:

- Small Engine Ignition
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls

POWER DARLINGTON TRANSISTORS
8 AMPERES
300, 350, 400 VOLTS
80 WATTS





CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	MJE5740	MJE5741	MJE5742	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	300	350	400	Vdc
Collector–Emitter Voltage	V_{CEV}	600	700	800	Vdc
Emitter Base Voltage	V_{EB}	8			Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8 16			Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5			Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 16			Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 640			Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle = 10%.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)						
Collector–Emitter Sustaining Voltage (I_C = 50 mA, I_B = 0)	MJE5740 MJE5741 MJE5742	$V_{CEO(sus)}$	300 350 400	— — —	— — —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	— —	— —	1 5	mAdc
Emitter Cutoff Current (V_{EB} = 8 Vdc, I_C = 0)		I_{EBO}	—	—	75	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 6			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 7			

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

(continued)

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5 Vdc) (I_C = 4 Adc, V_{CE} = 5 Vdc)		h_{FE}	50 200	100 400	— —	—
Collector–Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.2 Adc) (I_C = 8 Adc, I_B = 0.4 Adc) (I_C = 4 Adc, I_B = 0.2 Adc, T_C = 100°C)		$V_{CE(sat)}$	— — —	— — —	2 3 2.2	Vdc
Base–Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.2 Adc) (I_C = 8 Adc, I_B = 0.4 Adc) (I_C = 4 Adc, I_B = 0.2 Adc, T_C = 100°C)		$V_{BE(sat)}$	— — —	— — —	2.5 3.5 2.4	Vdc
Diode Forward Voltage (2) (I_F = 5 Adc)		V_f	—	—	2.5	Vdc
SWITCHING CHARACTERISTICS						
Typical Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, $I_{C(pk)}$ = 6 A I_{B1} = I_{B2} = 0.25 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	—	0.04	—	μs
Rise Time		t_r	—	0.5	—	μs
Storage Time		t_s	—	8	—	μs
Fall Time		t_f	—	2	—	μs
Inductive Load, Clamped (Table 1)						
Voltage Storage Time	($I_{C(nk)}$ = 6 A, $V_{CE(nk)}$ = 250 Vdc I_{B1} = 0.06 A, $V_{BE(off)}$ = 5 Vdc)	t_{sv}	—	4	—	μs
Crossover Time		t_c	—	2	—	μs

(1) Pulse Test: Pulse Width 300 μs, Duty Cycle = 2%.

(2) The internal Collector–to–Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

TYPICAL CHARACTERISTICS

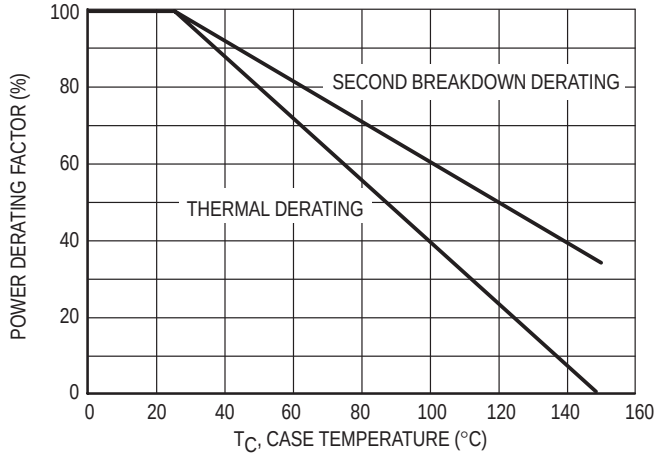


Figure 1. Power Derating

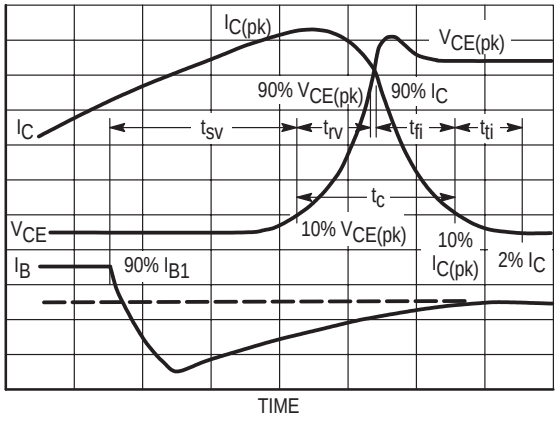


Figure 2. Inductive Switching Measurements

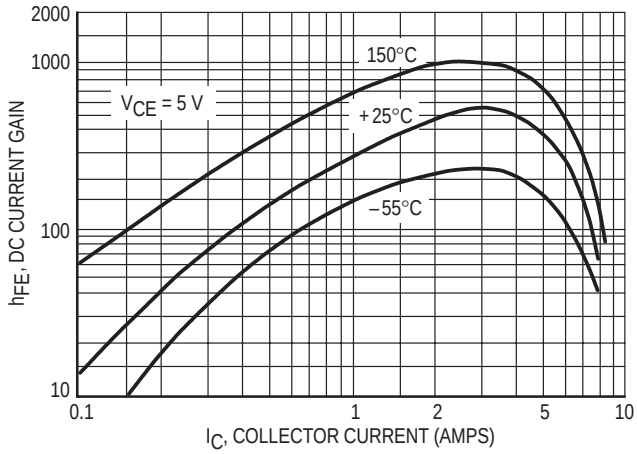


Figure 3. DC Current Gain

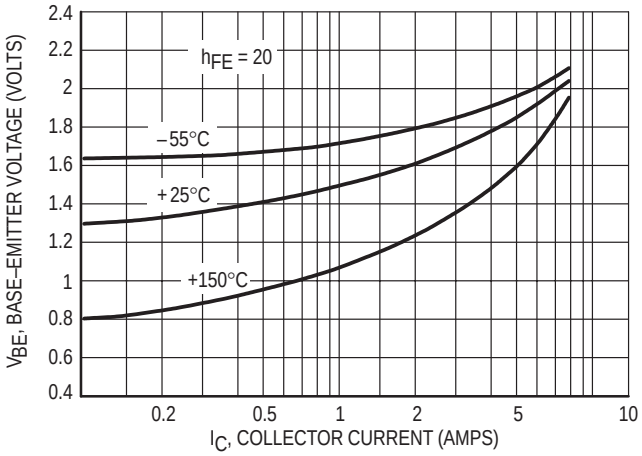
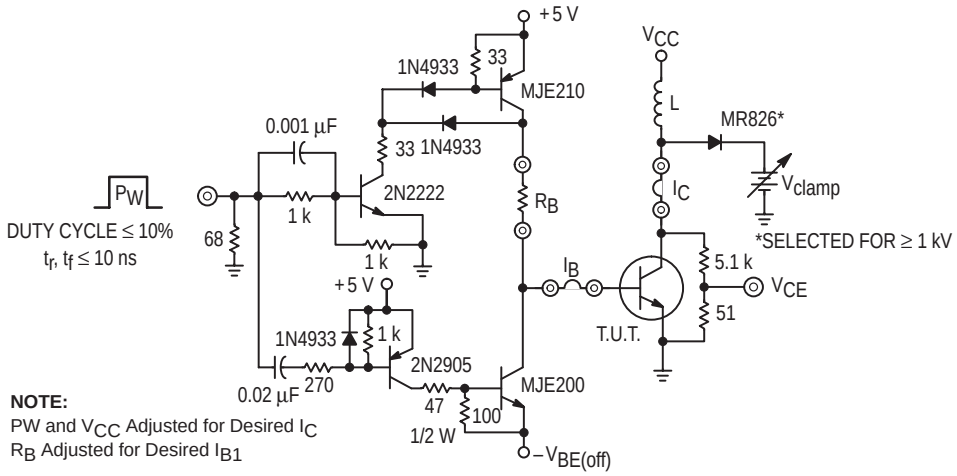
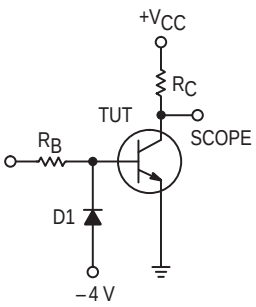
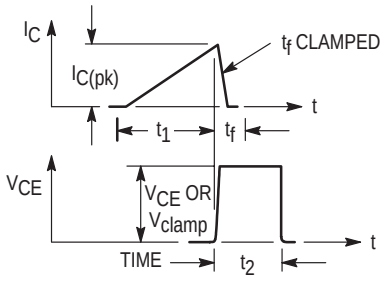
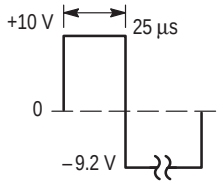


Figure 4. Base–Emitter Voltage

Table 1. Test Conditions for Dynamic Performance

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	COIL DATA: FERROXCUBE CORE #6656 FULL BOBBIN (~16 TURNS) #16 GAP FOR 200 µH/20 A L_{coil} = 200 µH V_{CC} = 30 V $V_{CE(pk)}$ = 250 Vdc $I_{C(pk)}$ = 6 A	V_{CC} = 250 V D1 = 1N5820 OR EQUIV.
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 ADJUSTED TO OBTAIN I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ TEST EQUIPMENT SCOPE–TEKTRONICS 475 OR EQUIVALENT	 t_r, t_f < 10 ns DUTY CYCLE = 1% R_B AND R_C ADJUSTED FOR DESIRED I_B AND I_C

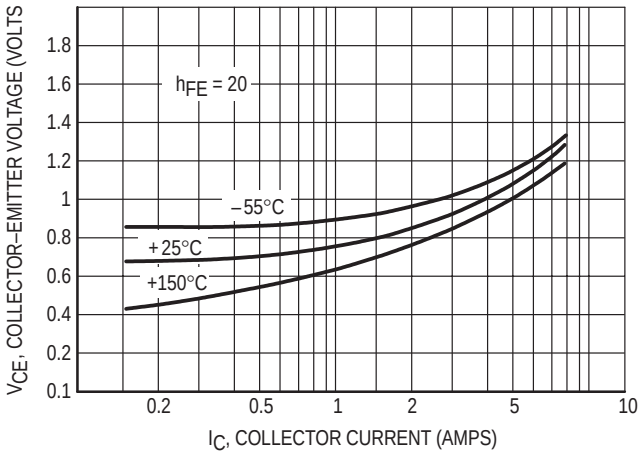


Figure 5. Inductive Switching Measurements

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 6 may be found at any case temperature by using the appropriate curve on Figure 1.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives the complete RBSOA characteristics.

The Safe Operating Area figures shown in Figures 6 and 7 are specified ratings for these devices under the test conditions shown.

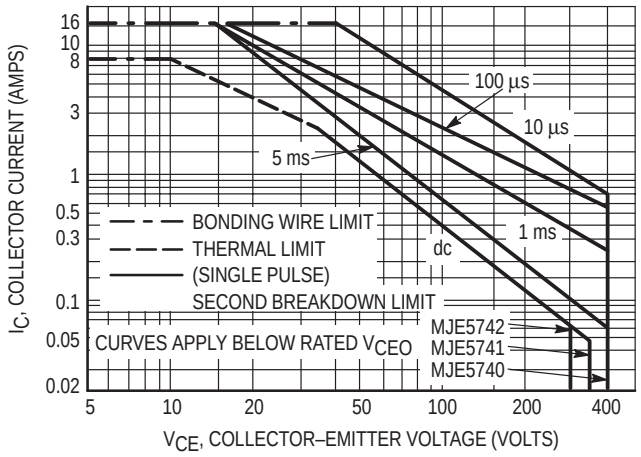


Figure 6. Forward Bias Safe Operating Area

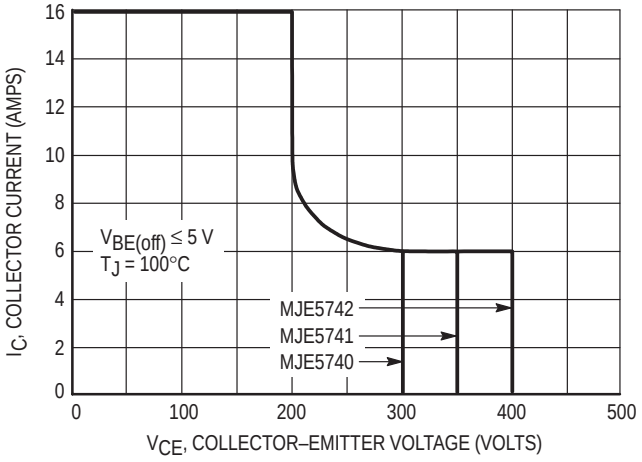


Figure 7. Reverse Bias Safe Operating Area

RESISTIVE SWITCHING PERFORMANCE

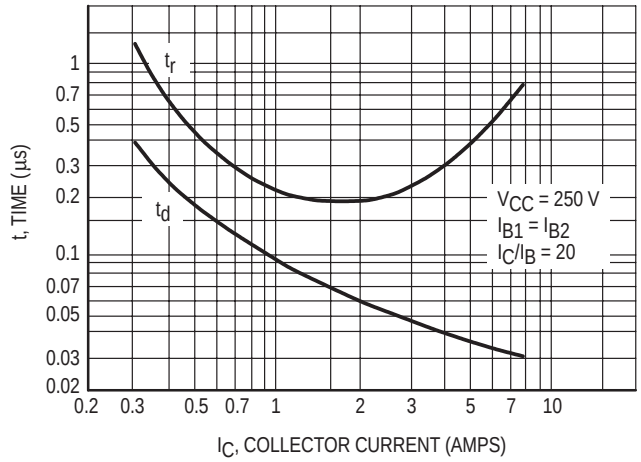


Figure 8. Turn–On Time

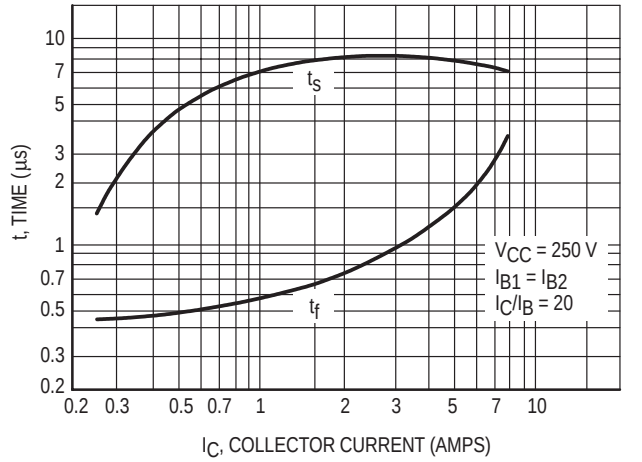


Figure 9. Turn–Off Time

MJE5850
MJE5851*
MJE5852*

*Motorola Preferred Device

Designer's™ Data Sheet

SWITCHMODE Series
PNP Silicon Power Transistors

8 AMPERE
PNP SILICON
POWER TRANSISTORS
300, 350, 400 VOLTS
80 WATTS

The MJE5850, MJE5851 and the MJE5852 transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

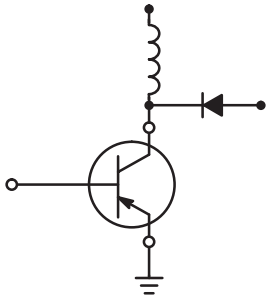
Fast Turn–Off Times

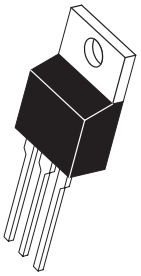
100 ns Inductive Fall Time @ 25°C (Typ)
125 ns Inductive Crossover Time @ 25°C (Typ)

Operating Temperature Range –65 to +150°C

100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents





CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	MJE5850	MJE5851	MJE5852	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	300	350	400	Vdc
Collector–Emitter Voltage	V_{CEV}	350	400	450	Vdc
Emitter Base Voltage	V_{EB}	6.0			Vdc
Collector Current — Continuous Peak (1)	I_C I_{CM}	8.0 1 6			Adc
Base Current — Continuous Peak (1)	I_B I_{BM}	4.0 8.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.640			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to 150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	MJE5850 MJE5851 MJE5852	$V_{CEO(sus)}$	300 350 400	 — —	 — —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	 — —	 — —	 0.5 2.5	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 12			
Clamped Inductive SOA with base reverse biased		RBSOA	See Figure 13			
***ON CHARACTERISTICS**						
DC Current Gain (I_C = 2.0 Adc, V_{CE} = 5 Vdc) (I_C = 5.0 Adc, V_{CE} = 5 Vdc)		h_{FE}	 15 5	 — —	 — —	—
Collector–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 1.0 Adc) (I_C = 8.0 Adc, I_B = 3.0 Adc) (I_C = 4.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{CE(sat)}$	 — — —	 — — —	 2.0 5.0 2.5	Vdc
Base–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 1.0 Adc) (I_C = 4.0 Adc, I_B = 1.0 Adc, T_C = 100°C)		$V_{BE(sat)}$	 — —	 — —	 1.5 1.5	Vdc
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	—	270	—	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, t_p = 50 μs, Duty Cycle ≤ 2%)	t_d	—	0.025	0.1	μs
Rise Time		t_r	—	0.100	0.5	μs
Storage Time	(V_{CC} = 250 Vdc, I_C = 4.0 A, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%)	t_s	—	0.60	2.0	μs
Fall Time		t_f	—	0.11	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_{CM} = 4 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	0.8	3.0	μs
Crossover Time		t_c	—	0.4	1.5	μs
Fall Time		t_{fi}	—	0.1	—	μs
Storage Time	(I_{CM} = 4 A, V_{CEM} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	—	0.5	—	μs
Crossover Time		t_c	—	0.125	—	μs
Fall Time		t_{fi}	—	0.1	—	μs

* Pulse Test: PW = 300 μs. Duty Cycle ≤ 2%

TYPICAL ELECTRICAL CHARACTERISTICS

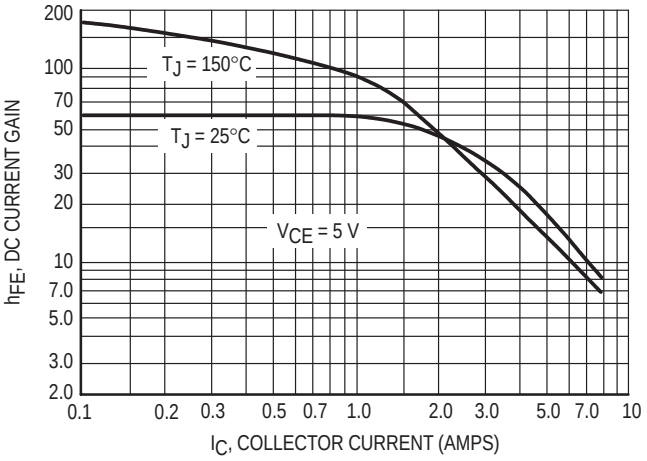


Figure 1. DC Current Gain

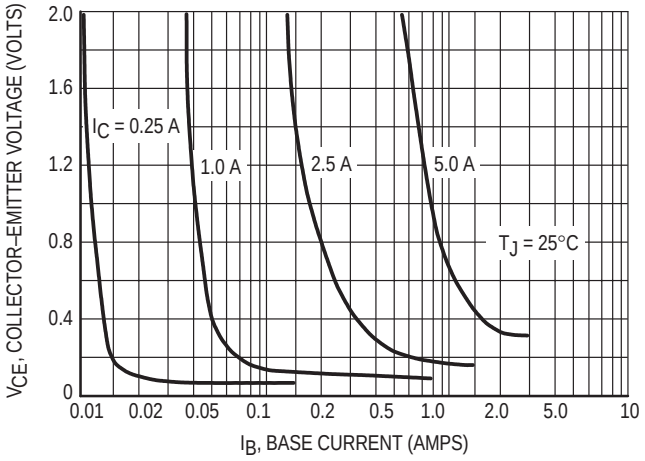


Figure 2. Collector Saturation Region

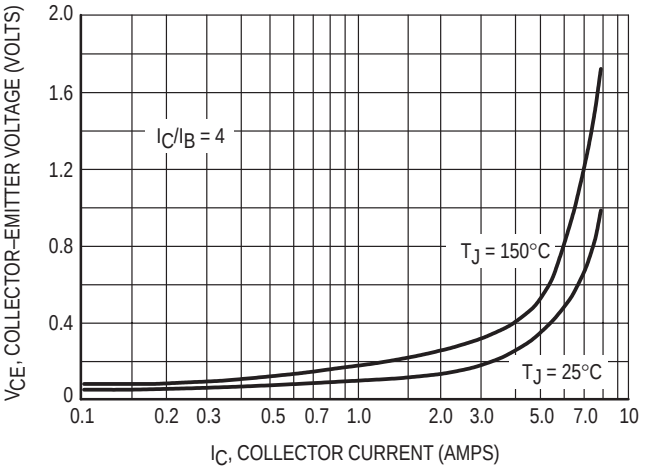


Figure 3. Collector–Emitter Saturation Voltage

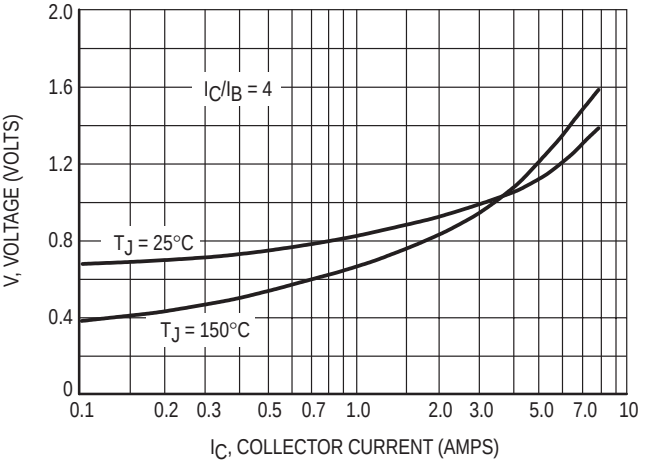


Figure 4. Base–Emitter Voltage

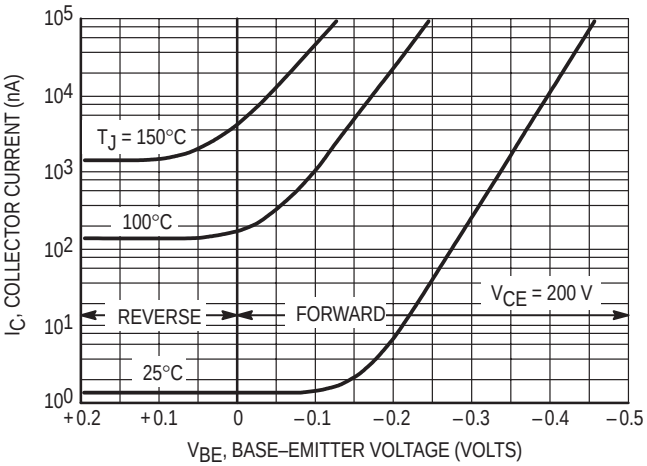


Figure 5. Collector Cutoff Region

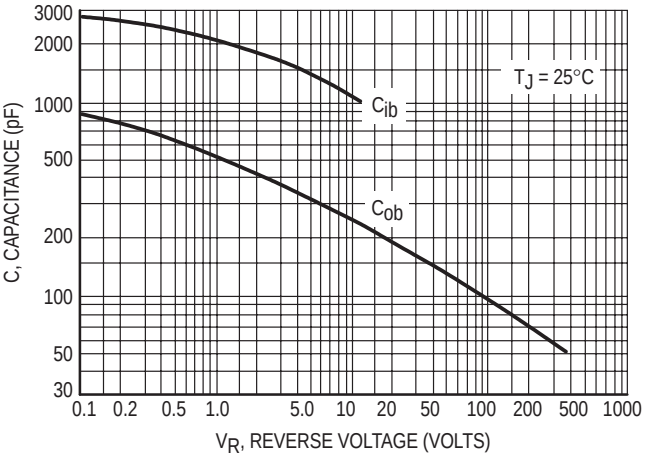


Figure 6. Capacitance

Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	–10 V, 20, 1, 0, 2 PW Varied to Attain I_C = 100 mA	+ V, 50 µF, 0.0025 µF, 0.2 µF, 500 Ω 1/2 W, MJE15029, 0.1 µF, 1N4934, INPUT, 0.1 µF, 500 Ω 1/2 W, 0.0033 µF, 1 Ω 2 W, MJE15028, 50 Ω 2 W, 0.2 µF, 50 µF, – V – V adjusted to obtain desired I_{B1} + V adjusted to obtain desired $V_{BE(off)}$	TURN–ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN–OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 62 Ω Pulse Width = 10 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT TUT, 1, INPUT, 1N4937 OR EQUIVALENT, R_{coil}, L_{coil}, SEE ABOVE FOR DETAILED CONDITIONS, V_{clamp}, V_{CC}, RS = 0.1 Ω OUTPUT WAVEFORMS I_C, I_{CM}, t_f Clamped, t_1, t_f, V_{CE}, V_{CEM}, V_{clamp}, TIME, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent		RESISTIVE TEST CIRCUIT TUT, 1, 2, R_L, V_{CC}

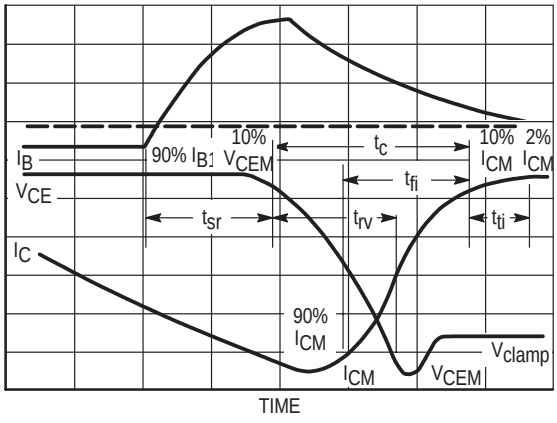


Figure 7. Inductive Switching Measurements

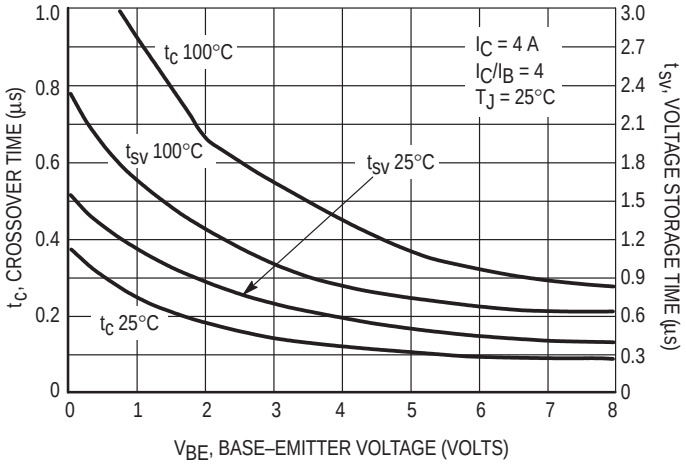


Figure 8. Inductive Switching Times

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
t_{rv} = Voltage Rise Time, 10–90% V_{CEM}
t_{fi} = Current Fall Time, 90–10% I_{CM}
t_{ti} = Current Tail, 10–2% I_{CM}
t_c = Crossover Time,10% V_{CEM} to 10% I_{CM}

An enlarged portion of the inductive switching waveform is shown in Figure 7 to aid on the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222A:

$$P_{SWT} = 1/2\ V_{CC} I_C(t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

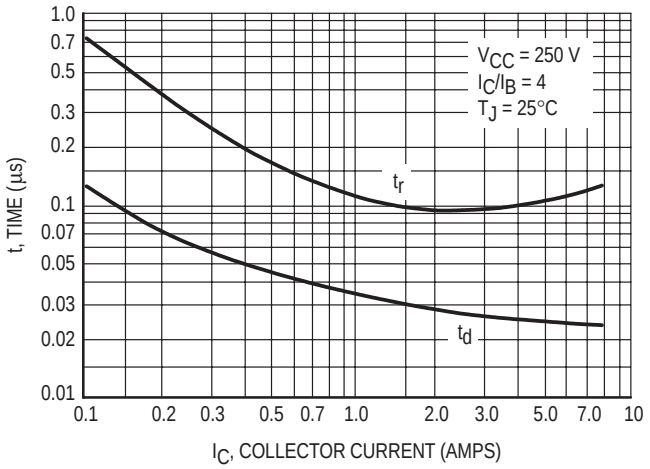


Figure 9. Turn–On Switching Times

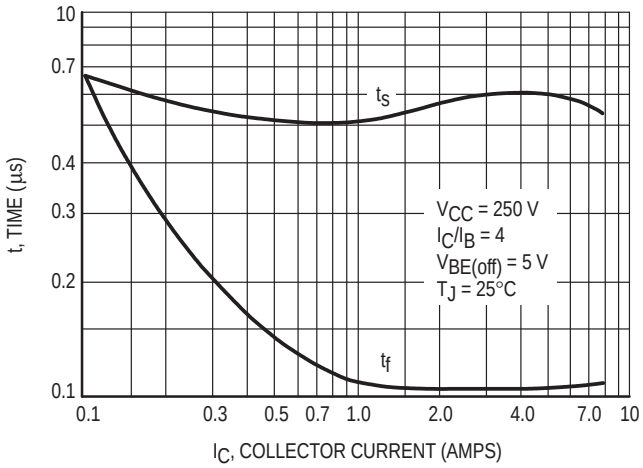


Figure 10. Turn–Off Switching Time

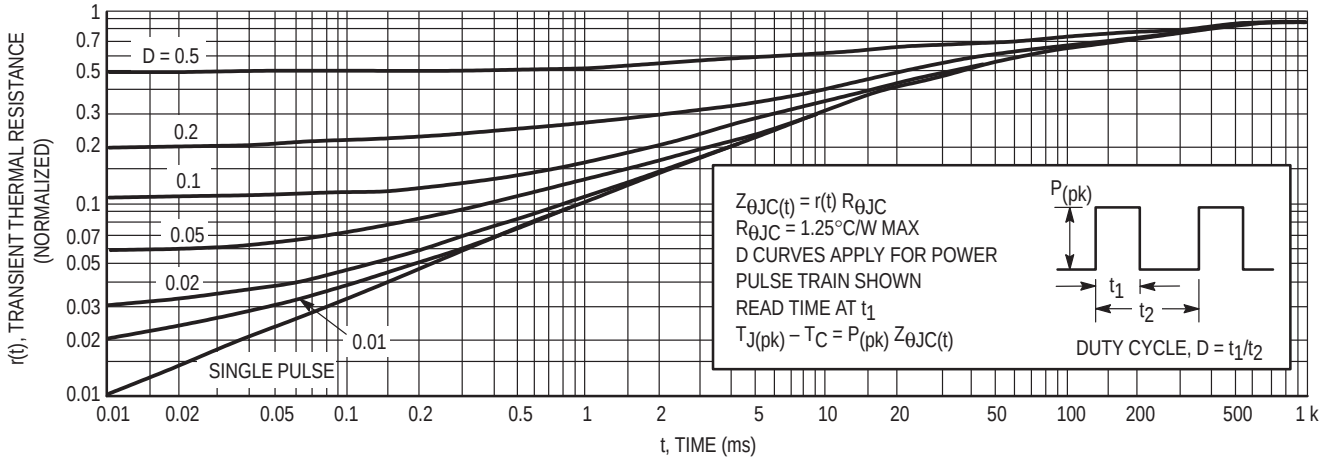


Figure 11. Typical Thermal Response [$Z_{\theta JC}(t)$]

The Safe Operating Area figures shown in Figures 12 and 13 are specified for these devices under the test conditions shown.

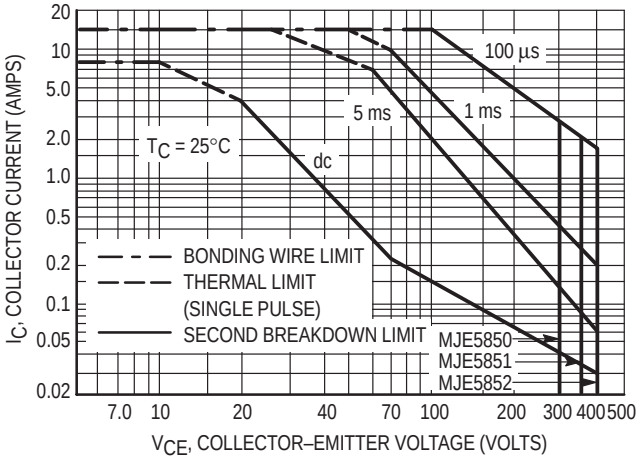


Figure 12. Maximum Forward Bias Safe Operating Area

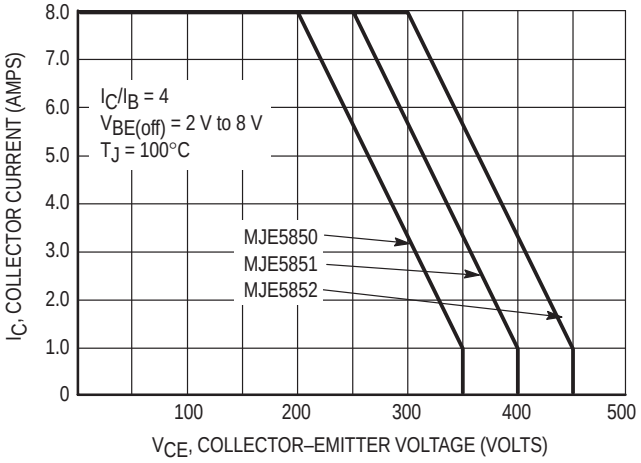


Figure 13. RBSOA, Maximum Reverse Bias Safe Operating Area

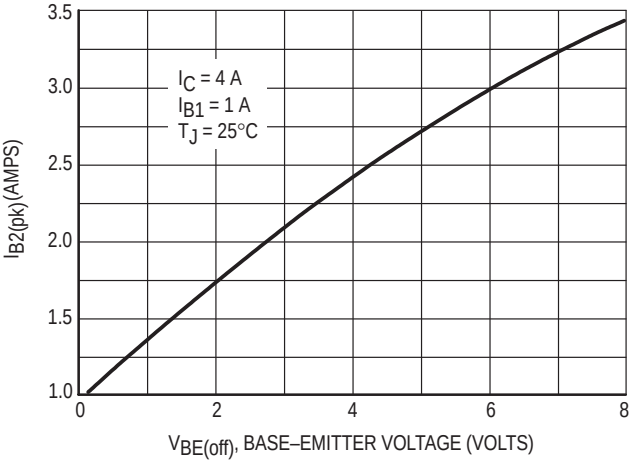


Figure 14. Peak Reverse Base Current

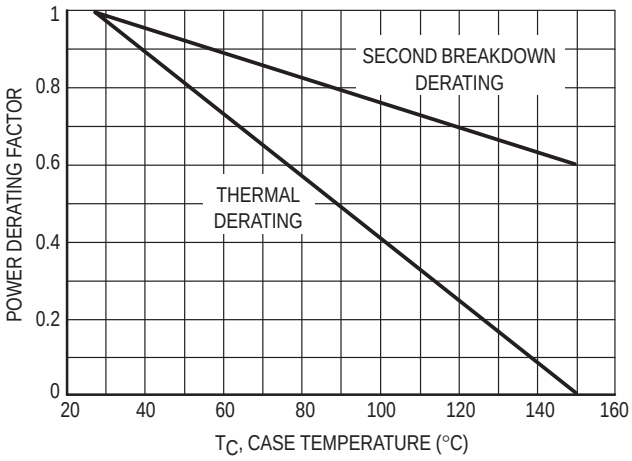


Figure 15. Forward Bias Power Derating

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the RBSOA characteristics.

MJE8503A*

*Motorola Preferred Device

Advance Information

SWITCHMODE™ Series

NPN Bipolar Power Transistor

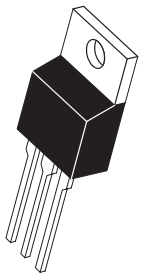
POWER TRANSISTORS
5.0 AMPERES
1500 VOLTS — BV_{CES}
80 WATTS

The MJE8503A transistor is designed for high voltage, high speed, power switching in inductive circuits where fall time is critical. They are suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits

Featuring

- 1500 Volt Collector-Base Breakdown Capability
- Fast Switching:
  - 180 ns Typical Fall Times
  - 450 ns Typical Crossover Times
  - 1.2 μs Typical Storage Times
- Low Collector-Emitter Leakage Current — 100 μA Max @ 1500 V_{CES}



CASE 221A–06
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	Vdc
Collector-Emitter Voltage	V_{CES}	1500	Vdc
Collector-Base Voltage	V_{CBO}	1500	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current — Continuous — Peak (1)	I_C	5.0 10	Adc
Collector Current — Continuous — Peak	I_B I_{BM}	4.0 4.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	80 21 0.8	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–65 to +125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 5 sec.	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle < 10%.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)		$V_{CEO(sus)}$	700	—	—	Vdc
Collector Cutoff Current		I_{CES}				mAdc
(V_{CE} = 1500 Vdc, V_{BE} = 0, T_C = 25°C)			—	—	0.1	
(V_{CE} = 1500 Vdc, V_{BE} = 0, T_C = 125°C)			—	—	2.0	
Collector Cutoff Current (V_{CE} = 1500 Vdc, R_{BE} = 50 Ohms, T_C = 100°C)		I_{CER}	—	—	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector with Base Forward Biased		$I_{S/b}$	See Figure 2			
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				—
(I_C = 1.0 Adc, V_{CE} = 5.0 Vdc)			7.5	—	—	
(I_C = 4.5 Adc, V_{CE} = 5.0 Vdc)			2.25	—	—	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 2.5 Adc, I_B = 1.0 Vdc)			—	—	1.5	
(I_C = 4.5 Adc, I_B = 2.0 Vdc)			—	—	1.5	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 2.5 Adc, I_B = 1.0 Vdc)			—	—	2.0	
(I_C = 4.5 Adc, I_B = 2.0 Vdc)			—	—	3.0	
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)		f_T	—	7.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 0.1 MHz)		C_{ob}	—	125	—	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(I_C = 2.5 Adc, I_B = 1.0 Adc, V_{CC} = 500 Vdc $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs)	t_d	—	0.06	0.2	μs
Rise Time		t_r	—	0.08	2.0	
Storage Time		t_s	—	1.2	4.0	
Fall Time		t_f	—	0.7	2.0	
Inductive Load (Table 1)						
Storage Time	(I_C = 2.5 Adc, I_B = 1.0 Adc, V_{clamp} = 500 Vdc $V_{BE(off)}$ = 5.0 Vdc, t_p = 50 μs)	t_{sv}	—	1.2	—	μs
Crossover Time		t_c	—	0.45	—	
Fall Time		t_{fi}	—	0.18	—	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%

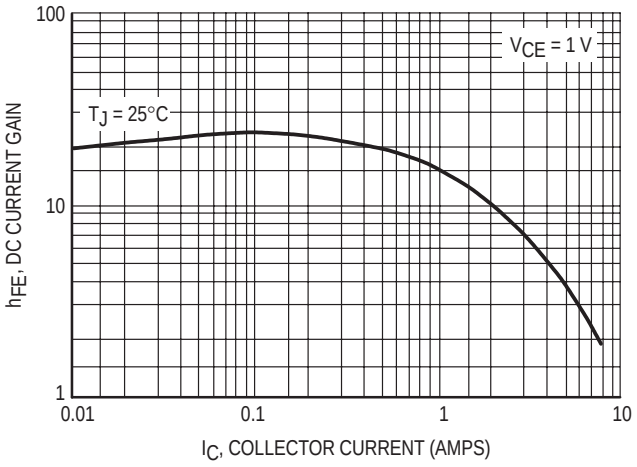


Figure 1. DC Current Gain

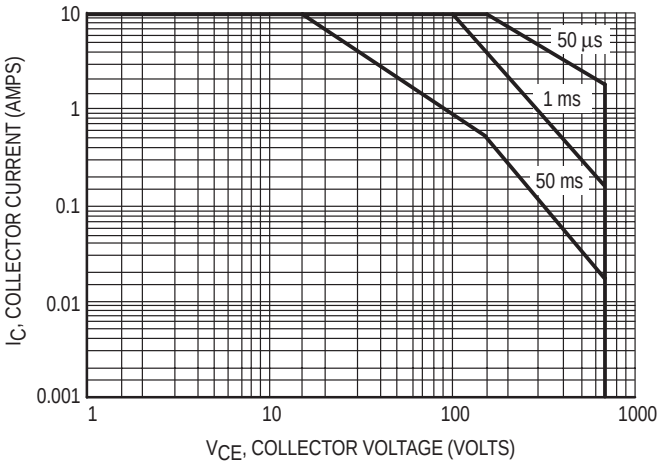


Figure 2. Forward Bias Safe Operating Area (FBSOA)

MJE9780*

*Motorola Preferred Device

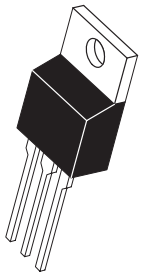
Advance Information

PNP Silicon Power Transistor

The MJE9780 is designed for vertical output of 14–inch to 17–inch televisions and CRT monitors, as well as other applications requiring a 150 volt PNP transistor. Features:

- Standard TO–220AB Package
- Gain Range of 50 – 200 at 500 mAdc/10 volts

PNP SILICON POWER TRANSISTOR
3.0 AMPERES
150 VOLTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	MJE9780	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	150	Vdc
Collector–Base Voltage	V_{CBO}	200	Vdc
Emitter–Base Voltage	V_{EBO}	6.0	Vdc
Collector Current — Continuous — Peak	I_C I_{CM}	3.0 5.0	Adc
Total Power Dissipation (T_A = 25°C) Derate above 25°C	P_D	2.0 0.016	Watts W/°C
Total Power Dissipation Derate above 25°C	P_D	40 0.32	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	– 55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS*					
Collector–Emitter Sustaining Voltage (I_C = 50 mA, I_B = 0)	$V_{CEO(sus)}$	150	—	—	Vdc
Collector–Base Voltage (I_C = 5.0 mAdc)	V_{CBO}	200	—	—	Vdc
Emitter–Base Voltage (I_B = 5.0 mAdc)	V_{EBO}	6.0	—	—	Vdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	—	10	μAdc
Collector Cutoff Current (V_{CB} = 150 Vdc, I_E = 0)	I_{CBO}	—	—	10	μAdc

* Indicates Pulse Test: P.W. = 300 μsec max, Duty Cycle = 2%.

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS*					
Collector–Emitter Saturation Voltage (I_C = 500 mAdc, I_B = 50 mAdc)	$V_{CE(sat)}$	—	—	0.8	Vdc
Base–Emitter On Voltage (I_C = 500 mAdc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	—	1.5	Vdc
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc) (I_C = 500 mAdc, V_{CE} = 10 Vdc)	h_{FE}	60 50	— —	— 200	—
DYNAMIC CHARACTERISTICS					
Current Gain Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	—	5.0	—	MHz

* Indicates Pulse Test: P.W. = 300 μsec max, Duty Cycle = 2%.

MJE13002*
MJE13003*

*Motorola Preferred Device

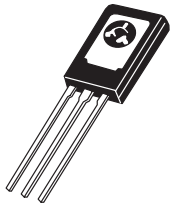
Designer's™ Data Sheet

SWITCHMODE Series
NPN Silicon Power Transistors

1.5 AMPERE
NPN SILICON
POWER TRANSISTORS
300 AND 400 VOLTS
40 WATTS

These devices are designed for high–voltage, high–speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.
SPECIFICATION FEATURES:

- Reverse Biased SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 0.5 to 1.5 Amp, 25 and 100°C
  . . . t_c @ 1 A, 100°C is 290 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	MJE13002	MJE13003	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector–Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	1.5 3		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	0.75 1.5		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	2.25 4.5		Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.4 11.2		Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	89	°C/W
Maximum Load Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 4

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector–Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	MJE13002 MJE13003	$V_{CEO(sus)}$	 300 400	 — —	 — —	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	 — —	 — —	 1 5	mAdc
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	—	—	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with bass forward biased		$I_{S/b}$	See Figure 11			
Clamped Inductive SOA with base reverse biased		RBSOA	See Figure 12			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 2 Vdc) (I_C = 1 Adc, V_{CE} = 2 Vdc)		h_{FE}	 8 5	 — —	 40 25	—
Collector–Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 0.1 Adc) (I_C = 1 Adc, I_B = 0.25 Adc) (I_C = 1.5 Adc, I_B = 0.5 Adc) (I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)		$V_{CE(sat)}$	 — — — —	 — — — —	 0.5 1 3 1	Vdc
Base–Emitter Saturation Voltage (I_C = 0.5 Adc, I_B = 0.1 Adc) (I_C = 1 Adc, I_B = 0.25 Adc) (I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)		$V_{BE(sat)}$	 — — —	 — — —	 1 1.2 1.1	Vdc
DYNAMIC CHARACTERISTICS						
Current–Gain — Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4	10	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	21	—	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 1 A, I_{B1} = I_{B2} = 0.2 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	—	0.05	0.1	μs
Rise Time		t_r	—	0.5	1	μs
Storage Time		t_s	—	2	4	μs
Fall Time		t_f	—	0.4	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Storage Time	(I_C = 1 A, V_{clamp} = 300 Vdc, I_{B1} = 0.2 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	1.7	4	μs
Crossover Time		t_c	—	0.29	0.75	μs
Fall Time		t_{fi}	—	0.15	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

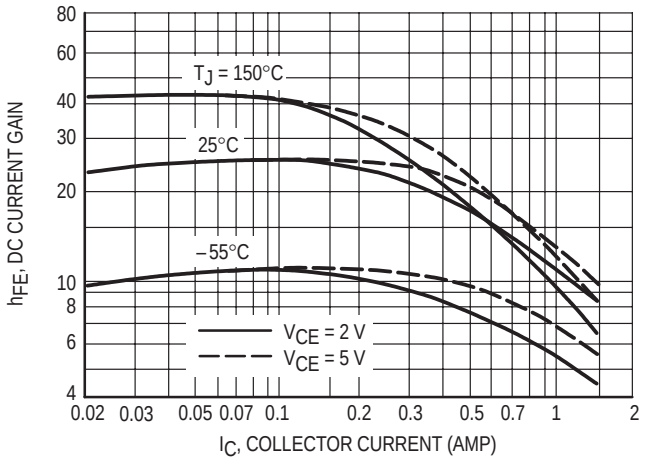


Figure 1. DC Current Gain

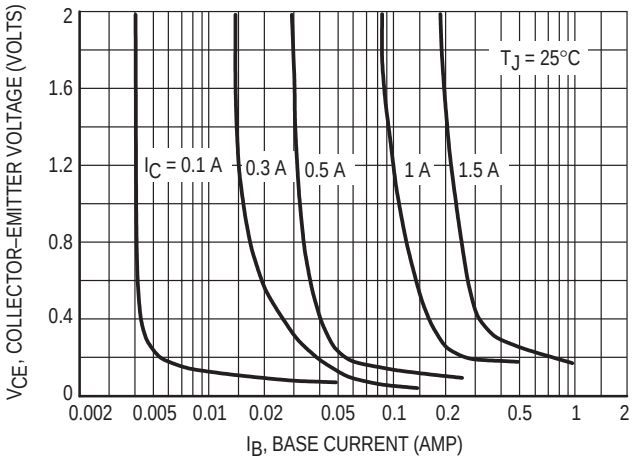


Figure 2. Collector Saturation Region

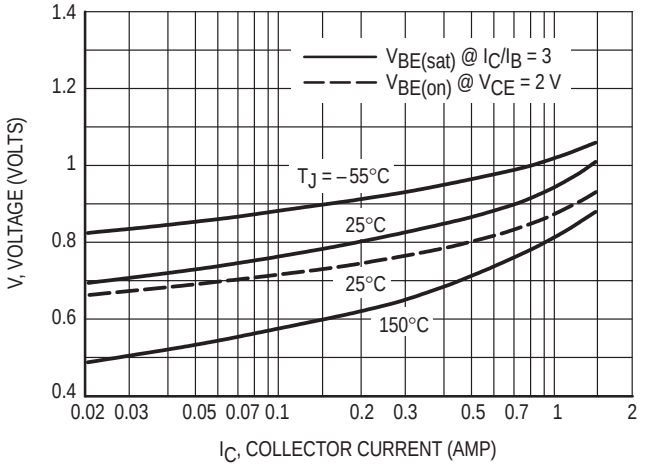


Figure 3. Base−Emitter Voltage

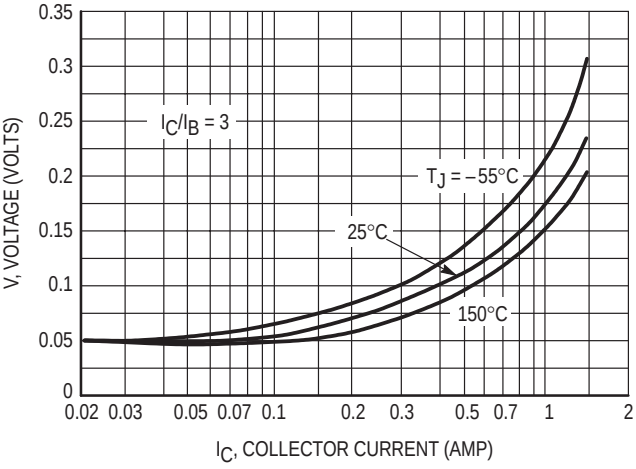


Figure 4. Collector−Emitter Saturation Region

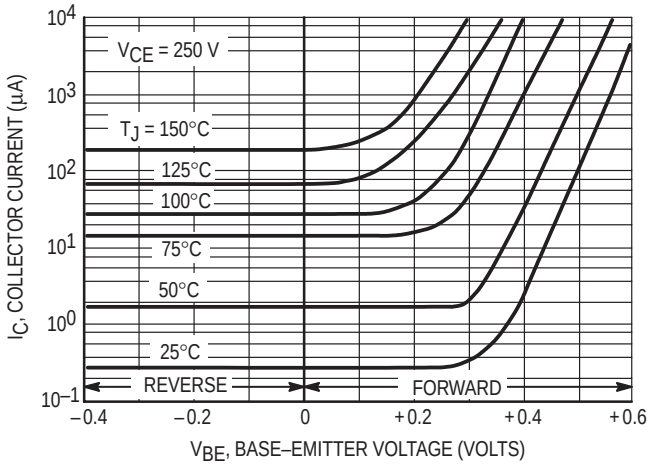


Figure 5. Collector Cutoff Region

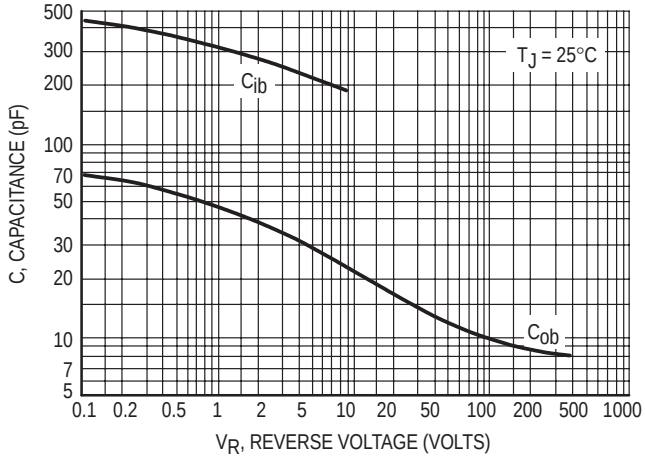
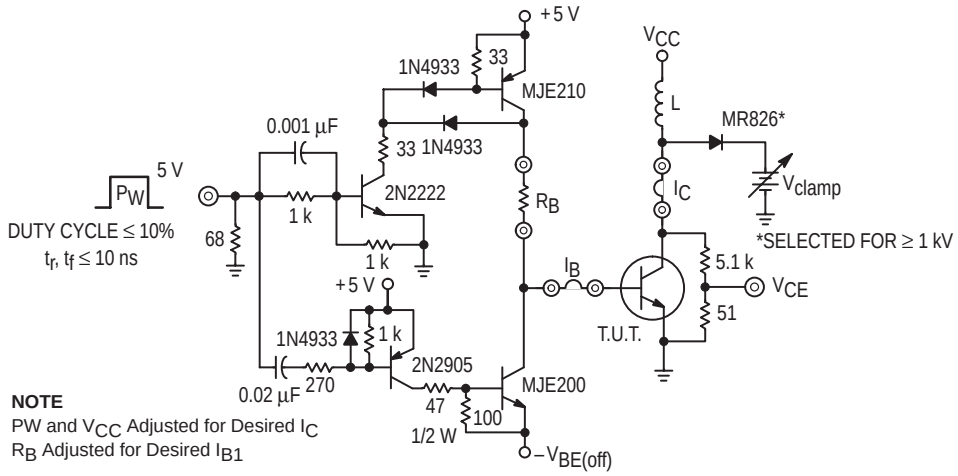
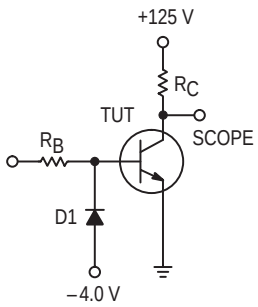
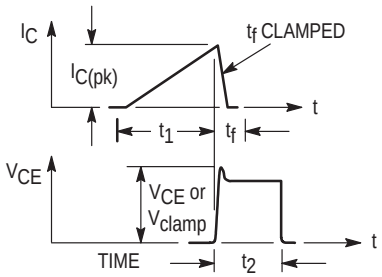
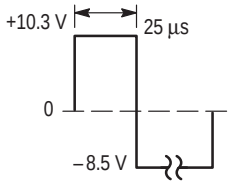


Figure 6. Capacitance

Table 1. Test Conditions for Dynamic Performance

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~200 Turns) #20 GAP for 30 mH/2 A L_{coil} = 50 mH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 125 Ω D1 = 1N5820 or Equiv. R_B = 47 Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope–Tektronics 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

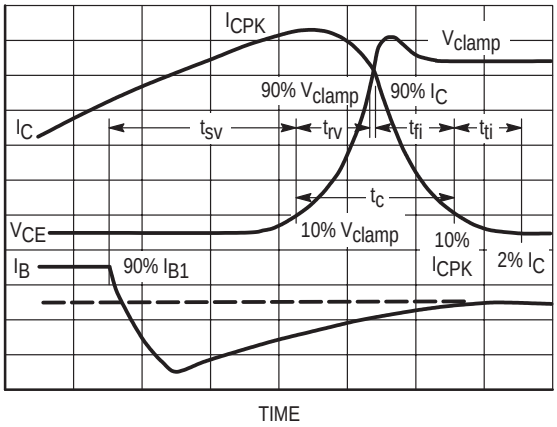


Figure 7. Inductive Switching Measurements

Table 2. Typical Inductive Switching Performance

I_C AMP	T_C °C	t_{sv} µs	t_{rv} µs	t_{fi} µs	t_{ti} µs	t_c µs
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

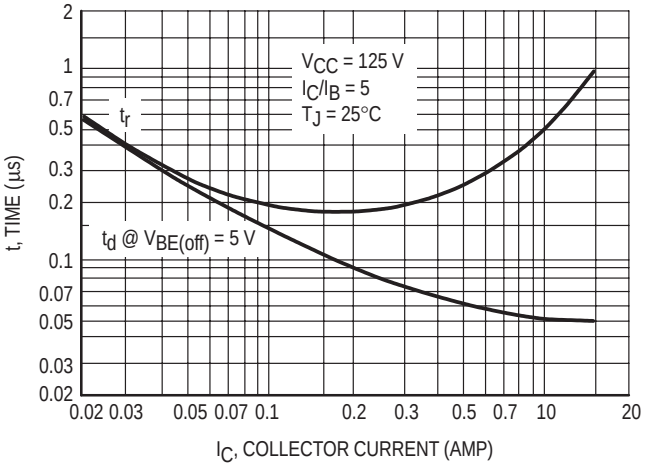


Figure 8. Turn–On Time

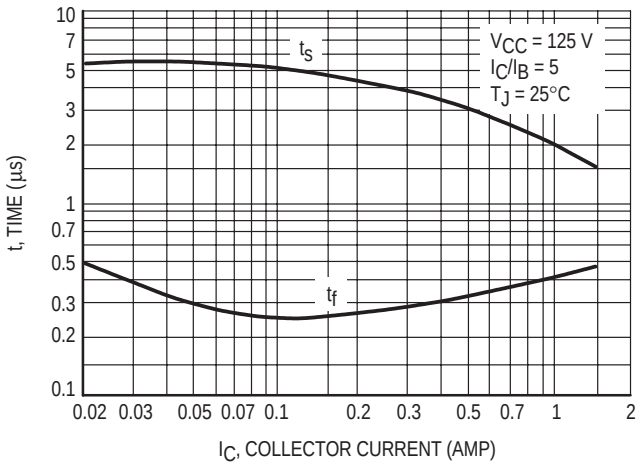


Figure 9. Turn–Off Time

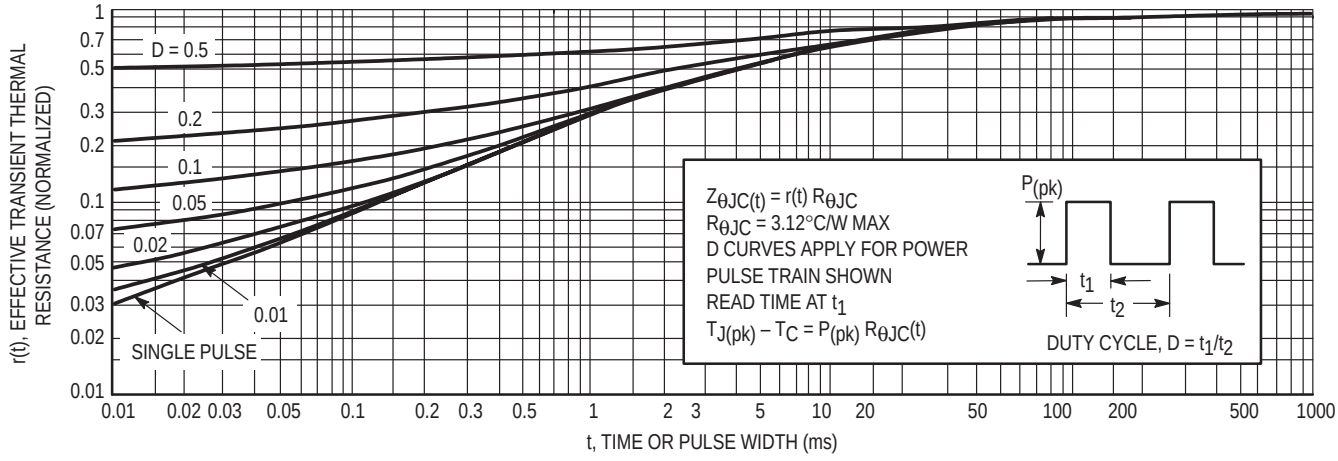


Figure 10. Thermal Response

The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

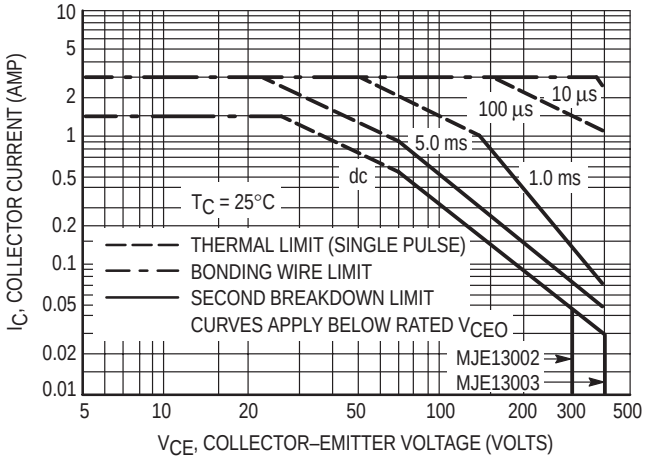


Figure 11. Active Region Safe Operating Area

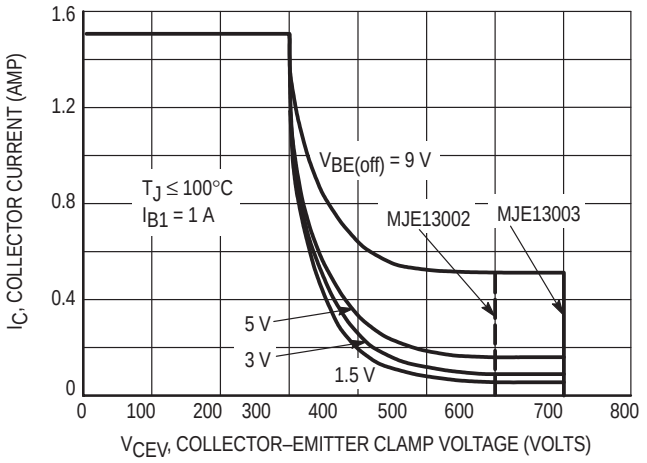


Figure 12. Reverse Bias Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives RBSOA characteristics.

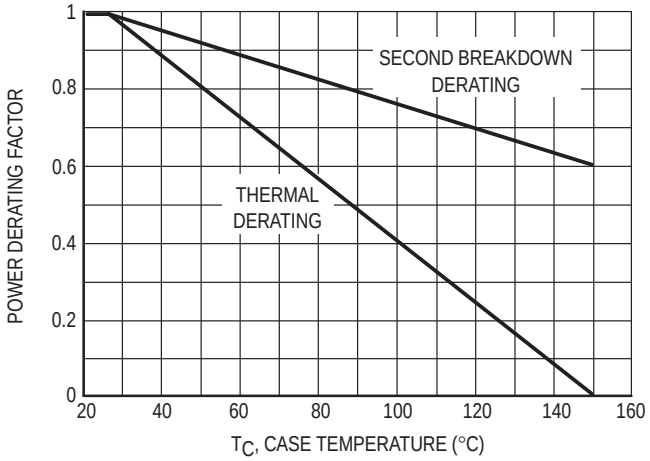


Figure 13. Forward Bias Power Derating

MJE13005*

*Motorola Preferred Device

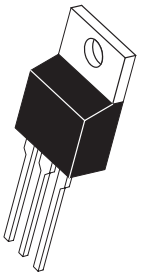
Designer's™ Data Sheet

SWITCHMODE Series NPN Silicon Power Transistors

4 AMPERE
NPN SILICON
POWER TRANSISTOR
400 VOLTS
75 WATTS

These devices are designed for high–voltage, high–speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulator's, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.
SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 2 to 4 Amp, 25 and 100°C
  . . . t_c @ 3A, 100°C is 180 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information.



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector–Emitter Voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EBO}	9	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	4 8	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	6 12	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 16	Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 600	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**						
Collector–Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)		$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			—	—	1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			—	—	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	—	—	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$		See Figure 11		
Clamped Inductive SOA with Base Reverse Biased		RBSOA		See Figure 12		
***ON CHARACTERISTICS**						
DC Current Gain		h_{FE}				—
(I_C = 1 Adc, V_{CE} = 5 Vdc)			10	—	60	
(I_C = 2 Adc, V_{CE} = 5 Vdc)			8	—	40	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 1 Adc, I_B = 0.2 Adc)			—	—	0.5	
(I_C = 2 Adc, I_B = 0.5 Adc)			—	—	0.6	
(I_C = 4 Adc, I_B = 1 Adc)			—	—	1	
(I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)			—	—	1	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 1 Adc, I_B = 0.2 Adc)			—	—	1.2	
(I_C = 2 Adc, I_B = 0.5 Adc)			—	—	1.6	
(I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)			—	—	1.5	
DYNAMIC CHARACTERISTICS						
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	65	—	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 2)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 2 A, I_{B1} = I_{B2} = 0.4 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	—	0.025	0.1	μs
Rise Time		t_r	—	0.3	0.7	μs
Storage Time		t_s	—	1.7	4	μs
Fall Time		t_f	—	0.4	0.9	μs
Inductive Load, Clamped (Table 2, Figure 13)						
Voltage Storage Time	(I_C = 2 A, V_{clamp} = 300 Vdc, I_{B1} = 0.4 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	—	0.9	4	μs
Crossover Time		t_c	—	0.32	0.9	μs
Fall Time		t_{fi}	—	0.16	—	μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

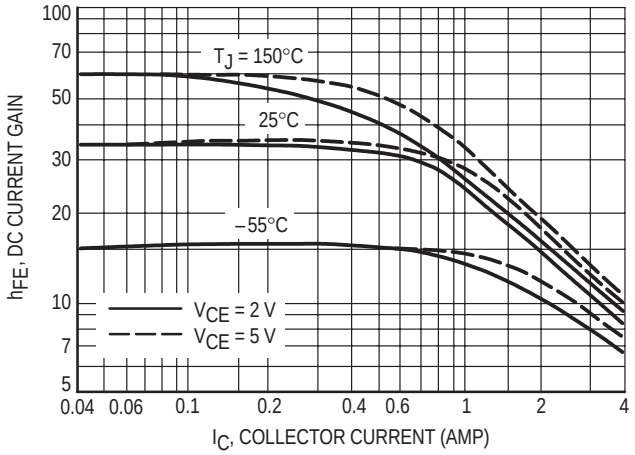


Figure 1. DC Current Gain

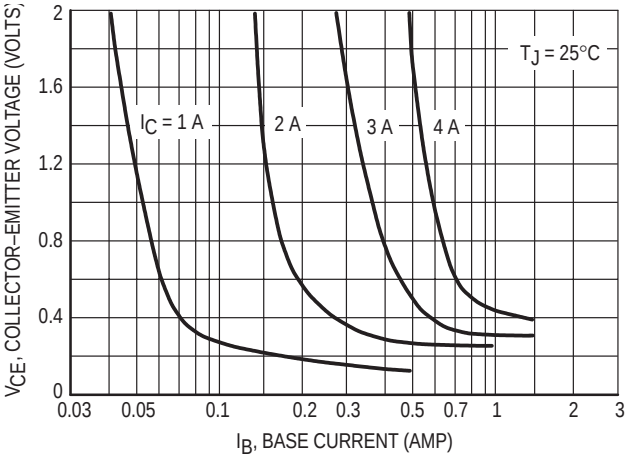


Figure 2. Collector Saturation Region

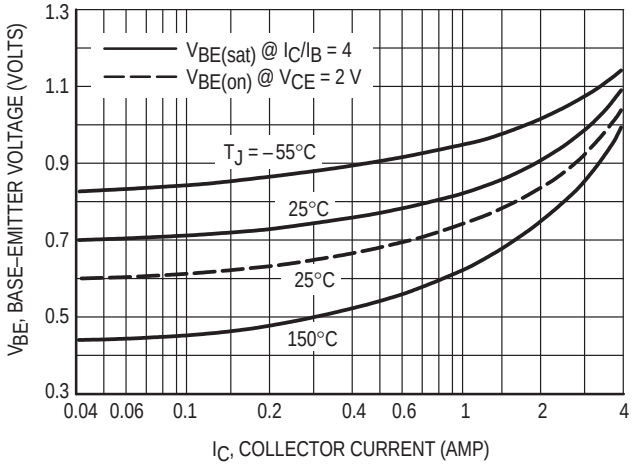


Figure 3. Base–Emitter Voltage

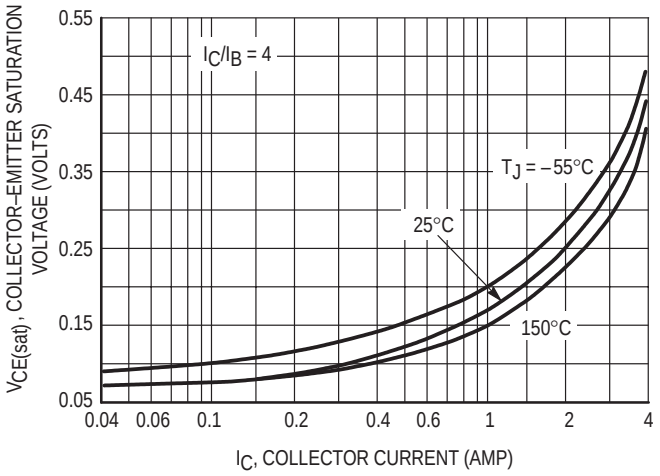


Figure 4. Collector–Emitter Saturation Voltage

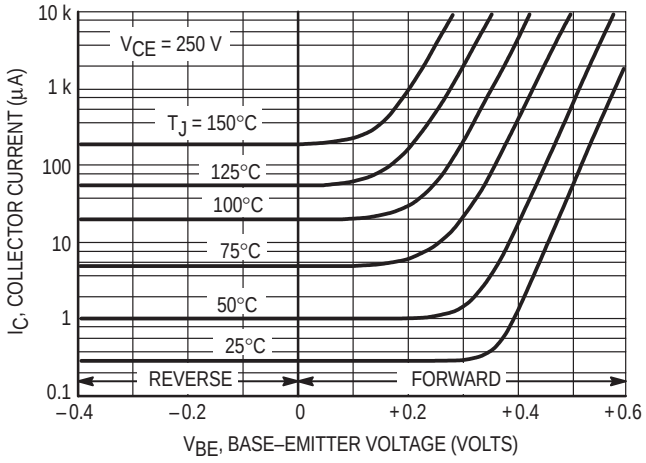


Figure 5. Collector Cutoff Region

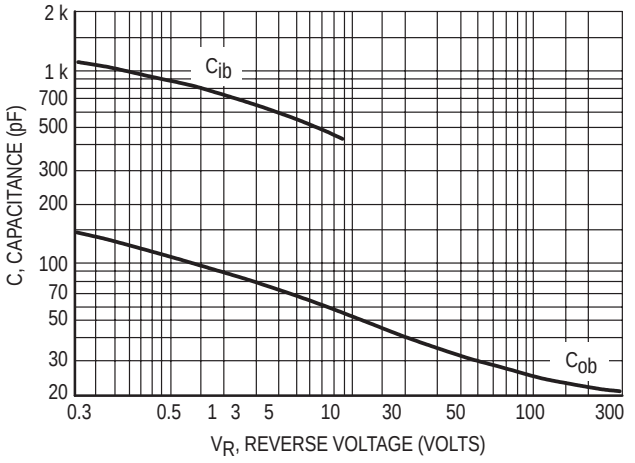


Figure 6. Capacitance

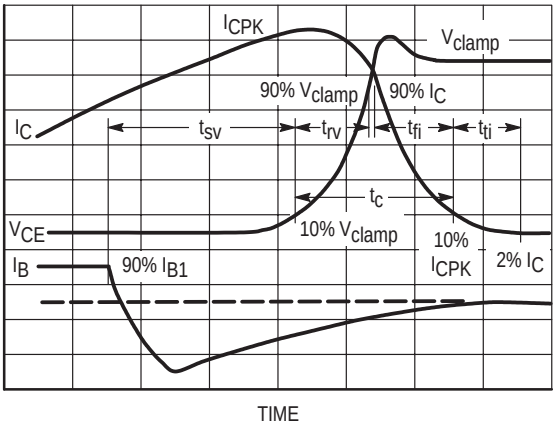


Figure 7. Inductive Switching Measurements

Table 1. Typical Inductive Switching Performance

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
2	25 100	600 900	70 110	100 240	80 130	180 320
3	25 100	650 950	60 100	140 330	60 100	200 350
4	25 100	550 850	70 110	160 350	100 160	220 390

NOTE: All Data recorded in the inductive Switching Circuit In Table 2.

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

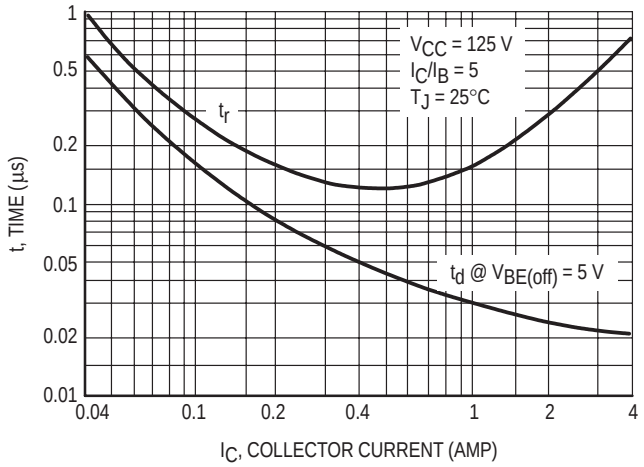


Figure 8. Turn–On Time

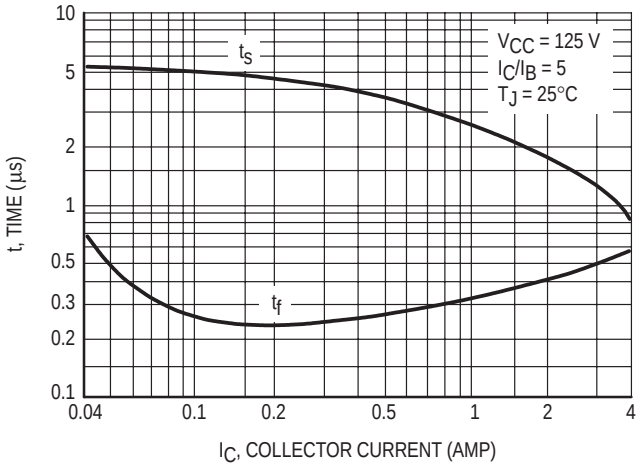
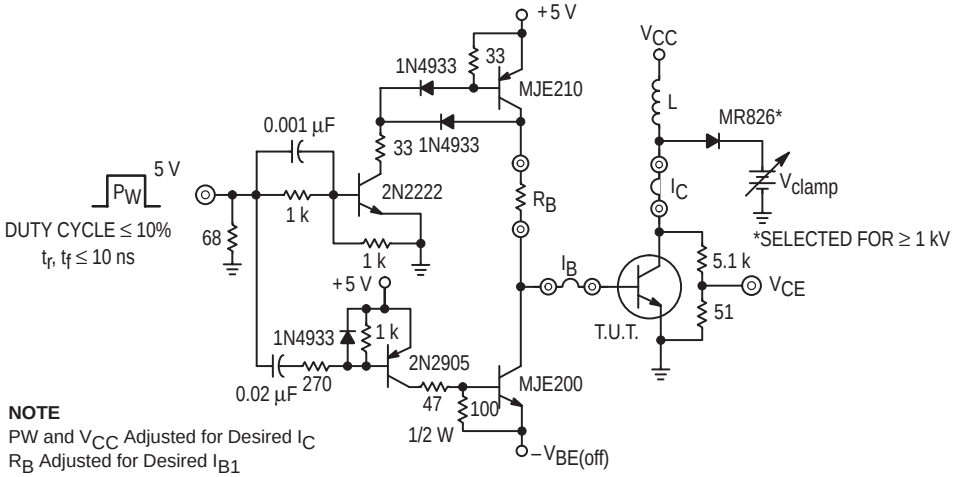
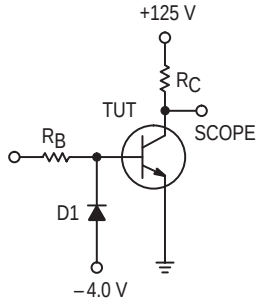
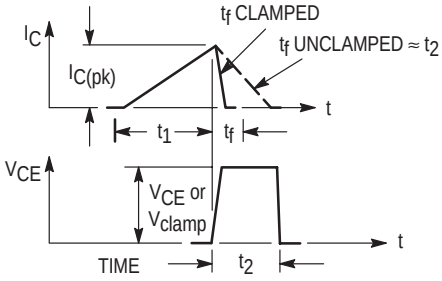
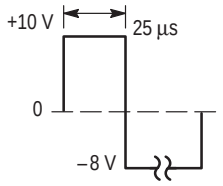


Figure 9. Turn–Off Time

Table 2. Test Conditions for Dynamic Performance

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 µH/20 A L_{coil} = 200 µH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 62 Ω D1 = 1N5820 or Equiv. R_B = 22 Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 ADJUSTED TO OBTAIN I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope–Tektronics 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

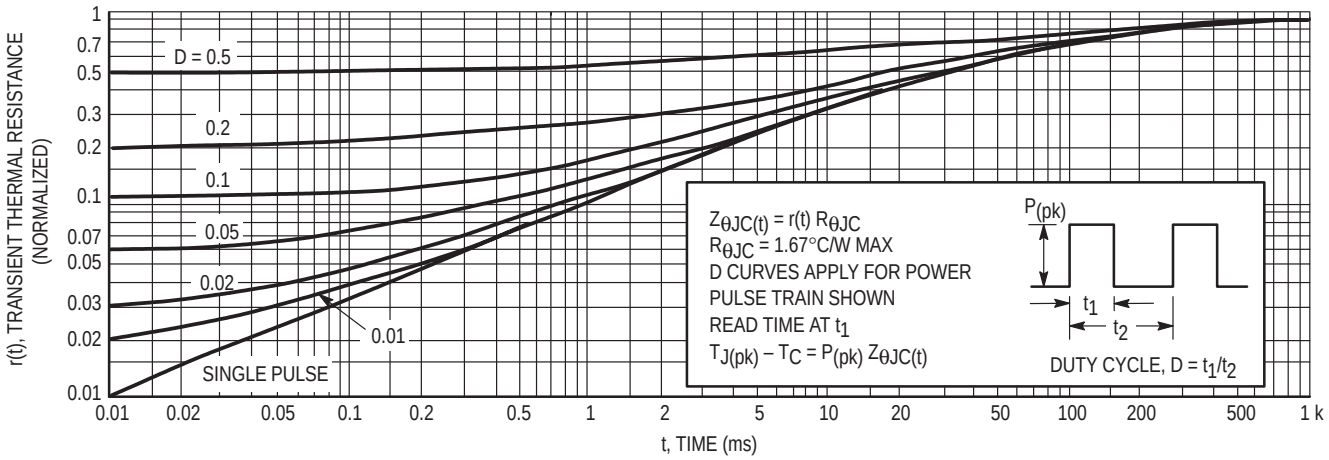


Figure 10. Typical Thermal Response [$Z_{\theta JC}(t)$]

The Safe Operating Area Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

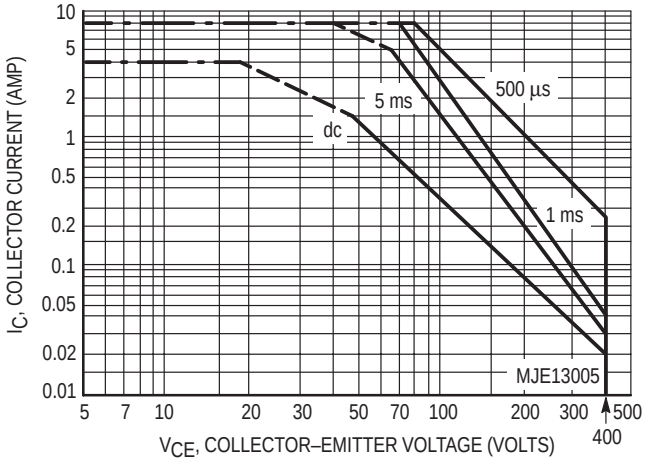


Figure 11. Forward Bias Safe Operating Area

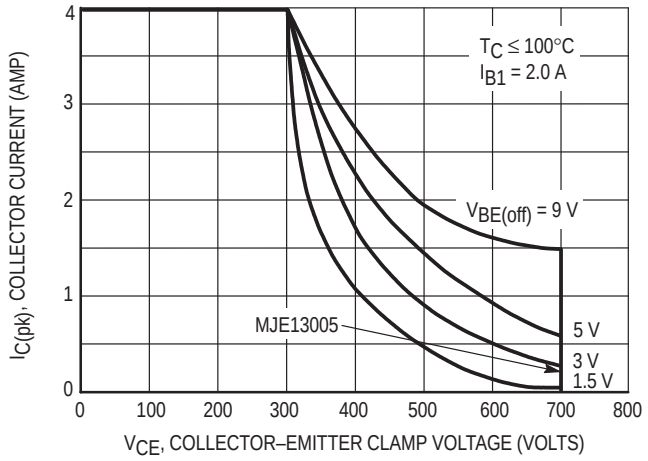


Figure 12. Reverse Bias Switching Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete RBSOA characteristics.

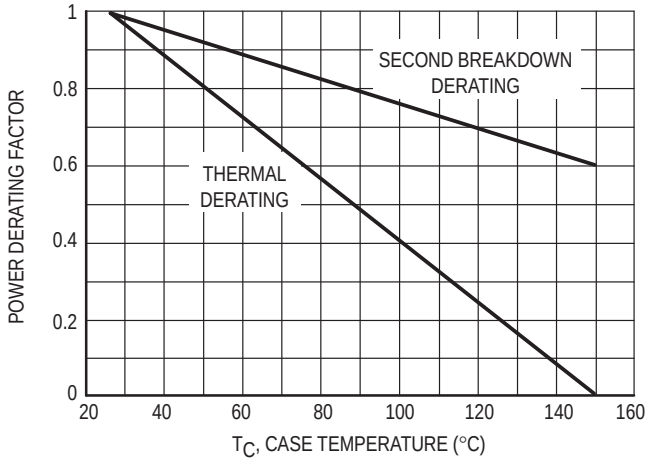


Figure 13. Forward Bias Power Derating

MJE13007
MJF13007

Designer's Data Sheet

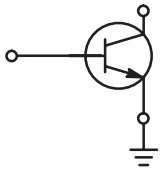
SWITCHMODE™

NPN Bipolar Power Transistor For Switching Power Supply Applications

POWER TRANSISTOR
8.0 AMPERES
400 VOLTS
80/40 WATTS

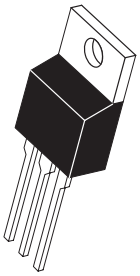
The MJE/MJF13007 is designed for high–voltage, high–speed power switching inductive circuits where fall time is critical. It is particularly suited for 115 and 220 V switchmode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

- $V_{CEO(sus)}$ 400 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- 700 V Blocking Capability
- SOA and Switching Applications Information
- Two Package Choices: Standard TO–220 or Isolated TO–220
- MJF13007 is UL Recognized to 3500 V_{RMS}, File #E69369



MAXIMUM RATINGS

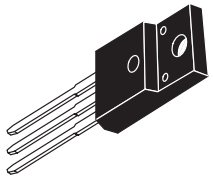
Rating	Symbol	MJE13007	MJF13007	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	400		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	700		Vdc
Emitter–Base Voltage	V_{EBO}	9.0		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8.0 16		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4.0 8.0		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	12 24		Adc
RMS Isolation Voltage (for 1 sec, R.H. < 30%, T_A = 25°C) Test No. 1 Per Fig. 15 Test No. 2 Per Fig. 16 Test No. 3 Per Fig. 17 Proper strike and creepage distance must be provided	V_{ISOL}	 — — —	 4500 3500 1500	V
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.64	40* 0.32	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	– 65 to 150		°C



CASE 221A–06
TO–220AB
MJE13007

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.56 62.5	3.12 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C



CASE 221D–02
ISOLATED TO–220 TYPE
UL RECOGNIZED
MJF13007

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
*Measurement made with thermocouple contacting the bottom insulated mountign surface of the package (in a location beneath the die), the device mounted on a heatsink with thermal grease applied at a mounting torque of 6 to 8•lbs.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**							
Collector–Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)			$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current			I_{CES}				mAdc
(V_{CES} = 700 Vdc)				—	—	0.1	
(V_{CES} = 700 Vdc, T_C = 125°C)				—	—	1.0	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)			I_{EBO}	—	—	100	μAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$	See Figure 6			
Clamped Inductive SOA with Base Reverse Biased			—	See Figure 7			
***ON CHARACTERISTICS**							
DC Current Gain			h_{FE}				—
(I_C = 2.0 Adc, V_{CE} = 5.0 Vdc)				8.0	—	40	
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)				5.0	—	30	
Collector–Emitter Saturation Voltage			$V_{CE(sat)}$				Vdc
(I_C = 2.0 Adc, I_B = 0.4 Adc)				—	—	1.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc)				—	—	2.0	
(I_C = 8.0 Adc, I_B = 2.0 Adc)				—	—	3.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)				—	—	3.0	
Base–Emitter Saturation Voltage			$V_{BE(sat)}$				Vdc
(I_C = 2.0 Adc, I_B = 0.4 Adc)				—	—	1.2	
(I_C = 5.0 Adc, I_B = 1.0 Adc)				—	—	1.6	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)				—	—	1.5	
DYNAMIC CHARACTERISTICS							
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)			f_T	4.0	14	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)			C_{ob}	—	80	—	pF
Collector to Heatsink Capacitance, MJF13007			$C_{c–hs}$	—	3.0	—	pF
SWITCHING CHARACTERISTICS							
Resistive Load (Table 1)							
Delay Time	(V_{CC} = 125 Vdc, I_C = 5.0 A, I_{B1} = I_{B2} = 1.0 A, t_p = 25 μs, Duty Cycle ≤ 1.0%)		t_d	—	0.025	0.1	μs
Rise Time			t_r	—	0.5	1.5	
Storage Time			t_s	—	1.8	3.0	
Fall Time			t_f	—	0.23	0.7	
Inductive Load, Clamped (Table 1)							
Voltage Storage Time	V_{CC} = 15 Vdc, I_C = 5.0 A, V_{clamp} = 300 Vdc	T_C = 25°C	t_{sv}	—	1.2	2.0	μs
		T_C = 100°C		—	1.6	3.0	
Crossover Time	$I_{B(on)}$ = 1.0 A, $I_{B(off)}$ = 2.5 A, L_C = 200 μH	T_C = 25°C	t_c	—	0.15	0.30	μs
		T_C = 100°C		—	0.21	0.50	
Fall Time		T_C = 25°C	t_{fi}	—	0.04	0.12	μs
		T_C = 100°C		—	0.10	0.20	

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

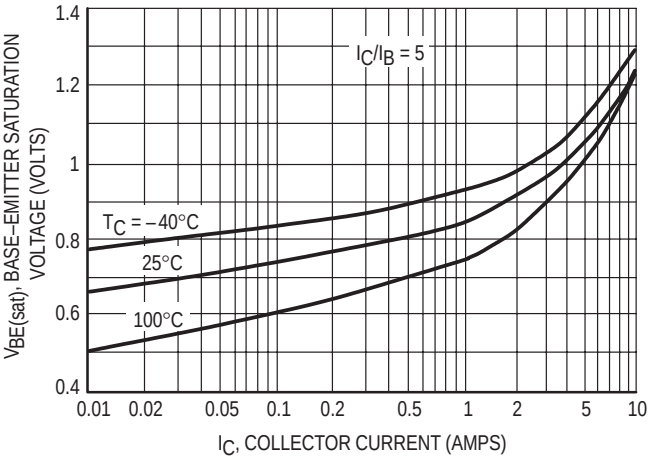


Figure 1. Base–Emitter Saturation Voltage

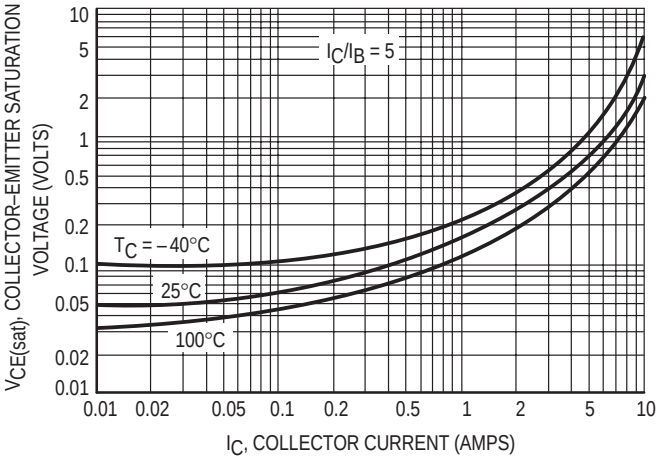


Figure 2. Collector–Emitter Saturation Voltage

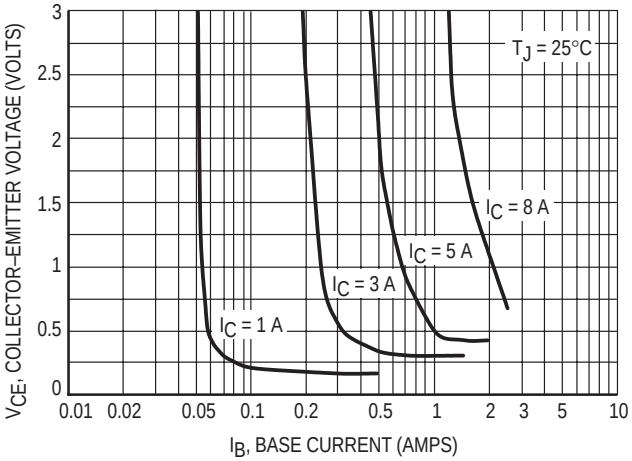


Figure 3. Collector Saturation Region

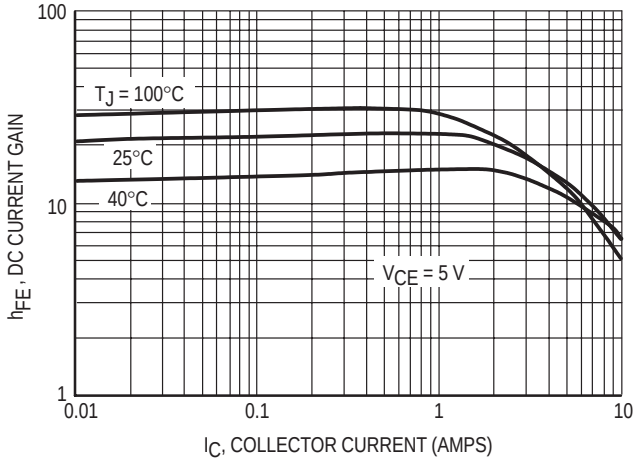


Figure 4. DC Current Gain

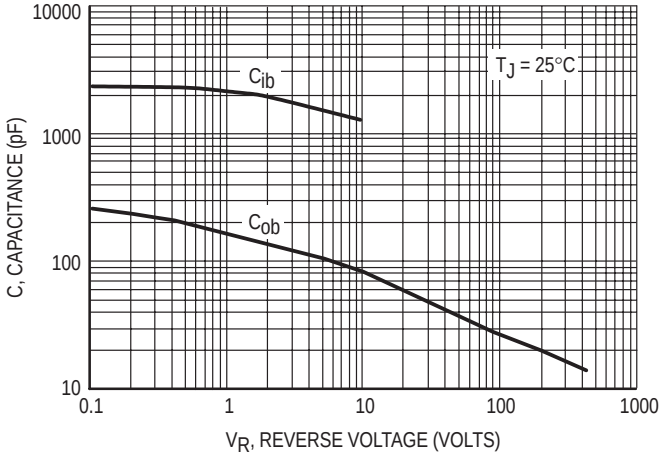


Figure 5. Capacitance

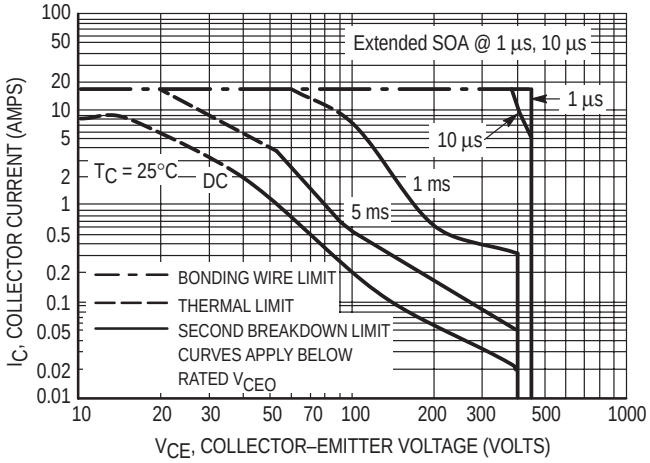


Figure 6. Maximum Forward Bias Safe Operating Area

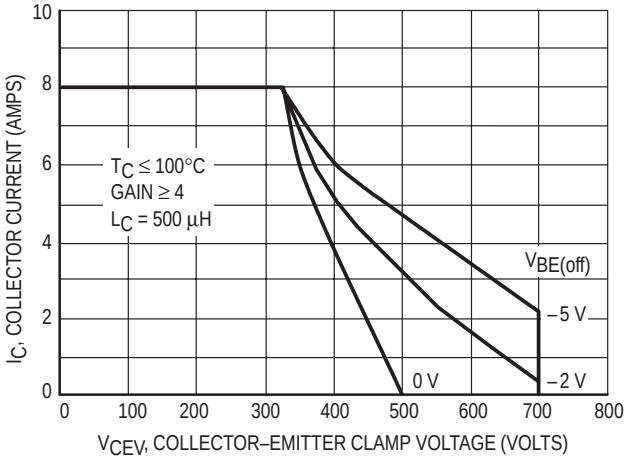


Figure 7. Maximum Reverse Bias Switching Safe Operating Area

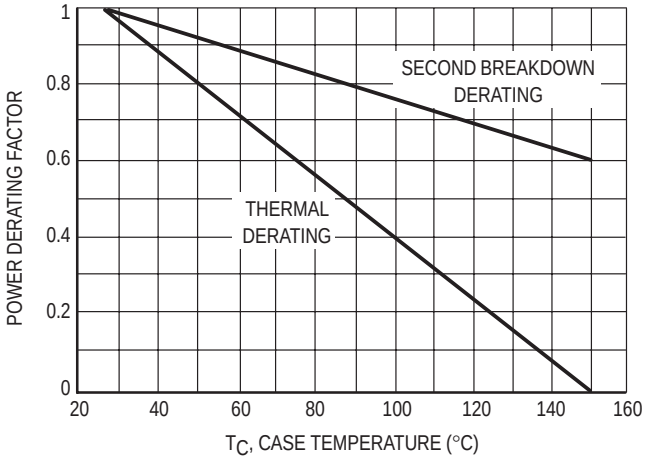


Figure 8. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C — V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge$ 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 6 may be found at any case temperature by using the appropriate curve on Figure 8.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 7) is discussed in the applications information section.

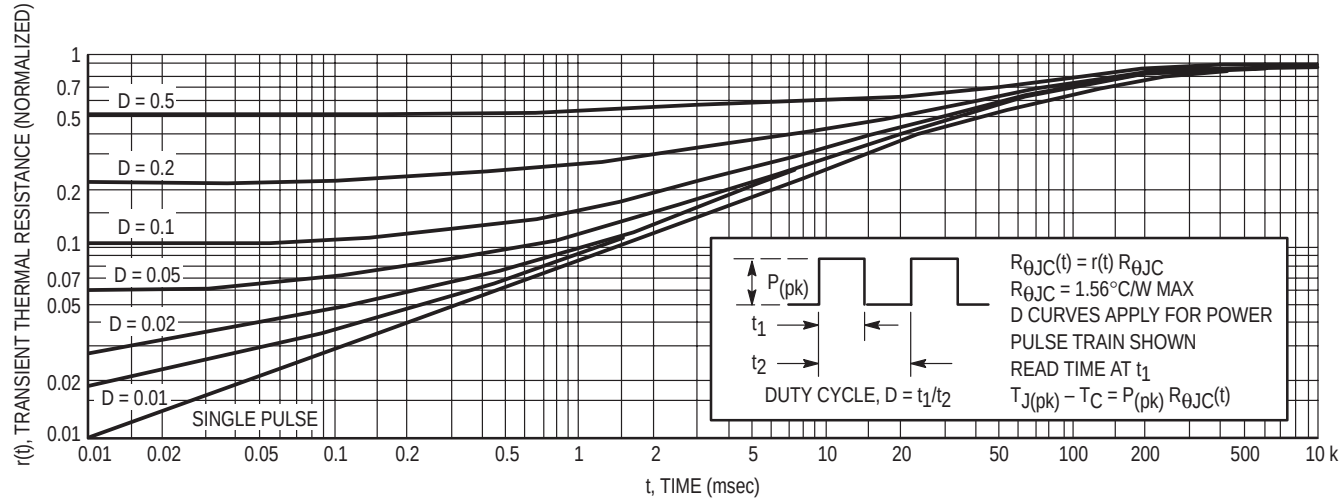


Figure 9. Typical Thermal Response for MJE13007

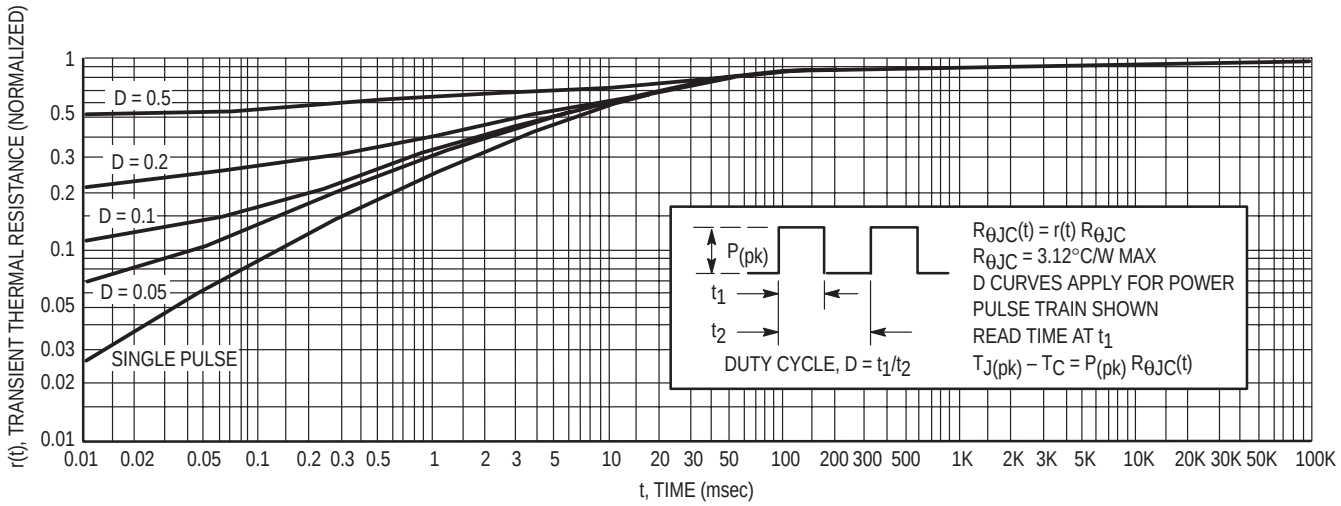


Figure 10. Typical Thermal Response for MJF13007

SPECIFICATION INFORMATION FOR SWITCHMODE APPLICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

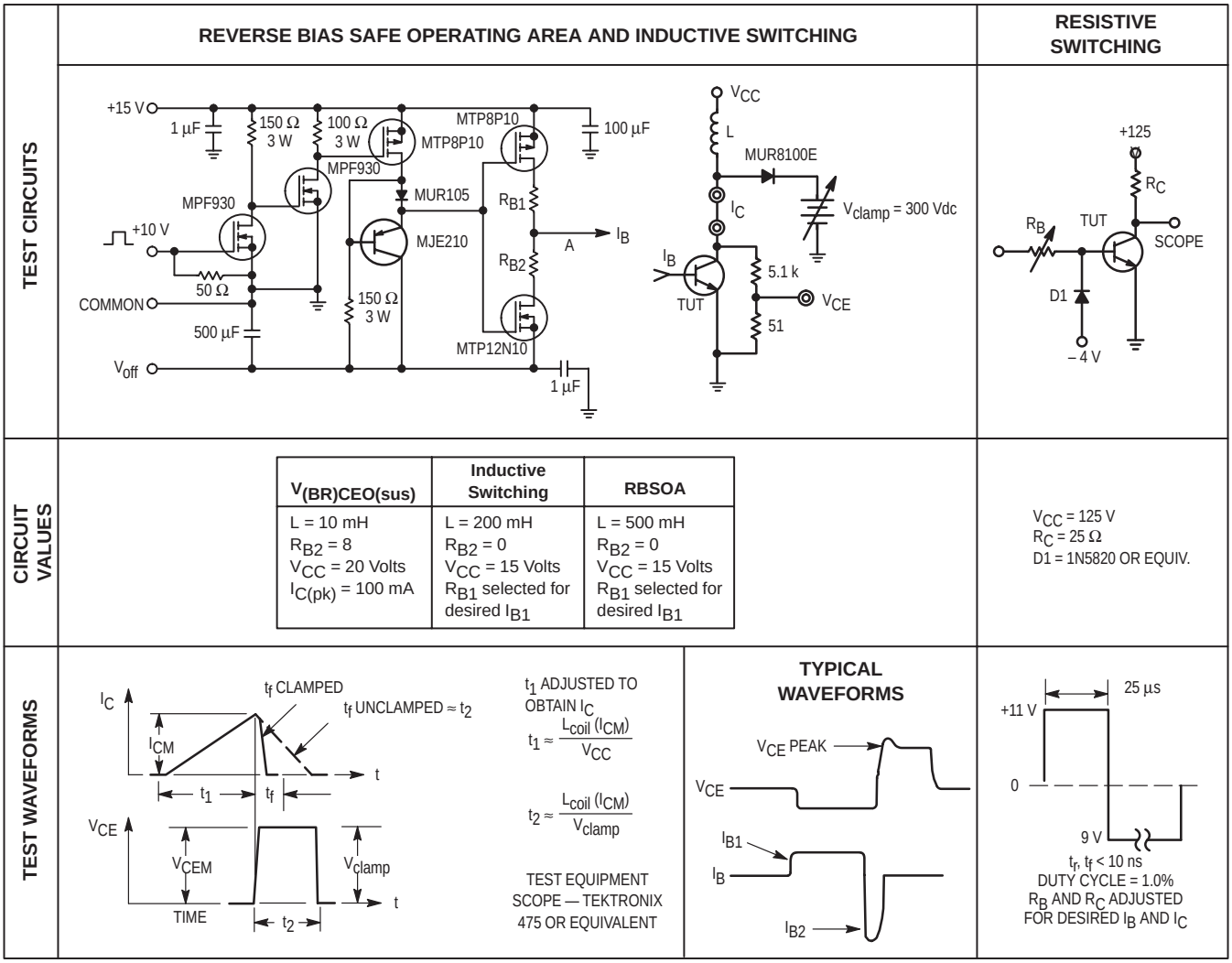
Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn–on and turn–off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn–on and the pulsed forward bias SOA curves (Figure 6) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 7) which represents voltage–current conditions that can be sustained during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

(1) For detailed information on specific switching applications, see Motorola Application Note AN719, AN873, AN875, AN951.

Table 1. Test Conditions For Dynamic Performance



VOLTAGE REQUIREMENTS (continued)

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn–off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn–on and within the reverse bias SOA curve during turn–off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.

(2) The turn–on time does not exceed 10 µs (see standard pulsed forward SOA curves in Figure 6).

(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 7).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 5.0 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base–emitter junction during turn–off. The reverse biased switching characteristics for inductive loads are shown in Figures 13 and 14 and resistive loads in Figures 11 and 12. Usually the inductive load components will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (see Table 1) providing correlation between test procedures and actual use conditions.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and any coil driver, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn–off waveforms is shown in Figure 13 to aid in the visual identity of these terms. For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN222A:

$$P_{SWT} = 1/2\ V_{CC} I_C(t_c)\ f$$

Typical inductive switching times are shown in Figure 14. In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

SWITCHING PERFORMANCE

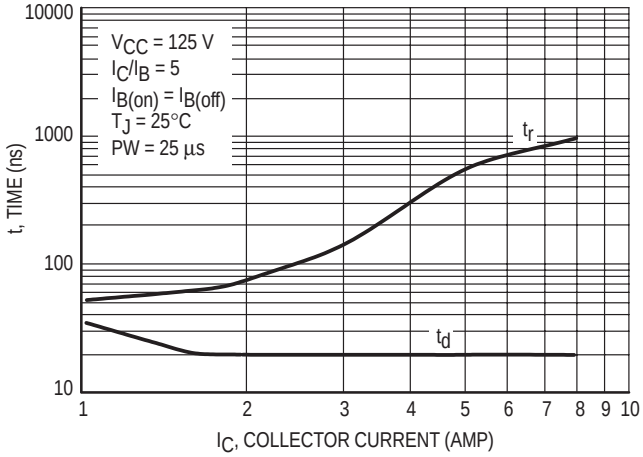


Figure 11. Turn–On Time (Resistive Load)

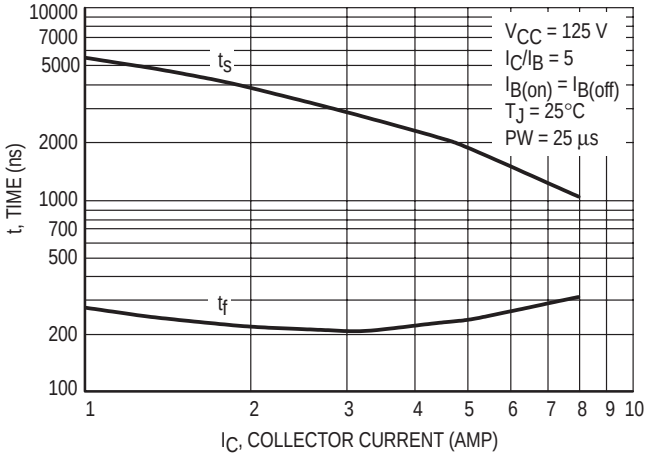


Figure 12. Turn–Off Time (Resistive Load)

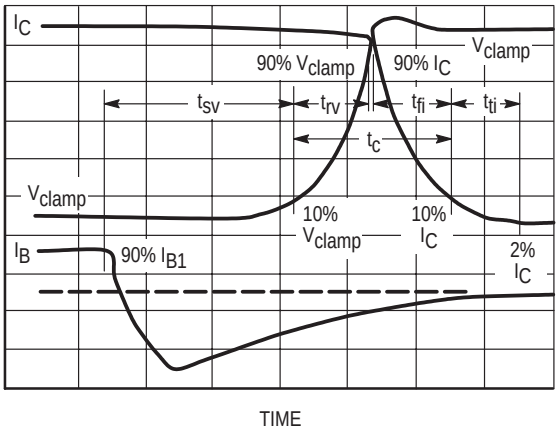


Figure 13. Inductive Switching Measurements

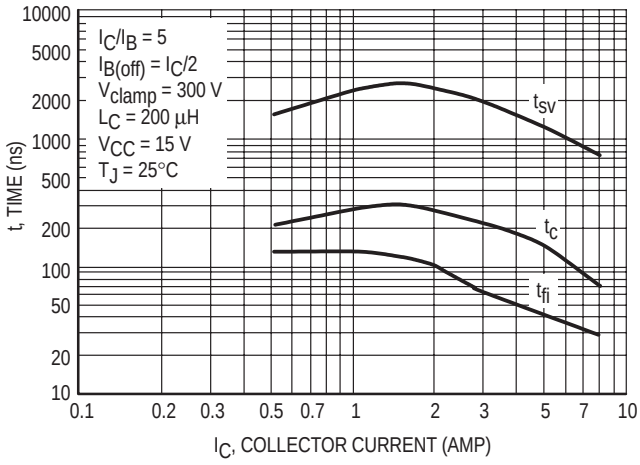
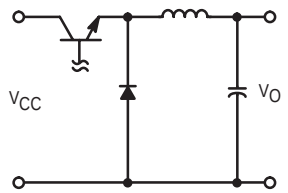
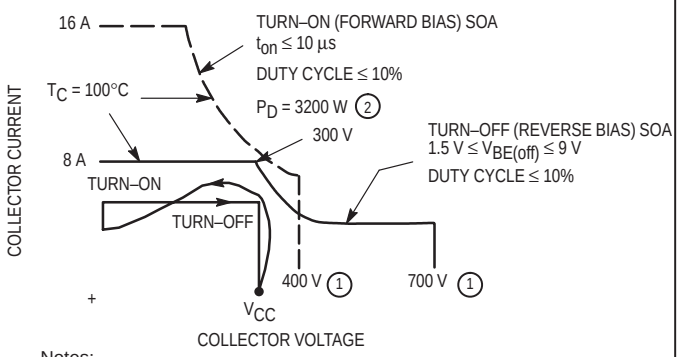
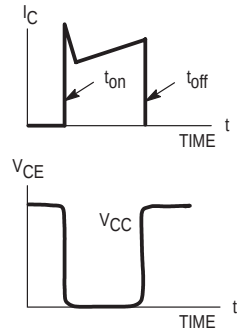
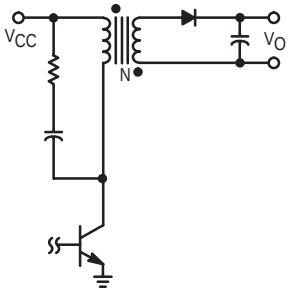
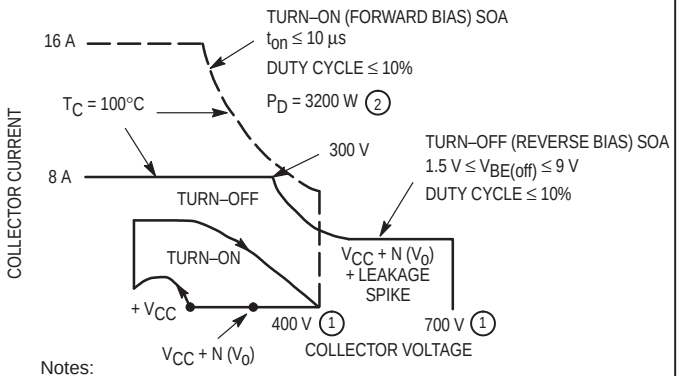
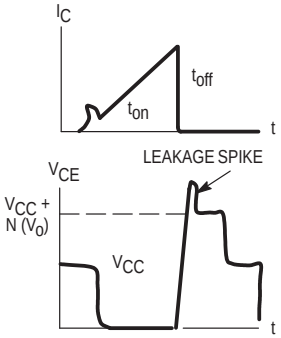
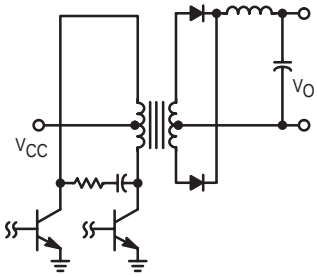
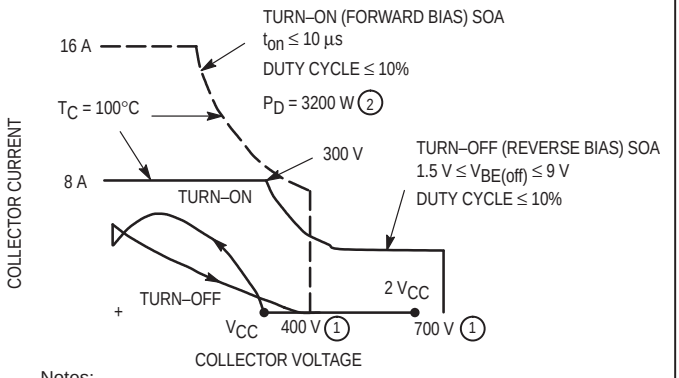
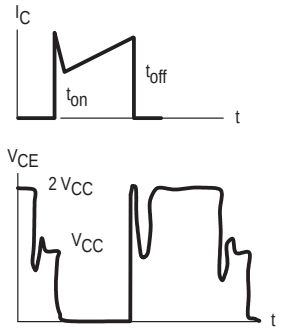
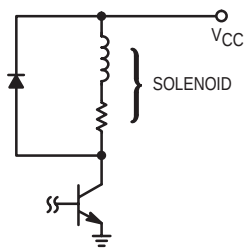
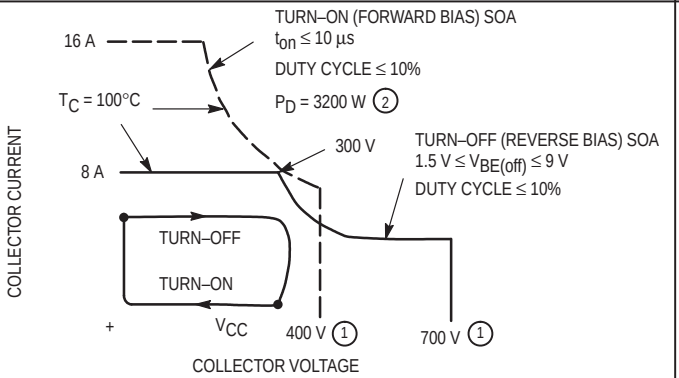
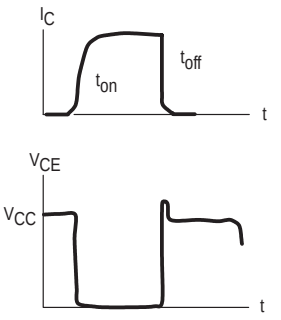


Figure 14. Typical Inductive Switching Times

Table 2. Applications Examples of Switching Circuits

	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 	 Notes: (1) See AN569 for Pulse Power Derating Procedure.	
B	**FLYBACK INVERTER** 	 Notes: (1) See AN569 for Pulse Power Derating Procedure.	
C	**PUSH–PULL INVERTER/CONVERTER** 	 Notes: (1) See AN569 for Pulse Power Derating Procedure.	
D	**SOLENOID DRIVER** 	 Notes: (1) See AN569 for Pulse Power Derating Procedure.	

TEST CONDITIONS FOR ISOLATION TESTS*

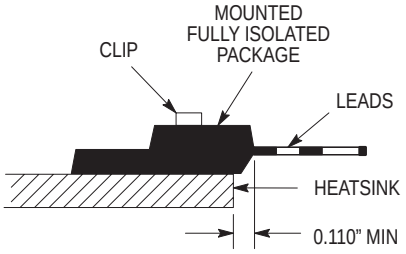


Figure 15. Screw or Clip Mounting Position for Isolation Test Number 1

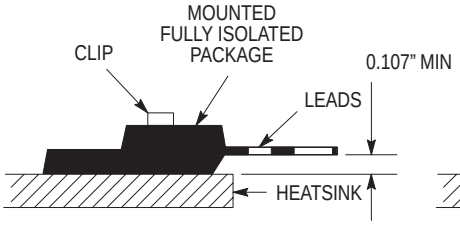


Figure 16. Clip Mounting Position for Isolation Test Number 2

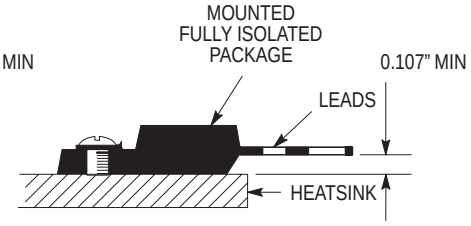


Figure 17. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

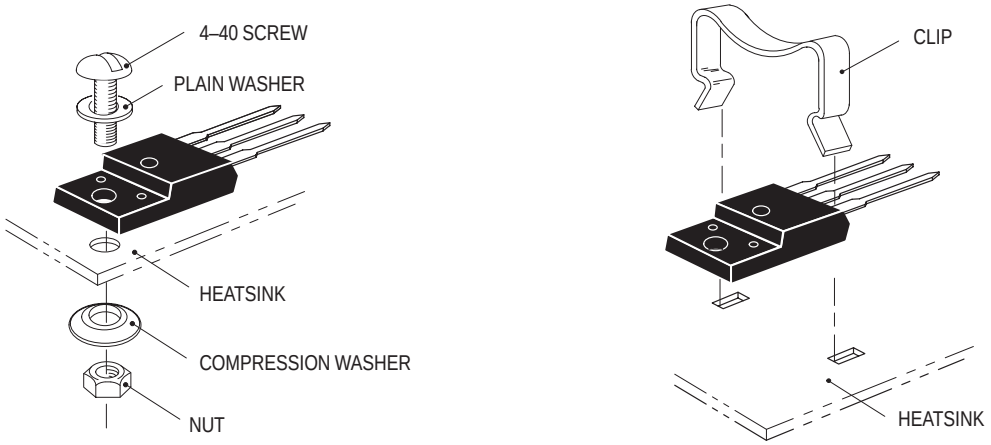


Figure 18. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

MJE13009*

*Motorola Preferred Device

Designer's™ Data Sheet

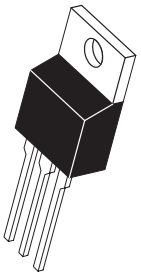
SWITCHMODE Series NPN Silicon Power Transistors

12 AMPERE
NPN SILICON
POWER TRANSISTOR
400 VOLTS
100 WATTS

The MJE13009 is designed for high–voltage, high–speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switchmode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 3 to 12 Amp, 25 and 100°C
  . . . t_c @ 8 A, 100°C is 120 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector–Emitter Voltage	V_{CEV}	700	Vdc
Emitter Base Voltage	V_{EBO}	9	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	12 24	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	6 12	Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	18 36	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 16	Watts mW/°C
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 800	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Collector–Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		—	—	1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		—	—	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	—	—	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 1			
Clamped Inductive SOA with Base Reverse Biased	—	See Figure 2			
***ON CHARACTERISTICS**					
DC Current Gain	h_{FE}				
(I_C = 5 Adc, V_{CE} = 5 Vdc)		8	—	40	
(I_C = 8 Adc, V_{CE} = 5 Vdc)		6	—	30	
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 1 Adc)		—	—	1	
(I_C = 8 Adc, I_B = 1.6 Adc)		—	—	1.5	
(I_C = 12 Adc, I_B = 3 Adc)		—	—	3	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)		—	—	2	
Base–Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 1 Adc)		—	—	1.2	
(I_C = 8 Adc, I_B = 1.6 Adc)		—	—	1.6	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)		—	—	1.5	
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	—	180	—	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	t_d	—	0.06	0.1	µs
Rise Time	t_r	—	0.45	1	µs
Storage Time	t_s	—	1.3	3	µs
Fall Time	t_f	—	0.2	0.7	µs
Inductive Load, Clamped (Table 1, Figure 13)					
Voltage Storage Time	t_{sv}	—	0.92	2.3	µs
Crossover Time	t_c	—	0.12	0.7	µs

(V_{CC} = 125 Vdc, I_C = 8 A, I_{B1} = I_{B2} = 1.6 A, t_p = 25 µs, Duty Cycle ≤ 1%)

(I_C = 8 A, V_{clamp} = 300 Vdc, I_{B1} = 1.6 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)

*Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2%.

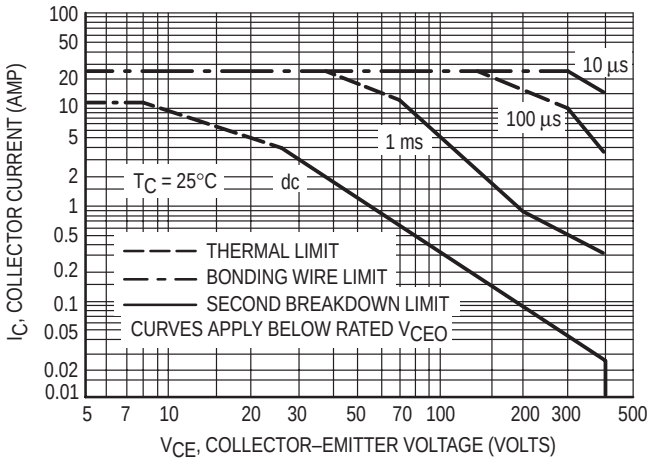


Figure 1. Forward Bias Safe Operating Area

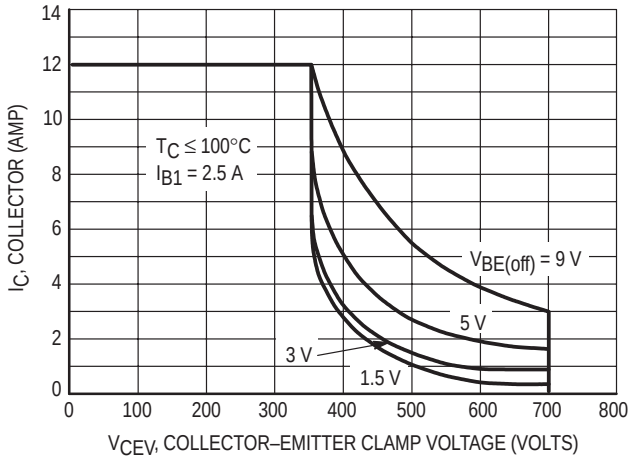


Figure 2. Reverse Bias Switching Safe Operating Area

The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

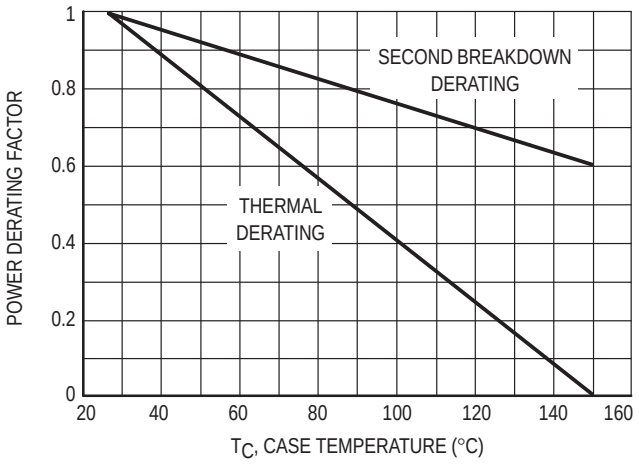


Figure 3. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

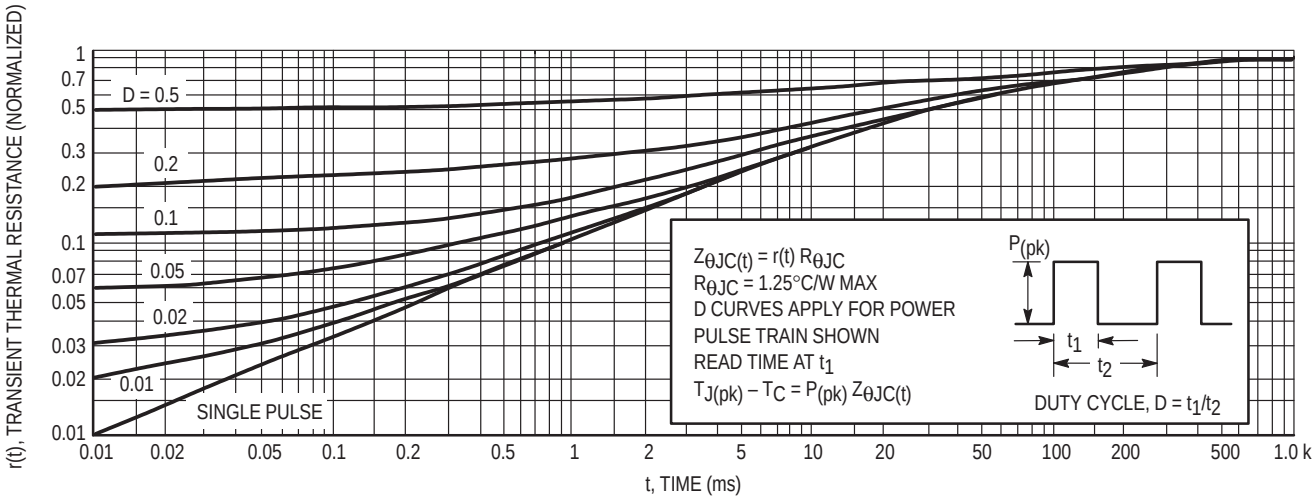


Figure 4. Typical Thermal Response [$Z_{\theta JC}(t)$]

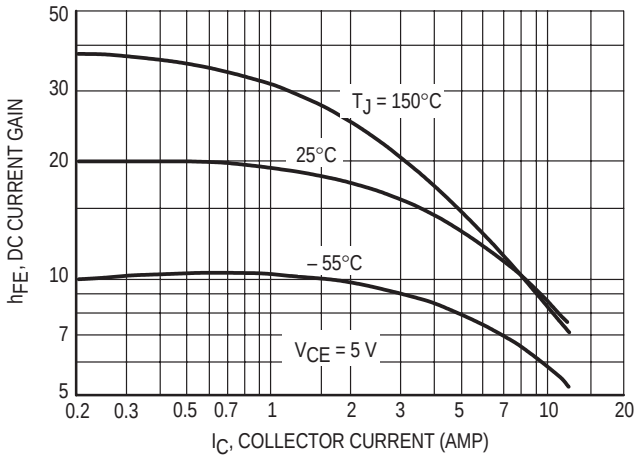


Figure 5. DC Current Gain

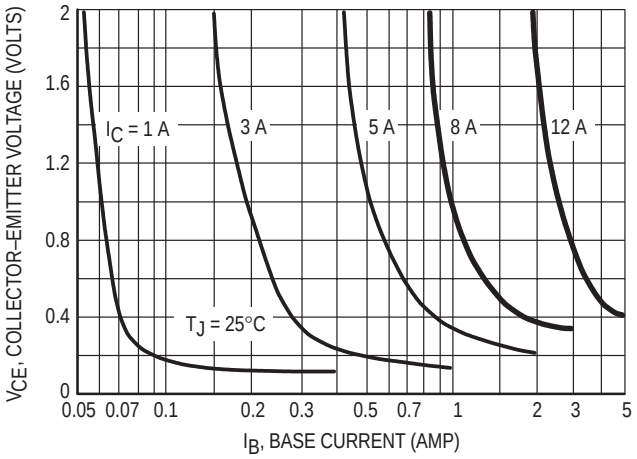


Figure 6. Collector Saturation Region

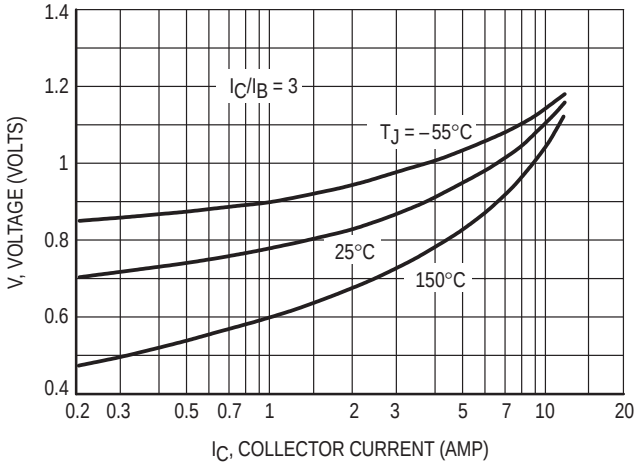


Figure 7. Base–Emitter Saturation Voltage

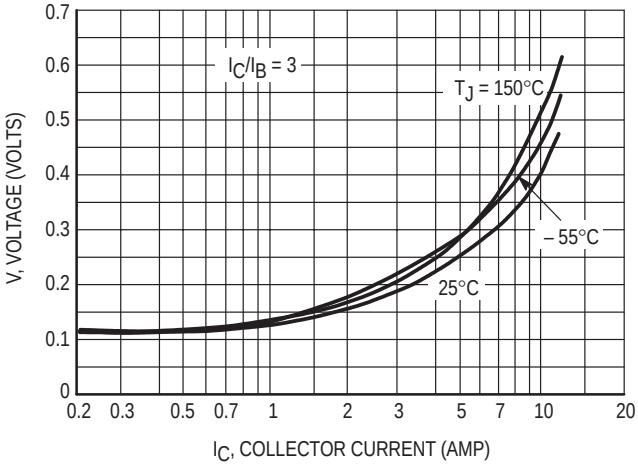


Figure 8. Collector–Emitter Saturation Voltage

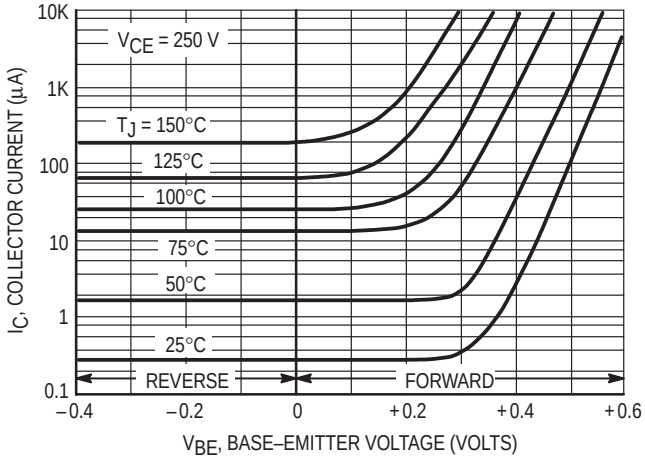


Figure 9. Collector Cutoff Region

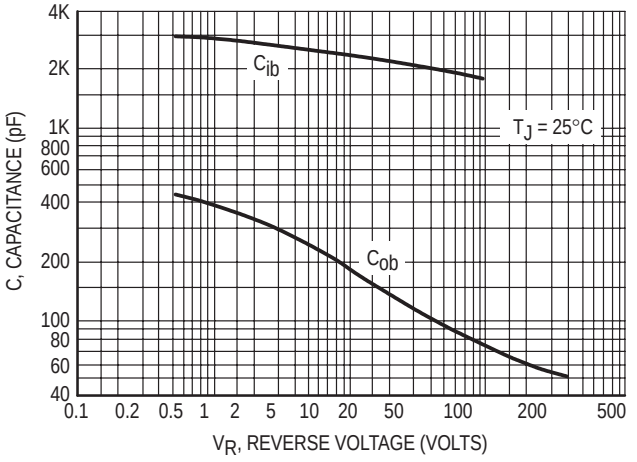
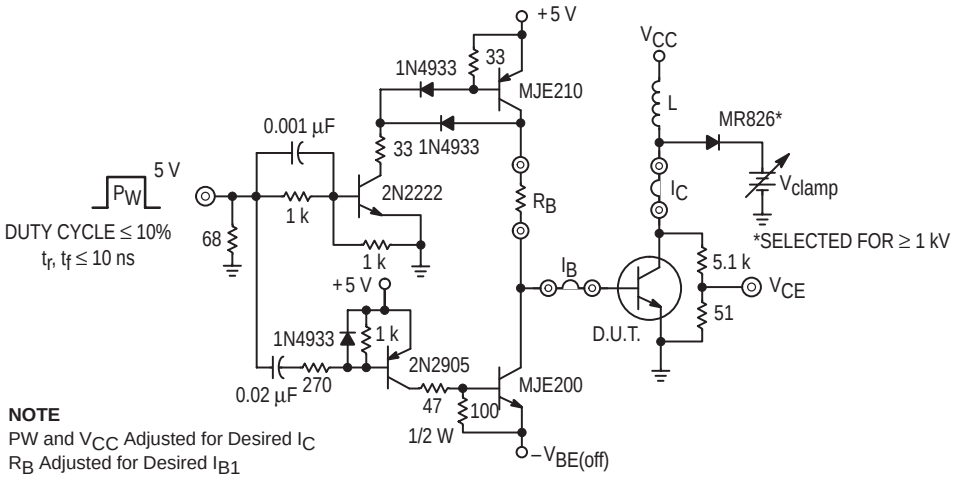
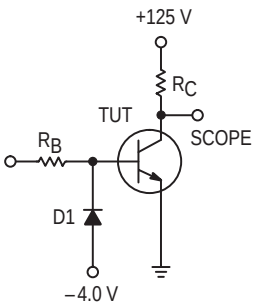
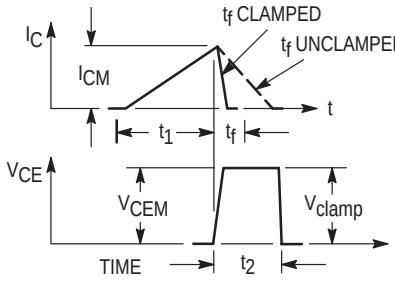
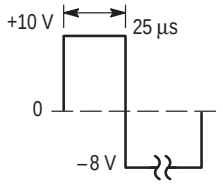


Figure 10. Capacitance

Table 1. Test Conditions for Dynamic Performance

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 µH/20 A L_{coil} = 200 µH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 15 Ω D1 = 1N5820 or Equiv. R_B = Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 ADJUSTED TO OBTAIN I_C $t_1 \approx \frac{L_{coil}(I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{CM})}{V_{clamp}}$ Test Equipment Scope–Tektronics 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

APPLICATIONS INFORMATION FOR SWITCHMODE SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn–on and turn–off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn–on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage–current conditions that can be sustained during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN–719, AN–767.

VOLTAGE REQUIREMENTS (continued)

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn–off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn–on and within the reverse bias SOA curve during turn–off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.
(2) The turn–on time does not exceed 10 µs (see standard pulsed forward SOA curves in Figure 1).
(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 8 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base–emitter junction during turn–off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

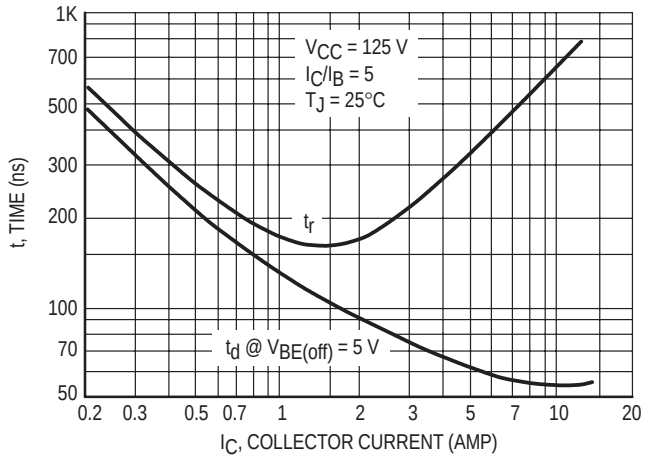


Figure 11. Turn–On Time

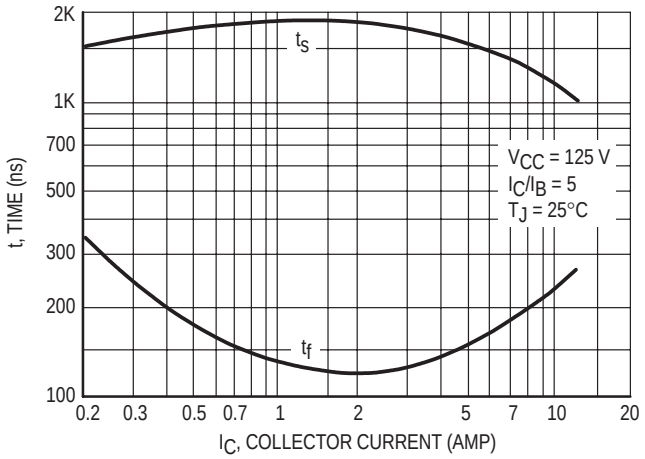


Figure 12. Turn–Off Time

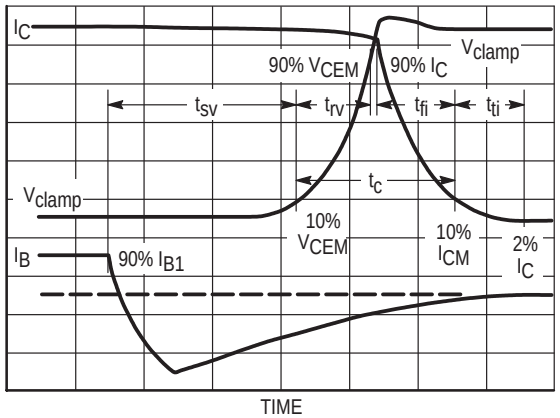


Figure 13. Inductive Switching Measurements

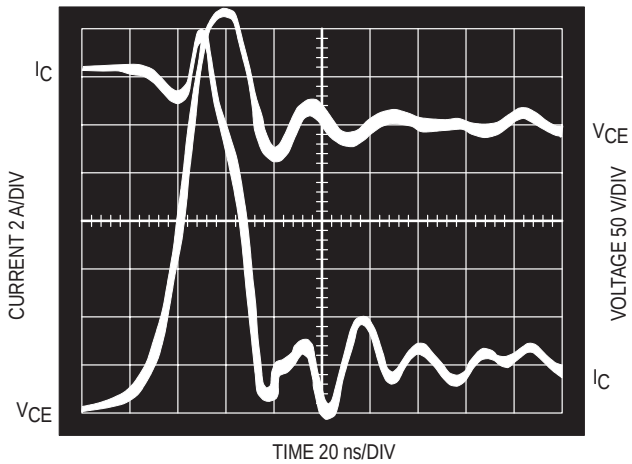


Figure 14. Typical Inductive Switching Waveforms (at 300 V and 12 A with I_{B1} = 2.4 A and $V_{BE(off)}$ = 5 V)

Table 2. Applications Examples of Switching Circuits

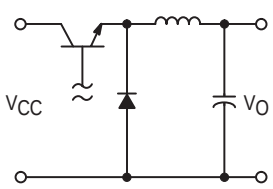
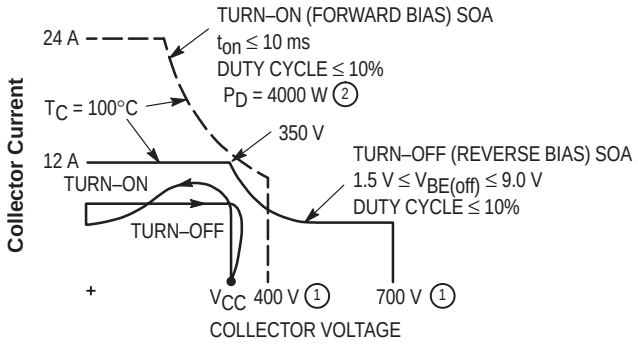
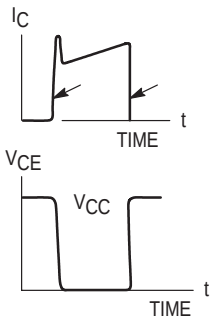
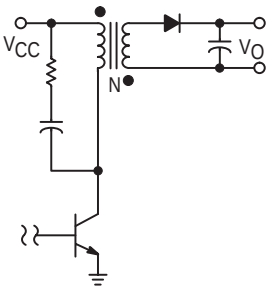
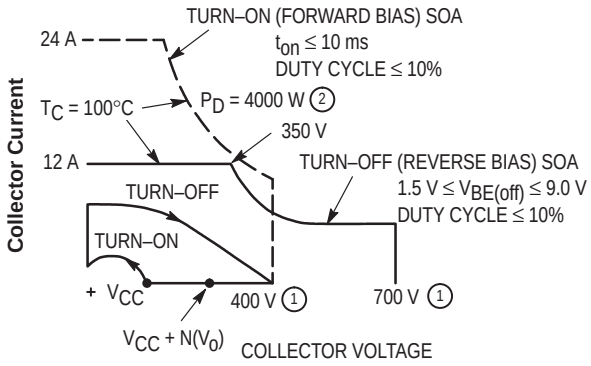
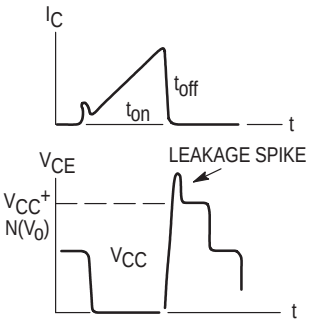
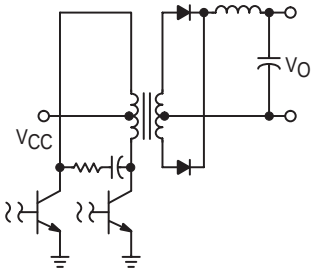
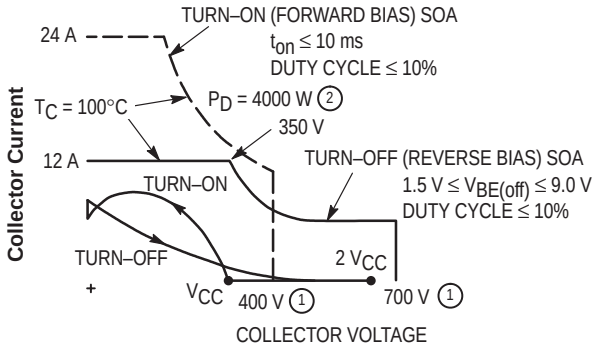
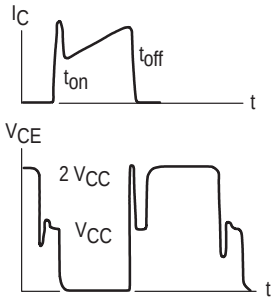
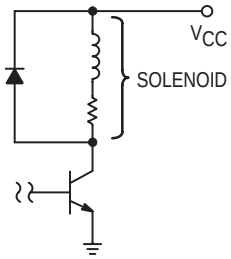
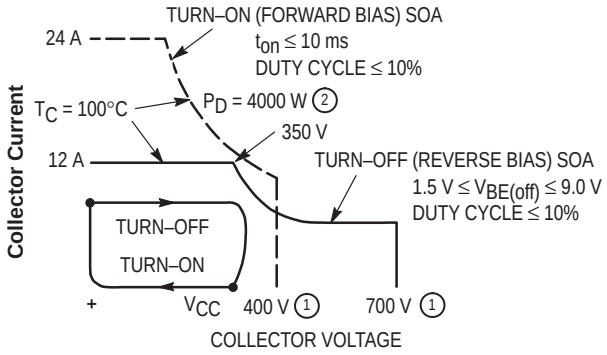
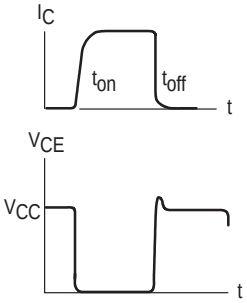
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 		
B	**RINGING CHOKE INVERTER** 		
C	**PUSH–PULL INVERTER/CONVERTER** 		
D	**SOLENOID DRIVER** 		

Table 3. Typical Inductive Switching Performance

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
3	25 100	770 1000	100 230	150 160	200 200	240 320
5	25 100	630 820	72 100	26 55	10 30	100 180
8	25 100	720 920	55 70	27 50	2 8	77 120
12	25 100	640 800	20 32	17 24	2 4	41 54

NOTE: All Data recorded In the Inductive Switching Circuit In Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CEM}
t_{rv} = Voltage Rise Time, 10–90% V_{CEM}
t_{fi} = Current Fall Time, 90–10% I_{CM}
t_{ti} = Current Tail, 10–2% I_{CM}
t_c = Crossover Time, 10% V_{CEM} to 10% I_{CM}

An enlarged portion of the turn–off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

Complementary Silicon Plastic Power Transistors

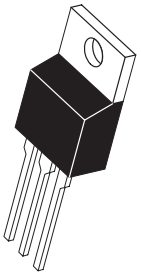
. . . designed for use as high–frequency drivers in audio amplifiers.

- DC Current Gain Specified to 4.0 Amperes
  h_{FE} = 40 (Min) @ I_C = 3.0 Adc
  = 20 (Min) @ I_C = 4.0 Adc
- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 120 Vdc (Min) — MJE15028, MJE15029
  = 150 Vdc (Min) — MJE15030, MJE15031
- High Current Gain — Bandwidth Product
  f_T = 30 MHz (Min) @ I_C = 500 mAdc
- TO–220AB Compact Package

NPN
MJE15028*
MJE15030*
PNP
MJE15029*
MJE15031*

***Motorola Preferred Device**

8 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
120 – 150 VOLTS
50 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	MJE15028 MJE15029	MJE15030 MJE15031	Unit
Collector–Emitter Voltage	V_{CEO}	120	150	Vdc
Collector–Base Voltage	V_{CB}	120	150	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous — Peak	I_C	8.0 16		Adc
Base Current	I_B	2.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.40		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

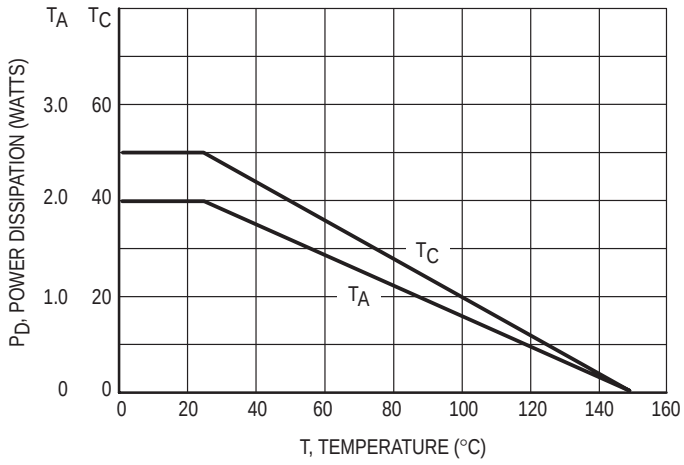


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	MJE15028, MJE15029 MJE15030, MJE15031	$V_{CEO(sus)}$	 120 150	 — —	Vdc
Collector Cutoff Current (V_{CE} = 120 Vdc, I_B = 0) (V_{CE} = 150 Vdc, I_B = 0)	MJE15028, MJE15029 MJE15030, MJE15031	I_{CEO}	 — —	 0.1 0.1	mAdc
Collector Cutoff Current (V_{CB} = 120 Vdc, I_E = 0) (V_{CB} = 150 Vdc, I_E = 0)	MJE15028, MJE15029 MJE15030, MJE15031	I_{CBO}	 — —	 10 10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	10	μAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 2.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	 40 40 40 20	 — — — —	—
DC Current Gain Linearity (V_{CE} From 2.0 V to 20 V, I_C From 0.1 A to 3 A) (NPN TO PNP)		h_{FE}	**Typ** 2 3		
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	—	0.5	Vdc
Base–Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 2.0 Vdc)		$V_{BE(on)}$	—	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain — Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	30	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.

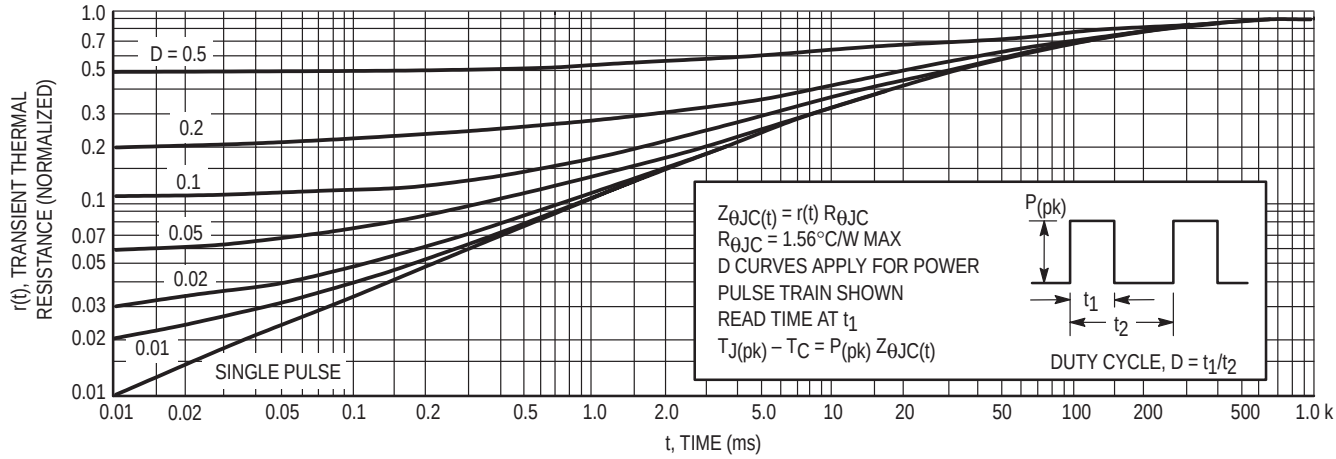


Figure 2. Thermal Response

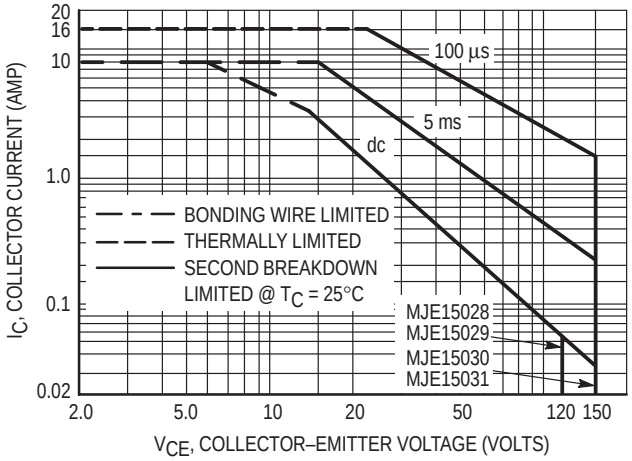


Figure 3. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figures 3 and 4 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

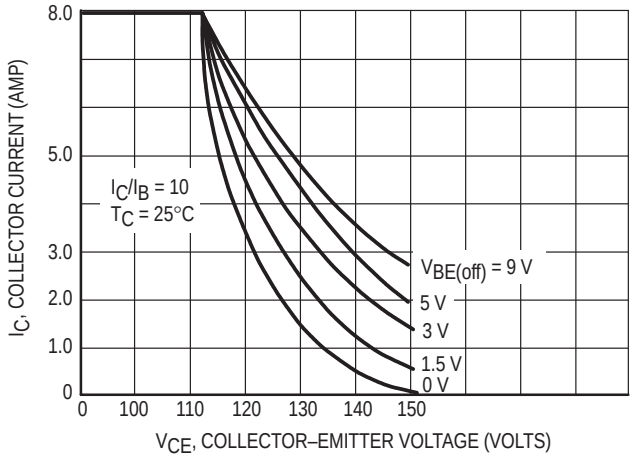


Figure 4. Reverse–Bias Switching Safe Operating Area

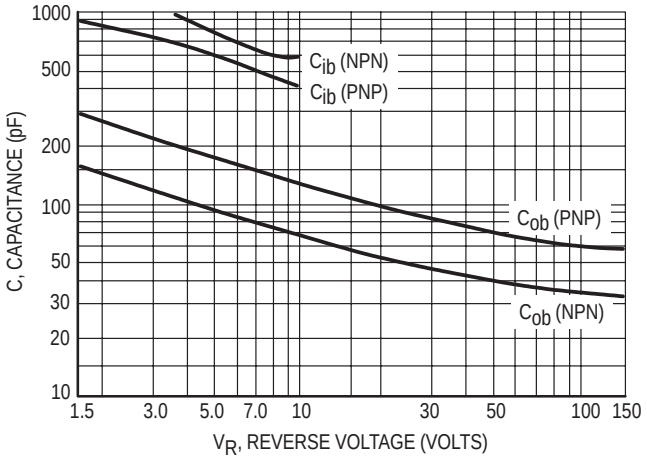


Figure 5. Capacitances

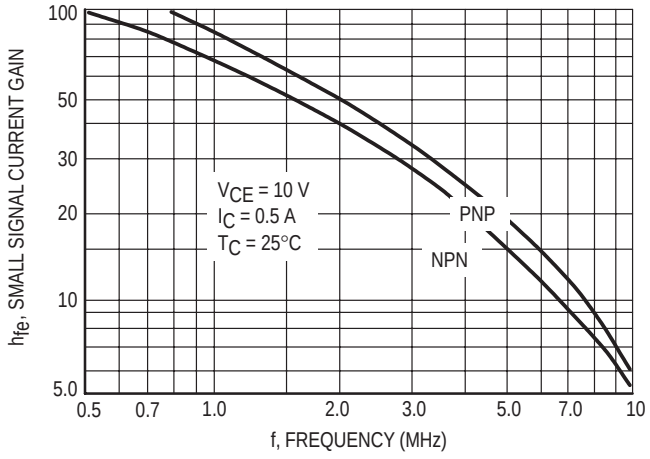


Figure 6. Small–Signal Current Gain

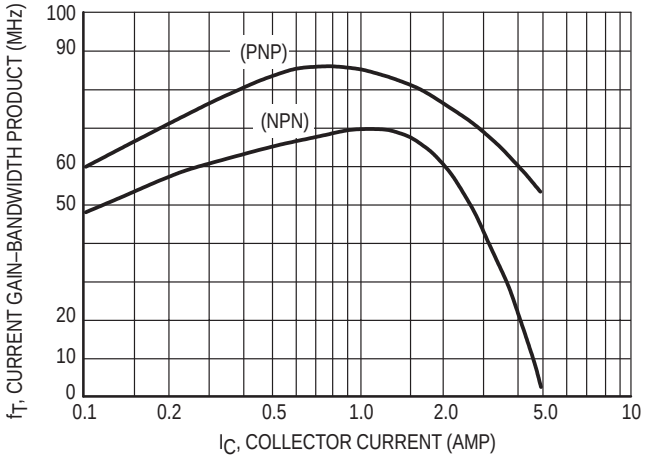
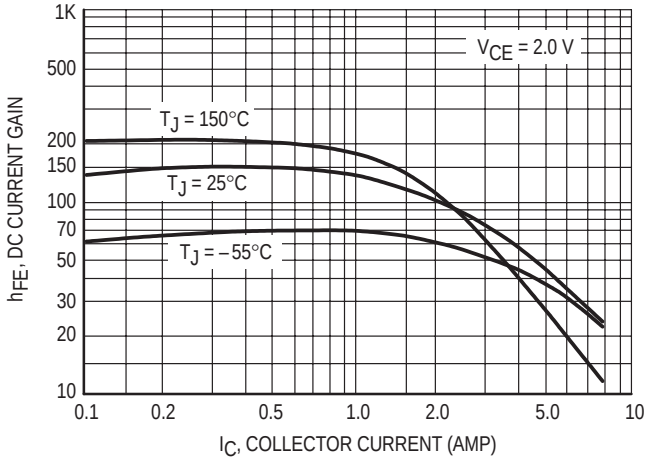


Figure 7. Current Gain–Bandwidth Product

NPN — MJE15028 MJE15030



PNP — MJE15029 MJE15031

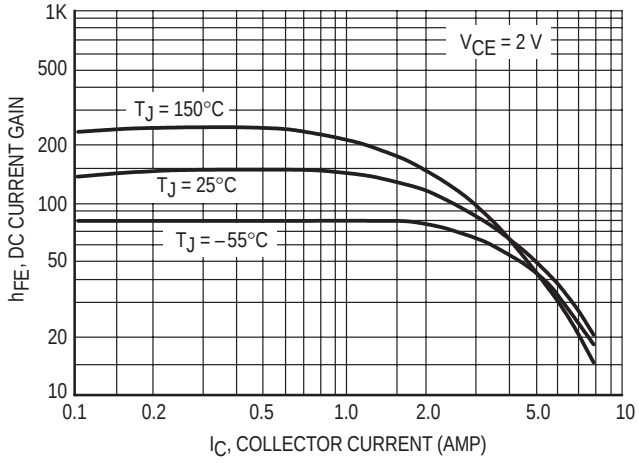
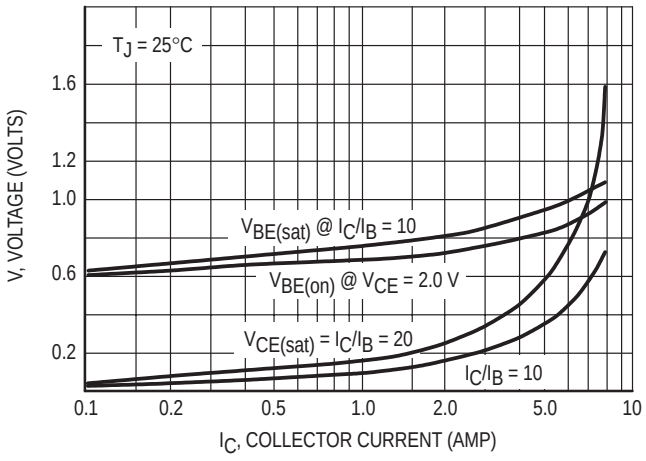


Figure 8. DC Current Gain

NPN



PNP

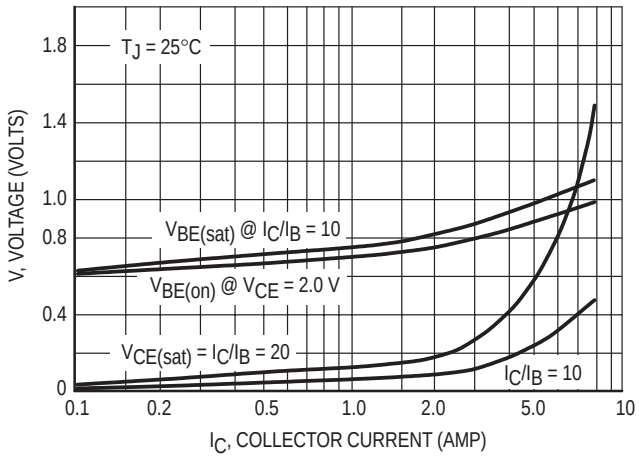


Figure 9. “On” Voltage

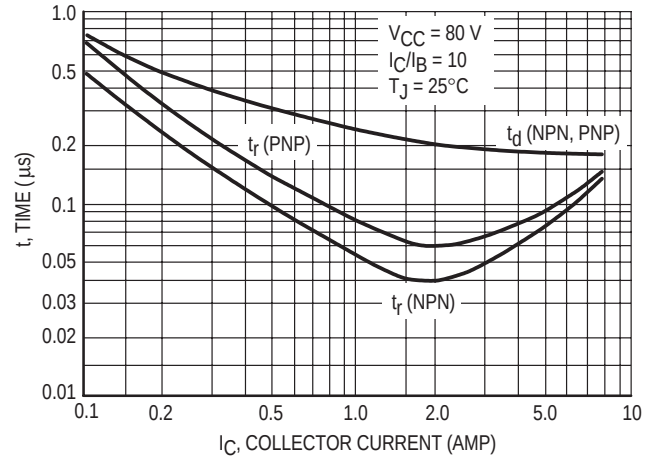


Figure 10. Turn–On Times

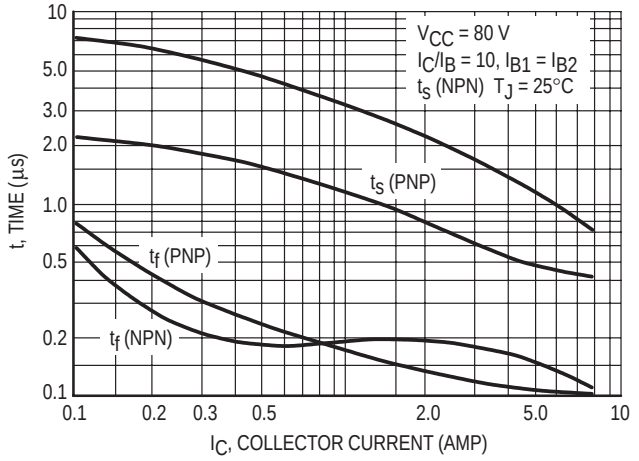


Figure 11. Turn–Off Times

MJE16002*
MJE16004*

*Motorola Preferred Device

Designer's™ Data Sheet

SWITCHMODE Series
NPN Silicon Power Transistors

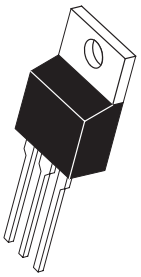
5.0 AMPERE
NPN SILICON
POWER TRANSISTORS
450 VOLTS
80 WATTS

These transistors are designed for high–voltage, high–speed switching of inductive circuits where fall time and RBSOA are critical. They are particularly well–suited for line–operated switchmode applications.

The MJE16004 is a high–gain version of the MJE16002 and MJH16002 for applications where drive current is limited.

Typical Applications:

- Switching Regulators
- High Resolution Deflection Circuits
- Inverters
- Motor Drives
- Fast Switching Speeds
  - 50 ns Inductive Fall Time @ 75°C (Typ)
  - 70 ns Crossover Time @ 75°C (Typ)
- 100°C Performance Specified for:
  - Reverse–Biased SOA
  - Inductive Switching Times
  - Saturation Voltages
  - Leakage Currents



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO(sus)}$	450	Vdc
Collector–Emitter Voltage	V_{CEV}	850	Vdc
Emitter–Base Voltage	V_{EB}	6.0	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5.0 10	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4.0 8.0	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above T_C = 25°C	P_D	80 32 0.64	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector–Emitter Sustaining Voltage (Table 2) (I_C = 100 mA, I_B = 0)		$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 850 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		I_{CEV}	 — —	 — —	 0.25 1.5	mAdc
Collector Cutoff Current (V_{CE} = 850 Vdc, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	—	—	2.5	mAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc, I_C = 0)		I_{EBO}	—	—	1.0	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 17 or 18			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 19			
ON CHARACTERISTICS (1)						
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 1.5 Adc, I_B = 0.2 Adc)	MJE16002		—	—	1.0	
(I_C = 1.5 Adc, I_B = 0.15 Adc)	MJE16004		—	—	1.0	
(I_C = 3.0 Adc, I_B = 0.4 Adc)	MJE16002		—	—	2.5	
(I_C = 3.0 Adc, I_B = 0.3 Adc)	MJE16004		—	—	2.5	
(I_C = 3.0 Adc, I_B = 0.4 Adc, T_C = 100°C)	MJE16002		—	—	2.5	
(I_C = 3.0 Adc, I_B = 0.3 Adc, T_C = 100°C)	MJE16004		—	—	2.5	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 3.0 Adc, I_B = 0.4 Adc)	MJE16002		—	—	1.5	
(I_C = 3.0 Adc, I_B = 0.3 Adc)	MJE16004		—	—	1.5	
(I_C = 3.0 Adc, I_S = 0.4 Adc, T_C = 100°C)	MJE16002		—	—	1.5	
(I_C = 3.0 Adc, I_B = 0.3 Adc, T_C = 100°C)	MJE16004		—	—	1.5	
DC Current Gain		h_{FE}				—
(I_C = 5.0 Adc, V_{CE} = 5.0 Vdc)	MJE16002		5.0	—	—	
	MJE16004		7.0	—	—	
DYNAMIC CHARACTERISTICS						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)		C_{ob}	—	—	200	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)	**MJE16002/MJH10002**					
Delay Time	(I_C = 3.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.4 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%) (I_{B2} = 0.8 Adc, R_{B2} = 8.0 Ω)	t_d	—	30	100	ns
Rise Time		t_r	—	100	300	
Storage Time		t_s	—	1000	3000	
Fall Time		t_f	—	60	300	
Storage Time	($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	400	—	
Fall Time		t_f	—	130	—	
Resistive Load (Table 1)	**MJE16004/MJH16004**					
Delay Time	(I_C = 3.0 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.3 Adc, PW = 30 μs, Duty Cycle ≤ 2.0%) (I_{B2} = 0.6 Adc, R_{B2} = 8.0 Ω)	t_d	—	30	100	ns
Rise Time		t_r	—	130	300	
Storage Time		t_s	—	800	2700	
Fall Time		t_f	—	80	350	
Storage Time	($V_{BE(off)}$ = 5.0 Vdc)	t_s	—	250	—	
Fall Time		t_f	—	60	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

$$*\beta_f = \frac{I_C}{I_{B1}}$$

SWITCHING CHARACTERISTICS (continued)

Characteristics			Symbol	Min	Typ	Max	Unit
Inductive Load (Table 2) MJE16002							
Storage Time	(I_C = 3.0 Adc, I_{B1} = 0.4 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	500	1600	ns
Fall Time			t_{fi}	—	100	200	
Crossover Time			t_c	—	120	250	
Storage Time		(T_J = 150°C)	t_{sv}	—	600	—	
Fall Time			t_{fi}	—	120	—	
Crossover Time			t_c	—	160	—	
Inductive Load (Table 2) MJE16004							
Storage Time	(I_C = 3.0 Adc, I_{B1} = 0.3 Adc, $V_{BE(off)}$ = 5.0 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	400	1300	ns
Fall Time			t_{fi}	—	80	150	
Crossover Time			t_c	—	90	200	
Storage Time		(T_J = 150°C)	t_{sv}	—	450	—	
Fall Time			t_{fi}	—	100	—	
Crossover Time			t_c	—	110	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

$$*\beta_f = \frac{I_C}{I_{B1}}$$

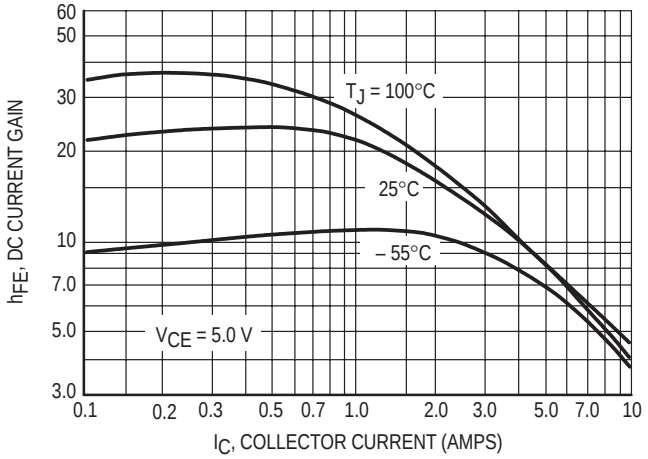


Figure 1. DC Current Gain

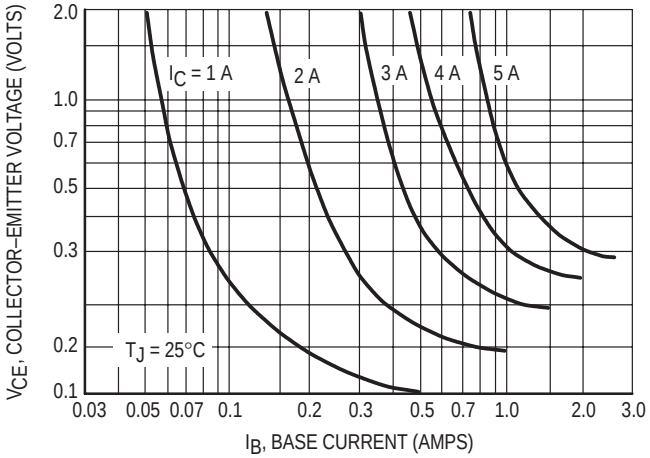


Figure 2. Collector Saturation Region

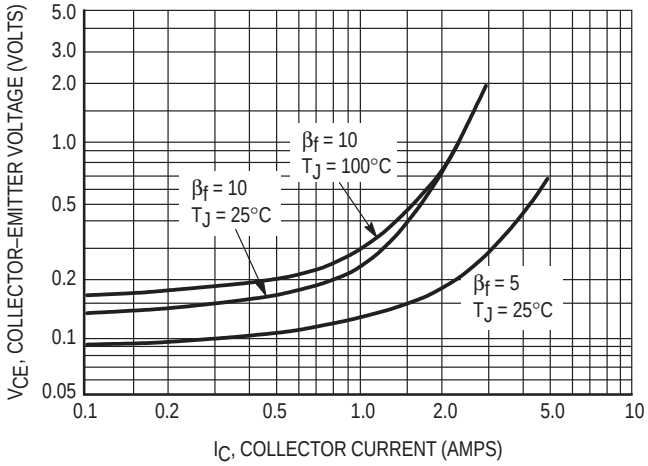


Figure 3. Collector–Emitter Saturation Region

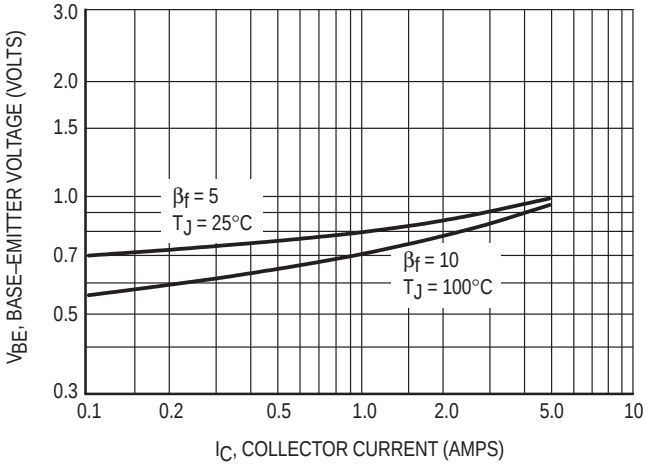


Figure 4. Base–Emitter Voltage

TYPICAL STATIC CHARACTERISTICS (continued)

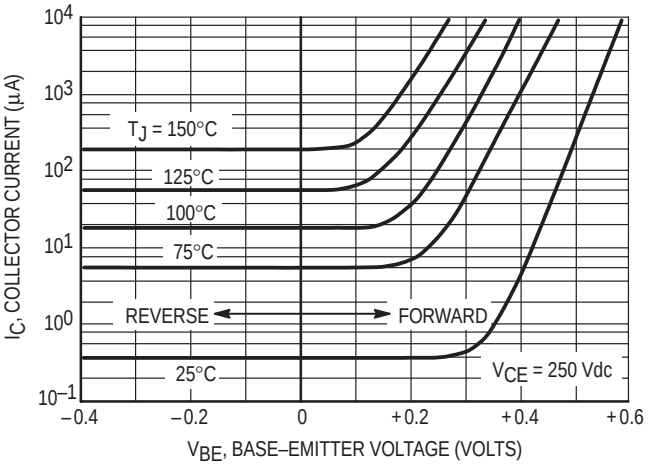


Figure 5. Collector Cutoff Region

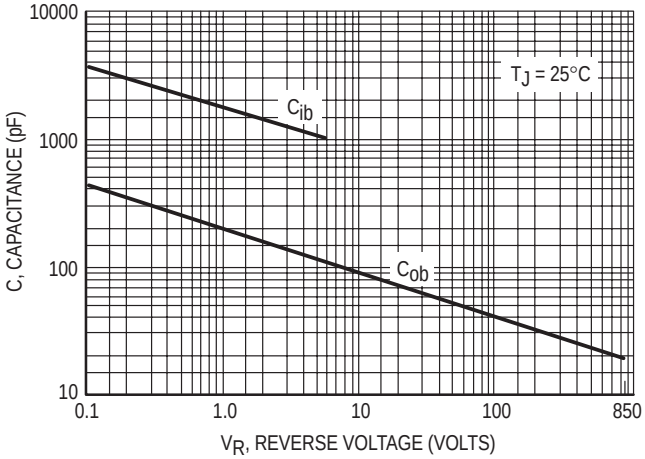


Figure 6. Capacitance

TYPICAL DYNAMIC CHARACTERISTICS

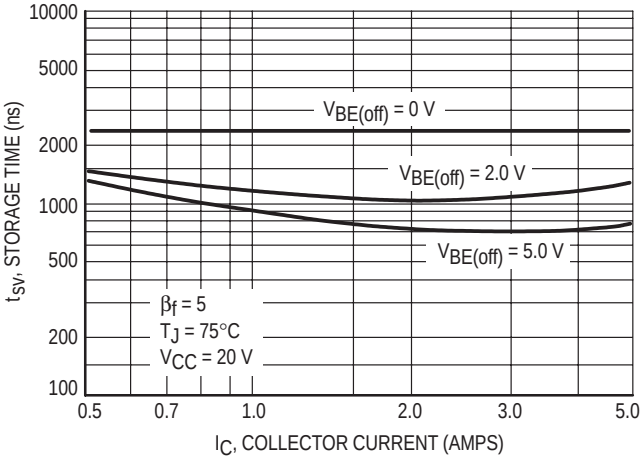


Figure 7. Storage Time

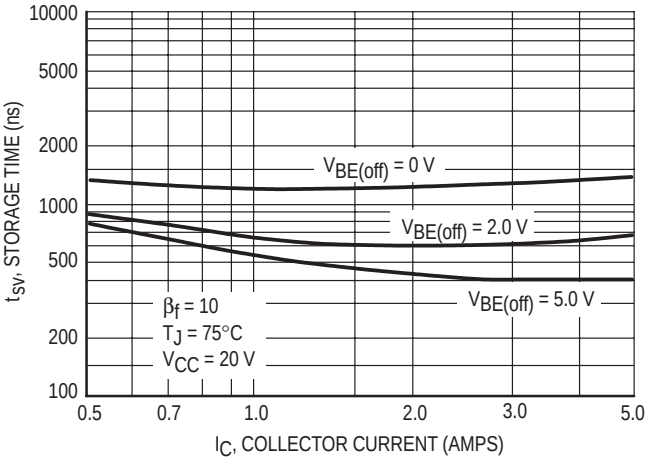


Figure 8. Storage Time

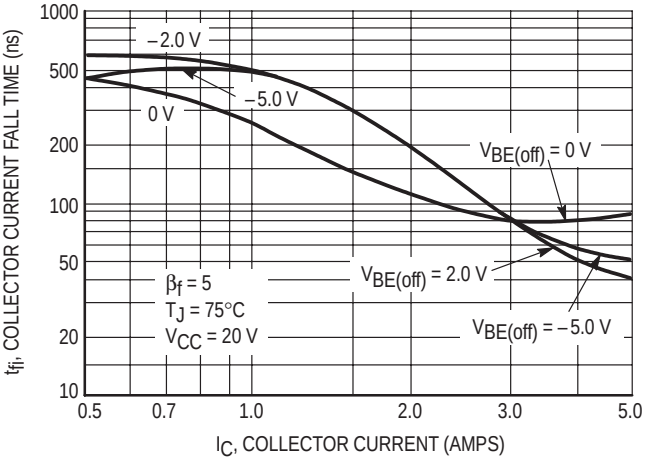


Figure 9. Collector Current Fall Time

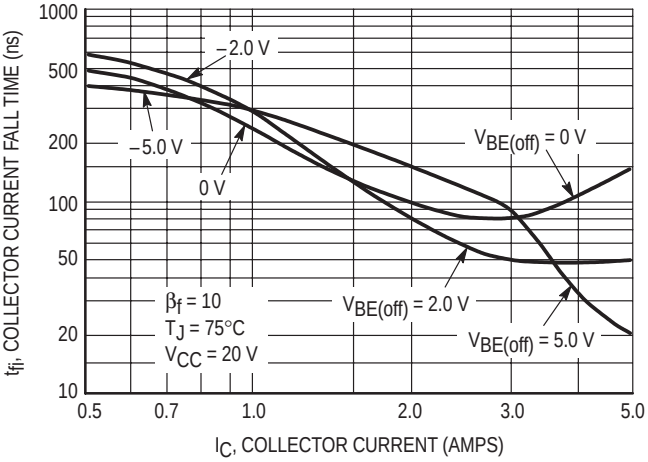


Figure 10. Collector Current Fall Time

TYPICAL DYNAMIC CHARACTERISTICS (continued)

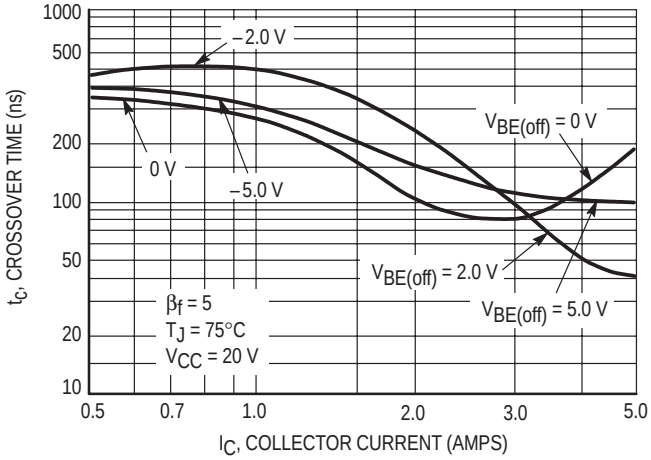


Figure 11. Crossover Time

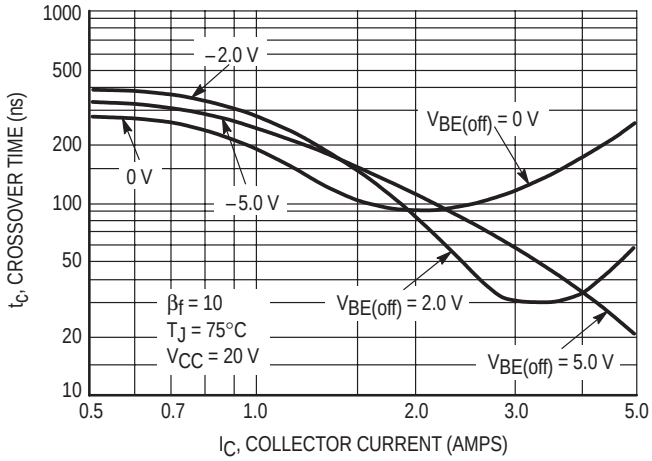


Figure 12. Crossover Time

TYPICAL ELECTRICAL CHARACTERISTICS

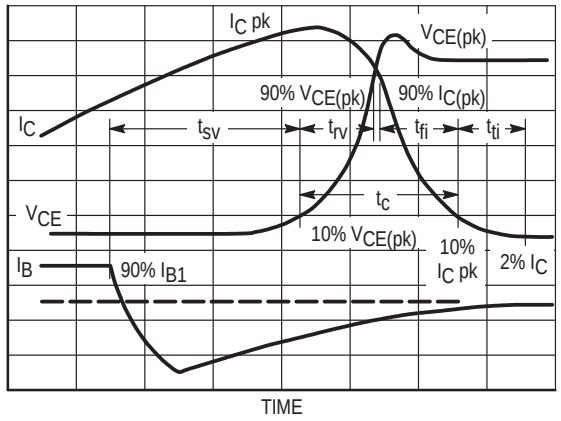


Figure 13. Inductive Switching Measurements

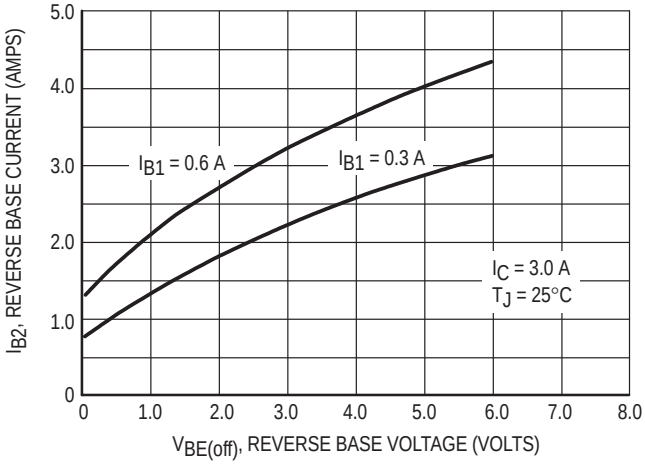


Figure 14. Peak Reverse Base Current

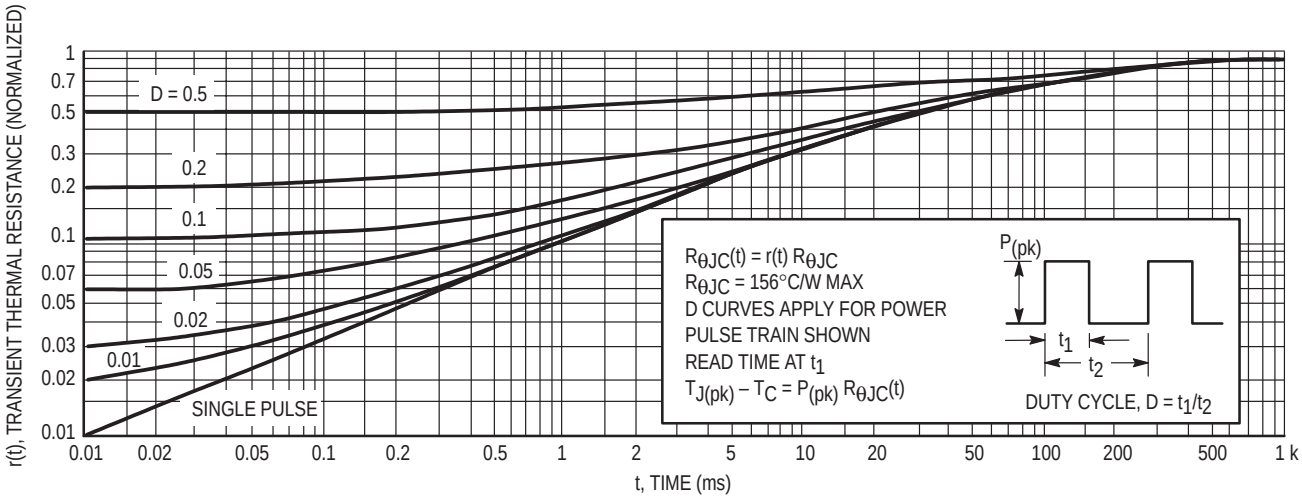


Figure 15. Thermal Response (MJE16002 and MJE16004)

SAFE OPERATING AREA INFORMATION

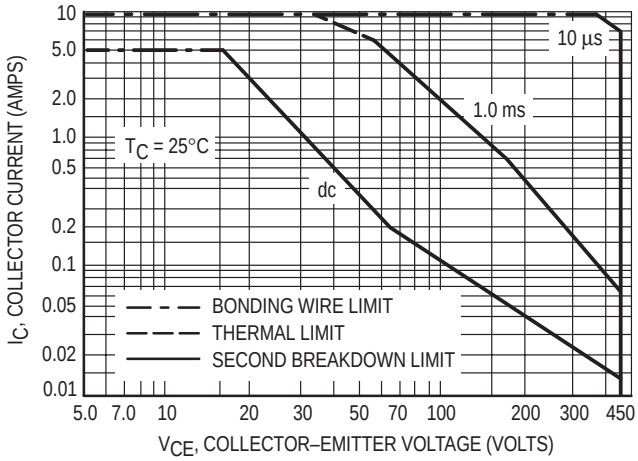


Figure 16. Maximum Rated Forward Bias Safe Operating Area (MJE16002 and MJE16004)

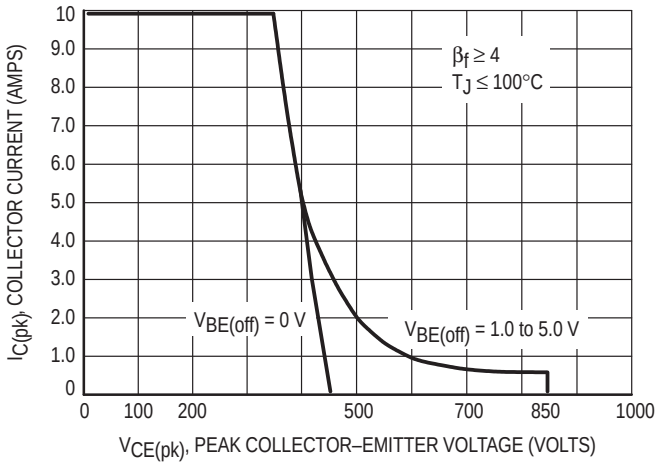


Figure 17. Maximum Rated Reverse Bias Safe Operating Area

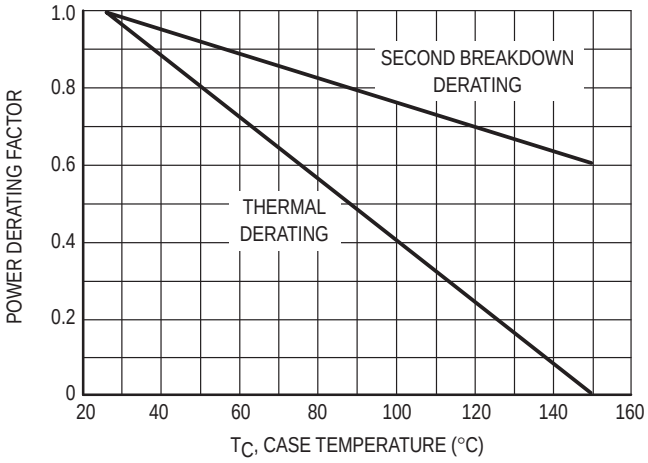


Figure 18. Power Derating

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 16 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 17 and 18 may be found at any case temperature by using the appropriate curve on Figure 20.

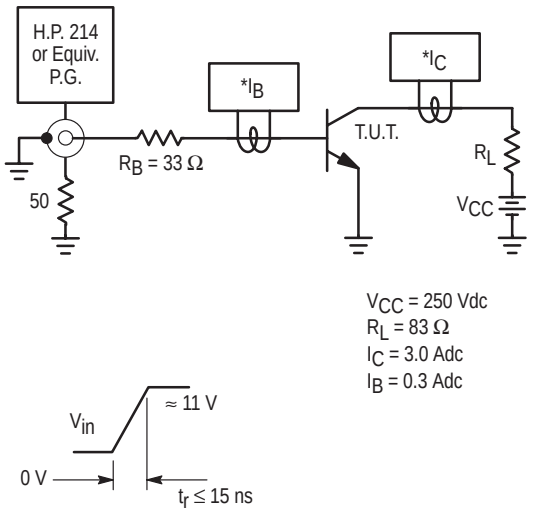
$T_{J(pk)}$ may be calculated from the data in Figure 15. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe 0perating Area and represents the voltage–current condition allowable pulling reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 17 gives the RBSOA characteristics.

Table 1. Resistive Load Switching

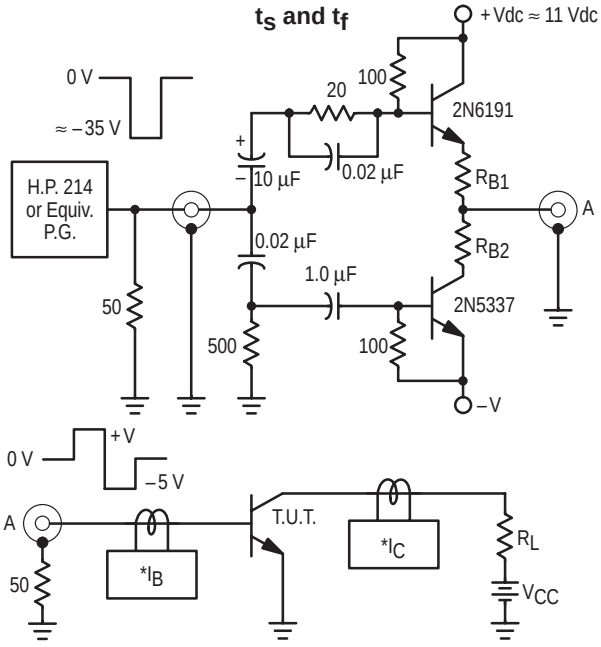
t_d and t_r



V_{CC} = 250 Vdc
R_L = 83 Ω
I_C = 3.0 Adc
I_B = 0.3 Adc

*Tektronix
P–6042 or
Equivalent

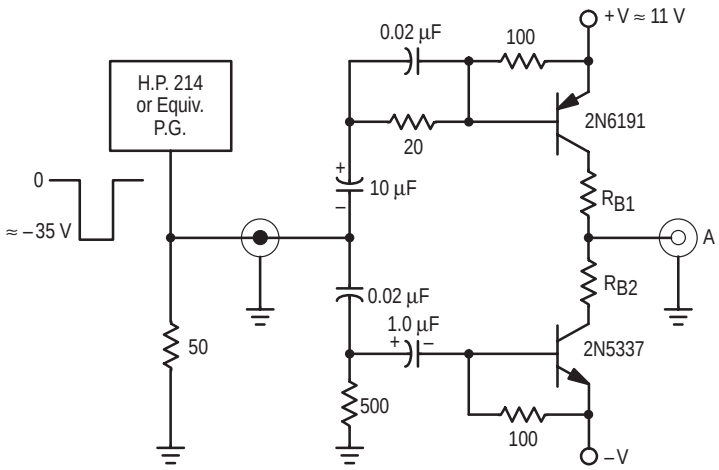
t_s and t_f

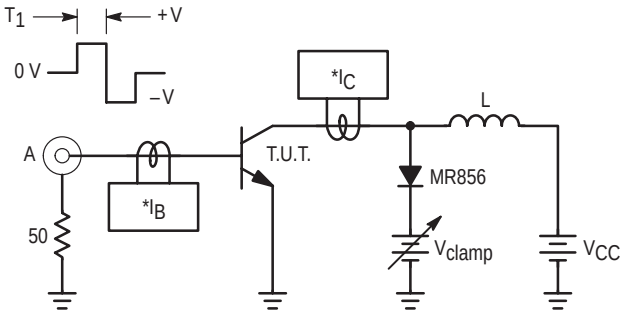


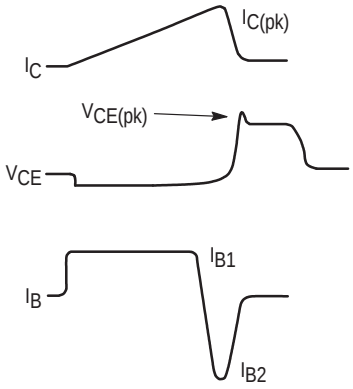
V_{CC} = 250	I_{B1} = 0.3 Adc	R_{B1} = 33 Ω
R_L = 83 Ω	I_{B2} = 0.6 Adc	R_{B2} = 8.0 Ω
I_C = 3.0 Adc	For $V_{BE(off)}$ = 5.0 V	R_{B2} = 0 Ω

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

Table 2. Inductive Load Switching







$T_1 \approx \frac{L_{coil}\ (I_{Cpk})}{V_{CC}}$

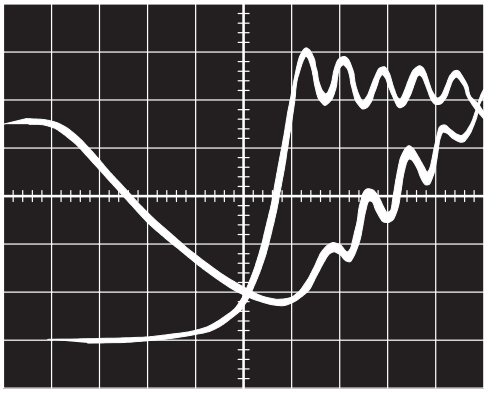
T_1 adjusted to obtain $I_{C(pk)}$

$V_{CEO(sus)}$	**Inductive Switching**	**RBSOA**
L = 10 mH	L = 200 µH	L = 200 µH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 20 Volts	V_{CC} = 20 Volts
	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}
*Tektronix P–6042 or Equivalent	Scope — Tektronix 7403 or Equivalent	

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

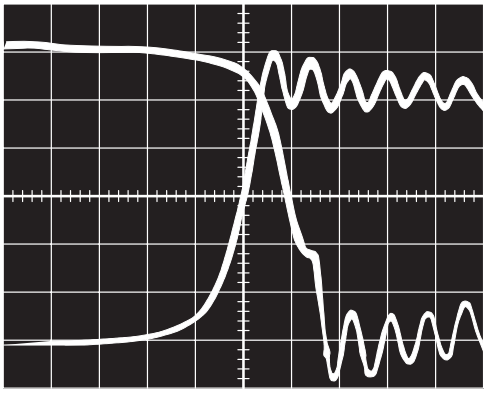
TYPICAL INDUCTIVE SWITCHING WAVEFORMS

t_{sv}



$I_{C(pk)}$ = 3.0 Amps
I_{B1} = 0.3 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 300 Volts
T_C = 25°C
Time Base = 20 ns/cm

t_{fi}, t_c



$I_{C(pk)}$ = 3.0 Amps
I_{B1} = 0.3 Amp
$V_{BE(off)}$ = 5.0 Volts
$V_{CE(pk)}$ = 300 Volts
T_C = 25°C
Time Base = 20 ns/cm

MJE16106

Designer's™ Data Sheet

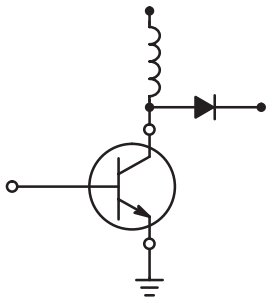
NPN Silicon Power Transistor

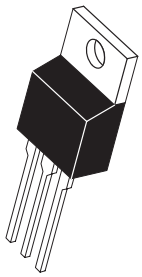
Switchmode Bridge Series

POWER TRANSISTORS
8 AMPERES
400 VOLTS
100 AND 125 WATTS

. . . specifically designed for use in half bridge and full bridge off line converters.

- Excellent Dynamic Saturation Characteristics
- Rugged RBSOA Capability
- Collector–Emitter Sustaining Voltage — $V_{CEO(sus)}$ — 400 V
- Collector–Emitter Breakdown — $V_{(BR)CES}$ — 650 V
- State–of–Art Bipolar Power Transistor Design
- Fast Inductive Switching:
  - t_{fi} = 30 ns (Typ) @ 100°C
  - t_c = 65 ns (Typ) @ 100°C
  - t_{sv} = 1.3 μs (Typ) @ 100°C
- Ultrafast FBSOA Specified
- 100°C Performance Specified for:
  - RBSOA
  - Inductive Load Switching
  - Saturation Voltages
  - Leakages





CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	$V_{CEO(sus)}$	400	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	650	Vdc
Emitter–Base Voltage	V_{EBO}	6	Vdc
Collector Current — Continuous — Pulsed (1)	I_C I_{CM}	8 16	Adc
Base Current — Continuous — Pulsed (1)	I_B I_{BM}	6 12	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derated above 25°C	P_D	100 40 0.8	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	–55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.25	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)							
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 20 mAdc, I_B = 0)			$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current (V_{CE} = 650 Vdc, $V_{BE(off)}$ = 1.5 V) (V_{CE} = 650 Vdc, $V_{BE(off)}$ = 1.5 V, T_C = 100°C)			I_{CEV}	 — —	 — —	 100 1000	μAdc
Collector Cutoff Current (V_{CE} = 650 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	—	1000	μAdc
Emitter–Base Leakage (V_{EB} = 6.0 Vdc, I_C = 0)			I_{EBO}	—	—	10	μAdc
ON CHARACTERISTICS (1)							
Collector–Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 0.25 Adc) (I_C = 5.0 Adc, I_B = 0.5 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)			$V_{CE(sat)}$	 — — — —	 0.2 0.4 0.2 0.3	 0.9 2.0 1.0 1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 1.0 Adc) (I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)			$V_{BE(sat)}$	 — —	 0.9 0.8	 1.5 1.5	Vdc
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 5.0 Vdc)			h_{FE}	6	13	22	—
DYNAMIC CHARACTERISTICS							
Dynamic Saturation			$V_{CE(dsat)}$	See Figures 11, 12, and 13			V
Output Capacitance (V_{CE} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz)			C_{ob}	—	—	300	pF
SWITCHING CHARACTERISTICS							
Inductive Load (Table 1)							
Storage	I_C = 5.0 A, I_{B1} = 0.5 A, $V_{BE(off)}$ = 5 V, $V_{CE(pk)}$ = 250 V	T_J = 25°C	t_{sv}	—	950	2000	ns
Crossover			t_c	—	45	150	
Fall Time			t_{fi}	—	20	75	
Storage		T_J = 100°C	t_{sv}	—	1300	2600	
Crossover			t_c	—	65	200	
Fall Time			t_{fi}	—	30	125	
Resistive Load (Table 2)							
Delay Time	I_C = 5.0 A, I_{B1} = 0.5 A, V_{CC} = 250 V, PW = 30 μs, Duty Cycle = ≤ 2.0%	I_{B2} = 1.0 A	t_d	—	30	—	ns
Rise Time			t_r	—	200	—	
Storage Time			t_s	—	1800	—	
Fall Time			t_f	—	100	—	
Storage Time		$V_{BE(off)}$ = 5 V	t_s	—	1200	—	
Fall Time			t_f	—	70	—	

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL STATIC CHARACTERISTICS

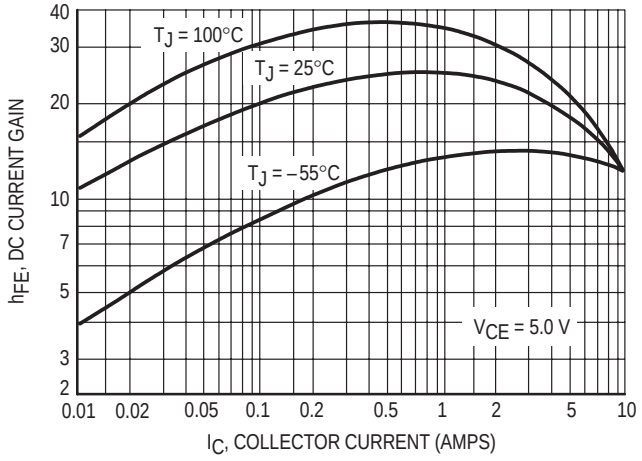


Figure 1. DC Current Gain

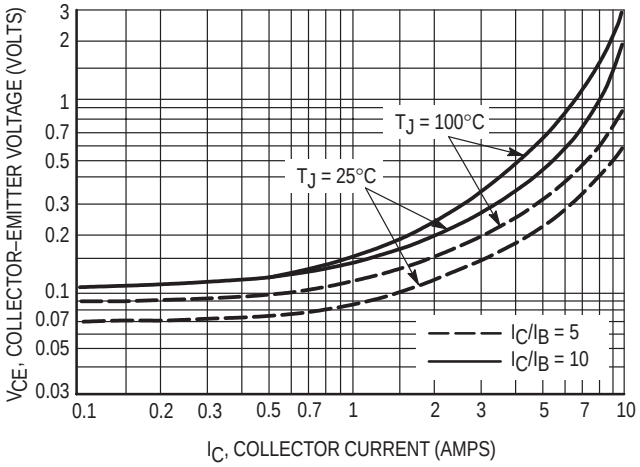


Figure 2. Collector–Emitter Saturation Voltage

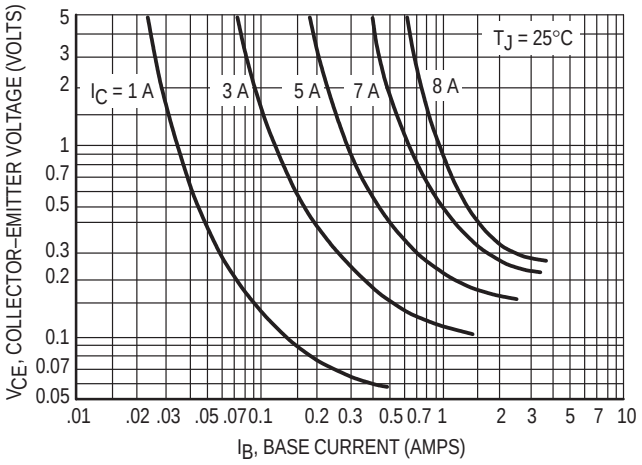


Figure 3. Collector–Emitter Saturation Region

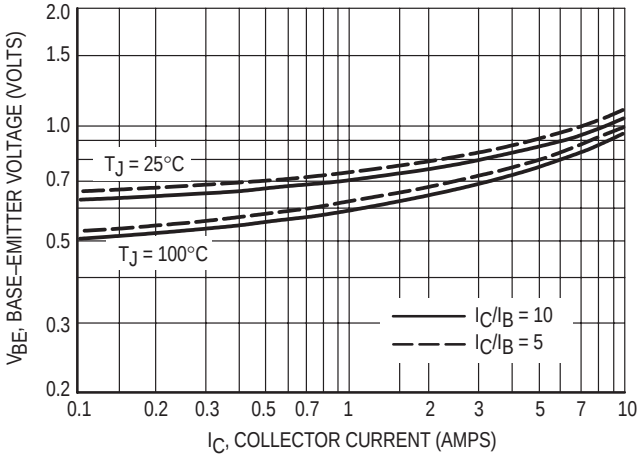


Figure 4. Base–Emitter Saturation Region

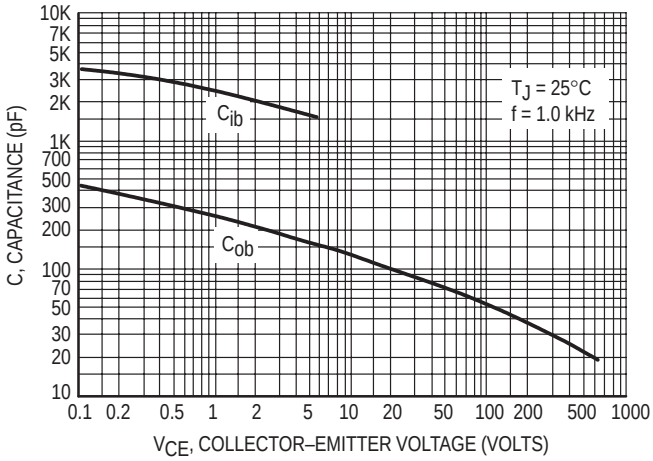


Figure 5. Capacitance

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS
$I_C/I_B = 10$, $T_C = 100°C$, $V_{CE(pk)} = 250$ V

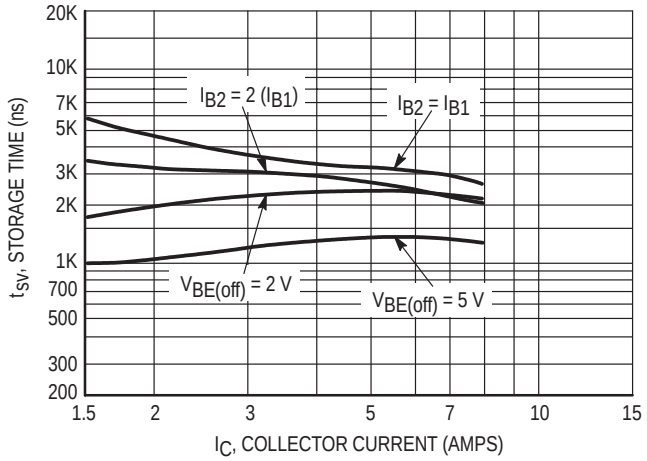


Figure 6. Inductive Storage Time

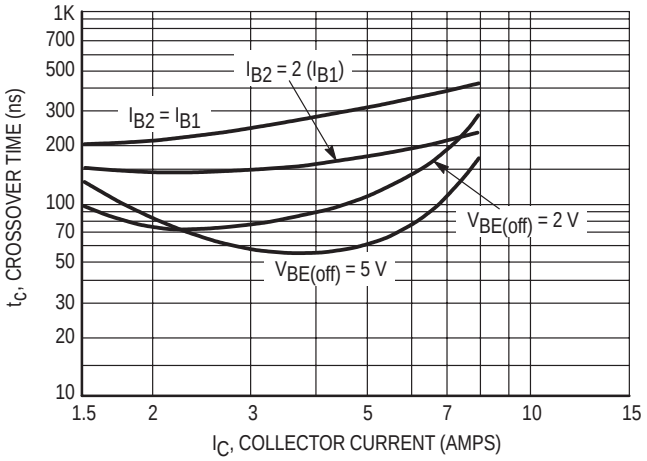


Figure 7. Crossover Time

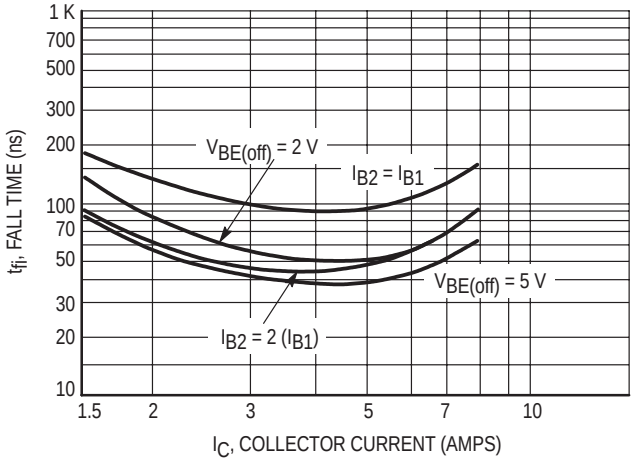


Figure 8. Collector Current Fall Time

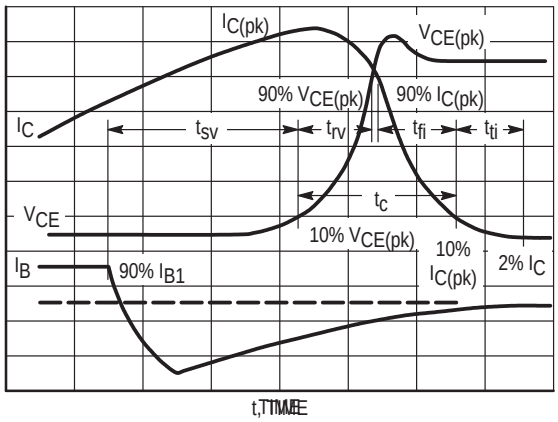


Figure 9. Inductive Switching Measurements

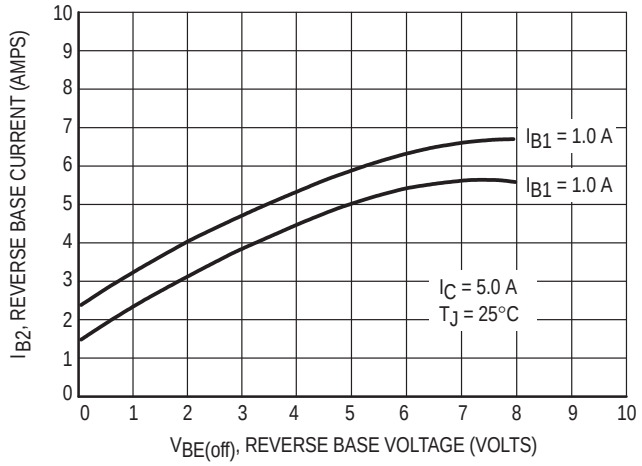
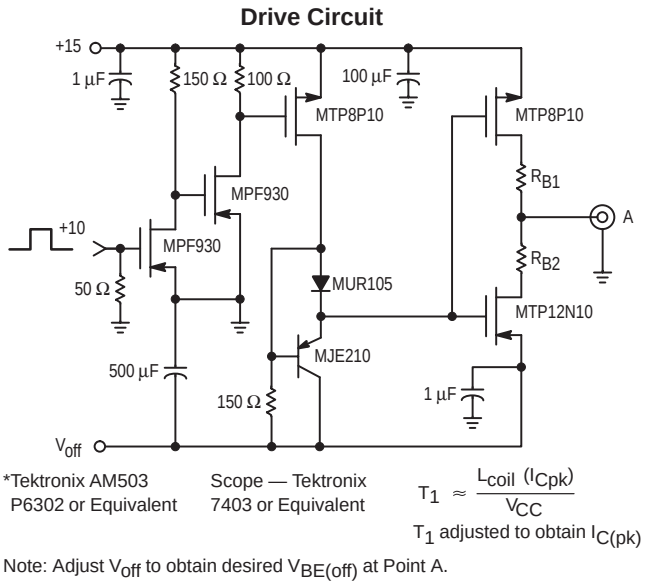


Figure 10. Peak Reverse Base Current

Table 1. Inductive Load Switching



Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A.

$V_{CEO(sus)}$
L = 10 mH
R_{B2} = ∞
V_{CC} = 20 Volts
$I_{C(pk)}$ = 20 mA

Inductive Switching
L = 200 µH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 200 µH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

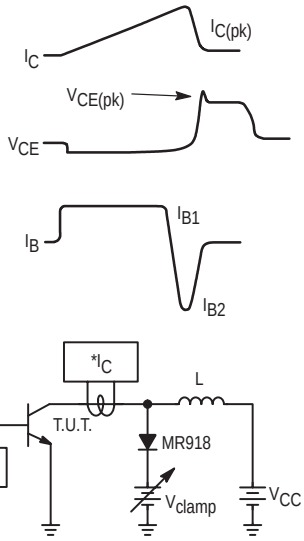
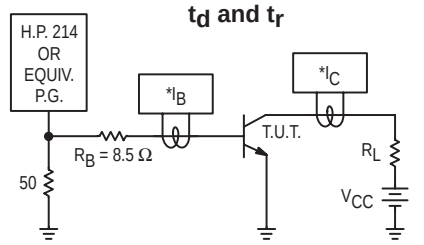
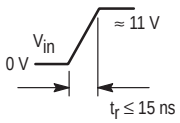


Table 2. Resistive Load Switching

t_d and t_r



V_{CC}	250 Vdc
R_L	25 Ω
I_C	5 A
I_B	0.5 A

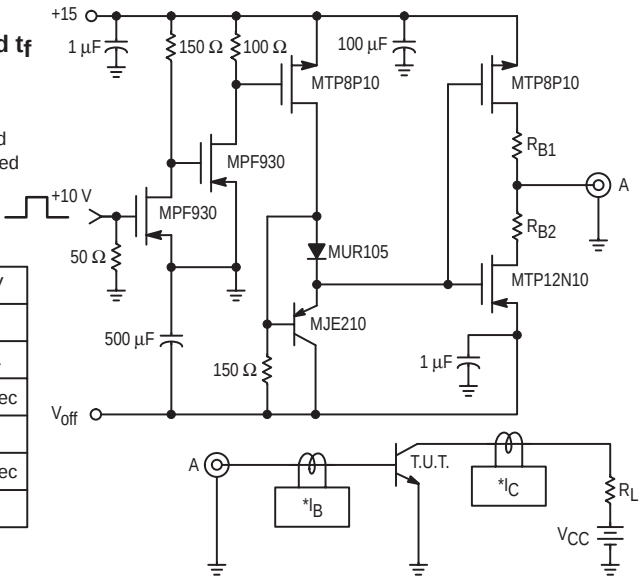


*Tektronix AM503
P6302 or Equivalent

t_s and t_f

$V_{(off)}$ adjusted to give specified off drive

V_{CC}	250 V
I_C	5 A
I_{B1}	0.5 A
I_{B2}	Per Spec
R_{B1}	30 Ω
R_{B2}	Per Spec
R_L	25 Ω



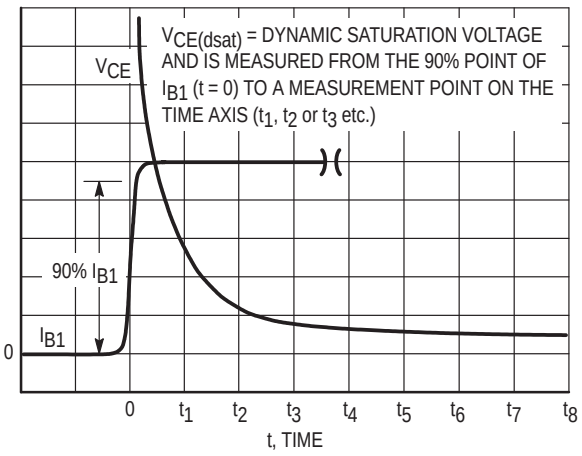


Figure 11. Definition of Dynamic Saturation Measurement

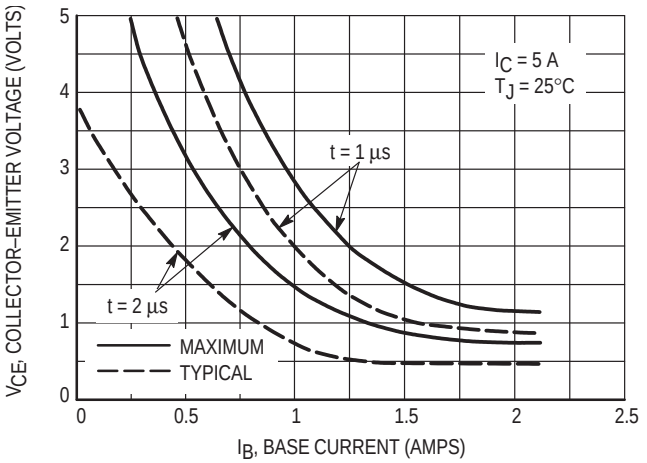


Figure 12. Dynamic Saturation Voltage

DYNAMIC SATURATION VOLTAGE

For bipolar power transistors low DC saturation voltages are achieved by conductivity modulating the collector region. Since conductivity modulation takes a finite amount of time, DC saturation voltages are not achieved instantly at turn–on. In bridge circuits, two transistor forward converters, and two transistor flyback converters dynamic saturation characteristics are responsible for the bulk of dynamic losses. The MJE16106 has been designed specifically to minimize these losses. Performance is roughly four times better than the original version of MJ16006.

From a measurement point of view, dynamic saturation voltage is defined as collector–emitter voltage at a specific point in time after I_{B1} has been applied, where t = 0 is the 90% point on the I_{B1} rise time waveform. This definition is illustrated in Figure 11. Performance data was taken in the circuit that is shown in Figure 13. The 24 volt rail allows a Tektronix 2445 or equivalent scope to operate at 1 volt per division without input amplifier saturation.

Dynamic saturation performance is illustrated in Figure 12. The MJE16106 reaches DC saturation levels in approximately 2 μs, provided that sufficient base drive is provided. The dependence of dynamic saturation voltage upon base drive suggests a spike of I_{B1} at turn–on to minimize dynamic saturation losses, and also avoid overdrive at turn–off. However, in order to simulate worst case conditions the guaranteed dynamic saturation limits in this data sheet are specified with a constant level of I_{B1}.

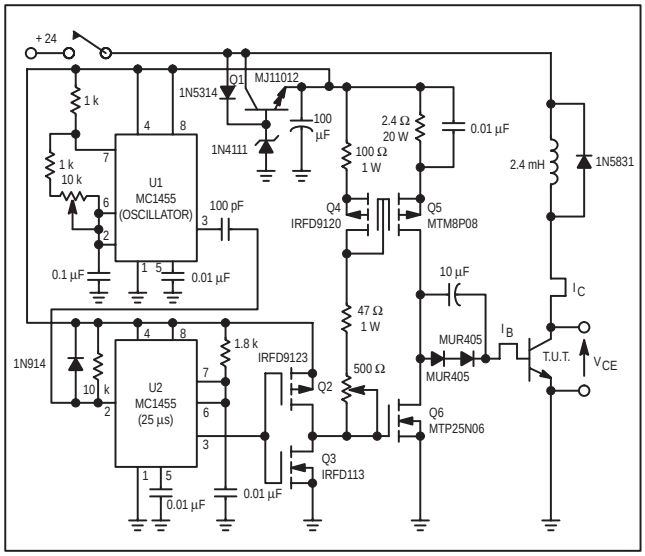


Figure 13. Dynamic Saturation Test Circuit

GUARANTEED SAFE OPERATING AREA INFORMATION

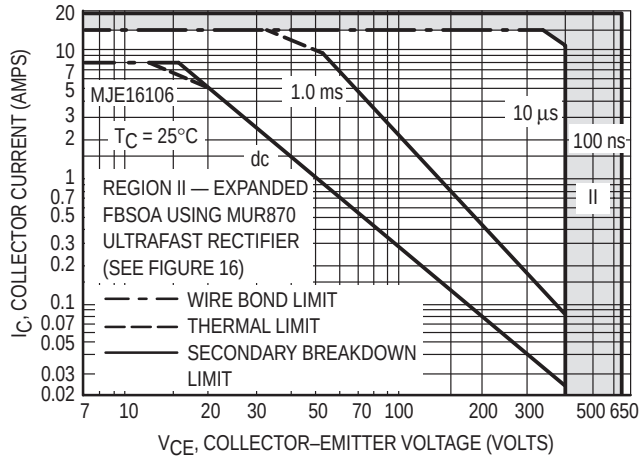


Figure 14. Maximum Rated Forward Bias Safe Operating Area

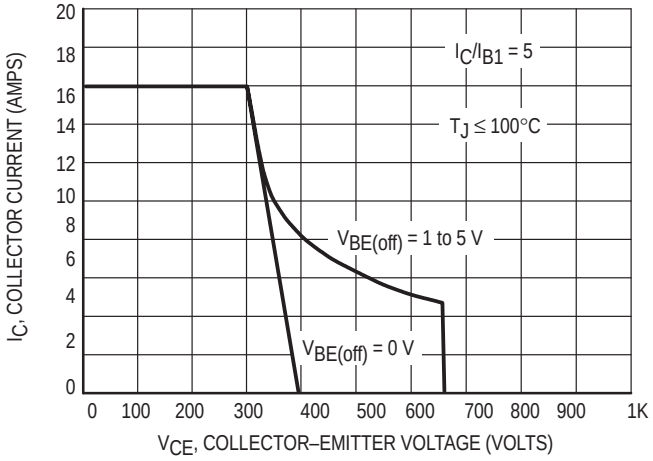


Figure 15. Maximum Rated Reverse Bias Safe Operating Area

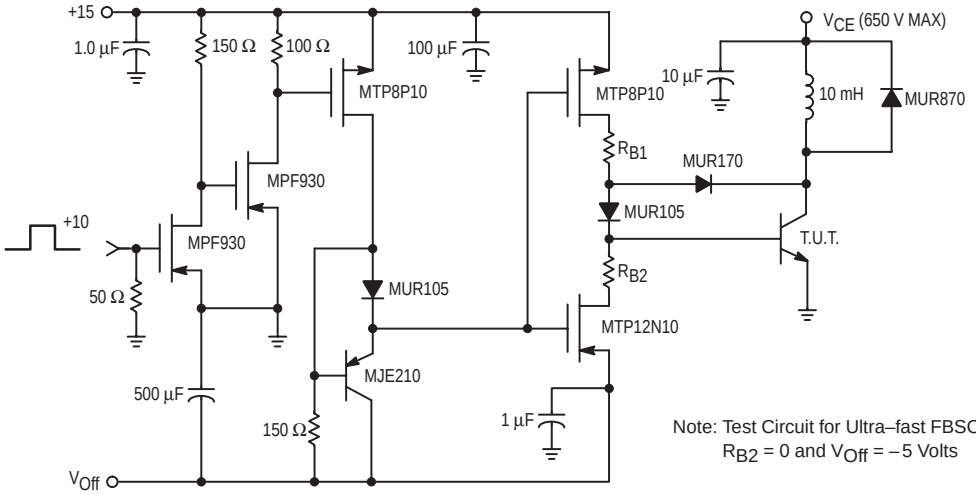


Figure 16. Switching Safe Operating Area

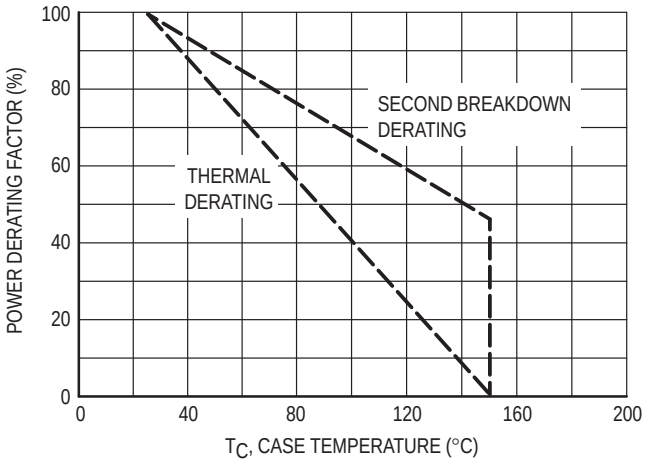


Figure 17. Power Derating

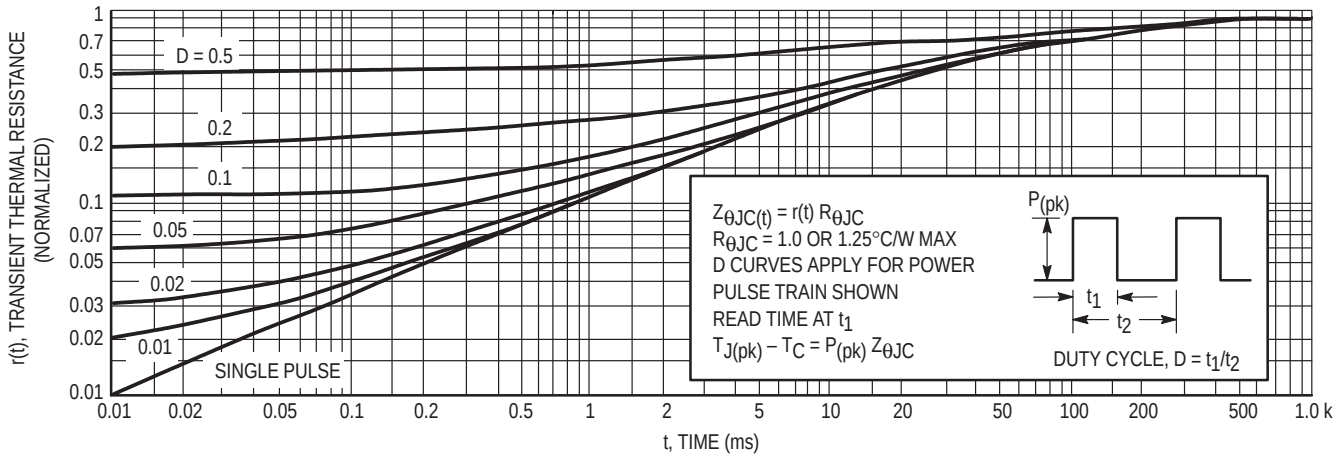


Figure 18. Typical Thermal Response [$Z_{\theta JC}(t)$]

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data in Figure 14 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 14 may be found at any case temperature by using the appropriate curve on Figure 17.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

SWITCHMODE III DESIGN CONSIDERATIONS

FBSOA

Allowable dc power dissipation in bipolar power transistors decreases dramatically with increasing collector–emitter voltage. A transistor which safely dissipates 100 watts at 10 volts will typically dissipate less than 10 watts at its rated $V_{(BR)CEO(sus)}$. From a power handling point of view, current and voltage are not interchangeable (see Application Note AN875).

TURN–ON

Safe turn–on load line excursions are bounded by pulsed FBSOA curves. The 10 μs curve applies for resistive loads, most capacitive loads, and inductive loads that are clamped by standard or fast recovery rectifiers. Similarly, the 100 ns curve applies to inductive loads which are clamped by ultra–fast recovery rectifiers, and are valid for turn–on crossover times less than 100 ns (AN952).

At voltages above 75% of $V_{(BR)CEO(sus)}$, it is essential to provide the transistor with an adequate amount of base drive VERY RAPIDLY at turn–on. More specifically, safe operation according to the curves is dependent upon base current rise time being less than collector current rise time. As a general rule, a base drive compliance voltage in excess of 10 volts is required to meet this condition (see Application Note AN875).

TURN–OFF

A bipolar transistor's ability to withstand turn–off stress is dependent upon its forward base drive. Gross overdrive violates the RBSOA curve and risks transistor failure. For this reason, circuits which use fixed base drive are more likely to fail at light loads due to heavy overdrive (see Application Note AN875).

OPERATION ABOVE $V_{(BR)CEO(sus)}$

When bipolars are operated above collector–emitter breakdown, base drive is crucial. A rapid application of adequate forward base current is needed for safe turn–on, as is a stiff negative bias needed for safe turn–off. Any hiccup in the base–drive circuitry that even momentarily violates either of these conditions will likely cause the transistor to fail. Therefore, it is important to design the driver so that its output is negative in the absence of anything but a clean crisp input signal (see Application Note AN952).

RBSOA

Reversed Biased Safe Operating Area has a first order dependency on circuit configuration and drive parameters. The RBSOA curves in this data sheet are valid only for the conditions specified. For a comparison of RBSOA results in several types of circuits (see Application Note AN951).

DESIGN SAMPLES

Transistor parameters tend to vary much more from wafer lot to wafer lot, over long periods of time, than from one device to the next in the same wafer lot. For design evaluation it is advisable to use transistors from several different date codes.

BAKER CLAMPS

Many unanticipated pitfalls can be avoided by using Baker Clamps. MUR105 and MUR170 diodes are recommended for base drives less than 1 amp. Similarly, MUR405 and MUR470 types are well–suited for higher drive requirements (see Article Reprint AR131).

Designer's™ Data Sheet
SWITCHMODE™
NPN Bipolar Power Transistor For Switching Power Supply Applications

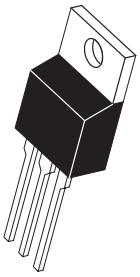
MJE18002*
MJF18002*

*Motorola Preferred Device

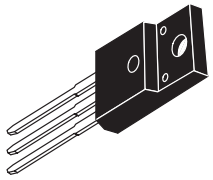
POWER TRANSISTOR
2.0 AMPERES
1000 VOLTS
25 and 50 WATTS

The MJE/MJF18002 have an applications specific state–of–the–art die designed for use in 220 V line operated Switchmode Power supplies and electronic light ballasts. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - — High and Flat DC Current Gain h_{FE}
  - — Fast Switching
  - — No Coil Required in Base Circuit for Turn–Off (No Current Tail)
- Tight Parametric Distributions are Consistent Lot–to–Lot
- Two Package Choices: Standard TO–220 or Isolated TO–220
- MJF18002, Case 221D, is UL Recognized at 3500 V_{RMS}: File #E69369



CASE 221A–06
TO–220AB
MJE18002



CASE 221D–02
ISOLATED TO–220 TYPE
UL RECOGNIZED
MJF18002

MAXIMUM RATINGS

Rating	Symbol	MJE18002	MJF18002	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000		Vdc
Emitter–Base Voltage	V_{EBO}	9.0		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	2.0 5.0		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	1.0 2.0		Adc
RMS Isolated Voltage(2) Test No. 1 Per Fig. 1 (for 1 sec, R.H. < 30%, Test No. 2 Per Fig. 2 T_C = 25°C) Test No. 3 Per Fig. 3	V_{ISOL}	— — —	4500 3500 1500	V
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	50 0.4	25 0.2	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18002	MJF18002	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	5.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0) T_C = 125°C (V_{CE} = 800 V, V_{EB} = 0) T_C = 125°C	I_{CES}	— — —	— — —	100 500 100	μAdc
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

(continued)

(2) Proper strike and creepage distance must be provided.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS								
Base–Emitter Saturation Voltage (I_C = 0.4 Adc, I_B = 40 mAdc) (I_C = 1.0 Adc, I_B = 0.2 Adc)				$V_{BE(sat)}$	— —	0.825 0.92	1.1 1.25	Vdc
Collector–Emitter Saturation Voltage (I_C = 0.4 Adc, I_B = 40 mAdc) @ T_C = 125°C (I_C = 1.0 Adc, I_B = 0.2 Adc) @ T_C = 125°C				$V_{CE(sat)}$	 — — — —	 0.2 0.2 0.25 0.3	 0.5 0.5 0.5 0.6	Vdc
DC Current Gain (I_C = 0.2 Adc, V_{CE} = 5.0 Vdc) @ T_C = 125°C (I_C = 0.4 Adc, V_{CE} = 1.0 Vdc) @ T_C = 125°C (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc) @ T_C = 125°C (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)				h_{FE}	14 — 11 11 6.0 5.0 10	— 27 17 20 8.0 8.0 20	34 — — — — — —	—
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)				f_T	—	13	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)				C_{ob}	—	35	60	pF
Input Capacitance (V_{EB} = 8.0 V)				C_{ib}	—	400	600	pF
Dynamic Saturation: determined 1.0 μs and 3.0 μs after rising I_{B1} reach 0.9 final I_{B1} (see Figure 18)	I_C = 0.4 A I_{B1} = 40 mA V_{CC} = 300 V	1.0 μs	@ T_C = 125°C	$V_{CE(dsat)}$	— —	3.5 8.0	— —	Vdc
		3.0 μs	@ T_C = 125°C		— —	1.5 3.8	— —	
	I_C = 1.0 A I_{B1} = 0.2 A V_{CC} = 300 V	1.0 μs	@ T_C = 125°C		— —	8.0 14	— —	
		3.0 μs	@ T_C = 125°C		— —	2.0 7.0	— —	
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)								
Turn–On Time	I_C = 0.4 Adc I_{B1} = 40 mAdc I_{B2} = 0.2 Adc V_{CC} = 300 V		@ T_C = 125°C	t_{on}	— —	200 130	300 —	ns
Turn–Off Time			@ T_C = 125°C	t_{off}	— —	1.2 1.5	2.5 —	μs
Turn–On Time	I_C = 1.0 Adc I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc V_{CC} = 300 V		@ T_C = 125°C	t_{on}	— —	85 95	150 —	ns
Turn–Off Time			@ T_C = 125°C	t_{off}	— —	1.7 2.1	2.5 —	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)								
Fall Time	I_C = 0.4 Adc, I_{B1} = 40 mAdc, I_{B2} = 0.2 Adc		@ T_C = 125°C	t_{fi}	— —	125 120	200 —	ns
Storage Time			@ T_C = 125°C	t_{si}	— —	0.7 0.8	1.25 —	μs
Crossover Time			@ T_C = 125°C	t_c	— —	110 110	200 —	ns
Fall Time	I_C = 1.0 Adc, I_{B1} = 0.2 Adc, I_{B2} = 0.5 Adc		@ T_C = 125°C	t_{fi}	— —	110 120	175 —	ns
Storage Time			@ T_C = 125°C	t_{si}	— —	1.7 2.25	2.75 —	μs
Crossover Time			@ T_C = 125°C	t_c	— —	200 250	300 —	ns
Fall Time	I_C = 0.4 Adc, I_{B1} = 50 mAdc, I_{B2} = 50 mAdc		@ T_C = 125°C	t_{fi}	— —	140 185	200 —	ns
Storage Time			@ T_C = 125°C	t_{si}	— —	2.2 2.5	3.0 —	μs
Crossover Time			@ T_C = 125°C	t_c	— —	140 220	250 —	ns

TYPICAL STATIC CHARACTERISTICS

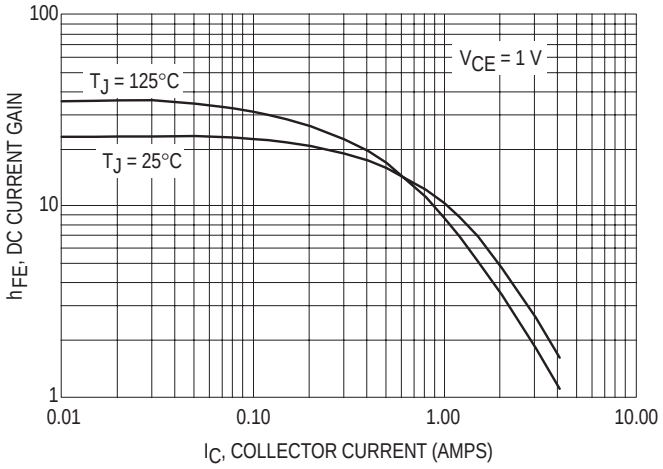


Figure 1. DC Current Gain @ 1 Volt

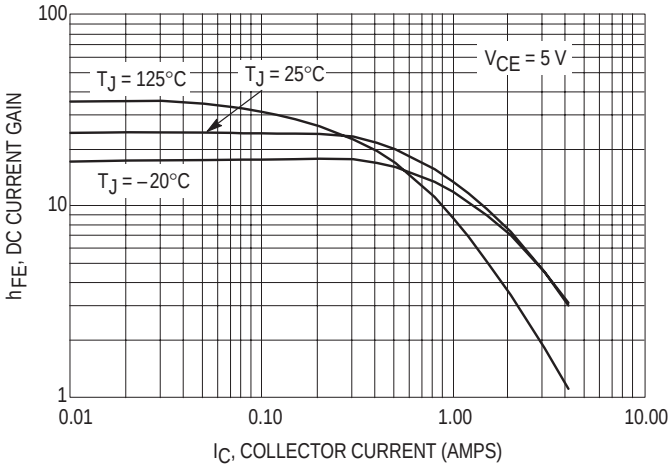


Figure 2. DC Current Gain @ 5 Volts

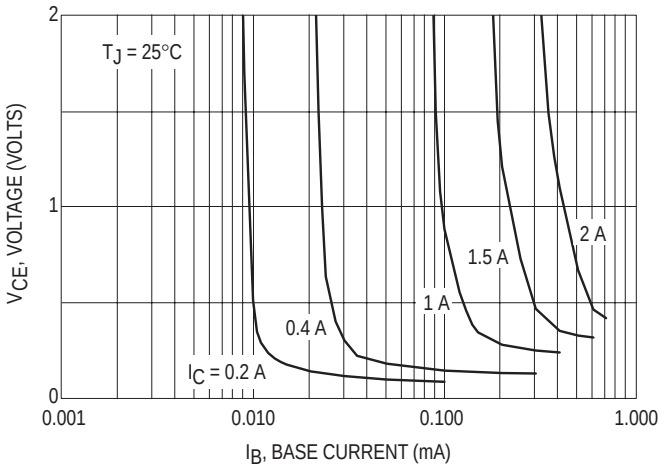


Figure 3. Collector Saturation Region

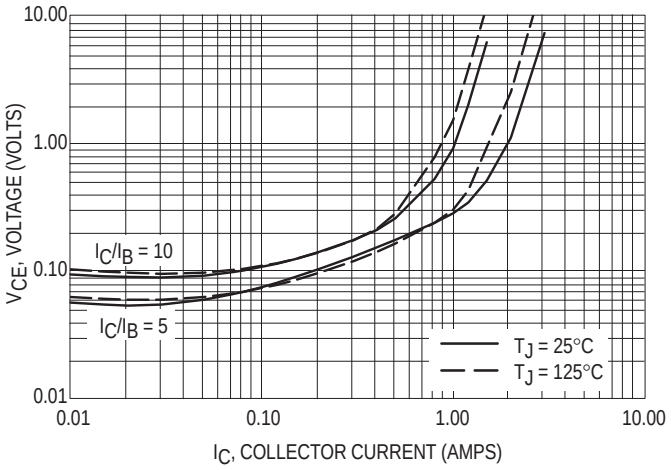


Figure 4. Collector–Emitter Saturation Voltage

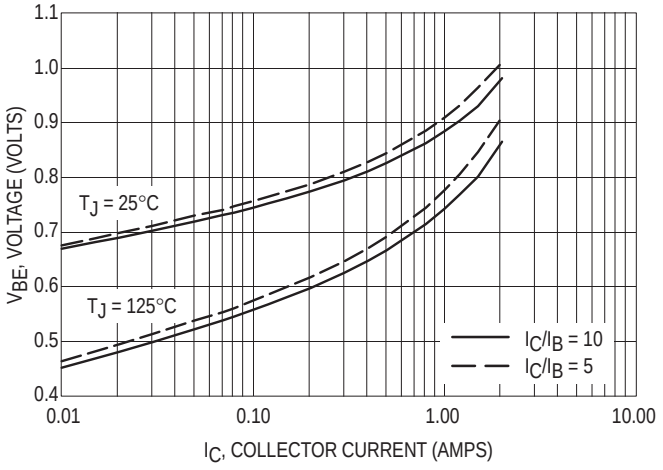


Figure 5. Base–Emitter Saturation Region

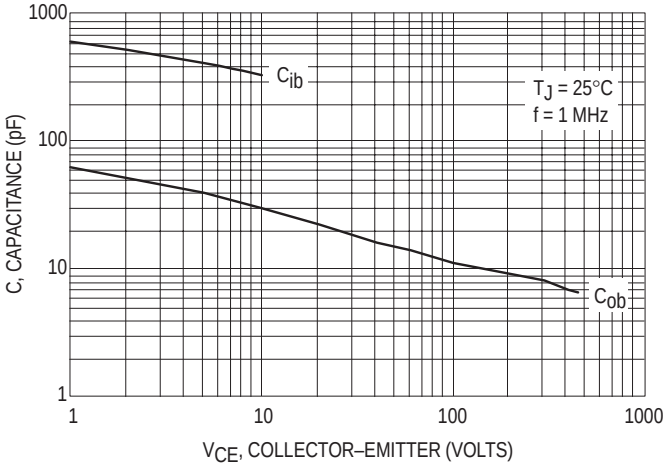


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

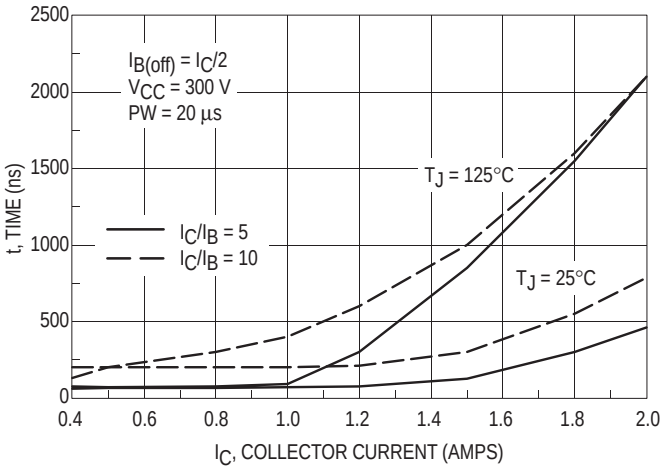


Figure 7. Resistive Switching, t_{on}

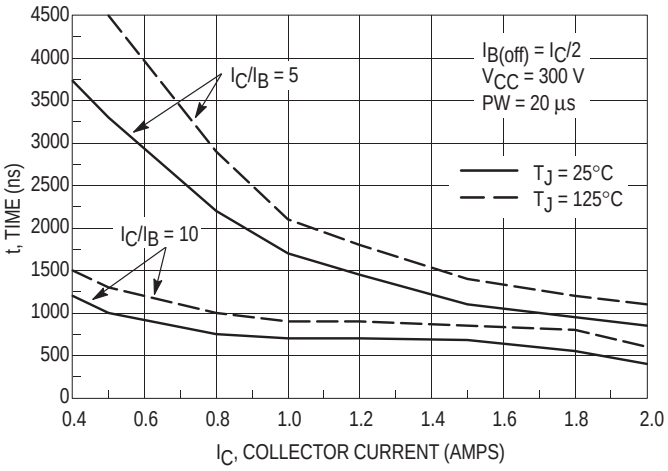


Figure 8. Resistive Switching, t_{off}

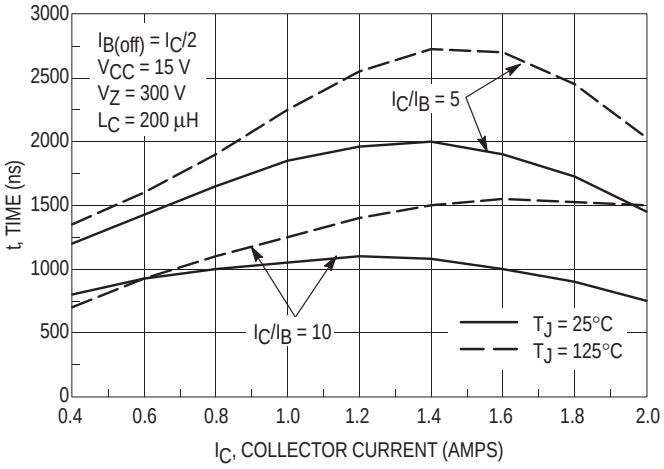


Figure 9. Inductive Storage Time, t_{si}

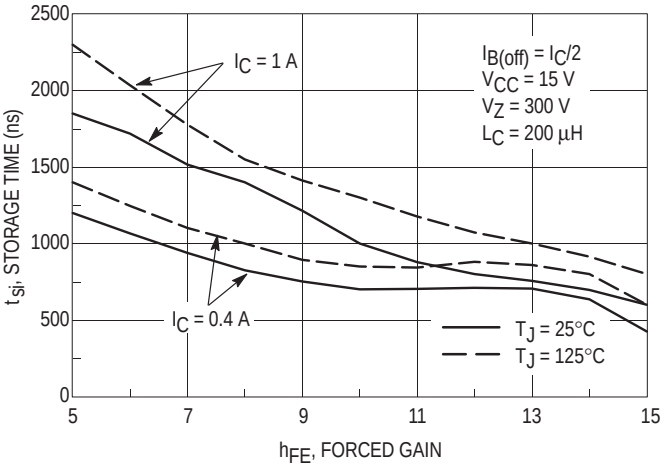


Figure 10. Inductive Storage Time

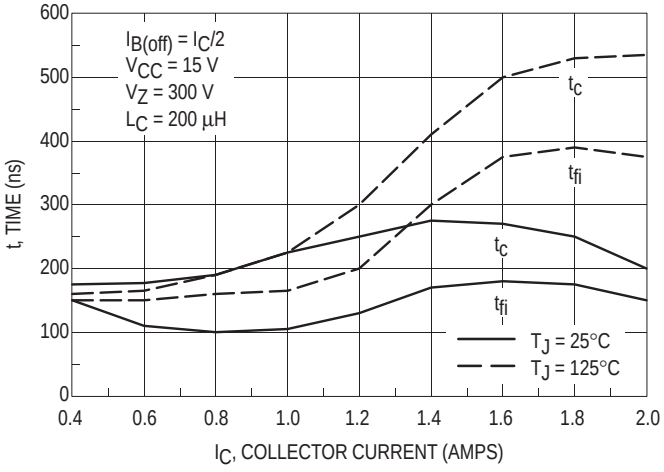


Figure 11. Inductive Switching, t_c & t_{fi}, I_C/I_B = 5

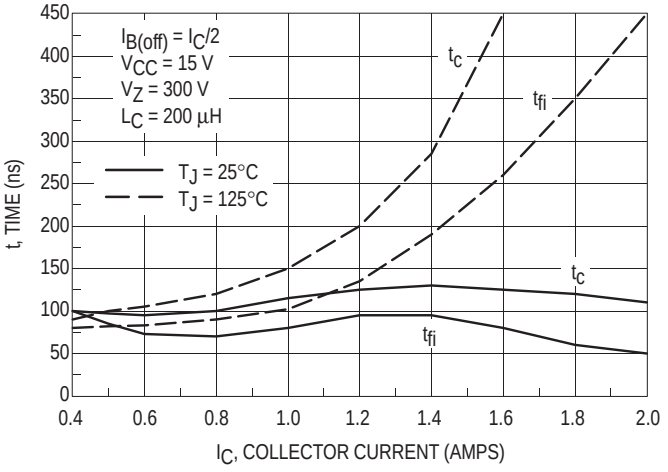


Figure 12. Inductive Switching, t_c & t_{fi}, I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

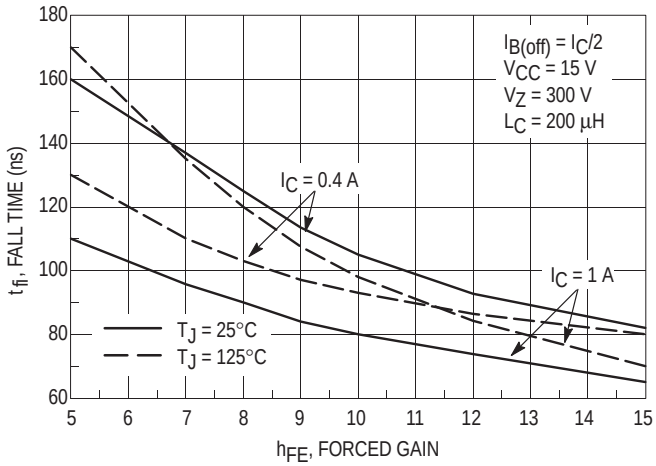


Figure 13. Inductive Fall Time

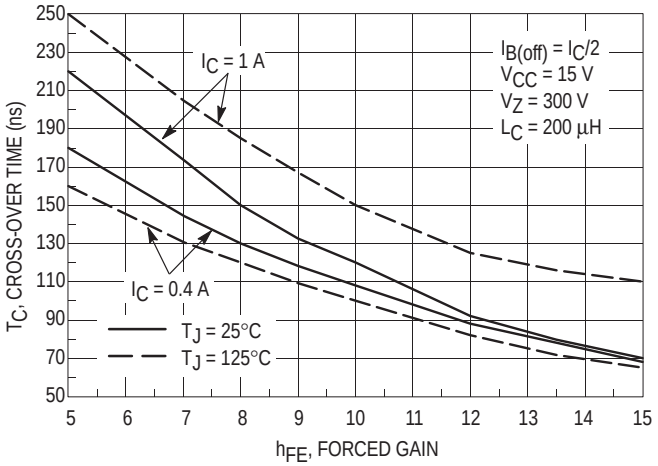


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

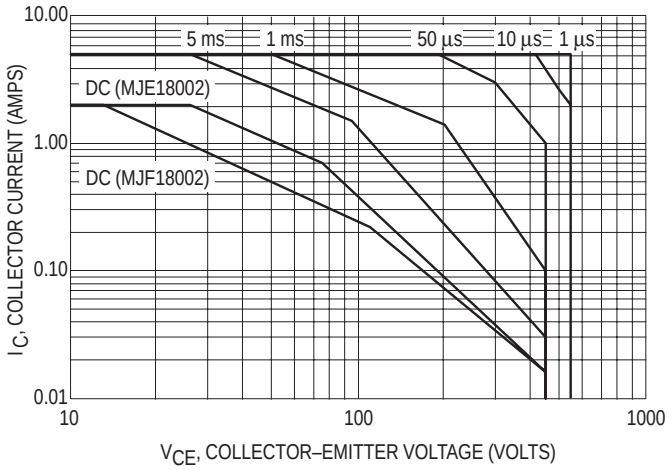


Figure 15. Forward Bias Safe Operating Area

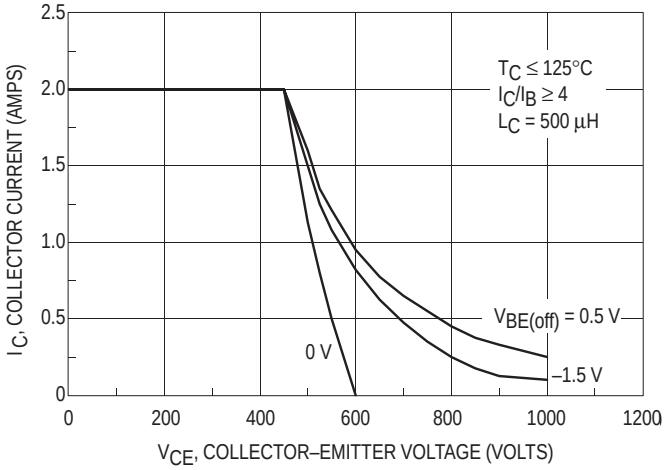


Figure 16. Reverse Bias Switching Safe Operating Area

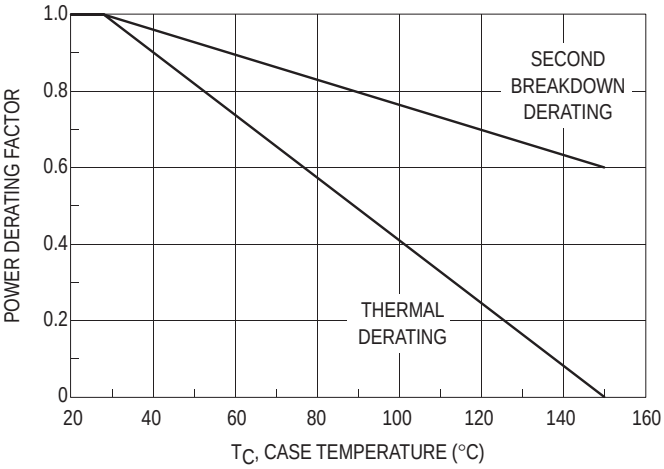


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; T_J(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. T_J(pk) may be calculated from the data in Figures 20 and 21. At any case temperatures, thermal limitations will reduce the power that can be handled to values less the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

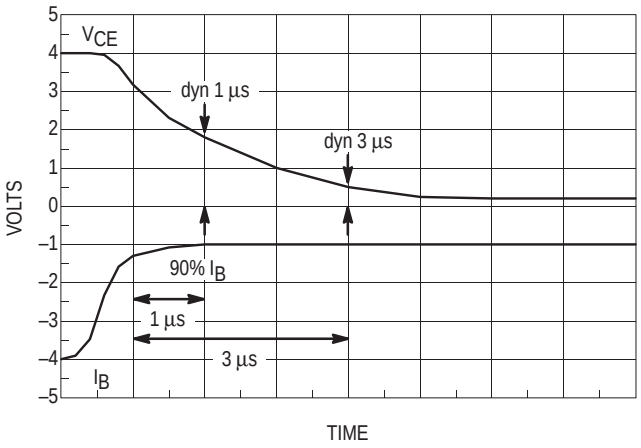


Figure 18. Dynamic Saturation Voltage Measurements

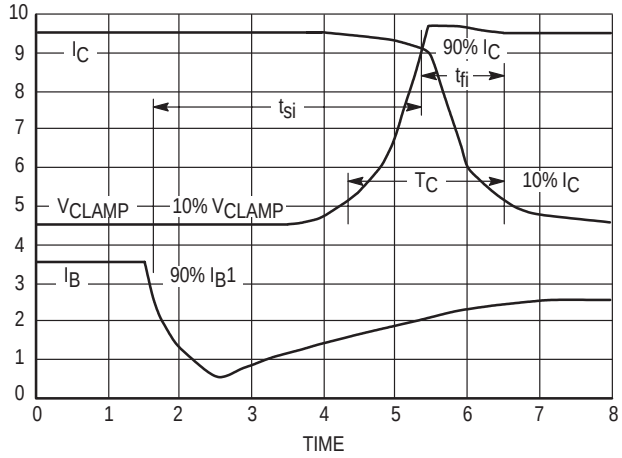
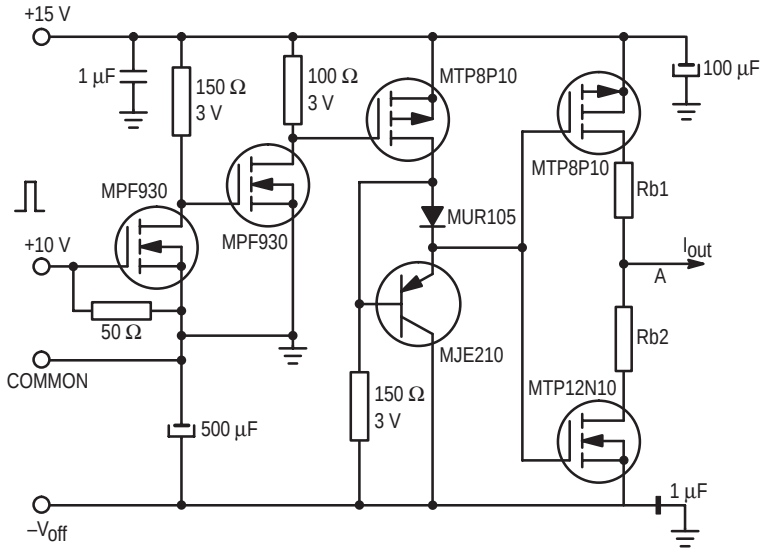
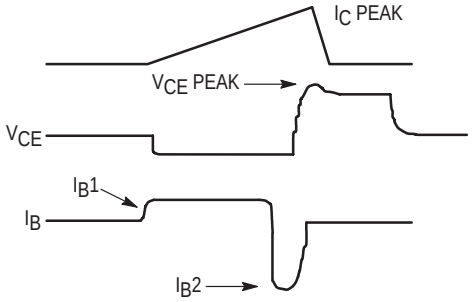


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 µH	L = 200 µH	L = 500 µH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_B1	RB1 SELECTED FOR DESIRED I_B1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

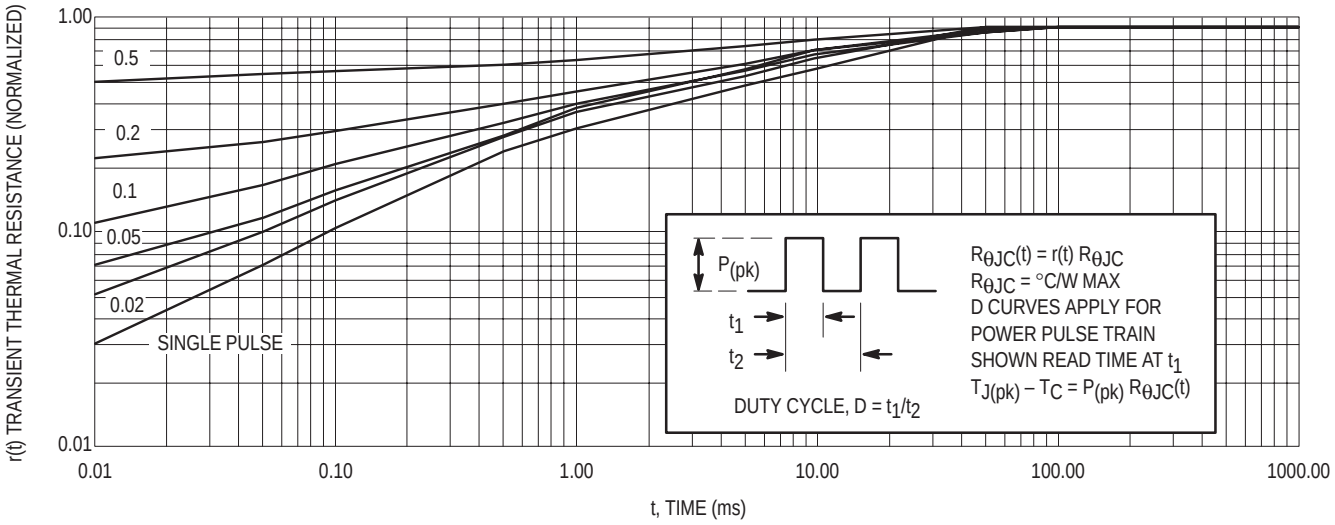


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJE18002

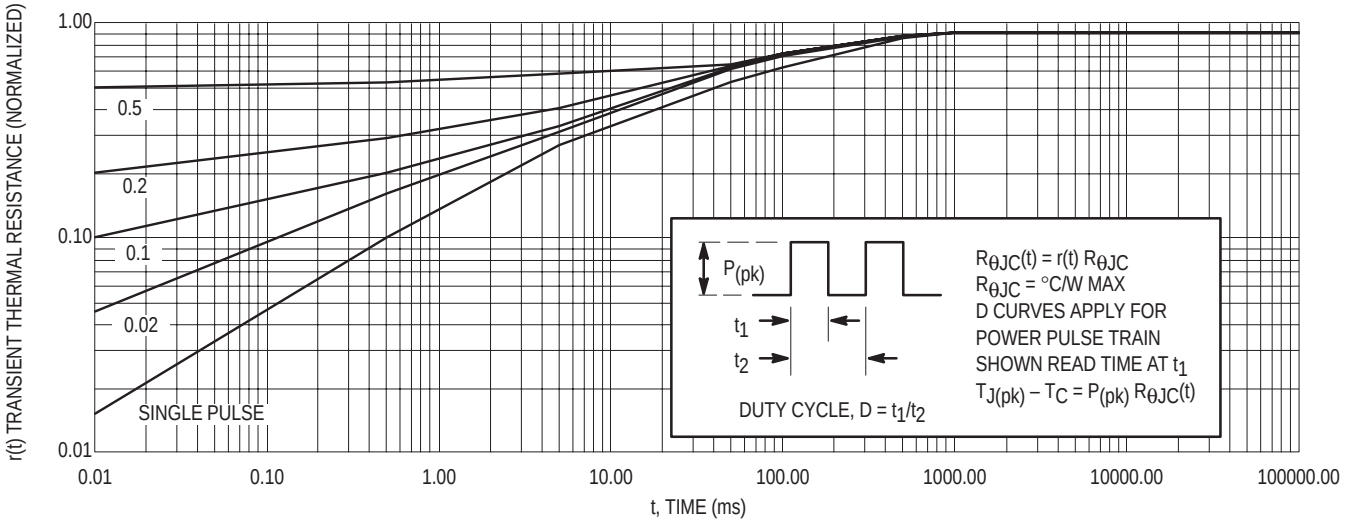


Figure 21. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJF18002

TEST CONDITIONS FOR ISOLATION TESTS*

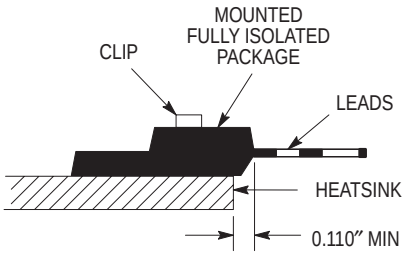


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

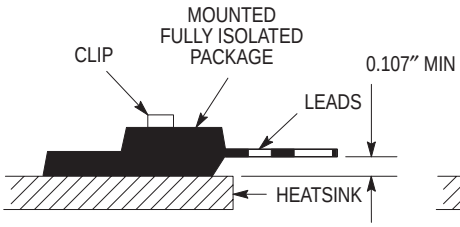


Figure 22b. Clip Mounting Position for Isolation Test Number 2

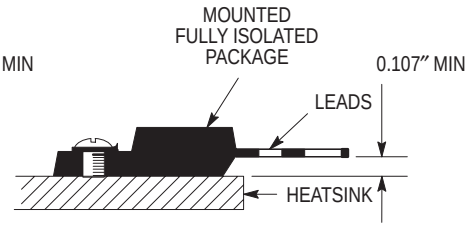


Figure 22c. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION**

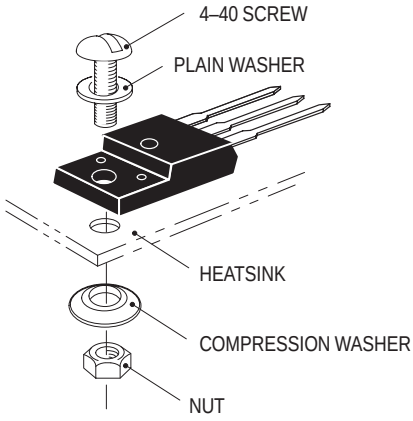


Figure 23a. Screw–Mounted

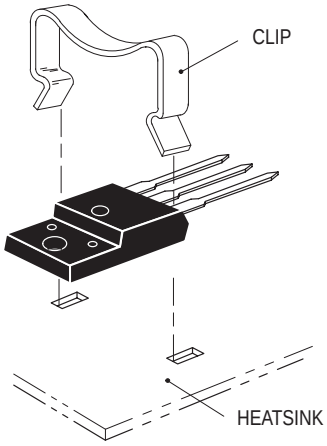


Figure 23b. Clip–Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

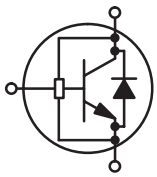
** For more information about mounting power semiconductors see Application Note AN1040.

MJE18002D2

Advance Information

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

POWER TRANSISTORS
2 AMPERES
1000 VOLTS
50 WATTS



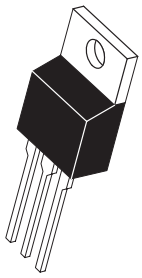
The MJE18002D2 use a newly developed technology, so called H2BIP*, to design the state of art transistor dedicated to the Electronic Light Ballast and PFC** circuit.

The main advantages brought by these new transistors are:

- Improved Global Efficiency Due to the Low Base Drive Requirements
- DC Current Gain Typically Centered at 45
- Extremely Low Storage Time Variation, Thanks to the Antisaturation Network
- Easy to Use Thanks to the Integrated Collector/Emitter Diode

The MOTOROLA "Sig Sixma" philosophy provides tight and reproductible parameter distribution.

* High speed High gain BIPolar transistor
** Power Factor Control



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	1000	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000	Vdc
Emitter–Base Voltage	V_{EBO}	12	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	2 5	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	1 2	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	50 0.4	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	450	570		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CES}			100 500	μAdc
(V_{CE} = 500 V, V_{EB} = 0)	@ T_C = 125°C				100	
Emitter–Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 0.4 Adc, I_B = 40 mAdc)	@ T_C = 25°C			0.78	1	
(I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C			0.87	1.1	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 0.4 Adc, I_B = 40 mAdc)	@ T_C = 25°C			0.36	0.6	
	@ T_C = 125°C			0.5	1	
(I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C			0.4	0.75	
	@ T_C = 125°C			0.65	1.2	
DC Current Gain		h_{FE}				—
(I_C = 0.4 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C		14	25		
	@ T_C = 125°C		8	15		
(I_C = 1 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C		6	10		
	@ T_C = 125°C		4	6		
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}		50	100	pF
Input Capacitance (V_{EB} = 8 Vdc)		C_{ib}		340	500	pF
DIODE CHARACTERISTICS						
Forward Diode Voltage		V_{EC}				V
(I_{EC} = 1 Adc)	@ T_C = 25°C			1.2	1.5	
(I_{EC} = 0.2 Adc)	@ T_C = 25°C			0.9	1.2	
	@ T_C = 125°C			0.6		
(I_{EC} = 0.4 Adc)	@ T_C = 25°C			1	1.3	
	@ T_C = 125°C			0.6		
Forward Recovery Time		t_{fr}				ns
(I_F = 0.2 Adc, di/dt = 10 A/μs)	@ T_C = 25°C			540		
(I_F = 0.4 Adc, di/dt = 10 A/μs)	@ T_C = 25°C			517		
(I_F = 1 Adc, di/dt = 10 A/μs)	@ T_C = 25°C			480		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)							
Turn–on Time	I_C = 1 Adc, I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		100 94	150	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}	0.95	 1.5	1.25	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 0.4 Adc I_{B1} = 40 mAdc I_{B2} = 0.2 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		130 120	175	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		0.55 0.7	0.65	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		110 100	175	ns
Fall Time	I_C = 0.8 Adc I_{B1} = 160 mAdc I_{B2} = 160 mAdc	@ T_C = 25°C @ T_C = 125°C	t_f		130 140	175	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	2.1	 3	2.4	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		275 350	350	ns
Fall Time	I_C = 1 Adc I_{B1} = 0.2 Adc I_{B2} = 0.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		100 100	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		1.05 1.45	1.2	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		100 115	150	ns

DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 0.4 Adc I_{B1} = 40 mA V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C	$V_{CE(dsat)}$		7.4		V
		@ 3 μs	@ T_C = 25°C			2.5		
	I_C = 1 Adc I_{B1} = 0.2 A V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C			11.7		
		@ 3 μs	@ T_C = 25°C			1.3		

Designer's™ Data Sheet
SWITCHMODE™
NPN Bipolar Power Transistor
For Switching Power Supply Applications

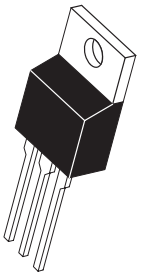
MJE18004*
MJF18004*

*Motorola Preferred Device

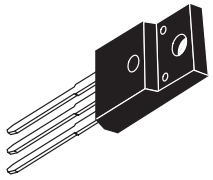
POWER TRANSISTOR
5.0 AMPERES
1000 VOLTS
35 and 75 WATTS

The MJE/MJF18004 have an applications specific state–of–the–art die designed for use in 220 V line operated Switchmode Power supplies and electronic light ballasts. This high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - — High and Flat DC Current Gain h_{FE}
  - — Fast Switching
  - — No Coil Required in Base Circuit for Turn–Off (No Current Tail)
- Full Characterization at 125°C
- Motorola "6 SIGMA" Philosophy Provides Tight and Reproducible Parametric Distributions
- Two Package Choices: Standard TO–220 or Isolated TO–220
- MJF18004, Case 221D, is UL Recognized at 3500 V_{RMS}: File #E69369



CASE 221A–06
TO–220AB
MJE18004



CASE 221D–02
ISOLATED TO–220 TYPE
MJF18004

MAXIMUM RATINGS

Rating	Symbol	MJE18004	MJF18004	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000		Vdc
Emitter–Base Voltage	V_{EBO}	9.0		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	5.0 10		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	2.0 4.0		Adc
RMS Isolation Voltage(2) Test No. 1 Per Fig. 22a (for 1 sec, R.H. Test No. 2 Per Fig. 22b < 30%, T_A = 25°C) Test No. 3 Per Fig. 22c	V_{ISOL}	— — —	4500 3500 1500	Volts
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	75 0.6	35 0.28	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18004	MJF18004	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	3.55 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0) (T_C = 25°C)	I_{CES}	—	—	100	μAdc
(T_C = 125°C)		—	—	500	
(V_{CE} = 800 V, V_{EB} = 0) (T_C = 125°C)		—	—	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise specified)

Characteristic				Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS								
Base–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 0.1 Adc)				$V_{BE(sat)}$	—	0.82	1.1	Vdc
(I_C = 2.0 Adc, I_B = 0.4 Adc)					—	0.92	1.25	
Collector–Emitter Saturation Voltage				$V_{CE(sat)}$				Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)					—	0.25	0.5	
			(T_C = 125°C)		—	0.29	0.6	
(I_C = 2.0 Adc, I_B = 0.4 Adc)					—	0.3	0.45	
			(T_C = 125°C)		—	0.36	0.8	
(I_C = 2.5 Adc, I_B = 0.5 Adc)					—	0.5	0.75	
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 2.5 Vdc)				h_{FE}	12	21	—	—
			(T_C = 125°C)		—	20	—	
(I_C = 0.3 Adc, V_{CE} = 5.0 Vdc)					14	—	34	
			(T_C = 125°C)		—	32	—	
(I_C = 2.0 Adc, V_{CE} = 1.0 Vdc)					6.0	11	—	
			(T_C = 125°C)		—	7.5	—	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)					10	22	—	
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)				f_T	—	13	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)				C_{ob}	—	50	65	pF
Input Capacitance (V_{EB} = 8.0 V)				C_{ib}	—	800	1000	pF
Dynamic Saturation Voltage:	(I_C = 1.0 Adc	1.0 µs	(T_C = 125°C)	$V_{CE(dsat)}$	—	6.8	—	Vdc
Determined 1.0 µs and 3.0 µs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18)	I_{B1} = 100 mAdc V_{CC} = 300 V)				—	14	—	
		3.0 µs	(T_C = 125°C)		—	2.4	—	
					—	5.6	—	
	(I_C = 2.0 Adc	1.0 µs	(T_C = 125°C)		—	11.3	—	
	I_{B1} = 400 mAdc V_{CC} = 300 V)				—	15.5	—	
		3.0 µs	(T_C = 125°C)		—	1.3	—	
					—	6.1	—	
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 µs)								
Turn–On Time	(I_C = 1.0 Adc, I_{B1} = 0.1 Adc,			t_{on}	—	210	300	ns
	I_{B2} = 0.5 Adc, V_{CC} = 300 V)		(T_C = 125°C)		—	180	—	
Turn–Off Time				t_{off}	—	1.0	1.7	µs
			(T_C = 125°C)		—	1.3	—	
Turn–On Time	(I_C = 2.0 Adc, I_{B1} = 0.4 Adc,			t_{on}	—	75	110	ns
	I_{B1} = 1.0 Adc, V_{CC} = 300 V)		(T_C = 125°C)		—	90	—	
Turn–Off Time				t_{off}	—	1.5	2.5	µs
			(T_C = 125°C)		—	1.8	—	
Turn–On Time	(I_C = 2.5 Adc, I_{B1} = 0.5 Adc,			t_{on}	—	450	800	ns
	I_{B2} = 0.5 Adc, V_{CC} = 250 V)		(T_C = 125°C)		—	900	1400	
Storage Time				t_s	—	2.0	3.0	µs
			(T_C = 125°C)		—	2.2	3.5	
Fall Time				t_f	—	275	400	ns
			(T_C = 125°C)		—	500	800	

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)						
Fall Time	(I_C = 1.0 Adc, I_{B1} = 0.1 Adc, I_{B2} = 0.5 Adc)	t_{fi}	— —	100 100	150 —	ns
Storage Time	(T_C = 125°C)	t_{si}	— —	1.1 1.4	1.7 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	180 160	250 —	ns
Fall Time	(I_C = 2.0 Adc, I_{B1} = 0.4 Adc, I_{B2} = 1.0 Adc)	t_{fi}	— —	90 150	175 —	ns
Storage Time	(T_C = 125°C)	t_{si}	— —	1.7 2.2	2.5 —	μs
Crossover Time	(T_C = 125°C)	t_c	— —	180 250	300 —	ns
Fall Time	(I_C = 2.5 Adc, I_{B1} = 0.5 Adc, I_{B2} = 0.5 Adc, $V_{BE(off)}$ = –5.0 Vdc) (T_C = 125°C)	t_{fi}	— —	70 100	130 175	ns
Storage Time	(T_C = 125°C)	t_{si}	— —	0.75 1.0	1.0 1.3	μs
Crossover Time	(T_C = 125°C)	t_c	— —	250 250	350 500	ns

TYPICAL STATIC CHARACTERISTICS

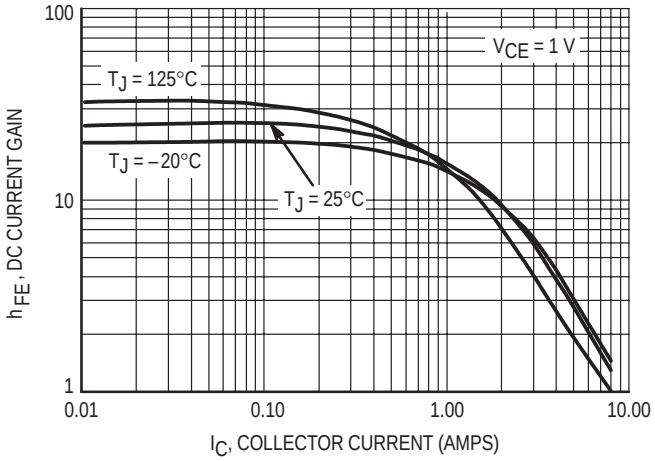


Figure 1. DC Current Gain @ 1 Volt

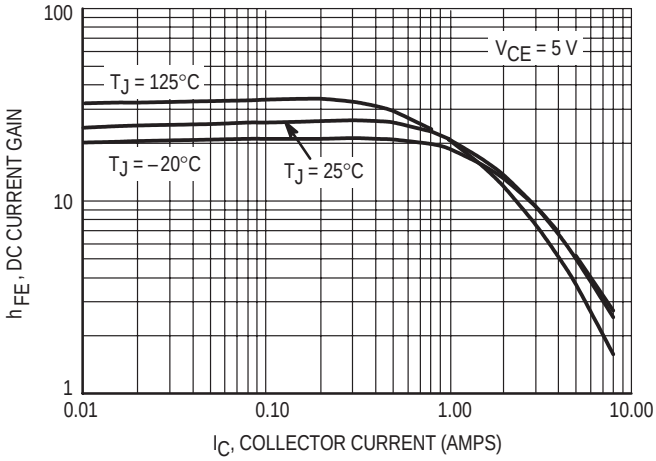


Figure 2. DC Current Gain @ 5 Volts

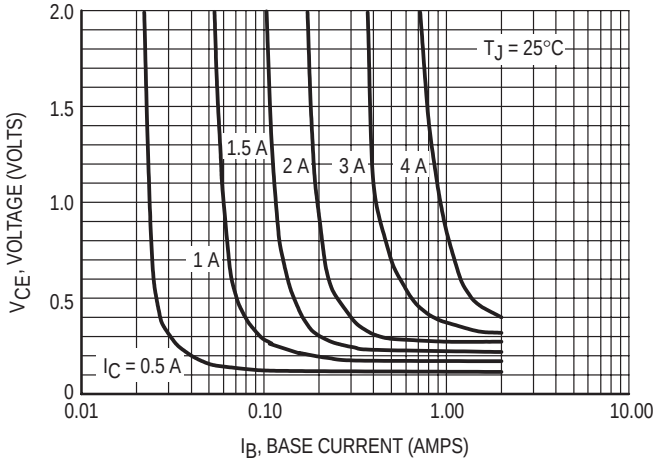


Figure 3. Collector Saturation Region

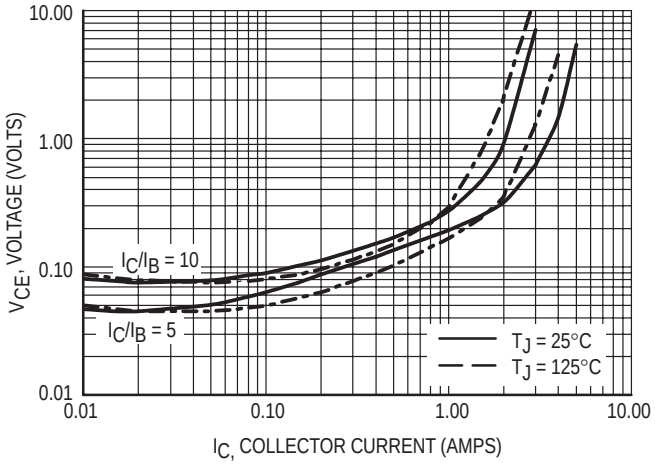


Figure 4. Collector–Emitter Saturation Voltage

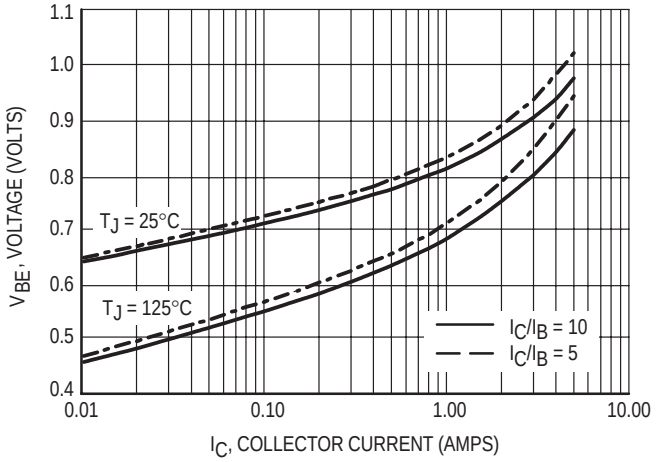


Figure 5. Base–Emitter Saturation Region

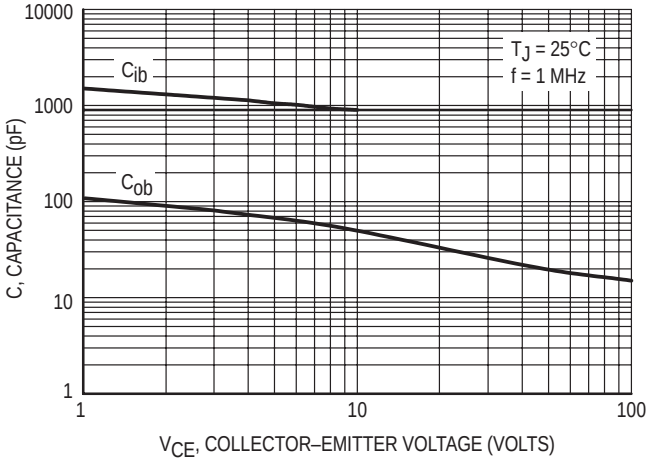


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

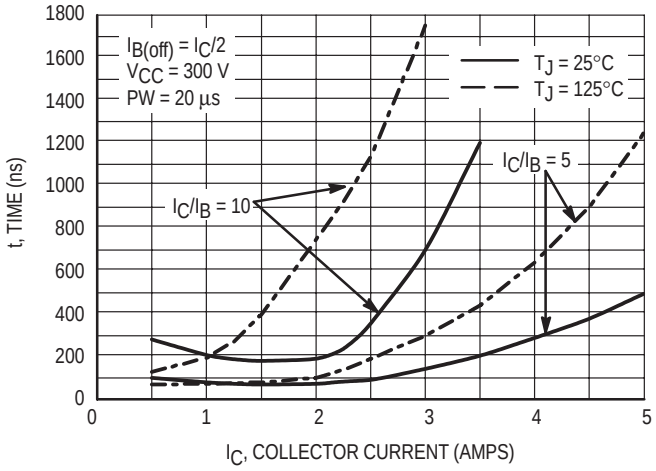


Figure 7. Resistive Switching, t_{on}

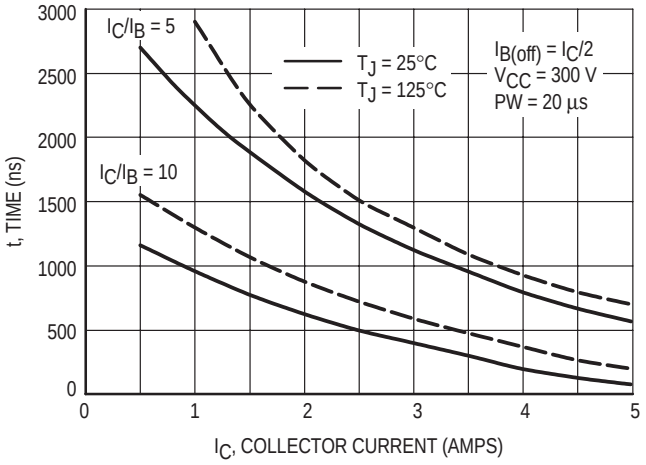


Figure 8. Resistive Switching, t_{off}

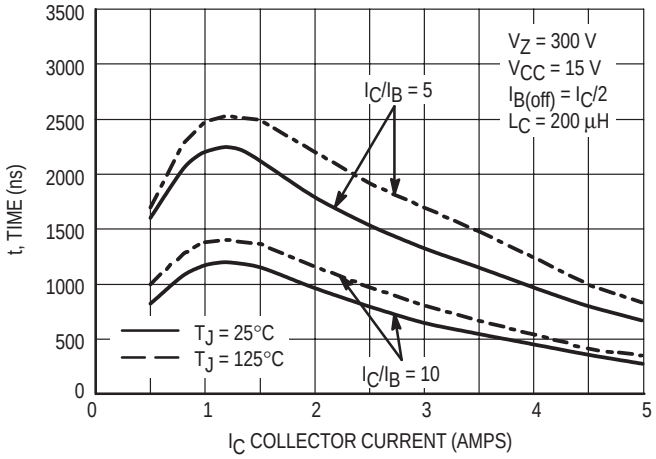


Figure 9. Inductive Storage Time, t_{si}

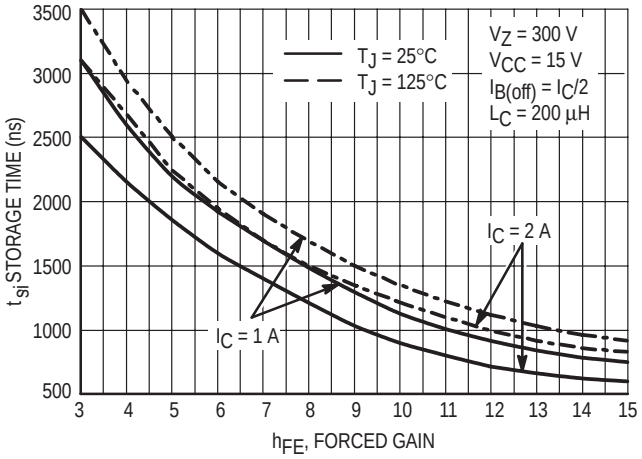


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

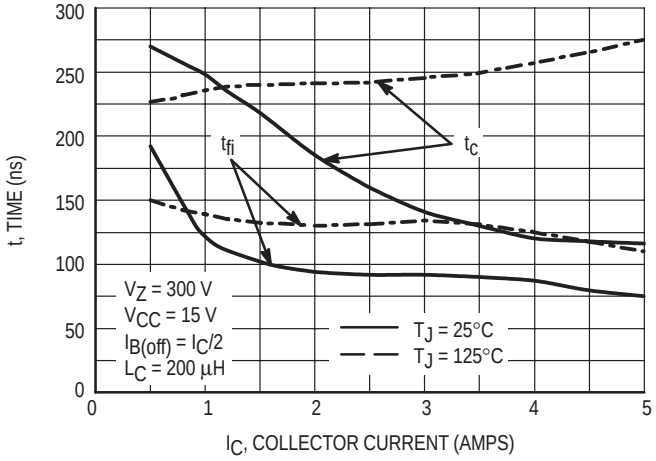


Figure 11. Inductive Switching, t_c & t_{fi}, $I_C/I_B = 5$

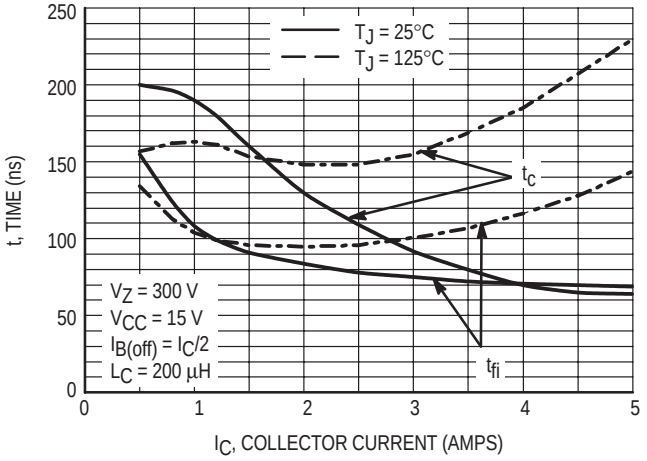


Figure 12. Inductive Switching, t_c & t_{fi}, $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

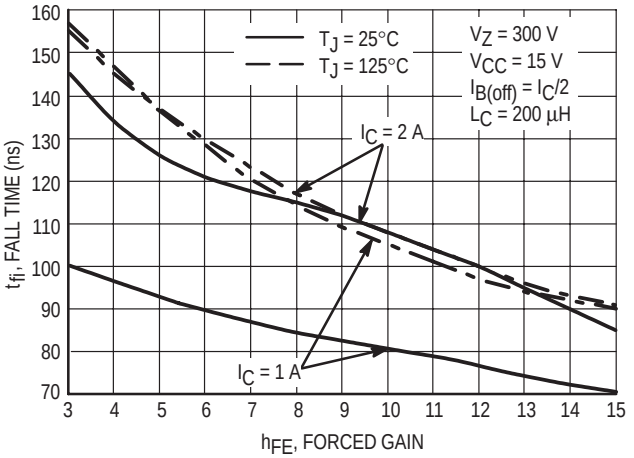


Figure 13. Inductive Fall Time

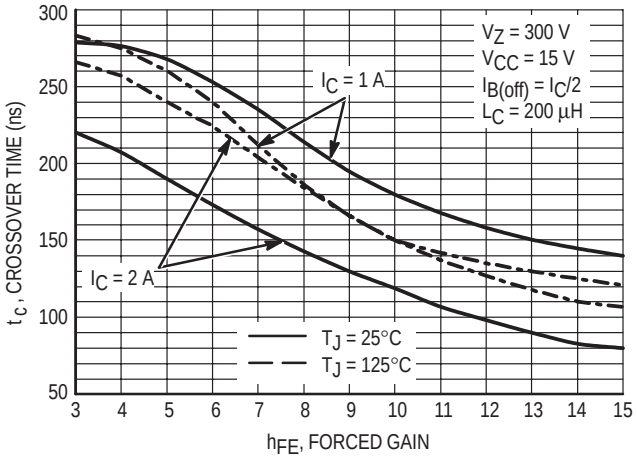


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

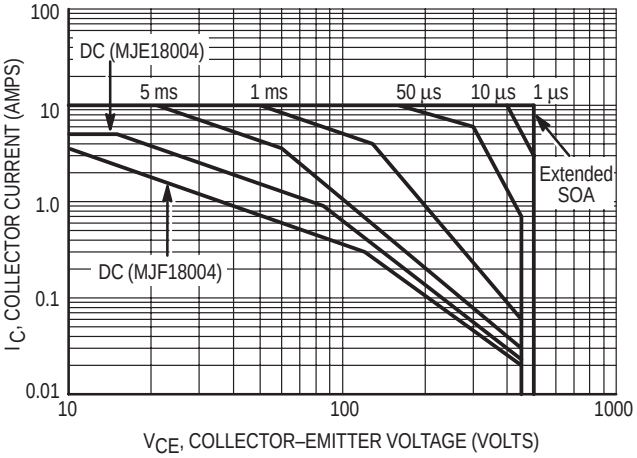


Figure 15. Forward Bias Safe Operating Area

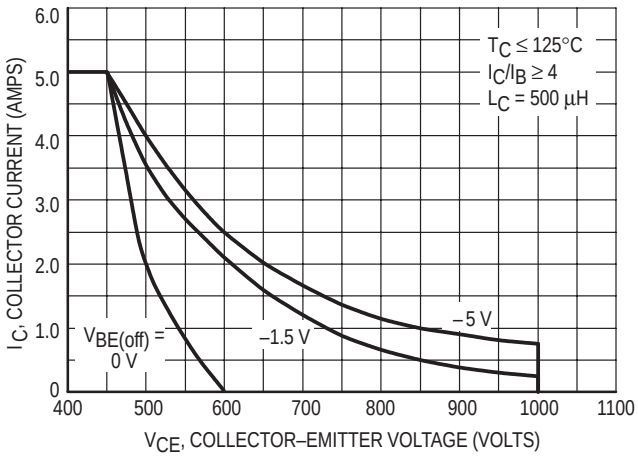


Figure 16. Reverse Bias Safe Operating Area

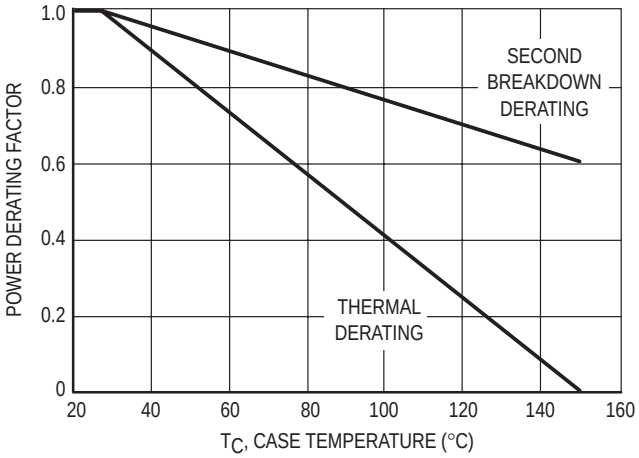


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; T_J(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. T_J(pk) may be calculated from the data in Figures 20 and 21. At any case temperatures, thermal limitations will reduce the power that can be handled to values less the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse biased. The safe level is specified as a reverse–biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

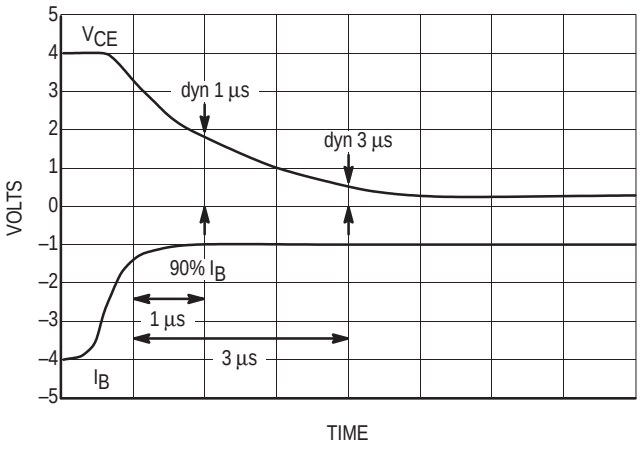


Figure 18. Dynamic Saturation Voltage Measurements

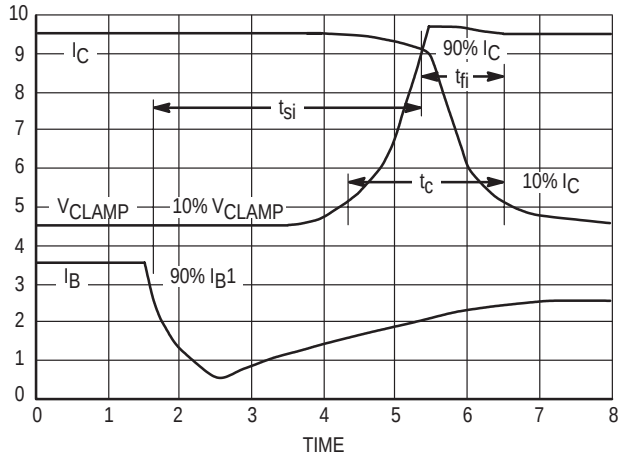
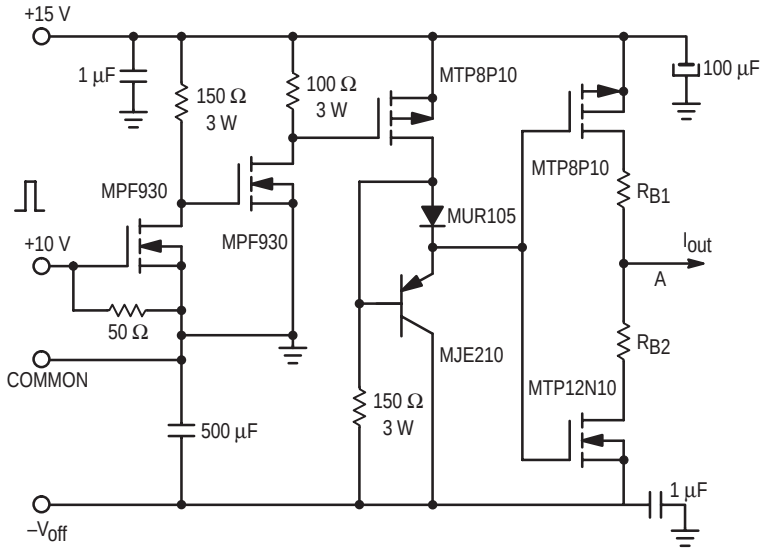
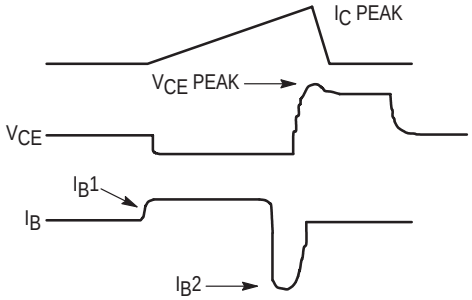


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_B1	RB1 SELECTED FOR DESIRED I_B1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

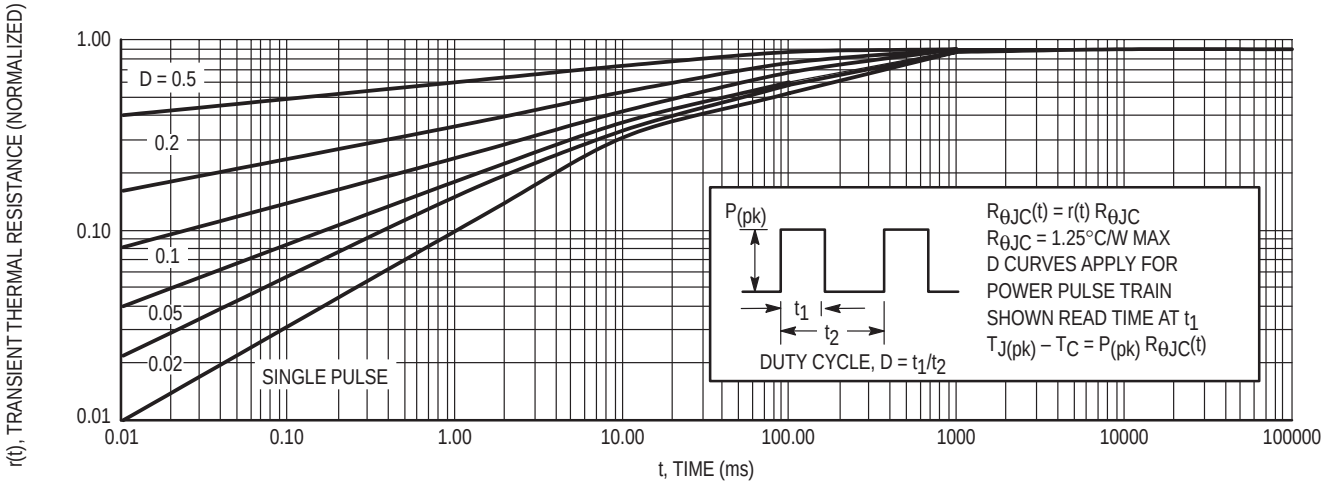


Figure 20. Typical Thermal Response ($Z_{\theta JC(t)}$) for MJE18004

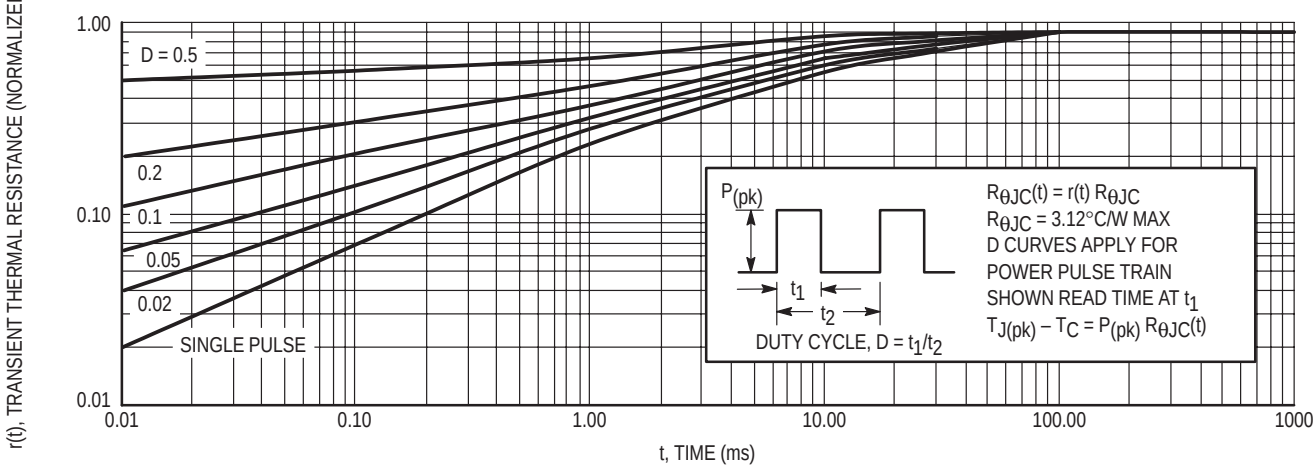


Figure 21. Typical Thermal Response for MJF18004

TEST CONDITIONS FOR ISOLATION TESTS*

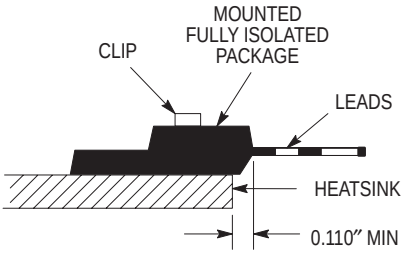


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

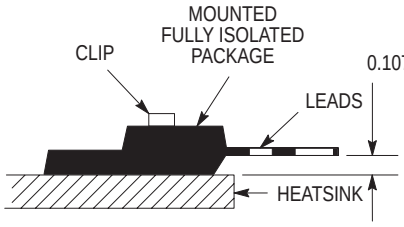


Figure 22b. Clip Mounting Position for Isolation Test Number 2

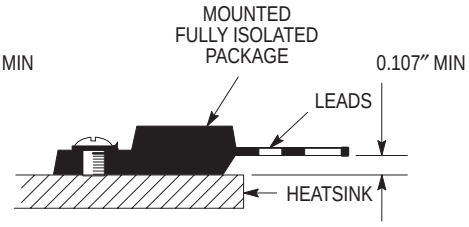


Figure 22c. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION**

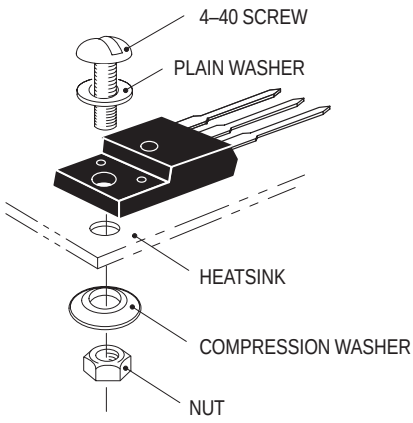


Figure 23a. Screw–Mounted

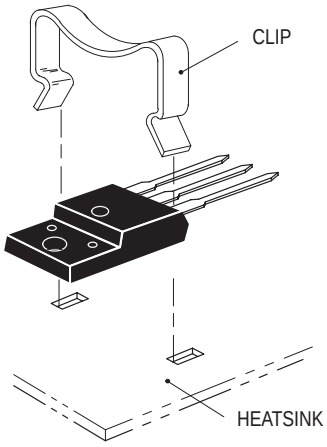


Figure 23b. Clip–Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

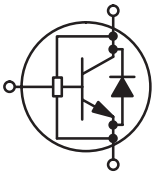
** For more information about mounting power semiconductors see Application Note AN1040.

MJE18004D2

Designer's™ Data Sheet

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network

POWER TRANSISTORS
5 AMPERES
1000 VOLTS
75 WATTS

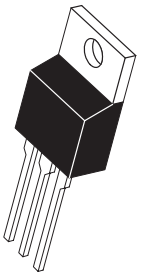


The MJE18004D2 is state–of–art High Speed High gain BIPolar transistor (H2BIP). High dynamic characteristics and lot to lot minimum spread (±150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no need to guarantee an h_{FE} window.

Main features:

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ I_C = 100 mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector–Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic $V_{CE(sat)}$
- "6 Sigma" Process Providing Tight and Reproductible Parameter Spreads

It's characteristics make it also suitable for PFC application.



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	1000	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000	Vdc
Emitter–Base Voltage	V_{EBO}	12	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5 10	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	75 0.6	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)			$V_{CEO(sus)}$	450	547		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)			V_{CBO}	1000	1100		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)			V_{EBO}	12	14		Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)			I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C @ T_C = 125°C		I_{CES}			100 500	μAdc
(V_{CE} = 500 V, V_{EB} = 0)	@ T_C = 125°C					100	
Emitter–Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)			I_{EBO}			100	μAdc
ON CHARACTERISTICS							
Base–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)	@ T_C = 25°C @ T_C = 125°C		$V_{BE(sat)}$		0.8 0.7	1 0.9	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C				0.9 0.8	1 0.9	
Collector–Emitter Saturation Voltage (I_C = 0.8 Adc, I_B = 80 mAdc)	@ T_C = 25°C @ T_C = 125°C		$V_{CE(sat)}$		0.38 0.55	0.5 0.75	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C				0.45 0.75	0.75 1	
(I_C = 0.8 Adc, I_B = 40 mAdc)	@ T_C = 25°C @ T_C = 125°C				0.9 1.6	1.5	
(I_C = 1 Adc, I_B = 0.2 Adc)	@ T_C = 25°C @ T_C = 125°C				0.25 0.28	0.5 0.6	
DC Current Gain (I_C = 0.8 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		h_{FE}	15 10	28 14		—
(I_C = 2 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C			6 4	8 6		
(I_C = 1 Adc, V_{CE} = 2.5 Vdc)	@ T_C = 25°C @ T_C = 125°C			18 14	28 20		
DYNAMIC SATURATION VOLTAGE							
Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1 Adc I_{B1} = 100 mA V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C	$V_{CE(dsat)}$		9 16		V
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C			3.1 9		
	I_C = 2 Adc I_{B1} = 0.4 A V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C @ T_C = 125°C			11 18		
		@ 3 μs	@ T_C = 25°C @ T_C = 125°C			1.4 8		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS							
Forward Diode Voltage (I_{EC} = 1 Adc)		@ T_C = 25°C @ T_C = 125°C	V_{EC}		0.96 0.72	1.5	V
(I_{EC} = 2 Adc)		@ T_C = 25°C @ T_C = 125°C			1.15 0.8	1.7	
Forward Recovery Time (I_F = 0.4 Adc, di/dt = 10 A/μs)		@ T_C = 25°C	t_{fr}		440		ns
(I_F = 1 Adc, di/dt = 10 A/μs)		@ T_C = 25°C			335		
(I_F = 2 Adc, di/dt = 10 A/μs)		@ T_C = 25°C			335		
DYNAMIC CHARACTERISTICS							
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)			f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)			C_{ob}		60	100	pF
Input Capacitance (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)			C_{ib}		450	750	pF
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Turn–on Time	I_C = 2.5 Adc, I_{B1} = 0.5 Adc I_{B2} = 1 Adc V_{CC} = 250 Vdc	@ T_C = 25°C	t_{on}		500	750	ns
Turn–off Time		@ T_C = 25°C	t_{off}	1.1		1.4	μs
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 1 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		100 150	150	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		1.15 1.6	1.3	μs
Turn–on Time	I_C = 2.5 Adc, I_{B1} = 0.5 Adc I_{B2} = 0.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		120 500	150	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}	1.85	 2.6	2.15	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{CC} = 15 V)							
Fall Time	I_C = 2.5 Adc I_{B1} = 500 mAdc I_{B2} = 500 mAdc V_Z = 350 V L_C = 300 μH	@ T_C = 25°C @ T_C = 125°C	t_f		130 300	175	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		2.12 2.6	2.4	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		355 750	500	ns
Fall Time	I_C = 2 Adc I_{B1} = 400 mAdc I_{B2} = 400 mAdc V_Z = 300 V L_C = 200 μH	@ T_C = 25°C @ T_C = 125°C	t_f		95 230	150	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	2.1	 2.9	2.4	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		300 700	450	ns
Fall Time	I_C = 1 Adc I_{B1} = 100 mAdc I_{B2} = 500 mAdc V_Z = 300 V L_C = 200 μH	@ T_C = 25°C @ T_C = 125°C	t_f		70 100	90	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		0.7 1.05	0.9	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		75 160	120	ns

TYPICAL STATIC CHARACTERISTICS

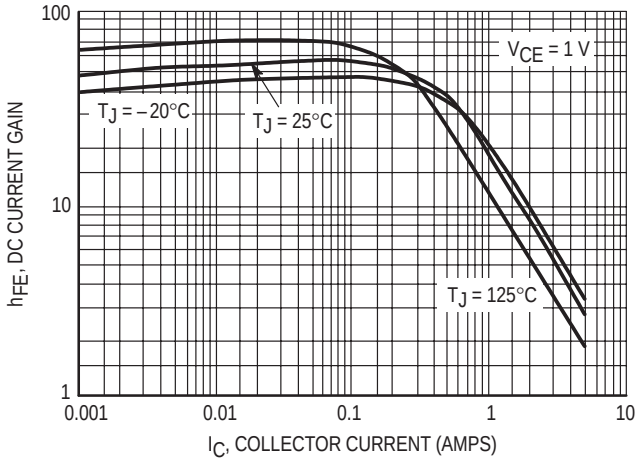


Figure 1. DC Current Gain @ 1 Volt

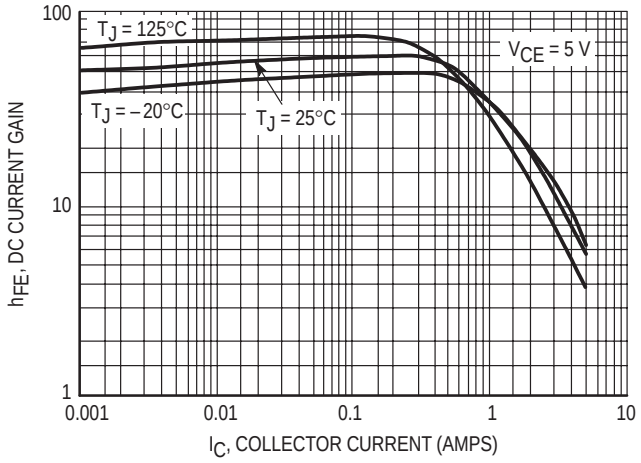


Figure 2. DC Current Gain @ 5 Volt

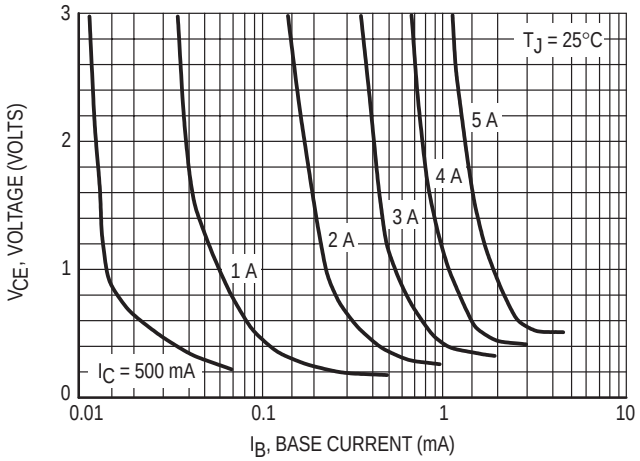


Figure 3. Collector Saturation Region

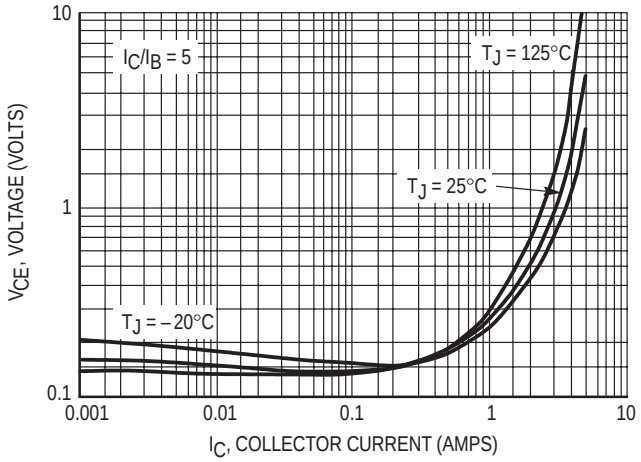


Figure 4. Collector–Emitter Saturation Voltage

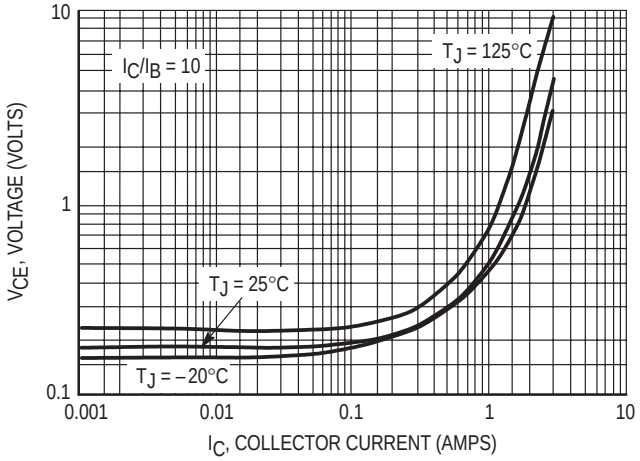


Figure 5. Collector–Emitter Saturation Voltage

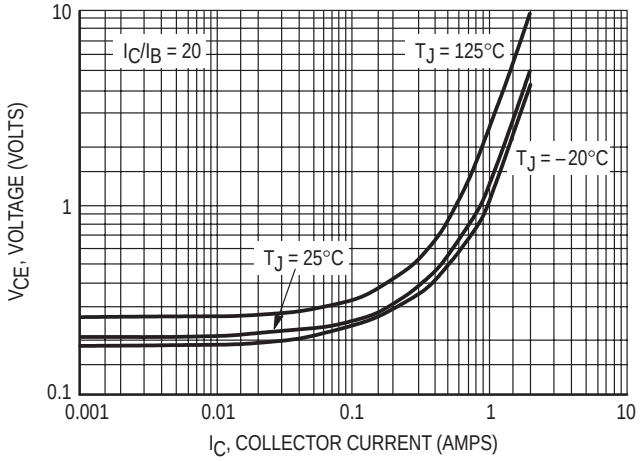


Figure 6. Collector–Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

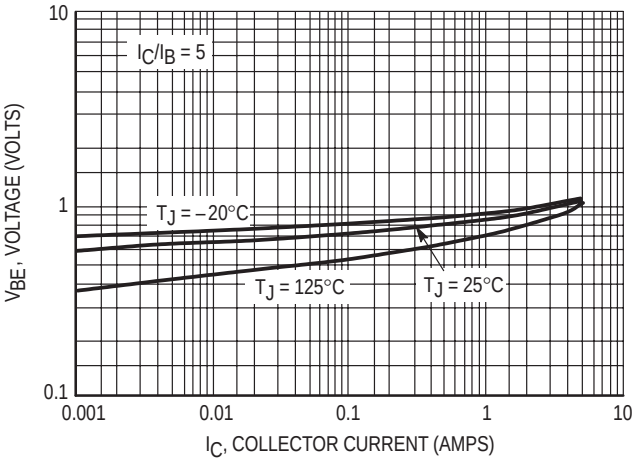


Figure 7. Base–Emitter Saturation Region

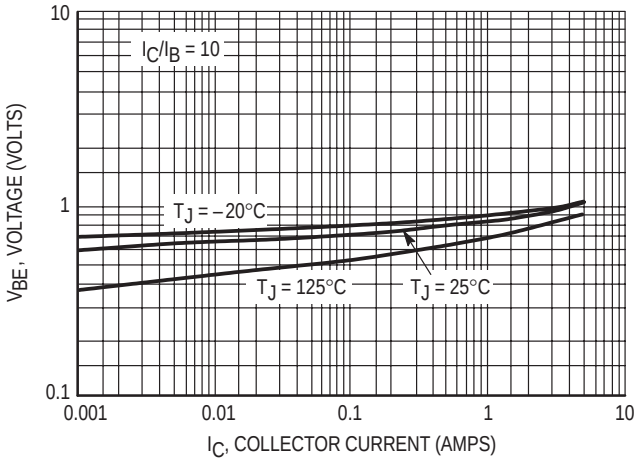


Figure 8. Base–Emitter Saturation Region

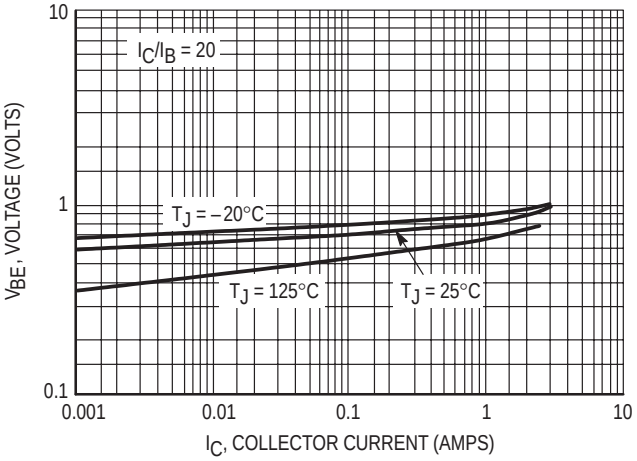


Figure 9. Base–Emitter Saturation Region

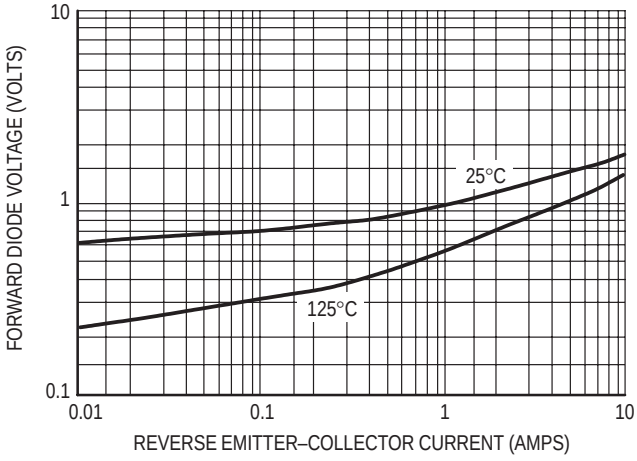


Figure 10. Forward Diode Voltage

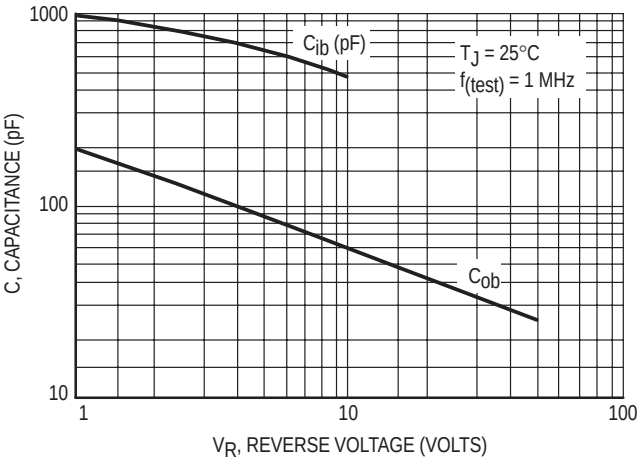


Figure 11. Capacitance

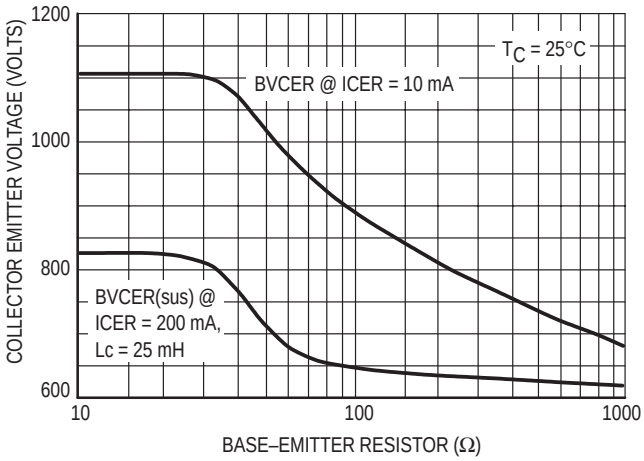


Figure 12. BVCER = f(R_{BE})

TYPICAL SWITCHING CHARACTERISTICS

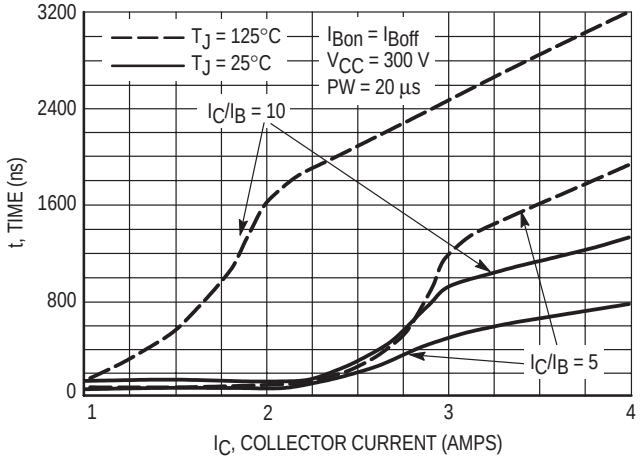


Figure 13. Resistive Switch Time, t_{on}

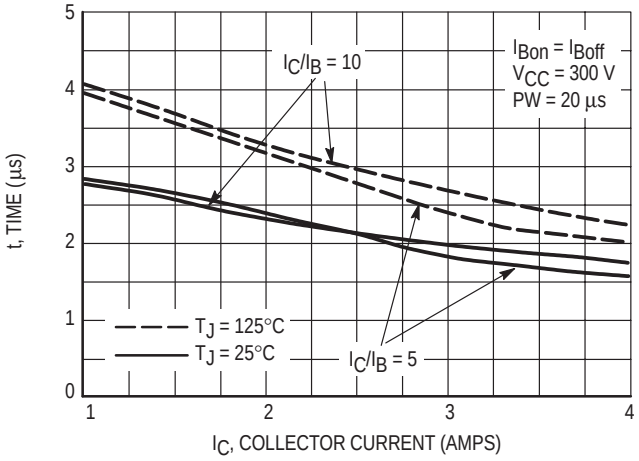


Figure 14. Resistive Switch Time, t_{off}

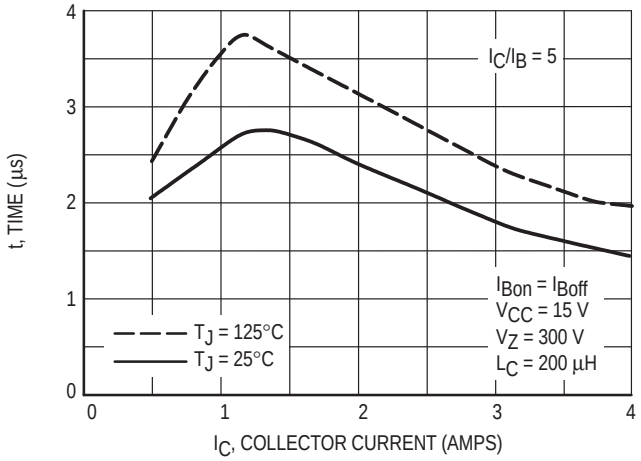


Figure 15. Inductive Storage Time, t_{si} @ I_C/I_B = 5

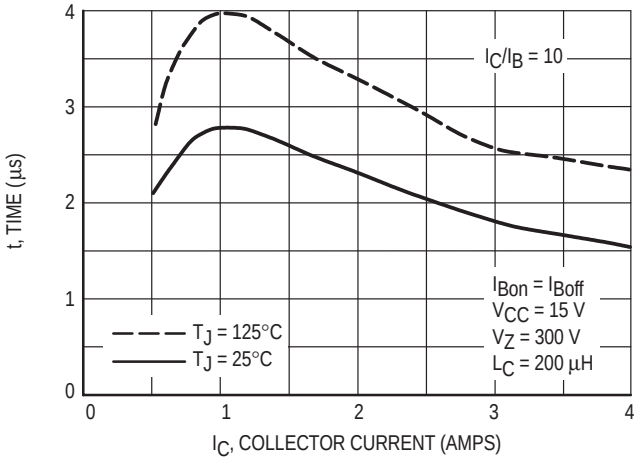


Figure 16. Inductive Storage Time, t_{si} @ I_C/I_B = 10

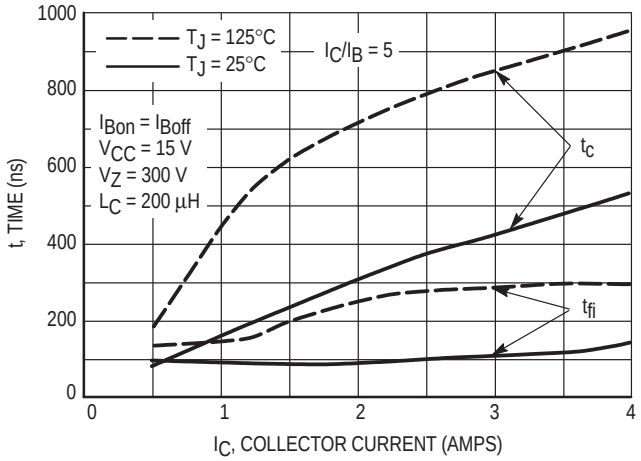


Figure 17. Inductive Switching Time, t_c & t_{fi} @ I_C/I_B = 5

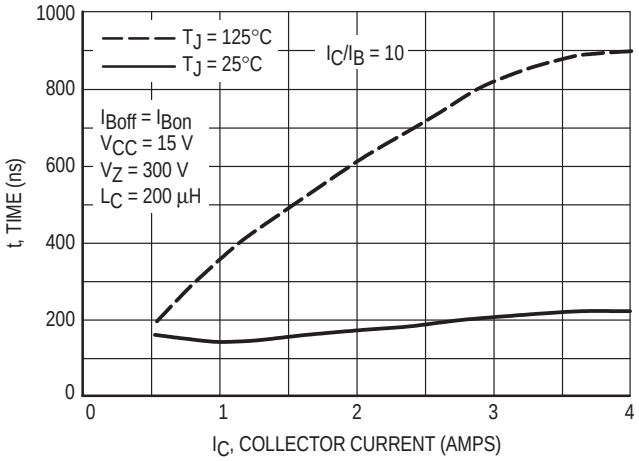


Figure 18. Inductive Switching Time, t_{fi} @ I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS

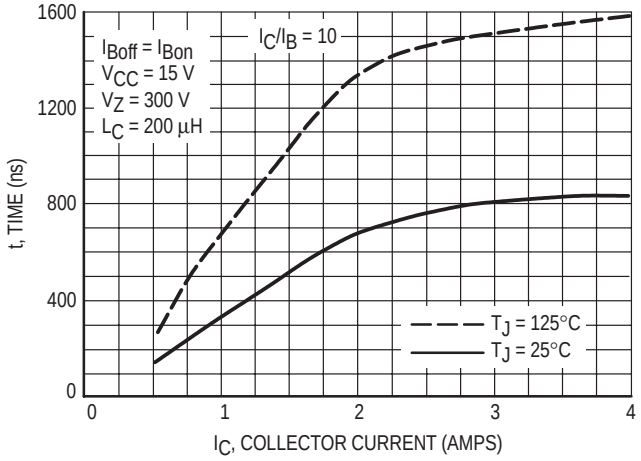


Figure 19. Inductive Switching, t_c @ I_C/I_B = 10

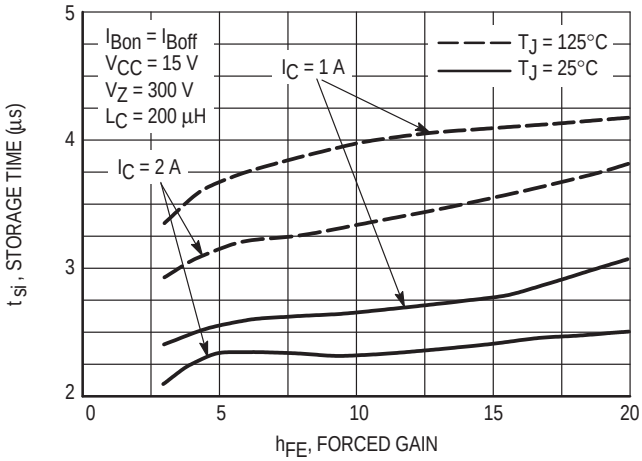


Figure 20. Inductive Storage Time

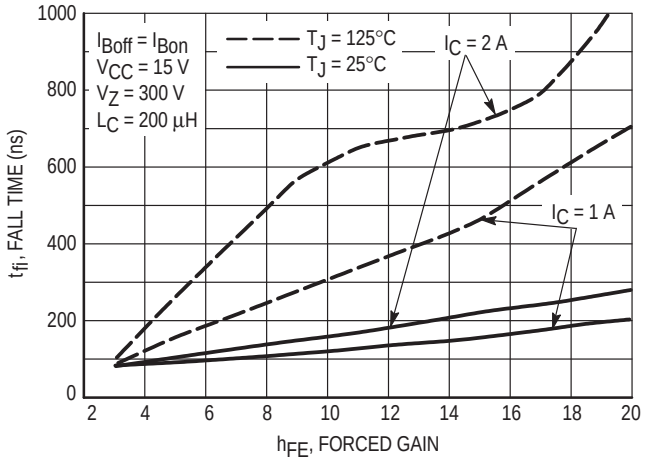


Figure 21. Inductive Fall Time

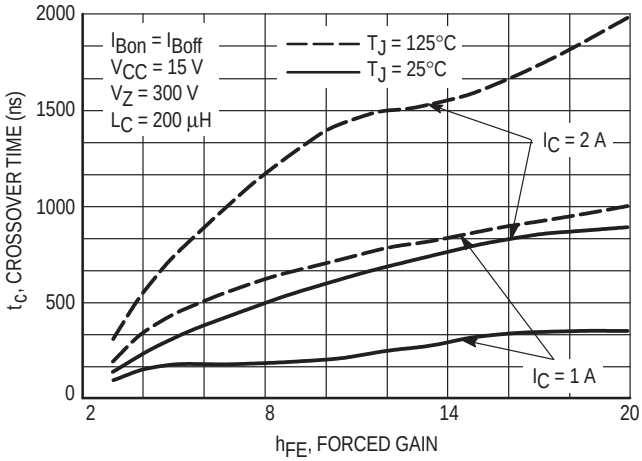


Figure 22. Inductive Crossover Time

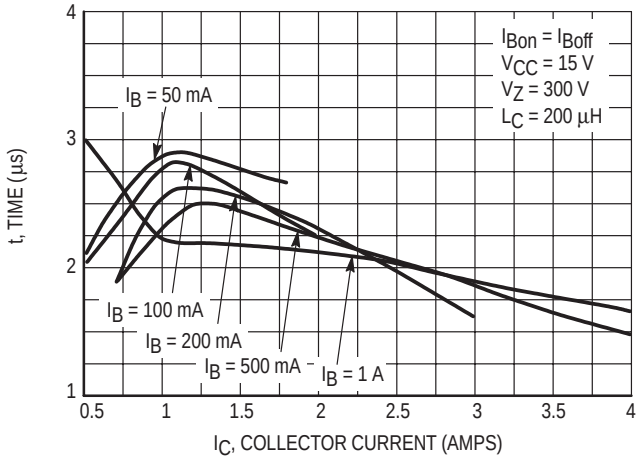


Figure 23. Inductive Storage Time, t_{si}

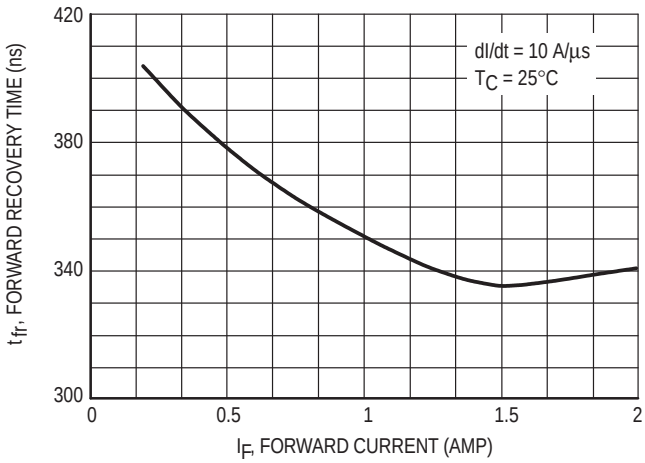


Figure 24. Forward Recovery Time, T_{FR}

TYPICAL SWITCHING CHARACTERISTICS

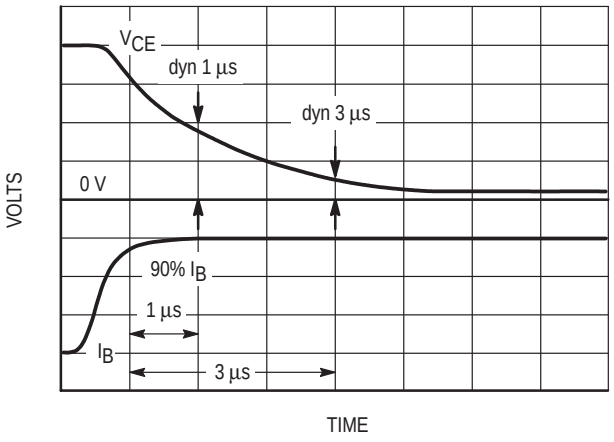


Figure 25. Dynamic Saturation Voltage Measurements

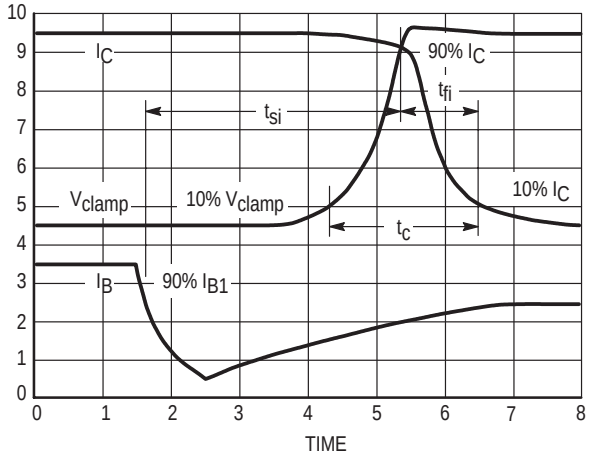


Figure 26. Inductive Switching Measurements

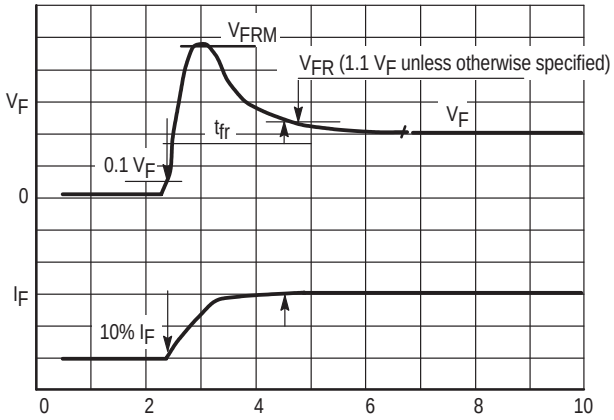
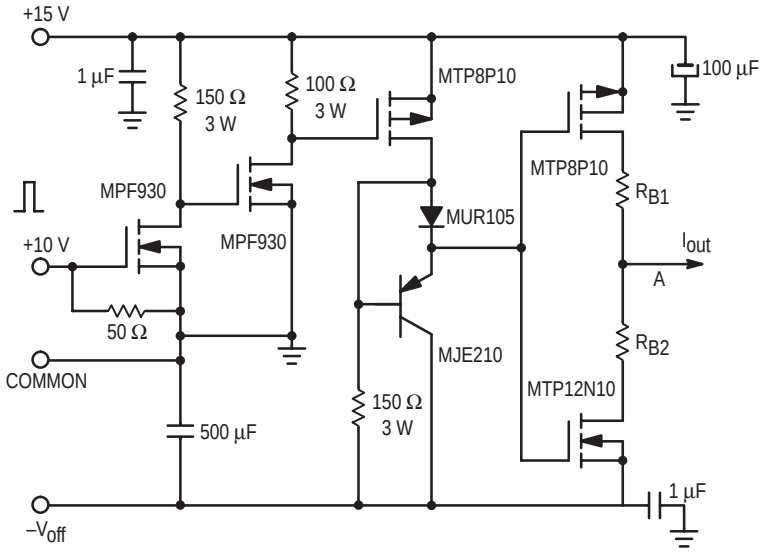
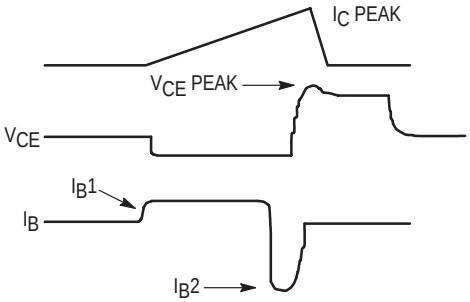


Figure 27. t_{fr} Measurements

TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 µH	L = 500 µH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	RB1 selected for desired Ib1	RB1 selected for desired Ib1

TYPICAL CHARACTERISTICS

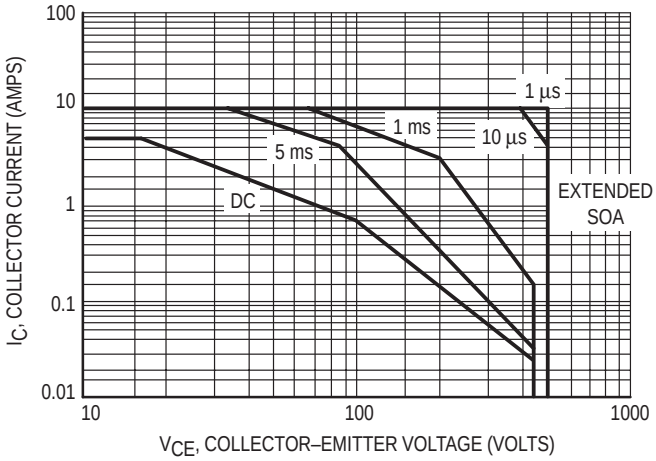


Figure 28. Forward Bias Safe Operating Area

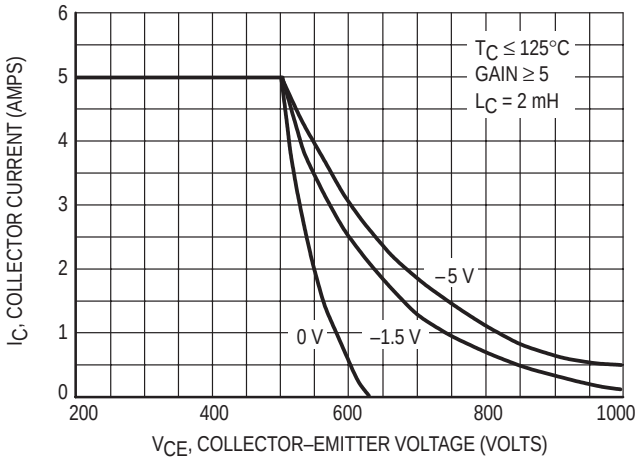


Figure 29. Reverse Bias Safe Operating Area

TYPICAL CHARACTERISTICS

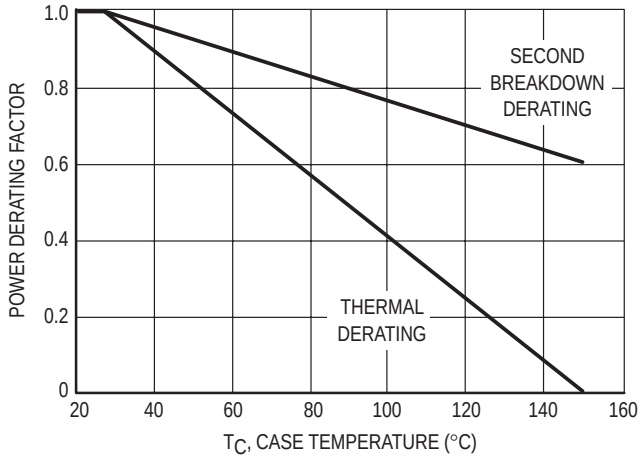


Figure 30. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on T_C = 25°C; T_J(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

T_J(pk) may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse biased. The safe level is specified as a reverse–biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL THERMAL RESPONSE

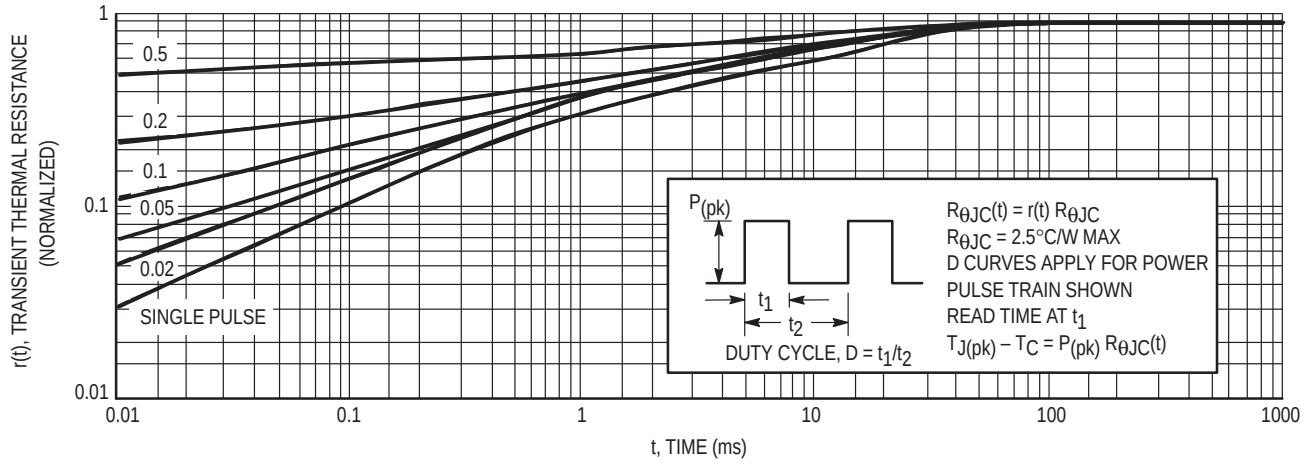


Figure 31. Typical Thermal Response ($Z_{\theta JC(t)}$) for MJE18004D2

Designer's™ Data Sheet
SWITCHMODE™
NPN Bipolar Power Transistor For Switching Power Supply Applications

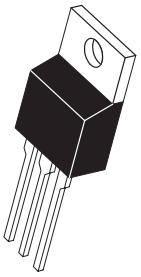
MJE18006*
MJF18006*

*Motorola Preferred Device

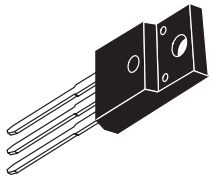
POWER TRANSISTOR
6.0 AMPERES
1000 VOLTS
40 and 100 WATTS

The MJE/MJF18006 have an applications specific state–of–the–art die designed for use in 220 V line–operated Switchmode Power supplies and electronic light ballasts. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - — High and Flat DC Current Gain h_{FE}
  - — Fast Switching
  - — No Coil Required in Base Circuit for Turn–Off (No Current Tail)
- Tight Parametric Distributions are Consistent Lot–to–Lot
- Two Package Choices: Standard TO–220 or Isolated TO–220
- MJF18006, Case 221D, is UL Recognized at 3500 V_{RMS}: File #E69369



CASE 221A–06
TO–220AB
MJE18006



CASE 221D–02
ISOLATED TO–220 TYPE
UL RECOGNIZED
MJF18006

MAXIMUM RATINGS

Rating	Symbol	MJE18006	MJF18006	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000		Vdc
Emitter–Base Voltage	V_{EBO}	9.0		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	6.0 15		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	4.0 8.0		Adc
RMS Isolation Voltage(2) Test No. 1 Per Fig. 22a (for 1 sec, R.H. < 30%, Test No. 1 Per Fig. 22b T_C = 25°C) Test No. 1 Per Fig. 22c	V_{ISOL}	— — —	4500 3500 1500	Volts
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	100 0.8	40 0.32	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18006	MJF18006	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.25 62.5	3.125 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	—	—	100	μAdc
(T_C = 125°C)		—	—	500	
(V_{CE} = 800 V, V_{EB} = 0) (T_C = 125°C)		—	—	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise specified)

Characteristic				Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS								
Base–Emitter Saturation Voltage (I_C = 1.3 Adc, I_B = 0.13 Adc) (I_C = 3.0 Adc, I_B = 0.6 Adc)				$V_{BE(sat)}$	— —	0.83 0.94	1.2 1.3	Vdc
Collector–Emitter Saturation Voltage (I_C = 1.3 Adc, I_B = 0.13 Adc) (I_C = 3.0 Adc, I_B = 0.6 Adc)			(T_C = 125°C) (T_C = 125°C)	$V_{CE(sat)}$	— — — —	0.25 0.27 0.35 0.4	0.6 0.65 0.7 0.8	Vdc
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 1.3 Adc, V_{CE} = 1.0 Vdc) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)			(T_C = 125°C) (T_C = 125°C) (T_C = 25 to 125°C)	h_{FE}	14 — 6.0 5.0 11 10	— 32 10 8.0 17 22	34 — — — — —	—
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)				f_T	—	14	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)				C_{ob}	—	75	120	pF
Input Capacitance (V_{EB} = 8.0 V)				C_{ib}	—	1000	1500	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18)	(I_C = 1.3 Adc, I_{B1} = 130 mAdc, V_{CC} = 300 V)	1.0 μs	(T_C = 125°C)	$V_{CE(dsat)}$	— —	5.5 12	— —	Volts
		3.0 μs	(T_C = 125°C)		— —	3.0 7.0	— —	
	(I_C = 3.0 Adc, I_{B1} = 0.6 Adc, V_{CC} = 300 V)	1.0 μs	(T_C = 125°C)		— —	9.5 14.5	— —	
		3.0 μs	(T_C = 125°C)		— —	2.0 7.5	— —	
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)								
Turn–On Time	(I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B2} = 1.5 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	— —	90 100	180 —	ns
Turn–Off Time			(T_C = 125°C)	t_{off}	— —	1.7 2.1	2.5 —	μs
Turn–On Time	(I_C = 1.3 Adc, I_{B1} = 0.13 Adc, I_{B2} = 0.65 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	— —	200 130	300 —	ns
Turn–Off Time			(T_C = 125°C)	t_{off}	— —	1.2 1.5	2.5 —	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)								
Fall Time	(I_C = 1.5 Adc, I_{B1} = 0.13 Adc, I_{B2} = 0.65 Adc)		(T_C = 125°C)	t_{fi}	— —	100 120	180 —	ns
Storage Time			(T_C = 125°C)	t_{si}	— —	1.5 1.9	2.5 —	μs
Crossover Time			(T_C = 125°C)	t_c	— —	220 230	350 —	ns
Fall Time	(I_C = 3.0 Adc, I_{B1} = 0.6 Adc, I_{B2} = 1.5 Adc)		(T_C = 125°C)	t_{fi}	— —	85 120	150 —	ns
Storage Time			(T_C = 125°C)	t_{si}	— —	2.15 2.75	3.2 —	μs
Crossover Time			(T_C = 125°C)	t_c	— —	200 310	300 —	ns

TYPICAL STATIC CHARACTERISTICS

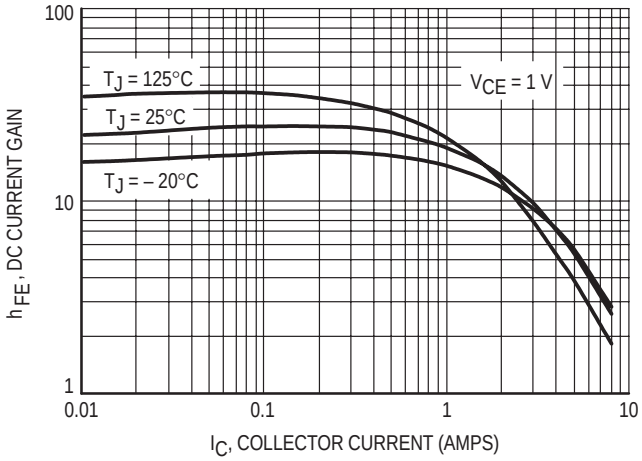


Figure 1. DC Current Gain @ 1 Volt

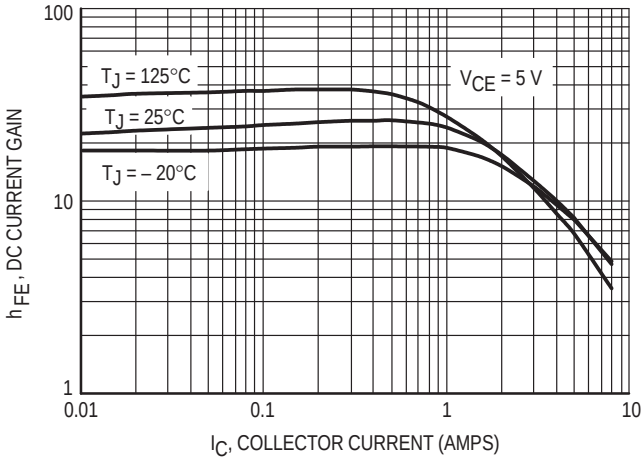


Figure 2. DC Current Gain @ 5 Volts

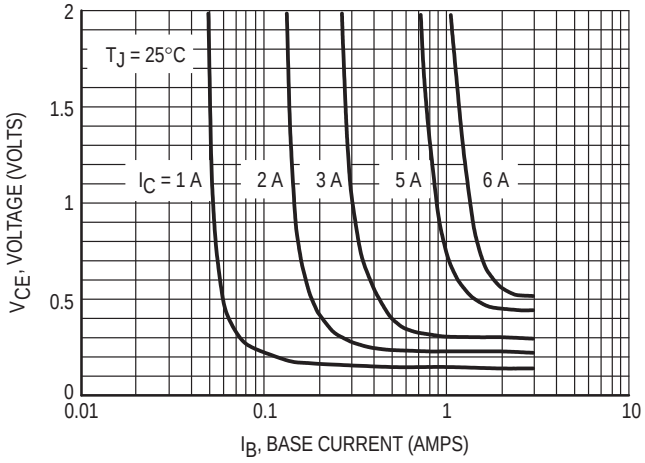


Figure 3. Collector Saturation Region

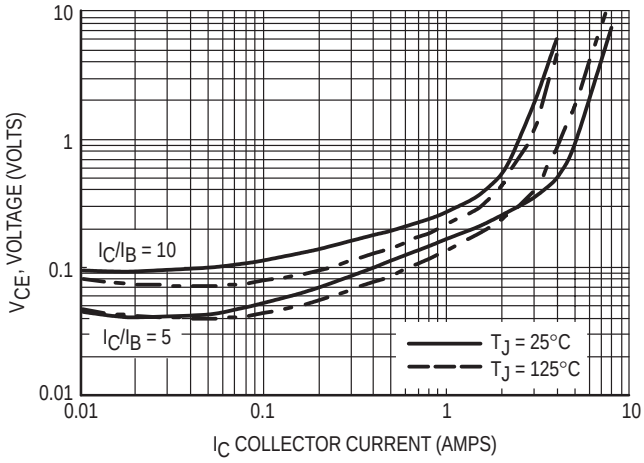


Figure 4. Collector–Emitter Saturation Voltage

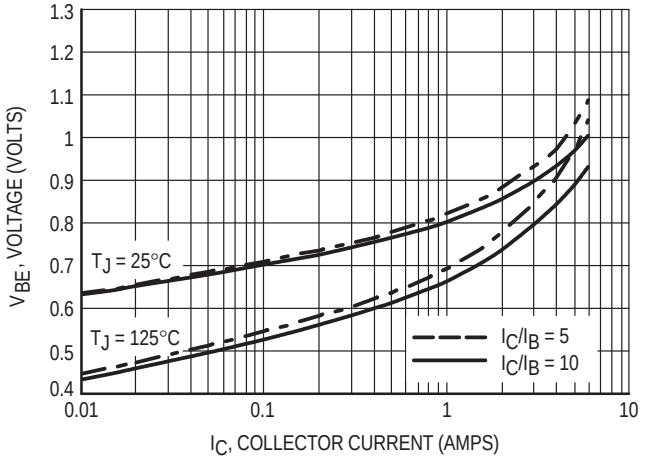


Figure 5. Base–Emitter Saturation Region

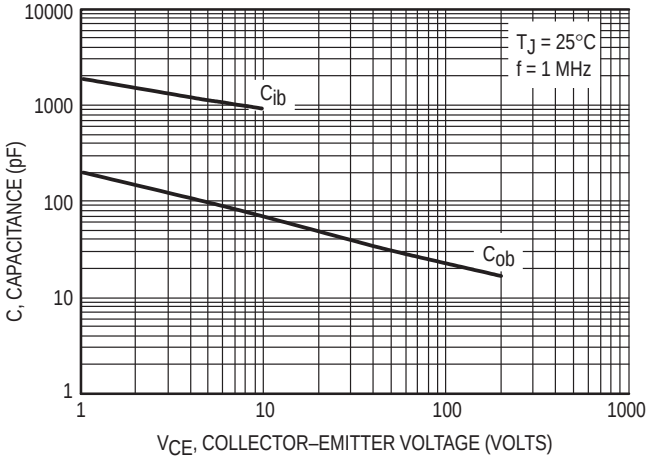


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

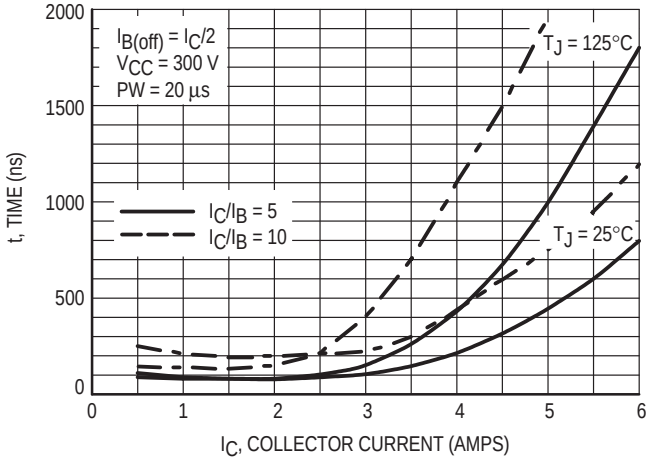


Figure 7. Resistive Switching, t_{on}

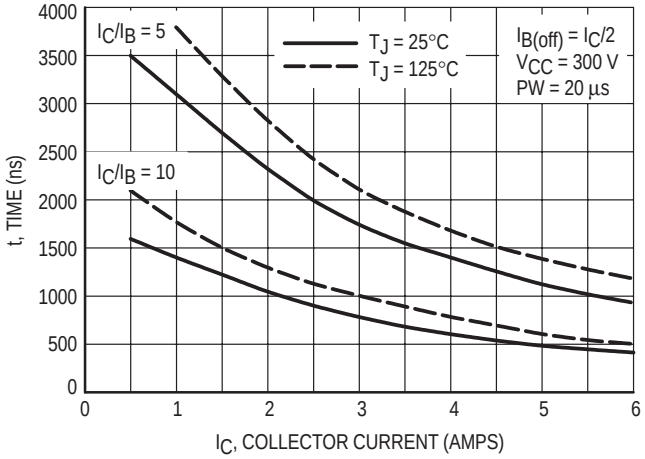


Figure 8. Resistive Switching, t_{off}

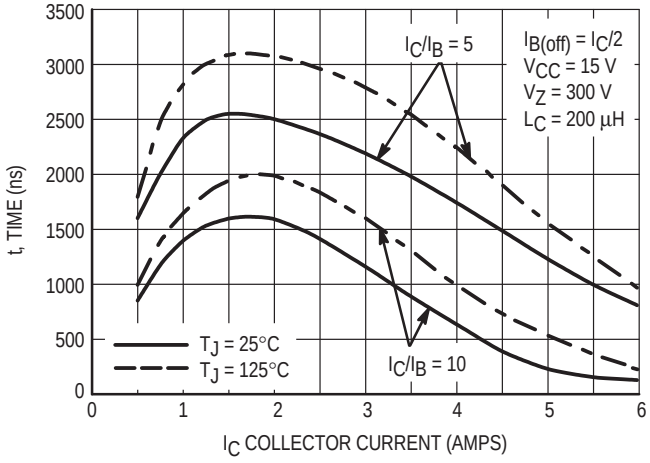


Figure 9. Inductive Storage Time, t_{si}

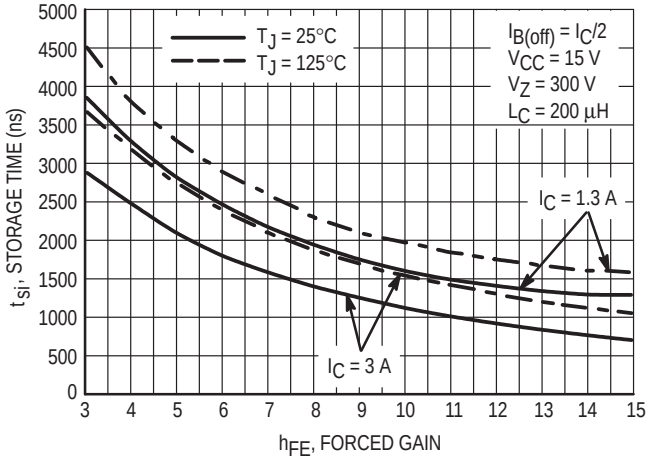


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

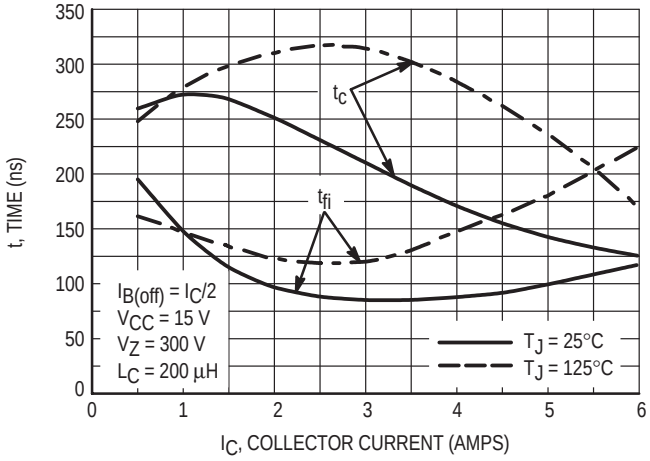


Figure 11. Inductive Switching, t_c and t_{fi}
I_C/I_B = 5

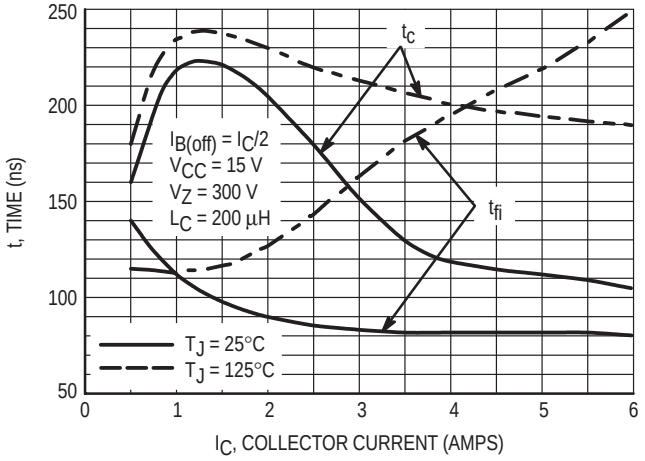


Figure 12. Inductive Switching, t_c and t_{fi}
I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

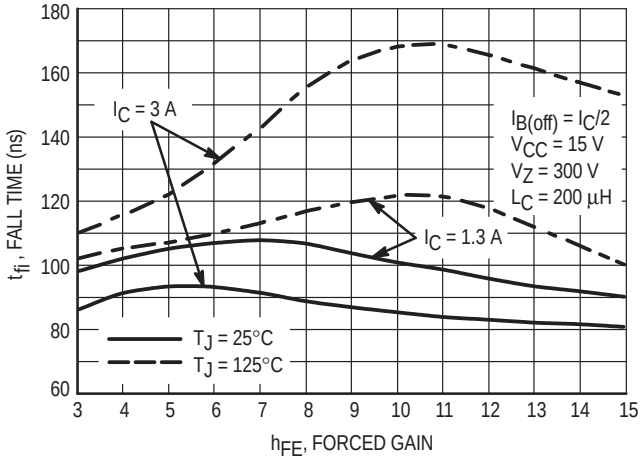


Figure 13. Inductive Fall Time

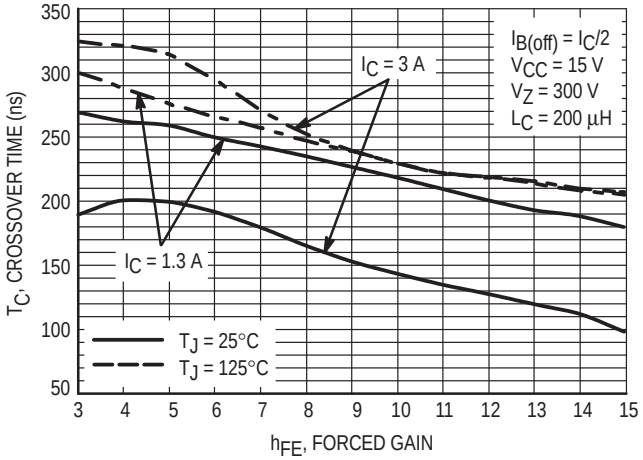


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

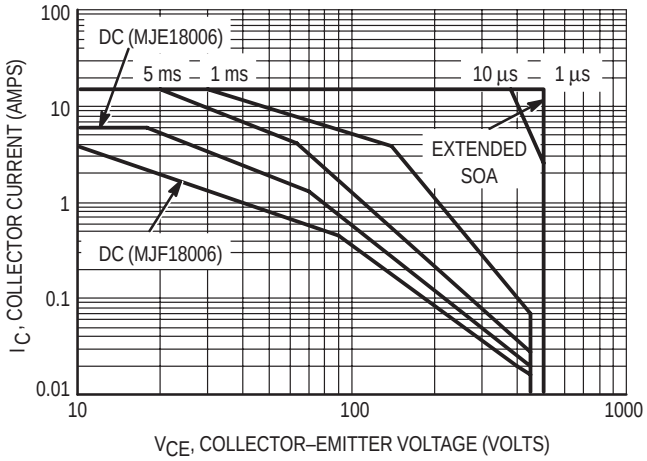


Figure 15. Forward Bias Safe Operating Area

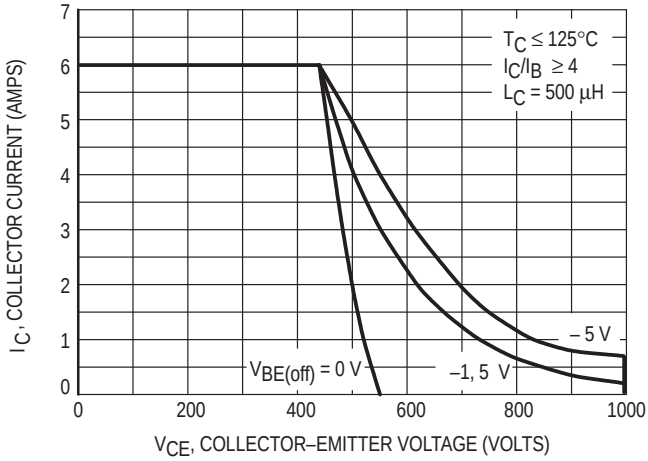


Figure 16. Reverse Bias Switching Safe Operating Area

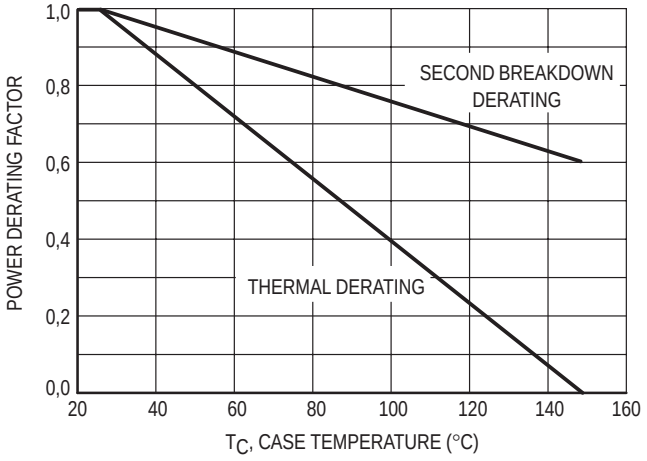


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \ge 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figure 20 and 21. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse–biased. The safe level is specified as a reverse–biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

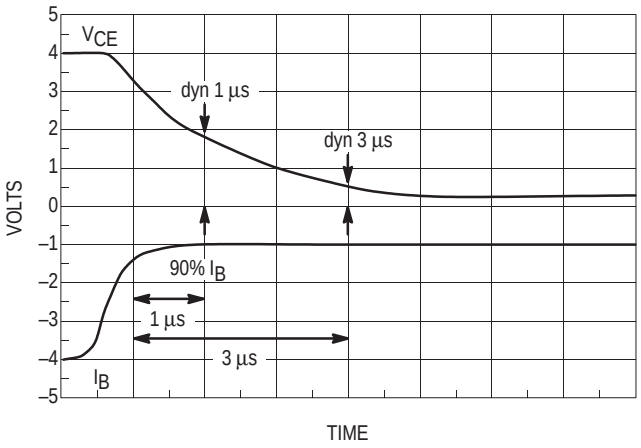


Figure 18. Dynamic Saturation Voltage Measurements

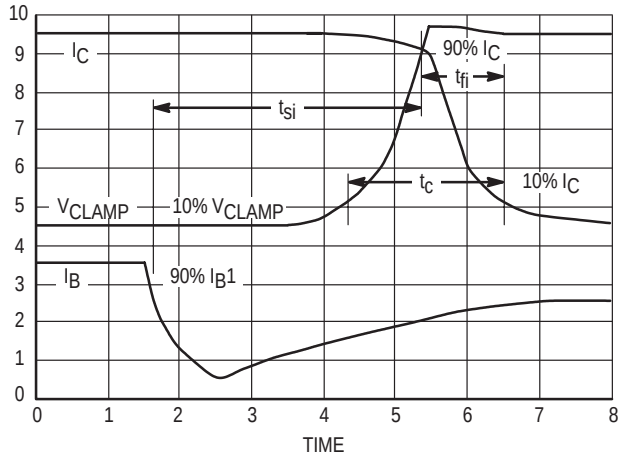
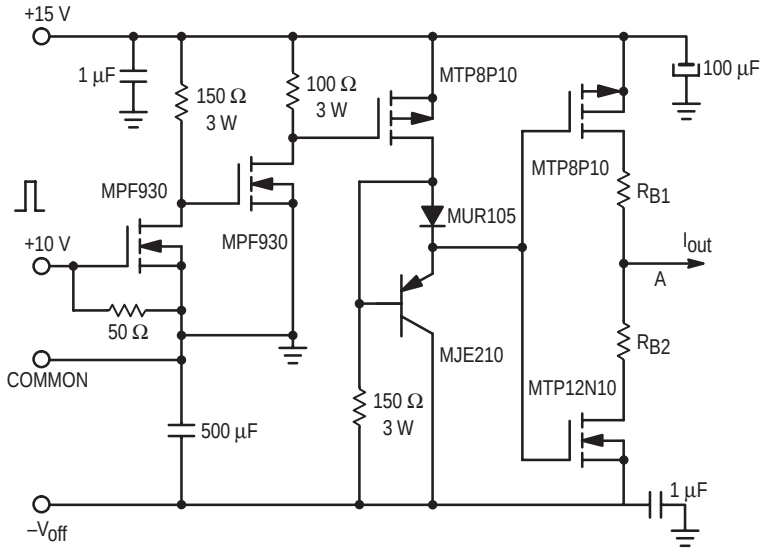
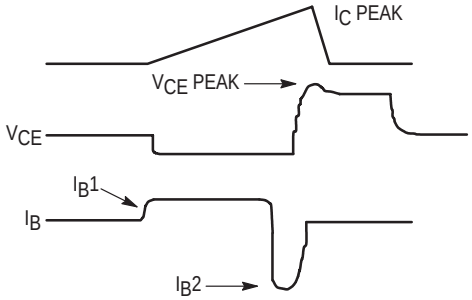


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_B1	RB1 SELECTED FOR DESIRED I_B1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

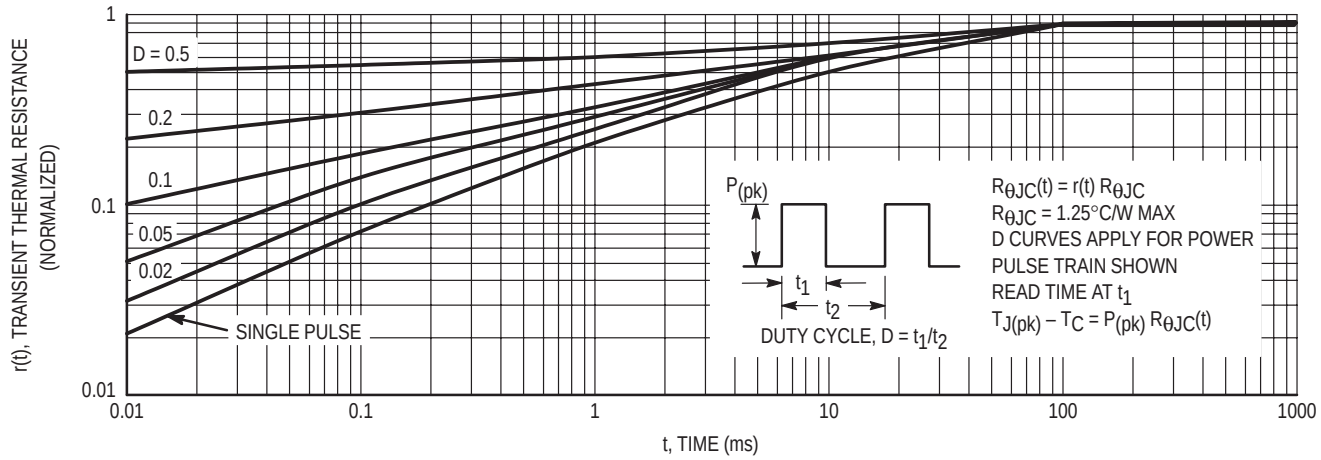


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJE18006

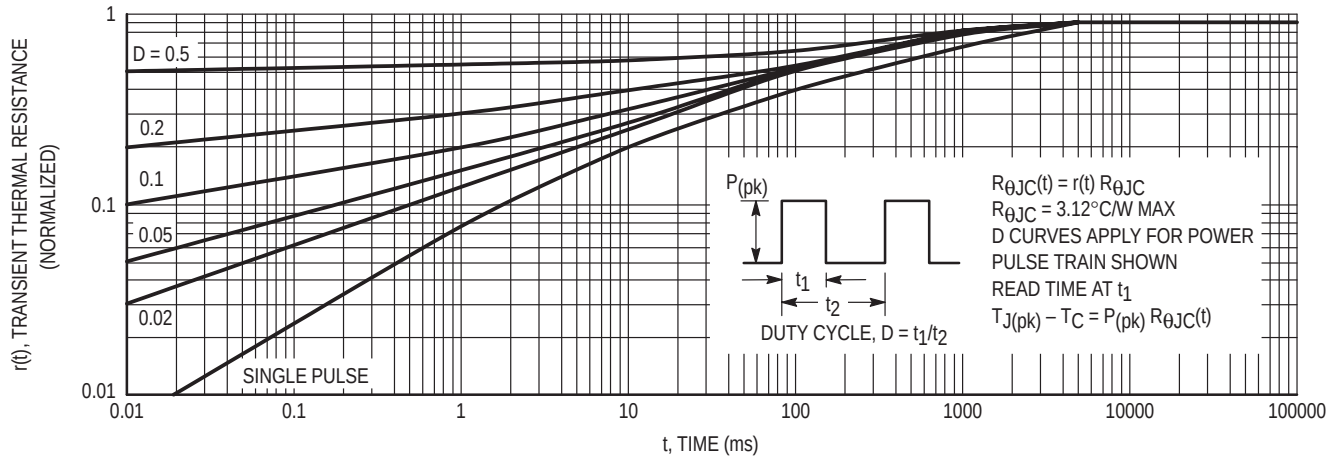


Figure 21. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJF18006

TEST CONDITIONS FOR ISOLATION TESTS*

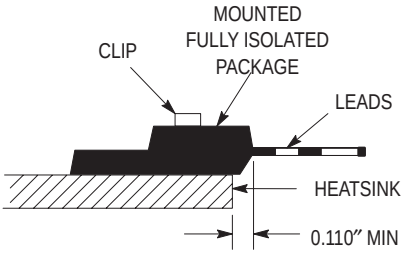


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

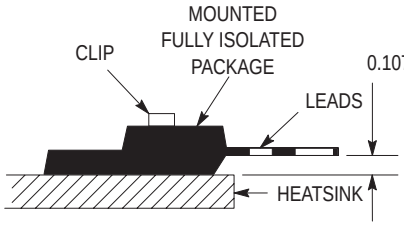


Figure 22b. Clip Mounting Position for Isolation Test Number 2

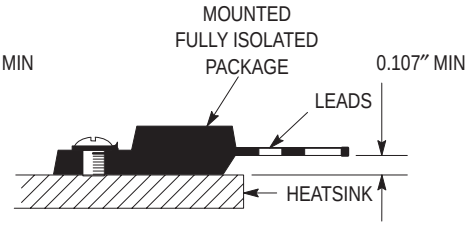


Figure 22c. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION**

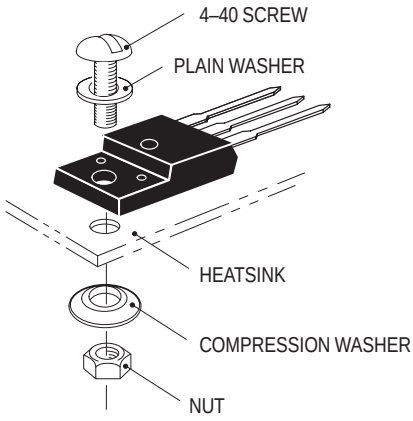


Figure 23a. Screw–Mounted

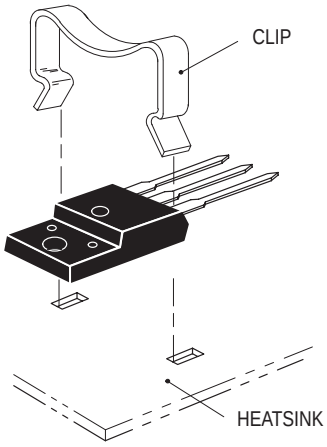


Figure 23b. Clip–Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

Designer's™ Data Sheet
SWITCHMODE™
NPN Bipolar Power Transistor For Switching Power Supply Applications

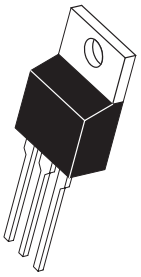
MJE18008*
MJF18008*

*Motorola Preferred Device

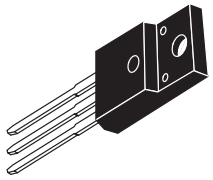
POWER TRANSISTOR
8.0 AMPERES
1000 VOLTS
45 and 125 WATTS

The MJE/MJF18008 have an applications specific state–of–the–art die designed for use in 220 V line–operated Switchmode Power supplies and electronic light ballasts. These high voltage/high speed transistors offer the following:

- Improved Efficiency Due to Low Base Drive Requirements:
  - — High and Flat DC Current Gain h_{FE}
  - — Fast Switching
  - — No Coil Required in Base Circuit for Turn–Off (No Current Tail)
- Tight Parametric Distributions are Consistent Lot–to–Lot
- Two Package Choices: Standard TO–220 or Isolated TO–220
- MJF18008, Case 221D, is UL Recognized at 3500 V_{RMS}: File #E69369



CASE 221A–06
TO–220AB
MJE18008



CASE 221D–02
ISOLATED TO–220 TYPE
UL RECOGNIZED
MJF18008

MAXIMUM RATINGS

Rating	Symbol	MJE18008	MJF18008	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000		Vdc
Emitter–Base Voltage	V_{EBO}	9.0		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	8.0 16		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	4.0 8.0		Adc
RMS Isolation Voltage(2) Test No. 1 Per Fig. 22a (for 1 sec, R.H. < 30%, Test No. 1 Per Fig. 22b T_C = 25°C) Test No. 1 Per Fig. 22c	V_{ISOL}	— — —	4500 3500 1500	Volts
Total Device Dissipation (T_C = 25°C) Derate above 25°C	P_D	125 1.0	45 0.36	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18008	MJF18008	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	2.78 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)	$V_{CEO(sus)}$	450	—	—	Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)	I_{CEO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	I_{CES}	—	—	100	μAdc
(T_C = 125°C)		—	—	500	
(V_{CE} = 800 V, V_{EB} = 0) (T_C = 125°C)		—	—	100	
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise specified)

Characteristic				Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS								
Base–Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc) (I_C = 4.5 Adc, I_B = 0.9 Adc)				$V_{BE(sat)}$	— —	0.82 0.92	1.1 1.25	Vdc
Collector–Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 0.2 Adc) (I_C = 4.5 Adc, I_B = 0.9 Adc)				$V_{CE(sat)}$	 — — — —	 0.3 0.3 0.35 0.4	 0.6 0.65 0.7 0.8	Vdc
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 4.5 Adc, V_{CE} = 1.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 1.0 Vdc) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)				h_{FE}	14 — 6.0 5.0 11 11 10	— 28 9.0 8.0 15 16 20	34 — — — — — —	—
DYNAMIC CHARACTERISTICS								
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)				f_T	—	13	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)				C_{ob}	—	100	150	pF
Input Capacitance (V_{EB} = 8.0 V)				C_{ib}	—	1750	2500	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18)	(I_C = 2.0 Adc I_{B1} = 200 mAdc V_{CC} = 300 V)	1.0 μs	(T_C = 125°C)	$V_{CE(dsat)}$	— —	5.5 11.5	— —	Vdc
		3.0 μs	(T_C = 125°C)		— —	3.5 6.5	— —	
	(I_C = 5.0 Adc I_{B1} = 1.0 Adc V_{CC} = 300 V)	1.0 μs	(T_C = 125°C)		— —	11.5 14.5	— —	
		3.0 μs	(T_C = 125°C)		— —	2.4 9.0	— —	
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)								
Turn–On Time	(I_C = 2.0 Adc, I_{B1} = 0.2 Adc, I_{B2} = 1.0 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	— —	200 190	300 —	ns
Turn–Off Time			(T_C = 125°C)	t_{off}	— —	1.2 1.5	2.5 —	μs
Turn–On Time	(I_C = 4.5 Adc, I_{B1} = 0.9 Adc, I_{B2} = 2.25 Adc, V_{CC} = 300 V)		(T_C = 125°C)	t_{on}	— —	100 250	180 —	ns
Turn–Off Time			(T_C = 125°C)	t_{off}	— —	1.6 2.0	2.5 —	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)								
Fall Time	(I_C = 2.0 Adc, I_{B1} = 0.2 Adc, I_{B2} = 1.0 Adc)		(T_C = 125°C)	t_{fi}	— —	100 120	180 —	ns
Storage Time			(T_C = 125°C)	t_{si}	— —	1.5 1.9	2.75 —	μs
Crossover Time			(T_C = 125°C)	t_c	— —	250 230	350 —	ns
Fall Time	(I_C = 4.5 Adc, I_{B1} = 0.9 Adc, I_{B2} = 2.25 Adc)		(T_C = 125°C)	t_{fi}	— —	85 135	150 —	ns
Storage Time			(T_C = 125°C)	t_{si}	— —	2.0 2.6	3.2 —	μs
Crossover Time			(T_C = 125°C)	t_c	— —	210 250	300 —	ns

TYPICAL STATIC CHARACTERISTICS

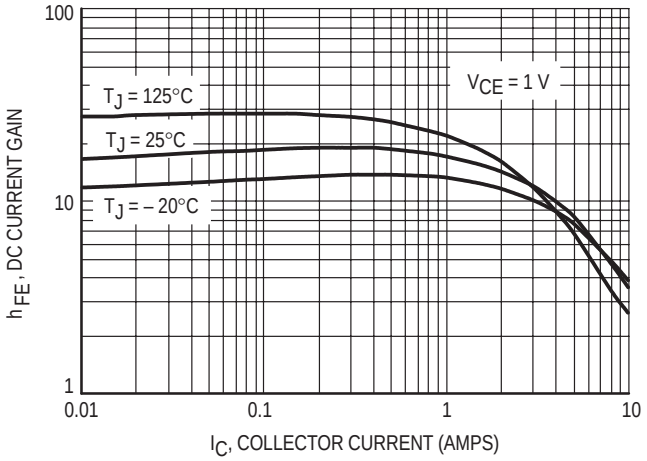


Figure 1. DC Current Gain @ 1 Volt

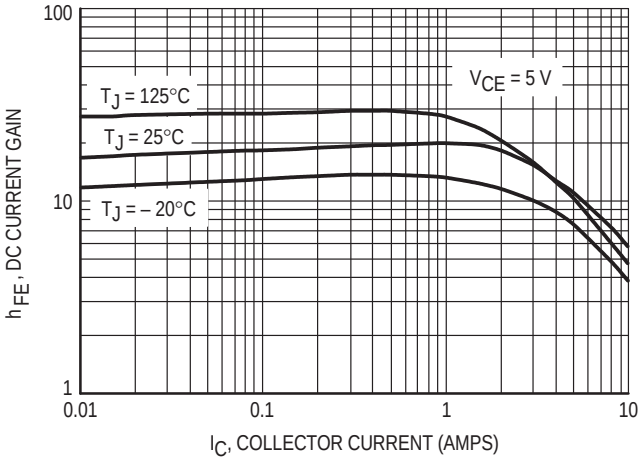


Figure 2. DC Current Gain @ 5 Volts

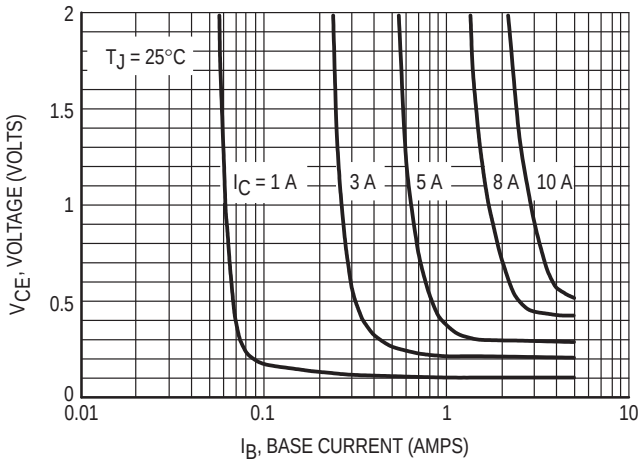


Figure 3. Collector Saturation Region

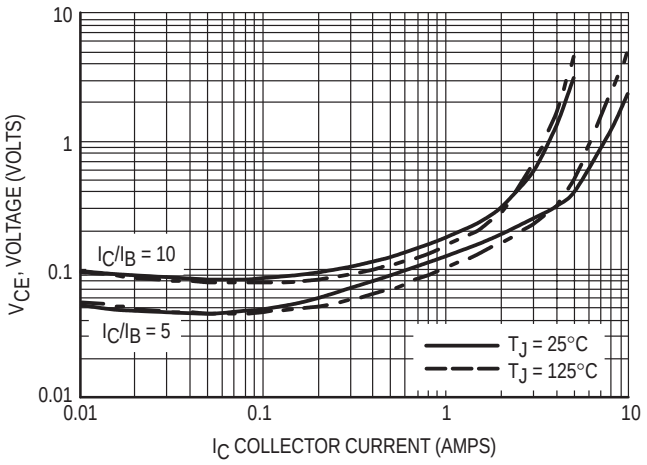


Figure 4. Collector–Emitter Saturation Voltage

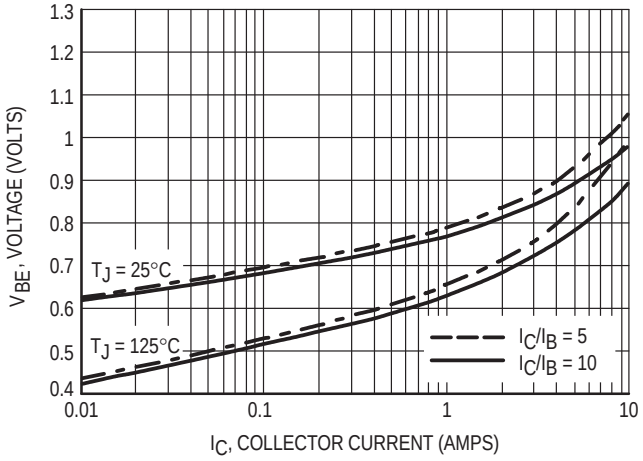


Figure 5. Base–Emitter Saturation Region

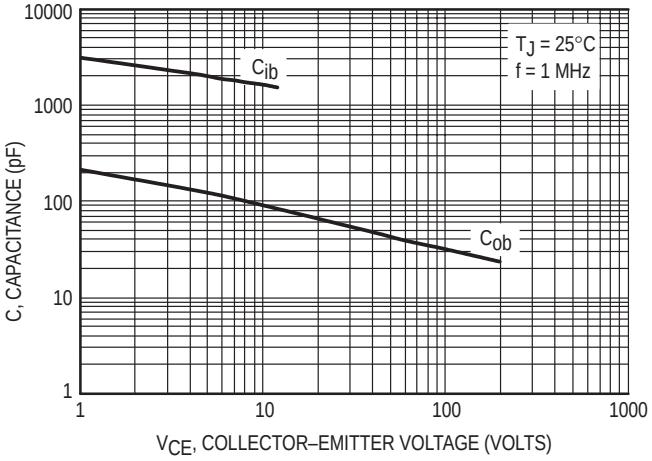


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

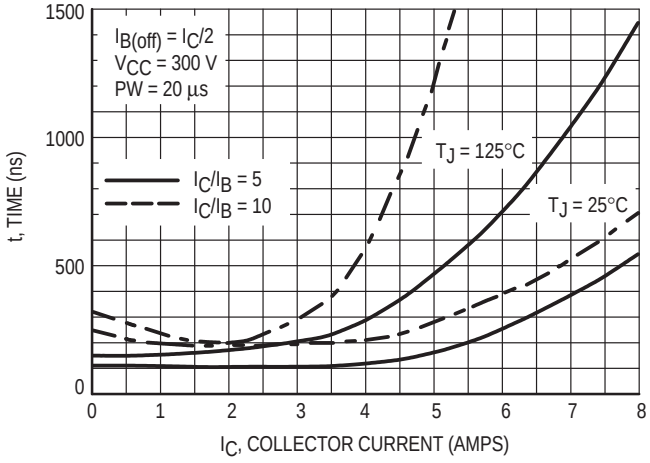


Figure 7. Resistive Switching, t_{on}

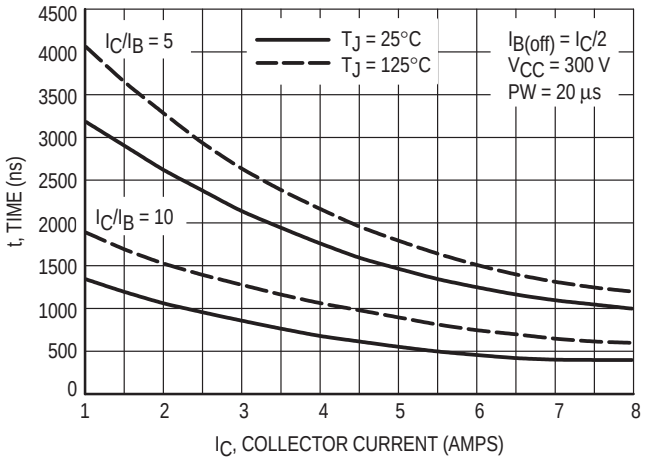


Figure 8. Resistive Switching, t_{off}

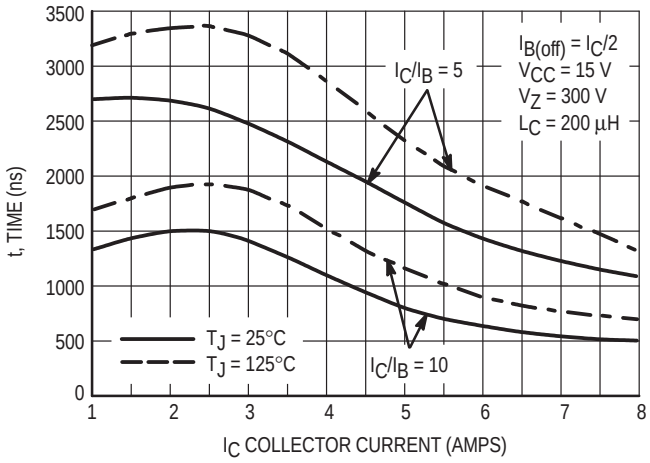


Figure 9. Inductive Storage Time, t_{si}

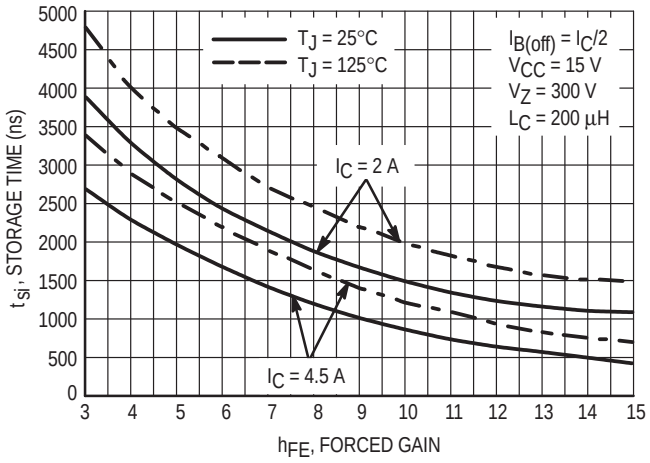


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

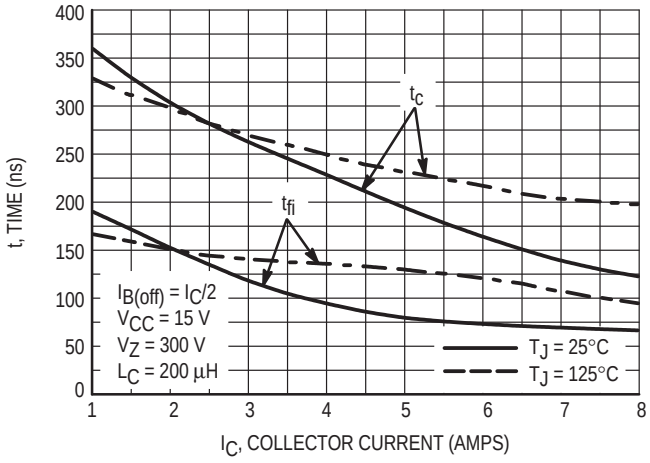


Figure 11. Inductive Switching, t_c and t_{fi}
I_C/I_B = 5

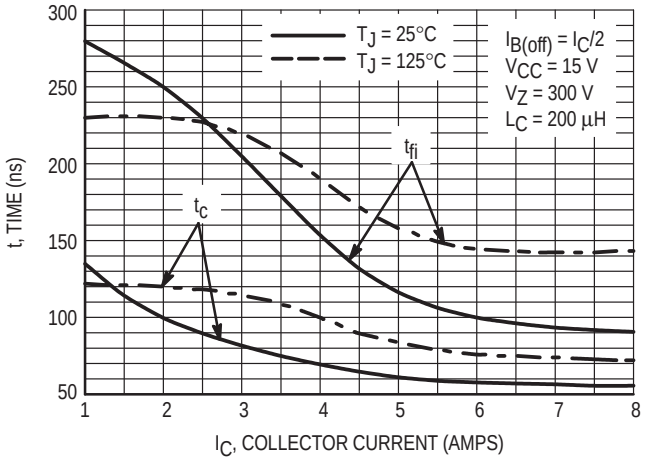


Figure 12. Inductive Switching, t_c and t_{fi}
I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

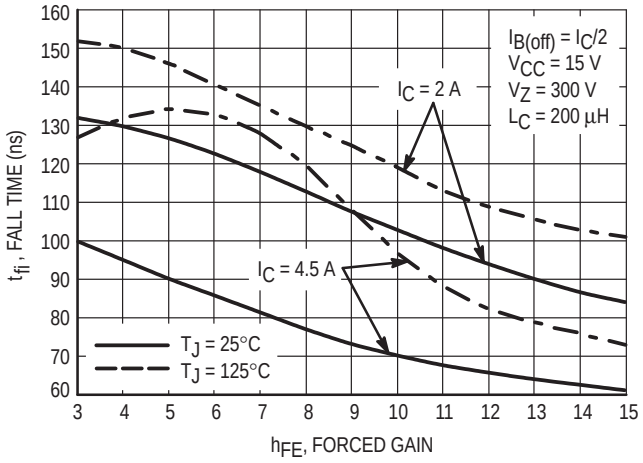


Figure 13. Inductive Fall Time

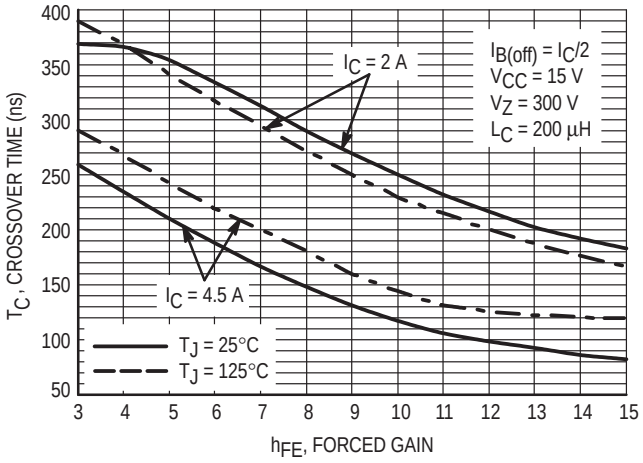


Figure 14. Inductive Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

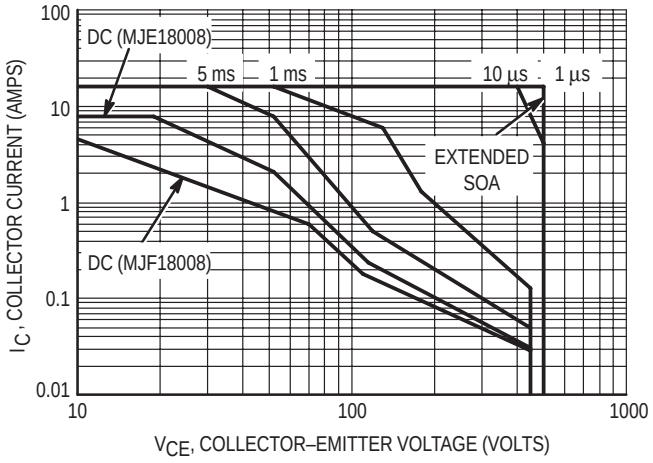


Figure 15. Forward Bias Safe Operating Area

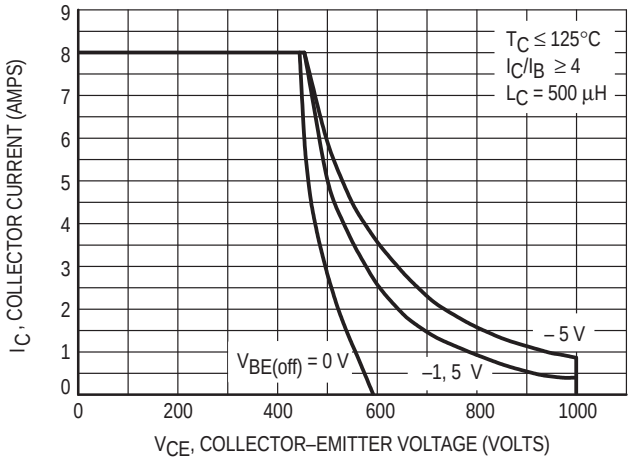


Figure 16. Reverse Bias Switching Safe Operating Area

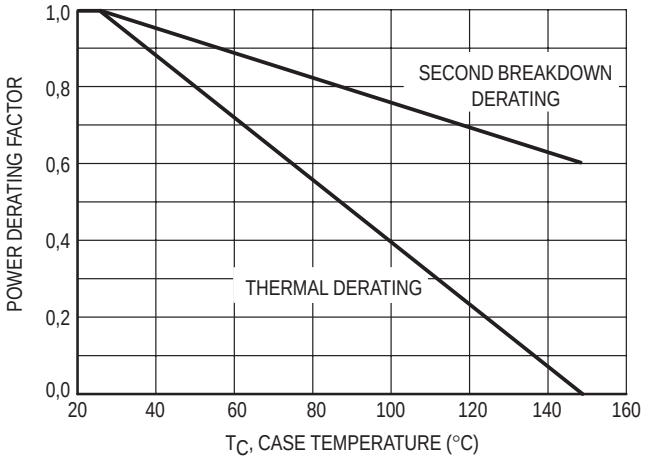


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figure 20 and 21. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse–biased. The safe level is specified as a reverse–biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

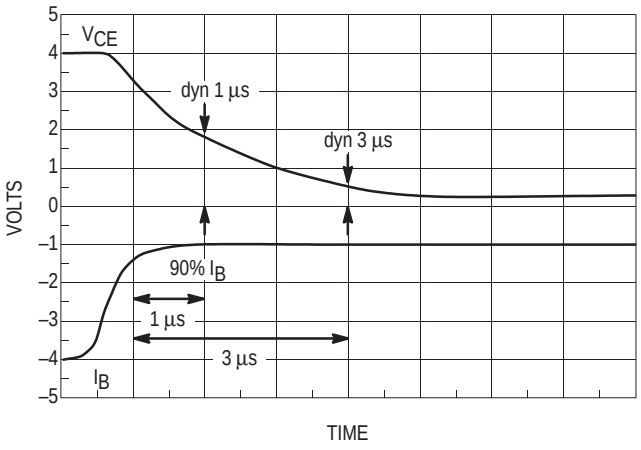


Figure 18. Dynamic Saturation Voltage Measurements

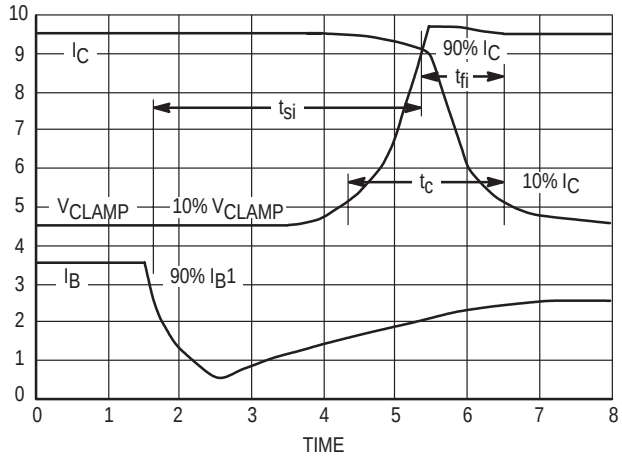
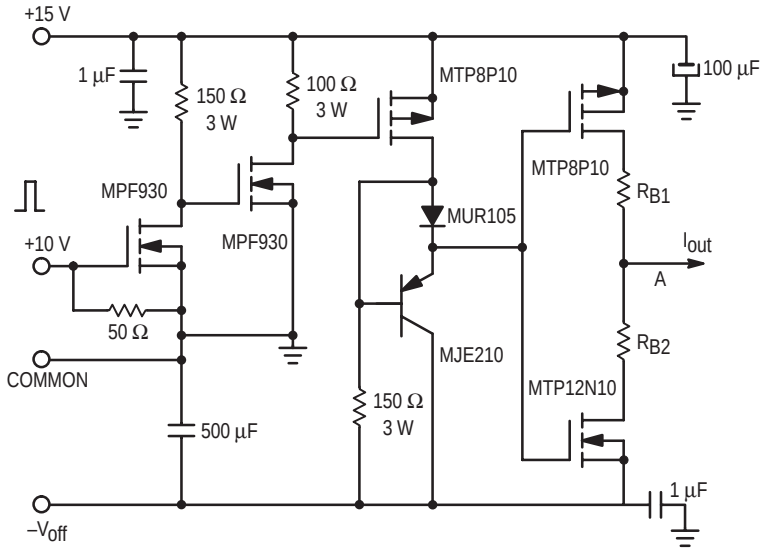
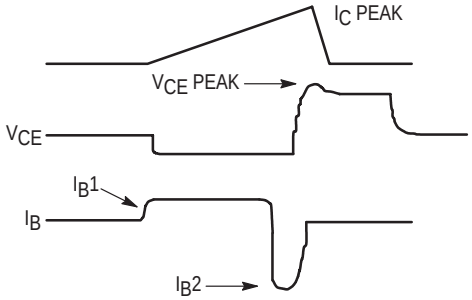


Figure 19. Inductive Switching Measurements





V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
V_{CC} = 20 VOLTS	V_{CC} = 15 VOLTS	V_{CC} = 15 VOLTS
I_C(pk) = 100 mA	RB1 SELECTED FOR DESIRED I_B1	RB1 SELECTED FOR DESIRED I_B1

Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

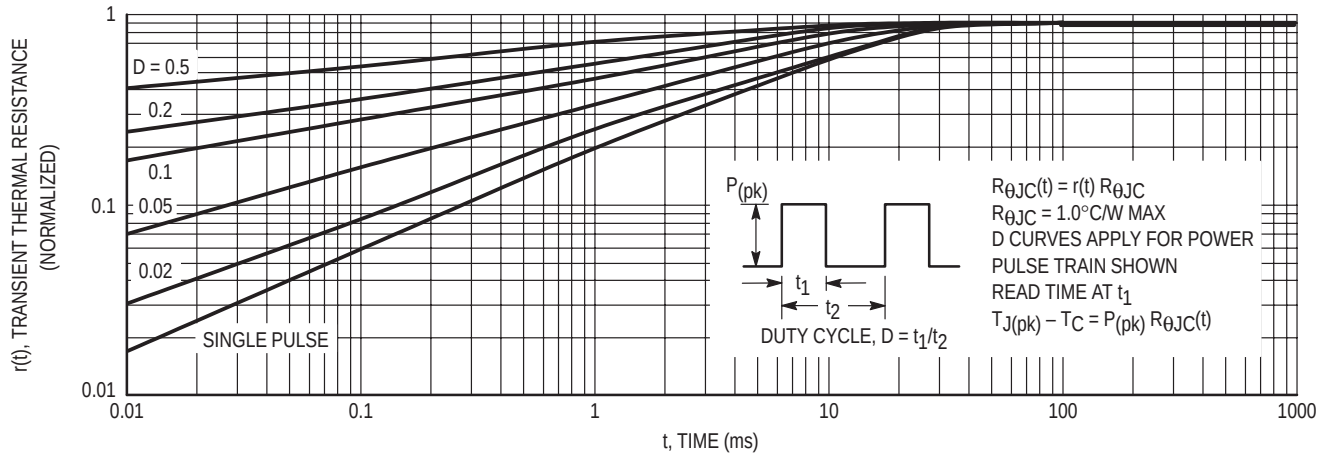


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJE18008

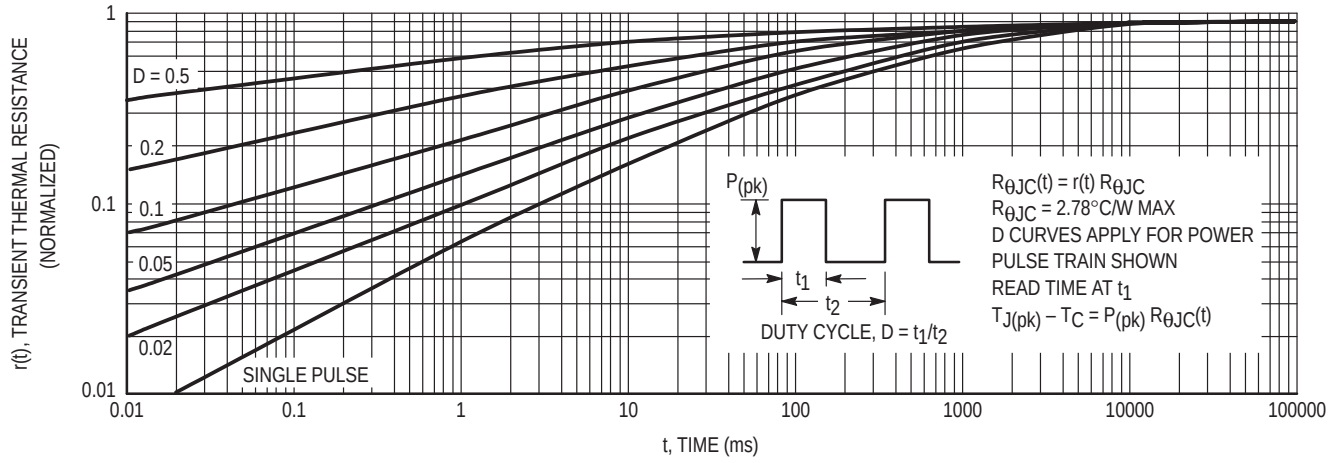


Figure 21. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJF18008

TEST CONDITIONS FOR ISOLATION TESTS*

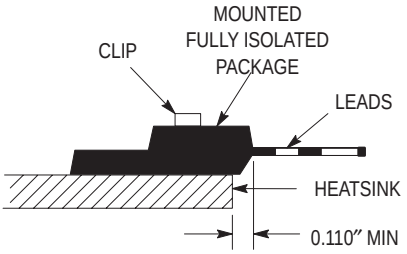


Figure 22a. Screw or Clip Mounting Position for Isolation Test Number 1

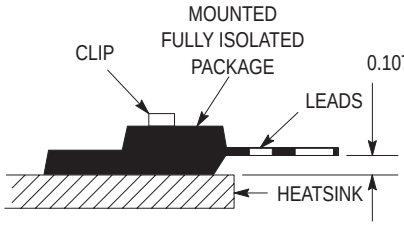


Figure 22b. Clip Mounting Position for Isolation Test Number 2

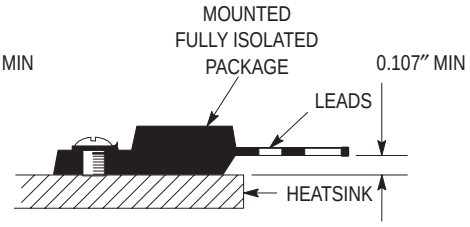


Figure 22c. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION**

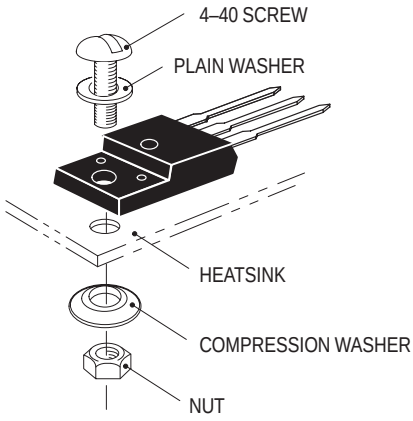


Figure 23a. Screw–Mounted

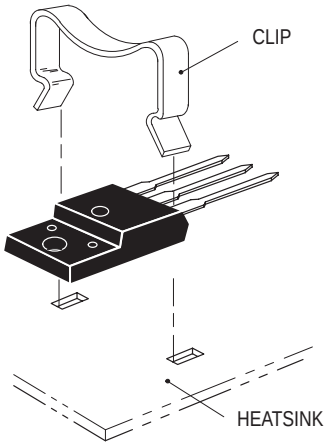


Figure 23b. Clip–Mounted

Figure 23. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

MJE18009
MJF18009

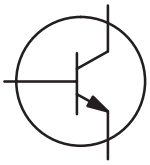
POWER TRANSISTORS
10 AMPERES
1000 VOLTS
50 and 150 WATTS

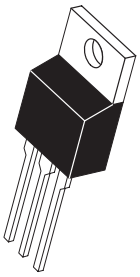
Designer's™ Data Sheet

SWITCHMODE™ NPN Silicon Planar Power Transistor

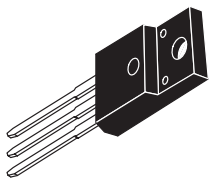
The MJE/MJF18009 has an application specific state–of–the–art die designed for use in 220 V line–operated Switchmode Power supplies and electronic ballast ("light ballast"). These high voltage/high speed transistors exhibit the following main features:

- Improved Efficiency Due to Low Base Drive Requirements:
  - — High and Flat DC Current Gain h_{FE}
  - — Fast Switching
  - — No Coil Required in Base Circuit for Turn–Off (No Current Tail)
- Full Characterization at 125°C
- Motorola "6 SIGMA" Philosophy Provides Tight and Reproducible Parametric Distributions
- Specified Dynamic Saturation Data
- Two Package Choices: Standard TO–220 or Isolated TO–220





CASE 221A–06
TO–220AB



CASE 221D–02
TO–220 FULLPACK

MAXIMUM RATINGS

Rating	Symbol	MJE18009	MJF18009	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450		Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000		Vdc
Collector–Base Breakdown Voltage	V_{CBO}	1000		Vdc
Emitter–Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 20		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4 8		Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	150 1.2	50 0.4	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150		°C
RMS Isolation Voltage (2) Per Figure 22 (1s, 25°C, Humidity ≤ 30%) Per Figure 23 T_C = 25°C Per Figure 24	V_{ISOL1} V_{ISOL2} V_{ISOL3}		4500 3500 1500	V

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18009	MJF18009	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 62.5	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH)		$V_{CEO(sus)}$	450			Vdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, I_B = 0)		I_{CEO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)	@ T_C = 25°C	I_{CES}			100	μAdc
	@ T_C = 125°C				500	
(V_{CE} = 800 V, V_{EB} = 0)	@ T_C = 125°C				100	
Emitter–Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 3 Adc, I_B = 0.3 Adc)				0.8	1.1	
(I_C = 5 Adc, I_B = 1 Adc)				0.9	1.15	
(I_C = 7 Adc, I_B = 1.4 Adc)				0.9	1.25	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 3 Adc, I_B = 0.3 Adc)	@ T_C = 25°C			0.3	0.6	
	@ T_C = 125°C			0.3	0.65	
(I_C = 5 Adc, I_B = 1 Adc)	@ T_C = 25°C			0.3	0.6	
	@ T_C = 125°C			0.3	0.65	
(I_C = 7 Adc, I_B = 1.4 Adc)	@ T_C = 25°C			0.35	0.7	
	@ T_C = 125°C			0.4	0.9	
DC Current Gain		h_{FE}				—
(I_C = 1.5 Adc, V_{CE} = 5 Vdc)	@ T_C = 25°C		14		34	
	@ T_C = 125°C			29		
(I_C = 5 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C		10	13		
	@ T_C = 125°C		8	11.5		
(I_C = 7 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C		7	10		—
	@ T_C = 125°C		5	7.5		
(I_C = 10 mAdc, V_{CE} = 5 Vdc)	@ T_C = 25°C		10	25		—
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T		12		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}		150	200	pF
Input Capacitance (V_{EB} = 8 Vdc)		C_{ib}		2750	3500	pF
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 3 Adc, I_{B1} = 300 mAdc, V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C	$V_{CE(dsat)}$		8		V
			@ T_C = 125°C			13.5		
		@ 3 μs	@ T_C = 25°C			4		
			@ T_C = 125°C			8		
	I_C = 7 Adc, I_{B1} = 1.4 Adc, V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C			15		
			@ T_C = 125°C			21		
		@ 3 μs	@ T_C = 25°C			2		
			@ T_C = 125°C			2.7		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)							
Turn–on Time	I_C = 3 Adc, I_{B1} = 0.3 Adc I_{B2} = 1.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		220 220	300	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		1.28 1.6	2.5	μs
Turn–on Time	I_C = 5 Adc, I_{B1} = 1 Adc I_{B2} = 2.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		120 350	250	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		2.2 2.6	2.5	μs
Turn–on Time	I_C = 7 Adc, I_{B1} = 1.4 Adc I_{B2} = 3.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		175 500	300	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		1.75 2.1	2.5	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 3 Adc I_{B1} = 0.3 Adc I_{B2} = 1.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		110 125	200	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		2 2.6	2.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		250 300	350	ns
Fall Time	I_C = 5 Adc I_{B1} = 1 Adc I_{B2} = 2.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		110 135	200	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		2.4 3.1	3.5	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		260 300	350	ns
Fall Time	I_C = 7 Adc I_{B1} = 1.4 Adc I_{B2} = 3.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		105 150	200	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		1.75 2.25	2.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		225 300	350	ns

TYPICAL STATIC CHARACTERISTICS

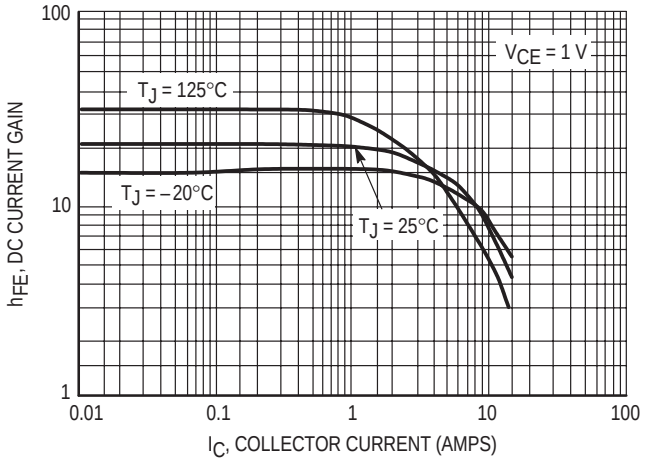


Figure 1. DC Current Gain @ 1 Volt

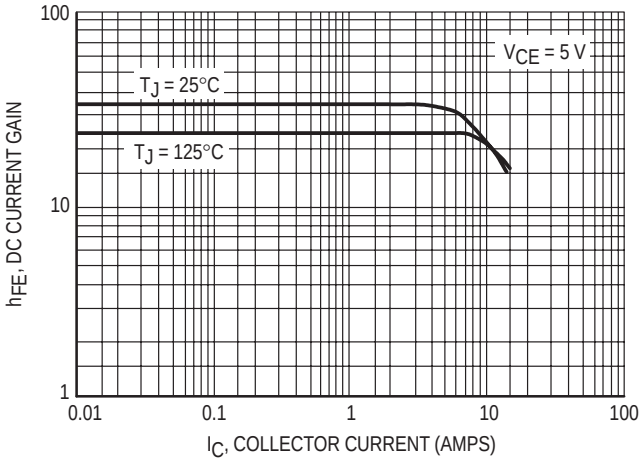


Figure 2. DC Current Gain @ 5 Volt

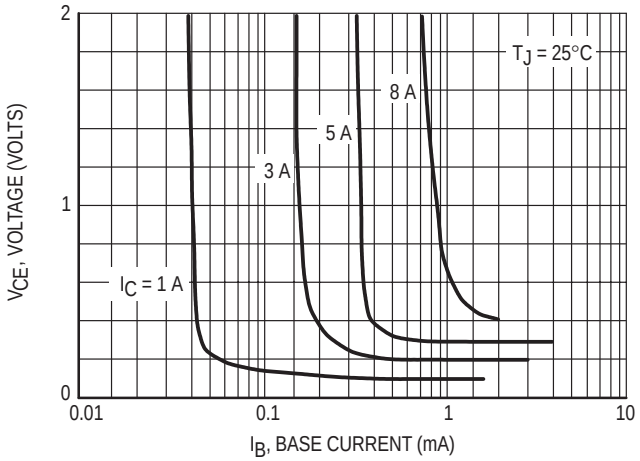


Figure 3. Collector Saturation Region

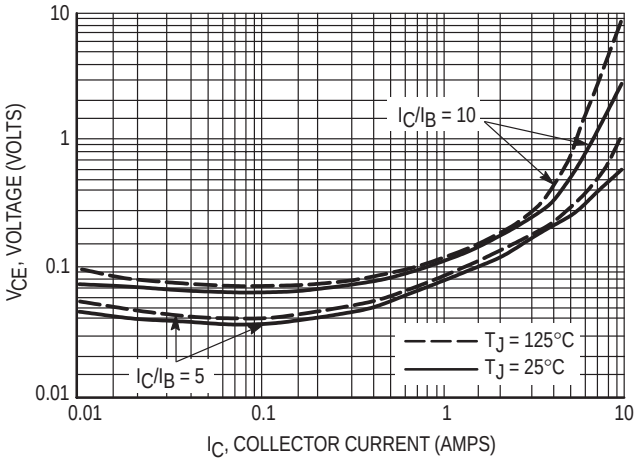


Figure 4. Collector–Emitter Saturation Voltage

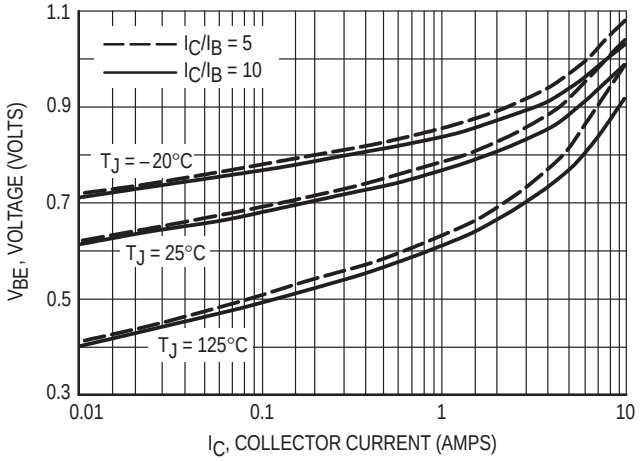


Figure 5. Base–Emitter Saturation Region

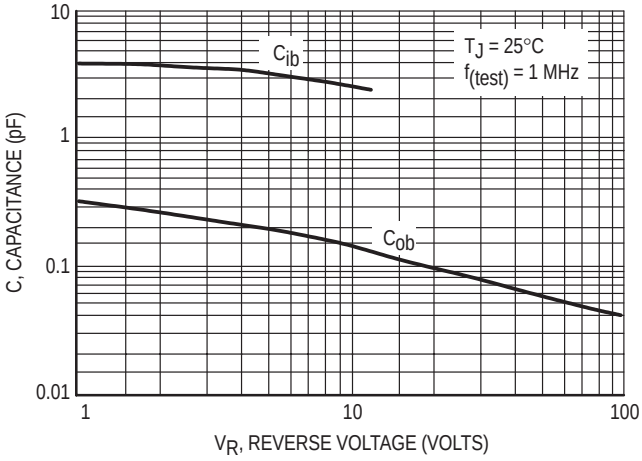


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS

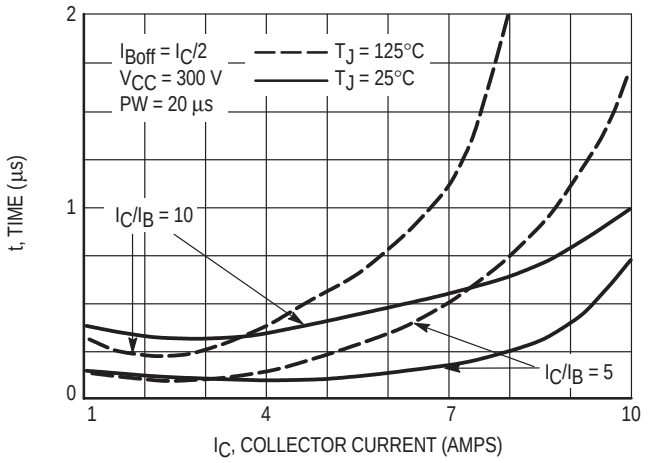


Figure 7. Resistive Switching, t_{on}

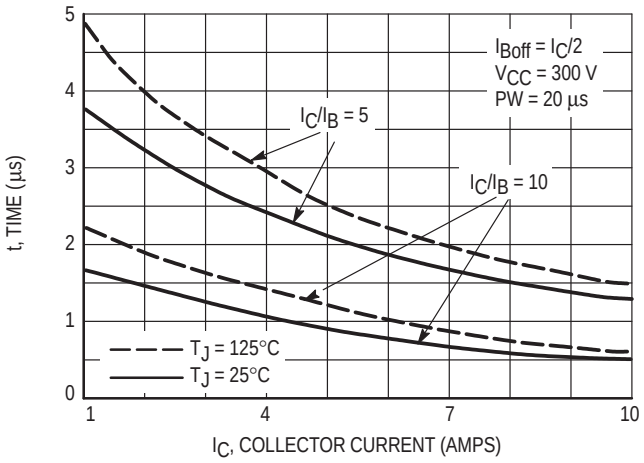


Figure 8. Resistive Switching, t_{off}

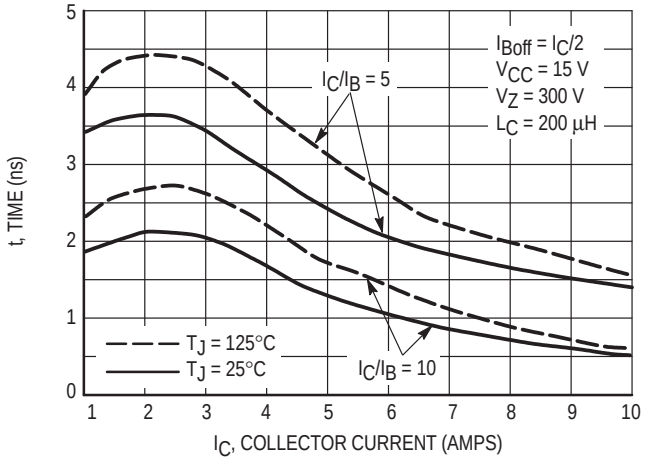


Figure 9. Inductive Storage Time, t_{si}

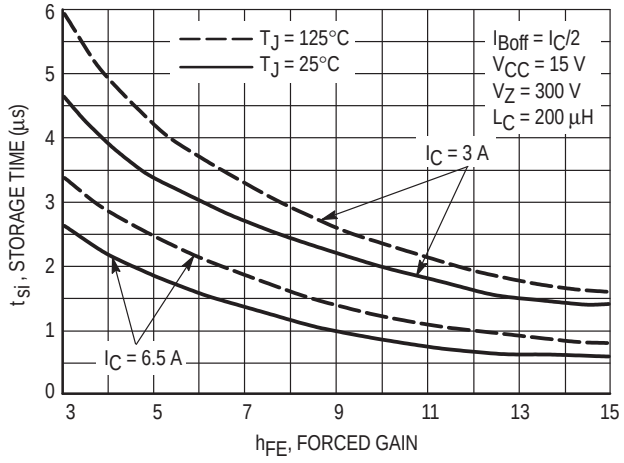


Figure 10. Inductive Storage Time

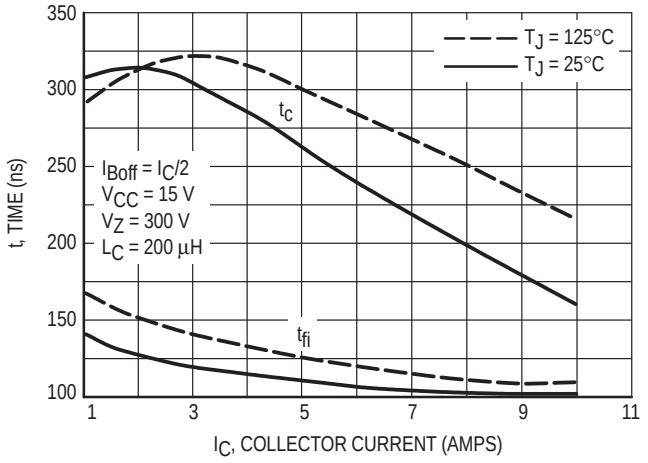


Figure 11. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 5

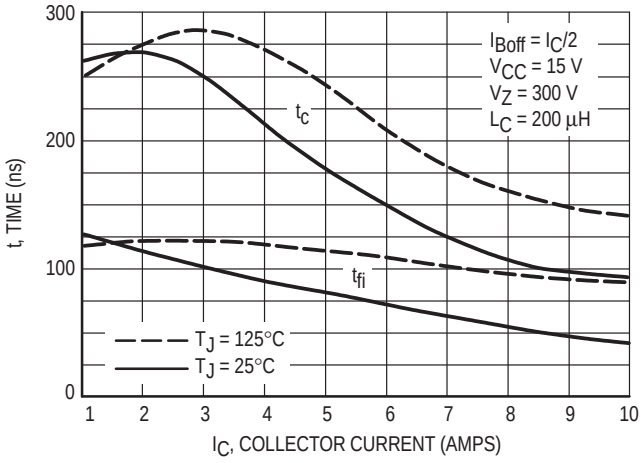


Figure 12. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 10

TYPICAL SWITCHING CHARACTERISTICS

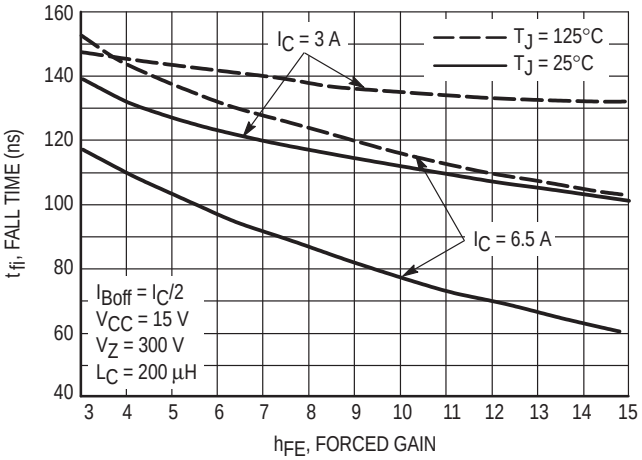


Figure 13. Inductive Fall Time

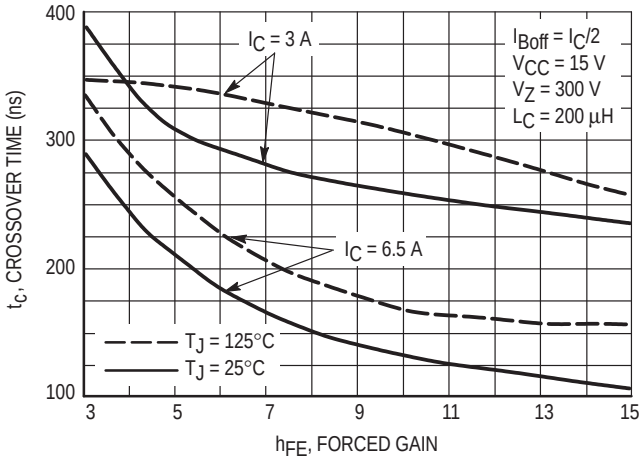


Figure 14. Inductive Crossover Time

TYPICAL CHARACTERISTICS

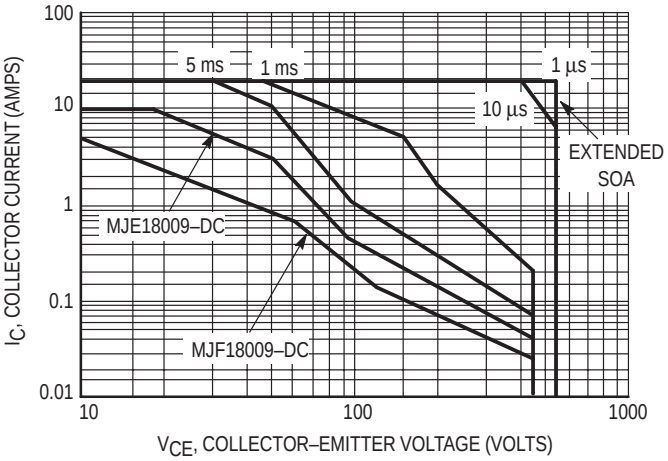


Figure 15. Forward Bias Safe Operating Area

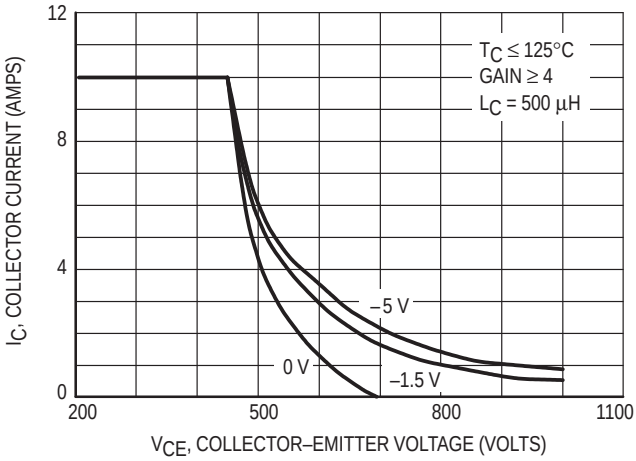


Figure 16. Reverse Bias Switching Safe Operating Area

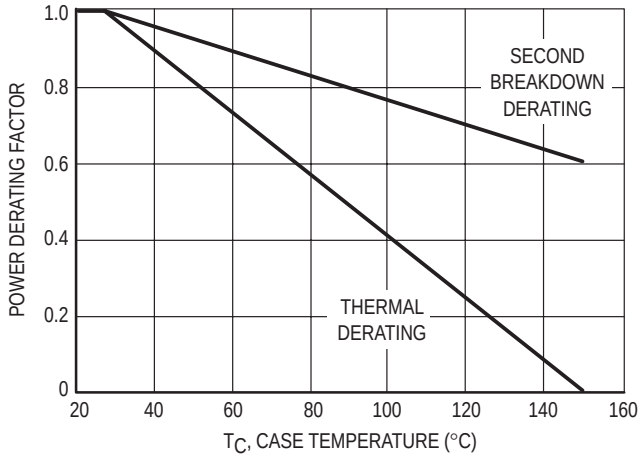


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on T_C = 25°C; T_J(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17.

T_J(pk) may be calculated from the data in Figures 20 and 21. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse biased. The safe level is specified as a reverse–biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL SWITCHING CHARACTERISTICS
($I_B = I_C/2$ FOR ALL CURVES)

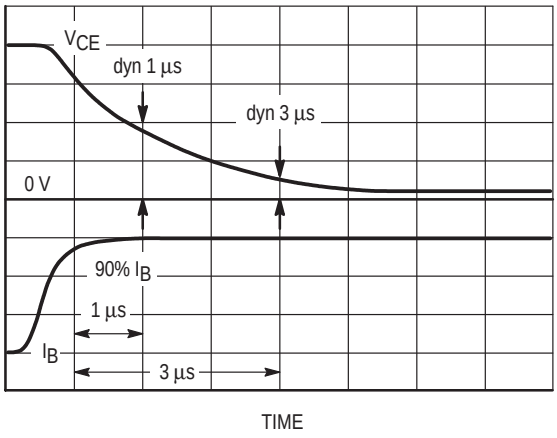


Figure 18. Dynamic Saturation Voltage Measurements

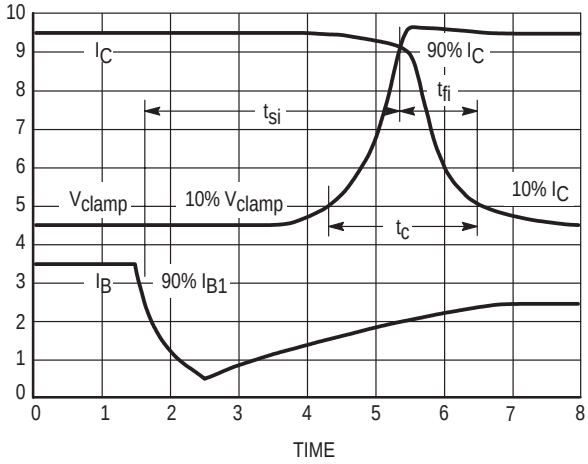
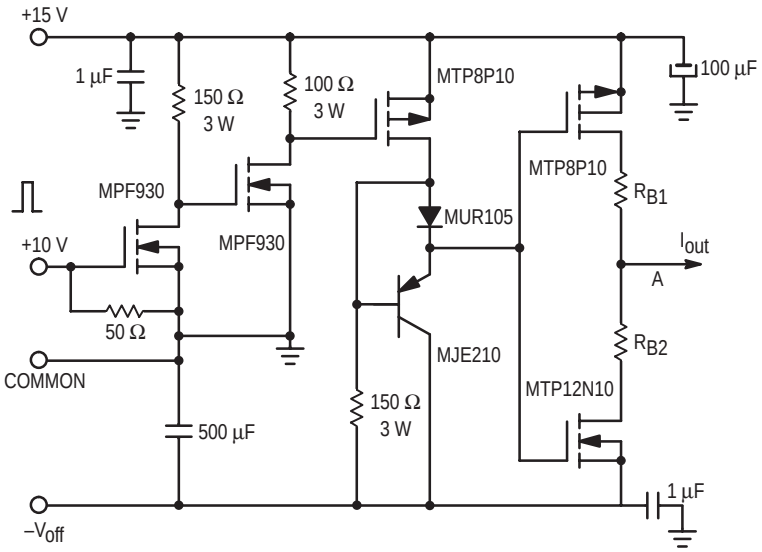
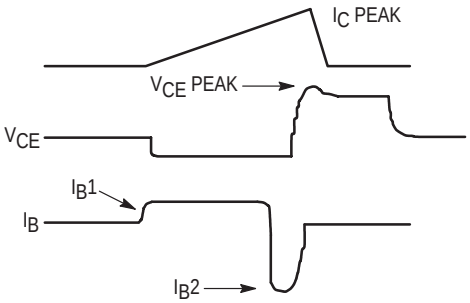


Figure 19. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
$R_{B2} = \infty$	$R_{B2} = 0$	$R_{B2} = 0$
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL THERMAL RESPONSE
($I_B = I_C/2$ FOR ALL CURVES)

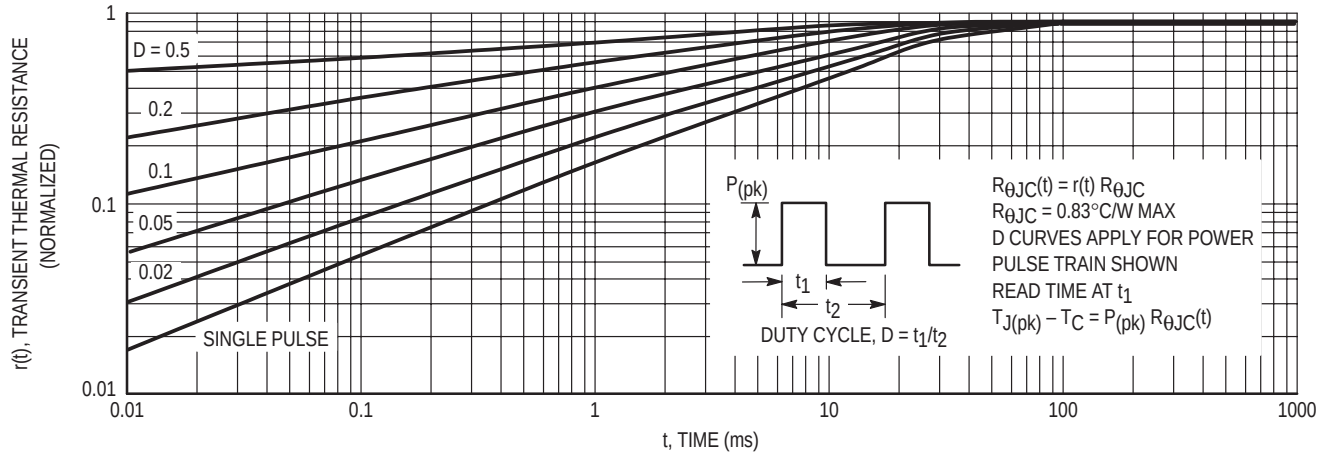


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJE18009

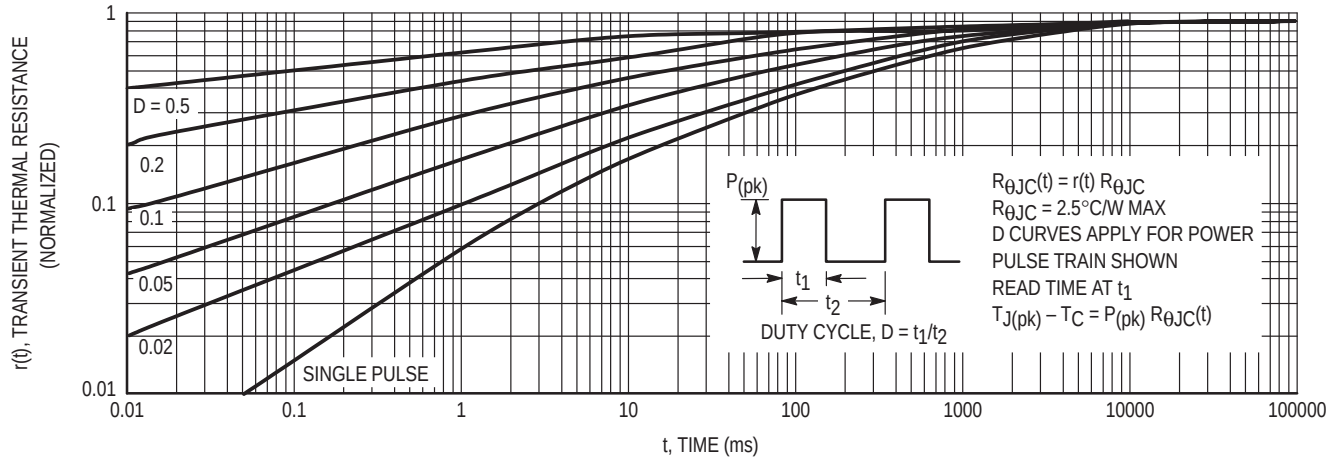


Figure 21. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJF18009

TEST CONDITIONS FOR ISOLATION TESTS*

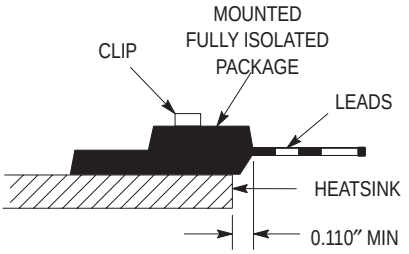


Figure 22. Clip Mounting Position for Isolation Test Number 1

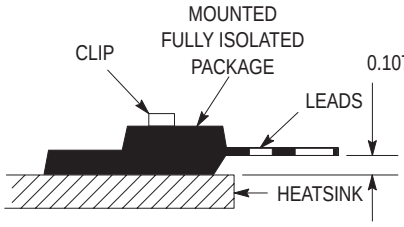


Figure 23. Clip Mounting Position for Isolation Test Number 2

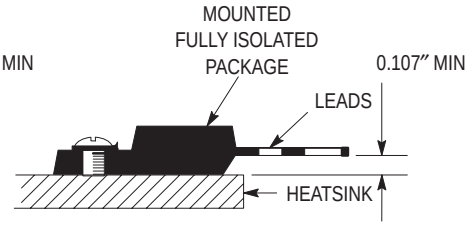


Figure 24. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION**

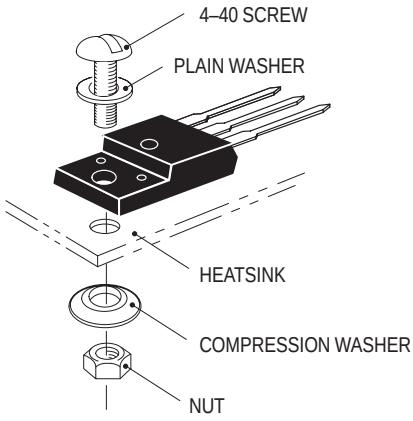


Figure 25a. Screw–Mounted

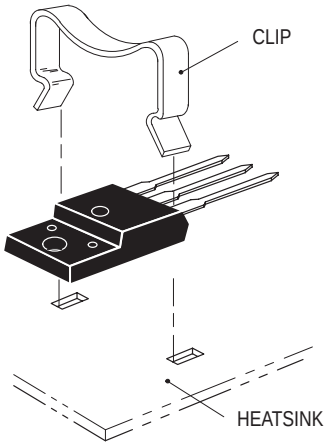


Figure 25b. Clip–Mounted

Figure 25. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

MJE18204
MJF18204

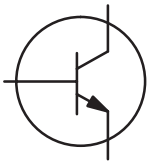
POWER TRANSISTORS
5 AMPERES
1200 VOLTS
35 and 75 WATTS

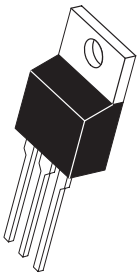
Designer's™ Data Sheet

SWITCHMODE™ NPN Bipolar Power Transistor for Electronic Light Ballast and Switching Power Supply Applications

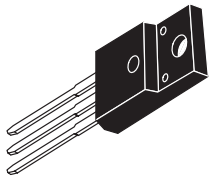
The MJE/MJF18204 have an application specific state–of–the–art die dedicated to the electronic ballast ("light ballast") and power supply applications.

- Improved Global Efficiency Due to Low Base Drive Requirements:
  - — High and Flat DC Current Gain h_{FE}
  - — Fast Switching
  - — No Coil Required in Base Circuit for Fast Turn–Off (No Current Tail)
- Full Characterization at 125°C
- Motorola "6 SIGMA" Philosophy Provides Tight and Reproducible Parametric Distributions
- Two Package Choices: Standard TO–220 or Isolated TO–220





CASE 221A–06
TO–220AB



CASE 221D–02
TO–220 FULLPACK

MAXIMUM RATINGS

Rating	Symbol	MJE18204	MJF18204	Unit
Collector–Emitter Voltage	V_{CEO}	600		Vdc
Collector–Base Voltage	V_{CBO}	1200		Vdc
Collector–Emitter Voltage	V_{CES}	1200		Vdc
Emitter–Base Voltage	V_{EBO}	10		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	5 10		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4		Adc
RMS Isolation Voltage (2) Per Figure 22 (for 1 sec, R.H. ≤ 30%) Per Figure 23 T_C = 25°C Per Figure 24	V_{ISOL1} V_{ISOL2} V_{ISOL3}		4500 3500 1500	Volts
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	75 0.6	35 0.28	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18204	MJF18204	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	3.55 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Voltage (I_C = 1 mA, I_B = 0)		V_{CEO}	600	660		Vdc
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH) (I_C = 200 mA, L = 25 mH, R = 2 Ω)		$V_{CEO(sus)}$ $V_{CER(sus)}$	550 600	630 700		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA, I_E = 0)		V_{CBO}	1200	1300		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA, I_C = 0)		V_{EBO}	10	12.9		Vdc
Collector Cutoff Current (V_{CE} = 600 V, I_B = 0) (V_{CE} = 550 V, I_B = 0)	@ T_C = 25°C @ T_C = 125°C	I_{CEO}			200 2000	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{BE} = 0) (V_{CE} = 1000 V, V_{BE} = 0)	@ T_C = 25°C @ T_C = 125°C @ T_C = 125°C	I_{CES}			100 500 100	μAdc
Collector Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)		I_{CBO}			100	μAdc
Emitter–Cutoff Current (V_{EB} = 10 Vdc, I_C = 0)		I_{EBO}			100	μAdc
ON CHARACTERISTICS						
Base–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.1 Adc) (I_C = 2 Adc, I_B = 0.4 Adc)		$V_{BE(sat)}$		0.83 0.92	1.1 1.25	Vdc
Collector–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.1 Adc)	@ T_C = 25°C @ T_C = 125°C	$V_{CE(sat)}$		0.3 0.7	1 1.25	Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)	@ T_C = 25°C @ T_C = 125°C			0.3 0.8	0.6 1.25	
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3 Vdc)	@ T_C = 25°C @ T_C = 125°C	h_{FE}	18	23	35	—
(I_C = 1 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		10 8	13	22	
(I_C = 2 Adc, V_{CE} = 1 Vdc)	@ T_C = 25°C @ T_C = 125°C		5 4	8 6		—
(I_C = 5 mAdc, V_{CE} = 5 Vdc)	@ T_C = 25°C @ T_C = 125°C		10	25 33		—
DYNAMIC CHARACTERISTICS						
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)		C_{ob}			200	pF
Input Capacitance (V_{EB} = 8 Vdc)		C_{ib}			2000	pF
DYNAMIC SATURATION VOLTAGE						
Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 2 Adc, I_{B1} = 660 mAdc, V_{CC} = 300 V; @ 3 μs; @ T_C = 25°C	$V_{CE(dsat)}$		2.5		V
	@ T_C = 125°C			7.5		
	I_C = 2 Adc, I_{B1} = 0.4 Adc, V_{CC} = 300 V; @ 3 μs; @ T_C = 25°C			7		
	@ T_C = 125°C			15		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 20 μs)							
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 1 Adc V_{CC} = 300 Vdc	@ T_C = 25°C	t_{on}		105	175	ns
Turn–off Time		@ T_C = 25°C	t_{off}		1.75	2.5	μs
Turn–on Time	I_C = 2 Adc, I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc V_{CC} = 300 Vdc	@ T_C = 25°C	t_{on}		95	200	ns
Turn–off Time		@ T_C = 25°C	t_{off}		3.5	4.5	μs
Turn–on Time	I_C = 0.7 Adc, I_{B1} = 50 mAdc I_{B2} = 0.4 Adc V_{CC} = 125 Vdc PW = 70 μs	@ T_C = 25°C	t_d		70	150	ns
			t_r		210	400	ns
Turn–off Time		@ T_C = 25°C	t_s		0.9	1.2	μs
			t_f		275	450	ns
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 1 Adc I_{B1} = 0.1 Adc I_{B2} = 0.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		110 95	175	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		1.35 1.9	2	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		150 115	250	ns
Fall Time	I_C = 2 Adc I_{B1} = 0.4 Adc I_{B2} = 1 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		120 180	200	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		1.9 2.35	2.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		190 180	300	ns
Fall Time	I_C = 2 Adc I_{B1} = 0.4 Adc I_{B2} = 0.4 Adc	@ T_C = 25°C	t_f		185	300	ns
Storage Time		@ T_C = 25°C	t_s		4	5	μs
Crossover Time		@ T_C = 25°C	t_c		350	500	ns

TYPICAL STATIC CHARACTERISTICS

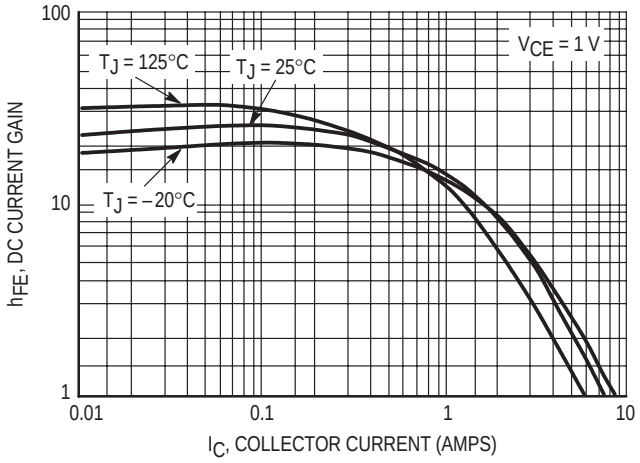


Figure 1. DC Current Gain @ 1 Volt

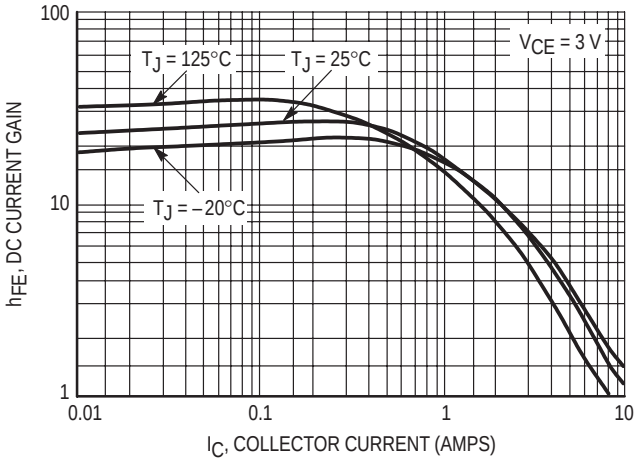


Figure 2. DC Current Gain @ 3 Volts

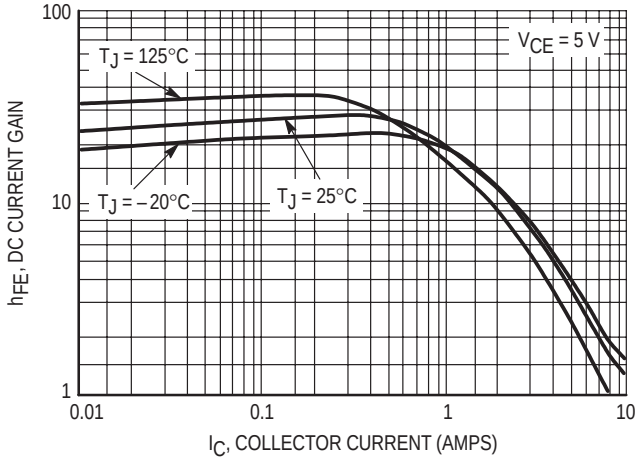


Figure 3. DC Current Gain @ 5 Volts

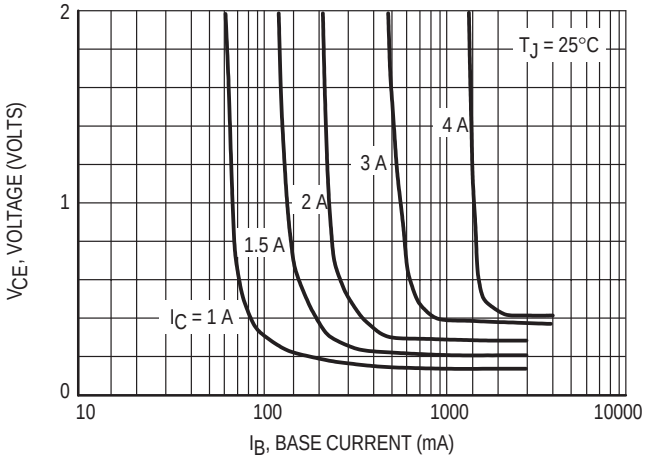


Figure 4. Collector Saturation Region

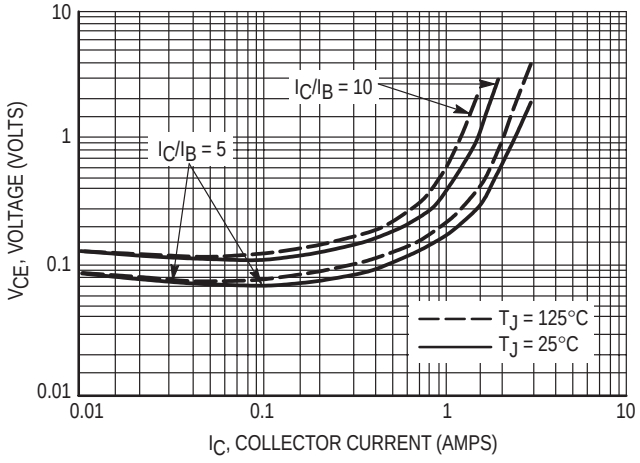


Figure 5. Collector–Emitter Saturation Voltage

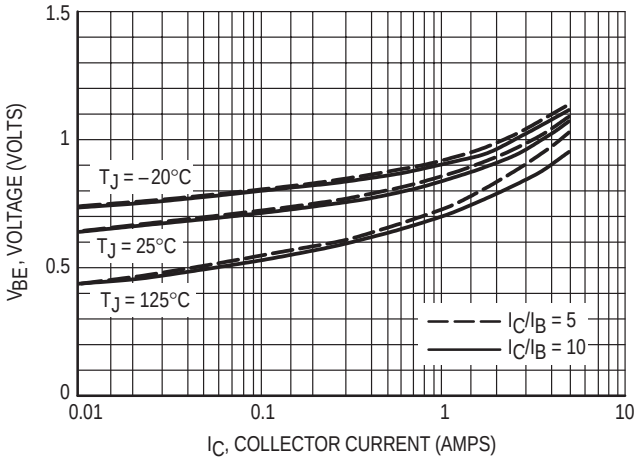


Figure 6. Base–Emitter Saturation Region

TYPICAL STATIC CHARACTERISTICS

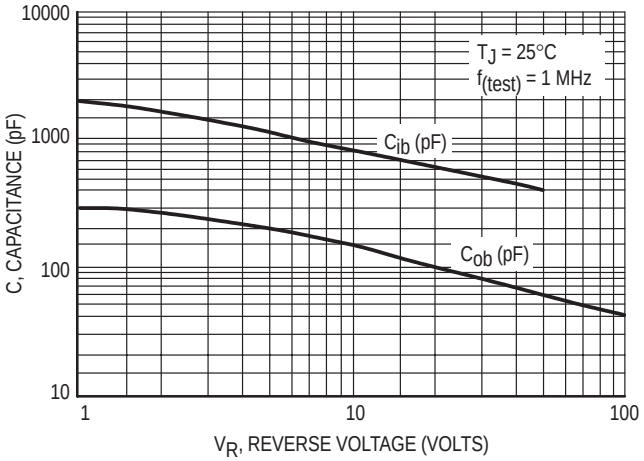


Figure 7. Capacitance

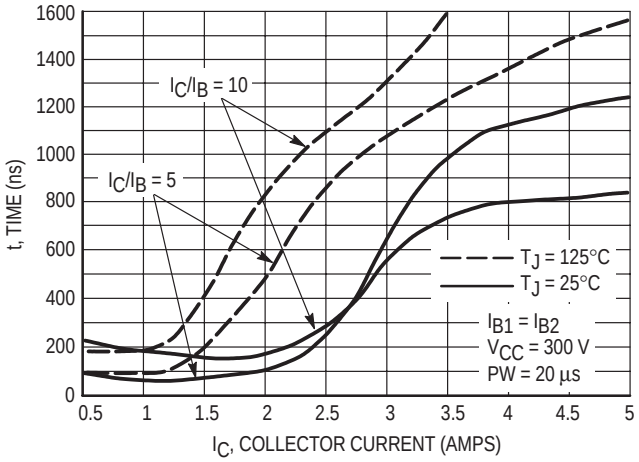


Figure 8. Resistive Switching, t_{on}

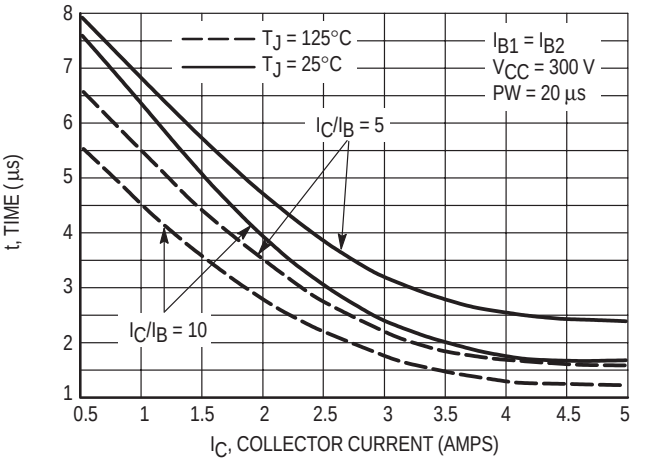


Figure 9. Resistive Switching, t_{off}

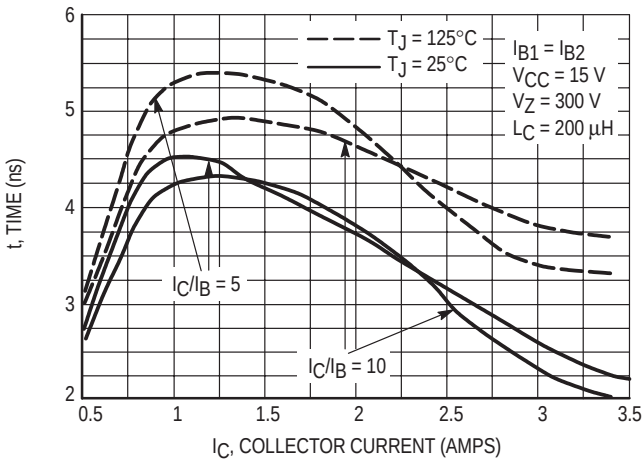


Figure 10. Inductive Storage Time, t_{si}

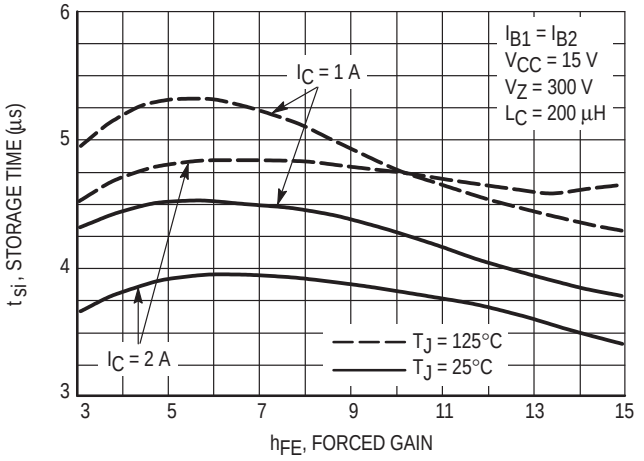


Figure 11. Inductive Storage Time, t_{si} (h_{FE})

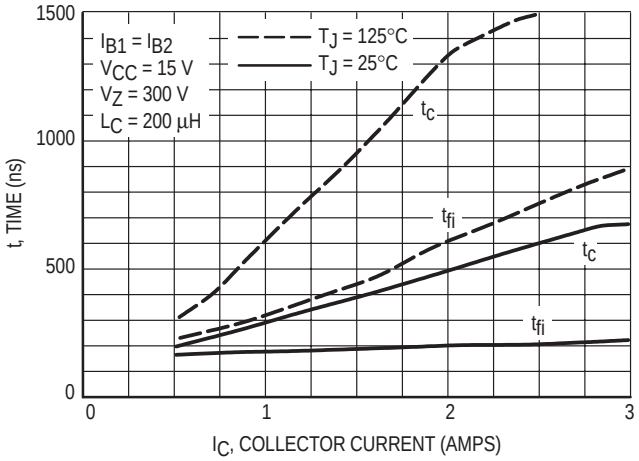


Figure 12. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 5

TYPICAL STATIC CHARACTERISTICS

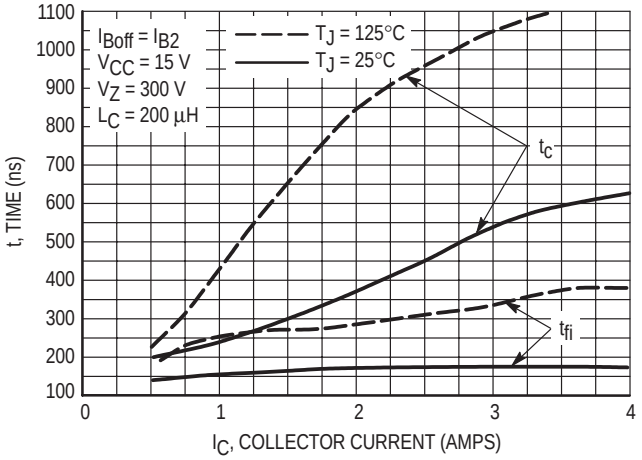


Figure 13. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 10

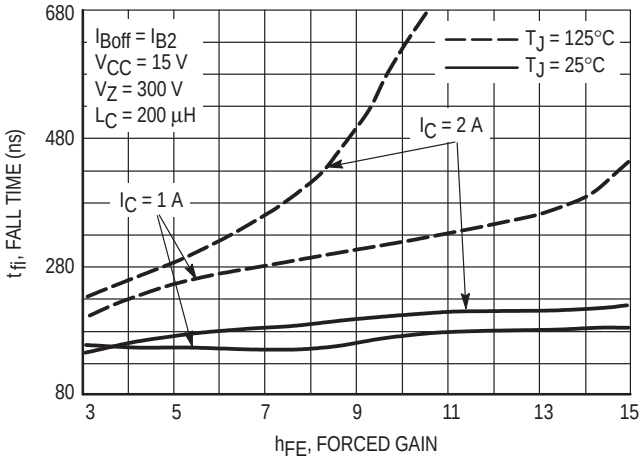


Figure 14. Inductive Fall Time

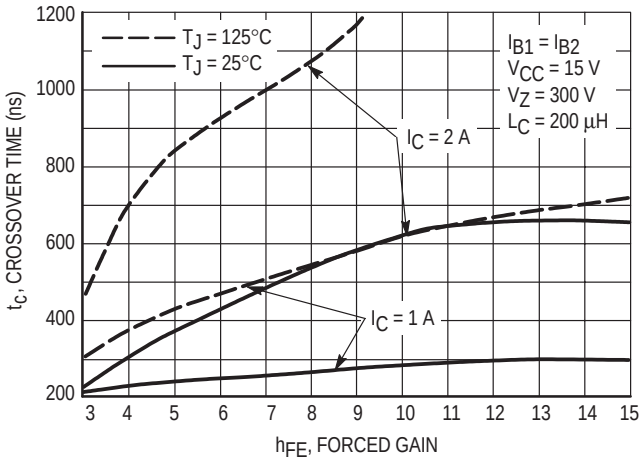


Figure 15. Inductive Crossover Time

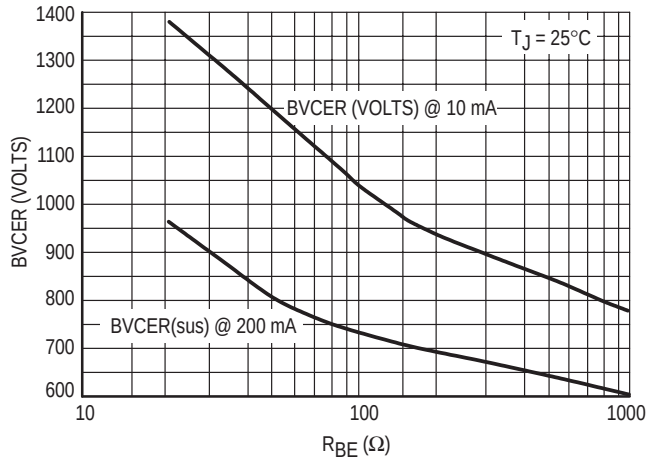


Figure 16. BVCER = f (R_{BE})

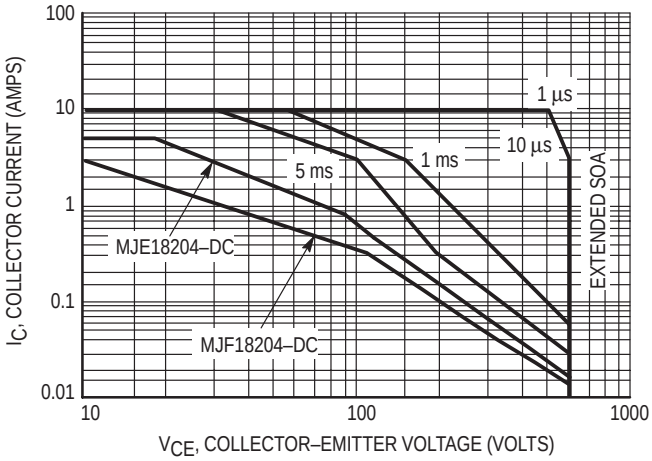


Figure 17. Forward Bias Safe Operating Area

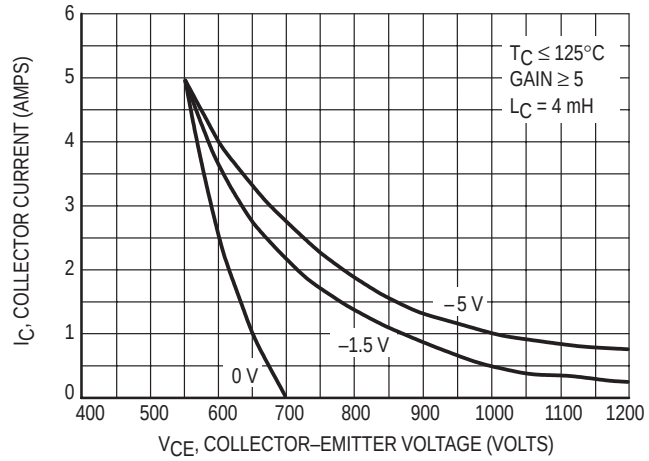


Figure 18. Reverse Bias Switching Safe Operating Area

TYPICAL STATIC CHARACTERISTICS

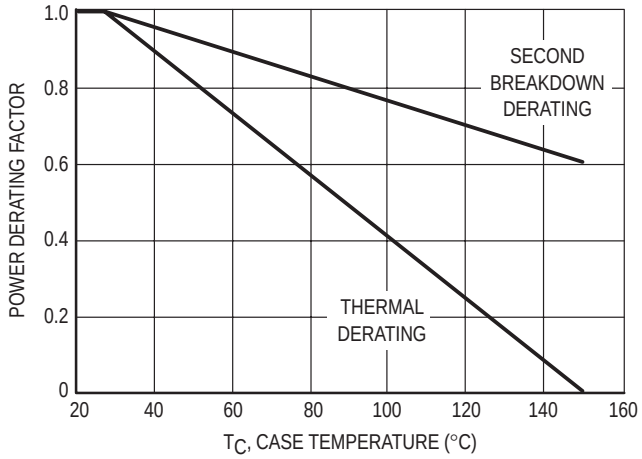


Figure 19. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 19 is based on T_C = 25°C; T_J(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 16 may be found at any case temperature by using the appropriate curve on Figure 18.

T_J(pk) may be calculated from the data in Figures 21 and 22. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse biased. The safe level is specified as a reverse–biased safe operating area (Figure 17). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL SWITCHING CHARACTERISTICS
(I_{B1} = I_{B2} FOR ALL CURVES)

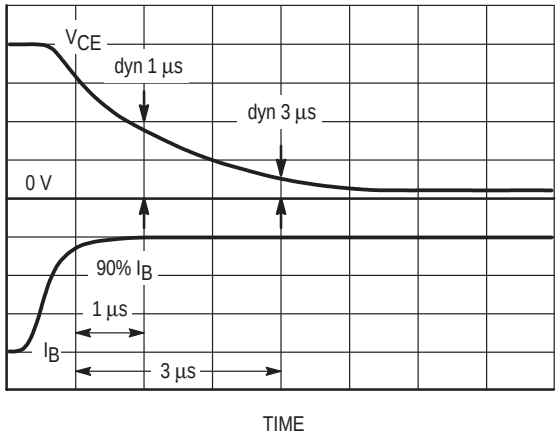


Figure 20. Dynamic Saturation Voltage Measurements

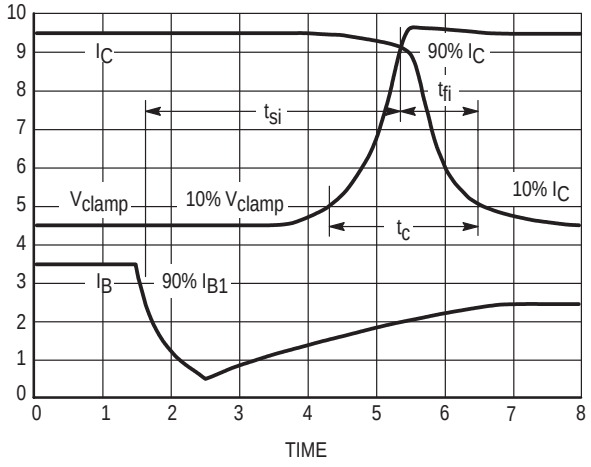
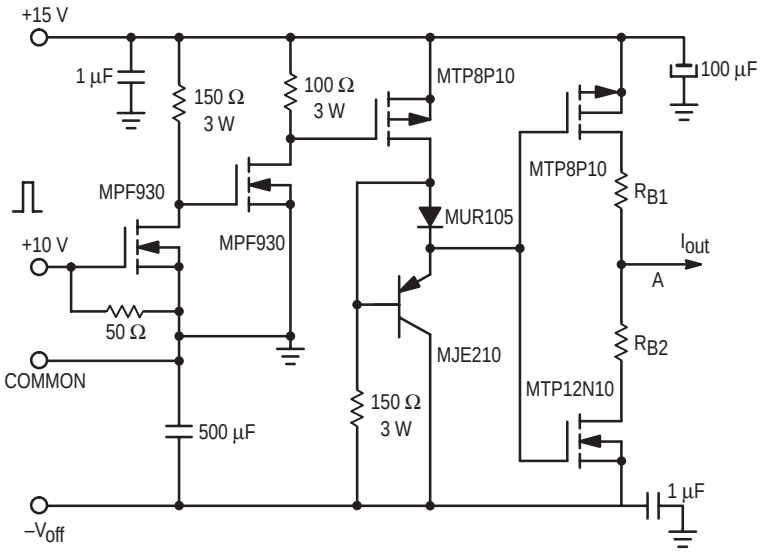
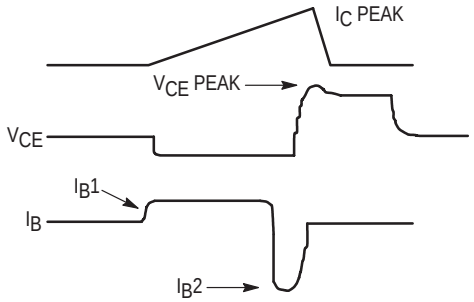


Figure 21. Inductive Switching Measurements

TYPICAL SWITCHING CHARACTERISTICS
(I_{B1} = I_{B2} FOR ALL CURVES)

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 µH	L = 500 µH
R_{B2} = ∞	R_{B2} = 0	R_{B2} = 0
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL THERMAL RESPONSE
(I_{B1} = I_{B2} FOR ALL CURVES)

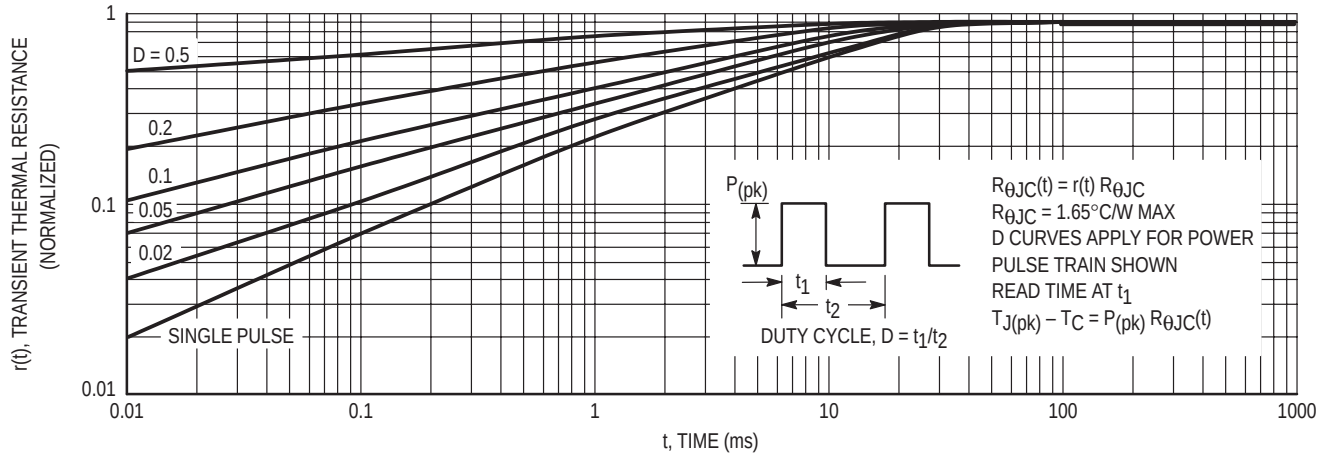


Figure 22. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJE18204

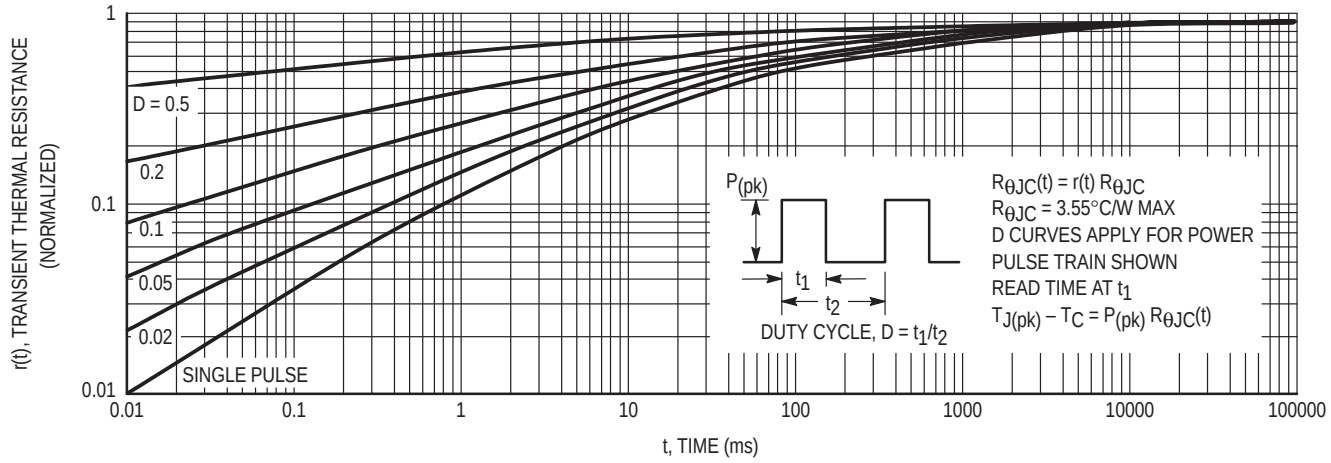


Figure 23. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJF18204

TEST CONDITIONS FOR ISOLATION TESTS*

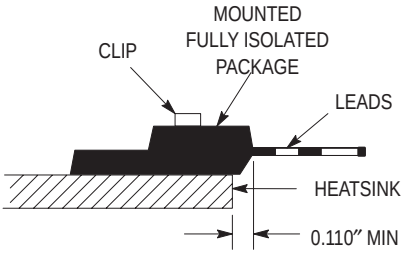


Figure 24. Screw or Clip Mounting Position for Isolation Test Number 1

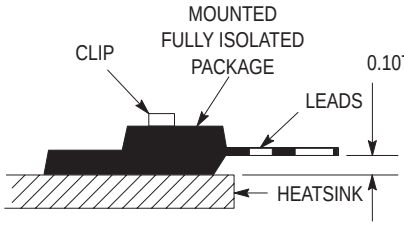


Figure 25. Clip Mounting Position for Isolation Test Number 2

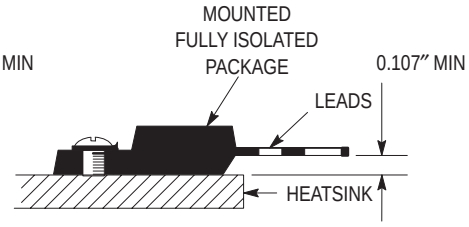


Figure 26. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION**

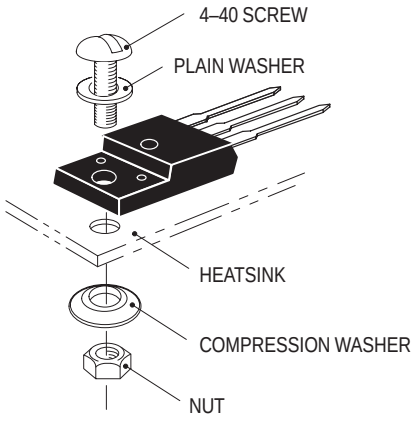


Figure 27a. Screw–Mounted

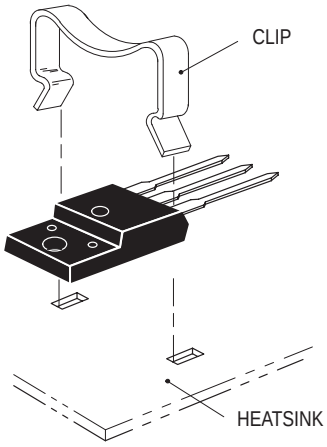


Figure 27b. Clip–Mounted

Figure 27. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

MJE18206
MJF18206

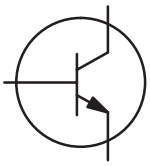
POWER TRANSISTORS
8 AMPERES
1200 VOLTS
40 and 100 WATTS

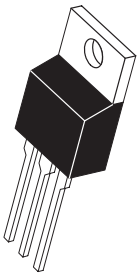
Designer's™ Data Sheet

SWITCHMODE™ NPN Bipolar Power Transistor for Electronic Light Ballast and Switching Power Supply Applications

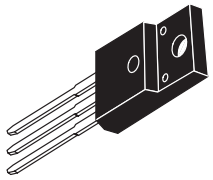
The MJE/MJF18206 have an application specific state–of–the–art die dedicated to the electronic ballast ("light ballast") and power supply applications.

- Improved Global Efficiency Due to Low Base Drive Requirements:
  - — High and Flat DC Current Gain h_{FE}
  - — Fast Switching
  - — No Coil Required in Base Circuit for fast Turn–Off (No Current Tail)
- Full Characterization at 125°C
- Motorola "6 SIGMA" Philosophy Provides Tight and Reproducible Parametric Distributions
- Two Package Choices: Standard TO–220 or Isolated TO–220





CASE 221A–06
TO–220AB



CASE 221D–02
TO–220 FULLPACK

MAXIMUM RATINGS

Rating	Symbol	MJE18206	MJF18206	Unit
Collector–Emitter Voltage	V_{CEO}	600		Vdc
Collector–Base Voltage	V_{CBO}	1200		Vdc
Collector–Emitter Voltage	V_{CES}	1200		Vdc
Emitter–Base Voltage	V_{EBO}	10		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8 16		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	5 9		Adc
RMS Isolation Voltage (2) Per Figure 22 (for 1 sec, R.H. ≤ 30%) Per Figure 23 T_C = 25°C Per Figure 24	V_{ISOL1} V_{ISOL2} V_{ISOL3}		4500 3500 1500	Volts
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	100 0.8	40 0.32	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	MJE18206	MJF18206	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.25 62.5	3.125 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	260		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH) (I_C = 200 mA, L = 25 mH, R = 200 Ω)			$V_{CEO(sus)}$ $V_{CER(sus)}$	 550 600	 630 700		Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA, I_E = 0)			V_{CBO}	1200	1320		Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA, I_C = 0)			V_{EBO}	10	12.9		Vdc
Collector Cutoff Current (V_{CE} = 550 V, I_B = 0) (V_{CE} = 550 V, I_B = 0)	@ T_C = 25°C @ T_C = 125°C		I_{CEO}			200 2000	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{BE} = 0) (V_{CE} = 1000 V, V_{BE} = 0)	@ T_C = 25°C @ T_C = 125°C @ T_C = 125°C		I_{CES}			100 1000 100	μAdc
Collector Cutoff Current (V_{CB} = 1200 V, I_E = 0)			I_{CBO}			100	μAdc
Emitter–Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)			I_{EBO}			100	μAdc
ON CHARACTERISTICS							
Base–Emitter Saturation Voltage (I_C = 1.3 Adc, I_B = 0.13 Adc) (I_C = 2 Adc, I_B = 0.4 Adc) (I_C = 3 Adc, I_B = 0.6 Adc)	 @ T_C = 25°C @ T_C = 125°C @ T_C = 25°C @ T_C = 125°C @ T_C = 25°C @ T_C = 125°C		$V_{BE(sat)}$	 	 0.77 0.67 0.85 0.75 0.91 0.8	 1 0.9 1.1 1 1.1 1	Vdc
Collector–Emitter Saturation Voltage (I_C = 1.3 Adc, I_B = 0.13 Adc) (I_C = 3 Adc, I_B = 0.6 Adc)	 @ T_C = 25°C @ T_C = 125°C @ T_C = 25°C @ T_C = 125°C		$V_{CE(sat)}$	 	 0.3 0.4 0.4 0.8	 0.75 1 0.75 1.25	Vdc
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 5 Vdc) (I_C = 1 Adc, V_{CE} = 5 Vdc) (I_C = 3 Adc, V_{CE} = 1 Vdc) (I_C = 10 mAdc, V_{CE} = 5 Vdc)	 @ T_C = 25°C @ T_C = 125°C @ T_C = 25°C @ T_C = 125°C @ T_C = 25°C @ T_C = 125°C @ T_C = 25°C @ T_C = 125°C		h_{FE}	 18 5 4 11 	 25 25 20 8 6 33	 45 50 	— — —
DYNAMIC CHARACTERISTICS							
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)			f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)			C_{ob}			200	pF
Input Capacitance (V_{EB} = 8 Vdc)			C_{ib}			2000	pF
DYNAMIC SATURATION VOLTAGE							
Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 1.3 Adc I_{B1} = 130 mAdc V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C	$V_{CE(dsat)}$		7.5		V
		@ 3 μs	@ T_C = 25°C			4.5		
	I_C = 3 Adc I_{B1} = 0.6 Adc V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C			14.5		
		@ 3 μs	@ T_C = 25°C			6		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Turn–on Time	I_C = 3 Adc, I_{B1} = 0.6 Adc I_{B2} = 1.5 Adc V_{CC} = 300 Vdc	@ T_C = 25°C	t_{on}		200	350	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		2 2.5	2.5	μs
Turn–on Time	I_C = 3 Adc, I_{B1} = 0.6 Adc I_{B2} = 0.6 Adc V_{CC} = 300 Vdc	@ T_C = 25°C	t_{on}		190	250	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		3.7 4.5	4.5	μs
Turn–on Time	I_C = 1 Adc, I_{B1} = 70 mAdc I_{B2} = 1 Adc V_{CC} = 125 Vdc PW = 70 μs	@ T_C = 25°C	t_d		125	300	ns
			t_r		400	750	ns
Turn–off Time		@ T_C = 25°C	t_s		600	1.2	μs
			t_f		450	700	ns
Turn–on Time	I_C = 1 Adc, I_{B1} = 100 mAdc I_{B2} = 500 mAdc V_{CC} = 300 Vdc	@ T_C = 25°C @ T_C = 125°C	t_{on}		250 225	350	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		2 2.5	2.75	μs
SWITCHING CHARACTERISTICS: Inductive Load (V_{clamp} = 300 V, V_{CC} = 15 V, L = 200 μH)							
Fall Time	I_C = 1.3 Adc I_{B1} = 0.13 Adc I_{B2} = 0.65 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		150 225	200	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		1.6 1.9	2	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		260 300	350	ns
Fall Time	I_C = 3 Adc I_{B1} = 0.6 Adc I_{B2} = 1.5 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		300 400	450	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		2.25 2.5	2.75	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		500 700	800	ns
Fall Time	I_C = 3 Adc I_{B1} = 0.6 Adc I_{B2} = 0.6 Adc	@ T_C = 25°C @ T_C = 125°C	t_f		350 500	500	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		4.25 5.1	5	μs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		600 1100	800	ns

TYPICAL STATIC CHARACTERISTICS

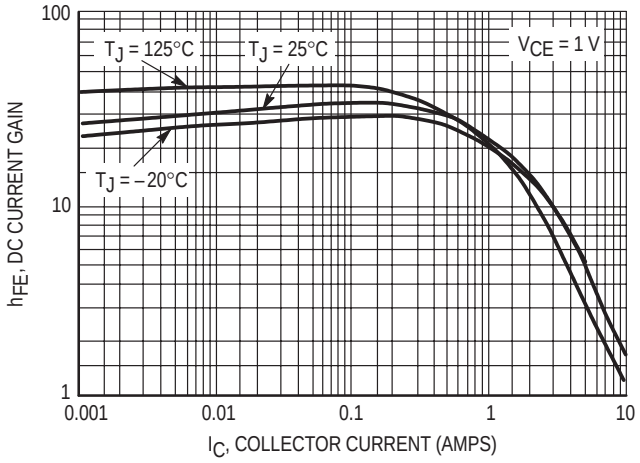


Figure 1. DC Current Gain @ 1 Volt

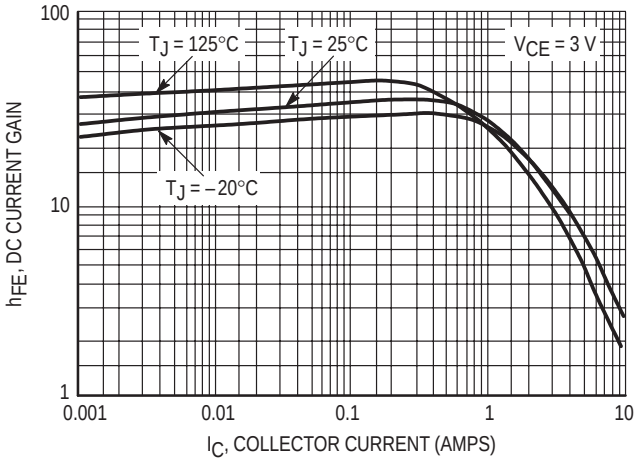


Figure 2. DC Current Gain @ 3 Volts

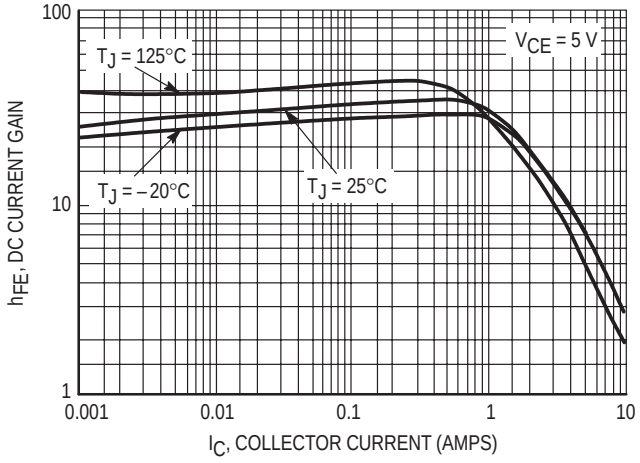


Figure 3. DC Current Gain @ 5 Volts

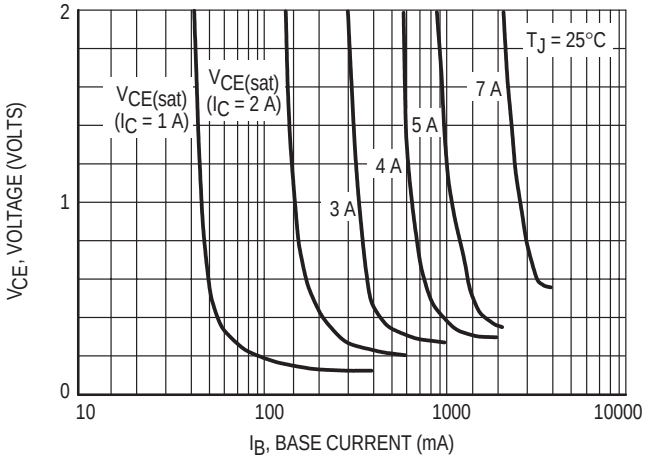


Figure 4. Collector Saturation Region

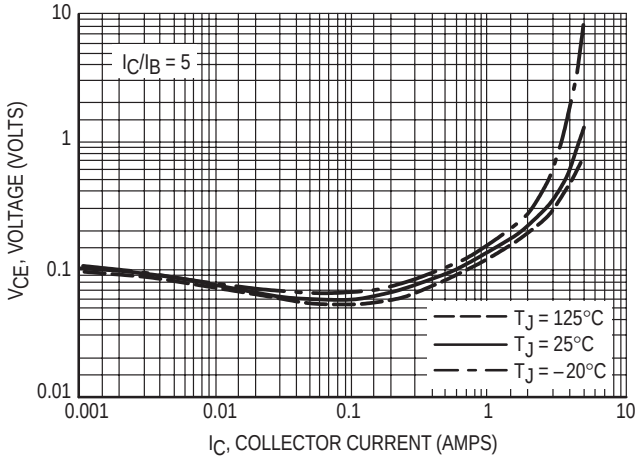


Figure 5A. Collector–Emitter Saturation Voltage

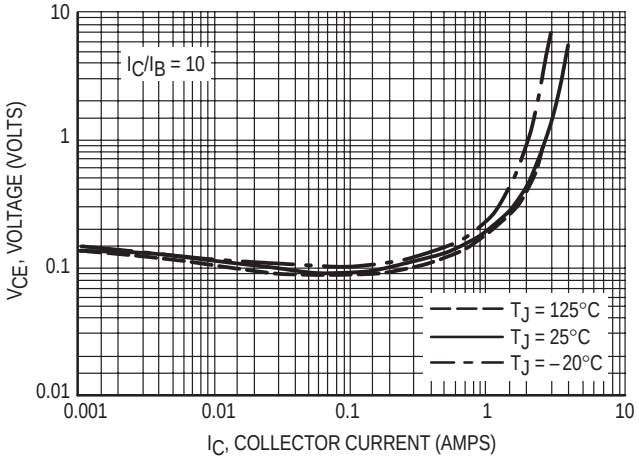


Figure 5B. Collector–Emitter Saturation Voltage

TYPICAL STATIC CHARACTERISTICS

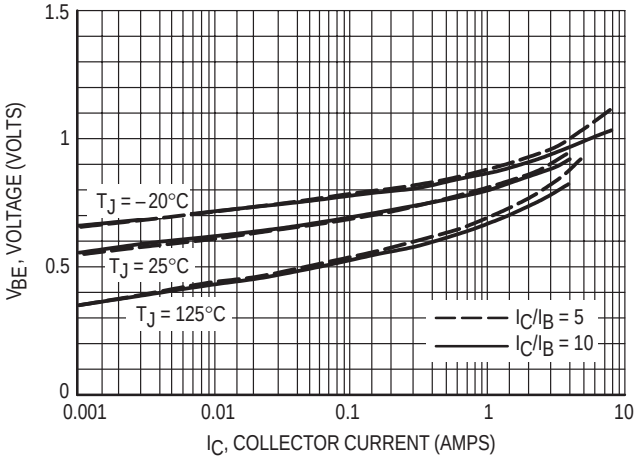


Figure 6. Base–Emitter Saturation Region

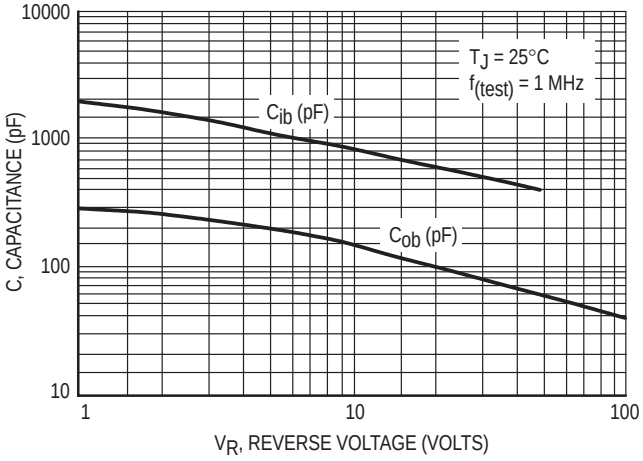


Figure 7. Capacitance

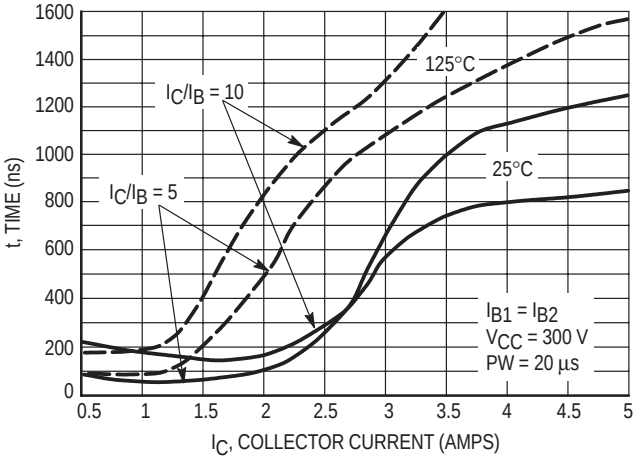


Figure 8. Resistive Switching, t_{on}

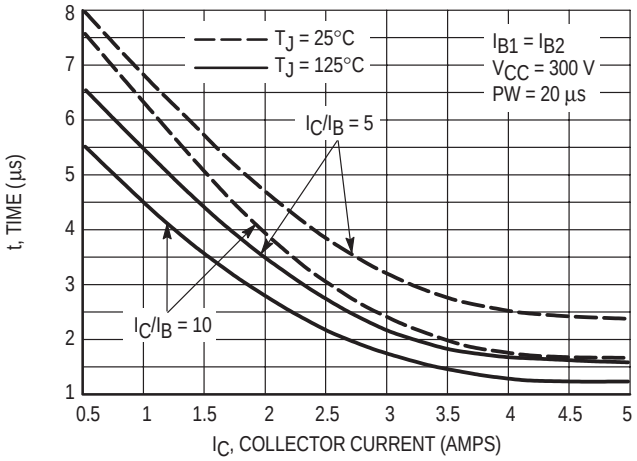


Figure 9. Resistive Switching, t_{off}

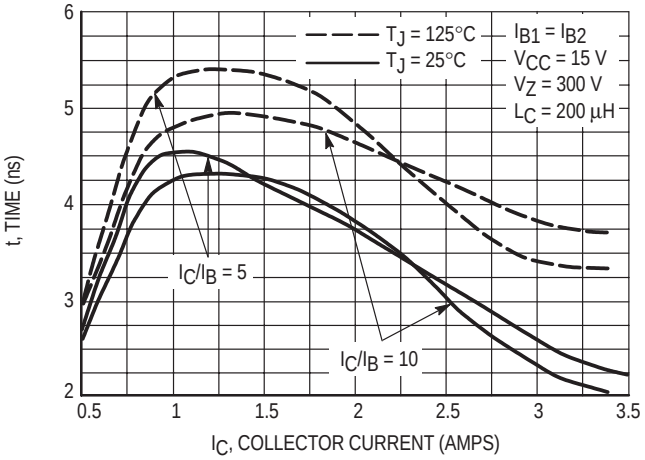


Figure 10. Inductive Storage Time, t_{si}

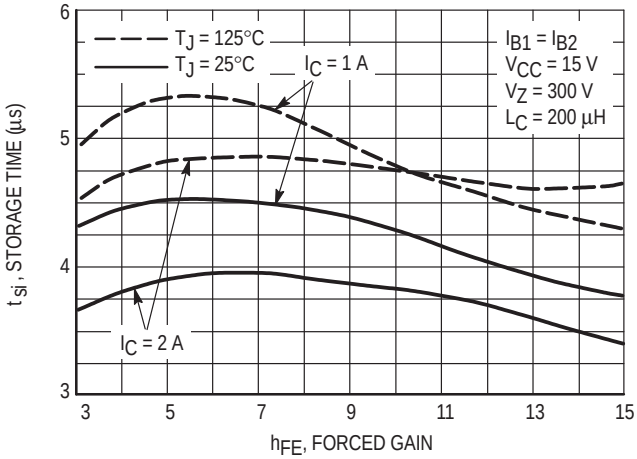


Figure 11. Inductive Storage Time

TYPICAL STATIC CHARACTERISTICS

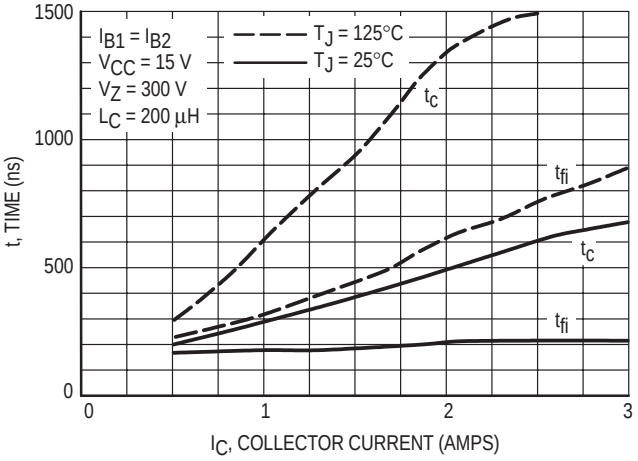


Figure 12. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 5

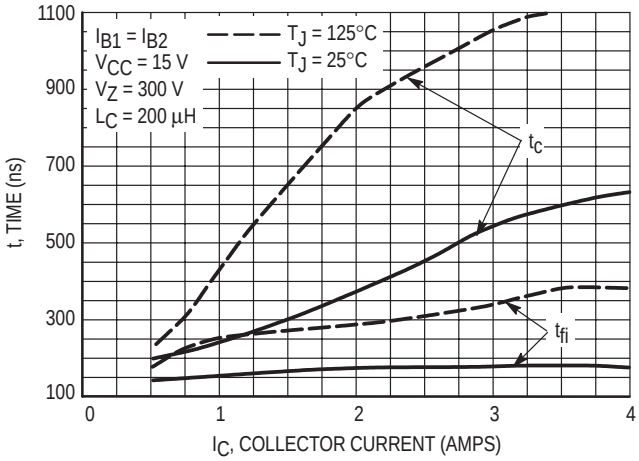


Figure 13. Inductive Switching, t_c & t_{fi} @ I_C/I_B = 10

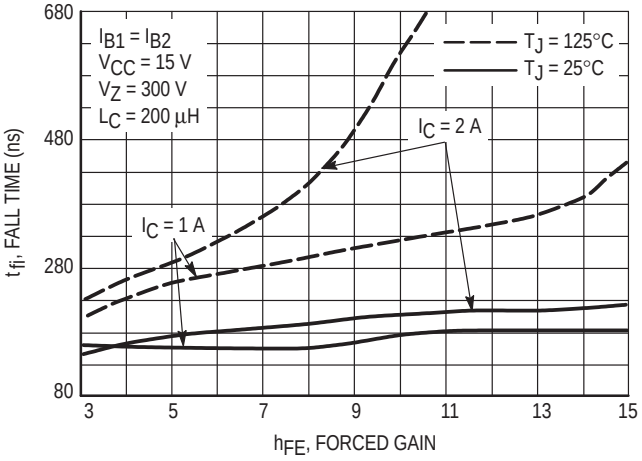


Figure 14. Inductive Fall Time

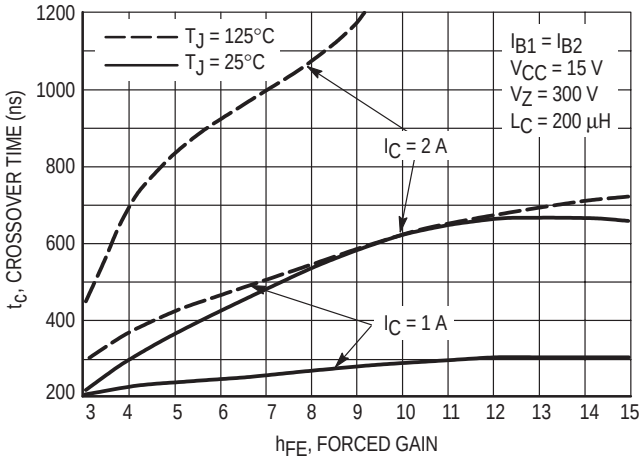


Figure 15. Inductive Crossover Time

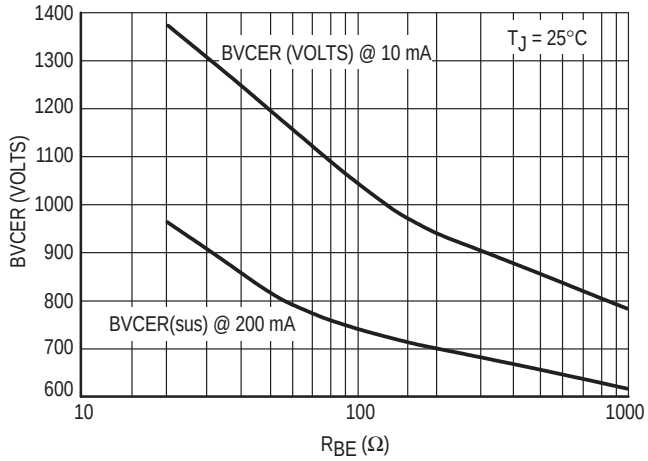


Figure 16. BVCER = f (R_{BE})

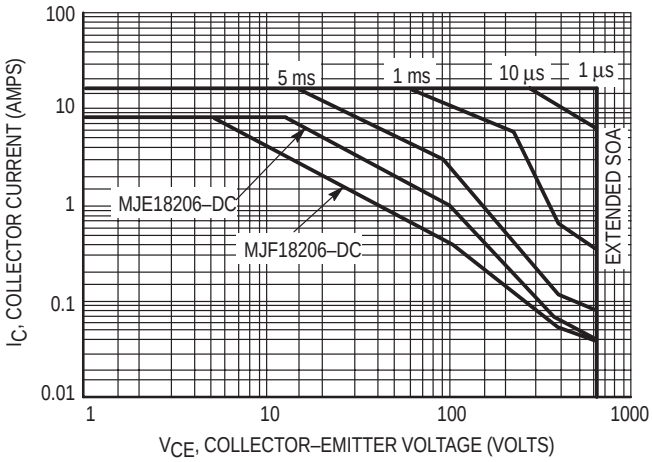


Figure 17. Forward Bias Safe Operating Area

TYPICAL STATIC CHARACTERISTICS

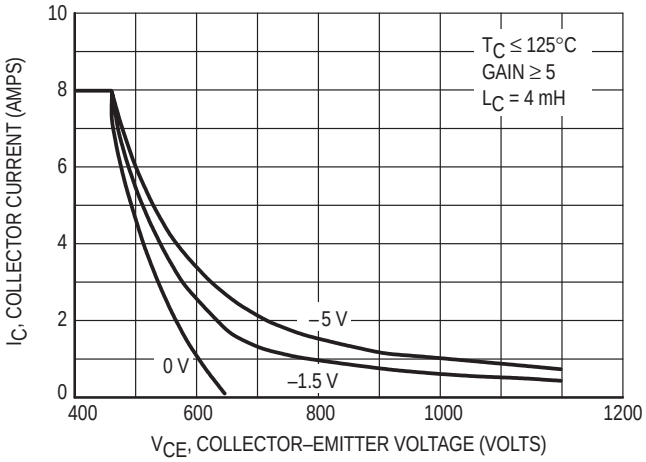


Figure 18. Reverse Bias Switching Safe Operating Area

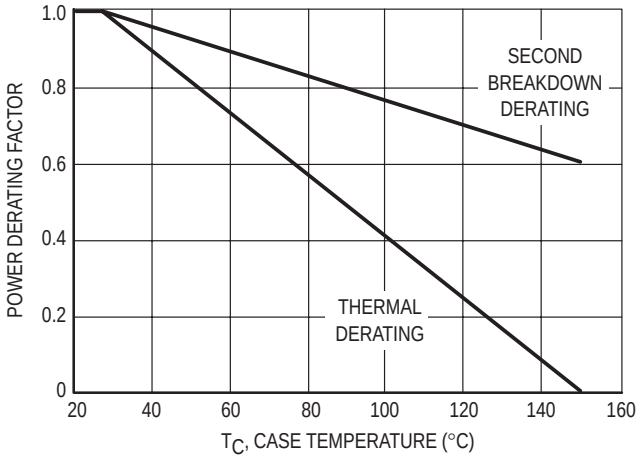


Figure 19. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 17 is based on T_C = 25°C; T_J(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when T_C > 25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 17 may be found at any case temperature by using the appropriate curve on Figure 19.

T_J(pk) may be calculated from the data in Figures 22 and 23. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn–off with the base–to–emitter junction reverse biased. The safe level is specified as a reverse–biased safe operating area (Figure 18). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

TYPICAL SWITCHING CHARACTERISTICS (I_{B1} = I_{B2} FOR ALL CURVES)

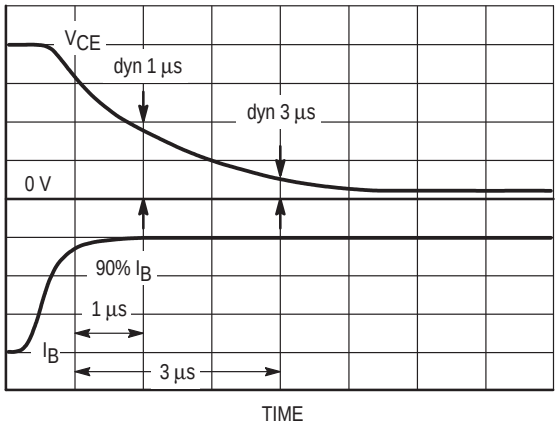


Figure 20. Dynamic Saturation Voltage Measurements

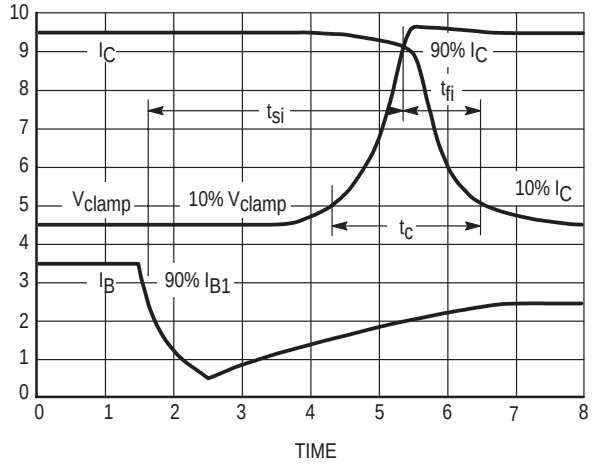
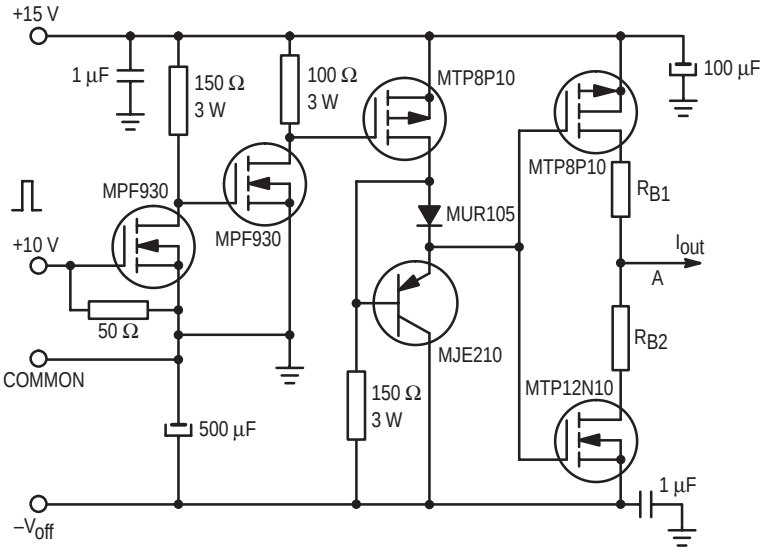
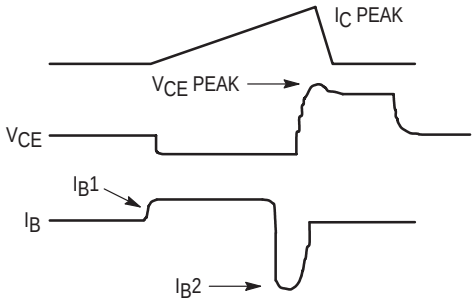


Figure 21. Inductive Switching Measurements

TYPICAL SWITCHING CHARACTERISTICS
($I_{B1} = I_{B2}$ FOR ALL CURVES)

Table 1. Inductive Load Switching Drive Circuit





$V_{(BR)CEO(sus)}$	Inductive Switching	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
$R_{B2} = \infty$	$R_{B2} = 0$	$R_{B2} = 0$
V_{CC} = 20 Volts	V_{CC} = 15 Volts	V_{CC} = 15 Volts
$I_{C(pk)}$ = 100 mA	R_{B1} selected for desired I_{B1}	R_{B1} selected for desired I_{B1}

TYPICAL THERMAL RESPONSE
(I_{B1} = I_{B2} FOR ALL CURVES)

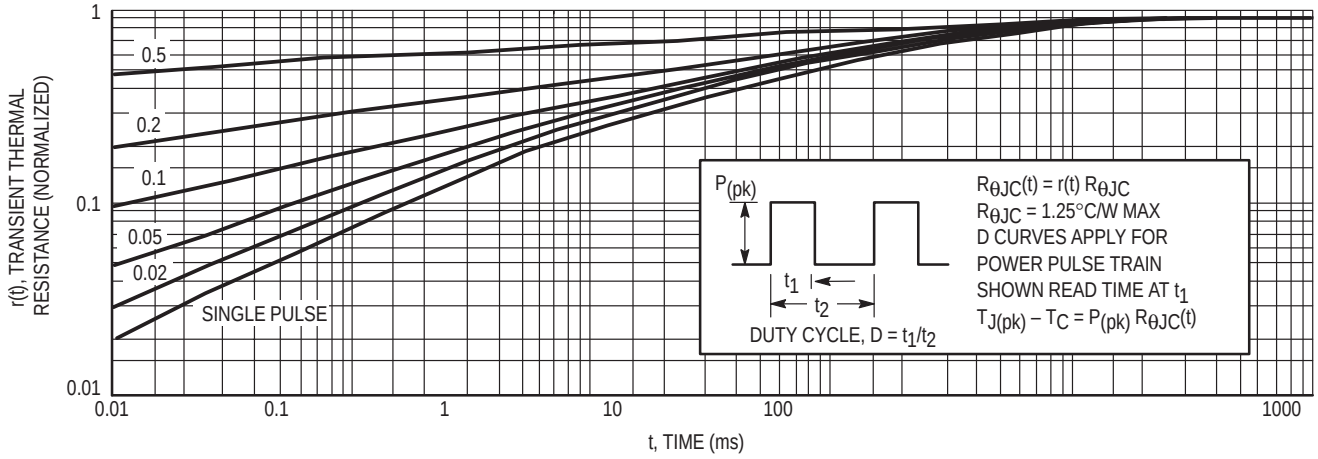


Figure 22. Typical Thermal Response ($Z_{\theta JC(t)}$) for MJE18206

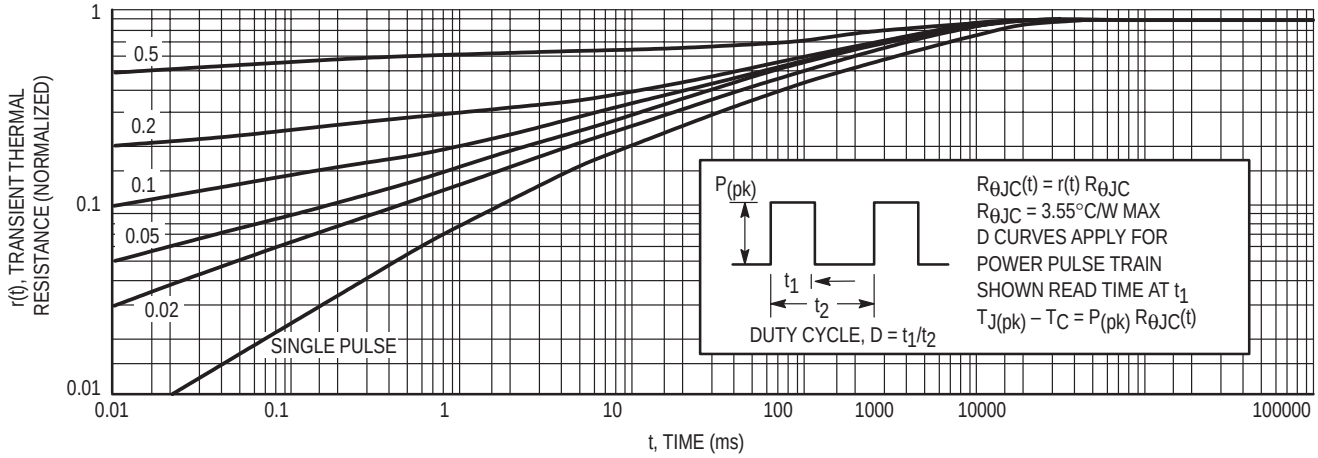


Figure 23. Typical Thermal Response ($Z_{\theta JC(t)}$) for MJF18206

TEST CONDITIONS FOR ISOLATION TESTS*

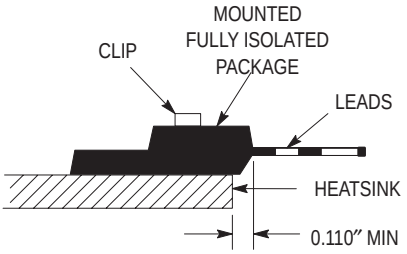


Figure 24. Clip Mounting Position for Isolation Test Number 1

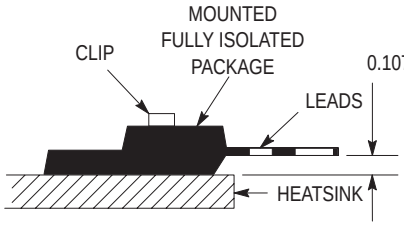


Figure 25. Clip Mounting Position for Isolation Test Number 2

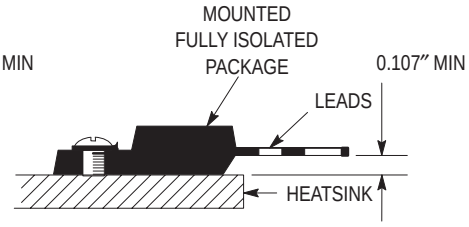


Figure 26. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION**

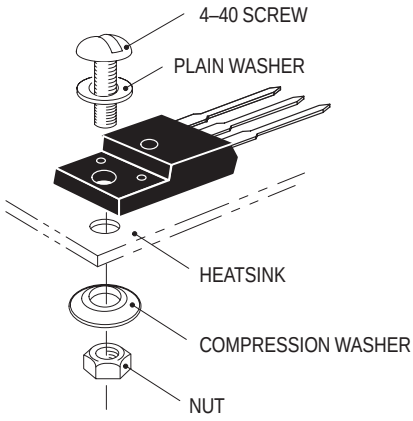


Figure 27a. Screw–Mounted

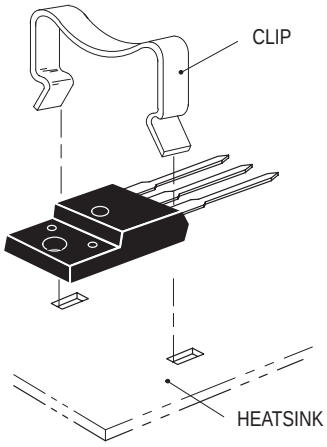


Figure 27b. Clip–Mounted

Figure 27. Typical Mounting Techniques for Isolated Package

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

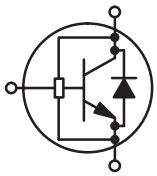
** For more information about mounting power semiconductors see Application Note AN1040.

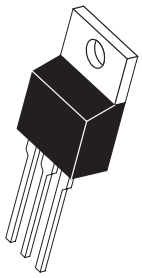
MJE18604D2

Advance Information

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector-Emitter Diode and Built-in Efficient Antisaturation Network for 1600 V Applications

POWER TRANSISTORS
3 AMPERES
1600 VOLTS
100 WATTS





CASE 221A–06
TO–220AB

The MJE18604D2 is state–of–art High Speed High gain BIPolar transistor (H2BIP). Tight dynamic characteristics and lot to lot low spread (±150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no more a need to guarantee an h_{fe} window.

Main features:

- Low Base Drive Requirement
- High DC Current Gain (30 Typical) @ I_C = 400 mA
- Extremely Low Storage Time Min/Max Guarantees Due to the Internal Active Antisaturation (H2BIP) Structure which Minimizes the Spread
- Integrated Collector–Emitter Free Wheeling Diode Matched with the Power Transistor
- Fully Characterized and Guaranteed Dynamic $V_{CE(sat)}$
- "6 Sigma" Process Providing Tight and Reproductible Parameter Spreads

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Breakdown Voltage	V_{CEO}	800	Vdc
Collector–Emitter Sustaining Voltage @ R = 200 Ω	V_{CER}	800	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	1600	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1600	Vdc
Emitter–Base Voltage	V_{EBO}	12	Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	3 8	Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4	Adc
*Total Device Dissipation @ T_C = 25°C *Derate above 25°C	P_D	100 0.8	Watt W/°C
Operating and Storage Temperature	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.25 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8″ from case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector–Emitter Sustaining Voltage (I_C = 100 mA, L = 25 mH, R_{BE} = 200 Ω)			$V_{CER(sus)}$	800			Vdc
Collector–Base Breakdown Voltage (I_{CBO} = 1 mA)			V_{CBO}	1600			Vdc
Emitter–Base Breakdown Voltage (I_{EBO} = 1 mA)			V_{EBO}	12	14		Vdc
Collector Cutoff Current (V_{CBO} = Rated V_{CBO}, I_B = 0)			I_{CBO}			100	μAdc
Collector Cutoff Current (V_{CE} = Rated V_{CES}, V_{EB} = 0)		@ T_C = 25°C	I_{CES}			100	μAdc
		@ T_C = 125°C				1000	
(V_{CE} = 1300 V, V_{EB} = 0)		@ T_C = 125°C				100	
Emitter–Cutoff Current (V_{EB} = 11 Vdc, I_C = 0)			I_{EBO}			500	μAdc
ON CHARACTERISTICS							
Base–Emitter Saturation Voltage			$V_{BE(sat)}$				Vdc
(I_C = 0.5 Adc, I_B = 0.1 Adc)		@ T_C = 25°C			0.8	1.1	
		@ T_C = 125°C			0.6	1	
(I_C = 1 Adc, I_B = 0.1 Adc)		@ T_C = 25°C			0.8	1	
		@ T_C = 125°C				1	
(I_C = 2 Adc, I_B = 0.4 Adc)		@ T_C = 25°C			0.9	1.2	
		@ T_C = 125°C			0.8	1.1	
Collector–Emitter Saturation Voltage			$V_{CE(sat)}$				Vdc
(I_C = 250 mAdc, I_B = 25 mAdc)		@ T_C = 25°C			1	1.25	
		@ T_C = 125°C			1.7		
(I_C = 0.5 Adc, I_B = 50 mAdc)		@ T_C = 25°C			2.1	2.4	
		@ T_C = 125°C			4		
(I_C = 0.8 Adc, I_B = 80 mAdc)		@ T_C = 25°C			3.7	5	
		@ T_C = 125°C					
DC Current Gain			h_{FE}				—
(I_C = 0.4 Adc, V_{CE} = 3 Vdc)		@ T_C = 25°C		20		40	
		@ T_C = 125°C		6	10		
(I_C = 5 mAdc, V_{CE} = 10 Vdc)		@ T_C = 25°C		20	35		
		@ T_C = 125°C		20	55		
DYNAMIC SATURATION VOLTAGE							
Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	I_C = 0.3 Adc, I_{B1} = 50 mA, V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C	$V_{CE(dsat)}$		4.7		V
			@ T_C = 125°C			9.3		
		@ 3 μs	@ T_C = 25°C			2.6		
			@ T_C = 125°C			5.4		
	I_C = 0.5 Adc, I_{B1} = 50 mA, V_{CC} = 300 V	@ 1 μs	@ T_C = 25°C			9.7		
			@ T_C = 125°C			18		
		@ 3 μs	@ T_C = 25°C			6.4		
			@ T_C = 125°C			12.3		
DIODE CHARACTERISTICS							
Forward Diode Voltage			V_{EC}				V
(I_{EC} = 0.4 Adc)		@ T_C = 25°C			0.9	1.2	
		@ T_C = 125°C			0.6		
(I_{EC} = 1 Adc)		@ T_C = 25°C			1.05	1.5	
		@ T_C = 125°C			0.7		
Forward Recovery Time			t_{fr}				μs
(I_F = 0.4 Adc, di/dt = 10 A/μs)		@ T_C = 25°C			0.9		
		@ T_C = 125°C			1.5		
(I_F = 1.0 Adc, di/dt = 10 A/μs)		@ T_C = 25°C			1.15		
		@ T_C = 125°C			1.6		

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS							
Current Gain Bandwidth (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1 MHz)			f_T		13		MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)			C_{ob}		230	500	pF
Input Capacitance (V_{CE} = 8 Vdc)			C_{ib}		480	1000	pF
SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)							
Delay Time	I_C = 0.5 Adc I_{B1} = 66 mAdc I_{B2} = 390 mAdc V_{CC} = 125 V	@ T_C = 25°C @ T_C = 125°C	t_d		95 110	150	ns
Rise Time		@ T_C = 25°C @ T_C = 125°C	t_r		475 900	750	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	400	 910	700	ns
Fall Time		@ T_C = 25°C @ T_C = 125°C	t_f		675 775	850	ns
Turn–on Time	I_C = 0.3 Adc I_{B1} = 50 mAdc I_{B2} = 50 mAdc V_{CC} = 125 V	@ T_C = 25°C @ T_C = 125°C	t_{on}		440 570		ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		4 5.9		μs
Fall Time		@ T_C = 25°C @ T_C = 125°C	t_f		375 675		ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		4.5 6.6		μs
Turn–on Time	I_C = 0.3 Adc I_{B1} = 50 mAdc I_{B2} = 150 mAdc V_{CC} = 125 V	@ T_C = 25°C @ T_C = 125°C	t_{on}		465 550	600	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	500	 1800	800	ns
Fall Time		@ T_C = 25°C @ T_C = 125°C	t_f		800 550	1000	ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		1.5 2.4	1.75	μs
Turn–on Time	I_C = 0.5 Adc I_{B1} = 50 mAdc I_{B2} = 50 mAdc V_{CC} = 125 V	@ T_C = 25°C @ T_C = 125°C	t_{on}		550 1300		ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		4.35 5		μs
Fall Time		@ T_C = 25°C @ T_C = 125°C	t_f		500 2000		ns
Turn–off Time		@ T_C = 25°C @ T_C = 125°C	t_{off}		4.8 7		μs
Delay Time	I_C = 0.5 Adc I_{B1} = 50 mAdc I_{B2} = 250 mAdc V_{CC} = 125 V	@ T_C = 25°C	t_d		100	300	ns
Rise Time		@ T_C = 25°C	t_r		300	800	ns
Storage Time		@ T_C = 25°C	t_s		1	1.2	μs
Fall Time		@ T_C = 25°C	t_f		200	350	ns

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS: Inductive Load (V_{CC} = 15 V)							
Fall Time	I_C = 300 mAdc I_{B1} = 50 mAdc I_{B2} = 50 mAdc V_Z = 300 V L_C = 200 µH	@ T_C = 25°C @ T_C = 125°C	t_f		170 210		ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		1.7 2.7		µs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		150 400		ns
Fall Time	I_C = 300 mAdc I_{B1} = 50 mAdc I_{B2} = 150 mAdc V_Z = 300 V L_C = 200 µH	@ T_C = 25°C @ T_C = 125°C	t_f		160 150	250	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	0.7	 1.1	1	µs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		160 160	250	ns
Fall Time	I_C = 500 mAdc I_{B1} = 50 mAdc I_{B2} = 50 mAdc V_Z = 300 V L_C = 200 µH	@ T_C = 25°C @ T_C = 125°C	t_f		165 700		ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s		3 4.1		µs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		200 800		ns
Fall Time	I_C = 500 mAdc I_{B1} = 50 mAdc I_{B2} = 250 mAdc V_Z = 300 V L_C = 200 µH	@ T_C = 25°C @ T_C = 125°C	t_f		110 130	175	ns
Storage Time		@ T_C = 25°C @ T_C = 125°C	t_s	0.7	 1.8	1	µs
Crossover Time		@ T_C = 25°C @ T_C = 125°C	t_c		130 250	200	ns

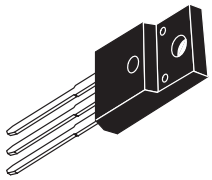
MJF47

High Voltage Power Transistor
Isolated Package Applications

Designed for line operated audio output amplifiers, switching power supply drivers and other switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Electrically Similar to the Popular TIP47
- 250 $V_{CEO(sus)}$
- 1 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation

NPN SILICON
POWER TRANSISTOR
1 AMPERE
250 VOLTS
28 WATTS



CASE 221D–02
TO–220 TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CB}	350	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T_A = 25°C) Test No. 1 Per Fig. 10 / Test No. 2 Per Fig. 11 / Test No. 3 Per Fig. 12	V_{ISOL}	4500 / 3500 / 1500	V_{RMS}
Collector Current — Continuous / Peak	I_C	1 / 2	Adc
Base Current	I_B	0.6	Adc
Total Power Dissipation* @ T_C = 25°C / Derate above 25°C	P_D	28 / 0.23	Watts / W/°C
Total Power Dissipation @ T_A = 25°C / Derate above 25°C	P_D	2 / 0.016	Watts / W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	4.4	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

* Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.

(1) Proper strike and creepage distance must be provided.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	—	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0)	I_{CEO}	—	0.2	mAdc
Collector Cutoff Current (V_{CE} = 350 Vdc, V_{BE} = 0)	I_{CES}	—	0.1	mAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	1	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 10 Vdc) (I_C = 1 Adc, V_{CE} = 10 Vdc)	h_{FE}	30 10	150 —	—
Collector–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.2 Adc)	$V_{CE(sat)}$	—	1	Vdc
Base–Emitter On Voltage (I_C = 1 Adc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 0.2 Adc, V_{CE} 10 Vdc, f = 2 MHz)	f_T	10	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

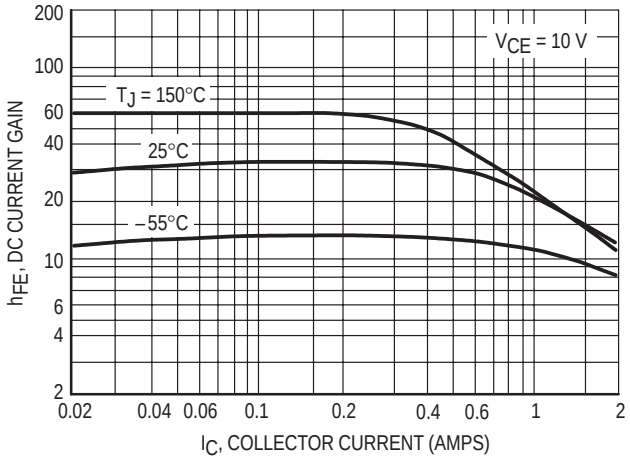


Figure 1. DC Current Gain

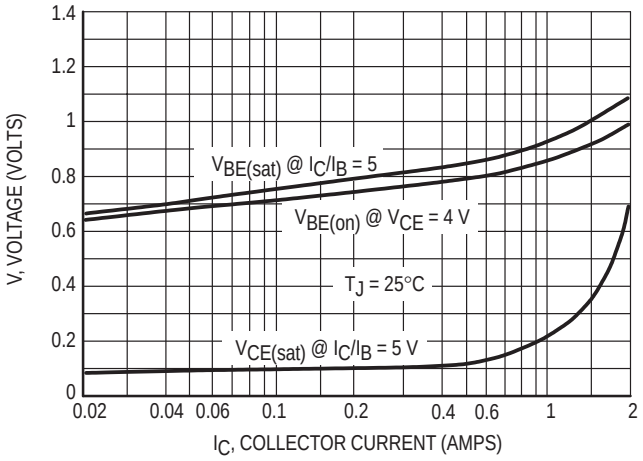


Figure 2. “On” Voltages

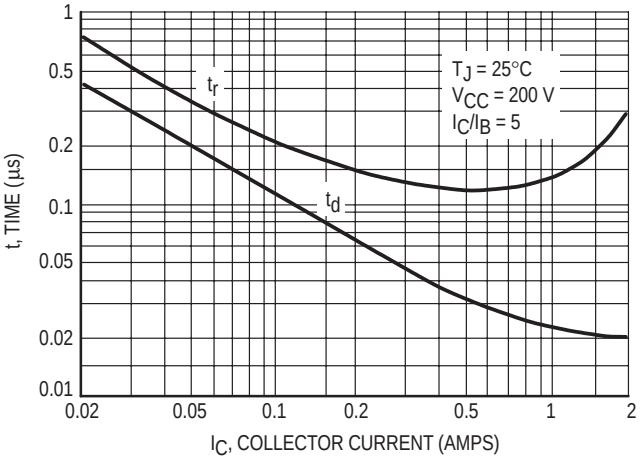


Figure 3. Turn–On Time

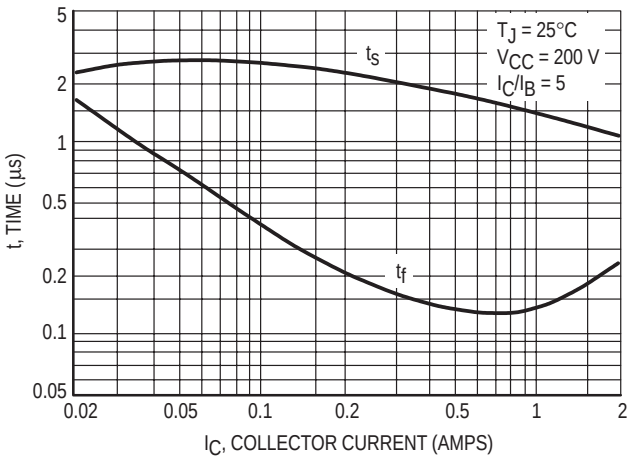


Figure 4. Turn–Off Time

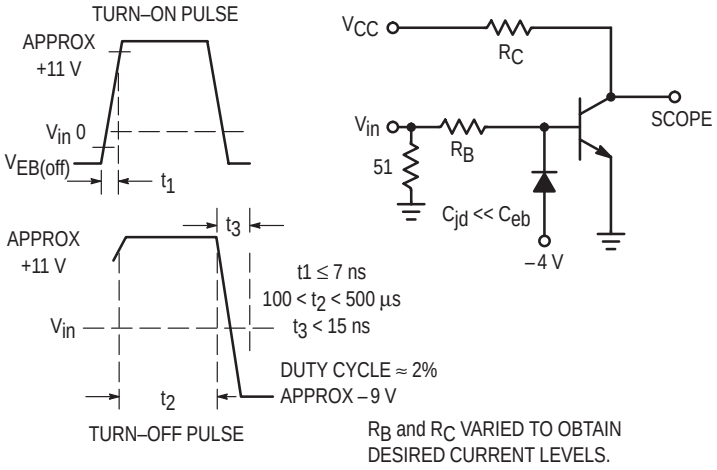


Figure 5. Switching Time Equivalent Circuit

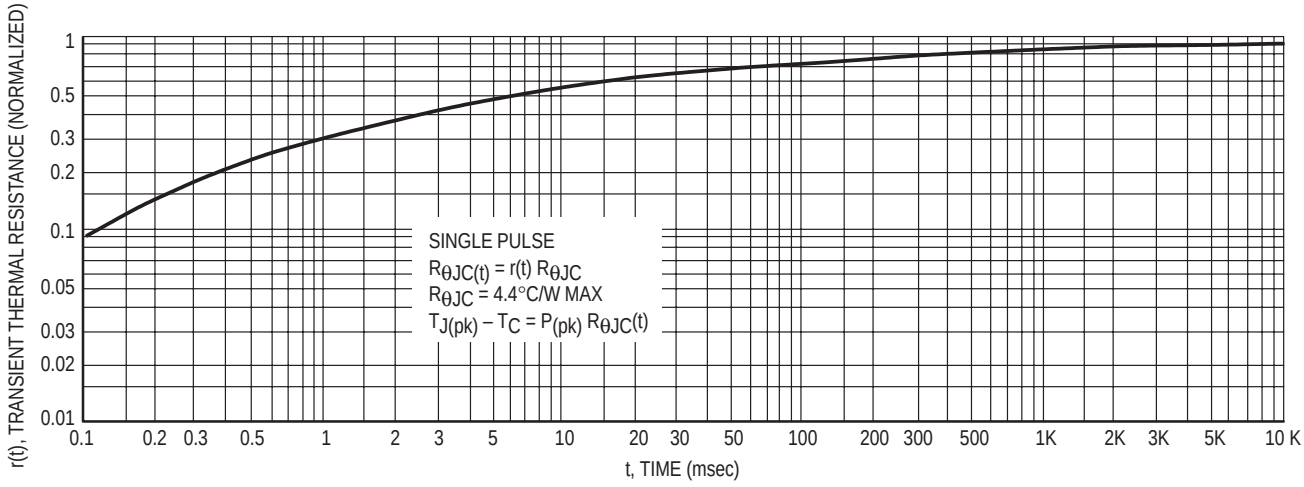


Figure 6. Thermal Response

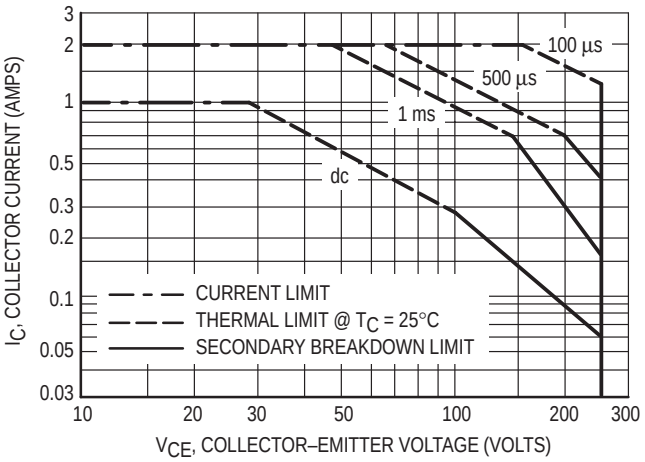


Figure 7. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 6. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

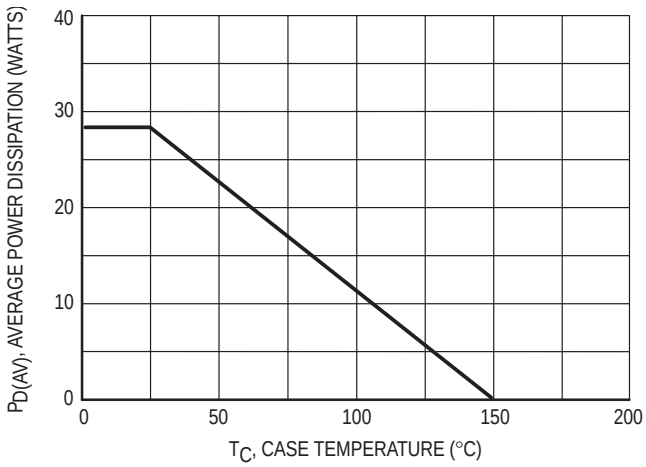


Figure 8. Power Derating

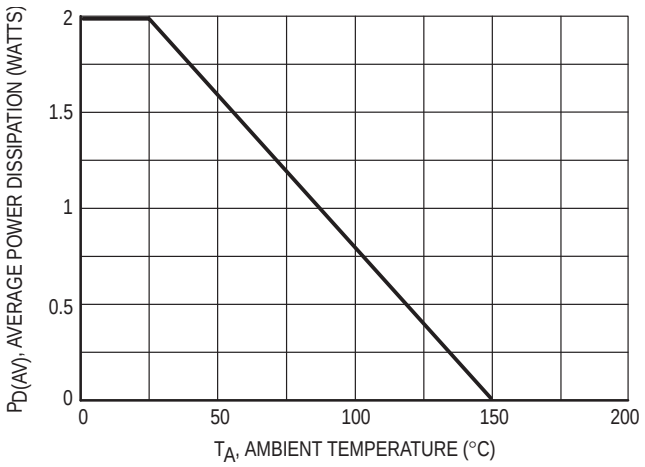


Figure 9. Power Derating

TEST CONDITIONS FOR ISOLATION TESTS*

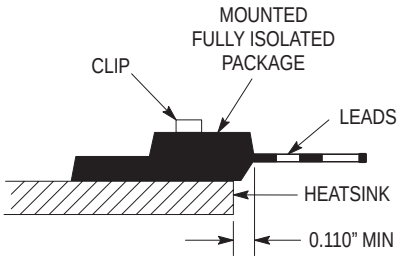


Figure 10. Clip Mounting Position for Isolation Test Number 1

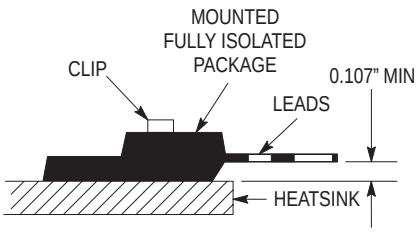


Figure 11. Clip Mounting Position for Isolation Test Number 2

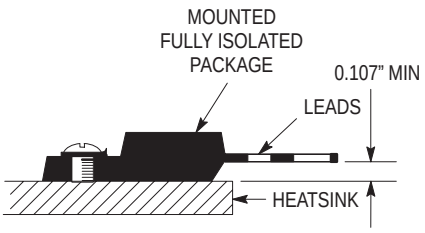


Figure 12. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

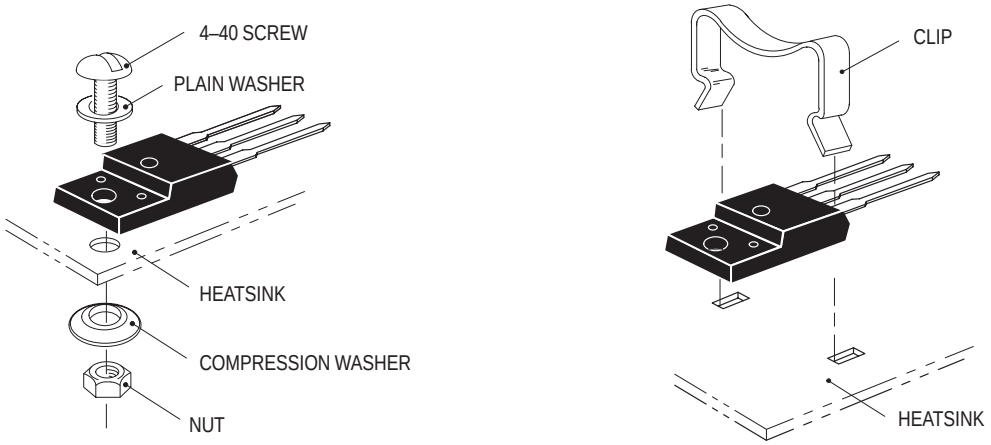


Figure 13. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

Complementary Power Darlingtons

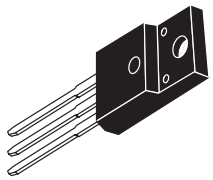
For Isolated Package Applications

NPN
MJF122
PNP
MJF127

COMPLEMENTARY SILICON POWER DARLINGTONS
5 AMPERES
100 VOLTS
30 WATTS

Designed for general–purpose amplifiers and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Electrically Similar to the Popular TIP122 and TIP127
- 100 $V_{CEO(sus)}$
- 5 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High DC Current Gain — 2000 (Min) @ I_C = 3 Adc
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation



CASE 221D–02
TO–220 TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T_A = 25°C) Test No. 1 Per Fig. 14 Test No. 2 Per Fig. 15 Test No. 3 Per Fig. 16	V_{ISOL}	4500 3500 1500	V_{RMS}
Collector Current — Continuous Peak	I_C	5 8	Adc
Base Current	I_B	0.12	Adc
Total Power Dissipation* @ T_C = 25°C Derate above 25°C	P_D	30 0.24	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2 0.016	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	I_C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	4.1	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

* Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.

(1) Proper strike and creepage distance must be provided.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)		$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)		I_{CEO}	—	10	μAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)		I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)		I_{EBO}	—	2	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3 Vdc) (I_C = 3 Adc, V_{CE} = 3 Vdc)		h_{FE}	1000 2000	— —	—
Collector–Emitter Saturation Voltage (I_C = 3 Adc, I_B = 12 mAdc) (I_C = 5 Adc, I_B = 20 mAdc)		$V_{CE(sat)}$	— —	2 3.5	Vdc
Base–Emitter On Voltage (I_C = 3 Adc, V_{CE} = 3 Vdc)		$V_{BE(on)}$	—	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 3 Adc, V_{CE} = 4 Vdc, f = 1 MHz)		h_{fe}	4	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJF127 MJF122	C_{ob}	— —	300 200	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

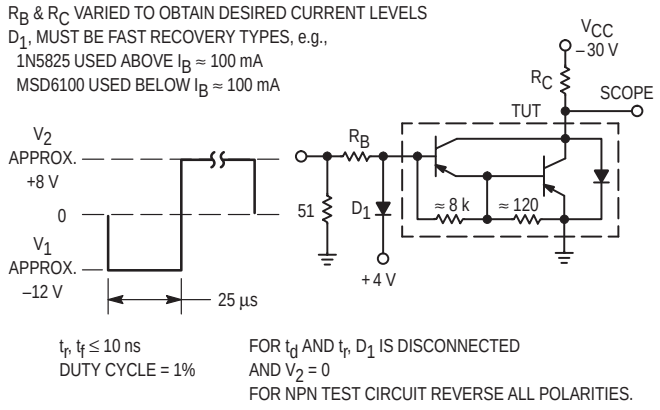


Figure 1. Switching Times Test Circuit

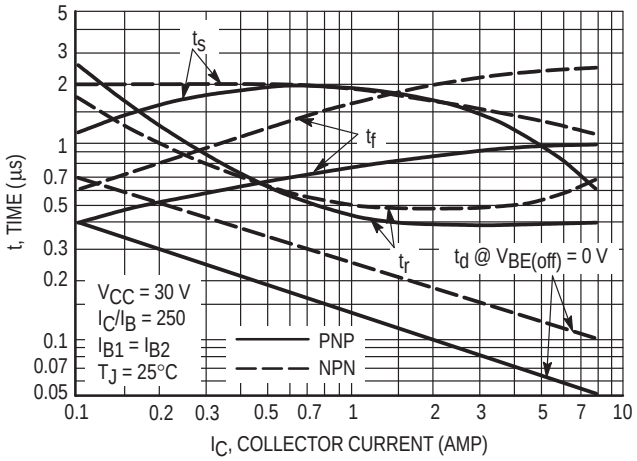


Figure 2. Typical Switching Times

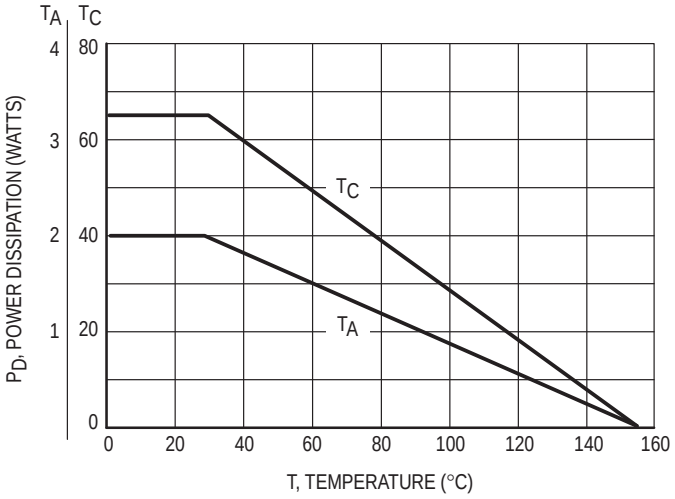


Figure 3. Maximum Power Derating

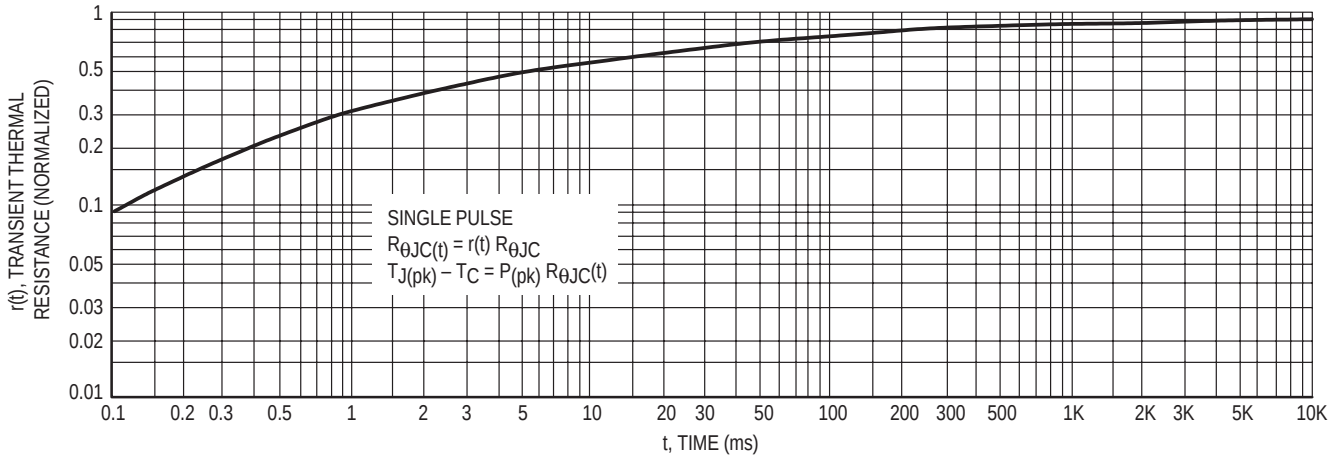


Figure 4. Thermal Response

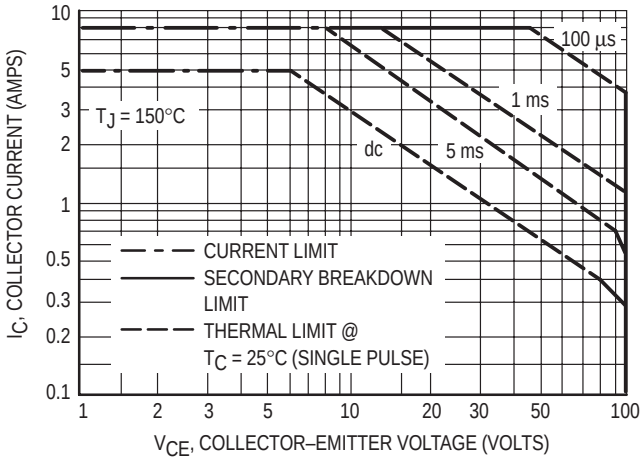


Figure 5. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

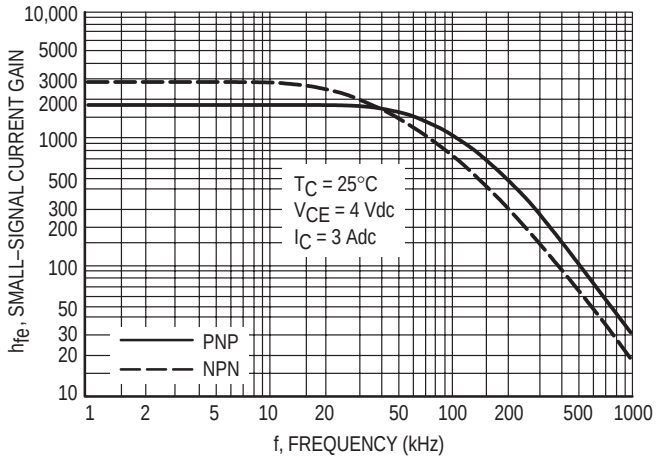


Figure 6. Typical Small–Signal Current Gain

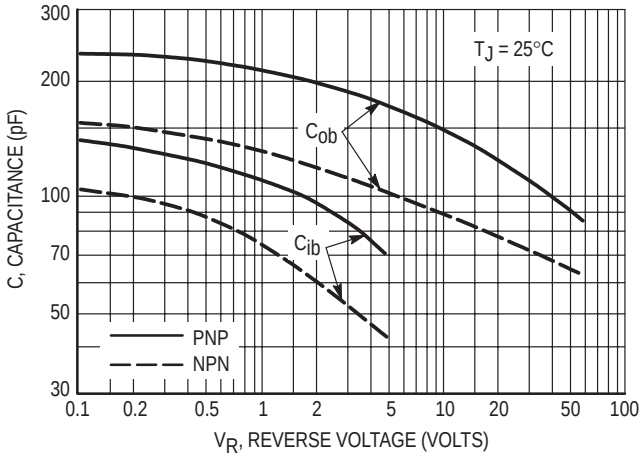


Figure 7. Typical Capacitance

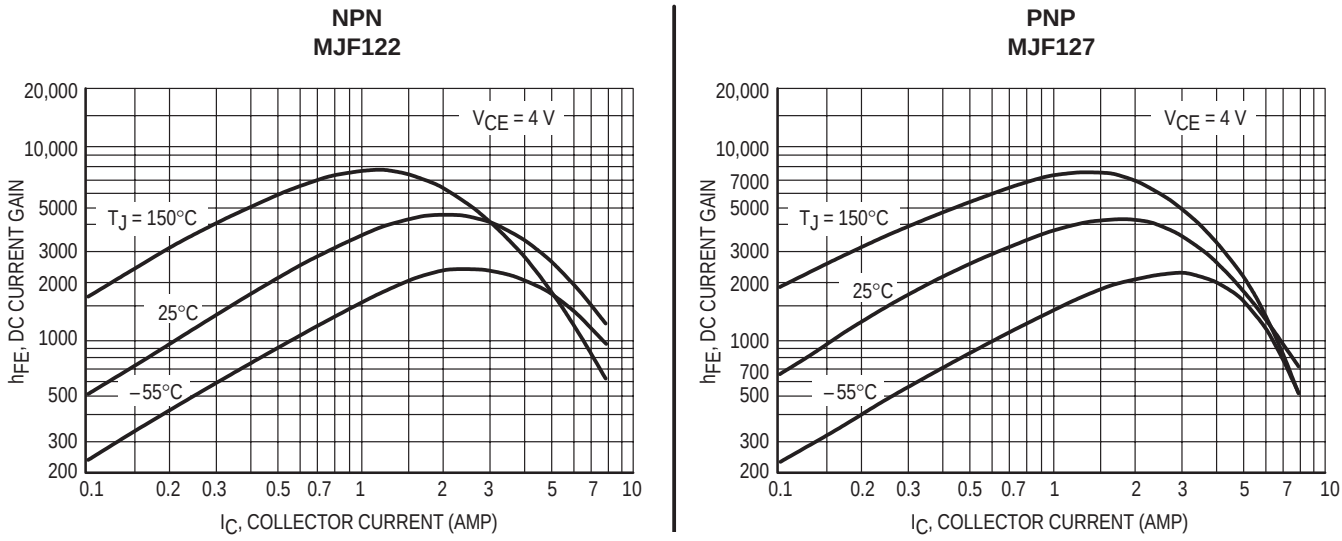


Figure 8. Typical DC Current Gain

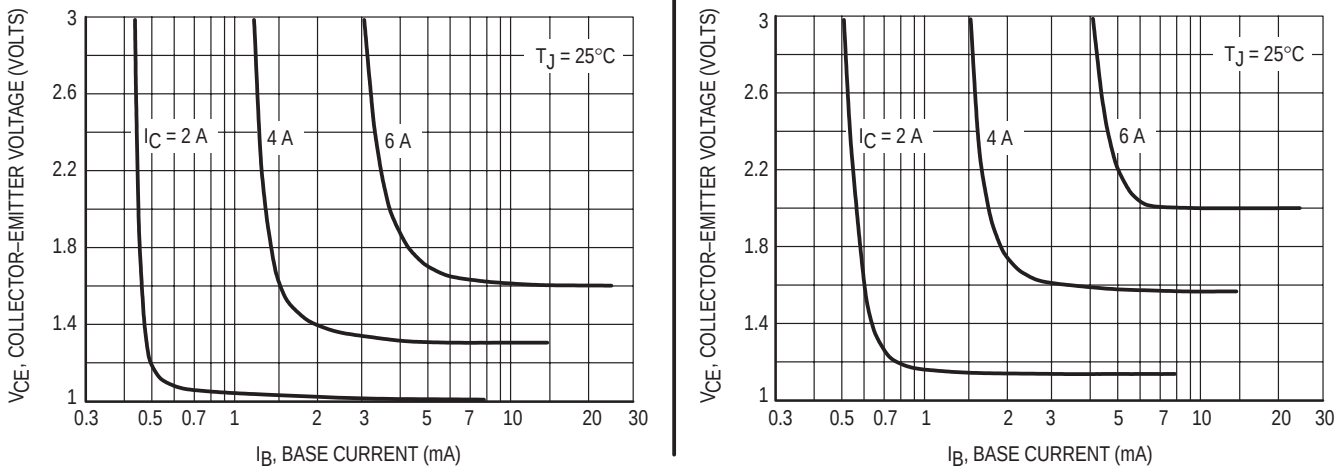
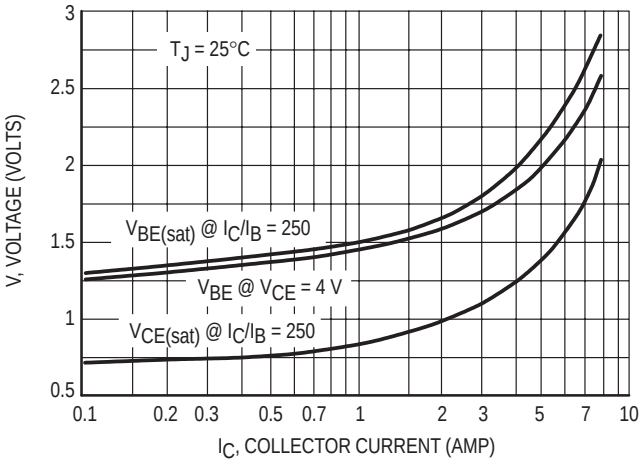


Figure 9. Typical Collector Saturation Region

NPN
MJF122



PNP
MJF127

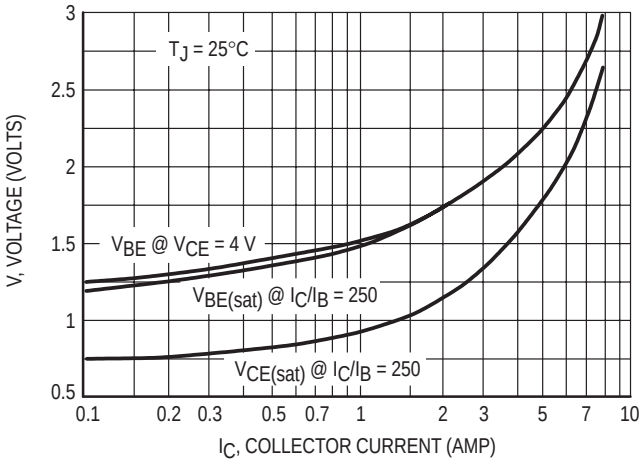
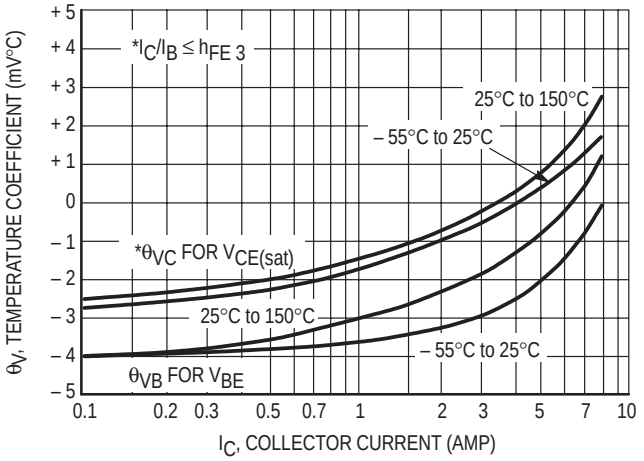


Figure 10. Typical “On” Voltages



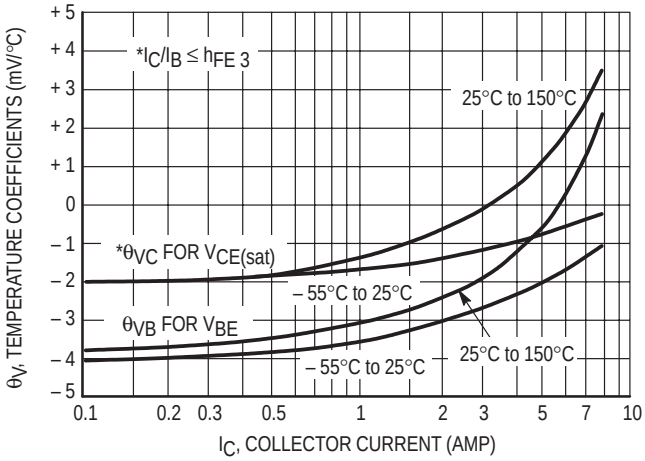
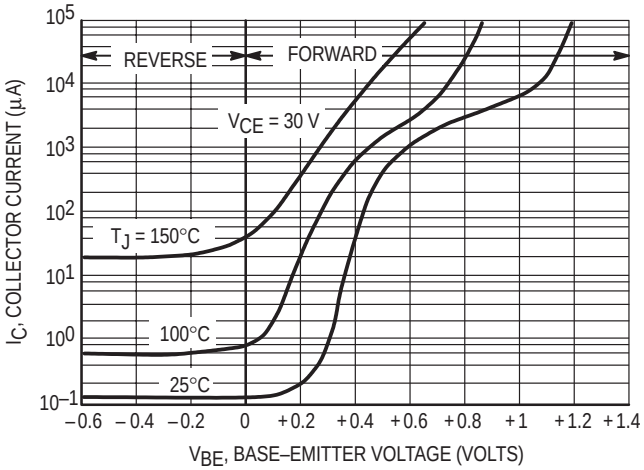


Figure 11. Typical Temperature Coefficients



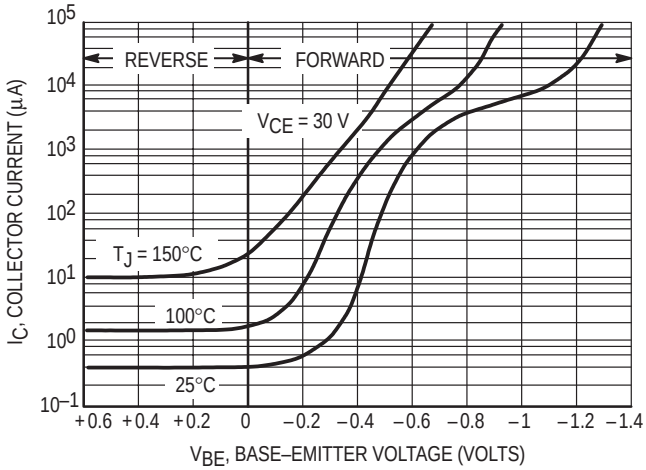


Figure 12. Typical Collector Cut–Off Region

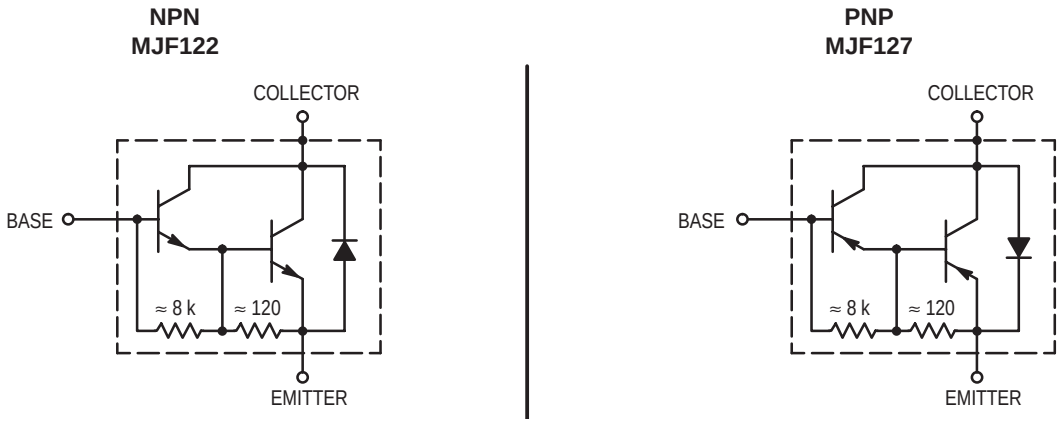


Figure 13. Darlington Schematic

TEST CONDITIONS FOR ISOLATION TESTS*

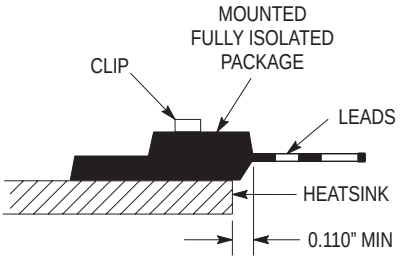


Figure 14. Clip Mounting Position for Isolation Test Number 1

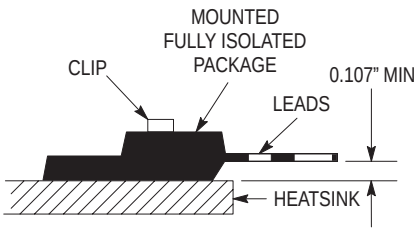


Figure 15. Clip Mounting Position for Isolation Test Number 2

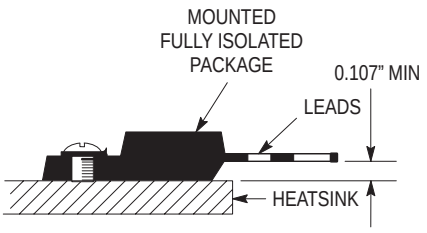


Figure 16. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

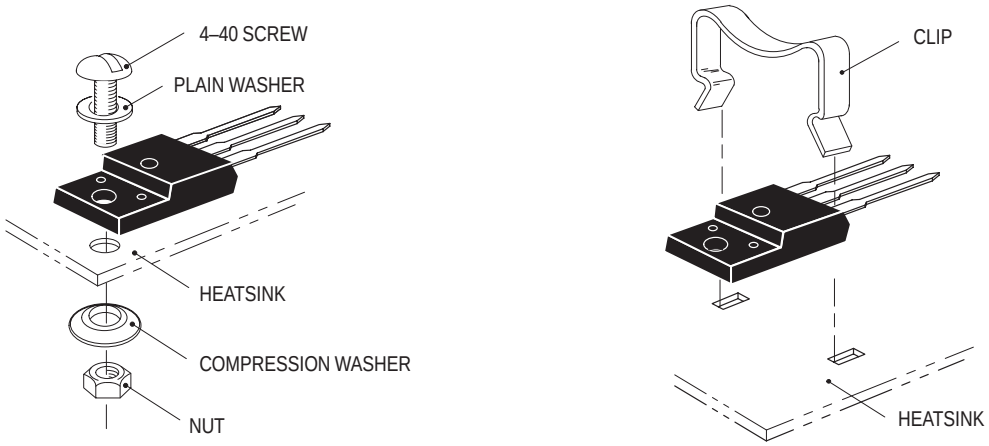


Figure 17. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

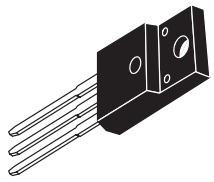
Complementary Silicon Power Transistors

NPN
MJF3055
PNP
MJF2955

. . . specifically designed for general purpose amplifier and switching applications.

- Isolated Overmold Package (1500 Volts RMS Min)
- Electrically Similar to the Popular MJE3055T and MJE2955T
- Collector–Emitter Sustaining Voltage — $V_{CEO(sus)}$ 90 Volts
- 10 Amperes Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation

COMPLEMENTARY SILICON POWER TRANSISTORS
10 AMPERES
90 VOLTS
30 WATTS



CASE 221D–02
TO–220 TYPE

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector–Emitter Sustaining Voltage		$V_{CEO(sus)}$	90	Vdc
Collector–Emitter Breakdown Voltage		V_{CES}	90	Vdc
Base–Emitter Voltage		V_{EBO}	5	Vdc
Collector Current — Continuous		I_C	10	Adc
Base Current — Continuous		I_B	6	Adc
RMS Isolation Voltage (3) (for 1 sec, R.H. < 30%, T_A = 25°C)	Test No. 1 Per Fig. 4 Test No. 2 Per Fig. 5 Test No. 3 Per Fig. 6	V_{ISOL}	4500 3500 1500	V_{RMS}
Total Power Dissipation @ T_C = 25°C (2) Derate above 25°C		P_D	30 0.25	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C		P_D	2 0.016	Watts W/°C
Operating and Storage Temperature Range		T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case (2)	$R_{\theta JC}$	4	°C/W
Thermal Resistance — Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Lead Temperature for Soldering Purposes	T_L	260	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.
(2) Measurement made with thermocouple contacting the bottom insulated surface (in a location beneath the die), the devices mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.
(3) Proper strike and creepage distance must be provided.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)				
Collector–Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	90	—	Vdc
Collector Cutoff Current (V_{CE} = 90 Vdc, V_{BE} = 0)	I_{CES}	—	1	μAdc
Collector Cutoff Current (V_{CE} = 90 Vdc, I_E = 0)	I_{CBO}	—	1	μAdc
Emitter–Base Leakage (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	—	1	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_{CE} = 4 Adc, V_{CE} = 4 Vdc) (I_{CE} = 10 Adc, V_{CE} = 4 Vdc)	h_{FE}	20 5	100 —	—
Collector–Emitter Saturation Voltage (I_C = 4 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	 — —	 1 2.5	Vdc
Base–Emitter On Voltage (I_C = 4 Adc, V_{BE} = 4 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain–Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.5 Adc, f_{test} = 500 kHz)	f_T	2	—	MHz

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

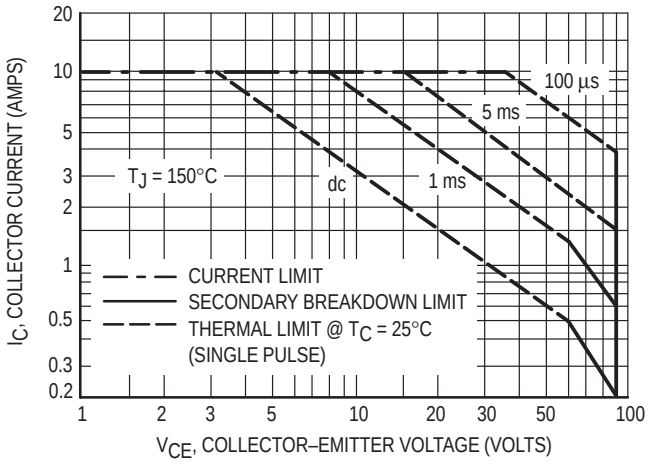


Figure 1. Maximum Forward Bias Safe Operating Area

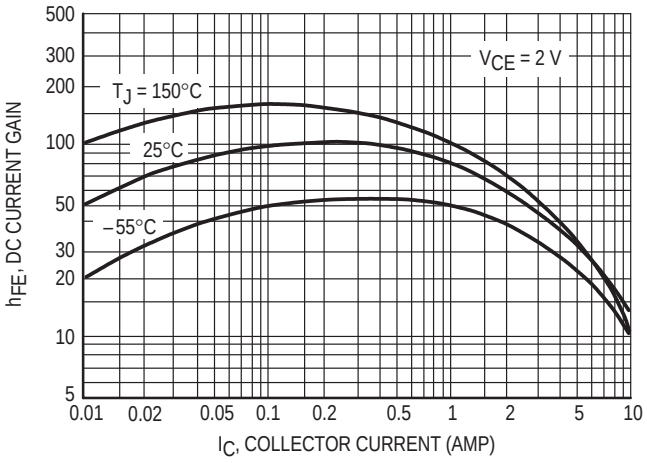


Figure 2. DC Current Gain

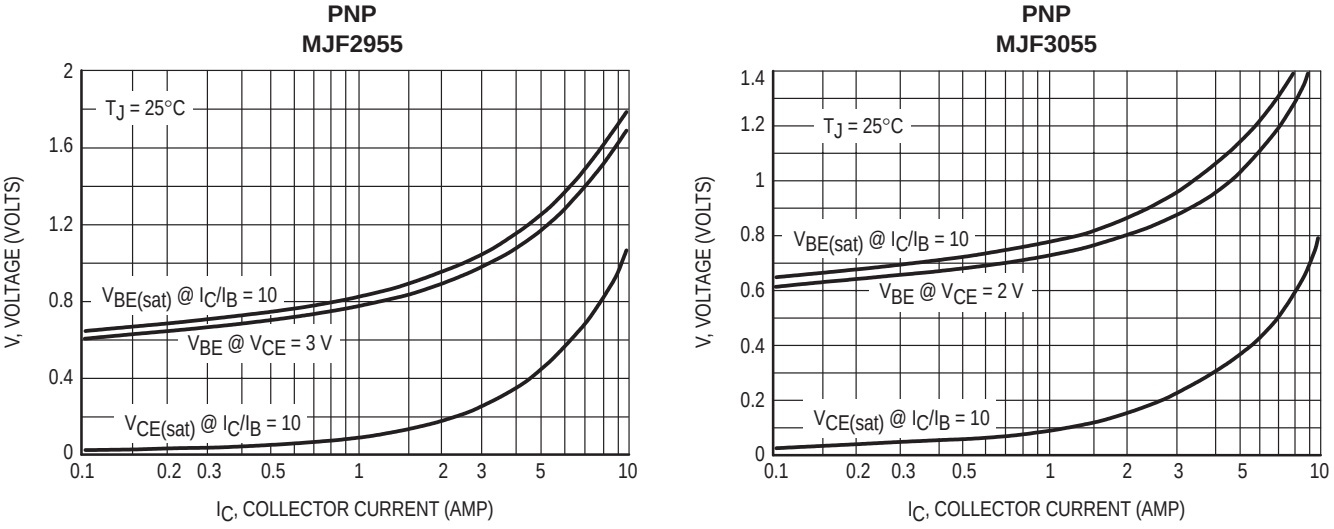


Figure 3. "On" Voltages

TEST CONDITIONS FOR ISOLATION TESTS*

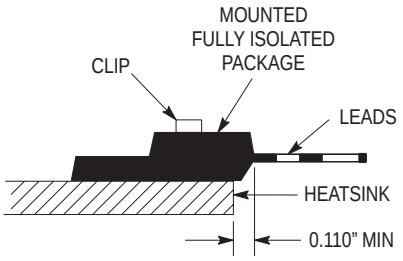


Figure 4. Clip Mounting Position for Isolation Test Number 1

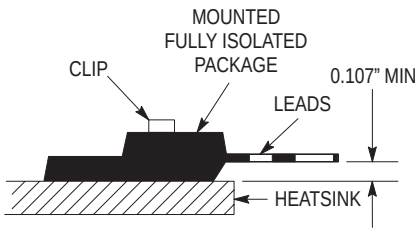


Figure 5. Clip Mounting Position for Isolation Test Number 2

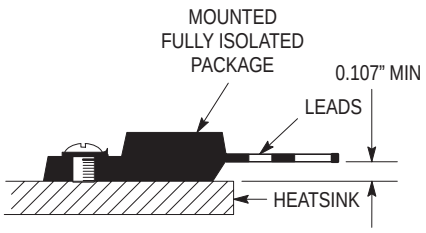


Figure 6. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

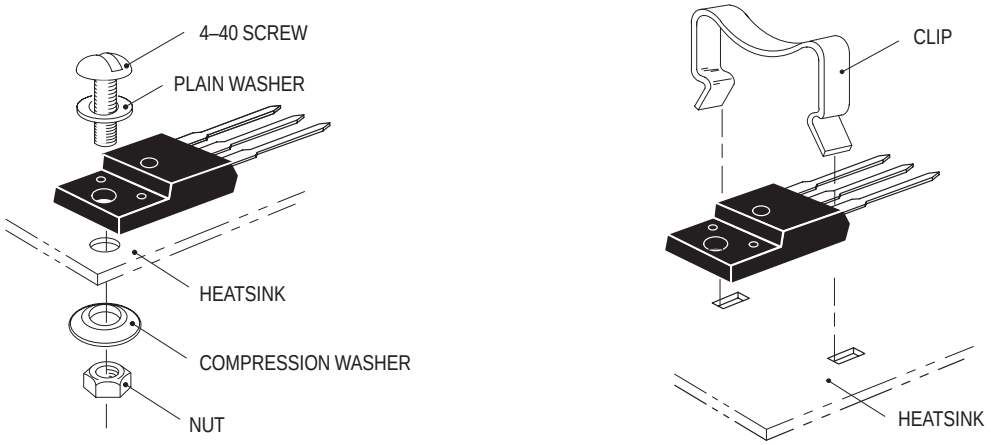


Figure 7. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

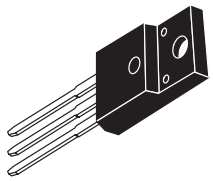
MJF6107

Power Transistor
For Isolated Package Applications

PNP SILICON
POWER TRANSISTOR
7 AMPERES
70 VOLTS
34 WATTS

Designed for general–purpose amplifier and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Electrically Similar to the Popular 2N6107
- 70 $V_{CEO(sus)}$
- 7 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High Current Gain–Bandwidth Product
  f_T = 4 MHz (Min) Ca, I_C = 500 mAdc
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation



CASE 221D–02
TO–220 TYPE

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector–Emitter Voltage		V_{CEO}	70	Vdc
Collector–Base Voltage		V_{CB}	80	Vdc
Emitter–Base Voltage		V_{EB}	5	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T_A = 25°C)	Test No. 1 Per Fig. 13 Test No. 2 Per Fig. 14 Test No. 3 Per Fig. 15	V_{ISOL}	4500 3500 1500	V_{RMS}
Collector Current — Continuous Peak		I_C	7 10	Adc
Base Current		I_B	3	Adc
Total Power Dissipation* @ T_C = 25°C Derate above 25°C		P_D	34 0.27	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C		P_D	2 0.016	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	3.7	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

* Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.

(1) Proper strike and creepage distance must be provided.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	70	—	Vdc
Collector Cutoff Current (V_{CE} = 80 Vdc, I_B = 0)	I_{CES}	—	1	μAdc
Collector Cutoff Current (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc)	I_{CEX}	—	1	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	1	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 2 Adc, V_{CE} = 4 Vdc) (I_C = 7 Adc, V_{CE} = 4 Vdc)	h_{FE}	30 5	90 —	—
Collector–Emitter Saturation Voltage (I_C = 7 Adc, I_B = 3 Adc)	$V_{CE(sat)}$	—	2	Vdc
Base–Emitter On Voltage (I_C = 7 Adc, V_{CE} = 4 Vdc)	$V_{BE(on)}$	—	2	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain–Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 4 Vdc, f_{test} = 1 MHz)	f_T	4	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1 MHz)	C_{ob}	—	250	pF
Small–Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 4 Vdc, f = 50 kHz)	h_{fe}	20	—	—

NOTES:
1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. $f_T = |h_{fe}| \bullet f_{test}$.

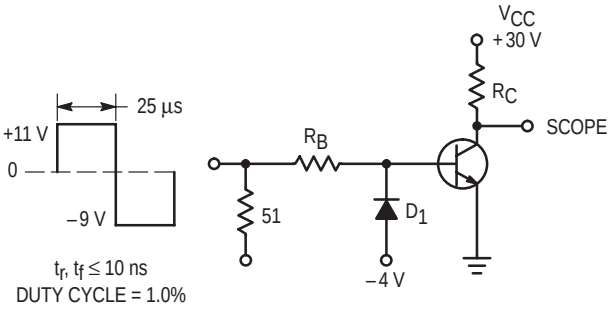


Figure 1. Switching Time Test Circuit

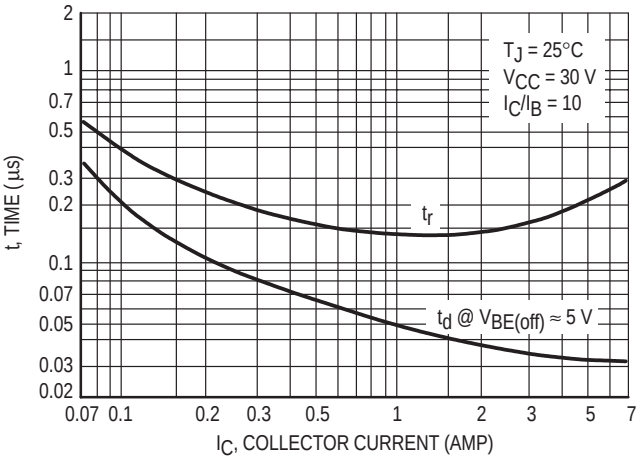


Figure 2. Turn–On Time

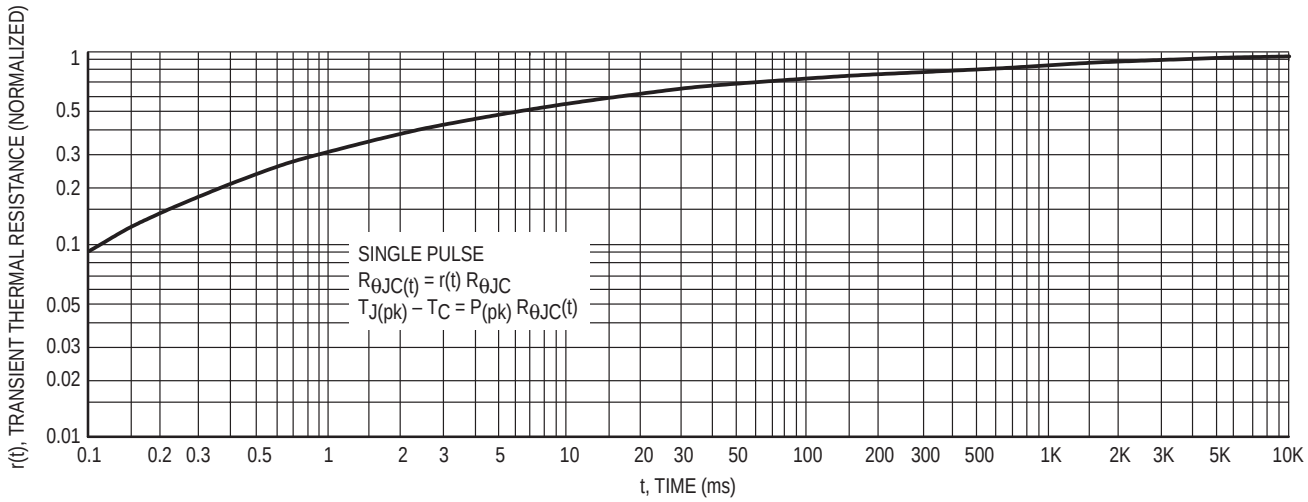


Figure 3. Thermal Response

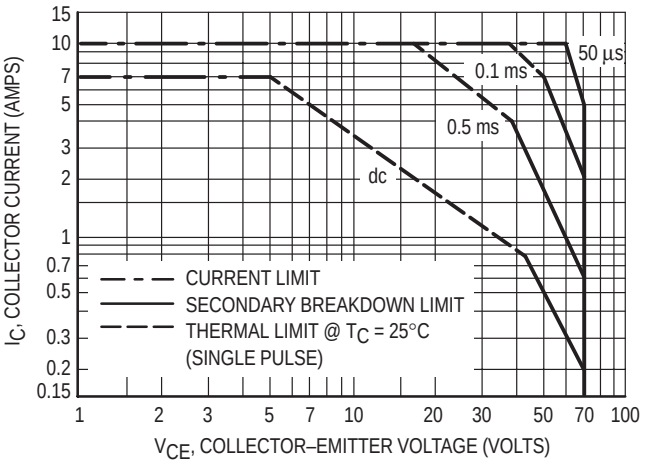


Figure 4. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

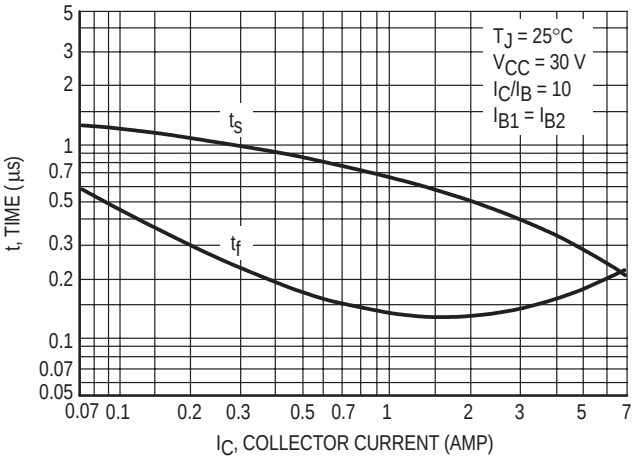


Figure 5. Turn–Off Time

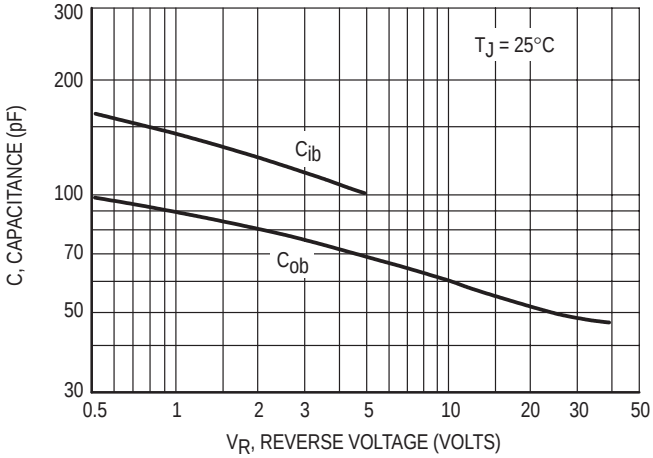


Figure 6. Capacitance

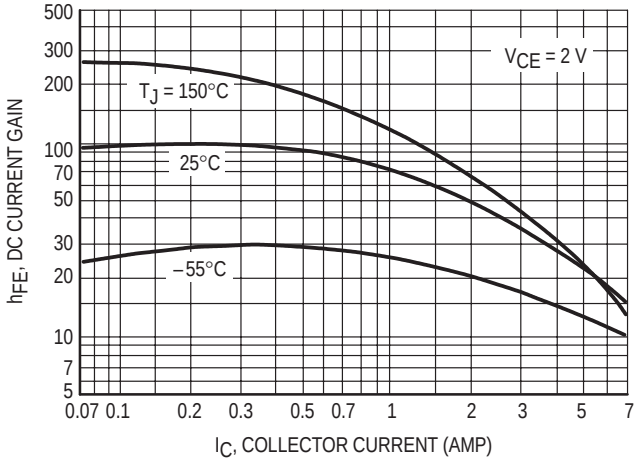


Figure 7. DC Current Gain

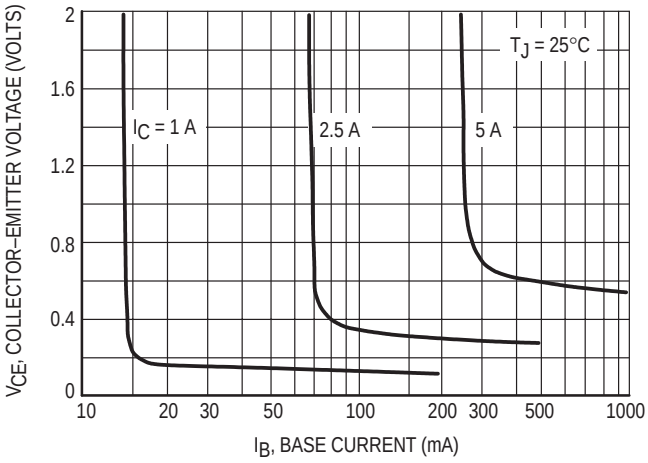


Figure 8. Collector Saturation Region

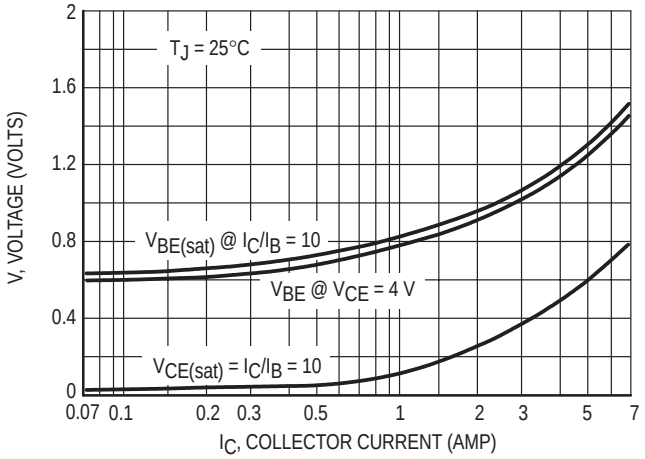


Figure 9. “On” Voltages

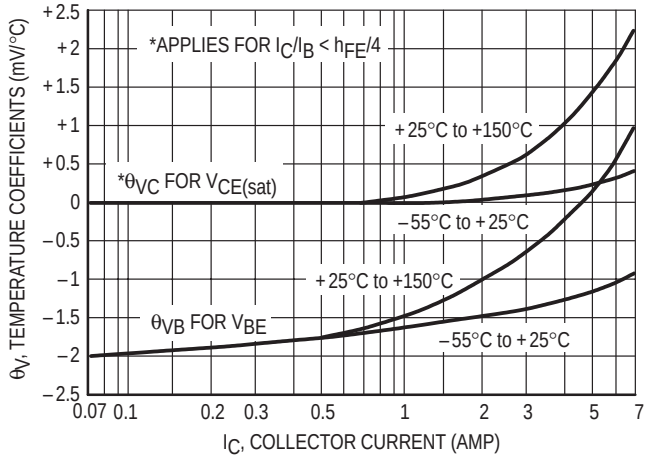


Figure 10. Temperature Coefficients

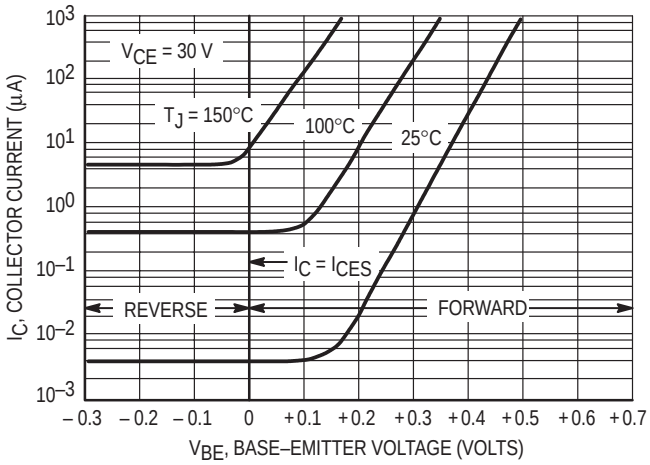


Figure 11. Collector Cut–Off Region

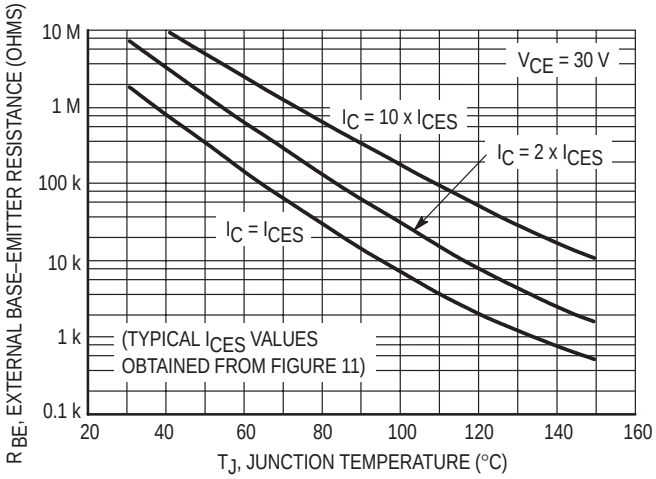


Figure 12. Effects of Base–Emitter Resistance

TEST CONDITIONS FOR ISOLATION TESTS*

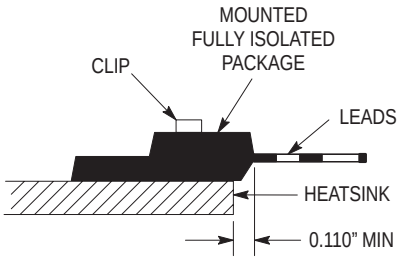


Figure 13. Clip Mounting Position for Isolation Test Number 1

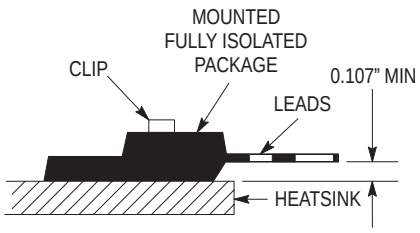


Figure 14. Clip Mounting Position for Isolation Test Number 2

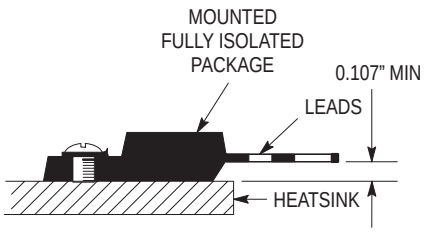


Figure 15. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

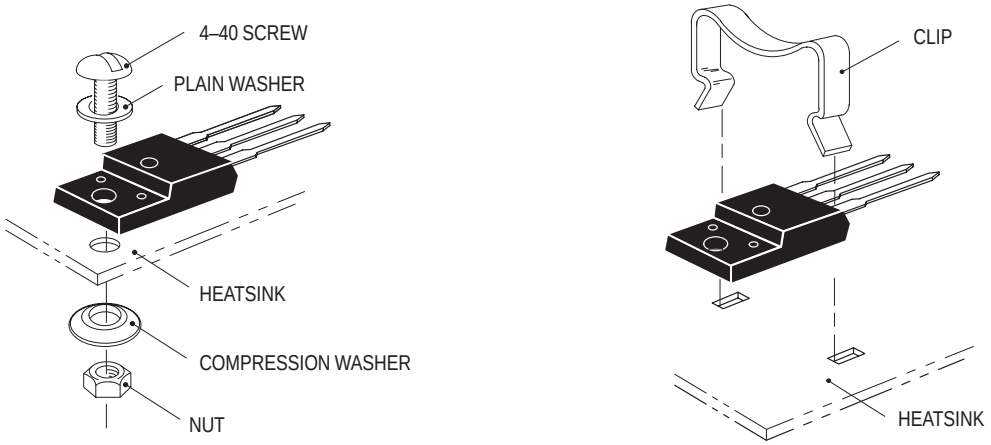


Figure 16. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

Complementary Power Darlingtons

For Isolated Package Applications

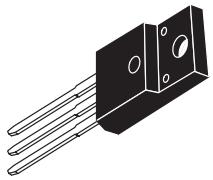
NPN
MJF6388*
PNP
MJF6668*

*Motorola Preferred Devices

Designed for general–purpose amplifiers and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Isolated Overmold Package, TO–220 Type
- Electrically Similar to the Popular 2N6388, 2N6668, TIP102 and TIP107
- 100 $V_{CEO(sus)}$
- 10 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High DC Current Gain — 1000 (Min) @ I_C = 5.0 Adc
- High Isolation Voltage (up to 4500 VRMS)
- Case 221D is UL Recognized at 3500 VRMS: File #E69369

COMPLEMENTARY
SILICON
POWER DARLINGTONS
10 AMPERES
100 VOLTS
40 WATTS



CASE 221D–02
UL RECOGNIZED

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T_A = 25°C) Test No. 1 Per Figure 14 / Test No. 2 Per Figure 15 / Test No. 3 Per Figure 16	V_{ISOL}	4500 / 3500 / 1500	V
Collector Current — Continuous / — Peak(2)	I_C	10 / 15	Adc
Base Current	I_B	1.0	Adc
Total Power Dissipation* @ T_C = 25°C / Derate above 25°C	P_D	40 / 0.31	Watts / W/°C
Total Power Dissipation @ T_A = 25°C / Derate above 25°C	P_D	2.0 / 0.016	Watts / W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	3.2	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

(1) Proper strike and creepage distance must be provided.
(2) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
* Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink, thermal grease applied and a mounting torque of 6 to 8 in•lbs.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 80 Vdc, I_B = 0)	I_{CEO}	—	10	μAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	I_{CEX}	— —	10 3.0	μAdc mAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 3.0 Vdc)	h_{FE}	3000 1000 200 100	15000 — — —	—
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 6.0 mAdc) (I_C = 5.0 Adc, I_B = 0.01 Adc) (I_C = 8.0 Adc, I_B = 80 mAdc) (I_C = 10 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	— — — —	2.0 2.0 2.5 3.0	Vdc
Base–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.01 Adc) (I_C = 10 Adc, I_B = 0.1 Adc)	$V_{BE(sat)}$	— —	2.8 4.5	Vdc
Base–Emitter On Voltage (I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	2.5	Vdc
DYNAMIC CHARACTERISTICS				
Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	$\|h_{fe}\|$	20	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz) MJF6388 MJF6668	C_{ob}	—	200 300	pF
Insulation Capacitance (Collector–to–External Heatsink)	C_{c-hs}	—	3.0 Typ	pF
Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	h_{fe}	1000	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

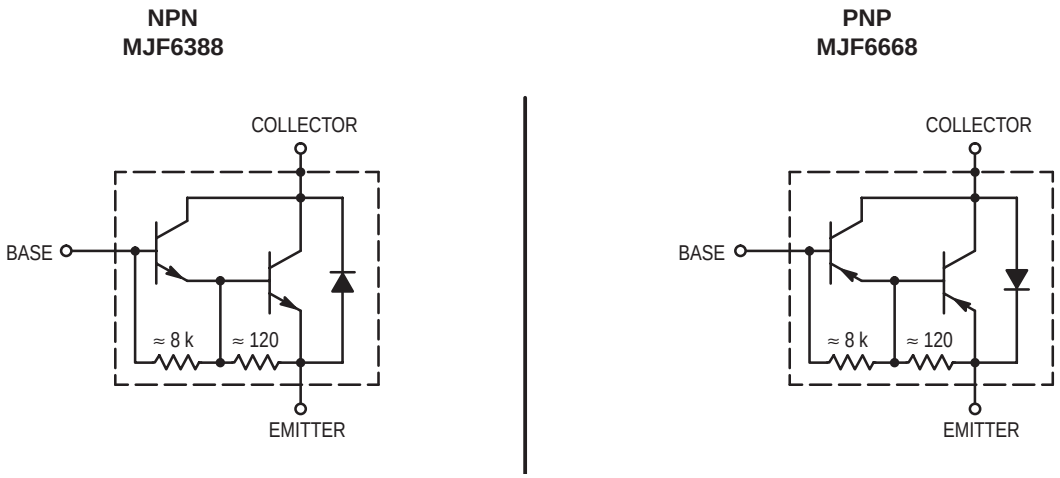


Figure 1. Darlington Schematic

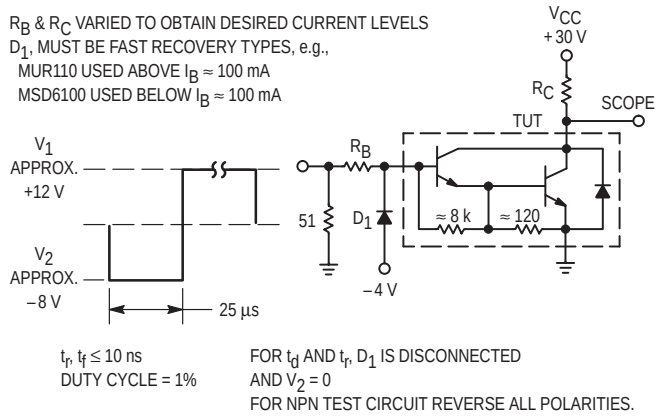


Figure 2. Switching Times Test Circuit

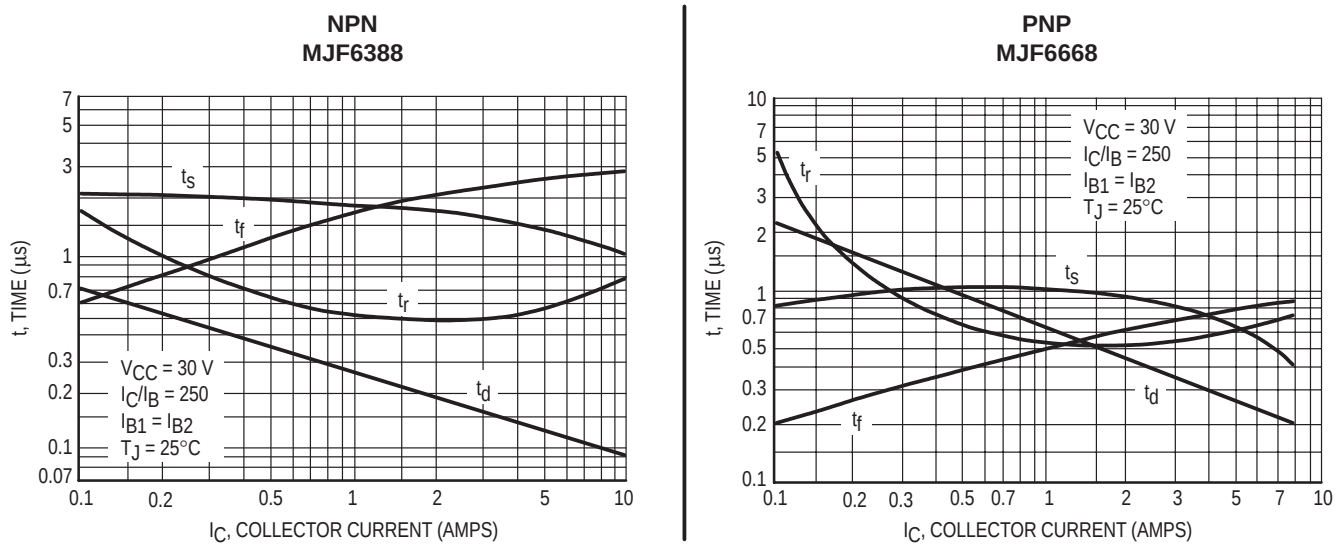


Figure 3. Typical Switching Times

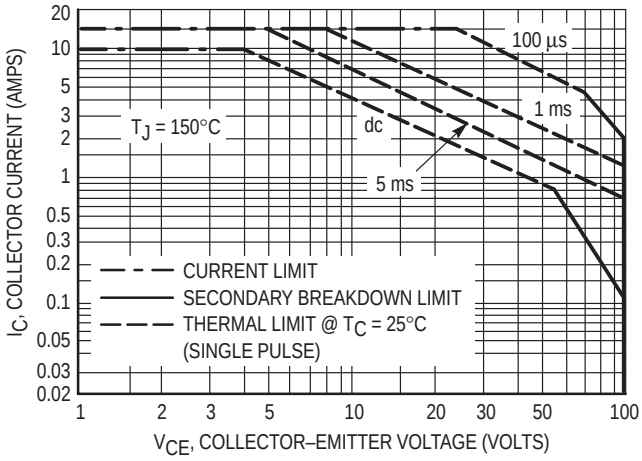


Figure 4. Maximum Forward Bias Safe Operating Area

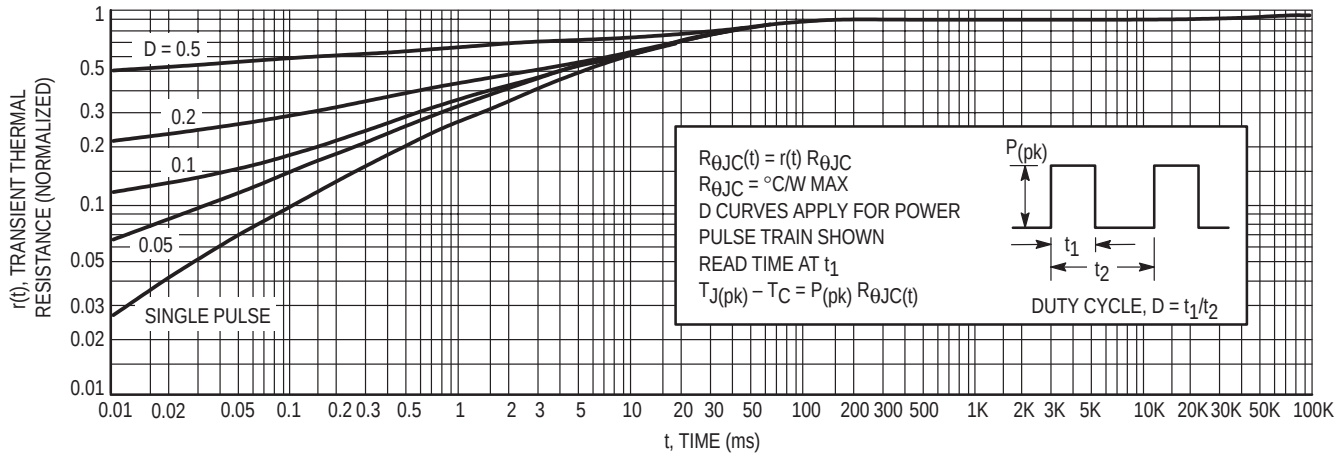


Figure 5. Thermal Response

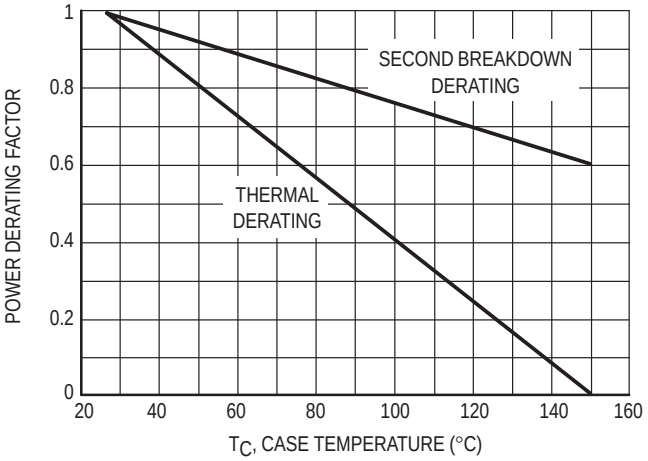


Figure 6. Maximum Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)}$ = l50°C; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

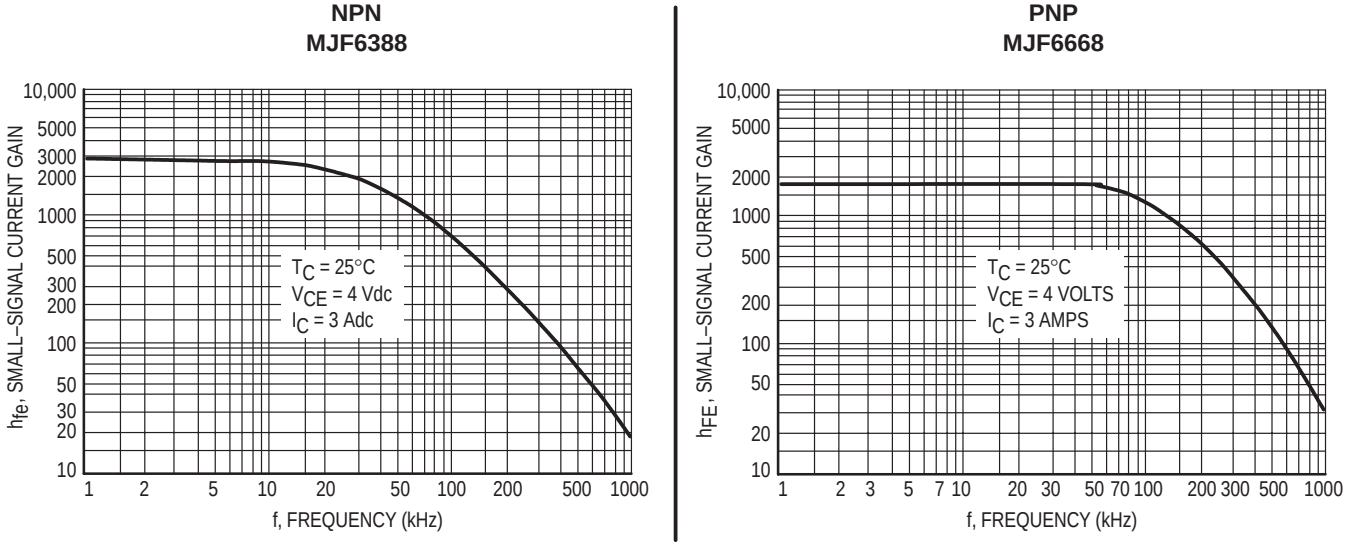


Figure 7. Typical Small–Signal Current Gain

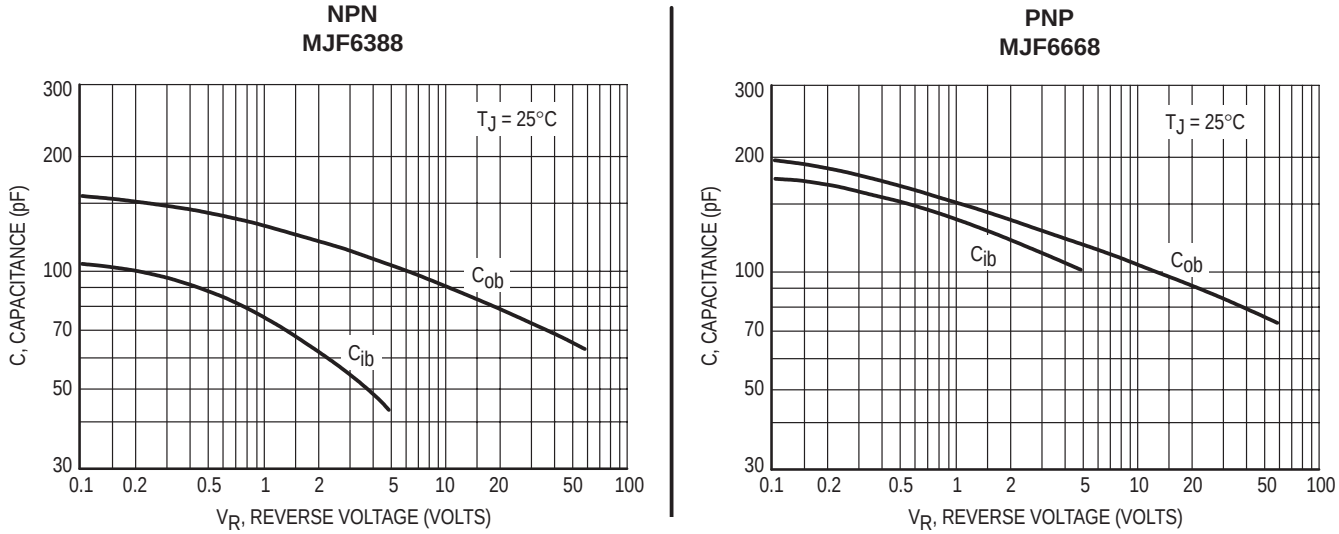


Figure 8. Typical Capacitance

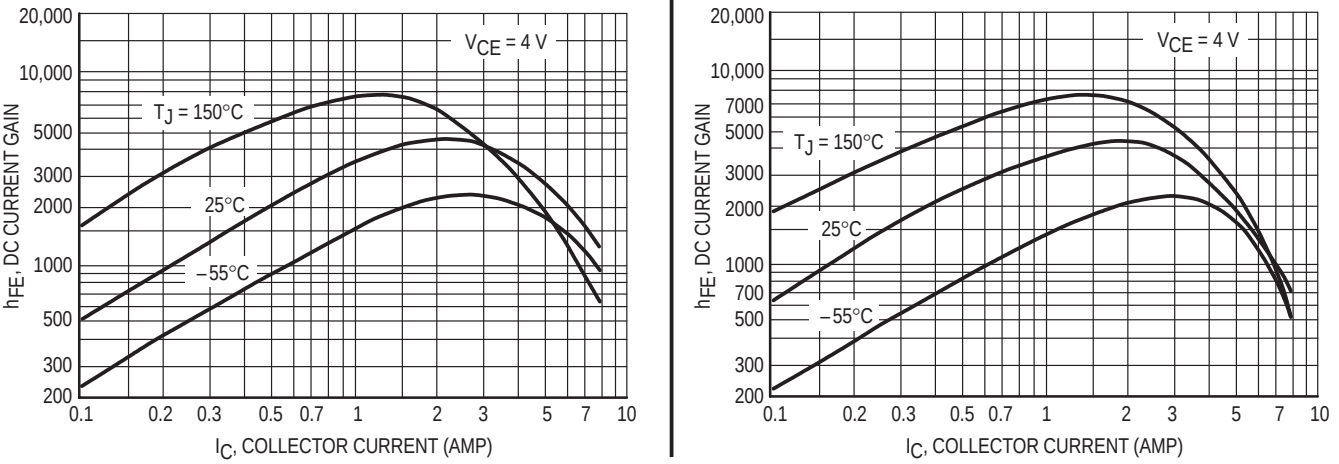


Figure 9. Typical DC Current Gain

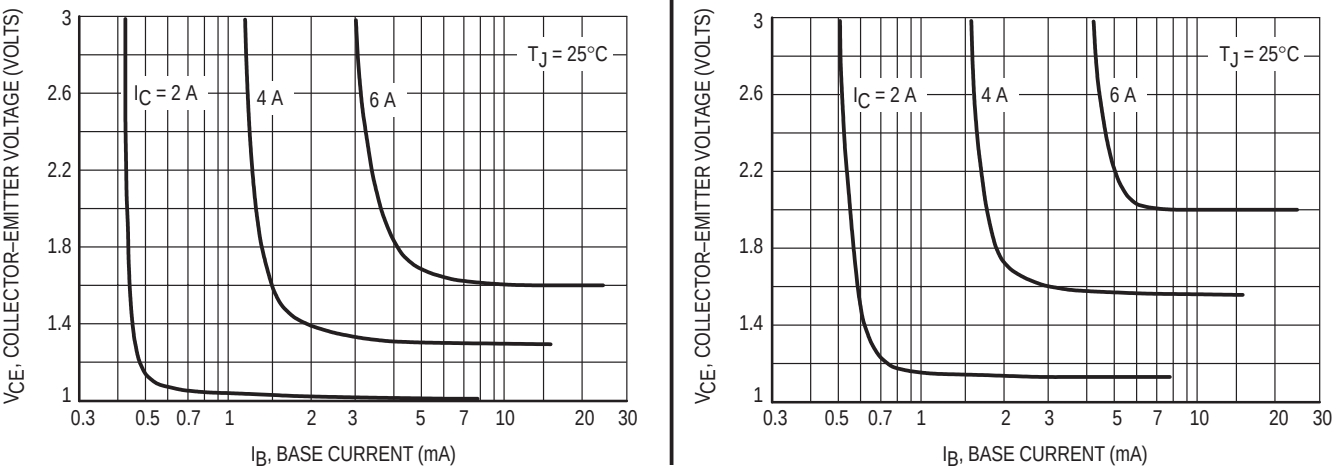
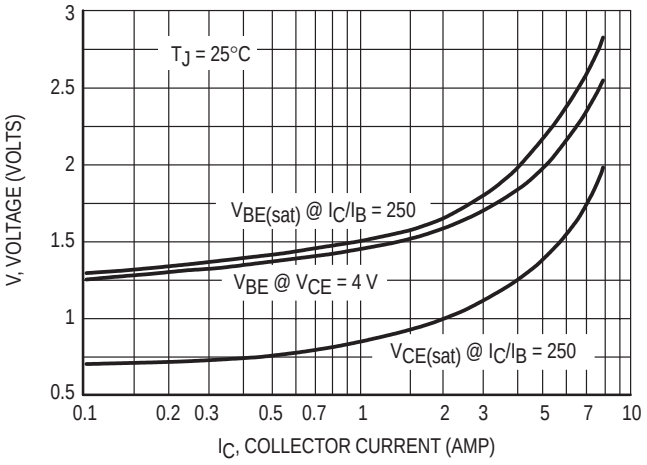


Figure 10. Typical Collector Saturation Region

NPN
MJF6388



PNP
MJF6668

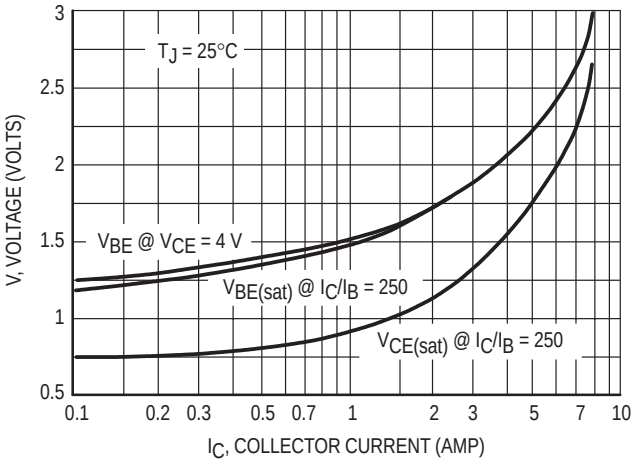
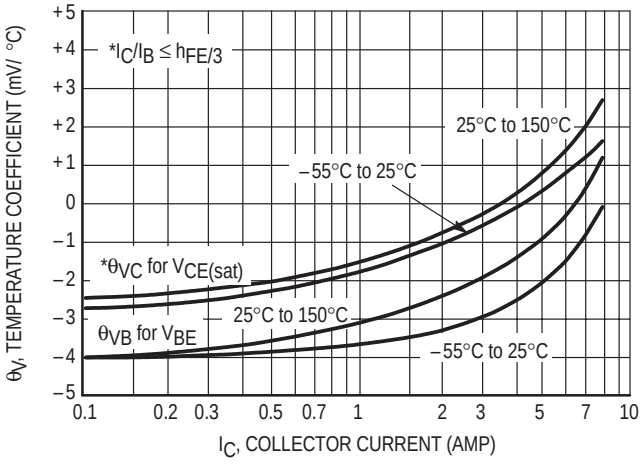


Figure 11. Typical “On” Voltages



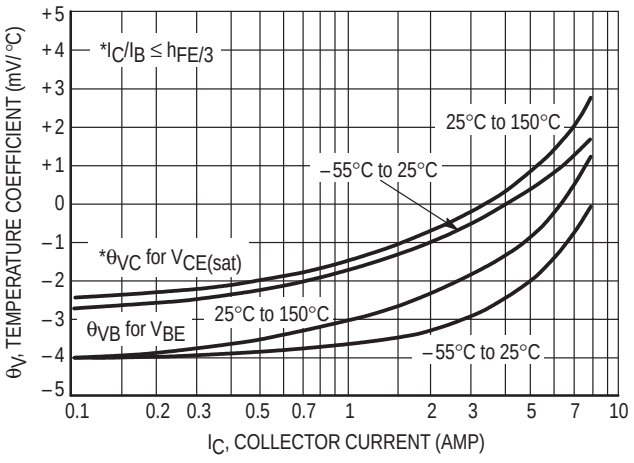
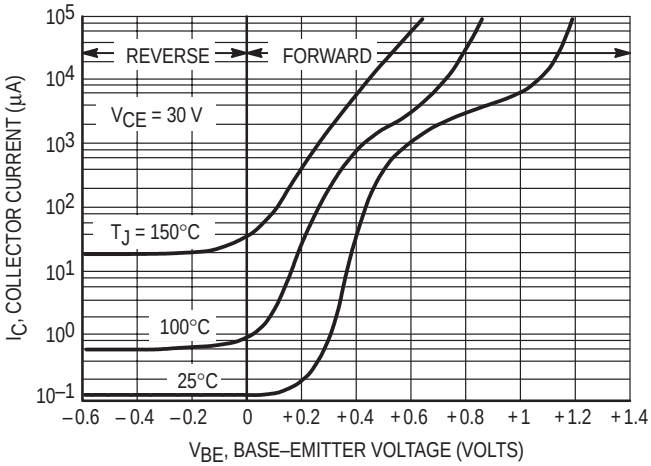


Figure 12. Typical Temperature Coefficients



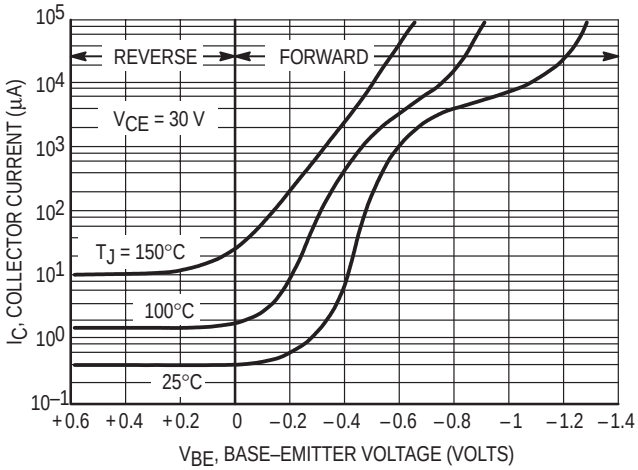


Figure 13. Typical Collector Cut–Off Region

TEST CONDITIONS FOR ISOLATION TESTS*

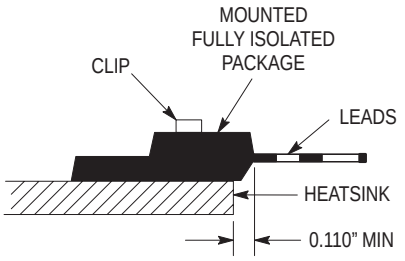


Figure 14. Clip Mounting Position for Isolation Test Number 1

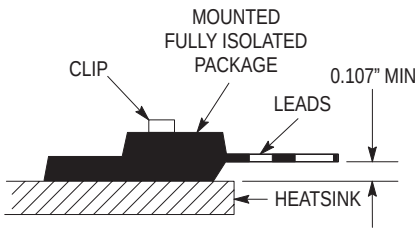


Figure 15. Clip Mounting Position for Isolation Test Number 2

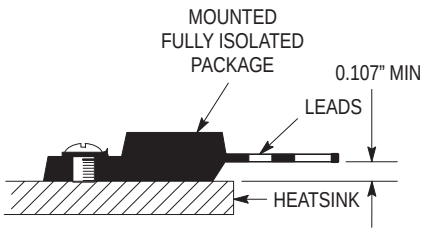


Figure 16. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

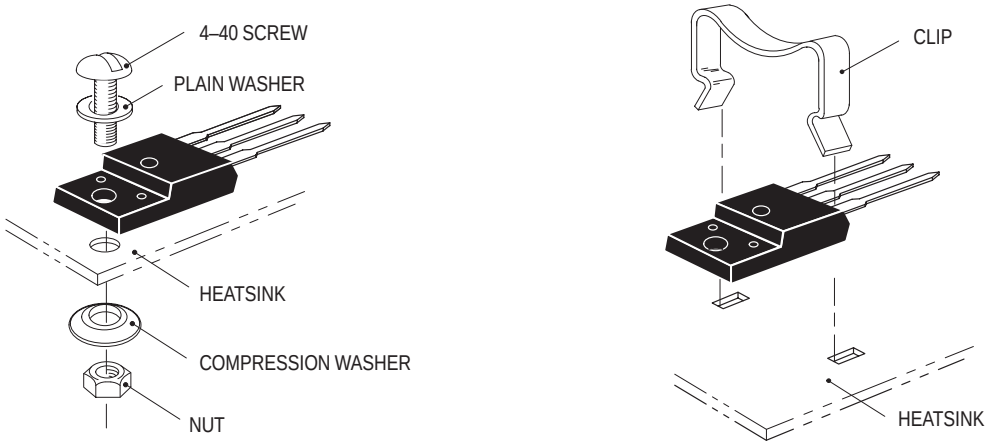


Figure 17. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

Complementary Power Transistors

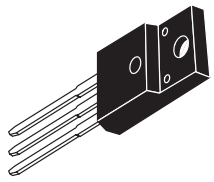
For Isolated Package Applications

NPN
MJF15030
PNP
MJF15031

Designed for general–purpose amplifier and switching applications, where the mounting surface of the device is required to be electrically isolated from the heatsink or chassis.

- Electrically Similar to the Popular MJE15030 and MJE15031
- 150 $V_{CEO(sus)}$
- 8 A Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- High Current Gain–Bandwidth Product
  f_T = 30 MHz (Min) @ I_C = 500 mAdc
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation

COMPLEMENTARY SILICON POWER TRANSISTORS
8 AMPERES
150 VOLTS
36 WATTS



CASE 221D–02
TO–220 TYPE

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector–Emitter Voltage		V_{CEO}	150	Vdc
Collector–Base Voltage		V_{CB}	150	Vdc
Emitter–Base Voltage		V_{EB}	5	Vdc
RMS Isolation Voltage (1) (for 1 sec, R.H. < 30%, T_A = 25°C)	Test No. 1 Per Fig. 11 Test No. 2 Per Fig. 12 Test No. 3 Per Fig. 13	V_{ISOL}	4500 3500 1500	V_{RMS}
Collector Current — Continuous — Peak		I_C	8 16	Adc
Base Current		I_B	2	Adc
Total Power Dissipation* @ T_C = 25°C Derate above 25°C		P_D	36 0.29	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C		P_D	2 0.016	Watts W/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case*	$R_{\theta JC}$	3.5	°C/W
Lead Temperature for Soldering Purpose	T_L	260	°C

* Measurement made with thermocouple contacting the bottom insulated mounting surface (in a location beneath the die), the device mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.

(1) Proper strike and creepage distance must be provided.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	150	—	Vdc
Collector Cutoff Current (V_{CE} = 150 Vdc, I_B = 0)	I_{CEO}	—	10	μAdc
Collector Cutoff Current (V_{CB} = 150 Vdc, I_E = 0)	I_{CBO}	—	10	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	10	μAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 0.1 Adc, V_{CE} = 2 Vdc) (I_C = 2 Adc, V_{CE} = 2 Vdc) (I_C = 3 Adc, V_{CE} = 2 Vdc) (I_C = 4 Adc, V_{CE} = 2 Vdc)	h_{FE}	40 40 40 20	— — — —	—
DC Current Gain Linearity (V_{CE} from 2 V to 20 V, I_C from 0.1 A to 3 A) (NPN to PNP)	h_{FE}	**Typ** 2 3		
Collector–Emitter Saturation Voltage (I_C = 1 Adc, I_B = 0.1 Adc)	$V_{CE(sat)}$	—	0.5	Vdc
Base–Emitter On Voltage (I_C = 1 Adc, V_{CE} = 2 Vdc)	$V_{BE(on)}$	—	1	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain–Bandwidth Product (2) (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)	f_T	30	—	MHz

NOTES:
1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. $f_T = |h_{fe}| \bullet f_{test}$.

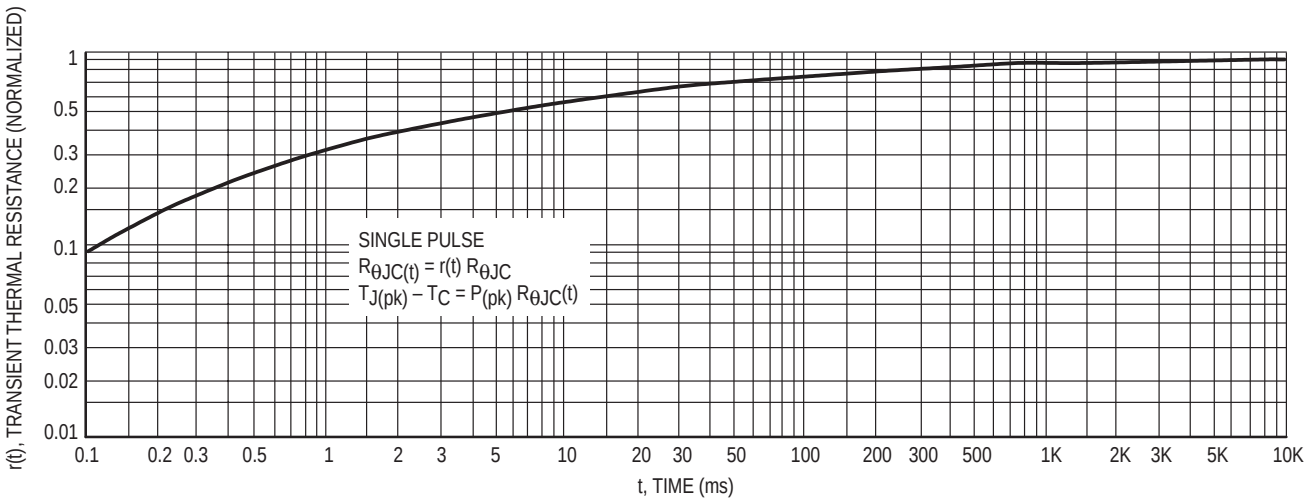


Figure 1. Thermal Response

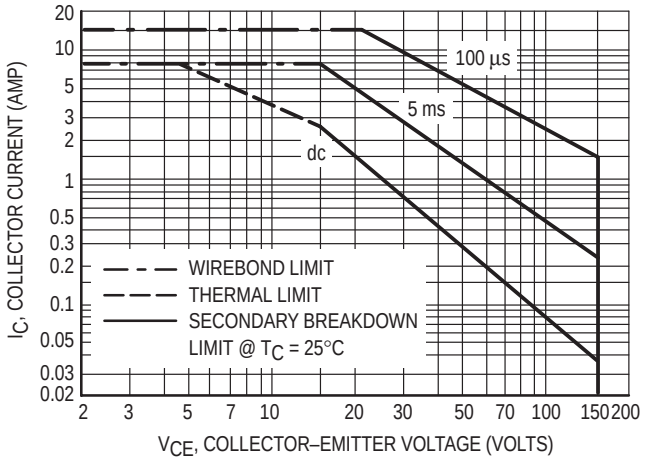


Figure 2. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 2 and 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 1. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

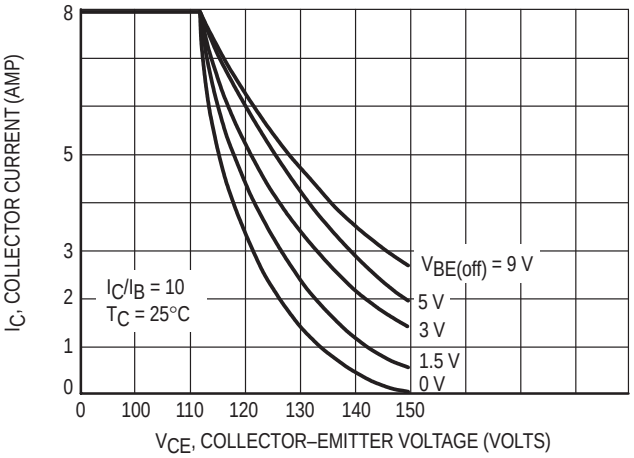


Figure 3. Reverse Bias Switching Safe Operating Area

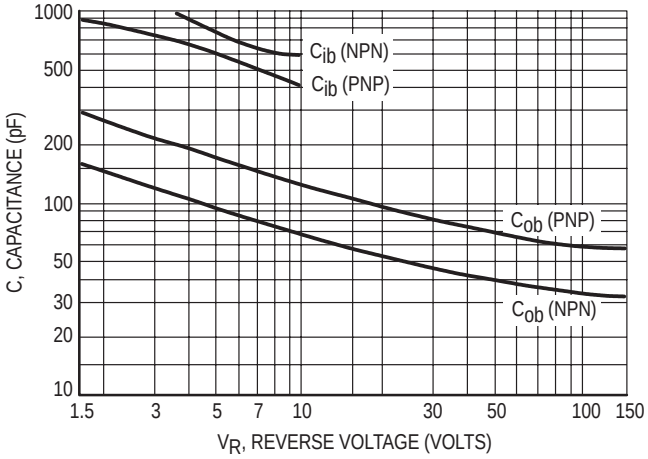


Figure 4. Capacitances

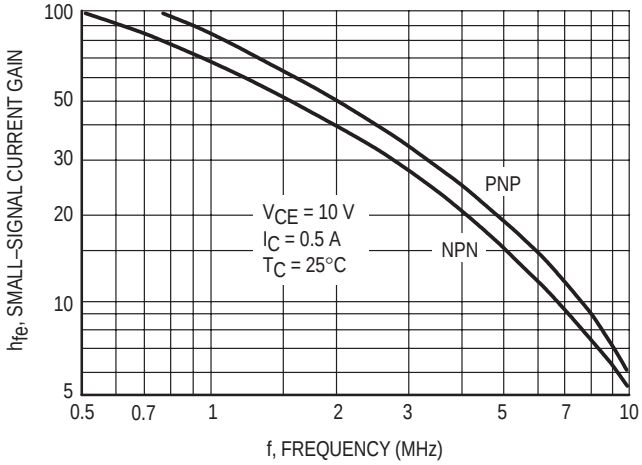


Figure 5. Small–Signal Current Gain

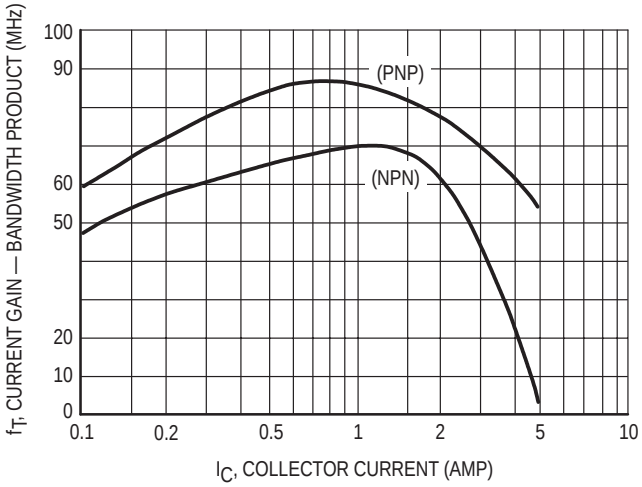


Figure 6. Current Gain — Bandwidth Product

DC CURRENT GAIN

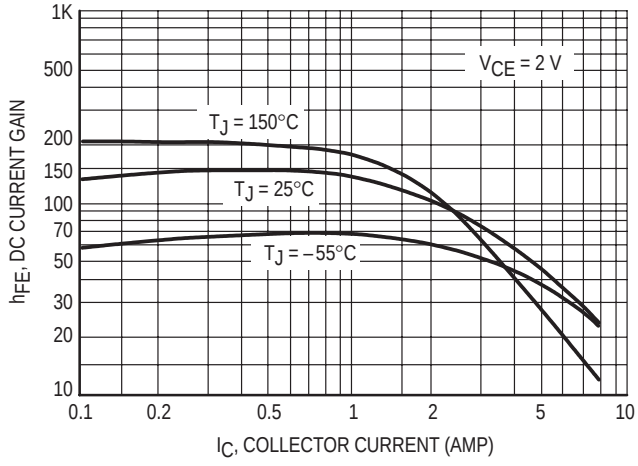


Figure 7a. MJF15030 NPN

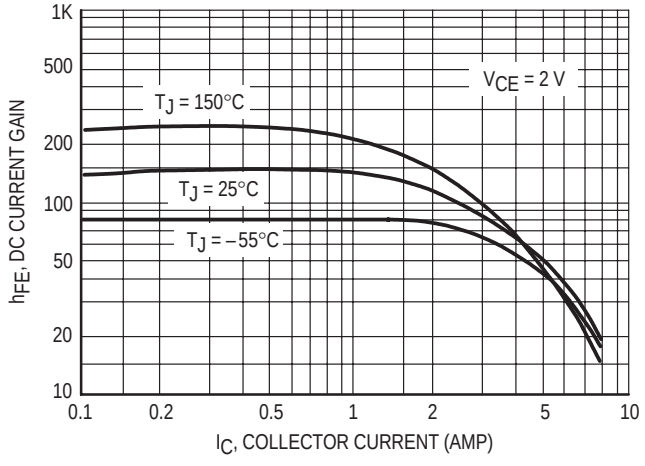


Figure 7b. MJF15031 PNP

"ON" VOLTAGE

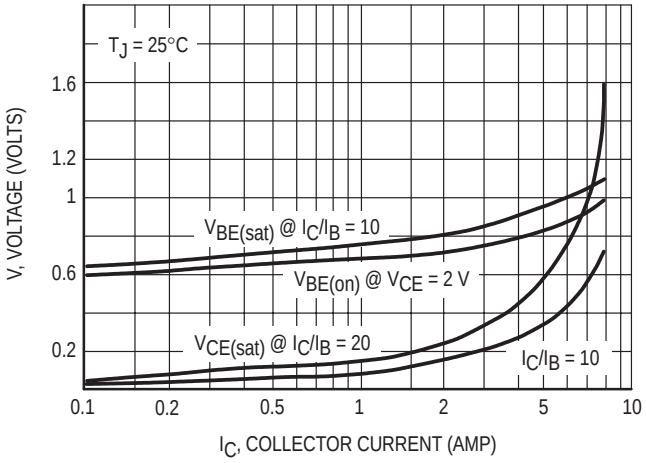


Figure 8a. MJF15030 NPN

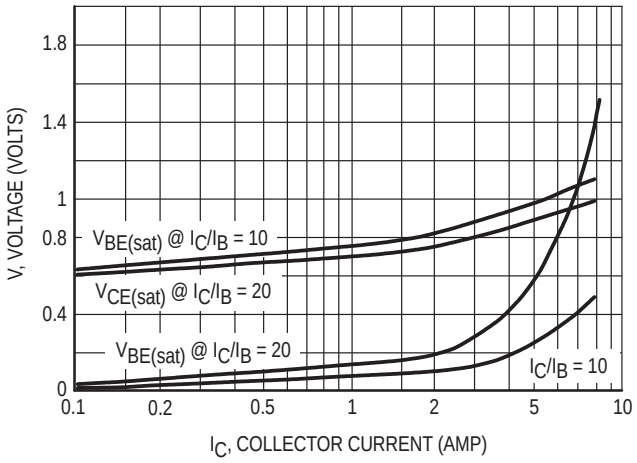


Figure 8b. MJF15031 PNP

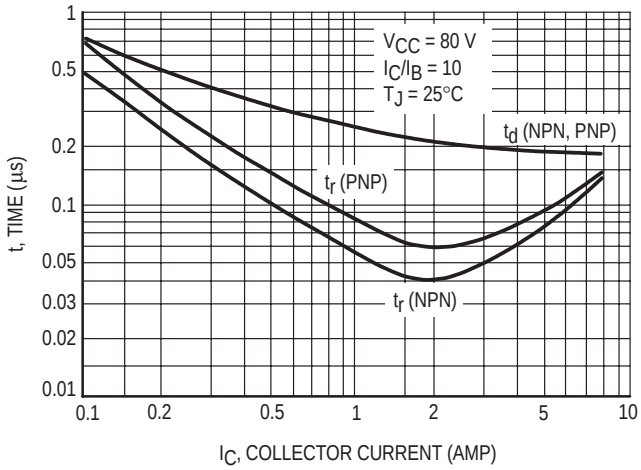


Figure 9. Turn–On Times

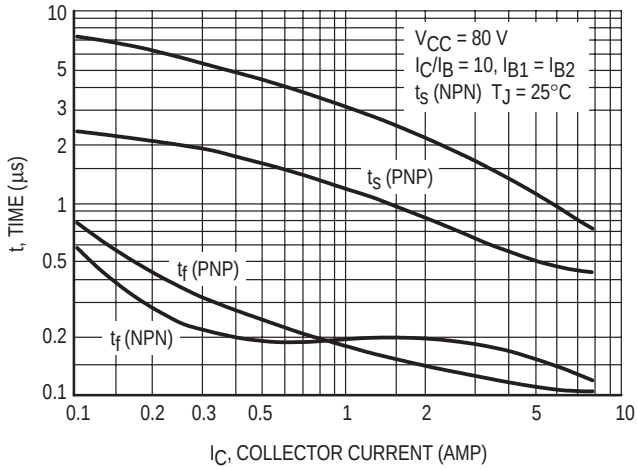


Figure 10. Turn–Off Times

TEST CONDITIONS FOR ISOLATION TESTS*

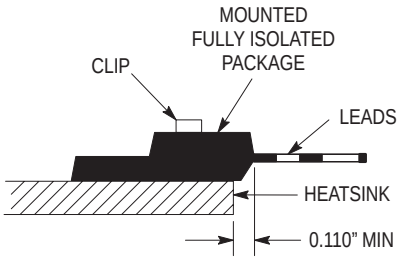


Figure 11. Clip Mounting Position for Isolation Test Number 1

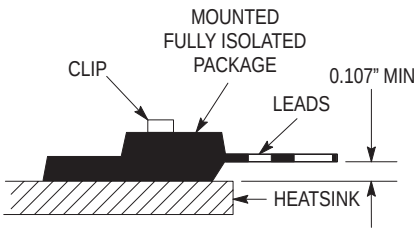


Figure 12. Clip Mounting Position for Isolation Test Number 2

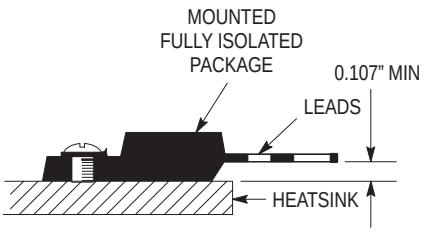


Figure 13. Screw Mounting Position for Isolation Test Number 3

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION

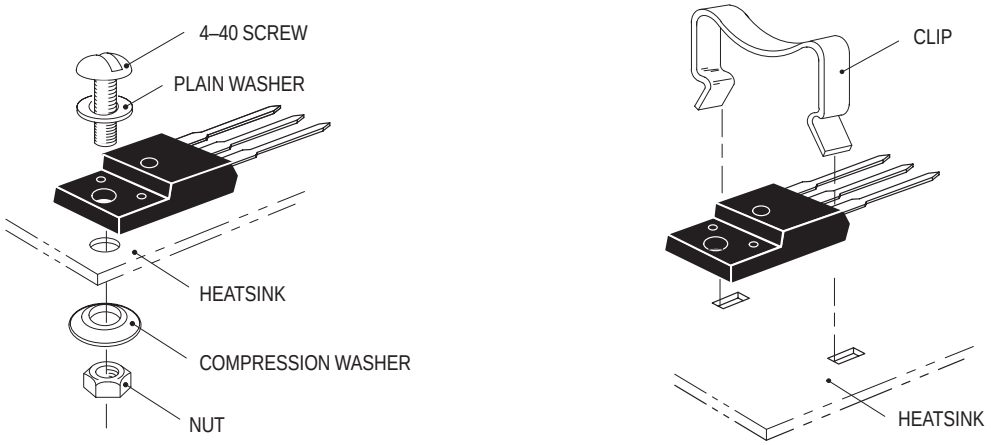


Figure 14. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4–40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4–40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

Designer's™ Data Sheet

SCANSWITCH™

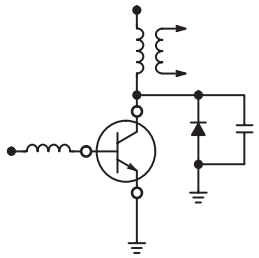
NPN Bipolar Power Deflection Transistor For High and Very High Resolution Monitors

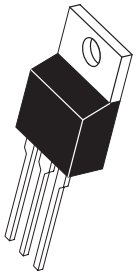
MJE16204

POWER TRANSISTORS
6.0 AMPERES
550 VOLTS — V_{CES}
45 AND 80 WATTS

The MJE16204 is a state–of–the–art SWITCHMODE™ bipolar power transistor. It is specifically designed for use in horizontal deflection circuits for 20 mm diameter neck, high and very resolution, full page, monochrome monitors.

- **550 Volt Collector–Base Breakdown Capability**
- Typical Dynamic Desaturation Specified (New Turn–Off Characteristic)
- Application Specific State–of–the–Art Die Design
- Isolated or Non–Isolated TO–220 Type Packages
- Fast Switching:
  65 ns Inductive Fall Time (Typ)
  680 ns Inductive Storage Time (Typ)
- Low Saturation Voltage:
  0.4 Volts at 3.0 Amps Collector Current and 400 mA Base Drive
- Low Collector–Emitter Leakage Current — 100 μA Max at 550 Volts — V_{CES}
- High Emitter–Base Breakdown Capability For High Voltage Off Drive Circuits — 9.0 Volts (Min)
- Case 221D is UL Recognized at 3500 V_{RMS}: File #E69369





CASE 221A–06
TO–220AB
MJE16204

MAXIMUM RATINGS

Rating	Symbol	MJE16204	Unit
Collector–Emitter Breakdown Voltage	V_{CES}	550	Vdc
Collector–Emitter Sustaining Voltage	$V_{CEO(sus)}$	250	Vdc
Emitter–Base Voltage	V_{EBO}	8.0	Vdc
RMS Isolation Voltage(2) Per Fig. 14 (for 1 sec, T_A = 25°C, Per Fig. 15 Rel. Humidity < 30%) Per Fig. 16	V_{ISOL}	— — —	V
Collector Current — Continuous — Pulsed (1)	I_C I_{CM}	6.0 8.0	Adc
Base Current — Continuous — Pulsed (1)	I_B I_{BM}	2.0 4.0	Adc
Repetitive Emitter–Base Avalanche Energy	$W_{(BER)}$	0.2	mJ
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derated above T_C = 25°C	P_D	80 32 0.64	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C

THERMAL CHARCTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.56	°C/W
Lead Temperature for Soldering Purposes 1/8″ from the case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.
* Measurement made with thermocouple contacting the bottom insulated mounting surface of the package (in a location beneath the die), the device mounted on a heatsink thermal grease applied, and a mounting torque of 6 to 8 in•lbs.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

(REPLACES MJF16204)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector Cutoff Current (V_{CE} = 550 Vdc, V_{BE} = 0 V)	I_{CES}	—	—	100	μAdc
Emitter–Base Leakage (V_{EB} = 8.0 Vdc, I_C = 0)	I_{EBO}	—	—	10	μAdc
Emitter–Base Breakdown Voltage (I_E = 1.0 mA, I_C = 0)	$V_{(BR)EBO}$	8.0	11	—	Vdc
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	325	—	Vdc
ON CHARACTERISTICS (1)					
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 133 mAdc) (I_C = 3.0 Adc, I_B = 400 mAdc)	$V_{CE(sat)}$	— —	0.25 0.4	0.6 1.0	Vdc
Base–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 400 mAdc)	$V_{BE(sat)}$	—	0.9	1.5	Vdc
DC Current Gain (ICE = 6.0 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	8.0	14	20	—
DYNAMIC CHARACTERISTICS					
Dynamic Desaturation Interval (I_C = 3.0 A, I_{B1} = 400 mA)	t_{ds}	—	50	—	ns
Output Capacitance (V_{CE} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	—	90	150	pF
Gain Bandwidth Product (V_{CE} = 10 Vdc, I_C = 1.0 A, f_{test} = 1.0 MHz)	f_T	10	—	—	MHz
Emitter–Base Turn–Off Energy ($EB_{(avalanche)}$ = 500 ns, R_{BE} = 22 Ω)	$EB_{(off)}$	—	6.6	—	μJ
Collector–Heatsink Capacitance (Mounted on a 1″ x 2″ x 1/16″ Copper Heatsink, V_{CE} = 0, f_{test} = 100 kHz)	$C_{c–hs}$	—	3.0	—	pF
SWITCHING CHARACTERISTICS					
Inductive Load (Table 2) (I_C = 3.0 A, I_B = 400 mA) Storage Fall Time	 t_{sv} t_{fi}	 — —	 680 65	 1500 150	ns

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

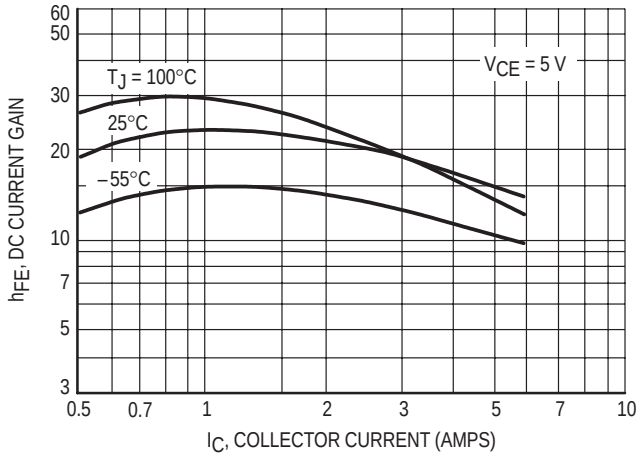


Figure 1. Typical DC Current Gain

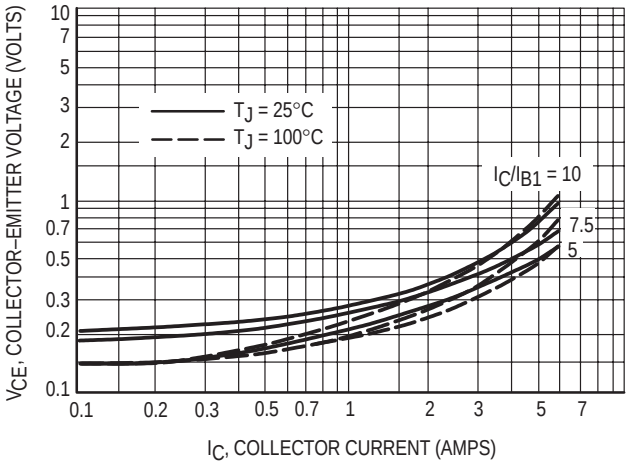


Figure 2. Typical Collector–Emitter Saturation Voltage

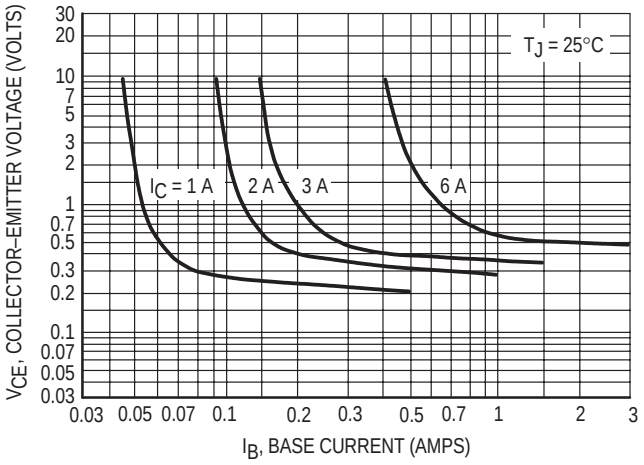


Figure 3. Typical Collector–Emitter Saturation Region

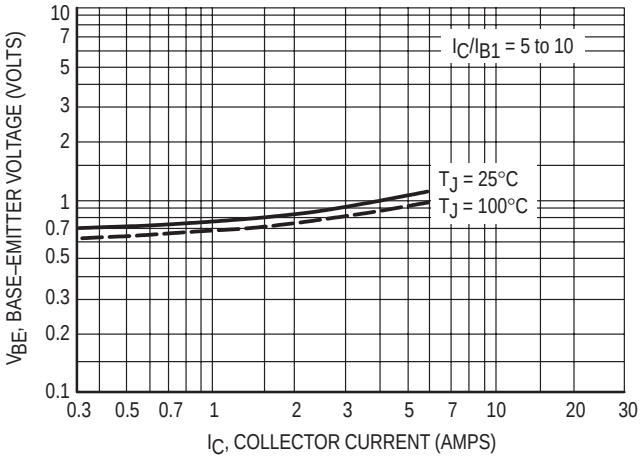


Figure 4. Typical Base–Emitter Saturation Voltage

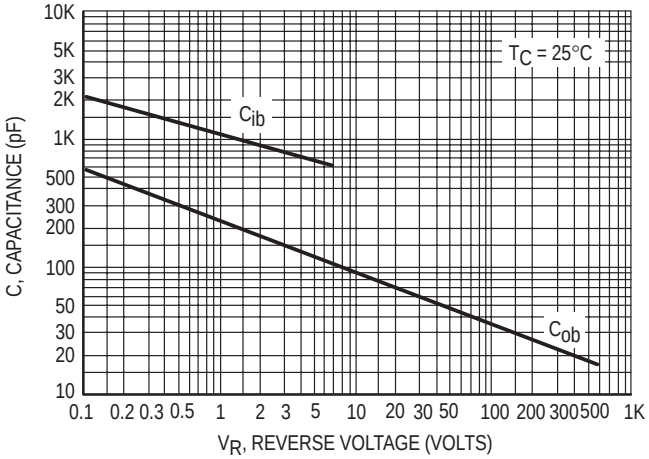


Figure 5. Typical Capacitance

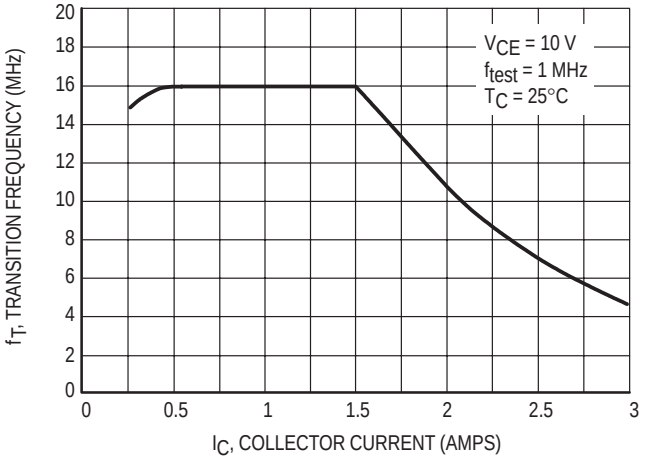


Figure 6. Typical Transition Frequency

SAFE OPERATING AREA

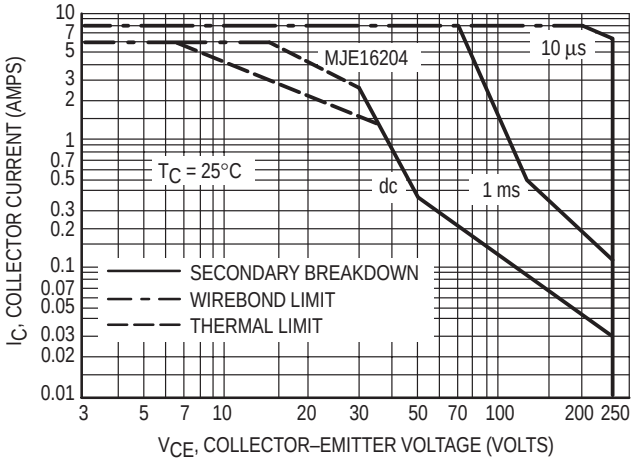


Figure 7. Maximum Forward Biased Safe Operating Area

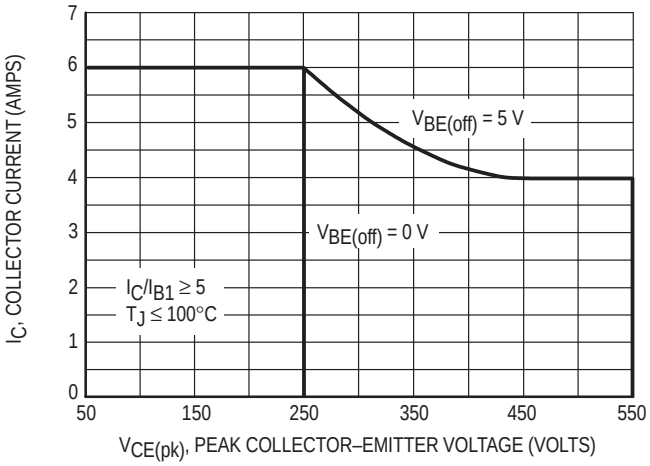


Figure 8. Maximum Reverse Biased Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

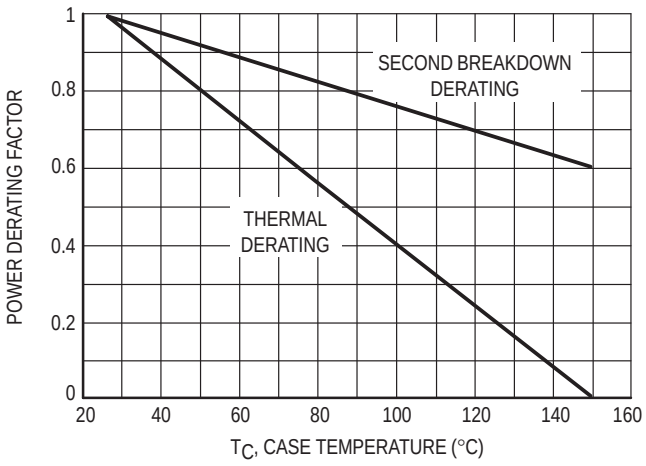


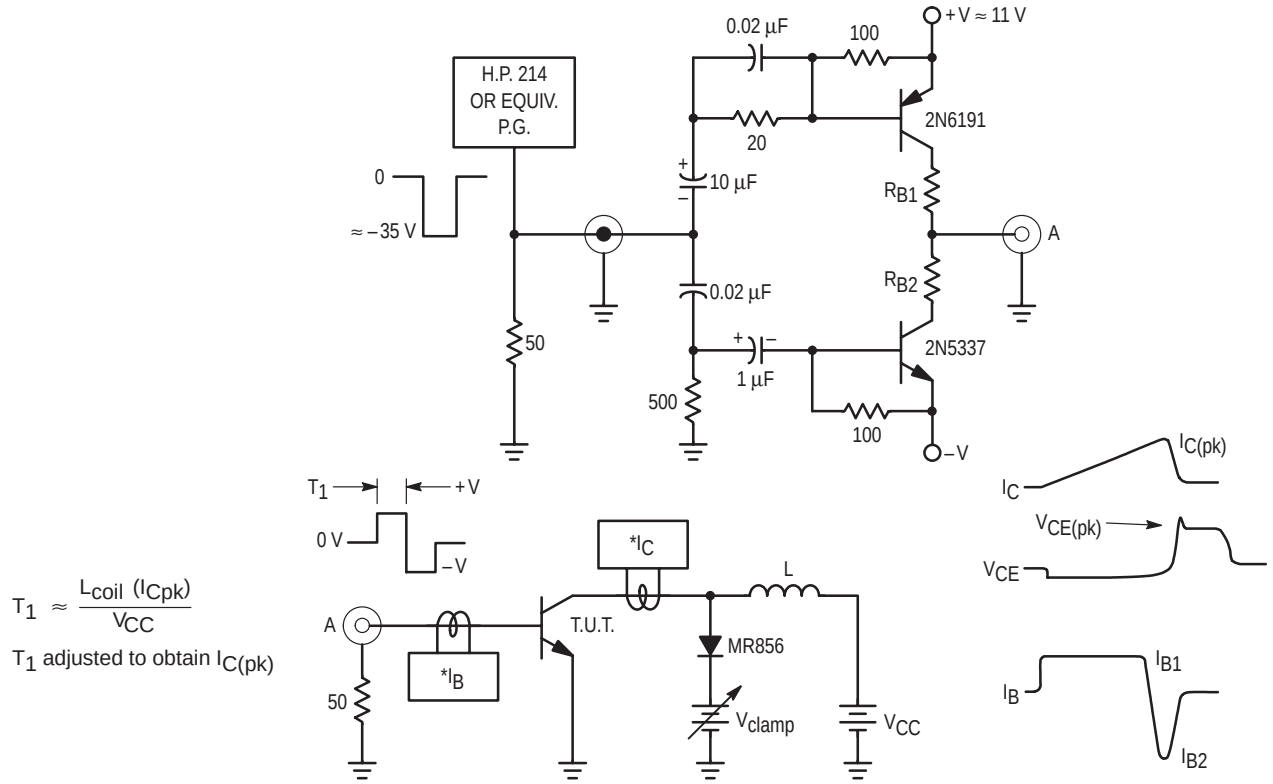
Figure 9. Power Derating

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc.

The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage–current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 8 gives the RBSOA characteristics.

Table 1. RBSOA/$V_{(BR)CEO(sus)}$ Test Circuit



$T_1 \approx \frac{L_{coil}\ (I_{Cpk})}{V_{CC}}$

T_1 adjusted to obtain $I_{C(pk)}$

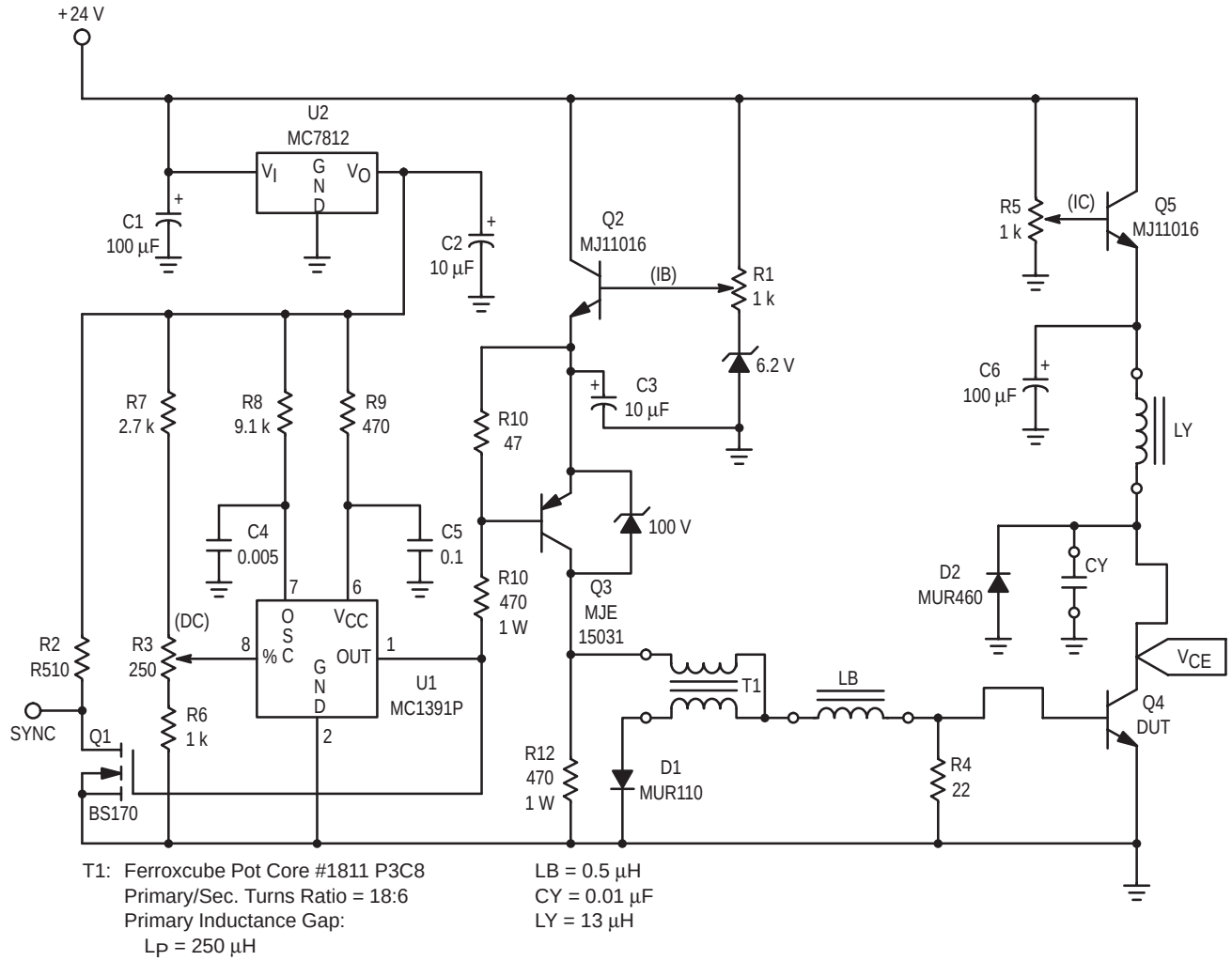
$V_{(BR)CEO}$
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts

*Tektronix
P–6042 or
Equivalent

RBSOA
L = 200 µH
$R_{B2} = 0$
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

Table 2. High Resolution Deflection Application Simulator



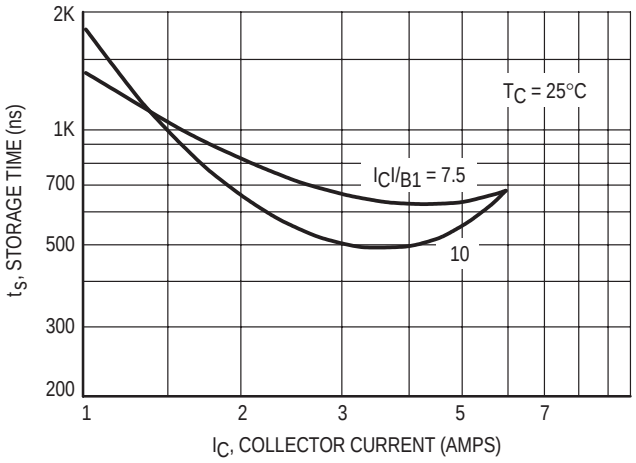


Figure 10. Typical Collector Current Storage Time in Deflection Circuit Simulator

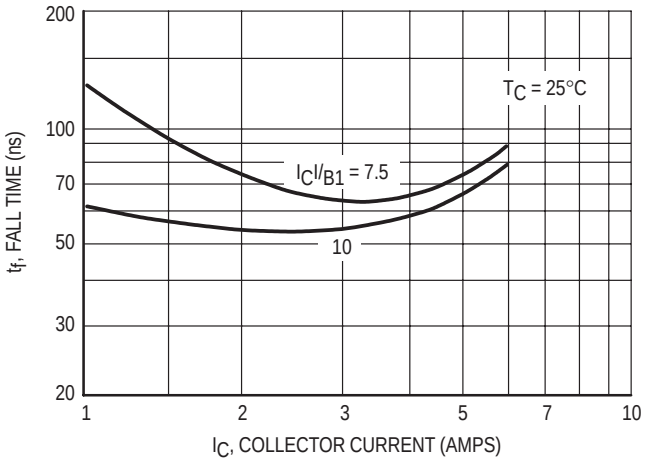


Figure 11. Typical Collector Current Fall Time in Deflection Circuit Simulator

DYNAMIC DESATURATIION

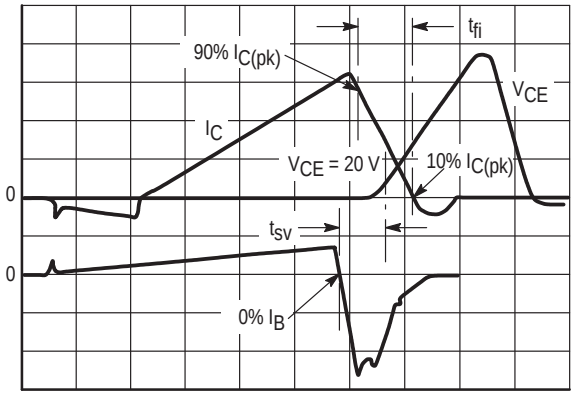


Figure 12. Deflection Simulator Switching Waveforms From Circuit in Table 2

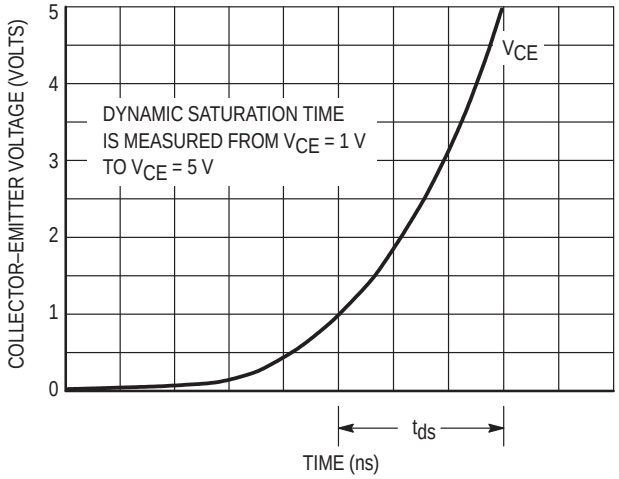


Figure 13. Definition of Dynamic Saturation Measurement

The SCANSWITCH series of bipolar power transistors are specifically designed to meet the unique requirements of horizontal deflection circuits in computer monitor applications. Historically, deflection transistor design was focused on minimizing collector current fall time. While fall time is a valid figure of merit, a more important indicator of circuit performance as scan rates are increased is a new characteristic, “dynamic desaturation.” In order to assure a linear collector current ramp, the output transistor must remain in hard saturation during storage time and exhibit a rapid turn–off transition. A sluggish transition results in serious consequences. As the saturation voltage of the output transistor increases, the voltage across the yoke drops. Roll off in the collector current ramp results in improper beam deflection and distortion of the image at the right edge of the screen. Design changes have been made in the structure of the SCANSWITCH series of devices which minimize the dynamic desaturation interval. Dynamic desaturation has been defined in terms of the time required for the V_{CE} to rise from 1.0 to 5.0 volts (Figures 12 and 13) and typical performance at optimized drive conditions has been specified. Optimization of device structure results in a linear collector current ramp, excellent turn–off switching performance, and significantly lower overall power dissipation.

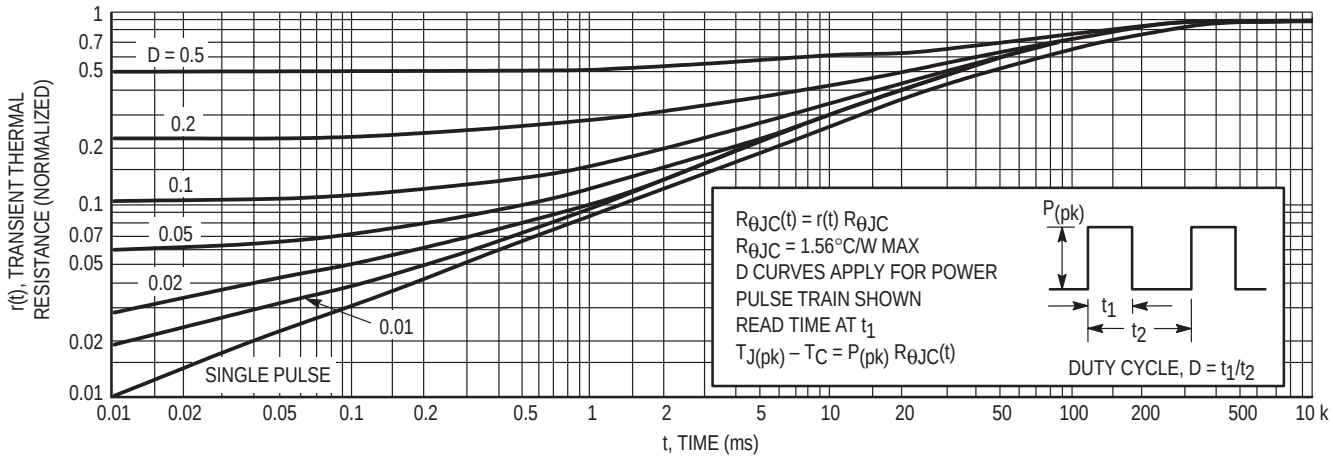


Figure 14. Typical Thermal Response for MJE16204

Darlington Complementary Silicon Power Transistors

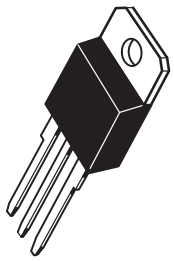
. . . designed for general–purpose amplifier and low–speed switching motor control applications.

- Similar to the Popular NPN 2N6282, 2N6283, 2N6284 and the PNP 2N6285, 2N6286, 2N6287
- Rugged RBSOA Characteristics
- Monolithic Construction with Built–in Collector–Emitter Diode

NPN
MJH6282
MJH6283*
MJH6284*
PNP
MJH6285
MJH6286*
MJH6287*

***Motorola Preferred Device**

DARLINGTON
20 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
60, 80, 100 VOLTS
160 WATTS



CASE 340D–01

MAXIMUM RATINGS

Rating	Symbol	MJH6282 MJH6285	MJH6283 MJH6286	MJH6284 MJH6287	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	20 40			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	160 1.28			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.78	°C/W

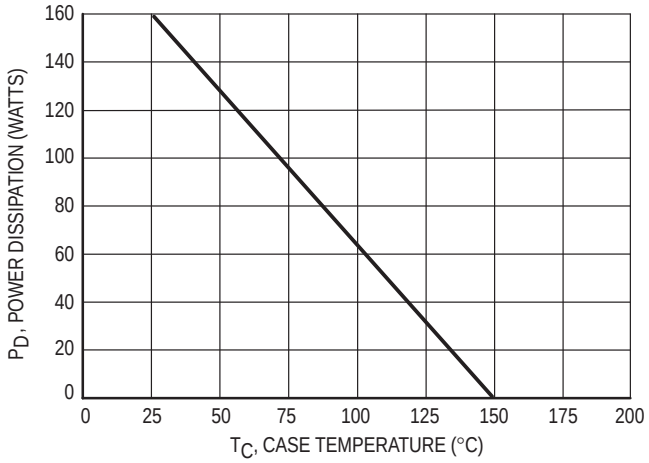


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

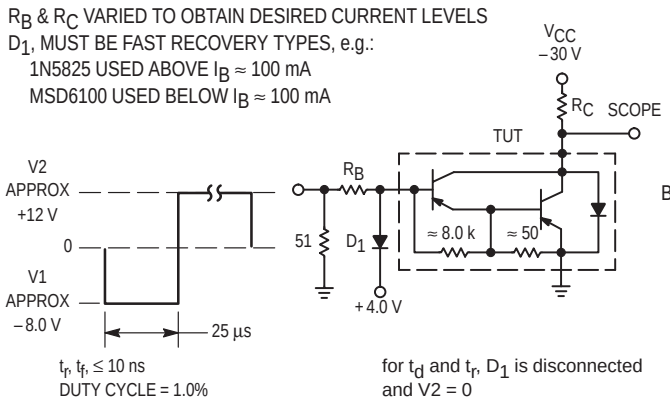
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 0.1 Adc, I_B = 0)	MJH6282, MJH6285 MJH6283, MJH6286 MJH6284, MJH6287	$V_{CEO(sus)}$	 60 80 100	 — — —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	 MJH6282, MJH6285 MJH6283, MJH6286 MJH6284, MJH6287	I_{CEO}	 — — —	 1.0 1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	 — —	 0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc) (I_C = 20 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	750 100	18,000 —	—
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 40 mAdc) (I_C = 20 Adc, I_B = 200 mAdc)		$V_{CE(sat)}$	— —	2.0 3.0	Vdc
Base–Emitter On Voltage (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
Base–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 200 mAdc)		$V_{BE(sat)}$	—	4.0	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain Bandwidth Product (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		f_T	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	 MJH6282, 83, 84 MJH6285, 86, 87	C_{ob}	 — —	 400 600	pF
Small–Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	—	—

SWITCHING CHARACTERISTICS

Resistive Load		Symbol	Typical NPN	Typical PNP	Unit
Delay Time	V_{CC} = 30 Vdc, I_C = 10 Adc I_{B1} = I_{B2} = 100 mA Duty Cycle = 1.0%	t_d	0.1	0.1	µs
Rise Time		t_r	0.3	0.3	
Storage Time		t_s	1.0	1.0	
Fall Time		t_f	3.5	2.0	

(1) Pulse test: Pulse Width = 300 µs, Duty Cycle = 2.0%.



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

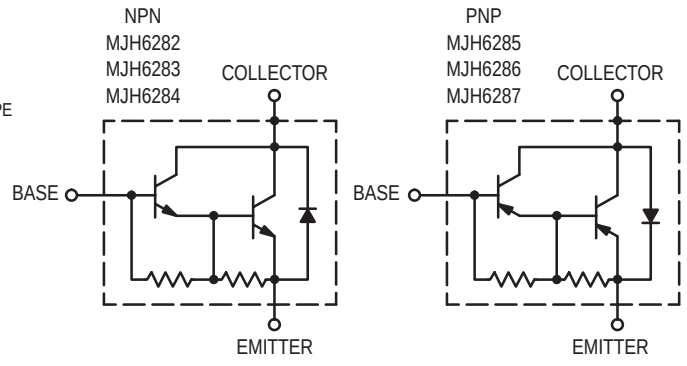


Figure 3. Darlington Schematic

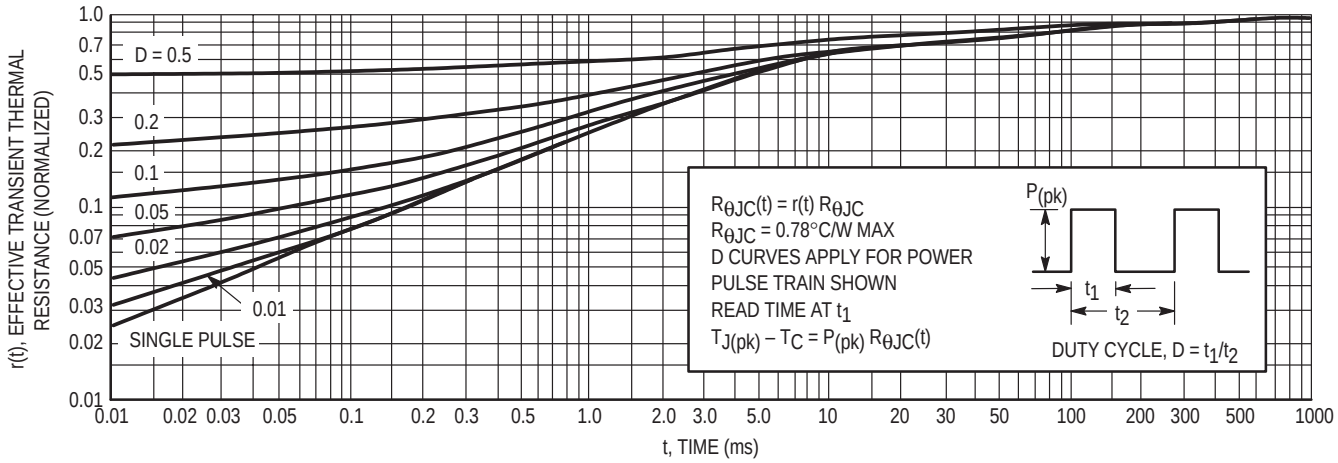


Figure 4. Thermal Response

FBSOA, FORWARD BIAS SAFE OPERATING AREA

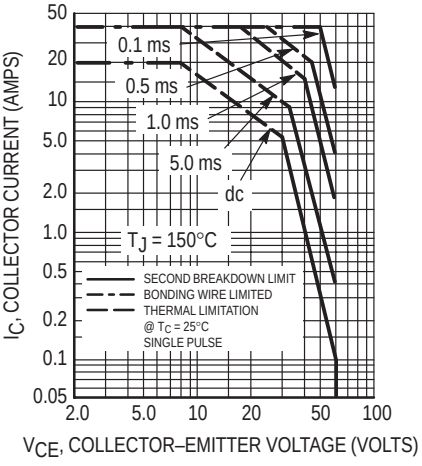


Figure 5. MJH6282, MJH6285

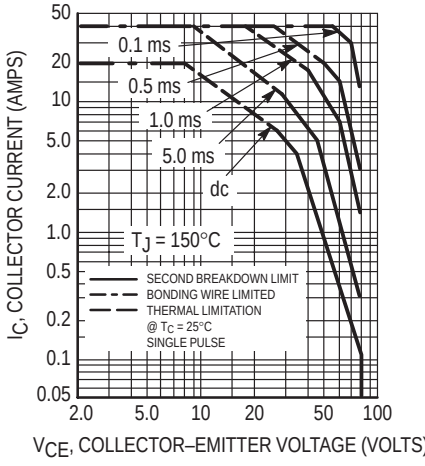


Figure 6. MJH6283, MJH6286

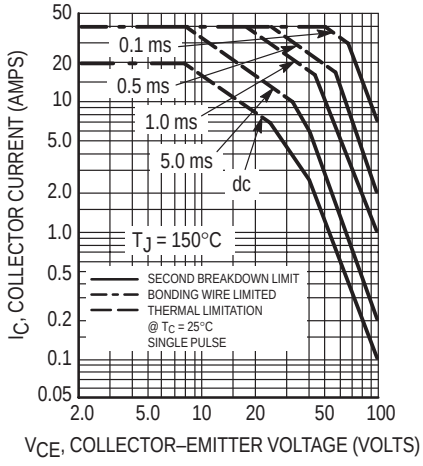


Figure 7. MJH6284, MJH6287

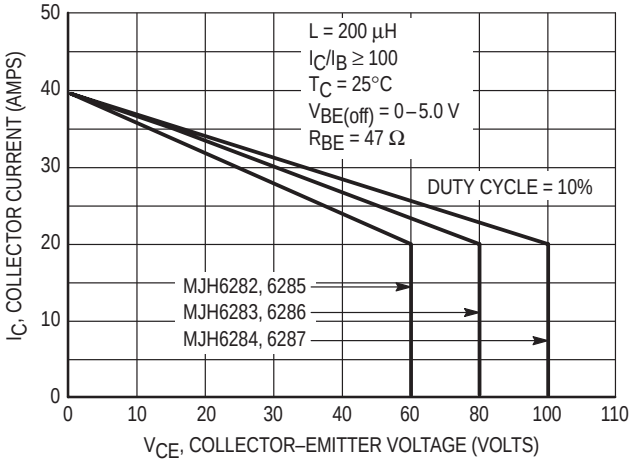


Figure 8. Maximum RBSOA, Reverse Bias Safe Operating Area

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5, 6 and 7 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

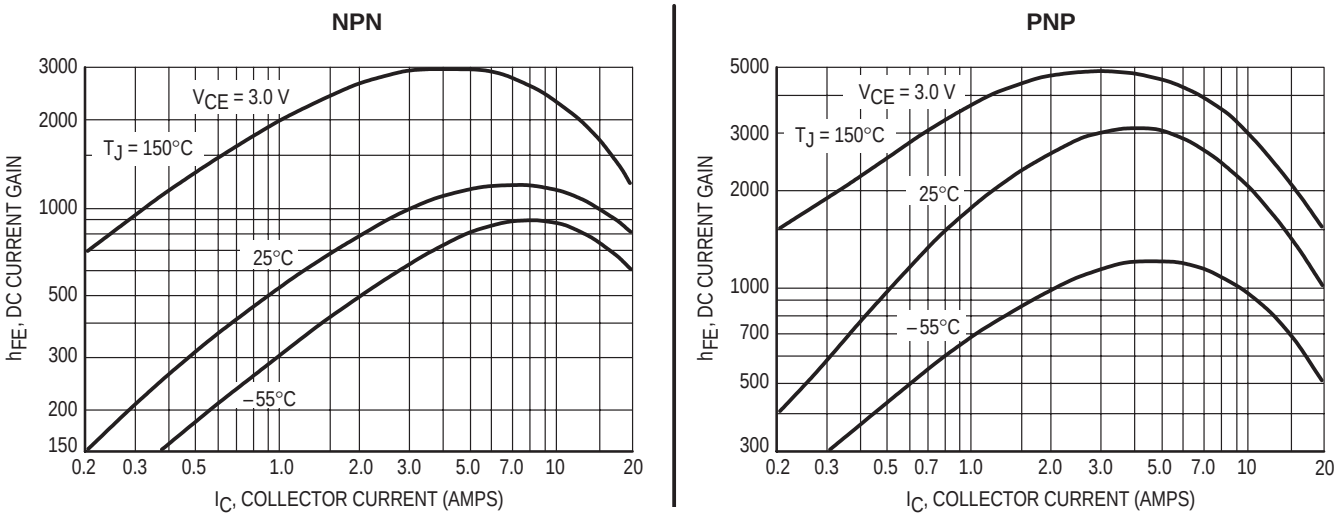


Figure 9. DC Current Gain

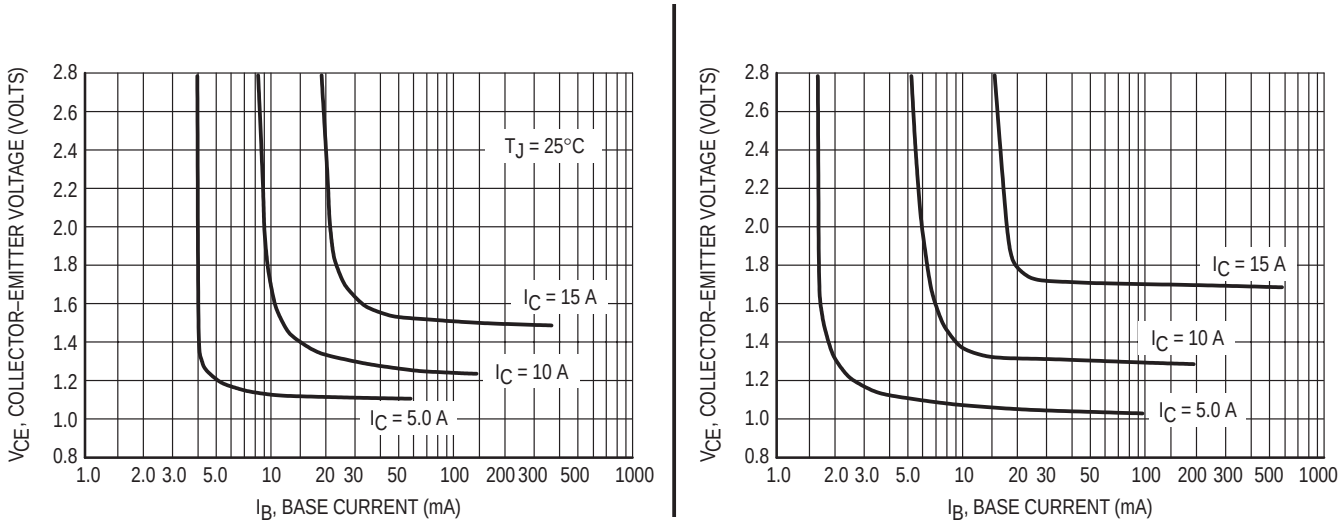


Figure 10. Collector Saturation Region

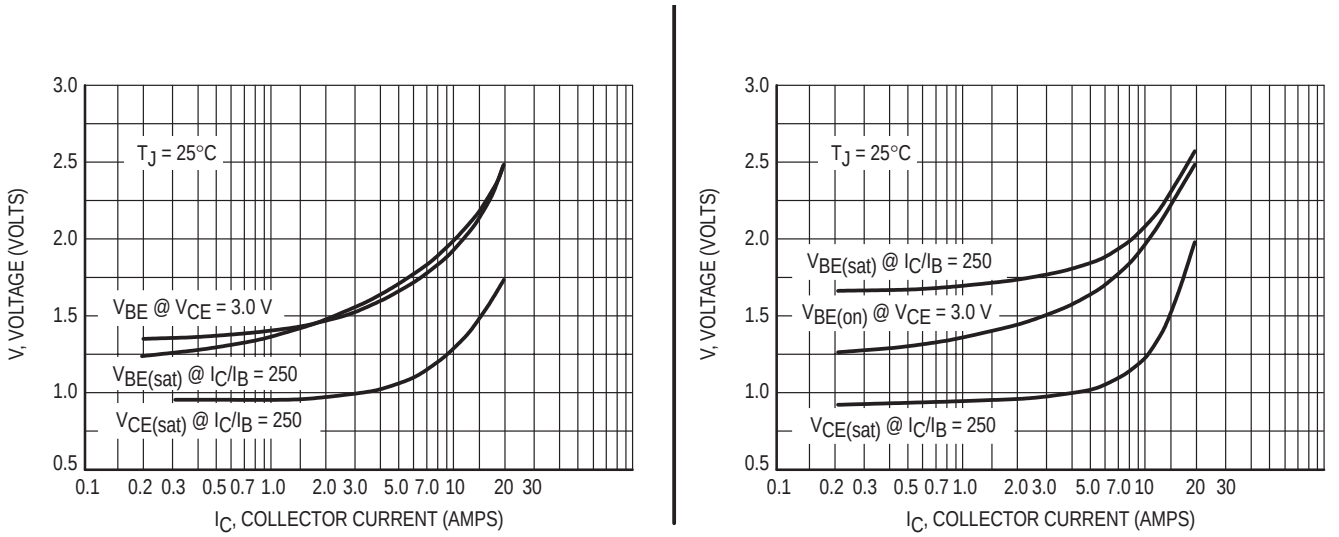


Figure 11. “On” Voltages

MJH10012
(See MJ10012)

Complementary Darlington Silicon Power Transistors

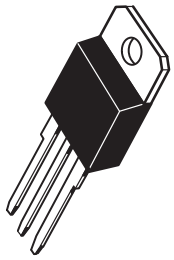
. . . designed for use as general purpose amplifiers, low frequency switching and motor control applications.

- High DC Current Gain @ 10 Adc — h_{FE} = 400 Min (All Types)
- Collector–Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 150 Vdc (Min) — MJH11018, 17
  = 200 Vdc (Min) — MJH11020, 19
  = 250 Vdc (Min) — MJH11022, 21
- Low Collector–Emitter Saturation Voltage
  $V_{CE(sat)}$ = 1.2 V (Typ) @ I_C = 5.0 A
  = 1.8 V (Typ) @ I_C = 10 A
- Monolithic Construction

PNP
MJH11017*
MJH11019*
MJH11021*
NPN
MJH11018*
MJH11020*
MJH11022*

*Motorola Preferred Device

15 AMPERE
DARLINGTON
COMPLEMENTARY SILICON
POWER TRANSISTORS
150, 200, 250 VOLTS
150 WATTS



CASE 340D–01

MAXIMUM RATINGS

Rating	Symbol	MJH 11018 11017	MJH 11020 11019	MJH 11022 11021	Unit
Collector–Emitter Voltage	V_{CEO}	150	200	250	Vdc
Collector–Base Voltage	V_{CB}	150	200	250	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous — Peak (1)	I_C	15 30			Adc
Base Current	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C Derate Above 25°C	P_D	150 1.2			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance. Junction to Case	$R_{\theta JC}$	0.83	°C/W

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

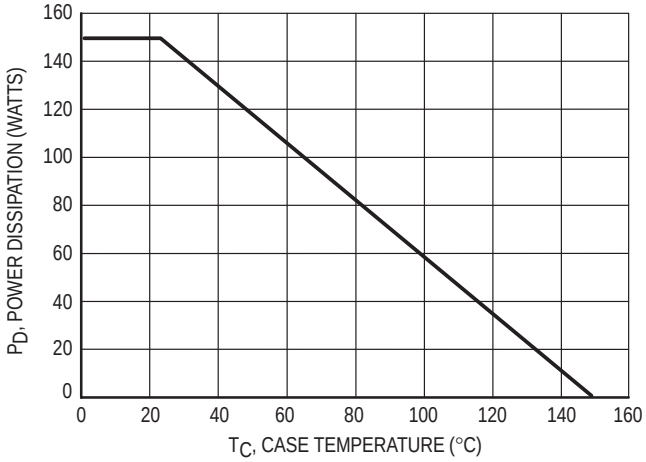


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 0.1 Adc, I_B = 0)	MJH11017, MJH11018	$V_{CEO(sus)}$	150	—	Vdc
	MJH11019, MJH11020		200	—	
	MJH11021, MJH11022		250	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 75 Vdc, I_B = 0)	MJH11017, MJH11018		—	1.0	
(V_{CE} = 100 Vdc, I_B = 0)	MJH11019, MJH11020		—	1.0	
(V_{CE} = 125 Vdc, I_B = 0)	MJH11021, MJH11022		—	1.0	
Collector Cutoff Current		I_{CEV}			mAdc
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc)			—	0.5	
(V_{CE} = Rated V_{CB}, $V_{BE(off)}$ = 1.5 Vdc, T_J = 150°C)			—	5.0	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 10 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	400	15,000	—
(I_C = 15 Adc, V_{CE} = 5.0 Vdc)			100	—	
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 100 mA)		$V_{CE(sat)}$	—	2.5	Vdc
(I_C = 15 Adc, I_B = 150 mA)			—	4.0	
Base–Emitter On Voltage (I_C = 10 A, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
Base–Emitter Saturation Voltage (I_C = 15 Adc, I_B = 150 mA)		$V_{BE(sat)}$	—	3.8	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain Bandwidth Product (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		f_T	3.0	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	MJH11018, MJH11020, MJH11022	C_{ob}	—	400	pF
	MJH11017, MJH11019, MJH11021		—	600	
Small–Signal Current Gain (I_C = 10 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	75	—	—

SWITCHING CHARACTERISTICS

Characteristic		Symbol	Typical NPN	Typical PNP	Unit
Delay Time	(V_{CC} = 100 V, I_C = 10 A, I_B = 100 mA $V_{BE(off)}$ = 5.0 V) (See Figure 2)	t_d	150	75	ns
Rise Time		t_r	1.2	0.5	µs
Storage Time		t_s	4.4	2.7	µs
Fall Time		t_f	2.5	2.5	µs

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤ 2.0%.

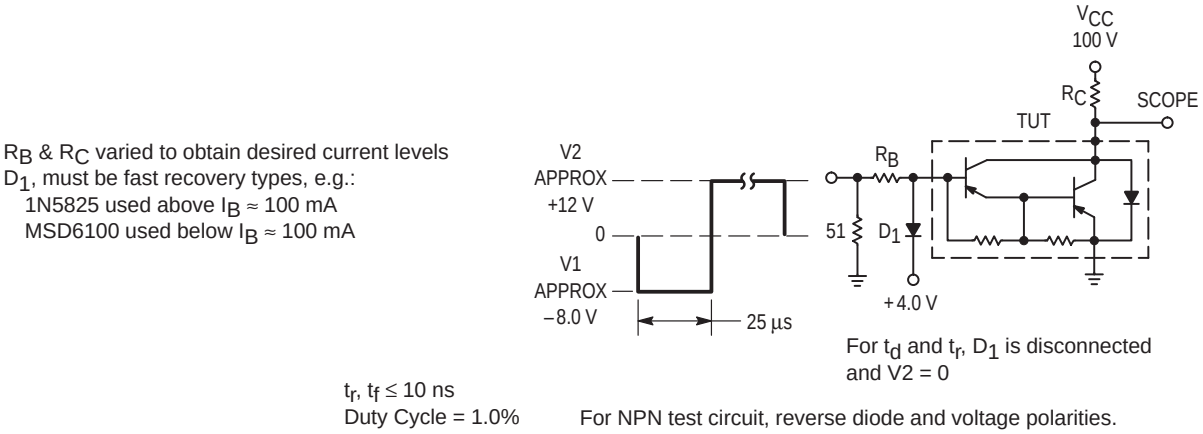


Figure 2. Switching Times Test Circuit

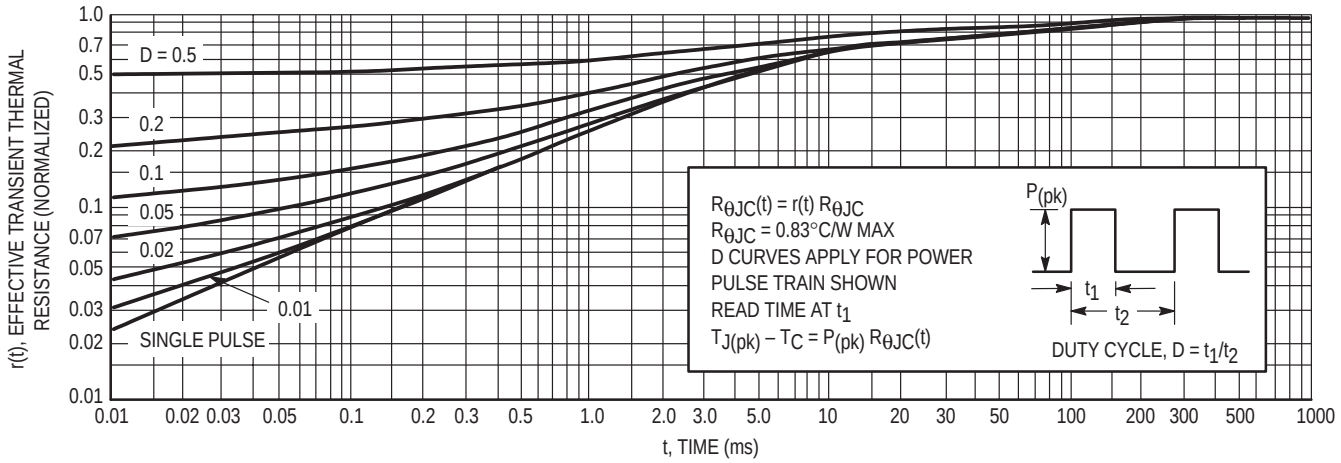


Figure 3. Thermal Response

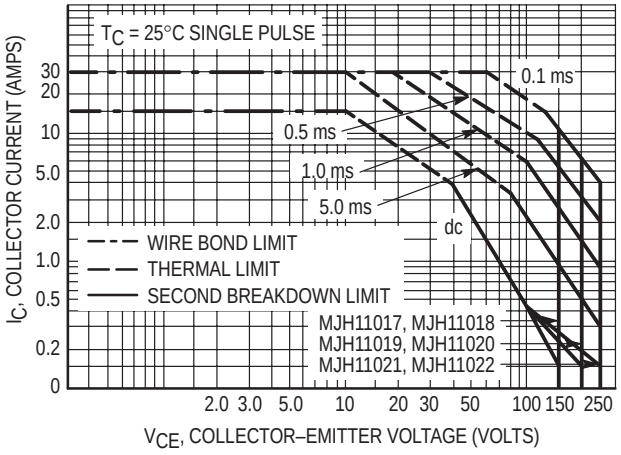


Figure 4. Maximum Rated Forward Bias Safe Operating Area (FBSOA)

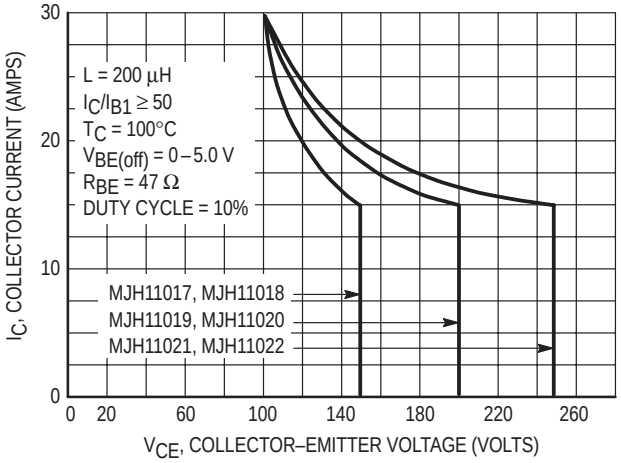


Figure 5. Maximum Rated Reverse Bias Safe Operating Area (RBSOA)

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives RBSOA characteristics.

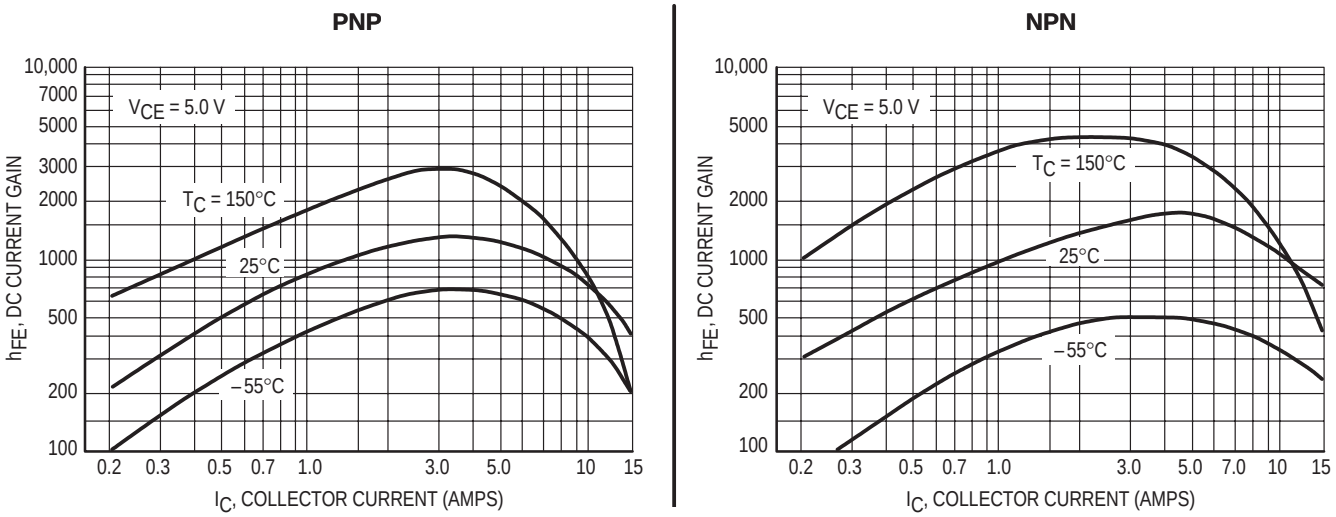


Figure 6. DC Current Gain

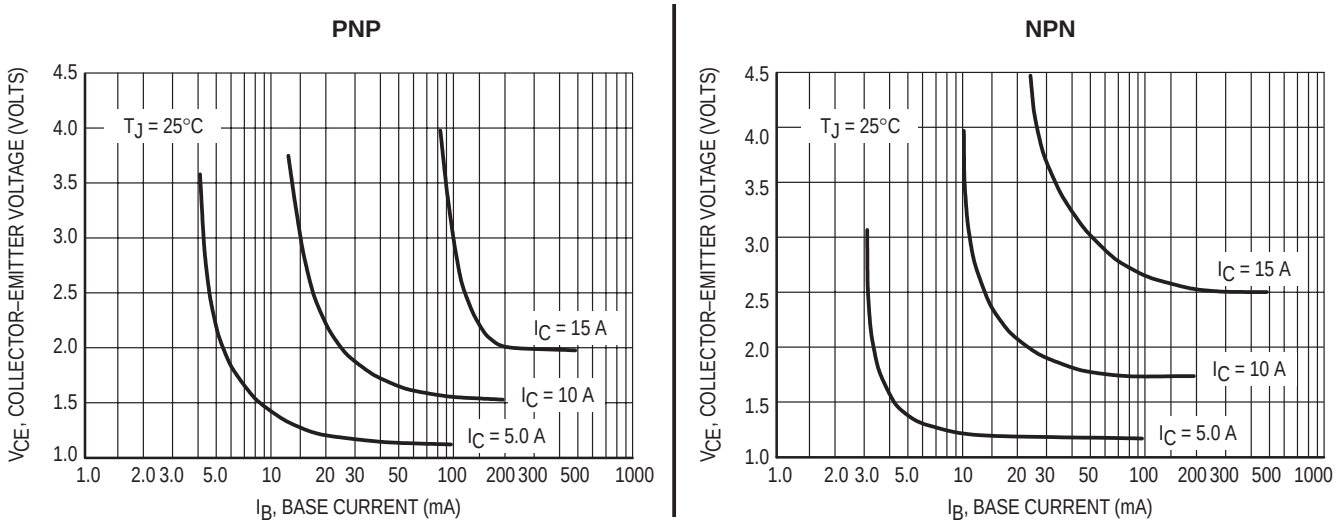


Figure 7. Collector Saturation Region

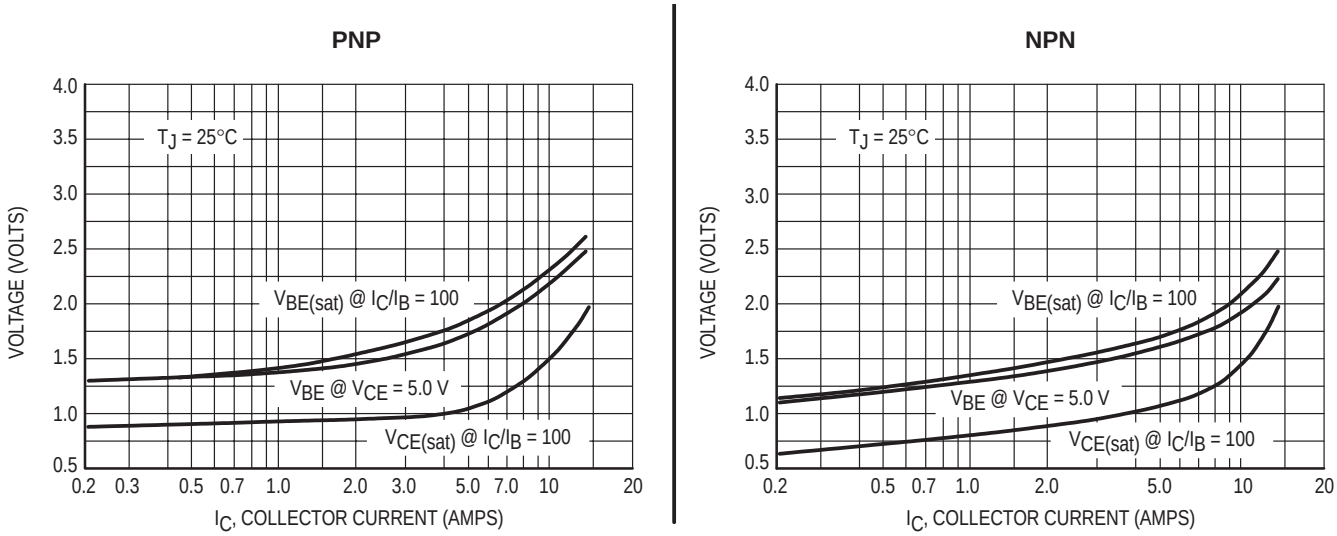


Figure 8. “On” Voltages

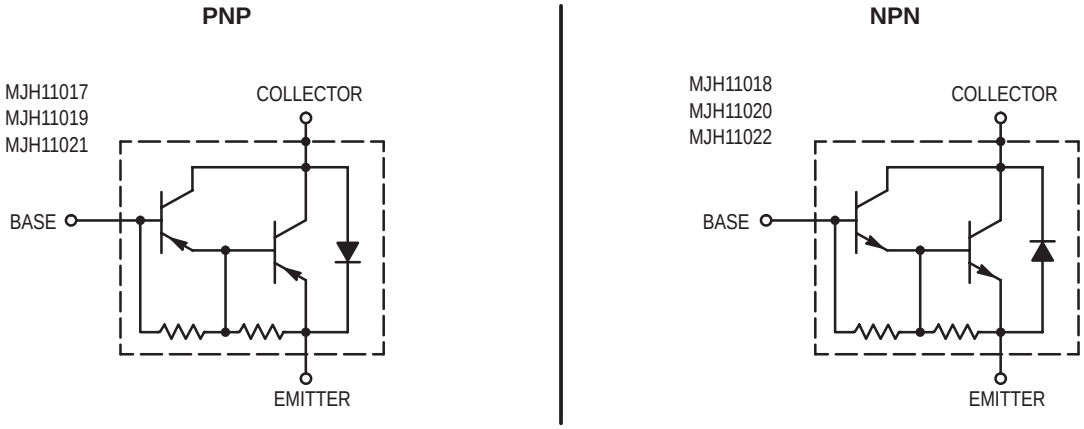


Figure 9. Darlington Schematic

MJH16006A

Designer's™ Data Sheet

NPN Silicon Power Transistor

1 kV SWITCHMODE Series

POWER TRANSISTORS
8 AMPERES
500 VOLTS
150 WATTS

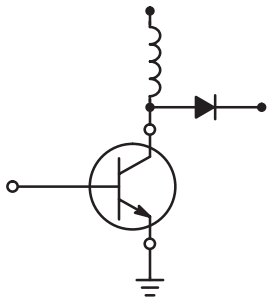
These transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated switchmode applications.

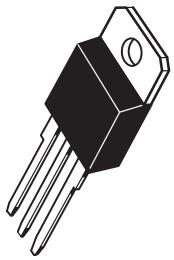
Typical Applications:

- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

Features:

- Collector–Emitter Voltage — V_{CEV} = 1000 Vdc
- Fast Turn–Off Times
  - 80 ns Inductive Fall Time — 100°C (Typ)
  - 120 ns Inductive Crossover Time — 100°C (Typ)
  - 800 ns Inductive Storage Time — 100°C (Typ)
- 100°C Performance Specified for:
  - Reverse–Biased SOA with Inductive Load
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents
- Extended FBSOA Rating Using Ultra–fast Rectifiers
- Extremely High RBSOA Capability





CASE 340D–01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	500	Vdc
Collector–Emitter Voltage	V_{CEV}	1000	Vdc
Emitter–Base Voltage	V_{EB}	6	Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	8 16	Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	6 12	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above T_C = 25°C	P_D	125 50 1	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS(1)							
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)			$V_{CEO(sus)}$	500	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			I_{CEV}	 — —	 0.003 0.020	 0.15 1.0	mAdc
Collector Cutoff Current (V_{CE} = 1000 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	0.020	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)			I_{EBO}	—	0.005	0.15	mAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$	See Figure 14a or 14b			
Clamped Inductive SOA with Base Reverse Biased			RBSOA	See Figure 15			
ON CHARACTERISTICS(1)							
Collector–Emitter Saturation Voltage (I_C = 3 Adc, I_B = 0.6 Adc) (I_C = 5 Adc, I_B = 1 Adc) (I_C = 5 Adc, I_B = 1 Adc, T_C = 100°C)			$V_{CE(sat)}$	 — — —	 0.35 0.50 0.60	 0.7 1 1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc) (I_C = 5 Adc, I_B = 1 Adc, T_C = 100°C)			$V_{BE(sat)}$	 — —	 1 1	 1.5 1.5	Vdc
DC Current Gain (I_C = 8 Adc, V_{CE} = 5 Vdc)			h_{FE}	5	8	—	—
DYNAMIC CHARACTERISTICS							
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 kHz)			C_{ob}	—	—	350	pF
SWITCHING CHARACTERISTICS							
Inductive Load (Table 1)							
Storage Time	(I_C = 5 Adc, I_{B1} = 0.66 Adc, $V_{BE(off)}$ = 5 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	800	2000	ns
Fall Time			t_{fi}	—	80	200	
Crossover Time			t_c	—	120	300	
Storage Time		(T_J = 150°C)	t_{sv}	—	1000	—	
Fall Time			t_{fi}	—	90	—	
Crossover Time			t_c	—	150	—	
Resistive Load (Table 2)							
Delay Time	(I_C = 5 Adc, V_{CC} = 250 Vdc, I_{B1} = 0.66 Adc, PW = 30 µs, Duty Cycle ≤ 2%)	(I_{B2} = 1.3 Adc, R_{B1} = R_{B2} = 4 Ω)	t_d	—	25	100	ns
Rise Time			t_r	—	400	700	
Storage Time			t_s	—	1400	3000	
Fall Time			t_f	—	175	400	
Storage Time		($V_{BE(off)}$ = 5 Vdc)	t_s	—	475	—	
Fall Time			t_f	—	100	—	

(1) Pulse Test: PW = 300 µs, Duty Cycle ≤ 2%.

TYPICAL STATIC CHARACTERISTICS

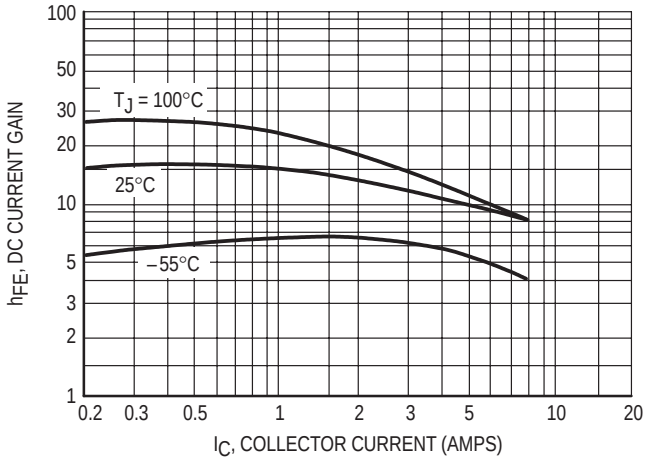


Figure 1. DC Current Gain

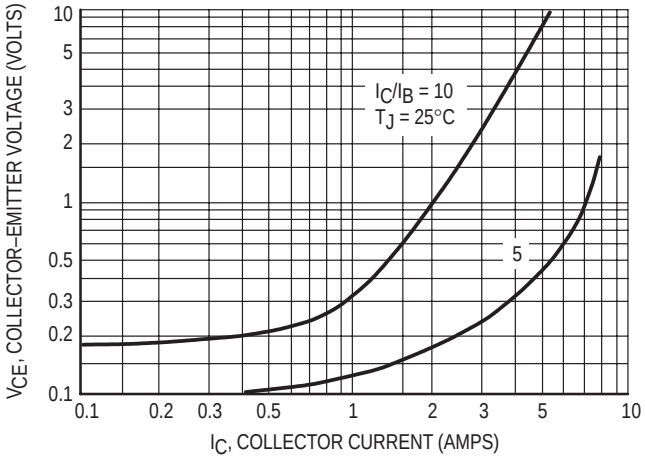


Figure 2. Collector–Emitter Saturation Region

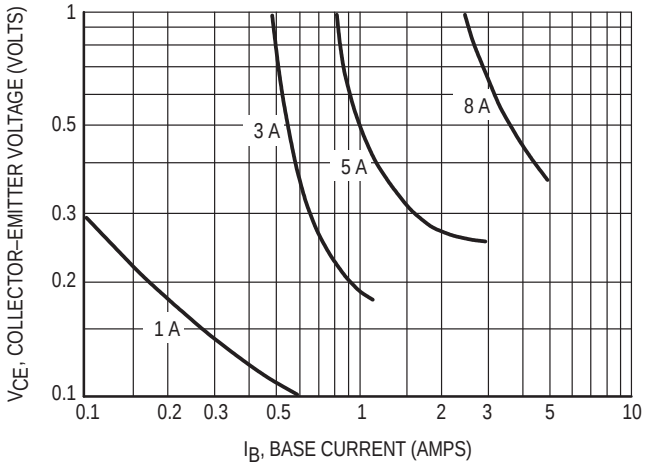


Figure 3. Collector–Emitter Saturation Region

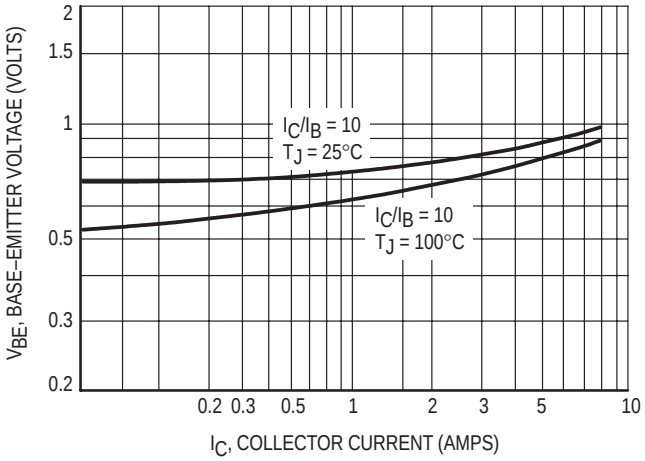


Figure 4. Base–Emitter Saturation Region

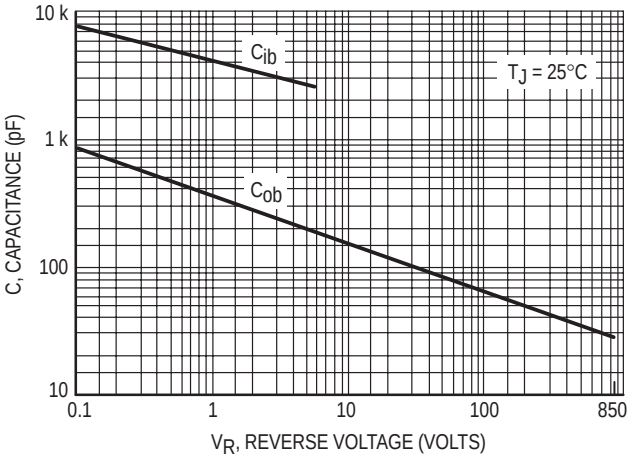


Figure 5. Capacitance

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

I_C/I_{B1} = 5, T_C = 75°C, $V_{CE(pk)}$ = 400 V

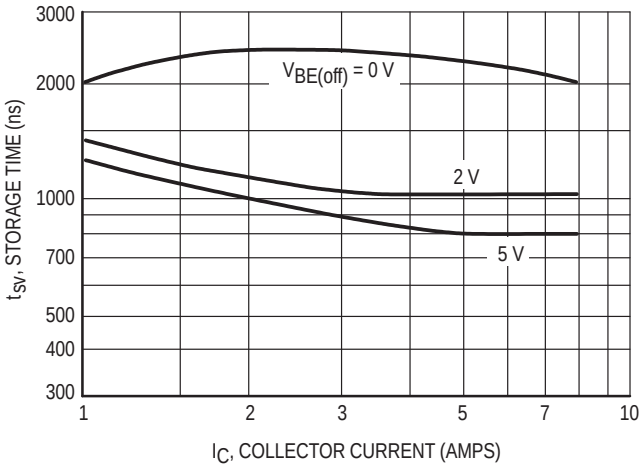


Figure 6. Storage Time

I_C/I_{B1} = 10, T_C = 75°C, $V_{CE(pk)}$ = 400 V

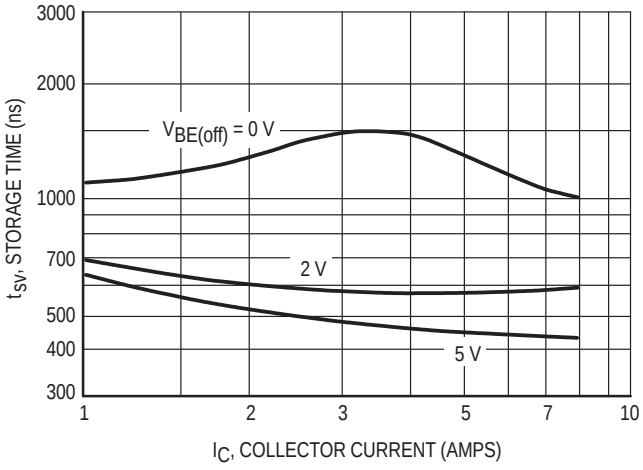


Figure 7. Storage Time

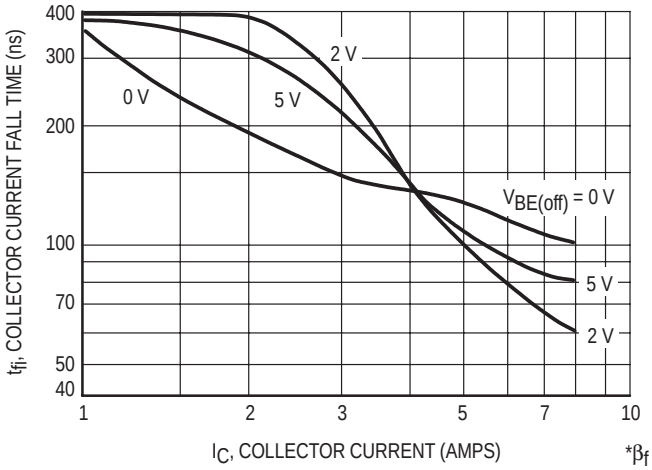


Figure 8. Collector Current Fall Time

$$*\beta_f = \frac{I_C}{I_{B1}}$$

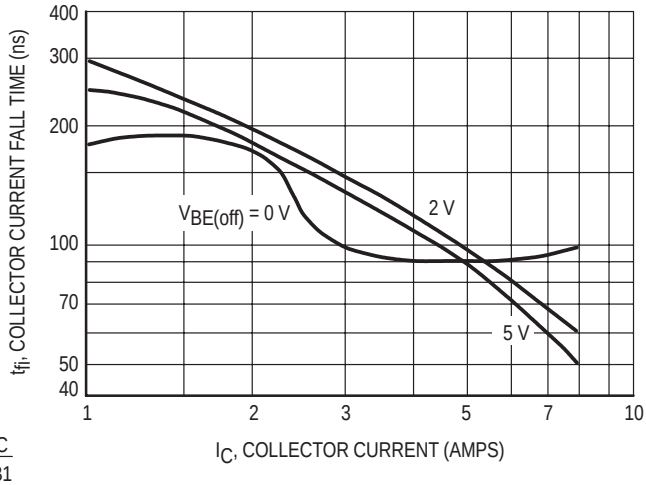


Figure 9. Collector Current Fall Time

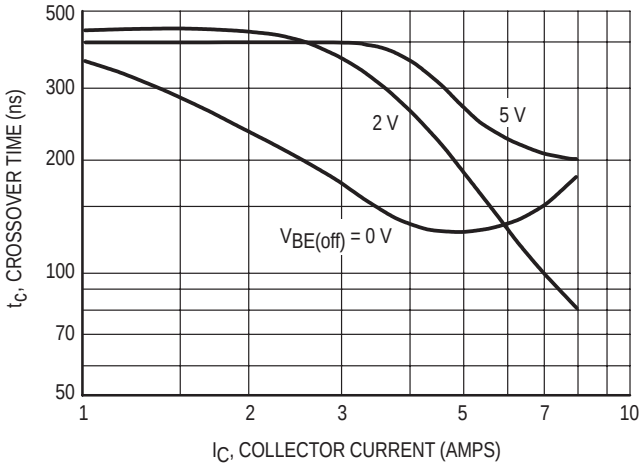


Figure 10. Crossover Time

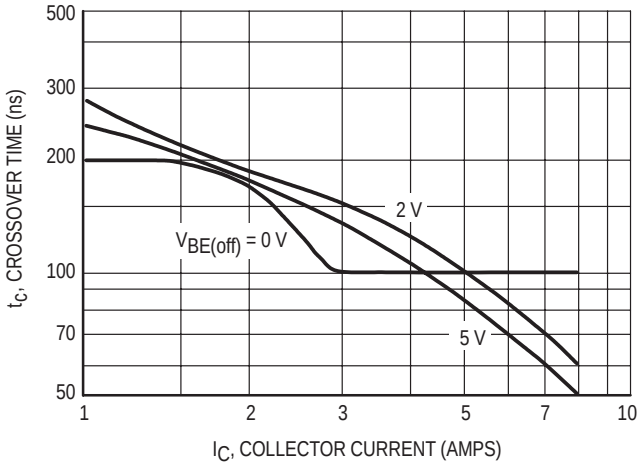
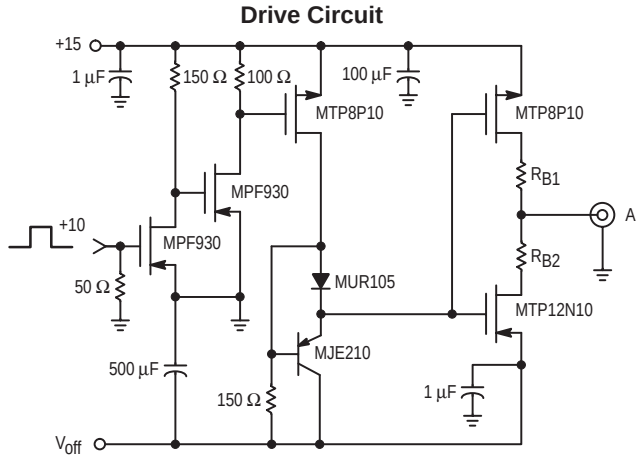


Figure 11. Crossover Time

Table 1. Inductive Load Switching

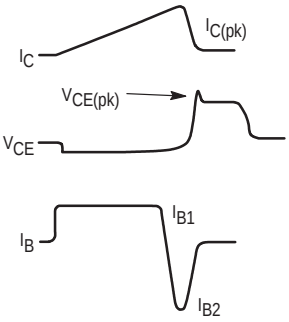


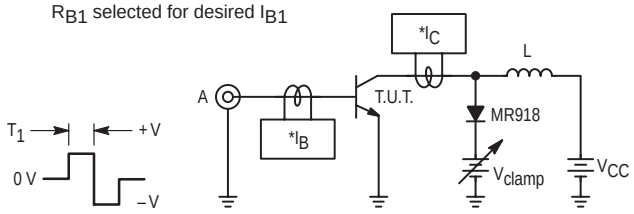
Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A.

$V_{CEO(sus)}$
L = 10 mH
R_{B2} = ∞
V_{CC} = 20 Volts

Inductive Switching
L = 750 µH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 750 µH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}





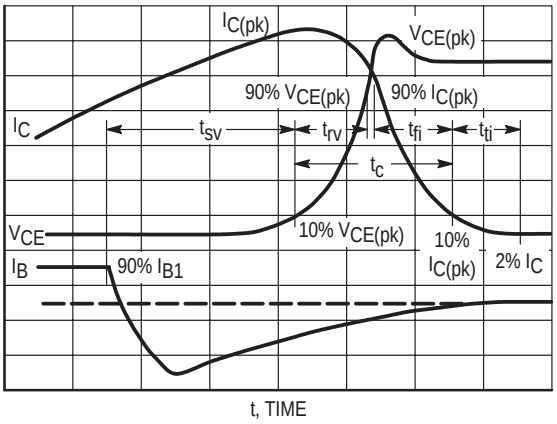


Figure 12. Inductive Switching Measurements

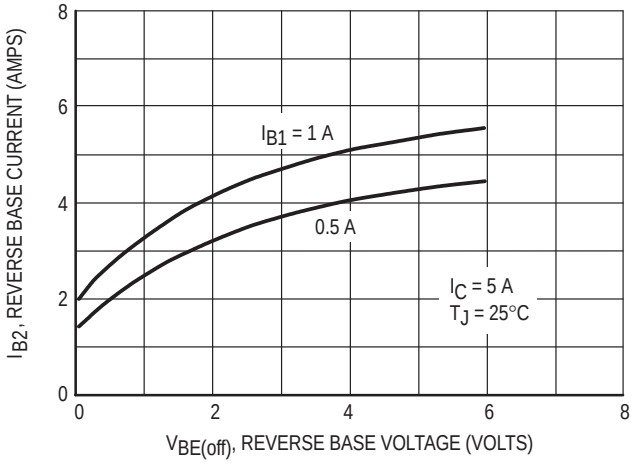
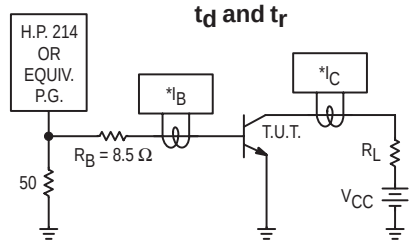
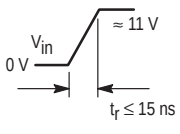


Figure 13. Peak Reverse Base Current

Table 2. Resistive Load Switching

t_d and t_r



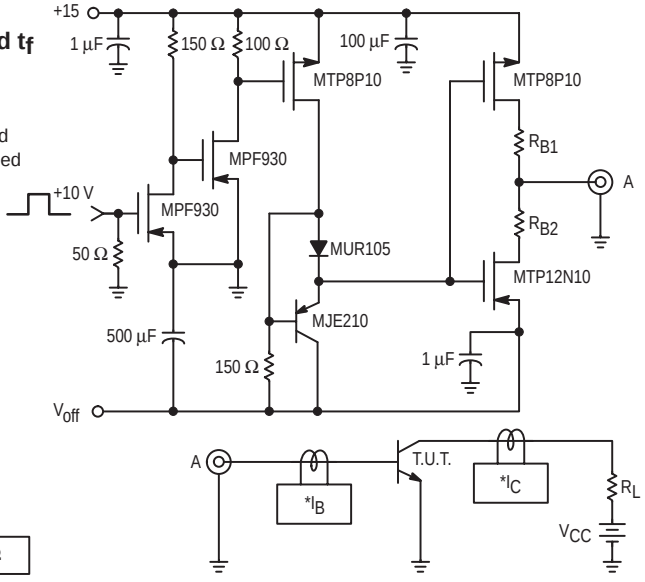


V_{CC}	250 V
R_L	50 Ω
I_C	5 A
I_B	0.66 A

*Tektronix AM503
P6302 or Equivalent

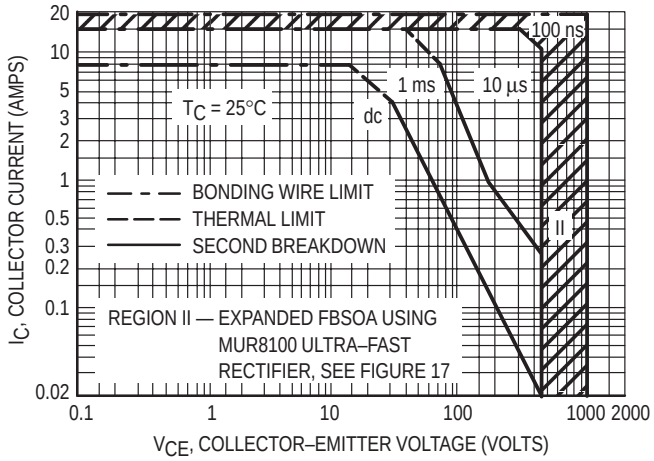
t_s and t_f

$V_{(off)}$ adjusted to give specified off drive

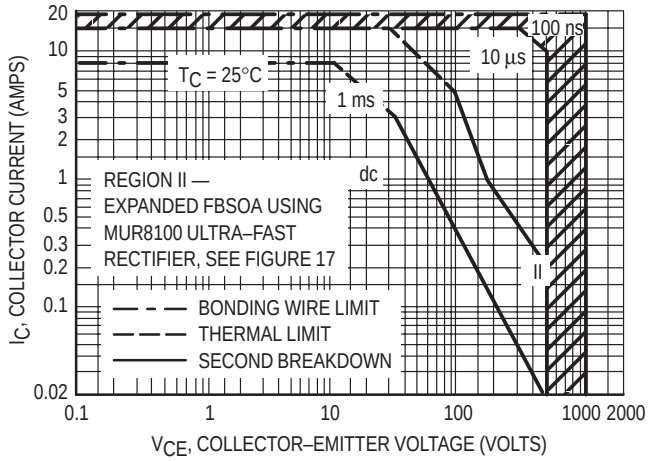


R_L	50 Ω

GUARANTEED SAFE OPERATING AREA LIMITS



a. MJ16006A



a. MJH16006A

Figure 14. Maximum Rated Forward Biased Safe Operating Area

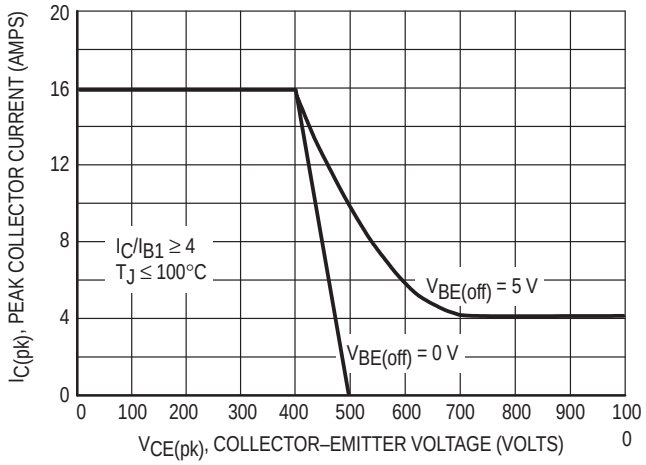


Figure 15. Maximum Reverse Biased Safe Operating Area

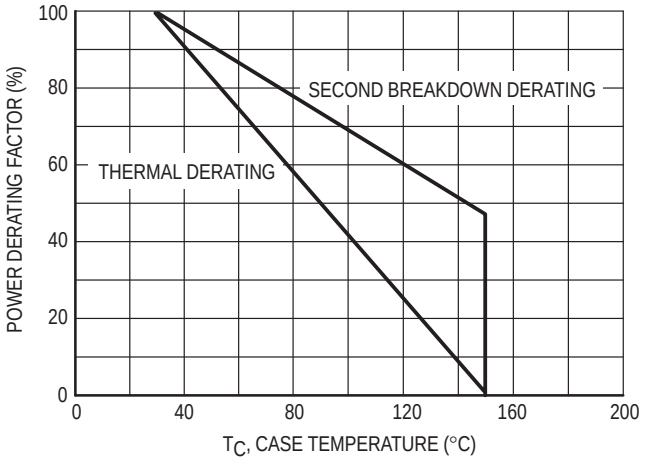


Figure 16. Power Derating

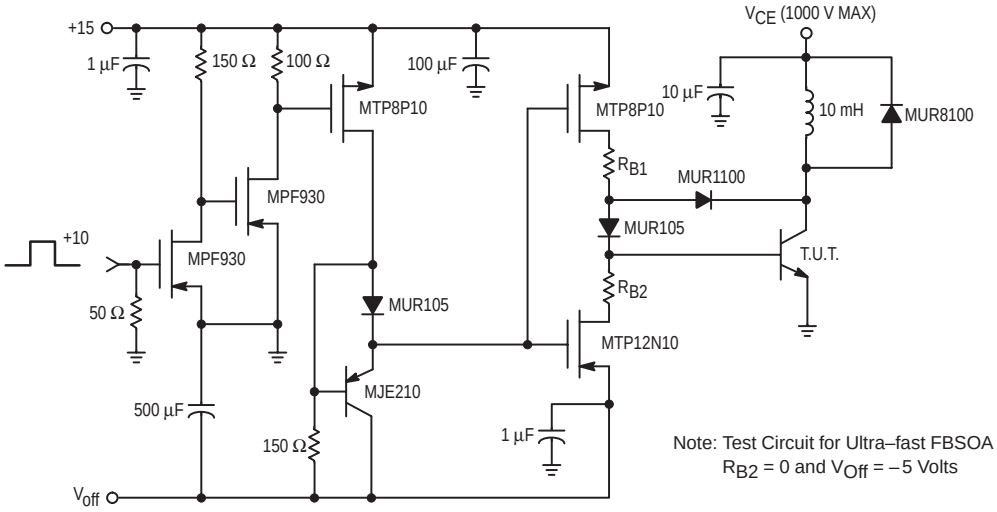


Figure 17. Switching Safe Operating Area

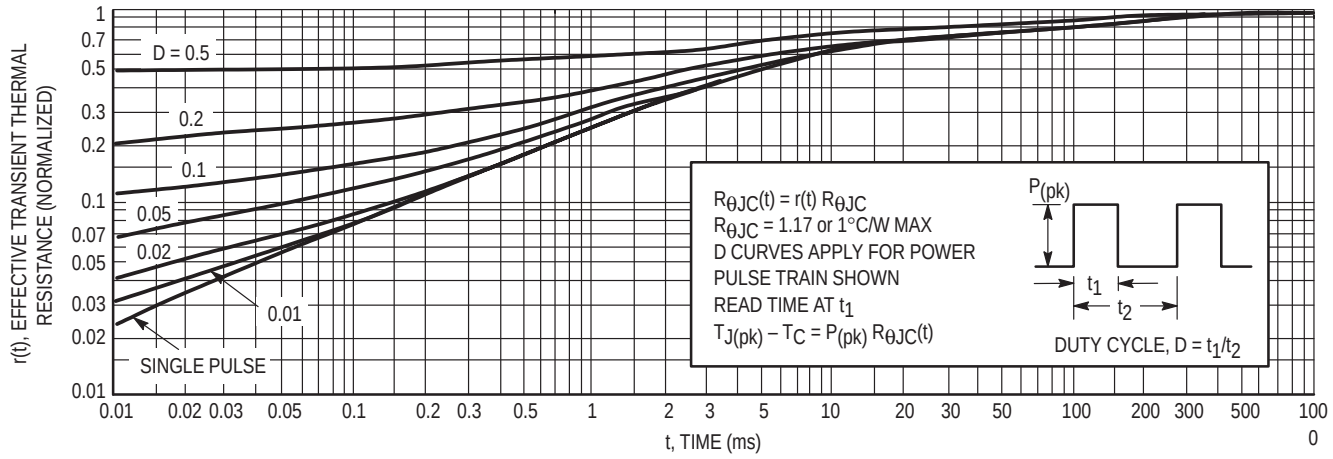


Figure 18. Thermal Response

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 14a and 14b is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 14a and 14b may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

SWITCHMODE III DESIGN CONSIDERATIONS

1. FBSOA —

Allowable dc power dissipation in bipolar power transistors decreases dramatically with increasing collector emitter voltage. A transistor which safely dissipates 100 watts at 10 volts will typically dissipate less than 10 watts at its rated $V_{CEO(sus)}$. From a power handling point of view, current and voltage are not interchangeable (see Application Note AN875).

2. TURN–ON —

Safe turn–on load line excursions are bounded by pulsed FBSOA curves. The 10 μs curve applies for resistive loads, most capacitive loads, and inductive loads that are clamped by standard or fast recovery rectifiers. Similarly, the 100 ns curve applies to inductive loads which are clamped by ultra–fast recovery rectifiers, and are valid for turn–on crossover times less than 100 ns (see Application Note AN952).

At voltages above 75% of $V_{CEO(sus)}$, it is essential to provide the transistor with an adequate amount of base drive VERY RAPIDLY at turn–on. More specifically, safe operation according to the curves is dependent upon base current rise time being less than collector current rise time. As a general rule, a base drive compliance voltage in excess of 10 volts is required to meet this condition (see Application Note AN875).

3. TURN–OFF —

A bipolar transistor's ability to withstand turn–off stress is dependent upon its forward base drive. Gross overdrive violates the RBSOA curve and risks transistor failure. For this reason, circuits which use fixed base drive are often more likely to fail at light loads due to heavy overdrive (see Application Note AN875).

4. OPERATION ABOVE $V_{CEO(sus)}$ —

When bipolars are operated above collector–emitter breakdown, base drive is crucial. A rapid application of adequate forward base current is needed for safe turn–on, as is a stiff negative bias needed for safe turn–off. Any hiccup in the base–drive circuitry that even momentarily violates either of these conditions will likely cause the transistor to fail. Therefore, it is important to design the driver so that its output is negative in the absence of anything but a clean crisp input signal (see Application Note AN952).

SWITCHMODE DESIGN CONSIDERATIONS (Cont.)

5. RBSOA —

Reverse Biased Safe Operating Area has a first order dependency on circuit configuration and drive parameters. The RBSOA curves in this data sheet are valid only for the conditions specified. For a comparison of RBSOA results in several types of circuits (see Application Note AN951).

6. DESIGN SAMPLES —

Transistor parameters tend to vary much more from wafer lot to wafer lot, over long periods of time, than from one device to the next in the same wafer lot. For design evaluation it is advisable to use transistors from several different date codes.

7. BAKER CLAMPS —

Many unanticipated pitfalls can be avoided by using Baker Clamps. MUR105 and MUR1100 diodes are recommended for base drives less than 1 amp. Similarly, MUR405 and MUR4100 types are well–suited for higher drive requirements (see Article Reprint AR131).

Silicon Power Transistors

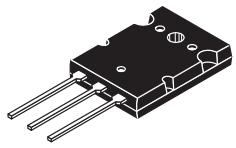
PNP
MJL21193*
NPN
MJL21194*

*Motorola Preferred Device

The MJL21193 and MJL21194 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain – h_{FE} = 25 Min @ I_C = 8 Adc
- Excellent Gain Linearity
- High SOA: 2.25 A, 80 V, 1 Second

16 AMPERE
COMPLEMENTARY
SILICON POWER
TRANSISTORS
250 VOLTS
200 WATTS



CASE 340G–02
TO–3PBL

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CBO}	400	Vdc
Emitter–Base Voltage	V_{EBO}	5	Vdc
Collector–Emitter Voltage – 1.5 V	V_{CEX}	400	Vdc
Collector Current — Continuous Peak (1)	I_C	16 30	Adc
Base Current – Continuous	I_B	5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	200 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	– 65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 μs, Duty Cycle ≤10%.

(continued)

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)	I_{EBO}	—	—	100	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	—	—	100	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$				Adc
(V_{CE} = 50 Vdc, t = 1 s (non–repetitive))		4.0	—	—	
(V_{CE} = 80 Vdc, t = 1 s (non–repetitive))		2.25	—	—	
ON CHARACTERISTICS					
DC Current Gain	h_{FE}				
(I_C = 8 Adc, V_{CE} = 5 Vdc)		25	—	75	
(I_C = 16 Adc, I_B = 5 Adc)		8	—	—	
Base–Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	—	—	2.2	Vdc
Collector–Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 8 Adc, I_B = 0.8 Adc)		—	—	1.4	
(I_C = 16 Adc, I_B = 3.2 Adc)		—	—	4	
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output	T_{HD}				%
V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS} h_{FE} unmatched		—	0.8	—	
(Matched pair h_{FE} = 50 @ 5 A/5 V) h_{FE} matched		—	0.08	—	
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	4	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	—	500	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

PNP MJL21193

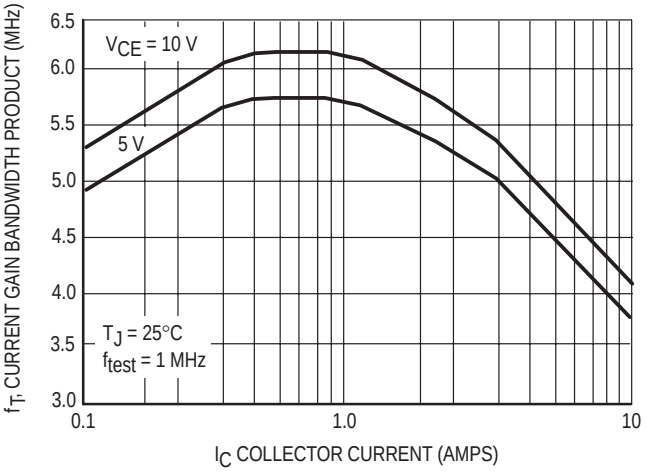


Figure 1. Typical Current Gain Bandwidth Product

NPN MJL21194

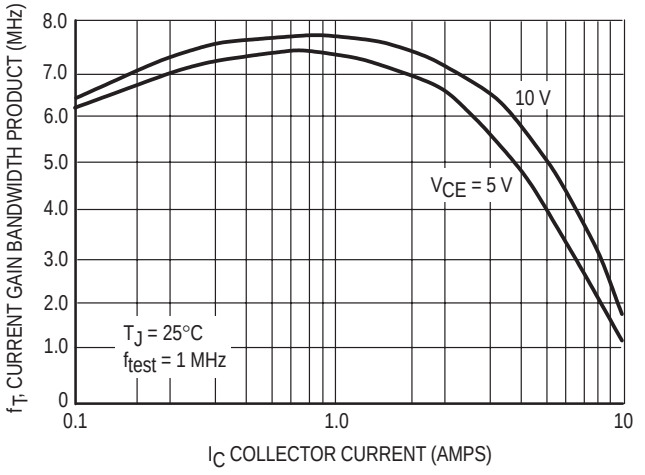


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJL21193

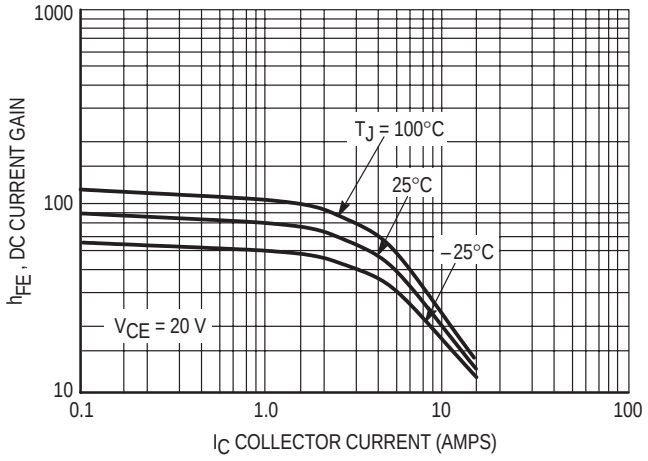


Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJL21194

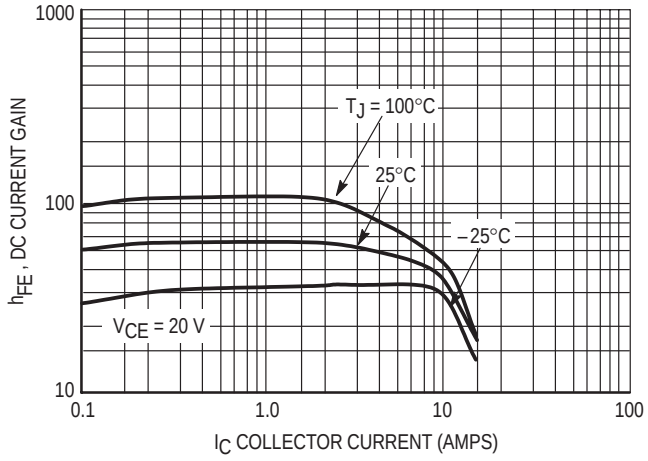


Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJL21193

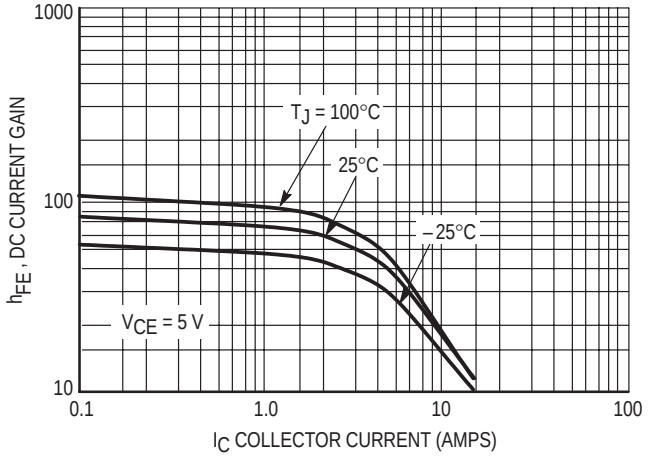


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJL21194

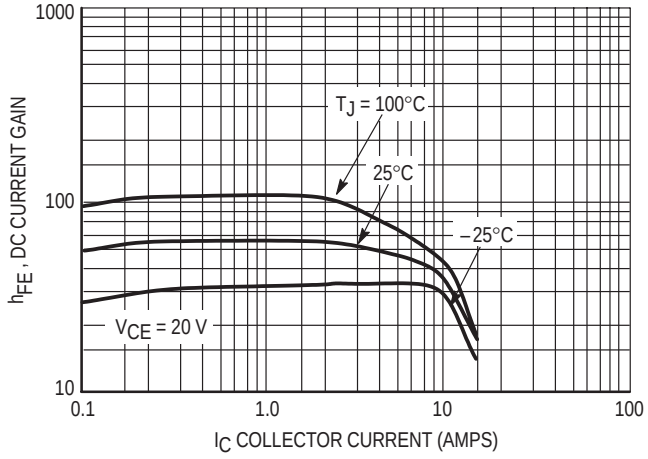


Figure 6. DC Current Gain, V_{CE} = 5 V

PNP MJL21193

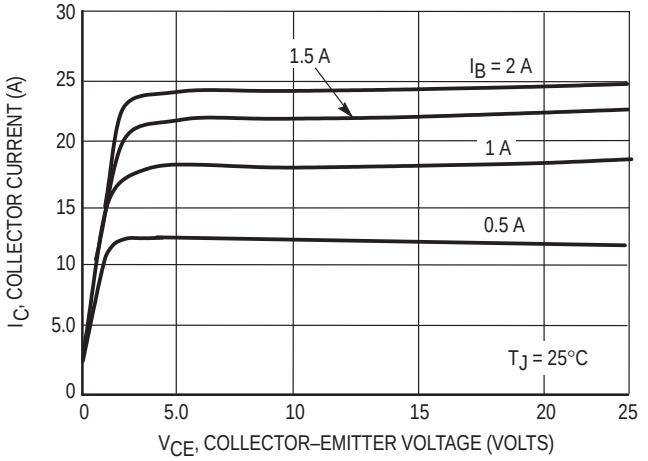


Figure 7. Typical Output Characteristics

NPN MJL21194

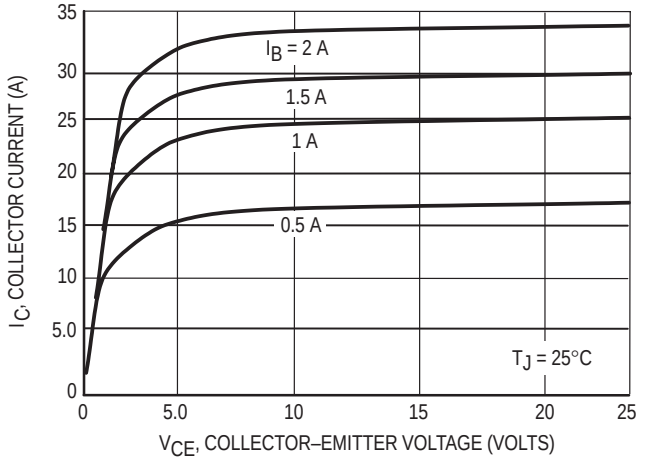


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJL21193

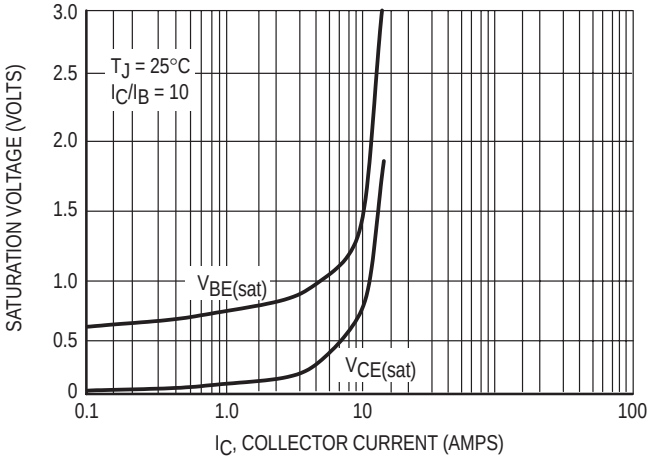


Figure 9. Typical Saturation Voltages

NPN MJL21194

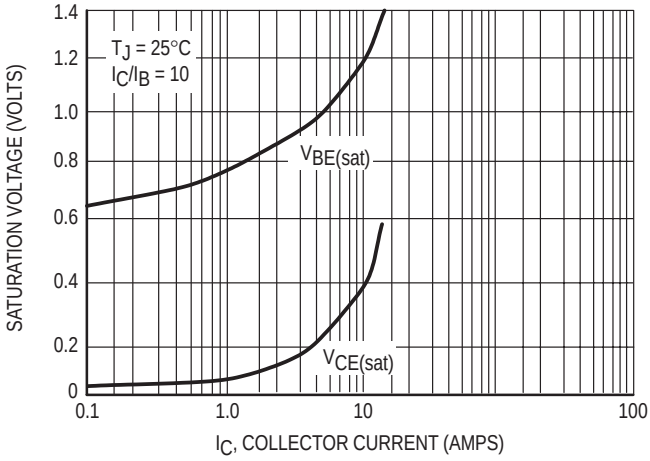


Figure 10. Typical Saturation Voltages

PNP MJL21193

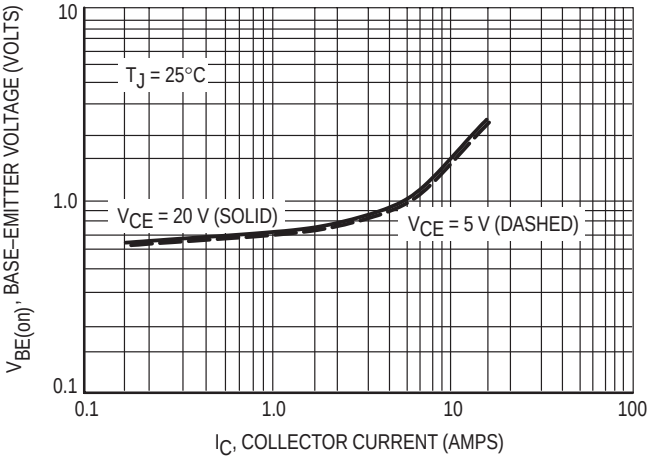


Figure 11. Typical Base–Emitter Voltage

NPN MJL21194

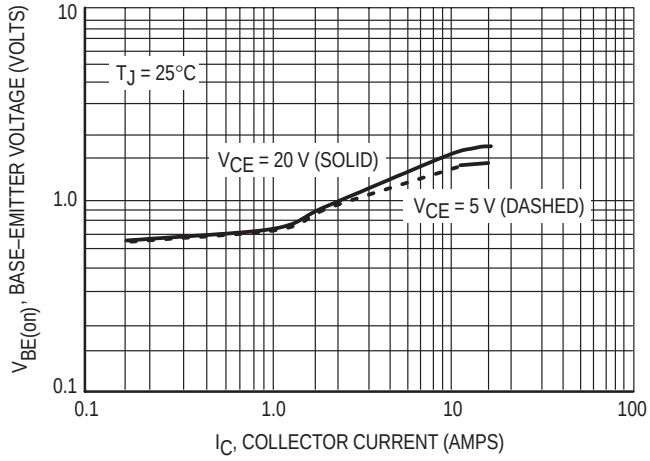


Figure 12. Typical Base–Emitter Voltage

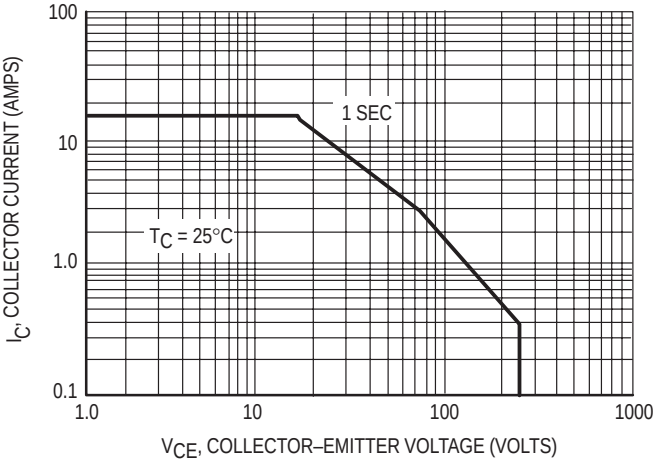


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

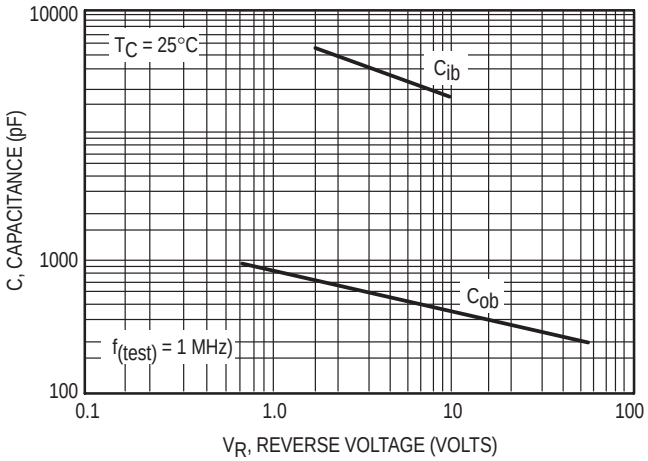


Figure 14. MJL21193 Typical Capacitance

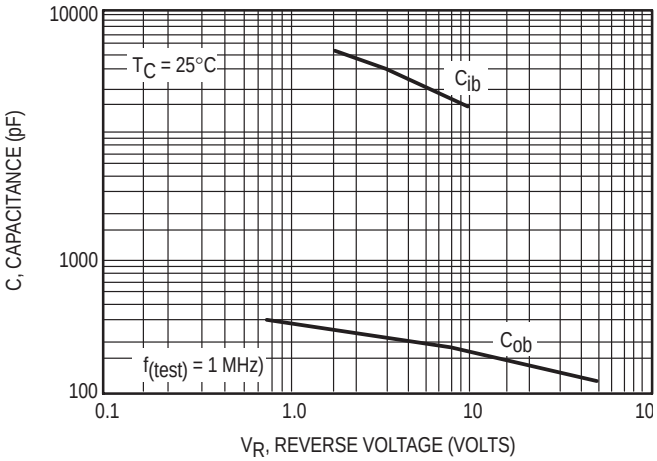


Figure 15. MJL21194 Typical Capacitance

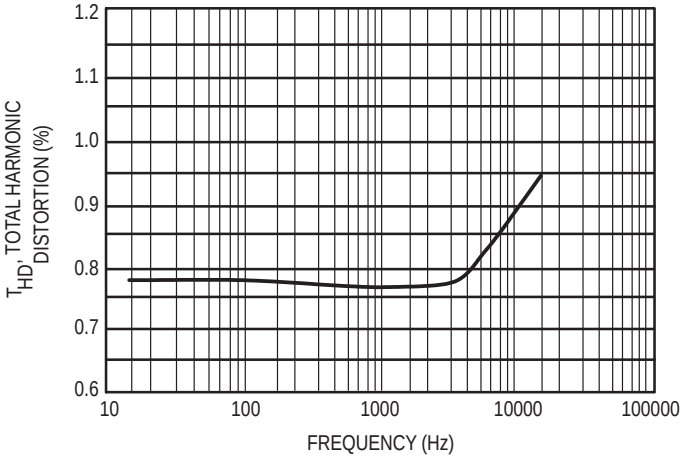


Figure 16. Typical Total Harmonic Distortion

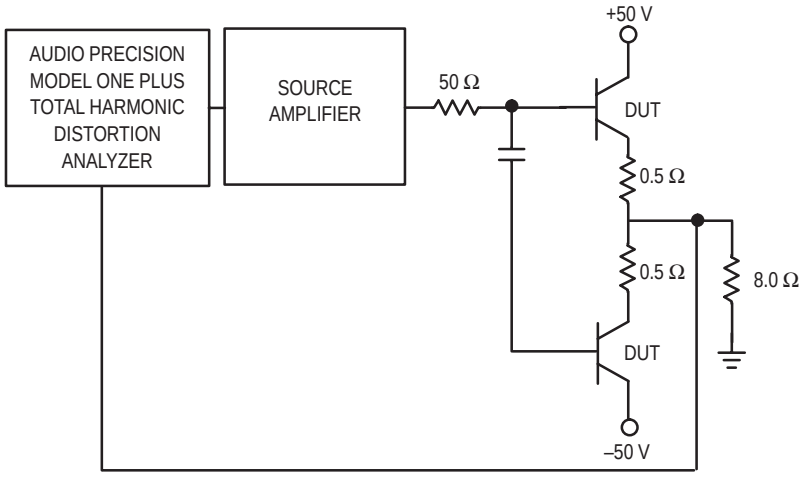


Figure 17. Total Harmonic Distortion Test Circuit

NPN
MJL3281A*
PNP
MJL1302A*

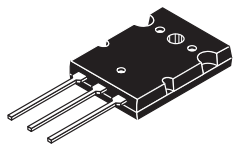
*Motorola Preferred Device

Designer's™ Data Sheet

Complementary NPN-PNP Silicon Power Bipolar Transistor

- The MJL3281A and MJL1302A are PowerBase power transistors for high power audio, disk head positioners and other linear applications.
- Designed for 100 W Audio Frequency
- Gain Complementary:
  - — Gain Linearity from 100 mA to 7 A
  - — High Gain — 60 to 175
  - — h_{FE} = 45 (Min) @ I_C = 8 A
- Low Harmonic Distortion
- High Safe Operation Area — 1 A/100 V @ 1 sec
- High f_T — 30 MHz Typical

15 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 200 VOLTS 200 WATTS



CASE 340G–02, STYLE 2 TO–264

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	200	Vdc
Collector–Base Voltage	V_{CBO}	200	Vdc
Emitter–Base Voltage	V_{EBO}	7	Vdc
Collector–Emitter Voltage — 1.5 V	V_{CEX}	200	Vdc
Collector Current — Continuous — Peak (1)	I_C	15 25	Adc
Base Current — Continuous	I_B	1.5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	200 1.43	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	200	—	—	Vdc
Emitter–Base Voltage (I_E = 100 μAdc, I_C = 0)	V_{EBO}	7	—	—	Vdc
Collector Cutoff Current (V_{CB} = 200 Vdc, I_E = 0)	I_{CBO}	—	—	50	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	—	—	5	μAdc
Emitter Cutoff Current (V_{EB} = 7 Vdc, I_C = 0)	I_{EBO}	—	—	25	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector with Base Forward Biased	$I_{S/b}$				Adc
(V_{CE} = 50 Vdc, t = 1 s (non–repetitive)		4	—	—	
(V_{CE} = 100 Vdc, t = 1 s (non–repetitive)		1	—	—	
ON CHARACTERISTICS					
DC Current Gain	h_{FE}				
(I_C = 100 mAdc, V_{CE} = 5 Vdc)		60	125	175	
(I_C = 1 Adc, V_{CE} = 5 Vdc)		60	—	175	
(I_C = 3 Adc, V_{CE} = 5 Vdc)		60	—	175	
(I_C = 5 Adc, V_{CE} = 5 Vdc)		60	—	175	
(I_C = 7 Adc, V_{CE} = 5 Vdc)		60	115	175	
(I_C = 8 Adc, V_{CE} = 5 Vdc)		45	—	—	
(I_C = 15 Adc, V_{CE} = 5 Vdc)		12	35	—	
Collector–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1 Adc)	$V_{CE(sat)}$	—	—	3	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)	f_T	—	30	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	—	—	600	pF

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

PNP MJL1302A

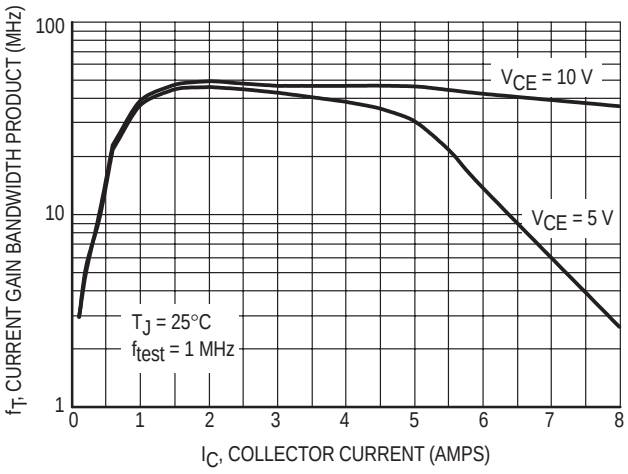


Figure 1. Current–Gain — Bandwidth Product

NPN MJL3281A

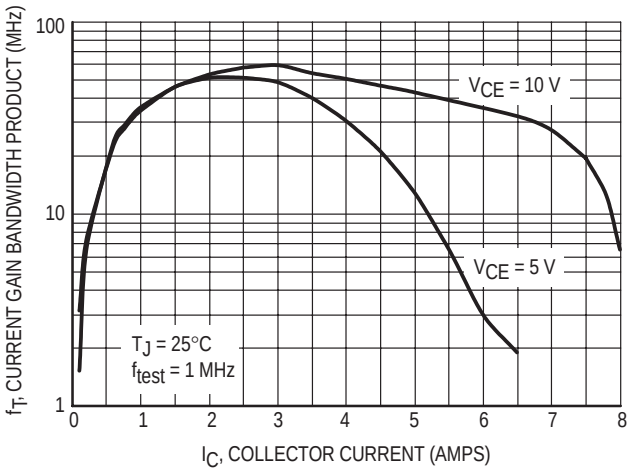


Figure 2. Current–Gain — Bandwidth Product

PNP MJL1302A

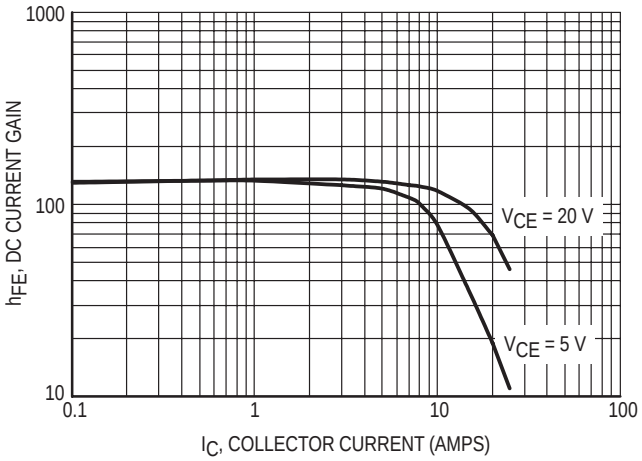


Figure 3. DC Current Gain

NPN MJL3281A

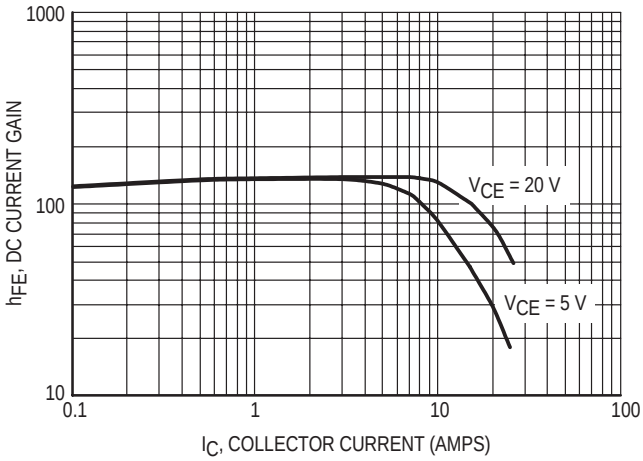


Figure 4. DC Current Gain

PNP MJL1302A

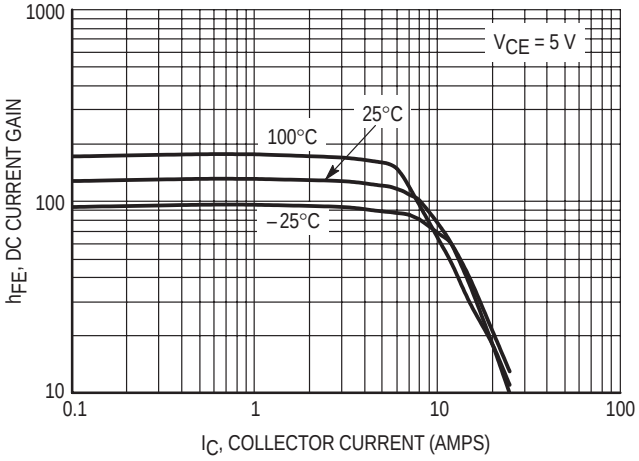


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJL3281A

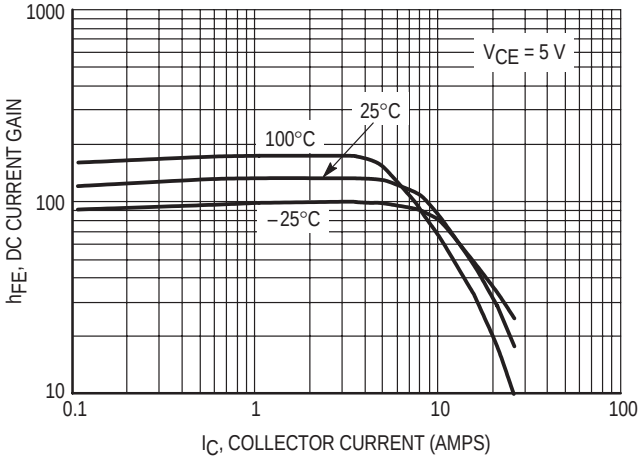


Figure 6. DC Current Gain, V_{CE} = 5 V

TYPICAL CHARACTERISTICS

PNP MJL1302A

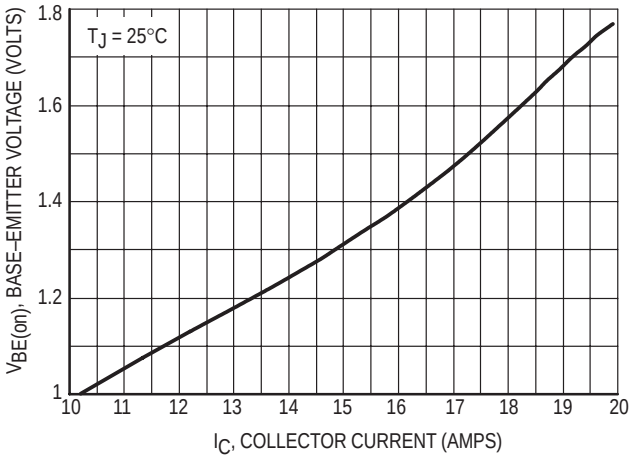


Figure 7. Typical Base–Emitter Voltage

NPN MJL3281A

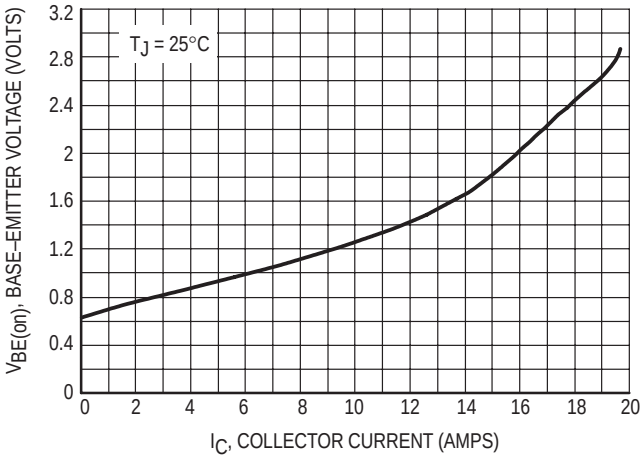


Figure 8. Typical Base–Emitter Voltage

PNP MJL1302A

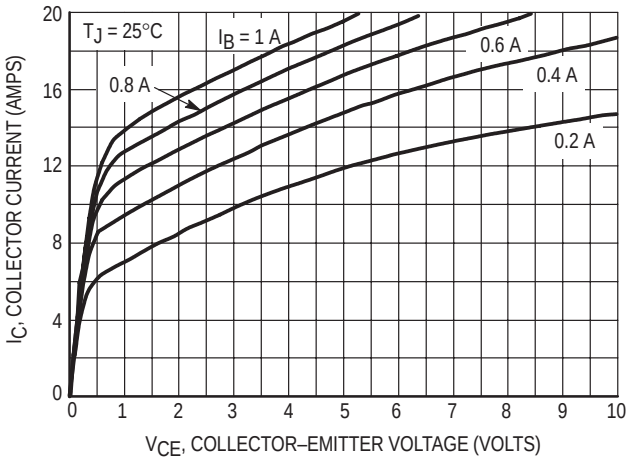


Figure 9. Typical Output Characteristics

NPN MJL3281A

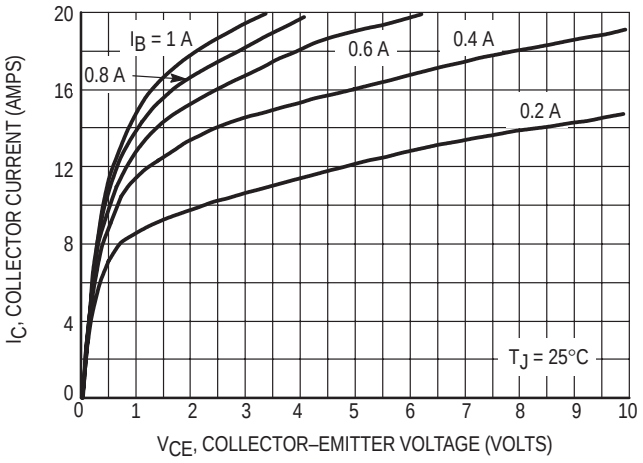


Figure 10. Typical Output Characteristics

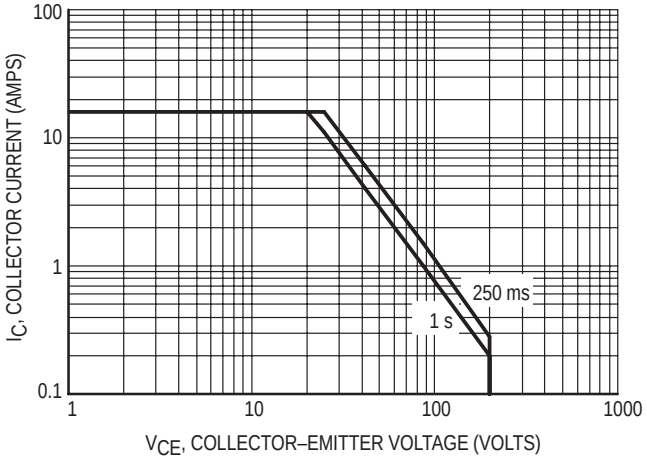


Figure 11. Forward Bias Safe Operating Area (FBSOA)

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

MJW16010A*

*Motorola Preferred Device

POWER TRANSISTORS
15 AMPERES
500 VOLTS
125 AND 175 WATTS

Designer's™ Data Sheet

NPN Silicon Power Transistors

1 kV SWITCHMODE Series

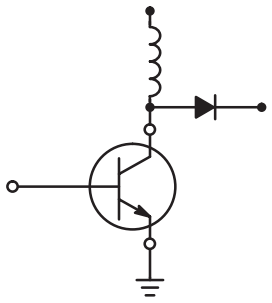
These transistors are designed for high–voltage, high–speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line–operated switchmode applications.

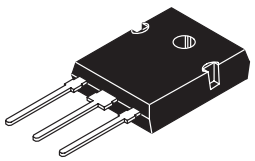
Typical Applications:

- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

Features:

- Collector–Emitter Voltage — V_{CEV} = 1000 Vdc
- Fast Turn–Off Times
  50 ns Inductive Fall Time — 100°C (Typ)
  90 ns Inductive Crossover Time — 100°C (Typ)
  900 ns Inductive Storage Time — 100°C (Typ)
- 100°C Performance Specified for:
  Reverse–Biased SOA with Inductive Load
  Switching Times with Inductive Loads
  Saturation Voltages
  Leakage Currents
- Extended FBSOA Rating Using Ultra–fast Rectifiers
- Extremely High RBSOA Capability





CASE 340F–03
TO–247AE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	500	Vdc
Collector–Emitter Voltage	V_{CEV}	1000	Vdc
Emitter–Base Voltage	V_{EB}	6	Vdc
Collector Current— Continuous — Peak(1)	I_C I_{CM}	15 20	Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	10 15	Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above T_C = 25°C	P_D	135 54 1.09	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	I_C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.92	°C/W
Lead Temperature for Soldering Purposes: 1/8″ from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS(1)							
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)			$V_{CEO(sus)}$	500	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			I_{CEV}	 — —	 0.003 0.020	 0.15 1.0	mAdc
Collector Cutoff Current (V_{CE} = 1000 Vdc, R_{BE} = 50 Ω, T_C = 100°C)			I_{CER}	—	0.020	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)			I_{EBO}	—	0.005	0.15	mAdc
SECOND BREAKDOWN							
Second Breakdown Collector Current with Base Forward Biased			$I_{S/b}$	See Figure 14a or 14b			
Clamped Inductive SOA with Base Reverse Biased			RBSOA	See Figure 15			
ON CHARACTERISTICS(1)							
Collector–Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc) (I_C = 10 Adc, I_B = 2 Adc) (I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)			$V_{CE(sat)}$	 — — —	 0.25 0.45 0.60	 0.7 1 1.5	Vdc
Base–Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2 Adc) (I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)			$V_{BE(sat)}$	 — —	 1.2 1.2	 1.5 1.5	Vdc
DC Current Gain (I_C = 15 Adc, V_{CE} = 5 Vdc)			h_{FE}	5	8	—	—
DYNAMIC CHARACTERISTICS							
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 kHz)			C_{ob}	—	—	400	pF
SWITCHING CHARACTERISTICS							
Inductive Load (Table 1)							
Storage Time	(I_C = 10 Adc, I_{B1} = 1.3 Adc, $V_{BE(off)}$ = 5 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	900	2000	ns
Fall Time			t_{fi}	—	50	250	
Crossover Time			t_c	—	90	300	
Storage Time		(T_J = 150°C)	t_{sv}	—	1100	—	
Fall Time			t_{fi}	—	70	—	
Crossover Time			t_c	—	120	—	
Resistive Load (Table 2)							
Delay Time	(I_C = 10 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.3 Adc, PW = 30 μs, Duty Cycle ≤ 2%)	(I_{B2} = 2.6 Adc, R_{B2} = 1.6 Ω)	t_d	—	25	100	ns
Rise Time			t_r	—	325	600	
Storage Time			t_s	—	1300	3000	
Fall Time			t_f	—	175	400	
Storage Time		($V_{BE(off)}$ = 5 Vdc)	t_s	—	700	—	
Fall Time			t_f	—	80	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL STATIC CHARACTERISTICS

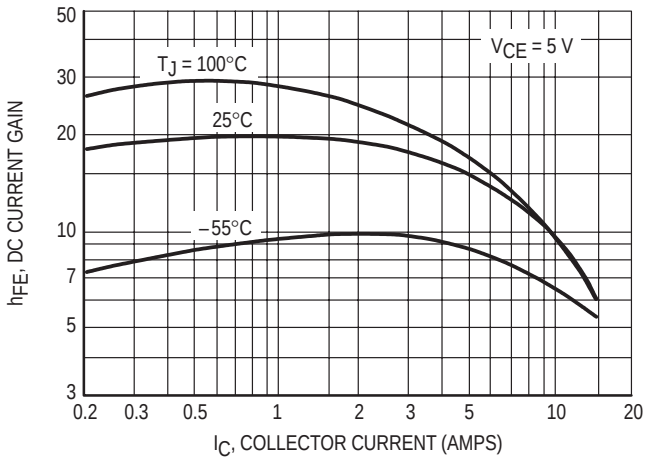


Figure 1. DC Current Gain

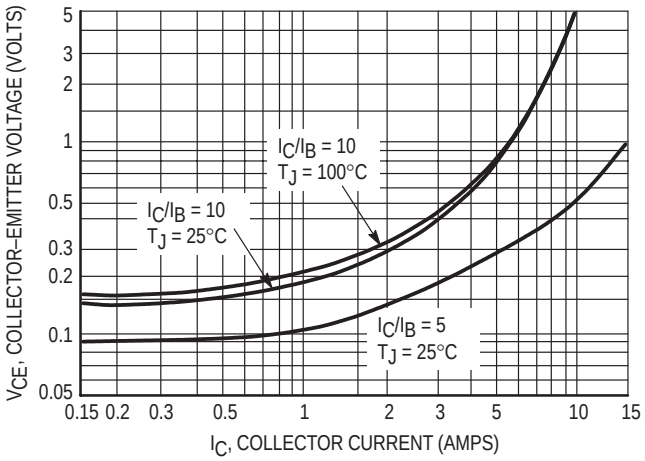


Figure 2. Collector–Emitter Saturation Region

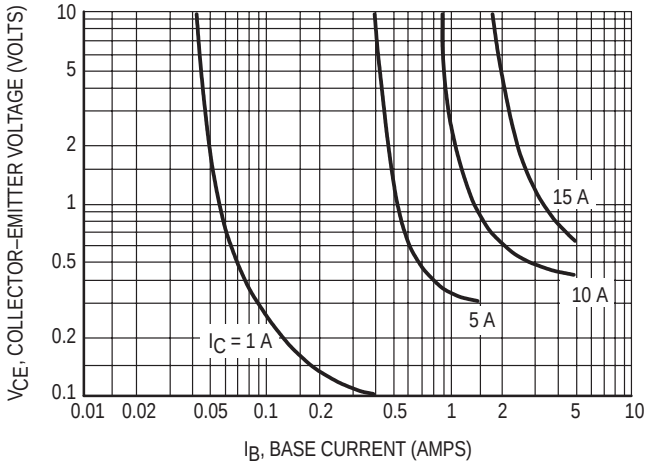


Figure 3. Collector–Emitter Saturation Region

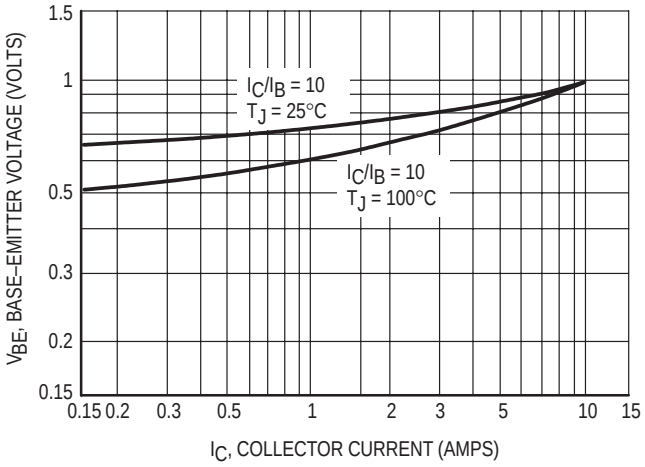


Figure 4. Base–Emitter Saturation Region

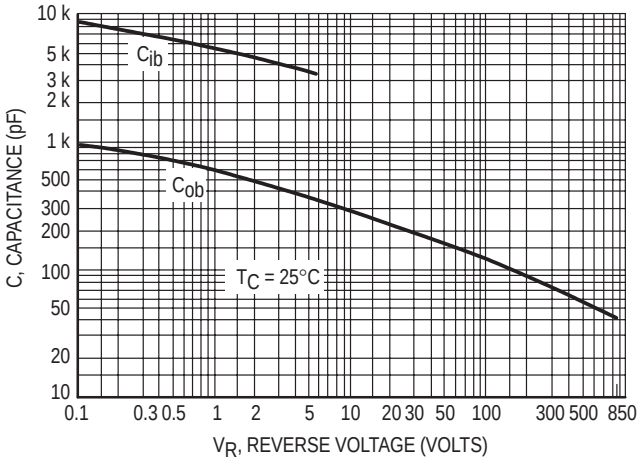


Figure 5. Capacitance

TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

I_C/I_{B1} = 5, T_C = 75°C, $V_{CE(pk)}$ = 400 V

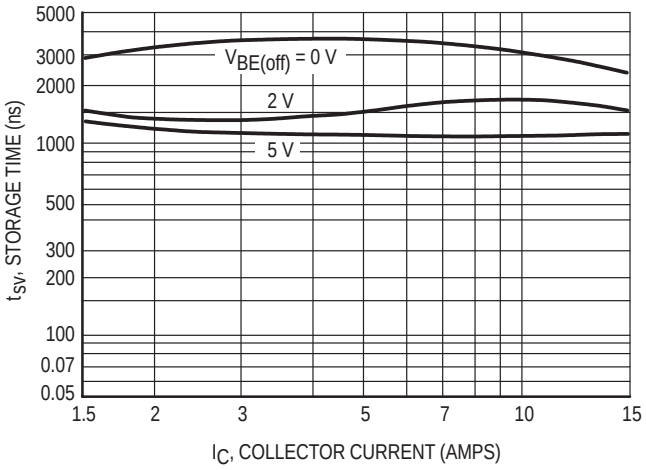


Figure 6. Storage Time

I_C/I_{B1} = 10, T_C = 75°C, $V_{CE(pk)}$ = 400 V

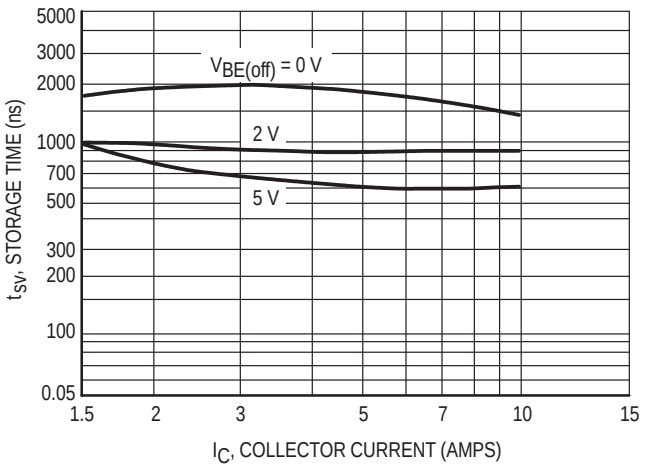


Figure 7. Storage Time

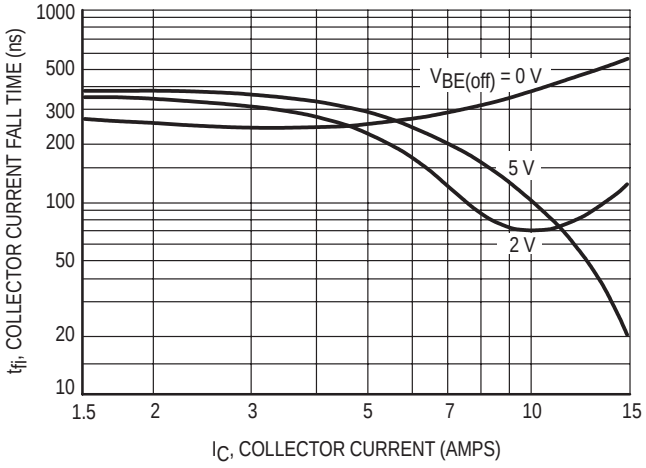


Figure 8. Collector Current Fall Time

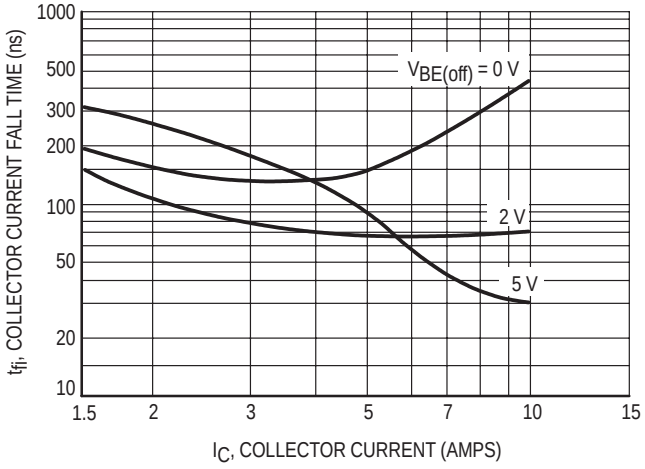


Figure 9. Collector Current Fall Time

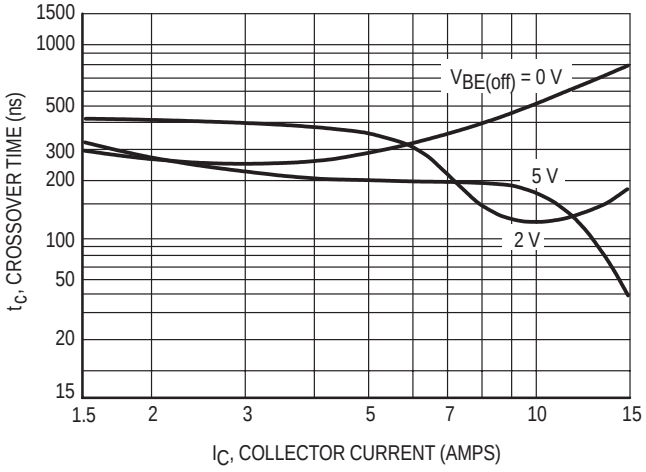


Figure 10. Crossover Time

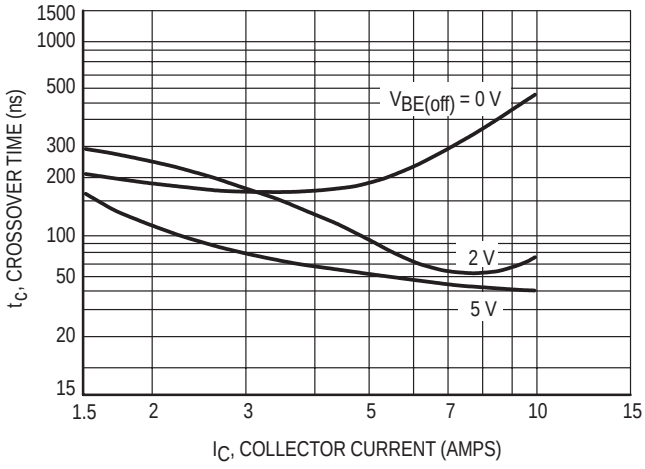
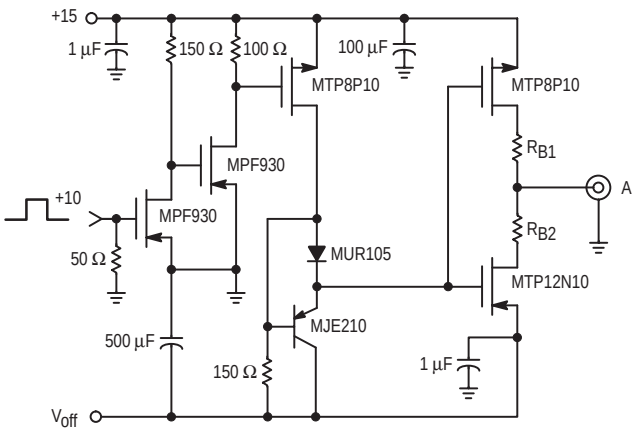


Figure 11. Crossover Time

Table 1. Inductive Load Switching

Drive Circuit



*Tektronix AM503
P6302 or Equivalent

Scope — Tektronix
7403 or Equivalent

$$T_1 \approx \frac{L_{coil}\ (I_{Cpk})}{V_{CC}}$$

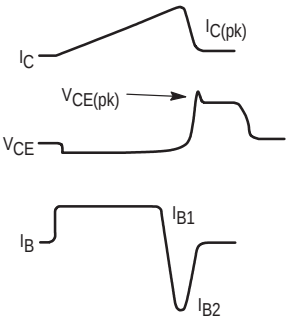
T_1 adjusted to obtain $I_{C(pk)}$

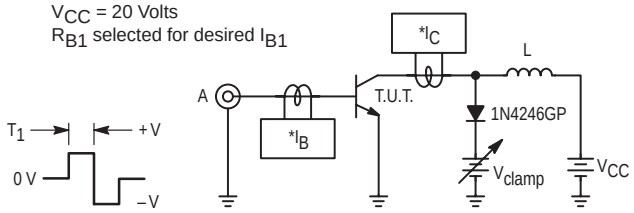
Note: Adjust V_{off} to obtain desired $V_{BE(off)}$ at Point A.

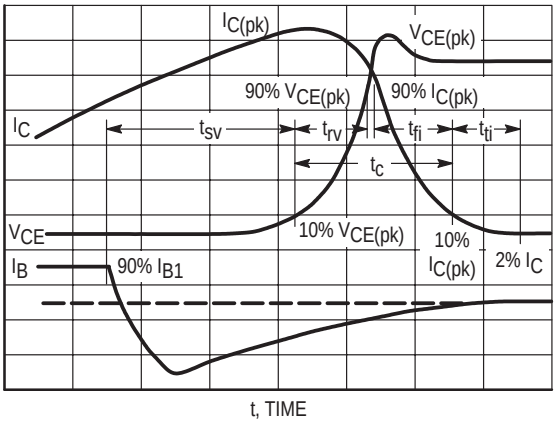
$V_{CEO(sus)}$
L = 10 mH
R_{B2} = ∞
V_{CC} = 20 Volts
$I_{C(pk)}$ = 100 mA

Inductive Switching
L = 200 µH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

RBSOA
L = 200 µH
R_{B2} = 0
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}







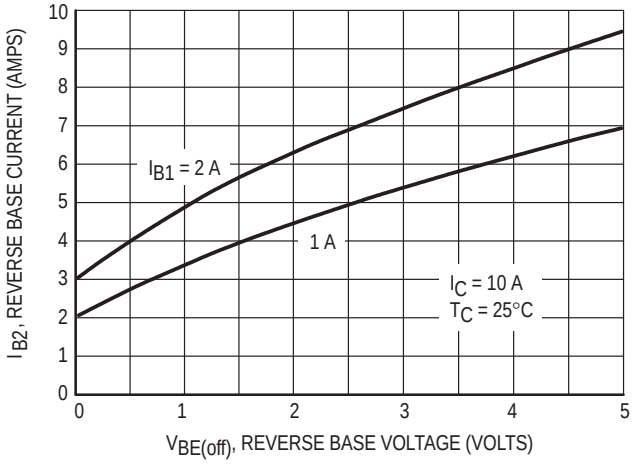
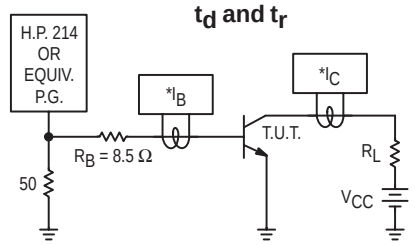


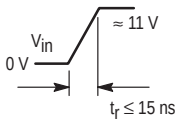
Figure 12. Inductive Switching Measurements

Figure 13. Peak Reverse Base Current

Table 2. Resistive Load Switching

t_d and t_r



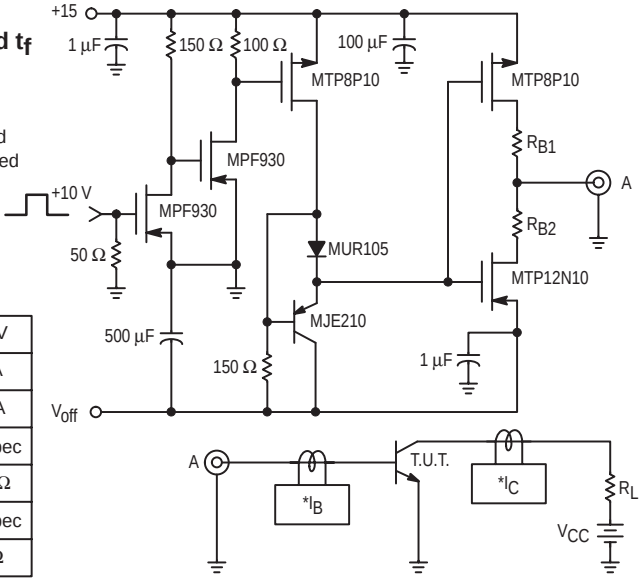


V_{CC}	250 Vdc
R_L	25 Ω
I_C	10 A
I_B	1.3 A

*Tektronix AM503
P6302 or Equivalent

t_s and t_f

$V_{(off)}$ adjusted to give specified off drive



V_{CC}	250 V
I_C	10 A
I_{B1}	1.3 A
I_{B2}	Per Spec
R_{B1}	11.5 Ω
R_{B2}	Per Spec
R_L	25 Ω

GUARANTEED OPERATING AREA INFORMATION

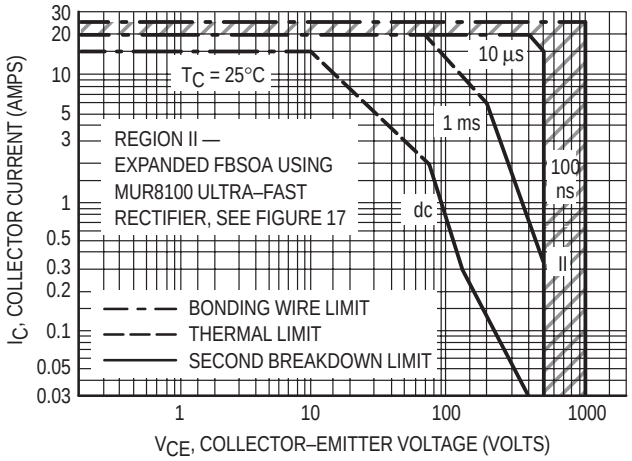


Figure 14. Maximum Rated Forward Biased Safe Operating Area

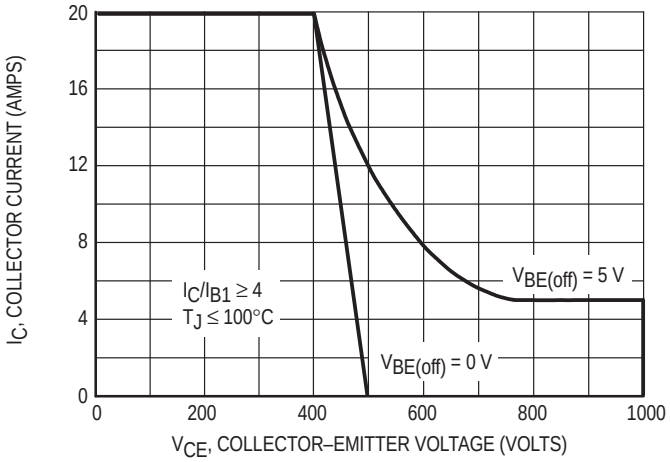


Figure 15. Maximum Reverse Biased Safe Operating Area

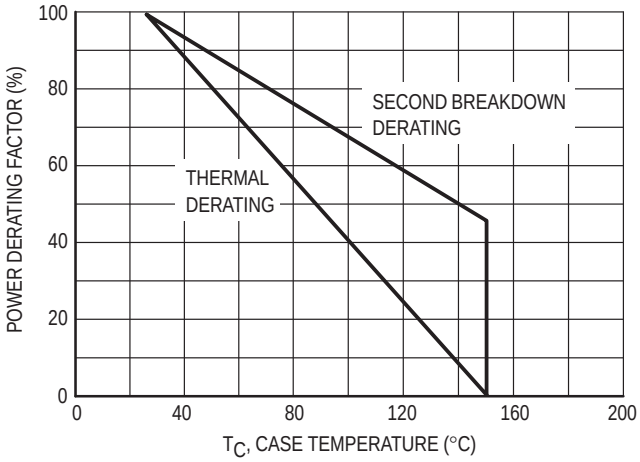


Figure 16. Power Derating

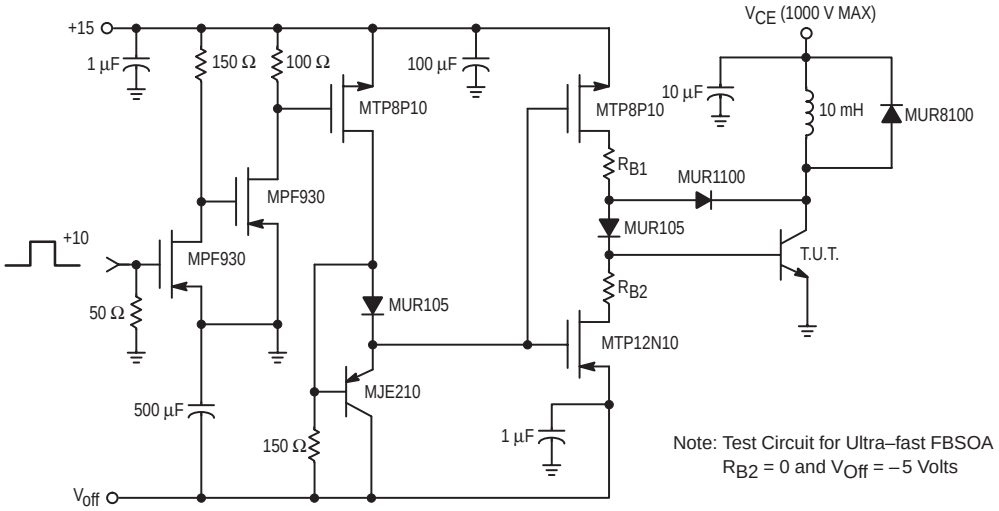


Figure 17. Switching Safe Operating Area

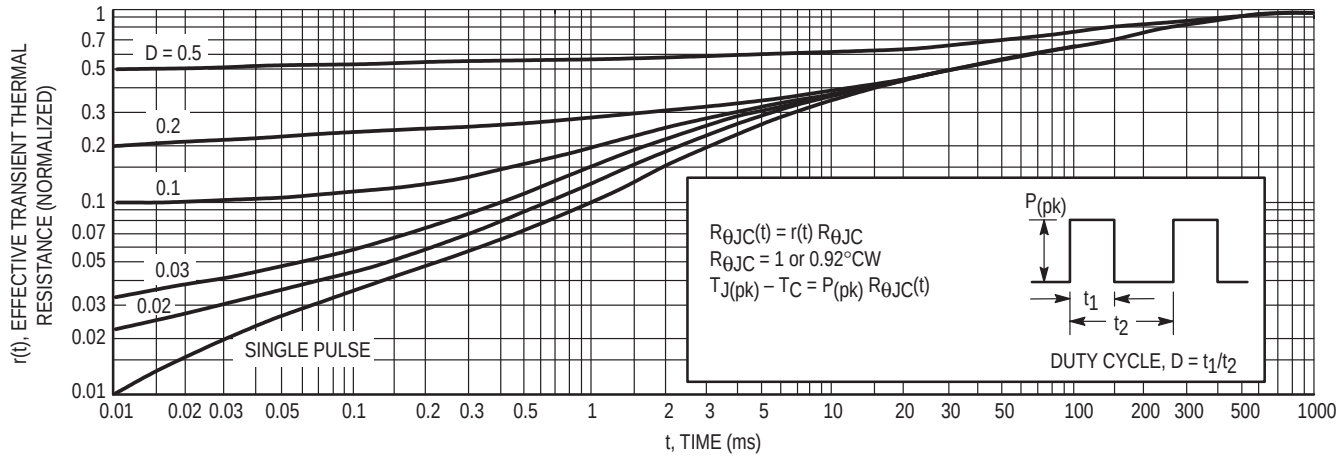


Figure 18. Thermal Response

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 14a and 14b is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 14a and 14b may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

SWITCHMODE DESIGN CONSIDERATIONS

1. FBSOA —

Allowable dc power dissipation in bipolar power transistors decreases dramatically with increasing collector–emitter voltage. A transistor which safely dissipates 100 watts at 10 volts will typically dissipate less than 10 watts at its rated $V_{CEO(sus)}$. From a power handling point of view, current and voltage are not interchangeable (see Application Note AN875).

2. TURN–ON —

Safe turn–on load line excursions are bounded by pulsed FBSOA curves. The 10 μs curve applies for resistive loads, most capacitive loads, and inductive loads that are clamped by standard or fast recovery rectifiers. Similarly, the 100 ns curve applies to inductive loads which are clamped by ultra–fast recovery rectifiers, and are valid for turn–on crossover times less than 100 ns (see Application Note AN952).

At voltages above 75% of $V_{CEO(sus)}$, it is essential to provide the transistor with an adequate amount of base drive VERY RAPIDLY at turn–on. More specifically, safe operation according to the curves is dependent upon base current rise time being less than collector current rise time. As a general rule, a base drive compliance voltage in excess of 10 volts is required to meet this condition (see Application Note AN875).

3. TURN–OFF —

A bipolar transistor's ability to withstand turn–off stress is dependent upon its forward base drive. Gross overdrive violates the RBSOA curve and risks transistor failure. For this reason, circuits which use fixed base drive are often more likely to fail at light loads due to heavy overdrive (see Application Note AN875).

4. OPERATION ABOVE $V_{CEO(sus)}$ —

When bipolars are operated above collector–emitter breakdown, base drive is crucial. A rapid application of adequate forward base current is needed for safe turn–on, as is a stiff negative bias needed for safe turn–off. Any hiccup in the base–drive circuitry that even momentarily violates either of these conditions will likely cause the transistor to fail. Therefore, it is important to design the driver so that its output is negative in the absence of anything but a clean crisp input signal (see Application Note AN952).

SWITCHMODE III DESIGN CONSIDERATIONS (Cont.)

5. RBSOA —

Reverse Biased Safe Operating Area has a first order dependency on circuit configuration and drive parameters. The RBSOA curves in this data sheet are valid only for the conditions specified. For a comparison of RBSOA results in several types of circuits (see Application Note AN951).

6. DESIGN SAMPLES —

Transistor parameters tend to vary much more from wafer lot to wafer lot, over long periods of time, than from one device to the next in the same wafer lot. For design evaluation it is advisable to use transistors from several different date codes.

7. BAKER CLAMPS —

Many unanticipated pitfalls can be avoided by using Baker Clamps. MUR105 and MUR1100 diodes are recommended for base drives less than 1 amp. Similarly, MUR405 and MUR4100 types are well–suited for higher drive requirements (see Article Reprint AR131).

MJW16206

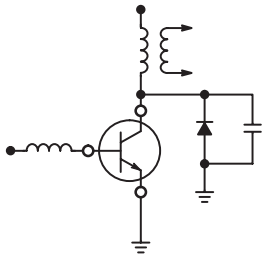
SCANSWITCH™

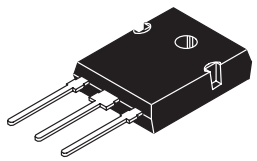
NPN Bipolar Power Deflection Transistors For High and Very High Resolution CRT Monitors

POWER TRANSISTORS
12 AMPERES
1200 VOLTS — V_{CES}
50 and 150 WATTS

The MJF16206 and the MJW16206 are state–of–the–art SWITCHMODE bipolar power transistors. They are specifically designed for use in horizontal deflection circuits for high and very high resolution, monochrome and color CRT monitors.

- **1200 Volt V_{CES} Breakdown Capability**
- Typical Dynamic Desaturation Specified (New Turn–Off Characteristic)
- Maximum Repetitive Emitter–Base Avalanche Energy Specified (Industry First)
- High Current Capability: Performance Specified at 6.5 Amps
  Continuous Rating — 12 Amps Max
  Pulsed Rating — 15 Amps Max
- Isolated MJF16206 is UL Recognized
- Fast Switching: 100 ns Inductive Fall Time (Typ)
  1000 ns Inductive Storage Time (Typ)
- Low Saturation Voltage
  0.25 Volts (Typ) at 6.5 Amps Collector Current
- High Emitter–Base Breakdown Capability For High Voltage Off Drive Circuits — 8.0 V (Min)





CASE 340F–02
TO–247AE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Breakdown Voltage	V_{CES}	**1200**	Vdc
Collector–Emitter Sustaining Voltage	$V_{CEO(sus)}$	500	Vdc
Emitter–Base Voltage	V_{EBO}	8.0	Vdc
Isolation Voltage (RMS for 1 sec., T_A = 25°C, Figure 19 Relative Humidity ≤ 30%) Figure 20	V_{ISOL}	— —	V_{rms}
Collector Current — Continuous — Pulsed (1)	I_C I_{CM}	12 15	Adc
Base Current — Continuous — Pulsed (1)	I_B I_{BM}	5.0 10	Adc
Repetitive Emitter–Base Avalanche Energy	$W_{(BER)}$	0.2	mjoules
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derated above 25°C	P_D	150 39 1.49	Watts W/°C
Operating and Storage Temperature	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	0.67	°C/W
Lead Temperature for Soldering Purposes 1/8″ from the Case for 5 seconds	T_L	260	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Collector Cutoff Current (V_{CE} = 1200 Vdc, V_{BE} = 0 V) (V_{CE} = 850 Vdc, V_{BE} = 0 V)	I_{CES}	 — —	 — —	 250 25	μAdc
Emitter–Base Leakage (V_{EB} = 8.0 Vdc, I_C = 0)	I_{EBO}	—	—	25	μAdc
Collector–Emitter Sustaining Voltage (Figure 10) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	500	—	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 1.0 mA, I_C = 0)	$V_{(BR)EBO}$	8.0	11	—	Vdc
ON CHARACTERISTICS (1)					
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 400 mAdc) (I_C = 6.5 Adc, I_B = 1.5 Adc)	$V_{CE(sat)}$	 — —	 0.15 0.25	 1.0 1.0	Vdc
Base–Emitter Saturation Voltage (I_C = 6.5 Adc, I_B = 1.5 Adc)	$V_{BE(sat)}$	—	0.9	1.5	Vdc
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc) (I_C = 10 Adc, V_{CE} = 5.0 Vdc) (I_C = 12 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	 — 5.0 3.0	 24 8.0 6.0	 — 13 —	—
DYNAMIC CHARACTERISTICS					
Dynamic Desaturation Interval (Figure 15) (I_C = 6.5 Adc, I_B = 1.5 Adc, L_B = 0.5 μH)	t_{ds}	—	250	—	ns
Emitter–Base Avalanche Turn–off Energy (Figure 15) (t = 500 ns, R_{BE} = 22 Ω)	$EB_{(off)}$	—	30	—	μjoules
Output Capacitance (V_{CE} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	—	180	350	pF
Gain Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.5 A, f_{test} = 1.0 MHz)	f_T	—	3.0	—	MHz
Collector–Heatsink Capacitance — MJF16206 Isolated Package (Mounted on a 1″ x 2″ x 1/16″ Copper Heatsink, V_{CE} = 0, f_{test} = 100 kHz)	$C_{c–hs}$	—	17	—	pF
SWITCHING CHARACTERISTICS					
Inductive Load (Figure 15) (I_C = 6.5 A, I_B = 1.5 A) Storage Fall Time	 t_{sv} t_{fi}	 — —	 1000 100	 2250 250	ns

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

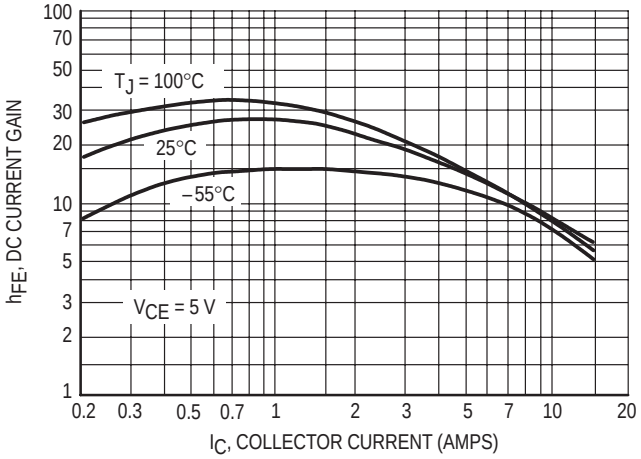


Figure 1. Typical DC Current Gain

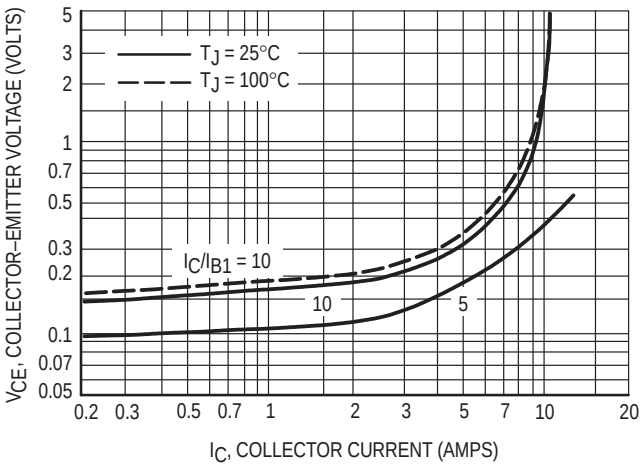


Figure 2. Typical Collector–Emitter Saturation Voltage

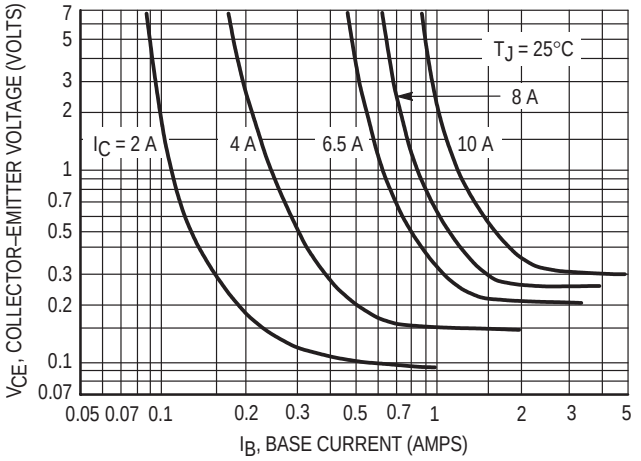


Figure 3. Typical Collector Saturation Region

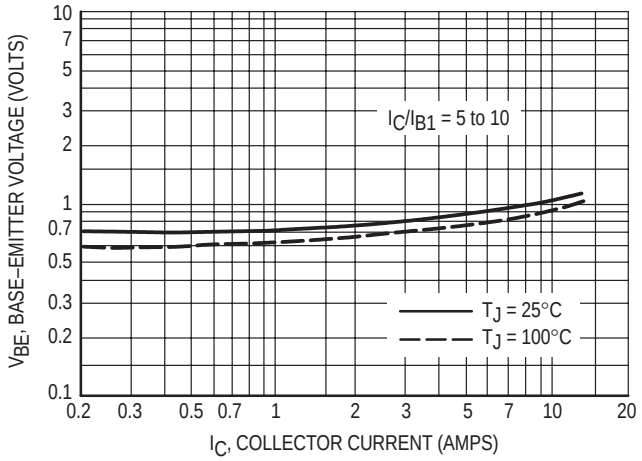


Figure 4. Typical Base–Emitter Saturation Voltage

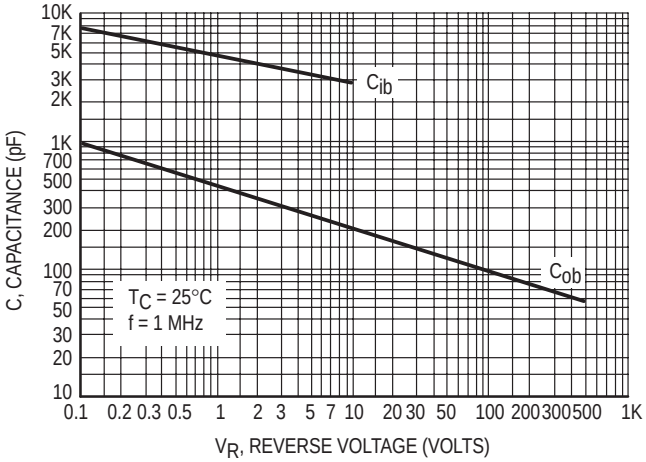


Figure 5. Typical Capacitance

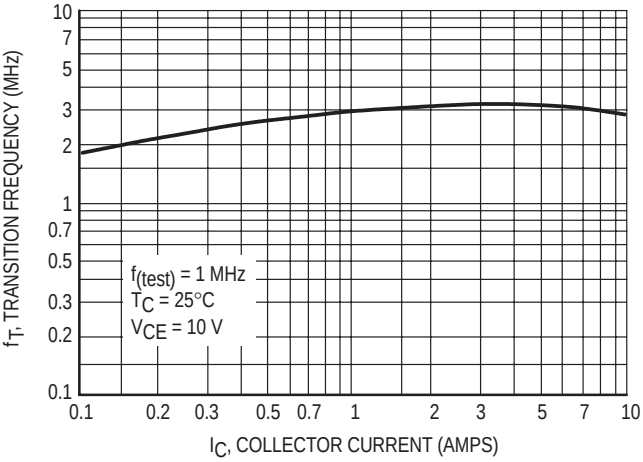
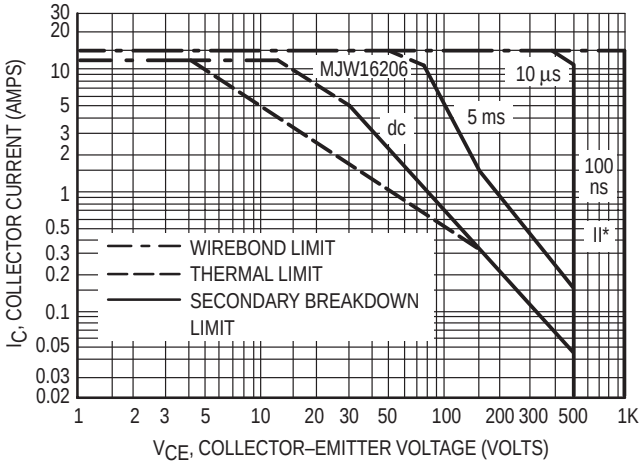


Figure 6. Typical Transition Frequency

SAFE OPERATING AREA INFORMATION



*REGION II — EXPANDED FBSOA USING
MUR8100E, ULTRAFAST RECTIFIER (SEE FIGURE 12)

Figure 7. Maximum Forward Biased Safe Operating Area

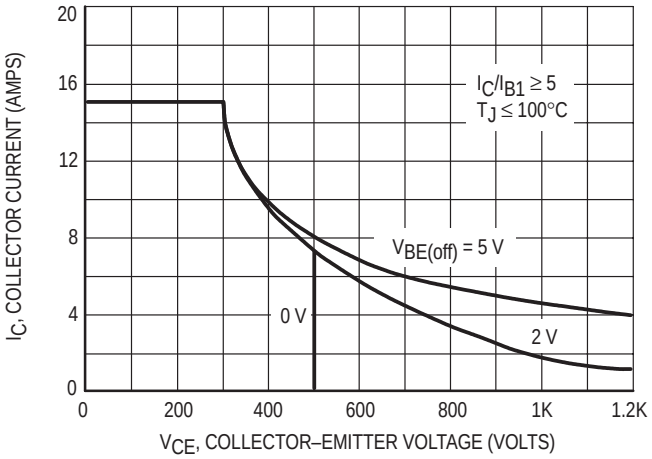


Figure 8. Maximum Reverse Bias Safe Operating Area

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

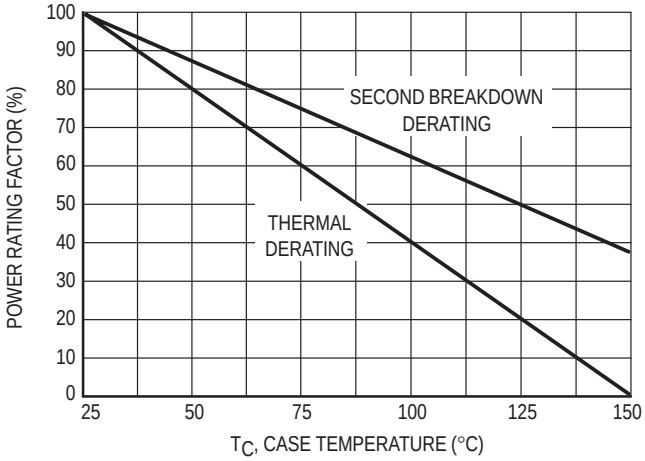


Figure 9. Power Derating

REVERSE BIAS

Inductive loads, in most cases, require the emitter–to–base junction be reversed biased because high voltage and high current must be sustained simultaneously during turn–off. Under these conditions, the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 8 gives the RBSOA characteristics.

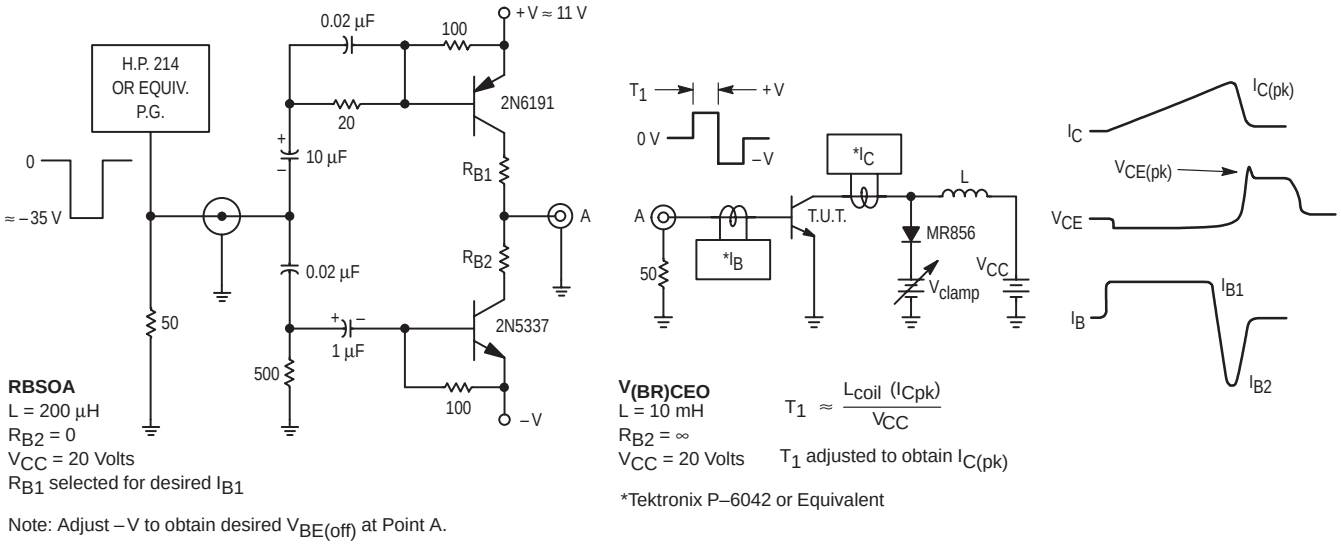


Figure 10. RBSOA/$V_{(BR)CEO(sus)}$ Test Circuit

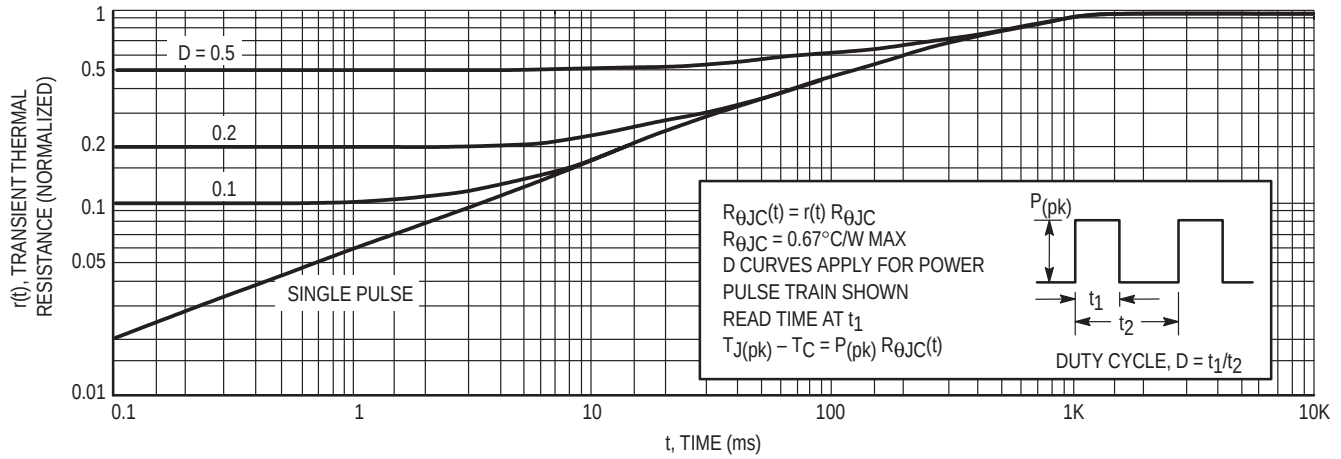


Figure 11. Thermal Response

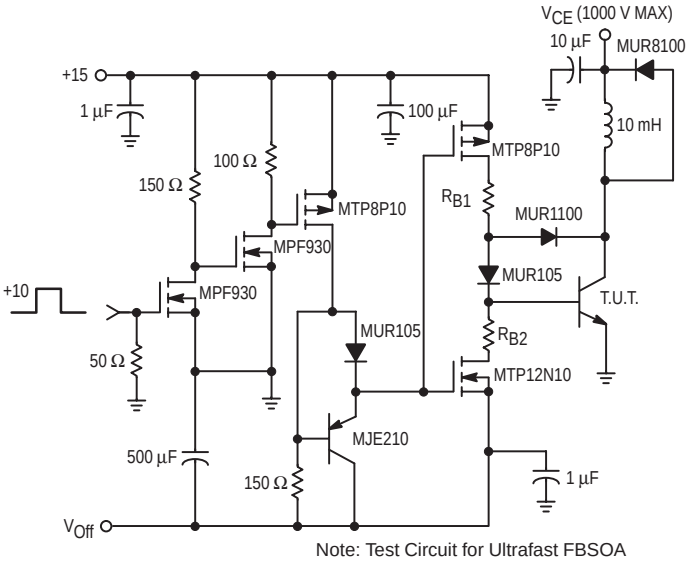


Figure 12. Switching Safe Operating Area

DYNAMIC DESATURATION

The SCANSWITCH series of bipolar power transistors are specifically designed to meet the unique requirements of horizontal deflection circuits in computer monitor applications. Historically, deflection transistor design was focused on minimizing collector current fall time. While fall time is a valid figure of merit, a more important indicator of circuit performance as scan rates are increased is a new characteristic, “dynamic desaturation.” In order to assure a linear collector current ramp, the output transistor must remain in hard saturation during storage time and exhibit a rapid turn–off transition. A sluggish transition results in serious consequences. As the saturation voltage of the output transistor increases, the voltage across the yoke drops. Roll off in the collector current ramp results in improper beam deflection and distortion of the image at the right edge of the screen. Design changes have been made in the structure of the SCANSWITCH series of devices which minimize the dynamic desaturation interval. Dynamic desaturation has been defined in terms of the time required for the V_{CE} to rise from 1.0 to 5.0 volts (Figures 13 and 14) and typical performance at optimized drive conditions has been specified. Optimization of device structure results in a linear collector Current ramp, excellent turn–off switching performance, and significantly lower overall power dissipation.

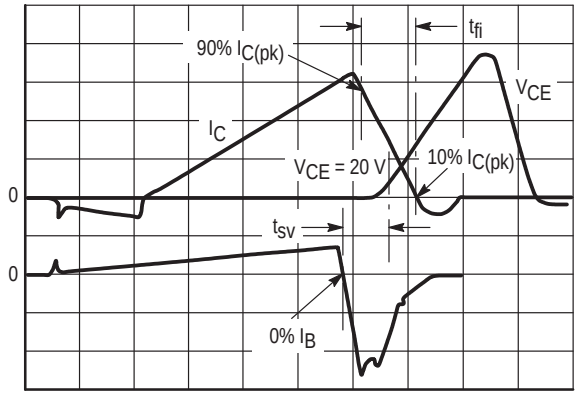


Figure 13. Deflection Simulator Switching Waveforms From Circuit in Figure 15

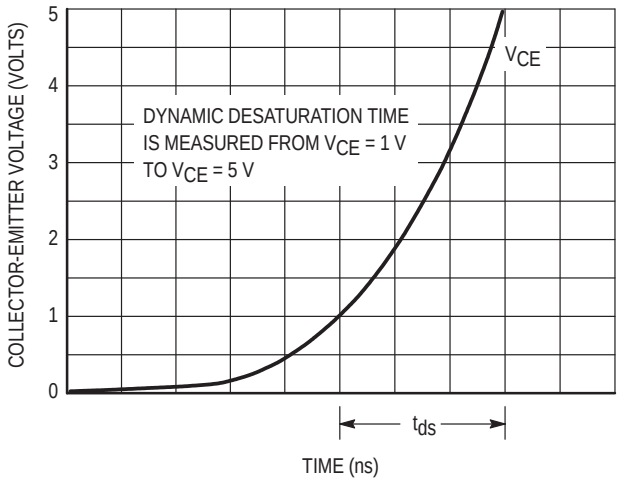


Figure 14. Definition of Dynamic Desaturation Measurement

EMITTER–BASE TURN–OFF ENERGY

Typical techniques for driving horizontal outputs rely on a pulse transformer to supply forward base current, and a turn–off network that includes a series base inductor to limit the rate of transition from forward to reverse drive. An alternate drive scheme has been used to characterize the SCANSWITCH series of devices (see Figure 15). This circuit produces a ramp of base drive, eliminating the heavy overdrive at the beginning of the collector current ramp and underdrive just prior to turnoff produced by typical drive strategies. This high performance drive has two additional important advantages. First, the configuration of T_1 allows L_B to be placed outside the path of forward base current making it unnecessary to expend energy to reverse current flow as in a series base inductor. Second, there is no base resistor to limit forward base current and hence no power loss associated with setting the value of the forward base current. The process of generating the ramp stores rather than dissipates energy. Tailoring the amount of energy stored in T_1 to the amount of energy, $EB_{(off)}$, that is required to turn–off the output transistor results in essentially lossless operation. [Note: B+ and the primary inductance of T_1 (L_P) are chosen such that $1/2\ L_P\ I_b^2 = EB_{(off)}$].

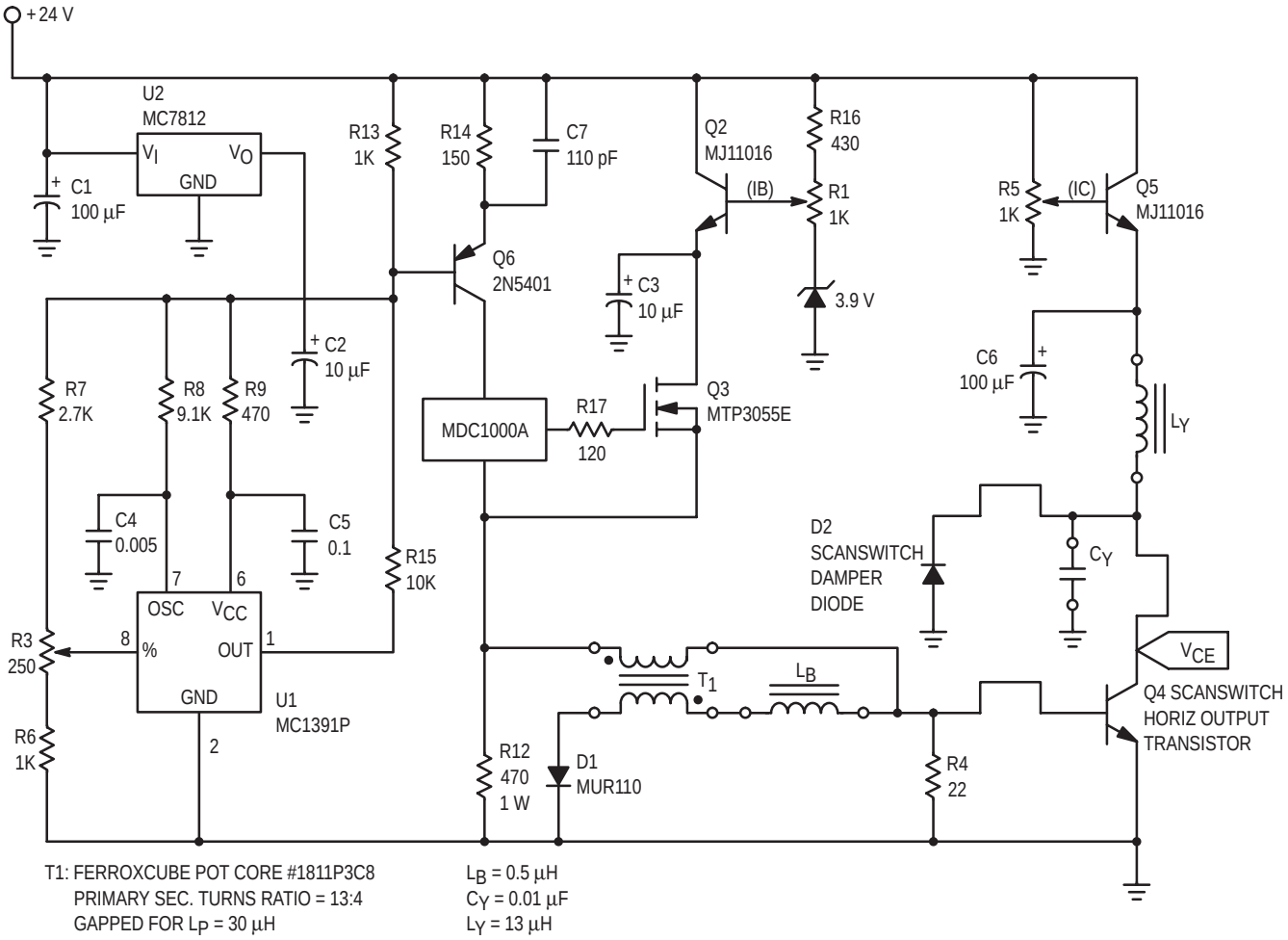
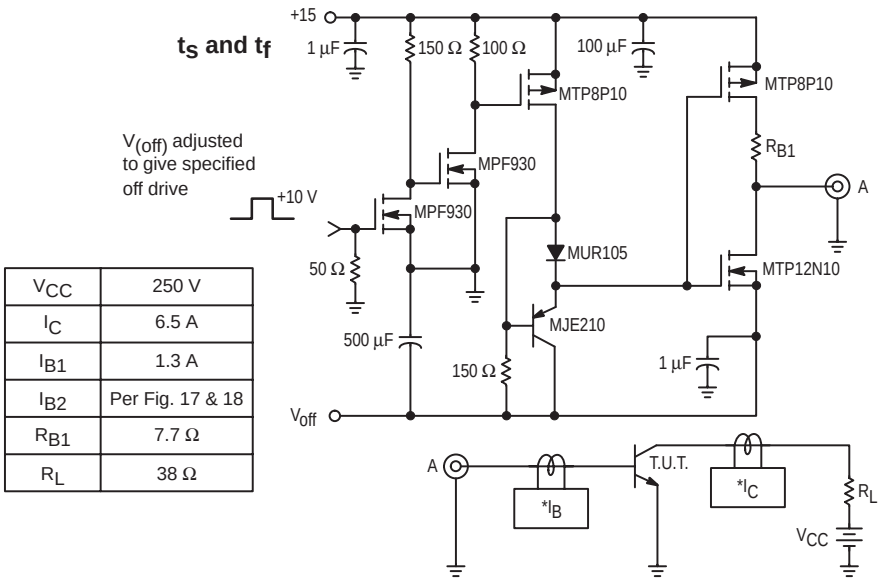


Figure 15. High Resolution Deflection Application Simulator



V_{CC}	250 V
I_C	6.5 A
I_{B1}	1.3 A
I_{B2}	Per Fig. 17 & 18
R_{B1}	7.7 Ω
R_L	38 Ω

Figure 16. Resistive Load Switching

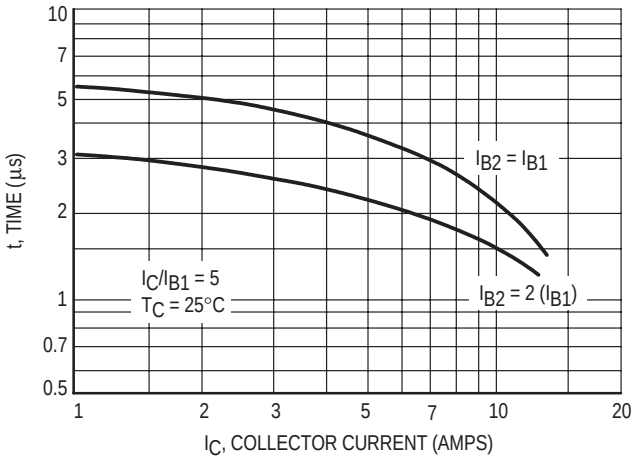


Figure 17. Typical Resistive Storage Time

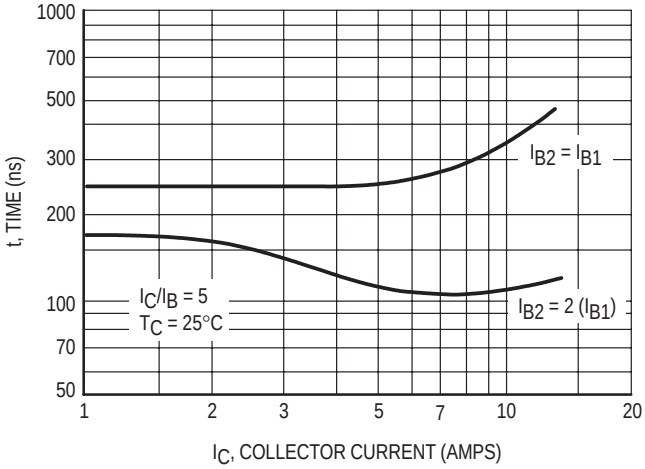


Figure 18. Typical Resistive Fall Time

TEST CONDITIONS FOR ISOLATION TESTS*

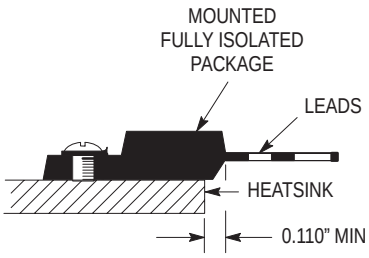


Figure 19. Screw or Clip Mounting Position for Isolation Test Number 1

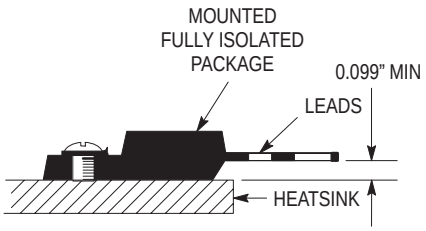
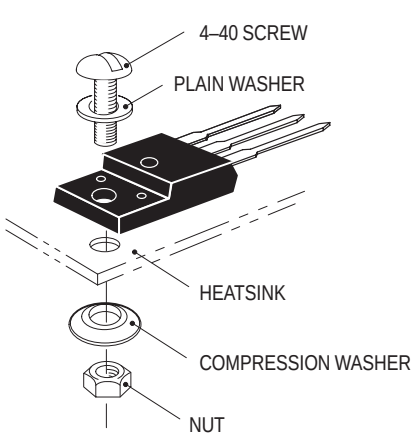


Figure 20. Screw or Clip Mounting Position for Isolation Test Number 2

* Measurement made between leads and heatsink with all leads shorted together.

MOUNTING INFORMATION**



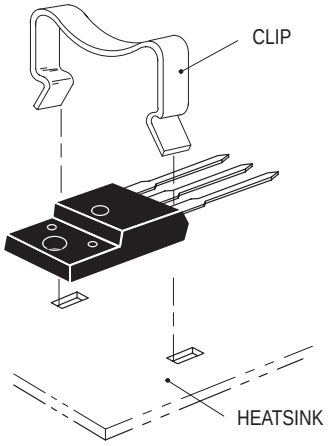


Figure 21. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4-40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4-40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

MJF18002 (See MJE18002)
MJF18004 (See MJE18004)
MJF18006 (See MJE18006)
MJF18008 (See MJE18008)

SCANSWITCH™

NPN Bipolar Power Deflection Transistor For High and Very High Resolution Monitors

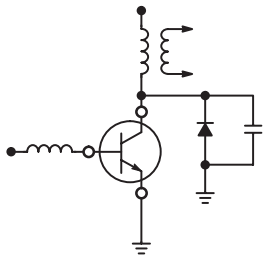
MJW16212*

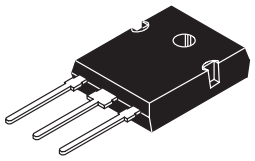
*Motorola Preferred Device

The MJW16212 is a state–of–the–art SWITCHMODE™ bipolar power transistor. It is specifically designed for use in horizontal deflection circuits for 20 mm diameter neck, high and very high resolution, full page, monochrome monitors.

- 1500 Volt Collector–Emitter Breakdown Capability
- Typical Dynamic Desaturation Specified (New Turn–Off Characteristic)
- Application Specific State–of–the–Art Die Design
- Fast Switching:
  200 ns Inductive Fall Time (Typ)
  2000 ns Inductive Storage Time (Typ)
- Low Saturation Voltage:
  0.15 Volts at 5.5 Amps Collector Current and 2.5 A Base Drive
- Low Collector–Emitter Leakage Current — 250 μA Max at 1500 Volts — V_{CES}
- High Emitter–Base Breakdown Capability For High Voltage Off Drive Circuits — 8.0 Volts (Min)

POWER TRANSISTOR
10 AMPERES
1500 VOLTS – V_{CES}
50 AND 150 WATTS





CASE 340F–03
TO–247AE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Breakdown Voltage	V_{CES}	1500	Vdc
Collector–Emitter Sustaining Voltage	$V_{CEO(sus)}$	650	Vdc
Emitter–Base Voltage	V_{EBO}	8.0	Vdc
RMS Isolation Voltage (2) (for 1 sec, T_A = 25°C, Per Fig. 14 Rel. Humidity < 30%) Per Fig. 15	V_{ISOL}	 — —	V
Collector Current — Continuous — Pulsed (1)	I_C I_{CM}	10 15	Adc
Base Current — Continuous — Pulsed (1)	I_B I_{BM}	5.0 10	Adc
Maximum Repetitive Emitter–Base Avalanche Energy	W (BER)	0.2	mJ
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derated above T_C = 25°C	P_D	150 39 1.49	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	0.67	°C/W
Lead Temperature for Soldering Purposes 1/8″ from the case for 5 seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
(2) Proper strike and creepage distance must be provided.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)					
Collector Cutoff Current (V_{CE} = 1500 V, V_{BE} = 0 V) (V_{CE} = 1200 V, V_{BE} = 0 V)	I_{CES}	— —	— —	250 25	μAdc
Emitter–Base Leakage (V_{EB} = 8.0 Vdc, I_C = 0)	I_{EBO}	—	—	25	μAdc
Emitter–Base Breakdown Voltage (I_E = 1.0 mA, I_C = 0)	$V_{(BR)EBO}$	8.0	11	—	Vdc
Collector–Emitter Sustaining Voltage (Table 1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	650	—	—	Vdc
ON CHARACTERISTICS (2)					
Collector–Emitter Saturation Voltage (I_C = 5.5 Adc, I_B = 2.2 Adc) (I_C = 3.0 Adc, I_B = 400 mAdc)	$V_{CE(sat)}$	— —	0.15 0.14	1.0 1.0	Vdc
Base–Emitter Saturation Voltage (I_C = 5.5 Adc, I_B = 2.2 Adc)	$V_{BE(sat)}$	—	0.9	1.5	Vdc
DC Current Gain (I_C = 1.0 A, V_{CE} = 5.0 Vdc) (I_C = 10 A, V_{CE} = 5.0 Vdc)	h_{FE}	— 4.0	24 6.0	— 10	—
DYNAMIC CHARACTERISTICS					
Dynamic Desaturation Interval (I_C = 5.5 A, I_{B1} = 2.2 A, LB = 1.5 μH)	t_{ds}	—	350	—	ns
Output Capacitance (V_{CE} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)	C_{ob}	—	180	350	pF
Gain Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.5 A, f_{test} = 1.0 MHz)	f_T	—	2.75	—	MHz
Emitter–Base Turn–Off Energy ($EB_{(avalanche)}$ = 500 ns, R_{BE} = 22 Ω)	$EB_{(off)}$	—	35	—	μJ
Collector–Heatsink Capacitance — MJF16212 Isolated Package (Mounted on a 1″ x 2″ x 1/16″ Copper Heatsink, V_{CE} = 0, f_{test} = 100 kHz)	$C_{c–hs}$	—	5.0	—	pF
SWITCHING CHARACTERISTICS					
Inductive Load (I_C = 5.5 A, I_B = 2.2 A), High Resolution Deflection Simulator Circuit Table 2 Storage Fall Time	 t_{sv} t_{fi}	 — —	 2000 200	 4000 350	ns

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

SAFE OPERATING AREA

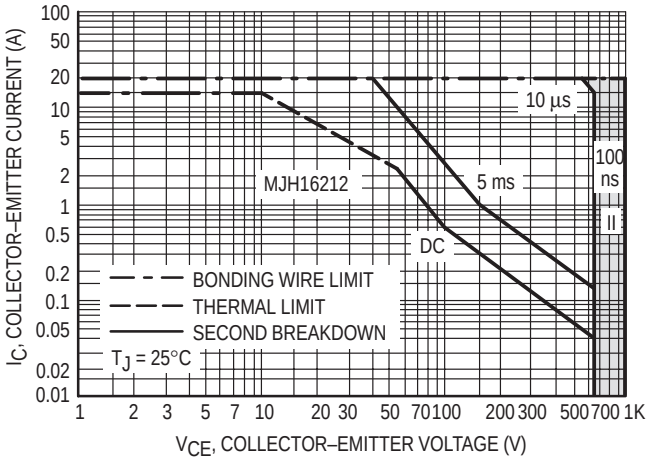


Figure 1. Maximum Forward Bias Safe Operating Area

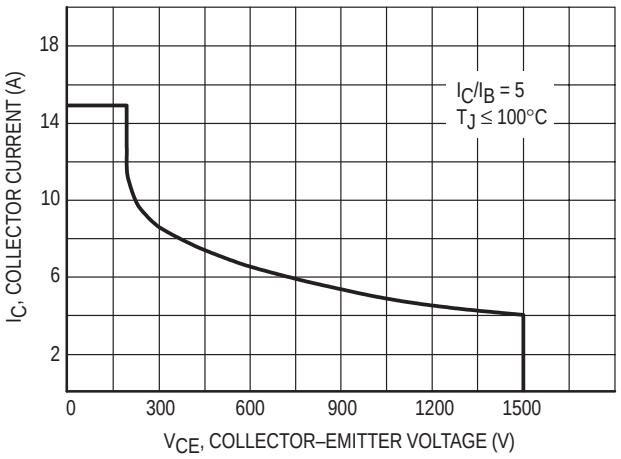


Figure 2. Maximum Reverse Bias Safe Operating Area

SAFE OPERATING AREA (continued)

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

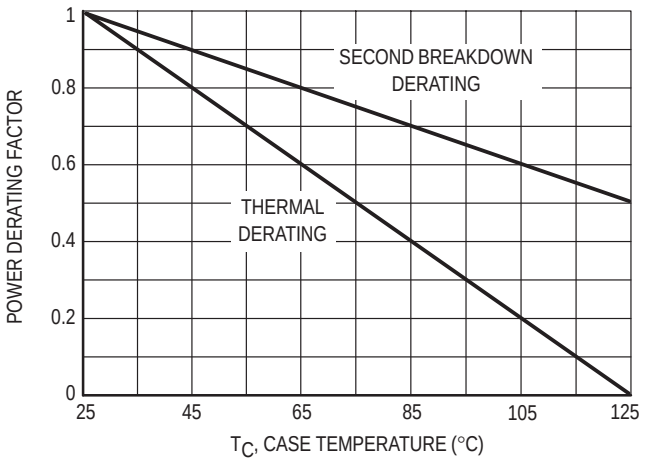


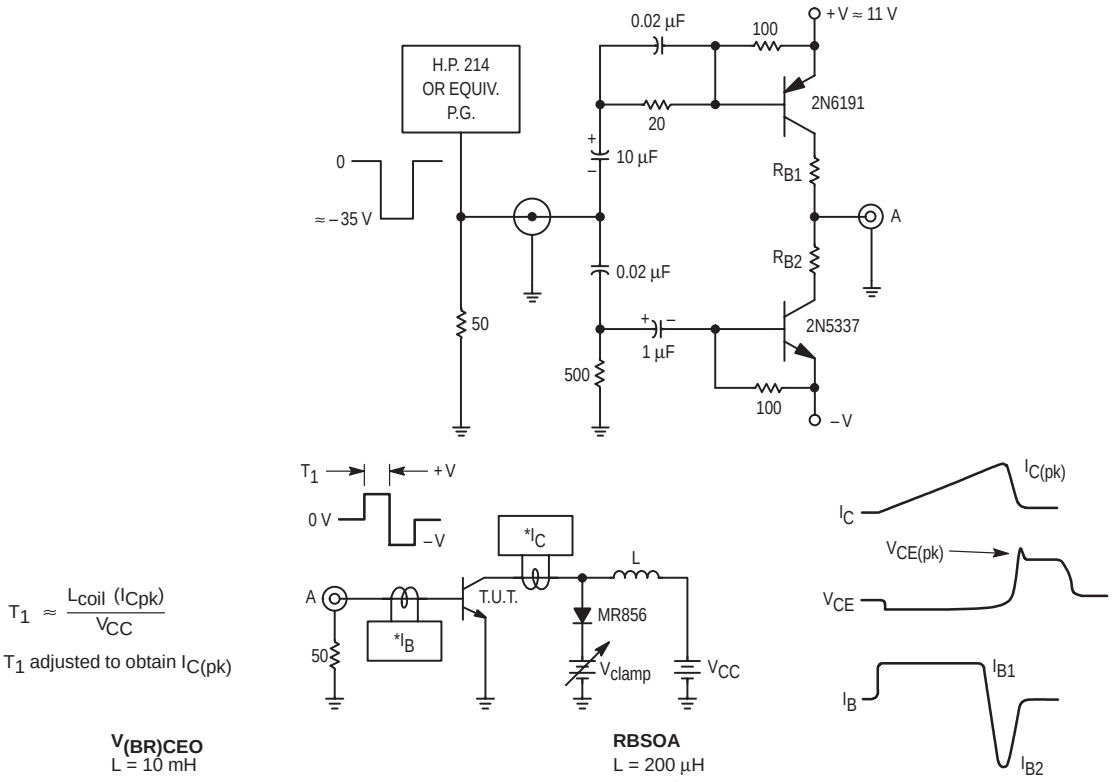
Figure 3. Power Derating

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base–to–emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc.

The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage–current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 2 gives the RBSOA characteristics.

Table 1. RBSOA/$V_{(BR)CEO(SUS)}$ Test Circuit



$$T_1 \approx \frac{L_{coil}\ (I_{Cpk})}{V_{CC}}$$

T_1 adjusted to obtain $I_{C(pk)}$

$V_{(BR)CEO}$
L = 10 mH
$R_{B2} = \infty$
V_{CC} = 20 Volts

*Tektronix
P–6042 or
Equivalent

RBSOA
L = 200 µH
$R_{B2} = 0$
V_{CC} = 20 Volts
R_{B1} selected for desired I_{B1}

Note: Adjust –V to obtain desired $V_{BE(off)}$ at Point A.

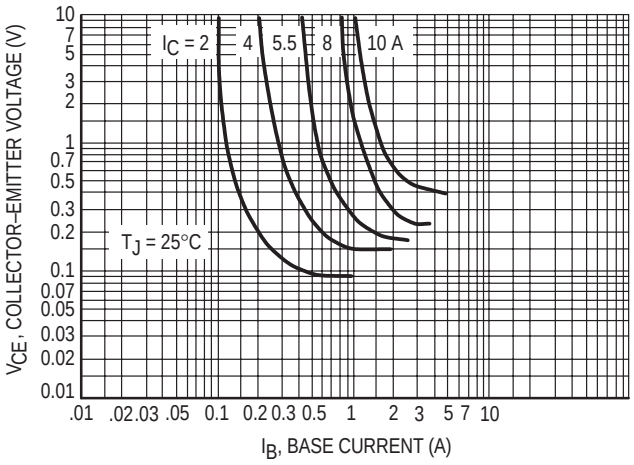


Figure 4. Typical Collector–Emitter Saturation Region

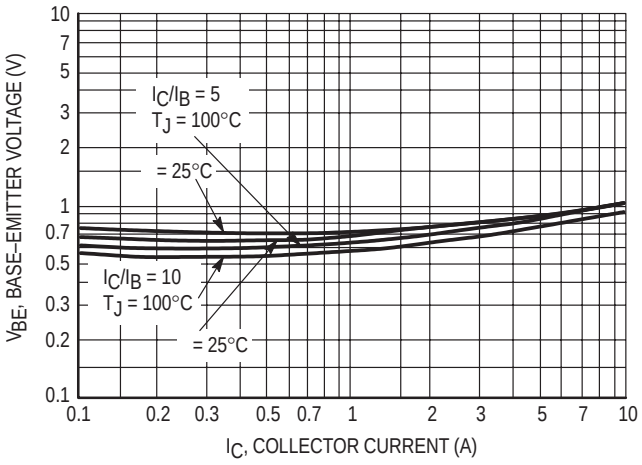


Figure 5. Typical Emitter–Base Saturation Voltage

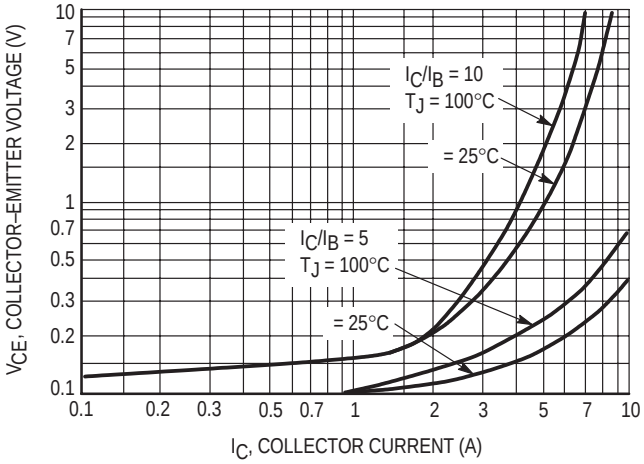


Figure 6. Typical Collector–Emitter Saturation Voltage

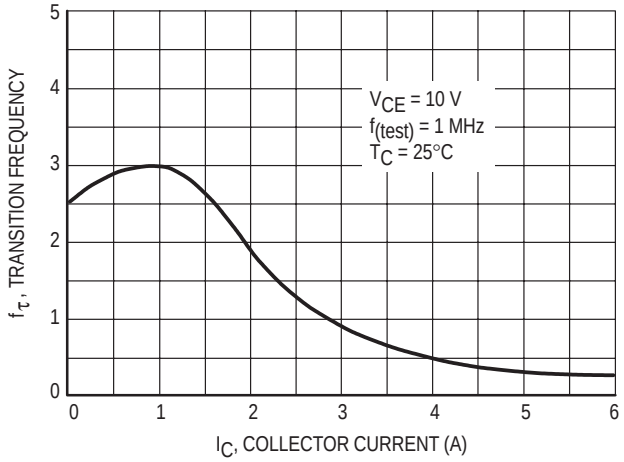


Figure 7. Typical Transition Frequency

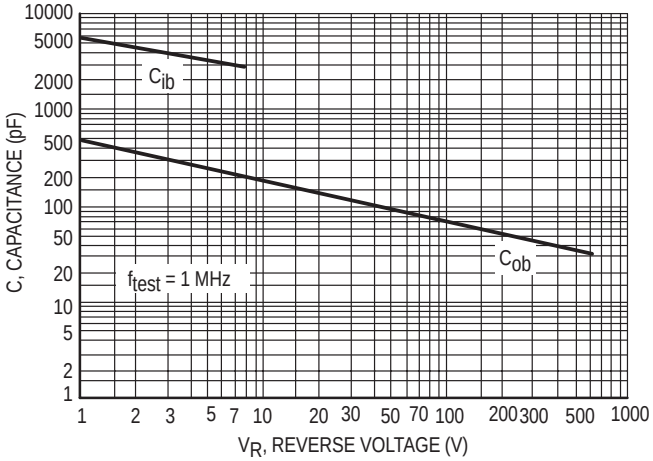
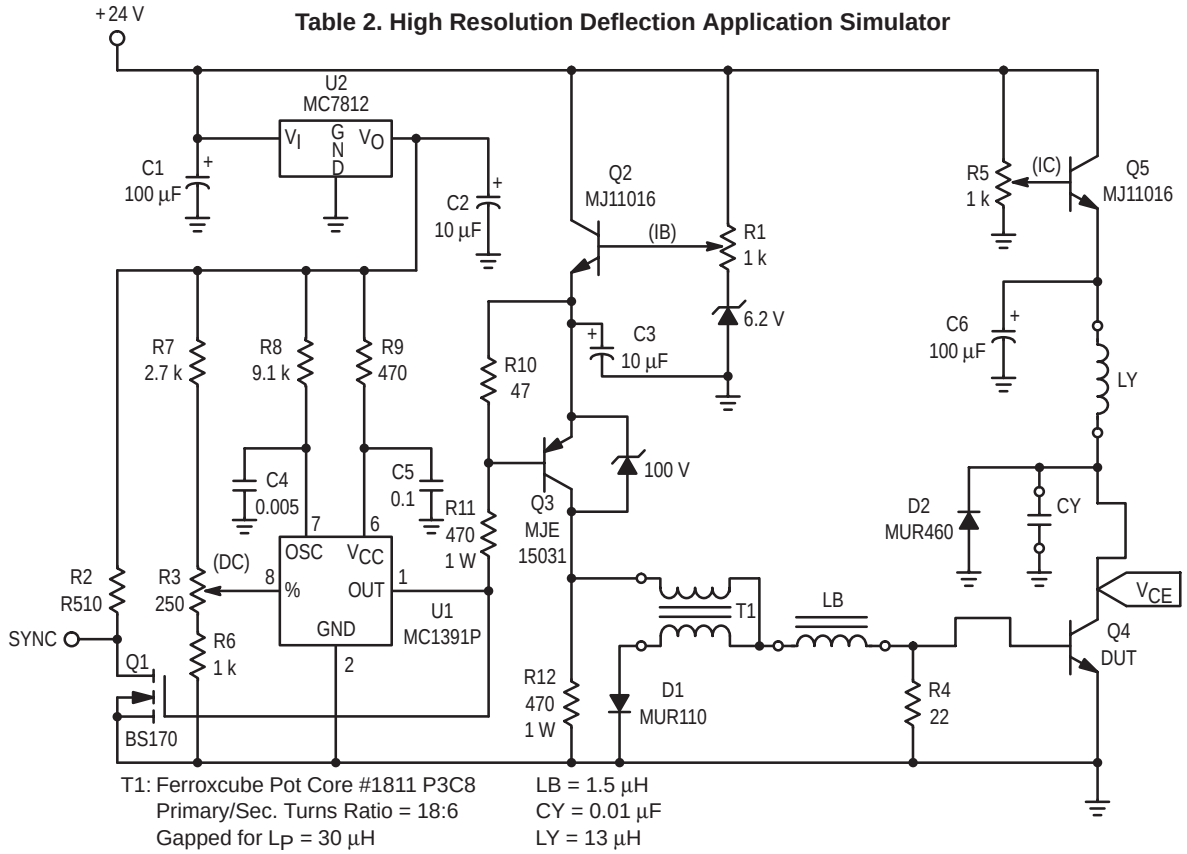


Figure 8. Typical Capacitance

DYNAMIC DESATURATIION

The SCANSWITCH series of bipolar power transistors are specifically designed to meet the unique requirements of horizontal deflection circuits in computer monitor applications. Historically, deflection transistor design was focused on minimizing collector current fall time. While fall time is a valid figure of merit, a more important indicator of circuit performance as scan rates are increased is a new characteristic, “dynamic desaturation.” In order to assure a linear collector current ramp, the output transistor must remain in hard saturation during storage time and exhibit a rapid turn–off transition. A sluggish transition results in serious consequences. As the saturation voltage of the output transistor increases, the voltage across the yoke drops. Roll off in the collector current ramp results in improper beam deflection and distortion of the image at the right edge of the screen. Design changes have been made in the structure of the SCANSWITCH series of devices which minimize the dynamic desaturation interval. Dynamic desaturation has been defined in terms of the time required for the V_{CE} to rise from 1.0 to 5.0 volts (Figures 9 and 10) and typical performance at optimized drive conditions has been specified. Optimization of device structure results in a linear collector current ramp, excellent turn–off switching performance, and significantly lower overall power dissipation.

Table 2. High Resolution Deflection Application Simulator



T1: Ferroxcube Pot Core #1811 P3C8
Primary/Sec. Turns Ratio = 18:6
Gapped for L_P = 30 µH

LB = 1.5 µH
CY = 0.01 µF
LY = 13 µH

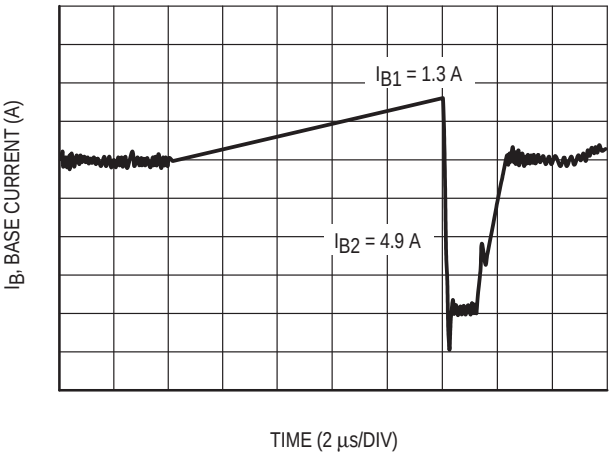


Figure 9. Deflection Simulator Circuit Base Drive Waveform

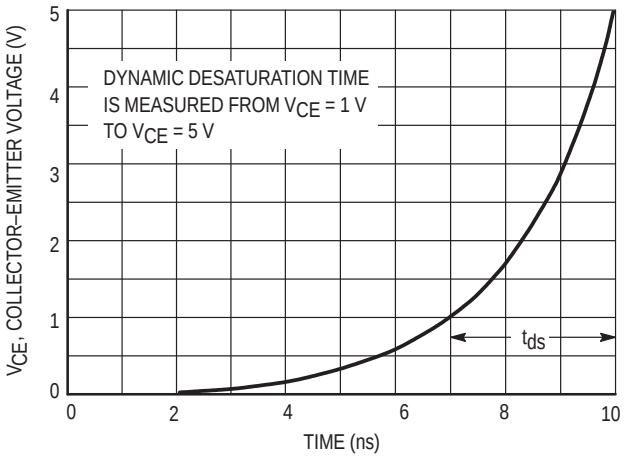


Figure 10. Definition of Dynamic Desaturation Measurement

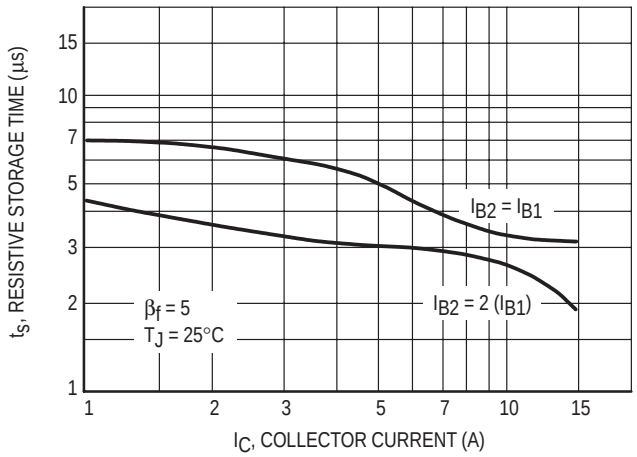


Figure 11. Typical Resistive Storage Time

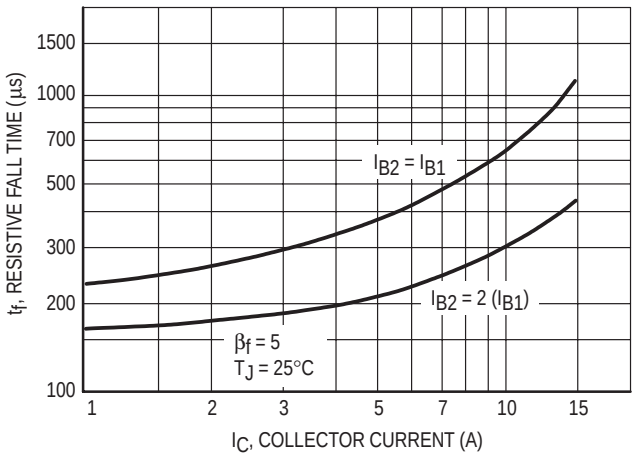
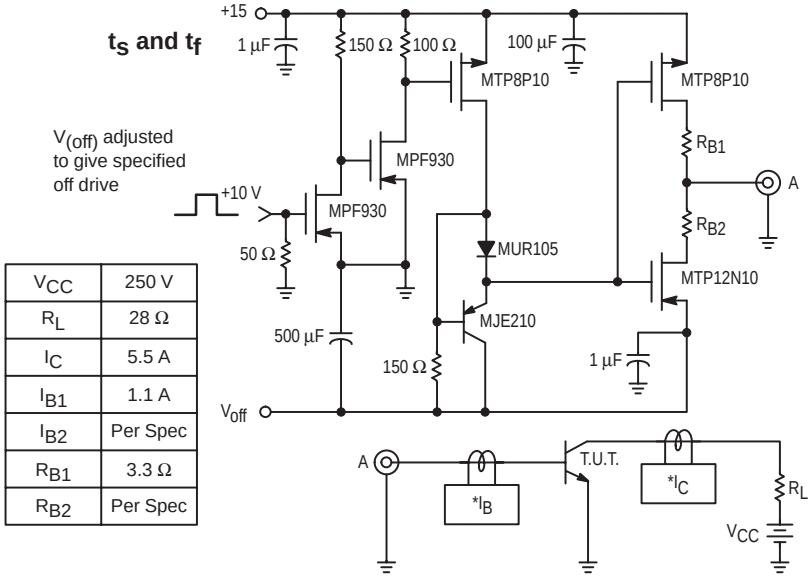


Figure 12. Typical Resistive Fall Time

Table 3. Resistive Load Switching



V_{CC}	250 V
R_L	28 Ω
I_C	5.5 A
I_{B1}	1.1 A
I_{B2}	Per Spec
R_{B1}	3.3 Ω
R_{B2}	Per Spec

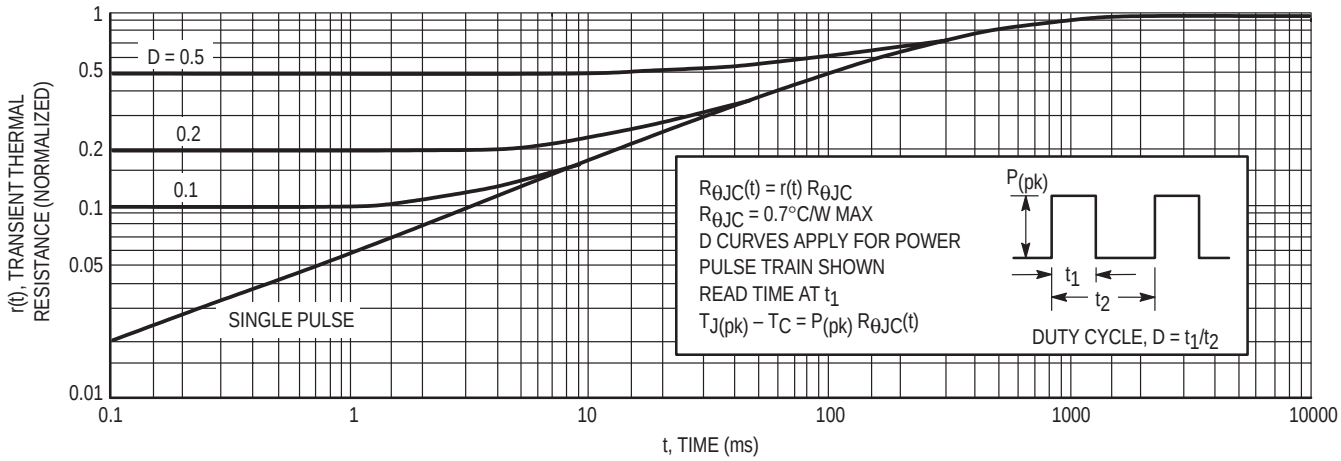


Figure 13. Thermal Response

EMITTER–BASE TURN–OFF ENERGY, $EB_{(off)}$

Emitter–base turn–off energy is a new specification included on the SCANSWITCH data sheets. Typical techniques for driving horizontal outputs rely on a pulse transformer to supply forward base current, and a turnoff network that includes a series base inductor to limit the rate of transition from forward to reverse. An alternate drive scheme has been used to characterize the SCANSWITCH series of devices (see Figure 2). This circuit ramps the base drive to eliminate the heavy overdrive at the beginning of the collector current ramp and underdrive just prior to turn–off observed in typical drive topologies. This high performance drive has two additional important advantages. First, the configuration of T1 allows L_b to be placed outside the path of forward base current making it unnecessary to expend energy to reverse the current flow as in a series based inductor. Second, there is no base resistor to limit forward base current and hence no power loss associated with setting the value of the forward base current. The ramp generating process stores rather than dissipates energy. Tailoring the amount of energy stored in T1 to the amount of energy, $EB_{(off)}$, that is required to turn the output transistor off results in essentially lossless operation. [Note: B+ and the primary inductance of T1 (L_P) are chosen such that $1/2L_PI_b^2 = EB_{(off)}$.]

TEST CONDITIONS FOR ISOLATION TESTS* (MJF16212 ONLY)

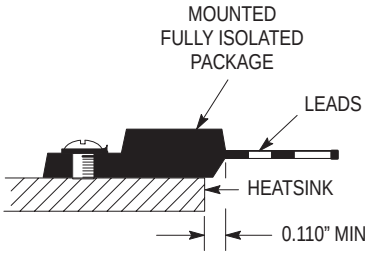


Figure 14. Screw or Clip Mounting Position for Isolation Test Number 1

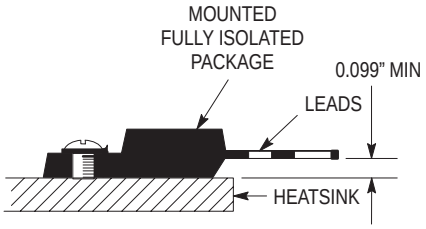


Figure 15. Screw or Clip Mounting Position for Isolation Test Number 2

* Measurement made between leads and heatsink with all leads shorted together

MOUNTING INFORMATION** (MJF16212 ONLY)

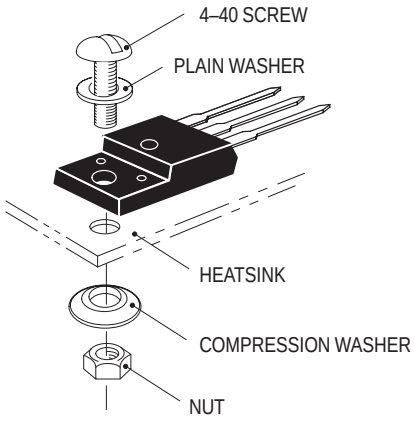


Figure 16a. Screw–Mounted

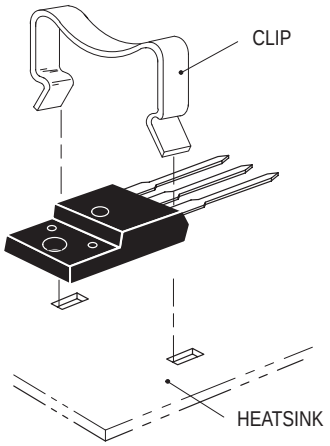


Figure 16b. Clip–Mounted

Figure 16. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4-40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4-40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, Motorola does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

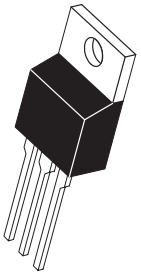
** For more information about mounting power semiconductors see Application Note AN1040.

Complementary Silicon Plastic Power Transistors

. . . designed for use in general purpose amplifier and switching applications. Compact TO–220 AB package.

NPN
TIP29B
TIP29C
PNP
TIP30B
TIP30C

1 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
80 – 100 VOLTS
30 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	TIP29B TIP30B	TIP29C TIP30C	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	1.0 3.0		Adc
Base Current	I_B	0.4		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	30 0.24		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016		Watts W/°C
Unclamped Inductive Load Energy (See Note 3)	E	32		mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	4.167	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP29B, TIP30B TIP29C, TIP30C	$V_{CEO(sus)}$	80 100	— —	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0)		I_{CEO}	—	0.3	mAdc
Collector Cutoff Current (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	 TIP29B, TIP30B TIP29C, TIP30C	I_{CES}	 — —	 200 200	µAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.2 Adc, V_{CE} = 4.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	40 15	— 75	—
Collector–Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 125 mAdc)		$V_{CE(sat)}$	—	0.7	Vdc
Base–Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	1.3	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (2) (I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	3.0	—	MHz
Small–Signal Current Gain (I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	—	—

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$.
(3) This rating based on testing with L_C = 20 mH, R_{BE} = 100 Ω, V_{CC} = 10 V, I_C = 1.8 A, P.R.F = 10 Hz.

REV 1

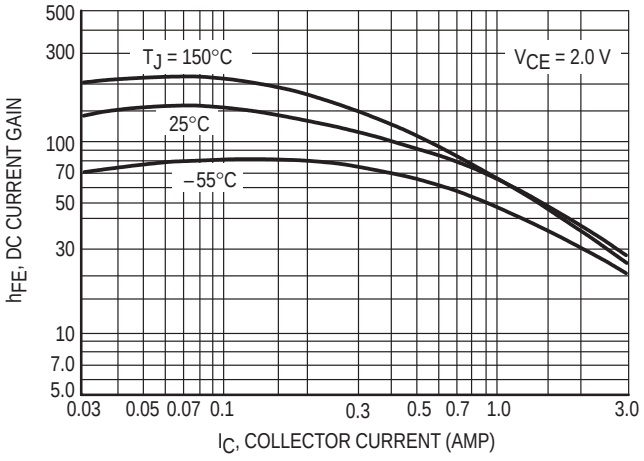


Figure 1. DC Current Gain

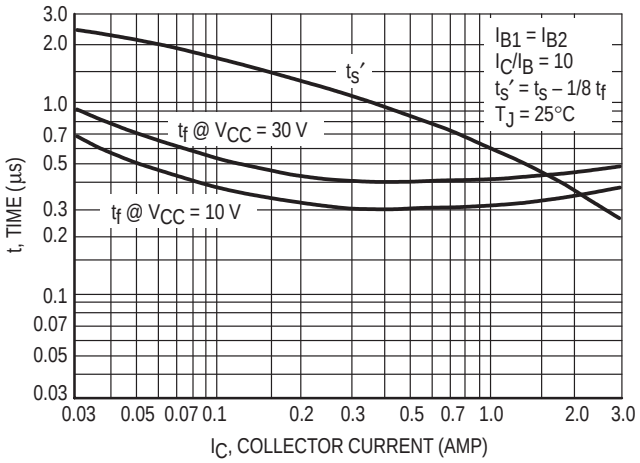


Figure 2. Turn–Off Time

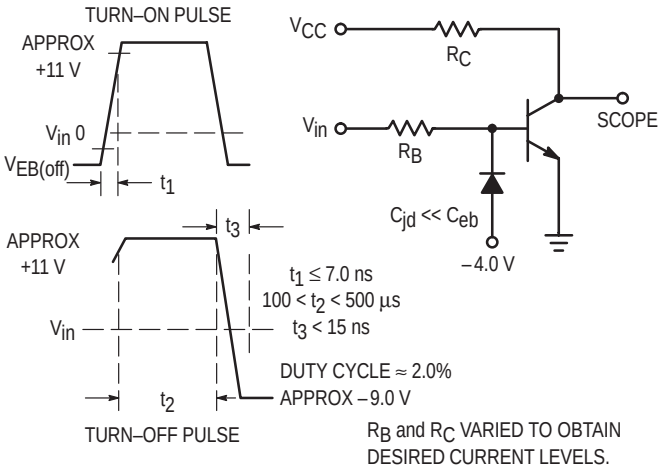


Figure 3. Switching Time Equivalent Circuit

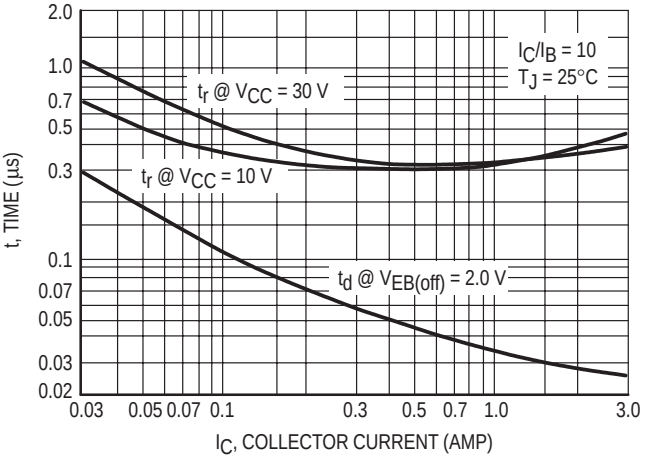


Figure 4. Turn–On Time

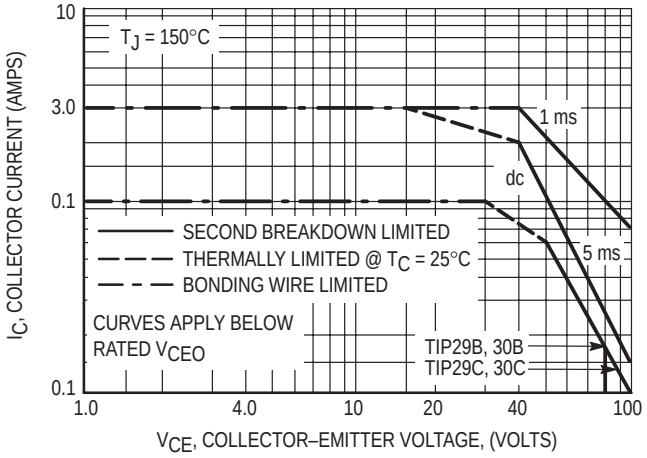


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Complementary Silicon Plastic Power Transistors

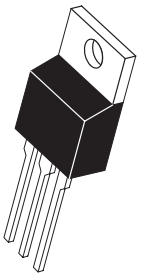
. . . designed for use in general purpose amplifier and switching applications.

- Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.2 Vdc (Max) @ I_C = 3.0 Adc
- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP31A, TIP32A
  = 80 Vdc (Min) — TIP31B, TIP32B
  = 100 Vdc (Min) — TIP31C, TIP32C
- High Current Gain — Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO–220 AB Package

NPN
TIP31A
TIP31B*
TIP31C*
PNP
TIP32A
TIP32B*
TIP32C*

***Motorola Preferred Device**

3 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60 – 80 – 100 VOLTS
40 WATTS



CASE 221A–06
TO–220AB

***MAXIMUM RATINGS**

Rating	Symbol	TIP31A TIP32A	TIP318 TIP32B	TIP31C TIP32C	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	3.0 5.0			Adc
Base Current	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Unclamped Inductive Load Energy (1)	E	32			mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W

(1) I_C = 1.8 A, L = 20 mH, P.R.F. = 10 Hz, V_{CC} = 10 V, R_{BE} = 100 Ω..

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP31A, TIP32A	$V_{CEO(sus)}$	60	—	Vdc
	TIP31B, TIP32B		80	—	
	TIP31C, TIP32C		100	—	
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	TIP31A, TIP32A	I_{CEO}	—	0.3	mAdc
(V_{CE} = 60 Vdc, I_B = 0)	TIP31B, TIP31C		—	0.3	
	TIP32B, TIP32C		—	0.3	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = 60 Vdc, V_{EB} = 0)	TIP31A, TIP32A		—	200	
(V_{CE} = 80 Vdc, V_{EB} = 0)	TIP31B, TIP32B		—	200	
(V_{CE} = 100 Vdc, V_{EB} = 0)	TIP31C, TIP32C		—	200	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	25	—	—
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			10	50	
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 375 mAdc)		$V_{CE(sat)}$	—	1.2	Vdc
Base–Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	1.8	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	3.0	—	MHz
Small–Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

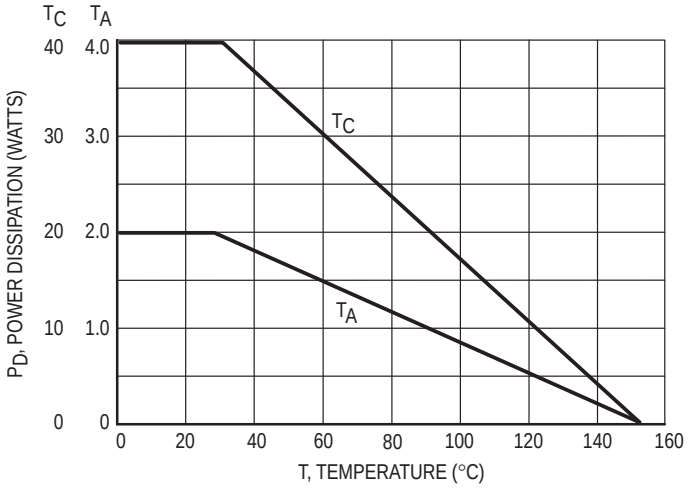


Figure 1. Power Derating

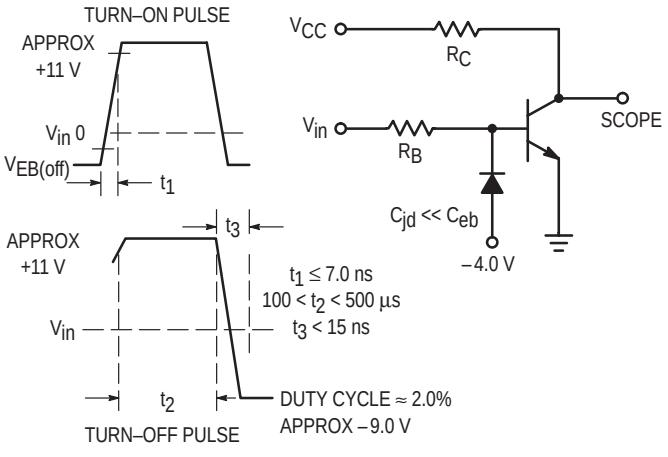


Figure 2. Switching Time Equivalent Circuit

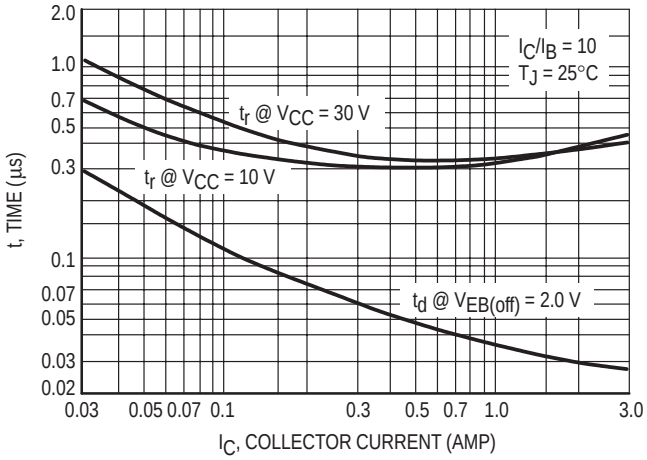


Figure 3. Turn–On Time

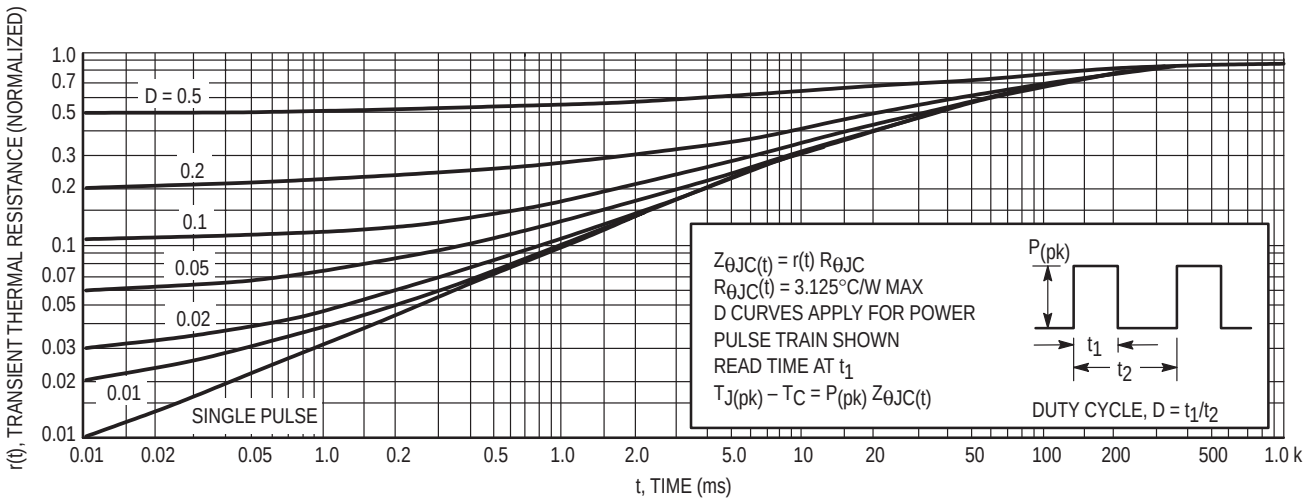


Figure 4. Thermal Response

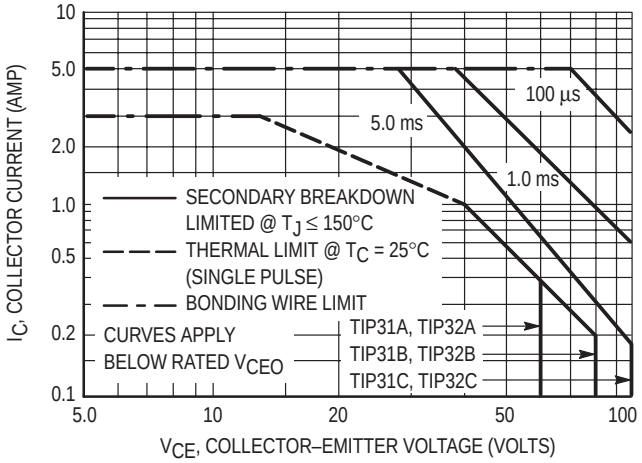


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

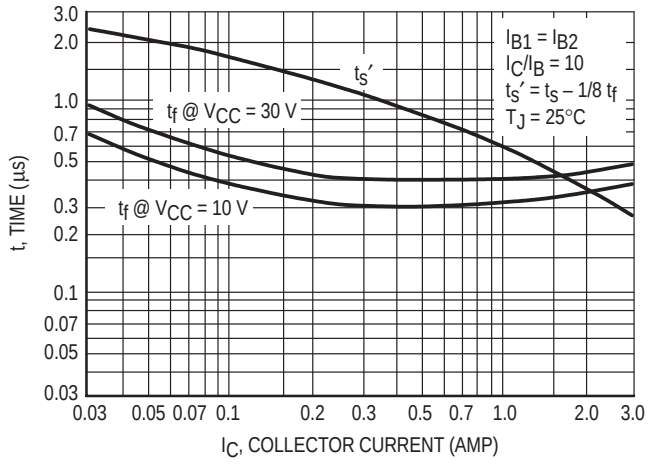


Figure 6. Turn–Off Time

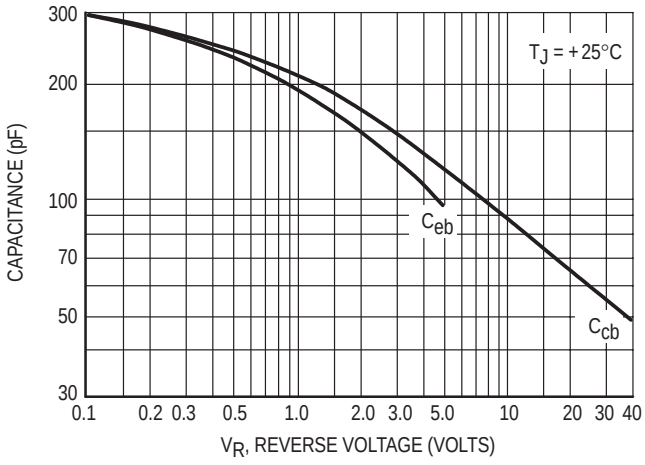


Figure 7. Capacitance

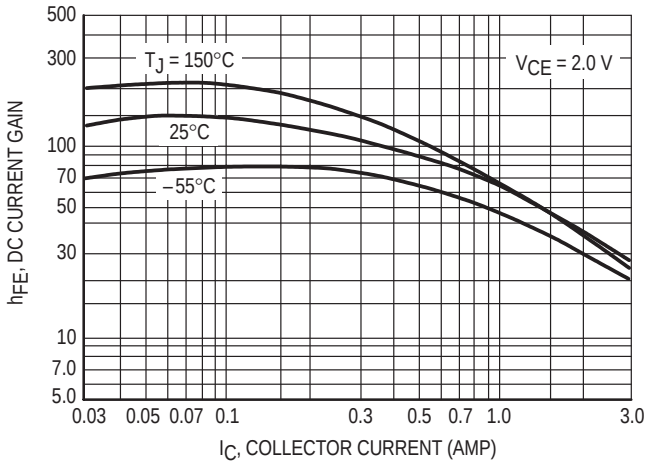


Figure 8. DC Current Gain

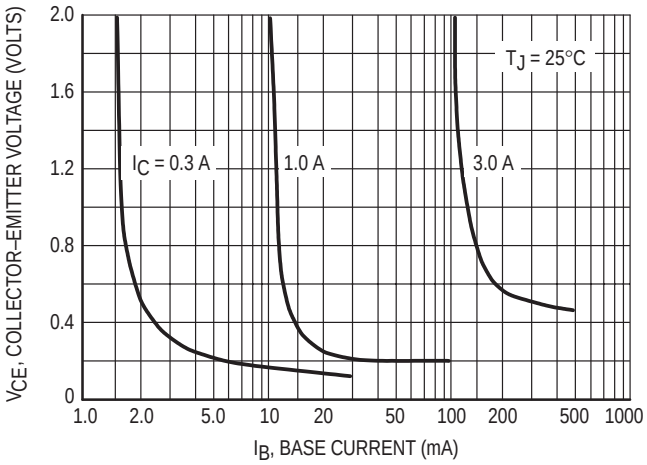


Figure 9. Collector Saturation Region

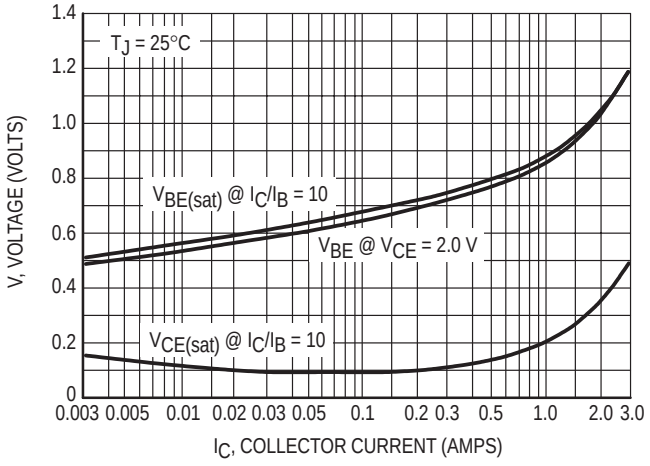


Figure 10. “On” Voltages

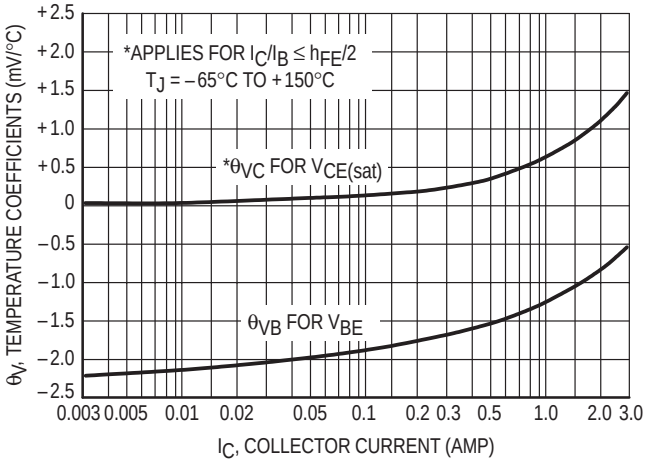


Figure 11. Temperature Coefficients

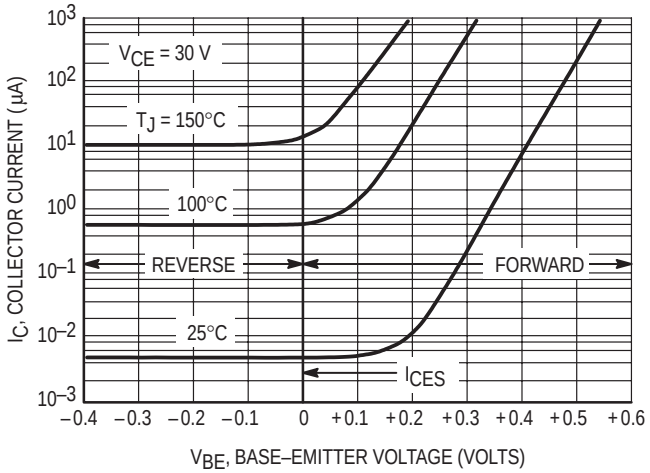


Figure 12. Collector Cut–Off Region

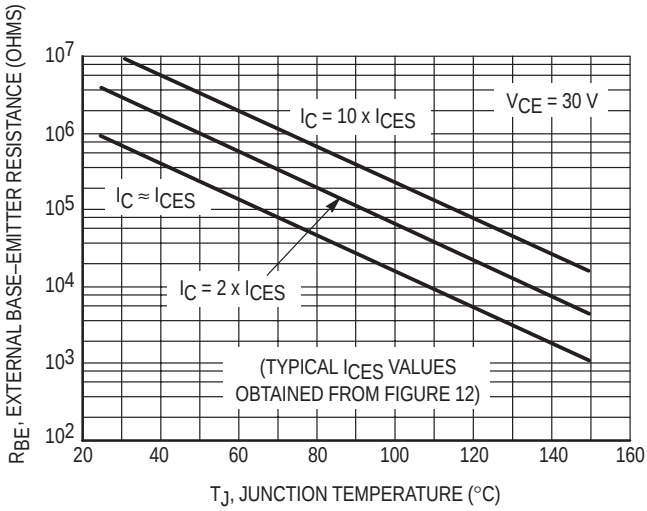


Figure 13. Effects of Base–Emitter Resistance

Complementary Silicon High-Power Transistors

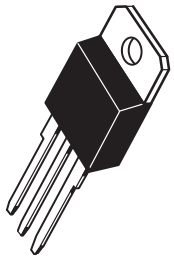
. . . for general–purpose power amplifier and switching applications.

- 10 A Collector Current
- Low Leakage Current — I_{CEO} = 0.7 mA @ 60 V
- Excellent dc Gain — h_{FE} = 40 Typ @ 3.0 A
- High Current Gain Bandwidth Product — h_{fe} = 3.0 min @ I_C = 0.5 A, f = 1.0 MHz

NPN
TIP33B*
TIP33C
PNP
TIP34B*
TIP34C

*Motorola Preferred Device

10 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
100 VOLTS
80 WATTS



CASE 340D–01
TO–218AC

MAXIMUM RATINGS

Rating	Symbol	TIP33B TIP34B	TIP33C TIP34C	Unit
Collector–Emitter Voltage	V_{CEO}	80 V	100 V	Vdc
Collector–Base Voltage	V_{CB}	80 V	100 V	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak (1)	I_C	10 15		Adc
Base Current — Continuous	I_B	3.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.64		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Junction–To–Free–Air Thermal Resistance	$R_{\theta JA}$	35.7	°C/W

(1) Pulse Test: Pulse Width = 10 ms, Duty Cycle ≤ 10%.

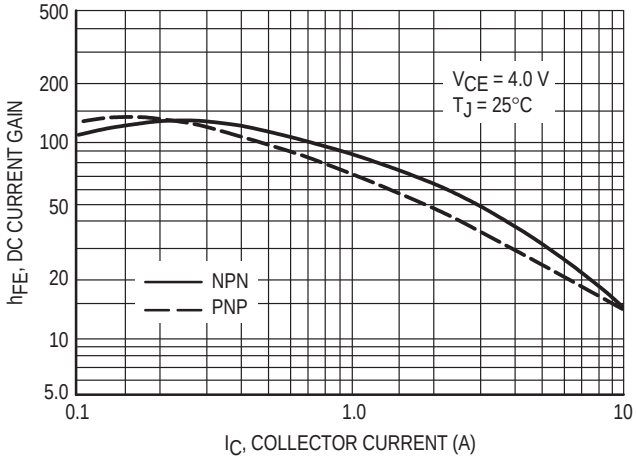


Figure 1. DC Current Gain

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mA, I_B = 0)	TIP33B, TIP34B TIP33C, TIP34C	$V_{CEO(sus)}$	 80 100	 — —	Vdc
Collector–Emitter Cutoff Current (V_{CE} = 60 V, I_B = 0)	TIP33B, TIP33C, TIP34B, TIP34C	I_{CEO}	—	0.7	mA
Collector–Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)		I_{CES}	—	0.4	mA
Emitter–Base Cutoff Current (V_{EB} = 5.0 V, I_C = 0)		I_{EBO}	—	1.0	mA
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 1.0 A, V_{CE} = 4.0 V) (I_C = 3.0 A, V_{CE} = 4.0 V)		h_{FE}	 40 20	 — 100	—
Collector–Emitter Saturation Voltage (I_C = 3.0 A, I_B = 0.3 A) (I_C = 10 A, I_B = 2.5 A)		$V_{CE(sat)}$	 — —	 1.0 4.0	Vdc
Base–Emitter On Voltage (I_C = 3.0 A, V_{CE} = 4.0 V) (I_C = 10 A, V_{CE} = 4.0 V)		$V_{BE(on)}$	 — —	 1.6 3.0	Vdc
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 0.5 A, V_{CE} = 10 V, f = 1.0 kHz)		h_{fe}	20	—	—
Current–Gain — Bandwidth Product (I_C = 0.5 A, V_{CE} = 10 V, f = 1.0 MHz)		f_T	3.0	—	MHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

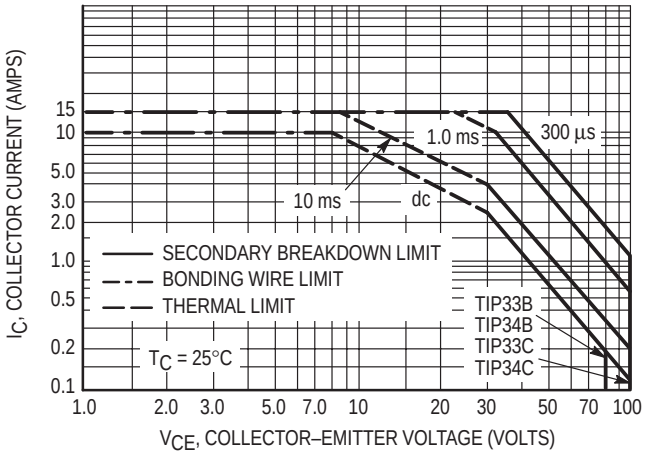


Figure 2. Maximum Rated Forward Bias Safe Operating Area

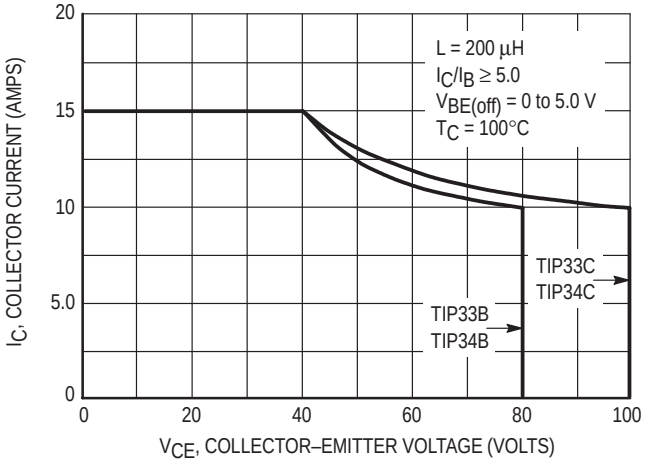


Figure 3. Maximum Rated Forward Bias Safe Operating Area

FORWARD BIAS

The Forward Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during forward bias. The data is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10%, and must be derated thermally for T_C > 25°C.

REVERSE BIAS

The Reverse Bias Safe Operating Area represents the voltage and current conditions these devices can withstand during reverse biased turn–off. This rating is verified under clamped conditions so the device is never subjected to an avalanche mode.

Complementary Silicon High-Power Transistors

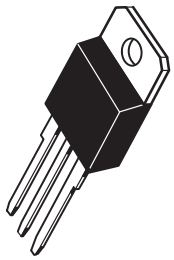
. . . for general–purpose power amplifier and switching applications.

- 25 A Collector Current
- Low Leakage Current — I_{CEO} = 1.0 mA @ 30 and 60 V
- Excellent DC Gain — h_{FE} = 40 Typ @ 15 A
- High Current Gain Bandwidth Product — $|h_{fe}|$ = 3.0 min @ I_C = 1.0 A, f = 1.0 MHz

NPN
TIP35A
TIP35B*
TIP35C*
PNP
TIP36A
TIP36B*
TIP36C*

*Motorola Preferred Device

25 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60–100 VOLTS 125 WATTS



CASE 340D–01
TO–218AC

MAXIMUM RATINGS

Rating	Symbol	TIP35A TIP36A	TIP35B TIP36B	TIP35C TIP36C	Unit
Collector–Emitter Voltage	V_{CEO}	60 V	80 V	100 V	Vdc
Collector–Base Voltage	V_{CB}	60 V	80 V	100 V	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak (1)	I_C	25 40			Adc
Base Current — Continuous	I_B	5.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1.0			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C
Unclamped Inductive Load	E_{SB}	90			mJ

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Junction–To–Free–Air Thermal Resistance	$R_{\theta JA}$	35.7	°C/W

(1) Pulse Test: Pulse Width = 10 ms, Duty Cycle ≤ 10%.

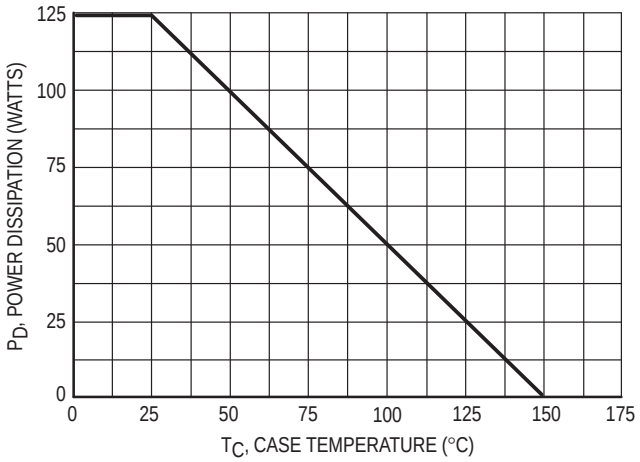


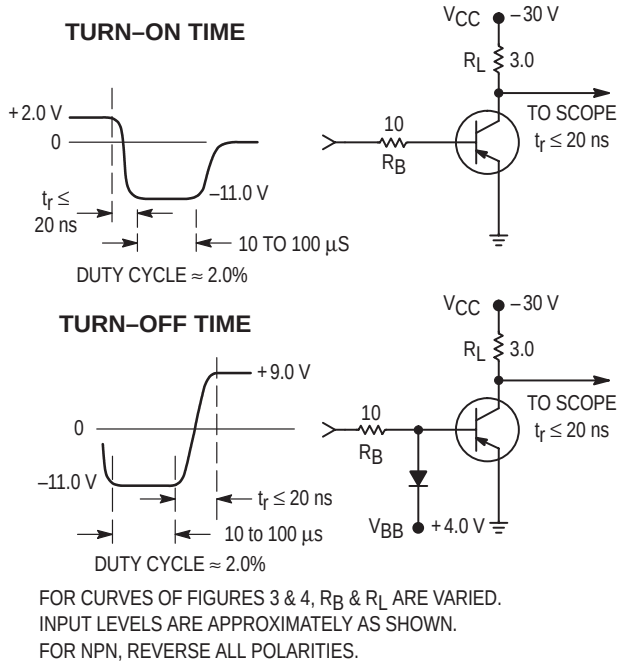
Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mA, I_B = 0)	TIP35A, TIP36A		60	—	
	TIP35B, TIP36B		80	—	
	TIP35C, TIP36C		100	—	
Collector–Emitter Cutoff Current		I_{CEO}			mA
(V_{CE} = 30 V, I_B = 0)	TIP35A, TIP36A		—	1.0	
(V_{CE} = 60 V, I_B = 0)	TIP35B, TIP35C, TIP36B, TIP36C		—	1.0	
Collector–Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)		I_{CES}	—	0.7	mA
Emitter–Base Cutoff Current (V_{EB} = 5.0 V, I_C = 0)		I_{EBO}	—	1.0	mA
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 1.5 A, V_{CE} = 4.0 V)			25	—	
(I_C = 15 A, V_{CE} = 4.0 V)			15	75	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 15 A, I_B = 1.5 A)			—	1.8	
(I_C = 25 A, I_B = 5.0 A)			—	4.0	
Base–Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 15 A, V_{CE} = 4.0 V)			—	2.0	
(I_C = 25 A, V_{CE} = 4.0 V)			—	4.0	
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 kHz)		h_{fe}	25	—	—
Current–Gain — Bandwidth Product (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 MHz)		f_T	3.0	—	MHz

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤ 2.0%.



FOR CURVES OF FIGURES 3 & 4, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN, REVERSE ALL POLARITIES.

Figure 2. Switching Time Equivalent Test Circuits

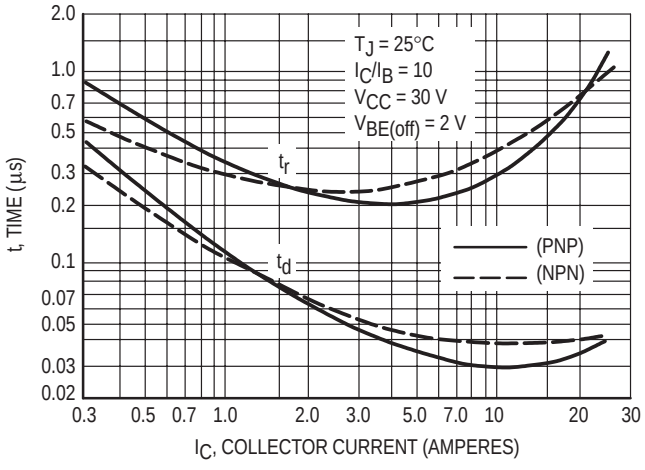


Figure 3. Turn–On Time

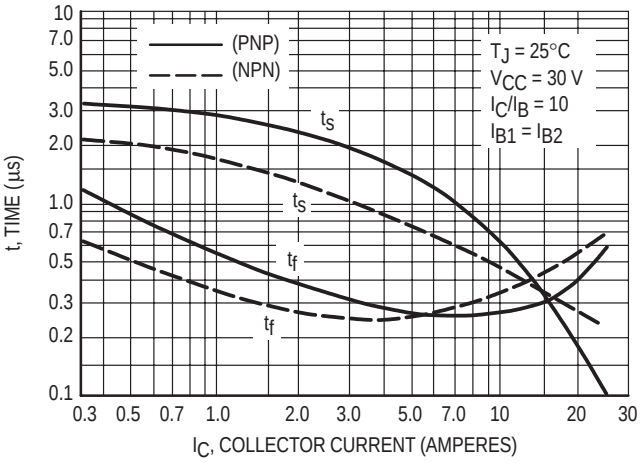


Figure 4. Turn–Off Time

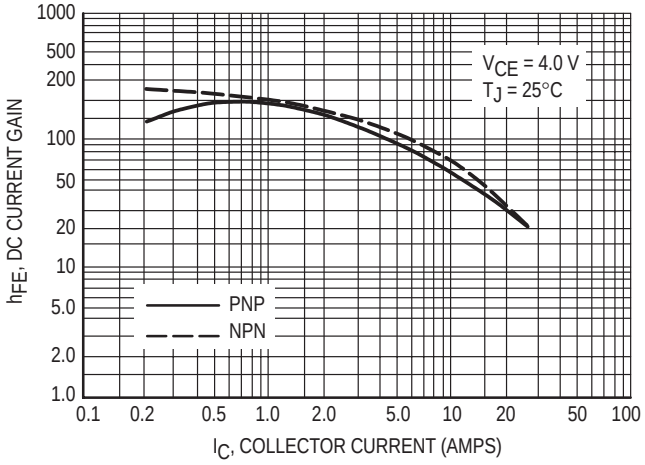


Figure 5. DC Current Gain

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq$ 25°C. Second breakdown limitations do not derate the same as thermal limitations.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives RBSOA characteristics.

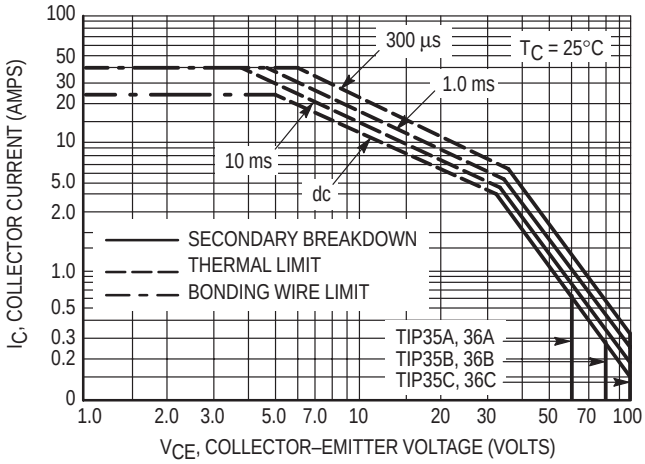


Figure 6. Maximum Rated Forward Bias Safe Operating Area

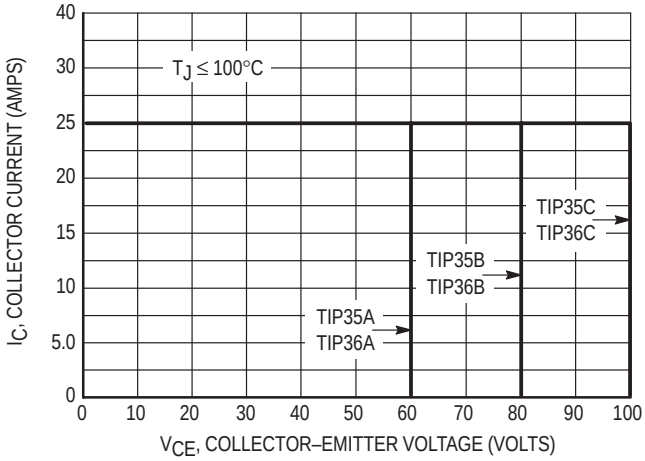
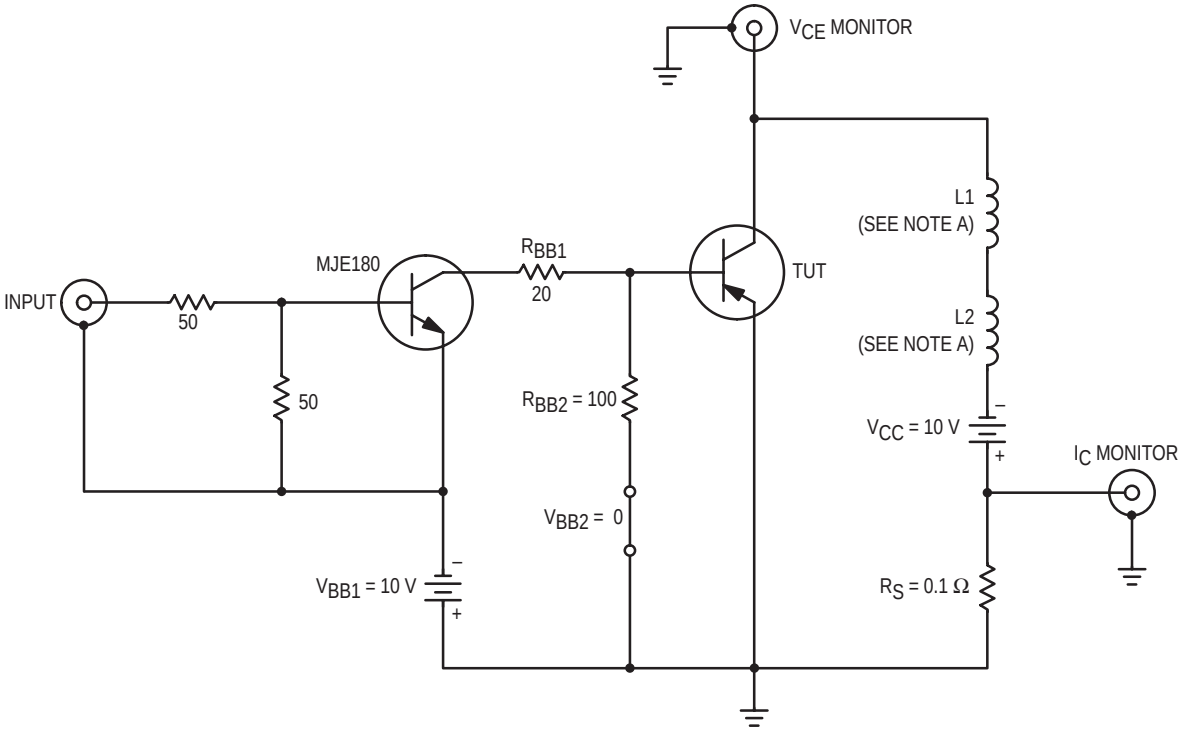
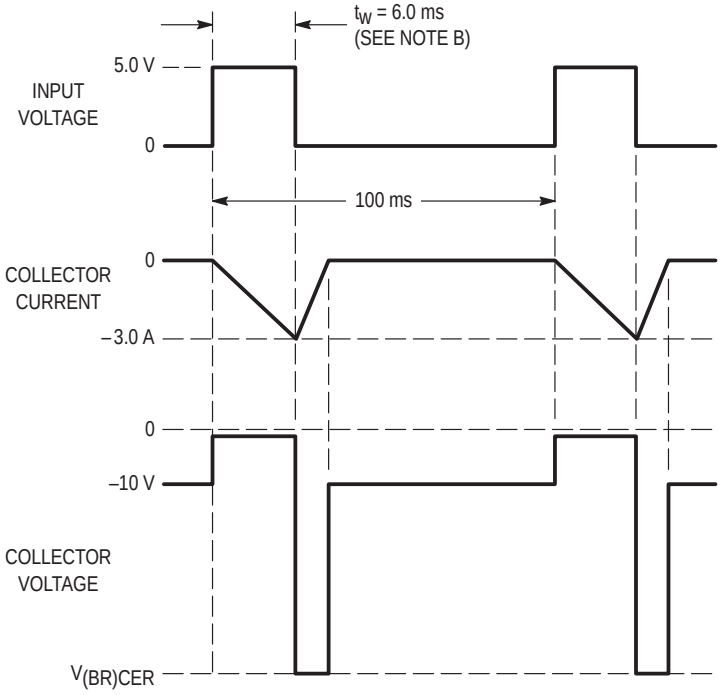


Figure 7. Maximum Rated Forward Bias Safe Operating Area

TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS



NOTES:

A. L1 and L2 are 10 mH, 0.11 Ω, Chicago Standard Transformer Corporation C–2688, or equivalent.
B. Input pulse width is increased until $I_{CM} = -3.0$ A.
C. For NPN, reverse all polarities.

Figure 8. Inductive Load Switching

Complementary Silicon Plastic Power Transistors

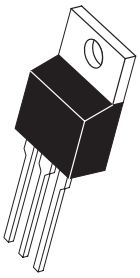
. . . designed for use in general purpose amplifier and switching applications.

- Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.5 Vdc (Max) @ I_C = 6.0 Adc
- Collector–Emitter Sustaining Voltage —
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP41A, TIP42A
  = 80 Vdc (Min) — TIP41B, TIP42B
  = 100 Vdc (Min) — TIP41C, TIP42C
- High Current Gain — Bandwidth Product
  f_T = 3.0 MHz (Min) @ I_C = 500 mAdc
- Compact TO–220 AB Package

NPN
TIP41A
TIP41B*
TIP41C*
PNP
TIP42A
TIP42B*
TIP42C*

***Motorola Preferred Device**

6 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60 – 80 – 100 VOLTS
65 WATTS



CASE 221A–06
TO–220AB

***MAXIMUM RATINGS**

Rating	Symbol	TIP41A TIP42A	TIP41B TIP42B	TIP41C TIP42C	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	6 10			Adc
Base Current	I_B	2.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	65 0.52			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Unclamped Inductive Load Energy (1)	E	62.5			mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W

(1) I_C = 2.5 A, L = 20 mH, P.R.F. = 10 Hz, V_{CC} = 10 V, R_{BE} = 100 Ω.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	$V_{CEO(sus)}$	60 80 100	— — —	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 60 Vdc, I_B = 0)	TIP41A, TIP42A TIP41B, TIP41C TIP42B, TIP42C	I_{CEO}	— — —	0.7 0.7 0.7	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, V_{EB} = 0) (V_{CE} = 80 Vdc, V_{EB} = 0) (V_{CE} = 100 Vdc, V_{EB} = 0)	TIP41A, TIP42A TIP41B, TIP42B TIP41C, TIP42C	I_{CES}	— — —	400 400 400	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	1.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 0.3 Adc, V_{CE} = 4.0 Vdc) (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	30 15	— 75	—
Collector–Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 600 mAdc)		$V_{CE(sat)}$	—	1.5	Vdc
Base–Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	3.0	—	MHz
Small–Signal Current Gain (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	20	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

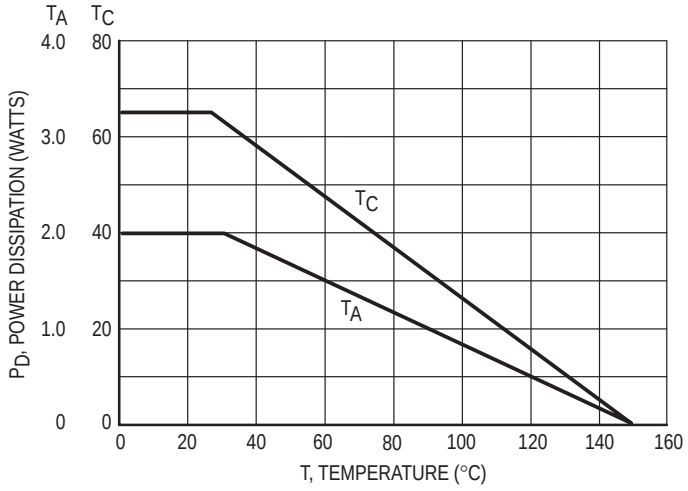
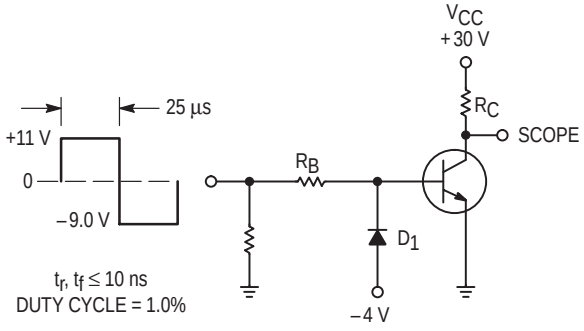


Figure 1. Power Derating



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS

D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx 100$ mA
MSD6100 USED BELOW $I_B \approx 100$ mA

Figure 2. Switching Time Test Circuit

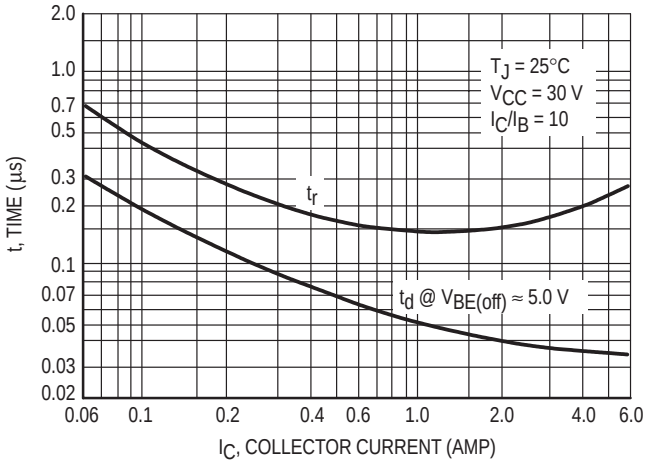


Figure 3. Turn–On Time

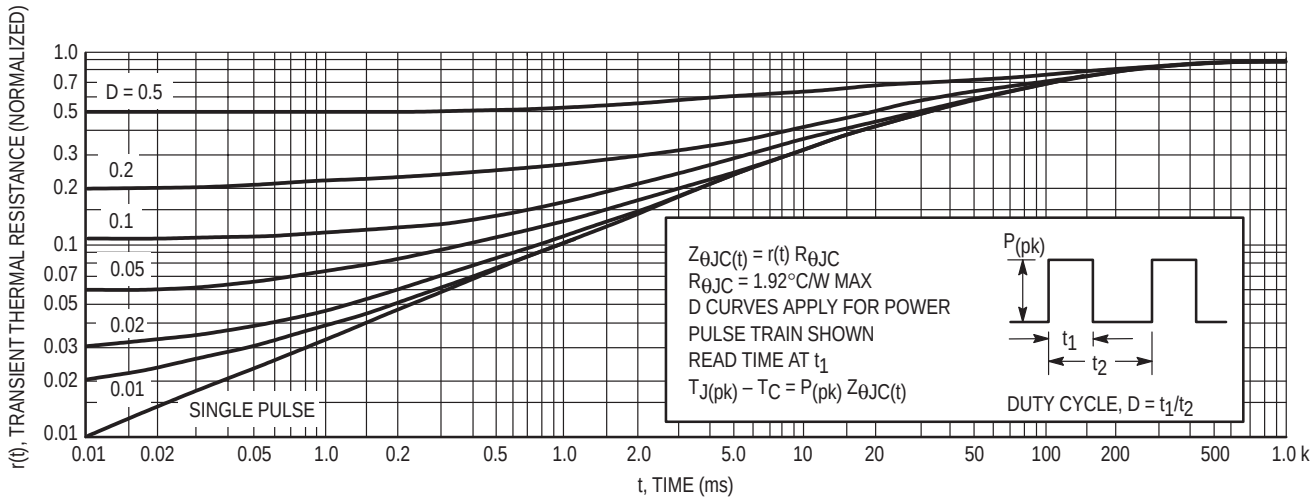


Figure 4. Thermal Response

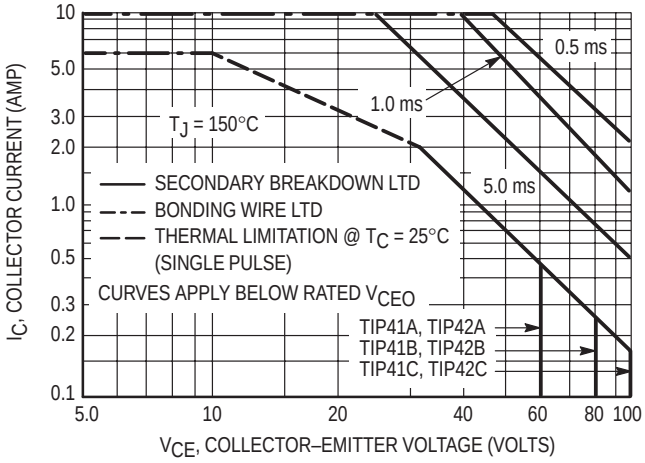


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

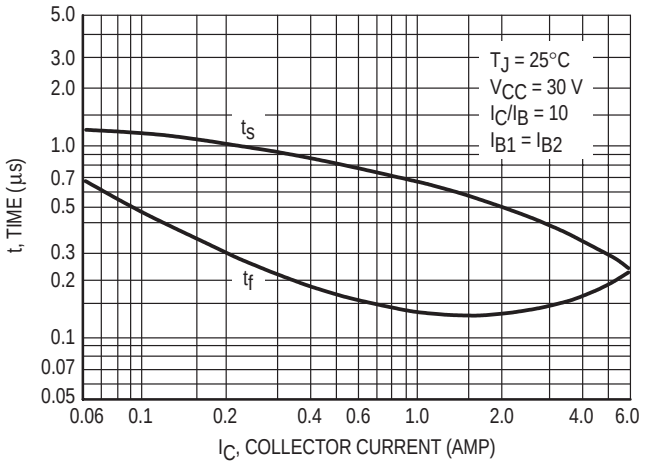


Figure 6. Turn–Off Time

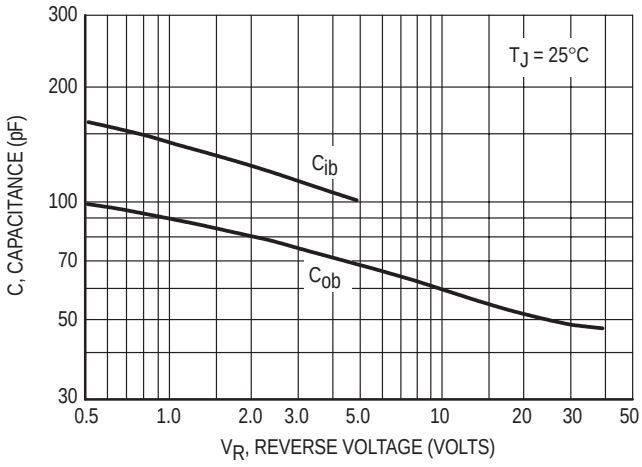


Figure 7. Capacitance

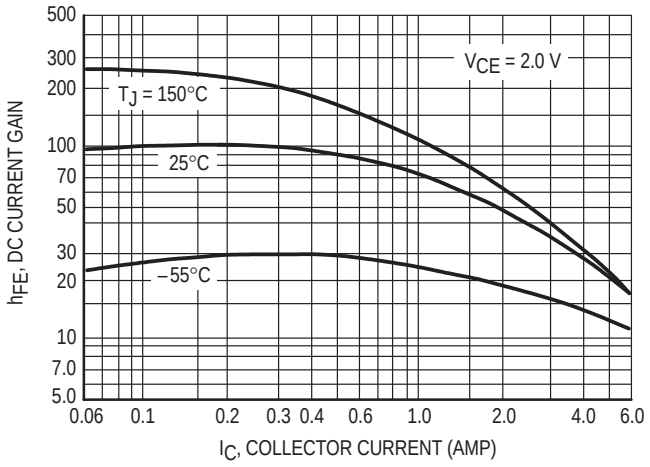


Figure 8. DC Current Gain

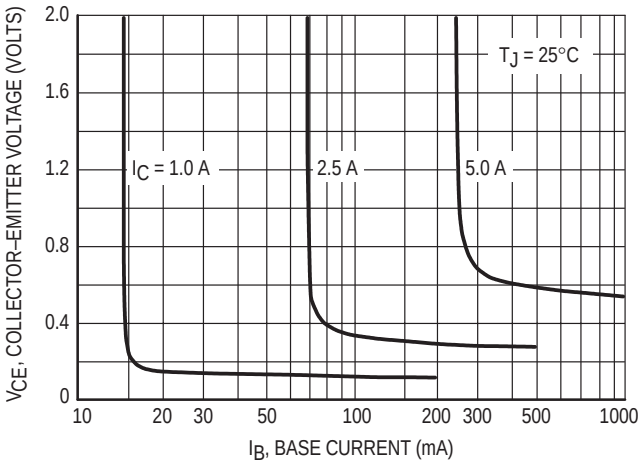


Figure 9. Collector Saturation Region

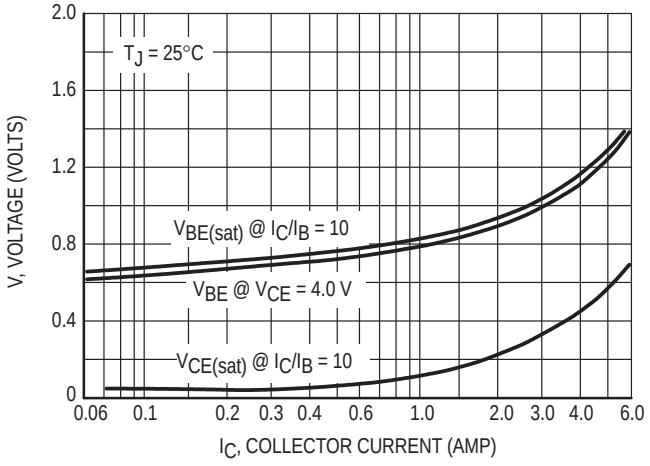


Figure 10. “On” Voltages

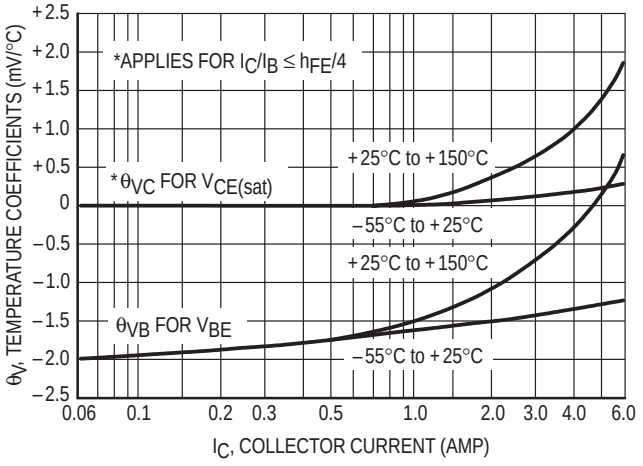


Figure 11. Temperature Coefficients

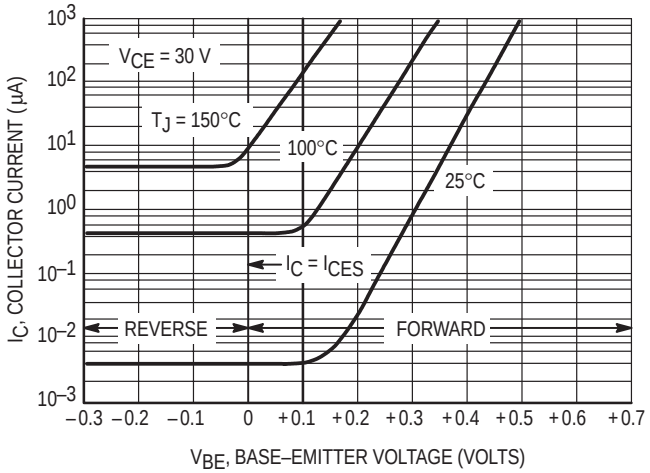


Figure 12. Collector Cut–Off Region

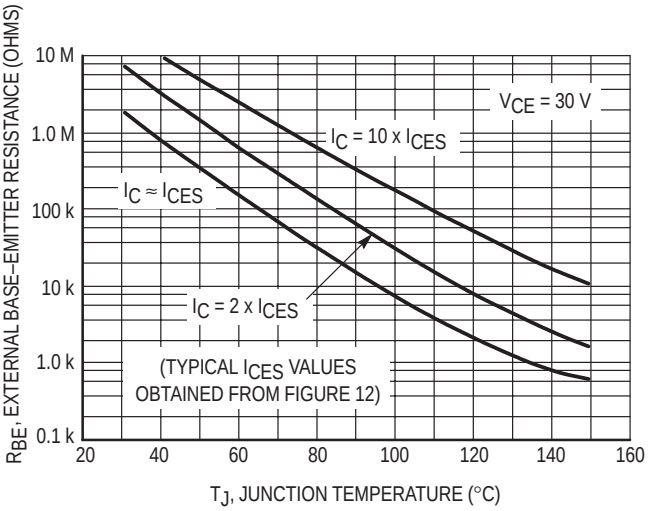


Figure 13. Effects of Base–Emitter Resistance

TIP47*
TIP49*
TIP48*
TIP50*

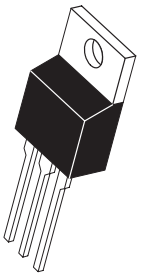
*Motorola Preferred Device

1.0 AMPERE
POWER TRANSISTORS
NPN SILICON
250 – 300 – 350 – 400 VOLTS
40 WATTS

High Voltage NPN Silicon Power Transistors

. . . designed for line operated audio output amplifier, Switchmode power supply drivers and other switching applications.

- 250 V to 400 V (Min) — $V_{CEO(sus)}$
- 1 A Rated Collector Current
- Popular TO–220 Plastic Package



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	TIP47	TIP48	TIP49	TIP50	Unit
Collector–Emitter Voltage	V_{CEO}	250	300	350	400	Vdc
Collector–Base Voltage	V_{CB}	350	400	450	500	Vdc
Emitter–Base Voltage	V_{EB}	5.0				Vdc
Collector Current — Continuous Peak	I_C	1.0 2.0				Adc
Base Current	I_B	0.6				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32				Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016				Watts W/°C
Unclamped Inducting Load Energy (See Figure 8)	E	20				mJ
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.125	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

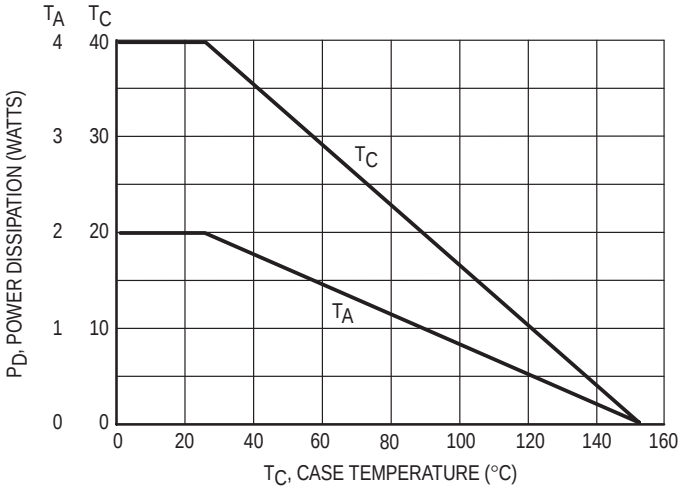


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)	TIP47	$V_{CEO(sus)}$	250	—	Vdc
(I_C = 30 mAdc, I_B = 0)	TIP48		300	—	
	TIP49		350	—	
	TIP50		400	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 150 Vdc, I_B = 0)	TIP47		—	1.0	
(V_{CE} = 200 Vdc, I_B = 0)	TIP48		—	1.0	
(V_{CE} = 250 Vdc, I_B = 0)	TIP49		—	1.0	
(V_{CE} = 300 Vdc, I_B = 0)	TIP50		—	1.0	
Collector Cutoff Current		I_{CES}			mAdc
(V_{CE} = 350 Vdc, V_{BE} = 0)	TIP47		—	1.0	
(V_{CE} = 400 Vdc, V_{BE} = 0)	TIP48		—	1.0	
(V_{CE} = 450 Vdc, V_{BE} = 0)	TIP49		—	1.0	
(V_{CE} = 500 Vdc, V_{BE} = 0)	TIP50		—	1.0	
Emitter Cutoff Current		I_{EBO}	—	1.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 0.3 Adc, V_{CE} = 10 Vdc)			30	150	
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)			10	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$	—	1.0	Vdc
(I_C = 1.0 Adc, I_B = 0.2 Adc)					
Base–Emitter On Voltage		$V_{BE(on)}$	—	1.5	Vdc
(I_C = 1.0 Adc, V_{CE} = 10 Vdc)					
DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product		f_T	10	—	MHz
(I_C = 0.1 Adc, V_{CE} = 10 Vdc, f = 2.0 MHz)					
Small–Signal Current Gain		h_{fe}	25	—	—
(I_C = 0.2 Adc, V_{CE} = 10 Vdc, f = 1.0 kHz)					

(1) Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2.0%.

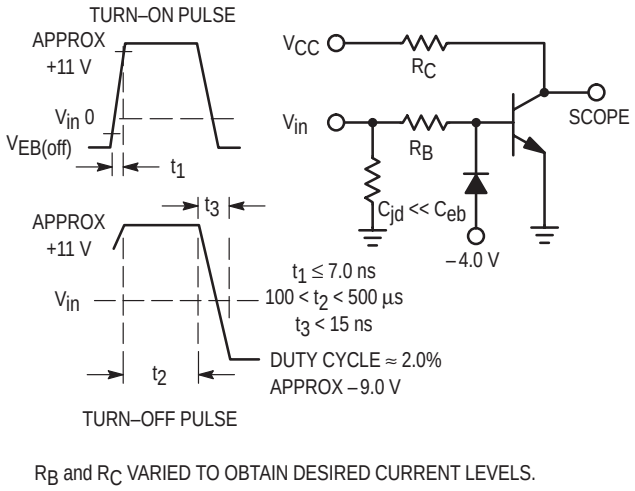


Figure 2. Switching Time Equivalent Circuit

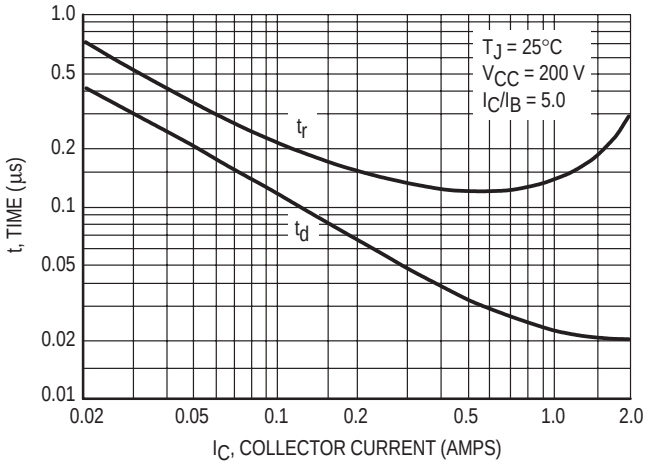


Figure 3. Turn–On Time

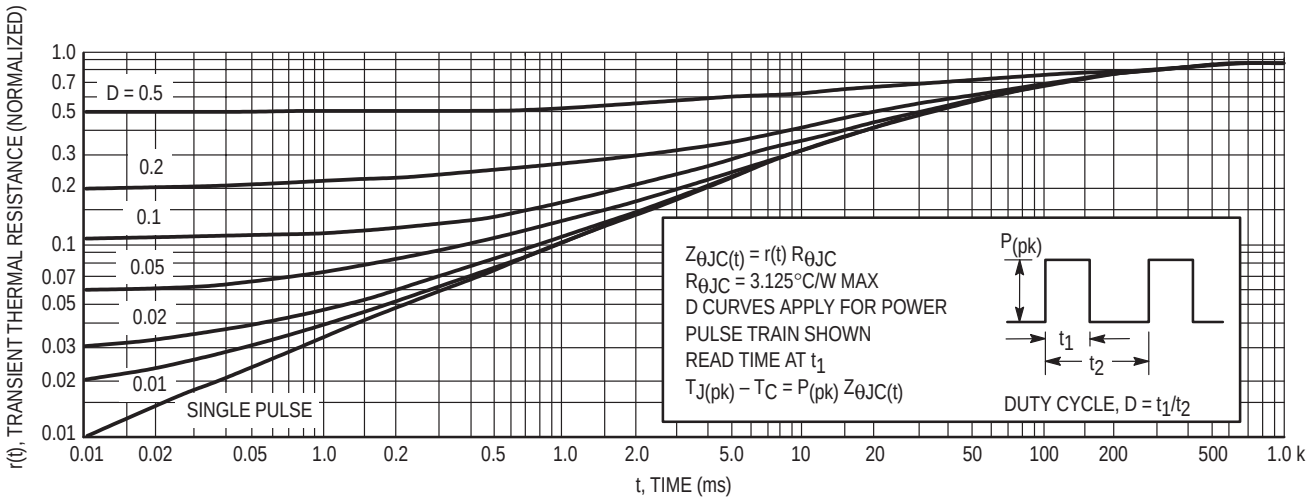


Figure 4. Thermal Response

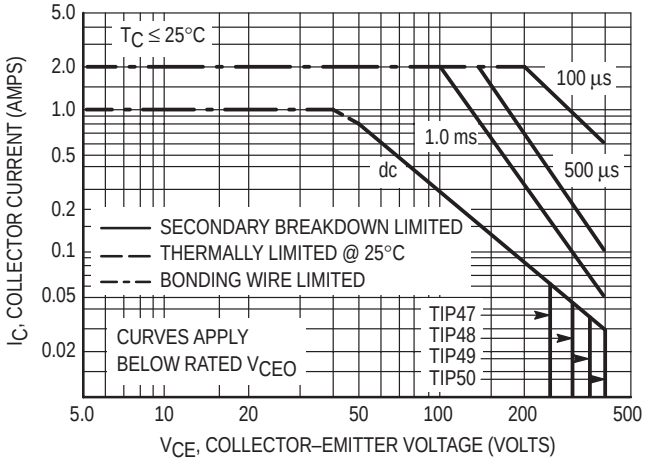


Figure 5. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

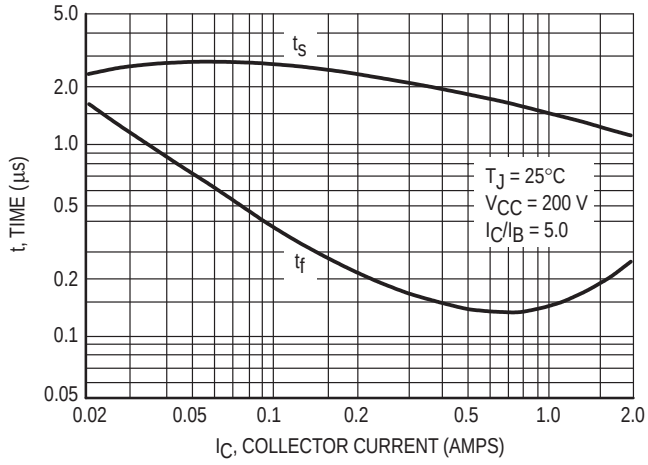


Figure 6. Turn–Off Time

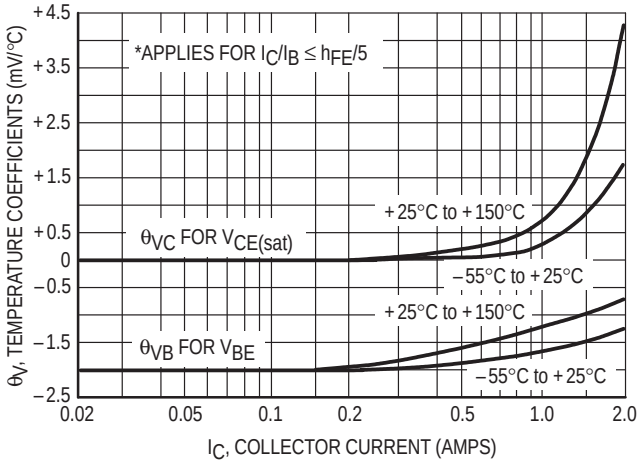
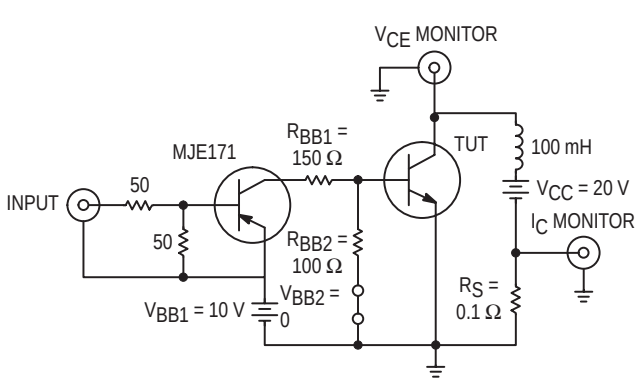
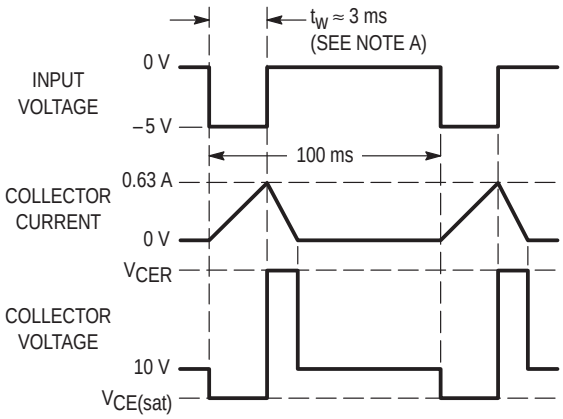


Figure 7. Temperature Coefficients





Note A: Input pulse width is increased until I_{CM} = 0.63 A.

Figure 8. Inductive Load Switching

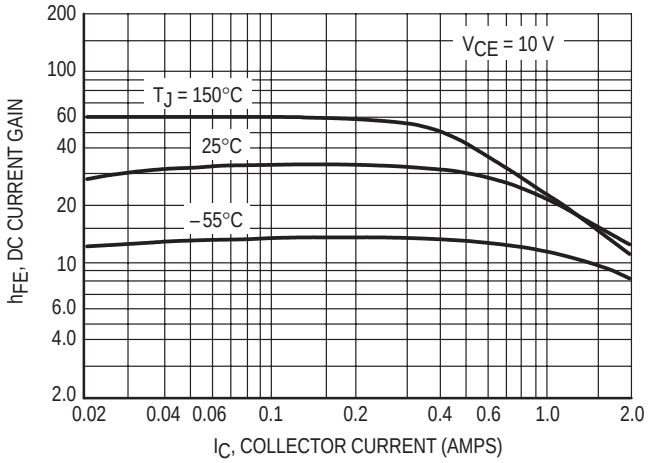


Figure 9. DC Current Gain

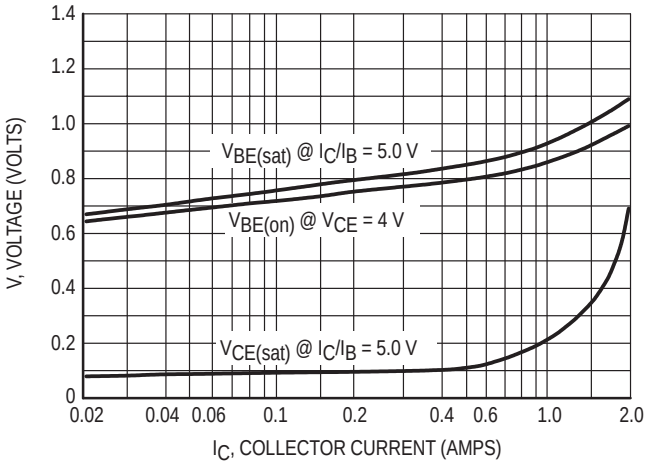


Figure 10. “On” Voltages

Plastic Medium-Power Complementary Silicon Transistors

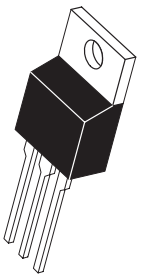
. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector–Emitter Sustaining Voltage — @ 30 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP100, TIP105
  = 80 Vdc (Min) — TIP101, TIP106
  = 100 Vdc (Min) — TIP102, TIP107
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 2.5 Vdc (Max) @ I_C = 8.0 Adc
- Monolithic Construction with Built–in Base–Emitter Shunt Resistors
- TO–220AB Compact Package

NPN
TIP100
TIP101*
TIP102*
PNP
TIP105
TIP106*
TIP107*

***Motorola Preferred Device**

DARLINGTON
8 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
60 – 80 – 100 VOLTS
80 WATTS



CASE 221A–06
TO–220AB

***MAXIMUM RATINGS**

Rating	Symbol	TIP100, TIP105	TIP101, TIP106	TIP102, TIP107	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	8.0 15			Adc
Base Current	I_B	1.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	80 0.64			Watts W/°C
Unclamped Inductive Load Energy (1)	E	30			mJ
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 1.1 A, L = 50 mH, P.R.F. = 10 Hz, V_{CC} = 20 V, R_{BE} = 100 Ω.

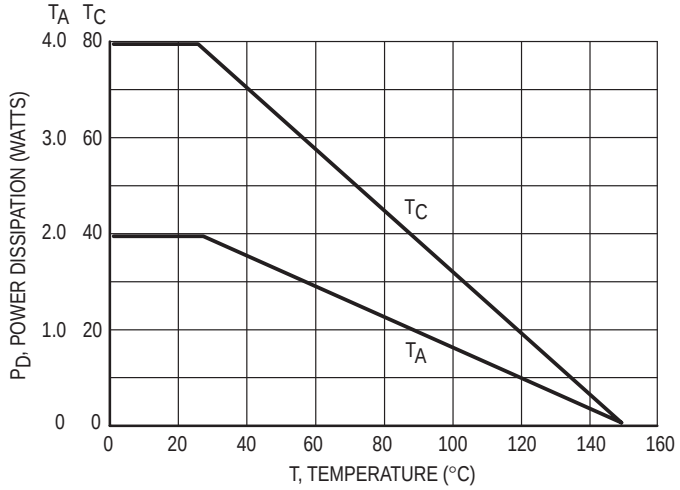


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	TIP100, TIP105		60	—	
	TIP101, TIP106		80	—	
	TIP102, TIP107		100	—	
Collector Cutoff Current		I_{CEO}			μAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP100, TIP105		—	50	
(V_{CE} = 40 Vdc, I_B = 0)	TIP101, TIP106		—	50	
(V_{CE} = 50 Vdc, I_B = 0)	TIP102, TIP107		—	50	
Collector Cuttoff Current		I_{CBO}			μAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP100, TIP105		—	50	
(V_{CB} = 80 Vdc, I_E = 0)	TIP101, TIP106		—	50	
(V_{CB} = 100 Vdc, I_E = 0)	TIP102, TIP107		—	50	
Emitter Cutoff Current		I_{EBO}	—	8.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc)			1000	20,000	
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)			200	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 6.0 mAdc)			—	2.0	
(I_C = 8.0 Adc, I_B = 80 mAdc)			—	2.5	
Base–Emitter On Voltage		$V_{BE(on)}$	—	2.8	Vdc
(I_C = 8.0 Adc, V_{CE} = 4.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain		h_{fe}	4.0	—	
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)					—
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP105, TIP106, TIP107		—	300	
	TIP100, TIP101, TIP102		—	200	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

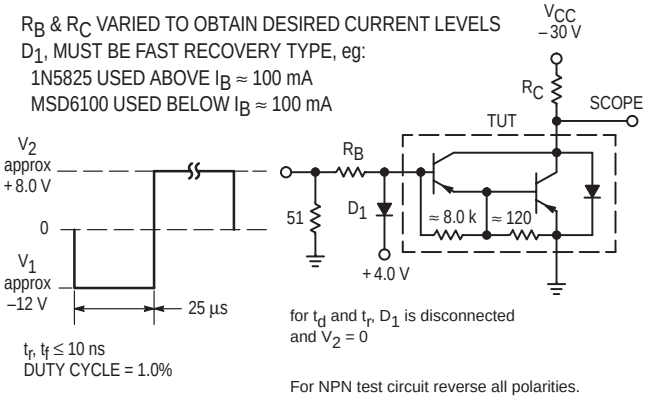


Figure 2. Switching Times Test Circuit

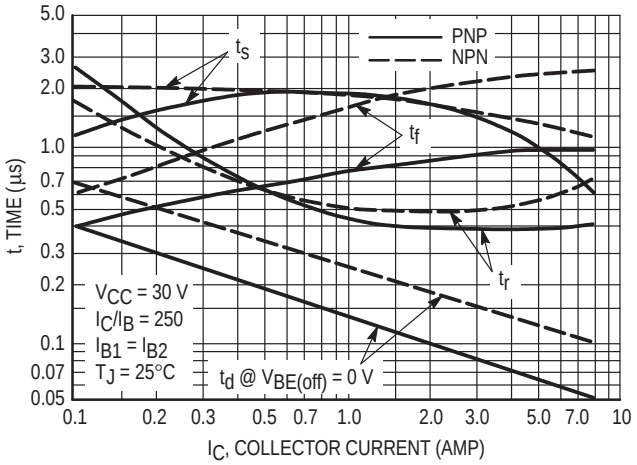


Figure 3. Switching Times

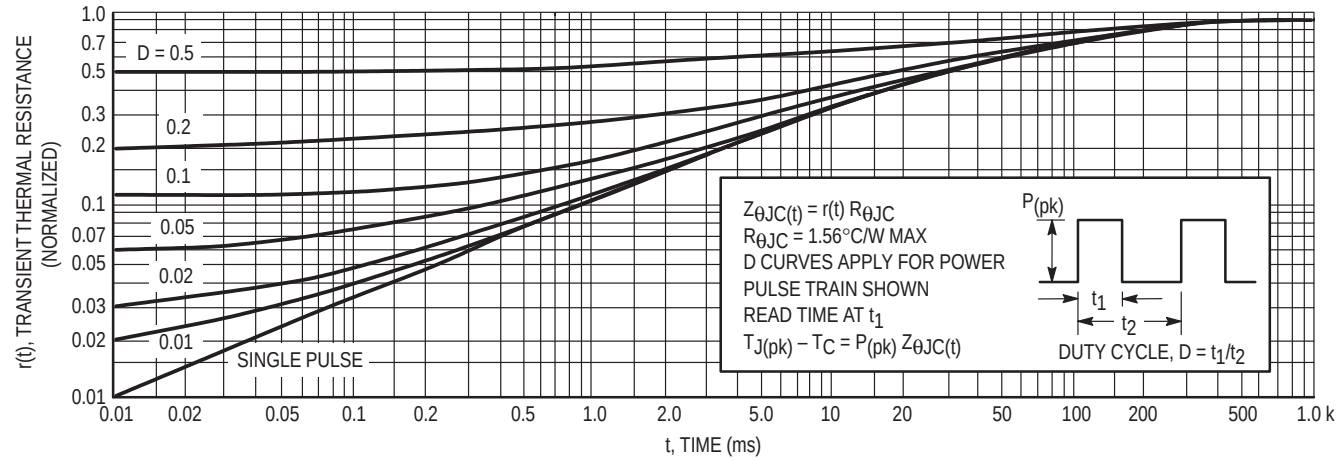


Figure 4. Thermal Response

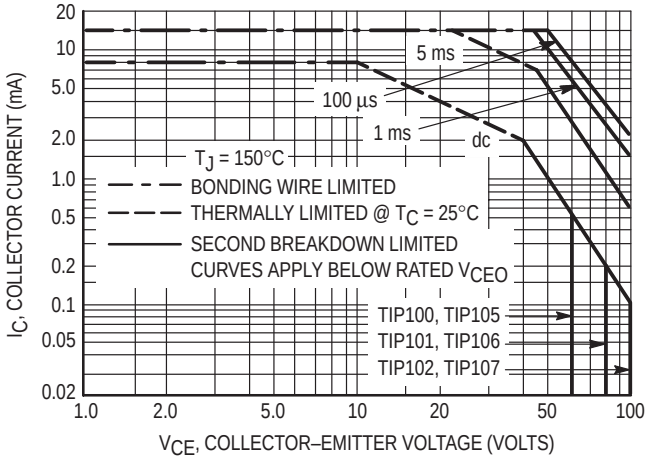


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

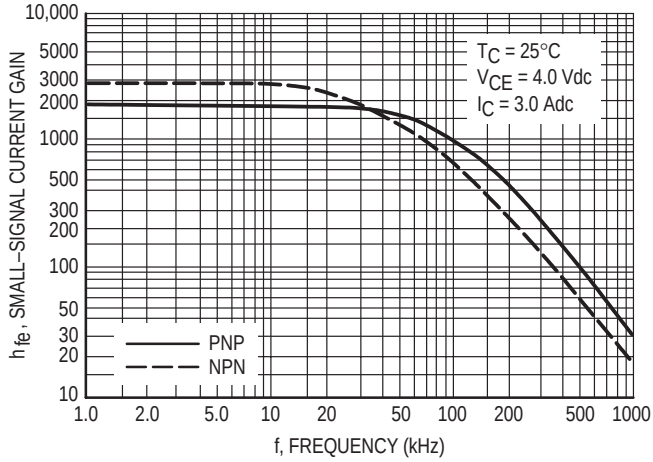


Figure 6. Small–Signal Current Gain

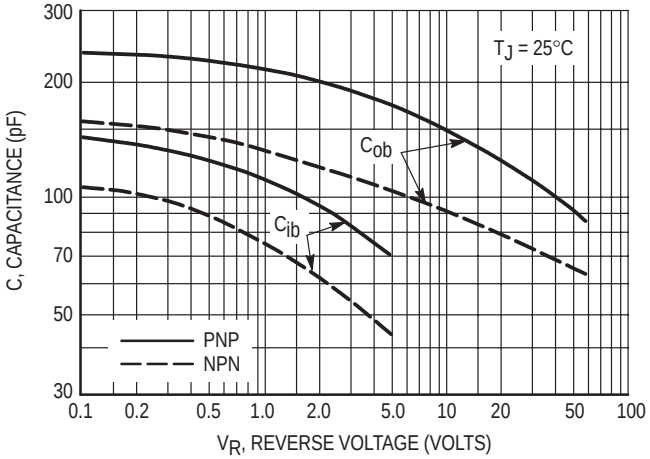
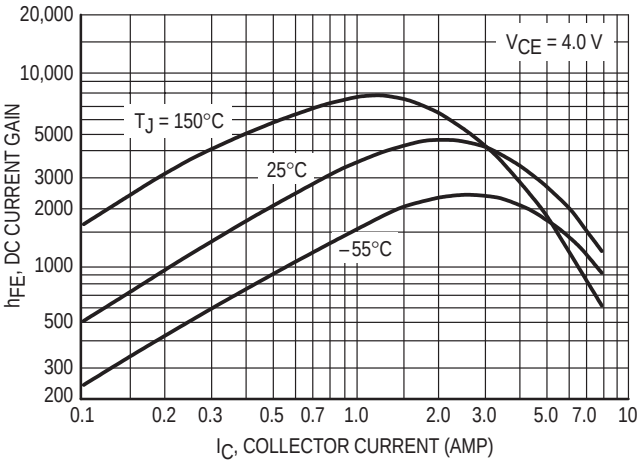


Figure 7. Capacitance

NPN
TIP100, TIP101, TIP102



PNP
TIP105, TIP106, TIP107

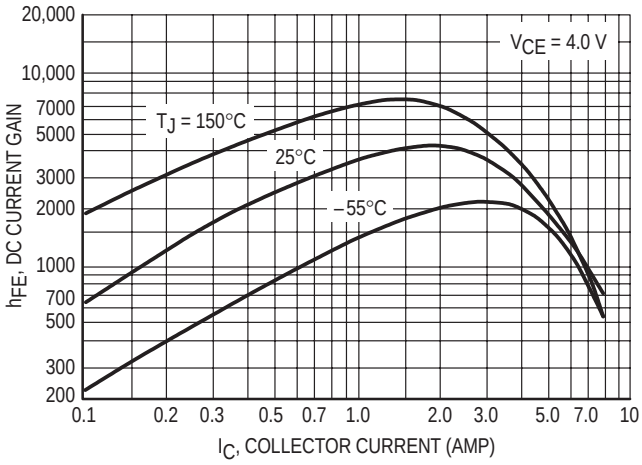
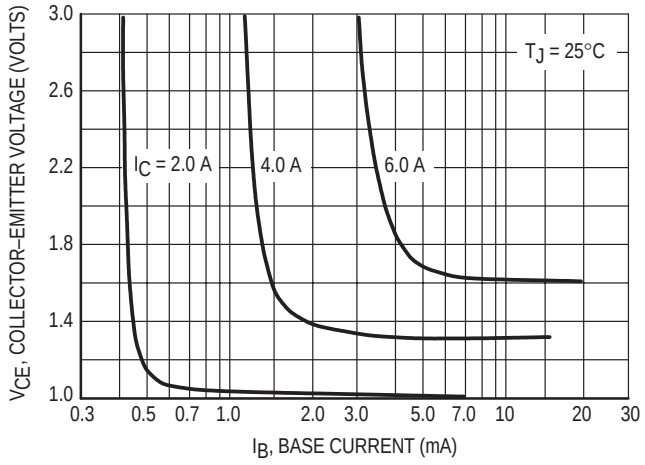


Figure 8. DC Current Gain



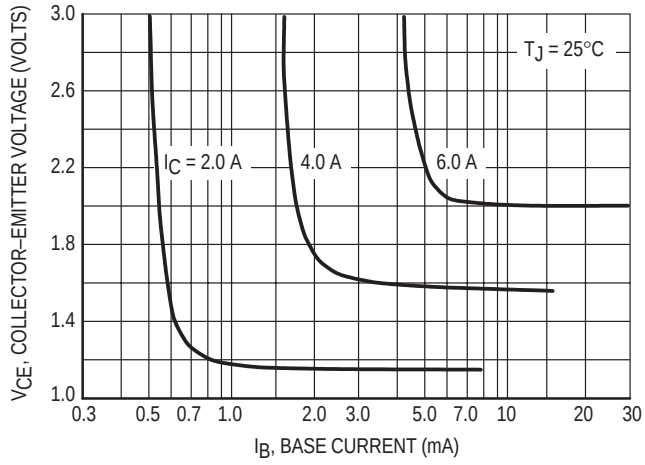
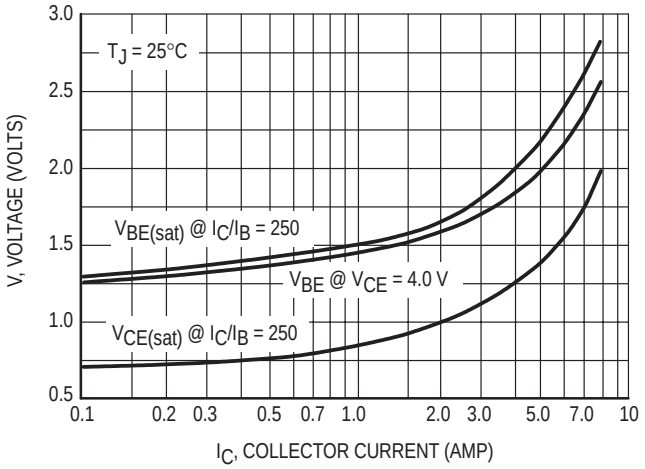


Figure 9. Collector Saturation Region



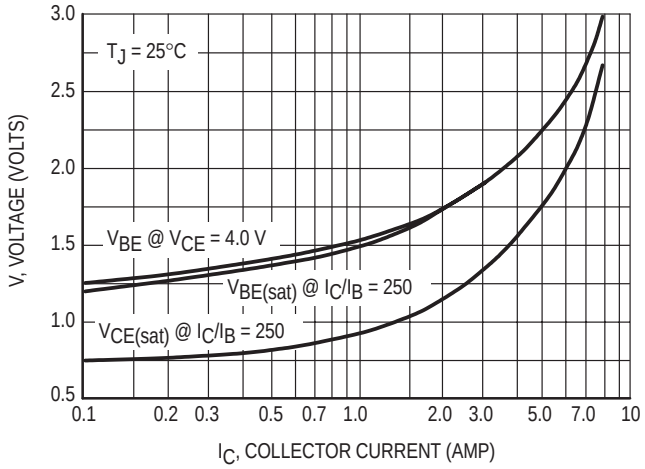


Figure 10. “On” Voltages

Plastic Medium-Power Complementary Silicon Transistors

. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 1.0 Adc
- Collector–Emitter Sustaining Voltage — @ 30 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP110, TIP115
  = 80 Vdc (Min) — TIP111, TIP116
  = 100 Vdc (Min) — TIP112, TIP117
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.5 Vdc (Max) @ I_C = 2.0 Adc
- Monolithic Construction with Built–in Base–Emitter Shunt Resistors
- TO–220AB Compact Package

NPN
TIP110
TIP111*
TIP112*
PNP
TIP115
TIP116*
TIP117*

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DARLINGTON
2 AMPERE
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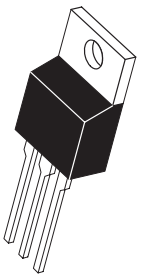


CASE 221A–06
TO–220AB

***MAXIMUM RATINGS**

Rating	Symbol	TIP110, TIP115	TIP111, TIP116	TIP112, TIP117	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	2.0 4.0			Adc
Base Current	I_B	50			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Unclamped Inductive Load Energy — Figure 13	E	25			mJ
Operating and Storage Junction	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

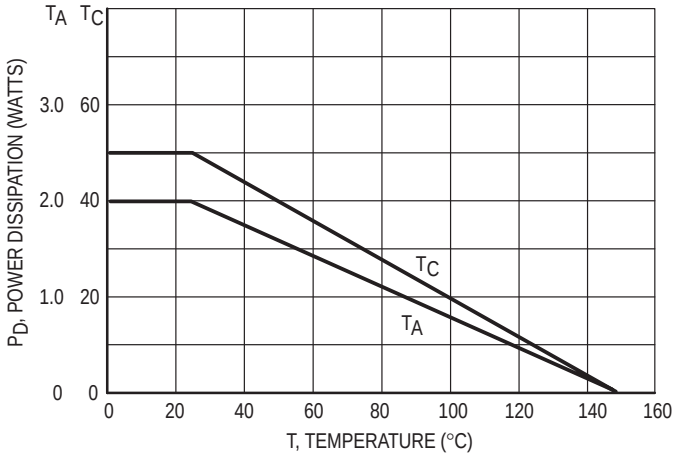


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mAdc, I_B = 0)	TIP110, TIP115		60	—	
	TIP111, TIP116		80	—	
	TIP112, TIP117		100	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP110, TIP115		—	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	TIP111, TIP116		—	2.0	
(V_{CE} = 50 Vdc, I_B = 0)	TIP112 ,TIP117		—	2.0	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP110, TIP115		—	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	TIP111, TIP116		—	1.0	
(V_{CB} = 100 Vdc, I_E = 0)	TIP112, TIP117		—	1.0	
Emitter Cutoff Current		I_{EBO}	—	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 1.0 Adc, V_{CE} = 4.0 Vdc)			1000	—	
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)			500	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$	—	2.5	Vdc
(I_C = 2.0 Adc, I_B = 8.0 mAdc)					
Base–Emitter On Voltage		$V_{BE(on)}$	—	2.8	Vdc
(I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain		h_{fe}	25	—	—
(I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)					
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	TIP115, TIP116, TIP117		—	200	
	TIP110, TIP111, TIP112		—	100	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

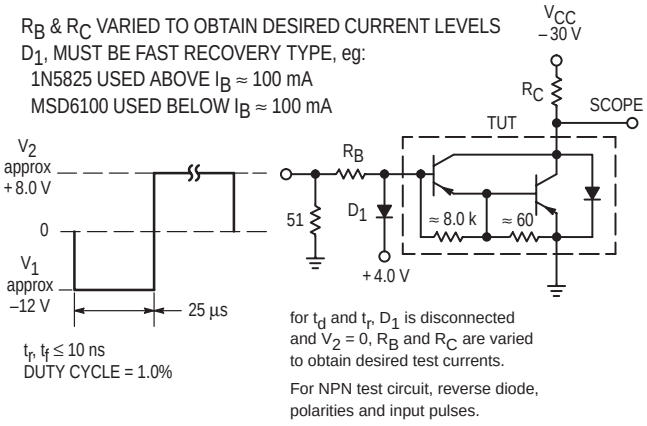


Figure 2. Switching Times Test Circuit

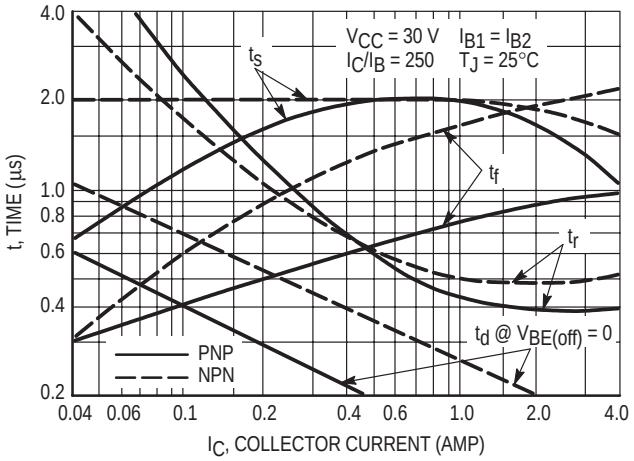


Figure 3. Switching Times

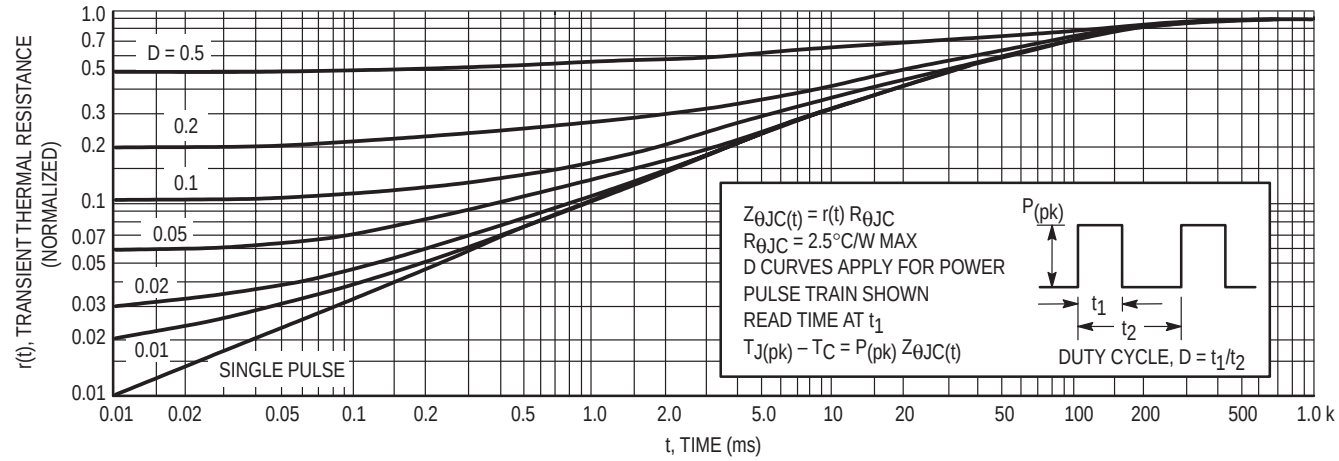


Figure 4. Thermal Response

ACTIVE–REGION SAFE–OPERATING AREA

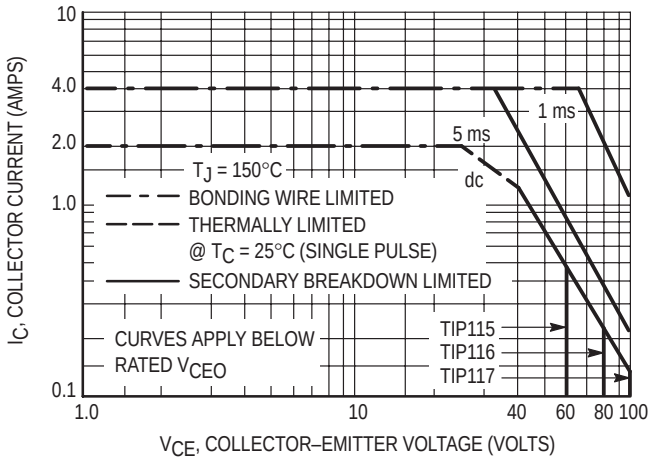


Figure 5. TIP115, 116, 117

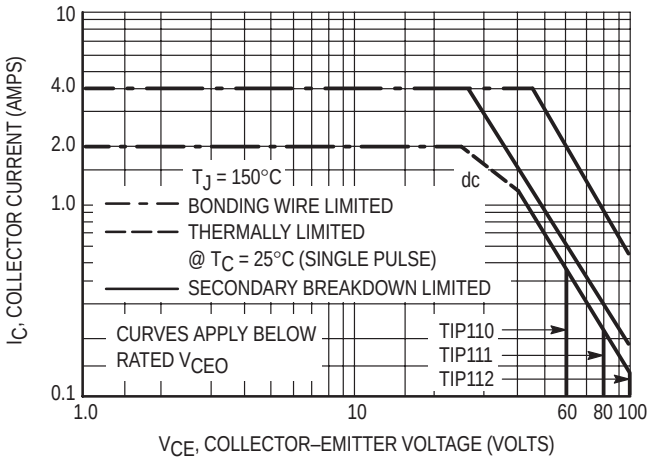


Figure 6. TIP110, 111, 112

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

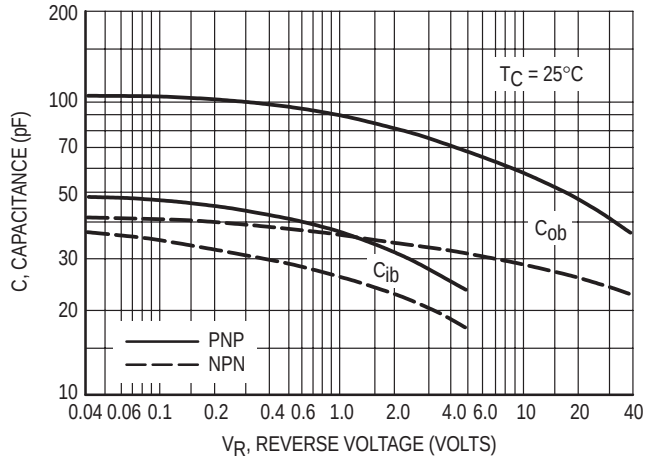
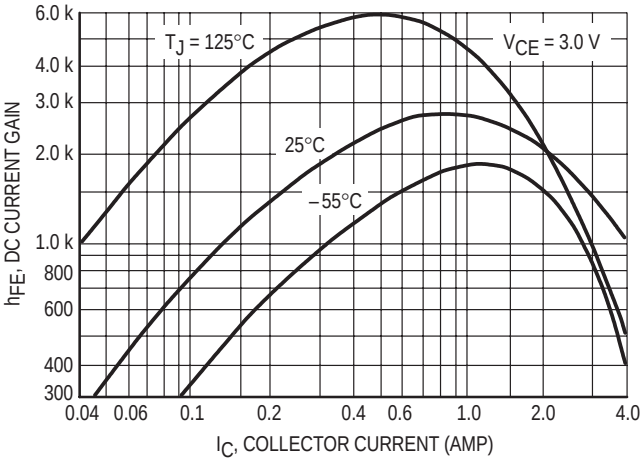


Figure 7. Capacitance

NPN
TIP110, 111, 112



PNP
TIP115, 116, 117

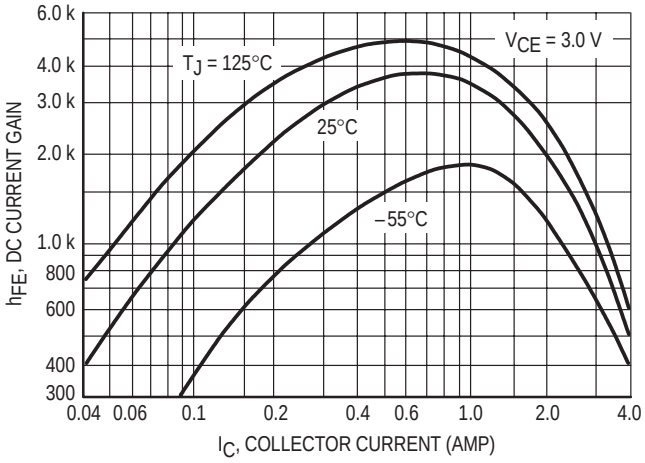
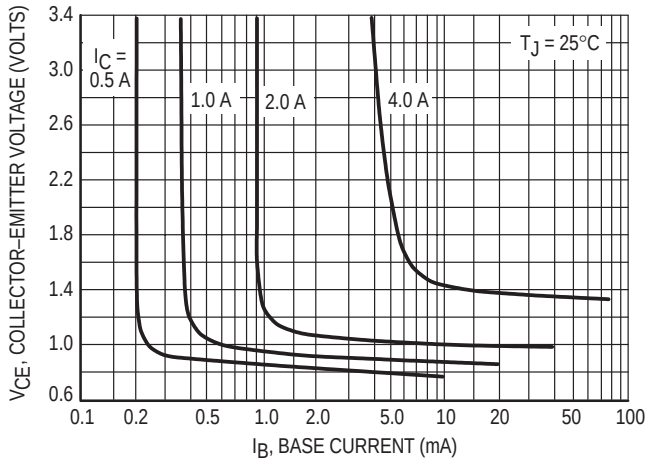


Figure 8. DC Current Gain



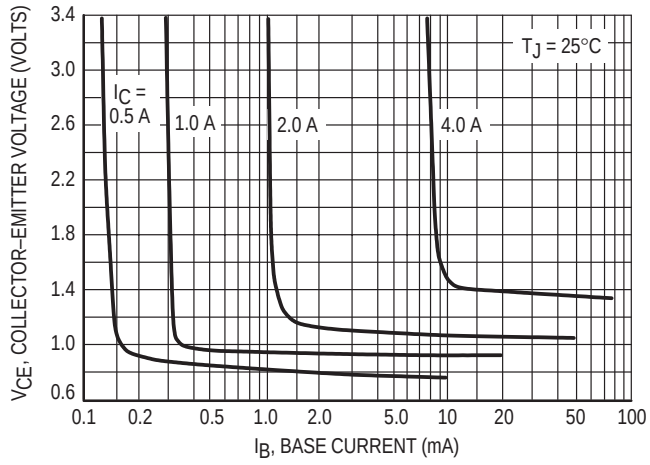
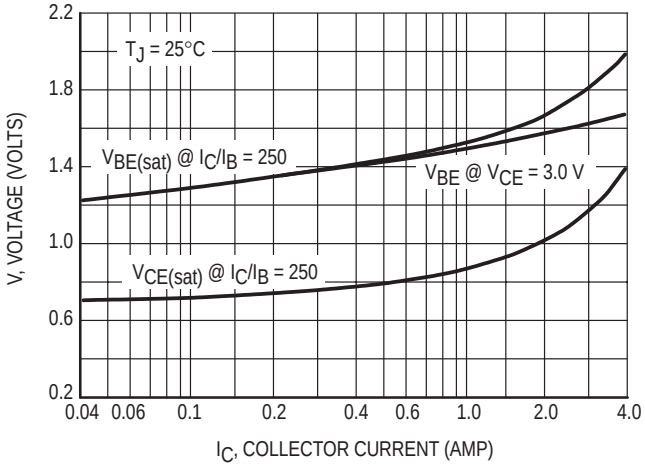


Figure 9. Collector Saturation Region



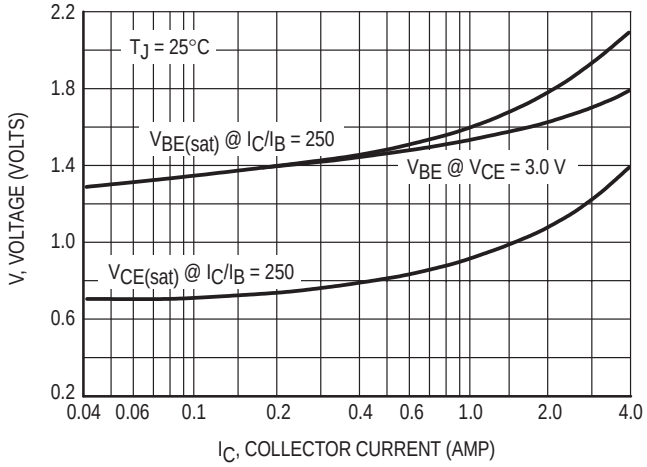
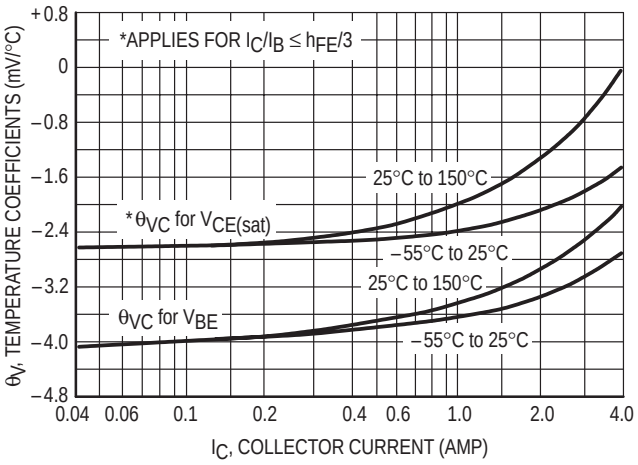


Figure 10. “On” Voltages

NPN
TIP110, 111, 112



PNP
TIP115, 116, 117

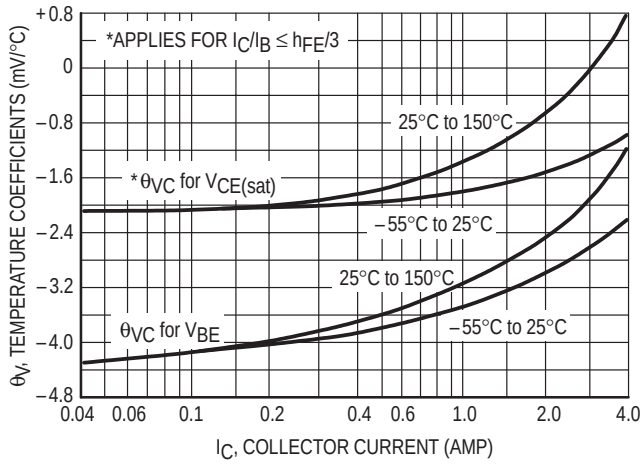
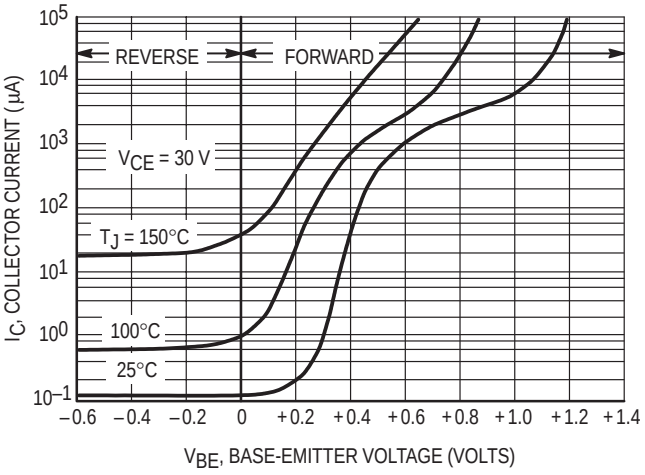


Figure 11. Temperature Coefficients



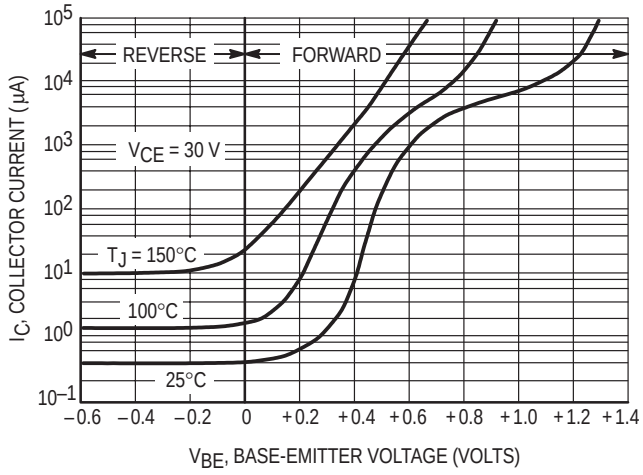
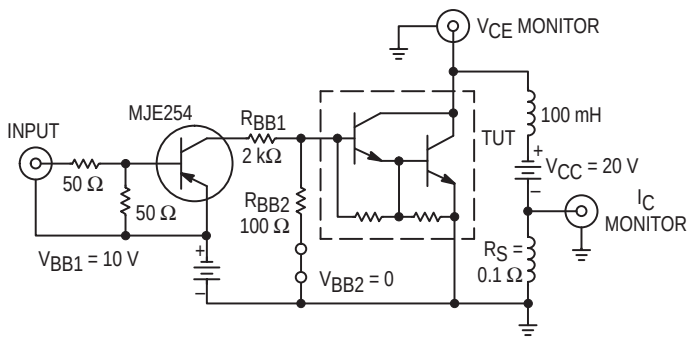


Figure 12. Collector Cut-Off Region

TEST CIRCUIT



Note A: Input pulse width is increased until I_{CM} = 0.71 A,
NPN test shown; for PNP test
reverse all polarity and use MJE224 driver.

VOLTAGE AND CURRENT WAVEFORMS

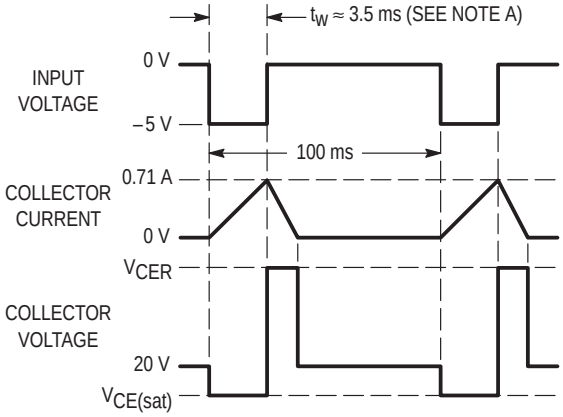


Figure 13. Inductive Load Switching

Plastic Medium-Power Complementary Silicon Transistors

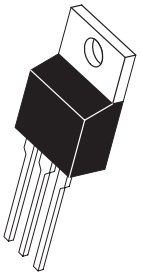
. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector–Emitter Sustaining Voltage — @ 100 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP120, TIP125
  = 80 Vdc (Min) — TIP121, TIP126
  = 100 Vdc (Min) — TIP122, TIP127
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors
- TO–220AB Compact Package

NPN
TIP120*
TIP121*
TIP122*
PNP
TIP125*
TIP126*
TIP127*

***Motorola Preferred Device**

DARLINGTON
5 AMPERE
COMPLEMENTARY SILICON
POWER TRANSISTORS
60 – 80 – 100 VOLTS
65 WATTS



CASE 221A–06
TO–220AB

***MAXIMUM RATINGS**

Rating	Symbol	TIP120, TIP125	TIP121, TIP126	TIP122, TIP127	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak	I_C	5.0 8.0			Adc
Base Current	I_B	120			mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	65 0.52			Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016			Watts W/°C
Unclamped Inductive Load Energy (1)	E	50			mJ
Operating and Storage Junction, Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

(1) I_C = 1 A, L = 100 mH, P.R.F. = 10 Hz, V_{CC} = 20 V, R_{BE} = 100 Ω.

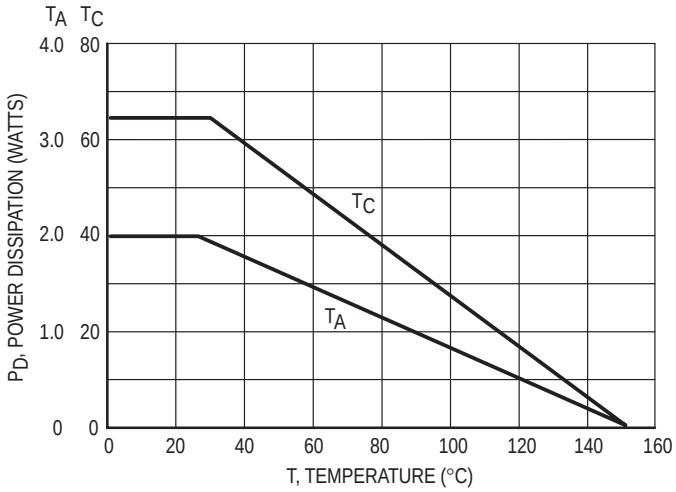


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	TIP120, TIP125		60	—	
	TIP121, TIP126		80	—	
	TIP122, TIP127		100	—	
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, I_B = 0)	TIP120, TIP125		—	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	TIP121, TIP126		—	0.5	
(V_{CE} = 50 Vdc, I_B = 0)	TIP122, TIP127		—	0.5	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	TIP120, TIP125		—	0.2	
(V_{CB} = 80 Vdc, I_E = 0)	TIP121, TIP126		—	0.2	
(V_{CB} = 100 Vdc, I_E = 0)	TIP122, TIP127		—	0.2	
Emitter Cutoff Current		I_{EBO}	—	2.0	mAdc
(V_{BE} = 5.0 Vdc, I_C = 0)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			—
(I_C = 0.5 Adc, V_{CE} = 3.0 Vdc)			1000	—	
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)			1000	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 12 mAdc)			—	2.0	
(I_C = 5.0 Adc, I_B = 20 mAdc)			—	4.0	
Base–Emitter On Voltage		$V_{BE(on)}$	—	2.5	Vdc
(I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)					
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain		h_{fe}	4.0	—	—
(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)					
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz	TIP125, TIP126, TIP127		—	300	
	TIP120, TIP121, TIP122		—	200	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

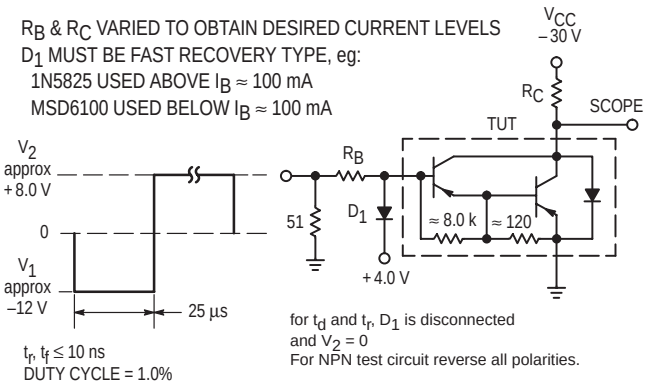


Figure 2. Switching Times Test Circuit

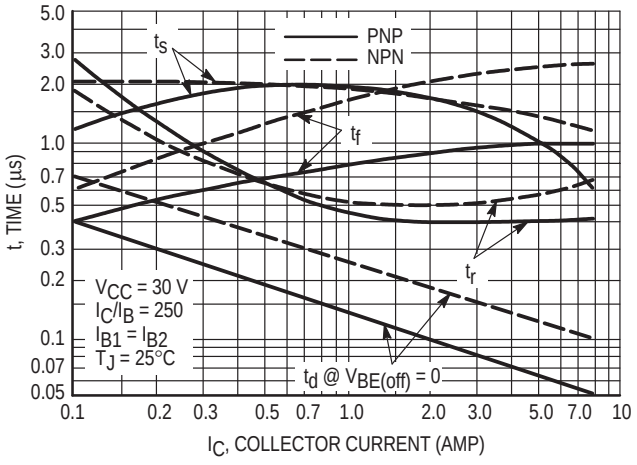


Figure 3. Switching Times

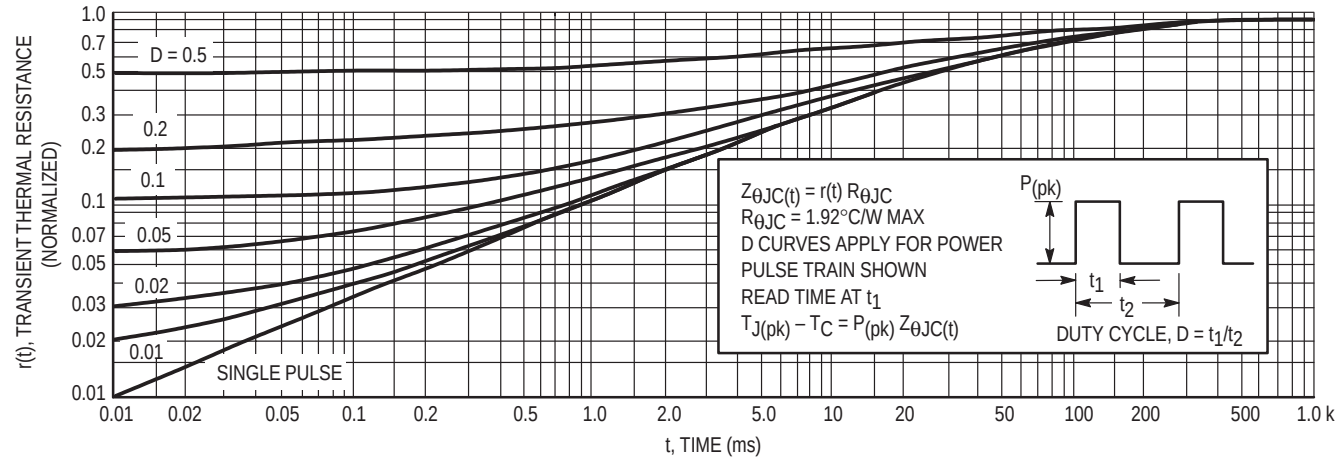


Figure 4. Thermal Response

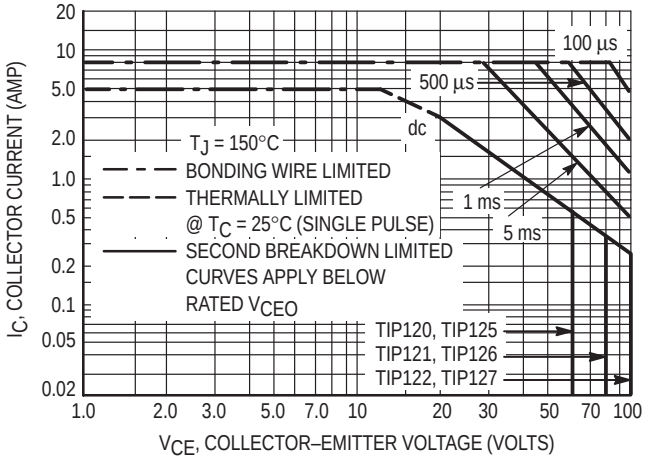


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

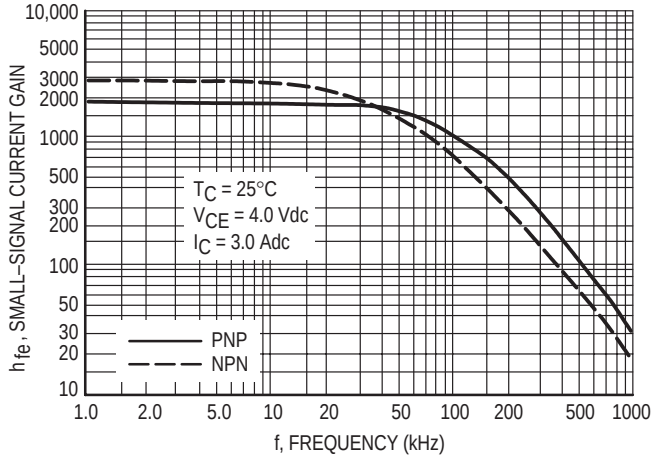


Figure 6. Small–Signal Current Gain

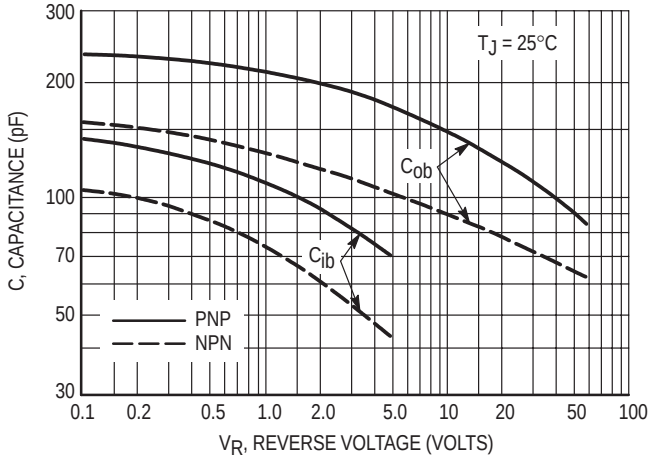
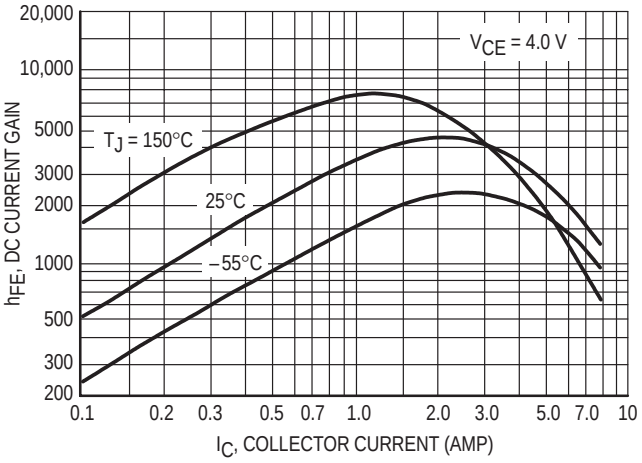


Figure 7. Capacitance

NPN
TIP120, TIP121, TIP122



PNP
TIP125, TIP126, TIP127

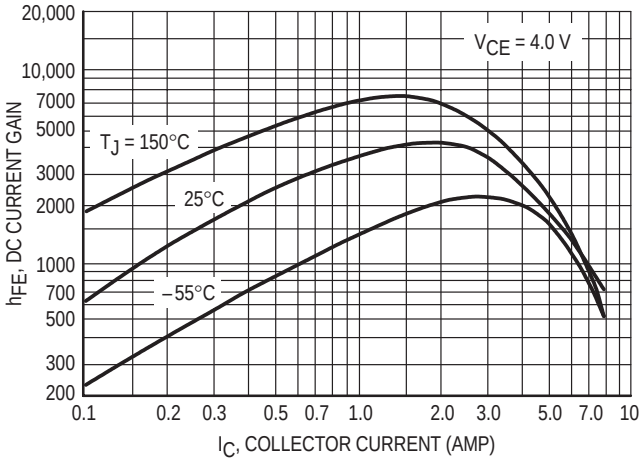
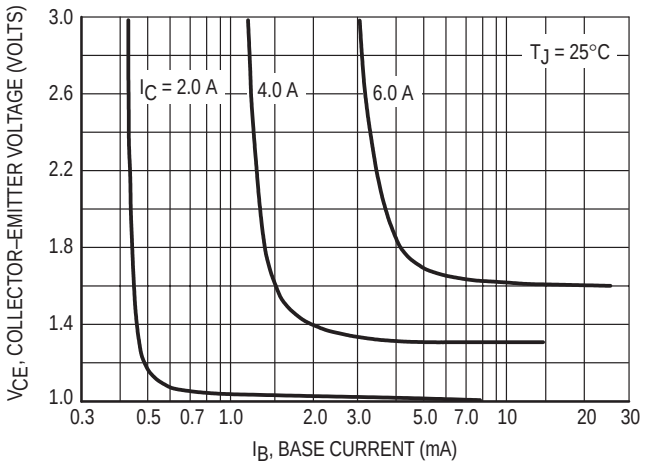


Figure 8. DC Current Gain



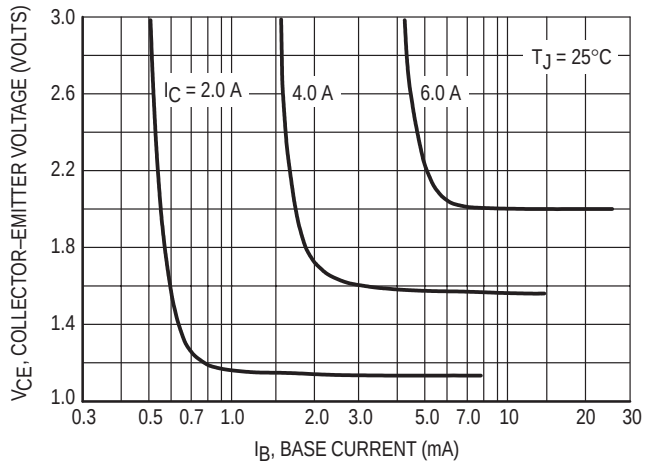
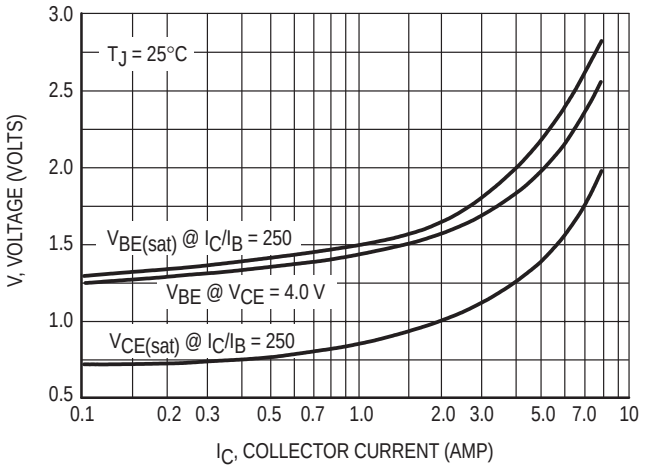


Figure 9. Collector Saturation Region



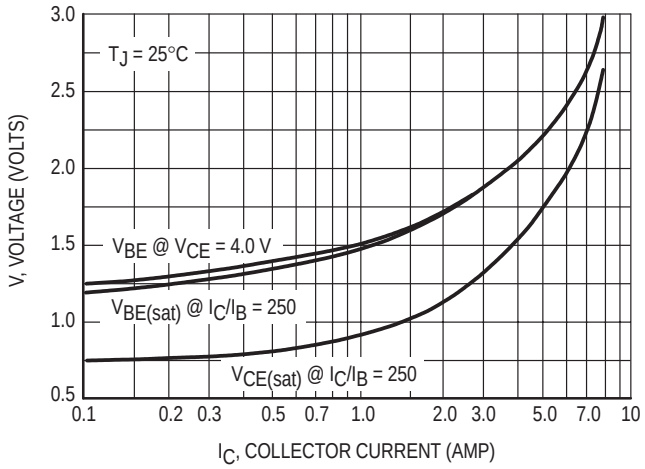


Figure 10. “On” Voltages

Darlington Complementary Silicon Power Transistors

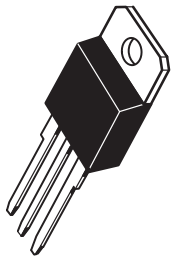
. . . designed for general–purpose amplifier and low frequency switching applications.

- High DC Current Gain — Min h_{FE} = 1000 @ I_C = 5 A, V_{CE} = 4 V
- Collector–Emitter Sustaining Voltage — @ 30 mA
  $V_{CEO(sus)}$ = 60 Vdc (Min) — TIP140, TIP145
  80 Vdc (Min) — TIP141, TIP146
  100 Vdc (Min) — TIP142, TIP147
- Monolithic Construction with Built–In Base–Emitter Shunt Resistor

NPN
TIP140
TIP141*
TIP142*
PNP
TIP145
TIP146*
TIP147*

***Motorola Preferred Device**

10 AMPERE
DARLINGTON
COMPLEMENTARY SILICON
POWER TRANSISTORS
60 – 100 VOLTS
125 WATTS



CASE 340D–01

MAXIMUM RATINGS

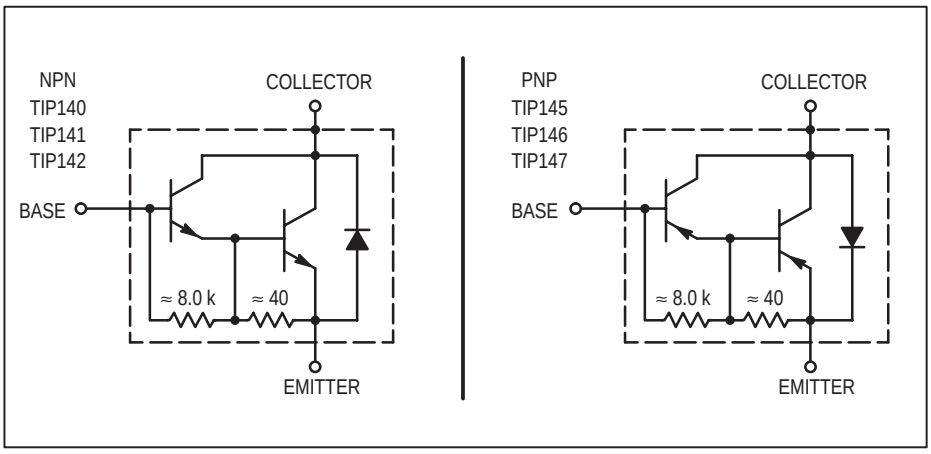
Rating	Symbol	TIP140 TIP145	TIP141 TIP146	TIP142 TIP147	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector–Base Voltage	V_{CB}	60	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0			Vdc
Collector Current — Continuous Peak (1)	I_C	10 15			Adc
Base Current — Continuous	I_B	0.5			Adc
Total Device Dissipation @ T_C = 25°C	P_D	125			Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Thermal Resistance, Case to Ambient	$R_{\theta JA}$	35.7	°C/W

(1) 5 ms, ≤ 10% Duty Cycle.

DARLINGTON SCHEMATICS

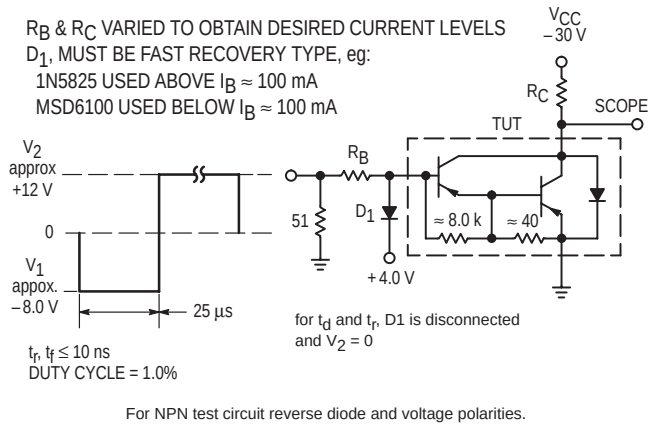


Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Sustaining Voltage (1)		$V_{CEO(sus)}$				Vdc
(I_C = 30 mA, I_B = 0)	TIP140, TIP145		60	—	—	
	TIP141, TIP146		80	—	—	
	TIP142, TIP147		100	—	—	
Collector Cutoff Current		I_{CEO}				mA
(V_{CE} = 30 Vdc, I_B = 0)	TIP140, TIP145		—	—	2.0	
(V_{CE} = 40 Vdc, I_B = 0)	TIP141, TIP146		—	—	2.0	
(V_{CE} = 50 Vdc, I_B = 0)	TIP142, TIP147		—	—	2.0	
Collector Cutoff Current		I_{CBO}				mA
(V_{CB} = 60 V, I_E = 0)	TIP140, TIP145		—	—	1.0	
(V_{CB} = 80 V, I_E = 0)	TIP141, TIP146		—	—	1.0	
(V_{CB} = 100 V, I_E = 0)	TIP142, TIP147		—	—	1.0	
Emitter Cutoff Current (V_{BE} = 5.0 V)		I_{EBO}	—	—	2 0	mA
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				—
(I_C = 5.0 A, V_{CE} = 4.0 V)			1000	—	—	
(I_C = 10 A, V_{CE} = 4.0 V)			500	—	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 5.0 A, I_B = 10 mA)			—	—	2.0	
(I_C = 10 A, I_B = 40 mA)			—	—	3.0	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$	—	—	3.5	Vdc
(I_C = 10 A, I_B = 40 mA)						
Base–Emitter On Voltage		$V_{BE(on)}$	—	—	3.0	Vdc
(I_C = 10 A, V_{CE} = 4.0 Vdc)						
SWITCHING CHARACTERISTICS						
Resistive Load (See Figure 1)						
Delay Time	(V_{CC} = 30 V, I_C = 5.0 A, I_B = 20 mA, Duty Cycle ≤ 2.0%, I_{B1} = I_{B2}, R_C & R_B Varied, T_J = 25°C)	t_d	—	0.15	—	µs
Rise Time		t_r	—	0.55	—	µs
Storage Time		t_s	—	2.5	—	µs
Fall Time		t_f	—	2.5	—	µs

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤ 2.0%.



For NPN test circuit reverse diode and voltage polarities.

Figure 1. Switching Times Test Circuit

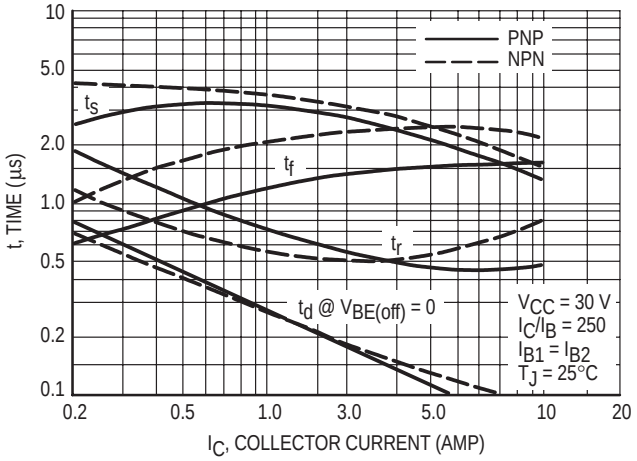
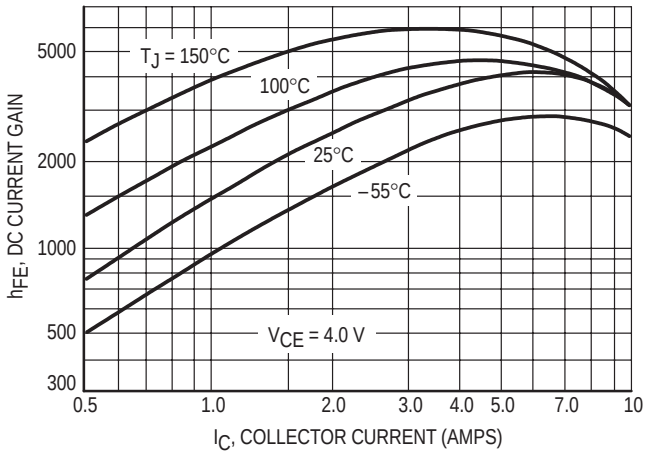


Figure 2. Switching Times

TYPICAL CHARACTERISTICS

NPN
TIP140, TIP141, TIP142



PNP
TIP145, TIP146, TIP147

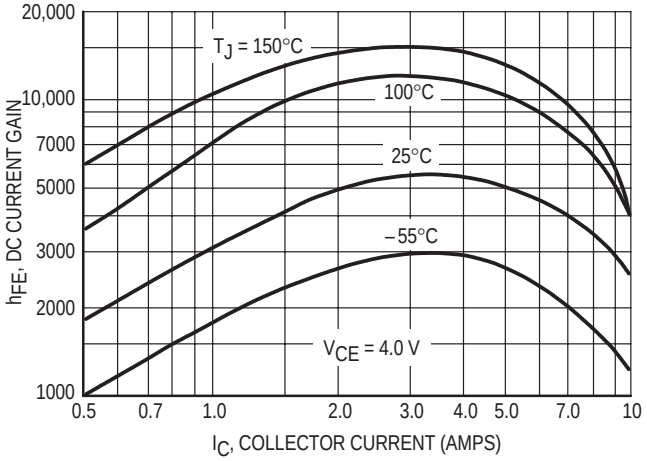
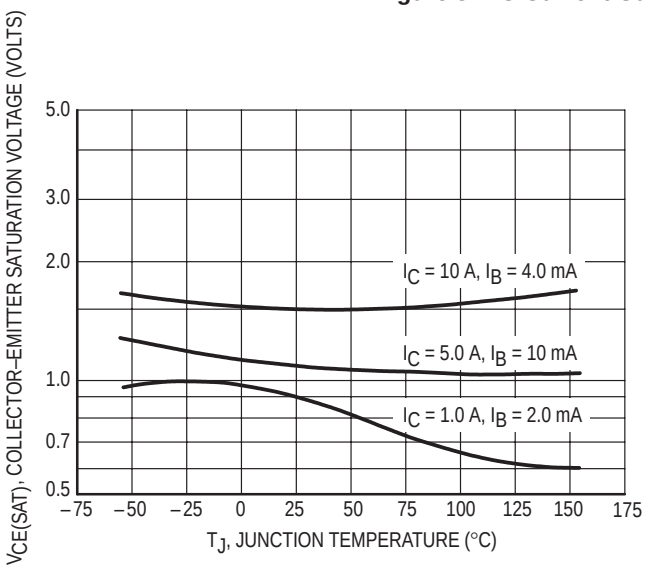


Figure 3. DC Current Gain versus Collector Current



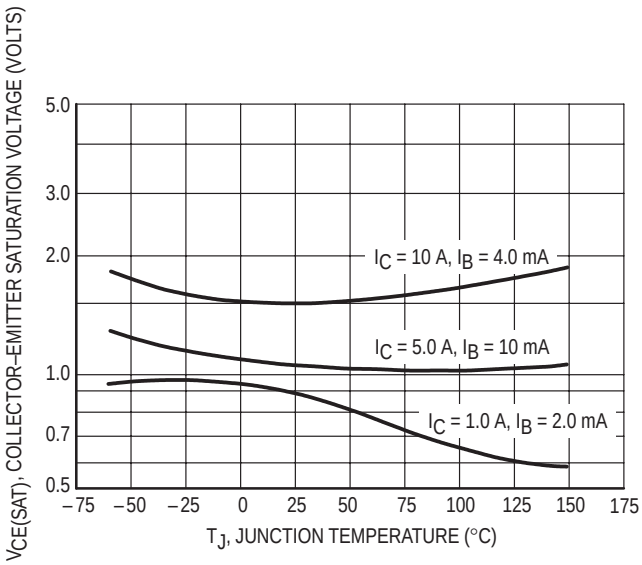
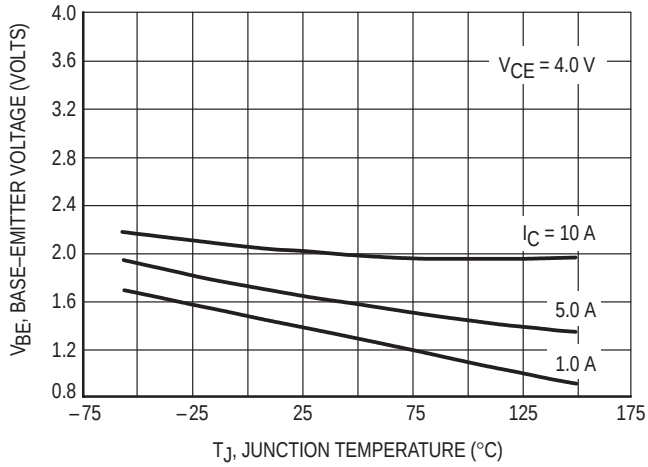


Figure 4. Collector–Emitter Saturation Voltage



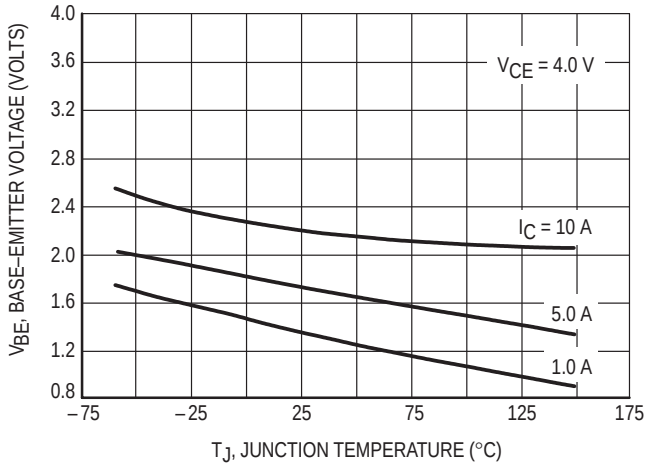


Figure 5. Base–Emitter Voltage

ACTIVE–REGION SAFE OPERATING AREA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

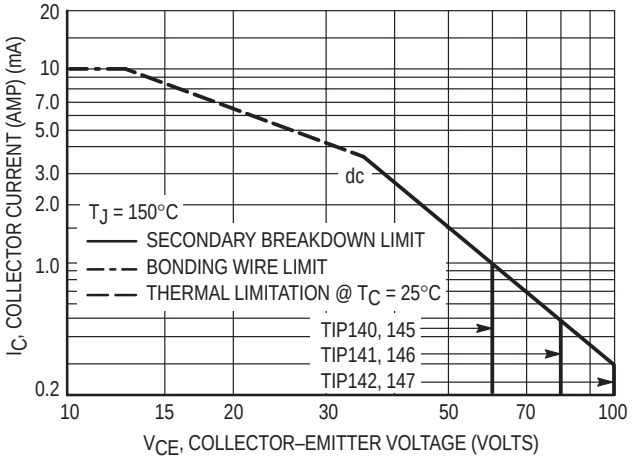


Figure 6. Active–Region Safe Operating Area

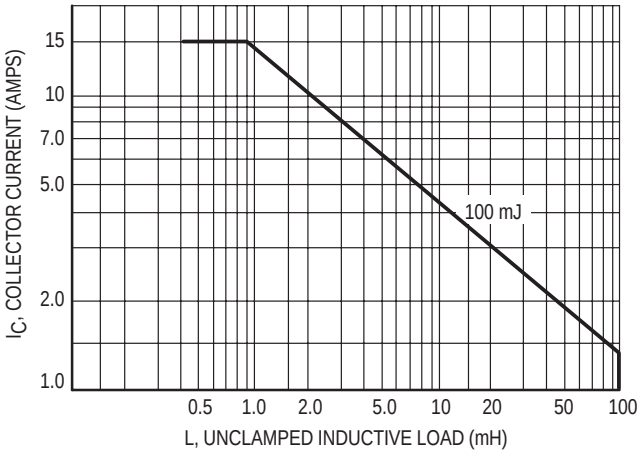
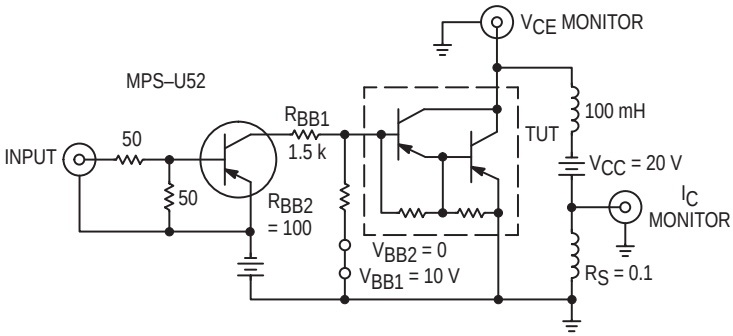
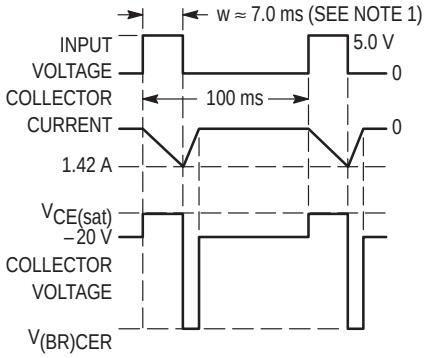


Figure 7. Unclamped Inductive Load



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTE 1: Input pulse width is increased until I_{CM} = 1.42 A.
NOTE 2: For NPN test circuit reverse polarities.

Figure 8. Inductive Load

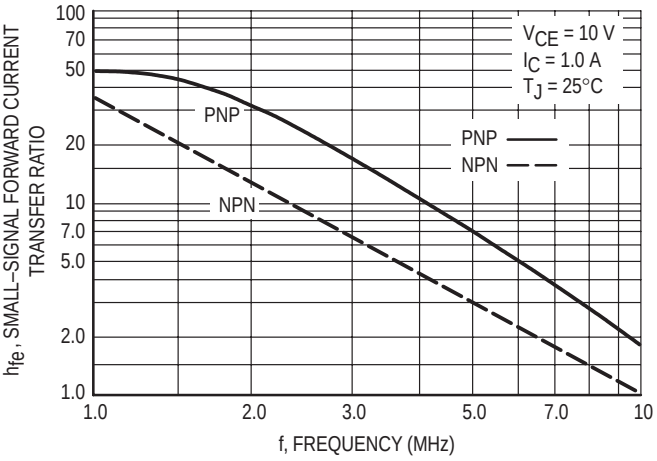


Figure 9. Magnitude of Common Emitter Small–Signal Short–Circuit Forward Current Transfer Ratio

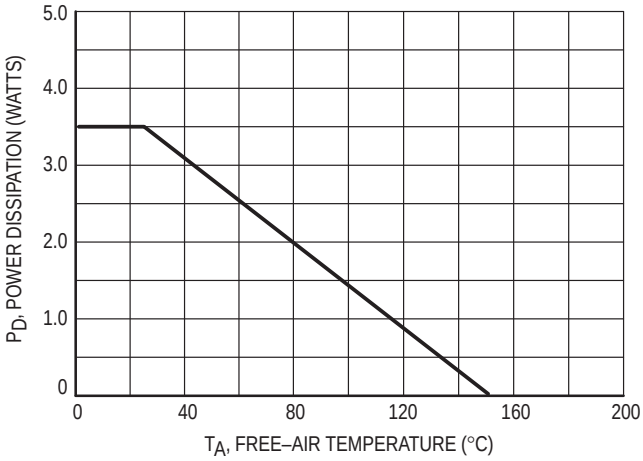


Figure 10. Free–Air Temperature Power Derating

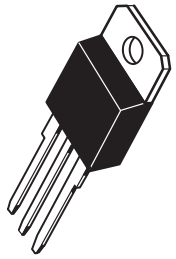
Complementary Silicon Power Transistors

. . . designed for general–purpose switching and amplifier applications.

- DC Current Gain — h_{FE} = 20–70 @ I_C = 4.0 Adc
- Collector–Emitter Saturation Voltage — $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C = 4.0 Adc
- Excellent Safe Operating Area

NPN
TIP3055
PNP
TIP2955

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60 VOLTS
90 WATTS



CASE 340D–01

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	60	Vdc
Collector–Emitter Voltage	V_{CER}	70	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	7.0	Vdc
Collector Current — Continuous	I_C	1 5	Adc
Base Current	I_B	7.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	90 0.72	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.39	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	35.7	°C/W

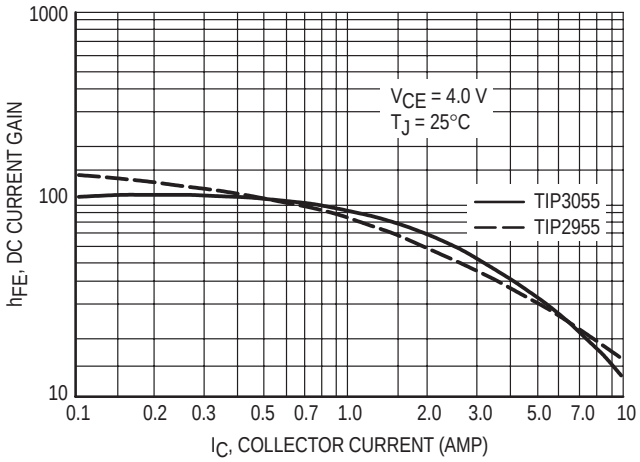


Figure 1. DC Current Gain

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	—	Vdc
Collector Cutoff Current (V_{CE} = 70 Vdc, R_{BE} = 100 Ohms)	I_{CER}	—	1.0	mAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEV}	—	5.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	 20 5.0	 70 —	—
Collector–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	 — —	 1.1 3.0	Vdc
Base–Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	1.8	Vdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 30 Vdc, t = 1.0 s; Nonrepetitive)	$I_{s/b}$	3.0	—	Adc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	—	MHz
Small–Signal Current Gain (V_{CE} = 4.0 Vdc, I_C = 1.0 Adc, f = 1.0 kHz)	h_{fe}	15	—	kHz

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

NOTE: For additional design curves, refer to electrical characteristics curves of 2N3055.

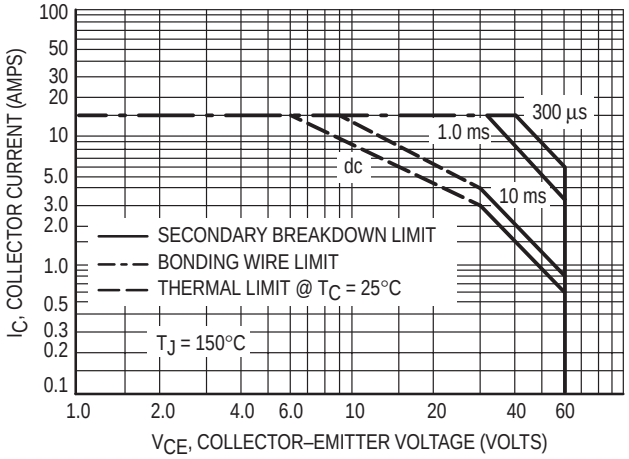
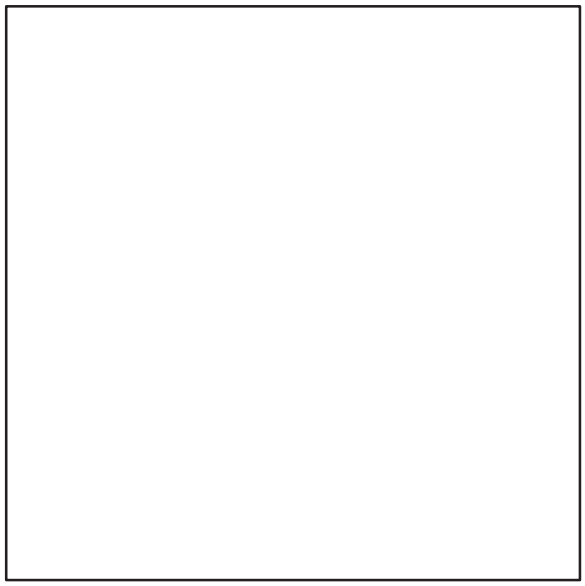


Figure 2. Maximum Rated Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature.

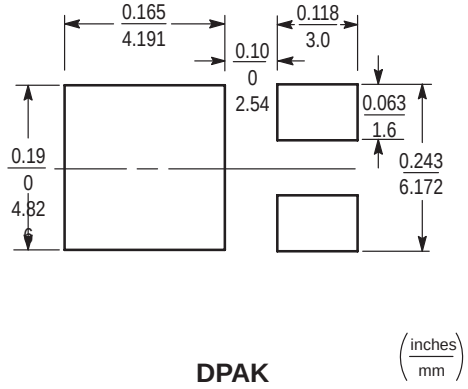


Surface Mount Package Information and Tape and Reel Specifications

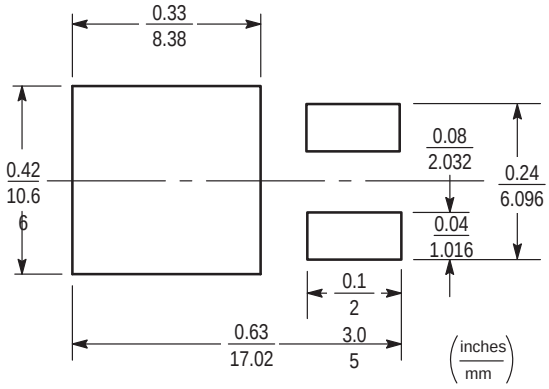
INFORMATION FOR USING SURFACE MOUNT PACKAGES

RECOMMENDED FOOTPRINTS FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



DPAK



D2PAK

POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For example, for a D2PAK, P_D is calculated as follows.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ watts}$$

The 50 °C/W for the D2PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain/collector pad. By increasing the area of the drain/collector pad, the power dissipation can be increased. Although the power dissipation can almost be doubled with this method, area is taken up on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figures 1 and 2.

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

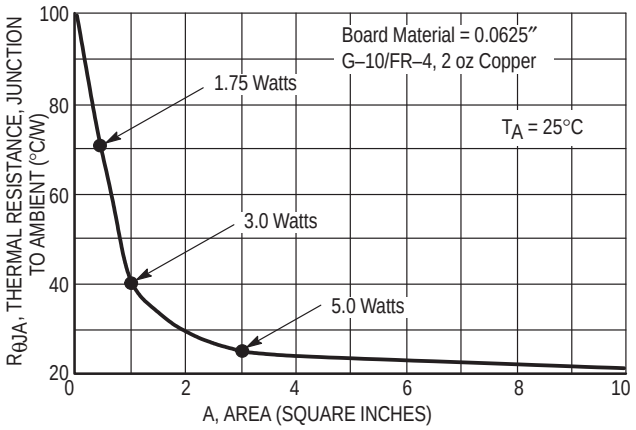


Figure 1. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)

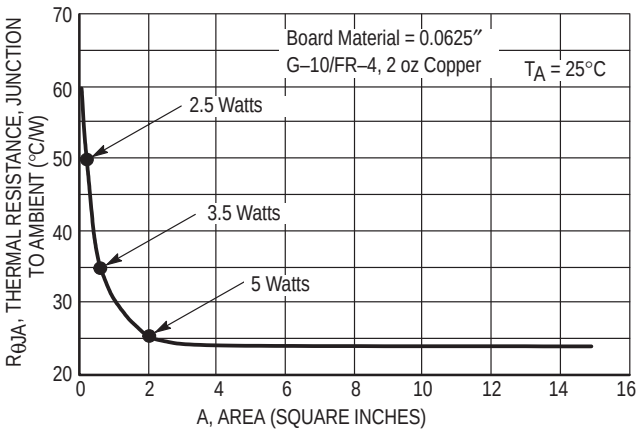


Figure 2. Thermal Resistance versus Drain Pad Area for the D2PAK Package (Typical)

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. This is not the case with the DPAK and D^2PAK packages. If a 1:1 opening is used to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 3 shows a typical stencil for the DPAK and D^2PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

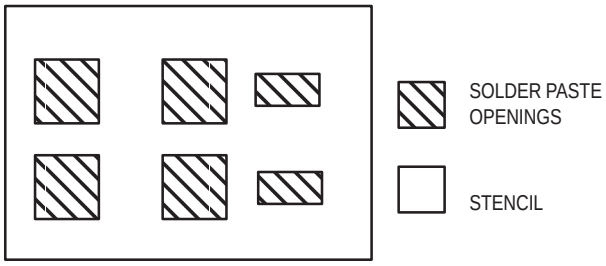


Figure 3. Typical Stencil for DPAK and D^2PAK Packages

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used since the use of forced cooling will increase the temperature gradient and will result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D^2PAK is not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 5 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

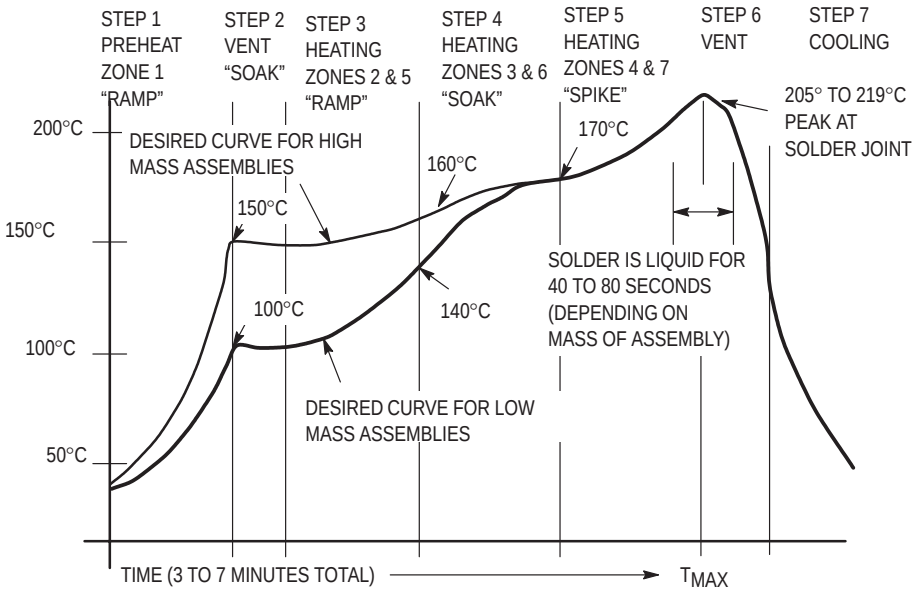


Figure 4. Typical Solder Heating Profile

Mounting Hardware and Techniques

There are many methods available and options possible for installing power semiconductors. A complete discussion of mounting is contained in Motorola Application Note AN1040,"Mounting Considerations for Power Semiconductors," reprinted in Section 6 of this data book. Various suppliers of mounting hardware, listed below, may be contacted for their catalogs which contain considerable technical information.

Sources for Mounting Hardware

Manufacturer	Joint Compound	Adhesives	Insulators						Heatsinks	Clips
			BeO	AlO_2	Anodize	Mica	Plastic Film	Silicone Rubber		
Aavid Eng.	—	—	—	—	—	—	X	X	X	X
AHAM-TOR	—	—	—	—	—	—	—	—	X	—
Asheville-Schoonmaker	—	—	—	—	—	X	—	—	—	—
Astrodynamics	X	—	—	—	—	—	—	—	X	—
Delbert Blinn	—	—	X	—	X	X	X	X	X	—
IERC	X	—	—	—	—	—	—	—	X	—
Staver	—	—	—	—	—	—	—	—	X	—
Thermalloy	X	X	X	X	X	X	X	X	X	X
Tran-tec	X	—	X	X	X	X	—	X	X	—
Wakefield Eng.	X	X	X	—	X	—	—	X	X	X

Other sources for silicone rubber pads: Chomerics, Berquist

Suppliers Addresses

Aavid Engineering, Inc., P.O. Box 400, Laconia, New Hampshire 03247 (603) 528-1478

AHAM-TOR Heatsinks, 27901 Front Street, Rancho, California 92390 (714) 676-4151

Asheville-Schoonmaker, 900 Jefferson Ave., Newport News, VA 23607 (804) 244-7311

Astro Dynamics, Inc., 2 Gill St., Woburn, Massachusetts 01801 (617) 935-4944

Berquist, 5300 Edina Industrial Blvd., Minneapolis, Minnesota 55435 (612) 835-2322

Chomerics, Inc., 16 Flagstone Drive, Hudson, New Hampshire 03051 1-800-633-8800

Delbert Blinn Company, P.O. Box 2007, Pomona, California 91769 (714) 623-1257

International Electronic Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502 (213) 849-2481

The Staver Company, Inc., 41-51 Saxon Avenue, Bay Shore, Long Island, New York 11706 (516) 666-8000

Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234 (214) 243-4321

Tran-tec Corporation, P.O. Box 1044, Columbus, Nebraska 68601 (402) 564-2748

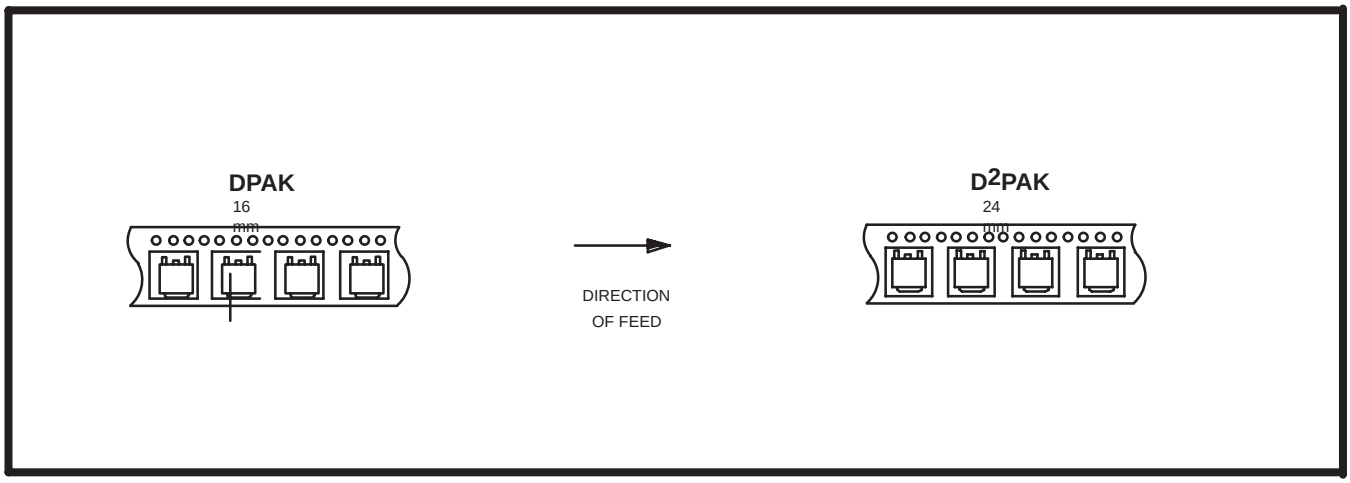
Wakefield Engineering, Inc., Wakefield, Massachusetts 01880 (617) 245-5900

Tape and Reel Specifications and Packaging Specifications

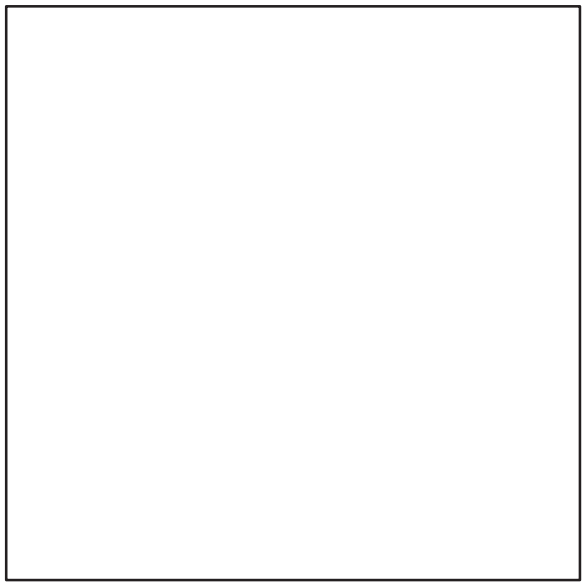
Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the “peel–back” cover tape.

- Two Reel Sizes Available (7″ and 13″)
- Used for Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA 481, –1, –2
- DPAK SO–14, in 16 mm Tape
- D^2PAK in 24 mm Tape

Use the standard device title and add the required suffix as listed in the option table on the following page. Note that the individual reels have a finite number of devices depending on the type of product contained in the tape. Also note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.

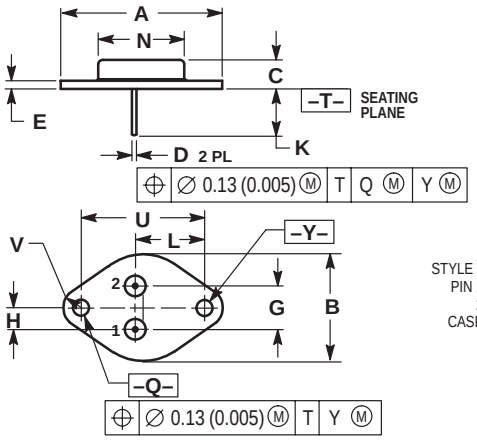


Package	Tape Width (mm)	Reel Size (inch)				
DPAK	16	8.0 ± 0.1 (.315 ± .004)	330	(13)	2,500	T4
D^2PAK	24	16.0 ± 0.1 (.630 ± .004)	330	(13)	800	T4



Outline Dimensions and Leadform Options

Outline Dimensions

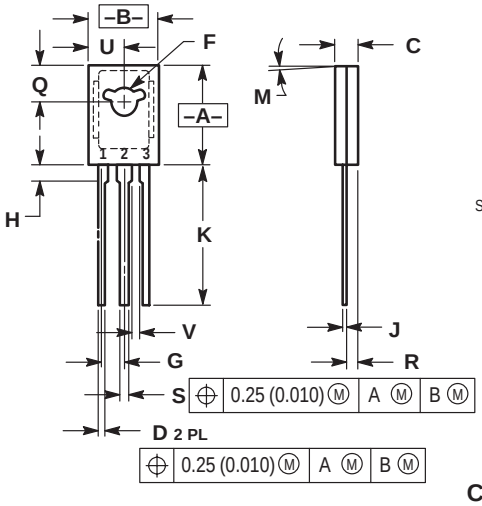


STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

CASE 1–07
(TO–204AA)

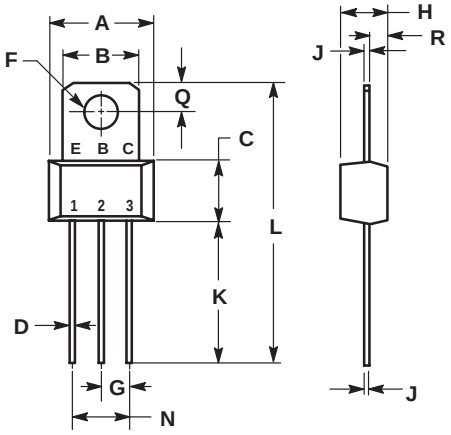


STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.055	1.15	1.39
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	—	1.02	—

CASE 77–08
(TO–225AA)



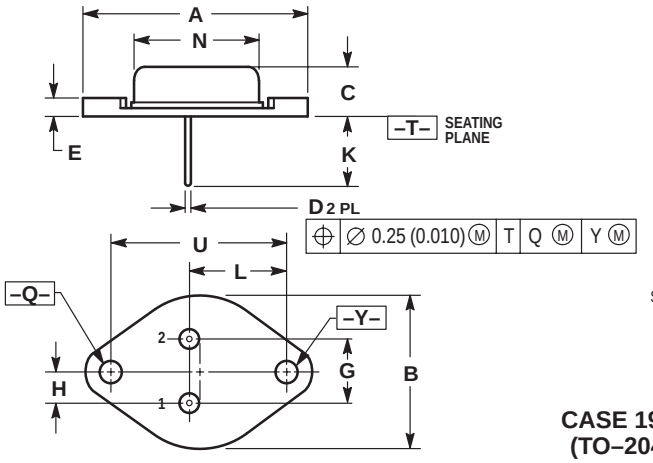
STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR
(COLLECTOR CONNECTED TO TAB)

NOTES:
1. LEADS WITHIN 0.15 (0.006) TOTAL OF TRUE POSITION AT CASE, AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.14	9.53	0.360	0.375
B	6.60	7.24	0.260	0.285
C	5.41	5.66	0.213	0.223
D	0.38	0.53	0.015	0.021
F	3.18	3.33	0.125	0.131
G	2.54 BSC		0.100 BSC	
H	3.94	4.19	0.155	0.165
J	0.36	0.41	0.014	0.016
K	11.63	12.70	0.458	0.500
L	24.58	25.53	0.968	1.005
N	5.08 BSC		0.200 BSC	
Q	2.39	2.69	0.094	0.106
R	1.14	1.40	0.045	0.055

CASE 152-02

Outline Dimensions (continued)

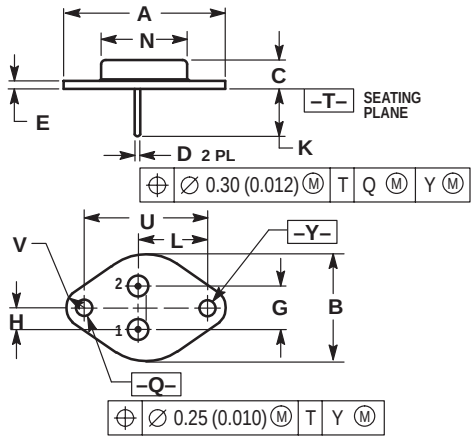


STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	0.980	1.050	24.89	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.135	1.52	3.43
G	0.420	0.440	10.67	11.18
H	0.205	0.225	5.21	5.72
K	0.440	0.480	11.18	12.19
L	0.655	0.675	16.64	17.15
N	0.760	0.830	19.30	21.08
Q	0.151	0.175	3.84	4.19
U	1.177	1.197	29.90	30.40

CASE 197–05
(TO–204AE)

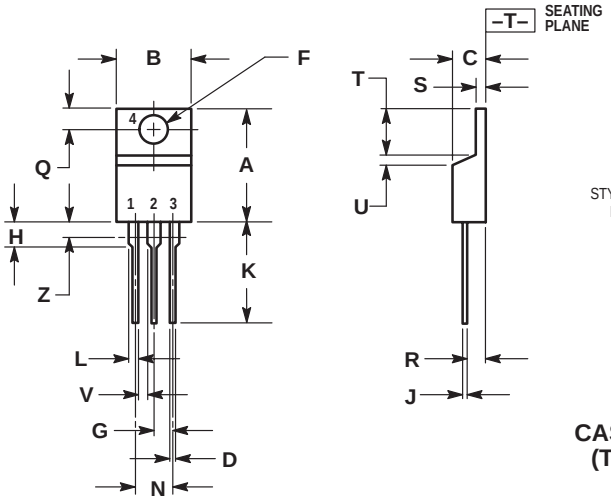


STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

CASE 197A–05
(TO–204AA)



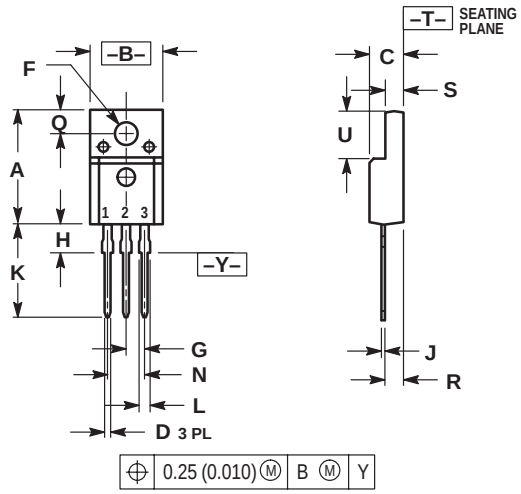
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A–06
(TO220–AB)

Outline Dimensions (continued)

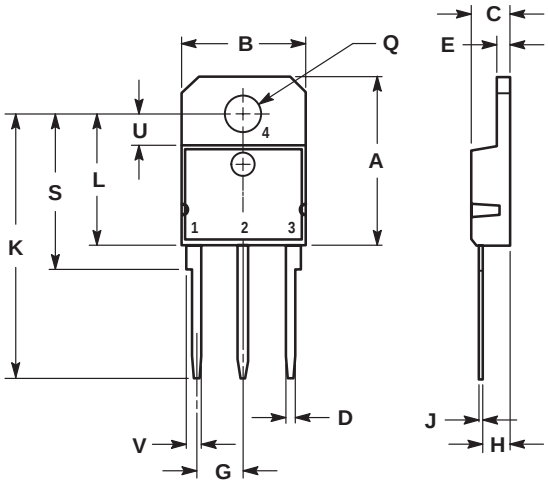


STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

CASE 221D–02
(TO–220)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.621	0.629	15.78	15.97
B	0.394	0.402	10.01	10.21
C	0.181	0.189	4.60	4.80
D	0.026	0.034	0.67	0.86
F	0.121	0.129	3.08	3.27
G	0.100 BSC		2.54 BSC	
H	0.123	0.129	3.13	3.27
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
N	0.200 BSC		5.08 BSC	
Q	0.126	0.134	3.21	3.40
R	0.107	0.111	2.72	2.81
S	0.096	0.104	2.44	2.64
U	0.259	0.267	6.58	6.78

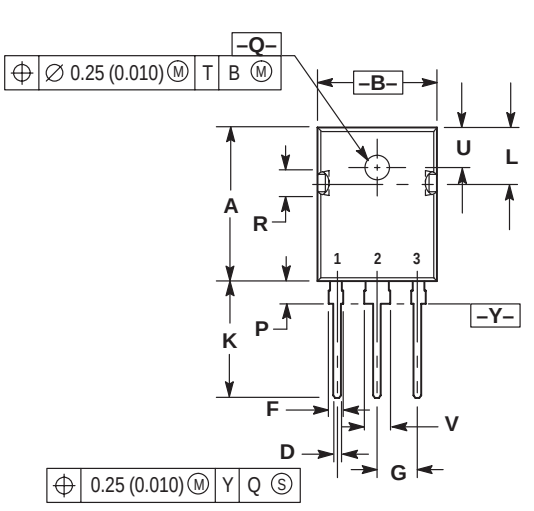


STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340D–01
(TO–218)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.00	19.60	0.749	0.771
B	14.00	14.50	0.551	0.570
C	4.20	4.70	0.165	0.185
D	1.00	1.30	0.040	0.051
E	1.45	1.65	0.058	0.064
G	5.21	5.72	0.206	0.225
H	2.60	3.00	0.103	0.118
J	0.40	0.60	0.016	0.023
K	28.50	32.00	1.123	1.259
L	14.70	15.30	0.579	0.602
Q	4.00	4.25	0.158	0.167
S	17.50	18.10	0.689	0.712
U	3.40	3.80	0.134	0.149
V	1.50	2.00	0.060	0.078



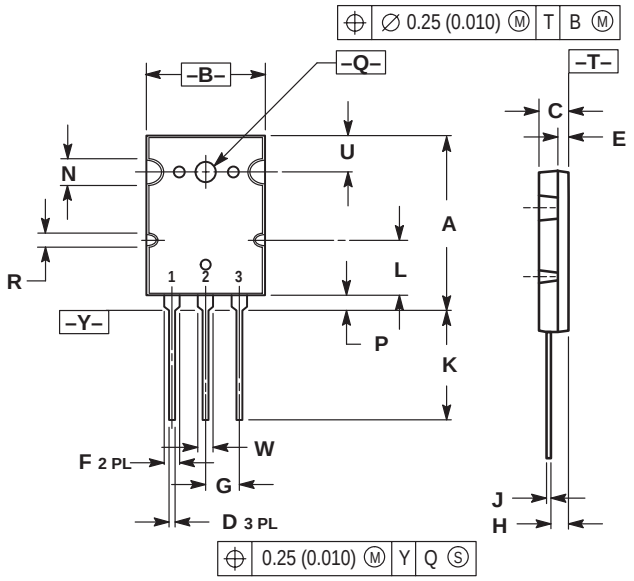
STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340F–03
(TO–247AE)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.40	20.90	0.803	0.823
B	15.44	15.95	0.608	0.628
C	4.70	5.21	0.185	0.205
D	1.09	1.30	0.043	0.051
E	1.50	1.63	0.059	0.064
F	1.80	2.18	0.071	0.086
G	5.45 BSC		0.215 BSC	
H	2.56	2.87	0.101	0.113
J	0.48	0.68	0.019	0.027
K	15.57	16.08	0.613	0.633
L	7.26	7.50	0.286	0.295
P	3.10	3.38	0.122	0.133
Q	3.50	3.70	0.138	0.145
R	3.30	3.80	0.130	0.150
U	5.30 BSC		0.209 BSC	
V	3.05	3.40	0.120	0.134

Outline Dimensions (continued)

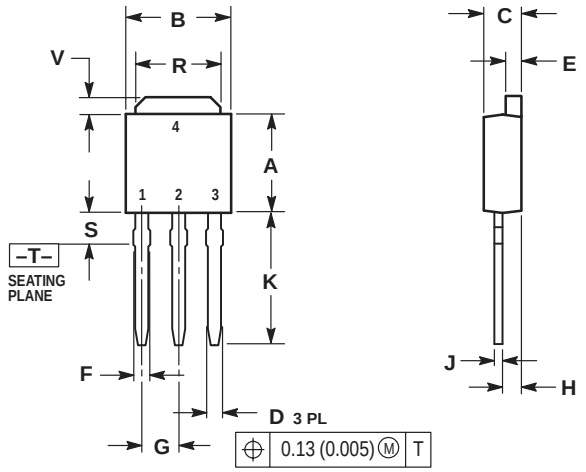


STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

CASE 340G–02
(TO–3PBL)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.8	2.9	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.0	11.4	0.433	0.449
N	3.95	4.75	0.156	0.187
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.15	2.35	0.085	0.093
U	6.1	6.5	0.240	0.256
W	2.8	3.2	0.110	0.125

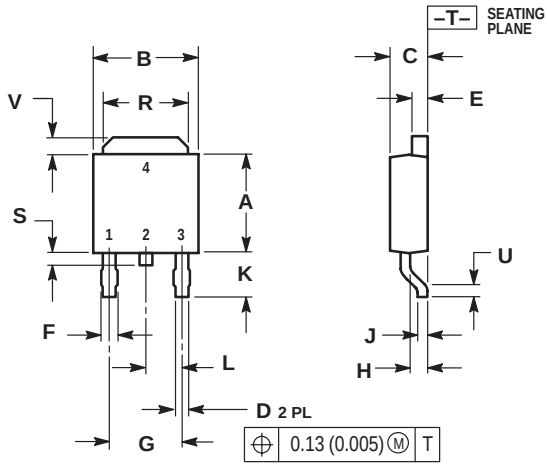


STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 369–07

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 369A–13

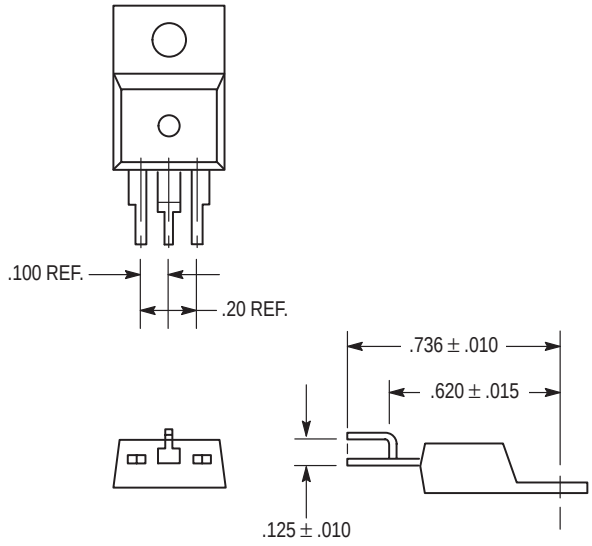
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	—	0.51	—
V	0.030	0.050	0.77	1.27
Z	0.138	—	3.51	—

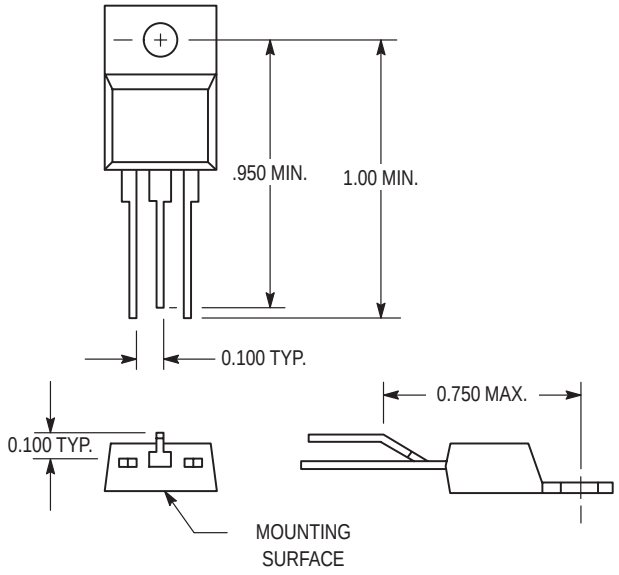
Leadform Options — TO–220 (Case 221A)

- **Leadform options require assignment of a special part number before ordering.**
- **Contact your local Motorola representative for special part number and pricing.**
- **10,000 piece minimum quantity orders are required.**
- **Leadform orders are non–cancellable after processing.**
- **Leadforms apply to both Motorola Case 221A–04 and 221A–06 except as noted.**

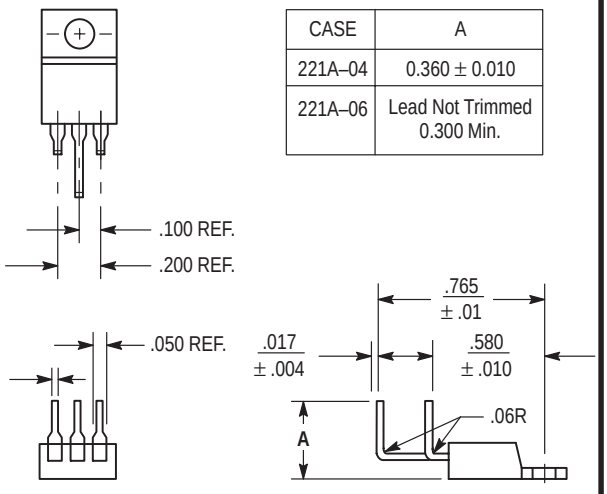
LEADFORM AS



LEADFORM BC



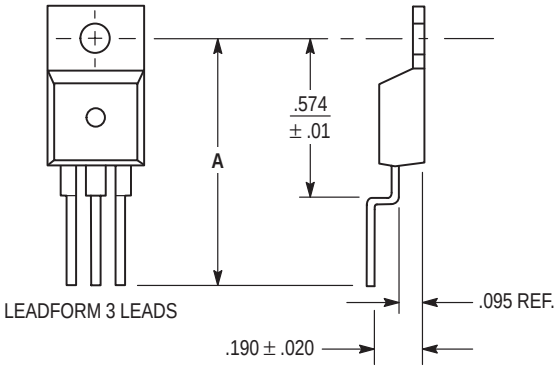
LEADFORM AJ



CASE	A
221A–04	0.360 ± 0.010
221A–06	Lead Not Trimmed 0.300 Min.

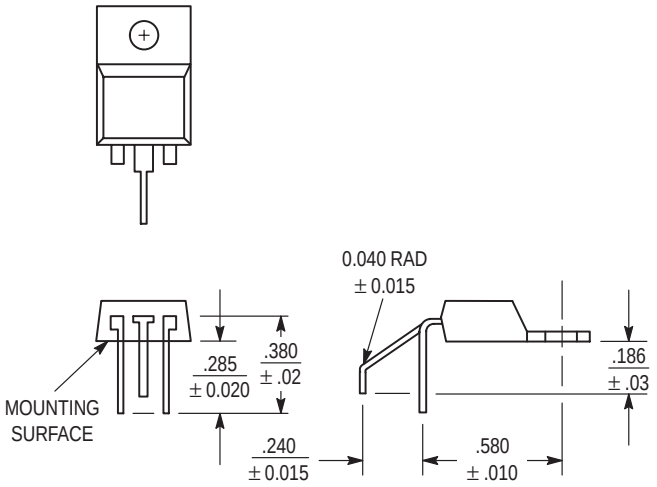
LEADFORM AU

CASE	A
221A–04	0.920 Min.
221A–06	0.885 Min.

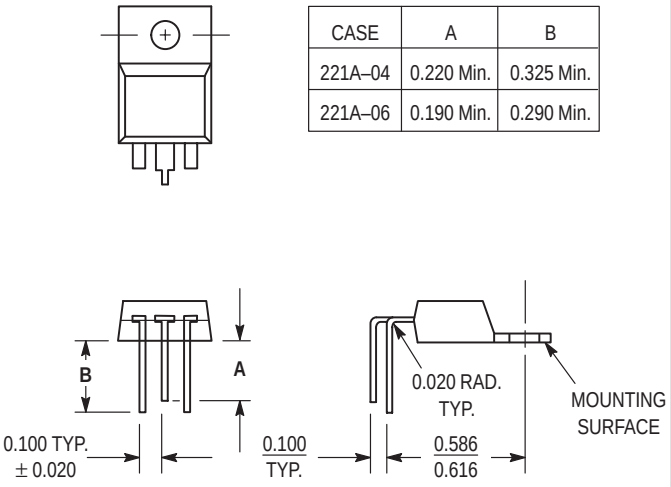


TO–220 Leadform Options (continued)

LEADFORM AN

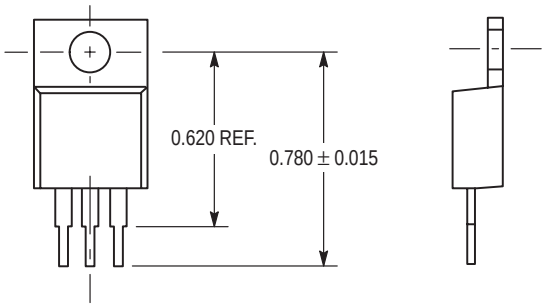


LEADFORM BA



CASE	A	B
221A–04	0.220 Min.	0.325 Min.
221A–06	0.190 Min.	0.290 Min.

LEADFORM BG



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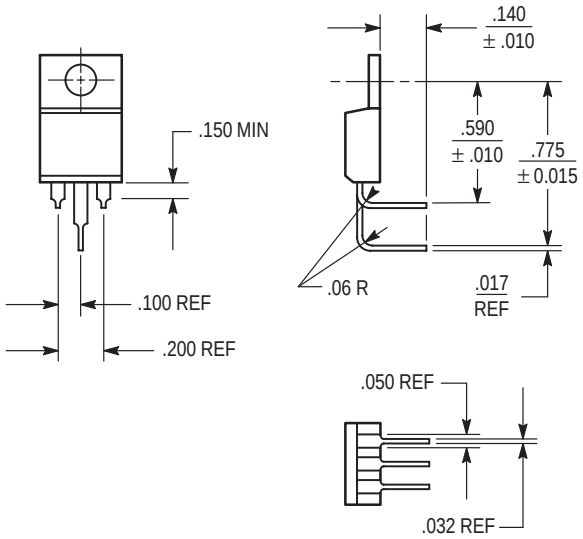

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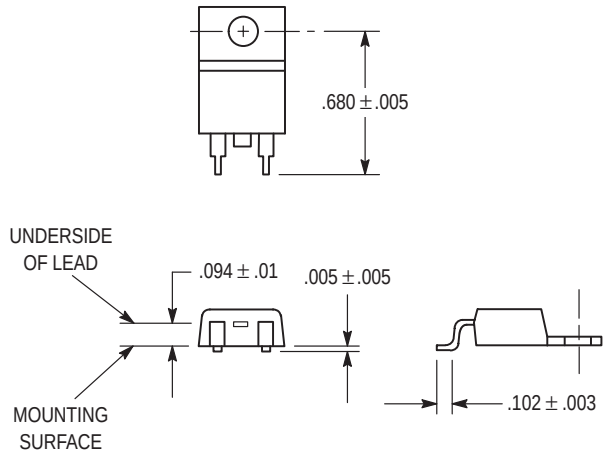

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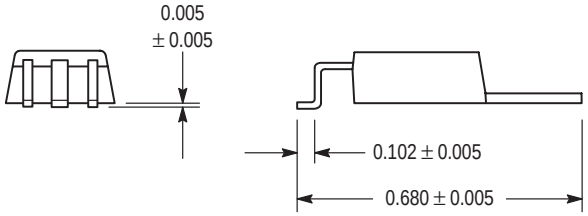
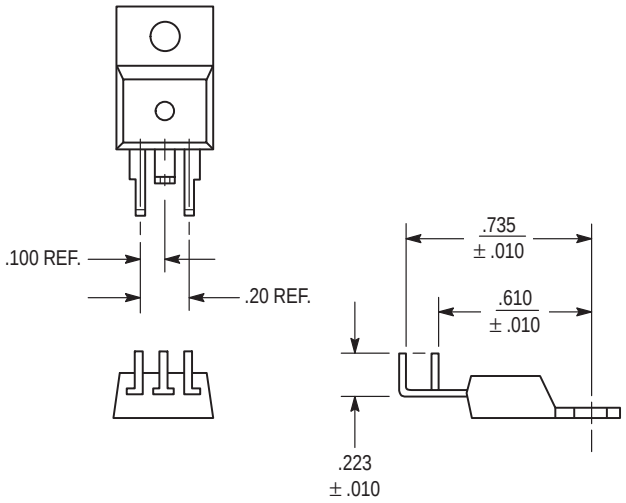


LEADFORM BD



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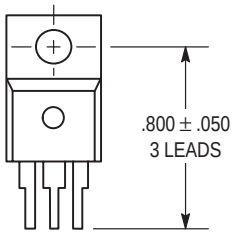
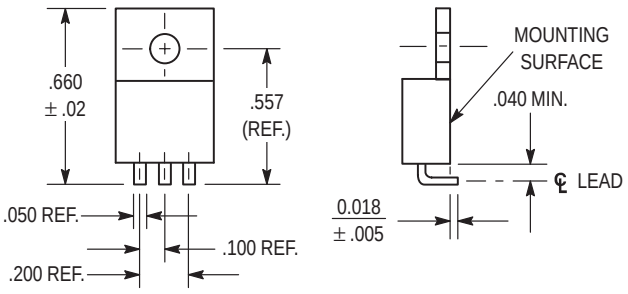


TO–220 Leadform Options (continued)

LEADFORM AF



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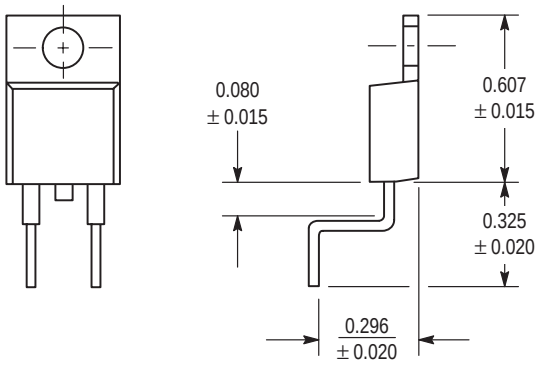
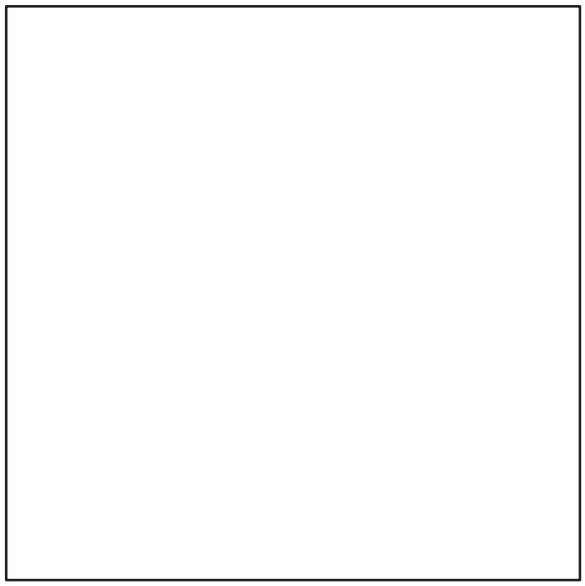




Applications Information

Applications Literature

AN222A The ABC's of Solid State DC–to–AC Inverters

AN485 High–Power Audio Amplifiers with Short–Circuit Protection

AN569 Transient Thermal Resistance—General Data and its Use

AN703 Designing Digitally–Controlled Power Supplies

AN719 A New Approach to Switching Regulators

AN803 The Effect of Emitter–Base Avalanching on High–Voltage Power Switching

AN861 Power Transistors Safe Operating Area – Special Considerations for Motor Drives

AN873 Understanding Power Transistor Dynamic Behavior – dv/dt Effects on Switching RBSOA

AN875 Power Transistor Safe Operating Area – Special Considerations for Switching Power Supplies

AN915 Characterizing Collector–To–Emitter and Drain–To–Source Diodes for Switchmode Applications

AN951 Drive Optimization for 1 kV Offline Converter Transistors

AN952 Ultrafast Recovery Rectifiers Extend Power Transistor SOA

AN1040 Mounting Techniques for Power Semiconductors

AN1049 Electronic Control of Flourescent Tubes

AN1076 Speeding Up Horizontal Outputs

AR109 Power Transistor Safe Operating Area – Special Considerations for Motor Drives

AR119 Dynamic Saturation Voltage – A Designer's Comparison

AR120 Speeding Up the High Voltage Transistor

AR131 Baker Clamps

AR180 Electronic Ballast

AR181 Bipolar Transistors Excel in Off–Line Resonant Converters

AR302 Thermal Management of Surface Mount Power Devices

AR317 Advanced Processing Improves Bipolar Dynamic Saturation

AR319 DPAK: A Surface Mount Package for Discrete Power Devices

AR323 Managing Heat Dissipation in DPAK Surface Mount Power Packages

AR328 Application Specific Transistors

EB85A Full–Bridge Switching Power Supplies

Additional Literature

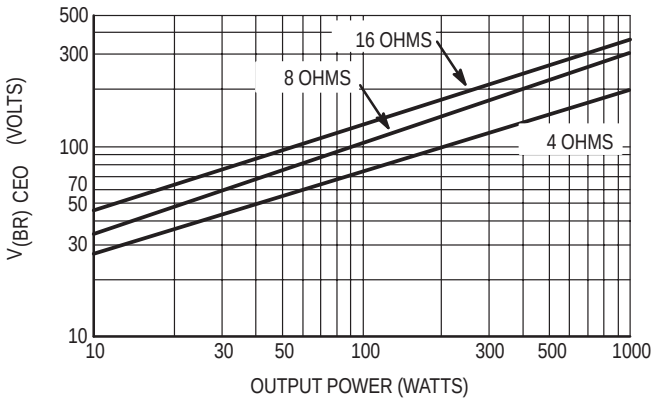
DPAKPAK/D Literature Package for Surface Mount DPAK Power Products

SWMPAK/D Literature Package for Switchmode Power Supply Products

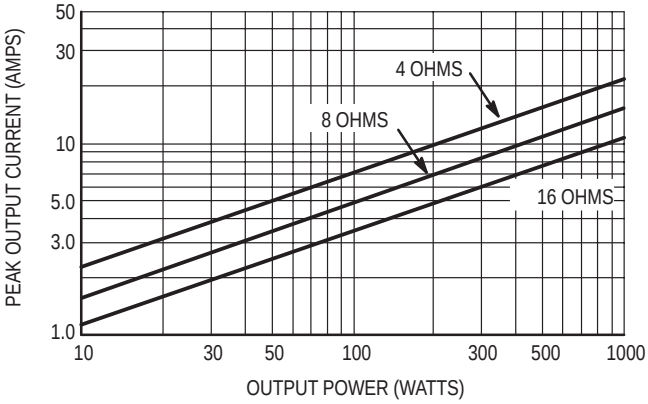
D^{3}PAK/D Literature Package for High Power Surface Mount

Audio
GENERAL DESIGN CURVES FOR POWER AUDIO OUTPUT STAGES

$V_{(BR)CEO}$ Required on Output and Driver Transistor versus Output Power for 4, 8 and 18 Ohm Loads



Output Transistor Peak Collector Current versus Output Power for 4, 8 and 16 Ohm Loads



Another important parameter that must be considered before selecting the output transistors is the safe–operating area these devices must withstand. For a complete discussion see Application Note AN485.

Table 1. Recommended Power Transistors for Audio/Servo Loads

RMS Power Output	NPN	PNP	Case	P_D Watts @ 25°C	V_{CEO}	h_{FE} @ Min/Max	I_C Amps	f_T MHz Typ	ISB Volts/Amps
To 25W	MJE15030	MJE15031	TO–220	50	150	20 min	4	30	14/3.6
	MJE15032	MJE15033	TO–220	50	250	50 min	1	40	50/1
25 to 50W	2N3055A	MJ2955A	TO–204	120	120	20/70	4	3	60/2
	MJ15001	MJ15002	TO–204	200	140	25/150	4	3	40/5
50 to 100W	MJ15015	MJ15016	TO–204	180	120	20/70	4	3	60/3
	MJ15003	MJ15004	TO–204	250	140	25/150	5	3	100/1
	MJ15020	MJ15021	TO–204	150	250	30 min	1	20	50/3
Over 100W	MJ15024	MJ15025	TO–204	250	250	15/60	8	8	80/2.2
	MJ3281A	MJ1302A	TO–204	250	200	60/175	7	30	50/4
	MJL3281A	MJL1302A	340G–01	150	200	60/175	7	30	40/4
	MJ21194	MJ21193	TO–204	250	250	25/75	8	7	100/2
	MJL21194	MJL21193	340G–01	200	200	25/75	8	7	100/2

The Power Transistors shown are provided for reference only and show device capability. The final choice of the Power Transistors used is left to the circuit designer and depends upon the particular safe–operating area required and the mounting and heat sinking configuration used.

CRT Deflection

A new family of SCANSWITCH™ bipolar power transistors, containing state–of–the–art application specific die, and a series of damper diodes have been designed for high and very high resolution horizontal deflection circuits. The horizontal output transistors minimize fall time, storage time and dynamic desaturation; turn–off energy is specified for optimum design considerations. The power rectifiers, designed for use as damper diodes in horizontal deflection circuits, are enhanced for turn–on overshoot voltage and forward recovery time. Overall circuit performance is optimized when these damper diodes are paired with their specific horizontal output transistors.

Dynamic Desaturation

A large amount of power dissipation in horizontal deflection output circuitry occurs during the transistor's turn–off. Most of this dissipation happens as the collector–emitter voltage rises during storage time. Since there is a tendency for the voltage waveform to be soft and rou1nded as opposed to abrupt and square. The parameter used to describe this behavior is dynamic desaturation and is shown in Figure A as the area below the dashed line. The SCANSWITCH series of transistors has been designed to minimize dynamic desaturation and simultaneously avoid collector current tailing.

Optimized Base Drive

The base drive can be optimized to take full advantage of the advanced device design of the SCANSWITCH series of transistors. The five conditions necessary for optimization are:

1) Provide adequate drive just prior to turn–off to minimize dynamic desaturation.

2) Avoid overdrive during any portion of the turn–on time to avoid collector current tailing.

3) Provide reverse base current that is independent of forward base current so full transistor performance can be realized.

4) Provide for a controlled rate of transition from forward to reverse drive to avoid tailing.

5) Avalanche the base–emitter junction during fall time.

Typical techniques for driving horizontal outputs use a base drive waveform which results in overdrive at turn–on and underdrive just prior to turn–off. An optimized base drive is one with the same forced gain throughout the turn–on period. A comparison of the two drives is shown in Figure B.

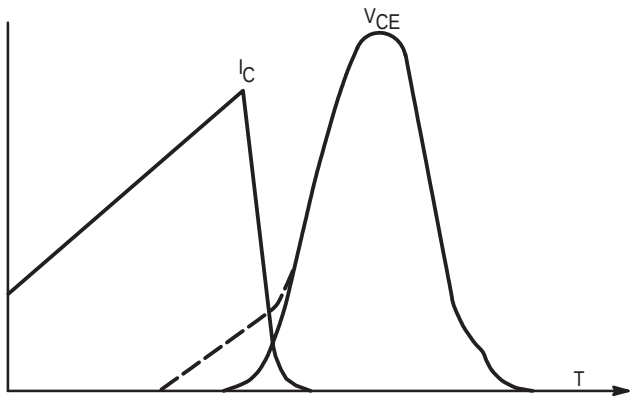


Figure A. Dynamic Desaturation

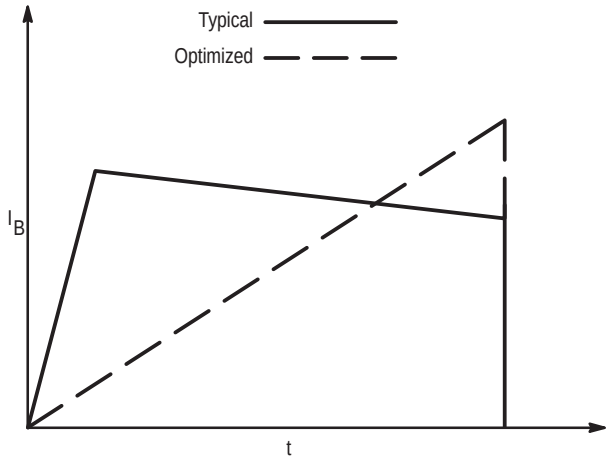


Figure B. Base Drive Comparison

Table 2. Horizontal CRT Deflection Transistor Selector Guide

Monitor Description	Horizontal Scan Freq.	CRT Size	Pixel Size	Transistor	Diode
Monochrome					
Low Resolution to Mid Resolution	15–50 kHz	12–15 in.	>1024 x 768	MJE/MJF16204	MUR860E
High Resolution	50–100 kHz	15–19 in.	>2000 x 1600	MJW16206 MJW16210 MJW16212	MR/MUR10120E MR/MUR10120E MR/MUR10150E
Ultra–High Resolution	>100 kHz	19–24 in.	>2000 x 2000	MJL16218	MR/MUR10150E
Color					
Low Resolution	15–22 kHz	12–15 in.	>320 x 200	BU508A	MUR5150E
Mid Resolution	22–50 kHz	12–15 in.	>1024 x 768	BU508A	MUR5150E
High Resolution	50–90 kHz	17–27 in.	>1280 x 1024	MJW16206 MJW16210 MJW16212	MR/MUR10120E MR/MUR10120E MR/MUR10150E
Ultra–High Resolution	>90 kHz	17–27 in.	>1600 x 1280	MJW16210(17) MJL16218	MUR8100E(17) MR/MUR10150E

(15) To be introduced.
(17) Use two in parallel.

AN1040

Mounting Considerations For Power Semiconductors

Prepared by: Bill Roehr
Staff Consultant, Motorola Semiconductor Sector

TABLE OF CONTENTS

INTRODUCTION

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead–mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one–half for a decrease in junction temperature from 160°C to 135°C.(1) Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.(2) Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger.

Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic–packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

(1) MIL–HANDBOOK — 2178, SECTION 2.2.
(2) "Navy Power Supply Reliability — Design and Manufacturing Guidelines" NAVMAT P4855–1, Dec. 1982 NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.

Figure 1 shows an example of doing nearly everything wrong. A tab mount TO–220 package is shown being used as a replacement for a TO–213AA (TO–66) part which was socket mounted. To use the socket, the leads are bent — an operation which, if not properly done, can crack the package, break the internal bonding wires, or crack the die. The package is fastened with a sheet–metal screw through a 1/4″ hole containing a fiber–insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, possibly causing enough distortion to crack the die. In addition the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all poor mounting practices would be covered.

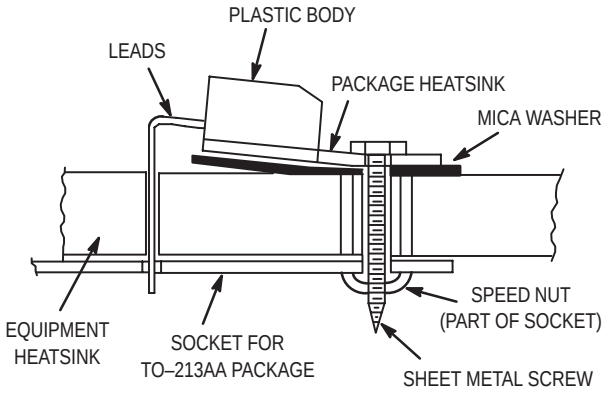


Figure 1. Extreme Case of Improperly Mounting a Semiconductor (Distortion Exaggerated)

In many situations the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc–over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:

1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:

Stud Mount
Flange Mount
Pressfit
Plastic Body Mount
Tab Mount
Surface Mount

Appendix A contains a brief review of thermal resistance concepts. Appendix B discusses measurement difficulties with interface thermal resistance tests. Appendix C indicates the type of accessories supplied by a number of manufacturers.

MOUNTING SURFACE PREPARATION

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high–power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 2. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e, $\Delta h/TIR$, if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.

Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory; a finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy using a copper TO–204 (TO–3) package with a typical 32–microinch finish, showed that heatsink finishes between 16 and 64 μ–in caused less than ± 2.5% difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.(3) Most commercially available cast or extruded heatsinks will require spotfacing when used in high–power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO–3, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This “crater” in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat–dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early–life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine–edge blanking or sheared–through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four–post die sets equipped with proper pressure pads and holding fixtures.

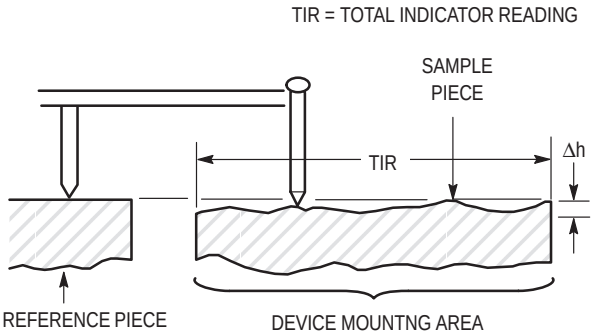


Figure 2. Surface Flatness Measurement

(3) Catalog #87–HS–9, (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381–0839.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

Surface Treatment

Many aluminum heatsinks are black–anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromateacid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 volts.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

INTERFACE DECISIONS

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pock–marked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section.

To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal and therefore partially fill voids when under pressure.

Thermal Compounds (Grease)

Joint compounds are a formulation of fine zinc or other conductive particles in a silicone oil or other synthetic base fluid which maintains a grease–like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic–encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the semiconductor chip.

The silicone oil used in most greases has been found to evaporate from hot surfaces with time and become deposited on other cooler surfaces. Consequently, manufacturers must determine whether a microscopically thin coating of silicone oil on the entire assembly will pose any problems. It may be necessary to enclose components using grease. The newer synthetic base greases show far less tendency to migrate or creep than those made with a silicone oil base. However, their currently observed working temperature range are less, they are slightly poorer on thermal conductivity and dielectric strength and their cost is higher.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

Conductive Pads

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a greased bare joint and a joint using Grafoil, a dry graphite compound, is shown in the data of Figure 3. Grafoil is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from Aavid is called KON–DUX. It is made with a unique, grain oriented, flake–like structure (patent pending). Highly compressible, it becomes formed to the surface roughness of both the heatsink and semiconductor. Manufacturer's data

Table 1. Approximate Values for Interface Thermal Resistance Data from Measurements Performed in Motorola Applications Engineering Laboratory

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink. (See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

Package Type and Data		Interface Thermal Resistance (°C/W)						
			Metal–to–Metal		With Insulator			
JEDEC Outlines	Description	Test Torque In–Lb	Dry	Lubed	Dry	Lubed	Type	See Note
DO–203AA, TO–210AA TO–208AB	10–32 Stud 7/16″ Hex	15	0.3	0.2	1.6	0.8	3 mil Mica	
DO–203AB, TO–210AC TO–208	1/4–28 Stud 11/16″ Hex	25	0.2	0.1	0.8	0.6	5 mil Mica	
DO–208AA	Pressfit, 1/2″	—	0.15	0.1	—	—	—	
TO–204AA (TO–3)	Diamond Flange	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO–213AA (TO–66)	Diamond Flange	6	1.5	0.5	2.3	0.9	2 mil Mica	
TO–126	Thermopad 1/4″ x 3/8″	6	2.0	1.3	4.3	3.3	2 mil Mica	
TO–220AB	Thermowatt	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

NOTES: 1. See Figures 3 and 4 for additional data on TO–3 and TO–220 packages.
2. Screw not insulated. See Figure 12.

shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers. They are a fairly recent development; long term problems, if they exist, have not yet become evident.

INSULATION CONSIDERATIONS

Since most power semiconductors use are vertical device construction it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non isolated packages. In these situations insulators are used to isolate the individual components from the heatsink. Newer packages, such as the Motorola Full Pak and EMS modules, contain the electrical isolation material within, thereby saving the equipment manufacturer the burden of addressing the isolation problem.

Insulator Thermal Resistance

When an insulator is used, thermal grease is of greater importance than with a metal–to–metal contact, because two interfaces exist instead of one and some materials, such as mica, have a hard, markedly uneven surface. With many isolation materials reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO–204 (TO–3) and TO–220 packages, are shown in Figure 3, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case).

Referring to Figure 3, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraided, as the dust is highly toxic.) Thermafilm is a filled polyimide material which is used for isolation (variation of Kapton). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high breakdown voltage and fairly low thermal resistance at a low cost but it certainly should be used with grease.

Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut–through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton or fiberglass. By comparing Figures 3c and 3d, it can be noted that Thermasil, a filled silicone rubber, without grease, has about the same interface thermal resistance as greased mica for the TO–220 package.

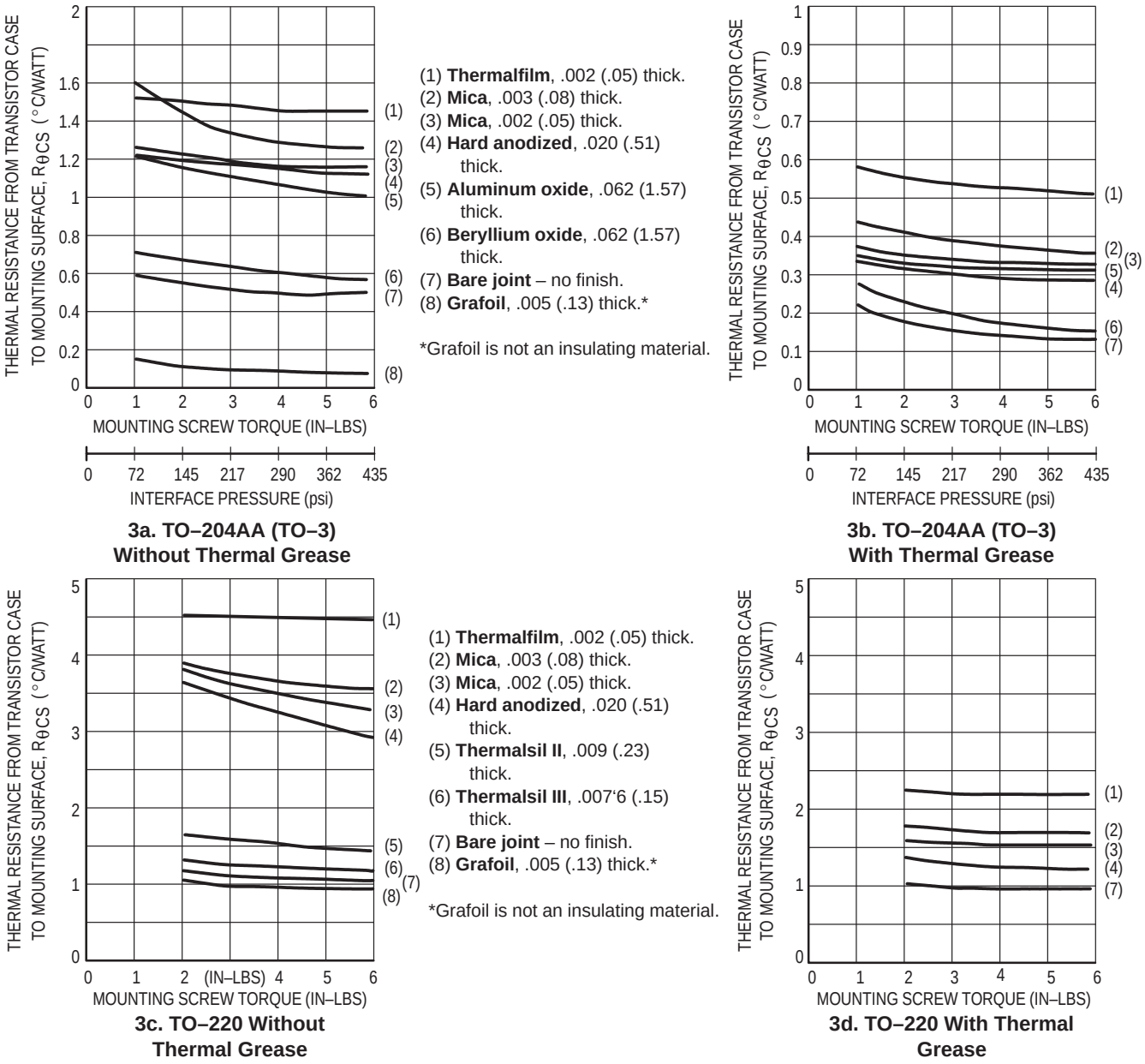


Figure 3. Interface Thermal Resistance for TO–204, TO–3 and TO–220 Packages using Different Insulating Materials as a Function of Mounting Screw Torque (Data Courtesy Thermalloy)

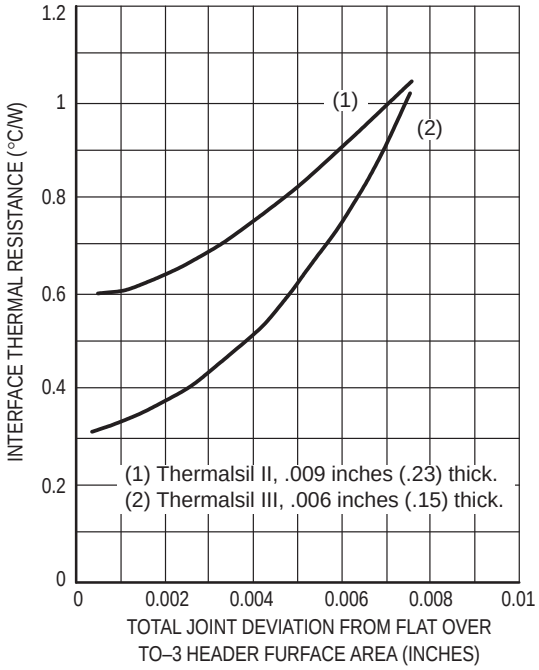
A number of manufacturers offer silicone rubber insulators. Table 2 shows measured performance of a number of these insulators under carefully controlled, nearly identical conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out–of–flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K–10 pad, for example, is described as having about 2/3 the interface resistance of the Sil Pad 1000 which would place its performance close to the Chomerics 1671 pad. AAVID also offers an isolated pad called Rubber–Duc, however it is only available vulcanized to a heatsink and therefore was not included in the comparison. Published data from AAVID shows $R_{\theta CS}$ below 0.3°C/W for pressures above 500 psi. However, surface flatness and other details are not specified so a comparison cannot be made with other data in this note.

Table 2. Thermal Resistance of Silicone Rubber Pads

Manufacturer	Product	$R_{\theta CS}$ @ 3 Mils*	$R_{\theta CS}$ @ 7.5 Mils*
Wakekfield	Delta Pad 173–7	.790	1.175
Bergquist	Sil Pad K–4	.752	1.470
Stockwell Rubber	1867	.742	1.015
Bergquist	Sil Pad 400–9	.735	1.205
Thermalloy	Thermalsil II	.680	1.045
Shin–Etsu	TC–30AG	.664	1.260
Bergquist	Sil Pad 400–7	.633	1.060
Chomerics	1674	.592	1.190
Wakefield	Delta Pad 174–9	.574	.755
Bergquist	Sil Pad 1000	.529	.935
Ablestik	Thermal Wafers	.500	.990
Thermalloy	Thermalsil III	.440	1.035
Chomerics	1671	.367	.655

*Test Fixture Deviation from flat from Thermalloy EIR86–1010.

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO–204AA (TO–3) package insulated with Thermasil is shown on Figure 4. Observe that the “worst case” encountered (7.5 mils) yields results having about twice the thermal resistance of the “typical case” (3 mils), for the more conductive insulator. In order for Thermasil lll to exceed the performance of greased mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.



Data courtesy of Thermalloy

Figure 4. Effect of Total Surface Flatness on Interface Resistance Using Silicon Rubber Insulators

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the Cho–Therm 1688 pad thermal interface impedance dropped from 0.90°C/W to 0.70°C/W at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R_{\theta CS}$ measured 0.74°C/W. The torque on the conventional mounting hardware had decreased to 3 in–lb from an initial 6 in–lb. With nonconformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Table 3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing ASTM Committee D9 is developing a standard for interface measurements.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will out perform the commonly used mica with grease. Cost may be a determining factor in making a selection.

Table 3. Performance of Silicon Rubber Insulators Tested Per MIL–I–49456

Material	Measured Thermal Resistance (°C/W)	
	Thermalloy Data(1)	Berquist Data(2)
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	—
Cho–Therm, 1617	0.233	—
Q Pad (non–insulated)	—	0.009
Sil–Pad, K–10	0.263	0.200
Thermasil III	0.267	—
Mica, greased	0.329	0.400
Sil–Pad 1000	0.400	0.300
Cho–therm 1674	0.433	—
Thermasil II	0.500	—
Sil–Pad 400	0.533	0.440
Sil–Pad K–4	0.583	0.440

(1) From Thermalloy EIR 87–1030
(2) From Berquist Data Sheet

Insulation Resistance

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly; so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi–pot testing should be done on prototypes and a large margin of safety employed.

Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost–effective insulated packages since the 1950’s. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late eighties, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The EMS (Energy Management Series) Modules, shown on Figure 8, Case 806 (ICePAK) and Case 388A (TO–258AA) (see Figure 11) are examples of parts in this category. The second category contains parts which have a plastic overmold covering the metal mounting base. The isolated, Case 221C, illustrated in Figure 13, is an example of parts in the second category.

Parts in the first category — those with an exposed metal flange or tab — are mounted the same as their non–insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the overmolded type should be used with a conical compression washer, described later in this note.

FASTENER AND HARDWARE CHARACTERISTICS

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 5, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection — generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A new variation of the conical washer includes it as part of a nut assembly. Called a Sync Nut, the patented device can be soldered to a PC board and the semiconductor mounted with a 6–32 machine screw.(4)

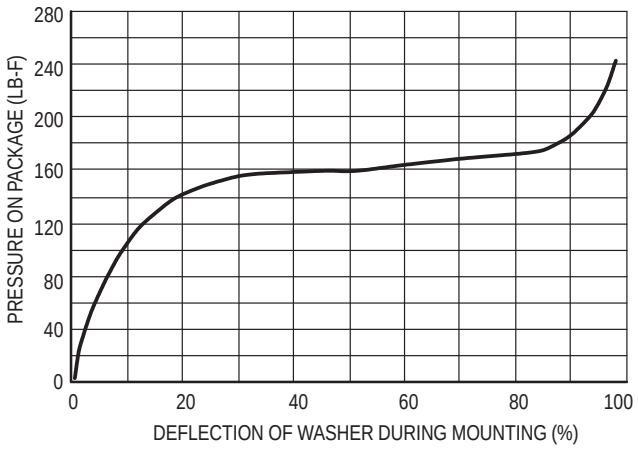


Figure 5. Characteristics of the Conical Compression Washers Designed for Use with Plastic Body Mounted Semiconductors

Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small boardmounted or free–standing heat dissipaters with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO–220 and TO–126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO–220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

Machine Screws

Machine screws, conical washers, and nuts (or syncnuts) can form a trouble–free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case may occur.

Self–Tapping Screws

Under carefully controlled conditions, sheet–metal screws are acceptable. However, during the tapping process with a standard screw, a volcano–like protrusion will develop in the metal being threaded; an unacceptable surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speednut. If a self tapping process is desired, the screw type must be used which roll–forms machine screw threads.

Rivets

Rivets are not a recommended fastener for any of the plastic packages. When a rugged metal flange–mount package or EMS module is being mounted directly to a heatsink, rivets can be used provided press–riveting is used. Crimping force must be applied slowly and evenly. Pop–riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional belt–furnace, irons, vapor–phase reflow, and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

(4) ITW Shakeproof, St. Charles Road, Elgin, IL 60120.

Adhesives

Adhesives are available which have coefficients of expansion compatible with copper and aluminum.(5) Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non–field serviceable systems or low strength types for field serviceable systems. Adhesive bonding is attractive when case mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

Plastic Hardware

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.

FASTENING TECHNIQUES

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel– or gold–plated. Consequently, precautions must be taken not to mar the finish.

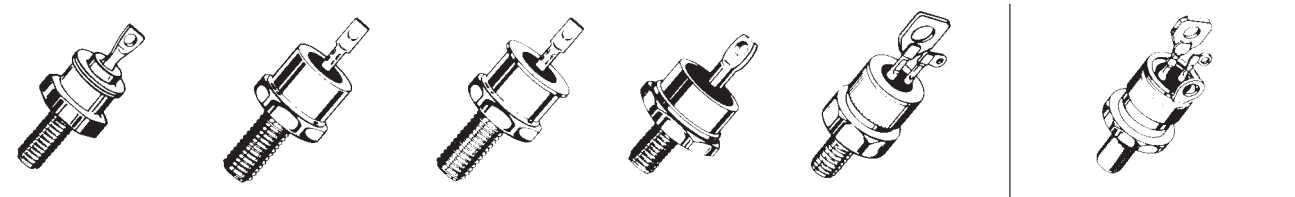
Another factor to be considered is that when a copper based part is rigidly mounted to an aluminum heatsink, a bimetallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminum, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws the semiconductor chip could be damaged. Bending can be minimized by:

1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some slip between surfaces can occur as temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semiconductor to minimize the temperature gradient and allow for movement.

Stud Mount

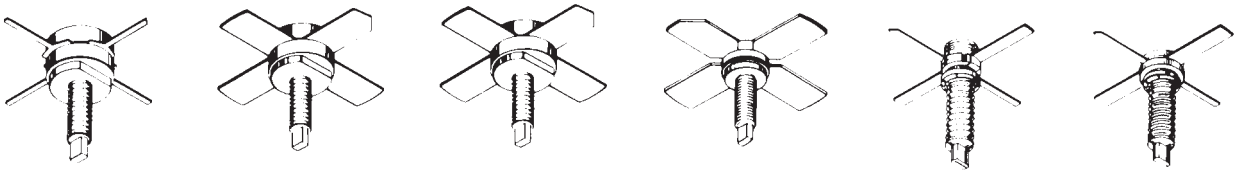
Parts which fall into the stud–mount classification are shown in Figure 6. Mounting errors with non–insulated stud–mounted parts are generally confined to application of excessive torque or tapping the stud into a threaded heatsink hole. Both these practices may cause a warpage of the hex base which may crack the semiconductor die. The only recommended fastening method is to use a nut and washer; the details are shown in Figure 7.

(5) Robert Batson, Elliot Fraunglass and James P Moran, “Heat Dissipation Through Thermalloy Conductive Adhesives,” EMTAS ’83. Conference, February 1 – 3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI 48128.



CASE 42A (DO–5) | **CASE 56–03 DO–203AA (DO–4)** | **CASE 245 (DO–4)** | **CASE 257 DO–203AB (DO–5)** | **CASE 263–04** | **CASE 311–02**

6a. Standard Non–Isolated Types | **6b. Isolated Type**



CASE 144B–05 (.380″ STUD) | **CASE 145A–09 (.380″ STUD)** | **CASE 145A–10 (.500″ STUD)** | **CASE 244–04 (.280″ STUD)** | **CASE 305–01 (.204″ STUD)** | **CASE 332–04 (.380″ STUD)**

6c. RF Stripline Opposed Emitter (SOE) Series

Figure 6. A Variety of Stud–Mount Parts

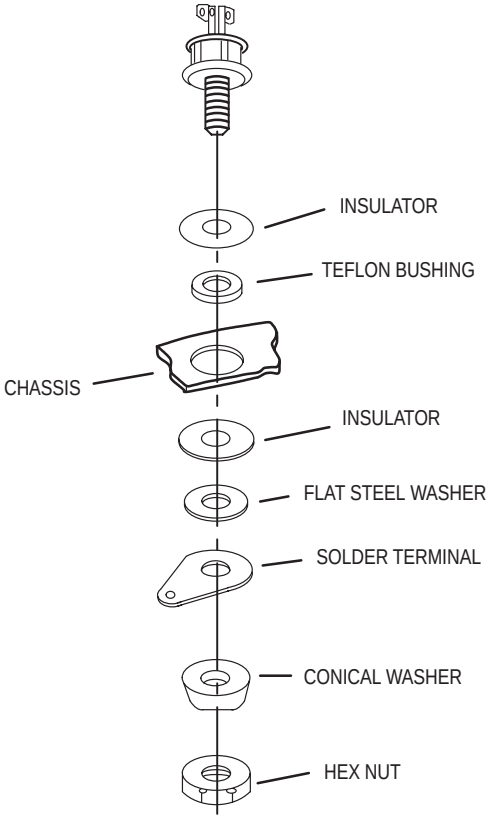


Figure 7. Isolating Hardware Used for a Non–IsolatedStud–Mount Package

Insulated electrode packages on a stud mount base require less hardware. They are mounted the same as their non–insulated counterparts, but care must be exercised to avoid applying a shear or tension stress to the insulation layer, usually a berrylium oxide (BeO) ceramic. This requirement dictates that the leads must be attached to the circuit with flexible wire. In addition, the stud hex should be used to hold the part while the nut is torqued.

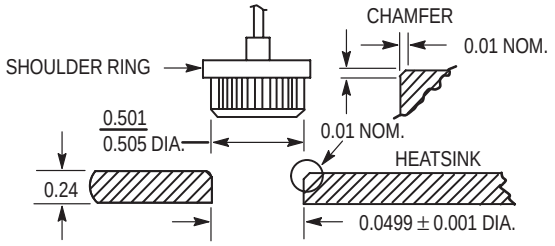
R.F. transistors in the stud–mount stripline opposed emitter (SOE) package impose some additional constraints because of the unique construction of the package. Special techniques to make connections to the stripline leads and to mount the part so no tension or shear forces are applied to any ceramic — metal interface are discussed in the section entitled “Connecting and Handling Terminals.”

Press Fit

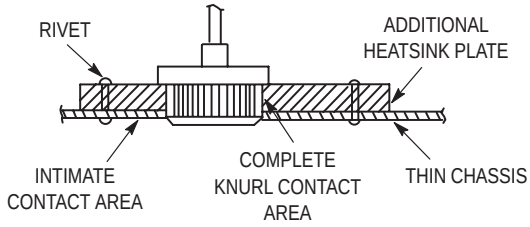
For most applications, the press–fit case should be mounted according to the instructions shown in Figure 8. A special fixture meeting the necessary requirements must be used.

Flange Mount

A large variety of parts fit into the flange mount category as shown in Figure 9. Few known mounting difficulties exist with the smaller flange mount packages, such as the TO–204 (TO–3). The rugged base and distance between die and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. It is therefore good practice



Heatsink Mounting



Thin–Chassis Mounting

The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the case during press–in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the heatsink material. Recommended hardnesses are: copper–less than 50 on the Rockwell F scale; aluminum–less than 65 on the Brinell scale. A heatsink as thin as 1/8″ may be used, but the interface thermal resistance will increase in direct proportion to the contact area. A thin chassis requires the addition of a backup plate.

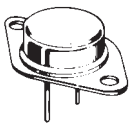
Figure 8. Press–Fit Package

to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger–tight the hardware should be torqued to its final specification in at least two sequential steps. A typical mounting installation for a popular flange type part is shown in Figure 10. Machine screws (preferred) self–tapping screws, eyelets, or rivets may be used to secure the package using guidelines in the previous section, “Fastener and Hardware Characteristics.”

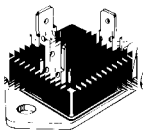
The copper flange of the Energy Management Series (EMS) Modules is very thick. Consequently, the parts are rugged and indestructible for all practical purposes. No special precautions are necessary when fastening these parts to a heatsink.

Some packages specify a tightening procedure. For example, with the Power Tap package, Figure 9b, final torque should be applied first to the center position.

The RF power modules (MHW series) are more sensitive to the flatness of the heatsink than other packages because a ceramic (BeO) substrate is attached to a relatively thin, fairly long, flange. The maximum allowable flange bending to avoid mechanical damage has been determined and presented in detail in EB107 “Mounting Considerations for Motorola RF Power Modules.” Many of the parts can handle a combined heatsink and flange deviation from flat of 7 to 8 mils which is commonly available. Others must be held to 1.5 mils, which requires that the heatsink have nearly perfect flatness.

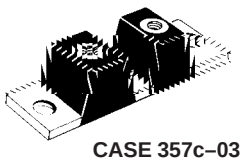


CASE 1, 11
TO–204AA
(TO–3)



CASE 383–01

9a. TO–3 Variations



CASE 357c–03

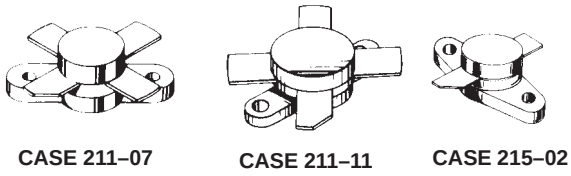
9b. Plastic Power Tap

CASE 373–01 CASE 807–03 CASE 807A–03 CASE 808–01

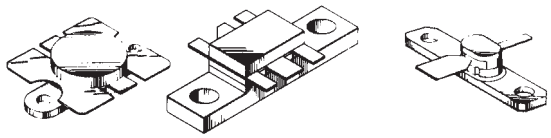
CASE 809–02 CASE 812–02 CASE 813–02

CASE 814–02 CASE 816–02 CASE 819–02

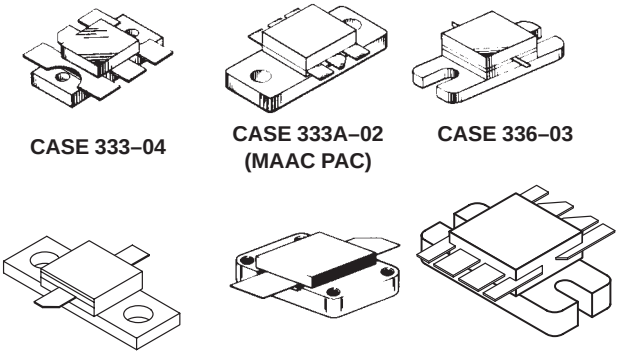
9c. Energy Management Series
(Isolated Base Plate)



CASE 211–07 CASE 211–11 CASE 215–02



CASE 316–01 CASE 319–07
(CS–12) CASE 328A–03



CASE 333–04 CASE 333A–02
(MAAC PAC) CASE 336–03

CASE 337–02 CASE 368–03
(HOG PAC) CASE 744A–01

9d. RF Stripline Isolated Output Opposed Emitter
(SOE) Series

Figure 9. A Large Array of Parts Fit into the Flange–Mount Classification

Specific mounting recommendations are critical to RF devices in isolated packages because of the internal ceramic substrate. The large area Case 368–03 (HOG PAC) will be used to illustrate problem areas. It is more sensitive to proper mounting techniques than most other RF power devices.

Although the data sheets contain information on recommended mounting procedures, experience indicates that they are often ignored. For example, the recommended maximum torque on the 4–40 mounting screws is 5 in/lbs. Spring and flat washers are recommended. Over torquing is a common problem. In some parts returned for failure analysis, indentions up to 10 mils deep in the mounting screw areas have been observed.

Calculations indicate that the length of the flange increases in excess of two mils with a temperature change of 75°C. In such cases, if the mounting screw torque is excessive, the flange is prevented from expanding in length, instead it bends upwards in the mid–section, cracking the BeO and the die. A similar result can also occur during the initial mounting of the device if an excessive amount of thermal compound is applied. With sufficient torque, the thermal compound will squeeze out of the mounting hole areas, but will remain under the center of the flange, deforming it. Deformations of 2 – 3 mils have been measured between the center and the ends under such conditions (enough to crack internal ceramic).

Another problem arises because the thickness of the flange changes with temperature. For the 75°C temperature excursion mentioned, the increased amount is around 0.25 mils which results in further tightening of the mounting screws, thus increasing the effective torque from the initial value. With a decrease in temperature, the opposite effect occurs. Therefore thermal cycling not only causes risk of structural damage but often causes the assembly to loosen which raises the interface resistance. Use of compression hardware can eliminate this problem.

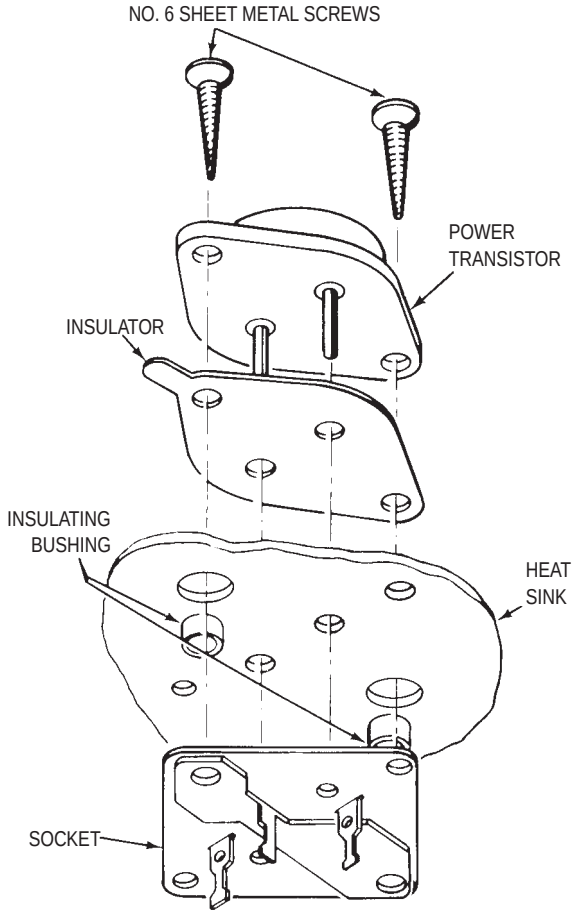


Figure 10. Hardware Used for a TO–204AA (TO–3) Flange Mount Part

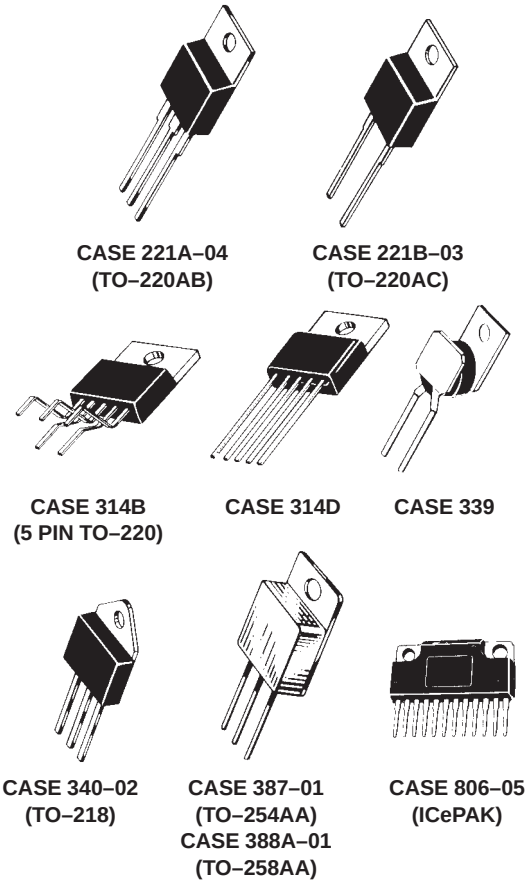


Figure 11. Several Types of Tab–Mount Parts

Tab Mount

The tab mount class is composed of a wide array of packages as illustrated in Figure 11. Mounting considerations for all varieties are similar to that for the popular TO–220 package, whose suggested mounting arrangements and hardware are shown in Figure 12. The rectangular washer shown in Figure 12a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6–32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch–pounds is suggested when using a 6–32 screw.

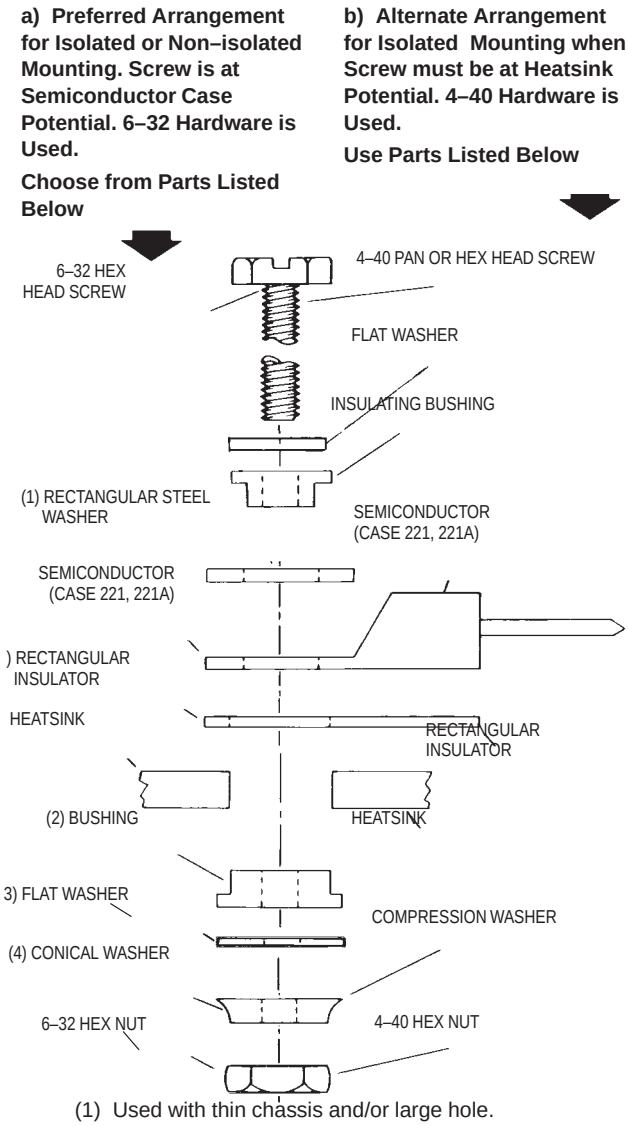
Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, Motorola TO–220 packages have a chamfer on one end. TO–220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

The popular TO–220 Package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure B1.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab.(6) In addition, it separates the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 15c. To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

The ICePAK (Case 806–05) is basically an elongated TO–220 package with isolated chips. The mounting precautions for the TO–220 consequently apply. In addition, since two mounting screws are required, the alternate tightening procedure described for the flange mount package should be used.

In situations where a tab mount package is making direct contact with the heatsink, an eyelet may be used, provided sharp blows or impact shock is avoided.

(6) Catalog, Edition 18, Richco Plastic Company, 5825 N. Tripp Ave., Chicago, IL 60546.



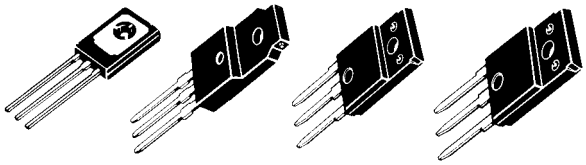
(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing is used.

Figure 12. Mounting Arrangements for Tab Mount TO–220

Plastic Body Mount

The Thermopad and isolated plastic power packages shown in Figure 13 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance. For the Thermopad (Case 77) parts this is accomplished by die–bonding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface. The copper sheet has a hole for mounting; plastic is molded enveloping the chip but leaving the mounting hole open. The low thermal resistance of this construction is obtained at the expense of a requirement that strict attention be paid to the mounting procedure.

The isolated (Case 221C–02) is similar to a TO–220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO–220 and is similar to that of the Thermopad.



CASE 77 TO–225AA/ TO–126 (THERMOPAD) | **CASE 221C–02 (FULLY ISOLATED)** | **CASE 221D–02 (FULLY ISOLATED)** | **CASE 340B–03 (FULLY ISOLATED)**

Figure 13. Plastic Body–Mount Packages

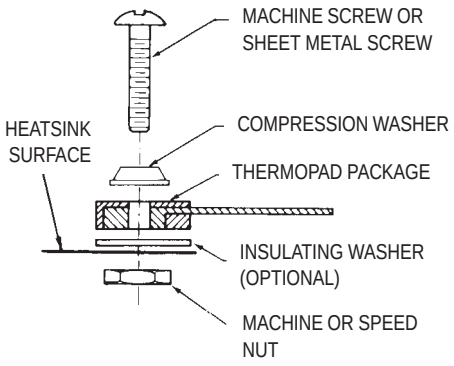
Several types of fasteners may be used to secure these packages; machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air–driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 5.

Figure 14 shows details of mounting Case 77 devices. Clip mounting is fast and requires minimum hardware, however, the clip must be properly chosen to insure that the proper mounting force is applied. When electrical isolation is required with screw mounting, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.

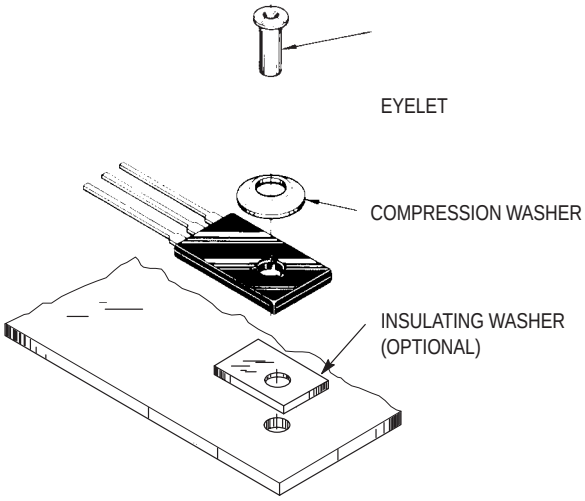
The isolated, (Case 221C, 221D and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO–220. As shown in Figure 15c, one properly chosen clip, inserted into two slotted holes in the heatsink, is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure B1 of Appendix B.) The interface should consist of a layer of thermal grease or a highly conductive thermal pad. Of course, screw mounting shown in Figure 15b may also be used but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO–220 package which is shown in Figure 15a.

Surface Mount

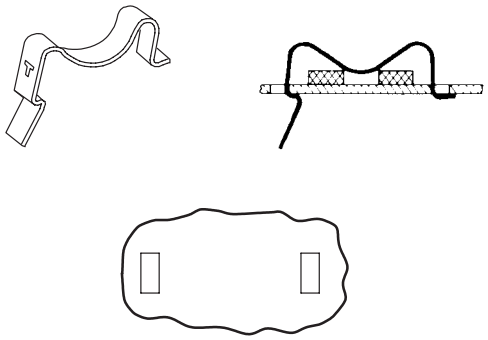
Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 16, for example, will accommodate a die up to 112 mils x 112 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resistance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.



14a. Machine Screw Mounting

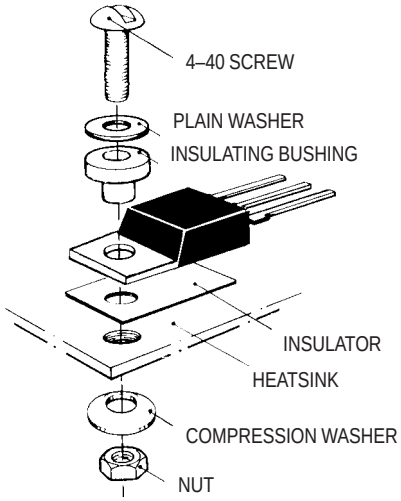


14b. Eyelet Mounting

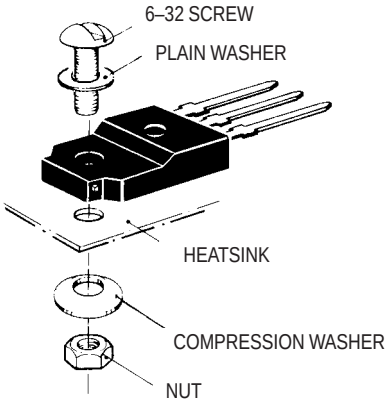


14c. Clips

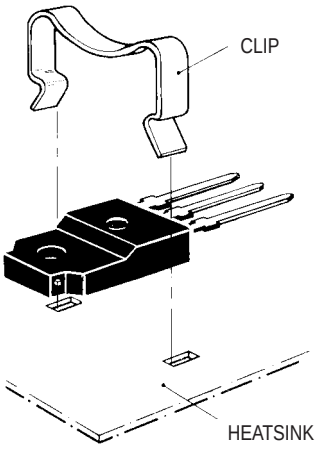
Figure 14. Recommended Mounting Arrangements forTO–225AA (TO–126) Thermopad Packages



15a. Screw–Mounted TO–220



15b. Screw–Mounted Isolated Package



15c. Clip–Mounted Isolated Package

Figure 15. Mounting Arrangements for the Isolated Package as Compared to a Conventional TO–220

CASE 369–07 CASE 369A–13

Figure 16. Surface Mount D–PAK Parts

Standard Glass–Epoxy 2–ounce boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 17 shows, thermal resistance assymtotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

Boards are offered that have thick aluminum or copper substrates. A dielectric coating designed for low thermal resistance is overlaid with one or two ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type.(7) The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

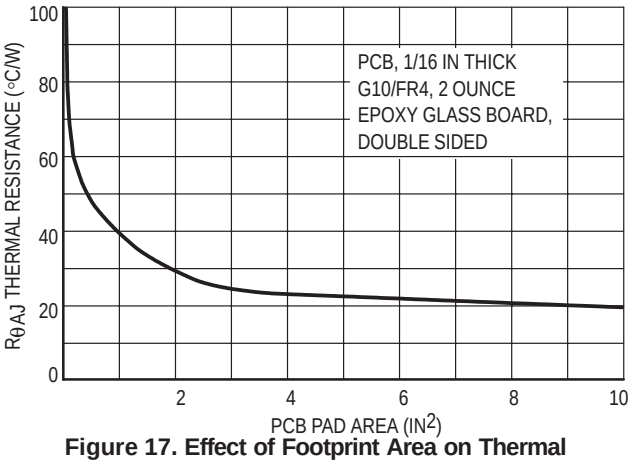
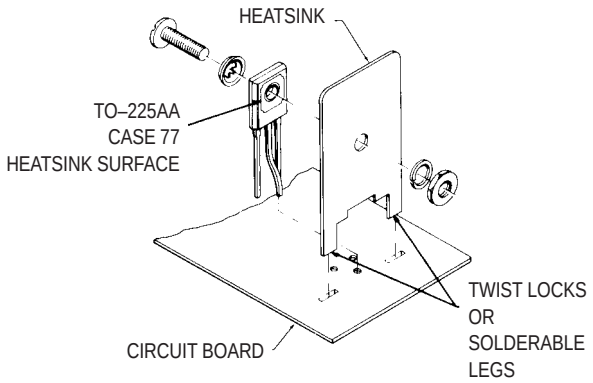


Figure 17. Effect of Footprint Area on Thermal Resistance of DPAK Mounted on a Glass–Epoxy Board

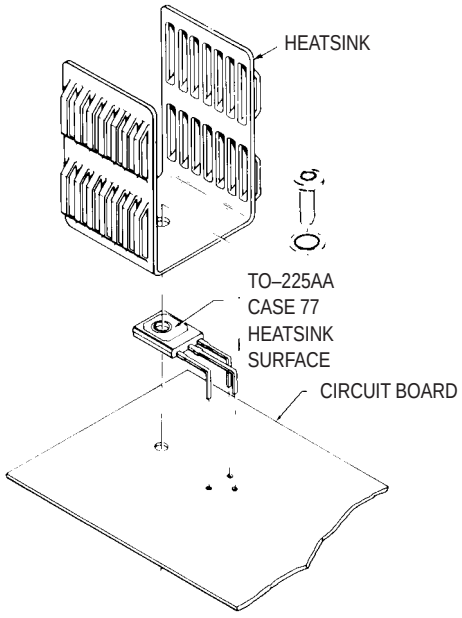
FREE AIR AND SOCKET MOUNTING

In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice however, it is better to support the package. A plastic support for the TO–220 Package and other similar types is offered by heatsink accessory vendors.

In many situations, because its leads are fairly heavy, the CASE 77 (TO–225AA) (TO–127) package has supported a small heatsink; however, no definitive data is available. When using a small heatsink, it is good practice to have the sink rigidly mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 18. The arrangement of part (a) could be used with any plastic package, but the scheme of part (18b) is more practical with Case 77 Thermopad devices. With the other package types, mounting the transistor on top of the heatsink is more practical.



18a. Simple Plate, Vertically Mounted



18b. Commercial Sink, Horizontally Mounted

Figure 18. Methods of Using Small Heatsinks With Plastic Semiconductor Packages

(7) Herb Fick, “Thermal Management of Surface Mount Power Devices,” Powerconversion and Intelligent Motion, August 1987.

In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from Motorola. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

CONNECTING AND HANDLING TERMINALS

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions as a result of thermal cycling over operating temperature extremes must be considered. Standard metal, plastic, and RF stripline packages each have some special considerations.

Metal Packages

The pins and lugs of metal packaged devices using glass to metal seals are not designed to handle any significant bending or stress. If abused, the seals could crack. Wires may be attached using sockets, crimp connectors or solder, provided the data sheet ratings are observed. When wires are attached directly to the pins, flexible or braided leads are recommended in order to provide strain relief.

EMS Modules

The screw terminals of the EMS modules look deceptively rugged. Since the flange base is mounted to a rigid heatsink, the connection to the terminals must allow some flexibility. A rigid buss bar should not be bolted to terminals. Lugs with braid are preferred.

Plastic Packages

The leads of the plastic packages are somewhat flexible and can be reshaped although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead–bending unnecessary. Numerous lead and tab–forming options are available from Motorola on large quantity orders. Preformed leads remove the users risk of device damage caused by bending.

If, however, lead–bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A leadbend radius greater than 1/16 inch is advisable for TO–225AA (CASE 77) and 1/32 inch for TO–220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead–to–plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire–wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case.

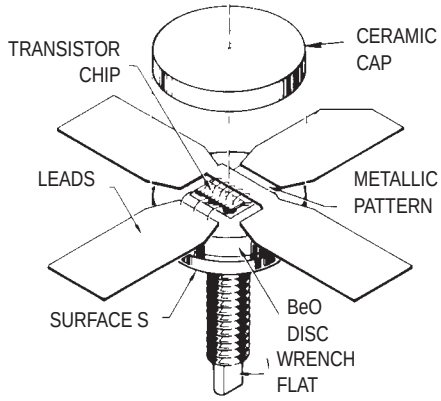
Stripline Packages

The leads of stripline packages normally are soldered into a board while the case is recessed to contact a heatsink as shown in Figure 19. The following rules should be observed:

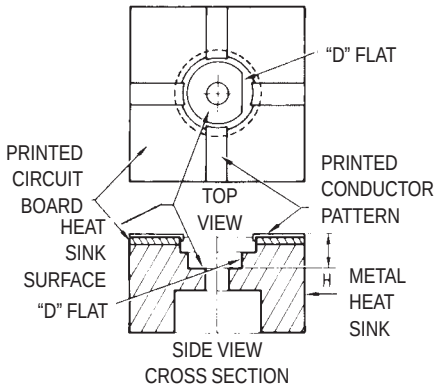
1. The device should never be mounted in such a manner as to place ceramic–to–metal joints in tension.
2. The device should never be mounted in such a manner as to apply force on the strip leads in a vertical direction towards the cap.
3. When the device is mounted in a printed circuit board with the copper stud and BeO portion of the header passing through a hole in the circuit boards, adequate clearance must be provided for the BeO to prevent shear forces from being applied to the leads
4. Some clearance must be allowed between the leads and the circuit board when the device is secured to the heatsink.
5. The device should be properly secured into the heatsinks before its leads are attached into the circuit.
6. The leads on stud type devices must not be used to prevent device rotation during stud torque application. A wrench flat is provided for this purpose.

Figure 19b shows a cross–section of a printed circuit board and heatsink assembly for mounting a stud type stripline device. H is the distance from the top surface of the printed circuit board to the D–flat heatsink surface. If H is less than the minimum distance from the bottom of the lead material to the mounting surface of the package, there is no possibility of tensile forces in the copper stud — BeO ceramic joint. If, however, H is greater than the package dimension, considerable force is applied to the cap to BeO joint and the BeO to stud joint. Two occurrences are possible at this point. The first is a cap joint failure when the structure is heated, as might occur during the lead–soldering operation; while the second is BeO to stud failure if the force generated is high enough. Lack of contact between the device and the heatsink surface will occur as the differences between H and the package dimension become larger, this may result in device failure as power is applied.

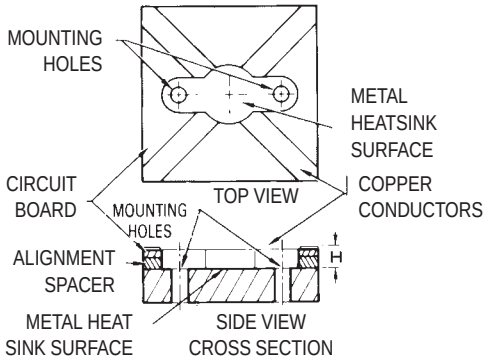
Figure 19c shows a typical mounting technique for flange–type stripline transistors. Again, H is defined as the distance from the top of the printed circuit board to the heatsink surface. If distance H is less than the minimum distance from the bottom of transistor lead to the bottom surface of the flange, tensile forces at the various joints in the package are avoided. However, if distance H exceeds the package dimension, problems similar to those discussed for the stud type devices can occur.



19a. Component Parts of a Stud Mount Stripline Package. Flange Mounted Packages are Similarly Constructed



19b. Typical Stud Type SOE Transistor Mounting Method



19c. Flange Type SOE Transistor Mounting Method

Figure 19. Mounting Details for SOE Transistors

CLEANING CIRCUIT BOARDS

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline and chlorinated Freon may cause the encapsulant to swell, possibly damaging the transistor die.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free–standing without support.

THERMAL SYSTEM EVALUATION

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see Motorola Application Note, AN569.

Other applications, notably RF power amplifiers or switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where T_J = junction temperature (°C)
T_C = case temperature (°C)
$R_{\theta JC}$ = thermal resistance junction–to case as specified on the data sheet (°C/W)
P_D = power dissipated in the device (W)

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the “test” position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

APPENDIX A
THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady–state conditions is generally written as:

$$q = hA\Delta T \quad (1)$$

where q = rate of heat transfer or power dissipation (P_D)
h = heat transfer coefficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance, R_θ, is

$$R_\theta = \Delta T/q = 1/hA \quad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm’s Law is often made to form models of heat flow. Note that T could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A1.

The equivalent electrical circuit may be analyzed by using Kirchoff’s Law and the following equation results:

$$T_J = P_D (R_{\theta JC} + P_{\theta CS} + R_{\theta SA}) + T_A \quad (3)$$

where T_J = junction temperature,
PD = power dissipation
$R_{\theta JC}$ = semiconductor thermal resistance (junction to case),
$R_{\theta CS}$ = interface thermal resistance (case to heat–sink),
$R_{\theta SA}$ = heat sink thermal resistance (heatsink to ambient),
T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance, $R_{\theta CS}$, may be significant compared to the other thermal resistance terms. A proper mounting procedure can minimize $R_{\theta CS}$.

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications such as in RF power amplifiers and short–pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.

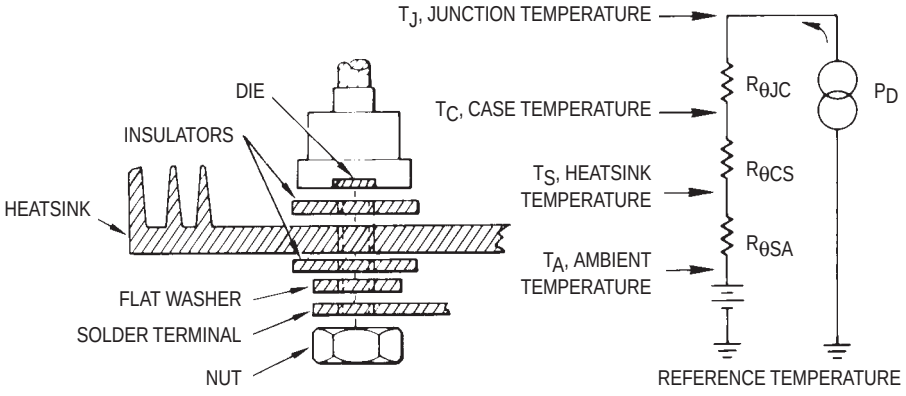


Figure A1. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor

APPENDIX B
MEASUREMENT OF INTERFACE THERMAL RESISTANCE

Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring DC power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO–3 package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL–I–49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is "application oriented."

Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The Motorola fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path.

As described previously, some packages, such as a TO–220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15 to 20% error in $R_{\theta CS}$ can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure the semiconductor case temperature. Consider the TO–220 package shown in Figure B1. The mounting pressure at one end causes the other end — where the die is located — to lift off the mounting surface slightly. To improve contact, Motorola TO–220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure. Three thermocouple locations are shown:

a. The Motorola location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

b. The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

c. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

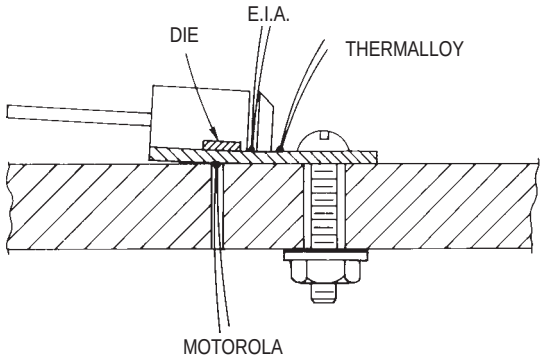


Figure B1. JEDEC TO–220 Package Mounted to Heatsink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the Motorola location is even hotter. Since junction–to–sink thermal resistance must be constant for a given test setup, the calculated junction–to–case thermal resistance values decrease and case–to–sink values increase as the "case" temperature thermocouple readings become warmer. Thus the choice of reference point for the "case" temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower but close to the temperature at the EIA location as the lateral heat flow is generally small. The Motorola location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The Motorola location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the

case and may yield results differing up to 1°C/W for a TO–220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified junction–to–case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heatsink. The washer is flat to within 1 mil/inch, has a finish better than 63 μ–inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application–oriented. It is also easy to use but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction–to–case thermal resistance while testing for interface thermal resistance. If the junction–to–case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

APPENDIX C
Sources of Accessories

Manufacturer	Joint Compound	Adhesives	Insulators						Heatsinks	Clips
			BeO	AlO_2	Anodize	Mica	Plastic Film	Silicone Rubber		
Aavid Eng.	—	—	—	—	—	—	X	X	X	X
AHAM–TOR	—	—	—	—	—	—	—	—	X	—
Asheville–Schoonmaker	—	—	—	—	—	X	—	—	—	—
Astrodynamis	X	—	—	—	—	—	—	—	X	—
Delbert Blinn	—	—	X	—	X	X	X	X	X	—
IERC	X	—	—	—	—	—	—	—	X	—
Staver	—	—	—	—	—	—	—	—	X	—
Thermalloy	X	X	X	X	X	X	X	X	X	X
Tran–tec	X	—	X	X	X	X	—	X	X	—
Wakefield Eng.	X	X	X	—	X	—	—	X	X	X

Other Sources for silicone rubber pads: Chomerics, Berquist

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Asheville–Schoonmaker, 900 Jefferson Ave., Newport News, VA 23607 (804) 244–7311

Astro Dynamics, Inc., 2 Gill St., Woburn, Massachusetts 01801 (617) 935–4944

Berquist, 5300 Edina Industrial Blvd., Minneapolis, Minnesota 55435 (612) 835–2322

Chomerics, Inc.,16 Flagstone Drive, Hudson, New Hampshire 03051 1–800–633–8800

Delbert Blinn Company, P.O. Box 2007, Pomona, California 91769 (714) 623–1257

International Electronic Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502 (213) 849–2481

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Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234 (214) 243–4321

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Wakefield Engineering, Inc., Wakefield, Massachusetts 01880 (617) 245–5900

PACKAGE INDEX

PREFACE

When the JEDEC registration system for package outlines started in 1957, numbers were assigned sequentially whenever manufacturers wished to establish a package as an industry standard. As minor variations developed from these industry standards, either a new, non–related number was issued by JEDEC or manufacturers would attempt to relate the part to an industry standard via some appended description.

In an attempt to ease confusion, JEDEC established the present system in late 1968 in which new packages are assigned into a category, based on their general physical appearance. Differences between specific packages in a category are denoted by suffix letters. The older package designations were re–registered to the new system as time permitted.

For example the venerable TO–3 has many variations. Can heights differ and it is available with 30, 40, 50, and 60 mil pins, with and without lugs. It is now classified in the TO–204 family. The TO–204AA conforms to the original outline for the TO–3 having 40 mil pins while the TO–204AE has 60 mil pins, for example.

The new numbers for the old parts really haven't caught on very well. It seems that the DO–4, DO–5 and TO–3 still convey sufficient meaning for general verbal communication.

Motorola Case Number	JEDEC Outline		Notes	Mounting Class
	Original System	Revised System		
001	TO-3	TO-204AA		Flange
003	TO-3		2	Flange
009	TO-61	TO-210AC		Stud
011	TO-3	TO-204AA	—	Flange
011A	TO-3	—	2	Flange
012	TO-3	—	2	Flange
036	TO-60	TO-210AB	—	Stud
042A	DO-5	DO-203AB	—	Stud
044	DO-4	DO-203AA	—	Stud
054	TO-3	—	2	Flange
056	DO-4	—	—	Stud
058	DO-5	—	2	Stud
61-04				Flange
63-02	TO-64	TO-208AB		Stud
63-03	TO-64	TO-2088AB		Stud
077	TO-126	TO-225AA	—	Plastic
080	TO-66	TO-213AA	—	Flange
086	—	TO-208	1	Stud
086L	—	TO-298	1	Stud
144B-05				Stud
145A-09				Stud
145A-10				Stud
145C	TO-232		1	Stud
157	—	DO-203	1	Stud
160-03	TO-59	TO-210AA	—	Stud
167	—	DO-203	1	Stud
174-04				Pressfit

Notes: 1. Would fit within this family outline if registered with JEDEC.
2. Not within all JEDEC dimensions.

Motorola Case Number	JEDEC Outline		Notes	Mounting Class
	Original System	Revised System		
175-03				Stud
197	—	TO-204AE	—	Flange
211-07				Flange
211-11				Flange
215-02				Flange
221	—	TO-220AB	—	Tab
221C-02				Plastic
221D-02	—	—	Isolated TO-220	Plastic
235	—	TO-208	1	Stud
235-03				Stud
238	—	TO-208	1	Stud
239	—	TO-208	—	Stud
244-04				Stud
245	DO-4	—	—	Stud
257-01	DO-5	—	—	Stud
263	—	TO-208	—	Stud
263-04				Stud
283	DO-4	—	—	Stud
289	—	TO-209	1	Stud
305-01				Stud
310-02				Pressfit
311-02			Isolated	Stud
311-02				Pressfit
311-02				Stud
314B-03				Tab

Motorola Case Number	JEDEC Outline		Notes	Mounting Class
	Original System	Revised System		
314D-03				Tab
316-01				Flange
319-06				Flange
328A-03				Flange
332-04				Stud
333-04				Flange
333A-02				Flange
336-03				Flange
337-02				Flange
340		TO-218AC		Tab
340A-02				Plastic
340B-03			Isolated TO-218	Plastic
342-01				Flange
357B-01				Flange
361-01				Flange
368-02				Flange
369-06		TO-251		Insertion
369A-12		TO-252		Surface
373-01			Isolated	Flange
383-01			Isolated	Flange
387-01		TO-254AA	Isolated 2	Tab
388A-01		TO-258AA	Isolated 2	Tab
744-02				Flange
744A-01				Flange
043-07	DO-21	DO-208AA		Pressfit

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