APPLICATION NOTES

APPLICATION NOTE SELECTION GUIDE

APPLICATION CATEGORY	APPLICATION NOTE NUMBER
DIGITAL	
MDTL	AN-235, AN-262A, AN-263, AN-283, AN-284, AN-408, AN-409, AN-487
MECL	AN-187, AN-194A, AN-202, AN-233, AN-239, AN-244, AN-257, AN-266, AN-274, AN-277, AN-278, AN-280, AN-417, AN-418, AN-456, AN-487, AN-488
MHTL	AN-298, AN-414, AN-467
MRTL	AN-234, AN-251, AN-252, AN-253, AN-254, AN-264, AN-279, AN-285, AN-286, AN-291, AN-296, AN-408, AN-424, AN-435, AN-451
MTTL	AN-446, AN-464, AN-465, AN-476, AN-488
Memory Circuits	AN-245A, AN-446, AN-464, AN-474
General	AN-270, AN-298

APPLICATION CATEGORY	APPLICATION NOTE NUMBER
LINEAR	
Operational Amplifiers	AN-204, AN-248, AN-258, AN-261, AN-273, AN-276, AN-400, AN-403, AN-405, AN-407, AN-411, AN-438, AN-439, AN-452, AN-459, AN-460
Sense Amplifiers and Differential Comparators	AN-245A
High-Frequency Circuits (Differential, Video, IF, and RF Amplifiers; Oscillators)	AN-203, AN-247, AN-259, AN-299, AN-404, AN-475
Low-Frequency Circuits	AN-401
Multipliers	AN489, AN-490
Regulators	AN-457, AN-473, AN-480
Consumer Linear Circuits	AN-420, AN-430, AN-432A, AN-434, AN-486
General	AN-166, AN-215, AN-223, AN-271, AN-297, AN-402, AN-421, AN-463, AN-471

APPLICATION NOTE ABSTRACTS

The application notes listed in this section have been prepared to acquaint the circuits and systems engineer with the broad line of Motorola integrated circuits and their applications. Application notes with a star (*) before the AN number are printed in this section of the DATA BOOK. To obtain copies of the notes which are not printed in this book, simply list the AN number or numbers and send your request on your company letterhead to: Technical Information Center, Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, Arizona 85036.

AN-166 Using Linvill Techniques for RF Amplifiers

A design procedure, derived from theory developed by J. G. Linvill, simplifies the design of single stage small-signal RF amplifiers. A 200 MHz amplifier serves as an example of the technique.

AN-187 MECL Integrated Circuit Line Driver

Specially designed for high fan-out capabilities, this integrated circuit line driver can supply a signal to 150 logic gates without deterioration.

AN-194A Designing Integrated Serial Counters

MECL monolithic integrated J-K flip-flops serve as building blocks for ultra-high-speed ripple counters. General design techniques for designing counters of any arbitrary count.

AN-202 Noise Margins of MECL Integrated Circuits

A knowledge of ground line and signal line dc and pulse noise margins is essential to the logic designers. Many curves illustrate the variations of input and ground line noise margins with temperature and fan-out.

AN-203 Tuned Amplifier Design with an Emitter-Coupled Integrated RF Amplifier

This note describes the design of a tuned amplifier utilizing the MC1110 integrated circuit as a basic building block. DC considerations, characterization in terms of y-parameters, and amplifier design using Linvill's method are discussed.

AN-204 High Performance Integrated Operational Amplifiers

Two new high performance monolithic operational amplifiers feature exceptionally high input impedance and high open loop gain. This note describes

***AN-215 RF Small Signal Design Using Admittance Parameters**

The author shows that the power gain and stability of high frequency transistors may be completely described by two-port parameters.

This paper presents a summary of the overall design solution for the small signal RF amplifier using admittance parameters. Design considerations and relationships for both stable and the potentially unstable transistor are presented together with a discussion of the neutralized, unneutralized, matched, and mis-matched amplifiers.

AN-223 Cascade Noise Figure for Integrated Circuit Transistors

In vacuum tube circuitry, the combination of the grounded-cathode and the grounded-grid cascade has superior noise properties to all other two-stage amplifiers. In transistor circuitry the noise performance of a single-stage amplifier is well known, but little information has been published about the best performance obtainable from two-stage transistor amplifiers. This paper evaluates the noise performance of all possible two-stage transistor amplifiers. Also, since the noise contribution of stages beyond the second is normally small, this analysis will be valid for amplifiers with any number of stages.

AN-233 Design of Monostable Multivibrators Using MECL Integrated Circuits

This application note describes an integrated monostable multivibrator composed of a MECL R-S or J-K flip-flop plus a few discrete components. A main feature of the multivibrators is their complete compatibility with the MECL family of current mode integrated circuits. These multivibrators can provide a timed output ranging from 60 ns to the millisecond range. The note discusses special circuits which have

even faster recovery times. Pulsed recovery (recovery during any point during the delay time) is possible with both types of multivibrators.

AN-234 MRTL Family of Integrated Circuits

The purpose of this note is to familiarize the logic designer with the Motorola Resistor Transistor Logic (MRTL) family. Logic diagrams, pin layouts, and loading data are given for each device. Three illustrative applications of MRTL; an asynchronous 4-bit comparator, an asynchronous 5-bit adder, and a shift register, serve as design examples. This family is noted for its economy and variety of logical elements.

AN-235 Using the Motorola MDTL Line of Integrated Circuits

The MDTL line of integrated circuits is briefly characterized with important capabilities of the MDTL series, such as noise immunity, discussed. MDTL applications are presented, including shift registers, ripple counters, clocked counters, and decade shift counters.

AN-239 MECL Integrated Circuit Schmitt Triggers

The Schmitt Trigger, a regenerative circuit which changes state abruptly when the input signal crosses specified dc trigger levels, can be fabricated from MECL integrated logic gates. This note describes the modifications necessary to convert standard MECL logic gates to Schmitt Triggers, and also the performance to be expected from such units. Examples of the MECL Schmitt Trigger used for wave shaping and pulse generator applications are also included.

AN-244 The MECL Line of Digital Integrated Circuits

This note familiarizes the digital integrated circuit user with Motorola MECL integrated circuits; pin layouts, and logical diagrams. Pertinent characteristics for each device in the MECL integrated circuit line are given. The note includes applications of various circuits illustrating the versatility of the MECL family. High speed operation, high input impedance, high fan-out, and very low internally generated noise characterize the line of integrated circuits.

★AN-245A An Integrated Core Memory Sense Amplifier

This application note discusses core memories and related design considerations for a sense amplifier. Performance and environmental specifications for the amplifier design are carefully established so that the circuit will work with any computer using core memories. The final circuit design is then analyzed and measured performance is discussed. The amplifier features a small uncertainty region (6 mV max), adjustable voltage gain, and fast cycle time (0.5 μs).

AN-247 An Integrated Circuit RF-IF Amplifier

A new, versatile integrated circuit for RF-IF applications is introduced which offers high gain, extremely low internal feedback and wide AGC range. The circuit is a common-emitter, common-base pair (the cascade connection) with an AGC transistor and associated biasing circuitry. The amplifier is built on a very small die and is economically comparable to a single transistor, yet it offers performance advantages unobtainable with a single device. This application note describes the AC and DC operation of the circuit, a discussion of Y-parameters for calculating optimum power and voltage gain, and a variety of applications as an IF single-tuned amplifier, IF stagger-tuned amplifier, oscillator, video-audio amplifier and modulator. A discussion of noise figure is also included.

AN-248 A High Voltage Monolithic Operational Amplifier

This note introduces a high voltage monolithic operational amplifier featuring high open loop gain, large common mode input signal, and low drift. The function of each stage in the circuit is analyzed, and methods for frequency compensating the amplifier are discussed. DC biasing parameters are also examined. Four applications using the amplifier are discussed: a source follower, a twin tee filter and oscillator, a voltage regulator, and a high input impedance voltmeter.

AN-251 Decade Counters Using MRTL Integrated Circuits

This application note discusses the design and implementation of decade counters using the MRTL family of integrated logic. Ripple counters, shift counters, and parallel clocked counters are developed using BCD, 2'421, and excess 3 digital codes. Up and down counting techniques are discussed. Output decoding, problem areas and circuit limitations are covered for all counter types.

AN-252 Choosing MRTL Integrated Logic Circuits

This article discusses resistor-transistor logic, MRTL, integrated circuits, and the considerations a user should make prior to using this integrated circuit family. Full consideration is given to the advantages as well as the limitations one encounters with this logic form. The discussion is general in nature and applies to all popular versions of resistor-transistor logic.

AN-253 An Analysis of MRTL Integrated Logic Circuits

Special emphasis is given to noise margin specifications, large circuit fan-out, operating speeds, and interfacing with saturated logic in this analysis of Motorola MRTL integrated logic circuits. The J-K

flip-flop circuit is reviewed and basic counting and shifting circuits are presented to illustrate typical J-K applications.

AN-254 Using MRTL Integrated Circuit Flip-Flops

Circuit operation of MRTL J-K flip-flops is explained fully. The R-S flip-flop is also briefly discussed. Pulse input requirements and loading considerations are discussed and some applications of the J-K flip-flop shown in the form of minimum-logic small-count counters.

AN-257 Decade Counters Using MECL J-K Flip-Flops

This note discusses the use of MECL integrated circuits in four types of decade counters. The logic and circuit design of an excess three up-down counter, a 2'421 up-down counter, a Gray code counter, and a switch-tail ring counter with ten line output are illustrated.

AN-258 Monostable Multivibrator Design Using An Integrated Circuit Operational Amplifier

This application note discusses the use of integrated operational amplifiers connected as monostable multivibrators. The classical monostable circuit including some limitations with respect to the conventional component and integrated device designs are briefly reviewed. The basic circuit theory and qualifications of the operational amplifier connected as a monostable device are then discussed and the timing equation derived. Alternate monostable configurations and their ultimate design limitations are briefly reviewed with respect to utilization of the MC1430/1530 and MC1431/1531 family of devices. Finally a design example is used to illustrate the principles and limitations outlined.

AN-259 Using Integrated Circuits in a Stagger Tuned IF Strip

Integrated Circuits are quickly becoming "the way to go" in the electronic industry, and justifiably so. Their small size and high reliability, coupled with low cost make them an ideal component for radio, television, communication gear, computers, and an infinite number of other uses. This application note describes the use of an Integrated Circuit High Frequency Amplifier, the MC1550, in a stagger tuned I-F strip. The design frequency is 45 MHz; however, the procedure is similar for designs covering its full range of operation (DC to 300 MHz).

★AN-261 Transistor Logarithmic Conversion Using an Operational Amplifier

The design of a log amplifier using a common base transistor configuration as the feedback element of an integrated circuit operational amplifier circuit is discussed in this application note. Six decades of logarithmic conversion are obtained with less than 1% error of output voltage. The possible causes of error are discussed followed by two applications: direct multiplication of two numbers, and solution of the equation $Z = X^n$.

AN-262A Decade Counters Using MDTL Integrated Circuits

Decade counting is a basic digital operation and may be performed by a wide variety of counting circuits. This note illustrates how some of the commonly used $\div 10$ counting techniques can be accomplished with Motorola Diode-Transistor Logic (MDTL) integrated circuits. Ripple, clocked, and shift decade counters using a variety of coding methods are discussed.

AN-263 Choosing DTL Integrated Logic Circuits

This article discusses diode-transistor logic, DTL, integrated circuits, and the considerations a user should make in choosing this integrated circuit family. Consideration is given to the advantages and limitations one encounters with this logic form. Three versions of DTL are considered in this report; conventional DTL, modified DTL, and high noise immunity DTL.

AN-264 MRTL Integrated Circuit Shift Registers

This note discusses the design considerations for the implementation of a 16-bit shift register using J-K flip-flops. The shift register described has the capability, upon command, to shift left or shift right and to enter information serially or in parallel. All problems encountered in the implementation and operation of the register are discussed.

AN-266 MECL Integrated Circuit Flip-Flops

Current Mode bi-stable elements are discussed along with pertinent characteristics and specifications. The R-S, J-K, and Master-Slave types of flip-flops are evaluated according to performance. Methods of reducing overshoot when driving a large number of flip-flops and flip-flop fan-in, fan-out capabilities are also given.

AN-270 Nanosecond Pulse Handling Techniques

The rapid advancement in the field of high speed digital integrated circuits has brought into focus many problem areas in the methods of pulse measurement techniques and new concepts dealing with these problems. This paper is intended to discuss the more common, yet perhaps not well known, pitfalls of measurement systems, a method of detecting them and possible solutions.

AN-271 Breadboard Techniques For Low Frequency Integrated Circuit Feedback Amplifiers

Certain considerations, unnecessary for discrete devices, are of critical importance in the breadboarding of integrated circuit systems. This paper provides the engineer or technician with some wiring tips and important precautions for integrated circuit breadboarding.

AN-273 More Value out of Integrated Operational Amplifier Data Sheets

The operational amplifier is rapidly becoming a basic building block in present day solid state electronic systems. The purpose of this application note is to provide a better understanding of the open loop characteristics of the amplifier and their significance to overall circuit operation. Also, each parameter is defined and reviewed with respect to closed loop considerations. The importance of loop gain stability and bandwidth is discussed at length. Input offset circuits are also reviewed with respect to closed loop operation.

AN-274 MECL Integrated Circuit Shift Registers

A generic shift-right, shift-left register with parallel entry, end-around-shift, and complementation capabilities is discussed. Maximum practical operating speed, delay times and timing considerations of the logic gating signals are determined. The basic register as developed may be used for data handling, for number scaling, or in the arithmetic portion of a digital computer.

AN-276 Useful Frequency Range Extension for MC1530 Operational Amplifiers

This application note explains various frequency compensating techniques designed to extend operating frequency of the MC1530. In addition circuit configurations and frequency response curves are shown for various compensation techniques. Examination shows this amplifier can be used at frequencies up to 14 MHz.

AN-277 Overshoot and Ringing in High-Speed Digital Systems

The amount of overshoot and ringing that may be expected in a system is determined as a function of driving source impedance, rise-time, wiring length, and loading. Determination of allowed overshoot and methods of reducing overshoot are discussed for conventional point to point wiring methods. Capacitive loading effects of MECL devices and circuit hardware are also discussed.

AN-278 Using Shift Registers as Pulse Delay Networks

This note discusses high speed clocked shift registers using J-K flip-flops and employed as a digital incremental delay. The register may be clocked with a frequency division counter to accomplish any desired delay with increments as small as 20 ns. The circuit as developed may be used for timing basic computer decisions or as an adjustable delay line for pulse.

AN-279 Setup and Release Times in the MRTL J-K Flip-Flop

This application note discusses the setup and release times for J-K flip-flops. The method used to measure setup and release time is discussed. A few simple decade counters are analyzed for worst case release times.

AN-280 MECL 85 MHz J-K Flip-Flop

A new high-speed J-K flip-flop is discussed. Capabilities, performance, and applications are explained along with typical and worst case operating data. This flip-flop with four J inputs and four K inputs more than doubles the operating speed of registers and counters as employed in a system.

AN-283 Using MDTL IC Flip-Flops

To properly implement a logic system with integrated circuits, it is important that the logic designer be familiar with the devices he uses. One of the more complex of integrated circuits is the clocked flip-flop. The purpose of this report is to acquaint the reader with the operation of the MDTL flip-flop, to discuss the different modes of operation, and to show some typical uses for this flip-flop.

*AN-284 MDTL IC Shift Registers

This report shows some frequently encountered shift register designs implemented with MDTL logic devices. Various operating characteristics are discussed as well as some of the important design considerations.

AN-285 Loading Factors and Paralleling Rules for MRTL Integrated Circuits

The need for loading factors in Motorola Resistor Transistor Logic (MRTL) is discussed and proper usage is illustrated. Modification of loading factors is covered for the case when circuit outputs are paralleled. Illustrations are provided by using the MC700P Series of integrated circuits.

AN-286 Binary Addition Using MRTL IC's

This note discusses the principles of binary addition with positive numbers and considers the implementation of binary adders with MRTL. The full adder function is illustrated using MRTL half adders, NOR gates arranged to simulate half adders, and with NOR gates in a two level logic scheme.

The full adder and associated logic is developed for a four-bit parallel (asynchronous) adder and for serial (synchronous) adder.

AN-291 External Direct Setting of MRTL Dual J-K Flip-Flops

A method is described to obtain full functional capability from MRTL dual flip-flops by connecting external circuitry to the proper terminals. Applications are provided that illustrate a reduction in package count by using this configuration as compared to the employment of single unit, full capability flip-flop circuits.

AN-296 Construction of A Master-Slave Flip-Flop from MRTL Gates

Information is provided on the construction of a master-slave flip-flop circuit from standard MRTL gates. Characteristics of the resulting circuit are given and an application of the configuration illustrates the advantage of this type of flip-flop.

AN-297 Integrated Circuits for High Frequency to Voltage Conversion

This application note concerns the technique of using integrated circuits in a linear frequency to voltage converter from 1 MHz to 30 MHz. A theoretical analysis is given as well as a working design.

*AN-298 Noise Immunity With High Threshold Logic

A comparison of noise immunity characteristics is made between MHTL devices and standard saturated logic devices.

AN-299 An IC Wideband Video Amplifier With AGC

This application describes the use of the MC1550 as a wideband video amplifier with AGC. The analysis of a single stage amplifier with 28 dB of gain and 22 MHz bandwidth is given with the results extended to a 78 dB video amplifier with 10 MHz bandwidth.

AN-400 An Operational Amplifier Tester

A simple and inexpensive tester for Motorola's line of operational amplifiers is described which will measure the open loop voltage gain, the equivalent input offset voltage, the maximum positive and negative output voltage swing, and a view of the transfer function which shows the linearity of the device.

Included is an elementary discussion of the parameters measured and their relationship to closed loop performance.

AN-401 The MC1554 One-Watt Monolithic Integrated Circuit Power Amplifier

This application note discusses four different applications for the MC1554, along with a circuit description including dc characteristics, frequency response, and distortion. A section of the note is also devoted to package power dissipation calculations including the use of the curves on the power amplifier data sheet.

AN-402 Insulated Gate FET's Used in IC's

The note acquaints the circuit designer with the integrated FET. A brief description of the operation of the Insulated-Gate Field Effect transistor is presented. This discussion is followed by a description of the FET in integrated form and finally, the basic advantages of FET IC's are explored.

*AN-403 Single Power Supply Operation of IC Op Amps

A split zener biasing technique that permits use of the MC1530/1531, MC1533, and MC1709 operational amplifiers and their restricted temperature counterparts MC1430/1431, MC1433 and MC1709C from a single power supply voltage is discussed in detail. General circuit considerations as well as specific ac and dc device considerations are outlined to minimize operating and design problems.

*AN-404 A Wideband Monolithic Video Amplifier

This note describes the basic principles of ac and dc operation of the MC1552G and MC1553G, characteristics obtained as a function of the device operating modes, and typical circuit applications.

AN-405 DC Comparator Operations Utilizing Monolithic IC Amplifiers

The use of the MC1533 operational amplifier and the MC1710 differential comparator are discussed. The capabilities and performance are given along with typical operating curves for both devices.

AN-407 A General Purpose IC Differential Output Operational Amplifier

This application note discusses four different applications for the MC1520 and a complete description of the device itself. The final sections of the note discuss such topics as operation from single and split power supplies, frequency compensation, and various feedback schemes.

AN-408 Problems and Solutions With MDTL and MRTL

Problems which may be encountered in using MRTL or MDTL integrated circuits in low or medium speed systems are examined in this report. Methods of shaping clock waveforms, restrictions on input and output terminals when interfacing with discrete components, and techniques for extending temperature range are discussed.

AN-409 MDTL Multivibrator Circuits

This note describes methods of using MDTL gates to form astable and monostable multivibrators. The operation of the MC951/MC851 monostable multivibrator is also covered as well as a simple pulse-shaping circuit.

AN-411 The MC1535 Monolithic Dual Op Amp

This note discusses two dual operational amplifier applications and an input compensation scheme for fast slew rate for the MC1535. A complete ac and dc circuit analysis is presented in addition to many of the pertinent electrical characteristics and how they might affect the system performance.

AN-414 Operation and Application of MHTL I/C Flip-Flops

A master-slave R-S and a dual J-K are the initial flip-flop elements available in the Motorola High Threshold Logic (MHTL) family. This note describes operation and characteristics of each unit and illustrates several applications of these devices.

AN-417 IC Crystal Controlled Oscillators

Crystal controlled square wave oscillators can be used as clock drivers, harmonic sources for frequency markers, in frequency synthesizers, frequency comparators, etc. It is difficult to obtain high frequency square waves due to the long propagation delays of the most integrated circuits. The MECL II clock driver with 2 ns propagation delay eliminates this problem. This note describes square wave oscillator circuits with crystal control that are capable of output frequencies, inverted and non-inverted, up to 150 MHz.

AN-418 High Speed Monostable Multivibrator Design with MECL Integrated Circuits

This note describes two configurations of monostable multivibrators using the MC1023 clock driver and a delay element. Operating frequencies in excess of 70 MHz and pulse widths of 4 nanoseconds are possible. Methods of obtaining the predetermined delay are also discussed.

AN-420 An Integrated Circuit Stereo Preamplifier

This note describes the use of the MC1303P dual preamplifier integrated circuit in a high quality stereo preamplifier circuit. It shows the designer how to adapt or modify the circuit to meet particular needs. The resultant preamplifier is suitable for use in systems having the most critical requirements.

AN-421 Semiconductor Noise Figure Considerations

A summary of many of the important noise figure considerations related with the design of low noise amplifiers is presented. The basic fundamentals involving noise, noise figure, and noise figure-frequency characteristics are then discussed with the emphasis on characteristics common to all semiconductors. A brief introduction is made to various methods of data sheet presentation of noise figure and a summary is given for the various methods of measurement. A discussion of low noise circuit design, utilizing many of the previously discussed considerations, is included.

AN-424 Designing a Digital Organ Tone Generator

A digital organ tone generator is described here to familiarize the reader with the capabilities of Motorola in-stock integrated circuits in novel electronic organ designs. An organ using this kind of tone generator has several advantages over the conventional 12-master oscillator divider organ.

AN-430 An Integrated-Circuit Chroma Demodulator for Solid-State Color Television Receivers

This note describes an integrated-circuit chroma demodulator for solid-state television receivers, using the Motorola XC-1325P. The demodulator requires only the chroma signal and two reference phases from the 3.58 MHz color oscillator for providing low-impedance color difference signals to drive the chroma output stages directly.

*AN-432A A Monolithic Integrated FM Stereo Decoder System

This application note discusses the circuit approach that has been taken in the realization of the first monolithic integrated stereo multiplex decoder built for consumer usage, as well as some of the details concerning its incorporation in an FM stereo receiver.

AN-434 The Motorola Autobass and Percussion System

A new musical feature that could readily be incorporated in any electronic organ is described in this note. This feature provides an attractive selling point to beginner organists, as it substantially reduces the number of techniques they must learn to perform a satisfactory accompaniment. The implementation of the system with integrated circuits is straightforward and quite simple.

AN-435 The Electronic "Strobotuner", An Accurate Digital Musical Instrument Tuning Aid

This report presents the electrical design of an accurate digital tool for tuning musical instruments.

The concepts basic to the design and the principles of operation are discussed with a step-by-step procedure for using the tuner. A method of checking the accuracy after a tuning procedure is also included.

*AN-438 Analysis and Design of Active Filters Using Op Amps

Excellent filters for frequencies below 100 kHz can be economically realized with operational amplifiers. Increased Q, design flexibility, reduced weight and cost also add to the attractiveness of operational amplifier active filters. Rigorous design theory and practical circuit examples are given in this note.

★AN-439 MC1539 Op Amp and its Applications

This application note discusses the MC1539, a second generation operational amplifier. The general use and operation of the amplifier is discussed with special mention made of improved operation over that of its first generation predecessor–the 709 type amplifier.

In addition to the detailed discussion on the dc and ac operation of the device, considerable emphasis is placed on operational performance. Many applications are offered to demonstrate the device capability, including a high frequency feed-forward scheme, and a source follower application.

AN-446 128-Bit Read Only Memory

Read Only Memories can now be fabricated as integrated circuit arrays and hence will have a great impact upon digital system design. Applications of the Motorola 16-word, 8-bit Read Only Memory (ROM) are discussed. The applications are grouped into two classifications according to the type of memory addressing utilized – (1) Random Accessing (2) Sequential Addressing.

AN-451 A Frequency Counter Using Motorola RTL Integrated Circuits

A frequency-period counter with a total hardware cost under $200.00, based on unit quantity prices, is described. The instrument measures the periods and frequencies of periodic waveforms, ranging in frequency from 10 Hz to 20 MHz, and counts random occurances for selected gate times of one millisecond to 10 seconds. A four digit decimal readout is provided. The low cost is achieved by utilizing plastic MRTL devices in unique versions of a crystal controlled oscillator, a period selector, a one shot multivibrator, a pulse shaper, and a switch contact bounce eliminator circuit.

AN-452 An Op Amp RC Bandpass Filter

The design of audio range active filters using operational amplifiers and RC frequency elements is discussed. A computer program in BASIC is given for general design. The design example, a filter with a center frequency of about 1600 Hz and adjustable Q from 10–200, is provided.

★AN-456 A 50 MHz Programmable Counter Designed with MECL II Integrated Circuits

A high speed programmable counter using the MECL II family of logic is discussed. The counter is designed to accept an input frequency up to 50 MHz and divide it by any number from 2 to 999. This number is programmed into three decades of synchronous down counters. These decades with additional decoding and control logic comprise a complete high speed divide-by-N counter system.

AN-457 Switching Voltage Regulator Uses Discrete and Integrated-Circuit Approaches

A switching voltage regulator can be considerably more efficient than the conventional series-pass continuously conducting regulator. This note discusses the operation of switching regulators including design information. It also describes practical regulators using discrete and integrated-circuit driver circuits.

★AN-459 A Simple Technique for Extending Op Amp Power Bandwidth

The design of fast response amplifiers is presented without the use of "tricky" compensation procedures or calculations using data sheet information. Circuit analysis for compensation procedure is given.

★AN-460 Using Transient Response to Determine Operational Amplifier Stability

This application note describes a technique for evaluating the stability of any particular feedback amplifier configuration by analyzing its response to a step-function input. A theoretical analysis is given along with an example.

AN-463 An Integrated Circuit Phase-Locked Loop Digital Frequency Synthesizer

A digital frequency synthesizer design is detailed which incorporates digital channel selection and exhibits excellent frequency stability through the use of a phase-locked loop. The system design takes advantage of state of the art in both linear and digital monolithic integrated circuits, plus some ideas new to the synthesizer field.

AN-464 MTTL Designer's Note – The MC4004/MC4005, A 16-Bit Random Access Memory

High speed, non-destructive readout (NDRO) memory systems can be constructed with the MTTL 16-bit memory chip. Information concerning the chip that is pertinent to the design of a complete memory system is herein presented. The topics discussed are: (1) operation of the 16-bit memory including typical read and write sequences, (2) typical dc and switching characteristics as a function of temperature, power supply, and output load, and (3) examples of memory system organization utilizing the 16-bit memory as the basic cell.

AN-465 MTTL Designer's Note – The MC4006/MC4007 Decoders

Two MTTL complex functions, the MC4006 Binary to One-of-Eight Decoder and the MC4007 Dual Binary to One-of-Four Decoder are discussed. Their basic modes of operation and expansion capabilities are described. Examples of the use of the decoders in various systems are presented.

***AN-467 Using Motorola High Threshold Logic**

This application note explains operation of the Motorola High Threshold Logic (MHTL) family of integrated circuits. It briefly describes the members of the family and provides many of the characteristics of the units. Several examples are provided to aid the reader in the application of this unique logic family.

AN-471 Analog-To-Digital Conversion Techniques

The subject of analog-to-digital conversion and many of the techniques that can be used to accomplish it are discussed. The paper is written in general terms from a system point of view and is intended to assist the reader in determining which conversion technique is best suited for a given application.

***AN-473 A Monolithic High-Power Series Voltage Regulator**

This note discusses MC1560/MC1561 voltage regulator in terms of internal operation, development of these circuits, and how they are advantageously used in supply fabrication.

AN-474 The MC1541 – A Gated Dual-Channel Sense Amplifier for Core Memories

The MC1541 sense amplifier can provide many magnetic core memory systems with lower system cycle times and a lower package count than with previous sense amplifiers. Circuit operation, design considerations, interface problems and typical applications are discussed.

***AN-475 Using the MC1545 – A Monolithic, Gated-Video Amplifier**

Because of the unique design of the MC1545, this amplifier can be used as a gated video amplifier, sense amplifier, amplitude modulator, frequency shift keyer, balanced modulator, pulse amplifier, and many other applications. This note describes the ac and dc operation of the circuit and presents applications of the device as a video switch, amplitude modulator, balanced modulator, pulse amplifier, and others.

AN-476 MTTL Designer's Note – The MC4000 Data Selector and the MC4002 Data Distributor

Two MTTL complex functions, the MC4002 four and two-channel data distributor, and the MC4000 dual four-channel data selector are discussed. Their basic modes of operation and expansion capabilities are described. Examples of the use of the data distributor and the data selector in various systems are presented.

***AN-480 Regulators Using Operational Amplifiers**

The theory of op amp voltage regulator design is discussed. The problem areas associated with such designs are also detailed. The MC1560 is used as a OTC voltage reference in the op amp regulator designs that are shown. It is shown that regulation from 0.01% to 0.001% is possible.

AN-486 A Monolithic Circuit for Television Sound Systems

This application note describes the MC1351P monolithic integrated circuit designed for television sound systems. The circuit consists of a limiting 4.5 MHz IF amplifier and a full wave quadrature detector; in addition, it has an audio preamplifier and an audio driver on the same chip, capable of delivering 3 Vrms to the audio output stage.

AN-487 A High-Speed Ripple-Through Arithmetic Processor

A simple, systematic building block approach for designing a high-speed, ripple-through arithmetic processor is described. Using only gates and full adders, ultra-high speed multiplication, division, square root extraction, addition, and subtraction may be performed. Several variations of an arithmetic processor design are detailed and comparisons of speed and package count using the MECL and MDTL logic in 14-pin, 16-pin, 24-pin, 32-pin, and 64-pin packages are given.

AN-488 High-Speed Addition Using Lookahead Carry Techniques

The use of the lookahead carry principle to increase the operating speed of adder systems is described. Several adders of different sizes using variations of lookahead carry are developed and the logical implementation of these using the MTTL III and MECL II and III logic families is given.

***AN-489 Analysis and Basic Operation of the MC1595**

The MC1595 monolithic linear four-quadrant multiplier is discussed. The equations for the analysis are given along with performance that is characteristic of the device. A few basic applications are given to assist the designer in system design.

***AN-490 Using the MC1595 Multiplier in Arithmetic Operations**

This application note discusses the use of the MC1595 linear four quadrant multiplier in arithmetic operations. Included is a discussion of the MC1595 used in the multiply, divide, square and square root modes of operation. Actual circuits for these functions are shown with measured data and a discussion of the errors occurring in each mode.

★AN-492 Operating Characteristics of the MC3000/ MC3100 Series Transistor-Transistor Logic Gates

This application note explains the advantages of using the MC3000/MC3100 Series of Motorola Transistor-Transistor Logic gates over conventional TTL. Design data is included which should allow determination of the operating characteristics under almost any set of conditions.

★AN-493 The MC3000/3100 Series Transistor-Transistor Logic Flip-Flops

This application note explains the basic operation of the various flip-flops available in the MC3000/3100 series of transistor-transistor logic from Motorola. Typical operating characteristics are included so that operation under different conditions can be determined.

★AN-494 The Motorola Transistor-Transistor Logic Lines

This application note contains a general description and comparison of Motorola's MTTL I, MTTL II, MTTL III, MTTL5400/7400, and the MC4000 lines. The basic gate and the MTTL III bypass circuit are discussed and tables of electrical characteristics are included. Two appendices provide definitions of common MTTL terms, a discussion of the effect of input diodes, and loading rules for the MC4000 series complex functions.

AN-215

RF SMALL SIGNAL DESIGN USING ADMITTANCE PARAMETERS

INTRODUCTION

Design of the solid-state small-signal RF amplifier using two port parameters is a systematic, mathematical procedure, with an exact solution (free from approximation) available for the complete design problem. The only sources of error in the final design are parameter variations resulting from transistor parameter distributions and strays in the physical circuit. Parameter distributions result from limits in measurement and random variations among identically designed transistors.

The purpose of this paper is to provide, in a single working reference, the important relationships necessary for the complete solution of the RF small signal design problem using admittance parameters. Further, equations are given in the appendix for the conversion of other sets of two-port parameters to admittance parameters.

The paper is based on work by Linvill[1], Stern[2], and others. Those who may wish to consider the derivations of some of the expressions should refer to the original work presented in the references.

The report assumes that the reader is familiar with the two port parameter method of describing a linear active network. Several references are available on this subject.[1,2,6]

It has also been assumed that a suitable transistor for the task at hand has been selected, and that two-port parameters are available for the frequency and bias point which will be used. Device selection will not be covered as a separate topic in this report; rather, a thorough understanding of the material in the report should provide the designer with the tools he needs to select transistors for a particular small signal application.

The equations given in the text of the report are applicable to the common emitter, common base, or common collector configuration, if the applicable set of parameters (common emitter, common base, or common collector parameters) is used. Equations for the conversion of the admittance or hybrid parameters of any configuration to either of the other two configurations of the same parameter set are given in the appendix.

While directed primarily toward circuit design with conventional junction transistors, two port network theory has the advantage of being applicable to any linear active network. The same design approach and equations may therefore be used with field effect transistors[7], integrated circuits, or any other device which may be described as a linear active two-port network with measurable parameters.

Finally, various parameter interrelationships and other data are given in the Appendix.

GENERAL DESIGN CONSIDERATIONS

Design of the RF small signal tuned amplifier is usually based on a requirement for a specified power gain at a given frequency. Other design goals include bandwidth, stability, and input-output isolation. After a basic circuit type is selected, the applicable design equations can be solved.

Circuits may be categorized according to feedback (neutralization, unilateralization, or no feedback), and matching at transistor terminals (circuit admittances either matched or mismatched to transistor input and output admittances). Each of these circuit categories will be discussed, including the applicable design equations and the considerations leading to the selection of a particular configuration.

STABILITY

A major factor in the overall design is the potential stability of the transistor. This may be determined by computing the Linvill stability factor[1] C using the following expression: †

$$C = \frac{|y_{12}\, y_{21}|}{2g_{11}\, g_{22} - \mathrm{Re}\,(y_{12}y_{21})} \qquad (1)$$

When C is less than 1, the transistor is unconditionally stable. When C is greater than 1, the transistor is potentially unstable.

The C factor is a test for stability under a hypothetical worst case condition; that is, with both input and output transistor terminals open circuited. With no external feedback, an unconditionally stable transistor will not oscillate with any combination of source and load. If a transistor is potentially unstable, certain source and load combinations will produce oscillations.

Although the C factor may be used to determine the potential stability of a transistor, the conditions of open circuited source and load which are assumed in the C factor test are not applicable to a practical amplifier. Consequently it is also desirable to compute the relative stability of actual amplifier circuits, and Stern[2] has defined a stability factor k for this purpose. The k factor is similar to the C factor except that it also takes into account finite source and load admittances connected to the transistor. The expression for k is:

$$k = \frac{2\,(g_{11} + G_s)\,(g_{22} + G_L)}{|y_{12}y_{21}| + \mathrm{Re}\,(y_{12}y_{21})} \qquad (2)$$

If k is greater than one, the circuit will be stable. If k is less than one, the circuit will be potentially unstable and will very likely oscillate at some frequency.

Note that the C factor simply predicts potential stability of a transistor with an open circuited source and load, while the k factor provides a stability computation for a specific circuit.

Stability considerations will be discussed further in the descriptions of each basic circuit type to follow.

GENERAL DESIGN EQUATIONS

There are a number of design equations which are applicable to most types of amplifiers. These equations will be discussed first. Descriptions of specific amplifier types will then follow, and each will contain additional design equations applicable to that particular amplifier.

POWER GAIN

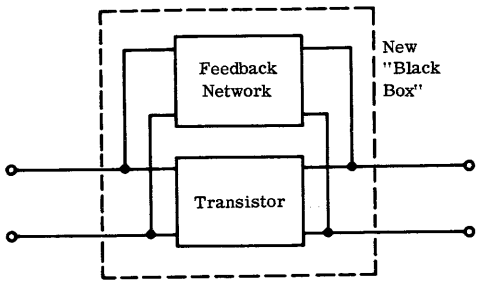
The general expression for power gain is:

$$G = \frac{|y_{21}|^2\, \mathrm{Re}\,(Y_L)}{\left|Y_L + y_{22}\right|^2 \mathrm{Re}\left(y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L}\right)} \qquad (3)$$

Equation 3 applies to circuits with no external feedback. It can also be used with circuits which have external feedback if the composite y parameters of both transistor and feedback network are substituted for the transistor y parameters in the equation. The composite y parameters

† $\mathrm{Re}\,(Y_{12}Y_{21})$ = Real part of $(Y_{12}Y_{21})$

are determined by considering the transistor and the feedback network to be two "black boxes" in parallel:



For example, the above combination of transistor and feedback network may be characterized as a single "black box" by the following equations:†

$$y_{11c} = y_{11t} + y_{11f}$$
$$y_{12c} = y_{12t} + y_{12f}$$
$$y_{21c} = y_{21t} + y_{21f} \qquad (4)$$
$$y_{22c} = y_{22t} + y_{22f}$$

Where:

y_{11c}, y_{12c}, y_{21c}, y_{22c} are the composite y parameters of the parallel combination of transistor and feedback network.

y_{11t}, y_{12t}, y_{21t}, y_{22t} are the y parameters of the transistor.

y_{11f}, y_{12f}, y_{21f}, y_{22f} are the y parameters of the feedback network.

Note that, since this approach treats the transistor and feedback network combination as a single "black box" with y_{11c}, y_{12c}, y_{21c}, and y_{22c} as its y parameters, the composite y parameters may therefore be substituted in any of the design equations applicable to a linear, active, two port analysis.

The neutralized and unilateralized amplifiers are special cases of this general concept, and equations associated with those special cases will be given later.

Equation 3 provides a solution for power gain of the linear active network (transistor) only. Input and output networks are considered to be part of the source and load, respectively. Two important points should therefore be kept in mind:

(1) Power gain computed from equation 3 will not take into account network losses. Input network loss reduces power delivered to the transistor. Power lost in the output network is computed as useful power output, since the load admittance Y_L is the combination of the output network and its load.

(2) Power gain is independent of source admittance. An input mismatch results in less input power being delivered to the transistor. Accordingly, note that equation 3 does not contain the term Y_S.

†Refer to Seshu and Balabanian, "Linear Network Analysis, "John Wiley and Sons, 1959, P321

The power gain of a transistor together with its associated input and output networks may be computed by measuring the input and output network losses, and subtracting them from the power gain computed with equation 3 .

In some cases it may be desirable to include the effects of input matching in power gain computations. A convenient term is transducer gain G_T, defined as output power delivered to a load by the transistor, divided by the maximum input power available from the source.

The equation for transducer gain is:

$$G_T = \frac{4 \, \mathrm{Re}(Y_s) \, \mathrm{Re}(Y_L) \, |y_{21}|^2}{|(y_{11} + Y_s)(y_{22} + Y_L) - y_{12}y_{21}|^2} \qquad (5)$$

In this equation, Y_L is the composite transistor load admittance-composed of both output network and its load, and Y_S is the composite transistor source admittance-composed of both input network and its source. Therefore, transducer gain includes the effects of the degree of admittance match at the transistor input terminals but does not take into account input and output network losses.

As in equation 3 , the composite y parameters of a transistor feedback network combination may be substituted for the transistor y parameters when such a combination is used.

The Maximum Available Gain MAG is an often used transistor figure-of-merit. The MAG is the theoretical power gain of a transistor with its reverse transfer admittance y_{12} set equal to zero, and its source and load admittances conjugately matched to y_{11} and y_{22}, respectively.

If $y_{12} = 0$, the transistor exhibits an input admittance equal to y_{11} and an output admittance equal to y_{22}.† The equation for MAG is, therefore, obtained by solving the general power gain expression, equation 3 , with the conditions

$$y_{12} = 0$$
$$y_L = y_{22}^*$$
$$\text{and } y_s = y_{11}^*$$

which yields:

$$MAG = \frac{|y_{21}|^2}{4 \, \mathrm{Re}(y_{11}) \, \mathrm{Re}(y_{22})} \qquad (6)$$

MAG is a figure of merit only, since it is physically impossible to reduce y_{12} to zero without changing the other parameters of the transistor. An external feedback network may be used to achieve a composite y_{12} of zero, but then the other composite parameters will also be modifed according to the relationships given in the discussion of the composite transistor - feedback network "black box."

TRANSISTOR INPUT AND OUTPUT ADMITTANCES

The expression for the input admittance of a transistor is:

$$Y_{IN} = y_{11} - \frac{y_{12} y_{21}}{y_{22} + Y_L} \qquad (7)$$

†Obtained by solving the equations for transistor Y_{IN} and Y_{OUT} with y_{12} equal to zero. These equations are given later in the report.

The expression for the output admittance of a transistor is:

$$Y_{OUT} = y_{22} - \frac{y_{12}\, y_{21}}{y_{11} + Y_s} \qquad (8)$$

When the feedback parameter y_{12} is not zero, Y_{IN} is dependent on load admittance and Y_{OUT} is dependent on source admittance.

AMPLIFIER STABILITY

One of the major considerations in RF amplifier design is stability. The stability of a final design can be assured by including stability computations and considering stability in all design decisions relating to feedback and transistor source and load admittances.

The potential stability of the transistor should first be computed using equation 1 .

The various alternatives concerning input - output matching and neutralization - unilateralization will now be discussed for both the unconditionally stable transistor and the potentially unstable transistor.

THE UNCONDITIONALLY STABLE TRANSISTOR

When the Linvill stability factor of the transistor as determined by equation 1 is less than one, the transistor is unconditionally stable. Oscillations will not occur using any combination of source and load admittances without external feedback. Stability is therefore eliminated as a factor in the remainder of the design, and complete freedom is possible with regard to matching and neutralization to optimize the amplifier for other performance requirements.

AMPLIFIERS WITHOUT FEEDBACK

The amplifier with no feedback is a logical choice for the unconditionally stable transistor in many applications since it may offer the advantages of fewer components and a simple tuning procedure.

Source and load admittances may be selected for maximum gain and/or any number of other requirements. Power gain and transducer gain may be computed using equations 3 and 5 , respectively; input and output admittances may be computed using equations 7 and 8 , respectively.

The amplifier stability factor may be computed using equation 2 . While amplifier stability was assured from the beginning by the use of an unconditionally stable transistor, the designer may still wish to perform this computation to provide some insight into danger of instability under adverse environmental conditions, source and load variations, etc.

G_{max}

G_{max}, the highest transducer gain possible without external feedback, forms a special case of the no feedback amplifier.

The source and load admittances required to achieve G_{max} may be computed from the following:

$$G_s = \frac{1}{2\ \mathrm{Re}(y_{22})} \left| \left[2\ \mathrm{Re}(y_{11})\, \mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) \right]^2 - \left| y_{12}y_{21} \right|^2 \right|^{\frac{1}{2}} \qquad (9)$$

$$B_s = -\mathrm{Im}(y_{11}) + \frac{\mathrm{Im}(y_{21}y_{12})}{2\ \mathrm{Re}(y_{22})} \qquad (10)$$

$$G_L = \frac{1}{2\ \mathrm{Re}(y_{11})} \left| \left[2\ \mathrm{Re}(y_{11})\, \mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) \right]^2 - \left| y_{12}y_{21} \right|^2 \right|^{\frac{1}{2}} \qquad (11)$$

$$B_L = -\mathrm{Im}(y_{22}) + \frac{\mathrm{Im}(y_{21}y_{12})}{2\ \mathrm{Re}(y_{11})} \qquad (12)$$

Therefore, if the maximum possible power gain without feedback is desired for an amplifier, equations 9, 10, 11, and 12 are used to compute Y_S and Y_L.

The magnitude of G_{max} may be computed from the following expression:

$$G_{max} = \frac{|y_{21}|^2}{2\ \mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) + \left| \left[2\ \mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) \right]^2 - \left| y_{12}y_{21} \right|^2 \right|^{\frac{1}{2}}} \qquad (13)$$

Equations 9, 10, 11, and 12 can be obtained by differentiating equation 5 with respect to G_S, B_S, G_L, and B_L, and setting the four derivatives equal to zero. The G_S, B_S, G_L, and B_L thus computed can then be substituted in equation 5 to obtain the expression for G_{max}, equation 13.

THE LINVILL METHOD

The amplifier without feedback design problem may also be solved graphically using a technique developed by J.G. Linvill.† Linvill's technique is very useful for a certain class of problems. Since it is so fully discussed in many good references we will not go into it further here. An advantage of the Linvill technique is that it provides a reasonably rapid graphic solution relating gain, bandwidth, and stability. A disadvantage is its scope of usefulness, since the standard Linvill solution applies only to an amplifier with no external feedback and with Y_S conjugately matched to the transistor input admittance, Y_{IN}.

THE UNILATERALIZED AMPLIFIER

Unilateralization consists of employing an external feedback network to achieve a composite y_{12} of zero.

While unilateralization is perhaps most often used to achieve stability with a potentially unstable transistor, other circuit considerations may also warrant the use of unilateralization with the unconditionally stable transistor. For example, the input-output isolation afforded by unilateralization may be desirable in a particular design.

Design equations for the unilateralized case are obtained by first computing the composite y parameters of the transistor - feedback network combination and then substituting the composite parameters in the general equations.

Referring to the discussion on composite y parameters and setting up the basic condition that y_{12c} must equal zero, the other composite y parameters can be computed. Assuming that a passive feedback network is being used, then

$$y_{11f} = y_{22f} = -y_{12f} = -y_{21f},$$

and since $y_{12c} = 0$, $y_{12t} + y_{12f} = 0$

then $y_{12t} = -y_{12f}$,

and $y_{12t} = -y_{12f} = y_{11f} = y_{22f} = -y_{21f}$

†Application Note AN166.
See also reference 5 in the bibliography.

Substituting the above results in equations 4 yields the following:

$$y_{11c} = y_{11t} + y_{12t}$$

$$y_{22c} = y_{22t} + y_{12t}$$

$$y_{12c} = y_{12t} - y_{12t} = 0$$

$$y_{21c} = y_{21t} - y_{12t}$$

Substituting these composite y parameters in equations 7, 8, 3, 16, and 5 respectively, yields equations 14, 15, 16, 17 and 18 for the unilateralized case:

Unilateralized input admittance

$$Y_{IN} = y_{11} + y_{12} \tag{14}$$

Unilateralized output admittance

$$Y_{OUT} = y_{22} + y_{12} \tag{15}$$

Unilateralized power gain, general expression:

$$G_{PU} = \frac{\left|y_{21} - y_{12}\right|^2 \mathrm{Re}\,(Y_L)}{\left|Y_L + y_{22} + y_{12}\right|^2 \mathrm{Re}(y_{11})} \tag{16}$$

Unilateralized power gain with Y_L conjugately matched to Y_{OUT}:

$$G_U = \frac{\left|y_{21} - y_{12}\right|^2}{4\,\mathrm{Re}(y_{11} + y_{12})\,\mathrm{Re}(y_{22} + y_{12})} \tag{17}$$

Unilateralized transducer gain:

$$G_{TU} = \frac{4\,\mathrm{Re}(Y_s)\,\mathrm{Re}(Y_L)\left|y_{21} - y_{12}\right|^2}{\left|(y_{11} + y_{12} + Y_s)(y_{22} + y_{12} + Y_L)\right|^2} \tag{18}$$

Note that equations 14, 15, 16, 17, and 18, are given entirely in terms of the transistor y parameters, not those of the feedback network or the composite.

Another benefit of unilateralization is input - output isolation. As can be seen in equations 14 and 15, Y_{IN} is completely independent of Y_L, and Y_{OUT} is similarly independent of Y_S. In a practical sense, this means that in a single or multi-stage amplifier using unilateralized stages, tuning of any one network will not affect tuning in other parts of the circuit. Thus, the troublesome task of having to re-peak an entire amplifier following a change in tuning at a single point can be eliminated.

NEUTRALIZATION

Neutralization consists of employing a feedback network to reduce y_{12} to some value other than zero. Neutralization is generally used for the same purposes as unilateralization, but provides something less than the ideal cancellation of the transistor feedback parameter which unilateralization achieves. A typical example of neutralization might be a feedback network which provides a composite b_{12} of zero while having only a negligible effect on the transistor g_{12}.

The equations for a particular neutralized case would be developed in the same manner as those for the unilateralized case. Since there are an infinite number of possibilities, no specific equations will be given here.

This completes the discussion of design with the unconditionally stable transistor. The potentially unstable transistor will now be considered.

THE POTENTIALLY UNSTABLE TRANSISTOR

When the Linvill stability factor of the transistor as determined by equation 1 is greater than one, the transistor is potentially unstable. Certain combinations of source and load admittances will cause oscillations if no feedback is used. In designing with the potentially unstable transistor, steps must be taken to insure that the amplifier will be stable.

Stability is usually achieved by one or both of two methods:

(1) Using a feedback network which reduces the composite y_{12} to a value which insures stability.

(2) Choosing a source and load admittance combination which provides stability.

A discussion of these basic methods is given below.

USING FEEDBACK TO ACHIEVE STABILITY

Either unilateralization or neutralization may be used to achieve stability. If unilateralization is used, the transistor-feedback network combination will be unconditionally stable. This may be verified by computing the Linvill stability factor of the combination. Since $y_{12c} = 0$, the numerator in equation 1 would be zero.

With stability thus assured, the remainder of the design may then be done to satisfy other requirements placed on the amplifier. After unilateralization has converted the potentially unstable transistor to an unconditionally stable combination, all other aspects of the design are identical to the unilateralized case with the unconditionally stable transistor. Power gains and input and output admittances may be computed using equations 14 through 18.

If neutralization is used to achieve stability, the Linvill stability factor can be used to compute the potential stability of any transistor - neutralization-network combination. Since in this case $y_{12c} \neq 0$, C will have a value other than zero.

After unconditional stability of the transistor-neutralization network combination has been achieved, the design may then be completed by treating the combination as an unconditionally stable transistor, and proceeding with the case of the unconditionally stable transistor in an amplifier without feedback. Power gains, input and output admittances, and the circuit stability factor may be computed by using the composite parameters of the combination in equations 2, 3, 5, 7, and 8.

STABILITY WITHOUT FEEDBACK

A stable design with the potentially unstable transistor is possible without external feedback by proper choice of source and load admittances. This can be seen by inspection of equation 2; G_S and/or G_L can be made large enough to yield a stable circuit regardless of the degree of potential instability of the transistor.

This suggests a relatively simple way to achieve a stable design with a potentially unstable transistor. A circuit stability factor k is selected, and equation 2 is used to arrive at values of G_S and G_L which will provide the desired k. In achieving a particular circuit stability factor, the designer may choose any of the following combinations of matching or mismatching of G_S and G_L to the transistor input and output conductances, respectively:

(1) G_S matched and G_L mismatched

(2) G_L matched and G_S mismatched

(3) Both G_S and G_L mismatched

Often a decision on which combination to use will be dictated by other performance requirements or practical considerations.

Once G_S and G_L have been chosen, the remainder of the design may be completed using the relationships which apply to the amplifier without feedback. Power gain and input and output admittances may be computed using equations 3, 5, 7, and 8.

Although the above procedure may be adequate in many cases, a more systematic method of source and load admittance determination is desirable for designs which demand maximum power gain per degree of circuit stability. Stern has analyzed this problem and developed equations for computing the conductance and susceptance of both Y_S and Y_L for maximum power gain for a particular circuit stability factor.[2,4] These equations are given here:

$$G_s = \sqrt{\frac{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}{2}} \cdot \sqrt{\frac{g_{11}}{g_{22}}} - g_{11} \tag{19}$$

$$G_L = \sqrt{\frac{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}{2}} \cdot \sqrt{\frac{g_{22}}{g_{11}}} - g_{22} \tag{20}$$

$$B_s = \frac{(G_s + g_{11})\ Z_o}{\sqrt{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}} - b_{11} \tag{21}$$

$$B_L = \frac{(G_L + g_{22})\ Z_o}{\sqrt{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}} - b_{22} \tag{22}$$

Where,

$$Z = \frac{(B_s + b_{11})(G_L + g_{22}) + (B_L + b_{22})\ k(L+M)/2(G_L + g_{22})}{\sqrt{k\ (L + M)}} \tag{23}$$

$$L = \left|y_{12}y_{21}\right| \tag{24}$$

$$M = \mathrm{Re}(y_{12}y_{21}) \tag{25}$$

Defining D as the denominator in equation 5 yields:

$$D = \frac{Z^4}{4} + \frac{\left[k(L + M) + 2M\right] Z^2}{2} - 2NZ\sqrt{k(L + M)} + A^2 + N^2 \tag{26}$$

where,

$$A = \frac{k(L + M)}{2} - M, \tag{27}$$

$$N = \mathrm{Im}(y_{12}y_{21}), \tag{28}$$

and,

Z_o = that real value of Z which results in the smallest minimum of D, found by setting,

$$\frac{dD}{dZ} = Z^3 + \left[k(L + M) + 2M\right] Z - 2N\sqrt{k(L + M)}. \tag{29}$$

equal to zero.

Computation of Y_S and Y_L using equations 19 through 29 is a bit tedious to be done very frequently, and this may have discouraged wide usage of the complete Stern solution. However, examination of Stern's work suggests some interesting shortcuts:

(A) COMPUTATION OF G_S AND G_L ONLY, USING EQUATIONS 19 AND 20. If a value equal to $-b_{22}$ is then chosen for B_L, the resulting Y_L will be very close to the true Y_L for maximum gain. The transistor Y_{IN} can then be computed from Y_L using equation 7, and B_S can be set equal to $-I_m(Y_{IN})$.

Computation of B_S and B_L comprise by far the more complex portion of the Stern solution. This alternate method therefore permits the designer to closely approximate the exact Stern solution for Y_S and Y_L while avoiding that portion of the computations which are the most complex and time consuming. Further, the circuit can be designed with tuning adjustments for varying B_S and B_L, thereby creating the possibility of experimentally achieving the true B_S and B_L for maximum gain as accurately as if all the Stern equations had been solved.

(B) MISMATCHING G_S TO g_{11} AND G_L TO g_{22} BY AN EQUAL RATIO YIELDS A TRUE STERN SOLUTION FOR G_S AND G_L. This can be derived from equations 19 and 20, which lead to the following result:

$$\frac{G_L}{g_{22}} = \frac{G_s}{g_{11}} \tag{30}$$

If a mismatch ratio, R, is defined as follows,

$$R = \frac{G_L}{g_{22}} = \frac{G_s}{g_{11}} \tag{31}$$

then R may be computed for any particular circuit stability factor using the equation:

$$(1 + R)^2 = k\left[\frac{\left|y_{21}y_{12}\right| + \mathrm{Re}(y_{12}y_{21})}{2\ g_{11}\ g_{22}}\right] \tag{32}$$

Equation 32 was derived from equations 2 and 31. Having thus determined R, G_S and G_L can be quickly found using equation 31.

B_S and B_L can then be determined in the manner described above in alternate method (A).

This alternate method may be advantageous if source and load admittances and power gains for several different values of k are desired. Once the R for a particular k has been determined, the R for any other k may be quickly found from the equation

$$\frac{(1 + R_1)^2}{(1 + R_2)^2} = \frac{k_1}{k_2} \tag{33}$$

where R_1 and R_2 are values of R corresponding to k_1 and k_2, respectively.

(C) COMPUTER DESIGN. The complete Stern design problem may be programmed into a computer. Power gain, circuit stability factor, Y_S and Y_L can be obtained from the computer for any value of k. MAG, G_U, and the Linvill stability factor of the transistor may also be included in the program.

After employing either the complete Stern solution or an alternate method to obtain Y_S and Y_L for the potentially unstable transistor in an amplifier without feedback, power gains and input and output admittances may be obtained using equations 3, 5, 7, and 8.

SENSITIVITY

In all but the unilateralized amplifier, Y_{IN} is a function of load admittance. Thus Y_{IN} changes with output circuit tuning, and this can be troublesome. Consequently, it is sometimes desirable to compute the extent of variation of Y_{IN} with changes in Y_L. A term, sensitivity δ, has been defined to provide a measure of this characteristic, and is equal to per cent change in Y_{IN} divided by per cent change in Y_L. The equation for sensitivity is:

$$\delta = \left|\frac{Y_L}{y_{22} + Y_L}\right| \cdot \left|\frac{g_{11}}{y_{11}}\right| \cdot \frac{K}{\left|\frac{y_{22} + Y_L}{g_{22}} + \frac{g_{11}}{y_{11}}\ K\ e^{j\Theta}\right|} \tag{34}$$

where,

$$K = \left|\frac{y_{21}\ y_{12}}{g_{11}\ g_{22}}\right|$$

$$\Theta = \arg\ (-y_{12}y_{21}) \cdot$$

$$K\ e^{j\Theta} = K\ (\cos\Theta + j\ \sin\Theta)$$

A more complete discussion of sensitivity is given in reference 6.

SUMMARY

The small signal amplifier performance of a transistor is completely described by two port admittance parameters. Based on these parameters, equations for computing the stability, gain, and optimum source and load admittances for the unilateralized, neutralized, and no-feedback amplifier cases have been discussed.

The unconditionally stable transistor will not oscillate with any combination of source and load admittances, and circuits using a stable transistor may be optimized for other performance requirements without fear of oscillations.

The potentially unstable transistor requires that steps be taken to guarantee a stable design. Stability is usually achieved by unilateralization, neutralization, or selection of source and load admittances which result in a stable amplifier.

Unilateralization and neutralization reduce the composite reverse transfer admittance. They may be used to achieve stability, input - output isolation, or both.

Maximum power gain per degree of circuit stability without feedback may be achieved using Stern's equations.

The degree of input - output isolation is described by the term sensitivity, which makes it possible to compute changes in input admittance for any change in load admittance.

The theory and design equations in this report are applicable to any linear active device which may be characterized as a two-port network. Therefore, the term "transistor" used herein refers generally to all such devices, including FETs and integrated circuits.

BIBLIOGRAPHY

1. "Transistors and Active Circuits," by Linvill and Gibbons, McGraw-Hill, 1961.
2. "Stability and Power Gain of Tuned Transistor Amplifiers," by Arthur P. Stern, Proc. IRE, March, 1957.
3. "Using Linvill Techniques for R.F. Amplifiers," Motorola Semiconductor Products, Inc., Application Note 166.
4. "High-Gain, High-Frequency Amplifiers," by Peter M. Norris, Electro-Technology, January, 1966.
5. "Linvill Technique Speeds High Frequency Amplifier Design," by John Lauchner and Marvin Silverstein, Electronic Design, April 12, 1966.
6. "The Design of Alignable Transistor Amplifiers," by J.F. Gibbons, Stanford University Technical Report No. 106, May 7, 1956.
7. "Field Effect Transistor R. F. Amplifier Design Techniques," Motorola Semiconductor Products Inc., Application Note 423.

GLOSSARY

C	=	Linvill's stability factor
k	=	Stern's stability factor
G_s	=	Real part of the source admittance
G_L	=	Real part of the load admittance
B_s	=	Imaginary part of the source admittance
B_L	=	Imaginary part of the load admittance
g_{11}	=	Real part of y_{11}
g_{22}	=	Real part of y_{22}
G	=	Generalized power gain
Y_L	=	Complex load admittance
Y_s	=	Complex source admittance
G_T	=	Transducer gain
MAG	=	Maximum available gain
*	=	Conjugate
Y_{IN}	=	Input admittance
Y_{OUT}	=	Output admittance
G_{max}	=	Maximum gain without feedback
G_U	=	Unilateralized gain
G_{TU}	=	Unilateralized transducer gain
δ	=	Sensitivity

APPENDIX I

A. Conversions among parameter types for y, z, h, and g parameters.

h to y

$$y_{11} = \frac{1}{h_{11}} \qquad y_{12} = \frac{-h_{12}}{h_{11}} \qquad y_{21} = \frac{h_{21}}{h_{11}} \qquad y_{22} = \frac{\Delta h}{h_{11}}$$

where $\Delta h = h_{11} h_{22} - h_{12} h_{21}$

y to h

$$h_{11} = \frac{1}{y_{11}} \qquad h_{12} = \frac{-y_{12}}{y_{11}} \qquad h_{21} = \frac{y_{21}}{y_{11}} \qquad h_{22} = \frac{\Delta y}{y_{11}}$$

where $\Delta y = y_{11} y_{22} - y_{12} y_{21}$

h to z

$$z_{11} = \frac{\Delta h}{h_{22}} \qquad z_{12} = \frac{h_{12}}{h_{22}} \qquad z_{21} = \frac{-h_{21}}{h_{22}} \qquad z_{22} = \frac{1}{h_{22}}$$

z to h

$$h_{11} = \frac{\Delta z}{z_{22}} \qquad h_{12} = \frac{z_{12}}{z_{22}} \qquad h_{21} = \frac{-z_{21}}{z_{22}} \qquad h_{22} = \frac{1}{z_{22}}$$

where $\Delta z = z_{11} z_{22} - z_{12} z_{21}$

h to g

$$g_{11} = \frac{h_{22}}{\Delta h} \qquad g_{12} = \frac{-h_{12}}{\Delta h} \qquad g_{21} = \frac{-h_{21}}{\Delta h} \qquad g_{22} = \frac{h_{11}}{\Delta h}$$

where $\Delta h = h_{11} h_{22} - h_{12} h_{21}$

g to h

$$h_{11} = \frac{g_{22}}{\Delta g} \qquad h_{12} = \frac{-g_{12}}{\Delta g} \qquad h_{21} = \frac{-g_{21}}{\Delta g} \qquad h_{22} = \frac{g_{11}}{\Delta g}$$

where $\Delta g = g_{11} g_{22} - g_{12} g_{21}$

z to y

$$y_{11} = \frac{z_{22}}{\Delta z} \qquad y_{12} = \frac{-z_{12}}{\Delta z} \qquad y_{21} = \frac{-z_{21}}{\Delta z} \qquad y_{22} = \frac{z_{11}}{\Delta z}$$

where $\Delta z = z_{11} z_{22} - z_{12} z_{21}$

y to z

$$z_{11} = \frac{y_{22}}{\Delta y} \qquad z_{12} = \frac{-y_{12}}{\Delta y} \qquad z_{21} = \frac{-y_{21}}{\Delta y} \qquad z_{22} = \frac{y_{11}}{\Delta y}$$

where $\Delta y = y_{11} y_{22} - y_{12} y_{21}$

z to g

$$g_{11} = \frac{1}{z_{11}} \qquad g_{12} = \frac{-z_{12}}{z_{11}} \qquad g_{21} = \frac{z_{21}}{z_{11}} \qquad g_{22} = \frac{\Delta z}{z_{11}}$$

where $\Delta z = z_{11} z_{22} - z_{12} z_{21}$

g to z

$$z_{11} = \frac{1}{g_{11}} \qquad z_{12} = \frac{-g_{12}}{g_{11}} \qquad z_{21} = \frac{g_{21}}{g_{11}} \qquad z_{22} = \frac{\Delta g}{g_{11}}$$

where $\Delta g = g_{11} g_{22} - g_{12} g_{21}$

g to y

$$y_{11} = \frac{\Delta g}{g_{22}} \qquad y_{12} = \frac{g_{12}}{g_{22}} \qquad y_{21} = \frac{-g_{21}}{g_{22}} \qquad y_{22} = \frac{1}{g_{22}}$$

where $\Delta g = g_{11} g_{22} - g_{12} g_{21}$

y to g

$$g_{11} = \frac{\Delta y}{y_{22}} \qquad g_{12} = \frac{y_{12}}{y_{22}} \qquad g_{21} = \frac{-y_{21}}{y_{22}} \qquad g_{22} = \frac{1}{y_{22}}$$

where $\Delta y = y_{11} y_{22} - y_{12} y_{21}$

B. Conversions among common emitter, common base, and common collector parameters of the same type for y, and h parameters.

Common emitter y parameters in terms of common base and common collector y parameters.

$$y_{11e} = y_{11b} + y_{12b} + y_{21b} + y_{22b} = y_{11c}$$

$$y_{12e} = -(y_{12b} + y_{22b}) = -(y_{11c} + y_{12c})$$

$$y_{21e} = -(y_{21b} + y_{22b}) = -(y_{11c} + y_{21c})$$

$$y_{22e} = y_{22b} = y_{11c} + y_{12c} + y_{21c} + y_{22c}$$

Common base y parameters in terms of common emitter and common collector y parameters.

$$y_{11b} = y_{11e} + y_{12e} + y_{21e} + y_{22e} = y_{22c}$$

$$y_{12b} = -(y_{12e} + y_{22e}) = -(y_{21c} + y_{22c})$$

$$y_{21b} = -(y_{21e} + y_{22e}) = -(y_{12c} + y_{22c})$$

$$y_{22b} = y_{22e} = y_{11c} + y_{12c} + y_{21c} + y_{22c}$$

Common collector y parameters in terms of common emitter and common base y parameters.

$$y_{11c} = y_{11e} = y_{11b} + y_{12b} + y_{21b} + y_{22b}$$

$$y_{12c} = -(y_{11e} + y_{12e}) = -(y_{11b} + y_{21b})$$

$$y_{21c} = -(y_{11e} + y_{21e}) = -(y_{11b} + y_{12b})$$

$$y_{22c} = y_{11e} + y_{12e} + y_{21e} + y_{22e} = y_{11b}$$

Common emitter h parameters in terms of common base and common collector h parameters.

$$h_{11e} = \frac{h_{11b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{h_{11b}}{1 + h_{21b}} = h_{11c}$$

$$h_{12e} = \frac{h_{11b} h_{22b} - h_{12b}(1+h_{21b})}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{h_{11b} h_{22b}}{1 + h_{21b}} - h_{12b} = 1-h_{12c}$$

$$h_{21e} = \frac{-h_{21b}(1-h_{12b}) - h_{22b} h_{11b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{-h_{21b}}{1 + h_{21b}} = -(1 + h_{21c})$$

$$h_{22e} = \frac{h_{22b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{h_{22b}}{1 + h_{21b}} = h_{22c}$$

Common base h parameters in terms of common emitter and common collector h parameters.

$$h_{11b} = \frac{h_{11e}}{(1 + h_{21e})(1-h_{12e}) + h_{11e} h_{22e}} \approx \frac{h_{11e}}{1 + h_{21e}}$$

$$= \frac{h_{11c}}{h_{11c} h_{22c} - h_{21c} h_{12c}} \approx \frac{-h_{11c}}{h_{21c}}$$

$$h_{12b} = \frac{h_{11e} h_{22e} - h_{12e}(1 + h_{21e})}{(1 + h_{21e})(1-h_{12e}) + h_{11e} h_{22e}} \approx \frac{h_{11e} h_{22e}}{1 + h_{21e}} - h_{12e}$$

$$= \frac{h_{21c}(1-h_{12c}) + h_{11c} h_{22c}}{h_{11c} h_{22c} - h_{21c} h_{12c}} \approx (h_{12c} - 1) - \frac{h_{11c} h_{22c}}{h_{21c}}$$

$$h_{21b} = \frac{-h_{21e}(1-h_{12e}) - h_{11e} h_{22e}}{(1 + h_{21e})(1-h_{12e}) + h_{11e} h_{22e}} \approx \frac{-h_{21e}}{1 + h_{21e}}$$

$$= \frac{h_{12c}(1 + h_{21c}) - h_{11c} h_{22c}}{h_{11c} h_{22c} - h_{21c} h_{12c}} \approx \frac{-(1 + h_{21c})}{h_{21c}}$$

$$h_{22b} = \frac{h_{22e}}{(1 + h_{21e})(1-h_{12e}) + h_{11e} h_{22e}} \approx \frac{h_{22e}}{1 + h_{21e}}$$

$$= \frac{h_{22c}}{h_{11c} h_{22c} - h_{21c} h_{12c}} \approx \frac{h_{22c}}{h_{21c}}$$

Common collector h parameters in terms of common base and common emitter h parameters.

$$h_{11c} = \frac{h_{11b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b}\,h_{11b}} \approx \frac{h_{11b}}{1 + h_{21b}} = h_{11e}$$

$$h_{12c} = \frac{1 + h_{21b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b}\,h_{11b}} \approx 1 = 1-h_{12e}$$

$$h_{21c} = \frac{h_{12b} - 1}{(1 + h_{21b})(1-h_{12b}) + h_{22b}\,h_{11b}} \approx \frac{-1}{1 + h_{21b}} = -(1 + h_{21e})$$

$$h_{22c} = \frac{h_{22b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b}\,h_{11b}} \approx \frac{h_{22b}}{1 + h_{21b}} = h_{22e}$$

Expressions for voltage gain, current gain, input impedance, and output impedance in terms of y, z, h, and g parameters.

Voltage Gain

$$A_v = \frac{z_{21}\,Z_L}{\Delta z + z_{11}\,Z_L} = \frac{-y_{21}}{y_{22} + Y_L} = \frac{-h_{21}\,Z_L}{h_{11} + \Delta h Z_L} = \frac{g_{21}\,Z_L}{g_{22} + Z_L}$$

Current Gain

$$A_i = \frac{-z_{21}}{z_{22} + Z_L} = \frac{-y_{21}\,Y_L}{\Delta y + y_{11}\,Y_L} = \frac{-h_{21}\,Y_L}{h_{22} + Y_L} = \frac{-g_{21}}{\Delta g + g_{11}\,Z_L}$$

Input Impedance

$$Z_{IN} = \frac{\Delta z + z_{11}\,Z_L}{z_{22} + Z_L} = \frac{y_{22} + Y_L}{\Delta y + y_{11}\,Y_L} = \frac{\Delta h + h_{11}\,Y_L}{h_{22} + Y_L} = \frac{g_{22} + Z_L}{\Delta g + g_{11}\,Z_L}$$

Output Impedance

$$Z_{OUT} = \frac{\Delta z + z_{22}\,Z_s}{z_{11} + Z_s} = \frac{y_{11} + Y_s}{\Delta y + y_{22}\,Y_s} = \frac{h_{11} + Z_s}{\Delta h + h_{22}\,Z_s} = \frac{\Delta g + g_{22}\,Y_s}{g_{11} + Y_s}$$

Conversion between y parameters and s (scattering) parameters:

$$s_{11} = \frac{(1-y_{11})(1+y_{22}) + y_{12}\,y_{21}}{(1+y_{11})(1+y_{22}) - y_{12}\,y_{21}}\ \dagger$$

$$s_{12} = \frac{-2y_{12}}{(1+y_{11})(1+y_{22}) - y_{12}\,y_{21}}\ \dagger$$

$$s_{21} = \frac{-2y_{21}}{(1+y_{11})(1+y_{22}) - y_{12}\,y_{21}}\ \dagger$$

$$s_{22} = \frac{(1+y_{11})(1-y_{22}) + y_{21}\,y_{12}}{(1+y_{11})(1+y_{22}) - y_{12}\,y_{21}}\ \dagger$$

$$y_{11} = \left[\frac{(1+s_{22})(1-s_{11}) + s_{12}\,s_{21}}{(1+s_{11})(1+s_{22}) - s_{12}\,s_{21}}\right]\frac{1}{Z_o}$$

$$y_{12} = \left[\frac{-2s_{12}}{(1+s_{11})(1+s_{22}) - s_{12}\,s_{21}}\right]\frac{1}{Z_o}$$

$$y_{21} = \left[\frac{-2s_{21}}{(1+s_{11})(1+s_{22}) - s_{12}\,s_{21}}\right]\frac{1}{Z_o}$$

$$y_{22} = \left[\frac{(1+s_{11})(1-s_{22}) + s_{12}\,s_{21}}{(1+s_{22})(1+s_{11}) - s_{12}\,s_{21}}\right]\frac{1}{Z_o}$$

Where Z_O = the characteristic impedance of the transmission lines used in the scattering parameter system, usually 50 ohms.

Conversion between h parameters and s parameters:

$$s_{11} = \frac{(h_{11}-1)(h_{22}+1) - h_{12}\,h_{21}}{(h_{11}+1)(h_{22}+1) - h_{12}\,h_{21}}\ \dagger\dagger$$

$$s_{12} = \frac{2h_{12}}{(h_{11}+1)(h_{22}+1) - h_{12}\,h_{21}}\ \dagger\dagger$$

$$s_{21} = \frac{-2h_{21}}{(h_{11}+1)(h_{22}+1) - h_{12}\,h_{21}}\ \dagger\dagger$$

$$s_{22} = \frac{(1+h_{11})(1-h_{22}) + h_{12}\,h_{21}}{(h_{11}+1)(h_{22}+1) - h_{12}\,h_{21}}\ \dagger\dagger$$

$$h_{11} = \left[\frac{(1+s_{11})(1+s_{22}) - s_{12}\,s_{21}}{(1-s_{11})(1+s_{22}) + s_{12}\,s_{21}}\right] Z_o$$

$$h_{12} = \frac{2s_{12}}{(1-s_{11})(1+s_{22}) + s_{12}\,s_{21}}$$

$$h_{21} = \frac{-2s_{21}}{(1-s_{11})(1+s_{22}) + s_{12}\,s_{21}}$$

$$h_{22} = \left[\frac{(1-s_{22})(1-s_{11}) - s_{12}\,s_{21}}{(1-s_{11})(1+s_{22}) + s_{12}\,s_{21}}\right]\frac{1}{Z_o}$$

---

† In converting from y to s parameters, the y parameters must first be multiplied by Z_O and then substituted in the equations for conversion to s parameters.

†† In converting from h to s parameters, the h parameters must first be normalized to Z_O in the following manner and then substituted in the equations for conversion to s parameters:

Parameter	To Normalize
h_{11}	divide by Z_o
h_{12}	use as is
h_{21}	use as is
h_{22}	multiply by Z_o

AN-245 A
AN INTEGRATED SENSE AMPLIFIER FOR CORE MEMORIES

INTRODUCTION

A definition of a sense amplifier could be "the interface circuitry between the storage elements of a memory and the logic output elements of the memory." By this definition, a sense amplifier can have many different type inputs and outputs. This paper will discuss a sense amplifier for ferrite core memories. Specific sense amplifier requirements were received from computer and core memory manufacturers. From these requirements, design goals were evolved for a sense amplifier that would satisfy the market.

An integrated sense amplifier offers advantages other than such obvious ones as saving weight, space, and assembly wiring; the inherent ability to match active components within the integrated circuit gives the integrated sense amplifier a distinct advantage over the discrete versions. In some cases, it would be very difficult to build a discrete circuit of the same quality as an integrated circuit, or to do so could be quite expensive. Therefore, a well-designed integrated sense amplifier will offer superior performance and be less expensive than its discrete counterpart.

THE CORE MEMORY

Figure 1 is a typical core memory subsystem of a general purpose digital computer. The appropriate x and y lines are selected by the memory address register (MAR). The selection technique depends on the memory organization and will not be discussed in this application note. The most common organizations use one core per bit so the number of cores which must be sensed simultaneously is determined by the "word" length. However, each sense line links one bit for all words in the memory. When a particular word is selected the sense amplifiers detect the presence of "ones" or "zeroes" in all the bits and this information is then placed in the memory data register (MDR). The time required to get the information from the cores to the MDR is called the "access" time. If the memory is of the "destructive readout" type, the information in the MDR must be written back into the memory at the same location. The time required to do this is called the "write" time. The sum of the "read" and "write" times is defined as the cycle time and indicates the speed of the memory.

The various memory organizations use different sense line configurations and current drive techniques. However, in all the configurations the sense winding is routed so as to obtain an optimum signal-to-noise ratio. This generally means the sense winding goes through half the cores in one direction and half in the opposite direction (See Figure 2). The purpose of this wiring technique is to

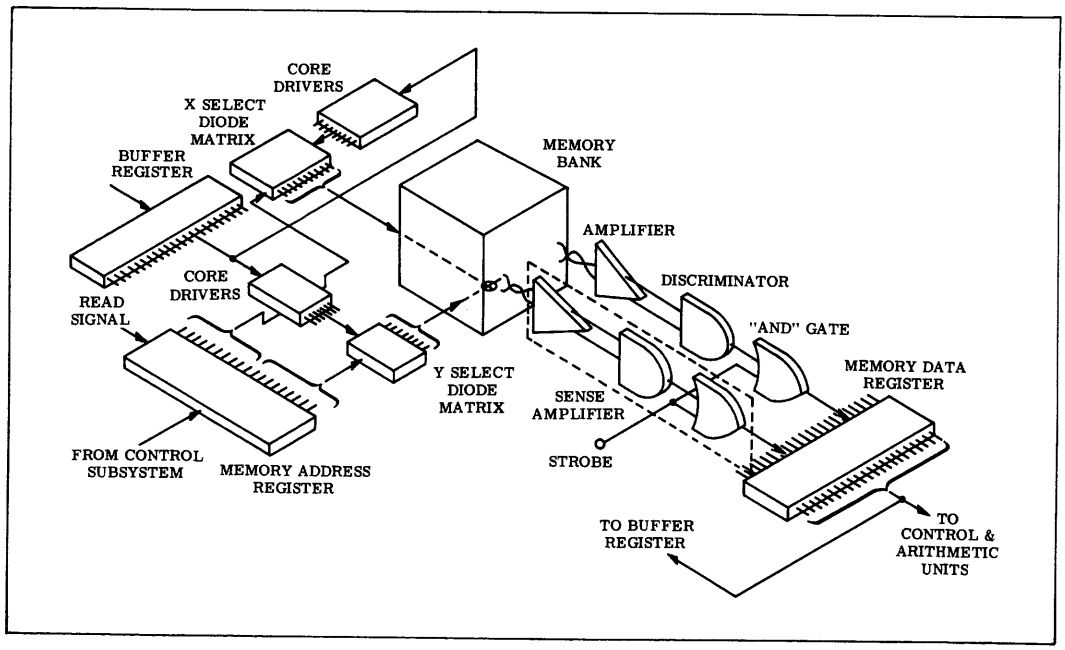


FIGURE 1 — GENERAL PURPOSE COINCIDENT CURRENT CORE MEMORY SUBSYSTEM

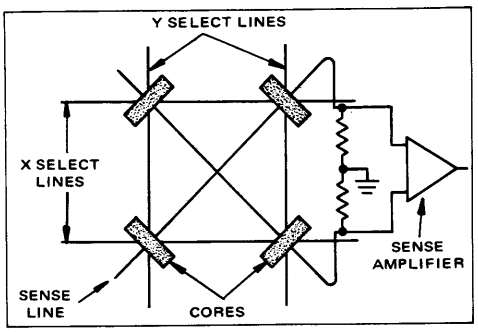


FIGURE 2 – HALF SELECT WIRING

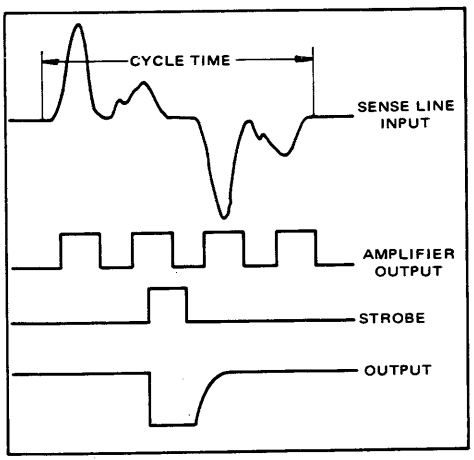


FIGURE 3a – TYPICAL SIGNAL WAVEFORMS

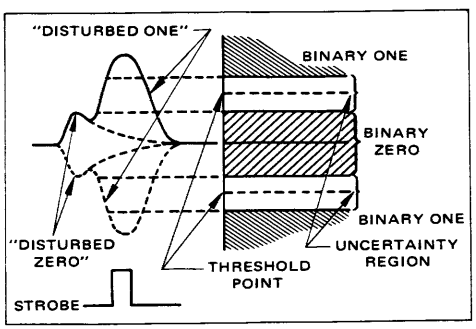


FIGURE 3b – TYPICAL CORE OUTPUT SIGNAL

cause voltages induced in the sense line to cancel. The sense amplifier must detect the difference between the minimum "disturbed one" signal and the maximum "disturbed zero" signal. The "disturbed one" signal can be either positive or negative so the sense amplifier must be bipolar (See Figure 3a).

Typical signal waveforms at the input to the sense amplifier, amplifier output, discriminator output, and strobe are shown in Figure 3a. This is an idealized signal waveform at the input to the sense amplifier. In actuality, there are common and differential mode noise at the input during most of the memory cycle. Figure 3b shows the typical signal as seen at the input to the sense amplifier. The amplitude of the "disturbed one" signal depends on the size of the core and the rise time and amplitude of the select currents from the core drivers. The area between the minimum "disturbed one" signal and the maximum sum of "disturbed zero" signals is called the uncertainty region (See Figure 3b). This area would ideally be as large as possible, since it is very important in the overall performance of the memory subsystem. Normally, the threshold of the sense amplifier will be set in the middle of the uncertainty region.

SENSE AMPLIFIER DESIGN CRITERIA

Many factors must be considered in the design of an integrated core memory sense amplifier. First, the amplifier should be as versatile as possible. The design must meet a wide variety of speed requirements and should be suitable for low cost fabrication. Additional criteria are:

1. The amplifier must be able to detect bipolar signals.
2. The threshold should be adjustable in order to meet the maximum number of requirements with a single amplifier.
3. The threshold should be constant with temperature. This requires the memory manufacturer to compensate the switching currents for the change in core output voltage rather than depend on the sense amplifier to have precisely the correct threshold versus temperature characteristic.
4. The uncertainty region should be as small as possible.
5. The power supplies should be commonly used values and the tolerances on these supplies should be as loose as possible.
6. The sense amplifier requires a strobe to "enable" the amplifier at the optimum point.
7. The bandwidth of the amplifier must be sufficiently high to pass the fastest rise time signals with as little degradation as possible.
8. The amplifier must be able to recover rapidly from large common mode and large differential mode signals.

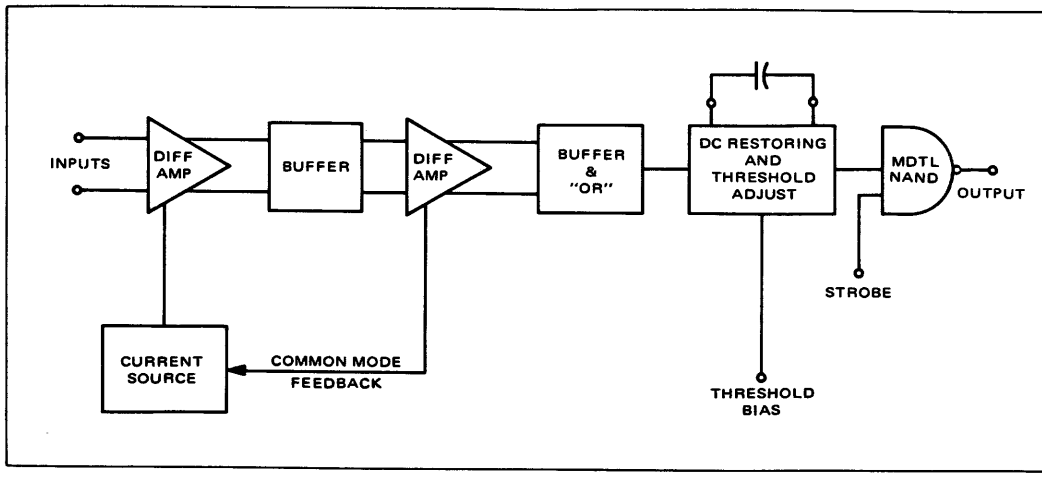


FIGURE 4 – BLOCK DIAGRAM OF MC1540

THE MC1540

Figure 4 is a block diagram of the MC1540. The amplifier portion is a two-stage differential amplifier with emitter degeneration in each stage, buffering between stages, and overall common mode feedback. The schematic of the amplifier section is shown in Figure 5. The low frequency differential voltage gain of the first stage, assuming it is driven from a voltage source, can be closely approximated by:

$$A_{diff} \approx \frac{R_L}{r_e + R_E + \frac{r_b}{\beta + 1}}$$

R_E is the emitter degeneration resistor on each side and r_e approximately $\frac{KT}{qI_E}$. With β relatively high, the last term in the denominator can be neglected and the equation for the gain reduces to the following equation:

$$A_{diff} \approx \frac{R_L}{r_e + R_E} = \frac{R_L}{R_E} \frac{1}{1 + \frac{r}{R_E}}$$

This equation shows that the gain is a function of resistor ratios rather than resistor magnitudes. R_L and R_E are formed during the base diffusion so that the ratio R_L/R_E should be constant from run to run. Also, r_e is directly proportional to a resistor which is formed during the base diffusion and is a function of temperature so that gain variations with temperature change are to be expected. However, the gain variation will be significantly less than for a circuit with no emitter degeneration.

Since the amplifier incorporates differential gain of the first stage and single ended gain of the second stage, the overall gain can be approximated by the following equation:

$$A \approx \left(\frac{R_{L_1}}{r_{e_1} + R_{E_1}}\right) \left[\frac{R_{L_2}}{2(r_{e_2} + R_{E_2})}\right]$$

The buffering between the two stages significantly increases the bandwidth of the amplifier. Without buffering, the predominant pole would be caused by the Miller effect capacitance of the second stage being driven from a high impedance. Buffering reduces this impedance approximately by a factor of β of the transistor.

Some of the data taken on this amplifier in integrated form is shown below.

1. Voltage gain – The voltage gain on all units was between 37.5 dB and 40 dB.
2. Gain versus temperature – The gain changed less than 1.0 dB when the temperature was varied over a -55°C to +125°C range.
3. Bandwidth – The 3.0 dB point on all units was in excess of 50 MHz. The rise time of the amplifier was less than 7.0 ns.
4. Propagation delay – This was found to be between 8.0 and 11.0 ns on all units. The measurement was made between the 50% points of the input and the output waveforms. The rise and fall times of the input were approximately 10 ns and the amplitude was 25 mV.
5. Common mode rejection – The low level common mode rejection defined as the differential mode gain divided by the common mode gain, was found to be 57.0 dB at 10 MHz. Figures 6a and 6b show the amplifier response to a ± 1.0 volt and a ± 2.0 volt common mode input respectively. Figure 6c shows the amplifier response to a 20 mV differential input.

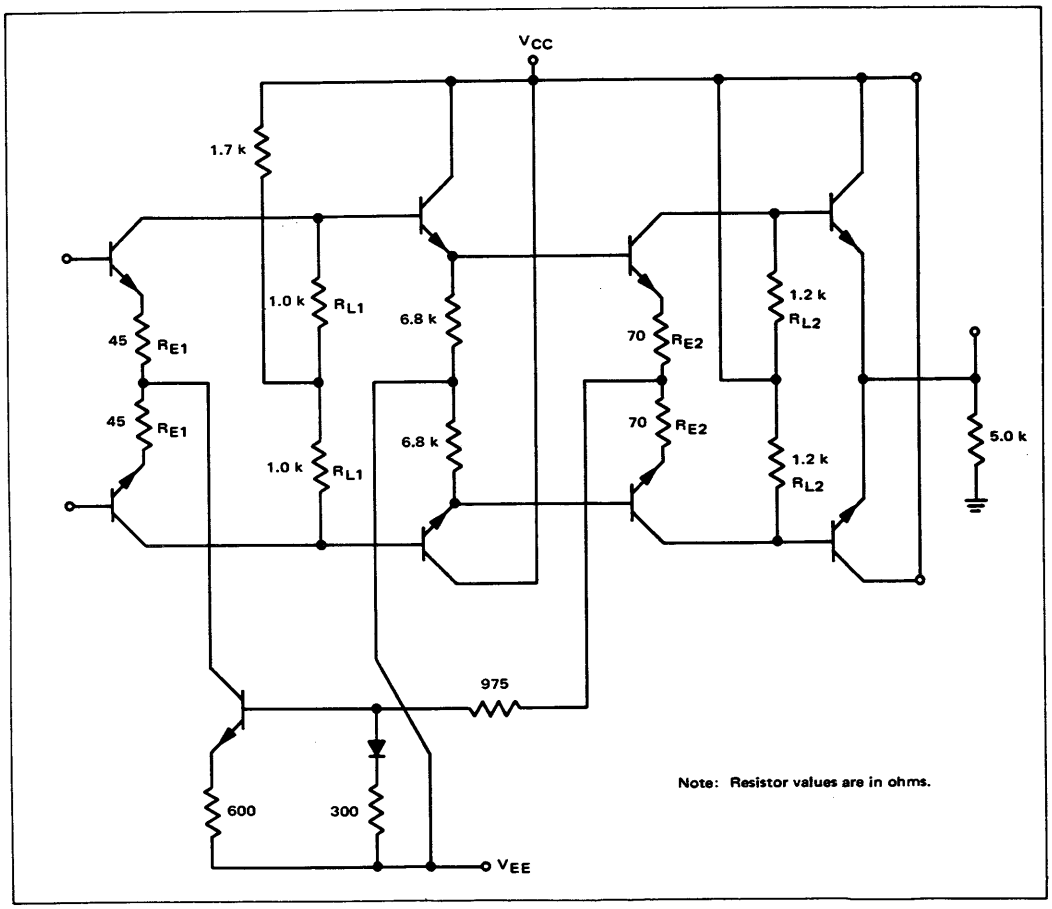


FIGURE 5 – DIFFERENTIAL AMPLIFIER SCHEMATIC

The schematic of the dc restoration circuit, the threshold adjusting circuit, and the output gate is shown in Figure 7. The threshold of the sense amplifier is dependent upon the dc voltage at point A. Since R1 is much larger than R2 or R3, changes in the dc voltage at point C reflects as a dc voltage change at point A; thus, the threshold changes.

The dc restoration action can be explained as follows: The input signal to the collector of Q_1 and the capacitor is positive from a low impedance and the entire signal is coupled through the capacitor. When the leading edge of the signal occurs at point A, both the base-emitter junctions of Q_1 and the gate input diode become reverse biased and the capacitor will start to charge through R4. When the negative going edge of the signal arrives at point A, Q_1 is turned on, and point A becomes a low impedance node because of the emitter follower action. The capacitor will discharge through Q_1 very rapidly. The base of Q_1 is driven by a low impedance source so that the transient base current during the time the capacitor is being discharged produces a negligible voltage change at the base of Q_1. Also Q_1 is designed to supply the maximum transient current required for pulse widths up to 750 ns. Since the dc level at the emitter of Q_1 is restored rapidly, the sense amplifier threshold does not change significantly with a change in duty cycle.

As temperature increases, the threshold of the DTL gate decreases by 2 $\Delta V_{BE}/^{o}C$. The four diodes in the base of Q_2 will decrease the dc level at the base of Q_2 by 4 $\Delta V_{BE}/^{o}C$. The V_{BE} change of Q_1 will cancel one of these, and the V_{BE} change of Q_2 will cancel another; hence the dc level at point A will also decrease by 2 $\Delta V_{BE}/^{o}C$. Therefore, if the amplifier voltage gain does not change with temperature, the sense amplifier threshold will be constant.

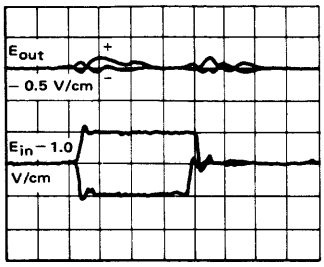


FIGURE 6a – COMMON MODE RECOVERY TIME (E_{in} = ± 1.0 V)

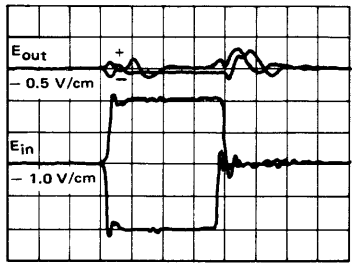


FIGURE 6b – COMMON MODE RECOVERY TIME (E_{in} = ± 2.0 V)

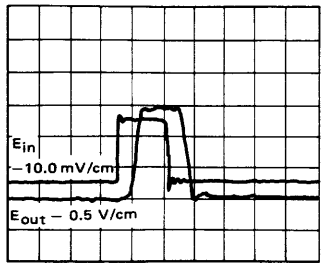


FIGURE 6c – AMPLIFIER RESPONSE TIME

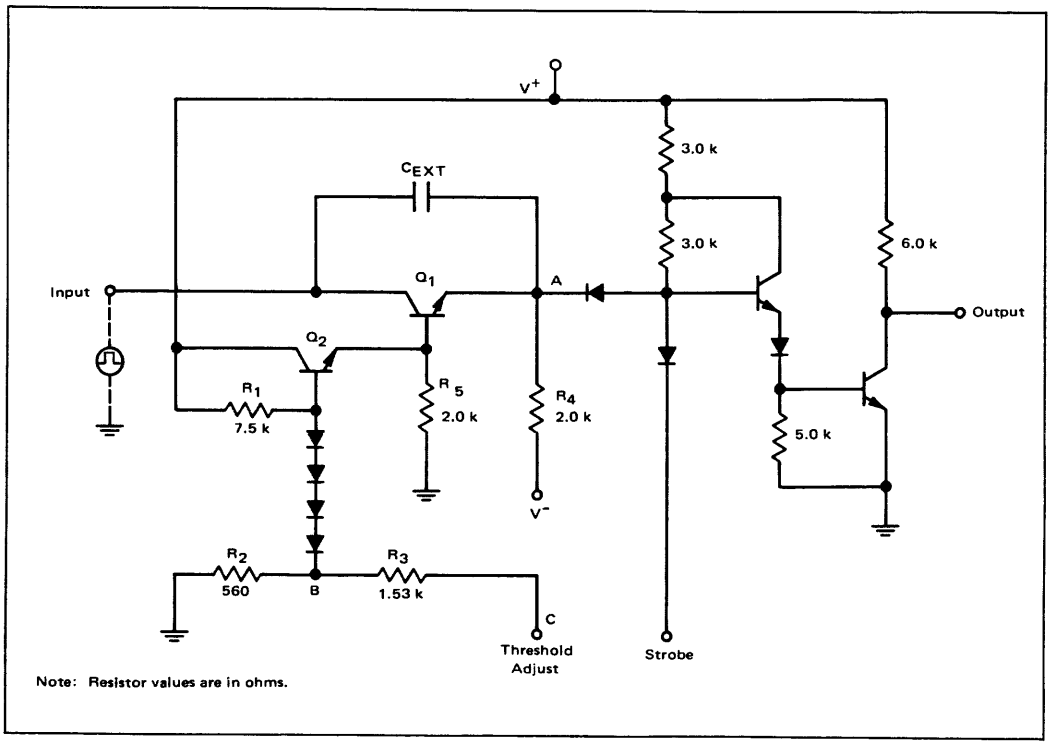


FIGURE 7 – DC RESTORATION CIRCUIT, THRESHOLD ADJUSTING CIRCUIT, AND OUTPUT GATE

The output gate is similar to that of the popular MDTL logic family. Both the amplified signal from the memory and the strobe signal must be above the gate threshold level before the output transistor will saturate. The output transistor is capable of "sinking" 6.0 mA with a saturation voltage less than 400 mV. This guarantees a noise margin equal to that of the MDTL logic family. Many sense amplifiers may be strobed from a common source with no ill effects, as long as the driving unit has sufficient fan-out capability. Also the outputs of several sense amplifiers can be wire-ORed. Figure 8 shows the voltage transfer characteristic of the gate. The width of the transition is approximately 200 mV. This would refer to the input of the sense amplifier as a transition width of 2.0 mV if the voltage gain was 100.

Additional data taken on the sense amplifier are listed below.

1. Threshold – 17 mV nominal for $V^- = -6.0$ V, $V^+ = +6.0$ V, and $V_{th} = -6.0$ V.
2. Threshold temperature coefficient – $-10\ \mu V/^oC$.
3. Threshold range – The nominal threshold varies from 13 mV at -5.0 V threshold bias to 21 mV at -7.0 V threshold bias.
4. Propagation delay from input to output – Typically 20 ns.
5. Propagation delay from strobe input to output – Typically 10 ns.

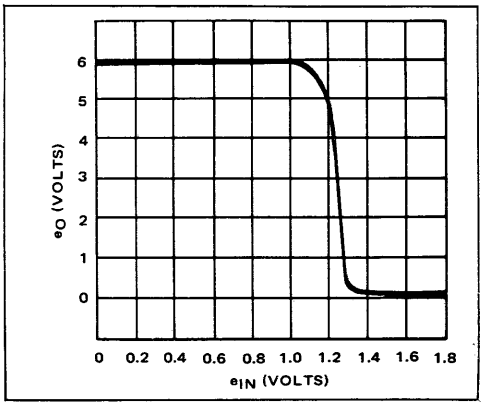


FIGURE 8 – OUTPUT GATE TRANSFER CHARACTERISTICS

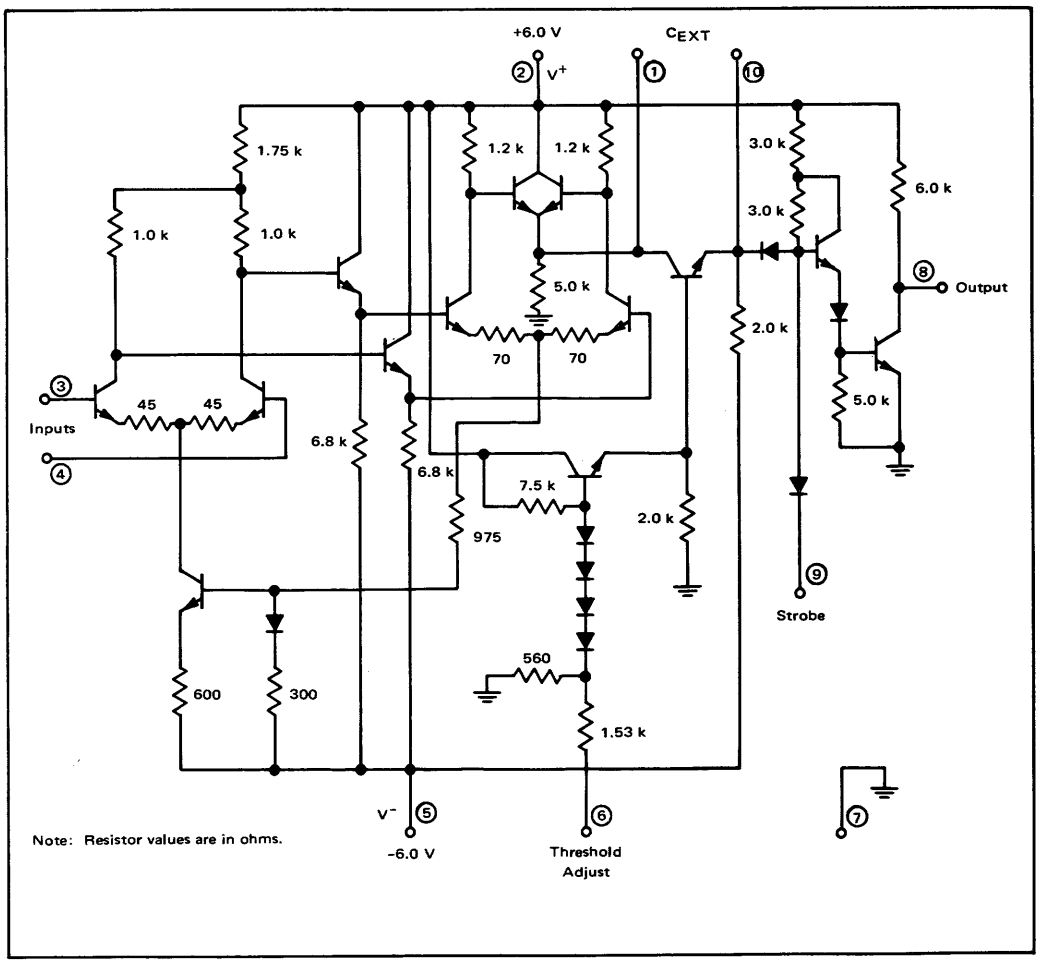


FIGURE 9 – CORE MEMORY SENSE AMPLIFIER

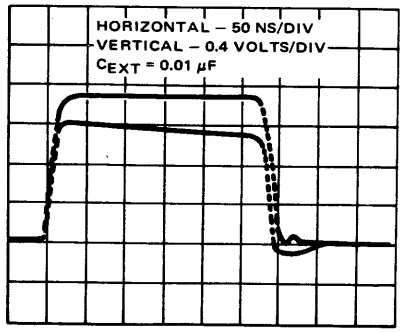


FIGURE 10 – SIGNAL WAVEFORM AT PINS ONE AND TEN

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Threshold	V_{th}	14	17	20	mV
Uncertainty Region			2	6	mV
Amplifier Voltage Gain	Av		80		
Propagation					
Input to Amplifier Output	$t_{3^+10^+}$			15	ns
Input to Gate Output	$t_{3^+8^-}$			30	ns
Strobe to Gate Output	$t_{9^+8^-}$			15	ns
Recovery Time					
e_{in} = ±400 mV (DM)	tr (DM)		20	50	ns
e_{in} = ±2.0 volts (CM)	tr (CM)		40	50	ns

Figure 9 is the schematic of the complete sense amplifier. External components that must be supplied are appropriate resistors for terminating the sense windings and a coupling capacitor. The size of the capacitor is dependent on the width of the disturbed "1" signal from the memory. The capacitor should be of sufficient size to ensure that the "sagging" due to the capacitor charging does not affect the threshold. Also the capacitor must be large enough so that noise, just before the disturbed "1" signal, does not affect the threshold. Figure 10 illustrates the charging and discharging time of a 0.01 μF capacitor. The typical excursion below the base line is approximately 100 mV for an input pulse 300 ns wide.

The rise time of the output can be decreased significantly by connecting an external resistor from the output to the positive power supply. This resistor must be large enough so that the sum of the current through the resistor and the current from an external load does not exceed the rated value of 6.0 mA if a 400 mV V_{sat} at +125°C is a required specification.

The sense amplifier also works fine with +5.0 V and -6.0 V power supplies. If the threshold-adjust pin is also tied to -6.0 V, the nominal threshold increases to approximately 20 mV. However, -5.3 volts on the threshold-adjust pin sets the nominal threshold at 17 mV for +5.0 V and -6.0 V power supply operation. If the threshold-adjust pin is tied to the negative power supply, the nominal threshold is also 17 mV for power supplies of +5.0 V and -5.0 V. Operation is marginal for ±4.5 V power supplies. Therefore it is recommended that ±5% supplies be used if the sense amplifier is operated with ±5.0 V power supplies.

SPECIFICATIONS

Specifications for a sophisticated integrated circuit must be such that the customer is guaranteed a circuit that will meet his requirements. The most important specifications for a sense amplifier are threshold limits (or uncertainty region), propagation delays, and recovery times. Other characteristics must also be limited so that good circuit performance and reliability result.

Some of the important specifications for the MC1540 are listed in the table above. For a complete specification and the manner in which each test is made, refer to the MC1540 data sheet.

SUMMARY

The MC1540 was designed with both customer requirements and integrated circuit production capabilities in mind. The circuit will operate properly with large variations in temperature and power supplies. It requires only three external components to achieve the complete core memory sense amplifier function. It has a saturated logic type output and can be strobed from any saturated logic family. It can be packaged in either the 10 pin TO-5, the 10 pin ceramic flat pack, or the dual in-line plastic package.

AN-261

TRANSISTOR LOGARITHMIC CONVERSION USING AN INTEGRATED OPERATIONAL AMPLIFIER

INTRODUCTION

Many approaches have been made to the design of logarithmic amplifier circuits, using both active and passive elements. With the proper circuit configuration of diodes or transistors a log amplifier can be constructed using the logarithmic characteristics of these semiconductor devices. All diodes and transistors do not exhibit good logarithmic characteristics, so care must be taken in selecting the proper device. This application note deals with a technique for obtaining logarithmic conversion using operational amplifier-transistor feedback circuits, beginning with an analysis of the logarithmic characteristics of transistors. A brief look at the basic logarithmic amplifier will be given followed by two log function generator applications: direct multiplication of two numbers, and solution of the parabolic equation $Z = X^n$.

TRANSISTOR LOGARITHMIC CHARACTERISTICS

Shockley's first-order theory of a p-n junction

$$I = I_o [e^{(qV/kT)} - 1]$$

considers only diffusion current; however, it is popular because of its simplicity. In other circumstances the series resistance associated with the bulk semiconductor material must be accounted for. Also such mechanisms as surface inversion layers and generation-recombination in the space charge regions are not accounted for in the above expression. Consequently a diode or transistor configuration must be devised which will minimize these adverse effects. The common base transistor configuration discussed in this application note does this very well. By using the transfer conductance and fulfilling certain conditions, the desired logarithmic characteristics can be obtained.

The derivation of the transfer conductance is based around an NPN silicon all-diffused transistor as shown in Figure 1. The detailed derivation is given in the Appendix. The resulting collector current expression is

$$I_c = -\alpha_n I_{es} [e^{qV_E/kT}] \qquad (1)$$

It is important to note that a non-constant base transport factor will cause α_N to vary, consequently, a diffused base transistor such as the 2N2218 is best suited for this application. The base transport factor is within a few tenths of a percent of unity. The upper end range of equation (1) is usually between 1 and 10 mA of collector current depending upon the junction area and contact size of the transistor being used. Measurements elsewhere[1] indicate an 8 to 10 decade range of collector current yielding a logarithmic relation. Simple practical integrated circuit operational amplifiers operating with only a single polarity input are limited to from 3 to 7 decades depending upon the particular amplifier being used and also on the effort expended to reduce external disturbances.

LOGARITHMIC AMPLIFIER TRANSFER FUNCTION

The basic function generator configuration for logarithmically compressing data is shown in Figure 2. In this configuration the requirement that the collector voltage be equal to zero is virtually met. The small amount of collector potential that does exist will be negligible for all practical purposes. Rewriting equation (1) for the direction of collector current shown in Figure 2, we find

$$I_c = +\alpha_n I_{es} [e^{qV_E/kT}] \qquad (2)$$

If $I_b \ll I_c$, which is the condition that governs the lower limit of operation, then

$$I_c = \frac{E_{in}}{R_s} \qquad (3)$$

The polarity of V_E is shown in Figure 2. Combining equations (2) and (3) and the condition of $V_{out} = V_E$ yields

$$\frac{E_{in}}{R_s} = \alpha_n I_{es} [e^{qV_{out}/kT}]$$

or

$$V_{out} = \frac{kT}{q} \ln \frac{E_{in}}{R_s \alpha_n I_{es}}$$

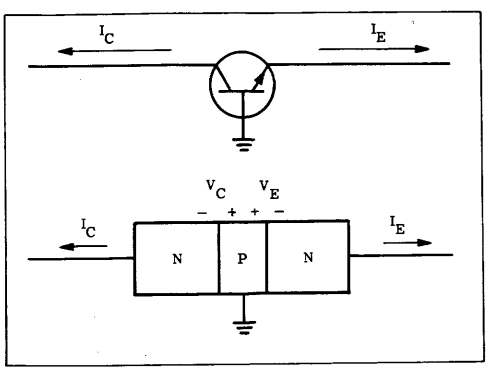


FIGURE 1 — NPN SILICON TRANSISTOR MODEL

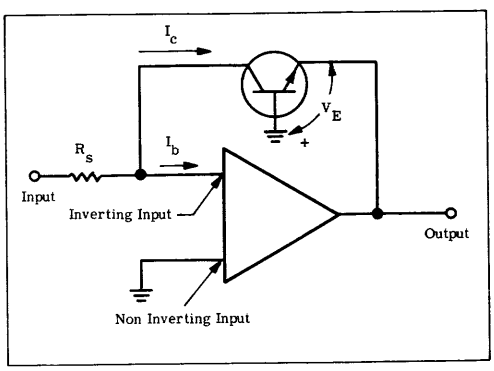


FIGURE 2 — BASIC LOG AMPLIFIER

Converting from $\ln_e$ to $\log_{10}$ gives

$$V_{out} = 2.3 \frac{kT}{q} \log_{10} \left(\frac{E_{in}}{R_s \alpha_n I_{es}}\right)$$

$$V_{out} = 2.3 \frac{kT}{q} \log_{10}(E_{in}) + 2.3 \left(\frac{kT}{q}\right) \log_{10} \left(\frac{1}{R_s \alpha_n I_{es}}\right) \quad (4)$$

at $T = 27°C$ $\quad \frac{kT}{q} = 0.026\ V$

$$V_{out} = 0.06 \log_{10}(E_{in}) + K \quad (5)$$

The empirical results obtained from the log amplifier are plotted in Figure 3a. From Figure 3a the transfer function was found to be

$$E_{out} = 0.062 \log_{10}(E_{in}) + 0.450 \quad (6)$$

where E_{out} and E_{in} are in volts.

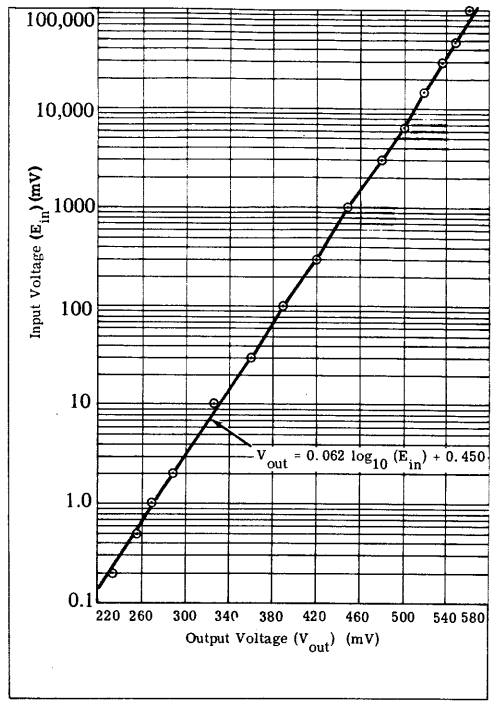


FIGURE 3a — INPUT VS. OUTPUT RESPONSE OF LOGARITHMIC AMPLIFIER OF FIGURE 3b

OPERATIONAL AMPLIFIER LOG AMPLIFIER

The operational amplifier used in the log amplifier is the MC 1533. Frequency compensation of the operational amplifier is chosen such that the amplifier will be stable with a closed loop gain of unity. The 0.1 μF capacitor between pins 1 and 5 is necessary to reduce the ac gain of the feedback transistor. It is usually necessary to bypass the power supplies right at the amplifier socket with a 0.01 or 0.1 μF low-inductive capacitor to eliminate any internal high frequency oscillations which might occur because of excessive impedance in the power supplies.

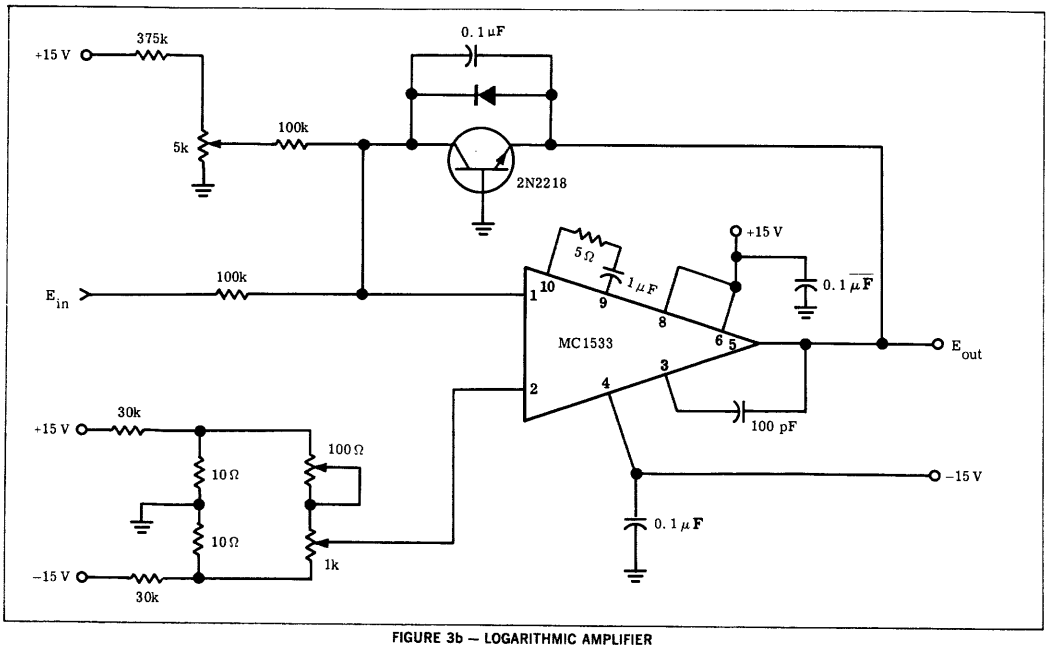


FIGURE 3b — LOGARITHMIC AMPLIFIER

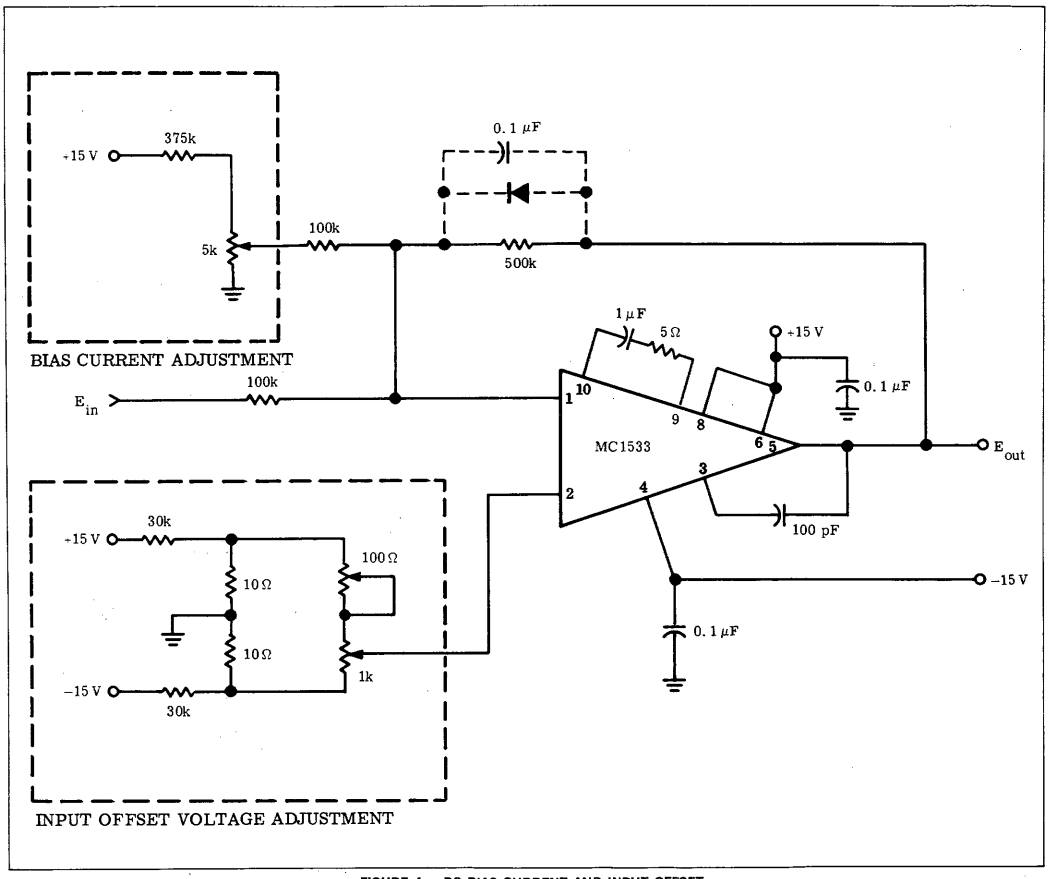


FIGURE 4 — DC BIAS CURRENT AND INPUT OFFSET VOLTAGE SUPPLIES

The extremely wide range of input voltage required makes it necessary that input offset voltage and bias currents be properly compensated for. The typical bias current for the MC 1533 is 0.5 μA. If the amplifier were used without proper bias current compensation, this would require an input voltage of 50 mV above a 100k input resistor just to overcome the bias current requirements. This would immediately swamp out the lower end input of a 4 to 5 decade log amplifier where input voltages are in the 1 to 10 mV range. Input offset voltage, which is reflected to the output by the closed loop gain of the amplifier, will cause an appreciable error, and must be compensated for with an external supply.

The method of dc compensation used is shown in Figure 4. The input offset voltage adjustment is made with pin 1 shorted to ground and E_{out} adjusted to zero. The bias current adjustment is accomplished by placing a 500k feedback resistor in place of the transistor and then monitoring E_{out} and E_{in} and adjusting the bias current pot until E_{out}/E_{in} = 500k/100k = 5 throughout the desired input range. This procedure must be carried out individually for each operational amplifier that is to be used as a log amplifier. After completion of the bias adjustments, the feedback resistor may be replaced by the feedback transistor in the configuration shown in Figure 3b.

The same type of bias current compensation is required in the $\log^{-1}$ amplifier where input voltage levels are in the 300 to 600 mV range. The offset voltage adjustment, however, may be replaced by approximately 100 ohms to ground, since the offset level is insignificant with respect to the input voltage range.

The effect of having an improperly adjusted offset voltage pot or bias current pot is demonstrated in Figure 5. It may be necessary to slightly adjust the bias current pot in order to straighten out the log characteristics, even after the initial adjustment procedure. It is extremely important in applications where log-analog operations are to be performed, that the logarithmic transistors have identical characteristic slopes. Level shifts are not important, since they can be easily adjusted for at the summing point of one of the internal amplifier stages as shown later in the multiplier circuit application.

MULTIPLICATION USING TRANSISTOR LOGARITHMIC CHARACTERISTICS

The following example explains a method of obtaining the product Z = XY. The circuit used is shown in Figure 6. The inputs and output are monitored in millivolts and the scale is selected such that one machine unit equals 10 mV. The circuit can be broken into three por-

tions: the input logarithmic amplifier, the summing point amplifier, and the output $\log^{-1}$ amplifier. The frequency compensation for each amplifier is the same as that shown in Figure 3b.

A. Input Logarithmic Amplifier: Each input in this portion of the product function generator is identical to that shown in Figure 4, with the feedback resistor replaced by the log transistor. Initial adjustments must be carried out in the same manner as discussed previously. The output of amplifier #1 will be of the form

$$E_{out(1)} = -(\text{alog } X + C_1) \quad (7)$$

and amplifier #2 will be identical except for the constant C_1

$$E_{out(2)} = -(\text{alog } Y + C_2) \quad (8)$$

The constants C_1 and C_2 are in the order of 300 mV while a = 62 as determined previously from Figure 3a.

B. Summing Point Amplifier: The output of this amplifier will be

$$E_{out(SPA)} = \text{alog } X + \text{alog } Y + C_1 + C_2 - E_c$$

$$= \text{alog } XY + C_1 + C_2 - E_c \quad (9)$$

The input required for the output $\log^{-1}$ amplifier stage must be of the form alog XY + C_3. With the proper selection of E_c the term $C_1 + C_2 - E_c$ can be made equal to C_3, resulting in the required input of the $\log^{-1}$ amplifier stage.

C. Output Log^{-1} Amplifier: This stage uses a 2N2906 transistor connected in a common base configuration at the input of the operational amplifier to achieve an anti-logarithmic amplifier. This stage must have a base current supply added to avoid having base current drawn from the input voltage. Distortion in the $\log^{-1}$ characteristic would result without this supply. The initial calibration of this stage must be determined by plotting input voltage $E_{in(OLA)}$ versus output voltage on semi-log paper and adjusting the 5 k base current pot until a straight line is obtained over the desired output range.

The results obtained from this circuit configuration are tabulated in Table 1 along with the correct product and percent error. Up to 7.7% error in output voltage was observed over the 3 decades of operation; however, simple calculations indicate that a 0.35% error in $E_{in(OLA)}$ will cause a 10% error in output voltage at the upper end of the output range. A 0.51% error in $I_{in(OLA)}$ will cause a 10% error in output voltage at the lower end of the output range. It becomes apparent why both an input offset voltage adjustment supply and a base current adjustment supply must be provided for where wide ranges of input or output voltages are to occur.

ANALOG SOLUTION OF THE PARABOLIC EQUATION $Z = X^n$

The circuit shown in Figure 7 was used to generate Z for three different values of "n" (3, 2, and 0.5). The results are shown in Figures 8, 9, and 10, respectively. The value of E_c (summing point amplifier) is positive for n > 1 and negative for n < 1. As shown in Figure 7, E_c is positive and "n" is equal to 3. It is important here that the ratio of R_f/R_s be selected accurately to avoid additional error in the computation of X^n. The degree of accuracy maintained was 8% for "n" = 3, 9% for "n" = 2, and 5% for "n" = 0.5. As in the output stage of the previous application, a very small percentage error in input will increase more than an order of magnitude at the output.

Temperature variation will cause large deviations in output voltage accuracy since the output voltage of the first stage is directly proportional to temperature in degrees Kelvin.

$$E_{out(1)} = T[2.3(\frac{k}{q})\log_{10}(E_{in}) + 2.3(\frac{k}{q})\log_{10}(\frac{1}{R_s \alpha_n I_{Es}})]$$

The temperature effect will cancel itself if the junction temperatures of the input and output transistors are kept equal. Methods of obtaining the required temperature equalization might be the use of a common heatsink for all the log transistors, use of multiply packaged transistors, or ultimately the use of a monolithic chip containing the logarithmic transistors. A multiply packaged transistor MD 985 (PNP-NPN) was tried in the $Z = X^3$ configuration and resulted in an output error reduction of from 8% maximum to 4% maximum.

CONCLUSION

A diffused base transistor operating in a common base emitter follower configuration, with the collector at zero potential, has a wide range of logarithmic impedance. This configuration can be used to obtain a logarithmic compression of input data over 6 decades of operation with an error of less than 1%. The author feels that additional range could be obtained by the use of a chopper stabilized operational amplifier. Two arithmetic problem solution applications were shown; however, accuracy was limited by temperature variations, interstage inaccuracies, and resistor ratio inaccuracies over the three decades of input and output swing. A monolithic configuration of log transistors is felt to be the best method of compensation for temperature effects.

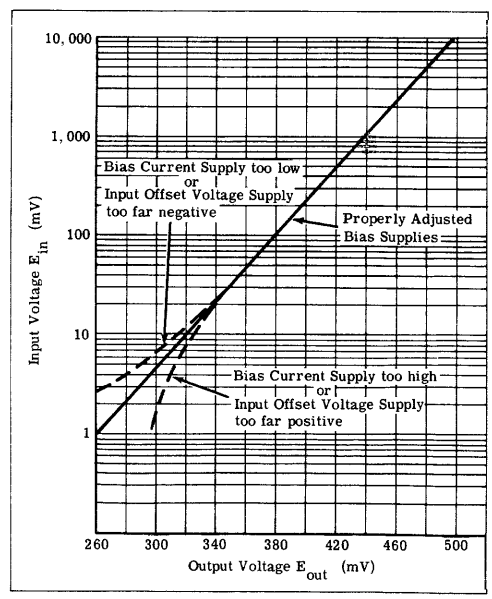


FIGURE 5 — IMPROPER DC COMPENSATION EFFECTS

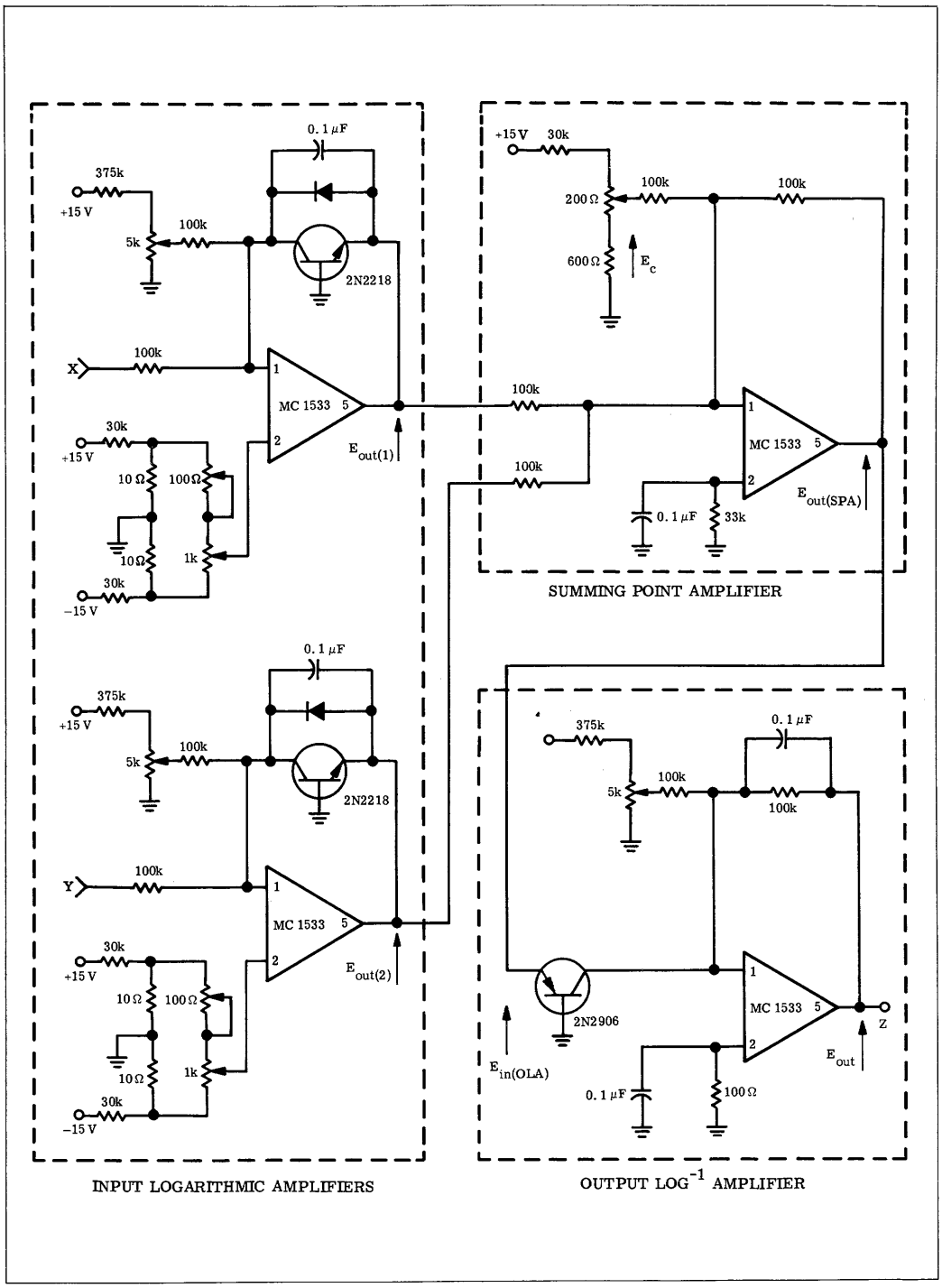


FIGURE 6 – CIRCUIT FOR Z = XY FUNCTION GENERATOR

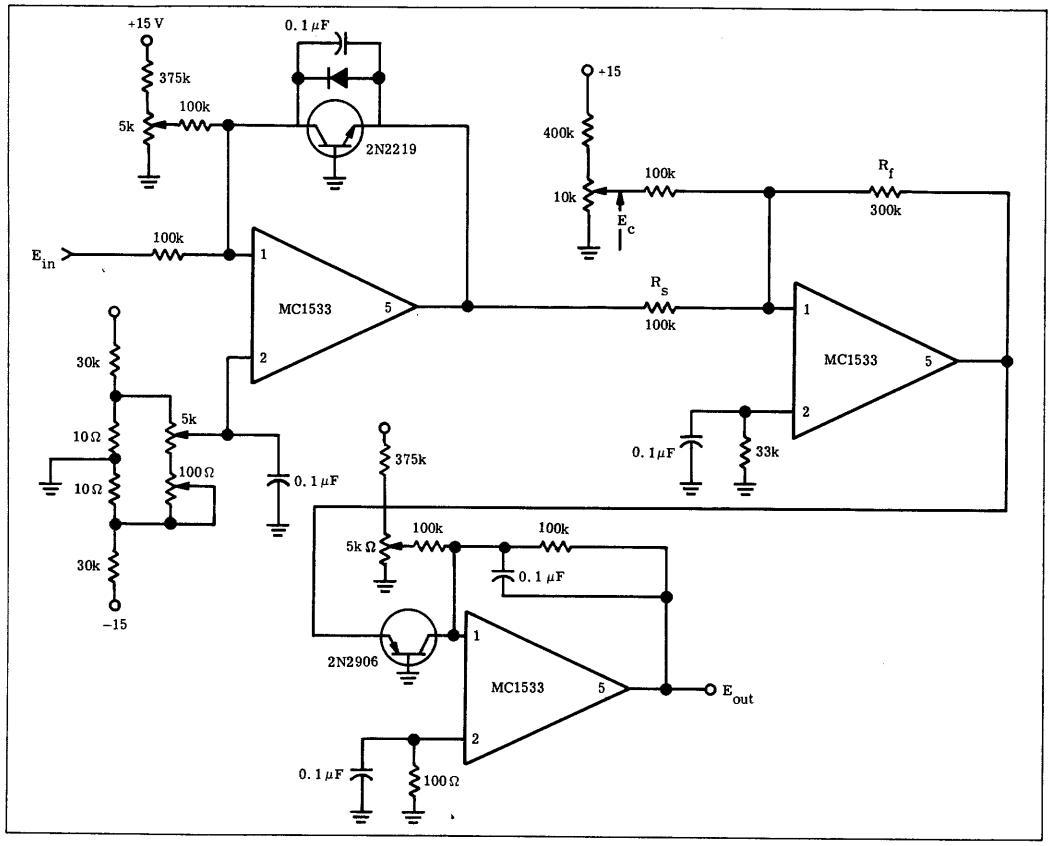


FIGURE 7 — CIRCUIT FOR COMPUTING $Z = X^n$

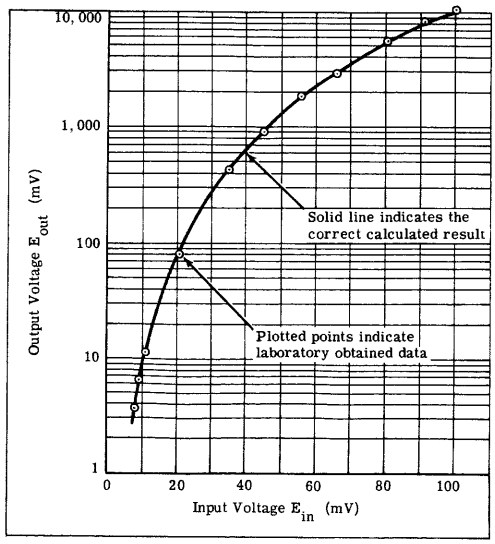


FIGURE 8 — OUTPUT VS. INPUT RESPONSE OF FIGURE 7 FOR a = 2

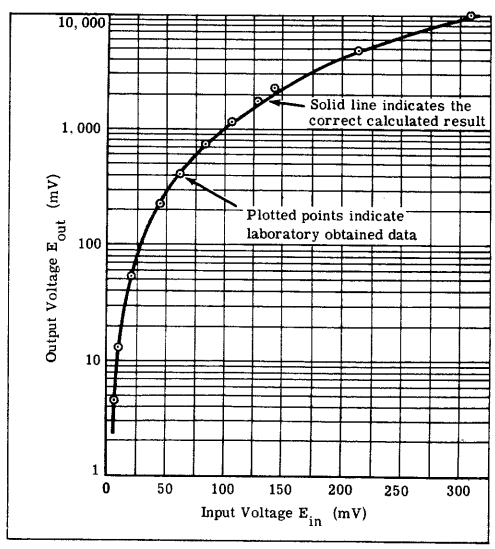


FIGURE 9 — OUTPUT VS. INPUT RESPONSE OF FIGURE 7 FOR a = 3

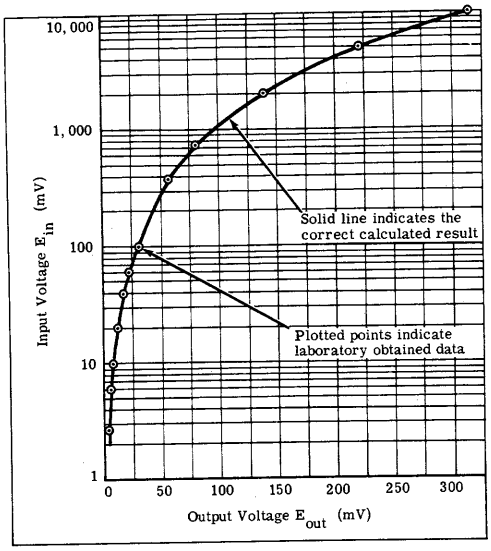


FIGURE 10 — OUTPUT VS. INPUT RESPONSE OF FIGURE 7 FOR a = ½

X Input #1	Y Input #2	Z Output	Calculated Z = XY	Difference	% Error
0.995 mV	13.8 mV	14.0 mV	13.72	0.28	2.04
	81 mV	82.4 mV	80.6	1.8	2.2
	297 mV	308 mV	295.5	12.5	4.2
	605 mV	695 mV	647	48	7.4
	1.042 V	1.110 V	1.038	0.072	6.9
	1.346 V	1.44 V	1.338	0.102	7.7
	2.98 V	2.99 V	2.965	0.025	0.8
	4.99 V	5.04 V	4.97	0.07	1.4
	10.11 V	10.34 V	10.06	0.28	2.8
	12.97 V	12.5 V	12.4	0.1	0.8
4.0 mV	14.44 mV	47.0 mV	57.8	0.8	1.4
	40.9 mV	154.9 mV	163.8	8.9	5.4
	102.3 mV	397 mV	410	13	3.2
	250 mV	1.02 V	1.00	0.02	2.0
	500 mV	2.05 V	2.00	0.05	2.5
	730 mV	3.08 V	2.95	0.13	4.4
	1.003 V	4.28 V	4.02	0.26	6.5
9.8 mV	7.45 mV	72.9 mV	73	0.1	0.14
	14.5 mV	143 mV	142	1	0.7
	40.9 mV	407 mV	401	6	1.5
	85 mV	837 mV	833	4	0.48
	199 mV	2.04 V	1.95	0.09	4.6
	250 mV	2.54 V	2.45	0.09	3.7
50 mV	14 mV	754 mV	700	54	7.7
	50 mV	2.56 V	2.5	0.06	2.4
	102 mV	5.31 V	5.10	0.21	4.1
	155 mV	7.94 V	7.75	0.19	2.5
	207 mV	10.38 V	10.35	0.03	0.29
	250 mV	12.54 V	12.50	0.04	0.32
100.3 mV	5.6 mV	598 mV	562	36	6.4
	14.5 mV	1.44 V	1.455	0.015	1.0
	50 mV	4.91 V	5.02	0.11	2.2
	102 mV	10.2 V	10.23	0.03	0.29
	120 mV	11.87 V	12.04	0.17	1.4
499 mV	5.07 mV	2.48 V	2.53	0.05	2.0
	10.08 mV	5.02 V	5.04	0.02	0.4
	20.15 mV	9.30 V	10.07	0.77	7.7

TABLE I — TABULATED RESULTS FROM MULTIPLIER CIRCUIT Z = XY

APPENDIX

The emitter current of Figure 1 is given by the expression

$$I_E = I_{ES}[e^{qV_E/kT} - 1] - \alpha_I I_{CS}[e^{qV_C/kT} - 1] \qquad (10)$$

where I_{ES} = emitter reverse saturation current
I_{CS} = collector reverse saturation current
α_I = inverted common base current gain

The collector current is given by

$$I_C = I_{CS}[e^{qV_C/kT} - 1] - \alpha_n I_{ES}[e^{qV_E/kT} - 1] \qquad (11)$$

where α_n = normal common base current gain.

Equations (1) and (2) must be modified to include those adverse components such as surface leakage currents and space charge generated currents. Since these currents generally behave as majority carriers in the base region, they are consequently not collected and do not appear at the collector junction. These currents may be included in equations (10) and (11) as follows:

$$I_E = I_{ES}[e^{qV_E/kT} - 1] - \alpha_I I_{CS}[e^{qV_C/kT} - 1] + \Sigma I_{ES_i}[e^{qV_E/kTm_i} - 1] \qquad (12)$$

$$I_C = I_{CS}[e^{qV_C/kT} - 1] - \alpha_n I_{ES}[e^{qV_E/kT} - 1] + \Sigma I_{CS_j}[e^{qV_C/kTm_j} - 1] \qquad (13)$$

If we now set $V_C = 0$ in equation (13) we find

$$I_C = -\alpha_n I_{ES}[e^{qV_E/kT} - 1] \qquad (14)$$

For $V_E > 100$ mV, equation (14) reduces to

$$I_C = -\alpha_n I_{ES}[e^{qV_E/kT}] \qquad (15)$$

REFERENCES

1. William L. Paterson: Multiplication and Logarithmic Conversion by Operational Amplifier-Transistor Circuits. The Review of Scientific Instruments. Vol. 34. No. 12, Dec. 1963.

2. Leo L. Wisseman: A High Voltage Monolithic Operational Amplifier. Integrated Circuits Application Note, AN-248.

AN-284
MDTL INTEGRATED CIRCUIT SHIFT REGISTERS

INTRODUCTION

A shift register is a group of serially connected flip-flops which may be used for temporary storage of information and/or the transforming of serial information to parallel form. By the addition of a parallel input feature to the shift register it is possible to reverse this transformation as well as increasing the adaptability of the shift register to certain logic operations. Other features which may be desired include end-around-shift, complementation, and shift-right, shift-left capabilities. Examples of shift registers with each of these features as well as a generic shift register which incorporates all the above capabilities will be discussed.

MDTL FLIP-FLOPS

The MDTL family contains a wide selection of binary elements which enables the systems designer to select a device with the particular characteristics which meets the needs of the application. In the interest of simplicity, the MC945/MC845 flip flop with direct clear as well as direct set inputs available is used as the basic building block for the shift registers discussed. Appendix "A" lists the modifications necessary to construct the shift registers using other binary elements within the MDTL family.

BASIC SHIFT REGISTERS

A shift right register is illustrated in Figure 1. In operation, the data present at the serial input terminals (D, $\overline{D}$) is shifted into the first flip flop at each negative transition of the clock pulse. Concurrently, the data stored in the (n-1)th flip flop is shifted into the nth flip flop and replaced by the data contained in the (n-2)th flip flop. Information shifted into the flip flop may be read out in a parallel manner by sensing the states of all the flip flops or may be collected serially at the output of the nth flip flop.

Some applications require retention of the stored data during serial readout. Shift registers with end-around-shift capabilities are frequently used for this purpose. The basic change necessary to provide this feature consists of connecting the output of the n^{th} stage to the serial data inputs of the 1^{st} stage. Provisions for data entry may take the form of a logic network which defeats the end-around-shift, thereby allowing serial data entry, or the use of direct set and direct clear in-

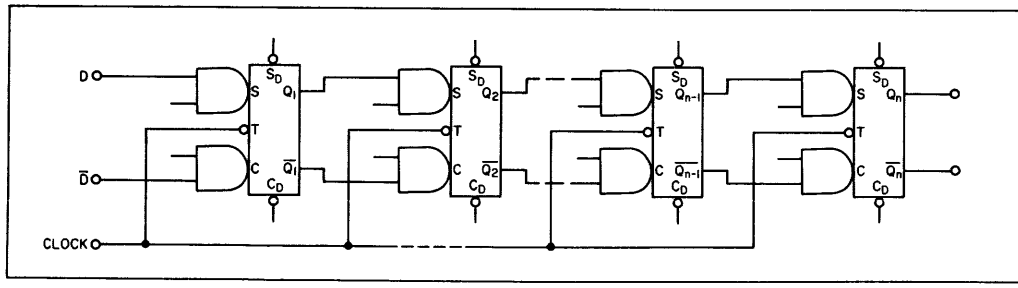


FIGURE 1 – SHIFT RIGHT REGISTER

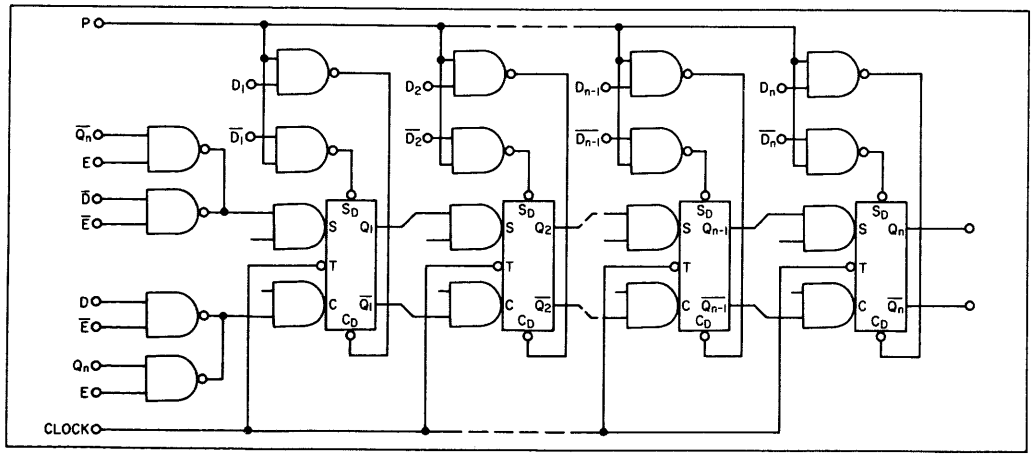


FIGURE 2 – END-AROUND-SHIFT RIGHT REGISTER WITH SERIAL AND PARALLEL DATA INPUTS

puts to allow parallel data entry. An end-around-shift register with provisions for either serial or parallel entry is shown in Figure 2.

Note that the parallel data inputs may be simplified if incorporated in a shift–right register in an application where serial input is not required and it is known that at least "n" negative transitions will occur prior to the arrival of a second parallel data entry command. For such an application, the synchronous set input to the first flip flop may be permanently held at ground potential. This eliminates the necessity for the gating associated with the C_D terminals.

The capability of shifting stored data either right or left is useful in some applications. Figure 3 illustrates a shift register with this capability. Note that the control signals (R and L) must be complementary to enable the shift register to function correctly. An exception to this may be noted in applications involving subtraction or multiplication where it may be desired to complement the information stored in the register. It can be seen that a negative transition of the clock pulse will toggle each flip flop if both R and L are low. If the complementation feature is desired, it is necessary to operate the flip flops in the J-K mode as shown ($\overline{Q}$ connected to S_2, Q connected to C_2). The second set of steering inputs may be left open if only the shift-left, shift-right capabilities are to be used.

It is sometimes desirable to incorporate the complementation feature in registers which do not require a bidirectional shift capability. Such a configuration is shown in Figure 4. The logic is such that a low level at the control point ($\overline{I}$) inhibits the normal logic levels at the inputs and results in toggling of each flip flop at a negative transition of the clock pulse.

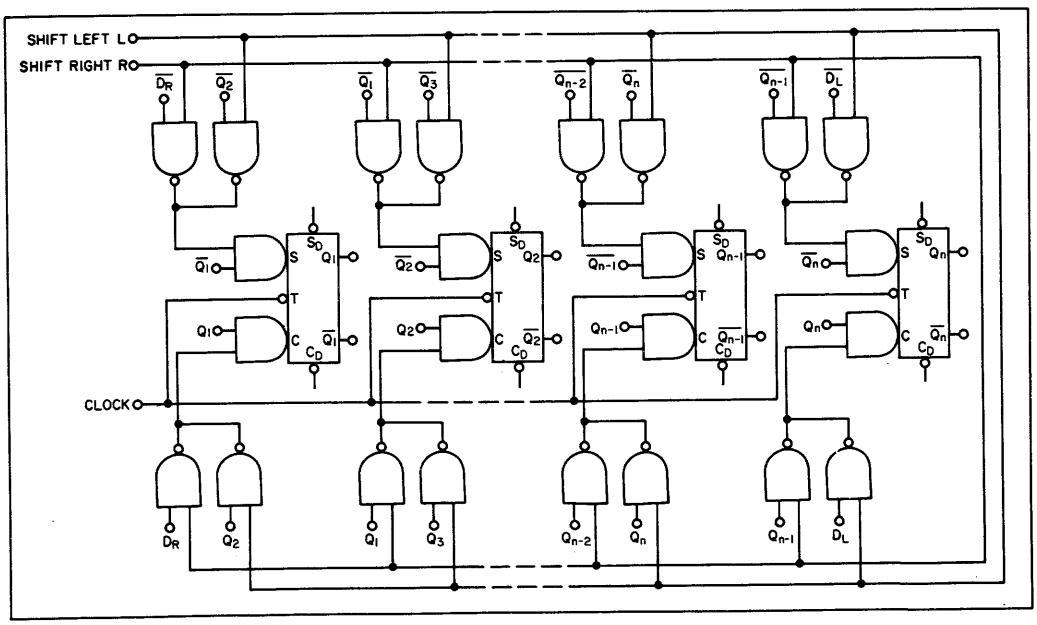


FIGURE 3 — SHIFT RIGHT-SHIFT LEFT REGISTER

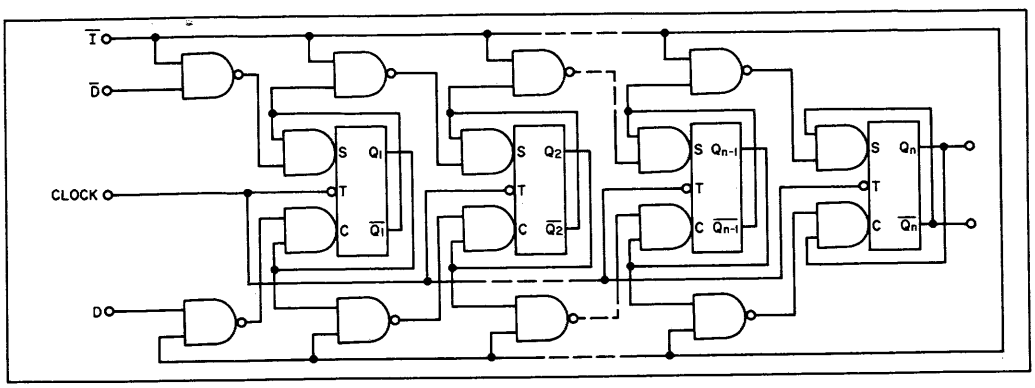


FIGURE 4 — SHIFT RIGHT REGISTER WITH COMPLEMENTATION FEATURE

The generic shift register of Figure 5 incorporates all the features described previously in a single register. Figure 6 tabulates the logic levels required at each control point to insure that the register performs the desired function.

It should be noted that the wired-collector gate configuration is used extensively in the generic shift register to minimize both "can count" and logic delays through the gates. This precludes the use of the buffer element (MC932/MC832) for any of the gates shown (exceptions are those controlling parallel data inputs, but the characteristics of the buffer are not required in these positions) as well as the gates providing the logic levels at the R and L control points. It may be advantageous to form the logic which controls the direction of shift in such a manner that points R and L may be held low simultaneously. This eliminates the need for the two gates used to inhibit the logic levels at the inputs of the flip-flops and also allows the use of buffer elements to control the R and L points. Each flip-flop toggles on the negative transition of the clock if R and L are low, provided that the parallel input control (P) is also low.

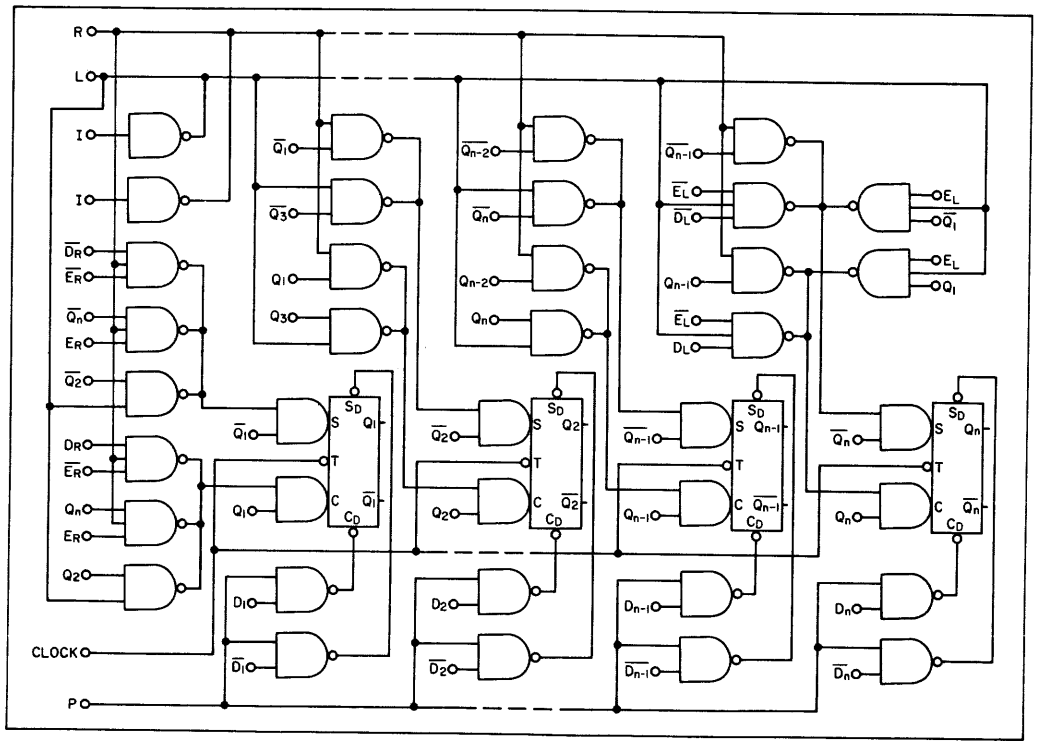


FIGURE 5 — GENERIC MDTL SHIFT REGISTER

COMMAND	R	L	E_L	$\overline{E}_L$	E_R	$\overline{E}_R$	I	P	D_R	$\overline{D}_R$	D_L	$\overline{D}_L$	CLOCK
SHIFT DATA RIGHT "R"	Hi	Lo	Lo	Lo	Lo	Lo	Lo	Lo	X	$\overline{X}$	ϕ	ϕ	Y
SHIFT DATA LEFT "L"	Lo	Hi	Lo	Lo	Lo	Lo	Lo	Lo	ϕ	ϕ	X	$\overline{X}$	Y
END-AROUND-SHIFT RIGHT "E_R"	Hi	Lo	Lo	Lo	Hi	Lo	Lo	Lo	ϕ	ϕ	ϕ	ϕ	Y
END-AROUND-SHIFT LEFT "E_L"	Lo	Hi	Hi	Lo	Lo	Lo	Lo	Lo	ϕ	ϕ	ϕ	ϕ	Y
INHIBIT AND COMPLEMENT "T"	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	Hi	Lo	ϕ	ϕ	ϕ	ϕ	Z
PARALLEL DATA ENTRY "P"	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	Hi	ϕ	ϕ	ϕ	ϕ	ϕ

EXPLANATION OF SYMBOLS

D_R, $\overline{D}_R$ = Data input for shift right
D_L, $\overline{D}_L$ = Data input for shift left
D_1, $\overline{D}_1$, ... D_n, $\overline{D}_n$ = Parallel input data
X, $\overline{X}$ = Serial input data
Hi ≥ V_{IH} Per MC945/MC845 specification
Lo ≤ V_{IL} Per MC945/MC845 specification
ϕ = Hi or Lo Level (Optional)
Y = Register shifted on each negative clock transition
Z = Register complemented on each negative clock transition

FIGURE 6 — GENERIC SHIFT REGISTER COMMANDS

TIMING CONSIDERATIONS

With any shift register more complex than a basic shift-right with serial inputs, it is necessary to insure that the command instructions have settled out prior to the ensuing clock pulse transition. As an example, consider that the generic shift register of Figure 5 is required to shift right for a period of time corresponding to "N" clock pulses and must shift left on all clock pulses following the Nth pulse. It is, therefore, mandatory that the information in the master of the flip flop be made to conform to a left-shift prior to the negative transition of the N+1 clock pulse. The direction of shift controls must, therefore, be complemented at least two gate delays prior to the negative transition of the N+1 clock pulse. (One of these gate delays is due to interstage gating while the second results from the cross-coupled gate configuration of the master flip-flop.) The complementation may safely occur up to 10 nanoseconds prior to the end of the Nth clock pulse. For operation at 8 MHz, the interval during which reversal of directional shift commands may be safely accomplished is 25 nanoseconds in duration.

Timing considerations for the end-around-shift commands are identical. An additional gate delay is necessary for the inhibit command for obvious reasons. The parallel input data command should be returned to a low level at least 80 nanoseconds prior to the first clock pulse which is required to shift the register. The minimum time interval between a given clock pulse and the initiation of the parallel input command is determined by the required read-out time which is dictated by systems requirements

CONCLUSIONS

Shift registers with capabilities ranging from a basic shift-right configuration to a generic shift register incorporating parallel as well as serial inputs, shift-right, shift-left, end-around-shift, and complementation features have been discussed. The basic building block utilized was the MC945/MC845 flip-flop with both direct set and direct clear inputs available and it was assumed that operating frequency was such that the additional delay introduced by the necessary logic would not impair operation of the registers. Modifications necessary to permit the use of other flip-flops within the MDTL family and operating frequency limitations are discussed in the appendix.

APPENDIX A – MODIFICATIONS NECESSARY TO PERMIT USE OF ANY MDTL FLIP-FLOP IN SHIFT REGISTERS

INTRODUCTION

Including package and temperature range options, a total of 32 types of flip-flops is offered in the MDTL family. Due to pin limitations, individual direct clear inputs are not always available which may complicate parallel data input provisions. In addition, the truth table of the MC950/MC850 binary element is such that extensive revision of the preceding configurations is necessary when this device is used, particularly if the complementation feature is desired.

Some of the important characteristics of the MDTL flip-flops are tabulated in Figure A-1. More information on these devices may be obtained from AN-283 "Using MDTL I/C Flip-Flops" and from current MDTL data brochures.

MC931/MC831 FLIP-FLOPS

This device differs from the MC945/MC845 type in that outputs are not buffered and the direct inputs (S_D and C_D) affect only the slave portion of the flip-flop. Due to the latter characteristic, direct inputs should be applied to the MC931/MC831 only when the clock pulse is high. It should also be noted that the slave will switch to the state stored in the master portion when the clock returns to a zero level. In general, the MC945/MC845 flip-flop is preferred when the application calls for the parallel input feature and either the Unibloc or the ceramic flat package is to be used. Since the MC931/MC831 may be "cleared" by the simple expedient of forcing the true output to a low state (observing the requirement of a high level on the clock pulse) while no provision for direct clearing of the MC945G/MC845G (TO-100

DEVICE TYPE	OUTPUT PULL-UP	DIRECT CLEAR	FLIP-FLOPS PER PACKAGE	TYPICAL MAX. TOGGLE FREQ. (MHz)
MC931G/MC831G	6 kΩ	None*	1	10
MC945G/MC845G	6 kΩ	None	1	10
MC948G/MC848G	2 kΩ	None	1	12
MC950G/MC850G	Active	Yes	1	40
MC931F/MC831F/MC831P	6 kΩ	Yes	1	10
MC945F/MC845F/MC845P	6 kΩ	Yes	1	10
MC948F/MC848F/MC848P	2 kΩ	Yes	1	12
MC950F/MC850F/MC850P	Active	Yes	1	40
MC952F/MC852F/MC852P	6 kΩ	Common**	2	10
MC953F/MC853F/MC853P	6 kΩ	None	2	10
MC955F/MC855F/MC855P	2 kΩ	Common**	2	12
MC956F/MC856F/MC856P	2 kΩ	None	2	12

* Outputs are not buffered – direct clear is possible.
** These types also have common clock input.

FIGURE A-1 – MDTL FLIP-FLOP CHARACTERISTICS

package) is available, the choice between these flip-flops frequently becomes a matter of designer's preference. With the exception of parallel entry, the MC931/MC831 device types may be used in the configurations shown in the main portion of this report with no modifications necessary.

MC948/MC848 FLIP-FLOPS

There is no difference in the truth table or operation of the direct inputs between this device and the MC945/MC845 flip-flop. The shift registers described previously will operate with this type of flip-flop with no modifications, provided that Unibloc or ceramic flat packages are used.

FLIP-FLOPS IN TO-100 PACKAGES

The direct clear input is not available with either the MC945/MC845 or the MC948/MC848 when these devices are housed in the ten-lead TO-100 package. This complicates the parallel input of data in situations where the flip-flops are not cleared through normal operation of the register. One means of circumventing this problem is shown in Figure A-2. The method is quite similar to that used for complementation with the exception that a high level on the synchronous clear inputs is maintained and the gates controlling the direct set inputs are enabled. Since the synchronous inputs are overridden by the direct set, clocking the register results in all flip-flops attaining the states dictated by the parallel input data. Although the configuration appears relatively complex, the "can count" is only two inverters per stage greater than that normally required for parallel data input with flip-flops which have direct clear inputs available.

DUAL J-K FLIP-FLOPS

Monolithic dual J-K flip-flops have recently been introduced in the MDTL family. In general, the MC953/MC853 and the MC956/MC856 device types should be used in shift register applications only if parallel entry of data is not required or if the application is such that the register is cleared during normal operation. These devices have separate clock inputs and no provision for direct clear while the MC952/MC852 and the MC955/MC855 have a common clock input and a common direct clear. The latter feature is attractive for parallel entry while the common clock feature reduces the number of external connections necessary.

Figure A-3 illustrates a method of entering data into the register in parallel form. A monostable multivibrator is utilized and a restriction is placed on the clock pulse which requires that no negative transition should occur during the parallel data entry interval. It is also necessary to insure that the parallel data command pulse has a width of at least 200 nanoseconds. Note that the modification results in a savings in "can-count" for registers with greater than 4-bit capacity and does not require complementary data inputs. The method may, therefore, be preferred to that of Figure 2 in some applications which use the MC945/MC845 flip flops with direct clear inputs.

MC950/MC850 FLIP-FLOP

The truth table of this device differs significantly from those presented previously. Since no combination of fixed dc inputs causes the device to "toggle" on each clock pulse, it is necessary to sense the level of the output of each flip-flop in order to achieve complementation. A method of using the MC950/MC850 in a shift right register is shown in Figure A-4 and the logic necessary to implement the complementation feature is illustrated in Figure A-5. A generic shift register using the MC950/

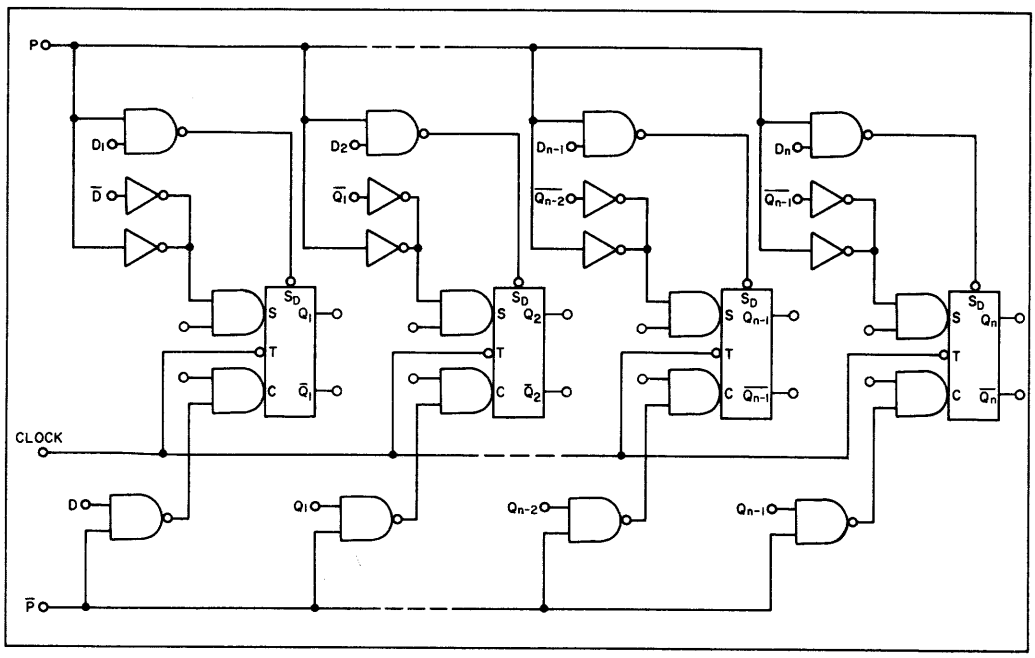


FIGURE A-2 — SHIFT RIGHT REGISTER WITH PARALLEL DATA INPUT PROVISIONS

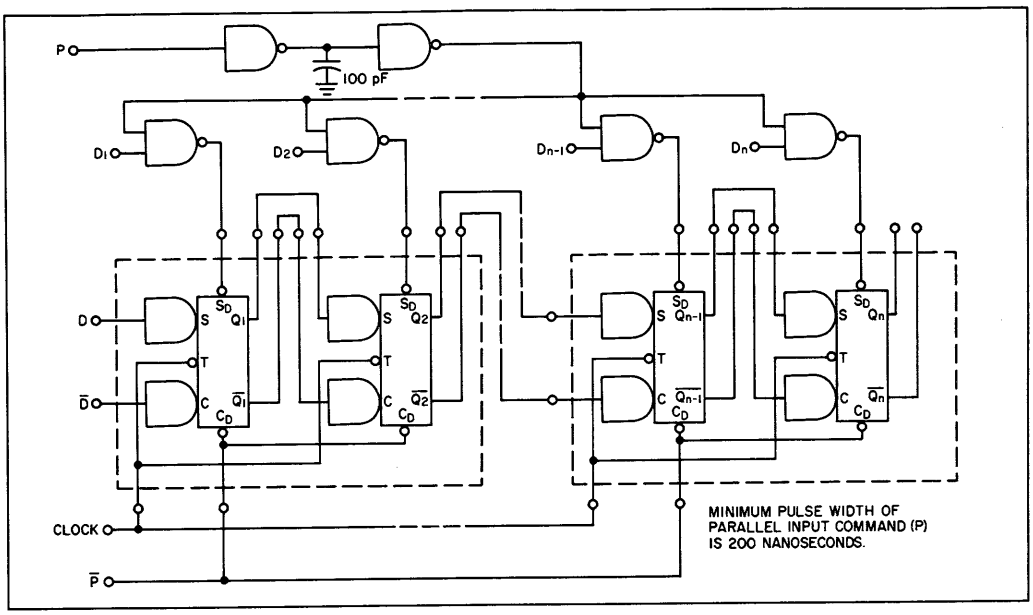


FIGURE A-3 – SHIFT RIGHT REGISTER WITH PARALLEL DATA INPUTS USING COMMON DIRECT CLEAR

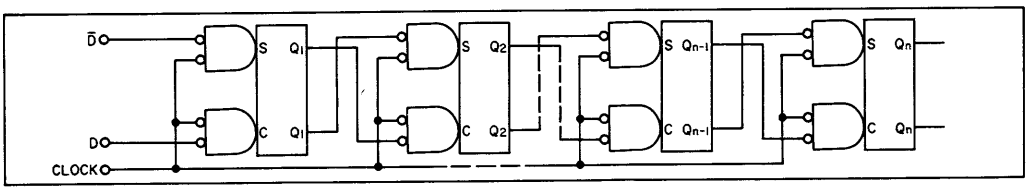


FIGURE A-4 – SHIFT RIGHT REGISTER USING MC950/MC850 FLIP-FLOPS

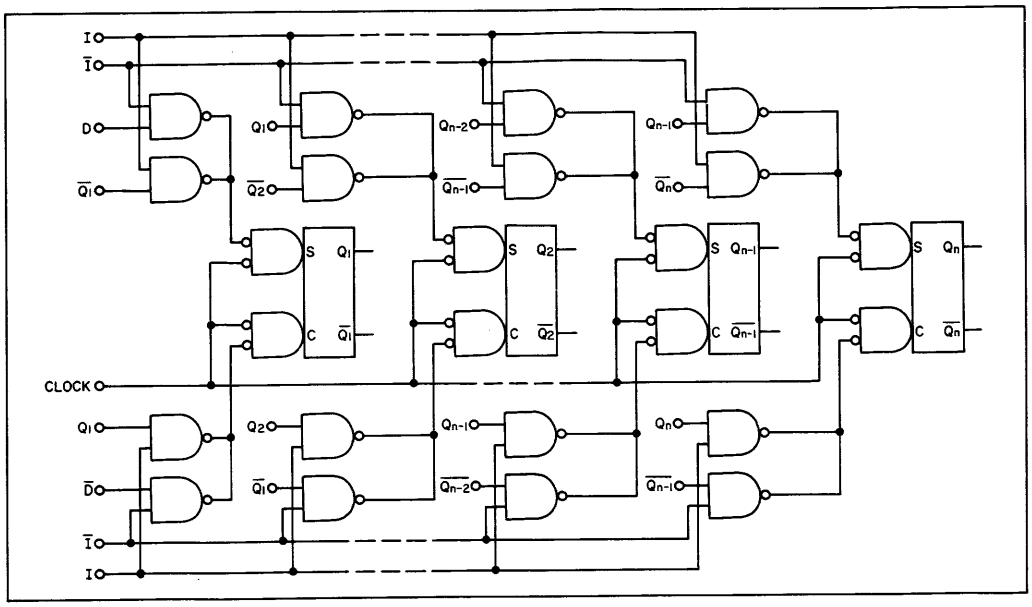


FIGURE A-5 – SHIFT RIGHT REGISTER WITH COMPLEMENT CAPABILITIES USING MC950/MC850 FLIP-FLOPS

MC850 is shown in Figure A-6. The register responds to the commands tabulated in Figure 6 of the main portion of this report. Note that both direct set and direct clear inputs are available on the MC950/MC850 regardless of package option, so provisions for parallel entry are easily implemented.

MAXIMUM OPERATING FREQUENCY

The maximum operating frequency of the basic shift register is determined by the capabilities of the flip-flops used and closely approximates the maximum toggle frequency of the flip-flops. An exception to this is sometimes noted when the MC950/MC850 is used. The clock drive mechanism frequently determines the maximum operating frequency for these devices due to the capacitance associated with the clock inputs.

Provisions for other features which necessitate interstage gating tend to reduce the maximum operating frequency. It should be noted, however, that no more than one level of interstage gating is required for any of the registers previously described. The maximum operating frequency of any of these registers with minimum output loading and a 50% clock duty cycle is typically 75% of the maximum toggle frequency provided that direct coupled flip flops are used. Optimum results are obtained by reducing the clock duty cycle to 35% and minimizing capacitive loading of the outputs while increasing fan-out of all outputs.

Due to the high speed capabilities of the MC950/MC850, shift registers utilizing this component together with interstage gating exhibit a typical maximum operating frequency of 20 MHz. In general, the register will still be limited by the clock drive mechanism even when interstage gating is used

SUMMARY

Parallel entry of data into registers which utilize flip-flops with restrictions on direct inputs and the complementation feature when utilizing the MC950/MC850 device require techniques which differ from those illustrated in the main portion of this report. Modifications can be made to allow the use of any MDTL flip-flop in the implementation of the previously described shift register features.

Examination of the more complex registers reveals that the maximum operating frequency is reduced by 25 to 50% of the maximum toggle frequency of the flip flop depending upon the type of binary element used.

ACKNOWLEDGEMENTS The author would like to acknowledge the efforts of Frank Kramer whose laboratory efforts were essential in the preparation of this report.

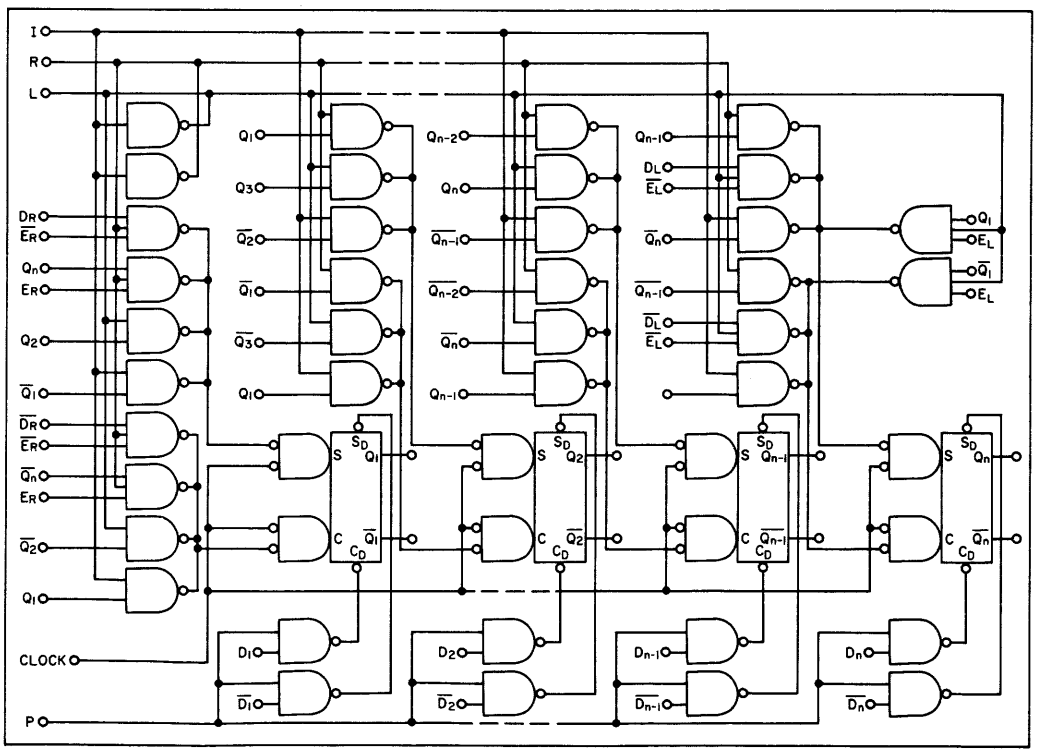


FIGURE A-6 — GENERIC MDTL SHIFT REGISTER USING MC950/MC850 FLIP-FLOPS

AN-298
NOISE IMMUNITY WITH HIGH THRESHOLD LOGIC

INTRODUCTION

The following material discusses general noise considerations and compares the noise immunity of the new high threshold devices with standard saturated logic devices. Some basic illustrations are provided which indicate the flexibility of usage that may be achieved with the MHTL family.

Typical characteristics of the MHTL family are:

Single 15-volt power supply
7.5V switching threshold
6 volt signal line noise margins
13 volt logic swing
30 mW gate power dissipation
85 ns gate propagation delay
4 MHz flip-flop toggle frequency
-30^{o} to $+75^{o}C$ operating temperature range

NOISE INJECTION

Electrical noise has always been a source of trouble for electronic systems whether they are composed of discrete components or integrated circuits. Origination of electrical noise can be from many sources both external to the electronic system under consideration and self-induced noise by the circuitry itself. Examples of external sources would be switching of inductive circuits, rotating machinery, and various electronic control circuits as depicted in Figure 1.

Internal noise may be caused by the switching of one circuit affecting the state of another circuit (Figure 2). The amount of noise induced into the passive circuit is a function of the voltage swing, current change, and the switching speed of the active circuit and the inductive and capacitive coupling between the two circuits. Coupling may also take place by the use of a common path for the active and passive devices such as a power supply or ground lead. Noise from external sources is induced into the system under similar conditions. Generally, noise is a random combination of many sources and as such is extremely hard to analyze. The net result, however, is that induced positive and negative spikes relative to the quiescent condition of a line may cause erroneous information to be absorbed into the system. This condition must be avoided if proper operation is to be achieved by the unit.

NOISE REDUCTION TECHNIQUES

Several schemes have commonly been employed to reduce the effect of electrical noise on a system composed of integrated circuits. Physical shielding of the integrated circuits and its associated wiring prevents external electromagnetic radiation from inducing noise into the circuitry. Special buffering circuits may be employed between the electronic circuits and signal leads dependent on external sources. These signal leads in many cases require special routing considerations and special shielding. Extra filtering of the power supply leads may be required to reduce the noise introduced by this route. Internal noise generation may require special spacing and routing considerations as well as maintaining short lead lengths. In some cases the power supply may need to be by-passed at several points on a board.

The amount of additional components and equipment necessary to protect integrated circuits from electrical noise can increase to a point where it is economically desirable to seek other methods of operation to obtain the desired results. It would be advantageous to have an integrated circuit family with a high degree of inherent noise immunity for economical construction of an electronic system. This will minimize the amount of special care needed for proper circuit operation in areas with a high electrical noise environment.

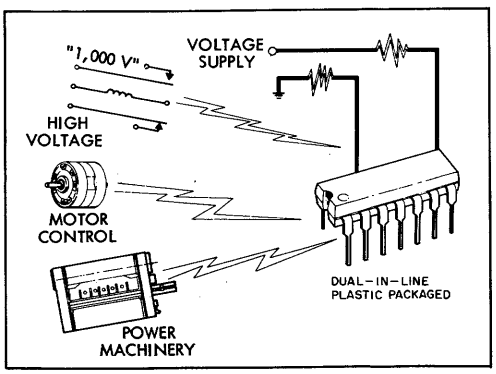


FIGURE 1 - EXTERNAL NOISE GENERATOR

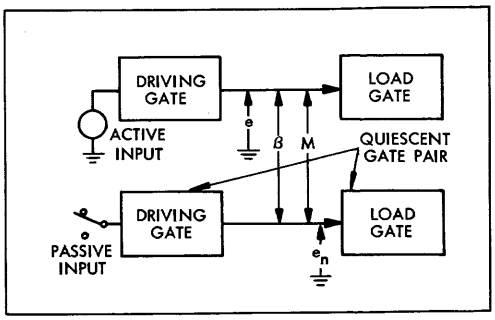


FIGURE 2 - INTERNAL NOISE GENERATOR

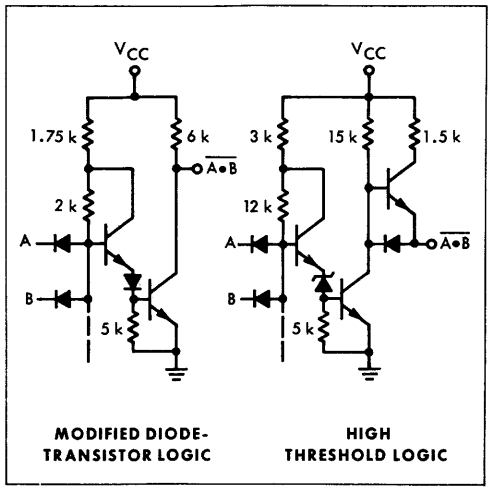


FIGURE 3 - GATE COMPARISONS

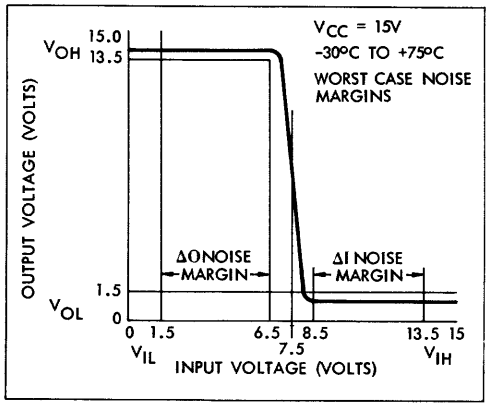


FIGURE 4 - TYPICAL HIGH THRESHOLD TRANSFER CURVE

A HIGH THRESHOLD LOGIC

The most popular families of integrated circuits in use today exhibit a comparatively high speed of operation and have typical threshold values between 0.7 and 1.5 volts. A new type of logic family, High Threshold Logic (MHTL), has been developed that closely resembles the modified diode-transistor logic family (Figure 3). The basic difference is that the high threshold logic uses a reverse biased base-emitter junction operating in the avalanche breakdown mode as a threshold element. As can be seen in the figure, the logical NAND function is provided by each gate. The inputs of the modified diode-transistor gate must exceed two forward base emitter drops or typically 1.5 volts before base current is applied to the output inverting transistor providing the "0" state. In the high threshold device, however, the inputs must exceed the reverse biased base-emitter breakdown plus one forward V_{BE} drop or typically 7.5 volts before the output inverting transistor turns on. Since the other logic families exhibit a threshold level similar to or less than the modified diode-transistor device, a considerable increase in threshold level has been obtained with the new configuration. The higher threshold incorporated in the devices demands a higher power supply and a nominal 15 volts is used. The transfer curve for the basic gate operating with a 15-volt supply is shown in Figure 4. It can be seen that for any input signal up to 6.5 volts, the output will remain in the high state or above 13.5 volts. A 2-volt margin, from 6.5 volts to 8.5 volts, is used for the transition region and guards against variations between manufacturing lots and temperature effects from -30°C to +75°C. At 8.5 volts on the input, the output is in the low state or less than 1.5 volts and remains there for any further increase of the input voltage. This diagram indicates worst case noise margins of 5 volts in both the high and low states for a V_{CC} of 15 volts while typical values are about 6 volts.

LOGIC FAMILY COMPARISONS

BASIC OPERATING CHARACTERISTICS

A comparison of basic operating characteristics for high threshold logic with the standard forms of logic is provided in the table shown in Figure 5. The values given are typical for an ambient temperature of 25°C and indicate relative characteristics between the different families. One difference that should be noted is that the high threshold logic is slower than the other families. This characteristic aids in the rejection of noise and will be illustrated in following figures.

	V_{CC} (VOLTS)	GATE POWER DISSIPATION (mW)	PROPAGATION DELAY (ns)	DC NOISE IMMUNITY (VOLTS)	LOGIC SWING (VOLTS)
RESISTOR TRANSISTOR LOGIC	3.6	12	25	0.5	1.0
MODIFIED DIODE TRANSISTOR LOGIC	5.0	8	30	1.2	4.5
TRANSISTOR – TRANSISTOR LOGIC	5.0	15	10	1.2	3.5
HIGH THRESHOLD LOGIC	15	30	85	6	13

FIGURE 5 - BASIC OPERATING CHARACTERISTICS

SIGNAL LINE NOISE IMMUNITY

Measurements were made on the different logic families to determine the signal line noise immunity not only from a voltage margin consideration, but also from a pulse width and energy point of view as well. Figure 6-A illustrates a test set-up to measure immunity of the gate to noise on the signal lead. Positive going noise was injected on the signal lead for this set-up with the output of gate #1 in the low state. When sufficient noise was injected, the flip-flop driven by the second gate would begin to toggle indicating the effect of the injected noise. This type of test not only measures the power needed for disturbance, but also the pulse width of noise necessary to propagate through and cause faulty operation of a driven device. A series of values of voltage level and injected current to cause disturbance were taken versus the pulse width at each corresponding point. Current readings were obtained as a voltage drop across the pulse generator resistor. The pulse generator offset voltage was adjusted to eliminate the effect of its quiescent condition on gate levels. Voltage threshold as a function of pulse width is plotted in Figure 6-B. The energy of each logic family is plotted in bar graph form at the knee of each respect-

ive curve in Figure 6-C. For narrower pulse widths, the energy necessary to cause a disturbance increases. The high energy value obtained for MHTL is a result of the high threshold voltage and low gate impedance in this state.

Figure 7-A illustrates a similar test except that gate #1 is in the high state and negative going noise is injected on the signal lead. Similar results are shown in Figure 7-B and C.

GROUND LINE IMMUNITY

Tests were made on the devices to provide information on the immunity to noise injected on the ground terminal. The test configuration is shown in the first part of Figure 8. A plot of voltage threshold versus pulse width is given in Figure 8-B for the worst case condition found for the particular family dependent on the input state. The energy relationships are provided in Figure 8-C.

POWER SUPPLY IMMUNITY

A similar test was made for noise injected on the power supply lead. In this case, the flip-flop will only be affected by negative going noise and the results indicate worst case conditions for the particular family dependent on the state of the first gate. The test configuration and results are given in Figure 9.

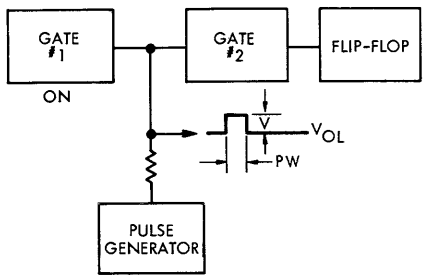


FIGURE 6A

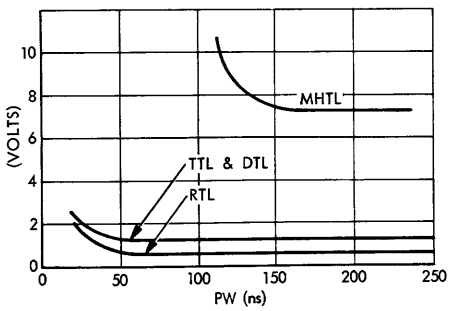


FIGURE 6B

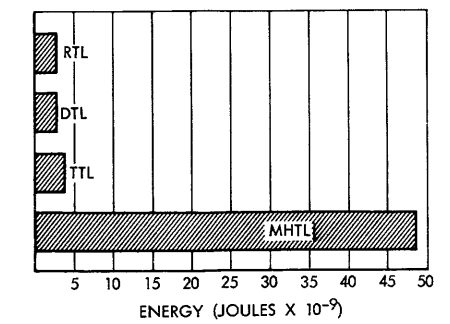


FIGURE 6C

SIGNAL LINE NOISE IMMUNITY

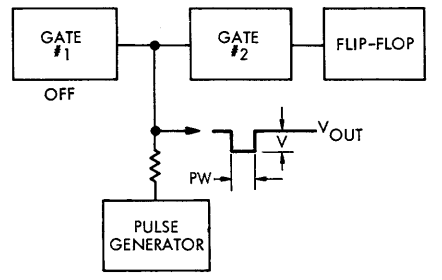


FIGURE 7A

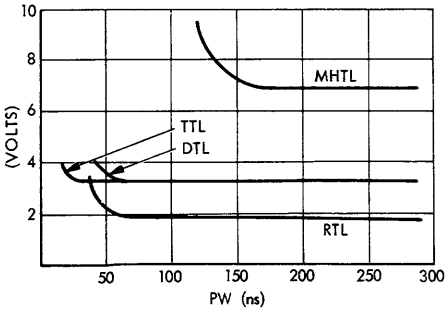


FIGURE 7B

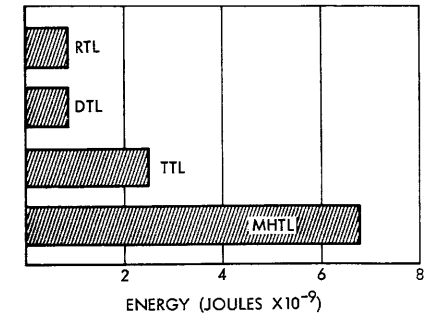


FIGURE 7C

SIGNAL LINE NOISE IMMUNITY

The preceding tests were taken with a fanout of one on the first gate and a fanout of the flip-flop only on the second gate. This condition tends to be an advantage for the RTL family and the results are somewhat optimistic in this case.

These comparisons indicate that the high threshold logic has an appreciable inherent advantage over the standard families of integrated circuits. In addition, the higher threshold level present in these devices provides a considerable margin that may be used in conjunction with simplified buffering networks to filter out excessive noise spikes under very extreme conditions.

USAGE

The preceding discussion has generally referred to the basic high threshold gate circuit. Additional components are available, however, which exhibit the same noise immunity characteristics obtained by reverse biased base-emitter breakdown action. The availability of other units such as line drivers, J-K flip-flops, R-S flip-flops, and monostables will allow the designer to construct a complete logic system with a high degree of noise immunity throughout.

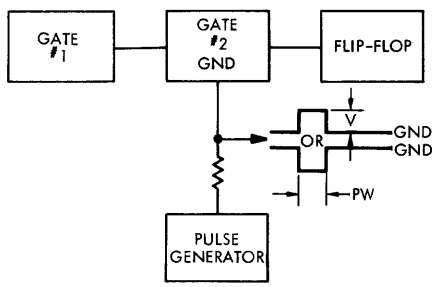


FIGURE 8A

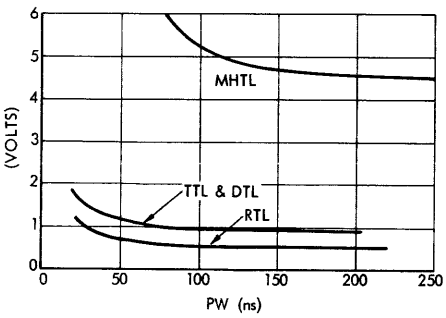


FIGURE 8B

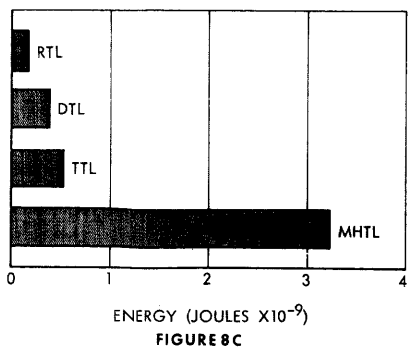


FIGURE 8C

GROUND LINE NOISE IMMUNITY

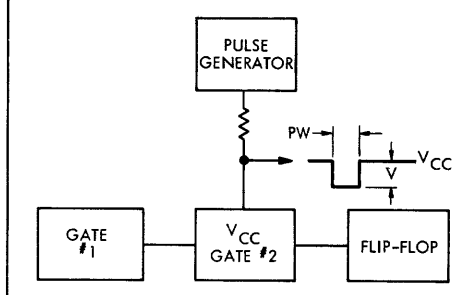


FIGURE 9A

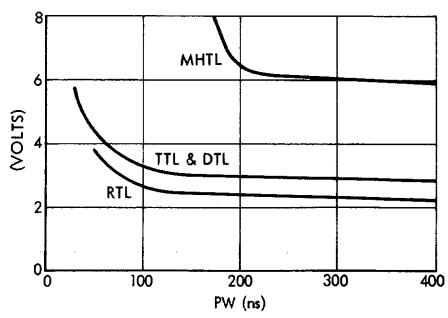


FIGURE 9B

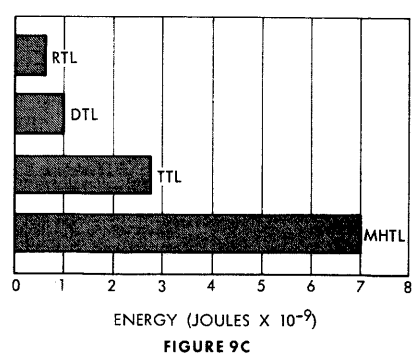


FIGURE 9C

POWER SUPPLY NOISE IMMUNITY

Situations arise where it would be advantageous to work into a system that operates at a higher speed than is obtainable by the high threshold devices. Translation between high threshold logic and standard logic families can be accomplished to allow the usage of high threshold devices as peripheral circuitry to a higher speed logic system. Thus, the high threshold devices may be operated in the noise environments and translation may take place into the lower threshold and higher speed system at the appropriate locations as indicated in Figure 10.

The higher supply voltage used in this logic family provides for the convenient interfacing with many discrete components. For example (Figure 11), the input may be controlled by a photo transistor so that illumination will cause the gate output to be high and darkness will provide a low output state. The output of the gate might feed into a logic system such that after a specific count would operate a relay. If a line driver unit were used as the output element, a 35mA, 15-volt relay could be employed. Other components such as lamps, SCRs, or transistors may also be driven directly at the output. As can be seen, the uses of the high threshold devices are many and varied.

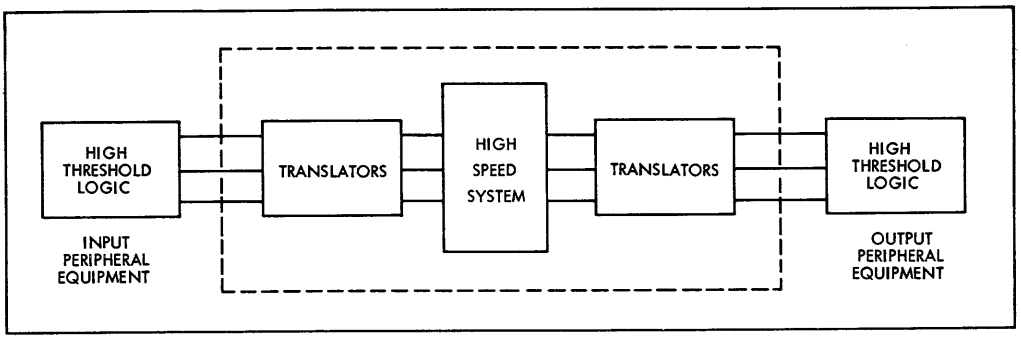


FIGURE 10 - OPERATING AS PERIPHERAL COMPONENTS

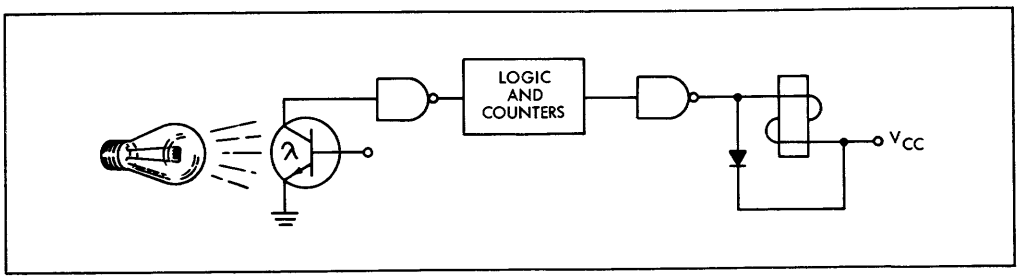


FIGURE 11 - OPERATING WITH DISCRETE COMPONENTS

SUMMARY

The new high threshold logic provides an integrated circuit logic family with a greater inherent immunity to electrical noise than is available with standard logic families. This logic family is ideal for situations where a large degree of electrical noise exists and where it is desirable to minimize the additional precautions necessary to reduce the effects of electrical noise. Input and output compatibility of the units with discrete components opens the door for a wide range of device employment.

AN-403
SINGLE POWER SUPPLY OPERATION OF I/C OPERATIONAL AMPLIFIERS

INTRODUCTION

The operational amplifier is gaining wide recognition as a versatile, predictable and economical system building block. It is being used in the more common configurations such as scaling, summing, phase shifting, etc., as well as in special design configurations such as modulators, demodulators, and multiplexers.

The I/C operational amplifier is generally designed to operate from symmetrical positive and negative power supply voltages with a resultant frequency response extending down to dc. In some system applications, the circuit designer requires many of the desirable ac characteristics of the operational amplifier, but does not have both positive and negative power supplies available nor require the dc response capability.

This application note describes a technique that can be used with the Motorola family of operational amplifiers to permit operation from a single power supply with a minimum of design compromise. General considerations as well as those falling specifically under ac and dc considerations are discussed to permit maximum design versatility with a minimum of design problems.

It should be noted that the information discussed in this application note applies not only to the MC1530, MC1531, MC1533, and MC1709 series of operational amplifiers, but also to the MC1430, MC1431, MC1433, and MC1709C restricted temperature range devices of the series.

GENERAL CONSIDERATIONS

The same maximum device ratings that are published on the data sheet are applicable to the operational amplifiers when operating from a single polarity power supply and must be observed for normal operation.

Power supply decoupling capacitors are prominent on all of the configurations to be discussed. The importance of the decoupling capacitors, whether with single supply operation or dual supply operation, cannot be overemphasized. These operational amplifiers are high gain, high frequency devices and stray signals coupled back through the power supply can create instability problems. The decoupling capacitors should be placed physically as close as possible to the device to minimize the effects of the inductance of the power supply leads.

Finally, the circuit interconnections should be laid out such that the lead lengths to the summing point are short to minimize pickup and such that ground loops are avoided.

DC CONSIDERATIONS

There are three basic techniques readily apparent for setting up single polarity power supply operation of the I/C operational amplifiers:

1. Separate power supplies.
2. Split zeners from a single supply voltage.
3. Divider networks from a single supply voltage.

The split zener method was chosen from these to be most representative of what designers would employ and will be used in the illustrations.

Other techniques and modifications will be also apparent to many designers and will no doubt be useful if the basic rules outlined below are followed.

The first area of concern in setting up for single supply operation is to maintain the dc voltage levels between particular circuit nodes. The Motorola MC1530/1531 operational amplifier has three reference levels which, when operating from dual supplies, are +V, ground, and -V (e.g. +6 V, 0, -6 V). Thus for single supply operation these reference levels can be maintained by using ++V, +V, and ground (e.g. +12 V, +6 V, 0), where ++V represents a voltage level a factor of two higher than +V. This is illustrated in Figure 1(d) where the MC1530/1531 is connected in the split zener biasing mode. Note how the appropriate device terminals are biased up to the proper levels. Pin 4, the negative terminal, is set at ground; pin 3, the ground terminal, is set at one-half the device zener supply voltage; pin 6, the positive terminal, is set at the total device zener supply voltage. In addition, the differential input terminals, pins 1 and 2, which are normally at ground potential in the dual supply mode, must also now be biased up to one-half the device zener supply voltage.

With the input terminals of the device biased up to one-half the zener supply voltage, the output terminal, pin 5, also will be at one-half the zener voltage plus or minus an offset voltage error due to input offset voltage, input offset current, and impedance unbalance. Normally, these error voltages are or can be maintained at low levels such that the resultant dynamic output range capability of the device is not degraded appreciably.

To minimize offset errors due to unequal voltage drops caused by the input bias currents across unequal resistances, it is recommended that the magnitude of isolation offset resistance R_4 be equal to the parallel combination of R_2 and R_3.[1]

As with any operational amplifier, the deviation between the absolute zener levels will also contribute to an error in the output voltage level. However, due to the excellent matching characteristics of monolithic device parameters, this error is in the range of 50-100 μV per volt deviation of zener level and will generally be inconsequential when compared to the offset errors discussed above even when using higher closed loop gains.

Figures 2 and 3 illustrate the split zener biasing mode as applicable to the MC1533 and MC1709. Note that due to the absence of a ground reference terminal in the normal mode of operation, only the input device terminals are set at one-half the zener supply voltage. Otherwise, the dc biasing scheme is identical to that for the MC1530/1531.

In this discussion a positive power supply was assumed. There is no reason why a negative power supply could not be employed as long as the maximum ratings and node voltage levels of the devices are maintained.

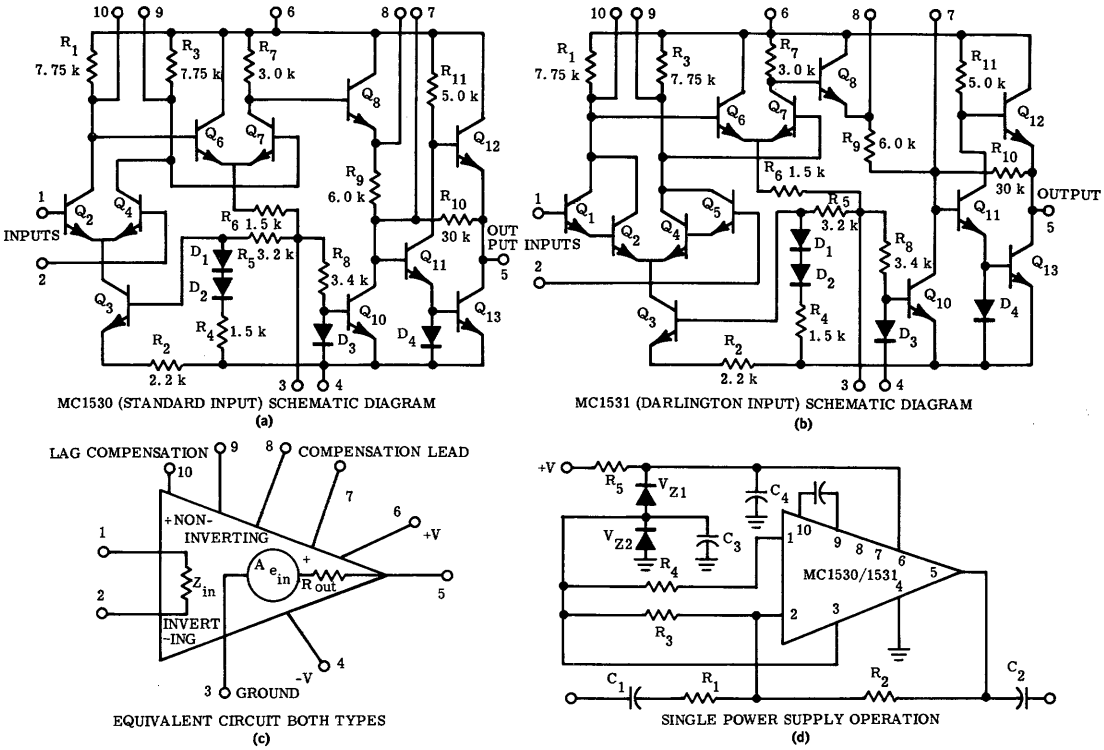


FIGURE 1 — SINGLE POWER SUPPLY OPERATION OF MC1530 AND MC1531

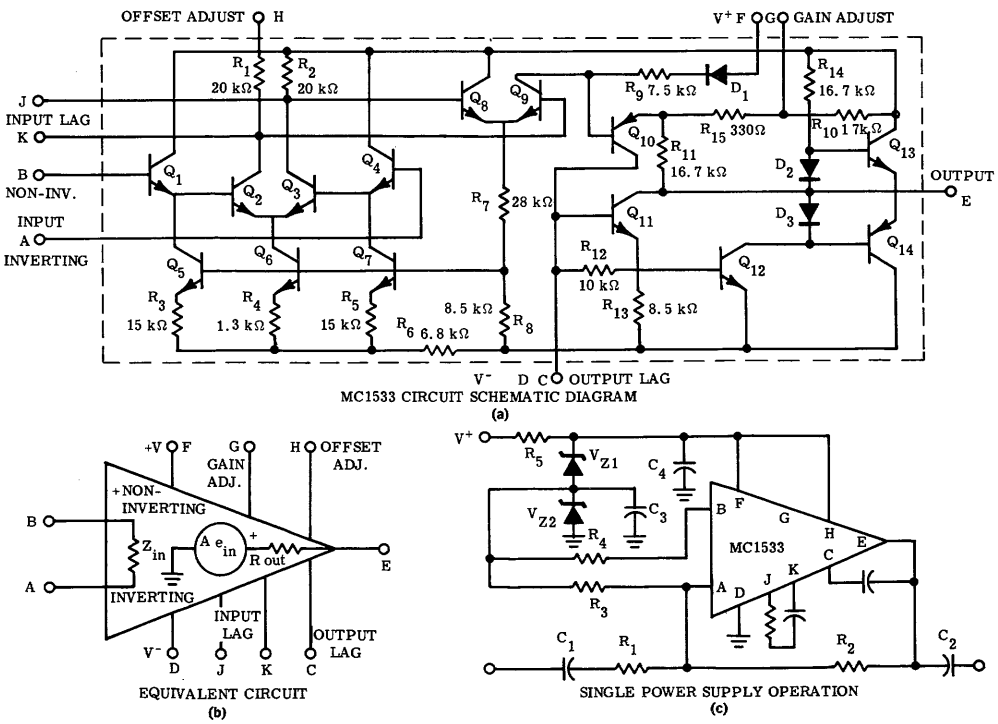
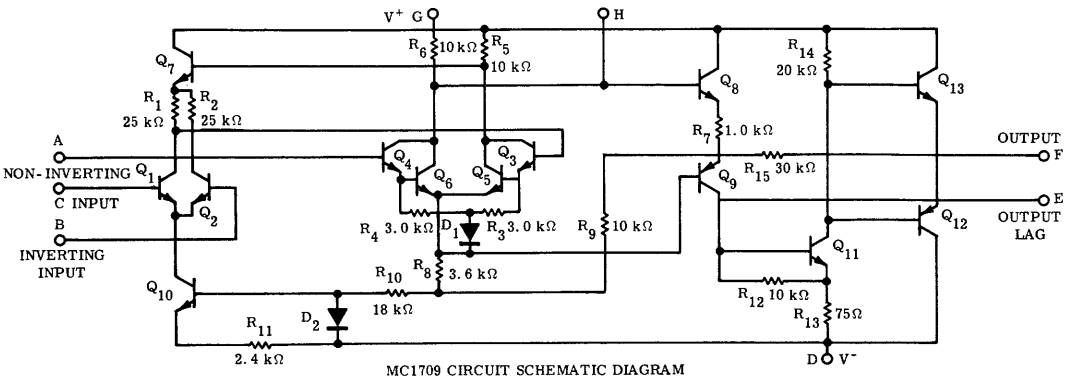
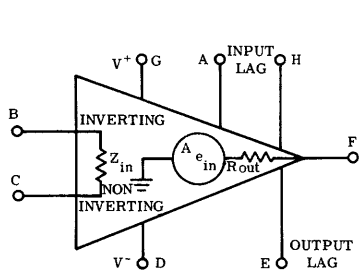


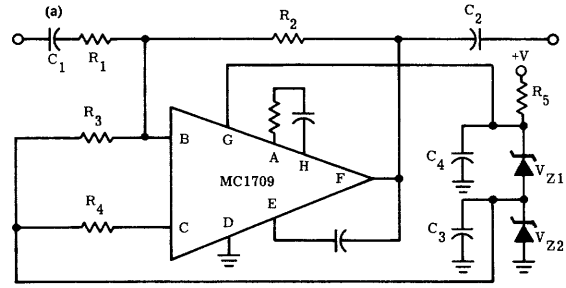
FIGURE 2 — SINGLE POWER SUPPLY OPERATION OF MC1533



MC1709 CIRCUIT SCHEMATIC DIAGRAM



EQUIVALENT CIRCUIT
(b)



SINGLE POWER SUPPLY OPERATION
(c)

FIGURE 3 – SINGLE POWER SUPPLY OPERATION OF MC1709

AC CONSIDERATIONS

From an ac standpoint with only a few exceptions, the basic circuit functions identically to that of one using dual power supplies. The normal frequency compensation techniques required for stability of each device[2, 3] still hold; the closed loop gain of these test vehicles is still the ratio of $\frac{R_2}{R_1}$.

Since the summing point (input base) and output of the device are at one-half the zener supply voltage rather than ground, capacitors C_1 and C_2 must be used for coupling signals to the input and from the output. The size of these capacitors will then determine the lower frequency response of the device.

It should be noted here, that with the split zener approach, decoupling capacitors, C_3 and C_4, can in some instances be much larger than when operating directly from an external power supply due to the relative difference between the zener and power supply impedance levels.

The magnitude of isolation resistance R_3 should be chosen such that the input terminal, summing point, can be biased without seriously degrading the equivalent input impedance of the device due to the shunting effect of this resistance. If the degradation becomes excessive, serious closed loop gain errors can occur. Conversely, excessive resistance magnitudes can lower the open loop gain capability of the amplifier. Resistances in the order of 50-100 k should not be considered excessive.

Offset resistance R_4 is chosen to minimize offset error due to impedance unbalance as discussed under dc considerations and may or may not be used as dictated by impedance levels and output dynamic range considerations.

CONCLUSIONS

A method has been illustrated to permit operating the Motorola line of I/C operational amplifiers from a single supply by using a split zener biasing mode.

This technique when properly applied permits ac operation of the operational amplifier with little or no compromise of device characteristics. Although only the inverting mode of operation was illustrated in the examples, non-inverting modes, ac summing, etc., may also be used with the devices by observing the general considerations outlined.

ACKNOWLEDGEMENT

The author wishes to thank Van Osdel for his assistance in the preparation of this application note.

REFERENCES

1. Application Note AN-273 – Getting More Value Out of an Integrated Operational Amplifier Data Sheet – K. Blair.
2. Application Note AN-204 – High Performance Integrated Operational Amplifiers – L. Wisseman and J. Robertson.
3. Application Note AN-248 – A High Voltage Monolithic Operational Amplifier – L. Wisseman.

AN-404
A WIDE BAND MONOLITHIC VIDEO AMPLIFIER

INTRODUCTION

The Motorola MC1552G and MC1553G series of video amplifiers are silicon passivated monolithic integrated circuits designed for wide band system applications. The device characteristics should be effective in the design of wide band communications systems where low intermodulation and harmonic distortions are required and in radar or PCM pulse applications where gain stability and fast rise times are of concern.

Wide bandwidth, low distortion, gain predictability, and stability are enhanced in both devices by use of negative feedback. A temperature compensated dc feedback network is also employed to stabilize quiescent operating points for maximum dynamic range capability over the military temperature range of -55°C to +125°C.

GENERAL DESCRIPTION

The MC1552G and MC1553G video amplifier configurations are similar as shown in the schematic diagrams of Figures 1 and 2. The main difference between devices is the magnitude of the feedback and emitter resistances used to set up the voltage gain levels. Both devices are designed for single-ended input and single-ended output operation from one power supply.

Each device employs a three-stage direct coupled common emitter cascade (Q_1, Q_2, Q_3) with series-series negative feedback from the third stage emitter to the first stage emitter.[1] This particular multiple stage feedback configuration supplies a solution to the problem of gain control and gain stability in the units. The variation of active and passive device parameters with material properties, process controls, temperature, etc., in integrated circuits normally prohibits gain predictability and stability. The proximity of the elements on a monolithic chip contributes to a commonality of characteristics in the form of matching of active element characteristics, low tolerance resistance ratios, and similar temperature characteristics. All ultimately contribute to controlled operation of the video amplifiers. In this particular area the multiple stage series-series feedback configuration delegates dependence of closed loop voltage gain upon the magnitude of resistance ratios (Appendix A), which are controllable within a few percent and track within a few percent over a temperature range, and thus supplies a predictable and stable gain.

The negative feedback also extends the effective bandwidth of the devices by trading gain for bandwidth. A more constant gain-bandwidth product can usually be obtained with the multiple stage feedback used in the MC1552G and MC1553G than with feedback in single amplifier stages connected in cascade.

An emitter follower Q4 is used at the output of the basic feedback triple to provide low output impedance to enhance output efficiency and to minimize bandwidth degradation due to capacitive loading. A separate shunt-shunt dc feedback loop, which is normally decoupled with respect to ac signals, consisting of emitter follower resistor R9, and shunt feedback resistor R7 extends from the input to the output of the devices to set the quiescent output voltage. Current extracted from this loop by current source Q5 provides close temperature compensation of the quiescent point (±50mV).[2]

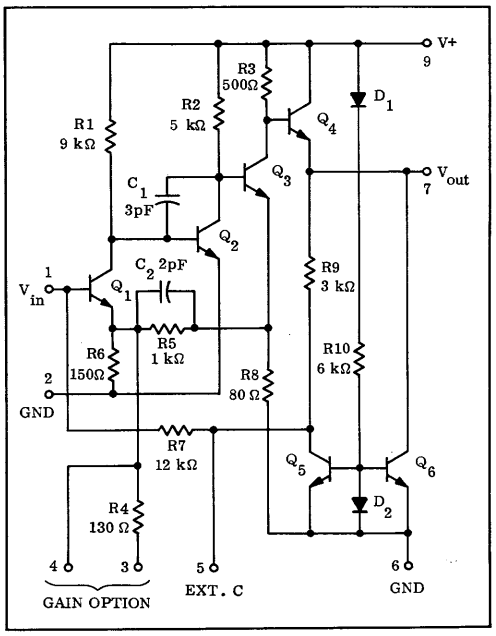


FIGURE 1 — MC1552 (LOW GAIN) SCHEMATIC DIAGRAM

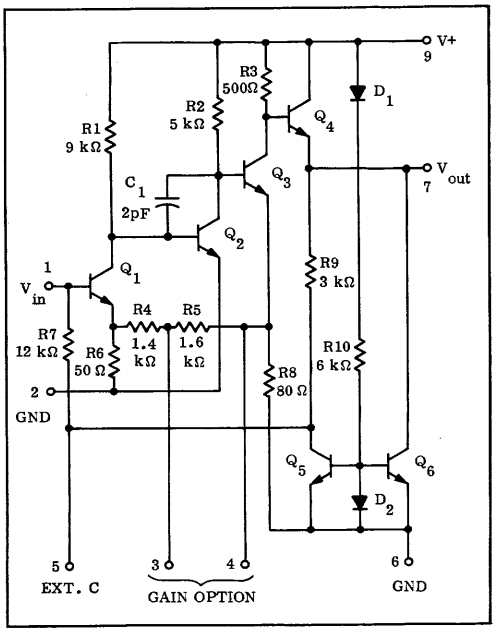


FIGURE 2 — MC1553 (HIGH GAIN) SCHEMATIC DIAGRAM

The diode bleeder network consisting of D_1-R_{10}-D_2 determines the magnitude of sink current flowing in current sources Q5 and Q6. As implied above and discussed in other publications,[3] when the diode D2 and transistors Q5 and Q6 are in close proximity on the monolithic chip, the diode V-I relationship will be essentially identical to that of the base-emitter diode of Q5 and Q6. Therefore, when a finite dc current is driven through diode D2, an identical dc emitter current flows through the transistors thereby establishing bias conditions.

The output quiescent level of the devices is maintained at one-half the operating supply voltage. Current source Q6 is used to establish symmetrical positive and negative load current excursions regardless of emitter resistance magnitude, power supply voltage, or ambient temperature.

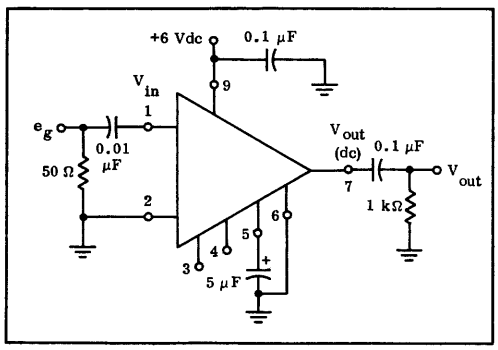
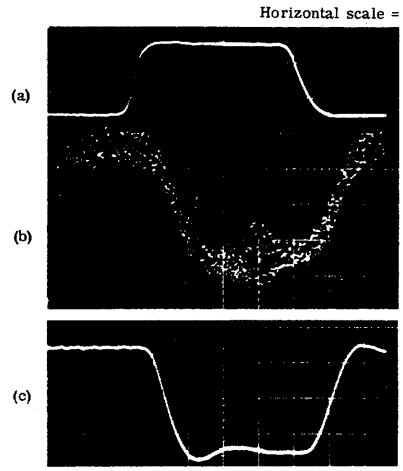


FIGURE 3 – TEST CIRCUIT FOR MC1552G/1553G VIDEO AMPLIFIERS

CHARACTERISTICS

Figure 3 is the test circuit used to determine the characteristics of the video amplifiers. There are several considerations that should be followed when operating the MC1552G and MC1553G video amplifiers to assure reliable operation and correlation of device characteristics.



(a) Input pulse
(b) Output pulse with inadequate bypass capacitor
(c) Output pulse with adequate bypass capacitor

FIGURE 4 – EFFECT OF POWER SUPPLY BYPASS CAPACITOR ON AMPLIFIER OPERATION

1. A high frequency capacitor should be used to bypass the power supply (Figure 3). This capacitor should be as close to the device as possible to minimize the effects of power supply lead inductance. Figure 4 illustrates pulse degradation that can occur with inadequate power supply decoupling. In this particular example, instability was encountered.

TABLE I – VOLTAGE GAIN LEVELS OBTAINABLE WITH MC1552G/MC1553G VIDEO AMPLIFIERS

Device	Voltage Gain Volts/Volt	Configuration	Comments
MC1552G	50	Figure 3	
	100	Figure 3	Ground Pin 3
	50 to 3000	Figure 3	Connect external resistance from Pin 4 to gnd
	1< to 3000	Figure 6	Non-inverting Voltage gain = $6.25 \times \frac{1000}{R}$
MC1553G	400		Output @ Pin 7
	61	Figure 7	Non-inverting Output @ Pin 4
	29		Non-inverting Output @ Pin 3
	200	Figure 7	Connect Pin 3 to Pin 4 Output @ Pin 7
	30		Non-inverting Connect Pin 3 to Pin 4 Output @ Pin 3/4
	400 to 3000	Figure 7	Connect external resistance from Pin 3 to gnd Output @ Pin 7
	61 to 480		Non-inverting Connect external resistance from Pin 3 to gnd Output @ Pin 4
	29		Non-inverting Connect external resistance from Pin 3 to gnd Output @ Pin 3

2. Terminal 6 of the device should be grounded as close to the can as possible to minimize overshoot in pulse applications.
3. If large input and output coupling capacitors are used, it may be necessary to place a shield between them to avoid input-output coupling.
4. The shunt feedback decoupling capacitor on terminal 5 is required to preserve the input impedance and the resultant gain when driving from higher source impedance levels.

VOLTAGE GAIN

The MC1552G and MC1553G video amplifiers present numerous voltage gain options that may be used to establish a broad range of gain levels. In order to review the gain options adequately with a minimum of confusion, the available options of each device will be discussed individually. The voltage gain options and conditions are catalogued in Table I for reference. The appropriate voltage gain equations are also derived in the Appendices and may be used to verify and determine gain levels.

MC1552G GAIN OPTIONS

As outlined in Table I, when connected in the test configuration of Figure 3 without any modifications, the MC-1552G video amplifier has a voltage gain of 50 volts/volt. Grounding pin 3 of the device introduces a resistor in shunt with the existing first stage emitter resistor and increases this gain by a factor of two to the 100 V/V level. These are fixed gain options.

The gain can be adjusted over a much wider dynamic range and in smaller increments by inserting an external resistance from pin 4 of the device to ground in the configuration of Figure 3. This simply places a discrete resistance in shunt with the emitter resistance. As shown in Table I and indicated in Figure 5, curve A, the gain can be adjusted continuously from 50 V/V to 600 V/V.

The MC1552G can also be used as a non-inverting amplifier with a wide range of voltage gains. In this mode of operation, shown in Figure 6, the input signal is inserted through an external series resistor into the emitter of the input transistor. The normal input terminal, pin 1, is connected to ac ground. With this technique the amplifier gain can be adjusted over a range of less than unity to 600 V/V as shown in Table I and indicated in Figure 5, curve B. In this configuration, the gain is a linear function of the external series resistance. (See Appendix C)

MC1553 GAIN OPTIONS

The MC1553G video amplifier also exhibits great versatility with respect to available gain levels, but in a slightly different manner.

Figure 7 shows the MC1553G connected much in the same manner as the test circuit of Figure 3. The exception is that, in Figure 7, two additional output signal terminals, V_1 and V_2, are provided. Inspection of Figure 2, the schematic diagram of the device, shows that these extra output terminals are available and each is capable of supplying graded gain levels for a given device gain. As listed in Table I, the signal gain from input pin 1 to output pin 7 is normally 400 V/V; 61 V/V and non-inverted at output pin 4; 29 V/V, and non-inverted at output pin 3. (See Appendix A) Connecting pins 3 and 4 together short out a portion of the feedback resistance and reduce the gain at output pin 7 by a factor of 2 to 200 V/V; the gain at pins 3 and 4 remains at the 29 V/V level non-inverted.

The voltage gain of this video amplifier can also be adjusted over a wider dynamic range and in smaller incre-

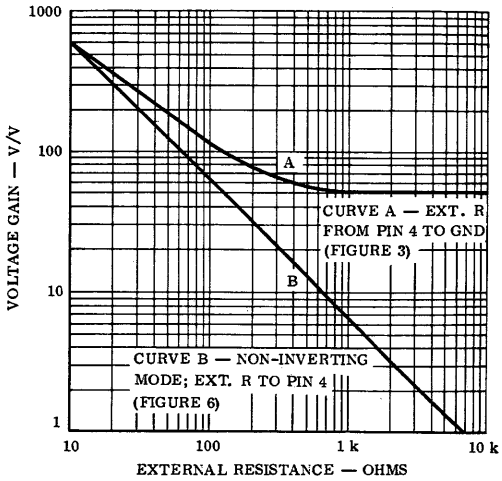


FIGURE 5 — MC1552G VOLTAGE GAIN ADJUSTMENT WITH EXTERNAL RESISTANCE

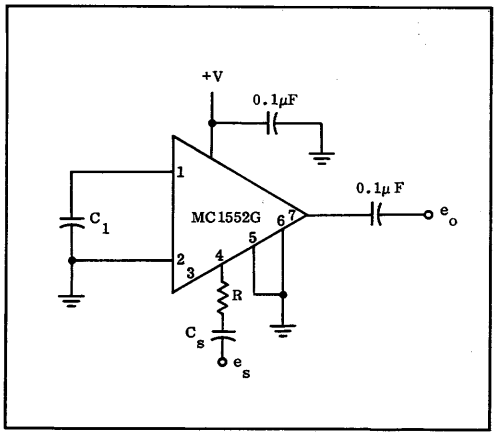


FIGURE 6 — MC1552G CONNECTED IN NON-INVERTING MODE

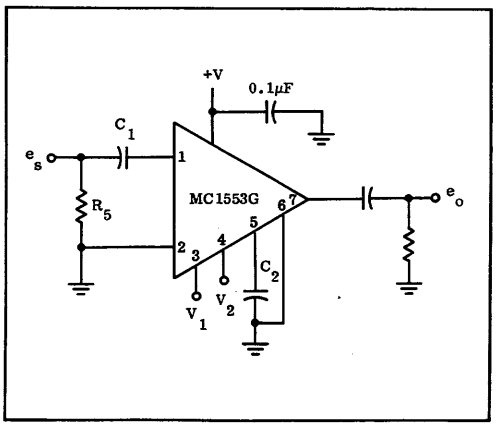


FIGURE 7 — MC1553G CONFIGURATION WITH MULTIPLE OUTPUT CAPABILITY

ments by use of external resistance (Appendix B). As indicated in Table I and shown in Figure 8, insertion of an external resistance from pin 3 to ground permits a significant gain adjustment range at two of the three output terminals by introducing a voltage divider in the feedback network.

Insertion of external resistances will, in some instances, permit a higher gain error and gain variation with temperature because of the tolerances and differences in temperature coefficients between the internal and external resistances.

HIGH FREQUENCY RESPONSE

The low output impedance of the video amplifiers prohibits load capacity from seriously degrading the high frequency performance. The high input impedance of the conventional configuration (Figure 3) will begin to restrict the bandwidths due to input capacity when the devices are driven from high impedance sources. This will generally not occur until the source impedance exceeds several hundred ohms. Negative feedback is used to extend the effective bandwidth of the devices by trading gain for bandwidth. Therefore, as illustrated for the two examples of Figure 9, the video amplifier bandwidth will be modified as the gain of the device is adjusted for the conventional configurations.

In the non-inventory configuration of Figure 6 the bandwidth degradation with gain is not nearly as severe as with the conventional configurations until the higher gain levels are reached. Figure 10 shows the pulse response of the MC1552G connected in the non-inverting mode at gain levels of 1.2, and 52. Note that the bandwidth degradation is minor. Examination of the circuit shows that, in the gain ranges of concern in the non-inverting mode, the amplifier feedback loop is not significantly disturbed and thus the bandwidth is preserved.

In Figure 11 the effect of load capacity on the responses at the output terminals of the MC1553G is illustrated. As shown, any variations in frequency response encountered was in a manner to enhance high frequency operation.

LOW FREQUENCY RESPONSE

The low frequency response of the MC1552G and MC-1553G video amplifiers is dependent upon the magnitudes of the input-output coupling capacitors and the decoupling capacitor used with the dc shunt feedback loop.

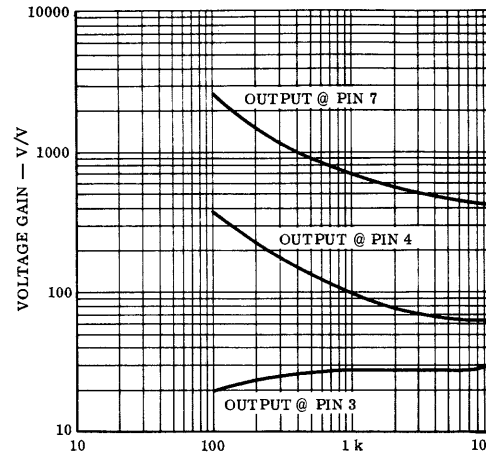


FIGURE 8 — MC1553G VOLTAGE GAIN ADJUSTMENT WITH EXTERNAL RESISTANCE

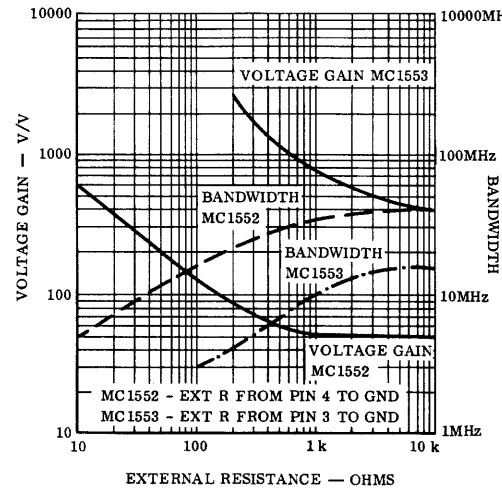
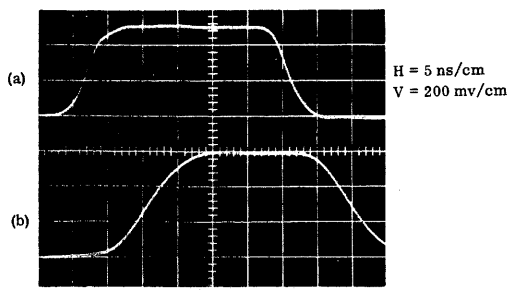


FIGURE 9 — BANDWIDTH MODIFICATION WITH GAIN ADJUSTMENTS



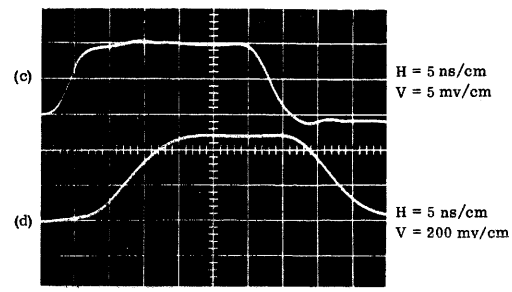


FIGURE 10 — PULSE RESPONSE OF MC1552G IN NON-INVERTING MODE

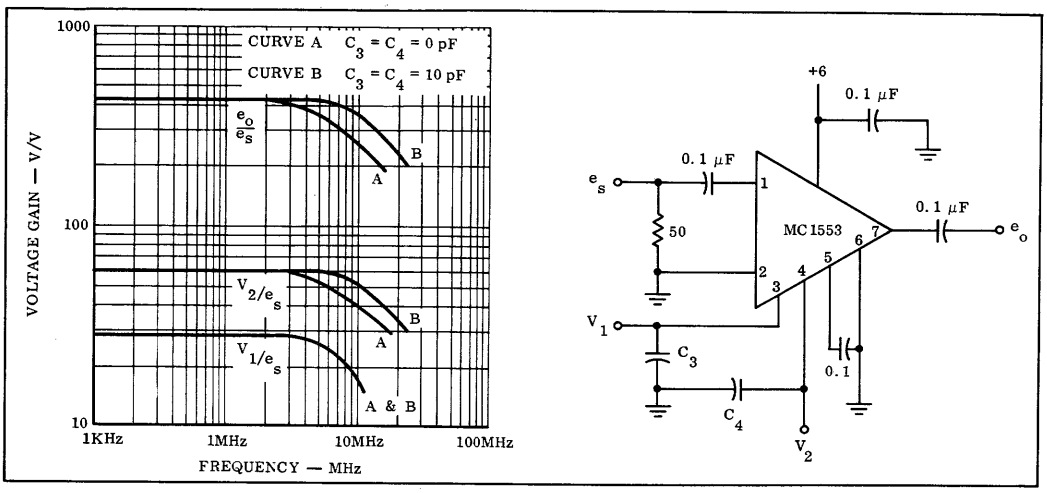


FIGURE 11 — EFFECT OF LOAD CAPACITIES ON FREQUENCY RESPONSE OF MC1553G

The response curves of Figure 12 in conjunction with the three typical device configurations illustrated in Tables II, III, and IV permit rapid determination of the coupling and decoupling capacitor magnitudes for the necessary low frequency response. To obtain a given low frequency response, simply select the curve number in Figure 12 that corresponds to the response and gain desired. The table associated with the particular circuit configuration chosen in Tables II, III, or IV is then scanned for the appropriate capacitor magnitudes.

Example: Assume that a fixed gain of 100 and a low frequency response of 1 KHz is desired with the configuration illustrated in Table II (Figure 3). In Figure 12 this would be curve 2C. Table II indicates that a 0.01μF coupling capacitor and an 8μF feedback decoupling capacitor are required. To obtain the voltage gain of 100, the terminal 3 of the MC1552G can be grounded as indicated in Table I.

If the gain is established by use of external resistances, as per Figure 5 or 8, the curves of Figure 12 are no longer valid. Instead, the equations listed in Table V for the various configurations should be used to determine the capacitor values for the lower cutoff frequency, f_c. In Table V capacitor C_S is the series input coupling capacitor for the MC1552G non-inverting mode.

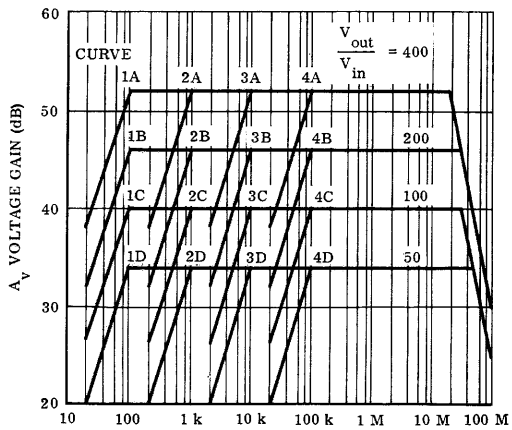


FIGURE 12 — LOW FREQUENCY RESPONSE CURVES

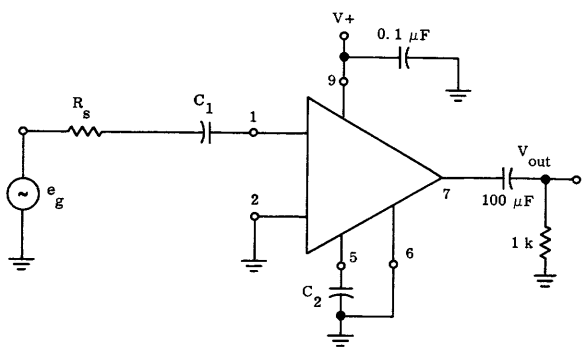


TABLE II — CAPACITOR VALUES FOR CAPACITIVE COUPLED INPUT (R_S < 5 KΩ)

CURVE NO.	C_1 (μF)	C_2 (μF)
1A	0.1	250
1B	0.1	150
1C	0.1	70
1D	0.1	40
2A	0.01	30
2B	0.01	18
2C	0.01	8.0
2D	0.01	4.0
	(pF)	
3A	1000	3.0
3B	1000	1.8
3C	1000	0.8
3D	1000	0.4
4A	100	0.3
4B	100	0.18
4C	100	0.08
4D	100	0.04

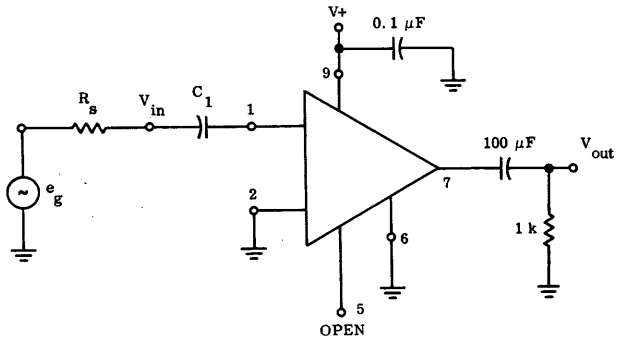


TABLE III — CAPACITOR VALUES FOR CAPACITIVE COUPLED INPUT ($R_s < 500\ \Omega$)

CURVE NO.	C_1 (μF)
1A	20
1B	10
1C	7.0
1D	3.0
2A	3.0
2B	1.0
2C	0.8
2D	0.5
3A	0.4
3B	0.2
3C	0.1
3D	0.06
4A	0.04
4B	0.02
4C	0.01
4D	0.007

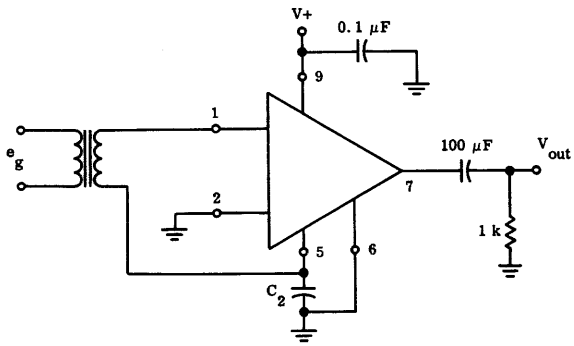


TABLE IV — CAPACITOR VALUES FOR TRANSFORMER COUPLED INPUT

CURVE NO.	C_2 (μF)
1A	200
1B	100
1C	70
1D	30
2A	20
2B	10
2C	7.0
2D	3.0
3A	2.0
3B	1.0
3C	0.7
3D	0.3
4A	0.2
4B	0.1
4C	0.07
4D	0.03

TABLE V — CAPACITOR VALUES FOR AMPLIFIERS USING EXTERNAL GAIN ADJUST RESISTORS

Configuration	C_1 (farads)	C_2 (farads)	C_s (farads)
Table II Capacitive Coupled Input (Rs< 5K)	$\frac{1}{2\pi f_c(1.7 \times 10^4)}$	$8C_1\left(\frac{V_{out}}{V_{in}}\right)$	—
Table III Capacitive Coupled Input (Rs < 500Ω)	$\frac{V_{out}/V_{in}}{2\pi f_c(1.5 \times 10^4)}$	—	—
Table IV Transformer Coupled Input	—	$\frac{V_{out}/V_{in}}{2\pi f_c(3 \times 10^3)}$	—
Figure 6 Capacitive Coupled Input Non-inverting	$\frac{1}{2\pi f_c(100)}$	—	$\frac{1}{2\pi Rf_c}$

C_s = Series coupling capacitor, non-inverting mode.

PERFORMANCE WITH POWER SUPPLY VARIATIONS

In the design of some systems it is sometimes advantageous to operate the video amplifiers from a supply voltage other than the 6 volt supply used to characterize the devices. This is permissable as long as the maximum device ratings are not exceeded or levels reduced so as to render the device inoperable. Figures 13, 14, and 15 illustrate typical variations of conventional configuration device parameters as the supply voltage is modified. Figure 13 depicts the typical device current drain at the various usable supply voltage levels. The peak to peak output voltage swing capability of the devices with various loads is shown in Figure 14. Figure 15 shows the dependence of pulse rise time (bandwidth) upon supply voltage.

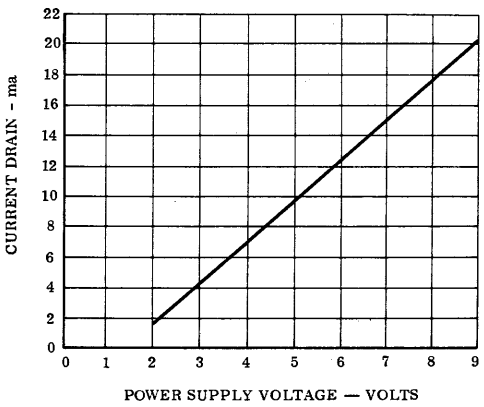


FIGURE 13 — VIDEO AMPLIFIER CURRENT DRAIN VS POWER SUPPLY VOLTAGE

APPLICATIONS

The MC1552G and MC1553G video amplifiers can be used in a wide variety of design applications. Any solid state system that requires wide bandwidth, gain predictability and stability will find these versatile amplifiers capable of meeting design requirements.

In addition to the conventional linear operating modes (i. e., pulse amplifiers, wide band, etc.) the video amplifiers can also be used in many alternate configurations, both linear and non-linear. Actually the number of applications is limited only by the ingenuity of the circuit designer. As long as the maximum ratings of the devices are observed in all applications and reasonable dc operating levels maintained in the linear operating modes, full versatility of the devices can be realized.

PULSE AMPLIFIER

One of the prime design functions of the MC1552G and MC1553G devices is the processing of complex video pulses or pulse trains. The capability of the MC1552 device when connected in the mode of Figure 3 was illustrated in Figure 4 for a high speed pulse.

When connected in the non-inverting configuration of Figure 6, the MC1552G still maintains its high frequency capability as was shown in the output waveshapes of Figure 10.

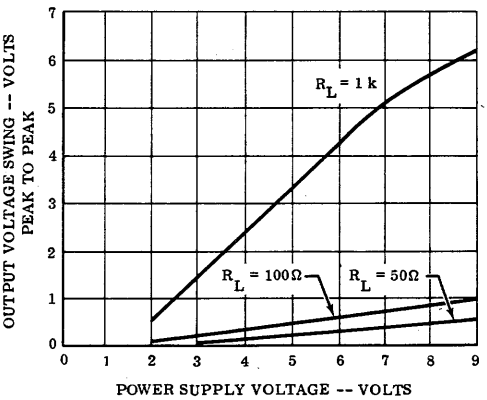
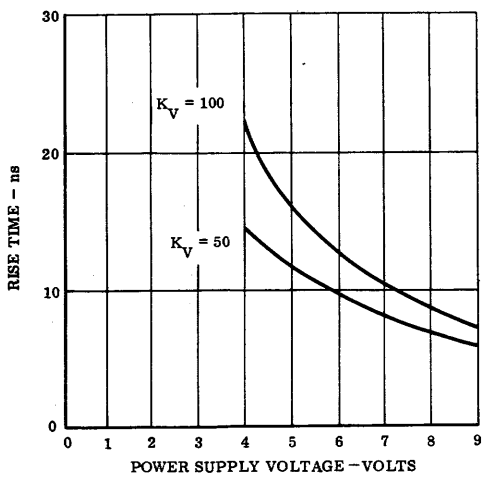
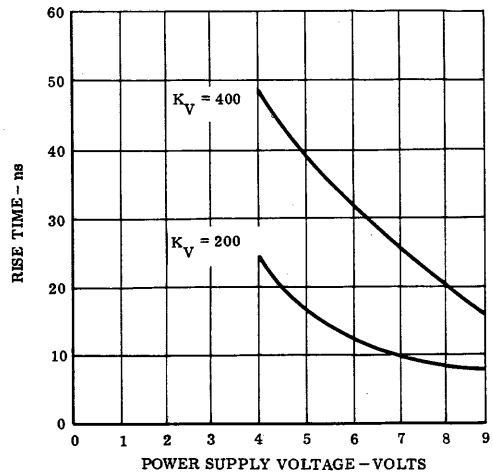


FIGURE 14 — TYPICAL PEAK TO PEAK OUTPUT SWING AS A FUNCTION OF POWER SUPPLY VOLTAGE AND LOAD RESISTANCE



(a) MC1552



(b) MC1553

FIGURE 15 — DEVICE RISE TIME AS A FUNCTION OF POWER SUPPLY VOLTAGE

In either mode of operation, the considerations outlined for operating the devices should be observed to assure reliable operation.

SUMMING/SCALING AMPLIFIER

Figure 16 illustrates the MC1552G video amplifier connected as a summing/scaling amplifier. In this noninverting configuration the summation of input signal currents is accomplished at the summing point, pin 4, through the input resistors. Scale factor considerations are accomplished by adjustment of the design values of the input summing resistors.

The voltage gain associated with each input signal is discussed in Appendix C. Using the resistor values indicated in Figure 16 to establish the scale factor levels, the input signals of Figure 17a were injected into the amplifier. The composite summed/scale output wave shape is shown in Figure 17b.

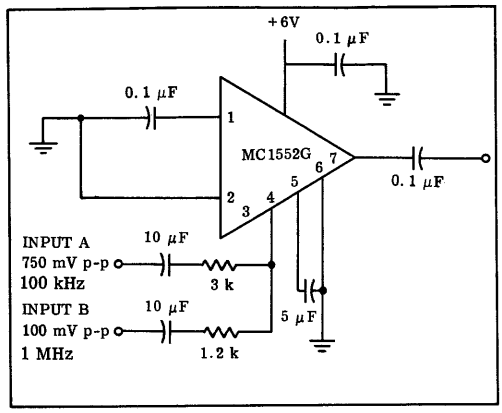
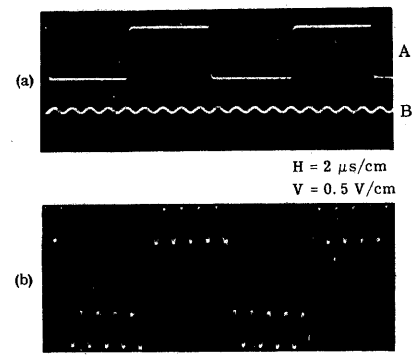


FIGURE 16 – MC1552G CONNECTED IN SUMMING/SCALING AMPLIFIER PERFORMANCE

OSCILLATOR

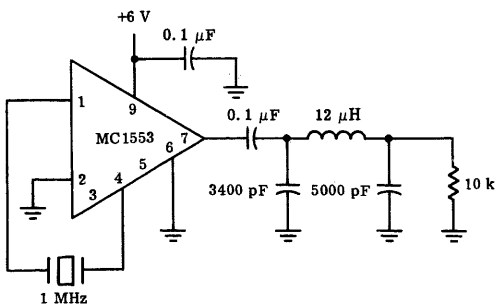
The wide bandwidth and output swing capability of the video amplifiers makes them suitable for high frequency master clocks or local oscillators in many system designs. One possible configuration is shown in Figure 18. In this instance positive feedback is injected through the 1 MHz series mode crystal to input pins 1. The bias decoupling capacitor normally on pin 5 should be omitted in this oscillator design to insure that the crystal operates into a relatively low impedance. The output of the oscillator is taken from pin 7 which is buffered from the oscillator circuit proper by a stage of gain and an emitter follower. As shown in Figure 18a, no provisions were made in the design to control the loop gain or the amplitude of oscillation in order to reduce harmonic content. Instead, a "brute-force" π filter was inserted at the output (pin 7) to extract the fundamental frequency. Figure 18b shows the resultant output waveform.

For more sophisticated designs or for higher frequencies, a tuned feedback network can be used in conjunction with the crystal to provide the necessary phase shift adjustment and feedback control to insure oscillation and reduce harmonic content. If desired, AGC networks can also be included.

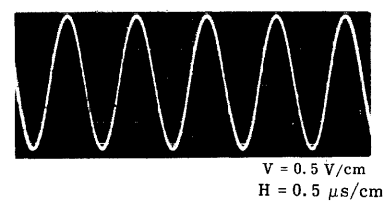


(a) Input signal waveforms
(b) Composite output signal waveform

FIGURE 17 – SUMMING/SCALING AMPLIFIER WAVEFORMS



(a) Oscillator configuration



(b) Output waveform

FIGURE 18 – MC1553G CONNECTED AS OSCILLATOR

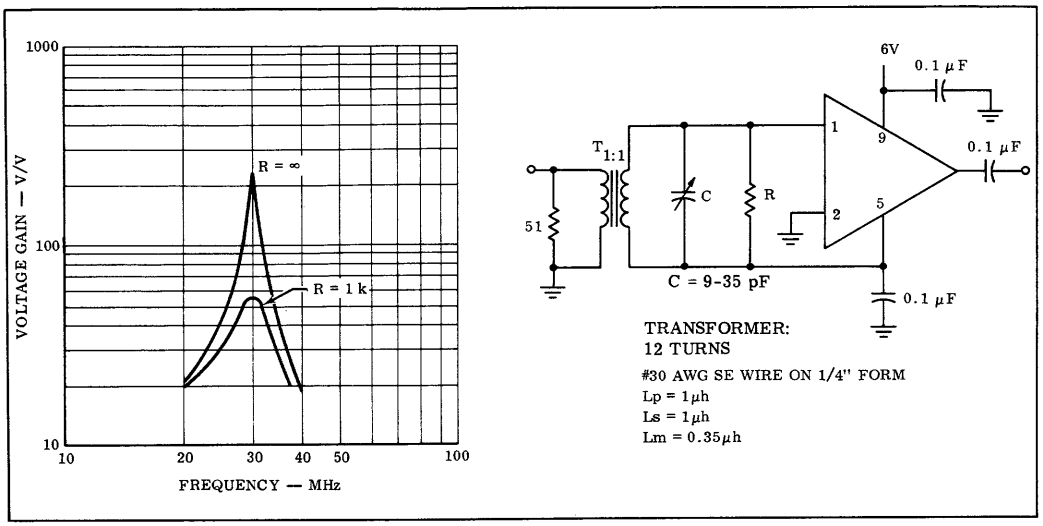


FIGURE 19 — RESPONSE OF MC1552G WITH TRANSFORMER COUPLED INPUT

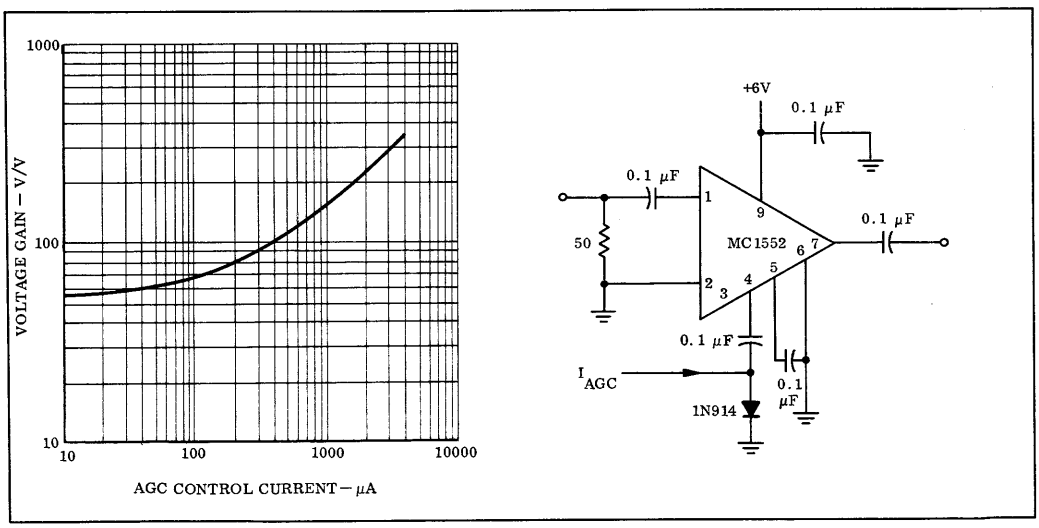


FIGURE 20 — MC1552G GAIN CONTROL WITH EXTERNAL DIODE

TUNED AMPLIFIER

The gain and frequency capabilities of the MC1552G and MC1553G video amplifiers makes them logical choices for tuned amplifier applications. The high input impedance associated with the devices can accomodate narrow bandwidth requirements in a tuned configuration.

Figure 19 illustrates how the MC1552G video amplifier can be used with a single tuned transformer coupled input. Two responses are presented. The first uses the input impedance of the video amplifier as the transformer secondary termination, and the second uses a 1K damping resistor on the secondary. Insertion of the damping resistance broadens the response at the expense of gain but at the same time reduces loading variations on the source which can become substantial with this particular type of tuning.

The overall amplifier gains are substantial because of the transformer characteristics and can be calculated from the gain equation derived for this type of coupling in Appendix D. Examination of the equations will also indicate that maximum gain does not occur when the secondary is tuned to the center frequency. This is simply because of the primary inductance and reflected inductance or capacitance of the secondary as indicated.

AGC

In many amplifier applications it is necessary to include AGC capabilities to accommodate signal levels with

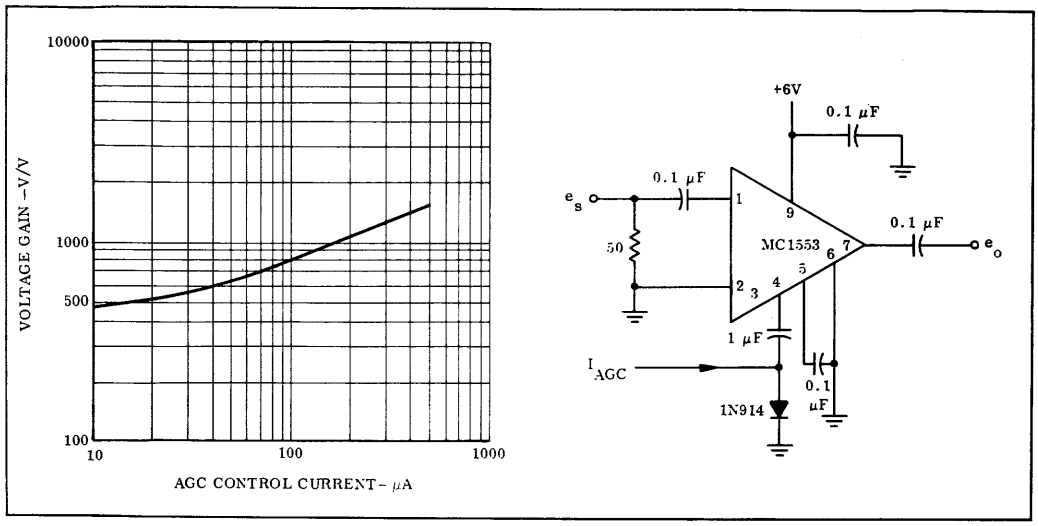


FIGURE 21 – MC1553 GAIN CONTROL WITH EXTERNAL DIODE

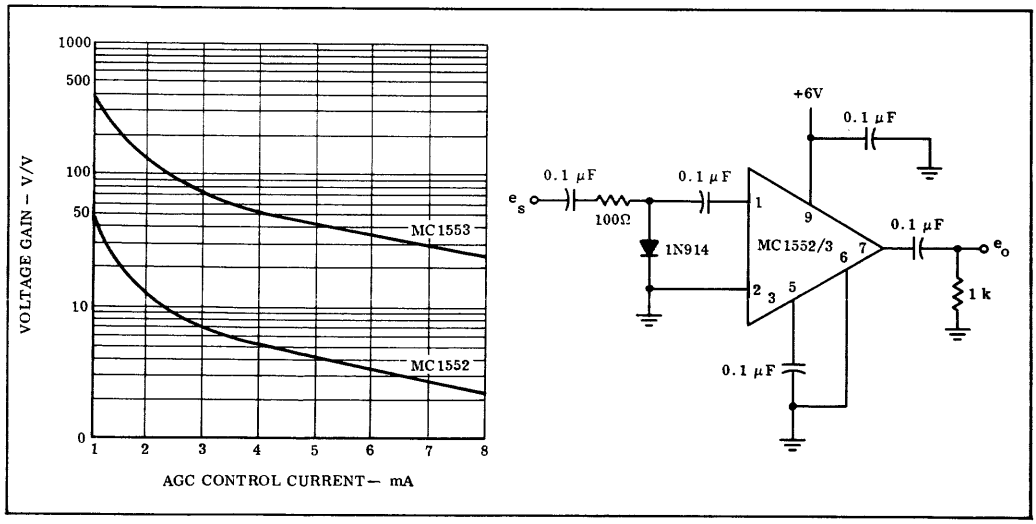


FIGURE 22 – VIDEO AMPLIFIER GAIN CONTROL WITH EXTERNAL DIODE

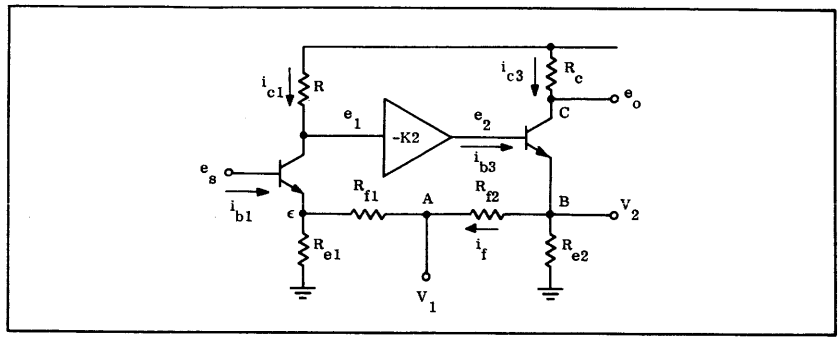


FIGURE 23 – SIMPLIFIED VIDEO AMPLIFIER AC EQUIVALENT CIRCUIT

wide dynamic ranges. As discussed previously, the gains of the MC1552G and MC1553G video amplifiers can be adjusted with external resistances. A logical design point for AGC considerations would be the replacement of the external resistances with variable resistances or simply diodes.

In Figures 20 and 21 the external resistances were replaced with 1N914 diodes and the gain of the amplifiers measured as a function of diode control (AGC) current. As illustrated, a wide range of gain control is obtained. The 1N914 diodes were chosen solely for convenience in this instance and can be replaced by any other suitable diode on the market.

This type of AGC control does have the limitations that the lowest level of gain that can be obtained is the normal unmodified gain of the amplifier. For lower gain level control an alternate design approach is necessary. Figure 22 illustrates a configuration that can be used with the video amplifiers to obtain AGC at reduced gain levels. In this configuration the diode is used simply as a variable impedance in a voltage divider network.

APPENDIX A – VIDEO AMPLIFIER VOLTAGE GAIN

When the schematic diagrams of Figures 1 and 2 are examined from an ac point of view, without the bias circuitry, the simplified representation shown in Figure 23 evolves. This simplified ac circuit is adequate to determine the voltage gain between the input, pin 1, and any of the designated output terminals. (In the MC1552G video amplifier, nodes A and B are not available and feedback resistors R_{f1} and R_{f2} are a single resistor.)

VOLTAGE GAIN FROM INPUT TO NODE A

From Figure 23 the following nodal equations can be written to determine the voltage gain from the input of the video amplifier to node A,

$$V_1 = V_2 \left[\frac{R_{f1} + R_{e1}}{R_{e1} + R_{f1} + R_{f2}}\right] = V_2 - i_f R_{f2} \quad (1)$$

$$V_2 = e_i(-K_2) \quad (2)$$

$$e_1 = (e_s - \epsilon)(-K_1) \quad (3)$$

where $K_1 = \frac{R}{R_{e1}}$

$$V_2 = (e_s - \epsilon)(K_1 K_2) \quad (4)$$

$$\epsilon = V_2 \left[\frac{R_{e1}}{R_{e1} + R_{f1} + R_{f2}}\right] \quad (5)$$

Substituting equation (5) into (4)

$$V_2 = \left[e_s - \left(\frac{R_{e1}}{R_{e1} + R_{f1} + R_{f2}}\right) V_2\right] K_1 K_2 \quad (6)$$

$$V_2 \left[1 + \frac{R_{e1}(K_1 K_2)}{R_{e1} + R_{f1} + R_{f2}}\right] = e_s K_1 K_2 \quad (7)$$

$$V_2 = \frac{e_s K_1 K_2}{1 + \left(\frac{R_{e1}}{R_{e1} + R_{f1} + R_{f2}}\right) K_1 K_2} \quad (8)$$

Substituting equation (8) into (1) and simplifying

$$\frac{V_1}{e_s} = \frac{R_{e1} + R_{f1}}{\frac{R_{e1} + R_{f1} + R_{f2}}{K_1 K_2} + R_{e1}} \quad (9)$$

If the forward voltage gain K_1K_2 is large, as it normally would be in a feedback amplifier, then equation (9) reduces to

$$\frac{V_1}{e_s} = 1 + \frac{R_{f1}}{R_{e1}} \quad (10)$$

Equation 10 illustrates how the voltage gain at node A is determined by the ratio of two resistors. In integrated circuit fabrication resistance ratios can be controlled to much smaller tolerances (2-3%) than resistor magnitudes (15-20%) thus more predictable gains can be established by the former method.

VOLTAGE GAIN FROM INPUT TO NODE B

To determine the voltage gain to node B, the original nodal equations of node A, with two exceptions, may be used. The two exceptions are that equation (1) is no longer required, and that:

$$i_f = \frac{V_2 - \epsilon}{R_{f1} + R_{f2}} \quad (11)$$

This family of equations again yields a complex gain equation which when the amplifier forward gain is assumed large reduces to

$$\frac{V_2}{e_s} = 1 + \frac{R_{f1} + R_{f2}}{R_{e1}} \quad (12)$$

which is again determined by resistance ratios.

VOLTAGE GAIN FROM INPUT TO NODE C

To determine the voltage gain to node C, one equation must be added to those used for node B.

$$e_o = -i_{c3} R_c = -\beta_3 i_{b3} R_c \quad (13)$$

With a large forward voltage gain the voltage gain from the input to node C can be written as

$$\frac{e_o}{e_s} = -\frac{R_c}{Re_2}\left(1 + \frac{R_{f1} + R_{f2} + Re_2}{Re_1}\right) \quad (14)$$

In equation (14) the concept of resistance ratios is still maintained. In addition, note that the gain is now inverted due to the inversion of the final gain stage.

APPENDIX B – MC1553G VOLTAGE GAIN WITH EXTERNAL GAIN ADJUST RESISTOR.

The voltage gain of the MC1533G video amplifier can be adjusted by the use of an external resistor connected between pin 3 and ground. (Figure 2). This resistor in effect introduces a voltage divider in the feedback loop which by reducing the feedback factor increases the gain.

Figure 24 is the simplified AC circuit of the video amplifier with the external resistor R_{f3} inserted. From this model the voltage gain to any of the output nodes can be determined.

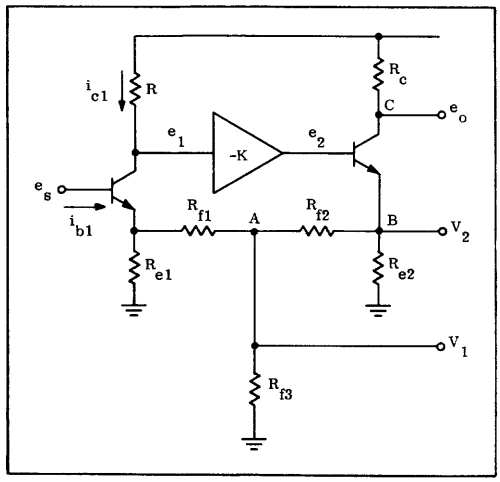


FIGURE 24 – SIMPLIFIED VIDEO AMPLIFIER CIRCUIT WITH EXTERNAL GAIN ADJUST RESISTOR

VOLTAGE GAIN FROM INPUT TO NODE A

Examination of Figure 24 indicates that nodal equations (1) through (6) of Appendix A still are applicable. Additional nodal equations required to account for the external resistor are

$$\epsilon = (i_{e1} + i_f + i_x)\,Re_1 = (\beta_1 i_{b1} + i_f - i_x)\,Re_1 \qquad (15)$$

$$i_x = \frac{V_1}{R_{f3}} \qquad (16)$$

$$i_f = \frac{V_1 - \epsilon}{R_{f1}} + i_x \qquad (17)$$

If again the forward gain is assumed large, the complex equation that evolves can be reduced to

$$\frac{V_1}{e_s} = 1 + \frac{R_{f1}}{Re_1} \qquad (18)$$

which is identical to equation (10), the gain to node A without an external gain adjust resistor. Because the node in question is adjacent to the summing point, (first stage emitter), alteration of the feedback loop will not appreciably alter the resultant gain at the node. This point is illustrated in Figure 8.

VOLTAGE GAIN FROM INPUT TO NODE B

For this node the same nodal equations can be used as for node A and the solution oriented to solve for the gain at this point. With a large forward gain the simplified gain to node B can be written as:

$$\frac{V_2}{e_s} = 1 + \frac{R_{f1} + R_{f2} + \dfrac{R_{f1}\,R_{f2}}{R_{f3}}}{Re_1} \qquad (19)$$

This equation can be verified by letting resistor R_{f3} become infinite and comparing to equation (12).

VOLTAGE GAIN FROM INPUT TO NODE C

Extending the nodal equations for the gain at node B to include node C (equation 13) and assuming a high forward gain, the voltage gain to node C can be written as

$$\frac{e_o}{e_s} = -\frac{R_c}{Re_2}\;1 + \qquad (20)$$

$$\frac{R_{e1}\,Re_2 + R_{f1}\,(Re_2 + R_{f2})}{R_{f3}}$$

$$\frac{R_{f1} + R_{f2} + Re_2 + \dfrac{R_{f3}}{Re_1}}{}$$

which, when $R_{f3} = \infty$, is identical to equation (14).

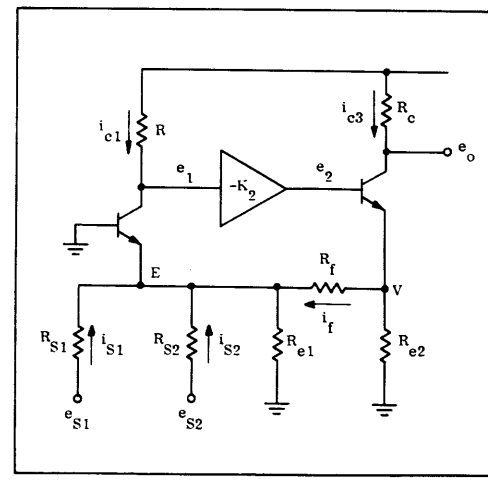


FIGURE 25 – SIMPLIFIED VIDEO AMPLIFIER CIRCUIT IN NON-INVERTING SUMMING AMPLIFIER MODE

APPENDIX C – MC1552G NON-INVERTING SUMMING AMPLIFIER VOLTAGE GAIN

From Figure 25 the following nodal equations can be written

$$e_o = -i_{c3}\,R_c = -\beta_3 i_{b3} R_c \qquad (21)$$

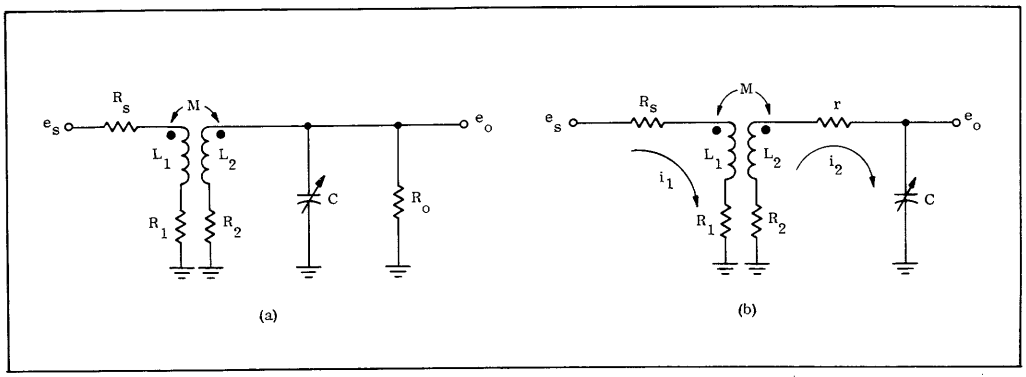


FIGURE 26 – INPUT TRANSFORMER AC EQUIVALENT CIRCUIT

$$i_{b3} = \frac{e_2 - V}{\beta_3 re_3} \quad (22)$$

$$e_2 = K_2 e_1 \quad (23)$$

$$e_1 = i_{c1} R = -i_{e1} R \quad (24)$$

$$i_{e1} = -\frac{\epsilon}{re_1} \quad (25)$$

$$\epsilon = (i_{s1} + i_{s2} + i_{e1} + i_f) Re_1 \quad (26)$$

$$i_{s1} = \frac{e_{s1} - \epsilon}{R_{s1}} \quad (27)$$

$$i_{s2} = \frac{e_{s2} - \epsilon}{R_{s2}} \quad (28)$$

$$i_f = \frac{V - \epsilon}{R_f} \quad (29)$$

$$V = (i_{e3} - i_f) Re_2 = (\beta_3 i_{b3} - i_f) Re_2 \quad (30)$$

$$e_o = \left(\frac{e_{s1}}{R_{s1}} + \frac{e_{s2}}{R_{s2}}\right)\left(\frac{R_c}{R_{e2}}\right)(R_f + R_{e2}) \quad (31)$$

APPENDIX D – TUNED AMPLIFIER GAIN

The input circuitry of Figure 19 at the frequencies of interest can be drawn as shown in Figure 26a. Resistances R_1 and R_2 are the primary and secondary ac resistances, R_s the source or terminating resistance, and R_o the amplifier input impedance. The exact expression for the voltage gain of the transformer is cumbersome because the secondary circuit is series - parallel as far as the secondary induced voltage is concerned. The parallel combination of R_o and L can be replaced by a series combination of r and L as shown in Figure 26b if R is much greater than L (normally true except for very low Q circuits),[3] where

$$r = \frac{(\omega L)^2}{R}$$

Writing the primary and secondary loop equations (32) & (33)

Combining these equations and solving for the output voltage e_o yields (when high forward gains are assumed)

$$e_s = i_1 (R_s + R_1 + J\omega L_1) - i_2 (J\omega M) \quad (32)$$

$$0 = i_1 (J\omega M) - I_2 \left(r + R_2 + J\omega L_2 + \frac{1}{J\omega C}\right) \quad (33)$$

The output voltage is

$$e_o = i_2 \left(\frac{1}{J\omega C}\right) \quad (34)$$

Substituting equations (32) and (33) into equation (34) yields for the transfer functions.

$$\frac{e_o}{e_s} = \frac{M/C}{(R_1 + R_s + J\omega L_1)\left[r + R_2 + J\left(\omega L_2 - \frac{1}{\omega C}\right)\right] + (\omega M)^2} \quad (35)$$

From equation (36) it can be seen that maximum gain does not occur when the secondary is tuned to resonance.

ACKNOWLEDGEMENT

The author wishes to thank Van Osdel for his assistance in the preparation of this application note.

REFERENCES

1. A Monolithic Feedback Triple With 3 GHz Gain - Bandwidth Product - J. E. Solomon, G. R. Wilson; International Solid State Circuits Conference, Philadelphia, Pa. February 1966.

2. A Highly Desensitized Wideband Monolithic Amplifier J. E. Solomon, G. R. Wilson; IEEE Journal of Solid State Circuits, Vol SC-1, No. 1, Sept. 1966, . . .

3. An Integrated Circuit RF-IF Amplifier - J. J. Robertson; B. Welling; Application Note AN-247.

AN-432 A
A MONOLITHIC INTEGRATED FM STEREO DECODER SYSTEM

INTRODUCTION

The use of integrated circuits in high quality FM receivers is already a fact. As the trend continues to a more extensive use of these units, the development of an integrated circuit FM stereo decoder becomes most desirable.

In practice, the integration of a discrete multiplex circuit cannot be restricted to the realization of the different stages involved in the stereo decoding action, but should consider the incorporation, in the same chip, of some of the auxiliary circuits so often used in FM stereo design. The number and type of these auxiliary circuits vary from one receiver to another. In some of them it reduces to a simple lamp indicator, in others it evolves into a more sophisticated approach where automatic, as well as manual selection for the muting and the stereo-monaural mode are available.

A comprehensive solution of all these circuit problems is given by either the MC1304 or the MC1305 versions of the IC multiplex. These two ICs consist of two different functional blocks, one containing the stereo decoder, the other containing three auxiliary circuits providing muting, stereo-monaural selection, and stereo lamp indication. The MC1305, in particular, has provision to incorporate an external variable resistor (pin 9) to adjust the channel separation. (Figure 3)

These auxiliary circuits can be combined in several ways, giving the designer a choice of several combinations which meet personal design preferences. Muting between stations, automatic switching to monaural reception for weak stereo signals, and "stereo select" action, are some of these options.

Special care has been taken to assure the quality of

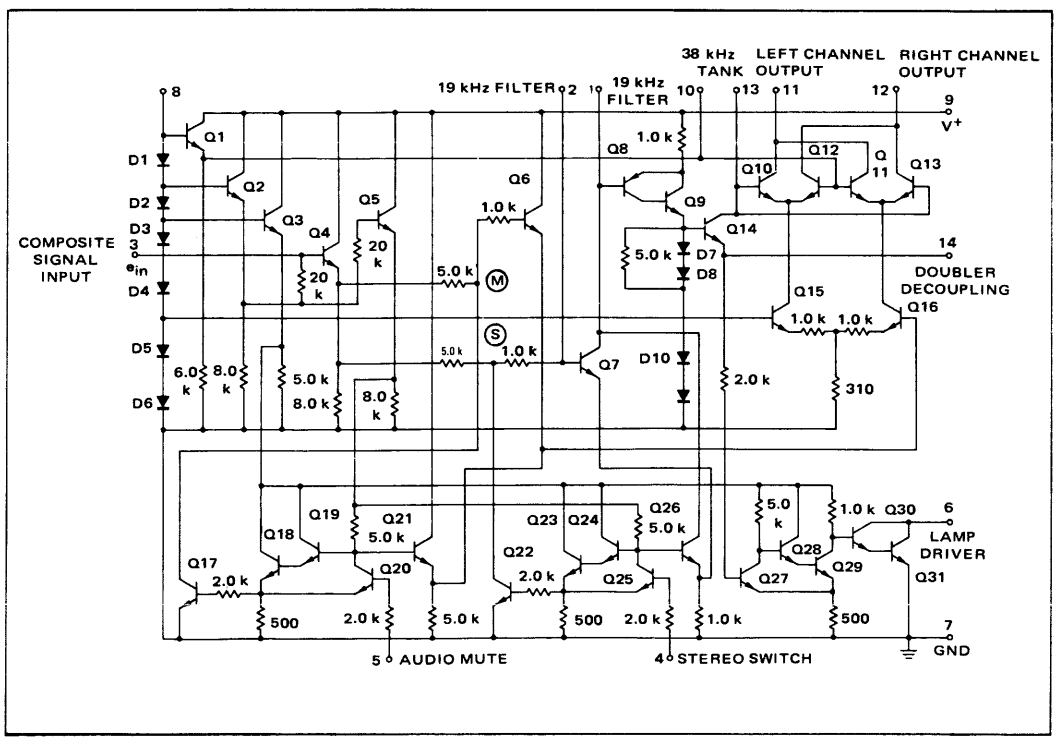


FIGURE 1 – MC1304 Circuit Schematic

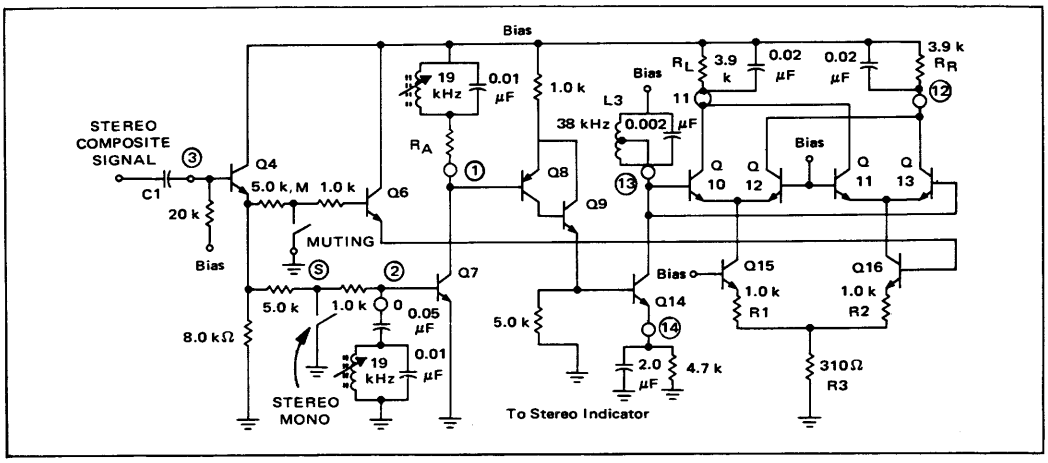


FIGURE 2 – Simplified Diagram of Stereo Decoder Portion

these auxiliary circuits. The stereo lamp indicator in particular has a built-in hysteresis that makes it possible to tune a stereo station without flickering.

The ICs feature excellent channel separation across the entire audio range (in excess of 30 dB); good ultrasonic rejection (in excess of 20 dB at 38 kHz); low THD content at the output (less than 1%*) and excellent SCA immunity for services using a 67 kHz subcarrier (in excess of 50 dB without the use of an external trap).

Power supply requirements are mainly determined by the lamp indicator circuit, which handles up to 40 mA. The rest of the IC requires 10 mA at 8.5 V.

FM STEREO DECODER CIRCUIT OPERATION

The complete circuit diagram of the MC1304 is shown in Figure 1. (No functional differences exist between the MC1304 and 1305 versions.) For the sake of simplicity, Figure 2 shows only the FM stereo decoder portion neglecting the auxiliary switching and biasing circuits.

The composite signal from the FM detector is coupled to the base of Q4, via C1. This capacitor, in conjunction with the input impedance of the integrated circuit, gives an R-C time constant which will determine the minimum frequency response in the circuit, and consequently, the highest channel separation obtainable at the low frequency end of the audio spectrum.

In receivers where a strong high frequency roll-off of the composite signal is expected, parallel R-C compensation could be used in series with the input to improve channel separation at the high frequency end.

Transistor Q4 is used as an emitter follower to provide the high input impedance level needed in the IC to avoid any serious loading of the FM detector. Actually, due to the high degree of feedback provided by its associated emitter resistance, the input impedance is determined primarily by the 20 kilohm resistor connected between its base and the biasing network. The output of Q4 is fed to the detector, via Q6, another emitter follower stage, and to Q7, the 19 kHz amplifier.

For the recovery of the 19 kHz pilot signal, a parallel tuned circuit is used across the input of Q7. To further increase the overall selectivity of the circuit at 19 kHz, thus improving its noise immunity, a second high-Q resonant circuit is used at the output of this stage.

The combination Q8–Q9 acts as a high gain PNP transistor which couples the 19 kHz signal into the base of Q14, the frequency doubler, which has a high-Q parallel-tuned circuit for its collector load. The coil of this tuned circuit is tapped down to reflect a low impedance across the output of Q14. A 10:1 transformation sets an output impedance not higher than 2 kilohm, avoiding saturation of Q14. If higher impedances are used, the time symmetry of the 38 kHz signal could be lost and a severe degradation of the channel separation is to be expected.

A synchronous detector is used to demodulate the stereophonic information. When a stereo signal reaches the detector, the 38 kHz voltage developed across the doubler load will switch the transistors of the two upper differential pairs ON and OFF, according to the polarity of the driving signal. A time multiplexing of the composite stereo signal takes place (see Appendices I and II) at a

*NOTE: If the THD (stereo mode) of audio frequencies higher than 3 kHz is being evaluated using a distortion analyzer, values in excess of 1% will be recorded. This apparent discrepancy is due to the presence of spurious frequency by-products (beating between the 19 kHz pilot and the audio information) that fall in the harmonic frequency spectrum of the incoming audio signal, and are not attenuated by the frequency roll-off of the de-emphasis network. If a wave analyzer is used, a true reading for the THD, as well as the incidence of these by-products is obtained.

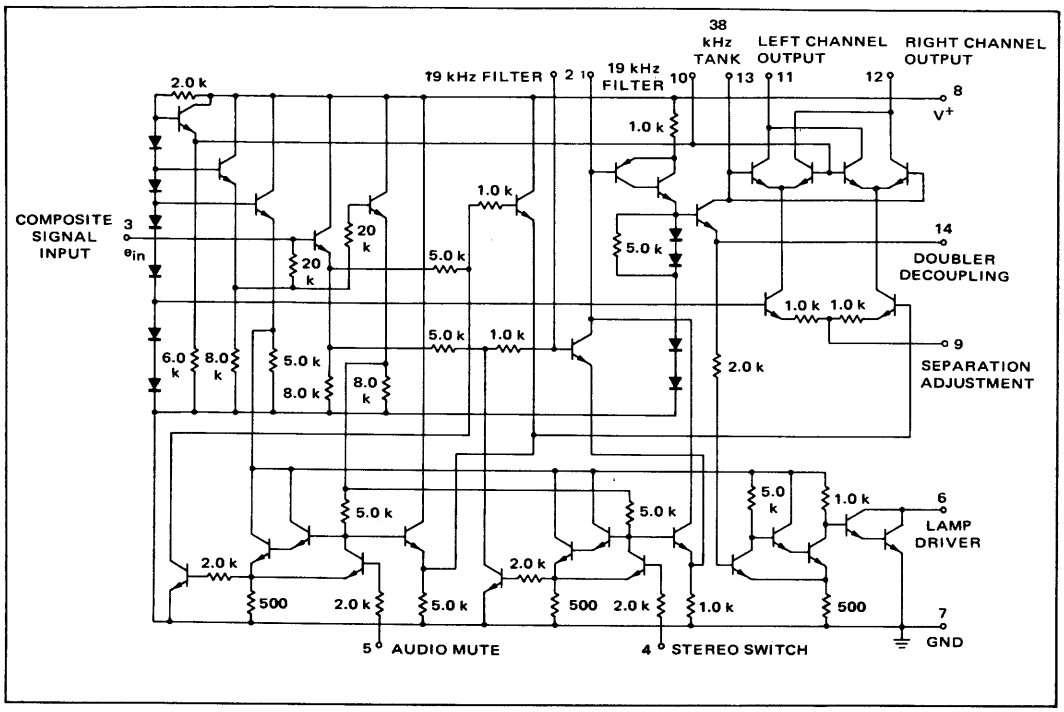


FIGURE 3 – MC1305 Circuit Schematic

38 kHz rate, permitting the separation of the left and right channel information.

The three resistors (R1, R2, and R3) associated with the lower pair in the synchronous detector help increase the channel separation by adding matrixing action to the decoding process (see Appendix II). As it was stated in the introduction, R3 becomes an external adjustable resistor.

An additional feature of this demodulator is its capability of cancelling, to a large extent, the ultrasonic components that otherwise would be present at the audio outputs when a stereo signal is being processed. This cancellation is obtained by combining two equal but opposite in-phase voltage variations in a given load, by cross coupling the collectors in the two upper pairs.

If the time symmetry of the 38 kHz square wave driving the detector is maintained by choosing the proper ac load for the doubler, no even harmonics of the 38 kHz drive will be present in the detector and, consequently, no SCA intermodulation will take place.

As could be expected, the degree of time-symmetry that can be obtained in a practical circuit has certain limitations. Even so, the minimum attenuation achieved in this circuit for any one of the SCA intermodulation products* (Table III) is not lower than 55 dB below the 1 kHz output level, obtained with an input signal of 200 mV(rms) (L = 0; R = 1 or vice versa).

This effective 67 kHz "built-in" trapping action makes it unnecessary to use an external SCA trap and, consequently, better channel separation is available at the high end of the audio range at lower cost.

The detector can also handle a monaural signal. In this case, the two upper differential pairs (Q10–Q12, and Q11–Q13) will be inactive and the monaural signal fed to the lower pair will be developed across the output load resistors, R_L and R_R, as for stereo (Figure 2).

The overall gain of the decoder could be made a function of the B+ voltage being used. When an 8.5 V power supply is used, the gain is very close to unity. If more gain is needed, the B+ voltage and the values used for R_L and R_R could be increased. The associated capacitors will have to be modified to preserve the 75 μs de-emphasis required by the system. In particular, if a 14 V B+ voltage is selected, $R_L = R_R = 10$ kilohm and the overall gain will be around 4.5 dB above the level obtained using an 8.5 V supply. A 6 dB lower output is to be expected when a stereo signal is processed using the monaural mode of operation.

AUXILIARY CIRCUITS

Three auxiliary circuits are incorporated in the MC1304. Each consists of an electronic switch associated with a Schmitt Trigger. This provides fast and positive switching after the respective threshold levels have been reached.

Muting and Stereo/Monaural Switches. Both the muting and the stereo/monaural switch are "normally closed"

*NOTE: See reference.

switches so they will open only if a minimum dc voltage is supplied to the proper terminal. The values required to turn the switches ON and OFF are given in Table IV.

If no voltage is supplied to these circuits, the muting switch and the stereo/monaural switch will ground points Ⓜ and Ⓢ (Figure 2) through Q17 and Q22, respectively.

To avoid overloading in these switching transistors, points Ⓜ and Ⓢ each have a 5.0 kilohm resistor in series with the driving source.

An effective ac grounding of the signal at Ⓜ makes it possible to obtain a high level of audio attenuation at the output of the decoder. This muting action can be achieved automatically. If this is the case, the dc voltages needed to turn the switch ON and OFF become a function of the S/N level of the incoming RF signal, as mentioned in "Circuit Considerations".

The Stereo Lamp Indicator. The stereo lamp indicator is connected internally and represents a "normally open" switch in series with the bulb and the power supply.

When a stereo signal is received, the dc voltage on the emitter of Q14 rises, triggering the switch ON.

The 19 kHz pilot level needed at the input of the IC to turn the stereo lamp indicator ON (pilot sensitivity) can be adjusted, within a certain range, by adding a resistor, R_A, in series with pin 1. This resistor will change the threshold level of the combination Q8–Q9. In a typical unit, the pilot sensitivity is increased by a factor of 2:1 by changing the value of the series resistance from 0 to 240 ohm (see Data Sheet).

The dc voltages required to turn this switch ON and OFF differ by 2 mV on the average, which is the built-in hysteresis mentioned before. The hysteresis assures a definite ON condition once the threshold level of the switch has been reached.

Functional Arrangements of the Auxiliary Circuits. The three auxiliary circuits can be combined in various ways to form different functional arrangements. Specific circuit considerations are discussed in a following section.

One of these arrangements has already been mentioned when referring to the automatic mute action. In this case only one switch has been considered at a time.

Other schemes, combining the action of two switches, are also available; for example, the mute switch could be driven using the dc voltage developed across the 38 kHz emitter decoupling network (pin 14). If this is the case, the mute driving voltage could be made low enough, under the absence of a stereo signal, as to keep the switch in the ON position, muting any monaural station as well as the interstation noise.

The short circuit between Ⓜ and ground decreases the effective emitter resistance in series with Q4, but still provides a high enough load to develop a substantial 19 kHz signal at the input of Q7 (pin 2) if a stereophonic signal is fed to the input. Accordingly, the dc voltage at pin 14 increases, triggering the mute switch OFF. The final result of this combination will be a receiver with a "stereo select" action, able to reject any monaural program automatically. When this combination is being used, the use of a stereo lamp indicator becomes redundant.

Stereo reception is poor when the signal to noise ratio is low, and it is, therefore, desirable to detect weak signals monaurally. Such action is easily obtained automatically by making the dc driving voltage applied to the stereo-monaural switch a fraction of that applied to the mute switch. The voltage divider is designed in such a way that any RF level below a predetermined point considered acceptable, will not provide enough dc voltage to switch the stereo-monaural switch into the stereo mode.

CIRCUIT EVALUATION

The circuit evaluation has been conducted using different levels of composite and pilot signal levels. The circuit used for this purpose is shown in Figure 4. The overall performance of a typical circuit is summarized in Tables I, II, III, IV, V and VI.

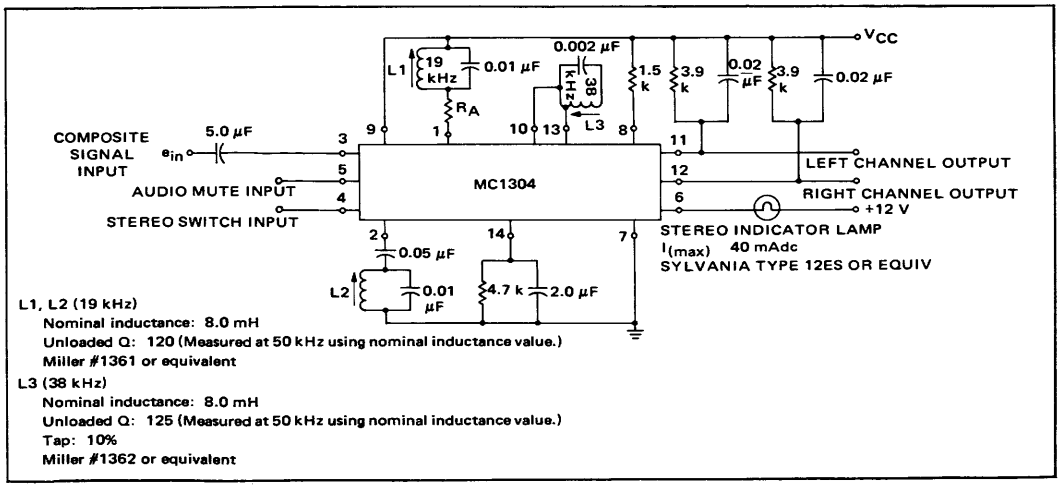


FIGURE 4 – Typical Circuit Configuration

TABLE I – Channel Separation versus Frequency

Input signal: 200 mVrms, 10% pilot (L = 1; R = 0 or vice versa)

Frequency	Channel Separation dB	
Hz	R = 1; L = 0	R = 0; L = 1
100	35	36
1000	47	46
10,000	34	35

TABLE II – Ultrasonic Frequency Rejection

(measured with respect to the 1 kHz level)

Input signal: 280 mV peak (L = -R), 10% pilot

Frequency	Attenuation
kHz	dB
19	31
38	23

TABLE III – 67 kHz SCA Rejection

(measured with respect to the 1 kHz level, without an input trap)

Input signal: 200 mVrms composite signal, 10% pilot adjusted to F.C.C. specs*

SCA Frequency	Frequency By-Products	Attenuation
kHz	kHz	dB
60	3	60
67	9	75
	10	75
74	2	70

*NOTE: 80% composite, 10% pilot; 10% SCA

TABLE IV – Auxiliary Circuits

Mute Switch	Typical Values
Minimum dc voltage to be applied to Pin 5 to turn the Mute OFF	1.5 V
Maximum dc voltage to be applied to Pin 5 to turn the Mute ON	0.7 V

Stereo-Monaural Switch

Minimum dc voltage to be applied to Pin 4 to have stereo operation	1.5 V
Maximum dc voltage to be applied to Pin 4 to have monaural operation	0.7 V

TABLE V – Channel Separation at 1 kHz versus Temperature

Ambient Temperature	1 kHz Channel* Separation	
°C	dB	
	R	L
25	46	46
55	40	48

*NOTE: Using polystyrene RPJ Centralab capacitors (Tol. ± 10%)

TABLE VI – 1 kHz Channel Separation versus Pilot Level

Pilot Level	Channel Separation
mVrms	dB
15	42
50	38
100	25

The data sheet on either the MC1304 or 1305 complements the information given above, showing the 19 kHz sensitivity of the unit and the THD performance, for both, the monaural and the stereo mode.

REFERENCE

Popp, D. J. – The study of SCA Interference in Stereo FM Receivers

IEEE Transactions on Broadcast and TV Receivers – July 1963

CIRCUIT CONSIDERATIONS

The incorporation of the MC1304 in an FM receiver calls for two basic considerations:

(A) The selection of the B+ voltages for the IC and lamp indicator.

(B) The derivation of the dc voltages needed to drive the mute and stereo-monaural switches.

A – POWER SUPPLY SELECTION

Two practical situations could occur: (a) The IC is being incorporated in an existing receiver where discrete components are being used; (b) An entirely new design is being worked out.

In the first case the selection of the B+ voltage for the IC and the lamp indicator will be mainly determined by the B+ availability of the receiver while in the case of a new design the gain of the multiplex unit could be the determining factor for the choice of the B+.

In any case, the B+ voltage for the IC should have some degree of regulation to overcome the usual variations on the main voltage (±10%). This regulation is needed because the percentage of THD in the unit is bias dependent. For this reason, independently of the value being chosen for the B+, the voltage between pin 8 and ground (MC1304) should be kept close to 4.6 V. This condition can be easily achieved selecting the proper value for the resistor connected between pin 8 and B+.

If an MC1305 is used instead, the B+ voltage should be 8.5 V because a 2 kilohm resistor (Figure 3) has been integrated on the chip.

The maximum dc current taken by the MC1304, under any B+ condition, never exceeds the 20 mA range.

For the lamp indicator the maximum B+ value is limited to 22 V because no higher voltage between any pin and ground is permitted (see maximum ratings). The type of lamp being used will determine the maximum load in the circuit. Care should be taken not to exceed the 40 mA maximum rating.

The use of separate supplies for the IC and the lamp driver is strongly recommended. This circuit approach simplifies the design of both power supplies and does away with the B+ modulation effect that, otherwise, will be present when switching the lamp indicator ON or OFF.

B – DERIVATION OF THE DC DRIVING VOLTAGES

The stereo lamp driver switch is the only switch that is driven internally. If automatic muting or stereo-monaural selection are required, the dc driving voltage to those circuits will have to be made dependent on the RF incoming signal.

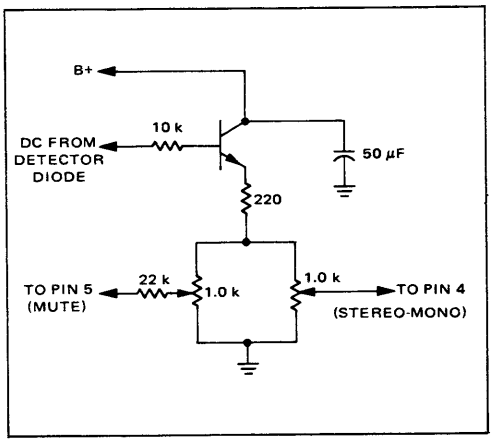


FIGURE 5 – Suggested Emitter Follower Circuit for Driving Voltages of Auxiliary Circuit Functions

Probably the most economical way to achieve this goal is to use the dc voltage available at the output of one of the ratio detector diodes (the one producing a dc voltage positive with respect to ground).

This voltage, due to the presence of filtering capacitances, is fairly immune to noise "spikes", a condition that is highly desirable when driving a Schmitt trigger switch. The only limitation for its usage is generally related to the available dynamic change of this dc voltage.

A minimum of 2:1 is required for the switch circuits. Obtaining the actual values are not usually a problem. The switch will remain in the mute mode if the value of the voltage applied to pin 5 is lower than 0.6 V, and it will change its state if this voltage becomes higher than 1.2 V. If the ratio is available, a voltage divider could be always designed to get the proper values.

In some receivers the sensitivity is too high, limiting the dynamic dc change to a ratio lower than 2:1. If this is the case, a small reduction of the sensitivity will be usually sufficient to improve the dynamic range. In a new design, of course, this problem could be contemplated from the start.

To avoid any loading from the IC, the auxiliary circuits could be isolated from the detector load using an emitter follower such as the one shown in Figure 5. This circuit permits an independent adjustment of the mute and stereo-monaural switches, which is desirable because they act at different RF signal levels.

APPENDIX I
SYNCHRONOUS DETECTOR WITH IMPROVED CHANNEL SEPARATION

To have a better understanding of how the synchronous detector in the MC1304 works, the detector is redrawn in Figure 1A, showing one of the outputs with solid lines and the other with dotted lines.

The pair Q15–Q16 is common to both channels.

Due to the inherent mechanism of a balanced pair, a phase inversion is always present between the two transistors in the pair.

In particular, as Q10 and Q13 are driven in parallel, there is a 180° phase shift between Q12 and Q13. A similar situation occurs between Q15 and Q16, in the lower pair.

The signal developed across R is the sum of two signal products. One is the product of the square wave present at Q13 and the signal present at Q16. The other is the product of the square wave present at Q12 and the signal present at Q15.

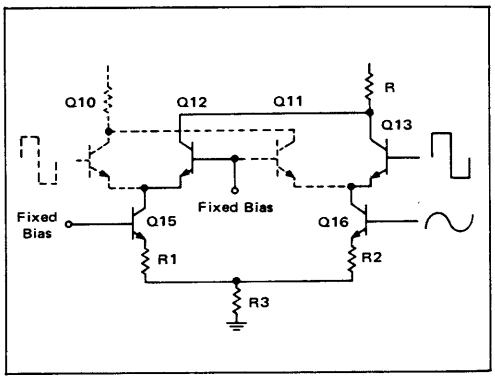


FIGURE 1A – Synchronous Detector

The signal at Q15 will be 180° out of phase with respect to Q16. Only a fraction (k) of the voltage fed to Q15 will be present at Q16, due to the presence of R1, R2, and R3. If both the square wave at Q13 and the composite signal at Q16 are assumed to have the same phase, then

$$V_{out} = \left|(L+R) + (L-R)\cos\omega_{sc}t\right|\left(1 + \frac{4}{\pi}\cos\omega_{sc}t\right) - k\left|(L+R) + (L-R)\cos\omega_{sc}t\right|\left(1 - \frac{4}{\pi}\cos\omega_{sc}t\right) \quad (1)$$

where: $[k] < 1$

If only the audio frequencies are being considered, the former expression becomes:

$$V_{out} = (L+R) + \frac{2}{\pi}(L-R) - k(L+R) + \frac{2k}{\pi}(L-R) \quad (2)$$

$$V_{out} = R\left(1 - \frac{2}{\pi} - k - \frac{2k}{\pi}\right) + L\left(1 + \frac{2}{\pi} - k + \frac{2k}{\pi}\right) \quad (3)$$

As can be seen, the output signal contains not only the wanted left channel information, but some unwanted right channel information. But this remainder is a function of the value given to k. In particular, if

$$1 - \frac{2}{\pi} - k - \frac{2k}{\pi} = 0 \qquad (4)$$

then an optimum value for k that cancels the crosstalk in the detector can be found.

$$k = \frac{\pi - 2}{\pi + 2} \cong 0.221 \qquad (5)$$

Replacing the value given by (5) in expression (3), we can find the value of the output signal:

$$V_{out} = \frac{8L}{2 + \pi} \qquad (6)$$

$$V_{out} = 1.55\ L \qquad (7)$$

A similar analysis could be done for the other channel.

APPENDIX II
ANALYSIS OF THE MATRIX CIRCUIT

The lower differential pair is redrawn in Figure 2A.

A variation of the incoming signal (Δe_i) is assumed to take place at the base of Q1. Considering the base of Q2 to be grounded for ac, and disregarding V_{BE} in both transistors, we will have:

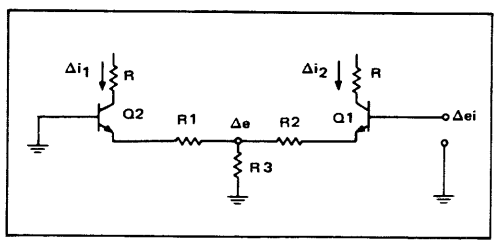


FIGURE 2A – Lower Differential Pair

$$\Delta e = \Delta e_i \frac{\frac{R_3 R_1}{R_3 + R_1}}{R_2 + \frac{R_1 R_3}{R_1 + R_3}}$$

Making

$$\frac{R_3 R_1}{R_3 + R_1} = P$$

and $R_2 + P = S$

then, $\Delta e = \Delta e_i \frac{P}{S}$

The value of Δi_2 will be given by

$$\Delta i_2 = \frac{\Delta e_i}{R_2 + \frac{R_3 R_1}{R_3 + R_1}}$$

or $\Delta i_2 = \frac{\Delta e_i}{S}$

For Δi_1 the value will be given by

$$\Delta i_1 = \frac{\Delta e}{R_1}$$

Then,

$$\frac{\Delta i_1}{\Delta i_2} = \frac{\Delta e}{R_1} \frac{S}{e_i} = \Delta e_i \frac{P}{S R_1} \quad \frac{S}{\Delta e_i}$$

or

$$\frac{\Delta i_1}{\Delta i_2} = \frac{\frac{R_3 R_1}{R_3 + R_1}}{R_1} = \frac{R_3}{R_3 + R_1}$$

in our circuit, $R_1 = 1.0\ k\Omega$

$R_2 = 1.0\ k\Omega$

$R_3 = 310\Omega$ (Three 930Ω resistors in parallel.)

Then,

$$\frac{\Delta i_1}{\Delta i_2} = \frac{310}{1{,}310} = 0.236$$

This value is a satisfactory approximation to the value needed for k as described in Appendix I.

AN-438
ANALYSIS AND DESIGN OF ACTIVE FILTERS USING OPERATIONAL AMPLIFIERS

INTRODUCTION

Frequency selective networks for use in the frequency range below 100 kHz have always been a problem. In this area of operation the inductors and capacitors required are large, both in value and physical size. Also, at these frequencies inductors and capacitors become quite lossy and the circuit Q's begin to suffer.

The answer to this problem is to exchange the large inductor and capacitor for a large block of gain, and use well known feedback principles to achieve selectivity with R-C active filters. Previously, to achieve a high degree of accuracy and circuit stability, a large number of active components was required in a fairly sophisticated circuit. Consequently, the design time and number of active components required made the use of active filters quite expensive.

The solution to this problem came with the advent of integrated circuits which allowed transistors to be "less expensive" than resistors. Now, excellent gain blocks can be fabricated at fairly reasonable costs. And as technology improves, the performance will continue to improve and the costs will continue decline, making the use of active filters very economical.

Although a great deal of work and investigation has been focused at placing the entire selectivity function on a single silicon chip, the large values of capacitors required in most instances has precluded this approach in all but the most specialized applications.

This paper discusses the use of operational amplifiers as gain blocks for active filters. A section on stability is also included along with various practical examples.

I. BASIC TWO-PORT ANALYSIS OF AN OPERATIONAL AMPLIFIER WITH FEEDBACK

Consider an operational amplifier (op-amp) and feedback in the form of two-port y parameters as shown in Figure 1.

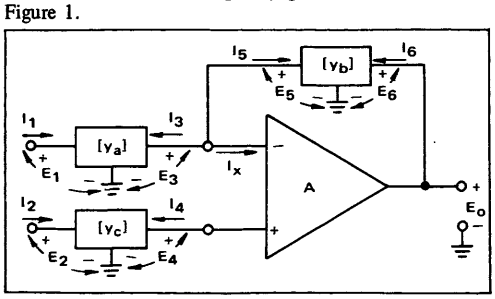


FIGURE 1 – Basic Two-Port Analysis of an Operational Amplifier with Feedback

For this network the following two-port equations can be written for the amplifier:

$$I_1 = y_{11_a} E_1 + y_{12_a} E_3 \quad (1.a)$$

$$I_3 = y_{21_a} E_1 + y_{22_a} E_3 \quad (1.b)$$

$$I_2 = y_{11_c} E_2 + y_{12_c} E_4 \quad (2.a)$$

$$I_4 = y_{21_c} E_2 + y_{22_c} E_4 \quad (2.b)$$

$$I_5 = y_{11_b} E_5 + y_{12_b} E_6 \quad (3.a)$$

$$I_6 = y_{21_b} E_5 + y_{22_b} E_6 \quad (3.b)$$

These equations can be manipulated to find the output voltage E_o, as a function of E_1, E_2, the y-parameters, and the open-loop gain, A. This approach is somewhat rigorous and the resulting equation would be too complicated to be of any practical use. However, with a few normally valid assumptions, the complexity of the solution for E_o is greatly reduced and results in a very simple and easily used form.

One assumption is that the input impedance of the operational amplifier is very large with the result that $I_x \approx 0$ and $I_4 \approx 0$. Then, from Equation (2.b),

$$E_4 = -E_2 \frac{y_{21_c}}{y_{22_c}} \quad (4)$$

also, because

$$I_x \approx 0, I_3 \approx -I_5. \quad (5)$$

Then from equations (1.b) and (3.a)

$$y_{21_a} E_1 + y_{22_a} E_3 = -y_{11_b} E_5 - y_{12_b} E_6. \quad (6)$$

Because the amplifier is assumed to have an extremely large open-loop gain ($A \rightarrow \infty$), the differential input signal, $E_3 - E_4$, required is very small. Assuming that $E_3 \approx E_4 \approx E_5$, then from Equation (4),

$$E_5 \approx -E_2 \left(\frac{y_{21_c}}{y_{22_c}}\right), \quad (7)$$

$$E_3 \approx -E_2 \left(\frac{y_{21_c}}{y_{22_c}}\right). \quad (8)$$

Substituting Equations (4), (7) and (8) into Equation (6) gives the following expression for the output voltage, E_6,

$$E_6 = -E_1\left(\frac{y_{21_a}}{y_{12_b}}\right) + E_2\left(\frac{y_{21_c}}{y_{22_c}}\right)\left(\frac{y_{11_b} + y_{22_a}}{y_{12_b}}\right) \quad , \quad (9)$$

as a function of the input voltages and the feedback networks. As a simple example to verify this equation, consider the amplifier shown in Figure 2.

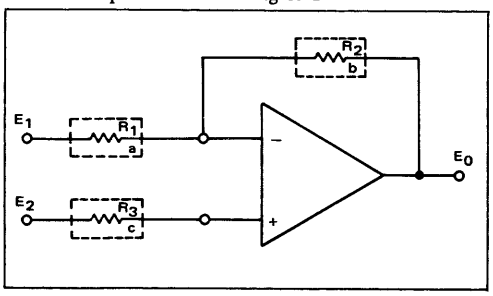


FIGURE 2 – Basic Example of Two-Port Analysis

For this example,

$$y_{21_a} = -\frac{1}{R_1} \quad y_{12_b} = -\frac{1}{R_2} \quad y_{21_c} = -\frac{1}{R_3} \quad ,$$

$$y_{22_a} = \frac{1}{R_1} \quad y_{11_b} = \frac{1}{R_2} \quad y_{22_c} = \frac{1}{R_3} \quad ,$$

Then from Equation (9),

$$E_O = -E_1\left(\frac{R_2}{R_1}\right) + E_2\left(1 + \frac{R_2}{R_1}\right) . \quad (10)$$

From this equation it is seen that for $E_2 = 0$ (inverting amplifier) the closed loop gain is the familiar expression:

$$\frac{E_0}{E_1} = -\frac{R_2}{R_1} \quad . \quad (11)$$

Similarly for $E_1 = 0$, the non-inverting gain is found to be,

$$\frac{E_0}{E_2} = 1 + \frac{R_2}{R_1} \quad . \quad (12)$$

For the discussion to follow, the inverting amplifier mode of operation ($E_2 = 0$) will be used because of its simplicity as seen in Equation (9). However, a similar discussion could be generated using the non-inverting mode with $E_1 = 0$. The purpose of the foregoing discussion was two-fold–first to generate a general equation for closed loop gain from which an active filter discussion might begin and second, to bring light upon the operation of an op-amp when feedback networks, other than pure resistive networks, are used in either mode of operation.

II. ACTIVE FILTER ANALYSIS

It should be noted that the expression for the closed loop gain in the inverting mode

$$\frac{E_0}{E_1} = -\frac{y_{21_a}}{y_{12_b}} \quad (13)$$

does not make any assumptions that the networks $[y_a]$, $[y_b]$ or $[y_c]$ are passive. Indeed, these networks could be active. For the case at hand, however, these networks will be considered to be passive, in which case

$$y_{21_b} = y_{12_b}$$

and equation (11) becomes

$$\frac{E_0}{E_1} = -\left(\frac{y_{21_a}}{y_{21_b}}\right) . \quad (14)$$

The synthesis of a particular frequency response curve will in most cases be done using RC networks in various combinations. For most applications these networks will be combinations of series or parallel connected resistors and capacitors as shown in Figure 3.

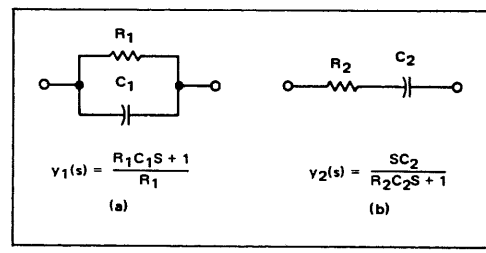


FIGURE 3

The problem of synthesizing filters with networks such as those shown in Figure 3 is not as futile as it may first appear.

From Equations (1.b) and (3.b), it is seen that

$$y_{21_a} = \left.\frac{I_3}{E_1}\right|_{E_3 = 0} \quad \text{and} \quad y_{21_b} = \left.\frac{I_6}{E_5}\right|_{E_6 = 0} . \quad (15)$$

This indicates that the synthesis problem reduces to that of finding the relationship between the input voltage and the short circuit output current. Or in other words, the problem has reduced in complexity from a two-port network to a one-port network.

For many circuits, the relationship between the short-circuit current and an impressed input voltage can be written by inspection of the circuit. For more complicated networks, simple Laplace transform methods may be required, or perhaps even the use of signal flow graphs, matrix algebra or state variables for extremely difficult problems.

The approach of this section will be to exploit a very simple, but often forgotten method of "working backwards" and also includes a discussion of a general method for finding y_{21}'s.

A. "Backwards Method"

This method is best explained with an example. Consider the network shown in Figure 4, where

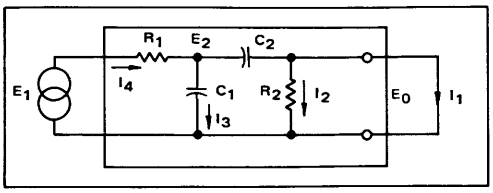


FIGURE 4 – Example of "Backwards Method"

It is necessary to find $y_{21} = \frac{I_1}{E_1}\Big|_{E_0 = 0}$.

Assume $I_1 = 1$ ampere. Because of the shorted output, $I_2 = 0$. $E_2(s)$ can be expressed as

$$E_2(s) = I_1 \left(\frac{1}{SC_2}\right) = \frac{1}{SC_2} \quad . \tag{16}$$

$I_3(s)$ can be expressed as

$$I_3(s) = E_2(s)\, SC_1 = \frac{SC_1}{SC_2} = \frac{C_1}{C_2} \quad . \tag{17}$$

It is known that

$$I_4 = I_1 + I_3 = 1 + \frac{C_1}{C_2} \tag{18}$$

and

$$E_1(s) = E_2(s) + I_4 R_1 \tag{19}$$

or

$$E_1(s) = \frac{1}{SC_2} + \left(1 + \frac{C_1}{C_2}\right) R_1 = \frac{SC_2 R_1 \left(1 + \frac{C_1}{C_2}\right) + 1}{SC_2} \tag{20}$$

Since this is the voltage function that will produce $I_1 = 1$, then

$$\frac{I_1}{E_1} = \frac{SC_2}{SC_2 R_1 \left(1 + \frac{C_1}{C_2}\right) + 1} = y_{21} \tag{21}$$

However, the direction of current for I_1 was assumed in the opposite direction from that which was derived in the two-port model, and hence, the sign on the transfer function must be changed. Then finally,

$$y_{21} = \frac{-SC_2}{SC_2 R_1 \left(1 + \frac{C_1}{C_2}\right) + 1} \quad . \tag{22}$$

This method does not require the use of long involved laplace equations for loops or nodes and greatly simplifies the algebra involved.

B. General Method

A procedure for finding the forward transfer admittance for any generalized network can be found by considering an application of Kirchhoffs voltage law with a slight modification. Consider a generalized network consisting of k loops with $I_1, I_2, \ldots I_k$ being the transforms of the loop currents, and $V_1, V_2, \ldots V_k$ the transforms of the driving voltage in each loop respectively.

Application of Kirchhoffs voltage law results in k simultaneous equations

$$V_1 = Z_{11}I_1 + Z_{12}I_2 + \ldots Z_{1k}I_k$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2 + \ldots Z_{2k}I_k$$

$$\vdots$$

$$V_k = Z_{k1}I_1 + Z_{k2}I_2 + \ldots Z_{kk}I_k \tag{23}$$

where Z_{ii} = total impedance around the i-th loop and Z_{ij} = the total impedance common to the i-th loop and the j-th loop.

For the case under discussion, only one voltage source, V_1, is present and hence, $V_k = 0$ for $k \neq 1$.

The problem is now to find I_k, the output current, when the output terminal is shorted. It should be noted that by shorting the output terminals, a modification to Z_{kk} must be made. Once this modification to Z_{kk} is made, the transfer function can be found by solving the determinant.

To demonstrate this, consider the following two examples.

Example 1

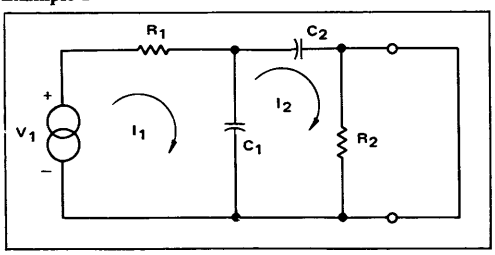


FIGURE 5 – Circuit of Example 1

For the circuit of Figure 5 we have the following:

$$Z_{11} = R_1 + \frac{1}{SC_1}$$

$$Z_{12} = \frac{-1}{SC_1}$$

$$Z_{21} = -\frac{1}{SC_1} \tag{24}$$

with the output shorted Z_{22} becomes

$$Z_{22} = \frac{1}{SC_1} + \frac{1}{SC_2} \quad . \tag{25}$$

Solving for $\frac{I_2}{V_1}$,

$$\frac{I_2}{V_1} = \frac{\begin{vmatrix} (R_1 + \frac{1}{SC_1}) & 1 \\ (-\frac{1}{SC_1}) & 0 \end{vmatrix}}{\begin{vmatrix} (R_1 + \frac{1}{SC_1})(-\frac{1}{SC_1}) & \\ (-\frac{1}{SC_1})(\frac{1}{SC_1} + \frac{1}{SC_2}) & \end{vmatrix}} = \frac{SC_2}{SC_2R_1(1 + \frac{C_1}{C_2}) + 1} \quad (26)$$

Again adding the minus sign, it is seen that this is the same result obtained for the previous "backwards" example for Figure 4.

Example 2

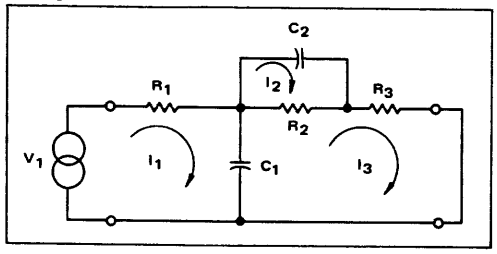


FIGURE 6 – Circuit of Example 2

Consider a slightly more complicated network as shown in Figure 6.

For this network,

$$Z_{11} = R_1 + \frac{1}{SC_1},\ Z_{21} = 0,\ Z_{31} = \frac{-1}{SC_1}$$

$$Z_{12} = 0,\ Z_{22} = R_2 + \frac{1}{SC_2},\ Z_{32} = -R_2$$

$$Z_{13} = -\frac{1}{SC_1},\ Z_{23} = -R_2,\ Z_{33} = R_2 + R_3 + \frac{1}{SC_1}.$$

Then

$$\frac{I_3}{V_1} = \frac{\begin{vmatrix} (R_1 + \frac{1}{SC_1}) & 0 & 1 \\ 0 & (R_2 + \frac{1}{SC_2}) & 0 \\ -\frac{1}{SC_1} & -R_2 & 0 \end{vmatrix}}{\begin{vmatrix} (R_1 + \frac{1}{SC_1}) & 0 & -\frac{1}{SC_1} \\ 0 & (R_2 + \frac{1}{SC_2}) & -R_2 \\ -\frac{1}{SC_1} & -R_2 & (R_2 + R_3 + \frac{1}{SC_1}) \end{vmatrix}}. \quad (27)$$

Solution of this determinant gives

$$\frac{I_3}{V_1} = \frac{k_0(S + \omega_1)}{S^2 + a\omega_2 + (\omega_2)^2}, \quad (28)$$

where

$$K_o = \frac{1}{R_1R_3C_1},\quad \omega_1 = \frac{1}{R_2C_2}$$

$$(\omega_2)^2 = \frac{R_1 + R_2 + R_3}{R_1R_2R_3} \cdot \frac{1}{C_1C_2}$$

$$a = \frac{R_1(R_2 + R_3)C_1 + R_2(R_1 + R_3)C_2}{\sqrt{R_1R_2R_3(R_1 + R_2 + R_3)C_1C_2}}.$$

The short circuit transfer admittances of a number of second-order RC networks are given Figure 7.

III. THE PROBLEM OF SYNTHESIS

A great deal of work has been done concerning the problem of passive network synthesis. Unfortunately, most of the effort to date has been concerned with synthesis of driving point impedances, matching networks, and voltage transfer functions. Very little literature is available concerning the synthesis of transfer admittances. However, a basic approach to the problem follows.

If networks $[y_a]$ and $[y_b]$ are passive RC networks, their poles will be on the negative real axis of the complex frequency plane; however, the zeros of the transfer admittances of $[y_a]$ and $[y_b]$ can be located anywhere in the complex frequency plane. From this, it can be concluded that if the poles of y_{21_a} are the same as the poles of y_{21_b}, the denominators of Equation (14) will cancel and almost any desired pole-zero configuration can be synthesized.

In mathematical terms, this means that y_{21_a}, is chosen as

$$y_{21_a} = \frac{P(s)}{Q(s)},$$

and

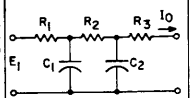
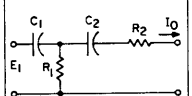
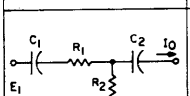
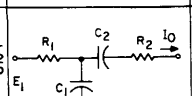
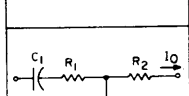
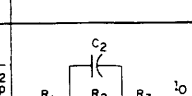
$$y_{21_b} = \frac{R(s)}{Q(s)}.$$

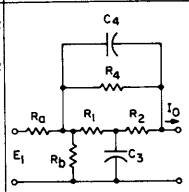
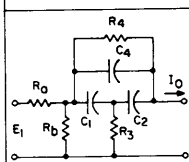
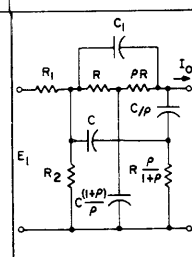
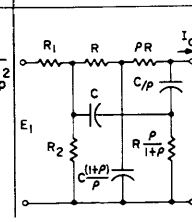
then

$$E_0 = -\left(\frac{y_{21_a}}{y_{21_b}}\right) = -\frac{P(s)}{R(s)}.$$

This is the general method. Simplicity and ease of calculation will, however, always dictate the approach used. For example, suppose it is required to synthesize the following filter response:

Transfer Admittance of Some Representative Second-Order RC Networks †

TRANSFER ADMITTANCE	RC NETWORK	PARAMETER–COMPONENT RELATIONS
(1) $K_R \frac{1}{s^2+\frac{\omega_p}{q_R}s+\omega_p^2}$		$K_R = \frac{1}{R_1R_2R_3C_1C_2}$ $\omega_p^2 = \frac{R_1+R_2+R_3}{R_1R_2R_3C_1C_2}$ $q_R = \frac{\sqrt{R_1R_2R_3(R_1+R_2+R_3)C_1C_2}}{R_1(R_2+R_3)C_1+R_3(R_1+R_2)C_2}$
(2) $K_R \frac{s^2}{s^2+\frac{\omega_p}{q_R}s+\omega_p^2}$		$K_R = \frac{1}{R_2}$; $\omega_p^2 = \frac{1}{R_1R_2C_1C_2}$ $q_R = \frac{\sqrt{R_1R_2C_1C_2}}{R_1(C_1+C_2)+R_2C_2}$
		$K_R = \frac{1}{R_1}$; $\omega_p^2 = \frac{1}{R_1R_2C_1C_2}$ $q_R = \frac{\sqrt{R_1R_2C_1C_2}}{(R_1+R_2)C_1+R_2C_2}$
(3) $K_R \frac{s}{s^2+\frac{\omega_p}{q_R}s+\omega_p^2}$		$K_R = \frac{1}{R_1R_2C_1}$; $\omega_p^2 = \frac{1}{R_1R_2C_1C_2}$ $q_R = \frac{\sqrt{R_1R_2C_1C_2}}{R_1(C_1+C_2)+R_2C_2}$
		$K_R = \frac{1}{R_1R_2C_2}$; $\omega_p^2 = \frac{1}{R_1R_2C_1C_2}$ $q_R = \frac{\sqrt{R_1R_2C_1C_2}}{(R_1+R_2)C_1+R_2C_2}$
(4) $K_R \frac{s+\omega_z}{s^2+\frac{\omega_p}{q_R}s+\omega_p^2}$		$K_R = \frac{1}{R_1R_3C_1}$; $\omega_z^2 = \frac{1}{R_2C_2}$ $\omega_p^2 = \frac{R_1+R_2+R_3}{R_1R_2R_3}\ \frac{1}{C_1C_2}$ $q_R = \frac{\sqrt{R_1R_2R_3(R_1+R_2+R_3)C_1C_2}}{R_1(R_2+R_3)C_1+R_2(R_1+R_3)C_2}$

TRANSFER ADMITTANCE	RC NETWORK	PARAMETER–COMPONENT RELATIONS
(5) $K_R \frac{s^2+\frac{\omega_z}{q_z}s+\omega_z^2}{s^2+\frac{\omega_p}{q_R}s+\omega_p^2}$		$K_R = \frac{1}{R_a}$; $\omega_z^2 = \frac{1}{R_pR_qC_3C_4}$ $q_z = \frac{\sqrt{\left(1+\frac{R_4}{R_1+R_2}\right)R_pR_4C_3C_4}}{R_pC_3+R_4C_4}$ $\omega_p^2 = \frac{1}{R_pR_qC_3C_4}\left(1+\frac{R_q}{R_m}\right)$ $q_R = \frac{\sqrt{\left(1+\frac{R_4}{R_1+R_2}\right)\left(1+\frac{R_q}{R_m}\right)R_pR_4C_3C_4}}{R_4C_4+R_pC_3\left[1+\frac{R_4}{R_1}+\frac{R_4}{R_m}\right]}$ WHERE $R_p = \frac{R_1R_2}{R_1+R_2}$ $R_m = \frac{R_aR_b}{R_a+R_b}$; $R_q = \frac{R_4(R_1+R_2)}{R_1+R_2+R_4}$
		$K_R = \frac{1}{R_a}$; $\omega_z^2 = \frac{1}{R_3R_4C_pC_q}$ $q_z = \frac{\sqrt{R_3R_4C_pC_q}}{R_3C_p+R_4C_4}$, $\omega_p^2 = \frac{1+R_4/R_m}{R_3R_4C_pC_q}$ $q_p = \frac{\sqrt{(1+R_4/R_m)R_3R_4C_pC_q}}{(1+R_4/R_m)R_3C_p+R_4(C_1+C_4)}$ WHERE: $C_p = C_1+C_2$ $C_q = C_4+\frac{C_1C_2}{C_1+C_2}$; $R_m = \frac{R_aR_b}{R_a+R_b}$
		$K_R = \frac{1}{R_1}$; $\omega_z^2 = \frac{1}{R^2C^2[1+\alpha]}$ $q_z = \frac{\sqrt{1+\alpha}}{\alpha}$; $\omega_p^2 = \frac{1+\beta}{R^2C^2[1+\alpha]}$ $q_R = \frac{\sqrt{(1+\alpha)(1+\beta)}}{\alpha+\beta+2(1+\rho)}$ WHERE: $\alpha = \frac{C_1(1+\rho)}{C}$ $\beta = R(1+\rho)/\frac{R_1R_2}{R_1+R_2}$
(6) $K_R \frac{s^2+\omega_z^2}{s^2+\frac{\omega_p}{q_R}s+\omega_p^2}$		$K_R = \frac{1}{R_1}$; $\omega_z = \frac{1}{RC}$ $\omega_p^2 = \frac{1}{R^2C^2}[1+(1+\rho)\alpha]$ $q_R = \frac{1}{1+\rho}\frac{\sqrt{1+(1+\rho)\alpha}}{2+\alpha}$ WHERE: $\alpha = R/\frac{R_1R_2}{R_1+R_2}$

†Courtesy of G. S. Moschytz from "Active RC Filter Building Blocks Using Frequency Emphasizing Networks." June 1967, IEEE Journal of Solid-State Circuits.

FIGURE 7

$$\frac{E_{0(s)}}{E_1} = \frac{-5(S+100)(S+10{,}000)}{(S+500)(S+1000)} = \frac{-5(S^2+10.1\times10^3 S+10^6)}{(S+500)(S+1000)}$$

The straight line Bode approximation of this function is shown in Figure 8.

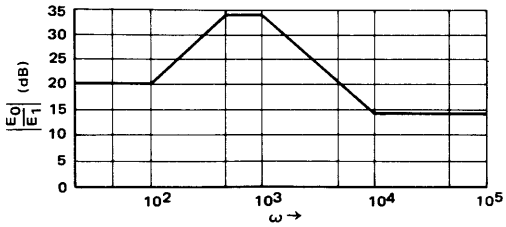


FIGURE 8 – Bode Plot of $\frac{E_0}{E_1} = \frac{5(S+100)(S+10{,}000)}{(S+500)(S+1000)}$

Next, consider the transfer admittance which results when the networks shown in Figure (3.a) and (3.b) are connected in parallel.

$$y_T(s) = y_1(s) + y_2(s) = \frac{R_1C_1S+1}{R_1} + \frac{SC_2}{R_2C_2S+1}$$

or

$$y_T(s) = \frac{C_1\left[S^2 + S\left(\frac{1}{R_2C_2}+\frac{1}{R_1C_1}+\frac{1}{R_2C_1}\right)+\frac{1}{R_1C_1R_2C_2}\right]}{\left[s+\frac{1}{R_2C_2}\right]}.$$

If we let this be the transfer function for $y21_a$, and use the network of Figure 3.a for the feedback $y21_b$, then the overall transfer function becomes

$$\frac{E_{0(s)}}{E_1} = \frac{C_1\left[S^2+S\left(\frac{1}{R_2C_2}+\frac{1}{R_1C_1}+\frac{1}{R_2C_1}\right)+\frac{1}{R_1C_1R_2C_2}\right]}{C_3\left[S+\frac{1}{R_2C_2}\right]\left[S+\frac{1}{R_3C_3}\right]}$$

For this problem,

(a) $\frac{1}{R_2C_2} = 500$

(b) $\frac{1}{R_3C_3} = 1000$

(c) $\frac{1}{R_1C_1R_2C_2} = 10^6$

(d) $\frac{1}{R_2C_2}+\frac{1}{R_1C_1}+\frac{1}{R_2C_1} = 10.1\times10^3.$

Also, from the dc gain considerations,

$$\left.\frac{y21_a}{y21_b}\right|_{s=0} = 10 = \frac{R_3}{R_1}, \qquad (29)$$

or

$R_3 = 10R_1.$

Since there are five independent equations and six unknowns, one unknown may be arbitrarily chosen from which the remaining five can be calculated.

Let $R_2 = 1\ k\Omega$

Then,

$C_2 = 2\ \mu F$

$C_1 = 0.1315\ \mu F$

$R_1 = 38\ k\Omega$

$R_3 = 3.8\ k\Omega$

$C_3 = 0.0265\ \mu F$

The circuit to synthesize this transfer function is shown in Figure 9.

A very important point should be made at this time. The impedance which is used to terminate the non-inverting (+) input should be the *dc Thevenin equivalent resistance* that is found by "standing" at the inverting (–) input and looking back away from the amplifier. By doing this, one eliminates the dc output offset voltage component that is due to the bias current of the amplifier. Thus, for the first stage the dc Thevenin resistance is the parallel combination of a 3.8 kΩ resistor and a 38 kΩ resistor, hence a standard value resistor of 3.6 k has been used.

Another and perhaps more expedient approach to this problem would be to use the Motorola MC1437P Dual Operational Amplifier and take advantage of the isolation properties between the amplifiers. If this is done, the original transfer function can be broken up into two transfer functions and the calculations become very simple.

That is,

$$\frac{E_0}{E_1} = \frac{E_{01}}{E_1}\cdot\frac{E_0}{E_{01}} \qquad (30)$$

where

$$\frac{E_{01}}{E_1} = \frac{-5(S+100)}{(S+500)}, \quad \frac{E_0}{E_{01}} = \frac{-(S+10{,}000)}{(S+1000)}. \qquad (31)$$

For the first amplifier,

$$\frac{E_{01}}{E_1} = \frac{-5(S+100)}{(S+500)} = \left(-\frac{y21_a}{y21_b}\right). \qquad (32)$$

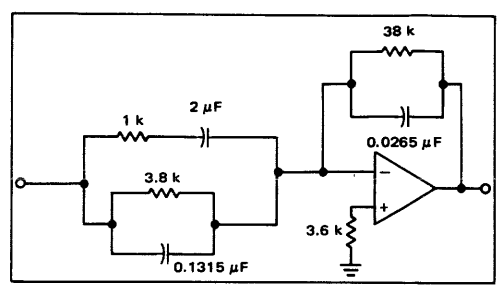


FIGURE 9

Figure 3 shows that a parallel RC network for both networks will provide the desired response as shown in Figure 10.

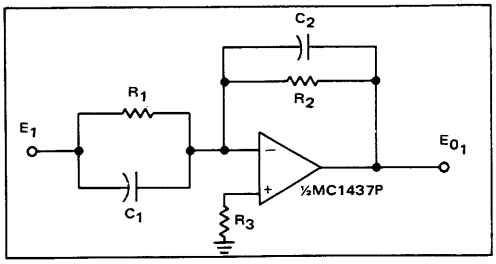


FIGURE 10 – Parallel RC Feedback Example

Using a parallel RC network for both y_{21_a} and y_{21_b} as shown in Figure 10, Equation 33 can be written.

$$\frac{E_{01}}{E_1} = -\frac{y_{21_a}}{y_{21_b}} = -\frac{\frac{R_1C_1S+1}{R_1}}{\frac{R_2C_2S+1}{R_2}} = -\frac{C_1}{C_2}\frac{\left(S+\frac{1}{R_1C_1}\right)}{\left(S+\frac{1}{R_2C_2}\right)} \quad (33)$$

where

$$\frac{C_1}{C_2} = 5, \quad \frac{1}{R_1C_1} = 100, \quad \frac{1}{R_2C_2} = 500.$$

When one of the components has been selected the others can then be found. Therefore, suppose an additional requirement is imposed that the input impedance for a dc input must be at least 10 kΩ. Since the inverting operational amplifier input impedance is simply the impedance placed between the voltage source and the inverting terminal, the dc impedance is merely R1. The problem is now to select components which are standard or near standard values. If R1 is selected to be 16 kΩ, then $C1 \approx \frac{C1}{5} = 0.02\ \mu F$, from which R2 can be found to be 16 kΩ also.

The second amplifier can be analyzed in a similar straight forward manner with the resulting circuit shown in Figure 11.

This gives rise to a second point that should be made. The dc gain of the first stage is unity and as a consequence the amplifier has been compensated for unity gain as suggested on the data sheet. The dc gain of the second stage is 10 and subsequently, the amplifier is compensated for a gain of 10 as suggested on the data sheet. Both compensation networks are shown in Figure 11. Without compensation, instability may occur–in fact is may occur anyway. The investigation of this is found in the next section.

IV. STABILITY CONSIDERATIONS

Consider the basic negative feedback circuit as shown in Figure 12.

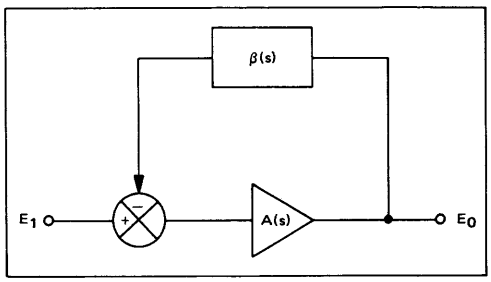


FIGURE 12

For this circuit, the closed loop gain is given by:

$$\frac{E_0}{E_1} = \frac{A(s)}{1 + A(s)\,\beta(s)}, \quad (34)$$

and the characteristic equation for stability is

$$C(s) = 1 + A(s)\,\beta(s). \quad (35)$$

When C(s) = 0, that is to say,

$$A(s)\,\beta(s) = 1\angle 180^{o} \quad (36)$$

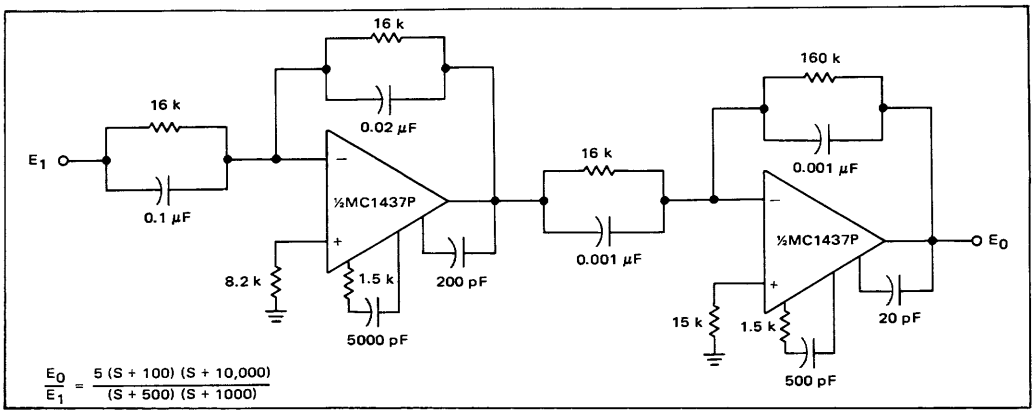


FIGURE 11 – A Resulting Filter Using a Dual Operational Amplifier.

The closed loop system is unstable. To investigate this, the problem becomes one of finding β (s) in terms of the feedback y-parameters since the properly compensated open-loop amplifier function, A (s), is usually known and can be approximated as

$$A(s) = \frac{-A\omega_0}{S + \omega_0}, \quad (37)$$

where A is the dc open loop gain of the amplifier given on the data sheet (AVOL) and ω_0 is the open loop −3 db break frequency for the compensated amplifier, also given in curves on the data sheet for various compensation networks.

To find the expression for $\beta(s)$ consider Figure 13:

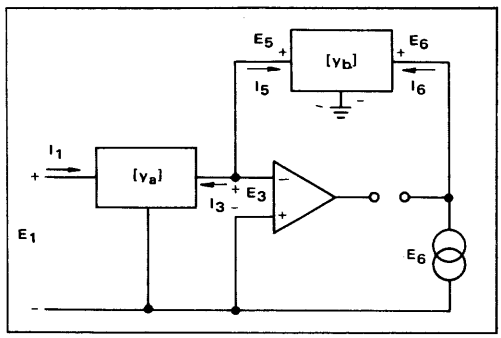


FIGURE 13

By definition of $\beta(s)$, we must find

$$\beta(s) = \frac{E_3}{E_6}. \quad (38)$$

From Equation (1.b), with E1 = 0 we have

$$I_3 = y_{22_a} E_3.$$

Analogous to the discussion of Section I,

$$I_3 = -I_5$$

and

$$E_3 = E_5.$$

Substituting these expressions into Equation (3.a) we have

$$-y_{22_a} E_3 = y_{11_b} E_3 + y_{21_b} E_6,$$

or

$$\frac{E_3}{E_6} = \frac{-y_{12_b}}{y_{22_1} + y_{11_b}} = \beta(s) \quad (39)$$

Knowing $\beta(s)$, we can now find the stability conditions. From Equation (36),

$$\frac{A\omega_0}{S + \omega_0} \cdot \frac{y_{12_b}(s)}{y_{22_a}(s) + y_{11_b}(s)} = 1 < 180^0$$

For

$$\beta(s) = \frac{a_n s^n + a_{n-1} s^{n-1} + \ldots . a_1 s + a_0}{b_m s^m + b_{m-1} s^{m-1} + \ldots . b_1 s + b_0}.$$

The stability criteria becomes,

(i) m = n unconditional stability

(ii) m ≥ n+1 conditional or marginal stability

Example 1

As an example of this stability discussion, consider the filter network of Figure 14.

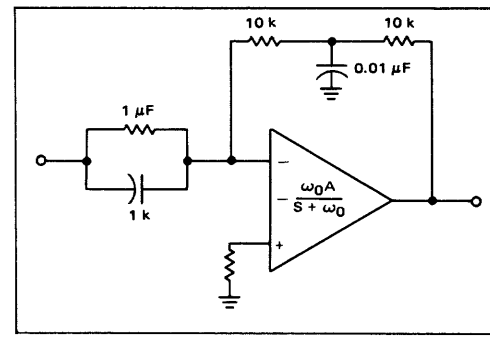


FIGURE 14.

For the network of Figure 14,

$$y_{22_a} = 10^{-6}(S + 10^3),$$

$$y_{11_b} = \frac{10^{-4}(S + 10^4)}{(S + 2 \times 10^4)},$$

$$y_{12_b} = \frac{-1}{(S + 2 \times 10^4)},$$

Solving for $\beta(s)$ gives

$$\beta(s) = \frac{-10^2}{S^2 + 1.11 \times 10^4 S + 1.1 \times 10^7} = \frac{-100}{(S + 10^4)(S + 1.1 \times 10^3)},$$

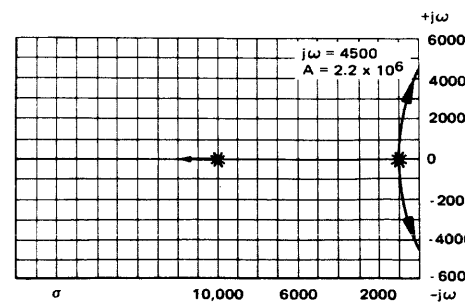


FIGURE 15 – Root Locus for

$$A(s)\,\beta(s) = \frac{10^5 A}{(S + 10^3)(S + 1.1 \times 10^3)(S + 10^4)}$$

and

$$A(s)\,\beta(s) = \frac{100\omega_0 A}{(S+\omega_0)(S+10^4)(S+1.11\times10^3)}\ .$$

Assume that the operational amplifier has been compensated such that $\omega_0 = 10^3$.

Then,

$$A(s)\,\beta(s) = \frac{10^5 A}{(S+10^3)(S+10^4)(S+1.1\times10^3)}\ . \qquad (40)$$

The root locus for this function is shown in Figure 15. From the root locus, the frequency at which the poles just cross the $j\omega$ axis is found to be 4500 rad/sec. Letting S = j4500 in Equation 40 and setting the magnitude of the equation equal to 1 will determine the open loop gain "A" that will make the system unstable:

$$1 = \frac{10^5 A}{|1+j4.5|\ |10+j4.5|\ |1.1+j4.5|\ 10^9}.$$

Solving for "A",

$$A = 2.2\times10^6.$$

From this result we can deduce two things: (1) most operational amplifiers on the market ($A_{OL} < 10^6$) would be stable in this application,(2) an "ideal" op amp ($A_{OL} = \infty$) would oscillate!

Example 2

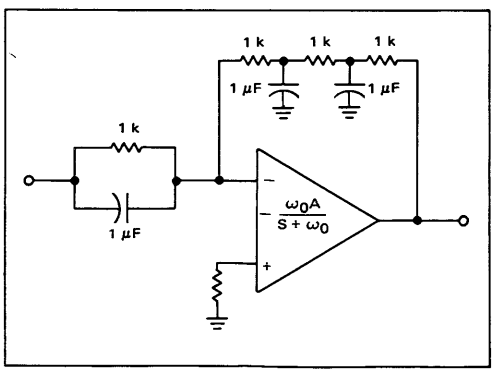


FIGURE 16 – Network for Stability Example Number 2.

For the network shown in Figure 16,

$$y22_a = 10^{-6}(S+10^3)$$

$$y21_b = \frac{-10^3}{S^2+4\times10^3 S+3\times10^6}$$

$$y11_b = \frac{S_2+3\times10^3 S+10^6}{10^3(S^2+4\times10^3 S+3\times10^6)}\ .$$

Solving for $\beta(s)$,

$$\beta(s) = \frac{10^9}{(S+2\times10^3)(S+3.4\times10^3)(S+5.9\times10^2)}\ .$$

If it is assumed that

$$\omega_0 = 8\times10^2.$$

the value of open loop gain that will make the closed loop system oscillate can be found in a similar fashion as Example 1. For this example,

$$A = 38\ .$$

The root locus plot of this example is shown in Figure 17.

To perform a filter function with this network would be idiocy.

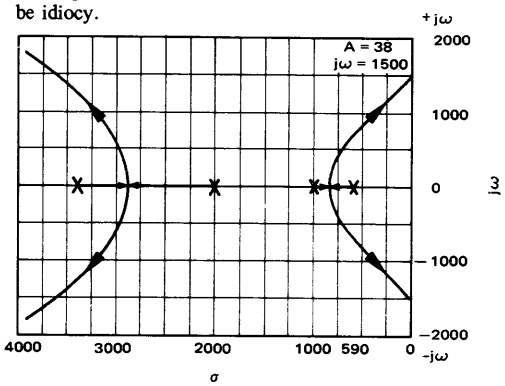


FIGURE 17 – Root Locus Plot

$$\frac{8\times10^{11} A}{(S+8\times10^2)(S+2\times10^3)(S+2.3\times10^3)(S+5.9\times10^2)}$$

V. PRACTICAL DESIGN EXAMPLE

It was required that a filter be designed for a phase locked loop frequency synthesizer that meets the following specifications:

(a). dc Voltage Gain 15 V/V

(b). Reference frequency (5 kHz) at least 70 dB down from dc gain

(c). First harmonic of the reference frequency (10 kHz) at least 60 dB down from dc gain

(d). All other harmonics of the reference frequency (15 kHz, 20 kHz, etc.) at least 50 dB down.

Examination of Figure 7 shows that an infinite Q zero (for ideal components) can be achieved using the circuit shown for circuit #6. It is also noted that at the zero, a positive 180° phase shift occurs, with the overall phase shift at $\omega = \rightarrow \infty$ being 0°. It was decided that two such networks might be connected in tandem using the MC1437P dual operational amplifier with the first notch set at 5 kHz and the second notch set at 10 kHz. However, each network of #6 also contains two poles which must be taken into account. It was then decided that the best way to handle this problem was to place a two section RC network on the output of the op amp to roll off the high frequency components. The overall design is shown in Figure 18.

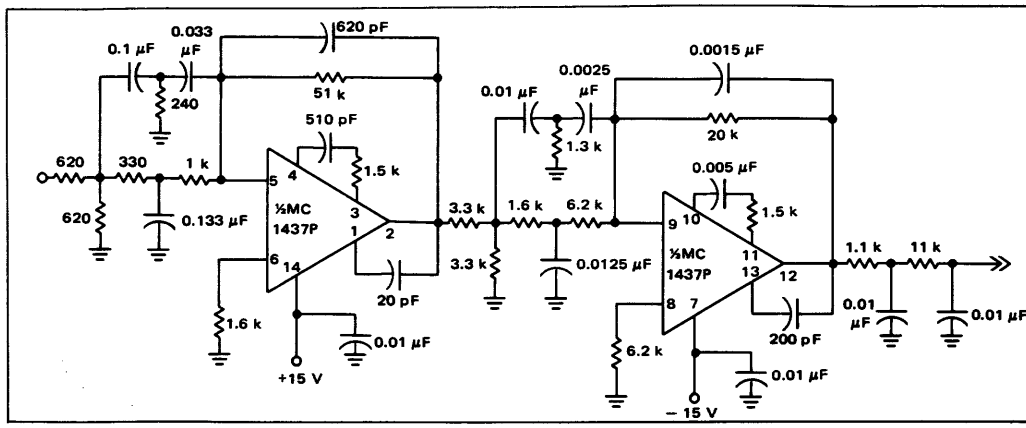


FIGURE 18 – Dual Notch Filter.

From Figure 7

$$T(s) = \frac{K_R (S^2 + \omega_z^2)}{S^2 + \frac{\omega_p}{q_R} S + \omega_p^2}$$

where

$$K_R = \frac{1}{R_1}$$

$$\omega_z = \frac{1}{RC}$$

$$\omega_p^2 = \frac{[1 + (1 + \rho)\, a]}{R^2C^2}$$

$$q_R = \frac{1}{1 + \rho} \cdot \frac{\sqrt{1 + (1 + \rho)\, a}}{(2 + a)}$$

$$a = \frac{R}{\left(\frac{R_1 R_2}{R_1 + R_2}\right)}$$

The calculations for the first network are as follows:

(a) $\omega_z = \frac{1}{RC} = (2\pi)\,(5\text{ kHz})$

Arbitrarily select R = 330Ω from which C is found to be C ≈ 0.1 μF

(b) Choose $R_1 = R_2 = 620\Omega$

Then "a" is calculated to be

$$a = \frac{R}{\left(\frac{R_1 R_2}{R_1 + R_2}\right)} = \frac{330}{310}$$

a = 1.06

(c) The next step is to find a value for ρ which will place the poles of T(s) on both sides of the notch. By trial and error, a value of ρ = 3 was selected.

(d) For ρ = 3, the following were found

$\omega_p = 2.29\ \omega_z = (2\pi)\,(11.45\text{ kHz})$

$q_R = 0.187$

and the poles of T(s) are

$S_1 = (2\pi)\,(59\text{ kHz})$

$S_2 = (2\pi)\,(2.29\text{ kHz})$

From a noise consideration, it is advantageous to put the majority of the overall gain in the first stage. Therefore, a feedback resistor for the first stage was found that would give a dc gain of 15 V/V. This calculation is straightforward and is explained as follows:

Setting S = 0 in the expression for T(s) gives a dc transfer admitttnce of

$$y21_a\Big|_{s=o} = \frac{(\omega_2)^2}{R_1\, \omega_p^2}$$

substituting the values of ω_z, ω_p and R1 into this equation gives

$$y21_a\Big|_{s=o} = \frac{1}{3.2\ 8k\Omega}$$

Recall

$$\frac{E_0}{E_1} = 15 = \frac{y21_a}{y21_b} = \frac{\frac{1}{3.28\text{ k}\Omega}}{\frac{1}{R_F}}$$

Solving for R_F

$R_F = 49.3\text{ k}\Omega$

A standard value of 51 kΩ was selected.

If a capacitor is placed in shunt across the feedback resistor, a greater amount of negative feedback occurs to an AC signal and consequently reduces the gain as the frequency is increased. This will give additional high frequency roll off to the filter. In each stage, the value of this capacitor was selected such that

$$\frac{1}{R_F C_F} = (2\pi)\ (5\ \text{kHz})\ .$$

The calculations for the 2-section RC network are fairly straight-forward. The criteria for component selection was to choose the two poles to both be at about 7 kHz to roll of the high frequency harmonics.

The design of the second active filter proceeds exactly as the previous explanation with the notch set at 10 kcps.

It should be pointed out that the second amplifier is operating at unity gain and is compensated for such operation. The first stage is operating at a gain of 15 V/V and so has been compensated for a gain of about 15 V/V. The overall frequency response is shown in Figure 19. It is easily seen that all of the design specifications have been met.

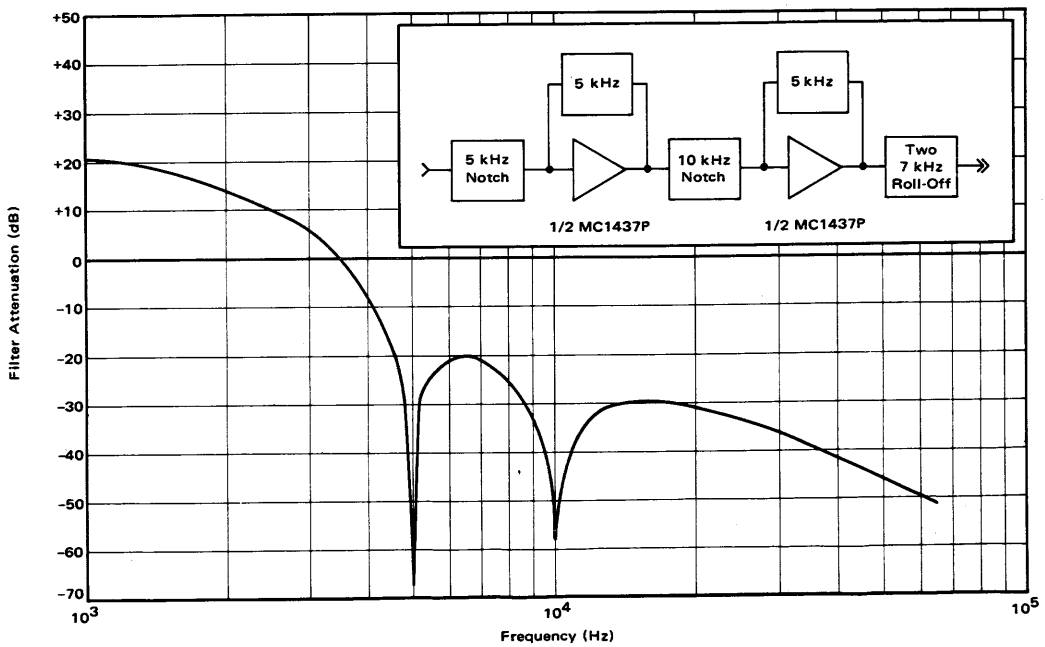


FIGURE 19 – Phase Locked Loop Filter Response

AN-439
THE MC1539 OPERATIONAL AMPLIFIER AND ITS APPLICATIONS

INTRODUCTION

The MC1539 is a second generation monolithic operational amplifier designed to operate nominally from ±15 volt supplies. It has output short circuit protection and input over-voltage protection not previously available with first generation monolithic operational amplifiers. The MC1539 is a pin-for-pin replacement for the 709 type amplifier and offers capabilities not possible in this first generation device.

The MC1539 exhibits low input offset voltage and current (1 mV and 20 nA typically at 25°C) and has outstanding offset characteristics over its temperature range. The very nearly constant, temperature stable input offset voltage and current can be very important in some applications. Another outstanding feature of this amplifier is the 34 V/μs typical slew rate obtainable in the gain-of-100 configuration. The only external components needed for normal operation are the supply decoupling capacitors and the RC network for closed loop stability.

This application note is designed to provide the circuit and system designer with a basic understanding of the MC1539 operational amplifier, both from a "black box" concept and from an actual circuit operation point of view. The application note begins with the circuit description (since parts of the MC1539 circuit are proprietary at the time of this writing, the circuit analysis will be somewhat limited) followed by the frequency response and compensation techniques for various modes of operation, and a discussion on the device operational capabilities . . . large signal swing, noise characteristics, and temperature effects. Applications are given to demonstrate the superiority of the device and include a voltage comparator, a summing amplifier, and a voltage follower circuit. The unity gain amplifier circuit is extended to encompass a feed-forward concept where the frequency range of the system is extended into the 1 MHz range.

The circuit diagram and the equivalent circuit as they appear on the data sheet are shown in Figure 1. The MC1539 is a pin-for-pin replacement for first generation operational amplifiers of the 709 type.

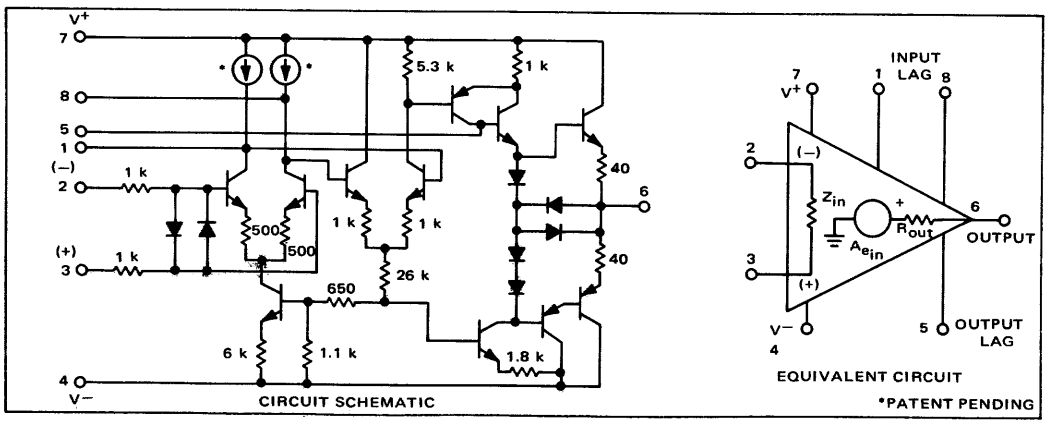


FIGURE 1 – The MC1539

CIRCUIT DESCRIPTION

The MC1539 is a three-stage amplifier with the first stage differential-in, differential-out amplifier designed for high gain, high common-mode rejection, and input over-voltage protection. The second stage is a differential-in, single-ended-out amplifier with low gain and high common mode rejection. Common mode feedback is employed from the second stage back to the first stage to further aid in the control of a common-mode input signal. Through these two differential amplifier stage and the utilization of common-mode feedback, a typical common-mode rejection of 110 dB is obtained. The third stage is a single ended amplifier that provides high gain, voltage translation to a ground reference, output current drive capabilities, and output short circuit protection.

The first two stages are shown in Figure 2. The two diodes D1 and D2 and the two 1 kΩ resistors R1 and R2 provide the desired input over-voltage protection. With this protection, one input can be connected to the +V supply and the other to the –V supply without damage to the input differential amplifier. Should this extreme condition occur, a current (I_i) would appear through the appropriate forward biased input diode of magnitude:

$$I_i = \frac{V^+ - V^- - V_D}{R_1 + R_2}, \quad (1)$$

which ignores the forward resistance of the conducting diode. For ±15 V operation,

$$I_i = \frac{+15 - (-15) - 0.7}{1k + 1k}$$

$$I_i = 14.65 \text{ mA}. \quad (2)$$

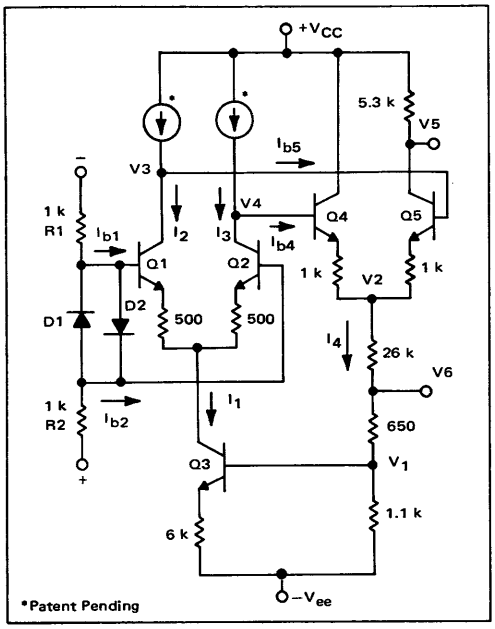


FIGURE 2 – Input Stages

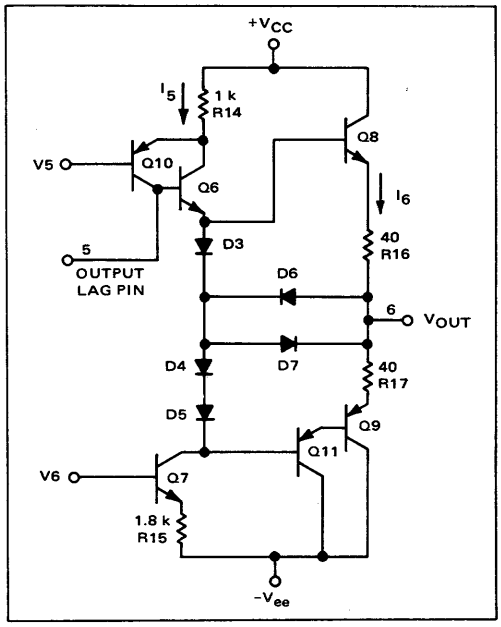


FIGURE 3 – Output Stage

Since this is a known worst case condition, D1, D2, R1, R2 can be easily designed to handle this input condition. Hence, maximum differential input without device damage is stated as ± V; however, this is a maximum rating and not a normal mode of operation. With this input protection, a maximum differential signal from base to base of the input differential amplifier is about 750 millivolts which eliminates the possibility of reverse biasing the base-emitter junction of one of the input differential amplifier transistors.

Before continuing with the discussion on the circuit behavior, the following basic assumptions and circuit constraints are made to simplify the analysis:

1. Transistors, where necessary, are matched. β's are identical. I_b terms are identical with offsets (voltage and current) assumed to be zero.
2. Transistor beta = 160 for input stage (β_1)
   = 120 for second stage (β_2)
   = 50 for output stage (β_3) for all output stage transistors except Q10.
3. $V_D = V_{BE} = 0.7$ volts

Since developing the quiescent levels requires a knowledge of the proprietary portions of the circuit, the quiescent levels will simply be stated in Table I and the derivation omitted.

TABLE I – Quiscent Circuit Levels (For ±15 V Supply)

$V_1 = -13.9$ V
$V_2 = +13.75$ V
$V_3 = V_4 \approx +14.5$ V
$V_5 = +13.5$ V
$I_1 = 66\ \mu A$
$I_2 = I_3 \approx 33\ \mu A$
$I_4 = 1.0$ mA

These voltage and currents are shown in Figures 2 and 3.

In the collectors of the input differential amplifier is a network that acts as a current source. Consequently, the impedance seen looking into this network from the collector of Q1 or Q2 is very high and will be assumed infinite. Knowing this, it can be assumed that the load seen by the first differential amplifier is the input impedance of the second differential amplifier. This impedance is found as

$$R_{L_1} = \beta_2 R_{e_2}, \tag{3}$$

where $R_{e_2} = r_{e_2} + 1\ k\Omega$, the effective emitter resistance in the second stage (Q4 or Q5). For room temperature operation, bulk emitter resistance is given as:

$$r_e = \frac{kT}{qI_e} \approx \frac{26\ mV}{I_e}. \tag{4}$$

Therefore,

$$R_{L_1} = \beta_2 \left[\frac{26\ mV}{\frac{1}{2}(I_4)} + 1\ k\Omega \right]$$

$$= (120) \times (1\ k\Omega + 93\Omega)$$

$$R_{L_1} = 131\ k\Omega. \tag{5}$$

Equation (5) represents the effective load that each collector sees to ground in the first differential amplifier stage.

The gain for the first stage is found as

$$A_{d_1} = \frac{R_{L_1}}{R_{e_1}}, \tag{6}$$

where $R_{e1} = r_{e1} + 500\,\Omega$. For room temperature considerations again using Equation (4), obtain

$$r_{e1} = 290\Omega, \tag{7}$$

therefore,

$$A_{d1} \frac{131 \times 10^3}{(500 + 290)}$$

$$A_{d1} = 166 \frac{\text{volts}}{\text{volt}} . \tag{8}$$

Continuing on into the second differential amplifier stage, it is seen that

$$A_{d2} = \frac{R_{L2}}{2R_{e2}} , \tag{9}$$

where $R_{L2} = 5.3\ k\Omega$ (collector resistor for Q5) since the input impedance into the third stage is very high, and $R_{e2} = r_{e2} + 1\ k\Omega$.

$$A_{d2} = \frac{5.3\ k}{2 \times (1.093\ k)}$$

$$A_{d2} = 2.42 \frac{\text{volts}}{\text{volt}} \tag{10}$$

Thus the gain of the first two stages as obtained from Equations (8) and (10) as

$$A_V = A_{d1} \times A_{d2}$$

$$= 166 \times 2.42$$

$$A_V = 400 \frac{\text{volts}}{\text{volt}} . \tag{11}$$

The output stage is illustrated in Figure 3. The quiescent operating levels are found for ± 15 volt operation as

$$I_5 = \frac{V_{CC} - V_5 + V_{BE}}{R_{14}}$$

$$I_5 = 0.80\ mA. \tag{12}$$

The output drivers are biased Class-AB by diodes D3, D4, and D5. These diodes match the base-emitter characteristics of the output devices resulting in an output standby current (I6) equal to that of I5.

$$I_6 = 0.80\ mA. \tag{13}$$

The gain of the output stage is found as

$$A_{V3} = \frac{R_{L3}}{R_{e3}} , \tag{14}$$

where R_{L3} is an output impedance ($1/h_{oe}$) of transistor Q7, known to be about 300 kΩ. Hence,

$$A_{V3} = \frac{300\ k}{1\ k}$$

$$A_{V3} = 300\ \text{volts/volt}. \tag{15}$$

The open-loop gain (A_{VOL}) is found as

$$A_{VOL} = A_V \times A_{V3}$$

$$= (400) \times (300)$$

$$A_{VOL} = 120{,}000 \frac{\text{volts}}{\text{volt}} . \tag{16}$$

This value of A_{VOL} is typically found; however, the device is specified at 50,000 (minimum) over the full operating range of −55°C to +125°C range.

Looking at the quiescent values for the entire circuit, the standby current drain (I_S) can be approximated:

$$I_S = I_1 + I_4 + I_5 + I_6$$

$$= 66\ \mu A + 1\ mA + 0.8\ mA + 0.8\ mA$$

$$I_S \approx 2.7\ mA. \tag{17}$$

For ±15 volt supplies, this results in a standby power drain of

$$P_D = I_S \times (30\ \text{volts})$$

$$= (2.7\ mA) \times (30\ \text{volts})$$

$$P_D = 81\ mW. \tag{18}$$

Standby power dissipation is specified as 90 mW typically and 150 mW maximum. Power dissipation versus temperature will be discussed later in more detail.

The input bias current I_{b1} (or I_{b2}) can be approximated knowing I_2 (or I_3) and β_1 of the input transistors:

$$I_{b1} \approx \frac{I_2}{\beta_1}$$

$$\approx \frac{33\ \mu A}{160}$$

$$I_{b1} \approx 206\ nA. \tag{19}$$

Input bias current is specified as 200 nA at room temperature and 230 nA at −55°C. Input offset current is the magnitude of the difference between the input bias currents,

$$I_{io} = |I_{b1} - I_{b2}| , \tag{20}$$

and is typically 20 nA. Small I_{io} and it's very low temperature dependance are important items as will be illustrated later.

The output impedance, specified as 4 kΩ, can be verified since the impedance at the collector of Q10 is known to be about 10 MΩ. It was stated earlier that $\beta_3 = 50$; therefore, the output impedance in an open-loop condition (Z_{out}) is determined as

$$Z_{\substack{out \\ O.L.}} = \frac{10 \times 10^6\Omega}{(50)^2}$$

$$= 4\ k\Omega. \tag{21}$$

This impedance, however, does not appear in the closed-loop condition. The closed-loop output impedance Z_{out} is found as C.L.

$$Z_{out}_{C.L.} = \frac{\left(\frac{Z_{out}}{O.L.}\right)\left(1 + \frac{R_2}{R_1}\right)}{A_{VOL}(\omega)} \quad (22)$$

Equation (22) demonstrates that the closed-loop output impedance is inversely proportional to open-loop gain as a function of frequency. As an example, in the unity gain mode (R2 = R1), at low frequencies, the maximum closed-loop output impedance is

$$Z_{out}_{C.L.} = \frac{(4\ k\Omega)\ (1 + 1)}{5 \times 10^4}$$

$$= 0.16\Omega. \quad (23)$$

At higher frequencies of operation the output no longer looks like an ideal source. At the unity crossing frequency (ω_u) the open-loop gain A_{VOL} (ω_u) is equal to the closed-loop gain and

$$Z_{out}_{C.L.} = Z_{out}_{O.L.} = 4\ k\Omega \text{ at this frequency.}$$

The single ended input impedance (Z_{in}) to the amplifier is found as

$$Z_{in} = 2\ [1\ k + \beta_1\ (r_{e_1} + R_{E_1})\ ]$$

$$= 2\ [1\ k + 160\ (290 + 500)\ ]$$

$$Z_{in} = 254\ k\Omega. \quad (24)$$

The input impedance of the MC1539 is specified as 300 kΩ typically and 150 kΩ minimum.

The common-mode input impedance, which is not specified for the device, is found in a slightly different manner. From Figure 2, it is seen that, when driving the amplifier with both inputs tied together, the common-mode input impedance is now found to be the impedance looking into one input in parallel with the impedance looking into the other input. Since symmetry and balance can be assumed, the common-mode input impedance is one-half the input impedance seen in the voltage follower configuration. A ballpark number for common-mode input impedance is 100 MΩ. Common-mode input impedance is not a straight forward, simple parameter to measure because of the impedance levels involved, and will vary with temperature and common-mode input voltage.

The output stage shown in Figure 3 illustrates the output short-circuit protection offered by the MC1539. From the emitter of Q6 to the output pin, there exists two paths for conduction. One is through diodes D3 and D7 and the other is through the base-emitter junction of Q8 and the resistor R16. Output current will flow through the emitter follower transistor Q8 through the 40 Ω resistor R16 as long as the voltage drop across R16 is less than one diode forward drop. When approximately 15 mA of output current (the maximum rating) flows through the 40Ω emitter resistor, the resulting 600 mV will bring into conduction the diode string D3 and D7 which in turn "shuts down" the output emitter follower by removing base current from transistor Q8. A similar argument holds for the diode string D4, D5, D6 in parallel with the base-emitter junctions of Q9 and Q11 and the 40Ω resistor R17. Hence the output, as well as the input, are well protected from accidental misapplications of the device.

MAXIMUM RATINGS

On the front page of the MC1539 data sheet there is a table entitled MAXIMUM RATINGS. This table is reprinted, for ease of reference, in Figure 4. The *output short circuit protection* is illustrated in the continuous output short circuit duration (t_s). The *input over-voltage protection* is also demonstrated in that the Differential Input Signal is allowable to $\pm V^+$ volts where V^+ is the positive supply voltage. The input is also protected from excessive common-mode input levels, as illustrated by the $\pm V^+$ rating. These obviously are not operating ratings, but simply levels of voltage that can be applied without damage to the device.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Power Supply Voltage	V^+ V^-	+18 −18	Vdc Vdc
Differential Input Signal	V_{in}	$\pm V^+$	Volts
Common Mode Input Swing	CMV_{in}	$\pm V^+$	Volts
Load Current	I_L	15	mA
Output Short Circuit Duration	t_s	Continuous	
Power Dissipation (Package Limitation) Derate above T_A = 25°C	P_D	680 4.6	mW mW/°C
Operating Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

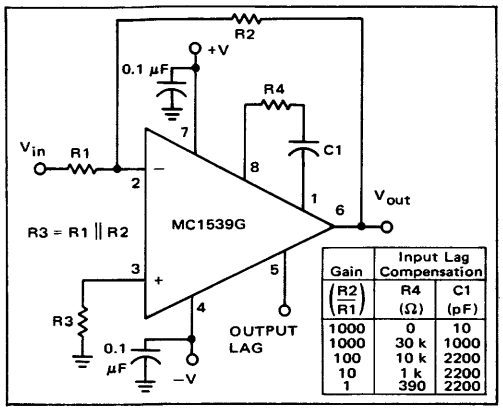
FIGURE 4 – Maximum Ratings from Data Sheet

Another limitation is the Power Dissipation which is limited to 680 mW at 25°C ambient. This limitation is a package constraint and not necessarily a chip limitation. The power dissipation is to be derated from room temperature (T_A = +25°C) by a 4.6 mW/°C factor. It is also seen that the MC1539G will function with supplies to ±18 volts and over the full military temperature range, −55° to +125°C. Care must be taken when operating at extremes: i.e., when operating at ±18 V supplies at +125°C the MC1539G dissipates typically 140 mW (from the Power Dissipation versus Power Supply Voltage curve on the data sheet) plus (4.6 mW/°C) (100°C), which equals 600 mW *unloaded* with V_{out} = 0. Since 680 mW is the package limitation, the output swing and load must be such that they don't exceed the additional 80 mW.

COMPENSATION TECHNIQUES

Input Lag Compensation

The MC1539 offers access to the collectors of the first differential gain stage for frequency compensation purposes (input lag). Component values for compensation in the various gain configurations are listed in Figure 5 and are from the data sheet.



Gain (R2/R1)	Input Lag Compensation R4 (Ω)	C1 (pF)
1000	0	10
1000	30 k	1000
100	10 k	2200
10	1 k	2200
1	390	2200

FIGURE 5 – Operational Amplifier in Closed-Loop Configuration with Input Compensation.

Figure 5 also illustrates the MC1539G in a closed-loop frequency compensated configuration, where frequency compensation is achieved with a resistor (R4) and a capacitor (C1) as shown. The often-asked question of how frequency stability is obtained by using this R4 C1 network between pins 1 and 8 merits some discussion.

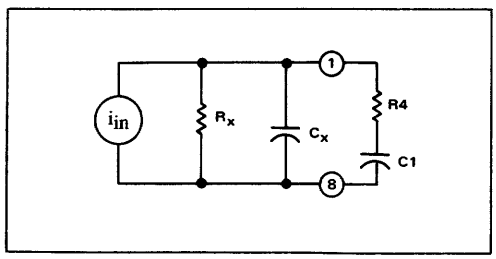


FIGURE 6 – Input Lag Model

Figure 6 illustrates a first-order model for the differential voltage at the collectors of the first stage. Since the current sources in the collectors of Q1 and Q2 represent an assumed infinite impedance, the resistor R_X is the differential load of the second stage, $R_X \approx 260\ k\Omega$. The parasitic capacitance between the collectors is represented by capacitor C_X. From Figure 6, the pole location for the first stage with no compensation applied is expressed as

$$P_{N.C.} = \frac{1}{2\pi R_X C_X}. \qquad (25)$$

Curve A of Figure 7 shows a measured open-loop, uncompensated response of the MC1539 and the arrows indicate approximate pole locations on the uncompensated open-loop response. The second pole location at 350 kHz is due to the first differential amplifier stage. From equation (25) it is seen that

$$C_X = \frac{1}{2\pi R_X P_{N.C.}}$$

$$= \frac{0.159}{(2.6 \times 10^5)(3.5 \times 10^5)}$$

$$= 1.75\ pF. \qquad (26)$$

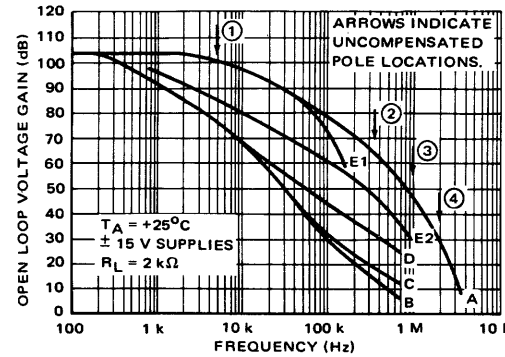


FIGURE 7 – Open Loop Voltage Gain versus Frequency

This is a reasonable value and will be used in further calculations involving C_X.

Frequency compensation added between pins 1 and 8 in the form of an R4-C1 series network, is to modify the original pole at 350 kHz by moving the original pole, adding a second pole, and introducing a zero. Instead of the single pole function seen at the input lag pins when uncompensated, the compensated function now appears as:

$$\frac{[1 + j\omega\,(\text{zero})]}{[1 + j\omega\,(\text{pole}_1)]\ [1 + j\omega\,(\text{pole}_2)]},$$

and the pole and zero locations can be approximated as:

$$\text{Zero} = \frac{1}{2\pi R_4 C_1}, \qquad (27)$$

$$\text{Pole}_1 = \frac{1}{2\pi R_X C_1}, \qquad (28)$$

$$\text{Pole}_2 = \frac{1}{2\pi R_4 C_X}. \qquad (29)$$

A more rigorous expression for the pole and zero locations is developed in Appendix B. Equation (27) is an exact expression where Equations (28) and (29) are approximate relations. For all of the recommended compensation networks, the resulting pole and zero locations are shown in Table II.

TABLE II – First Stage Pole and Zero Locations for Input Lag Compensation

Gain (V/V)	R_4 (Ω)	C_1 (pF)	Zero (Hz)	$Pole_1$ (Hz)	$Pole_2$*** (Hz)	Bode Plot in Fig 8
1	390	2200	185 k	278	204 M	B
10	1 k	2200	72.3 k	278	79.6 M	C
100	10 k	2200	7.23 k	278	7.96 M	D
1000	0	10	—	60 k*	—	E_1
1000	30 k	1000	5.3 k	610	2.65 M	E_2
A_{VOL} uncompensated	∞	—	—	350k**	—	A

* From equation (25) with $R_X = 260\ k\Omega$ and $C_X = 11.75\ pF$.

** From equation (25) with $R_X = 260\ k\Omega$ and $C_X = 1.75\ pF$.

*** C_X assumed to be 2 pF.

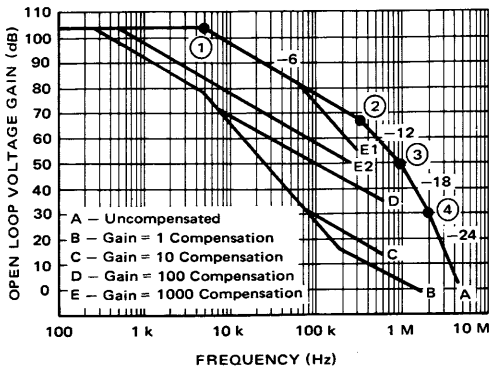


FIGURE 8 – MC1539 Open Loop Bode Plot Responses

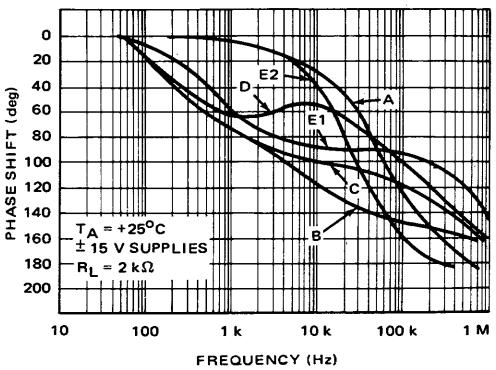


FIGURE 9 – Open Loop Phase Shift vs. Frequency

Figure 8 illustrates the open-loop response in Bode plot form using pole and zero locations shown in Table II. Plot A is for the uncompensated open-loop response. It shows four breakpoints representing the four poles of the amplifier. The first breakpoint, ①, occurs at about 5 kHz and is caused by a pole associated with the lateral PNP (Q10). The second breakpoint, ②, occurs about 350 kHz due to the pole resulting from the input differential amplifier stage. It is the location of this pole that is altered by input lag compensation. The third break occurs at about 1 MHz due to the second differential amplifier pole. The fourth break, due to the output stage pole, occurs at about 2 MHz.

From this illustration, the expression for the uncompensated open-loop transfer function is

$$\frac{e_{out}}{e_{in}} = \frac{-K}{\left(1+j\frac{\omega}{\omega_1}\right)\left(1+j\frac{\omega}{\omega_2}\right)\left(1+j\frac{\omega}{\omega_3}\right)\left(1+j\frac{\omega}{\omega_4}\right)}, \quad (30)$$

where,

$$\omega_1 = 2\pi\,(5 \times 10^3)$$
$$\omega_2 = 2\pi\,(3.5 \times 10^5)$$
$$\omega_3 = 2\pi\,(1.0 \times 10^6)$$
$$\omega_4 = 2\pi\,(2.0 \times 10^6)$$
$$K = A_{VOL}(\omega) \text{ for } \omega = 0. \quad (31)$$

The insertion of the input lag compensation network modifies the location of the ω_2-pole. As shown in Table II, an additional pole and zero are introduced and the transfer function with R4 C1 network inserted is

$$\frac{e_{out}}{e_{in}} = \frac{-K\,(1+j\omega[\text{zero}])}{\left(1+j\frac{\omega}{\omega_1}\right)\left(1+j\omega[\text{Pole}_1]\right)\left(1+j\omega[\text{Pole}_2]\right)\left(1+j\frac{\omega}{\omega_3}\right)\left(1+j\frac{\omega}{\omega_4}\right)} \quad (32)$$

where [zero], [Pole$_1$], and [Pole$_2$] are defined in equations (27), (28), and (29) respectively. For the different gain compensation networks, Bode Plots B, C. D, and E2 of Figure 8 are defined. These Bode Plots demonstrate the unconditional stability offered by the MC1539 in a gain of 1, 10, 100, or 1000 closed-loop configuration using input lag compensation as suggested on the data sheet. The unconditional stability is assured by the –6dB/octave slope that exists at the closed-loop gain crossing.

For the closed-loop gain of 1000, where R4 = 0, C1 = 10 pF is recommended, the compensation merely moves the 350 KHz pole down to about 60 kHz and conditional stability results from the –12 dB/octave slope that exists at the 60 dB crossing. This compensation technique has been used for some time, is valid and usually stable but the designer should be fully aware of what has happened. The 10 pF compensation offers a wider bandwidth and a faster response time at the expense of overshoot and ringing.

Figure 9 furthers this discussion by illustrating the phase shift of the open-loop device for the various compensation networks. From this set of curves, phase margin can easily be obtained for the open-loop device.

When operating the compensated amplifier over its rated temperature range, one should be very careful of the variation of the component values due to temperature in the compensation network. A capacitor with poor temperature characteristics can cause instability for a circuit that is room temperature stable.

MCH1539G Internally Compensated Hybrid Version

For those applications requiring an operational amplifier that is internally compensated, Motorola has made available the MCH1539G, and the commercial version, the MCH1439G. Figure 10 illustrates this hybrid configuration where unity gain compensation (390Ω and 2200 pF) is internal to the high profile TO-5 package. The resistor is Nichrome (390Ω ± 10%), and the capacitor is Ceramic (2200 pF ± 10% that is held within ±10% over the full temperature range). The MCH1539G is a pin-for-pin replacement with the MC1539G.

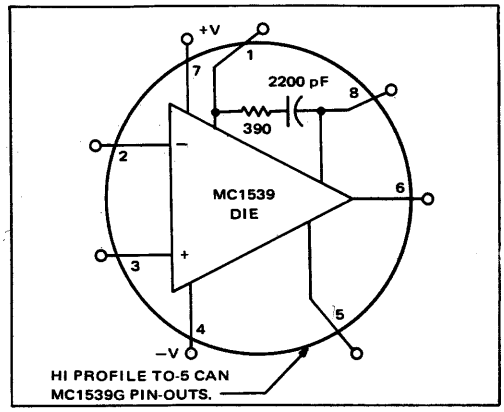


FIGURE 10 – MCH1539G (Internally Compensated) Operational Amplifier.

The MCH1539G will meet all specifications that the MC1539G is guaranteed for, in the properly compensated unity gain configuration. An illustration of the hybrid construction is shown in Figure 11. As seen in Figure 10, although the device is internally compensated, pins 1 and 8 are brought out so that additional compensation may be added or so that the output nulling scheme (discussed later) can be applied.

FIGURE 11 – MCH1539G Hybrid Layout.

Slew Rate

The slewing rate of an operational amplifier is the maximum rate of change of the output voltage (e_O), with respect to time, that the device is capable of producing while maintaining its linear characteristics.

$$\text{Slew Rate} = \frac{de_O}{dt}(\text{max})\frac{\text{volts}}{\text{second}} \qquad (25)$$

Slew rate and the full power response of the device are related. Full power response is the maximum frequency measured in a closed-loop unity gain configuration for which rated output voltage, $\pm E_O$, can be obtained for a sinusoidal signal, with a specified load, and without distortion due to slew rate limiting. For a sinusoidal signal, the output wave can be written as

$$e_O = E_O \text{Sin } 2\pi f_M t \ , \qquad (26)$$

where f_M is the full power response frequency, in Hz. The slew rate can be found as:

$$\frac{de_O}{dt} = 2\pi f_M E_O \text{Cos } 2\pi f_M t \ , \qquad (27)$$

and since the maximum rate of change occurs as the waveform crosses the zero axis, the slew rate – full power response relationship can be shown as

$$\text{Slew Rate} = 2\pi f_M E_O \ . \qquad (28)$$

Note that this is done on a distortion limitation and not on a gain reduction limitation. From Equation (28), as the voltage swing (E_O) is reduced, the operating frequency can be proportionally increased without exceeding the maximum slew rate. Extending this, as the operating frequency approaches unity gain bandwidth, the corresponding voltage swing will define the maximum peak amplitude for "small signal" unity gain response.

To illustrate the validity of Equation (28), consider the typical slew rate specified for the unity gain configuration (4.2 V/μs). From Equation (28) obtain

$$f_M = \frac{\text{Slew Rate}}{2\pi E_O} \ . \qquad (29)$$

For full power response, $E_O \approx 12$ volts, and

$$f_M = \frac{4.2 \times 10^6 \text{ volts/second}}{2\pi(12 \text{ volts})} = 55 \text{ kHz.} \qquad (30)$$

As will be shown later in the section on performance characteristics, the full power bandwidth figure from Equation (30) is reasonably valid.

The MC1539 specifies slew rate as shown in Table III (taken from the data sheet).

TABLE III – Typical Slew Rates

Gain Configuration	$\frac{dE_O}{dt}$ (V/μs)
1	4.2
10	6.25
100	34

An easy way to observe and measure the slew rate of an operational amplifier is to measure the slope of the output waveform of a square wave input signal. The input square wave must have a rise time that exceeds the slew rate capability of the amplifier. The MC1539 demonstrates superior capabilities in that it will slew 34 V/μs typically in a closed loop gain of 100 condition, 6.2 V/μs and 4.1 V/μs in a closed loop gain of 10 and 1 respectively. Figure 12 illustrates the output waveform of a MC1539 in a closed loop gain of 100 configuration with the input being overdriven. The waveform shows about 40 V/μs in both directions.

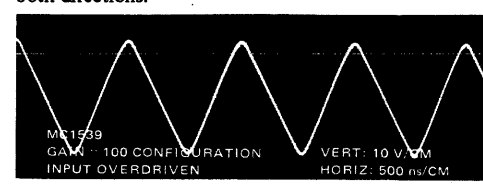


FIGURE 12 – Slew Rate Limiting.

What can cause slew rate limiting when using an operational amplifier?

It appears that the most significant contributor to slew rate limiting can be related to the input lag compensation network (R4 C1). It is known that the rate of change of voltage with respect to time across a capacitor is given by

$$I = C\frac{\Delta V_C}{\Delta t} \qquad (31)$$

where I is the current into the constant capacitance C. In the R4-C1 network, there will exist a voltage change from pins 1 to 8 (call it ΔV_{18}) which will cause a current (i) to flow in the R4-C1 series network. The voltage change seen across the capacitor will be ($\Delta V_{18} - iR_4$) and will determine $\Delta V_C/\Delta t$. There is no known, easily obtainable relationship to link the slew rate with R4 and C1, and to be sure it would be a rather complicated relationship involving not only R4 and C1 but also the closed loop gain, the load impedance, and other factors. It is easily seen that as R4 is increased (as the closed-loop gain is increased), holding C1 = 2200 pF, constant, that the slew rate increases.

The slew rate can also be reduced by adding capacitance from pin 5 to ground. This is due to the lowering of the frequency of the first pole and reducing the bandwidth (f_M in Equation 28). Still another external connection to improve the slew rate capability is the addition of the 10 kΩ resistor from pin 5 (output lag pin) to the output (pin 6). The effect of this resistor is seen by referring once again to Figure 3. The collector of Q10 is nominally at about +1.8 volts. To drive the output in a positive direction (without the 10 kΩ resistor), the voltage V5 is driven down and the base of Q6 is driven, which in turn causes the output to rise. This would happen rapidly because charge could easily be driven into the base of Q6. However, when the voltage V5 is driven positive, transistor Q10 is turned off causing a high impedance discharge path to exist to rid Q6 of its base charge. This in turn causes a slowly changing negative going output compared to what is possible going the other direction. To solve this high impedance discharge path problem, a 10 kΩ resistor is placed from pin 5 to pin 6. This causes 0.18 mA of current to be pulled out of this high impedance node, resulting in more than an order of magnitude improvement in slew rate. The closed loop gain of 100 typical slew rate is increased from 1.7 V/μs to 34 V/μs with this additional resistor.

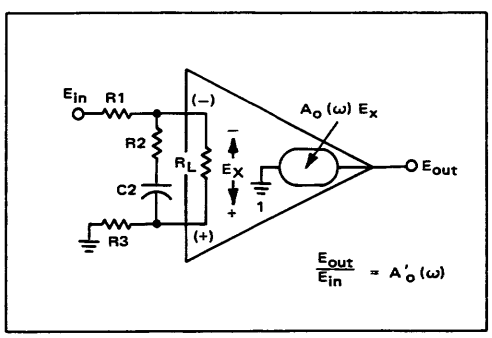


FIGURE 13 – Input Phase Compensation Scheme For the MC1539.

Phase Compensation

By utilizing an input compensation network the MC1539 can be phase compensated for unity gain and still exhibit uncompensated slew rate capabilities. A suggested compensation network is shown in Figure 13. The uncompensated open-loop response is shown in Figure 14, along with the compensated response $|A'_o(\omega)|$ resulting from the input phase compensation network of Figure 13.

The transfer function of Figure 13 is

$$\frac{E_{out}}{E_{in}} = \frac{A_o(\omega)\left[\dfrac{R_i\left(R_2 + \dfrac{1}{j\omega C_2}\right)}{\left(R_i + R_2 + \dfrac{1}{j\omega C_2}\right)}\right]}{R_1 + R_3 + \left[\dfrac{R_i\left(R_2 + \dfrac{1}{j\omega C_2}\right)}{\left(R_i + R_2 + \dfrac{1}{j\omega C_2}\right)}\right]} \qquad (32)$$

Rearranging Equation (32),

$$\frac{E_{out}}{E_{in}} = \frac{A_o(\omega)\, R_i\,[1 + j\omega C_2 R_2]}{\left[R_i + R_1 + R_3\right]\left[1 + j\omega C_2\left\{R_2 + \dfrac{R_i\,(R_1 + R_3)}{R_i + R_1 + R_3}\right\}\right]} \qquad (33)$$

and dividing numerator and denominator of Equation (33) by R_i,

$$\frac{E_{out}}{E_{in}} = \frac{A_o(\omega)\,[1 + j\omega C_2 R_2]}{\left[1 + \dfrac{R_1 + R_3}{R_i}\right]\left[1 + j\omega C_2\left\{R_2 + \dfrac{R_1 + R_3}{1 + \left(\dfrac{R_1 + R_3}{R_i}\right)}\right\}\right]} \qquad (34)$$

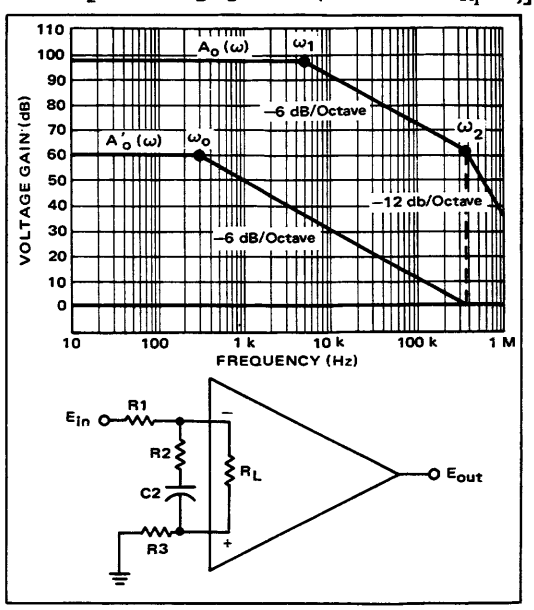


FIGURE 14 – Phase Compensation Bode Plots

When R1 and R3 are chosen such that $(R1 + R3) << R_i$, Equation (34) may be further simplified to

$$\frac{E_{out}}{E_{in}} = \frac{A_O(\omega)\,[1 + j\omega C_2 R_2]}{1 + j\omega C_2\,[R_2 + R_1 + R_3]}. \quad (35)$$

The $A_O(\omega)$ term that has been carried this far has four poles (see Figure 8 and is of the form

$$A_O(\omega) = \frac{-K}{(1 + j\frac{\omega}{\omega_1})(1 + j\frac{\omega}{\omega_2})(1 + j\frac{\omega}{\omega_3})(1 + j\frac{\omega}{\omega_4})} \quad (36)$$

where $K = A_{VOL}(o)$ and $\omega = 2\pi f$.

From Figure 14 we select ω_O such that $A'_O(\omega)$, rolling off at −6 dB/octave, shall intersect the 0 dB axis at or before ω_2, and that the zero location in Equation (35) resulting from the input compensation will occur at ω_1. The placement of the zero at ω_1 results in the cancellation of the first pole in the open-loop response of the operational amplifier. Hence, the transfer function obtained by substituting Equation (36) into Equation (35) is

$$\frac{E_{out}}{E_{in}} = \frac{-A_{VOL}(o)\,[1 + j\omega C_2 R_2]}{(1 + j\frac{\omega}{\omega_1})(1 + j\frac{\omega}{\omega_2})(1 + j\frac{\omega}{\omega_3})(1 + j\frac{\omega}{\omega_4})(1 + j\omega C_2\,[R_2 + R_1 + R_3])} \quad (37)$$

Therefore, for pole cancellation to occur,

$$\omega_1 = \frac{1}{R_2 C_2}. \quad (38)$$

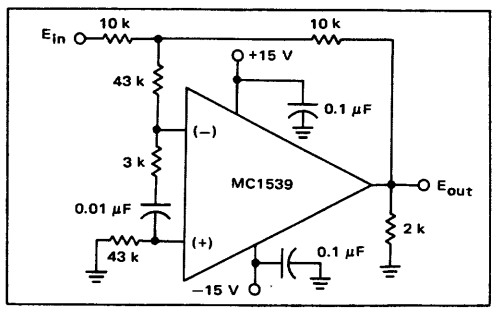


FIGURE 15 – Unity Gain Circuit for Fast Response Time.

In the uncompensated open-loop response of Figure 15, described by Equation (36), the following is recalled:

$$\begin{aligned} A_{VOL}(o) &= 50{,}000 \text{ min; } 120{,}000 \text{ typ} \\ \omega_1 &\approx 2\pi\,(5 \text{ kHz}) \\ \omega_2 &\approx 2\pi\,(350 \text{ kHz}) \\ \omega_3 &\approx 2\pi\,(1.0 \text{ MHz}) \\ \omega_4 &\approx 2\pi\,(2.0 \text{ MHz}) \\ R_i &= 150\ \text{k}\Omega \text{ min} \end{aligned} \quad (39)$$

From Equation (33) for $(\omega = 0)$ we have

$$A'_O(o) = \frac{A_O(o)\,R_i}{R_i + R_1 + R_3} \quad (40)$$

Once R1 and R3 have been chosen, then the phase compensated open-loop voltage gain is known. When this is known, the low frequency pole (ω_O) is known and R2 and C2 are obtained from

$$\omega_O = \frac{1}{C_2\left[R_2 + \frac{R_1 + R_3}{1 + \frac{R_1 + R_3}{R_i}}\right]} \quad (41)$$

and

$$\omega_1 = \frac{1}{R_2 C_2} \quad (42)$$

Example

Determine input phase compensation so that $A'_O(\omega) = 60$ dB as $\omega \to 0$. Using minimum specified values from the MC1539 data sheet,

$$60\text{ dB} = \frac{(94\text{ dB})\,(150\ \text{k}\Omega)}{(150\ \text{k}\Omega + R_1 + R_3)} \quad (43)$$

Hence,

$$R_1 + R_3 = (\frac{94}{60} - 1)\,150\ \text{k}\Omega$$
$$= 0.57 \times 150\ \text{k}\Omega$$
$$R_1 + R_3 = 85.3\ \text{k}\Omega\,. \quad (44)$$

If R1 = R3 for good bias current error cancellation then

$$R_1 = R_3 = 42.65\ \text{k}\Omega\,. \quad (45)$$

The nearest standard value is 43 kΩ.

For $A_O(\omega) = 60$ dB and $\omega 2 = 2\pi$ (350 kHz) we find that $\omega_O = 2\pi$ (280 Hz) as seen in Figure 14.

Equations (41) and (42) can now be solved for R2 and C2, as

$$\omega_O C_2\left[R_2 + \frac{R_1 + R_3}{1 + \frac{R_1 + R_3}{R_i}}\right] = 1$$

$$C_2 = \frac{1}{R_2 \omega_1}$$

and

$$R_2 = \frac{R_1 + R_3}{(\frac{\omega_1}{\omega_O} - 1)(1 + \frac{R_1 + R_3}{R_i})} \quad (46)$$

For the present problem,

$$R_2 = \frac{(85.3\text{ k})}{(\frac{5K}{0.280\text{ k}} - 1)(1 + \frac{85.3\text{ k}}{150\text{ k}})}$$

$$= \frac{85.3\text{ k}\Omega}{(17.85)(1.57)}$$

$$= 3.04\text{ k}\Omega\text{ (3 k}\Omega\text{ std value)}, \quad (47)$$

and

$$C_2 = \frac{1}{(3\text{ k})(2\pi)(5\text{ k})}$$

$$= \frac{10^{-7}}{3\pi}$$

$$= 0.0106\ \mu\text{F (0.01 }\mu\text{F std. value)}. \quad (48)$$

Warning: It can be seen from Figure 15 that if $A_O(\omega)$ is larger than 60 dB, instability may occur in a closed-loop unity gain configuration. This is because an increase in $A_O(\omega)$, holding ω_O fixed, will shift the Bode Plot up vertically, allowing the ω_2 breakpoint to be present before the unity gain crossing is achieved. This is caused, from Equation (43), by assuming a minimum input impedance in that calculation. The author experienced this problem and had to increase the values of R1 and R3 to regain unity gain stability. If one experiences instability when evaluating this technique, this may be the reason.

Table IV lists the experimental results using the compensation technique. The test circuit, showing the unity gain configuration, is illustrated in Figure 15.

TABLE IV – Performance Comparison (Unity Gain)

Electrical Characteristics	Input Compensation	Suggested compensation from MC1539 data sheet
Small Signal Bandwidth	250 kHz	1 MHz
Large Signal Slew Rate	39 V/μs	4.2 V/μs
Power Bandwidth (20 V pk=pk)	110 kHz	50 kHz
Output Noise (R_S = 10 kΩ)	27.0 mV	4.5 mV
Open Loop Voltage Gain	1000 min	50,000 min

The input phase compensation scheme offers the advantage of high power bandwidth and slew rate with relatively few additional components. The lower small signal bandwidth, higher output noise, and lower open-loop voltage gain are the obvious disadvantages. This technique should be evaluated in the context of a particular application.

Another scheme will be shown in the applications section of this note where a unity-gain power bandwidth of 1 MHz is possible by using the feed-forward capabilities designed into the MC1539 amplifier.

PERFORMANCE CHARACTERISTICS

Considerable data has been compiled on the MC1539, both in evaluating its performance and in comparing it with competitive devices. This section is devoted to a discussion of performance capabilities, and how this performance compares with other known operational amplifiers.

The MC1539 uses three stages of gain and level translation. Its open-loop uncompensated response shows that four poles are present before the response crosses the 0 dB axis. This can be seen in Figures 7 and 8. As discussed earlier, the amplifier if improperly compensated will exhibit instability in a closed loop configuration. The input lag compensation is the most generally used as it is very straightforward, well understood, and easily applied. Unless otherwise stated, input lag compensation will be used throughout the performance discussion.

The following discussion will include many curves from the data sheet with pertinent comments related to each. For a good discussion about getting more value out of an operational amplifier data sheet, refer to Motorola Application Note AN-273.

Figure 16 illustrates the test circuit used for evaluation of the MC1539, and Table V lists the test conditions recommended for evaluation of the device.

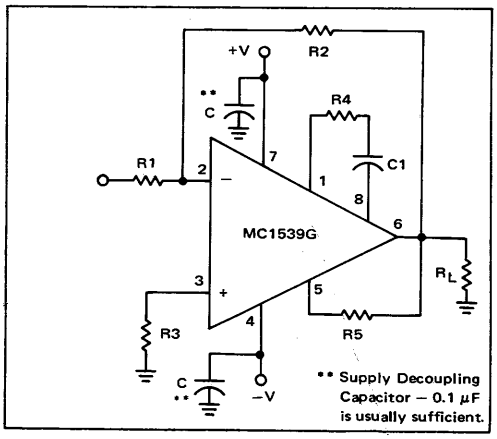


FIGURE 16 – Test Circuit.

TABLE V – Recommended Test Conditions

Curve No.	Voltage Gain	Test Conditions				
		R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	C_1 (pF)
A	A_{VOL}	0	∞	0	∞	0
B	1	10 k	10 k	5 k	390	2200
C	10	1 k	10 k	1 k	1 k	2200
D	100	1 k	100 k	1 k	10 k	2200
E_1	1000	1 k	1 M	1 k	30 k	1000
E_2	1000	1 k	1 M	1 k	0	10

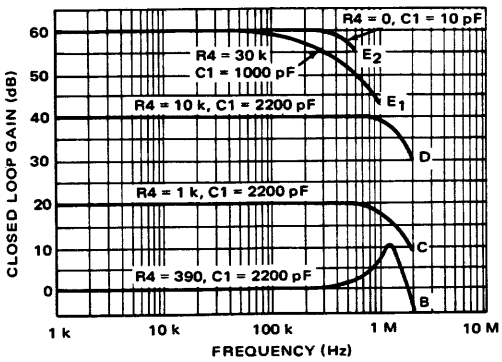


FIGURE 17 – Closed Loop Gain vs. Frequency

Recalling the open-loop voltage gain and phase shift curves, using the recommended test conditions of Table V, the closed-loop gain vs. frequency curves shown in Figure 17, are obtained. Two things are readily observed in Figure 17. First, the effect of the two different compensation networks in the gain of 1000 mode; and second, the unity gain curve shows some peaking. This peaking results from the effects of the closeness of the poles at 1 MHz and 2 MHz, and can be reduced by adding heavier compensation which will result in a slight reduction in bandwidth. The stability of the response over the full temperature range will be discussed in the Temperature Effects section.

Figure 18 illustrates the power bandwidth capability of the MC1539. This curve was obtained by operating the device at room temperature (+25°C), using ±15 V supplies,

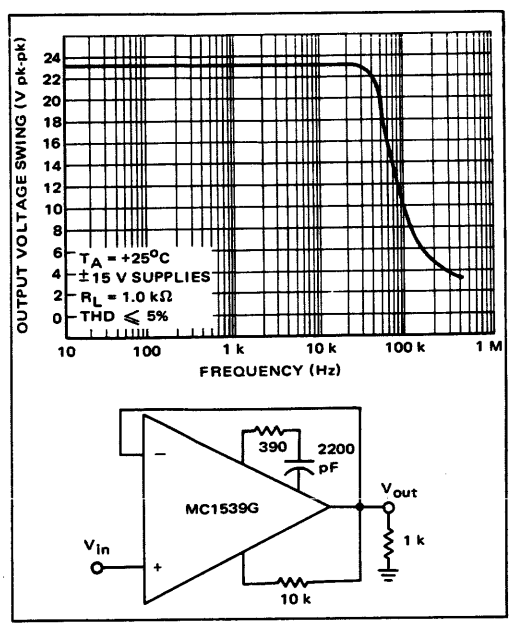


FIGURE 18 – Power Bandwidth (Voltage Follower Configuration)

driving a 1 kΩ load, while maintaining a total harmonic distortion (THD) of less than 5%. The curve shows a full 20 V pk-pk response to 50 kHz. A similar test, run on competitive devices, resulted in a 20 V pk-pk signal to 5 kHz for the 709-type amplifier (using data sheet recommended compensation: 1.5 kΩ, 5000 pF, 200 pF), and a 10 kHz bandwidth (20 V pk-pk) for the 101-type amplifier using the recommended 30 pF compensation. The superior performance of the MC1539 is evident.

In addition to the power bandwidth curve of Figure 18, large signal swing vs. frequency data is also available for all of the standard closed-loop configurations. Figure 19 shows the curves that were obtained, again driving a 1 kΩ load.

Figure 20 slows the output swing capabilities for different load resistances and supplies. In determining these curves, a standard closed loop gain configuration of 100 (R2 = 100 kΩ) was used at room temperature with a 1 kHz input signal. The output was observed while maintaining a THD < 5%. Supplies of ±12 V, ±15 V, and ±18 V were chosen giving a 6 volt operating area about the nominal ±15 V operating voltage. Intermediate values can be obtained by interpolation. The closed-loop gain configuration of 100 was used so that the 100 kΩ feedback resistor would be large enough to not alter the

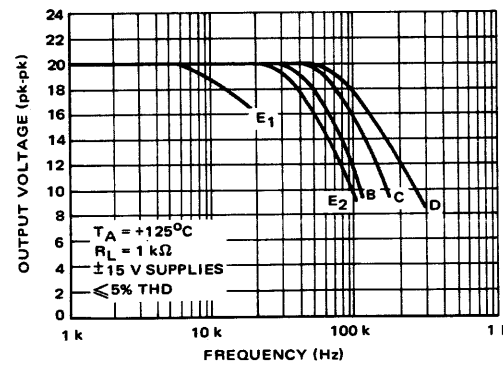


FIGURE 19 – Large Signal Swing vs. Frequency

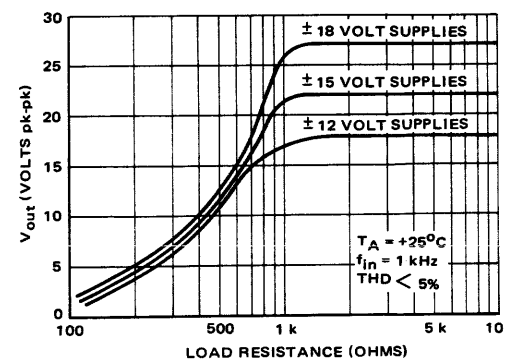


FIGURE 20 – Output Swing vs. Load Resistance.

effective load resistance. When a small value of R2 is used, it must be factored when determining the load size. As shown in Figure 20, a 1 kΩ load is the practical lower limit. This is expected since the known output load current upper limit is 15 mA from ±15 volt supplies. Removing the THD < 5% restriction and allowing the output to go into saturation produces the curve shown in Figure 21. Here the 1 kΩ load is used and the supplies are varied. The test circuit used was a standard gain configuration of 10 at room temperature (+25°C) with a 1 kHz input signal.

The improved performance of the MC1539 over its "Brand-X" counterparts is shown in Figure 22. The voltage follower pulse response (Figure 22) is as much as an order of magnitude better than its competition, which is not surprising considering the slew rate and response times specified for the device.

Figure 23 shows the positive and negative common-mode limits for various supply voltages. The common-mode input can go further negative than positive due to the current source type circuits in the collectors of the input differential amplifier. Figure 24 indicates the common-mode rejection at +25°C, with ±15 volt supplies, for a circuit having unity gain compensation (worst case) over the frequency range. For lighter compensation, the rolloff does not occur as low in frequency.

Temperature Effects

The excellent temperature stability is partially shown in Figure 25 by plotting Common-mode Rejection vs. Temperature for f_{in} = 1 kHz at 20 V pk-pk,

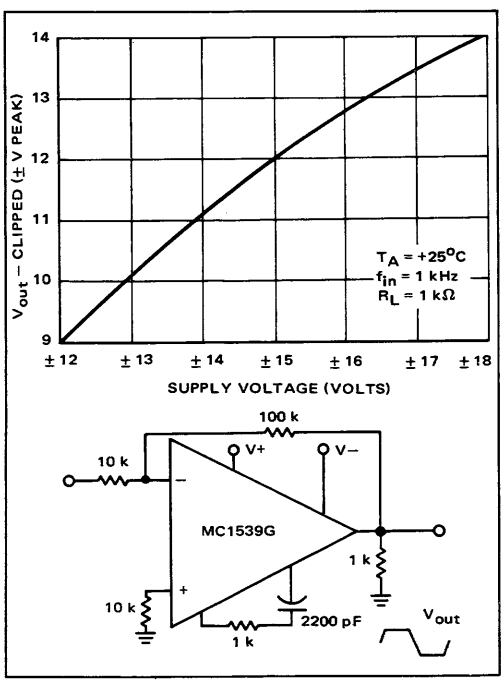


FIGURE 21 – Output Voltage Swing (To Clipping) vs. Supply

and ±15 volt supplies. The following equations are for calculating common-mode rejection (CM_{rej}):

$$AV_{CM} = 20 \log \left[\left(\frac{e_{out}}{e_{in}} \right)_{CM} \right] \quad (49)$$

$$CM_{rej} = AV_{CM} - AVOL \quad (50)$$

where $\left(\frac{e_{out}}{e_{in}}\right)_{CM}$ is the common-mode gain in volts/volt and AV_{CM} and AVOL are in units of dB. The circuit used is shown below the curve in Figure 25.

Figures 26, 27, and 28 are reprints from the data sheet showing input offset voltage and current, and input bias current over the full temperature range. These curves again emphasize the superior temperature stability of the device and can be very important in some applications. One that comes to mind is a comparator circuit being driven from a voltage source having a reasonably high source impedance. The low bias current will cause very little error due to the high source impedance, and the very stable bias and offset currents over temperature will reduce the amount of error due to shift in the comparator's reference point.

Figures 29, 30, 31, and 32 show the variation in the closed-loop gain response curves over the full temperature range, –55°C to +125°C. Figure 33 illustrates the stability

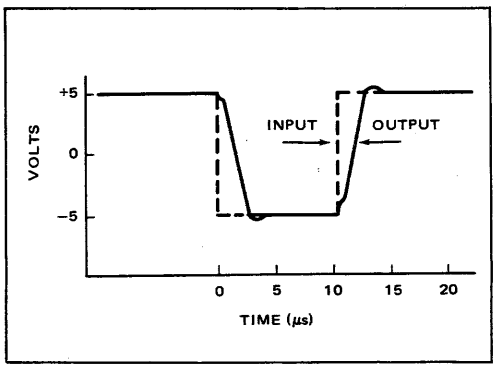


FIGURE 22 – Voltage Follower Pulse Response

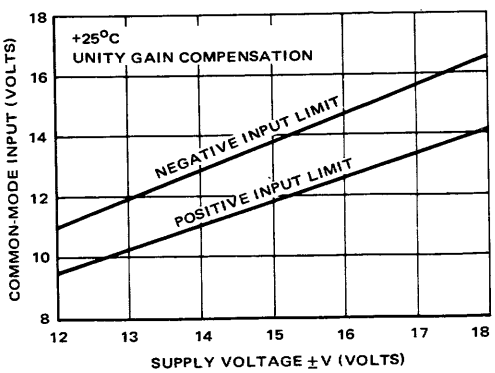


FIGURE 23 – Common-Mode Input Voltage vs. Supply

of the devise's power dissipation over temperature. This curve represents the device dissipation for zero output and ±15 V supplies.

Noise Considerations

The MC1539 was not designed especially for low noise applications as was, for example, the MC1535. However, considering the very large open-loop gain (120,000 typ.) the device offers fairly good noise characteristics.

Table VI shows a comparison of the noise at the output for five currently available monolithic operational amplifiers.

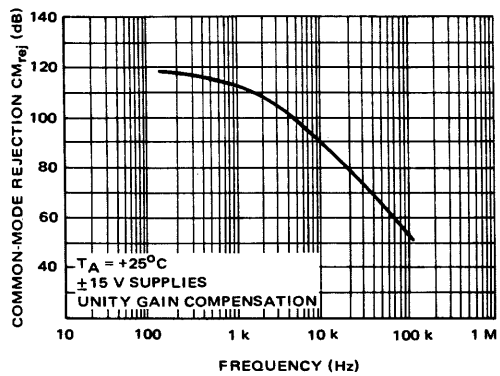


FIGURE 24 – Common-Mode Rejection vs. Frequency

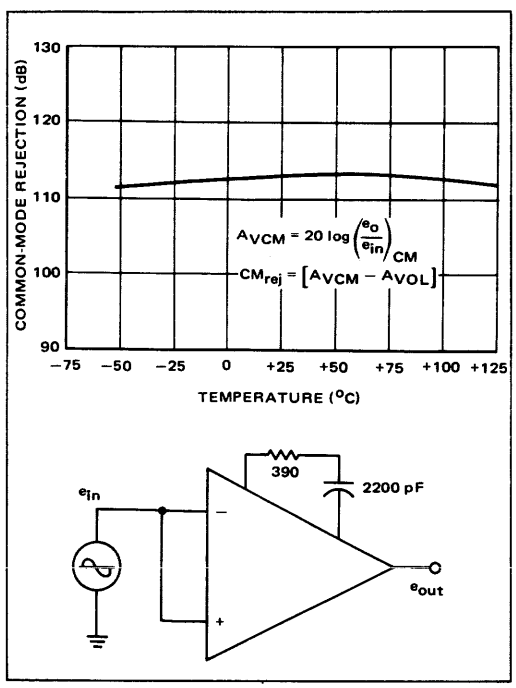


FIGURE 25 – Common-Mode Rejection (CM_{rej}) vs. Temperature

TABLE VI – Output Noise Voltage Comparison

Device Type	Output Noise Voltage for Closed Loop Gain of 100 (Equal Bandwidths)
MC1530	3.0 mV
MC1533	1.25 mV (low gain) 1.90 mV (high gain)
MC1535	0.72 mV
MC1539	1.5 mV
MC1709	0.8 mV

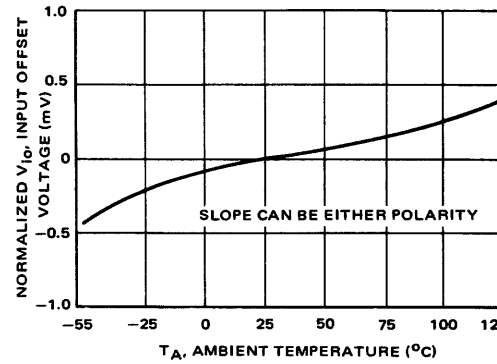


FIGURE 26 – Input Offset Voltage vs. Temperature

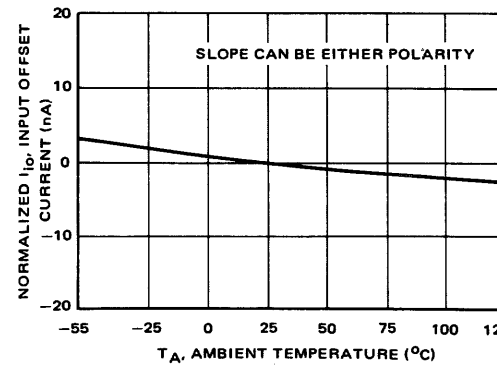


FIGURE 27 – Input Offset Current vs. Temperature

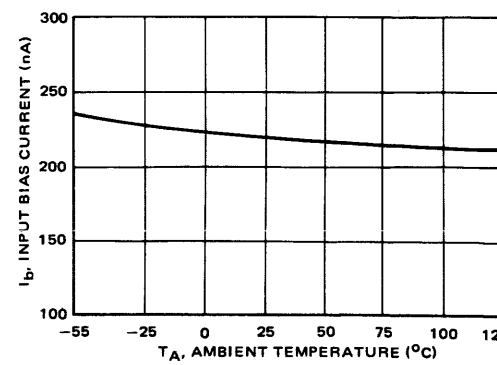


FIGURE 28 – Input Bias Current vs. Temperature

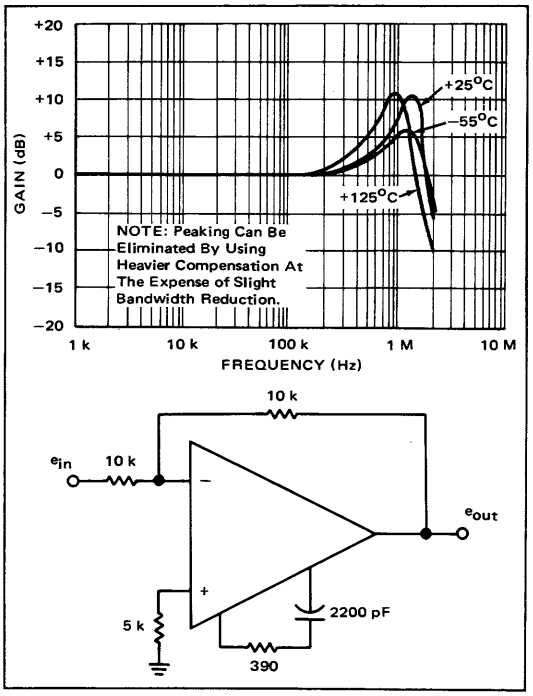


FIGURE 29 – A_{CL} = 1 Response vs. Temperature

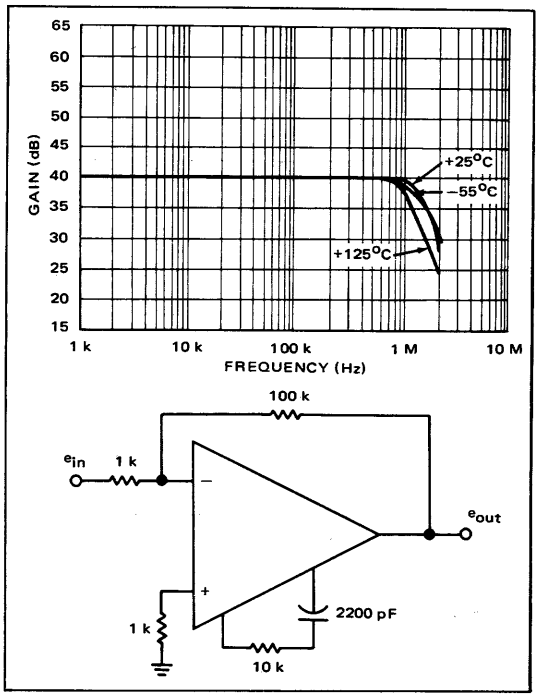


FIGURE 31 – A_{CL} = 100 Response vs. Temperature.

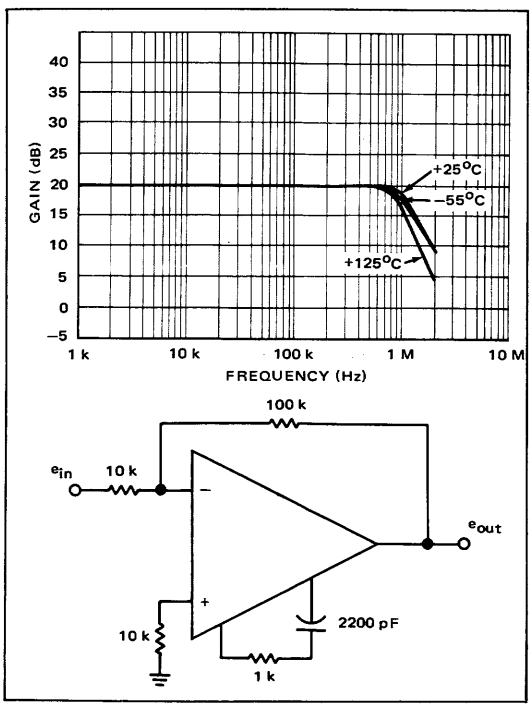


FIGURE 30 – A_{CL} = 10 Response vs. Temperature

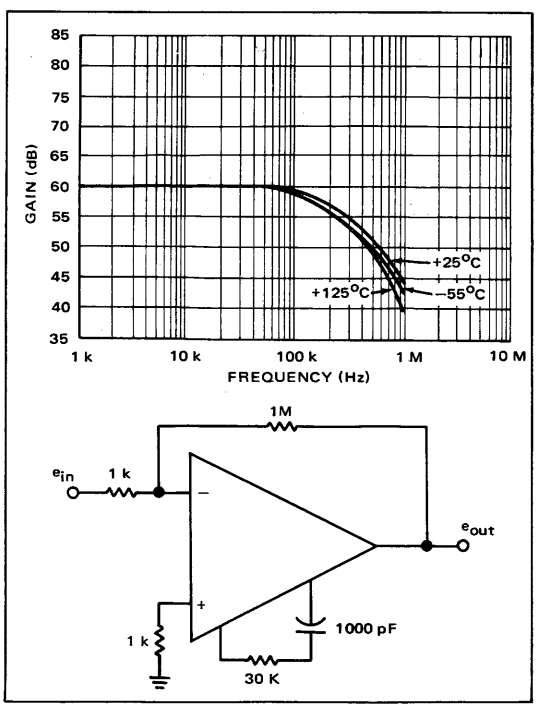


FIGURE 32 – A_{CL} = 1000 Response vs. Temperature

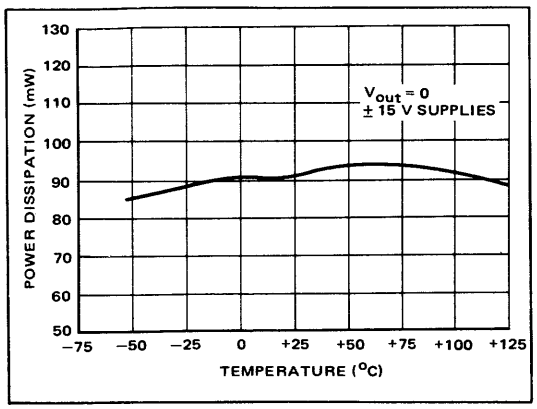


FIGURE 33 – Power Dissipation vs. Temperature

Figure 34 offers what should be a very practical and useful set of curves by showing output noise vs. source reistance for closed-loop gains of 1, 10, 100, and 1000.

CIRCUIT APPLICATIONS

This section includes some circuit configurations suggested to make the MC1539 a more versatile device. Also included are some test circuits used to observe parameters, and applications using the MC1539.

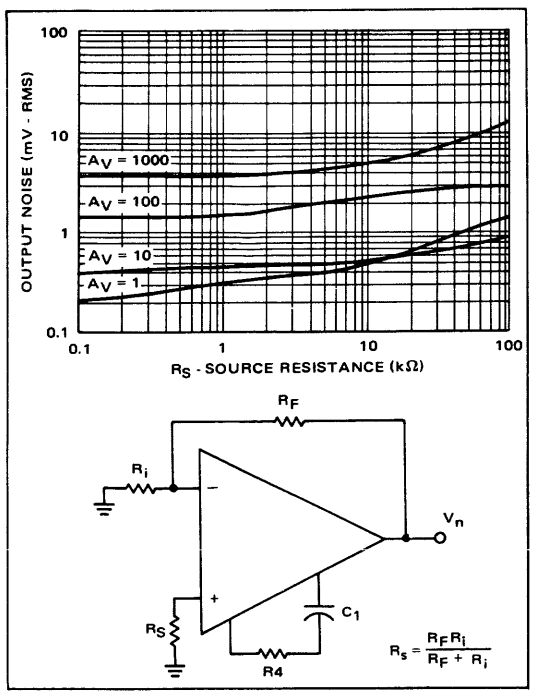


FIGURE 34 – Output Noise vs. Source Resistance

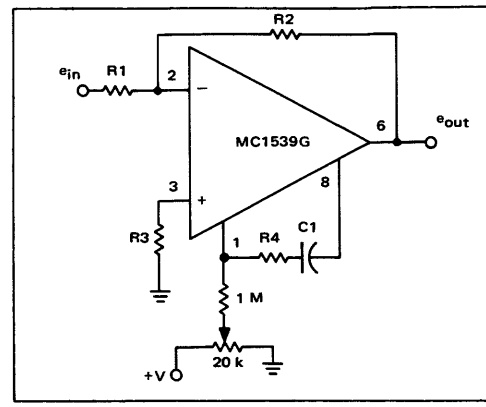


FIGURE 35 – Output Nulling Circuit

Output Nulling

It has been shown that the error due to the bias current can be compensated by setting (see Figure 35)

$$R_3 = \frac{R_1 R_2}{R_1 + R_2}. \quad (51)$$

There will still remain, however, an output error term due to the input offset current and voltage. This output error can be nulled out by introducing a small current source at either pin 1 or pin 8. This adds current to, or takes current out of one node which allows the output to be nulled. The 1 MΩ resistor offers sufficient impedance so as not to alter proper circuit operation.

I_{io} and V_{io} Test Circuit

The input offset parameters, voltage and current, and their stability with temperature variation are two of the many reasons why the MC1539 is a second generation device. The circuit of Figure 36 will allow the user to measure I_{io} and V_{io} for himself so that he might become more confident in the excellence of the MC1539. The operation of the test circuit is as follows:

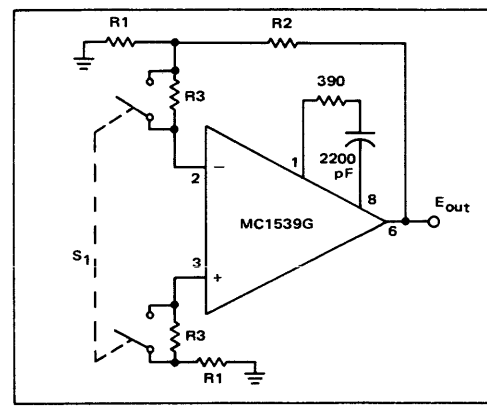


FIGURE 36 – Input Offset Test Circuit

1. Close S1 and measure E_o. Call this voltage E1.
2. Open S1 and measure E_o. Call this voltage E2.

The following equations define the offset parameters:

$$V_{io} = \frac{E_1}{\left(\frac{R_2}{R_1}\right)} \text{ volts} \quad (52)$$

$$I_{io} = \frac{|E_1 - E_2|}{R_3\left(1 + \frac{R_2}{R_1}\right)} \text{ amps.} \quad (53)$$

Equations (52) and (53) are developed, along with the test circuit in Appendix A.

Substituting some numbers into equations (52) and (53) let

$R_1 = 51\Omega$

$R_2 = 5.1\ k\Omega$

$R_3 = 100\ k\Omega \pm 1\%$

then

$$V_{io} = \frac{E_1}{100} \text{ volts,}$$

and

$$I_{io} = \frac{|E_1 - E_2|}{(1 + 100)(10^5)} \text{ amps.}$$

Comparator

The low input bias current (I_b) and input offset current (I_{io}) plus their excellent temperature characteristics and the very high slewing rate make the MC1539 a good device to use as a comparator. Figure 37 shows one comparator configuration that has been used with good success. The zener diode connected to pin 5 limits the positive going waveform at the output to about 2 volts below the zener voltage. The silicon diode connected to the output limits the output negative excursion to protect the logic circuit that is being driven. The output parallel RC network provides two functions: first, recalling charge control concepts,[2] it is known that a parallel RC network can be made to match the input characteristics of the logic circuit, eliminating any reduction in response time due to RC charging time; second, some saturated logic circuits (MRTL for example) have a rather low value of input base resistance, R_B, (as low as 450Ω), and the additional resistance in series with the output will help minimize the output current overload problem.

One thing that should be pointed out to avoid trouble when trying to use the MC1539 in a "parallel bank A-D converter" type of application, is that when the differential input voltage exceeds about 750 mV, the input protective circuitry begins to draw current. The effect is that when the differential input exceeds that amount needed to cause one of the input diodes to conduct, the input impedance of the comparator is reduced, causing a relatively heavier load to exist on the source. In the circuit of Figure 37, this is of no concern because only one comparison is being made; however, if 32 comparators were paralleled to perform a 5-bit high speed A-D function, then error problems can arise when input signal source impedance is not low enough. Many of the 32 paralleled comparators will have differential inputs in excess of 750 mV. One solution to this dilemma is to use a different type of comparator, like the MC1710 or the MC1711.

Supply Protection

If there is concern about the possibility of the ±V supply leads being reversed in a system, which could have rather disappointing results, the simple circuit shown in Figure 38 is offered as food for thought in this area. The MZ500-23 zener diodes exhibit an 18 volt (typical) zener knee and will remain non-conductive if the ±15 V leads are switched to the device. This type of protection might be worth considering during the bread-boarding phase of a program where there is a limited number of sample devices to evaluate. With the diodes in position, the output voltage swing is obviously reduced since the effective supply voltage at the device has been reduced by two diode forward-voltage drops.

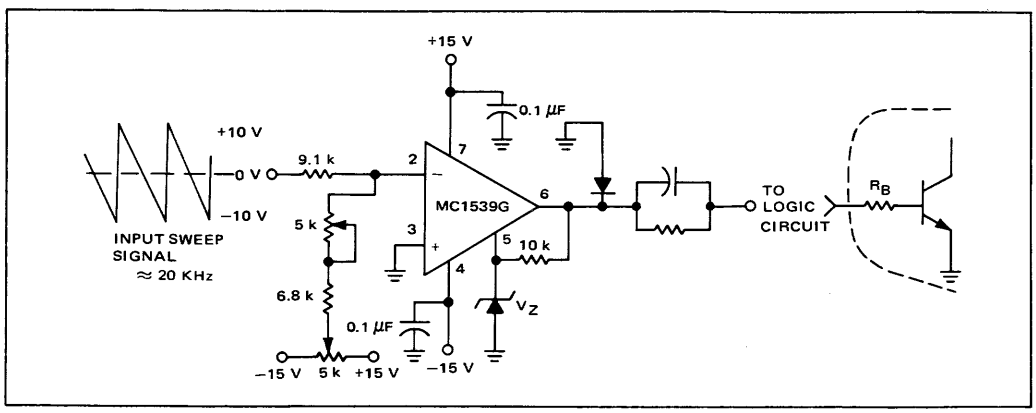


FIGURE 37 – Voltage Comparator

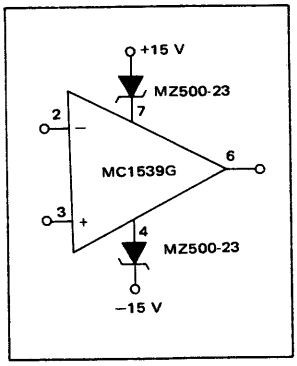


FIGURE 38 – Supply Protection

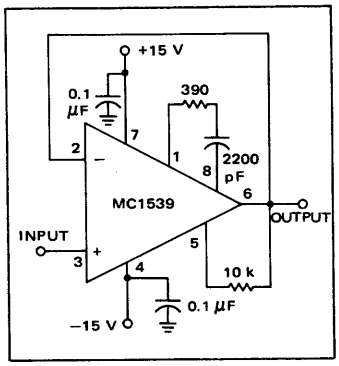


FIGURE 39 – Voltage Follower

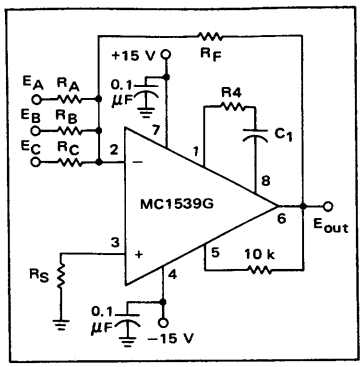


FIGURE 40 – Summing Amplifier

Voltage Follower

As has been mentioned before, the MC1539 is an excellent choice for the voltage follower application. Figure 39 illustrates this configuration. Unity gain compensation is shown since the device is being operated in a non-inverting unity gain mode.

The MC1539 does not experience the common-mode latch-up problem that the 709-type amplifier is plagued with in this configuration. This allows the output to be tied directly back to the (–) input, pin 2, as shown in Figure 39.

Recalling from Equation (22) the output impedance for this configuration at low frequencies is

$$Z_{out} = \frac{(4\ k\Omega)\ (1 + 0)}{1.2 \times 10^5}$$

$$= 3.33 \times 10^{-2}\Omega$$

$$= 33.33 \text{ milliohms}, \qquad (54)$$

which represents a relatively good voltage source. The input impedance can be approximated as

$$Z_{in\ V.F.} = \frac{A_{VOL}(\omega)\, Z_{in}}{1 + \frac{R_2}{R_1}}, \qquad (55)$$

and at low frequencies

$$Z_{in\ V.F.} = \frac{(1.2 \times 10^5)(3.00 \times 10^5)}{1 + 0}$$

$$= 3.6 \times 10^{10}\Omega \qquad (56)$$

which is indeed high. However, the input impedance is limited by the value of the common-mode input impedance and the value expressed in Equation (56) is a theoretical value. However, one can expect the input impedance for the voltage follower to exceed 100 MΩ. With these input and output characteristics, the device makes an excellent buffering element.

Summing Amplifier

When thinking of operational amplifiers, traditionally, the analog computer summing amplifier application comes to mind. Because of the high open-loop gain found in the MC1539, the device functions with a small amount of loop-gain error as a closed-loop summing amplifier. Figure 40 illustrates this classic configuration. To minimize the output error due to input bias current, the R_S resistor value should be selected to equal the dc Thevenin equivalent seen looking out of pin 2:

$$R_S = R_A \parallel R_B \parallel R_C \parallel R_F\ . \qquad (57)$$

Another point worth mentioning is that the input lag compensation need only be sufficient to handle the highest gain condition. Compensation must be suitable for the closed loop gain ratio of

$$\frac{R_F}{R_A \parallel R_B \parallel R_C}\ .$$

For the configuration shown in Figure 40, the output is expressed as

$$E_{out} = -\left[\frac{R_F}{R_A} E_A + \frac{R_F}{R_B} E_B + \frac{R_F}{R_C} E_C\right] \qquad (58)$$

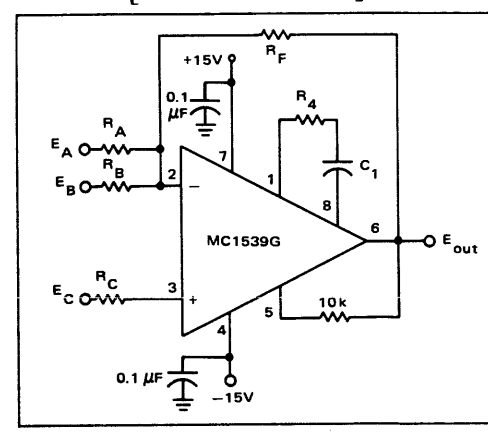


FIGURE 41 – Differential Amplifier

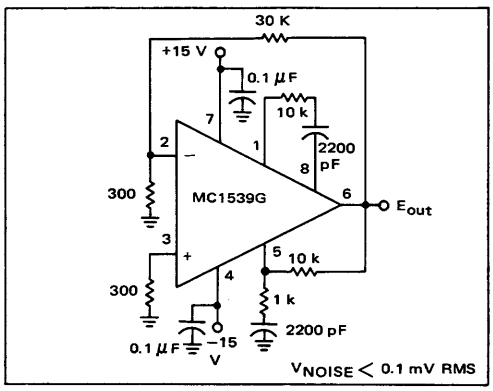


FIGURE 42 – Low Noise Output

Differential Amplifier

Another classic configuration that comes to mind is that of the differential amplifier. The basic configuration is shown in Figure 41. Again for best input offset error cancellation, one should select

$$R_C = R_A \parallel R_B \,, \tag{59}$$

and the resulting output expression is

$$E_{out} = -\left[\frac{R_F}{R_A}E_A + \frac{R_F}{R_B}E_B\right] + \left[1 + \frac{R_F}{R_C}\right]E_C \tag{60}$$

where R_C is defined in Equation (59).

Again, the R_4C_1 compensation should be sufficient to handle the gain condition of

$$\frac{R_F}{\left(\frac{R_A R_B}{R_A + R_B}\right)}$$

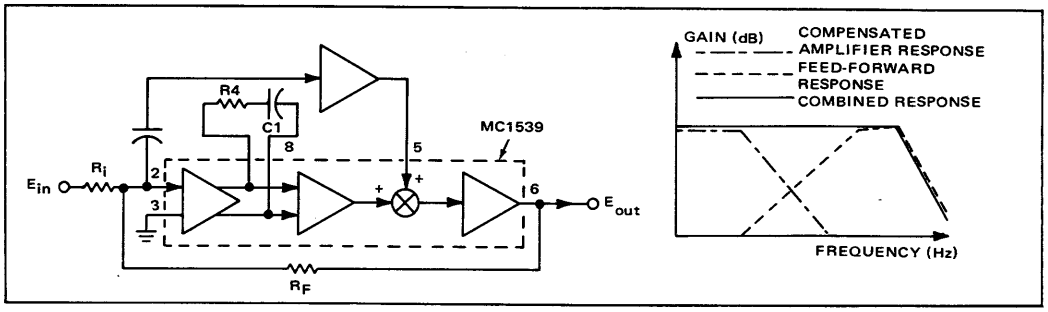


FIGURE 43 – Basic Feed-Forward Circuit

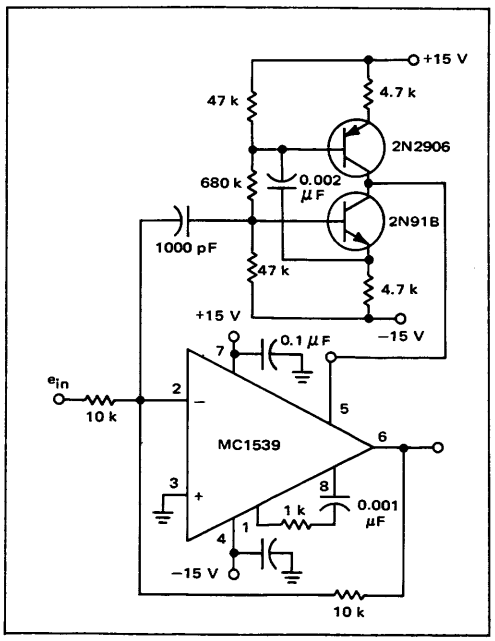


FIGURE 44 – Unity Gain Feed-Forward Amplifier

Low Noise Circuit

The need arises from time to time to further suppress the amount of noise at the output of the MC1539 in a closed-loop mode. As an example of this consider an application where it is required to operate in the non-inverting gain of 100 mode with a source impedance of about 300Ω. The circuit is also required to operate at reasonably low frequencies with output noise of less than 0.5 mV-rms.

From Figure 34, for a closed-loop gain of 100, R_S = 300Ω, and using a standard R_4C_1 compensation, about 1.4 mV-rms of noise can be expected at the output. By further suppressing the noise at the output stage of the amplifier (pin 5) it is possible to achieve much higher noise suppression at the expense of closed-loop bandwidth.

The circuit of Figure 42 illustrates this solution where the output noise measured is less than 0.1 mV-rms and the circuit bandwidth is about 5 kHz.

Feed-Forward Technique

The MC1539 was designed with the feed-forward idea in mind. The basic principle in the feed-forward concept is to extend the power-bandwidth of the amplifier by routing the high frequencies around the first two stages of the operational amplifier, as seen in Figure 43. The high frequency boost circuit is designed to complement the natural roll-off of the compensated closed loop amplifier. The high frequency circuit takes over completely when the input frequency is too high for the input stage to

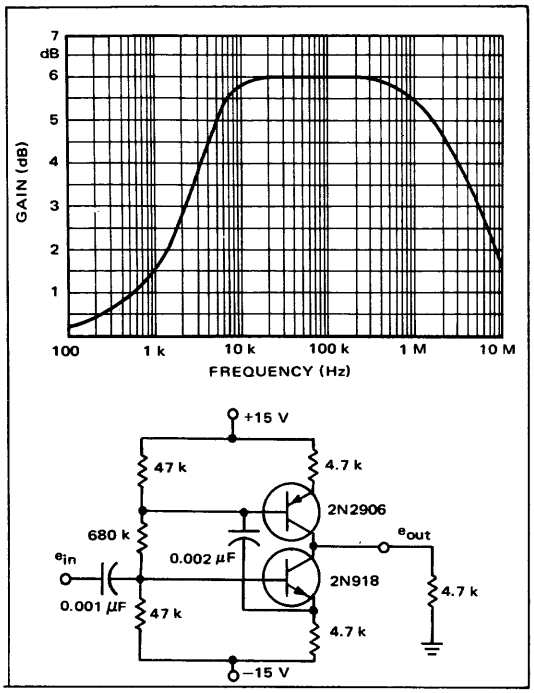


FIGURE 45 – Feed-Forward Amplifier Response.

respond, and the ultimate roll-off is due to the output stage which must pass all frequencies, and the expected roll-off due to the feed-forward amplifier.

Figure 44 illustrates the MC1539 with the feed-forward amplifier in place. In this particular configuration, a 10 volt pk-pk output (unity gain) was obtained at frequencies in excess of 1 MHz. By increasing the gain of the feed-forward amplifier, a 10 V pk-pk output signal (closed loop gain of 10) has been obtained at 2 MHz.

The feed-forward concept offers a fast responding, slow settling, response to a step function input. The relationship is developed in Appendix C, and the band-pass qualities of the feed-forward amplifier are illustrated in Figure 45.

Acknowledgment

The author wishes to thank M. Garden, K. Wolf, and M. Free for their contributions in the preparation of this note.

References

1. "Getting More Out of an Integrated Operational Amplifier Data Sheet", Motorola Application Note AN-273.
2. Millman, J. and H. Taub, Pulse, Digital, and Switching Waveforms, McGraw-Hill Book Company, 1965.
3. "The MC1535 Monolithic Dual Operational Amplifier", Motorola Application Note AN-411.
4. D'Azzo, J. and C. Houpis, Feedback Control Systems Analysis and Synthesis, Second Edition, McGraw-Hill Book Company, 1966.

APPENDIX A

INPUT OFFSET TEST CIRCUIT DEVELOPMENT

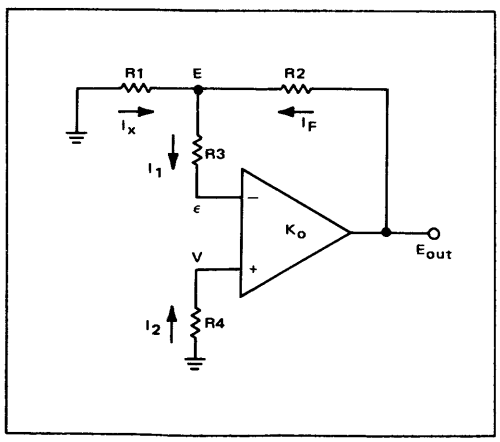


FIGURE A1 – Basic Circuit for Offset Analysis.

Assuming the basic circuit shown in Figure A1, where the amplifier has very high open-loop gain, ($k_o \rightarrow \infty$), the following can be equated:

$$E_o = k_o(V-\epsilon) \quad \text{(A1)}$$

$$V = -I_2R_4 \quad \text{(A2)}$$

$$\epsilon = E - I_1R_3 \quad \text{(A3)}$$

$$E = -I_xR_1 \quad \text{(A4)}$$

$$I_x = I_1 - I_F \quad \text{(A5)}$$

$$I_F = \frac{E_o - E}{R_2} \quad \text{(A6)}$$

These six equations can be combined and reduced (assuming $k_o \rightarrow \infty$) as:

$$E_o = -k_oR_4I_2 + k_oR_3I_1 - k_oE \quad \text{(A7)}$$

$$E = \frac{R_1}{R_2}E_o - R_1I_1 - \frac{R_1}{R_2}E. \quad \text{(A8)}$$

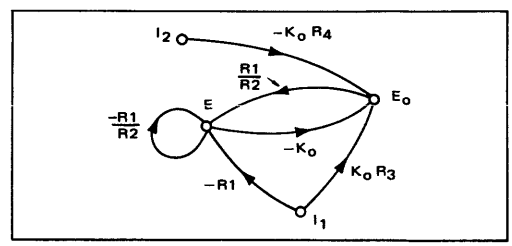


FIGURE A2 – Signal Flow-Graph of Basic Circuit.

Equations (A7) and (A8) are easily flow-graphed, as shown in Figure A2.

The output voltage (E_o) is calculated as

$$E_o = I_2\left[R_4\left(1+\frac{R_2}{R_1}\right)\right] - I_1\left[R_3\left(1+\frac{R_2}{R_1}\right)+R_2\right] . \quad (A9)$$

Equation (A9) shows the output as a function of I_1 and I_2. These two currents include both I_b and I_{io} terms as

$$I_b = \frac{I_1 + I_2}{2} \quad (A10)$$

$$I_{io} = |I_1 - I_2| . \quad (A11)$$

To eliminate the effect of the bias current (I_b) term in the output, let $R3 = 0$ and $I_1 = I_2$. E_o must now equal zero:

$$E_o = I_2\left[R_4\left(1+\frac{R_2}{R_1}\right)\right] - I_1\left[R_2\right] = 0$$

$$R_4\left(1+\frac{R_2}{R_1}\right) R_2 = 0$$

$$R_4 = \frac{R_1 R_2}{R_1 + R_2} . \quad (A12)$$

Equation (A12) shows the optimum value of R4 for eliminating the I_b error term in the output voltage.

Figure A3 illustrates a test circuit that allows the $R_3 = 0$ selection. From Figure A3, if the output is alternately measured with R_3 shorted and with R_3 in the circuit, the difference between these readings is proportional to I_{io}. The output when $R_3 = 0$ is called E_1, when $R_3 = 0$, it is called E2. The offset equations follow as

$$V_{io} = \frac{E_1}{\left(\frac{R_2}{R_1}\right)} , \quad (A13)$$

$$I_{io} = \frac{|E_1 - E_2|}{R_3\left(1+\frac{R_2}{R_1}\right)} \quad (A14)$$

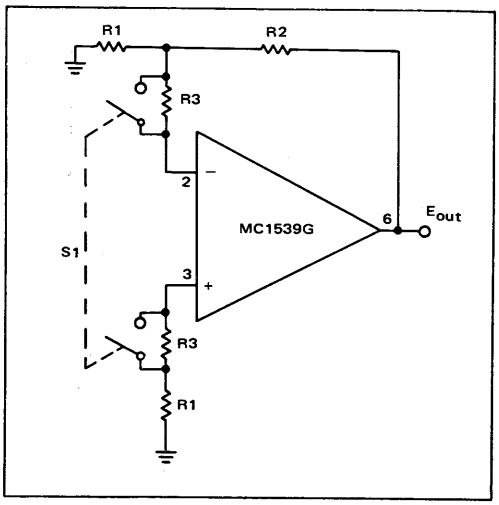


FIGURE A3 – Offset Test Circuit

As an example, let

$R_1 = 51\Omega$

$R_2 = 5.1\ k\Omega$

$R_3 = 100\ k \pm 1\%$.

Illustrative values for E1 and E2 might be

$E_1 = 83\ mV$

$E_2 = 363\ mV$.

Then from Equations (A13) and (A14),

$$V_{io} = \frac{83\ mV}{(1+100)} = 0.82\ mV$$

$$I_{io} = \frac{280\ mV}{(100\ k\Omega)(1+100)} = 27.7\ nA.$$

APPENDIX B

DEVELOPMENT OF POLE LOCATION FOR INPUT LAG COMPENSATION

Figure B1 represents the model for the input lag compensation. Writing loop equations, the following are obtained:

$$e_{in} = \left(R_X + \frac{1}{SC_X}\right) I_1 - \frac{1}{SC_X} I_2$$

$$0 = -\frac{1}{SC_X} I_1 + \left(R_4 + \frac{1}{SC_X} + \frac{1}{SC_1}\right) I_2 . \quad (B1)$$

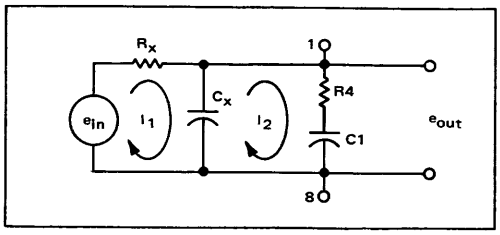


FIGURE B1 – Equivalent Circuit for Input Lag Compensation

and the output is either

$$e_{out} = \left(R_4 + \frac{1}{SC_1}\right) I_2, \tag{B2}$$

or

$$e_{out} = \frac{1}{SC_1}\ I_1. \tag{B3}$$

To formalize the notation, the system equations can be expressed as:

$$\begin{bmatrix} e_{in} \\ 0 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, \tag{B4}$$

where

$$z_{11} = R_X + \frac{1}{SC_X}$$

$$z_{12} = z_{21} = -\frac{1}{SC_X}$$

$$z_{22} = R_4 + \frac{1}{SC_X} + \frac{1}{SC_1}\ .$$

Using the above,

$$[E] = [Z]\ [I]\ , \tag{B5}$$

and if the system matrix [Z] has an inverse, the current matrix can be solved for as

$$[I] = [Z]^{-1}\ [E] \tag{B6}$$

where

$$[Z]^{-1} = \frac{\begin{bmatrix} z_{22} & -z_{12} \\ -z_{21} & z_{11} \end{bmatrix}}{\Delta} \tag{B7}$$

and

$$\Delta = z_{11}\, z_{22} - z_{12}\, z_{21}\ . \tag{B8}$$

Combining Equations (B6) and (B7), obtain

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} \frac{z_{22}}{\Delta} & \frac{-z_{12}}{\Delta} \\ \frac{-z_{21}}{\Delta} & \frac{z_{11}}{\Delta} \end{bmatrix} \begin{bmatrix} e_{in} \\ 0 \end{bmatrix}, \tag{B9}$$

or

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} \frac{z_{22}\ e_{in}}{\Delta} \\ \frac{-z_{21}\ e_{in}}{\Delta} \end{bmatrix}\ . \tag{B10}$$

Using these results in Equation (B2) or (B3), it can be shown (with rather messy algebraic manipulations) that the voltage transfer function for either expression is

$$\frac{e_{out}}{e_{in}} = \frac{K\ (S + a)}{S^2 + (bc)S + c} \tag{B11}$$

where

$$K = \frac{1}{R_X C_X}$$

$$a = \frac{1}{R_4 C_1}$$

$$b = R_X C_X + R_X C_1 + R_4 C_1$$

$$c = \frac{1}{R_X R_4 C_X C_1}\ .$$

Looking at Equation (B11) it is seen that the transfer function is a first order function divided by a second order function. The first order zero is purely a function of the frequency compensation components R4 and C1, as shown in Equation (27).

The two poles are functions of not only the external components (R4 and C1) but also of internal parameters (C_X and R_X).

From the Equation (B11), the poles are given by

$$P_{1,2} = \frac{-bc}{2} \pm \sqrt{\left(\frac{bc}{2}\right)^2 - c}\ , \tag{B12}$$

or

$$P_{1,2} = \frac{-bc}{2}\left[1 \pm \sqrt{1 - \frac{4}{b^2 c}}\right] \tag{B13}$$

The number inside the bracket in Equation (B13) will be either very small or approximately two. This indicates that one pole will be very small and the other will be approximately −bc.

Solving Equation (B13) on the computer for sufficient accuracy, the pole locations (and the zero locations from Equation (17) in the text are shown in Table A.

TABLE A – Frequency Compensated First Stage Pole and Zero Locations

R_4 (Ω)	C_1 (pF)	Zero (Hz)	Pole 1 (Hz)	Pole 2 (Hz)
390	2200	185 k	272	204 M
1 k	2200	72 k	271	80 M
10 k	2200	7.2 k	263	8.2 M
30 k	1000	5.3 k	610	2.65 M

The previous analysis holds only for the R4C1 input lag compensation combination. For the gain of 1000 compensation (R_4 = 0, C_1 = 10 pF) the 350 kHz pole is merely shifted to about 60 kHz.

APPENDIX C
BASIC FEED-FORWARD STEP RESPONSE ANALYSIS

Figure C1 illustrates a Bode Plot of the combined feed-forward, closed-loop system response. For a unit amplitude step function input, we can write, in Laplace notation:

$$V_{out} = V_{in} \cdot A_V(s) \tag{C1}$$

$$V_{out} = \frac{A_o\left(1+\frac{S}{Z_1}\right)}{S\left(1+\frac{S}{P_1}\right)\left(1+\frac{S}{P_2}\right)}$$

$$V_{out} = \frac{A_o P_1 P_2}{Z_1} \quad \frac{(S+Z_1)}{S(S+P_1)(S+P_2)} \quad , \tag{C2}$$

or in a slightly more directly usable form,

$$V_{out} = \frac{A_o P_1 P_2}{Z_1}\left[\frac{1}{(S+P_1)(S+P_2)} + \frac{Z_1}{S(S+P_1)(S+P_2)}\right]. \tag{C3}$$

To find V_{out} as a time function it is necessary to take the inverse Laplace transform of Equation (C3):

$$V_o(t) = \mathcal{L}^{-1}\left[V_{out(s)}\right] . \tag{C4}$$

by using a set of transform tables, Equation (C3) in the time domain becomes

$$V_o(t) = \frac{A_o P_1 P_2}{Z_1}\left[\frac{e^{-P_1 t} - e^{P_2 t}}{(P_1 - P_2)} + \frac{Z_1 P_2 (1 - e^{-P_1 t}) - Z_1 P_1 (1 - e^{-P_2 t})}{P_1 P_2 (P_2 - P_1)}\right]. \tag{C5}$$

Combining terms and rearranging,

$$V_o(t) = A_o + \frac{A_o P_1 P_2}{Z(P_2 - P_1)}\left[e^{-P_1 t}\left(1 - \frac{Z_1}{P_1}\right) - e^{-P_2 t}\left(1 - \frac{Z_1}{P_2}\right)\right]. \tag{C6}$$

which represents an exact expression for $v_o(t)$ as a function of pole and zero locations.

The zero (Z1) is referred to as a "phantom zero". The optimum output response results when Z1 cancels with P1. For phantom zero cancellation let $Z1 = P1\ (1 + \epsilon)$ where ϵ is small and $P2 \gg P1$ (i.e., $\frac{P1}{P2} \approx \frac{1}{400}$ or so).

If the following assumptions are made,

$$\frac{P_2 - P_1}{P_2} \approx 1$$

$$\frac{P_1(1+\epsilon)}{P_2} \ll 1$$

$$K_o = \frac{A_o P_2}{(1+\epsilon)(P_2 - P_1)}$$

then with algebraic manipulations of Equation (C6), the output voltage expression is of the form

$$V_o(t) \approx K_o\left[\epsilon(1 - e^{-P1t}) + (1 - e^{-P2t})\right. \tag{C7}$$

which is illustrated in Figure C2.

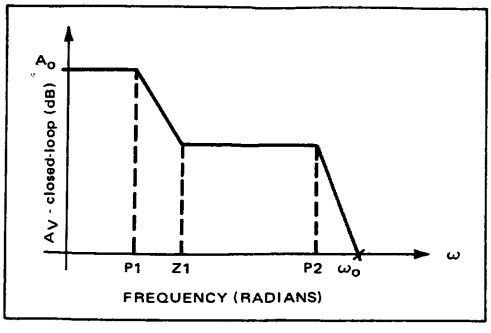


FIGURE C1 – Bode Plot for Feed-Forward System

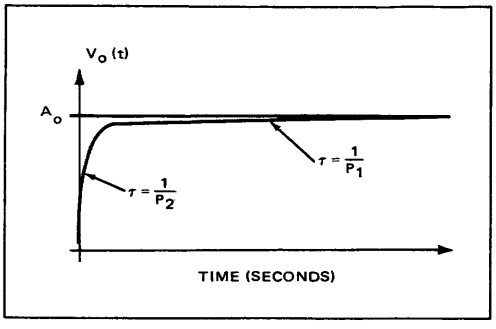


FIGURE C2 – Output Voltage-Time Response

AN-446
THE XC170 128-BIT READ ONLY MEMORY

INTRODUCTION

A Read Only Memory is a digital storage device containing information that cannot be altered during the normal operating sequence. Such a memory is often referred to by such titles as fixed-constant memory, non-alterable memory, fixed-program memory, etc. The semiconductor Read Only Memory (ROM) described herein has information stored during the manufacturing process that cannot be electrically altered. The storage pattern is inserted as the final step in the processing sequence and hence the user can obtain a given function in a custom integrated circuit at a price based upon the development of a single mask and the related processing.

The Motorola XC170 128-bit ROM is organized as 16 words by 8 bits. Four address bits (see Figure 1) provide binary-coded inputs to select the desired word. The chip also contains four enable inputs useful for address expansion. (The availability of enable inputs depends upon the package, two enable inputs are provided in the 16-pin package.) A word line is enabled (in high or "1" state) when all enable inputs are driven high. With the connections as shown in Figure 1, word line 0 will forward bias the word-line buffer transistors $Q_{0,0}$ through $Q_{0,7}$. The current from the word-line buffer transistors, $Q_{0,0}$, for example, flowing through R1 will forward bias the base-emitter junction of the bit 0 output transistor Q_{BO} and cause the output to go low. Under these conditions the presence or absence of connections between the emitters of the word-line buffer transistors and the resistor connected to the base of the output transistors (between $Q_{0,0}$ and R_1 for bit 0) determines the presence of a stored "1" or a "0" for each bit. If the connection is present and the output is low, a "1" is stored for that particular bit. Hence, the circuit is initially constructed with all "1's" stored and is programmed with the desired "0's" by etching away the link connections. Wired-ORing on the outputs is facilitated by the open collector outputs. The output transistors are capable of sinking 20 mA.

ROMs with a basic organization as described above may have a transient characteristic that is undesirable in some applications. This is only true for certain storage patterns. A "glitch" (a positive pulse in this case) may occur in the output waveform during a transition between two address states for all bits where both words contain a "1". In reference to Figure 1, suppose word 0 and 15 both had "1's" stored for bit 7. An address state change from word 0 to word 15 will cause word line 0 to go low and $Q_{0,7}$ to turn-off. The same address state change will cause word line 15 to go high, turn $Q_{15,7}$ on and drive the bit 7 output low. However, there is no guarantee that $Q_{0,7}$ will not turn off before $Q_{15,7}$ turns on and cause the bit 7 output to go high temporarily. These transition pulses may occur even if only one address input changes state.

It should be emphasized that this transition pulse occurs only if the corresponding bits of both words contain "1's". In most applications the transition pulse does not affect system operation or can be eliminated by (1) added output capacitance or (2) gating stages.

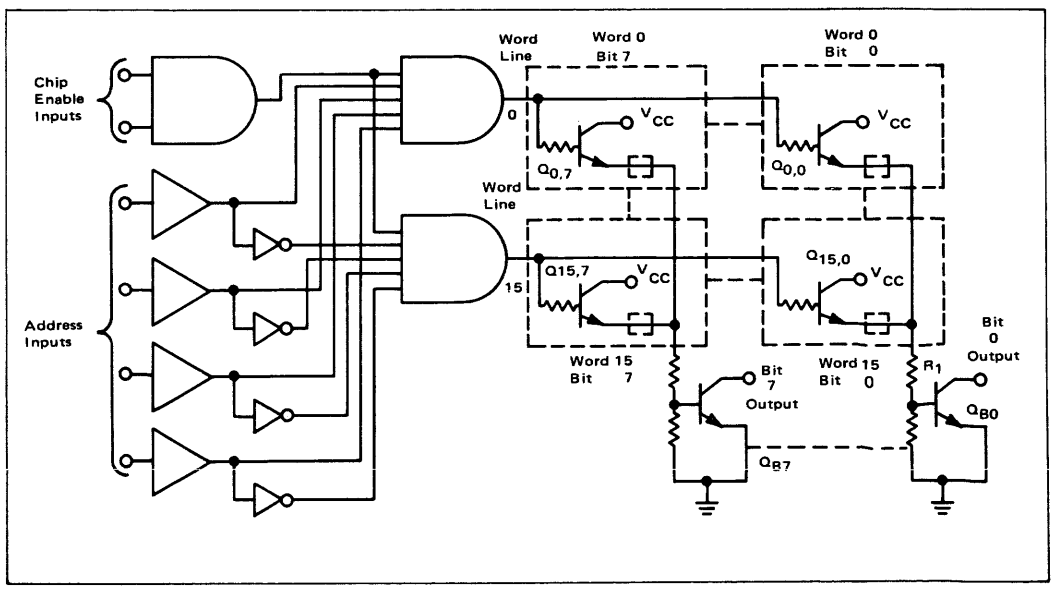
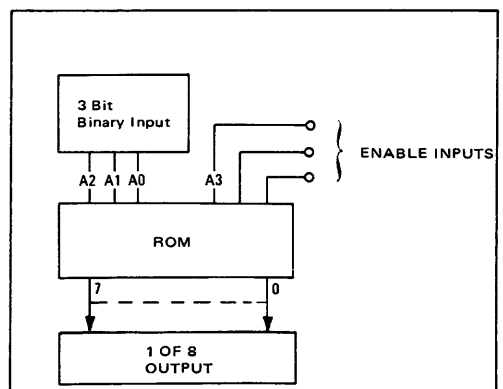


FIGURE 1 – 16 Word, 8 Bit Read Only Memory

APPLICATIONS

A large number of read only memory applications fall into the random accessing category. This classification of ROM applications may also be thought of as code translation since in these instances the function of the memory is to convert an address code to the code stored at that address. This basic concept can be used for a variety of system tasks. Typical random accessing applications discussed in this note are: (A) binary to one-of-N decoding (B) binary to two-of-eight decoding (C) data distribution (D) BCD to seven-segment indicator lamp decoding (E) binary to sixteen-segment lamp decoding (F) logic function generation (G) simple parity checking (H) Hamming single-error parity generation and detection (I) right-most one detection (J) right-most one detection and zeroing. These examples will serve to illustrate the possible uses of ROMS in the random accessing category.

Many other uses for read only memories belong in the sequential addressing category. These applications utilize the code translation function of a ROM and, in addition, use sequential addressing of memory locations to generate a series of coded information.



INPUT				OUTPUT (BIT NO.)							
A_3	A_2	A_1	A_0	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

FIGURE 2 – Binary-to-One-of-Eight Decoder

A fundamental operation in digital system is to perform, under direction of the system control, a sequence of operations on digital data. This fundamental operation is required whether the machine is wired-program controlled, stored-program controlled, or any of the intermediate compromises. In a stored program computer there are many sequences such as a sequence of instructions or the gating sequences necessary to process a single instruction. Many wired-program machines contain or can be organized to contain sequencing type circuits. Read Only Memories such as the Motorola XC-170 can provide the above sequences and thereby incorporate the advantages of arrays into many systems.

I. RANDOM ACCESSING APPLICATIONS

A. Binary to One-of-N Decoding

A binary to one-of-eight decoder can be constructed utilizing a ROM chip with the storage pattern shown in Figure 2. The three binary-coded inputs drive address lines A_0, A_1, and A_2. Address line A_3 as well as the enable inputs can be used for enable gating in this scheme. Note that the output is low for the selected bit and hence inverters may be required at the output in some applications. The need for these inverters can be eliminated by utilizing the inverted pattern shown in Figure 3 which provides a high output for the selected bit. In this variation the chip enable inputs must be permanently high to keep the outputs low when not selected. This has the disadvantage of preventing the use of the enable inputs for gating. A one-of-sixty-four decoder (Figure 4) can be constructed using nine ROM packages with the storage pattern of Figure 3.

A third useful one-of-eight decoding pattern is shown in Figure 5. Address line A_3 acts as an inversion control for the output. Hence a single part number could be used in two designs requiring inverted outputs.

B. Binary to Two-of-Eight Decoding

A four-bit binary to two-of-eight decoder is useful in a variety of applications including memory address decoding. A storage pattern fulfilling this application is shown in Figure 6.

Note that bits 0-3 decode address bits A_2 and A_3. Similarly bits 4-7 decode address bits A_0 and A_1. This circuit can also be thought of as a dual two-bit binary to one-of-four decoder.

INPUT				OUTPUT (BIT NO.)							
A_3	A_2	A_1	A_0	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1
0	1	0	0	1	1	1	1	1	1	1	1
0	1	0	1	1	1	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	1	1	0
1	0	0	1	1	1	1	1	1	1	0	1
1	0	1	0	1	1	1	1	1	0	1	1
1	0	1	1	1	1	1	1	0	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1
1	1	0	1	1	1	0	1	1	1	1	1
1	1	1	0	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1	1	1

FIGURE 3 – Inverted ROM Storage Pattern for a One-of-Eight Decoder

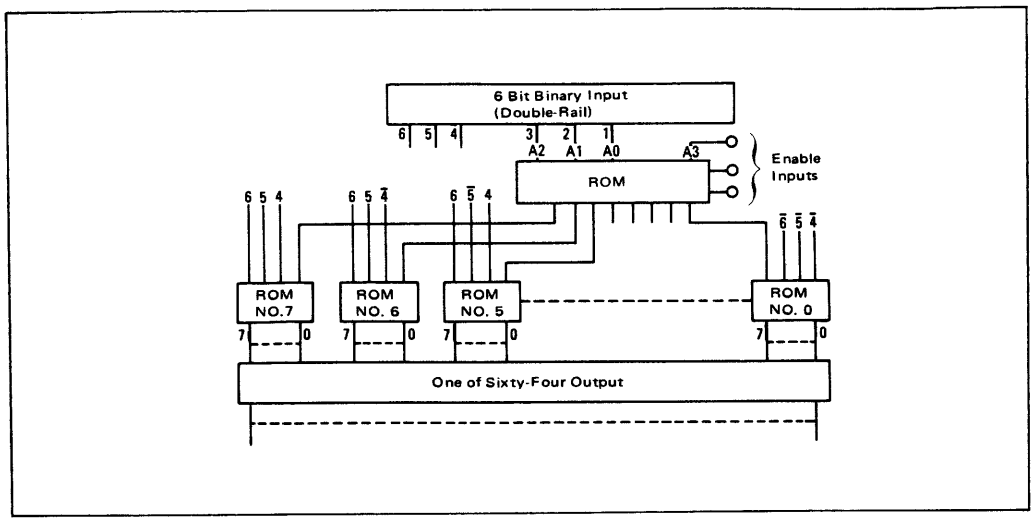


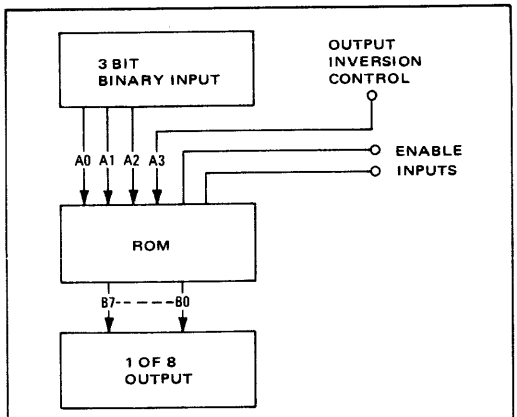
FIGURE 4 – Binary to One of Sixty-Four Decoder

C. Data Distribution

A data distributor that routes input data to one-of-N outputs as directed by the control lines is often required. The simple data distributor shown in Figure 7 routes the data appearing on the single input data line to one-of-eight outputs according to the binary information received on the three control lines.

An ROM with the storage pattern described previously for a one-of-eight decoder can provide data distribution to one-of-eight outputs. If the data line (address input line A_3 in Figure 2) is in the "1" state the output line specified by bits A_0, A_1, and A_2 contains a "1". The comments made previously concerning the use of an inverted pattern to eliminate output inverters apply here also. However, in the case of a data distributor the capability to perform the wired "OR" function at the cell output may be valuable and so the non-inverted pattern (Figure 3) may be preferred. As an example of the use of ROM chips for data distribution, a circuit to distribute eight bits of data to one-of-eight registers is shown in Figure 8. The register selection bits specify which of the eight registers is to be the destination register.

A slightly different data distribution circuit which makes use of the ROM wired "OR" output feature is shown in Figure 9. The information on the eight data lines is routed to the eight output lines as directed by the three control bits. Hence eight different combinations of routing are available. This system has some of the attributes of a switching matrix such as a crossbar switch in that the input data can be routed to any of the eight outputs as specified by the control. The various interconnection patterns can be generated: (1) external to the ROMs by utilizing a basic storage pattern such as is shown in Figure 2 and wiring the chip outputs for the appropriate interconnections or (2) internally in the ROMs by generating a separate pattern for each storage chip.



ROM STORAGE PATTERN

INPUT				OUTPUT (BIT NO.)							
A_3	A_2	A_1	A_0	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	0	0	0	1	0
0	1	1	1	0	0	0	0	0	0	0	1
1	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1
1	0	1	0	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	0	1	1	1	1
1	1	0	0	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0

FIGURE 5. Inverting/Noninverting Decoder

INPUT				OUTPUT (BIT NO.)							
A_3	A_2	A_1	A_0	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1
0	0	1	0	0	1	0	0	0	0	0	1
0	0	1	1	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	1	0	0	1	0
0	1	0	1	0	0	1	0	0	0	1	0
0	1	1	0	0	1	0	0	0	0	1	0
0	1	1	1	1	0	0	0	0	0	1	0
1	0	0	0	0	0	0	1	0	1	0	0
1	0	0	1	0	0	1	0	0	1	0	0
1	0	1	0	0	1	0	0	0	1	0	0
1	0	1	1	1	0	0	0	0	1	0	0
1	1	0	0	0	0	0	1	1	0	0	0
1	1	0	1	0	0	1	0	1	0	0	0
1	1	1	0	0	1	0	0	1	0	0	0
1	1	1	1	1	0	0	0	1	0	0	0

FIGURE 6 – ROM Storage Pattern for a Four Bit Binary to Two of Eight Decoder

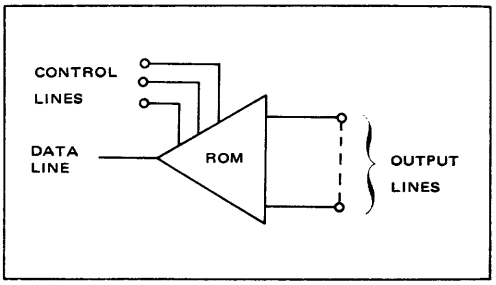


FIGURE 7. Basic Data Distributor

D. BCD to Seven-Segment Indicator Lamp Decoding

The typical ROM application requires that multiple functions be derived from a single set of input variables. The digit indicator illustrated in Figure 10 is an example of this type of requirement. In the indicator, the digits are illuminated by activating combinations of the seven individual lamps. For example, if segments 3, 4, 5, 6, and 7 are illuminated a three will appear. The indicator uses seven lamp lines in ten combinations to provide a full decimal display.

The Motorola ROM, with its 16 word by 8 bit organization, readily provides the needed indicator codes when it is programmed as shown in Figure 10. In this example, the input digit information is in BCD and is translated by the ROM to the corresponding indicator code. ROM output bit 0 provides the drive function for indicator segment 1, output bit 1 provides the function for segment 2, and so on. Note that the remaining six BCD input states and the six corresponding ROM words could be used for other characters.

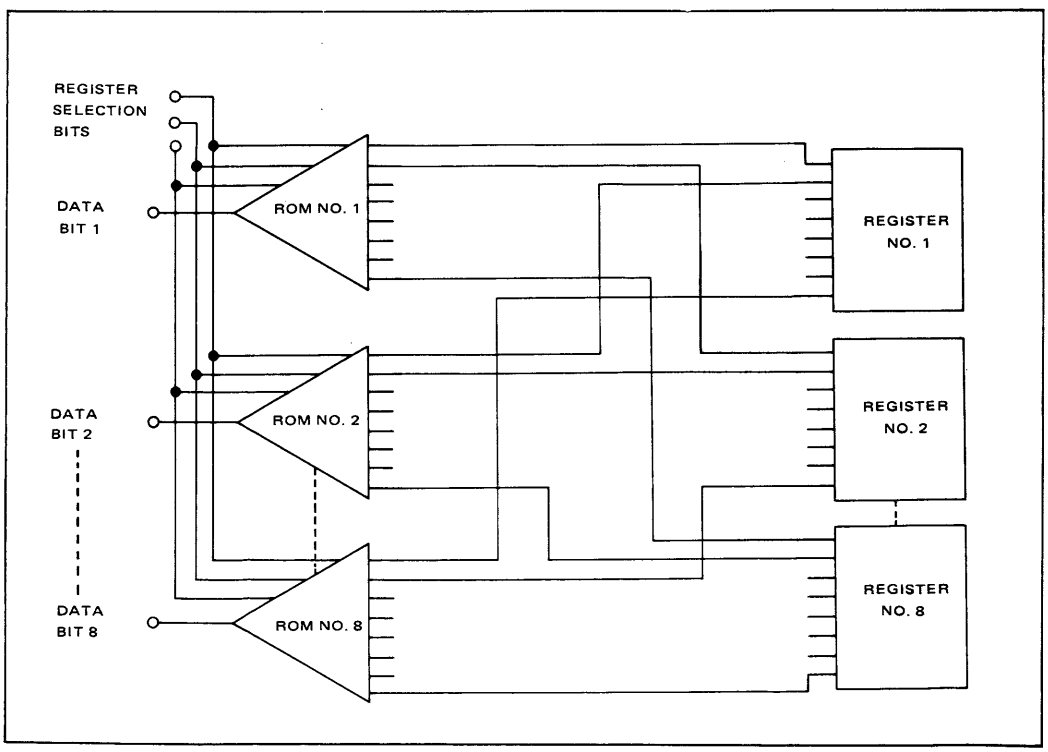


FIGURE 8 – Data Distributor — Distributes Eight Bits to One of Eight Registers

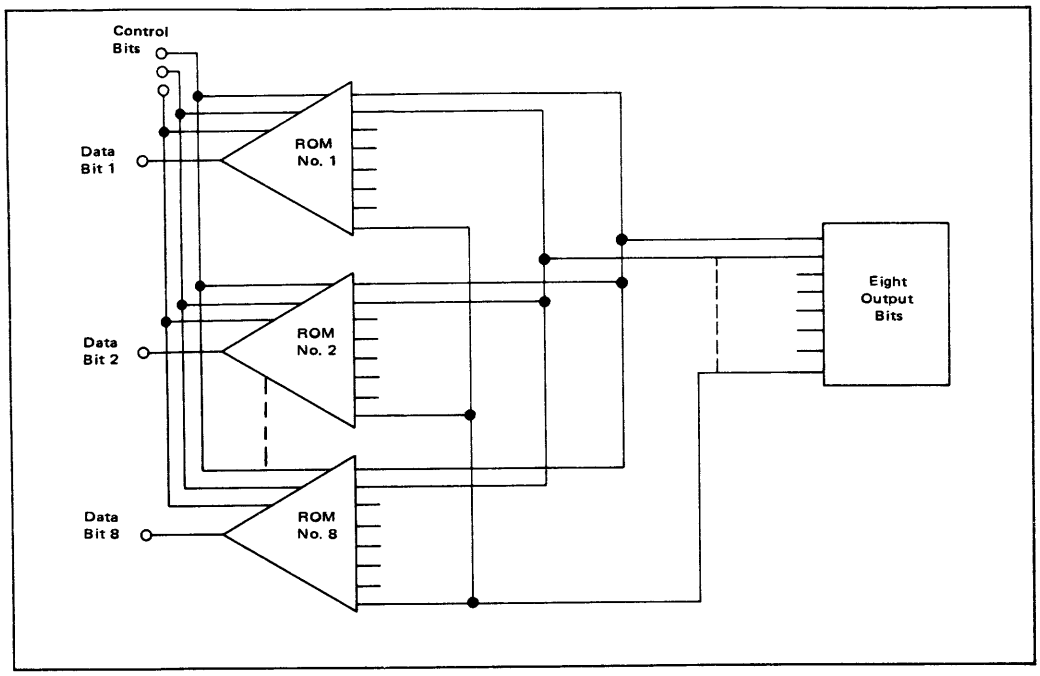


FIGURE 9 – Data Distributor – Distributes Eight Bits to Eight Output Lines

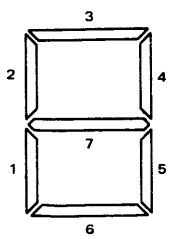
E. Binary to 16-Segment Indicator Decoding

A circuit to translate a six-bit binary word into the code necessary to drive a 16-segment indicator is shown in Figure 11. A possible character set is also shown. In order to achieve the translation with only five of the 128-bit ROMs, display of the symbols 0 through 9 is restricted to seven of the segments in the right half of the 16 segment indicator. Hence, the circuit shown provides 32 words with a 16-bit length for character display and 9 additional words for numeral display.

F. Logic Function Generation

A single cell of the ROM is capable of generating eight logic combinations of two, three, or four variables. The particular logic combinations desired will of course depend upon the system requirements. Many practical sets would probably include the following:

$$F = A_0 + A_1 + A_2 + A_3$$
$$F = A'_0 + A'_1 + A'_2 + A'_3$$
$$F = A_0 \oplus [A_1 \oplus (A_2 \oplus A_3)]$$
$$F = A_0 A_1 A_2 A_3$$
$$F = A'_0 A'_1 A'_2 A'_3$$



DIGIT INDICATOR

DIGIT	SEGMENTS ILLUMINATED	INPUT				ROM OUTPUT (BIT NO.)							
		A_3	A_2	A_1	A_0	7	6	5	4	3	2	1	0
0	1, 2, 3, 4, 5, 6,	0	0	0	0	0	0	1	1	1	1	1	1
1	4, 5	0	0	0	1	0	0	0	1	1	0	0	0
2	1, 3, 4, 6, 7	0	0	1	0	0	1	1	0	1	1	0	1
3	3, 4, 5, 6, 7	0	0	1	1	0	1	1	1	1	1	0	0
4	2, 4, 5, 7	0	1	0	0	0	1	0	1	1	0	1	0
5	2, 3, 5, 6, 7	0	1	0	1	0	1	1	1	0	1	1	0
6	1, 2, 5, 6, 7	0	1	1	0	0	1	1	1	0	0	1	1
7	3, 4, 5	0	1	1	1	0	0	0	1	1	1	0	0
8	1, 2, 3, 4, 5, 6, 7	1	0	0	0	0	1	1	1	1	1	1	1
9	2, 3, 4, 5, 7	1	0	0	1	0	1	0	1	1	1	1	0

INDICATOR CODE | INPUT CODE | ROM STORAGE PATTERN

FIGURE 10. BCD to Seven Segment Indicator Lamp Decoder

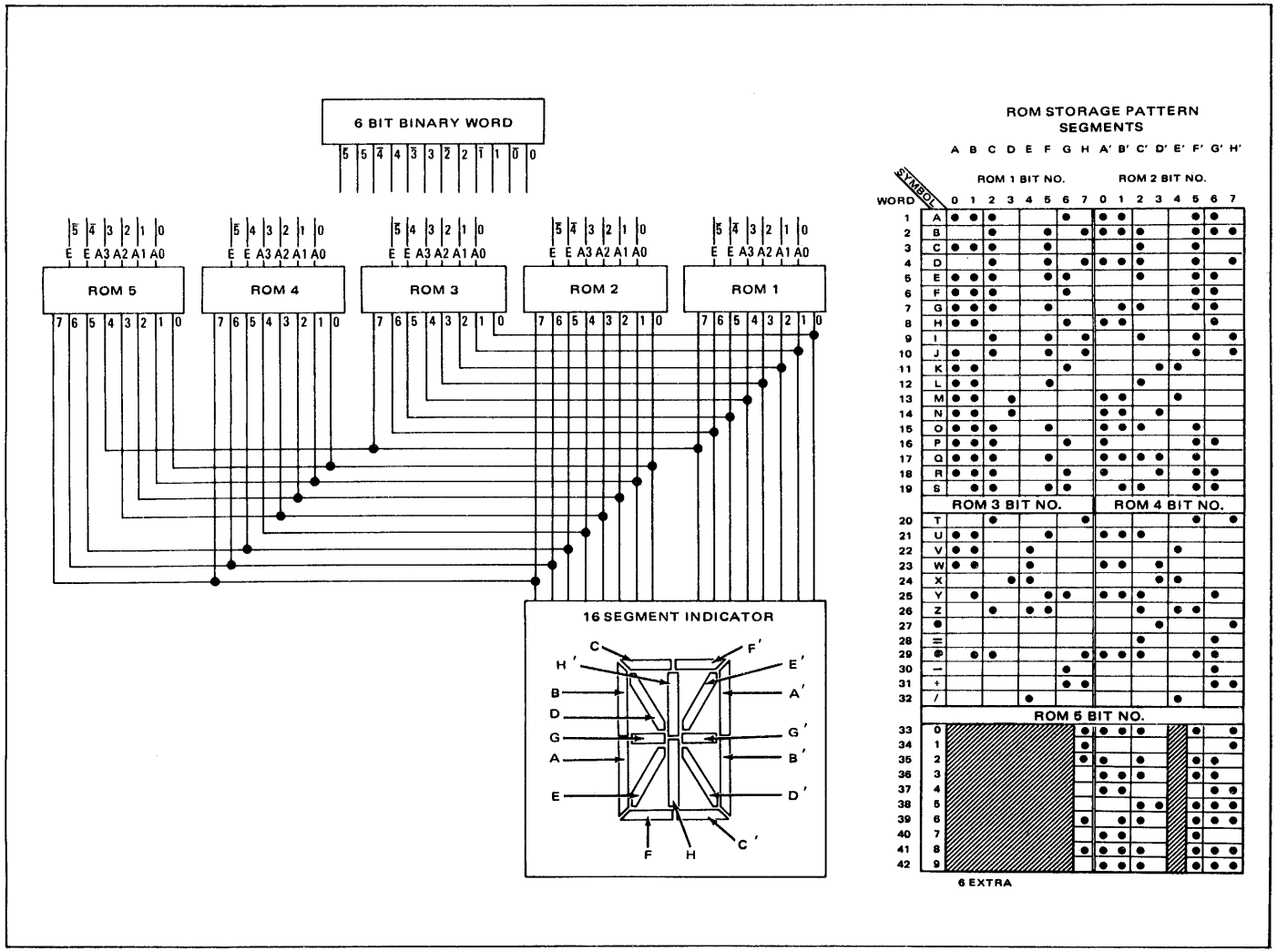


FIGURE 11. 16 Segment Indicator Decoder

G. Simple Parity Checking

A circuit to detect simple parity can be constructed with the Motorola 16-word, 8-bit ROM. Such a parity circuit has a low package count when compared with equivalent parity trees utilizing basic gate packages. All of the ROM chips needed to perform simple parity detection over a N-bit word use the same memory storage pattern.

The parity tree utilizing ROM chips is identical in concept to the tree technique used for parity detection circuits realized with gates. However, instead of three bits per tree element, this particular ROM approach examines four bits within the basic element.

The ROM cell is metalized to have a "0" in bit position 7 for all memory locations where the four address bits constitute even parity. A "1" is stored in bit position 7 for the remaining words. The ROM storage pattern is shown in Figure 12.

A parity tree utilizing five identical ROM chips to perform simple parity checking over a 16-bit word is shown in Figure 13. The bit 7 outputs from the four cells in the first level of the tree are the inputs to the single ROM needed for the second level of the tree. A "0" output from the second stage chip (ROM 5) indicates even parity and a "1" output indicates odd parity.

The parity tree can be expanded as needed to provide parity checking over a long word. A tree with three levels of decoding utilizing 21 ROM packages can serve a 64 bit word.

INPUT				OUTPUT (BIT NO.)							
A_3	A_2	A_1	A_0	7	6	5	4	3	2	1	0
0	0	0	0	0	–	–	–	–	–	–	–
0	0	0	1	1	–	–	–	–	–	–	–
0	0	1	0	1	–	–	–	–	–	–	–
0	0	1	1	0	–	–	–	–	–	–	–
0	1	0	0	1	–	–	–	–	–	–	–
0	1	0	1	0	–	–	–	–	–	–	–
0	1	1	0	0	–	–	–	–	–	–	–
0	1	1	1	1	–	–	–	–	–	–	–
1	0	0	0	1	–	–	–	–	–	–	–
1	0	0	1	0	–	–	–	–	–	–	–
1	0	1	0	0	–	–	–	–	–	–	–
1	0	1	1	1	–	–	–	–	–	–	–
1	1	0	0	0	–	–	–	–	–	–	–
1	1	0	1	1	–	–	–	–	–	–	–
1	1	1	0	1	–	–	–	–	–	–	–
1	1	1	1	0	–	–	–	–	–	–	–

FIGURE 12 – ROM Storage Pattern for an Even Parity Code

H. Hamming Single Error Detection and Parity Generation

A single error in a word can be detected by adding an extra bit to the word. By adding several extra bits to the original word, the location (bit number) of the error can be identified. One scheme for performing this function is the Hamming parity code. Single error detection and correction over a word containing four information bits will first be described.

The number of extra bits that must be added to the word is found from the inequality $2^k \geq m + k + 1$ where m is the number of information bits and k is the number of correction bits necessary. Hence, for four message bits, three correction or parity bits are necessary. These three parity bits, P_1, P_2, P_4 are inserted into the message bits M_1, M_2, M_3, M_4, in the sequence M_4, M_3, M_2, P_4, M_1, P_2, P_1. Parity bit P_1 is generated by requiring bits P_1, M_1, M_2, M_4, to possess even parity. P_2 examines P_2, M_1, M_3, M_4. P_4 examines P_4, M_2, M_3, M_4. With the parity bits calculated and inserted, parity code generation is complete and the resulting seven bit word can be stored, transmitted or go through any other operation where errors may be induced.

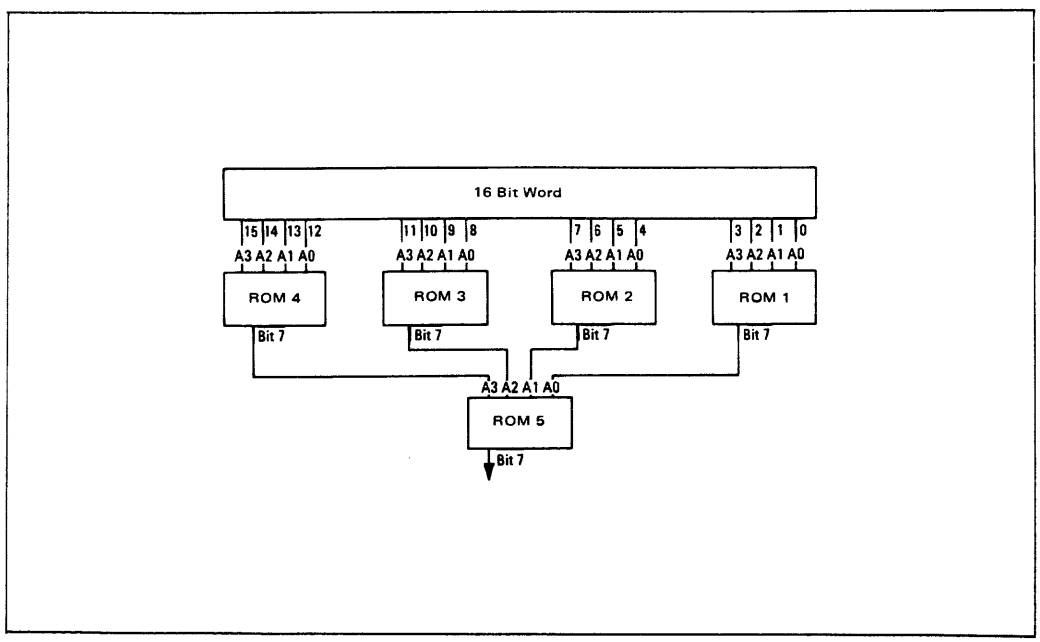


FIGURE 13 – Parity Tree For 16 Bit Word

The following procedure is used to determine if an error has been induced into a word that possesses Hamming parity bits. The three parity bits are recalculated from the transmitted message bits using the above procedure. These new parity bits are then individually exclusive-ORed with the corresponding transmitted parity bits. An output from the exclusive-OR (non-match of parity bits) shows an error has occurred and by considering the parity bit weights will indicate the position of the bit in error.

As explained, a single ROM memory chip can perform the parity generation function, but three exclusive-OR circuits plus a ROM are required to perform the error detection function over the four information bits. The ROM chip calculates the parity bits P_1, P_2, and P_4 when the four information bits serve as the address bits. Each of the 16 memory locations is programmed to contain the proper parity information for P_1, P_2, and P_4 for the corresponding combinations of input variables. Note that only three of the eight storage bits are required. As shown in Figure 14 the parity bits P_1,P_2, and P_4 are generated by a direct read of the ROM. Error detection is performed by comparing the generated parity bits with the transmitted parity bits.

Bits 1, 2, and 3 of the storage pattern shown in Figure 15 specify the pattern required to generate P_1, P_2, and P4 for the four message bits. (Bit 0 of Figure 15 is a simple odd parity bit. Bits 4-7 are used in a later example of Hamming parity generation.)

The Hamming method can be expanded to cover longer words. Consider a word with 32 information bits. According to the Hamming parity formula, the number of correction bits, k, equals 6 for this case. Figure 16 indicates the message bits of this word that are checked by the 6 parity bits. Here, as in the previous example, the idea is to choose a parity bit that will provide even parity for a new word composed of the generated parity bit and the message bits it covers.

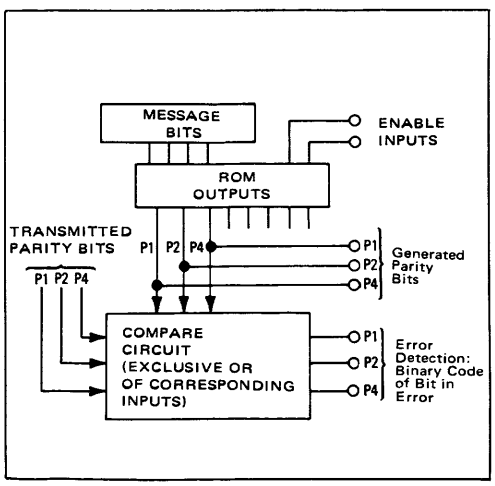


FIGURE 14 – Hamming Single Error Detection and Parity Generation 4 Message Bits

INPUT				OUTPUT (BIT NO.)							
A_3	A_2	A_1	A_0	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	1	0	0	0	1	1	0
0	0	1	0	1	1	0	1	1	0	1	0
0	0	1	1	0	0	0	1	1	1	0	1
0	1	0	0	1	1	1	0	1	1	0	0
0	1	0	1	0	0	1	0	1	0	1	1
0	1	1	0	0	0	1	1	0	1	1	1
0	1	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1	0
1	0	0	1	0	0	1	1	1	0	0	1
1	0	1	0	0	0	1	0	0	1	0	1
1	0	1	1	1	1	1	0	0	0	1	0
1	1	0	0	0	0	0	1	0	0	1	1
1	1	0	1	1	1	0	1	0	1	0	0
1	1	1	0	1	1	0	0	1	0	0	0
1	1	1	1	0	0	0	0	1	1	1	1

FIGURE 15 – Universal Storage Pattern for Hamming and Simple Parity Generation

	P_1	P_2	P_4	P_8	P_{16}	P_{32}
M_1	×	×				
M_2	×		×			
M_3		×	×			
M_4	×	×	×			
M_5	×			×		
M_6		×		×		
M_7	×	×		×		
M_8			×	×		
M_9	×		×	×		
M_{10}		×	×	×		
M_{11}	×	×	×	×		
M_{12}	×				×	
M_{13}		×			×	
M_{14}	×	×			×	
M_{15}			×		×	
M_{16}	×		×		×	
M_{17}		×	×		×	
M_{18}	×	×	×		×	
M_{19}				×	×	
M_{20}	×			×	×	
M_{21}		×		×	×	
M_{22}	×	×		×	×	
M_{23}			×	×	×	
M_{24}	×		×	×	×	
M_{25}		×	×	×	×	
M_{26}	×	×	×	×	×	
M_{27}	×					×
M_{28}		×				×
M_{29}	×	×				×
M_{30}			×			×
M_{31}	×	×	×			×
M_{32}		×	×			×
	P_1	P_2	P_4	P_8	P_{16}	P_{32}

FIGURE 16 – Hamming Parity for 32 Information Bits

P_1 is calculated by examining the bits shown for all 32 bits, i.e. M_1, M_2, M_4, M_5, etc. P_2 is calculated by examining message bits M_1, M_3, M_4, M_6, M_7, M_{10}, M_{11}, etc. Figure 16 also shows which message bits P_4, P_8, P_{16}, and P_{32} cover. Since the Motorola ROM has four address inputs the word must be handled in groups of four message bits and parity trees must be used to calculate the six parity bits for the 32 bit message. As shown in Figure 17, each ROM in the first level of the tree calculates the parity bits P_{1S} through P_{32S} for each 4 message-bit word sections. (As used here the S denotes that P_{1S} is generated over a section or group of sections of the original word, as differentiated from the master parity bit P_1 which is calculated over the entire word. In figure 7, for example, the bit 7 outputs from the first level of the parity tree could be called P_{1S}. Then the bit 7 output from ROM Z would be the master parity bit P.)

The second stage of parity calculations is performed at the second ROM tree level. (ROM X and ROM Y in Figure 17). The eight P_{1S} outputs of the first level (ROM A through H) are divided into two sets of four and serve as address inputs to ROM X and Y. The two P_{1S} outputs of ROM X and Y serve as address inputs to ROM Z. The output P_1 of ROM Z is the desired master parity bit P_1 over the 32 message bits. Likewise, in calculating each of the other parity bits, P_2, P_4, P_8, P_{16} and P_{32}, a separate 2nd and 3rd level of the parity tree shown in Figure 17 is required. Altogether, eight first level, 12 second level, and three third level ROM chips are needed for Hamming parity generation over a 32 bit word.

The preceding material serves as a general approach to Hamming parity code generation over a long word. An additional design constraint would probably be to require a single ROM pattern to be used throughout the design. Such a restraint may require more ROM parts than the method outlined in Figure 17. The following example adheres to the single part number criterion.

Figure 15 shows the entire ROM storage pattern for generating P_{1S}, P_{2S}, and P_{4S}, etc. and inserting them in the proper sequence among the four examined message bits. The bit 7 pattern represents a simple parity calculation and can be used to perform the second and third stages of the parity calculation as indicated in Figure 17. The ROM contains a "0" in bit 7 for all words at the address inputs

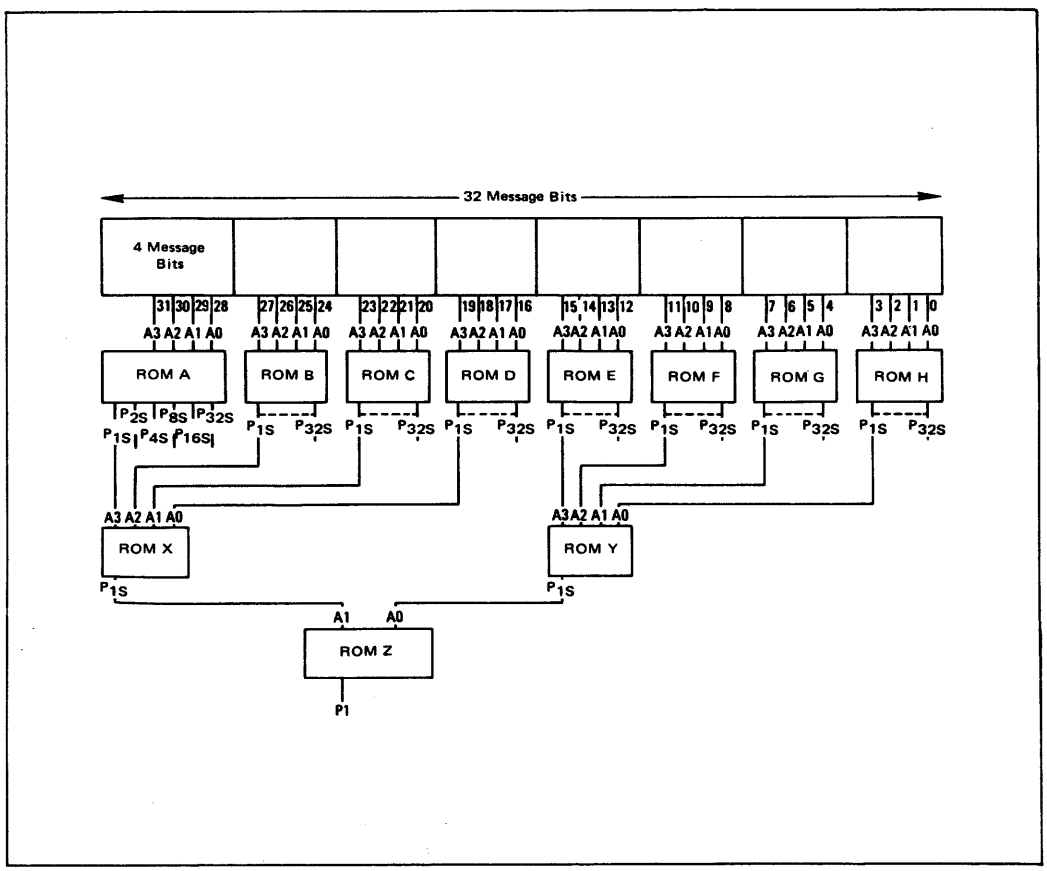


FIGURE 17–Basic Concept of Hamming Parity Generation–32 Bits

that present even parity over all four bits. This represents even parity which is useful for simple parity checking.

Figure 18 shows the 32 message bit word and proper spaces for six parity bits divided in a manner which allows the use of a single storage pattern in all ROMs needed for the generation of Hamming parity bits P_1, P_2, P_4, P_8, P_{16}, and P_{32}. For convenience, word division differs slightly from the preceding example. The basic ROM storage pattern is the one chosen to generate the required parity bits over message bits M_{23}, M_{24}, M_{25}, and M_{26}. (Section G of Figure 18, corresponding to ROM G in Figure 19).

In this case, as in the previous 32 bit example, four message bits drive ROM address inputs A_0 thru A_3 and the ROM storage pattern generates the needed parity bits. Parity bit P_{1S}, appearing at ROM output G_4 (ROM G bit 4 output), provides even parity by examining message bits M_{24} and M_{26} (on address inputs A_1 and A_3). Similarly, P_{2S} provides even parity by examining M_{25} and M_{26} while P_{4S}, P_{8S}, and P_{16S} each examine M_{23} thru M_{26}.

Note that P_1 is generated by examining every other bit of a word formed by inserting the parity bits in the message bits as shown in figure 18. The basic storage pattern (Figure 15) supplies even parity at the bit 4 output to satisfy the P_{1S} requirement for the four address bits. The P_{1S} requirement can be generated in a similar manner for any group of four message bits. Likewise, P_{2S} is generated by examining the third and fourth message bits of each section. Since the basic pattern complies with this requirement by supplying even parity at the bit 5 output, a valid P_{2S} can be generated over any group of four message bits. The same reasoning holds for P_{4S}, P_{8S}, and P_{16S}, which generate even parity over all four message bits and are supplied at the 6 and 7 output positions. The choice of outputs here depends on the fanout requirements of specific connections.

Thus a single ROM storage pattern, as described in Figure 15, provides: odd parity over four message bits at output bit position zero; even parity over four message bits at outputs one, two, and three required to generate Hamming parity bits P_1, P_2, and P_4; and the even parity needed for longer message lengths at outputs four thru seven. This enables the user to purchase ROM chips with a single pattern versatile enough to accommodate most parity generation applications regardless of word length.

By taking advantage of the simplifying relationships which resulted from the chosen message bit groupings, all the required parity bits can be obtained from this one ROM pattern. Section F, for example, requires an examination of message bits similar to that of section G except for P_{4S}. Since section F does not enter into the calculation of P_4, the ROM bit output corresponding to P_{4S} of section F is not fed into the second level of the parity tree used in calculating P_4. Sections H and I contain the only message bits examined by P_{32}, hence the simple parity or four message bits section of the ROM pattern is used. P_{32S} is obtained at ROM output 7. These and other circuit simplifications are summarized in Figure 18.

	HAMMING PARITY BIT						BIT NO.	SECTION
	P_1	P_2	P_4	P_8	P_{16}	P_{32}		
P_1	x						1	
P_2		x				2	2	
M_1	x	x					3	
P_4			x				4	A
M_2	x		x				5	
M_3		x	x				6	
M_4	x	x	x				7	
P_8				x			8	B
M_5	x			x			9	
M_6		x		x			10	
M_7	x	x		x			11	
M_8			x	x			12	C
M_9	x		x	x			13	
M_{10}		x	x	x			14	
M_{11}	x	x	x	x			15	
P_{16}					x		16	D
M_{12}	x				x		17	
M_{13}		x			x		18	
M_{14}	x	x			x		19	
M_{15}			x		x		20	E
M_{16}	x		x		x		21	
M_{17}		x	x		x		22	
M_{18}	x	x	x		x		23	
M_{19}				x	x		24	F
M_{20}	x			x	x		25	
M_{21}		x		x	x		26	
M_{22}	x	x		x	x		27	
M_{23}			x	x	x		28	G
M_{24}	x		x	x	x		29	
M_{25}		x	x	x	x		30	
M_{26}	x	x	x	x	x		31	
P_{32}						x	32	H
M_{27}	x					x	33	
M_{28}		x				x	34	
M_{29}	x	x				x	35	
M_{30}			x			x	36	I
M_{31}	x	x	x			x	37	
M_{32}		x	x			x	38	
	4	5	6 or 7					
	ROM UT		ROM OUTPUT BIT					

NOTES

1. Basic ROM pattern generated for bits 28 thru 31 (M_{23}, M_{24}, M_{25}, M_{26})
2. P_1 requires examination of every section (A – I)
3. P_2 requires examination of every section (A – I)
4. P_4 requires examination of sections A, C, E, G, I with address input A_0 (bit 4) of section A inhibited
5. P_8 requires examination of sections B, C, F, G with address input A_0 (bit 8) of section B inhibited
6. P_{16} requires examination of sections D, E, F, G with address input A_0 (bit 16) of section D inhibited
7. P_{32} requires examination of sections H, I with address input A_0 (bit 32) of section H inhibited

FIGURE 18 – Hamming Parity for 32 Information Bits

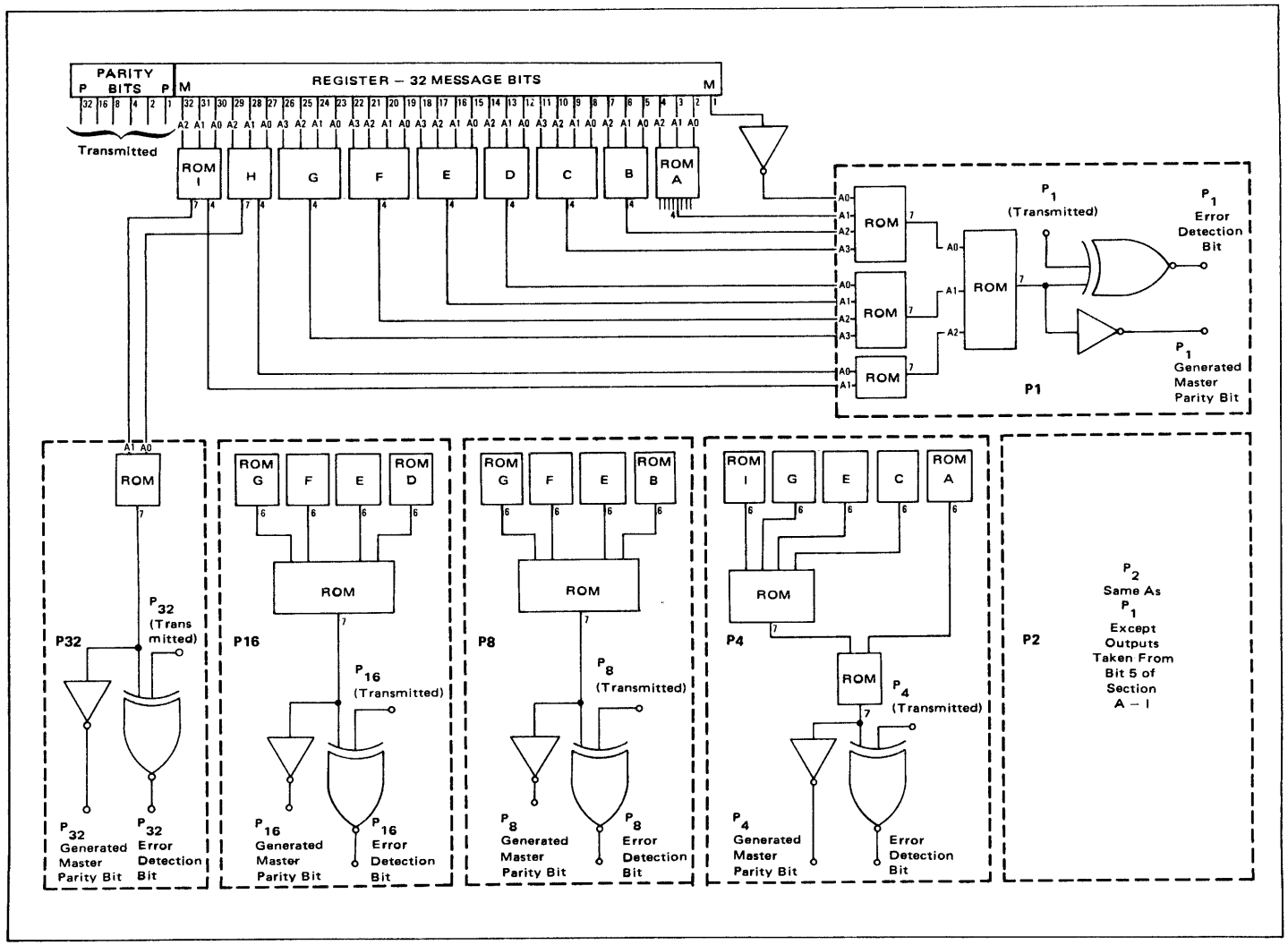


FIGURE 18. Hamming Single Error Detection and Correction Over 32 Message Bits

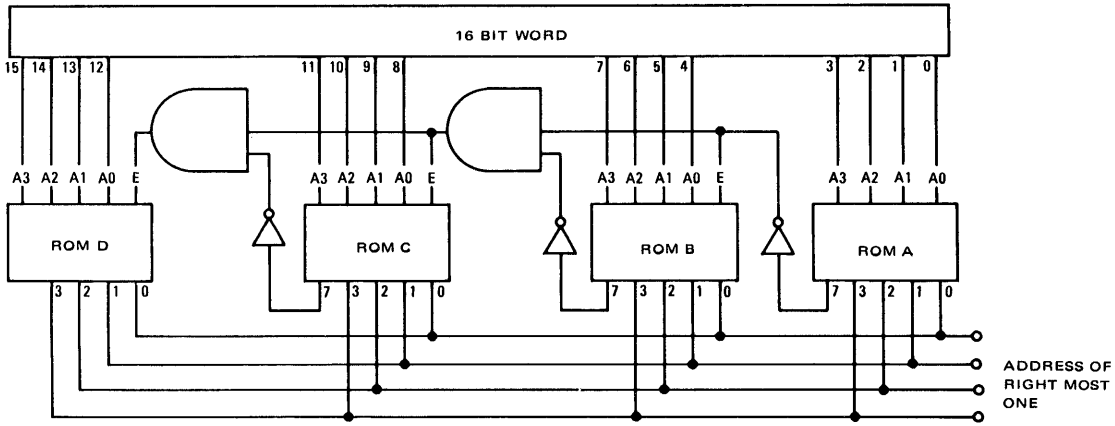


FIGURE 20. Detect Right Most One Circuit

ROM A PATTERN

INPUT				OUTPUT BIT NO.							
A_3	A_2	A_1	A_0	7	6	5	4	3	2	1	0
0	0	0	0	1	–	–	–	0	0	0	0
0	0	0	1	0	–	–	–	0	0	0	1
0	0	1	0	0	–	–	–	0	0	1	0
0	0	1	1	0	–	–	–	0	0	0	1
0	1	0	0	0	–	–	–	0	0	1	1
0	1	0	1	0	–	–	–	0	0	0	1
0	1	1	0	0	–	–	–	0	0	1	0
0	1	1	1	0	–	–	–	0	0	0	1
1	0	0	0	0	–	–	–	0	1	0	0
1	0	0	1	0	–	–	–	0	0	0	1
1	0	1	0	0	–	–	–	0	0	1	0
1	0	1	1	0	–	–	–	0	0	0	1
1	1	0	0	0	–	–	–	0	0	1	1
1	1	0	1	0	–	–	–	0	0	0	1
1	1	1	0	0	–	–	–	0	0	1	0
1	1	1	1	0	–	–	–	0	0	0	1

ROM B PATTERN

INPUT				OUTPUT BIT NO.							
A_3	A_2	A_1	A_0	7	6	5	4	3	2	1	0
0	0	0	0	1	–	–	–	0	0	0	0
0	0	0	1	0	–	–	–	0	1	0	1
0	0	1	0	0	–	–	–	0	1	1	0
0	0	1	1	0	–	–	–	0	1	0	1
0	1	0	0	0	–	–	–	0	1	1	1
0	1	0	1	0	–	–	–	0	1	0	1
0	1	1	0	0	–	–	–	0	1	1	0
0	1	1	1		–	–	–	0	1	0	1
1	0	0	0	0	–	–	–	1	0	0	0
1	0	0	1	0	–	–	–	0	1	0	1
1	0	1	0	0	–	–	–	0	1	1	0
1	0	1	1	0	–	–	–	0	1	0	1
1	1	0	0	0	–	–	–	0	1	1	1
1	1	0	1	0	–	–	–	0	1	0	1
1	1	1	0	0	–	–	–	0	1	1	0
1	1	1	1	0	–	–	–	0	1	0	1

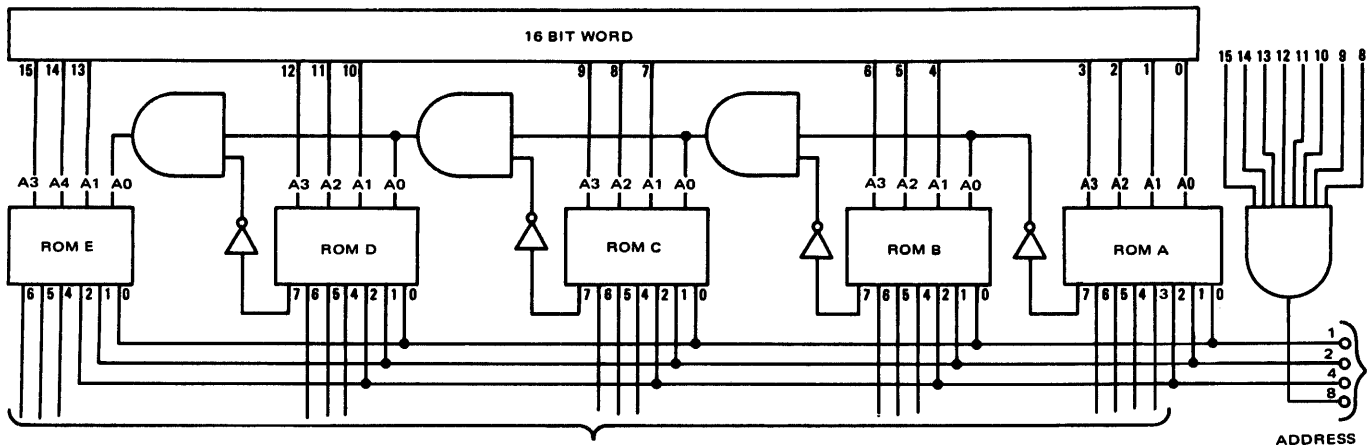


FIGURE 21. Detect and Zero Right Most One Circuit

ROM B PATTERN

INPUT				OUTPUT (BIT NO.)							
A_3	A_2	A_1	A_0	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	–	0	0	0
0	0	0	1	1	0	0	0	–	0	0	0
0	0	1	0	0	0	0	1	–	0	0	0
0	0	1	1	0	0	0	0	–	1	0	1
0	1	0	0	0	0	1	0	–	0	0	0
0	1	0	1	0	1	0	0	–	1	1	0
0	1	1	0	0	0	1	1	–	0	0	0
0	1	1	1	0	0	1	0	–	1	0	1
1	0	0	0	0	1	0	0	–	0	0	0
1	0	0	1	0	1	0	0	–	1	1	1
1	0	1	0	0	1	0	1	–	0	0	0
1	0	1	1	0	1	0	0	–	1	0	1
1	1	0	0	0	1	1	0	–	0	0	0
1	1	0	1	0	1	0	0	–	1	1	1
1	1	1	0	0	1	1	1	–	0	0	0
1	1	1	1	0	1	1	0	–	1	0	1

ROM A PATTERN

INPUT				OUTPUT (BIT NO.)							
A_4	A_2	A_1	A_0	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	1	0
0	0	1	1	0	0	0	0	1	0	0	1
0	1	0	0	0	0	0	0	0	0	1	1
0	1	0	1	0	0	1	0	0	0	0	1
0	1	1	0	0	0	1	0	0	0	1	0
0	1	1	1	0	0	1	1	0	0	0	1
1	0	0	0	0	0	0	0	0	1	0	0
1	0	0	1	0	1	0	0	0	0	0	1
1	0	1	0	0	1	0	0	0	0	1	0
1	0	1	1	0	1	0	1	0	0	0	1
1	1	0	0	0	1	0	0	0	0	1	1
1	1	0	1	0	1	1	0	0	0	0	1
1	1	1	0	0	1	1	0	0	0	1	0
1	1	1	1	0	1	1	1	0	0	0	1

The complete circuit for generating P_1 showing the 2nd and 3rd levels of the parity tree is illustrated in Figure 19. As indicated, master parity bits P_2, P_4, P_8, P_{16}, and P_{32} each must pass, like P_1, thru 2nd and possible 3rd levels of a parity tree. An exclusive-OR comparison of each master bit with the corresponding transmitted parity bit must be made, to achieve error detection.

Since a single ROM can provide both the Hamming and simple parity functions, the system to provide Hamming single error detection and parity over a word of 32 message bits requires 22 chips plus comparison circuits as shown in Figure 19. The resulting hardware saving over an implementation requiring several hundred gates illustrates the value of the ROM to the system designer. For systems where error correction circuitry has been restricted because of hardware cost, the ROM now makes additional error control economically feasible. This will result in more dependable systems.

I. Right-Most One Detection Circuits

A circuit to detect the right-most one in a word is often needed in computers which scan peripheral units. The right-most one, as used here, means the least significant bit of the word that contains a logical one. The binary code for the bit location of the right-most one within a 16 bit word can be provided by a circuit using four ROM chips requiring four bit patterns. This circuit is shown in Figure 20 along with the ROM patterns for the first 8 bits.

Detection is handled in groups of four bits starting at the least significant. Note that, if all four bits contain zeroes, the ROM storage pattern provides an output that enables the next ROM while non-enabled ROM output transistors are off. Therefore, the first ROM encountering a logical one on its address inputs has control of the detection process and provides the binary coded address of the right-most one.

J. Right-Most One Detection and Zeroing Circuits

A frequent additional requirement for the previous circuit is the capability of providing an output which consists of the original word with the right-most one (RM1) zeroed. This new word can then be examined for the next right-most one. Each ROM chip of Figure 21, if enabled, must code the RM1 address and furnish bits for the next 16 bit word. ROM A, since it is the right-most chip, merely removes the right-most one it it exists in the first four bits. The pattern for ROM A and all following chips is derived as follows. If address input A_0 is enabled (all bits examined by chips to the right of this ROM are zero) them ROM output bits three thru six should be the input address with the right-most one bit zeroed. A zero (a one somewhere to the right) for input A_0 will pass the present input to the output without alteration.

SEQUENTIAL ADDRESSING APPLICATIONS

Many applications require a series of codes to be generated in sequence. The ROM can provide a sixteen word sequence of up to eight bits by either of two methods: by sequential addressing with the use of a binary address counter, or by the use of feedback from the ROM output.

The block diagram of a sequence generator utilizing a 16-word, 8-bit ROM is shown in Figure 22. The address counter, a four-bit binary counter, causes each of the 16 words to be addressed in sequence. The code used for each 8-bit word will, of course, depend on the number of different operations to be performed. If only 8 different operations are to be performed a 1 of 8 code would be utilized. If many different operations are to be performed, a stage of translation utilizing additional ROM chips can be used to convert the storage code to a 1 of N code.

The above sequence generation method can be expanded to provide longer, multiple-of-eight word lengths and longer sequences since larger read only memories are usually required for sequence generation. Two features of the Motorola ROM were specifically included to allow memory capacity expansion: enable inputs and wired-OR output capability. To illustrate the flexibility these features provide, a 64 word, 32 bit memory requiring no additional address decoding is shown in Figure 23. As shown, the address drivers must fanout to 16 ROMS.

Sequence generators constructed from the XC-170 can be used to perform many essential functions for both stored program and wired program digital systems. Among these are: the generation of subroutines such as square roots, etc. and the control of gating sequence operations (micro-instruction generation).

The previous discussion has dealt with the use of the ROM as a combinational circuit where the present inputs completely determines the output. It is also possible to use the ROM as a sequential circuit by using feedback from one or more of the output lines.

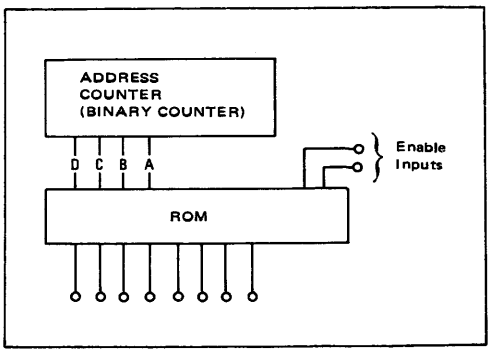


FIGURE 22. Sequence Generator

Summary

The XC-170 128 bit Read Only Memory can be used in a variety of applications where up to eight functions are to be generated from a 4-bit binary code. The basic chip permits input address expansion and has output wired-OR capability to allow the interconnection of several ROMS to form larger memories. System designers will find the Motorola 128-bit Read Only Memory an attractive alternative for custom design of integrated functions.

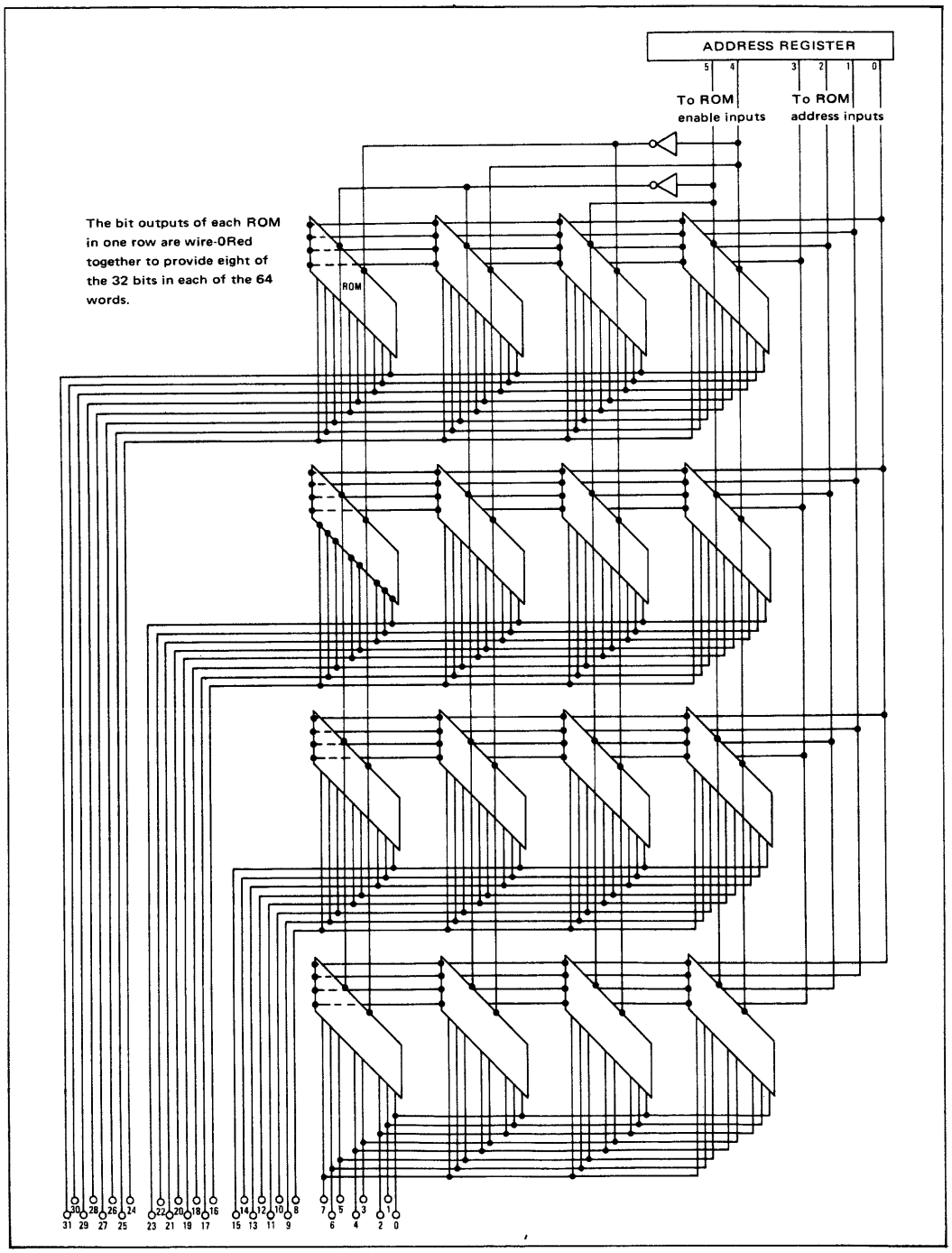


FIGURE 23— 64 Word, 32 Bit Read Only Memory

AN-456
A 50 MHz PROGRAMMABLE COUNTER DESIGNED WITH MECL II INTEGRATED CIRCUITS

INTRODUCTION

This note illustrates a programmable counter designed with elements of the MECL II digital logic family. The Divide-by-N Counter will receive any input frequency up to 50 MHz and produce a selected output frequency of F_{in}/N for any N from 2 through 999. Divide-by-N counters find applications in frequency synthesizers and other forms of digital processing instruments. The outstanding feature of the counter is its high input frequency capability that in many cases eliminates the need for any prescaling of a frequency before it is applied to the ÷ N counter.

The note is organized with an explanation of system operation followed by detailed design of each of the major sections of the counter.

SYSTEM OPERATION

Figure 1 is a block diagram showing the operation of the 50 MHz ÷ N counter. The logic diagram of the counter is illustrated in Figure 2. The divisor N is programmed into the counter by three decades of BCD input data. This can be accomplished with decimal-to-BCD encoding thumb wheel switches or any other type of decimal-to-BCD data input methods. The binary encoded divisor is gated into the decade counters while the clock line is held high by the control section. When the high level is removed from the clock line the counter begins counting down. Near the end of the countdown, the control logic decodes the binary number six (0110) and initiates a sequence that: 1) inhibits the clock line, 2) while generating an output pulse and strobing the preset gating section to condition the decade counters for the next countdown, 3) then removes the inhibit level on the clock line so that the counting sequence can begin again.

DOWN COUNTERS DESIGNS

The counter design uses MECL II JK flip-flops, the MC1013 or the MC1027, that toggle at a typical 85 MHz and 120 MHz, respectively. Their four J and four K inputs and short propagation delays make these flip-flops highly versatile in logic designs. The pin configuration of the MC1013/MC1027 is shown in Figure 3.

Three decade counters are used in the ÷ N counter design: two 9-0 BCD down-counters and a 13-4 down-counter. The two counter types are designed in a conventional manner as illustrated in Application Note AN-257 and Tables 1-5.

The use of four flip-flops in a down counter produces sixteen possible states as illustrated in Table 3. To form a

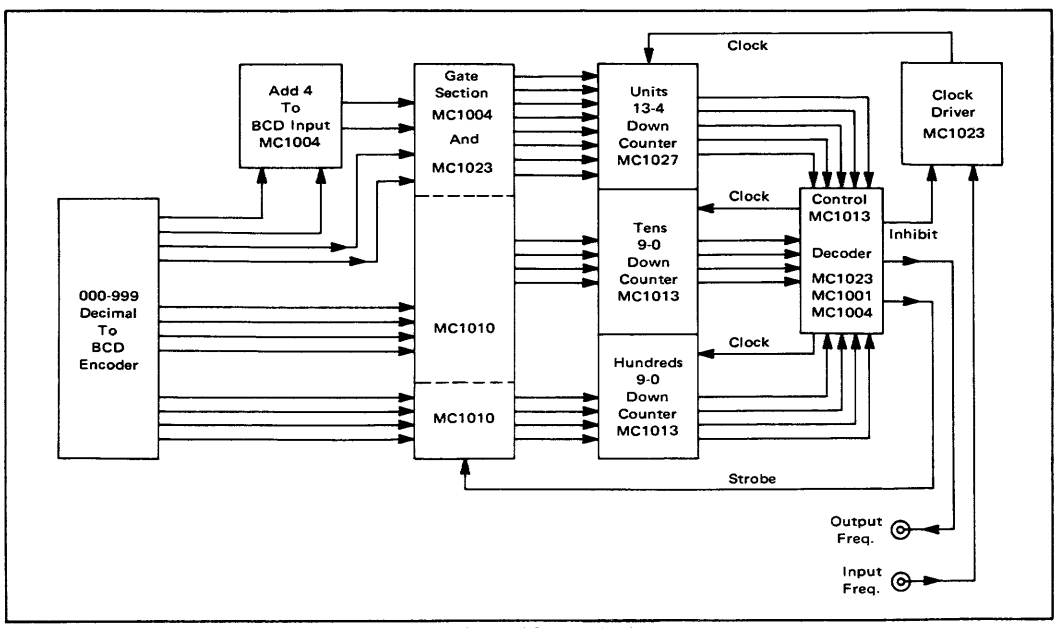


FIGURE 1 – Divide by N Counter Block Diagram

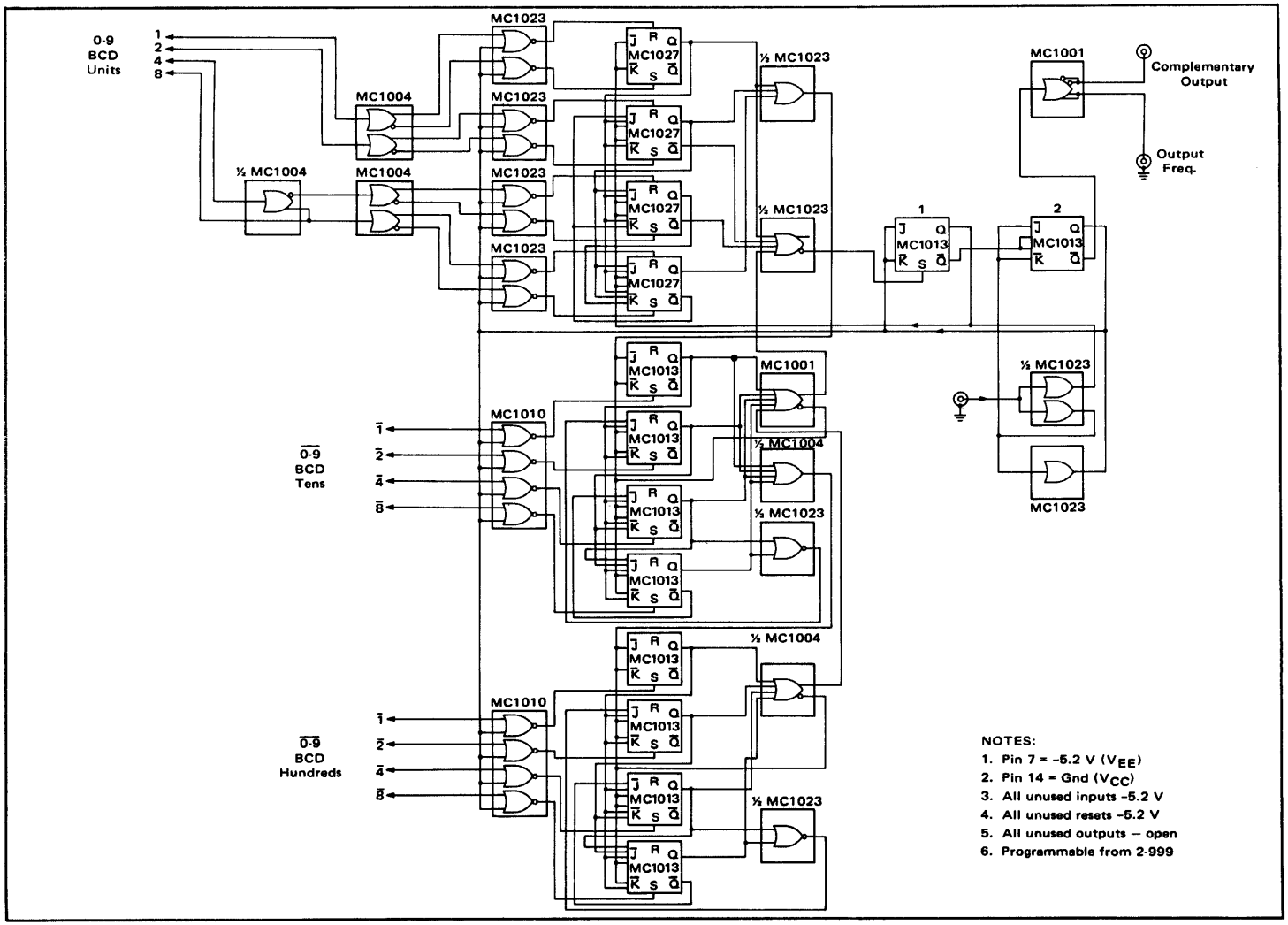


FIGURE 2 – Logic Diagram of MECL II 50 MHz ÷N Counter

counter of modulus ten, six of the possible states must be discarded. The counter must cycle through the ten desired states and, if started in an unused state, it must cycle back into one of the ten desired states to prevent lockup.

The 9-0 down counter input conditions listed in Table 4, can be transformed into a Boolean expression and simplified to the following equations by standard mapping techniques:

$$A\bar{J} = 0 \qquad A\bar{K} = 0$$
$$B\bar{J} = \bar{C}\,\bar{D} + A \qquad B\bar{K} = A$$
$$C\bar{J} = A + \bar{D} \qquad C\bar{K} = A + B$$
$$D\bar{J} = A + B + C \qquad D\bar{K} = A$$

These equations result in the 9-0 synchronous down counter shown in Figure 4. Note that an additional NOR gate is necessary to implement the $\bar{C}\,\bar{D}$ portion of the $B\bar{J}$ equation. The following worst case calculations determine the maximum operating frequency of the 9-0 down counter at 75°C.

Required down time of the clock	= 7 ns
t_{pd++} of the MC1013 flip-flop	= 9 ns
t_{pd+-} of the MC1023 gate	= 4 ns
Worst case clock period	= 20 ns
Worst case frequency of operation	= 50 MHz

The 9-0 down counter design of Figure 4 is used for both the tens and hundreds decades and may also be used in the units decade, but with some loss in maximum frequency of operation. By using the faster MC1027 flip-flops in the 9-0 down counter in place of the MC1013 flip-flops the calculated worst case frequency of operation at 75°C becomes 55 MHz.

An unusual 13-4 down counter was used in the units decade. This design yields a decade requiring no additional gating, resulting in an improvement in operating frequency. By using Table 5 and mapping techniques the following equations are obtained:

$$A\bar{J} = 0 \qquad A\bar{K} = 0$$
$$B\bar{J} = A + \bar{D} \qquad B\bar{K} = A$$
$$C\bar{J} = A + B \qquad C\bar{K} = A + \bar{D}$$
$$D\bar{J} = A + B \qquad D\bar{K} = A + B + C$$

Implementation of these input logic equations results in the down counter of Figure 5. The following worst case calculations determine the maximum operating frequency for the 13-4 down counter at 75°C

Required down time of the clock	= 7 ns
t_{pd++} of the MC1013 flip-flop	= 9 ns
Worst case clock period	= 16 ns
Worst case frequency of operation	≈ 65 MHz

TABLE 1 – Clocked $\bar{J}$-$\bar{K}$ Truth Table

Pin #	$\bar{J}$ *	$\bar{K}$ *	$\bar{C}_D$ **	Q^{n+1} 13
	ϕ	ϕ	0	Q^n
	0	0	1	$\bar{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

All other $\bar{J}$-$\bar{K}$ inputs and the R-S inputs are at a "0" level

TABLE 2 – $\bar{J}_D$-$\bar{K}_D$ Truth Table

Pin #	$\bar{J}_D$ *	$\bar{K}_D$ *	Q^{n+1} 13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\bar{Q}^n$

All other $\bar{J}$-$\bar{K}$ inputs and the R-S inputs are at a "0" level

NOTES:
1. *Any one of the $\bar{J}$ or $\bar{K}$ inputs may be used.
2. **Any $\bar{J}$ and $\bar{K}$ inputs may be tied together to form $\bar{C}_D$.
3. -0.75 V nominal is defined as a logic "1" or high level and -1.55 V nominal is defined as a logic "0" or low level. $\bar{J}$ and $\bar{K}$ refer to static levels while $\bar{J}_D$, $\bar{K}_D$, $\bar{C}_D$ refer to dynamic positive-going transitions for a "1".

A high level on a $\bar{J}$ input inhibits the flip-flop from being set by a $\bar{J}_D$ input. Likewise a "1" level on a $\bar{K}$ inhibits a $\bar{K}_D$ from resetting the flip-flop. The $\bar{J}$ and $\bar{K}$ inputs perform the "OR" function in preventing a $\bar{J}_D$ or $\bar{K}_D$ from setting or resetting the flip-flop.

TABLE 3 – Possible States

Binary Weight:	8	4	2	1
Decimal Number	D	C	B	A
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

TABLE 4 – 9-0 Counter Input Requirements

F/F	B		C		D	
STATE	$\bar{J}$	$\bar{K}$	$\bar{J}$	$\bar{K}$	$\bar{J}$	$\bar{K}$
9	1	+	1	+	+	1
8	0	+	0	+	+	0
7	+	1	+	1	1	+
6	+	0	+	1	1	+
5	1	+	+	1	1	+
4	0	+	+	0	1	+
3	+	1	1	+	1	+
2	+	0	1	+	1	+
1	1	+	1	+	1	+
0	1	+	1	+	0	+

$J_A = K_A = 0$
+ = Don't care condition

TABLE 5 – 13-4 Counter Input Requirements

F/F	B		C		D	
STATE	$\bar{J}$	$\bar{K}$	$\bar{J}$	$\bar{K}$	$\bar{J}$	$\bar{K}$
13	1	+	+	1	+	1
12	0	+	+	0	+	1
11	+	1	1	+	+	1
10	+	0	1	+	+	1
9	1	+	1	+	+	1
8	0	+	0	+	+	0
7	+	1	1	1	1	+
6	+	0	+	1	1	+
5	1	+	+	1	1	+
4	1	+	+	1	0	+

$J_A = K_A = 0$
+ = Don't care condition

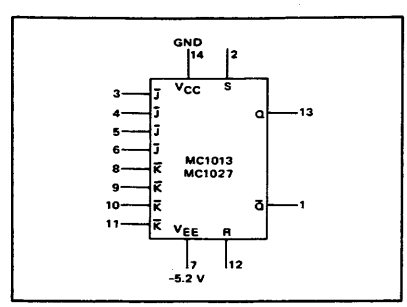


FIGURE 3 – Pin Configuration of MC1013/MC1027

If the faster MC1027 flip-flops are used in place of the MC1013 flip-flops the calculated worst case frequency of operation at 75°C is 72 MHz. All worst case frequencies are for the decade counters only, and do not include any output decoding delays. With good layout techniques the total ÷ N counter system will operate at 50 MHz over a temperature range of 0°C to +75°C.

PRESET GATING SECTION

The function of the gating section is to preset the divisor N into the set and reset terminals of the counter flip-flops when strobed by the decoder control section. The use of the 13-4 counter in the units decade requires that both the set and reset inputs of the four flip-flops be capable of being updated. There are two reasons for this requirement. First, the counter's lowest binary count is 0100 (binary 4) and not 0000 (binary 0) precluding the simple setting of the four units flip-flops as is the case in the tens and hundreds decades. The second reason is the inhibiting of the clock at count 0110 (binary 6) by the control section. This results in the toggling of Flip-Flop A (Figure 5) to a "1" level and Flip-Flop B to a "0" level. Therefore, it may be necessary to reset flip-flops A or C for certain divisors. Only the set terminals in the tens and hundreds decades need be gated at the end of a count cycle since, at strobe time, these decades have already been counted down to zero. The unused reset terminals are returned to V_{EE} (-5.2 V) on these two counters. The input gating section is illustrated in Figure 6. Note that the 9-0 down counter input gates require the 1-2-4-8 complements on their inputs.

INPUT LINE CODE TRANSLATOR FOR 13-4 COUNTER

The use of a 4-13 decade counter circuit to improve operating frequency requires that the units place of the

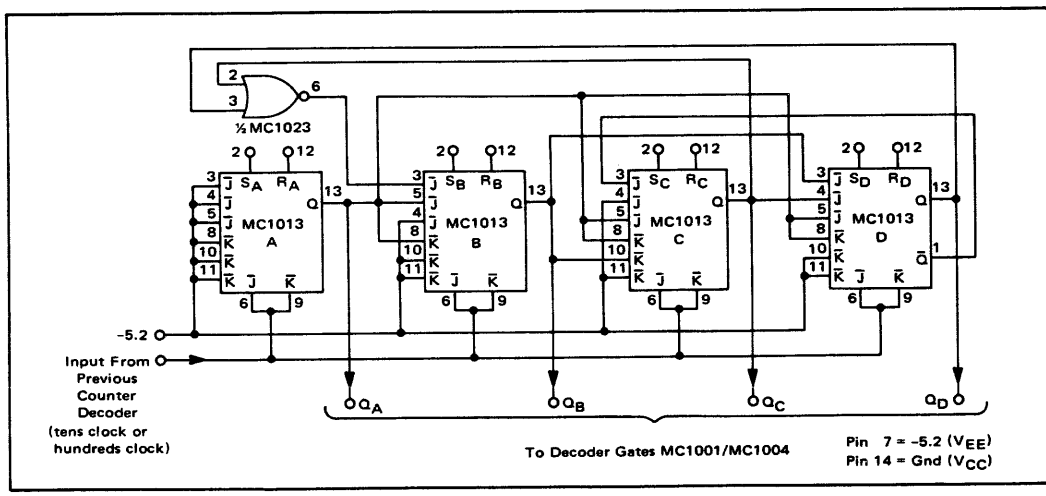


FIGURE 4 – 9-0 BCD Down Counter Tens or Hundreds Decades

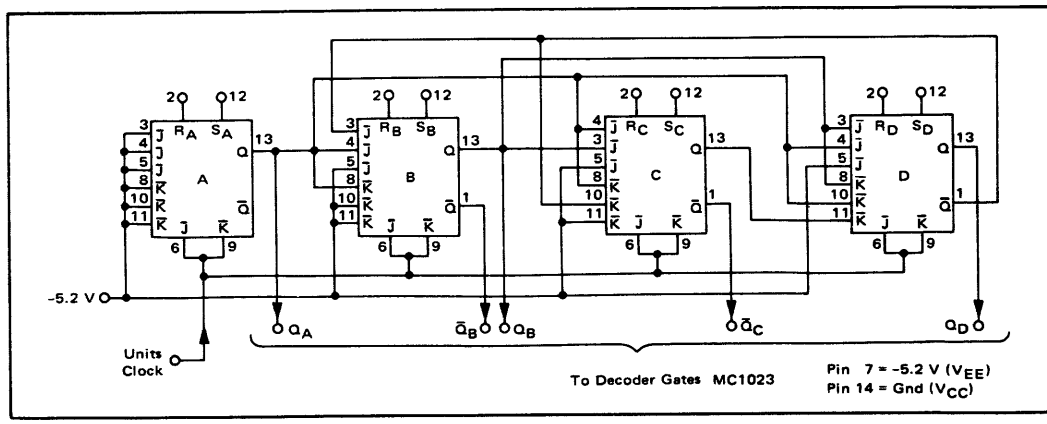


FIGURE 5 – 13-4 Down Counter Units Decade 4-MC1013 or 4-MC1027

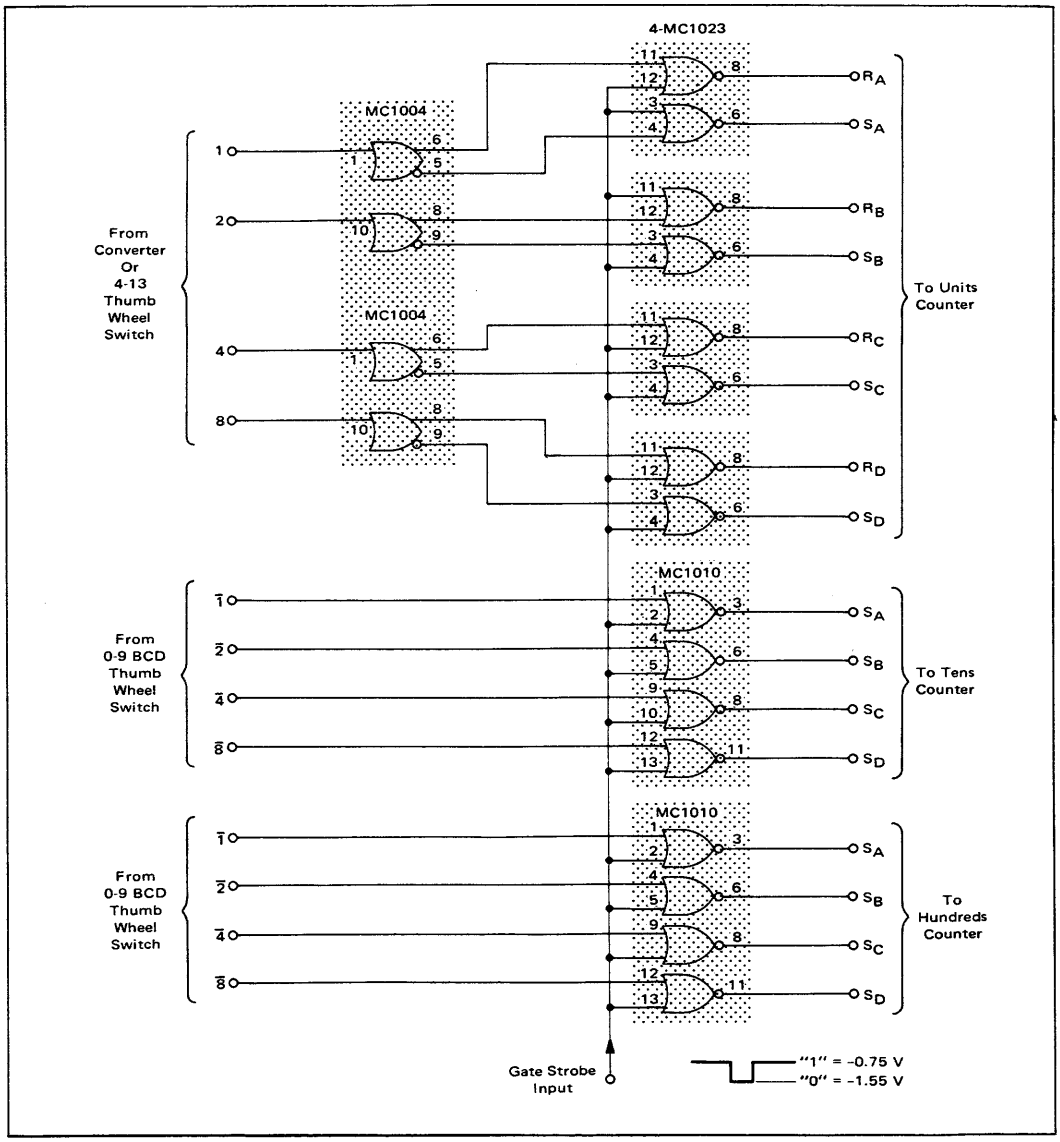


FIGURE 6 – Gating Section

TRUTH TABLE

	D	C	B	A		D'	C'	B'	A'
0	0	0	0	0	4	0	1	0	0
1	0	0	0	1	5	0	1	0	1
2	0	0	1	0	6	0	1	1	0
3	0	0	1	1	7	0	1	1	1
4	0	1	0	0	8	1	0	0	0
5	0	1	0	1	9	1	0	0	1
6	0	1	1	0	10	1	0	1	0
7	0	1	1	1	11	1	0	1	1
8	1	0	0	0	12	1	1	0	0
9	1	0	0	1	13	1	1	0	1

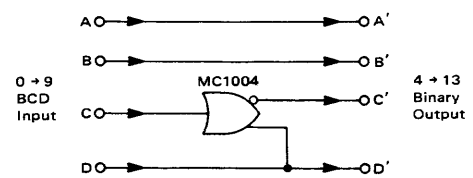


FIGURE 7 – 0-9 to 4-13 Converter

divisor, encoded in a 0-9 BCD code, be converted to a 4-13 code. This is readily done by the use of an MC1004 OR/NOR gate. This circuit, illustrated in Figure 7, could be eliminated by having the 4-13 binary code externally available, as from a special thumb-wheel switch. In addition, Figure 8 illustrates a decimal-to-BCD encoder using three 10-position switches and supplementary gating that could be used to provide the three required decades of BCD. In this encoder both the function and its complement are available.

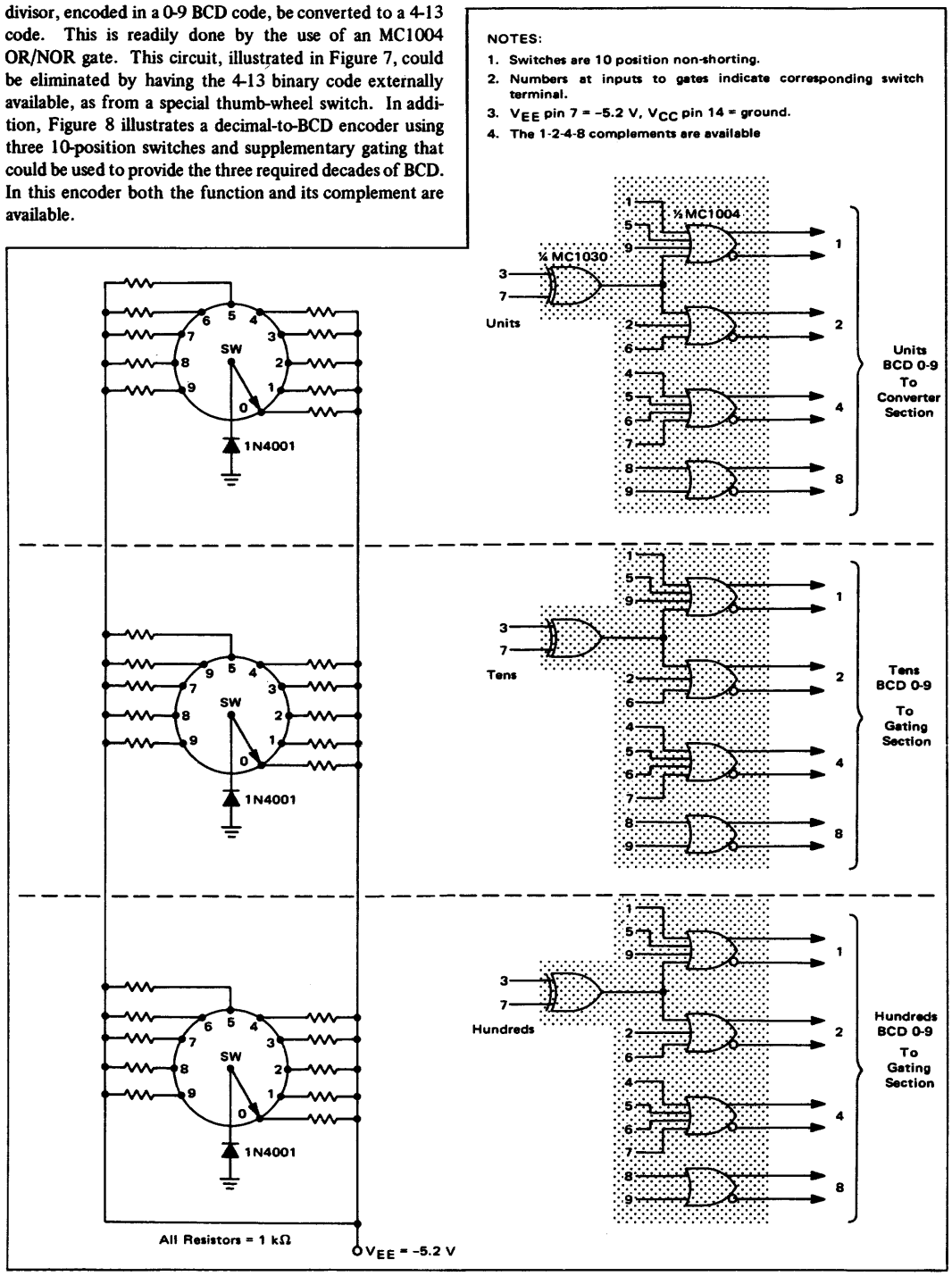


FIGURE 8 – 3 Decade Decimal to BCD Encoder

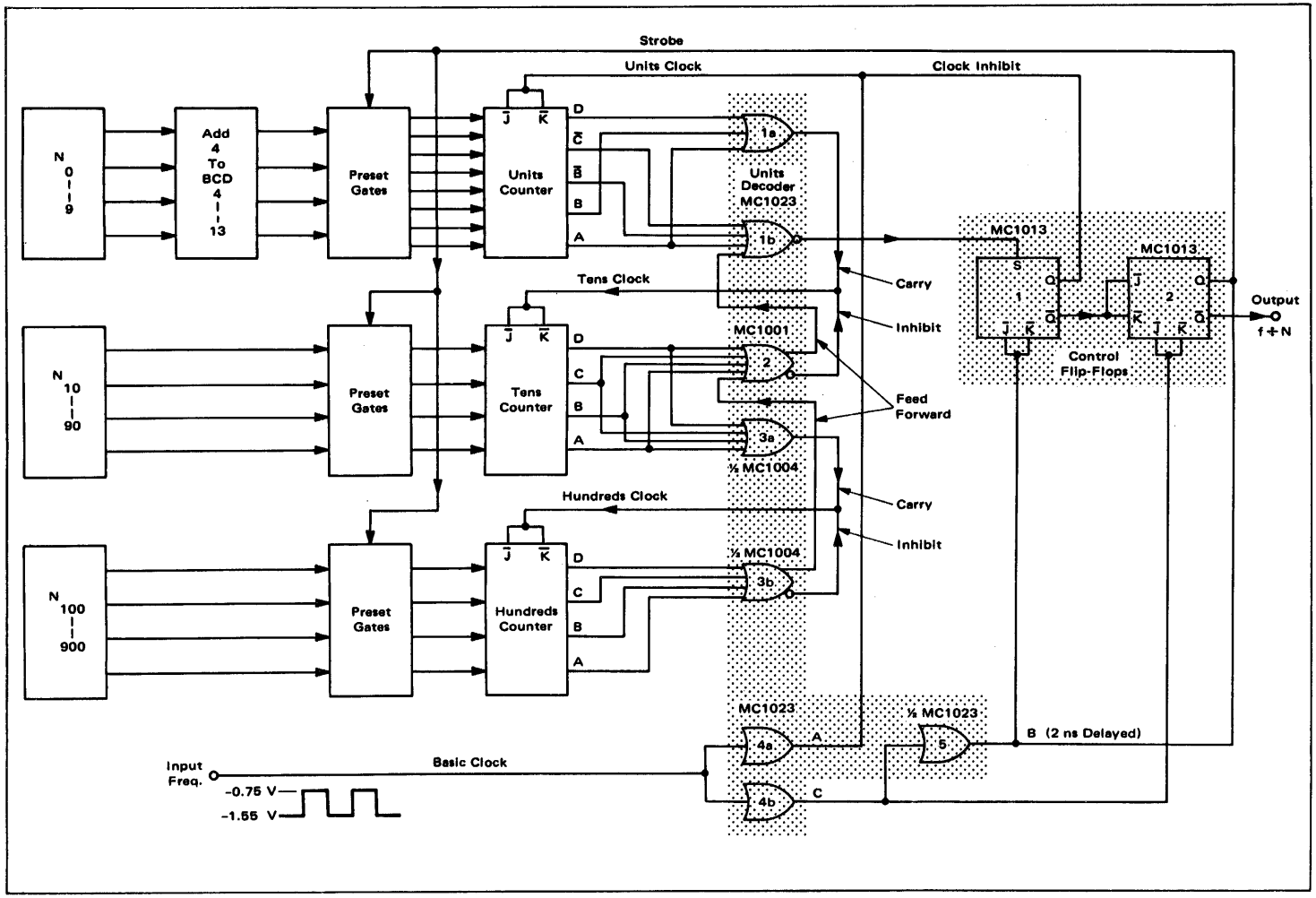


FIGURE 9 – Control Section

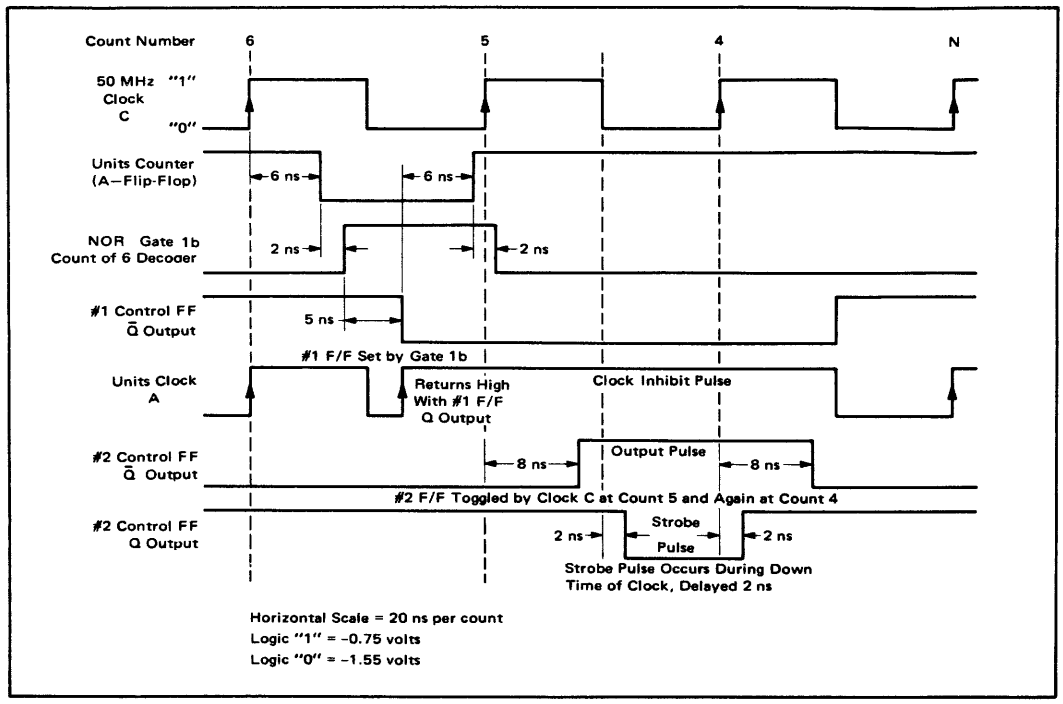


FIGURE 10 – Control Timing Diagram

CLOCK DRIVER AND DECODER

The input frequency is fed into an MC1023 clock driver, one half of which drives the four flip-flops in the units decade. The other half drives control Flip-Flop #2 and gate #5. (see Figure 9). Another MC1023 (gates 1a and 1b in Figure 9) is used in the units decade to decode a 0100 (binary 4) for the carry output, which drives the next decade counter, and a 0110 (binary 6) for the overall output decoding sequence. The sequence of events can be followed more easily by referring to Figures 9 and 10. This timing diagram represents the last portion of the decoding sequence for the units decade after previous decades have counted down to zero.

As the ÷N system counts down from its preset number (the divisor, N), the units decade repeatedly cycles through its 13 to 4 sequence. When the hundreds and tens decade have counted down to zero, a feed-forward signal is produced by an MC1001 six input OR/NOR gate connected to the tens decade as a four place binary zero (0000) decoder. This low feed-forward signal enables the decoder in the units decade (1b in Figure 9) to detect the next count of six.

Six nanoseconds after the count of six reaches the units decade clock input, the Q output of Flip-Flop A goes low. Then, two nanoseconds later, (typical MC1023 delay) the NOR output of the count of six decoder goes high. This high level sets the Q output of control Flip-Flop 1 to a logical "1" level and the $\bar{Q}$ output to a logical "0" level, after a five nanosecond delay. (Typical delay from set/reset inputs to Q/$\bar{Q}$ outputs).

Prior to this time, the Q output of Flip-Flop 1, which is wire ORed with clock A, remained at a low level and did not affect the toggling of the units counter by the positive transitions of the clock. (In a MECL system if any of the input paths to a wired OR connection are at a high level, the OR connection is maintained high). When the Q output of control Flip-Flop 1 is set to a "1" by the NOR output of the count of six decoder, the OR connection changes from low to high. The counter is thus inhibited while the strobe pulse presets the counters. Although the units counter is inhibited, the final events are sequenced by the control section so that no count is lost.

The logical "0" level on the $\bar{Q}$ output of control Flip-Flop 1 enables control Flip-Flop 2 to toggle on the next positive transition of clock C (count 5), after an eight nanosecond delay. At this time the Q output of Flip-Flop 2 goes low and its $\bar{Q}$ output goes high. The $\bar{Q}$ transition is the start of the counter output pulse.

Since the Q output is wire ORed with clock B, (the MC1023 clock driver, gate 5 in Figure 9) which is still in the positive portion of count 5, the OR connection is held high until the negative transition. The fall of clock B then serves as the leading edge of the strobe pulse. The strobe

pulse is terminated ten nanoseconds later at the positive transition of clock B entering count 4.

The count 4 positive transition on clock C will toggle control Flip-Flop 2, after an eight nanosecond delay. The change of state of the $\bar{Q}$ output terminates the 20 nanosecond output pulse. The same count 4 positive transition, that occurs two nanoseconds later on clock B than clock C, also toggles control Flip-Flop 1, after an eight nanosecond delay, to end the control sequence.

Expansion of the ÷ N counter to accept larger divisors can be accomplished in the following manner. By duplicating the decoding design employed in the tens decade, the hundreds decade can accept a feed forward decoding pulse and also generate a carry pulse. This is the only modification necessary for the addition of more BCD decade counters.

SUMMARY

This note has illustrated the use of emitter coupled logic as applied to a divide-by-N counter system. The use of this logic family provides a considerably higher operating frequency than is obtainable in a ÷ N counter system using a saturated logic family. The worst case data given in this note are conservative and, therefore, intended for system design. Due to the high frequencies of operation, performance depends heavily upon system layout and the counter will work best when used with two-sided printed circuit cards where lead lengths have been minimized. Since the introduction of higher speed MECL III, the ÷ N counter can be fabricated to operate in the 100 MHz + area.

ACKNOWLEDGMENT

The author wishes to thank Al Collum for the comprehensive data and laboratory checkout that was done in support of this note. He also wishes to convey acknowledgment to Chuck Byers for his work on the 13-4 counter.

AN-459
A SIMPLE TECHNIQUE FOR EXTENDING OP AMP POWER BANDWIDTH

INTRODUCTION

Unity gain compensation for operational amplifiers usually yields the poorest slew rate and consequently the lowest frequency-large signal swing. The listed 3 dB point may mean nothing if the available output swing is only a fraction of a volt and you need 10 volts. For most amplifiers slew rate is dependent on the size of the compensating capacitor at the input stage; the larger the capacitor (largest at unity gain), the lower the slew rate. One way to get unity closed loop response and still maintain large signal swings, is to reduce loop gain and use only as much compensation as needed. A simple method of achieving this is illustrated in Figure 1.

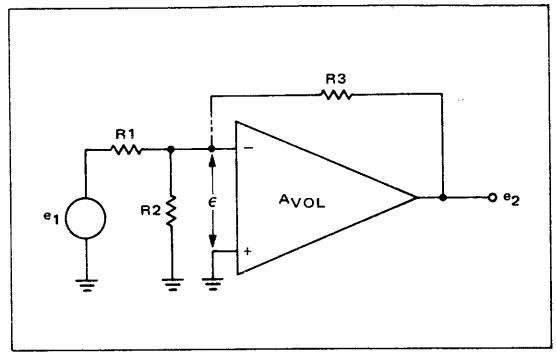


FIGURE 1 – Operational Amplifier Compensated for Unity Gain and Large Signal Swings.

CIRCUIT ANALYSIS

To analyze the circuit, error voltage ϵ may be approximated by assuming $Z_{in} >> R_3$. With this assumption, Figure 1 may be redrawn as Figure 2.

By resolving the voltage sources and their apparent source impedances (R_1 & R_3) into current sources, the circuit can be given in Norton form, Figure 3.

The error voltage can then be calculated as:

$$\epsilon = \left[\frac{e_1}{R_1} + \frac{e_2}{R_3}\right] \left[R_1 \parallel R_2 \parallel R_3\right]$$

$$\text{let } R_1 \parallel R_2 \parallel R_3 = R_{eq}$$

$$\epsilon = R_{eq}\left[\frac{e_1}{R_1} + \frac{e_2}{R_3}\right]$$

then,

$$e_2 = -A_{VOL} \times \epsilon$$

$$e_2 = \frac{-A_{VOL} \times e_1 \times R_{eq}}{R_1} + \frac{-A_{VOL} \times e_2 \times R_{eq}}{R_3}$$

$$\frac{e_2}{e_1} = \frac{-A_{VOL} \times \left[\frac{R_{eq}}{R_1}\right]}{1 + \frac{A_{VOL} \times R_{eq}}{R_3}} = -\frac{G}{1+GH} \qquad (1)$$

where $G = A_{VOL} \times \left[\frac{R_{eq}}{R_1}\right]$

$$H = \frac{R_1}{R_3}$$

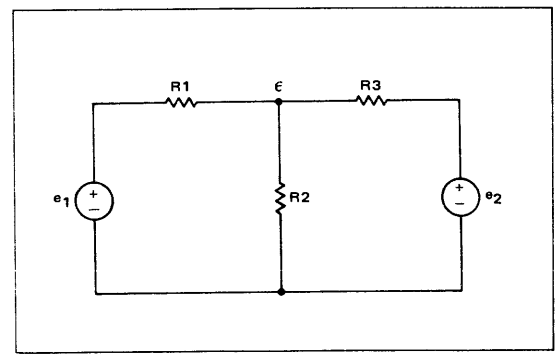


FIGURE 2 – Equivalent Circuit of Figure 1 for Calculating Error Voltage.

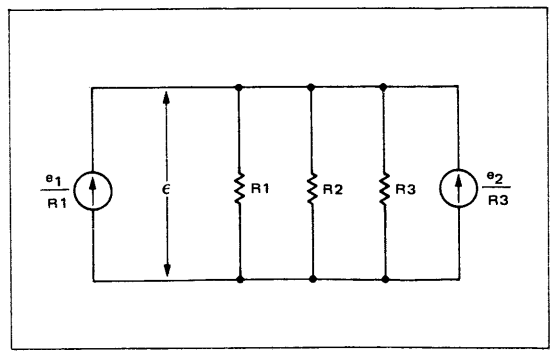


Figure 3 – Current Generator (Norton) Equivalent of Figure 2 for Error Voltage Calculation.

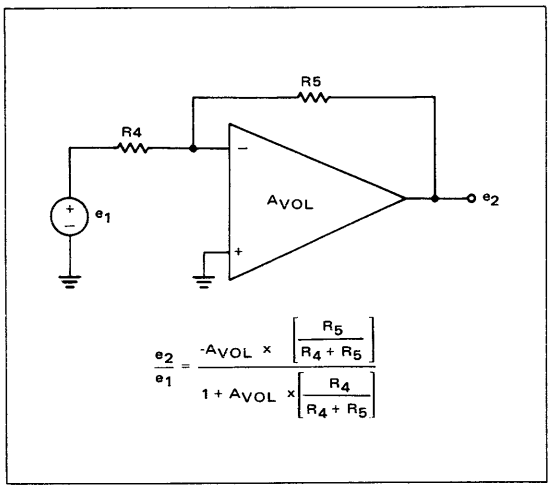


FIGURE 4 – Normal Inverting Amplifier.

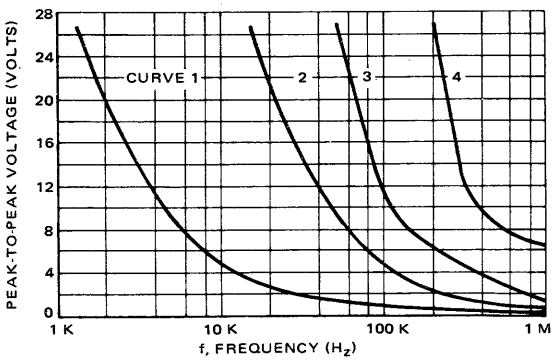


FIGURE 5 – Large-Signal Output Swing versus Frequency for the MC1533G Operational Amplifier.

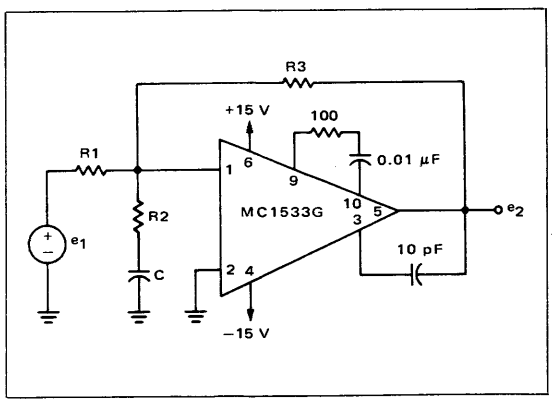


FIGURE 6 – Compensation for Eliminating Offset Multiplication.

The feedback (H) is the same as in the normal inverting configuration, but the loop gain (GH) is lower. This permits use of lighter compensation (smaller capacitor). Compensation needed may be estimated if the loop gain for this circuit is compared to that of the normal inverting amplifier (Figure 4).

Amplifier compensation given in data sheets for given values of gain actually apply more correctly to the value of loop gain

$$\left[\frac{A_{VOL}\, R_4}{R_4 + R_5}\right]$$

This is related to the closed loop gain by:

$$GH \approx A_{VOL} \times \left[\frac{R_4}{R_5}\right] = \frac{A_{VOL}}{K}$$

where K = closed loop gain.

From Equation (1):

$$GH = A_{VOL} \times \left[\frac{R_{eq}}{R_3}\right]$$

For compensation purposes, then, $K_e = \frac{R_3}{R_{eq}}$ (2)

Usually the highest data sheet slew rate is that given for K = 100. Designing an example around this value, assume $R_1 = R_3 = 100\ k\Omega$.

$$\frac{R_3}{R_{eq}} = 100 \approx \frac{R_3}{R_2} \text{ for } R_2 \ll R_1, R_3$$

$$R_2 = 1\ k\Omega.$$

The expected large signal swing for the example can be found from the data sheet for the device used. Motorola's MC1533G data sheet lists the expected output swing vs frequency for several values of compensation, (Figure 5).

From these curves the large signal (20 V p-p, 5% THD) bandwidth should be increased from approximately 2 kHz to 70 kHz by going to K = 100 compensation (curve 3). The circuit of figure 6 was built and the power bandwidth was 110 kHz (20 V p-p, 5% THD). Note that the compensation is much less than the 1 μF suggested for unity gain. This same amplifier, connected in the standard inverting configuration showed a unity gain power bandwidth of 1.8 kHz (20 V p-p, 5% THD).

TRADEOFFS

From the reduced loop gain if can be concluded that error will increase as we reach for higher slew rates. Error for the circuit of Figure 1 is given by:

$$\frac{e_o\,(\text{actual})}{e_o\,(\text{ideal})} = \frac{1}{1 + GH} = \frac{1}{1 + A_{VOL} \times \left[\frac{R_{eq}}{R_3}\right]} \approx \frac{R_3}{A_{VOL} \times R_2} \text{(dc)}$$

Error for the previous example (due to low loop gain) would typically be 0.16%. If a larger power bandwidth were desired, R_2 could be reduced to 100 Ω and the error will increase to 1.6% (discounting the effects of offsets).

The second effect, and probably most noticeable, is the increased offset voltage at the output. Even for a circuit gain of 1 the V_{io} will be multiplied by the effective gain K_e, Equation (2). If K_e = 100, the output offset due to V_{io} would be 100 x V_{io}. With addition of a capacitor in series with R_2, (Figure 6) this offset multiplication can be eliminated. For dc the gain is the same as the circuit of Figure 4, which exhibits output offset of 2 V_{io} for unity gain.

Size of C should be such that the frequency given by

$$f = \frac{1}{2\pi R_2 C}$$

is at least a decade below the loop gain 0 dB crossover. (Figure 7)

Curve 1 of Figure 7 represents a typical open loop response of an operational amplifier. If the ratio R_1/R_2 (Figure 1) were 100 (40 dB), curve 2 would represent the loop gain (with K = 100 compensation) of Figure 1. Adding capacitor C modifies the loop gain to allow normal gain for dc

$$\left(\frac{A_{VOL}}{2}\right)$$

and yet reduces to the modified loop function when

$$f > \frac{1}{2\pi R_2 C}$$

(Figure 8).

CONCLUSION

Wider power bandwidths may be easily obtained with a minimum of parts using the circuit of Figure 1. The amount of improvement depends on the predominance of the input lag network over the slew rate. When the rate of improvement diminishes (as in going from K = 100 compensation to K = 1000) then it pays to look at other external capacitors (notably, the output lag) which may be the limiting factor for rates beyond 40 V/μs. Design of the above fast response amplifiers has been straightforward without any "tricky" compensation procedures or calculations; data sheet information is all that is needed.

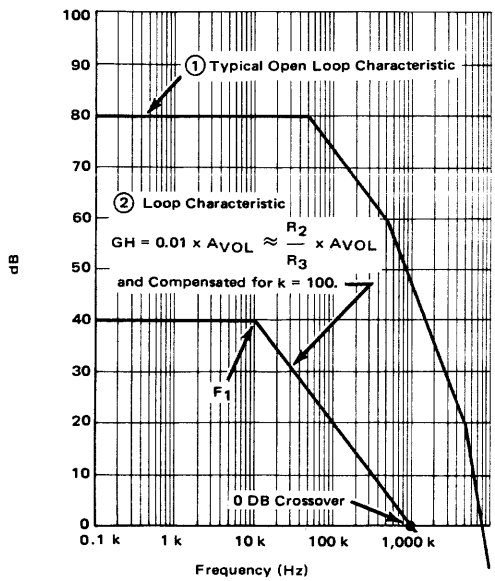


FIGURE 7 – Loop Characteristic for k = 100.

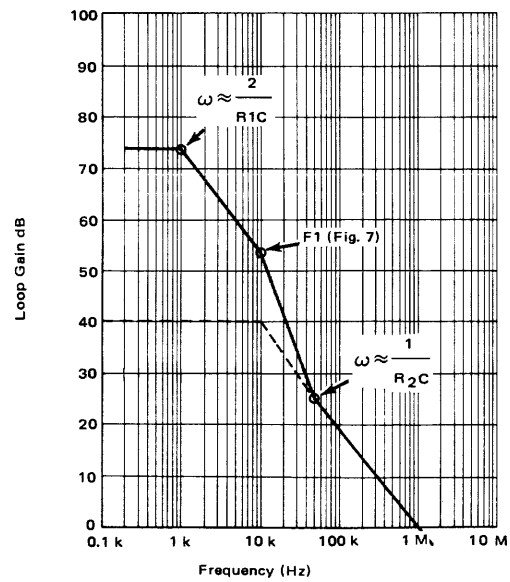


FIGURE 8 – Modified Loop Gain with x100 Compensation and Capacitor C.

AN-460

USING TRANSIENT RESPONSE TO DETERMINE OPERATIONAL AMPLIFIER STABILITY

INTRODUCTION

System stability is one of the primary concerns of a user of feedback amplifiers. Much time and effort is expended in a painstaking analysis (often undertaken with insufficient information about the characteristics of the amplifier) to confirm or insure unconditional stability. This is usually followed by extensive bench testing involving time consuming gain-bandwidth measurements. Frequently the amplifier data sheet will specify the required compensation but only for three or four different gain configurations. In an effort to save time the designer may use one of these worst case configurations, possibly resulting in the use of more restrictive compensation components than would actually be required.

The method described herein enables the designer to evaluate his design with a simple measurement, to make the indicated modifications, repeat the measurement, etc., until the desired performance is obtained. Although the example presented is for an operational amplifier, the technique is applicable to any system that can be characterized by a second-order response.

BASIS FOR ANALYSIS

Most operational amplifiers have an uncompensated, open-loop frequency response that can be approximated by the form shown in Figure 1-A, the familiar Bode plot, where the vertical scale is magnitude in dB and the horizontal log scale is frequency.

The equation representing this response is:

$$A_{VOL} = \frac{A\,\omega_0\,\omega_1\,\omega_2\,\omega_3}{(s+\omega_0)(s+\omega_1)(s+\omega_2)(s+\omega_3)}. \qquad (1)$$

However, when the open-loop amplifier is compensated for use as a feedback amplifier with a closed loop gain as low as unity, the slope of the compensated open loop Bode plot as it passes through zero dB must be less than 12 dB/octave or the closed loop system will be unstable. If the open loop slope is a constant 6 dB/octave (single pole), the closed system is unconditionally stable and the output waveform will have no overshoot to a step input. This is a trivial solution and will not be included in the discussion of this paper. For open loop compensated amplifiers that have a slope greater than 6 dB/octave, the closed loop system is marginally stable (having a certain amount of phase margin) and will possibly have overshoot in its step response and peaking in its frequency response. Therefore, the most general open loop, compensated amplifier system that can be used in closed loop systems with gains greater than or equal to unity is a two pole system. Hence, the generalized two pole system will be the subject of this paper. For this case the response is given by:

$$A'_{VOL} = \frac{A\,\omega_0\,\omega_1}{(s+\omega_0)(s+\omega_1)} \qquad (2)$$

A Bode plot of this equation is shown in Figure 1-B. When the amplifier is used in a closed loop configuration, with a feedback of β, the closed loop gain with negative feedback is given by

$$A_{VCL} = \frac{A'_{VOL}}{1 + A'_{VOL}\beta}. \qquad (3)$$

Substituting equation (2) into (3) yields

$$A_{VCL} = \frac{\dfrac{A\,\omega_0\,\omega_1}{(s+\omega_0)(s+\omega_1)}}{1 + \dfrac{A\beta\,\omega_0\,\omega_1}{(s+\omega_0)(s+\omega_1)}}. \qquad (4)$$

Simplifying and replacing s by $j\omega$ gives:

$$A_{VCL} = \frac{A\,\omega_0\,\omega_1}{(j\omega+\omega_0)(j\omega+\omega_1) + A\beta\,\omega_0\,\omega_1}. \qquad (5)$$

Further manipulation will put it into standard form. i.e.,

$$A_{VCL}(\omega) = \frac{1/\beta}{\left[1 + j\omega\left(\dfrac{\omega_0+\omega_1}{A\beta\,\omega_0\,\omega_1}\right) + \dfrac{1}{A\beta\,\omega_0\,\omega_1}(j\omega)^2\right]}, \qquad (6)$$

which is precisely the response for a second order system, as will be shown.

THEORETICAL BASIS

A second order system can be described by the following general differential equation:

$$\frac{d^2x}{dt^2} + a\frac{dx}{dt} + bx = c. \qquad (7)$$

As derived in the appendix, a general transient solution for this, when c is a step input, is:

$$x(t) = ke^{-\left(\zeta\omega_n t\right)}\left[\sin\left(\omega_n\sqrt{1-\zeta^2}\,t + \phi\right)\right]. \qquad (8)$$

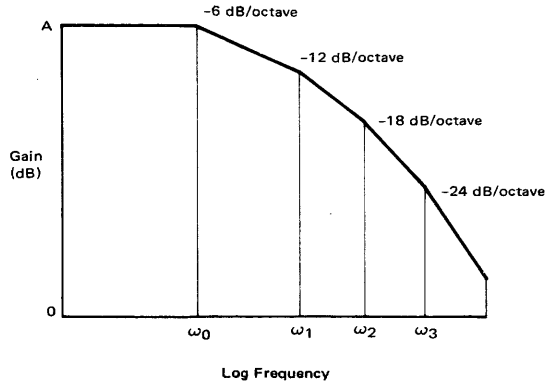


FIGURE 1-A – Typical Open Loop Operational Amplifier Frequency Response

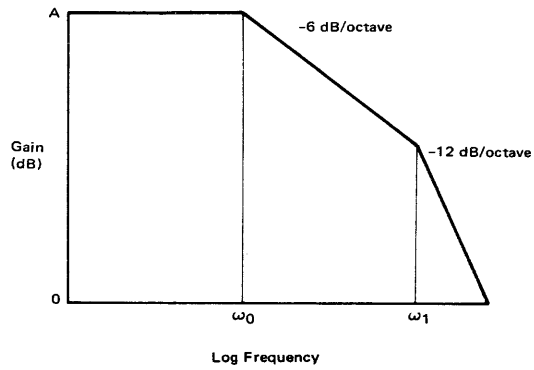


FIGURE 1-B – Open Loop Compensated Operational Amplifier Response

The preceding response is a sine wave of frequency

$$\omega_d = \omega_n \sqrt{1-\zeta^2} \tag{9}$$

and amplitude

$$A = ke^{-\zeta\omega_n t}, \tag{10}$$

where ω_d is the damped frequency of oscillation, ζ is called the damping ratio, and ω_n is the natural (or undamped) frequency of oscillation. The total solution (including steady state) for an amplifier with a closed loop gain of A_{VCL} is

$$V_o(t) = A_{VCL}\left[1 - \frac{e^{-(\zeta\omega_n t)}}{\sqrt{1-\zeta^2}} \sin\left(\omega_n\sqrt{1-\zeta^2}\, t + \cos^{-1}\zeta\right)\right] \tag{11}$$

Neglecting A_{VCL} for the moment as a scale factor, then $V_o(t)$ plotted as a function of t would appear as in Figure 2.

We are interested in easily measured parameters of this response which will enable us to completely characterize it, i.e., find ζ and ω_n. As derived in the appendix, knowing the values of the first three peaks and when in time the first and third peaks occur, ζ and ω_n are as follows:

$$\zeta = \frac{\left|\log_{10}\left(\frac{V_{p1}-V_{p3}}{V_{p2}}\right)\right|}{\sqrt{\log^2 10\left(\frac{V_{p1}-V_{p3}}{V_{p2}}\right)+1.8615}} \tag{12}$$

$$\omega_n = \frac{2\pi}{(t_3-t_1)\sqrt{1-\zeta^2}}. \tag{13}$$

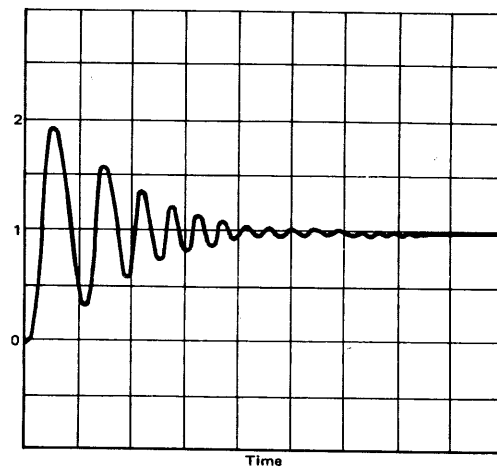


FIGURE 2 – Transient Response of Second Order System

Thus the response can be completely characterized by taking these five measurements from one test set-up.

The response of the system can also be evaluated in the frequency domain. As derived in the appendix, the corresponding characteristic equation in the frequency domain for a second order system is:

$$\frac{A_{VCL}}{\left[1 + j\omega\left(\frac{2\zeta}{\omega_n}\right) + \frac{1}{\omega_n^2}(j\omega)^2\right]}. \tag{14}$$

Equation (14) can be compared term-for-term with Equation (6) to show what effect A, β, ω_0, and ω_1 have on determining A_{VCL}, ω_n and ζ.

This gives the following relationships:

$$A_{VCL} = 1/\beta, \tag{15}$$

$$\omega_n = \sqrt{A\beta(\omega_0)(\omega_1)}, \tag{16}$$

$$\zeta = \frac{\omega_0 + \omega_1}{2\sqrt{A\beta(\omega_0)(\omega_1)}}. \tag{17}$$

Equation (15) confirms what would be expected, i.e., that the closed loop gain is inversely proportional to β, indeed is equal to $1/\beta$. Equation (16) shows that for a given set of break frequencies (ω_0 and ω_1) the natural frequency is proportional to the square root of the product of A and β. Since A is the open loop gain and $1/\beta$ is the closed loop gain, the product $A\beta$, called the loop gain, is a measure of how much the amplifier has been closed down. In a similar manner, Equation (17) shows that ζ is inversely proportional to the square root of $A\beta$ and verifies the fact that as the loop is closed down more and more, that is β becomes larger, ζ becomes smaller and the amplifier becomes less stable.

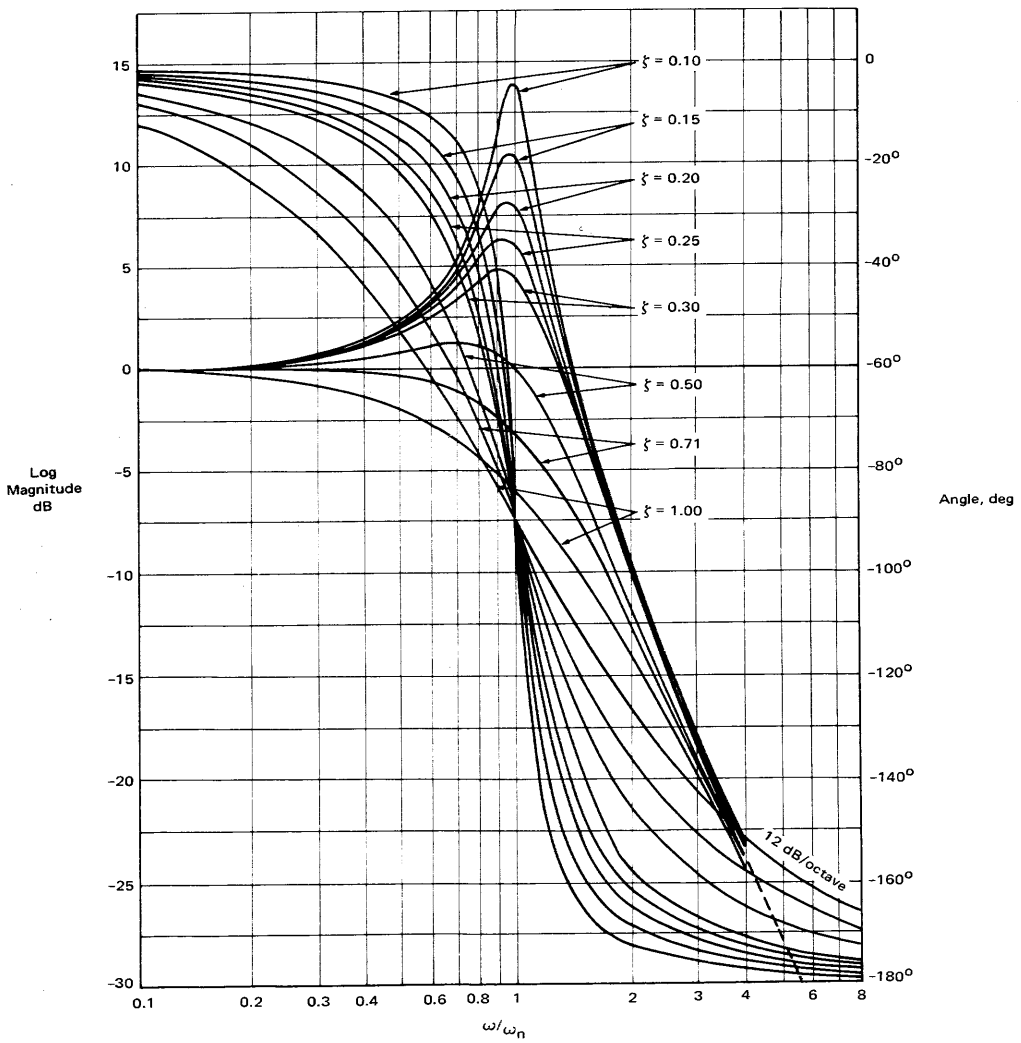


FIGURE 3 – Normalized Log Magnitude and Phase of $\left[1 + j\omega \frac{2\zeta}{\omega_n} + \frac{1}{\omega_n^2}(j\omega)^2\right]^{-1}$

TABLE A

ZETA(ζ)	P dB PEAKING
0.01	33.9803
0.02	27.9609
0.03	24.4412
0.04	21.9454
0.05	20.0111
0.06	18.4323
0.07	17.099
0.08	15.9457
0.09	14.9301
0.1	14.0232
0.15	10.5565
0.2	8.13619
0.3	4.84662
0.4	2.69544
0.5	1.2494
0.6	0.35458
0.7	0.00173

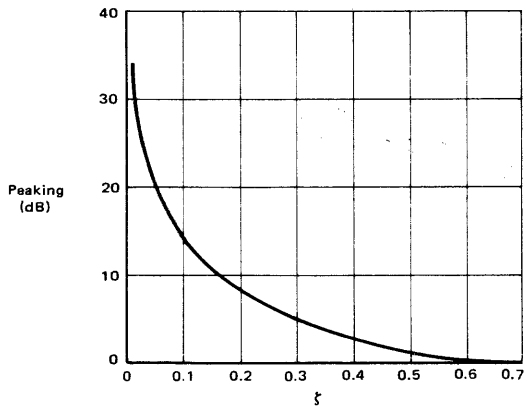


FIGURE 4 – Peaking (dB) as a Function of ζ

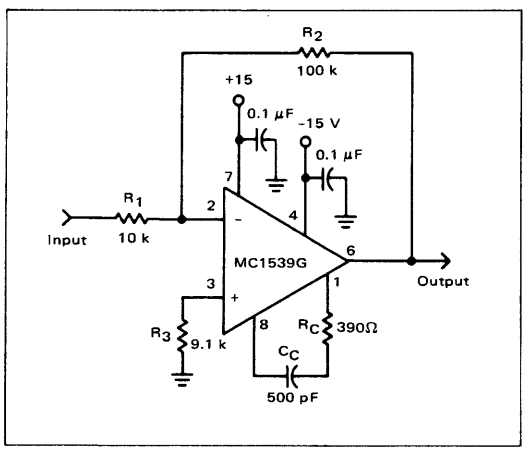


FIGURE 5 – Amplifier Example

The next section will consider the analysis of the second order or two pole system when a step function is applied to its input.

Referring again to Equation (14), by neglecting A_{VCL} as a scale factor, the response is left in a normalized form. The characteristics of this function are treated extensively in the literature. Figure 3 shows both a magnitude and phase plot versus $\frac{\omega}{\omega_n}$ for selected values of ζ.

The log magnitude plot of Figure 3 represents precisely the frequency response of the amplifier configuration. Therefore by knowing ζ it is possible to calculate the magnitude of peaking that can be expected. This can be done accurately by setting the derivative of Equation (14) to zero and solving. This leads us to the following result:

$$P\,(\text{dB peaking}) = 20\log_{10}\left[\frac{1}{2\zeta\sqrt{1-\zeta^2}}\right] \quad \zeta < 0.707 \quad (18)$$

where P is the increase in gain (in dB) because of peaking.

Table A lists "dB of peaking" versus ζ for selected values of ζ while Figure 4 is a plot of Equation (18) which shows graphically the effect of ζ on peaking.

PRACTICAL APPLICATION

The amplifier under test should conform as closely as possible to the actual operating conditions.

The input pulse may be simulated with the use of a square wave generator that has rise and fall times on the order of 100 nanoseconds. An alternative source would be a pulse generator but it must be capable of pulse widths on the order of 100 microseconds. Both the square wave generator and pulse generator should be capable of frequencies below 5 kHz. These last two restrictions may be required to insure that the response has sufficient time to reach a steady state before the next pulse appears. The input amplitude should be small enough to preclude the effects of slew rate limiting or saturation of the amplifier.

The key to accurate measurement lies in the display of the output response on the oscilloscope. To achieve maximum accuracy, the response waveform should be displayed so that it occupies as much of the area of the oscilloscope face as possible. The graticule is then scaled with the initial value of the waveform at zero and the final value at one. The horizontal scale should be adjusted so that the three peaks required for determination of ζ are visible.

The values obtained from this display are then substituted into the equations to determine ζ and ω_n.

Referring to Figure 3, the log magnitude curve for the calculated ζ is traced to where it crosses the 0 dB line on the modified vertical scale. The abscissa value of this point is $\frac{\omega}{\omega_n}$ and by knowing ω_n from the output response, ω represents the small signal unity gain bandwidth. The intersection of this line with the proper ζ-valued phase shift plot yields the phase shift at 0 dB. The difference between this value and 180^o represents the phase margin.

EXAMPLE

The example to be considered is an amplifier with a closed loop gain of 10. The particular operational amplifier used is the MC1539. Although the recommended compensation is R_C = 390 ohms and C_C = 2200 pF, 500 pF was used for C_C. The amplifier configuration is shown in Figure 5. The pulse generator is terminated in its matching impedance, R_T, to obtain quality pulses. The pulse width and frequency controls are adjusted to allow sufficient settling time for the amplifier to reach quiescent values.

RESULTS

The pulse response is shown in Figure 6. The following values were interpreted from it:

$$V_{P1} = 1.867$$
$$V_{P2} = 0.366$$
$$V_{P3} = 1.534$$
$$t_1 = 1.16\,\mu s$$
$$t_3 = 3.48\,\mu s$$

Substitution of these values into Equations (12) and (13) respectively yields:

$$\zeta = 0.029$$
$$\omega_n = 2.71 \times 10^6 \text{ radians}$$
$$f_n = 431 \text{ kHz}$$

A frequency response was run on the configuration to verify the results of the pulse response. Figure 7 shows this response and indicates 20 dB of peaking at a frequency of 425 kHz.

For the above calculated value of ζ, and using Table A, approximately 24 dB of peaking would be expected. Thus, the theoretical analysis and actual results agree quite closely.

SUMMARY

This application note has shown how the stability of a second-order system, in this case, a feedback amplifier, can be evaluated using simple measurements. This frees the designer to optimize his design within a relatively short time. Although the example presented a case of non-standard compensation, the technique is applicable to evaluating the effects of other parameters that can lead to instability such as capacitive loading at the output.

REFERENCE

1. D'Azzo, J. and C. Houpis, Feedback Control Systems Analysis and Synthesis, Second Edition, McGraw-Hill Book Company, 1966.

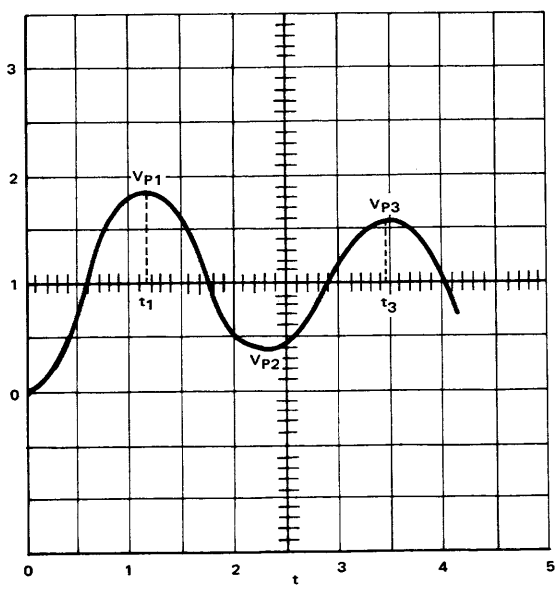


FIGURE 6 – Pulse Response

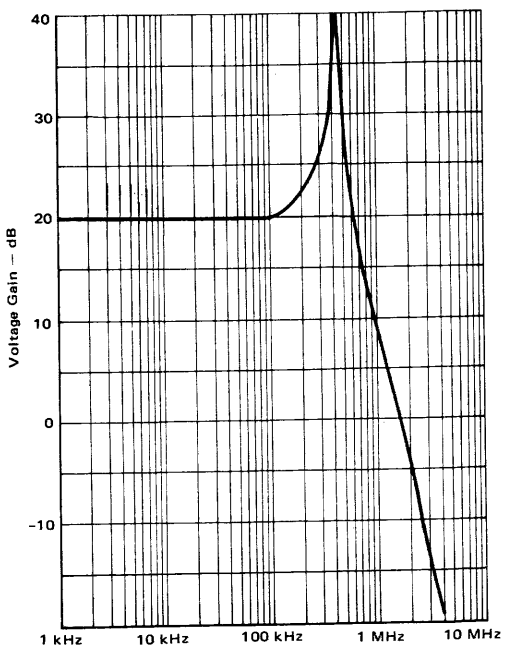


FIGURE 7 – Frequency Response

APPENDIX

THEORETICAL DERIVATION

The differential equation used to describe a second order system is as follows:

$$\frac{d^2x}{dt^2} + a\frac{dx}{dt} + bx = c. \quad \text{(A1)}$$

The basic solution for x requires that x be of the form

$$x(t) = ke^{mt}. \quad \text{(A2)}$$

Substituting into Equation (A1) yields

$$m^2 ke^{mt} + amke^{mt} + bke^{mt} = c. \quad \text{(A3)}$$

Since the system is linear, one solution can be obtained by setting c equal to zero thus making the solution independent of the input. This is known as the characteristic equation:

$$m^2 ke^{mt} + amke^{mt} + bke^{mt} = 0. \quad \text{(A4)}$$

Since e^{mt} cannot be zero for all time it can be factored out leaving

$$m^2 k + am\,k + bk = 0. \quad \text{(A5)}$$

This can be written in terms of new constants as:

$$a\,m^2 + \beta m + \delta = 0. \quad \text{(A6)}$$

This is a quadratic equation in m whose roots are:

$$m_1, m_2 = \frac{-\beta \pm \sqrt{\beta^2 - 4a\delta}}{2a}. \quad \text{(A7)}$$

Since the quantity under the radical sign can be negative, Equation (A7) can be rewritten in terms of general complex solutions,

$$m_1 = \sigma + j\omega_d \quad \text{(A8a)}$$

$$m_2 = \sigma - j\omega_d \quad \text{(A8b)}$$

where $j = \sqrt{-1}$.

Substituting Equations (A8a) and (A8b) into Equation (A2) and adding yields

$$x(t) = k_1 e^{(\sigma + j\omega_d)t} + k_2 e^{(\sigma - j\omega_d)t}. \quad \text{(A9)}$$

Using Euler's expansion: $e^{\pm j\omega_d t} = \cos\omega_d t \pm j \sin\omega_d t$ and factoring out $e^{\sigma t}$, Equation (A9) can be written:

$$x(t) = k_1 e^{\sigma t}(\cos\omega_d t + j\sin\omega_d t) + k_2 e^{\sigma t}(\cos\omega_d t - j\sin\omega_d t) \quad \text{(A10)}$$

Combining terms yields:

$$x(t) = e^{\sigma t}\,[(k_1 + k_2)\cos\omega_d t + j(k_1 - k_2)\sin\omega_d t]. \quad \text{(A11)}$$

Because this equation represents a real physical system, constraints are placed on k_1 and k_2 such that:

$k_1 + k_2$ = real number

$j(k_1 - k_2)$ = real number

Therefore let $k_1 = k_0 e^{j\theta}$ and $k_2 = k_0 e^{-j\theta}$.

Substituting these expressions into Equation (A9) gives:

$$x(t) = k_0 e^{j\theta}\left[e^{(\sigma + j\omega_d)t}\right] + k_0 e^{-j\theta}\left[e^{(\sigma - j\omega_d)}\right] \quad \text{(A12)}$$

Expanding this expression yields

$$x(t) = e^{\sigma t}\left[k_0 e^{j(\omega_d t + \theta)} + k_0 e^{-j(\omega_d t + \theta)}\right]. \quad \text{(A13)}$$

Knowing that:

$$\cos\beta = \frac{e^{j\beta} + e^{-j\beta}}{2}$$

$$x(t) = 2k_0 e^{\sigma t}\left[\cos(\omega_d t + \theta)\right]. \quad \text{(A14)}$$

Letting $\phi = \theta + \pi/2$, (A14) can be rewritten,

$$x(t) = 2k_0 e^{\sigma t}\left[\sin(\omega_d t + \phi)\right] \text{ or,}$$

$$x(t) = ke^{\sigma t}\left[\sin(\omega_d t + \phi)\right]. \quad \text{(A15)}$$

Returning for the moment to Equation (A7) and letting $\zeta = \frac{\beta}{2\sqrt{a\delta}}$ and $\omega_n = \sqrt{\frac{\delta}{a}}$

(A7) can then be rewritten as:

$$m_1, m_2 = -\zeta\omega_n \pm j\omega_n\sqrt{1 - \zeta^2}. \quad \text{(A16)}$$

Referring to Equation (A8a) and (A8b) then it can be seen that:

$$a = -\zeta\omega_n \quad \text{(A17a)}$$

and

$$\omega_d = \omega_n\sqrt{1 - \zeta^2}. \quad \text{(A17b)}$$

Substituting these into (A15) yields

$$x(t) = k e^{-\zeta \omega_n t} \left[\sin(\omega_n \sqrt{1-\zeta^2}\, t + \phi)\right]. \qquad \text{(A18)}$$

This equation defines a sine wave of frequency $\omega_d = \omega_n \sqrt{1-\zeta^2}$ and amplitude $A = k e^{-(\zeta \omega_n t)}$. Therefore ω_d is the damped frequency of oscillation, ζ is called the damping ratio and ω_n is the natural (or undamped) frequency of oscillation when the damping ratio ζ is equal to zero. Intuitively the exponent of e must be negative to insure that the oscillations eventually deteriorate. If the exponent is zero or positive the indication is that the oscillation will continue at some constant amplitude or will grow until limited by other system constraints.

Equation (A18) represents the transient response. The steady-state response can be added to it for a complete solution. The steady state output will be the product of the unit step-function input and the closed loop dc gain of the amplifier. Therefore the complete solution is given by

$$V_o(t) = V_{in} A_{VCL}\, u(t) + k e^{-(\zeta \omega_n t)} \left[\sin(\omega_n \sqrt{1-\zeta^2}\, t + \phi)\right] \qquad \text{(A19)}$$

where $u(t) = 0 \quad -\infty < t < 0$

$= 1 \quad 0 < t < \infty$.

The two constants k and ϕ need to be determined and can be from the initial conditions. At time $t = 0^+$ (just after V_{in})

$$V_o(t) = V_{in} A_{VCL} + k \sin\phi = 0. \qquad \text{(A20)}$$

This assumes the output of the system is at zero immediately after application of the step-function. This is because it was zero immediately prior to the step-function and due to capacitance of the system the output cannot change instantaneously. This constraint gives us a second equation to use in finding k and ϕ. That is,

$$\frac{d[V_o(t)]}{dt} = 0 \text{ at } t = 0. \qquad \text{(A21)}$$

Differentiating Equation (A19) yields:

$$\frac{d[V_o(t)]}{dt} = k e^{-(\zeta \omega_n t)} \cos(\omega_n \sqrt{1-\zeta^2}\, t + \phi)\, \omega_n \sqrt{1-\delta^2} + (-\zeta \omega_n)\, k e^{-(\zeta \omega_n t)} \sin(\omega_n \sqrt{1-\zeta^2}\, t + \phi). \qquad \text{(A22)}$$

Setting $t = 0$ and $\frac{d[V_o(t)]}{dt} = 0$:

$$0 = k(\cos\phi)\, \omega_n \sqrt{1-\zeta^2} - k\zeta\omega_n \sin\phi. \qquad \text{(A23)}$$

Equations (A20) and (A23) can be solved for k and ϕ:

$$\phi = \cos^{-1}\zeta \qquad \text{(A24)}$$

$$k = \frac{-V_{in} A_{VCL}}{\sqrt{1-\zeta^2}}. \qquad \text{(A25)}$$

so that (A19) becomes:

$$V_o(t) = V_{in} A_{VCL} - \frac{V_{in} A_{VCL}}{\sqrt{1-\zeta^2}} e^{-(\zeta \omega_n t)} \sin(\omega_n \sqrt{1-\zeta^2}\, t + \cos^{-1}\zeta) \quad \text{or}$$

$$V_o(t) = V_{in} A_{VCL} \left[1 - \frac{e^{-(\zeta \omega_n t)}}{\sqrt{1-\zeta^2}} \sin(\omega_n \sqrt{1-\zeta^2}\, t + \cos^{-1}\zeta)\right]. \qquad \text{(A26)}$$

The peak values of the oscillation can be determined by differentiating Equation (A26) and equating it to zero.

The derivative of (A26) reduces to

$$\sin(\omega_n \sqrt{1-\zeta^2}\, t).$$

This is equal to zero at

$$\omega_n \sqrt{1-\zeta^2}\, t = N\pi \quad N = 0, 1, 2, 3, \ldots .$$

Solving for t yields

$$t = \frac{N\pi}{\omega_n \sqrt{1-\zeta^2}}. \qquad \text{(A27)}$$

Substituting this value of t into Equation (A26) gives:

$$V_o(t) = V_{in} A_{VCL} \left[1 - (\cos N\pi)(e^{\frac{-\zeta N\pi}{\sqrt{1-\zeta^2}}})\right]. \qquad \text{(A28)}$$

Neglecting the scale factor $V_{in} A_{VCL}$ and evaluating for n = 1, 2, and 3,

$$V_o\left(\frac{\pi}{\omega_n \sqrt{1-\zeta^2}}\right) = 1 + e^{\frac{-\zeta\pi}{\sqrt{1-\zeta^2}}} = V_{P1},$$

$$V_o\left(\frac{2\pi}{\omega_n \sqrt{1-\zeta^2}}\right) = 1 - e^{\frac{-2\zeta\pi}{\sqrt{1-\zeta^2}}} = V_{P2},$$

$$V_o\left(\frac{3\pi}{\omega_n \sqrt{1-\zeta^2}}\right) = 1 + e^{\frac{-3\zeta\pi}{\sqrt{1-\zeta^2}}} = V_{P3}.$$

Therefore:

$$\frac{V_{P1}-V_{P3}}{V_{P2}} = \frac{1+e^{\frac{-\zeta\pi}{\sqrt{1-\zeta^2}}} - 1 - e^{\frac{-3\zeta\pi}{\sqrt{1-\zeta^2}}}}{1-e^{\frac{-2\zeta\pi}{\sqrt{1-\zeta^2}}}},$$

$$\frac{V_{P1}-V_{P3}}{V_{P2}} = e^{\frac{-\zeta\pi}{\sqrt{1-\zeta^2}}}\left[\frac{1-e^{\frac{-2\zeta\pi}{\sqrt{1-\zeta^2}}}}{1-e^{\frac{-2\zeta\pi}{\sqrt{1-\zeta^2}}}}\right] = e^{\frac{-\zeta\pi}{\sqrt{1-\zeta^2}}}$$

Taking the natural logarithm of both sides:

$$\log_e\left(\frac{V_{P1}-V_{P3}}{V_{P2}}\right) = \frac{-\zeta\pi}{\sqrt{1-\zeta^2}}$$

(Since $\log_e N = 2.3 \log_{10} N$)

$$\log_{10}\left(\frac{V_{P1}-V_{P3}}{V_{P2}}\right) = \frac{-\pi\zeta}{(2.3)\sqrt{1-\zeta^2}}$$

Or solving for ζ:

$$\zeta = \frac{\left|\log_{10}\left(\frac{V_{P1}-V_{P3}}{V_{P2}}\right)\right|}{\sqrt{\log^2_{10}\left(\frac{V_{P1}-V_{P3}}{V_{P2}}\right)+1.8615}}. \qquad (A29)$$

Where the peak values are normalized according to the vertical scale shown in Figure A1.

Knowing the value of ζ, Equation (A27) can be used to find ω_n by finding t at N = 1, the first peak, and at N = 3, the third peak.

Therefore

$$\omega_n = \frac{2\pi}{(t_3-t_1)\sqrt{1-\zeta^2}}, \qquad (A30)$$

where t_1 is the time to the first peak and t_3 is the time to the third peak as shown in Figure A1.

Thus the two parameters ζ and ω_n completely specify the response of a second order system.

The next part of this analysis concerns the application of this time domain solution to an analysis in the frequency domain. This is done so that the performance of the system can be evaluated in the parameters more meaningfully interpreted in stability analysis, bandwidth and phase margin.

Recalling the original Equation (7)

$$\frac{d^2x}{dt^2} + a\frac{dx}{dt} + bx = c. \qquad (7)$$

This can be rewritten taking the Laplace transform of both sides

$$s^2x + asx + bx = c. \qquad (A31)$$

Where it is understood that x is the output in response to the input c.

Equation (A31) becomes

$$\frac{x}{c} = \frac{1}{s^2+as+b}. \qquad (A32)$$

This represents the transfer function of the system. The system is unstable where $s^2 + as + b = 0$. This is precisely equivalent to Equation (A6). Therefore the roots of Equation (A6) as finally defined by Equation (A16) are also the roots of the denominator of the right hand side of Equation (A32). Since these have been determined, the function, $\frac{x}{c}$, of Equation (A32) can be evaluated by substituting in the roots and replacing s by $j\omega$.

$$(s^2+as+b) = (j\omega+\zeta\omega_n+j\omega_n\sqrt{1-\zeta^2})(j\omega+\zeta\omega_n-j\omega_n\sqrt{1-\zeta^2})$$

$$(s^2+as+b) = [(j\omega)^2+j\omega 2\zeta\omega_n+\zeta^2\omega^2+\omega_n^2(1-\zeta^2)]$$

$$(s^2+as+b) = (j\omega)^2+j\omega 2\zeta\omega_n+\omega_n^2$$

$$\frac{1}{s^2+as+b} = \frac{1}{\omega_n^2}\left[1+j\omega\frac{2\zeta}{\omega_n}+\frac{1}{\omega_n^2}(j\omega^2)\right]^{-1}. \qquad (A33)$$

Equation (A33) can be normalized to a gain of A_{VCL} at dc by multiplying it by $A_{VCL}\,\omega_n^2$ so the transfer function becomes:

$$A_{VCL}(\omega) = \frac{x}{c} = \frac{A_{VCL}(o)\,\omega_n^2}{s^2+as+b}$$

$$= \frac{A_{VCL}(o)}{\left[1+j\omega\frac{2\zeta}{\omega_n}+\frac{1}{\omega_n^2}(j\omega)^2\right]}.$$

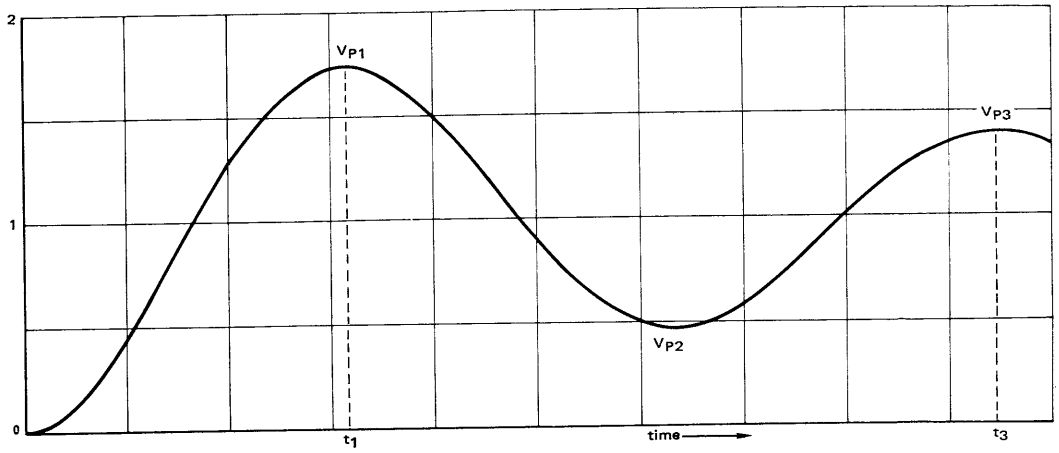


FIGURE A1 – Typical Second-Order Response

AN-467
USING HIGH THRESHOLD LOGIC

The introduction of integrated circuits has triggered an expansion in usage of electronic circuits. In the digital field, initial devices available consisted of families which generally exhibited reasonably fast operating times and operated from power supplies of 3 to 6 volts (e.g., resistor-transistor, diode-transistor, transistor-transistor and emitter-coupled logic families). The inherent advantages of integrated circuits made these families particularly attractive to the computer market and other similar fields. The industrial community, however, normally does not require high-speed operation; and it is more concerned with the electrical noise that is usually present in industrial environments. For these reasons, early digital integrated circuits did not possess the characteristics that would provide the maximum appeal to the industrial market.

Now, however, a new family of digital integrated circuits exhibits characteristics that are attractive to industrial and similar users. It is Motorola High Threshold Logic (MHTL) in the MC660 series. A summary of typical characteristics of this family are given in Table I.

This note describes members of the family, operating characteristics, and application information to help the designer to more fully utilize the logic family.

TABLE I – TYPICAL CHARACTERISTICS

V_{CC} = 15 ± 1 V
7.5-Volt Threshold
6.0-Volt Noise Margin
100 ns Propagation Delay
Fanout Capability of 10
-30°C to +75°C Operation

DEVICE OPERATION

The basic MHTL gate is shown in Figure 1A. It may be noted that this gate is very similar in configuration and operation to the Motorola Diode-Transistor Logic (MDTL) gate shown in Figure 1B. The basic difference is in diode D1, resistor values, and the collector supply voltage (V_{CC}). In MDTL, D1 is a base-emitter diode operated in its forward direction and having a drop of approximately 0.75 volt. The input threshold level of MDTL is seen to be a net of two forward diode drops (the input diode offsets a diode drop in the other direction) or about 1.5 volts. In MHTL, D1 is a base-emitter junction that is operated in its reverse direction; this is commonly called zener operation. Conduction occurs, in this case, when the junction has approximately 6.7 volts across it. Thus the threshold voltage for MHTL is one forward diode drop plus one reverse diode drop or about 7.5 volts. The normal supply voltage for this family is 15 volts ± 1 volt and in order to keep the power dissipation down, the gates have higher resistance values than comparable resistors in MDTL devices.

The MHTL gate provides the same positive-logic NAND function as the MDTL gate. It can be noted that if either of the A or B inputs is below the threshold level, possible base current to the transistor Q1 is routed to the low input. If both inputs are above the threshold level, Q1, D1 and output transistor Q2 all turn on and the output goes low. Thus the output is true or high if A or B is not true, i.e., $F = \overline{A \cdot B} = \overline{A} + \overline{B}$.

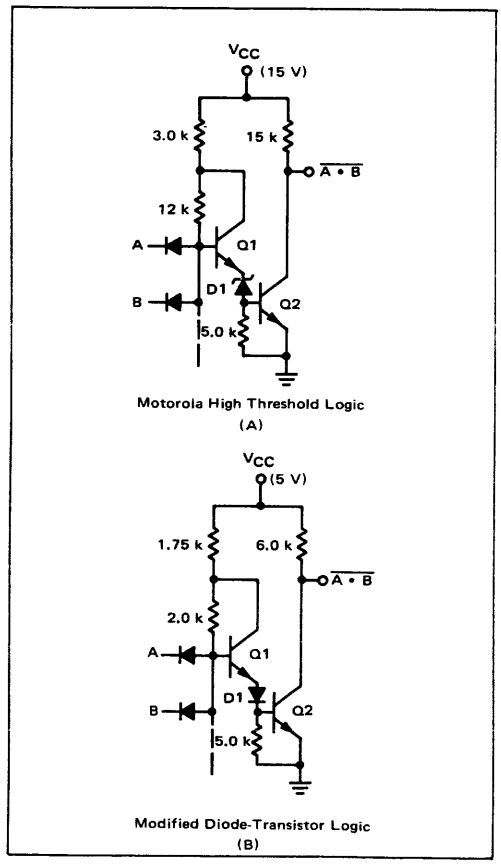


FIGURE 1 – Circuit Comparison Between the Input of High-Threshold Logic Gate (A) and Modified Diode-Transistor Logic Gate (B).

A typical MHTL transfer curve is shown in Figure 2. For normal input low voltages, less than 1.5 volts, it can be noted that the output exceeds V_{CC} minus 1.5 volts and will continue to do so for any input up to 6.5 volts, a tested point. A transition width is specified from 6.5 volts to 8.5 volts and once the input exceeds 8.5 volts, the output is guaranteed to be below 1.5 volts. This will remain true for any further increase in the input voltage. It can be noted that with a 15 volt supply, worst-case noise margin in either the high or low state is 5.0 volts. Normally, the low input voltage is 1 volt, the transition region is between 7 and 8 volts, and the high output voltage is better than 14 volts, thus typical noise margins of 6 volts are obtained in either state. As a comparison, the transfer region for other forms of integrated circuit logic generally lies within the unshaded area shown in the lower left-hand portion of the figure. From this it can be seen that MHTL could be considered as a "big brother" to other families of integrated circuits.

Although the basic gate was shown and is available with a nominal 15-kilohm pullup resistor, the devices are normally supplied with the active pullup configuration shown in Figure 3. In this circuit when Q2 is off, base current is supplied to Q3 from the 15-kilohm resistor and load current is effectively supplied through the 1.5-kilohm resistor. When Q2 is on, load current flows through D2 and Q2. Base current is also shunted from Q3 and this transistor is off in this state. The diode drop across D2 accounts for the somewhat higher low state voltage of MHTL as compared to other forms of logic families.

Each form of output has its advantages and disadvantages and the particular application would determine which device to use. The active pullup configuration has a lower output impedance in the high state and consequently will provide a higher degree of noise immunity from an energy point of view. This lower impedance can also better drive a load when in the high state, thus it is a superior interface for discrete components such as NPN transistors. The outputs of the functions with active pullup should not be connected together unless all inputs are also paralleled, to insure simultaneous operation of all devices. If one device were turned on while another device were off, the device in the low state would be required to sink current from the active pullup configuration of the high state unit. This will not damage the devices, but it leaves very little margin for providing load capacity to other devices.

The main advantage of the passive pullup configuration is its ability to have outputs of separate devices connected together. For each additional gate connected to the output of a gate, the original output loading factor of that gate must be reduced 1.25 because of the additional current that will be handled when a device is in the low state. When passive outputs are connected together, the impedance in the high state is reduced, and correspondingly the noise immunity from an energy standpoint is increased as compared to that for a single gate. The passive gate also normally has a lower V_{OL} than the active pullup configuration since only a $V_{CE(sat)}$ is involved although V_{OL} is still tested at 1.5 V with an I_{OL} of 12 mA.

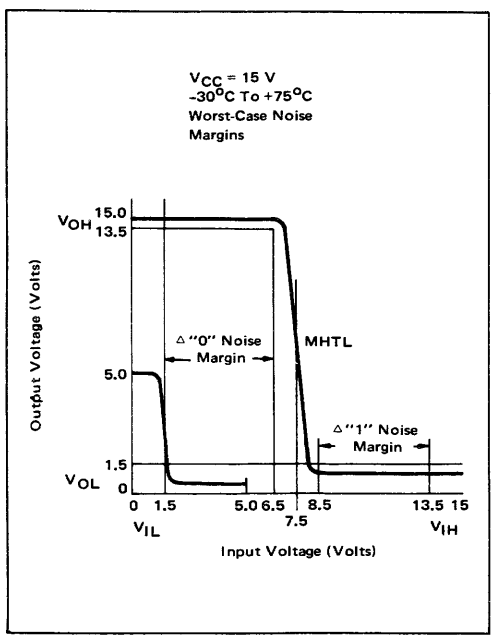


FIGURE 2 – High-Threshold Logic Transfer Curves.

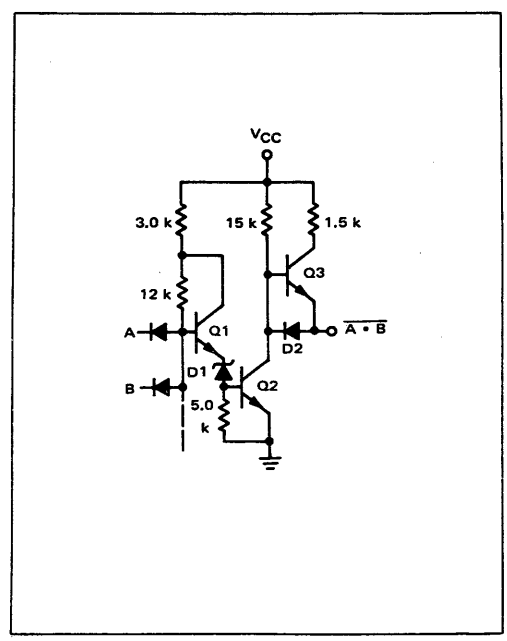


FIGURE 3 – MHTL Gate with Active Pullup

MHTL FAMILY

The MHTL family contains a sufficient variety of devices that the system designer can build complete systems with high-threshold characteristics. Gate devices providing the positive-logic NAND function are available as duals, triples and quads, as illustrated in Figure 4. Each basic configuration is available with active or passive pullup. Special logic functions are provided by the AND-OR-INVERT gates. For each gate, fanout capability is ten with a loading factor of one on each input. In addition, a dual, 4-input line driver (MC662) is available; it has a fanout capability of 30 loads while maintaining an input loading factor of one. This unit has a lower pullup impedance (1 kΩ) than the basic gate and is better suited for driving capacitive loads of discrete devices.

Two types of flip-flops are available in the MHTL family. The first is a dual J-K flip-flop that operates on a stored-charge principle and consequently is dependent on fast rise and fall times (less than 500 nanoseconds through the transition region of 6.5 to 8.5 volts) for proper operation. It is the MC663 shown in block form in Figure 5A. The second type (MC664, Figure 5B) is a single master-slave flip-flop which has a built-in diode offset between the master and slave sections. This feature makes transfer of data into the device virtually insensitive to clock rise and fall times. Both devices typically have maximum toggle frequencies of approximately 4 MHz. A detailed explanation of these two flip-flops is given in Motorola Application Note AN414, "Operation and Application of MHTL IC Flip-Flops."

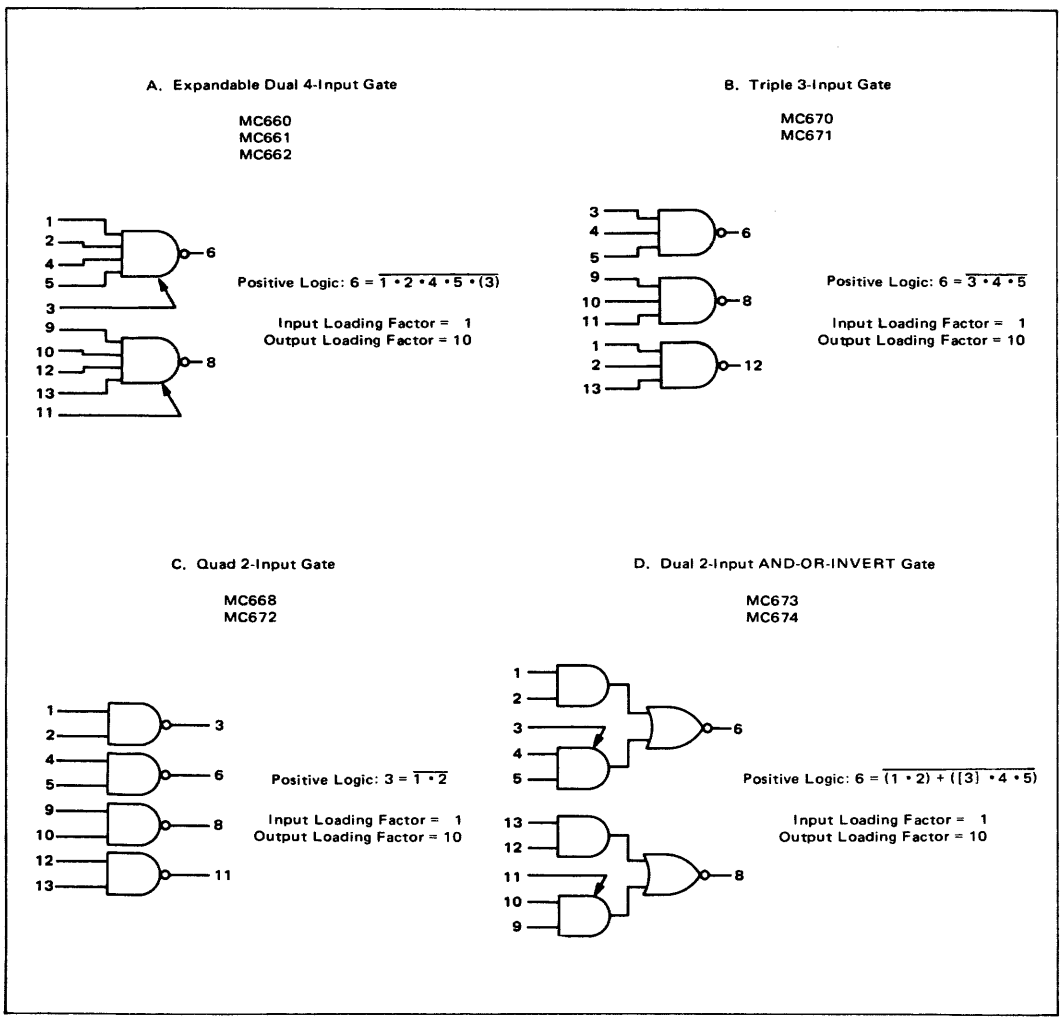
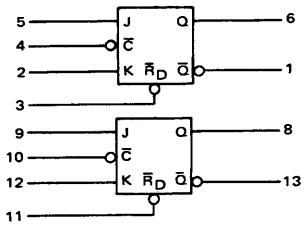


FIGURE 4 – Motorola High-Threshold Logic Gates

MC663



Truth Table

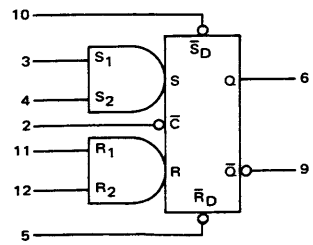
t_n		t_{n+1}	
J	K	Q	$\bar{Q}$
0	0	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
1	1	$\bar{Q}_n$	Q_n

Input Loading Factor:
$\bar{R}_D$ Input = 2
$\bar{C}$ Input = 1.5
Other Inputs = 1
Output Loading Factor = 9
Loading factors are valid from −30°C to +75°C with V_{CC} = 15 ± 1 Vdc
f_{Tog} = 4.0 MHz typ
Total Power Dissipation = 200 mW typ

Direct input ($\bar{R}_D$) must be high.
0 = low state
1 = high state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n
NOTE: A low state "0" at the direct reset $\bar{R}_D$ causes a low state "0" at the Q output and the complement at the $\bar{Q}$ output.

FIGURE 5A – MHTL J-K Flip-Flops.

MC664



Direct Input Operation

$\bar{R}_D$	$\bar{S}_D$	Q	$\bar{Q}$
1	1	NC	NC
1	0	0	1
0	0	NA	NA

NC = No Change
NA = Not allowed
$\bar{C}$ must be low

Clocked Operation

t_n				t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

Input Loading Factor:
$\bar{C}$ Input = 3
Other Inputs = 1
Output Loading Factor = 8
Loading factors are valid from −30°C to +75°C with V_{CC} = 15 ± 1 Vdc
f_{Tog} = 4.0 MHz typ
Total Power Dissipation = 160 mW typ

Notes for Clocked Operation Truth Table:

Direct inputs ($\bar{R}_D$, $\bar{S}_D$) must be high.
0 = low state
1 = high state
X = state of input does not affect state of the circuit
U = indeterminate state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

FIGURE 5B – MHTL Clocked R-S Master-Slave Flip-Flop.

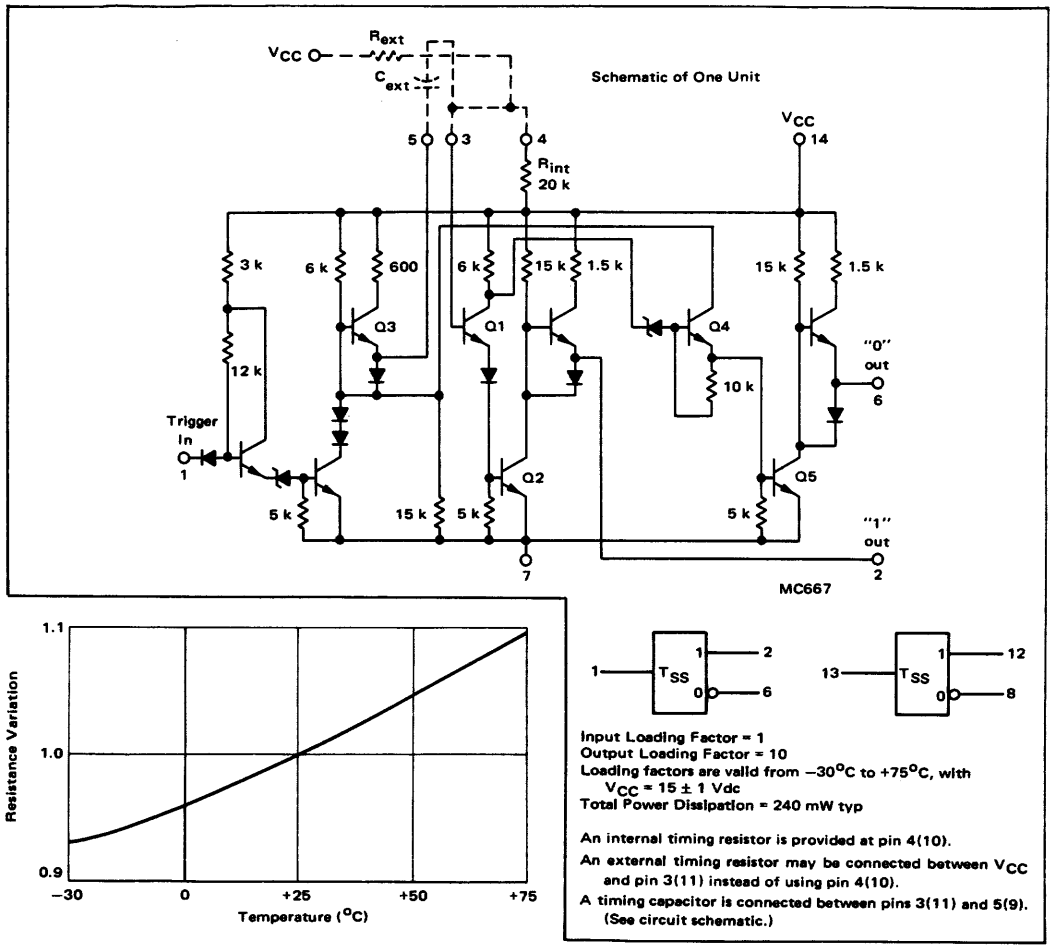


FIGURE 6B – Typical Resistance Variations with Temperature Change.

FIGURE 6A – Dual Monostable Multivibrator.

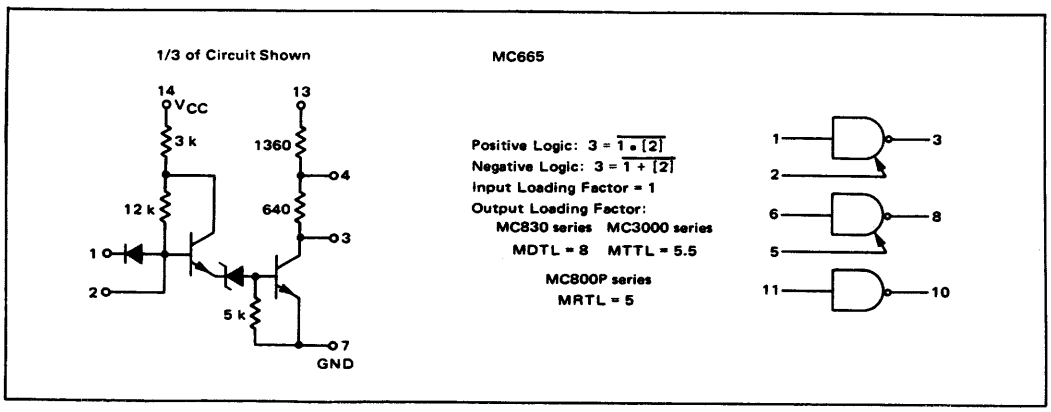


FIGURE 7 – Translator from MHTL to MRTL, MDTL or MTTL.

A dual monostable multivibrator (MC667) available in the family is illustrated in Figure 6. Each section provides both a positive-going and a negative-going pulse upon triggering by a positive-going signal that passes through the MHTL transition region of 6.5 to 8.5 volts. This is a direct-coupled circuit and will not be triggered by sharp noise pulses that do not exceed the threshold level. The width of the pulse may be adjusted with an external capacitor. The duration is approximately determined by the equation, $PW = 0.7\ R_T C_T$. An internal 20 kilohm resistor is provided for each multivibrator, but external resistors may be used for the timing function. The initial tolerances of the internal resistance may approach ± 20% with a typical temperature variation characteristic for the resistor as illustrated in Figure 6B.

Termination of the generated pulse occurs when the timing capacitor is discharged to the point where Q1 and Q2 conduct and the potential of pin three is clamped at three V_{BE} drops. However, because of this type of operation, the device is susceptible to negative noise spikes at the timing capacitor terminals. These spikes could cause Q1 and Q2 to turn off, triggering the device by turning on Q4 and Q5. Impedance at these points is kept down to approximately 600 ohms in the quiescent state by keeping Q3 on through the 15-kilohm resistor in the emitter circuit, thus aiding in noise rejection. Additionally a negative-going spike on the ground line may cause false triggering. Typical noise margins on these two leads exceed 1.5 volts. For these reasons, however, it is desirable to bypass the power supply and ground terminals at the device if noise is present on these leads and to shield the timing capacitor from noise if it exists at this point.

The design of this monostable multivibrator allows the generation of output pulses with widths virtually independent of trigger pulsewidths. However, the device does require a recovery time that begins at the end of the generated output pulse or when the trigger input returns to the "0" state, whichever is later. Allowable duty cycle may be determined from the equation, $\text{Duty cycle} = \frac{R_T \times 100}{R_T + 4.5}\%$ where R_T is in kilohms.

Two translators are available in the MHTL family and both are triple devices. The first (MC665) will convert high-threshold logic to RTL, DTL or TTL. It is shown in Figure 7. For conversion to DTL and TTL, a 5-volt supply is connected to a 2-kilohm pullup resistor through pin 13. For translation to RTL levels, pins 4, 9 and 12 are connected to the RTL supply voltage (nominally 3.6 volts). Output test conditions closely match those given for the popular Motorola MC800P series of MRTL devices and for the MC830 series of MDTL integrated circuits. Expander points without diodes are present at the inputs of two of the units, but not on the third unit. This is because of the need for additional leads for the RTL power supply and the pin limitation of the 14-lead package.

The second translator (MC666, Figure 8) is also a

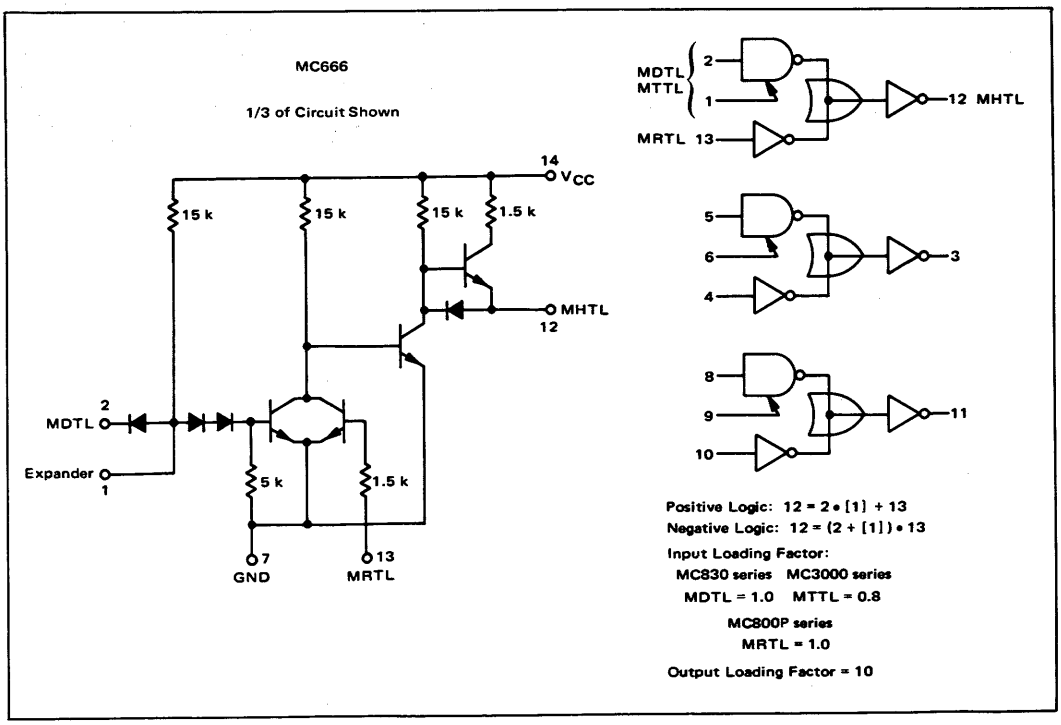


FIGURE 8 – Translator from MRTL, MDTL or MTTL to MHTL.

triple unit, but converts from DTL, TTL or RTL levels up to HTL levels. Signals from DTL/TTL sources are applied to one set of input terminals while signals from RTL sources are applied to another terminal. The different inputs provide threshold levels and characteristics compatible with MDTL/MTTL and MRTL families. Each DTL/TTL section also has an input expander terminal without diodes. These terminals may be used to expand input logic capability or to utilize high-voltage diodes to readily interface high-voltage relay or switch circuits to HTL levels. Both types of inputs may be applied simultaneously, with the output going high if the logic function of either input goes high. If the RTL input is used by itself, the DTL/TTL input must be grounded for proper operation. This is not necessary if the DTL/TTL input is being used by itself, but it is advisable under this condition to ground the RTL input to reduce any possible noise pickup.

A dual 4-input expander unit is also available in the MHTL family. It may be used to expand the input logic power of devices that have an expander node brought out for this purpose: the dual 4-input gates (MC660, 661), dual 2-input AND-OR-INVERT gates (MC673, 674), dual 4-input line driver (MC662) and the MC665 translator. The expander devices may also be connected directly to a normal diode input terminal. Operation in this manner reduces the threshold by a forward V_{BE} drop on those inputs associated with the expander units. Nominal threshold in this case is approximately 6.7 volts which is still adequate for normal operation.

The devices that have been listed in this section have been formally introduced. Expansion of the family, including complex functions, is continuing, thus providing a versatile logic family with high-noise-immunity throughout.

Propagation Delay Times

The MHTL family of devices exhibits a slower propagation time than that normally provided by other integrated circuit logic families. This is an additional aid in rejecting electrical noise because of the inability of the circuits to respond to narrow spikes of noise. Maximum propagation delays for each device are given on the appropriate data sheets. For these measurements, loading composed of a discrete RC network simulates full fanout for the device.

When actual devices are used as a load to measure propagation delay, a shoulder on the positive-going waveform may be observed at the threshold level as shown in Figure 9. This is caused by the decoupling of the actual gate loads from the driving gate. Since this point is very near the 50% level of the waveshape, a variation of approximately 50 nanoseconds may result in propagation time depending on whether the 50% point is above or below the threshold levels of the devices being used in the test. For this reason, discrete loads are used to insure repeatibility of the test conditions and yet provide an indication of the actual propagation delay.

Typical values of the propagation delays for the NAND gates with active pullup outputs are shown as a function of temperature in Figure 10.

Supply Voltage Variations

MHTL devices are tested to ensure proper operation with full fanout capability over the -30°C to +75°C temperature range and with supply voltages between 14 and 16 volts. Normally the devices will provide proper operation if the voltage varies from the specified range, but they are not tested for this operation. When the 16-volt limit is exceeded, devices may exhibit a higher leakage current on the off transistors, although typical units will endure 20 volts collector supply before this becomes evident.

Another drawback to using higher power supply values is the increased power dissipation of the circuits. Thus to keep junction temperatures within acceptable limits on

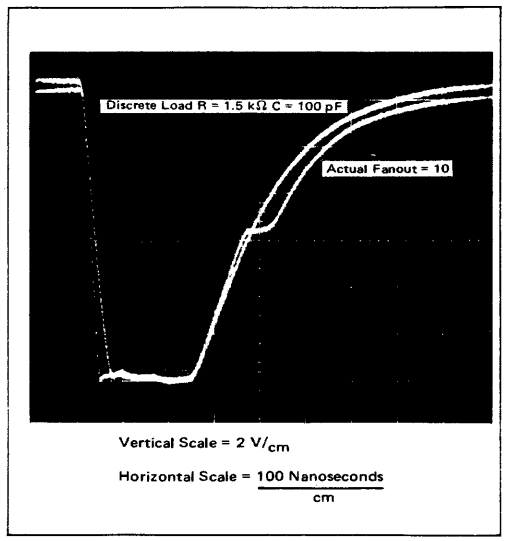


FIGURE 9 – Propagation Delay Waveforms

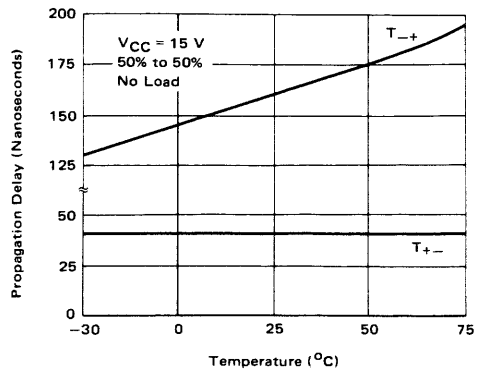


FIGURE 10 – Typical NAND-Gate Propagation Delay Times.

some devices, the ambient temperature limits must be reduced. Because of these two conditions, it is not advisable to exceed the 16-volt supply rating unless the devices have been tested to insure proper operation.

When a V_{CC} below 14 volts is used, the base drive to the output transistor is reduced and is not capable of handling the rated fanout. Figure 11 illustrates the V_{OL} values of typical units as a function of temperature with a V_{CC} of 14 volts and an I_{OL} of 12 mA. However, since the devices are not tested to operate below 14 volts, operation of the devices at these levels cannot be guaranteed. A second disadvantage of operating the units at a lower V_{CC} voltage is the reduction of the noise margin in the high state. This may be seen from Figure 2 by realizing that V_{OH} decreases while the device threshold remains constant.

LINE DRIVING

Applications exist where it is desirable to transmit data over an appreciable distance. The large logic swing of MHTL provides the means of transmitting data while minimizing the effects of noise. Unfortunately, most transmission lines have impedances below 150 ohms. The output impedance of MHTL devices is not an ideal match for these impedances, and consequently reflections may be observed on the transmission line waveforms. The line driver (MC662) has the lowest output impedance but it is still not down in the 150 ohm region. An improvement can be made in the impedance level by connecting an external resistor at the output of the line driver to V_{CC}. The additional current from a 510-ohm resistor can be handled by the MC662 when in the low state and is used to help charge the transmission line when going to the high state. Figure 12A illustrates a test set-up with 500 ft. of #22

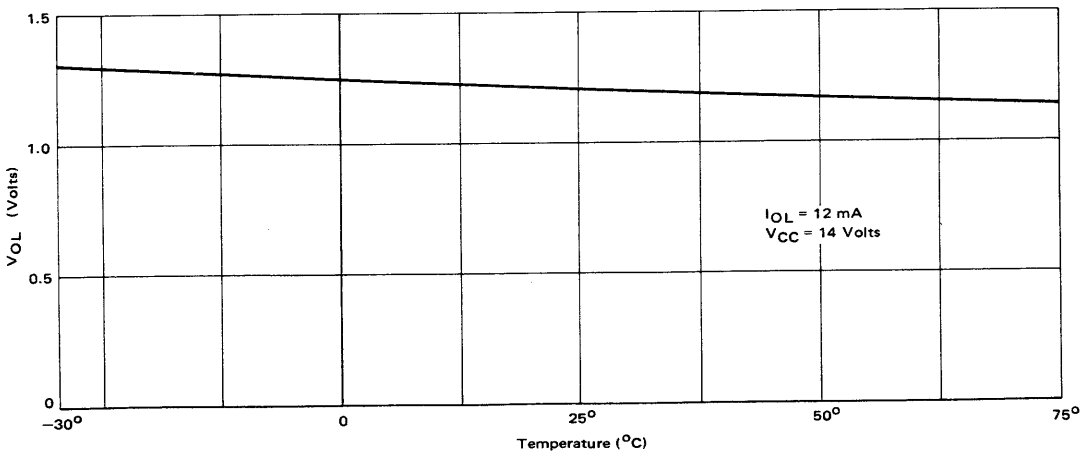


FIGURE 11 – Typical Variation in V_{OL} with Temperature.

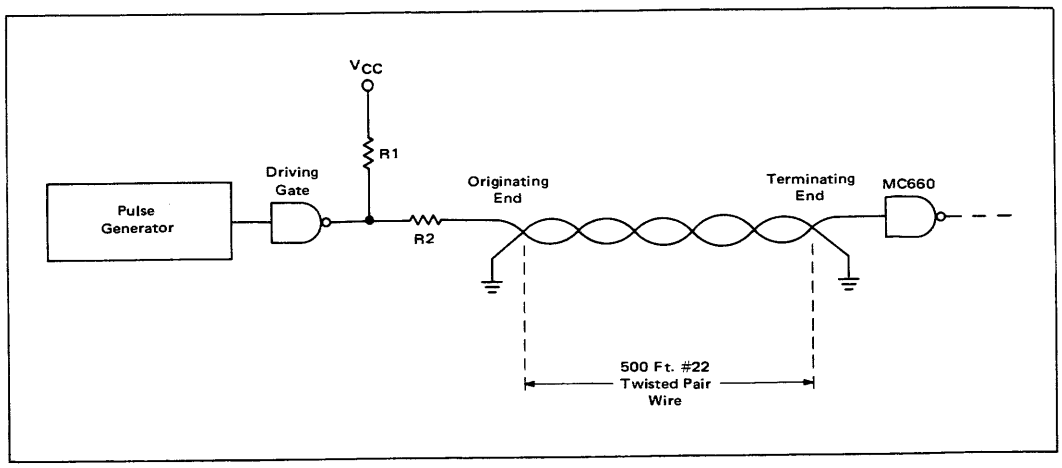


FIGURE 12A – Line-Driving Test Configuration

twisted-pair wire. Waveshapes of this connection are shown in Figures 12B, C, and D where the driving device is a standard gate output, a line-driver output, and a line driver with an external 510-ohm resistor to V_{CC} plus a 100-ohm series terminating resistor.

Special Gate Applications

Two MHTL gates may be connected with two additional resistors as shown in Figure 13A to form a Schmitt trigger. With the input originally low, gate one will be off, which turns gate two on and the output will be low. As the input rises, a point is reached where gate one turns on sufficiently to cause gate two to begin to turn off. Turn off of gate two feeds back to the input of gate one causing a regenerative action and a sharp waveshape at the output. The feedback through R2 and its action on R1 provides hysteresis for the circuit as well as sharp waveshapes. Typical values of turn-on and turn-off voltages are given in Figure 13B as a function of values of resistors R1 and R2.

In this connection, the active pullup devices should be used to minimize the effects of the feedback resistor and input voltage level when the output is in the high state. This configuration is ideal for receiving information transmitted over long lines as described previously.

Additional current sourcing may be obtained from the devices when in the high state by connecting an external resistor from the output to V_{CC} in the manner mentioned for driving transmission lines. The current from the extra resistor must be handled by the device when in the low state, which reduces fanout capability. The resistor used should not allow current to exceed the tested I_{OL} value to maintain V_{OL} values within their specified range. When using this scheme to drive an NPN device, however, an additional silicon diode is required in the base or emitter lead of the driven device to offset the normal V_{OL} value present for this type of operation.

Because of the typical V_{OL} level of 1 volt for the active

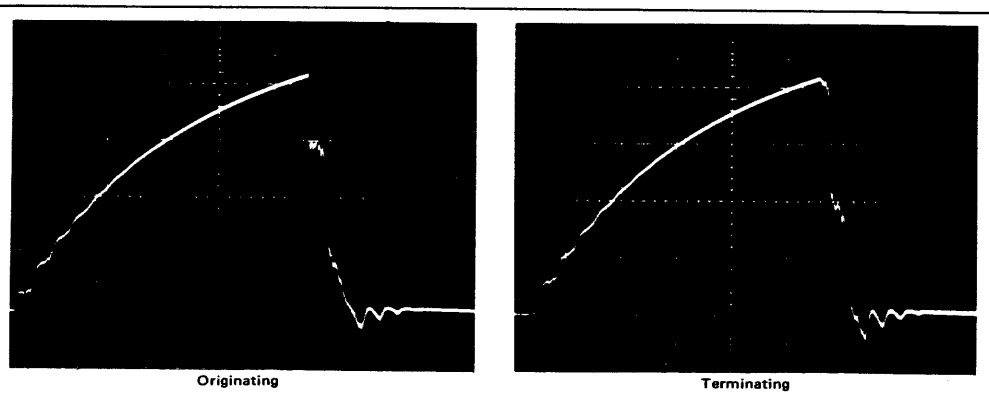


FIGURE 12B – Driving Gate – MC660 $R_1 = \infty$; $R_2 = 0$ Vert. –2 V/cm; Horiz – 5 μs/cm

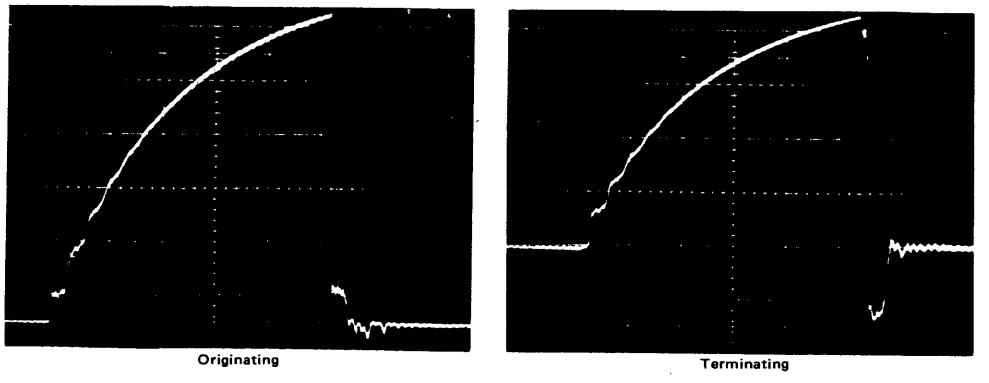


FIGURE 12C – Driving Gate – MC662 $R_1 = \infty$; $R_2 = 0$ Vert –2 V/cm; Horiz – 5 μs/cm

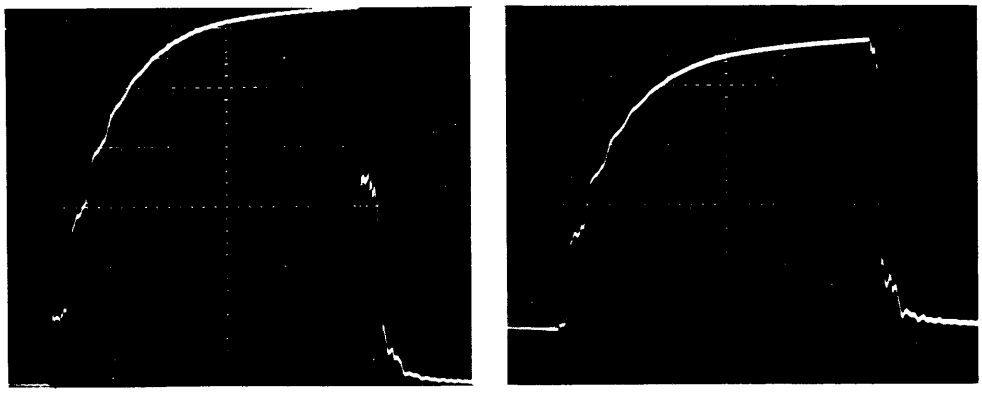


FIGURE 12D – Driving Gate – MC662 R_1 = 510 Ω; R_2 = 100 Ω Vert – 2 V/cm; Horiz – 5 μs/cm

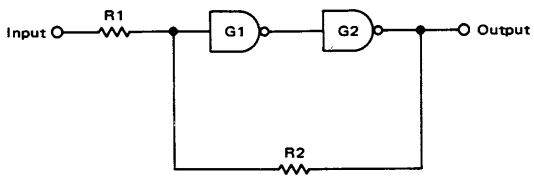


FIGURE 13A – Schmitt Trigger Connection

	R_1 = 1 kΩ		R_1 = 2 kΩ		R_1 = 5.1 kΩ	
R_2	V_{OFF}	V_{ON}	V_{OFF}	V_{ON}	V_{OFF}	V_{ON}
18 k	7.2	6.5	7.1	5.6	6.8	2.9
27 k	7.1	6.6	6.9	5.9	6.0	3.5
39 k	7.0	6.7	6.7	6.0	5.8	4.0
51 k	7.0	6.7	6.7	6.1	5.5	4.2
75 k	7.0	6.8	6.6	6.2	5.3	4.4
100 k	6.9	6.8	6.5	6.2	5.2	4.6

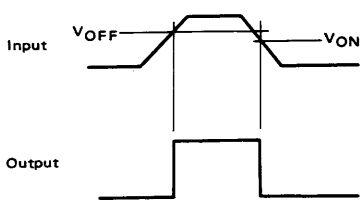


FIGURE 13B – Typical Schmitt Trigger Characteristics

pullup devices, they would not normally be considered suitable for driving NPN transistors directly because of the turn-off voltage. The active pullup devices can be used for driving NPN transistors, however, if that is the only load on the output, as shown in Figure 14. The higher V_{OL} voltage is partially due to the extra diode on the output, but if the gate is not required to sink current, then the voltage on the base of the NPN transistor will be very close to ground. It is equal to the resistance value of R1 times the leakage current of the collector-base junction of the transistor.

Cross connection of the gates as shown in Figure 15 forms a simple storage element. A momentary logic "0" on the S terminal causes the Q output to go high and the Q output to go low. A momentary low on the R terminal reverses the output state. Thus two flip-flops may be obtained from a single quad 2-input gate package.

SUMMARY

The Motorola High Threshold Logic family provides the system designer with devices that can be used to construct a complete system with noise immunity that is not available with the more familiar forms of integrated-circuit logic families. Operating from a nominal 15-volt power supply, which results in large logic swings, the family allows simple interfacing with discrete devices: MHTL devices can be used in peripheral equipment operating in noisy environments, with translators feeding into low-level, higher-speed systems in quieter locations. The unique characteristics of high-threshold logic make it ideal for many applications where integrated circuits have not previously been considered practical.

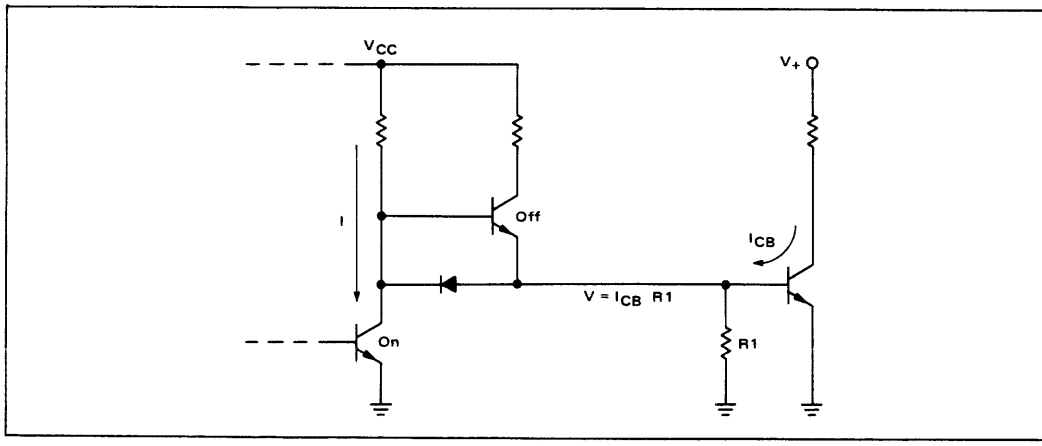
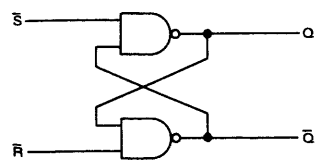


FIGURE 14 – Driving Discrete Transistors



Truth Table

S̄	R̄	Q
0	0	*
0	1	1
1	0	0
1	1	No Change

* This condition provides a high level on both outputs. The output state is indeterminable, however, if both inputs simultaneously go to a logic "1".

FIGURE 15 – Gate Memory Unit

AN-473
THE MC1561 — A MONOLITHIC HIGH-POWER SERIES VOLTAGE REGULATOR

INTRODUCTION

A complete monolithic high-power series voltage regulator circuit has been designed, which incorporates an on-chip power transistor to supply up to 1/2 ampere of current to an external load. Excellent regulation characteristics are achieved over an output voltage range of 2.5 to 37 volts, with performance being essentially independent of voltage. A new design approach is used, which results in excellent transient response and a low value of output impedance (0.02 ohm). This impedance is maintained to beyond 100 kHz, where the lead inductance to the load dominates. The use of special temperature compensation circuitry has provided a dc output voltage stability of ±20 ppm/°C, over the temperature range of -55°C to +125°C, despite the use of only diffused components. Load currents in excess of 10 ampere are possible by using a single external power transistor.

In the sections below, the series voltage regulator is analyzed using a feedback amplifier viewpoint, temperature compensation circuits are discussed, a novel lateral p-n-p biasing circuit is introduced, and experimental results are reported.

CONSTRAINTS OF THE IC TECHNOLOGY

The IC technology readily offers devices for the error amplifier and the voltage reference element V_R of the basic series voltage regulator shown in Figure 1. The series pass transistor appears to be the most difficult device to realize. A power p-n-p transistor may at first appear to be the best choice as it can be easily driven by an n-p-n stage without using auxiliary power supplies. However, the power p-n-p is difficult to realize in monolithic form.

An n-p-n series pass device requires a source of base current that must be derived from a voltage larger in magnitude than the output voltage. Auxiliary supplies can be avoided by using a current source that is operated directly from the unregulated input. A JFET operating at pinch off could be used but would add considerably to the IC fabrication costs and would require a large minimum biasing voltage ($V_{in}-V_O$). The lateral p-n-p transistor can be used for the required dc current source without degrading ac performance, increasing fabrication costs, or requiring an excessive input-output voltage differential. The preferred configuration for the monolithic series regulator is therefore one employing the n-p-n pass device with a lateral p-n-p current source supplying the base drive.

BASIC DESIGN APPROACH

In the conventional series regulator (Figure 1), a resistive divider is used to adjust the output voltage. Using this feedback network within the regulator loop has many undesirable effects on dc performance: 1) the loop transmission is an inverse function of the magnitude of the dc output voltage and because of this the performance of the regulator degrades at higher output voltages, and 2) the voltage drop due to the base current of the error amplifier (which is supplied through the divider network) is large enough that a carefully balanced symmetrical input circuit must be used. For low drift, h_{FE} and the base biasing resistors of the input transistors must match and this match must be maintained over a wide range of temperature. These base current problems limit the magnitude of the collector bias current that can be used, and this reduces the transconductance of the input differential amplifier. Also, for external adjustment of the feedback network (to achieve variable output voltages) either the temperature coefficient of the external feedback resistors (TCR) must match the TCR of the on-die diffused resistors, or all three dc factors, use of the resistive divider adds phase lag to the loop, which cannot be eliminated without the use of additional external capacitors.

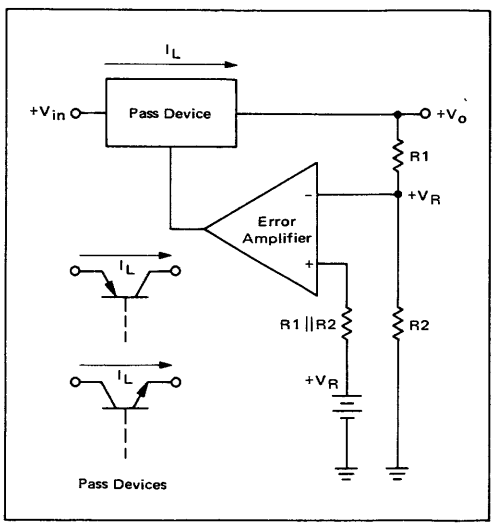


FIGURE 1 – Basic Series Voltage Regulator

Performance has been significantly improved by developing a configuration that operates with a unity feedback factor (i.e., no feedback resistance). The required dc level shifting to achieve a particular value of output voltage can then be provided in a circuit separate from the main regulator. Such an approach, in which a second low-power series regulator is used to provide the dc level shifting, is described in this paper. This "regulator-within-a-regulator" concept is shown in Figure 2 where the usual compromises made between ac and dc performance are no longer necessary.

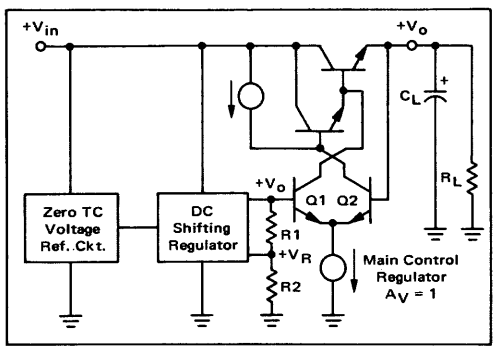


FIGURE 2 – Regulator Within a Regulator

CIRCUIT IMPLEMENTATION

Main Regulator

The dynamic performance of conventional voltage regulators is often limited by frequency compensation used internally to the error amplifier. Such compensation, which narrowbands this amplifier to obtain loop stability, causes the output impedance to rise at frequencies as low as 100 Hz. This also produces poor output voltage transient response for abrupt changes in load current and can cause undesirable coupling between circuits powered by the regulator. An improved regulator configuration results if no compensation is added to the loop, other than the capacitor (C_L of Figure 2) which is typically placed across the output terminals to maintain a low output impedance at high frequencies. It will be shown that compensation of this sort is possible, and that it results in: 1) an easily stabilized high-gain loop, and 2) an output impedance, which is essentially constant to frequencies well beyond the band edge of the loop transmission function.

Figure 3 is the ac equivalent circuit of the main control regulator shown in Figure 2. Using a feedback amplifier approach [1] and simple models for the transistors [2] we can identify the following relations for the frequency range of interest ($\omega < \omega_t/\beta_o$). The open-loop gain α_ν is given by

$$\alpha_\nu(S) = \frac{V_o}{V_s}(S) \cong \frac{\alpha_o}{(1 + S/\omega_p)} \qquad (1)$$

where

$$\alpha_o \cong \frac{\beta_o^2 R_L}{2r_e}; \qquad r_e = \frac{kT}{qI_E} \approx \frac{26\text{ mV}}{I_E} \text{ at } +25^oC$$

I_E = emitter current of Q1, Q2

β_o = low-frequency common-emitter current gain and the dominant pole is given by

$$\omega_p \cong \frac{1/R_a + 1/\beta_o^2 R_L}{C_a + C_L/\beta_o^2} \cong \frac{1}{R_L C_L}. \qquad (2)$$

The loop transmission becomes

$$T = \alpha_\nu f_\nu = \alpha_\nu \qquad (3)$$

for $f_\nu = 1$. α_ν is defined in (1) and the open-loop output impedance Z_{OL} is

$$Z_{OL} \cong R_L/(1 + S/\omega_p). \qquad (4)$$

The closed-loop output impedance Z_{CL} is then found to be

$$Z_{CL} = \frac{Z_{OL}}{1 + T} \cong 2r_e/\beta_o^2 \frac{1}{(1 + S/\alpha_o\omega_p)}. \qquad (5)$$

Two things are apparent from these equations. From (2) it is seen that at the low frequencies of interest in regulator design, a dominant single pole roll-off is produced by the load elements R_L and C_L, which results in good loop stability despite the use of high-loop gain. Second, it is seen from (5) that the open-loop dominant pole of T, ω_p, does not appear as a zero in the closed-loop impedance Z_{CL}. This results since the dominant pole of Z_{OL} is also ω_p, which cancels with the zero due to T. For conventional designs with a dominant pole in T only (those using frequency compensation internal to the main regulator), this cancellation does not occur and a low-frequency zero results in Z_{CL}, which degrades the performance of the regulator. Equation (5) shows that Z_{CL} remains small well beyond the low-frequency pole, ω_p, which was required for loop stability. As an example, for I_E = 0.6 mA,

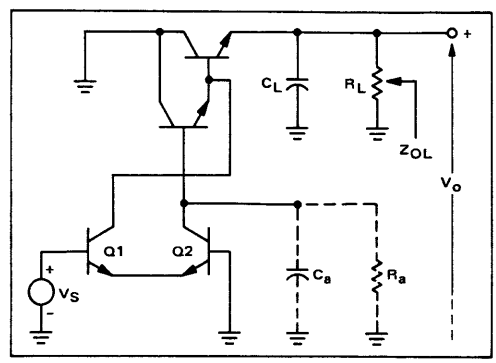


FIGURE 3 – AC Equivalent Circuit of Main Control Regulator. R_a and C_c Represent Stray Loading at the Collector of Q2

$\beta_O = 60$, $R_L = 20$ ohms, and $C_L = 10\ \mu F$; we find T = 840, $\omega_p/2\pi = 800$ Hz, and $Z_{CL} = 0.02$ ohm from dc to approximately 1 MHz.

The effects of the beta cut-off frequencies and additional phase shifts of the transistors will limit the maximum bandwidth that can be obtained in Z_{CL}. In practice, lead reactance in series with the load dominates the high-frequency response.

AC Reference Shifting Circuit

As shown in Figure 4, the auxiliary dc shifting regulator has been designed for essentially zero base current with little concern over the resulting loss in frequency response. Thus, the problem of drift arising from poorly controlled voltage drops due to base current in R4 and R2 || R1 is eliminated. In addition, the auxiliary regulator is purposely narrowbanded by an external capacitor C_N to attenuate the noise that originates in the avalanche (zener) reference diode. This noise roll-off is effectively set using a small valued capacitor since a high impedance node is available. A much larger capacitor is required in conventional regulators where one must bypass a low impedance zener diode.

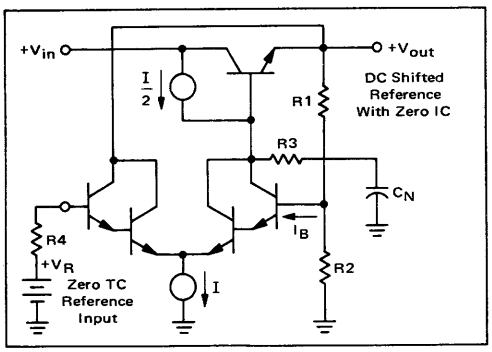


FIGURE 4 – DC Reference Shifting Circuit

Voltage and Current Reference Generation

It is well known that the excellent component matching available in IC fabrication permits realization of very low drift dc amplifiers. This low drift, combined with known drifts of an on-die voltage reference diode and other elements such as forward diodes, can be used to produce a reference voltage V_R, which is essentially constant, independent of temperature (zero TC). The voltage reference diode used is a reverse-biased base-emitter junction, which has a positive temperature coefficient (TC). This is balanced against the negative temperature coefficient of forward biased junctions. The circuit of Figure 5 provides a zero TC current reference for lateral p-n-p current sources and n-p-n current sources which are needed throughout the regulator. In the design of this circuit, a number n of base-emitter diodes (where $V_{BE} = \phi$) is assumed at the top end of the resistor string, and a number m of diodes is assumed at the lower end as shown. From Figure 5, it is seen that

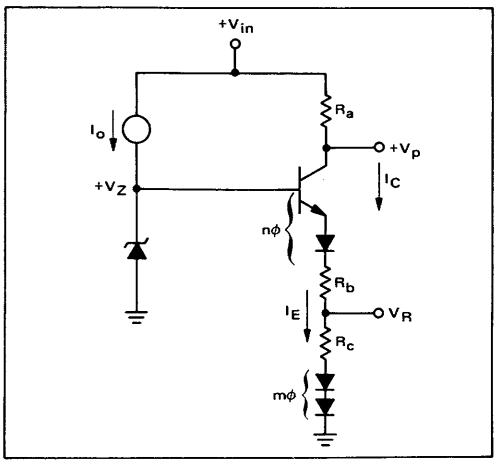


FIGURE 5 – Circuit to Generate the Zero TC Voltage Reference V_R

$$V_R = \frac{R_c V_z + \phi(mR_b - nR_c)}{R_b + R_c} \tag{6}$$

and

$$\frac{\partial V_R}{\partial T} = \frac{R_c \dfrac{\partial V_z}{\partial T} + (mR_b - nR_c)\dfrac{\partial \phi}{\partial T}}{(R_b + R_c)} \tag{7}$$

where the resistors R_b and R_c are assumed to have the same TCR.

For a zero TC voltage reference, it is required that

$$R_c \frac{\partial V_z}{\partial T} = -(mR_b - nR_c)\frac{\partial \phi}{\partial T} \tag{8}$$

or

$$\frac{R_b}{R_c} = \frac{n + K}{m} \tag{9}$$

where

$$K = -\frac{\partial V_z}{\partial T} \Big/ \frac{\partial \phi}{\partial T}.$$

The current, I_E flowing in these resistors is given by

$$I_E = \frac{V_z - p\phi}{R} \tag{10}$$

where $R = R_b + R_e$ and $p = n + m$, and the temperature change of this current is given by

$$\frac{\partial I_E}{\partial T} = \frac{-R\dfrac{\partial \phi}{\partial T}(K + p) - (V_z - p\phi)\dfrac{\partial R}{\partial T}}{R^2}. \tag{11}$$

Over the temperature range of interest, the temperature dependence of the diffused resistor is approximately given by:

$$R(T) \cong R_O + \alpha R_O(T - T_O) \qquad (12)$$

where $R_O = R(T_O)$, $T_O = +25^oC$, and α = temperature coefficient of resistance from which

$$\frac{\partial R}{\partial T} = \alpha R_O. \qquad (13)$$

Substituting (13) into (11) and solving for a constant current with temperature requires that

$$p = \frac{\alpha V_Z + K\dfrac{\partial \phi}{\partial T}}{\alpha \phi - \dfrac{\partial \phi}{\partial T}}. \qquad (14)$$

For a zero TC current reference, a total number of diodes p is required such that the positive change of the zener voltage and the diffused resistors is balanced by the negative change due to these diodes. As an example, the zener reference diodes used have a breakdown voltage of 7 volts and a TC of +3.5 mV/°C (K of (9) = 1.75). The TCR of the 200 Ω/□ diffused resistor gives a value of $\alpha = 1.9 \times 10^{-3}/^oC$ and the forward biased diodes have a temperature change of -2 mV/°C. Putting these values into (14) gives a value for p of 2.94, which is sufficiently close to the integer 3 to proceed with the design. As will be seen, the undesirable effects of the nonlinear TC of the diffused resistors [a linear TCR is assumed in (12)] are minimized by 1) choosing a value of R_b close to the value of R_c for the generation of V_R, and 2) using current source tracking in the differential amplifiers.

In addition to the zero TC requirements, the magnitude of V_R can be designed to have one of several values as given by

$$V_R = \frac{V_Z + K\phi}{1 + \left(\dfrac{n + K}{m}\right)}. \qquad (15)$$

The values of n = 1 and m = 2 (V_R = 3.46 volts) were chosen because this leads to the smaller ratio of R_b/R_c; which can be more accurately fabricated in IC form. With this choice, (9) gives

$$\frac{R_b}{R_c} = \frac{1 + K}{2} = 1.375$$

which completes the design for both a zero TC voltage reference V_R and the zero TC biasing current references I_E and I_C.

It is noted that use of this circuit causes the complete biasing of the regulator to be approximately independent of both the unregulated input voltage, the regulated output voltage, and the temperature.

Tracking Current Sources

To further improve the temperature stability of the output voltage, circuitry has been used to reduce temperature induced voltage offsetting (V_{OS}) in the differential amplifier stages of the IC regulator. As shown in Figure 4, two current sources are associated with the biasing of each differential amplifier stage. If under temperature variation these currents change in an unrelated manner, the magnitude of $\pm V_{OS}$ would change and thereby introduce a temperature variation in the output voltage V_O. This is avoided by deriving both of these currents from the same compensated reference to insure tracking for all temperature.

Biasing the Lateral p-n-p Current Sources

The lateral p-n-p transistors are ideal for use as dc current sources since they can be designed for large output impedance and low output capacitance, but they suffer from batch to batch variation in h_{FE}. A bias scheme is needed that will operate the lateral p-n-p in the common base orientation (for high output impedance) and which will also provide a predictable current magnitude that is insensitive to h_{FE} variations. The circuit shown in Figure 6 satisfies these requirements.[1] The reference voltage $+V_p$ (of Figure 5) is used to establish the total current flow in R_E. (For simplicity, it can be assumed that the V_{BE} drop of the n-p-n is cancelled by the V_{BE} rise of the p-n-p such

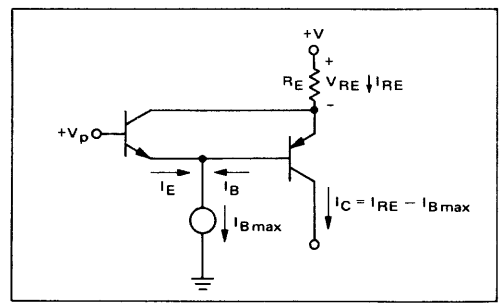


FIGURE 6 – Lateral p-n-p Current Source Biasing Circuit

that the voltage V_p appears at the lower end of R_E or $V_{RE} = V - V_p$). This current I_{RE} has two paths: the collector of the n-p-n or the emitter of the p-n-p. Neglecting the base current of the n-p-n, it can be seen that the current that enters the collector of the n-p-n reappears at the emitter and adds with the base current of the p-n-p, I_B, to satisfy the current source $I_{B\ max}$. Thus, the collector current of the p-n-p must simply be the difference between I_{RE} and $I_{B\ max}$, both of which are well controlled. In operation, the n-p-n is brought into that level

[1] This circuit was suggested by J. E. Thompson.

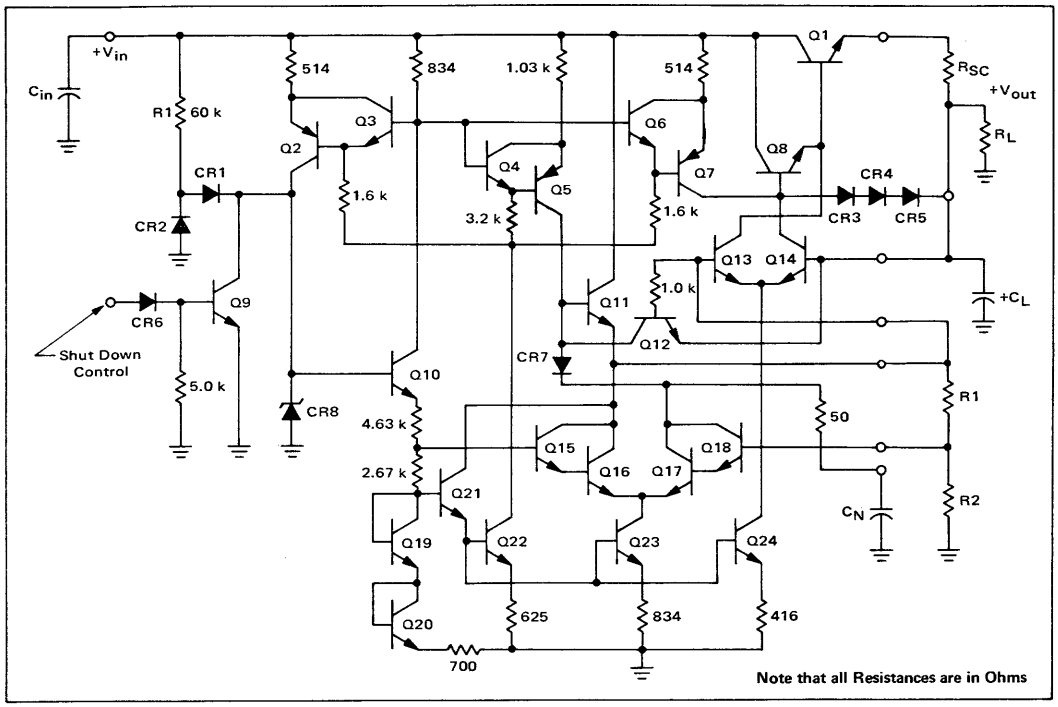


FIGURE 7 – Monolithic Series Voltage Regulator.

of conduction necessary to satisfy ($I_{B\ max} - I_B$) and in the limit, for low h_{FE} of the p-n-p, the n-p-n just ceases to conduct. Over the region in which h_{FE} of the p-n-p is greater than a minimum value, i.e., $I_C/I_{B\ max} < h_{FE} < \infty$, the collector current of the p-n-p is closely controlled.

THE COMPLETE CIRCUIT

The individual elements previously described are combined in Figure 7 to form the circuit implementation of the block diagram illustrated in Figure 2. In addition to the major elements already discussed, several secondary functions are included in the complete circuit. These are discussed below.

The bias current of the control amplifier Q13 is used to pre-bias the driver transistor of the series pass device Q8. This improves the h_{FE} and f_t of Q8, especially when operating with small values of load current.

Due to the necessary independence of the biasing currents from the input voltage, a "start" circuit must be used to allow the regulator to initially setup. To accomplish this function, a second zener reference diode, CR2 is biased by a large valued resistor R1 directly from $+V_{in}$. This auxiliary zener is coupled to the main reference zener CR8, using a diode-disconnect scheme. When an input voltage is first applied, a path is provided from $+V_{in}$ through the resistor R1, the coupling diode CR1, and into the base of the current reference transistor Q10. This guarantees the initial bias setup. With both zeners conducting, the coupling diode has zero volts across it, and therefore, goes to an OFF state. Thus, ripple and noise present at the start zener cannot feed through to the main zener and degrade performance.

Short circuit current is controlled by the external resistor R_{SC}, which brings three diodes into conduction at a selected maximum load current. These diodes are used to divert the available drive current for the Darlington series pass pair, Q8 and Q1. This passive scheme has the advantage that local frequency instabilities cannot occur during current limiting and provides a foldback in the current magnitude as the die heats under the higher dissipation short-circuit condition.

Under a short-circuit condition, the differential input voltage to the control amplifier may exceed the reverse base-emitter breakdown of the input transistors. Such breakdown is prevented by a normally OFF transistor Q12, which samples this voltage and is brought into conduction during an output short circuit condition. The collector of Q12 diverts the drive current of the dc level shifting amplifier so that the output reference voltage applied to the main control amplifier is also brought down to approximately zero volts under output short circuiting.

The capability of electronically shutting down the regulator to conserve system power or to provide an ac and dc squelch is desirable in some applications. This function has been accomplished by adding a normally OFF transistor Q9 in shunt with the reference zener. When this

device is brought into conduction, the zener goes OFF and the voltage at this node falls to essentially zero volts. This causes all current sources of the regulator to go OFF with the result that the output voltage goes to zero and the only current drain in the system is the small current that flows through the resistor R1 (60 kΩ). A high voltage diode CR7 in the level shifting amplifier is used to prevent the energy stored in the noise filter capacitor from discharging back into the IC during shutdown.

EFFICIENCY

A simple model of the regulator (Figure 8) can be used for the calculation of efficiency. In this model the current source I_B represents the current consumed by the regulator circuitry that is unavailable to the load R_L. The voltage source V_B represents the requirement for an input voltage somewhat in excess of the output voltage to provide the proper bias for the regulator. This voltage is, therefore, dropped across the regulator circuitry and is unavailable to the load.

The efficiency η is defined as

$$\eta = \frac{P_o}{P_{in}}$$

where

$$P_{in} = V_{in}(I_B + I_L)$$

or

$$\eta = \frac{1}{\left(1 + \frac{V_B}{V_o}\right)\left(1 + \frac{I_B}{I_L}\right)} \qquad (16)$$

Efficiency is seen to depend upon the comparison of the load current I_L to the bias current I_B, and also the comparison of the output voltage V_O to the bias voltage V_B (or "input-output voltage differential").

For an example, consider the regulator operating at a load current of 500 mA, and an output voltage of 35 volts (I_B is 5 mA and V_B = 2.5 volts). The maximum efficiency (for a dc input voltage) is found, from (16), to be 0.92. If the input voltage contains large ac components or large minimum-maximum variations η will be lower than 0.92 since P_{in} depends upon the average input voltage, which exceeds the required minimum total instantaneous input voltage (V_{IN} (min) = $V_O + V_B$).

SPECIAL DEVICES

A photomicrograph of the IC die is shown in Figure 9. Several devices on this die are of novel design. The high current n-p-n series pass transistor Q1 is a 5-stripe interdigitated structure with ballast resistors of approximately 1.5 ohms each used in the common emitter lead to each stripe. These resistors equalize current flow and thereby eliminate hot spot formation and second breakdown problems. In addition they provide a convenient crossover point to allow single layer metallization of the power transistor.

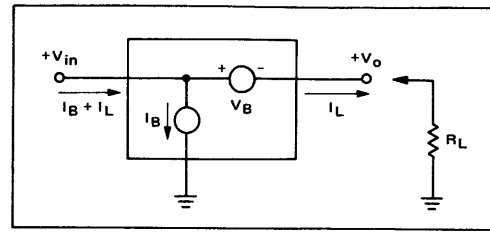


FIGURE 8 – Simplified Bias Model of Regulator

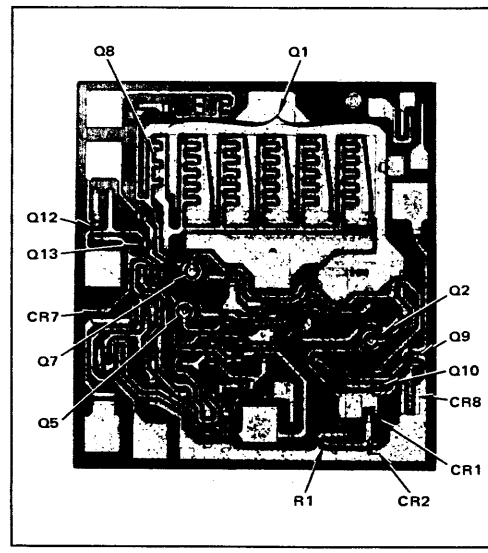


FIGURE 9 – Photomicrograph of IC Chip

Problems of building an avalanche (zener) diode with a low dynamic impedance at low bias currents were resolved by using an oval geometry for the active junction instead of the typical rectangular geometry. This eliminates corner breakdown and helps guarantee uniform breakdown of the complete junction. A small area device (5.6 mils by 7.4 mils), CR8, provides a dynamic impedance of 20 ohms.

The requirement for a high voltage diode with small current loss to the substrate (CR7 of Figure 7) has been solved by use of a lateral p-n-p structure with a base-collector short. The injected holes under forward bias are collected by transistor action and the usual current loss due to the substrate parasitic p-n-p transistor action is greatly reduced. Compared with the base-collector junction of a typical low-level buried-layer n-p-n transistor, the substrate current loss at 300 μA forward bias is reduced from 200 μA to 2 μA.

The use of lateral p-n-p structures for dc current sources is becoming common in IC designs. In this circuit, a circular geometry was used with a wide spacing from emitter to collector (0.6 mil) to increase the output impedance. This has provided an output impedance of 4 MΩ at I_C = 0.6 mA while maintaining a useful h_{FE} (8 to 16).

PERFORMANCE OF IC REGULATOR

Typical performance of the IC regulator is given in Table I. The close component matching and thermal tracking achieved in the IC realization, in combination with the added zero TC circuitry, has proven very effective in reducing dc output voltage changes with temperature. Many units have been measured which have an output temperature drift of only ±10 ppm/°C. The ability to achieve this performance depends primarily upon ability to control the temperature coefficient of the zener diode. This coefficient is a direct function of the magnitude of the breakdown voltage, with a change of ±0.2 volts, creating a total change in the temperature drift of ±20 ppm/°C. Present control of diffusion tolerance has provided units with an output voltage change less than ±30 ppm/°C.

TABLE I
TYPICAL PERFORMANCE

Temperature Drift of V_{out}	±30 ppm/°C
Z_o (Independent of V_{out})	0.020 ohms
Input Regulation	0.003%/V
Transient Recovery Time (I_{load} = 150 mA; ΔI_{load} = 50 mA	0.3 μs
Regulator Bias Current	5.0 mA
Maximum Load Current	600 mA
Output Noise (With C_N = 0.1 μF)	0.15 mVrms
Minimum Voltage Differential ($V_{in} - V_{out}$)	2.1 volts

The output impedance of 0.02 ohm is maintained essentially constant from dc to approximately 1 MHz as a result of using frequency compensation at the load only. A special printed circuit board layout with low inductance leads to the load is necessary to reduce the lead reactance contribution in the frequency range above 300 kHz. This technique is also needed to provide the optimum transient response in V_O for step changes in load current. Tests made with a constant load current of 150 mA and positive and negative step changes of 50 mA (with a rise and fall time of approximately 20 ns) have shown the peak overshoot to be 50 mV with a recovery time of less than 0.3 μs.

The maximum load current is established by current density limits of the standard-thickness (10,000 A) aluminum interconnect metal [3]. For wide temperature operation this current limit is approximately 500 mA, although the transistor structure used will carry currents of 1 ampere. Problems of short-circuit dissipation are created at these large current levels. A new 9-pin TO-66 package, which was designed for high-power integrated circuits, that allows a dissipation of 18 watts at T_{case} = +25°C (for a T_j = +150°C) is used.

SOME INTERESTING APPLICATIONS

The capacility of electronic shutdown can be used in many ways to extend the versatility of the basic unit. In addition to power savings and squelching, a novel application results from noting that the threshold voltage for this control is simply that of two base-emitter junctions. The ON voltage of these junctions is inversely dependent on chip temperature, so a fixed dc input voltage applied at the shutdown control produces automatic shutdown of the regulator at some desired maximum junction temperature. Thus, the unit can be completely protected regardless of heat sinking used or operating conditions chosen. Alternatively, by using a few external components, shutdown can be used to eliminate short-circuit dissipation, or a simple relaxation oscillator circuit can be added to cause a low duty cycle ON-OFF sequencing during short-circuiting to reduce dissipation, with normal operation automatically restored on the ON cycle following removal of the short.

A negative output voltage is possible and external n-p-n or p-n-p transistors can be added to boost both the load current capabilities and the high end of the output voltage range. Output over-voltage protection and the usual power supply features of remote sensing, complementary tracking, and output voltage programming can also be accomplished. Finally, a negative supply can be introduced at the normal ground point to provide a laboratory-type supply capable of achieving an adjustable output voltage with a minimum of zero volts.

CONCLUSIONS

Additional transistors made available in an IC realization have been used to provide improved regulator performance over that which can be economically achieved in discrete designs. The low drift dc capabilities of the IC technology are seen to give excellent temperature performance in an all-diffused circuit without the requirement for specially trimmed temperature independent resistors. The overall performance that has been achieved using a single die exceeds that required in most electronic systems and can be obtained at relatively low cost.

ACKNOWLEDGMENT

The author would like to acknowledge the contributions of J. E. Dunkley, who was responsible for the device designs; B. Backus, who designed the layout of the die; D. Alexander, who designed the 9-pin TO-66 power package; and J. E. Solomon, who offered many helpful suggestions in the preparation of the manuscript.

REFERENCES

[1] R. D. Thorton et al., Multistage Transistor Circuits, Semiconductor Electronics Education Committee, vol. 5. New York: Wiley, 1964, sect. 3.

[2] C. L. Searle et al., Elementary Circuit Properties of Transistors, Semiconductor Electronics Education Committee, vol. 3. New York: Wiley, 1964, sect. 3.

[3] J. Black, "Metallization Failures in Integrated Circuits," Semiconductor Division, Motorola, Inc., Phoenix, Ariz., Tech. Rept. No. RADC-TR-68, June 1968.

[4] Frederiksen, "A Monolithic High-Power Series Voltage Regulator," IEEE Journal of Solid State Circuits, Vol. SC3 #4, pp 380-7.

AN-475
USING THE MC1545, A MONOLITHIC GATED VIDEO AMPLIFIER

INTRODUCTION

The MC1545 is a monolithic integrated circuit that was designed for use as a wideband amplifier; however, because of its novel design, the MC1545 can be used in a variety of applications, that include a gated video switch, preamplifier for core memory sense amplifier, balanced modulator, frequency shift keyer for FSK systems, amplitude modulator, pulse amplifier, and multiplexing circuits, to name a few.

This application note will discuss briefly the dc and ac operation of the MC1545 and present some of its many applications.

I. CIRCUIT DESCRIPTION AND OPERATION

A schematic of the MC1545 with pin numbers for the TO-5 package (G suffix) is shown in Figure 1. The circuit consists of a constant current source transistor, Q7, and a switching differential amplifier, Q5 and Q6, which splits the constant current between two differential amplifiers, or channels, composed of transistor pairs Q1 – Q2 and Q3 – Q4 depending on the voltage applied at pin 1, the gating pin. The collectors of both channels are tied together and connected to a common load resistor (1 kΩ). By using this technique, the amount of current flowing through each of the 1 kΩ load resistors is constant and independent of which channel, Q1 – Q2 or Q3 – Q4, is conducting. As a result, there is essentially no dc level shift at the output when one channel is turned off and the other channel is turned on. The steady-state change measured in the differential output voltage when switching from one channel to the other is typically 15 mV. The amplified signal which appears at the collectors of the input channels is transferred to the output via Darlington emitter followers for a low output impedance and at the same time buffer the input differential amplifiers from any capacitive loading which would tend to lessen the frequency response.

Common mode feedback is provided from the emitter of the first emitter follower back to constant current source, Q7, to stabilize the dc operating point of the circuit

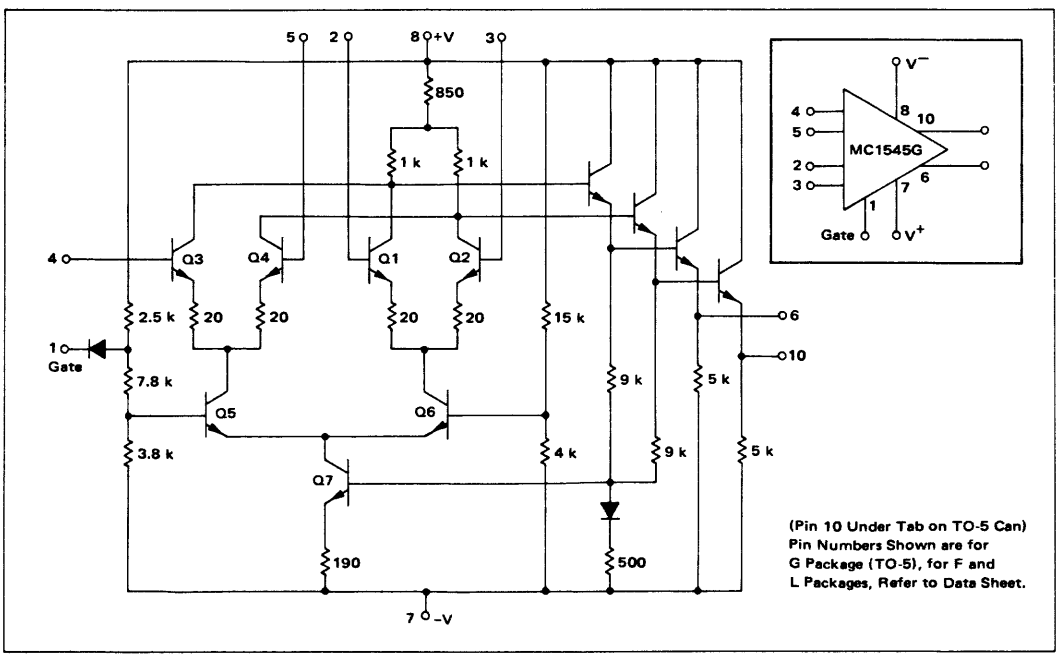


FIGURE 1 – MC1545G Circuit Schematic

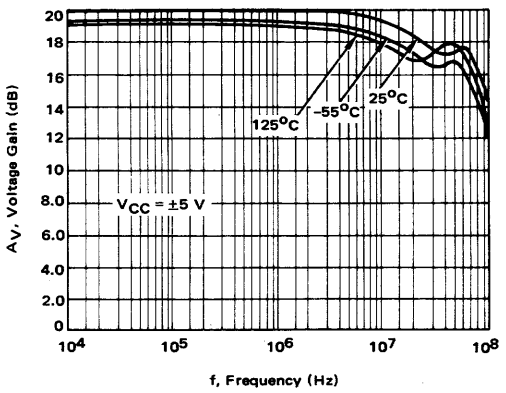


FIGURE 2 – Single Ended Voltage Gain versus Frequency

and provide excellent common mode rejection.

The manner by which either of the two input channels can be selected is as follows: The biasing of the MC1545 is such that with a sufficiently positive voltage applied to the gating pin (pin 1 on the "G" package), or with the gating pin left open, the voltage at the base of transistor Q6 is more negative than the voltage at the base of transistor Q5. As a result, transistor Q5 is "on" and transistor Q6 is "off". Under this condition, all of the constant current which is established in the collector of Q7 passes through transistor Q5 and establishes a bias current in the differential amplifier composed of Q3 and Q4. Hence, any signal applied to these transistors is amplified and will appear differentially at the output. However, if the gating pin is connected to ground or some negative value, the voltage at the base of transistor Q5 becomes more negative than the voltage at the base of Q6, which causes the constant current to flow through Q6 and establish the bias current in the differential amplifier composed of transistors Q1 and Q2. In this state, any signal which is applied to transistors Q1 and Q2 is amplified and will appear at the output, while the signal that is applied to transistors Q3 and Q4 is now gated off. The voltage required to perform this gating function at pin 1 is compatible with all standard forms of saturated logic (MRTL, MDTL, TTL, etc.). In this manner either of two signals can be gated through the amplifier depending upon the application of a logic signal to the gating pin. This immediately points to the use of the MC1545 as a video matrix cross-point switch, a frequency shift keyer for FSK systems, a gated video amplifier, a gated oscillator, a preamplifier for core memory sensing, a channel selector for data acquisition, and many more. In addition to these obvious uses, there exist a number of less obvious uses which take advantage of the unique design and versatility of the MC1545. Among these is its use as an amplitude modulator and balanced modulator. These will be explained in more detail later in this application note.

Figure 2 shows a plot of voltage gain versus frequency for the three temperature extremes of -55°C, 25°C and 125°C. It is apparent from this plot that the MC1545 is a very wideband device and will serve well as a pulse amplifier. In addition to its wide bandwidth, the MC1545 has the added advantages of being dc coupled and providing a differential output from which a signal and its complement are available for driving logic functions which require both the signal and its complement as inputs. Rise time, fall time, and propagation delay are typically 6 ns for this device, making it compatible with modern, second generation logic systems.

As was explained earlier, the amount of attenuation which is given to an input signal when the amplifier is gated "OFF" is a function of the dc voltage at the gating pin. A curve showing this attenuation versus gate voltage is seen in Figure 3. As would be expected, the amount of attenuation of the input signal is a function of the input frequency. A curve of this characteristic is shown in Figure 4. This curve indicates that above 30 kHz, the amplifier begins to show a certain amount of capacitive feedthrough, primarily due to the physical closeness of the pins, and can be improved by the use of proper shielding between pins. However, even at an input frequency of 10 MHz, a channel separation of better than 60 dB can be achieved.

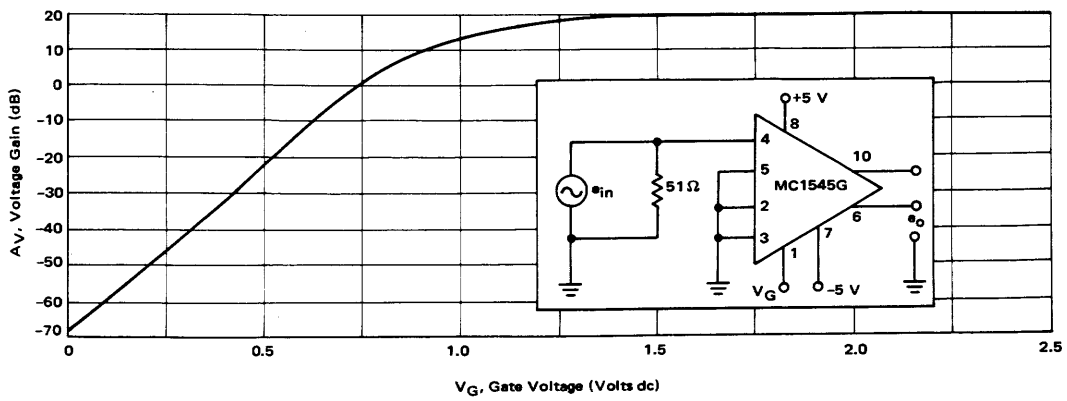


FIGURE 3 – Voltage Gain versus Gate Voltage

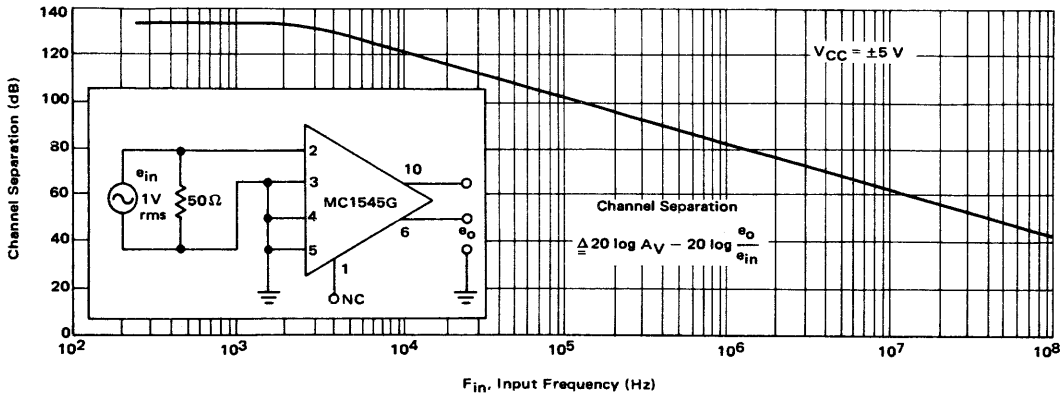


FIGURE 4 – Channel Separation versus Input Frequency

Another important parameter of any wideband amplifier is common mode rejection, which again is a definite function of frequency. This is shown in Figure 5 which demonstrates that the MC1545, even though very simple in concept, design and operation, has excellent common mode rejection.

To demonstrate the great versatility of this device, a number of applications will now be shown.

II. APPLICATIONS

A. Video Switch

Figure 6 shows the MC1545G connected as a gated analog switch. It should be pointed out here that the number of external components required for this application is very minimal. This particular usage requires only one resistor. In this application, a signal (analog or digital) is applied to the amplifier at pin 4. With the logic signal at pin 1 at a logic 1 state (positive voltage) the input signal is amplified and passed through the amplifier. However, if the logic signal at pin 1 is at a logic 0 state, the amplifier is turned off and no signal will pass through the device. If it were required that the opposite logic levels pass or block the signal, the input signal can just as easily be applied to pin 2 or 3 with pins 4 and 5 grounded. In this case, a high logic level would block transmission and a low logic level would pass the signal, making the use of inverters unnecessary. Taking "channel select time" as the time delay from the 50% point of the gate pulse to the 50% point of the full output swing, it is observed to be approximately 20 ns. During the time that the gating logic is in the low state, the circuit which gates the MC1545 must sink a maximum of 2.5 mA, which most forms of saturated logic can do easily. When the gating logic is in the high state, the circuit that gates the MC1545 must source only the leakage current of a reverse biased diode, which is 2 μA maximum. These requirements are quite similar to the input requirements of a standard DTL or TTL logic gate.

B. Frequency Shift Keyer

Rather than grounding pins 2 and 3 as in the previous example, it is possible to apply a second frequency to these input pins and select which of the two frequencies, either F1 or F2, will be passed through the amplifier. This is illustrated in Figure 7. As the circuit is shown, frequency F2 will be passed when the voltage at pin 1 is greater than +1.5 volt and F1 will be passed when the voltage at pin 1 is approximately zero volts.

The MC1545 can be used as a gated sense amplifier – preamplifier in core memory systems. By being able to strobe independent of the systems read signal, the sense amplifier can be gated on after the large common-mode pulse has passed and sense the low voltage differential signal stored in the core. This reduces the sense amplifier recovery time from microseconds to nanoseconds since the channel select propagation delay time is of the order of 20 ns.

In addition to this preamplifier application, another use can be made of this idea by paralleling and cascading a number of MC1545's to perform a one-of-N data selector for data processing. A simple example of this is shown graphically in Figure 8.

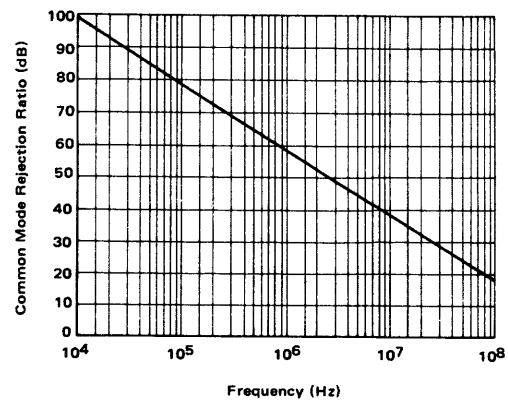


FIGURE 5 – Common Mode Rejection versus Frequency

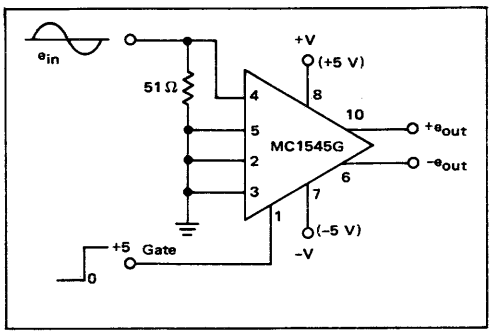


FIGURE 6 – Video Switch

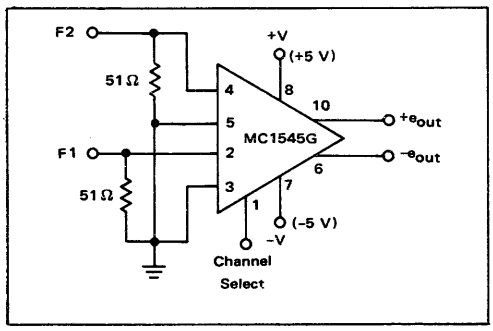


FIGURE 7 – Multiplexer (FSK)

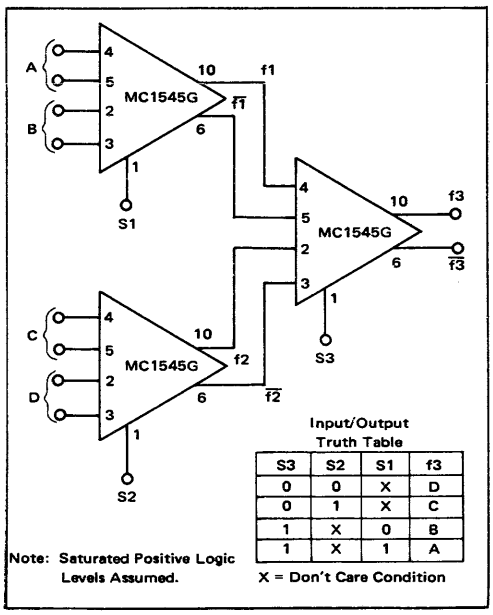


FIGURE 8 – One-Out-Of-Four Data Selector

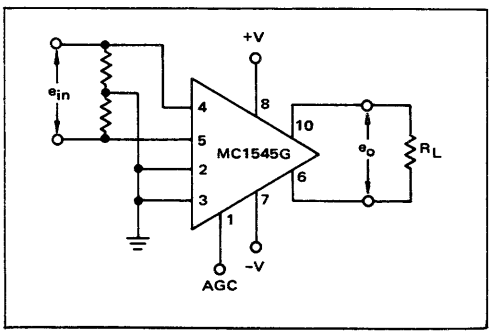


FIGURE 9 – Wideband Amplifier with AGC

C. Wideband Differential Amplifier with AGC

The gate characteristics of the MC1545, as shown in Figure 3, also make it useful as an AGC amplifier. With a dc voltage applied to the gate pin, as much as 100 dB of AGC can be obtained. Since there is essentially no dc level shift with AGC, the output waveform will collapse symmetrically about zero with little or no distortion. This application is shown in Figure 9.

D. Amplitude Modulator

The gate characteristics of the MC1545 also makes it useful as an amplitude modulator. Figure 10 shows the measured gate characteristics, with gain plotted on a linear scale. By biasing the gate at Point B and impressing an audio signal on the bias, the gain of the channel varies quite linearly between the points "A" and "C" on the curve, giving very little distortion on the output. Using the gate characteristics in Figure 10, the up-modulation (M_U) and down-modulation (M_D) may be calculated. Referring to Figure 11, the up and down modulation factors are defined as:

$$M_U = \frac{E_{max} - E}{E} \text{ (upward modulation)} \qquad (1)$$

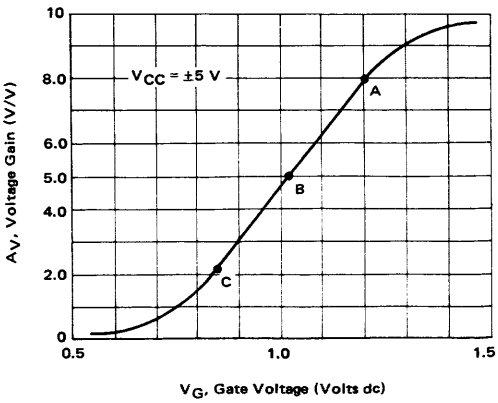


FIGURE 10 – Voltage Gain versus Gate Voltage

$$M_D = \frac{E - E_{min}}{E} \text{ (down modulation)} \qquad (2)$$

where:

E = peak amplitude of the unmodulated carrier

E_{max} = maximum amplitude attained by the modulated carrier envelope

E_{min} = minimum amplitude of the modulated carrier envelope

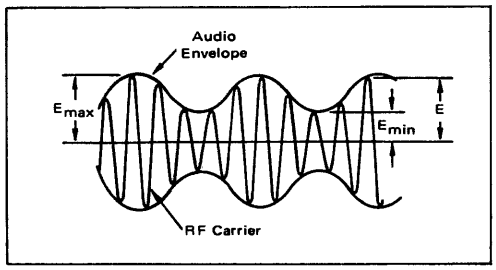


FIGURE 11 – Amplitude Modulated Waveform

Constraining the gate voltage to vary about the point "B" with a maximum occurring at point "A" and a minimum at point "C" and letting the RF carrier input be e_{in}, (See Figure 12), then

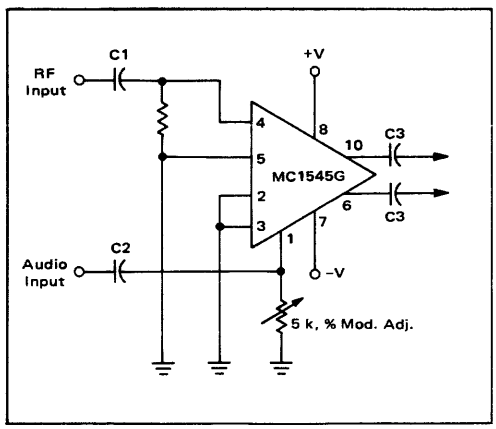


FIGURE 12 – Amplitude Modulator

$$e_o = e_{in} A_{V_1} \qquad (3)$$

Thus the values of E, E_{max}, and E_{min} are

$$E = e_{in} (A_{V_1})_B \qquad (4)$$

$$E_{max} = e_{in} (A_{V_1})_A \qquad (5)$$

$$E_{min} = e_{in} (A_{V_1})_C \qquad (6)$$

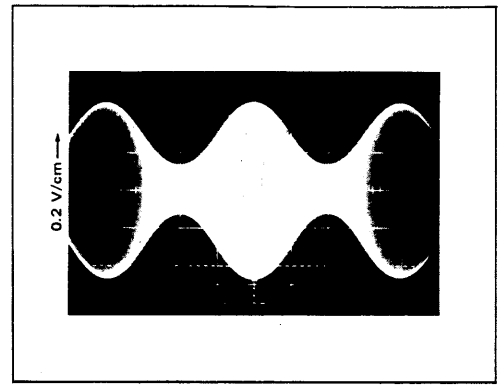


FIGURE 13 – Output Waveform of Amplitude Modulator with 25 MHz RF and 5 kHz Audio

and by using equations (1) and (2), obtain

$$M_U = \frac{(A_{V_1})_A - (A_{V_1})_B}{(A_{V_1})_B} \qquad (7)$$

$$M_D = \frac{(A_{V_1})_B - (A_{V_1})_C}{(A_{V_1})_B}. \qquad (8)$$

Substituting the values of $(A_{V_1})_A$, $(A_{V_1})_B$, and $(A_{V_1})_C$, from Figure 10 into equations (7) and (8) we find

$$M_U = 0.58$$

$$M_D = 0.54$$

These are the values of up and down modulation which can be expected without appreciable distortion.

When the circuit shown in Figure 12 was breadboarded and the resistor adjusted to give the proper bias

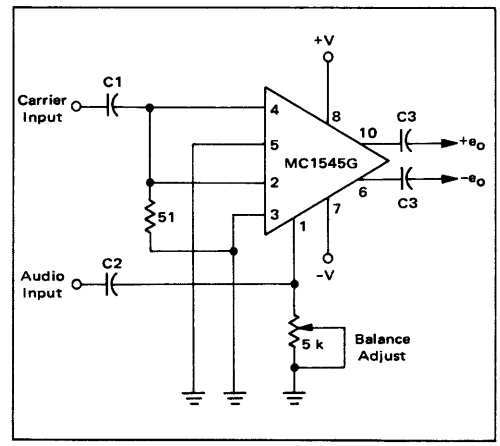


FIGURE 14 – Balanced Modulator

point, the results for a carrier frequency of 25 MHz and an audio frequency of 5 kHz were

$$M_U = 0.54, \qquad M_D = 0.52.$$

From Figure 10, the audio signal required to perform this modulation is approximately 350 mV peak to peak. The output waveform for this circuit is shown in Figure 13. Note that the distortion is very low.

E. Balanced Modulator

The MC1545 can be connected as shown in Figure 14 to function as a balanced modulator. The operation here is quite similar to the operation previously discussed for the amplitude modulator except that the input differential amplifiers have been connected such that their collectors are cross-coupled. This is obvious in Figure 15 where the input stage has been redrawn to reflect its actual operation. If the carrier level is sufficient to completely switch the top differential amplifier pairs, the circuit functions as shown by the approximate equivalent circuit in Figure 15. Here the modulation signal is alternately switched between differential amplifiers at the carrier rate. The result is that the modulation input signal is multipled by a symmetrical switching function which shifts the spectrum of the modulation input and places it symmetrically about the odd harmonics of the carrier. A pictorial explanation of this is shown in Figure 16.

Mathematically the switching function can be written as

$$S(t) = 2\sum_{n=1}^{\infty} A_n \mathrm{Cos} n\omega_c t \qquad (9)$$

where

$$A_n = \left[\frac{\mathrm{Sin}\ \frac{n\pi}{2}}{\frac{n\pi}{2}}\right] \qquad (10)$$

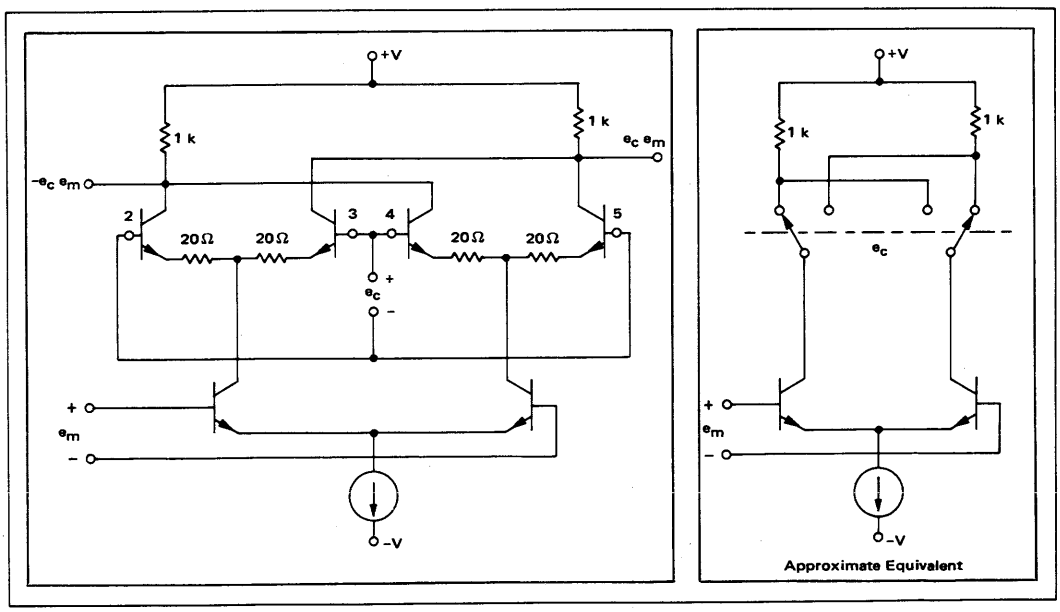


FIGURE 15 – Balanced Modulator Model

Only the odd harmonics are present since $\mathrm{Sin}\ \frac{n\pi}{2} = 0$, for n even.

If the input modulation is given by

$$e_m = E_m \mathrm{Cos}\omega_m t, \qquad (11)$$

then the output will be given by

$$e_o = 2E_m\sum_{n=1}^{\infty} A_n \mathrm{Cos} n\omega_c t \mathrm{Cos}\omega_m t. \qquad (12)$$

By use of the following trigonometric identity,

$$\mathrm{CosACosB} = 1/2\ [\mathrm{Cos}(A+B) + \mathrm{Cos}(A-B)]. \qquad (13)$$

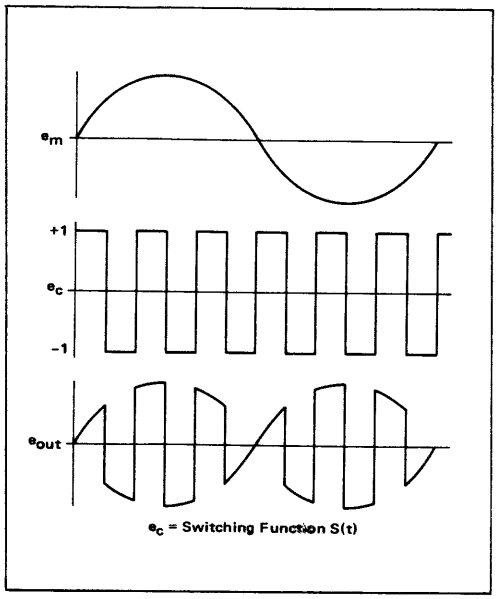


FIGURE 16 – Modulator Waveforms

The final result is expressed in the desired form,

$$e_o = E_m \sum_{n=1}^{\infty} A_n \left[\cos(n\omega_c + \omega_m)t + \cos(n\omega_c - \omega_m)t\right]. \quad (14)$$

Hence, the output is composed of only the sum and difference frequencies (sidebands), and the carrier is suppressed. When the circuit of Figure 14 was evaluated, the carrier rejection that could be achieved was as follows: 62 dB with f_c = 15 kHz and f_m = 3 kHz; 47 dB with f_c = 455 kHz and f_m = 10 kHz, and 36 dB with f_c = 30 MHz and f_m = 10 kHz.

F. Pulse Amplifier

Pulse amplifiers are used in many applications such as pulse radar IF's, pulse width modulation, and pulse amplitude modulation systems.

The MC1545 offers a number of advantages as a pulse amplifier. It has a large bandwidth as is seen in Figure 2. It has dc coupling which provides low frequency response and therefore no droop, and with its differential input and output, common mode signals, such as noise, are greatly attenuated.

Figure 17 shows a typical pulse amplifier connection for the MC1545 giving a voltage gain of 10 V/V (20 dB).

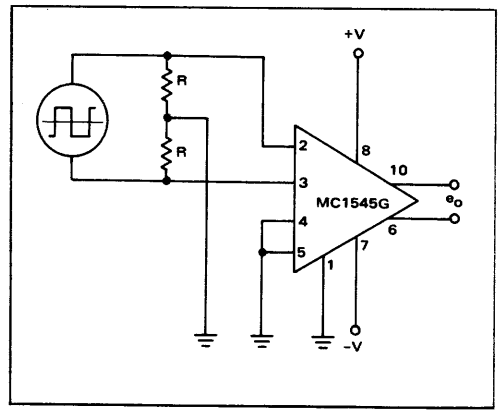


FIGURE 17 – Pulse Amplifier

III. CONCLUSION

A versatile integrated circuit, the MC1545, has been discussed that takes advantage of state-of-the-art I/C fabrication techniques and novel design to give the circuit and systems designers a new building block. The MC1545 serves well in a number of applications, such as a video amplifier, pulse amplifier, FSK keyer, balanced modulator, amplitude modulator, differential amplifier with AGC, preamplifier for core memory sense amplifiers, and many more. The flexibility of this circuit is limited only by the user's imagination.

AN-480
REGULATORS USING OPERATIONAL AMPLIFIERS

INTRODUCTION

Regulators using op-amps as the gain elements usually exhibit better regulation than their IC counterparts due to the higher available loop gain in the op-amp. Voltage drops of less than 0.01% over the entire load range are commonplace, and with care 0.001% is feasible. It is useful to look at all elements of such a regulator design so that in the final result, performance is predictable over load and temperature variations.

This application note will describe the most important device and circuit parameters in regulator design, and show an example of how they may be applied.

BASIC THEORY

Regulators can best be analyzed as a feedback system and as such, can be drawn in block form as in Figure 1. Output voltage for this simplified system is given by:

$$V_O = V_{ref} \frac{G}{1 + GH}$$

where

G = Amplifier gain, A_{VOL}

H = The fraction of V_O fed back to the summing point.

Output voltage, V_O, is less than V_{ref} by the term

$$V_{ref} - V_O = V_{ref} \frac{1}{1 + G} \text{ for } H = 1.$$

For the regulator of Figure 1, improved regulation results from higher amplifier gain.

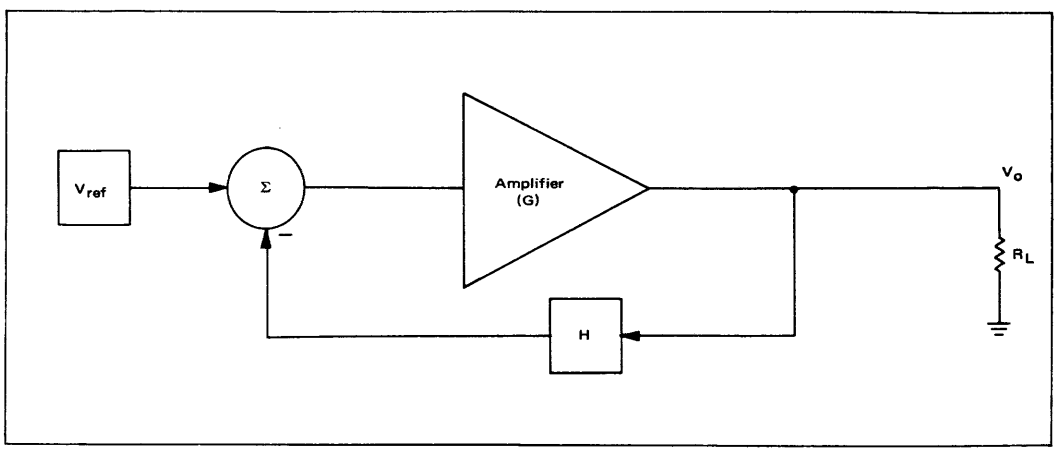


FIGURE 1 – Feedback Amplifier Form of Voltage Regulator

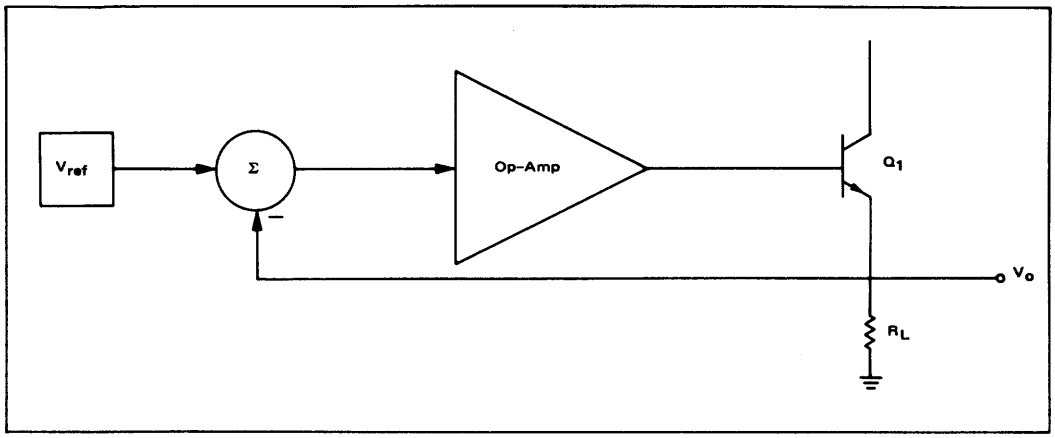


FIGURE 2 – Feedback Regulator with Increased Current Capability

So far no mention has been made of load effects. Indeed, since an ideal amplifier was assumed in the initial circuit, its regulation would be perfect. Therefore, difficulties with regulation may be traced to amplifier qualities so far ignored ... primarily output impedance. The general form of the regulator amplifier is an operational amplifier with an additional emitter follower stage to provide necessary current gain for useful output current, as illustrated in Figure 2. Output impedance for the emitter follower can be quiet low, being approximately the impedance seen at the base of Q_1 divided by the beta of Q_1. The base impedance is predominantly the open loop output impedance of the operational amplifier. Therefore, the open loop (no feedback) output impedance of the regulator is

$$Z_O \text{ (open loop)} \approx \frac{Z_O \text{ (op amp)}}{\beta Q_1}$$

However, when feedback is applied around the amplifier, Z_O drops by the amount of loop gain. For full feedback (H = 1) the output impedance becomes:

$$Z_O \text{ (closed loop)} \approx \frac{Z_O \text{ (op amp)}}{\beta Q_1 (1 + G)}$$

It is obvious that for large amplifier gains there is a big improvement in regulator performance; the output impedance drops. For a second model, the regulator can be drawn as a voltage source with a finite output impedance as shown in Figure 3. Output voltage and percent regulation are now easily calculated as

$$V_O = V' - I_L R_O \text{ and}$$

$$\text{percent regulation} = \frac{V' - V_O}{V'} \times 100$$

$$= \frac{I_L R_O}{V'} \times 100(\%)$$

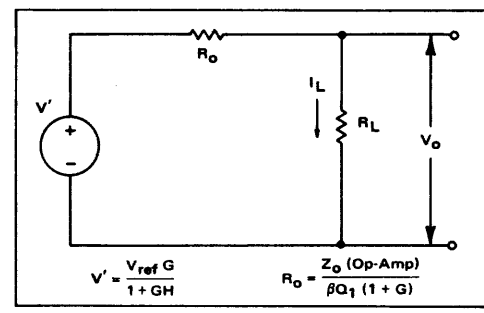


FIGURE 3 – Regulator Model

For some applications the previous equations will adequately describe the dc behavior of the circuit. However, for present day operational amplifiers, capable of gains in excess of 100,000, other factors begin to change the performance to something other than expected. To evaluate these other sources of error, consider an example based on what has been derived so far. Assume an operational amplifier with an open-loop gain of 100,000, an output impedance of 1000Ω, and an emitter follower with a worst case beta (β) of 20. With V_{ref} = 10 volts, the expected no load output voltage, from Equation 2, would be low by an amount

$$V_{ref} - V_O = \frac{10}{1 + 10^5}$$

$$= 0.1 \text{ mV},$$

and regulation from Equation (6) would be:

$$\% \text{ regulation} = \frac{I_L \times R_O}{V'} \times 100$$

$$R_O \approx \frac{10^3}{(20)(10^5)} = 0.5 \text{ m}\Omega$$

$$\% \text{ regulation} \approx \frac{I_L \times 0.5 \times 10^{-3}}{10} \times 10^2$$

for $I_L = 100$ mA

% regulation $\approx 0.05 \times 10^{-2}$

$= 0.0005\%$.

This is indeed good regulation. However, the measured value of such a system may vary by more than an order of magnitude from this figure. Normally neglected amplifier and circuit parameters must now be considered to determine a closer measure of actual performance.

VOLTAGE OFFSETS

According to the calculation in Equation (7), the output voltage will only be 0.1 mV less than the reference. This small difference is usually masked by the input offset voltage (V_{io}) of the operational amplifier which typically runs from 1 to 10 mV for monolithic amplifiers. Therefore, increased gain, without a tighter voltage offset specification, will not guarantee closer tracking of the output voltage to the reference. A second effect of V_{io} is output drift with temperature and loading. Temperature coefficient of the input offset voltage is roughly proportional to V_{io}; drift is typically 5 μV/°C to 20 μV/°C. This not only exhibits itself as added shift between V_O and V_{ref} over temperature, but over loading as well. For example, assume an amplifier operating under the following conditions:

$V_{supply} = \pm 15$ volts

$TCV_{io} = 20\ \mu V/°C$

$I_{Load} = 0, +15$ mA

$\phi_{JA} = 4.6$ mW/°C

The term ϕ_{JA} is thermal conductance from the chip to ambient and can be used to determine junction temperature rise for a given power dissipation. Temperature coefficient of the input offset voltage is not the linear function that the drift specification would indicate (which is usually an average or straight line approximation), but for a rough approximation around normal room ambient it will be sufficient. Added temperature rise due to output loading (for the example given) can be calculated by:

$$°C_{rise} = \frac{\Delta P_{diss}}{\phi_{JA}}$$

$$°C_{rise} = \frac{(15 \times .015)}{\phi_{JA}}$$

$$= 49°C$$

and the input offset drift will be

$$V_{io\ drift} = \frac{\mu V}{°C} \times 49°C$$

$$= 0.98\ mV.$$

For base current requirements of Q_1 approaching the maximum available op amp current (usually 10-15 mA), this drift will be an error in measuring regulation. Output voltage will appear to drift after the load is applied, and after some time will settle to a constant value. The regulation figure ascertained in Equation (8) will be of little value if the V_{io} drift completely covers the excellent short term regulation due to amplifier gain. The thermal time constant associated with chip temperature rise is on the order of 1 or 2 minutes and can easily interfere with attempts to obtain good regulation over load, even though the ac output impedance may appear to be excellent. Since the regulation in Equation (8) corresponds to a voltage change of only 50 μV, virtually any temperature shift on the chip (or in the ambient) can cause the output to move by a significant amount.

COMMON MODE AND POWER SUPPLY REJECTION

If the op amp is connected directly across the incoming voltage (Figure 4), another type of error can occur which

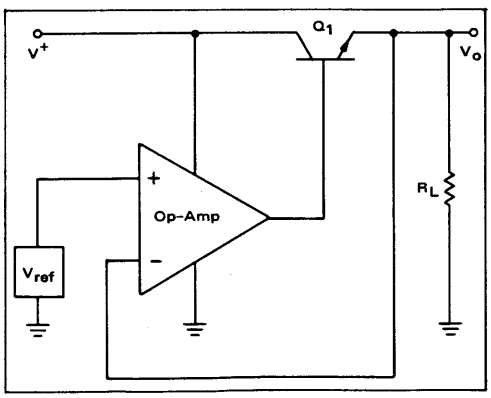


FIGURE 4 – Op-Amp Powered by Line Voltage

again will make the regulation appear much worse than 0.0005%. This is due to dropping input voltage with load current being coupled to the op amp output by the parameter "power supply sensitivity".

If V_{ref} is a value other than the average of V^+ and V^-, the op amp can exhibit a gain, which is specified under "common mode rejection ratio", CMRR. When Q_1 is operated from the same input voltage as the amplifier an effort is usually made to minimize voltage differential across the series pass transistor to maximize efficiency. The common mode voltage $\left(\frac{V^+ + V^-}{2} - V_{ref}\right)$ is then usually quite high under these circumstances and the error that results can become significant if CMRR is less than 80 dB. Common mode error appears as an offset of either polarity at the output and will vary over temperature. For the above mentioned minimum (CMRR = 80 dB), offset will be $\pm 100\ \mu$V per volt of common mode. Rejection of at least 90 dB is desirable to establish minimum offsets from amplifier to amplifier.

VOLTAGE REFERENCE

Output voltage stability with time and temperature depends for the most part on the quality of the voltage reference. Specifying a tight amplifier drift specification alone will not guarantee a stable regulator over temperature, only a good OTC reference will. Other factors to consider, however, are: line rejection, cost, and ease of adjustment (if any). The most obvious solution is to use a zener diode which has a low temperature coefficient by nature (about 5.1 volts), or one that has been compensated by adding forward diodes. Low voltage zeners lack flexibility for use in higher voltage supplies, especially when it is desirable to have $V_{ref} = V_O$, and high-voltage compensated zeners are normally expensive. In addition, when the reference voltage equals the output, current from the input voltage must be used to excite the zener which will cause some line ripple to feed through to the output. A first try at establishing a reference circuit is shown in Figure 5. Since the diode also exhibits a finite resistance

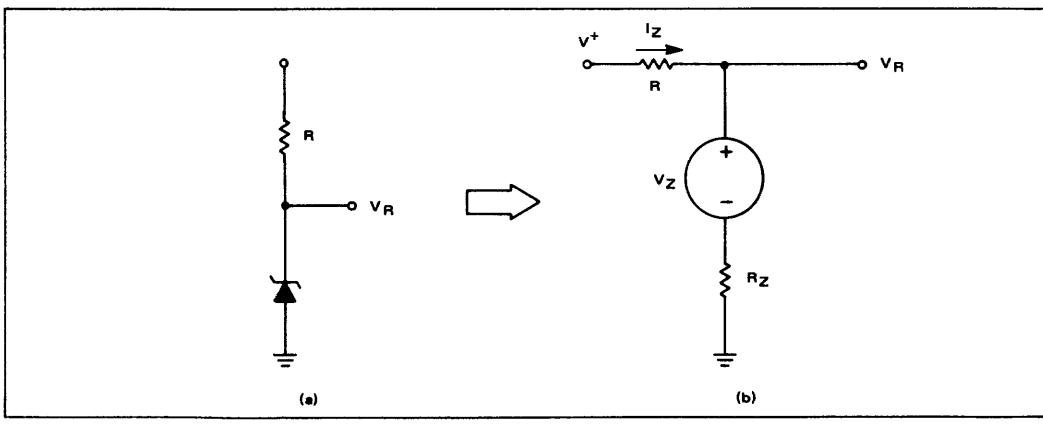


FIGURE 5 – Zener Diode Reference

at each current level, the equivalent circuit may be approximately redrawn as Figure 5B. Reference voltage V_R is now composed of two components, V_Z and $I_Z R_Z$; assuming $I_L = 0$,

$$V_R = V_Z + I_Z R_Z$$

$$I_Z = \frac{V^+ - V_Z}{R + R_Z}$$

$$V_R = \left[\frac{V^+ - V_Z}{R + R_Z}\right] R_Z + V_Z$$

$$V_R = \frac{V^+ R_Z}{R + R_Z} + V_Z \left\{1 - \left[\frac{R_Z}{R + Z_Z}\right]\right\}$$

Note that a portion of the input voltage is coupled into V_R due to R_Z causing input voltage influence at the output. By replacing the resistor R with a current source, V_R may be rendered nearly independent of the input voltage. This is illustrated in Figure 6. Two terminal current regulator "diodes" are now available that have extremely high impedance when operated with more than one or two volts across them and have an upper voltage limit of about 100 volts. A less expensive, but more variable method is the use of a FET with the gate and source pins externally shorted yielding an I_{DSS} current above the pinch off region. An example of this using an N-channel JFET (2N5457) is seen in Figure 6b. This arrangement can also offer an equivalent resistance of several hundred thousand ohms while delivering milliamperes of current to the zener, requiring but a few volts to operate.

Expanding further on the circuit of Figure 6, if the current source is very good, the zener may be replaced by a resistor to establish a voltage whose value is $I_D \times R_2$, as shown in Figure 7. A completely variable reference can be realized by making R a potentiometer. The reference is now at the mercy of the temperature coefficient of the FET, which can be poor unless compensated. But for short term stability this does offer the flexibility of a variable V_R.

A stable, positive voltage reference can be obtained from a currently marketed voltage regulator IC. Only the compensated reference portion of the circuit is used, but it is priced well below compensated zener units which approach its drift specification of 0.002%/°C (typ.). The regulator IC is the MC1560-1460 series. With two external resistors, the reference voltage can set up to 17 volts, as seen in Figure 8. Here, then, is a flexible, stable voltage which should suffice for all but the most critical regulator applications. A high voltage version of this circuit (MC1461-1561) offers outputs to 37 volts to satisfy most system reference needs. Care must be taken, however, when choosing the resistors (R_1 and R_2 in Figure 8) to insure that their temperature coefficients match as closely as possible the device TC for its full value to be realized.

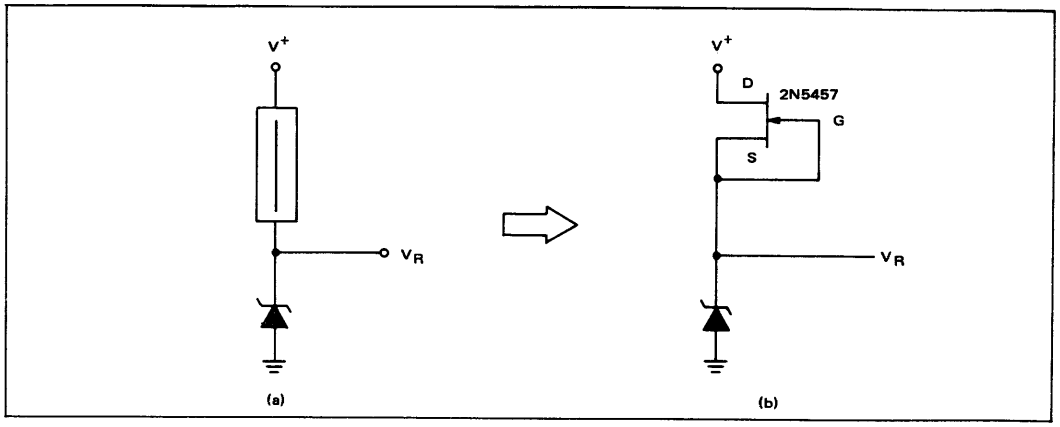


FIGURE 6 – Current Source Stabilized Zener Reference

GROUND LOOPS

So far, considerable discussion has been centered around devices and their effect on overall performance, but the truth is, much regulation can be sacrificed by improper layout and current path considerations. A regulator diagram is given in Figure 9 with critical load path wire resistances shown as R_{W_1} and R_{W_2}. These are the most important simply because they carry the most current and thus drop the most voltage.

Even if $V_O = V_{ref}$, (H = 1), and with $A_V = \infty$, the voltage across the load (V_L) will be only a fraction of V_O

$$V_L = V_O \times \frac{R_L}{R_{W_1} + R_{W_2} + R_L}$$

This may seem insignificant at first glance, but #20 wire exhibits 10 mΩ/ft, which means 1 mV per 100 mA per foot. For the hypothetical regulator designed earlier this completely masks the true regulation. An additional problem can be contact resistance if the regulator output is connected to the system by binding posts or a similar connector rather than being soldered. Even solder joints can result in loss of millivolts if not properly made. Either of the above conditions can be minimized (not eliminated) by "remote sensing" as shown in Figure 10. Voltages at the amplifier inputs are now:

$$V_{\epsilon}^{-} = V_L + I_L R_{W_2},$$

$$V_{\epsilon}^{+} = V_{ref} + I_L R_{W_2},$$

$$V_{\epsilon}^{+} - V_{\epsilon}^{-} = \epsilon = V_{ref} - V_L, \text{ and}$$

$$\frac{V_{\epsilon}^{+} + V_{\epsilon}^{-}}{2} = \frac{V_L + V_{ref}}{2} + I_L R_{W_2}$$

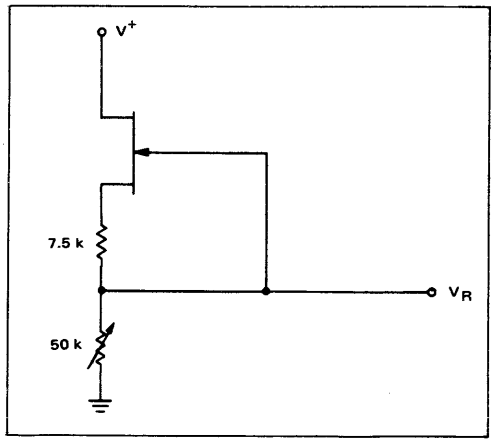


FIGURE 7 – FET Current Source with Potentiometer for Variable V_R

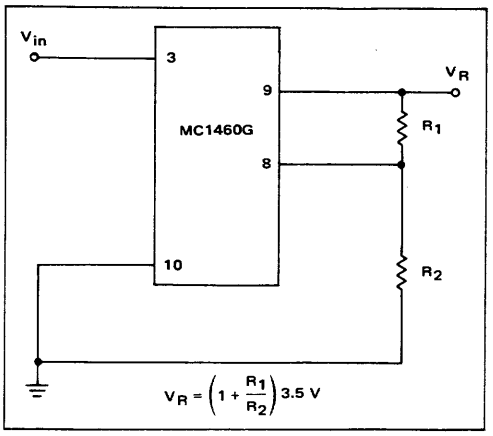


FIGURE 8 – Monolithic Voltage Regulator Used as TC Reference

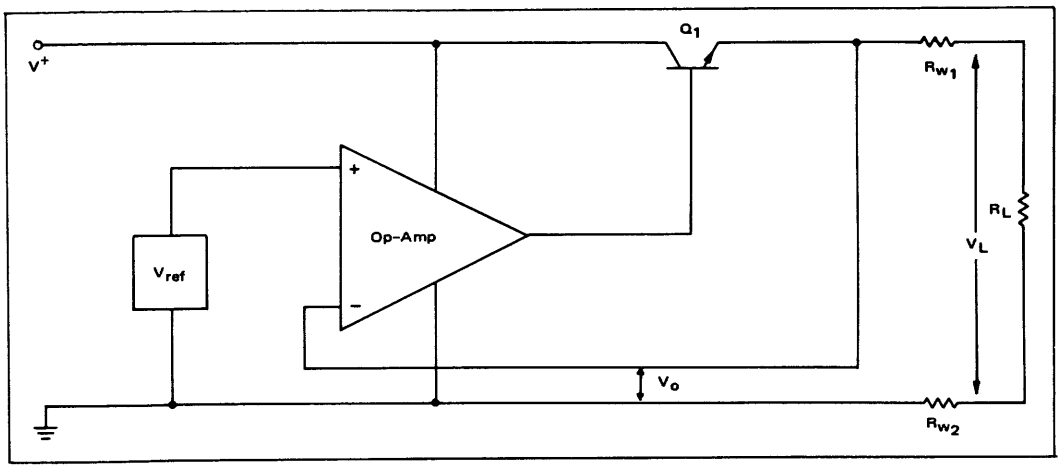


FIGURE 9 – Ground Loop Model

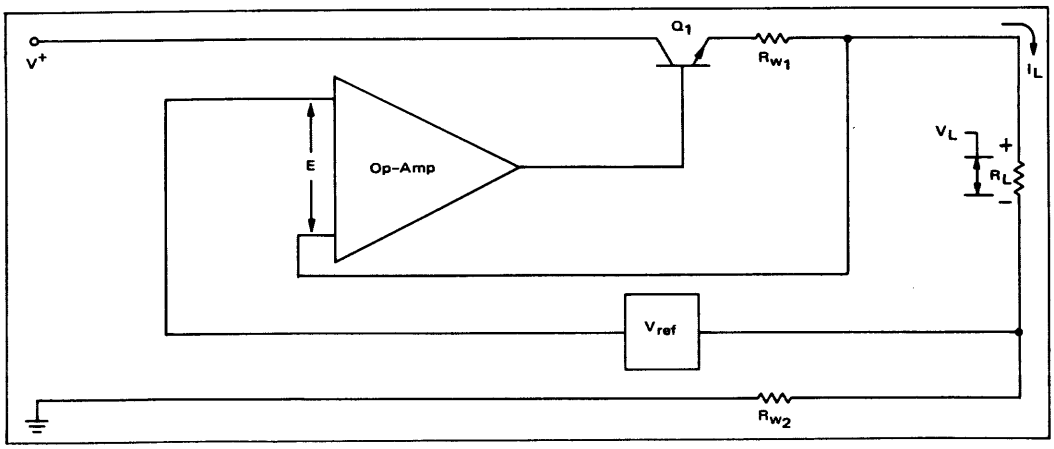


FIGURE 10 – Voltage Regulator with Remote Sensing

Error given by Equation (13) is the same as for the circuit of Figure 4, except that the common mode voltage from Equation (14) is increased by the value $I_L R_{W_2}$. If the common mode rejection of the amplifier is good, this added voltage won't significantly affect performance of the regulator. The sense lines may be small gauge wire since they carry very little current. Resistance R_{W_1} increases the open loop output impedance of the regulator but in most instances an additional 10 or 20 mΩ will not significantly affect performance.

BUILDING A REGULATOR

As an example, using the previous equations and techniques, a +15 volt regulator will be designed using a monolithic operational amplifier. For a preliminary specification, or design goal, assume a tentative 0.1% regulation for a current load change of 0-300 mA and see if it can be realized. Calculated output voltage change from no-load to full-load must be no more than 15 mV, which from Equation (6) indicated a maximum regulator output impedance of 50 mΩ. It is evident from Equation (4) that some consideration must be given to three primary factors influencing output impedance: series pass transistor gain (βQ_1), op-amp open-loop output impedance, and op amp open loop gain (A_{VOL}). A wide range of devices are available that will give the desired result, so they are usually chosen for reasons other than performance, for example, cost and availability. For good performance at moderate cost a 2N4921 will be used as Q_1 and an MC1539 as the operational amplifier. The pertinent device parameters, are:

$\beta Q_1 = 20$ (min),

A_{VOL} (op-amp) = 50,000 (min),

Z_0 (op-amp) = 4 kΩ,

CMRR = 100 dB,

Offset Voltage – 4 mV (max),

TC_{vio} = 5 μV/°C, and

Power supply Sensitivity = 150 μV/V (max).

Regulator output impedance (from Equation (4)) for this combination of devices is 4 mΩ causing a voltage drop under full load of 1.2 mV, only a small part of the allowable error. Maximum current supplied by the amplifier (MC1539) is specified as 15 mA. For a single supply of +30 volts this signifies an additional power drop (besides normal operating power) of 225 mW. Assuming the same ϕ_{JA} as in Equation (8), the additional chip-temperature rise will be 49°C, and the possible offset voltage drift could be as high as 0.245 mV, which is negligible in this case. Since the output voltage is one half the single supply value (+30) and V_{ref} = +15 V, no consideration need be given to common mode effects. Power supply variations affect the output only to the extent listed under "power supply sensitivity", not including reference disturbances, and will also be assumed negligible for this example.

Since typical or minimum performance values were used for both the transistor and the op amp, the fact that regulation is better than the design goal is not surprising.

Static (dc) curves of performance are usually difficult to measure because of output voltage drift and noise. The former is caused by a combination of excellent regulation and relatively poor temperature coefficients. If R_1 and R_2 were matched to 0.02%/°C the output voltage would shift 3 mV for each degree change in their temperature, and this can easily happen when Q_1 begins to heat as load current increases. Regulation, then, becomes dependent on the proximity of R_1, R_2 and Q_1, where it becomes obvious that no amount of amplifier gain can alleviate the difficulties caused by temperature gradients. Transient behavior, however, is indicative of true regulation if done in the proper manner. For noise levels below 1 mV a pulsed load technique may be used and the shift in output voltage noted on an oscilloscope. This is also valuable in establishing overall transient response although the usual "spikes" will be considerably off the scope face when measuring the relatively quiescent dc level shift, illustrated in Figure 13. Another method, although not as direct, can give good results if the operational amplifier

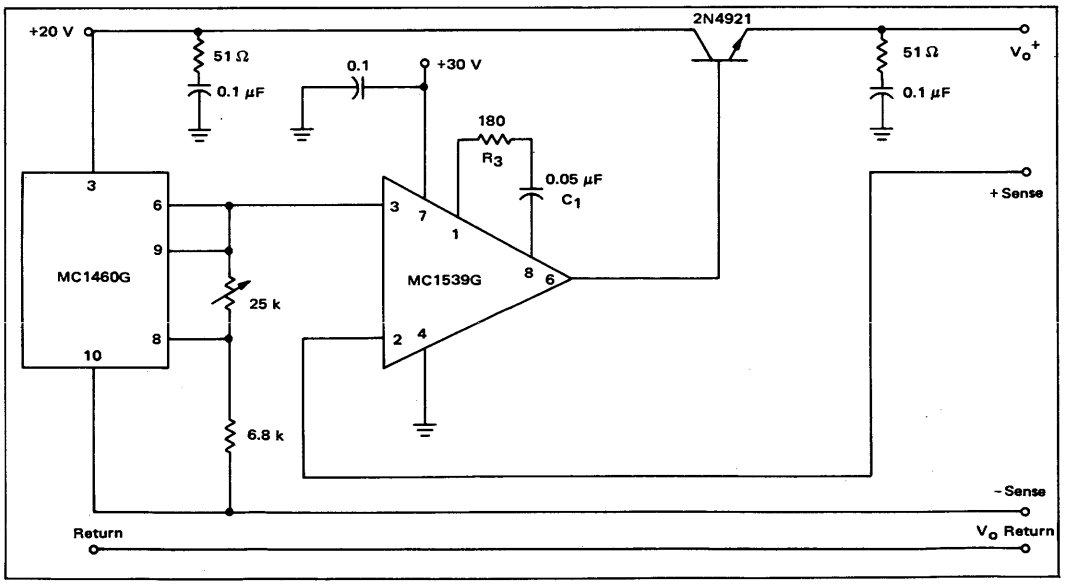


FIGURE 11 – +15 Volt Regulator

As a reference for our regulator, an MC1460G will be used to take advantage of its low temperature coefficient and excellent line rejection. Since ordinary carbon resistors will be used to set the reference level, overall TC will be determined by the TC differences in the resistive divider. However, this effect should show up primarily as output voltage drift with temperature.

The regulator, designed as just described, is shown in Figure 11, and when tested, exhibited the regulation shown in Figure 12.

frequency characteristics are known. If a known value of dc current is drawn through a load of known transconductance, and modulated by a low frequency signal (See Figure 14), any signal voltage appearing as the output will be a function of the signal load-current and the output impedance at that frequency. If the op amp break-points are known, output impedance (slope of $\frac{\Delta V_o}{\Delta I_o}$) can be calculated for a wide range of frequencies (and loads if the dc load level were changed). For the

example regulator, a narrow band (tuneable) RMS voltmeter that will accurately measure ac output voltages in a band from approximately 100 Hz to 100 kHz is used. With a value of 100 Hz as starting point, at a dc load of 100 mA and an ac modulation of 10 mA (RMS), the output voltage is 0.1 mV RMS (BW = 10 Hz). This corresponds to an output impedance of 10 mΩ. However from the compensation values used (0.05 μF, 180 Ω), it is known that the first pole or break point occurs at approximately 10 Hz, a factor of 10 from the signal frequency. If the opamp rolloff is 6 dB/oct, then at dc the output impedance would be 1 mΩ. For frequencies much removed from the audio region, other poles (or zeros) may make the calculation more difficult; a choice of frequencies between the first pole and zero ($f_Z = \frac{1}{2\,R_3C_1}$) is usually wise.

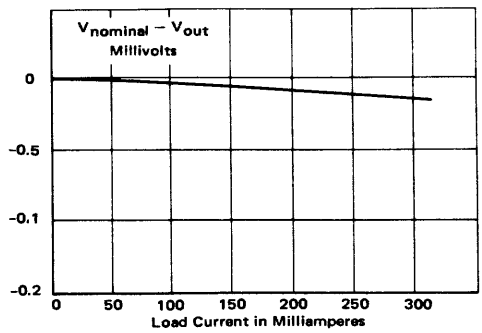


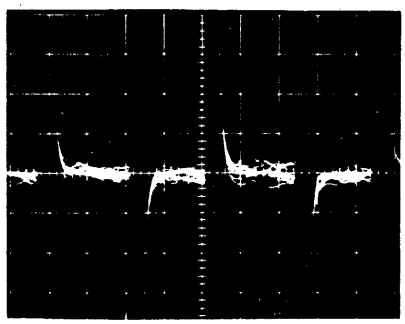
FIGURE 12 – Load Regulation for Circuit in Figure 11

TRANSIENT RESPONSE

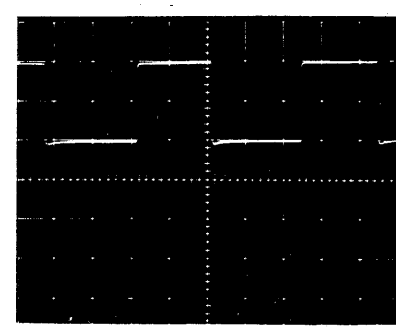
Output impedance vs frequency and transient response are not unrelated for a small signal analysis. If the output impedance remains low at high frequencies, then transients will disturb the output voltage very little. However, as noted, op-amps tend to begin "rolling off" frequency response rather early (for stability considerations) and hence the output impedance, directly related to amplifier gain, goes up with frequency, even with output capacitors. Operational amplifiers with relatively low gain (<10,000) usually exhibit better bandwidth than high gain units and make better regulators where medium frequency output impedance is a factor. However, for non-linear loop response, small signal parameters become useless and slew rate must be considered as the prime parameter for designing performance. Non-linear operation is encountered if transient speed is faster than the amplifier's ability to correct or follow. Speed of recovery is then a function of the amplifier's large-signal maximum rate of change as indicated by its power bandwidth or slew rate. Since direct feedback usually dictates unity gain compensation, good transient response may be difficult.

CONCLUSION

Excellent dc regulators can be constructed using operational amplifiers if adequate precautions are taken in construction and sensing. Open loop gains in excess of 100,000 are beneficial unless very tight specifications on amplifier input offset and reference drift are established. Short term regulation of 0.01% is easily realizable with 0.001% well within expectations if some care is exercised.



Regulator Output under Pulsed Load Condition (12 b)
Horizontal Scale: 200 μs/cm
Vertical Scale: 1 mV/cm



Load Current Waveform for 12 a
Horizontal Scale: 200 μs/cm
Vertical Scale: 100 mA/cm

FIGURE 13 – Regulator Test Waveforms

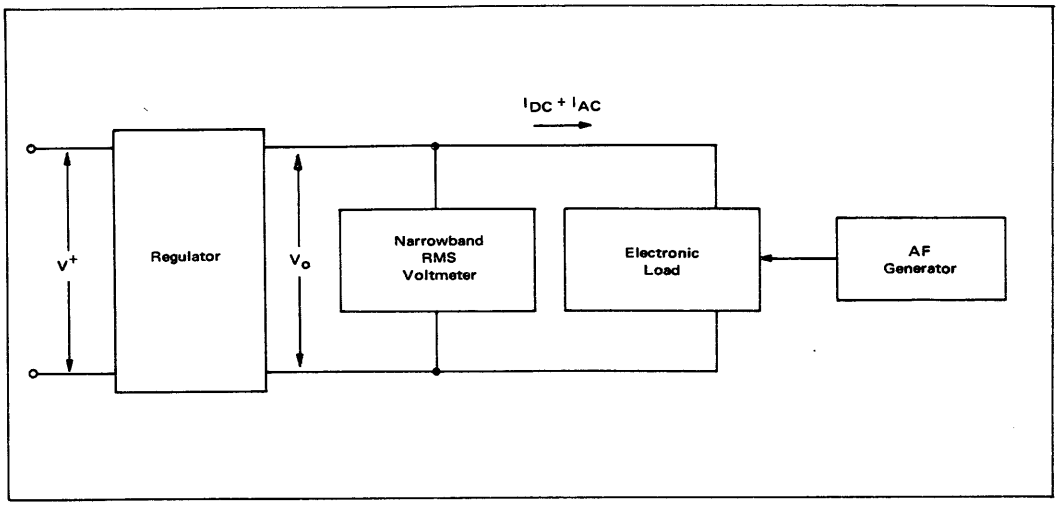


FIGURE 14 – Regulator Test Using RMS, Narrow-Band Voltmeter

APPENDIX A

If the regulator output is to be a multiple of the reference voltage the circuit of Figure A-1 is usually used. Regulation for this circuit will be worse than for a circuit where the reference and output voltages are equal because of the loop attenuation introduced by R_1 and R_2. Output impedance is given by

$$Z_0 \text{ (closed loop)} = \frac{Z_0 \text{ (op amp)}}{\beta_{Q_1}\left[1+\left(\frac{A_{VOL}R_1}{R_1+R_2}\right)\right]}$$

Common mode rejection and power supply sensitivity are degraded to:

$$CMRR^* = CMRR\left|_{dB} - (1+\frac{R_2}{R_1})\right|_{dB}$$

$$\text{Power Supply Sensitivity}^* \approx PSS\left[1+\frac{R_2}{R_1}\right]$$

Not only is the reference increased by $(1+\frac{R_2}{R_1})$, but the offset voltage and its drift as well as the reference drift. For many reasons this connection can be shown to be inferior except from the standpoint of slew rate where the attenuation of $\frac{R_1}{R_1+R_2}$ allows a compensation other than unity giving a wider power bandwidth.

APPENDIX B

"Floating" IC Regulators

Voltage regulators utilizing monolithic operational amplifiers are often used for stabilizing voltages considerably higher than their ratings. This control is possible because the entire circuit is not referenced to ground, but rather "floated" between ground and the supply voltage. A simplified version of the most popular form is illustrated in Figure B-1.

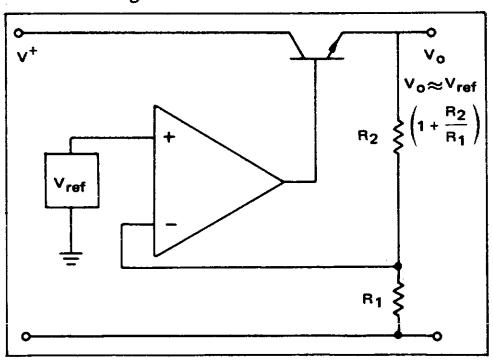


FIGURE A-1 – Regulator Circuit Using a Reference that is a Multiple of the Output

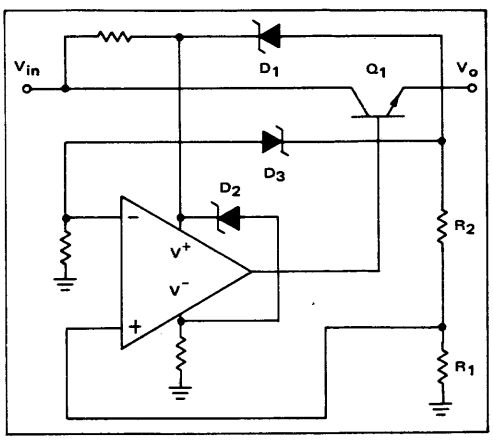


FIGURE B-1 – Floating Regulator

Zener D_1 insures that the IC positive supply is greater than the required output swing. D_2 maintains a constant supply voltage for the unit ($V^+ + V^-$) = V_{D_2}. The voltage across the IC, is then tied to the output voltage by fixed constants.

Disregarding the power source for the op amp (discussed above), the schematic can be further simplified to that of Figure B-2.

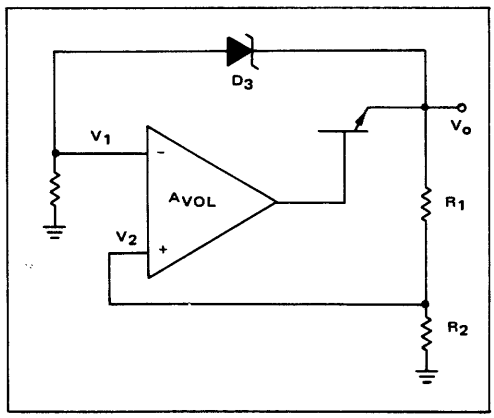


FIGURE B-2 – Simplified Floating Regulator Model

The transfer function $\frac{V_0}{V_{D_3}}$ may be simply derived if common mode effects are neglected:

$$V_2 = \frac{R_2}{R_1 + R_2} V_0$$

$$V_1 = V_0 - V_{D_3}$$

$$V_0 = A_{VOL}(V_2 - V_1)$$

$$V_0 = A_{VOL}\left[\frac{V_0 R_2}{R_1 + R_2} - V_0 + V_{D_3}\right]$$

$$V_0 = A_{VOL} V_0\left[\frac{R_2}{R_1 + R_2} - 1\right] + A_{VOL} V_{D_3}$$

$$V_0 \quad 1 + A_{VOL}\left(1 - \frac{R_2}{R_1 + R_2}\right) = A_{VOL} V_{D_3}$$

$$\frac{V_0}{V_{D_3}} = \frac{A_{VOL}}{1 + A_{VOL}\frac{R_1}{R_1 + R_2}}$$

for $A_{VOL}\frac{R_1}{R_1 + R_2} \gg 1$

$$\frac{V_0}{V_{D_3}} = \frac{R_1 + R_2}{R_1} \text{ or } V_0 = \frac{R_1 + R_2}{R_1}(V_{D_3})$$

The circuit responds as a zener "multiplier"; the output voltage (V_0) is a multiple of the reference voltage. Another circuit which performs the same function is illustrated in Figure B-3. The chief drawback of the circuit of Figure B-3 is that the output voltage can be much higher (for large multiplication ratios) than the common mode voltage (V_Z). For the floating regulator (Figures B-1 and B-2), the output voltage may rise as high as voltage precautions permit, but it is not limited by either common mode or differential voltage problems.

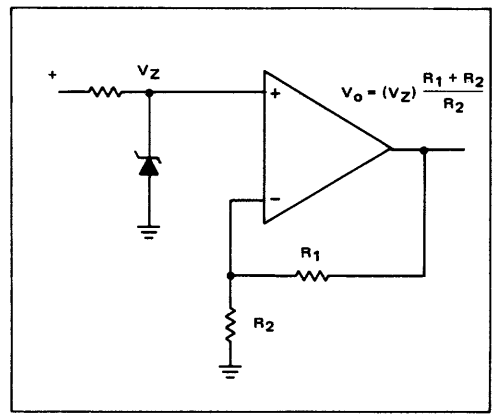


FIGURE B-3

One limitation peculiar to this regulator is that regulation decreases for increasing output voltages. This is a result of the loop gain being dependent on the zener multiplication factor $\frac{R_1}{R_1 + R_2}$. For example, if $A_{VOL} = 50{,}000$, $V_{D_1} = 10$ V, and $V_0 = 100$ V, the resultant loop gain is $\frac{A_{VOL}}{10} = 5000$. This value may not be sufficient to support the desired regulation; the degradation of output impedance should be kept in mind for variable voltage supplies constructed in this manner.

PRECAUTIONS

Zener voltage values cannot be chosen haphazardly, although there is some margin. The value of V_{D_2} (of Figure B-1) is determined by the power supply requirements of the op amp, but will usually be 30 volts. Values of V_{D_1} and V_{D_3} are interdependent and will be governed by the weight placed on loop gain (regulation) versus ease of finding a good zener with a low temperature coefficient. Nominally, V_{D_1} may be chosen to be 10 volts. V_{D_3} should be chosen to place the op amp input in a favorable common mode range. To visualize this, consider Figure B-4 where an output voltage of 75 volts is to be regulated. V_{D_2} and V_{D_1} have been chosen as above.

Zero common mode level (relative to the power supplied) is: $\frac{85+55}{2} = 70$ V. This would indicate that V_{D3} may be anywhere in the range of 5 V $\pm V_{max(cm)}$. For stability, the value may be 5.6 volts which is nearly zero-TC without compensation. If V_{D1} had been a smaller value, the common mode limits would have been lower, and the allowable values of V_{D3} higher. The components under a high voltage stress are resistor R_2 and the series pass transistor if appreciable voltage is dropped across it. Regulation for a circuit of this type is always a function of the desired output voltage level, decreasing proportional to the zener multiplication factor, but can provide reasonably good regulation at moderate voltages (100-250 volts) and in a small package.

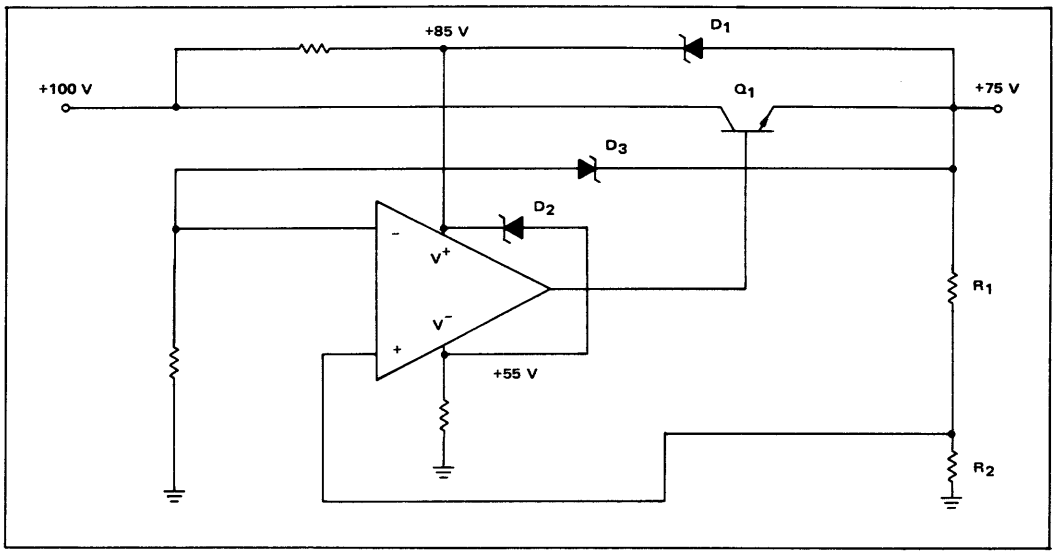


FIGURE B-4

AN-489
ANALYSIS AND BASIC OPERATION OF THE MC1595

INTRODUCTION

The Motorola MC1595 four quadrant multiplier is the second basic building block now available to analog systems designers. Any control or instrumentation problem which requires the product, square, square root or ratio of two analog quantities can be easily achieved with the MC1595. Monitoring power, brake horsepower, fluid flow, solving of complex non-linear equations (using analog computer techniques), frequency doubling, phase detection, dynamic gain control, taking roots or powers, modulation circuits, navigational problems, velocity, acceleration and distance for linear or non-linear inputs, root mean square calculations, and generation of trigonometric functions are only a few of the applications for this device.

This note will be concerned with an analysis of the MC1595, the basic operating and design procedure and a few applications that will hopefully encourage the designer to consider the multiplier in his future system designs.

REVIEW OF MULTIPLICATION TECHNIQUES

There are many methods of performing analog multiplication.[1] The following partial list is offered as a brief comparison of techniques:

1. **Hall Effect** – The basic principle behind the hall effect multiplier is that the voltage across a conductor is proportional to both the current through it and the strength of the magnetic field across it.

2. **Magnetoresistance** – A magnetoresistance multiplier is basically a Wheatstone bridge made up of flux-sensitive resistors where the two variables to be multipled are the current in the coil producing the flux and the voltage across the bridge.

3. **Variable Transconductance** – A multiplier of the variable transconductance variety is based on the idea that the output of a transistor amplifier depends upon the input signal and the magnitude of the effective emitter resistance (common-emitter configuration assumed) which can be controlled by the magnitude of the emitter current. Hence, the output at the collector is proportional to the input signal times a function of the emitter current.

4. **Quarter Square** – This technique makes use of the mathematical identity $XY = 1/4\ [(X + Y)^2 - (X - Y)^2]$. Diodes are generally used to generate the square-law functions required.

5. **Pulse Height/Width** – An oscillator generates a train of rectangular pulses in which the height of the pulses is modulated by one input and the other input modulates the width. The area of the pulses is then proportional to the product of the two inputs.

6. **Triangle Averaging** – This is a variation of the quarter-square method. Instead of the square-law functions used in the quarter-square method, quadratic functions are generated by integration of clipped triangular waveforms.

7. **Logarithmic Sum** – This is the technique by which an everyday slide rule operates. XY = antilog [log X + log Y]. Log and antilog functions can be easily generated using a nonlinear element in conjunction with an operational amplifier.[2]

Of these seven methods of performing analog multiplication, the third (Variable Transconductance) is best suited to monolithic implementation. The concept of variable transconductance is used in the implementation of analog multipliers in monolithic form, the MC1595.

MULTIPLIER DISCUSSION

Multiplier circuits have been constructed using digital techniques but for reasonable accuracy the gate-count is quite high. However, the use of a linear circuit had the disadvantage of distorting at least one input due to the nonlinear processing involved. The MC1595, on the other hand, has overcome the distortion problem by preconditioning one input that cancels the nonlinear processing distortion. This preconditioning is shown in Figure 1.

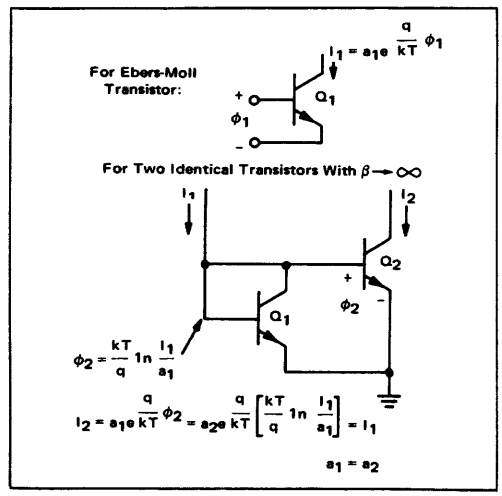


FIGURE 1 – Multiplier Preconditioning Principle

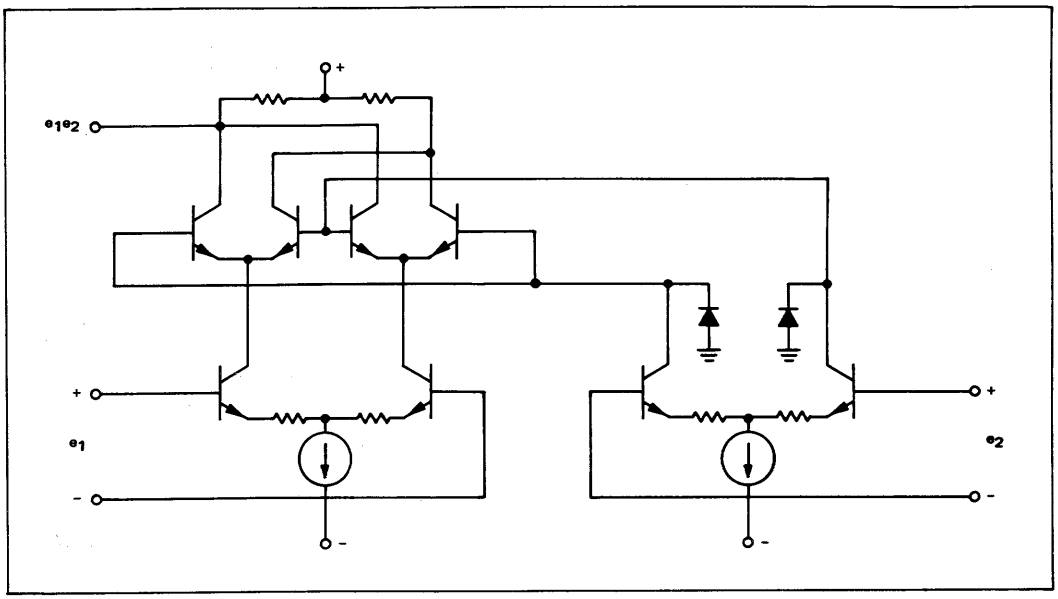


FIGURE 2 – Linear Four-Quadrant Multiplier Model

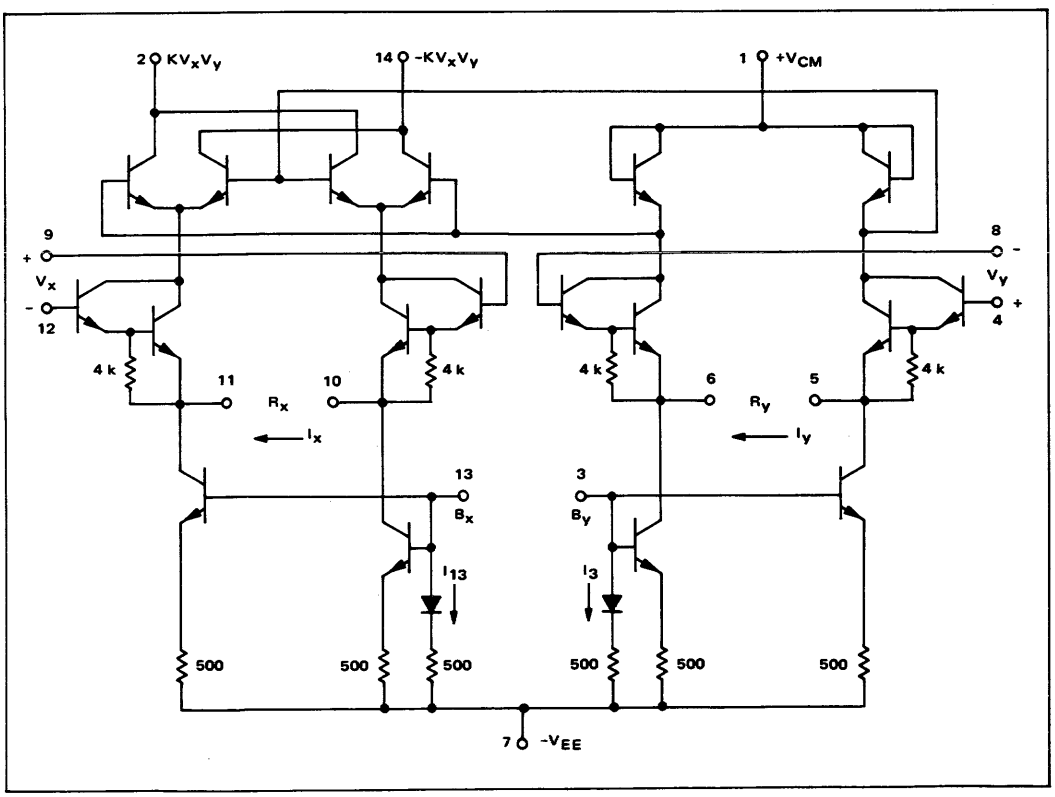


FIGURE 3a – Monolithic Realization of the MC1595 Linear Multiplier

Briefly, this operation can be explained by considering the collector response of a transistor to an input base-emitter voltage. For two identical transistors, as shown, an input I_1 is seen to produce an output I_2 that is approximately equal to I_1. This is achieved by first converting the input current into a voltage ϕ_1 which is logarithmically related to I_1, and then converting ϕ_1 into a current I_2, that is exponentially related to ϕ_1. Since the transistors used are identical, the logarithmic operation cancels the exponential operation and output I_2 responds linearly to input I_1. Note that I_1 has been processed nonlinearly in the transistor junctions.

In Figure 2, a modified version of the balanced multiplier is shown in which the e_2 input has been processed through a diode-transistor network to produce a linear response via nonlinear preconditioning. The original circuit responds linearly to the e_1 input, so the output is now linearly dependent upon the product of e_1 and e_2. A monolithic realization of the complete multiplier circuit is shown in Figure 3a, where the input emitter degeneration and operating currents are adjustable to accommodate a variety of input signals and applications. The circuit just developed is the new Motorola MC1595 Linear Four-Quadrant Multiplier. A photograph of the MC1595 die is shown in Figure 3b.

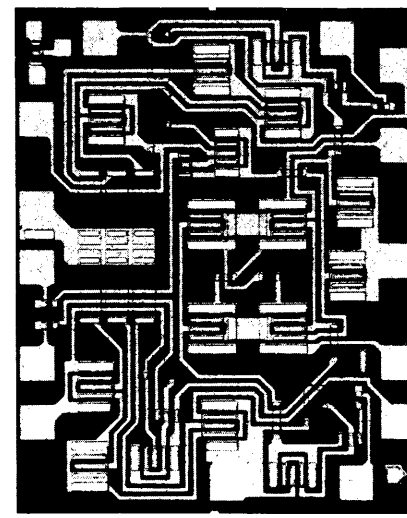


FIGURE 3b – MC1595 Die

MC1595 ANALYSIS

Figure 4 will be used as the equivalent model for the analysis of the MC1595 multiplier. For the purposes of this analysis, the following conventional assumptions have been made for simplification: (1) Devices of similar geometry within a monolithic chip are assumed identical and matched where necessary, and (2) transistor base currents are ignored with respect to the magnitude of collector currents; therefore, collector and emitter currents are assumed equal.

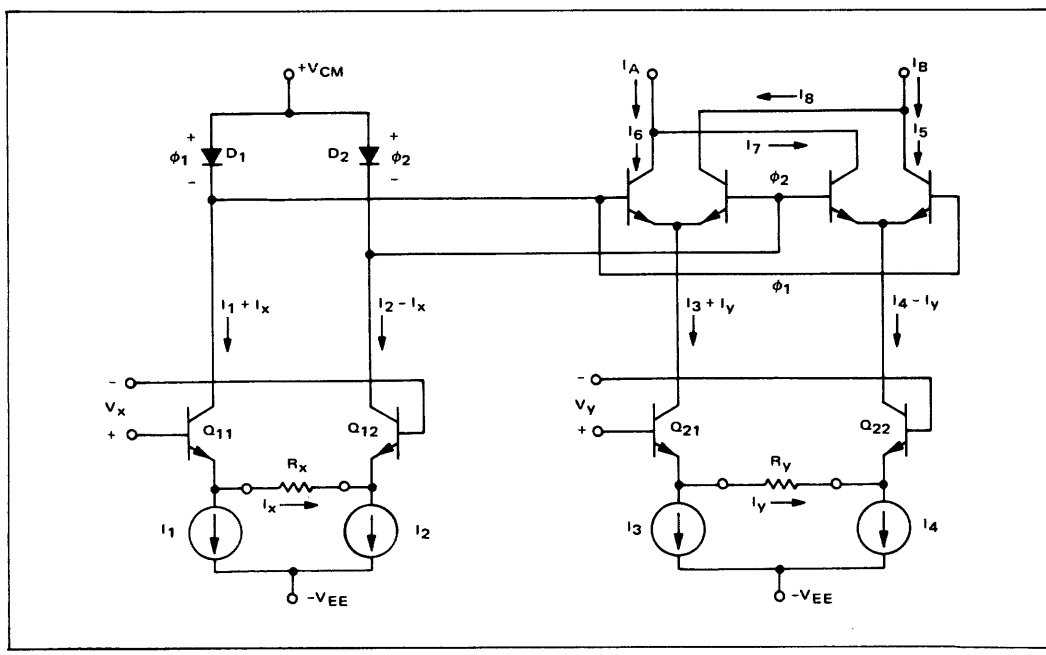


FIGURE 4 – MC1595 Equivalent Model for Analysis

From the model of Figure 4, the following equations are obtained:

$$I_3 + I_y = I_6 + I_8 \quad (1)$$

$$I_4 - I_y = I_5 + I_7 \quad (2)$$

$$I_A = I_6 + I_7 \quad (3)$$

$$I_B = I_8 + I_5 \quad (4)$$

$$I_8 = \frac{I_3 + I_y}{1 + e^{\left[\frac{\phi 1 - \phi 2}{V_T}\right]}} \quad (5)$$

$$I_5 = \frac{I_4 - I_y}{1 + e^{\left[\frac{\phi 2 - \phi 1}{V_T}\right]}} \quad (6)$$

$$I_6 = \frac{I_3 + I_y}{1 + e^{\left[\frac{\phi 2 - \phi 1}{V_T}\right]}} \quad (7)$$

$$I_7 = \frac{I_4 - I_y}{1 + e^{\left[\frac{\phi 1 - \phi 2}{V_T}\right]}} \quad (8)$$

where $V_T = \frac{kT}{q} \approx 26$ mV at +25°C.

For simplicity, let us define

$$m = \frac{\phi 1 - \phi 2}{V_T}. \quad (9)$$

Substituting (5) and (6) into (4), and solving for I_B, obtain

$$I_B = \frac{I_3(1 + e^{-m}) + I_4(1 + e^{m}) - I_y(e^{m} - e^{-m})}{(1 + e^{m})(1 + e^{-m})} \quad (10)$$

and similarily with equations (7), (8), and (3) I_A can be solved for:

$$I_A = \frac{I_3(1 + e^{m}) + I_4(1 + e^{-m}) + I_y(e^{m} - e^{-m})}{(1 + e^{m})(1 + e^{-m})} \quad (11)$$

A differential output current defined as

$$\Delta I = I_A - I_B \quad (12)$$

can be expressed as

$$\Delta I = \frac{(e^{m} - e^{-m})(I_3 - I_4 + 2I_y)}{(1 + e^{m})(1 + e^{-m})} \quad (13)$$

Now, for diodes D_1 and D_2 in Figure 4 the following can be written,

$$I_1 + I_x = a_{11}(e^{\frac{\phi 1}{V_T}} - 1) \approx a_{11} e^{\frac{\phi 1}{V_T}} \quad (14)$$

$$I_2 - I_x = a_{11}(e^{\frac{\phi 2}{V_T}} - 1) \approx a_1 e^{\frac{\phi 2}{V_T}} \quad (15)$$

where the approximate equivalence is justified by assuming that the diodes are sufficiently forward biased. Further, it is observed that

$$\frac{I_1 + I_x}{I_2 - I_x} = e^{\left[\frac{\phi 1 - \phi 2}{V_T}\right]} = e^{m} \quad (16)$$

which, when substituted into equation (13), yields

$$\Delta I = \frac{(I_1 - I_2 + 2I_x)(I_3 - I_4 + 2I_y)}{(I_1 + I_2)}. \quad (17)$$

For the desired case where $I_1 = I_2$ and $I_3 = I_4$ (which can be controlled quite well on a monolithic chip),

$$\Delta I = \frac{2I_xI_y}{I_1}. \quad (18)$$

The currents I_x and I_y are given by

$$I_x = \frac{V_x}{R_x + r_{e11} + r_{e12}} \quad (19)$$

$$I_y = \frac{V_y}{R_y + r_{e21} + r_{e22}} \quad (20)$$

where r_{e11}, r_{e12}, r_{e21}, and r_{e22} are the bulk emitter resistances of the model transistors Q_{11}, Q_{12}, Q_{21}, and Q_{22} respectively. The bulk emitter resistance can be expressed as

$$r_e = \frac{kT}{qI_E} \approx \frac{26\text{ mV}}{I_E} \quad (21)$$

at +25°C. It will be shown that the maximum value for any of the bulk emitter resistances will be limited by placing a minimum constraint condition on the I_E terms in Equation (21). In doing so, the following approximation is seen:

$$\Delta I = \frac{2V_xV_y}{I_1(R_x + r_{e11} + r_{e12})(R_y + r_{e21} + r_{e22})} \approx \frac{2V_xV_y}{I_1R_xR_y}, \quad (22)$$

and if I_A and I_B from Equation (12) are dropped across a

load resistor (R_L), a differential output voltage approximation would be

$$\Delta V_O = \Delta I R_L$$

$$\approx \frac{2R_L V_X V_Y}{I_1 R_X R_Y} \qquad (23)$$

which illustrates the four-quadrant capability of the MC1595, giving sign and magnitude information linearly with respect to each input.

If the approximations of Equations (22) and (23) are to be valid, the bulk emitter resistances must be kept small to minimize the error introduced by the currents I_X and I_Y. For example, with I_X and I_Y in the direction shown in Figure 4 and $I_1 = I_2$, $I_3 = I_4$ as discussed previously, then the bulk resistances seen in the model circuit are

$$r_{e11} \approx \frac{V_T}{I_1 + I_X},$$

$$r_{e12} \approx \frac{V_T}{I_1 - I_X},$$

$$r_{e21} \approx \frac{V_T}{I_3 + I_y},$$

$$r_{e22} \approx \frac{V_T}{I_3 - I_y}, \qquad (24)$$

where, as before, $V_T \approx 26$ mV at +25°C. The two "problem" resistances are r_{e12} and r_{e22}. r_{e12} will become very large as $(I_1 - I_X)$ approaches zero. That is, if $I_1 = I_X$, then transistor Q_{12} is not conducting and the r_{e12} appears to be quite large. Considerable nonlinearity and distortion will result if the emitter currents are ever allowed to become too small. As a working constraint, the emitter currents will never be lower than one-third the value fixed in the current sources I_1 (= I_2) or I_3 (= I_4)

From Figure 3, values of the current sources are set by applying a bias voltage to pins 3($I_1 = I_2$) and 13($I_3 = I_4$). Referring once again to Figure 3, and recalling that we have assumed that base currents can be ignored in calculations, then the current flowing into pin 3 is equal to the value of each of the current sources designated I_1 and I_2 in Figure 4, and similarly the current flowing into pin 13 is equal to the value of each of I_3 and I_4 in Figure 4. To avoid any further confusion in notation, we will designate the current into pin 3 as I_3 and the current into pin 13 as I_{13} (as illustrated in Figure 3).

By using the emitter current constraints (see next section, "Using the Multiplier"), the bulk emitter resistances can be less than 1% of the emitter degeneration resistors (R_X and R_Y), and hence can be ignored. Therefore, the differential output voltage can be expressed as

$$V_O = KV_XV_y, \qquad (25)$$

where

$$K = \frac{2R_L}{I_3 R_X R_y}. \qquad (26)$$

USING THE MULTIPLIER

From the previous circuit analysis of the MC1595, the circuit of Figure 5 illustrates the basic configuration for using the multiplier.

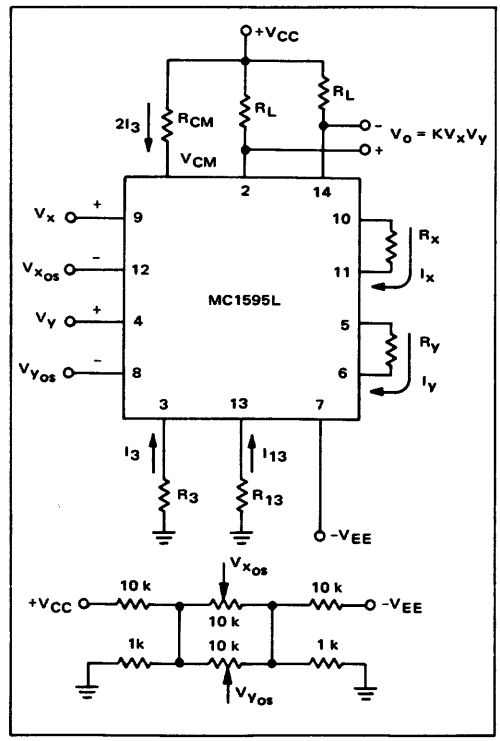


FIGURE 5 – Basic Multiplier Configuration

To demonstrate the thought process one would go through in the initial design phase, consider the following example which is widely used in multiplier applications.

Example:

Input Voltage Ranges:

$-10\text{ V} \leqslant V_X \leqslant +10\text{ V}$

$-10\text{ V} \leqslant V_Y \leqslant +10\text{ V}$

Output Dynamic Swing: ±10 V

$$K = \frac{1}{10}$$

A good place to begin is the current sources since most other decisions will depend on their value.

The value of the current sources I_3 and I_{13} can be determined by applying a known potential to pins 3 and 13 respectively. One should select a value of current that will keep the chip power dissipation to an acceptable value and still maintain operation in a good exponential portion of the diode curve. A value of 0.5 mA to 2.0 mA is seen to be feasible, and a value of 1.0 mA is used to illustrate the operation of the device in this example. The value of the current sources can be fixed once the value of the negative supply has been chosen. A negative supply of -15 volts has been selected for this mode of operation which will allow a -10 V input capability and insure linear operation in the current source transistor, and stay within the 30 volt MAXIMUM RATING between any input pin and the negative supply pin (as specified in the data sheet). With $-V_{EE}$ = -15 V, the current sources are each set to 1.0 mA by putting a resistor from pin 3 to ground and from pin 13 to ground as

$$(R + 500\Omega)\,(1\text{ mA}) = (15 - 0.7)\text{V}$$
$$R = 13.8\text{ k}\Omega \qquad (27)$$

where the forward voltage of a silicon diode is assumed to be 0.7 volts. Since this is not a critical adjustment, a convenient value of 13.7 kΩ, 1/4 W composition is used.

Recalling the emitter current constraints, from which we were able to ignore the bulk emitter resistance terms, the following is seen for the emitter resistors R_X and R_Y:

$$R_X = \frac{V_{x(max)}}{I_{x(max)}} \qquad (28)$$

$$= \frac{V_{x(max)}}{2/3\,(I_{13})} \qquad (29)$$

$$= \frac{+10\text{ V}}{2/3\,(1.0\text{ mA})}$$

$$= 15\text{ k}\Omega$$

and

$$R_y = \frac{V_{y(max)}}{I_{y(max)}} \qquad (30)$$

$$= \frac{V_{y(max)}}{2/3\,(I_3)} \qquad (31)$$

$$= \frac{+10\text{ V}}{2/3\,(1.0\text{ mA})}$$

$$= 15\text{ k}\Omega.$$

R_X and R_Y are equal in this example because the maximum voltage at both inputs are equal, which is not necessarily so in all applications.

From Equation (26) the value of the load resistors are each found to be

$$R_L = \frac{KI_3R_XR_y}{2}$$

$$= \frac{(10^{-1})(10^{-3})(15 \times 10^3)(15 \times 10^3)}{2}$$

$$= 11.25\text{ k}\Omega \qquad (32)$$

and if I_3 is varied slightly, a standard value 11 kΩ resistor can be used. To vary I_3, R_3 is a 10 k resistor in series with a 5 k pot. At this point, everything necessary for operation of the device has been specified except the common-mode resistor (R_{CM}) at pin 1 and the positive supply ($+V_{CC}$).

With a +10 V input at V_y, the voltage at the collectors of the V_y-input differential amplifier should be about 13 V to insure linear operation; hence, the common-mode voltage at pin 1 must be about +13.7 V. The +13 V collector potential appears at the bases of the cross-coupled differential pair where the minimum collector potential, again to insure linear operation, should be about +16 V. With a minimum of about 16 volts and a 10 volt swing, the quiescent collector potential is about 21 volts. In this quiescent condition the current source value (1 mA) is seen in each load resistor (11 kΩ); therefore, a positive supply of 32 volts is required. Using $+V_{CC}$ = +32 V, the desired voltage at pin 1 is obtained through a common-mode resistor, R_{CM} as

$$R_{CM} = \frac{(32 - 13.7)\text{V}}{2\text{ mA}}$$

$$= 9.15\text{ k}\Omega. \qquad (33)$$

Since the collector potential is not critical, a value of 9.1 kΩ, is acceptable.

To summarize the operating configuration:

$+V_{CC}$ = +32 V
$-V_{EE}$ = -15 V
R_{13} = 13.7 kΩ
R_3 = 10 kΩ + 5 kΩ pot (Gain Adjust)
$R_x = R_y$ = 15 kΩ
R_L = 11 kΩ
R_{CM} = 9.1 kΩ

which is illustrated in Figure 6.

One final item that needs to be mentioned is that each input will exhibit some input offset voltage, which can be nulled as shown in Figure 6. Also, the differential output will exhibit some offset, which can be nulled as shown.

A brief set-up procedure is as follows:

SET-UP PROCEDURE (FIGURE 6)

1. Set $V_X = V_Y = 0$ and adjust differential output offset to zero.
2. Set V_X = 5.0 V, V_Y = 0.0 V and adjust V_Y-offset until output is zero.
3. Set V_Y = 5.0 V, V_X = 0.0 V and adjust V_X-offset until output is zero.
4. Repeat Step 1.
5. Set $V_X = V_Y$ = +5.000 V and adjust gain control until output is +2.500 V.
6. Set $V_X = V_Y$ = -5.000 V. If output error is appreciable, repeat steps 1 through 5.

When the multiplier is operated in a dc mode, the dc output at pins 2 and 14 will ride a large common-mode voltage (≈ +22 volts in this example). Some common-mode level translating circuits will be shown in the following section; however, the present circuit (Figure 6) can be operated in an ac mode where the output can be very effectively ac-coupled.

The output response exhibits a single pole characteristic, due to R_L and stray (or load) capacitance. In an operating condition where R_L = 5.6 kΩ the bandwidth capability of the multiplier is observed and illustrated in Figure 7. Here, one input is a constant 1-volt dc and the other is 1 V(rms). The output is 0.1 V(rms) out to 1 MHz, is 3 dB down at 4.5 MHz, and 10 dB at about 14 MHz. The frequency response curve exhibits a single pole characteristic, with the pole located about 4.5 MHz. At this frequency, their exists 45° of phase shift. Hence, the single-ended output can be expressed as

$$V_O = V_X V_Y \cos\theta, \qquad (34)$$

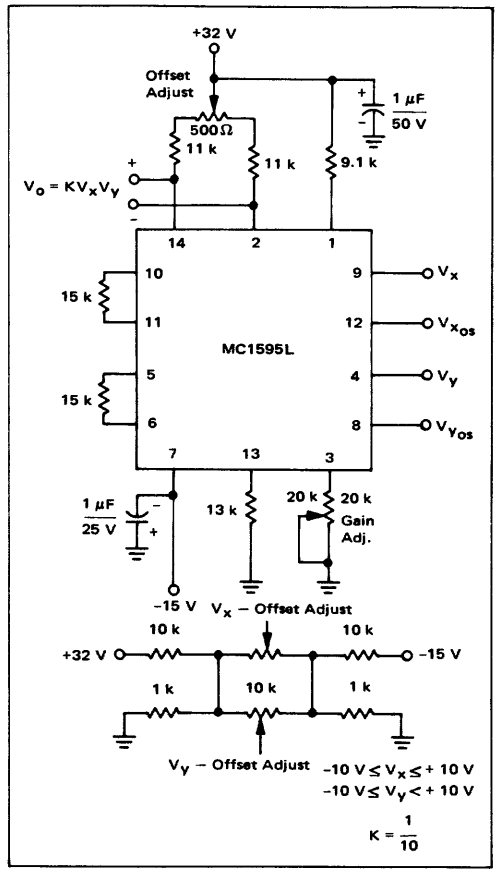


FIGURE 6 – Basic Multiply Circuit

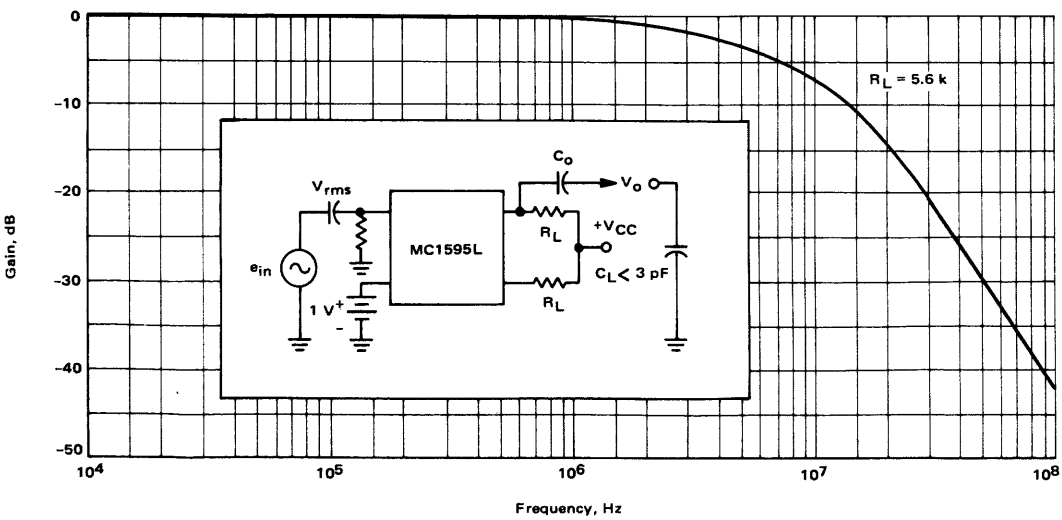


FIGURE 7 – Multiplier Bandwidth

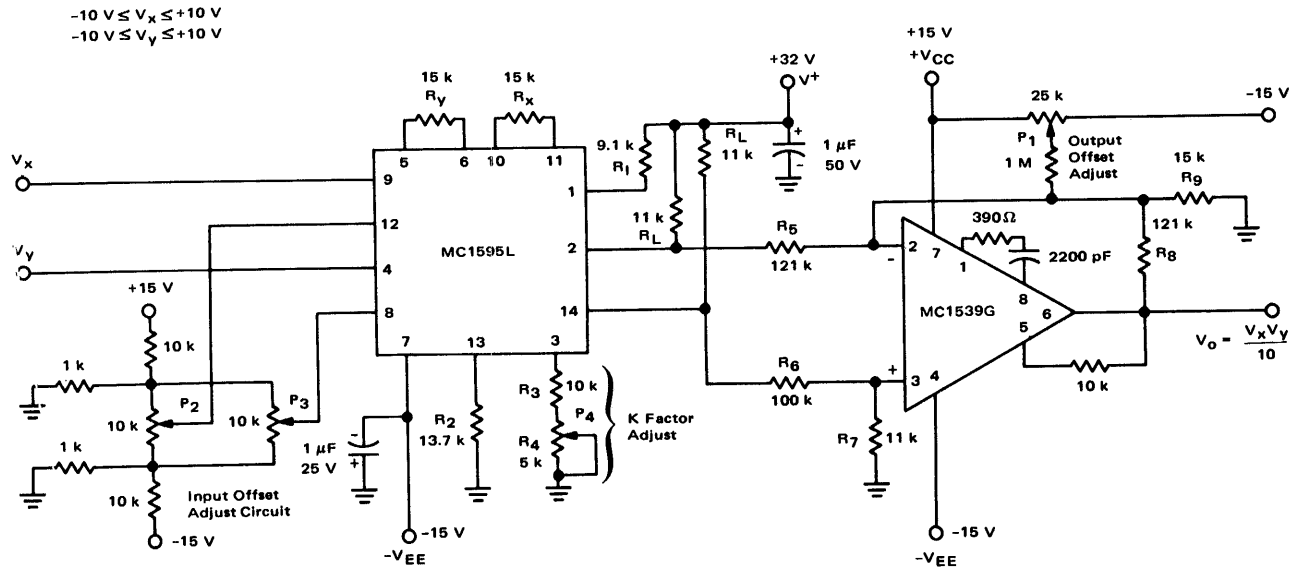


FIGURE 8 – Multiply with Op Amp Level Shift

where in Figure 7, V_X = +1.0 Vdc, V_y = 1.414 Cosωt, and θ is the relative phase shift observed due to roll-off. A 3° roll-off will cause the output to fall off by about 0.15%, which ideally occurs at each output, as can be visualized by representing Equation (34) in vector notation.

In the configuration of Figure 6, the common mode output is seen to be about +22 V. In many applications, it is desirable to level shift to a ground reference. One method of obtaining this is shown in Figure 8. Here the common-mode voltage is reduced by the 10-1 attenuation networks and the differential output voltage is fed into an operational amplifier, which can operate easily with +2 V common-mode, and whose closed loop gain is 10. The resulting output is still $\frac{V_X V_y}{10}$ which appears single ended about a ground reference. This circuit has the advantage of being rather simple and relatively insensitive to temperature. It has the disadvantage of being frequency limited to about 50 kHz for large signal swings (±10 V), due to the slew rate of the MC1539 operational amplifier. Another disadvantage of this configuration is the need for a third power supply.

Figure 9 uses discrete components to perform the level shifting making it very inexpensive, simple, and permits operation at higher frequencies (limited by the 7.5 kΩ resistor and stray capacitance associated with the output). The circuit of Figure 9 also has the added advantage of operating entirely from ±15 V supplies. This circuit has the disadvantage, however, of being somewhat temperature sensitive if the base emitter junctions of the NPN and the PNP (denoted by *) are not matched to track with temperature. This problem can be greatly reduced by using complementary pair transistors mounted in the same package such as the Motorola MD6100. A second problem with this level shifting circuit is that it has a high output impedance with little current drive capabilities. The problem can be solved by placing an operational amplifier connected as a source follower as shown in Figure 10.

Therefore, for dc operation over wide temperature extremes, the circuit shown in Figure 8 is preferred; for ac applications in which the input and output can be capacitively coupled, the circuit shown in Figure 9 is preferred.

Using the configuration of Figure 8, a general set-up procedure for this circuit is as follows:

SET-UP PROCEDURE (FIGURE 8)

1. Set V_X = V_y = 0 V. Adjust output offset potentiometer P_1 until the output reads zero volts.

TABLE I – Element Values for Figure 11

$V_x\|max$ $V_y\|max$ $V_{out}\|max$	R_x R_y	R_L	R_1	R_3*	R_{13}	V_{CC}	V_7	V_{CM}
±10 V	15 kΩ	11 kΩ	9.1 kΩ	13.7 kΩ	13.7 kΩ	+32 V	-15 V	+21 V
±5 V	8.2 kΩ	3.3 kΩ	3.9 kΩ	13.7 kΩ	13.7 kΩ	+15 V	-15 V	11.7 V

*Value given for R_3 is approximate – use potentiometer to adjust K factor exactly.

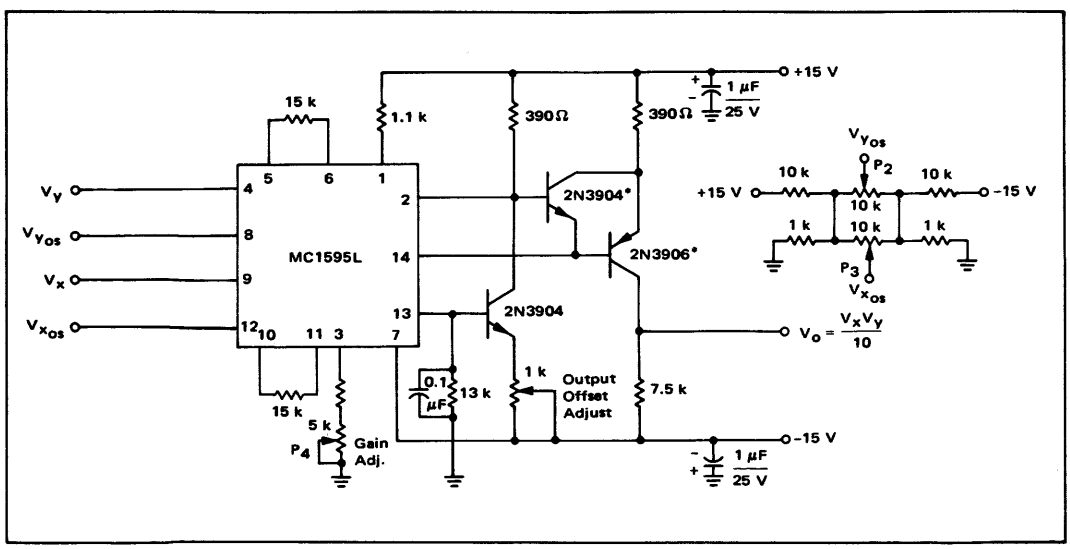


FIGURE 9 – Discrete Level Shifting Circuit

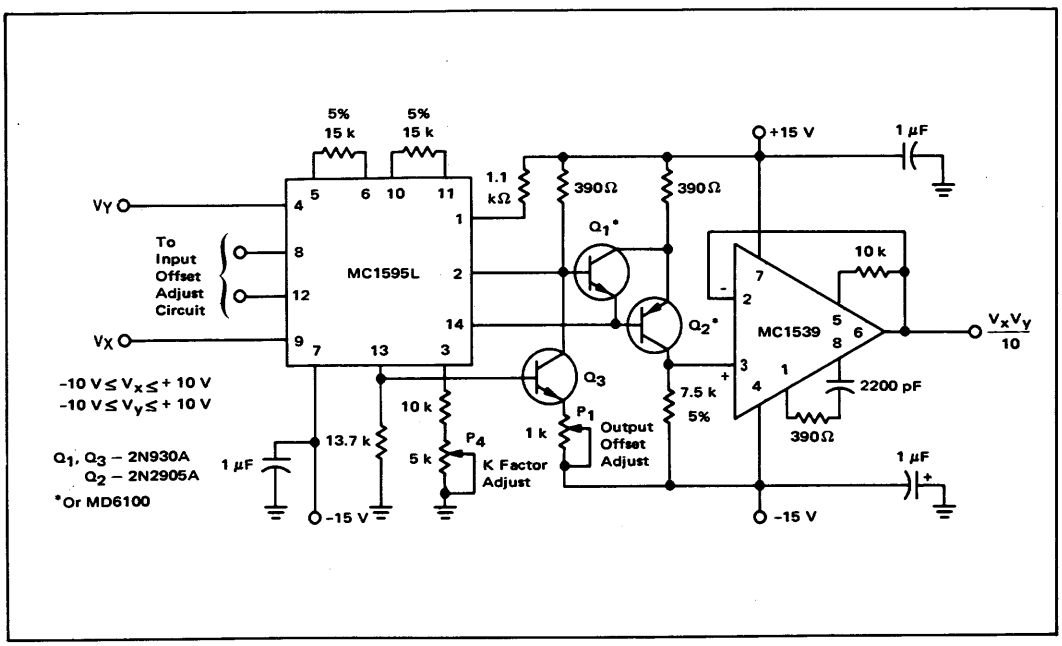


FIGURE 10 – Multiply with Discrete Level Shift

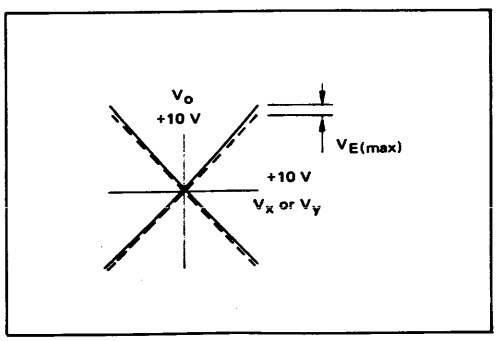


FIGURE 11 –

2. Set V_X = 5.000 V, V_Y = 0.000 V and adjust potentiometer P_3 until output reads zero volts.
3. Set V_Y = 5.000 V, V_X = 0.000 V and adjust the voltage at pin 9 (Potentiometer P_2) until output reads zero volts.
4. Repeat Step 1.
5. Set $V_X = V_Y$ = 5.000 V and adjust the gain potentiometer (P_4) until output reads -2.500 V.
6. Set $V_X = V_Y$ = -5.000 V and note the output. The output should again be -2.500 V. If the error is appreciable (greater than 1 or 2 percent), repeat steps 1 through 6.

To summarize the set-up process, the following equations are seen (Ref - Figure 5):

$$I_3 = \frac{-0.7\ V - (-V_{EE})}{R_3 + 500\ \Omega} \tag{35}$$

$$I_{13} = \frac{-0.7\ V - (-V_{EE})}{R_{13} + 500\ \Omega} \tag{36}$$

$$R_{CM} = \frac{+V_{CC} - V_{CM(pin\ 1)}}{2I_3}. \tag{37}$$

For the constraint (r_e is neglected):

$$I_{x(max)} \leq (2/3)\, I_{13}$$

$$I_{y(max)} \leq (2/3)\, I_3$$

$$R_X = \frac{V_{x(max)}}{I_{x(max)}} = \frac{V_{x(max)}}{(2/3)\, I_{13}} \tag{38}$$

$$R_Y = \frac{V_{y(max)}}{I_{y(max)}} = \frac{V_{y(max)}}{(2/3)\, I_3}. \tag{39}$$

$-V_{EE}$ is selected by knowing V_X and V_Y maximum negative values.

$+V_{CC}$ is selected knowing V_X, V_Y, R_L, and I_3, I_{13}.

SOURCES OF MULTIPLIER ERROR

A. The major source of error in the multiplier arises from voltage offsets and ohmic base resistances in the four output transistors and the base diodes. The static error adjustment procedure removes as much of this error as possible by offsetting the input differential amplifiers to compensate for the output unbalance.

B. A second and usually small source of error can arise from signal non-linearity in the x- and y-input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough that non-linear base-emitter voltage variation can be ignored.

C. Care must also be taken to avoid aging and temperature drift in the external components used with the multiplier. This is especially important in the level translation circuitry of Figures 9 and 10.

CHOICE OF CIRCUIT CONSTANTS

Typical element values and power supplies required to provide multiplier operation for two input and output ranges are shown in Table I. In this table, note that the value given for R_3 is approximate; it should be adjusted to set the I_3 which provides the exact gain (K-factor) desired. In some cases, it may be desirable to provide separate power supply regulation for I_3, since the multiplier gain is directly dependent on this current.

LINEARITY

Linearity is measured for V_X and V_Y separately using an x-y plotter with the circuit in Figure 5. It is defined to be the maximum deviation of output voltage from a straight line transfer function expressed as error in percent of full scale, see Figure 11. For example, if the maximum deviation, $V_{E(max)}$, is 100 mV and the full scale output is 10 V, then the error is

$$E_R = \frac{V_{E(max)}}{V_{o(max)}} \times 100$$

$$= \frac{100 \times 10^{-3}}{10\ V} \times 100$$

$$= 1\%$$

To measure this the x-y plotter is set up first to plot V_{out} versus V_X in all four quadrants ($V_Y = \pm 10$ V, $-10\ V \leq V_X \leq +10$ V) then V_{out} versus V_Y ($V_X = \pm 10$ V, $-10\ V \leq V_Y \leq +10$ V). The maximum deviations for x and for y are then determined as shown in Figure 11. It is desirable, but not necessary to zero out the multiplier static error before making this test.

SQUARING MODE ACCURACY

Squaring Mode Accuracy is defined as the maximum absolute deviation from a square law curve expressed as a percent of full scale output. This deviation may be measured by connecting the x and y inputs together (squaring mode) and plotting output versus input, $-10\ V \leq V_X = V_Y \leq +10$ V, using an x - y plotter. Before carrying out this test, the multiplier static error must be zeroed out.

POWER DISSIPATION

Because this circuit has no direct positive power supply connections, power dissipation, P_D, within the actual IC package should be calculated as the summation of the voltage-current products at each port (neglect base currents).

Under normal operating conditions, (Ref. to Figure 5), it is valid to assume:

$$I_2 = I_{14} = I_{13},\ I_1 = 2I_3,\ \text{and}\ V_2 = V_{14} \qquad (40)$$

then

$$P_D = 2\,(V_2 - V_7)\,I_{13} + 2\,(V_1 - V_7)\,I_3 + (V_{13} - V_7)\,I_{13} + (V_3 - V_7)\,I_3 \qquad (41)$$

for the circuit in Figure 11, this is

$$P_D \approx 2\,(36)\,(10^{-3}) + 2\,(29)\,(10^{-3}) + (1.2)\,(10^{-3}) + (1.2)\,(10^{-3})$$

$$\approx 133\ \text{mW}. \qquad (42)$$

BANDWIDTH AND PHASE

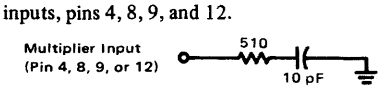
Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, small valued load resistors and/or a wideband op amp should be used.

Phase shift in the multiplier circuit results from two sources; phase shift common to both x and y channels (due to the pole at the multiplier output mentioned above), and relative phase shift between x and y channels (due to differences in transadmittance in the x and y channels). If the relative phase shift between channels is only two degrees, the output product of two sine waves will exhibit a maximum magnitude error of 3.5%, which is illustrated in Figure 12. A 2% error due to phase shift occurs at about 200 kHz in the MC1595, and a 3^{o} phase error bandwidth is specified typically as 750 kHz.

PARASITIC OSCILLATION

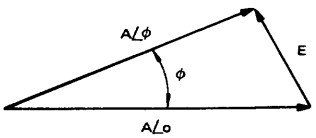
When long leads are used on the input, oscillation may occur. In this event, an R-C parasitic suppression network similar to the one shown below should be connected directly to each input using short leads. The purpose of the network is to reduce the Q of source-tuned circuits which cause the oscillation.

Another technique which is also adequate in most applications is to insert a 510 Ω resistor in series with the multiplier inputs, pins 4, 8, 9, and 12.



APPLICATIONS

The applications of a four-quadrant linear multiplier are almost limitless. Any control or instrumentation prob-



For ϕ small, $E \approx A \sin\phi \approx A\phi$

For $\phi = 2^o$, $\frac{E}{A} \approx 0.0349$

Hence the magnitude of the error vector for 2^o phase error is 3.49% relative.

FIGURE 12 – Relative Phase Error

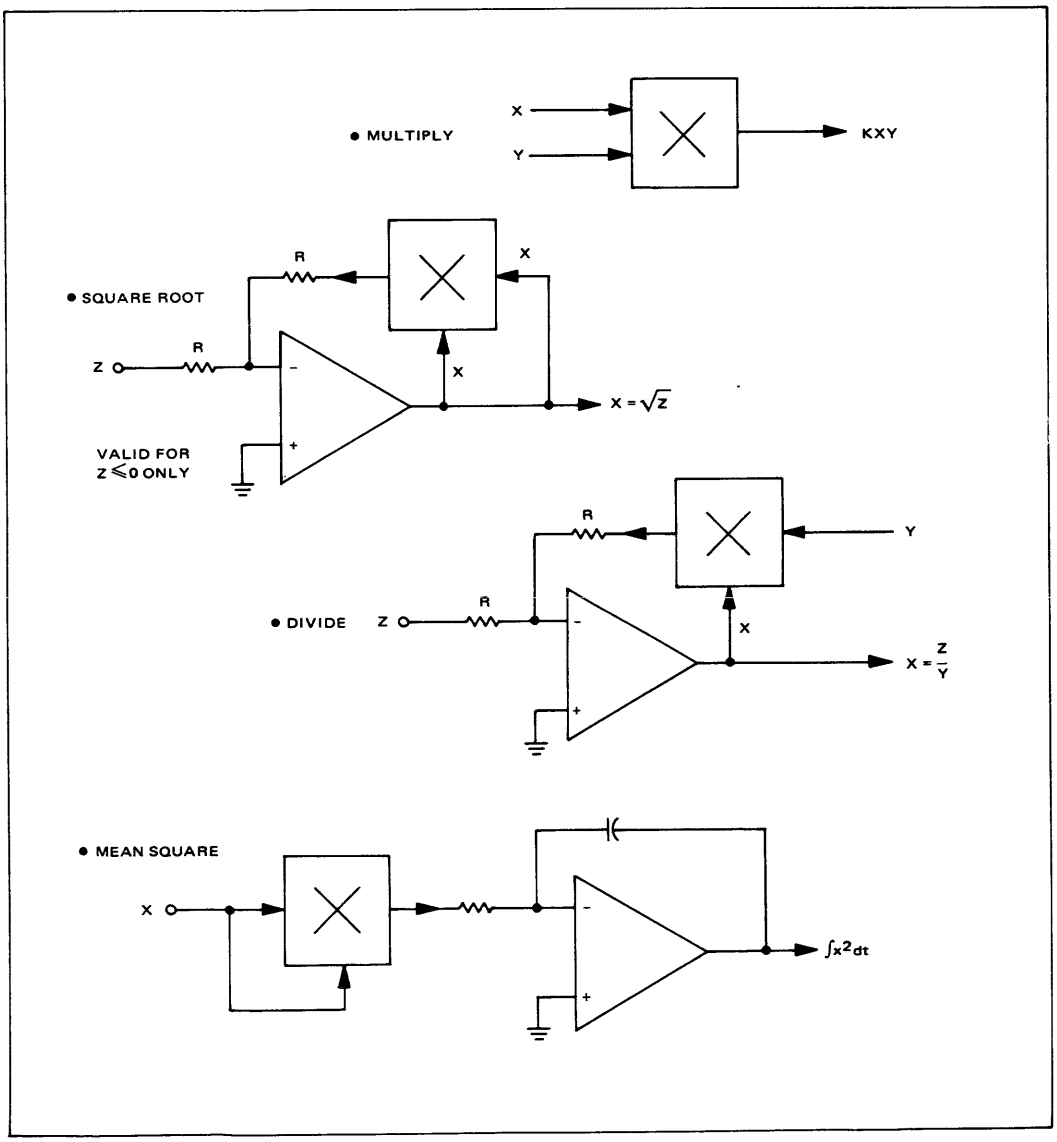


FIGURE 13 – Basic Multiplier Applications

lem requiring the product of two or more quantities is a potential application for the device. The following represents some of the more basic uses of the four-quadrant multiplier, from which more specific applications can be derived. Figure 13 illustrates four basic uses – that of multiplication, division, taking the square root, and obtaining the mean square. In the divide and square root applications, the multiplier is used as a feedback element around an operational amplifier in such a way that the multiplier output is forced to equal the magnitude of the -Z input. The circuit accuracy is somewhat worse in the divide and square root modes than in the multiply or square modes. For a multiply accuracy of 1% of full scale (this means that, if the maximum multiply output is ±10 V, an error of ±0.1 V is obtained regardless of input), the divide error can be several percent of full scale as the divisor decreases below a few volts.

Three additional applications are shown in block diagram form, in Figure 14. The frequency doubler operates on the principle that

$$(\text{Cos}\omega t)^2 = 1/2(1 + \text{Cos}2\omega t), \qquad (43)$$

which results in a dc offset and the doubled frequency signal. The linear phase detector operates on the principle that

$$K\text{Cos}\omega t\text{Cos}(\omega t+\phi)=\frac{K}{2}\text{Cos}(2\omega t+\phi)+\frac{K}{2}\text{Cos}\phi \qquad (44)$$

and with the insertion of a low-pass filter (LPF), the output Cosϕ is easily obtained. This differs from flip-flop phase detectors or sample-hold phase detectors in that these conventional phase detectors produce a voltage proportional to the phase difference, where the multiplier approach will produce a voltage proportional to the cosine of the phase difference. The roots or powers block diagram is relatively self-explanatory. The log and antilog functions can be obtained by taking advantage of the exponential relationships found in a transistor's base-emitter junction when used with an operational amplifiers.[2]

The applications illustrated very briefly in Figures 13 and 14, and others, will be discussed in detail in Parts II and III of this series of application notes.

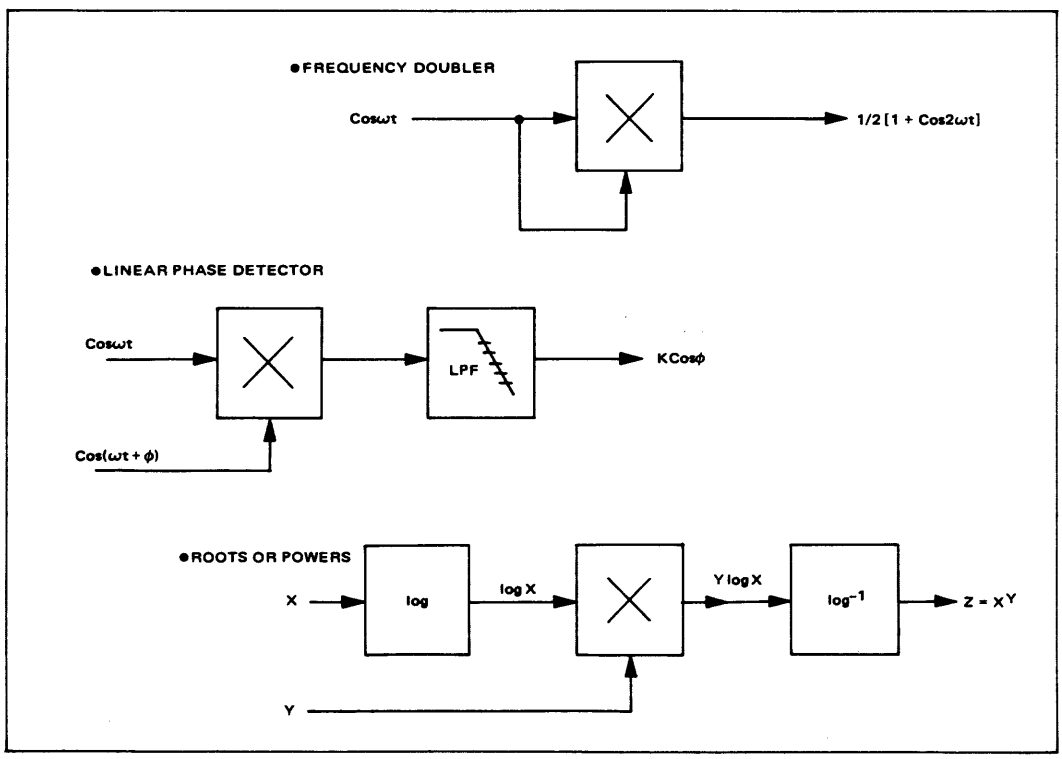


FIGURE 14 – More Basic Applications

ACKNOWLEDGMENT

The author wishes to acknowledge and thank Loren Kinsey for his outstanding evaluation efforts and many useful comments.

REFERENCES

1. EEE Special Survey: Packaged Analog Multipliers, EEE, November, 1968, pp. 80-94.
2. Transistor Logarithmic Conversion Using An Integrated Operational Amplifier, Motorola Application Note AN-261.
3. Solomon, James E., Recent Advances in Space Communications, Linear Integrated Circuits For Space Applications Series, Lecture 8, University of California Extension, Los Angeles, Summer, 1968.
4. Renschler, E. L., "A New Basic Building Block – The Linear Four-Quadrant Multiplier", Proceedings of the EEE Linear IC Clinic, New York City, March 24, 1969.
5. Renschler, E. L., "New Linear IC Building Blocks for Communications Applications", Proceedings of the 1969 EDN Seminar Series on Applications of Linear IC's, Los Angeles, February 11, 1969, Boston, March 4, 1969, and New York City, March 5, 1969.
6. Free, Maurice G., An Integrated Linear – Transconductance Analog Multiplier, a thesis for the degree of Master of Science in Electrical Engineering at the University of Arizona, Tucson, Arizona, 1969.
7. Gilbert, Barrie, "A Precise Four-Quadrant Multiplier with Subnanosecond Response", IEEE Journal of Solid-State Circuits, December 1968.
8. Renschler, E., "Theory and Application of a Linear Four-Quadrant Monolithic Multiplier", EEE Magazine, Vol. 17, No. 5, May 1969.

AN-490
USING THE MC1595 MULTIPLIER IN ARITHMETIC OPERATIONS

INTRODUCTION

The Motorola MC1595 four quadrant multiplier (see Figure 1) is the second basic building block that is now available to the analog systems designer. Any control or instrumentation problem which requires the product, square, square root or ratio of two analog quantities can be easily solved using the MC1595. Monitoring power, brake horsepower, fluid flow, solving of complex nonlinear equations (using analog computer techniques), frequency doubling, phase detection, dynamic gain control, taking roots or powers, modulation circuits, navigational problems, velocity, acceleration and distance for linear or nonlinear inputs, root mean square calculations, and generation of trigonemetric functions are only a few of the thousands of applications for this device.

This particular application note will be concerned with the use of the multiplier building block to perform a few of the basic arithmetic operations such as multiply, divide, square and square root. Using these techniques, the circuit designer can then model and construct very complicated systems using combinations of the above functions in conjunction with operational amplifiers which may be used to add or subtract.

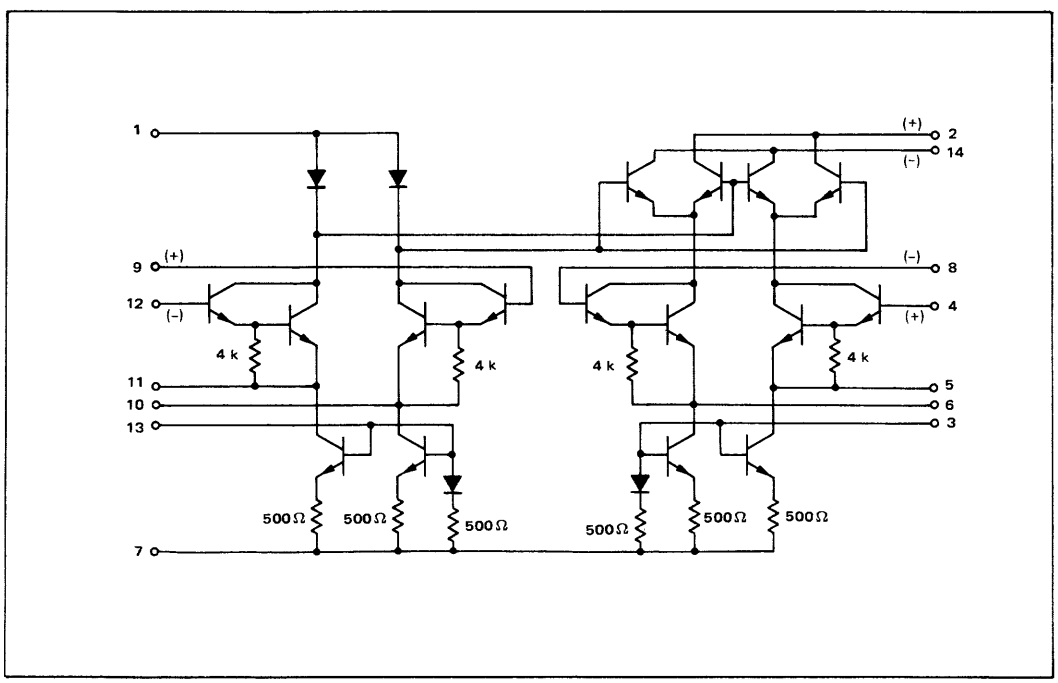


FIGURE 1 – MC1595L Four Quadrant Multiplier

THE MC1595 MULTIPLIER

A comprehensive discussion of the MC1595's circuitry and operation is found in Part 1 of this series (AN-489) and will not be further elaborated upon here. In that reference, it was shown that the MC1595 provided a differential output voltage, V_O, which is proportional to the product of the input voltages, V_X and V_Y. That is to say,

$$V_O = KV_XV_Y \quad (1)$$

where,

$$K = \frac{2R_L}{I_3R_XR_Y} \quad (2)$$

and R_L is the load resistor (pins 2 and 14)

I_3 is the current flowing into pin 3

R_X is the resistor between pins 10 and 11

R_Y is the resistor between pins 5 and 6.

Usually, K is set equal to 1/10; however, the constant K can easily be made equal to 1/20, 1/5, or any other fraction which is compatible with the other system constraints.

MULTIPLY

It was shown in Part 1 of this series that the output of the multiplier is a differential output which rides on a large common mode voltage. Hence, for most applications, the output of the multiplier must be level shifted and converted to a single-ended output. Two circuits that perform this function are shown in Figures 2 and 3. Figure 2 shows the use of an operational amplifier for level shifting. This circuit has the advantage of being rather simple and relatively temperature insensitive. It has the disadvantage of being frequency limited to about 50 kHz for large signal swings (±10 V). This is due to the slew rate of the operational amplifier.

Figure 3 uses discrete components to perform the level shifting which makes it very inexpensive, simple, and permits operation at higher frequencies (limited by the 7.5 kΩ resistor and stray capacitance associated with the output). The circuit of Figure 3 also has the added advantage of operating from ±15 volt supplies. This circuit has the disadvantage, however, of being somewhat temperature sensitive if the base-emitter junctions of the NPN and the PNP are not matched to track with temperature. This problem can be greatly reduced by using complementary-pair transistors mounted in the same package such as the MD6100. A second problem with this level shifting circuit is that it has a high output impedance with little current drive capability. The problem can be solved by placing an operational amplifier connected as a source follower at the output as shown in Figure 4. Therefore, for dc operation

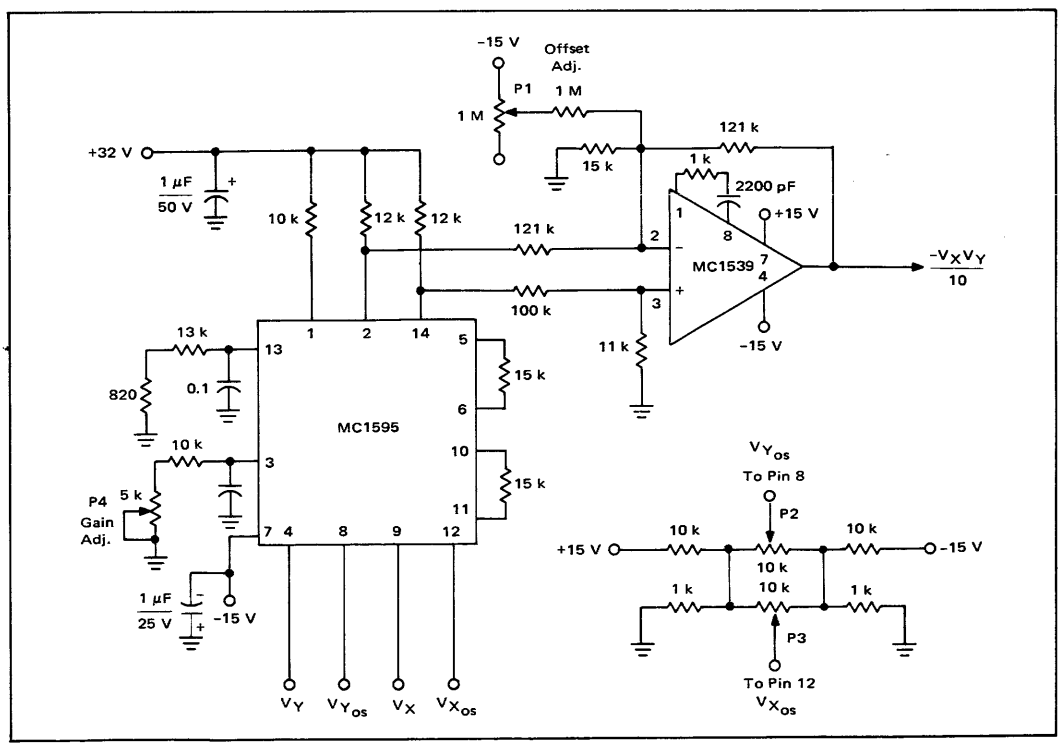


FIGURE 2 – Operational Amplifier Level Shifting Circuit

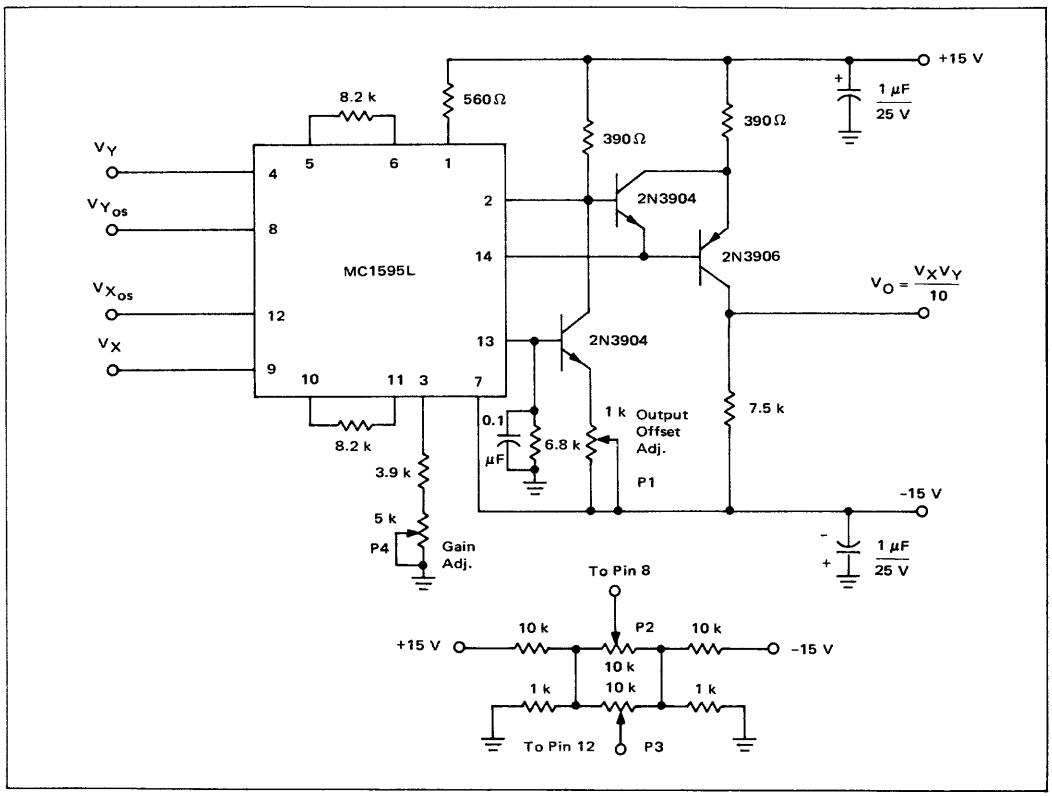


FIGURE 3 – Discrete Level Shifting Circuit

over wide temperature extremes, the circuit shown in Figure 2 is preferred. For ac applications in which the input and output can be capacitively coupled, the circuit shown in Figure 3 is preferred. For this application note, since the circuit functions are generally used in dc operation, the level shifting circuit shown in Figure 2 will be used in each case. A general set-up procedure for this circuit is as follows:

1. Set $V_X = V_Y = 0$ volts. Adjust offset pot P1 until the output reads zero volts.
2. Set $V_X = 5.000$ volts, $V_Y = 0.000$ volts and adjust potentiometer P2 until output reads zero volts.
3. Set $V_Y = 5.000$ volts, $V_X = 0.000$ volts and adjust the voltage at pin 12 (Pot P3) until output reads zero volts.
4. Repeat step 1.
5. Set $V_X = V_Y = 5.000$ volts and adjust the gain pot (P4) until output reads -2.5000 volts (K = 1/10).
6. Set $V_X = V_Y = -5.000$ volts and note the output. The output should again be -2.5000 volts. If the error is appreciable (greater than 1 or 2 percent), repeat steps 1 thru 6.

SQUARING CIRCUIT

Obviously, if the V_X and V_Y inputs are connected together in the basic multiplier circuit, the resulting output is given by:

$$V_O = KV^2 \tag{3}$$

where,

$$V_X = V_Y = V.$$

Hence, the output is proportional to the square of the input voltage. The proportionality constant is still given by:

$$K = \frac{2R_L}{I_3 R_X R_Y}. \tag{4}$$

The circuit which provides this function, with K = 1/10, is shown in Figure 5. The set-up procedure is exactly the same as that given for the basic multiplier circuit. Table I shows the measured results of the squaring circuit.

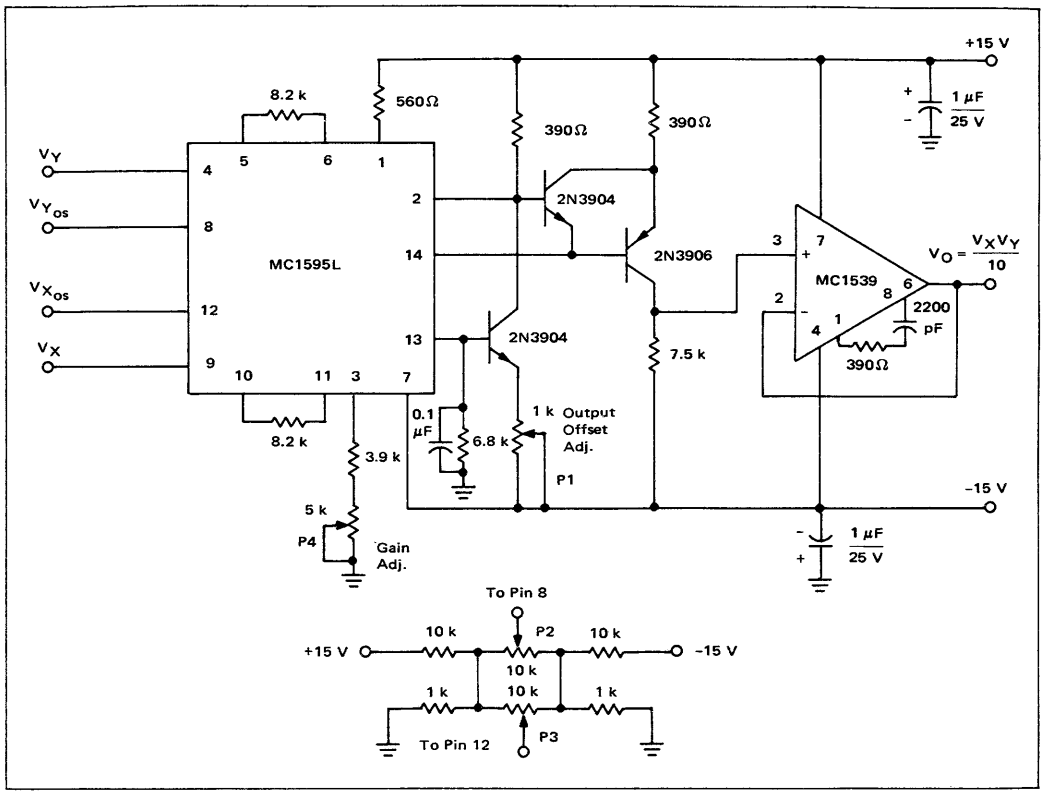


FIGURE 4 – Discrete Level Shifting Circuit with Source Follower Output

DIVIDE CIRCUIT

Consider the circuit shown in Figure 6 in which the multiplier is placed in the feedback path of an operational amplifier. For this configuration, the operational amplifier will try to maintain a "virtual ground" at the inverting (-) input. Assuming that the bias current of the operational amplifier is negligible, then $I_1 = I_2$ and

$$\frac{KV_XV_Y}{R1} = \frac{-V_Z}{R2}. \tag{5}$$

Solving for V_X,

$$V_X = \frac{-R1}{R2\,K}\,\frac{V_Z}{V_Y}. \tag{6}$$

If R1 = R2

$$V_X = \frac{-V_Z}{KV_Y} \tag{7}$$

If R1 = KR2

$$V_X = \frac{-V_Z}{V_Y} \tag{8}$$

Hence, the output voltage is the ratio of V_Z to V_Y and provides a divide function. This analysis is, of course, the ideal condition. If the multiplier error is taken into account, the output voltage is found to be

$$V_X = -\left[\frac{R1}{R2\,K}\right]\frac{V_Z}{V_Y} + \frac{\Delta E}{K V_Y}, \tag{9}$$

where ΔE is the error voltage at the output of the multiplier. From this equation, it is seen that divide accuracy is strongly dependent upon the accuracy at which the multiplier can be set, particularly at small values of V_Y. For example, assume that R1 = R2, and K = 1/10. For these conditions the output of the divide circuit is given by:

$$V_X = \frac{-10V_Z}{V_Y} + \frac{10\,\Delta E}{V_Y}. \tag{10}$$

From equation 10, it is seen that only when V_Y = 10 V is the error voltage of the divide circuit as low as the error of the multiply circuit. And when V_Y is small, say 0.1 volt, the error voltage of the divide circuit can be expected to be a hundred times the error of the basic multiplier circuit! In terms of percentage error,

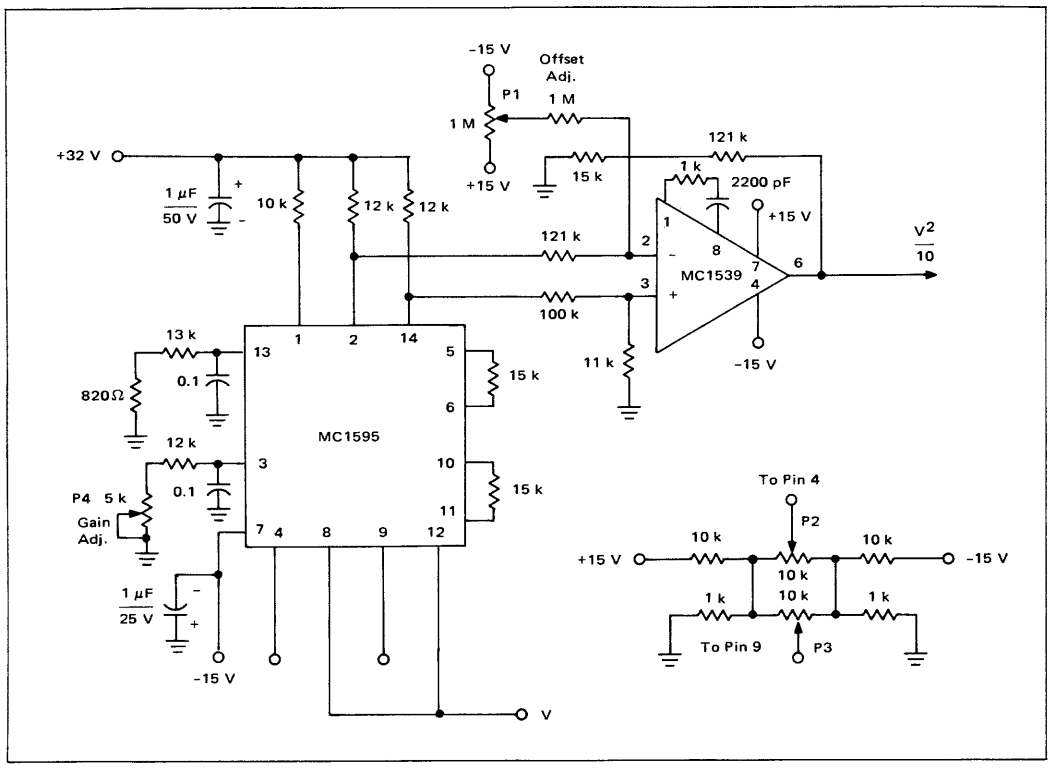


FIGURE 5 – Squaring Circuit

TABLE I – Squaring Circuit Results

V Volts	V_D Calculated	V_O Measured	% Error *
0	0.000	0.000	0
1	0.100	0.0994	0.6
2	0.400	0.3996	0.1
3	0.900	0.9002	0.022
4	1.600	1.601	0.063
5	2.500	2.503	0.12
6	3.600	3.602	0.055
7	4.900	4.905	0.1
8	6.400	6.408	0.125
9	8.100	8.105	0.062
10	10.000	10.051	0.51

*% Error is Relative – Not Full Scale.

$$\text{percentage error} = \frac{\text{error}}{\text{actual}} \times 100\% \qquad (11)$$

or from equation (9),

$$\text{P.E.}_D = \frac{\frac{\Delta E}{KV_Y}}{\left[\frac{R1}{R2\,K}\right]\frac{V_Z}{V_Y}} = \left[\frac{R2}{R1}\right]\frac{\Delta E}{V_Z}. \qquad (12)$$

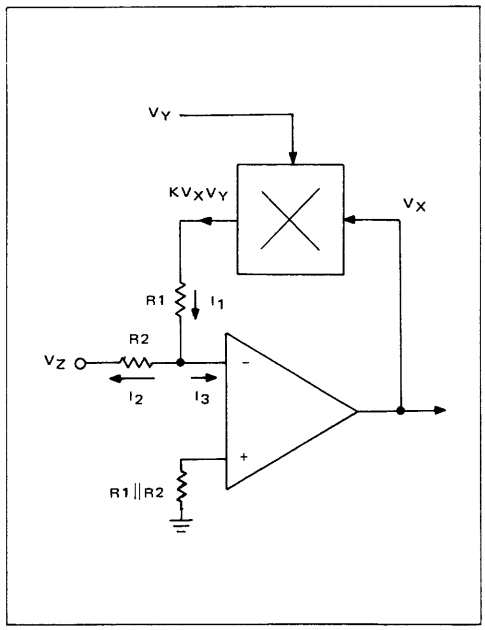


FIGURE 6 – Current Flow for Squaring and Square Root Circuit

From equation 12, the percentage error is inversely related to voltage V_Z (i.e., for increasing values of V_Z, the percentage error decreases).

A circuit that performs the divide function is shown in Figure 7. For this circuit,

$$\frac{R1}{R2} = K, \qquad (13)$$

and as a result, the output voltage is given by

$$V_O = \frac{-V_Z}{V_Y}. \qquad (14)$$

The adjustment procedure for this circuit is as follows:

1. Remove or disconnect amplifier A2 from the circuit and use adjustment procedure given in previous section for multiply operation.
2. Connect A2 into the circuit. Set V_Y = 10.000 V and V_Z = 0.000 volts (connect to ground). Adjust pot P1 to read zero volts at output (pin 12) of the MC1595).
3. Set $V_Y = V_Z$ = 10.000 volts and adjust gain pot P4 to give -1.000 volts at the output.

Table 2 shows the actual measured performance of this circuit.

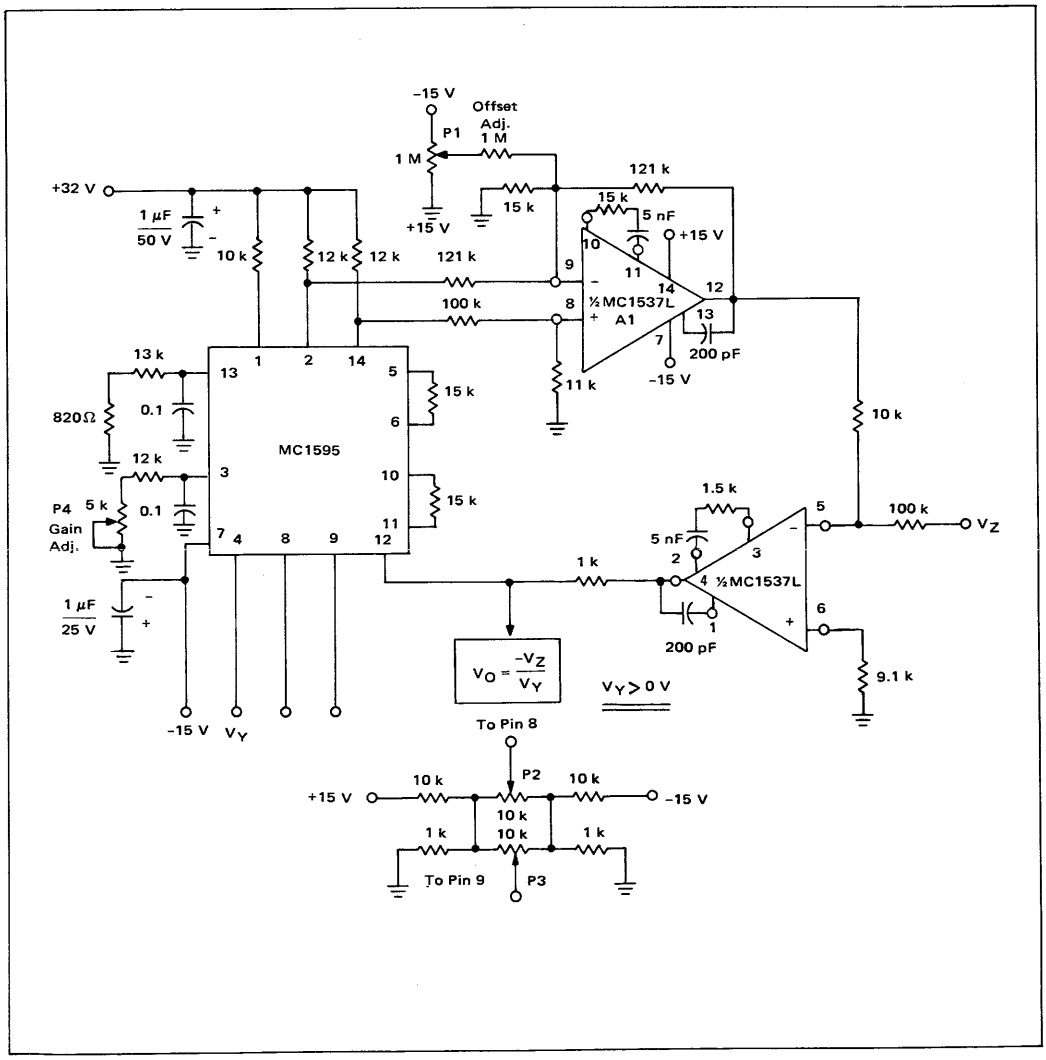


FIGURE 7 – Divide Circuit

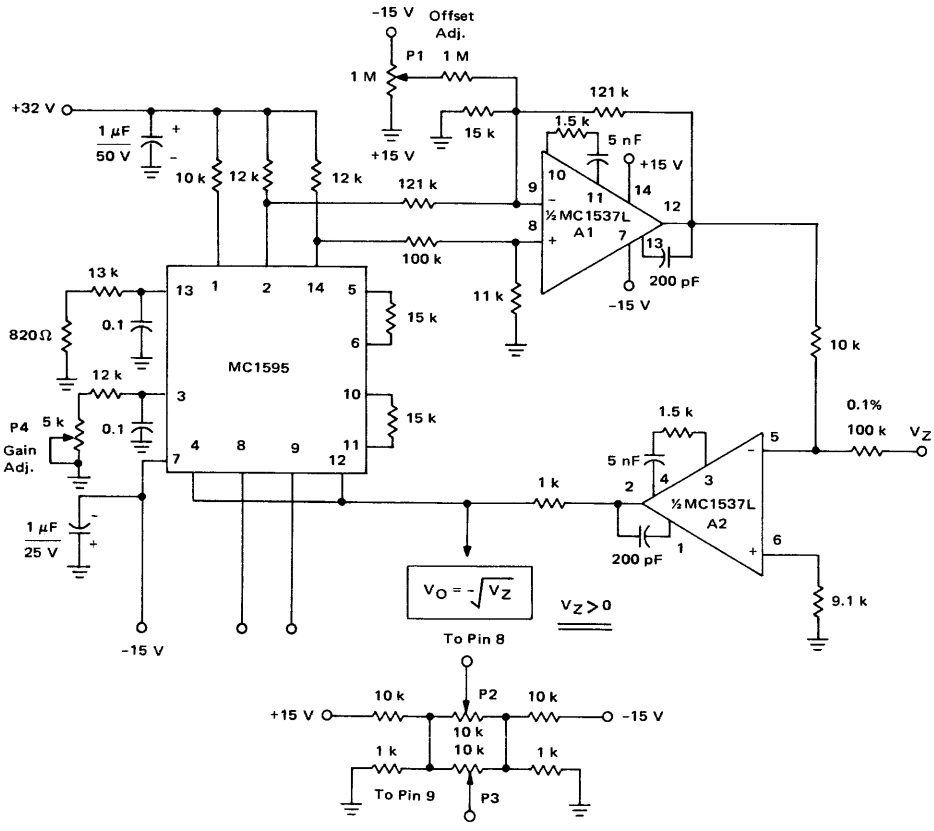


FIGURE 8 – Square Root Circuit

TABLE II – Divide Performance, V_Y = 8.000 Volts

V_Z Volts	V_O Calculated	V_O Measured	% Error*
1	0.125	0.141	13.6
2	0.250	0.266	6.4
4	0.500	0.517	3.4
8	1.000	1.019	1.9
10	1.250	1.270	1.6
12	1.500	1.521	1.4
16	2.000	2.023	1.15
20	2.500	2.526	1.04
24	3.000	3.031	1.04
32	4.000	4.042	1.05
40	5.000	5.060	1.20
64	8.000	8.090	1.12
80	10.000	10.120	1.2

*Note % Error is Relative Error – Not Referenced to Full Scale.

SQUARE ROOT

If in Figure 6, both the V_X and V_Y inputs are tied together, the result is

$$\frac{V_Z}{R2} = \frac{KV_X^2 + \Delta E}{R1} \qquad (15)$$

or

$$V_X = \sqrt{\frac{R1\,V_Z}{R2\,K} - \frac{\Delta E}{K}} \qquad (16)$$

where ΔE is again the multiplier error.

If R1 = R2

$$V_X = \sqrt{\frac{V_Z}{K} - \frac{\Delta E}{K}} \qquad (17)$$

and if $\frac{R1}{R2} = K$,

$$V_X = \sqrt{V_Z - \frac{\Delta E}{K}} \qquad (18)$$

Assume the ideal case for which $\Delta E = 0$, then,

$$V_X = \sqrt{V_Z} \qquad (19)$$

and the square root function is accomplished. Several points should be made concerning this circuit. First, with the op amp level shift (Figure 2), the output of the multiplier is given by:

$$V_O = \frac{-V_X V_Y}{10}. \qquad (20)$$

For the squaring circuit and the square root circuit, the output of the level shift op amp will be given by:

$$V_O = \frac{-V^2}{10}, \qquad (21)$$

where $V_X = V_Y = V$.

From Equation 21, regardless of the polarity of the input signal, V, the output of the level shift op amp will be negative. Using this information and referring to Figure 6, the obvious direction of current flow for I_1 and I_2 is actually reversed from that shown for these two circuits. This means that V_Z must always be positive. If it is required that V_Z be negative, pins 9 and 12 can be interchanged. However, operation at or around $V_Z = 0$ volts is not permitted for either connection (pin 9 and pin 12). Secondly, care must be taken to insure that pins 8 and 4 are not interchanged. This would cause positive feedback and the op amp circuit will latch to one of the supply voltages. Thirdly, the set-up procedure changes slightly due to the restriction that $V_Z = 0$. The set up procedure is as follows:

1. Remove or disconnect amplifier A2 from the circuit and use the adjustment procedure given in the multiply section.
2. Connect A2 into the circuit. Set $V_Z = 25.000$ volts and adjust the gain pot, P4, until the output reads -5.000 volts.
3. Set $V_Z = 1.000$ volts and adjust the offset adjust pot, P1, until the output reads -1.000 volt.
4. Repeat steps 2 and 3 until the desired accuracy is achieved.

From equation 18, the percentage error (P.E.) in the square root mode of operation is given by:

$$P.E._{SR} = \left[1 - \sqrt{1 - \frac{\Delta E}{KV_Z}}\right] X\,100 \qquad (22)$$

for $\frac{R1}{R2} = K$.

For K = 1/10, Equation (22) becomes

$$P.E._{SR} = \left[1 - \sqrt{1 - \frac{10\Delta E}{V_Z}}\right] X\,100. \qquad (23)$$

If $\frac{10\,\Delta E}{V_Z} << 1$, then the percentage error is given approximately by:

$$P.E._{SR} \approx \frac{10\,\Delta E}{2V_Z}\,X\,100 \qquad (24)$$

or, in the general case, for any K,

$$P.E._{SR} \approx \frac{R2\,\Delta E}{2R1\,V_Z} \qquad (25)$$

which is exactly half of the percentage error which was found for the divide circuit (Equation 12). The measured performance of the square root circuit is found in Table III.

TABLE III – Square Root Performance

V_Z Volts	V_O Calculated	V_O Measured	% Error*
1	1.000	0.924	7.6
2	1.414	1.371	3.1
4	2.000	1.966	1.7
8	2.828	2.800	1.0
16	4.000	3.982	0.45
25	5.000	4.993	0.14
36	6.000	6.008	0.13
49	7.000	7.028	0.40
64	8.000	8.058	0.73
81	9.000	9.098	1.1

*Note % Error is Relative Error – Not Referenced to Full Scale.

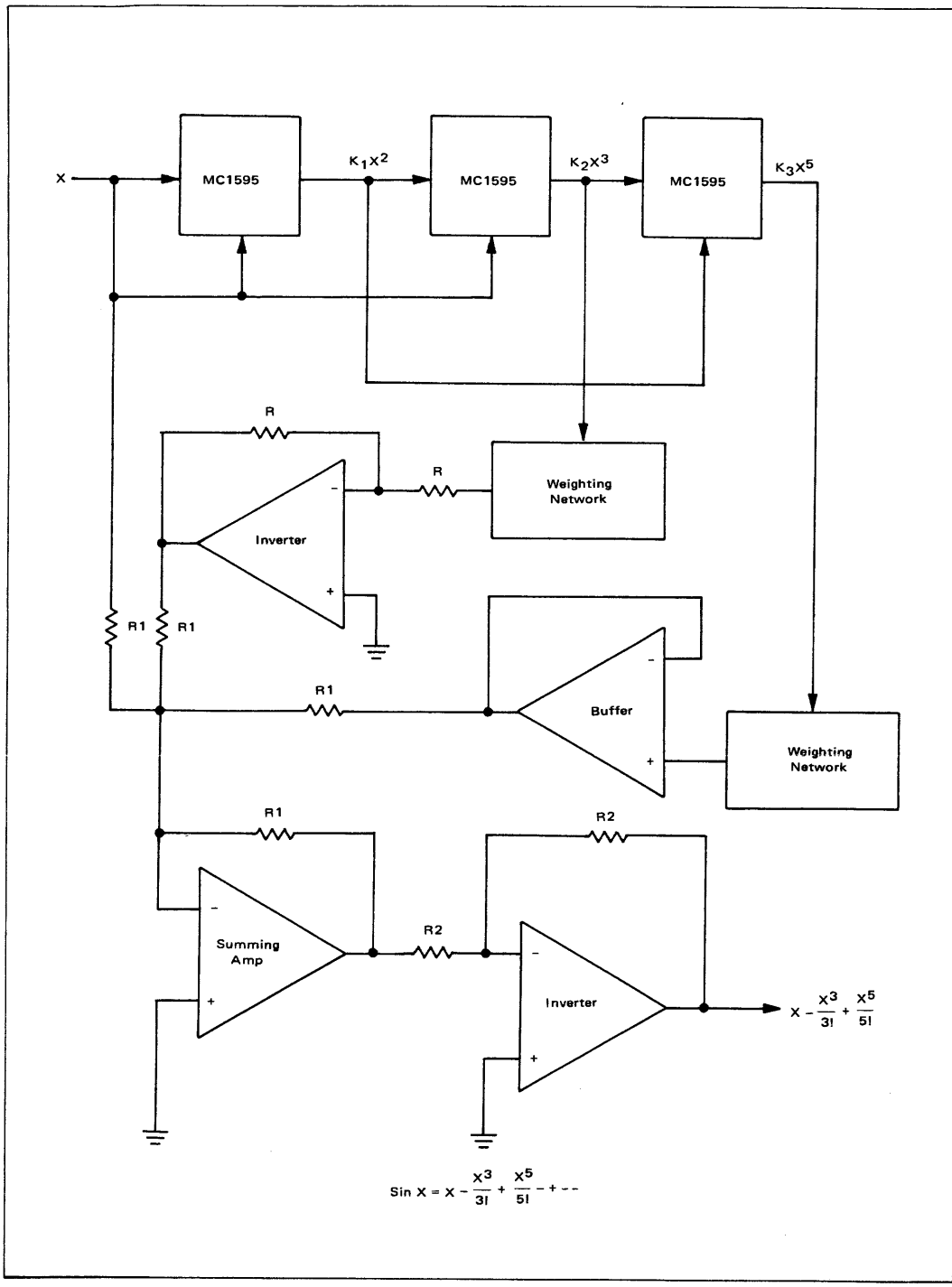


FIGURE 9 – Generation of Sin X (X≤ 1.6 Radians)

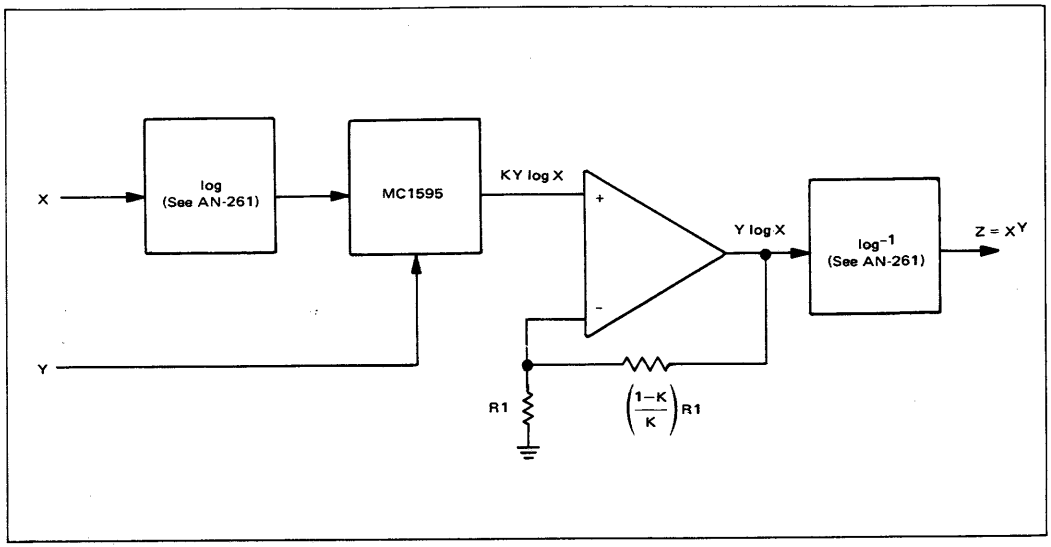


FIGURE 10 – Roots (|Y| < 1) or Powers (|Y| > 1) of X

SPECIAL CONSIDERATIONS

1. **Decoupling**

   Since this circuit is fabricated with VHF transistors, normal decoupling of power supplies is necessary.

2. **Oscillations**

   The first indication of the presence of oscillations is the inability to adjust the multiplier to better than 1% accuracy. If long line lengths are used at the inputs, Q-reducing networks may be necessary at the inputs to prevent parasitic oscillations. An effective technique is to place a 510 ohm resistor in series with each input (pins 4, 8, 9, and 12).

CONCLUSION

In this application note, the arithmetic operations of the MC1595 multiplier have been discussed. Obviously with various combinations of these basic circuits when used in conjunction with operational amplifiers to add and subtract, much larger systems can be constructed to solve problems directly. For example, the solutions to a second order equation; solutions to gas flow problems; pressure, volume, temperature (PVT) equations, generation of sine and cosine functions and many others.

Two examples of this are shown in Figures 9 and 10 where the MC1595 multiplier has been incorporated to generate the sine of X, and the roots or powers of X respectively.

AN-492

OPERATING CHARACTERISTICS OF THE MC3000/MC3100 SERIES TRANSISTOR-TRANSISTOR LOGIC GATES

INTRODUCTION

Transistor-transistor logic is rapidly becoming one of the most popular logic families in the industry today. Motorola now has available a series of MTTL III, MC3000 (0 to +75°C)/MC3100, -55 to +125°C integrated circuits designed with speeds approaching the limits of saturated logic along with good load driving capability. The Motorola MTTL III circuits, in addition to the many characteristics that have made transistor-transistor logic so popular, have several advantages over conventional TTL. A summary of the advantages are:

1. Superior transfer characteristics
2. Minimization of problems with overshoot or ringing (addition of input diodes)
3. Wide range of logic functions
4. Compatible with MDTL (Motorola Diode-Transistor Logic)
5. Low output impedance in "high" and "low" state
6. Less power dissipation versus frequency than conventional TTL.

Each of these important points will be discussed in detail.

TRANSFER CHARACTERISTICS

The first point to be discussed will be the superior transfer characteristic of the MC3000/MC3100 Series, beginning with the operation of conventional TTL.

CONVENTIONAL TTL

Applying a "low" to either A or B inputs of the gate shown in Figure 2, a base-to-emitter diode of transistor Q1 becomes forward biased. No base drive is available for transistor Q2 which turns OFF and causes transistor Q5 to turn OFF. The collector of Q2 rises toward the supply voltage, V_{CC}, and supplies base drive to turn ON transistor Q3, causing transistor Q4 to turn ON. Transistors Q3 and Q4 act as emitter-followers and this places the output, V_O, two V_{BE} drops below V_{CC} in its quiescent "high" state, or approximately 3.5 volts.

Consider the case where input A is "high" and input B begins to go from a "low" to a "high." Base drive is gradually applied to transistor Q2 which now starts to conduct with emitter current initially flowing through R4. As transistor Q2 turns ON, the collector current of Q2 produces a voltage drop across resistor R2. The collector of Q2 is connected to output V_O by means of the two emitter-follower transistors, Q3 and Q4, and therefore, the output V_O tracks the voltage at the collector of Q2. As the voltage at input B increases, the base of Q2 tracks voltage by the difference of $V_{BE} - V_{BC}$ of transistor Q1. The collector current through Q2 increases, causing a larger drop across resistor R2. The output, V_O, now changes at a rate of

$$\Delta V_B \frac{R_2}{R_4}$$

as shown in Figure 1, between points a and b on the transfer characteristic. When the emitter current of Q2 increases to the point where the drop across R4 equals one V_{BE}, transistor Q5 begins to conduct. Point b on the transfer characteristic has been reached. With a further increase in the voltage at input B, transistor Q5 saturates and point c on the transfer characteristic is reached. The collector of transistor Q2 now sits of V_{EB} of Q5 plus V_{CE} of Q2. This voltage is not positive enough to sustain operation of transistors Q3 and Q4, and these devices are OFF. The output is now in its quiescent "low" state of V_{CE} equal to approximately 0.2 volts.

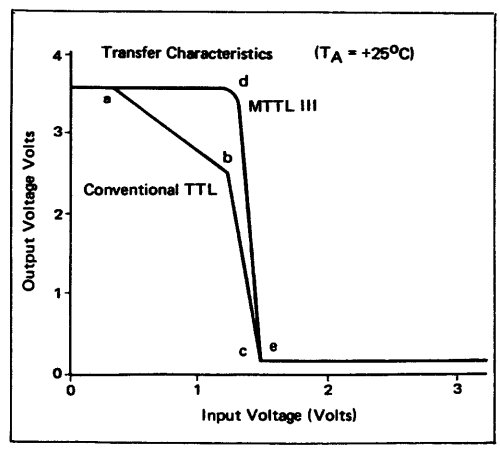


FIGURE 1 – Comparison of MTTL and MTTL III

MC3000/MC3100 MTTL III

One difference between MTTL III and conventional TTL is the replacement of resistor R4 in Figure 2 with resistors R4a and R4b and transistor Q6 in Figure 3.

With a "low" on either A or B, a base-to-emitter diode of transistor Q1 is forward-biased and no base drive is avail-

able for transistor Q2, which keeps Q2 OFF as well as transistors Q5 and Q6. The collector of transistor Q2 is approximately supply voltage V_{CC}, and base current is supplied to transistor Q3, keeping this device and Q4 ON.

Assume now that input A is "high" and input B gradually goes from a "low" to a "high." The base of transistor Q2 tracks the voltage at input B as in conventional TTL by the difference of $V_{BE} - V_{BC}$ of transistor Q1. At the point where transistor Q2 turns on in conventional TTL, transistor Q2 does not turn on in MTTL III, since the equivalent of an open circuit exists at its emitter. With no current flow, the collector of Q2 remains near the supply voltage, V_{CC}. Since transistors Q3 and Q4 act as emitter-followers, the output remains at the "high" level, approximately two V_{BE} drops below V_{CC}. The bypass network turns on when the potential at the base of Q2 is two V_{BE} drops above ground, causing the output transistor Q5 to turn on as well as bypass transistor Q6. This is point d on the Motorola MTTL III transfer characteristic (Figure 1).

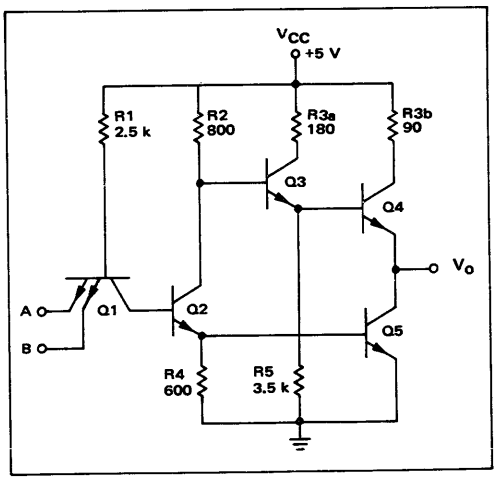


FIGURE 2 – Conventional High-Speed TTL Gate

As the potential on input B increases further, output transistor Q5 saturates and point e is reached on the MTTL III transfer characteristic. The resistors in the bypass network are chosen so that the network conducts the same current as resistor R4 in Figure 2 when transistor Q5 is saturated.

Due to the square shape of the transfer characteristic, dc noise immunity of the Motorola MC3000/MC3100 Series is improved considerably. The bypass network used to achieve the described transfer characteristic provides additional advantages over the simple resistor.

Figure 4 compares the variation with temperature of a standard monolithic resistor and the MTTL III bypass network impedance. As can be seen from this figure, there is a much smaller impedance variation with temperature in the MTTL III bypass network. Other advantages of the bypass network include:

1. When turning off, transistor Q6 turns off after transistor Q5. This provides faster turn-off at elevated temperatures of the output transistor because of lower bypass impedance.
2. Faster switching and lower power consumption resulting from a lower current spike during the turn-off transient at high temperatures.
3. A faster turn-on time at low temperatures.

ADDITION OF INPUT DIODES

Due to high speeds of operation, TTL generates large values of current and voltage rates of change. A 1 volt in approximately 1.3 nanoseconds for the rise time and a

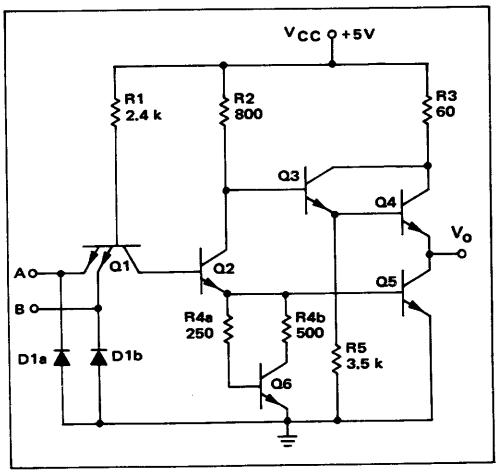


FIGURE 3 – Improved MTTL III Gate

1 volt change in approximately 1.0 nanoseconds for the fall time provides dV/dt rates on the order of 10^9 volts per second. With these rates of change, undershoot exceeding 2 volts can develop in the system which can cause two very serious problems. First, false triggering of the following stage is possible since a positive overshoot follows the large undershoot. This positive overshoot may act as a "high" signal and turn on the following stage for a short period of time. The diodes D1a and D1b on inputs

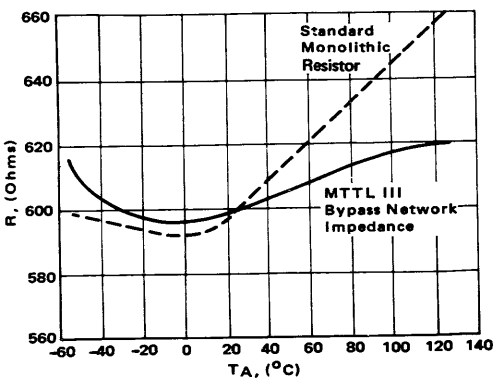


FIGURE 4 – MTTL III Bypass Network Impedance versus Temperature

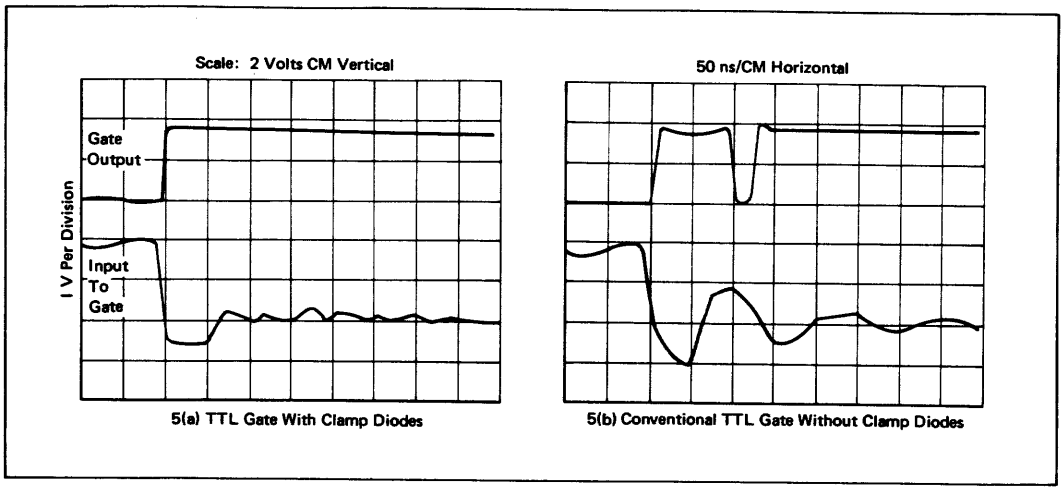


FIGURE 5 – Comparison of Waveforms with (a) and Without (b) Input Clamp Diodes

A and B, respectively, in Figure 3, limit the negative value of the undershoot, dissipating the ringing energy and thereby reducing the positive overshoot. Figure 5 shows the effect of adding the clamp diodes on inputs of TTL gates at the end of a 93 ohm line. In Figure 5b it can be seen that without clamp diodes, the positive overshoot has turned the following gate on momentarily. The second problem results if the unused inputs of a gate are returned to the supply voltage and a negative undershoot in excess of 2 volts occurs. These reversed-biased emitters may break down and draw excessive current, generating noise in the system.

ADDITIONAL GATES – AND GATE

The basic gate in the TTL logic family performs the NAND function. One of the many advantages in using MTTL III MC3000/MC3100 Series is the additional logic functions available in its series of gates. Figure 6 shows the AND gate function. The technique used to generate this function consists of adding the network composed of transistor Q7, diode D2, and resistor R6 to the basic NAND gate. With this network inserted between transistors Q1 and Q2, the voltage levels presented to transistor Q2 are the same as in the case of the NAND function, only inverted in phase. The inversion of the NAND function is, of course, the AND function. This additional inversion stage adds 3 nanoseconds propagation delay and around 6 mW power dissipation to the basic gate characteristics.

AND-OR-INVERT GATE

A limitation on TTL with its active pull-up circuit on the output is the prohibition of the wired-OR function.

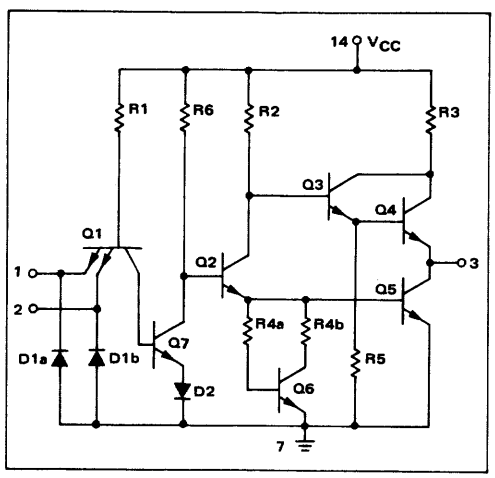


FIGURE 6 – MTTL Positive Logic AND Gate

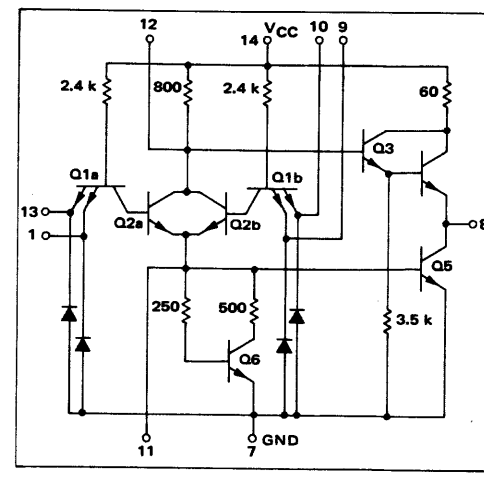


FIGURE 7 – MTTL III "AND-OR-INVERT" Gate Circuit

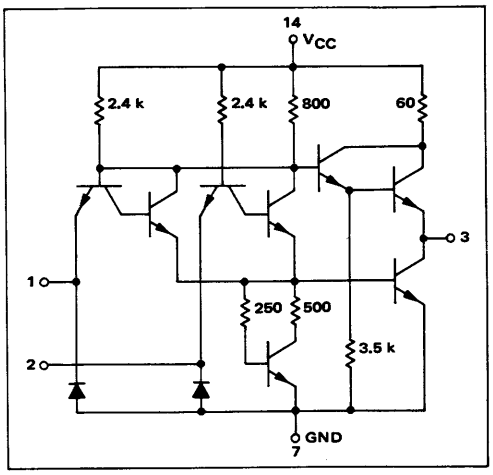


FIGURE 8 – MTTL III POSITIVE LOGIC "NOR" Gate Circuit

Motorola's MC3000/MC3100 Series offers the AND-OR-INVERT gate shown in Figure 7. This gate incorporates two 2-input AND functions (transistors Q1A and Q1B) and two inverters (transistors Q2A and Q2B). The inverter transistors (Q2A and Q2B) operate in parallel and perform the OR and INVERT functions. With "highs" on both of the inputs to either Q1A and Q1B, either Q2A or Q2B is ON thus causing transistor Q5 to be ON with the output being "low." With "highs" on all inputs, both transistors Q2A and Q2B are ON again causing transistor Q5 to be ON and the output is "low." With "lows" on both emitter inputs to transistors Q1A and Q1B, both transistors will be OFF thus causing transistors Q3 and Q4 to be ON and the output high.

NOR GATES

The NOR function is available by a slight modification to the AND-OR-INVERT gate just discussed. If one emitter is removed from each of the input transistors, Q1a and Q1b of Figure 7, we have a gate which performs the NOR function (Figure 8).

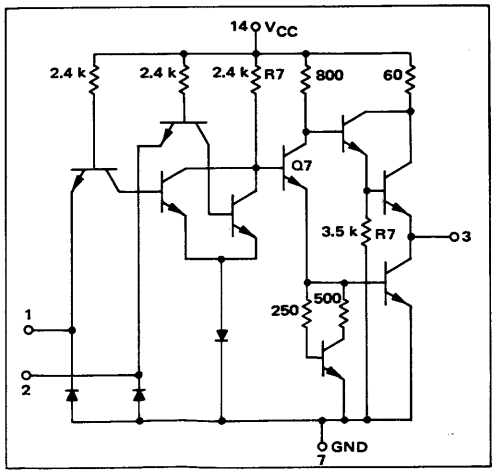


FIGURE 9 – MTTL III Positive Logic "OR" Gate Circuit

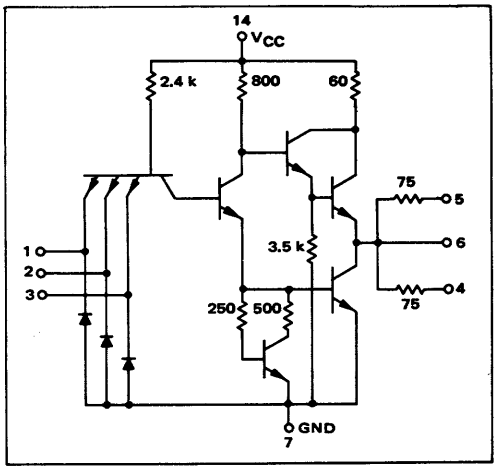


FIGURE 10 – MTTL III Terminated Line Driver (NAND)

OR GATES

By the addition of a transistor and a resistor to the NOR gate, the OR function can be performed. Figure 9 is the same as the NOR gate of Figure 8 with the addition of transistor Q7 and resistor R7 to perform the necessary phase inversion for the OR function.

LINE DRIVERS

Using an unterminated line driver, a line appears essentially as an open circuit at each end. Any pulse traveling down the line will see a reflection almost equal in magnitude to the original pulse. By terminating at the loaded end, reflections are minimized.

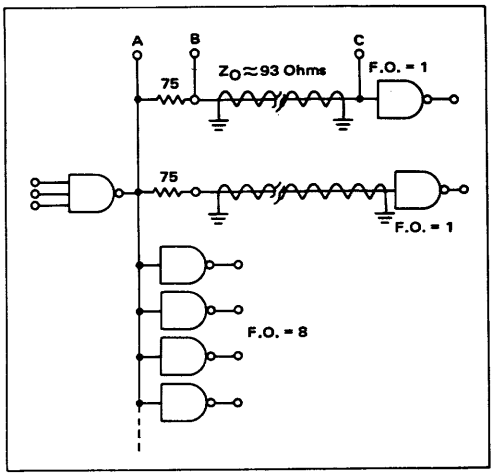


FIGURE 11 – Typical Application of the Line Driver

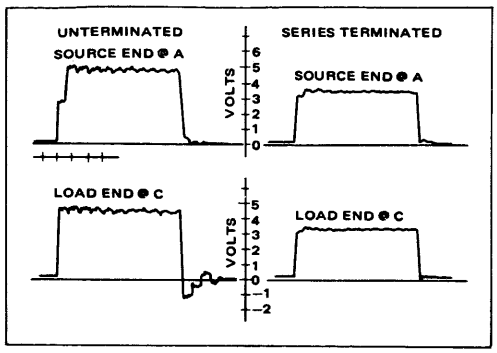


FIGURE 12 – Effects Of Series Termination With A MTTL III Gate Driving a 93-Ohm Line

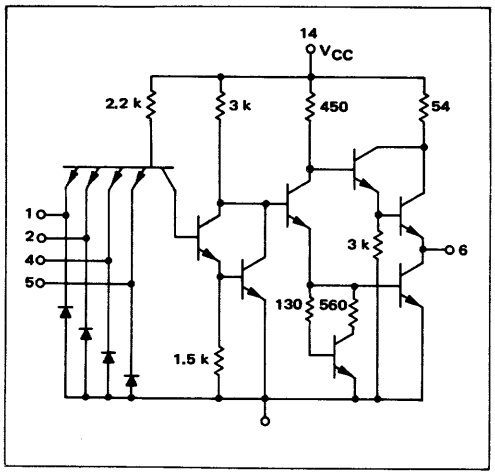


FIGURE 13 – MTTL III Power Gate Circuit (AND)

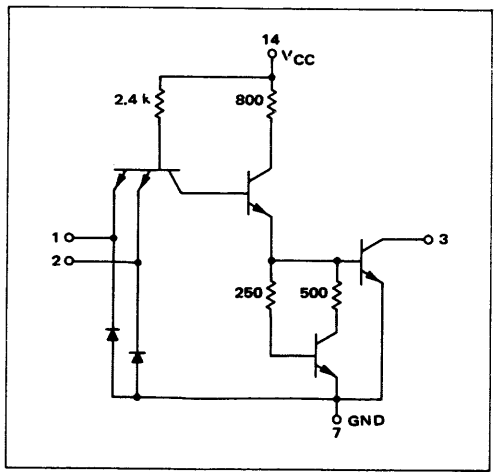


FIGURE 14 – Open Collector Gate For Implementing the "Wired OR" Function

To minimize switching transients on long lines, the MTTL III family includes a pair of series-terminated gates. Each of these gates has three outputs. Two of the outputs have 75-ohm resistors in series with the standard output node, and one connected directly to the node. For driving 93-ohm coax or 120-ohm twisted pair, a good match can be made at the output of each resistor. For loads of 50 to 93 ohms, the two resistive outputs are shorted together for better impedance matching. The non-resistive output can be used to drive gates in a normal fashion.

Figure 10 shows the circuit of the NAND line driver. Figure 11 shows a typical application of this circuit and Figure 12 demonstrates the effects of the better impedance matching of series termination gained at the expense of some loss of noise immunity.

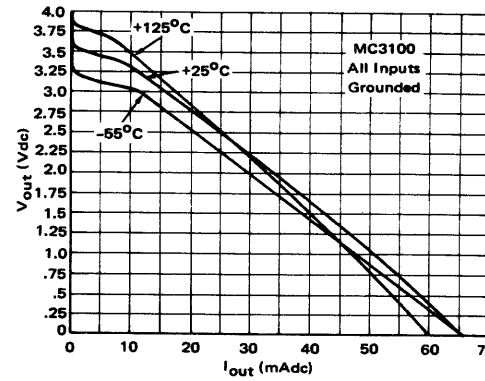


FIGURE 15 – Output Current versus Output Voltage

POWER GATES

Standard MTTL III gates offer good load driving capability and high fan-out. In some systems, however, there are a few requirements that exceed the capability of a standard gate. The MTTL III power gates are designed to meet these requirements with a minimum of additional circuitry. Available in both NAND and AND functions, the power gates feature output circuitry designed to provide twice the fan-out of conventional gates – 20 standard gate loads instead of 10. Figure 13 shows the MTTL III AND Power Gate.

OPEN COLLECTOR GATES

The standard MTTL III gates with the active pull-up circuit on the output prohibit the wired-OR function. To overcome this difficulty, the MTTL III Series has gates with no output pull-up circuit. The MTTL III open-collector NAND gate of Figure 14 is designed for use where the wired-OR function is required or for driving discrete components.

MDTL COMPATIBLE

The MC3000/MC3100 Series of transistor-transistor logic is pin compatible with the MDTL (Motorola Diode-Transistor Logic) family. Supply voltage is applied to pin 14, and ground is applied to pin 7 in both families. Because of its "square" transfer characteristic, the MTTL III family is the only TTL line that has a DTL type transfer

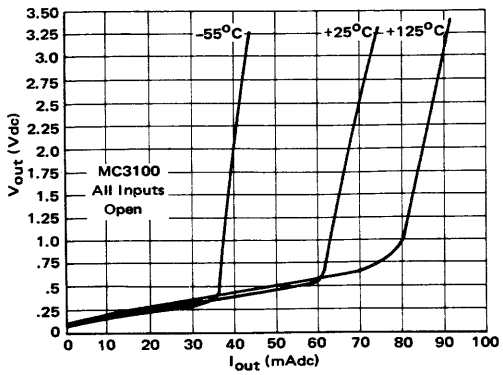


FIGURE 16 – Output Current versus Output Voltage

function. This is an additional feature to consider when updating present systems so that the faster switching times of TTL can be utilized.

LOW STATE OUTPUT IMPEDANCE IN "HIGH" AND "LOW" STATE

The Darlington output configuration provides extremely low output impedance in the "high" state. The low impedance results in excellent noise immunity and allows high-speed operation while driving large capacitive loads. Figure 15 shows the "high" state output impedance under the condition that all inputs are grounded. Calculating the resistance at room temperature from the slope of the curve a value of 10 ohms is found at 3.5 volts ranging up to 64 ohms at lower voltage levels.

Figure 16 illustrates the "low" state output impedance under the condition that all inputs are left open or returned to the supply voltage, V_{CC}. Again calculating the resistance at room temperature from the slope of the curve, a value of 6.0 ohms is found at $-V_{out}$ of 0.2 volts, ranging up to 480 ohms at voltages greater than 0.5 volts.

Under normal operating conditions the "high" state value of resistance would be 10 ohms at 3.5 volts and the "low" state value would be 6.0 ohms at 0.2 volts.

POWER DISSIPATION

One disadvantage of the TTL "totem pole" output is that both output transistors are ON during a portion of the switching time. Since the turn-off time of a transistor is normally greater than the turn-on time, the following occurs (refer to Figure 2).

In going from a "high" state to a "low" state on the output, transistor Q4 is initailly ON and is in the process of turning OFF. Transistor Q5 at the same instant in time is off and is attempting to turn on. Transistor Q5 turns ON before transistor Q4 can turn OFF. The result is a current spike through both transistors and the load resistor. The same effect takes place when the conditions are reversed and transistor Q4 turns ON before transistor Q5 can turn OFF. The active bypass network in the MC3000/MC3100 Series, shown in Figure 3, helps to limit this problem. As mentioned in the section ON Transfer Characteristics, the bypass network provides faster turn-off times. Figure 17 shows the power dissipation versus frequency for the MC3000/MC3100 quad 2-input NAND gate. The power dissipation per gate would be the values indicated divided by four. From Figure 17 we find that power dissipation increases at the rate of 0.4 mW/MHz for a single MC3000/MC3100 NAND gate, as opposed to an increase of 0.7 mW/MHz for a single gate in other high-frequency TTL families.

TYPICAL DATA

The following set of curves represents the typical operating characteristics of the MC3000/MC3100 quad 2-input NAND gate.

Samples of the device were chosen from dc data, and typical units were tested as a function of fanout, capacitive loading, temperature, and power supply variations.

The following curves were plotted from the data:

A. Transfer Characteristics
   V_{in} versus V_{out} for F.O. = 0, 1, and 10 @ T_A = -55°C, +25°C, + 125°C (Figures 18, 19, and 20).

B. Rise and Fall Times
   t_r versus C_T for F.O. = 1 and 10 @ -55, +25, and +125°C (Figure 21)
   t_f versus C_T for F.O. = 1 and 10 @ -55, +25°, and +125°C (Figure 22)
   t_r versus temperature for F.O. = 1 and 10 @ C_T = 25, 33, and 100 pF (Figure 23)
   t_f versus temperature for F.O. = 1 and 10 @ C_T = 25, 33, and 100 pF (Figure 24)

C. Propagation Delays
   t_{pd1}, t_{pd0} versus temperature, for F.O. = 1 and 10 @ C_T of 25, 33, and 100 pF (Figures 25 and 26)
   t_{pd1}, t_{pd0} versus C_T = 25, to 100 pF, F.O. = 1, 10 @ -55, +25, and +125°C (Figures 27 and 28)
   t_{pd1}, t_{pd0} versus V_{CC} for F.O. = 1 and 10 @ C_T = 25, 33 and 100 pF at 25°C (Figures 29 and 30)

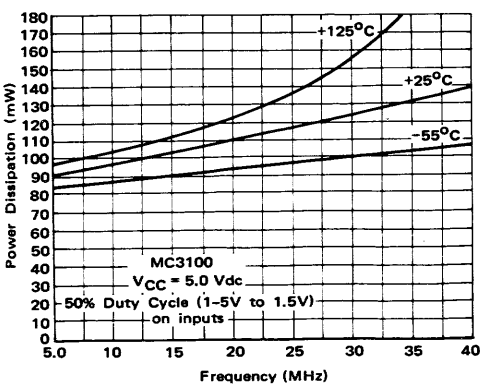


FIGURE 17 – Power Dissipation versus Frequency

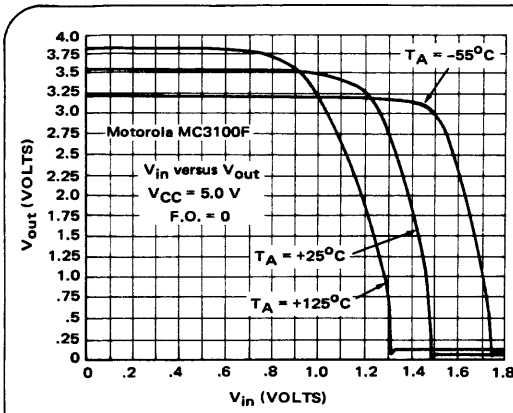


FIGURE 18 – TTL Transfer Characteristics

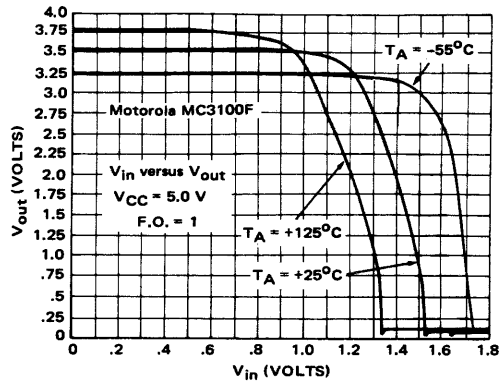


FIGURE 19 – TTL Transfer Characteristics

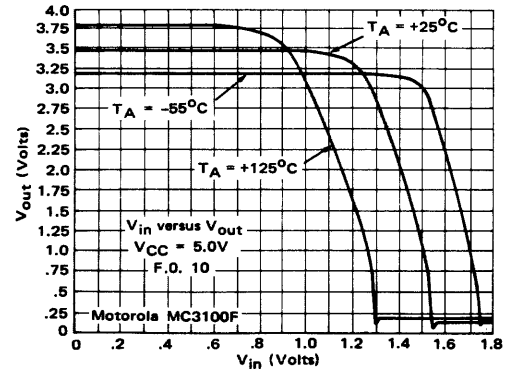


FIGURE 20 – TTL Transfer Characteristics

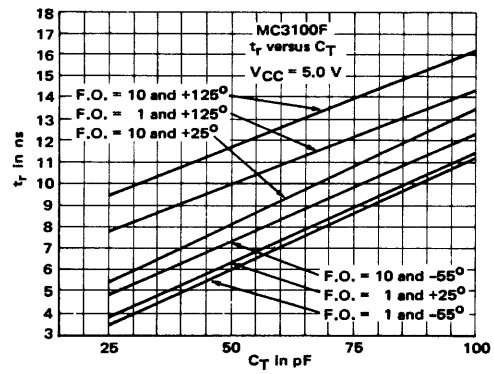


FIGURE 21 – Rise Time versus Capacitance

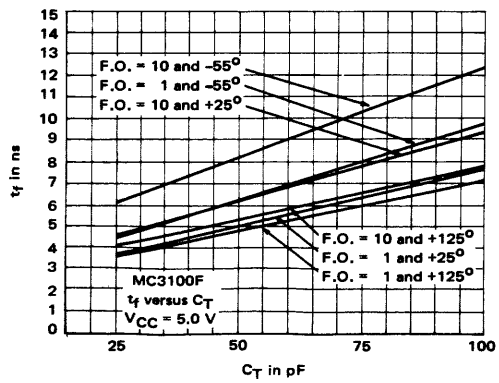


FIGURE 22 – Fall Time versus Capacitance

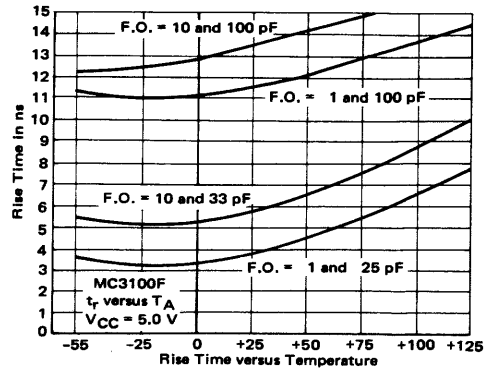


FIGURE 23 – Rise Time versus Temperature

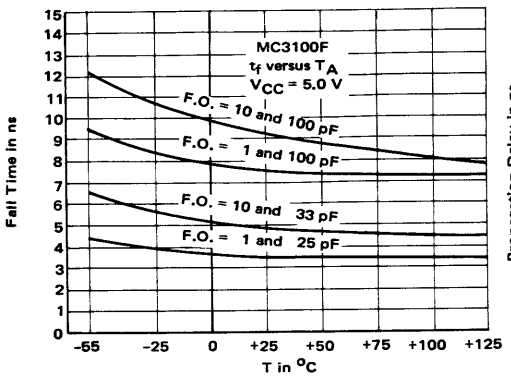


FIGURE 24 – Fall Time versus Temperature

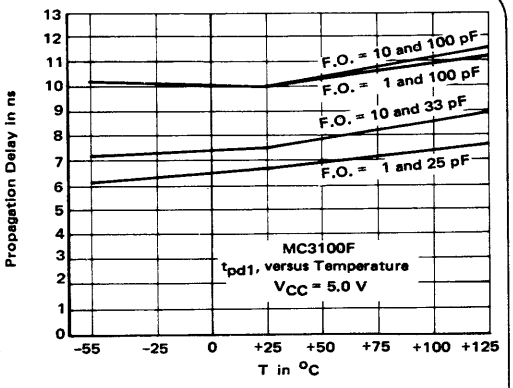


FIGURE 25 – Propagation Delay versus Temperature

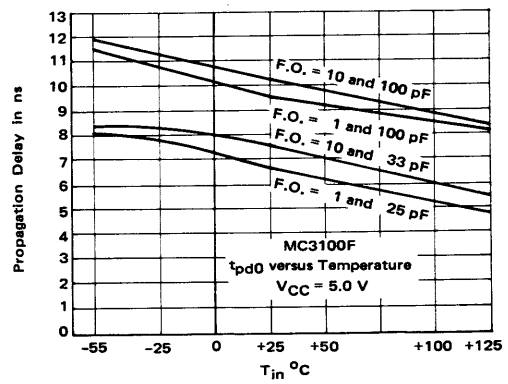


FIGURE 26 – Propagation Delay versus Temperature

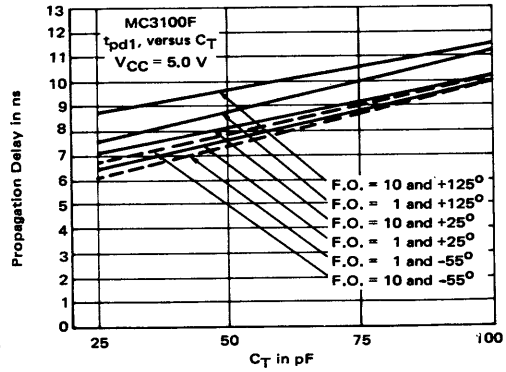


FIGURE 27 – Propagation Delay versus Capacitance

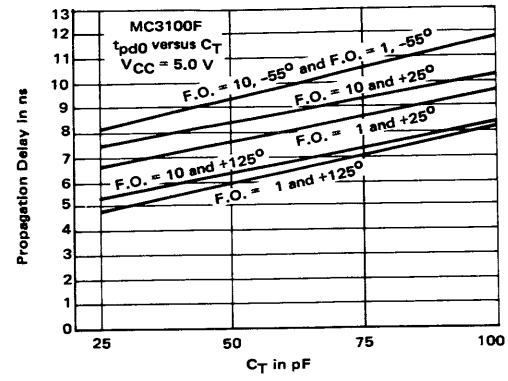


FIGURE 28 – Propagation Delay versus Capacitance

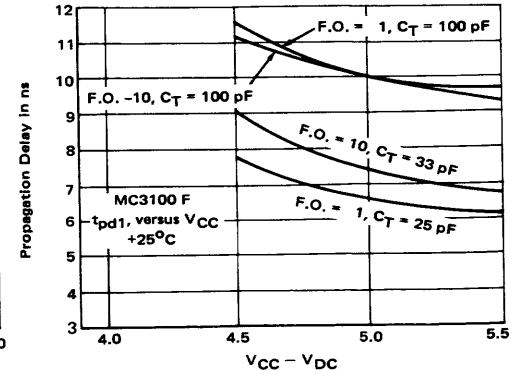


FIGURE 29 – Propagation Delay versus Voltage

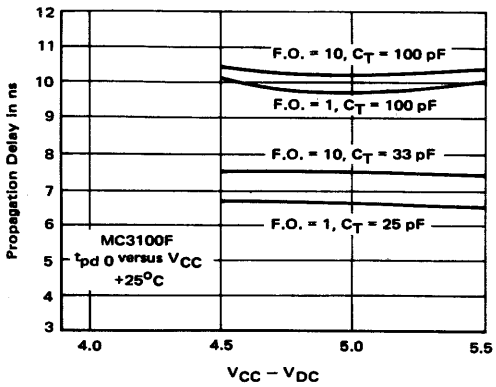


FIGURE 30 – Propagation Delay versus Voltage

Using these curves, a design engineer should be able to determine typical operating characteristics under almost any set of conditions. While these curves are for the MC3000/MC3100 Series quad 2-input NAND gate, this data could be used with good approximations to other gates with appropriate corrections as called out in the text of this application note. Table 1 lists the gates that are discussed in this application note.

SUMMARY

This application note has explained the advantages of using the MC3000/MC3100 Series transistor-transistor logic gates over other conventional lines available in the industry today. The design data that has been included should allow determination of operating characteristics under almost any set of conditions.

DEFINITIONS

C_T	Total parasitic capacitance, which include probe, wiring, and load capacitance
t_+	Voltage rise time
t_-	Voltage fall time
V_{CB}	Collector base voltage
$t_{pd\,1}$	Turn-off delay time
$t_{pd\,0}$	Turn-on delay time
Z_{out}	Output impedance
V_{CE}	Collector-emitter voltage

Table I

MC3100	Quad 2-Input NAND Gate
MC3101	Quad 2-Input AND Gate
MC3102	Quad 2-Input NOR Gate
MC3103	Quad 2-Input OR Gate
MC3120	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate
MC3129	Dual 3-Input 3-Output NAND Series Terminated Line Driver
MC3126	Dual 4-Input AND Power Gate
MC3104	Quad 2-Input NAND Gate (Open Collector)

AN-493
THE MC3100/MC3000 SERIES TRANSISTOR-TRANSISTOR LOGIC FLIP-FLOPS

INTRODUCTION

The success of any logic family depends on the capabilities of its storage elements. The flip-flops in the MC3000 (0 to 75°C) and MC3100 (-55 to +125°C) series are designed to provide maximum logic utility with fewer restrictions than their predecessors. Eliminating serious disadvantages of existing products was a major philosophy in the design of the storage elements of the MC3100 series.* The resulting improvements center on the following considerations:

1. The inputs to the storage element must have the same threshold characteristics as a standard gate.
2. Undershoot as normally found in the system shall cause no malfunction.
3. Clocking must occur on a single transition of the clock where the clock is defined to have any duty cycle such that the minimum up and down times are met or exceeded.
4. The propagation delay should be as equal as possible under normal load conditions.
5. Loading of one output should minimally affect the delay of the other output.
6. The direct set and reset inputs should completely override the clock and synchronous inputs under all conditions.
7. The synchronous logic inputs should have short input response times to both the "1" and "0" inputs.

*Reference will be made to the MC3100 series throughout, however, a comparable MC3000 part exists.

MC3100 SERIES FLIP-FLOP CIRCUITS

Table I lists the flip-flops that are discussed in the MC3100 series.

TABLE I – MTTL III Flip-Flops

Single J-K flip-flop with positive edge clock	MC3150
Single J-K flip-flop with negative edge clock	MC3151
Single master-slave J-K flip-flop	MC3152
Common clock, common reset, separate sets, dual J-K flip-flops with negative edge clock	MC3161
Separate clock, no reset, separate sets, dual J-K flip-flops with negative edge clock	MC3162
Type "D", Dual type D flip-flops with positive edge clock	MC3160

The three basic designs are typified by the MC3150, MC3160, and MC3161. Common to all designs are:

1. Edge clocking.

The flip-flop is clocked at the normal MTTL III threshold voltage (approximately 1.5 V @ 25°C).

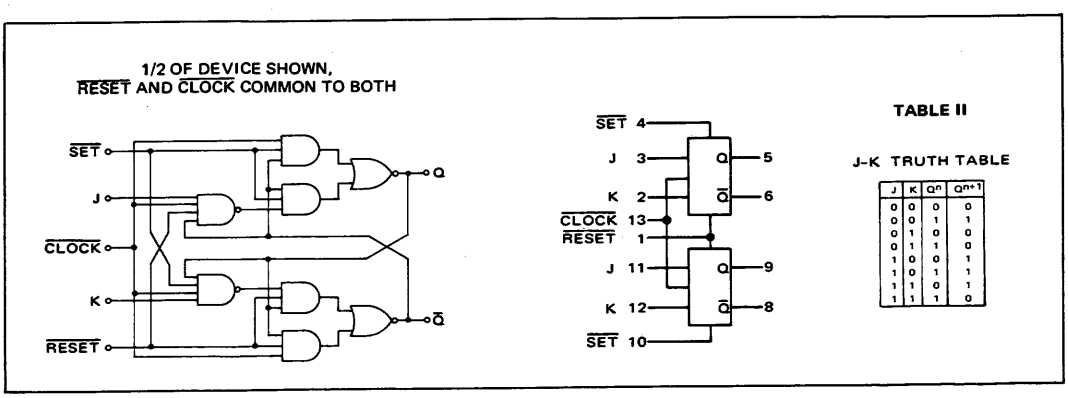


FIGURE 1 – MC3161 Logic Diagram

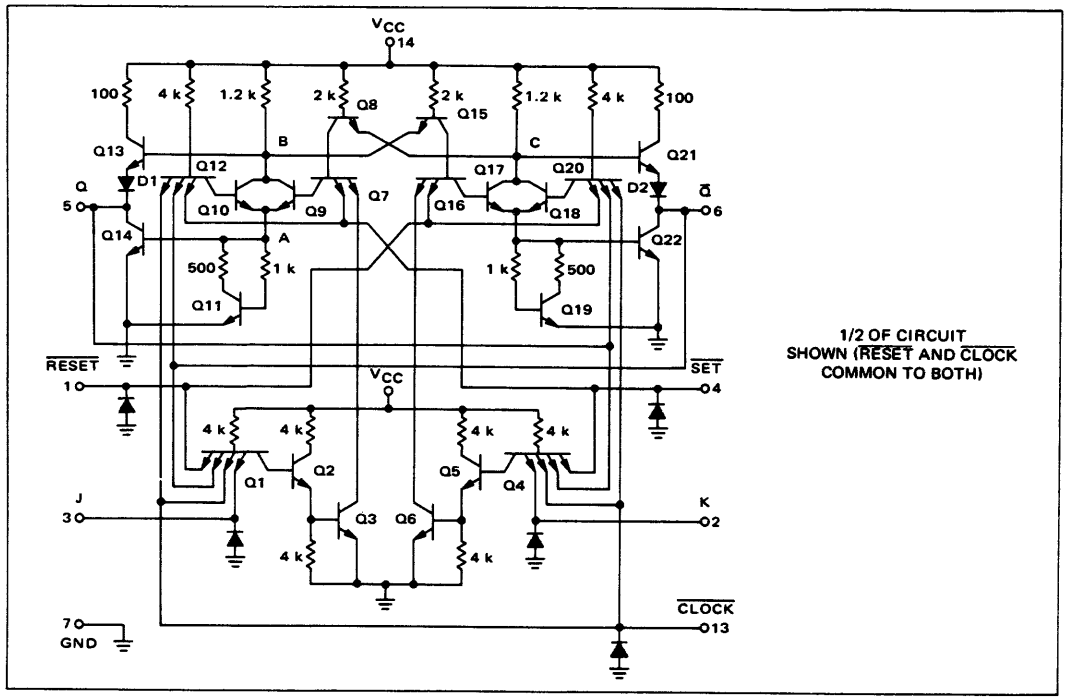


FIGURE 2 – MC3161 Dual J-K Flip-Flop Schematic

2. Overriding asynchronous inputs.

The direct set and reset input functions control regardless of the information on the clock or synchronous inputs.

3. Short set-up times.

Prior to the clocking edge, the input information must become stable. The MTTL III flip-flops require only a minimum of time to read a "1" or a "0". Unlike master-slave or charge storage types, control of the clock pulse width is no longer required to realize maximum usefulness.

4. Logic inputs require no special loading rules.

All inputs to the storage elements, including the clock input, are compatible with all three MTTL families. Each input can be expressed as a multiple of a MTTL input load. (One load is a 4 kΩ resistor to V_{CC} through the base-emitter junction of a multiple-emitter transistor). The switching threshold is the same as a standard gate ($2\ V_{be} - V_{offset}$).

The MC3150 and MC3160 flip-flops are positive edge triggered storage elements. That is, the inputs are enabled on the negative edge of the clock and the information is stored in the flip-flop on the positive edge of the clock. The MC3161 and MC3162, dual flip-flops, and the MC3151 single J-K flip-flop are negative edge triggered devices and therefore operate in the opposite manner. That is, data is stored on the negative edge of the clock.

In addition to the previously mentioned storage elements, the MC3152 master-slave flip-flop is also available. Data is stored in the master flip-flop when the clock is low and transferred to the slave flip-flop when the clock goes high.

Detailed discussion of each of the MC3100 series flip-flops is the subject of this application note.

MC3161 DUAL J-K FLIP-FLOP

The MC3161 dual J-K flip-flop triggers on the negative edge of the clock. Each flip-flop is provided with a separate direct $\overline{SET}$ input in addition to the common direct $\overline{RESET}$ input. These direct inputs provide a means of resetting a group of flip-flops, such as a register, which may be followed by the presetting of a data pattern. The clock input for this device is common for both flip-flops making it particularly useful in registers or other common clock applications.

Data may be applied to, or changed at, the clocked inputs at any time during the clock cycle except during the time interval between the Setup and Hold times. The inputs are inhibited when the clock is low and enabled when the clock goes high. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between the Setup and Hold times is stored in the flip-flop when the clock falls. Each flip-flop may be set at any time without regard to the clock state by applying a low level

to the $\overline{SET}$ input. In addition, both flip-flops may be reset simultaneously by using the common $\overline{RESET}$ in a similar manner.

Figure 1 is the logic and block diagram for the MC3161 while Table II is the J-K truth table of operation. Operation of the circuit (Figure 2) is as follows: Assume that the $\overline{SET}$ and $\overline{RESET}$ inputs are "high", the $\overline{Q}$ output terminal is "high", and Q output terminal is "low". Also assume that the J and K terminals are "high". With the clock "low", a "low" is applied to one emitter of transistors Q1, Q4, Q12, and Q20. With $\overline{Q}$ "high", a "high" is applied to one emitter of transistors Q1 and Q12. With Q "low", a "low" is applied to one emitter of transistors Q4 and Q20. With the $\overline{SET}$ and $\overline{RESET}$ terminals "high", a "high" is applied to one emitter of transistors Q7, Q4, Q16, and Q1. Under these assumptions, the state of individual transistors in

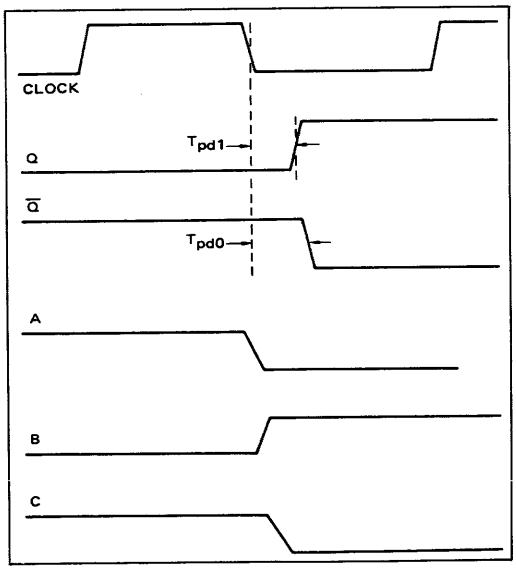


FIGURE 3 – MC3161 Voltage Waveforms

the flip-flop can be determined. With a "low" applied to one emitter of transistor Q1, transistors Q2 and Q3 are OFF. This same condition occurs at one emitter of transistor Q4, which causes transistors Q5 and Q6 to be OFF. A "low" applied to an emitter of Q12 keeps transistor Q10 OFF. The two "lows" applied to the emitters of Q20 keeps transistor Q18 OFF. With $\overline{Q}$ "high," transistor Q21 is ON, which means that point C (the base of Q21) sets near supply voltage, V_{CC}. The base-to-emitter diode of transistor Q8 is reversed-biased and current flows through the forward-biased base-to-collector diode of this device. With transistor Q3 OFF, as previously determined, both emitters of transistors Q7 are "high." The base-to-collector diode of transistor Q7 is forward-biased which causes transistor Q9 to be ON, which in turn causes transistors Q11 and Q14 to be ON. The voltage at point B sets at V_{BE} of transistor Q14 plus V_{CE} of Q9 which is not positive enough to sustain operation of transistor Q13 and diode D1, thereby causing these devices to be OFF. Under these conditions the base-to-emitter diode of transistor Q15 is forward-biased. This condition, along with the two previous "highs" determined at the emitters of transistor Q16, cause transistors Q16, Q17, Q19 and Q22 to be OFF. Point C sits near the supply voltage, V_{CC}, as previously assumed, turning Q21 and D2 ON, resulting in the $\overline{Q}$ output being "high."

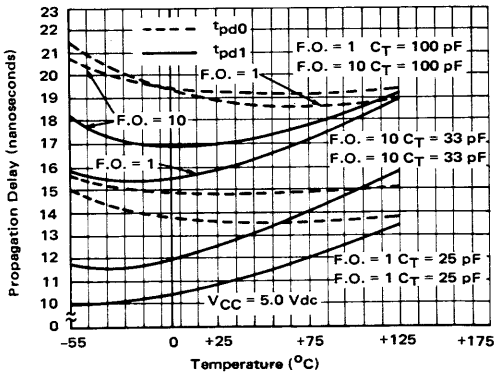


FIGURE 4a – MC3161 t_{pd0} and t_{pd1} versus Temperature

Now assume that the clock goes "high." All inputs to transistor Q1 are "high" causing transistors Q2 and Q3 to turn ON. The same condition exists at the inputs of transistor Q12. With all inputs to transistor Q12 "high," transistor Q10 turns ON, maintaining the ON conditions of transistors Q11 and Q14. With transistor Q3 ON, a "low" is applied to one emitter of transistor Q7, in turn removing base drive from transistor Q9, turning it OFF. Transistor Q10 has turned ON before transistor Q9 turns OFF and output Q has not changed state. Looking at the other side

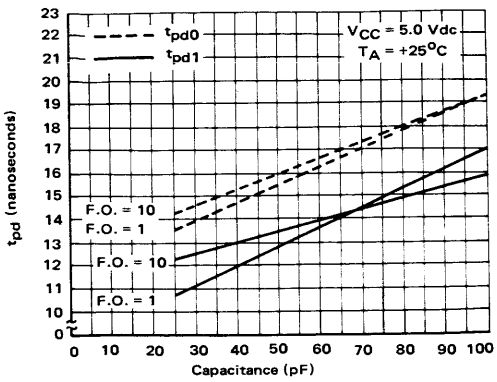


FIGURE 4b – MC3161 t_{pd1} and t_{pd0} versus Capacitance

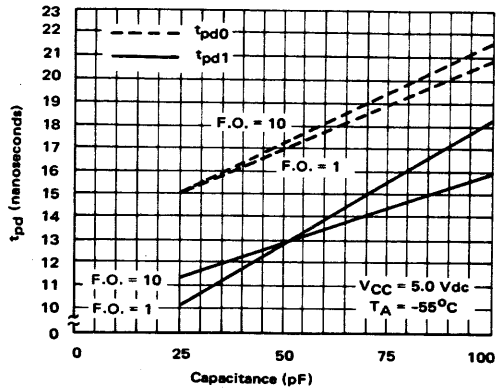


FIGURE 4c – MC3161 t_{pd1} and t_{pd0} versus Capacitance

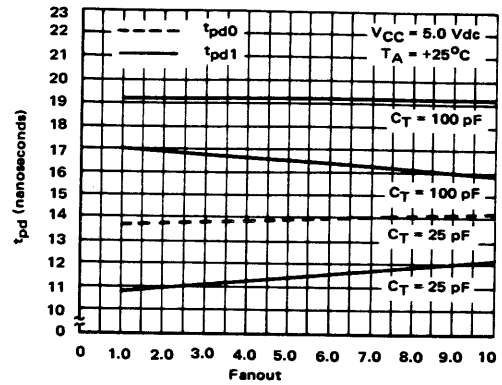


FIGURE 4e – MC3161 t_{pd1} and t_{pd0} versus Fanout

of the flip-flop, allowing the clock to go from a "low" to a "high" state does not effect transistors Q4 and Q20 as both have one other "low" applied to their input terminals. The state of the flip-flop has been maintained.

With the flip-flop in its present state and with the input information on both the J and K terminals "high," allow the clock to go "low." When the clock goes "low," transistor Q10 turns OFF which causes transistors Q11 and Q14 to turn OFF. The same condition (allowing the clock to go low) turns transistors Q2 and Q3 OFF. In this switching operation, transistor Q3 must remain ON long enough to allow transistors Q10, Q11, and Q14 to turn OFF. Point B has now risen near supply voltage, V_{CC}, causing transistor Q13 and diode D1 to turn ON. Current is forced through the forward biased base-to-collector diode of transistor Q15 (since both emitter inputs to transistor Q16 are "high") and through the forward biased base-to-collector diode of transistor Q16. This condition causes transistors Q17, Q19 and Q22 to turn ON. When transistors Q17, Q19 and Q22 turn ON, point C drops to a voltage level equal to the V_{BE} of transistor Q22 plus V_{CE} of transistor Q17 allowing transistor Q21 and diode D2 to turn OFF. Regeneration has taken place and the flip-flop has changed state.

With the flip-flop in its previous state (before the clock went "low") assume that a "low" is applied to the J terminal and a "high" to the K terminal. When the clock goes "low," the transistor combination of Q7 and Q8 will remain enabled and the flip-flop will not change state. In the switching operations it must be emphasized that transistors Q3 and Q6 must remain ON long enough for regeneration to take place. Figure 3 shows the voltage levels at the indicated points in the circuit of Figure 2. The voltage level at point A determines the conditions that exist at points B and C, as explained above. The conditions existing at the clock and the two outputs, Q and $\overline{Q}$, are also shown.

As can be seen from the circuit diagram, (Figure 2) the cross-coupling is internal during the regeneration period, thus the propagation times of one output are relatively unaffected by loading of the other output.

Figures 4a through 4h represent the typical operating

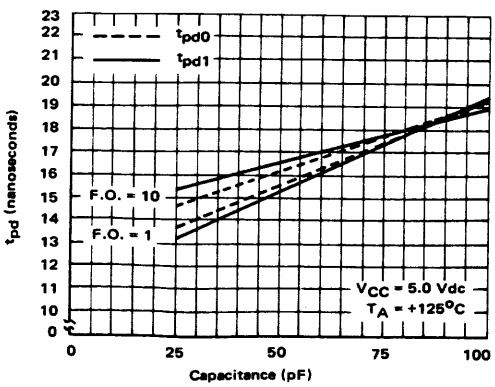


FIGURE 4d – MC3161 t_{pd1} and t_{pd0} versus Capacitance

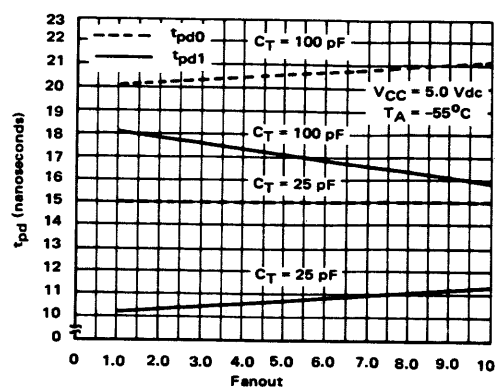


FIGURE 4f – MC3161 t_{pd1} and t_{pd0} versus Fanout

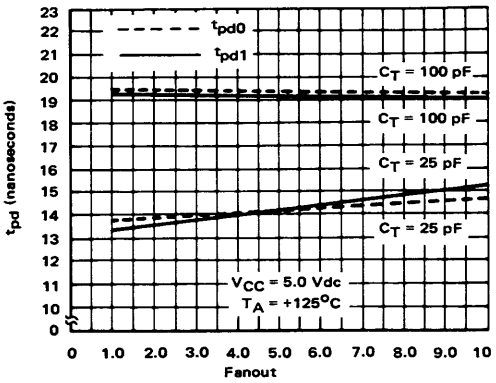


FIGURE 4g – MC3161 t_{pd0} and t_{pd1} versus Fanout

characteristics of the MC3161 dual J-K flip-flop. Samples were chosen from the dc data and typical turn-on delay (t_{pd0}) and turn-off delay (t_{pd1}) times were obtained as a function of fanout, capacitive loading, and temperature. Toggle frequency versus temperature is plotted for different loading conditions.

The logical "1" setup time is defined as the minimum time that high state data must be applied prior to the clock edge. Figure 5 shows the relation existing between information on the J terminal, the negative edge of the clock pulse, and the output terminal "Q" for a given fanout of one and capacitance load of 25 pF. The typical value of minimum logical "1" setup time is 8.1 nanoseconds. Table III lists typical values of logical "1" setup time under different loading conditions.

The logical "0" setup time is defined as the minimum time that low state data must be applied prior to the clocking edge. Figure 6 shows the relations existing between information on the J terminal, negative edge of clock pulse, and output terminal "Q" for a given fanout of one and capacitance load of 25 pF. The typical value of minimum logical "0" setup time is 7.8 nanoseconds. Table IV lists typical values of logical "0" setup time under different loading conditions.

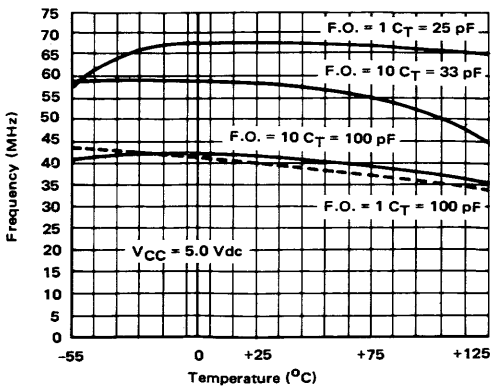


FIGURE 4h – MC3161 f_t versus Temperature

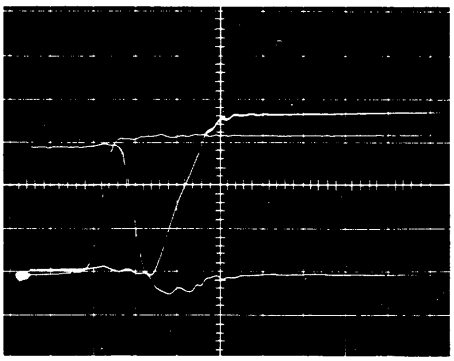


FIGURE 5 – MC3161 Logical "1" Setup Time

From Left to Right:
1st Pulse – "J" input
2nd Pulse – Negative edge of clock
3rd Pulse – "Q" Output

Vert. = 1 V/div.
Horiz. = 10 ns/div.
V_{CC} = 5.0 Vdc
T_A = +25°C
F.O. = 1 and C_T = 25 pF

Load	Logical "1" Setup Time
F.O. = 1 and 25 pF	8.1 ns
F.O. = 10 and 33 pF	6.6 ns

TABLE III

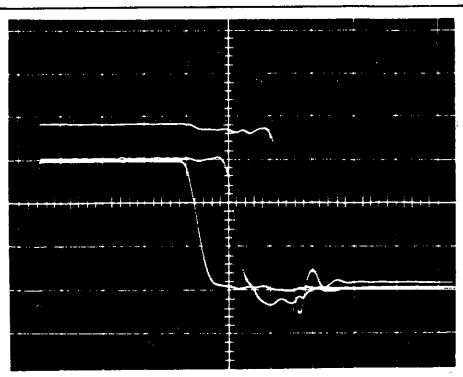


FIGURE 6 – MC3161 Logical "0" Setup Time

From Left to Right:
1st Pulse – "J" input
2nd Pulse – Negative edge of clock
3rd Pulse – "Q" output

Vert. = 1 V/div.
Horiz. = 10 ns/div.
V_{CC} = 5.0 Vdc
T_A = +25°C
F.O. = 1 and C_T = 25 pF

Load	Logical "0" Setup Time
F.O. = 1 and 25 pF	7.8 ns
F.O. = 10 and 33 pF	8.0 ns

TABLE IV

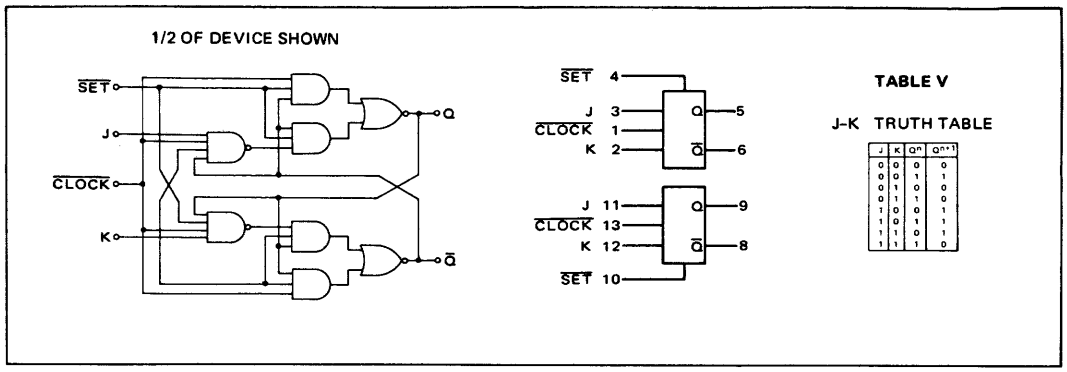


FIGURE 7 – MC3162 Logic Diagram

As can be seen from Figures 1 and 2, all inputs to the flip-flop (which includes J and K terminals, $\overline{SET}$ and $\overline{RESET}$ inputs, and clock input) have the same threshold characteristics as a standard gate which is 2 V_{BE} or, approximately 1.5 volts.

Input diodes are present on all inputs to the flip-flop such that undershoot as normally found in the system will cause no malfunction of the device. (See Appendix A).

Outputs Q and $\overline{Q}$ are characterized by the familiar MC3000 series transfer characteristic. (See Appendix B).

MC3162 DUAL J-K FLIP-FLOP

The MC3162 dual J-K flip-flop is identical in circuit operation to the MC3161. The MC3162, however, has separate clock inputs and no common direct $\overline{RESET}$ input. Figure 7 is the logic diagram along with the block diagram of the device while Table V lists the operation of the device.

MC3151 SINGLE J-K FLIP-FLOP

The MC3151 single J-K flip-flop (see Figure 8) is identical in circuit operation to the MC3161. An AND input gating configuration formed by three J inputs ANDed together and three K inputs ANDed together minimizes external gating requirements. The enable input (JK) consists of a J and a K input internally connected. This input provides gating for the J and K inputs or an additional logic input for use in counters or other applications. A direct $\overline{SET}$ and direct $\overline{RESET}$ are provided to permit presetting data such as initial conditions into the flip-flop.

MC3150 SINGLE J-K FLIP-FLOP WITH POSITIVE EDGE CLOCK

Figure 9 shows the circuit of the MC3150, and Figure 10, the logic diagram, block diagram, and truth table of operation, Table VI.

This J-K flip-flop triggers on the positive edge of the clock. An AND input gating configuration formed by three J inputs ANDed together and three K inputs ANDed together, minimizes the requirements for external gating. The enable input (JK) consists of a J and K input internally connected together. This input provides gating for the J and K inputs or an additional logic input for use in counters or other applications. A direct SET and RESET are provided to permit presetting data such as initial conditions into the flip-flop. The direct SET and RESET inputs fully override the clock; i.e., the direct SET and RESET inputs control the operation of the flip-flop regardless of the state of the clock.

Information may be applied to, or changed at, the J and K inputs any time in a clock cycle except during the

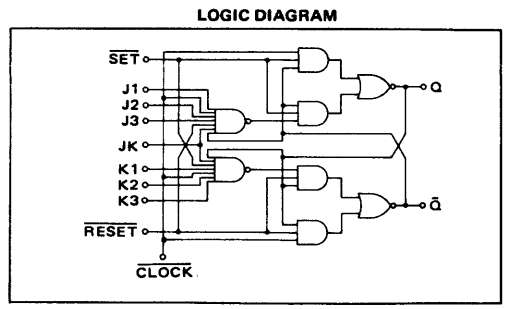


FIGURE 8 – MC3151 Logic Diagram

interval of time between the Setup and Hold times. The inputs are inhibited while the clock is high and data is entered into the input steering section of the flip-flop when the clock goes low. The input steering section of the flip-flop continually reflects the input state when the clock is low. Data present during the time interval between the Setup and Hold times is transferred to the bistable section on the positive edge of the clock and the outputs Q and $\overline{Q}$ respond accordingly. The flip-flop can be set or reset directly by applying a high state to the SET or RESET inputs.

The circuit operation for this device will be explained by referring to the logic diagram of Figure 10. A set of

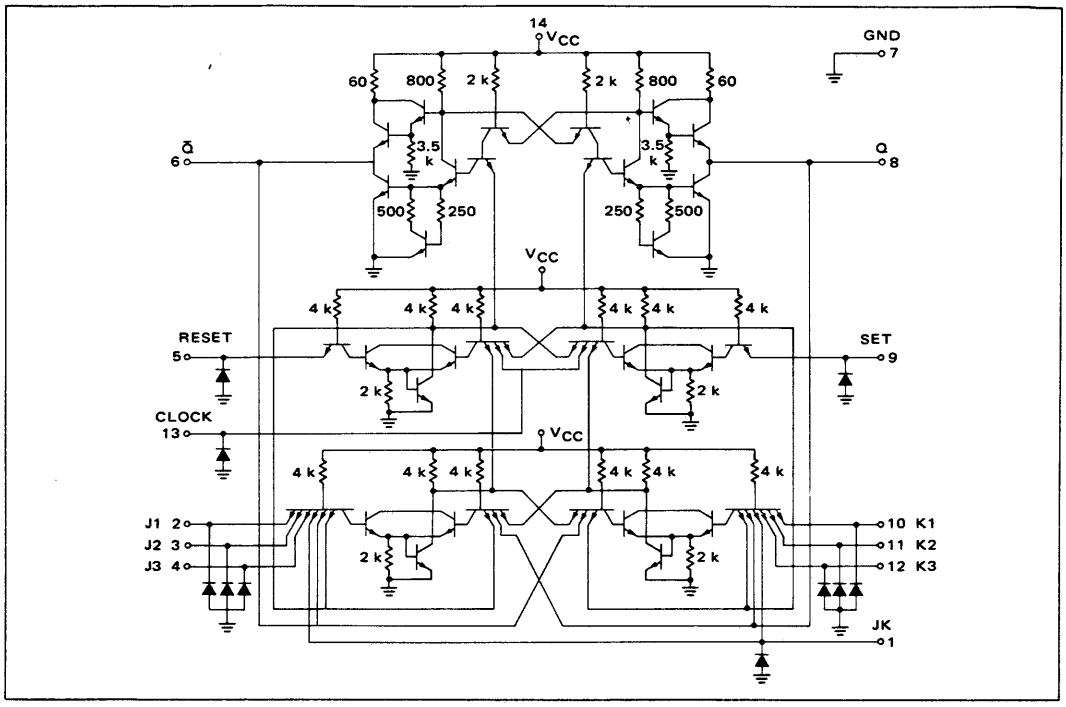


FIGURE 9 – MC3150 "AND" J-K Flip-Flop Schematic

gates, a and b, are connected in parallel with another set of gates, g and h, with appropriate feedback from the outputs to provide J-K operation. The three J inputs are ANDed together at the g gate and the three K inputs are ANDed together at the h gate. Assuming the clock is low, the input data can affect only the two gates, a and b, after being initially applied to gates g and h. With the clock "low," gates c and d are cut off; both outputs are "high." The last pair of gates, e and f, store the previous information and provide the outputs of the flip-flop. When the clock is changed from a "low" to a "high," only one of the gates, c or d, can turn ON since the data input is indirectly applied to gate d and the data's complement is applied to gate c. The gate (c or d) that turns ON provides two functions. It gates the feedback that stabilizes its inputs and transfers data to the output gates e and f.

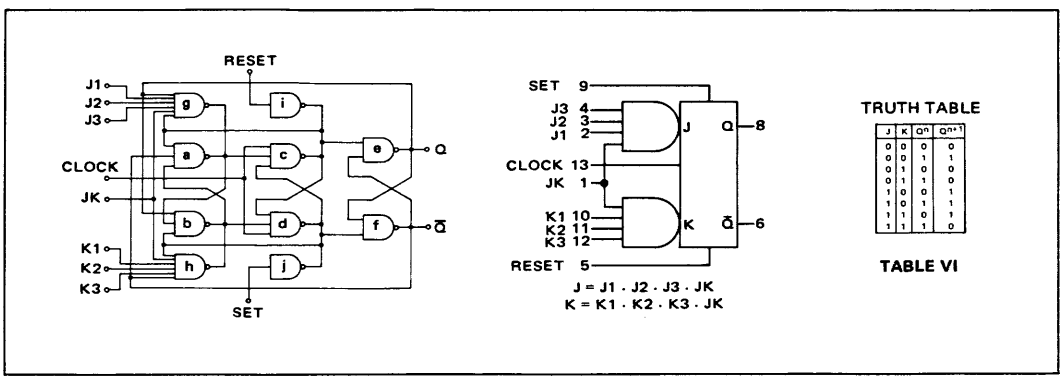


FIGURE 10 – MC3150 Logic Diagram

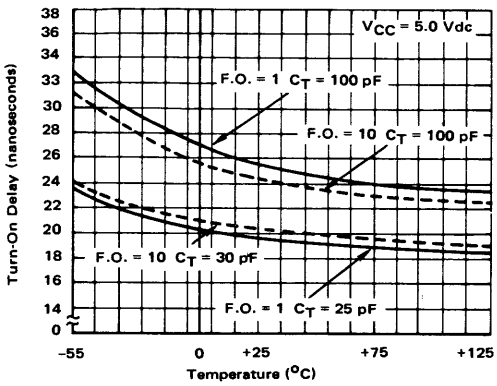


FIGURE 11a – MC3150 t_{pd0} versus Temperature

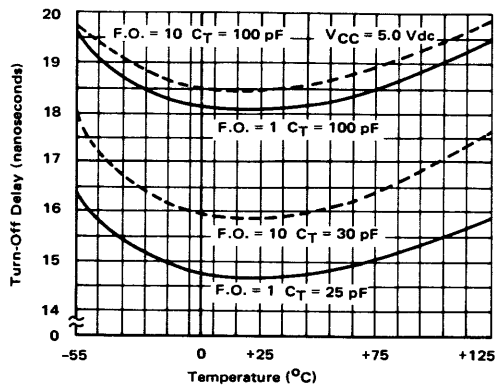


FIGURE 11c – MC3150 t_{pd1} versus Temperature

Figures 11a through 11e represent the typical operating characteristics of the MC3150 J-K flip-flop. Samples of the device were chosen from the dc data and typical turn-on delay (t_{pd0}) and turn-off delay (t_{pd1}) times were obtained as a function of temperature and capacitive loading. Toggle frequency as a function of temperature is plotted under different loading conditions.

Typical values for logical "1" setup times and logical "0" setup times are 10 nanoseconds and 5.0 nanoseconds, respectively. The logical "1" hold time, (the minimum time that the "high" state data must be maintained after the clocking edge) is typically 5.0 nanoseconds. The logical "0" hold time (the minimum time that the "low" state data must be maintained after the clocking edge) is typically 5.0 nanoseconds.

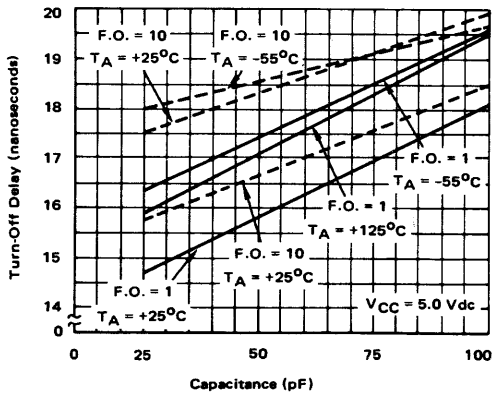


FIGURE 11d – MC3150 t_{pd1} versus Capacitance

MC3160 – TYPE "D" DUAL FLIP-FLOP WITH POSITIVE EDGE CLOCK

Figure 12 shows circuit schematic for the MC3160, and Figure 13 the logic and block diagrams of the device. Table VII lists typical operating characteristics of the device.

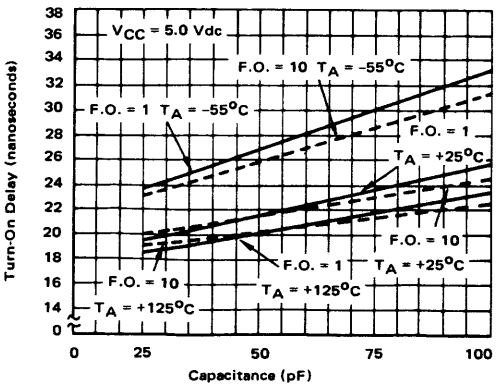


FIGURE 11b – MC3150 t_{pd0} versus Capacitance

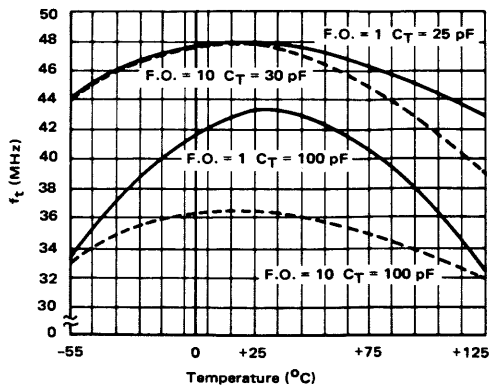


FIGURE 11e – MC3150 f_t versus Temperature

The MC3160 dual flip-flop triggers on the positive edge of the clock and performs the Type "D" flip-flop function. This device consists of two completely independent Type "D" flip-flops, both having direct $\overline{SET}$ and $\overline{RESET}$ inputs for asynchronous operations such as parallel data entry in shift register applications.

Information may be applied to, or changed at, the D inputs any time during the clock cycle except during the time interval between the Setup and Hold times. The clocked inputs are inhibited when the clock is high and

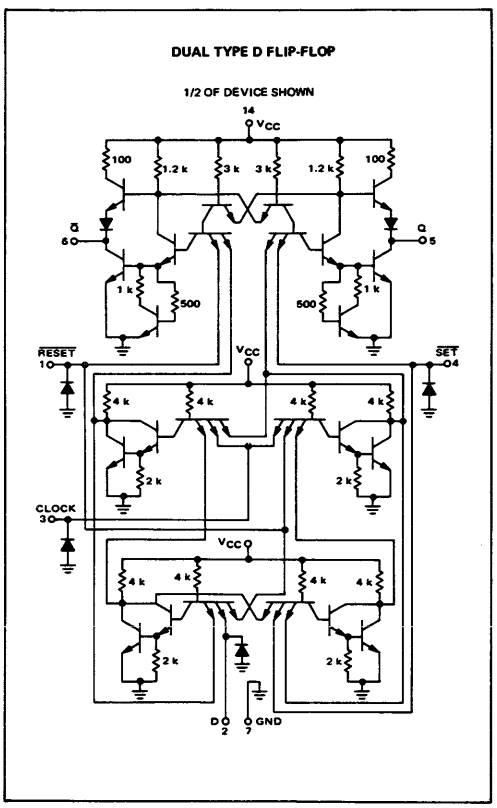


FIGURE 12 – MC3160 Dual Type D Flip-Flop Schematic

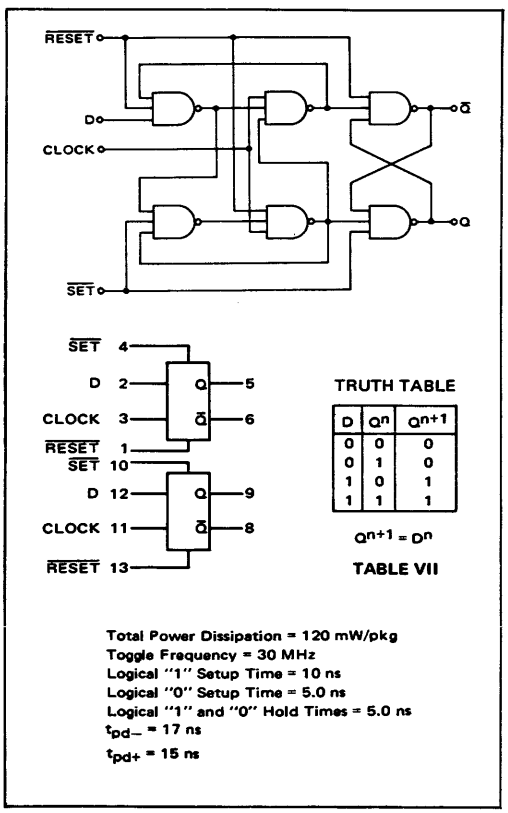


FIGURE 13 – MC3160 Logic Diagram

data may be applied to the input steering section of the flip-flop when the clock goes low. The input steering section continually reflects the input state being applied when the clock is low. The information present at the inputs during the time interval between the Setup and Hold times is transferred to the bistable section on the positive edge of the clock, and the outputs Q and $\overline{Q}$ respond accordingly.

The flip-flop can also be set or reset directly at any time, regardless of the state of the clock, by applying a low state to the direct $\overline{SET}$ or $\overline{RESET}$ inputs.

The circuit operation is similar to the explanation given for the MC3150 flip-flop.

MC3152 – "AND" INPUT $J\overline{J}$-$K\overline{K}$ FLIP-FLOP

In addition to the previously mentioned flip-flops, the MC3152 master-slave J-K shown in Figure 14 is also available. The logic diagram, block diagram, and typical characteristics are indicated in Figure 15.

The MC3152 is a master-slave J-K flip-flop that triggers on the positive edge of the clock. The flip-flop has an AND input configuration consisting of two J-inputs and a $\overline{J}$-input ANDed together and two K-inputs and a $\overline{K}$-input ANDed together. An enable input (J-K) is also provided consisting of an additional J and K input internally connected together. This input provides gating in addition to the clock for the clocked inputs (J, $\overline{J}$, K and $\overline{K}$) or an additional logic input (J-K) for use in counters or certain other applications. A direct $\overline{SET}$ and $\overline{RESET}$ are provided to enable presetting data into the flip-flop such as initial conditions. The direct $\overline{SET}$ and $\overline{RESET}$ control the operation of the clock.

Information is normally applied to, or changed at, the clocked inputs while the clock is in the high state since the inputs are inhibited under this condition. Information may

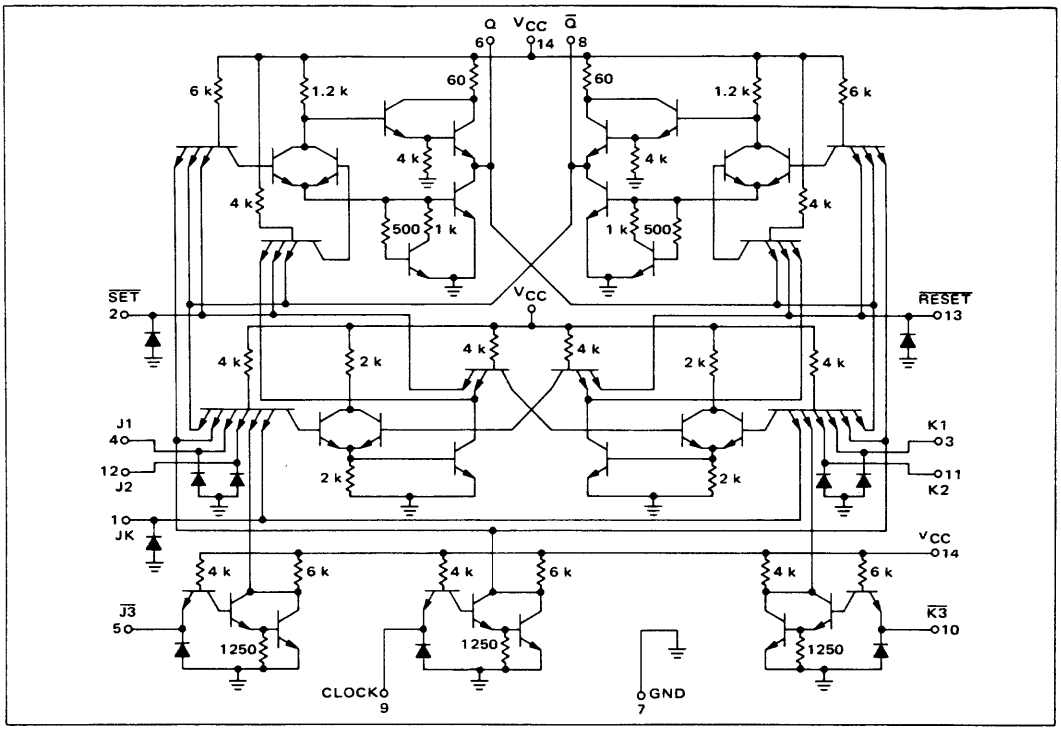


FIGURE 14 – MC3152 "AND" Input JJ̄-KK̄ Flip-Flop Schematic

be stored in the master flip-flop section when the clock goes low. Once input data has been stored in the master flip-flop section it cannot be removed (or changed) by means of the clocked input. The direct $\overline{SET}$ or $\overline{RESET}$ provide the only means of removing previously stored information. The state of the master flip-flop is transferred to the slave flip-flop section on the positive transition of the clock and the outputs respond accordingly. The flip-flop can be set or reset directly by applying the low state to the direct $\overline{SET}$ or $\overline{RESET}$ inputs.

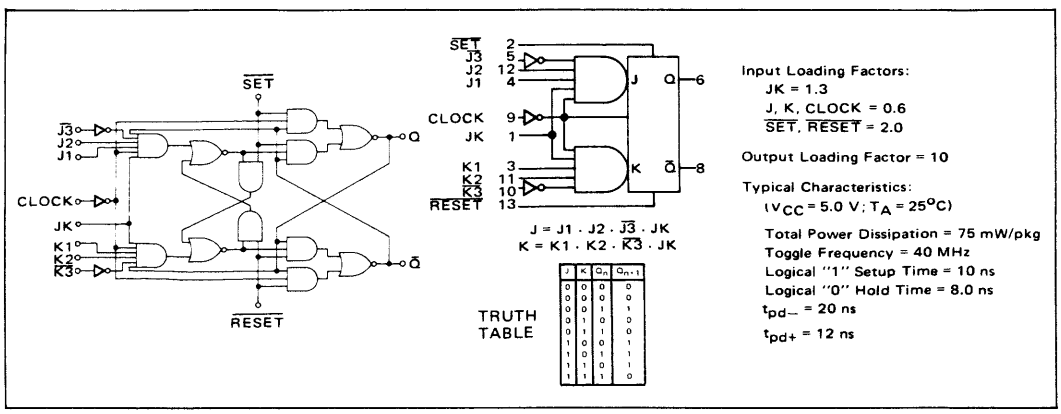


FIGURE 15 – MC3152 Logic Diagram

CONCLUSION

This application note has explained the basic operation of the various flip-flops available in the MC3100 series of transistor-transistor logic from Motorola. Typical operating characteristics have been included for various devices such that operation under almost any set of conditions can be determined.

APPENDIX A

ADDITION OF INPUT DIODES

Due to high speeds of operation TTL generates large values of current and voltage rates of change. A 1 volt change in approximately 1.3 nanoseconds for the rise time and a 1 volt change in about 1.0 nanoseconds for the fall time, provides dV/dt rates on the order of 10^9 volts per second. With these rates of change, undershoot exceeding 2 volts can develop in the system which can cause problems in succeeding circuits. Two very serious problems result from the possible undershoot. First false triggering of the following stage is possible since a positive overshoot follows the large undershoot. This positive overshoot may act as a "high" signal and turn on the following stage for a short period of time. Diodes on inputs limit the negative value of the undershoot dissipating the ringing energy and thereby limiting the positive overshoot. Figures 16a and 16b show the effect of adding the clamp diodes on inputs of TTL gates at the end of a 93 ohms line. In Figure 16b it can be seen that without clamp diodes the positive overshoot has turned the following gate ON momentarily. The second problem results if the unused inputs of a gate are returned to the supply voltage and a negative undershoot in excess of 2 volts occurs. These reverse biased emitters may breakdown and draw excessive current which creates noise in the system.

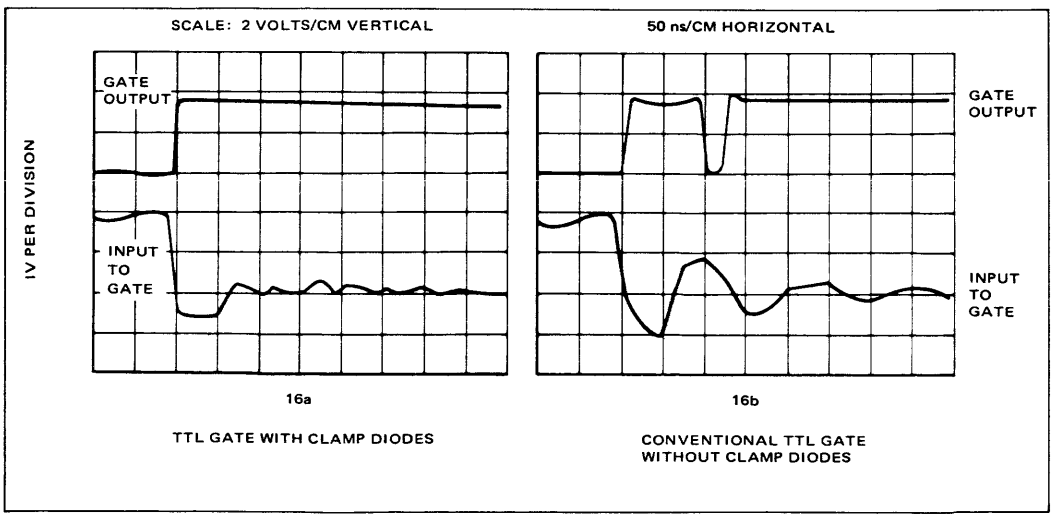


FIGURE 16 – Comparison of Waveforms With (a) and Without (b) Input Clamp Diodes

APPENDIX B
COMPARISON OF TRANSFER CURVES

CONVENTIONAL TTL

By applying a "low" to either A or B inputs of the gate shown in Figure 17, a base-to-emitter diode of transistor Q1 becomes forward biased. No base drive is available for transistor Q2 which turns OFF and causes transistor Q5 to turn OFF. The collector of Q2 rises toward the supply voltage, V_{CC}, and supplies base drive to turn ON transistor Q3 which causes transistor Q4 to turn ON. Transistors Q3 and Q4 act as emitter followers and this places the output, V_O, two V_{BE} drops below V_{CC} in its quiescent "high" state or approximately 3.5 volts.

Consider the case where input A is "high" and input B begins to go from a "low" to a "high". Base drive is gradually applied to transistor Q2 which now starts to conduct with emitter current initially flowing through R4. As transistor Q2 turns ON the collector current of Q2 produces a voltage drop across resistor R2. The collector of Q2 is connected to output V_O by means of the two emitter follower transistors Q3 and Q4 and therefore the output V_O tracks the voltage at the collector of Q2. As the voltage at input B increases the base of Q2 tracks this voltage by the difference of $V_{BE} - V_{CB}$ of transistor Q1. The collector current through Q2 increases causing a larger drop across resistor R2. The output V_O now changes at a rate ΔV_B R2/R4 as shown on Figure 18 between points a and b on the transfer characteristic. When the emitter current of Q2 increases to the point where the drop across R4 equals one V_{BE}, transistor Q5 begins to conduct. Point b on the transfer characteristic has been reached. With a further increase in the voltage at input B, transistor Q5 saturates and point c on the transfer characteristic is reached. The collector of transistor Q2 now sits at V_{BE} of Q5 plus V_{CE} of Q2. This voltage is not positive enough to sustain operation of transistors Q3 and Q4, and these devices are OFF. The output is now in its quiescent "low" state of V_{CE} equal to approximately 0.2 volts.

MC3100 TTL

The difference between Motorola's TTL III and conventional TTL is the replacement of resistor R4 in Figure 17 with resistors R4a and R4b and transistor Q6 in Figure 19.

With a "low" on either A or B, a base-to-emitter diode of transistor Q1 is forward biased and no base drive is available for transistor Q2, which keeps Q2 OFF as well as transistors Q5 and Q6. The collector of transistor Q2 sits near supply voltage V_{CC} and base current is supplied to transistor Q3 keeping this device and Q4 ON.

Assume now that input A is "high" and input B gradually goes from a "low" to a "high". The base of transistor Q2 tracks the voltage at input B as in conventional TTL by the difference of $V_{BE} - V_{CB}$ of transistor Q1. At the point where transistor Q2 turns "ON" in conventional TTL, transistor Q2 does not turn ON in Motorola's TTL III since the equivalent of an open circuit exists at its emitter. With no current flow the collector of Q2 remains near the supply voltage V_{CC}. Since transistors Q3 and Q4 act as emitter followers the output remains at the "high" level which is approximately two V_{BE} drops below V_{CC}. The bypass network turns ON when the potential at the base of Q2 is two V_{BE} drops above ground which also causes the output transistor Q5 to turn ON. In Figure 18 this is point d on the Motorola TTL III transfer characteristic. As the potential on input B increases further, output transistor Q5 saturates and point e is reached on the Motorola TTL III transfer characteristic. The resistors in the bypass network are chosen such that the network conducts the same current as resistor R4 in Figure 17 when transistor Q5 is saturated.

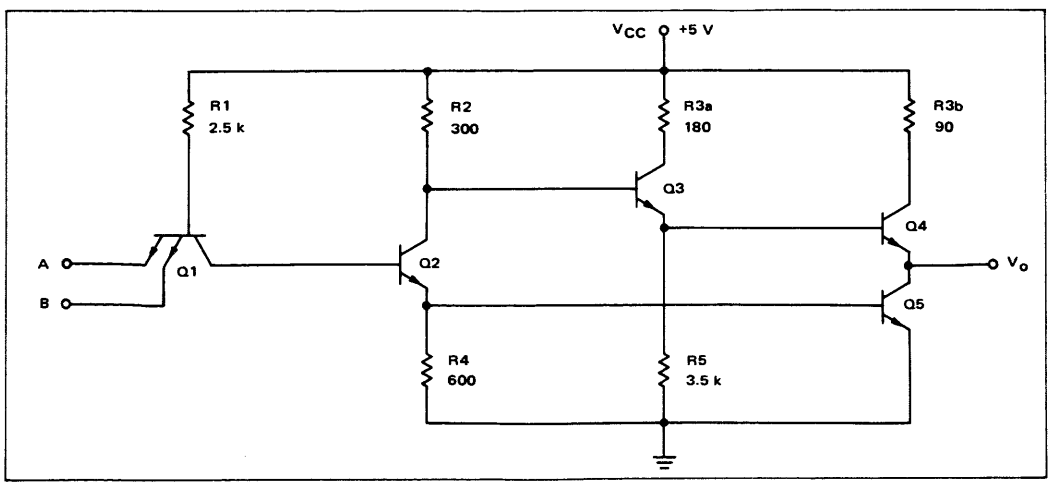


FIGURE 17 – Conventional TTL Gate

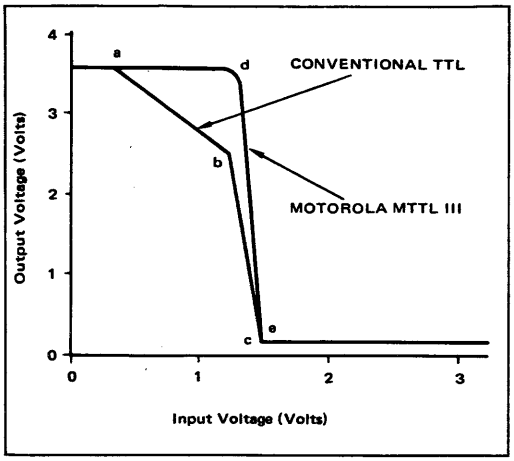


FIGURE 18 – Comparison of TTL and MTTL III

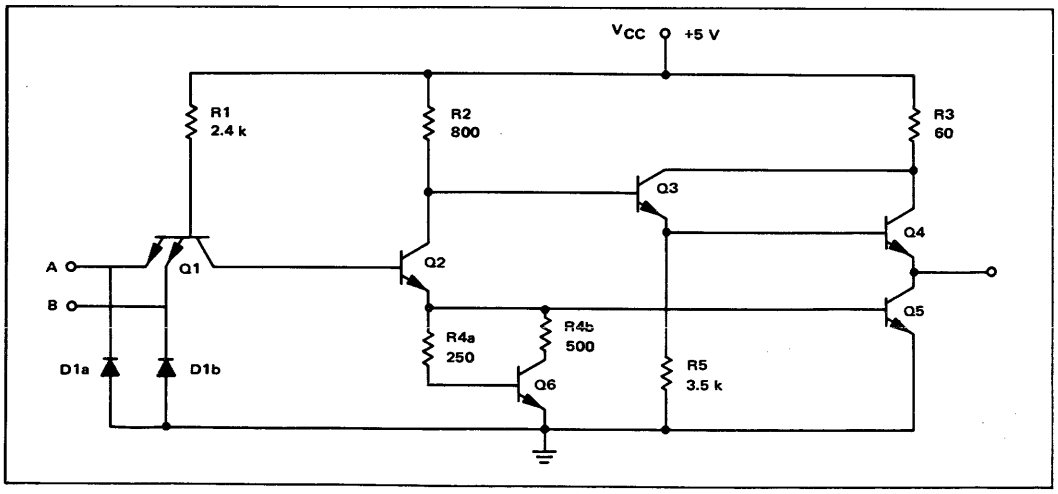


FIGURE 19 – Improved MTTL III Gate

The transfer characteristics just described compare the operation of the Motorola MC3100 series of transistor-transistor logic with other high frequency forms of this logic available on the market today. Due to the square type transfer characteristic of the Motorola MC3100 series the dc noise immunity of this particular family of TTL is considerably improved over other available families. The bypass network used to achieve the described transfer characteristic provides additional advantages over the simple resistor.

Figure 20 shows the variation with temperature of a standard monolithic resistor and the MTTL III bypass network impedance. As can be seen from this figure there is a much smaller impedance variation with temperature in the case of the MTTL III bypass network. The bypass network offers several advantages over the simple resistor due to its improved impedance variation with temperature.

(1) When turning OFF, transistor Q6 (Figure 19) turns OFF after transistor Q5. This provides for faster turn-off at elevated temperatures of the output transistor by means of lower bypass impedance.

(2) Faster switching and lower power consumption resulting from a lower current spike during the turn-off transient at high temperatures.

(3) At low temperatures, a faster turn-ON time.

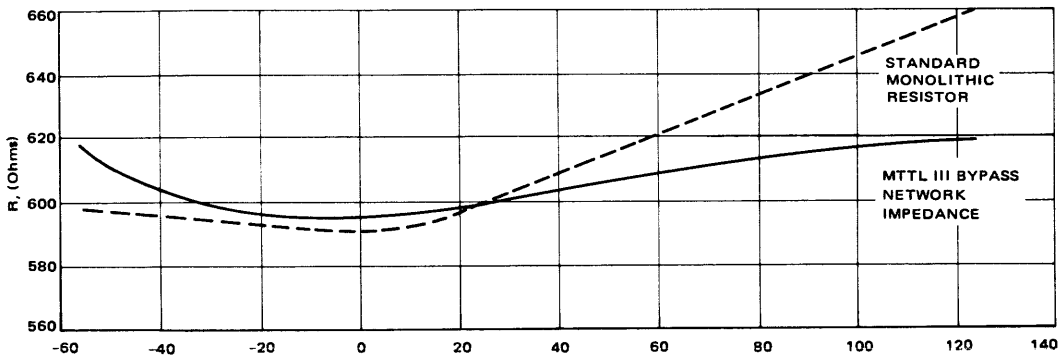


FIGURE 20 – MTTL III Bypass Network Impedance versus Temperature

AN-494
TRANSISTOR-TRANSISTOR LOGIC LINES

THE MTTL LINES

Motorola offers extensive lines of transistor-transistor logic (MTTL) providing medium-to-high speed, high-noise immunity, and performance advantages compared to competitive types. Transistor-transistor logic is the fastest form of saturated logic available to the designer. As a result of this high speed, transmission line problems such as ringing and line reflections can cause false switching. All Motorola TTL designs incorporate clamp diodes on the inputs to clamp any negative ringing that may occur to a level that will not cause false triggering. The effect of these diodes is discussed in Appendix A.

The MC5400/7400 Series is function and pin compatible with the SN54/74 series. This series is characterized by typical propagation delays of 13 ns/gate and 30 ns/flip-flop. Power dissipation is typically 10 mW/gate and 40 mW/flip-flop. A list of all MTTL device electrical characteristics is given in Figure 1.

MTTL I is similar to the MC5400/7400 Series, but offers increased speed. The basic gate consists of three parts: 1. A multiple-emitter input transistor; 2. A phase splitting transistor; and 3. A "totem pole" output transistor pair. MTTL I devices provide 10 ns/gate average propagation delays and moderately good output drive capabilities. The "totem-pole" output is utilized to increase switching speed on the "low" to "high" output transition.

MTTL II is a higher-speed version of MTTL I. It provides propagation delays that are nearly twice as fast as comparable MTTL I gates. This speed is gained at a 7 mW cost in power dissipation (per gate). This is roughly a 50

ELECTRICAL COMPARISON OF MTTL LINES

Parameter	MTTL I MC500/550 MC400/450	MTTL II MC2100/2150 MC2000/2050	MTTL III MC3100 MC3000	MC5400/MC7400 MC5400 MC7400
V_{CC} max cont. pulsed < 1 sec nominal	+8.0 V +7.0 V +12.0 V +12.0 V +4.5 to 6.0 V	+8.0 V +7.0 V +12.0 V +4.5 to 6.0 V	+7.0 V +4.5 to 5.5	+7.0 V +4.75 to 5.25 +4.5 to 5.5
V_{in} max	+5.5 V	+5.5	+5.5	+5.5 V
V_{out}	+5.5 V	+5.5	+5.5	+5.5 V
Power Diss. Gate F-F	15 mW 40 to 50 mW	22 mW 40 to 50 mW	22 mW 50 to 80 mW	10 mW 40 mW
DC Noise Margin-High -Low	0.700 V 0.600 V 0.750	0.700 0.600 0.650	0.700 0.700	0.400 V 0.400 V
Operating Temp. Range	-55 to 125°C 0 to +75°C	-55 to 125°C 0 to +75°C	-55 to 125°C, 0 to 75°C	-55 to +125°C 0 to +70°C
Storage Temp. Range	F & L -65 to +200°C P -55 to +125°C	F & L -65 to +200°C P -55 to +125°C	F & L -65 to +175°C P -55 to +125°C	L -65 to +150°C P -55 to +125°C
θ_{JC} Ceramic (F & L)	0.09°C/mW	0.09°C/mW	0.09°C/mW	0.09°C/mW
θ_{JC} Plastic (P)	0.15°C/mW	0.15°C/mW	0.15°C/mW	0.15°C/mW
θ_{JA} Ceramic (F & L)	0.26°C/mW	0.26°C/mW	0.26°C/mW	0.26°C/mW
θ_{JA} Plastic (P)	0.30°C/mW	0.30°C/mW	0.30°C/mW	0.30°C/mW
T_J max	+175°C +150°C	+175°C +150°C		+175°C +150°C
Fanout Capability	15/7 12/6 or 600 pF	11/6 9/5 or 600 pF	10 or 600 pF	10 or 600 pF
Z_{out}-High	70 Ω	10 Ω	10 Ω	70 Ω
-Low	10 Ω	10 Ω	10 Ω	10 Ω
Z_{in}-High	400 kΩ	400 kΩ	400 kΩ	400 kΩ
-Low	4.0 kΩ	2.5 kΩ	2.4 kΩ	4.0 kΩ
Switching Threshold	1.5 V	1.5 V	1.5 V	1.5 V
Speed: t_d	10 ns/Gate 18 ns/FF	6 ns/Gate 15 ns/FF	6 ns/Gate 13 ns/FF	13 ns/Gate 30 ns/FF
t_r	2.5 ns	1.0 ns	1.0 ns	2.5 ns
t_f	1.5 ns	1.3 ns	1.3 ns	1.5 ns
Flip-Flops: f_T	30 MHz	50 MHz	70 MHz	15 MHz typ
Min Clock Pulse Width	20 ns	15 ns		20 ns
Max Clock Fall Time	150 ns	100 ns	None	
Min Clock Amplitude	1.8 V	1.8 V		
Logical "1" Setup Time			10 ns	
Logical "0" Setup Time			5 ns	
Logical "1" Hold Time			5 ns	
Logical "0" Hold Time			5 to 6 ns	
AC Power Diss. @ 25°	0.35 mW/MHz/gate	0.7 mW/MHz/gate	0.4 mW/MHz/gate	0.3 mW/MHz/gate

FIGURE 1 – Electrical Characteristics of MTTL Families

percent power increase. The only major circuit change from MTTL I is the addition of a transistor in the pullup portion of the output.

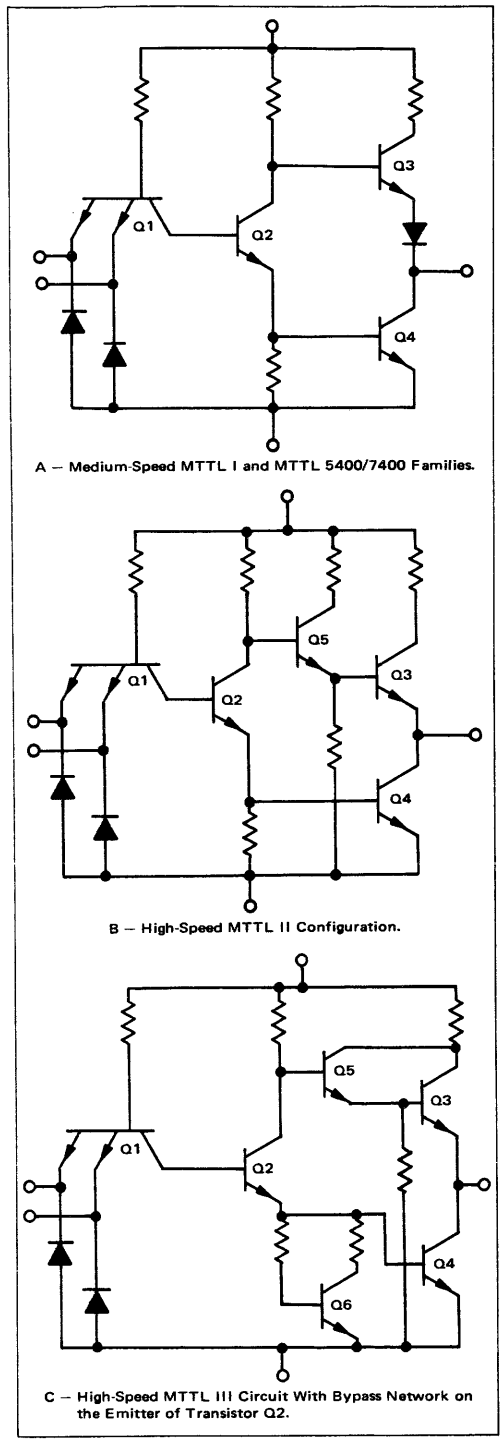
MTTL III is the most advanced version of TTL gate presently available. It has the same dc power dissipation and propagation delay as MTTL II but has much improved ac power dissipation characteristics (a factor of two better than MTTL II) and has much more stable speed characteristics over the full temperature range. The reason for this difference is the active bypass in the lower output stage. A detailed explanation of this circuit is included in a later section. A significant advantage of MTTL III flip-flops is that input information can be changed while the clock is in either the high or low states.

The MC4000 series offers a large number of MTTL complex functions. These functions fall in the MSI or Medium Scale Integration class of 25 to 100 gates per device. Their use allows considerable savings of space, cost per logic decision, power dissipation, time delay per gate, and cost of assembly.

OPERATION OF THE BASIC GATE

The building block of MTTL logic is the NAND gate shown in Figure 2. MTTL logic can be identified by a multiple emitter input transistor and an active pull-up in the output network. It functions as follows: Suppose one of the emitters on the input transistor is at ground (low) potential. A transistor with a forward base-emitter bias would normally conduct. However, in this case, collector current is limited by the magnitude of the reverse base current of Q2. Thus, when any of the emitters of Q1 are in a low state, Q1 will saturate in the forward direction and quickly pull Q2 into cutoff. Now, let all the emitters of Q1 be at a high potential. Note that the collector voltage is lower than the emitter and the base voltages, i.e., the collector-base junction is forward biased and the base-emitter junction is reverse biased (the opposite of normal transistor biasing). Q1 acts as a transistor with collector and emitter currents flowing in directions opposite from normal. Such operation is not particularly useful under normal conditions because of its inefficiencies, but it is ideal for this application. Because transistor beta is very low in the reverse mode, most of the collector current comes from the base instead of the emitter. This minimizes the input loading of the gate for the high state.

The state of Q2 is completely controlled by the input emitters of Q1. Q2 is a phase splitting transistor used to drive the output stages. Since the inverted output drives the upper output transistor and the noninverting output drives the lower transistor, both output transistors cannot be ON simultaneously except for a brief time during switching. When both output transistors are ON, a low impedance path exists from power supply to ground. As a result, a power supply current "spike" appears during switching. At high switching rates, enough spikes occur per second to cause a significant increase in power consumption.



A – Medium-Speed MTTL I and MTTL 5400/7400 Families.

B – High-Speed MTTL II Configuration.

C – High-Speed MTTL III Circuit With Bypass Network on the Emitter of Transistor Q2.

FIGURE 2 – Basic MTTL Gate Circuits

AOI GATES

MTTL devices with the active pullup in the output circuit cannot be "WIRE-ORed" as can MDTL circuits (See Figure 3). If the outputs of the devices are tied together, it is possible for the lower transistor of one circuit and the upper transistor of the other circuit to be "ON" simultaneously. This condition provides a low impedance path from V_{CC} to ground and the current that flows exceeds the guaranteed sink current. As a result, the saturated state cannot be maintained and the desired logic function is not satisfied.

For this reason, Motorola offers "AND-OR-INVERT" gates which perform the same function as the "WIRED-OR" but at higher speeds. Open collector devices are also available to permit the user to "WIRE-OR" if he wishes.

MTTL III OPERATION AND ADVANTAGES

MTTL III circuits incorporate an active bypass network in the base circuit of the output-pulldown transistor. This bypass circuit lowers the impedance for the base turnoff current of the lower output transistor thus providing a faster turnoff. The faster turnoff reduces the time that the output transistors are simultaneously in their active regions. Thus, there is a narrower current spike during switching, and the ac power dissipation is reduced. An additional advantage of the bypass network is a more nearly square transfer characteristic (see Figure 4) which approximates that obtained with MDTL devices.

BYPASS OPERATION

In conventional TTL logic designs, a resistor is designed in from the emitter to ground in the phase splitting transistor, Q2 (See Figure 2). Thus when the base voltage rises above cutoff in this transistor, current flows in the collector circuit. The resulting voltage drop at the collector begins to turn OFF the Darlington output on the upper half of the circuit. The pulldown transistor, Q4, does not start to turn ON until its cutoff voltage is reached. Thus, the switching transition is spread over about 0.8 volt as seen in Figure 4.

When the active bypass is added, voltage at the base of the phase-splitter must rise to two base-emitter cutoff voltages before any current will flow in its collector circuit. Both the bypass transistor, Q6, and the pulldown transistor, Q4, remain in cutoff until this voltage is reached and thus constitute a high impedance path from the emitter of Q2 to ground. Negligible current flows in Q2 until the pulldown transistor turns ON. Consequently, the voltage drop at the collector of Q2, and therefore the "turnoff" of the Darlington pair coincides with the "turnon" of the pulldown transistor and the transfer characteristic is more nearly square.

The bypass network also increases switching speed. When the output is in the zero state, the pulldown transistor is ON and in saturation. In order to cut this transistor OFF, the stored charge must be pulled out of its base. Conventionally, this charge is leaked out at an R-C time con-

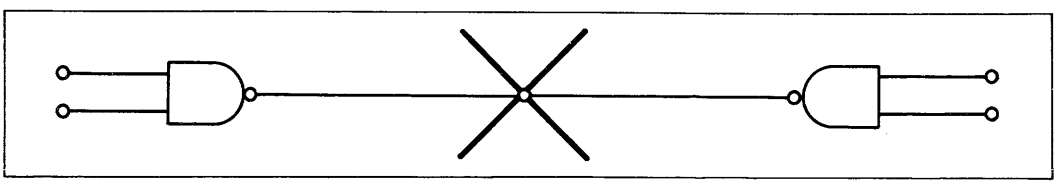


FIGURE 3A – The Outputs of MTTL Gates May not be Tied Together

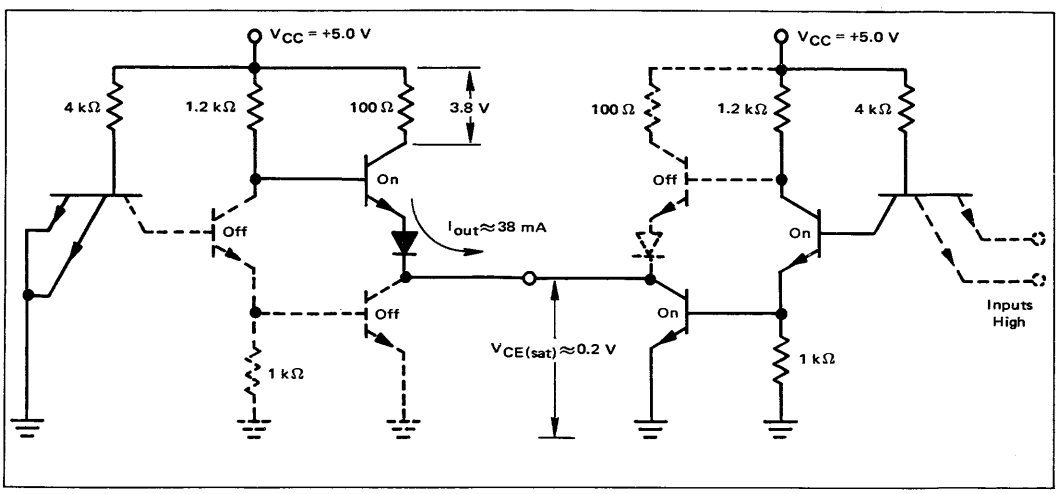


FIGURE 3B – With the Totem Pole Output, Excessive Output Current May be Drawn if this Restriction is Ignored

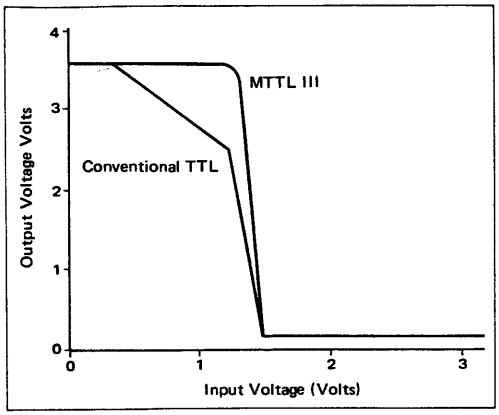


FIGURE 4 – Comparison of Conventional TTL and MTTL III Series Transfer Characteristics

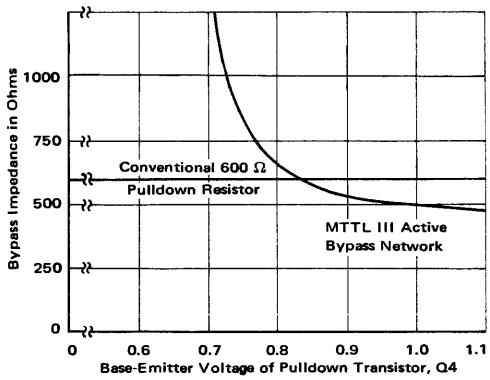


FIGURE 5 – Comparison of Active Bypass Network Impedance to a Fixed Resistor

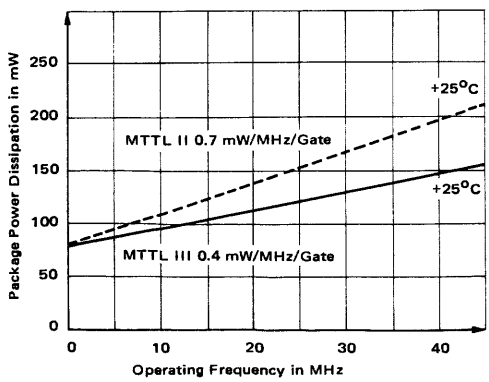
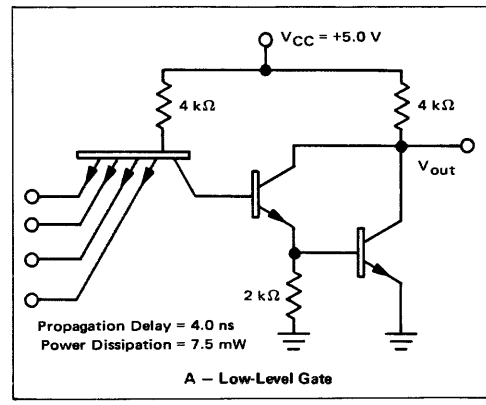


FIGURE 6 – MTTL III versus MTTL II AC Power Dissipation Comparison for Quad 2-Input NAND Gates

stant through a "pulldown" resistor from its base to ground or to a negative voltage. As seen in Figure 5, the bypass provides a low "pulldown" impedance resulting in a faster shutdown. A significant ac power decrease results because the current spikes which occur during switching have a narrower pulse width. A comparison is shown in Figure 6.

MOTOROLA COMPLEX FUNCTIONS: THE MC4000 SERIES

The MTTL MC4000 series of complex functions is designed for general purpose, medium-and high-speed digital applications requiring clock frequencies up to the 30-to 40-MHz range. The MSI (Medium Scale Integration) complexity of these devices allows significant reductions in package count, space, assembly cost, and cost per logical decision. In addition, the MC4000 series MSI devices offer increased speed at lower dissipation for identical functions.



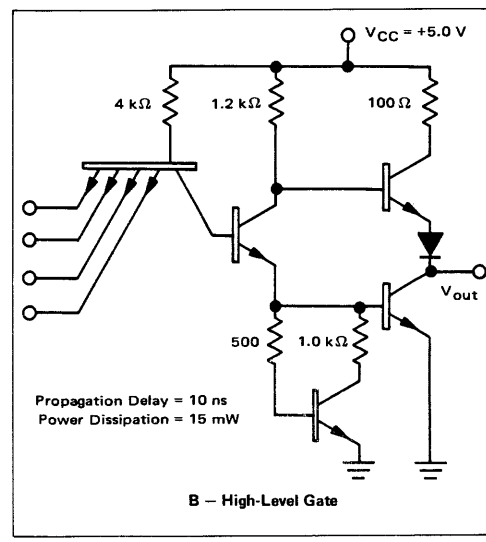


FIGURE 7 – Building Blocks for MC4000 Series Complex Functions

The MC4000 series is compatible with all the MTTL and MDTL lines. Input and output loading data are given (Appendix A) in terms of MTTL and MDTL devices so that the designer can intermix them with a minimum of difficulty.

The MC4000 series utilizes two forms of the TTL gates. Shown in Figure 7 are the low-level gate (7A), a very high-speed low-power gate useful within the device itself to drive the internal circuitry not requiring high fanout capabilities, and a high-level gate (7B) with the MTTL bypass used to drive loads on the output pins.

The low level Darlington circuit, with its non-saturating output device, was chosen for several reasons.

1. The total ON and OFF power when used internally, is approximately equal which tends to keep the package power constant as a function of the logic applied. The generation of switching noise is also reduced.

2. The switching times (t_{on} and t_{off}) are balanced allowing more constant propagation delays with respect to input logic.

3. The speed deviation with respect to power supply and temperature is minimal.

4. The input threshold voltage is compatible with the existing gate functions.

5. The variation of the "low" level with fanout is small because of the low impedance.

This gate has an ON level of $V_{be} + V_{offset}$. Figure 4 compares the actual transfer characteristic of a conventional TTL gate to the transfer characteristic of a MTTL gate with the bypass network previously discussed. If the ON level voltage of the low level Darlington Network is applied to a conventional TTL gate, the input voltage would be beyond the first breakpoint. This results in a lowering of the high output level. To achieve the maximum high level consistent with the standard gates, the configuration of Figure 7B is used. This high level gate has a bypass network so that the resulting voltage transfer characteristic has the improved shape shown in Figure 4 for the MTTL III series.

CONCLUSION

This application note has given a general description and comparison of Motorola's MTTL I, MTTL II, MTTL III, MTTL 5400/7400 and the MC4000 lines. The basic gates and the bypass circuit have been discussed along with existing and proposed complex functions in the MC4000 series. An appendix has been included which defines some of the more important terms used to specify device characteristics.

APPENDIX A

EFFECT OF INPUT DIODES

Due to high speeds of operation TTL generates large values of current and voltage rates of change. A 1 volt change in approximately 1.3 nanoseconds for the rise time and a 1 volt change in about 1.0 nanoseconds for the fall time, provides $\frac{dV}{dt}$ rates on the order of 10^9 volts per second. With these rates of change, undershoot exceeding 2 volts can develop in the system which can cause problems in succeeding circuits. Two very serious problems result from the possible undershoot. First false triggering of the following stage is possible since a positive overshoot follows the large undershoot. This positive overshoot may act as a "high" signal and turn on the following stage for a short period of time. Diodes on inputs limit the negative value of the undershoot dissipating the ringing energy and thereby limit the positive overshoot. Figure A1 shows the effect of adding the clamp diodes on inputs of TTL gates at the end of a 93 ohm line. It can be seen that without clamp diodes the positive overshoot has turned the following gate ON momentarily. The second problem results if the unused inputs of a gate are returned to the supply voltage and a negative undershoot in excess of 2 volts occurs. These reversed biased emitters may break down and draw excessive current which creates noise in the system.

LOADING RULES FOR MC4000 SERIES COMPLEX FUNCTIONS

The characteristics of the MC4000 series, were defined so that loading rules could be calculated for using the MC4000 series with any of the TTL families that are available from Motorola. In addition, rules were established for using MC4000 devices with the MDTL family. The loading rules for interfacing with the various product lines are based on worst case conditions for each family. Worst case conditions for determining output loading factors (fan out) are defined as operation at minimum low state output current (I_{OL} at $V_{OL} \leq 0.4$ V at minimum supply voltage (V_{CC}) for the MC4000 series) while driving another series of industrial grade devices at maximum forward current (I_F). Under the specified conditions, the fan outs

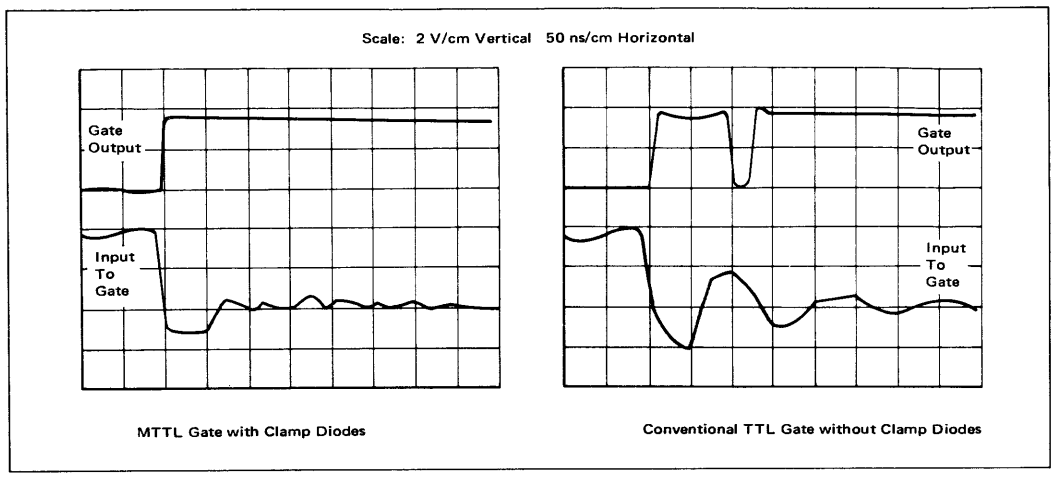


FIGURE A1 – Effect of Clamp Diodes on Inputs of an MTTL Gate at the end of a 93-Ohm Line

for MC4000 circuits driving other MC4000, MTTL, or MDTL devices are listed below.

OUTPUT LOADING FACTORS

MC4000 Driving MC4000

V_{OL} = 0.4 Vdc at I_{OL} = 16 mAdc, V_{CC} = 4.75 Vdc
(I_F = 1.6 mAdc max at V_{CC} = 5.5 Vdc)
F.O. = 10

MC4000 Driving MTTL I

V_{OL} = 0.4 Vdc at I_{OL} = 16 mAdc, V_{CC} = 4.75 Vdc
(I_F = 1.66 mAdc at V_{CC} = 5.0 Vdc)
F.O. = 9 MTTL I Gates

MC4000 Driving MTTL II

V_{OL} = 0.4 Vdc at I_{OL} = 16.0 mAdc, V_{CC} = 4.75 Vdc
(I_F = 2.5 mAdc at V_{CC} = 5.0 Vdc)
F.O. = 6 MTTL II Gates

MC4000 Driving MTTL III

V_{OL} = 0.4 Vdc at I_{OL} = 16 mAdc, V_{CC} = 4.75 Vdc
(I_F = 2.3 mAdc at V_{CC} = 5.5 Vdc)
F.O. = 6 MTTL III Gates

MC4000 Driving MC7400

V_{OL} = 0.4 Vdc at I_{OL} = 16 mAdc, V_{CC} = 4.75 Vdc
(I_F = 1.6 mAdc at V_{CC} = 5.25 Vdc)
F.O. = 10 MC7400 Gates

MC4000 Driving MC830 MDTL

V_{OL} = 0.4 Vdc at I_{OL} = 16 mAdc, V_{CC} = 4.75 Vdc
(I_F = 1.4 mAdc at V_{CC} = 5.0 Vdc)
F.O. = 11 MC830 Gates

The above fan outs are determined by expressing MC4000 characteristics in terms of the devices interfaced, therefore, the numbers vary according to the driven element. It should be emphasized that these are worst case factors and they may be improved by using the higher grade devices in the particular family or by maintaining identical voltages at the supply terminals.

INPUT LOADING FACTORS

Input loading factors referenced to each product line are listed below. The input loading factor relative to the MC830 applies only to gates with two kilohm pull-up resistors. Because of high state current limitations MC830 gates with six kilohm pull-ups can only drive three MC4000 inputs.

DRIVING ELEMENT	INPUT CHARACTERISTICS OF DRIVING ELEMENT	MC4000 INPUT LOADING FACTOR
MC4000	I_F = 1.6 mAdc, V_{CC} = 5.5 Vdc, V_F = 0.4 Vdc	1.0
MTTL I	I_F = 1.66 mAdc, V_{CC} = 5.0 Vdc, V_F = 0 Vdc	1.0
MTTL II	I_F = 2.5 mAdc, V_{CC} = 5.0 Vdc, V_F = 0 Vdc	0.67
MTTL III	I_F = 2.3 mAdc, V_{CC} = 5.5 Vdc, V_F = 0.4 Vdc	0.7
MC7400	I_F = 1.6 mAdc, V_{CC} = 5.25 Vdc, V_F = 0.4 Vdc	1.0
MC830	I_F = 1.4 mAdc, V_{CC} = 5.0 Vdc, V_F = 0 Vdc	1.15

APPENDIX B

DEFINITIONS OF COMMON MTTL TERMS

AC Measurements

t_+ or t_r (Rise Time): Time differential between the 1 and 2 volt or 10% to 90% points on the output during a transition to a logical "1" state.

t_- or t_f (Fall Time): Time differential between the 2 and 1 volt or 90% to 10% points on the output during a transition to a logical "0" state.

t_{pd+} or $t_{d(off)}$: Time differential from the 1.5 volt point of the input to the 1.5 volt of the output transition to a logical "1" state.

t_{pd-} or $t_{d(on)}$: Time differential from the 1.5 volt point of the input to the 1.5 volt point of the output transition to a logical "0" state.

$t_{pd} = \frac{(t_{pd-}) + (t_{pd+})}{2}$: Average transition time.

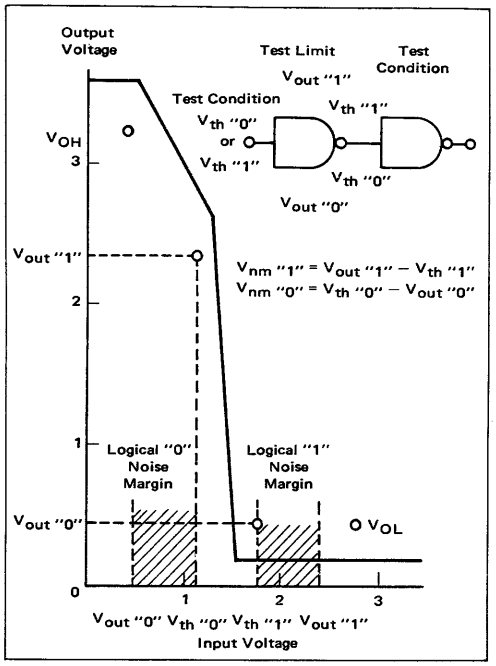


FIGURE B1 – Logical "0" and "1" Noise Margins

DC Noise Immunity

Logical "1" noise margin is defined as the difference between guaranteed minimum output voltage in the "1" state and the threshold voltage (V_{th} "1") for the 1 to 0 transition (See Figure B1).

Logical "0" noise margin is the difference between the guaranteed maximum output voltage in the "0" state and the threshold voltage (V_{th} "0") for the 0 to 1 transition.

Flip-Flop Set-Up and Hold Times

Flip-flop set-up time is defined as the time a data signal must be present on the input before the clock transition in order for proper operation to occur (See Figure B2).

Hold time is the time a data signal must be present on the input after the clock transition to assure proper operation. (See sketch).

Setup and hold times frequently differ depending on whether the transition is to the high or the low output state.

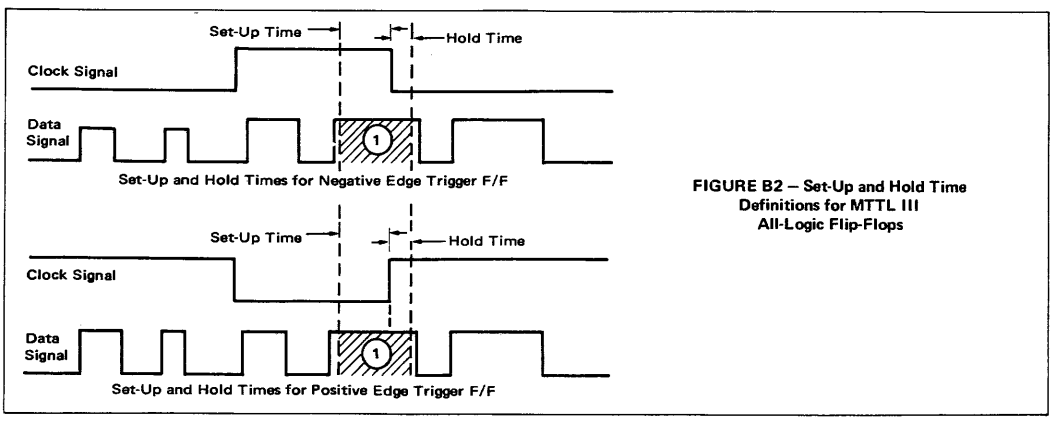


FIGURE B2 – Set-Up and Hold Time Definitions for MTTL III All-Logic Flip-Flops