Volume 6 / Series B

Semiconductor Data Library

LINEAR INTEGRATED CIRCUITS

MOTOROLA Semiconductor Products Inc.

Volume 6/Series B

prepared by
Technical Information Center

Semiconductor Data Library

LINEAR INTEGRATED CIRCUITS

This Linear Integrated Circuit Data Book contains data sheets for one of the largest selections of linear ICs in the industry. Included are devices that were developed by the various Motorola R&D groups, as well as an extensive second-source inventory of the most popular circuits developed elsewhere. The data sheets are arranged by product or market category.

To provide the user with a quick overview of Motorola's complete line of standard linear ICs, a number of selector guides separate the total line into market or product divisions. This provides a quick comparison of similar devices, spelling out the most signficant differences. Also included are a cross-reference table of second-source devices and other product-related information.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent rights of any manufacturer.

Series B

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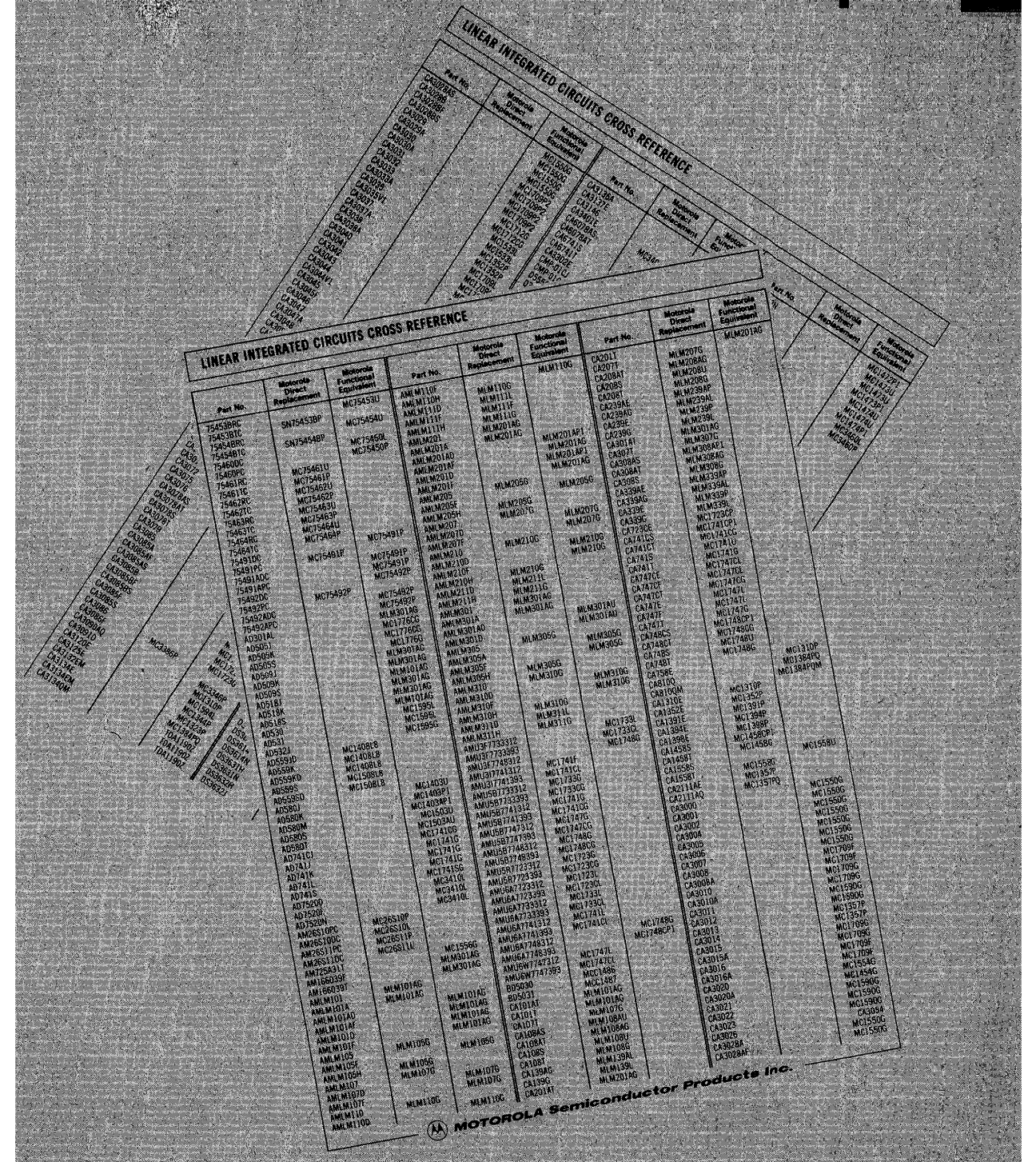

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MOTOROLA — LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

. . . provides a complete interchangeability list linking over 6000 devices offered by most major Linear Integrated Circuits manufacturers to the nearest equivalent Motorola device. The Motorola "Direct Replacement" column lists devices with identical pin connections and package and the same or better electrical characteristics and temperature range. The Motorola "Functional Replacement" column provides a device which performs the same function but with possible differences in package configurations, pin connections, temperature range or electrical specifications.

Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
709BE	MC1709G	
709BH	MC1709F	
709CE	MC1709CG	
709CH	MC1709CF	
709CJ	MC1709CP2	
710BE	MC1710G	
710BH	MC1710F	
710CE	MC1710CG	
711BE	MC1711G	
711BH	MC1711F	
711BN	MC1711L	
711CE	MC1711CG	
711CJ	MC1711CP	
723BE	MC1723G	
723CE	MC1723CG	
723CJ	MC1723CL	
741BE	MC1741G	
741BH	MC1741F	
741BN	MC1741L	
741CE	MC1741CG	
747BE		MC1747G
747BN		MC1747L
747CE		MC1747CG
748BE		MC1748G
748CE		MC1748CG
809BE		MC1776G
809CE		MC1776CG
823AE		MC1723G
1458CE	MC1458CG	
3232		MC3232AL
3245	MC3245L	
5524DM	MC5524L	
5525DM	MC5525L	
5528DM	MC5528L	
5529DM	MC5529L	
5534DM	MC5534L	
5535DM	MC5535L	
5538DM	MC5538L	
5539DM	MC5539L	
6605J		MC3443P
6605L		MC3443L
7524DC	MC7524L	
7524PC	MC7524P	
7525DC	MC7525L	
7525PC	MC7525P	
7528DC	MC7528L	
7528PC	MC7528P	
7529DC	MC7529L	
7529PC	MC7529P	
7534DC	MC7534L	
7534PC	MC7534P	
7535DC	MC7535L	
7535PC	MC7535P	
7538DC	MC7538L	
7538PC	MC7538P	
7539DC	MC7539L	
7539PC	MC7539P	
8216		MC8T26L
8226		MC8T28L
9614DC		MC75110L
9614DM		MC75110L
9614FM		MC75110L
9615DC		MC75108L
9615DM		MC55108L
9615FM		MC55108L
9616CDC		MC1488L
9616EDC		MC1488L
9616DM		MC1488L
9617DC		MC1489AL
9620DC		MC75110L
9620DM		MC75110L
9621DC		MC75108L
9621DM		MC55108L
9622DC		MC75140P1
9622DM		MC75140P1
9624DC		MMH0026CL
9624DM		MMH0026CL
9625DC		MMH0026CL
9625DM		MMH0026CL
9627CDC		MC1489AL
9627DM		MC1489AL
9636T	MC3488P	
9637T	MC3486P	
9638T	MC3487P	
9640J	MC3443P	
9640D		MC3443P
9640DC		MC3440P
9640NC	MC3440P	
9665PC	MC1411P	
9666PC	MC1412P	
9667PC	MC1413P	
9668PC	MC1416P	
9665DC	MC1411L	
9666DC	MC1412L	
9667DC	MC1413L	
9668DC	MC1416L	
55107ADM	MC55107L	
55108ADM	MC55108L	
55107BDM		MC55107L
55108BDM		MC55108L
55110DM		MC75110L
55121DM		MC8T13L
55122DM		MC8T14L
55207DM		MC55107L
55208DM		MC55108L
55224DM		MC5524L
55225DM		MC5525L
55232DM		MC5528L
55233DM		MC5529L
55234DM		MC5534L
55235DM		MC5535L
55238DM		MC5538L
55239DM		MC5539L
55325DM	MC55325L	
55325FM	MC55325F	
75107ADC	MC75107L	
75107BDC		MC75107L
75107APC	MC75107P	
75107BPC		MC75107P
75108ADC	MC75108L	
75108BDC		MC75108L
75108APC	MC75108P	
75108BPC		MC75108P
75110DC	MC75110L	
75110PC	MC75110P	
75121DC	MC8T13L	
75121PC	MC8T13P	
75122DC	MC8T14L	
75122PC	MC8T14P	
75123DC	MC8T23L	
75123PC	MC8T23P	
75124DC	MC8T24L	
75124PC	MC8T24P	
75207DC		MC75107L
75207PC		MC75107P
75208DC		MC75108L
75208PC		MC75108P
75224DC		MC7524L
75224PC		MC7524P
75225DC		MC7525L
75225PC		MC7525P
75232DC		MC7528L
75232PC		MC7528P
75233DC		MC7529L
75333PC		MC7529P
75234DC		MC7534L
75234PC		MC7534P
75235DC		MC7535L
75235PC		MC7535P
75238DC		MC7538L
75238PC		MC7538P
75239DC		MC7539L
75239PC		MC7539P
75325DC	MC75325L	
75325PC	MC75325P	
75450ADC	MC75450L	
75450APC	MC75450P	
75451APC	MC75451U	
75451ATC	MC75451P	
75452ARC	MC75452U	
75452ATC	MC75452P	
75453ARC	MC75453U	
75453ATC	MC75454P	
75454ARC	MC75454U	
75454ATC	MC75454P	
75450BDC		MC75450L
75450BPC		MC75450P
75451BRC		MC75451U
75451BTC	SN75451BP	
75452BRC		MC75452U
75452BTC	SN75452BP	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
75453BRC		MC75453U
75453BTC	SN75453BP	
75454BRC		MC75454U
75454BTC	SN75454BP	
7546ODC		MC75450L
75460PC		MC75450P
75461RC	MC75461U	
75461TC	MC75461P	
75462RC	MC75462U	
75462TC	MC75462P	
75463RC	MC75463U	
75463TC	MC75463P	
75464RC	MC75464U	
75464TC	MC75464P	
75491DC		MC75491P
75491PC	MC75491P	
75491ADC		MC75491P
75491APC		MC75491P
75492DC		MC75492P
75492PC	MC75492P	
75492ADC		MC75492P
75492APC		MC75492P
AD301AL		MLM301AG
AD505J		MC1776CG
AD505K		MC1776CG
AD505S		MC1776G
AD509J		MLM301AG
AD509K		MLM301AG
AD509S		MLM101AG
AD518J		MLM301AG
AD518K		MLM301AG
AD518S		MLM101AG
AD530		MC1595L
AD531		MC1595L
AD532J		MC1595G
AD559JD	MC1408L8	
AD559K	MC1408L8	
AD559KD	MC1408L8	
AD559S	MC1508L8	
AD559SD	MC1508L8	
AD580J		MC1403U
AD580K		MC1403P1
AD580M		MC1403AP1
AD580S		MC1503U
AD580T		MC1503AU
AD741CJ		MC1741CG
AD741J		MC1741G
AD741K		MC1741G
AD741L		MC1741G
AD741S		MC1741SG
AD752OD		MC3410L
AD752OF		MC3410L
AD752ON		MC3410L
AM26S10PC	MC26S10P	
AM26S10DC	MC26S10L	
AM26S11PC	MC26S11P	
AM26S11DC	MC26S11L	
AM725A31T		MC1556G
AM166039F		MLM301AG
AM166039T		MLM301AG
AMLM101	MLM101AG	
AMLM101A	MLM101AG	
AMLM101AD		MLM101AG
AMLM101AF		MLM101AG
AMLM101D		MLM101AG
AMLM101F		MLM101AG
AMLM105	MLM105G	
AMLM105F		MLM105G
AMLM105H	MLM105G	
AMLM107	MLM107G	
AMLM107D		MLM107G
AMLM107F		MLM107G
AMLM110	MLM110G	
AMLM110D		MLM110G
AMLM110F		MLM110G
AMLM110H	MLM110G	
AMLM111D	MLM111L	
AMLM111F	MLM111F	
AMLM111H	MLM111G	
AMLM201	MLM201AG	
AMLM201A	MLM201AG	
AMLM201AD		MLM201AP1
AMLM201AF		MLM201AG
AMLM201D		MLM201AP1
AMLM201F		MLM201AG
AMLM205	MLM205G	
AMLM205F		MLM205G
AMLM205H	MLM205G	
AMLM207	MLM207G	
AMLM207D		MLM207G
AMLM207F		MLM207G
AMLM210	MLM210G	
AMLM210D		MLM210G
AMLM210F		MLM210G
AMLM210H	MLM210G	
AMLM211D	MLM211L	
AMLM211H	MLM211G	
AMLM301	MLM301AG	
AMLM301A	MLM301AG	
AMLM301AD		MLM301AU
AMLM301D		MLM301AU
AMLM305	MLM305G	
AMLM305A		MLM305G
AMLM305F		MLM305G
AMLM305H	MLM305G	
AMLM310	MLM310G	
AMLM310D		MLM310G
AMLM310F		MLM310G
AMLM310H	MLM310G	
AMLM311D	MLM311L	
AMLM311H	MLM311G	
AMU3F7733312		MC1733L
AMU3F7733393		MC1733CL
AMU3F7748312		MC1748G
AMU3I7741312	MC1741F	
AMU3I7741393	MC1741CL	
AMU5B7733312	MC1733G	
AMU5B7733393	MC1733CG	
AMU5B7741312	MC1741G	
AMU5B7741393	MC1741CG	
AMU5B7747312	MC1747G	
AMU5B7747393	MC1747CG	
AMU5B7748312	MC1748G	
AMU5B7748393	MC1748CG	
AMU5R7723312	MC1723G	
AMU5R7723393	MC1723CG	
AMU6A7723312	MC1723L	
AMU6A7723393	MC1723CL	
AMU6A7733312	MC1733L	
AMU6A7733393	MC1733CL	
AMU6A7741312	MC1741L	
AMU6A7741393	MC1741CL	
AMU6A7748312		MC1748G
AMU6A7748393		MC1748CP1
AMU6W7747312	MC1747L	
AMU6W7747393	MC1747CL	
BD5030	MCC1486	
BD5031	MCC1487	
CA101AT	MLM101AG	
CA101T	MLM101AG	
CA107T	MLM107G	
CA108AS	MLM108AU	
CA108AT	MLM108AG	
CA108S	MLM108U	
CA108T	MLM108G	
CA139AG	MLM139AL	
CA139G	MLM139L	
CA201AT	MLM201AG	
CA201T		MLM201AG
CA207T	MLM207G	
CA208AT	MLM208AG	
CA208S	MLM208U	
CA208T	MLM208G	
CA239AE	MLM239AP	
CA239AG	MLM239AL	
CA239E	MLM239P	
CA239G	MLM239L	
CA301AT	MLM301AG	
CA307T	MLM307G	
CA308AS	MLM308AP1	
CA308AT	MLM308AG	
CA308S	MLM308G	
CA339AE	MLM339AP	
CA339AG	MLM339AL	
CA339E	MLM339P	
CA339G	MLM339L	
CA723CE	MC1723CP	
CA741CS	MC1741CP1	
CA741CT	MC1741CG	
CA741S	MC1741U	
CA741T	MC1741G	
CA747CE	MC1747CL	
CA747CF	MC1747CL	
CA747CT	MC1747CG	
CA747E	MC1747L	
CA747F	MC1747L	
CA747T	MC1747G	
CA748CS	MC1748CP1	
CA748CT	MC1748CG	
CA748S	MC1748U	
CA748T	MC1748G	
CA758E		MC1310P
CA810Q		MC1384PQ
CA810QM		MC1384PQM
CA1310E	MC1310P	
CA1352E	MC1352P	
CA1391E	MC1391P	
CA1394E	MC1394P	
CA1398E	MC1398P	
CA1458S	MC1458CP1	
CA1458T	MC1458G	
CA1558S		MC1558U
CA1558T	MC1558G	
CA2111AE	MC1357P	
CA2111AQ	MC1357PQ	
CA3000		MC1550G
CA3001		MC1550G
CA3002		MC1550G
CA3004		MC1550G
CA3005		MC1550G
CA3006		MC1550G
CA3007		MC1550G
CA3008		MC1709F
CA3008A		MC1709F
CA3010		MC1709G
CA3010A		MC1709G
CA3011		MC1590G
CA3012		MC1590G
CA3013		MC1357P
CA3014		MC1357P
CA3015		MC1709G
CA3015A		MC1709G
CA3016		MC1709F
CA3016A		MC1709F
CA3020		MC1554G
CA3020A		MC1454G
CA3021		MC1590G
CA3022		MC1590G
CA3023		MC1590G
CA3026		CA3054
CA3028A		MC1550G
CA3028AF		MC1550G

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
CA3028AS		MC1550G
CA3028B		MC1550G
CA3028BF		MC1550G
CA3028BS		MC1550G
CA3029		MC1709P2
CA3029A		MC1709P2
CA3030		MC1709P2
CA3030A		MC1709P2
CA3031		MC1712G
CA3032		MC1712CG
CA3033		MC1533L
CA3033A		MC1533L
CA3035		MC1352P
CA3035V1		MC1352P
CA3037		MC1709L
CA3037A		MC1709L
CA3038		MC1709L
CA3038A		MC1709L
CA3040		MC1510G
CA3041		MC1351P
CA3042		MC1357P
CA3043		MC1357P
CA3044		MC1364P
CA3044V1		MC1364P
CA3045		MC3346P
CA3045F		MC3346P
CA3046	MC3346P	
CA3047		MC1433L
CA3047A		MC1433L
CA3048		MC3301P
CA3052		MC3301P
CA3053		MC1550G
CA3053F		MC1550G
CA3053S		MC1550G
CA3054	CA3054	
CA3056	MC1741CG	
CA3056A	MC1741G	
CA3058		CA3059
CA3059	CA3059	
CA3064		MC1364P
CA3064E	MC1364P	
CA3065	MC1358P	
CA3066		MC1399P
CA3067		MC1323P
CA3068		MC1352P
CA3070		MC1399P
CA3071		MC1399P
CA3072		MC1323P
CA3075	MC1375P	
CA3076		MC1590G
CA3078AS		MC1776G
CA3078AT		MC1776G
CA3078S		MC1776CG
CA3078T		MC1776CG
CA3079		CA3059
CA3085		MC1723G
CA3085A		MC1723G
CA3085AF		MC1723L
CA3085AS		MC1723G
CA3085B		MC1723G
CA3085BF		MC1723L
CA3085BS		MC1723G
CA3085F		MC1723L
CA3085S		MC1723G
CA3086	MC3386P	
CA3086F		MC3346P
CA3090AQ		MC1310P
CA3091D		MC1594L
CA3120E		MC1344P
CA3125E		MC1323P
CA3132EM		MC1384PQ
CA3134E		TDA1190Z
CA3134EM		TDA1190Z
CA3134QM		TDA1190Z
CA3136A		MC3346P
CA3137E		MC1323P
CA3146		MC3346P
CA3401E	MC3401P	
CA6078AS		MC1776G
CA6078AT		MC1776G
CA6741S		MC1776G
CA6741T		MC1776G
CA3302E	MC3302P	
CMP-01CJ		MC1556G
CMP-01CP		MC1556P
D555CJ		MC1555G
D3232	MC3232AP	
D3245	MC3245P	
D8216		MC8T26L
D8226		MC8T28L
DAC-01		MC1506L
DAC-08		MC1408L8
DM7820AD		MC75140P1
DM7820J		MC75140P1
DM7822J		MC1489AL
DM7837J		MC3437L
DM7838J		MC3438L
DM7887J		MC3490P
DM7887N		MC3490P
DM7889J		MC3491P
DM7889N		MC3491P
DM7897J		MC3494P
DM7897N		MC3494P
DM8820AN		MC75140P1
DM8820J		MC75140P1
DM8820N		MC75140P1
DM8822J		MC1489AL
DM8822N		MC1489AP
DM8837N	MC3437P	
DM8838N	MC3438P	
DM8861N		MC75491P
DM8863N		MC75492P
DM8887J		MC3490P
DM8889J		MC3491P
DM8897J		MC3494P
DM75491N	MC75491P	
DM75492N	MC75492P	
DS0026CG		MMH0026CG
DS0026CH	MMH0026CG	
DS0026CJ	MMH0026CL	
DS0026CN	MMH0026CP1	
DS0026G		MMH0026G
DS0026H	MMH0026G	
DS0026J	MMH0026L	
DS0056CG		MMH0026CG
DS0056CH		MMH0026CG
DS0056CJ		MMH0026CL
DS0056CN		MMH0026CP1
DS0056G		MMH0026G
DS0056H		MMH0026G
DS0056J		MMH0026L
DS1488J	MC1488L	
DS1489AJ	MC1489AL	
DS1489J	MC1489L	
DS3486N	MC3486P	
DS3687N	MC3487P	
DS3611H		MC1471U
DS3611N		MC1471P1
DS3612H		MC1472U
DS3612N		MC1472P1
DS3613H		MC1473U
DS3613N		MC1473P1
DS3614H		MC1474U
DS3614N		MC1474P1
DS3631H		MC1471U
DS3631N		MC1471P1
DS3632H		MC1472U
DS3632J		MC1472U
DS3632N		MC1472P1
DS3633H		MC1473U
DS3633J		MC1473U
DS3633N		MC1473P1
DS3634H		MC1474U
DS3634J		MC1474U
DS3634N		MC1474P1
DS3644J		MC3460L
DS3644N		MC3460P
DS3650J	MC3450L	
DS3650N	MC3450P	
DS3651J	MC3430L	
DS3651N	MC3430P	
DS3652J	MC3452L	
DS3652N	MC3452P	
DS3653J	MC3432L	
DS3653N	MC3432P	
DS3674J	MC3460L	
DS3674N	MC3460P	
DS55107J	MC55107L	
DS55107W		MC55107L
DS55108J	MC55108L	
DS55108W		MC55108L
DS55110J		MC75110L
DS55121J		MC8T13L
DS55121W		MC8T13L
DS55122J		MC8T14L
DS55122W		MC8T14L
DS5524AJ	MC5524AL	
DS5524J	MC5524L	
DS5525J	MC5525L	
DS5528AJ	MC5528AL	
DS5528J	MC5528L	
DS5529J	MC5529L	
DS55325J	MC55325L	
DS55325W	MC55325F	
DS5534AJ	MC5534AL	
DS5534J	MC5534L	
DS5535J	MC5535L	
DS5538AJ	MC5538AL	
DS5538J	MC5538L	
DS5539J	MC5539L	
DS75107J	MC75107L	
DS75107N	MC75107P	
DS75108J	MC75108L	
DS75108N	MC75108P	
DS75109N	MC75109P	
DS75110J	MC75110L	
DS75110N	MC75110P	
DS75121J	MC8T13L	
DS75121N	MC8T13P	
DS75122J	MC8T14L	
DS75122N	MC8T14P	
DS75123J	MC8T23L	
DS75123N	MC8T23P	
DS75124J	MC8T24L	
DS75124N	MC8T24P	
DS75207J		MC75107L
DS75207N		MC75107P
DS75208J		MC75108L
DS75208N		MC75108P
DS7520AJ	MC7520AL	
DS7520AN	MC7520AP	
DS7524AJ	MC7524AL	
DS7524AN	MC7524AP	
DS7524J	MC7524L	
DS7524N	MC7524P	
DS7525J	MC7525L	
DS7525N	MC7525P	
DS7528AJ	MC7528AL	
DS7528AN	MC7528AP	
DS7528J	MC7528L	
DS7528N	MC7528P	
DS7529J	MC7529L	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
DS7529N	MC7529P	
DS75325J	MC75325L	
DS75325N	MC75325P	
DS7534AJ	MC7534AL	
DS7534AN	MC7534AP	
DS7534J	MC7534L	
DS7534N	MC7534P	
DS7535J	MC7535L	
DS7535N	MC7535P	
DS75365J	MC75365L	
DS75365N	MC75365P	
DS7538AJ	MC7538AL	
DS7538AN	MC7538AP	
DS7538J	MC7538L	
DS7538N	MC7538P	
DS7539J	MC7539L	
DS7539N	MC7539P	
DS75450J	MC75450L	
DS75450N	MC75450P	
DS75451H		MC75451U
DS75451N	SN75451BP	
DS75452H		MC75452U
DS75452N	SN75452BP	
DS75453H		MC75453U
DS75453N	SN75453BP	
DS75454H		MC75454U
DS75454N	SN75454BP	
DS75461H		MC75461U
DS75461N	MC75461P	
DS75462H		MC75462U
DS75462N	MC75462P	
DS75463H		MC75463U
DS75463N	MC75463P	
DS75464H		MC75464U
DS75464N	MC75464P	
DS75491J		MC75491P
DS75491N	MC75491P	
DS75492J		MC75492P
DS75492N	MC75492P	
DS7837J		MC3437L
DS7837W		MC3437L
DS7838J		MC3438L
DS7838W		MC3438L
DS7887J		MC3490P
DS7889J		MC3491P
DS7897J		MC3494P
DS8833J		MC8T28L
DS8833N		MC8T28P
DS8834J		MC8T26L
DS8834N		MC8T26P
DS8835J		MC8T26L
DS8835N		MC8T26P
DS8837J	MC3437L	
DS8837N	MC3437P	
DS8838J	MC3438L	
DS8838N	MC3438P	
DS8839J		MC8T28L
DS8839N		MC8T28P
DS8887J		MC3490P
DS8887N		MC3490P
DS8889J		MC3491P
DS8889N		MC3491P
DS8897J		MC3494P
DS8897N		MC3494P
ICB8000C		MLM111L
ICB8001C		MLM111L
ICB8741C		MC1741CG
ICH8500ATV		MC1776CG
ICH8500TV		MC1776CG
ICL101ALNDP		MLM101AG
ICL101ALNFB		MLM101AG
ICL101ALNTY		MLM101AG
ICL301ALNPA		MLM301AG
ICL301ALNTY		MLM301AG
ICL741CLNPA		MC1741CP1
ICL741CLNTY		MC1741CP1
ICL741LNDP		MC1741L
ICL741LNFB		MC1741L
ICL741LNTY		MC1741L
ICL8001CTZ		MLM111L
ICL8001MTZ		MLM111L
ICL8007CTA		MC1709CG
ICL8007MTA		MC1709CG
ICL8008CPA		MLM301AP1
ICL8008CTY		MLM301AP1
ICL8013A		MC1594G
ICL8013B		MC1594G
ICL8013C		MC1594G
ICL8017CTW		MLM301AP1
ICL8017MTW		MLM301AP1
ICL8021C		MC1776G
ICL8021M		MC1776G
ICL8022C		MC1776G
ICL8022M		MC1776G
ICL8043CDE		MC1776G
ICL8043CPE		MC1776G
ICL8043MDE		MC1776G
ICL8048CDE		MC1776G
ICL8048DPE		MC1776G
IH5101IIE		MC1545G
IH5101MIE		MC1545G
ITT641		MC1385P
ITT652	MC1411P	
ITT654	MC1412P	
ITT656	MC1413P	
ITT1330	MC1330P	
ITT1352	MC1352P	
ITT3064	MC1364P	
ITT3065	MC1358P	
ITT3066		MC1399P
ITT3701		TDA1190Z
ITT3707		MC1399P
ITT3710		MC1391P
ITT3714		MC1394P
L144AP		MLM324P
L201	MC1411P	
L202	MC1412P	
L203	MC1413P	
LD110CJ		MC14435VP
LD111CJ	MC1405L	
LD114CR		MC14435VR
LF152D		LF155U
LF155AH	LF155AH	
LF155AJG	LF155AJ-8	
LF155AL	LF155AH	
LF155H	LF155H	
LF155JG	LF155J-8	
LF155L	LF155H	
LF156AH	LF156AH	
LF156AJG	LF156AJ-8	
LF156AL	LF156AH	
LF156H	LF156H	
LF156JG	LF156J-8	
LF156L	LF156H	
LF157AH	LF157AH	
LF157AJG	LF157AJ-8	
LF157AL	LF157AH	
LF157H	LF157H	
LF157JG	LF157J-8	
LF157L	LF157H	
LF252D		LF155U
LF255H	LF155H	
LF255JG	LF155J-8	
LF255L	LF155H	
LF255P	LF155J-8	
LF256H	LF156H	
LF256JG	LF156J-8	
LF256L	LF156H	
LF256P	LF156J-8	
LF257H	LF157H	
LF257JG	LF157J-8	
LF257L	LF157H	
LF257P	LF157J-8	
LF352D		LF355U
LF355AH	LF355AH	
LF355AJG	LF355AJ-8	
LF355AL	LF355AH	
LF355AP	LF355AN	
LF355H	LF355H	
LF355JG	LF355J-8	
LF355L	LF355H	
LF355N	LF355N	
LF355P	LF355N	
LF356AH	LF356AH	
LF356AL	LF356AH	
LF356AJG	LF356AJ-8	
LF356AP	LF356AN	
LF356H	LF356H	
LF356JG	LF356J-8	
LF356L	LF356H	
LF356N	LF356N	
LF356P	LF356N	
LF357AH	LF357AH	
LF357H	LF357H	
LF357JG	LF357J-8	
LF357L	LF357H	
LF357N	LF357N	
LF357P	LF357N	
LH0001ACH		MC1776CG
LH0001AH		MC1776G
LH0001ACD		MC1776CG
LH0001AD		MC1776G
LH0001ACF		MC1776CG
LH0001AF		MC1776G
LH0002CH		MC1538R
LH0002H		MC1538R
LH0004CH		MC1436G
LH0004H		MC1536G
LH0042CH		MC1776G
LH101F		MC1741F
LH101H		MC1741G
LH201F		MC1741F
LH201H		MC1741G
LH740ACH		LF355H
LH740AH		LF155H
LH2101AD		MC1537L
LH2101AF		MC1537L
LH2201AD		MC1537L
LH2201AF		MC1537L
LH2301AD		MC1437L
LH2301AF		MC1437L
LM100F		MLM105G
LM100H		MLM105G
LM101AD		MLM101AG
LM101AF		MLM101AG
LM101AH	MLM101AG	
LM101AJ		MLM101AU
LM101AJ-14		MLM101AU
LM101AJG	MLM101AU	
LM101AL	MLM101AG	
LM101D		MLM101AU
LM101F		MLM101AG
LM101H	MLM101AG	
LM101J-14		MLM101AU
LM102H	MLM110G	
LM104F		MLM104G
LM104H	MLM104G	
LM104J		MLM104G
LM104L	MLM104G	
LM105F		MLM105G
LM105H	MLM105G	
LM105JG		MLM105G

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
LM105L	MLM105G	
LM106H		MC1710G
LM107D		MLM107U
LM107F		MLM107G
LM107H	MLM107G	
LM107J	MLM107U	
LM107J-14		MLM107U
LM107JG	MLM107U	
LM107L	MLM107G	
LM108AD	MLM108AL	
LM108AF	MLM108AF	
LM108AH	MLM108AG	
LM108AJ	MLM108AU	
LM108D	MLM108L	
LM108F	MLM108F	
LM108H	MLM108G	
LM109H	MLM109G	
LM109K	MLM109K	
LM109LA	MLM109K	
LM110D		MLM110G
LM110F		MLM110G
LM110H	MLM110G	
LM111D	MLM111L	
LM111F	MLM111F	
LM111H	MLM111G	
LM112D		MC1556L
LM112F		MC1556L
LM112H		MC1556G
LM117H	LM117H	
LM117K	LM117K	
LM118D		MC1741SL
LM118F		MC1741SL
LM118H		MC1741SG
LM120H-5.0		MC7905CK
LM120H-5.2		MC7905.2CK
LM120H-6.0		MC7906CK
LM120H-8.0		MC7908CK
LM120H-12		MC7912CK
LM120H-15		MC7915CK
LM120H-18		MC7918CK
LM120H-24		MC7924CK
LM120K-5.0		MC7905CK
LM120K-5.2		MC7905.2CK
LM120K-6.0		MC7906CK
LM120K-8.0		MC7908CK
LM120K-12		MC7912CK
LM120K-15		MC7915CK
LM120K-18		MC7918CK
LM120K-24		MC7924CK
LM122F		MC1555G
LM122H		MC1555G
LM123K	LM123K	
LM124AD		MLM124L
LM124AF		MLM124L
LM124AJ		MLM124L
LM124D	MLM124L	
LM124F		MLM124L
LM124J	MLM124L	
LM125H		MC1568G
LM126H		MC1568G
LM128H		MC1568G
LM139AD	MLM139AL	
LM139AJ	MLM139AL	
LM139D	MLM139L	
LM139J	MLM139L	
LM140LAH-5.0		MC78L05ACG
LM140LAH-6.0		MC78L06ACG
LM140LAH-8.0		MC78L08ACG
LM140LAH-12		MC78L12ACG
LM140LAH-15		MC78L15ACG
LM140LAH-18		MC78L18ACG
LM140LAH-24		MC78L24ACG
LM143D		MC1536G
LM143F		MC1536G
LM143H		MC1536G
LM145K		MC7905CK
LM148D	MC4741L	
LM148F		MC4741L
LM149D		MC4741L
LM149F		MC4741L
LM158AH		MLM158G
LM158H	MLM158G	
LM158JG	MLM158U	
LM158L	MLM158G	
LM163J		MC3450L
LM171H		MC1590G
LM200F		MLM205G
LM200H		MLM205G
LM201AD		MLM201AU
LM201AF		MLM201AG
LM201AH	MLM201AG	
LM201AJ		MLM201AU
LM201AJG	MLM201AU	
LM201AL	MLM201AG	
LM201AN		MLM201AP1
LM201AP	MLM201AP1	
LM201AJ-14		MLM201AU
LM201D		MLM201AU
LM201F		MLM201AG
LM201H	MLM201AG	
LM201J	MLM201AU	
LM201J-14		MLM201AU
LM202H	MLM210G	
LM204H	MLM204G	
LM204F		MLM204G
LM205F		MLM205G
LM205H	MLM205G	
LM206H		MC1710CG
LM207D		MLM207U
LM207F		MLM207G
LM207H	MLM207G	
LM207J	MLM207U	
LM207J-14		MLM207U
LM208AD	MLM208AL	
LM208AF	MLM208AF	
LM208AH	MLM208AG	
LM208AJ	MLM208AU	
LM208D		MLM208U
LM208F	MLM208F	
LM208H	MLM208G	
LM209K	MLM209K	
LM209H	MLM209G	
LM210D		MLM210G
LM210F		MLM210G
LM210H	MLM210G	
LM211D	MLM211L	
LM211F	MLM211F	
LM211H	MLM211G	
LM212D		MC1556L
LM212F		MC1556L
LM212H		MC1456G
LM217H	LM117H	
LM217K	LM117K	
LM218D		MC1741SL
LM218F		MC1741SL
LM218H		MC1741SG
LM220H-5.0		MC7905CK
LM220H-5.2		MC7905.2CK
LM220H-6.0		MC7906CK
LM220H-8.0		MC7908CK
LM220H-12		MC7912CK
LM220H-15		MC7915CK
LM220H-18		MC7918CK
LM220H-24		MC7924CK
LM220K-5.0		MC7905CK
LM220K-5.2		MC7905.2CK
LM220K-6.0		MC7906CK
LM220K-8.0		MC7908CK
LM220K-12		MC7912CK
LM220K-15		MC7915CK
LM220K-18		MC7918CK
LM220K-24		MC7924CK
LM222H		MC1555G
LM223K	LM123K	
LM224AD		MLM224L
LM224AF		MLM224L
LM224AJ		MLM224L
LM224D	MLM224L	
LM224F		MLM224L
LM224J	MLM224L	
LM225H		MC1568G
LM226H		MC1568G
LM228H		MC1568G
LM239AD	MLM239AL	
LM239AJ	MLM239AL	
LM239D	MLM239L	
LM239J	MLM239L	
LM240LAH-5.0		MC78L05ACG
LM240LAH-6.0		MC78L06ACG
LM240LAH-8.0		MC78L08ACG
LM240LAH-12		MC78L12ACG
LM240LAH-15		MC78L15ACG
LM240LAH-18		MC78L18ACG
LM240LAH-24		MC78L24ACG
LM240LAZ-5.0		MC78L05ACP
LM240LAZ-6.0		MC78L06ACP
LM240LAZ-8.0		MC78L08ACP
LM240LAZ-12		MC78L12ACP
LM240LAZ-15		MC78L15ACP
LM240LAZ-18		MC78L18ACP
LM240LAZ-24		MC78L24ACP
LM243H		MC1536G
LM245K		MC7905CK
LM248D	MC4741L	
LM248J	MC4741L	
LM249D		MC4741L
LM249J		MC4741L
LM258AH		MLM258G
LM258H	MLM258G	
LM271H		MC1590G
LM300F		MLM305G
LM300H		MLM305G
LM301AD		MLM301AU
LM301AF		MLM301AG
LM301AH	MLM301AG	
LM301AJ	MLM301AU	
LM301AJG	MLM301AU	
LM301AL	MLM301AG	
LM301AN	MLM301AP1	
LM301AP	MLM301AP1	
LM302H	MLM310G	
LM304F		MLM304G
LM304H	MLM304G	
LM304J		MLM304G
LM304L	MLM304G	
LM304N		MLM304G
LM305AH		MLM305G
LM305AJG		MLM305G
LM305AL		MLM305G
LM305AP		MLM305G
LM305F		MLM305G
LM305H	MLM305G	
LM305JG		MLM305G
LM305L	MLM305G	
LM305P		MLM305G
LM306H		MC1710CG
LM307D		MLM307U
LM307F		MLM307G
LM307H	MLM307G	
LM307J	MLM307U	
LM307JG	MLM307U	
LM307J-14		MLM307U

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
LM307L	MLM307G	
LM307N	MLM307P1	
LM307P	MLM307P1	
LM308AD	MLM308AL	
LM308AF		MLM308AL
LM308AH	MLM308AG	
LM308AH-1		MLM308AG
LM308AH-2		MLM308AG
LM308AJ	MLM308AU	
LM308D	MLM308L	
LM308H	MLM308G	
LM308N	MLM308P1	
LM309H	MLM309G	
LM309K	MLM309K	
LM309KC	MLM309K	
LM309LA	MLM309K	
LM310D		MLM310G
LM310F		MLM310G
LM310H	MLM310G	
LM310J-8		MLM310P1
LM310N	MLM310P1	
LM311D	MLM311L	
LM311F	MLM311F	
LM311H	MLM311G	
LM311N	MLM311P1	
LM311N-14	MLM311L	
LM312D		MC1456L
LM312F		MC1456L
LM312H		MC1456G
LM317H	LM317H	
LM317K	LM317K	
LM317P	LM317T	
LM317T	LM317T	
LM318D		MC1741SCL
LM318F		MC1741SCL
LM318H		MC1741SCG
LM318N		MC1741SCP1
LM320H-5.0		MC7905CK
LM320H-5.2		MC7905.2CK
LM320H-6.0		MC7906CK
LM320H-8.0		MC7908CK
LM320H-12		MC7912CK
LM320H-15		MC7915CK
LM320H-18		MC7918CK
LM320H-24		MC7924CK
LM320K-5.0		MC7905CK
LM320K-6.0		MC7906CK
LM320K-8.0		MC7908CK
LM320K-12		MC7912CK
LM320K-15		MC7915CK
LM320K-18		MC7918CK
LM320K-24		MC7924CK
LM320MP-5.0		MC7905CT
LM320MP-5.2		MC7905.2CT
LM320MP-6.0		MC7906CT
LM320MP-8.0		MC7908CT
LM320MP-12		MC7912CT
LM320MP-15		MC7915CT
LM320MP-18		MC7918CT
LM320MP-24		MC7924CT
LM320T-5.0		MC7905CT
LM320T-5.2		MC7905.2CT
LM320T-6.0		MC7906CT
LM320T-8.0		MC7908CT
LM320T-12		MC7912CT
LM320T-15		MC7915CT
LM320T-18		MC7918CT
LM320T-24		MC7924CT
LM322H		MC1455G
LM322N		MC1455P1
LM323K	LM323K	
LM324AJ		MLM324L
LM324AN		MLM324P
LM324J	MLM324L	MC3403L
LM324N	MLM324P	MC3403P
LM325AN		MC1468L
LM325H		MC1468G
LM325N		MC1468L
LM326H		MC1468G
LM326N		MC1468L
LM328AN		MC1468L
LM328H		MC1468G
LM328N		MC1468L
LM339AD	MLM339AL	
LM339AN	MLM339AP	
LM339N	MLM339P	
LM340K-5.0	MC7805CK	
LM340K-6.0	MC7806CK	
LM340K-8.0	MC7808CK	
LM340K-12	MC7812CK	
LM340K-15	MC7815CK	
LM340K-18	MC7818CK	
LM340K-24	MC7824CK	
LM340KC-5.0	MC7805CK	
LM340KC-6.0	MC7806CK	
LM340KC-8.0	MC7808CK	
LM340KC-12	MC7812CK	
LM340KC-15	MC7815CK	
LM340KC-18	MC7818CK	
LM340KC-24	MC7824CK	
LM340LAH-5.0		MC78L05ACG
LM340LAH-6.0		MC78L06ACG
LM340LAH-8.0		MC78L08ACG
LM340LAH-12		MC78L12ACG
LM340LAH-15		MC78L15ACG
LM340LAH-18		MC78L18ACG
LM340LAH-24		MC78L24ACG
LM340LAZ-5.0		MC78L05ACP
LM340LAZ-6.0		MC78L06ACP
LM340LAZ-8.0		MC78L08ACP
LM340LAZ-12		MC78L12ACP
LM340LAZ-15		MC78L15ACP
LM340LAZ-18		MC78L18ACP
LM340LAZ-24		MC78L24ACP
LM340T-5.0	MC7805CT	
LM340T-6.0	MC7806CT	
LM340T-8.0	MC7808CT	
LM340T-12	MC7812CT	
LM340T-15	MC7815CT	
LM340T-18	MC7818CT	
LM340T-24	MC7824CT	
LM341P-5.0	MC78M05CT	
LM341P-6.0	MC78M06CT	
LM341P-8.0	MC78M08CT	
LM341P-12	MC78M12CT	
LM341P-15	MC78M15CT	
LM341P-18	MC78M18CT	
LM341P-24	MC78M24CT	
LM342P-5.0	MC78M05CT	
LM342P-6.0	MC78M06CT	
LM342P-8.0	MC78M08CT	
LM342P-12	MC78M12CT	
LM342P-15	MC78M15CT	
LM342P-18	MC78M18CT	
LM342P-24	MC78M24CT	
LM343D		MC1436G
LM343H		MC1436G
LM345K		MC7905CK
LM348D	MC4741L	
LM348J	MC4741CL	
LM348N	MC4741CP	
LM349D		MC4741CL
LM349J		MC4741CL
LM349N		MC4741CL
LM358AH		MLM358G
LM358AN		MLM358P1
LM358H	MLM358G	
LM358JG	MLM358U	
LM358L	MLM358G	
LM358N	MLM358P1	
LM358P	MLM358P1	
LM363AJ		MC3450L
LM363AN		MC3450P
LM363J		MC3450L
LM363N		MC3450P
LM371H		MC1590G
LM376JG		MLM305G
LM376L	MLM305G	
LM376N		MLM305G
LM376P		MLM305G
LM380N		MC1384PQ
LM381N		MC1303P
LM382N		MC1303P
LM384N		MC1384PQ
LM386N		MC1306P
LM388N		MC1384PQ
LM390N		MC1384PQ
LM555CH	MC1455G	
LM555CN	MC1455P1	
LM555H	MC1555G	
LM556CD	MC3456L	
LM556CJ	MC3456L	
LM556CN	MC3456P	
LM556D	MC3556L	
LM556J	MC3556L	
LM565CH		MLM565CP
LM565CN	MLM565CP	
LM565H		MLM565CP
LM703LN		MC1350P
LM709AH	MC1709AG	
LM709AJ	MC1709AL	
LM709CH	MC1709CG	
LM709CJ	MC1709CL	
LM709CN	MC1709CP2	
LM709CN-8	MC1709CP1	
LM709H	MC1709G	
LM709J	MC1709L	
LM710CH	MC1710CG	
LM710CN	MC1710CP	
LM710H	MC1710G	
LM711CH	MC1711CG	
LM711CN	MC1711CP	
LM711H	MC1711G	
LM723CD	MC1723CL	
LM723CH	MC1723CG	
LM723CJ	MC1723CL	
LM723CN	MC1723CP	
LM723D	MC1723L	
LM723H	MC1723G	
LM723J	MC1723L	
LM733CD	MC1733CL	
LM733CH	MC1733CG	
LM733CJ	MC1733CL	
LM733CN	MC1733CP	
LM733D	MC1733L	
LM733H	MC1733G	
LM733J	MC1733L	
LM741AD		MC1741L
LM741AF		MC1741F
LM741AH		MC1741G
LM741AJ-14		MC1741L
LM741CD	MC1741CL	
LM741CF	MC1741CF	
LM741CH	MC1741CG	
LM741CJ	MC1741CU	
LM741CJ-14	MC1741CL	
LM741CN	MC1741CP1	
LM741CN-14	MC1741CP2	
LM741D	MC1741L	
LM741ED		MC1741CL
LM741EH		MC1741CG
LM741EJ		MC1741CU

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
LM741EJ-14		MC1741CL
LM741EN		MC1741CP1
LM741F	MC1741F	
LM741H	MC1741G	
LM741J-14	MC1741L	
LM746N		MC1323P
LM747CD	MC1747CL	
LM747CF	MC1747CF	
LM747CH	MC1747CG	
LM747CJ	MC1747CL	
LM747CN	MC1747CP2	
LM747D	MC1747L	
LM747F	MC1747F	
LM747H	MC1747G	
LM747J	MC1747L	
LM748CH	MC1748CG	
LM748CJ	MC1748CU	
LM748CN	MC1748CP1	
LM748H	MC1748G	
LM748J	MC1748U	
LM1303N	MC1303P	
LM1307N	MC1307P	
LM1310N	MC1310P	
LM1351N	MC1351P	
LM1391N	MC1391P	
LM1394N	MC1394P	
LM1414J	MC1414L	
LM1414N	MC1414P	
LM1458H	MC1458G	
LM1458J	MC1458U	
LM1458N	MC1458P1	
LM1458N-14	MC1458P2	
LM1488J	MC1488L	
LM1489AJ	MC1489AL	
LM1489J	MC1489L	
LM1496H	MC1496G	
LM1496J	MC1496L	
LM1496N	MC1496P	
LM1514J	MC1514L	
LM1558H	MC1558G	
LM1558J	MC1558U	
LM1596H	MC1596G	
LM1596J	MC1596L	
LM1800AN		MC1310P
LM1800N		MC1310P
LM1805		MC1385P
LM1808N		TDA1190Z
LM1828N		MC1323P
LM1841N	MC1356P	
LM1845N		MC1344P
LM1848N		MC1323P
LM1850N		MC3426L
LM1900D		MC3301L
LM2111N	MC1357P	
LM2113N		MC1357P
LM2900J		MC3301L
LM2900N		MC3301P
LM2901N	MLM2901P	
LM2902J	MLM2902L	
LM2902N	MLM2902P	
LM2904N		MLM358P1
LM2905N		MC1455P1
LM2907N		MC3315P
LM2917N		MC3315P
LM3011H		MC1550G
LM3026		CA3054
LM3045		MC3346P
LM3046N	MC3346P	
LM3054	CA3054	
LM3064N	MC1364P	
LM3065N	MC1358P	
LM3066N		MC1399P
LM3067N		MC1323P
LM3070N		MC1399P
LM3071N		MC1399P
LM3075N	MC1375P	
LM3086N	MC3386P	
LM3126		MC1399P
LM3146		MC3346P
LM3146A		MC3346P
LM3301N	MC3301P	
LM3302J	MC3302L	
LM3302N	MC3302P	
LM3401N	MC3401P	
LM3900N		MC3401P
LM3905N		MC1455P1
LM4250CH		MC1776CG
LM4250CN		MC1776CP1
LM4250H		MC1776G
LM5524J	MC5524L	
LM5525J	MC5525L	
LM5528J	MC5528L	
LM5529J	MC5529L	
LM5534J	MC5534L	
LM5535J	MC5535L	
LM5538J	MC5538L	
LM5539J	MC5539L	
LM7524J	MC7524L	
LM7524N	MC7524P	
LM7525J	MC7525L	
LM7525N	MC7525P	
LM7528J	MC7528L	
LM7528N	MC7528P	
LM7529J	MC7529L	
LM7529N	MC7529P	
LM7534J	MC7534L	
LM7534N	MC7534P	
LM7535J	MC7535L	
LM7535N	MC7535P	
LM7538J	MC7538L	
LM7538N	MC7538P	
LM7539J	MC7539L	
LM7539N	MC7539P	
LM7805KC	MC7805CK	
LM7806KC	MC7806CK	
LM7808KC	MC7808CK	
LM7812KC	MC7812CK	
LM7815KC	MC7815CK	
LM7818KC	MC7818CK	
LM7824KC	MC7824CK	
LM55107AJ	MC55107L	
LM55108AJ	MC55108L	
LM55109J		MC75110L
LM55110J		MC75110L
LM55121J		MC8T13L
LM55122J		MC8T14L
LM55123J		MC8T23L
LM55124J		MC8T24L
LM55325N	MC55325L	
LM75107AJ	MC75107L	
LM75107AN	MC75107P	
LM75108AJ	MC75108L	
LM75108AN	MC75108P	
LM75110J	MC75110L	
LM75110N	MC75110P	
LM75121J	MC8T13L	
LM75121N	MC8T13P	
LM75122J	MC8T14L	
LM75122N	MC8T14P	
LM75123J	MC8T23L	
LM75123N	MC8T23P	
LM75124J	MC8T24L	
LM75124N	MC8T24P	
LM75207L		MC75107L
LM75207N		MC75107P
LM75208J		MC75108L
LM75208N		MC75108P
LM75324J		MC75325L
LM75324N		MC75325P
LM75325J	MC75325P	
LM75325N	MC75325L	
LM75450N	MC75450P	
LM75451N	MC75451P	
LM75452N	MC75452P	
LM75453N	MC75453P	
LM75454N	MC75454P	
LM78L05ACH	MC78L05ACG	
LM78L05ACZ	MC78L05ACP	
LM78L05CH	MC78L05CG	
LM78L05CZ	MC78L05CP	
LM78L08ACH	MC78L08ACG	
LM78L08ACZ	MC78L08ACP	
LM78L08CH	MC78L08CG	
LM78L08CZ	MC78L08CP	
LM78L12ACH	MC78L12ACG	
LM78L12ACZ	MC78L12ACP	
LM78L12CH	MC78L12CG	
LM78L12CZ	MC78L12CP	
LM78L15ACH	MC78L15ACG	
LM78L15ACZ	MC78L15ACP	
LM78L15CH	MC78L15CG	
LM78L15CZ	MC78L15CP	
LM78L18ACH	MC78L18ACG	
LM78L18ACZ	MC78L18ACP	
LM78L18CH	MC78L18CG	
LM78L18CZ	MC78L18CP	
LM78L24ACH	MC78L24ACG	
LM78L24ACZ	MC78L24ACP	
LM78L24CH	MC78L24CG	
LM78L24CZ	MC78L24CP	
MC1310A	MC1310P	
MC1408B	MC1408P8	
MC1408F	MC1408L8	
MC1458JG	MC1458U	
MC1458L	MC1458G	
MC1458P	MC1458P1	
MC1558JG	MC1558U	
MC1558L	MC1558G	
MH0026H		MMH0026CG
MH0026CH	MMH0026CG	
MH0026CN	MMH0026CP1	
MH0026G		MMH0026CG
MH0026CG		MMH0026CG
MH0026F		MMH0026CL
MH0026CF		MMH0026C1
MIC709-1	MC1709G	
MIC709-5	MC1709CG	
MIC710-1B	MC1710F	
MIC710-1C	MC1710G	
MIC710-5B	MC1710CF	
MIC710-5C	MC1710CG	
MIC711-1B	MC1711F	
MIC711-1C	MC1711G	
MIC711-5B	MC1711CF	
MIC711-5C	MC1711CG	
MIC712-1B	MC1712F	
MIC712-1C	MC1712G	
MIC712-1D	MC1712L	
MIC712-5B	MC1712CF	
MIC712-5C	MC1712CG	
MIC712-5D	MC1712CL	
MIC723-1	MC1723G	
MIC723-5	MC1723CG	
MIC741-1C	MC1741G	
MIC741-1D	MC1741L	
MIC741-5C	MC1741CG	
MIC741-5D	MC1741CL	
ML101AF		MLM101AG
ML101AM		MLM101AG
ML101AT	MLM101AG	
ML101F		MLM101AG
ML101M		MLM101AG

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
ML101T	MLM101AG	
ML107F		MLM107G
ML107M		MLM107G
ML107T	MLM107G	
ML108AF		MC1556G
ML108AM	MLM108AL	
ML108AT	MLM108AG	
ML108M	MLM108L	
ML108T	MLM108G	
ML111F	MLM111F	
ML111M	MLM111L	
ML111S		MLM111L
ML111T	MLM111G	
ML118F		MC1741SG
ML118M		MC1741SG
ML118T		MC1741SG
ML201AF		MLM201AG
ML201AM		MLM201AG
ML201AT	MLM201AG	
ML201F		MLM201AG
ML201M		MLM201AG
ML201T	MLM201AG	
ML207F		MLM207G
ML207M		MLM207G
ML207T	MLM207G	
ML208AF		MC1556G
ML208AM	MLM208AL	
ML208AT	MLM208AG	
ML208M	MLM208L	
ML208T	MLM208G	
ML211F	MLM211F	
ML211M	MLM211L	
ML211S	MLM211P1	
ML211T	MLM211G	
ML218F		MC1741SG
ML218M		MC1741SG
ML218T		MC1741SG
ML301AP		MLM301AP1
ML301AS	MLM301AP1	
ML301AT	MLM301AG	
ML301P		MLM301AP1
ML301S	MLM301AP1	
ML301T	MLM301AG	
ML307P		MLM307G
ML307S	MLM307P1	
ML307T	MLM307G	
ML308AM	MLM308AL	
ML308AT	MLM308AG	
ML308M	MLM308L	
ML308T	MLM308G	
ML311M	MLM311L	
ML311P	MLM311L	
ML311S	MLM311P1	
ML311T	MLM311G	
ML318M		MC1741SCP1
ML318T		MC1741SCG
ML709AF	MC1709AF	
ML709AM	MC1709AL	
ML709AT	MC1709AG	
ML709CP	MC1709CP2	
ML709CT	MC1709CG	
ML709F	MC1709F	
ML709M	MC1709L	
ML709T	MC1709G	
ML723CF		MC1723CL
ML723CM	MC1723CL	
ML723CP	MC1723CL	
ML723CT	MC1723CG	
ML723F		MC1723L
ML723M	MC1723L	
ML723T	MC1723G	
ML741AF		MC1556G
ML741AM		MC1556G
ML741AT		MC1556G
ML741CP	MC1741CP2	
ML741CS	MC1741CP1	
ML741CT	MC1741CG	
ML741F	MC1741F	
ML741M	MC1741L	
ML741T	MC1741G	
ML747CP	MC1747CL	
ML747CT	MC1747CG	
ML747F	MC1747F	
ML747M	MC1747L	
ML747T	MC1747G	
ML748CP		MLM301AP1
ML748CS	MLM301AP1	
ML748CT	MC1748CG	
ML748F		MC1748G
ML748M		MC1748G
ML748T	MC1748G	
ML1436T	MC1436G	
ML1437P	MC1437P	
ML1458P	MC1458P2	
ML1458S	MC1458P1	
ML1458T	MC1458G	
ML1488M	MC1488L	
ML1489AM	MC1489AL	
ML1489M	MC1489L	
ML1536T	MC1536G	
ML1537M	MC1537L	
ML1558M	MC1558L	
ML1558T	MC1558G	
ML3046P	MC3346P	
ML4250T		MC1776G
ML4250CS		MC1776CG
ML4250CT		MC1776CG
ML4251T		MC1776G
ML4251CS		MC1776CG
ML4251CT		MC1776CG
ML6503M		MC1537L
ML7503M		MC1437L
N5065A	MC1358P	
N5070B		MC1399P
N5071A		MC1399P
N5072A		MC1323P
N5556T	MC1456G	
N5556V	MC1456P1	
N5558F	MC1458L	
N5558T	MC1458G	
N5558V	MC1458P1	
N5595A	MC1495L	
N5595F	MC1495L	
N5596A	MC1496L	
N5596K	MC1496G	
N5709A	MC1709CP2	
N5709G	MC1709CF	
N5709T	MC1709CG	
N5709V	MC1709CP1	
N5710A	MC1710CP	
N5710T	MC1710CG	
N5711A	MC1711CP	
N5711K	MC1711CG	
N5723A		MC1723CP
N5723T	MC1723CG	
N5733K	MC1733CG	
N5741A	MC1741CP2	
N5741T	MC1741CG	
N5741V	MC1741CP1	
N5747A	MC1747CL	
N5747F	MC1747CL	
N5748A		MC1747CG
N5748T	MC1748CG	
N7520B	MC7520P	
N7521B	MC7521P	
N7522B	MC7522P	
N7523B	MC7523P	
N7524B	MC7524P	
N7525B	MC7525P	
N8T13B	MC8T13P	
N8T13P	MC8T13L	
N8T14B	MC8T14P	
N8T14E	MC8T14L	
N8T15A		MC1488L
N8T15F		MC1488L
N8T16A		MC1489L
N8T23B	MC8T23P	
N8T23E	MC8T23L	
N8T24B	MC8T24P	
N8T24E	MC8T24L	
N8T26AB	MC8T26AP	
N8T26AE	MC8T26AL	
N8T26B	MC8T26P	
N8T28B	MC8T28P	
N8T37A	MC3437P	
N8T38A	MC3438P	
N8T95B	MC8T95P	
N8T95F	MC8T95L	
N8T96B	MC8T96P	
N8T96F	MC8T96L	
N8T97B	MC8T97P	
N8T97F	MC8T97L	
N8T98B	MC8T98P	
N8T98F	MC8T98L	
NE501A		MC1733CL
NE501K		MC1733CG
NE515A		MC1420G
NE515G		MC1520F
NE515K		MC1420G
NE516A		MC1420G
NE516G		MC1520F
NE516K		MC1420G
NE528B		MC1444L
NE528E		MC1444L
NE531G		MC1439G
NE531T		MC1439G
NE531V		MC1439P
NE533G		MC1776CG
NE533T		MC1776CG
NE533V		MC1776CG
NE537G		MC1456G
NE537T		MC1456G
NE540L		MC1554G
NE550A		MC1723CP
NE550L		MC1723CG
NE555JG	MC1455U	
NE555L	MC1455G	
NE555P	MC1455P1	
NE555T	MC1455G	
NE555V	MC1455P1	
NE556A	MC3456P	
NE556I	MC3456L	
NE565A	MLM565CP	
NE565K		MLM565CP
NE592A	NE592L	
NE592K	NE592G	
OP-01C		MC1536
OP-01G		MC1536
OP-01H		MC1536
OP-01J		MC1536G
OP-01L		MC1536G
OP-01P		MC1536P
OP-08		MC1776
OP-08A		MC1776
OP-08B		MC1776
OP-08C		MC1776
OP-08E		MC1776
PA239A		MC1303P
RC702T	MC1712CG	
RC709D	MC1709CL	
RC709DN	MC1709CP1	
RC709DP	MC1709CP2	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
RC709Q	MC1709CF	
RC709T	MC1709CG	
RC710DC	MC1710CL	
RC710DP	MC1710CP	
RC710Q	MC1710CF	
RC710T	MC1710CG	
RC711DC	MC1711CL	
RC711DP	MC1711CP	
RC711Q	MC1711CF	
RC711T	MC1711CG	
RC723D	MC1723CL	
RC723T	MC1723CG	
RC733D	MC1733CL	
RC733T	MC1733CG	
RC741D	MC1741CL	
RC741DN	MC1741CP1	
RC741DP	MC1741CP2	
RC741Q	MC1741CF	
RC741T	MC1741CG	
RC747D	MC1747CL	
RC747T	MC1747CG	
RC748T	MC1748CG	
RC1414DC	MC1414L	
RC1414DP	MC1414P	
RC1437D	MC1437L	
RC1437DP	MC1437P	
RC1458DN	MC1458P1	
RC1458T	MC1458G	
RC1488DC	MC1488L	
RC1489ADC	MC1489AL	
RC1489DC	MC1489L	
RC1556T	MC1456CG	
RC1558T	MC1558G	
RC3302DB	MC3302P	
RC4131DP		MC1471SCP1
RC4131T		MC1741SG
RC4136D		MC3403L
RC4136DP		MC3403P
RC4136J		MC3403L
RC4136N		MC3403P
RC4195T		MC1468G
RC4195TK		MC1468R
RC4444R	MC3416L	
RC4558DN	MC4558CP1	
RC4558JG	MC4558CU	
RC4558L	MC4558CG	
RC4558P	MC4558CP1	
RC4558T	MC4558CG	
RC4739D		MC1303P
RC4739DB		MC1303P
RC4739DP	MC1303P	
RC7522M	MC7522L	
RC7523M	MC7523L	
RC7524M	MC7524L	
RC7525M	MC7525L	
RC8T13DD	MC8T13L	
RC8T13MP	MC8T13P	
RC8T14DD	MC8T14L	
RC8T14MP	MC8T14P	
RC8T23DD	MC8T23L	
RC8T23MP	MC8T23P	
RC8T24DD	MC8T24L	
RC8T24MP	MC8T24P	
RC75107AD	MC75107L	
RC75107ADP	MC75107P	
RC75108AD	MC75108L	
RC75108ADP	MC75108P	
RC75109D		MC75110L
RC75109DP		MC75110P
RC75110D	MC75110L	
RC75110DP	MC75110P	
RC75325DD	MC75325L	
RM702Q	MC1712F	
RM702T	MC1721G	
RM709D	MC1709L	
RM709Q	MC1709F	
RM709T	MC1709G	
RM710D	MC1710L	
RM710Q	MC1710F	
RM710T	MC1710G	
RM711DC	MC1711L	
RM711Q	MC1711F	
RM711T	MC1711G	
RM723D	MC1723L	
RM723T	MC1723G	
RM733D	MC1733L	
RM733T	MC1733G	
RM741D	MC1741L	
RM741DP	MC1741P	
RM741Q	MC1741F	
RM741T	MC1741G	
RM747D	MC1747L	
RM747T	MC1747G	
RM748T	MC1748G	
RM1514DC	MC1514L	
RM1537D	MC1537L	
RM4136D		MC3503L
RM4136J		MC3503L
RM4195T		MC1568G
RM4195TK		MC1568R
RM4558D	MC4558U	
RM4558JG	MC4558U	
RM4558L	MC4558G	
RM4558T	MC4558G	
RM55107AD	MC55107L	
RM55325DD	MC55325L	
RV3301DB	MC3301P	
S5556T	MC1556G	
S5558E	MC1558L	
S5558T	MC1558G	
S5596F	MC1596L	
S5596K	MC1596G	
S5709G	MC1709F	
S5709T	MC1709G	
S5710T	MC1710G	
S5711K	MC1711G	
S5723T	MC1723G	
S5733K	MC1733G	
S5741T	MC1741G	
S8T13E		MC8T13L
S8T14E		MC8T14L
SE501K		MC1733G
SE515G		MC1520F
SE515K		MC1520G
SE516A		MC1520G
SE516G		MC1520F
SE516K		MC1520G
SE528E		MC1544L
SE528R		MC1544L
SE531G		MC1539G
SE531T		MC1539G
SE533G		MC1776G
SE533T		MC1776G
SE537G		MC1556G
SE537T		MC1556G
SE550L		MC1723G
SE555JG	MC1555U	
SE555L	MC1555G	
SE555T	MC1555G	
SE556A	MC3556L	
SE565A		MLM565CP
SE565K		MLM565CP
SE592A	SE592L	
SE592K	SE592G	
SG100T		MC1723G
SG101AD		MLM101AG
SG101AT	MLM101AG	
SG101J		MLM101AG
SG101T	MLM101AG	
SG102J		MLM110G
SG102T	MLM110G	
SG104T	MLM104G	
SG105N		MLM105G
SG105T	MLM105G	
SG107J		MLM107G
SG107T	MLM107G	
SG108AJ	MLM108AL	
SG108AT	MLM108AG	
SG108J	MLM108L	
SG108T	MLM108G	
SG109K	MLM109K	
SG109T	MLM109G	
SG110D		MLM110G
SG110T	MLM110G	
SG111D	MLM111L	
SG111M	MLM111P1	
SG111T	MLM111G	
SG118J		MC1741SL
SG118T		MC1741SG
SG120K-05		MC7905CK
SG120K-5.2		MC7905.2CK
SG120K-12		MC7912CK
SG120K-15		MC7915CG
SG120T-05		MC7905CT
SG120T-5.2		MC7905.2CK
SG120T-12		MC7912CT
SG120T-15		MC7915CT
SG124J	MLM124L	
SG140K-05		MC7805CK
SG140K-06		MC7806CK
SG140K-08		MC7808CK
SG140K-12		MC7812CK
SG140K-15		MC7815CK
SG140K-18		MC7818CK
SG140K-24		MC7824CK
SG200T		MC1723G
SG201AD		MLM201AG
SG201AM	MLM201AP1	
SG201AN		MLM201AP1
SG201AT	MLM201AG	
SG201J		MLM201AG
SG201M	MLM201AP1	
SG201N		MLM201AP1
SG201T	MLM201AG	
SG202J		MLM210G
SG202M		MLM210G
SG202N		MLM210G
SG202T	MLM210G	
SG204T	MLM204G	
SG205N		MLM205G
SG205T	MLM205G	
SG207J		MLM207G
SG207M		MLM207G
SG207N		MLM207G
SG207T	MLM207G	
SG208AJ	MLM208AL	
SG208AM	MLM208AU	
SG208AT	MLM208AG	
SG208J	MLM208L	
SG208M	MLM208U	
SG208T	MLM208G	
SG209K	MLM209K	
SG209T	MLM209G	
SG210D		MLM210G
SG210M		MLM210G
SG210N		MLM210G
SG210T	MLM210G	
SG211D	MLM211L	
SG211M	MLM211P1	
SG211T	MLM211G	
SG218J		MC1741SL
SG218M		MC1741SL

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
SG218T		MC1741SG
SG224J	MLM224L	
SG224N	MLM224P	
SG300N		MC1723CP
SG300T		MC1723CG
SG301AD		MLM301AG
SG301AM	MLM301AP1	
SG301AN		MLM301AP1
SG301AT	MLM301AG	
SG302J		MLM310P1
SG302M	MLM310P1	
SG302N		MLM310P1
SG302T	MLM310G	
SG304T	MLM304G	
SG305AT		MLM305G
SG305N		MLM305G
SG305T	MLM305G	
SG307J		MLM307P1
SG307M	MLM307P1	
SG307N		MLM307P1
SG307T	MLM307G	
SG308AJ	MLM308AL	
SG308AM	MLM308AP1	
SG308AT	MLM308AG	
SG308J	MLM308L	
SG308M	MLM308P1	
SG308T	MLM308G	
SG309K	MLM309K	
SG309T	MLM309G	
SG310D		MLM310P1
SG310M	MLM310P1	
SG310N		MLM310P1
SG310T	MLM310G	
SG311D	MLM311L	
SG311M	MLM311P1	
SG311T	MLM311G	
SG318J		MC1741SCL
SG318M		MC1741CP1
SG318T		MC1741CG
SG320K-05		MC7905CK
SG320K-5.2		MC7905.2CK
SG320K-12		MC7912CK
SG320K-15		MC7915CK
SG320T-05		MC7905CT
SG320T-5.2		MC7905.2CT
SG320T-12		MC7912CT
SG320T-15		MC7915CT
SG324J	MLM324L	
SG324N	MLM324P	
SG340K-05	MC7805CK	
SG340K-06	MC7806CK	
SG340K-08	MC7808CK	
SG340K-12	MC7812CK	
SG340K-15	MC7815CK	
SG340K-18	MC7818CK	
SG340K-24	MC7824CK	
SG555CM	MC1455P1	
SG555CT	MC1455G	
SG555T	MC1555G	
SG556CJ	MC3456L	
SG556CN	MC3456P	
SG556J	MC3556L	
SG556N	MC3556L	
SG710CD	MC1710CL	
SG710CF	MC1710CF	
SG710CN	MC1710CP	
SG710CT	MC1710CG	
SG710D	MC1710L	
SG710F	MC1710F	
SG710N	MC1710P	
SG710T	MC1710G	
SG711CD	MC1711CL	
SG711CF	MC1711CF	
SG711CN	MC1711CP	
SG711CT	MC1711CG	
SG711D	MC1711L	
SG711F	MC1711F	
SG711N	MC1711P	
SG711T	MC1711G	
SG723CD	MC1723CL	
SG723CN	MC1723CP	
SG723CT	MC1723CG	
SG723D	MC1723L	
SG723T	MC1723G	
SG733CD	MC1733CL	
SG733CN		MC1733CP
SG733CT	MC1733CG	
SG733D	MC1733L	
SG733N		MC1733L
SG733T	MC1733G	
SG741CD	MC1741CL	
SG741CF	MC1741CF	
SG741CM	MC1741CP1	
SG741CN	MC1741CP2	
SG741CT	MC1741CG	
SG741D	MC1741L	
SG741F	MC1741F	
SG741T	MC1741G	
SG741SCM	MC1741SCP1	
SG741SCT	MC1741SCG	
SG741ST	MC1741SG	
SG747CJ	MC1747CL	
SG747CN	MC1747CP2	
SG747CT	MC1747CG	
SG747J	MC1747L	
SG747T	MC1747G	
SG748CD		MC1748CP1
SG748CM		MC1748CP1
SG748CN		MC1748CP1
SG748CT	MC1748CG	
SG748D		MC1748G
SG748T	MC1748G	
SG777CJ		MLM308AL
SG777CM		MLM308AP1
SG777CN		MLM308AP1
SG777CT		MLM308AG
SG777J		MLM108AL
SG777T		MLM108AG
SG1118AJ		MLM108AL
SG1118AT		MLM108AG
SG1118J		MLM108L
SG1118T		MLM108G
SG1217		MC1741G
SG1217J		MC1741SL
SG1217T		MC1741SG
SG1250T		MC1776G
SG1401N		MC1533G
SG1401T		MC1533G
SG1402N		MC1594L
SG1402T		MC1594L
SG1436CT	MC1436CG	
SG1436M	MC1436U	
SG1436T	MC1436G	
SG1456CT	MC1456CG	
SG1456T	MC1456G	
SG1458M	MC1458P1	
SG1458T	MC1458G	
SG1468J	MC1468L	
SG1468N	MC1468L	
SG1468T	MC1468G	
SG1495D	MC1495L	
SG1495N	MC1495L	
SG1496D	MC1496L	
SG1496N		MC1496L
SG1496T	MC1496G	
SG1501AD		MC1568L
SG1501AT		MC1568G
SG1501D	MC1568L	
SG1501T	MC1568G	
SG1502D		MC1568L
SG1502N		MC1568L
SG1524J		MC3520L
SG1536T	MC1536G	
SG1556T	MC1556G	
SG1558T	MC1558G	
SG1595D	MC1595L	
SG1596D	MC1596L	
SG1596T	MC1596G	
SG1660D		MLM301AG
SG1660J		MLM308L
SG1660M		MLM308P1
SG1660T		MLM308G
SG1760D		MLM307G
SG1760F		MLM307G
SG1760J		MLM308L
SG1760M		MLM308P1
SG1760T		MLM308G
SG2118AJ		MLM208AL
SG2118AM		MLM208AU
SG2118AT		MLM208AG
SG2118J		MLM208L
SG2118M		MLM208U
SG2118T		MLM208G
SG2250T		MC1776G
SG2401N		MC1433G
SG2402N		MC1494L
SG2402T		MC1494L
SG2501AD		MC1468L
SG2501AT		MC1468G
SG2501D	MC1468L	
SG2501N	MC1468L	
SG2501T	MC1468G	
SG2502D		MC1468L
SG2502N		MC1468L
SG2502T		MC1468G
SG2524J		MC3520L
SG3118AJ		MLM308AL
SG3118AM		MLM308AP1
SG3118AT		MLM308AG
SG3118J		MLM308L
SG3118M		MLM308P1
SG3118T		MLM308G
SG3250T		MC1776G
SG3401N		MC1433G
SG3401T		MC1433G
SG3402N		MC1494L
SG3402T		MC1494L
SG3501AD	MC1468L	
SG3501AT	MC1468G	
SG3501D	MC1468L	
SG3501N	MC1468L	
SG3501T	MC1468G	
SG3502D		MC1468L
SG3502G		MC1468G
SG3502N		MC1468L
SG3524J		MC3420L
SG4250CM		MC1776CP1
SG4250CT		MC1776CG
SG4250T		MC1776G
SG4501D	MC1468L	
SG4501N	MC1468L	
SG4501T	MC1468G	
SG7524J	MC7524L	
SG7524N	MC7524P	
SG7525J	MC7525L	
SG7525N	MC7525P	
SG7528J	MC7528L	
SG7528N	MC7528P	
SG7529J	MC7529L	
SG7529N	MC7529P	
SG7805CK	MC7805CK	
SG7805K		MC7805CK

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
SG7806CK	MC7806CK	
SG7806K		MC7806CK
SG7808CK	MC7808CK	
SG7808K		MC7808CK
SG7812CK	MC7812CK	
SG7812K		MC7812CK
SG7815CK	MC7815CK	
SG7815K		MC7815CK
SG7818CK	MC7818CK	
SG7818K		MC7818CK
SG7824CK	MC7824CK	
SG7824K		MC7824CK
SH0013HC		MMH0026CG
SH0013HM		MMH0026G
SH2001FC		MC75462P
SH2001FM		MC75462P
SH2001HC		MC75462P
SH2001HM		MC75462P
SH2002FC		MC75462P
SH2002FM		MC75462P
SH2002HC		MC75462P
SH2002HM		MC75462P
SH2002HC		MC75462P
SH2200FC		MC75462P
SH2200FM		MC75462P
SH2200HC		MC75462P
SH2200HM		MC75462P
SH2200PC		MC75462P
SH8090FM		MC1508L8
SN5510FA	MC1510F	
SN5510L	MC1510G	
SN5522J	MC5522L	
SN5523J	MC5523L	
SN5524J	MC5524L	
SN5525J	MC5525L	
SN5528J	MC5528L	
SN5529J	MC5529L	
SN7510FA	MC1410F	
SN7524J	MC7524L	
SN7524N	MC7524P	
SN7525J	MC7525L	
SN7525N	MC7525P	
SN7528J	MC7528L	
SN7528N	MC7528P	
SN7529J	MC7529L	
SN7529N	MC7529P	
SN52101AL	MLM101AG	
SN52104L	MLM104G	
SN52105L	MLM105G	
SN52106FA		MC1710F
SN52106J		MC1710L
SN52106L		MC1710G
SN52107L	MLM107G	
SN52108AL	MLM108AG	
SN52108L	MLM108G	
SN52109L	MLM109G	
SN52110L	MLM110G	
SN52510FA		MC1710F
SN52510J		MC1710L
SN52510L		MC1710G
SN52514J	MC1514L	
SN52555L	MC1555G	
SN52558L	MC1558G	
SN52702AFA		MC1712F
SN52702AJ		MC1712L
SN52702AL		MC1712G
SN52702FA	MC1712F	
SN52702J	MC1712L	
SN52702L	MC1712G	
SN52709AFA	MC1709AF	
SN52709AJ	MC1709AL	
SN52709AL	MC1709AG	
SN52709FA	MC1709F	
SN52709J	MC1709L	
SN52709L	MC1709G	
SN52710FA	MC1710F	
SN52710J	MC1710L	
SN52710L	MC1710G	
SN52711FA	MC1711F	
SN52711J	MC1711L	
SN52711L	MC1711G	
SN52723FA	MC1723F	
SN52723J	MC1723L	
SN52723L	MC1723G	
SN52733J	MC1733L	
SN52733L	MC1733G	
SN52741FA	MC1741F	
SN52741J	MC1741L	
SN52741L	MC1741G	
SN52747FA	MC1747F	
SN52747J	MC1747L	
SN52747L	MC1747G	
SN52748L	MC1748G	
SN52770L		MC1556G
SN52771L		MC1556G
SN52810FA		MC1710F
SN52810J		MC1710L
SN52810L		MC1710G
SN52811FA		MC1711F
SN52811J		MC1711L
SN52811L		MC1711G
SN55107AJ	MC55107L	
SN55107BJ		MC55107L
SN55108AJ	MC55108L	
SN55108BJ		MC55108L
SN55109J		MC75110L
SN55110J		MC75110L
SN55232J		MC5534L
SN55233J		MC5535L
SN55234J		MC5524L
SN55235J		MC5525L
SN55238J		MC5538L
SN55239J		MC5539L
SN55244J	MC1544L	
SN55325J	MC55325L	
SN72301AL	MLM301AG	
SN72301AP	MLM301AP1	
SN72304L	MLM304G	
SN72305AL		MLM305G
SN72305L	MLM305G	
SN72306J		MC1710CL
SN72306L		MC1710CG
SN72306N		MC1710CP
SN72307L	MLM307G	
SN72308AL	MLM308AG	
SN72308L	MLM308G	
SN72309L	MLM309G	
SN72310L	MLM310G	
SN72311L	MLM311G	
SN72311P	MLM311P	
SN72376L		MLM305G
SN72440J		MC3370P
SN72440N		MC3370P
SN72510J		MC1710CL
SN72510L		MC1710CG
SN72510N		MC1710CP
SN72514J		MC1414L
SN72514N		MC1414P
SN72555L	MC1455G	
SN72555P	MC1455P1	
SN72558L	MC1458G	
SN72558P	MC1458P1	
SN72702J	MC1712CL	
SN72702L	MC1712CG	
SN72709J	MC1709CL	
SN72709L	MC1709CG	
SN72709N	MC1709CP2	
SN72709P	MC1709CP1	
SN72710J	MC1710CL	
SN72710L	MC1710CG	
SN72710N	MC1710CP	
SN72711J	MC1711CL	
SN72711L	MC1711CG	
SN72711N	MC1711CP	
SN72720J		MC1710CL
SN72720L		MC1710CG
SN72720N		MC1710CP
SN72723J	MC1723CL	
SN72723L	MC1723CG	
SN72733J	MC1733CL	
SN72733L	MC1733CG	
SN72741FA	MC1741CF	
SN72741J	MC1741CL	
SN72741L	MC1741CG	
SN72741N	MC1741CP2	
SN72741P	MC1741CP1	
SN72747FA	MC1747CF	
SN72747J	MC1747CL	
SN72747L	MC1747CG	
SN72747N	MC1747CP2	
SN72748L	MC1748CG	
SN72748P	MC1748CP1	
SN72770L		MC1456G
SN72771L		MC1456G
SN72810FA		MC1710CF
SN72810J		MC1710CL
SN72810L		MC1710CG
SN72810N		MC1710CP
SN72811FA		MC1711CF
SN72811J		MC1711CL
SN72811L		MC1711CG
SN72811N		MC1711CP
SN72905	MC7905CP	
SN72906	MC7906CP	
SN72908	MC7908CP	
SN72912	MC7912CP	
SN72915	MC7915CP	
SN72L022P		MLM358P1
SN72L044JA		MLM324P
SN72L044N		MLM324P
SN75107AJ	MC75107L	
SN75107AN	MC75107P	
SN75107BJ		MC75107L
SN75107BN		MC75107P
SN75108AJ	MC75108L	
SN75108AN	MC75108P	
SN75108BJ		MC75108L
SN75108BN		MC75108P
SN75110J	MC75110L	
SN75110N	MC75110P	
SN75121J	MC8T13L	
SN75121N	MC8T13P	
SN75122J	MC8T14L	
SN75122N	MC8T14P	
SN75123J	MC8T23L	
SN75123N	MC8T23P	
SN75124J	MC8T24L	
SN75124N	MC8T24P	
SN75138N		MC3443P
SN75138J		MC3443P
SN75140P	MC75140P1	
SN75150J		MC1488L
SN75150N		MC1488L
SN75154J		MC1489L
SN75154N		MC1489L
SN75188J	MC1488L	
SN75188N	MC1488L	
SN75189AJ	MC1489AL	
SN75189J	MC1489L	
SN75189AN	MC1489AL	
SN75189N	MC1489L	
SN75207J		MC75107L

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
SN75207N		MC75107P
SN75208J		MC75108L
SN75208N		MC75108P
SN75232J		MC7534L
SN75232N		MC7534P
SN75233J		MC7535L
SN75233N		MC7535P
SN75234J		MC7534L
SN75234N		MC7534P
SN75235J		MC7535L
SN75235N		MC7535P
SN75238J		MC7538L
SN75238N		MC7538P
SN75239J		MC7539L
SN75239N		MC7539P
SN75261N		MC3461L
SN75322N		MC3460P
SN75362P		MMH0026CP
SN75365J	MC75365L	
SN75365N	MC75365P	
SN75368J	MC75368L	
SN75368N	MC75368P	
SN75369P	MMH0026CP	
SN75450AJ	MC75450L	
SN75450AN	MC75450P	
SN75450BN		MC75450P2
SN75450N	MC75450P2	
SN75451AP	MC75451P	
SN75451P	MC75451P	
SN75452P	MC75452P	
SN75453P	MC75453P	
SN75454P	MC75454P	
SN75460AJ	MC75460L	
SN75460AN	MC75460P	
SN75461	MC75461	
SN75461AP	MC75461P	
SN75462	MC75462	
SN75462AP	MC75462P	
SN75463	MC75463	
SN75463AP	MC75463P	
SN75464	MC75464	
SN75464AP	MC75464P	
SN75461N	MC75491P	
SN75466J	MC1411L	
SN75466N	MC1411P	
SN75467J	MC1412L	
SN75467N	MC1412P	
SN75468J	MC1413L	
SN75468N	MC1413P	
SN75475P	MC1472P1	
SN75475JG	MC1472U	
SN75491N	MC75491P	
SN75492N	MC75492P	
SN76000P		MC1306P
SN76005ND		MC1384PQ
SN76011ND		MC1384PQ
SN76021ND		MC1384PQ
SN76024ND		MC1384PQ
SN76104N		MC1310P
SN76105N		MC1310P
SN76111N		MC1310P
SN76113N		MC1310P
SN76115N	MC1310P	
SN76116N		MC1310P
SN76117N		MC1310P
SN76130N		MC1303P
SN76131N		MC1303P
SN76149N		MC1303P
SN76242N		MC1399P
SN76243N		MC1399P
SN76246N		MC1323P
SN76298N	MC1398P	
SN76514L		MC1496G
SN76514N	MC1496P	
SN76530P	MC1330P	
SN76564N	MC1364P	
SN76565N	MC1364P	
SN76591P	MC1391P	
SN76594P	MC1394P	
SN76600P	MC1350P	
SN76642N	MC1357P	
SN76644N		MC1352P
SN76650N	MC1352P	
SN76651N	MC1351P	
SN76653N		MC1352P
SN76660N		MC1357P
SN76665N	MC1364P	
SN76666N	MC1358P	
SN76669N	MC1356P	
SN76675N	MC1375P	
SN76678P		MC1355P
SSS101AL		MLM101AG
SSS101AJ	MLM101AG	
SSS101AP		MLM101AP1
SSS107J	MLM107G	
SSS107P		MLM107G
SSS201AJ	MLM201AG	
SSS201AL		MLM201AG
SSS201AP		MLM201AP1
SSS207J	MLM207G	
SSS207P		MLM207G
SSS301AJ	MLM301AG	
SSS301AL		MLM301AG
SSS301AP	MLM301AP1	
SSS741BJ		MC1741G
SSS741BL		MC1741F
SSS741BP	MC1741P2	
SSS741CJ		MC1741CG
SSS741CL		MC1741CF
SSS741CP	MC1741CP2	
SSS741GJ	MC1741SG	
SSS741GP		MC1741SG
SSS741J		MC1741G
SSS741L		MC1741F
SSS741P		MC1741P2
SSS747B2	MC1747F	
SSS747BP		MC1747L
SSS747CK		MC1747CG
SSS747CM		MC1747CF
SSS747CP		MC1747CL
SSS747GK		MC1747G
SSS747GM	MC1747F	
SSS747GP		MC1747L
SSS747L		MC1747F
SSS747P		MC1747L
SSS1408A-6Z	MC1408L6	
SSS1408A-7Z	MC1408L7	
SSS1408A-8Z	MC1408L8	
SSS1508A-8Z	MC1508L8	
SSS1458J	MC1458G	
SSS1558J	MC1558G	
TAA630		MC1327P
TBA120S		MC1358P
TBA440		MC1352P
TBA520		MC1327P
TBA800		MC1384PQ
TBA810AS		MC1384PQM
TBA810S		MC1384PQ
TBA920		MC1391P
TBA920S		MC1391P
TBA940		MC1344P
TBA950		MC1344P
TBA990		MC1327P
TBA1190Z	TBA1190Z	
TL022CJG		MLM358U
TL022CL		MLM358G
TL022CP		MLM358P1
TL022MJG		MLM158U
TL022ML		MLM158G
TL044CJ		MLM324L
TL044CN		MLM324P
TL044MJ		MLM124L
TL497CJ		MC3420L
TL497CN		MC3420P
TL497MJ		MC3520L
UDN5711M	MC1471P1	
UDN5712M	MC1472P1	
UDN5713M	MC1473P1	
UDN5714M	MC1474P1	
UDN-7183A		MC3491P
UDN-7184A		MC3491P
UDN-7186A		MC3491P
UDN-6144A		MC3490P
UDN-6164A		MC3490P
UDN-6184A		MC3490P
UHD-490		MC3494P
UHP-490		MC3494P
UHD-491		MC3494P
UHP-491		MC3494P
UHP-495		MC3490P
ULN2001A	ULN2001A	
ULN2002A	ULN2002A	
ULN2003A	ULN2003A	
ULN2004A	ULN2004A	
ULN2111A	MC1357P	
ULN2111N	MC1357PQ	
ULN2113A		MC1357P
ULN2113N		MC1357P
ULN2114A		MC1323P
ULN2114K		MC1323P
ULN2114N		MC1323P
ULN2120A		MC1310P
ULN2121A		MC1310P
ULN2122A		MC1310P
ULN2124A		MC1399P
ULN2125A		MC1344P
ULN2126A		MC1303P
ULN2127A		MC1399P
ULN2128A		MC1310P
ULN2129A	MC1375P	
ULN2136A	MC1356P	
ULN2139D		MC1439G
ULN2139G		MC1439G
ULN2139H		MC1439P2
ULN2139M		MC1439P1
ULN2151D		MC1741CG
ULN2151G		MC1741CF
ULN2151H		MC1741CP2
ULN2151M		MC1741CP1
ULN2156D		MC1456G
ULN2156G		MC1456G
ULN2156H		MC1456G
ULN2156M		MC1456G
ULN2157A		MC1458P2
ULN2157H		MC1458P2
ULN2157K		MC1458G
ULN2165A	MC1358P	
ULN2165N	MC1358PQ	
ULN2209A		MC1356P
ULN2210A	MC1310P	
ULN2224A	MC1324P	
ULN2228A		MC1323P
ULN2244A		MC1310P
ULN2262A		MC1399P
ULN2264A	MC1364P	
ULN2267A		MC1323P
ULN2280A		MC1384PQ
ULN2285P		MC1384PQ
ULN2298A	MC1398P	
ULN2741D		MC1741CG
ULN2747A		MC1747CL
ULS2139D		MC1539G

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
ULS2139G		MC1539G
ULS2139H		MC1539L
ULS2139M		MC1439P1
ULS2151D		MC1741G
ULS2151G		MC1741F
ULS2151H		MC1741L
ULS2151M		MC1741CP1
ULS2156D		MC1556G
ULS2156G		MC1556G
ULS2156H		MC1556G
ULS2156M		MC1556G
ULS2157A		MC1558L
ULS2157H		MC1558L
ULS2157K		MC1558G
uA0802DC-1	MC1408L8	
uA0802DC-2	MC1408L7	
uA0802DC-3	MC1408L6	
uA0802DM-1	MC1508L8	
uA0802PC-1	MC1408P8	
uA0802PC-2	MC1408P7	
uA0802PC-3	MC1408P6	
uA101AD		MLM101AU
uA101AF		MLM101AP1
uA101AH	MLM101AG	
uA101D		MLM101AU
uA101F		MLM101AP1
uA101H	MLM101AG	
uA102M	MLM110G	
uA104HM	MLM104G	
uA105HM	MLM105G	
uA107H	MLM107G	
uA108AD	MLM108AL	
uA108AF	MLM108AF	
uA108AH	MLM108AG	
uA108D	MLM108L	
uA108F	MLM108F	
uA108H	MLM108G	
uA109KM	MLM109K	
uA110M	MLM110G	
uA201AD		MLM201AU
uA201AF		MLM201AP1
uA201AH	MLM201AG	
uA201D		MLM201AU
uA201F		MLM201AP1
uA201H	MLM201AG	
uA207H	MLM207G	
uA208AD	MLM208AL	
uA208AF	MLM208AF	
uA208AH	MLM208AG	
uA208D	MLM208L	
uA208F	MLM208F	
uA208H	MLM208G	
uA209KM	MLM209K	
uA301AD		MLM301AU
uA301AH	MLM301AG	
uA301AT	MLM301AP1	
uA302C	MLM310G	
uA304HC	MLM304G	
uA305AHC		MLM305G
uA305HC	MLM305G	
uA307H	MLM307G	
uA307T	MLM307P1	
uA308AD	MLM308AL	
uA308AH	MLM308AG	
uA308D	MLM308L	
uA308H	MLM308G	
uA309KC	MLM309K	
uA310CH	MLM310G	
uA311T	MLM311P1	
uA376TC		MLM305G
uA555HC	MC1455G	
uA555HM	MC1555G	
uA555TC	MC1455P1	
uA556DC	MC3456L	
uA556DM	MC3556L	
uA556PC	MC3456P	
uA702DC	MC1712CL	
uA702DM	MC1712L	
uA702FM	MC1712F	
uA702HC	MC1712CG	
uA702HM	MC1712G	
uA702MJ	MC1712L	
uA702ML	MC1712G	
uA706APC		MC1384PQ
uA709ADM	MC1709AL	
uA709AFM	MC1709AF	
uA709AHM	MC1709AG	
uA709AMJ	MC1709AL	
uA709AMJG	MC1709AU	
uA709AML	MC1709AG	
uA709CJ	MC1709CL	
uA709CJG	MC1709CU	
uA709CL	MC1709CG	
uA709CN	MC1709CP2	
uA709CP	MC1709CP1	
uA709DC	MC1709CL	
uA709DM	MC1709L	
uA709FM	MC1709F	
uA709HC	MC1709CG	
uA709HM	MC1709G	
uA709MJ	MC1709L	
uA709MJG	MC1709U	
uA709ML	MC1709G	
uA709TC	MC1709CP1	
uA709PC	MC1709CP2	
uA710CH	MC1710CF	
uA710DC	MC1710CL	
uA710DM	MC1710L	
uA710FM	MC1710F	
uA710HC	MC1710CG	
uA710HM	MC1710G	
uA710PC	MC1710CP	
uA711DC	MC1711CL	
uA711DM	MC1711L	
uA711FM	MC1711F	
uA711HC	MC1711CG	
uA711HM	MC1711G	
uA711PC	MC1711CP	
uA715DC		MC1741SCL
uA715DM		MC1741SL
uA715HC		MC1741SCG
uA715HM		MC1741SG
uA723CJ	MC1723CL	
uA723CL	MC1723CG	
uA723CN	MC1723CP	
uA723DC	MC1723CL	
uA723DM	MC1723L	
uA723HC	MC1723CG	
uA723HM	MC1723G	
uA723MJ	MC1723L	
uA723ML	MC1723G	
uA723PC	MC1723CP	
uA725AHM		MLM108AG
uA725EHC		MLM308AG
uA725HC		MLM308AG
uA725HM		MLM108AG
uA727HC		MC1420G
uA727HM		MC1520G
uA730HC		MC1420G
uA730HM		MC1520G
uA732DC		MC1310P
uA732PC		MC1310P
uA733CJ	MC1733CL	
uA733CL	MC1733CG	
uA733CN	MC1733CP	
uA733DC	MC1733CL	
uA733DM	MC1733L	
uA733FM	MC1733F	
uA733HC	MC1733CG	
uA733HM	MC1733G	
uA733MJ	MC1733L	
uA733ML	MC1733G	
uA734DC		MLM311L
uA734DM		MLM111L
uA734HC		MLM311G
uA734HM		MLM111G
uA739DC		MC1303P
uA739PC		MC1303P
uA740HC		LF355H
uA740HM		LF155H
uA741ADM		MC1741L
uA741AFM		MC1741F
uA741AHM		MC1741G
uA741CJ	MC1741CL	
uA741CJG	MC1741CU	
uA741CL	MC1741CG	
uA741CN	MC1741CP2	
uA741CP	MC1741CP1	
uA741DC	MC1741CL	
uA741DM	MC1741L	
uA741EDC		MC1741L
uA741EHC		MC1741G
uA741FC	MC1741CF	
uA741FM	MC1741F	
uA741HC	MC1741CG	
uA741HM	MC1741G	
uA741MJ	MC1741L	
uA741MJG	MC1741U	
uA741ML	MC1741G	
uA741RC	MC1741CU	
uA741RM	MC1741U	
uA741PC	MC1741CP2	
uA741TC	MC1741CP1	
uA742DC		CA3059
uA746DC		MC1323P
uA746HC		MC1323P
uA747ADM		MC1747L
uA747AHM		MC1747G
uA747CJ	MC1741CL	
uA747CL	MC1747CG	
uA747CN	MC1747CP2	
uA747DC	MC1747CL	
uA747DM	MC1747L	
uA747EDC	MC1747CCBM	
uA747EHC	MC1747CICM	
uA747HC	MC1747CG	
uA747HM	MC1747G	
uA747MJ	MC1747L	
uA747ML	MC1747G	
uA747PC	MC1747CP2	
uA748AFM		MC1748F
uA748AHM		MC1748G
uA748CJ	MC1748CL	
uA748CJG	MC1748CU	
uA748CL	MC1748CG	
uA748CN	MC1748CP2	
uA748CP	MC1748CP1	
uA748DC	MC1748CL	
uA748DM	MC1748L	
uA748FM	MC1748F	
uA748HC	MC1748CG	
uA748HM	MC1748G	
uA748MJ	MC1748L	
uA748MJG	MC1748U	
uA748ML	MC1748G	
uA748TC	MC1748CP1	
uA749DC		MC1435L
uA749DHC		MC1435G
uA749DM		MC1535L
uA749HC		MC1435G
uA749PC		MC1303P
uA753TC		MC1356P

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
uA754HC		MC1355P
uA754TC		MC1355P
uA757DC		MC1350P
uA757DM		MC1350P
uA758DC		MC1310P
uA758PC		MC1310P
uA767DC		MC1310P
uA767PC		MC1310P
uA772		MC1741S
uA775DC	MLM339L	
uA775DM	MLM139L	
uA775PC	MLM339P	
uA776DC		MC1776CG
uA776DM		MC1776G
uA776HC	MC1776CG	
uA776HM	MC1776G	
uA776TC	MC1776CP1	
uA777CJ		MLM308AU
uA777CJG		MLM308AU
uA777CL		MLM308AG
uA777CN		MLM308AP1
uA777CP		MLM308AP1
uA777DC		MLM308AU
uA777HC		MLM308AG
uA777MJ		MLM108AU
uA777MJG		MLM108AU
uA777ML		MLM108AG
uA777TC		MLM308AP1
uA780DC		MC1399P
uA780PC		MC1399P
uA781DC		MC1399P
uA781PC		MC1399P
uA786DC		MC1327P
uA787PC		MC1399P
uA791KC		MC1438R
uA791KM		MC1538R
uA791P5		MC1438R
uA796HC	MC1496G	
uA796HM	MC1596G	
uA796DC	MC1496L	
uA796DM	MC1596L	
uA798HC	MC3458G	
uA798HM	MC3558G	
uA798RC	MC3458U	
uA798RM	MC3558U	
uA798TC	MC3458P1	
uA799HC		MC1741G
uA799HM		MC1741G
uA1312PC	MC1312P	
uA1314PC	MC1314P	
uA1315PC	MC1315P	
uA1391PC	MC1391P	
uA1394PC	MC1394P	
uA1458CHC	MC1458CG	
uA1458CP	MC1458CP1	
uA1458CRC	MC1458CU	
uA1458CTC	MC1458CP1	
uA1458E	MC1458G	
uA1458HC	MC1558G	
uA1458P	MC1458P1	
uA1458RC	MC1458U	
uA1458TC	MC1458P1	
uA1558E	MC1558G	
uA1558HM	MC1558G	
uA2136PC	MC1356P	
uA2240DC		MC1455U
uA2240DM		MC1555G
uA2240PC		MC1455P1
uA3026HM		CA3054
uA3045		MC3346P
uA3046DC	MC3346P	
uA3054DC	CA3054P	
uA3064PC	MC1364P	
uA3065PC	MC1358P	

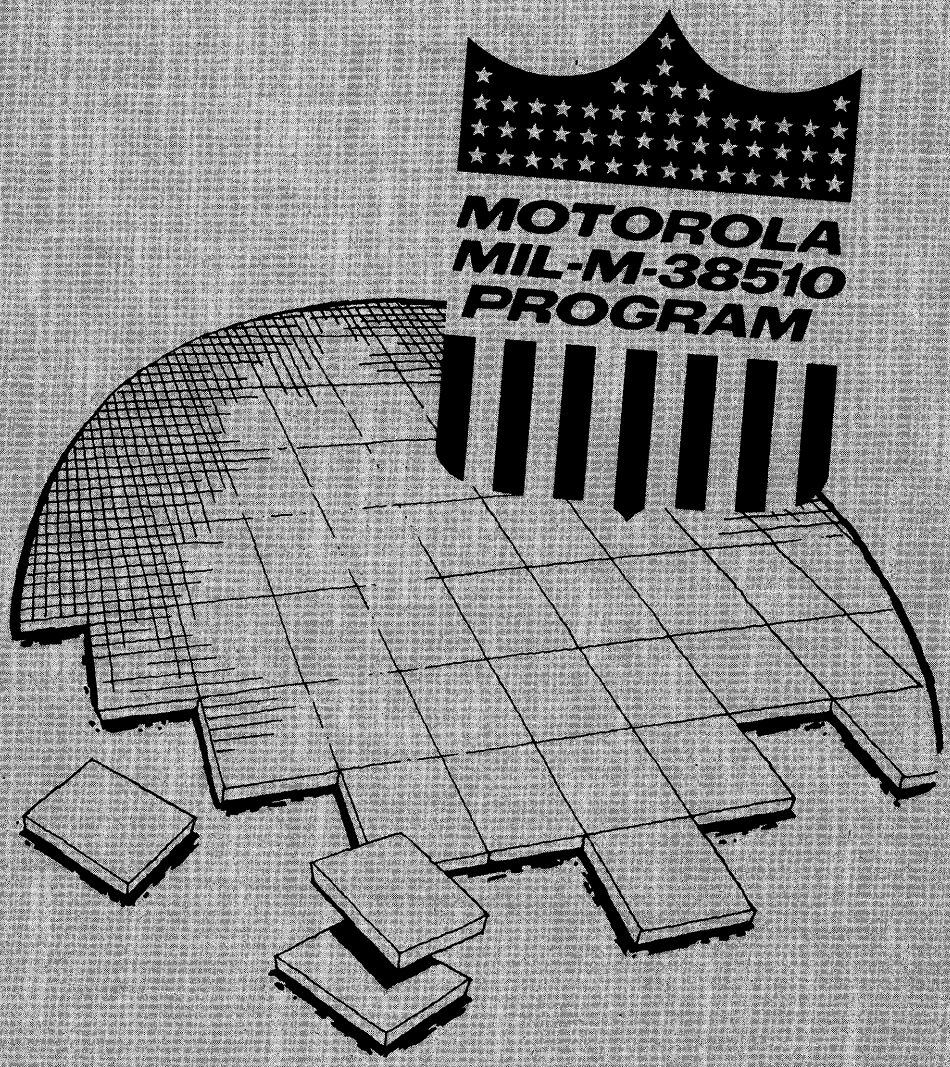
Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
uA3075PC	MC1375P	
uA3086DM	MC3386P	
uA3301P	MC3301P	
uA3302P	MC3302P	
uA3303P	MC3303P	
uA3401P	MC3401P	
uA3403D	MC3403L	
uA3403P	MC3403P	
uA4136DC		MC4741CL
uA4136DM		MC4741L
uA4136PC		MC4741CP
uA4558HC	MC4558CG	
uA4558HM	MC4558G	
uA4558TC	MC4558CP1	
uA7805CKC	MC7805CT	
uA7805KC	MC7805CK	
uA7805KM		MC7805CK
uA7805UC	MC7805CT	
uA7806CKC	MC7806CT	
uA7806KC	MC7806CK	
uA7806KM		MC7806CK
uA7806UC	MC7806CT	
uA7808CKC	MC7808CT	
uA7808KC	MC7808CK	
uA7808KM		MC7808CK
uA7808UC	MC7808CT	
uA7812CKC	MC7812CT	
uA7812KC	MC7812CK	
uA7812KM		MC7812CK
uA7812UC	MC7812CT	
uA7815CKC	MC7815CT	
uA7815KC	MC7815CK	
uA7815KM		MC7815CK
uA7815UC	MC7815CT	
uA7818CKC	MC7818CT	
uA7818KC	MC7818CK	
uA7818KM		MC7818CK
uA7818UC	MC7815CT	
uA7824CKC	MC7824CT	
uA7824KC	MC7824CK	
uA7824KM		MC7824CK
uA7824UC	MC7824CT	
uA78GHM		LM117K
uA78GKC		LM117K
uA78GKM		LM117K
uA78GU1C		LM317T
uA78H05KC		MC7805CK
uA78L02ACJG		MC78L02ACG
uA78L02ACLP	MC78L02ACP	
uA78L02CJG		MC78L02CG
uA78L02CLP	MC78L02CP	
uA78L05ACJG		MC78L05ACG
uA78L05ACLP	MC78L05ACP	
uA78L05AHC	MC78L05ACG	
uA78L05AWC	MC78L05ACP	
uA78L05CJG		MC78L05CG
uA78L05CLP	MC78L05CP	
uA78L05HC	MC78L05CG	
uA78L05WC	MC78L05CP	
uA78L06ACJG		MC78L06ACG
uA78L06ACLP	MC78L06ACP	
uA78L06CJG		MC78L06CG
uA78L06CLP	MC78L06CP	
uA78L08ACJG		MC78L08ACG
uA78L08ACLP	MC78L08ACP	
uA78L08CJG		MC78L08CG
uA78L08CLP	MC78L08CP	
uA78L12ACJG		MC78L12ACG
uA78L12ACLP	MC78L12ACP	
uA78L12AHC	MC78L12ACG	
uA78L12AWC	MC78L12ACP	
uA78L12CJG		MC78L12CG
uA78L12CLP	MC78L12CP	
uA78L12HC	MC78L12CG	

Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
uA78L12WC	MC78L12CP	
uA78L15ACJG		MC78L15ACG
uA78L15ACLP	MC78L15ACP	
uA78L15AHC	MC78L15ACG	
uA78L15AWC	MC78L15ACP	
uA78L15CJG		MC78L15CG
uA78L15CLP	MC78L15CP	
uA78L15HC	MC78L15CG	
uA78L15WC	MC78L15CP	
uA78L26AWC	MC7802ACP	
uA78MGHC		LM317H
uA78MGT2C		LM317T
uA78MGU1C		LM317T
uA78M05CKC	MC78M05CT	
uA78M05HC	MC78M05CG	
uA78M05HM		MC78M05CG
uA78M05UC	MC78M05CT	
uA78M06CKC	MC78M06CT	
uA78M06HC	MC78M06CG	
uA78M06HM		MC78M06CG
uA78M06UC	MC78M06CT	
uA78M08CKC	MC78M08CT	
uA78M08HC	MC78M08CG	
uA78M08HM		MC78M08CG
uA78M08UC	MC78M08CT	
uA78M12CKC	MC78M12CT	
uA78M12HC	MC78M12CG	
uA78M12HM		MC78M12CG
uA78M12UC	MC78M12CT	
uA78M15CKC	MC78M15CT	
uA78M15HC	MC78M15CG	
uA78M15HM		MC78M15CG
uA78M15UG	MC78M15CT	
uA78M18HC	MC78M18CG	
uA78M18HM		MC78M18CG
uA78M18UG	MC78M18CT	
uA78M20CKC	MC78M20CT	
uA78M20HC	MC78M20CG	
uA78M20HM		MC78M20CG
uA78M20UG	MC78M20CT	
uA78M24CKC	MC78M24CT	
uA78M24HC	MC78M24CG	
uA78M24HM		MC78M24CG
uA78M24UC	MC78M24CT	
uA7902KC	MC7902K	
uA7902KM		MC7902K
uA7902UC	MC7902CT	
uA7905KC	MC7905CK	
uA7905KM		MC7905CK
uA7905UC	MC7905CT	
uA7906KC	MC7906CK	
uA7906KM		MC7906CK
uA7906UC	MC7906CT	
uA7908KC	MC7908CK	
uA7908KM		MC7908CK
uA7908UC	MC7908CT	
uA7912KC	MC7912CK	
uA7912KM		MC7912CK
uA7912UC	MC7912CT	
uA7915KC	MC7915CK	
uA7915KM		MC7915CK
uA7915UC	MC7915CT	
uA7918CKC	MC7918CT	
uA7918KC	MC7918CK	
uA7918KM		MC7918CK
uA7918UC	MC7918CT	
uA7924CKC	MC7924CT	
uA7924KC	MC7924CK	
uA7924KM		MC7924CK
uA7924UC	MC7924CT	
uA79L05AHC	MC79L05ACG	
uA79L05AWC	MC79L05ACP	
uA79L05HC	MC79L05CG	
uA79L05WC	MC79L05CP	

LINEAR INTEGRATED CIRCUITS CROSS REFERENCE

Part No.	Motorola Direct Replacement	Motorola Functional Equivalent
uA79L12AHC	MC79L12ACG	
uA79L12AWC	MC79L12ACP	
uA79L12HC	MC79L12CG	
uA79L12WC	MC79L12CP	
uA79L15AHC	MC79L15ACG	
uA79L15AWC	MC79L15ACP	
uA79L15HC	MC79L15CG	
uA79L15WC	MC79L15CP	
uA79M05AHM		MC7905CK
uA79M05AUC		MC7905CT
uA79M05CKC	MC7905CT	
uA79M05HM		MC7905CK
uA79M05UC		MC7905CT
uA79M06AHM		MC7906CK
uA79M06AUC		MC7906CT
uA79M06CKC	MC7906CT	
uA79M06HM		MC7906CK
uA79M06UC		MC7906CT
uA79M08AHM		MC7908CK
uA79M08AUC		MC7908CT
uA79M08CKC	MC7908CT	
uA79M08HM		MC7908CK
uA79M08UC		MC7908CT
uA79M12AHM		MC7912CK
uA79M12AUC		MC7912CT
uA79M12CKC	MC7912CT	
uA79M12HM		MC7912CK
uA79M12UC		MC7912CT
uA79M15AHM		MC7915CK
uA79M15AUC		MC7915CT
uA79M15CKC	MC7915CT	
uA79M15HM		MC7915CK
uA79M15UC		MC7915CT
uA79M18AHM		MC7918CK
uA79M18AUC		MC7918CT
uA79M18HM		MC7918CK
uA79M18UC		MC7918CT
uA79M24AHM		MC7924CK
uA79M24AUC		MC7924CT
uA79M24HM		MC7924CK
uA79M24UC		MC7924CT
uA8T13DC	MC8T13L	
uA8T13PC	MC8T13P	
uA8T14DC	MC8T14L	
uA8T14PC	MC8T14P	
uA8T23DC	MC8T23L	
uA8T23PC	MC8T23P	
uA8T24DC	MC8T24L	
uA8T24PC	MC8T24P	
uAF155AHM	LF155AH	
uAF155HM	LF155H	
uAF156AHM	LF156AH	
uAF156HM	LF156H	
uAF157AHM	LF157AH	
uAF157HM	LF157H	
uAF355AHC	LF355AH	
uAF355HC	LF355H	
uAF356AHC	LF356AH	
uAF356HC	LF356H	
uAF357AHC	LF357AH	
uAF357HC	LF357H	

MIL-M-38510 Program and Chip Information / Chapter 2



THE MOTOROLA MIL-M-38510 PROGRAM

2

Motorola, a pioneer in the manufacture of *high-reliability* integrated circuits*, now offers you a two-way program for MIL-M-38510 products.

1. A growing line of JAN-**QUALIFIED** integrated circuits.
2. An extensive program to supply MIL-M-38510 PROCESSED devices that approaches the Qualified Reliability goals without the delay time and high cost of the actual qualification program.

Motorola stocks many circuits which meet JAN-QUALIFIED specifications, and is actively persuing an expansion of this qualification listing with product in all IC categories — encompassing Bipolar Digital, Linear and MOS technologies.

Motorola 38510 PROCESSED products complement JAN-QUALIFIED products by making available hi-rel versions of nearly all Motorola full-temperature range circuits, while adding the advantage of *hi-rel standardization.*

THE MOTOROLA MIL-M-38510 PROGRAM OFFERS YOU THESE BENEFITS:

1. Standardization of environmental and electrical test procedures.
2. Less specification writing required.
3. Less time required in negotiating specifications.
4. Fast delivery.
5. Lower costs.

*Motorola, in early 1971, was the first company to be qualified as a MIL-M-38510 approved facility by the Defense Electronics Supply Center of DOD.

MIL-M-38510 JAN-QUALIFIED PRODUCT

SCREENING LEVELS

Class A | Class B | Class C

JAN-QUALIFIED DEVICE MARKINGS

APPLIES TO ALL TYPES OF INTEGRATED CIRCUITS

JM38510/XXXXX**A**YY JM38510/XXXXX**B**YY JM38510/XXXXX**C**YY

FEATURES:

1. Manufactured in a government-approved facility.
2. G.S.I. (Government Source Inspection) provided upon request.

Example of MIL-M-38510 **JAN-Qualified** markings

ORDER: JM38510/10101BGB

MARKING: JM38510/10101BGB

HOW TO ORDER MIL-M-38510 JAN-QUALIFIED PRODUCT

Basic Numbering Parameters — Example: JM38510/XXXXXYYY

J	M38510	/XXX	XX	Y	Y	Y
INDICATES A QUALIFIED DEVICE	MILITARY DESIGNATOR	DETAIL SPECIFICATION NUMBER	DEVICE TYPE WITHIN DETAIL SPECIFICATION	CLASS A, B, OR C (SEE DEVICE CLASS TABLE)	CASE OUTLINE (SEE CASE OUTLINE TABLE)	LEAD FINISH (SEE LEAD FINISH TABLE)

CASE OUTLINE TABLE

A — ¼″ x ¼″ flat pack, 14-pin
C — ¼″ x ¾″ dual-in-line, 14-pin
E — ¼″ x ¾″ dual-in-line, 16-pin
F — ¼″ x ⅜″ flat pack, 16-pin
G — 8-lead can
H — ¼″ x ¼″ flat pack, 10-lead
I — 10-lead can
J — ½″ x 1¼″ dual-in-line, 24-pin
K — ⅜″ x ½″ flat pack, 24-pin
X — 3-lead can
Y — 2-lead power can

LEAD FINISH TABLE

A — Kovar or Alloy 42, with hot solder dip
B — Kovar or Alloy 42, with acid tin plate
C — Kovar or Alloy 42, with gold plate
X — Any of the above, for ordering purposes only.

MIL-M-38510 PROCESSED PRODUCT

2

SCREENING LEVELS

Class A | Class B | Class D | Class C

PROCESSED DEVICE MARKINGS

APPLIES TO ALL TYPES OF INTEGRATED CIRCUITS

MC38510/XXXX**A**YY**M**	MC38510/XXXX**B**YY**M**	MC38510/XXXX**D**YY**M**	MC38510/XXXX**C**YY**M**
MC38510/XXXX**A**YY**S**	MC38510/XXXX**B**YY**S**	MC38510/XXXX**D**YY**S**	MC38510/XXXX**C**YY**S**

FEATURES:

1. Lower cost than JAN-QUALIFIED.
2. Devices manufactured using design and processing guidelines contained in MIL-M-38510.
3. Product supplied with Motorola standard data sheet electricals ("S" suffix) or MIL-M-38510 electricals ("M" suffix).
4. G.S.I. (Government Source Inspection) provided upon request.

Example of MIL-M-38510 **Processed** markings

DEVICE: MC1741BGBS

ORDER: MC1741BGBS

MARKING: MC38510/1741BGBS

HOW TO ORDER MIL-M-38510 PROCESSED PRODUCT

Basic Numbering Parameters — Example: MCXXXXYYYS or M

MCXXXX Y Y Y S or M

- MCXXXX — MOTOROLA DEVICE TYPE
- Y — CLASS A, B, C, OR D (SEE DEVICE CLASS TABLE)
- Y — CASE OUTLINE (SEE CASE OUTLINE TABLE)
- Y — LEAD FINISH (SEE LEAD FINISH TABLE)
- S or M — S = MOTOROLA DATA SHEET ELECTRICALS; M = JAN SLASH SHEET ELECTRICALS

CASE OUTLINE TABLE

A — ¼″ x ¼″ flat pack, 14-pin
C — ¼″ x ¾″ dual-in-line, 14-pin
E — ¼″ x ¾″ dual-in-line, 16-pin
F — ¼″ x ⅜″ flat pack, 16-pin
G — 8-lead can
H — ¼″ x ¼″ flat pack, 10-lead
I — 10-lead can, pin 10 at tab
J — ½″ x 1¼″ dual-in-line, 24-pin
K — ⅜″ x ½″ flat pack, 24-pin
X — 3-lead can
Y — 2-lead power can

*3 — 8-lead dual-in-line
*8 — 10-lead can, pin 1 at tab
*9 — 10-lead tall can
*R — 9-lead power can

*Linear processed devices only.

LEAD FINISH TABLE

A — Kovar or Alloy 42, with hot solder dip
B — Kovar or Alloy 42, with acid tin plate
C — Kovar or Alloy 42, with gold plate
X — Any of the above, for ordering purposes only.

SCREENING PROCEDURES

FOR MIL-M-38510 JAN-QUALIFIED AND MIL-M-38510 PROCESSED PRODUCT

(TO MIL-STD-883 REQUIREMENTS)

In recognition of the fact that the level of screening has a direct impact on the cost of the product, as well as its quality and reliability, four standard levels of screening are provided to coincide with four device classes, or levels of quality assurance.

Flexibility is provided in the choice of test conditions and stress levels, to provide screens tailored to a particular product or application. Selection of a level **better** than that required for the specific product and application will result in unnecessary expense. A level **less** than that required may result in a risk that reliability requirements will not be met. For general hi-rel applications, the Class B or D screening levels should be considered.

DEVICE CLASS TABLE

	CLASS A		CLASS B		CLASS D[1]		CLASS C	
SCREEN	**METHOD**	**RQMT**	**METHOD**	**RQMT**	**METHOD**	**RQMT**	**METHOD**	**RQMT**
Internal Visual (Precap)	2010 Condition A and 38510	100%	2010 Condition B and 38510	100%	2010 Condition B and 38510	100%	2010 Condition B and 38510	100%
Stabilization Bake	1008, 24 hrs min. test Condition C	100%	1008, 24 hrs min. test Condition C	100%	1008, 24 hrs min. test Condition C	100%	1008, 24 hrs min. test Condition C	100%
Temperature Cycling	1010 Condition C	100%	1010 Condition C	100%	1010 Condition C	100%	1010 Condition C	100%
Constant Acceleration	2001 Condition E (min.) Y1 plane	100%	2001 Condition E (min.) Y1 plane	100%	2001 Condition E (min.) Y1 plane	100%	2001 Condition E (min.) Y1 plane	100%
Seal (a) Fine (b) Gross			1014	100%	1014	100%	1014	100%
Serialization		100%		—		—		—
Interim Electrical Parameters	Per applicable device specification[2]	100%	Per applicable device specification[2]	[3]	Per applicable device specification[2]	[3]		—
Burn-in Test	1015 240 hrs @ 125°C min.	100%	1015 160 hrs @ 125°C min.	100%	1015 160 hrs @ 125°C min.	100%		—
Interim Electrical Parameters	Per applicable device specification[2]	100%		—		—		—
Reverse Bias Burn-in	1015 Condition A or C 72 hrs at 150°C min.	100%		—		—		—
Interim Electrical Parameters	Per applicable device specification[2]	100%	Per applicable device specification[2]	100%	Per applicable device specification[2]	100%		—
Seal (a) Fine (b) Gross	1014	100%		—		—		—
Final Electrical Tests (a) Static tests (1) 25°C (subgroup 1, table 1, 5005)	Per applicable device specification[2]	100%	Per applicable device specification[2]	100%	Per applicable device specification[2]	100%	Per applicable device specification[2]	100%
(2) Max. and min. rated operating temp. (subgroups 2 and 3, table 1, 5005)		100%		100%		Sample at Group A		Sample at Group A
(b) Dynamic tests and/or switching tests @ 25°C (subgroup 4 and 9, table 1, 5005)		100%		100%		Sample at Group A		Sample at Group A
(c) Functional test @ 25°C (subgroup 7, table 1, 5005)		100%		100%		100%		100%
Radiographic	2012	100%		—		—		—
Qualification or Quality Conformance Inspection	5005 Class A	Sample per 38510[4]	5005 Class B	Sample per 38510[4]	5005 Class B	Sample per 38510[4]	5005 Class	Sample per 38510[4]
External Visual	2009	100%	2009	100%	2009	100%	2009	100%

[1] For MIL-M-38510 PROCESSED product only.

[2] MIL-M-38510 QUALIFIED product is tested per applicable 38510 detail specification. MIL-M-38510 PROCESSED product is tested per applicable 38510 detail specification ("M" suffix), or per the Motorola standard data sheet electrical specification ("S" suffix).

[3] When specified in the applicable device specification 100% of the devices shall be tested.

[4] For MIL-M-38510 PROCESSED product, Group A is performed per 5005 and Groups B, C, and D are available upon request.

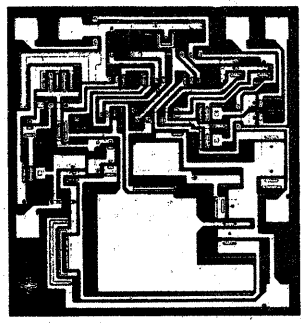
CHIPS

Most of the linear integrated circuit devices in this Data Book are available in chip form. Many are offered in two options – conventional (face up bonding) and flip-chip versions. Motorola offers many standard linear chips from warehouse stock either directly from the factory or through franchised distributors. In addition, custom linear IC chips may be designed and to meet a specific need.

Specific information on chip processing, testing, and handling can be obtained in the **Chips Data Book** *(Volume 8 of the Motorola* **Semiconductor Data Library***).*

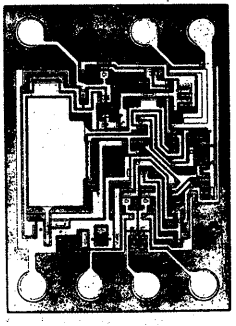
LINEAR CHIP FORMATS

Conventional Chips encompass by far the greatest number of available linear IC chips. These silicon chips use gold backside metalization for easy eutectic bonding to the metalized area of hybrid assemblies. The interconnecting metalization and bonding pad areas are formed from evaporated aluminum. Either gold or aluminum wire may be employed for connection between on-chip bonding pads and the external circuit.

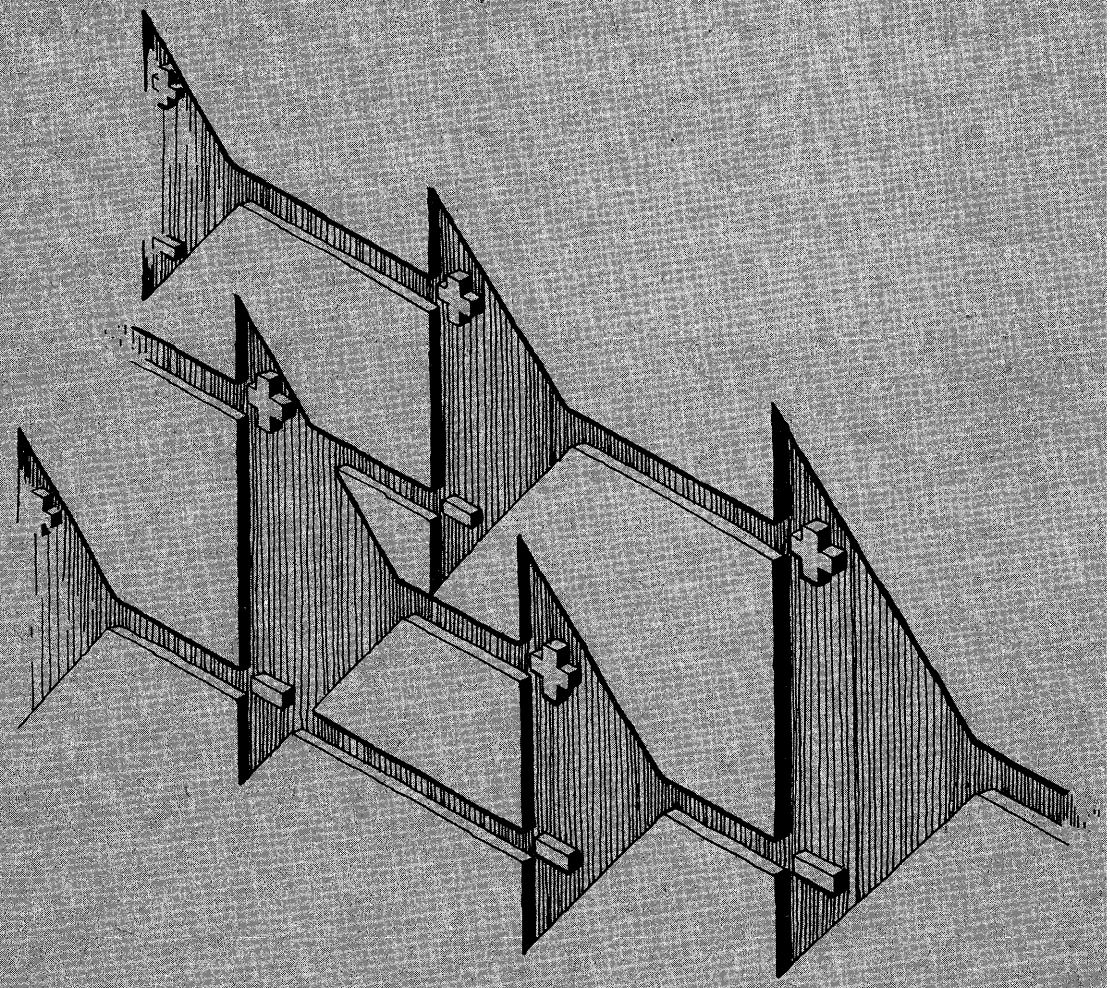


Flip-chips can be mounted to a hybrid substrate in a single operation.

Connection to the substrate bonding pads is made by means of raised "solder bumps" that protrude above the chip surface at the integrated-circuit bonding pads. The devices are mounted to the substrate metalization areas circuit side down by means of conventional reflow solder techniques.



Operational Amplifiers / Chapter 3



OPERATIONAL AMPLIFIERS

Temperature Range 0 to 70°C	Temperature Range -55 to 125°C	Other		Page
LF355,A	LF155,A	–	Monolithic JFET Operational Amplifier	3-7
LF356,A	LF156,A	–	Monolithic JFET Operational Amplifier	3-7
LF357,A	LF157,A	–	Monolithic JFET Operational Amplifier	3-7
MC1420	MC1520	–	Differential Output Operational Amplifier	3-12
MC1430	MC1530	–	General Purpose Operational Amplifier	3-16
MC1431	MC1531	–	Darlington Input Operational Amplifier	3-16
MC1433	MC1533	–	General Purpose Operational Amplifier	3-20
MC1435	MC1535	–	Dual Operational Amplifier	3-25
MC1436,C	MC1536	–	High Voltage Operational Amplifier	3-30
MC1437	MC1537	–	Dual MC1709 Operational Amplifier	3-34
MC1439	MC1539	–	High Slew Rate Operational Amplifier	3-38
MC1456,C	MC1556	–	High Performance Operational Amplifier	3-46
MC1458,C	MC1558	–	Dual MC1741 Operational Amplifier	3-52
MC1458N	MC1558N	–	Low Noise Dual Operational Amplifier	3-52
MC1458S	MC1558S	–	High Slew Rate Dual Operational Amplifier	3-57
MC1709C	MC1709,A	–	General Purpose Operational Amplifier	3-63
MC1712C	MC1712	–	Wideband DC Amplifier	3-67
MC1741C	MC1741	–	General Purpose Operational Amplifier	3-72
MC1741NC	MC1741N	–	Low Noise Operational Amplifier	3-72
MC1741SC	MC1741S	–	High Slew Rate Operational Amplifier	3-77
MC1747C	MC1747	–	Dual MC1741 Operational Amplifier	3-83
MC1748C	MC1748	–	General Purpose Operational Amplifier	3-87
MC1776C	MC1776	–	Programmable Operational Amplifier	3-91
–	–	MC3301	Quad Operational Amplifier	3-100
MC3401	–	–	Quad Operational Amplifier	3-108
MC3403	MC3503	MC3303	Quad Differential Input Operational Amplifier	3-116
MC3458	MC3558	MC3358	Dual Operational Amplifier	3-122
MC3471	MC3571	–	Quad FET Input Operational Amplifier	3-128
MC3476	–	–	Programmable Operational Amplifier	3-130
MC4202C	–	–	Programmable Quad Operational Amplifier	3-134
MC4558C	MC4558	–	Dual High Frequency Operational Amplifier	3-138
MC4741C	MC4741	–	Quad MC1741 Operational Amplifier	3-140
MLM301A	MLM101A	MLM201A	General Purpose Operational Amplifier	3-146
MLM307	MLM107	MLM207	General Purpose Operational Amplifier	3-150
MLM308,A	MLM108,A	MLM208,A	Precision Operational Amplifier	3-154
MLM310	MLM110	MLM210	Unity Gain Operational Amplifier	3-159
MLM324	MLM124	MLM224	Quad Operational Amplifier	3-161
MLM358	MLM158	MLM258	Dual Operational Amplifier	3-167
–	–	MLM2902	Quad Operational Amplifier	3-173

Single Operational Amplifiers

NONCOMPENSATED

Devices listed in ascending order of price

I_{IB} μA max	V_{IO} mV max	TC_{VIO} μV/°C typ	I_{IO} nA max	A_{vol} V/V min	BW(Av=1) MHz typ	SR(Av=1) V/μs typ	Supply Voltage V min	Supply Voltage V max	Description	Device	Packages
Military Temperature Range (-55°C to +125°C)											
.5	5	15	200	25K	1	.3	±3	±18	General Purpose	MC1709	601, 606, 632, 693
.5	5	15	200	50K	1	.5	±3	±22	General Purpose	MC1748	601, 693
.075	2	10	10	50K	1	.5	±3	±22	General Purpose	MLM101A	601, 693
.5	3	15	60	50K	2	4.2	±4	±18	High Slew Rate	MC1539	601, 632
5	2	15	500	2.5K	7	1.5	+12 -6	+12 -6	Wideband DC Amplifier	MC1712	601, 606, 632
1	5	15	150	40K	.8	2.0	±4	±20	General Purpose	MC1533	602B, 606, 632
2	10	15	100	1K	10	5.0	±4	±8	Differential Output	MC1520	602A, 606
.6	3	5	100	25K	1	.5	±3	±18	High Performance MC1709	MC1709A	601, 606, 632
.002	2	3	.2	50K	1	.3	±3	±20	Precision	MLM108	601, 606, 693
10	5	15	2000	4.5K	3	1.0	±4	±9	General Purpose	MC1530	602B, 606, 632
15	10	15	25	2.5K	2	1.0	±4	±9	General Purpose (Darlington Input)	MC1531	602B, 606, 632
.002	.5	1	.2	80K	1	.3	±3	±20	Precision	MLM108A	601, 606, 693
Industrial Temperature Range (0°C to +70°C)											
.25	7.5	10	50	25K	1	.5	±3	±18	General Purpose	LM301A	601, 626 693
.5	6	15	200	20K	1	.5	±3	±18	General Purpose	MC1748C	601, 626 693
1.5	7.5	15	500	15K	1	.3	±3	±18	General Purpose	MC1709C	601, 606, 626, 632, 646, 693
7	7.5	15	1	25K	1	.3	±3	±18	Precision	LM308	601, 606, 626, 693
7.5	5	15	2000	2K	7	1.5	+12 -6	+12 -6	Wideband DC Amplifier	MC1712C	601, 606, 632
4	15	15	200	750	10	5.0	±4	±8	Differential Output	MC1420	602A, 606
1	7.5	15	100	15K	2	4.2	±6	±18	High Slew Rate	MC1439	601, 626, 632, 646
2	7.5	15	50	30K	.8	2.0	±4	±18	General Purpose	MC1433	602B, 606, 632, 646
7	.5	5	1	80K	1	.3	±3	±18	Precision	LM308A	601, 606, 626, 693
15	10	15	4000	3K	3	1.0	±4	±8	General Purpose	MC1430	602B, 606, 632, 646
.3	15	15	100	1.5K	2	1.0	±4	±8	General Purpose (Darlington Input)	MC1431	602B, 606, 632, 646

Single Operational Amplifiers

INTERNALLY COMPENSATED

Devices listed in ascending order of price

I_{IB} uA max	V_{IO} mV max	TC_{VIO} uV/°C typ	I_{IO} nA max	A_{vol} V/V min	BW(Av=1) MHz typ	SR(Av=1) V/us typ	Supply Voltage V min	Supply Voltage V max	Description	Device	Packages
Military Temperature Range (-55°C to +125°C)											
.5	5	15	200	50K	1	.5	±3	±22	General Purpose	MC1741	601, 606, 632, 693
.20	-	-	3000	90	90	-	±4	±8	Differential Wide-band Video Amp	MC1733	603, 632
.5	5	15	200	50K	1	.5	±3	±22	Low Noise	MC1741N	601, 606 632, 693
.5	5	15	200	50K	1	10	±3	±22	High Slew Rate	MC1741S	601, 632, 693
.075	2	10	10	50K	1	.5	±3	±22	General Purpose	MLM107	601, 693
.003	4	12	-	Unity	20	30	±3	±18	Unity Gain	MLM110	601
.015	4	10	2	100K	1	2.5	±3	±22	High Performance	MC1556	601, 632
.0075	5	15	3	200K	1	.2	±1.5	±18	uPower Programmable	MC1776	601, 632
.02	5	10	3	100K	1	2.0	±15	±40	High Voltage	MC1536	601
100pA	5	5	20pA	50K	1	5	±5	±22	FET Input	LF155	601*
100pA	5	5	20pA	50K	2	15	±5	±22	FET Input	LF156	601*
100pA	5	5	20pA	50K	3	75	±5	±22	Wideband FET Input	LF157	601*
50pA	2	3	10pA	50K	1	5	±5	±22	FET Input	LF155A	601*
50pA	2	3	10pA	50K	2	15	±5	±22	FET Input	LF156A	601*
50pA	2	3	10pA	50K	3	75	±5	±22	Wideband FET Input	LF157A	601*

*This Circuit to be Introduced

I_{IB} uA max	V_{IO} mV max	TC_{VIO} uV/°C typ	I_{IO} nA max	A_{vol} V/V min	BW(Av=1) MHz typ	SR(Av=1) V/us typ	Supply Voltage V min	Supply Voltage V max	Description	Device	Packages
Industrial Temperature Range (0°C to +70°C)											
.5	6	15	200	20K	1.0	.5	±3	±18	General Purpose	MC1741C	601, 632, 626, 646, 693
.25	7.5	10	50	25K	1.0	.5	±3	±18	General Purpose	MLM307	601, 626, 693
30	-	-	5000	80	90	-	±4	±8	Differential Wide-band Video Amp	MC1733C	601, 632, 646
.05	6	15	25	50K	1.0	.2	±1.5	±18	Low Cost uPower, Programmable	MC3476	601, 626
.5	6	15	200	20K	1.0	.5	±3	±18	Low Noise	MC1741NC	601, 632, 626, 646, 693
.5	6	15	200	20K	1.0	10	±3	±18	High Slew Rate	MC1741SC	601, 632, 626, 646, 693
.007	7.5	12	-	Unity	20.0	30	±3	±18	Unity Gain	MLM310	601
.003	6	15	3	100K	1.0	.2	±1.5	±18	uPower, Programmable	MC1776C	601
.03	10	12	10	70K	1.0	2.5	±3	±18	High Performance	MC1456	601, 632
.04	10	12	10	70K	1.0	2.0	±15	±34	High Voltage	MC1436	601
200pA	10	5	50pA	50K	1.0	5	±5	±18	FET Input	LF355	601*
200pA	10	5	50pA	50K	2.0	15	±5	±18	FET Input	LF356	601*
200pA	10	5	50pA	50K	3.0	75	±5	±18	Wideband FET Input	LF357	601*
50pA	2	1	10pA	50K	1.0	5	±5	±18	FET Input	LF355A	601*
50pA	2	1	10pA	50K	2.0	15	±5	±18	FET Input	LF356A	601*
50pA	2	1	10pA	50K	3.0	75	±5	±18	Wideband FET Input	LF357A	601*

*This Circuit to be Introduced

Dual Operational Amplifiers

INTERNALLY COMPENSATED

Devices listed in ascending order of price

I_{IB} uA max	V_{IO} mV max	TC_{VIO} uV/°C typ	I_{IO} nA max	A_{vol} V/V min	BW(Av=1) MHz typ	SR(Av=1) V/us typ	Supply Voltage V min	Supply Voltage V max	Description	Device	Packages
Military Temperature Range (-55°C to +125°C)											
.5	5	10	200	50K	1.1	.8	±3	±22	Dual MC1741	MC1558	601, 632 693
.5	5	10	200	50K	1	.5	±3	±22	Dual MC1741	MC1747	601, 632
.5	5	10	200	50K	1.1	.8	±3	±22	Dual Low Noise	MC1558N	601, 632, 693
.5	5	10	200	50K	4	1.5	±3	±22	High Frequency Dual	MC4558	601, 632 693
.15	5	10	30	50K	1	.6	±1.5 +3	±18 +36	Single Supply Dual (Low Power Consumption)	MLM158	601, 632, 693
.5	5	10	200	50K	1	10	±3	±22	High Slew Rate Dual	MC1558S	601, 632, 693
.5	5	10	50	50K	1	.6	±1.5 +3	±18 +36	Single Supply Dual	MC3558	601, 632, 693
Industrial Temperature Range (0°C to +70°C)											
.5	6	10	200	20K	1.1	.8	±3	±18	Dual MC1741	MC1458	601, 626, 632, 646, 693
.5	6	10	200	25K	1	.5	±3	±18	Dual MC1741	MC1747C	603, 632, 646
.25	6	7	50	25K	1	.6	±1.5 +3.0	±18 +36	Single Supply Dual (Low Power Consumption)	MLM358	601, 626, 693
.5	6	10	200	20K	3	1.5	±3	±18	Dual High Frequency	MC4558C	601, 626 693
.5	10	7	50	20K	1	.6	±1.5 +3.0	±18 +36	Single Supply Dual (Low Crossover Distortion)	MC3458	601, 626 693
.5	6	10	200	20K	1	10	±3	±18	High Slew Rate Dual	MC1458S	601, 626, 632, 646, 693
.5	6	10	200	20K	1.1	.8	±3	±18	Dual Low Noise	MC1458N	601, 626, 632, 646, 693
Automotive Temperature Range (-40°C to +85°C)											
5	8	10	75	20K	1	.6	±1.5 +3	±18 +36	Single Supply Dual	MC3358	626

NONCOMPENSATED

Military Temperature Range (-55°C to +125°C)											
.5 3	5 3	10 10	200 300	25K 4K	1 1	.25 .01	±3 ±2	±18 ±10	Dual MC1709 Dual General Purpose	MC1537 MC1535	632 601, 606, 632
Industrial Temperature Range (0°C to +70°C)											
1.5 5	7.5 5	10 10	500 500	15K 3.5K	1 1	.25 .01	±3 ±2	±18 ±9	Dual MC1709 Dual General Purpose	MC1437 MC1435	632, 646 602B, 607 632

Quad Operational Amplifiers

INTERNALLY COMPENSATED

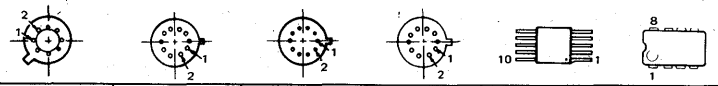
Devices listed in ascending order of price

I_{IB} uA max	V_{IO} mV max	TC_{VIO} uV/°C typ	I_{IO} nA max	A_{vol} V/V min	BW(Av=1) MHz typ	SR(Av=1) V/us typ	Supply Voltage V min	Supply Voltage V max	Description	Device	Packages
Military Temperature Range (-55°C to +125°C)											
.5	5	15	200	50K	1	.5	±3	±22	Quad MC1741	MC4741	632, 646
.15	5	7	30	50K	1	.6	±1.5 +3.0	±16 +32	Quad (Lower Power Consumption)	MLM124	632, 646
.5	5	7	50	50K	1	.6	±1.5 +3.0	±18 +36	Quad General Purpose Low Power	MC3503	632, 646
200pA	5	10	20pA	50K	10	20	±3.0	±18	Quad Active Filter FET Input, High Frequency	MC3571	632, 646*
Industrial Temperature Range (0°C to 10°C)											
.3	-	-	-	1K	5	.6	±1.5 +3.0	±18 +36	Low Cost Quad	MC3401	632, 646
.25	6	7	50	25K	1	.6	±1.5 +3.0	±16 +32	Quad (Low Power Consumption)	MLM324	632, 646
.5	10	7	50	20K	1	.6	±1.5 +3.0	±18 +36	Quad (No Crossover Distortion)	MC3403	632, 646
.5	6	15	200	20K	1	.5	±3	±18	Quad MC1741	MC4741C	632, 646
.1	5	10	10	10K	5	1.5	±1.5	±18	Quad Programmable Low Power	MC4202C	632, 646*
200pA	6	10	20pA	25K	10	20	±3.0	±18	Quad Active Filter FET Input, High Frequency	MC3471	632, 646*

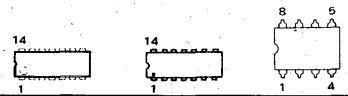
*This Circuit to be Introduced

Automotive Temperature Range (-40°C to +85°C)											
.3	-	-	-	1K	4	.6	±2 +4	±15 +28	Quad Mirror Gain	MC3301	646
.5	10	-	50	-	1	.6	±1.5 +3	±13 +26	Quad Diff. (Low Power)	MLM2902	646
.5	8	10	75	20K	1	.6	±1.5 +3	±18 +36	Quad Diff. General Purpose	MC3303	646

PACKAGE STYLES



CASE	601	602A	602B	603	606	626
MATERIAL	Metal	Metal	Metal	Metal	Ceramic	Plastic
SUFFIX after type number	G	G	G	G	F	P,P1,N



CASE	632	646	693
MATERIAL	Ceramic	Plastic	Ceramic
SUFFIX after type number	L	P	U

LF155•LF156•LF157*
LF155A•156A•157A
LF355•LF356•LF357
LF355A•356A•357A

Advance Information

MONOLITHIC
JFET
OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

3

MONOLITHIC JFET INPUT OPERATIONAL AMPLIFIERS

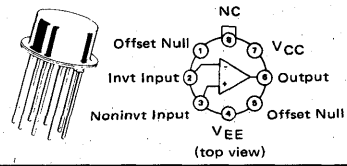
These internally compensated operational amplifiers incorporate highly matched JFET transistors on the same chip with standard bipolar transistors. The JFET transistors enhance the input characteristics of these operational amplifiers by more than an order of magnitude over conventional amplifiers.

This series of op amps combines the low current characteristics typical of FET amplifiers with the low initial offset voltage and offset voltage stability of bipolar amplifiers. Also nulling the offset voltage does not degrade the drift or common mode rejection.

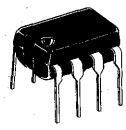
- Low Input Bias Current – 30 pA
- Low Input Offset Current – 3.0 pA
- Low Input Offset Voltage – 1.0 mV
- Temperature Compensation of Input Offset Voltage – 3.0 $\mu V/^{o}C$
- Low Input Noise Current – 0.01 $pA/\sqrt{Hz}$
- High Input Impedance – $10^{12}\Omega$
- High Common-Mode Rejection Ratio – 100 dB
- High DC Voltage Gain – 106 dB

	LF155A	LF156A	LF157A
Fast Settling Time to 0.01%	4.0 μs	1.5 μs	1.5 μs
Fast Slew Rate	5.0 $V/\mu s$	12 $V/\mu s$	50 $V/\mu s$
Wide Gain Bandwidth	2.5 MHz	5.0 MHz	20 MHz
Low Input Noise Voltage	20 $nV/\sqrt{Hz}$	12 $nV/\sqrt{Hz}$	12 $nV/\sqrt{Hz}$

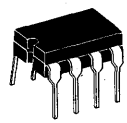
H SUFFIX
METAL PACKAGE
CASE 601

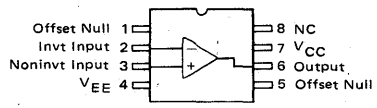


N SUFFIX
PLASTIC PACKAGE
CASE 626



J-8 SUFFIX
CERAMIC PACKAGE
CASE 693





APPLICATIONS

The LF series is suggested for all general purpose FET input amplifier requirements where precision and frequency response flexibility are of prime importance.

Specific applications include:

- Sample and Hold Circuits
- High Impedance Buffer
- Fast D/A and A/D Converters
- Precision High Speed
- Integrators

*NOTE: The LF 157 series is designed for wider bandwidth applications. The series is decompensated (AV min = 5).

This is advance information and specifications are subject to change without notice.

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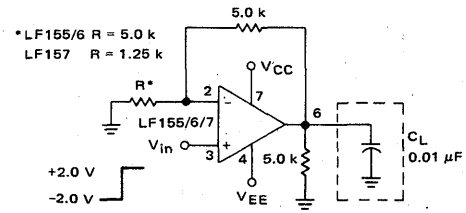
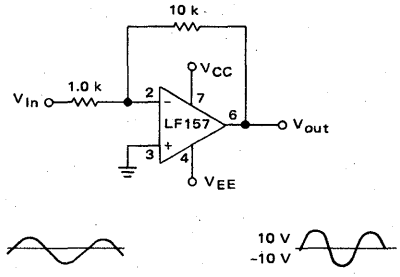
TYPICAL CIRCUIT CONNECTIONS

FIGURE 1 – DRIVING CAPACITIVE LOADS



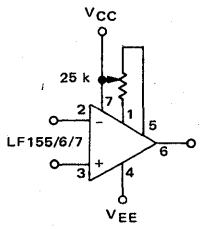
Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability.
$C_{L(max)} \cong 0.01\ \mu F$.
Overshoot ≤ 20%
Settling time (t_s) ≅ 5.0 μs

FIGURE 2 – LARGE POWER BANDWIDTH AMPLIFIER



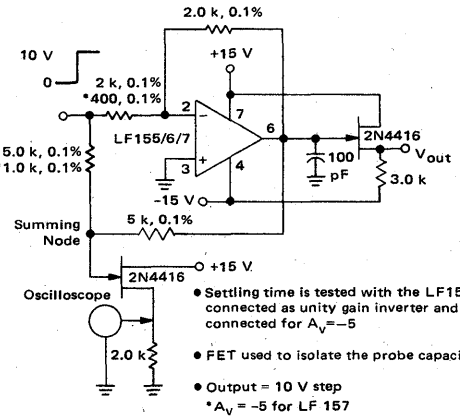
For distortion < 1% and a 20 Vp-p V_{Out} swing, power bandwidth is: 500 kHz.

FIGURE 3 – INPUT OFFSET VOLTAGE ADJUSTMENT



- V_{IO} is adjusted with a 25 k potentiometer
- The potentiometer wiper is connected to V_{CC}
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 μV/°C/mV of adjustment.
- Typical overall drift: 5.0 μV/°C ±(0.5 μV/°C/mV of adjustment.)

FIGURE 4 – SETTLING TIME TEST CIRCUIT



- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for A_V=−5
- FET used to isolate the probe capacitance
- Output = 10 V step

*A_V = −5 for LF 157

MAXIMUM RATINGS

Rating	Symbol	LF155A, 156A, 157A	LF355A, 356A, 357A	LF155, LF156, LF157	LF355, LF356, LF357	Unit
Supply Voltage	V_{CC} V_{EE}	+22 -22	+22 -22	+22 -22	+18 -18	V
Differential Input Voltage	V_{ID}	±40	±40	±40	±30	V
Input Voltage Range (1)	V_{IDR}	±20	±20	±20	±16	V
Output Short-Circuit Duration	I_{SC}	Continuous				
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	-55 to +125	0 to +70	°C
Operating Junction Temperature	T_J	150	100	150	100	°C
Storage Temperature Range	T_{stg}	-65 to +150				°C

Note 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 15 to 20 V, V_{EE} = −15 to −20 V, T_A = T_{low} to T_{high} (note 2) unless otherwise noted.)

Characteristic	Symbol	LF155/6/7			LF355/6/7*			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}							mV
(R_S = 50 Ω, V_{CM} = 0)		–	–	7.0	–	–	13	
(T_A = 25°C)		–	3.0	5.0	–	3.0	10	
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$							μV/°C
(R_S = 50 Ω)		–	5.0	–	–	5.0	–	
Change in Average TC with V_{IO} Adjust	$\Delta TC/\Delta V_{IO}$							μV/°C
(R_S = 50 Ω) (3)		–	0.5	–	–	0.5	–	per mV
Input Offset Current	I_{IO}							
(T_J = 25°C) (2)		–	3.0	20	–	3.0	50	pA
($T_J \leq T_{high}$, V_{CM} = 0)		–	–	20	–	–	2.0	nA
Input Bias Current	I_{IB}							
(T_J = 25°C) (2)		–	30	100	–	30	200	pA
($T_J \leq T_{high}$, V_{CM} = 0)		–	–	50	–	–	8.0	nA
Input Resistance	r_i							Ω
(T_J = 25°C)		–	10^{12}	–	–	10^{12}	–	
Large Signal Voltage Gain	A_{VOL}							V/mV
(V_{CC} = ±15 V)		25	–	–	15	–	–	
(V_O = ±10 V, R_L = 2.0 k, T_A = 25°C)		50	200	–	25	200	–	
Output Voltage Swing	V_O							V
(V_{CC} = ±15 V, R_L = 10 kΩ)		±12	±13	–	±12	±13	–	
Input Common-Mode Voltage Range	V_{ICR}	±11	+15.1	–	±10	+15.1	–	V
(V_{CC} = ±15 V)			−12.0			−12.0		
Common-Mode Rjection Ratio	CMRR	85	100	–	80	100	–	dB
Supply Voltage Rejection Ratio	PSRR	85	100	–	80	100	–	dB
Supply Current	I_D							mA
LF155/355		–	2.0	4.0	–	2.0	4.0	
LF156/157		–	5.0	7.0	–	–	–	
LF356/357		–	–	–	–	5.0	10	

*V_{CC} = ±15 V

AC ELECTRICAL CHARACTERISTICS (V_{CC} = ±15 V; T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	LF155/355			LF156/356			LF157/357			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Slew Rate	SR	–	5.0	–	7.5*	12	–	30*	50	–	V/μs
(A_V = 1) LF155,6											
(A_V = 5) LF157											
Gain-Bandwidth Product	BWp	–	2.5	–	–	5.0	–	–	20	–	MHz
Settling Time to 0.01% (4)	t_s	–	4.0	–	–	1.5	–	–	20	–	μs
Equivalent Input Noise Voltage	e_n										nV/√Hz
(R_S = 100 Ω, f = 100 Hz)		–	25	–	–	15	–	–	15	–	
(R_S = 100 Ω, f = 1000 Hz)		–	20	–	–	12	–	–	12	–	
Equivalent Input Noise Current	i_n										pA/√Hz
(f = 100 Hz)		–	0.01	–	–	0.01	–	–	0.01	–	
(f = 1000 Hz)		–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_i	–	3.0	–	–	3.0	–	–	3.0	–	pF

*These minimum limits apply for the LF156 and LF157 only.

NOTE:

(1) Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

(2) T_{low} = −55°C for LF155/155A/156/156A/157/157A
= 0°C for LF355/355A/356/356A/357/357A
T_{high} = +125°C for LF155/155A/156/156A/157/157A
= +70°C for LF355/355A/356/356A/357/357A

(3) The temperature coefficient of the adjusted input offset voltage changes only a small amount (0.5 μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

(4) Settling time is defined here, for a unity gain inverter connection using 2.0 k resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10 V step input is applied to the inverter. For the LF157, A_V = −5.0, the feedback resistor from output to input is 2.0 k and the output step is 10 V (see settling time test circuit).

3

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 15 to 20 V, V_{EE} = -15 to -20 V, T_A = T_{low} to T_{high} (note 2) unless otherwise noted.)

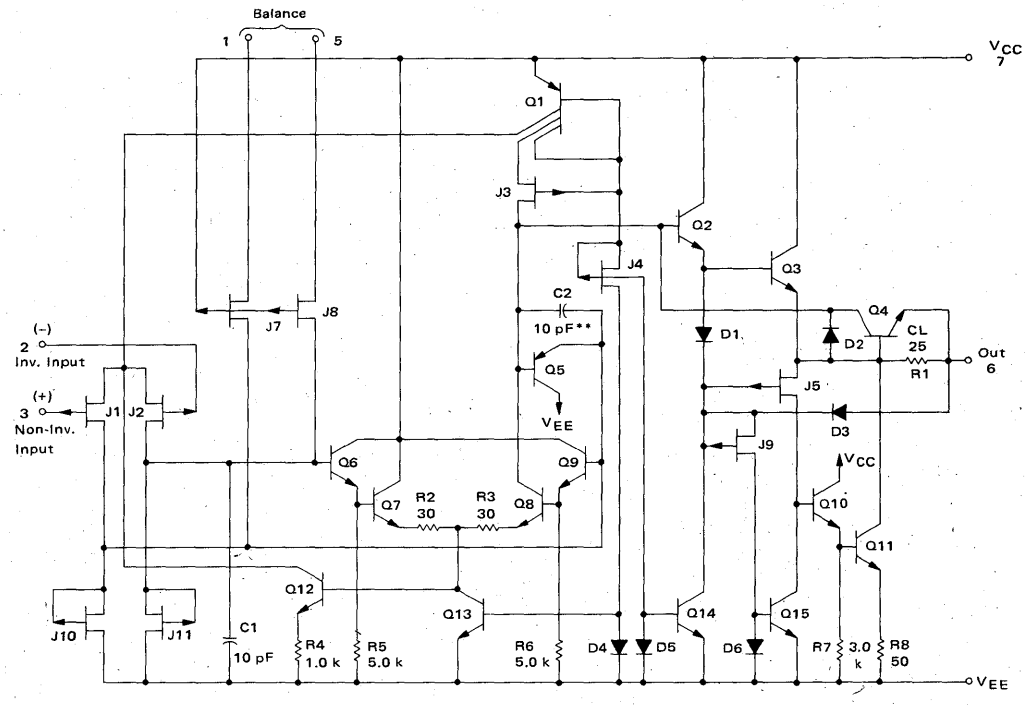
Characteristic	Symbol	LF155A/6A/7A			LF355A/6A/7A			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}							mV
(R_S = 50 Ω, V_{CM} = 0)		–	–	2.5	–	–	2.3	
(T_A = 25°C)		–	1.0	2.0	–	1.0	2.0	
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$							µV/°C
(R_S = 50 Ω)		–	3.0	5.0	–	3.0	5.0	
Change in Average TC with V_{IO} Adjust	$\Delta TC/\Delta V_{IO}$							µV/°C
(R_S = 50 Ω) (3)		–	0.5	–	–	0.5	–	per mV
Input Offset Current	I_{IO}							
(T_J = 25°C) (2)		–	3.0	10	–	3.0	10	pA
($T_J \leq T_{high}$, V_{CM} = 0)		–	–	10	–	–	1.0	nA
Input Bias Current	I_{IB}							
(T_J = 25°C) (2)		–	30	50	–	30	50	pA
($T_J \leq T_{high}$, V_{CM} = 0)		–	–	25	–	–	5.0	nA
Input Resistance	r_i							Ω
(T_J = 25°C)		–	10^{12}	–	–	10^{12}	–	
Large Signal Voltage Gain	A_{VOL}							V/mV
(V_{CC} = ±15 V)		25	–	–	25	–	–	
(V_O = ±10 V, R_L = 2.0 k, T_A = 25°C)		50	200	–	50	200	–	
Output Voltage Swing	V_O							V
(V_{CC} = ±15 V, R_L = 10 kΩ)		±12	±13	–	±12	±13	–	
Input Common-Mode Voltage Range	V_{ICR}		+15.1			+15.1		V
(V_{CC} = ±15 V)		±11	-12.0	–	±11	-12.0	–	
Common-Mode Rejection Ratio	CMRR	85	100	–	85	100	–	dB
Supply Voltage Rejection Ratio	PSRR	85	100	–	85	100	–	dB
Supply Current	I_D							mA
LF155A/355A		–	2.0	4.0	–	2.0	4.0	
LF156A/7A/356A/7A		–	5.0	7.0	–	5.0	7.0	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = ±15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	LF155A/355A			LF156A/356A			LF157A/357A			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Slew Rate	SR	3.0	5.0	–	10	12	–	40	50	–	V/µs
(A_V = 1) LF155A/6A											
(A_V = 5) LF157A											
Gain-Bandwidth Product	BWp	–	2.5	–	4.0	4.5	–	15	20	–	MHz
Settling Time to 0.01% (4)	t_s	–	4.0	–	–	1.5	–	–	1.5	–	µs
Equivalent Input Noise Voltage	e_n										nV/√Hz
(R_S = 100 Ω)											
(f = 100 Hz)		–	25	–	–	15	–	–	15	–	
(f = 1000 Hz)		–	20	–	–	12	–	–	12	–	
Equivalent Input Noise Current	i_n										pA/√Hz
(f = 100 Hz)		–	0.01	–	–	0.01	–	–	0.01	–	
(f = 1000 Hz)		–	0.01	–	–	0.01	–	–	0.01	–	
Input Capacitance	C_i	–	3.0	–	–	3.0	–	–	3.0	–	pF

For Notes 1, 2, 3, 4, see previous page.

CIRCUIT SCHEMATIC



**C = 2.0 pF on LF157.

ORDERING INFORMATION

Device	Temperature Range	Package	Device	Temperature Range	Package
LF155H, LF155AH	-55 to +125°C	Metal Can	LF356N, LF356AN	0 to +70°C	Plastic DIP
LF155J-8, LF155AJ-8	-55 to +125°C	Ceramic DIP	LF356J-8, LF356AJ-8	0 to +70°C	Ceramic DIP
LF355H, LF355AH	0 to +70°C	Metal Can	LF157H, LF157AH	-55 to +125°C	Metal Can
LF355N, LF355AN	0 to +70°C	Plastic DIP	LF157J-8, LF157AJ-8	-55 to +125°C	Ceramic DIP
LF355J-8, LF355AJ-8	0 to +70°C	Ceramic DIP	LF357H, LF357AH	0 to +70°C	Metal Can
LF156H, LF156AH	-55 to +125°C	Metal Can	LF357N, LF357AN	0 to +70°C	Plastic DIP
LF156J-8, LF156AJ-8	-55 to +125°C	Ceramic DIP	LF357J-8, LF357AJ-8	0 to +70°C	Ceramic DIP
LF356H, LF356AH	0 to +70°C	Metal Can			

ORDERING INFORMATION

Device	Temperature Range	Package
MC1420G	0°C to +70°C	Metal Can
MC1520F	−55°C to +125°C	Ceramic Flat
MC1520G	−55°C to +125°C	Metal Can

MC1420
MC1520

3

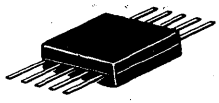
DIFFERENTIAL OUTPUT OPERATIONAL AMPLIFIER

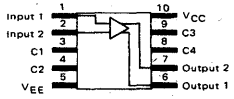
A wide-band, general-purpose operational amplifier which features both differential inputs and outputs. Open loop gain is approximately 3000 V/V but may be adjusted with external feedback components. This device is particularly useful in applications which require differential outputs.

- Differential Input and Differential Output
- Wide Closed-Loop Bandwidth; 10 MHz
- Differential Gain; 70 dB
- High Input Impedance; 2.0 Megohms:
- Low Output Impedance; 50 ohms

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT



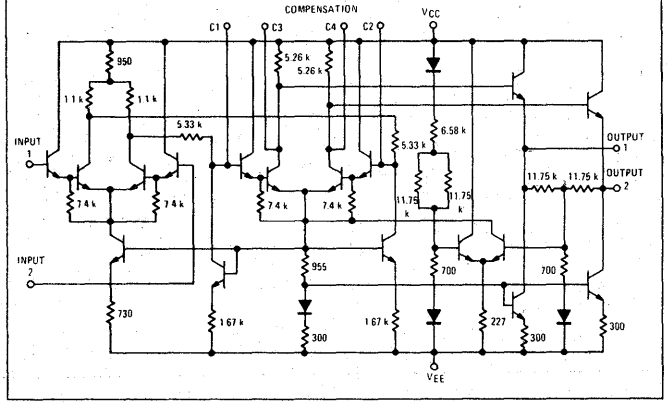


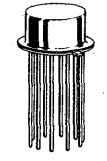
F SUFFIX
CERAMIC PACKAGE
CASE 606
(TO-91)

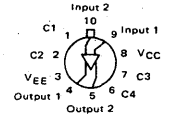
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC} V_{EE}	+8.0 -8.0	Vdc
Differential Input Signal		V_{in}	±8.0	Vdc
Load Current		I_{L1}, I_{L2}	15	mA
Power Dissipation (Package Limitation) Metal Package Derate above T_A = +25°C Flat Package Derate above T_A = +25°C		P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range	MC1520 MC1420	T_A	-55 to +125 0 to + 75	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

FIGURE 1 – CIRCUIT SCHEMATIC







G SUFFIX
METAL PACKAGE
CASE 603

SINGLE-ENDED ELECTRICAL CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1520 Min	MC1520 Typ	MC1520 Max	MC1420 Min	MC1420 Typ	MC1420 Max	Unit
Open Loop Voltage Gain	A_{vol}	1000	1500	–	750	1500	–	V/V
(T_{low} ② ≦ T_A ≦ T_{high} ②)		60	64	–	–	64	–	dB
Output Impedance (f = 20 Hz)	z_{os}	–	50	100	–	50	–	ohms
Input Impedance (f = 20 Hz)	z_{is}	0.5	2.0	–	–	2.0	–	megohms
Output Voltage Swing (R_L = 7.0 kΩ [Figure 8])	V_O	±3.5	±4.0	–	±3.0	±4.0	–	V_{peak}
Input Common-Mode Voltage Swing	V_{ICR}	±2.0	±3.0	–	–	±3.0	–	V_{peak}
Common-Mode Rejection Ratio	CMRR	75	90	–	60	90	–	dB
Input Bias Current $\left(\left[I_{IB} = \frac{I_1 + I_2}{2}\right], T_A = +25°C\right)$	I_{IB}	–	0.8	2.0	–	2.0	4.0	μA
Input Offset Current	$\lvert I_{IO}\rvert$							nA
($I_{IO} = I_1 - I_2$)		–	30	100	–	30	200	
($I_{IO} = I_1 - I_2$, $T_A = T_{low}$)		–	–	200	–	–	–	
($I_{IO} = I_1 - I_2$, $T_A = T_{high}$)		–	–	200	–	–	–	
Input Offset Voltage (T_A = +25°C)	$\lvert V_{IO}\rvert$	–	5.0	10	–	5.0	15	mV
Step Response								
Gain = 1.0, 10% Overshoot	t_{THL}	–	80	–	–	80	–	ns
R_1 = 10 kΩ	t_{PLH},t_{PHL}	–	70	–	–	70	–	ns
R_2 = 10 kΩ	dV_{out}/dt ①	–	5.0	–	–	5.0	–	V/μs
R_3 = 5.0 kΩ								
C_s = 39 pF								
Gain = 10, 10% Overshoot	t_{THL}	–	80	–	–	80	–	ns
R_1 = 10 kΩ	t_{PLH},t_{PHL}	–	70	–	–	70	–	ns
R_2 = 100 kΩ	dV_{out}/dt ①	–	15	–	–	15	–	V/μs
R_3 = 10 kΩ								
C_s = 10 pF								
Gain = 100, No Overshoot	t_{THL}	–	80	–	–	80	–	ns
R_1 = 1.0 kΩ	t_{PLH},t_{PHL}	–	70	–	–	70	–	ns
R_2 = 100 kΩ	dV_{out}/dt ①	–	30	–	–	30	–	V/μs
R_3 = 1.0 kΩ								
C_s = 1.0 pF								
Open Loop, No Overshoot	t_{THL}	–	180	–	–	180	–	ns
R_1 = 50 Ω	t_{PLH},t_{PHL}	–	70	–	–	70	–	ns
R_2 = ∞	dV_{out}/dt ①	–	35	–	–	35	–	V/μs
R_3 = 50 Ω								
C_s = 0								
Bandwidth:	–							MHz
(Open Loop [Figure 4])		–	2.0	–	–	2.0	–	
(Closed Loop [Unity Gain]) (Figure 5)		–	10	–	–	10	–	
Input Noise Voltage (Open Loop) (5.0 Hz - 5.0 MHz)	$V_{n(in)}$	–	11	15	–	11	–	μV(rms)
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = T_{low} to T_{high})	$\Delta V_{IO}/\Delta T$	–	2.0	–	–	2.0	–	μV/°C
DC Power Dissipation (V_O = 0)	P_D	–	120	240	–	120	240	mW
Power Supply Sensitivity (V_O = 0)	$S^{\pm}$	–	250	450	–	250	–	μV/V

① dV_{out}/dt = Slew Rate

② T_{low} = 0°C for MC1420, -55°C for MC1520 T_{high} = +75°C for MC1420, +125°C for MC1520

DIFFERENTIAL ELECTRICAL CHARACTERISTICS

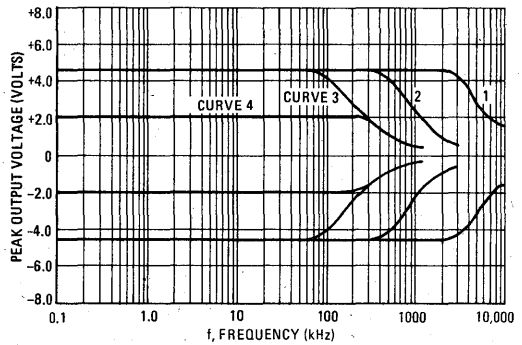
(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C, unless otherwise noted.)

Characteristic	Symbol	MC1520 Min	MC1520 Typ	MC1520 Max	MC1420 Min	MC1420 Typ	MC1420 Max	Unit
Gain (Open Loop)	A_{vol}	2000 66	3000 70	– –	1500 64	3000 70	– –	V/V dB
Input Impedance (f = 20 Hz)	z_{id}	0.5	2.0	–	–	2.0	–	megohms
Output Impedance (f = 20 Hz)	z_{od}	–	100	200	–	100	–	ohms
Common-Mode Output Voltage	$V_{O(CM)}$	-0.5	0	+0.5	–	0	–	Vdc
Output Voltage Swing (R_L = 7.0 kΩ)	V_O	±7.0	±8.0	–	±6.0	±8.0	–	V_{peak}

TYPICAL CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 2 – LARGE SIGNAL SWING versus FREQUENCY



TEST CIRCUIT

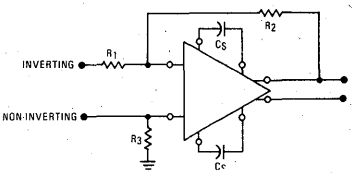


FIGURE NO.	CURVE NO.	MODE	VOLTAGE GAIN	TEST CONDITIONS R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_S (pF)	NOISE OUTPUT mV (rms)
3	1	INVERTING	100	1.0 k	100 k	1.0 k	1.0	2.0
	2	INVERTING	10	10 k	100 k	10 k	10	0.55
	3	INVERTING	1.0	10 k	10 k	5.0 k	39	0.17
	4	NON-INVERTING	1.0	∞	10 k	10 k	39	0.17
4	1	NON-INVERTING	A_{vol}	0	∞	50	1.0	1.0
	2	NON-INVERTING	A_{vol}	0	∞	50	10	2.0
	3	NON-INVERTING	A_{vol}	0	∞	50	39	5.2
5	1	NON-INVERTING	100	100	10 k	100	1.0	2.0
	2	NON-INVERTING	10	1.0 k	9.1 k	910	10	0.55
	3	NON-INVERTING	1.0	∞	10 k	10 k	39	0.17

FIGURE 3 – OPEN LOOP VOLTAGE GAIN

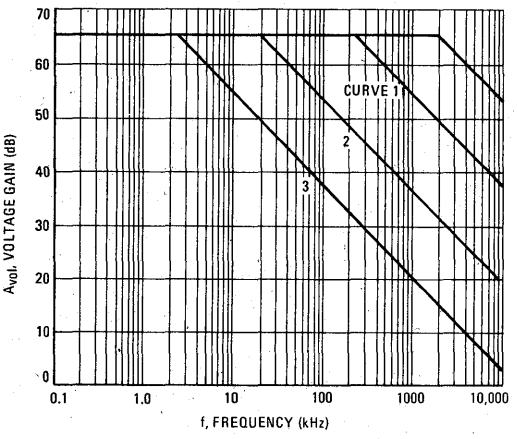
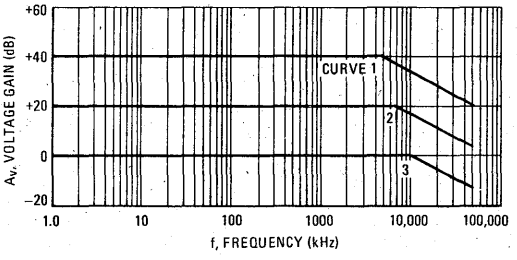


FIGURE 4 – CLOSED LOOP VOLTAGE GAIN versus FREQUENCY



TYPICAL OUTPUT CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 5 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

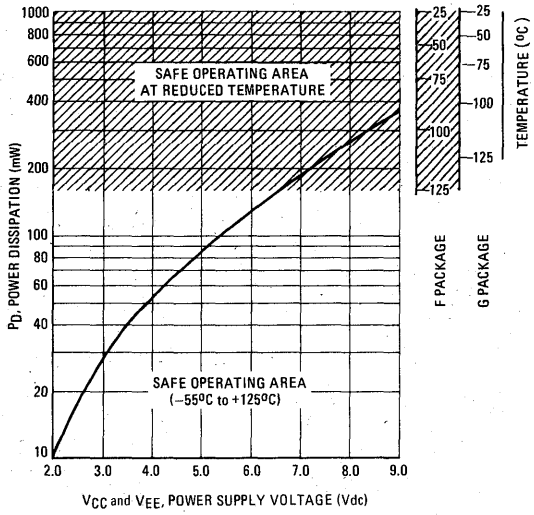


FIGURE 6 – OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

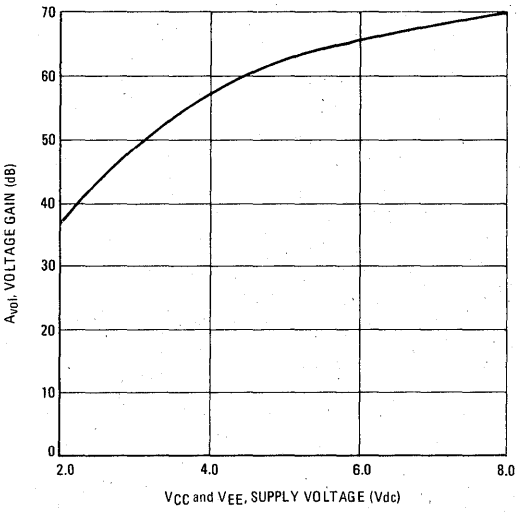


FIGURE 7 – SINGLE ENDED OUTPUT VOLTAGE versus LOAD RESISTANCE

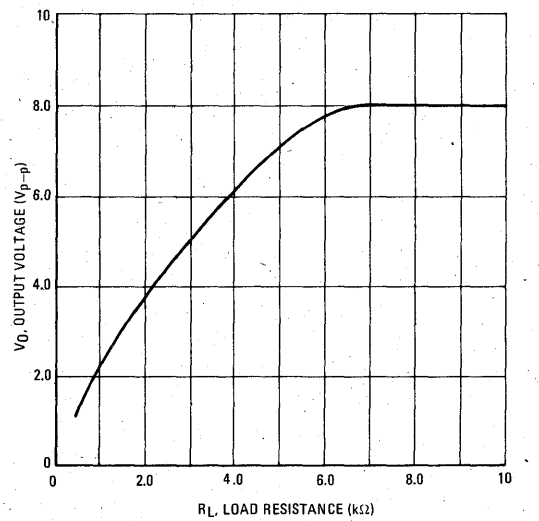
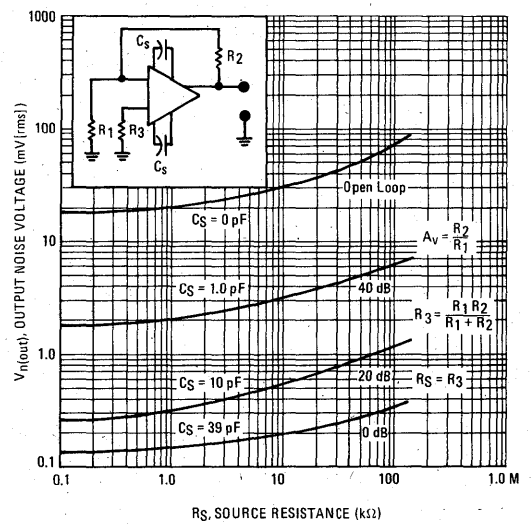


FIGURE 8 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE



ORDERING INFORMATION

Device	Temperature Range	Package
MC1430F,1431F	0°C to +70°C	Ceramic Flat
MC1430G,1431G	0°C to +70°C	Metal Can
MC1430P,1431P	0°C to +70°C	Plastic DIP
MC1530F,1531F	−55°C to +125°C	Ceramic Flat
MC1530G,1531G	−55°C to +125°C	Metal Can

MC1430, MC1431
MC1530, MC1531

OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

The MC1531 (MC1431) is provided with Darlington inputs to increase input impedance; otherwise the MC1531 (MC1431) circuit is identical with the MC1530 (MC1430) circuit.

- High Open Loop Voltage Gain — 4500 min (MC1530)
  — 2500 min (MC1531)
- High Input Impedance — 10 Kilohms min (MC1530)
  — 1.0 Megohm min (MC1531)
- Low Output Impedance — 50 Ohms max
- High Slew Rate — 6.0 V/μs typ @ A_{VS} = 10
- High Open Loop Bandwidth — 2.0 MHz typ (MC1530)
  0.4 MHz typ (MC1531)

OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

MAXIMUM RATINGS (T_A = 25°C unless otherwsie noted)

Rating	Symbol	Value	Unit
Power Supply Voltage MC1530, MC1531 MC1430, MC1431	V_{CC}, V_{EE} V_{CC}, V_{EE}	+9.0, −9.0 +8.0, −8.0	Vdc
Differential Input Voltage Range	V_{IDR}	± 5.0	Volts
Load Current	I_L	10	mA
Power Dissipation (Package Limitation) Metal Package Derate above T_A = +25°C Flat Package Derate above T_A = +25°C Dual In-Line Plastic Package MC1430, MC1431 Derate above +25°C	P_D	 680 4.6 500 3.3 400 3.3	 mW mW/°C mW mW/°C mW mW/°C
Operating Ambient Temperature Range MC1530, MC1531 MC1430, MC1431	T_A	 −55 to +125 0 to +75	°C
Storage Temperature Range Metal and Ceramic Package Plastic Package MC1430, MC1431	T_{stg}	 −65 to +175 −55 to +150	°C

CIRCUIT SCHEMATICS

FIGURE 1 — MC1530/MC1430 (STANDARD INPUT)

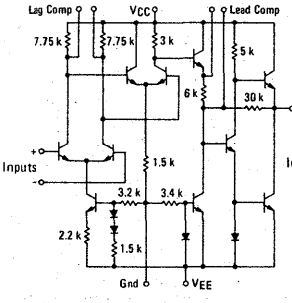
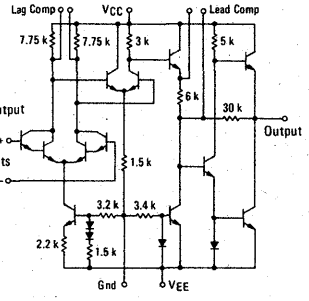
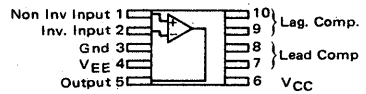


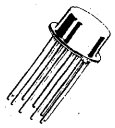
FIGURE 2 — MC1531/MC1431 (DARLINGTON INPUT)



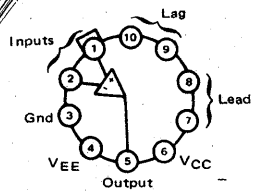
PIN CONNECTIONS

F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

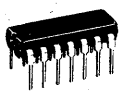


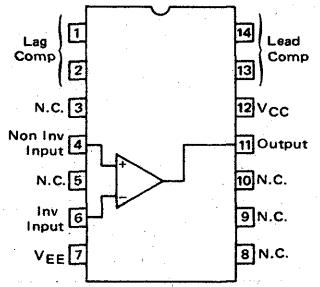


G SUFFIX
METAL PACKAGE
CASE 603 B



P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1430P/MC1431P only)



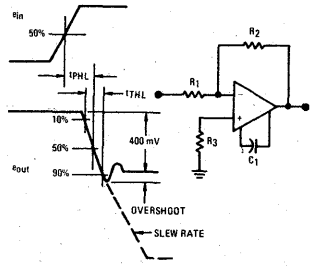


ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted)

Characteristic		Symbol	MC1530 Min	MC1530 Typ	MC1530 Max	MC1430 Min	MC1430 Typ	MC1430 Max	Unit
Input Bias Current		I_{IB}	–	3.0	10	–	5.0	15	μAdc
Input Offset Current		I_{IO}	–	0.2	2.0	–	0.4	4.0	μAdc
Input Offset Voltage	T_A = +25°C	V_{IO}	–	1.0	5.0	–	2.0	10	mVdc
	$T_A = T_{low}$ (1)		–	–	6.0	–	–	11	
	$T_A = T_{high}$ (1)		–	–	6.0	–	–	12	
Single-Ended Input Impedance (Open-Loop, f = 30 Hz)		z_{is}	10	20	–	5.0	15	–	k Ω
Common-Mode Input Voltage Swing		V_{ICR}	± 2.0	± 2.7	–	± 2.0	± 2.5	–	V_{pk}
Equivalent Input Noise Voltage (Open-Loop, R_s = 50 ohms, BW = 5.0 MHz)		e_N	–	10	–	–	10	–	μV(rms)
Common-Mode Rejection Ratio (f = 100 Hz)		CMRR	70	75	–	65	75	–	dB
Open-Loop Voltage Gain,	T_A = +25°C	A_{vol}	–	–	–	3000	5000	–	V/V
	$T_A = T_{low}$ to T_{high}		4500	5000	12,500	–	–	–	
Bandwidth (Open-Loop, -3.0 dB, no roll-off capacitance)		BW	1.0	2.0	–	1.0	2.0	–	MHz
Output Impedance (f = 100 Hz)		z_o	–	25	50	–	25	50	ohms
Output Voltage Swing (R_L = 1.0 k ohms)		V_O	± 4.5	± 5.2	–	± 4.0	± 5.0	–	V_{pk}
Power Supply Sensitivity ($R_s \leq$ 10 k Ω)		PSRR	–	100	–	–	100	–	μV/V
Power Supply Current		I_{CC}, I_{EE}	–	9.2	12.5	–	9.2	12.5	mAdc
DC Quiescent Power Consumption (V_O = 0)		P_C	–	110	150	–	110	150	mW

ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted)

Characteristic		Symbol	MC1531 Min	MC1531 Typ	MC1531 Max	MC1431 Min	MC1431 Typ	MC1431 Max	Unit
Input Bias Current		I_{IB}	–	0.025	0.150	–	0.1	0.3	μAdc
Input Offset Current		I_{IO}	–	0.003	0.025	–	0.01	0.1	μAdc
Input Offset Voltage	T_A = +25°C	V_{io}	–	3.0	10	–	5.0	15	mVdc
	$T_A = T_{low}$ (1)		–	–	18	–	–	–	
	$T_A = T_{high}$ (1)		–	–	16.5	–	–	–	
Single-Ended Input Impedance (Open-Loop, f = 30 Hz)		z_{is}	1000	2000	–	300	600	–	k Ω
Common-Mode Input Voltage Swing		V_{ICR}	± 2.0	± 2.4	–	± 2.0	± 2.2	–	V_{pk}
Equivalent Input Noise Voltage (Open-Loop, R_s = 50 ohms, BW = 5.0 MHz)		e_N	–	20	–	–	20	–	μV(rms)
Common-Mode Rejection Ratio (f = 100 Hz)		CMRR	65	65	–	60	75	–	dB
Open-Loop Voltage Gain	T_A = +25°C	A_{vol}	–	–	–	1500	3500	–	V/V
	$T_A = T_{low}$ to T_{high}		2500	3500	7000	–	–	–	
Bandwidth (Open-Loop, -3.0 dB, no roll-off capacitance)		BW	–	0.4	–	–	0.4	–	MHz
Output Impedance (f = 30 Hz)		z_o	–	25	50	–	25	50	ohms
Output Voltage Swing (R_L = 1.0 k ohms)		V_O	± 4.5	± 5.2	–	± 4.0	± 5.0	–	V_{pk}
Power Supply Sensitivity ($R_S \leq$ 10 k Ω)		PSRR	–	100	–	–	100	–	μV/V
Power Supply Current		I_{CC},I_{EE}	–	9.2	12.5	–	9.2	12.5	mAdc
DC Quiescent Power Consumption (V_O = 0)		P_C	–	110	150	–	110	150	mW



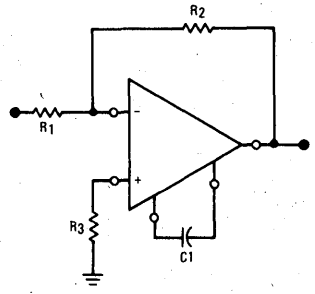
STEP RESPONSE, TYPICAL CHARACTERISTICS
(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, V_O = 400 mVdc, T_A = +25°C)

	Symbol	MC1530 MC1430	MC1531 MC1431	
Step Response				
Gain = 100, 0% overshoot,	t_{THL}	0.13	0.36	μs
R_1 = 1.0 k ohm, R_2 = 100 k ohms,	t_{PHL}	0.11	0.21	μs
R_3 = 1.0 k ohm, C_1 = 750 pF	SR	33	16	V/μs
Gain = 10, 10% overshoot,	t_{THL}	0.34	0.30	μs
R_1 = 10 k ohms, R_2 = 100 k ohms,	t_{PHL}	0.25	0.28	μs
R_3 = 10 k ohms, C_1 = 6800 pF	SR	6.0	5.5	V/μs
Gain = 1.0, 5.0% overshoot,	t_{THL}	0.28	0.37	μs
R_1 = 10 k ohms, R_2 = 10 k ohms,	t_{PHL}	0.16	0.17	μs
R_3 = 5.0 k ohms, C_1 = 33,000 pF	SR	1.7	1.4	V/μs

(1) T_{low}: 0°C for MC1430, -55°C for MC1530; T_{high}: +75°C for MC1430, +125°C for MC1530
T_{low}: 0°C for MC1431, -55°C for MC1531; T_{high}: +75°C for MC1431, +125°C MC1531

3

FIGURE 3 – TEST CIRCUIT



TYPICAL OUTPUT CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C)

FIG. NO.	CURVE NO.	VOLTAGE GAIN	DEVICE NO.	TEST CONDITIONS			
				R_1 (kΩ)	R_2 (kΩ)	R_3 (Ω)	C_1 (pF)
5	1,2	100	MC1530/MC1430, MC1531/MC1431	1.0	100	1.0 k	750
	3	10	MC1530/MC1430, MC1531/MC1431	10	100	10 k	6800
	4	1	MC1530/MC1430, MC1531/MC1431	10	10	5.0 k	33,000
6	1	100	MC1530/MC1430	1.0	100	1.0 k	750
	2	10	MC1530/MC1430	10	100	10 k	6800
	3	10	MC1530/MC1430	1.0	10	1.0 k	6800
	4	1	MC1530/MC1430	10	10	5.0 k	33,000
	5	1	MC1530/MC1430	1.0	1.0	500	33,000
7	1	100	MC1531/MC1431	1.0	100	1.0 k	750
	2	10	MC1531/MC1431	10	100	10 k	6800
	3	1	MC1531/MC1431	10	10	5.0 k	33,000
8	1	A_{VOL}	MC1530/MC1430	0	∞	0	0
	2	A_{VOL}	MC1530/MC1430	0	∞	0	750
	3	A_{VOL}	MC1530/MC1430	0	∞	0	6800
	4	A_{VOL}	MC1530/MC1430	0	∞	0	33,000
9	1	A_{VOL}	MC1531/MC1431	0	∞	0	0
	2	A_{VOL}	MC1531/MC1431	0	∞	0	750
	3	A_{VOL}	MC1531/MC1431	0	∞	0	6800
	4	A_{VOL}	MC1531/MC1431	0	∞	0	33,000

FIGURE 4 – LARGE SIGNAL SWING versus FREQUENCY

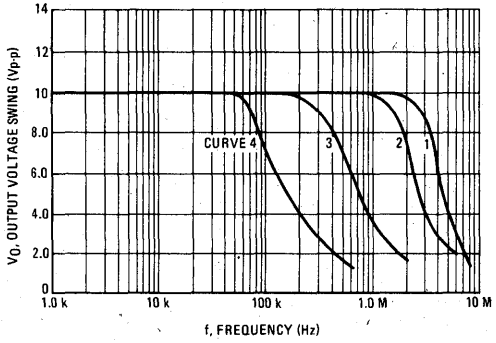


FIGURE 5 – MC1530/MC1430 VOLTAGE GAIN versus FREQUENCY

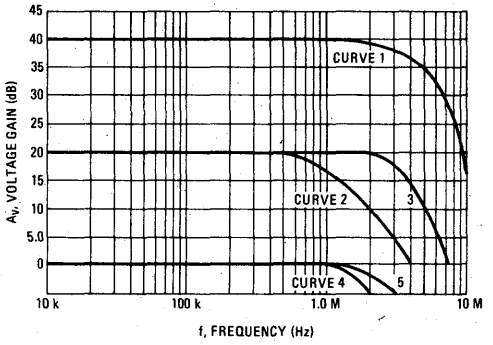


FIGURE 6 – MC1531/MC1431 VOLTAGE GAIN versus FREQUENCY

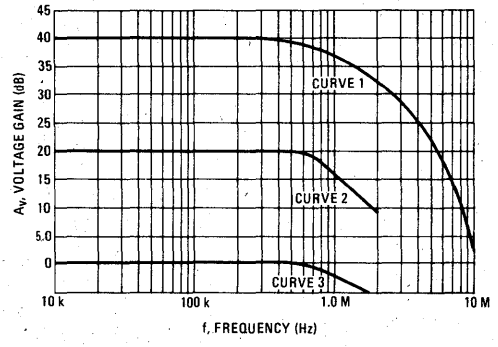


FIGURE 7 – MC1530/MC1430 OPEN LOOP VOLTAGE GAIN versus FREQUENCY

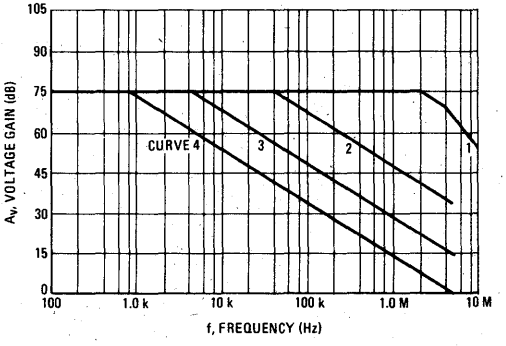


FIGURE 8 – MC1531/MC1431 OPEN LOOP VOLTAGE GAIN versus FREQUENCY

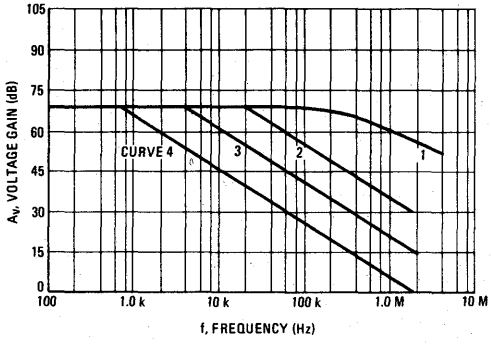


FIGURE 9 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

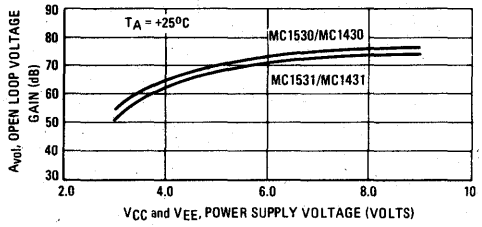


FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

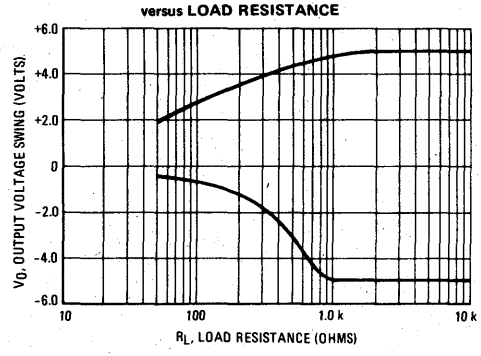


FIGURE 11 – COMMON-MODE SWING versus POWER SUPPLY VOLTAGE

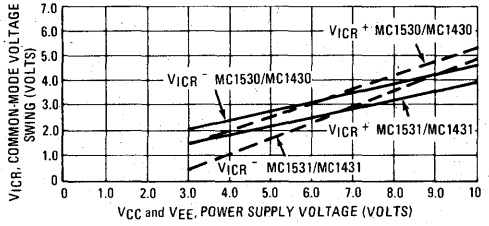
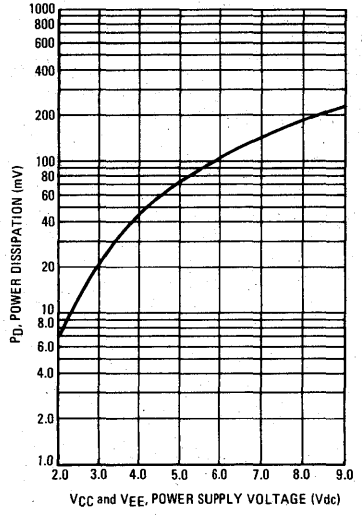


FIGURE 12 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGE



ORDERING INFORMATION

Device	Temperature Range	Package
MC1433F	0°C to +70°C	Ceramic Flat
MC1433G	0°C to +70°C	Metal Can
MC1433L	0°C to +70°C	Ceramic DIP
MC1433P	0°C to +70°C	Plastic DIP
MC1533F	−55°C to +125°C	Ceramic Flat
MC1533G	−55°C to +125°C	Metal Can
MC1533L	−55°C to +125°C	Ceramic DIP

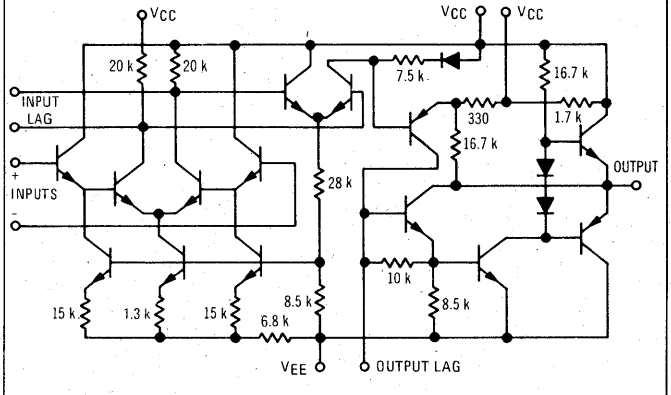
MC1433
MC1533

3

OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

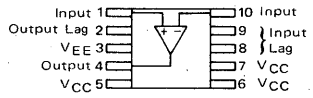
- High-Performance Open Loop Gain Characteristics
  A_{Vol} = 60,000 typical
- Low Temperature Drift – ±5 μV/°C
- Large Output Voltage Swing –
  ±13 V typical @ ±15 V Supply
- Low Output Impedance – z_o = 100 ohms typical



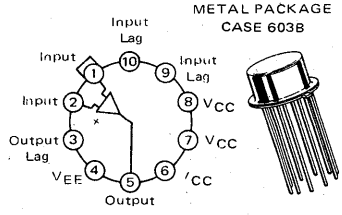
OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

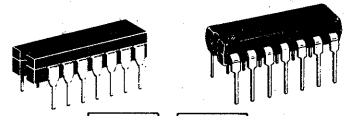


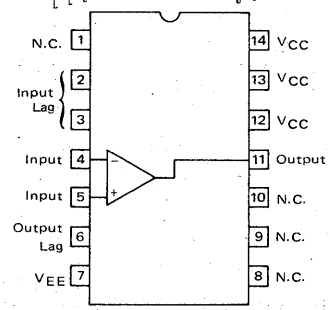
G SUFFIX
METAL PACKAGE
CASE 603B



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1433P Only)





ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} -15 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Symbol	MC1533 Min	MC1533 Typ	MC1533 Max	MC1433 Min	MC1433 Typ	MC1433 Max	Unit
Open Loop Voltage Gain	A_{VOL}							—
(T_A = +25°C)		40,000	60,000	—	30,000	60,000	—	
(T_A = T_{low} ① to T_{high} ①)		35,000	50,000	—	20,000	50,000	—	
Output Impedance	z_o							Ω
(f = 20 Hz)		—	100	150	—	100	150	
Input Impedance	z_i							kΩ
(f = 20 Hz)		500	1000	—	300	600	—	
Output Voltage Range	V_o							V_{peak}
(R_L = 10 kΩ)		±12	±13	—	±12	±13	—	
(R_L = 2 kΩ)		±11	±12	—	±10	±12	—	
Input Common Mode Voltage Range	V_{ICR}	+9.0	+10	—	+8.0	+9.0	—	V_{peak}
		-8.0	-9.0	—	-8.0	-9.0	—	
Common Mode Rejection Ratio	CMRR	90	100	—	80	100	—	dB
Input Bias Current	I_{IB}							μA
(T_A = +25°C)		—	0.5	1.0	—	0.5	2.0	
(T_A = T_{low})		—	—	3.0	—	—	4.0	
Input Offset Current	I_{IO}							μA
(T_A = +25°C)		—	0.03	0.15	—	0.1	0.50	
(T_A = T_{low})		—	—	0.5	—	—	0.75	
(T_A = T_{high})		—	—	0.2	—	—	0.75	
Input Offset Voltage ②	V_{IO}							mV
(T_A = +25°C)		—	1.0	5.0	—	1.0	7.5	
(T_A = T_{low}, T_{high})		—	—	6.0	—	—	10	
Step Response (C_2 = 10 pF)								
Gain = 100, 10% overshoot,	t_{TLH}	—	0.25	—	—	0.25	—	μs
R_1 = 10 kΩ, R_2 = 1.0 MΩ,	t_{pd}	—	0.1	—	—	0.1	—	μs
R_3 = 100 Ω, C_1 = 0.01 μF	SR	—	6.2	—	—	6.2	—	V/μs
Gain = 10, no overshoot,	t_{TLH}	—	0.3	—	—	0.3	—	μs
R_1 = 10 kΩ, R_2 = 100 kΩ,	t_{pd}	—	0.1	—	—	0.1	—	μs
R_3 = 10 Ω, C_1 = 0.1 μF	SR	—	2.9	—	—	2.9	—	V/μs
Gain = 1, 5% overshoot,	t_{TLH}	—	0.2	—	—	0.2	—	μs
R_1 = 10 kΩ, R_2 = 10 kΩ,	t_{pd}	—	0.1	—	—	0.1	—	μs
R_3 = 10 Ω, C_1 = 1.0 μF	SR	—	2.0	—	—	2.0	—	V/μs
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$							μV/°C
(T_A = T_{low} to +25°C)		—	8.0	—	—	10	—	
(T_A = +25°C to T_{high})		—	5.0	—	—	8.0	—	
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$							nA/°C
(T_A = T_{low} to T_{high})		—	0.1	—	—	0.1	—	
(T_A = +25°C to T_{high})		—	0.05	—	—	0.05	—	
DC Power Consumption	P_C							mW
(Power Supply = ±15 V, V_o = 0)		—	125	170	—	125	240	
Positive Supply Sensitivity	PSRR+							μV/V
(V_{EE} constant)		—	50	150	—	50	200	
Negative Supply Sensitivity	PSSR-							μV/V
(V_{CC} constant)		—	50	150	—	50	200	

① T_{high} = +75°C for MC1433, +125°C for MC1533 T_{low} = 0 for MC1433, -55°C for MC1533

② Input offset voltage (V_{IO}) may be adjusted to zero.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage MC1533,MC1433	V_{CC}	+20,+18	Vdc
MC1533,MC1433	V_{EE}	-20,-18	Vdc
Differential Input Voltage Range	V_{IDR}	±10	Volts
Common Mode Input Voltage Range	V_{ICR}	±V_{CC}	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_S	0.1	s
Power Dissipation (Package Limitation)	P_D		
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Flat Package		500	mW
Derate above T_A = +25°C		3.3	mW/°C
Dual In-Line Ceramic Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Dual In-Line Plastic Package		400	mW
Derate above T_A = +25°C		3.3	mW/°C
Operating Ambient Temperature Range	T_A		°C
MC1533		-55 to +125	
MC1433		0 to +75	
Storage Temperature Range	T_{stg}	-65 to +150	°C

TYPICAL CHARACTERISTICS

FIGURE 2 – TEST CIRCUIT

V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C

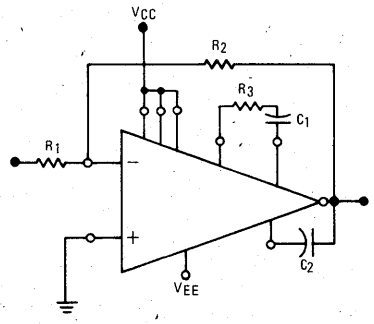


Fig. No.	Curve No.	Test Conditions				
		R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_1 (μF)	C_2 (pF)
3	1	10 k	10 k	10	1.0	10
	2	10 k	100 k	10	0.1	10
	3	10 k	1.0 M	100	0.01	10
	3	1.0 k	1.0 M	390	0.002	10
4	1	10 k	10 k	10	1.0	10
	2	10 k	100 k	10	0.1	10
	3	10 k	1.0 M	100	0.01	10
	4	1.0 k	1.0 M	390	0.002	10
5	1	0	∞	10	1.0	10
	2	0	∞	10	0.1	10
	3	0	∞	100	0.01	10
	4	0	∞	390	0.002	10

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} -15 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 3 – LARGE-SIGNAL RANGE versus FREQUENCY

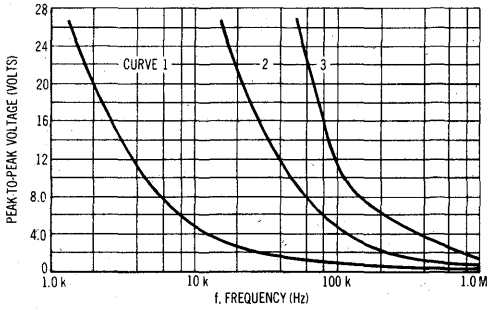


FIGURE 4 – VOLTAGE GAIN versus FREQUENCY

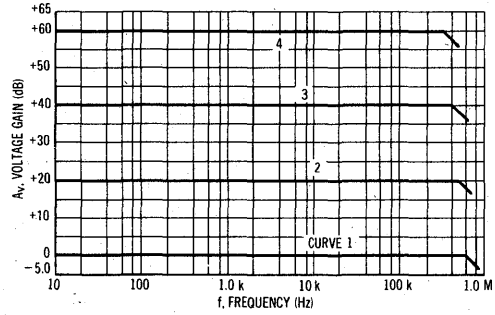


FIGURE 5 – OFFSET ADJUST CIRCUIT

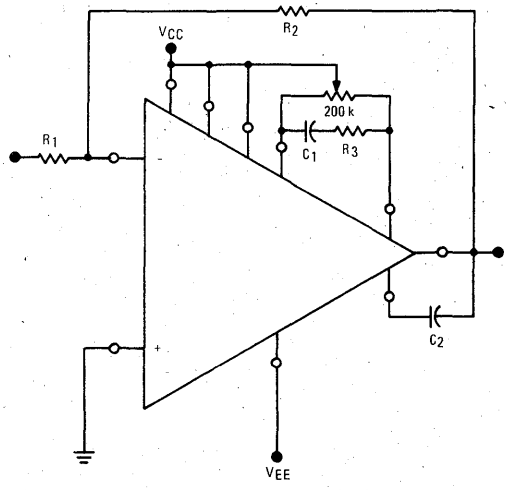
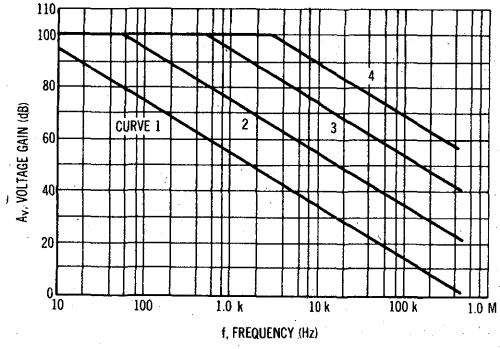


FIGURE 6 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY
(HIGH GAIN CONFIGURATION)



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TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGE

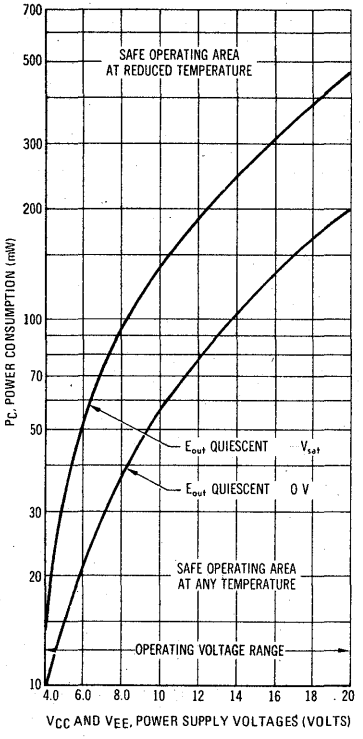


FIGURE 8 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

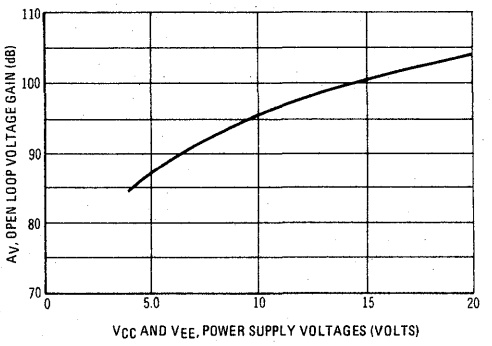


FIGURE 9 – COMMON MODE RANGE versus POWER SUPPLY VOLTAGE

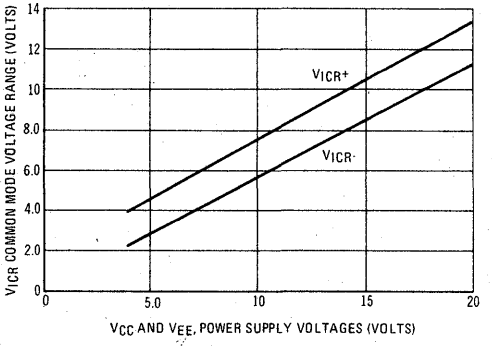
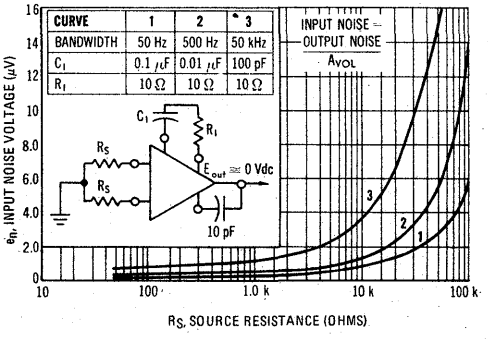


FIGURE 10 – INPUT NOISE VOLTAGE versus SOURCE RESISTANCE



ORDERING INFORMATION

Device	Temperature Range	Package
MC1435F	0°C to +70°C	Ceramic Flat
MC1435G	0°C to +70°C	Metal Can
MC1435L	0°C to +70°C	Ceramic DIP
MC1435P	0°C to +70°C	Plastic DIP
MC1535F	−55°C to +125°C	Ceramic Flat
MC1535G	−55°C to +125°C	Metal Can
MC1535L	−55°C to +125°C	Ceramic DIP

MC1435
MC1535

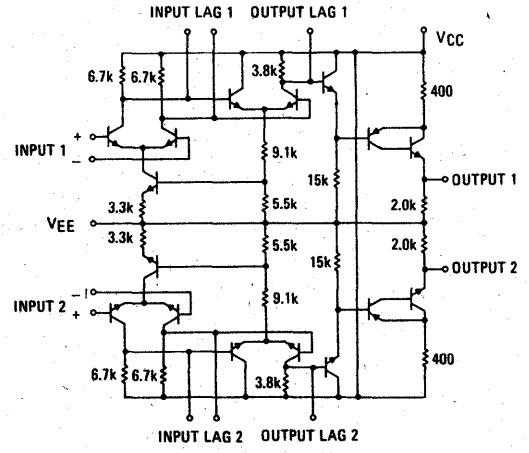
DUAL OPERATIONAL AMPLIFIERS

. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.

Typical Amplifier Features:

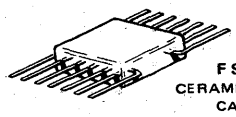
- High Open Loop Gain Characteristics — A_{VOL} = 7,000
- Low Temperature Drift — ±10 μV/°C
- Low Input Offset Voltage — 1.0mV
- Low Input Noise Voltage — 0.5μV

CIRCUIT SCHEMATIC

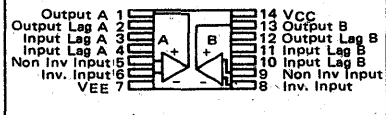


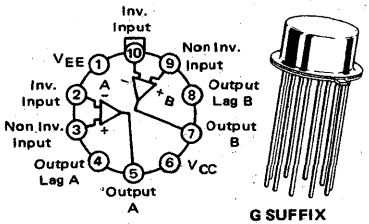
DUAL OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

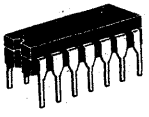


F SUFFIX
CERAMIC PACKAGE
CASE 607

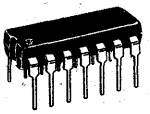




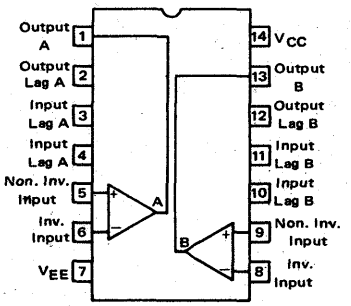
G SUFFIX
METAL PACKAGE
CASE 603B



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

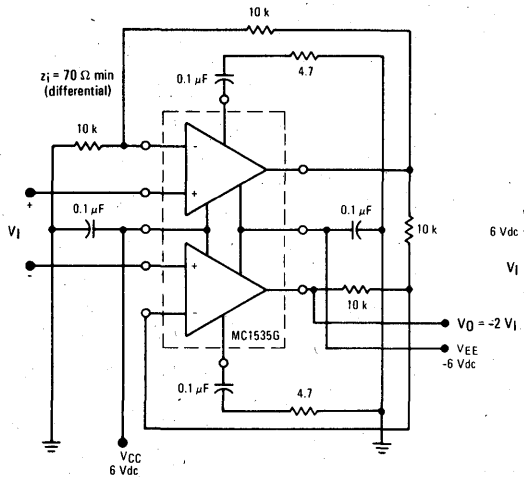


P SUFFIX
PLASTIC PACKAGE
CASE 646

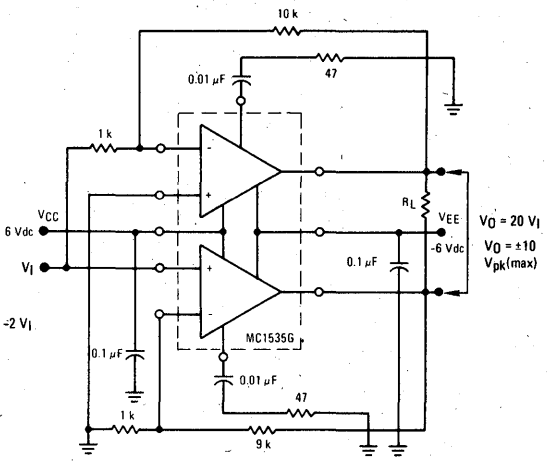


3

HIGH z_i, DIFFERENTIAL TO SINGLE-ENDED AMPLIFIER



LARGE OUTPUT SWING CONFIGURATION (FLOATING LOAD)



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MC1535	MC1435	Unit
Power Supply Voltage	V_{CC} V_{EE}	+10 -10	+9.0 -9.0	Vdc
Input Differential Voltage Range	V_{IDR}	±5.0	±5.0	Volts
Common-Mode Input Voltage Range	V_{ICR}	+5.0, -4.0	+5.0 -4.0	Volts
Load Current	I_L	20	20	mA
Output Short-Circuit Duration	t_S	Continuous		
Power Dissipation (Package Limitation) Flat Ceramic Package Derate above T_A = +25°C Metal Package Derate above T_A = +25°C Ceramic Dual In-Line Package Derate above T_A = +25°C	P_D	 500 3.3 680 4.6 625 5.0		 mW mW/°C mW mW/°C mW mW/°C
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Each Amplifier) (V_{CC} = +6.0 Vdc, V_{EE} = −6.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristics	Symbol	MC1535 Min	MC1535 Typ	MC1535 Max	MC1435 Min	MC1435 Typ	MC1435 Max	Unit
Input Bias Current $I_{IB} = \frac{I_1 + I_2}{2}$, T_A = +25°C T_A = T_{low} to T_{high} ①	I_{IB}	– –	1.2 –	3.0 6.0	– –	1.2 –	5.0 10	μAdc
Input Offset Current T_A = +25°C T_A = +25°C to T_{high} T_A = T_{low} to +25°C	I_{IO}	– – –	50 – –	300 300 900	– – –	50 – –	500 1500 1500	nAdc
Input Offset Voltage T_A = +25°C T_A = T_{low} to T_{high}	V_{IO}	– –	1.0 –	3.0 5.0	– –	1.0 –	5.0 7.5	mVdc
Differential Input Impedance (Open-Loop, f = 20 Hz) Parallel Input Resistance Parallel Input Capacitance	 r_i C_i	 10 –	 45 6.0	 – –	 10 –	 45 –	 – –	 k ohms pF
Common-Mode Input Impedance (f = 20 Hz)	z_i	–	250	–	–	250	–	Megohms
Common-Mode Input Voltage Swing See Figure 7.	V_{ICR}	+3.0 -2.0	+3.9 -2.7	– –	+3.0 -2.0	+3.9 -2.7	– –	V_{pk}
Equivalent Input Noise Voltage (A_v = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz)	e_n	–	45	–	–	45	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 100 Hz)	CMRR	-70	-90	–	-70	-90	–	dB
Open Loop Voltage Gain (T_A = T_{low} to T_{high})	A_{vol}	4,000	7,000	10,000	3,500	7,000	–	V/V
Power Bandwidth (See Figure 2, Curve 3A.) (A_V = 1, R_L = 2.0 kohms, THD ≤ 5%, V_O = 20 Vp-p)	BWp	–	40	–	–	40	–	kHz
Unity Gain Crossover Frequency (open-loop)	f_c	–	2.0	–	–	2.0	–	MHz
Phase Margin (open-loop, unity gain)	ϕm	–	75	–	–	75	–	degrees
Gain Margin	A_M	–	18	–	–	18	–	dB
Step Response Gain = 100, 30% overshoot, R1 = 4.7 kΩ, R2 = 470 kΩ, R3 = 150 Ω, C1 = 1,000 pF	 t_{PHL} t_P SR	 – – –	 0.3 0.1 0.167	 – – –	 – – –	 0.3 0.1 0.167	 – – –	 μs μs V/μs
Gain = 10, 10% overshoot, R1 = 47 kΩ, R2 = 470 kΩ, R3 = 47 Ω, C1 = 0.01 μF	t_{PHL} t_P SR	– – –	1.9 0.3 0.111	– – –	– – –	1.9 0.3 0.111	– – –	μs μs V/μs
Gain = 1, 5% overshoot, R1 = 47 kΩ, R2 = 47 kΩ, R3 = 4.7 Ω, C1 = 0.1 μF	t_{PHL} t_P SR	– – –	27 0.25 0.013	– – –	– – –	27 0.25 0.013	– – –	μs μs V/μs
Output Impedance (f = 20 Hz)	z_o	–	1.7	–	–	1.7	–	k ohms
Short-Circuit Output Current	I_{OS}	–	±17	–	–	±17	–	mAdc
Output Voltage Swing (R_L = 10 k ohms)	V_O	±2.5	±2.8	–	±2.3	±2.7	–	V_{pk}
Power Supply Sensitivity V_{EE} = constant, R_s ≤ 10 k ohms V_{CC} = constant, R_s ≤ 10 k ohms	 PSS+ PSS-	 – –	 50 100	 – –	 – –	 50 100	 – –	μV/V
Power Supply Current (Total)	I_{CC} I_{EE}	– –	8.3 8.3	12.5 12.5	– –	8.3 8.3	15 15	mAdc
DC Quiescent Power Consumption (Total) (V_O = 0)	P_C	–	100	150	–	100	180	mW

MATCHING CHARACTERISTICS

Open Loop Voltage Gain	$A_{vol1}-A_{vol2}$	–	±1.0	–	–	±1.0	–	dB
Input Bias Current	$I_{IB1}-I_{IB2}$	–	±0.15	–	–	±0.15	–	μA
Input Offset Current	$I_{IO1}-I_{IO2}$	–	±0.02	–	–	±0.02	–	μA
Average Temperature Coefficient	$TCI_{IO1}-TCI_{IO2}$	–	±0.1	–	–	±0.1	–	nA/°C
Input Offset Voltage	$V_{IO1}-V_{IO2}$	–	±0.1	–	–	±0.1	–	mV
Average Temperature Coefficient	$TCV_{IO1}-TCV_{IO2}$	–	±0.5	–	–	±0.5	–	μV/°C
Channel Separation (See Fig. 10) (f = 10 kHz)	$\frac{e_{o1}}{e_{o2}}$	–	-60	–	–	-60	–	dB

① T_{low}: 0°C for MC1435
-55°C for MC1535
T_{high}: +75°C for MC1435
+125°C for MC1535

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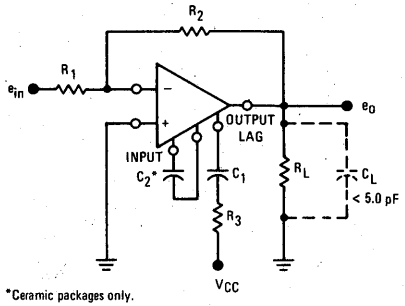
TYPICAL OUTPUT CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C.)

FIGURE 1 – TEST CIRCUIT



*Ceramic packages only.

FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS R_1(Ω)	R_2(Ω)	C_1(pF)	R_3(Ω)	C_2(pF)	OUTPUT NOISE mV(RMS)
2	3	1	47 k	47 k	100,000	4.7	0	0.12
	3A	or 1	47 k	47 k	0	∞	50,000	0.46
3	1	100	4.7 k	470 k	1,000	150	0	1.7
		or 100	4.7 k	470 k	0	∞	510	2.1
	2	10	47 k	470 k	10,000	47	0	1.0
		or 10	47 k	470 k	0	∞	5,000	2.1
	3	1	47 k	47 k	100,000	4.7	0	0.12
		or 1	47 k	47 k	0	∞	50,000	0.46
4	1	or Avol	100	∞	1,000	150	0	8.1
		Avol	100	∞	0	∞	510	8.1
	2	or Avol	100	∞	10,000	47	0	5.5
		Avol	100	∞	0	∞	5,000	5.5
	3	or Avol	100	∞	100,000	4.7	0	4.4
			100	∞	0	∞	50,000	4.4

FIGURE 2 – LARGE SIGNAL SWING versus FREQUENCY

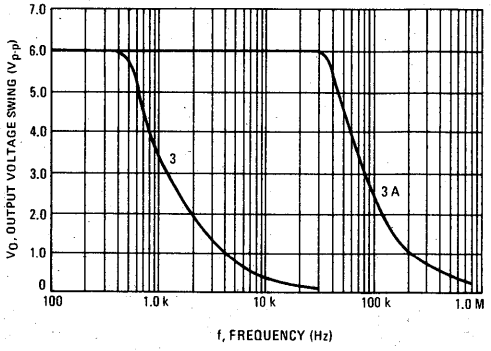


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

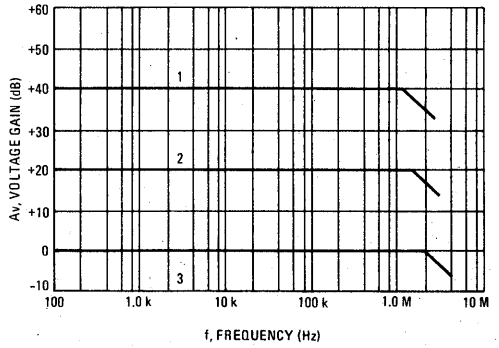


FIGURE 4 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

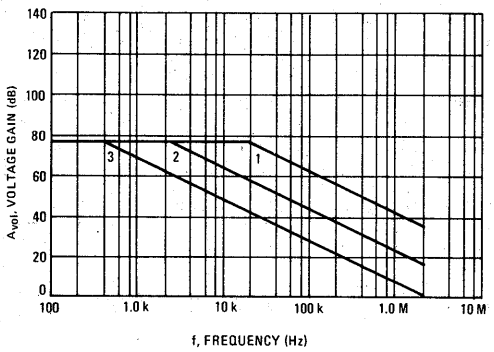
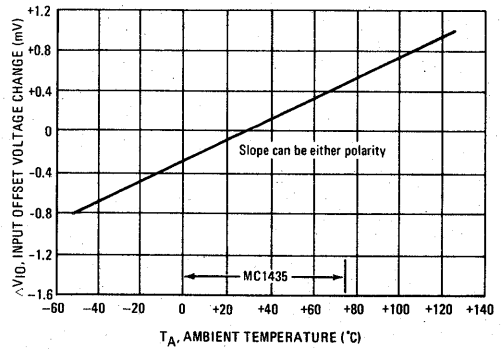


FIGURE 5 – INPUT OFFSET VOLTAGE versus TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

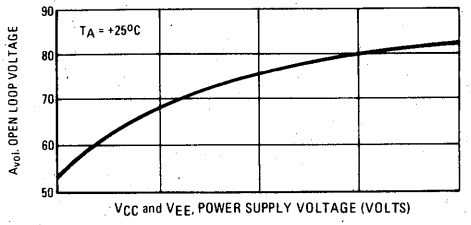


FIGURE 7 – COMMON MODE SWING versus POWER SUPPLY VOLTAGE

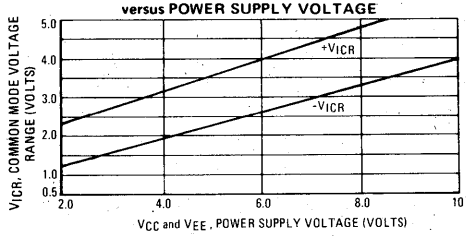


FIGURE 8 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGE

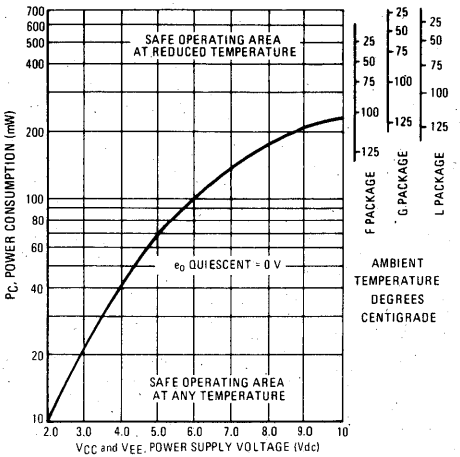
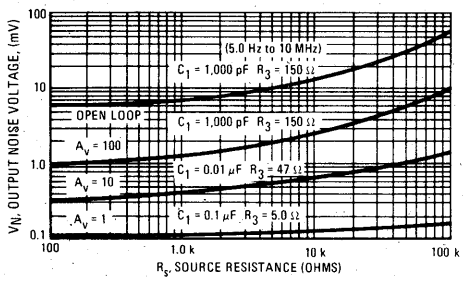


FIGURE 9 – OUTPUT WIDEBAND NOISE VOLTAGE versus SOURCE RESISTANCE



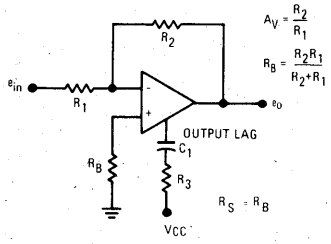
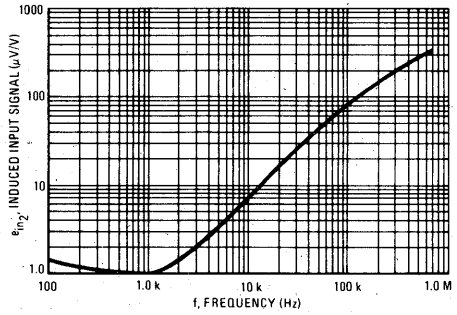
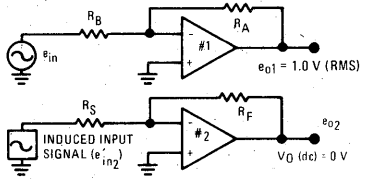


FIGURE 10 – INDUCED INPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY





Induced input signal (μV of induced input signal in amplifier #2 per volt of output signal at amplifier #1)

$e_{o2} = e_{in2}\left(\frac{RF}{RS}\right)$, where e_{o2} is the component of e_{o2} due only to lack of perfect separation between the two amplifiers.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1436G	0°C to +70°C	Metal Can
MC1436U	0°C to +70°C	Ceramic DIP
MC1436CG	0°C to +70°C	Metal Can
MC1436CU	0°C to +70°C	Ceramic DIP
MC1536G	−55°C to +125°C	Metal Can
MC1536U	−55°C to +125°C	Ceramic DIP

MC1436
MC1436C
MC1536

3

HIGH VOLTAGE, INTERNALLY COMPENSATED OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Maximum Supply Voltage – ±40 Vdc (MC1536)
- Output Voltage Swing –
  ±30 $V_{pk(min)}$ (V_{CC} = +36 V, V_{EE} = -36 V) (MC1536)
  ±22 $V_{pk(min)}$ (V_{CC} = +28 V, V_{EE} = -28 V)
- Input Bias Current – 20 nA max (MC1536)
- Input Offset Current – 3.0 nA max (MC1536)
- Fast Slew Rate – 2.0 V/μs typ
- Internally Compensated
- Offset Voltage Null Capability
- Input Over-Voltage Protection
- A_{VOL} – 500,000 typ
- Characteristics Independent of Power Supply Voltages – (±5.0 Vdc to ±36 Vdc)

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

METAL PACKAGE
CASE 601

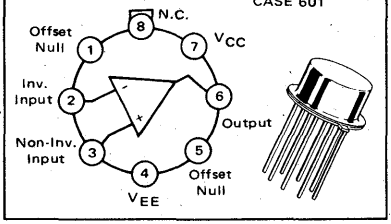
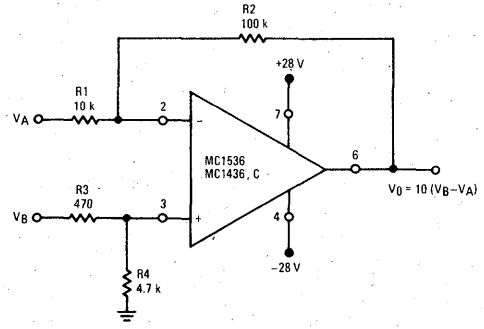
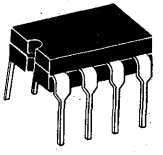


FIGURE 1 – DIFFERENTIAL AMPLIFIER WITH ± 20 V COMMON-MODE INPUT VOLTAGE RANGE



U SUFFIX
CERAMIC PACKAGE
CASE 693



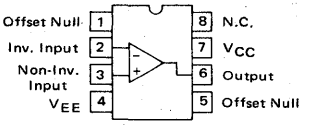


FIGURE 2 – TYPICAL NON-INVERTING X10 VOLTAGE AMPLIFIER

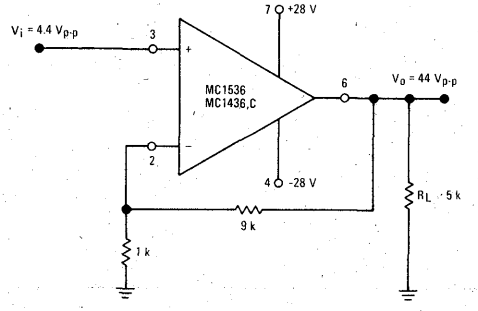
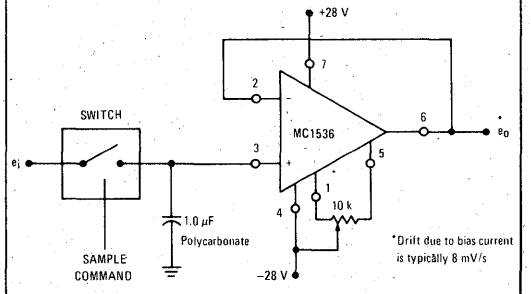


FIGURE 3 – LOW-DRIFT SAMPLE AND HOLD



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1536	MC1436	MC1436C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+40 -40	+34 -34	+30 -30	Vdc
Input Differential Voltage Range	V_{IDR}	± (V_{CC} + V_{EE} [-3])			Volts
Input Common-Mode Voltage Range	V_{ICR}	+V_{CC}, - (V_{EE} [-3])			Volts
Output Short Circuit Duration (V_{CC} = V_{EE} = 28 Vdc, V_o = 0)	t_S	5.0			s
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6			mW mW/°C
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70		°C
Storage Temperature Range	T_{stg}	-65 to +150			°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +28 Vdc, V_{EE} = - 28 Vdc, T_A = +25°C unless otherwise noted)

Characteristics	Symbol	MC1536 Min	MC1536 Typ	MC1536 Max	MC1436 Min	MC1436 Typ	MC1436 Max	MC1436C Min	MC1436C Typ	MC1436C Max	Unit
Input Bias Current	I_{IB}										nAdc
T_A = +25°C		–	8.0	20	–	15	40	–	25	90	
T_A = T_{low} to T_{high} (See Note 1)		–	–	35	–	–	55	–	–	–	
Input Offset Current	I_{IO}										nAdc
T_A = +25°C		–	1.0	3.0	–	5.0	10	–	10	25	
T_A = +25°C to T_{high}		–	–	4.5	–	–	14	–	–	–	
T_A = T_{low} to +25°C		–	–	7.0	–	–	14	–	–	–	
Input Offset Voltage	V_{IO}										mVdc
T_A = +25°C		–	2.0	5.0	–	5.0	10	–	5.0	12	
T_A = T_{low} to T_{high}		–	–	7.0	–	–	14	–	–	–	
Differential Input Impedance (Open-Loop, f ≤ 5.0 Hz)											
Parallel Input Resistance	r_P	–	10	–	–	10	–	–	10	–	Meg ohms
Parallel Input Capacitance	C_P	–	2.0	–	–	2.0	–	–	2.0	–	pF
Common-Mode Input Impedance (f ≤ 5.0 Hz)	z_{ic}	–	250	–	–	250	–	–	250	–	Meg ohms
Input Common-Mode Voltage Range	V_{ICR}	±24	±25	–	±22	±25	–	±18	±20	–	V_{pk}
Equivalent Input Noise Voltage	e_n										nV/(Hz)½
(A_V = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz)		–	50	–	–	50	–	–	50	–	
Common-Mode Rejection Ratio (dc)	CMRR	80	110	–	70	110	–	50	90	–	dB
Large Signal dc Open Loop Voltage Gain	A_{VOL}										V/V
(V_o = ± 10 V, R_L = 100 k ohms) T_A = +25°C		100,000	500,000	–	70,000	500,000	–	50,000	500,000	–	
(V_o = ± 10 V, R_L = 100 k ohms) T_A = T_{low} to T_{high}		50,000	–	–	50,000	–	–	–	–	–	
(V_o = ±10 V, R_L = 10 k ohms, T_A = +25°C)		–	200,000	–	–	200,000	–	–	200,000	–	
Power Bandwidth (Voltage Follower)	BWp										kHz
(A_V = 1, R_L = 5.0 k ohms, THD ≤ 5%, V_O = 40 Vp-p)		–	23	–	–	23	–	–	23	–	
Unity Gain Crossover Frequency (open-loop)	f_c	–	1.0	–	–	1.0	–	–	1.0	–	MHz
Phase Margin (open-loop, unity gain)	ϕm	–	50		–	50	–	–	50	–	degrees
Gain Margin	A_M	–	18	–	–	18	–	–	18	–	dB
Slew Rate (Unity Gain)	SR	–	2.0	–	–	2.0	–	–	2.0	–	V/μs
Output Impedance (f ≤ 5.0 Hz)	z_o	–	1.0	–	–	1.0	–	–	1.0	–	k ohms
Short-Circuit Output Current	I_{OS}	–	±17	–	–	±17	–	–	±19	–	mAdc
Output Voltage Range (R_L = 5.0 k ohms)	V_{OR}										V_{pk}
V_{CC} = +28 Vdc, V_{EE} = -28 Vdc		±22	±23	–	±20	±22	–	±20	±22	–	
V_{CC} = +36 Vdc, V_{EE} = -36 Vdc		±30	±32	–	–	–	–	–	–	–	
Power Supply Sensitivity (dc)											μV/V
V_{EE} = constant, R_s = 10 k ohms	PSS+	–	15	100	–	35	200	–	50	–	
V_{CC} = constant, R_s = 10 k ohms	PSS-	–	15	100	–	35	200	–	50	–	
Power Supply Current (See Note 2)	I_{CC}	–	2.2	4.0	–	2.6	5.0	–	2.6	5.0	mAdc
	I_{EE}	–	2.2	4.0	–	2.6	5.0	–	2.6	5.0	
DC Quiescent Power Consumption	P_C										mW
(V_o = 0)		–	124	224	–	146	280	–	146	280	

Note 1: T_{low}: 0°C for MC1436,C
-55°C for MC1536
T_{high}: +70°C for MC1436,C
+125°C for MC1536

Note 2: V_{CC} = V_{EE} = 5.0 Vdc to 36 Vdc for MC1536
V_{CC} = V_{EE} = 5.0 Vdc to 30 Vdc for MC1436
V_{CC} = V_{EE} = 5.0 Vdc to 28 Vdc for MC1436C

3

FIGURE 4 – POWER BANDWIDTH

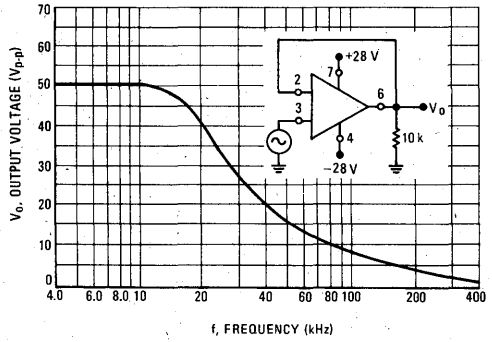


FIGURE 5 – PEAK OUTPUT VOLTAGE SWING versus POWER SUPPLY VOLTAGE

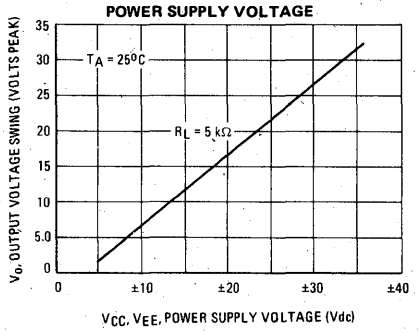


FIGURE 6 – OPEN-LOOP FREQUENCY RESPONSE

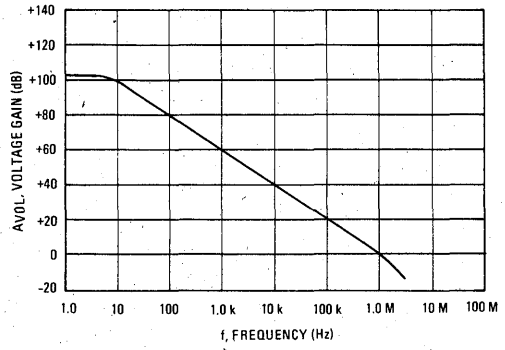


FIGURE 7 – OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE

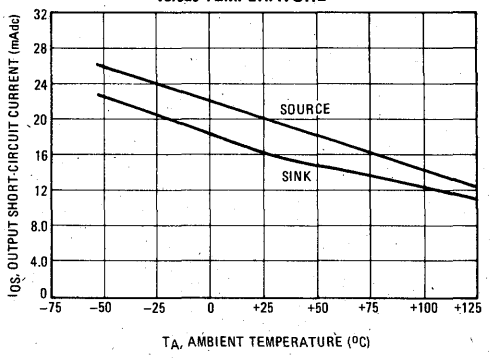


FIGURE 8 – INPUT BIAS CURRENT versus TEMPERATURE

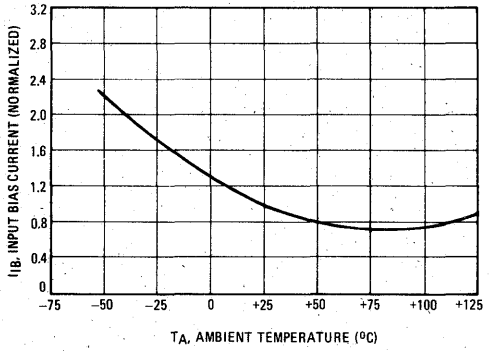


FIGURE 9 – INVERTING FEEDBACK MODEL

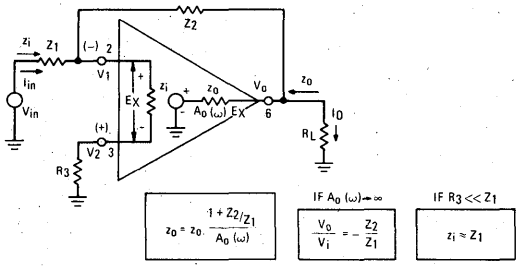


FIGURE 10 – NON-INVERTING FEEDBACK MODEL

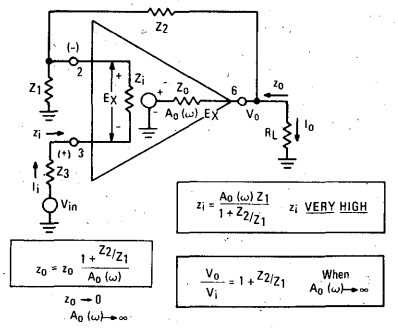


FIGURE 11 – AUDIO AMPLIFIER

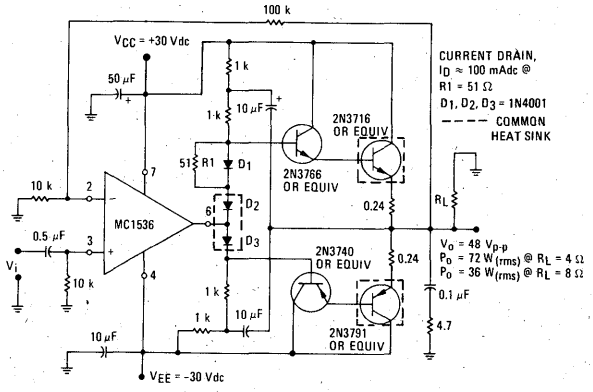


FIGURE 12 – VOLTAGE CONTROLLED CURRENT SOURCE or TRANSCONDUCTANCE AMPLIFIER WITH 0 TO 40 V COMPLIANCE

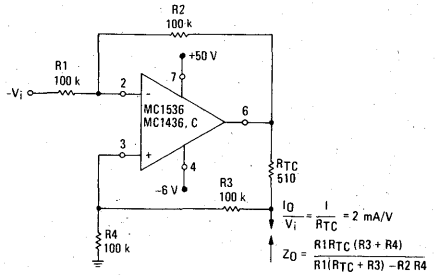


FIGURE 13 – REPRESENTATIVE CIRCUIT SCHEMATIC

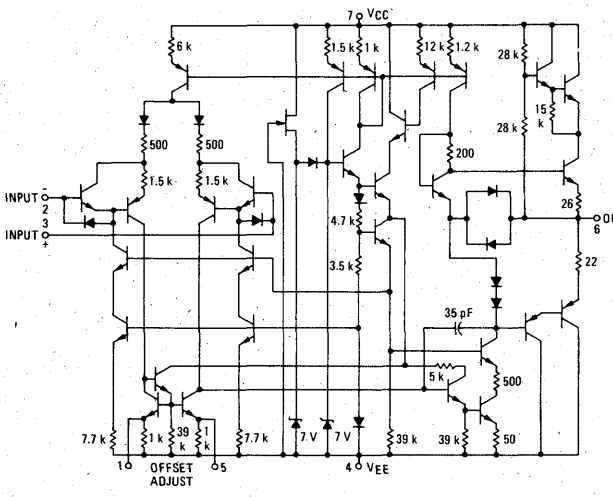
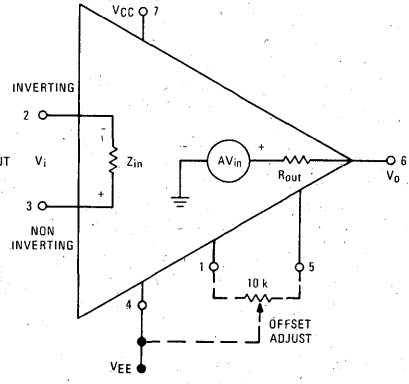


FIGURE 14 – EQUIVALENT CIRCUIT



ORDERING INFORMATION

Device	Temperature Range	Package
MC1437L	0°C to +70°C	Ceramic DIP
MC1437P	0°C to +70°C	Plastic DIP
MC1537L	−55°C to +125°C	Ceramic DIP

MC1437
MC1537

HIGHLY MATCHED DUAL OPERATIONAL AMPLIFIERS

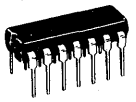
. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. Ideal for chopper stabilized applications where extremely high gain is required with excellent stability.

Typical Amplifier Features:

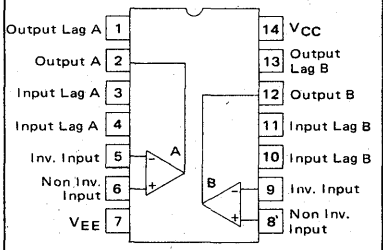
- High-Performance Open Loop Gain Characteristics – A_{VOL} = 45,000 typical
- Low Temperature Drift – ±3 μV/°C
- Large Output Voltage Swing – ±14 V typical @ ±15 V Supply

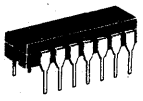
DUAL MC1709 OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1437P only)



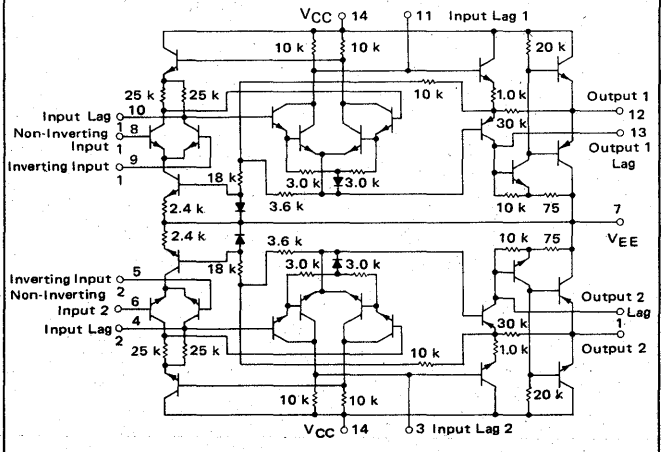


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

MAXIMUM RATINGS (T_A = +25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
	V_{EE}	-18	Vdc
Differential Input Voltage Range	V_{IDR}	±5.0	Volts
Common-Mode Input Voltage Range	V_{ICR}	$\pm V_{CC}$	Volts
Output Short Circuit Duration	t_S	5.0	s
Power Dissipation (Package Limitation)	P_D		
Ceramic Package		750	mW
Derate above T_A = +25°C		6.0	mW/°C
Plastic Package MC1437P		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Ambient Temperature Range	T_A		°C
MC1537		-55 to +125	
MC1437		0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS – Each Amplifier (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1537 Min	MC1537 Typ	MC1537 Max	MC1437 Min	MC1437 Typ	MC1437 Max	Unit
Open Loop Voltage Gain (R_L = 5.0 kΩ, V_o = ±10 V, T_A = T_{low} ① to T_{high} ②)	A_{VOL}	25,000	45,000	70,000	15,000	45,000	–	–
Output Impedance (f = 20 Hz)	z_o	–	30	–	–	30	–	Ω
Input Impedance (f = 20 Hz)	z_i	150	400	–	50	150	–	kΩ
Output Voltage Range (R_L = 10 kΩ)	V_{OR}	±12	±14	–	±12	±14	–	V_{peak}
(R_L = 2.0 kΩ)		±10	±13	–	–	–	–	
Input Common-Mode Voltage Range	V_{ICR}	±8.0	±10	–	±8.0	±10	–	V_{peak}
Common-Mode Rejection Ratio	CMRR	70	100	–	65	100	–	dB
Input Bias Current $\left(I_{IB} = \frac{I_1 + I_2}{2}\right)$ (T_A = +25°C)	I_{IB}	–	0.2	0.5	–	0.4	1.5	μA
(T_A = T_{low} ①)		–	0.5	1.5	–	–	2.0	
Input Offset Current ($I_{IO} = I_1 - I_2$)	I_{IO}	–	0.05	0.2	–	0.05	0.5	μA
($I_{IO} = I_1 - I_2$, T_A = T_{low} ①)		–	–	0.5	–	–	0.75	
($I_{IO} = I_1 - I_2$, T_A = T_{high} ②)		–	–	0.2	–	–	0.75	
Input Offset Voltage (T_A = +25°C)	V_{IO}	–	1.0	5.0	–	1.0	7.5	mV
(T_A = T_{low} ① to T_{high} ②)		–	–	6.0	–	–	10	
Step Response: Gain = 100, 5% overshoot, R_1 = 1 kΩ, R_2 = 100 kΩ, R_3 = 1.5 kΩ, C_1 = 100 pF, C_2 = 3.0 pF	t_{TLH}	–	0.8	–	–	0.8	–	μs
	t_{PLH}-t_{PHL}	–	0.38	–	–	0.38	–	μs
	SR	–	12	–	–	12	–	V/μs
Gain = 10, 10% overshoot, R_1 = 1 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 500 pF, C_2 = 20 pF	t_{TLH}	–	0.6	–	–	0.6	–	μs
	t_{PLH}-t_{PHL}	–	0.34	–	–	0.34	–	μs
	SR	–	1.7	–	–	1.7	–	V/μs
Gain = 1, 5% overshoot, R_1 = 10 kΩ, R_2 = 10 kΩ, R_3 = 1.5 kΩ, C_1 = 5000 pF, C_2 = 200 pF	t_{TLH}	–	2.2	–	–	2.2	–	μs
	t_{PLH}-t_{PHL}	–	1.3	–	–	1.3	–	μs
	SR	–	0.25	–	–	0.25	–	V/μs
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = T_{low} ① to T_{high} ②)	$\Delta V_{IO}/\Delta T$	–	1.5	–	–	1.5	–	μV/°C
($R_S \leq$ 10 kΩ, T_A = T_{low} ① to T_{high} ②)		–	3.0	–	–	3.0	–	
Average Temperature Coefficient of Input Offset Voltage (T_A = T_{low} ① to +25°C)	$\Delta I_{IO}/\Delta T$	–	0.7	–	–	0.7	–	nA/°C
(T_A = +25°C to T_{high} ②)		–	0.7	–	–	0.7	–	
DC Power Consumption (Total) (Power Supply = ±15 V, V_o = 0)	P_C	–	160	225	–	160	225	mW
Positive Supply Sensitivity (V_{EE} constant)	PSS+	–	10	150	–	10	200	μV/V
Negative Supply Sensitivity (V_{CC} constant)	PSS–	–	10	150	–	10	200	μV/V

① T_{low} = 0°C for MC1437
= -55°C for MC1537

② T_{high} = +70°C for MC1437
= +125°C for MC1537

MATCHING CHARACTERISTICS

Open Loop Voltage Gain	A_{VOL1}-A_{VOL2}	–	±1.0	–	–	±1.0	–	dB
Input Bias Current	I_{IB1}-I_{IB2}	–	±0.15	–	–	±0.15	–	μA
Input Offset Current	I_{IO1}-I_{IO2}	–	±0.02	–	–	±0.02	–	μA
Average Temperature Coefficient	$\left\lvert\frac{\Delta I_{IO1}}{\Delta T}\right\rvert - \left\lvert\frac{\Delta I_{IO2}}{\Delta T}\right\rvert$	–	±0.2	–	–	±0.2	–	nA/°C
Input Offset Voltage	V_{IO1}-V_{IO2}	–	±0.2	–	–	±0.2	–	mV
Average Temperature Coefficient	$\left\lvert\frac{\Delta V_{IO1}}{\Delta T}\right\rvert - \left\lvert\frac{\Delta V_{IO2}}{\Delta T}\right\rvert$	–	±0.5	–	–	±0.5	–	μV/°C
Channel Separation (f = 10 kHz)	$\frac{e_{o1}}{e_{o2}}$	–	90	–	–	90	–	dB

3

TYPICAL OUTPUT CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT
V_{CC} = +15 Vdc, V_{EE} = 15 Vdc, T_A = 25°C

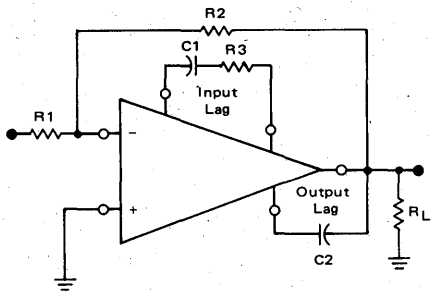


FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS $R_1(\Omega)$	$R_2(\Omega)$	$R_3(\Omega)$	C_1(pF)	C_2(pF)	OUTPUT NOISE (mV[rms])
4	1	1	10 k	10 k	1.5 k	5.0 k	200	0.10
	2	10	10 k	100 k	1.5 k	500	20	0.14
	3	100	10 k	1.0 M	1.5 k	100	3.0	0.7
	4	1000	1.0 k	1.0 M	0	10	3.0	5.2
5	1	1	10 k	10 k	1.5 k	5.0 k	200	0.10
	2	10	10 k	100 k	1.5 k	500	20	0.14
	3	100	10 k	1.0 M	1.5 k	100	3.0	0.7
	4	1000	1.0 k	1.0 M	0	10	3.0	5.2
6	1	A_{VOL}	0	∞	1.5 k	5.0 k	200	5.5
	2	A_{VOL}	0	∞	1.5 k	500	20	10.5
	3	A_{VOL}	0	∞	1.5 k	100	3.0	21.0
	4	A_{VOL}	0	∞	0	10	3.0	39.0
	5	A_{VOL}	0	∞	∞	0	3.0	—

FIGURE 4 – LARGE SIGNAL SWING versus FREQUENCY

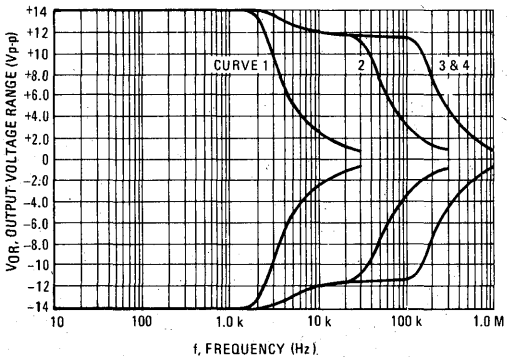


FIGURE 5 – VOLTAGE GAIN *versus* FREQUENCY

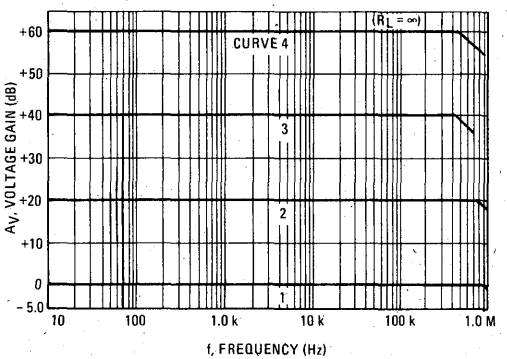


FIGURE 6 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

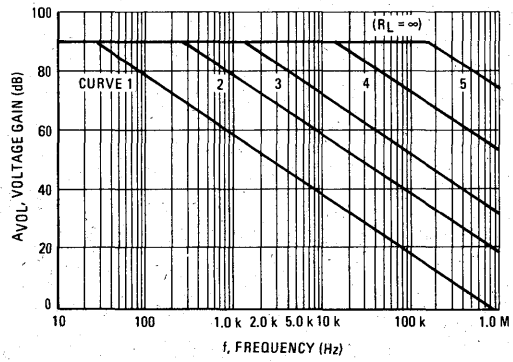
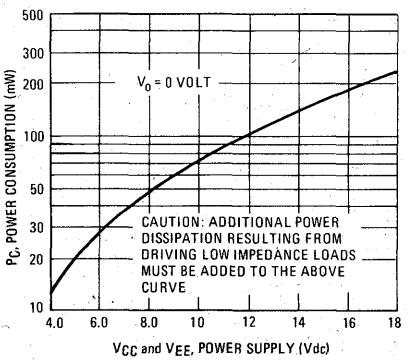


FIGURE 7 – TOTAL POWER CONSUMPTION versus POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

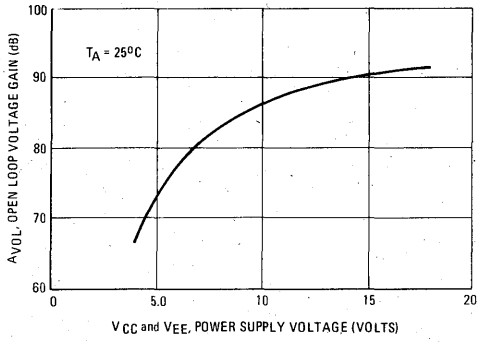


FIGURE 9 – COMMON INPUT SWING versus POWER SUPPLY VOLTAGE

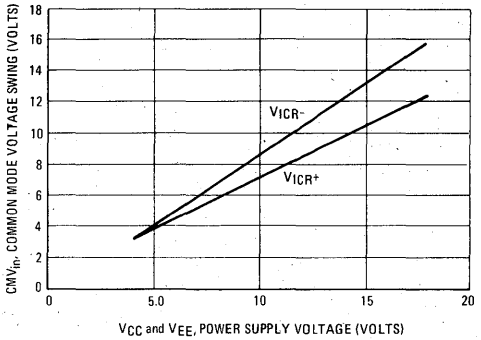


FIGURE 10 – INPUT OFFSET VOLTAGE versus TEMPERATURE

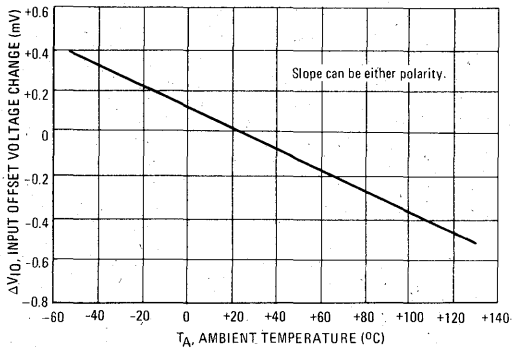


FIGURE 11 – OUTPUT NOISE VOLTAGE versus SOURCE RESISTANCE

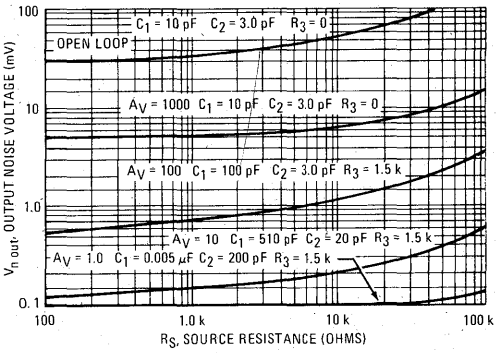
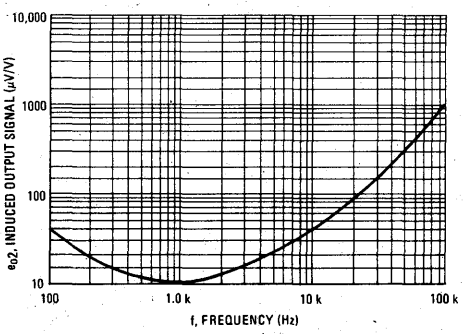
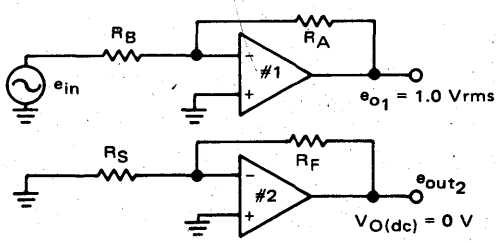


FIGURE 12 – INDUCED OUTPUT SIGNAL (CHANNEL SEPARATION) versus FREQUENCY





Induced output signal (μV of induced output signal in amplifier #2 per volt of output signal at amplifier #1).

ORDERING INFORMATION

Device	Temperature Range	Package
MC1439G	0°C to +70°C	Metal Can
MC1439L	0°C to +70°C	Ceramic DIP
MC1439P1,P2	0°C to +70°C	Plastic DIP
MC1539G	−55°C to +125°C	Metal Can
MC1539L	−55°C to +125°C	Ceramic DIP

MC1439
MC1539

UNCOMPENSATED OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components. For detailed information see Motorola Application Note AN-439.

- Low Input Offset Voltage – 3.0 mV max
- Low Input Offset Current – 60 nA max
- Large Power-Bandwidth – 20 V_{p-p} Output Swing at 20 kHz min
- Output Short-Circuit Protection
- Input Over-Voltage Protection
- Class AB Output for Excellent Linearity
- High Slew Rate – 34 V/μs typ

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

FIGURE 1 – HIGH SLEW-RATE INVERTER

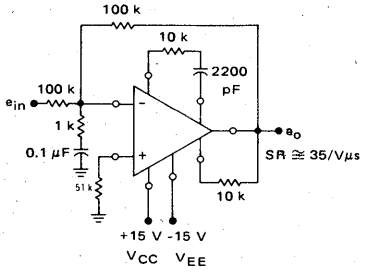
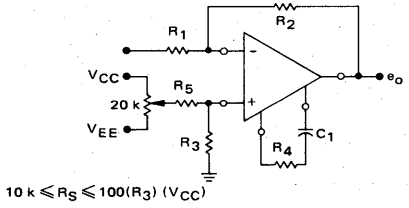
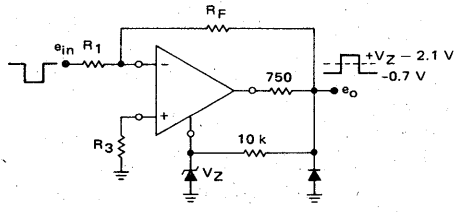


FIGURE 2 – OUTPUT NULLING CIRCUIT

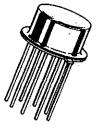


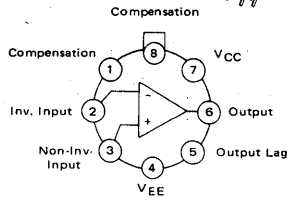
$10\ k \leqslant R_S \leqslant 100(R_3)\ (V_{CC})$

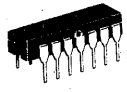
FIGURE 3 – OUTPUT LIMITING CIRCUIT



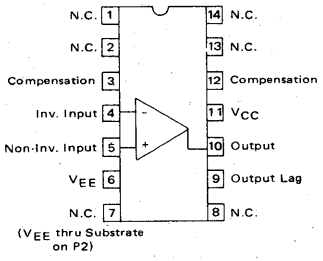
G SUFFIX
METAL PACKAGE
CASE 601



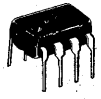




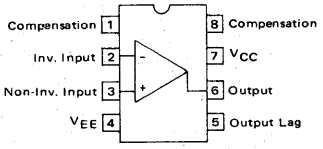
L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)



P2 SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1439 only)



P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1439 only)



MC1439, MC1539

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1539 Min	MC1539 Typ	MC1539 Max	MC1439 Min	MC1439 Typ	MC1439 Max	Unit
Input Bias Current	I_{IB}							μA
(T_A = +25°C)		–	0.20	0.50	–	0.20	1.0	
(T_A = T_{low} ①)		–	0.23	0.70	–	0.23	1.5	
Input Offset Current	$\|I_{IO}\|$							nA
(T_A = T_{low})		–	–	75	–	–	150	
(T_A = +25°C)		–	20	60	–	20	100	
(T_A = T_{high} ①)		–	–	75	–	–	150	
Input Offset Voltage	$\|V_{IO}\|$							mV
(T_A = +25°C)		–	1.0	3.0	–	2.0	7.5	
(T_A = T_{low}, T_{high})		–	–	4.0	–	–	–	
Average Temperature Coefficient of Input Offset Voltage (T_A = T_{low} to T_{high})	$\|TCV_{IO}\|$							μV/°C
(R_S = 50 Ω)		–	3.0	–	–	3.0	–	
($R_S \leq$ 10 kΩ)		–	5.0	–	–	5.0	–	
Input Impedance (f = 20 Hz)	z_{in}	150	300	–	100	300	–	kΩ
Input Common-Mode Voltage Range	V_{ICR}	±11	±12	–	±11	±12	–	V_{pk}
Equivalent Input Noise Voltage (R_S = 10 kΩ, Noise Bandwidth = 1.0 Hz, f = 1.0 kHz)	e_n	–	30	–	–	30	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 1.0 kHz)	CMRR	80	110	–	80	110	–	dB
Open-Loop Voltage Gain (V_O = ±10 V, R_L = 10 kΩ, R_S = ∞) (T_A = +25°C to T_{high})	A_{vol}	50,000	120,000	–	15,000	100,000	–	–
(T_A = T_{low})		25,000	100,000	–	15,000	100,000	–	
Power Bandwidth (A_v = 1, THD ≤ 5%, V_O = 20 Vp-p)	PBW							kHz
(R_L = 2.0 kΩ)		–	–	–	10	50	–	
(R_L = 1.0 kΩ, R_S = 10 k)		20	50	–	–	–	–	
Step Response								
Gain = 1000, no overshoot, R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ, R4 = 30 kΩ, R5 = 10 kΩ, C1 = 1000 pF	t_{THL}	–	130	–	–	130	–	ns
	t_{pd}	–	190	–	–	190	–	ns
	SR	–	6.0	–	–	6.0	–	V/μs
Gain = 1000, 15% overshoot, R1 = 1.0 kΩ, R2 = 1.0 MΩ, R3 = 1.0 kΩ, R4 = 0, R5 = 10 kΩ, C1 = 10 pF	t_{THL}	–	80	–	–	80	–	ns
	t_{pd}	–	100	–	–	100	–	ns
	SR	–	14	–	–	14	–	V/μs
Gain = 100, no overshoot, R1 = 1.0 kΩ, R2 = 100 kΩ, R3 = 1.0 kΩ, R4 = 10 kΩ, R5 = 10 kΩ, C1 = 2200 pF	t_{THL}	–	60	–	–	60	–	ns
	t_{pd}	–	100	–	–	100	–	ns
	SR	–	34	–	–	34	–	V/μs
Gain = 10, 15% overshoot, R1 = 1.0 kΩ, R2 = 10 kΩ, R3 = 1.0 kΩ, R4 = 1.0 kΩ, R5 = 10 kΩ, C1 = 2200 pF	t_{THL}	–	120	–	–	120	–	ns
	t_{pd}	–	80	–	–	80	–	ns
	SR	–	6.25	–	–	6.25	–	V/μs
Gain = 1, 15% overshoot, R1 = 10 kΩ, R2 = 10 kΩ, R3 = 5.0 kΩ, R4 = 390 Ω, R5 = 10 kΩ, C1 = 2200 pF	t_{THL}	–	160	–	–	160	–	ns
	t_{pd}	–	80	–	–	80	–	ns
	SR	–	4.2	–	–	4.2	–	V/μs
Output Impedance (f = 20 Hz)	z_o	–	4.0	–	–	4.0	–	kΩ
Output Voltage Swing	V_O							V_{pk}
(R_L = 2.0 kΩ, f = 1.0 kHz)		–	–	–	±10	±13	–	
(R_L = 1.0 kΩ, f = 1.0 kHz)		±10	±13	–	–	–	–	
Positive Supply Rejection Ratio (V_{EE} constant, R_S = ∞)	PSRR+	–	50	150	–	50	200	μV/V
Negative Supply Rejection Ratio (V_{CC} constant, R_S = ∞)	PSRR-	–	50	150	–	50	200	μV/V
Power Supply Current (V_O = 0)	I_{CC}	–	3.0	5.0	–	3.0	6.7	mAdc
	I_{EE}	–	3.0	5.0	–	3.0	6.7	

① T_{low} = 0°C for MC1439, −55°C for MC1539 T_{high} = +70°C for MC1439, +125°C for MC1539

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 +18	Vdc
Differential Input Voltage Range	V_{IDR}	±(V_{CC} + |V_{EE}|)	Vdc
Common-Mode Input Voltage Range	V_{ICR}	+V_{CC},-|V_{EE}|	Vdc
Load Current	I_L	15	mA
Output Short-Circuit Duration	t_S	Continuous	
Power Dissipation (Package Limitation) Metal Package Derate above T_A = +25°C Ceramic Dual In-Line Package Derate above T_A = +25°C Plastic Dual In-Line Packages MC1439 Derate above T_A = +25°C	P_D	 680 4.6 750 6.0 625 5.0	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range MC1539 MC1439	T_A	-55 to +125 0 to +70	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Packages	T_{stg}	 -65 to +150 -55 to +125	°C

FIGURE 4 – EQUIVALENT CIRCUIT SCHEMATIC

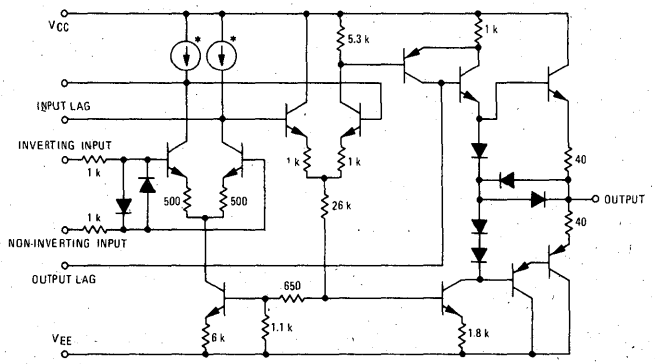
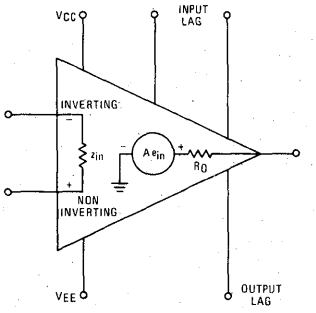


FIGURE 5 – EQUIVALENT CIRCUIT

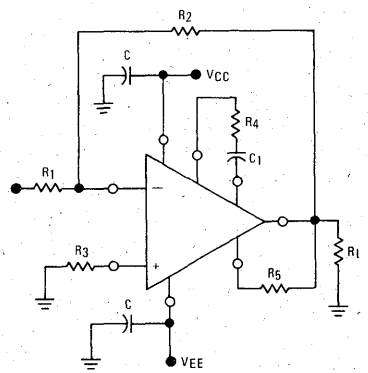


TYPICAL OUTPUT CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C

FIGURE NO.	CURVE NO.	VOLTAGE GAIN	TEST CONDITIONS (FIGURE 6) R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	R_5 (Ω)	C_1 (pF)
7,10,12	1	A_{vol}	0	∞	0	∞	∞	0
	2	1	10 k	10 k	5.0 k	390	10 k	2200
	3	10	1.0 k	10 k	1.0 k	1.0 k	10 k	2200
	4	100	1.0 k	100 k	1.0 k	10 k	10 k	2200
	5	1000	1.0 k	1.0 M	1.0 k	30 k	10 k	1000
	6	1000	1.0 k	1.0 M	1.0 k	0	10 k	10
8	1	A_{vol}	0	∞	0	∞	∞	0
	2	↓	↓	↓	↓	390	↓	2200
	3					1.0 k		2200
	4					10 k		2200
	5					30 k		1000
	6					0		10
13	ALL	1	10 k	10 k	5.0 k	390	10 k	2200
14	ALL	10	1.0 k	10 k	1.0 k	1.0 k	10 k	2200
15	ALL	100	1.0 k	100 k	1.0 k	10 k	10 k	2200
16	ALL	1000	1.0 k	1.0 M	1.0 k	30 k	10 k	2200

FIGURE 6 – TEST CIRCUIT



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 7 – LARGE-SIGNAL SWING versus FREQUENCY

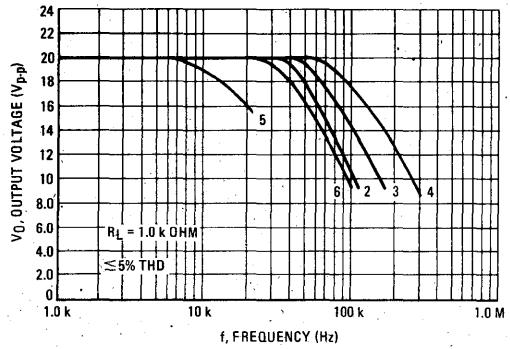


FIGURE 8 – OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

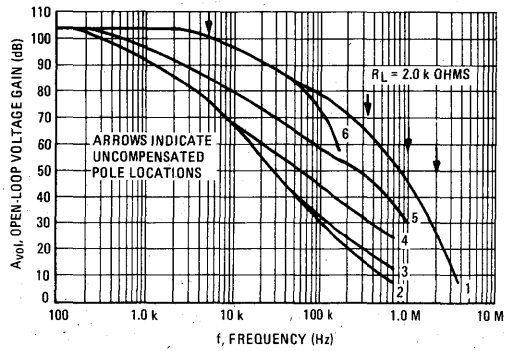


FIGURE 9 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

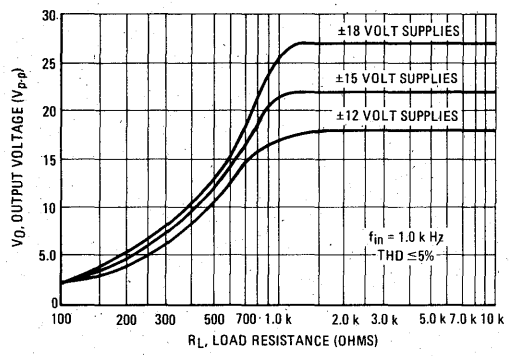


FIGURE 10 – OPEN-LOOP PHASE-SHIFT versus FREQUENCY

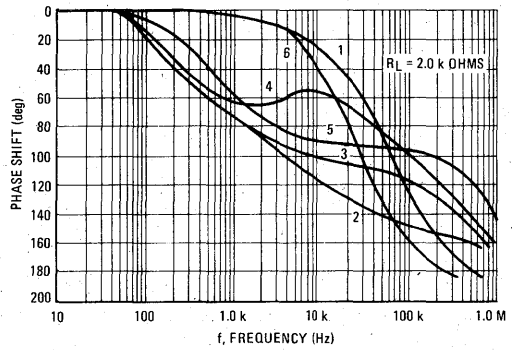


FIGURE 11 – OUTPUT VOLTAGE SWING (*to clipping*) versus SUPPLY

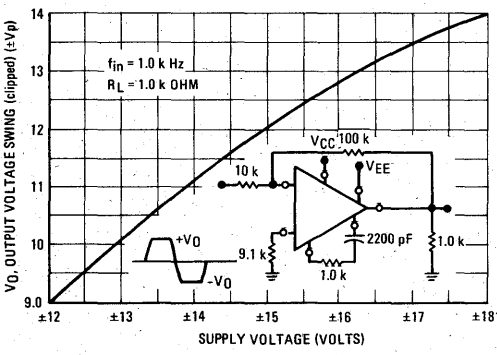
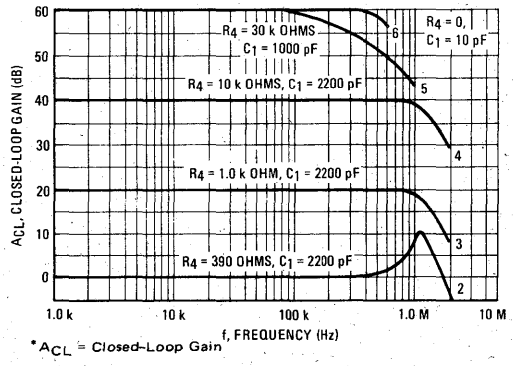


FIGURE 12 – CLOSED-LOOP GAIN versus FREQUENCY



*A_{CL} = Closed-Loop Gain

3

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 13 – A_{CL}* = 1 RESPONSE versus TEMPERATURE

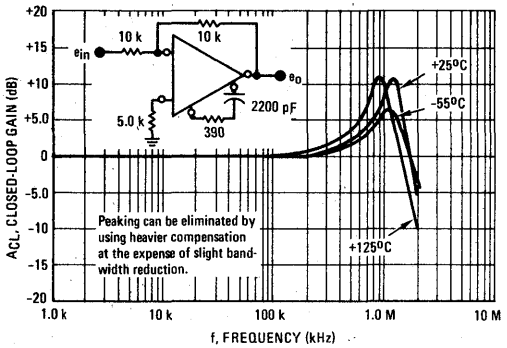


FIGURE 14 – A_{CL} = 10 RESPONSE versus TEMPERATURE

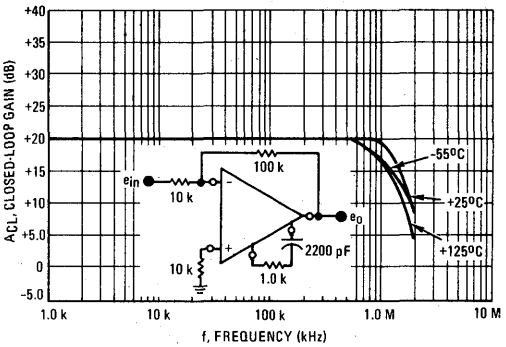


FIGURE 15 – A_{CL} = 100 RESPONSE versus TEMPERATURE

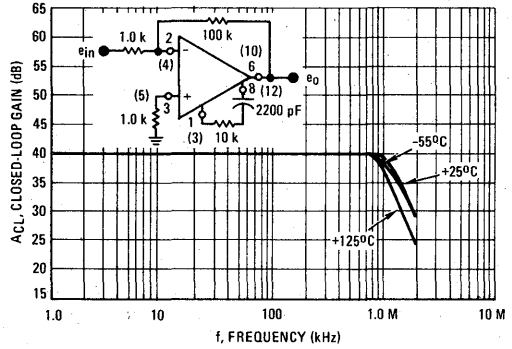


FIGURE 16 – A_{CL} = 1000 RESPONSE versus TEMPERATURE

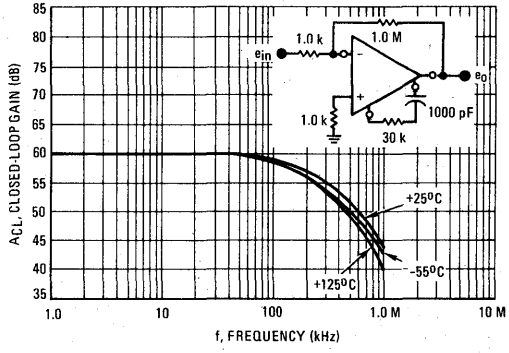


FIGURE 17 – SPECTRAL NOISE DENSITY

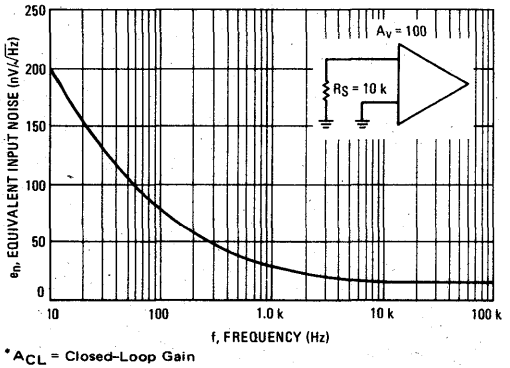
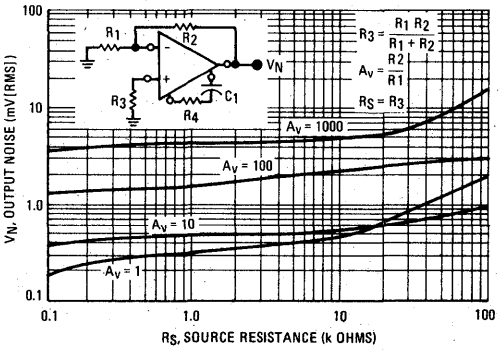


FIGURE 18 – OUTPUT NOISE versus SOURCE RESISTANCE



*A_{CL} = Closed-Loop Gain

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C, unless otherwise noted.)

FIGURE 19 – POWER DISSIPATION versus TEMPERATURE

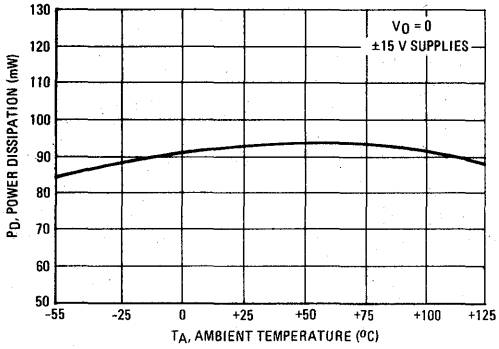


FIGURE 20 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE

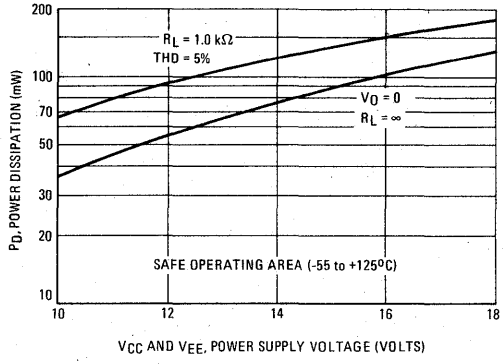


FIGURE 21 – POWER BANDWIDTH (LARGE-SIGNAL SWING versus FREQUENCY)

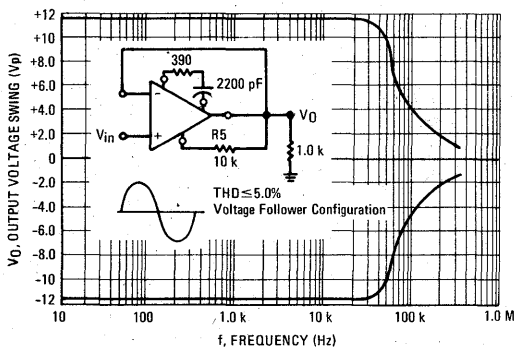


FIGURE 22 – COMMON-MODE INPUT VOLTAGE versus SUPPLY VOLTAGE

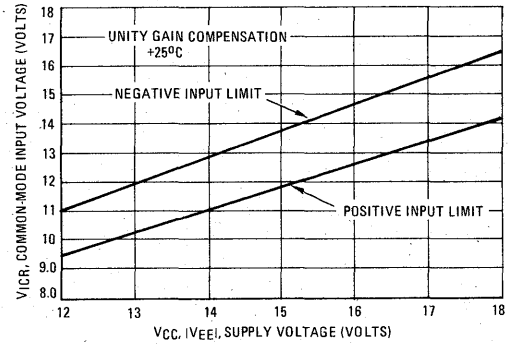


FIGURE 23 – COMMON-MODE REJECTION RATIO versus FREQUENCY

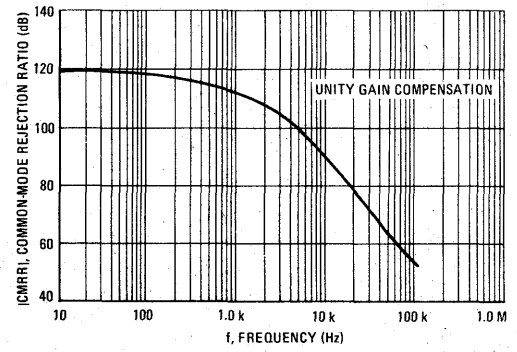


FIGURE 24 – COMMON-MODE REJECTION RATIO versus TEMPERATURE

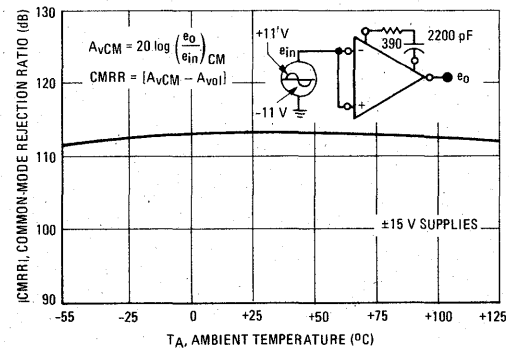
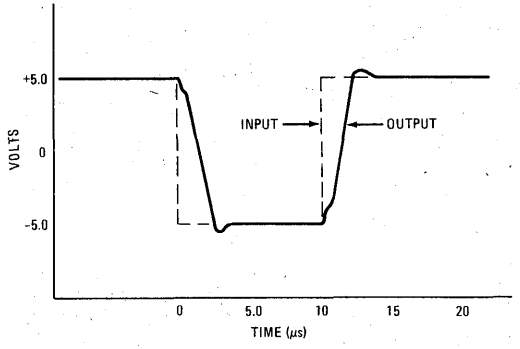
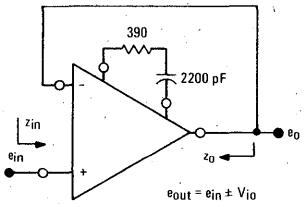


FIGURE 25 – VOLTAGE-FOLLOWER PULSE RESPONSE



TYPICAL APPLICATIONS

FIGURE 26 – VOLTAGE FOLLOWER

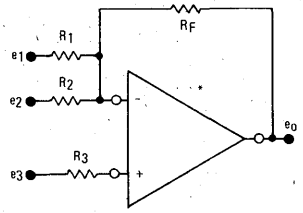


$e_{out} = e_{in} \pm V_{io}$

$z_{in} > 40$ M OHMS

$$z_{OCL} = z_{OOL}\left[\frac{1+\frac{R_F}{R_i}}{A_{OI}}\right] = 4\text{ k}\left[\frac{1+0}{10^5}\right] \approx 0.04\text{ OHM}$$

FIGURE 27 – DIFFERENTIAL AMPLIFIER

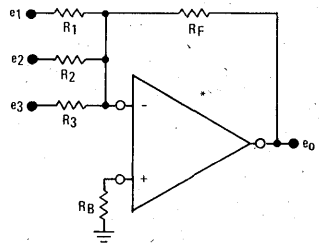


$$e_o = -\left[\frac{R_F}{R_1}e_1 + \frac{R_F}{R_2}e_2\right] + \left[1+\frac{R_F}{R_3}\right]e_3$$

For $R_3 = \frac{R_1, R_2}{R_1 + R_2}$

*Properly Compensated

FIGURE 28 – SUMMING AMPLIFIER

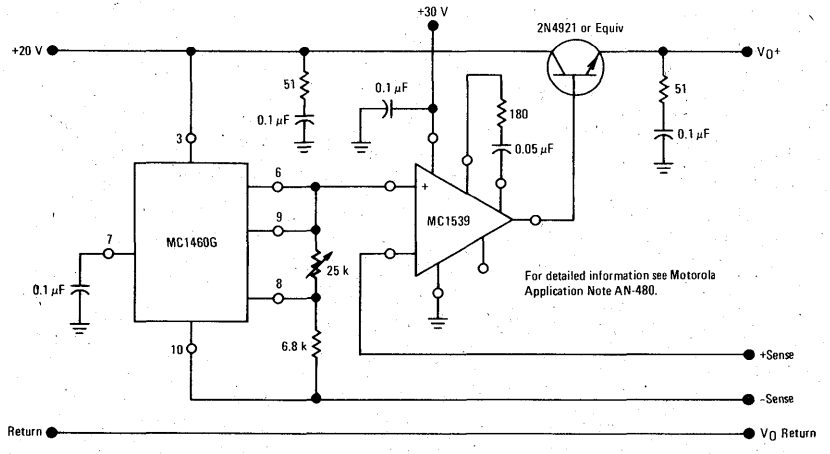


R_B = Parallel Combination of R_1, R_2, R_3, R_F.

$$e_o = -\left[\frac{R_F}{R_1}e_1 + \frac{R_F}{R_2}e_2 + \frac{R_F}{R_3}e_3\right]$$

*Properly Compensated

FIGURE 29 – +15 VOLT REGULATOR



TYPICAL APPLICATIONS (continued)

FIGURE 30 – LOAD REGULATION FOR CIRCUIT OF FIGURE 29

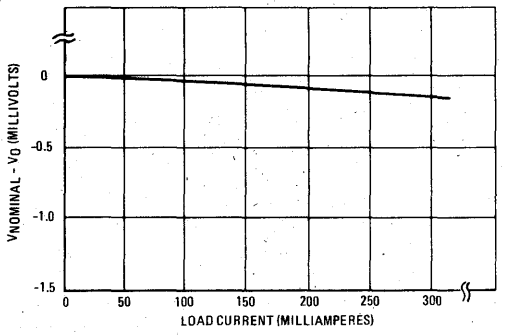
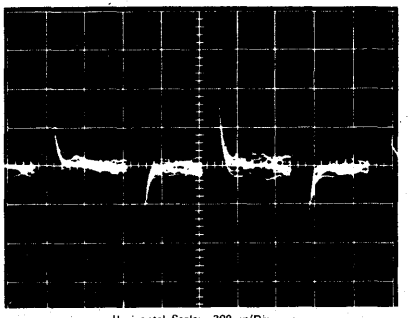


FIGURE 31 – REGULATOR OUTPUT VOLTAGE (under pulsed load condition)



Horizontal Scale: 200 μs/Div
Vertical Scale: 1 mV/Div

ORDERING INFORMATION

Device	Temperature Range	Package
MC1456G,CG	0°C to +70°C	Metal Can
MC1456CL,L,CU,U	0°C to +70°C	Ceramic DIP
MC1456CP1,P1	0°C to +70°C	Plastic DIP
MC1556G	−55°C to +125°C	Metal Can
MC1556L	−55°C to +125°C	Ceramic DIP
MC1556U	−55°C to +125°C	Ceramic DIP

MC1456
MC1456C
MC1556

3

INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATIONAL AMPLIFIER

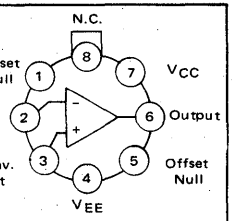
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components. For detailed information, see Application Note AN-522.

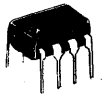
- Low Input Bias Current – 15 nA max
- Low Input Offset Current – 2.0 nA max
- Low Input Offset Voltage – 4.0 mV max
- Fast Slew Rate – 2.5 V/μs typ
- Large Power Bandwidth – 40 kHz typ
- Low Power Consumption – 45 mW max
- Offset Voltage Null Capability
- Output Short-Circuit Protection
- Input Over-Voltage Protection

OPERATIONAL AMPLIFIER

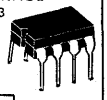
SILICON MONOLITHIC INTEGRATED CIRCUIT

G PACKAGE
CASE 601



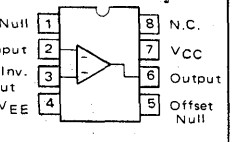


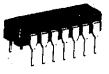
U SUFFIX
CERAMIC PACKAGE
CASE 693

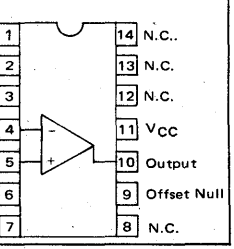


P1 SUFFIX
PLASTIC PACKAGE
CASE 626

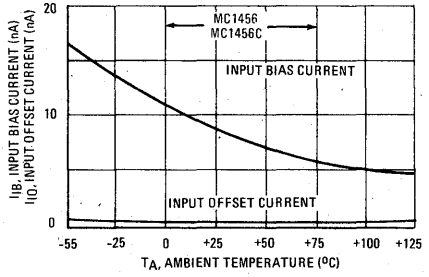
L PACKAGE
CASE 632
TO-116



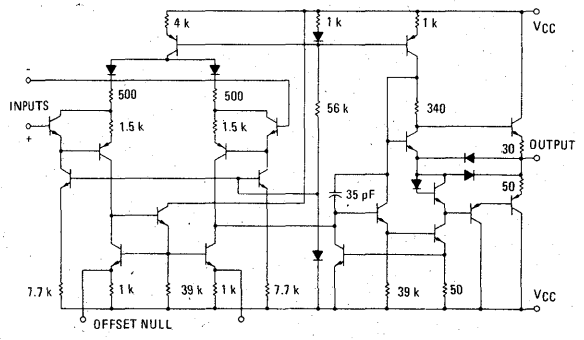




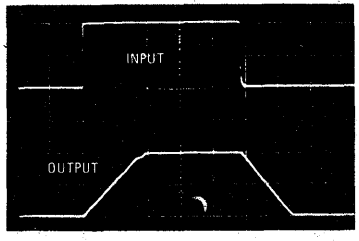
TYPICAL INPUT BIAS CURRENT AND INPUT OFFSET CURRENT versus TEMPERATURE for MC1556



REPRESENTATIVE CIRCUIT SCHEMATIC



VOLTAGE-FOLLOWER PULSE RESPONSE



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1556	MC1456 / MC1456C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Differential Input Voltage Range	V_{IDR}	±V_{CC}		Volts
Common-Mode Voltage Range	V_{ICR}	±V_{CC}		Volts
Load Current	I_L	20		mA
Output Short Circuit Duration	t_S	Continuous		
Power Dissipation (Package Limitation) *Derate above* T_A = +25°C	P_D	680 4.6		mW mW/°C
Operating Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = - 15 Vdc, T_A = +25°C *unless otherwise noted*).

Characteristic	Fig.	Symbol	MC1556 Min	MC1556 Typ	MC1556 Max	MC1456 Min	MC1456 Typ	MC1456 Max	MC1456C Min	MC1456C Typ	MC1456C Max	Unit
Input Bias Current		I_{IB}										nAdc
T_A = +25°C			–	8.0	15	–	15	30	–	15	90	
T_A = T_{low} to T_{high} (See Note 1)			–	–	30	–	–	40	–	–	–	
Input Offset Current		I_{IO}										nAdc
T_A = +25°C			–	1.0	2.0	–	5.0	10	–	5.0	30	
T_A = +25°C to T_{high}			–	–	3.0	–	–	14	–	–	–	
T_A = T_{low} to +25°C			–	–	5.0	–	–	14	–	–	–	
Input Offset Voltage		V_{IO}										mVdc
T_A = +25°C			–	2.0	4.0	–	5.0	10	–	5.0	12	
T_A = T_{low} to T_{high}			–	–	6.0	–	–	14	–	–	–	
Differential Input Impedance (Open-Loop, f = 20 Hz)												
Parallel Input Resistance		r_p	–	5.0	–	–	3.0	–	–	3.0	–	Megohms
Parallel Input Capacitance		c_p	–	6.0	–	–	6.0	–	–	6.0	–	pF
Common-Mode Input Impedance (f = 20 Hz)		z_i	–	250	–	–	250		–	250	–	Megohms
Common-Mode Input Voltage Range	1	V_{ICR}	±12	±13	–	+11	±12	–	±10.5	±12	–	V_{pk}
Equivalent Input Noise Voltage (A_V = 100, R_s = 10 k ohms, f = 1.0 kHz, BW = 1.0 Hz)	2	e_n	–	45			45	–	–	45	–	nV/(Hz)½
Common-Mode Rejection Ratio (f = 100 Hz)	3	CMRR	80	110	–	70	110	–	–	110	–	dB
Open-Loop Voltage Gain, (V_O = ± 10 V, R_L = 2.0 k ohms)	4,5,6	A_{VOL}										V/V
T_A = +25°C			100,000	200,000	–	70,000	100,000	–	25,000	100,000	–	
T_A = T_{low} to T_{high}			40,000	–	–	40,000	–	–	–	–	–	
Power Bandwidth (A_V = 1, R_L = 2.0 k ohms, THD≤5%, V_O = 20 Vp-p)	9	BW$_P$	–	40	–	–	40	–		40	–	kHz
Unity Gain Crossover Frequency (open-loop)	5	BW	–	1.0	–	–	1.0	–	–	1.0	–	MHz
Phase Margin (open-loop, unity gain)	5,7		–	70	–	–	70	–	–	70	–	degrees
Gain Margin	5,7		–	18	–	–	18	–	–	18	–	dB
Slew Rate (Unity Gain)		SR	–	2.5	–	–	2.5	–	–	2.5	–	V/μs
Output Impedance (f = 20 Hz)		z_o	–	1.0	2.0	–	1.0	2.5	–	1.0	–	kohms
Short-Circuit Output Current	8	I_{OS}	–	-17, +9.0	–	–	-17, +9.0	–	–	-17, +9.0	–	mAdc
Output Voltage Swing (R_L = 2.0 k ohms)	10	V_{OR}	±12	±13	–	+11	±12	–	±10	±12	–	V_{pk}
Power Supply Rejection Ratio												μV/V
V_{CC} = constant, R_S ≤ 10 k ohms		PSRR+		50	100	–	75	200	–	75	–	
V_{EE} = constant, R_S ≤ 10 k ohms		PSRR-		50	100	–	75	200	–	75	–	
Power Supply Current		I_{CC} I_{EE}	– –	1.0 1.0	1.5 1.5	– –	1.3 1.3	3.0 3.0	– –	1.3 1.3	4.0 4.0	mAdc
DC Quiescent Power Dissipation (V_O = 0)	11	P_D	–	30	45	–	40	90	–	40	120	mW

Note 1: T_{low}: 0° for MC1456 and MC1456C
-55°C for MC1556
T_{high}: +70°C for MC1456 and MC1456C
+125°C for MC1556

3

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted).

FIGURE 1 – INPUT COMMON-MODE SWING versus POWER SUPPLY VOLTAGE

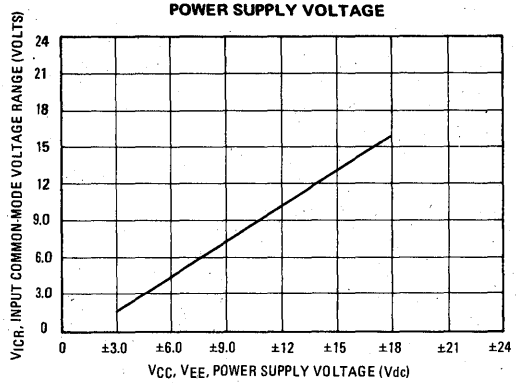


FIGURE 2 – SPECTRAL NOISE DENSITY

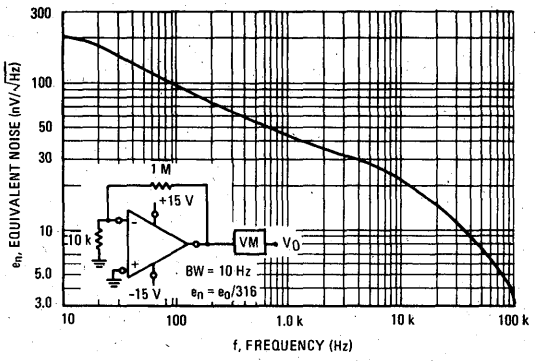


FIGURE 3 – COMMON-MODE REJECTION RATIO versus FREQUENCY

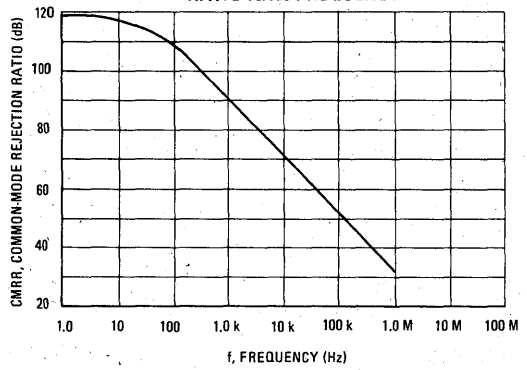


FIGURE 4 – OPEN-LOOP VOLTAGE GAIN versus TEMPERATURE

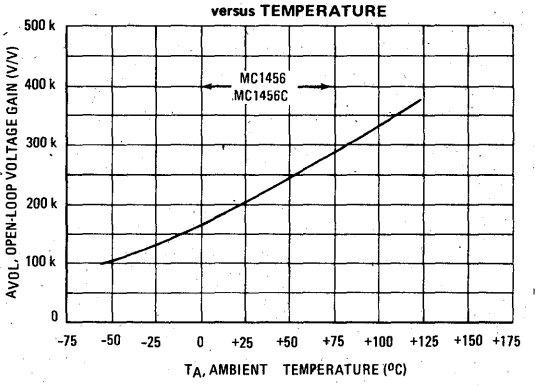


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

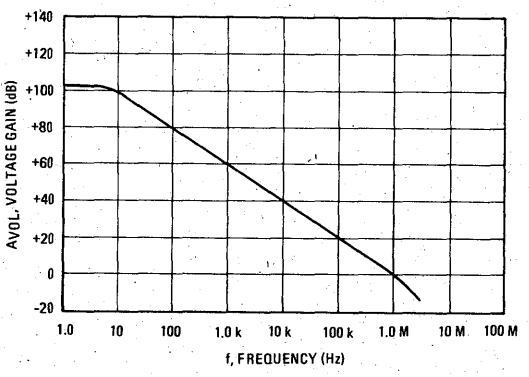
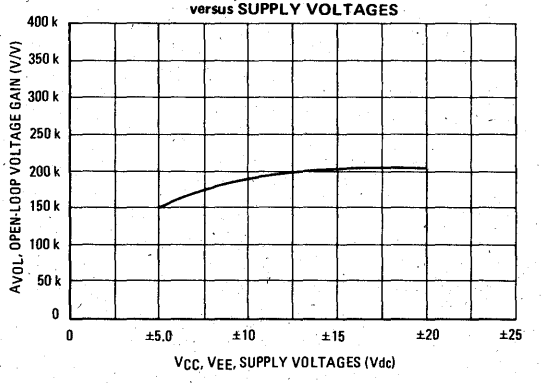


FIGURE 6 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGES



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OPEN-LOOP PHASE SHIFT

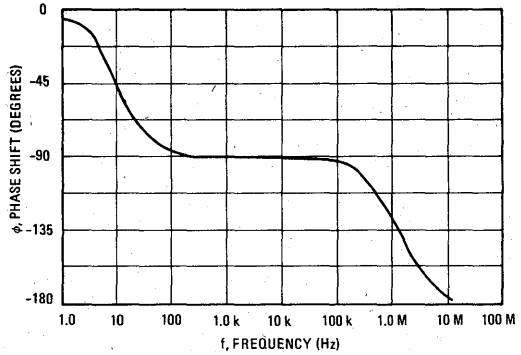


FIGURE 8 – OUTPUT SHORT-CIRCUIT CURRENT versus TEMPERATURE

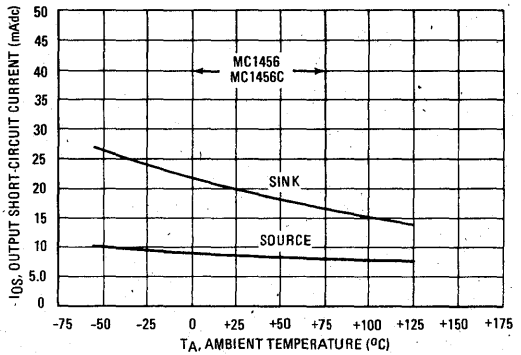


FIGURE 9 – POWER BANDWIDTH

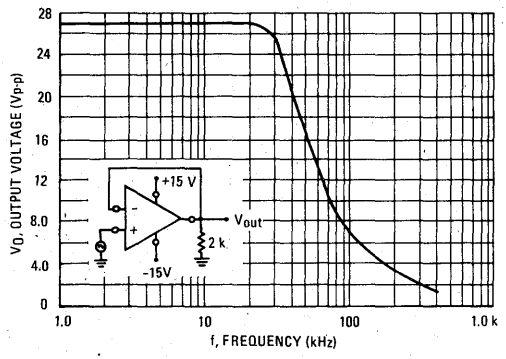


FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

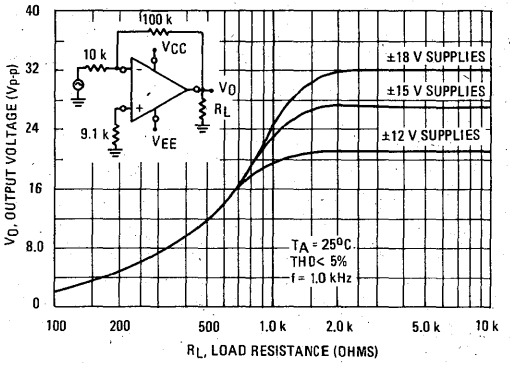
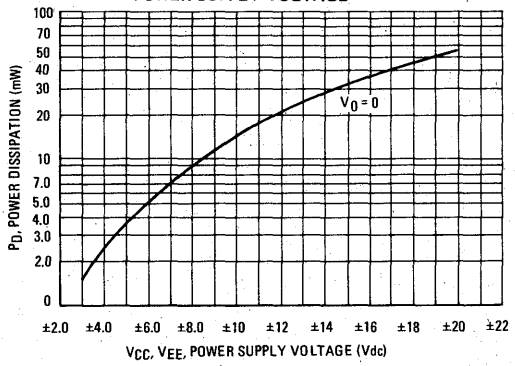


FIGURE 11 – POWER DISSIPATION versus POWER SUPPLY VOLTAGE



3

TYPICAL APPLICATIONS

Where values are not given for external components they must be selected by the designer to fit the requirements of the system.

FIGURE 12 – INVERTING FEEDBACK MODEL

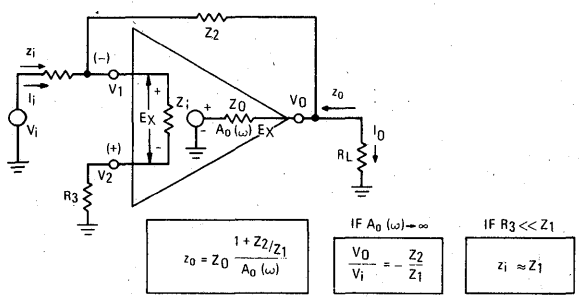


FIGURE 13 – NON-INVERTING FEEDBACK MODEL

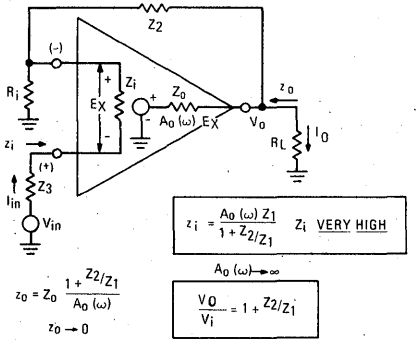


FIGURE 14 – LOW-DRIFT SAMPLE AND HOLD

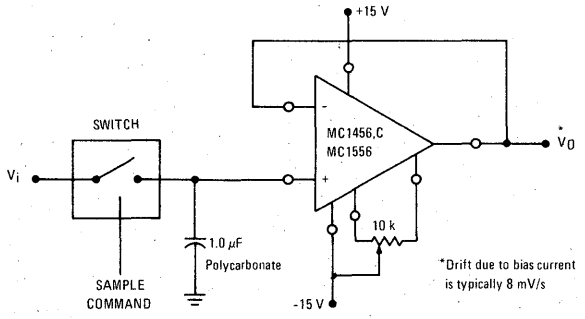
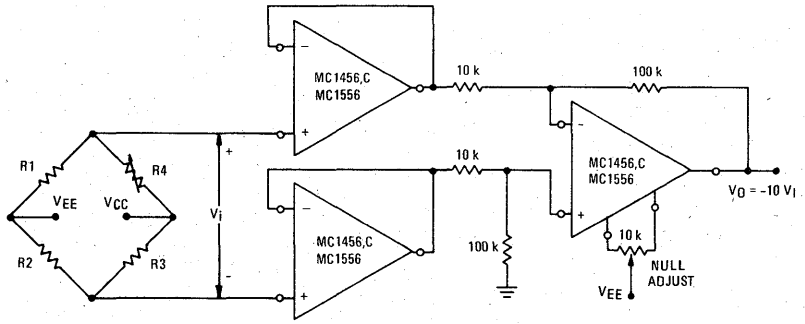


FIGURE 15 – HIGH IMPEDANCE BRIDGE AMPLIFIER



TYPICAL APPLICATIONS (continued)

FIGURE 16 – LOGARITHMIC AMPLIFIER

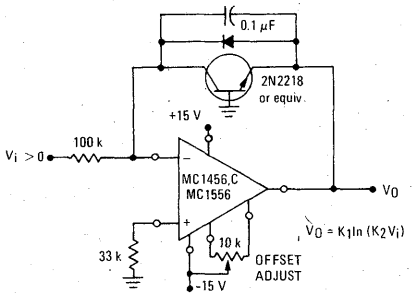
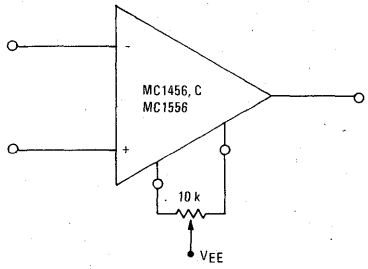
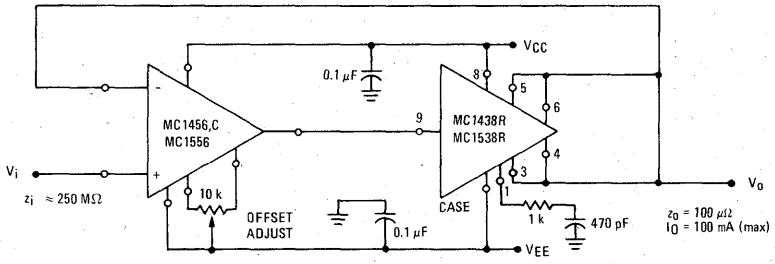


FIGURE 17 – VOLTAGE OFFSET NULL CIRCUIT



See Application Note AN-261A for further detail.

FIGURE 18 – HIGH INPUT IMPEDANCE, HIGH OUTPUT CURRENT VOLTAGE FOLLOWER



OUTLINE DIMENSIONS

ORDERING INFORMATION

Device	Temperature Range	Package
MC1458G,CG,NG	0°C to +70°C	Metal Can
MC1558G,NG	−55°C to +125°C	Metal Can
MC1458CL,CU,L, NL,NU,U	0°C to +70°C	Ceramic DIP
MC1558L,NL,NU,U	−55°C to +125°C	Ceramic DIP
MC1458CP1,CP2, NP1,NP2,P1,P2	0°C to +70°C	Plastic DIP

MC1458 MC1458N MC1458C MC1558 MC1558N

(DUAL MC1741)

DUAL OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

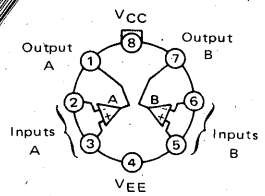
3

DUAL MC1741 INTERNALLY COMPENSATED, HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIERS

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

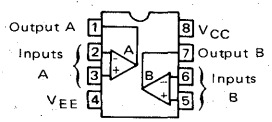
- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Low Noise Selections Offered — N Suffix

G SUFFIX
METAL PACKAGE
CASE 601

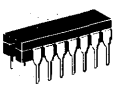


P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1458,MC1458C,MC1458N)

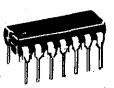
U SUFFIX
CERAMIC PACKAGE
CASE 693

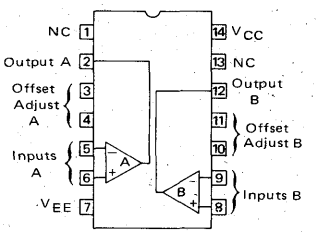


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



P2 SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1458,MC1458C,MC1458N)





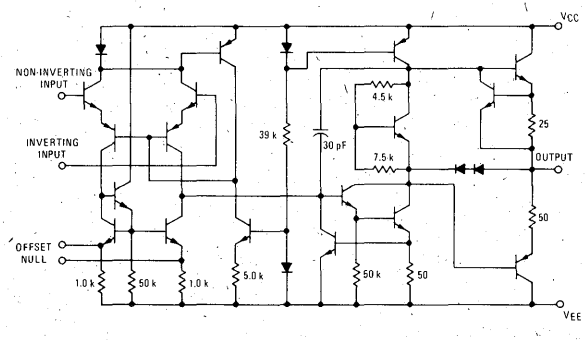
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1458	MC1558	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc Vdc
Input Differential Voltage	V_{ID}	±30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70	-55 to +125	°C
Storage Temperature Range Metal, Flat and Ceramic Packages Plastic Packages	T_{stg}	 -65 to +150 -55 to +125		°C
Junction Temperature Metal and Ceramic Package Plastic Package	T_J	 175 150		°C

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.

EQUIVALENT CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS — Note 1. (V_{CC} = 15 V, V_{EE} = 15 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}	–	1.0	5.0	–	2.0	6.0	–	2.0	10	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	–	20	300	nA
Input Bias Current	I_{IB}	–	80	500	–	80	500	–	80	700	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	–	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	–	±15	–	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	±11	±13	–	V
Large Signal Voltage Gain	A_v										V/mV
(V_O = ±10 V, R_L = 2.0 k)		50	200	–	20	200	–	–	–	–	
(V_O = ±10 V, R_L = 10 k)		–	–	–	–	–	–	20	200	–	
Output Resistance	r_o	–	75	–	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR	70	90	–	70	90	–	60	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	–	30	150	–	30	–	μV/V
Output Voltage Swing	V_O										V
($R_L \geq 10$ k)		±12	±14	–	±12	±14	–	±11	±14	–	
($R_L \geq 2$ k)		±10	±13	–	±10	±13	–	±9.0	±13	–	
Output Short-Circuit Current	I_{os}	–	20	–	–	20	–	–	20	–	mA
Supply Currents (Both Amplifiers)	I_D	–	2.3	5.0	–	2.3	5.6	–	2.3	8.0	mA
Power Consumption	P_C	–	70	150	–	70	170	–	70	240	mW
Transient Response (Unity Gain)											
(V_I = 20 mV, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	–	0.3	–	μs
(V_I = 20 mV, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Overshoot	os	–	15	–	–	15	–	–	15	–	%
(V_I = 10 V, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Slew Rate	SR	–	0.5	–	–	0.5	–	–	0.5	–	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = 15 V, T_A = *T_{high} to T_{low} unless otherwise noted).

Characteristic	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	–	–	12	mV
Input Offset Current	I_{IO}										nA
(T_A = 125°C)		–	7.0	200	–	–	–	–	–	–	
(T_A = -55°C)		–	85	500	–	–	–	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	300	–	–	400	
Input Bias Current	I_{IB}										nA
(T_A = 125°C)		–	30	500	–	–	–	–	–	–	
(T_A = -55°C)		–	300	1500	–	–	–	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	800	–	–	1000	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	–	–	–	V
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR	70	90	–	–	–	–	–	–	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	–	–	–	–	–	–	μV/V
Output Voltage Swing	V_O										V
($R_L \geq 10$ k)		±12	±14	–	±12	±14	–	–	–	–	
($R_L \geq 2$ k)		±10	±13	–	±10	±13	–	±9.0	±13	–	
Large Signal Voltage Gain	A_v										V/mV
(V_O = ±10 V, R_L = 2 k)		25	–	–	15	–	–	–	–	–	
(V_O = ±10 V, R_L = 10 k)		–	–	–	–	–	–	15	–	–	
Supply Currents (Both Amplifiers)	I_D										mA
(T_A = 125°C)		–	–	4.5	–	–	–	–	–	–	
(T_A = -55°C)		–	–	6.0	–	–	–	–	–	–	
Power Consumption (T_A = 125°C)	P_C	–	–	135	–	–	–	–	–	–	mW
(T_A = -55°C)		–	–	180	–	–	–	–	–	–	

*T_{high} = 125°C for MC1558 and 70°C for MC1458, MC1458C
T_{low} = -55°C for MC1558 and 0°C for MC1458, MC1458C

Note 1. Input pins of an unused amplifier must be grounded.

3

NOISE CHARACTERISTICS (Applies for MC1558N and MC1458N only, V_{CC} = 15 V, V_{EE} = -15 V, T_A = 25°C)

Characteristic	Symbol	MC1558N			MC1458N			Unit
		Min	Typ	Max	Min	Typ	Max	
Burst Noise (Popcorn Noise) (BW = 1.0 Hz to 1.0 kHz, t = 10 s, R_S = 100 kΩ) (Input Referenced)	E_n	–	–	20	–	–	20	μVpeak

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

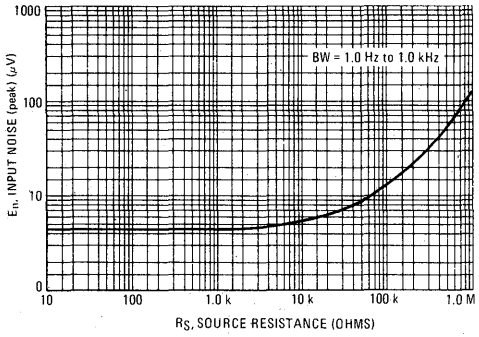


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE

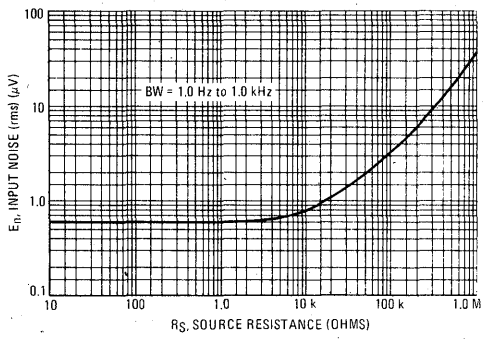


FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

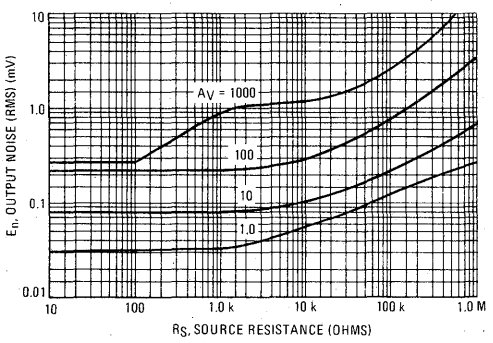


FIGURE 4 – SPECTRAL NOISE DENSITY

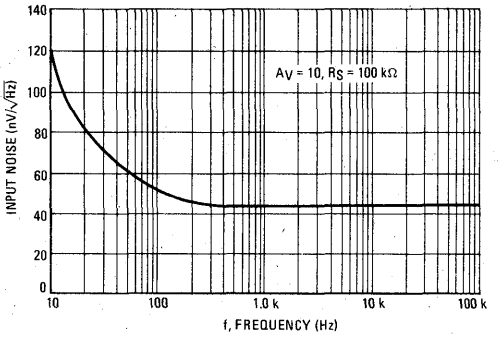
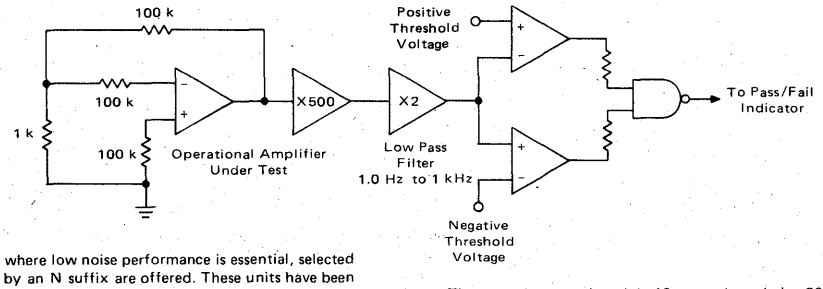


FIGURE 5 – BURST NOISE TEST CIRCUIT (N Suffixed Devices Only)



For applications where low noise performance is essential, selected devices denoted by an N suffix are offered. These units have been 100% tested for burst noise pulses on a special noise test system. Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted).

FIGURE 6 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

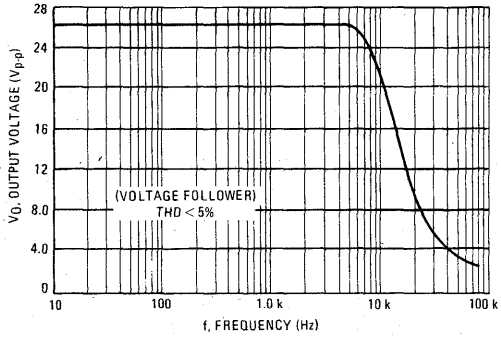


FIGURE 7 – OPEN LOOP FREQUENCY RESPONSE

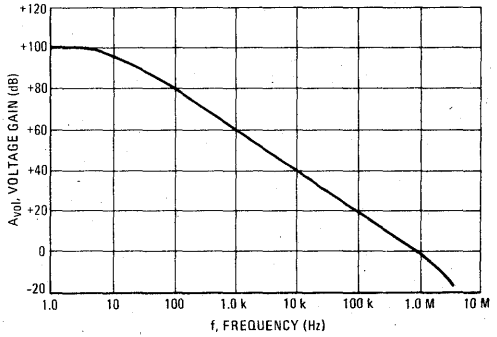


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

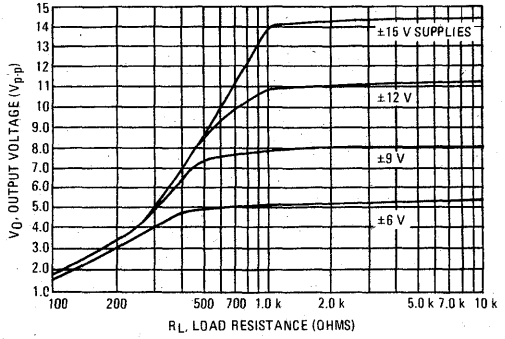


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

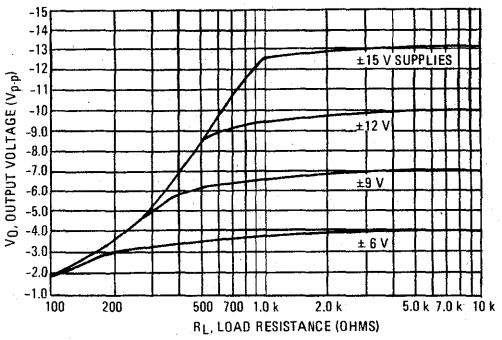


FIGURE 10 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE (Single Supply Operation)

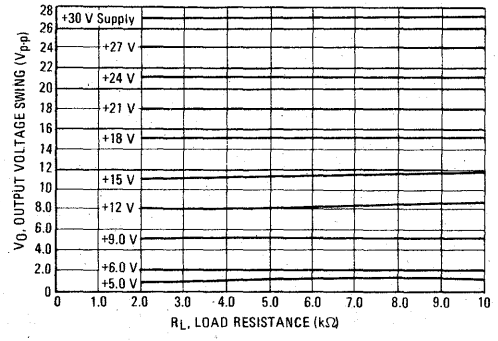


FIGURE 11 – SINGLE SUPPLY INVERTING AMPLIFIER

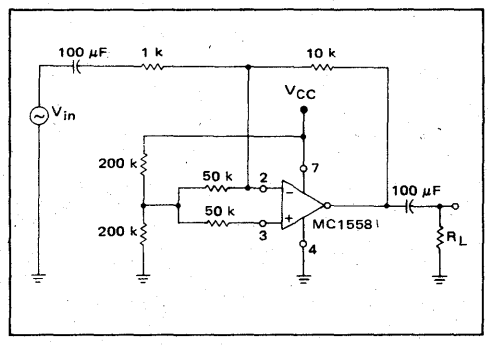


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FIGURE 12 – NON-INVERTING PULSE RESPONSE

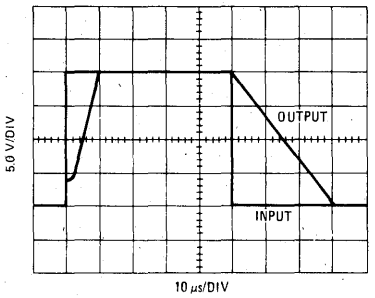


FIGURE 13 – TRANSIENT RESPONSE TEST CIRCUIT

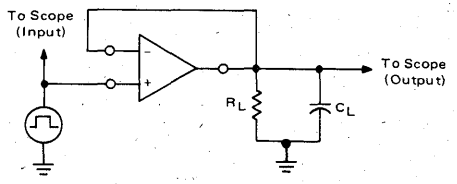
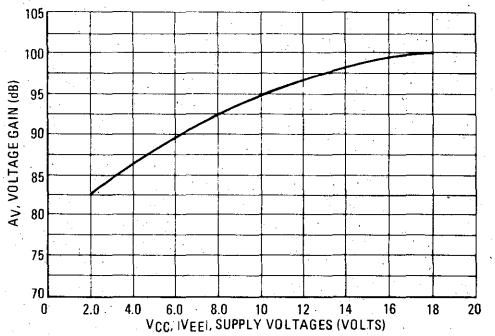


FIGURE 14 – OPEN LOOP VOLTAGE GAIN
versus SUPPLY VOLTAGE



ORDERING INFORMATION

Device	Temperature Range	Package
MC1458SG	0°C to +70°C	Metal Can
MC1458SL	0°C to +70°C	Ceramic DIP
MC1458SP1	0°C to +70°C	Plastic DIP
MC1458SP2	0°C to +70°C	Plastic DIP
MC1458SU	0°C to +70°C	Ceramic DIP
MC1558SG	−55°C to +125°C	Metal Can
MC1558SL	−55°C to +125°C	Ceramic DIP
MC1558SU	−55°C to +125°C	Ceramic DIP

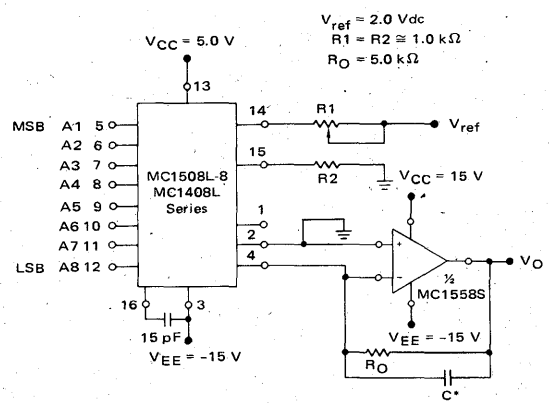
MC1458S
MC1558S

DUAL HIGH SLEW-RATE INTERNALLY-COMPENSATED OPERATIONAL AMPLIFIERS

The MC1558S is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1558 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D/A converters due to its fast settling time and high slew rate.

- High Slew Rate — 10 V/μs Guaranteed Minimum (for inverting unity gain only)
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

TYPICAL APPLICATION OF OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 μs from the time that all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

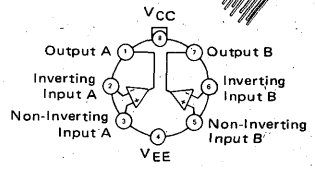
Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

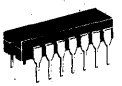
$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right] = 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

DUAL OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

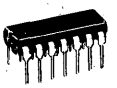
G SUFFIX
METAL PACKAGE
CASE 601

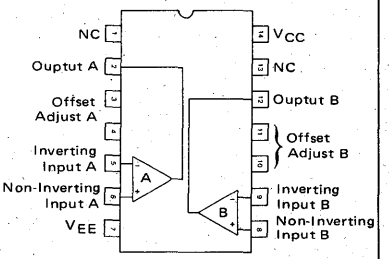




L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

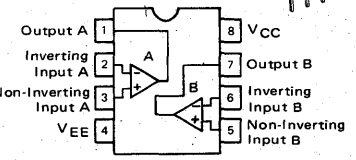
P2 SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1458S only)





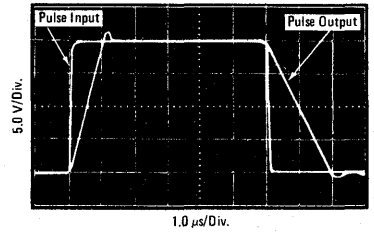
P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1458S Only)

U SUFFIX
CERAMIC PACKAGE
CASE 693

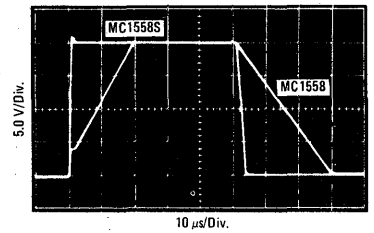


3

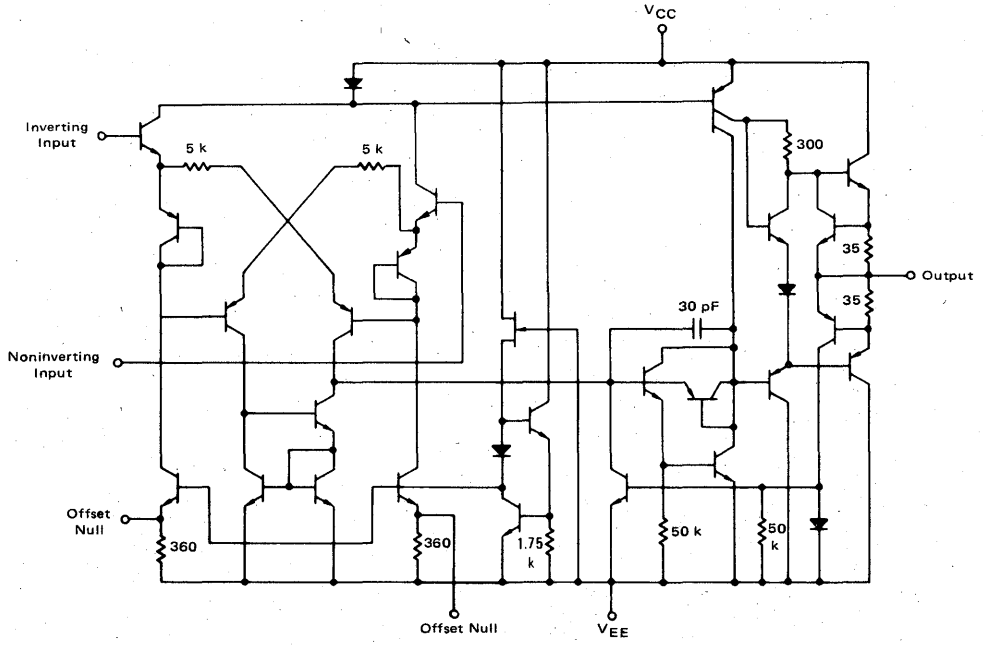
MC1558S LARGE-SIGNAL TRANSIENT RESPONSE
(Inverting Mode)



STANDARD MC1558 versus MC1558S RESPONSE COMPARISON
(Inverting Mode)



½ REPRESENTATIVE CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MC1558S	MC1458S	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Input Differential Voltage Range (1)	V_{IDR}	±30		Volts
Input Common-Mode Voltage Range (2)	V_{ICR}	±15		Volts
Output Short Circuit Duration	t_S	Continuous		
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C
Junction Temperature — Ceramic and Metal Package Plastic Package	T_J	175 150	175 150	°C °C

Note 1. For supply voltages less than ±15 Vdc, the absolute maximum input voltage is equal to the supply voltage.
Note 2. Supply voltage equal to or less than 15 Vdc.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1558S			MC1458S			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Bandwidth (See Figure 3) A_V = 1, R_L = 2.0 kΩ, THD = 5%; V_O = 20 V(p-p)	BW_P	150	200	–	150	200	–	kHz
Large-Signal Transient Response Slew Rate (Figures 10 and 11) V(-) to V(+) V(+) to V(-)	SR	10 10	20 12	– –	10 10	20 12	– –	V/μs
Settling Time (Figures 10 and 11) (to within 0.1%)	t_{setlg}	–	3.0	–	–	3.0	–	μs
Small-Signal Transient Response (Gain = 1, E_{in} = 20 mV, see Figures 7 and 8) Rise Time Fall Time Propagation Delay Time Overshoot	 t_{TLH} t_{THL} t_{PLH},t_{PHL} OS	 – – – –	 0.25 0.25 0.25 20	 – – – –	 – – – –	 0.25 0.25 0.25 20	 – – – –	 μs μs μs %
Short-Circuit Output Currents	I_{OS}	±10	–	±35	±10	–	±35	mA
Open-Loop Voltage Gain (R_L = 2.0 kΩ) (See Figure 4) V_O = ±10 V	A_{vol}	50,000	200,000	–	20,000	100,000	–	–
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	z_i	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Swing R_L = 10 kΩ R_L = 2.0 kΩ	V_O	±12 ±10	±14 ±13	– –	±12 ±10	±14 ±13	– –	V_{pk}
Input Common-Mode Voltage Swing	V_{ICR}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz)	CMRR	70	90	–	70	90	–	dB
Input Bias Current (See Figure 2)	I_{IB}	–	200	500	–	200	500	nA
Input Offset Current	$\|I_{IO}\|$	–	30	200	–	30	200	nA
Input Offset Voltage (R_S = ⩽10 kΩ)	$\|V_{IO}\|$	–	1.0	5.0	–	2.0	6.0	mV
DC Power Consumption (See Figure 9) (Power Supply = ±15 V, V_O = 0)	P_C	–	70	150	–	70	170	mW
Positive Voltage Supply Sensitivity (V_{EE} constant)	PSS+	–	2.0	150	–	2.0	150	μV/V
Negative Voltage Supply Sensitivity (V_{CC} constant)	PSS-	–	10	150	–	10	150	μV/V

**Plastic package offered in limited temperature range device only.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 Vdc, V_{EE} = -15 Vdc, T_A = -55 to +125°C for MC1558S and T_A = 0 to 70°C for MC1458S, unless otherwise noted.)

Characteristic	Symbol	MC1558S			MC1458S			Unit
		Min	Typ	Max	Min	Typ	Max	
Open Loop Voltage Gain V_O = ±10 V	A_{VOL}	25,000	–	–	15,000	–	–	V/V
Output Voltage Swing R_L = 10 kΩ R_L = 2 kΩ	V_O	±12 ±10	– –	– –	±12 ±10	– –	– –	V_{pk}
Input Common-Mode Voltage Range	V_{ICR}	±12	–	–	–	–	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz)	CMRR	70	–	–	–	–	–	dB
Input Bias Current T_A = 125°C T_A = -55°C T_A = 0 to 70°C	I_{IB}	– – –	200 500 –	500 1500 –	– – –	– – –	– – 800	nA
Input Offset Current T_A = 125°C T_A = -55°C T_A = 0 to 70°C	I_{IO}	– – –	30 – –	200 500 –	– – –	– – –	– – 300	nA
Input Offset Voltage R_S ⩽ 10 kΩ	V_{IO}	–	–	6.0	–	–	7.5	mV
DC Power Consumption V_O = 0 V	P_C	–	–	200	–	–	–	mW
Positive Power Supply Sensitivity V_{EE} ⩽ -15 V	P_{SS+}	–	–	150	–	–	–	μV/V
Negative Power Supply Sensitivity V_{CC} = 15 V	P_{SS-}	–	–	150	–	–	–	μV/V

3

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 1 – OFFSET ADJUST CIRCUIT

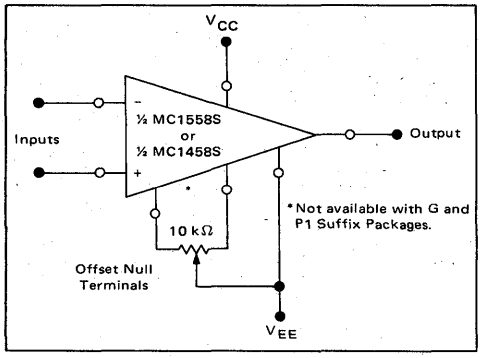


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE

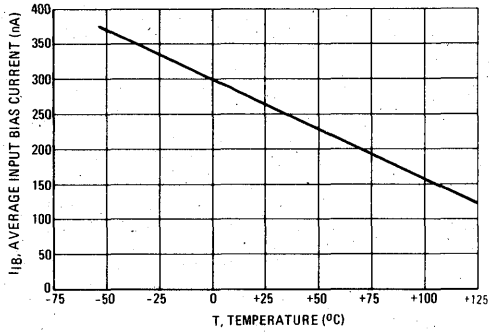


FIGURE 3 – POWER BANDWIDTH – NONDISTORTED OUTPUT VOLTAGE versus FREQUENCY

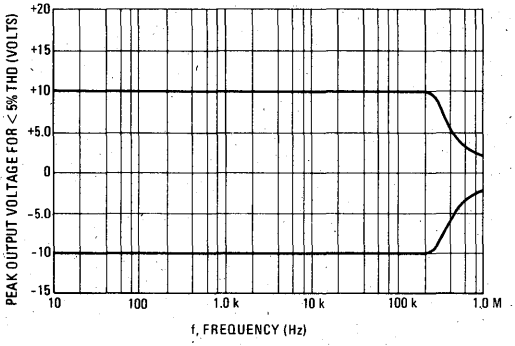


FIGURE 4 – OPEN-LOOP FREQUENCY RESPONSE

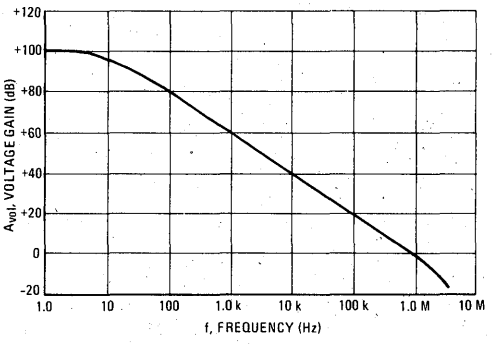
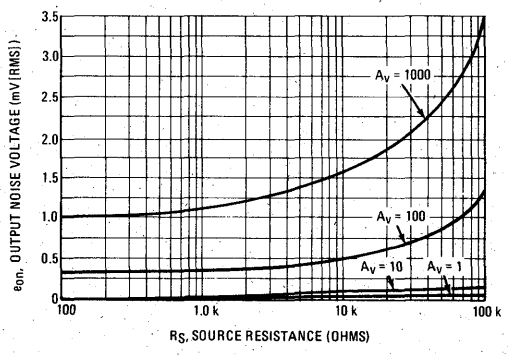


FIGURE 5 – OUTPUT NOISE versus SOURCE RESISTANCE



TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 6 — SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS

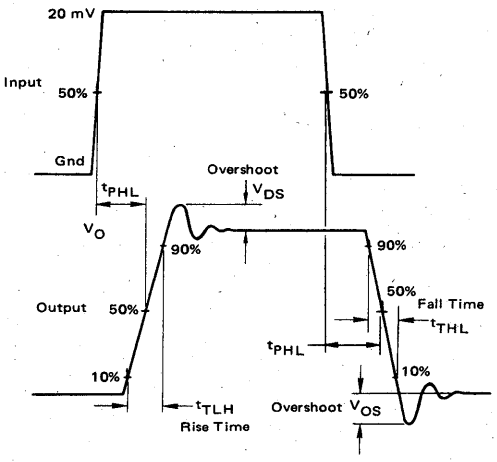


FIGURE 7 — SMALL-SIGNAL TRANSIENT RESPONSE

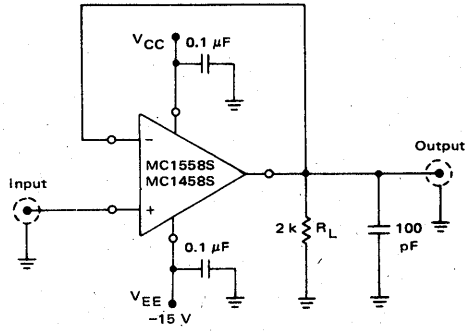


FIGURE 8 — POWER CONSUMPTION versus POWER SUPPLY VOLTAGES

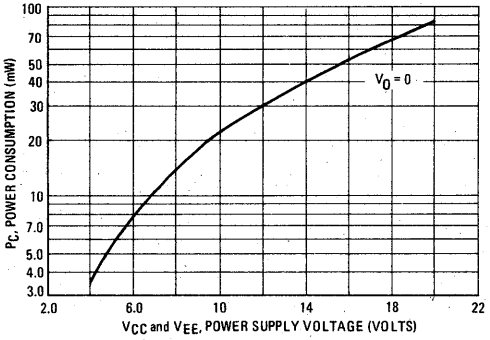


FIGURE 9 — LARGE-SIGNAL TRANSIENT WAVEFORMS

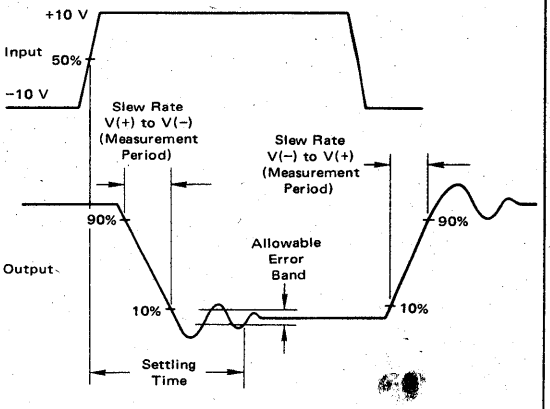
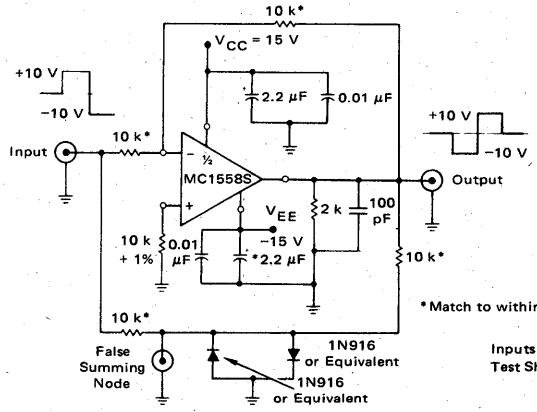


FIGURE 10 — SLEW RATE AND SETTLING TIME TEST CIRCUIT*



*Match to within 0.01%.

Inputs of Amplifier Not Under Test Should Be Grounded.

3

SETTLING TIME

In order to properly utilize the high slew rate and fast settling time of an operational amplifier, a number of system considerations must be observed. Capacitance at the summing node and at the amplifier output must be minimal and circuit board layout should be consistent with common high-frequency considerations. Both power supply connections should be adequately bypassed as close as possible to the device pins. In bypassing, both low and high-frequency components should be considered to avoid the possibility of excessive ringing. In order to achieve optimum damping, the selection of a capacitor in parallel with the feedback resistor may be necessary. A value too small could result in excessive ringing while a value too large will degrade slew rate and settling time.

SETTLING TIME MEASUREMENT

In order to accurately measure the settling time of an operational amplifier, it is suggested that the "false" summing junction approach be taken as shown in Figure 11. This is necessary since it is difficult to determine when the waveform at the output of the operational amplifier settles to within 0.1% of it's final value. Because the output and input voltages are effectively subtracted from each other at the amplifier inverting input, this seems like an ideal node for the measurement. However, the probe capacitance at this critical node can greatly affect the accuracy of the actual measurement.

The solution to these problems is the creation of a second or "false" summing node. The addition of two diodes at this node clamps the error voltage to limit the voltage excursion to the oscilloscope. Because of the voltage divider effect, only one-half of the actual error appears at this node. For extremely critical measurements, the capacitance of the diodes and the oscilloscope, and the settling time of the oscilloscope must be considered. The expression

$$t_{setlg} = \sqrt{x^2 + y^2 + z^2}$$

can be used to determine the actual amplifier settling time, where

t_{setlg} = observed settling time

x = amplifier settling time (to be determined)

y = false summing junction settling time

z = oscilloscope settling time

It should be remembered that to settle within ±0.1% requires 7RC time constants.

The ±0.1% factor was chosen for the MC1558S settling time as it is compatible with the ±1/2 LSB accuracy of the MC1508L-8 digital-to-analog converter. This D-to-A converter features ±0.19% maximum error.

FIGURE 11 – WAVEFORM AT FALSE SUMMING NODE

(Inverting Mode)

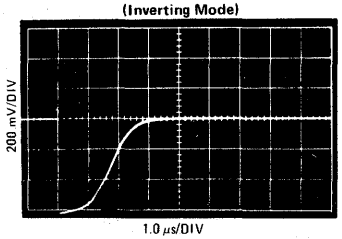
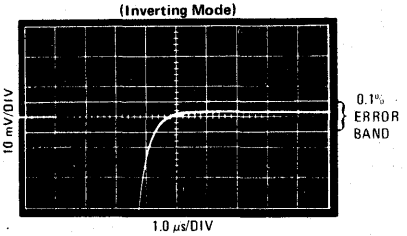


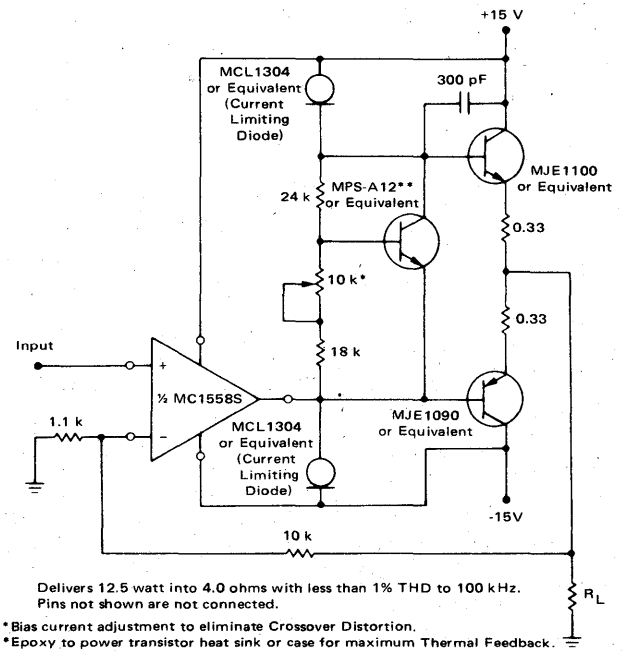
FIGURE 12 – EXPANDED WAVEFORM AT FALSE SUMMING NODE

(Inverting Mode)



TYPICAL APPLICATION

FIGURE 13 – 12.5-WATT WIDEBAND POWER AMPLIFIER



Delivers 12.5 watt into 4.0 ohms with less than 1% THD to 100 kHz.
Pins not shown are not connected.

*Bias current adjustment to eliminate Crossover Distortion.

**Epoxy to power transistor heat sink or case for maximum Thermal Feedback.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1709CF	0°C to +70°C	Ceramic Flat
MC1709CG	0°C to +70°C	Metal Can
MC1709CL,CU	0°C to +70°C	Ceramic DIP
MC1709CP1,CP2	0°C to +70°C	Plastic DIP
MC1709F,AF	−55°C to +125°C	Ceramic Flat
MC1709G,AG	−55°C to +125°C	Metal Can
MC1709L,AL,U	−55°C to +125°C	Ceramic DIP

MC1709
MC1709A
MC1709C

OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- High-Performance Open Loop Gain Characteristics
  A_{VOL} = 45,000 typical
- Low Temperature Drift − ±3.0 μV/°C typical (MC1709)
- Large Output Voltage Swing − ±14 V typical @ ±15 V Supply
- Low Output Impedance − z_o = 150 ohms typical

OPERATIONAL AMPLIFIER

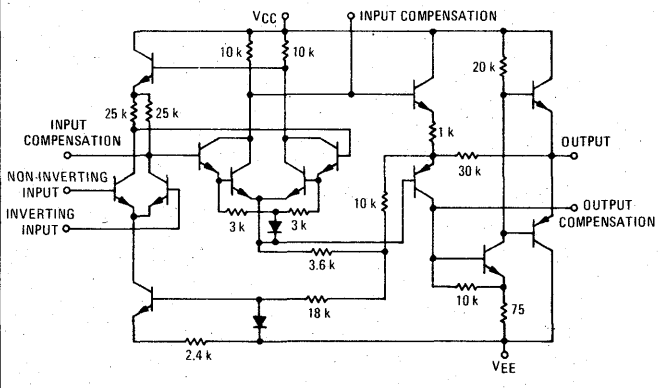
SILICON MONOLITHIC INTEGRATED CIRCUIT

3

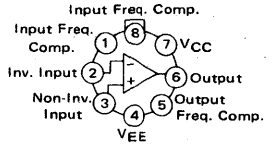
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC} V_{EE}	+18 -18	Vdc
Input Differential Voltage Range		V_{IDR}	±5.0	Volts
Input Common-Mode Range		V_{ICR}	±10	Volts
Output Load Current		I_L	10	mA
Output Short-Circuit Duration		t_S	5.0	s
Power Dissipation (Package Limitation)		P_D		
Metal Can			680	mW
Derate above T_A = +25°C			4.6	mW/°C
Flat Package			500	mW
Derate above T_A = +25°C			3.3	mW/°C
Plastic Dual In-Line Packages (MC1709C only)			625	mW
Derate above T_A = +25°C			5.0	mW/°C
Ceramic Dual In-Line Package			750	mW
Derate above T_A = +25°C			6.0	mW/°C
Operating Ambient Temperature Range	MC1709A, MC1709	T_A	-55 to +125	°C
	MC1709C		0 to +70	
Storage Temperature Range		T_{stg}		°C
Metal and Ceramic Packages			-65 to +150	
Plastic Packages			-55 to +125	

FIGURE 1 − EQUIVALENT CIRCUIT SCHEMATIC

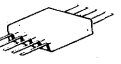


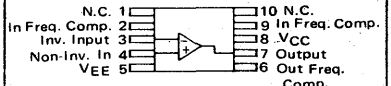
PIN CONNECTIONS



G SUFFIX
METAL PACKAGE
CASE 601

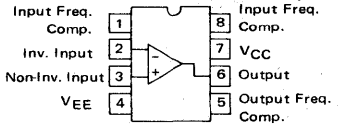
F SUFFIX
CERAMIC PACKAGE
CASE 606-04
TO-91



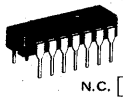


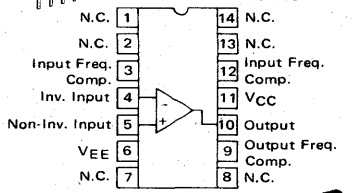
P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1709C only)

U SUFFIX
CERAMIC PACKAGE
CASE 693



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
TO-116





P2 SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1709C only)

ELECTRICAL CHARACTERISTICS (unless otherwise noted, 9.0 V ≤ V_{CC} ≤ 15 V, -9.0 V ≥ V_{EE} ≥ -15 V, T_A = 25°C)

Characteristic	Symbol	MC1709A			MC1709			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}	–	0.6	2.0	–	1.0	5.0	mV
Input Offset Current	I_{IO}	–	10	50	–	50	200	nA
Input Bias Current	I_{IB}	–	100	200	–	200	500	nA
Input Resistance	r_i	350	700	–	150	400	–	kΩ
Output Resistance	r_o	–	150	–	–	150	–	Ω
Power Supply Currents (V_{CC} = 15 V, V_{EE} = -15 V)	I_{CC}, I_{EE}	–	2.5	3.6	–	–	–	mA
Power Consumption (V_{CC} = 15 V, V_{EE} = -15 V)	P_C	–	75	108	–	80	165	mW
Transient Response (V_{CC} = 15 V, V_{EE} = -15 V) See Figure 8								
Risetime	t_{TLH}	–	–	1.5	–	0.3	1.0	μs
Overshoot	OS	–	–	30	–	10	30	%

ELECTRICAL CHARACTERISTICS (unless otherwise noted, 9.0 V ≤ V_{CC} ≤ 15 V, -9.0 V ≥ V_{EE} ≥ -15 V, T_A = -55°C to +125°C)

Characteristic	Symbol	MC1709A			MC1709			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}	–	–	3.0	–	–	6.0	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$							μV/°C
(R_S = 50 Ω, T_A = 25°C to 125°C)		–	1.8	10	–	–	–	
(R_S = 50 Ω, T_A = -55°C to 25°C)		–	1.8	10	–	–	–	
(R_S = 50 Ω, T_A = -55°C to 125°C)		–	–	–	–	3.0	–	
(R_S = 10 kΩ, T_A = 25°C to 125°C)		–	2.0	15	–	–	–	
(R_S = 10 kΩ, T_A = -55°C to 25°C)		–	4.8	25	–	–	–	
(R_S = 10 kΩ, T_A = -55°C to 125°C)		–	–	–	–	6.0	–	
Input Offset Current	I_{IO}							nA
(T_A = -55°C)		–	40	250	–	100	500	
(T_A = 125°C)		–	3.5	50	–	20	200	
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$							nA/°C
(T_A = -55°C to 25°C)		–	0.45	2.8	–	–	–	
(T_A = 25°C to 125°C)		–	0.08	0.5	–	–	–	
Input Bias Current (T_A = -55°C)	I_{IB}	–	300	600	–	500	1500	nA
Input Resistance (T_A = -55°C)	r_i	85	170	–	40	100	–	kΩ
Input Common-Mode Voltage Range (V_{CC} = 15 V, V_{EE} = -15 V)	V_{ICR}	±8.0	±10	–	±8.0	±10	–	V
Common Mode Rejection Ratio (R_S ≤ 10 kΩ)	CMRR	80	110	–	70	90	–	dB
Supply Voltage Rejection Ratio (V_{CC} = 15 V, V_{EE} = -15 V, R_S ≤ 10 kΩ)	PSRR	–	40	100	–	25	150	μV/V
Large Signal Voltage Gain (V_{CC} = 15 V, V_{EE} = -15 V, R_L ≥ 2.0 kΩ, V_O = ±15 V)	A_V	25	45	70	25	45	70	V/mV
Output Voltage Range (V_{CC} = 15 V, V_{EE} = -15 V)	V_{OR}							V
(R_L ≥ 10 kΩ)		±12	±14	–	±12	±14	–	
(R_L ≥ 2.0 kΩ)		±10	±13	–	±10	±13	–	
Power Supply Currents (V_{CC} = 15 V, V_{EE} = -15 V)	I_{CC}/I_{EE}							mA
(T_A = -55°C)		–	2.7	4.5	–	–	–	
(T_A = 125°C)		–	2.1	3.0	–	–	–	
Power Consumption (V_{CC} = 15, V_{EE} = -15 V)	P_C							mW
(T_A = -55°C)		–	81	135	–	–	–	
(T_A = 125°C)		–	63	90	–	–	–	

ELECTRICAL CHARACTERISTICS (unless otherwise noted, V_{CC} = 15 V, V_{EE} = -15 V, T_A = 25°C)

Characteristic	Symbol	MC1709C			Unit
		Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ, 9.0 V ≤ 15 V, -9.0 V ≥ V_{EE} ≥ -15 V)	V_{IO}	–	2.0	7.5	mV
Input Offset Current	I_{IO}	–	100	500	nA
Input Bias Current	I_{IB}	–	300	1500	nA
Input Resistance	r_i	50	250	–	kΩ
Output Resistance	r_o	–	150	–	Ω
Power Consumption	P_C	–	80	200	mW
Large Signal Voltage Gain ($R_L \geq 2.0$ kΩ, V_O = ±10 V)	A_V	15	45	–	V/mV
Output Voltage Range ($R_L \geq 10$ kΩ) ($R_L \geq 2.0$ kΩ)	V_{OR}	 ±12 ±10	 ±14 ±13	 – –	V
Input Common-Mode Voltage Range	V_{ICR}	±8.0	±10	–	V
Common Mode Rejection Ratio ($R_S \leq 10$ kΩ)	CMRR	65	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ kΩ)	PSRR	–	25	200	μV/V
Transient Response See Figure 8 Rise Time Overshoot	 T_{TLH} OS	 – –	 0.3 10	 – –	 μs %

ELECTRICAL CHARACTERISTICS (unless otherwise specified, V_{CC} = 15 V, V_{EE} = -15 V, T_A = 0°C to 70°C)

Parameter	Symbol	MC1709C			Unit
		Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ, 9.0 V ≤ V_{CC} ≤ 15 V, -9.0 V ≥ V_{EE} ≥ 15 V)	V_{IO}	–	–	10	mV
Input Offset Current	I_{IO}	–	–	750	nA
Input Bias Current	I_{IB}	–	–	2.0	μA
Large Signal Voltage Gain ($R_L \geq 2.0$ kΩ, V_O = ±10 V)	A_V	12	–	–	V/mV
Input Resistance	ri	35	–	–	kΩ

TYPICAL CHARACTERISTICS

FIGURE 2 – TEST CIRCUIT
(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C)

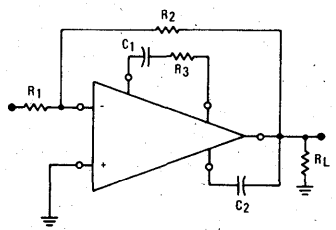


Fig. No.	Curve No.	Test Conditions				
		R_1(Ω)	R_2(Ω)	R_3(Ω)	C_1(pF)	C_2(pF)
3	1	10 k	10 k	1.5 k	5.0 k	200
	2	10 k	100 k	1.5 k	500	20
	3	10 k	1.0 M	1.5 k	100	3.0
	4	1.0 k	1.0 M	0	10	3.0
4	1	1.0 k	1.0 M	0	10	3.0
	2	10 k	1.0 M	1.5 k	100	3.0
	3	10 k	100 k	1.5 k	500	20
	4	10 k	10 k	1.5 k	5.0 k	200
5	1	0	∞	1.5 k	5.0 k	200
	2	0	∞	1.5 k	500	20
	3	0	∞	1.5 k	100	3.0
	4	0	∞	0	10	3.0

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FIGURE 3 – LARGE SIGNAL SWING versus FREQUENCY

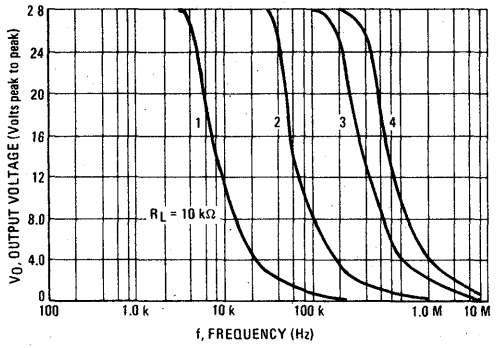


FIGURE 4 – CLOSED LOOP VOLTAGE GAIN versus FREQUENCY

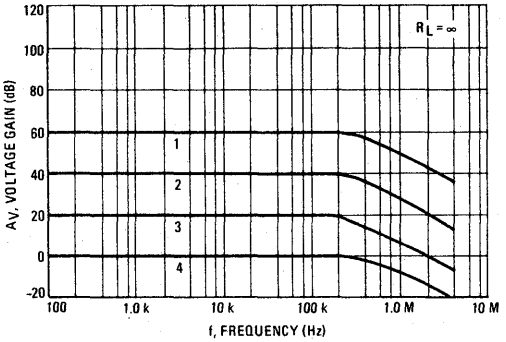


FIGURE 5 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

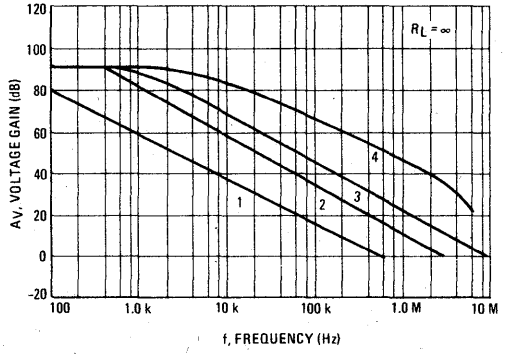


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

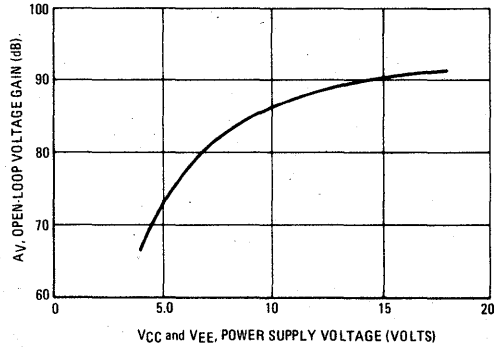


FIGURE 7 – SLEW RATE versus CLOSED LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS

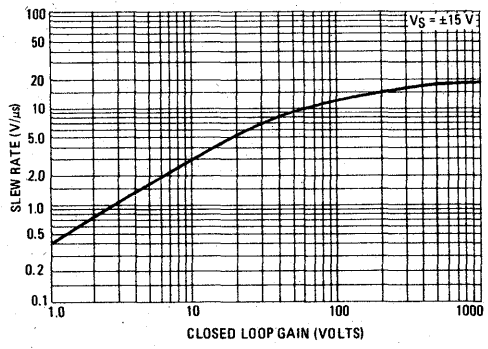
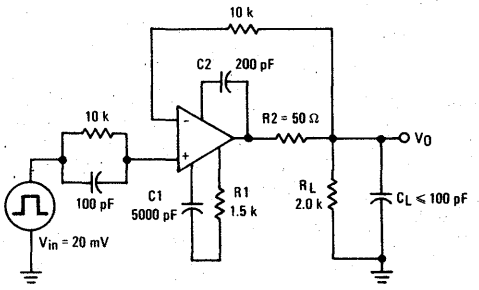


FIGURE 8 – TRANSIENT RESPONSE TEST CIRCUIT



ORDERING INFORMATION

Device	Temperature Range	Package
MC1712F	−55°C to +125°C	Ceramic Flat
MC1712G	−55°C to +125°C	Metal Can
MC1712L	−55°C to +125°C	Ceramic DIP
MC1712CF	0°C to +70°C	Ceramic Flat
MC1712CG	0°C to +70°C	Metal Can
MC1712CL	0°C to +70°C	Ceramic DIP
MC1712CP	0°C to +70°C	Plastic DIP

MC1712
MC1712C

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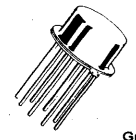
WIDEBAND DC AMPLIFIER

. . . designed for use as an operational amplifier utilizing operating characteristics as a function of the external feedback components.

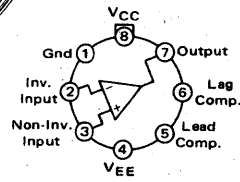
- Open Loop Gain A_{VOL} = 3600 typical
- Low Temperature Drift – ±2.5 μV/°C
- Output Voltage Swing – ±5.3 V typical @ +12 V and -6 V Supplies
- Low Output Impedance – z_o = 200 ohms typical

WIDEBAND DC AMPLIFIER

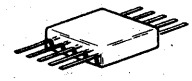
SILICON MONOLITHIC INTEGRATED CIRCUIT

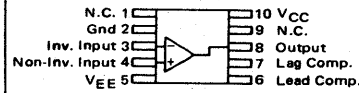


G SUFFIX
METAL PACKAGE
CASE 601

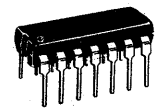


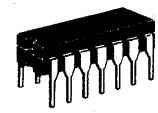
F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



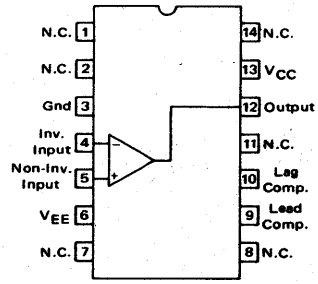


P SUFFIX
PLASTIC PACKAGE
CASE 646





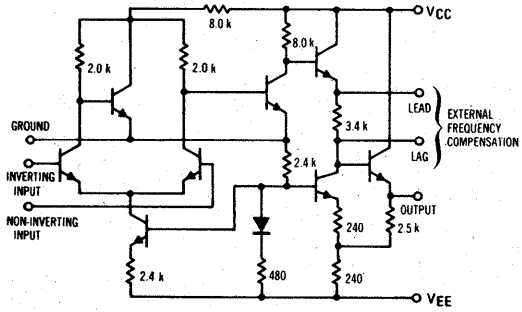
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage (Total between V_{CC} and V_{EE} terminals)	$\|V_{CC}\| + \|V_{EE}\|$	21	Vdc
Input Differential Voltage Range	V_I	±5.0	Volts
Input Common Mode Range	V_{ICR}	+1.5 -6.0	Volts
Peak Load Current	I_L	50	mA
Power Dissipation (Package Limitation)	P_D		
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Flat Ceramic Package		500	mW
Derate above T_A = +25°C		3.3	mW/°C
Dual In-Line Ceramic Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Ambient Temperature Range MC1712	T_A	-55 to +125	°C
MC1712C		0 to +75	
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



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MC1712 ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	V_{CC} = 12 V, V_{EE} = -6.0 V			V_{CC} = 6.0 V, V_{EE} = -3.0 V			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 2$ kΩ)	V_{IO}	–	0.5	2.0	–	0.7	3.0	mV
Input Offset Current	I_{IO}	–	180	500	–	120	500	nA
Input Bias Current	I_{IB}	–	2.0	5.0	–	1.2	3.5	μA
Input Resistance	r_i	16	40	–	22	67	–	kΩ
Input Voltage Range	V_I	-4.0	–	+0.5	-1.5	–	+0.5	V
Common Mode Rejection Ratio ($R_S \leq 2$ kΩ, f ≤ 1 kHz)	CMRR	80	100	–	80	100	–	dB
Large Signal Voltage Gain ($R_L \geq 100$ kΩ, V_{out} = ±5.0 V) ($R_L \geq 100$ kΩ, V_{out} = ±2.5 V)	A_{VOL}	2000 –	3600 –	6000 –	– 600	– 900	– 1500	
Output Resistance	r_o	–	200	500	–	300	700	Ω
Supply Current (V_{out} = 0)	I_D	–	5.0	6.7	–	2.1	3.3	mA
Power Consumption (V_{out} = 0)	P_C	–	90	120	–	19	30	mW
Transient Response (Unity-Gain) ($C1 = 0.01$ μF, $R1 = 20$ Ω, $R_L \leq 100$ kΩ, $V_{in} = 10$ mV, $C_L \leq 100$ pF) Rise Time Overshoot	 t_{TLH} OS	 – –	 25 10	 120 50	 – –	 – –	 – –	 ns %
Transient Response (x100 Gain) ($C3 = 50$ pF, $R_L \geq 100$ kΩ, $V_{in} = 1$ mV) Rise Time Overshoot	 t_{TLH} OS	 – –	 10 20	 30 40	 – –	 – –	 – –	 ns %

The following specifications apply for -55°C ≤ T_A ≤ +125°C:

Input Offset Voltage ($R_S \leq 2$ kΩ)	V_{IO}	–	–	3.0	–	–	4.0	mV
Average Temperature Coefficient of Input Offset Voltage ($R_S = 50$ Ω, T_A = 25°C to 125°C) ($R_S = 50$ Ω, T_A = 25°C to -55°C)	$\Delta V_{IO}/\Delta T$	– –	2.5 2.0	10 10	– –	3.5 3.0	15 15	μV/°C μV/°C
Input Offset Current (T_A = +125°C) (T_A = -55°C)	I_{IO}	– –	80 400	500 1500	– –	50 280	500 1500	nA nA
Average Temperature Coefficient of Input Offset Current (T_A = 25°C to +125°C) (T_A = 25°C to -55°C)	$\Delta I_{IO}/\Delta T$	– –	1.0 3.0	5.0 16	– –	0.7 20	4.0 13	nA/°C nA/°C
Input Bias Current (T_A = -55°C)	I_{IB}	–	4.3	10	–	2.6	7.5	μA
Input Resistance	r_i	6.0	–	–	8.0	–	–	kΩ
Common Mode Rejection Ratio ($R_S \leq 2$ kΩ, f ≤ 1 kHz)	CMRR	70	95	–	70	95	–	dB
Supply Voltage Rejection Ratio (V_{CC} = 12 V, V_{EE} = -6.0 V to V_{CC} = 6.0 V, V_{EE} = -3.0 V, $R_S \leq 2$ kΩ)	PSRR	–	75	200	–	75	200	μV/V
Large Signal Voltage Gain ($R_L \geq 100$ kΩ, V_{out} = ±5.0 V) ($R_L \geq 100$ kΩ, V_{out} = ±2.5 V)	A_{VOL}	2000 –	– –	7000 –	– 500	– –	– 1750	
Output Voltage Swing ($R_L \geq 100$ kΩ) ($R_L \geq 10$ kΩ)	V_O	±5.0 ±3.5	±5.3 ±4.0	– –	±2.5 ±1.5	±2.7 ±2.0	– –	V V
Supply Current (T_A = +125°C, V_{out} = 0) (T_A = -55°C, V_{out} = 0)	I_D	– –	4.4 5.0	6.7 7.5	– –	1.7 2.1	3.3 3.9	mA mA
Power Consumption (T_A = +125°C, V_{out} = 0) (T_A = -55°C, V_{out} = 0)	P_C	– –	80 90	120 135	– –	15 19	30 35	mW mW

MC1712C ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	V_{CC} = 12 V, V_{EE} = -6.0 V			V_{CC} = 6.0 V, V_{EE} = -3.0 V			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 2$ kΩ)	V_{IO}	–	1.5	5.0	–	1.7	6.0	mV
Input Offset Current	I_{IO}	–	0.5	2.0	–	0.3	2.0	μA
Input Bias Current	I_{IB}	–	2.5	7.5	–	1.5	5.0	μA
Input Resistance	r_i	10	32	–	16	55	–	kΩ
Input Voltage Range	V_I	-4.0	–	+0.5	-1.5	–	+0.5	V
Common Mode Rejection Ratio ($R_S \leq 2$ kΩ, $f \leq 1$ kHz)	CMRR	70	92	–	70	92	–	dB
Large Signal Voltage Gain ($R_L \geq 100$ kΩ, V_{out} = ±5.0 V) ($R_L \geq 100$ kΩ, V_{out} = ±2.5 V)	A_{VOL}	2000 –	3400 –	6000 –	– 500	– 800	– 1500	
Output Resistance	r_o	–	200	600	–	300	800	Ω
Supply Current (V_{out} = 0)	I_D	–	5.0	6.7	–	2.1	3.3	mA
Power Consumption (V_{out} = 0)	P_C	–	90	120	–	19	30	mW
Transient Response (Unity-Gain) ($C1 = 0.01$ μF, $R_I = 20$ Ω, $R_L \leq 100$ kΩ, $V_{in} = 10$ mV, $C_L \leq 100$ pF) Rise Time Overshoot	 t_{TLH} OS	 – –	 25 10	 120 50	 – –	 – –	 – –	 ns %
Transient Response (x100 Gain) ($C3 = 50$ pF, $R_L \geq 100$ kΩ, $V_{in} = 1$ mV) Rise Time Overshoot	 t_{TLH} OS	 – –	 10 20	 30 40	 – –	 – –	 – –	 ns %

The following specifications apply for 0°C ≤ T_A ≤ +70°C:

Input Offset Voltage ($R_S \leq 2$ kΩ)	V_{IO}	–	–	6.5	–	–	7.5	mV
Average Temperature Coefficient of Input Offset Voltage ($R_S = 50$ Ω, T_A = +70°C to 0°C)	$\Delta V_{IO}/\Delta T$	–	5.0	20	–	7.5	25	μV/°C
Input Offset Current	I_{IO}	–	–	2.5	–	–	2.5	μA
Average Temperature Coefficient of Input Offset Current (T_A = 25°C to +70°C) (T_A = 25°C to 0°C)	$\Delta I_{IO}/\Delta T$	 – –	 4.0 6.0	 10 20	 – –	 3.0 5.5	 8.0 18	 nA/°C nA/°C
Input Bias Current (T_A = 0°C)	I_{IB}	–	4.0	12	–	2.7	8	μA
Input Resistance	r_i	6.0	18	–	9.0	27	–	kΩ
Common Mode Rejection Ratio ($R_S \leq 2$ kΩ, $f \leq 1$ kHz)	CMRR	6.5	86	–	65	86	–	dB
Supply Voltage Rejection Ratio (V_{CC} = 12 V, V_{EE} = -6.0 V to V_{CC} = 6.0 V, V_{EE} = -3.0 V, $R_S \leq 2$ kΩ)	PSRR	–	90	300	–	90	300	μV/V
Large Signal Voltage Gain ($R_L \geq 100$ kΩ, V_{out} = ±5.0 V) ($R_L \geq 100$ kΩ, V_{out} = ±2.5 V)	A_{VOL}	1500 –	– –	7000 –	– 400	– –	– 1750	
Output Voltage Swing ($R_L \geq 100$ kΩ) ($R_L \geq 10$ kΩ)	V_O	±5.0 ±3.5	±5.3 ±4.0	– –	±2.5 ±1.5	±2.7 ±2.0	– –	V V
Supply Current (V_{out} = 0)	I_D	–	5.0	7.0	–	2.1	3.9	mA
Power Consumption (V_{out} = 0)	P_C	–	90	125	–	19	35	mW

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TYPICAL OUTPUT CHARACTERISTICS

(V_{CC} = 12 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C)

FIGURE 1 – OPEN LOOP GAIN versus POWER SUPPLY VARIATIONS

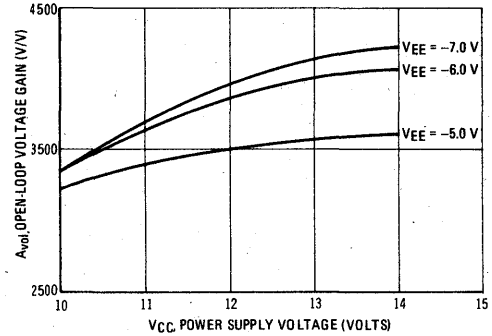


FIGURE 2 – OPEN LOOP VOLTAGE GAIN versus FREQUENCY

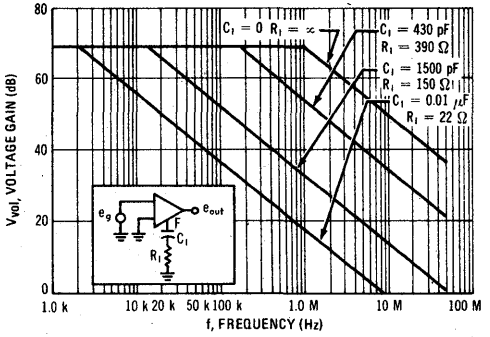


FIGURE 3 – VOLTAGE GAIN versus FREQUENCY

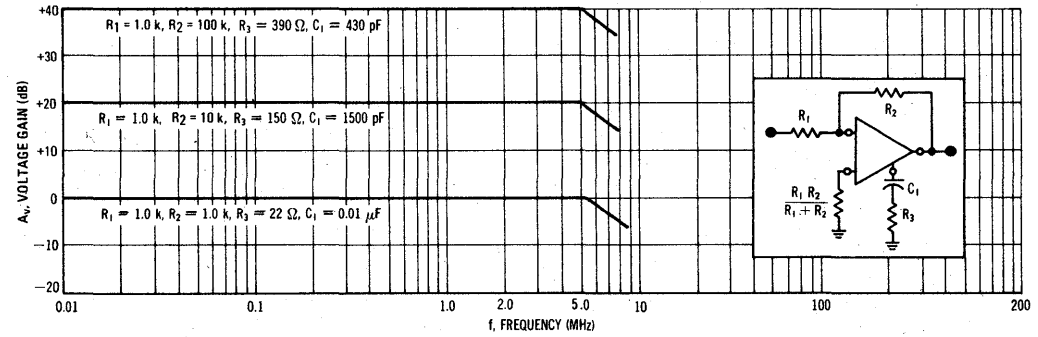
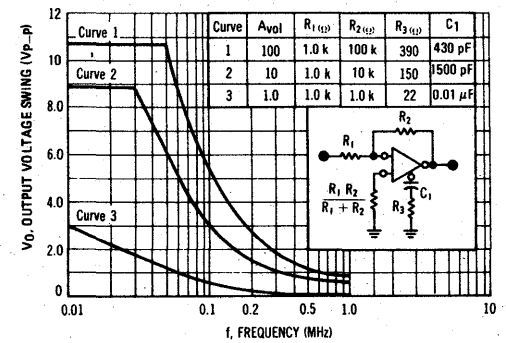
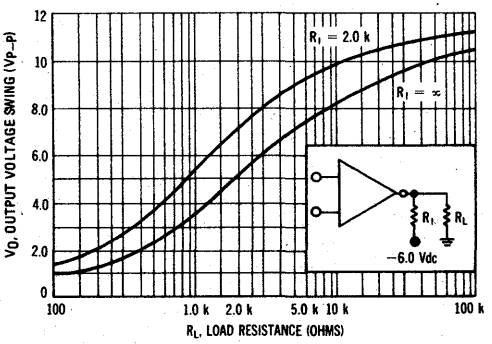


FIGURE 4 – MAXIMUM OUTPUT SWING versus FREQUENCY



Curve	A_{vol}	$R_{1\,(\Omega)}$	$R_{2\,(\Omega)}$	$R_{3\,(\Omega)}$	C_1
1	100	1.0 k	100 k	390	430 pF
2	10	1.0 k	10 k	150	1500 pF
3	1.0	1.0 k	1.0 k	22	0.01 μF

FIGURE 5 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE



TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – INPUT BIAS CURRENT versus TEMPERATURE

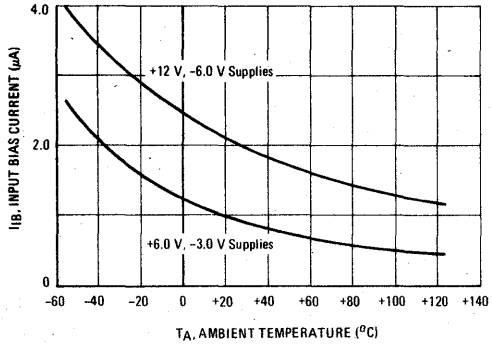


FIGURE 7 – INPUT OFFSET CURRENT versus TEMPERATURE

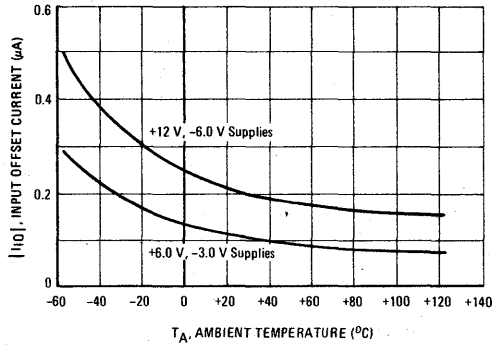


FIGURE 8 – INPUT OFFSET VOLTAGE versus TEMPERATURE

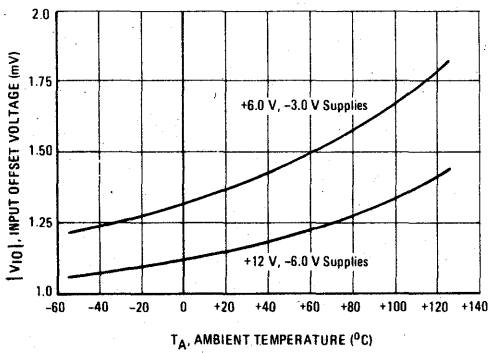
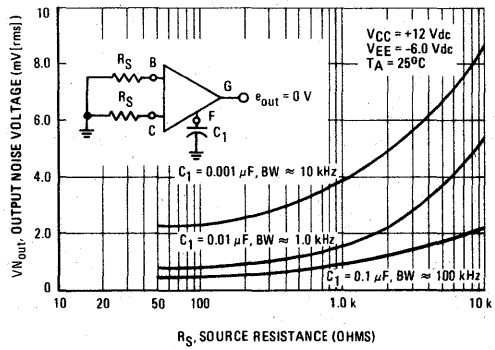


FIGURE 9 – OUTPUT NOISE VOLTAGE versus SOURCE IMPEDANCE



See last page of data sheet for ordering information.

MC1741, MC1741C
MC1741N, MC1741NC

OPERATIONAL AMPLIFIER
SILICON MONOLITHIC
INTEGRATED CIRCUIT

INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Low Noise Selections Offered – N Suffix

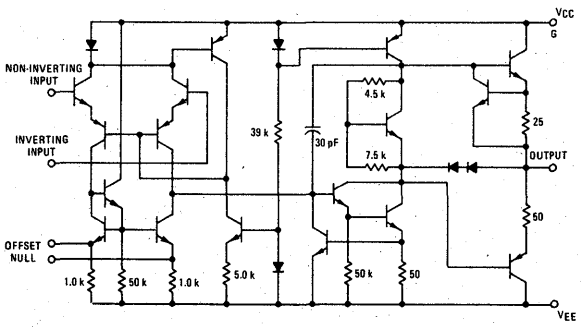
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1741C	MC1741	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc Vdc
Input Differential Voltage	V_{ID}	±30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70	-55 to +125	°C
Storage Temperature Range Metal, Flat and Ceramic Packages Plastic Packages	T_{stg}	-65 to +150 -55 to +125		°C
Junction Temperature Range Metal and Ceramic Packages Plastic Packages	T_J	175 150		°C

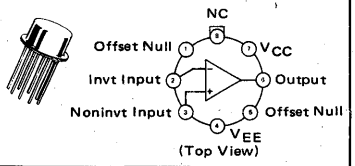
Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.

EQUIVALENT CIRCUIT SCHEMATIC

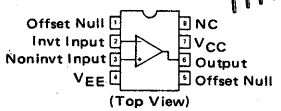


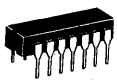
G SUFFIX
METAL PACKAGE
CASE 601



P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1741C,MC1741NC)

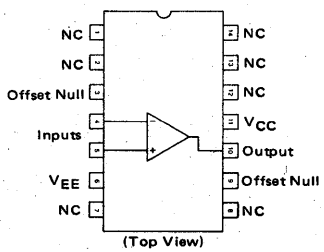
U SUFFIX
CERAMIC PACKAGE
CASE 693



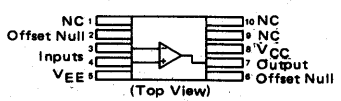


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P2 SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1741C,MC1741NC)



F SUFFIX
CERAMIC PACKAGE
CASE 606-04
TO-91



ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = 15 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	MC1741			MC1741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}	–	1.0	5.0	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	nA
Input Bias Current	I_{IB}	–	80	500	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, $R_L \geq 2.0$ k)	A_v	50	200	–	20	200	–	V/mV
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	–	30	150	μV/V
Output Voltage Swing	V_O							V
($R_L \geq 10$ k)		±12	±14	–	±12	±14	–	
($R_L \geq 2$ k)		±10	±13	–	±10	±13	–	
Output Short-Circuit Current	I_{os}	–	20	–	–	20	–	mA
Supply Current	I_D	–	1.7	2.8	–	1.7	2.8	mA
Power Consumption	P_C	–	50	85	–	50	85	mW
Transient Response (Unity Gain – Non-Inverting)								
(V_I = 20 mV, $R_L \geq 2$ k, $C_L \leq 100$ pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	μs
(V_I = 20 mV, $R_L \geq 2$ k, $C_L \leq 100$ pF) Overshoot	os	–	15	–	–	15	–	%
(V_I = 10 V, $R_L \geq 2$ k, $C_L \leq 100$ pF) Slew Rate	SR	–	0.5	–	–	0.5	–	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = 15 V, T_A = *T_{high} to T_{low} unless otherwise noted.)

Characteristic	Symbol	MC1741			MC1741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	mV
Input Offset Current	I_{IO}							nA
(T_A = 125°C)		–	7.0	200	–	–	–	
(T_A = -55°C)		–	85	500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	300	
Input Bias Current	I_{IB}							nA
(T_A = 125°C)		–	30	500	–	–	–	
(T_A = -55°C)		–	300	1500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	800	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	V
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR	70	90	–	–	–	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	–	–	–	μV/V
Output Voltage Swing	V_O							V
($R_L \geq 10$ k)		±12	±14	–	–	–	–	
($R_L \geq 2$ k)		±10	±13	–	±10	±13	–	
Large Signal Voltage Gain ($R_L \geq 2$ k, V_{out} = ±10 V)	A_v	25	–	–	15	–	–	V/mV
Supply Currents	I_D							mA
(T_A = 125°C)		–	1.5	2.5	–	–	–	
(T_A = -55°C)		–	2.0	3.3	–	–	–	
Power Consumption (T_A = +125°C)	P_C	–	45	75	–	–	–	mW
(T_A = -55°C)		–	60	100	–	–	–	

*T_{high} = 125°C for MC1741 and 70°C for MC1741C
T_{low} = -55°C for MC1741 and 0°C for MC1741C

NOISE CHARACTERISTICS (Applies for MC1741N and MC1741NC only, V_{CC} = 15 V, V_{EE} = -15 V, T_A = +25°C)

Characteristic	Symbol	MC1741N			MC1741NC			Unit
		Min	Typ	Max	Min	Typ	Max	
Burst Noise (Popcorn Noise) (BW = 1.0 Hz to 1.0 kHz, t = 10 s, R_S = 100 k) (Input Referenced)	E_n	–	–	20	–	–	20	μV/peak

FIGURE 1 – BURST NOISE versus SOURCE RESISTANCE

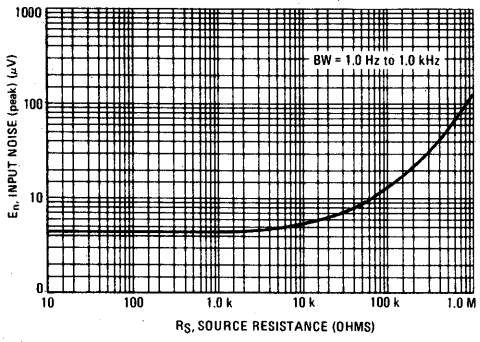


FIGURE 2 – RMS NOISE versus SOURCE RESISTANCE

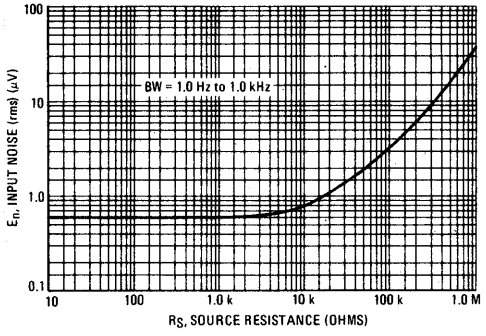


FIGURE 3 – OUTPUT NOISE versus SOURCE RESISTANCE

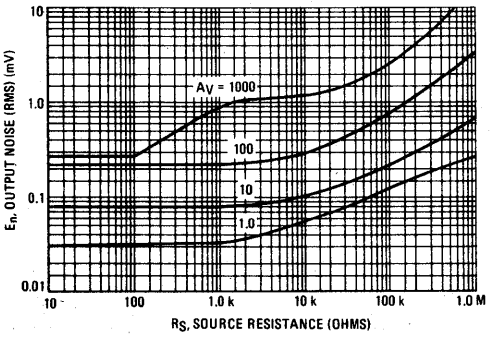


FIGURE 4 – SPECTRAL NOISE DENSITY

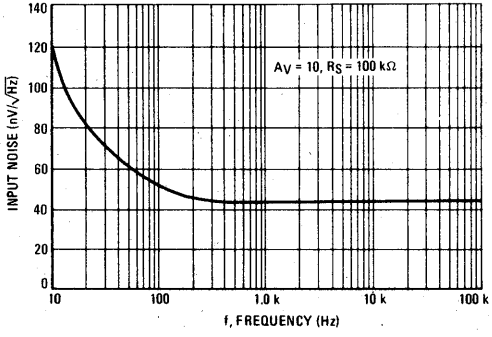
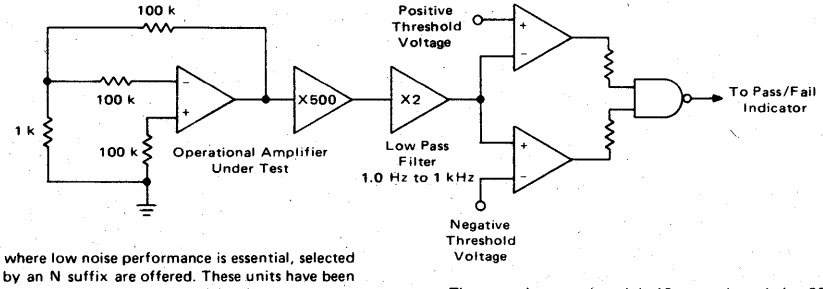


FIGURE 5 – BURST NOISE TEST CIRCUIT (N Suffixed Devices Only)



For applications where low noise performance is essential, selected devices denoted by an N suffix are offered. These units have been 100% tested for burst noise pulses on a special noise test system. Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 seconds and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier under test.

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted).

FIGURE 6 – POWER BANDWIDTH
(LARGE SIGNAL SWING versus FREQUENCY)

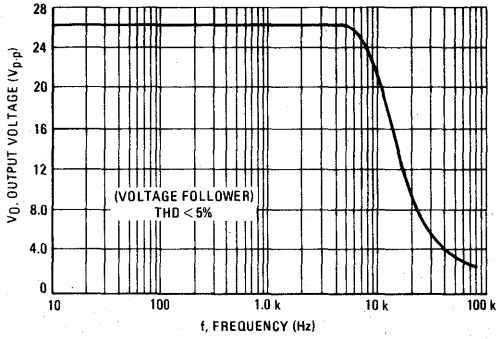


FIGURE 7 – OPEN LOOP FREQUENCY RESPONSE

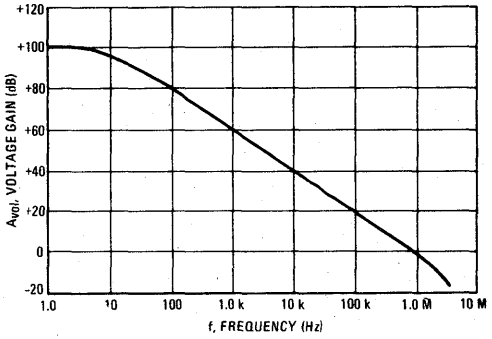


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE

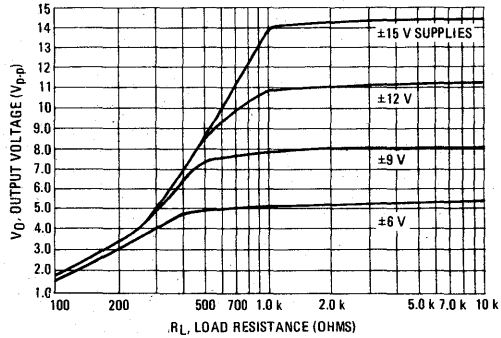


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING
versus LOAD RESISTANCE

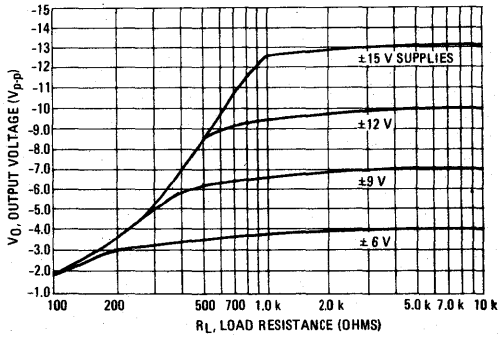


FIGURE 10 – OUTPUT VOLTAGE SWING versus
LOAD RESISTANCE (Single Supply Operation)

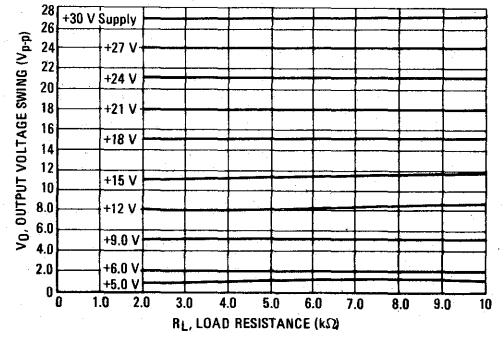
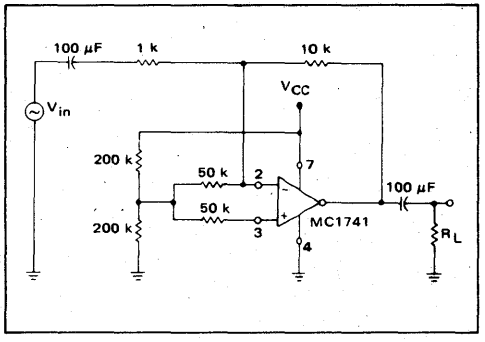


FIGURE 11 – SINGLE SUPPLY INVERTING AMPLIFIER



3

FIGURE 12 – NON-INVERTING PULSE RESPONSE

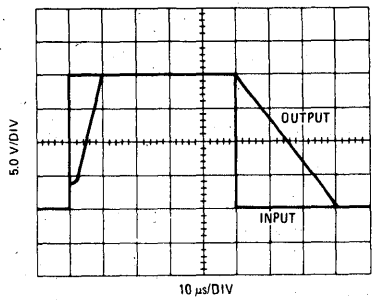


FIGURE 13 – TRANSIENT RESPONSE TEST CIRCUIT

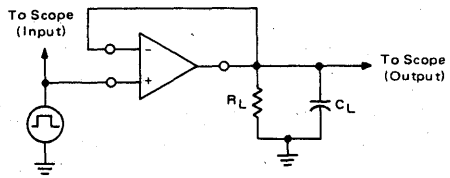
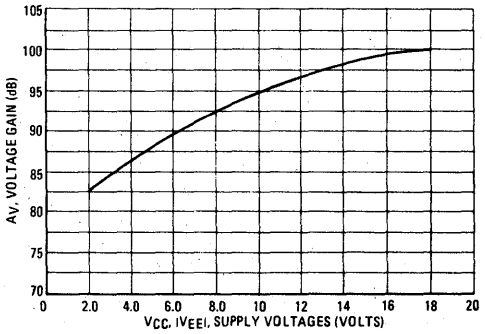


FIGURE 14 – OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1741CF,NCF	—	0°C to +70°C	Ceramic Flat
MC1741CG	LM741CD, μA741HC	0°C to +70°C	Metal Can
MC1741CL	LM741CD, μA741DC	0°C to +70°C	Ceramic DIP
MC1741CP1	LM741CN, μA741TC	0°C to +70°C	Plastic DIP
MC1741CP2, NCP1, NCP2	—	0°C to +70°C	Plastic DIP
MC1741CU,NCU	—	0°C to +70°C	Ceramic DIP
MC1741F,NF	—	−55°C to +125°C	Ceramic Flat
MC1741G,NG	—	−55°C to +125°C	Metal Can
MC1741L,NL	—	−55°C to +125°C	Ceramic DIP
MC1741U,NU	—	−55°C to +125°C	Ceramic DIP
MC1741NCG	—	0°C to +70°C	Metal Can
MC1741NCL	—	0°C to +70°C	Ceramic DIP

ORDERING INFORMATION

Device	Temperature Range	Package
MC1741SG	−55°C to +125°C	Metal Can
MC1741SU	−55°C to +125°C	Ceramic DIP
MC1741SCG	0°C to +70°C	Metal Can
MC1741SCP1	0°C to +70°C	Plastic DIP
MC1741SCU	0°C to +70°C	Ceramic DIP

MC1741S
MC1741SC

HIGH SLEW-RATE INTERNALLY-COMPENSATED OPERATIONAL AMPLIFIER

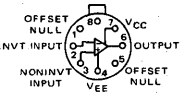
The MC1741S/MC1741SC is functionally equivalent, pin compatible, and possesses the same ease of use as the popular MC1741 circuit, yet offers 20 times higher slew rate and power bandwidth. This device is ideally suited for D-to-A converters due to its fast settling time and high slew rate.

- High Slew Rate — 10 V/μs Guaranteed Minimum (for unity gain only)
- No Frequency Compensation Required
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

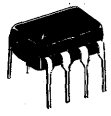
OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

G SUFFIX
METAL PACKAGE
CASE 601-02

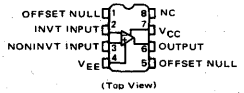


(Top View)



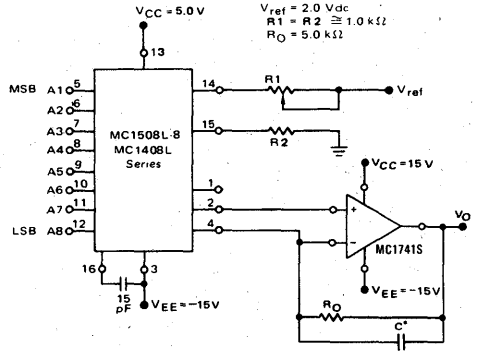
P1 SUFFIX
PLASTIC PACKAGE
CASE 626

U SUFFIX
CERAMIC PACKAGE
CASE 693



(Top View)

TYPICAL APPLICATION OF OUTPUT CURRENT TO VOLTAGE TRANSFORMATION FOR A D-TO-A CONVERTER



Pins not shown are not connected.

Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 μs from the time that all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 150 pF).

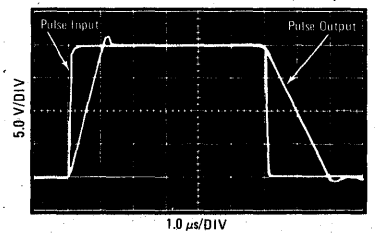
Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

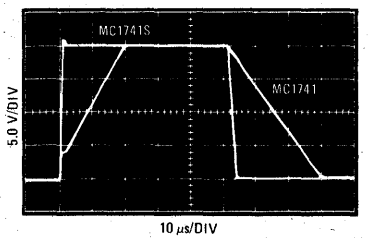
Adjust V_{ref}, R1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\,V}{1\,k}(5\,k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right] = 10\,V\left[\frac{255}{256}\right] = 9.961\,V$$

MC1741S LARGE-SIGNAL TRANSIENT RESPONSE

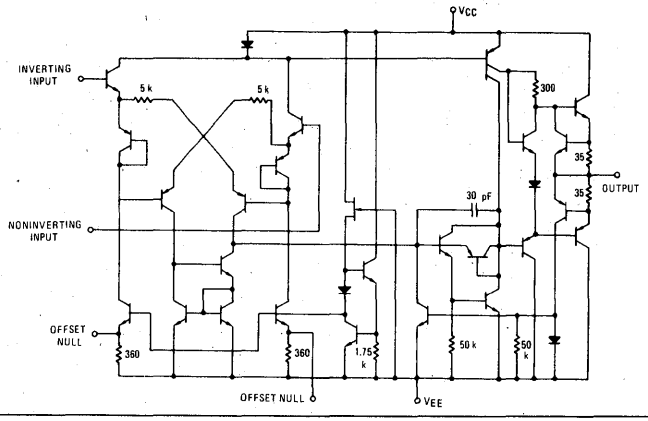


STANDARD MC1741 versus MC1741S RESPONSE COMPARISON



3

CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value MC1741SC	Value MC1741S	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc
Differential Input Signal Voltage	V_{ID}	±30		Volts
Common-Mode Input Voltage Swing (See Note 1)	V_{ICR}	±15		Volts
Output Short-Circuit Duration (See Note 2)	t_s	Continuous		
Power Dissipation (Package Limitation) Metal Package Derate above T_A = +25°C Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 680 4.6 625 5.0		 mW mW/°C mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	-55 to +125	°C
Storage Temperature Range Metal Package Plastic Package	T_{stg}	 -65 to +150 -55 to +125		°C

Note 1. For supply voltages less than ±15 Vdc, the absolute maximum input voltage is equal to the supply voltage.
Note 2. Supply voltage equal to or less than 15 Vdc.

FIGURE 1 – OFFSET ADJUST CIRCUIT

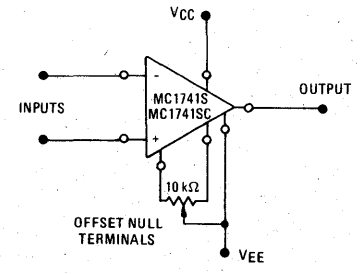
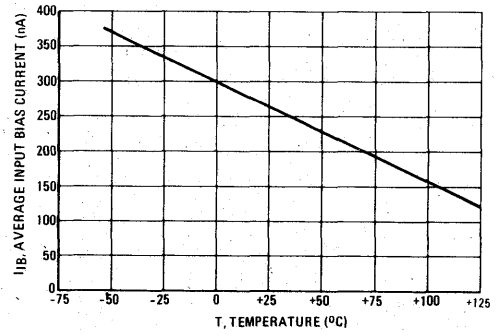


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1741S			MC1741SC			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Bandwidth (See Figure 3) A_V = 1, R_L = 2.0 kΩ, THD = 5%, V_O = 20 V(p-p)	BW_P	150	200	–	150	200	–	kHz
Large-Signal Transient Response Slew Rate (Figures 10 and 11) V(-) to V(+) V(+) to V(-)	SR	10 10	20 12	– –	10 10	20 12	– –	V/μs
Settling Time (Figures 10 and 11) (to within 0.1%)	t_{setlg}	–	3.0	–	–	3.0	–	μs
Small-Signal Transient Response (Gain = 1, E_{in} = 20 mV, see Figures 7 and 8) Rise Time	t_{TLH}	–	0.25	–	–	0.25	–	μs
Fall Time	t_{THL}	–	0.25	–	–	0.25	–	μs
Propagation Delay Time	t_{PLH},t_{PHL}	–	0.25	–	–	0.25	–	μs
Overshoot	OS	–	20	–	–	20	–	%
Short-Circuit Output Currents	I_{OS}	±10	–	±35	±10	–	±35	mA
Open-Loop Voltage Gain (R_L = 2.0 kΩ) (See Figure 4) V_O = ±10 V, T_A = +25°C V_O = ±10 V, T_A = T_{low}* to T_{high}*	A_{vol}	50,000 25,000	200,000 –	– –	20,000 15,000	100,000 –	– –	–
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	Ω
Input Impedance (f = 20 Hz)	z_i	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Swing R_L = 10 kΩ, T_A = T_{low} to T_{high} (MC1741S only) R_L = 2.0 kΩ, T_A = +25°C R_L = 2.0 kΩ, T_A = T_{low} to T_{high}	V_O	±12 ±10 ±10	±14 ±13 –	– – –	±12 ±10 ±10	±14 ±13 –	– – –	V_{pk}
Input Common-Mode Voltage Range T_A = T_{low} to T_{high} (MC1741S)	V_{ICR}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 20 Hz) T_A = T_{low} to T_{high} (MC1741S)	CMRR	70	90	–	70	90	–	dB
Input Bias Current (See Figure 2) T_A = +25°C and T_{high} T_A = T_{low}	I_{IB}	– –	200 500	500 1500	– –	200 –	500 800	nA
Input Offset Current T_A = +25°C and T_{high} T_A = T_{low}	$\|I_{IO}\|$	– –	30 –	200 500	– –	30 –	200 300	nA
Input Offset Voltage (R_S = ⩽10 kΩ) T_A = +25°C T_A = T_{low} to T_{high}	$\|V_{IO}\|$	– –	1.0 –	5.0 6.0	– –	2.0 –	6.0 7.5	mV
DC Power Consumption (See Figure 9) (Power Supply = ±15 V, V_O = 0) T_A = T_{low} to T_{high}	P_C	–	50	85	–	50	85	mW
Positive Voltage Supply Sensitivity (V_{EE} constant) T_A = T_{low} to T_{high} on MC1741S	PSS+	–	2.0	100	–	2.0	150	μV/V
Negative Voltage Supply Sensitivity (V_{CC} constant)	PSS-	–	10	150	–	10	150	μV/V

*T_{low} = 0 for MC1741SC
= -55 °C for MC1741S

T_{high} = +70°C for MC1741SC
= +125 °C for MC1741S

3

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3 – POWER BANDWIDTH – NONDISTORTED OUTPUT VOLTAGE versus FREQUENCY

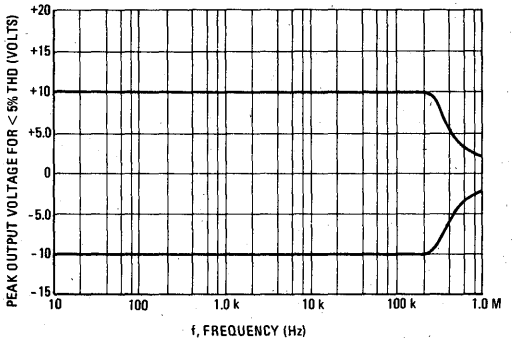


FIGURE 4 – OPEN-LOOP FREQUENCY RESPONSE

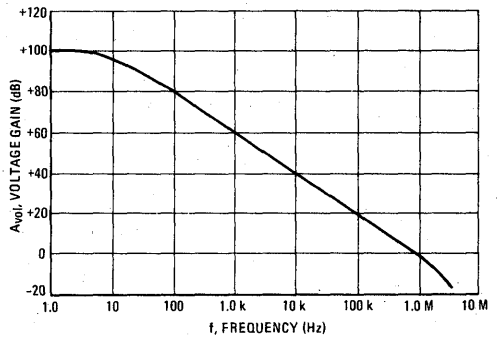


FIGURE 5 – NOISE versus FREQUENCY

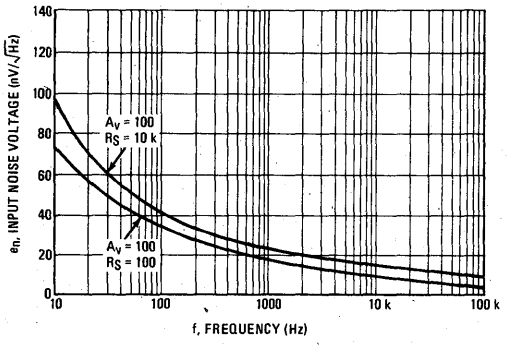


FIGURE 6 – OUTPUT NOISE versus SOURCE RESISTANCE

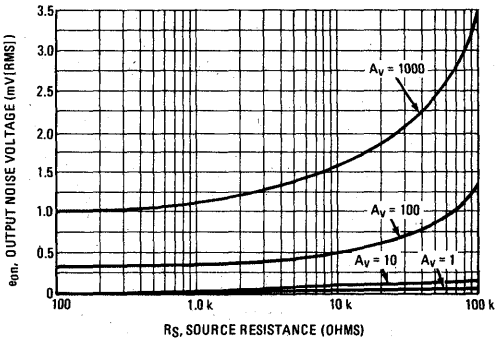


FIGURE 7 – SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS

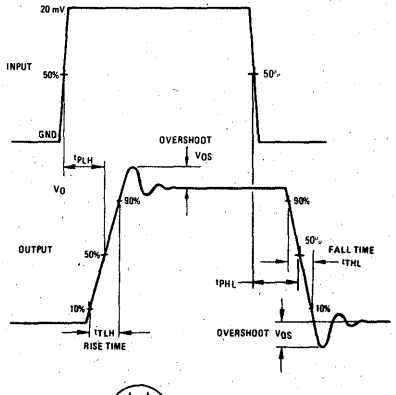
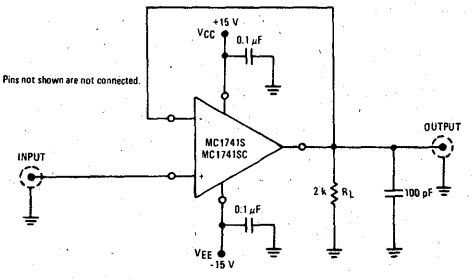


FIGURE 8 – SMALL-SIGNAL TRANSIENT RESPONSE TEST CIRCUIT



TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 9 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGES

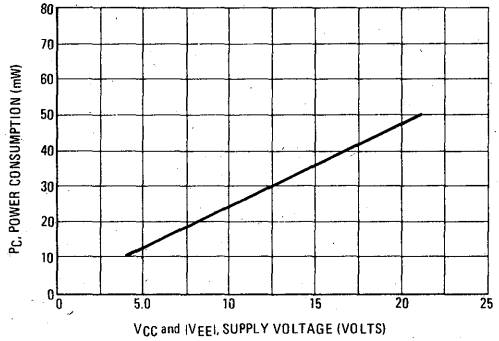


FIGURE 10 – LARGE-SIGNAL TRANSIENT WAVEFORMS

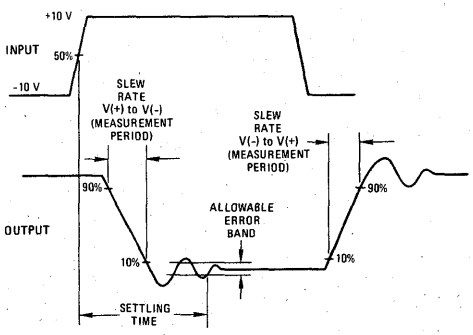
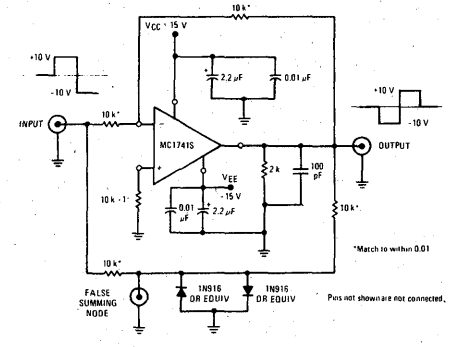


FIGURE 11 – SETTLING TIME AND SLEW RATE TEST CIRCUIT



SETTLING TIME

In order to properly utilize the high slew rate and fast settling time of an operational amplifier, a number of system considerations must be observed. Capacitance at the summing node and at the amplifier output must be minimal and circuit board layout should be consistent with common high-frequency considerations. Both power supply connections should be adequately bypassed as close as possible to the device pins. In bypassing, both low and high-frequency components should be considered to avoid the possibility of excessive ringing. In order to achieve optimum damping, the selection of a capacitor in parallel with the feedback resistor may be necessary. A value too small could result in excessive ringing while a value too large will degrade slew rate and settling time.

SETTLING TIME MEASUREMENT

In order to accurately measure the settling time of an operational amplifier, it is suggested that the "false" summing junction approach be taken as shown in Figure 11. This is necessary since it is difficult to determine when the waveform at the output of the operational amplifier settles to within 0.1% of it's final value. Because the output and input voltages are effectively subtracted from each other at the amplifier inverting input, this seems like an ideal node for the measurement. However, the probe capacitance at this critical node can greatly affect the accuracy of the actual measurement.

The solution to these problems is the creation of a second or "false" summing node. The addition of two diodes at this node clamps the error voltage to limit the voltage excursion to the oscilloscope. Because of the voltage divider effect, only one-half of the actual error appears at this node. For extremely critical measurements, the capacitance of the diodes and the oscilloscope, and the settling time of the oscilloscope must be considered. The expression

$$t_{setlg} = \sqrt{x^2 + y^2 + z^2}$$

can be used to determine the actual amplifier settling time, where

t_{setlg} = observed settling time

x = amplifier settling time (to be determined)

y = false summing junction settling time

z = oscilloscope settling time

It should be remembered that to settle within ±0.1% requires 7RC time constants.

The ±0.1% factor was chosen for the MC1741S settling time as it is compatible with the ±1/2 LSB accuracy of the MC1508L8 digital-to-analog converter. This D-to-A converter features ±0.19% maximum error.

3

FIGURE 12 – WAVEFORM AT FALSE SUMMING NODE

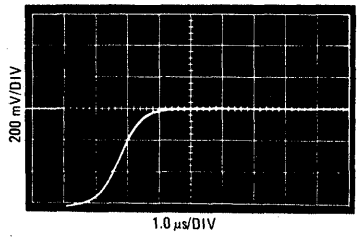
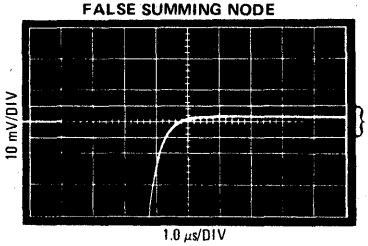
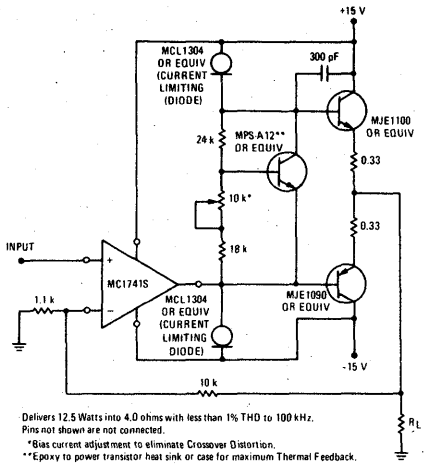


FIGURE 13 – EXPANDED WAVEFORM AT FALSE SUMMING NODE



TYPICAL APPLICATION

FIGURE 14 – 12.5-WATT WIDEBAND POWER AMPLIFIER



Delivers 12.5 Watts into 4.0 ohms with less than 1% THD to 100 kHz.
Pins not shown are not connected.
*Bias current adjustment to eliminate Crossover Distortion.
**Epoxy to power transistor heat sink or case for maximum Thermal Feedback.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1747F	−55°C to +125°C	Ceramic Flat
MC1747G	−55°C to +125°C	Metal Can
MC1747L	−55°C to +125°C	Ceramic DIP
MC1747CF	0°C to +75°C	Ceramic Flat
MC1747CG	0°C to +75°C	Metal Can
MC1747CL	0°C to +75°C	Ceramic DIP
MC1747CP2	0°C to +75°C	Plastic DIP

MC1747
MC1747C

(DUAL MC1741)

DUAL
OPERATIONAL AMPLIFIER

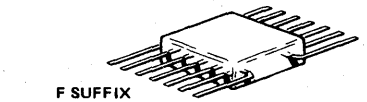
SILICON MONOLITHIC
INTEGRATED CIRCUIT

3

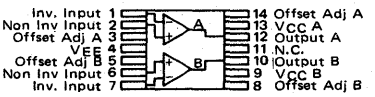
DUAL MC1741
INTERNALLY COMPENSATED, HIGH PERFORMANCE OPERATIONAL AMPLIFIER

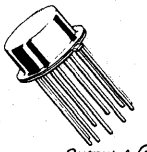
. . . designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. The MC1747L and MC1747CL are functionally, electrically, and pin-for-pin equivalent to the μA747 and μA747C respectively.

- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Offset Voltage Null Capability



F SUFFIX
CERAMIC PACKAGE
CASE 607





G SUFFIX
METAL PACKAGE
CASE 603

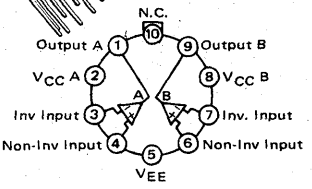
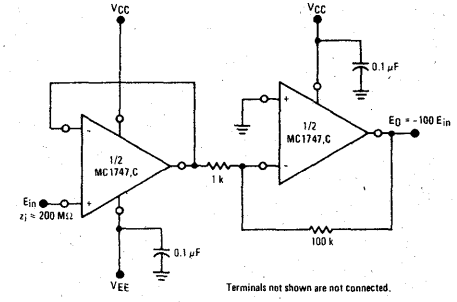
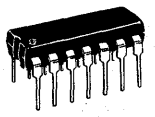


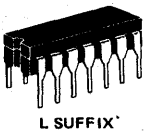
FIGURE 1 – HIGH-IMPEDANCE, HIGH-GAIN INVERTING AMPLIFIER



Terminals not shown are not connected.



P2 SUFFIX
PLASTIC PACKAGE
CASE 646



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
TO-116

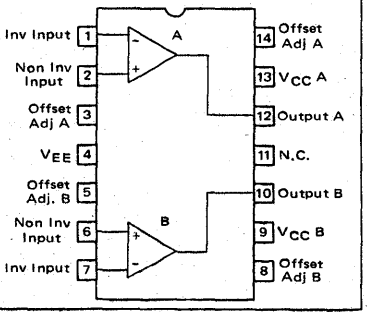
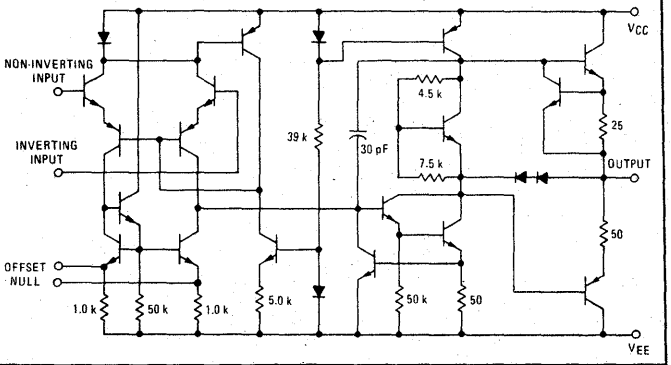


FIGURE 2 – CIRCUIT SCHEMATIC



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent right of Motorola Inc. or others.

DS 9254

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MC1747	MC1747C	Unit
Power Supply Voltages	V_{CC}	+22	+18	Vdc
	V_{EE}	-22	-18	
Differential Input Signal Voltage ①	V_{ID}	± 30		Volts
Common-Mode Input Swing Voltage ②	V_{ICR}	± 15		Volts
Output Short-Circuit Duration	t_{OS}	Continuous		
Voltage (Measurement between Offset Null and V_{EE})		± 0.5		Volts
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C
Junction Temperature Ceramic and Metal Package Plastic Package	T_J	175 150		°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristics	Symbol	MC1747			MC1747C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current	I_{IB}							nAdc
T_A = +25°C		–	80	500	–	80	500	
$T_A = T_{high}$ ③		–	30	500	–	30	800	
$T_A = T_{low}$ ③		–	300	1500	–	30	800	
Input Offset Current	I_{IO}							nAdc
T_A = +25°C		–	20	200	–	20	200	
$T_A = T_{high}$		–	7.0	200	–	7.0	300	
$T_A = T_{low}$		–	85	500	–	7.0	300	
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}							mVdc
T_A = +25°C		–	1.0	5.0	–	1.0	6.0	
$T_A = T_{low}$ to T_{high}		–	1.0	6.0	–	1.0	7.5	
Offset Voltage Adjustment Range		–	± 15	–	–	± 15	–	mV
Differential Input Impedance (Open-loop, f = 20 Hz)								
Parallel Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Parallel Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Common-Mode Input Voltage Swing	V_{ICR}							Volts
$T_{low} \leq T_A \leq T_{high}$		± 12	± 13	–	± 12	± 13	–	
Common-Mode Rejection Ratio (R_S = 10 kΩ)	CMRR							dB
$T_{low} \leq T_A \leq T_{high}$		70	90	–	70	90	–	
Open-Loop Voltage Gain	A_{vol}							Volts
T_A = +25°C (V_O = ±10 V, R_L = 2.0 kΩ)		50,000	200,000	–	25,000	200,000	–	
$T_A = T_{low}$ to T_{high} (V_O = ±10 V, R_L = 2.0 kΩ)		25,000	–	–	15,000	–	–	
Transient Response (Unity Gain) (V_{in} = 20 mV, R_L = 2.0 kΩ, $C_L \leq$ 100 pF)								
Rise Time	t_{PLH}	–	0.3	–	–	0.3	–	μs
Overshoot Percentage		–	5.0	–	–	5.0	–	%
Slew Rate (Unity Gain)	SR	–	0.5	–	–	0.5	–	V/μs
Output Impedance	z_o	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{OS}	–	25	–	–	25	–	mAdc
Channel Separation		–	120	–	–	120	–	dB
Output Voltage Swing ($T_{low} \leq T_A \leq T_{high}$)	V_{OR}							V_{pk}
R_L = 10 kΩ		± 12	± 14	–	± 12	± 14	–	
R_L = 2.0 kΩ		± 10	± 13	–	± 10	± 13	–	
Power Supply Sensitivity (T_{low} to T_{high})								μV/V
V_{EE} = Constant, $R_S \leq$ 10 kΩ	PSS+	–	30	150	–	30	150	
V_{CC} = Constant, $R_S \leq$ 10 kΩ	PSS-	–	30	150	–	30	150	
Power Supply Current (each amplifier)	I_{CC},I_{EE}							mAdc
T_A = +25°C		–	1.7	2.8	–	1.7	2.8	
$T_A = T_{low}$		–	2.0	3.3	–	2.0	3.3	
$T_A = T_{high}$		–	1.5	2.5	–	2.0	3.3	
DC Power Consumption (each amplifier)	P_C							mW
T_A = +25°C		–	50	85	–	50	85	
$T_A = T_{low}$		–	60	100	–	60	100	
$T_A = T_{high}$		–	45	75	–	60	100	

① For supply voltages of less than ± 15 V, the maximum differential input voltage is equal to ± (V_{CC} + |V_{EE}|).
② For supply voltages of less than ± 15 V, the maximum input voltage is equal to the supply voltage (+V_{CC}, -|V_{EE}|).
③ T_{low}: 0°C for MC1747CL
-55°C for MC1747L
T_{high}: +75°C for MC1747CL
+125°C for MC1747L

FIGURE 3 – TYPICAL FREQUENCY-SHIFT KEYER TONE GENERATOR TEST CIRCUIT

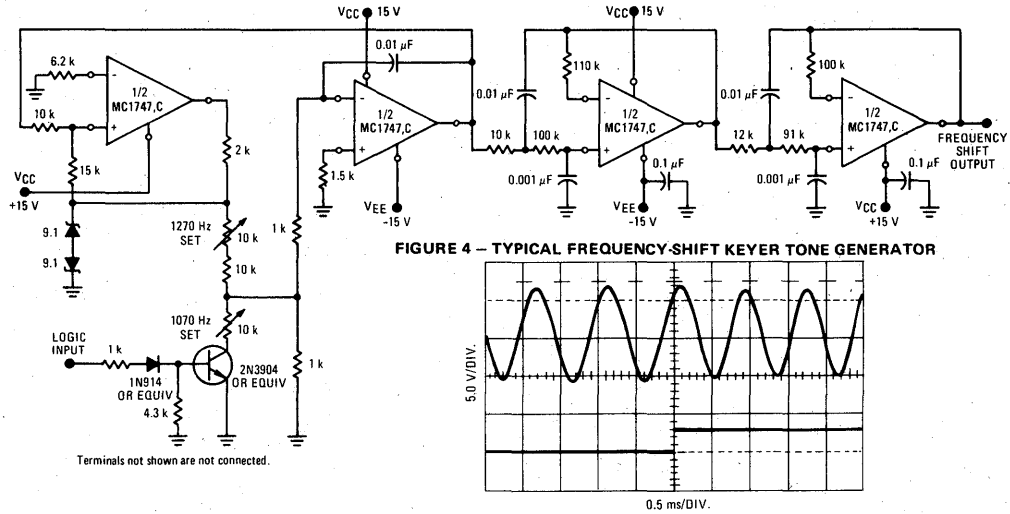


FIGURE 4 – TYPICAL FREQUENCY-SHIFT KEYER TONE GENERATOR

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 5 – OPEN-LOOP VOLTAGE GAIN versus POWER-SUPPLY VOLTAGE

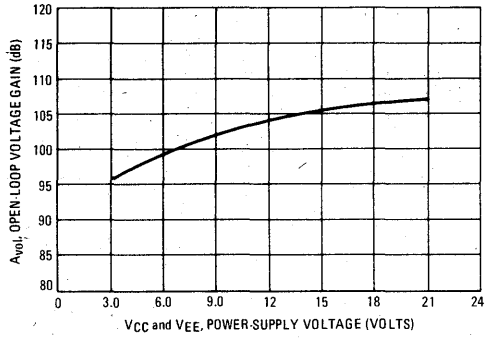


FIGURE 6 – OPEN-LOOP FREQUENCY RESPONSE

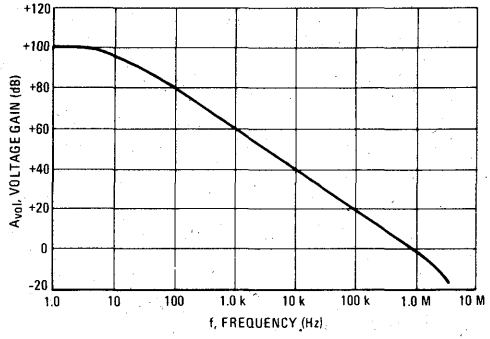


FIGURE 7 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

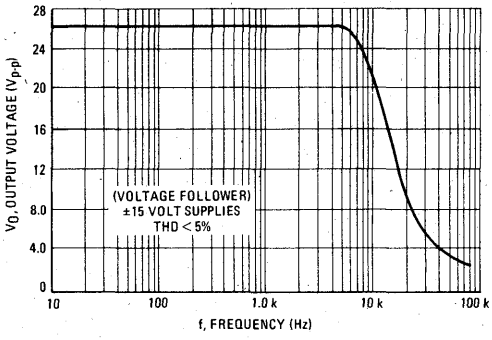
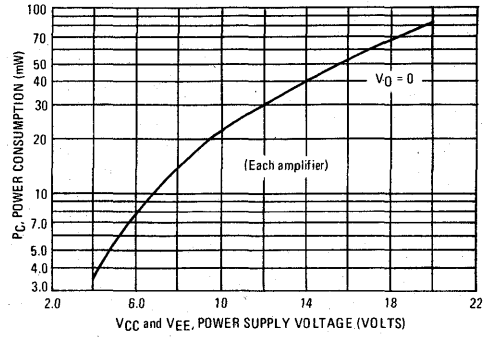


FIGURE 8 – POWER CONSUMPTION versus POWER SUPPLY VOLTAGE



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TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = −15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 9 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

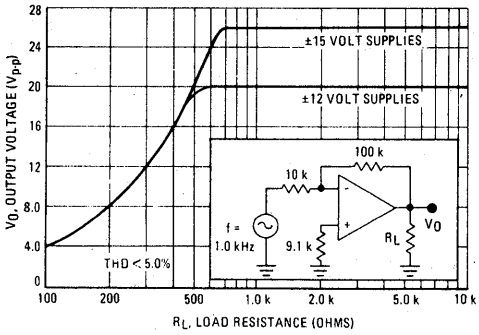
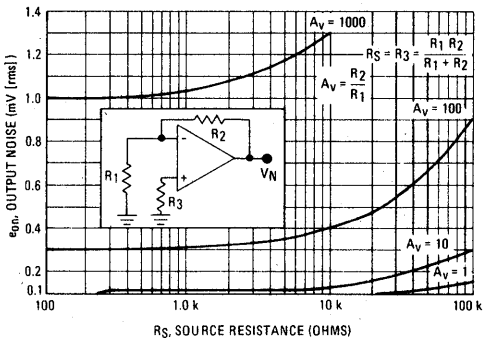


FIGURE 10 – OUTPUT NOISE versus SOURCE RESISTANCE



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

ORDERING INFORMATION

Device	Temperature Range	Package
MC1748G	−55°C to +125°C	Metal Can
MC1748U	−55°C to +125°C	Ceramic DIP
MC1748CG	0°C to +70°C	Metal Can
MC1748CP1	0°C to +70°C	Plastic DIP
MC1748CU	0°C to +70°C	Ceramic DIP

MC1748
MC1748C

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Noncompensated MC1741
- Single 30 pF Capacitor Compensation Required For Unity Gain
- Short-Circuit Protection
- Offset Voltage Null Capability
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up

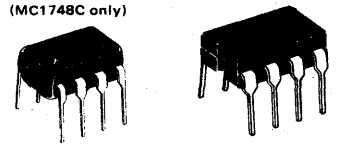
OPERATIONAL AMPLIFIER

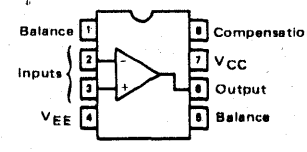
SILICON MONOLITHIC INTEGRATED CIRCUIT

3

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1748C only)

U SUFFIX
CERAMIC PACKAGE
CASE 693





G SUFFIX
METAL PACKAGE
CASE 601

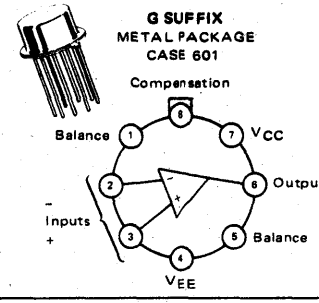
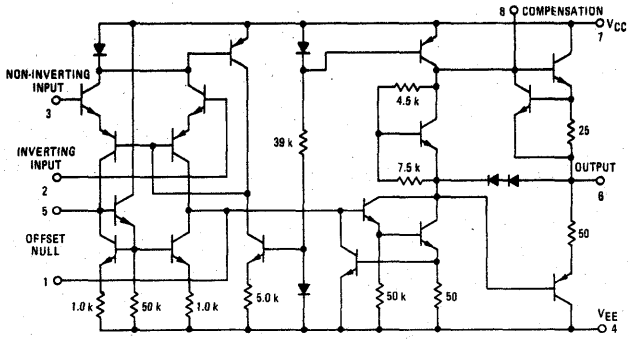


FIGURE 1 – CIRCUIT SCHEMATIC



TYPICAL COMPENSATION CIRCUITS

FIGURE 2 – OFFSET ADJUST AND FREQUENCY COMPENSATION

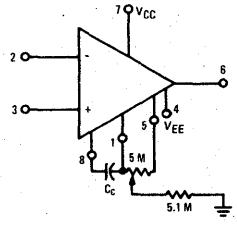


FIGURE 3 – SINGLE-POLE COMPENSATION

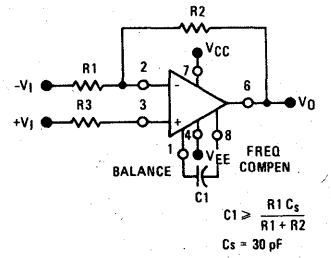
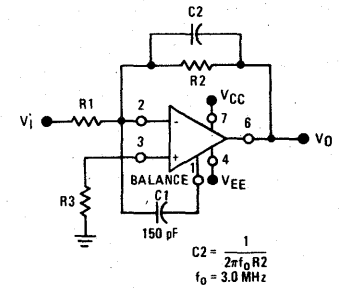


FIGURE 4 – FEEDFORWARD COMPENSATION



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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC1748	MC1748C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Differential Input Signal	V_{in}	±30		Volts
Common-Mode Input Swing ①	V_{ICR}	±15		Volts
Output Short Circuit Duration	t_s	Continuous		
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6		mW mW/°C
Operating Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

Characteristics	Symbol	MC1748 Min	MC1748 Typ	MC1748 Max	MC1748C Min	MC1748C Typ	MC1748C Max	Unit
Input Bias Current	I_{IB}							μAdc
T_A = +25°C		–	0.08	0.5	–	0.08	0.5	
$T_A = T_{low}$ to T_{high} ②		–	0.3	1.5	–	–	0.8	
Input Offset Current	$\|I_{IO}\|$							μAdc
T_A = +25°C		–	0.02	0.2	–	0.02	0.2	
$T_A = T_{low}$ to T_{high}		–	0.08	0.5	–	–	0.3	
Input Offset Voltage ($R_S \leq 10$ k Ω)	$\|V_{IO}\|$							mVdc
T_A = +25°C		–	1.0	5.0	–	1.0	6.0	
$T_A = T_{low}$ to T_{high}		–	–	6.0	–	–	7.5	
Differential Input Impedance (Open-Loop, f = 20 Hz)								
Parallel Input Resistance	R_p	0.3	2.0	–	0.3	2.0	–	Megohm
Parallel Input Capacitance	C_p	–	1.4	–	–	1.4	–	pF
Common-Mode Input Impedance (f = 20 Hz)	z_{in}	–	200	–	–	200		Megohms
Common-Mode Input Voltage Swing	V_{ICR}	±12	±13	–	±12	±13	–	V_{pk}
Common-Mode Rejection Ratio (f = 100 Hz)	CMRR	70	90	–	70	90	–	dB
Open-Loop Voltage Gain, (V_o = ±10 V, R_L = 2.0 k ohms)	A_{vol}							V/V
T_A = +25°C		50,000	200,000	–	20,000	200,000	–	
$T_A = T_{low}$ to T_{high}		25,000	–	–	15,000	–	–	
Step Response (V_{in} = 20 mV, C_c = 30 pF, R_L = 2 kΩ, C_L = 100 pF)								
Rise Time	t_r	–	0.3	–	–	0.3	–	μs
Overshoot Percentage		–	5.0	–	–	5.0	–	%
Slew Rate	dV_{out}/dt	–	0.8	–	–	0.8	–	V/μs
Output Impedance (f = 20 Hz)	z_o	–	75	–	–	75	–	ohms
Short-Circuit Output Current	I_{sc}	–	25	–	–	25	–	mAdc
Output Voltage Swing (R_L = 10 k ohms)	V_O	±12	±14	–	±12	±14	–	Vpk
R_L = 2 k ohms ($T_A = T_{low}$ to t_{high})		±10	±13	–	±10	±13	–	
Power Supply Sensitivity								μV/V
V_{EE} = constant, $R_s \leq 10$ k ohms	S+	–	30	150	–	30	150	
V_{CC} = constant, $R_s \leq 10$ k ohms	S-	–	30	150	–	30	150	
Power Supply Current	I_D^+	–	1.67	2.83	–	1.67	2.83	mAdc
	I_D^-	–	1.67	2.83	–	1.67	2.83	
DC Quiescent Power Dissipation	P_D							mW
(V_o = 0)		–	50	85	–	50	85	

① For supply voltages less than ±15 V, the Maximum Input Voltage is equal to the Supply Voltage.

② T_{low}: 0°C for MC1748C
-55°C for MC1748
T_{high}: +70° for MC1748C
+125°C for MC1748

TYPICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 5 – MINIMUM INPUT VOLTAGE RANGE

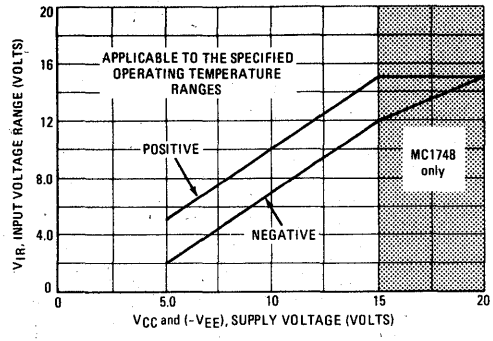


FIGURE 6 – MINIMUM OUTPUT VOLTAGE SWING

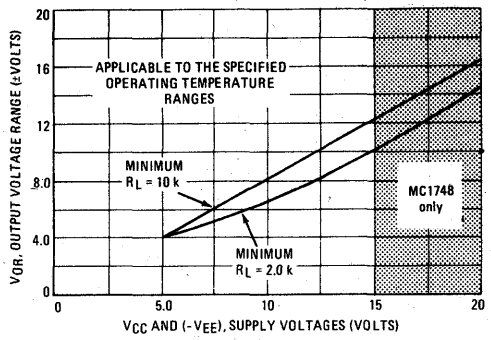


FIGURE 7 – MINIMUM VOLTAGE GAIN

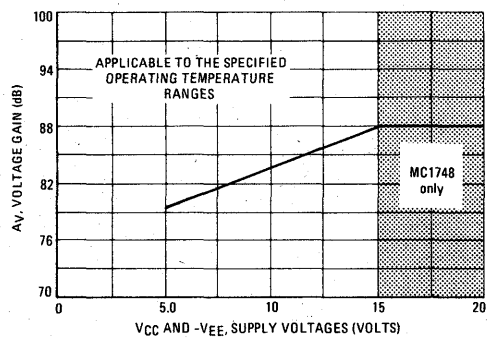


FIGURE 8 – TYPICAL SUPPLY CURRENTS

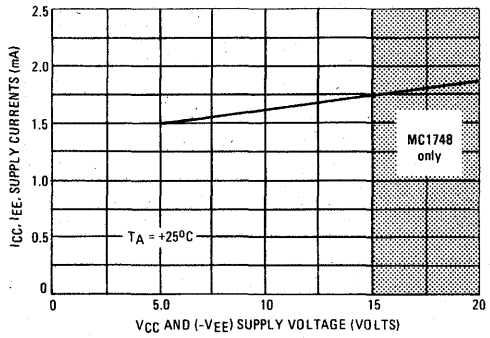


FIGURE 9 – OPEN-LOOP FREQUENCY RESPONSE

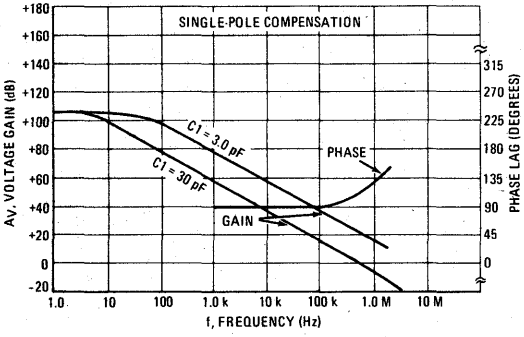
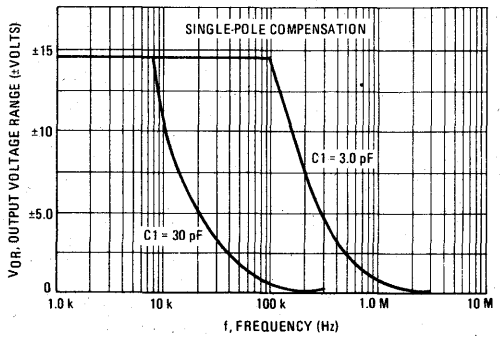


FIGURE 10 – LARGE-SIGNAL FREQUENCY RESPONSE



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TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 11 – VOLTAGE FOLLOWER PULSE RESPONSE

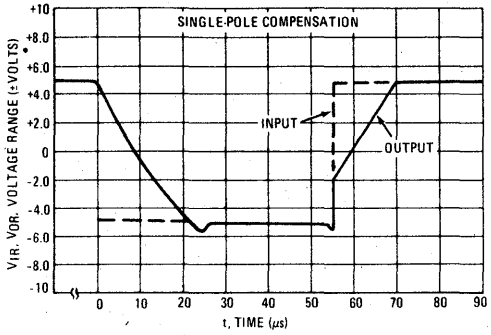


FIGURE 12 – OPEN-LOOP FREQUENCY RESPONSE

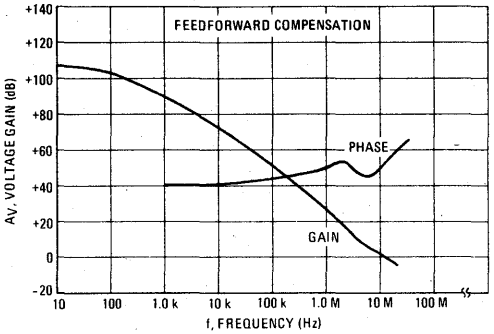


FIGURE 13 – LARGE-SIGNAL FREQUENCY RESPONSE

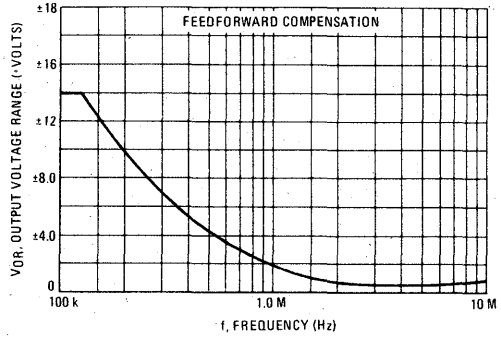
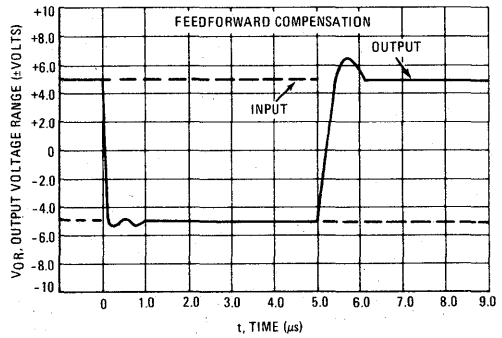


FIGURE 14 – INVERTER PULSE RESPONSE



ORDERING INFORMATION

Device	Temperature Range	Package
MC1776G	−55°C to +125°C	Metal Can
MC1776CG	0°C to +70°C	Metal Can
MC1776CP1	0°C to +70°C	Plastic DIP

MC1776
MC1776C

Specifications and Applications Information

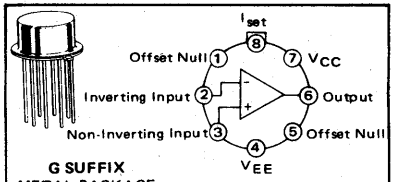
MICROPOWER PROGRAMMABLE OPERATIONAL AMPLIFIER

This extremely versatile operational amplifier features low-power consumption, high input impedance and low input noise levels. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current, power consumption and input voltage, and current noise despite wide variations in operating power supply voltages.

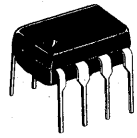
- ±1.2 V to ±18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short-Circuit Protection

PROGRAMMABLE OPERATIONAL AMPLIFIER

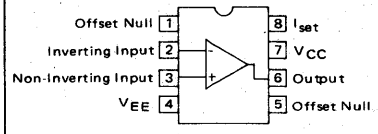
SILICON MONOLITHIC INTEGRATED CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 601-03

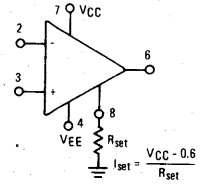


P1 SUFFIX
PLASTIC PACKAGE
CASE 626



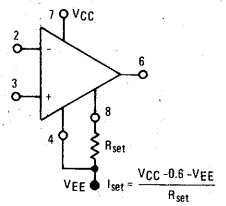
RESISTIVE PROGRAMMING (See Figure 1.)

R_{set} to GROUND



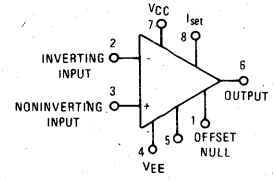
Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 μA	I_{set} = 15 μA
±6.0V	3.6 MΩ	360 kΩ
±10V	6.2 MΩ	620 kΩ
±12V	7.5 MΩ	750 kΩ
±15V	10 MΩ	1.0 MΩ

R_{set} to NEGATIVE SUPPLY
(Recommended for supply voltage less than ±6.0 V)



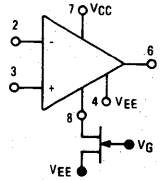
Typical R_{set} Values		
V_{CC}, V_{EE}	Iset = 1.5 μA	I_{set} = 15 μA
±1.5V	1.6 MΩ	160 kΩ
±3.0V	3.6 MΩ	360 kΩ
±6.0V	7.5 MΩ	750 kΩ
±15 V	20 MΩ	2.0 MΩ

PIN CONNECTIONS

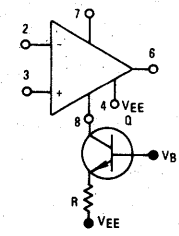


ACTIVE PROGRAMMING

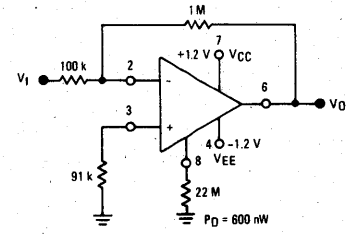
FET CURRENT SOURCE



BIPOLAR CURRENT SOURCE



NANOWATT AMPLIFIER APPLICATION

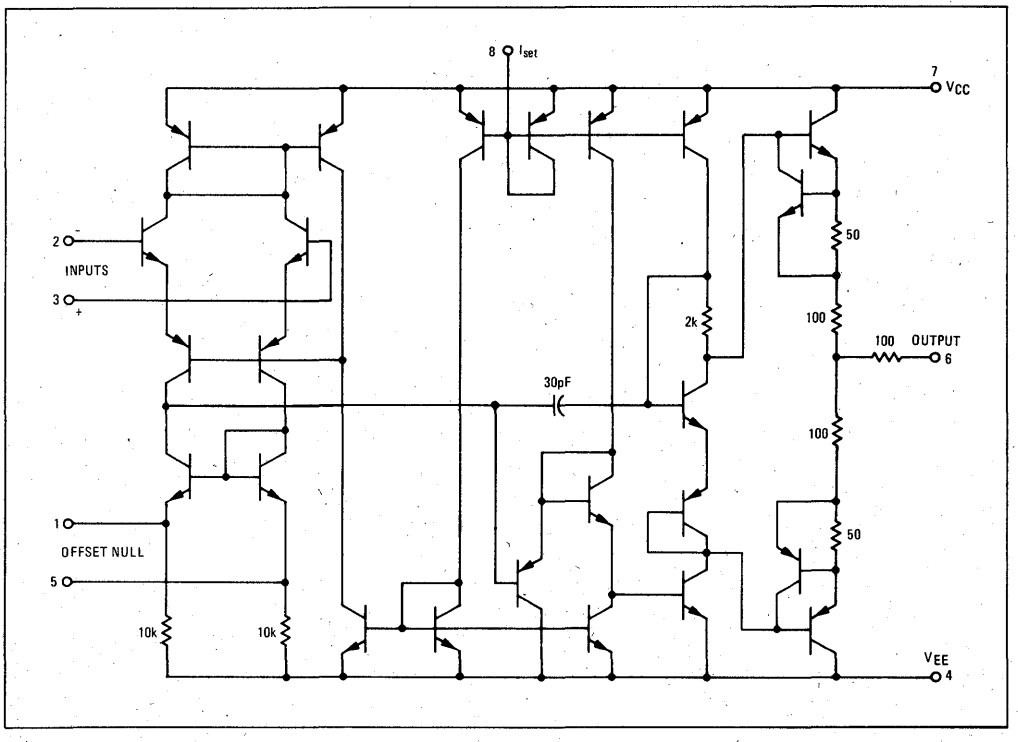


MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±18	Vdc
Differential Input Voltage	V_{ID}	±30	Vdc
Common-Mode Input Voltage V_{CC} and $\|V_{EE}\| < 15$ V V_{CC} and $\|V_{EE}\| \geq 15$ V	V_{ICM}	 V_{CC}, V_{EE} ±15	Vdc
Offset Null to V_{EE} Voltage	$V_{off}-V_{EE}$	±0.5	Vdc
Programming Current	I_{set}	500	μA
Programming Voltage (Voltage from I_{set} terminal to ground)	V_{set}	(V_{CC} - 2.0 V) to V_{CC}	Vdc
Output Short-Circuit Duration*	t_s	Indefinite	s
Operating Temperature Range MC1776 MC1776C	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6	mW mW/C°

*May be to ground or either Supply Voltage. Rating applies up to a case temperature of +125°C or ambient temperature of +75°C and $I_{set} \leq 30$ μA.

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, I_{set} = 1.5 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1776 Min	MC1776 Typ	MC1776 Max	MC1776C Min	MC1776C Typ	MC1776C Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	$\|V_{IO}\|$							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* ≤ $T_A \leq T_{high}$*		–	–	6.0	–	–	7.5	
Input Offset Current	$\|I_{IO}\|$							nA
T_A = +25°C		–	0.7	3.0	–	0.7	6.0	
$T_A = T_{high}$		–	–	5.0	–	–	6.0	
$T_A = T_{low}$		–	–	10	–	–	10	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	2.0	7.5	–	2.0	10	
$T_A = T_{high}$		–	–	7.5	–	–	10	
$T_A = T_{low}$		–	–	20	–	–	20	
Input Resistance	R_{in}	–	50	–	–	50	–	MΩ
Input Capacitance	C_{in}	–	2.0	–	–	2.0	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	9.0	–	–	9.0	–	mV
Large Signal Voltage Gain	A_{vol}							V/V
$R_L \geq 75$ kΩ, $V_O = \pm 10$ V, T_A = +25°C		200 k	400 k	–	50 k	400 k	–	
$R_L \geq 75$ kΩ, $V_O = \pm 10$ V, $T_{low} \leq T_A \leq T_{high}$		100 k	–	–	50 k	–	–	
Output Resistance	R_O	–	5.0	–	–	5.0	–	kΩ
Output Short-Circuit Current	I_{Osc}	–	3.0	–	–	3.0	–	mA
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		–	20	25	–	20	30	
$T_{low} \leq T_A \leq T_{high}$		–	–	30	–	–	35	
Power Dissipation	P_D							mW
T_A = +25°C		–	–	0.75	–	–	0.9	
$T_{low} \leq T_A \leq T_{high}$		–	–	0.9	–	–	1.05	
Transient Response (Unity Gain)								
V_{in} = 20 mV, $R_L \geq 5.0$ kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	1.6	–	–	1.6	–	μs
Overshoot	OS	–	0	–	–	0	–	%
Slew Rate ($R_L \geq 5.0$ kΩ)	SR	–	0.1	–	–	0.1	–	V/μs
Output Voltage Swing	V_O							V
$R_L \geq 75$ kΩ, T_A = +25°C		±12	±14	–	±12	±14	–	
$R_L \geq 75$ kΩ, $T_{low} \leq T_A \leq T_{high}$		±10	–	–	±10	–	–	
Input Voltage Range	V_{ID}							V
$T_{low} \leq T_A \leq T_{high}$		±10	–	–	±10	–	–	
Common-Mode Rejection Ratio	CMRR							dB
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		70	90	–	70	90	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		–	25	150	–	25	200	

*T_{low} = -55°C for MC1776
0°C for MC1776C

T_{high} = +125°C for MC1776
+70°C for MC1776C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, I_{set} = 15 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1776			MC1776C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ)	$\|V_{IO}\|$							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* ≤ $T_A \leq T_{high}$*		–	–	6.0	–	–	7.5	
Input Offset Current	$\|I_{IO}\|$							nA
T_A = +25°C		–	2.0	15	–	2.0	25	
$T_A = T_{high}$		–	–	15	–	–	25	
$T_A = T_{low}$		–	–	40	–	–	40	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	15	50	–	15	50	
$T_A = T_{high}$		–	–	50	–	–	50	
$T_A = T_{low}$		–	–	120	–	–	100	
Input Resistance	R_{in}	–	5.0	–	–	5.0	–	MΩ
Input Capacitance	C_{in}	–	2.0	–	–	2.0	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	–	18	–	mV
Large Signal Voltage Gain	A_{vol}							V/V
$R_L \geq 5.0$ kΩ, V_O = ±10 V, T_A = +25°C		100 k	400 k	–	50 k	400 k	–	
$R_L \geq 75$ kΩ, V_O = ±10 V $T_{low} \leq T_A \leq T_{high}$		75 k	–	–	50 k	–	–	
Output Resistance	R_O	–	1.0	–	–	1.0	–	kΩ
Output Short-Circuit Current	I_{Osc}	–	12	–	–	12	–	mA
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		–	160	180	–	160	190	
$T_{low} \leq T_A \leq T_{high}$		–	–	200	–	–	200	
Power Dissipation	P_D							mW
T_A = +25°C		–	–	5.4	–	–	5.7	
$T_{low} \leq T_A \leq T_{high}$		–	–	6.0	–	–	6.0	
Transient Response (Unity Gain)								
V_{in} = 20 mV, $R_L \geq 5.0$ kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	0.35	–	–	0.35	–	μs
Overshoot	OS	–	10	–	–	10	–	%
Slew Rate ($R_L \geq 5.0$ kΩ)	SR	–	0.8	–	–	0.8	–	V/μs
Output Voltage Swing	V_O							V
$R_L \geq 5.0$ kΩ, T_A = +25°C		±10	±13	–	±10	±13	–	
$R_L \geq 75$ kΩ, $T_{low} \leq T_A \leq T_{high}$		±10	–	–	±10	–	–	
Input Voltage Range	V_{ID}							V
$T_{low} \leq T_A \leq T_{high}$		±10	–	–	±10	–	–	
Common-Mode Rejection Ratio	CMRR							dB
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		70	90	–	70	90	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		–	25	150	–	25	200	

*T_{low} = -55°C for MC1776
0°C for MC1776C

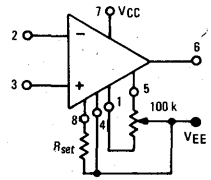
T_{high} = +125°C for MC1776
+70°C for MC1776C

ELECTRICAL CHARACTERISTICS (V_{CC} = +3.0 Vdc, V_{EE} = -3.0 Vdc, I_{set} = 1.5 μA, T_A = +25°C unless otherwise noted.)

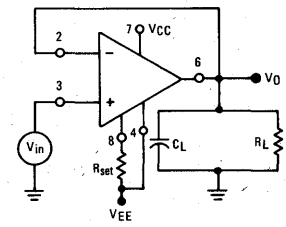
Characteristic	Symbol	MC1776 Min	MC1776 Typ	MC1776 Max	MC1776C Min	MC1776C Typ	MC1776C Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	$\|V_{IO}\|$							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* ≤ T_A ≤ T_{high}*		–	–	6.0	–	–	7.5	
Input Offset Current	$\|I_{IO}\|$							nA
T_A = +25°C		–	0.7	3.0	–	0.7	6.0	
T_A = T_{high}		–	–	5.0	–	–	6.0	
T_A = T_{low}		–	–	10	–	–	10	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	2.0	7.5	–	2.0	10	
T_A = T_{high}		–	–	7.5	–	–	10	
T_A = T_{low}		–	–	20	–	–	20	
Input Resistance	R_{in}	–	50	–	–	50	–	MΩ
Input Capacitance	C_{in}	–	2.0	–	–	2.0	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	9.0	–	–	9.0	–	mV
Large Signal Voltage Gain	A_{vol}							V/V
$R_L \geq 75$ kΩ, V_O = ±1.0 V, T_A = +25°C		50 k	200 k	–	25 k	200 k	–	
$R_L \geq 75$ kΩ, V_O = ±1.0 V, $T_{low} \leq T_A \leq T_{high}$		25 k	–	–	25 k	–	–	
Output Resistance	R_O	–	5.0	–	–	5.0	–	kΩ
Output Short-Circuit Current	I_{Osc}	–	3.0	–	–	3.0	–	mA
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		–	13	20	–	13	20	
$T_{low} \leq T_A \leq T_{high}$		–	–	25	–	–	25	
Power Dissipation	P_D							μW
T_A = +25°C		–	78	120	–	78	120	
$T_{low} \leq T_A \leq T_{high}$		–	–	150	–	–	150	
Transient Response (Unity Gain)								
V_{in} = 20 mV, $R_L \geq 5.0$ kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	3.0	–	–	3.0	–	μs
Overshoot	OS	–	0	–	–	0	–	%
Slew Rate ($R_L \geq 5.0$ kΩ)	S_R	–	0.03	–	–	0.03	–	V/μs
Output Voltage Swing	V_O							V
$R_L \geq 75$ kΩ, $T_{low} \leq T_A \leq T_{high}$		±2.0	±2.4	–	±2.0	±2.4	–	
Input Voltage Range	V_{ID}							V
$T_{low} \leq T_A \leq T_{high}$		±1.0	–	–	±1.0	–	–	
Common-Mode Rejection Ratio	CMRR							dB
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		70	86	–	70	86	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		–	25	150	–	25	200	

*T_{low} = -55°C for MC1776, 0°C for MC1776C T_{high} = +125°C for MC1776, +70°C for MC1776C

VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT-RESPONSE TEST CIRCUIT



Pins not shown are not connected.

3

ELECTRICAL CHARACTERISTICS (V_{CC} = +3.0 V, V_{EE} = -3.0 V, I_{set} = 15 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1776 Min	MC1776 Typ	MC1776 Max	MC1776C Min	MC1776C Typ	MC1776C Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	$\|V_{IO}\|$							mV
T_A = +25°C		–	2.0	5.0	–	2.0	6.0	
T_{low}* ≤ $T_A \leq T_{high}$*		–	–	6.0	–	–	7.5	
Input Offset Current	$\|I_{IO}\|$							nA
T_A = +25°C		–	2.0	15	–	2.0	25	
$T_A = T_{high}$		–	–	15	–	–	25	
$T_A = T_{low}$		–	–	40	–	–	40	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	15	50	–	15	50	
$T_A = T_{high}$		–	–	50	–	–	50	
$T_A = T_{low}$		–	–	120	–	–	100	
Input Resistance	R_{in}	–	5.0	–	–	5.0	–	MΩ
Input Capacitance	C_{in}	–	2.0	–	–	2.0	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	–	18	–	mV
Large Signal Voltage Gain	A_{vol}							V/V
$R_L \geq 5.0$ kΩ, V_O = ±1.0 V, T_A = +25°C		50 k	200 k	–	25 k	200 k	–	
$R_L \geq 5.0$ kΩ, V_O = 1.0 V, $T_{low} \leq T_A \leq T_{high}$		25 k	–	–	25 k	–	–	
Output Resistance	R_O	–	1.0	–	–	1.0	–	kΩ
Output Short-Circuit Current	I_{Osc}	–	5.0	–	–	5.0	–	mA
Supply Current	I_{CC}, I_{EE}							μA
T_A = +25°C		–	130	160	–	130	170	
$T_{low} \leq T_A \leq T_{high}$		–	–	180	–	–	180	
Power Dissipation	P_D							μW
T_A = +25°C		–	780	960	–	780	1020	
$T_{low} \leq T_A \leq T_{high}$		–	–	1080	–	–	1080	
Transient Response (Unity Gain)								
V_{in} = 20 mV, $R_L \geq 5.0$ kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	–	0.6	–	–	0.6	–	μs
Overshoot	OS	–	5.0	–	–	5.0	–	%
Slew Rate ($R_L \geq 5.0$ kΩ)	SR	–	0.35	–	–	0.35	–	V/μs
Output Voltage Swing	V_O							V
$R_L \geq 5.0$ kΩ, $T_{low} \leq T_A \leq T_{high}$		±1.9	±2.1	–	±2.0	±2.1	–	
Input Voltage Range	V_{ID}							V
$T_{low} \leq T_A \leq T_{high}$		±1.0	–	–	±1.0	–	–	
Common-Mode Rejection Ratio	CMRR							dB
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		70	86	–	70	86	–	
Supply Voltage Rejection Ratio	PSRR							μV/V
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		–	25	150	–	25	200	

*T_{low} = -55°C for MC1776
0°C for MC1776C

T_{high} = +125°C for MC1776
+70°C for MC1776C

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – SET CURRENT versus SET RESISTOR

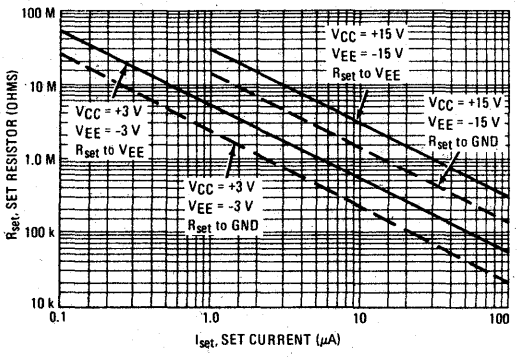


FIGURE 2 – POSITIVE STANDBY SUPPLY CURRENT versus SET CURRENT

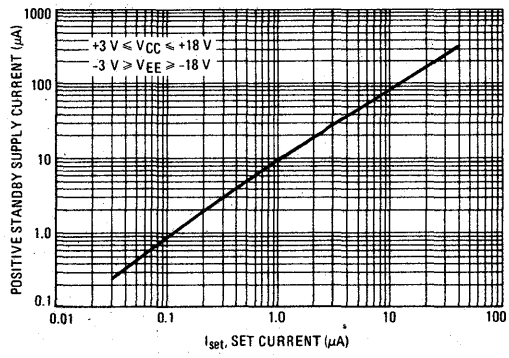


FIGURE 3 – OPEN-LOOP GAIN versus SET CURRENT

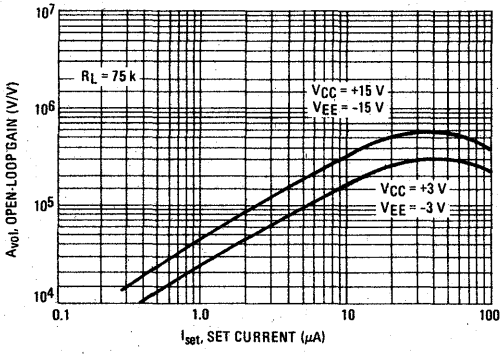


FIGURE 4 – INPUT BIAS CURRENT versus SET CURRENT

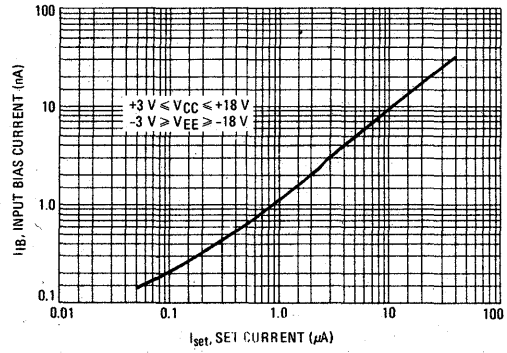


FIGURE 5 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

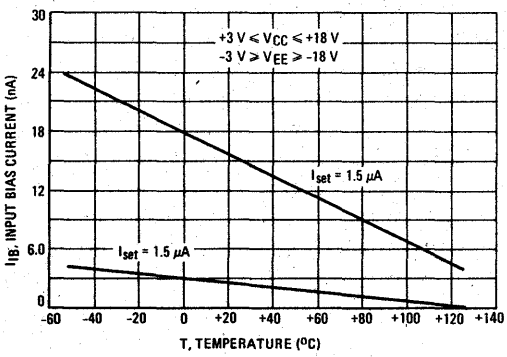
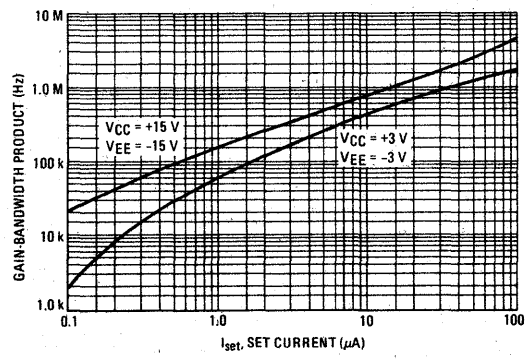


FIGURE 6 – GAIN-BANDWIDTH PRODUCT (GBW) versus SET CURRENT



3

TYPICAL CHARACTERISTICS (continued)

(T_A = +25°C unless otherwise noted.)

FIGURE 7 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

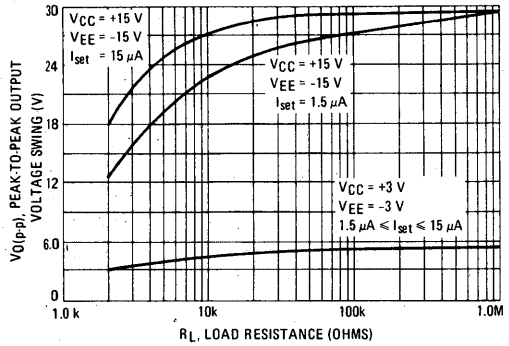


FIGURE 8 – SUPPLY CURRENT versus AMBIENT TEMPERATURE

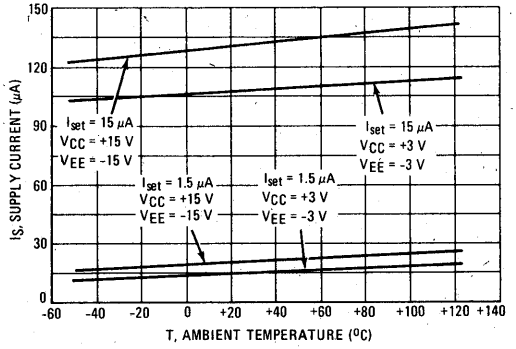


FIGURE 9 – OUTPUT SWING versus SUPPLY VOLTAGE

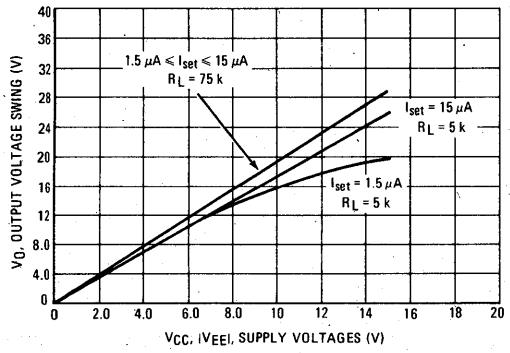


FIGURE 10 – SLEW RATE versus SET CURRENT

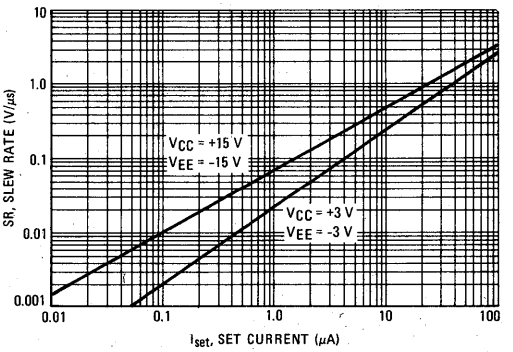


FIGURE 11 – INPUT NOISE VOLTAGE versus SET CURRENT

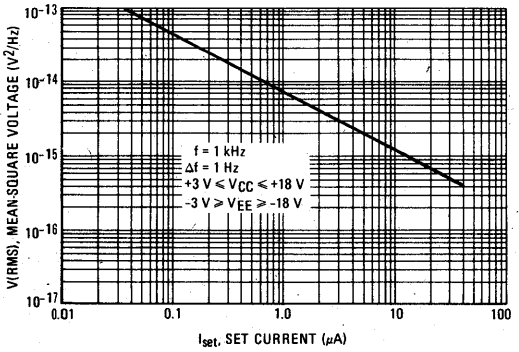
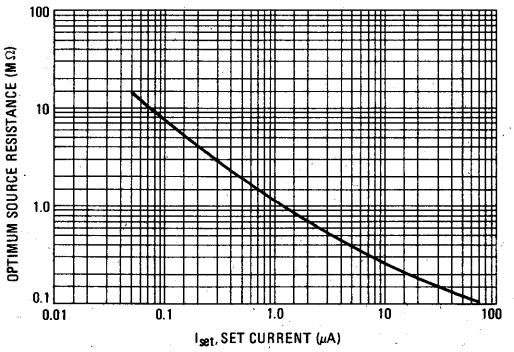
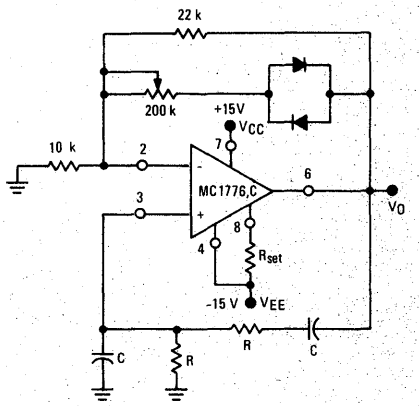


FIGURE 12 – OPTIMUM SOURCE RESISTANCE FOR MINIMUM NOISE versus SET CURRENT



APPLICATIONS INFORMATION

FIGURE 13 – WEIN BRIDGE OSCILLATOR

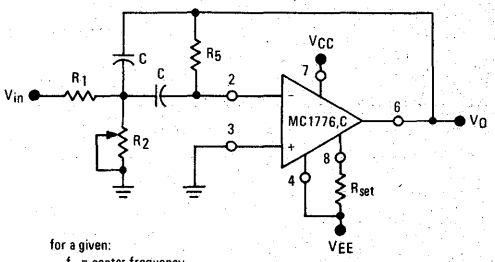


$$f_0 = \frac{1}{2\pi RC}$$

(for f_0 = 1.0 kHz)

R = 16 kΩ
C = 0.01 μF

FIGURE 14 – MULTIPLE FEEDBACK BANDPASS FILTER



for a given:
f_0 = center frequency
A (f_0) = Gain at center frequency
Q = quality factor
Choose a value for C, then

$$R5 = \frac{Q}{\pi f_0 C}$$

$$R1 = \frac{R5}{2A\,(f_0)}$$

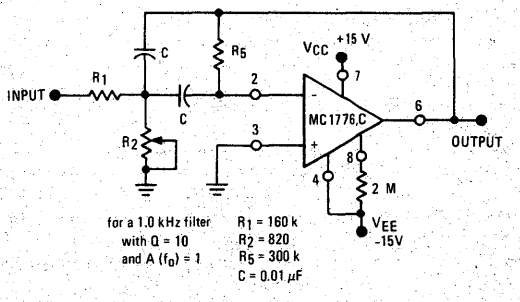
$$R2 = \frac{R1 \cdot R5}{4Q^2\,R1 - R5}$$

To obtain less than 10% error from the operational amplifier:

$$\frac{Q_0\, f_0}{GBW} \leq 0.1$$

where f_0 and GBW are expressed in Hz. GBW is available from Figure 6 as a function of Set Current, I_{set}.

FIGURE 15 – MULTIPLE FEEDBACK BANDPASS FILTER (1.0 kHz)



for a 1.0 kHz filter with Q = 10 and A (f_0) = 1

R_1 = 160 k
R_2 = 820
R_5 = 300 k
C = 0.01 μF

FIGURE 16 – GATED AMPLIFIER

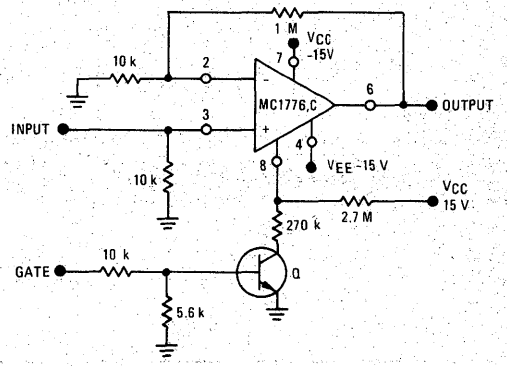
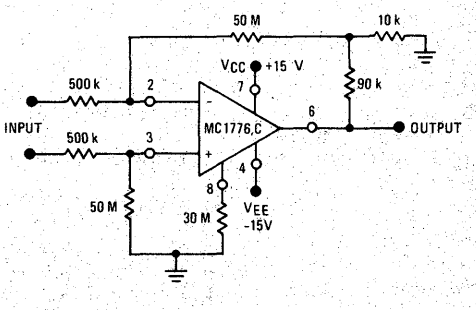


FIGURE 17 – HIGH INPUT IMPEDANCE AMPLIFIER



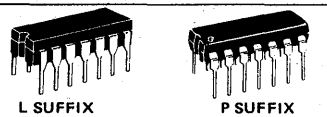
ORDERING INFORMATION

Device	Temperature Range	Package
MC3301L	−40°C to +85°C	Ceramic DIP
MC3301P	−40°C to +85°C	Plastic DIP

MC3301

QUAD OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

QUAD SINGLE-SUPPLY OPERATIONAL AMPLIFIER FOR AUTOMOTIVE APPLICATIONS

These internally compensated operational amplifiers are designed specifically for single positive power supply applications found in automotive and consumer electronics. Each MC3301 contains four independent amplifiers — making it ideal for automotive safety, pollution, and comfort controls. Some typical applications are tachometer, voltage regulator, logic circuits, power control and other similar usages.

- Wide Operating Temperature Range — -40 to +85°C
- Single-Supply Operation — +4.0 to +28 Vdc
- Internally Compensated
- Wide Unity Gain Bandwidth — 4.0 MHz typical
- Low Input Bias Current — 50 nA typical
- High Open-Loop Gain — 2000 V/V typical

FIGURE 1 — EQUIVALENT CIRCUIT

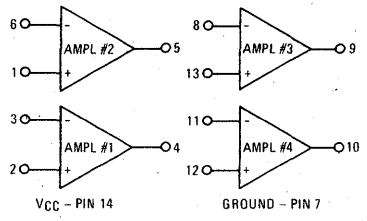
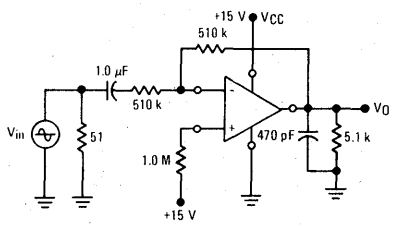


FIGURE 2 — SMALL-SIGNAL TRANSIENT RESPONSE



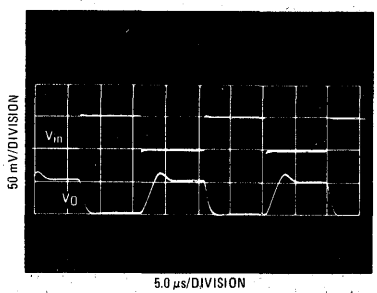


FIGURE 3 — INVERTING AMPLIFIER

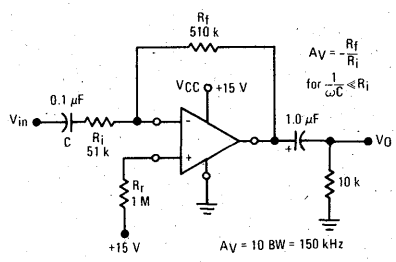
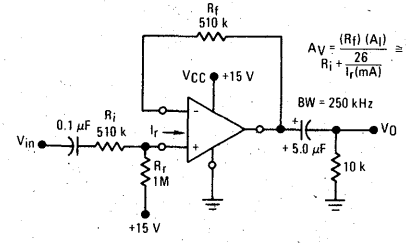


FIGURE 4 — NONINVERTING AMPLIFIER



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+28	Vdc
Noninverting Input Current	I_r	5.0	mA
Sink Current	I_{sink}	50	mA
Source Current	I_{source}	50	mA
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	625 5.0	mW mW/°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS [V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C (each amplifier) unless otherwise noted]

Characteristic	Fig.No.	Note	Symbol	Min	Typ	Max	Unit
Open-Loop Voltage Gain T_A = +25°C -40°C ≤ T_A ≤ +85°C	5		A_{vol}	 1000 –	 2000 1600	 – –	V/V
Quiescent Power Supply Current (Total for four amplifiers) Noninverting inputs open Noninverting inputs grounded	6	1	 I_{DO} I_{DG}	 – –	 6.9 7.8	 10 14	mAdc
Input Bias Current, R_L = ∞ T_A = +25°C -40°C ≤ T_A ≤ +85°C	7	2	I_{IB}	 – –	 50 100	 300 –	nAdc
Current Mirror Gain (I_r = 200 μAdc)	7	3	A_I	0.80	0.98	1.16	A/A
Current Mirror Gain Drift -40°C ≤ T_A ≤ +85°C				 –	 ±2.5	 –	%
Output Current Source Capability (V_{OH} = 0.4 Vdc) (V_{OH} = 9.0 Vdc) Sink Capability (V_{OL} = 0.4 Vdc)	8		 I_{source} I_{sink}	 3.0 – 0.5	 10 7.0 0.87	 – – –	mAdc
Output Voltage High Voltage Low Voltage (Inverting Input Driven) (Noninverting Input Driven)	6		 V_{OH} $V_{OL(inv)}$ $V_{OL(non)}$	 13.5 – –	 14.2 0.03 0.6	 – 0.1 –	Vdc
Input Resistance (Inverting input only)			R_{in}	0.1	1.0	–	Meg Ω
Slew Rate (C_L = 100 pF, R_L = 5.0 k)			SR	–	0.6	–	V/μs
Unity Gain Bandwidth		4	BW	–	4.0	–	MHz
Phase Margin		4	ϕm	–	70	–	Degrees
Power Supply Rejection (f = 100 Hz)			PSSR	–	55	–	dB
Channel Separation (f = 1.0 kHz)			e_{o1}/e_{o2}	–	65	–	dB

NOTES:

1. The quiescent current drain will increase approximately 0.3 mA for each inverting or noninverting input that is grounded.
2. Input bias current can be defined only for the inverting input. The noninverting input is not a true "differential input" – as with a conventional IC operational amplifier. As such this input does not have a requirement for input bias current.
3. Current mirror gain is defined as the current demanded at the inverting input divided by the current into the noninverting input.
4. Bandwidth and phase margin are defined with respect to the voltage gain from the inverting input to the output.

3

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted.)

FIGURE 5 – OPEN-LOOP VOLTAGE GAIN

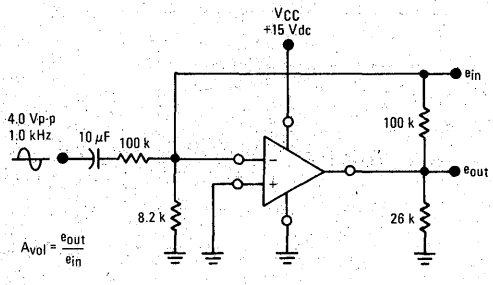
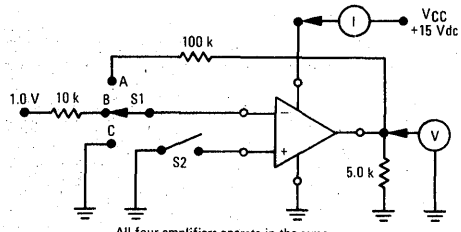


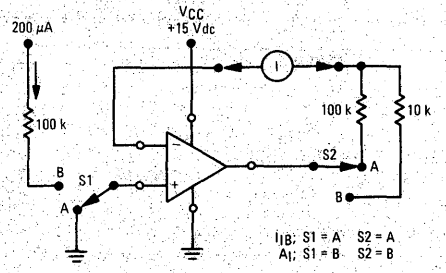
FIGURE 6 – QUIESCENT POWER SUPPLY CURRENT



All four amplifiers operate in the same configuration simultaneously.

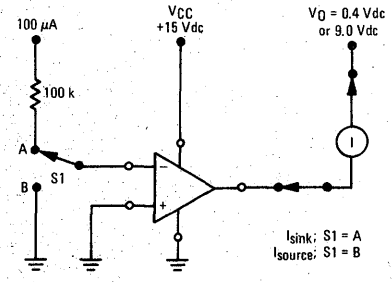
I_{DO}; S1 = A S2 = OPEN
I_{DG}; S1 = A S2 = CLOSED
$V_{OH}(-)$; S1 = C S2 = CLOSED
$V_{OL}(-)$; S1 = B S2 = CLOSED
$V_{OL}(+)$; S1 = A S2 = CLOSED

FIGURE 7 – INPUT BIAS CURRENT AND CURRENT MIRROR GAIN



I_{IB}; S1 = A S2 = A
A_I; S1 = B S2 = B

FIGURE 8 – OUTPUT CURRENT



I_{sink}; S1 = A
I_{source}; S1 = B

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted.)

FIGURE 9 – OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

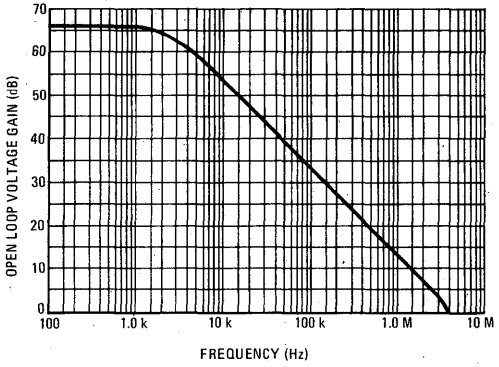


FIGURE 10 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

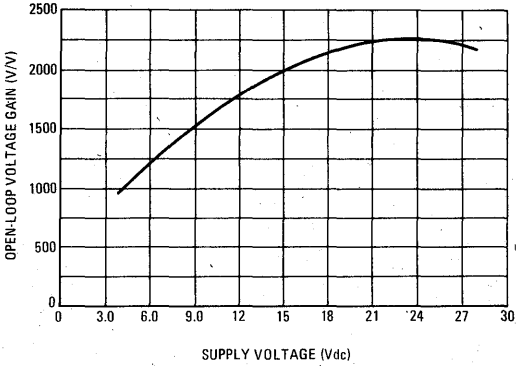


FIGURE 11 – OUTPUT RESISTANCE versus FREQUENCY

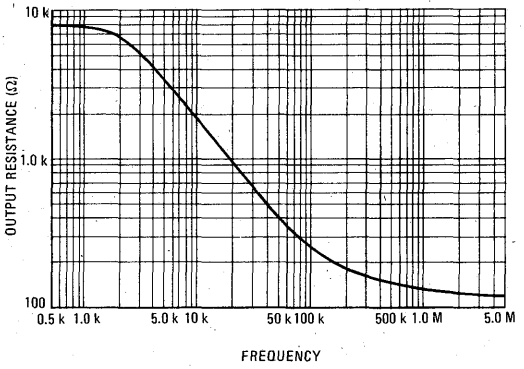


FIGURE 12 – SUPPLY CURRENT versus SUPPLY VOLTAGE

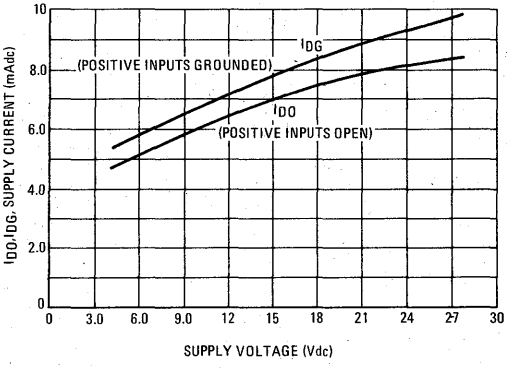


FIGURE 13 – LINEAR SOURCE CURRENT versus SUPPLY VOLTAGE

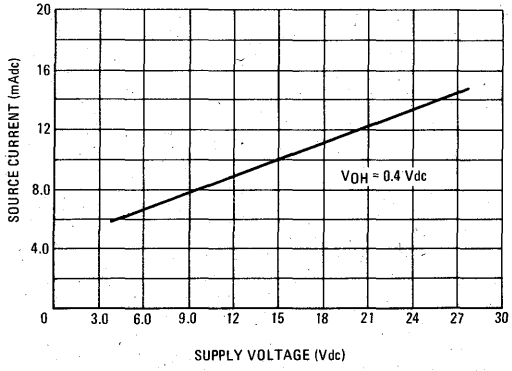
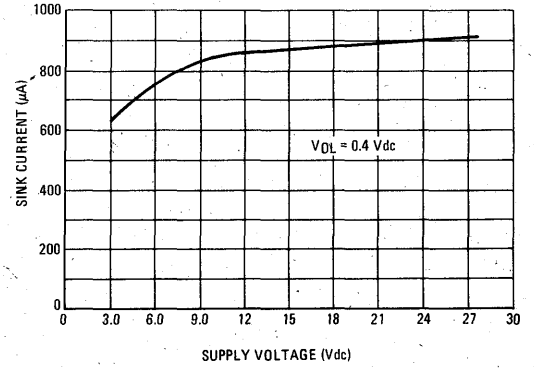


FIGURE 14 – LINEAR SINK CURRENT versus SUPPLY VOLTAGE

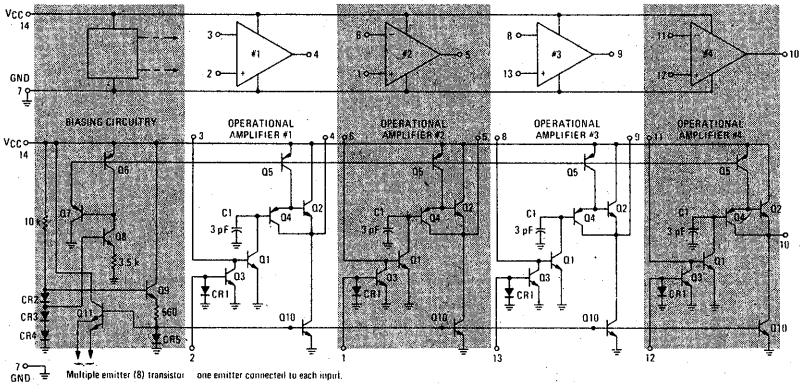


OPERATION AND APPLICATIONS

Basic Amplifier

The basic amplifier is the common emitter stage shown in Figures 15 and 16. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased class A by the current source I_2. The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled linear operation at the output. The sink current of the device can be forced to exceed the specified level by keeping the output dc voltage above ≈ 1.0 volt resulting in an increase in the distortion appearing at the output. Closed loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 18 on the following page. No external compensation is required.

FIGURE 15
BLOCK DIAGRAM



A noninverting input is obtained by adding a current mirror as shown in Figure 17. Essentially all current which enters the noninverting input, I_r, flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_r. Since the alpha current gain of Q3 ≈ 1, its collector current is approximately equal to I_r also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

FIGURE 16 – A BASIC GAIN STAGE

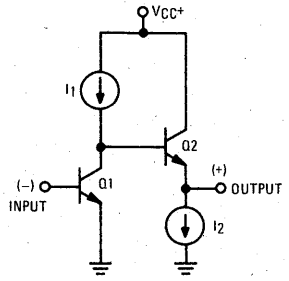
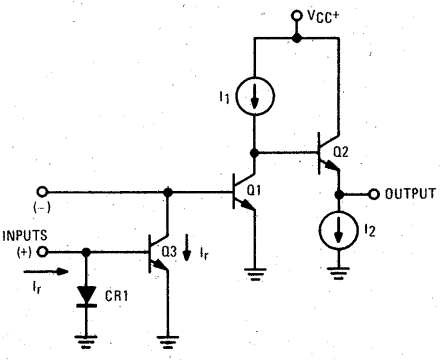


FIGURE 17 – OBTAINING A NONINVERTING INPUT



Biasing Circuitry

The circuitry common to all four amplifiers is shown in Figure 19, see next page. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, etc.) are set to the magnitude $V_{BE}/R1$ by transistor Q6. Transistor Q7 reduces base current loading. The voltage across resistor R2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5. The current thus set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage. Q11 (Figure 15) provides circuit protection from signals that are negative with respect to ground.

OPERATION AND APPLICATIONS (continued)

FIGURE 18 – A BASIC OPERATIONAL AMPLIFIER

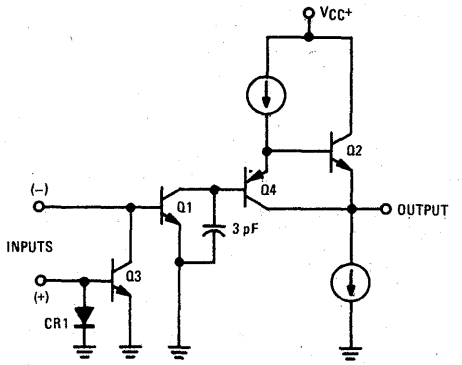
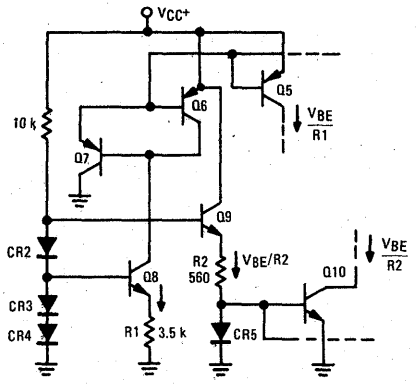


FIGURE 19 – BIASING CIRCUITRY



3

NORMAL DESIGN PROCEDURE

1. Output Q-Point Biasing

   A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing as shown in Figures 3 and 4 (see the first page of this specification). The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 10 μA to 200 μA range.

   B. V_{CC} Reference Voltage (see Figures 3 and 4)

   The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor, R_r, allowing the input current, I_r, to be within the range of 10 μA to 200 μA. Choosing the feedback resistor, R_f, to be equal to ½ R_r will now bias the amplifier output dc level to approximately $\frac{V_{CC}}{2}$. This allows the maximum dynamic range of the output voltage.

   C. Reference Voltage other than V_{CC} (see Figure 20)

   The biasing resistor R_r may be returned to a voltage (V_r) other than V_{CC}. By setting $R_f = R_r$, (still keeping I_r between 10 μA and 200 μA) the output dc level will be equal to V_r. The expression for determining V_{Odc} is:

$$V_{Odc} = \frac{(A_I)(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r} A_I\right) \phi$$

   where ϕ is the V_{BE} drop of the input transistors (approximately 0.6 Vdc @ +25°C and assumed equal). A_I is the current mirror gain.

2. Gain Determination

   A. Inverting Amplifier

   The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of

FIGURE 20 – INVERTING AMPLIFIER WITH ARBITRARY REFERENCE

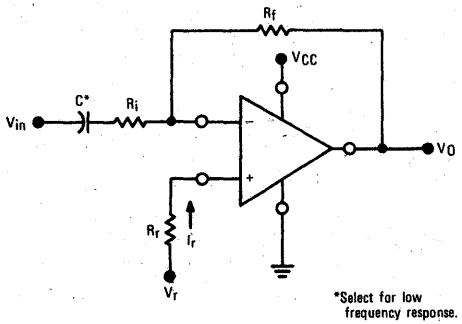
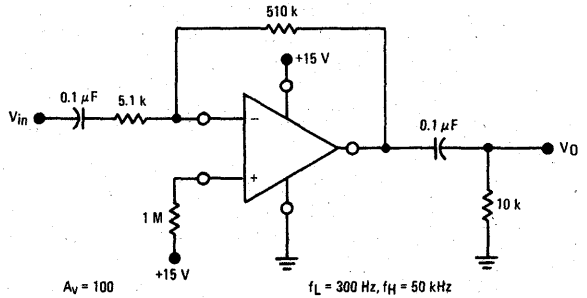


FIGURE 21 – INVERTING AMPLIFIER WITH A_v = 100 AND $V_r = V_{CC}$



NORMAL DESIGN PROCEDURE (continued)

I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier:

$$A_V = -\frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 4.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 400 kHz with 20 dB of closed loop gain or 40 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3.0 pF.

B. Noninverting Amplifier

The MC3301 may be used in the noninverting mode (see Figure 4, first page). The amplifier gain in this configuration is subject to the current mirror gain. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_r}$ ohms, where I_r is input current in milliamperes. The noninverting ac gain expression is given by:

$$A_V = \frac{(R_f)(A_I)}{R_i + \frac{26}{I_r\,(mA)}}$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For R_f = 510 kΩ the bandwidth will be in excess of 200 kHz for noninverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

TYPICAL APPLICATIONS

FIGURE 22 – TACHOMETER CIRCUIT

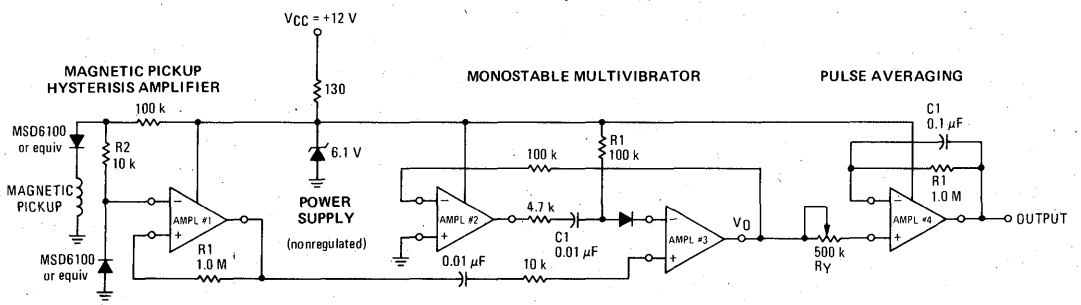


FIGURE 23 – VOLTAGE REGULATOR

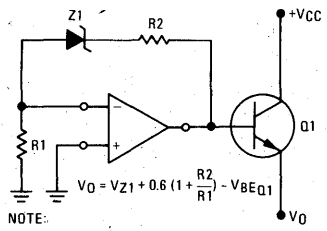
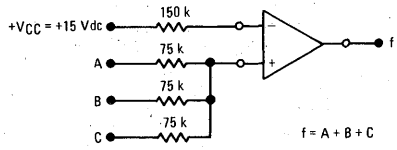


FIGURE 24 – LOGIC "OR" GATE



TYPICAL APPLICATIONS (continued)

FIGURE 25 – LOGIC "NAND" GATE (Large Fan-In)

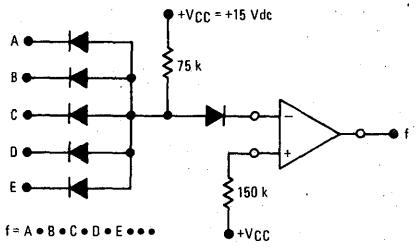


FIGURE 26 – LOGIC "NOR" GATE

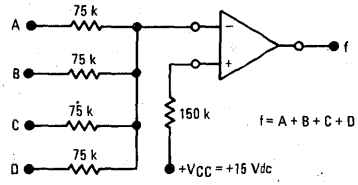


FIGURE 27 – R-S FLIP-FLOP

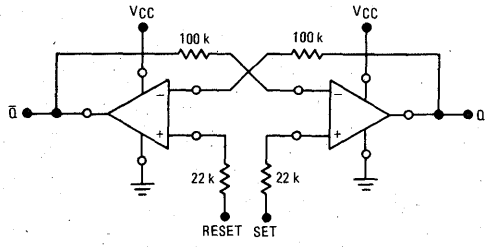


FIGURE 28 – ASTABLE MULTIVIBRATOR

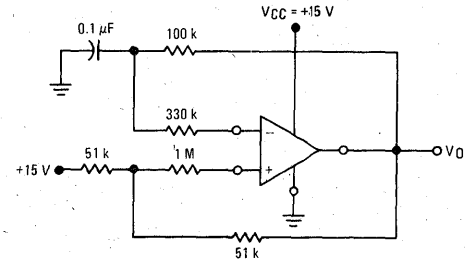


FIGURE 29 – POSITIVE-EDGE DIFFERENTIATOR

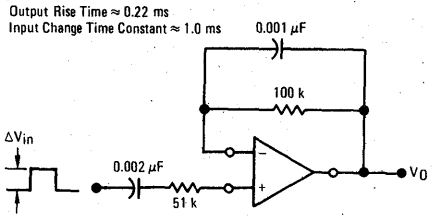
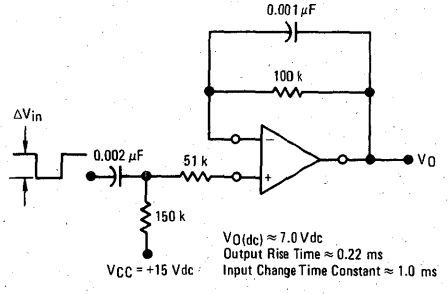


FIGURE 30 – NEGATIVE-EDGE DIFFERENTIATOR



ORDERING INFORMATION

Device	Temperature Range	Package
MC3401L	0°C to +70°C	Ceramic DIP
MC3401P	0°C to +70°C	Plastic DIP

MC3401

Specifications and Applications Information

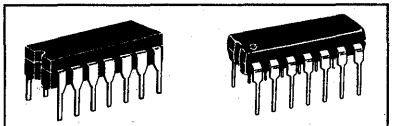
QUAD
OPERATIONAL AMPLIFIER
SILICON MONOLITHIC
INTEGRATED CIRCUIT

3

QUAD SINGLE-SUPPLY OPERATIONAL AMPLIFIER

These internally compensated operational amplifiers are designed specifically for single positive power supply applications found in industrial control systems and automotive electronics. Each MC3401 device contains four independent amplifiers — making it ideal for applications such as active filters, multi-channel amplifiers, tachometer, oscillator and other similar usages.

- Single-Supply Operation — +5.0 Vdc to +18 Vdc
- Internally Compensated
- Wide Unity Gain Bandwidth — 5.0 MHz typical
- Low Input Bias Current — 50 nA typical
- High Open-Loop Gain — 1000 V/V minimum



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

FIGURE 1 — EQUIVALENT CIRCUIT

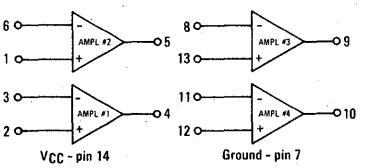


FIGURE 2 — SMALL-SIGNAL TRANSIENT RESPONSE

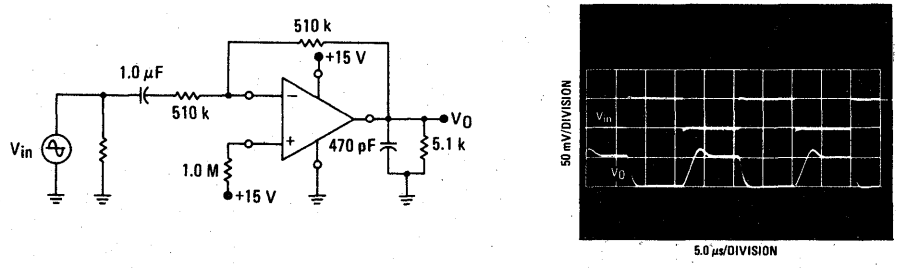


FIGURE 3 — INVERTING AMPLIFIER

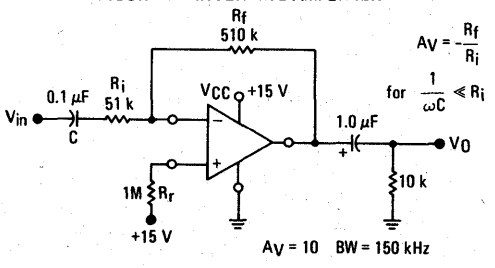
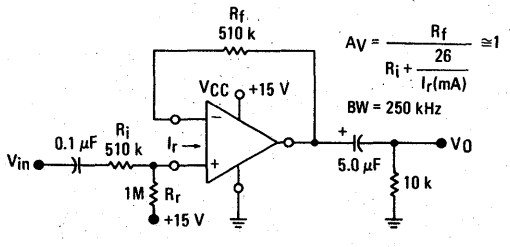


FIGURE 4 — NONINVERTING AMPLIFIER



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Non-inverting Input Current	I_{in}	5.0	mA
Power Dissipation Derate above T_A = +25°C	P_D	625 5.0	mW mW/°C
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS [V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C (each amplifier) unless otherwise noted]

Characteristic	Fig. No.	Note	Symbol	Min	Typ	Max	Unit
Open-Loop Voltage Gain	5,9,10	1	A_{vol}				V/V
T_A = +25°C				1000	2000	–	
0°C ≤ T_A ≤ +70°C				800	–	–	
Quiescent Power Supply Current (Total for four amplifiers)	6,12	2					mAdc
Noninverting inputs open			I_{DO}	–	6.9	10	
Noninverting inputs grounded			I_{DG}	–	7.8	14	
Input Bias Current, R_L = ∞	5	3	I_{IB}				nAdc
T_A = +25°C				–	50	300	
0°C ≤ T_A ≤ +70°C				–	–	500	
Output Current	5	4					mAdc
Source Capability	13		I_{source}	5.0	10	–	
Sink Capability	14		I_{sink}	0.5	1.0	–	
Output Voltage							Vdc
High Voltage	7	5	V_{OH}	13.5	14.2	–	
Low Voltage	7	5	V_{OL}	–	0.03	0.1	
Undistorted Output Swing (0°C < T_A < +70°C)	8	6	$V_{O(p-p)}$	10	13.5	–	$V_{(p-p)}$
Input Resistance	5		R_{in}	0.1	1.0	–	MEG Ω
Slew Rate (C_L = 100 pF, R_L = 5.0 k)			SR	–	0.6	–	V/μs
Unity Gain Bandwidth			BW	–	5.0	–	MHz
Phase Margin			ϕ_m	–	70	–	Degrees
Power Supply Rejection (f = 100 Hz)		7	PSSR	–	55	–	dB
Channel Separation (f = 1.0 kHz)			e_{o1}/e_{o2}	–	65	–	dB

NOTES

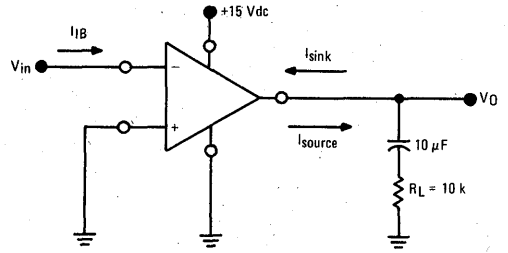
1. Open loop voltage gain is defined as the voltage gain from the inverting input to the output.
2. The quiescent current will increase approximately 0.3 mA for each noninverting input which is grounded. Leaving the noninverting input open causes the apparent input bias current to increase slightly (100 nA) at high temperatures.
3. Input bias current can be defined only for the inverting input. The noninverting input is not a true "differential input" – as with a conventional IC operational amplifier. As such this input does not have a requirement for input bias current.
4. Sink current is specified for linear operation. When the device is used as a gate or a comparator (non-linear operation), the sink capability of the device is approximately 5.0 milliamperes.
5. When used as a noninverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.
6. Peak-to-peak restrictions are due to the variations of the quiescent dc output voltage in the standard configuration (Figure 8).
7. Power supply rejection is specified at closed loop unity gain, and therefore indicates the supply rejection of both the biasing circuitry and the feedback amplifier.

3

SIMPLIFIED TEST CIRCUITS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted)

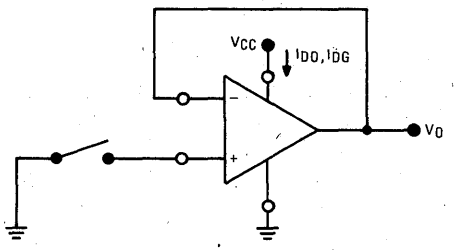
FIGURE 5 – OPEN-LOOP GAIN AND INPUT RESISTANCE (INPUT BIAS CURRENT, OUTPUT CURRENT)



$$R_{in} = \frac{\Delta V_{in}}{\Delta I_B} \quad A_{vol} = -\frac{\Delta V_O}{\Delta V_{in}}$$

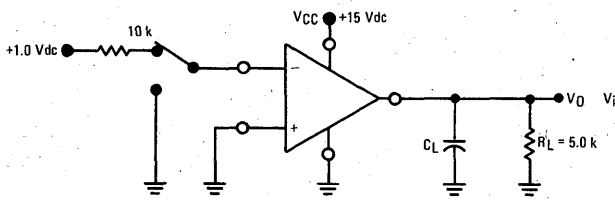
Amplifier must be biased (by V_{in}) in the linear operating region.

FIGURE 6 – QUIESCENT POWER SUPPLY CURRENT



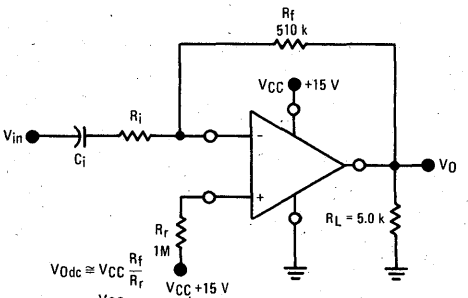
I_{DO} is total supply current with "+" input open.
I_{DG} is total supply current with "+" input grounded.

FIGURE 7 – OUTPUT VOLTAGE SWING



V_{OL} measured with "–" input biased up as shown.
V_{OH} measured with "–" input grounded.

FIGURE 8 – PEAK-TO-PEAK OUTPUT VOLTAGE



$$V_{Odc} \cong V_{CC}\frac{R_f}{R_r} \cong \frac{V_{CC}}{2}$$

for $R_r \cong 2R_f$

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, R_L = 5.0 kΩ, T_A = +25°C
[each amplifier] unless otherwise noted.)

FIGURE 9 – OPEN-LOOP VOLTAGE GAIN versus FREQUENCY

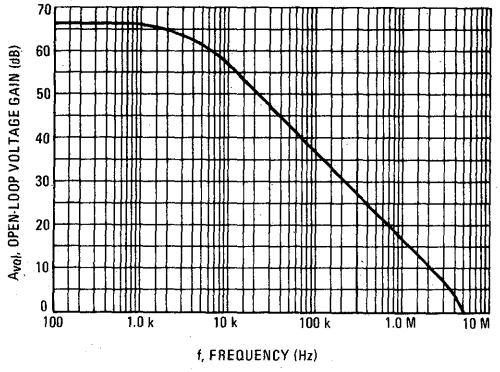


FIGURE 10 – OPEN-LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

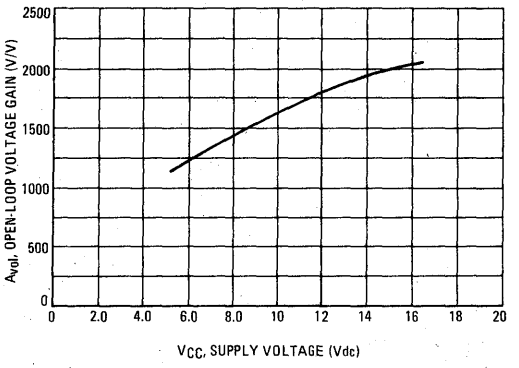


FIGURE 11 – OUTPUT RESISTANCE versus FREQUENCY

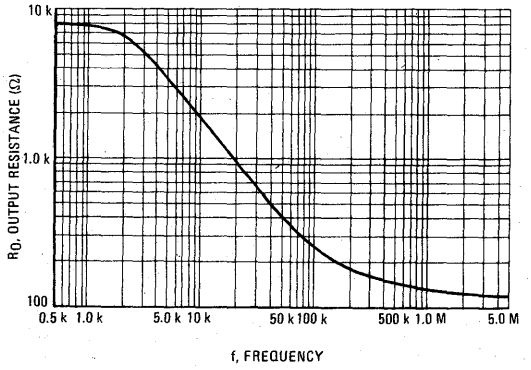


FIGURE 12 – SUPPLY CURRENT versus SUPPLY VOLTAGE

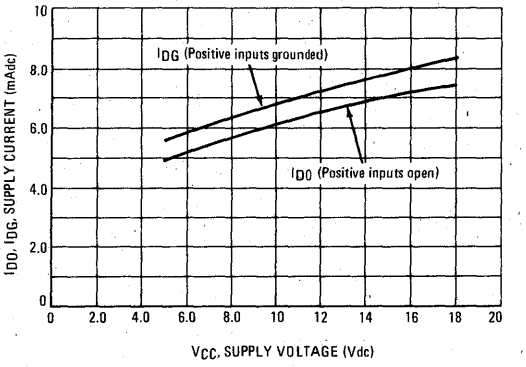


FIGURE 13 – LINEAR SOURCE CURRENT versus SUPPLY VOLTAGE

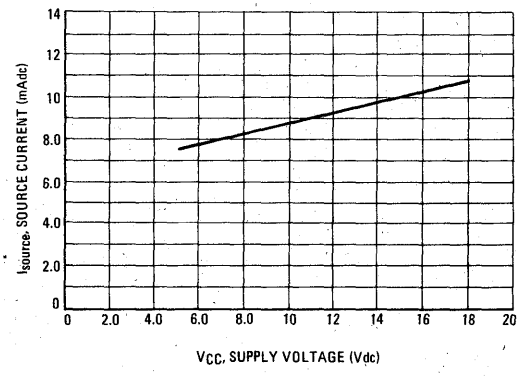
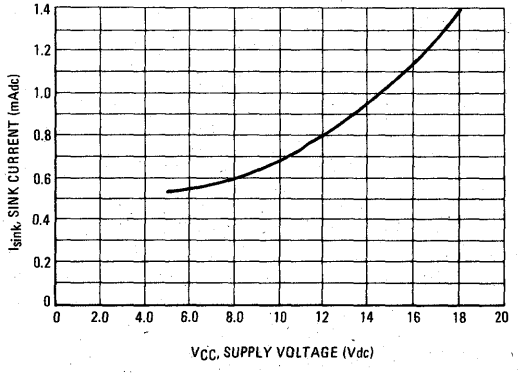


FIGURE 14 – LINEAR SINK CURRENT versus SUPPLY VOLTAGE

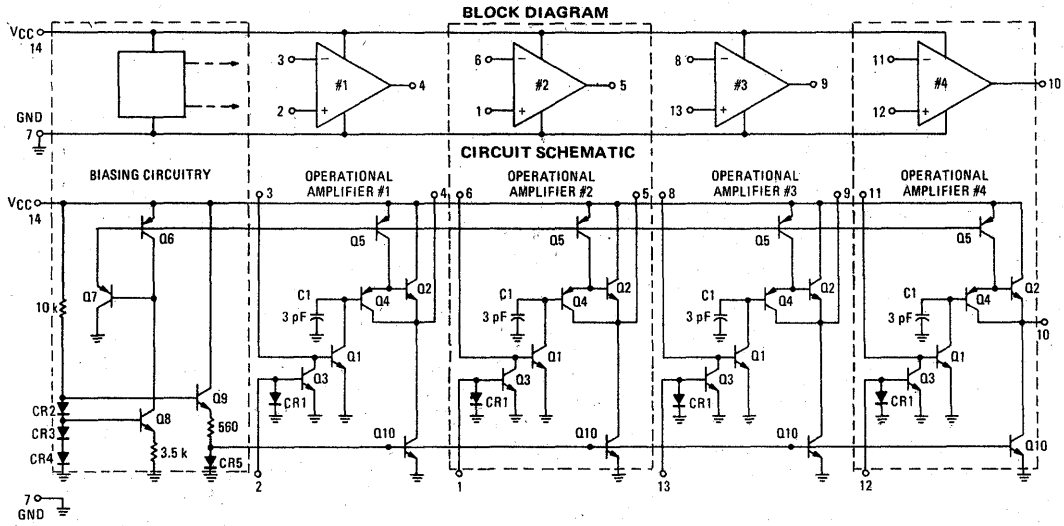


OPERATION AND APPLICATIONS

Basic Amplifier

The basic amplifier is the common emitter stage shown in Figures 15 and 16. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased class A by the current source I_2. The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled linear operation at the output. The sink current of the device can be forced to exceed the specified level with an increase in the distortion appearing at the output. Closed loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 18. No external compensation is required.

FIGURE 15



A noninverting input is obtained by adding a current mirror as shown in Figure 17. Essentially all current which enters the noninverting input, I_{in2}, flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_{in2}. Since the alpha current gain of Q3 $\approx$ 1, its collector current $\approx I_{in2}$ also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

FIGURE 16 – A BASIC GAIN STAGE

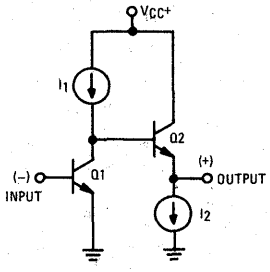
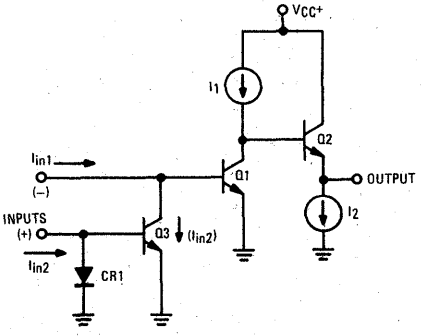


FIGURE 17 – OBTAINING A NONINVERTING INPUT



Biasing Circuitry

The circuitry common to all four amplifiers is shown in Figure 19. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, etc.) are set to the magnitude $V_{BE}/R1$ by transistor Q6. Transistor Q7 reduces base current loading. The voltage across resistor R2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5. The current thus set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage.

OPERATION AND APPLICATIONS (continued)

FIGURE 18 – A BASIC OPERATIONAL AMPLIFIER

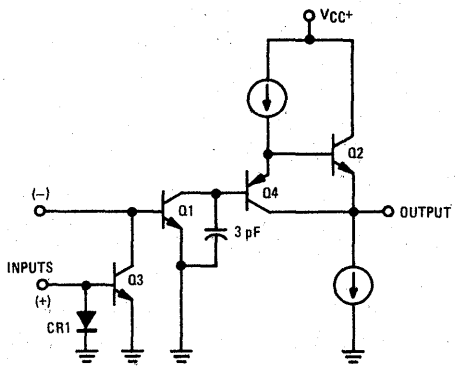
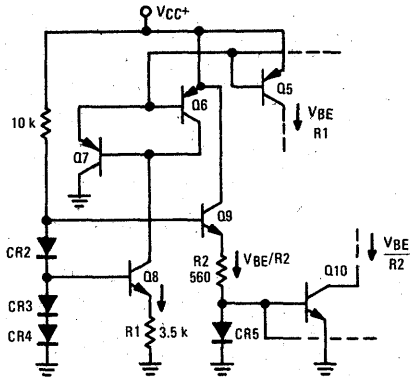


FIGURE 19 – BIASING CIRCUITRY



NORMAL DESIGN PROCEDURE

1. Output Q-Point Biasing
   A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing as shown in Figures 3 and 4. The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 5 μA to 100 μA range.
   B. V_{CC} Reference Voltage (see Figures 3 and 4)
   The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor, R_r, allowing the input current, I_r, to be within the range of 5 μA to 100 μA. Choosing the feedback resistor, R_f, to be equal to ½ R_r will now bias the amplifier output dc level to approximately $\frac{V_{CC}}{2}$. This allows for maximum dynamic range of the output voltage.
   C. Reference Voltage other than V_{CC} (See Figure 20).
   The biasing resistor R_r may be returned to a voltage (V_r) other than V_{CC}. By setting $R_f = R_r$, (still keeping I_r between 5 μA and 100 μA) the output dc level will be equal to V_r. Neglecting error terms, the expression for determining V_{Odc} is:

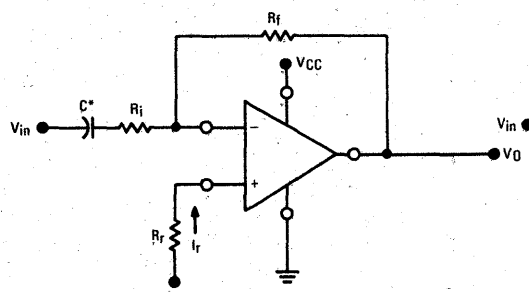
$$V_{Odc} = \frac{(V_r)\ (R_f)}{R_r} + \left(1 - \frac{R_f}{R_r}\right)\phi$$

where ϕ is the V_{BE} drop of the input transistors (approximately 0.7 Vdc @ +25°C).

The error terms not appearing in the above equation can cause the dc operating point to vary up to 20% from the expected value. Error terms are minimized by setting the input current within the range of 5 μA to 100 μA.

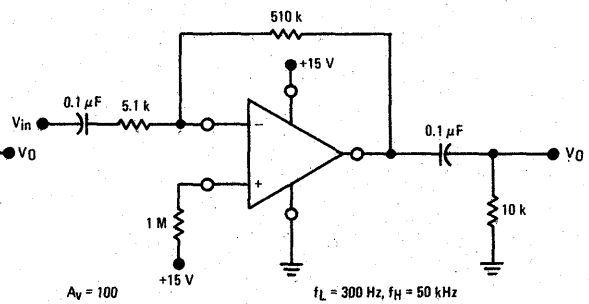
2. Gain Determination
   A. Inverting Amplifier
   The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of

FIGURE 20 – INVERTING AMPLIFIER WITH ARBITRARY REFERENCE



$$V_O \approx \frac{V_r R_f}{R_r} + \left(1 - \frac{R_f}{R_r}\right)\phi$$

FIGURE 21 – INVERTING AMPLIFIER WITH $A_v = 100$ AND $V_r = V_{CC}$



NORMAL DESIGN PROCEDURE (continued)

I_{sink} becomes a limitation with respect to the load driving capabilities of the device. The limitation is less severe if the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier:

$$A_V = -\frac{R_f}{R_i}$$

The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 5.0 MHz and with the gain roll-off at 20 dB per decade, bandwidth will typically be 500 kHz with 20 dB of closed loop gain or 50 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3.0 pF.

B. Noninverting Amplifier

Although recommended as an inverting amplifier, the MC 3401 may be used in the noninverting mode (see Figure 4). The amplifier gain in this configuration is subject to the same error terms that affect the output Q point biasing so the gain may deviate as much as ±20% from that expected. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_r}$ ohms, where I_r is input current in milliamperes. The noninverting gain expression is given by:

$$A_V = \frac{R_f}{R_i + \frac{26}{I_r\,(mA)}} \quad \pm 20\%.$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For, R_f = 510 kΩ the bandwidth will be in excess of 200 kHz for noninverting gains of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the input resistor is effectively isolated from the feedback loop.

TYPICAL APPLICATIONS

FIGURE 22 – AMPLIFIER AND DRIVER FOR A 50-OHM LINE

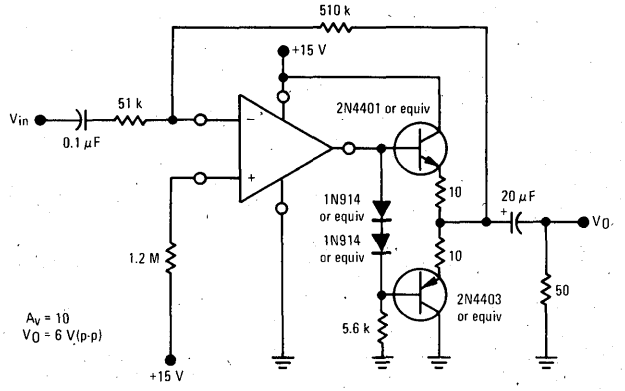
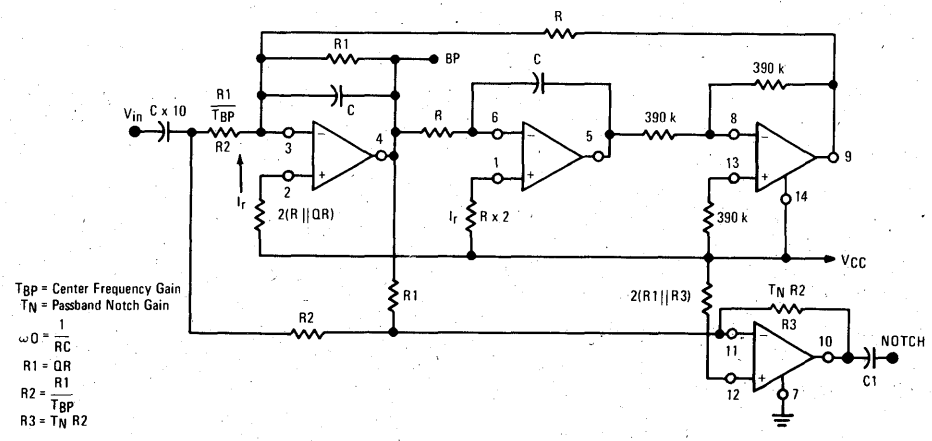


FIGURE 23 – BASIC BANDPASS AND NOTCH FILTER



TYPICAL APPLICATIONS (continued)

FIGURE 24 – BANDPASS AND NOTCH FILTER

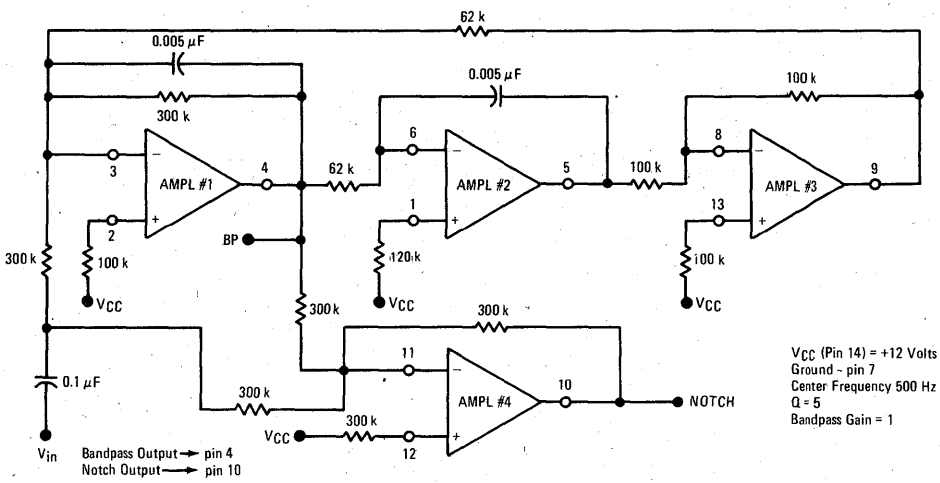
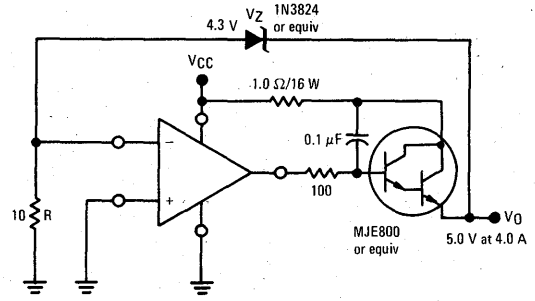


FIGURE 25 – VOLTAGE REGULATOR

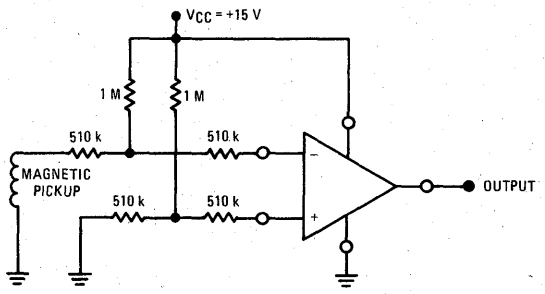


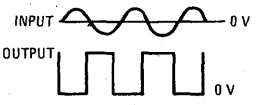
$V_O = V_Z + 0.6$ Vdc

NOTE 1: R is used to bias the zener.

NOTE 2: If the Zener TC is positive, and equal in magnitude to the negative TC of the input to the operational amplifier (≈ 2.0 mV/°C), the output is zero-TC. A 7.0-Volt Zener will give approximately zero-TC.

FIGURE 26 – ZERO CROSSING DETECTOR





ORDERING INFORMATION

Device	Temperature Range	Package
MC3303L	−40°C to +85°C	Ceramic DIP
MC3303P	−40°C to +85°C	Plastic DIP
MC3403L	0°C to +70°C	Ceramic DIP
MC3403P	0°C to +70°C	Plastic DIP
MC3503L	−55°C to +125°C	Ceramic DIP

MC3403P,L
MC3503L
MC3303P,L

Specifications and Applications Information

3

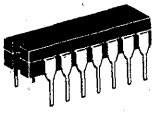
QUAD LOW POWER OPERATIONAL AMPLIFIERS

The MC3503 is a low-cost, quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular MC1741. However, the MC3503 has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 Volts or as high as 36 Volts with quiescent currents about one third of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

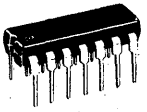
- Short Circuit Protected Outputs
- Class AB Output Stage for Minimal Crossover Distortion
- True Differential Input Stage
- Single Supply Operation: 3.0 to 36 Volts
- Split Supply Operation: ±1.5 to ±18 Volts
- Low Input Bias Currents: 500 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- Similar Performance to Popular MC1741

QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

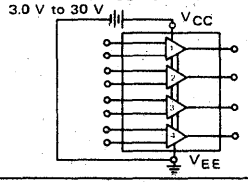


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

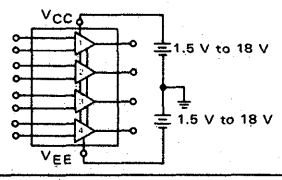


P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC3403 and MC3303 only)

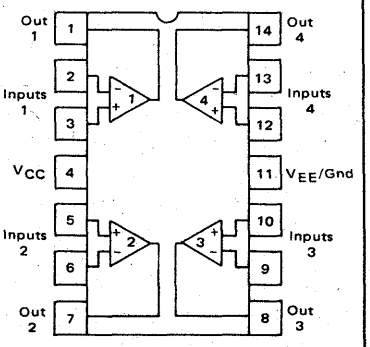
SINGLE SUPPLY



SPLIT SUPPLIES



PIN CONNECTIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages			Vdc
Single Supply	V_{CC}	36	
Split Supplies	V_{CC}	+18	
	V_{EE}	-18	
Input Differential Voltage Range (1)	V_{IDR}	±30	Vdc
Input Common Mode Voltage Range (1) (2)	V_{ICR}	±15	Vdc
Storage Temperature Range	T_{stg}		°C
Ceramic Package		-65 to +150	
Plastic Package		-55 to +125	
Operating Ambient Temperature Range	T_A		°C
MC3503		-55 to +125	
MC3403		0 to +70	
MC3303		-40 to +85	
Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	

(1) Split Power Supplies.
(2) For Supply Voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V for MC3503, MC3403, V_{CC} = +14 V, V_{EE} = Gnd for MC3303. T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC3503			MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	–	2.0	8.0	mV
$T_A = T_{high}$ to T_{low} (1)		–	–	6.0	–	–	12	–	–	10	
Input Offset Current	I_{IO}	–	30	50	–	30	50	–	30	75	nA
$T_A = T_{high}$ to T_{low}		–	–	200	–	–	200	–	–	250	
Large Signal Open-Loop Voltage Gain	A_{VOL}										V/mV
V_O = ±10 V, R_L = 2.0 kΩ,		50	200	–	20	200	–	20	200	–	
$T_A = T_{high}$ to T_{low}		25	300	–	15	–	–	15	–	–	
Input Bias Current	I_{IB}	–	-200	-500	–	-200	-500	–	-200	-500	nA
$T_A = T_{high}$ to T_{low}		–	-300	-1500	–	–	-800	–	–	-1000	
Output Impedance f = 20 Hz	z_o	–	75	–	–	75	–	–	75	–	Ω
Input Impedance f = 20 Hz	z_i	0.3	1.0	–	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Range	V_{OR}										V
R_L = 10 kΩ		±12	±13.5	–	±12	±13.5	–	+12	+12.5	–	
R_L = 2.0 kΩ		±10	±13	–	±10	±13	–	+10	+12	–	
R_L = 2.0 kΩ, $T_A = T_{high}$ to T_{low}		±10	–	–	±10	–	–	+10	–	–	
Input Common-Mode Voltage Range	V_{ICR}	+13 V -V_{EE}	+13.5 V -V_{EE}	–	+13 V -V_{EE}	+13.5V -V_{EE}	–	+13V -V_{EE}	+13.5V -V_{EE}	–	V
Common-Mode Rejection Ratio $R_S \leq 10$ kΩ	CMRR	70	90	–	70	90	–	70	90	–	dB
Power Supply Current (V_o = 0) R_L = ∞	I_{CC},I_{EE}	–	2.8	4.0	–	2.8	7.0	–	2.8	7.0	mA
Individual Output Short-Circuit Current (2)	$I_{OS±}$	±10	±30	±45	±10	±20	±45	±10	±30	±45	mA
Positive Power Supply Rejection Ratio	PSRR+	–	30	150	–	30	150	–	30	150	μV/V
Negative Power Supply Rejection Ratio	PSRR-	–	30	150	–	30	150	–	–	–	μV/V
Average Temperature Coefficient of Input Offset Current $T_A = T_{high}$ to T_{low}	$\Delta I_{IO}/\Delta T$	–	50	–	–	50	–	–	50	–	pA/°C
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{high}$ to T_{low}	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	μV/°C
Power Bandwidth A_V = 1, R_L = 2.0 kΩ, V_o = 20 V(p-p), THD = 5%	BWp	–	9.0	–	–	9.0	–	–	9.0	–	kHz
Small-Signal Bandwidth A_V = 1, R_L = 10 kΩ, V_o = 50 mV	BW	–	1.0	–	–	1.0	–	–	1.0	–	MHz
Slew Rate A_V = 1, V_i = -10 V to +10 V	SR	–	0.6	–	–	0.6	–	–	0.6	–	V/μs
Rise Time A_V = 1, R_L = 10 kΩ, V_o = 50 mV	t_{TLH}	–	0.35	–	–	0.35	–	–	0.35	–	μs
Fall Time A_V = 1, R_L = 10 kΩ, V_o = 50 mV	t_{THL}	–	0.35	–	–	0.35	–	–	0.35	–	μs
Overshoot A_V = 1, R_L = 10 kΩ, V_o = 50 mV	OS	–	20	–	–	20	–	–	20	–	%
Phase Margin A_V = 1, R_L = 2.0 kΩ, C_L = 200 pF	φm	–	60	–	–	60	–	–	60	–	Degrees
Crossover Distortion (V_{in} = 30 mVp-p, V_{out} = 2.0 Vp-p, f = 10 kHz)	–	–	1.0	–	–	1.0	–	–	1.0	–	%

(1) T_{high} = 125°C for MC3503, 70°C for MC3403, 85°C for MC3303
T_{low} = -55°C for MC3503, 0°C for MC3403, -40°C for MC3303

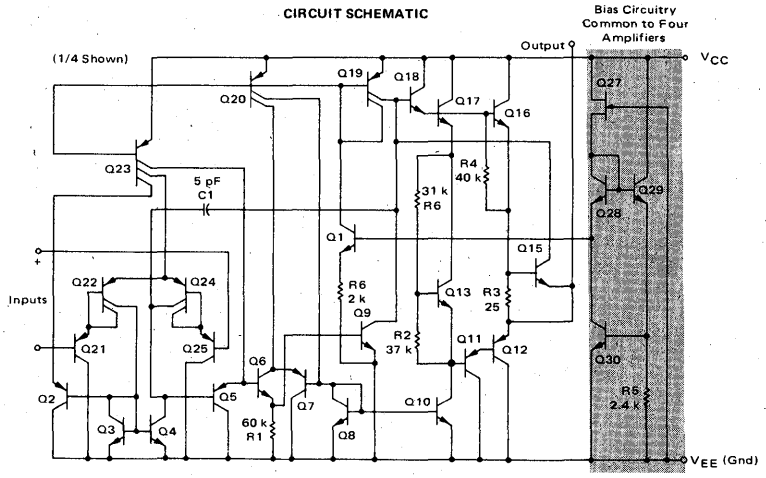
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC3503			MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	–	–	10	mV
Input Offset Current	I_{IO}	–	30	50	–	30	50	–	–	75	nA
Input Bias Current	I_{IB}	–	-200	-500	–	-200	-500	–	–	-500	nA
Large-Signal Open-Loop Voltage Gain R_L = 2.0 kΩ	A_{VOL}	20	200	–	20	200	–	20	200	–	V/mV
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	–	–	150	μV/V
Output Voltage Range (3)	V_{OR}										Vp-p
R_L = 10 kΩ, V_{CC} = 5.0 V		3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	
R_L = 10 kΩ, 5.0 V ≤ V_{CC} ≤ 30 V		V_{CC}-1.7	V_{CC}-1.5	–	V_{CC}-1.7	V_{CC}-1.5	–	V_{CC}-1.7	V_{CC}-1.5	–	
Power Supply Current	I_{CC}	–	2.5	4.0	–	2.5	7.0	–	2.5	7.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	–	–	-120	–	–	-120	–	–	-120	–	dB

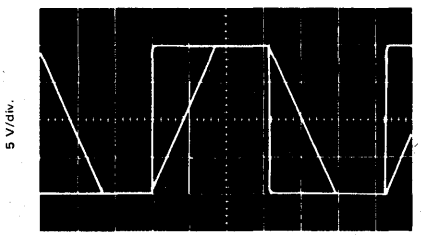
(2) Not to exceed maximum package power dissipation.
(3) Output will swing to ground

3

CIRCUIT SCHEMATIC



INVERTER PULSE RESPONSE



CIRCUIT DESCRIPTION

The MC3503/3403/3303 is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

TYPICAL PERFORMANCE CURVES

FIGURE 1 – SINE WAVE RESPONSE

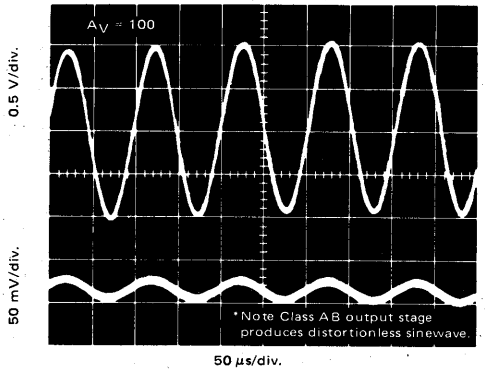


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

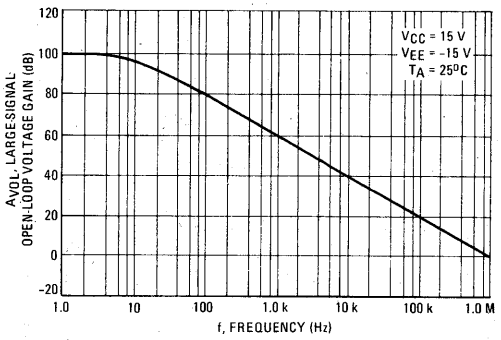


FIGURE 3 – POWER BANDWIDTH

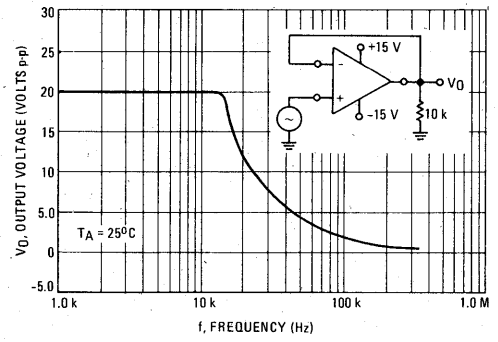


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

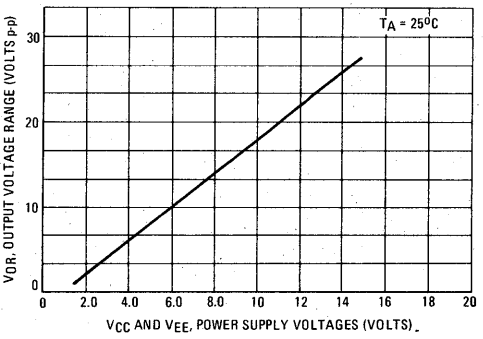


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

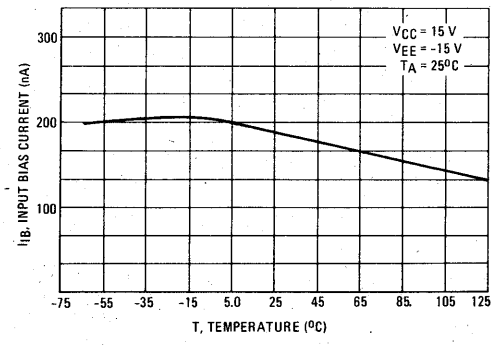
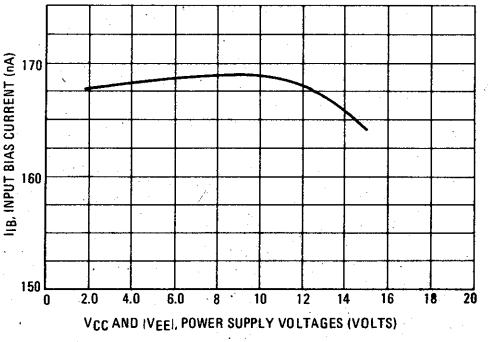


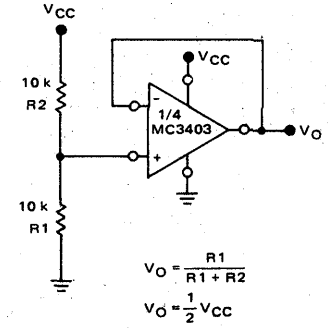
FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



3

APPLICATIONS INFORMATION

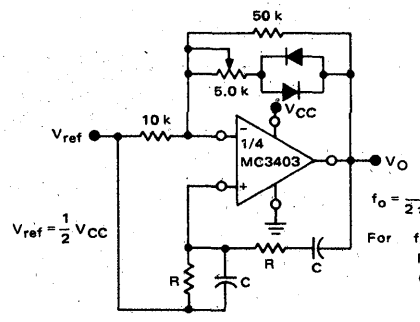
FIGURE 7 – VOLTAGE REFERENCE



$$V_O = \frac{R1}{R1 + R2}$$

$$V_O = \frac{1}{2} V_{CC}$$

FIGURE 8 – WEIN BRIDGE OSCILLATOR

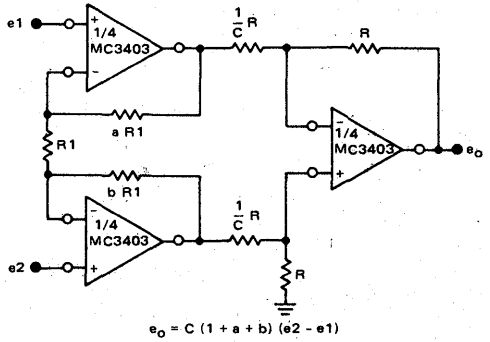


$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_o = \frac{1}{2 \pi RC}$$

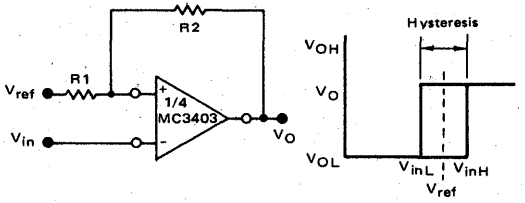
For f_o = 1 kHz
R = 16 kΩ
C = 0.01 μF

FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



$$e_o = C (1 + a + b) (e2 - e1)$$

FIGURE 10 – COMPARATOR WITH HYSTERESIS

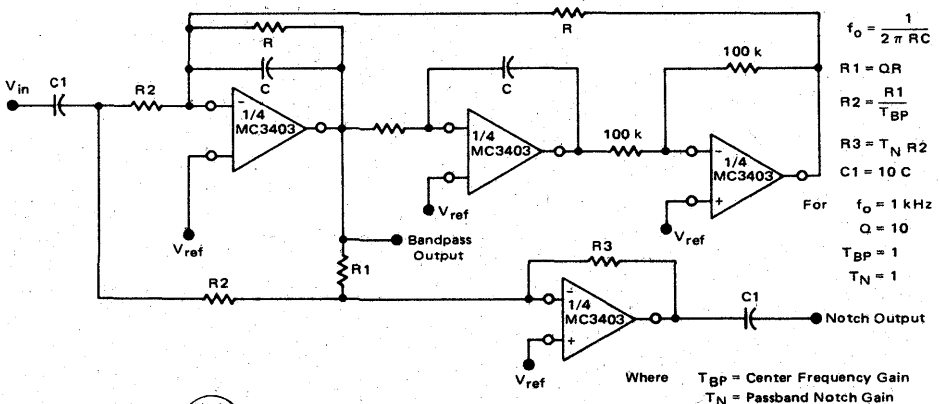


$$V_{inL} = \frac{R1}{R1 + R2} (V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2} (V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$$

FIGURE 11 – BI-QUAD FILTER



$$f_o = \frac{1}{2 \pi RC}$$

R1 = QR

$$R2 = \frac{R1}{T_{BP}}$$

$R3 = T_N R2$

C1 = 10 C

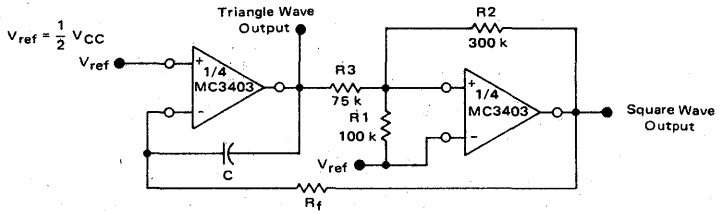
$$V_{ref} = \frac{1}{2} V_{CC}$$

For f_o = 1 kHz
Q = 10
T_{BP} = 1
T_N = 1

R = 160 kΩ
C = 0.001 μF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

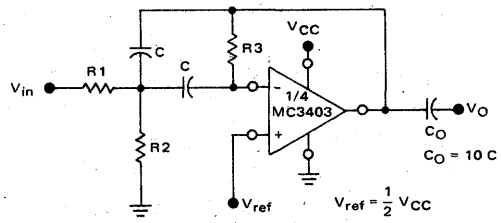
Where T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

FIGURE 12 – FUNCTION GENERATOR



$$f = \frac{R1 + R_C}{4 C R_f R1} \quad \text{if} \quad R3 = \frac{R2\ R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then:

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2 A(f_o)}$$

$$R2 = \frac{R1\ R5}{4Q^2 R1 - R5}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{BW} < 0.1$$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

ORDERING INFORMATION

Device	Temperature Range	Package
MC3358P1	−40°C to +85°C	Plastic DIP
MC3458G	0°C to +70°C	Metal Can
MC3458P1	0°C to +70°C	Plastic DIP
MC3458U	0°C to +70°C	Ceramic DIP
MC3558G	−55°C to +125°C	Metal Can
MC3558U	−55°C to +125°C	Ceramic DIP

MC3458
MC3558
MC3358

Specifications and Applications Information

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

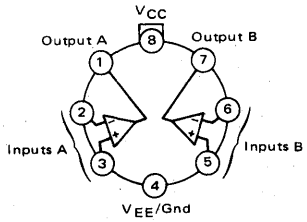
DUAL LOW POWER OPERATIONAL AMPLIFIERS

Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, 3) Single Supply or Split Supply operation and 4) pin outs compatible with the popular MC1558 dual operational amplifier. The MC3558 Series is equivalent to one-half of a MC3503.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 Volts or as high as 36 Volts with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

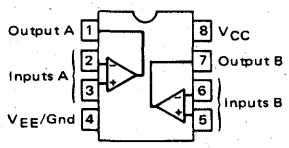
- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 36 Volts
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Class AB Output Stage for Minimum Crossover Distortion
- Single and Split Supply Operations Available
- Similar Performance to the Popular MC1558

G SUFFIX
METAL PACKAGE
CASE 601



P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC3458, MC3358 only)

U SUFFIX
CERAMIC PACKAGE
CASE 693



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC} V_{EE}	 36 +18 −18	Vdc
Input Differential Voltage Range (1)	V_{IDR}	±30	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	±15	Vdc
Input Forward Current (V_I < -0.3 V)	I_{IF}	50	mA
Junction Temperature Ceramic and Metal Packages Plastic Package	T_J	 175 150	°C
Storage Temperature Range Ceramic and Metal Packages Plastic Package	T_{stg}	 -65 to +150 -55 to +125	°C
Operating Ambient Temperature Range MC3558 MC3458 MC3358	T_A	 -55 to +125 0 to +70 -40 to +85	°C

(1) Split Power Supplies.
(2) For Supply Voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (For MC3558, MC3458, V_{CC} = +15 V, V_{EE} = -15 V, T_A = 25°C unless otherwise noted.) (For MC3358, V_{CC} = +14 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC3558			MC3458			MC3358			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $T_A = T_{high}$ to T_{low} (1)	V_{IO}	–	2.0	5.0	–	2.0	10	–	2.0	8.0	mV
		–	–	6.0	–	–	12	–	–	10	
Input Offset Current $T_A = T_{high}$ to T_{low}	I_{IO}	–	30	50	–	30	50	–	30	75	nA
		–	–	200	–	–	200	–	–	250	
Large Signal Open-Loop Voltage Gain V_O = ±10 V, R_L = 2.0 kΩ, $T_A = T_{high}$ to T_{low}	A_{VOL}	50	200	–	20	200	–	20	200	–	V/mV
		25	300	–	15	–	–	15	–	–	
Input Bias Current $T_A = T_{high}$ to T_{low}	I_{IB}	–	-200	-500	–	-200	-500	–	-200	-500	nA
		–	-300	-1500	–	–	-800	–	–	-1000	
Output Impedance f = 20 Hz	z_o	–	75	–	–	75	–	–	75	–	Ω
Input Impedance f = 20 Hz	z_i	0.3	1.0	–	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Range R_L = 10 kΩ R_L = 2.0 kΩ R_L = 2.0 kΩ, $T_A = T_{high}$ to T_{low}	V_{OR}	±12	±13.5	–	±12	±13.5	–	12	12.5	–	V
		±10	±13	–	±10	±13	–	10	12	–	
		±10	–	–	±10	–	–	10	–	–	
Input Common-Mode Voltage Range	V_{ICR}	+13 V -V_{EE}	+13.5 V -V_{EE}	–	+13 V -V_{EE}	+13.5V -V_{EE}	–	+12 V -V_{EE}	+12.5V -V_{EE}	–	V
Common-Mode Rejection Ratio $R_S \leq$ 10 kΩ	CMRR	70	90	–	70	90	–	70	90	–	dB
Power Supply Current (V_O = 0) $R_L = \infty$	I_{CC},I_{EE}	–	1.6	2.2	–	1.6	3.7	–	1.6	3.7	mA
Individual Output Short-Circuit Current (2)	$I_{OS\pm}$	±10	±30	±45	±10	±20	±45	±10	±30	±45	mA
Positive Power Supply Rejection Ratio	PSRR+	–	30	150	–	30	150	–	30	150	μV/V
Negative Power Supply Rejection Ratio	PSRR-	–	30	150	–	30	150	–	–	–	μV/V
Average Temperature Coefficient of Input Offset Current $T_A = T_{high}$ to T_{low}	$\Delta I_{IO}/\Delta T$	–	50	–	–	50	–	–	50	–	pA/°C
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{high}$ to T_{low}	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	μV/°C
Power Bandwidth A_V = 1, R_L = 2.0 kΩ, V_O = 20 V(p-p), THD = 5%	BWp	–	9.0	–	–	9.0	–	–	9.0	–	kHz
Small-Signal Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 50 mV	BW	–	1.0	–	–	1.0	–	–	1.0	–	MHz
Slew Rate A_V = 1, V_i = -10 V to +10 V	SR	–	0.6	–	–	0.6	–	–	0.6	–	V/μs
Rise Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{TLH}	–	0.35	–	–	0.35	–	–	0.35	–	μs
Fall Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{THL}	–	0.35	–	–	0.35	–	–	0.35	–	μs
Overshoot A_V = 1, R_L = 10 kΩ, V_O = 50 mV	OS	–	20	–	–	20	–	–	20	–	%
Phase Margin A_V = 1, R_L = 2.0 kΩ, C_L = 200 pF	φm	–	60	–	–	60	–	–	60	–	Degrees
Crossover Distortion (V_{in} = 30 mVp-p, V_{out} = 2.0 Vp-p, f = 10 kHz)	–	–	1.0	–	–	1.0	–	–	1.0	–	%

(1) T_{high} = 125°C for MC3558, 70°C for MC3458, 85°C for MC3358.
T_{low} = -55°C for MC3558, 0°C for MC3458, -40°C for MC3358.

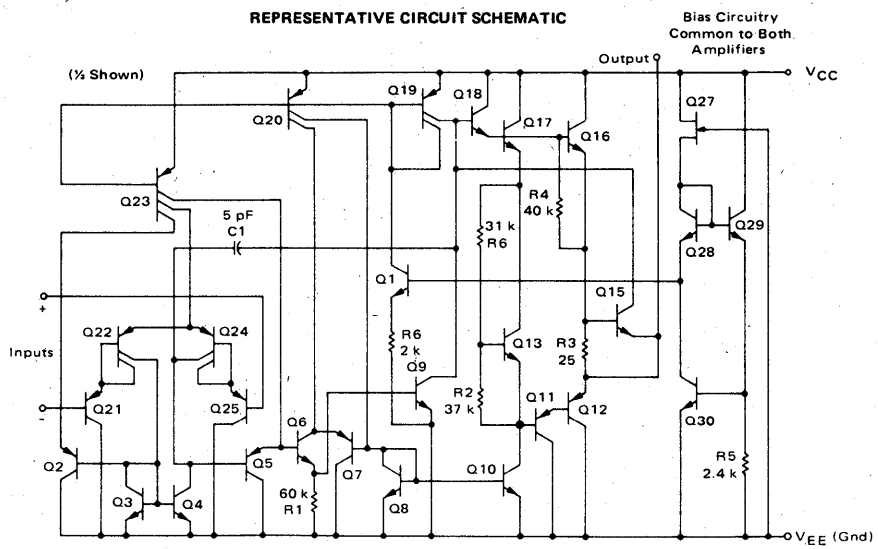
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC3558			MC3458			MC3358			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	–	2.0	10	mV
Input Offset Current	I_{IO}	–	30	50	–	30	50	–	–	75	nA
Input Bias Current	I_{IB}	–	-200	-500	–	-200	-500	–	–	-500	nA
Large-Signal Open-Loop Voltage Gain R_L = 2.0 kΩ	A_{VOL}	20	200	–	20	200	–	20	200	–	V/mV
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	–	–	150	μV/V
Output Voltage Range (3) R_L = 10 kΩ, V_{CC} = 5.0 V R_L = 10 kΩ, 5.0 V < V_{CC} < 30 V	V_{OR}	3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	Vp-p
		–	V_{CC} -1.7 V	–	–	V_{CC} -1.7 V	–	–	V_{CC} -1.7 V	–	
Power Supply Current	I_{CC}	–	2.5	4.0	–	2.5	7.0	–	2.5	4.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	–	–	-120	–	–	-120	–	–	-120	–	dB

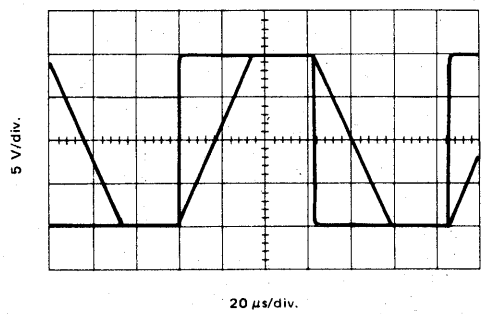
(2) Not to exceed maximum package power dissipation.
(3) Output will swing to ground

3

REPRESENTATIVE CIRCUIT SCHEMATIC



INVERTER PULSE RESPONSE



CIRCUIT DESCRIPTION

The MC3558 Series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

TYPICAL PERFORMANCE CURVES

FIGURE 1 – SINE WAVE RESPONSE

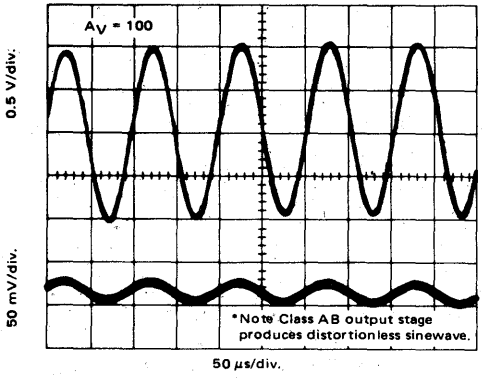


FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

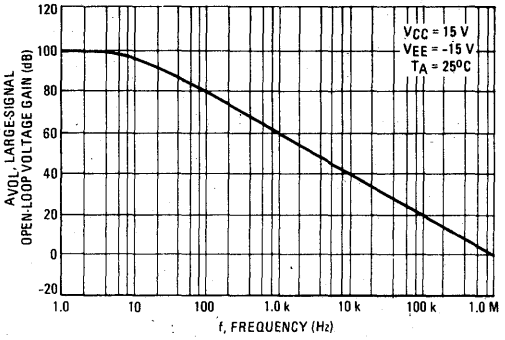


FIGURE 3 – POWER BANDWIDTH

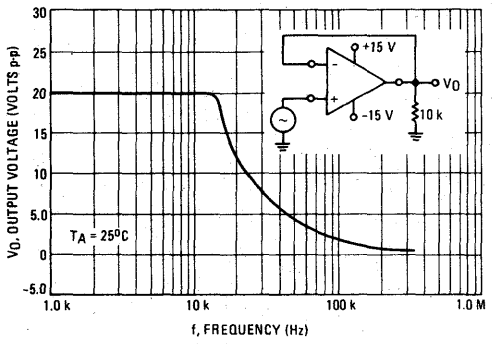


FIGURE 4 – OUTPUT SWING versus SUPPLY VOLTAGE

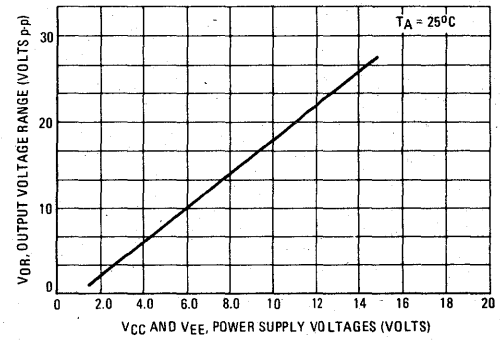


FIGURE 5 – INPUT BIAS CURRENT versus TEMPERATURE

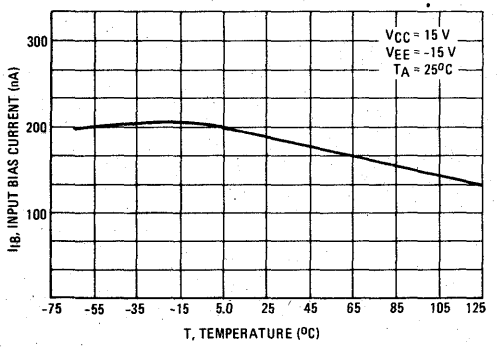
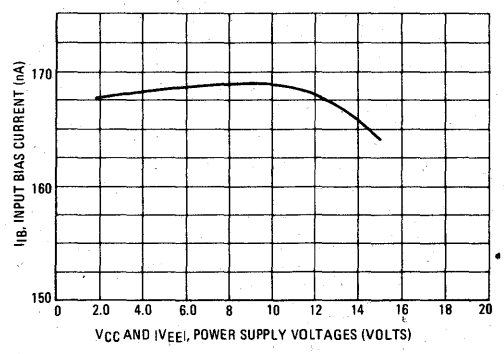


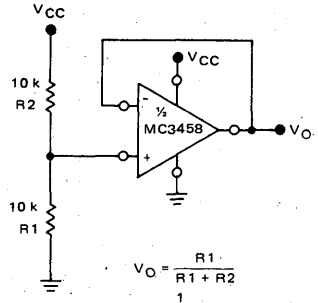
FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



3

APPLICATIONS INFORMATION

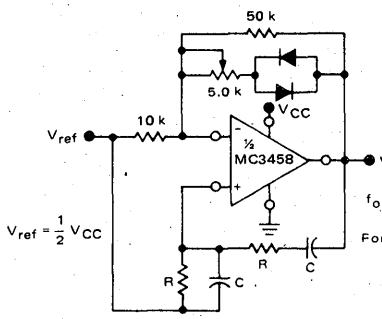
FIGURE 7 – VOLTAGE REFERENCE



$$V_O = \frac{R1}{R1 + R2}$$

$$V_O = \frac{1}{2} V_{CC}$$

FIGURE 8 – WEIN BRIDGE OSCILLATOR

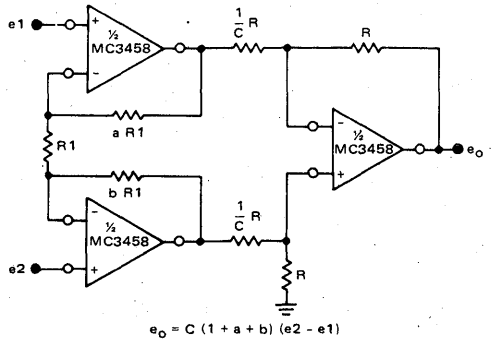


$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_o = \frac{1}{2 \pi RC}$$

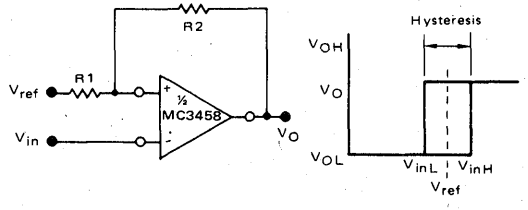
For f_o = 1 kHz
R = 16 kΩ
C = 0.01 μF

FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



$$e_o = C (1 + a + b) (e2 - e1)$$

FIGURE 10 – COMPARATOR WITH HYSTERESIS

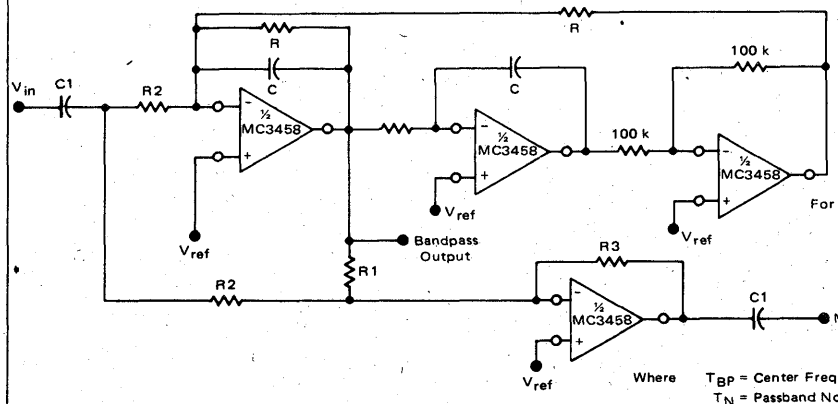


$$V_{inL} = \frac{R1}{R1 + R2} (V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2} (V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$$

FIGURE 11 – BI-QUAD FILTER



$$f_o = \frac{1}{2 \pi RC}$$

$$R1 = QR$$

$$R2 = \frac{R1}{T_{BP}}$$

$$R3 = T_N R2$$

$$C1 = 10 C$$

$$V_{ref} = \frac{1}{2} V_{CC}$$

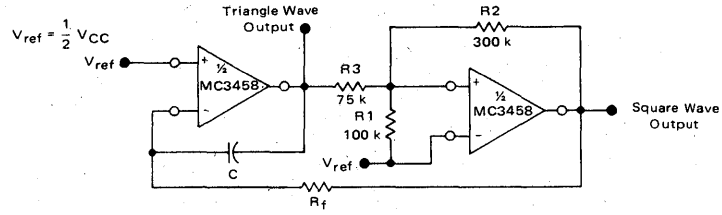
For f_o = 1 kHz
Q = 10
T_{BP} = 1
T_N = 1

R = 160 kΩ
C = 0.001 μF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

Where T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

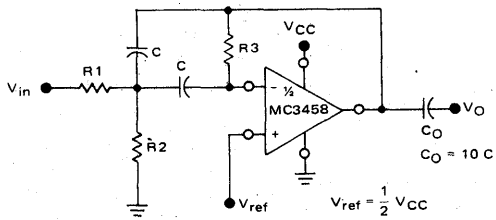
APPLICATIONS INFORMATION (continued)

FIGURE 12 – FUNCTION GENERATOR



$$f = \frac{R1 + R_C}{4 C R_f R1} \quad \text{if} \quad R3 = \frac{R2\ R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then:

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2 A(f_o)}$$

$$R2 = \frac{R1\ R3}{4Q^2 R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{BW} < 0.1$$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

MC3471
MC3571

Advance Information

QUAD WIDEBAND OPERATIONAL AMPLIFIERS

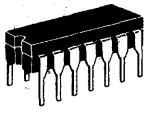
The MC3471/MC3571 is one of the first quad FET-input operational amplifiers offered to the industry. Its FET input gives the amplifier a very high input impedance and extremely low input characteristics. The MC3471 also features a **unity gain stable 10 MHz bandwidth.**

This large bandwidth makes this device excellent for active filter applications where high frequency performance is required. It is also very useful as a general purpose high performance operational amplifier because of its attractive input characteristics.

- Four Amplifiers on a Single Monolithic Chip
- FET Input
- Bandwidth = 10 MHz (Unity Gain Stable)
- High Input Impedance
- Low Input Offset Currents (20 pA)
- No External Compensation Required
- High Slew Rate (20 V/μs)

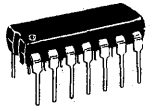
QUAD FET-INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P SUFFIX
PLASTIC PACKAGE
CASE 646



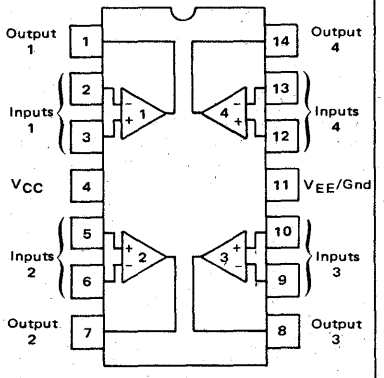
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	Volts
Input Differential Voltage	V_{ID}	±30	Volts
Input Common Mode Voltage	V_{IC}	±10	Volts
Output Short-Circuit Duration	t_S	Continuous	s
Power Dissipation Plastic package Ceramic package	P_D	 625 750	mW
Operating Temperature Range MC3471 MC3571	T_A	 0 to +70 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature Range	T_J	150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient Plastic (Case 646) Ceramic (Case 632)	$R_{\theta JA}$	 100 100	°C/W

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC3471L	0 to +70°C	Ceramic DIP
MC3471P	0 to +70°C	Plastic DIP
MC3571L	-55 to +125°C	Ceramic DIP

This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC3471			MC3571			Unit
		Min	Typ	Max	Min	Typ	Max	
Imput Offset Voltage	V_{IO}							mV
(R_S = 10 kΩ)		–	–	6.0	–	–	5.0	
(R_S = 10 kΩ, T_{low} to T_{high})		–	–	7.5	–	–	6.0	
Input Offset Current	I_{IO}	–	–	20	–	–	20	pA
Input Bias Current	I_{IB}	–	20	200	–	20	200	pA
Large-Signal Open Loop Voltage Gain	A_{VOL}							V/V
(R_L = 2.0 kΩ)		25 k	–	–	50 k	–	–	
(R_L = 2.0 kΩ, T_{low} to T_{high})		15 k	–	–	25 k	–	–	
Power Supply Current	I_{CC}							mA
(T_A = 25°C)		–	–	10	–	–	8.0	
(T_A = T_{low} to T_{high})		–	–	12	–	–	8.5	
(T_A = 25°C)	I_{EE}	–	–	10	–	–	8.0	
(T_A = T_{low} to T_{high})		–	–	12	–	–	8.5	
Common-Mode Rejection Ratio (T_{low} to T_{high})	CMRR	80	–	–	80	–	–	dB
Power Supply Rejection Ratio (T_{low} to T_{high})	PSRR	70	–	–	70	–	–	dB
Output Voltage	V_O							V
(R_L = 20 kΩ, T_{low} to T_{high})		±10	±12	–	±10	±12	–	
(R_L = 10 kΩ, T_{low} to T_{high})		±12	±13	–	±12	±13	–	
Input Common-Mode Voltage Range	V_{ICR}	±10	–	–	±10	–	–	V
Input Differential Voltage Range	V_{IDR}	±30	–	–	±30	–	–	V
Output Short-Circuit Current (Shorted to Supplies)	I_{OS}	–	25	–	–	25	–	mA
Small-Signal Bandwidth	BW	8.0	10	–	8.0	10	–	MHz
Power Bandwidth (V_{out} = ±10 V)	BW_P	200	–	–	200	–	–	kHz
Unity Gain Crossover Frequency	f_c	8.0	10	–	8.0	10	–	MHz
Power Consumption	P_C							mW
(T_A = 25°C)		–	–	300	–	–	240	
(T_A = T_{low} to T_{high})		–	–	360	–	–	255	
Channel Separation	–	80	–	–	80	–	–	dB
Slew Rate	SR	20	–	–	20	–	–	V/μs

ORDERING INFORMATION

Device	Temperature Range	Package
MC3476G	0°C to +70°C	Metal Can
MC3476P1	0°C to +70°C	Plastic DIP

MC3476

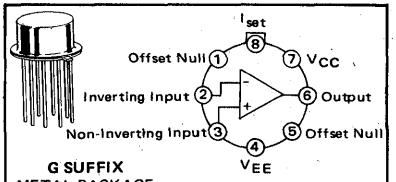
PROGRAMMABLE OPERATIONAL AMPLIFIER

This extremely versatile operational amplifier features low power consumption, and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current, power consumption and input voltage despite wide variations in operating power supply voltages.

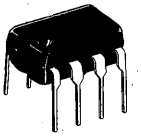
- ±6.0 V to ±15 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short-Circuit Protection

PROGRAMMABLE OPERATIONAL AMPLIFIER

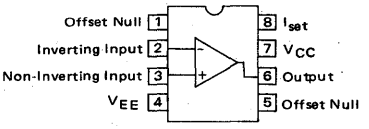
SILICON MONOLITHIC INTEGRATED CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 601-03

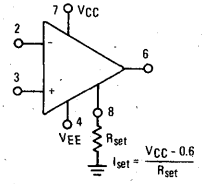


P1 SUFFIX
PLASTIC PACKAGE
CASE 626



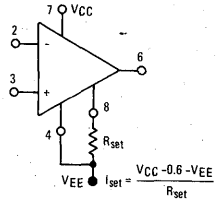
RESISTIVE PROGRAMMING (See Figure 1.)

R_{set} to GROUND



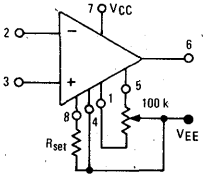
Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 10 μA	I_{set} = 15 μA
±6.0 V	560 kΩ	360 kΩ
±9.0 V	820 kΩ	560 kΩ
±12 V	1.0 MΩ	750 kΩ
±15 V	1.5 MΩ	1.0 MΩ

R_{set} to NEGATIVE SUPPLY



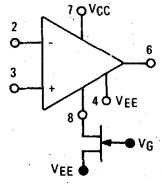
Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 10 μA	I_{set} = 15 μA
±6.0 V	1.0 MΩ	820 kΩ
±9.0 V	1.8 MΩ	1.2 MΩ
±12 V	2.2 MΩ	1.5 MΩ
±15 V	2.7 MΩ	2.0 MΩ

VOLTAGE OFFSET NULL CIRCUIT

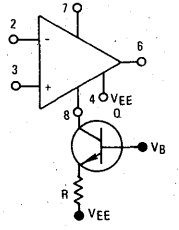


ACTIVE PROGRAMMING

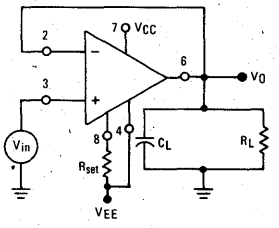
FET CURRENT SOURCE



BIPOLAR CURRENT SOURCE



TRANSIENT-RESPONSE TEST CIRCUIT

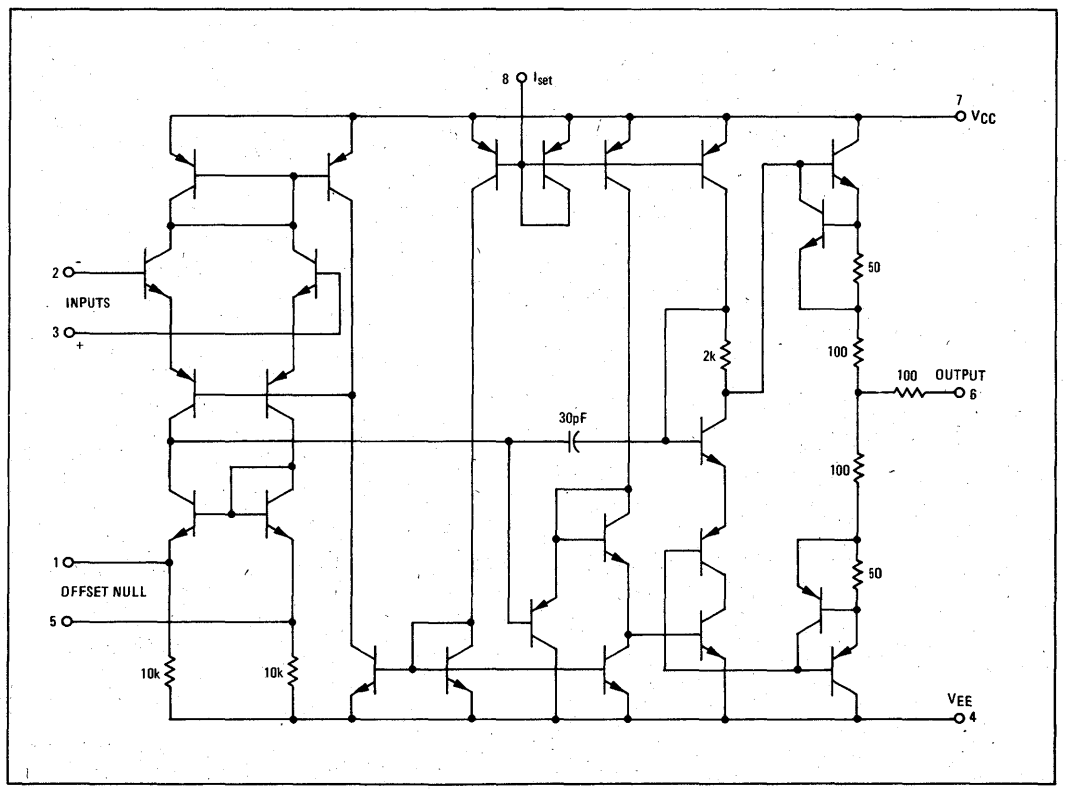


MAXIMUM RATINGS(T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±18	Vdc
Input Differential Voltage Range	V_{IDR}	±30	Vdc
Input Common-Mode Voltage Range	V_{ICR}	V_{CC}, V_{EE}	Vdc
Offset Null to V_{EE} Voltage	$V_{off}-V_{EE}$	±0.5	Vdc
Programming Current	I_{set}	200	μA
Programming Voltage (Voltage from I_{set} terminal to ground)	V_{set}	(V_{CC}-0.6 V) to V_{CC}	Vdc
Output Short-Circuit Duration*	t_S	Indefinite	s
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Power Dissipation (Package Limitation)	P_D		
Metal Package @ T_A = +25°C		680	mW
Derate above 25°C		4.6	mW/°C
Plastic Package @ T_A = +25°C		625	mW
Derate above 25°C		5.0	mW/°C

*Short-Circuit to ground with $I_{set} \leq 15$ μA. Rating applies up to ambient temperature of +70°C.

EQUIVALENT SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, I_{set} = 15 μA, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}				mV
T_A = +25°C		–	2.0	6.0	
0°C ≤ T_A ≤ 70°C		–	–	7.5	
Input Offset Current	I_{IO}				nA
T_A = +25°C		–	2.0	25	
T_A = 70°C		–	–	25	
T_A = 0°C		–	–	40	
Input Bias Current	I_{IB}				nA
T_A = +25°C		–	15	50	
T_A = 70°C		–	–	50	
T_A = 0°C		–	–	100	
Input Resistance	r_i	–	5.0	–	MΩ
Input Capacitance	C_i	–	2.0	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	mV
Large Signal Voltage Gain	A_{VOL}				V/V
$R_L \geq 10$ kΩ, V_O = ±10 V, T_A = +25°C		50 k	400 k	–	
$R_L \geq 10$ kΩ, V_O = ±10 V, 0°C ≤ T_A ≤ 70°C		25 k	–	–	
Output Resistance	r_o	–	1.0	–	kΩ
Output Short-Circuit Current	I_{OS}	–	12	–	mA
Supply Current	I_{CC}, I_{EE}				μA
T_A = +25°C		–	160	200	
0°C ≤ T_A ≤ 70°C		–	–	225	
Power Consumption	P_C				mW
T_A = +25°C		–	4.8	6.0	
0°C ≤ T_A ≤ 70°C		–	–	6.75	
Transient Response (Unity Gain)					
V_{in} = 20 mV, $R_L \geq 10$ kΩ, C_L = 100 pF					
Rise Time	t_{TLH}	–	0.35	–	μs
Overshoot	OS	–	10	–	%
Slew Rate ($R_L \geq 10$ kΩ)	SR	–	0.8	–	V/μs
Output Voltage Range	V_{OR}				V
$R_L \geq 10$ kΩ, T_A = +25°C		±12	±13	–	
$R_L \geq 10$ kΩ, 0°C ≤ T_A ≤ 70°C		±12	–	–	
Input Common-Mode Voltage Range	V_{ICR}	±10	–	–	V
0°C ≤ T_A ≤ 70°C					
Common-Mode Rejection Ratio	CMRR	70	90	–	dB
$R_S \leq 10$ kΩ, 0°C ≤ T_A ≤ 70°C					
Supply Voltage Rejection Ratio	PSRR	–	25	200	μV/V
$R_S \leq 10$ kΩ, 0°C ≤ T_A ≤ 70°C					

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 1 – SET CURRENT versus SET RESISTOR

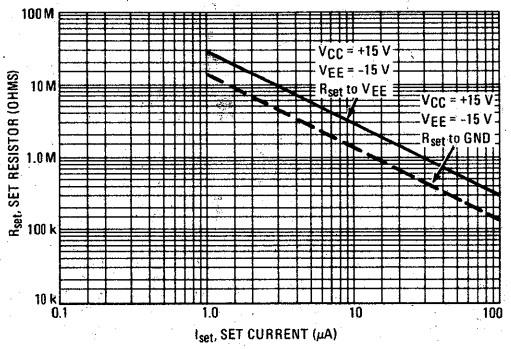
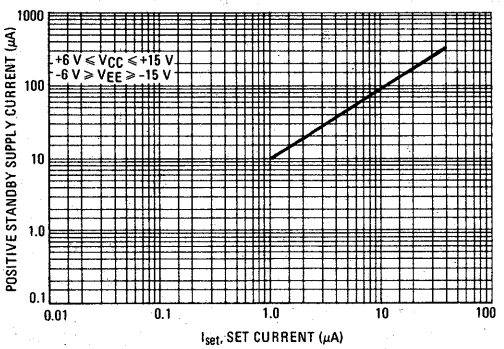


FIGURE 2 – POSITIVE STANDBY SUPPLY CURRENT versus SET CURRENT



TYPICAL CHARACTERISTICS (continued)

(T_A = +25°C unless otherwise noted.)

FIGURE 3 – OPEN-LOOP GAIN versus SET CURRENT

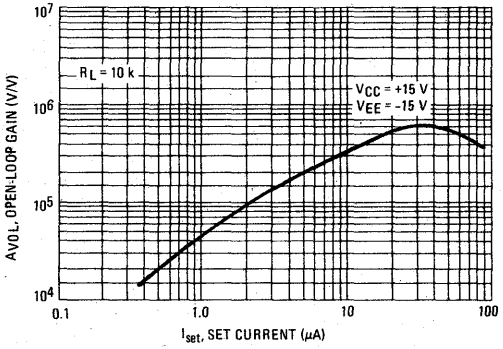


FIGURE 4 – INPUT BIAS CURRENT versus SET CURRENT

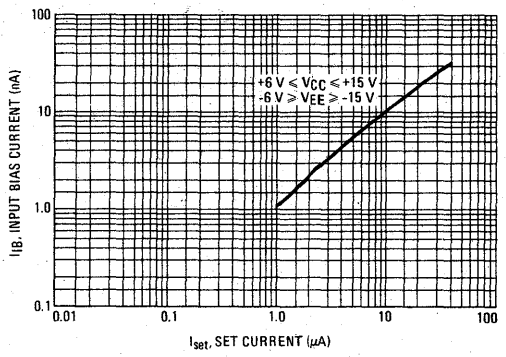


FIGURE 5 – SLEW RATE versus SET CURRENT

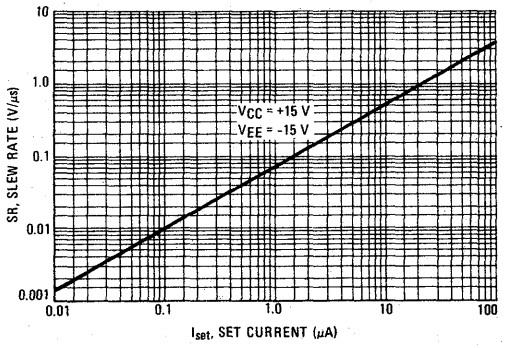


FIGURE 6 – GAIN-BANDWIDTH PRODUCT (GBW) versus SET CURRENT

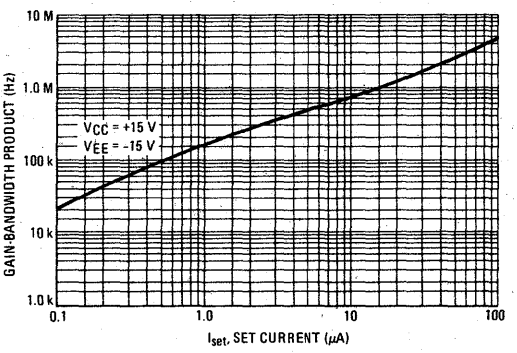


FIGURE 7 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

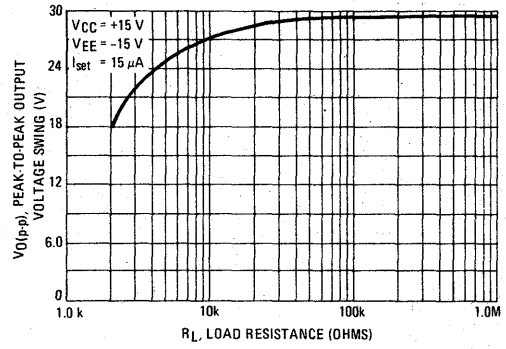
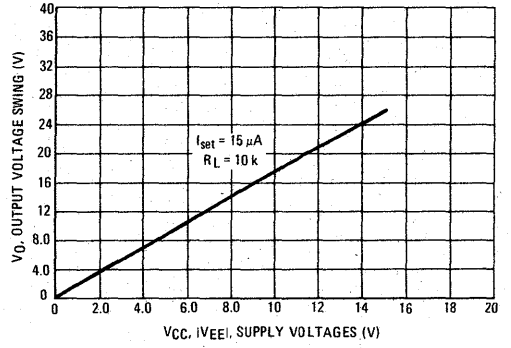


FIGURE 8 – OUTPUT SWING versus SUPPLY VOLTAGE



MC4202C

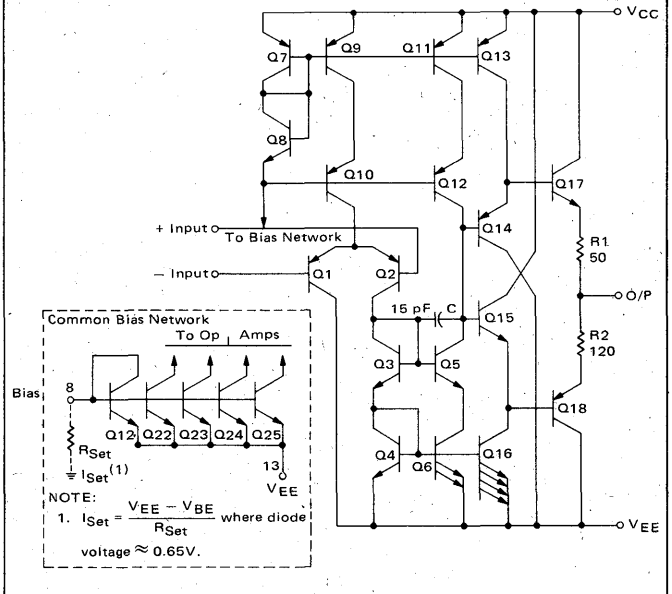
Advance Information

PROGRAMMABLE QUAD OPERATIONAL AMPLIFIER

The MC4202C is an array of four independent operational amplifiers on a single silicon chip. The operating current of the array is externally controlled by a single resistor or current source, allowing the user to trade-off power dissipation for bandwidth.

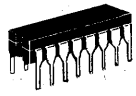
- Wide Input Voltage and Common Mode Range
- Externally Programmable
- Internal Frequency Compensation
- No Latch-Up
- Matched Parameters
- Short-Circuit Protection

SCHEMATIC DIAGRAM (Each Amplifier)

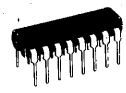


PROGRAMMABLE QUAD OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

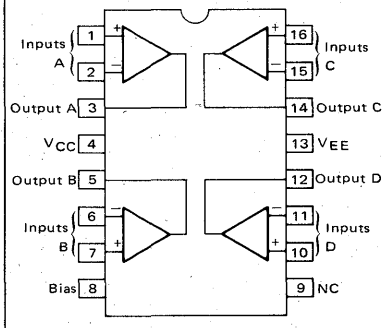


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC4202CL	0 to +70°C	Ceramic DIP
MC4202CP	0 to +70°C	Plastic DIP

This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol		Unit
Supply Voltage	V_{CC} V_{EE}	+18 -18	V
Differential Input Voltage Range	V_{IDR}	±30	V
Common-Mode Range	V_{ICM}	V_{EE} to V_{CC}	V
Short-Circuit Duration	T_S	Indefinite	–
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range Ceramic Package Plastic Package	T_J	 175 150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Notes:
1. Ceramic dual-in-line package rating applies for case temperatures to +125°C; derate linearly at 10 mW/°C for ambient temperatures above +95°C. Plastic dual-in-line package rating applies for case temperatures to 70°C; derate linearly at 6.7 mW/°C for ambient temperatures above +55°C.
2. Short-circuit may be taken to either supply line or ground on only one amplifier at a time.

ELECTRICAL CHARACTERISTICS* – High Power Mode (V_{CC} = 15 V, V_{EE} = -15 V, I_{Set} = 75 μA and T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Short-Circuit Current	I_{OS}	–	20	–	mA
Supply Current(1)	I_S	1.6	2.5	4.0	mA
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	1.0	5.0	mV
Input Bias Current	I_{IB}	–	200	500	nA
Input Offset Current	I_{IO}	–	5.0	50	nA
Input Resistance	r_i	20	200	–	kΩ
Input Common Mode Voltage Range	V_{ICR}	12	13	–	±V
Common Mode Rejection Ratio	CMRR	70	86	–	dB
Voltage Supply Rejection Ratio	PSRR	–	50	150	μV/V
Large-Signal Voltage Gain (R_L = 3.0 kΩ, ΔV_o = ±10 V)	A_{VOL}	 74	 86	 –	dB
Output Voltage Swing (R_L = 3.0 kΩ)	V_{out}	10	11	–	±V
Gain Bandwidth Product	f_1	–	2.5	–	MHz
Phase Margin	ϕm	–	45	–	Degrees
Rise Time (ΔV_o = ±20 mV)	t_r	–	140	–	ns
Overshoot (ΔV_o = ±20 mV)	t_o	–	20	–	%
Channel Separation (R_L = 2.0 kΩ, f = 1.0 Hz) (R_L = 2.0 kΩ, f = 10 kHz)	–	 – –	 100 120	 – –	dB
Slew Rate	SR	–	1.5	–	V/μs
Equivalent Input Voltage Noise (Bandwidth = 100 Hz to 10 KHz)	e_n	–	25	–	$nV\sqrt{Hz}$

3

ELECTRICAL CHARACTERISTICS* — Micropower Mode (V_{CC} = +1.5 V, V_{EE} = -1.5 V, I_{Set} = 1.0 μA unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current(1)	I_S	20	30	40	μA
Input Bias Current	I_{IB}	–	10	100	nA
Input Offset Current	I_{IO}	–	1.0	10	nA
Input Offset Voltage ($R_S \pm \leq 10$ kΩ)	V_{IO}	–	2.0	5.0	mV
Input Resistance	r_i	0.5	2.0	–	MΩ
Input Common Mode Voltage Range	V_{ICR}	0.3	0.5	–	±V
Common Mode Rejection Ratio	CMRR	60	80	–	dB
Voltage Supply Rejection Ratio	PSRR	–	50	200	μV/V
Large Signal Voltage Gain ($R_L \geq 100$ kΩ)	A_{VOL}	66	80	–	dB
Gain Bandwidth Product	f_1	–	50	–	kHz
Phase Margin	ϕm	–	45	–	Degrees
Slew Rate	SR	–	20	–	V/ms
Rise Time (ΔV_O = ±20 mV)	t_r	–	7.0	–	μs
Overshoot (ΔV_O = ±20 mV)	t_o	–	0	–	%
Channel Separation, Any Amplifier Pair	–				dB
(R_L = 20kΩ, f = 1.0 Hz, ΔV_O = ±0.5 V)		–	120	–	
(R_L = 10 kΩ, f = 1.0 kHz, ΔV_O = ±0.5 V)		–	120	–	
Equivalent Input Voltage Noise (Bandwidth = 100 Hz to 10 KHz)	e_n	–	200	–	$nV\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS — Parameter Matching (I_{Set} = 75 μA, tests apply for parameter matching between any operational amplifier pair.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	1.0	–	±mV
Input Bias Current	I_{IB}	–	10	–	±nA
Input Offset Current	I_{IO}	–	2.0	–	±nA
Gain Bandwidth Product	f_1	–	100	–	±kHz
Slew Rate	SR	–	0.2	–	±V/μs

Note:

*All tests refer to a single operational amplifier unless otherwise specified.

1. Tests apply to four op-amps and bias network.

TYPICAL CHARACTERISTIC CURVES

FIGURE 1 — TOTAL SUPPLY CURRENT versus SET CURRENT

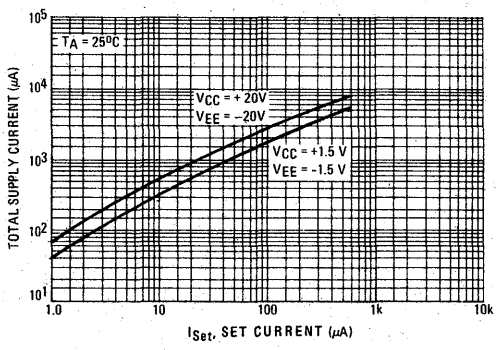


FIGURE 2 — OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

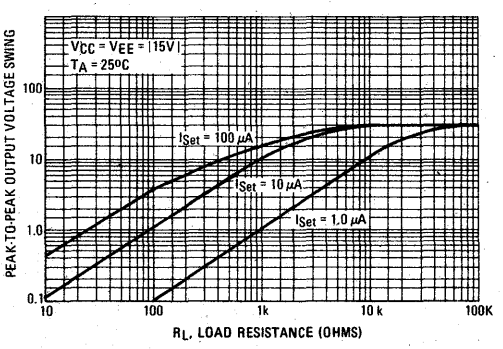


FIGURE 3 – INPUT BIAS CURRENT versus SET CURRENT

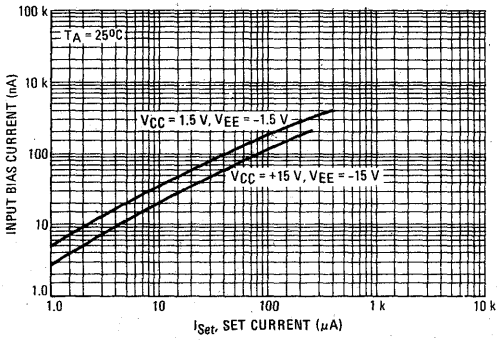


FIGURE 4 – TYPICAL FREQUENCY RESPONSES FOR VARIOUS SET CURRENTS I_{SET}

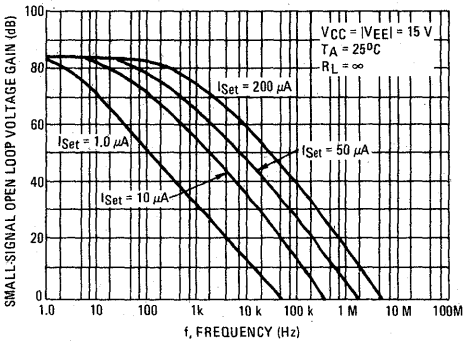
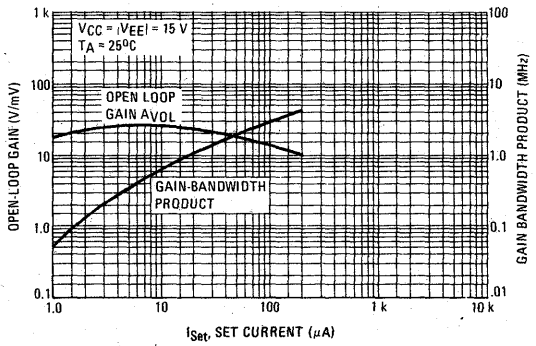


FIGURE 5 – GAIN-BANDWIDTH PRODUCT, A_{VOL} versus SET CURRENT



APPLICATIONS INFORMATION

The following approximate relations are useful for design:

Gain-Bandwidth Product	≈	50 (I_{Set})	(kHz)
Power Supply Current	≈	30 (I_{Set})	(μA)
Slew Rate	≈	20 (I_{Set})	(V/ms)

Where: I_{Set} is in μA, $I_{Set} = \frac{V_{EE} - V_{BE}}{R_{Set}}$

V_{BE} = Diode Voltage ≈ 0.65 Volts

MC4558
MC4558C

Advance Information

DUAL WIDEBAND OPERATIONAL AMPLIFIER

The MC4558 and MC4558C combine all the outstanding features of the MC1458, and in addition, possesses several times the unity gain bandwidth of the industry standard.

- **2.5 MHz Unity Gain Bandwidth Guaranteed**
- Internally Compensated
- Short Circuit Protection
- Gain and Phase Match Between Amplifiers
- Low Power Consumption

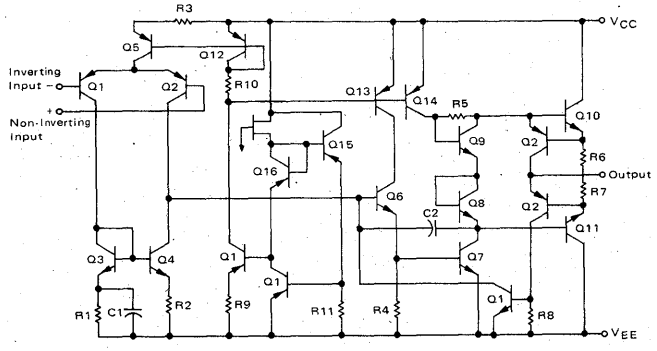
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MC4558C	MC4558	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 -18	+22 -22	Vdc Vdc
Input Differential Voltage	V_{ID}	±30		Volts
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		Volts
Output Short Circuit Duration (Note 2)	t_S	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70	-55 to +125	°C
Storage Temperature Range Metal, Flat and Ceramic Packages Plastic Packages	T_{stg}	 -65 to +150 -55 to +125		°C
Junction Temperature Metal and Ceramic Package Plastic Package	T_J	 175 150		°C

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. Supply voltage equal to or less than 15 V.

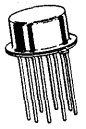
EQUIVALENT CIRCUIT SCHEMATIC



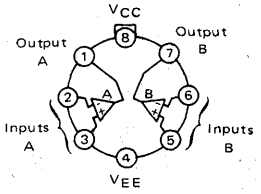
This is advance information and specifications are subject to change without notice.

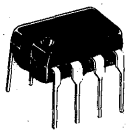
DUAL
OPERATIONAL AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

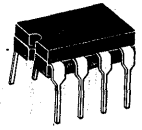


G SUFFIX
METAL PACKAGE
CASE 601

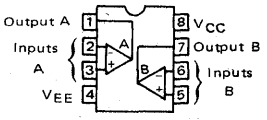




P1 SUFFIX
PLASTIC PACKAGE
CASE 626



U SUFFIX
CERAMIC PACKAGE
CASE 693



ORDERING INFORMATION

Device	Temperature Range	Package
MC4558G	-55 to +125°C	Metal Can
MC4558U	-55 to +125°C	Ceramic DIP
MC4558CG	0 to +70°C	Metal Can
MC4558CP1	0 to +70°C	Plastic DIP
MC4558CU	0 to +70°C	Ceramic DIP

FREQUENCY CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = -15 V, T_A = 25°C)

Characteristic	Symbol	MC4558 Min	MC4558 Typ	MC4558 Max	MC4558C Min	MC4558C Typ	MC4558C Max	Unit
Unity Gain Bandwidth (A_V = 1)	BW	2.5	2.8	–	2.0	2.8	–	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = -15 V, T_A = 25°C unless otherwise noted.)

Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	1.0	5.0	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	nA
Input Bias Current	I_{IB}	–	80	500	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_V	50	200	–	20	200	–	V/mV
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio ($R_S \leq 10$ kΩ)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ kΩ)	PSRR	–	30	150	–	30	150	μV/V
Output Voltage Swing	V_O							
($R_L \geq 10$ kΩ)		±12	±14	–	±12	±14	–	V
($R_L \geq 2$ kΩ)		±10	±13	–	±10	±13	–	
Output Short-Circuit Current	I_{os}	–	20	–	–	20	–	mA
Supply Currents (Both Amplifiers)	I_D	–	2.3	5.0	–	2.3	5.6	mA
Power Consumption	P_C	–	70	150	–	70	170	mW
Transient Response (Unity Gain)								
(V_I = 20 mV, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	μs
(V_I = 20 mV, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Overshoot	os	–	15	–	–	15	–	%
(V_I = 10 V, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Slew Rate	SR	–	1.5	–	–	1.0	–	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = -15 V, T_A = *T_{high} to T_{low} unless otherwise noted).

Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	mV
Input Offset Current	I_{IO}							
(T_A = 125°C)		–	7.0	200	–	–	–	nA
(T_A = -55°C)		–	85	500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	300	
Input Bias Current	I_{IB}							
(T_A = 125°C)		–	30	500	–	–	–	nA
(T_A = -55°C)		–	300	1500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	800	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	V
Common Mode Rejection Ratio ($R_S \leq 10$ kΩ)	CMRR	70	90	–	–	–	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ kΩ)	PSRR	–	30	150	–	–	–	μV/V
Output Voltage Swing	V_O							
($R_L \geq 10$ kΩ)		±12	±14	–	±12	±14	–	V
($R_L \geq 2$ kΩ)		±10	±13	–	±10	±13	–	
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2 kΩ)	A_V	25	–	–	15	–	–	V/mV
Supply Currents (Both Amplifiers)	I_D							
(T_A = 125°C)		–	–	4.5	–	–	–	mA
(T_A = -55°C)		–	–	6.0	–	–	–	
Power Consumption	P_C	–	–	135	–	–	–	mW
(T_A = 125°C)		–	–	180	–	–	–	
(T_A = -55°C)								

*T_{high} = 125°C for MC4558 and 70°C for MC4558C
T_{low} = -55°C for MC4558 and 0°C for MC4558C

ORDERING INFORMATION

Device	Temperature Range	Package
MC4741L	−55°C to +125°C	Ceramic DIP
MC4741CL	0°C to +70°C	Ceramic DIP
MC4741CP	0°C to +70°C	Plastic DIP

MC4741
MC4741C

Specifications and Applications Information

3

QUAD MC1741 OPERATIONAL AMPLIFIERS

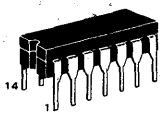
The MC4741 series is a true quad MC1741 Integrated on a single monolithic chip are four independent, low-power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance.

The MC4741 can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

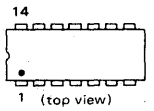
- Each Amplifier is Functionally Equivalent to the MC1741
- Class AB Output Stage Eliminates Crossover Distortion
- True Differential Inputs
- Internally Frequency Compensated
- Short Circuit Protection
- Low Power Supply Current (0.6 mA/Amplifier)

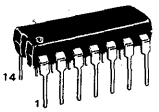
QUAD MC1741 DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT



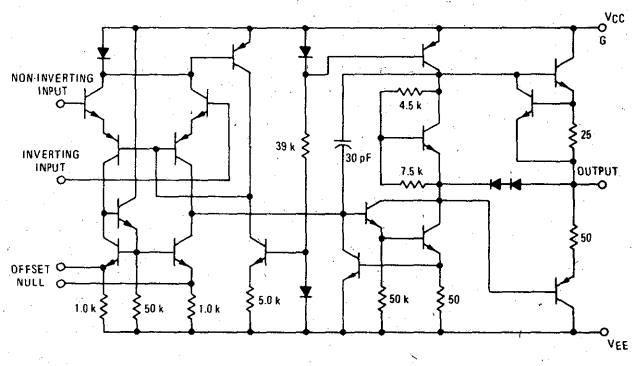
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



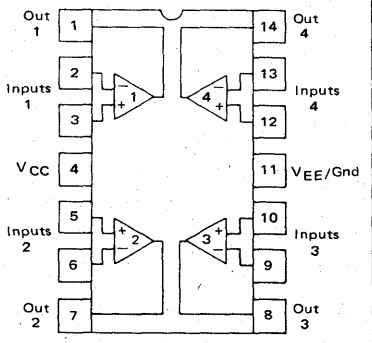


P SUFFIX
PLASTIC PACKAGE
CASE 646

EQUIVALENT CIRCUIT SCHEMATIC
(1/4 of Circuit Shown)



PIN CONNECTIONS

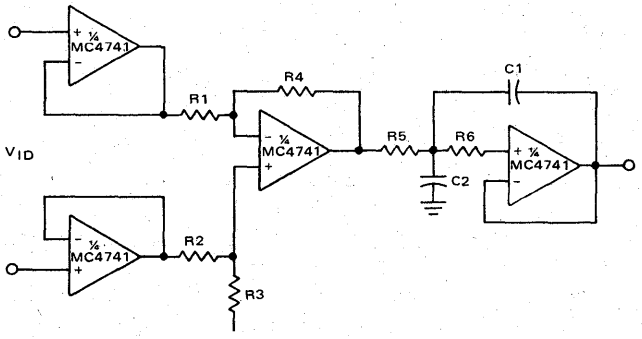


MAXIMUM RATINGS (T_A = +25°C unless otherwise noted).

Rating	Symbol	MC4741	MC4741C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc Vdc
Input Differential Voltage	V_{ID}	±44	±36	Volts
Input Common Mode Voltage	V_{ICM}	±22	±18	Volts
Output Short Circuit Duration	t_S	Continuous		
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 -65 to +150 -55 to +125		°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150		°C

TYPICAL APPLICATION

HIGH IMPEDANCE INSTRUMENTATION BUFFER/FILTER



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ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = 25°C unless otherwise noted).

Characteristic	Symbol	MC4741			MC4741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}	–	1.0	5.0	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	nA
Input Bias Current	I_{IB}	–	80	500	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, $R_L \geq 2.0$ k)	A_V	50	200	–	20	200	–	V/mV
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	–	30	150	μV/V
Output Voltage Swing	V_O							V
($R_L \geq 10$ k)		±12	±14	–	±12	±14	–	
($R_L \geq 2$ k)		±10	±13	–	±10	±13	–	
Output Short-Circuit Current	I_{os}	–	20	–	–	20	–	mA
Supply Current – (All Amplifiers)	I_D	–	2.4	4.0	–	3.5	7.0	mA
Power Consumption (All Amplifiers)	P_C	–	72	120	–	105	210	mW
Transient Response (Unity Gain – Non-Inverting)								
(V_I = 20 mV, $R_L \geq 2$ k, $C_L \leq 100$ pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	μs
(V_I = 20 mV, $R_L \geq 2$ k, $C_L \leq 100$ pF) Overshoot	os	–	15	–	–	15	–	%
(V_I = 10 V, $R_L \geq 2$ k, $C_L \leq 100$ pF) Slew Rate	SR	–	0.5	–	–	0.5	–	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = *T_{high} to T_{low} unless otherwise noted.)

Characteristic	Symbol	MC4741			MC4741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	mV
Input Offset Current	I_{IO}							nA
(T_A = 125°C)		–	7.0	200	–	–	–	
(T_A = -55°C)		–	85	500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	300	
Input Bias Current	I_{IB}							nA
(T_A = 125°C)		–	30	500	–	–	–	
(T_A = -55°C)		–	300	1500	–	–	–	
(T_A = 0°C to +70°C)		–	–	–	–	–	800	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	V
Common Mode Rejection Ratio ($R_S \leq 10$ k)	CMRR	70	90	–	–	–	–	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	–	30	150	–	–	–	μV/V
Output Voltage Swing	V_O							V
($R_L \geq 10$ k)		±12	±14	–	–	–	–	
($R_L \geq 2$ k)		±10	±13	–	±10	±13	–	
Large Signal Voltage Gain ($R_L \geq 2$ k, V_{out} = ±10 V)	A_V	25	–	–	15	–	–	V/mV
Supply Currents – (All Amplifiers)	I_D							mA
(T_A = 125°C)		–	2.4	3.4	–	–	–	
(T_A = -55°C)		–	3.6	5.0	–	–	–	
Power Consumption (T_A = +125°C)	P_C	–	72	102	–	–	–	mW
(All Amplifiers) (T_A = -55°C)		–	108	150	–	–	–	

*T_{high} = 125°C for MC4741 and 70°C for MC4741C
T_{low} = -55°C for MC4741 and 0°C for MC4741C

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted).

FIGURE 1 – POWER BANDWIDTH (LARGE SIGNAL SWING versus FREQUENCY)

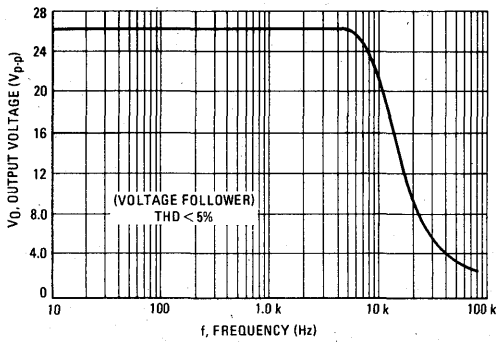

FIGURE 2 – OPEN LOOP FREQUENCY RESPONSE

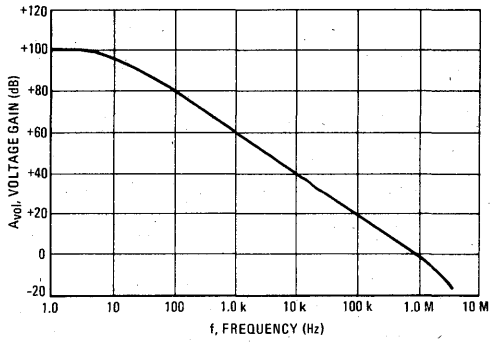

FIGURE 3 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

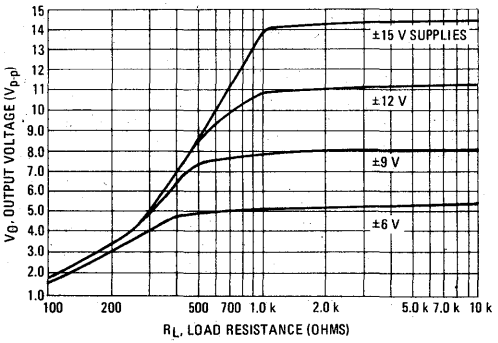

FIGURE 4 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

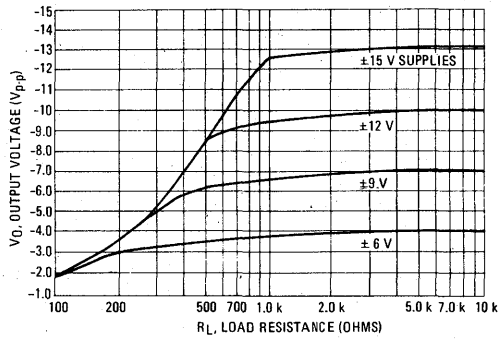

FIGURE 5 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE (Single Supply Operation)

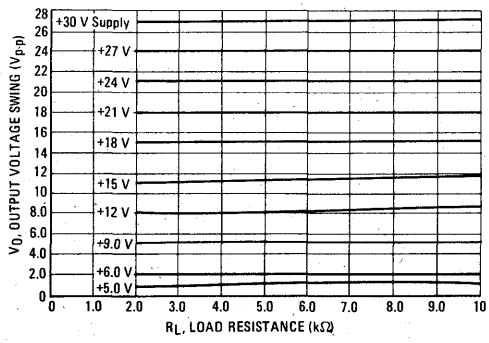

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FIGURE 6 – BI-QUAD FILTER

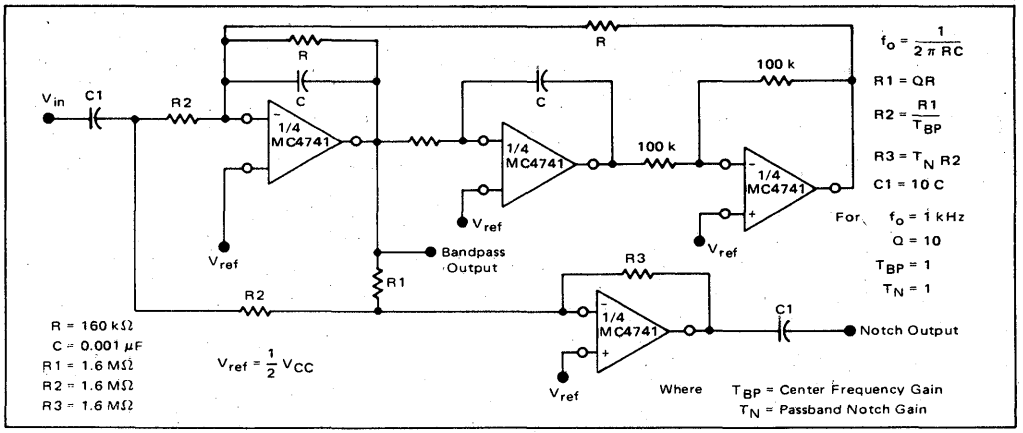


FIGURE 7 – NON-INVERTING PULSE RESPONSE

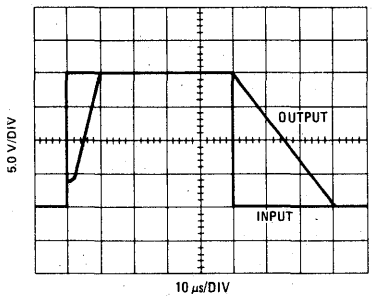


FIGURE 8 – OPEN LOOP VOLTAGE GAIN versus SUPPLY VOLTAGE

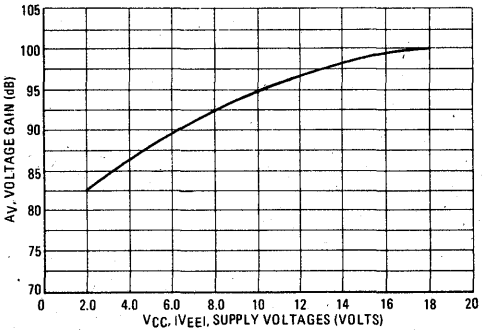


FIGURE 9 – TRANSIENT RESPONSE TEST CIRCUIT

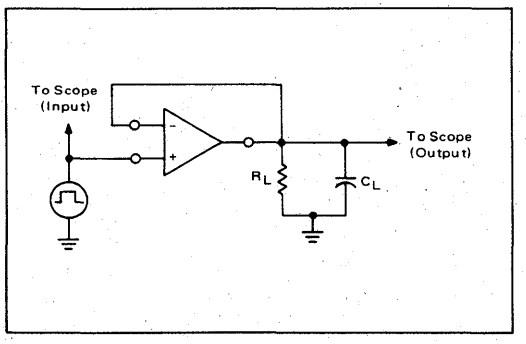
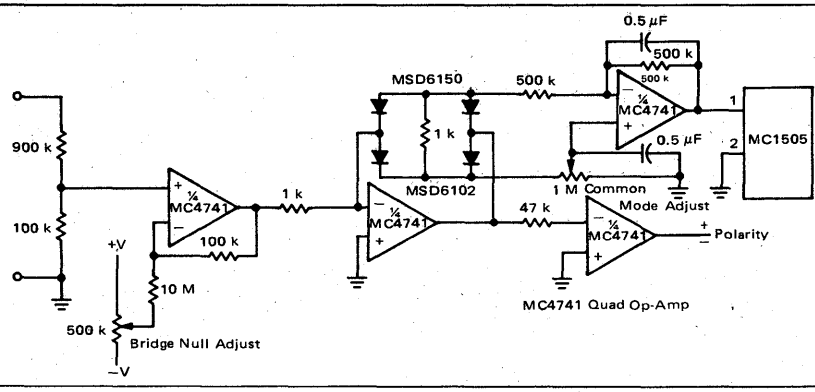


FIGURE 10 – ABSOLUTE VALUE DVM FRONT END



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MLM101AG	LM101AH	−55°C to +125°C	Metal Can
MLM101AU	—	−55°C to +125°C	Ceramic DIP
MLM201AG	—	−25°C to +85°C	Metal Can
MLM201AP1	—	−25°C to +85°C	Plastic DIP
MLM201AU	—	−25°C to +85°C	Ceramic DIP
MLM301AG	LM301AH	0°C to +70°C	Metal Can
MLM301AP1	LM301AN	0°C to +70°C	Plastic DIP
MLM301AU	—	0°C to +70°C	Ceramic DIP

MLM101A
MLM201A
MLM301A

3

OPERATIONAL AMPLIFIER

A general purpose operational amplifier that allows the user to choose the compensation capacitor best suited to his needs. With proper compensation summing amplifier slew rates to 10 V/μs can be obtained.

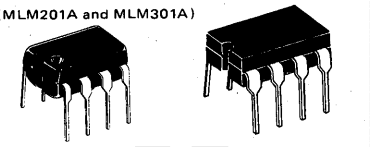
- Low Input Offset Current – 20 nA maximum Over Temperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short-Circuit Protection
- Guaranteed Drift Characteristics

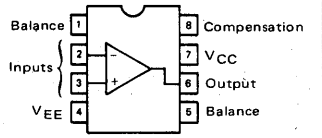
OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MLM201A and MLM301A)

U SUFFIX
CERAMIC PACKAGE
CASE 693





G SUFFIX
METAL PACKAGE
CASE 601

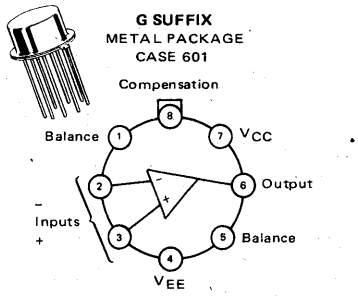


FIGURE 1 – STANDARD COMPENSATING AND OFFSET BALANCING CIRCUIT

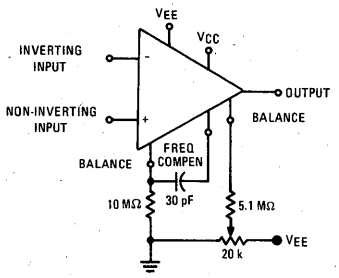
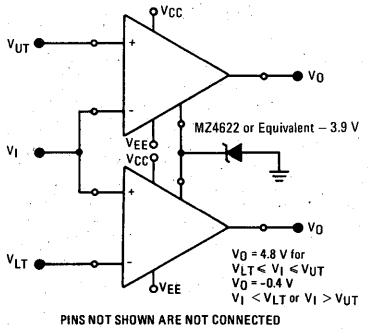
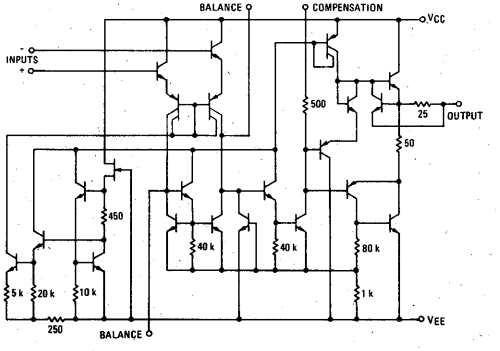


FIGURE 2 – DOUBLE-ENDED LIMIT DETECTOR



PINS NOT SHOWN ARE NOT CONNECTED

FIGURE 3 – REPRESENTATIVE CIRCUIT SCHEMATIC



MAXIMUM RATINGS

Rating	Symbol	VALUE MLM101A	VALUE MLM201A	VALUE MLM301A	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±22	±22	±18	Vdc
Input Differential Voltage	V_{ID}	±30			Volts
Input Common-Mode Range (Note 1)	V_{ICR}	±15			Volts
Output Short-Circuit Duration	t_S	Continuous			
Power Dissipation (Package Limitation)	P_D				
Metal Can		500			mW
Derate above T_A = +75°C		6.8			mW/°C
Plastic Dual In-Line Package (MLM201A/301A)		–	625	625	mW
Derate above T_A = +25°C		–	5.0	5.0	mW/°C
Ceramic Package		750			mW
Derate above 25°C		6.6			mW/°C
Operating Ambient Temperature Range	T_A	-55 to +125	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150			°C

Note 1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (T_A = +25°C *unless otherwise noted.*) Unless otherwise specified, these specifications apply for supply voltages from ±5.0 V to ±20 V for the MLM101A and MLM201A, and from ±5.0 V to ±15 V for the MLM301A.

Characteristics	Symbol	MLM101A/MLM201A Min	Typ	Max	MLM301A Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 50$ kΩ)	V_{IO}	–	0.7	2.0	–	2.0	7.5	mV
Input Offset Current	I_{IO}	–	1.5	10	–	3.0	50	nA
Input Bias Current	I_{IB}	–	30	75	–	70	250	nA
Input Resistance	r_i	1.5	4.0	–	0.5	2.0	–	Megohms
Supply Current	I_{CC}, I_{EE}							mA
V_{CC}/V_{EE} = ±20 V		–	1.8	3.0	–	–	–	
V_{CC}/V_{EE} = ±15 V		–	–	–	–	1.8	3.0	
Large Signal Voltage Gain	A_V							V/mV
V_{CC}/V_{EE} ±15 V, V_O = ± 10 V, R_L > 2.0 kΩ)		50	160	–	25	160	–	

The following specifications apply over the operating temperature range.

Input Offset Voltage ($R_S \leq$ 50 kΩ)	V_{IO}	–	–	3.0	–	–	10	mV
Input Offset Current	I_{IO}	–	–	20	–	–	70	nA
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$							µV/°C
$T_{A(min)} \leq T_A \leq T_{A(max)}$		–	3.0	15	–	6.0	30	
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$							nA/°C
+25°C $\leq T_A \leq T_{A(max)}$		–	0.01	0.1	–	0.01	0.3	
$T_{A(min)} \leq T_A \leq$ 25°C		–	0.02	0.2	–	0.02	0.6	
Input Bias Current	I_{IB}	–	–	100	–	–	300	nA
Large Signal Voltage Gain	A_V							V/mV
V_{CC}/V_{EE} = ± 15 V, V_O = ± 10 V, R_L > 2.0 kΩ		25	–	–	15	–	–	
Input Voltage Range	V_I							V
V_{CC}/V_{EE} = ±20 V		±15	–	–	–	–	–	
V_{CC}/V_{EE} = ±15 V		–	–	–	±12	–	–	
Common-Mode Rejection Ratio	CMRR							dB
$R_S \leq$ 50 kΩ		80	96	–	70	90	–	
Supply Voltage Rejection Ratio	PSSR							dB
$R_S \leq$ 50 kΩ		80	96	–	70	96	–	
Output Voltage Swing	V_O							V
V_{CC}/V_{EE} = ±15 V, R_L = 10 kΩ		±12	±14	–	±12	+14	–	
R_L = 2.0 kΩ		±10	±13	–	±10	±13	–	
Supply Currents ($T_A = T_{A(max)}$, V_{CC}/V_{EE} = ±20 V)	I_{CC}, I_{EE}	–	1.2	2.5	–	–	–	mA

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TYPICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 4 – MINIMUM INPUT VOLTAGE RANGE

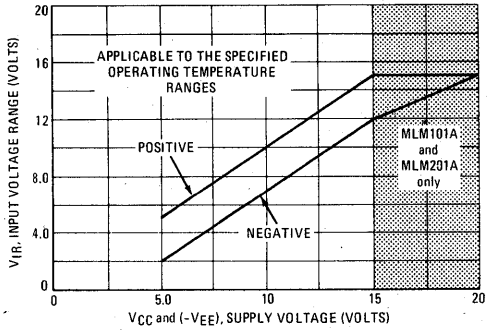


FIGURE 5 – MINIMUM OUTPUT VOLTAGE SWING

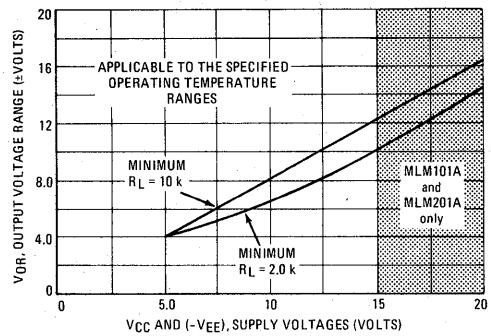


FIGURE 6 – MINIMUM VOLTAGE GAIN

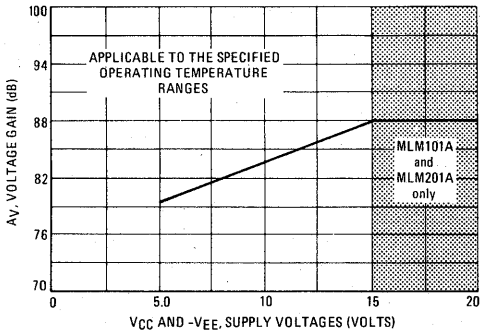


FIGURE 7 – TYPICAL SUPPLY CURRENTS

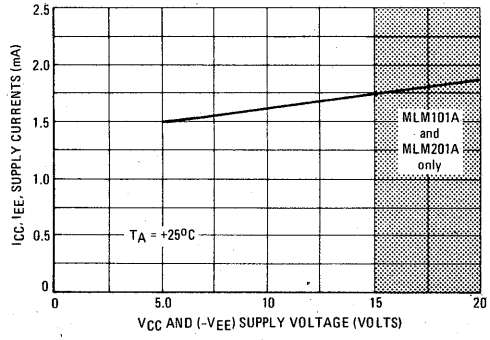


FIGURE 8 – OPEN-LOOP FREQUENCY RESPONSE

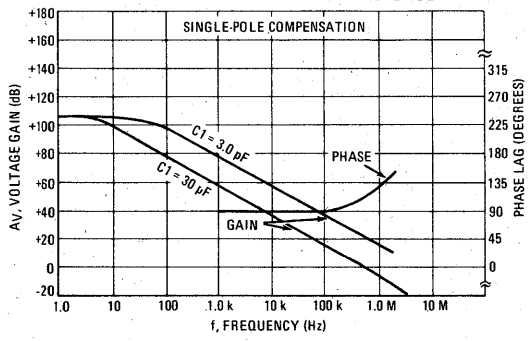
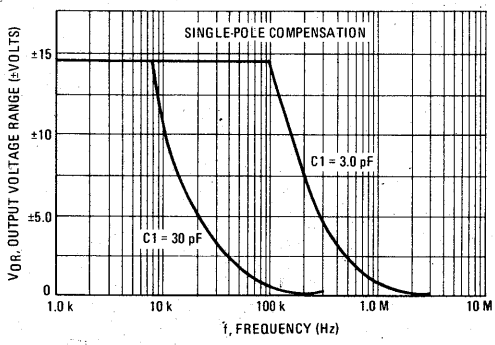


FIGURE 9 – LARGE-SIGNAL FREQUENCY RESPONSE



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 10 – VOLTAGE FOLLOWER PULSE RESPONSE

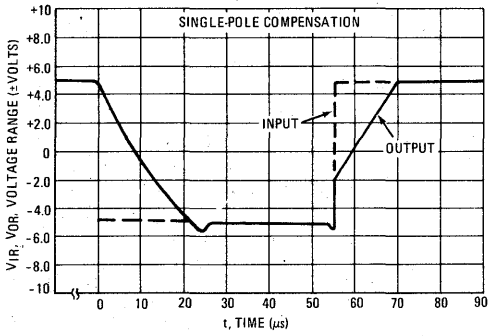


FIGURE 11 – OPEN-LOOP FREQUENCY RESPONSE

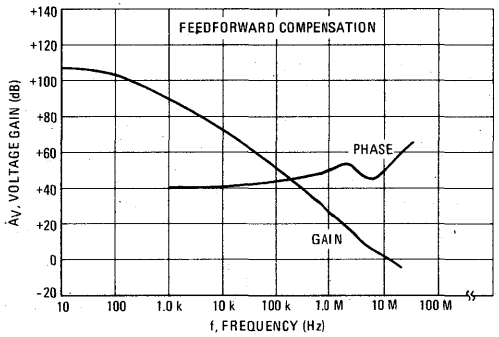


FIGURE 12 – LARGE-SIGNAL FREQUENCY RESPONSE

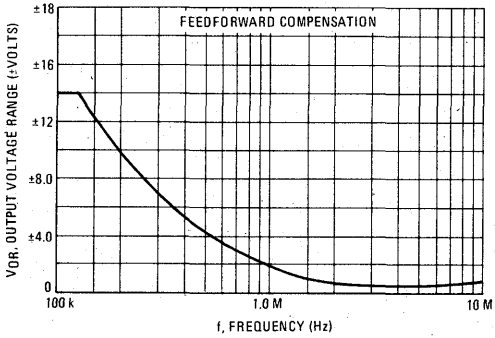
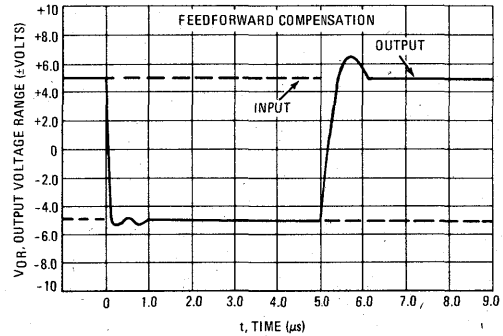


FIGURE 13 – INVERTER PULSE RESPONSE



TYPICAL COMPENSATION CIRCUITS

FIGURE 14 – SINGLE-POLE COMPENSATION

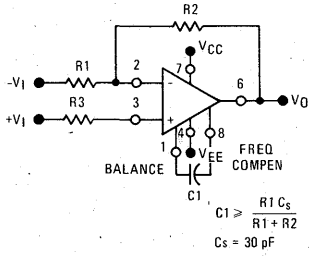
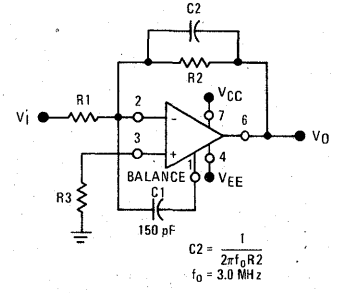


FIGURE 15 – FEEDFORWARD COMPENSATION



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MLM107G	—	−55°C to +125°C	Metal Can
MLM107U	—	−55°C to +125°C	Ceramic DIP
MLM207G	—	−25°C to +85°C	Metal Can
MLM207U	—	−25°C to +85°C	Ceramic DIP
MLM307G	—	0°C to +70°C	Metal Can
MLM307P1	LM307N	0°C to +70°C	Plastic DIP
MLM307U	—	0°C to +70°C	Ceramic DIP

MLM107
MLM207
MLM307

3

INTERNALLY COMPENSATED MONOLITHIC OPERATIONAL AMPLIFIER

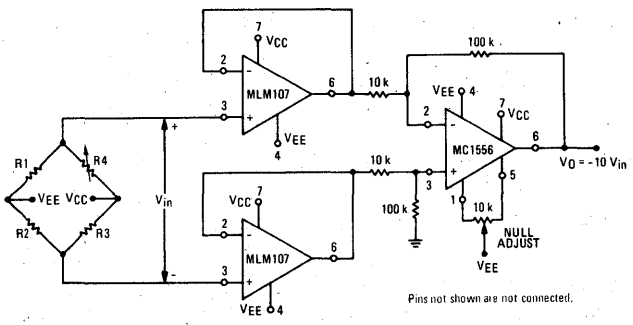
A general purpose operational amplifier series well suited for applications requiring lower input currents than are available with the popular MC1741. These improved input characteristics permit greater accuracy in sample and hold circuits and long interval integrators.

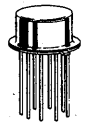
- Internally Compensated
- Low Offset Voltage: 2.0 mV max (MLM107)
- Low Input Offset Current: 10 nA max (MLM107)
- Low Input Bias Current: 75 nA max (MLM107)

OPERATIONAL AMPLIFIER INTEGRATED CIRCUIT

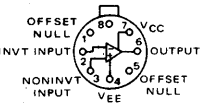
EPITAXIAL PASSIVATED

TYPICAL APPLICATION
HIGH IMPEDANCE BRIDGE AMPLIFIER

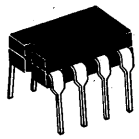




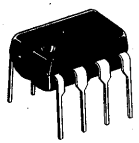
G SUFFIX
METAL PACKAGE
CASE 601-02



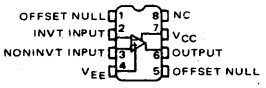
(Top View)



P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1741SC Only)

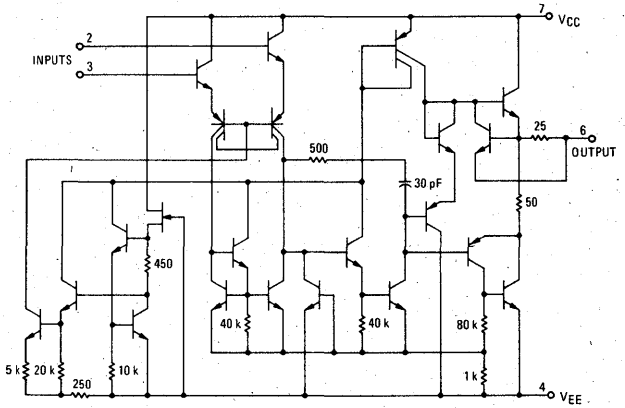


U SUFFIX
CERAMIC PACKAGE
CASE 693

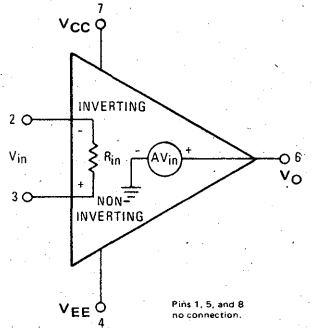


(Top View)

CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MLM107	MLM207	MLM307	Unit
Power Supply Voltages	V_{CC} V_{EE}	+22 -22	+22 -22	+18 -18	Vdc
Differential Input Signal Voltage	V_{ID}	±30	±30	±30	Volts
Common-Mode Input Swing (Note 1)	V_{ICR}	±15	±15	±15	Volts
Output Short-Circuit Duration	t_{OS}	Indefinite			
Power Dissipation (Package Limitation) (Note 2)	P_D	500	500	500	mW
Operating Temperature Range	T_A	-55 to +125	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted, see Note 3.)

Characteristics	Symbol	MLM107 MLM207			MLM307			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$\|V_{IO}\|$							mV
$R_S \leq 10\ k\Omega$, T_A = +25°C		–	0.7	2.0	–	–	–	
$R_S \leq 10\ k\Omega$, $T_A = T_{low}$ to T_{high}		–	–	3.0	–	–	–	
$R_S \leq 50\ k\Omega$, T_A = +25°C		–	–	–	–	2.0	7.5	
$R_S \leq 50\ k\Omega$, $T_A = T_{low}$ to T_{high}		–	–	–	–	–	10	
Input Offset Current	$\|I_{IO}\|$							nA
T_A = +25°C		–	1.5	10	–	3.0	50	
$T_A = T_{low}$ to T_{high}		–	–	20	–	–	70	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	30	75	–	70	250	
$T_A = T_{low}$ to T_{high}		–	–	100	–	–	300	
Input Resistance	R_{in}	1.5	4.0	–	0.5	2.0	–	Megohms
Supply Current	I_D							mA
V_S = ±20 V, T_A = +25°C		–	1.8	3.0	–	–	–	
V_S = ±20 V, $T_A = T_{high}$		–	1.2	2.5	–	–	–	
V_S = ±15 V, T_A = +25°C		–	–	–	–	1.8	3.0	
Large-Signal Voltage Gain	A_V							V/mV
V_S = ±15 V, V_O = ±10 V, $R_L \geq 2.0\ k\Omega$, T_A = +25°C		50	160	–	25	160	–	
V_S = ±15 V, V_O = ±10 V, $R_L \geq 2.0\ k\Omega$, $T_A = T_{low}$		25	–	–	15	–	–	
Average Temperature Coefficient of Input Offset Voltage	$\|TC_{V_{IO}}\|$							µV/°C
$T_{low} \leq T_A \leq T_{high}$		–	3.0	15	–	6.0	30	
Average Temperature Coefficient of Input Offset Current	$\|TC_{I_{IO}}\|$							nA/°C
+25°C ≤ $T_A \leq T_{high}$		–	0.01	0.1	–	0.01	0.3	
$T_{low} \leq T_A \leq$ +25°C		–	0.02	0.2	–	0.02	0.6	
Output Voltage Swing ($T_A = T_{low}$ to T_{high})	V_O							V
V_S = ±15 V, R_L = 10 kΩ		±12	±14	–	±12	+14	–	
R_L = 2.0 kΩ		±10	±13	–	±10	±13	–	
Input Voltage Range ($T_A = T_{low}$ to T_{high})	$V_{in\ R}$							V
V_S = ±20 V		±15	–	–	–	–	–	
V_S = ±15 V		–	–	–	±12	–	–	
Common-Mode Rejection Ratio ($T_A = T_{low}$ to T_{high})	CMRR							dB
$R_S \leq 50\ k\Omega$		80	96	–	70	90	–	
Supply-Voltage Rejection Ratio ($T_A = T_{low}$ to T_{high})	VSRR							dB
$R_S \leq 50\ k\Omega$		80	96	–	70	96	–	

Note 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Note 2. For operating at elevated temperatures, the device must be derated based on a maximum junction temperature of +150°C for the MLM107, and 100°C for the MLM207 and MLM307. The TO-99 package is derated based on a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case.

Note 3. Unless otherwise noted, these specifications apply for:

	T_{low}	T_{high}
±5.0 V ≤ $V_S \leq$ ±20 V,	-55°C ≤ $T_A \leq$	+125°C, MLM107
±5.0 V ≤ $V_S \leq$ ±20 V,	-25°C ≤ $T_A \leq$	+85°C, MLM207
±5.0 V ≤ $V_S \leq$ ±15 V,	0°C ≤ $T_A \leq$	+70°C, MLM307

3

TYPICAL CHARACTERISTICS

(V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 1 – MINIMUM INPUT VOLTAGE RANGE

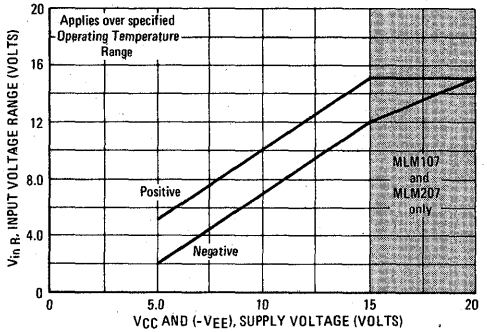


FIGURE 2 – MINIMUM OUTPUT VOLTAGE SWING

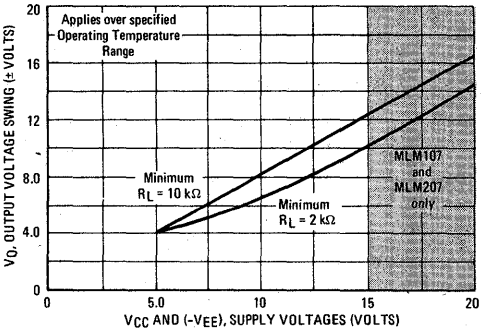


FIGURE 3 – MINIMUM VOLTAGE GAIN

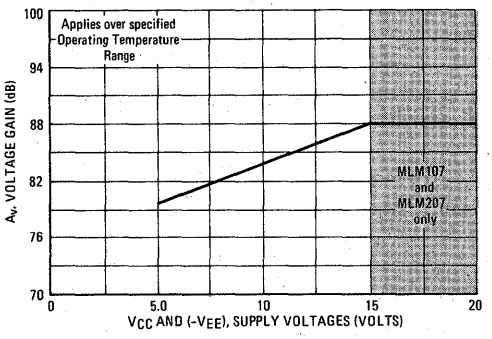


FIGURE 4 – TYPICAL SUPPLY CURRENTS

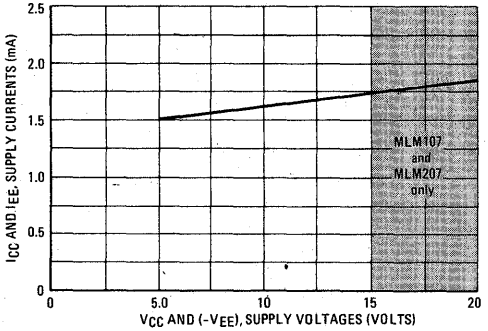


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

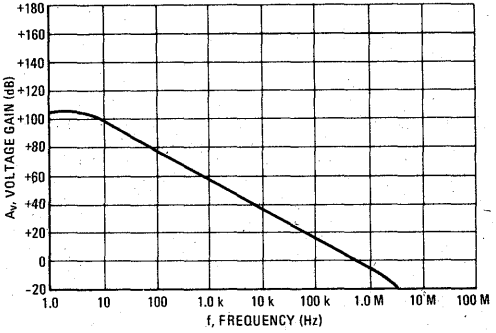
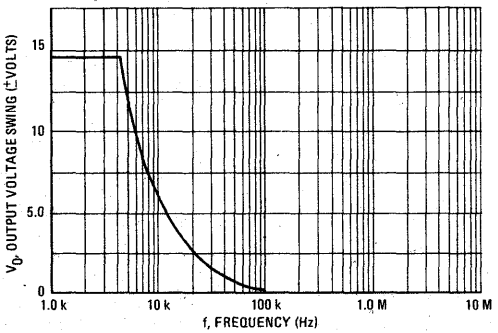
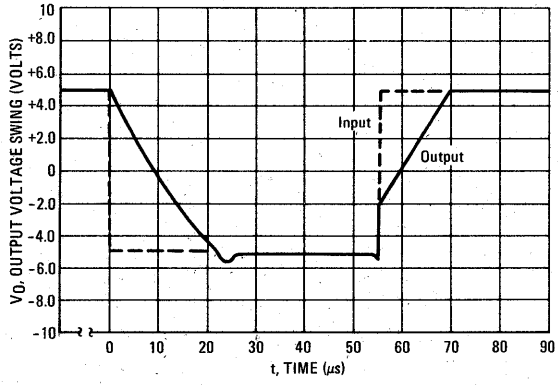


FIGURE 6 – LARGE-SIGNAL FREQUENCY RESPONSE



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – VOLTAGE FOLLOWER PULSE RESPONSE



MLM108, MLM108A
MLM208, MLM208A
MLM308, MLM308A

3

PRECISION OPERATIONAL AMPLIFIERS

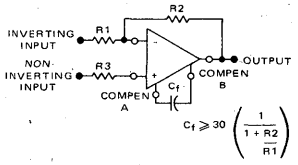
The MLM108/MLM208/MLM308 Series operational amplifiers provide high input impedance, low input offsets and temperature drifts, and low noise. These characteristics are made possible by use of a special Super Beta processing technology. This series of amplifiers is particularly useful for applications where high-accuracy and low-drift performance are essential. In addition high-speed performance may be improved by employing feed-forward compensation techniques to maximumize slew rate without compromising other performance criteria.

The MLM108A/MLM208A/MLM308A Series offers extremely low input offset voltage and drift specifications allowing usage in even the most critical applications without external offset nulling.

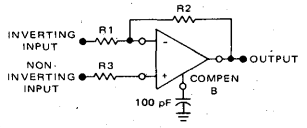
- Operation From a Wide Range of Power Supply Voltages
- Low Input Bias and Offset Currents
- Low Input Offset Voltage and Guaranteed Offset Voltage Drift Performance
- High Input Impedance
- Laser Trimmed and Ion Implanted

FREQUENCY COMPENSATION

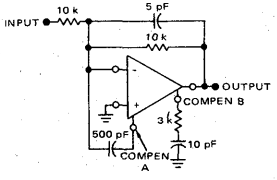
STANDARD COMPENSATION



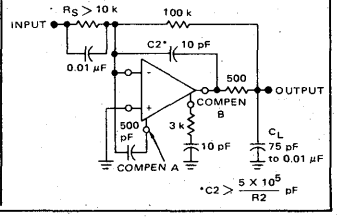
MODIFIED COMPENSATION



STANDARD FEEDFORWARD COMPENSATION



FEEDFORWARD COMPENSATION FOR DECOUPLING LOAD CAPACITANCE



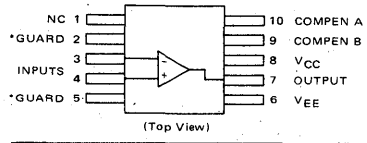
DEVICE SELECTION TABLE

	OPERATING TEMPERATURE RANGE		
	-55 to +125°C	-25 to +85°C	0 to +70°C
STANDARD OFFSET VOLTAGE SPECIFICATION	MLM108 Pkg. Suffix F, G or L	MLM208 Pkg. Suffix F, G or L	MLM308 Pkg. Suffix F, G, L or P1
TIGHTENED OFFSET VOLTAGE SPECIFICATION	MLM108A Pkg. Suffix F, G or L	MLM208A Pkg. Suffix F, G or L	MLM308A Pkg. Suffix F, G or L

LASER TRIMMED SUPER GAIN OPERATIONAL AMPLIFIERS

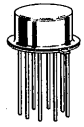
SILICON MONOLITHIC INTEGRATED CIRCUIT

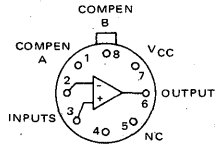
F SUFFIX
CERAMIC PACKAGE
CASE 606-04
TO-91



(Top View)

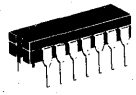
G SUFFIX
METAL PACKAGE
CASE 601

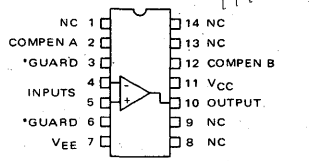




(Top View)

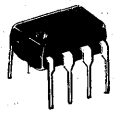
L SUFFIX
CERAMIC PACKAGE
CASE 632-02
TO-116

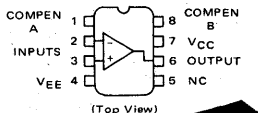




(Top View)

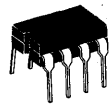
P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MLM308 Only)





(Top View)

U SUFFIX
CERAMIC PACKAGE
CASE 693



*Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	VALUE			Unit
		MLM108, MLM108A	MLM208, MLM208A	MLM308, MLM308A	
Power Supply Voltage	V_{CC}, V_{EE}	±20	±20	±18	Vdc
Input Voltage (See Note 1)	V_I	±15			Volts
Input Differential Current (See Note 2)	I_{ID}	±10			mA
Output Short-Circuit Duration	t_S	Indefinite			
Operating Ambient Temperature Range	T_A	-55 to +125	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150			°C
Junction Temperature Metal, Ceramic Package Plastic Package	T_J	 +175 +150			°C

Note 1. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.

Note 2. The inputs are shunted with back-to-back diodes for over-voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1.0 V is applied between the inputs unless some limiting resistance is used.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted these specifications apply for supply voltages of +5.0 V ≤ V_{CC} ≤ +20 V and -5.0 V ≥ V_{EE} ≥ -20 V, T_A = +25°C.)

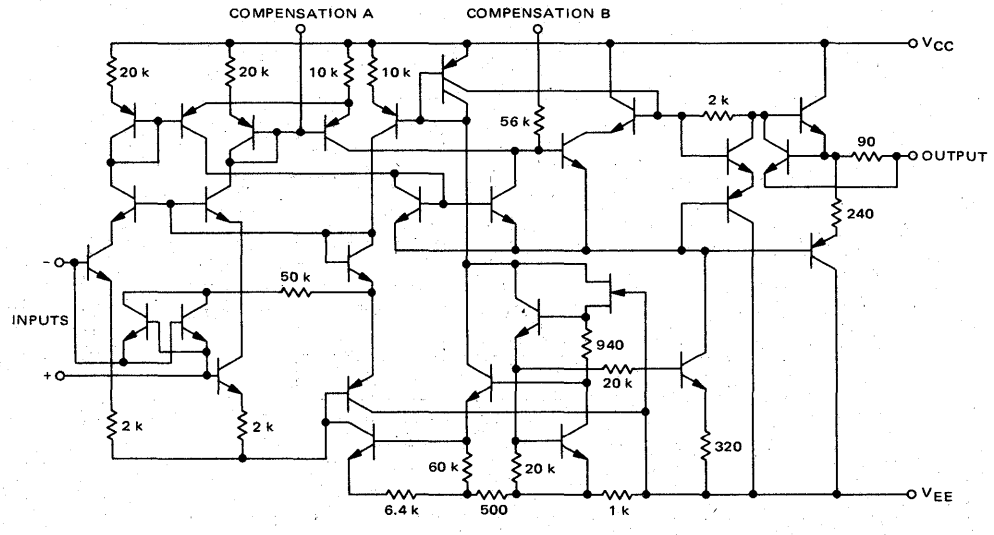
Characteristic	Symbol	MLM108A MLM208A			MLM108 MLM208			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	0.3	0.5	–	0.7	2.0	mV
Input Offset Current	I_{IO}	–	0.05	0.2	–	0.005	0.2	nA
Input Bias Current	I_{IB}	–	0.8	2.0	–	0.8	2.0	nA
Input Resistance	r_i	30	70	–	30	70	–	Megohms
Power Supply Currents V_{CC} = +20 V, V_{EE} = -20 V	I_{CC}, I_{EE}	–	±0.3	±0.6	–	±0.3	±0.6	mA
Large Signal Voltage Gain V_{CC} = $\|V_{EE}\|$ = +15 V, V_O = ±10 V, R_L ≥ 10 kΩ	A_{VOL}	80	300	–	50	300	–	V/mV
The following specifications apply over the operating temperature range.								
Input Offset Voltage	V_{IO}	–	–	1.0	–	–	3.0	mV
Input Offset Current	I_{IO}	–	–	0.4	–	–	0.4	nA
Average Temperature Coefficient of Input Offset Voltage T_A(min) ≤ T_A ≤ T_A(max)	$\Delta V_{IO}/\Delta T$	–	1.0	5.0	–	3.0	15	μV/°C
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	–	0.5	2.5	–	0.5	2.5	pA/°C
Input Bias Current	I_{IB}	–	–	3.0	–	–	3.0	nA
Large Signal Voltage Gain V_{CC} = $\|V_{EE}\|$ = +15 V, V_O = ±10 V, R_L = 10 kΩ	A_{VOL}	40	–	–	25	–	–	V/mV
Input Voltage Range V_{CC} = $\|V_{EE}\|$ = +15 V	V_{IR}	±13.5	–	–	±13.5	–	–	V
Common-Mode Rejection Ratio	CMRR	96	110	–	85	100	–	dB
Power Supply Voltage Rejection Ratio	PSSR	96	100	–	80	96	–	dB
Output Voltage Range V_{CC} = $\|V_{EE}\|$ = +15 V, R_L = 10 kΩ	V_{OR}	±13	±14	–	±13	±14	–	V
Supply Current (T_A = T_A[max])	I_{CC}, I_{EE}	–	±0.15	±0.4	–	±0.15	±0.4	mA

3

ELECTRICAL CHARACTERISTICS (*Unless otherwise noted these specifications apply for supply voltages of +5.0 V ≤ V_{CC} ≤ +15 V and −5.0 V ≥ V_{EE} ≥ −15 V, T_A = +25°C.*)

Characteristic	Symbol	MLM308A			MLM308			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	0.2	0.3	–	0.2	0.3	mV
Input Offset Current	I_{IO}	–	0.2	1.0	–	0.2	1.0	nA
Input Bias Current	I_{IB}	–	1.5	7.0	–	1.5	7.0	nA
Input Resistance	r_i	10	40	–	10	40	–	Megohms
Power Supply Currents V_{CC} = +15 V, V_{EE} = −15 V	I_{CC},I_{EE}	–	±0.3	±0.8	–	±0.3	±0.8	mA
Large Signal Voltage Gain V_{CC} = +15 V, V_{EE} = −15 V, V_O = ±10 V, R_L ≥ 10 kΩ	A_{VOL}	80	300	–	25	300	–	V/mV
The following specifications apply over the operating temperature range.								
Input Offset Voltage	V_{IO}	–	–	0.73	–	–	10	mV
Input Offset Current	I_{IO}	–	–	1.5	–	–	1.5	nA
Average Temperature Coefficient of Input Offset Voltage T_A(min) ≤ T_A ≤ T_A(max)	$\Delta V_{IO}/\Delta T$	–	1.0	5.0	–	6.0	30	µV/°C
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	–	2.0	10	–	2.0	10	pA/°C
Input Bias Current	I_{IB}	–	–	10	–	–	10	nA
Large Signal Voltage Gain V_{CC} = +15 V, V_{EE} = −15 V, V_O = ±10 V, R_L ≥ 10 kΩ	A_{VOL}	60	–	–	15	–	–	V/mV
Input Voltage Range V_{CC} = +15 V, V_{EE} = −15 V	V_{IR}	±13.5	–	–	±13.5	–	–	V
Common-Mode Rejection Ratio R_S ≤ 50 kΩ	CMRR	96	110	–	80	100	–	dB
Supply Voltage Rejection Ratio R_S ≤ 50 kΩ	PSSR	96	110	–	80	96	–	dB
Output Voltage Range V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kΩ	V_{OR}	±13	±14	–	±13	±14	–	V

REPRESENTATIVE CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

FIGURE 1 – INPUT BIAS AND INPUT OFFSET CURRENTS

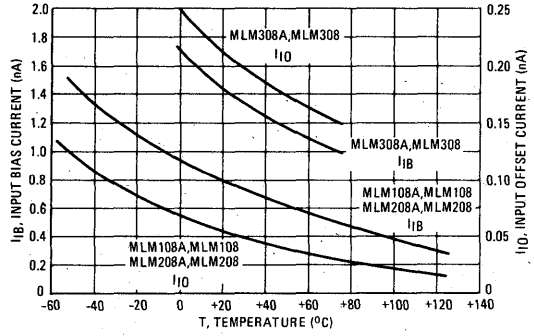


FIGURE 2 – MAXIMUM EQUIVALENT INPUT OFFSET VOLTAGE ERROR versus INPUT RESISTANCE

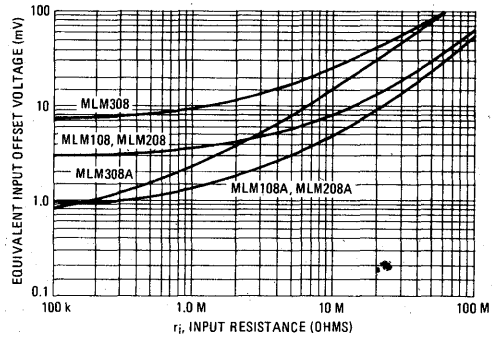


FIGURE 3 – VOLTAGE GAIN versus SUPPLY VOLTAGES

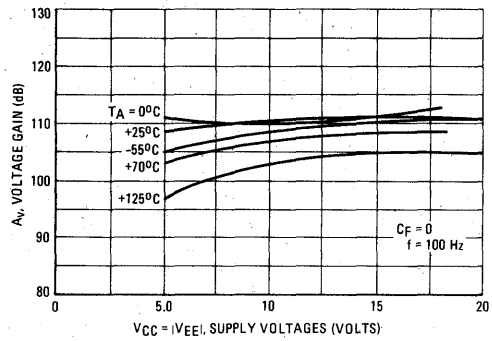


FIGURE 4 – POWER SUPPLY CURRENTS versus POWER SUPPLY VOLTAGE

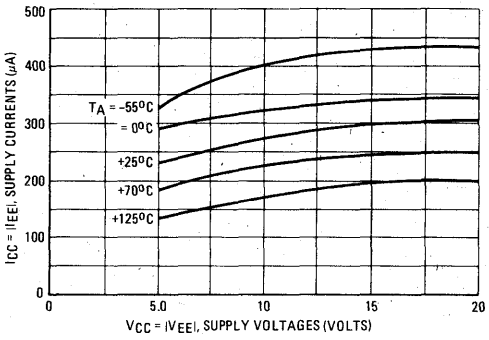


FIGURE 5 – OPEN-LOOP FREQUENCY RESPONSE

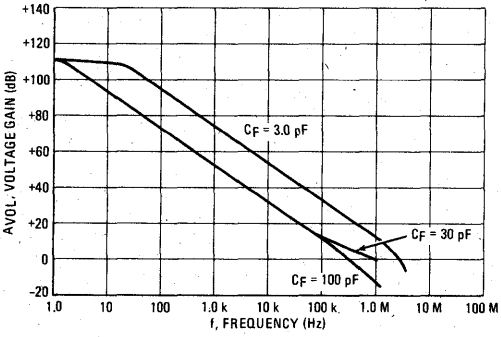
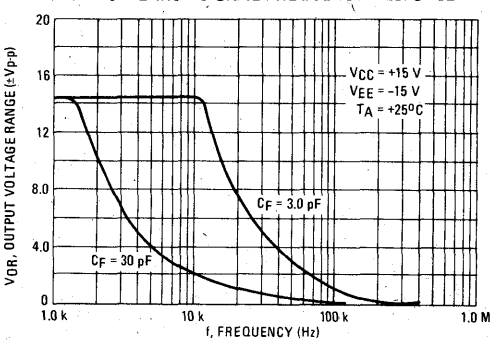


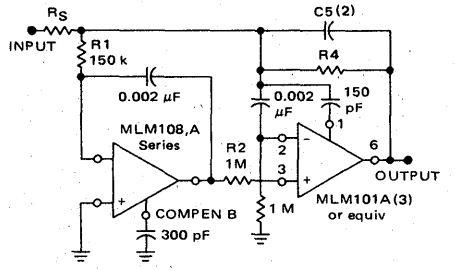
FIGURE 6 – LARGE-SIGNAL FREQUENCY RESPONSE



3

SUGGESTED DESIGN APPLICATIONS

FIGURE 7 – FAST (1) SUMMING AMPLIFIER WITH LOW INPUT CURRENT

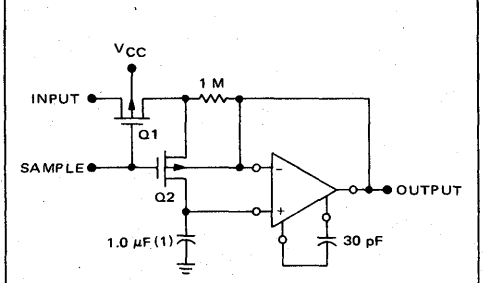


(1) Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10 V/μs

(2) $C5 = \frac{6 \times 10^{-8}}{R1}$

(3) In addition to increasing speed, the MLM101A raises high and low frrequency gain, increases output drive capability and eliminates thermal feedback.

FIGURE 8 – SAMPLE AND HOLD



(1) Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

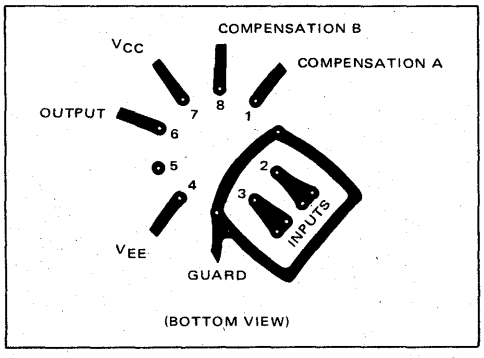
INPUT GUARDING

Special care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the MLM108,A amplifier series. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at +125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 type package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the boards. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

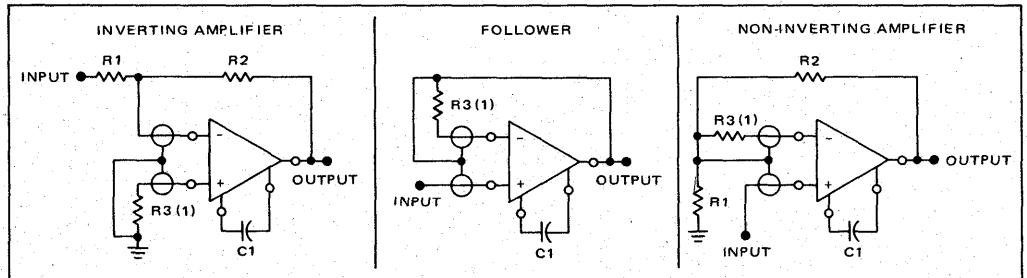
The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard MC1741 and MLM101A pin configuration).

FIGURE 9 – SUGGESTED PRINTED CIRCUIT BOARD LAYOUT for INPUT GUARDING USING METAL PACKAGED DEVICE



(BOTTOM VIEW)

FIGURE 10 – CONNECTION OF INPUT GUARDS



(1) Used to compensate for large source resistances.

Note: $\frac{R1\,R2}{R1 + R2}$ must be an impedance.

ORDERING INFORMATION

Device	Temperature Range	Package
MLM110G	−55°C to +125°C	Metal Can
MLM110U	−55°C to +125°C	Ceramic DIP
MLM210G	−25°C to +85°C	Metal Can
MLM210U	−25°C to +85°C	Ceramic DIP
MLM310G	0°C to +70°C	Metal Can
MLM310P1	0°C to +70°C	Plastic DIP
MLM310U	0°C to +70°C	Ceramic DIP

MLM110
MLM210
MLM310

OPERATIONAL AMPLIFIER VOLTAGE FOLLOWER

THE MLM110, MLM210, and MLM310 are functionally, electrically, and pin-for-pin equivalent to the LM110, LM210, and LM310 respectively.

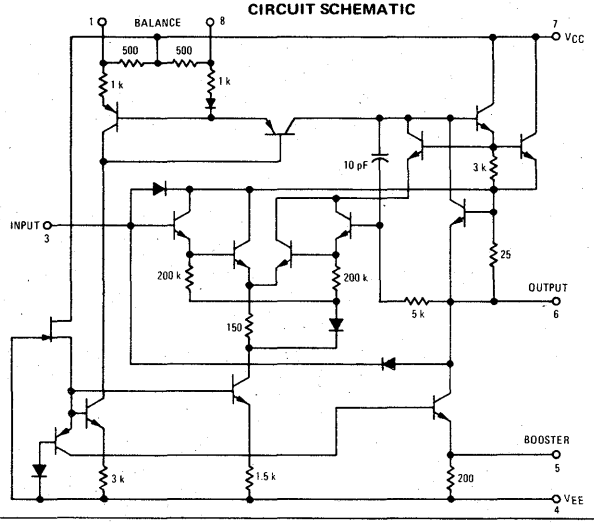
- Input Bias Current: 10 nA maximum over Temperature Range
- Small-Signal Bandwidth: 20 MHz typical
- Slew Rate: 30 Volts/μs typical
- Supply Voltage Range: ± 5.0 V to ± 18 V

OPERATIONAL AMPLIFIER VOLTAGE FOLLOWER

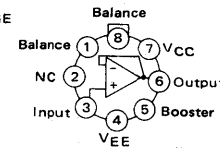
INTEGRATED CIRCUIT

3

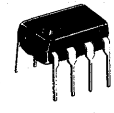
CIRCUIT SCHEMATIC



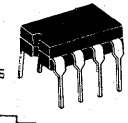
G SUFFIX
METAL PACKAGE
CASE 601

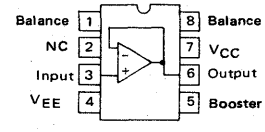


P1 SUFFIX
PLASTIC PACKAGE
CASE 626



U SUFFIX
CERAMIC PACKAGE
CASE 693





TYPICAL APPLICATIONS

FIGURE 1 – OFFSET BALANCING CIRCUIT

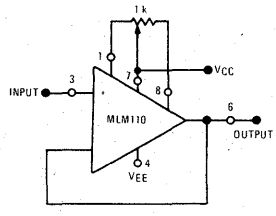
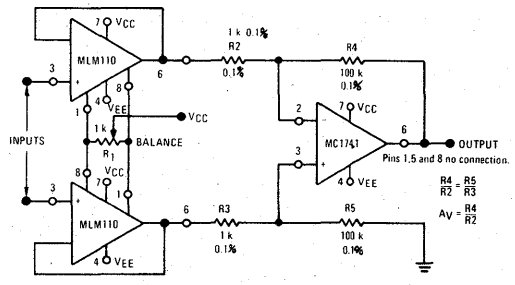


FIGURE 2 – DIFFERENTIAL INPUT INSTRUMENTATION AMPLIFIER



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MLM110	MLM210	MLM310	Unit
Power Supply Voltage	V_{CC}(max) V_{EE}(max)	+18 -18	+18 -18	+18 -18	Vdc
Input Voltage (Note 1)	V_{IC}	± 15	± 15	± 15	Volts
Output Short Circuit Duration (Note 2)	T_{sc}		Indefinite		
Operating Temperature Range	T_A	-55 to +125	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C
Lead Temperature (soldering, t = 10 s)	T_S	300	300	300	°C
Junction Temperature Ceramic, Metal Package Plastic Package	T_J		175 150		°C

ELECTRICAL CHARACTERISTICS (See Note 4)

Characteristic	Symbol	MLM110 MLM210			MLM310			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage T_A = +25°C T_A = T_{low}* to T_{high}**	V_{IO}	– –	1.5 –	4.0 6.0	– –	2.5 –	7.5 10	mV
Input Bias Current T_A = +25°C T_A = T_{low} to T_{high}	I_{IB}	– –	1.0 –	3.0 10	– –	2.0 –	7.0 10	nA
Input Resistance	r_i	10^{10}	10^{12}	–	10^{10}	10^{12}	–	ohms
Input Capacitance	C_i	–	1.5	–	–	1.5	–	pF
Large-Signal Voltage Gain (V_S = ± 15 V, V_O = +10 V) T_A = +25°C, R_L = 8.0 k ohms T_A = T_{low} to T_{high}, R_L = 10 k ohms	A_{VS}	 0.999 0.999	 0.9999 –	 – –	 0.999 0.999	 0.9999 –	 – –	V/V
Output Resistance T_A = +25°C	r_o	–	0.75	2.5	–	0.75	2.5	ohms
Small-Signal Bandwidth	BW	–	20	–	–	20	–	MHz
Slew Rate	SR	–	30	–	–	30	–	V/μs
Supply Current T_A = +25°C T_A = T_{high}	I_D	– –	3.9 2.0	5.5 4.0	– –	3.9 –	5.5 –	mA
Offset Voltage Temperature Drift -55°C ≤ T_A ≤ +85°C T_A = +125°C 0°C ≤ T_A ≤ +70°C	$\Delta V_{IO}/\Delta T$	– – –	6.0 12 –	– – –	– – –	– – 10	– – –	μV/°C
Output Voltage Swing V_S = ± 15 V, R_L = 10 k ohms	V_O	± 10	–	–	± 10	–	–	Volts
Supply Voltage Rejection Ratio ± 5.0 V ≤ V_S ≤ ± 18 V	PSRR	70	80	–	70	80	–	dB

*T_{low} = -55°C for MLM110
= -25°C for MLM210
= 0°C for MLM310

**T_{high} = +125°C for MLM110
= +85°C for MLM210
= +70°C for MLM310

Note 1. For supply voltages less than ± 15 volts, the absolute maximum input voltage is equal to the supply voltage.

Note 2. A continuous short-circuit duration capability is specified for MLM110 and MLM210 as follows: case temperatures up to +125°C and ambient temperatures up to +70°C; for the MLM310 up to +70°C case temperature and +55°C ambient temperature apply. A resistor (greater than 2.0 kilohms) must be inserted in series with the input when the amplifier is driven from a low impedance source, thus preventing damage when the output is shorted.

Note 3. The maximum junction temperature of the MLM110 is +150°C, for the MLM210 — +100°C, and for the MLM310 — +85°C. For operating at elevated temperatures, the package must be derated based on a thermal resistance of 150°C/W — junction to ambient, or 45°C — junction to case.

Note 4. All listed specifications apply for ± 5.0 V ≤ V_S ≤ ±18 V and T_A = +25°C unless otherwise noted.

Note 5. Increased output swing under load can be obtained by connecting an external resistor between the booster and V_{EE} terminals (pins 4 and 5).

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MLM124L	LM124D	−55°C to +125°C	Ceramic DIP
MLM224L	—	−25°C to +85°C	Ceramic DIP
MLM224P	—	−25°C to +85°C	Plastic DIP
MLM324L	LM324D	0°C to +70°C	Ceramic DIP
MLM324P	LM324N	0°C to +70°C	Plastic DIP

MLM124
MLM224
MLM324

Specifications and Applications Information

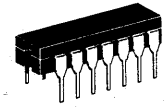
QUAD LOW POWER OPERATIONAL AMPLIFIERS

The MLM124 Series are low-cost, quad operational amplifiers with true differential inputs. These have several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 Volts or as high as 30 Volts with quiescent currents about one fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

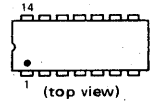
- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 30 Volts
- Low Input Bias Currents: 250 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply

QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

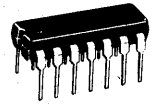
SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



(top view)



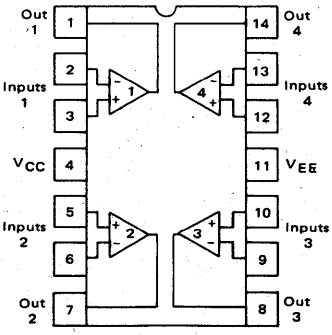
P SUFFIX
PLASTIC PACKAGE
CASE 646
(MLM224 and MLM324 only)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages			Vdc
Single Supply	V_{CC}	32	
Split Supplies	V_{CC}	+16	
	V_{EE}	−16	
Input Differential Voltage Range (1)	V_{IDR}	±32	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	−0.3 to 32	Vdc
Input Forward Current (V_I < −0.3 V)	I_{IF}	50	mA
Package Power Dissipation	P_D		
Plastic Dual-In-Line Package		625	mW
Derate above T_A = 25°C		5.0	mW/°C
Ceramic Dual-In-Line Package		750	mW
Derate above T_A = 25°C		6.0	mW/°C
Storage Temperature Range	T_{stg}		°C
Ceramic Package		−65 to +150	
Plastic Package		−55 to +125	
Operating Ambient Temperature Range	T_A		°C
MLM124		−55 to +125	
MLM224		−25 to +85	
MLM324		0 to +70	

(1) Split Power Supplies.
(2) For Supply Voltages less than 32 V, the absolute maximum input voltage is equal to the supply voltage.

PIN CONNECTIONS



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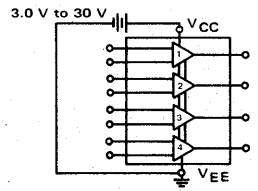
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted.)

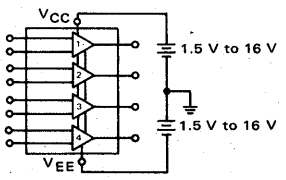
Characteristic	Symbol	MLM124			MLM224,MLM324			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	7.0	mV
$T_A = T_{high}$ to T_{low} (1)		–	–	7.0	–	–	9.0	
Input Offset Current	I_{IO}	–	3.0	30	–	5.0	50	nA
$T_A = T_{high}$ to T_{low}		–	–	100	–	–	150	
Large Signal Open-Loop Voltage Gain	A_{VOL}							V/mV
V_O = ±10 V, R_L = 2.0 kΩ, V_{CC} = 15 V,		50	100	–	25	100	–	
$T_A = T_{high}$ to T_{low}		25	–	–	15	–	–	
Input Bias Current	I_{IB}	–	-45	-150	–	-45	-250	nA
$T_A = T_{high}$ to T_{low}		–	–	-300	–	–	-500	
Common-Mode Rejection Ratio	CMRR	70	85	–	65	70	–	dB
$R_S \leq 10$ kΩ								
Power Supply Current (V_O = 0)	I_{CC}	–	0.8	2.0	–	0.8	2.0	mA
$R_L = \infty$, $T_A = T_{high}$ to T_{low}								
Power Supply Rejection Ratio	PSRR	65	100	–	65	70	–	dB
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	–	10	–	–	10	–	pA/°C
$T_A = T_{high}$ to T_{low}								
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	7.0	–	–	7.0	–	μV/°C
$T_A = T_{high}$ to T_{low}								
Input Common-Mode Voltage Range	V_{ICR}							V
V_{CC} = 30 V		0	–	28.5	0	–	28.5	
V_{CC} = 30 V, $T_A = T_{high}$ to T_{low}		0	–	28	0	–	28	
Amplifier-to-Amplifier Coupling	–	–	-120	–	–	-120	–	dB
1.0 kHz ≤ f ≤ 20 kHz, Input Referenced								
Differential Input Voltage Range	V_{IDR}	–	–	V_{CC}	–	–	V_{CC}	V
Output Voltage Range	V_{OR}	0	3.5	–	0	3.5	–	V
R_L = 2 kΩ								
Output Voltage – High Limit	V_{OH}							V
V_{CC} = 30 V, R_L = 2 kΩ, $T_A = T_{high}$ to T_{low}		26	–	–	26	–	–	
V_{CC} = 30 V, R_L = 10 kΩ, $T_A = T_{high}$ to T_{low}		27	28	–	27	28	–	
Output Voltage – Low Limit	V_{OL}	–	5.0	20	–	5.0	20	mV
V_{CC} = 5.0 V, R_L = 10 kΩ, $T_A = T_{high}$ to T_{low}								
Output Source Current	I_{O+}							mA
V_{ID} = +1.0 V, V_{CC} = 15 V		20	40	–	20	40	–	
V_{ID} = +1.0 V, V_{CC} = 15 V, $T_A = T_{high}$ to T_{low}		10	20	–	10	20	–	
Output Sink Current	I_{O-}							mA
V_{ID} = -1.0 V, V_{CC} = 15 V		10	20	–	10	20	–	
V_{ID} = -1.0 V, V_{CC} = 15 V, $T_A = T_{high}$ to T_{low}		5.0	8.0	–	5.0	8.0	–	
V_{ID} = -1.0 V, V_O = 200 mV		0.012	0.05	–	0.012	0.05	–	

(1) T_{high} = 125°C for MLM124, 70°C for MLM324, 85°C for MLM224.
T_{low} = -55°C for MLM124, 0°C for MLM324, -25°C for MLM224.

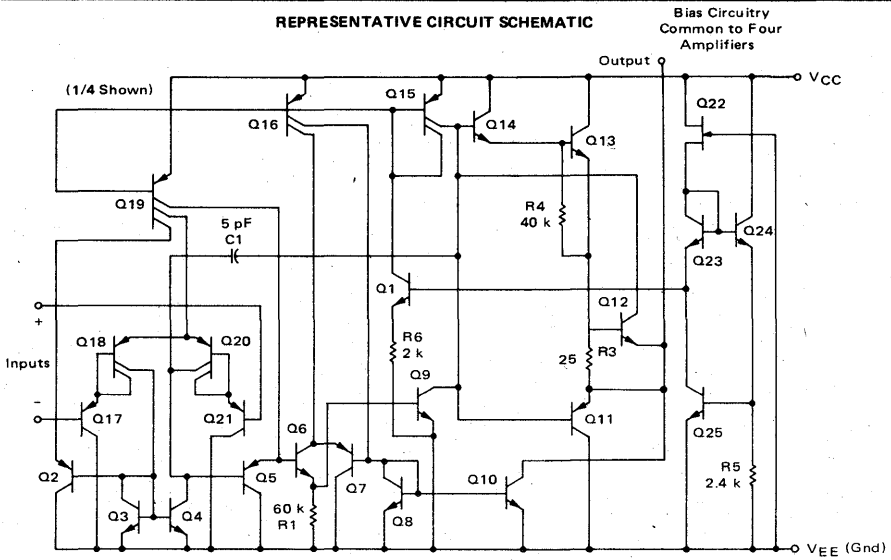
SINGLE SUPPLY



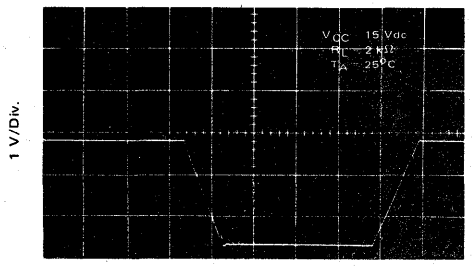
SPLIT SUPPLIES



REPRESENTATIVE CIRCUIT SCHEMATIC



LARGE SIGNAL VOLTAGE FOLLOWER RESPONSE



5.0 μs/Div.

CIRCUIT DESCRIPTION

The MLM124 Series is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

3

TYPICAL PERFORMANCE CURVES

FIGURE 1 – INPUT VOLTAGE RANGE

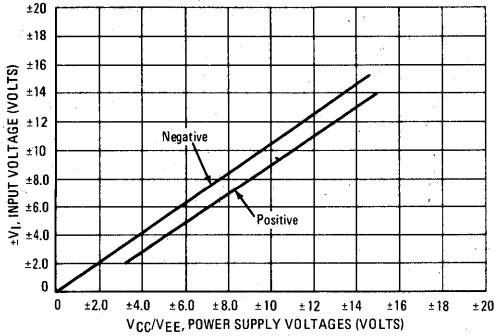


FIGURE 2 – OPEN LOOP FREQUENCY

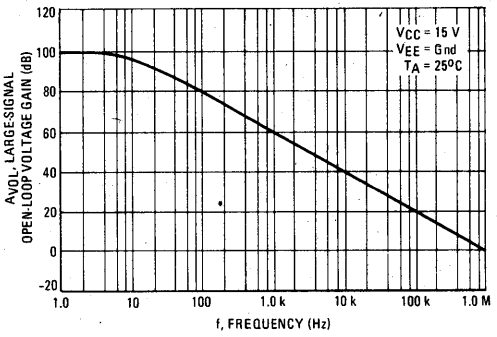


FIGURE 3 – LARGE-SIGNAL FREQUENCY RESPONSE

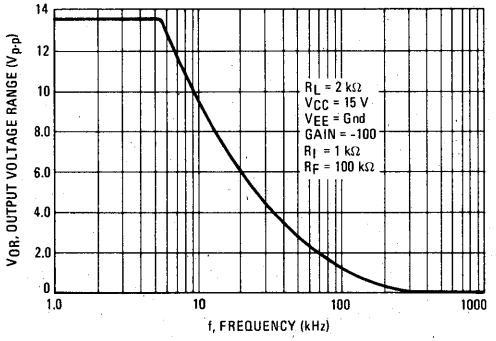


FIGURE 4 – SMALL-SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE
(Non-Inverting)

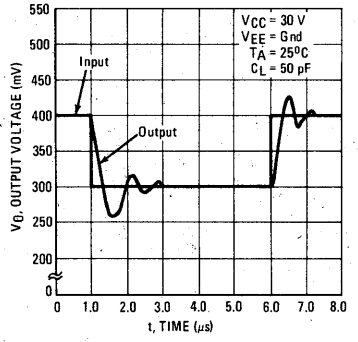


FIGURE 5 – POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

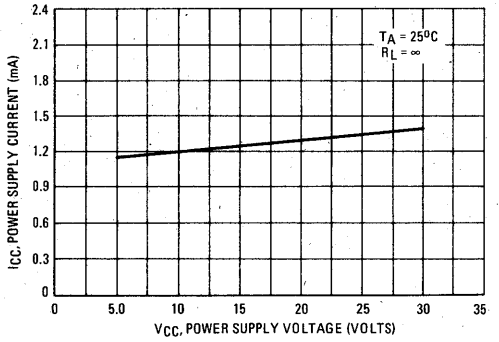
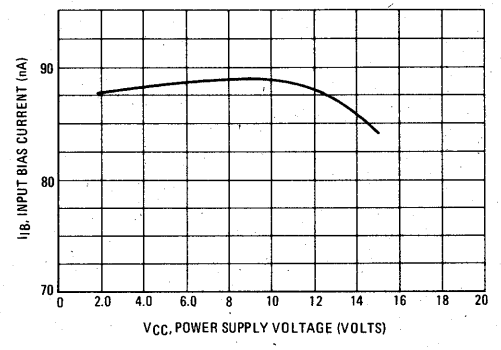
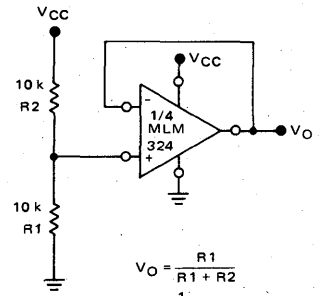


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

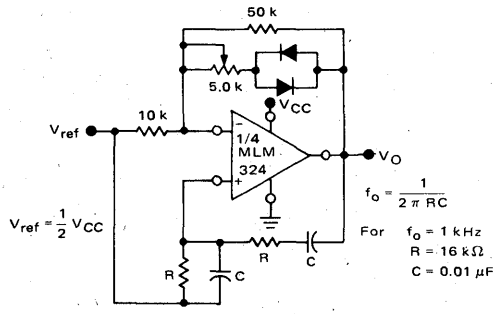
FIGURE 7 – VOLTAGE REFERENCE



$$V_O = \frac{R1}{R1 + R2}$$

$$V_O = \frac{1}{2} V_{CC}$$

FIGURE 8 – WEIN BRIDGE OSCILLATOR

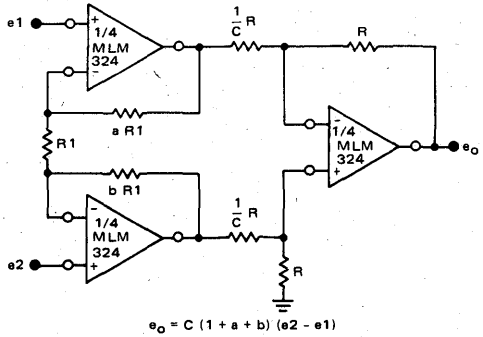


$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_o = \frac{1}{2 \pi RC}$$

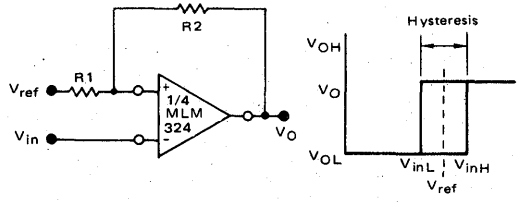
For $f_o = 1$ kHz
$R = 16\ k\Omega$
$C = 0.01\ \mu F$

FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



$$e_o = C\ (1 + a + b)\ (e2 - e1)$$

FIGURE 10 – COMPARATOR WITH HYSTERESIS

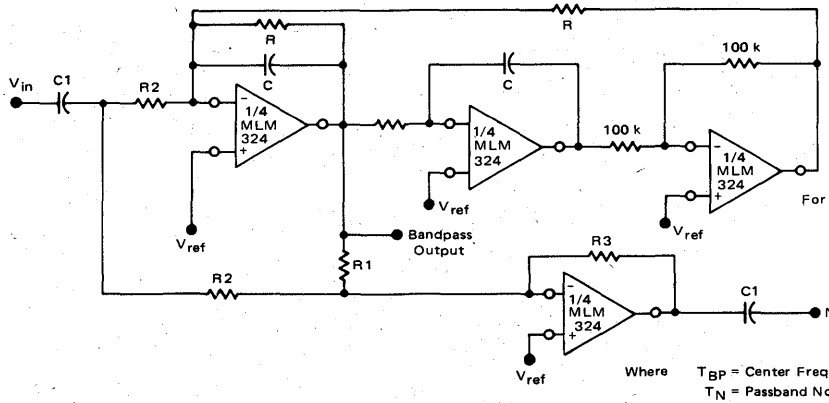


$$V_{inL} = \frac{R1}{R1 + R2} (V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2} (V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$$

FIGURE 11 – BI-QUAD FILTER



$$f_o = \frac{1}{2 \pi RC}$$

$R1 = QR$

$$R2 = \frac{R1}{T_{BP}}$$

$R3 = T_N\ R2$

$C1 = 10\ C$

$$V_{ref} = \frac{1}{2} V_{CC}$$

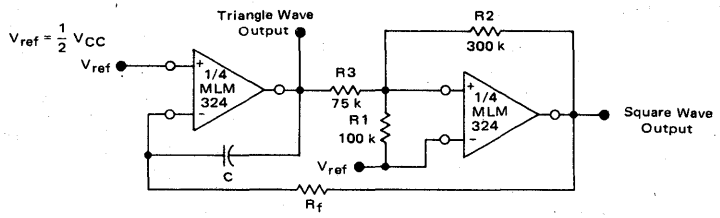
For $f_o = 1$ kHz
$Q = 10$
$T_{BP} = 1$
$T_N = 1$

$R = 160\ k\Omega$
$C = 0.001\ \mu F$
$R1 = 1.6\ M\Omega$
$R2 = 1.6\ M\Omega$
$R3 = 1.6\ M\Omega$

Where T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

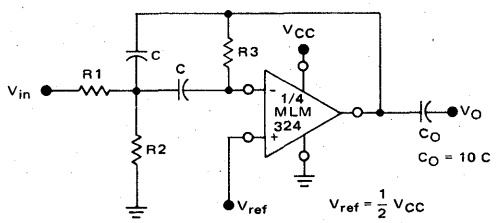
3

FIGURE 12 – FUNCTION GENERATOR



$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \quad \text{if} \quad R3 = \frac{R2\,R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then:

$$R3 = \frac{Q}{\pi\, f_o\, C}$$

$$R1 = \frac{R3}{2\,A(f_o)}$$

$$R2 = \frac{R1\,R5}{4Q^2\,R1 - R5}$$

For less than 10% error from op amp

$$\frac{Q_o\, f_o}{BW} < 0.1$$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MLM158G	LM158H	−55°C to +125°C	Metal Can
MLM158U	—	−55°C to +125°C	Ceramic DIP
MLM258G	—	−25°C to +85°C	Metal Can
MLM258P1	—	−25°C to +85°C	Plastic DIP
MLM258U	—	−25°C to +85°C	Ceramic DIP
MLM358G	LM358H	0°C to +70°C	Metal Can
MLM358P1	LM358N	0°C to +70°C	Plastic DIP
MLM358U	—	0°C to +70°C	Ceramic DIP

MLM158 MLM258 MLM358

Specifications and Applications Information

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

3

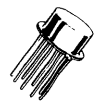
DUAL LOW POWER OPERATIONAL AMPLIFIERS

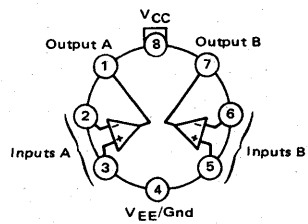
Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, 3) Single Supply or Split Supply operation and 4) pin outs compatible with the popular MC1558 dual operational amplifier. The MLM158 Series is equivalent to one-half of a MLM124.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 Volts or as high as 36 Volts with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 32 Volts
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Single and Split Supply Operations Available
- Similar Performance to the Popular MC1558

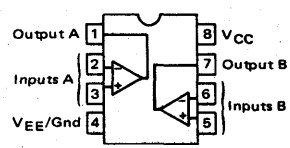
G SUFFIX
METAL PACKAGE
CASE 601





P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MLM258,MLM358 only)

U SUFFIX
CERAMIC PACKAGE
CASE 693



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC} V_{EE}	 32 +16 -16	Vdc
Input Differential Voltage Range (1)	V_{IDR}	±32	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	-0.3 to 32	Vdc
Input Forward Current ($V_I < -0.3$ V)	I_{IF}	50	mA
Junction Temperature Ceramic and Metal Packages Plastic Package	T_J	 175 150	°C
Storage Temperature Range Ceramic and Metal Packages Plastic Package	T_{stg}	 -65 to +150 -55 to +125	°C
Operating Ambient Temperature Range MLM158 MLM258 MLM358	T_A	 -55 to +125 -25 to +85 0 to +70	°C

(1) Split Power Supplies.
(2) For Supply Voltages less than 32 V, the absolute maximum input voltage is equal to the supply voltage.

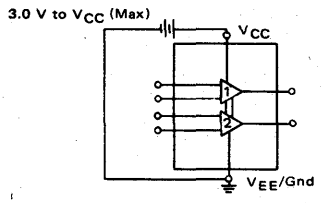
3

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted.)

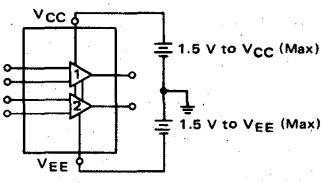
Characteristic	Symbol	MLM158			MLM258,MLM358			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	6.0	mV
$T_A = T_{high}$ to T_{low} (1)		–	–	7.0	–	–	7.5	
Input Offset Current	I_{IO}	–	3.0	30	–	5.0	50	nA
$T_A = T_{high}$ to T_{low}		–	–	100	–	–	150	
Large Signal Open-Loop Voltage Gain	A_{VOL}							V/mV
V_O = ±10 V, R_L = 2.0 kΩ, V_{CC} = 15 V,		50	100	–	25	100	–	
$T_A = T_{high}$ to T_{low}		25	–	–	15	–	–	
Input Bias Current	I_{IB}	–	-45	-150	–	-45	-250	nA
$T_A = T_{high}$ to T_{low}		–	–	-300	–	–	-500	
Common-Mode Rejection Ratio	CMRR	70	85	–	65	70	–	dB
$R_S \leq 10$ kΩ								
Power Supply Current (V_O = 0)	I_{CC}	–	0.5	1.2	–	0.5	1.2	mA
$R_L = \infty$, $T_A = T_{high}$ to T_{low}								
Power Supply Rejection Ratio	PSRR	65	100	–	65	70	–	dB
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	–	10	–	–	10	–	pA/°C
$T_A = T_{high}$ to T_{low}								
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	7.0	–	–	7.0	–	μV/°C
$T_A = T_{high}$ to T_{low}								
Input Common-Mode Voltage Range	V_{ICR}							V
V_{CC} = 30 V		0	–	28.5	0	–	28.5	
V_{CC} = 30 V, $T_A = T_{high}$ to T_{low}		0	–	28	0	–	28	
Amplifier-to-Amplifier Coupling	–	–	-120	–	–	-120	–	dB
1.0 kHz ≤ f ≤ 20 kHz, Input Referenced								
Differential Input Voltage Range	V_{IDR}	–	–	V_{CC}	–	–	V_{CC}	V
Output Voltage Range	V_{OR}	0	3.5	–	0	3.5	–	V
R_L = 2 kΩ								
Output Voltage – High Limit	V_{OH}							V
V_{CC} = 30 V, R_L = 2 kΩ, $T_A = T_{high}$ to T_{low}		26	–	–	26	–	–	
V_{CC} = 30 V, R_L = 10 kΩ, $T_A = T_{high}$ to T_{low}		27	28	–	27	28	–	
Output Voltage – Low Limit	V_{OL}	–	5.0	20	–	5.0	20	mV
V_{CC} = 5.0 V, R_L = 10 kΩ, $T_A = T_{high}$ to T_{low}								
Output Source Current	I_{O+}							mA
V_{ID} = +1.0 V, V_{CC} = 15 V		20	40	–	20	40	–	
V_{ID} = +1.0 V, V_{CC} = 15 V, $T_A = T_{high}$ to T_{low}		10	20	–	10	20	–	
Output Sink Current	I_{O-}							mA
V_{ID} = -1.0 V, V_{CC} = 15 V		10	20	–	10	20	–	
V_{ID} = -1.0 V, V_{CC} = 15 V, $T_A = T_{high}$ to T_{low}		5.0	8.0	–	5.0	8.0	–	
V_{ID} = -1.0 V, V_O = 200 mV		0.012	0.05	–	0.012	0.05	–	

(1) T_{high} = 125°C for MLM158, 70°C for MLM358, 85°C for MLM258.
T_{low} = -55°C for MLM158, 0°C for MLM358, -25°C for MLM258.

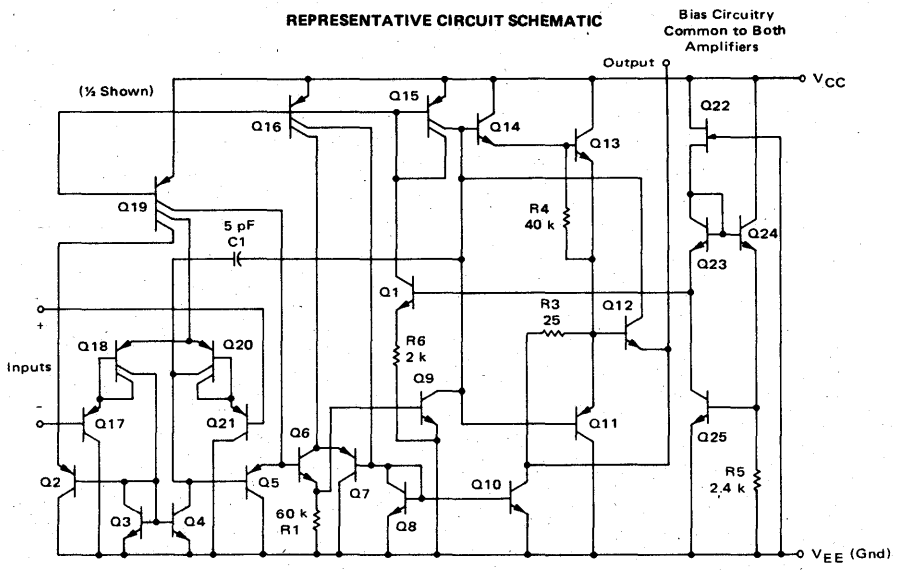
SINGLE SUPPLY



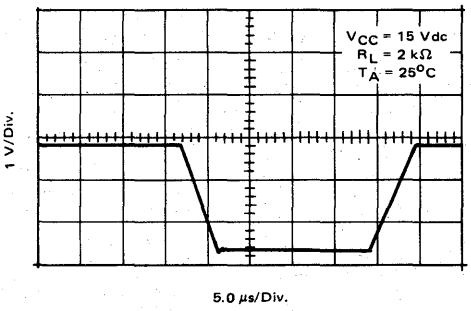
SPLIT SUPPLIES



REPRESENTATIVE CIRCUIT SCHEMATIC



LARGE SIGNAL VOLTAGE FOLLOWER RESPONSE



CIRCUIT DESCRIPTION

The MLM158 Series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

3

TYPICAL PERFORMANCE CURVES

FIGURE 1 – INPUT VOLTAGE RANGE

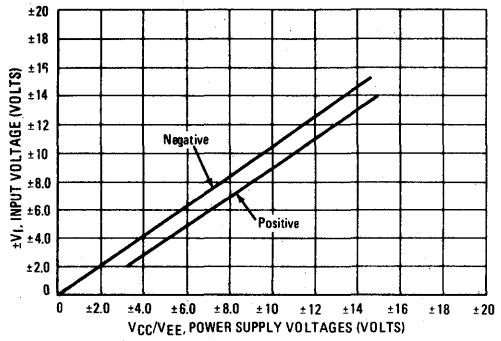


FIGURE 2 – OPEN LOOP FREQUENCY

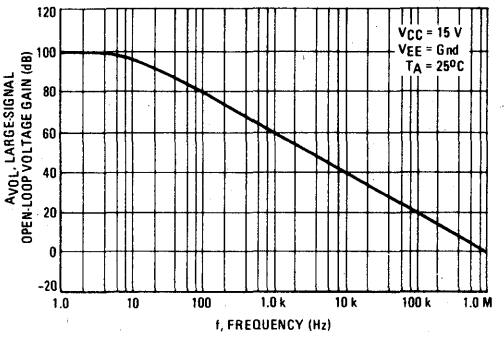


FIGURE 3 – LARGE-SIGNAL FREQUENCY RESPONSE

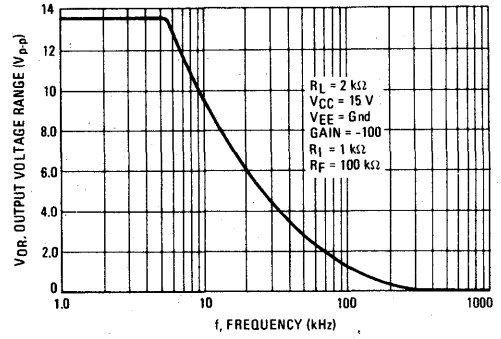


FIGURE 4 – SMALL-SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE
(Non-Inverting)

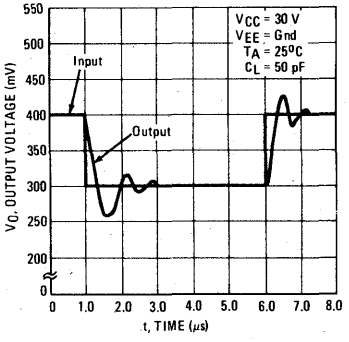


FIGURE 5 – POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

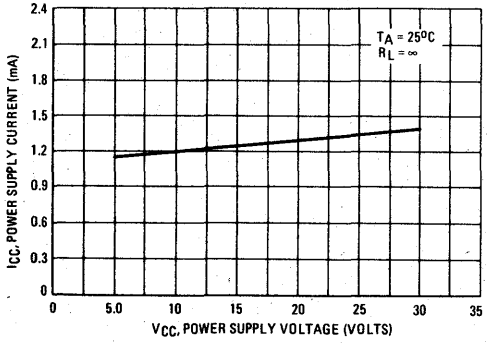
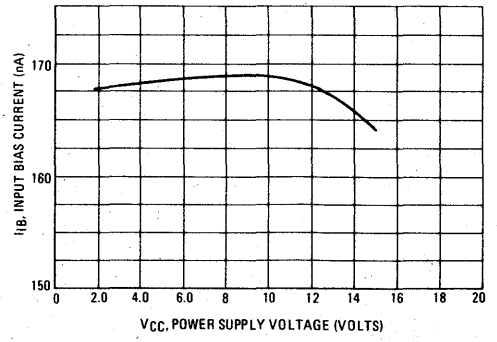
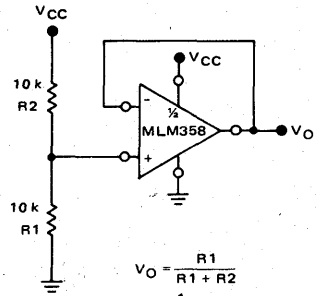


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

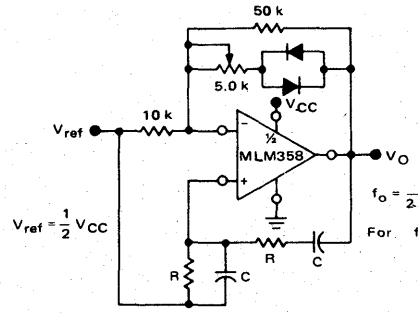
FIGURE 7 – VOLTAGE REFERENCE



$$V_O = \frac{R1}{R1 + R2}$$

$$V_O = \frac{1}{2} V_{CC}$$

FIGURE 8 – WEIN BRIDGE OSCILLATOR

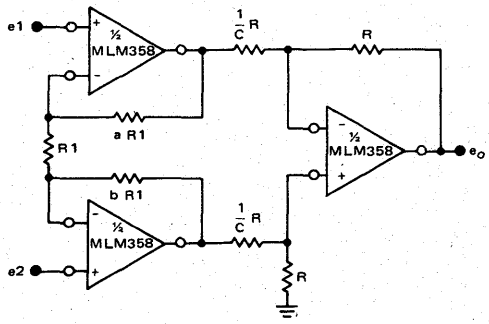


$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_o = \frac{1}{2\pi RC}$$

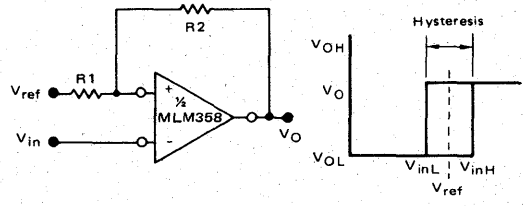
For f_o = 1 kHz
R = 16 kΩ
C = 0.01 μF

FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



$$e_o = C\,(1 + a + b)\,(e2 - e1)$$

FIGURE 10 – COMPARATOR WITH HYSTERESIS

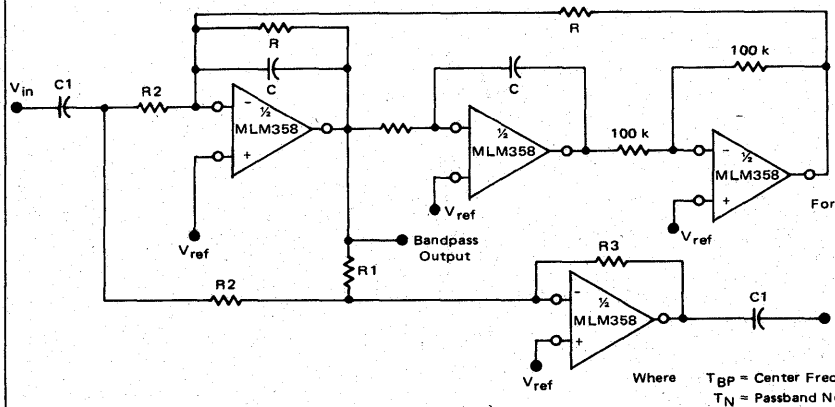


$$V_{inL} = \frac{R1}{R1 + R2}\,(V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2}\,(V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2}\,(V_{OH} - V_{OL})$$

FIGURE 11 – BI-QUAD FILTER



$$f_o = \frac{1}{2\pi RC}$$

$R1 = QR$

$$R2 = \frac{R1}{T_{BP}}$$

$R3 = T_N\,R2$

$C1 = 10\,C$

$$V_{ref} = \frac{1}{2} V_{CC}$$

For f_o = 1 kHz
Q = 10
T_{BP} = 1
T_N = 1

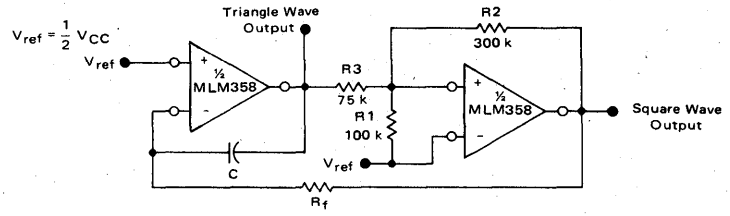
R = 160 kΩ
C = 0.001 μF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

Where T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

3

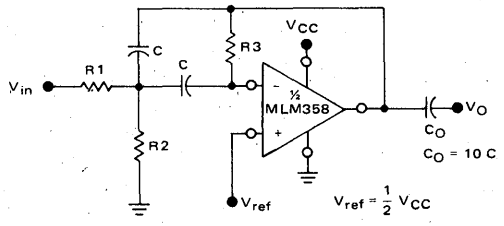
APPLICATIONS INFORMATION (continued)

FIGURE 12 – FUNCTION GENERATOR



$$f = \frac{R1 + R_C}{4 C R_f R1} \quad \text{if} \quad R3 = \frac{R2\ R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then:

$$R3 = \frac{Q}{\pi f_o C}$$

$$R1 = \frac{R3}{2 A(f_o)}$$

$$R2 = \frac{R1\ R3}{4Q^2\ R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_o f_o}{BW} < 0.1$$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section
T_A = Maximum Desired Operating Ambient Temperature
$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MLM2902P	LM2902N	−40°C to +85°C	Plastic DIP

MLM2902

Specifications and Applications Information

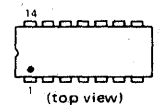
QUAD LOW POWER OPERATIONAL AMPLIFIER

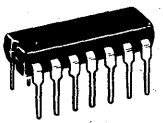
The MLM2902 is a low-cost, quad operational amplifier with true differential inputs. This has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 Volts or as high as 26 Volts with quiescent currents about one fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 to 26 Volts
- Low Input Bias Currents: 500 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply

QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT





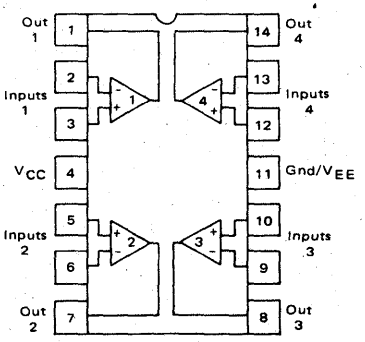
P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages			Vdc
Single Supply	V_{CC}	32	
Split Supplies	V_{CC}	+13	
	V_{EE}	-13	
Input Differential Voltage Range (1)	V_{IDR}	±26	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	-0.3 to 26	Vdc
Input Forward Current ($V_I < -0.3$ V)	I_{IF}	50	mA
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C

(1) Split Power Supplies.
(2) For Supply Voltages less than 32 V, the absolute maximum input voltage is equal to the supply voltage.

PIN CONNECTIONS



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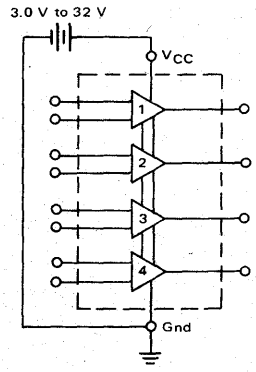
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted.)

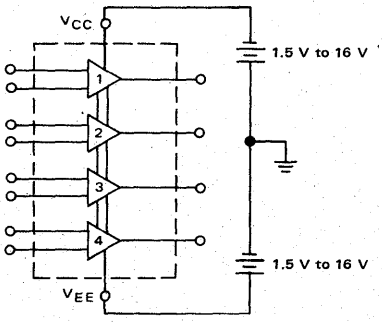
Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	–	2.0	10	mV
Input Offset Current	I_{IO}	–	5.0	50	nA
Large Signal Open-Loop Voltage Gain V_O = ±10 V, R_L = 2.0 kΩ	A_{VOL}	–	100	–	V/mV
Input Bias Current	I_{IB}	–	-45	-500	nA
Common-Mode Rejection Ratio	CMRR	–	85	–	dB
Power Supply Current (V_o = 0) R_L = ∞	I_{CC}	–	0.8	2.0	mA
Power Supply Rejection Ratio	PSRR	–	100	–	dB
Input Common-Mode Voltage Range	V_{ICR}	0	–	3.5	V
Amplifier-to-Amplifier Coupling 1.0 kHz ≤ f ≤ 20 kHz, Input Referenced	–	–	-120	–	dB
Output Voltage Range R_L = 2 kΩ	V_{OR}	0	3.5	–	V
Output Source Current V_{ID} = +1.0 V, V_{CC} = 15 V	I_{O+}	20	40	–	mA
Output Sink Current V_{ID} = -1.0 V	I_{O-}	8.0	20	–	mA

(1) T_{high} = +85°C
T_{low} = -40°C

SINGLE SUPPLY



SPLIT SUPPLIES



TYPICAL PERFORMANCE CURVES

FIGURE 1 – INPUT VOLTAGE RANGE

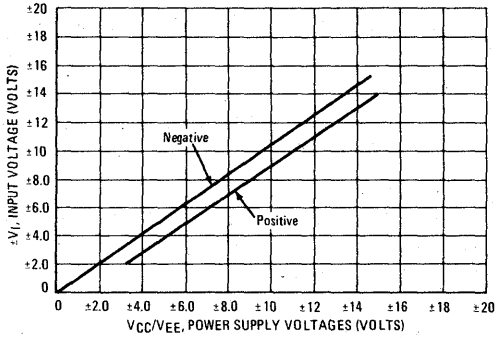


FIGURE 2 – OPEN LOOP FREQUENCY

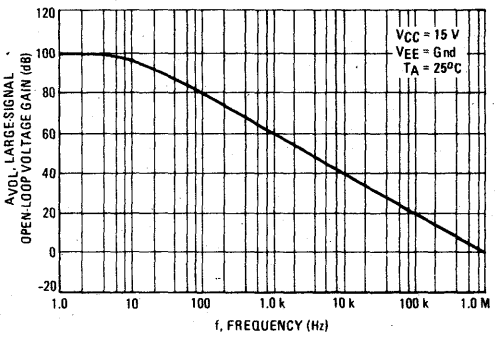


FIGURE 3 – LARGE-SIGNAL FREQUENCY RESPONSE

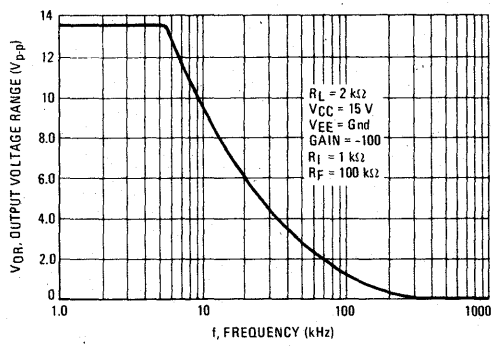


FIGURE 4 – SMALL-SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE (Non-Inverting)

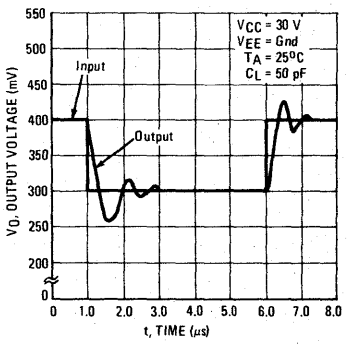


FIGURE 5 – POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

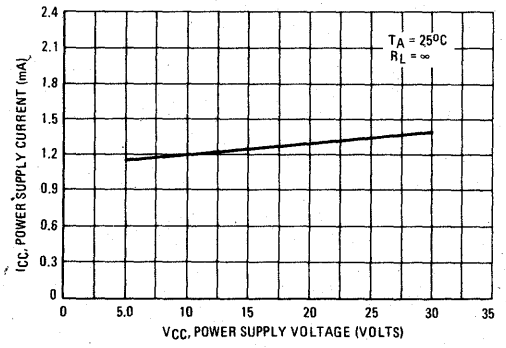
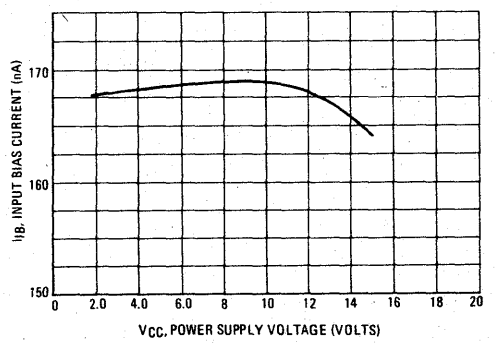


FIGURE 6 – INPUT BIAS CURRENT versus SUPPLY VOLTAGE



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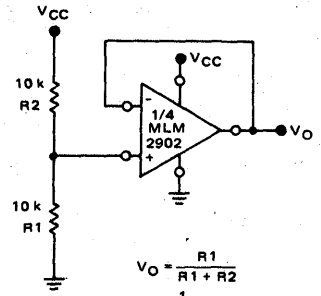
APPLICATIONS INFORMATION

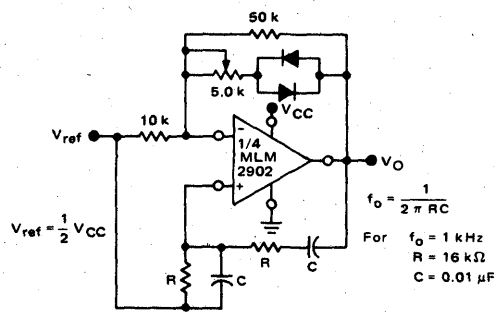
FIGURE 7 – VOLTAGE REFERENCE



$$V_O = \frac{R1}{R1 + R2}$$

$$V_O = \frac{1}{2} V_{CC}$$

FIGURE 8 – WEIN BRIDGE OSCILLATOR

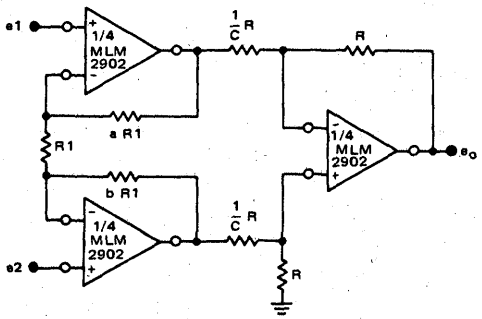


$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_o = \frac{1}{2 \pi RC}$$

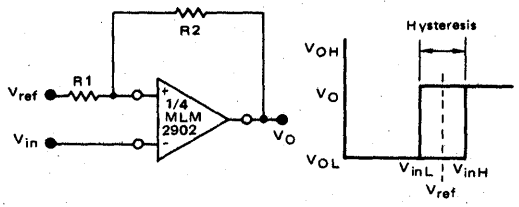
For f_o = 1 kHz
R = 16 kΩ
C = 0.01 μF

FIGURE 9 – HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



$$e_o = C\,(1 + a + b)\,(e2 - e1)$$

FIGURE 10 – COMPARATOR WITH HYSTERESIS

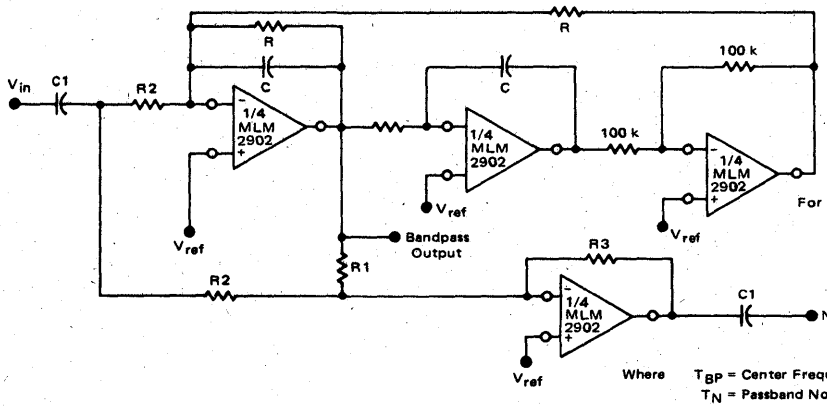


$$V_{inL} = \frac{R1}{R1 + R2}\,(V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2}\,(V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2}\,(V_{OH} - V_{OL})$$

FIGURE 11 – BI-QUAD FILTER



$$f_o = \frac{1}{2 \pi RC}$$

R1 = QR

$$R2 = \frac{R1}{T_{BP}}$$

R3 = T_N R2

C1 = 10 C

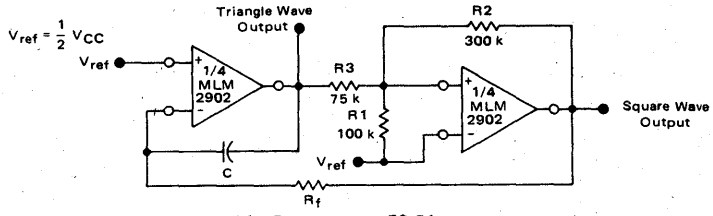
$$V_{ref} = \frac{1}{2} V_{CC}$$

For f_o = 1 kHz
Q = 10
T_{BP} = 1
T_N = 1

R = 160 kΩ
C = 0.001 μF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

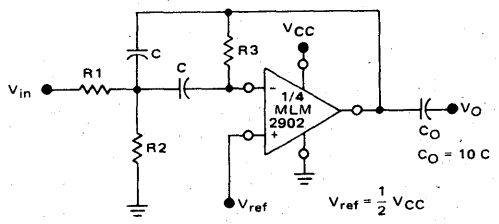
Where T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

FIGURE 12 – FUNCTION GENERATOR



$$f = \frac{R1 + R_C}{4\,C R_f\,R1} \quad \text{if} \quad R3 = \frac{R2\,R1}{R2 + R1}$$

FIGURE 13 – MULTIPLE FEEDBACK BANDPASS FILTER



Given f_o = Center Frequency
$A(f_o)$ = Gain at Center Frequency

Choose Value f_o, C
Then:

$$R3 = \frac{Q}{\pi\, f_o\, C}$$

$$R1 = \frac{R3}{2\,A(f_o)}$$

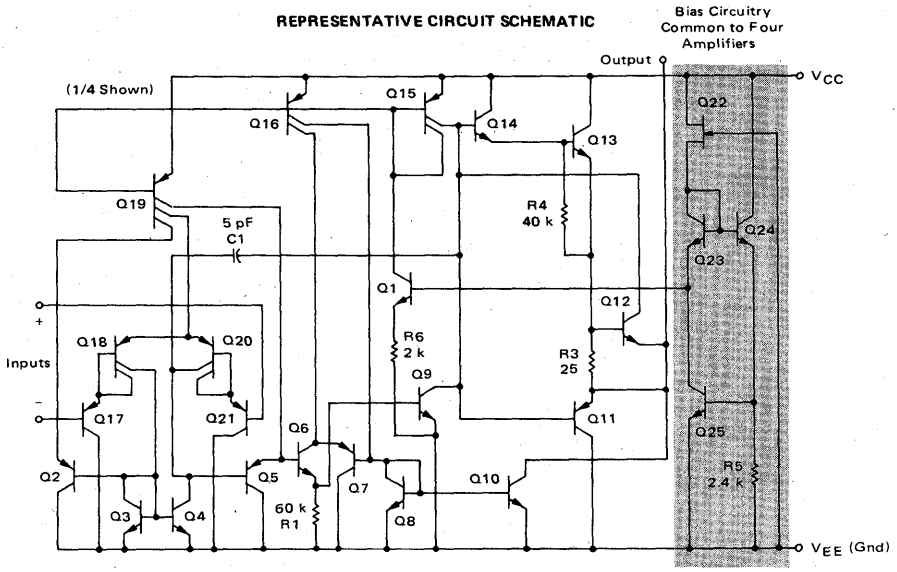
$$R2 = \frac{R1\,R5}{4Q^2\,R1 - R5}$$

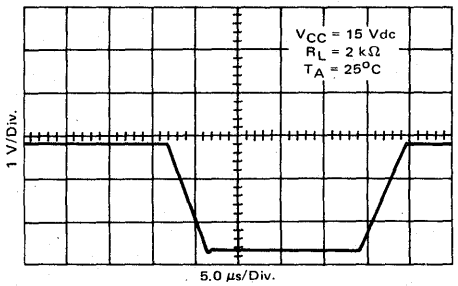
For less than 10% error from op amp

$$\frac{Q_o\, f_o}{BW} < 0.1$$ Where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

REPRESENTATIVE CIRCUIT SCHEMATIC





CIRCUIT DESCRIPTION

The MLM2902 is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

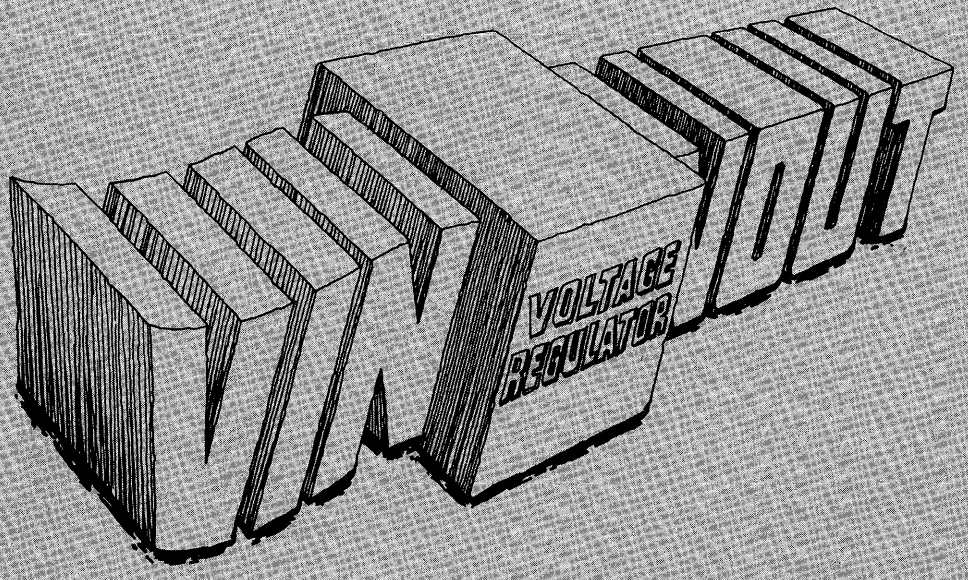
Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

Voltage Regulators / Chapter 4



VOLTAGE REGULATORS

Temperature Range				
0 to 70°C	-55 to 125°C	Other		Page
LM317	LM117	—	Three-Terminal Adjustable Positive Regulator	4-6
LM323	LM123	—	Positive Voltage Regulator	4-7
MC1403,A	MC1503,A	—	Precision Low-Voltage Reference	4-9
MC1460,61	MC1560,61	—	Positive Voltage Regulator	4-11
MC1463	MC1563	—	Adjustable Negative Regulator	4-12
MC1466	MC1566	—	Precision Floating Regulator	4-28
MC1468	MC1568	—	Dual ±15-Volt Tracking Regulator	4-38
MC1469	MC1569	—	Adjustable Positive Regulator	4-44
MC1723C	MC1723	—	Adjustable Positive or Negative Regulator	4-63
MC3420	MC3520	—	Switchmode Regulator Control Circuit	4-69
MC3422	—	—	Current Limiter	4-74
—	—	MC7700C	Series of Positive Regulators (750 mA)	4-76
—	—	MC7800C	Series of Positive Regulators (1.5 A)	4-84
—	—	MC78L00C,AC	Series of Positive Regulators (100 mA)	4-92
—	—	MC78M00C	Series of Positive Regulators (500 mA)	4-99
—	—	MC7900C	Series of Negative Regulators (1.5 A)	4-107
—	—	MC79L00C,AC	Series of Negative Regulators (100 mA)	4-116
MLM304	MLM104	MLM204	Adjustable Negative Regulator	4-122
MLM305	MLM105	MLM205	Adjustable Positive Regulator	4-124
MLM309	MLM109	MLM209	Positive Voltage Regulator	4-126

Fixed Output Voltage Regulators

Low cost, monolithic circuits for positive and/or negative regulation at currents from 100 mA to 3 A. These dedicated circuits require no external add-on component, although an input capacitor should be used if regulator is located an appreciable distance from the power supply filter, and an output capacitor could improve transient response. They are ideal for on-card regulation of sub-systems, affording possible economic advantages and performance improvement in applications where total system regulation is not required.

*Most devices are available in metal and plastic packages. All employ internal current limiting, thermal shutdown and safe-area compensation – making them essentially blow-out proof. All are designed to operate over a 0°C to 150°C junction temperature range, except *T_J = -55°C to +150°C.*

FIXED VOLTAGE, 3-TERMINAL REGULATORS FOR POSITIVE OR NEGATIVE POLARITY POWER SUPPLIES.

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Type Positive Output	Device Type Negative Output	V_{in} Min/Max	Reg_{line} mV	Reg_{load} mV	$\Delta V_O/\Delta T$ mV/°C	Case
2	± 0.1	1500	–	MC7902C	5.5/35	40	120	1.0	11, 313
3	± 0.15	100	–	MC79L03AC	4.7/30	60	72	0.6	
3	± 0.3	100	–	MC79L03C	4.7/30	80	72	0.6	29,79
5	±0.5	100	MC78L05C	MC79L05C	6.7/30	200	60	0.1	29, 79
	±0.25		MC75L05AC	MC79L05AC		150			
		500	MC78M05C	–	7/35	100	100	1.0	79, 313
		750	MC7705C	–					79, 313
		1500	MC7805C	MC7905C					11, 313
	± 0.4		LM109	–					11, 79
			LM209	–					
	± 0.25		LM309	–		50			11
	± 0.3	3000	**LM123*	–	7.5/20	25			
	± 0.2		**LM323	–					
5.2	± 0.26	1500	–	MC7905.2C	7.2/35	105	105	1.0	11, 313
6	± 0.3	500	MC78M06C	–	8/35	100	120	1.0	79, 313
		750	MC7706C	–		120			79, 313
		1500	MC7806C	MC7906C					11, 313
8	± 0.8	100	MC78L08C	–	9.7/30	200	80	0.16	29, 79
			MC78L08AC	–		175			
	± 0.4	500	MC78M08C	–	10/35	100	160	1.0	79, 313
		750	MC7708C	–		160			79, 313
		1500	MC7808C	MC7908C					11, 313
12	± 1.2	100	MC78L12C	MC79L12C	13.7/35	250	100	0.24	29, 79
	± 0.6		MC78L12AC	MC79L12AC					
		500	MC78M12C	–	14/35	100	240	1.0	79,313
		750	MC7712C	–		240			79, 313
		1500	MC7812C	MC7912C					11, 313
15	± 1.5	100	MC78L15C	MC79L15C	16.7/35	300	150	0.3	29, 79
	± 0.75		MC78L15AC	MC79L15A					
		500	MC78M15C	–	17/35	100	300	1.0	79, 313
		750	MC7715C	–		300			79, 313
		1500	MC7815C	MC7915C					11, 313
18	± 1.8	100	MC78L18C	MC79L18C	19.7/35	325	170	0.36	29, 79
	± 0.9		MC78L18AC	MC79L18AC					
		500	MC78M18C	–	20/35	100	360	1.0	79, 313
		750	MC7718C	–		360			79, 313
		1500	MC7818C	MC7918C					11, 313
20	±1.0	500	MC78M20C	–	22/40	10	400	1.0	79, 313
		750	MC7720C	–		400			
24	± 2.4	100	MC78L24C	MC79L24C	25.7/40	350	,200	0.48	29, 79
	± 1.2		MC78L24AC	MC79L24AC		300			29, 79
		500	MC78M24C	–	26/40	100	480	1.2	79, 313
		750	MC7724C	–		480		1.0	79, 313
		1500	MC7824C	MC7924C					11, 313

*T_J = -55 to +159°C
**To be introduced
†Output Voltage Tolerance for Worst Case

Variable Output Voltage Regulators

The regulators in the following tables can be tailored for any specific output voltage within the indicated ranges through the use of external resistors. The indicated output current is available directly from the device. Increased output current can usually be obtained through the use of external current – boosting circuits. All have internal provisions for current limiting, or are internally protected against excessive thermal or SOA overloads.

POSITIVE OUTPUT REGULATORS

I_O mA Max	Device Type	SUFFIX	V_{out} Volts Min	V_{out} Volts Max	V_{in} Volts Min	V_{in} Volts Max	$V_{in} - V_{out}$ Differential Volts Max	P_D Watts Max T_A = 25°C	P_D Watts Max T_C = 25°C	Regulation % V_{out} @ T_A = 25°C Typ Line	Regulation % V_{out} @ T_A = 25°C Typ Load	TC V_{out} Typ % / °C	T_J = °C Max	Case
20	MLM305	G	4.5	40	8.5	50	3.0	0.4	1.3	0.06	0.1	0.007	85	601
	MLM205							0.68	1.6				100	
	MLM105			30					2.7				150	
150	MC1723	CP	2.0	37	9.5	40	3.0	0.65	–	0.1	0.3	0.003	150	646
		CG						0.8	2.1	0.1		0.003		603C
		G								0.2		0.002		
		CL						1.0	–	0.1		0.003	175	632
		L							–	0.2		0.002		
250	MC1469	G	2.5	32	9	35	3.0	0.68	1.8	0.03	0.13	0.002	150	603
	MC1569			37	8.5	40	2.7			0.015				
600	MC1469	R	2.5	32	9.0	35	3.0	3.0	14.0	0.03	0.05	0.002	150	614
	MC1569			37	8.5	40	2.7			0.015				
1500	LM317*	T	1.2	37	5.0	40	3.0	Internally Limited		0.07	1.5	0.5	125	313
	LM317*	K												11
	LM117*									0.05	1.0		150	

*To be introduced

NEGATIVE OUTPUT REGULATORS

20	LM304	G	0.035	30	8.0	40	2.0	0.4	1.3	0.1	0.05	0.007	80	603
	LM204		0.015	40		50		0.68	1.6				100	
	LM104								2.7				150	
250	MC1463	G	3.8	32	9.0	35	3.0	0.68	1.8	0.03	0.05	0.002	150	603
	MC1563		3.6	33	8.5	40	2.7			0.015	0.13			
600	MC1463	R	3.8	34	9.0	35	3.0	2.4	9.0	0.03	0.05	0.002	175	614
	MC1463		3.6	37	8.5	40	2.7			0.015				

Switching Regulator

Used as the control circuit in PWM, push-pull, bridge and series type switchmode supplies. The device includes the reference, oscillator, pulse-width modulator, phase splitter and output sections. Frequency and duty cycle are independently adjustable.

I_O ± mA Max	V_{CC} Volts Min	V_{CC} Volts Max	f_o kHz Min	f_o kHz Max	Device Number	SUFFIX	T_A °C	Case
40	10	30	2.0	100	MC3420	P	0 to +70	648
						L		620
					MC3520	L	-55 to +125	620

Special Regulators

FLOATING VOLTAGE AND CURRENT REGULATORS. *Designed for laboratory type power supplies, these unique regulators can deliver hundreds of volts – limited only by the breakdown voltage of associated, external, series-pass transistors.*

V_{out} Volts		I_O mA	Device	SUFFIX	V_{aux} Volts		P_D Watts	$\Delta V_{ref}/V_{ref}$ %		$\Delta I_L/I_L$ %	$TC_{V_{out}}$ %/°C	Case
Min	Max	Max	Type		Min	Max	Max	Line	Load	Max	Typ	
0	*	*	MC1466	L	21	30	0.75	0.015	0.015	0.2	0.01	632
			MC1566	L	20	35		0.004	0.004	0.1	0.006	

*Dependent on characteristics of external series-pass elements.

4

DUAL ±15 V TRACKING REGULATORS. *Dual polarity regulator designed to provide balanced positive and negative output voltages. Internally, the device is set for ±15 V, but an external adjustment can change both outputs simultaneously, from 8.0 V to 20 V.*

V_{out} Volts		I_O mA	V_{in} Volts		Device	SUFFIX	P_D Watts	Regline	Regload	TC %/°C (T_{low} to T_{high})	T_A	Case
Min	Max	Max	Min	Max	Type		Max	mV	mV	Typ	°C	
14.8	15;2	±100	17	30	MC1468	G	0.8	10	10	3.0	0 to +75	603
						L	1.0					632
						R	2.4					614
					MC1568	G	0.8				-55 to +125	603
						L	1.0					632
						R	2.4					614

LOW TEMPERATURE DRIFT, LOW VOLTAGE REFERENCE

V_{out} Volts Typ	I_O mA Max	$\Delta V_{out}/\Delta T$ ppm/°C Typ	Device Type	SUFFIX	Reg_{line} (7.0 V ≤ V_I ≤ 30 V) Max	Reg_{line} (4.5 V ≤ V_{in} ≤ 7.0 V Max	Reg_{load} (1.0 mA < I_O < 11mA) mA Max	T_A °C	Case
2.5 ± 25 mV	10	10	MC1403	PI	6.0	3.0	10	0 to +70	626
			MC1403A	U					693
			MC1503	U				-55 to +125	693
			MC1503A						693

LM117
LM317

Advance Information

3-TERMINAL ADJUSTABLE VOLTAGE REGULATOR

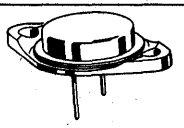
SILICON MONOLITHIC INTEGRATED CIRCUIT

3-TERMINAL ADJUSTABLE OUTPUT VOLTAGE REGULATOR

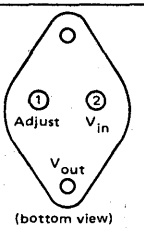
The LM117 and LM317 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. These voltage regulators are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM117/LM317 serve a wide variety of applications including local, on card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117/317 can be used as a precision current regulator.

- Output Current in Excess of 1.5 Ampere
- Output Adjustable Down to 1.2 V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-area Compensation
- Standard TO-220 3-lead Transistor Package



K SUFFIX
METAL PACKAGE
CASE 11
(TO-3 Type)

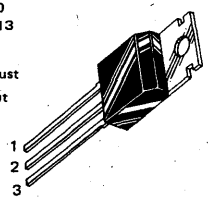


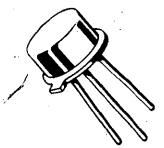
(bottom view)

Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

T SUFFIX
PLASTIC PACKAGE
TO-220
CASE 313

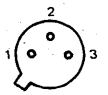
Pin 1 Adjust
Pin 2 V_{out}
Pin 3 V_{in}





Pin 1 V_{in}
Pin 2 Adjust
Pin 3 V_{out}

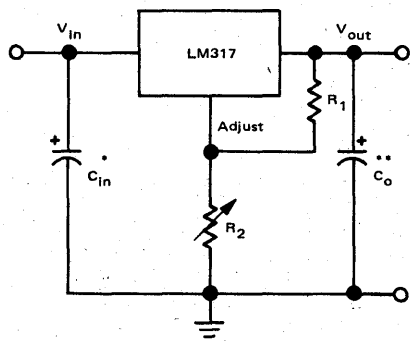
(Case is output)



(Bottom View)

H SUFFIX
METAL PACKAGE
CASE 79
(TO-39)

STANDARD APPLICATION



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.
** = C_o is not needed for stability, however it does improve transient response.

ORDERING INFORMATION

Device	Temperature Range	Package
LM117H	$-55^{\circ}C$ to $+125^{\circ}C$	Metal Can
LM117K	$-55^{\circ}C$ to $+125^{\circ}C$	Metal Power
LM317H	$0^{\circ}C$ to $+70^{\circ}C$	Metal Can
LM317K	$0^{\circ}C$ to $+70^{\circ}C$	Metal Power
LM317T	$0^{\circ}C$ to $+70^{\circ}C$	Plastic Power

This is advance information and specifications are subject to change without notice.

LM123
LM323

Product Preview

3 AMPERE - 5 VOLT POSITIVE VOLTAGE REGULATOR

The LM123/LM323 is a three-terminal positive regulator with a fixed 5 Volt output and a load driving capability of 3 Amperes.

These regulators are supplied in a hermetic TO-3 package which possesses high reliability and low thermal resistance. This package can provide up to 30 Watts power dissipation.

The LM123/LM323 employ internal current limiting, thermal shutdown and safe area compensation which make them essentially blow-out proof.

The LM123 has a guaranteed operation over the junction temperature range −55°C to +150°C while the LM323 is specified from 0°C to +125°C junction temperature.

- Delivers Up to 3 Amperes Output Current
- No External Component Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- 30 Watts Power Dissipation

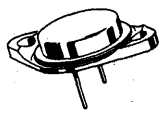
MAXIMUM RATINGS

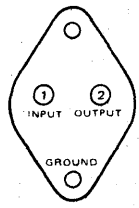
Rating	Symbol	Value	Unit
Input Voltage	V_{in}	20	Vdc
Power Dissipation	P_D	Internally Limited	
Thermal Resistance, Junction to Air	θ_{JA}	35	°C/W
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature Range LM123 LM323	T_J	 −55 to +150 0 to +125	°C

This is advance information and specifications are subject to change without notice.

3 AMPERE - 5 VOLT VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



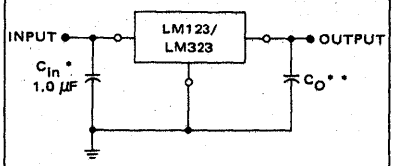


K SUFFIX
METAL PACKAGE
CASE 11
(TO-3 TYPE)

(bottom view)

Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_{in} (solid tantalum) is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response. If needed, its value should be greater than 0.1 μF.

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
LM123K	−55°C to +125°C	METAL POWER
LM323K	0°C to +70°C	METAL POWER

ELECTRICAL CHARACTERISTICS ($T_J = T_{low}$ to T_{high} [see Note 1] unless otherwise specified.)

Characteristic	Symbol	LM123 Min	LM123 Typ	LM123 Max	LM323 Min	LM323 Typ	LM323 Max	Unit
Output Voltage (V_{in} = 7.5 V, I_{out} = 0, T_J = 25°C)	V_O	4.7	5.0	5.3	4.8	5.0	5.2	V
Output Voltage (7.5 V ≤ V_{in} ≤ 15 V, 0 ≤ I_{out} ≤ 3.0 A, P ≤ 30 W)	V_O	4.6	–	5.4	4.75	–	5.25	V
Line Regulation (3) (7.5 V ≤ V_{in} ≤ 15 V, T_J = 25°C)	Reg_{in}	–	5.0	25	–	5.0	25	mV
Load Regulaton (3) (V_{in} = 7.5 V, 0 ≤ I_{out} ≤ 3.0 A, T_J = 25°C)	Reg_{load}	–	25	100	–	25	100	mV
Quiescent Current (7.5 V ≤ V_{in} ≤ 15 V, 0 ≤ I_{out} ≤ 3.0 A)	I_B	–	12	20	–	12	20	mA
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = 25°C)	V_N	–	40	–	–	40	–	μV_{rms}
Short Circuit Current Limit (V_{in} = 15 V, T_J = 25°C)	I_{SC}	–	3.0	4.5	–	3.0	4.5	mA
(V_{in} = 7.5 V, T_J = 25°C)		–	4.0	5.0	–	4.0	5.0	
Long Term Stability	S	–	–	35	–	–	35	mV
Thermal Resistance Junction to Case (2)	$R_{\theta JC}$	–	2.0	–	–	2.0	–	°C/W

Note 1. T_{low} = −55°C for LM123, = 0°C for LM323; T_{high} = +150°C for LM123, = +125°C for LM323

Although power dissipation is internally limited, specifications apply only for P ≤ 30 W.

Note 2. Without a heat sink, the thermal resistance of the TO-3 package is about 35° C/W. With a heat sink, the effective thermal resistance can only approach the specified values of 2.0° C/W, depending on the efficiency of the heat sink.

Note 3. Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width ≤ 1.0 ms and a duty cycle ≤ 5%.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}} \geq V_I I_S - V_O I_O$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}$(Typ) = Typical Thermal Resistance Junction to Ambient

I_S = Total Supply Current

MC1403,A
MC1503,A

Product Preview

LOW-VOLTAGE REFERENCE

A precision band-gap voltage reference designed for critical instrumentation and D/A converter applications. This unit is designed to work with Motorola MC1506, MC1508, and MC3510 D/A converters as well as numerous A/D systems. Low temperature drift is a prime design consideration.

- Nominal Output Voltage = 2.5 V ± 25 mV
- Input Voltage Range = 4.5 V to 35 V
- Quiescent Current = 1.2 mA typ
- Output Current = 10 mA
- Temperature Coefficient = 10 ppm/°C typ
- Temperature Sensing Diode Available
- Guaranteed Temperature Drift Specification
- Equivalent to AD580

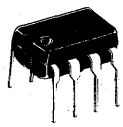
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_I	40	V
Storage Temperature	T_{stg}	-65 to 150	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	 °C °C
Operating Ambient Temperature Range MC1503, A MC1403, A	T_A	 -55 to +125 0 to +70	 °C °C

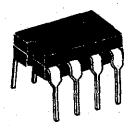
This is advance information and specifications are subject to change without notice.

PRECISION LOW-VOLTAGE REFERENCE

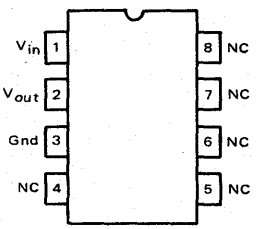
LASER TRIMMED
SILICON MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1403 only)



U SUFFIX
CERAMIC PACKAGE
CASE 693



ORDERING INFORMATION

Device	Temperature Range	Package
MC1503U	-55 to +125°C	Ceramic DIP
MC1503AU	-55 to +125°C	Ceramic DIP
MC1403U	0 to +70°C	Plastic DIP
MC1403AU	0 to +70°C	Plastic DIP
MC1403P1	0 to +70°C	Plastic DIP
MC1403AP1	0 to +70°C	Plastic DIP

4

ELECTRICAL CHARACTERISTICS (V_I = 15 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0 mA)	V_O	2.475	2.50	2.525	V
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				ppm/°C
MC1503		–	–	55	
MC1503A		–	–	25	
MC1403		–	10	40	
MC1403A		–	10	25	
Output Voltage Change (over specified temperature range)	ΔV_O				mV
MC1503		–	–	25	
MC1503A		–	–	11	
MC1403		–	–	7.0	
MC1403A		–	–	4.4	
Line Regulation	Reg_{in}				mV
(15 V ≤ V_I ≤ 40 V)		–	1.2	4.5	
(4.5 V ≤ V_I ≤ 15 V)		–	0.6	3.0	
Load Regulation (1.0 mA < I_O < 11 mA)	Reg_{load}	–	–	10	mV
Quiescent Current (I_O = 0 mA)	I_I	–	1.2	1.5	mA

MC1460, MC1461
MC1560, MC1561

POSITIVE VOLTAGE REGULATORS

These devices are not recommended for new design, but Motorola will continue to supply these devices for existing applications.

For a complete data sheet, mail your request to Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, Arizona 85036.

MC1463
MC1563

Specifications and Applications Information

NEGATIVE VOLTAGE REGULATOR

The MC1563/MC1463 is a "three terminal" negative regulator designed to deliver continuous load current up to 500 mAdc and provide a maximum negative input voltage of −40 Vdc. Output current capability can be increased to greater than 10 Adc through use of one or more external transistors.

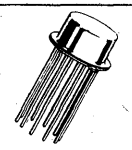
Specifications and performance of the MC1563/MC1463 Negative Voltage Regulator are nearly identical to the MC1569/MC1469 Positive Voltage Regulator. For systems requiring both a positive and negative power supply, these devices are excellent for use as complementary regulators and offer the advantage of operating with a common input ground.

The MC1563R/MC1463R case can be mounted directly to a grounded heat sink which eliminates the need for an insulator.

- Case is at Ground Potential (R package)
- Electronic "Shutdown" and Short-Circuit Protection
- Low Output Impedance — 20 Milliohms typical
- High Power Capability — 9.0 Watts
- Excellent Temperature Stability — $\Delta V_O/\Delta T = \pm 0.002\%/^oC$ typical
- High Ripple Rejection — 0.002% typical
- 500 mA Current Capability

NEGATIVE-POWER-SUPPLY VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



G SUFFIX
METAL PACKAGE
CASE 603

R SUFFIX
METAL PACKAGE
CASE 614

FIGURE 1 — TYPICAL CIRCUIT CONNECTION
($|-3.5| \leq V_O \leq |-37|$ Vdc, $1 \leq I_L \leq 500$ mA)

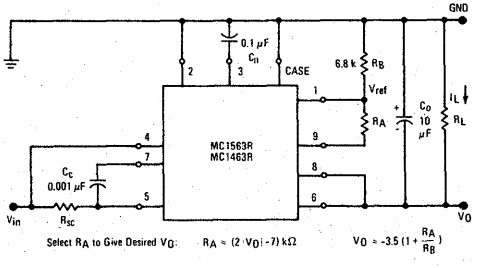


FIGURE 2 — TYPICAL NPN CURRENT BOOST CONNECTION
(V_O = 5.2 Vdc, I_L = 10 Adc [max])

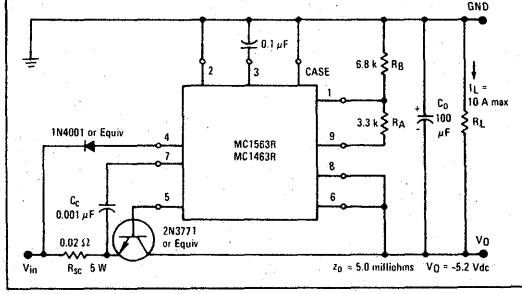
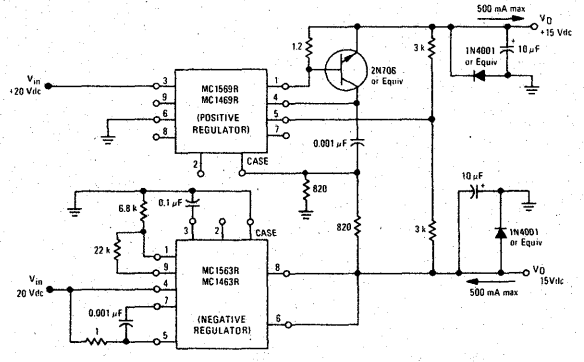


FIGURE 3 — ±15 V, ±400 mA COMPLEMENTARY TRACKING VOLTAGE REGULATOR



ORDERING INFORMATION		
DEVICE	TEMPERATURE RANGE	PACKAGE
MC1463G	0° C to +70° C	Metal Can
MC1463R	0° C to +70° C	Metal Power
MC1563G	−55° C to +125° C	Metal Can
MC1563R	−55° C to +125° C	Metal Power

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted.)

Rating	Symbol	Value		Unit
Input Voltage MC1463 MC1563	V_I	 −35 −40		Vdc
		G Package	R Package	
Load Current — Peak	I_L	250	600	mA
Current, Pin 2	I_2	10	10	mA
Power Dissipation and Thermal Characteristics T_A = 25°C Derate above T_A = 25°C Thermal Resistance, Junction to Air T_C = 25°C Derate above T_C = 25°C Thermal Resistance, Junction to Case	 P_D $1/R_{\theta JA}$ $R_{\theta JA}$ P_D $1/R_{\theta JC}$ $R_{\theta JC}$	 0.68 5.44 184 1.8 14.4 69.4	 2.4 16 62 9.0 61 17	 Watts mW/°C °C/W Watts mW/°C °C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

OPERATING TEMPERATURE RANGE

Operating Ambient Temperature Range MC1463 MC1563	T_A	 0 to +70 −55 to +125	°C

ELECTRICAL CHARACTERISTICS (I_L = 100 mAdc, T_C = +25°C, V_{in} = 15 V, V_O = 10 V unless otherwise noted.)

Characteristic	Fig.	Note	Symbol	MC1563 Min	MC1563 Typ	MC1563 Max	MC1463 Min	MC1463 Typ	MC1463 Max	Unit
Input Voltage (T_A = T_{low} ① to T_{high} ② I_L = 1.0 mA)	4	1,6	V_I	−8.5	–	−40	−9.0	–	−35	Vdc
Output Voltage Range (I_L = 1.0 mA)	4	–	V_O	−3.6	–	−37	−3.8	–	−32	Vdc
Reference Voltage (Pin 1 to Ground)	4	–	V_{ref}	−3.4	−3.5	−3.6	−3.2	−3.5	−3.8	Vdc
Minimum Input-Output Voltage Differential (R_{sc} = 0)	4	2	$\lvert V_{in} - V_O \rvert$	–	1.5	2.7	–	1.5	3.0	Vdc
Bias Current (Standby Current) (I_L = 1.0 mAdc, I_{IB} = I_I − I_L)	4	–	I_{IB}	–	7.0	11	–	7.0	14	mAdc
Output Noise (C_n = 0.1 μF, f = 10 Hz to 5.0 MHz)	4	–	v_N	–	120	–	–	120	–	μV(rms)
Temperature Coefficient of Output Voltage	4	3	$\Delta V_O/\Delta T$	–	±0.002	–	–	±0.002	–	%/°C
Operating Load Current Range (R_{sc} = 0.3 ohm) R Package (R_{sc} = 2.0 ohms) G Package	4	–	I_{LR}	 1.0 1.0	 – –	 500 200	 1.0 1.0	 – –	 500 200	mAdc
Input Regulation (V_{in} = 1.0 V rms, f = 1.0 kHz)	4	4	Reg_{line}	–	0.002	0.015	–	0.003	0.030	%/V_O
Load Regulation (T_J = Constant [1.0 mA ≤ I_L ≤ 20 mA]) (T_C = +25°C [1.0 mA ≤ I_L ≤ 50 mA]) R Package G Package	6	5	Reg_{load}	 – – –	 0.4 0.005 0.01	 1.6 0.05 0.13	 – – –	 0.7 0.005 0.01	 2.4 0.05 0.13	 mV %
Output Impedance (f = 1.0 kHz)	7	–	z_o	–	20	–	–	35	–	milliohms
Shutdown Current (V_I = −35 Vdc)	8	–	I_{sd}	–	7.0	15	–	14	50	μAdc

① T_{low} = 0°C for MC1463
= −55°C for MC1563

② T_{high} = +70°C for MC1463
= +125°C for MC1563

Heat sink required for T_{high} testing of "G" package.

Note 1. "Minimum Input Voltage" is the minimum "total instantaneous input voltage" required to properly bias the internal zener reference diode.

Note 2. This parameter states that the MC1563/MC1463 will regulate properly with the input-output voltage differential $|V_I - V_O|$ as low as 2.7 Vdc and 3.0 Vdc respectively. Typical units will regulate properly with $|V_I - V_O|$ as low as 1.5 Vdc as shown in the typical column.

Note 3. "Temperature Coefficient of Output Voltage" is defined as:

$$\Delta V_O/\Delta T = \frac{\pm (V_O \text{ max} - V_O \text{ min}) \ (100)}{\triangle T_A \ (V_O @ T_A = +25^oC)}$$

where $\triangle T_A = +180^oC$ for the MC1563
$+75^oC$ for the MC1463

The output-voltage adjusting resistors (R_A and R_B) must have matched temperature characteristics in order to maintain a constant ratio independent of temperature.

Note 4. Input regulation is the percentage change in output voltage per volt change in the input voltage and is expressed as

$$\text{Input Regulation} = \frac{V_O}{V_O \ (V_I)} \ 100 \ \ (\%/V_O).$$

where v_o is the change in the output voltage V_o for the input change v_{in}.

The following example illustrates how to compute maximum output voltage change for the conditions given:

$Reg_{in} = 0.015\%/V_O$
$V_O = 10$ Vdc
$v_{in} = 1.0$ V(rms)

$$V_O = \frac{(Reg_{line}) \ (V_I) \ (V_O)}{100}$$
$$= \frac{(0.015)(1.0)(10)}{100}$$
$$= 0.0015 \text{ V(rms)}$$

Note 5. Temperature drift effect must be taken into account separately for conditions of high junction temperature changes due to the thermal feedback that exists on the monolithic chip.

$$\text{Load Regulation} = \frac{V_O|_{I_L = 1.0 \text{ mA}} - V_O|_{I_L = 50 \text{ mA}}}{V_O|_{I_L = 1.0 \text{ mA}}} \times 100$$

Note 6. Not to exceed maximum package power dissipation.

TEST CIRCUITS

($I_L = 100$ mAdc, $T_C = +25^oC$ unless otherwise noted.)

FIGURE 4 – GENERAL TEST CIRCUIT

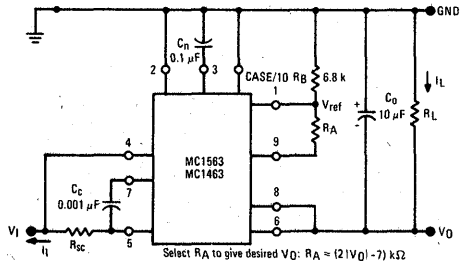


FIGURE 5 – LOAD TRANSIENT RESPONSE

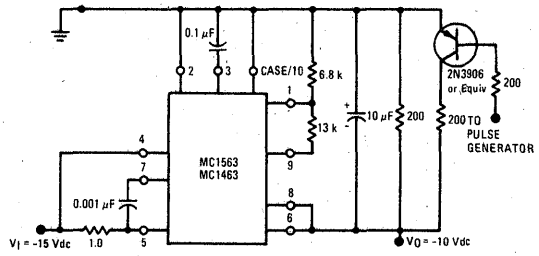


FIGURE 6 – LOAD REGULATION

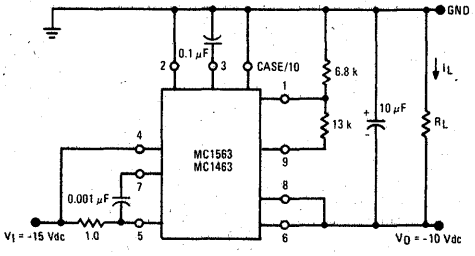


FIGURE 7 – OUTPUT IMPEDANCE

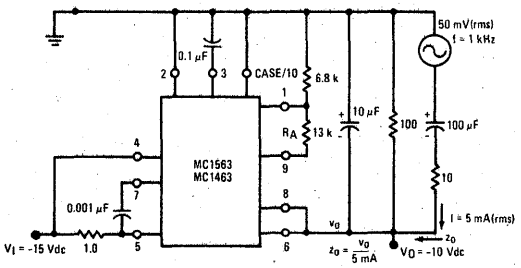
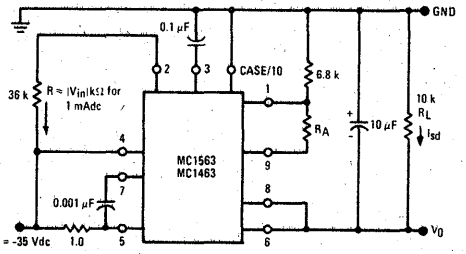


FIGURE 8 – SHUTDOWN CURRENT



GENERAL DESIGN INFORMATION

1. Output Voltage, V_O
   a) Output Voltage is set by resistors R_A and R_B (see Figure 9). Set R_B = 6.8 k ohms and determine R_A from the graph of Figure 11 or from the equation:

$$R_A \approx (2\,|V_O| - 7)\ k\Omega$$

   b) Output voltage can be varied by making R_A adjustable as shown in Figures 9 and 10.

   c) Output voltage, V_O, is determined by the ratio of R_A and R_B therefore optimum temperature performance can be achieved if R_A and R_B have the same temperature coefficient.

   d) $V_O = V_{ref}\left(1 + \frac{R_A}{R_B}\right)$; therefore the tolerance on output voltage is determined by the tolerance of V_{ref} and R_A and R_B.

2. Short-Circuit Current, I_{SC}
   Short-Circuit Current, I_{SC} is determined by R_{sc}. R_{sc} may be chosen with the aid of Figure 11 when using the typical circuit connection of Figure 9.

3. Compensation, C_c
   A 0.001 μF capacitor (C_c, see Figure 9), will provide adequate compensation in most applications, with or without current boost. Smaller values of C_c will reduce stability and larger values of C_c will degrade pulse response and output impedance versus frequency. The physical location of C_c should be close to the MC1563/MC1463 with short lead lengths.

4. Noise Filter Capacitor, C_n
   A 0.1 μF capacitor, C_n, from Pin 3 to ground will typically reduce the output noise voltage to 120 μV(rms). The value of C_n can be increased or decreased, depending on the noise voltage requirements of a particular application. A minimum value of 0.001 μF is recommended.

5. Output Capacitor, C_O
   The value of C_O should be at least 10 μF in order to provide good stability.

6. Shutdown Control
   One method of turning "OFF" the regulator is to draw 1 mA from Pin 2 (See Figure 8). This control can be used to eliminate power consumption by circuit loads which can be put in "standby" mode. Examples include, an ac or dc "squelch" control for communications circuits, and a dissipation control to protect the regulator under sustained output short-circuiting. As the magnitude of the input-threshold voltage at Pin 2 depends directly upon the junction temperature of the integrated circuit chip, a fixed dc voltage at Pin 2 will cause automatic shutdown for high junction temperatures. This will protect the chip, independent of the heat sinking used, the ambient temperature, or the input or output voltage levels. Standard Logic levels of MRTL, MDTL* or MTTL* can also be used to turn the regulator "ON" or "OFF".

7. Remote Sensing
   The connection to Pin 8 can be made with a separate lead direct to the load. Thus, "remote sensing" can be achieved and the effect of undesired impedances (including that of the milliammeter used to measure I_L) on z_o can be greatly reduced.

FIGURE 9 – TYPICAL CIRCUIT CONNECTION

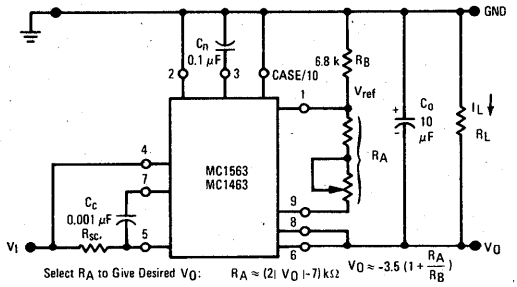


FIGURE 10 – R_A versus V_O

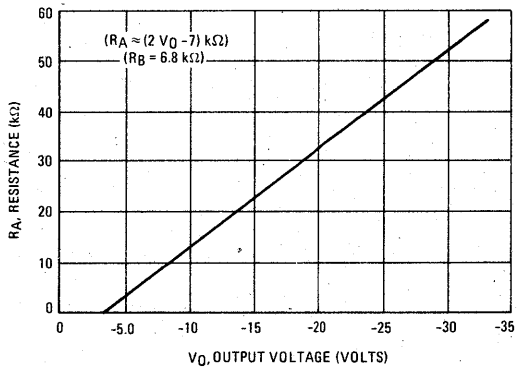
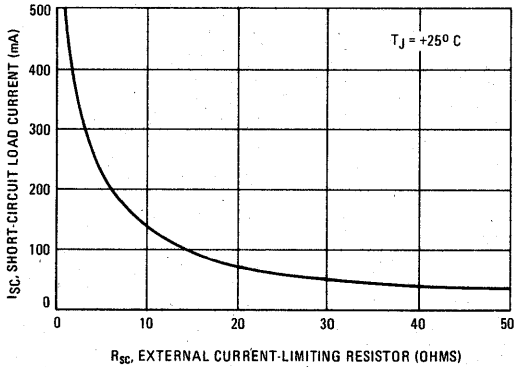


FIGURE 11 – I_{sc} versus R_{sc}



TYPICAL CHARACTERISTICS

Unless otherwise noted: $C_n = 0.1\,\mu F$, $C_c = 0.001\,\mu F$, $C_o = 10\,\mu F$, $T_C = +25^oC$, $V_{I(nom)} = -15$ Vdc, $V_{O(nom)} = -10$ Vdc, $I_L = 100$ mAdc.

FIGURE 12 – TEMPERATURE DEPENDENCE OF SHORT-CIRCUIT LOAD CURRENT

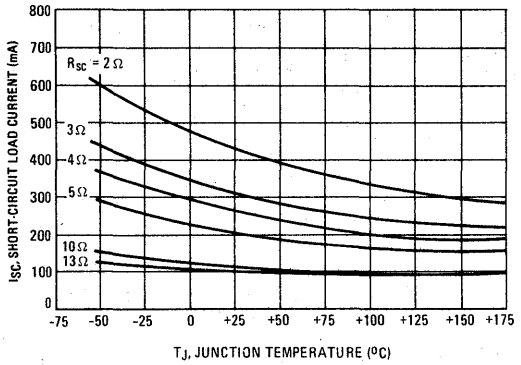


FIGURE 13 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE

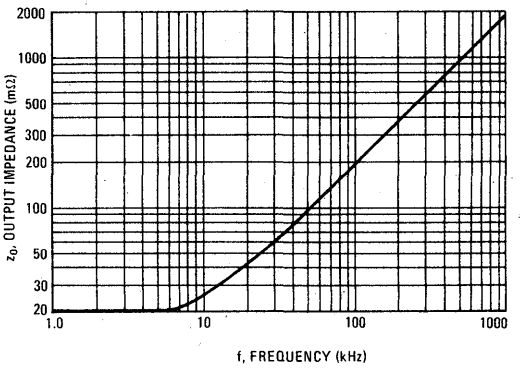


FIGURE 14 – DEPENDENCE OF OUTPUT IMPEDANCE ON OUTPUT VOLTAGE

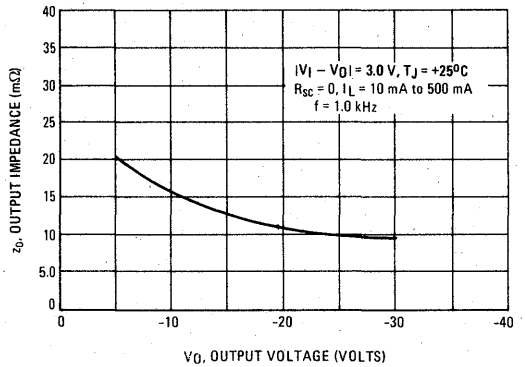


FIGURE 15 – OUTPUT IMPEDANCE versus R_{SC}

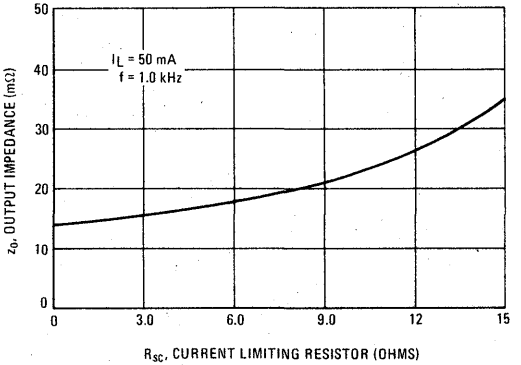
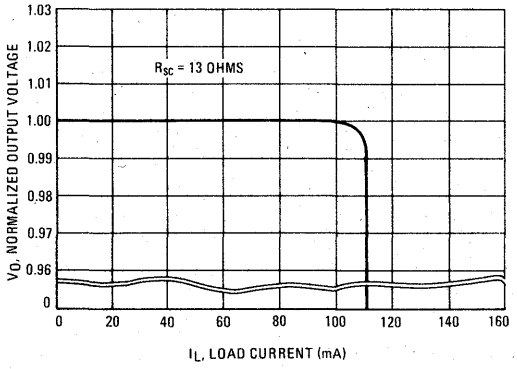


FIGURE 16 – CURRENT LIMITING CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

FIGURE 17 – BIAS CURRENT versus INPUT VOLTAGE

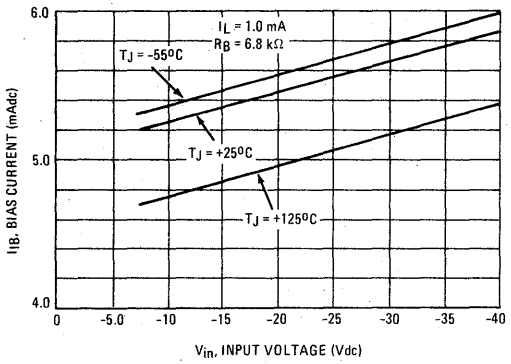


FIGURE 18 – EFFECTS OF LOAD CURRENT ON INPUT-OUTPUT VOLTAGE DIFFERENTIAL

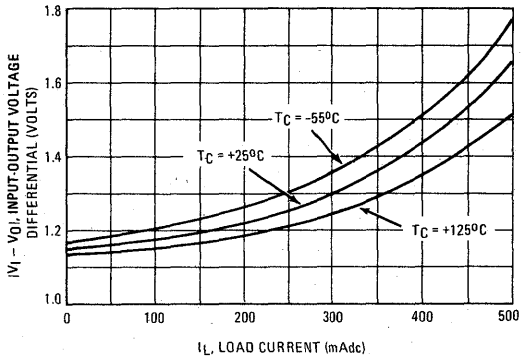


FIGURE 19 – EFFECT OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL ON INPUT REGULATION

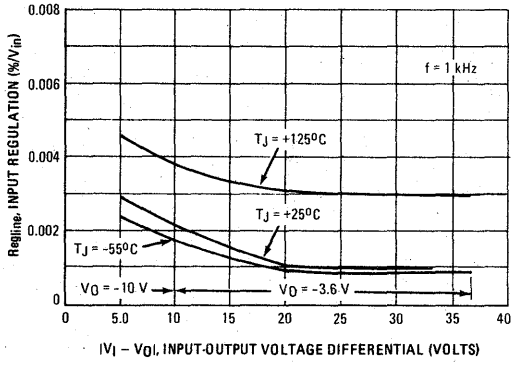


FIGURE 20 – INPUT TRANSIENT RESPONSE

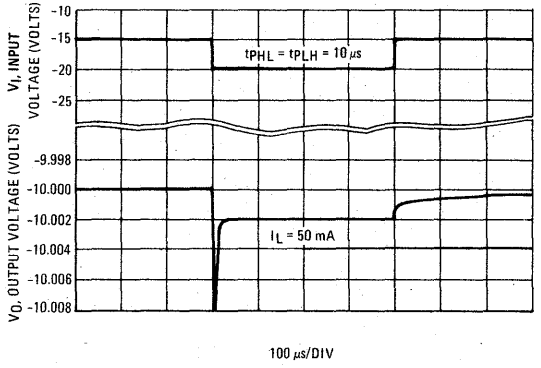


FIGURE 21 – LOAD TRANSIENT RESPONSE

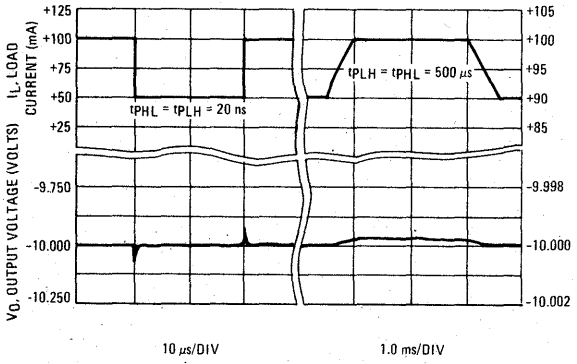
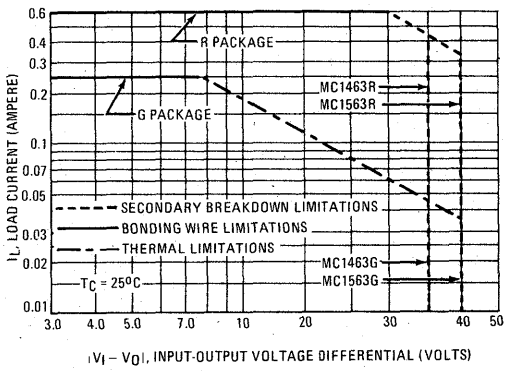


FIGURE 22 – DC OPERATING AREA



OPERATION AND APPLICATIONS

This section describes the operation and design of the MC1563 (MC1463) negative voltage regulator and also provides information on useful applications.

SUBJECT SEQUENCE INDEX

4

THEORY OF OPERATION

The usual series voltage regulator shown in Figure 23, consists of a reference voltage, an error amplifier, and a series control element. The error amplifier compares the output voltage with the reference voltage and adjusts the output accordingly until the error is essentially zero. For applications requiring output voltages larger than the reference, there are two options. The first is to use a resistive divider across the output and compare only a fraction of the output voltage to the reference. This approach suffers from reduced feedback to the error amplifier due to the attenuation of the resistive divider. This degrades load regulation especially at high voltage levels.

The alternative is to eliminate the resistive divider and to shift the reference voltage instead. To accomplish this, another amplifier is employed to amplify (or level shift) the reference voltage using an operational amplifier as shown in Figure 24. The gain-determining resistors may be external, enabling a wide range of output voltages. This is exactly the same approach used in the first option. That is, the output is being resistively divided to match the reference voltage. There is however, one big difference in that the output of this "regulator" is driving the input of another regulator (the error amplifier). The output of the reference amplifier has a relatively low impedance as compared to the input impedance of the error amplifier. Changes in the load of the output of the error amplifier are buffered to the extent that they have virtually no effect on the reference amplifier. If the feedback resistors are external (as they are on the MC1563) a wide range of reference voltages can be established.

The error amplifier can now be operated at unity gain to provide excellent regulation. In fact, this "regulator-within-a-regulator" concept permits the load regulation to be specified in terms of output impedance rather than as some percentage change of the output voltage. This approach was used in the design of the MC1563 negative voltage regulator.

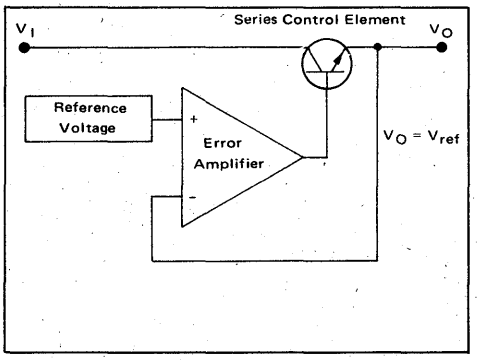


FIGURE 23 – Series Voltage Regulator

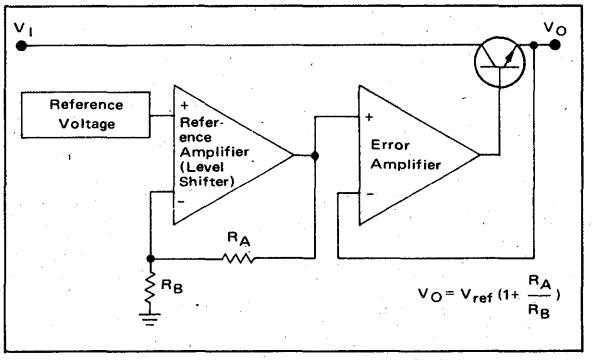
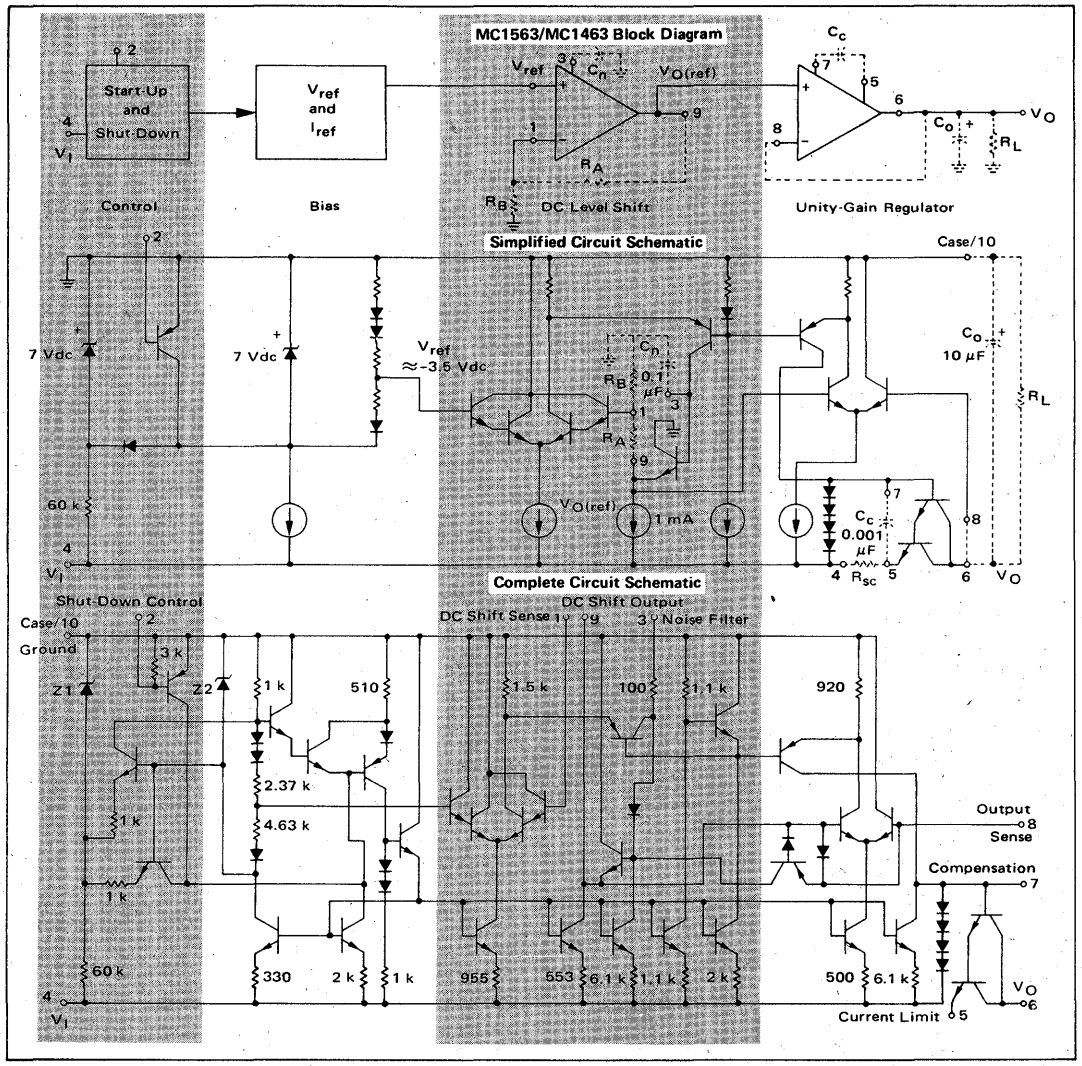


FIGURE 24 – The "Regulator-Within-A-Regulator" Approach

FIGURE 25
(Recommended External Circuitry is Depicted With Dotted Lines.)



MC1563 (MC1463) Operation

Figure 25 shows the MC1563 (MC1463) Negative Regulator block diagram, simplified schematic, and complete schematic. The four basic sections of the regulator are: Control, Bias, DC Level Shift, and Output (unity gain) Regulator. Each section is detailed in the following paragraphs.

Control

The control section involves two basic functions, start-up and shutdown. A start-up function is required since the biasing is essentially independent of the unregulated input voltage. It makes use of two zener diodes having the same breakdown voltage. A first or auxiliary zener is driven directly from the input voltage line through a resistor (60 kΩ) and permits the regulator to initially achieve the desired bias conditions. This permits the second, or reference zener to be driven from a current source. When the reference zener enters breakdown, the auxiliary zener is isolated from the rest of the regulator circuitry by a diode disconnect technique. This is necessary to keep the added noise and ripple of the auxiliary zener from degrading the performance of the regulator.

The shutdown control, in effect, consists of a PNP transistor across the reference zener diode. When this transistor is turned "ON", via Pin 2, the reference voltage is reduced to essentially zero volts and the regulator is forced to shutdown. During shutdown the current drain of the complete IC regulator drops to $V_{in}/60$ kΩ or 500 μA for a -30 V input.

Bias

A zener diode is the main reference element and forms the heart of the bias circuitry. Its positive temperature coefficient is balanced by the negative temperature coefficients of forward biased diodes in a ratio determined by the resistors in the diode string. The result is a reference voltage of approximately -3.5 Vdc with a typical temperature coefficient of 0.002%/°C. In addition, this circuit also provides a reference current which is used to bias all current sources in the remaining regulator circuitry.

4

DC Level Shift

The reference voltage is used as the input to a Darlington differential amplifier. The gain of this amplifier is quite high and it therefore may be considered to function as a conventional operational amplifier. Consequently, negative feedback can be employed using two external resistors (R_A and R_B) to set the closed-loop gain and to boost the reference voltage to the desired output voltage. A capacitor, C_n, is introduced externally into the level shift network (via Pin 3) to stabilize the amplifier and to filter the zener noise. The recommended value for this capacitor is 0.1 μF and should have a voltage rating in excess of the desired output voltage. Smaller capacitors (0.001 μF minimum) may be used but will cause a slight increase in output noise. Larger values of C_n will reduce the noise as well as delay the start-up of the regulator.

Output Regulator

The output of the shift amplifier is fed internally to the noninverting input of the output error amplifier. The inverting input to this amplifier is the Output Sense connection (Pin 8) of the regulator. A Darlington connected NPN power transistor is used to handle the load current. The short-circuit current limiting resistor, R_{SC}, is connected in the emitter of this transistor to sample the full load current. This connection enables a four-diode string to limit the drive current to the power transistors in a conventional manner.

Stability and Compensation

As has been seen, the MC1563 employs two amplifiers, each using negative feedback. This implies the possibility of frequency instability due to excessive phase shift at high frequencies. Since the error amplifier is normally used at unity gain (the worst case for stability) a high impedance node is brought out for compensation. For normal operation, a capacitor is connected between this point (Pin 7) and Pin 5. The recommended value of 0.001 μF will insure stability and still provide acceptable transient response (see Figure 21). It is also necessary to use an output capacitor, C_O, (typically 10 μF) directly from the output (Pin 6) to ground. When an external transistor is used to boost the current, C_O = 100 μF is recommended (see Figure 26).

NPN CURRENT BOOSTING

For applications requiring more than 500 mA of load current, or for minimizing voltage variations due to temperature changes in the IC regulator arising from changes of the internal power dissipation, the NPN current-boost circuits of Figure 2 or 26, are recommended. The circuit shown in Figure 26 can supply up to approximately 4.0 amperes (subject to safe area limitations). At higher currents the V_{BE} of the pass transistor may itself exceed the threshold of the current limit even for R_{SC} = 0. Figure 2 illustrates the use of an additional external diode from Pin 4 for higher current operation or for pass transistors exhibiting higher V_{BE}'s. It will probably be necessary to determine R_{SC} experimentally for each case where a pass transistor is used because V_{BE} varies from device to device.

The circuit of Figure 26 when set up for a -10 V output

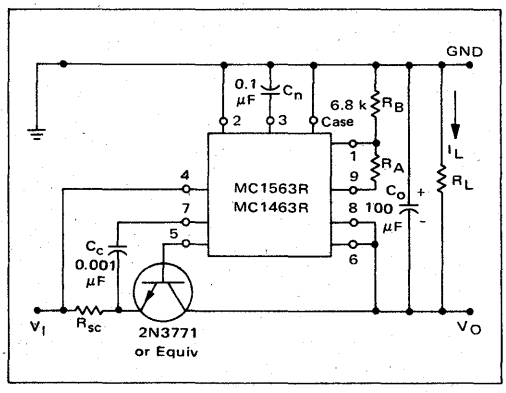


FIGURE 26 – Typical NPN Current Boost Connection

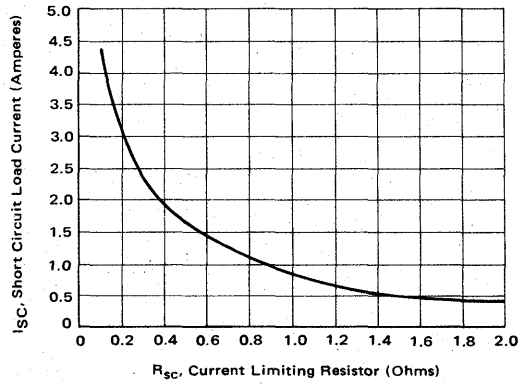


FIGURE 27 – I_{SC} versus R_{SC} (reference Figure 26)

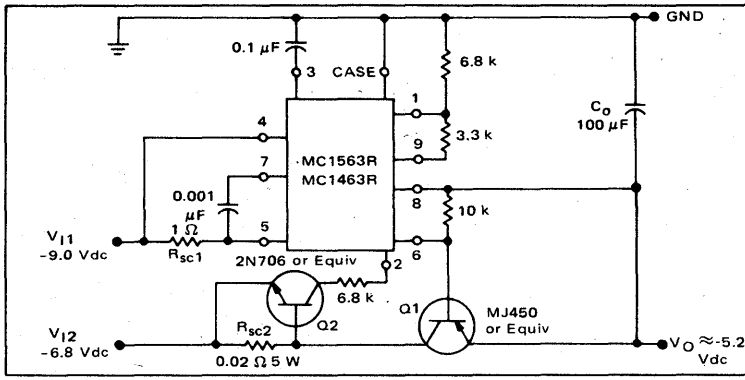


FIGURE 28 – PNP Current Boost Connection

(R_A = 13 kΩ) supply and operating with a -15 V input, with a R_{SC} of 0.1 Ω, will yield a change in output voltage of only 26 mV over a load current range of from 1 mA to 3.5 A. This corresponds to a dc output impedance of only 7.5 milliohms or a percentage load regulation of 0.26% for a full 3.5-ampere load current change. Figure 27 indicates how the short circuit current varies with the value of R_{SC} for this circuit.

PNP CURRENT BOOSTING

A PNP power transistor can also be used to boost the load current capabilities. To improve the efficiency of the PNP boost configuration, particularly for small output voltages, the circuit of Figure 28, is recommended. An auxiliary -9 volt supply is used to power the IC regulator and the heavy load current is obtained from a second supply of lower voltage. For the 10-ampere regulator of Figure 28 this represents a savings of 22 watts when compared with operating the regulator from the single -9 V supply. It can supply current to 10 amperes while requiring an input voltage to the collector of the pass transistor of -6.8 volts minimum. The pass transistor is limited to 10 amperes by the added short-circuit current network in its emitter (R_{SC2}) and the IC regulator is limited to 500 mA in the conventional manner (R_{SC1}). The MJ450 exhibits a minimum h_{FE} of 20 at 10 amperes, thus requiring only 500 mA from the MC1563R. Regulation of this circuit is comparable to that of the NPN boost configuration.

For higher output voltages the additional unregulated power supply is not required. The collector of the PNP boost transistor can tie directly to Pin 5 and the internal current limit circuit will provide short-circuit protection using R_{SC} (see Figure 11). Transistor Q2 and R_{SC2} will not be required and Pin 2 should be returned to ground.

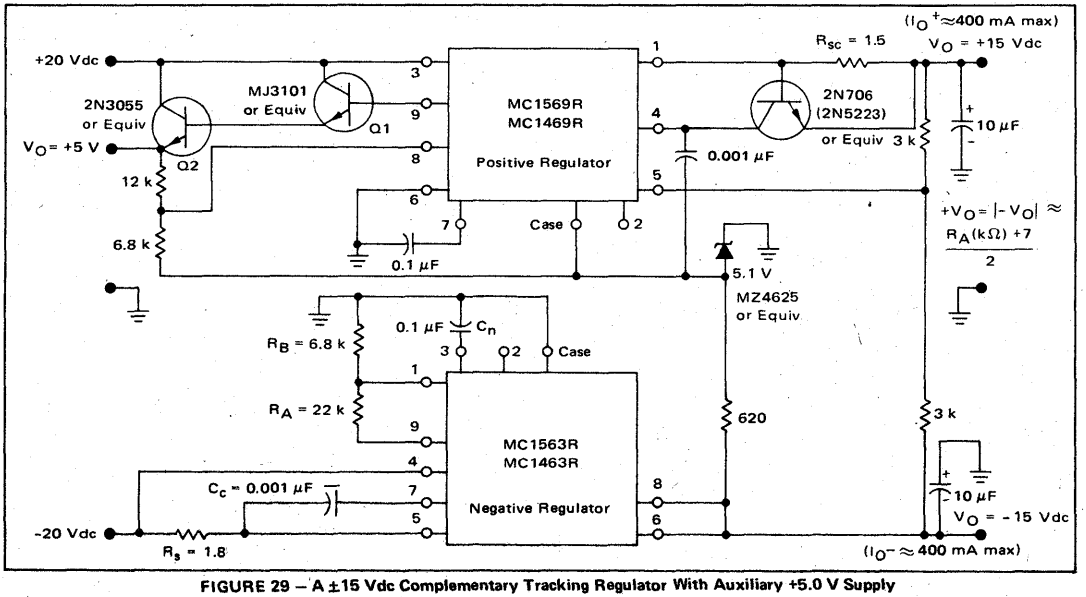


FIGURE 29 – A ±15 Vdc Complementary Tracking Regulator With Auxiliary +5.0 V Supply

(MC1563 – Pg. 10)

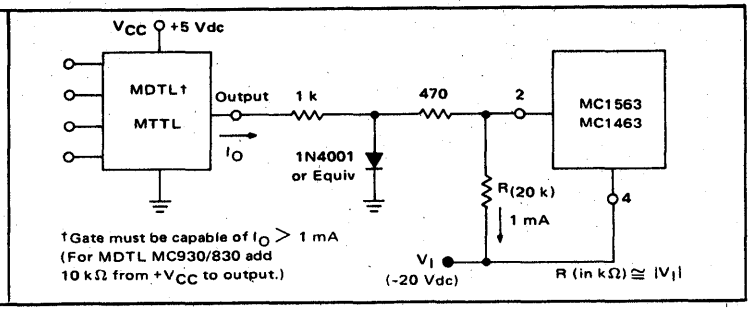


FIGURE 30 – Saturated Logic Level Shutdown Circuit

POSITIVE AND NEGATIVE POWER SUPPLIES

If the MC1563 is driven from a floating source it is possible to use it as a positive regulator by grounding the negative output terminal. The MC1563 may also be used with the MC1569 to provide completely independent positive and negative power regulators with comparable performance. When used in this manner a silicon diode such as the 1N4001 must be connected as a clamp on the output with the cathode to ground and the anode to the negative output voltage. This is to prevent the positive voltage in the system from forcing the output to a positive value and preventing the MC1563 from starting up.

Some applications may require complementary tracking in which both supplies arrive at the voltage level simultaneously, and variations in the magnitudes of the two voltages track. Figures 3 and 29 illustrate this approach. In this application, the MC1563 is used as the reference regulator, establishing the negative output voltage. The MC1569 positive regulator is used in a tracking mode by grounding one side of the differential amplifier (Pin 6 of the MC1569) and using the other side (Pin 5 of the MC1569) to sense the voltage developed at the junction of the two 3 k-ohm resistors. This differential amplifier controls the MC1569 series pass transistor such that the voltage at Pin 5 will be zero. When the voltage at pin 5 equals zero, $+|V_O|$ must equal $-|V_O|$.

For the configuration shown in Figure 29, the level shift amplifier in the MC1569 is employed to generate an auxiliary +5-volt supply which is boosted to a 2-ampere capability by Q1 and Q2. (The +5-volt supply, as shown, is not short-circuit protected.) The -15-volt supply varies less than 0.1 mV over a zero to -300 mAdc current range and the +15-volt supply tracks this variation. The +15-volt supply varies 20 mV over the zero to +300-mAdc load current range. The +5-volt supply varies less than 5 mV for $0 \leq I_L \leq 200$ mA with the other two voltages remaining unchanged. See MC1561 data sheet or MC1569 data sheet for information concerning latch-up when using plus and minus regulations.

SHUTDOWN TECHNIQUES

Pin 2 of the MC1563 is provided for the express purpose of shutting the regulator "OFF". Referring to the schematic, it can be seen that pin 2 goes to the base of a PNP transistor; which, if turned "ON", will deny current to all the biasing current sources. This action causes the output to go to essentially zero volts and the only current drawn by the IC regulator will be the small start current through the 60 k-ohm start resistor ($V_{in}/60$ kΩ). This feature provides additional versatility in the applications of the MC1563. Various sub-systems may be placed in a "standby" mode to conserve power until actually needed. Or the power may be turned "OFF" in response to other occurrences such as over-heating, over-voltage, shorted output, etc.

As an illustration of the first case, consider a system consisting of both positive-supply logic (MTTL) and negative-supply logic (MECL). The MECL logic may be used in a high-speed arithmetic processor whose services are not continuously required. Substantial power may

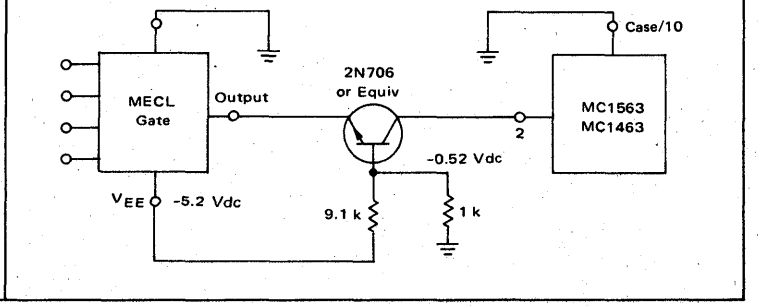


FIGURE 31 – MECL Logic Level Shutdown Circuit

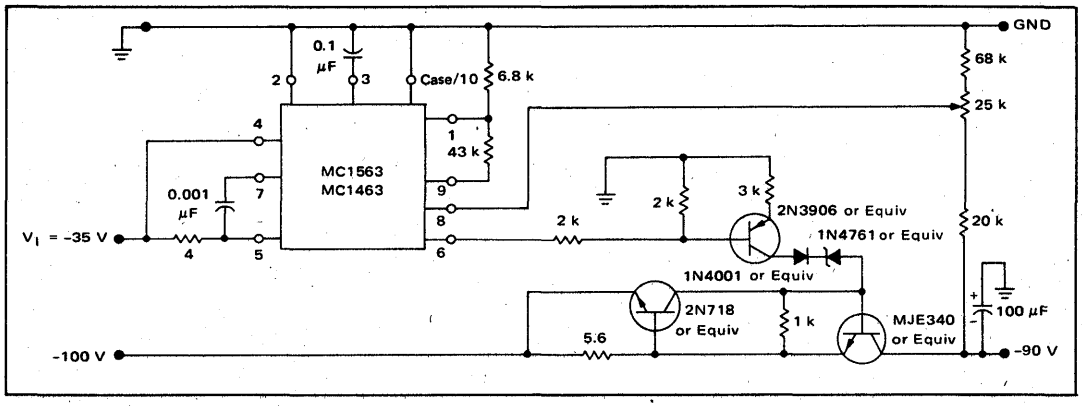


FIGURE 32 – Voltage Boosting Circuit

thus be conserved if the MECL circuitry remains unpowered except when needed. The negative regulator can be shutdown using any of the standard logic swings. For saturated logic control, Figure 30 shows a circuit that allows the normal positive output swing to cause the regulator to shutdown when the logic output is in the low voltage state. The negative output levels of a MECL gate can also be used for shutdown control as shown in Figure 31.

VOLTAGE BOOSTING

Some applications may require a high output voltage which may exceed the voltage rating of the MC1563. This must be solved by assuring that the IC regulator is operated within its limits. Three points in the regulator need to be considered:

1. The input voltage (Pin 4),
2. the output voltage (Pin 6) and,
3. the output sense lead (Pin 8).

A reduced input voltage can be provided by using a separate supply. The output voltage may be zener-level shifted, and the sense line can tie to a portion of the output voltage through a resistive divider. The voltage boost circuit of Figure 32 uses this approach to provide a -90 volt supply. This circuit will exhibit regulation of 0.001% over a 100 mA load current range.

REMOTE SENSING

The MC1563 offers a remote sensing capability. This is important when the load is remote from the regulator, as the resistances of the interconnecting lines (V_{EE} and GND) are added directly to the output impedance of the regulator. By remote sensing, this resistance is included inside the control loop of the regulator and is essentially eliminated. Figure 33 shows how remote sensing is accomplished using both a separate sense line from Pin 8 and a separate ground line from the regulator to the remote load.

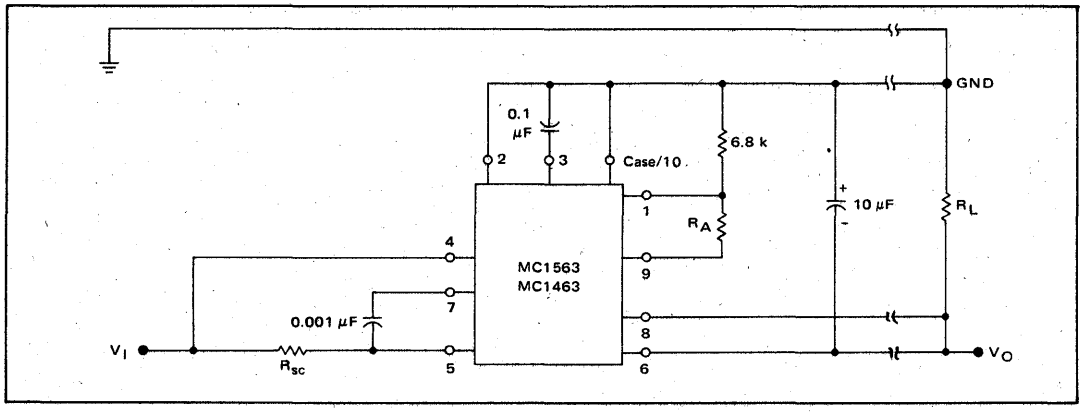


FIGURE 33 – Remote Sensing Circuit

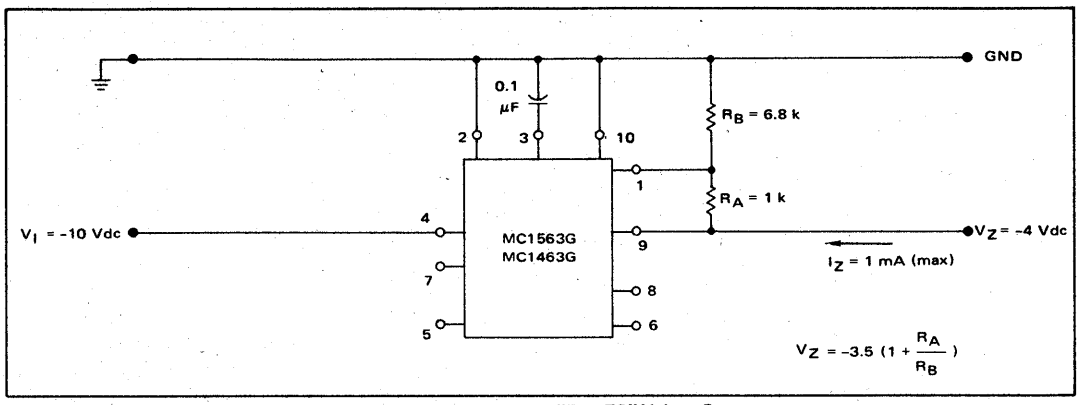


FIGURE 34 – An Adjustable "Zero-TC" Voltage Source

4

AN ADJUSTABLE ZERO-TEMPERATURE-COEFFICIENT (0-TC) VOLTAGE REFERENCE SOURCE

The MC1563, when used in conjunction with low-TC resistors, makes an excellent reference-voltage generator. If the -3.5 volt reference voltage of the IC regulator is a satisfactory value, then Pins 1 and 9 can be tied together and no resistors are needed. This will provide a voltage reference having a typical temperature coefficient of 0.002%/°C. By adding two resistors, R_A and R_B, any voltage between -3.5 Vdc and -37 Vdc can be obtained with the same low TC (see Figure 34)

THERMAL SHUTDOWN

By setting a fixed voltage at Pin 2, the MC1563 chip can be protected against excessive junction temperatures caused by power dissipation in the IC regulator. This is based on the negative temperature coefficient of the base-emitter junction of the shutdown transistor (-1.9 x 10^{-3}V/°C). By setting -0.61 Vdc externally, at Pin 2, the regulator will shutdown when the chip temperature reaches approximately 140°C. Figure 35 shows a circuit that uses a zero-TC zener diode and a resistive divider to obtain this voltage.

In the case where an external pass transistor is employed; its temperature, rather than that of the IC regulator, requires control. A technique similar to the one just discussed can be used by directly monitoring the case temperature of the pass transistor as is indicated in Figure 36. The case of the normally "OFF" thermal monitoring transistor, Q2, should be in thermal contact with, but electrically isolated from, the case of the boost transistor, Q1.

THERMAL CONSIDERATIONS

Monolithic voltage regulators are subjected to internal heating similar to a power transistor. Since the degree of internal heating is a function of the specific application,

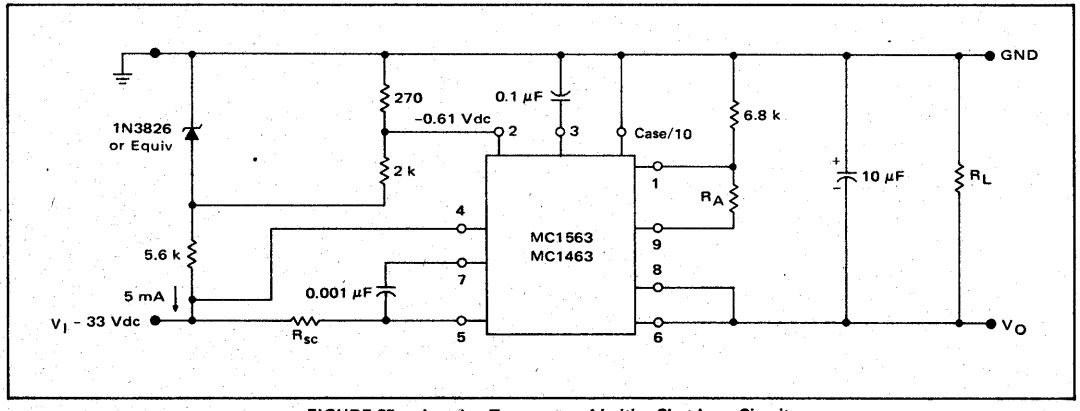


FIGURE 35 – Junction Temperature Limiting Shutdown Circuit

(MC1563 – Pg. 13)

the designer must use caution not to exceed the specified maximum junction temperature (+175°C). Exceeding this limit will reduce reliability at an exponential rate. Good heatsinking not only reduces the junction temperature for a given power dissipation; it also tends to improve the dc stability of the output voltage by reducing the junction temperature change resulting from a change in the power dissipation of the IC regulator. By using the derating factors or thermal resistance values given in the Maximum Ratings Table of this data sheet, junction temperature can be computed for any given application in the same manner as for a power transistor*. A short-circuit on the output terminal can produce a "worst-case" thermal condition especially if the maximum input voltage is applied simultaneously with the maximum value of short-circuit load current (500 mA). Care should be taken not to exceed the maximum junction temperature rating during this fault condition and, in addition, the dc safe operating area limit (see Figure 22).

Thermal characteristics for a voltage regulator are useful in predicting performance since dc load and line regulation are affected by changes in junction temperature. These temperature changes can result from either a change in the ambient temperature, T_A, or a change in the power dissipated in the IC regulator. The effects of ambient temperature change on the dc output voltage can be estimated from the "Temperature Coefficient of Output Voltage" characteristic parameter shown as ±0.002%/°C, typical. Power dissipation is typically changed in the IC regulator by varying the dc load current. To estimate the dc change in output voltage due to a change in the dc load current, three effects must be considered:

1. junction temperature change due to the change in the power dissipation
2. output voltage decrease due to the finite output impedance of the control amplifier
3. thermal gradient on the IC chip.

A temperature differential does exist across a power IC chip and can cause a dc shift in the output voltage. A "gradient coefficient," GCV_O, can be used to describe this effect and is typically +0.03%/watt for the MC1563R. For an example of the relative magnitudes of these effects, consider the following conditions:

Given: MC1563R

with V_I = -10 Vdc

V_O = -5 Vdc

and I_L = 100 mA to 200 mA
(ΔI_L = 100 mA)

assume T_A = +25°C

TO-66 Type Case with heatsink

*For more detailed information of methods used to compute junction temperature, see Motorola Application Note AN-226, Measurement of Thermal Properties of Semiconductors.

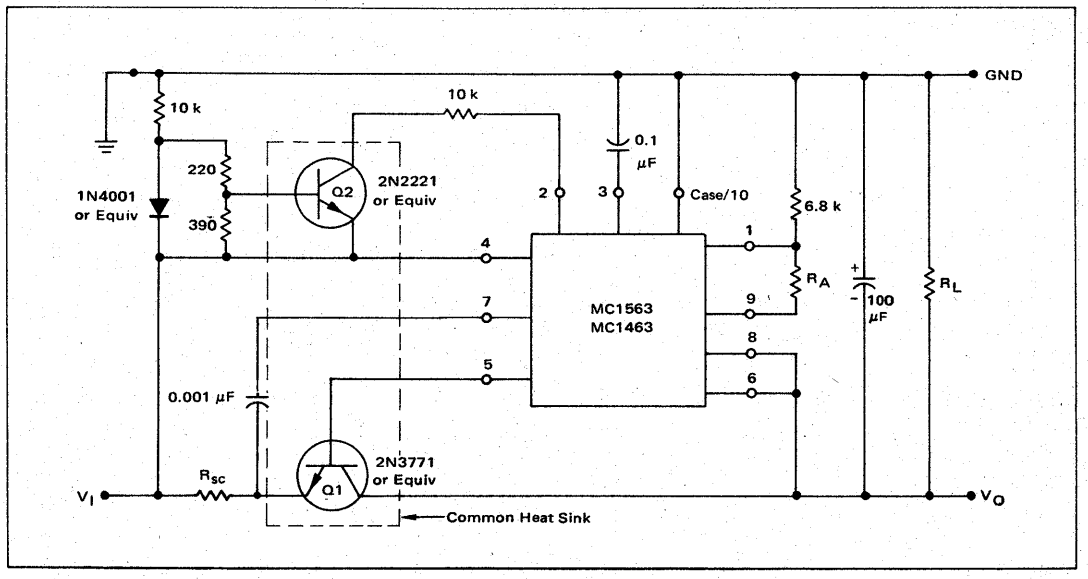


FIGURE 36 – Thermal Shutdown When Using External Pass Transistors

assume $R_{\theta CS} = 0.2^{o}C/W$

and $R_{\theta SA} = 2^{o}C/W$

It is desired to find the ΔV_O which results from this ΔI_L. Each of the three previously stated effects on V_O can now be separately considered.

1. ΔV_O due to ΔT_J

$$\Delta V_O = (V_O)(\Delta P_D)(\Delta V_O/\Delta T)(R_{\theta JC}+R_{\theta CS}+R_{\theta SA})$$

OR

$$\Delta V_O = (5\ V)(5\ V \times 0.1\ A)(\pm 0.002\%/^{o}C)(19.2^{o}C/W)$$

$$\Delta V_O \approx \pm 1.0\ mW$$

2. ΔV_O due to z_o

$$|\Delta V_O| = (-z_o)(I_L)$$

$$|\Delta V_O| = -(2 \times 10^{-2})(10^{-1}) = -2\ mV$$

3. ΔV_O due to gradient coefficient, $\Delta V_O/\Delta G$

$$|\Delta V_O| = (\Delta V_O/\Delta G)(V_O)(\Delta P_D)$$

$$|\Delta V_O| = (+3 \times 10^{-4}/W)(5\ volts)(5 \times 10^{-1} W)$$

$$|\Delta V_O| = +0.8\ mV$$

Therefore the total ΔV_O is given by

$$|\Delta V_O\ total| = \pm 1.0 - 2.0 + 0.8\ mV$$

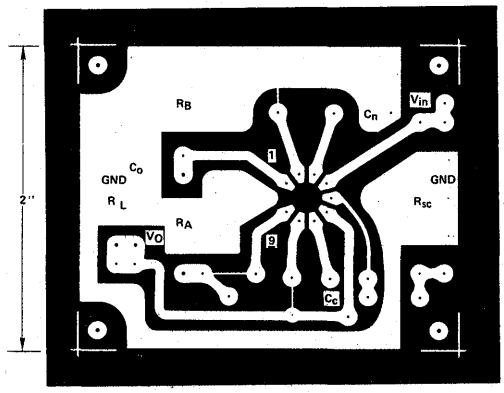
OR

$$-2.2\ mV \leqslant |V_O\ total| \leqslant -0.2\ mV$$

Other operating conditions may be substituted and computed in a similar manner to evaluate the relative effects of the parameters.

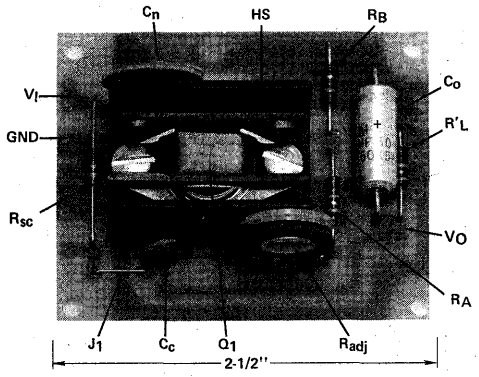
4

Typical Printed Circuit Board Layout



(MC1563 – Pg. 15)

FIGURE 37 – Location of Components



Note 1:
When R_{adj} is used it is necessary to remove the copper which shorts out R_{adj}.

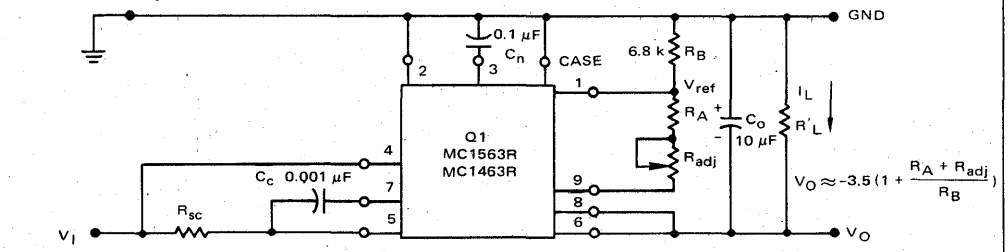
Note 2:
Extra holes are available in the circuit board to permit two resistors to be paralleled to obtain the desired value of R_{sc}.

Note 3:
If Pin 2 is used to shut down the regulator, remove the copper which shorts Pin 2 to ground.

Note 4:
Remote sensing can be achieved by removing the copper which shorts Pin 8 to Pin 6 and connecting Pin 8 directly to the "minus" load terminal. The circuit board ground should be connected to the unregulated power supply ground at the "plus" load terminal.

4

Typical Circuit Connection for Output Voltages Between -3.5 and -37 Volts



Select $R_A + R_{adj}$ to Give Desired V_O: $R_A + R_{adj} \approx (2|V_O| - 7)\ k\Omega$ with $R_B = 6.8\ k\Omega$

PARTS LIST

Component	Value	Description
R_A	Select	1/4 or 1/2 watt carbon
R_B	6.8 k	1/4 or 1/2 watt carbon
R_{adj}	Select	IRC Model X-201, Mallory Model MTC-1 or equivalent
R_{sc}	Select	1/2 watt carbon
R'_L	Select	For minimum current of 1 mAdc
C_o	10 μF	Sprague 1500 Series, Dickson D10C series or equivalent
C_n	0.1 μF	Ceramic Disc – Centralab DDA104, or equivalent
C_C	0.001 μF	Sprague TG-P10, or equivalent
J_1		Jumper
Q1		MC1563R or MC1463R
*HS		Heatsink Thermalloy #6168B or equivalent
*Socket	(Not Shown)	Robinson Nugent #0001306 or equivalent Electronic Molding Corp. #6341-210-1, 6348-188-1, 6349-188-1 or equivalent
PC Board		Circuit DOT, Inc. #PC1113 or equivalent 1155 W. 23rd St. Tempe, Arizona 85281

*Optional

(MC1563 – Pg. 16)

MC1466L
MC1566L

Specifications and Applications Information

MONOLITHIC VOLTAGE AND CURRENT REGULATOR

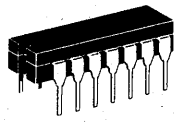
This unique "floating" regulator can deliver hundreds of volts — limited only by the breakdown voltage of the external series pass transistor. Output voltage and output current are adjustable. The MC1466/MC1566 integrated circuit voltage and current regulator is designed to give "laboratory" power-supply performance.

- Voltage/Current Regulation with Automatic Crossover
- Excellent Line Voltage Regulation, 0.01% +1.0 mV
- Excellent Load Voltage Regulation, 0.01% +1.0 mV
- Excellent Current Regulation, 0.1% +1.0 mA
- Short-Circuit Protection
- Output Voltage Adjustable to Zero Volts
- Internal Reference Voltage
- Adjustable Internal Current Source

PRECISION WIDE-RANGE VOLTAGE and CURRENT REGULATOR

EPITAXIAL PASSIVATED INTEGRATED CIRCUIT

CERAMIC PACKAGE
CASE 632
TO-116



ORDERING INFORMATION		
Device	**Temperature Range**	**Package**
MC1466L	0°C to +70° C	Ceramic DIP
MC1566L	−55°C to +125°C	Ceramic DIP

TYPICAL APPLICATIONS

FIGURE 1 – 0-TO-15 VDC, 10-AMPERES REGULATOR

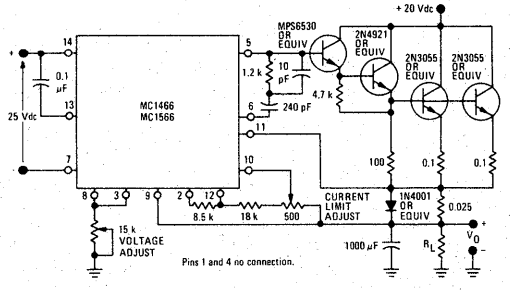


FIGURE 2 – 0-TO-40 VDC, 0.5-AMPERE REGULATOR

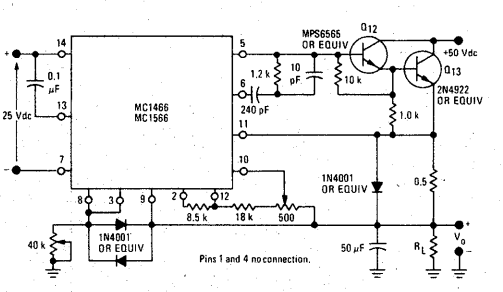


FIGURE 3 – 0-TO-250 VDC, 0.1-AMPERE REGULATOR

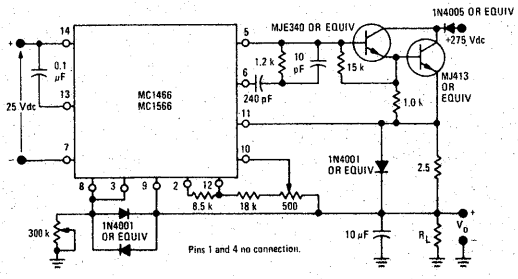
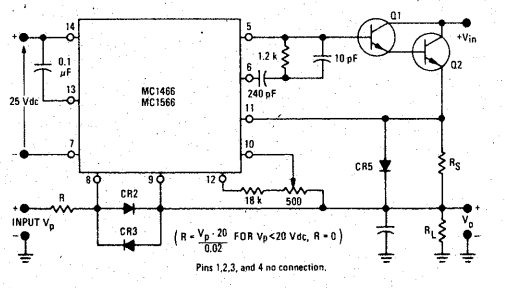


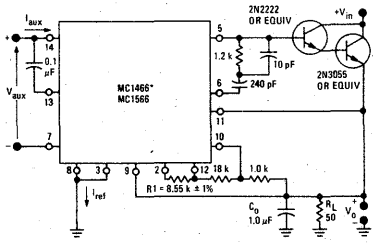
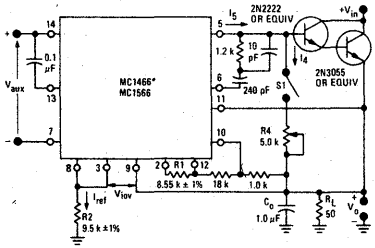
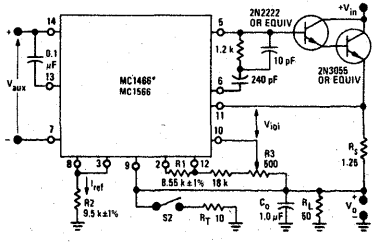
FIGURE 4 – REMOTE PROGRAMMING



MAXIMUM RATINGS (T_A = +25° unless otherwise noted)

Rating		Symbol	Value	Unit
Auxiliary Voltage	MC1466 MC1566	V_{aux}	 30 35	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +50°C		P_D $1/\theta_{JA}$	750 6.0	mW mW/°C
Operating Temperature Range	MC1466 MC1566	T_A	 0 to +70 −55 to +125	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{aux} = +25 Vdc unless otherwise noted)

Characteristic Definition	Characteristic		Symbol	Min	Typ	Max	Units
	Auxiliary Voltage (See Notes 1 & 2) (Voltage from pin 14 to pin 7)	MC1466 MC1566	V_{aux}	 21 20	 – –	 30 35	Vdc
	Auxiliary Current	MC1466 MC1566	I_{aux}	 – –	 9.0 7.0	 12 8.5	mAdc
	Internal Reference Voltage (Voltage from pin 12 to pin 7)	MC1466 MC1566	V_{IR}	 17.3 17.5	 18.2 18.2	 19.7 19	Vdc
	Reference Current (See Note 3)	MC1466 MC1566	I_{ref}	 0.8 0.9	 1.0 1.0	 1.2 1.1	mAdc
	Input Current-Pin 8	MC1466 MC1566	I_8	 – –	 6.0 3.0	 12 6.0	µAdc
	Power Dissipation	MC1466 MC1566	P_D	 – –	 – –	 360 300	mW
	Input Offset Voltage, Voltage Control Amplifier (See Note 4)	MC1466 MC1566	V_{iov}	 0 3.0	 15 15	 40 25	mVdc
	Load Voltage Regulation (See Note 5)	MC1466 MC1566	ΔV_{iov}	 – –	 1.0 0.7	 3.0 1.0	mV
		MC1466 MC1566	$\Delta V_{ref}/V_{ref}$	 – –	 0.015 0.004	 0.03 0.01	%
	Line Voltage Regulation (See Note 6)	MC1466 MC1566	ΔV_{iov}	 – –	 1.0 0.7	 3.0 1.0	mV
		MC1466 MC1566	$\Delta V_{ref}/V_{ref}$	 – –	 0.015 0.004	 0.03 0.01	%
	Temperature Coefficient of Output Voltage (T_A = 0 to +75°C) (T_A = −55 to +25°C) (T_A = +25 to +125°C)	 MC1466 MC1566 MC1566	TCV_o	 – – –	 0.01 0.006 0.004	 – – –	%/°C
	Input Offset Voltage, Current Control Amplifier (See Note 4) (Voltage from pin 10 to pin 11)	MC1466 MC1566	V_{ioi}	 0 3.0	 15 15	 40 25	mVdc
	Load Current Regulation (See Note 7)	MC1466 MC1566	$\Delta I_L/I_L$	 – –	 – –	 0.2 0.1	%
		MC1466 MC1566	ΔI_{ref}	 – –	 – –	 1.0 1.0	mAdc

*Pins 1 and 4 no connection.

NOTE 1:
The instantaneous input voltage, V_{aux}, must not exceed the maximum value of 30 volts for the MC1466 or 35 volts for the MC1566. The instantaneous value of V_{aux} must be greater than 20 volts for the MC1566 or 21 volts for the MC1466 for proper internal regulation.

NOTE 2:
The auxiliary supply voltage V_{aux}, must "float" and be electrically isolated from the unregulated high voltage supply, V_{in}.

NOTE 3:
Reference current may be set to any value of current less than 1.2 mAdc by applying the relationship:

$$I_{ref}\,(mA) = \frac{8.55}{R_1\,(k\Omega)}\ .$$

NOTE 4:
A built-in offset voltage (15 mVdc nominal) is provided so that the power supply output voltage or current may be adjusted to zero.

NOTE 5:
Load Voltage Regulation is a function of two additive components, ΔV_{iov} and ΔV_{ref}, where ΔV_{iov} is the change in input offset voltage (measured between pins 8 and 9) and ΔV_{ref} is the change in voltage across R2 (measured between pin 8 and ground). Each component may be measured separately or the sum may be measured across the load. The measurement procedure for the test circuit shown is:

a. With S1 open ($I_4 = 0$) measure the value of $V_{iov}\,(1)$ and $V_{ref}\,(1)$
b. Close S1, adjust R4 so that $I_4 = 500\ \mu A$ and note $V_{iov}\,(2)$ and $V_{ref}\,(2)$.

Then $\Delta V_{iov} = V_{iov}\,(1) - V_{iov}\,(2)$

% Reference Regulation =

$$\frac{[V_{ref}\,(1) - V_{ref}\,(2)]}{V_{ref}\,(1)}\,(100\%) = \frac{\Delta V_{ref}}{V_{ref}}\,(100\%)$$

Load Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}}\,(100\%) + \Delta V_{iov}\ .$$

NOTE 6:
Line Voltage Regulation is a function of the same two additive components as Load Voltage Regulation, ΔV_{iov} and ΔV_{ref} (see note 5). The measurement procedure is:

a. Set the auxiliary voltage, V_{aux}, to 22 volts for the MC1566 or the MC1466. Read the value of $V_{iov}\,(1)$ and $V_{ref}\,(1)$.
b. Change the V_{aux} to 28 volts for the MC1566 or the MC1466 and note the value of $V_{iov}\,(2)$ and $V_{ref(2)}$. Then compute Line Voltage Regulation:

$\Delta V_{iov} = \Delta V_{iov}\,(1) - V_{iov}\,(2)$

% Reference Regulation =

$$\frac{[V_{ref}\,(1) - V_{ref}\,(2)]}{V_{ref}\,(1)}\,(100\%) = \frac{\Delta V_{ref}}{V_{ref}}\,(100\%)$$

Line Voltage Regulation =

$$\frac{\Delta V_{ref}}{V_{ref}}\,(100\%) + \Delta V_{iov}\ .$$

NOTE 7:
Load Current Regulation is measured by the following procedure:

a. With S2 open, adjust R3 for an initial load current, $I_{L(1)}$, such that V_O is 8.0 Vdc.
b. With S2 closed, adjust R_T for $V_O = 1.0$ Vdc and read $I_{L(2)}$. Then Load Current Regulation =

$$\frac{[I_{L(2)} - I_{L(1)}]}{I_{L(1)}}\,(100\%) + I_{ref}$$

where I_{ref} is 1.0 mAdc, Load Current Regulation is specified in this manner because I_{ref} passes through the load in a direction opposite that of load current and does not pass through the current sense resistor, R_S.

FIGURE 5

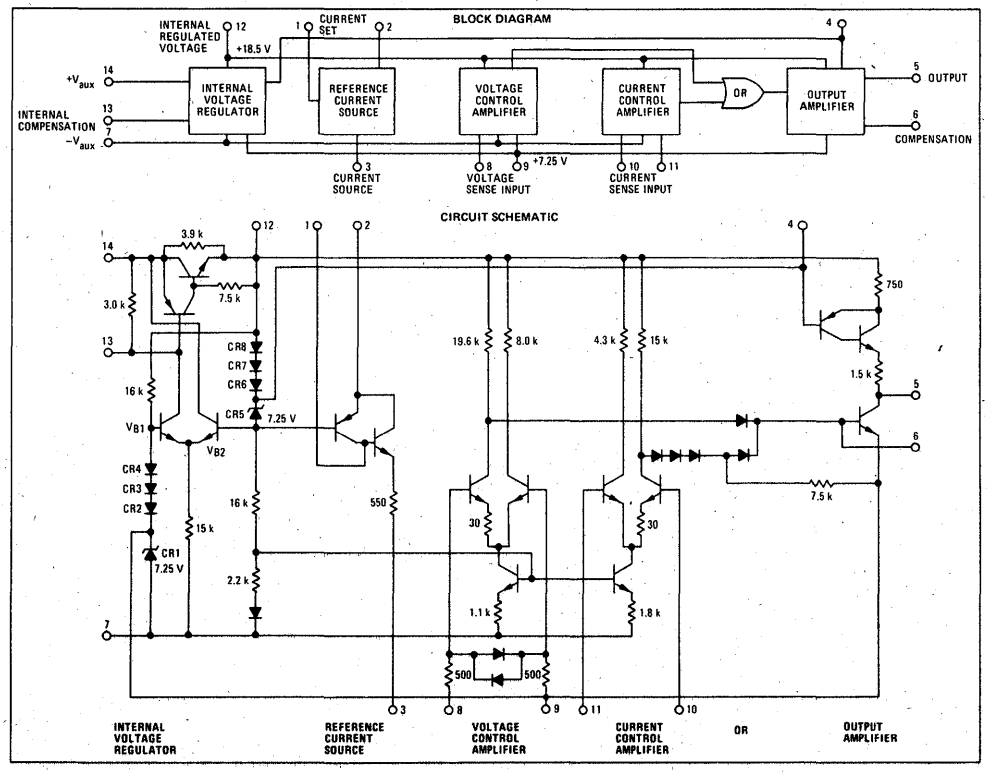
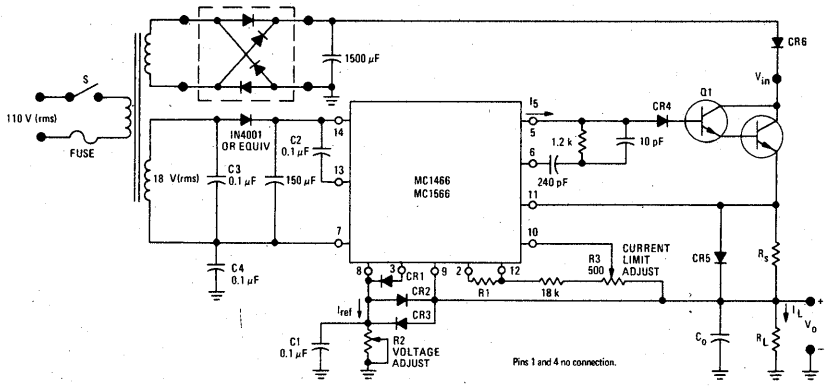
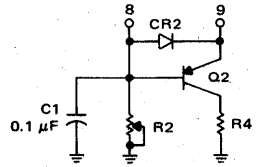


FIGURE 6 – TYPICAL CIRCUIT CONNECTION



NORMAL DESIGN PROCEDURE AND DESIGN CONSIDERATIONS

1. Constant Voltage:
   For constant voltage operation, output voltage V_O is given by:
   $$V_O = (I_{ref})(R_2)$$
   where R2 is the resistance from pin 8 to ground and I_{ref} is the output current of pin 3.
   The recommended value of I_{ref} is 1.0 mAdc. Resistor R1 sets the value of I_{ref}:
   $$I_{ref} = \frac{8.5}{R_1}$$
   where R1 is the resistance between pins 2 and 12.
2. Constant Current:
   For constant current operation:
   (a) Select R_S for a 250 mV drop at the maximum desired regulated output current, I_{max}.
   (b) Adjust potentiometer R3 to set constant current output at desired value between zero and I_{max}.
3. If V_{in} is greater than 20 Vdc, CR2, CR3, and CR4 are necessary to protect the MC1466/MC1566 during short-circuit or transient conditions.
4. In applications where very low output noise is desired, R2 may be bypassed with C1 (0.1 μF to 2.0 μF). When R2 is bypassed, CR1 is necessary for protection during short-circuit conditions.
5. CR5 is recommended to protect the MC1466/MC1566 from simultaneous pass transistor failure and output short-circuit.
6. The RC network (10 pF, 240 pF, 1.2 k ohms) is used for compensation. The values shown are valid for all applications. However, the 10 pF capacitor may be omitted if f_T of Q1 and Q2 is greater than 0.5 MHz.
7. For remote sense applications, the positive voltage sense terminal (pin 9) is connected to the positive load terminal through a separate sense lead; and the negative sense terminal (the ground side of R2) is connected to the negative load terminal through a separate sense lead.
8. C_O may be selected by using the relationship:
   $C_O = (100\ \mu F)\ I_{L(max)}$, where $I_{L(max)}$ is the maximum load current in amperes.
9. C2 is necessary for the internal compensation of the MC1466/MC1566.
10. For optimum regulation, current out of pin 5, I_5, should not exceed 0.5 mAdc. Therefore select Q1 and Q2 such that:
    $$\frac{I_{max}}{\beta 1 \beta 2} \leqslant 0.5 \text{ mAdc}$$
    where: I_{max} = maximum short-circuit load current (mAdc)
    $\beta 1$ = minimum beta of Q1
    $\beta 2$ = minimum beta of Q2
    Although Pin 5 will source up to 1.5 mAdc, $I_5 > 0.5$ mAdc will result in a degradation in regulation.
11. CR6 is recommended when $V_O > 150$ Vdc and should be rated such that Peak Inverse Voltage $> V_O$.
12. In applications where R2 might be rapidly reduced in value, it is recommended that CR3 be replaced by Q2 and R4.



This design consideration prevents R2 from being destroyed by excessive discharge current from C_O. Components Q2 and R4 should be selected such that:

$$R4 = \frac{R2}{10} \text{ and}$$

$$BV_{CEO} \text{ of Q2} \geqslant V_O$$

OPERATION AND APPLICATIONS

This section describes the operation and design of the MC1566/MC1466 voltage and current regulator and also provides information on useful applications.

SUBJECT SEQUENCE

Theory of Operation
Applications
Transient Failures
Voltage/Current-Mode Indicator

4

THEORY OF OPERATION

The schematic of Figure 5 can be simplified by breaking it down into basic functions, beginning with a simplified version of the voltage reference, Figure 7. Zener diodes CR1 and CR5 with their associated forward biased diodes CR2 through CR4 and CR6 through CR8 form the stable reference needed to balance the differential amplifier. At balance ($V_{B1} = V_{B2}$), the output voltage, ($V_{12} - V_7$), is at a value that is twice the drop across either of the two diode strings: $V_{12} - V_7 = 2\,(V_{CR1} + V_{CR2} + V_{CR3} + V_{CR4})$. Other voltages, temperature compensated or otherwise, are also derived from these diodes strings for use in other parts of the circuit.

The voltage controlled current source (Figure 8) is a PNP-NPN composite which, due to the high NPN beta, yields a good working PNP from a lateral device working at a collector current of only a few microamperes. Its base voltage (V_{B2}) is derived from a temperature compensated portion of the diode string and consequently the overall current is dependent on the value of emitter resistor R1. Temperature compensation of the base emitter junction of Q3 is not important because approximately 9 volts exists between V_{B2} and V_{12}, making the ΔV_{BE}'s very small in percentage. Circuit reference voltage is derived from the product of I_R and R_R; if I_R is set at 1 mA (R1 = 8.5 kΩ), then R_R (in kΩ) = V_O. Other values of current may be used as long as the following restraints are kept in mind: 1) package dissipation will be increased by about 11 mW/mA and 2) bias current for the voltage control amplifier is 3 μA, temperature dependent, and is extracted from the reference current. The reference current should

FIGURE 7 – REFERENCE VOLTAGE REGULATOR

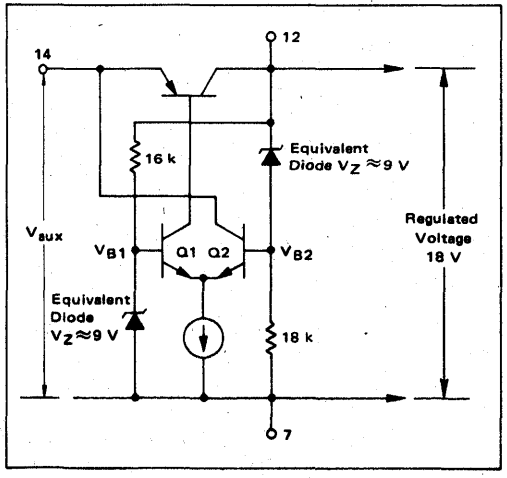
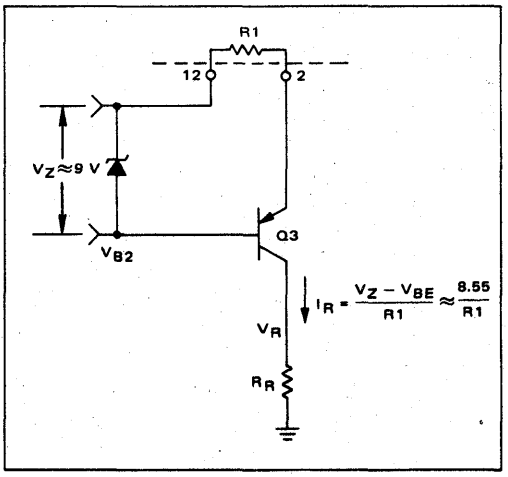


FIGURE 8 – VOLTAGE CONTROLLED CURRENT SOURCE



be at least two orders of magnitude above the largest expected bias current.

Loop amplification in the constant voltage mode is supplied by the voltage controlled amplifier (Figure 9), a standard high-gain differential amplifier. The inputs are diode-protected against differential overvoltages and an emitter degenerating resistor, R_{OS}, has been added to one of the transistors. For an emitter current in both Q5 and Q6 of 1/2 milliampere there will exist a preset offset voltage in this differential amplifier of 15 mV to insure that the output voltage will be zero when the reference voltage is zero. Without R_{OS}, the output voltage could be a few millivolts above zero due to the inherent offset. Since the load resistor is so large in this stage compared with the load (Q9) it will be more instructive to look at the gain on a transconductance basis rather than voltage gain. Transconductance of the differential stage is defined for small signals as:

$$g_m = \frac{I}{2r_e + R_E} \qquad (1)$$

where

$$r_e \approx \frac{0.026}{I_E} \text{ and}$$

R_E = added emitter degenerating resistance.

For $I_E = 0.5$ mA,

$$g_m = \frac{1}{104+30} = \frac{1}{134} = 7.5 \text{ mA/volt.} \qquad (2)$$

FIGURE 9 – VOLTAGE CONTROL AMPLIFIER

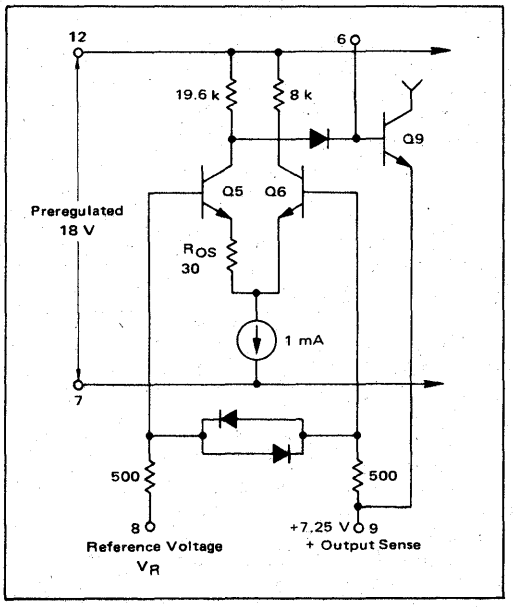
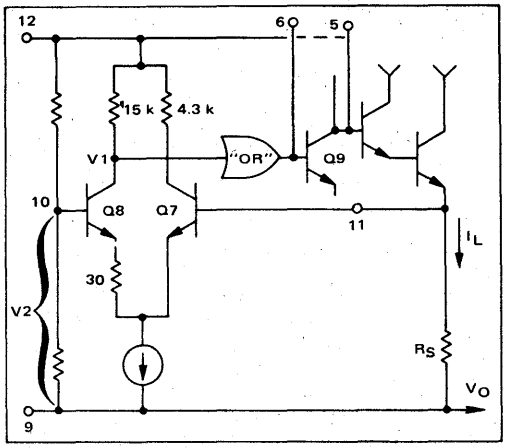


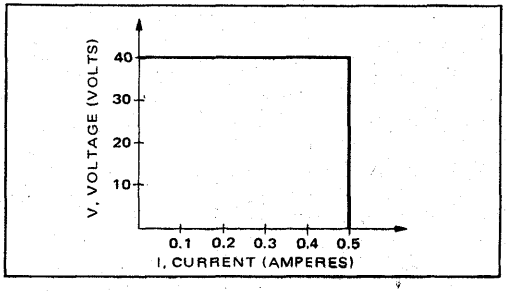
FIGURE 10 – CURRENT CONTROL CIRCUIT



This level is further boosted by the output stage such that in the constant voltage mode overall transconductance is about 300 mA/volt.

A second differential stage nearly identical to the first stage, serves as the current control amplifier (Figure 10). The gain of this stage insures a rapid crossover from the constant voltage to constant current modes and provides a convenient point to control the maximum deliverable load current. In use, a reference voltage derived from the preregulator and a voltage divider is applied to pin 10 while the output current is sampled across R_S by pin 11. When I_L R_S is 15 mV below the reference value, voltage V_1 begins to rapidly rise, eventually gaining complete control of Q9 and limiting output current to a value of V_2/R_S. If V_2 is derived from a variable source, short circuit current may be controlled over the complete output current capability of the regulator. Since the constant-voltage to constant-current change-over requires only a few millivolts the voltage regulation maintains its quality to the current limit and accordingly shows a very sharp "knee" (1% +1 mA, Figure 11). Note that the regulator can switch back into the constant voltage mode if the output voltage reaches a value greater than V_R. Operation through zero milliamperes is guaranteed by the inclusion of another emitter offsetting resistor.

FIGURE 11 – V_I CURVE FOR 0-TO-40 V, 0.5-AMPERE REGULATOR



Transistor Q9 and five diodes comprise the essential parts of the output stage (Figure 12). The diodes perform an "OR" function which allows only one mode of operation at a time - constant current or constant voltage. However, an additional stage (Q9) must be included to invert the logic and make it compatible with the driving requirements of series pass transistors as well as provide additional gain. A 1.5 mA collector current source sets the maximum deliverable output current and boosts the output impedance to that of the current source.

Note that the negative (substrate) side of the MC1566/MC1466 is 7.25 volts lower than the output voltage, and the reference regulator guarantees that the positive side is 11 volts above the output. Thus the IC remains at a voltage (relative to ground) solely dependent on the output, "floating" above and below V_O. V_{CE} across Q9 is only two or three V_{BE}'s depending on the number of transistors used in the series pass configuration.

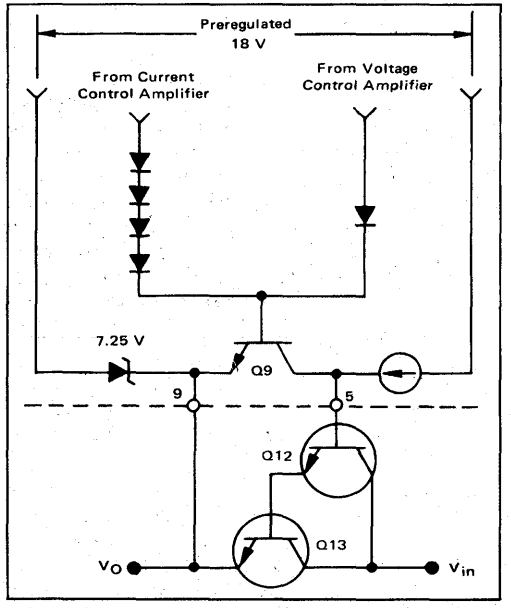
Performance characteristics of the regulator may be approximately calculated for a given circuit (Figure 2). Assuming that the two added transistors (Q12 and Q13) have minimum beta's of 20, then the overall regulator transconductance will be:

$$g_{mT} = (400)\,300 \text{ mA/volt} = 120 \text{ A/volt.} \quad (3)$$

For a change in current of 500 mA the output voltage will drop only:

$$\Delta V = \frac{0.5}{120} = 4.2 \text{ mV.} \quad (4)$$

FIGURE 12 – MC1566 OUTPUT STAGE



The analysis thus far does not consider changes in V_R due to output current changes. If I_L increases by 500 mA the collector current of Q9 decreases by 1.25 mA, causing the collector current of Q5 to increase by 30 μA. Accordingly, I_R will be decreased by $\approx$0.30 μA which will drop the output by 0.03%. This figure may be improved considerably by either using high beta devices as the pass transistors, or by increasing I_R. Note again, however, that the maximum power rating of the package must be kept in mind. For example if I_R = 4 mA, power dissipation is

$$P_D = 20 \text{ V } (8 \text{ mA}) + (11 \text{ V} \times 3 \text{ mA}) = 193 \text{ mW.} \quad (5)$$

This indicates that the circuit may be safely operated up to 118°C using 20 volts at the auxiliary supply voltage. If, however, the auxiliary supply voltage is 35 volts,

$$P_D = 35 \text{ V } (8 \text{ mA}) + 26 \text{ V } (3 \text{ mA}) = 358 \text{ mW.} \quad (6)$$

which dictates that the maximum operating temperature must be less than 91°C to keep package dissipation within specified limits.

Line voltage regulation is also a function of the voltage change between pins 8 and 9, and the change of V_{ref}. In this case, however, these voltages change due to changes in the internal regulator's voltages, which in turn are caused by changes in V_{aux}. Note that line voltage regulation is not a function of V_{in}. Note also that the instantaneous value of V_{aux} must always be between 20 and 35 volts.

Figure 6 shows six external diodes (CR_1 to CR_6) added for protective purposes. CR_1 should be used if the output voltage is less than 20 volts and CR_2, CR_3 are absent. For V_O higher than 20 volts, CR_1 should be discarded in favor of CR_2 and CR_3. Diode CR_4 prevents IC failure if the series pass transistors develop collector-base shorts while the main power transistor suffers a simultaneous open emitter. If the possibility of such a transistor failure mode seems remote, CR_4 may be deleted. To prevent instantaneous differential and common-mode breakdown of the current sense amplifier, CR_5 must be placed across the current limit resistor R_S.

Load transients occasionally produce a damaging reversal of current flow from output to input $V_O > 150$ volts (which will destroy the IC). Diode CR_6 prevents such reversal and renders the circuit immune from destruction for such conditions, e.g., adding a large output capacitor after the supply is turned "on". Diodes CR_1, CR_2, CR_3, and CR_5 may be general purpose silicon units such as 1N4001 or equivalent whereas CR_4 and CR_6 should have a peak inverse voltage rating equal to V_{in} or greater.

APPLICATIONS

Figure 2 shows a typical 0-to-40 volts, 0.5-ampere regulator with better than 0.01% performance. The RC network between pins 5 and 6 and the capacitor between pins 13 and 14 provide frequency compensation for the MC1566/MC1466. The external pass transistors are used to boost load current, since the output current of the regulator is less than 2 mA.

Figure 1 is a 0-to-15 volts, 10-ampere regulator with the pass transistor configuration necessary to boost the load current to 10 amperes. Note that C_O has been increased to 1000 μF following the general rule:

$$C_O = 100\ \mu F/A\ I_L.$$

The prime advantage of the MC1566/MC1466 is its use as a high voltage regulator, as shown in Figure 3. This 0-to-250 volts 0.1-ampere regulator is typical of high voltage applications, limited only by the breakdown and safe areas of the output pass transistors.

The primary limiting factor in high voltage series regulators is the pass transistor. Figure 13 shows a safe area curve for the MJ413. Looking at Figure 3, we see that if the output is shorted, the transistor will have a collector current of 100 mA, with a V_{CE} approximately equal to 260 volts. Thus this point falls on the dc line of the safe area curve, insuring that the transistor will not enter secondary breakdown.

In this respect (Safe Operating Area) the foldback circuit of Figure 14 is superior for handling high voltages and yet is short-circuit protected. This is due to the fact that load current is diminished as output voltage drops (V_{CE} increases as V_O drops) as seen in Figure 15. By careful design the load current at a short, I_{SC} can be made low enough such that the combined V_{CE} (V_{in}) and I_{SC} still falls within the dc safe operating area of the transistor. For the illustrated design (Figure 14), an input voltage of 210 volts is compatible with a short-circuit current of 100 mA. Yet current foldback allows us to design for a maximum regulated load current of 500 mA. The pertinent design equations are:

Let $R_2\ (k\Omega) = V_O$

$$\alpha = \frac{0.25}{V_O}\left[\frac{I_k}{I_{SC}} - 1\right]$$

$$R_1\ (k\Omega) = \frac{\alpha}{1-\alpha}\ V_O$$

$$R_{SC} = \frac{0.25}{(1-\alpha)\ I_{SC}}$$

FIGURE 13 – SAFE AREA CURVE FOR THE MJ413

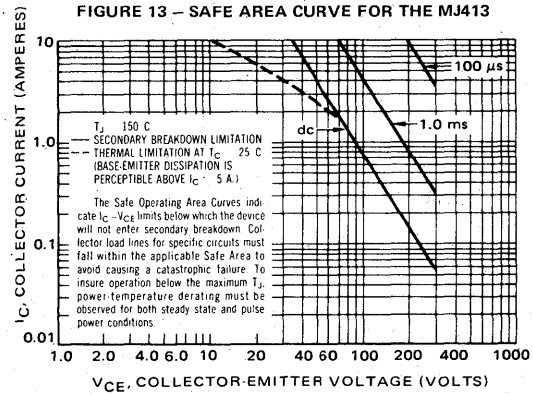
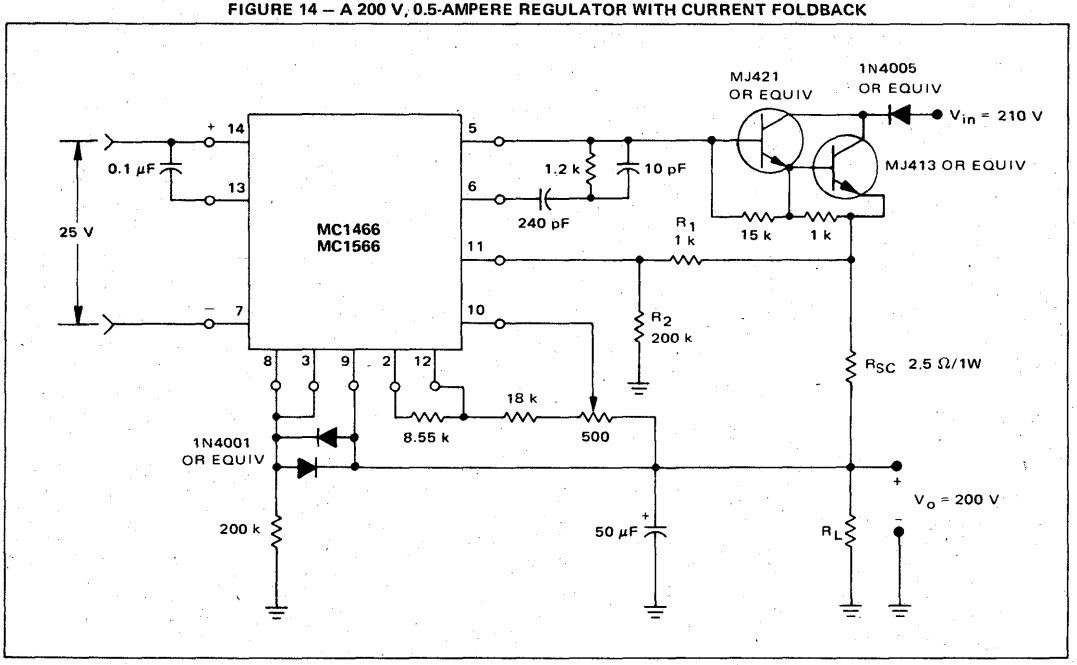


FIGURE 14 – A 200 V, 0.5-AMPERE REGULATOR WITH CURRENT FOLDBACK



The terms I_{SC} and I_K correspond to the short-circuit current and maximum available load current as shown in Figure 15.

FIGURE 15 – TYPICAL FOLDBACK PERFORMANCE

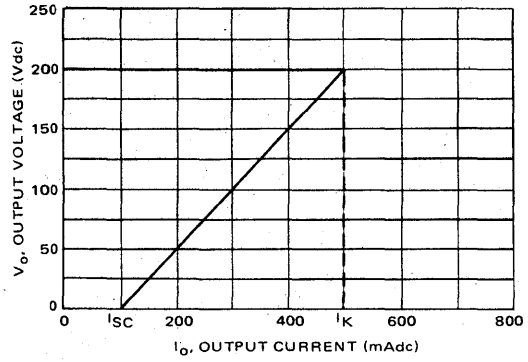


Figure 16 shows a remote sense application which should be used when high current or long wire lengths are used. This type of wiring is recommended for any application where the best possible regulation is desired. Since the sense lines draw only a small current, large voltage drops do not destroy the excellent regulation of the MC1566/MC1466.

TRANSIENT FAILURES

In industrial areas where electrical machinery is used the normal ac line often contains bursts of voltage running from hundreds to thousands of volts in magnitude and only microseconds in duration. Under some conditions this energy is dissipated across the internal zener connected between pins 9 and 7. This transient condition may produce a total failure of the regulator device without any apparent explanation. This type of failure is identified by absence of the 7-volt zener (CR1) between pin 9 and pin 7. To prevent this failure mode the use of a shielded power transformer is recommended, as shown in Figure 6. In addition, it is recommended that C1, C3 and C4 be included to aid in transient repression. These capacitors should have good high frequency characteristics.

If the possibility of transients on the output exists, the addition of a resistor and zener diode between pins 9 and 7 as shown on Figure 17 should be added.

VOLTAGE/CURRENT – MODE INDICATOR

There may be times when it is desirable to know when the MC1566/MC1466 is in the constant current mode or constant voltage mode. A mode indicator can be easily added to provide this feature. Figure 18 shows how a PNP transistor has replaced a protection doide between pins 8 and 9 of Figure 2. When the MC1566/MC1466 goes from constant voltage mode to constant current mode, V_O will drop below V_8 and the PNP transistor will turn on. The 1-mA current supplied by pin 8 will now be shunted to base of Q2 thereby turning on the indicator device I1.

FIGURE 16 – REMOTE SENSE

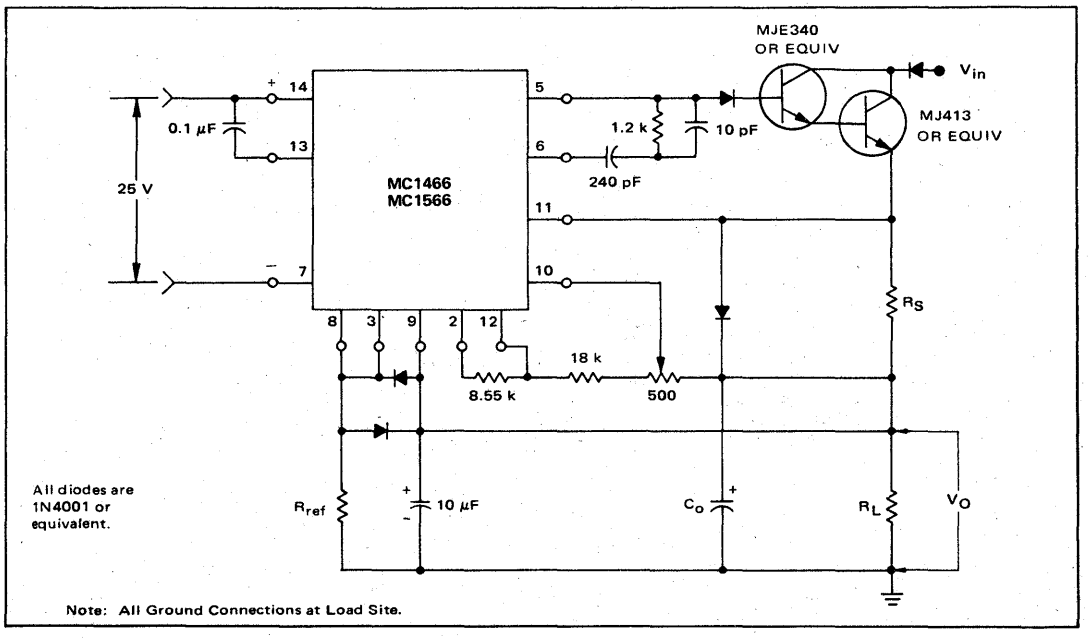


FIGURE 17 – A 0-TO-250 VOLT, 0.1-AMPERE REGULATOR

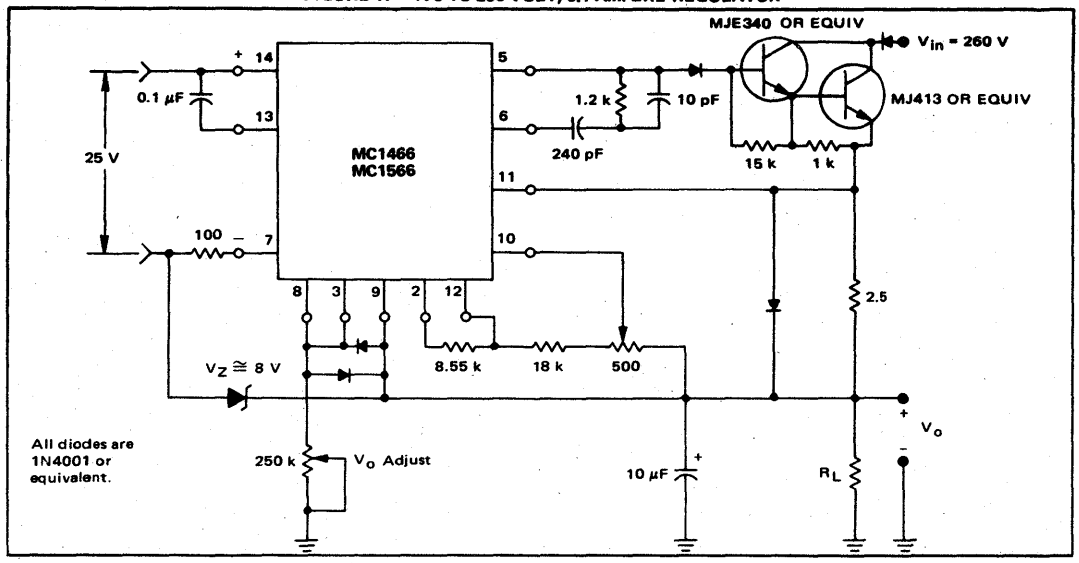
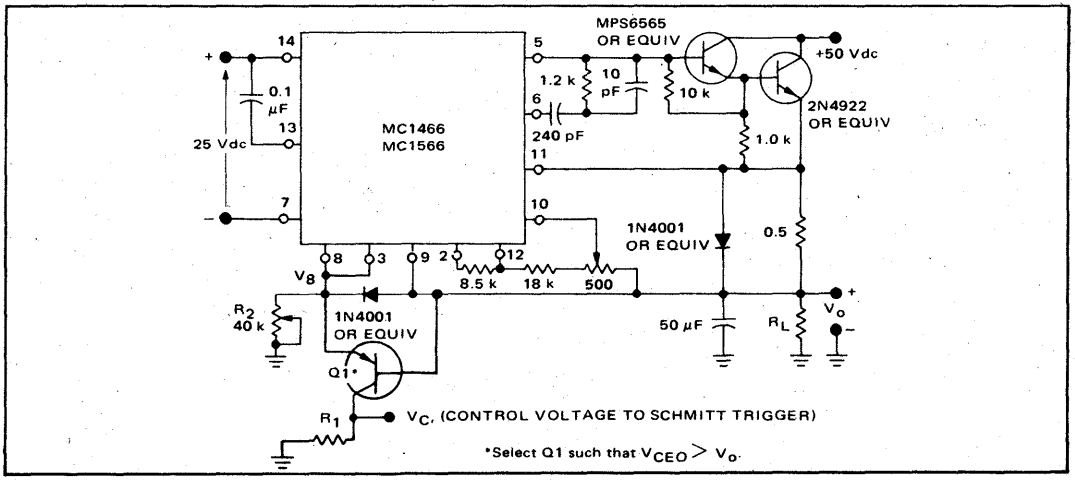


FIGURE 18 – 0-TO--40 Vdc, 0.5-AMPERE REGULATOR WITH MODE INDICATOR



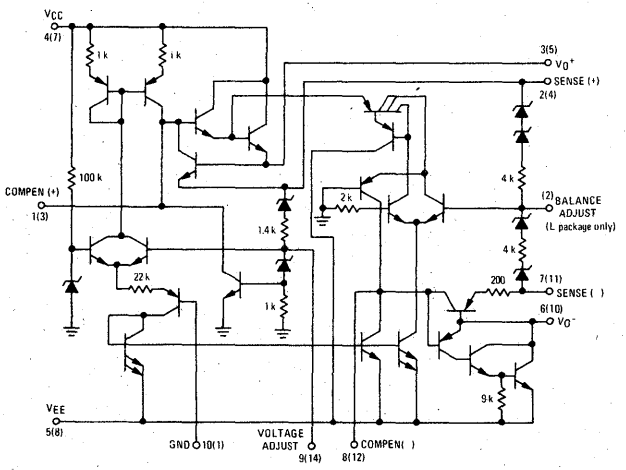
MC1468
MC1568

DUAL ±15-VOLT REGULATOR

The MC1568/MC1468 is a dual polarity tracking regulator designed to provide balanced positive and negative output voltages at currents to 100 mA. Internally, the device is set for ± 15-volt outputs but an external adjustment can be used to change both outputs simultaneously from 8.0 to 20 volts. Input voltages up to ± 30 volts can be used and there is provision for adjustable current limiting. The device is available in three package types to accomodate various power requirements.

- Internally set to ± 15 V Tracking Outputs
- Output Currents to 100 mA
- Outputs Balanced to within 1% (MC1568)
- Line and Load Regulation of 0.06%
- 1% Maximum Output Variation due to Temperature Changes
- Standby Current Drain of 3.0 mA
- Externally Adjustable Current Limit
- Remote Sensing Provisions
- Case is at Ground Potential (R suffix package)

CIRCUIT SCHEMATIC

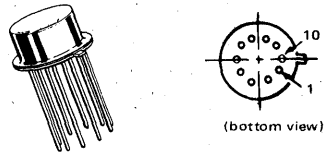


Pin numbers adjacent to terminals are for the G and R suffix packages only. Pin numbers in parentheses are for the L suffix package only.

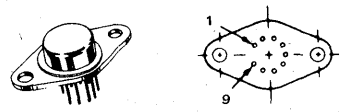
Pin 10 is ground for the G suffix package only. For the R package, the case is ground.

DUAL ±15-VOLT TRACKING REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

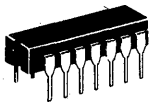


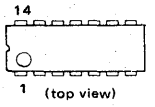
CASE 603C
METAL PACKAGE
TO-100
G SUFFIX



CASE 614
METAL PACKAGE
R SUFFIX

CASE 632
CERAMIC PACKAGE
TO-116
L SUFFIX





ORDERING INFORMATION		
DEVICE	TEMPERATURE RANGE	PACKAGE
MC1468G	0° C to +70° C	Metal Can
MC1468L	0° C to +70° C	Ceramic DIP
MC1468R	0° C to +70° C	Metal Power
MC1568G	−55° C to +125° C	Metal Can
MC1568L	−55° C to +125° C	Ceramic DIP
MC1568R	−55° C to +125° C	Metal Power

MAXIMUM RATINGS (T_C = +25°C unless otherwise noted.)

Rating	Symbol	Value			Unit
Input Voltage	V_{CC}, $\lvert V_{EE}\rvert$	30			Vdc
Peak Load Current	I_{PK}	100			mA
Power Dissipation and Thermal Characteristics		G Package	R Package	L Package	
T_A = +25°C	P_D	0.8	2.4	1.0	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	6.6	28.5	10	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	150	35	100	°C/W
T_C = +25°C	P_D	2.1	9.0	2.5	Watts
Derate above T_C = +25°C	$1/\theta_{JC}$	14	61	20	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	70	17	50	°C/W
Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175			°C
Minimum Short-Circuit Resistance	R_{SC}(min)	4.0			Ohms

OPERATING TEMPERATURE RANGE

Ambient Temperature	T_A		°C
MC1468		0 to +70	
MC1568		-55 to +125	

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 V, V_{EE} = -20 V, C1 = C2 = 1500 pF, C3 = C4 = 1.0 μF, $R_{SC}^+ = R_{SC}^- = 4.0\ \Omega$, $I_L^+ = I_L^- = 0$, T_C = +25°C unless otherwise noted.) (See Figure 1.)

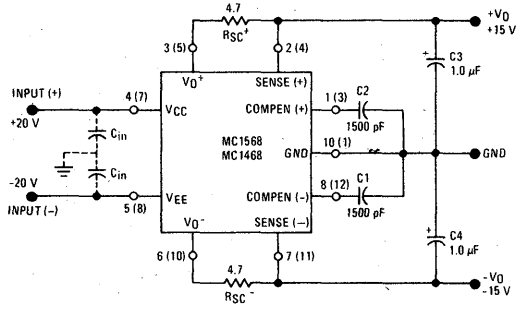
		MC1568			MC1468			
Characteristic	Symbol*	Min	Typ	Max	Min	Typ	Max	Unit
Output Voltage	V_O	±14.8	±15	±15.2	±14.5	±15	±15.5	Vdc
Input Voltage	V_{in}	–	–	±30	–	–	±30	Vdc
Input-Output Voltage Differential	$\lvert V_{in} - V_O\rvert$	2.0	–	–	2.0	–	–	Vdc
Output Voltage Balance	V_{Bal}	–	±50	±150	–	±50	±300	mV
Line Regulation Voltage	Reg_{in}							mV
(V_{in} = 18 V to 30 V)		–	–	10	–	–	10	
(T_{low} ① to T_{high} ②)		–	–	20	–	–	20	
Load Regulation Voltage	Reg_L							mV
(I_L = 0 to 50 mA, T_J = constant)		–	–	10	–	–	10	
(T_A = T_{low} to T_{high})		–	–	30	–	–	30	
Output Voltage Range	V_{OR}							Vdc
L Package (See Figure 4.)		±8.0	–	±20	±8.0	–	±20	
R and G Packages (See Figures 2 and 13.)		±14.5	–	±20	±14.5	–	±20	
Ripple Rejection (f = 120 Hz)	RR	–	75	–	–	75	–	dB
Output Voltage Temperature Stability (T_{low} to T_{high})	$\lvert TSV_O\rvert$	–	0.3	1.0	–	0.3	1.0	%
Short-Circuit Current Limit (R_{SC} = 10 ohms)	I_{SC}	–	60	–	–	60	–	mA
Output Noise Voltage (BW = 100 Hz - 10 kHz)	V_N	–	100	–	–	100	–	μV(RMS)
Positive Standby Current (V_{in} = +30 V)	I_B^+	–	2.4	4.0	–	2.4	4.0	mA
Negative Standby Current (V_{in} = -30 V)	I_B^-	–	1.0	3.0	–	1.0	3.0	mA
Long-Term Stability	$\Delta V_O/\Delta t$	–	0.2	–	–	0.2	–	%/k Hr

① T_{low} = 0°C for MC1468 = -55°C for MC1568

② T_{high} = +70°C for MC1468 = +125°C for MC1568

TYPICAL APPLICATIONS

FIGURE 1 – BASIC 50-mA REGULATOR

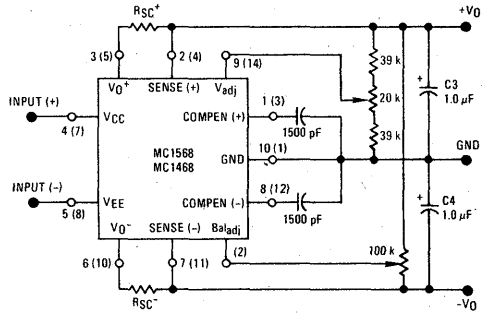


C1 and C2 should be located as close to the device as possible. A 0.1 μF ceramic capacitor (C_{in}) may be required on the input lines if the device is located an appreciable distance from the rectifier filter capacitors.

C3 and C4 may be increased to improve load transient response and to reduce the output noise voltage. At low temperature operation, it may be necessary to bypass C4 with a 0.1 μF ceramic disc capacitor.

FIGURE 2 – VOLTAGE ADJUST AND BALANCE ADJUST CIRCUIT

(14.5 V ⩽ V_{out} ⩽ 20 V)



Balance adjust available in MC1568L, MC1468L ceramic dual in-line package only.

FIGURE 3 – ±1.5-AMPERE REGULATOR

(Short-Circuit Protected, with Proper Heatsinking)
(Metal-Packaged Devices Only, R Suffix)

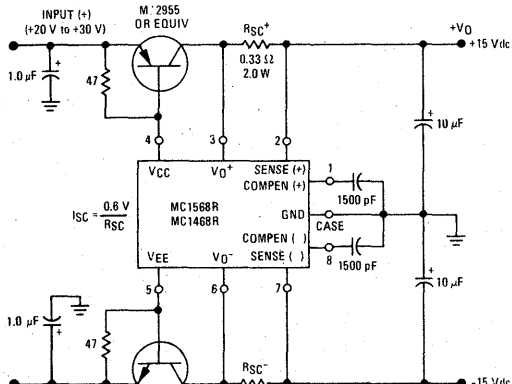
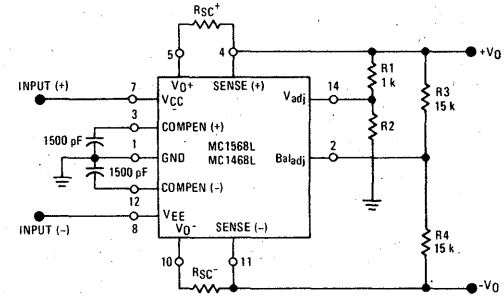


FIGURE 4 – OUTPUT VOLTAGE ADJUSTMENT

FOR 8.0 V ⩽ |±V_O| ⩽ 14.5 V

(Ceramic-Packaged Devices Only, L Suffix.)



The presence of the Bal_{adj} pin 2, on devices housed in the dual in-line package (L suffix) allows the user to adjust the output voltages down to ±8.0 V. The required value of resistor R2 can calculated from

$$R2 = \frac{R1\,R_{int}\,(\phi + V_Z)}{R_{int}\,(V_O - \phi - V_Z) - \phi\,R1}$$

Where: R_{int} = An Internal Resistor = R1 = 1 kΩ
ϕ = 0.68 V
V_Z = 6.6 V

Some common design values are listed below:

±V_O(V)	R2	$T_C V_O$ (%/°C)	I_B + (mA)
14	1.2 k	0.003	10
12	1.8 k	0.022	7.2
10	3.5 k	0.025	5.0
8.0	∞	0.028	2.6

TYPICAL CHARACTERISTICS

(V_{CC} = +20 V, V_{EE} = -20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 5 – LOAD REGULATION

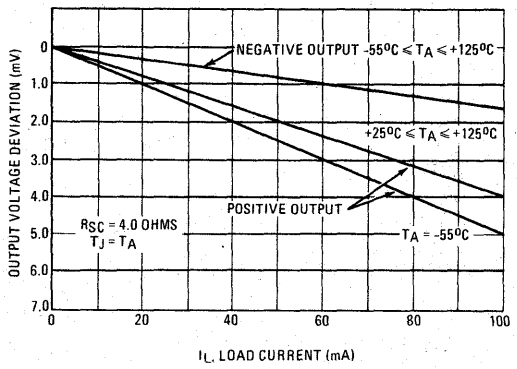


FIGURE 6 – REGULATOR DROPOUT VOLTAGE

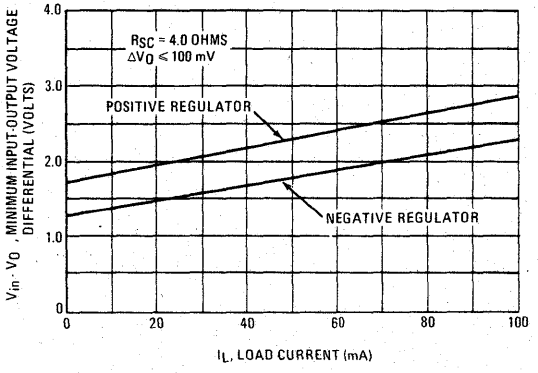


FIGURE 7 – MAXIMUM CURRENT CAPABILITY

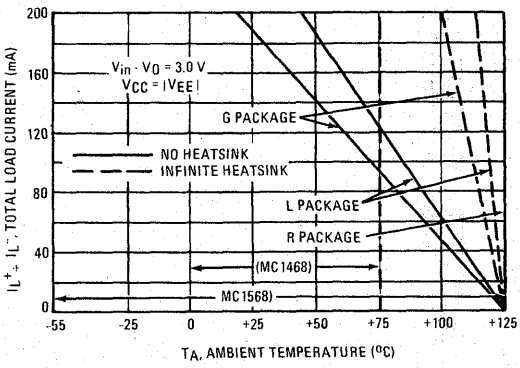


FIGURE 8 – MAXIMUM CURRENT CAPABILITY

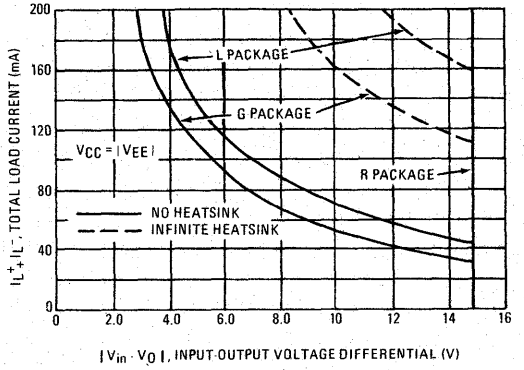


FIGURE 9 – I_{SC} versus R_{SC}

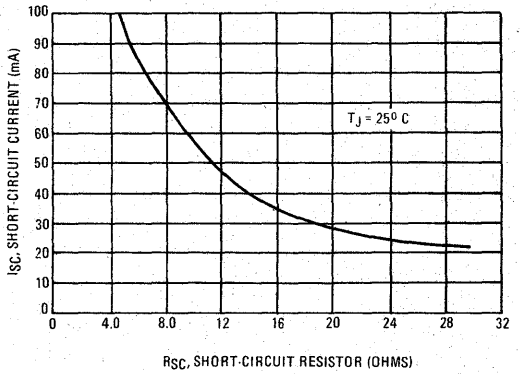
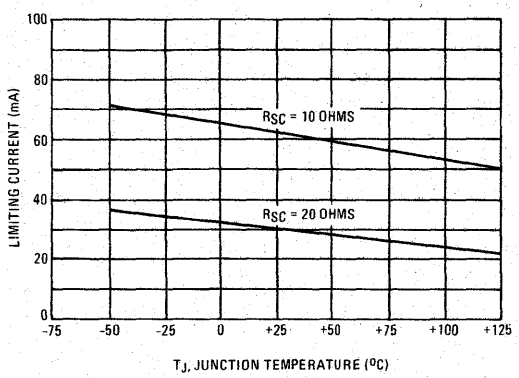


FIGURE 10 – CURRENT-LIMITING CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +20 V, V_{EE} = -20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

4

FIGURE 11 – STANDBY CURRENT DRAIN

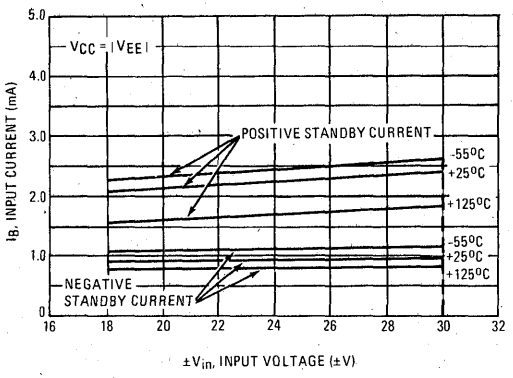


FIGURE 12 – STANDBY CURRENT DRAIN

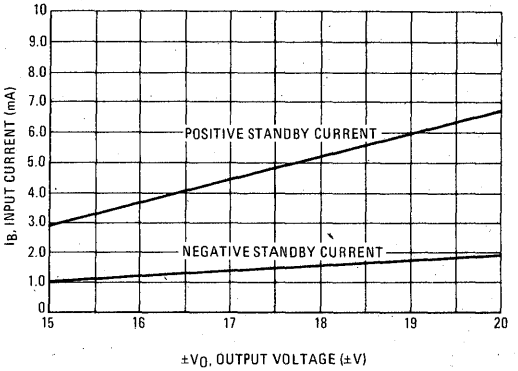


FIGURE 13 – TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE

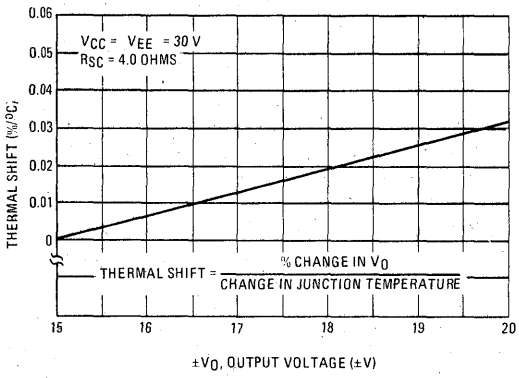


FIGURE 14 – LOAD TRANSIENT RESPONSE

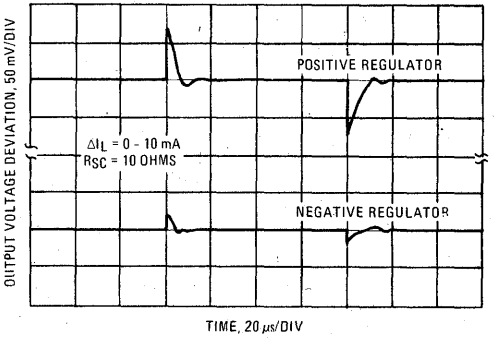


FIGURE 15 – LINE TRANSIENT RESPONSE

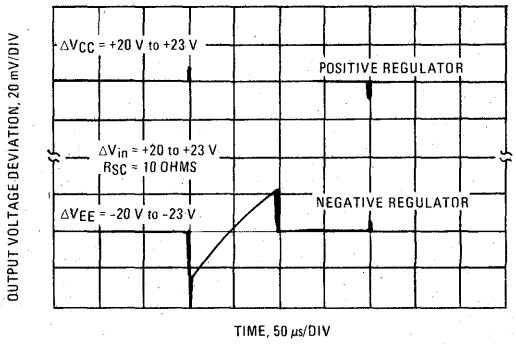
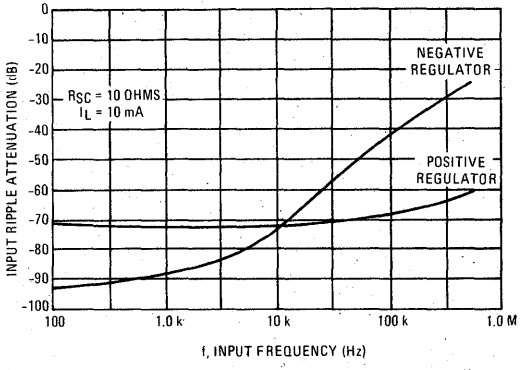


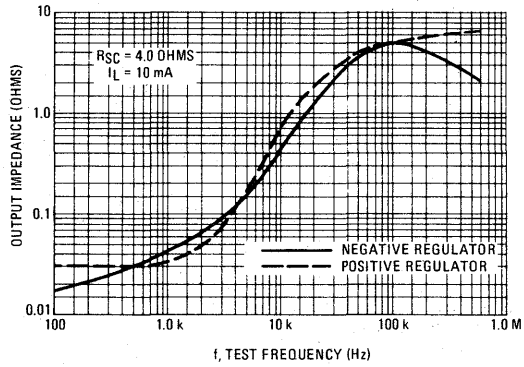
FIGURE 16 – RIPPLE REJECTION



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +20 V, V_{EE} = -20 V, V_O = ±15 V, T_A = +25°C unless otherwise noted.)

FIGURE 17 – OUTPUT IMPEDANCE



MC1469
MC1569

Specifications and Applications Information

MONOLITHIC VOLTAGE REGULATOR

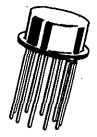
The MC1569/MC1469 is a positive voltage regulator designed to deliver continuous load current up to 500 mAdc. Output voltage is adjustable from 2.5 Vdc to 37 Vdc. The MC1569 is specified for use within the military temperature range (−55 to +125°C) and the MC1469 within the 0 to +70°C temperature range.

For systems requiring a positive regulated voltage, the MC1569 can be used with performance nearly identical to the MC1563 negative voltage regulator. Systems requiring both a positive and negative regulated voltage can use the MC1569 and MC1563 as complementary regulators with a common input ground.

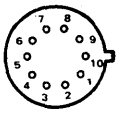
- Electronic "Shut-Down" Control
- Excellent Load Regulation (Low Output Impedance — 20 milliohms typ)
- High Power Capability: up to 17.5 Watts
- Excellent Temperature Stability: ±0.002 %/°C typ
- High Ripple Rejection: 0.002 %/V typ

POSITIVE VOLTAGE REGULATOR INTEGRATED CIRCUIT

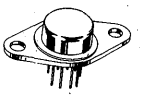
SILICON NONOLITHIC
EPITAXIAL PASSIVATED



CASE 603
METAL PACKAGE
G SUFFIX



(Bottom View)



CASE 614
METAL PACKAGE
R SUFFIX

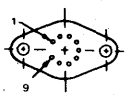
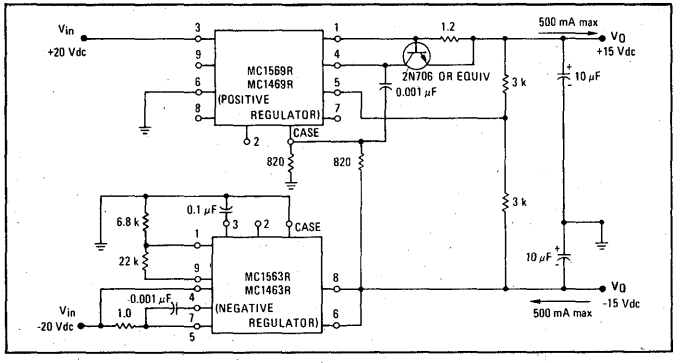


FIGURE 1 — ±15 V, ±400 mA COMPLEMENTARY TRACKING VOLTAGE REGULATOR



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC1469G	0° C to +70°C	Metal Can
MC1469R	0° C to +70° C	Metal Power
MC1569G	−55° C to +125° C	Metal Can
MC1569R	−55° C to +125° C	Metal Power

FIGURE 2 — TYPICAL CIRCUIT CONNECTION
(3.5 ≤ V_O ≤ 37 Vdc, 1 ≤ I_L ≤ 500 mA)

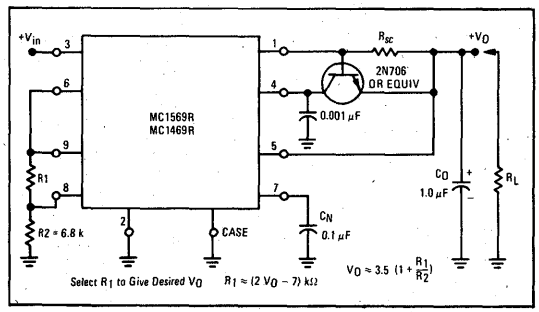
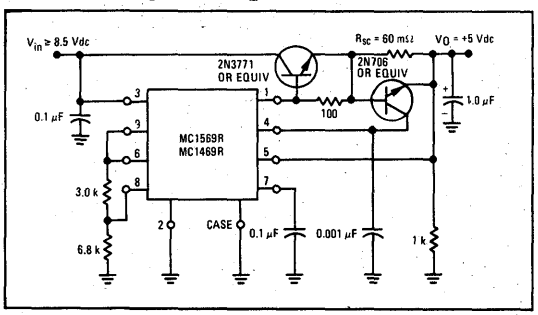


FIGURE 3 — TYPICAL NPN CURRENT BOOST CONNECTION
(V_O = 5.0 Vdc, I_L = 10 Adc [max])



MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Rating	Symbol	Value		Unit
Input Voltage MC1469 MC1569	V_{in}	35 40		Vdc
		G Package	R Package	
Peak Load Current	I_{PK}	250	600	mA
Current, Pin 2 Current, Pin 9	$I_{pin\ 2}$ $I_{pin\ 9}$	10 5.0	10 5.0	mA
Power Dissipation and Thermal Characteristics				
T_A = +25°C	P_D	0.68	3.0	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	5.44	24	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	184	41.6	°C/W
T_C = +25°C	P_D	1.8	14	Watts
Derate above T_C = +25°C	$1/\theta_{JC}$	14.4	140	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	69.4	7.15	°C/W
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150		°C

OPERATING TEMPERATURE RANGE

Ambient Temperature MC1469 MC1569	T_A	0 to +70 -55 to +125	°C

ELECTRICAL CHARACTERISTICS

(T_C = +25°C unless otherwise noted) (Load Current = 100 mA for "R" Package device, = 10 mA for "G" Package device, unless otherwise noted)

Characteristic	Fig.	Note	Symbol	MC1569 Min	MC1569 Typ	MC1569 Max	MC1469 Min	MC1469 Typ	MC1469 Max	Unit
Input Voltage (T_A = T_{low} ① to T_{high} ②)	4	1	V_{in}	8.5	–	40	9.0	–	35	Vdc
Output Voltage Range	4,5		V_O	2.5	–	37	2.5	–	32	Vdc
Reference Voltage (Pin 8 to Ground, V_{in} = 15 V	4		V_{ref}	3.4	3.5	3.6	3.2	3.5	3.8	Vdc
Minimum Input-Output Voltage Differential (R_{sc} = 0)	4	2	$V_{in} - V_O$	–	2.1	2.7	–	2.1	3.0	Vdc
Bias Current (V_{in} = 15 V) (I_L = 1.0 mAdc, R_2 = 6.8 k ohms, I_{IB} = I_{in} - I_L)	4		I_{IB}	–	4.0	9.0	–	5.0	12	mAdc
Output Noise (C_N = 0.1 μF, f = 10 Hz to 5.0 MHz)	4		v_N	–	0.150	–	–	0.150	–	mV(rms)
Temperature Coefficient of Output Voltage	4	3	TCV_O	–	±0.002	–	–	±0.002	–	%/°C
Operating Load Current Range ($R_{sc} \leq$ 0.3 ohms) R Package ($R_{sc} \leq$ 2.0 ohms) G Package	4		I_L	1.0 1.0	– –	500 200	1.0 1.0	– –	500 200	mAdc
Input Regulation	6	4	Reg_{in}	–	0.002	0.015	–	0.003	0.030	%/V_O
Load Regulation (T_J = Constant [1.0 mA$\leq I_L \leq$20 mA]) (T_C = +25°C [1.0 mA$\leq I_L \leq$50 mA]) R Package G Package	7	5	Reg_{load}	– – –	0.4 0.005 0.01	1.6 0.05 0.13	– – –	0.7 0.005 0.01	2.4 0.05 0.13	mV %
Output Impedance (C_C = 0.001 μF, R_{sc} = 1.0 ohm, f = 1.0 kHz, V_{in} = +14 Vdc, V_O = +10 Vdc)	8	6	z_o	–	20	–	–	35	–	milliohms
Shutdown Current (V_{in} = +35 Vdc)	9		I_{sd}	–	70	150	–	140	500	μAdc

① T_{low} = 0°C for MC1469 = -55°C for MC1569

② T_{high} = +70° C for MC1469 = +125°C for MC1569

Note 1. "Minimum Input Voltage" is the minimum "total instantaneous input voltage" required to properly bias the internal zener reference diode. For output voltages greater than approximately 5.5 Vdc the minimum "total instantaneous input voltage" must increase to the extent that it will always exceed the output voltage by at least the "input-output voltage differential".

Note 2. This parameter states that the MC1569/MC1469 will regulate properly with the input-output voltage differential ($V_{in} - V_O$) as low as 2.7 Vdc and 3.0 Vdc respectively. Typical units will regulate properly with ($V_{in} - V_O$) as low as 2.1 Vdc as shown in the typical column. (See Figure 21.)

Note 3. "Temperature Coefficient of Output Voltage" is defined as:

$$\text{MC1569, } TCV_O = \frac{\pm (V_O \text{ max} - V_O \text{ min}) (100)}{(180^\circ\text{C}) (V_O @ 25^\circ\text{C})} = \%/^\circ\text{C}$$

$$\text{MC1469, } TCV_O = \frac{\pm (V_O \text{ max} - V_O \text{ min}) (100)}{(75^\circ\text{C}) (V_O @ 25^\circ\text{C})} = \%/^\circ\text{C}$$

The output-voltage adjusting resistors (R1 and R2) must have matched temperature characteristics in order to maintain a constant ratio independent of temperature.

Note 4. Input regulation is the percentage change in output voltage per volt change in the input voltage and is expressed as

$$\text{Input Regulation} = \frac{v_o}{V_O (v_{in})} 100 \ (\%/V_O),$$

where v_o is the change in the output voltage V_O for the input change v_{in}.

The following example illustrates how to compute maximum output voltage change for the conditions given:

$$\text{Reg}_{in} = 0.015 \ \%/V_O$$
$$V_O = 10 \text{ Vdc}$$
$$v_{in} = 1.0 \text{ V(rms)}$$
$$v_o = \frac{(\text{Reg}_{in}) (v_{in}) (V_O)}{100}$$
$$= \frac{(0.015) (1.0) (10)}{100}$$
$$= 0.0015 \text{ V(rms)}$$

Note 5. Load regulation is specified for small ($\leqslant +17^\circ\text{C}$) changes in junction temperature. Temperature drift effect must be taken into account separately for conditions of high junction temperature changes due to the thermal feedback that exists on the monolithic chip.

$$\text{Load Regulation} = \frac{[V_O|I_L = 1.0 \text{ mA}] - [V_O|I_L = 50 \text{ mA}]}{V_O \, | I_L = 1.0 \text{ mA}} \times 100$$

TEST CIRCUITS

FIGURE 4 – CONNECTION FOR $V_O \geqslant 3.5$ Vdc

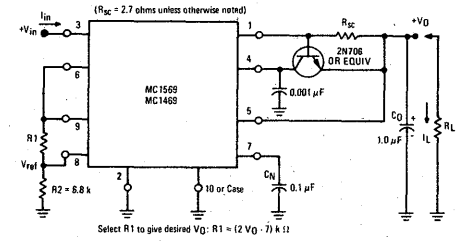


FIGURE 5 – CONNECTION FOR 2.5 Vdc $\geqslant V_O \leqslant$ 3.5 Vdc

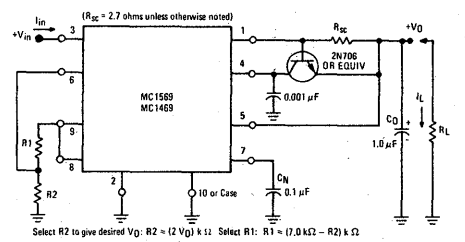


FIGURE 6 – INPUT REGULATION

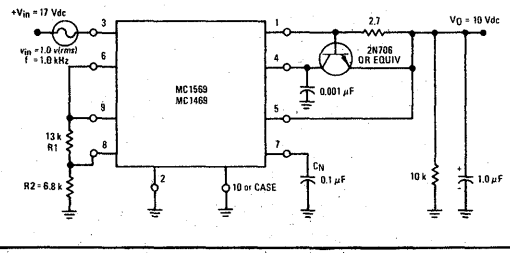


FIGURE 7 – LOAD REGULATION

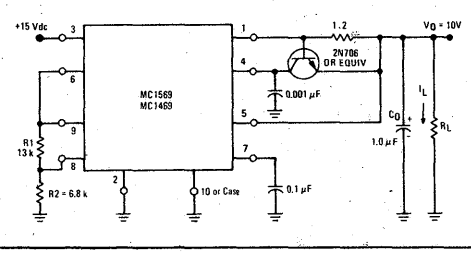


FIGURE 8 – OUTPUT IMPEDANCE

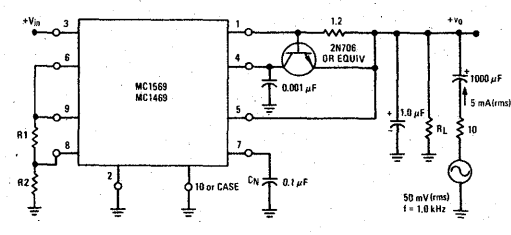
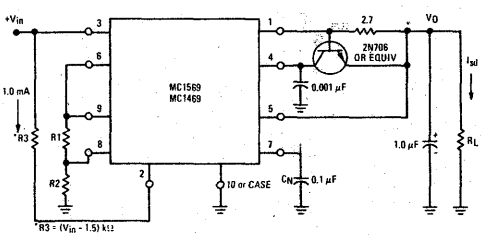


FIGURE 9 – SHUTDOWN CURRENT



GENERAL DESIGN INFORMATION

1. Output Voltage, V_O
   a) For $V_O \geq 3.5$ Vdc – Output voltage is set by resistors R1 and R2 (see Figure 4). Set R2 = 6.8 k ohms and determine R1 from the graph of Figure 10 or from the equation:
   $$R1 \approx (2\ V_O - 7)\ k\Omega$$
   b) For $2.5 \leq V_O \leq 3.5$ Vdc – Output voltage is set by resistors R1 and R2 (see Figure 5). Resistors R1 and R2 can be determined from the graph of Figure 11 or from the equations:
   $$R2 \approx 2\ (V_O)\ k\Omega$$
   $$R1 \approx (7\ k\Omega - R2)\ k\Omega$$
   c) Output voltage, V_O, is determined by the ratio of R1 and R2, therefore optimum temperature performance can be achieved if R1 and R2 have the same temperature coefficient.
   d) Output voltage can be varied by making R1 adjustable as shown in Figure 43.
   e) If V_O = 3.5 Vdc (to supply MRTL* for example), tie pins 6, 8 and 9 together. R1 and R2 are not needed in this case.
2. Short Circuit Current, I_{sc}
   Short Circuit Current, I_{sc}, is determined by R_{sc}. R_{sc} may be chosen with the aid of Figure 12 or the expression:
   $$R_{sc} \approx \frac{0.6}{I_{sc}}\ \text{ohm}$$
   where I_{sc} is measured in amperes. This expression is also valid when current is boosted as shown in Figure 2.
3. Compensation, C_C
   A 0.001 μF capacitor, C_C, from pin 4 to ground will provide adequate compensation in most applications, with or without current boost. Smaller values of C_C will reduce stability and larger values of C_C will degrade pulse response and output impedance versus frequency. The physical location of C_C should be close to the MC1569/MC1469 with short lead lengths.
4. Noise Filter Capacitor, C_N
   A 0.1 μF capacitor, C_N, from pin 7 to ground will typically reduce the output noise voltage to 150 μV(rms). The value of C_N can be increased or decreased, depending on the noise voltage requirements of a particular application. A minimum value of 0.001 μF is recommended.
5. Output Capacitor, C_O
   The value of C_O should be at least 1.0 μF in order to provide good stability. The maximum value recommended is a function of current limit resistor R_{sc}:
   $$C_O\ \text{max} \approx \frac{250\ \mu F}{R_{sc}}$$
   where R_{sc} is measured in ohms. Values of C_O greater than this will degrade the pulse response characteristics and increase the settling time.
6. Shut-Down Control
   One method of turning "OFF" the regulator is to apply a dc voltage at pin 2. This control can be used to eliminate power consumption by circuit loads which can be put in "standby" mode. Examples include, an ac or dc "squelch" control for communications circuits, and a dissipation control to protect the regulator under sustained output short-circuiting. As the magnitude of the input-threshold voltage at Pin 2 depends directly upon the junction temperature of the integrated circuit chip, a fixed dc voltage at Pin 2 will cause automatic shut-down for high junction temperatures. This will protect the chip, independent of the heat sinking used, the ambient temperature, or the input or output voltage levels. Standard Logic levels of MRTL, MDTL* or MTTL* can also be used to turn the regulator "ON" or "OFF".
7. Remote Sensing
   The connection to pin 5 can be made with a separate lead direct to the load. Thus, "remote sensing" can be achieved and the effect of undesired impedances (including that of the milliammeter used to measure I_L) on z_o can be greatly reduced.

FIGURE 10 – R1 versus V_O
($V_O \geq 3.5$ Vdc, See Figure 4)

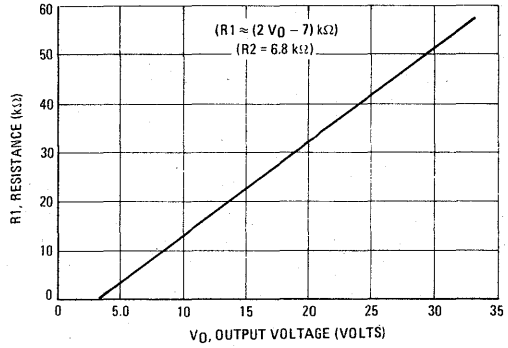


FIGURE 11 – R1 and R2 versus V_O
($2.5 \leq V_O \leq 3.5$ Vdc, See Figure 5)

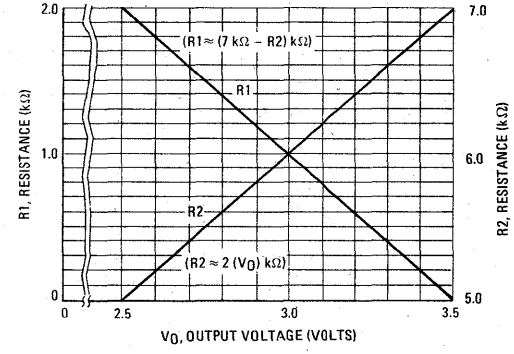
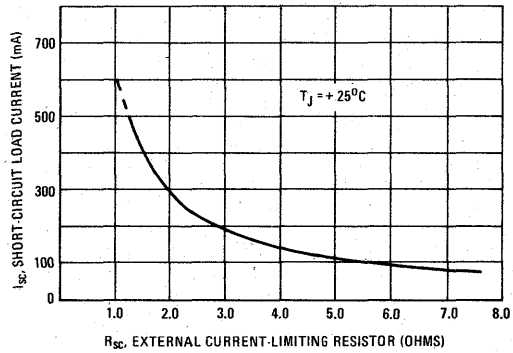


FIGURE 12 – I_{sc} versus R_{sc}



TYPICAL CHARACTERISTICS

Unless otherwise noted: $C_N = 0.1\ \mu F$, $C_C = 0.001\ \mu F$, $C_O = 1.0\ \mu F$, $T_C = +25^\circ C$, V_{in} nom = +9.0 Vdc, V_O nom = +5.0 Vdc, $I_L > 200$ mA for R package only.

FIGURE 13 – DEPENDENCE OF OUTPUT IMPEDANCE ON OUTPUT VOLTAGE

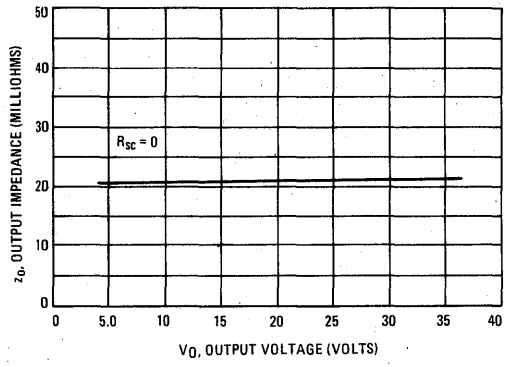


FIGURE 14 – OUTPUT IMPEDANCE versus R_{sc}

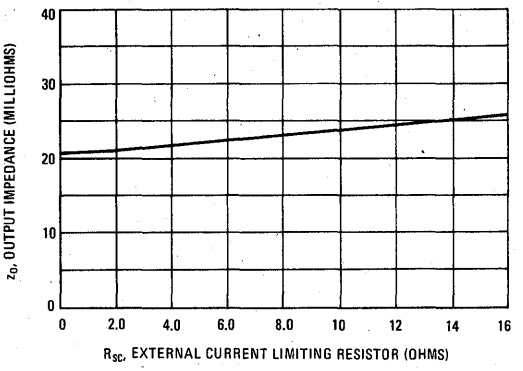


FIGURE 15 – FREQUENCY DEPENDENCE OF INPUT REGULATION, $C_O = 10\ \mu F$

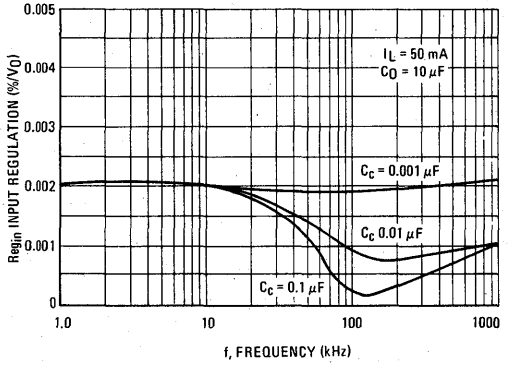


FIGURE 16 – FREQUENCY DEPENDENCE OF INPUT REGULATION, $C_O = 2.0\ \mu F$

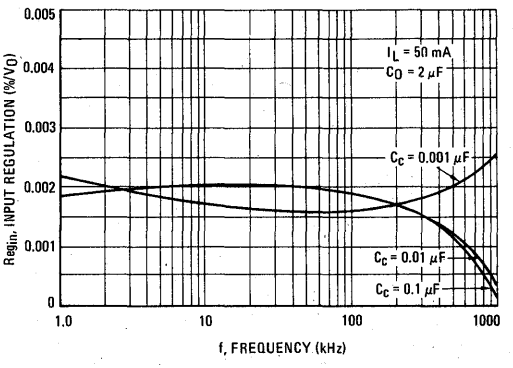


FIGURE 17 – CURRENT-LIMITING CHARACTERISTICS

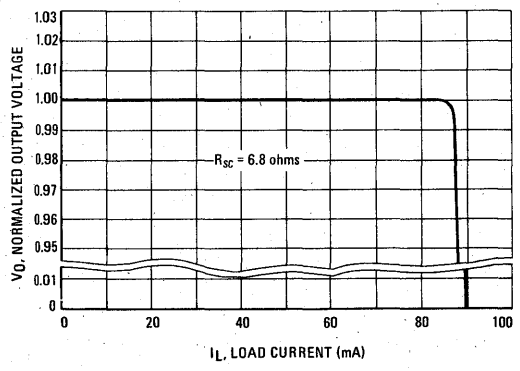
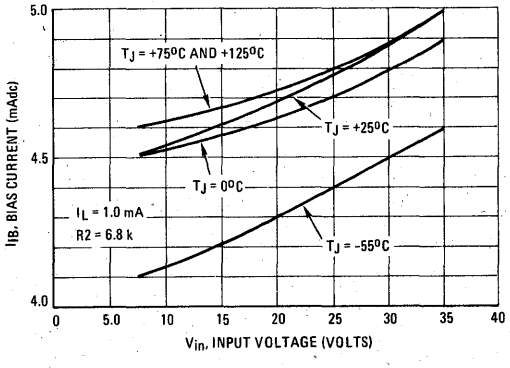


FIGURE 18 – BIAS CURRENT versus INPUT VOLTAGE



TYPICAL CHARACTERISTICS (continued)

Unless otherwise noted: $C_N = 0.1\ \mu F$, $C_c = 0.001\ \mu F$, $C_O = 1.0\ \mu F$, $T_C = +25°C$, V_{in} nom = +9.0 Vdc, V_O nom = +5.0 Vdc, $I_L > 200$ mA for R package only.

FIGURE 19 – EFFECT OF LOAD CURRENT ON INPUT-OUTPUT VOLTAGE DIFFERENTIAL

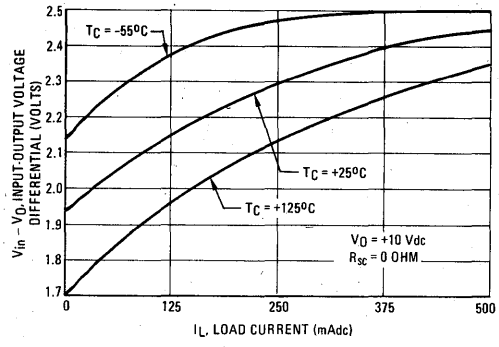


FIGURE 20 – EFFECT OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL ON INPUT REGULATION

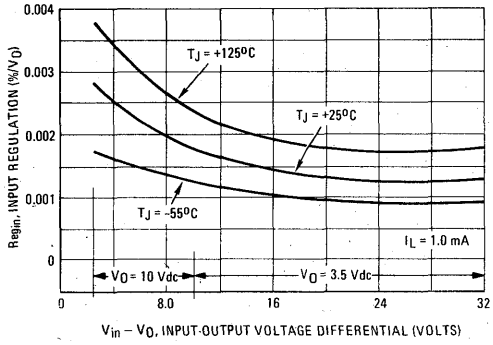


FIGURE 21 – INPUT TRANSIENT RESPONSE

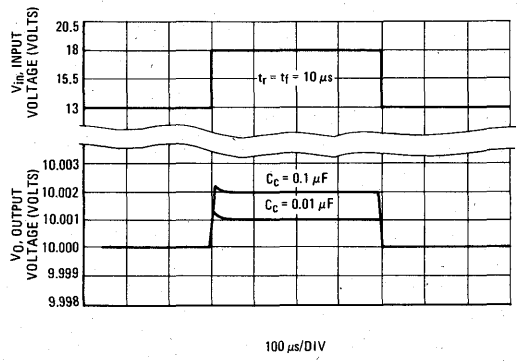


FIGURE 22 – TEMPERATURE DEPENDENCE OF SHORT-CIRCUIT LOAD CURRENT

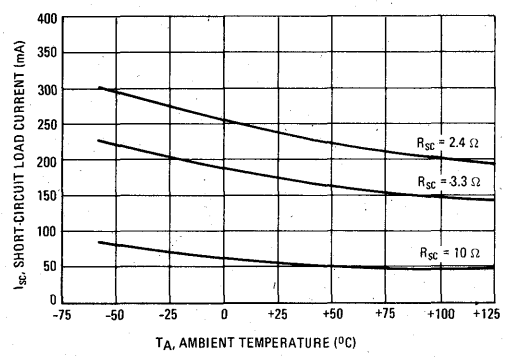


FIGURE 23 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE, C_O = 10 μF

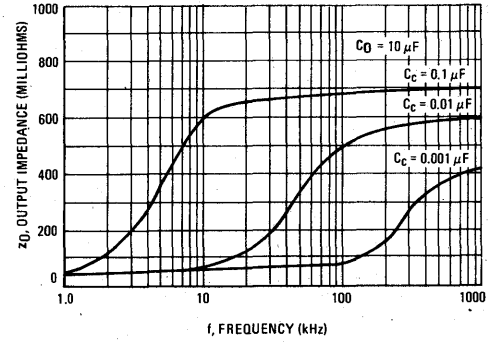
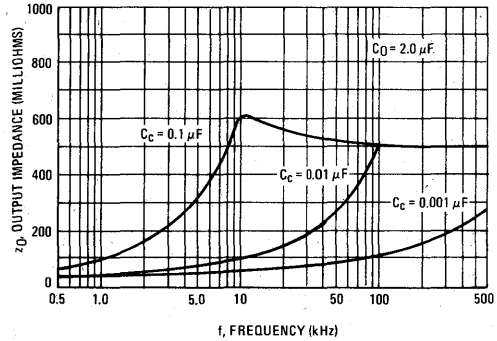


FIGURE 24 – FREQUENCY DEPENDENCE OF OUTPUT IMPEDANCE, C_O = 2.0 μF



OPERATIONS AND APPLICATIONS

This section describes the operation and design of the MC1569 positive voltage regulator and also provides information on useful applications.

SUBJECT SEQUENCE

Theory of Operation	Shutdown Techniques	Thermal Shutdown
NPN Current Boosting	Voltage Boosting	Thermal Considerations
PNP Current Boosting	Remote Sensing	Latch-Up
Switching Regulator	An Adjustable-Zero-Temperature-Coefficient Voltage Source	
Positive and Negative Power Supplies		

4

THEORY OF OPERATION

The usual series voltage regulator shown in Figure 25, consists of a reference voltage, an error amplifier, and a series control element. The error amplifier compares the output voltage with the reference voltage and adjusts the output accordingly until the error is essentially zero. For applications requiring output voltages larger than the reference, there are two options. The first is to use a resistive divider across the output and compare only a fraction of the output voltage to the reference. This approach suffers from reduced feedback to the error amplifier due to the attenuation of the resistive divider. This degrades load regulation especially at high voltage levels.

The alternative is to eliminate the resistive divider and to shift the reference voltage instead. To accomplish this, another amplifier is employed to amplify (or level shift) the reference voltage using an operational amplifier as shown in Figure 26. The gain-determining resistors may be external, enabling a wide range of output voltages. This is exactly the same approach used in the first option. That is, the output is being resistively divided to match the reference voltage. There is however, one big difference in that the output of this "regulator" is driving the input of another regulator (the error amplifier). The output of the reference amplifier has a relatively low impedance as compared to the input impedance of the error amplifier. Changes in the load of the output of the error amplifier are buffered to the extent that they have virtually no effect on the reference amplifier. If the feedback resistors are external (as they are on the MC1569) a wide range of reference voltages can be established.

The error amplifier can now be operated at unity gain to provide excellent regulation. In fact, this "regulator-within-a-regulator" concept permits the load regulation to be specified in terms of output impedance rather than as some percentage change of the output voltage. This approach was used in the design of the MC1569 positive-voltage regulator.

FIGURE 25 – SERIES VOLTAGE REGULATOR

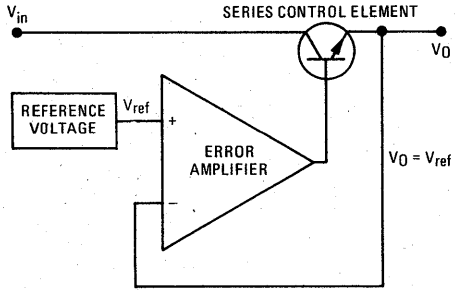


FIGURE 26 – THE "REGULATOR-WITHIN-A-REGULATOR" APPROACH

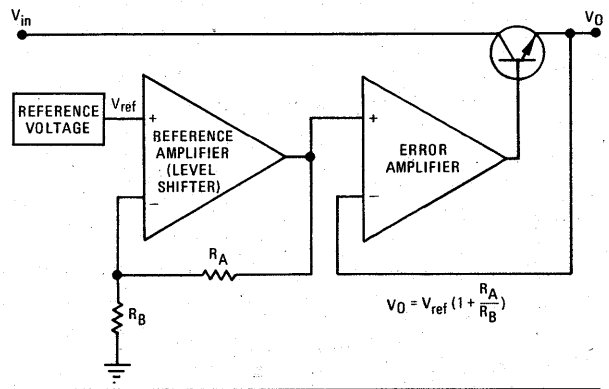
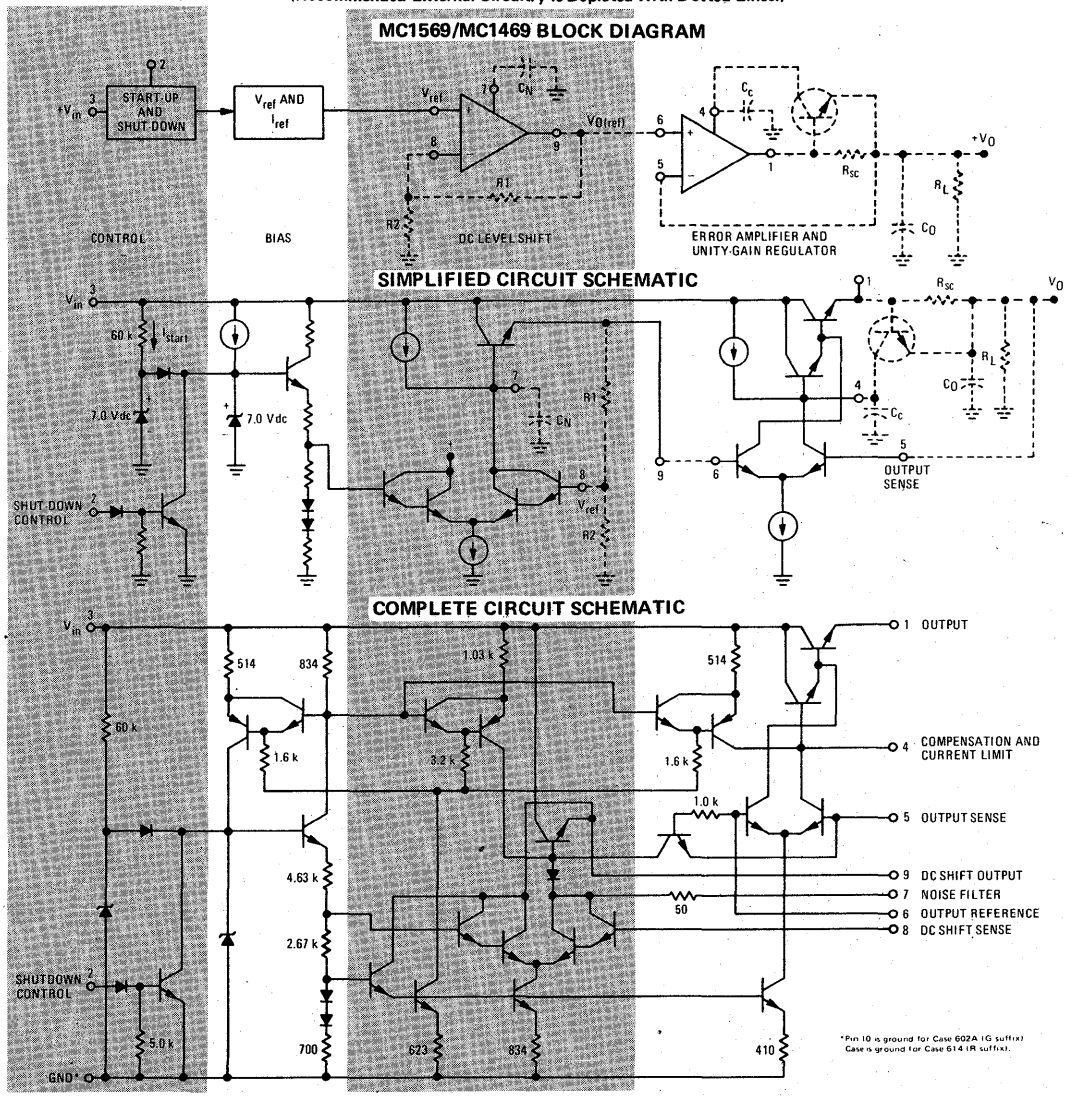


FIGURE 27
(Recommended External Circuitry is Depicted With Dotted Lines.)



MC1569 Operation

Figure 27 shows the MC1569 Regulator block diagram, simplified schematic, and complete schematic. The four basic sections of the regulator are: Control, Bias, DC Level Shift, and Output (unity gain) Regulator. Each section is detailed in the following paragraphs.

Control

The control section involves two basic functions, start-up and shutdown. A start-up function is required since the biasing is essentially independent of the unregulated input voltage. It makes use of two zener diodes having the same breakdown voltage. A first or auxiliary zener is driven directly from the input voltage line through a resistor (60 kΩ) and permits the regulator to initially achieve the desired bias conditions. This permits the second, or reference zener to be driven from a current source. When the reference zener enters breakdown, the auxiliary zener is isolated from the rest of the regulator circuitry by a diode disconnect technique. This is necessary to keep the added noise and ripple of the auxiliary zener from degrading the performance of the regulator.

The shutdown control consists of an NPN transistor across the reference zener diode. When this transistor is turned "ON", via pin 2, the reference voltage is reduced to essentially zero volts and the regulator is forced to shutdown. During shutdown the current drain of the complete IC regulator drops to $V_{in}/60$ kΩ or 500 μA for a 30 V input.

Bias

A zener diode is the main reference element and forms the heart of the bias circuitry. Its positive temperature coefficient is balanced by the negative temperature coefficients of forward biased diodes in a ratio determined by the resistors in the diode string. The result is a reference voltage of approximately 3.5 Vdc with a typical temperature coefficient of 0.002 %/°C. In addition, this circuit also provides a reference current which is used to bias all current sources in the remaining regulator circuitry.

DC Level Shift

The reference voltage is used as the input to a Darlington differential amplifier. The gain of this amplifier is quite high and it therefore may be considered to function as a conventional operational amplifier. Consequently, negative feedback can be employed using two external resistors (R1 and R2) to set the closed-loop gain and to boost the reference voltage to the desired output voltage. A capacitor, C_N, is introduced externally into the level shift network (via pin 7) to stabilize the amplifier and to filter the zener noise. The recommended value for this capacitor is 0.1 μF and should have a voltage rating in excess of the desired output voltage. Smaller capacitors (0.001 μF minimum) may be used but will cause a slight increase in output noise. Larger values of C_N will reduce the noise as well as delay the start-up of the regulator.

Output Regulator

The output of the level shift amplifier (pin 9) is fed to the noninverting input (pin 6) of the output error amplifier. The inverting input to this amplifier is the Output Sense connection (pin 5) of the regulator. A Darlington connected NPN power transistor is used to handle the load current. The short-circuit current limiting resistor, R_{sc}, is connected in the emitter of this transistor to sample the full load current. By placing an external low-level NPN transistor across R_{sc} as shown in Figure 27, output current can be limited to a predetermined value:

$$I_L \text{ max} \approx \frac{0.6}{R_{sc}} \text{ or } R_{sc} = \frac{0.6}{I_L \text{ max}}$$

where I_L max is the maximum load current (amperes) and R_{sc} is the value of the current limiting resistor (ohms).

Stability and Compensation

As has been seen, the MC1569 employs two amplifiers, each using negative feedback. This implies the possibility of instability, due to excessive phase shift at high frequencies. Since the error amplifier is normally used at unity gain (the worst case for stability) a high impedance node is brought out for compensation. For normal operation, a capacitor is connected between this point (pin 4) and ground. The recommended value of 0.001 μF will insure stability and still provide acceptable transient response (see Figure 28, A and B). It is also necessary to use an output capacitor, C_O (typically 1.0 μF) from the output, V_O, to ground. When an external transistor is used to boost the current, C_O = 1.0 μF is also recommended (see Figure 2).

FIGURE 28A – LOAD TRANSIENT RESPONSE

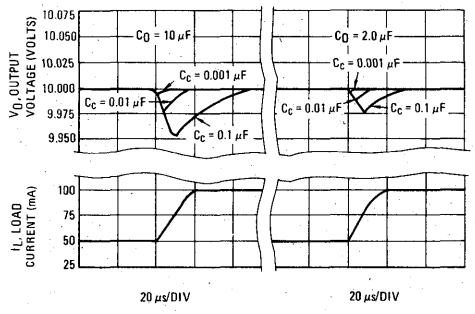
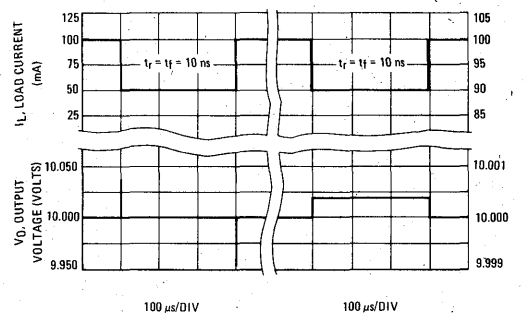


FIGURE 28B – LOAD TRANSIENT RESPONSE



TYPICAL NPN CURRENT BOOST CONNECTIONS

FIGURE 29A – 5 VOLT 5-AMPERE REGULATOR

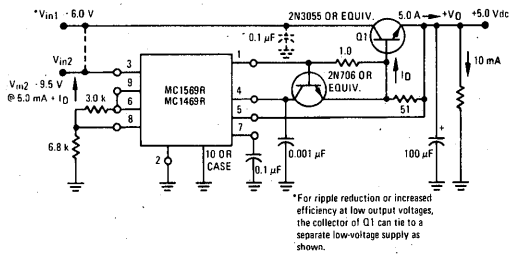


FIGURE 29B – 5-VOLT 5-AMPERE REGULATOR

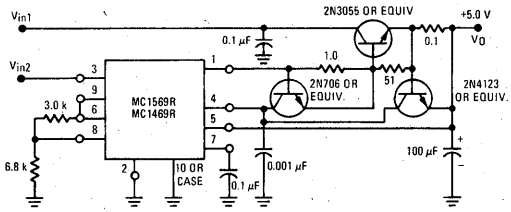
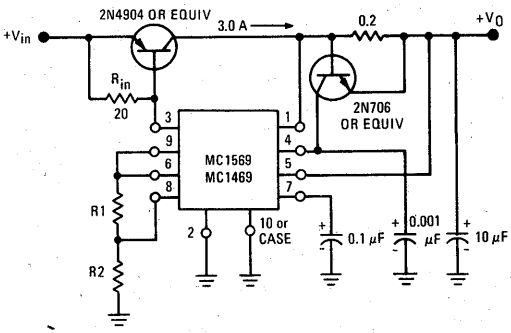


FIGURE 30 – PNP CURRENT BOOST CONNECTION



NPN CURRENT BOOSTING

For applications requiring more than 500 mA of load current, or for minimizing voltage variations due to temperature changes in the IC regulator arising from changes of the internal power dissipation, the NPN current-boost circuits of Figure 3 or 29 are recommended. The transistor shown in Figure 29A, the 2N3055 can supply currents to 5.0 amperes (subject, of course, to the safe area limitations). To improve the efficiency of the NPN boost configuration, particularly for small output voltages, the circuit of Figure 29 is recommended. An auxiliary 9.5-volt supply is used to power the IC regulator and the heavy load current is obtained from a second supply of lower voltage. For the 5.0 ampere regulator of Figure 29 this represents a savings of 17.5 watts when compared with operating the regulator from the single 9.5 V supply. It can supply current to 5.0 amperes while requiring an input voltage to the collector of the pass transistor of 6.0 volts minimum. The pass transistor is limited to 5.0 amperes by the added short-circuit current network in its emitter (R_{SC}), (Figure 29B).

PNP CURRENT BOOSTING

A typical PNP current boost circuit is shown in Figure 30. Voltages from 2.5 Vdc to 37 Vdc and currents of many amperes can be obtained with this circuit.

Since the PNP transistor must not be turned on by the MC1569 bias current (I_{IB}) the resistor R_{in} must meet the following condition

$$R_{in} < \frac{V_{BE}}{I_{IB}}$$

where V_{BE} is the base-to-emitter voltage required to turn on the PNP pass transistor, (typically 0.6 Vdc for silicon and 0.2 Vdc for germanium).

For germanium pass transistors, a silicon diode may be placed in series with the emitter to provide an additional voltage drop. This allows a larger value of R_{in} than would be possible if the diode were omitted. The diode will, however, be required to carry the maximum load current.

SELF-OSCILLATING SWITCHING REGULATOR

In all of the current boosting circuits shown thus far it has been assumed that the input-output voltage differential can be minimized to obtain maximum efficiency in both the external pass element as well as the MC1569. This may not be possible in applications where only a single supply voltage is available and high current levels preclude zener diode pre-regulating approaches. In such applications a switching-mode voltage regulator is highly desirable since the pass device is either ON or OFF. The theoretical efficiency of an ideal switching regulator is 100%. Realizable efficiencies of 90% are within the realm of possibility thus obviating the need for large power dissipating components. The output voltage will contain a ripple component; however, this can be made quite small if the switching frequency is made relatively high so filtering techniques are effective. Figure 31 shows a functional diagram for a self-oscillating voltage regulator. The comparator-driver will sense the voltage across the inductor, this voltage being related to the load current, I_L, by

$$L \frac{dI_L}{dt} = V.$$

For a first approximation this can be assumed to be a linear relationship.

Initially, V_O will be low and Q1 will be ON. The voltage at the non-inverting input will approach $\beta_1 V_{in}$, when:

$$\beta_1 V_{in} = \frac{V_{ref} R_a}{R_a + R_b} + \frac{V_c R_b}{R_a + R_b}.$$

When this output voltage is reached the comparator will switch, turning Q1 OFF. The diode, CR1, will now become forward biased and will supply a path for the inductor current. This current and the sense voltage will start to decrease until the output voltage reaches

$$\beta_2 V_{in} = \frac{V_{ref} R_a}{R_a + R_b}$$

where the comparator will again switch turning Q1 ON, and the cycle repeats. Thus the output voltage is approximately V_{ref} plus a ripple component.

The frequency of oscillation can be shown to be

$$f = \frac{V_O (V_{in} - V_O)}{L V_C I(max) - I_O)} \quad (1)$$

where

I (max) = The maximum value of inductor current

I_O = The minimum inductor current.

Normally this frequency will be in the range of approximately 2 kHz to 6 kHz. In this range, inductor values can be small and are compatible with the switching times of the pass transistor and diode. The switching time of the comparator is quite fast since positive feedback aids both turn-on and turn-off times. The limiting factors are the diode and pass transistor rise and fall times which should be quite fast or efficiency will suffer.

Figure 32 shows a self oscillating switching regulator which in many respects is similar to the PNP current boost previously discussed. The 6.8 kΩ resistor in conjunction with R1 sets the reference voltage, V_{ref}. Q1 and CR1 are selected for fast switching times as well as the necessary power dissipation ratings. Since a linear inductor is assumed, the inductor cannot be allowed to saturate at maximum load currents and should be chosen accordingly. If core saturation does occur, peak transistor and diode currents will be large and power dissipation will increase.

FIGURE 31 – BASIC SELF-OSCILLATING SWITCHING REGULATOR

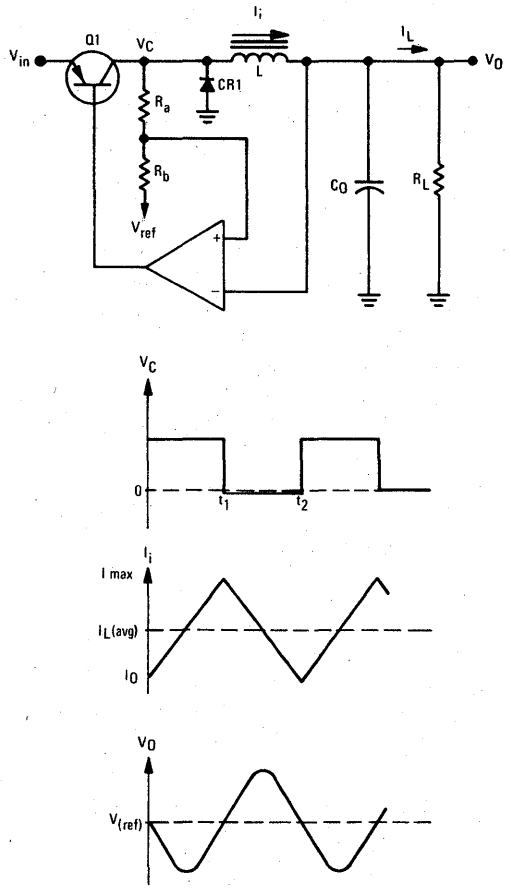
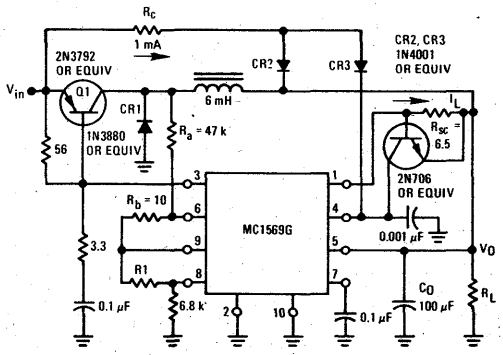


FIGURE 32 – MC1569 SELF-OSCILLATING SWITCHING REGULATOR



As a design center is required for a practical circuit, assume the following requirements:

V_{in} = +28 Volts

V_O = +10 Volts

ΔV_O = 50 mV

f ≅ 5 kHz

I(max) = 1.125 A

I_O = 1 A

$$\Delta V \approx V_{in} \frac{R_b}{R_a}. \qquad (2)$$

Using Equation (1), the inductor value can be found:

$$L = \frac{(28-10)}{2(1.125-1)} \frac{10}{28} \left(\frac{1}{5 \times 10^3}\right)$$

$$\approx 7 \text{ mH}.$$

For the test circuit, a value of 6 mH was selected. Using for a first approximation

$$C_O = \frac{(V_{in} - V_O)(V_O)}{8L f^2 V_{in} (\Delta V)}$$

$$= \frac{(28-10)10}{8(7 \times 10^{-3})(5 \times 10^3)^2 (28)(50 \times 10^{-3})}$$

$$\approx 95\ \mu F.$$

As shown, a value of 100 μF was selected. Since little current is required at pin 6, R_a can be large. Assume R_a = 47 kΩ and then use Equation (2) to determine R_b:

$$50 \times 10^{-3} = \frac{28}{47\ k\Omega} R_b$$

$$R_b = \frac{47}{28} 50 \approx 85\Omega.$$

Since the internal impedance presented by pin 9 is on the order of 60Ω, a value of R_b = 10Ω is adequate.

Diodes CR2, CR3, and R_c may be added to prevent saturation of the error amplifier to increase switching speed. When the output stage of the error amplifier approaches saturation, CR2 becomes forward biased and clamps the error amplifier. Resistor R_c should be selected to supply a total of 1 mAdc to CR2 and CR3.

To show correlation between the predicted and tested specifications the following data was obtained:

V_{in} = +28 (±1%) Volts

V_O = +10 Volts

ΔV_O = 60 mV

f = 7 kHz

@ I_L = 1A

which checks quite well with the predicted values. R_b can be adjusted to minimize the ripple component as well as to trim the operating frequency. Also this frequency will change with varying loads as is normal with this type of circuit. Pin 2 can still be used for shut-down if so desired. R_{sc} should be set such that the ratio of load current to base drive current is 10:1 in this case $I_1 \approx 100$ mA and R_{sc} = 6.5Ω.

POSITIVE AND NEGATIVE POWER SUPPLIES

If the MC1569 is driven from a floating source it is possible to use it as a negative regulator by grounding the positive output terminal. The MC1569 may also be used with the MC1563 to provide completely independent positive and negative voltage regulators with comparable performance.

Some applications may require complementary tracking in which both supplies arrive at the voltage level simultaneously, and variations in the magnitudes of the two voltages track. Figures 1 and 33 illustrate this approach. In this application, the MC1563 is used as the reference regulator, establishing the negative output voltage. The MC1569 positive regulator is used in a tracking mode by grounding one side of the differential amplifier (pin 6 of the MC1569) and using the other side (pin 5 of the MC1569) to sense the voltage developed at the junction of the two 3-k ohm resistors. This differential amplifier controls the MC1569 series pass transistor such that the voltage at pin 5 will be zero. When the voltage at pin 5 equals zero, $+V_O$ must equal $|-V_O|$.

For the configuration shown in Figure 33, the level shift amplifier in the MC1569 is employed to generate an auxiliary +5-volt supply which is boosted to a 2-ampere capability by Q1 and Q2. (The +5-volt supply, as shown,

is not short-circuit protected.) The −15-volt supply varies less than 0.1 mV over a zero to −300 mAdc current range and the +15-volt supply tracks this variation. The +15-volt supply varies 20 mV over the zero to +300 mAdc load current range. The +5-volt supply varies less than 5 mV for $0 \leq I_L \leq 200$ mA with the other two voltages remaining unchanged. See page 19 for additional information.

SHUTDOWN TECHNIQUES

Pin 2 of the MC1569 is provided for the express purpose of shutting the regulator "OFF". Referring to the schematic, it can be seen that pin 2 goes to the base of an NPN transistor, which, if turned "ON", will turn the zener "OFF" and deny current to all the biasing current sources. This action causes the output to go to essentially zero volts and the only current drawn by the IC regulator will be the small start current through the 60-k-ohm start resistor (V_{in}/60 kΩ). This feature provides additional versatility in the applications of the MC1569. Various subsystems may be placed in a "standby" mode to conserve power until actually needed. Or the power may be turned "OFF" in response to other occurrences such as overheating, over-voltage, shorted output, etc.

To activate shutdown, one simply applies a potential greater than two diode drops with a current capability of 1 mA. Note that if a hard supply (i.e., +3 V) is applied directly to pin 2, the shutdown circuitry will be destroyed since there is no inherent current limiting. Maximum rating for the drive current into pin 2 is 10 mA, while 1 mA is adequate for shutdown.

4

FIGURE 33 – A ±15 Vdc COMPLEMENTARY TRACKING REGULATOR WITH AUXILIARY +5.0 V SUPPLY

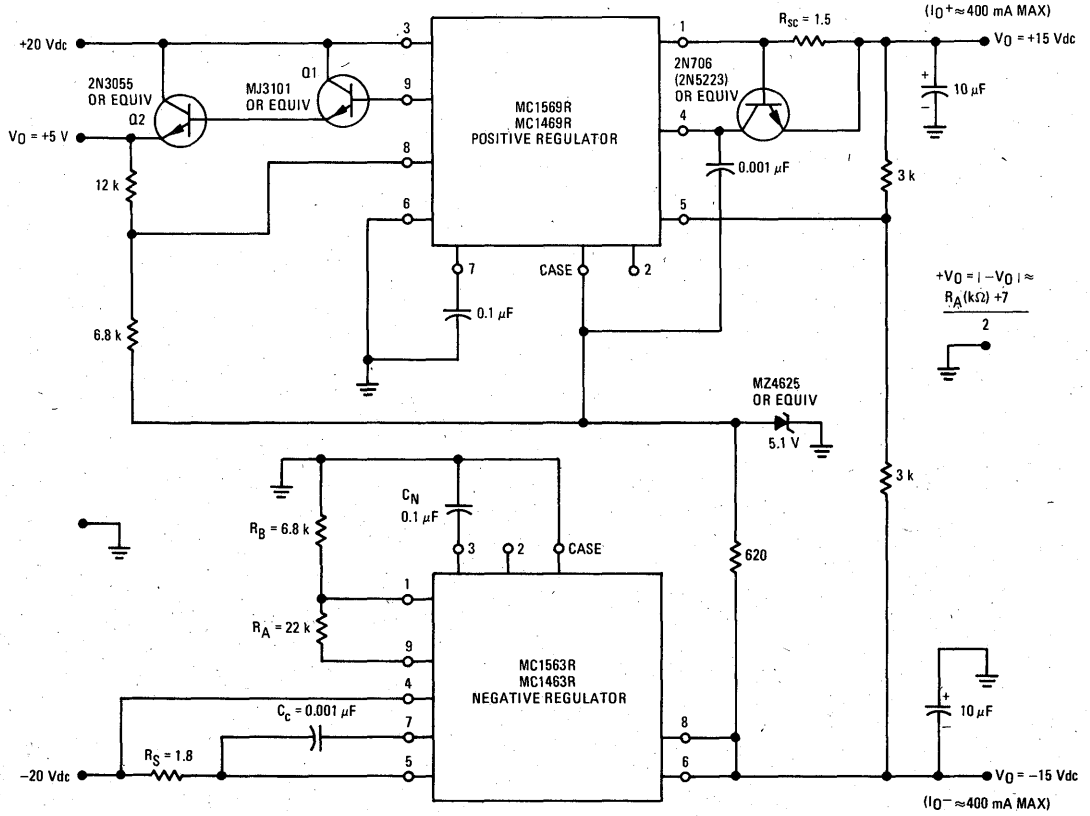


FIGURE 34 – ELECTRONIC SHUT-DOWN USING A MDTL GATE

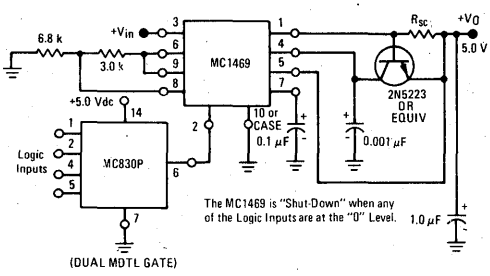


FIGURE 35 – AUTOMATIC LATCH INTO SHUT-DOWN WHEN OUTPUT IS SHORT-CIRCUITED WITH MANUAL RE-START

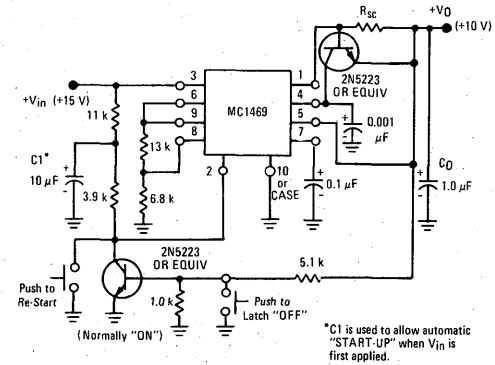


FIGURE 36 – VOLTAGE BOOSTING CIRCUIT

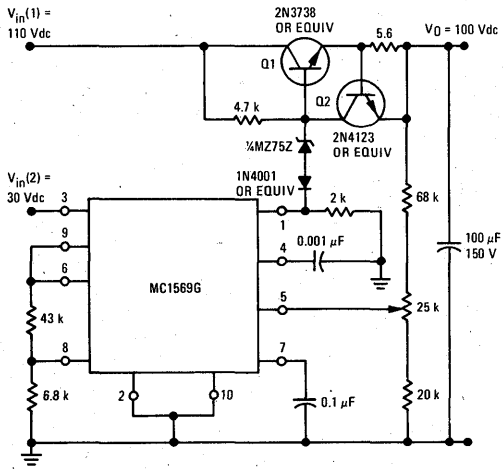


Figure 34 shows how the regulator can be controlled by a logic gate. Here, it is assumed that the regulator operates in its normal mode – as a positive regulator referenced to ground – and that the logic gate is of the saturating type, operating from a positive supply to ground. The high logic level should be greater than about 1.5 V and should source no more than 10 mA into pin 2.

The gate shown is of the MDTL type. MRTL and MTTL can also be used as long as the drive current is within safe limits (this is important when using MTTL, where the output stage uses an active pull-up).

In some cases a regulator can be designed which can handle the power dissipation resulting from normal operation but cannot safely dissipate the power resulting from a sustained short-circuit. The circuit of Figure 35 solves this problem by shutting down the regulator when the output is short-circuited.

VOLTAGE BOOSTING

The MC1569 has a maximum output voltage capability of 37 volts which covers the bulk of the user requirements. However, it is possible to obtain higher output voltages. One such voltage boosting circuit is shown in Figure 36.

Since high voltage NPN silicon devices are readily available, the only problem is the voltage limitations of the MC1569. This can be overcome by using voltage shift techniques to limit the voltage to 35 volts across the MC1569 while referencing to a higher output voltage.

The zener diode in the base lead of the NPN device is used to shift the output voltage of the MC1569 by approximately 75 volts to the desired high voltage level, in this case 100 volts. Another voltage shift is accomplished by the resistor divider on the output to accommodate the required 25 volt reference to the MC1569. The 2 kΩ resistor is used to bias the zener diode so the current through the 4.7 kΩ resistor can be controlled by the MC1569. The 1N4001 diode protects the MC1569 from supplying load current under short circuit conditions and Q2 serves to limit base current to Q1. For R_{SC} as shown, the short circuit current will be approximately 100 mA.

In order to use a single supply voltage, $V_{in}(2)$ can be derived from $V_{in}(1)$ with a zener diode, shunt pre-regulator.

It can be seen that loop gain has been reduced by the resistor divider and hence the closed loop bandwidth will be less. This of course will result in a more stable system, but regulator performance is degraded to some degree.

REMOTE SENSING

The MC1569 offers a remote sensing capability. This is important when the load is remote from the regulator,

as the resistance of the interconnecting lines (V_O and GND) are added directly to the output impedance of the regulator. By remote sensing, this resistance is included inside the control loop of the regulator and is essentially eliminated. Figure 37 shows how remote sensing is accomplished using both a separate sense line from pin 8 and a separate ground line from the regulator to the remote load.

AN ADJUSTABLE ZERO-TEMPERATURE-COEFFICIENT (0-TC) VOLTAGE REFERENCE SOURCE.

The MC1569, when used in conjunction with low TC resistors, makes an excellent reference-voltage generator. If the 3.5 volt reference voltage of the IC regulator is a satisfactory value, then pins 8 and 9 can be tied together and no resistors are needed. This will provide a voltage reference having a typical temperature coefficient of 0.002%/°C. By adding two resistors, R1 and R2, any voltage between 3.5 Vdc and 37 Vdc can be obtained with the same low TC (see Figure 38).

THERMAL SHUTDOWN

By setting a fixed voltage at pin 2, the MC1569 chip can be protected against excessive junction temperatures caused by power dissipation in the IC regulator. This is based on the negative temperature coefficient of the base-emitter junction of the shutdown transistor and the diode in series with pin 2 (-3.4×10^{-3} V/°C). By setting 1.0 Vdc externally at pin 2, the regulator will shutdown when the chip temperature reaches approximately +140°C. Figure 39 shows a circuit that uses a zero-TC zener diode and a resistive divider to obtain this voltage.

FIGURE 37 – REMOTE SENSING CIRCUIT

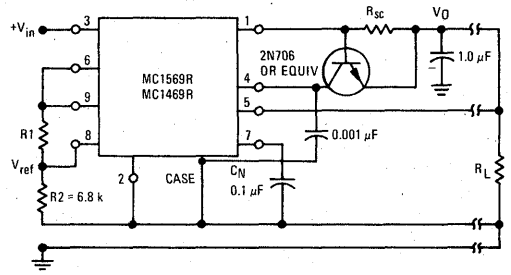


FIGURE 38 – AN ADJUSTABLE "ZERO-TC" VOLTAGE SOURCE

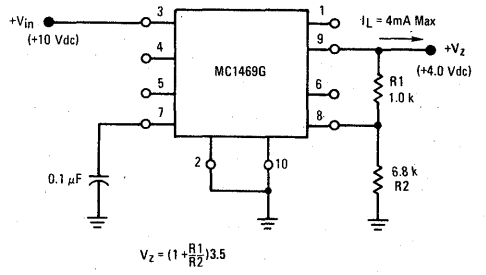


FIGURE 39 – JUNCTION TEMPERATURE LIMITING SHUTDOWN CIRCUIT

FIGURE 39A – USING A ZERO TC REFERENCE

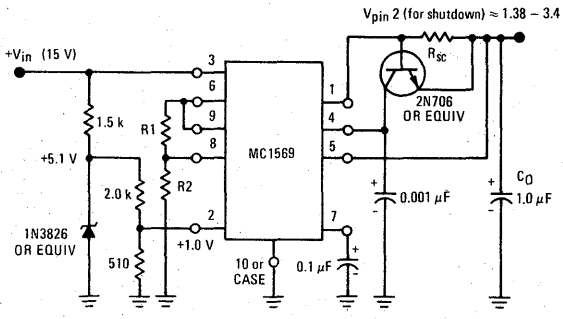


FIGURE 39B – USING A T_A REFERENCE

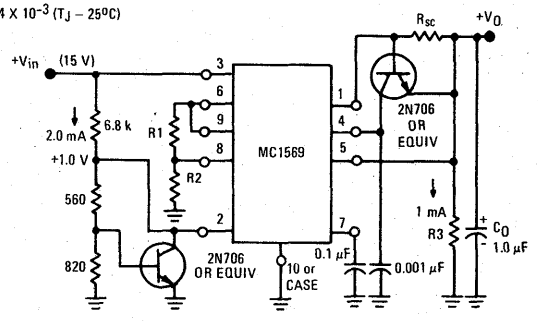


FIGURE 40 – THERMAL SHUTDOWN WHEN USING EXTERNAL PASS TRANSISTORS

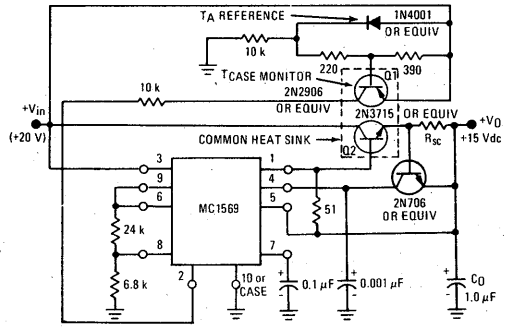
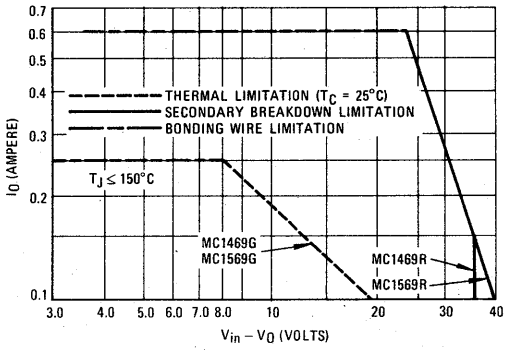


FIGURE 41 – DC SAFE OPERATING AREA



In the case where an external pass transistor is employed, its temperature, rather than that of the IC regulator, requires control. A technique similar to the one just discussed can be used by directly monitoring the case temperature of the pass transistor as is indicated in Figure 40. The case of the normally "OFF" thermal monitoring transistor, Q2, should be in thermal contact with, but electrically isolated from, the case of the boost transistor, Q1.

THERMAL CONSIDERATIONS

Monolithic voltage regulators are subjected to internal heating similar to a power transistor. Since the degree of internal heating is a function of the specific application, the designer must use caution not to exceed the specified maximum junction temperature (+150°C). Exceeding this limit will reduce reliability at an exponential rate. Good heatsinking not only reduces the junction temperature for a given power dissipation; it also tends to improve the dc stability of the output voltage by reducing the junction temperature change resulting from a change in the power dissipation of the IC regulator. By using the derating factors or thermal resistance values given in the Maximum Ratings Table of this data sheet, junction temperature can be computed for any given application in the same manner as for a power transistor*. A short-circuit on the output terminal can produce a "worst-case" thermal condition especially if the maximum input voltage is applied simultaneously with the maximum value of short-circuit load current. Care should be taken not to exceed the maximum junction temperature rating during this fault condition and, in addition, the dc safe operating area limit (see Figure 41).

Thermal characteristics for a voltage regulator are useful in predicting performance since dc load and line regulation are affected by changes in junction temperature. These temperature changes can result from either a change in the ambient temperature, T_A, or a change in the power dissipated in the IC regulator. The effects of ambient temperature change on the dc output voltage can be estimated from the "Temperature Coefficient of Output Voltage" characteristic parameter shown as ±0.002%/°C, typical. Power dissipation is typically changed in the IC regulator by varying the dc load current. To estimate the dc change in output voltage due to a change in the dc load current, three effects must be considered:

1. junction temperature change due to the change in the power dissipation
2. output voltage decrease due to the finite output impedance of the control amplifier
3. thermal gradient on the IC chip.

A temperature differential does exist across a power IC chip and can cause a dc shift in the output voltage. A "gradient coefficient," GCV_O, can be used to describe this effect and is typically –0.06%/watt for the MC1569. For an example of the relative magnitudes of these effects, consider the following conditions:

Given MC1569

with V_{in} = 10 Vdc

V_O = 5 Vdc

*For more detailed information of methods used to compute junction temperature, see Motorola Application Note AN-226, Measurement of Thermal Properties of Semiconductors.

and I_L = 100 mA to 200 mA

(ΔI_L = 100 mA)

assume T_A = +25°C

TO-66 Case with heatsink

assume θ_{CS} = 0.2°C/W

and θ_{SA} = 2°C/W

θ_{JC} = 7.15°C/W (from maximum ratings table)

4

It is desired to find the ΔV_O which results from this ΔI_L. Each of the three previously stated effects on V_O can now be separately considered.

1. ΔV_O due to ΔT_J

$$\Delta V_O = (V_O)(\Delta P_D)(TCV_O)(\theta_{JC} + \theta_{CS} + \theta_{SA})$$

OR

$$\Delta V_O = (5V)(5\ V \times 0.1A)(\pm 0.002\%/°C)(9.35°C/W)$$

$$\Delta V_O \approx \pm 0.5\ mV$$

2. ΔV_O due to z_o

$$|\Delta V_O| = (-z_o)(I_L)$$

$$|\Delta V_O| = -(2 \times 10^{-2})(10^{-1}) = -2\ mV$$

3. ΔV_O due to gradient coefficient, GCV_O

$$|\Delta V_O| = (GCV_O)(V_O)(\Delta P_D)$$

$$|\Delta V_O| = (-6 \times 10^{-4}/W)(5\ volts)(5 \times 10^{-1} W)$$

$$|\Delta V_O| = -1.6\ mV$$

Therefore the total ΔV_O is given by

$$|\Delta V_O\ total| = \pm 0.5 - 2.0 - 1.6\ mV$$

OR

$$-4.1\ mV \leqslant |V_O\ total| \leqslant -3.1\ mV$$

Other operating conditions may be substituted and computed in a similar manner to evaluate the relative effects of the parameters.

TYPICAL PRINTED CIRCUIT BOARD LAYOUT

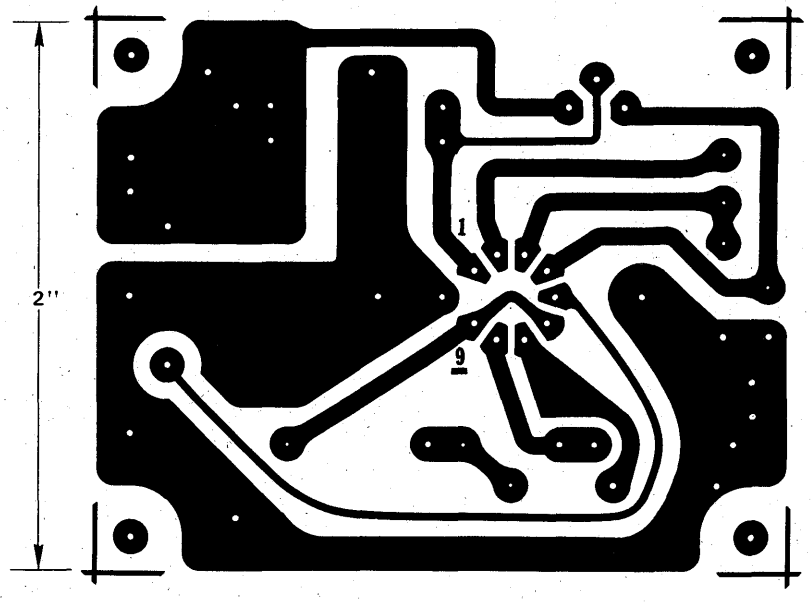


FIGURE 42 – LOCATION OF COMPONENTS

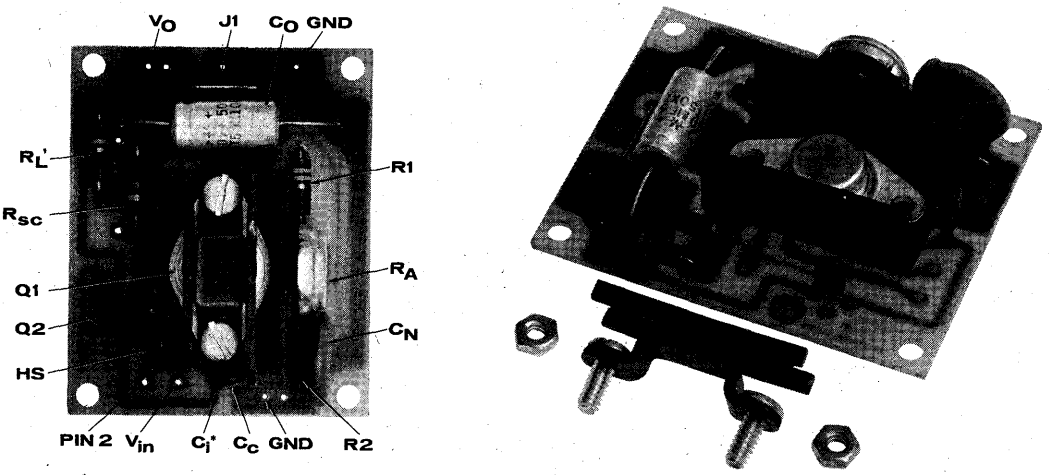
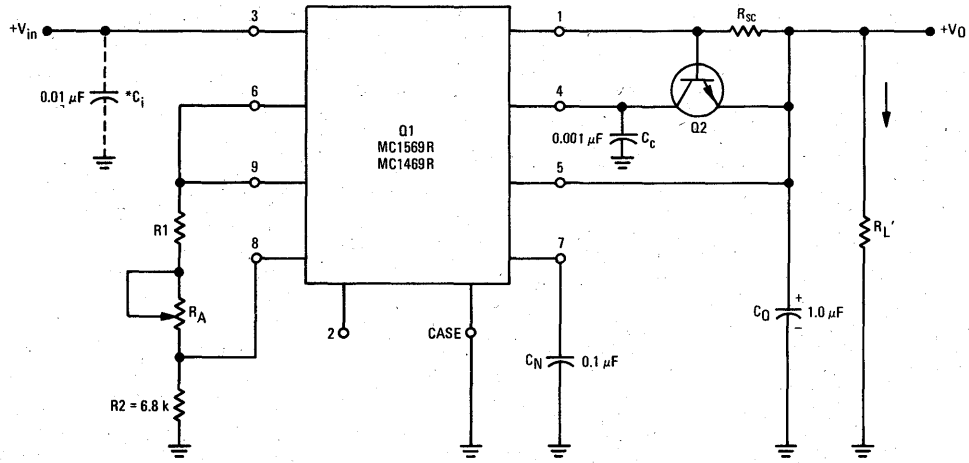


FIGURE 43 – CIRCUIT SCHEMATIC FOR PRINTED CIRCUIT BOARD (Pg. 17)
3.5 V≤V_O≤37 V, 1 mA≤I_L≤500 mA



Select R1 to give desired V_O: R1 ≈ (2 V_O –7) kΩ

*C_i – May be required if long input leads are used.

PARTS LIST

Component	Value	Description
R1 R2	Select 6.8 k	1/4 or 1/2 watt carbon
*R_A	Select	IRC Model X-201 Mallory Model MTC-1 or equivalent
R_{sc}	Select	1/2 watt carbon
*R_L	Select	For minimum current of 1 mAdc
C_O	1.0 μF	Sprague 1500 Series, Dickson D10C series or equivalent
C_N C_c *C_i	0.1 μF 0.001 μF 0.01 μF	Ceramic Disc – Centralab DDA104, Sprague TG-P10, or equivalent
Q1 Q2	MC1569R or MC1469R 2N5223, 2N706, or equivalent	
*HS	–	Heatsink Thermalloy #6168B
*Socket	(Not Shown)	Robinson Nugent #0001306 Electronic Molding Corp. #6341-210-1, 6348-188-1, 6349-188-1
PC Board	–	Circuit Dot, Inc. #PC1113 1155 W. 23rd St., Tempe, Ariz. 85281
*Optional		

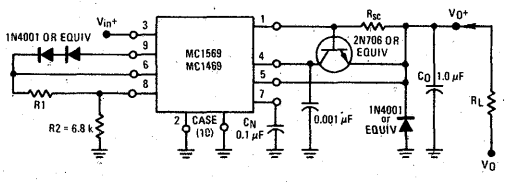
LATCH-UP

Latch-up of these and other regulators can occur if:

1. There are plus and minus voltages available
2. A load exists between V_O^+ and V_O^- (This "common load" may be something inconspicuous – e.g. an operational amplifier. Nearly everyone who uses + and – voltages will have a common load from V_{CC} to V_{EE}.)
3. V_{in}^+ and V_{in}^- are not applied at the same time.

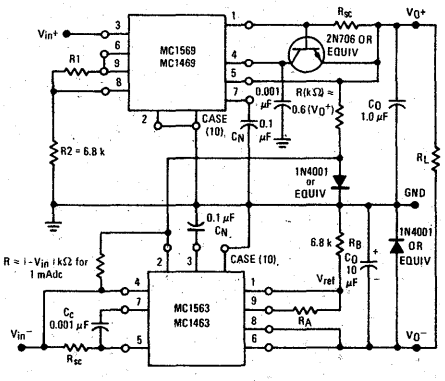
The above conditions result in one of the two outputs becoming reverse-biased which prevents the regulator from turning ON . Latch-up can be prevented by the circuit configurations shown in Figures 44 and 45.

FIGURE – 44



Note: This configuration increases minimum input-output differential voltage by ≈ 0.7 V.

FIGURE – 45



MC1723
MC1723C

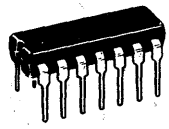
MONOLITHIC VOLTAGE REGULATOR

The MC1723 is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors. MC1723 is specified for operation over the military temperature range (-55°C to +125°C) and the MC1723C over the commercial temperature range (0 to +70°C)

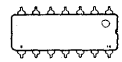
- Output Voltage Adjustable from 2 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line and 0.03% Load Regulation
- Adjustable Short-Circuit Protection

VOLTAGE REGULATOR

SILICON
MONOLITHIC
INTEGRATED CIRCUIT

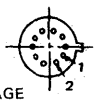


(top view)

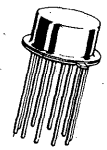


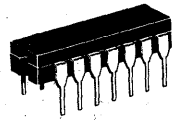
P SUFFIX
PLASTIC PACKAGE
CASE 646

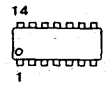
(bottom view)



G SUFFIX
METAL PACKAGE
CASE 603C
(TO-100 Type)





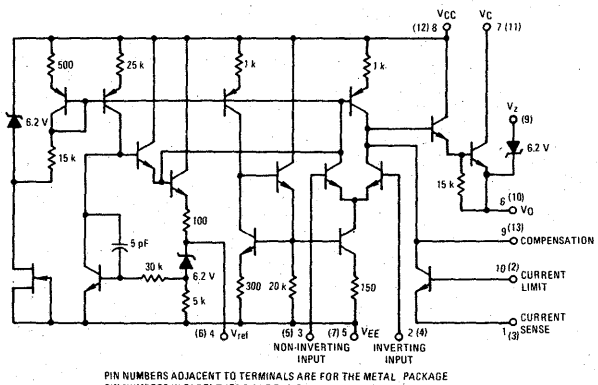


L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)

ORDERING INFORMATION

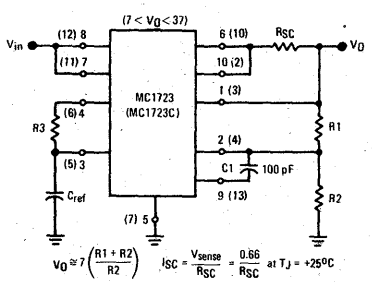
Device	Alternate	Temperature Range	Package
MC1723CG	LM723CH, μA723HC	0°C to 70°C	Metal Can
MC1723CL	LM723CD, μA723DC	0°C to +70°C	Ceramic DIP
MC1723CP	LM723CN, μA723PC	0°C to +70°C	Plastic DIP
MC1723G	–	-55°C to +125°C	Metal Can
MC1723L	–	-55°C to +125°C	Ceramic DIP

FIGURE 1 – CIRCUIT SCHEMATIC



PIN NUMBERS ADJACENT TO TERMINALS ARE FOR THE METAL PACKAGE
PIN NUMBERS IN PARENTHESIS ARE FOR DUAL IN-LINE PACKAGES.

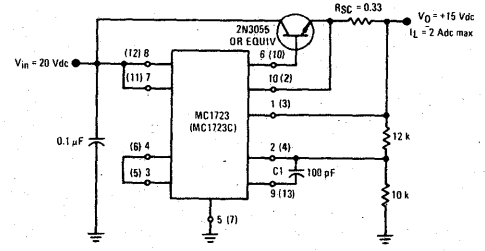
FIGURE 2 – TYPICAL CIRCUIT CONNECTION



$V_O \cong 7\left(\frac{R1 + R2}{R2}\right)$ $I_{SC} = \frac{V_{sense}}{R_{SC}} = \frac{0.66}{R_{SC}}$ at T_J = +25°C

For best results 10 k < R2 < 100 k
For minimum drift R3 = R1||R2

FIGURE 3 – TYPICAL NPN CURRENT BOOST CONNECTION



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Pulse Voltage from V_{CC} to V_{EE} (50 ms)	$V_{in(p)}$	50	V_{peak}
Continuous Voltage from V_{CC} to V_{EE}	V_{in}	40	Vdc
Input-Output Voltage Differential	$V_{in} - V_O$	40	Vdc
Maximum Output Current	I_L	150	mAdc
Current from V_{ref}	I_{ref}	15	mAdc
Current from V_z	I_z	25	mA
Voltage Between Non-Inverting Input and V_{EE}	V_{ie}	8.0	Vdc
Differential Input Voltage	V_{id}	±5.0	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
T_A = +25°C	P_D	1.25	W
Derate above T_A = +25°C	$1/\theta_{JA}$	10	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	100	°C/W
Metal Package			
T_A = +25°C	P_D	1.0	Watt
Derate above T_A = +25°C	$1/\theta_{JA}$	6.6	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	150	°C/W
T_C = +25°C	P_D	2.1	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	14	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	35	°C/W
Dual In-Line Ceramic Package	P_D	1.5	Watt
Derate above T_A = +25°C	$1/\theta_{JA}$	10	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	100	°C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}		°C
Metal Package		-65 to +150	
Dual In-Line Ceramic and Ceramic Flat Packages		-65 to +175	
Operating Ambient Temperature Range	T_A		°C
MC1723C		0 to +70	
MC1723		-55 to +125	

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: T_A = +25°C, V_{in} 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, C1 = 100 pF, C_{ref} = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 1)

Characteristic	Symbol	MC1723 Min	MC1723 Typ	MC1723 Max	MC1723C Min	MC1723C Typ	MC1723C Max	Unit
Input Voltage Range	V_{in}	9.5	–	40	9.5	–	40	Vdc
Output Voltage Range	V_O	2.0	–	37	2.0	–	37	Vdc
Input-Output Voltage Differential	$V_{in}-V_O$	3.0	–	38	3.0	–	38	Vdc
Reference Voltage	V_{ref}	6.95	7.15	7.35	6.80	7.15	7.50	Vdc
Standby Current Drain (I_L = 0, V_{in} = 30 V)	I_{IB}	–	2.3	3.5	–	2.3	4.0	mAdc
Output Noise Voltage (f = 100 Hz to 10 kHz)	V_N							μV(RMS)
C_{ref} = 0		–	20	–	–	20	–	
C_{ref} = 5.0 μF		–	2.5	–	–	2.5	–	
Average Temperature Coefficient of Output Voltage (T_{low} ① < T_A < T_{high} ②)	TCV_O	–	0.002	0.015	–	0.003	0.015	%/°C
Line Regulation	Reg_{in}							%V_O
(T_A = +25°C) 12 V < V_{in} < 15 V		–	0.01	0.1	–	0.01	0.1	
(T_A = +25°C) 12 V < V_{in} < 40 V		–	0.02	0.2	–	0.1	0.5	
(T_{low} ① < T_A < T_{high} ②) 12 V < V_{in} < 15 V		–	–	0.3	–	–	0.3	
Load Regulation (1.0 mA < I_L < 50 mA)	Reg_{load}							%V_O
T_A = +25°C		–	0.03	0.15	–	0.03	0.2	
T_{low} ① < T_A < T_{high} ②		–	–	0.6	–	–	0.6	
Ripple Rejection (f = 50 Hz to 10 kHz)	Rej_R							dB
C_{ref} = 0		–	74	–	–	74	–	
C_{ref} = 5.0 μF		–	86	–	–	86	–	
Short Circuit Current Limit (R_{SC} = 10 Ω, V_O = 0)	I_{SC}	–	65	–	–	65	–	mAdc
Long Term Stability	$\Delta V_O/\Delta t$	–	0.1	–	–	0.1	–	%/1000 Hr

① T_{low} = 0°C for MC1723C
= -55°C for MC1723

② T_{high} = +70°C for MC1723C
= +125°C for MC1723

TYPICAL CHARACTERISTICS

(V_{in} = 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, T_A = +25°C unless otherwise noted.)

FIGURE 4 – MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

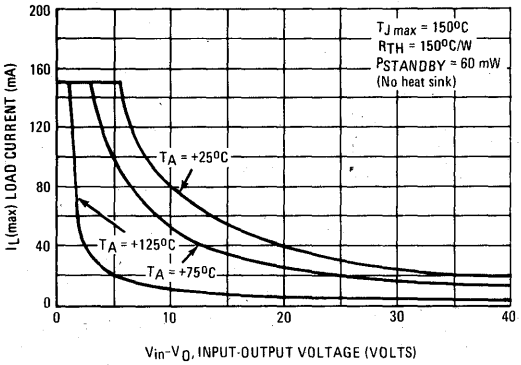


FIGURE 5 – LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING

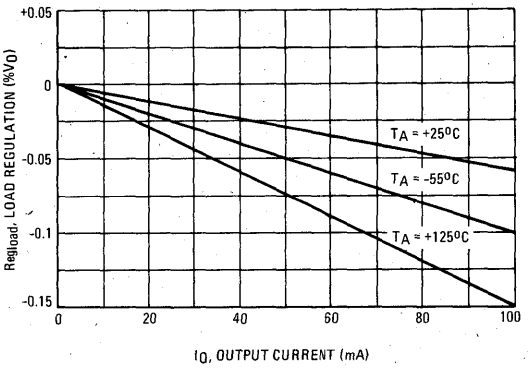


FIGURE 6 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

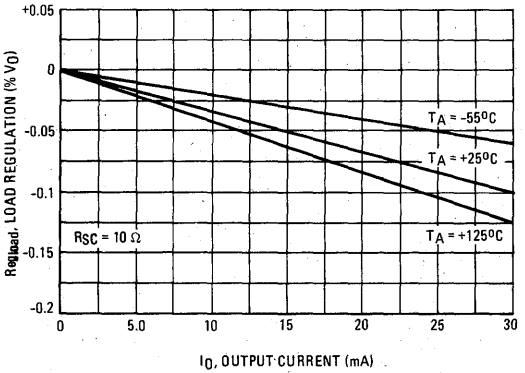


FIGURE 7 – LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

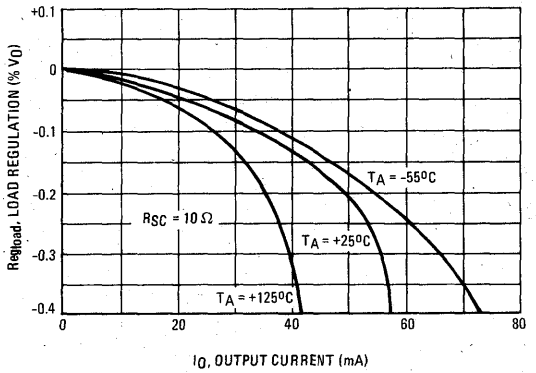


FIGURE 8 – CURRENT LIMITING CHARACTERISTICS

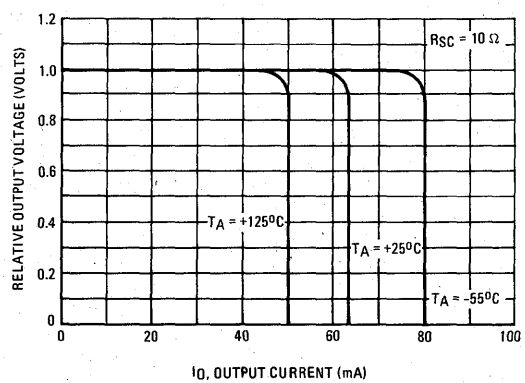
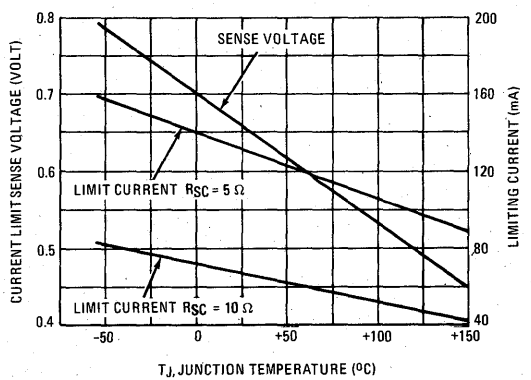


FIGURE 9 – CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



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TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

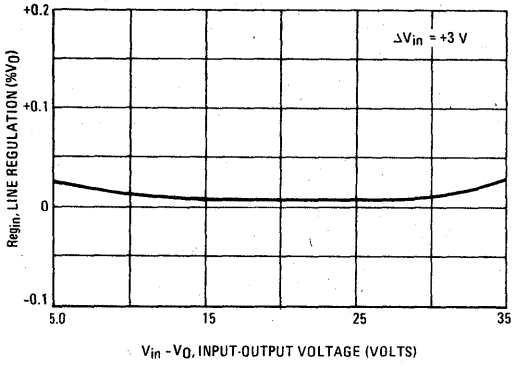


FIGURE 11 – LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

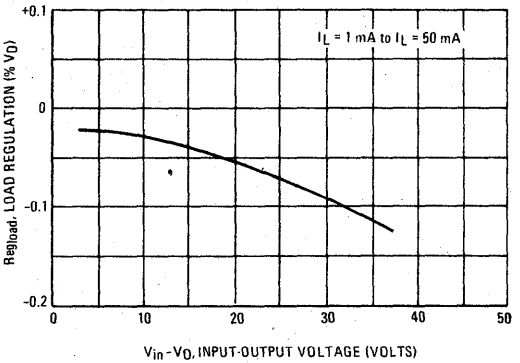


FIGURE 12 – STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

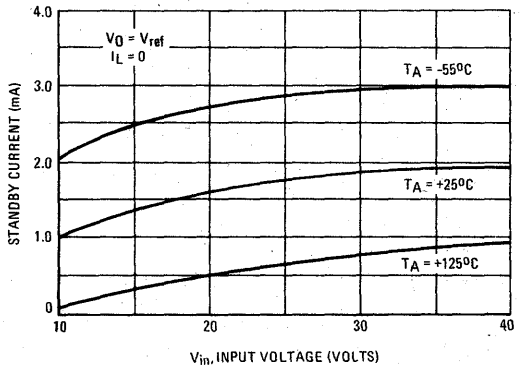


FIGURE 13 – LINE TRANSIENT RESPONSE

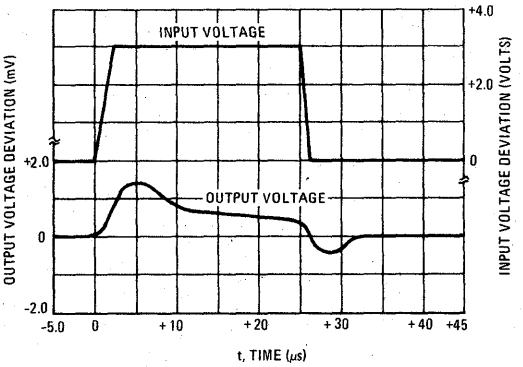


FIGURE 14 – LOAD TRANSIENT RESPONSE

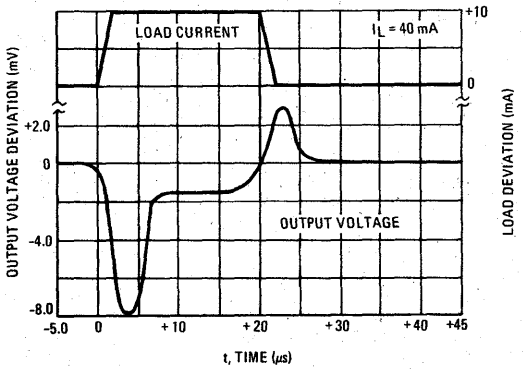
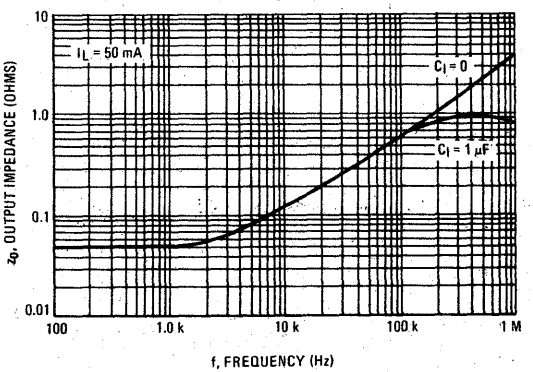


FIGURE 15 – OUTPUT IMPEDANCE AS FUNCTION OF FREQUENCY



TYPICAL APPLICATIONS

Pin numbers adjacent to terminals are for the metal package; pin numbers in parenthesis are for the dual in-line packages.

FIGURE 16 – TYPICAL CONNECTION FOR $2 < V_O < 7$

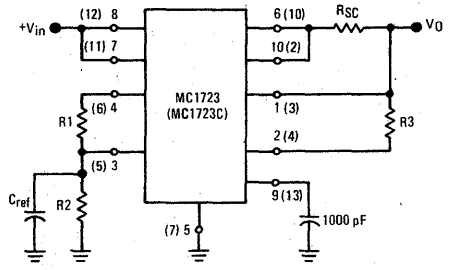


FIGURE 17 – MC1723,C FOLDBACK CONNECTION

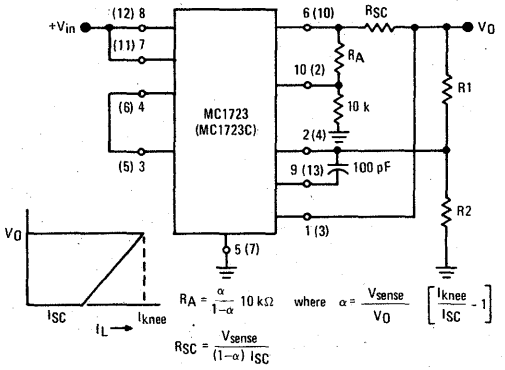


FIGURE 18 – +5 V, 1-AMPERE SWITCHING REGULATOR

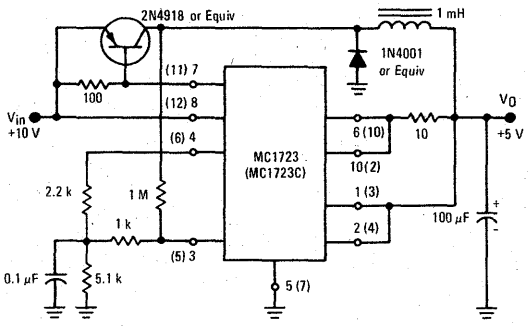


FIGURE 19 – +5 V, 1-AMPERE HIGH EFFICIENCY REGULATOR

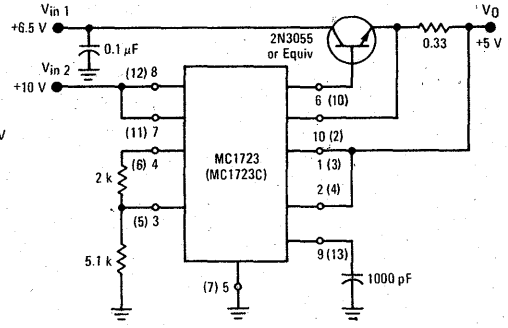


FIGURE 20 – +15 V, 1-AMPERE REGULATOR WITH REMOTE SENSE

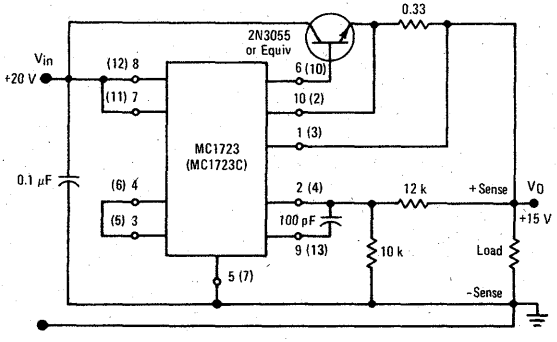
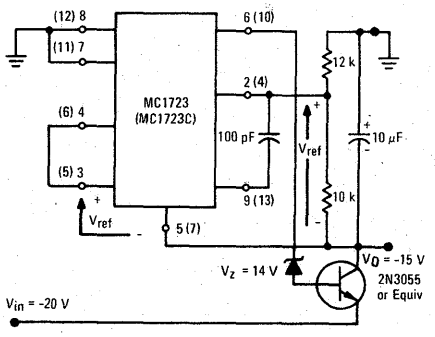
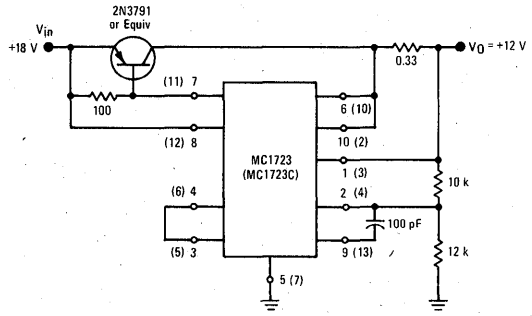


FIGURE 21 – -15 V NEGATIVE REGULATOR



TYPICAL APPLICATIONS (continued)

FIGURE 22 – +12 V, 1-AMPERE REGULATOR USING PNP CURRENT BOOST



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}} \geq V_I I_S - V_O I_O$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

I_S = Total Supply Current

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MC3420
MC3520

Advance Information

SWITCHMODE REGULATOR CONTROL CIRCUIT

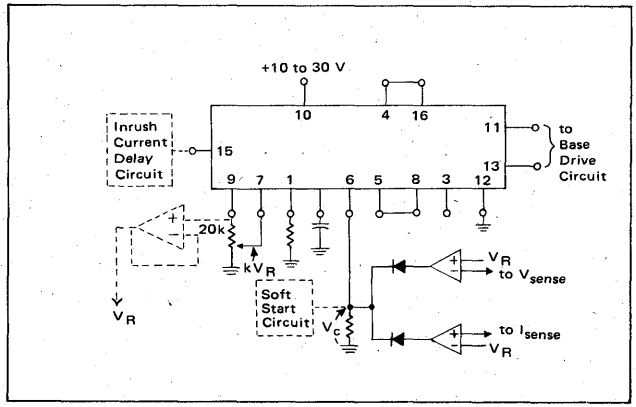
The MC3520/3420 is an inverter control unit which provides all the control circuitry for PWM push-pull, bridge and series type switch-mode power supplies.

These devices are designed to supply the pulse width modulated drive to the base of two external power transistors. Other applications where these devices can be used are in transformerless voltage doublers, transformer coupled dc to dc converters and other power control functions.

The MC3520 is specified over the military operating range of -55°C to +125°C. The MC3420 is specified from 0°C to +70°C.

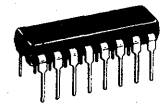
- Includes 100 kHz Symmetrical Oscillator
- On Chip Pulse Width Modulator, Voltage Reference, Dead Time Comparator, and Phase Splitter
- Output Frequency Adjustable (2 kHz to 100 kHz)
- Inhibit and Symmetry Correction Inputs Available
- Controlled Start-Up
- Frequency and Dead Time are Independently Adjustable (0% to 100%)
- Can be Slaved to Other MC3420's
- Open Collector Outputs
- Output Capability 50 mA (Max.)
- On Chip Protection Against Double Pulsing of Same Output During Load Transient Condition

FIGURE 1—TYPICAL APPLICATION

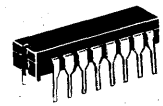


SWITCHMODE REGULATOR CONTROL CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUITS

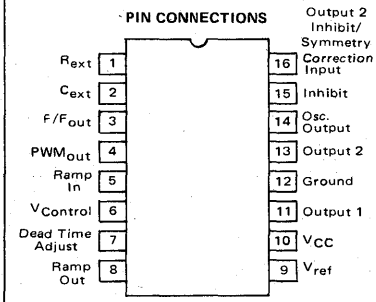


P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN CONNECTIONS



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC3420P	0 to +70°C	Plastic DIP
MC3420L	0 to +70°C	Ceramic DIP
MC3520L	-55 to +125°C	Ceramic DIP

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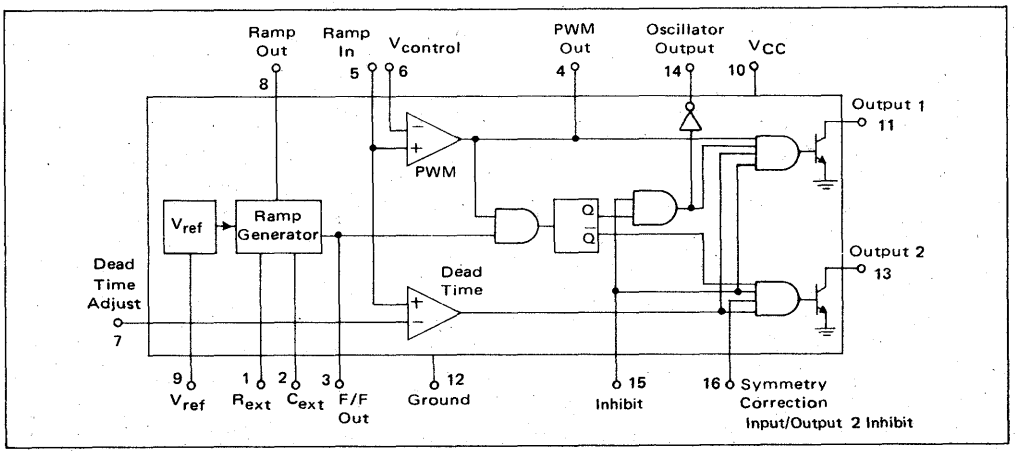
ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	10	–	30	V
Supply Current	I_{CC}	–	–	16	mA
Output Frequency Range	f_o	2.0	–	100	kHz
Frequency Stability ($T_A = T_{high}$ to T_{low}, $10<V_{CC}<30$ V)	–	–	4.0	–	%
Voltage Reference	V_{ref}	–	7.9	–	V
Temperature Coefficient of Voltage Reference (I_{ref} = 400 μA)	TCV_{ref}	–	0.006	0.02	%/°C
Output Voltage (I_{OL} = +40 mA) (I_{OL} = +25 mA)	V_{OL}	– –	– –	0.5 0.3	V
Output Blocking Voltage	–	–	–	40	V
Oscillator Output Voltage (I_{OL} = +5 mA)	V_{osc}	–	–	0.5	V
Temperature Coefficient of Dead Time	TC_{DT}	–	0.15	–	%/°C
Inhibit I_{IL} (V_{IL} = 0.7 V)	–	–	–	-0.2	mA
Inhibit I_{IH} (V_{IH} = 2.4V)	–	–	–	40	μA
Minimum Dead Time	–	0	–	–	μ

T_{low} = −55°C for MC3520, 0°C for MC3420 T_{high} = +125°C for MC3520, +70°C for MC3420

FIGURE 2–EQUIVALENT CIRCUIT



GENERAL INFORMATION

The internal block diagram of the MC3420 is shown in Figure 2, and consists of the following sections:

Voltage Reference

A stable reference voltage is generated by the MC3420 primarily for internal use. However, it is also available externally at Pin 9 (V_{ref}) for use in setting the dead time (Pin 7) and for use as a reference for the external control loop error amplifiers.

Ramp Generator

The ramp generator section produces a symmetrical triangular waveform ramping between 2.0 V and 6.0 V, with frequency determined by an external resistor (R_{ext}) and capacitor (C_{ext}) tied from Pins 1 and 2, respectively, to ground.

PWM Comparator

The output of the ramp generator at pin 8 is normally connected to Pin 5, RAMP IN. The PWM (pulse width modulation) comparator compares the voltage at Pin 6

($V_{control}$) to the ramp generator output. The level of $V_{control}$ determines the outputs' pulse width or duty cycle. The duty cycle of each output can vary, exclusive of dead time, from 50% (when $V_{control}$ is at approximately 2.0 V) to 0% ($V_{control}$ approximately 6.0 V).

Dead Time Comparator

An additional comparator has been included in MC3420 to allow independent adjustment of system dead time or maximum duty cycle. By dividing down V_{ref} at Pin 9 with a resistive divider or potentiometer, and applying this voltage to Pin 7, a stable dead time is obtained for prevention of inverter switching transistor cross conduction at high duty cycles due to storage time delays.

Phase Splitter

A phase splitter is included to obtain two 180° out of phase outputs for use in multiple transistor inverter systems. It consists of a toggle flip-flop whose clock signal is derived by "ANDing" the output of the PWM comparator and a signal from the ramp generator section. This "AND" gate ensures that the outputs truly alternate under control loop transient conditions. Better understanding of this feature and MC3420 operation may be gained by studying the circuit waveforms, shown in Figure 3.

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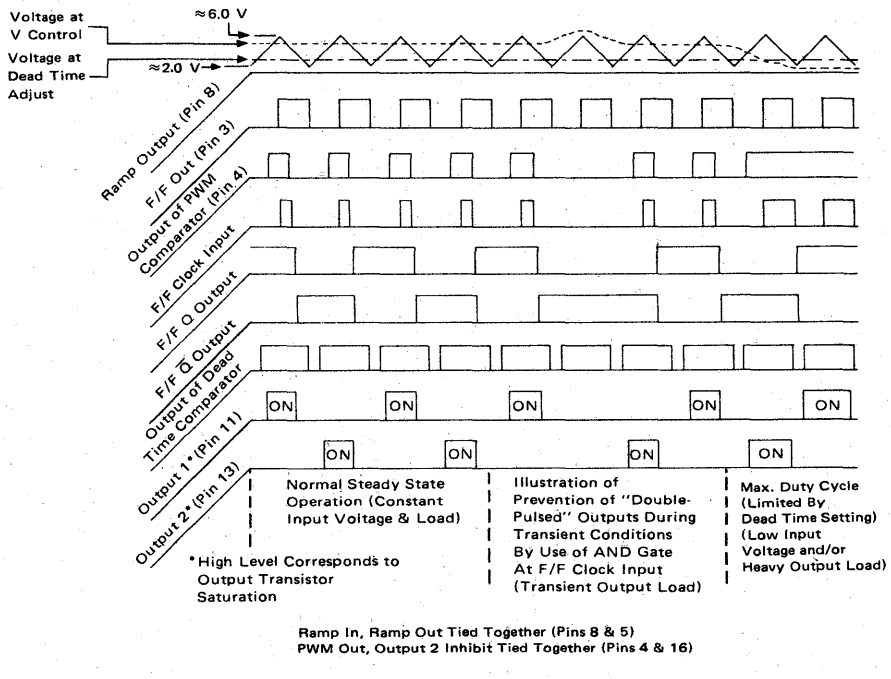
FIGURE 3 – INTERNAL WAVEFORMS



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Outputs

The outputs of the MC3420 are open collector transistors capable of sinking up to 50 mA and blocking up to 40 V. They may be wire-ORed for operation in single transistor inverter systems.

Symmetry Correction Input

In some PWM inverter/converter configurations it may be desirable that one output's duty cycle be controlled independently of the other's for implementation of a system symmetry correcting control loop. In these cases, independent control of output 2 (Pin 13) pulse width may be obtained by using the symmetry correction input (Pin 16).

Normally, Pin 16 is connected to Pin 4 (PWM OUT) and output 2's duty cycle is controlled by the PWM comparator, as is output 1's duty cycle. However, by not making this connection and driving Pin 16 externally, independent control of output 2's duty cycle from 0% to 50% (exclusive of dead time) can be obtained. Output 2 will be on (saturated) during its allowable conduction period if Pin 16 is at or above 2.4 V and will turn off when Pin 16 is at 0.7 V or less (TTL compatible).

Inhibit

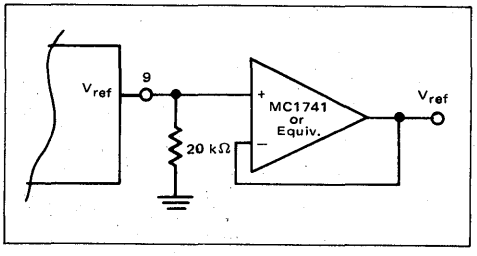
An inhibit function is also included in the MC3420. When Pin 15 is held at 0.7 V or less, both outputs of the MC3420 are forced off (non-conducting). In addition, this inhibit function disables an open-collector output, OSCILLATOR OUTPUT (Pin 14). This output normally switches at the same frequency as Output 1 with a constant 50% duty cycle, and can be used to implement various system features such as inrush current limiting (see Applications Information section).

APPLICATIONS INFORMATION

The Voltage Reference

The temperature coefficient of V_{ref} has been optimized for a 400 μA (≅20 kΩ) load. Different loadings of Pin 9 will result in decreased temperature stability. If increased current capability is required, an op amp buffer may be used, as shown in Figure 4, to prevent a decrease in V_{ref}'s temperature stability.

FIGURE 4



Output Frequency

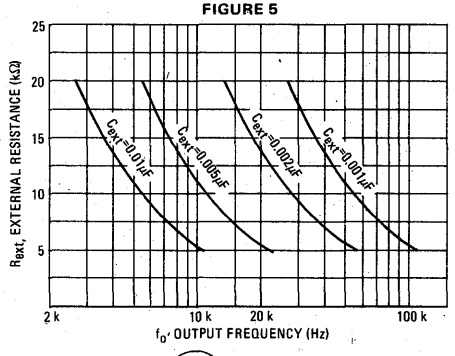
The values of R_{ext} and C_{ext} for a given output frequency, f_o, can be found from:

$$f_o \cong \frac{0.55}{R_{ext}\,C_{ext}}\ ;\ 5.0\ k\Omega \leq R_{ext} \leq 20\ k\Omega$$

or from the graph shown in Figure 5.

Note that f_o refers to the frequency of Output 1 (Pin 11) or Output 2 (Pin 13). The frequency of the ramp generator output waveform at Pin 8 will be twice f_o.

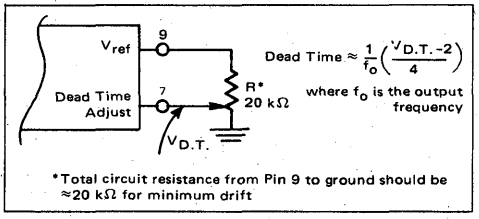
FIGURE 5



Dead Time

Figure 6 illustrates how to set or adjust the MC3420 outputs' dead time or maximum duty cycle. For minimum dead time drift with temperature or supply voltage, $V_{D.T.}$ should be derived from V_{ref} as shown.

FIGURE 6



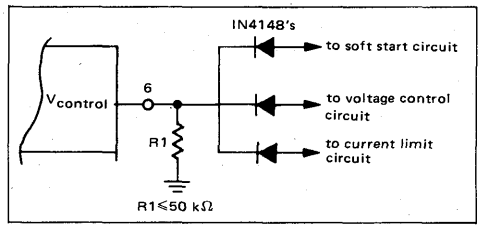
Connections to the $V_{control}$ Pin

In many systems, it is necessary to make multiple connections to the $V_{control}$ Pin in order to implement features in addition to voltage regulation such as current limiting, soft start, etc. These can be made by the use of a simple "diode-or" connection, as shown in Figure 7. This allows whichever control element is seeking the lowest PWM duty cycle to dominate. Note that a resistor, R1, whose value is ≤ 50 kΩ is placed from the $V_{control}$ Pin to ground. This is necessary to provide a dc path for the PWM comparator input bias current under all conditions.

Soft Start

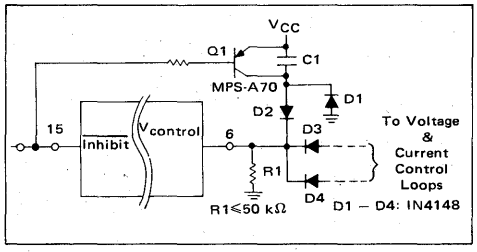
In most PWM switching supplies, a soft start feature is desired to prevent output voltage overshoots and magne-

FIGURE 7



tizing current imbalances in the power transformer primary. This feature forces the duty cycle of the switching elements to gradually increase from zero to their normal operating point during initial system power-up or after an inhibit. This feature can be easily implemented with the MC3420. One method is shown in Figure 8.

FIGURE 8



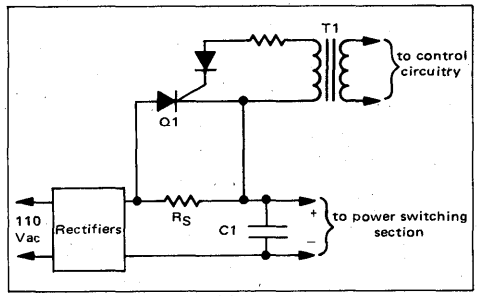
After an inhibit command or during power-up, the voltage on R1 and Pin 6 exponentially decays from V_{CC} toward ground with a time constant of R1C1, allowing a gradual increase in duty cycle. Diodes D2 – D4 provide a diode-or function at the $V_{control}$ Pin, while Q1 serves to reset the timing capacitor, C1, when an inhibit command is received thereby reinitializing the soft-start feature. D1 allows C1 to reset when power (V_{CC}) is turned off.

Inrush Current Limiting

Since many PWM switching supplies are operated directly off the rectified 110 Vac line with capacitive input filters, some means of preventing rectifier failure due to inrush surge currents is usually necessary. One method which can be used is shown in Figure 9.

In this circuit, a series resistor, R_S, is used to provide inrush surge current limiting. After the filter capacitor, C1, is charged, Q1 receives a trigger signal from the control circuitry through T1 and shorts R_S out of the circuit, eliminating its otherwise larger power dissipation. The trigger signal for Q1 may be derived from either the oscillator output (Pin 14) or one of the MC3420's outputs. If the oscillator output is used, it will be necessary

FIGURE 9

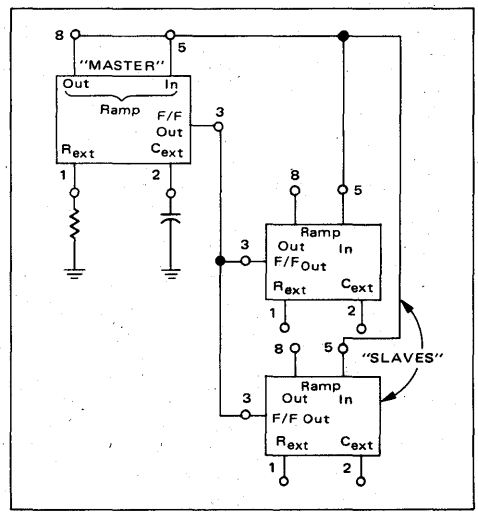


to provide a time delay on the inhibit pin to keep it low until the input filter capacitor, C1, has had time to charge, whereas the initial portion of the soft start timing cycle can be used for this delay if this signal is derived from one of the output pins. However, using the Oscillator Output Pin does offer the advantage that its waveform has a constant 50% duty cycle, independent of the outputs' duty cycle which can simplify the design of a drive circuit for T1.

Slaving

In some applications, as when one PWM inverter/converter is used to feed another, it may be desired that their frequencies be synchronized. This can be done with multiple MC3420s as shown in Figure 10. By omitting their R_{ext} and C_{ext}, up to two MC3420s may be slaved to a master MC3420.

FIGURE 10 – SLAVING THE MC3420



MC3422

Advance Information

SOLID STATE CURRENT LIMITER

Intended to protect sensitive circuitry from excessive current flow, this current limiter appears as a low impedance path with approximately 4.5 V drop until a current level of 225 mA is reached. At this point, the unit goes into a constant current mode preventing an increase in load current and protecting the load.

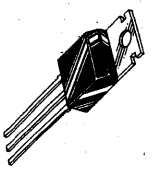
The high power dissipation in this mode causes the MC3422 die temperature to increase rapidly and when a temperature of about 125°C is reached, the device lowers the series current to about 15 mA to avoid destruction. The MC3422 will automatically reset itself to the normal operating mode when the fault condition is removed.

- Limiting Current – 225 mA Typ
- Thermal Shutdown
- Two Leads
- High Breakdown Voltage – 60 V Min

CURRENT LIMITER WITH THERMAL SHUTDOWN

SILICON MONOLITHIC INTEGRATED CIRCUIT

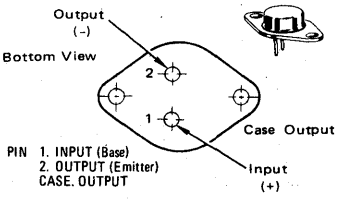
T SUFFIX
PLASTIC PACKAGE
CASE 313



PIN 1. INPUT
2. OUTPUT
3. N.C.

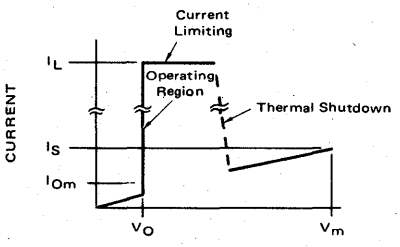
Heatsink surface connected to Pin 3.

R SUFFIX
METAL PACKAGE
CASE 80
TO-66



PIN 1. INPUT (Base)
2. OUTPUT (Emitter)
CASE. OUTPUT

FIGURE 1 – TYPICAL OPERATING AREA



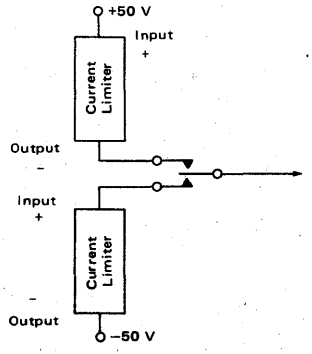
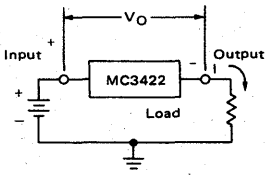


FIGURE 2 – CIRCUIT TO ELIMINATE CONTACT BURNING DUE TO CONTACT BUNCHING

TYPICAL CIRCUIT CONNECTION



ORDERING INFORMATION

Device	Temperature Range	Package
MC3422T	0 to +70°C	Plastic Power
MC3422R	0 to +70°C	Metal Power

This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Input Voltage	V_I	60	V
Load Current	I_L	Internally Limited	–
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature	T_J	Internally Limited	–
Storage Temperature Range Plastic Package Metal Package	T_{stg}	 –65 to +150 –65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typical	Unit
Thermal Resistance, Junction to Case Metal Package Plastic Package	$R_{\theta JC}$	 7.0 5.0	°C/W
Thermal Resistance, Junction to Ambient Metal Package Plastic Package	$R_{\theta JA}$	 50 75	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Limiting Current (V_f = 4.8 V) (V_f = 15 V)	I_L	 150 –	 225 225	 – 300	mA
Forward Voltage Drop (I_L = 1.5 mA) (I_L = 0.5 mA)	V_f	 3.8 –	 4.3 4.3	 – 4.5	V
Output Resistance (Non-Limiting Mode) (I_L = 60 mA to 10 mA)	r_o	–	1.0	2.0	Ohms
Shutdown Current (V_f = 60 V) (After Thermal Shutdown)	I_s	–	15	20	mA
Maximum Applied Voltage	V_m	–	–	60	V
Temperature Coefficient of Forward Voltage (I_L = 10 mA)	$\Delta V_f/\Delta T$	–	±1.0	–	mV/°C
Temperature Coefficient of Limiting Current	$\Delta I_L/\Delta T$	–	0.8	–	mA/°C

FIGURE 3 – LIMIT REED CONTACT PEAK CURRENT

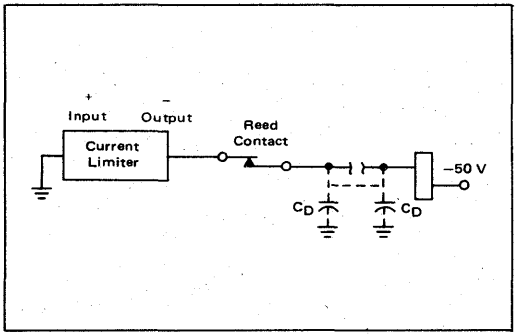
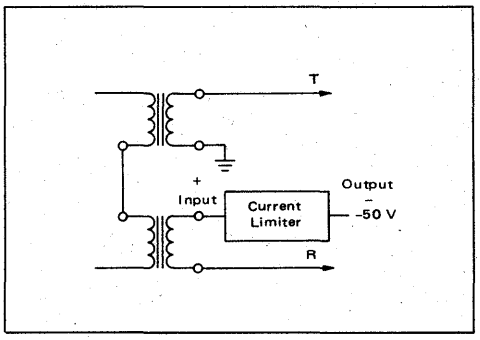


FIGURE 4 – LIMIT LINE LOOP CURRENTS



MC7700C series

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

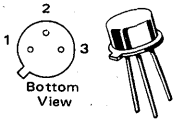
MC7700C SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC7700C Series positive voltage regulators are identical to the popular MC7800C Series devices, except that they are specified for only half the output current. Like the MC7800C devices, the MC7700C three-terminal regulators are intended for local, on-card voltage regulation.

Internal current limiting, thermal shutdown circuitry and safe-area compensation for the internal pass transistor combine to make these devices remarkably rugged under most operating conditions. Maximum output current, with adequate heatsinking is 750 mA.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 313 and Case 79 (TO-220 and Hermetic TO-39)

G SUFFIX
METAL PACKAGE
CASE 79
TO-39

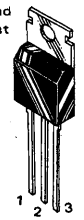


Pin 1. Input
2. Output
3. Ground

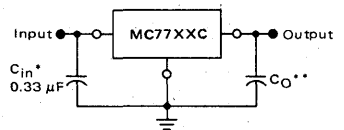
Case connected to Pin 3.

T SUFFIX
PLASTIC PACKAGE
CASE 313
(TO-220 Type)

Pin 1. Input
2. Ground
3. Output



STANDARD APPLICATION



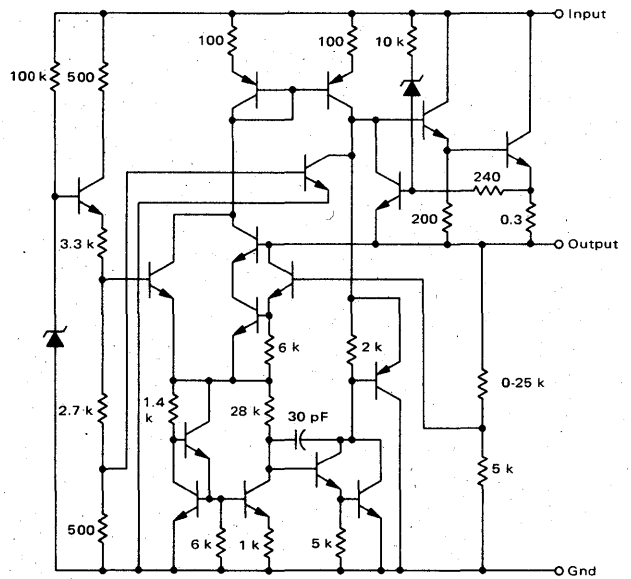
A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

REPRESENTATIVE SCHEMATIC DIAGRAM



ORDERING INFORMATION		
DEVICE	TEMPERATURE RANGE	PACKAGE
MC77XXCG	T_J = 0° C to +150°C	Metal Can
MC77XXCT	T_J = 0° C to +150°C	Plastic Power
XX indicates nominal voltage		

TYPE NO./VOLTAGE

MC7705C	5.0 Volts
MC7706C	6.0 Volts
MC7708C	8.0 Volts
MC7712C	12 Volts
MC7715C	15 Volts
MC7718C	18 Volts
MC7720C	20 Volts
MC7724C	24 Volts

MC7700C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V - 18 V) (20 V - 24 V)	V_I	35 40	Vdc
Power Dissipation (Package Limitation) Plastic Package T_A = 25°C Derate above T_A = 25°C T_C = 25°C Derate above T_C = 110°C Metal Package T_A = 25°C Derate above T_A = 25°C T_C = 25°C Derate above T_C = 85°C	 P_D θ_{JA} P_D θ_{JC} P_D θ_{JA} P_D θ_{JC}	 Internally Limited 70 Internally Limited 5.0 Internally Limited 185 Internally Limited 25	 °C/W °C/W °C/W °C/W
Operating Junction Temperature Range	T_J	0 to +125	°C
Operating Ambient Temperature Range	T_A	0 to +85	°C
Storage Temperature Range Plastic Package Metal Package	T_{stg}	 −65 to +150 −65 to +150	°C

MC7705C ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 250 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	Vdc
Line Regulation (T_J = +25°C, I_O = 50 mA) 7.0 Vdc ≤ V_I ≤ 25 Vdc 8.0 Vdc ≤ V_I ≤ 12 Vdc (T_J = +25°C, I_O = 250 mA) 7.0 Vdc ≤ V_I ≤ 25 Vdc 8.0 Vdc ≤ V_I ≤ 12 Vdc	Reg_{line}	 – – – –	 7.0 2.0 35 8.0	 50 25 100 50	 mV mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 750 mA 125 mA ≤ I_O ≤ 375 mA	Reg_{load}	 – –	 11 4.0	 100 50	mV
Output Voltage (7.0 Vdc ≤ V_I ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 500 mA, P ≤ P_{max}*)	V_O	4.75	–	5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change 7.0 Vdc ≤ V_I ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 750 mA	ΔI_{IB}	 – –	 – –	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	70	–	dB
Input-Output Voltage Differential I_O = 500 mA, T_J = +25°C	V_I-V_O	–	2.0	–	Vdc
Output Resistance (I_O = 250 mA)	r_o	–	30	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	375	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

*P_{max} = 7.5 W for Case 313
P_{max} = 5.0 W for Case 79

MC7706C ELECTRICAL CHARACTERISTICS (V_I = 11 V, I_O = 250 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	Vdc
Line Regulation	Reg_{line}				
(T_J = +25°C, I_O = 50 mA)					
8.0 Vdc ≤ V_I ≤ 25 Vdc		–	9.0	60	mV
9.0 Vdc ≤ V_I ≤ 13 Vdc		–	3.0	30	
(T_J = +25°C, I_O = 250 mA)					
8.0 Vdc ≤ V_I ≤ 25 Vdc		–	43	120	mV
9.0 Vdc ≤ V_I ≤ 13 Vdc		–	10	60	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 750 mA		–	13	120	
125 mA ≤ I_O ≤ 375 mA		–	5.0	60	
Output Voltage	V_O	5.7	–	6.3	Vdc
8.0 Vdc ≤ V_I ≤ 21 Vdc, 5.0 mA ≤ I_O ≤ 500 mA, P ≤ P_{max}*					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
8.0 Vdc ≤ V_I ≤ 25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 750 mA		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	45	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	24	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential	V_I-V_O	–	2.0	–	Vdc
I_O = 500 mA, T_J = +25°C					
Output Resistance (I_O = 250 mA)	r_o	–	35	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	275	–	mA
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C					

MC7708C ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 250 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	Vdc
Line Regulation	Reg_{line}				
(T_J = +25°C, I_O = 50 mA)					
10.5 Vdc ≤ V_I ≤ 25 Vdc		–	12	80	mV
11 Vdc ≤ V_I ≤ 17 Vdc		–	5.0	40	
(T_J = +25°C, I_O = 250 mA)					
10.5 Vdc ≤ V_I ≤ 25 Vdc		–	50	160	mV
11 Vdc ≤ V_I ≤ 17 Vdc		–	22	80	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 750 mA		–	26	160	
125 mA ≤ I_O ≤ 375 mA		–	9.0	80	
Output Voltage	V_O	7.6	–	8.4	Vdc
10.5 Vdc ≤ V_I ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 500 mA, P ≤ P_{max}*					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
10.5 Vdc ≤ V_I ≤ 25 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 750 mA		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	52	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	32	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	62	–	dB
Input-Output Voltage Differential	V_I-V_O	–	2.0	–	Vdc
I_O = 500 mA, T_J = +25°C					
Output Resistance (I_O = 250 mA)	r_o	–	40	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	225	–	mA
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C					

*P_{max} = 7.5 W for Case 313
P_{max} = 5.0 W for Case 79

MC7712C ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 250 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	Vdc
Line Regulation	Reg_{line}				
(T_J = +25°C, I_O = 50 mA)					
14.5 Vdc ≤ V_I ≤ 30 Vdc		–	13	120	mV
16 Vdc ≤ V_I ≤ 22 Vdc		–	6.0	60	
(T_J = +25°C, I_O = 250 mA)					
14.5 Vdc ≤ V_I ≤ 30 Vdc		–	55	240	mV
16 Vdc ≤ V_I ≤ 22 Vdc		–	24	120	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 750 mA		–	46	240	
125 mA ≤ I_O ≤ 375 mA		–	17	120	
Output Voltage 14.5 Vdc ≤ V_I ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 500 mA, P ≤ P_{max}*	V_O	11.4	–	12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
14.5 Vdc ≤ V_I ≤ 30 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 750 mA		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	75	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	48	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	61	–	dB
Input-Output Voltage Differential I_O = 500 mA, T_J = +25°C	V_I-V_O	–	2.0	–	Vdc
Output Resistance (I_O = 250 mA)	r_o	–	75	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	175	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7715C ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 250 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	Vdc
Line Regulation	Reg_{line}				
(T_J = +25°C, I_O = 50 mA)					
17.5 Vdc ≤ V_I ≤ 30 Vdc		–	14	150	mV
20 Vdc ≤ V_I ≤ 26 Vdc		–	6.0	75	
(T_J = +25°C, I_O = 250 mA)					
17.5 Vdc ≤ V_I ≤ 30 Vdc		–	57	300	mV
20 Vdc ≤ V_I ≤ 26 Vdc		–	27	150	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 750 mA		–	68	300	
125 mA ≤ I_O ≤ 375 mA		–	25	150	
Output Voltage 17.5 Vdc ≤ V_I ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 500 mA, P ≤ P_{max}*	V_O	14.25	–	15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
17.5 Vdc ≤ V_I ≤ 30 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 750 mA		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	90	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	60	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	60	–	dB
Input-Output Voltage Differential I_O = 500 mA, T_J = +25°C	V_I-V_O	–	2.0	–	Vdc
Output Resistance (I_O = 250 mA)	r_o	–	95	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	115	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

*P_{max} = 7.5 W for Case 313
P_{max} = 5.0 W for Case 79

MC7718C ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 250 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	Vdc
Line Regulation	Reg_{line}				
(T_J = +25°C, I_O = 50 mA)					
21 Vdc ≤ V_I ≤ 33 Vdc		–	25	180	mV
24 Vdc ≤ V_I ≤ 30 Vdc		–	10	90	
(T_J = +25°C, I_O = 250 mA)					
21 Vdc ≤ V_I ≤ 33 Vdc		–	90	360	mV
24 Vdc ≤ V_I ≤ 30 Vdc		–	50	180	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA		–	110	360	
125 mA ≤ I_O ≤ 375 mA		–	55	180	
Output Voltage	V_O	17.1	–	18.9	Vdc
21 Vdc ≤ V_I ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 500 mA, P ≤ P_{max}*					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.5	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
21 Vdc ≤ V_I ≤ 33 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 500 mA		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	110	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	72	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	59	–	dB
Input-Output Voltage Differential	V_I-V_O	–	2.0	–	Vdc
I_O = 500 mA, T_J = +25°C					
Output Resistance (I_O = 250 mA)	r_o	–	110	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	100	–	mA
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C					

MC7720C ELECTRICAL CHARACTERISTICS (V_I = 29 V, I_O = 250 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	19.2	20	20.8	Vdc
Line Regulation	Reg_{line}				
(T_J = +25°C, I_O = 50 mA)					
23 Vdc ≤ V_I ≤ 35 Vdc		–	27	200	mV
26 Vdc ≤ V_I ≤ 32 Vdc		–	11	100	
(T_J = +25°C, I_O = 250 mA)					
23 Vdc ≤ V_I ≤ 35 Vdc		–	100	400	mV
26 Vdc ≤ V_I ≤ 32 Vdc		–	56	200	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA		–	123	400	
125 mA ≤ I_O ≤ 375 mA		–	65	200	
Output Voltage	V_O	19	–	21	Vdc
23 Vdc ≤ V_I ≤ 35 Vdc, 5.0 mA ≤ I_O ≤ 500 mA, P ≤ P_{max}*					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.5	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
23 Vdc ≤ V_I ≤ 35 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 750 mA		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	130	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	80	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	58	–	dB
Input-Output Voltage Differential	V_I-V_O	–	2.0	–	Vdc
I_O = 500 mA, T_J = +25°C					
Output Resistance (I_O = 250 mA)	r_o	–	123	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	90	–	mA
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C					

*P_{max} = 7.5 W for Case 313
P_{max} = 5.0 W for Case 79

MC7724C ELECTRICAL CHARACTERISTICS (V_I = 33, I_O = 250 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	23	24	25	Vdc
Line Regulation (T_J = +25°C, I_O = 50 mA) 27 Vdc ≤ V_I ≤ 38 Vdc 30 Vdc ≤ V_I ≤ 36 Vdc (T_J = +25°C, I_O = 250 mA) 27 Vdc ≤ V_I ≤ 38 Vdc 30 Vdc ≤ V_I ≤ 36 Vdc	Reg_{line}	 – – – –	 31 14 118 70	 240 120 480 240	 mV mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA 125 mA ≤ I_O ≤ 375 mA	Reg_{load}	 – –	 150 85	mV 480 240	mV
Output Voltage 27 Vdc ≤ V_I ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 500 mA, P ≤ P_{max}*	V_O	22.8	–	25.2	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.6	8.0	mA
Input Bias Current Change 27 Vdc ≤ V_I ≤ 38 Vdc 5.0 mA ≤ I_O ≤ 500 mA	ΔI_{IB}	 – –	 – –	mA 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	170	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	96	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	56	–	dB
Input-Output Voltage Differential I_O = 500 mA, T_J = +25°C	V_I-V_O	–	2.0	–	Vdc
Output Resistance (I_O = 250 mA)	r_o	–	150	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	150	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

*P_{max} = 7.5 W for Case 313

P_{max} = 5.0 W for Case 79

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}} \geq V_I I_S - V_O I_O$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}$(Typ) = Typical Thermal Resistance Junction to Ambient

I_S = Total Supply Current

DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

4

TYPICAL PERFORMANCE CURVES

FIGURE 1 – WORST CASE POWER DISSIPATION AMBIENT TEMPERATURE TO-220 (CASE 313)

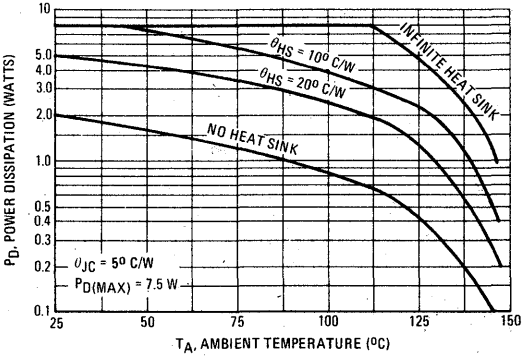


FIGURE 2 – WORST CASE POWER DISSIPATION AMBIENT TEMPERATURE TO-39 (CASE 79)

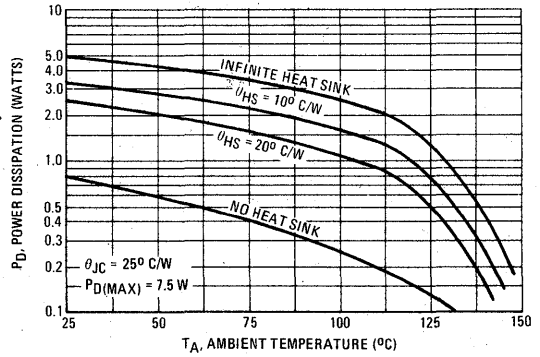


FIGURE 3 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

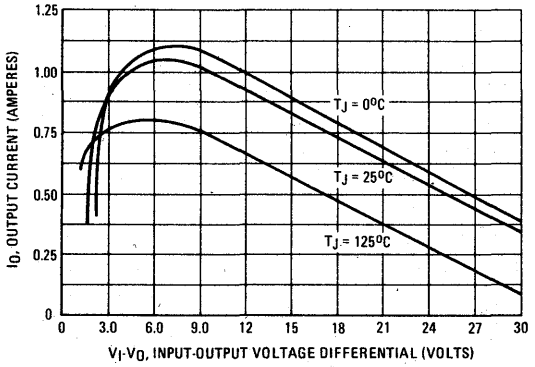
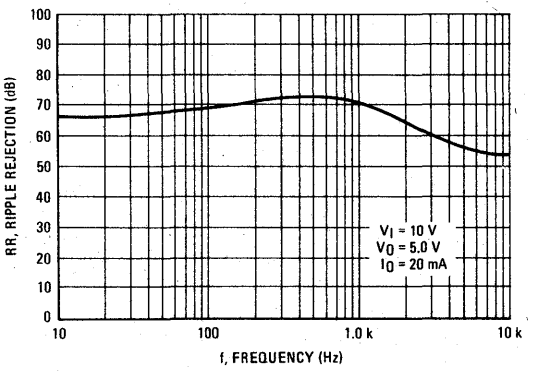


FIGURE 4 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



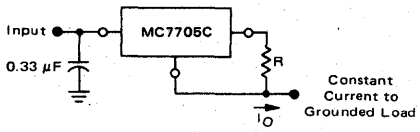
APPLICATIONS INFORMATION

Design Considerations

The MC7700C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 5 – CURRENT REGULATOR



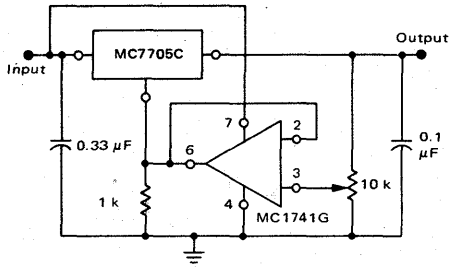
The MC7700C regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7705C is chosen in this application. Resistor R determines the current as follows:

$$I_O \cong \frac{5\ V}{R} + I_Q$$

I_Q = 1.5 mA over line and load changes

For example, a 500 mA current source would require R to be a 10-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7 volts.

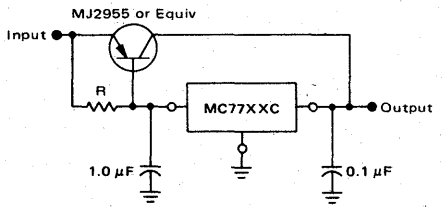
FIGURE 6 ADJUSTABLE OUTPUT REGULATOR)R



V_O, 7.0 V to 20 V
$V_{IN} - V_O \geq 2.0$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

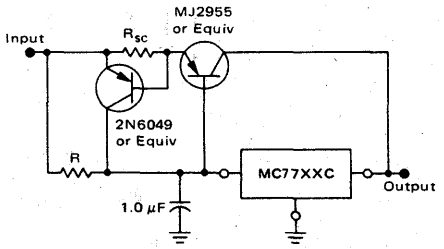
FIGURE 7 – CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC7700C series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 8 – SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 7 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{sc}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a two-ampere plastic power transistor is specified.

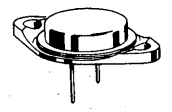
MC7800C Series

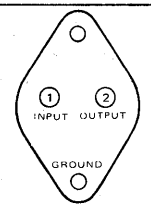
THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

MC7800C SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC7800C Series of three-terminal positive voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. Available in seven fixed output voltage options from 5.0-to-24 volts, these regulators employ internal current limiting, thermal shutdown, and safe area compensation — making them essentially blow-out proof. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere. The last two digits of the part number indicate nominal output voltage.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 313 and Case 11 (TO-220 and Hermetic TO-3)



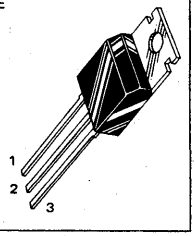


K SUFFIX
METAL PACKAGE
CASE 11-01
(TO-3 TYPE)

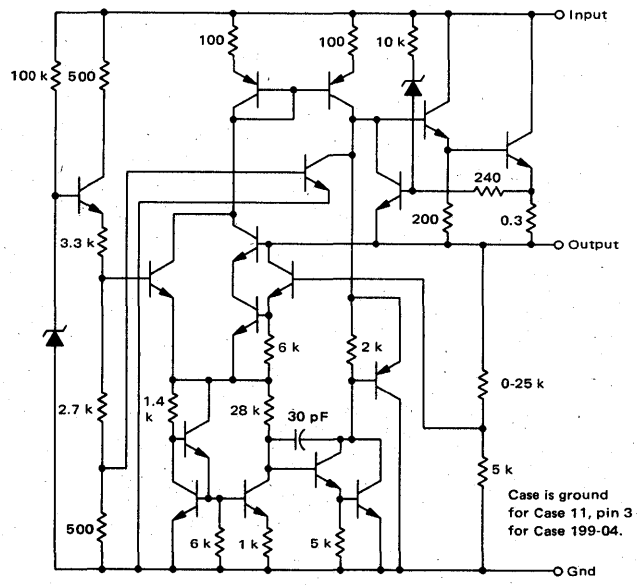
Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

T SUFFIX
PLASTIC PACKAGE
CASE 313
TO-220 Type

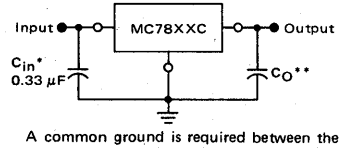
Pin 1. Input
2. Ground
3. Output



SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

XX indicates nominal voltage

TYPE NO./VOLTAGE

MC7805C 5.0 Volts	MC7808C 8.0 Volts	MC7818C 18 Volts
MC7806C 6.0 Volts	MC7812C 12 Volts	MC7824C 24 Volts
	MC7815C 15 Volts	

ORDERING INFORMATION		
DEVICE	TEMPERATURE RANGE	PACKAGE
MC78XXCK	T_J = 0° C to +150° C	Metal Power
MC78XXCT	T_J = 0° C to +150° C	Plastic Power

MC7800C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V - 18 V) (24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	15.4	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	65	°C/W
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +95°C (See Figure 1)	$1/\theta_{JC}$	200	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W
Metal Package			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	22.5	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	45	°C/W
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +65°C (See Figure 2)	$1/\theta_{JC}$	182	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.5	°C/W
Storage Junction Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

MC7805C ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
7.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	7.0	50	
8.0 Vdc ≤ V_{in} ≤ 12 Vdc		–	2.0	25	
(T_J = +25°C, I_O = 500 mA)					
7.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	35	100	
8.0 Vdc ≤ V_{in} ≤ 12 Vdc		–	8.0	50	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	11	100	
250 mA ≤ I_O ≤ 750 mA		–	4.0	50	
Output Voltage	V_O				Vdc
(7.0 Vdc ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)		4.75	–	5.25	
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
7.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k HRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	70	–	dB
Input-Output Voltage Differential	$V_{in}-V_O$				Vdc
(I_O = 1.0 A, T_J = +25°C)		–	2.0	–	
Output Resistance (I_O = 500 mA)	R_O	–	30	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	750	–	mA
Average Temperature Coefficient of Output Voltage	TCV_O				mV/°C
I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C		–	-1.0	–	

MC7806C ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
8.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	9.0	60	
9.0 Vdc ≤ V_{in} ≤ 13 Vdc		–	3.0	30	
(T_J = +25°C, I_O = 500 mA)					
8.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	43	120	
9.0 Vdc ≤ V_{in} ≤ 13 Vdc		–	10	60	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	13	120	
250 mA ≤ I_O ≤ 750 mA		–	5.0	60	
Output Voltage	V_O				Vdc
(8.0 Vdc ≤ V_{in} ≤ 21 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)		5.7	–	6.3	
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
8.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	45	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	24	mV/1.0 k HRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential	$V_{in}-V_O$				Vdc
(I_O = 1.0 A, T_J = +25°C)		–	2.0	–	
Output Resistance (I_O = 500 mA)	R_O	–	35	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	550	–	mA
Average Temperature Coefficient of Output Voltage	TCV_O				mV/°C
I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C		–	−1.0	–	

MC7808C ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
10.5 Vdc ≤ V_{in} ≤ 25 Vdc		–	12	80	
11 Vdc ≤ V_{in} ≤ 17 Vdc		–	5.0	40	
(T_J = +25°C, I_O = 500 mA)					
10.5 Vdc ≤ V_{in} ≤ 25 Vdc		–	50	160	
11 Vdc ≤ V_{in} ≤ 17 Vdc		–	22	80	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	26	160	
250 mA ≤ I_O ≤ 750 mA		–	9.0	80	
Output Voltage	V_O				Vdc
(10.5 Vdc ≤ V_{in} ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)		7.6	–	8.4	
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
10.5 Vdc ≤ V_{in} ≤ 25 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	52	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	32	mV/1.0 k HRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	62	–	dB
Input-Output Voltage Differential	$V_{in}-V_O$				Vdc
(I_O = 1.0 A, T_J = +25°C)		–	2.0	–	
Output Resistance (I_O = 500 mA)	R_O	–	40	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	450	–	mA
Average Temperature Coefficient of Output Voltage	TCV_O				mV/°C
I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C		–	-1.0	–	

MC7812C ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	Vdc
Input Regulation (T_J = +25°C, I_O = 100 mA) 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc (T_J = +25°C, I_O = 500 mA) 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc	Reg_{in}	 – – – –	 13 6.0 55 24	 120 60 240 120	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 46 17	 240 120	mV
Output Voltage (14.5 Vdc ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)	V_O	11.4	–	12.6	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.4	8.0	mA
Quiescent Current Change 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	75	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	48	mV/1.0kHRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	61	–	dB
Input-Output Voltage Differential (I_O = 1.0 A, T_J = +25°C)	V_{in}-V_O	–	2.0	–	Vdc
Output Resistance (I_O = 500 mA)	R_O	–	75	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	350	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	TCV_O	–	-1.0	–	mV/°C

MC7815C ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	Vdc
Input Regulation (T_J = +25°C, I_O = 100 mA) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc (T_J = +25°C, I_O = 500 mA) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc	Reg_{in}	 – – – –	 14 6.0 57 27	 150 75 300 150	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 68 25	 300 150	mV
Output Voltage (17.5 Vdc ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)	V_O	14.25	–	15.75	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.4	8.0	mA
Quiescent Current Change 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	90	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	60	mV/1.0kHRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	60	–	dB
Input-Output Voltage Differential (I_O = 1.0 A, T_J = +25°C)	V_{in}-V_O	–	2.0	–	Vdc
Output Resistance (I_O = 500 mA)	R_O	–	95	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	230	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	TCV_O	–	-1.0	–	mV/°C

MC7818C ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	Vdc
Input Regulation (T_J = +25°C, I_O = 100 mA) 21 Vdc ≤ V_{in} ≤ 33 Vdc 24 Vdc ≤ V_{in} ≤ 30 Vdc (T_J = +25°C, I_O = 500 mA) 21 Vdc ≤ V_{in} ≤ 33 Vdc 24 Vdc ≤ V_{in} ≤ 30 Vdc	Reg_{in}	 – – – –	 25 10 90 50	 180 90 360 180	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 110 55	 360 180	mV
Output Voltage (21 Vdc ≤ V_{in} ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)	V_O	17.1	–	18.9	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.5	8.0	mA
Quiescent Current Change 21 Vdc ≤ V_{in} ≤ 33 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	110	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	72	mV/1.0kHRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	59	–	dB
Input-Output Voltage Differential (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	 –	 2.0	 –	Vdc
Output Resistance (I_O = 500 mA)	R_O	–	110	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	200	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	TCV_O	 –	 -1.0	 –	mV/°C

MC7824C ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	23	24	25	Vdc
Input Regulation (T_J = +25°C, I_O = 100 mA) 27 Vdc ≤ V_{in} ≤ 38 Vdc 30 Vdc ≤ V_{in} ≤ 36 Vdc (T_J = +25°C, I_O = 500 mA) 27 Vdc ≤ V_{in} ≤ 38 Vdc 30 Vdc ≤ V_{in} ≤ 36 Vdc	Reg_{in}	 – – – –	 31 14 118 70	 240 120 480 240	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 150 85	 480 240	mV
Output Voltage (27 Vdc ≤ V_{in} ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)	V_O	22.8	–	25.2	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.6	8.0	mA
Quiescent Current Change 27 Vdc ≤ V_{in} ≤ 38 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	170	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	96	mV/1.0kHRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	56	–	dB
Input-Output Voltage Differential (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	–	2.0	–	Vdc
Output Resistance (I_O = 500 mA)	R_O	–	150	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	150	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	TCV_O	 –	 -1.0	 –	mV/°C

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 1 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 313)

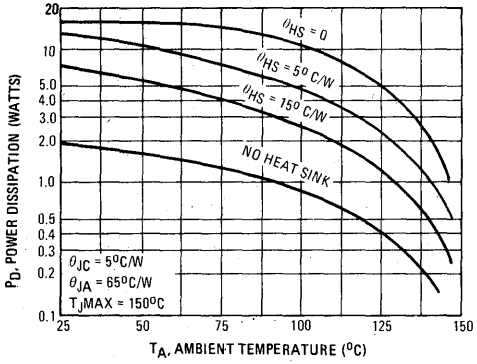


FIGURE 2 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE (Case 11)

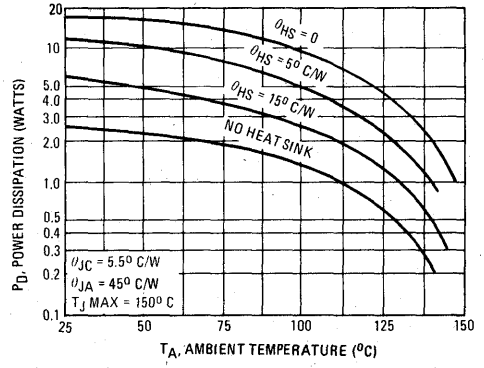


FIGURE 3 – INPUT OUTPUT DIFFERENTIAL AS A FUNCTION OF JUNCTION TEMPERATURE

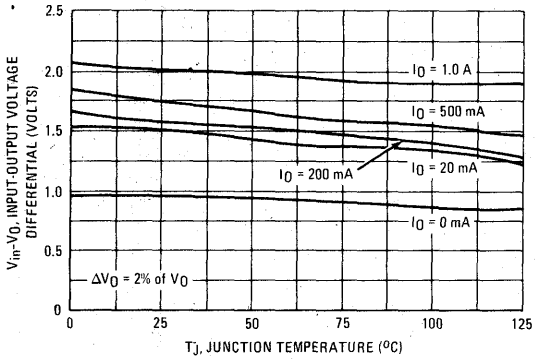


FIGURE 4 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

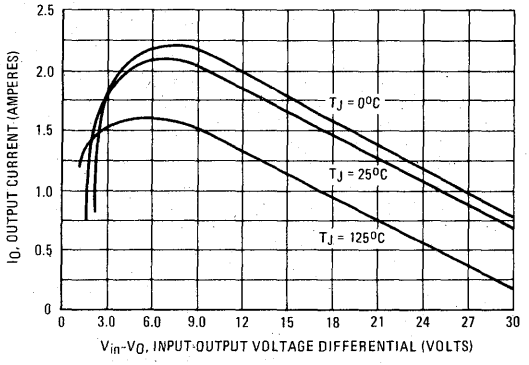


FIGURE 5 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

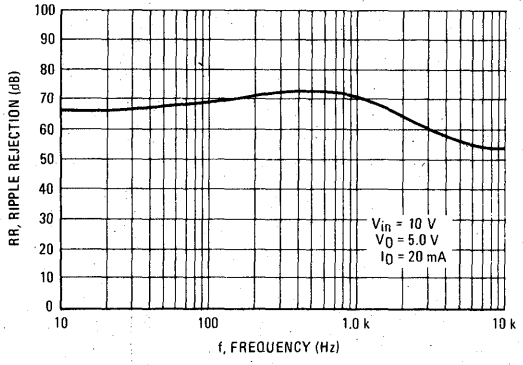
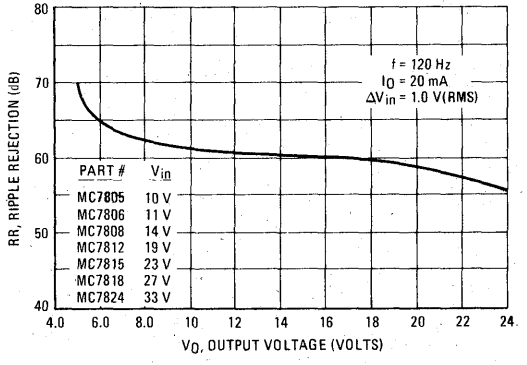


FIGURE 6 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES



TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

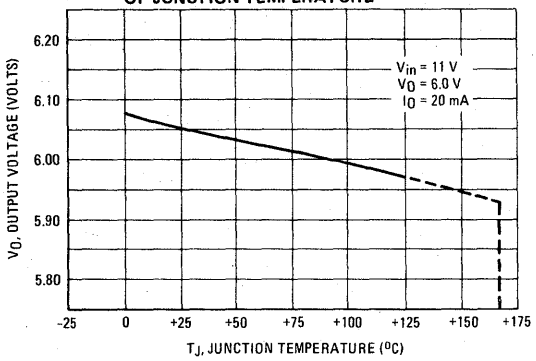


FIGURE 8 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE

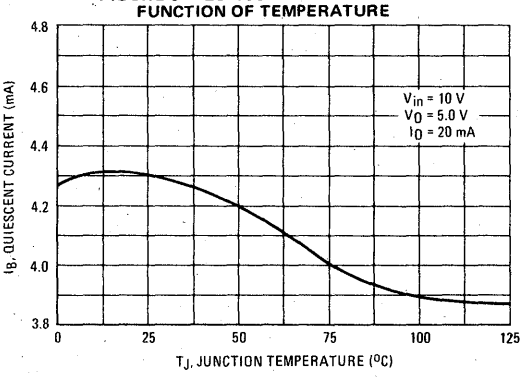
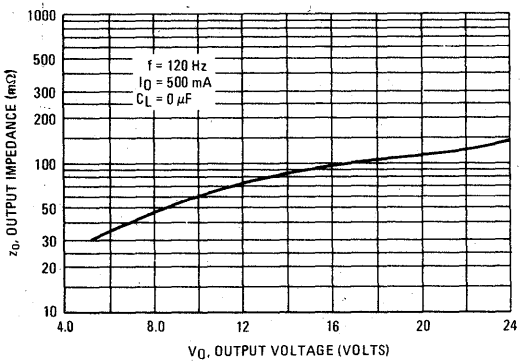


FIGURE 9 – OUTPUT IMPEDANCE AS A FUNCTION OF OUTPUT VOLTAGE



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}} \geq V_I I_S - V_O I_O$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}$(Typ) = Typical Thermal Resistance Junction to Ambient

I_S = Total Supply Current

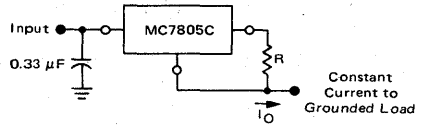
APPLICATIONS INFORMATION

Design Considerations

The MC7800C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 10 – CURRENT REGULATOR



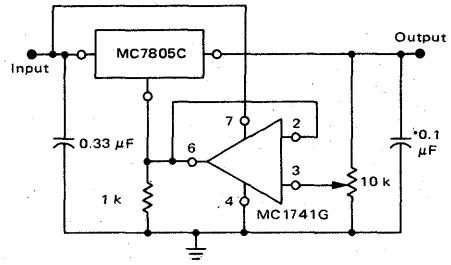
The MC7800C regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\ V}{R} + I_Q$$

$I_Q \cong 1.5$ mA over line and load changes

For example, a 1-ampere current source would require R to be a 5-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7 volts.

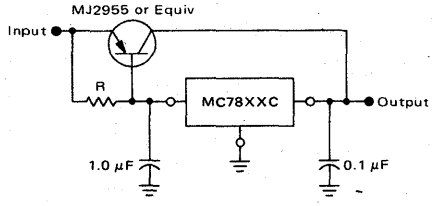
FIGURE 11 – ADJUSTABLE OUTPUT REGULATOR



V_O, 7.0 V to 20 V
$V_{IN} - V_O \geq 2.0$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

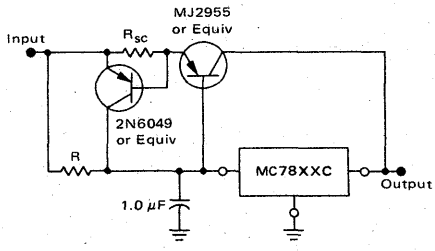
FIGURE 12 – CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC7800C series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 13 – SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 12 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

MC78L00C, AC Series

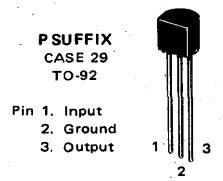
THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

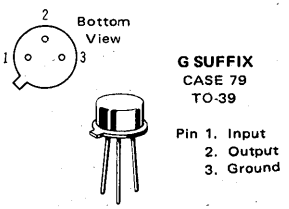
The MC78L00 Series of positive voltage regulators are inexpensive, easy-to-use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

These devices offer a substantial performance advantage over the traditional zener diode-resistor combination. Output impedance is greatly reduced and quiescent current is substantially reduced.

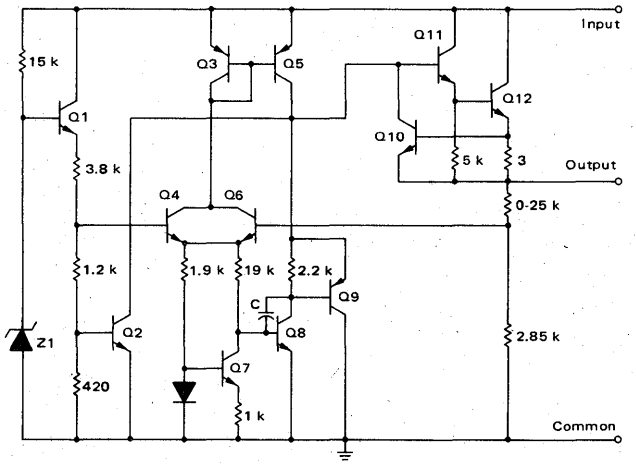
- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

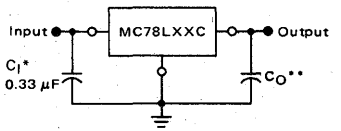




REPRESENTATIVE CIRCUIT SCHEMATIC



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_I is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

Device No. ±10%	Device No. ±5%	Nominal Voltage
—	MC78L02AC	2.6
MC78L05C	MC78L05AC	5.0
MC78L08C	MC78L08AC	8.0
MC78L12C	MC78L12AC	12
MC78L15C	MC78L15AC	15
MC78L18C	MC78L18AC	18
MC78L24C	MC78L24AC	24

ORDERING INFORMATION		
Device	Temperature Range	Package
MC78LXXACG	T_J = 0°C to +150°C	Metal Can
MC78LXXACP	T_J = 0°C to +150°C	Plastic Transistor
MC78LXXCG	T_J = 0°C to +150°C	Metal Can
MC78LXXCP	T_J = 0°C to +150°C	Plastic Transistor
XX indicates nominal voltage		

MC78L00 Series MAXIMUM RATINGS (T_A = +125°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.6 V – 8.0 V) (12 V – 18 V) (24 V)	V_I	30 35 40	Vdc
Storage Junction Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

MC78L02AC ELECTRICAL CHARACTERISTICS (V_I = 9.0 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C ≤ T_J ≤ +125°C unless otherwise noted.)

Characteristic	Symbol	MC7802AC Min	MC7802AC Typ	MC7802AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	2.5	2.6	2.7	Vdc
Input Regulation (T_J = +25°C) 4.75 Vdc ≤ V_I ≤ 20 Vdc 5.0 Vdc ≤ V_I ≤ 20 Vdc	Reg_{line}	 – –	 40 30	 100 75	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 10 4.0	 50 25	mV
Output Voltage (4.75 Vdc ≤ V_I ≤ 20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (4.75 Vdc ≤ V_I ≤ 20 Vdc, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 2.45 2.45	 – –	 2.75 2.75	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_B	 – –	 3.6 –	 6.0 5.5	mA
Input Bias Current Change (5.0 Vdc ≤ V_{in} ≤ 20 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_B	 – –	 – –	 2.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	30	–	μV
Ripple Rejection (f = 120 Hz, 6.0 V ≤ V_{in} ≤ 16 V, T_J = 25°C)	RR	43	51	–	dB
Input-Output Voltage Differential (T_J = 25°C)	V_I/V_O	–	1.7	–	Vdc

MC78L05C, MC78L05AC ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L05C Min	MC78L05C Typ	MC78L05C Max	MC78L05AC Min	MC78L05AC Typ	MC78L05AC Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.6	5.0	5.4	4.8	5.0	5.2	Vdc
Input Regulation (T_J = +25°C, I_O = 40 mA) 7.0 Vdc ≤ V_I ≤ 20 Vdc 8.0 Vdc ≤V_I ≤ 20 Vdc	Reg_{line}	 – –	 55 45	 200 150	 – –	 55 45	 150 100	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 11 5.0	 60 30	 – –	 11 5.0	 60 30	mV
Output Voltage (7.0 Vdc ≤ V_I ≤ 20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 10 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 4.5 4.5	 – –	 5.5 5.5	 4.75 4.75	 – –	 5.25 5.25	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.8 –	 6.0 5.5	 – –	 3.8 –	 6.0 5.5	mA
Input Bias Current Change (8.0 Vdc ≤ V_I ≤ 20 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.2	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	40	–	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	12	–	–	12	–	mV/1.0 k Hrs
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 8.0 V ≤ V_I ≤ 18 V, T_J = +25°C)	RR	40	49	–	41	49	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L08C, MC78L08AC ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L08C			MC78L08AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	7.36	8.0	8.64	7.7	8.0	8.3	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
10.5 Vdc ≤ V_I ≤ 23 Vdc		–	20	200	–	20	175	
11 Vdc ≤ V_I ≤ 23 Vdc		–	12	150	–	12	125	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	15	80	–	15	80	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	6.0	40	–	8.0	40	
Output Voltage	V_O							Vdc
(10.5 Vdc ≤ V_I ≤ 23 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		7.2	–	8.8	7.6	–	8.4	
(V_I = 14 V, 1.0 mA ≤ I_O ≤ 70 mA)		7.2	–	8.8	7.6	–	8.4	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.0	6.0	–	3.0	6.0	
(T_J = +125°C)		–	–	5.5	–	–	5.5	
Input Bias Current Change	ΔI_{IB}							mA
(11 Vdc ≤ V_I ≤ 23 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	52	–	–	60	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	20	–	–	20	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 12 V ≤ V_I ≤ 23 V, T_J = +25°C)	RR	36	55	–	37	57	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L12C, MC78L12AC ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC78L12C			MC78L12AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	11.1	12	12.9	11.5	12	12.5	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
14.5 Vdc ≤ V_I ≤ 27 Vdc		–	120	250	–	120	250	
16 Vdc ≤ V_I ≤ 27 Vdc		–	100	200	–	100	200	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	20	100	–	20	100	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	10	50	–	10	50	
Output Voltage	V_O							Vdc
(14.5 Vdc ≤ V_I ≤ 27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		10.8	–	13.2	11.4	–	12.6	
(V_I = 19 V, 1.0 mA ≤ I_O ≤ 70 mA)		10.8	–	13.2	11.4	–	12.6	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	4.2	6.5	–	4.2	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(16 Vdc ≤ V_I ≤ 27 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	80	–	–	80	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	24	–	–	24	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = +25°C)	RR	36	42	–	37	42	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L15C, MC78L15AC ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC78L15C			MC78L15AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	13.8	15	16.2	14.4	15	15.6	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
17.5 Vdc ≤ V_I ≤ 30 Vdc		–	130	300	–	130	300	
20 Vdc ≤ V_I ≤ 30 Vdc		–	110	250	–	110	250	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	25	150	–	25	150	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	12	75	–	12	75	
Output Voltage	V_O							Vdc
(17.5 Vdc ≤ V_I ≤ 30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		13.5	–	16.5	14.25	–	15.75	
(V_I = 23 V, 1.0 mA ≤ I_O ≤ 70 mA)		13.5	–	16.5	14.25	–	15.75	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	4.4	6.5	–	4.4	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(20 Vdc ≤ V_I ≤ 30 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	90	–	–	90	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	30	–	–	30	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = +25°C)	RR	33	39	–	34	39	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L18C, MC78L18AC ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC78L18C			MC78L18AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	16.6	18	19.4	17.3	18	18.7	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
21.4 Vdc ≤ V_I ≤ 33 Vdc		–	32	325				
20.7 Vdc ≤ V_I ≤ 33 Vdc					–	45	325	
22 Vdc ≤ V_I ≤ 33 Vdc		–	27	275				
21 Vdc ≤ V_I ≤ 33 Vdc					–	35	275	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	30	170	–	30	170	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	15	85	–	15	85	
Output Voltage	V_O							Vdc
(21.4 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		16.2	–	17.8				
(20.7 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)					17.1	–	18.9	
(V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)		16.2	–	17.8				
(V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)					17.1	–	18.9	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.1	6.5	–	3.1	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(22 Vdc ≤ V_I ≤ 33 Vdc)		–	–	1.5				
(21 Vdc ≤ V_I ≤ 33 Vdc)					–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	150	–	–	150	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	45	–	–	45	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 23 V ≤ V_I ≤ 33 V, T_J = +25°C)	RR	32	46	–	33	48	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

MC78L24C, MC78L24AC ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC78L24C			MC78L24AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	22.1	24	25.9	23	24	25	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
27.5 Vdc ≤ V_I ≤ 38 Vdc		–	35	350	–	–	–	
28 Vdc ≤ V_I ≤ 38 Vdc		–	30	300	–	50	300	
27 Vdc ≤ V_I ≤ 38 Vdc		–	–	–	–	60	350	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	40	200	–	40	200	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	20	100	–	20	100	
Output Voltage	V_O							Vdc
(28 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		21.6	–	26.4				
(27 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)					22.8	–	25.2	
(28 Vdc ≤ V_I ≤ 33 V, 1.0 mA ≤ I_O ≤ 70 mA)		21.6	–	26.4				
(27 Vdc ≤ V_I ≤ 33 V, 1.0 mA ≤ I_O ≤ 70 mA)					22.8	–	25.2	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.1	6.5	–	3.1	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(28 Vdc ≤ V_I ≤ 38 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	200	–	–	200	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	56	–	–	56	–	mV/1.0 k Hrs.
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 29 V ≤ V_I ≤ 35 V, T_J = +25°C)	RR	30	43	–	31	45	–	dB
Input-Output Voltage Differential (T_J = +25°C)	V_I/V_O	–	1.7	–	–	1.7	–	Vdc

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}} \geq V_I I_S - V_O I_O$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

I_S = Total Supply Current

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 1 – DROPOUT CHARACTERISTICS

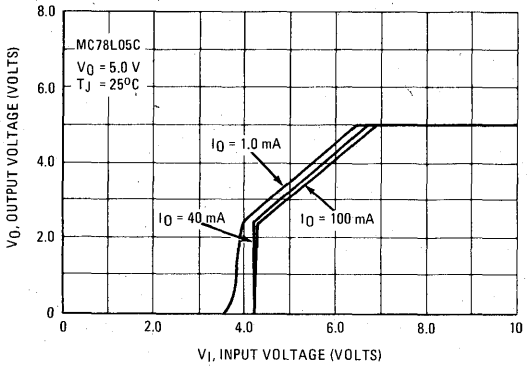


FIGURE 2 – DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

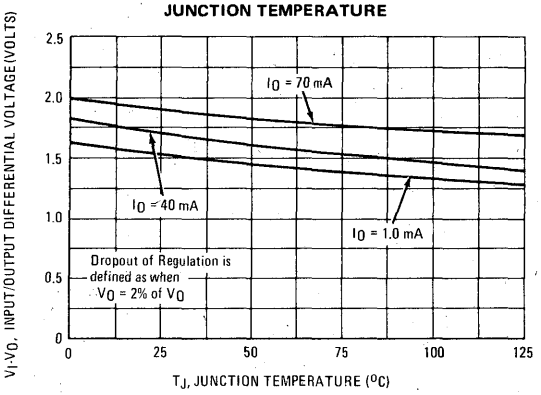


FIGURE 3 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

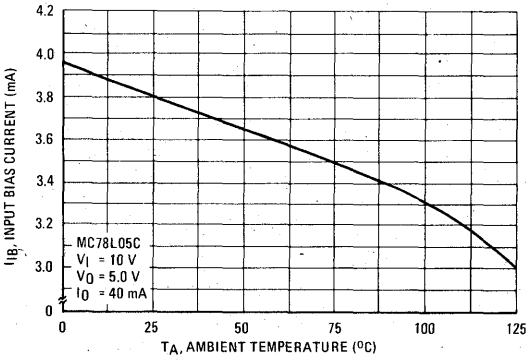


FIGURE 4 – INPUT BIAS CURRENT versus INPUT VOLTAGE

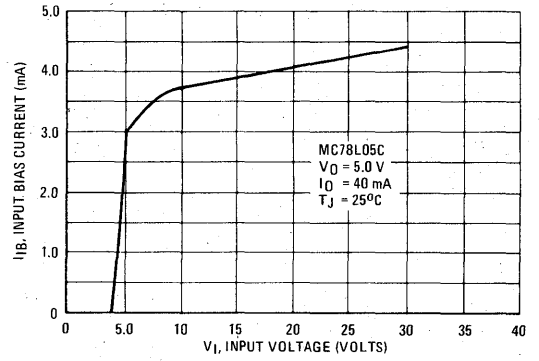


FIGURE 5 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-92 Type Package

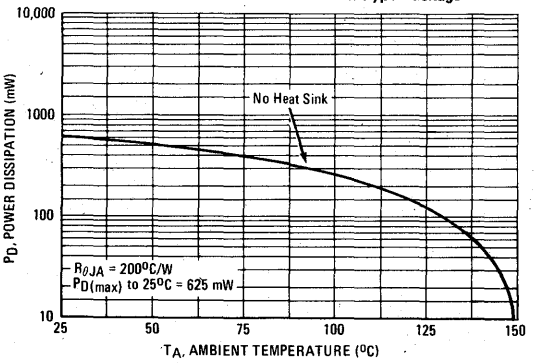
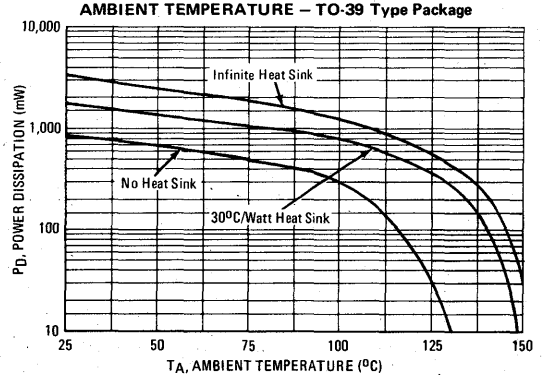


FIGURE 6 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-39 Type Package



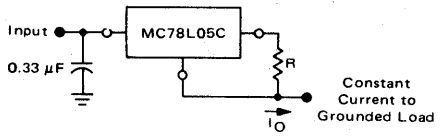
APPLICATIONS INFORMATION

Design Considerations

The MC78L00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 7 – CURRENT REGULATOR



The MC78L00C regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\ V}{R} + I_{IB}$$

I_{IB} = 3.8 mA over line and load changes

For example, a 100 mA current source would require R to be a 50-ohm, 1/2-W resistor and the output voltage compliance would be the input voltage less 7 volts.

FIGURE 8 – ±15 V TRACKING VOLTAGE REGULATOR

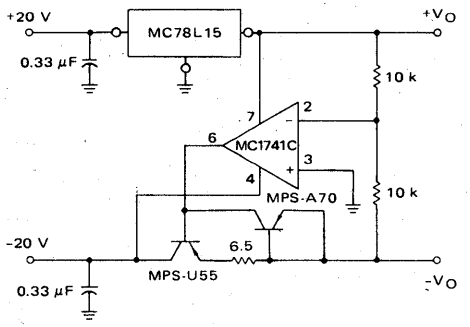
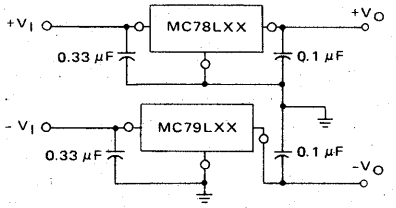


FIGURE 9 – POSITIVE AND NEGATIVE REGULATOR



MC78M00C series

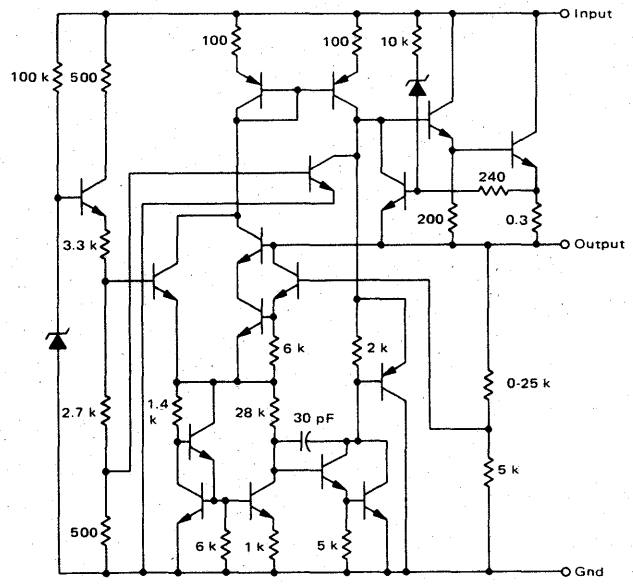
MC78M00C SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC78M00 Series positive voltage regulators are identical to the popular MC7800C Series devices, except that they are specified for only half the output current. Like the MC7800C devices, the MC78M00C three-terminal regulators are intended for local, on-card voltage regulation.

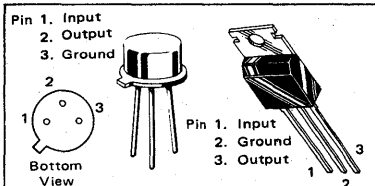
Internal current limiting, thermal shutdown circuitry and safe-area compensation for the internal pass transistor combine to make these devices remarkably rugged under most operating conditions. Maximum output current, with adequate heatsinking is 500 mA.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 313 and Case 79 (TO-220 and Hermetic TO-39)

REPRESENTATIVE SCHEMATIC DIAGRAM



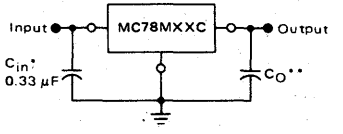
THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS



G SUFFIX
METAL PACKAGE
CASE 79
TO-39
(Case connected to Pin 3)

T SUFFIX
PLASTIC PACKAGE
CASE 313
(TO-220 Type)

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION		
DEVICE	TEMPERATURE RANGE	PACKAGE
MC78MXXCG	T_J = 0° C to +150° C	Metal Can
MC78MXXCT	T_J = 0° C to +150° C	Plastic Power
XX indicates nominal voltage		

TYPE NO./VOLTAGE

MC78M05C	5.0 Volts
MC78M06C	6.0 Volts
MC78M08C	8.0 Volts
MC78M12C	12 Volts
MC78M15C	15 Volts
MC78M18C	18 Volts
MC78M20C	20 Volts
MC78M24C	24 Volts

4

MC78M00C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V - 18 V) (20 V - 24 V)	V_I	35 40	Vdc
Power Dissipation (Package Limitation) Plastic Package T_A = 25°C Derate above T_A = 25°C T_C = 25°C Derate above T_C = 110°C Metal Package T_A = 25°C Derate above T_A = 25°C T_C = 25°C Derate above T_C = 85°C	 P_D θ_{JA} P_D θ_{JC} P_D θ_{JA} P_D θ_{JC}	 Internally Limited 70 Internally Limited 5.0 Internally Limited 185 Internally Limited 25	 °C/W °C/W °C/W °C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Operating Ambient Temperature Range	T_A	0 to +85	°C
Storage Temperature Range Plastic Package Metal Package	T_{stg}	 -65 to +150 -65 to +150	 °C °C

MC78M05C ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 200 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	Vdc
Line Regulation (T_J = +25°C) (7.0 Vdc ≤ V_I ≤ 25 Vdc) (8.0 Vdc ≤ V_I ≤ 25 Vdc)	Reg_{line}	 – –	 3.0 1.0	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 20 10	 100 50	mV
Output Voltage (7.0 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	4.75	–	5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.5	6.0	mA
Quiescent Current Change (8.0 Vdc ≤ V_I ≤ 25 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 8.0 V ≤ V_I ≤ 18 V) (I_O = 300 mA, f = 120 Hz, 8.0 ≤ V_I ≤ 18 V, T_J = 25°C)	RR	– –	80 80	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	300	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M06C ELECTRICAL CHARACTERISTICS (V_I = 11 V, I_O = 200 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	Vdc
Line Regulation (T_J = +25°C) (8.0 Vdc ≤ V_I ≤ 25 Vdc) (9.0 Vdc ≤ V_I ≤ 25 Vdc)	Reg_{line}	 – –	 5.0 1.5	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 20 10	 120 60	mV
Output Voltage (8.0 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	5.7	–	6.3	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.5	6.0	mA
Quiescent Current Change (9.0 Vdc ≤ V_I ≤ 25 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	45	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	24	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 9.0 V ≤ V_I ≤ 19 V) (I_O = 300 mA, f = 120 Hz, 9.0 V ≤ V_I ≤ 19 V, T_J = 25°C)	RR	– –	80 80	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	270	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	-0.5	–	mV/°C
Peak Output Current (T_J = 25°C) (T_J = 25°C)	I_O	–	700	–	mA

MC78M08C ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 200 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	Vdc
Line Regulation (T_J = +25°C) (10.5 Vdc ≤ V_I ≤ 25 Vdc) (11 Vdc ≤ V_I ≤ 25 Vdc)	Reg_{line}	 – –	 6.0 2.0	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 25 10	 160 80	mV
Output Voltage (10.5 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	7.6	–	8.4	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.6	6.0	mA
Quiescent Current Change (10.5 Vdc ≤ V_I ≤ 25 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	52	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	32	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 11.5 V ≤ V_I ≤ 21.5 V) (I_O = 300 mA, f = 120 Hz, 11.5 V ≤ V_I ≤ 21.5 V, T_J = 25°C)	RR	– –	80 80	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	250	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	-0.5	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

4

MC78M12C ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 200 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	Vdc
Line Regulation (T_J = +25°C) (14.5 Vdc ≤ V_I ≤ 30 Vdc) (16 Vdc ≤ V_I ≤ 22 Vdc)	Reg_{line}	 – –	 8.0 2.0	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 25 10	 240 120	mV
Output Voltage (14.5 Vdc ≤ V_I ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	11.4	–	12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.8	6.0	mA
Quiescent Current Change (14.5 Vdc ≤ V_I ≤ 30 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	75	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	48	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V) (I_O = 300 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = 25°C)	RR	– –	80 80	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	240	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M15C ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 200 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	Vdc
Input Regulation (T_J = +25°C) (17.5 Vdc ≤ V_I ≤ 30 Vdc) (20 Vdc ≤ V_I ≤ 30 Vdc)	Reg_{line}	 – –	 10 3.0	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 25 10	 150 75	mV
Output Voltage 17.5 Vdc ≤ V_I ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	14.25	–	15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.8	6.0	mA
Quiescent Current Change (18.5 Vdc ≤ V_I ≤ 30 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	90	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	60	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V) (I_O = 300 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = 25°C)	RR	– –	70 70	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	240	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M18C ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 200 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	Vdc
Line Regulation (T_J = +25°C) (21 Vdc ≤ V_I ≤ 33 Vdc) (24 Vdc ≤ V_I ≤ 33 Vdc)	Reg_{line}	 – –	 10 40	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 30 10	 360 180	mV
Output Voltage (21 Vdc ≤ V_I ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	17.1	–	18.9	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.8	6.5	mA
Quiescent Current Change (21 Vdc ≤ V_I ≤ 33 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	100	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	72	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V) (I_O = 300 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V, T_J = 25°C)	RR	– –	70 70	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	240	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M20C ELECTRICAL CHARACTERISTICS (V_I = 29 V, I_O = 200 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	19.2	20	20.8	Vdc
Line Regulation (T_J = +25°C) (23 Vdc ≤ V_I ≤ 35 Vdc) (24 Vdc ≤ V_I ≤ 35 Vdc)	Reg_{line}	 – –	 10 5.0	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 30 10	 400 200	mV
Output Voltage (23 Vdc ≤ V_I ≤ 35 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	19	–	21	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.9	6.5	mA
Quiescent Current Change (23 Vdc ≤ V_I ≤ 35 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	110	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	80	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 24 V ≤ V_I ≤ 34 V) (I_O = 300 mA, f = 120 Hz, 24 V ≤ V_I ≤ 34 V, T_J = 25°C)	RR	– –	70 70	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	–	240	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	$\Delta V_O/\Delta T$	–	-1.1	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

4

MC78M24C ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 200 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	23	24	25	Vdc
Line Regulation (T_J = +25°C) (27 Vdc ≤ V_I ≤ 38 Vdc) (28 Vdc ≤ V_I ≤ 38 Vdc)	Reg_{line}	 – –	 10 5.0	 100 50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 30 10	 480 240	mV
Output Voltage (27 Vdc ≤ V_I ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 200 mA)	V_O	22.8	–	25.2	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	5.0	7.0	mA
Quiescent Current Change (27 Vdc ≤ V_I ≤ 38 Vdc) (5.0 mA ≤ I_O ≤ 200 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	170	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	96	mV/1.0 k Hrs
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 28 V ≤ V_I ≤ 38 V) (I_O = 300 mA, f = 120 Hz, 28 V ≤ V_I ≤ 38 V, T_J = 25°C)	RR	– –	70 70	– –	dB
Input-Output Voltage Differential (T_A = +25°C)	V_I-V_O	–	2.0	–	Vdc
Short-Circuit Current Limit (T_J = +25°C)	I_{OS}	–	240	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	$\Delta V_O/\Delta T$	–	-1.2	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}(Typ)} \geqslant V_I I_S - V_O I_O$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient

I_S = Total Supply Current

DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

TYPICAL PERFORMANCE CURVES

FIGURE 1 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE TO-220 (CASE 313)

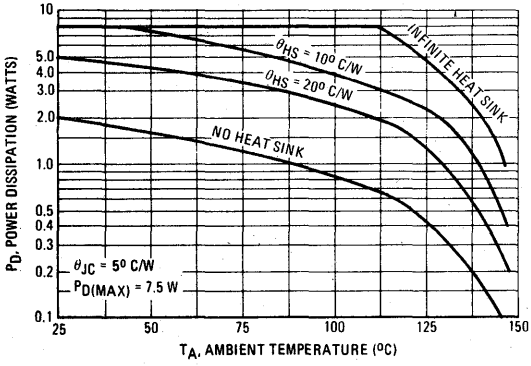


FIGURE 2 – WORST CASE POWER DISSIPATION versus AMBIENT TEMPERATURE TO-39 (CASE 79)

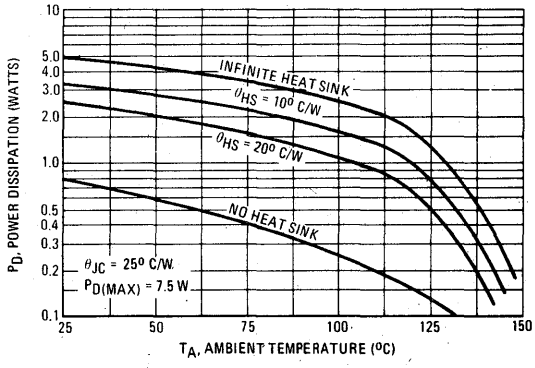


FIGURE 3 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

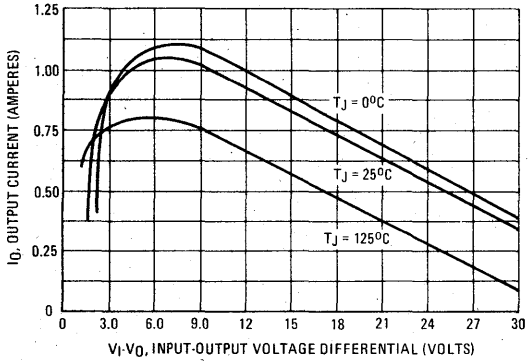
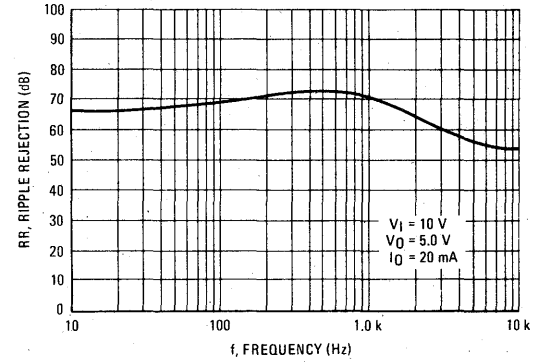


FIGURE 4 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



4

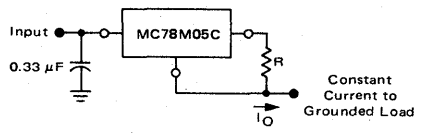
APPLICATIONS INFORMATION

Design Considerations

The MC78M00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

FIGURE 5 – CURRENT REGULATOR



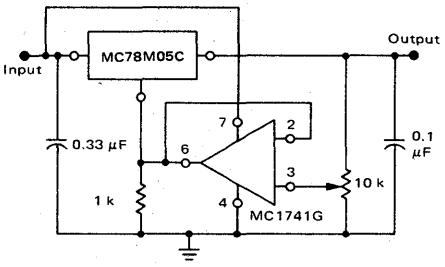
The MC7800C regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\ V}{R} + I_Q$$

I_Q = 1.5 mA over line and load changes

For example, a 500 mA current source would require R to be a 10-ohm, 10-W resistor and the output voltage compliance would be the input voltage less 7 volts.

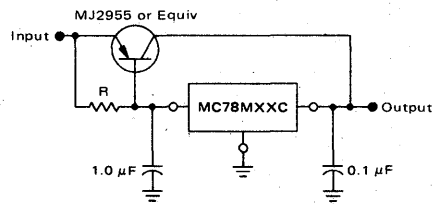
FIGURE 6 – ADJUSTABLE OUTPUT REGULATOR



V_O, 7.0 V to 20 V
$V_{IN} - V_O \geq 2.0$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 volts greater than the regulator voltage.

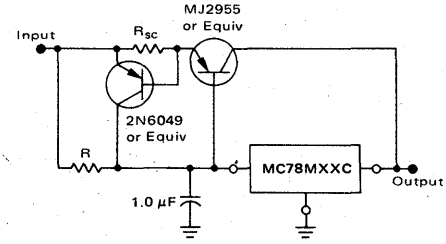
FIGURE 7 – CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The MC78M00C series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

FIGURE 8 – SHORT-CIRCUIT PROTECTION



XX = 2 digits of type number indicating voltage.

The circuit of Figure 7 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a two-ampere plastic power transistor is specified.

MC7900C Series

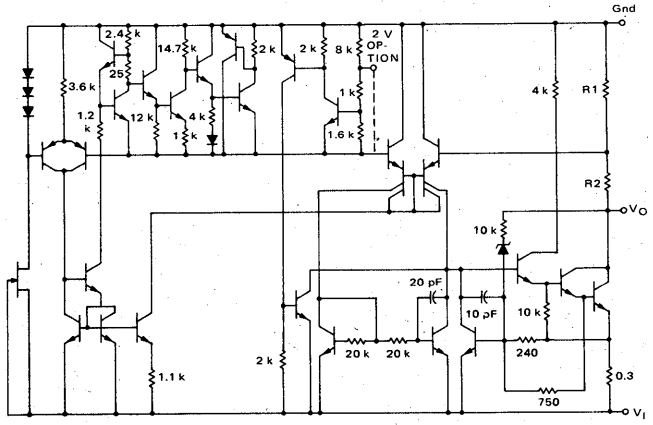
MC7900C SERIES THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

The MC7900C Series of fixed output negative voltage regulators are intended as complements to the popular MC7800C Series devices. These negative regulators are available in the same seven-voltage options as the MC7800C devices. In addition, two extra voltage options commonly employed in MECL systems are also available in the negative MC7900C Series.

Available in fixed output voltage options from -2.0 to -24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation – making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 313 and Case 11 (TO-220 and Hermetic TO-3)

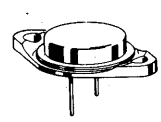
SCHEMATIC DIAGRAM



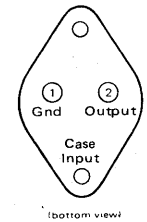
DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC7902C - 2.0 Volts	MC7906C - 6.0 Volts	MC7915C - 15 Volts
MC7905C - 5.0 Volts	MC7908C - 8.0 Volts	MC7918C - 18 Volts
MC7905.2C – 5.2 Volts	MC7912C - 12 Volts	MC7924C - 24 Volts

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS



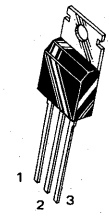
K SUFFIX
METAL PACKAGE
CASE 11-01
(TO-3 TYPE)



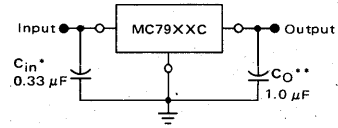
(bottom view)

T SUFFIX
PLASTIC PACKAGE
CASE 313

Pin 1. Ground
2. Input
3. Output



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC79XXCK	T_J = 0° C to +150° C	Metal Power
MD79XXCT	T_J = 0° C to +150° C	Plastic Power

XX indicates nominal voltage

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MC7900C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.0 V – 18 V) (24 V)	V_I	-35 -40	Vdc
Power Dissipation Plastic Package T_A = +25°C Derate above T_A = +25°C T_C = +25°C Derate above T_C = +95°C (See Figure 1) Metal Package T_A = +25°C Derate above T_A = +25°C T_C = +25°C Derate above T_C = +65°C	 P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JC}$ P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JC}$	 Internally Limited 15.4 Internally Limited 200 Internally Limited 22.2 Internally Limited 182	 Watts mW/°C Watts mW/°C Watts mW/°C Watts mW/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Range	T_J	0 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient – Plastic Package – Metal Package	$R_{\theta JA}$	65 45	°C/W
Thermal Resistance, Junction to Case – Plastic Package – Metal Package	$R_{\theta JC}$	5.0 5.5	°C/W

MC7902C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-1.92	-2.00	-2.08	Vdc
Line Regulation (T_J = +25°C, I_O = 100 mA) -7.0 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc (T_J = +25°C, I_O = 500 mA) -7.0 Vdc ≥ V_I ≥ -25 Vdc -8.0 Vdc ≥ V_I ≥ -12 Vdc	Reg_{line}	 – – – –	 8.0 4.0 18 8.0	 20 10 40 20	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 70 20	 120 60	mV
Output Voltage -7.0 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-1.90	–	-2.10	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change -7.0 Vdc ≥ V_I ≥ -25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 – –	 – –	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	3.5	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7905C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-4.8	-5.0	-5.2	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-7.0 Vdc ≥ V_I ≥ -25 Vdc		–	7.0	50	
-8.0 Vdc ≥ V_I ≥ -12 Vdc		–	2.0	25	
(T_J = +25°C, I_O = 500 mA)					
-7.0 Vdc ≥ V_I ≥ -25 Vdc		–	35	100	
-8.0 Vdc ≥ V_I ≥ -12 Vdc		–	8.0	50	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	11	100	
250 mA ≤ I_O ≤ 750 mA		–	4.0	50	
Output Voltage	V_O	-4.75	–	-5.25	Vdc
-7.0 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-7.0 Vdc ≥ V_{in} ≥ -25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	70	–	dB
Input-Output Voltage Differential	$\|V_I - V_O\|$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$					

MC7905.2C ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-5.0	-5.2	-5.4	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-7.2 Vdc ≥ V_I ≥ -25 Vdc		–	8.0	52	
-8.0 Vdc ≥ V_I ≥ -12 Vdc		–	2.2	27	
(T_J = +25°C, I_O = 500 mA)					
-7.2 Vdc ≥ V_I ≥ -25 Vdc		–	37	105	
-8.0 Vdc ≥ V_I ≥ -12 Vdc		–	8.5	52	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	12	105	
250 mA ≤ I_O ≤ 750 mA		–	4.5	52	
Output Voltage	V_O	-4.94	–	-5.46	Vdc
-7.2 Vdc ≥ V_I ≥ -20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-7.2 Vdc ≥ V_I ≥ -25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	42	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	68	–	dB
Input-Output Voltage Differential	$\|V_I - V_O\|$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, $0^oC \leq T_A \leq +125^oC$					

MC7906C ELECTRICAL CHARACTERISTICS (V_I = -11 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-5.75	-6.0	-6.25	Vdc
Line Regulation (T_J = +25°C, I_O = 100 mA) -8.0 Vdc ≥ V_I ≥ -25 Vdc -9.0 Vdc ≥ V_I ≥ -13 Vdc (T_J = +25°C, I_O = 500 mA) -8.0 Vdc ≥ V_I ≥ -25 Vdc -9.0 Vdc ≥ V_I ≥ -13 Vdc	Reg_{line}	 – – – –	 9.0 3.0 43 10	 60 30 120 60	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 13 5.0	 120 60	mV
Output Voltage -8.0 Vdc ≥ V_I ≥ -21 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)	V_O	-5.7	–	-6.3	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change -8.0 Vdc ≥ V_I ≥ -25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 – –	 – –	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	45	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	24	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7908C ELECTRICAL CHARACTERISTICS (V_I = -14 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-7.7	-8.0	-8.3	Vdc
Line Regulation (T_J = +25°C, I_O = 100 mA) -10.5 Vdc ≥ V_I ≥ -25 Vdc -11 Vdc ≥ V_I ≥ -17 Vdc (T_J = +25°C, I_O = 500 mA) -10.5 Vdc ≥ V_I ≥ -25 Vdc -11 Vdc ≥ V_I ≥ -17 Vdc	Reg_{line}	 – – – –	 12 5.0 50 22	 80 40 160 80	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 26 9.0	 160 80	mV
Output Voltage -10.5 Vdc ≥ V_I ≥ -23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	-7.6	–	-8.4	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change -10.5 Vdc ≥ V_I ≥ -25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	52	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	32	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	62	–	dB
Input-Output Voltage Differential I_O = 1.0 A, T_J = +25°C	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C

MC7912C ELECTRICAL CHARACTERISTICS (V_I = -19 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-11.5	-12	-12.5	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-14.5 Vdc ≥ V_I ≥ -30 Vdc		–	13	120	
-16 Vdc ≥ V_I ≥ -22 Vdc		–	6.0	60	
(T_J = +25°C, I_O = 500 mA)					
-14.5 Vdc ≥ V_I ≥ -30 Vdc		–	55	240	
-16 Vdc ≥ V_I ≥ -22 Vdc		–	24	120	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	46	240	
250 mA ≤ I_O ≤ 750 mA		–	17	120	
Output Voltage	V_O	-11.4	–	-12.6	Vdc
-14.5 Vdc ≥ V_I ≥ -27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-14.5 Vdc ≥ V_I ≥ -30 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	75	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	48	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	61	–	dB
Input-Output Voltage Differential	$\|V_I - V_O\|$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C					

MC7915C ELECTRICAL CHARACTERISTICS (V_I = -23 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-14.4	-15	-15.6	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-17.5 Vdc ≥ V_I ≥ -30 Vdc		–	14	150	
-20 Vdc ≥ V_I ≥ -26 Vdc		–	6.0	75	
(T_J = +25°C, I_O = 500 mA)					
-17.5 Vdc ≥ V_I ≥ -30 Vdc		–	57	300	
-20 Vdc ≥ V_I ≥ -26 Vdc		–	27	150	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	68	300	
250 mA ≤ I_O ≤ 750 mA		–	25	150	
Output Voltage	V_O	-14.25	–	-15.75	Vdc
-17.5 Vdc ≥ V_I ≥ -30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-17.5 Vdc ≥ V_I ≥ -30 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	90	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	60	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	60	–	dB
Input-Output Voltage Differential	$\|V_I - V_O\|$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C					

MC7918C ELECTRICAL CHARACTERISTICS (V_I = -27 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-17.3	-18	-18.7	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-21 Vdc ≥ V_I ≥ -33 Vdc		–	25	180	
-24 Vdc ≥ V_I ≥ -30 Vdc		–	10	90	
(T_J = +25°C, I_O = 500 mA)					
-21 Vdc ≥ V_I ≥ -33 Vdc		–	90	360	
-24 Vdc ≥ V_I ≥ -30 Vdc		–	50	180	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.0 A		–	110	360	
250 mA ≤ I_O ≤ 750 mA		–	55	180	
Output Voltage	V_O	-17.1	–	-18.9	Vdc
-21 Vdc ≥ V_I ≥ -33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.5	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-21 Vdc ≥ V_I ≥ -33 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	110	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	72	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	59	–	dB
Input-Output Voltage Differential	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C					

MC7924C ELECTRICAL CHARACTERISTICS (V_I = -33 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	-23	-24	-25	Vdc
Line Regulation	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
-27 Vdc ≥ V_I ≥ -38 Vdc		–	31	240	
-30 Vdc ≥ V_I ≥ -36 Vdc		–	14	120	
(T_J = +25°C, I_O = 500 mA)					
-27 Vdc ≥ V_I ≥ -38 Vdc		–	118	480	
-30 Vdc ≥ V_I ≥ -36 Vdc		–	70	240	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.0 A		–	150	480	
250 mA ≤ I_O ≤ 750 mA		–	85	240	
Output Voltage	V_O	-22.8	–	-25.2	Vdc
-27 Vdc ≥ V_I ≥ -38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.6	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
-27 Vdc ≥ V_I ≥ -38 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	–	170	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	96	mV/1.0 k Hrs
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	56	–	dB
Input-Output Voltage Differential	$\lvert V_I - V_O \rvert$	–	2.0	–	Vdc
I_O = 1.0 A, T_J = +25°C					
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	–	-1.0	–	mV/°C
I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C					

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 1 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220)

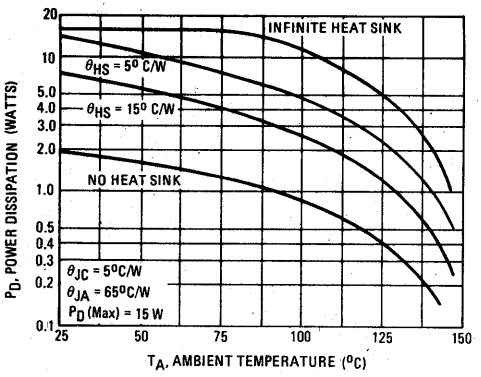


FIGURE 2 – WORST CASE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3)

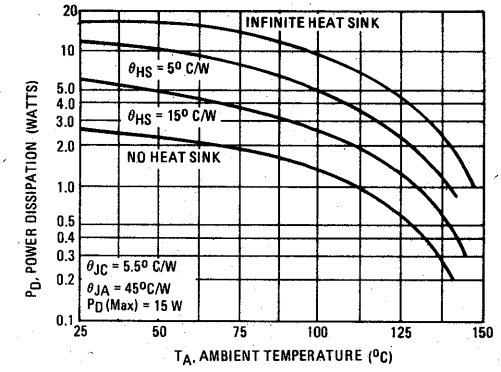


FIGURE 3 – PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE

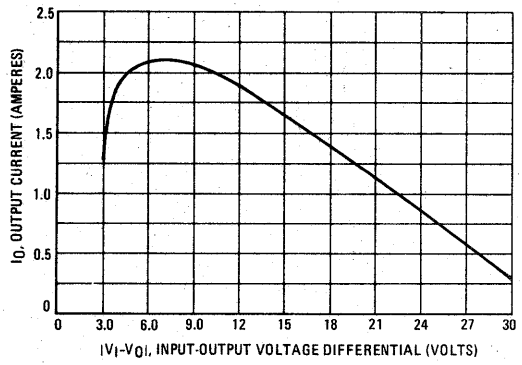


FIGURE 4 – RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

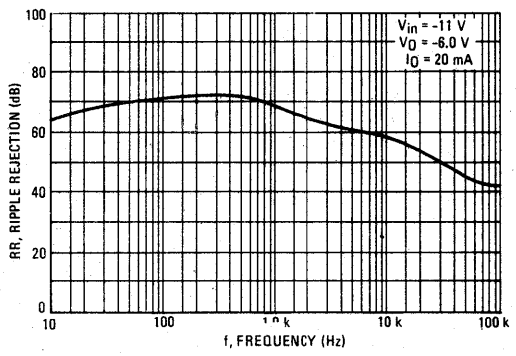


FIGURE 5 – RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES

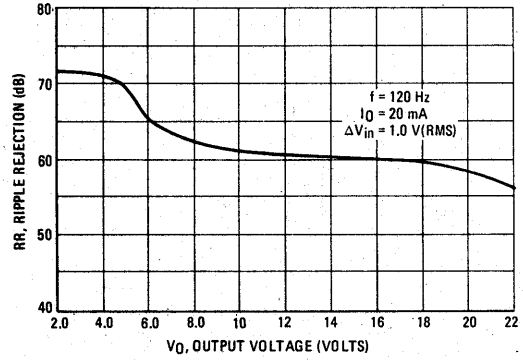
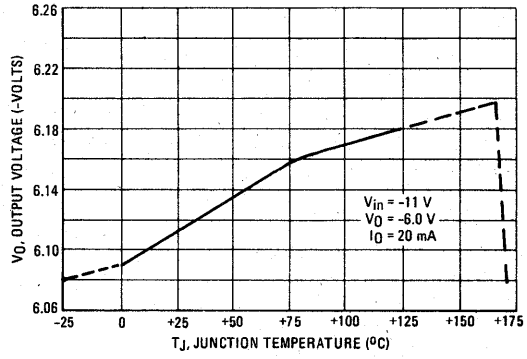


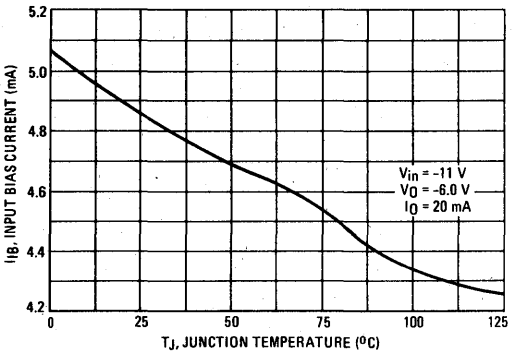
FIGURE 6 – OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



4

TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}} \geqslant V_I I_S - V_O I_O$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}$(Typ) = Typical Thermal Resistance Junction to Ambient

I_S = Total Supply Current

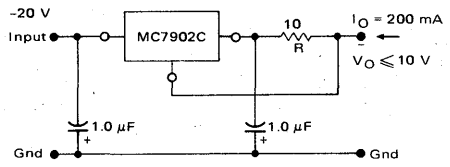
APPLICATIONS INFORMATION

Design Considerations

The MC7900C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

FIGURE 8 – CURRENT REGULATOR

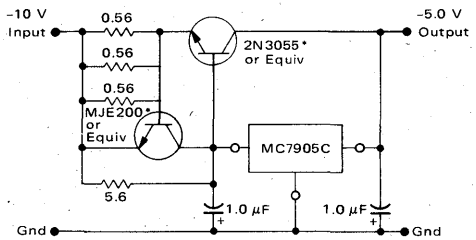


The MC7902, -2.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows:

$$I_O = \frac{2\ V}{R} + I_B$$

The quiescent current for this regulator is typically 4.3 mA. The 2.0 volt regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

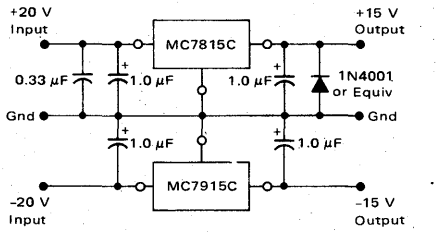
FIGURE 9 – CURRENT BOOST REGULATOR
(-5.0 V @ 4.0 A, with 5.0 A current limiting)



*Mounted on common heat sink, Motorola MS-10 or equivalent.

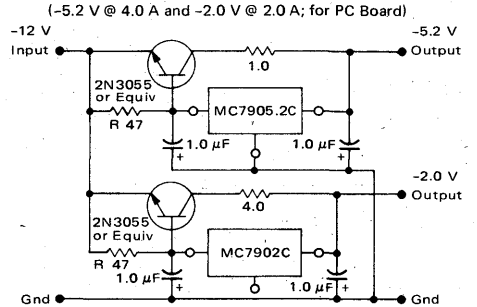
When a boost transistor is used, short-circuit currents are equal to the sum of the series pass and regulator limits, which are measured at 3.2 A and 1.8 A respectively in this case. Series pass limiting is approximately equal to 0.6 V/R_{SC}. Operation beyond this point to the peak current capability of the MC7905C is possible if the regulator is mounted on a heat sink; otherwise thermal shutdown will occur when the additional load current is picked up by the regulator.

FIGURE 10 – OPERATIONAL AMPLIFIER SUPPLY
(±15 V @ 1.0 A)



The MC7815 and MC7915 positive and negative regulators may be connected as shown to obtain a dual power supply for operational amplifiers. A clamp diode should be used at the output of the MC7815 to prevent potential latch-up problems.

FIGURE 11 – TYPICAL MECL SYSTEM POWER SUPPLY
(-5.2 V @ 4.0 A and -2.0 V @ 2.0 A; for PC Board)



When current-boost power transistors are used, 47-ohm base-to-emitter resistors (R) must be used to bypass the quiescent current at no load. These resistors, in conjunction with the V_{BE} of the NPN transistors, determine when the pass transistors begin conducting. The 1-ohm and 4-ohm dropping resistors were chosen to reduce the power dissipated in the boost transistors but still leave at least 2.0 V across these devices for good regulation.

MC79L00C, AC series

THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

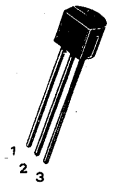
The MC79L00 Series negative voltage regulators are inexpensive, easy-to-use devices suitable for numerous applications requiring up to 100 mA. Like the higher powered MC7900 Series negative regulators, this series features thermal shutdown and current limiting, making them remarkably rugged. In most applications, no external components are required for operation.

The MC79L00 devices are useful for on-card regulation or any other application where a regulated negative voltage at a modest current level is needed. These regulators offer substantial advantage over the common resistor/zener diode approach.

- No External Components Required
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- Low Cost
- Complementary Positive Regulators Offered (MC78L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

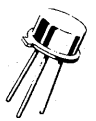
THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

P SUFFIX
CASE 29
TO-92

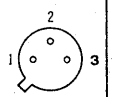


Pin 1. Ground
2. Input
3. Output

G SUFFIX
CASE 79
TO-39

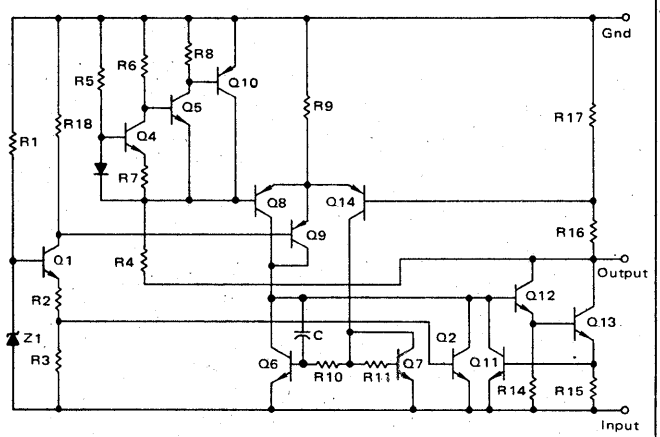


Pin 1. Ground
2. Output
3. Input

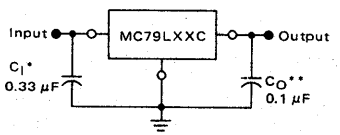


Bottom View

REPRESENTATIVE CIRCUIT SCHEMATIC



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_I is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

Device No. ±10%	Device No. ±5%	Nominal Voltage
MC79L03C	MC79L03AC	−3.0
MC79L05C	MC79L05AC	−5.0
MC79L12C	MC79L12AC	−12
MC79L15C	MC79L15AC	−15
MC79L18C	MC79L18AC	−18
MC79L24C	MC79L24AC	−24

ORDERING INFORMATION

Device	Temperature Range	Package
MC79LXXACG	T_J = 0°C to +150°C	Metal Can
MC79LXXACP	T_J = 0°C to +150°C	Plastic Power
MC79LXXCG	T_J = 0°C to +150°C	Metal Can
MC79LXXCP	T_J = 0°C to +150°C	Plastic Power

XX indicates nominal voltage

MC79L00C Series MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating		Symbol	Value	Unit
Input Voltage	(-3,-5 V) (-12,-15,-18 V) (-24 V)	V_I	-30 -35 -40	Vdc
Storage Temperature Range		T_{stg}	-65 to +150	°C
Junction Temperature Range		T_J	0 to +150	°C

4

MC79L03C, AC ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	MC79L03C			MC79L03AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-2.76	-3.00	-3.24	-2.88	-3.0	-3.12	Vdc
Input Regulation (T_J = +25°C) -7.0 Vdc ≥ V_I ≥ -20 Vdc -8.0 Vdc ≥ V_I ≥ -20 Vdc	Reg_{line}	 – –	 – –	 80 60	 – –	 – –	 60 40	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 72 36	 – –	 – –	 72 36	mV
Output Voltage -7.0 Vdc ≥ V_I ≥ -20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = -10 Vdc, 1.0 mA ≤I_O ≤ 70 mA	V_O	 -2.7 -2.7	 – –	 -3.3 -3.3	 -2.85 -2.85	 – –	 -3.15 -3.15	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6.0 5.5	 – –	 – –	 6.0 5.5	mA
Input Bias Current Change -8.0 Vdc ≥ V_I ≥ -20 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	 – –	 – –	 -1.5 -0.2	 – –	 – –	 -1.5 -0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	30	–	–	30	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	10	–	–	10	–	mV/1.0 k Hrs.
Ripple Rejection (-8.0 ≥ V_I ≥ -18 Vdc, f = 120 Hz, T_J = 25°C)	RR	44	51	–	45	51	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$/V_I-V_O/$	–	1.7	–	–	1.7	–	Vdc

MC79L05C, AC Series ELECTRICAL CHARACTERISTICS (V_I = -10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC79L05C			MC79L05AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-4.6	-5.0	-5.4	-4.8	-5.0	-5.2	Vdc
Input Regulation (T_J = +25°C)	Reg_{line}							mV
-7.0 Vdc ≥ V_I ≥ -20 Vdc		–	–	200	–	–	150	
-8.0 Vdc ≥ V_I ≥ -20 Vdc		–	–	150	–	–	100	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	60	–	–	60	
1.0 mA ≤ I_O ≤ 40 mA		–	–	30	–	–	30	
Output Voltage	V_O							Vdc
-7.0 Vdc ≥ V_I ≥ -20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-4.5	–	-5.5	-4.75	–	-5.25	
V_I = -10 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-4.5	–	-5.5	-4.75	–	-5.25	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.0	–	–	6.0	
(T_J = +125°C)		–	–	5.5	–	–	5.5	
Input Bias Current Change	ΔI_{IB}							mA
-8.0 Vdc ≥ V_I ≥ -20 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	40	–	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	12	–	–	12	–	mV/1.0 k Hrs.
Ripple Rejection (-8.0 ≥ V_I ≥ 18 Vdc, f = 120 kHz, T_J = 25°C)	RR	40	49	–	41	49	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$/V_I - V_O/$	–	1.7	–	–	1.7	–	Vdc

MC79L12C, AC ELECTRICAL CHARACTERISTICS (V_I = -19 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC79L12C			MC79L12AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-11.1	-12	-12.9	-11.5	-12	-12.5	Vdc
Input Regulation (T_J = +25°C)	Reg_{line}							mV
-14.5 Vdc ≥ V_I ≥ -27 Vdc		–	–	250	–	–	250	
-16 Vdc ≥ V_I ≥ -27 Vdc		–	–	200	–	–	200	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	100	–	–	100	
1.0 mA ≤ I_O ≤ 40 mA		–	–	50	–	–	50	
Output Voltage	V_O							Vdc
-14.5 Vdc ≥ V_I ≥ -27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-10.8	–	-13.2	-11.4	–	-12.6	
V_I = -19 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-10.8	–	-13.2	-11.4	–	-12.6	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
-16 Vdc ≥ V_I ≥ -27 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	80	–	–	80	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	24	–	–	24	–	mV/1.0 k Hrs.
Ripple Rejection (-15 ≤ V_I ≤ -25 Vdc, f = 120 Hz, T_J = +25°C)	RR	36	42	–	37	42	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$/V_I - V_O/$	–	1.7	–	–	1.7	–	Vdc

MC79L15C, AC ELECTRICAL CHARACTERISTICS (V_I = -23 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC79L15C			MC79L15AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-13.8	-15	-16.2	-14.4	-15	-15.6	Vdc
Input Regulation (T_J = +25°C)	Reg_{line}							mV
-17.5 Vdc ≥ V_I ≥ -30 Vdc		–	–	300	–	–	300	
-20 Vdc ≥ V_I ≥ -30 Vdc		–	–	250	–	–	250	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	150	–	–	150	
1.0 mA ≤ I_O ≤ 40 mA		–	–	75	–	–	75	
Output Voltage	V_O							Vdc
-17.5 Vdc ≥ V_I ≥ -30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-13.5	–	-16.5	-14.25	–	-15.75	
V_I = -23 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-13.5	–	-16.5	-14.25	–	-15.75	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
-20 Vdc ≥ V_I ≥ -30 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	90	–	–	90	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	30	–	–	30	–	mV/1.0 k Hrs.
Ripple Rejection (-18.5 ≤ V_I ≤ -28.5 Vdc, f = 120 Hz)	RR	33	39	–	34	39	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$/V_I-V_O/$	–	1.7	–	–	1.7	–	Vdc

MC79L18C, AC ELECTRICAL CHARACTERISTICS (V_I = -27 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC79L18C			MC79L18AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-16.6	-18	-19.4	-17.3	-18	-18.7	Vdc
Input Regulation (T_J = +25°C)	Reg_{line}							mV
-20.7 Vdc ≥ V_I ≥ -33 Vdc		–	–	–	–	–	325	
-21.4 Vdc ≥ V_I ≥ -33 Vdc		–	–	325	–	–	–	
-22 Vdc ≥ V_I ≥ -33 Vdc		–	–	275	–	–	–	
-21 Vdc ≥ V_I ≥ -33 Vdc		–	–	–	–	–	275	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	170	–	–	170	
1.0 mA ≤ I_O ≤ 40 mA		–	–	85	–	–	85	
Output Voltage	V_O							Vdc
-20.7 Vdc ≥ V_I ≥ -33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		–	–	–	-17.1	–	-18.9	
-21.4 Vdc ≥ V_I ≥ -33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-16.2	–	-19.8	–	–	–	
V_I = -27 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-16.2	–	-19.8	-17.1	–	-18.9	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
-21 Vdc ≥ V_I ≥ -33 Vdc		–	–	–	–	–	1.5	
-27 Vdc ≥ V_I ≥ -33 Vdc		–	–	1.5	–	–	–	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	150	–	–	150	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	45	–	–	45	–	mV/1.0 k Hrs.
Ripple Rejection (-23 ≤ V_I ≤ -33 Vdc, f = 120 Hz, T_J = +25°C)	RR	32	46	–	33	48	–	dB
Input-Output Voltage Differential I_O = 40 mA, T_J = +25°C	$/V_I-V_O/$	–	1.7	–	–	1.7	–	Vdc

MC79L24C, AC ELECTRICAL CHARACTERISTICS (V_I = -33 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, $0^oC < T_J < +125^oC$ unless otherwise noted.)

Characteristic	Symbol	MC79L24C			MC79L24AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	-22.1	-24	-25.9	-23	-24	-25	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C)								
-27 Vdc ≥ V_I ≥ -38 V		–	–	–	–	–	350	
-27.5 Vdc ≥ V_I ≥ -38 Vdc		–	–	350	–	–	–	
-28 Vdc ≥ V_I ≥ -38 Vdc		–	–	300	–	–	300	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	200	–	–	200	
1.0 mA ≤ I_O ≤ 40 mA		–	–	100	–	–	100	
Output Voltage	V_O							Vdc
-27 Vdc ≥ V_I ≥ -38 V, 1.0 mA ≤ I_O ≤ 40 mA		–	–	–	-22.8	–	-25.2	
-28 Vdc ≥ V_I ≥ -38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		-21.4	–	-26.4	–	–	–	
V_I = -33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		-21.4	–	-26.4	-22.8	–	-25.2	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
-28 Vdc ≥ V_I ≥ -38 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	200	–	–	200	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	56	–	–	56	–	mV/1.0 k Hrs.
Ripple Rejection	RR	30	43	–	31	47	–	dB
(-29 ≤ V_I ≤ -35 Vdc, f = 120 Hz, T_J = 25°C)								
Input-Output Voltage Differential	$/V_I - V_O/$	–	1.7	–	–	1.7	–	Vdc
I_O = 40 mA, T_J = +25°C								

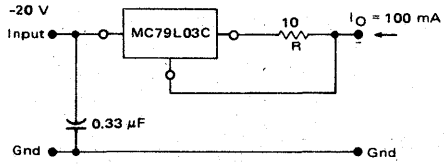
APPLICATIONS INFORMATION

Design Considerations

The MC79L00C Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

CURRENT REGULATOR

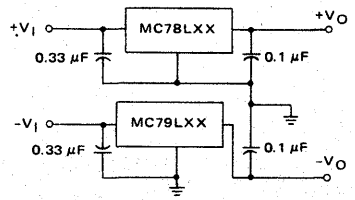


The MC79L03, -3.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows:

$$I_O = \frac{3\ V}{R} + I_B$$

The quiescent current for this regulator is typically 3.8 mA. The -3.0 volt regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

POSITIVE AND NEGATIVE REGULATOR



TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 1 – DROPOUT CHARACTERISTICS

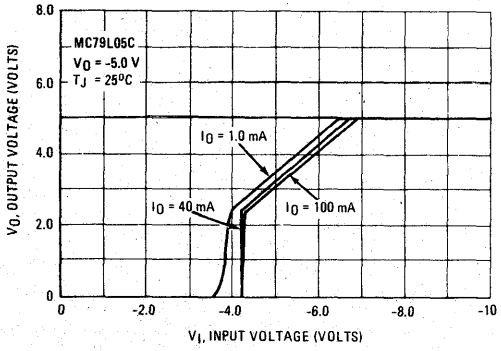


FIGURE 2 – DROPOUT VOLTAGE versus JUNCTION TEMPERATURE

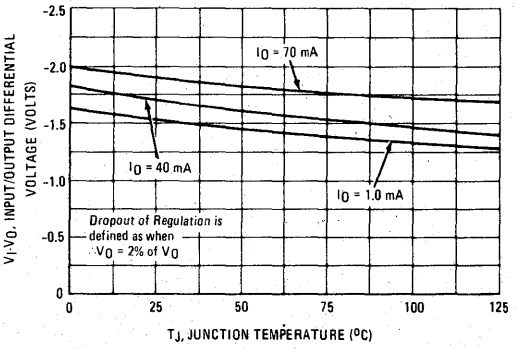


FIGURE 3 – INPUT BIAS CURRENT versus AMBIENT TEMPERATURE

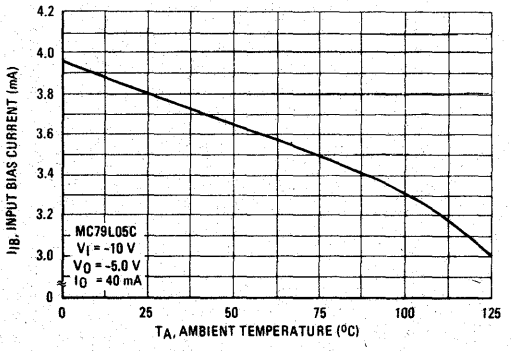


FIGURE 4 – INPUT BIAS CURRENT versus INPUT VOLTAGE

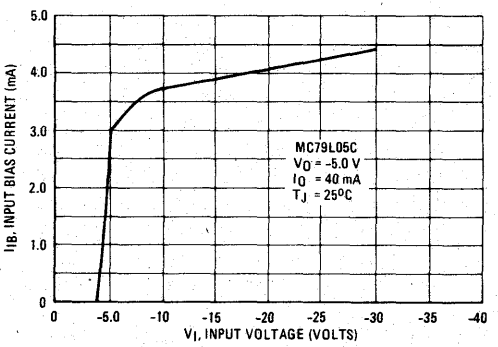


FIGURE 5 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-92 Type Package

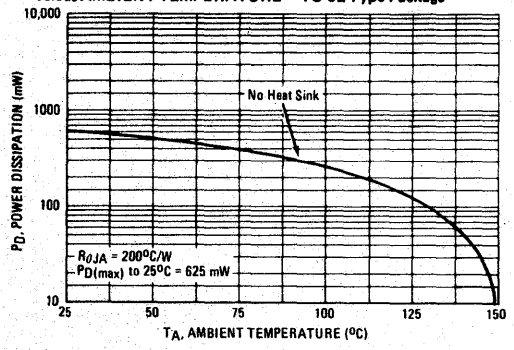
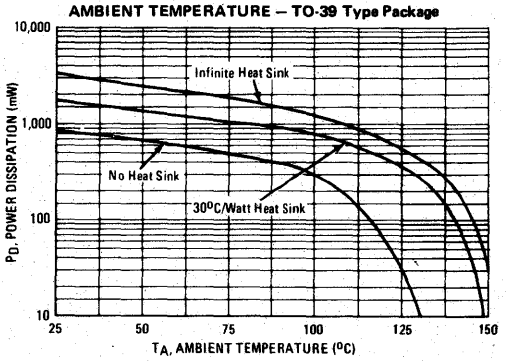


FIGURE 6 – MAXIMUM AVERAGE POWER DISSIPATION versus AMBIENT TEMPERATURE – TO-39 Type Package



4

MLM104
MLM204
MLM304

MONOLITHIC NEGATIVE VOLTAGE REGULATOR

The MLM104G, MLM204G, and MLM304G are functionally, electrically, and pin-for-pin equivalent to the LM104, LM204 and LM304 respecitvely.

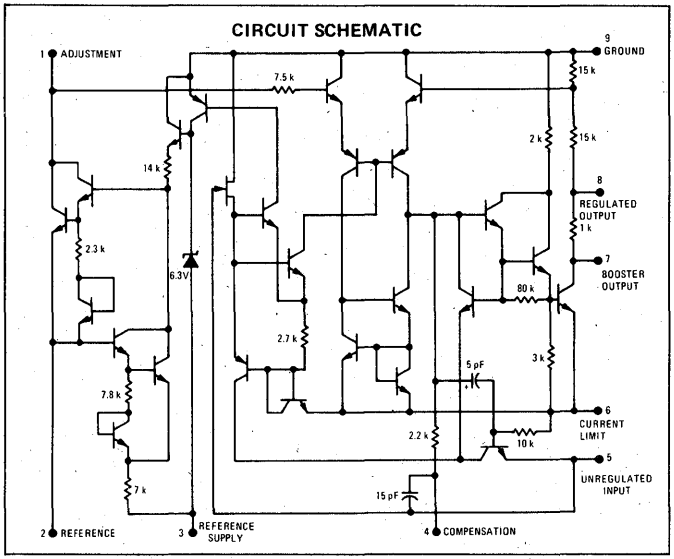
- Regulation No Load to Full Load – 1.0 mV
- Line Regulation – 0.01 %/V
- Ripple Rejection – 0.2 mV/V
- Temperature Stability Over Temperature Range – 0.3%

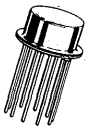
NEGATIVE VOLTAGE REGULATOR

MONOLITHIC SILICON INTEGRATED CIRCUIT

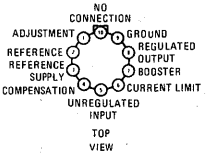
4

CIRCUIT SCHEMATIC





METAL PACKAGE
CASE 603
(TO-100)
$R_{\theta JA}$ = 160°C/W



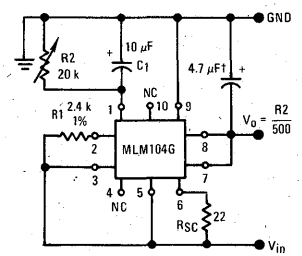
Pin 5 Electrically Connected to Case Through Substrate

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MLM104	–	-55°C to +125°C	Metal Can
MLM204		-25°C to +85°C	Metal Can
MLM304	LM304H	0°C to +70°C	Metal Can

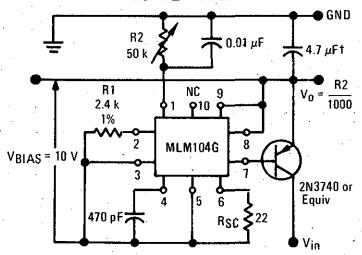
TYPICAL APPLICATIONS

FIGURE 1 – BASIC REGULATOR CIRCUIT



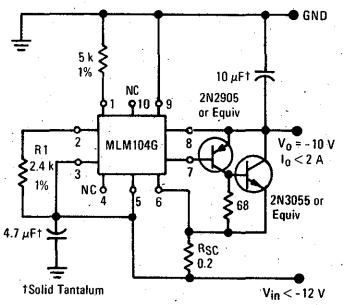
†Solid Tantalum
Trim R1 for exact scale factor.

FIGURE 2 – SEPARATE BIAS SUPPLY OPERATION



†Solid Tantalum

FIGURE 3 – HIGH CURRENT REGULATOR



†Solid Tantalum

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MLM104	MLM204	MLM304	Unit
Input Voltage	V_{in}	50	50	40	Vdc
Input-Output Voltage Differential	$V_{in}-V_o$	50	50	40	Vdc
Power Dissipation (See Note 1)	P_D	680	680	680	mW
Operating Temperature Range	T_A	-55 to +125	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C
Lead Temperature (soldering, t = 10 s)	T_S	300	300	300	°C

ELECTRICAL CHARACTERISTICS (*See Note 2*)

Characteristic	Symbol	MLM104 MLM204			MLM304			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	V_{in}	-8.0	–	-50	-8.0	–	-40	Volts
Output Voltage Range	V_o	-0.015	–	-40	-0.035	–	-30	Volts
Output-Input Voltage Differential	$\lvert V_{in}-V_o \rvert$							Volts
I_o = 20 mA		2.0	–	50	2.0	–	40	
I_o = 5.0 mA		0.5	–	50	0.5	–	40	
Load Regulation	Reg_{load}							mV
$0 \leqslant I_o \leqslant 20$ mA, R_{SC} = 15Ω		–	1.0	5.0	–	1.0	5.0	
Line Regulation	Reg_{in}							%
$V_o \leqslant -5.0$ V, ΔV_{in} = 0.1 V		–	0.056	0.1	–	0.056	0.1	
Ripple Rejection (See Figure 1)	Rej_R							mV/V
(C_1 = 10 μF, f = 120 Hz)								
$V_{in} < -15$ V		–	0.2	0.5	–	0.2	0.5	
$-7.0\ V \geqslant V_{in} \geqslant -15$ V		–	0.5	1.0	–	0.5	1.0	
Output Voltage Scale Factor	SF							V/k Ω
R_1 = 2.4 k Ω (See Figures 1,2 and 3)		1.8	2.0	2.2	1.8	2.0	2.2	
Temperature Stability	TCV_o							%
$V_o \leqslant -1.0$ V		–	0.3	1.0	–	–	–	
$V_o \leqslant -1.0$ V, $0°C \leqslant T_A \leqslant +70°C$	$\Delta V_o/\Delta T$	–	–	–	–	0.3	1.0	
Output Noise Voltage (See Figure 1)	V_n							
(10 Hz ≤ f ≤ 10 kHz)								
$V_o \leqslant -5.0$ V, C_1 = 0		–	0.007	–	–	0.007	–	%
C_1 = 10 μF		–	15	–	–	15	–	μV
Standby Current Drain (I_L = 5.0 mA)	I_B							mA
V_o = 0		–	1.7	2.5	–	1.7	2.5	
V_o = -40 V		–	3.6	5.0	–	–	–	
V_o = -30 V		–	–	–	–	3.6	5.0	
Long Term Stability	S							%
$V_o \leqslant -1.0$ V		–	0.1	1.0	–	0.1	1.0	

Note 1:

The maximum junction temperature of the MLM104 is +150°C, for the MLM204 – +100°C, and for the MLM304 – +85°C. For operating at elevated temperatures, the package must be derated based on a thermal resistance of 150°C/W – junction to ambient, or 45°C/W – junction to case.

Note 2:

These specifications apply for junction temperatures of –55°C to +150°C for the MLM104; –25°C to +100°C for the MLM204; and 0 to +85°C for the MLM304. The specifications also apply for input and output voltages within the indicated ranges (unless otherwise specified). Load and line regulation specifications given are for constant junction temperature. Temperature drift effects must be taken into account separately when the device is operating under conditions of high power dissipation.

MLM105
MLM205
MLM305

MONOLITHIC POSITIVE VOLTAGE REGULATOR

The MLM105, MLM205, and MLM305 are functionally, electrically, and pin-for-pin equivalent to the LM105, LM205, and LM305 respectively.

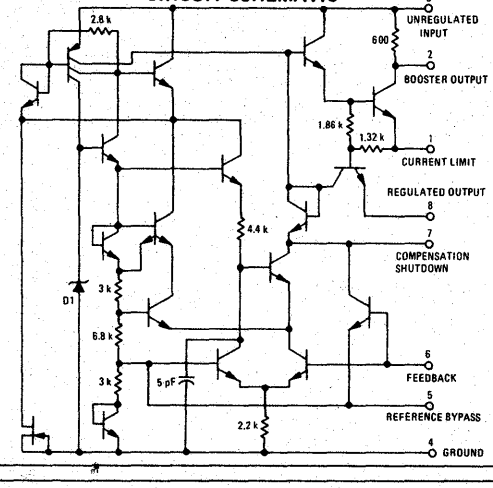
- Output Voltage Adjustable from 4.5 V to 40 V
- Output Currents in Excess of 10 A Possible by Addition of External Transistors
- Load Regulation Better than 0.1%, Full Load with Current Limiting
- DC Line Regulation, 0.03%/V
- Ripple Rejection, 0.01 %/V

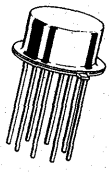
POSITIVE VOLTAGE REGULATOR
SILICON MONOLITHIC

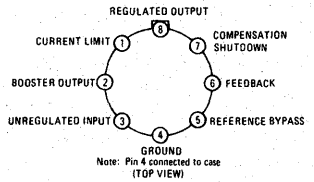
INTEGRATED CIRCUIT

4

CIRCUIT SCHEMATIC







ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MLM105G	—	-55°C to +125°C	Metal Can
MLM205G	—	-25°C to +85°C	Metal Can
MLM305G	LM305H	0°C to +70°C	Metal Can

TYPICAL APPLICATIONS

FIGURE 1 – BASIC REGULATOR CIRCUIT

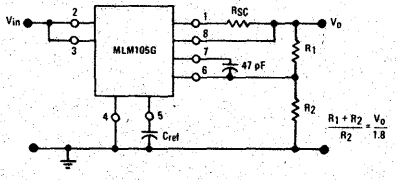


FIGURE 2 – 10 A REGULATOR with FOLDBACK CURRENT LIMITING

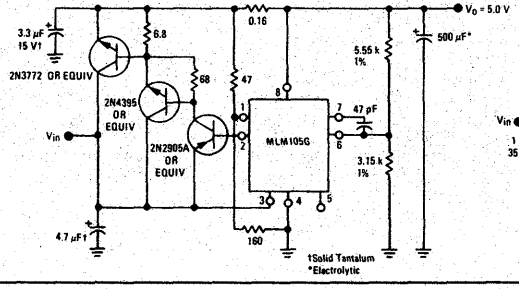
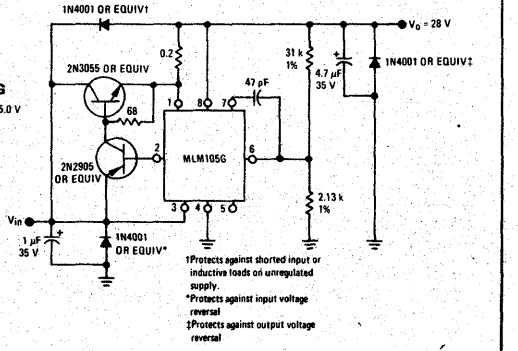


FIGURE 3 – 1.0 A REGULATOR with PROTECTIVE DIODES



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	MLM105	MLM205	MLM305	Unit
Input Voltage	V_{in}	50	50	40	Vdc
Input-Output Voltage Differential	$\lvert V_{in}\text{-}V_o \rvert$	40	40	40	Vdc
Power-Dissipation (See Note 1)	P_D	680	680	680	mW
Operating Temperature Range	T_A	-55 to +125	-25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C
Lead Temperature (soldering, t = 10 s)	T_S	300	300	300	°C

ELECTRICAL CHARACTERISTICS (See Note 2)

Characteristic	Symbol	MLM105 MLM205			MLM305			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	V_{in}	8.5	–	50	8.5	–	40	Volts
Output Voltage Range	V_o	4.5	–	40	4.5	–	30	Volts
Output-Input Voltage Differential	$\lvert V_{in}\text{-}V_o \rvert$	3.0	–	30	3.0	–	30	Volts
Load Regulation (See Figure 1)	Reg_{load}							%
$(0 \leq I_o \leq 12$ mA)								
R_{SC} = 18 Ω, T_A = +25°C		–	0.02	0.05	–	0.02	0.05	
R_{SC} = 10 Ω, $T_A = T_{high}$*		–	0.03	0.1	–	0.03	0.1	
R_{SC} = 18 Ω, $T_A = T_{low}$**		–	0.03	0.1	–	0.03	0.1	
Line Regulation	Reg_{in}							%/V
$V_{in}\text{-}V_o \leq 5.0$ V		–	0.025	0.06	–	0.025	0.06	
$V_{in}\text{-}V_o > 5.0$ V		–	0.015	0.03	–	0.015	0.03	
Ripple Rejection (See Figure 1)	$\frac{\Delta V_o}{V_o \Delta V_i}$	–	0.003	0.01	1.0	0.003	0.01	%/V
C_{ref} = 10 μF, f = 120 Hz								
Temperature Stability	TCV_o							%
T_{low}** $\leq T_A \leq T_{high}$*		–	0.3	1.0	–	0.3	1.0	
Feedback Sense Voltage	V_{ref}	1.63	1.7	1.81	1.63	1.7	1.81	Volts
Output Noise Voltage (See Figure 1)	V_n							%
(10 Hz ≤ f ≤ 10 kHz)								
C_{Ref} = 0		–	0.005	–	–	0.005	–	
$C_{Ref} > 0.1$ μF		–	0.002	–	–	0.002	–	
Standby Current Drain	I_B							mA
V_{in} = 50 V		–	0.8	2.0	–	–	–	
V_{in} = 40 V		–	–	–	–	0.8	2.0	
Long Term Stability	S	–	0.1	1.0	–	0.1	1.0	%

*T_{high} = +125°C for MLM105
+85°C for MLM205
+70°C for MLM305

**T_{low} = -55°C for MLM105
-25°C for MLM205
0°C for MLM305

Note 1:
The maximum junction temperature of the MLM105 is +150°C, for the MLM205 – +100°C, and for the MLM305 – +85°C. For operating at elevated temperatures, the package must be derated based on a thermal resistance of 150°C/W – junction to ambient, or 45°C/W – junction to case.

Note 2:
These specifications apply for junction temperatures of −55°C to +150°C for the MLM105, −25°C to +85°C for the MLM205, and 0 to +70°C for the MLM305. Specifications also apply for input and output voltages within the indicated ranges and for a divider impedance sensed by the feedback terminal of 2.0 kilohms (unless otherwise specified). Load and line regulation specifications given are for constant junction temperature. Temperature drift effects must be taken into account separately when the device is operating under conditions of high power dissipation.

MLM109
MLM209
MLM309

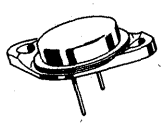
POSITIVE VOLTAGE REGULATOR

MONOLITHIC POSITIVE THREE - TERMINAL FIXED VOLTAGE REGULATOR

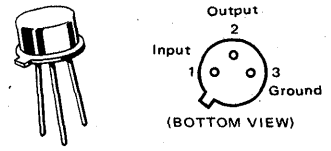
A versatile positive fixed +5.0-volt regulator designed for easy application as on on-card, local voltage regulator for digital logic systems. Current limiting and thermal shutdown are provided to make the units extremely rugged.

In most applications only one external component, a capacitor, is required in conjunction with the MLM109 Series devices. Even this component may be omitted if the power-supply filter is not located an appreciable distance from the regulator.

- High Maximum Output Current – Over 1.0 Ampere in TO-3 type Package – Over 200 mA in TO-39 Package
- Minimum External Components Required
- Internal Short-Circuit Protection
- Internal Thermal Overload Protection
- Excellent Line and Load Transient Rejection
- Designed for Use with Popular MDTL and MTTL Logic

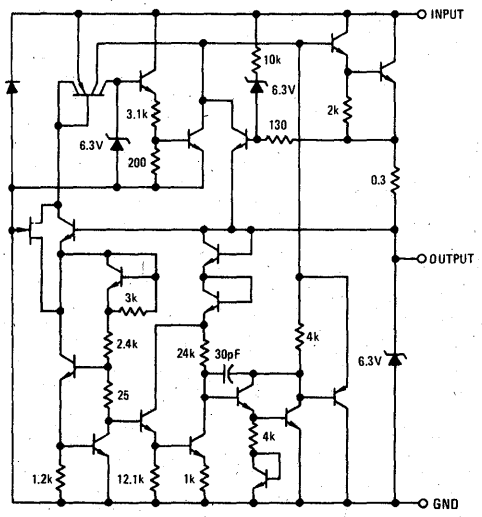


K SUFFIX
METAL PACKAGE
CASE 11-01
(TO-3 Type)



G SUFFIX
METAL PACKAGE
CASE 79-02
(TO-39)

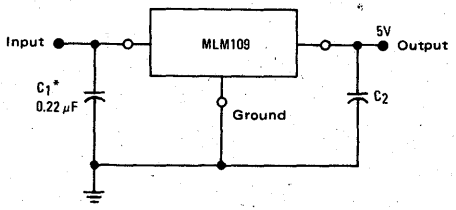
CIRCUIT SCHEMATIC



ORDERING INFORMATION			
DEVICE	ALTERNATE	TEMPERATURE RANGE	PACKAGE
MLM109G	–	T_J = –55° C to +150° C	Metal Can
MLM109K	–	T_J = –55° C to +150° C	Metal Power
MLM209G	–	T_J = –55° C to +150° C	Metal Can
MLM209K	–	T_J = –55° C to +150° C	Metal Power
MLM309G	LM309H	T_J = 0° C to +125° C	Metal Can
MLM309K	LM309K	T_J = 0° C to +125° C	Metal Power

TYPICAL APPLICATION

FIXED 5.0 V REGULATOR



*Required if regulator is located an appreciable distance from power supply filter. Although no output capacitor is needed for stability, it does improve transient response.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	35	Vdc
Power Dissipation	P_D	Internally Limited	
Junction Temperature Range MLM109 MLM209 MLM309	T_J	 -55 to +150 -55 to +150 0 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Temperature (soldering, t = 60 s)	T_S	300	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	MLM109 / MLM209 ① Min	Typ	Max	MLM309 ② Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.7	5.05	5.3	4.8	5.05	5.2	Vdc
Input Regulation (T_J = +25°C) 7.0 ≤ V_{in} ≤ 25 V	Reg_{in}	–	4.0	50	–	4.0	50	mV
Load Regulation (T_J = +25°C)	Reg_{load}							mV
Case 11-01 (type TO-3) 5.0 mA ≤ I_O ≤ 1.5A		–	50	100	–	50	100	
Case 79-02 (TO-39) 5.0 mA ≤ I_O ≤ 0.5A		–	20	50	–	20	50	
Output Voltage Range 7.0 V ≤ V_{in} ≤ 25 V 5.0 mA ≤ I_O ≤ I_{max}, P ≤ P_{max}	V_O	4.6	–	5.4	4.75	–	5.25	Vdc
Quiescent Current (7.0 V ≤ V_{in} ≤ 25 V)	I_B	–	5.2	10	–	5.2	10	mAdc
Quiescent Current Change (7.0 V ≤ V_{in} ≤ 25 V)	ΔI_B	–	–	0.5	–	–	0.5	
5.0 mA ≤ I_O ≤ I_{max}		–	–	0.8	–	–	0.8	
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_N	–	40	–	–	40	–	μV
Long Term Stability	S	–	–	10	–	–	20	mV
Thermal Resistance, Junction to Case ③	θJC							°C/W
Case 11-01 (type TO-3)		–	3.0	–	–	3.0	–	
Case 79-02 (TO-39)		–	15	–	–	15	–	

NOTES:

① Unless otherwise specified, these specifications apply for -55°C ≤ T_J ≤ +150° (-25°C ≤ T_J ≤ +150°C for the MLM209). For Case 79-02 (TO-39) V_{in} = 10 V, I_O = 0.1 A, I_{max} = 0.2 A and P_{max} = 2.0 W. For Case 11-01 (type TO-3) V_{in} = 10 V, I_O = 0.5 A, I_{max} = 1.0 A and P_{max} = 20 W.

② Unless otherwise specified, these specifications apply for 0°C ≤ T_J ≤ +125°C, V_{in} = 10V. For Case 79-02 (TO-39) I_O = 0.1A, I_{max} = 0.2A and P_{max} = 2.0 W. For Case 11-01 (type TO-3) I_O = 0.5 A, I_{max} = 1.0 A and P_{max} = 20 W.

③ Without a heat sink, the thermal resistance of the Case 79-02 (TO-39) package is about 150°C/W, while that of the Case 11-01 (type TO-3) package is approximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the heat sink.

TYPICAL CHARACTERISTICS

(V_{in} = 10 V, T_A = +25°C unless otherwise noted.)

FIGURE 1 – MAXIMUM AVERAGE POWER DISSIPATION (MLM109K, MLM209K)

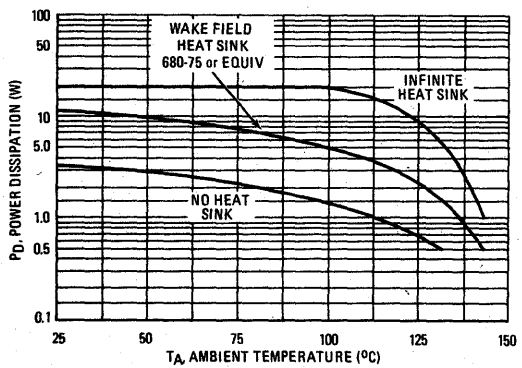
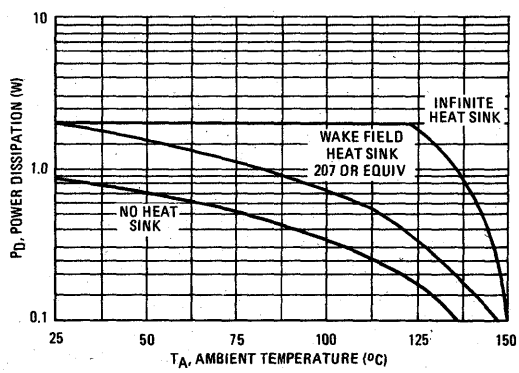


FIGURE 2 – MAXIMUM AVERAGE POWER DISSIPATION (MLM109G, MLM209G)



TYPICAL CHARACTERISTICS (continued)

(V_{in} = 10 V, T_A = +25°C unless otherwise noted.)

FIGURE 3 – MAXIMUM AVERAGE POWER DISSIPATION (MLM309K)

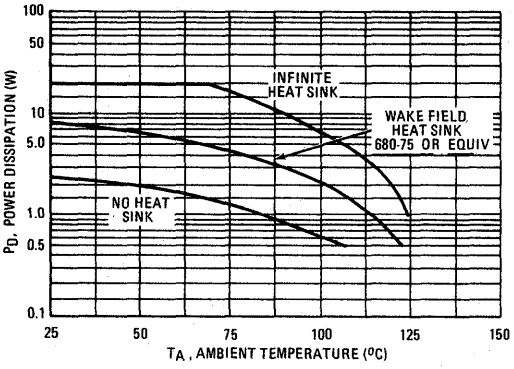


FIGURE 4 – MAXIMUM AVERAGE POWER DISSIPATION (MLM309G)

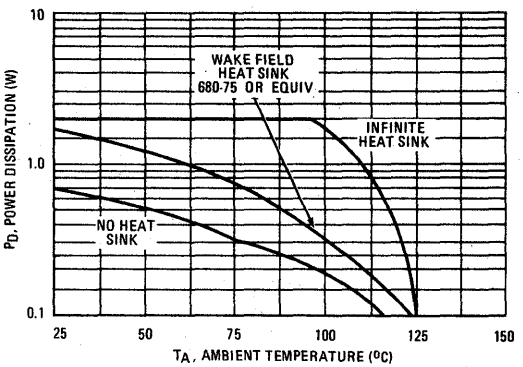


FIGURE 5 - OUTPUT IMPEDANCE versus FREQUENCY

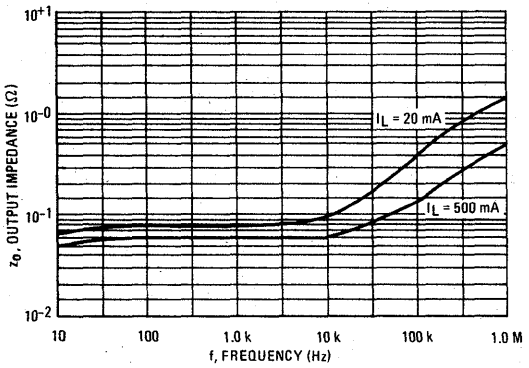


FIGURE 6 – PEAK OUTPUT CURRENT (K PACKAGE)

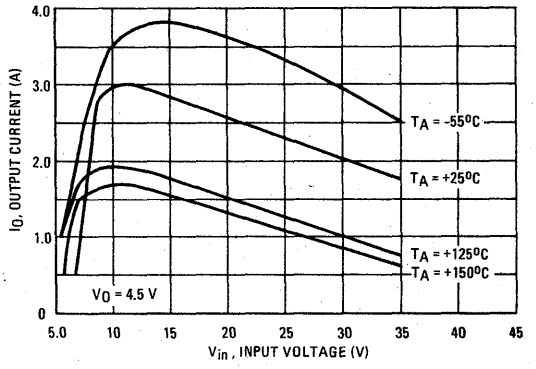


FIGURE 7 – PEAK OUTPUT CURRENT (G PACKAGE)

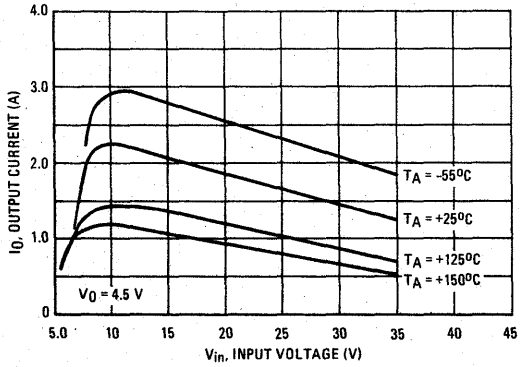
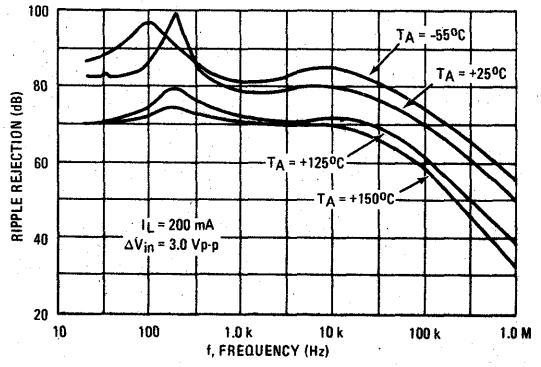


FIGURE 8 – RIPPLE REJECTION



TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – DROPOUT VOLTAGE

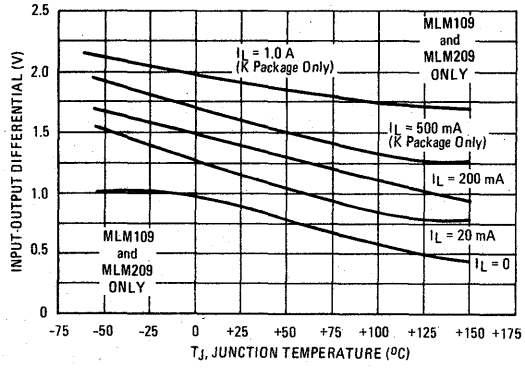


FIGURE 10 – DROPOUT CHARACTERISTIC (K PACKAGE)

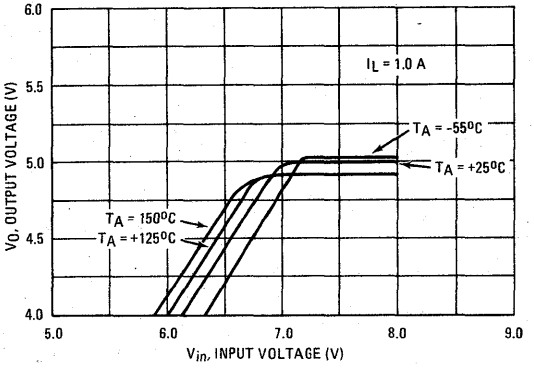


FIGURE 11 – OUTPUT VOLTAGE

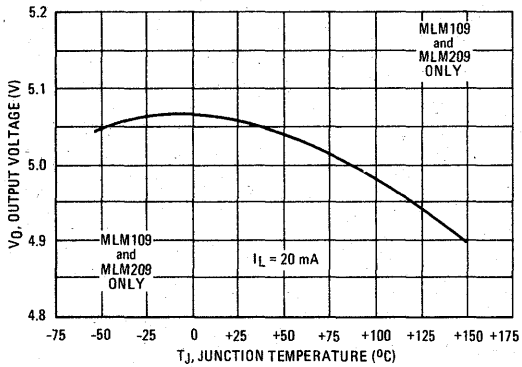


FIGURE 12 – OUTPUT NOISE VOLTAGE

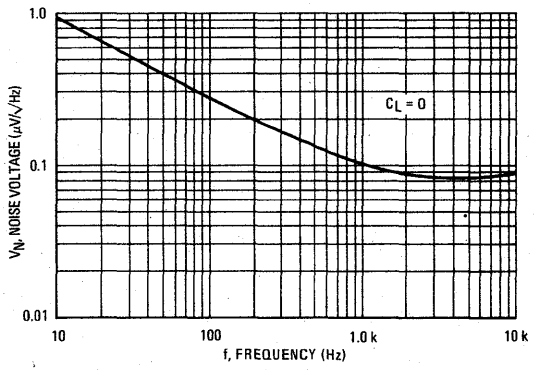


FIGURE 13 – QUIESCENT CURRENT

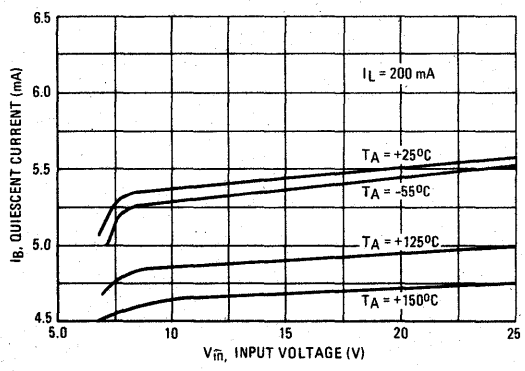
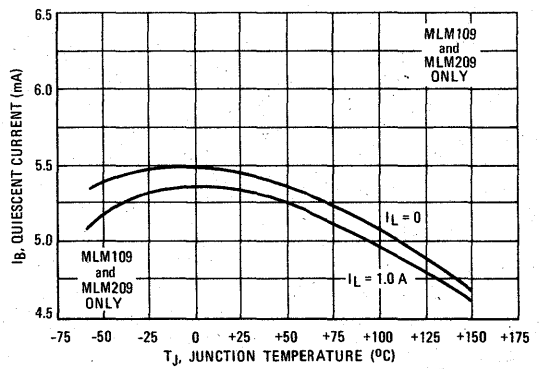


FIGURE 14 – QUIESCENT CURRENT



4

TYPICAL APPLICATIONS

FIGURE 15 – ADJUSTABLE OUTPUT REGULATOR

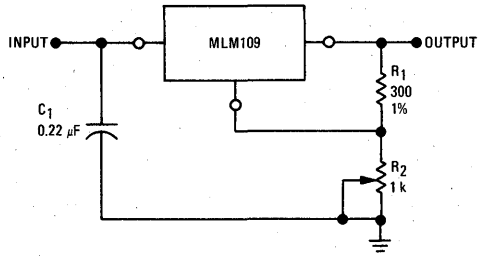
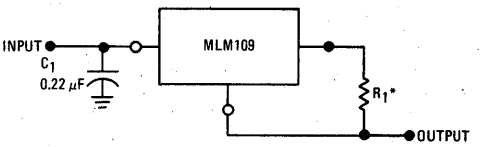


FIGURE 16 – CURRENT REGULATOR



*DETERMINES OUTPUT CURRENT.

4

FIGURE 17 – 5.0-VOLT, 3.0-AMPERE REGULATOR
(with plastic boost transistor)

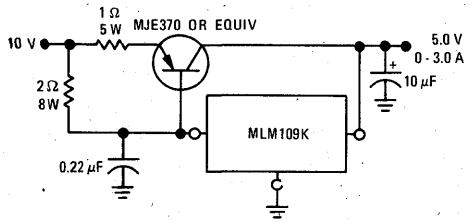


FIGURE 18 – 5.0 VOLT, 4.0-AMPERE TRANSISTOR
(with plastic Darlington boost transistor)

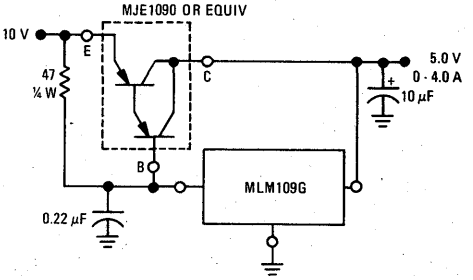


FIGURE 19 – 5.0-VOLT, 10-AMPERE REGULATOR

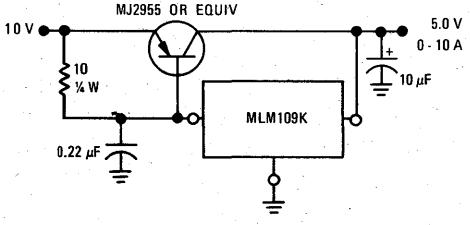
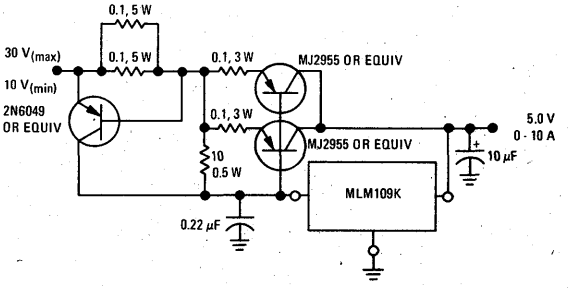
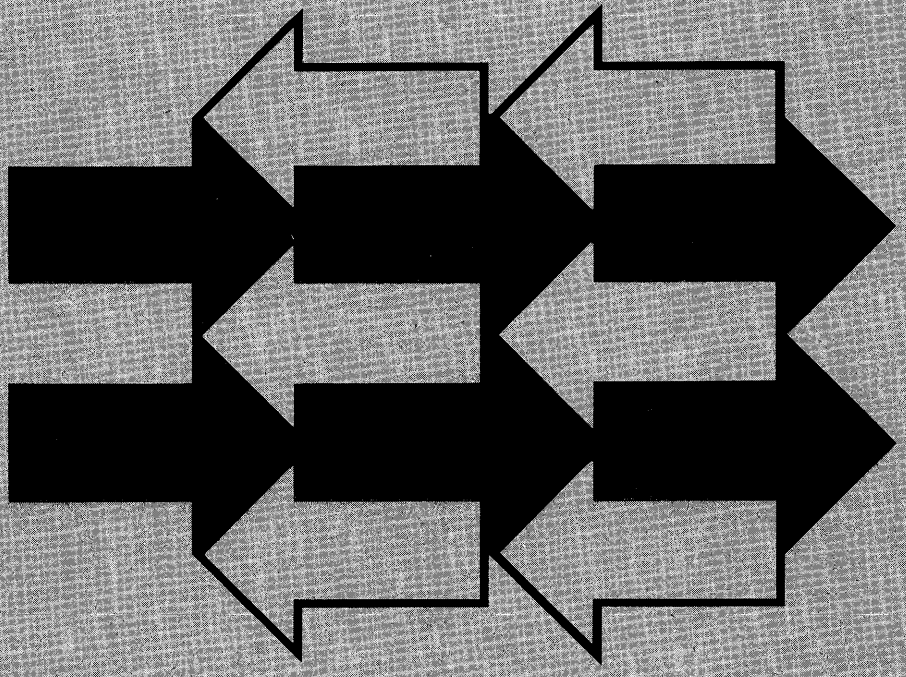


FIGURE 20 – 5.0-VOLT, 10-AMPERE REGULATOR
(with Short-Circuit Current Limiting for
Safe-Area Protection of pass transistors)



Interface Circuits / Chapter 5



INTERFACE CIRCUITS

INTERFACE CIRCUITS (continued)

*T_A = 0 to 85°C

BUS INTERFACE

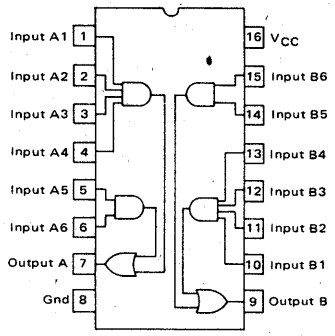
Computer Bus

Line drivers and receivers designed to operate compatibly. The MC8T13/MC8T14 combination is specified for general TTL system applications. The MC8T23/MC8T24 combination is specifically oriented toward IBM 360/370 system requirements.

DUAL LINE DRIVERS

MC8T13 – Open emitter driver; specified for general TTL systems.

MC8T23 – Open emitter driver; specified to meet IBM system requirements.



All four devices:
T_A = 0 to 75°C

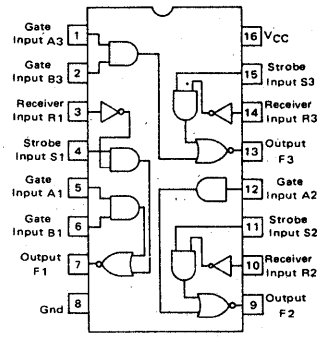
Packages:
L Suffix – Case 620
P Suffix – Case 648

Device Number	V_{OH} @ I_{OH} = -75 mA @ I_{OH} = -59.3 mA* Volts Max	I_{OS} @ V_O = 0 mA Max	t_{PLH} @ C_L = 15 pF ns Max
MC8T13	2.4	-30	20
MC8T23	3.11*	-30	20

TRIPLE LINE RECEIVERS

MC8T14 – Hysteresis-equipped receiver; specified for general TTL systems.

MC8T24 – Hysteresis-equipped receiver; specified to meet IBM system requirements.



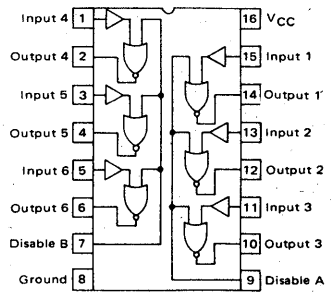
Device Number	$V_{H(R)}$ Volts Min	$I_{IH(R)}$ @ $V_{IH(R)}$ = 3.8 V @ $V_{IH(R)}$ = 3.11 V* mA Max	$t_{PLH(R)}$ @ C_L = 15 pF ns Max
MC8T14	0.3	0.17	30
MC8T24	0.2	0.17*	30

Minicomputer Bus

Transceivers and receivers for bus organized minicomputers employing 120-ohm terminated lines.

HEX RECEIVERS

MC3437 – Hysteresis-equipped for improved noise immunity. DS8837 equivalent.



All three devices:
T_A = 0 to 70°C

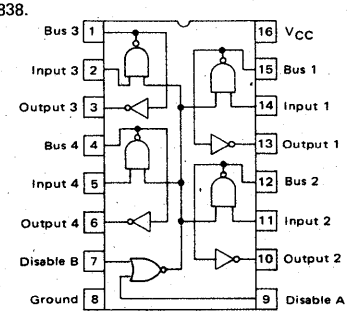
Packages:

MC3437
MC3438 DS6841
L Suffix – Case 620 – J Suffix
P Suffix – Case 648 – N Suffix

$I_{I(R)}$ @ $V_{I(R)}$ = 4.0 V µA Max	Hysteresis Volts Min	$t_{PLH(R)}$ @ C_L = 15 pF ns Max
50	0.5	30

QUAD TRANSCEIVERS

MC3438
DS8641 – Open collector driver outputs allow wire-OR connection. MC3438 has hysteresis-equipped receiver for improved noise immunity (not available with DS8641). MC3438 is equivalent DS8838.



Receiver Hysteresis Volts Min	$V_{L(BUS)}$ @ I_{BUS} = 50 mA Volts Max	I_{BUS} @ $V_{IH(BUS)}$ = 4.0 V µA Max	$t_{PLH(D)}$ @ C_L = 15 pF ns Max	$t_{PLH(R)}$ @ C_L = 15 pF ns Max
0.25*	0.7	100	25	30

*MC3438 only.

Microcomputer Bus

This family of devices is designed to extend the limited drive capabilities of today's standard 6800 and 8080 type NMOS microprocessors. All devices are fabricated with Schottky TTL technology for high speed.

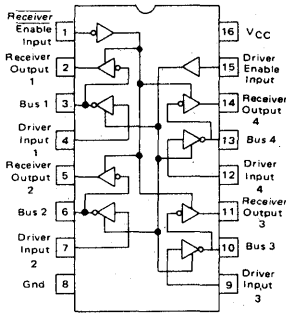
General features include:

- Single +5.0 V Power Supply Requirement
- Three-State Logic Output
- Low Input Loading – 200 μA Max.

DATA BUS EXTENDERS

Quad, Bidirectional, with 3-State Outputs

MC6880A/MC8T26A# – Inverting

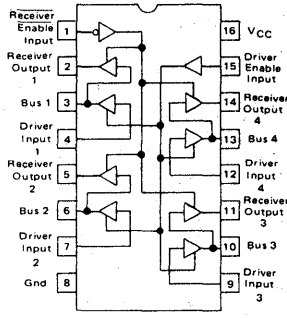


#These devices may be ordered by either of the paired numbers.

Both types:
T_A = 0 to 75°C

Packages:
L Suffix – Case 620
P Suffix – Case 648

MC6889/MC8T28# – Non-inverting

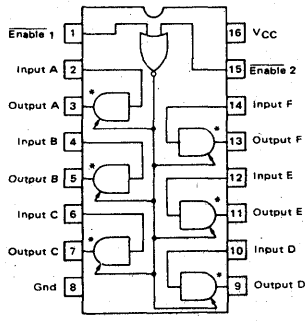


Device Number	Input Current I_{IH} μA Max	Input Current I_{IL} μA Max	I_{OHL} Output Disabled Leakage Current – High Logic State μA Max	t_{PLH}, t_{PHL} Propagation Delay Time – High to Low or Low to High ns Max
MC6880A/MC8T26A	25	-200	100	14
MC6889/MC8T28	25	-200	100	17

ADDRESS AND CONTROL BUS EXTENDERS

Hex, Unidirectional, with 3-State Outputs

MC6885/MC8T95# – Non-inverting
MC6886/MC8T96# – Inverting
Two-input Enable controls all six buffers.



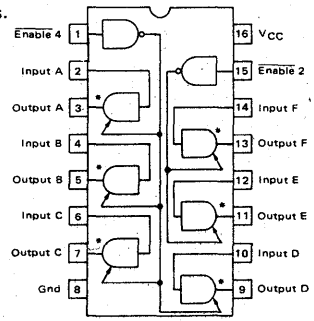
*Add inverter for MC6886/MC8T96.

#These devices may be ordered by either of the paired numbers.

All four types:
T_A = 0 to 75°C

Packages:
L Suffix – Case 620
P Suffix – Case 648

MC6887/MC8T97# – Non-inverting
MC6888/MC8T98# – Inverting
Two Enable inputs, one controlling four buffers and the other controlling the remaining two buffers.



*Add inverter for MC6888/MC8T98.

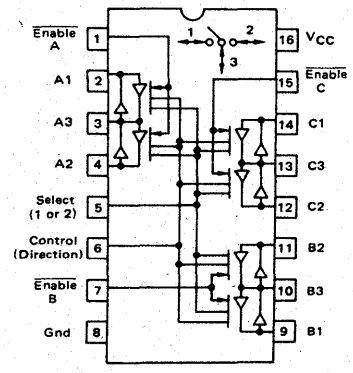
V_{OL} @ I_{OL} = 48 mA Volts Max	V_{OH} @ I_{OH} = -5.2 mA Volts Min	I_{OS} mA Typ	t_{PLH} ns Typ	$t_{P(Enable)}$ ns Typ
0.5	2.4	-80	6.0	11

5

Microcomputer Bus (continued)

BIDIRECTIONAL BUS SWITCH

MC6881/MC3449# — For exchanging TTL level digital information between selected pairs of ports in a 3-port network.



#This device may be ordered by either of the numbers.

Both types:
T_A = 0 to 70°C

Packages:
L Suffix — Case 620
P Suffix — Case 648

V_{OL} @ I_{OL} = 8.0 mA Volts Max	I_{OD} @ V_O = 2.7 V µA Max	I_{IL} @ V_{IL} = 0.4 V µA Max	I_{IH} @ V_{IH} = 2.7 V µA Max
0.5	25	-200	40

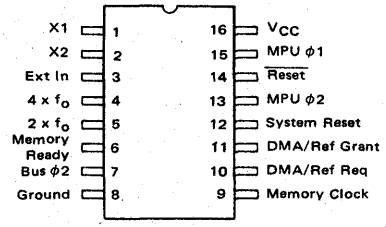
MC6881/MC3449 TRUTH TABLE

Enable	Select	Control	Data Flow
0	0	0	2→3
0	0	1	3→2
0	1	0	1→3
0	1	1	3→1
1	X	X	High Impedance

X - Don't Care

M6800 CLOCK GENERATOR

MC6875 — Provides the non-overlapping two-phase clock signals for M6800 MPU systems.



V_{OLC} = 0.3 V Max
V_{OHC} = V_{CC} − 0.3 V Min
f_{op} = 2.0 MHz Typ

5

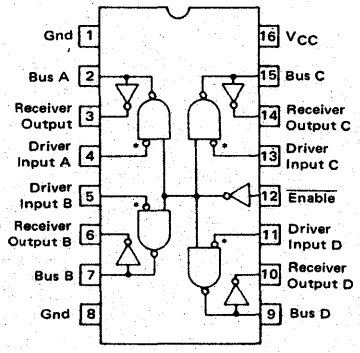
Instrumentation Bus

HIGH-CURRENT PARTY-LINE BUS TRANSCEIVERS

Devices for industrial control and data communication.

MC26S10 — Inverting
MC26S11 — Non-inverting

Quad transceivers with open-collector drivers and PNP-buffered inputs for MOS compatibility.



*Inverter on MC26S11 only.

Both types:
T_A = 0 to 70°C

Packages:
L Suffix — Case 620
P Suffix — Case 648

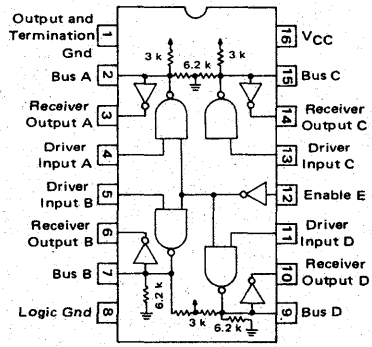
Test	Condition	Limits
V_{OL} (D)	I_{OL} = 100 mA	0.8 Volts Max
I_O (D)	V_{OH} = 4.5 V	100 µA Max
I_{O1}(D)	V_{CC} = 0 V, V_{OH} = 4.5 V	100 µA Max
I_{IH} (D)	V_{IH} = 2.7 V	30 µA Max
I_{IL} (D)	V_{IL} = 0.4 V	-0.54 mA Max
t_P (D)	MC26S10	15 ns Max
	MC26S11	19 ns Max
t_P (R)	Both Types	15 ns Max

Instrumentation Bus (continued)

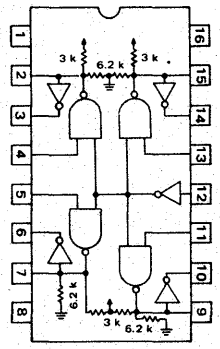
QUAD INTERFACE TRANSCEIVERS

These devices are designed to meet the HP-IB bus specification of IEEE Standard 488-1975, for the interconnection of Measurement Apparatus.

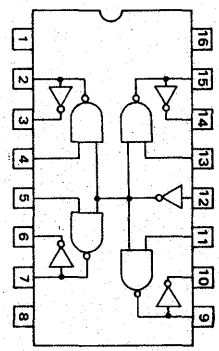
MC3440P – Three drivers with common Enable input; one driver without Enable.



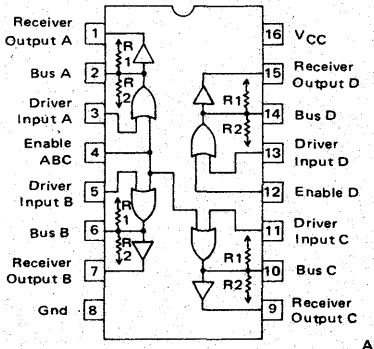
MC3441P – Four drivers with common Enable input.



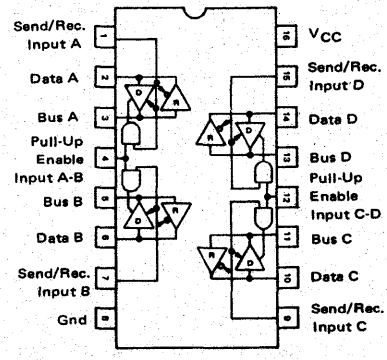
MC3443P – Four drivers with common Enable input; no termination resistors.



MC3446P – For low-power instruments, including MOS.



MC3448P – For common Send-Receive bus; bidirectional.



All types:
T_A = 0 to 70°C

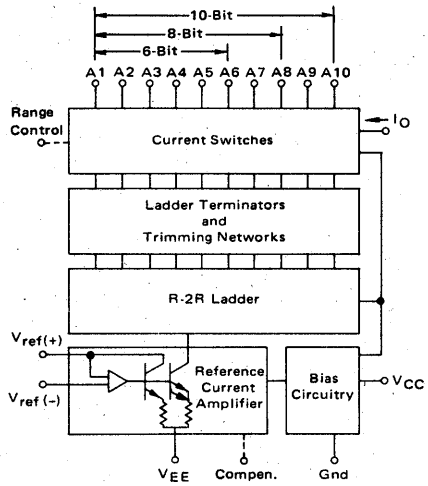
Package – Case 648

Device Number	Receiver Input Hysteresis mV Min	Drive Output Voltage @ I_{OL} = 48 mA; Volts Max	Bus Divider Voltage Volts	t_{PHL} (Driver or Receiver) ns Max
MC3440P	400	0.4	2.6 to 3.75	30
MC3441P	400	0.4	2.6 to 3.75	30
MC3443P	400	0.4	–	25(D) 22(R)
MC3446P	400	0.4	2.5 to 3.7	50
MC3448P	400	0.4	2.5 to 3.7	35

A-D/D-A CONVERSION

Low-cost building blocks for construction of D-A/A-D systems. Involves use of advanced technologies such as ion implantation, laser trimming and CMOS processing where necessary to achieve the required functional capability, operating accuracy and production repeatability.

D-A Converters



--- Dotted terminals available on 6- and 8-bit units only.

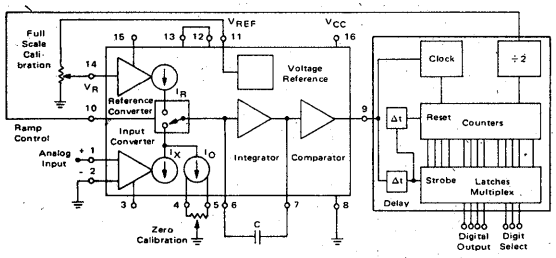
Multiplying D-A converters designed to supply an output current that is a linear product of an analog input reference voltage and a digital input word. Devices for 6-, 8- and 10-bit digital word inputs are available.

Device Number	Error % Max	P_D @ V_{EE} = -5 V mW Max	$t_{Settling}$ ns Typ	I_O @ V_{Ref} = 2 V mA	Suffix	Case
6-Bit						
MC1506*	±0.78	120	150	1.9 to 2.1	L	632
MC1406						
8-Bit						
MC1508L8*	±0.19	170	300	1.9 to 2.1	L	620
MC1408L8						
MC1408L7	±0.39				L, P	620, 648
MC1408L6	±0.78					
MC3408	±0.5				L	620
10-Bit						
MC3510*	±0.05	220	250	3.8 to 4.2	L	690
MC3410						
MC3410C	±0.1				L, P	690, 648

*T_A = -55 to 125°C,
Devices without asterisk: T_A = 0 to 70°C.

A-D Subsystems

2-Chip A-D Converter System Functional Diagram



These devices are relatively complex subsystems. The bipolar, dual-ramp A-D converter has up to 4-1/2-digit conversion capability. The CMOS logic subsystem specifically adapts the A-D converter to a 3-1/2-digit DVM function.

MC1505/1405 – A-D Converter

MC1505L – T_A = -55 to 125°C – Case 620
MC1405L – T_A = 0 to 70°C – Case 620

Linearity Error % Max	Voltage Reference Volts	Temperature Coefficient of Reference %/°C	I_{CC} @ V_{CC} = 5.0 V mA Max
±0.05	1.15 to 1.35	0.005	12

MC14435 – Digital Logic
(See Semiconductor Data Library Vol. 5 for data.)

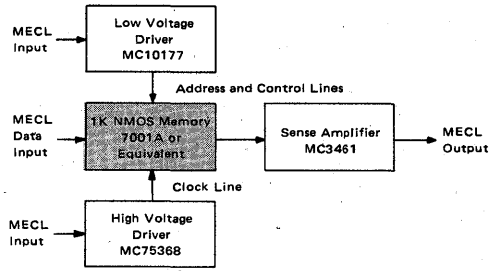
MC14435EFL/EVL* – T_A = -55 to 125°C – Case 620
MC14435FL/VL* – T_A = -40 to 85°C – Case 620
MC14435FP/VP* – T_A = -40 to 85°C – Case 648

P_C(quiescent) @ V_{DD} = 5.0 V mW Max	I_{OL} @ V_{DD} = 5.0 V (Digit Selects) mA Min	I_{OL} @ V_{DD} = 5.0 V (BCD Outputs) mA Min	I_{OL} @ V_{DD} = 5.0 V (All Outputs) mA Min
1.75	1.6	1.6	-0.2

*MC14435EFL/FL/FP: V_{DD} = 3.0 to 18 Vdc
MC14435EVL/VL/VP: V_{DD} = 3.0 to 6.0 Vdc

NMOS Memories to MECL Systems

The high-speed capabilities of some NMOS memories (example: 7001A types) make them desirable for use in conjunction with MECL logic for some applications. Yet, the *positive* input requirements of NMOS memories are incompatible with the negative voltage levels characteristic of the MECL family. Hence, level conversion is required—for both input and output matching of the NMOS memory. The interface devices below include driver/translators to feed the memory inputs and a sense amplifier to match the output.

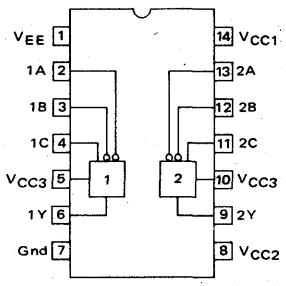


DRIVER/TRANSLATORS

MECL-to-MOS driver/translators convert standard MECL 10,000 input signals to suitable levels for NMOS memory systems. The MC75358 and MC75368 may also be used as positive logic NOR or non-inverting gates.

MC75368
MC75358 } — Dual Clock Line Drivers suitable for driving address, control, and timing inputs.

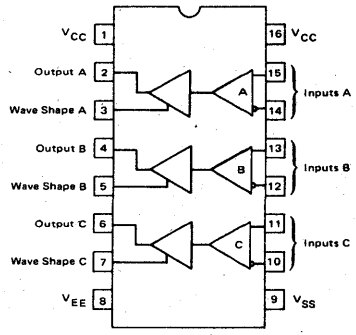
MC10177L — Triple Line Driver for driving address and control inputs.



T_A = -30 to 85°C
Package — Case 620

T_A = 0 to 70°C
Packages:
L Suffix — Case 632
P Suffix — Case 646

Maximum Supply Voltage:
MC75368 = 18 V
MC75858 = 22 V



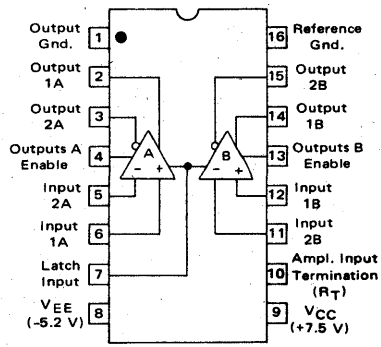
Device Number	V_{OH} Volts Min	@ I_{OH} mA	V_{OL} Volts Max	@ I_{OL} mA	t_{DHL} ns Max	@ C_L pF
MC75368	V_{CC2} - 0.3	0.1	0.3	10	26	300
MC75358	V_{CC2} - 0.3	0.1	0.3	10	24	390
MC10177	4.0	15	0.5	1.0	6.0	350

SENSE AMPLIFIER

MC3461L — Dual Sense Amplifier with MECL 10,000-compatible control inputs and complementary, open-emitter outputs. Designed for 7001 and 2105 type NMOS 1K RAMs.

T_A = 0 to 75°C
Package — Case 620

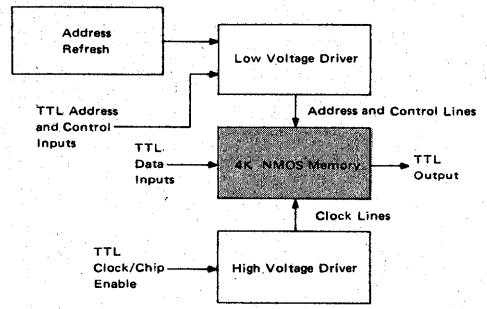
I_{TH} μA Max	t_{PD} (Amplifier) ns Max	t_{PD} (Enable) ns Max
±200	10	5.0



5

NMOS Memories to TTL Systems

The highly capacitive loads represented by NMOS memories are, in themselves, incompatible with the drive capabilities of conventional TTL logic circuits. So, also, are some of the voltage levels. The devices shown are used to match TTL capabilities to various types of popular NMOS memories.

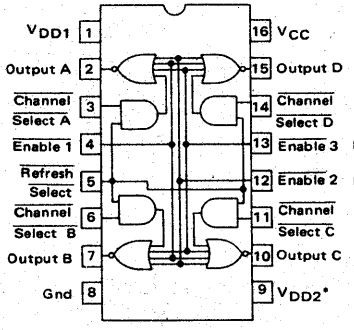


CLOCK AND CHIP ENABLE LINE DRIVERS (High Level)

MC3460, MC3466, MC3245 — Quad Clock Drivers with Refresh Select Logic

MC75365 — Quad Clock Driver or High-Current NAND Gate

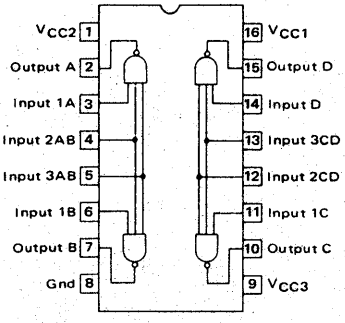
MMH0026, MMH0026C — Dual Clock Driver



*MC3245 — no connection; V_{DD2} not required.

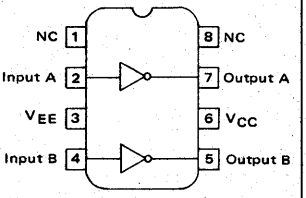
T_A = 0 to 70°C

Packages:
L Suffix — Case 620
P Suffix — Case 648



T_A = 0 to 70°C

Packages:
L Suffix — Case 620
P Suffix — Case 648



(Pin Connections for U or P1 Package)

T_A:
MMH0026 — −55 to 125°C
MMH0026C — 0 to 70°C

Packages
G Suffix — Case 601
L Suffix — Case 632
U Suffix — Case 693
P1 Suffix — Case 626 (For MMH0026C only)

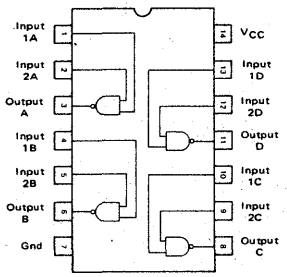
Device Number	V_{OH} Volts Min	@ I_{OH} mA	V_{OL} Volts Max	@ I_{OL} mA	t_{DHL} ns Max	@ C_L pF	Feature
MC3460	V_{DD1} − 1.0	−2.0	0.55	40	23	480	Specified for use with 4K NMOS dynamic memories.
MC3466	V_{DD1} − 1.3	−40	0.55	40	24	480	Specified for use with 1K NMOS dynamic memories (e.g., 7001A types).
MC3245	V_{DD} − 0.5	−1.0	0.45	5.0	32	250	Does not require second high voltage supply. Low input loading.
MC75365	V_{CC2} − 0.3	−0.1	0.3	10	18	200	Derives V_{CC1} power from TTL 5-V supply, and V_{CC2} and V_{CC3} from V_{SS} and V_{BB} supplies from NMOS memories.
MMH0026 MMH0026C	V_C − 1.0	0.4 V*	V_{EE} + 1.0	2.4 V*	12	1000	For very high capacitance loads.

*@ $V_I - V_{EE}$

NMOS Memories to TTL Systems (continued)

DATA AND ADDRESS LINE DRIVERS
(Low Level)

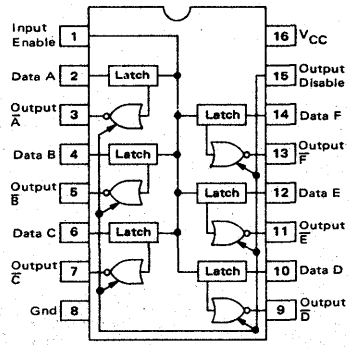
MC3459 — Quad Address Line Driver



T_A = 0 to 70°C

Packages:
L Suffix — Case 632
P Suffix — Case 646

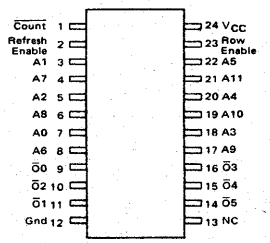
DS3645 / DS3675 — Hex 3-State Latch/Drivers. Output dumping resistor on DS3675



T_A = 0 to 75°C

Packages:
J Suffix — Case 620
N Suffix — Case 648

MC3232A — Address Multiplexer and Refresh Counter



T_A = 0 to 75°C

Packages
L Suffix — Case 649
P Suffix — Case 623

Device Number	V_{OH} Volts Min	@ I_{OH} mA	V_{OL} Volts Max	@ I_{OL} mA	Propagation Delay ns Max	@ C_L pF	Features
MC3459	2.4	-2.0	0.7	80	26	360	High fan-out capability.
DS3645	2.4	-1.0	0.6	20	25 Typ	500	Extremely low input currents for MOS input compatibility.
DS3675	2.5	-1.0	0.3	20			
MC3232A	2.8	-1.0	0.4	50	25	250	Multiplexes the 12 address bits to the 6 input address pins of 16-pin 4K RAMs.

MEMORY I/O REGISTERS
(Hex)

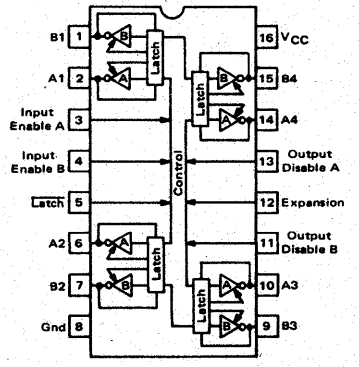
B Output

DS3647 — Inverting, 3-State
DS3677 — Non-inverting, 3-State
DS36147 — Inverting, Open Collector
DS36177 — Non-inverting, Open Collector

These registers, with two I/O ports per bit, can handle bidirectional data, with the direction of data controlled by Input Enables. An Expansion input disables both A and B outputs to permit multiplexing of other registers.

T_A = 0 to 70°C

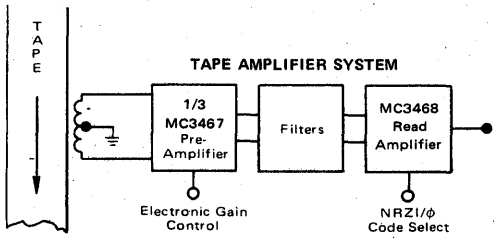
Packages:
J Suffix — Case 620
N Suffix — Case 648



Magnetic Memories to TTL Systems

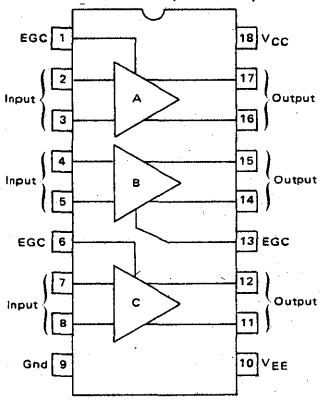
SENSE AMPLIFIERS

. . . for Magnetic Tape Memories



A two-component preamplifier/amplifier combination that provides the interface between magnetic tape heads and digital logic. Suitable for both open reel and cartridge tape systems. Triple preamp has individually adjustable gain controls. LSI Read Amplifier performs peak detection and threshold detection functions, as required for NRZI/phase encoded recording formats.

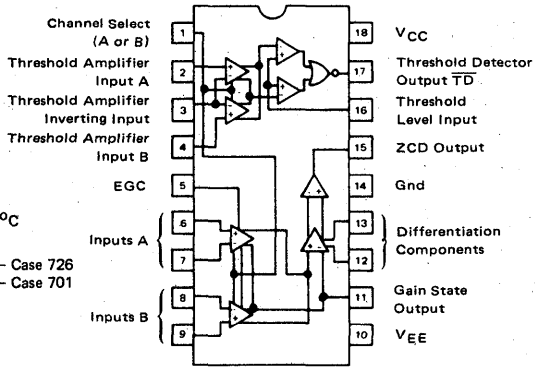
MC3467 – Triple Preamplifier



Both types:
T_A = 0 to 70°C

Packages:
L Suffix – Case 726
P Suffix – Case 701

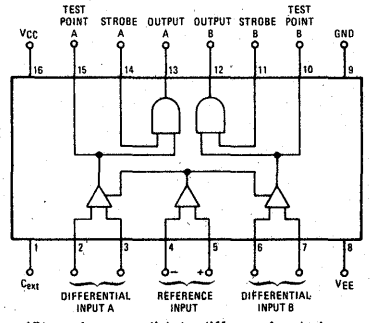
MC3468 – Read Amplifier



. . . for Core Memories

Feature adjustable threshold, time and amplitude signal discrimination, dual inputs with independent outputs, and a range of options.

Representative Diagram (MC5528/29)*



*Pin assignment slightly different for devices without test points.

	T_A = -55 to 125°C		T_A = 0 to 70°C		Test Points
AND Output	MC5524 MC5528	MC5525 MC5529	MC7524 MC7528	MC7525 MC7529	No Yes
NAND Output	MC5534 MC5538	MC5535 MC5539	MC7534 MC7538	MC7535 MC7539	No Yes
V_{TH} @ V_{Ref} = 15 mV =	10 to 20 mV	8 to 22 mV	11 to 19 mV	8 to 22 mV	
V_{TH} @ V_{Ref} = 40 mV	35 to 45 mV	33 to 47 mV	36 to 44 mV	33 to 47 mV	
Max I_{IB} =	100 μA	100 μA	75 μA	75 μA	
Max t_{PLH} @ C_L = 15 pF =	40 ns	40 ns	40 ns	40 ns	
Packages	L Suffix – Case 620		L Suffix – Case 620 P Suffix – Case 648		

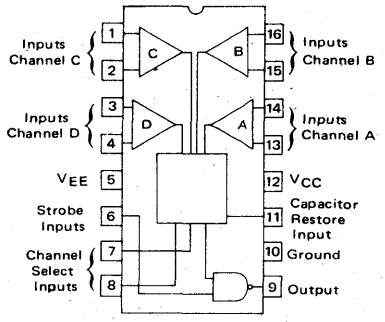
Magnetic Memories to TTL Systems (continued)

SENSE AMPLIFIERS (continued)

. . . for Plated Wire and Thin-Film Memories and other low-level sensing applications.

MC1544 – T_A = -55 to 125°C
MC1444 – T_A = 0 to 70°C
Features 4-channel input with decoded channel selection and strobed output capability.

Packages:
MC1544
L Suffix – Case 620
F Suffix – Case 650
MC1444
L Suffix – Case 620

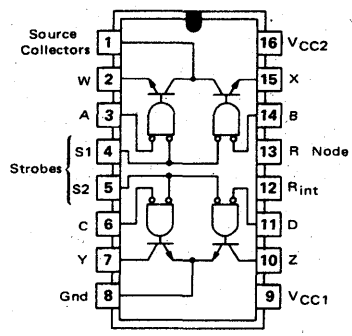


Device Number	V_{TH} mV	V_{OH} @ I_{OH} = -400 μA Volts Min	V_{OL} @ I_{OL} = 10 mA Volts Max	t_{PD} ns Max
MC1544	0.5 to 1.5	2.4	0.5	25
MC1444	0.3 to 2.3	2.4	0.5	25

CORE DRIVER

MC55325 – T_A = -55 to 125°C
MC75325 – T_A = 0 to 70°C
Contains two source switches and two sink switches. Source and sink selection is determined by one of two logic inputs, and turn-on is determined by the appropriate strobe.

Packages:
L Suffix – Case 620
F Suffix – Case 650
P Suffix – Case 648 (MC75325 only)



Device Number	V_{sat} @ I_{sink} or I_{source} = 600 mA Volts Max	I_{off} @ V_{CC2} = 24 V μA Max	t_{PLH} (Source) ns Max	t_{PLH} (Sink) ns Max
MC55325	0.70	150	50	45
MC75325	0.75	200	50	45

COMPUTER AND TERMINAL INTERFACE

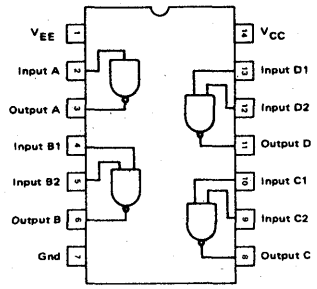
LINE DRIVERS AND RECEIVERS
for Modem/Terminal Applications

Voltage Mode

RS-232C SPECIFICATION

DRIVER

MC1488 – Quad; output current limiting.

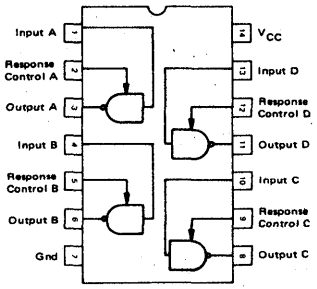


All devices:
T_A = 0 to 70°C
Package:
L Suffix – Case 632

V_{OH} @ V_{CC}/V_{EE} = ±9.0 V Volts Min	V_{OL} @ V_{CC}/V_{EE} = ±9.0 V Volts Max	I_{OS} mA	t_{PHL} @ C_L = 15 pF ns Max
6.0	-6.0	±6.0 to 12	175

RECEIVERS

MC1489 – Quad; 0.25 V input hysteresis.
MC1489A – Quad; 1.1 V input hysteresis.

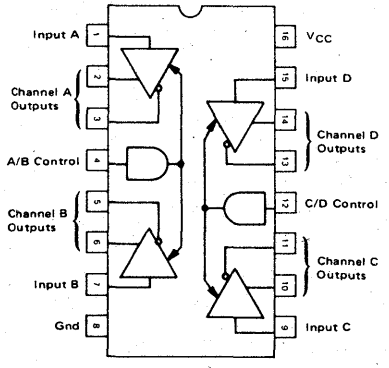


Device Number	Input V_{IHL} Volts	Input V_{ILH} Volts	t_{PHL} @ R_L = 390 Ω ns Max
MC1489	1.0 to 1.5	0.75 to 1.25	50
MC1489A	1.75 to 2.25	0.75 to 1.25	50

RS-422/423 SPECIFICATION

DRIVER

MC3487 – Quad; three-state outputs.

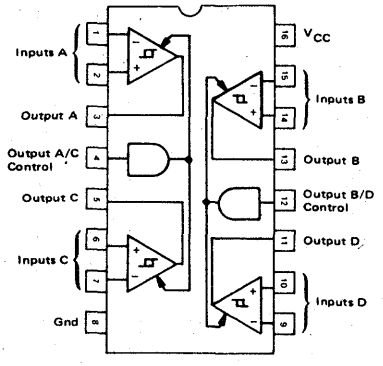


Both devices:
T_A = 0 to 70°C
Packages:
L Suffix – Case 620
P Suffix – Case 648

V_{OH} @ I_{OH} = 50 mA Volts Min	V_{OL} @ I_{OL} = 48 mA Volts Max	V_{OD}(Differential) @ R_L = 100 Ω Volts Min	t_{PLH}/t_{PHL} ns Typ
2.0	0.5	2.0	15

RECEIVER

MC3486 – Quad; three-state outputs and input hysteresis.

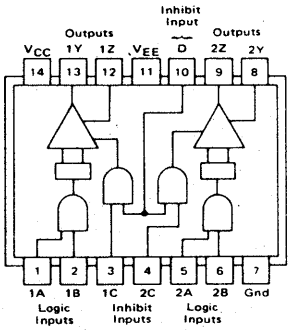


$V_{TH(D)}$ @ V_{ICM} = ±7.0 V Volts Max	I_{ID} @ V_{ID} = ±10 V V_{CC} = 0 to 5.25 V mA Max	t_{PHL}/t_{PLH} ns Typ	$t_{P(Control)}$ ns Typ
±0.2	±3.25	20/25	25

Differential Current Mode

DRIVERS

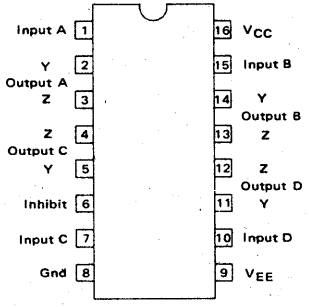
MC75110 – Dual; industry standard.



T_A = 0 to 70°C
(MC75xxx)
-55 to 125°C
(MC55xxx)

Packages:
L Suffix – Case 632
P Suffix – Case 646
(MC75xxx only)

MC3453 – Quad; common inhibit input; current sink approximately 12 mA.



All three devices:
T_A = 0 to 70°C

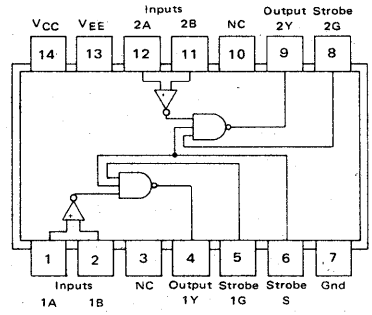
Packages:
L Suffix – Case 620
P Suffix – Case 648

BOTH DRIVERS

I_O (on) mA Min	I_O (off) µA Max	t_{PHL} ns Max
6.5	100	15

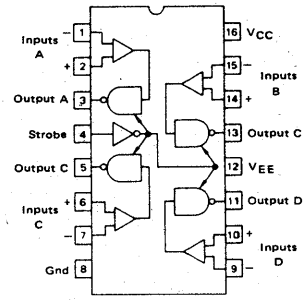
RECEIVERS

MC75107/MC55107 – Dual; active pullup output.
MC75108/MC55108 – Dual; open collector output.



MC3450 – Quad; active pullup outputs; common three-state enable.

MC3452 – Quad; open collector outputs.



ALL RECEIVERS

Input V_{TH} mV Max	I_{IH} @ V_{ID} = 0.5 V µA Max	I_{IL} @ V_{ID} = -2.0 V µA Max	t_{PLH} ns Max
±25	75	-10	25

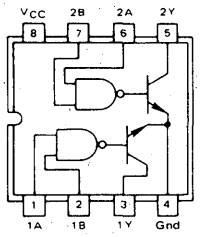
PERIPHERAL INTERFACE

Dual Drivers

. . . for relays, lamps, and other peripherals requiring more power than generally available from logic gates.

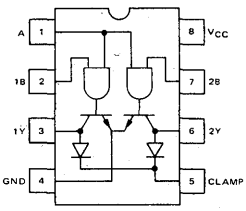
Representative Diagrams

MC754xx Series



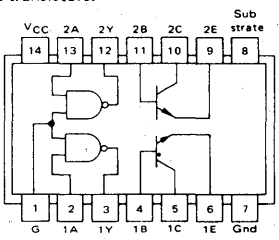
(MC75451/MC75461)

MC147x Series



(MC1472)

MC75450 – Similar to MC75451, but with uncommitted output transistors.



Logic gates vary to provide output shown:

Logic Output (Including Transistor Inversion)	$-BV_{CER}$			
	30 V	30 V	35 V	70 V Hi-Z Input
AND	MC75451	SN75451B*	MC75461	MC1471#
NAND	MC75452	SN75452B*	MC75462	MC1472
OR	MC75453	SN75453B*	MC75463	MC1473#
NOR	MC75454	SN75454B*	MC75464	MC1474#

*Same as equivalent MC types, but with guaranteed switching limits.
#To be introduced.

All Devices
T_A = 0 to 70°C

Packaging:
MC75450
L Suffix – Case 632
P Suffix – Case 646
MC75451–54/MC75461–64
P Suffix – Case 626
U Suffix – Case 693
MC1471–74
P1 Suffix – Case 626
U Suffix – Case 693

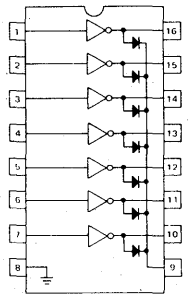
Driver Arrays

. . . Seven Darlington transistors with output clamp diodes.

Device Number	Application	Input Element
MC1411	General Purpose	Basic
MC1412	14–25 V PMOS	Zener and Series 10.5 kΩ resistor
MC1413	5 V CMOS or TTL	Series 2.7 kΩ resistor
MC1416	8–18 V MOS	Series 10.5 kΩ resistor

All Types:
V_{Max} = 50 V
I_{Max} = 500 mA
T_A = 0 to 85°C

Packages:
L Suffix – Case 620
P Suffix – Case 648

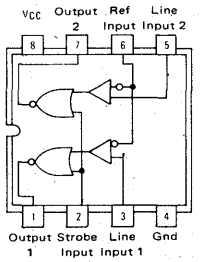


Dual Receiver

MC75140P1 – Dual single-ended receiver with common strobe and reference inputs for maximizing noise immunity. Useful for bus-organized (party line) TTL systems.

V_{TH}	V_{Ref}	$t_{PLH(L)}$
±100 V	1.5 to 3.5 V	35 ns

T_A = 0 to 70°C
Package – Case 626

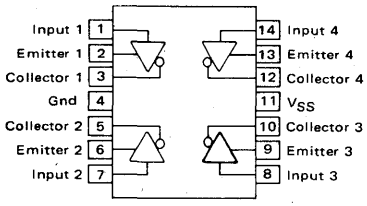


NUMERIC DISPLAY INTERFACE

. . . for mating multiplexed LED or gas discharge numeric displays to MOS or TTL logic systems.

LED Drivers for Common-Cathode Displays

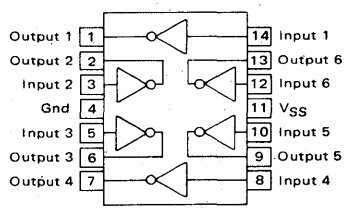
MC75491 – Quad segment driver



Both Devices:
T_A = 0 to 70°C

Packages:
L Suffix – Case 632
P Suffix – Case 646

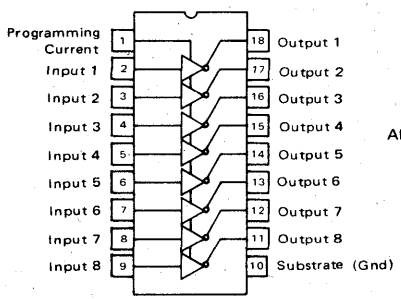
MC75492 – Hex digit driver



Device Number	I_I @ V_I = 10 V mA Max	V_{OL} Volts Max	@ I_{OL} mA	V_{SS} Volts Max
MC75491	3.3	1.2	250	10
MC75492	3.3	1.2	50	10

Gas Discharge Drivers

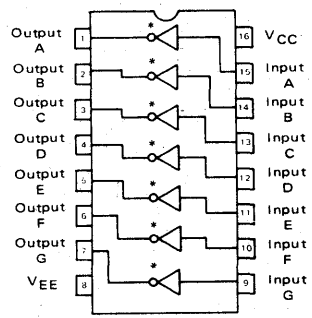
MC3491
MC3492 – Eight segment cathode drivers with programmable current.



All Devices:
T_A = 0 to 70°C

Package: P Suffix – Case 701

MC3490 – High Level
MC3494 – Low Level
Seven digit anode drivers



*Inverter on MC3494 only.
Package: P Suffix – Case 648

Device Number	Output ON Current mA Max	Breakdown Voltage Volts Min	Current Deviation (All 8 Outputs) % Max	Output Voltage Compliance Range Volts
MC3491	1.85	80	10	5.0 to 50
MC3492	5.25	80	10	5.0 to 50

Device Number	Breakdown Voltage Volts Min	Input Voltage (OFF-State) Volts	Input Voltage (ON-State) Volts	Input Current μA Max
MC3490	48	-5.0 Min	-2.0 Max	450
MC3494	48	-2.0 Max	-5.0 Min	-350

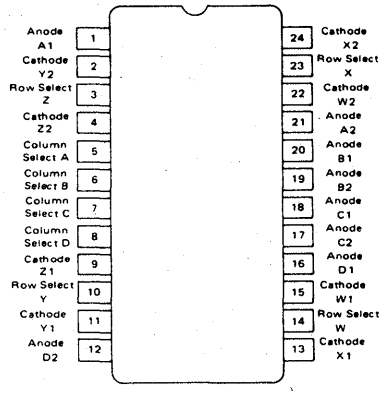
5

Crosspoint Switch

MC3416 – Low-cost solid-state crosspoint switch offers important advantages in modern telephone exchanges employing space-division switching. Features 4 x 4 two-wire monolithic structure for PABX applications. Select inputs are both CMOS and TTL compatible.

T_A = 0 to 70°C

Packages:
P Suffix – Case 649
L Suffix – Case 623



r_{off} @ V_{AK} = 10 V MΩ Min	r_{on} @ I_{AK} = 20 mA Ohms Max	BV_{AK} BV_{KA} Volts Min	V_{AK} @ I_{AK} = 20 mA Volts Max
100	10	25	1.1

Voice Encoding/ Decoding

Simplified voice encoding/decoding using continuous Variable Slope Delta Modulator (CVSD) technique.

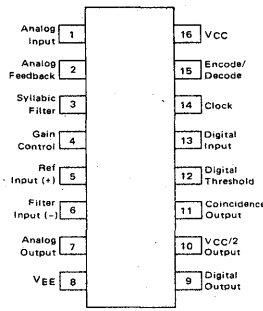
MC3417 – 3-bit algorithm; for military secure communication applications.

MC3418 – 4-bit algorithm; telephone quality.

T_A = 0 to 70°C*

Packages:
L Suffix – Case 620
P Suffix – Case 648

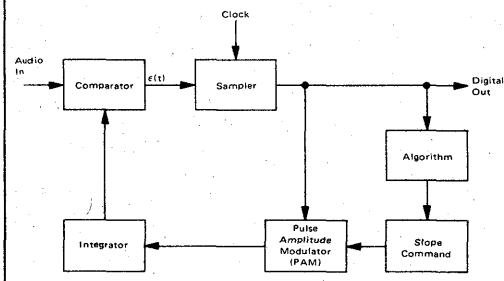
*Military temperature range devices (MC3517/18) to be offered in early 1977.



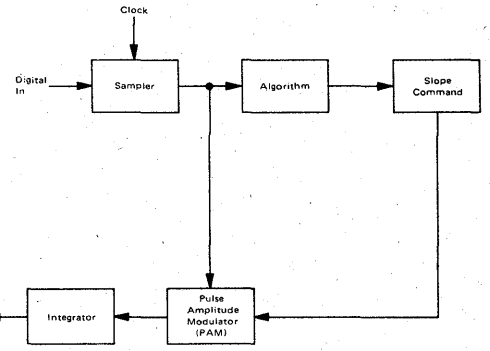
Device Number	Sample Rate Samples/s Typ	Total Loop Offset Voltage mV Max	t_{PD}, Clock Trigger to Output μs Max
MC3417	16 k	±5.0	2.5
MC3418	38 k	±2.0	2.5

Block Diagrams

CVSD Encoder



CVSD Decoder



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DS3645
DS3675

Product Preview

HEX LATCH/DRIVERS FOR MOS MEMORIES

These latch/drivers are intended to drive capacitive loads up to 500 pF associated with MOS memory systems. They feature PNP buffered inputs for low input loading, Schottky technology for high speed, and three-state configuration for bus type operation.

Fall-through latches are utilized which capture the data in parallel with the output, thereby eliminating the delay encountered in other latch circuits. The devices may be used either for the address or input/out data lines in MOS memory systems.

The DS3645 version provides an internal 15 ohm series damping resistor on each output, while the DS3675 features a low impedance output for use with or without an external resistor.

- Low Input Loading Ensured by PNP Buffered Inputs
- Heavy Drivers for Highly Capacitive Loads
- Three-State Outputs Permit Multiplying Outputs
- Schottky Technology for High Speed

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage, High Logic State	V_{IH}	7.0	Vdc
Input Voltage, Low Logic State	V_{IL}	-1.5	Vdc
Output Current, High Logic State	I_{OH}	-1.0	A
Output Current, Low Logic State	I_{OL}	1.0	A
Operating Ambient Temperature	T_A	0 to 70	°C
Storage Temperature	T_{stg}	-65 to 150	°C
Junction Temperature Plastic Package Ceramic Package	T_A	 150 175	°C

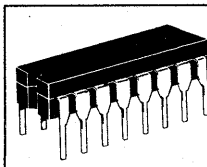
TRUTH TABLE

Input Enable	Output Disable	Data Input	Output	Operation
H	L	H	L	Data Feed Thru
H	L	L	H	Data Feed Thru
L	L	X	Q	Latched to Data Present When Enable Went Low
X	H	X	Z	High Impedance Output

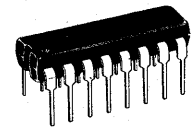
This is advance information and specifications are subject to change without notice.

HEX THREE-STATE LATCH/DRIVERS

SCHOTTKY
SILICON MONOLITHIC
INTEGRATED CIRCUIT

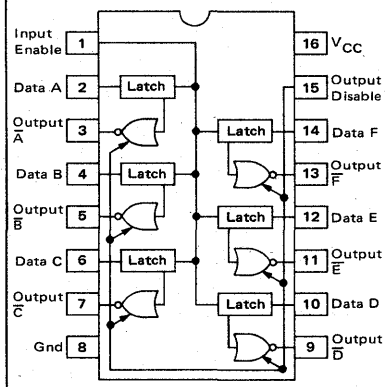


J SUFFIX
CERAMIC PACKAGE
CASE 620



N SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
DS3645N	0 to 70°C	Plastic DIP
DS3645J	0 to 70°C	Ceramic DIP
DS3675N	0 to 70°C	Plastic DIP
DS3675J	0 to 70°C	Ceramic DIP

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ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = 0 to +70°C, typical values measured at T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Voltage, Low Logic State		V_{IL}	–	–	0.8	V
Input Voltage, High Logic State		V_{IH}	2.0	–	–	V
Input Current, Low Logic State (V_{IL} = 0.5 V, V_{CC} = 5.5 V)		I_{IH}				μA
	Enable Input		–	-90	-250	
	Data Inputs		–	-180	-500	
Input Current, High Logic State (V_{IH} = 5.5 V, V_{CC} = 5.5 V)		I_{IH}				μA
	Enable Input		–	0.1	40	
	Data Inputs		–	–	80	
Input Clamp Voltage (V_{CC} = 4.5 V, I_{IC} = -18 mA)		V_{IC}	–	–	-1.2	V
Output Voltage, Low Logic State (V_{CC} = 4.5 V, I_{OL} = 0)		V_{OL}	–	0.25	0.45	V
(V_{CC} = 4.5 V, I_{OL} = 20 mA)	DS3645		–	0.6	1.1	
	DS3675		–	0.3	0.5	
Output Voltage, High Logic State (V_{CC} = 4.5 V, I_{OH} = 0)		V_{OH}	3.4	4.25	–	V
(V_{CC} = 4.5 V, I_{OH} = 1.0 mA)	DS3645		2.4	3.5	–	
	DS3675		2.5	3.5	–	
Output Driver Current, Low Logic State (V_{CC} = 4.5 V, V_O = 0 V) (Add 15 Ω series resistor on DS3675)		I_{DO}	–	170	–	mA
Output Driver Current, High Logic State (V_{CC} = 4.5 V, V_O = 4.5 V) (Add 15 Ω series resistor on DS3675)		I_{DH}	–	170	–	mA
Maximum Power Supply Current (V_{CC} = 5.5 V)		$I_{CC(max)}$	–	60	–	mA
Minimum Power Supply Current (V_{CC} = 5.5 V)		$I_{CC(min)}$	–	40	–	mA

SWITCHING CHARACTERISTICS (Add 15 Ω series resistor on DS3675 version. V_{CC} = 5.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Typ	Unit
Propagation Delay Time, Data Input to Output			ns
(C_L = 50 pF)	t_{PHL}	7.0	
(C_L = 250 pF)		15	
(C_L = 500 pF)		25	
(C_L = 50 pF)	t_{PLH}	7.0	
(C_L = 250 pF)		15	
(C_L = 500 pF)		25	
Setup Time on Data Inputs Before Input Enable Goes Low	t_{setup}	0	ns
Hold Time on Data Inputs After Input Enable Goes Low	t_{hold}	10	ns
Propagation Delay Time, Disable Input to Output			ns
High Impedance to Logic Low (C_L = 50 pF, R_L = 2 kΩ to V_{CC})	t_{PZL}	15	
High Impedance to Logic High (C_L = 50 pF, R_L = 2 kΩ to Gnd)	t_{PZH}	15	
Logic Low to High Impedance (C_L = 50 pF, R_L = 400 Ω to V_{CC})	t_{PLZ}	15	
Logic High to High Impedance (C_L = 50 pF, R_L = 400 Ω to Gnd)	t_{PHZ}	15	

SWITCHING TIMES WAVEFORMS AND CIRCUITS

FIGURE 1 – DATA INPUT TO OUTPUT

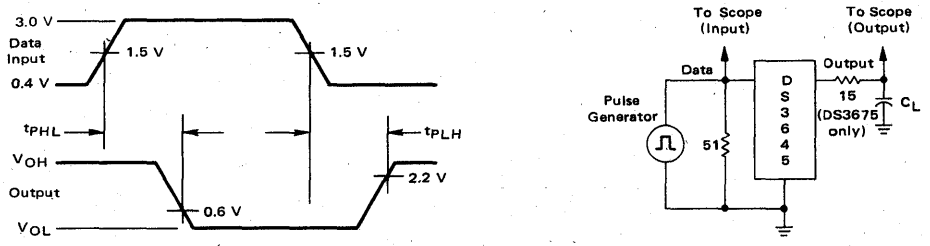


FIGURE 2 – HIGH IMPEDANCE TO OUTPUT LEVEL

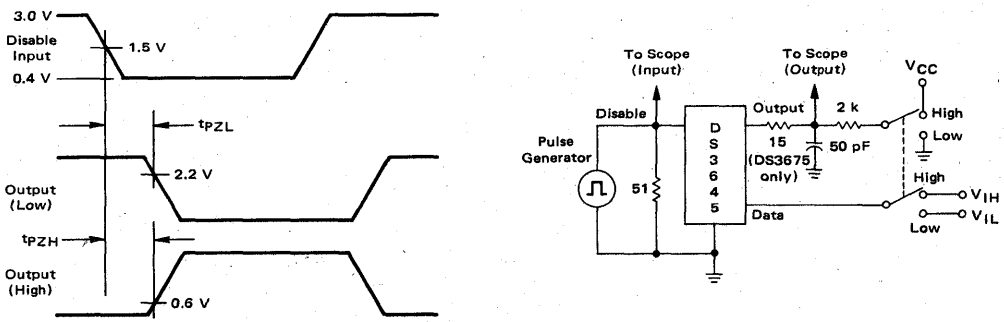
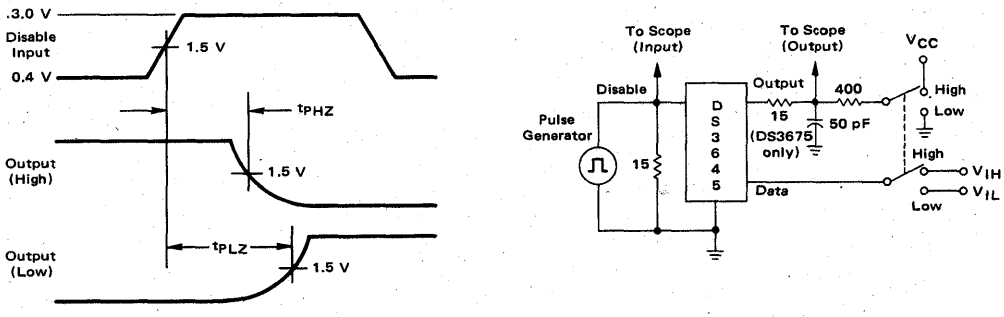


FIGURE 3 – LOGIC LEVEL TO HIGH IMPEDANCE



DS3647,DS36147
DS3677,DS36177

Product Preview

QUAD THREE-STATE MOS MEMORY I/O REGISTERS

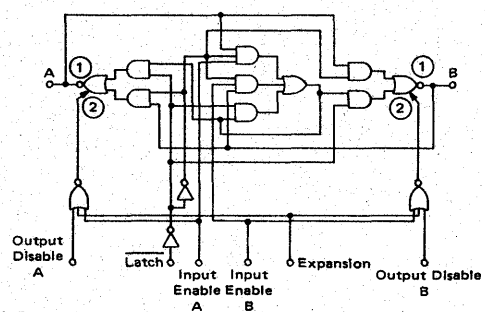
These 4-bit bidirectional I/O buffer registers are well suited for MOS memory systems. They all employ Schottky technology for high speed fall-through latches which capture data in parallel with the output, and PNP buffered inputs for low input loading and MOS campatatibility.

The DS3647 and DS3677 feature three-state logic on the B nodes while the DS36147 and DS36177 use open-collector nodes. All types have three-state logic on the A nodes. Data flowing from node A to B is inverted on the DS3647 and DS36147 and not inverted on the remaining types.

The architecture of these registers with two pins per bit allows them to handle both input and output data. Direction of flow is controlled by the Input Enables. The latch control causes the register to hold the data present at the time $\overline{\text{Latch}}$ is taken low and to display the data at the outputs. Data can be latched into the register without regard to the condition of the Output Disable or Expansion Inputs. The Output Disables may be used to take either or both outputs to the high impedance state (B node on DS3647 and DS3677 version only). The Expansion Input disables both A and B outputs to permit multiplexing other registers.

- Schottky Technology for High Speed – 15 ns (Typ)
- Fall-Through Latches for Minimum Delay
- PNP Buffered Input for Low Input Loading
- Choice of Inverting or Non-Inverting Version
- Bidirectional Data Flow
- Provisions for Easy Expansion
- Choice of Either Three-State or Open-Collector Line Driver Type Output (B)

EQUIVALENT LOGIC (¼ of Device Shown)



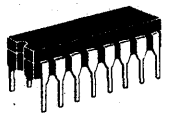
Device	B_{output}
DS3647	Inverting – Three State
DS3677	Noninverting – Three State
DS36147	Inverting – Open Collector
DS36177	Noninverting – Open Collector

NOTES:
1) Inverting for DS36147 and DS3647 only
2) Open Collector Output for DS36147 and DS36177

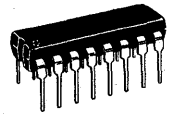
This is advance information and specifications are subject to change without notice.

QUAD THREE-STATE MOS MEMORY I/O REGISTERS

SCHOTTKY
SILICON MONOLITHIC
INTEGRATED CIRCUIT

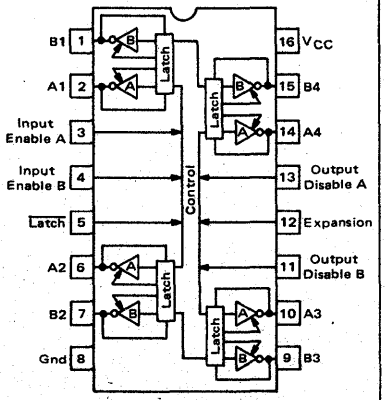


J SUFFIX
CERAMIC PACKAGE
CASE 620



N SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



ORDERING INFORMATION Temperature Range – (All Types) 0 to +70°C	
Device	**Package**
DS3647N, DS3677N	Plastic DIP
DS36147N, DS36177N	Plastic DIP
DS3647J, DS3677J	Ceramic DIP
DS36147J, DS36177J	Ceramic DIP

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MAXIMUM RATINGS (T_A = 25°C unless otherwise noted).

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	-1.5 to +7.0	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-50 to +150	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 0 to +70°C, typical values at T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State	V_{IL}	–	–	0.8	V
Input Voltage — High Logic State	V_{IH}	2.0	–	–	V
Input Current — Low Logic State (V_{CC} = 5.5 V, V_{IL} = 0.5 V) $\overline{\text{Latch}}$, Disable Inputs Data Pins (A or B) Enable Inputs	I_{IL}	 – – –	 – – –	 -200 -400 -1250	μA
Input Current — High Logic State (V_{CC} = 5.5 V, V_{IH} = 5.5 V) $\overline{\text{Latch}}$, Disable Inputs Data Pins (A or B) Enable Inputs	I_{IH}	 – – –	 – – –	 40 80 200	μA
Input Clamp Voltage (V_{CC} = 4.5 V, I_{IC} = -18 mA)	V_{IC}	–	–	-1.2	V
Output Voltage — Low Logic State A Port (V_{CC} = 4.5 V, I_{OL} = 20 mA) B Port (V_{CC} = 4.5 V, I_{OL} = 100 mA)	V_{OL}	 – –	 – –	 0.5 0.7	V
Output Voltage — High Logic State A Port (V_{CC} = 4.5 V, I_{OH} = -1.0 mA) B Port (V_{CC} = 4.5 V, I_{OH} = -5.2 mA) DS3647, DS3677 only	V_{OH}	 2.7 2.4	 3.4 3.3	 – –	V
Power Supply Current (V_{CC} = 5.5 V)	I_{CC}	–	–	100	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Propagation Delay Time — A to B or B to A (C_L = 50 pF)	 t_{PLH} t_{PHL}	 – –	 7.0 7.0	 – –	ns
Propagation Delay Time — Disable to A or B Output (C_L = 50 pF, R_L = 390 Ω to V_{CC}) DS3647, DS3677 only (C_L = 50 pF, R_L = 390 Ω to Gnd) DS3647, DS3677 only (C_L = 50 pF, R_L = 2.0 k to V_{CC}) DS3647, DS3677 only (C_L = 50 pF, R_L = 2.0 k to Gnd) DS3647, DS3677 only	 t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	 – – – –	 15 15 15 15	 – – – –	ns
Setup Time of Data Input Before $\overline{\text{Latch}}$ Goes Low	t_{setup}	–	0	–	ns
Hold Time of Data Input After $\overline{\text{Latch}}$ Goes Low	t_{hold}	–	7.0	–	ns

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TRUTH TABLE

Input Enables			Output Disables					
A	B	$\overline{\text{Latch}}$	A	B	Expansion	A1-A4	B1-B4	Comments
H	L	H	L	L	L	$\overline{Z}$	$\overline{A}$	Data Input A, Output B
L	H	H	L	L	L	$\overline{B}$	$\overline{Z}$	Data Input B, Output A
H	L	L	L	L	L	Hi-Z	$\overline{Q}$	Data stored which is present when $\overline{\text{Latch}}$ went low
L	H	L	L	L	L	$\overline{Q}$	Z	Data stored which is present when $\overline{\text{Latch}}$ went low
H	L	X	L	H	L	Z	Z	Both A and B Hi-Z Data Input on A, may be latched
L	H	X	H	L	L	Z	Z	Both A and B Hi-Z Data Input on B, may be latched
X	X	X	X	X	H	Z	Z	Both A and B Hi-Z

H = High Logic State
L = Low Logic State
X = Don't Care
Z = High Impedance "Third" State

NOTES:
1) Hi-Z on DS3647 and DS3677 Three-State types only.
2) Data may be Latched into the register independent of the Output Disables or Expansion.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section
T_A = Maximum Desired Operating Ambient Temperature.
$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

DS8641

Advance Information

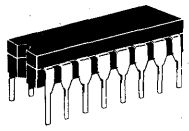
QUAD UNIFIED TRANSCEIVER

Consists of four pair of drivers and receivers with the output of each driver connected to the input of its mating receiver. These devices are intended for use in bus organized data transmission system employing terminated 120 Ω lines. A disable function consisting of a two-input NOR gate is provided to control all four drivers. Up to 27 driver/receiver pairs can share a common line.

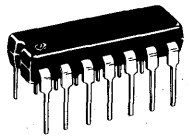
- Receiver Input Threshold Is Not Affected by Temperature
- Open Collector Driver Outputs Allow Wire-OR
- TTL Compatible Receiver Outputs and Disable and Driver Inputs
- Driver Propagation Delay = 15 ns
- Receiver Propagation Delay = 20 ns
- Guaranteed Minimum Bus Noise Immunity = 0.6 V
- Low Bus Terminal Current (Supply On or Off) = 30 μs typ

QUAD UNIFIED BUS TRANSCEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



J SUFFIX
CERAMIC PACKAGE
CASE 620



N SUFFIX
PLASTIC PACKAGE
CASE 648

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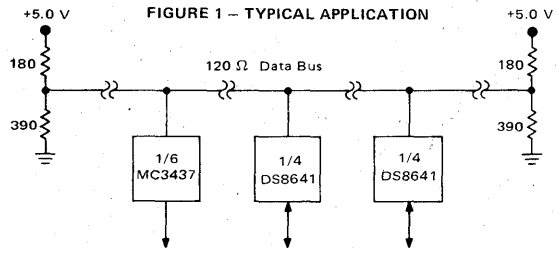
FIGURE 1 – TYPICAL APPLICATION



TRUTH TABLES

RECEIVER SECTION

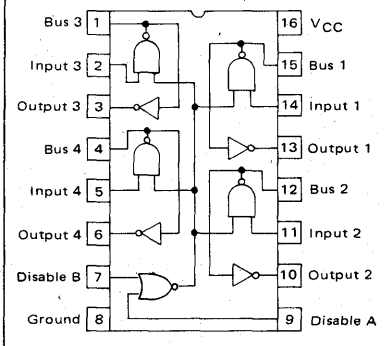
Bus	Output
$V_{IH(R)} > 1.7$ V	L
$V_{IL(R)} < 1.3$ V	H

Where: L = Low Logic State
H = High Logic State

DRIVER SECTION

Disable 1	Disable 2	Input	Bus
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	H

PIN CONNECTIONS



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	7.0	Vdc
Input and Output Voltage		V_O, V_I	5.5	Vdc
Junction Temperature	Plastic Ceramic	T_J	150 175	°C
Operating Ambient Temperature Range		T_A	0 to +70	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

ORDERING INFORMATION

Device	Temperature Range	Package
DS8641N	0 to +70°C	Plastic DIP
DS8641J	0 to +70°C	Ceramic DIP

This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for $0 \leq T_A \leq 70^oC$ and $4.75 \leq V_{CC} \leq 5.25$ V.)

Characteristic	Symbol	Min	Typ	Max	Unit
Disable Input Voltage – High Logic State	$V_{IH(DA)}$	2.0	–	–	V
Disable Input Voltage – Low Logic State	$V_{IL(DA)}$	–	–	0.8	V
Driver Input Voltage – High Logic State	$V_{IH(D)}$	2.0	–	–	V
Driver Input Voltage – Low Logic State	$V_{IL(D)}$	–	–	0.8	V
Receiver Input Threshold Voltage – High Logic State ($V_{IL(D)}$ = 0.8 V, $I_{OL(R)}$ = 16 mA, $V_{OL(R)} \leq$ 0.4 V)	$V_{ILH(R)}$	1.70	1.50	–	V
Receiver Input Threshold Voltage – Low Logic State ($V_{IL(D)}$ = 0.8 V, $I_{OH(R)}$ = –400 μA, $V_{OH(R)} \geq$ 2.4 V)	$V_{IHL(R)}$	–	1.50	1.30	V
Disable Input Current – High Logic State ($V_{IH(D)}$ = 2.4 V; $V_{IH(DA)}$ = 2.4 V) ($V_{IH(D)}$ = 5.5 V, $V_{IH(DA)}$ = 5.5 V)	$I_{IH(DA)}$	– –	– –	40 1.0	μA mA
Driver Input Current – High Logic State ($V_{IH(DA)}$ = 2.4 V; $V_{IH(D)}$ = 2.4 V) ($V_{IH(DA)}$ = 5.5 V, $V_{IH(D)}$ = 5.5 V)	$I_{IH(D)}$	– –	– –	40 1.0	μA mA
Disable Input Current – Low Logic State ($V_{IL(DA)}$ = 0.4 V, $V_{IL(D)}$ = 0.4 V)	$I_{IL(DA)}$	–	–	–1.6	mA
Driver Input Current – Low Logic State ($V_{IL(D)}$ = 0.4 V, $V_{IL(DA)}$ = 0.4 V)	$I_{IL(D)}$	–	–	–1.6	mA
Bus Current ($V_{IL(DA)}$ = 0.8 V, $V_{IL(D)}$ = 0.8, $V_{IH(BUS)}$ = 4.0 V) (V_{CC} = 5.25 V) (V_{CC} = 0 V)	I_{BUS}	 – –	 20 2.0	 100 100	μA
Bus Voltage – Low Logic State ($V_{IL(DA)}$ = 0.8 V, $V_{IH(D)}$ = 2.0 V, I_{BUS} = 50 mA)	$V_{L(BUS)}$	–	0.4	0.7	V
Receiver Output Voltage – High Logic State ($V_{IL(DA)}$ = 0.8 V, $V_{IL(D)}$ = 0.8 V, $V_{IL(BUS)}$ = 0.5 V, $I_{OH(R)}$ = –400 μA)	$V_{OH(R)}$	2.4	–	–	V
Receiver Output Voltage – Low Logic State ($V_{IL(DA)}$ = 0.8 V, $V_{IL(D)}$ = 0.8 V, $V_{IH(BUS)}$ = 4.0 V, $I_{OL(R)}$ = 16 mA)	$V_{OL(R)}$	–	0.25	0.4	V
Receiver Output Short Circuit Current ($V_{IL(DA)}$ = 0.8 V, $V_{IL(D)}$ = 0.8 V, $V_{IL(BUS)}$ = 0.5 V, V_{CC} = 5.25 V)	$I_{OS(R)}$	–18	–	–55	mA
Power Supply Current ($V_{IL(DA)}$ = 0 V, $V_{IH(D)}$ = 2.0 V)	I_{CC}	–	50	70	mA
Input Clamp Diode Voltage ($I_{I(DA)}$ = $I_{I(D)}$ = I_{BUS} = –12 mA)	V_I	–	–1.0	–1.5	V

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Disable Input to High Logic Level Output	$t_{PLH(DA)}$	–	19	30	ns
Propagation Delay Time from Disable Input to Low Logic Level Output	$t_{PHL(DA)}$	–	15	23	ns
Propagation Delay Time from Driver Input to High Logic Level Output	$t_{PLH(D)}$	–	17	25	ns
Progpgation Delay Time from Drive Input to Low Logic Level Output	$t_{PHL(D)}$	–	9.0	15	ns
Propagation Delay Time from Bus Input to High Logic Level Output	$t_{PLH(R)}$	–	20	30	ns
Propagation Delay Time from Bus Input to Low Logic Level Output	$t_{PHL(R)}$	–	18	30	ns

FIGURE 2 – DRIVER AND DISABLE TEST CIRCUIT AND WAVEFORMS

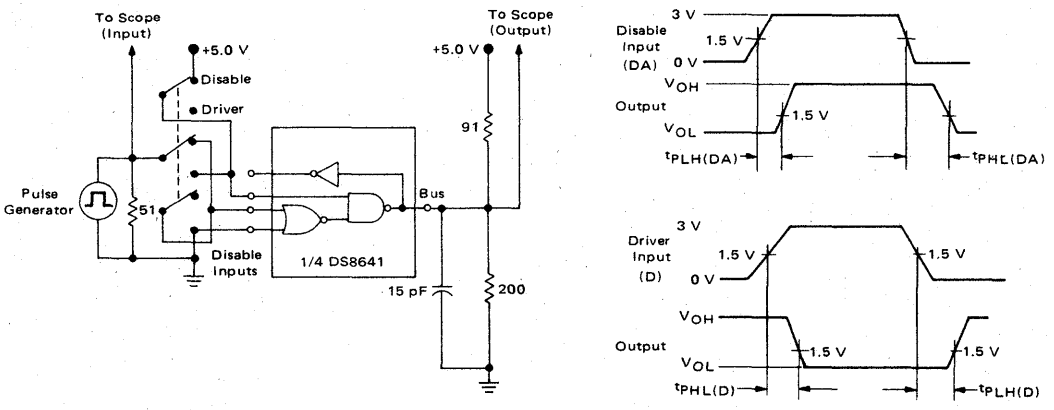
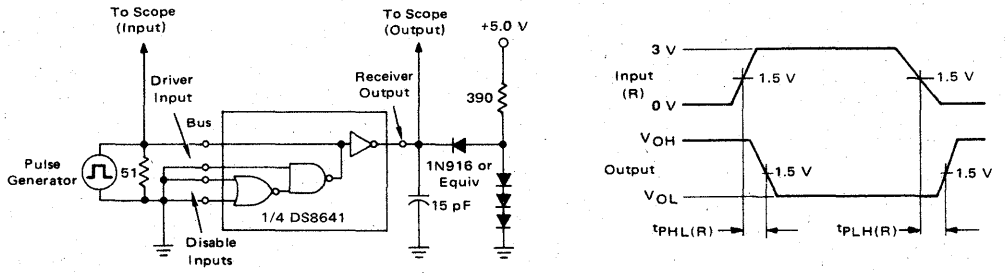
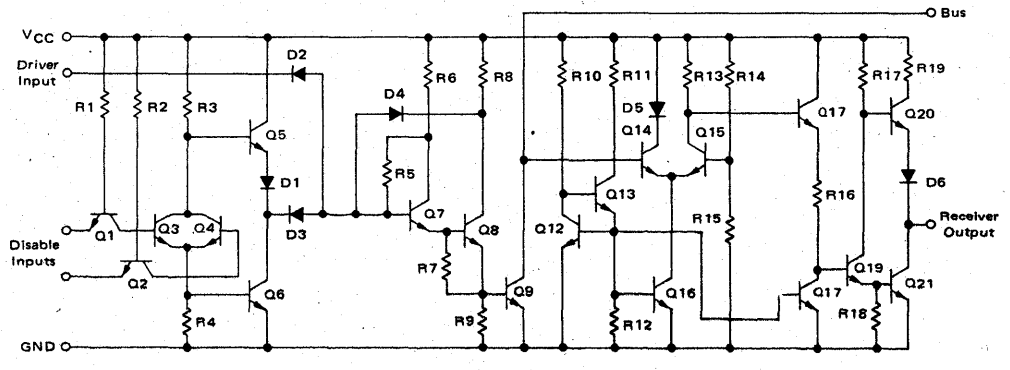


FIGURE 3 – RECEIVER TEST CIRCUIT AND WAVEFORM



REPRESENTATIVE CIRCUIT SCHEMATIC
(1/4 Shown)



ORDERING INFORMATION

Device	Temperature Range	Package
MC1405L	0°C to +70°C	Ceramic DIP
MC1505L	−55°C to +125°C	Ceramic DIP

MC1405L
MC1505L

DUAL RAMP A/D CONVERTER SUBSYSTEM

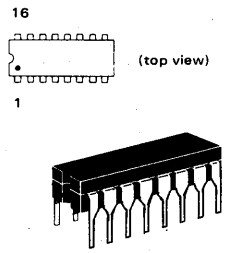
The MC1505/MC1405 is intended to perform the dual ramp function for either a 3-1/2 or 4-1/2 digit DVM or use as a general-purpose analog-to-digital (A/D) converter. It can be combined with the McMOS MC14435 logic system to produce the complete 3-1/2 digit DVM function.

The MC1505 uses the proven dual ramp A/D conversion technique. The subsystem consists of an on-chip voltage reference, a pair of voltage/current converters, an integrator, a comparator, a current switch and associated control and calibration circuitry. Only one capacitor and two calibration potentiometers are required for normal operation.

- Accuracies to 13 Bits
- Low Power Consumption: 42 mW @ +5.0 V
- Single Power Supply Operation – +5.0 V to +15 V
- Low Power Supply and Temperature Sensitivity
- Digital Inputs and Outputs Compatible with Both MTTL and McMOS
- Accepts Either Positive or Negative Input Voltages
- Combines with MC14435 to Produce 3-1/2 Digit A/D Converter

ANALOG-TO-DIGITAL CONVERTER SUBSYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT



CASE 620
CERAMIC PACKAGE

FIGURE 1 – COMPLETE A/D CONVERTER SYSTEM

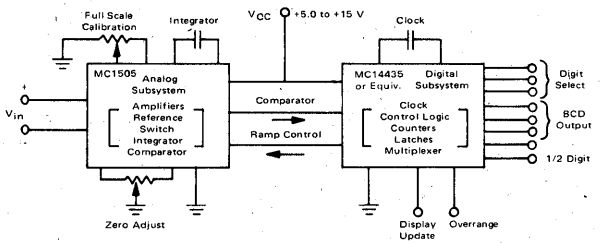
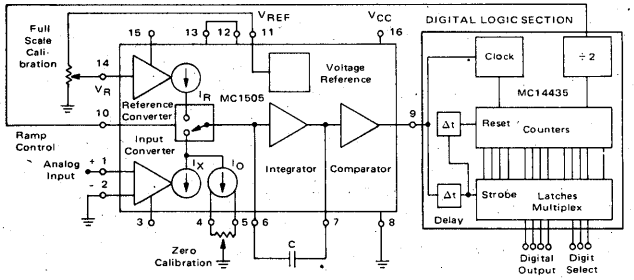


FIGURE 2 – PIN CONNECTIONS AND FUNCTIONAL DIAGRAM (as used in Figure 1)



TYPICAL APPLICATIONS

BCD A/D Converter: 2-1/2 to 4-1/2 Digits (LSI or MSI Logic)
- Panel Meters
- Digital Voltmeters
- Portable Instruments
- Industrial Measurement and Control

Binary A/D Converter: 8-to-13 Bits (LSI or MSI Logic)
- Industrial Measurement and Control
- High Noise Environments (Integrating Converter with MTTL, MHTL, and McMOS Compatibility)

Other Uses:
- Data Acquisition Systems with Remote MC1505
- Voltage to Frequency Conversion
- Delta Modulation and Signal Generation

MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+16.5	Vdc
Digital Input Voltage	V_{10}	+16.5	Volts
Reference Input Voltage	V_R	2.0	Volts
Unknown Input Voltage Range	V1 V2	±5.0 ±5.0	Volts
Zero Calibration Control Pin Voltage	V4	5.0	Volts
Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T_A = +25°C	P_D	1000 6.0	mW mW/°C
Operating Ambient Temperature Range MC1505L MC1405L	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_R = 1.000 Vdc, V1 = 2.000 Vdc, V2 = 0.000 Vdc, V10 ⩾ 2.0 Vdc, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Figure	MC1505 Min	MC1505 Typ	MC1505 Max	MC1405 Min	MC1405 Typ	MC1405 Max	Unit
A/D CONVERSION SYSTEM (1)									
Linearity: Deviation from Straight Line through Zero and Full Scale (2)	E_r	9, 11	–	±0.01	±0.05	–	±0.01	±0.05	%F.S.
Mid-Scale Power Supply Sensitivity (PSS of I_R-(I_X + I_O), V1 = 1.0 V)	PSSF	3	–	0.002	±0.02	–	0.002	±0.02	%/%
Zero Calibration Power Supply Sensitivity (V1 = V2 = 0 V)	PSSZ	9	–	0.001	–	–	0.001	–	%F.S./%
Input Common Mode Sensitivity (V_X = 2.0 V, V_{CM} = V2 is varied)	$\|CMSI_X\|$	3	–	0.0006	0.0012	–	0.0006	0.0018	%/mV
Full Scale Temperature Drift	$\|TCF\|$	9	–	0.001	–	–	0.001	–	%/°C
Zero Calibration Temperature Drift	$\|TCZ\|$	9	–	0.0005	–	–	0.0005	–	%F.S./°C
VOLTAGE REFERENCE									
Reference Voltage, Pin 11	V_{REF}	3	1.15	1.25	1.35	1.1	1.25	1.4	Vdc
Reference Voltage Power Supply Sensitivity	$PSSV_{REF}$	3	–	0.003	±0.01	–	0.003	±0.02	%/%
Reference Voltage Temperature Drift	$\|TCV_{REF}\|$	3	–	0.005	–	–	0.005	–	%/°C
REFERENCE CURRENT CONVERTER									
Reference Current	I_R	3	–	250	–	–	250	–	μA
Input Bias Current	I14	3	–	10	40	–	10	40	nA
Input Range of V_R	V14	3	0.8	–	1.2	0.8	–	1.2	Vdc
Input Offset Voltage (V14-V15)	$\|V_{RR}\|$	3	–	1.0	2.5	–	2.0	5.5	mV
INPUT CURRENT CONVERTER									
Unknown Current	I_X	3	–	500	–	–	500	–	μA
Input Resistance	R_I	3	–	4.0	–	–	4.0	–	kΩ
Input Differential Range	V_X	3,10	0	2.0	–	0	2.0	–	Volts
Input Common Mode Range	CMR	3,10,12	-1.5	–	+1.5	-1.5	–	+1.5	Volts
Input Bias Currents	11 12	3,9	– –	200 -300	– –	– –	200 -300	– –	μA
Input Offset Voltage (V13-V3)	$\|V_{XX}\|$	3	–	1.0	2.5	–	2.0	5.5	mV
RAMP OFFSET SOURCE									
Ramp Offset Current	I_O	4	–	25	–	–	25	–	μA

(1) System parameters measured using external voltage reference, independent of V11 = V_{REF}.
Integrator Capacitor = 2.0 μF
Clock Frequency = 30 kHz
V_{CC} = 15 V

(2) Does not include quanitizing error. See Figure 11 for calibration.

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ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_R = 1.000 Vdc, V1 = 2.000 Vdc, V2 = 0.000 Vdc, V10 ⩾ 2.0 Vdc, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Figure	MC1505 Min	MC1505 Typ	MC1505 Max	MC1405 Min	MC1405 Typ	MC1405 Max	Unit
CURRENT SWITCH									
Digital Input Logic Levels, Pin 10									
High Level, Logic "1"	V_{IH}	3,18	2.0	–	–	2.0	–	–	Vdc
Low Level, Logic "0"	V_{IL}	3,18	–	–	0.8	–	–	0.8	Vdc
Digital Input Current									
High Level, Logic "1"	I_{IH}	3	–	0	1.0	–	0	1.0	μA
Low Level, Logic "0"	I_{IL}	3	–	-5.0	-50	–	-5.0	-50	μA
INTEGRATOR									
Input Bias Current	I6	5	–	10	30	–	10	50	nA
Output Voltage Swing	V7	–							Volts
High			12.8	13.0	–	12.8	13.0	–	
Low			–	0.2	0.35	–	0.2	0.35	
COMPARATOR									
Output Logic Levels, Pin 9									Volts
High Level, Logic "1" $T_A = T_{low}$ to T_{high}	V_{OH}	3	13.5	14.0	–	13.5	14.0	–	
Low Leve, Logic "0" (Sink Current = 1.6 mA)	V_{OL}	3	–	0.35	0.5	–	0.35	0.5	
Input Threshold	$V_{TH(7)}$	–	0.9	1.0	1.1	0.9	1.0	1.1	Volts
POWER SUPPLY									
Power Supply Current	I_{CC}								mA
(V_{CC} = +5.0 Vdc)		3	–	8.4	12.0	–	8.4	12.0	
(V_{CC} = +15.0 Vdc)		3	–	9.0	13.0	–	9.0	13.0	
Power Supply Voltage Range	V_{CC}	–	4.75	–	16.5	4.75	–	16.5	Vdc
Power Dissipation	P_D								mW
(V_{CC} = +5.0 Vdc)		–	–	42	60	–	42	60	
(V_{CC} = +15.0 Vdc)		–	–	135	195	–	135	195	

T_{low} = -55°C for MC1505L, 0°C for MC1405L
T_{high} = +125°C for MC1505L, +70°C for MC1405L

FIGURE 3 – STANDARD TEST CONFIGURATION

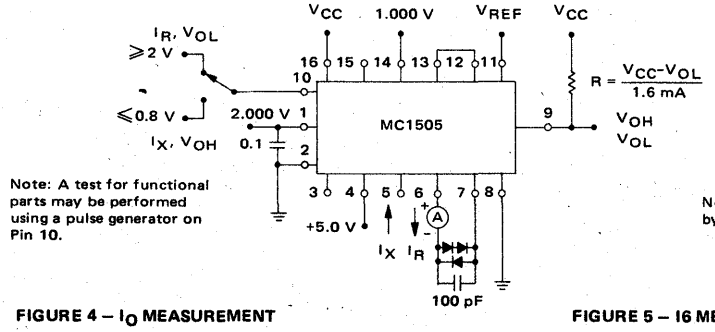


FIGURE 4 – I_O MEASUREMENT

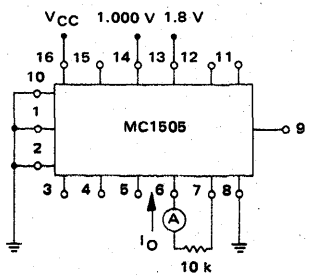
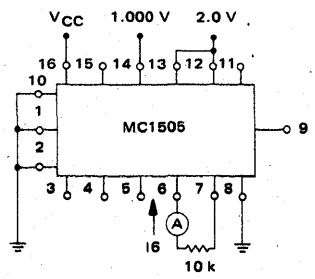


FIGURE 5 – I6 MEASUREMENT



GENERAL INFORMATION

Dual Ramp Analog-to-Digital Conversion

The dual ramp method of A/D conversion is a proven system which is capable of very high accuracy. The conversion is an integrating process which offers high noise rejection and immunity to changes in the clock rate and integrator capacitor value. The particular method used in the MC1505 is a noniterating dual slope technique which produces an accurate result after one conversion period.

Dual ramp conversion is accomplished with the system of Figure 2. The conversion begins at time t1, when current I_X causes the integrator output, or ramp, to cross the comparator threshold, as shown in Figure 6. The clock is activated and the counters begin counting from zero. The system counts for a fixed period T, with a ramp slope which depends on the input voltage, i.e., a steep slope is caused by a high input voltage. When the counters have reached full scale, the overflow count triggers a ÷ 2 flip-flop which changes the ramp control polarity current. I_R now controls the integrator and the down ramp begins at t2. This ramp continues at a fixed slope for a time period which depends on the amplitude achieved by the up ramp. Thus T2 is determined by the input voltage. When the ramp crosses the comparator threshold at t3, the clock stops and the counter holds a digital value which is proportional to the unknown input voltage.

After the down ramp crosses the comparator threshold, a timing sequence in the digital section strobes the latches to store the data, resets the counters, and reverses the ramp at t4 to begin a new conversion.

Since the voltage change across the capacitor is equal on the up and down ramps, an equal amount of charge is exchanged. The equations of Figure 6 show that the system output is the ratio of the unknown and reference currents, and long term changes in the clock rate and integrator capacitor do not effect the reading.

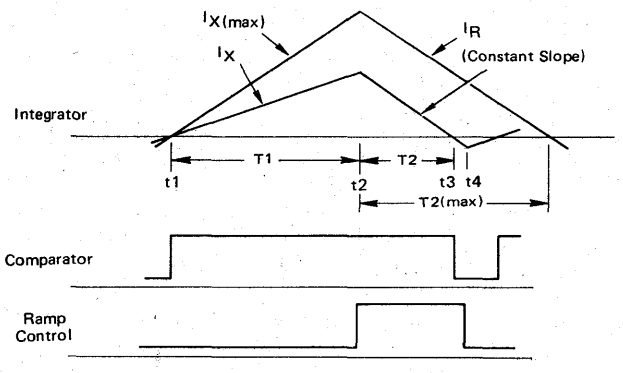
A/D Subsystem Circuit Description

The MC1505 incorporates special circuit features which allow all the analog functions of the dual ramp system to be performed on a single monolithic chip using standard bipolar processing.

Voltage-to-current conversion for both the input and reference voltages allows the use of a high-speed current switch and single supply operation. The unbuffered differential inputs have sufficiently high input impedance for power supply monitoring applications, and provide flexibility for other input formats since they will accept either positive or negative voltages.

The voltage reference, shown in Figure 7, is one of the six basic circuits in the subsystem. It provides a low impedance output which has excellent temperature stability, and high power supply rejection. Biasing for the other circuits in the MC1505 is derived from the voltage reference circuitry.

FIGURE 6 – DUAL RAMP A/D CONVERSION WAVEFORMS



ΔV on capacitor is equal in T1 and T2

$$\frac{1}{C}\int_{t1}^{t2} I_X\,dt = \frac{1}{C}\int_{t2}^{t3} I_R\,dt$$

Where I_X is opposite I_R polarity.

$$I_X\,T1 = I_R\,T2$$

Since I_X and I_R are proprotional to V_X and V_R,

$$V_X\,T1 = V_R\,T2$$

$$\boxed{T2 = T1\frac{V_X}{V_R}}$$

T2 corresponds to the number of counts in the output digital word.

T1 and T2 are derived from the clock, so their ratio is independent of clock frequency.

The same basic amplifier circuit is used in both the reference and input voltage-to-current converters. It is an extremely well balanced amplifier with low input offset voltage temperature drift. The reference converter uses a pair of PNP transistors to derive current I_R, in conjunction with a reference resistor which has the same temperature coefficient as those used in the input converter. The value of the reference current is $V_R/R5$. The collectors of transistors Q1, Q2 and Q3 in Figure 7 all track with a two diode temperature coefficient, which assures constant current ratios.

The reference resistor value can vary by 30% of 4.0 kΩ due to process variations. Moreover, these variations will also affect the input bridge resistors. Thus, the ratio of reference to unknown current has a close tolerance for a wide range of resistor values.

The input voltage-to-current converter is a bridge or bilateral current source whose output current is $V_X/R1$. If the bridge is perfectly balanced, its output impedance and common mode rejection are infinite. However, the design has the ability to tolerate bridge mismatches of approximately 0.5%. In order to tolerate this mismatch, the output of the bridge current source is connected to the current switch which is a low temperature coefficient, low impedance source of 1.25 volts. This technique effectively eliminates output current changes due to finite output impedance which is caused by resistor mismatch. This input current converter makes possible the use of a single supply voltage and differential inputs which can be used at or below ground potential.

An important feature of the MC1505 is the ramp offset current source which is added to the unknown current and does not allow the ramp to reach zero slope when the input voltage is zero. The ramp range is shown in Figure 8. The ramp offset current has a value of $I_R/10$, so that the minimum ramp slope is 5% of the full scale slope. This allows reliable conversion at low input voltages by assuring a nearly constant comparator propagation delay and a good ramp signal-to-noise ratio. It also prevents turn-off of the diode in the current switch at low levels, restricting the voltage change at the output of the resistor bridge. Still another feature is that it provides a convenient temperature compensated zero adjust which can correct errors in the resistor bridge and input buffer amplifiers when they are used. The ramp offset current is compensated by 100 extra counts in the digital logic during ramp down, so it does not appear in the digital output (see Figure 8).

The current switch uses current steering for very high speed operation. A smooth transition occurs as one current is turned on while the other is turned off. This minimizes error during the ramp reversal at its peak, especially since the reference current source has a very high output impedance and does not change value when switched. The settling time of the input current converter is not a factor in system accuracy. At the ramp peak, I_X is turned off, so the amplifier settles after the unknown current is decoupled from the integrator. When the ramp is below the comparator threshold, the unknown current is switched on and thus the current can settle before the ramp enters the active conversion range. The switch operates into a voltage of 1.95 volts and is translated by a follower so its input

5

FIGURE 7 – A/D CONVERTER ANALOG SUBSYSTEM

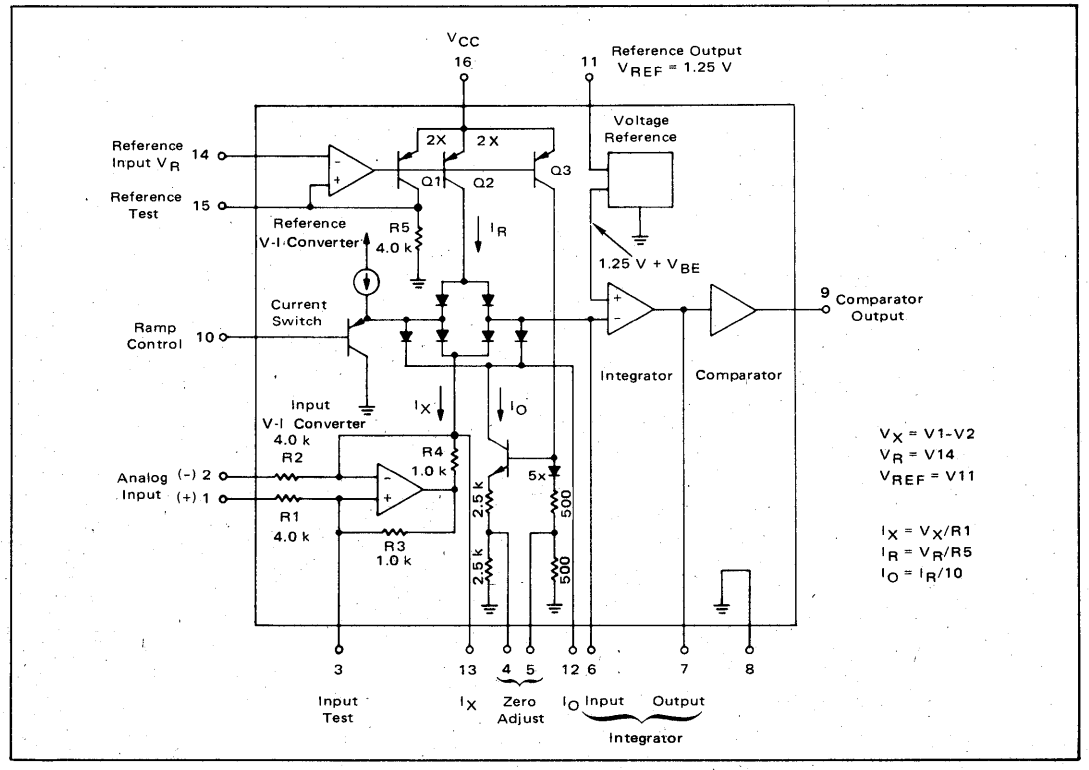
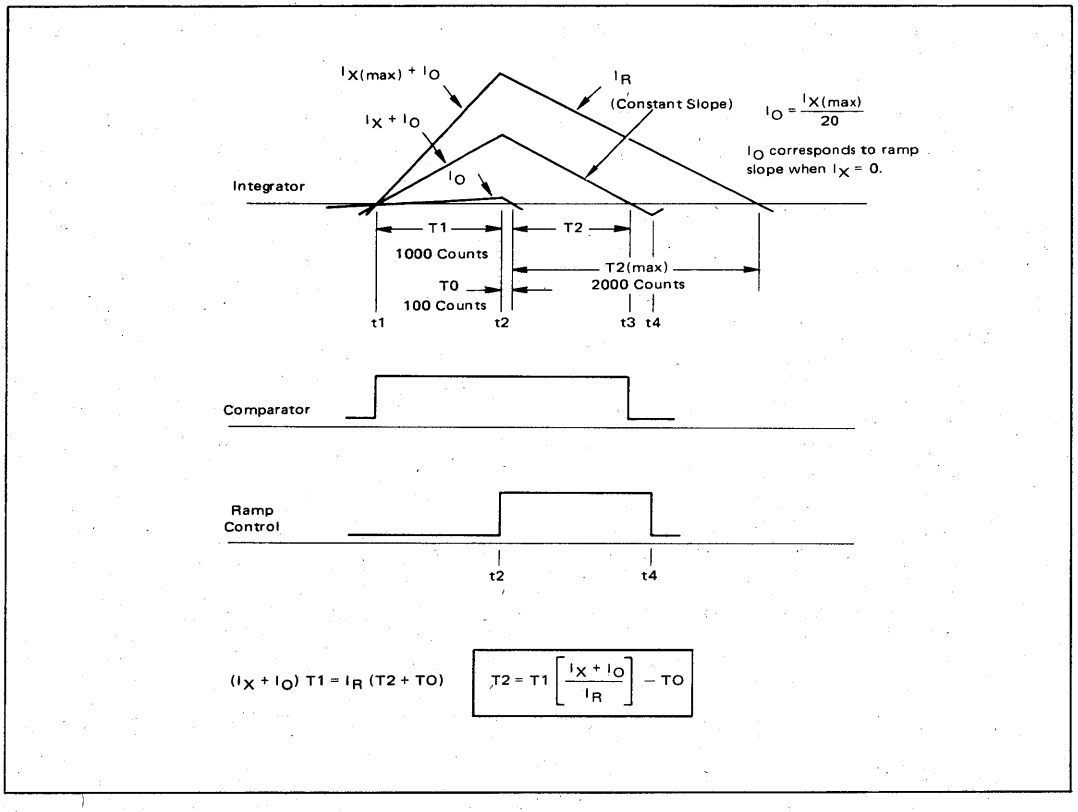


FIGURE 8 – MC1505 SYSTEM TIMING DIAGRAM
(2.0 Volt Full Scale Input)



threshold is 1.25 volts.

The integrator is a single stage, wide bandwidth amplifier. Its low propagation delay and low output impedance minimize ramp spikes due to output current reversal during ramp turn-around. The input bias current is typically one part in 50,000 of the full scale current, so that its temperature change contributes negligible error. Gain and input offset voltage are not critical since the integrator is driven from current sources.

The comparator is designed for low hysteresis by maintaining a constant power dissipation regardless of output state. This hysteresis is typically 0.1 mV and remains constant with temperature variations, so that no measurable system error is contributed. Temperature variations in the value of the comparator threshold are not an error factor, since the only requirement is that the threshold remain constant during a given conversion cycle. Voltage gain of the comparator is 2,000,000 when driving CMOS, and 40,000 with one TTL load. The comparator output is slew rate controlled to provide output rise and fall times of approximately 80 ns. This minimizes noise generation which could affect system stability.

The system is zeroed and full scale calibrated by potentiometers which provide temperature compensation. All the other resistors are diffused in close proximity, yielding reference and unknown currents which have a closely tracking resistive temperature coefficient.

APPLICATIONS INFORMATION

The input configurations for the MC1505 are shown in Figure 10. Note that the differential input voltage must always remain the same polarity with Pin 1 positive with respect to Pin 2. Figures 10 and 12 will aid in the understanding of the input circuitry.

The input common mode rejection of the MC1505 is high enough to maintain rated accuracy with small changes in common mode voltage, such as would be seen with ground errors and noise. The system must be recalibrated, however, for larger changes in common mode input voltage.

The MC1505 is arranged so that $I_X = I_R$ when $V_X = V_R$, or so that the ramp slopes are equal for input and reference voltages of 1 volt. As shown in Figure 8, a system with a 2 volt full-scale input requires twice as many digital counts during T2 as for T1. A system with a 1 volt full scale would require an equal number of counts in T1 and T2. Figure 9 illustrates a 3-1/2 digit system, but typical accuracies of the MC1505 allow its use in 4 digit applications. It can also be used in systems which require 4-1/2 digit resolution.

The ramp offset current and 100 count delay are shown in Figure 8. In certain applications, a different number of counts may be used. The system will not always operate properly, however, with a 10 count delay since the ramp offset current is used to zero the system and compensate for error in the input resistor bridge. This error, known as I_{XO}, is current which flows to or from the input converter with zero volts applied to the input. It is typically between ±5.0 μA, which is 1% of full scale in a 2 volt system. A 10 count delay would need a 0.5% ramp offset current, which would not always be able to cancel this error. Also, a 10 count delay does not provide enough signal-to-noise margin for consistently accurate low-level conversion.

The integrating capacitor is chosen with the equations shown in Figure 9. The maximum ramp voltage should be used for best signal-to-noise ratio, but temperature changes in I_X, I_R and the capacitor should be anticipated to prevent integrator saturation. Variations in clock frequency should also be considered. A non-polar capacitor with low dielectric absorption should be used for highest accuracy.

The lower half of the diode current switch is split with separate diodes for I_X and I_O. In most applications Pins 12 and 13 will be connected so that the two device emitters are effectively one, since the main purpose of these pins is for testing. Connecting these pins allows proper system zero adjustment and prevents turn-off of the switch diode with low unknown current levels. This yields better conversion accuracy.

FIGURE 9a – ACCURACY TEST
3-1/2 Digit Panel Meter

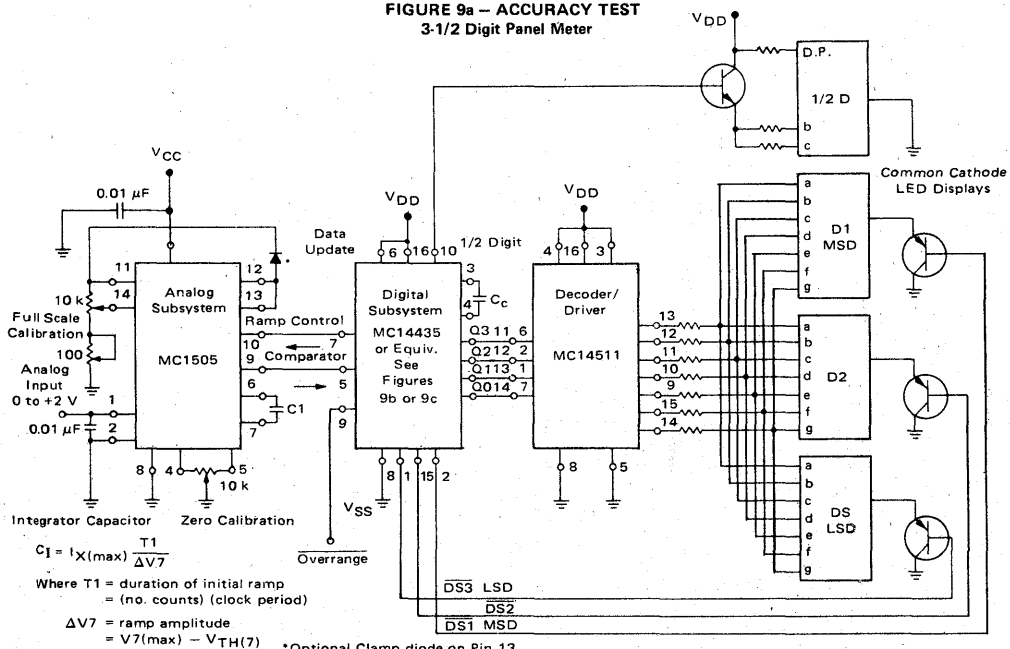
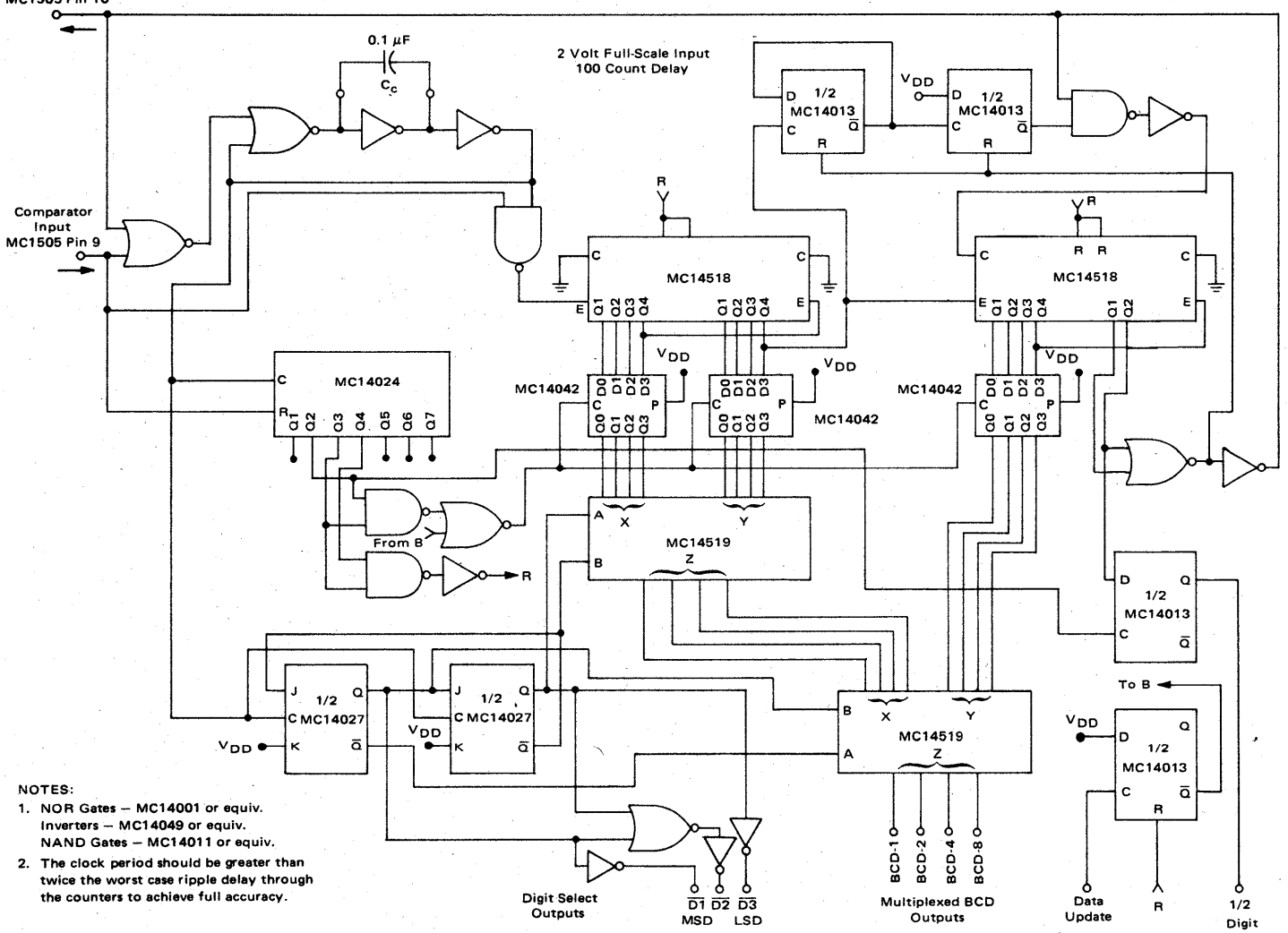


FIGURE 9b – McMOS DIGITAL SUBSYSTEM
3-1/2 Digit BCD A/D Converter



NOTES:
1. NOR Gates – MC14001 or equiv.
   Inverters – MC14049 or equiv.
   NAND Gates – MC14011 or equiv.
2. The clock period should be greater than twice the worst case ripple delay through the counters to achieve full accuracy.

FIGURE 9c – FUNCTIONAL DIAGRAM OF
MC14435 McMOS DIGITAL SUBSYSTEM

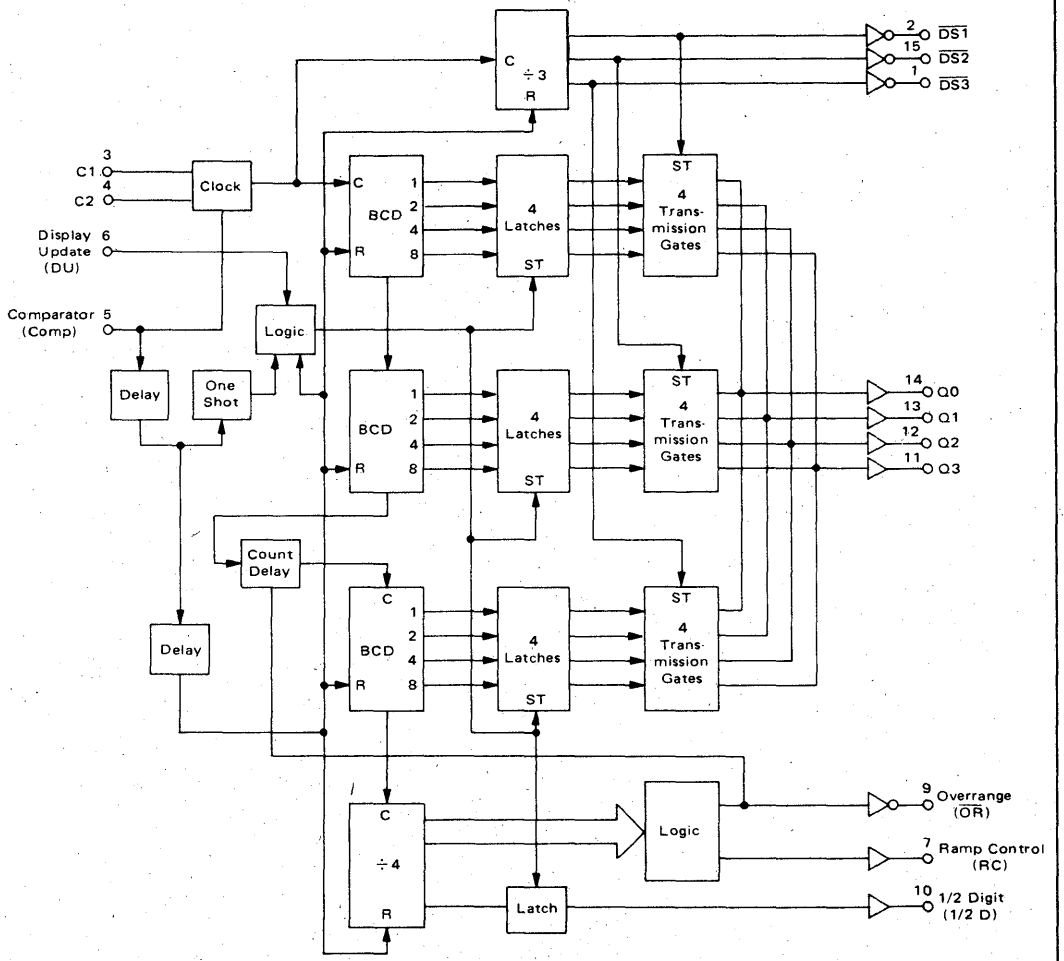


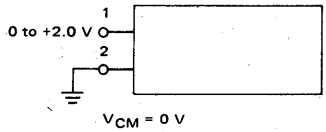
FIGURE 10 – ANALOG INPUT RANGE

The input circuit for the MC1505 has a unipolar differential input range of +2 volts and a bipolar common mode input range of ±1.5 volts.

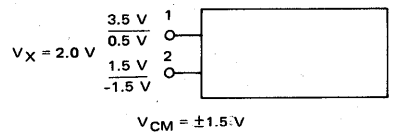
Positive Input:

$V_X = V1 - V2$ V_X Range 0 to +2.0 V

$V_{CM} = V2$ V_{CM} Range ±1.5 V



$V_{CM} = 0$ V

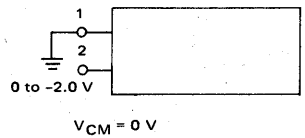


$V_{CM} = \pm 1.5$ V

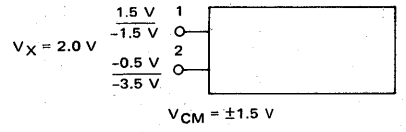
Negative Input:

$V_X = V1 - V2$ V_X Range 0 to +2.0 V

$V_{CM} = V1$ V_{CM} Range ±1.5 V



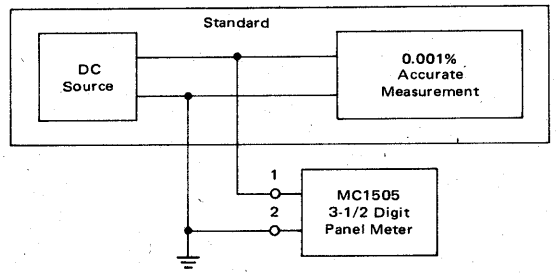
$V_{CM} = 0$ V



$V_{CM} = \pm 1.5$ V

Allowable Pin Voltages:
Pin 1: -1.5 V to +3.5 V
Pin 2: -3.5 V to +1.5 V

FIGURE 11 – CALIBRATION SET-UP



Zero Calibration:

Set standard at 0.0005 V.

Adjust zero potentiometer for panel meter display transition between 0.000 and 0.001 V. Note: An analog input of -1 mV yields a reading of 0.099.

Repeat zero and full scale calibration until meter is calibrated at both ends of the scale.

Full Scale Calibration:

Set standard at 1.9995 V.

Adjust full scale potentiometer for panel meter display transition between 1.999 and 1.000 V. (overrange)

Linearity Test:

Adjust standard for the desired panel meter transition and record the value of the standard.

5

TYPICAL PERFORMANCE CURVES

FIGURE 12 – MAXIMUM COMMON-MODE INPUT VOLTAGE versus TEMPERATURE

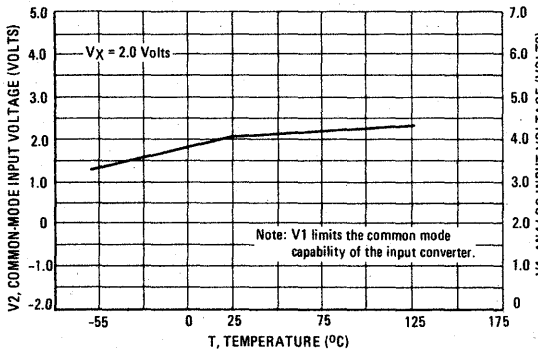


FIGURE 13 – INPUT CURRENT versus INPUT VOLTAGE

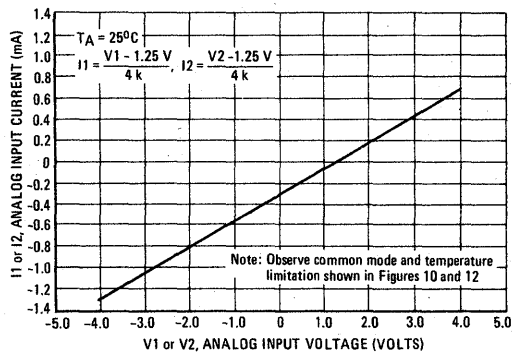


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FIGURE 14 – UNKNOWN CURRENT versus ANALOG INPUT VOLTAGE

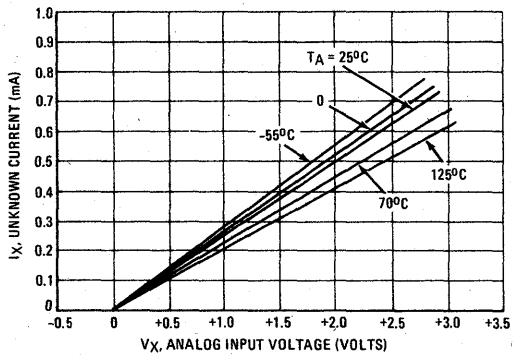


FIGURE 15 – REFERENCE CURRENT versus REFERENCE INPUT VOLTAGE

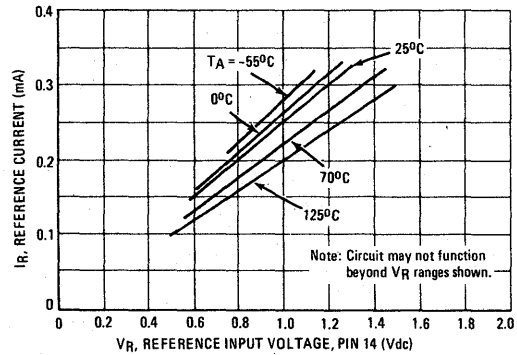


FIGURE 16 – TYPICAL POWER SUPPLY CURRENT versus POWER SUPPLY VOLTAGE

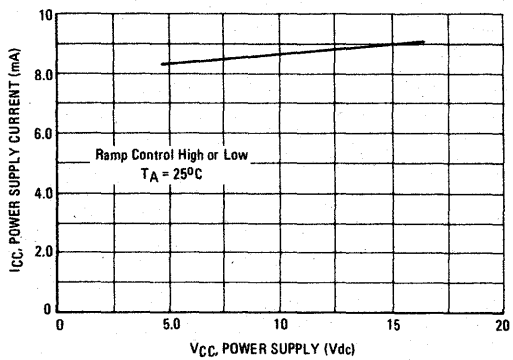


FIGURE 17 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE

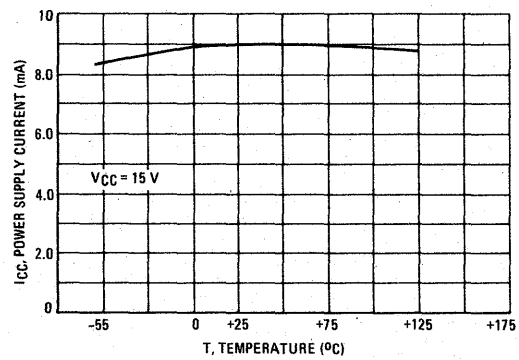


FIGURE 18 – CURRENT SWITCH TRANSFER CHARACTERISTIC

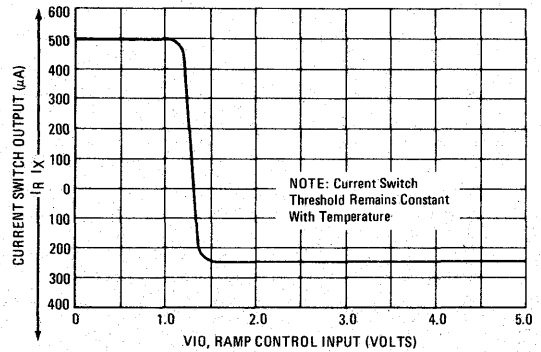


FIGURE 19 – INTEGRATOR OUTPUT SWING versus TEMPERATURE

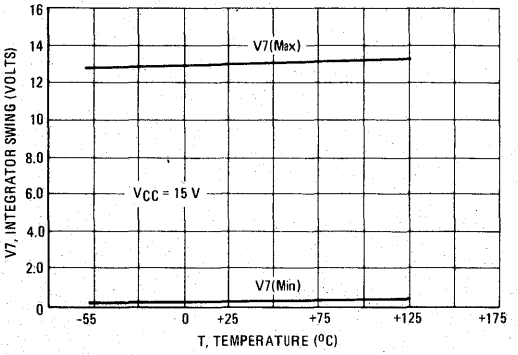


FIGURE 20 – COMPARATOR THRESHOLD versus TEMPERATURE

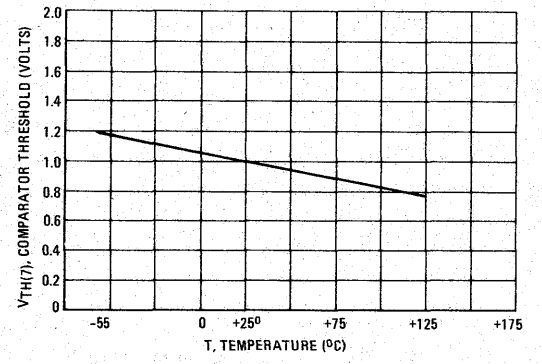


FIGURE 21 – RAMP CURRENT RATIO versus POWER SUPPLY

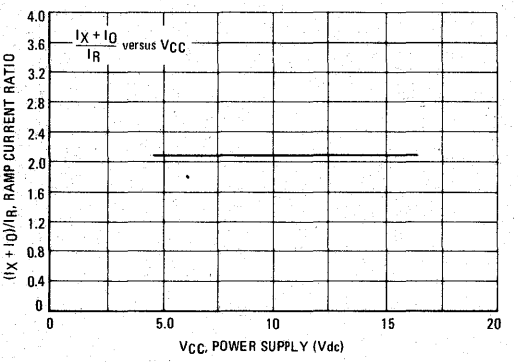
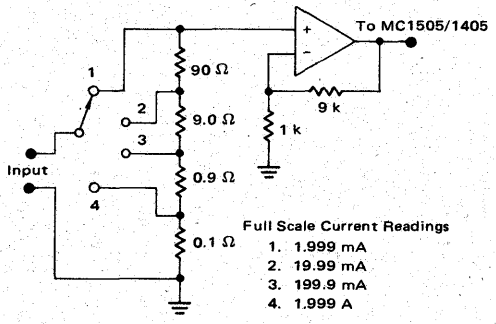


FIGURE 22 – CURRENT MEASUREMENT CIRCUITRY



If a voltage drop of 2.0 V full scale can be tolerated the resistors may be increased by a factor of ten and a unity gain buffer may be employed.

FIGURE 23 – DVM VOLTAGE RANGING

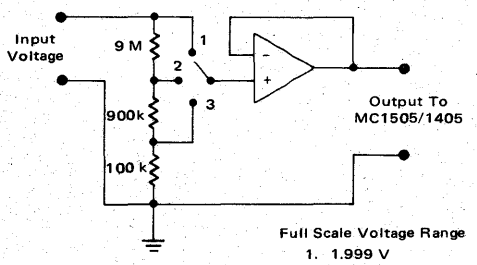
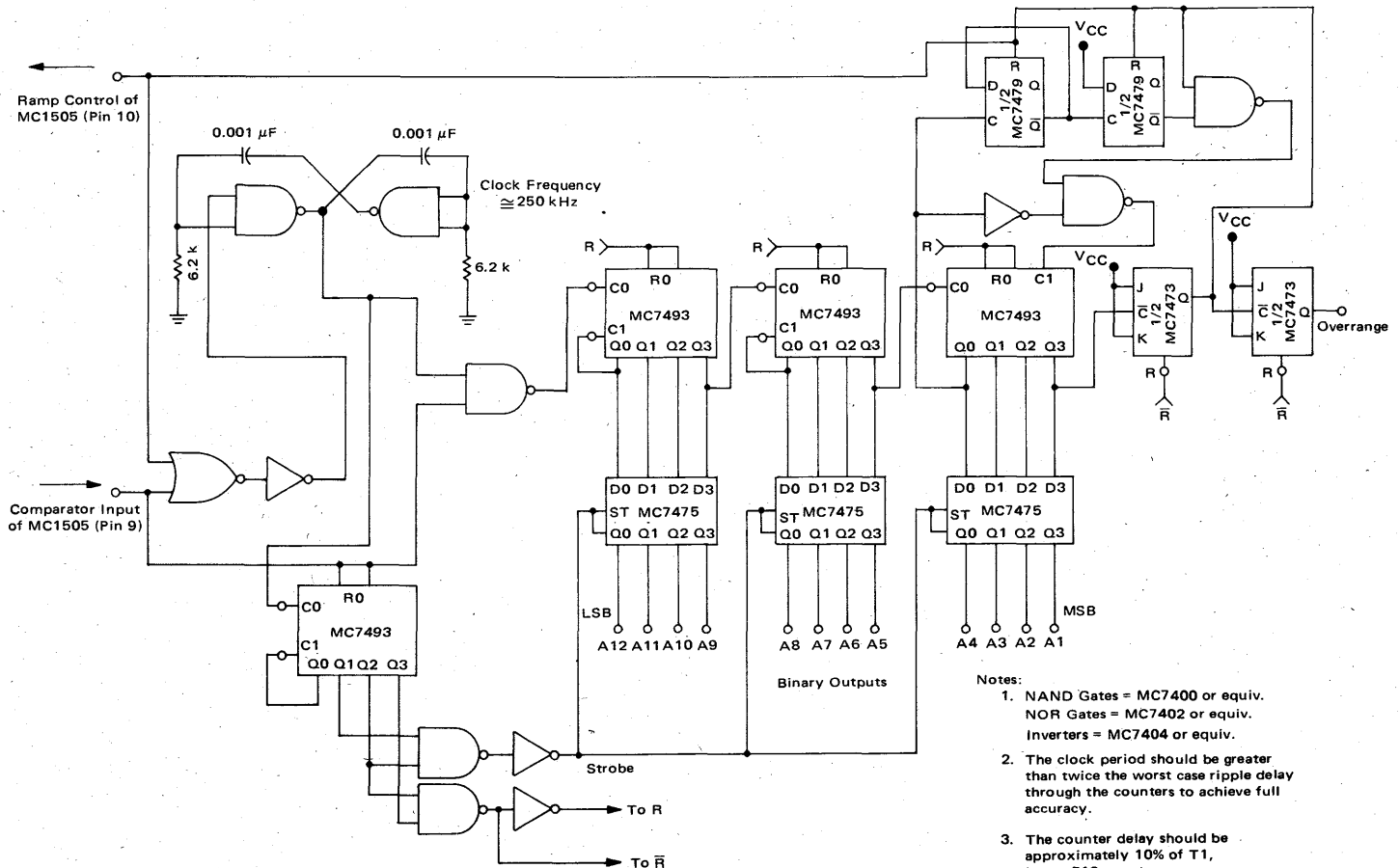


FIGURE 24 – MTTL DIGITAL SUBSYSTEM
12 Bit Binary A/D Converter
(1.0 Volt Full Scale, 512 Count Delay)



Notes:
1. NAND Gates = MC7400 or equiv.
   NOR Gates = MC7402 or equiv.
   Inverters = MC7404 or equiv.
2. The clock period should be greater than twice the worst case ripple delay through the counters to achieve full accuracy.
3. The counter delay should be approximately 10% of T1, hence 512 counts.

FIGURE 25 – 12-BIT BINARY A/D LOGIC SUBSYSTEM USING McMOS

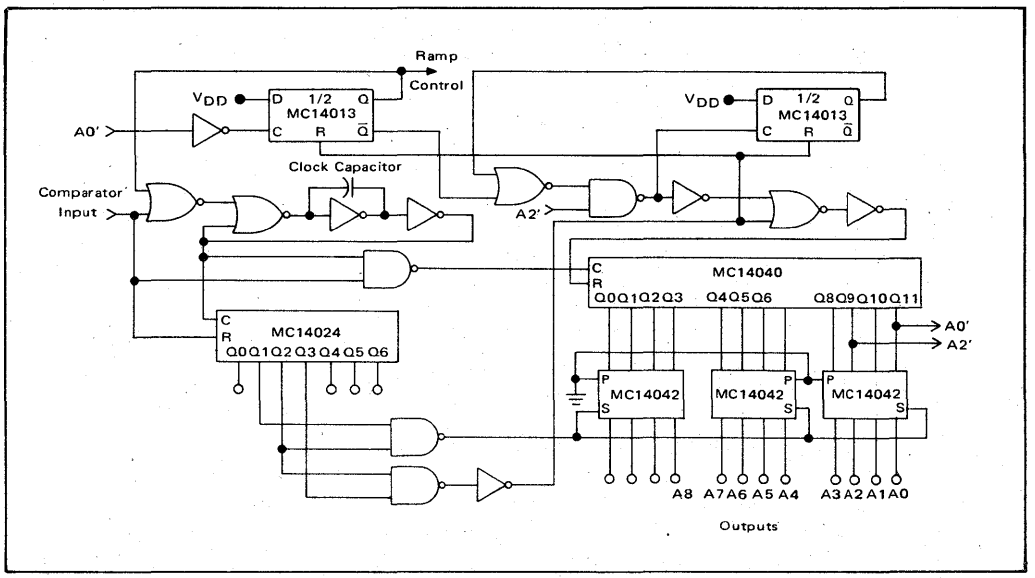
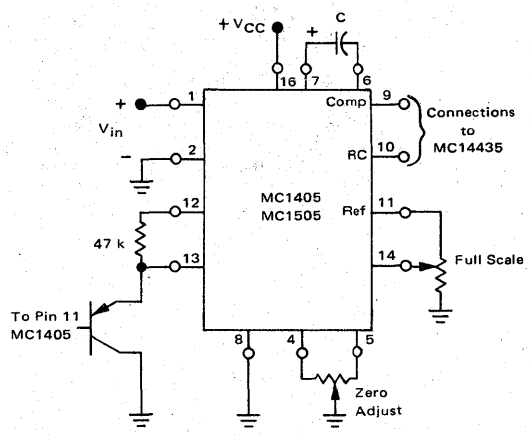


FIGURE 26 – CIRCUIT TO PREVENT POSSIBLE LATCHUP WITH APPLICATION OF NEGATIVE INPUT VOLTAGES

The MC1405/1505 A/D analog subsystem is intended for positive input voltages only (i.e., pin 1 positive with respect to pin 2). However, should pin 2 become more than 100 mV positive with respect to pin 1, the internal input amplifier may go into a latchup mode which will require that the system power be turned off and then reapplied to reset the system. To prevent this problem a PNP transistor can be used as shown in the accompanying figure. The base-emitter junction of the transistor clamps pin 13 at one diode drop above the reference voltage (pin 11) to prevent the latchup. The gain of the transistor insures that the reference need not sink more than 500 μA of current.

The 47 kΩ resistor is required only if the A/D system is to continue to convert under reverse polarity conditions such as for autopolarity schemes as shown in Engineering Bulletin EB-35.



*47 kΩ resistor required if conversions are to continue during input polarity reversal, otherwise tie pins 12 and 13 together.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1406L	0°C to +70°C	Ceramic DIP
MC1506L	−55°C to +125°C	Ceramic DIP

MC1406L
MC1506L

Specifications and Applications Information

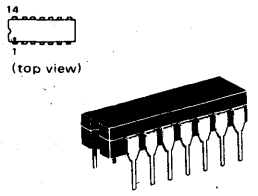
SIX BIT, MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

. . . designed for use where the output current is a linear product of a six-bit digital word and an analog input voltage.

- Digital Inputs are MDTL and MTTL Compatible
- Relative Accuracy — ±0.78% Error maximum
- Low Power Dissipation — 85 mW typical @ ±5.0 V
- Adjustable Output Current Scaling
- Fast Settling Time — 150 ns typical
- Standard Supply Voltage: +5.0 V and -5.0 V to -15 V

SIX BIT, MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 1 — OUTPUT CURRENT SETTLING TIME (ALL BITS SWITCHED, $R_L = 50\ \Omega$)

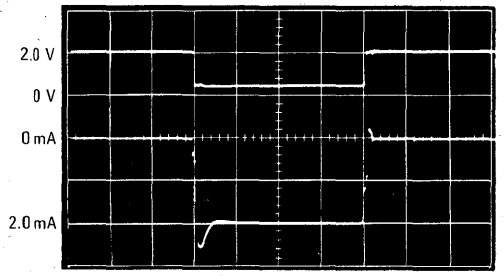
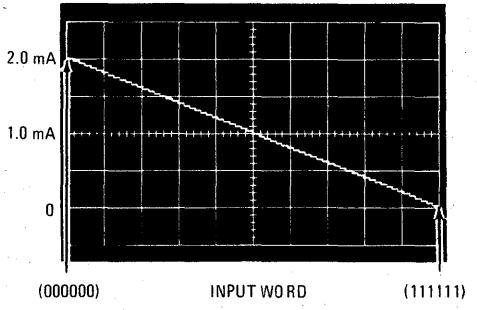


FIGURE 2 — D-to-A TRANSFER CHARACTERISTICS



TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- Digital-to-Analog Meter Readout
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- Digital Varicap Tuning
- Video Systems
- Stepping Motor Drive
- CRT Character Generation
- Digital Addition and Subtraction
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Programmable Power Supplies
- Speech Encoding

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+5.5 -16.5	Vdc
Digital Input Voltage	V_5 thru V_{10}	+8.0, V_{EE}	Vdc
Applied Output Voltage	V_O	±5.0	Vdc
Reference Current	I_{12}	5.0	mA
Reference Amplifier Inputs	V_{12}, V_{13}	V_{CC}, V_{EE}	Vdc
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C	P_D	 1000 6.7	 mW mW/°C
Operating Temperature Range MC1506L MC1406L	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = −15 Vdc, $\frac{V_{ref}}{R12}$ = 2.0 mA; all logic inputs in low logic state, $T_A = T_{high}$ to T_{low}, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O)	10	E_r	–	–	±0.78	%
Settling Time (within 1/2 LSB [includes t_d] T_A = +25°C)	9	t_S	–	150	300	ns
Propagation Delay Time T_A = +25°C	9	t_{PHL}, t_{PLH}	–	10	50	ns
Output Full Scale Current Drift		$\lvert TCI_O \rvert$	–	80	–	PPM/°C
Digital Input Logic Levels High Level, Logic "1" Low Level, Logic "0"	3,14	 V_{IH} V_{IL}	 2.4 –	 – –	 – 0.8	Vdc
Digital Input Current High Level, V_{IH} = 5.0 V Low Level, V_{IL} = 0.8 V	3,13	 I_{IH} I_{IL}	 – –	 0 -0.7	 +0.01 -1.5	mA
Reference Input Bias Current (Pin 13)	3	I_{13}	–	-0.002	-0.01	mA
Output Current Range V_{EE} = -5.0 V V_{EE} = -6.0 to -15 V	3	I_{OR}	 0 0	 2.0 2.0	 2.1 4.2	mA
Output Current V_{ref} = 2.000 V, R_{12} = 1.000 kΩ	3	I_O	 1.9	 1.97	 2.1	mA
Output Current (all bits high)	3	$I_{O(min)}$	 –	 0	 10	μA
Output Voltage Compliance ($E_r \leq \pm 0.78\%$ at T_A = +25°C)	3,4,5	V_{O+} V_{O-}	– –	+0.25 -0.45	+0.1 -0.3	Vdc
Reference Current Slew Rate (T_A = +25°C)	8,15	SR I_{ref}	 –	 2.0	 –	mA/μs
Output Current Power Supply Sensitivity	10	PSRR (−)	–	0.002	0.010	mA/V
Power Supply Current A1 thru A6; V_{IL} = 0.8 V A1 thru A6; V_{IH} = 2.4 V	3,11,12	 I_{CC} I_{EE}	 – –	 +7.2 -9.0	 +11 -11	mA
Power Dissipation (all bits high) V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc		P_D	 – –	 85 175	 120 240	mW

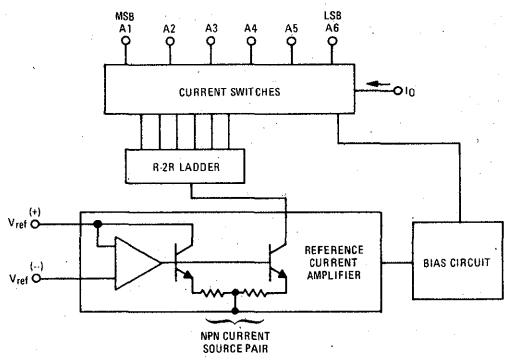
*T_{high} = +70°C for MC1406L T_{low} = 0°C for MC1406L
= +125°C for MC1506L = −55°C for MC1506L

The MC1506L consists of a reference current amplifier, and R-2R ladder, and six high-speed current switches. For many applications, only a reference resistor and a reference supply voltage need be added.

The switches are inverting in operation, therefore a low state at the input turns on the specified output current component. The switches use a current steering technique for high speed and a termination amplifier that consists of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching and provides a low impedance termination of equal voltage for all legs of the ladder.

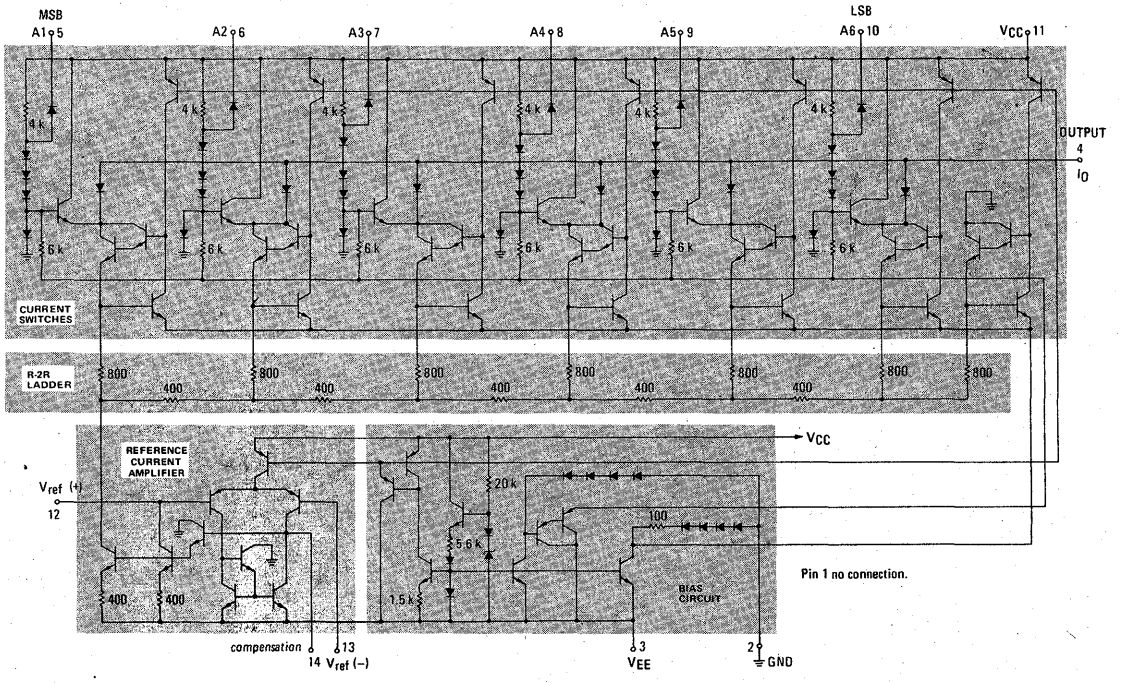
The R-2R ladder divides the reference amplifier current into binarily-related components which are fed to the switches. Note that there is always a remainder current that is equal to the least significant bit. This current is shunted to ground, and the maximum current is 63/64 of the reference amplifier current, or 1.969 mA for a 2.0 mA reference current if the NPN current source pair is perfectly matched.

BLOCK DIAGRAM



5

COMPLETE CIRCUIT SCHEMATIC
(Digital Inputs; pins 5,6,7,8,9,10)



TEST CIRCUITS AND TYPICAL CHARACTERISTICS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT

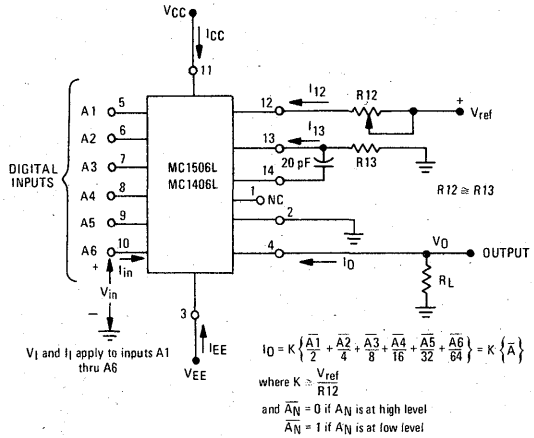


FIGURE 4 – OUTPUT CURRENT versus OUTPUT VOLTAGE

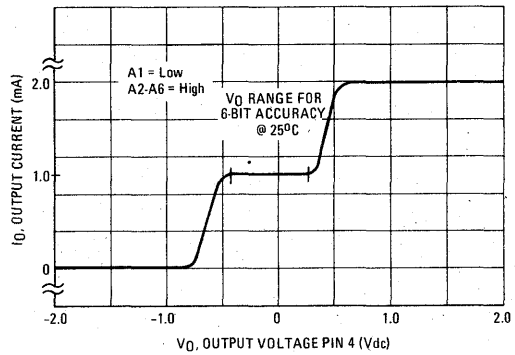


FIGURE 5 – MAXIMUM OUTPUT VOLTAGE versus TEMPERATURE

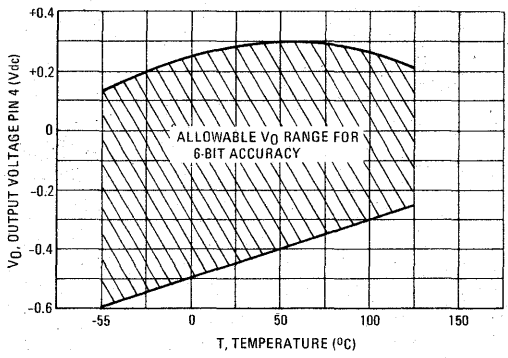


FIGURE 6 – POSITIVE V_{ref}

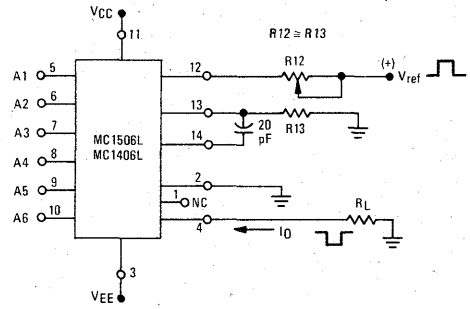


FIGURE 7 – NEGATIVE V_{ref}

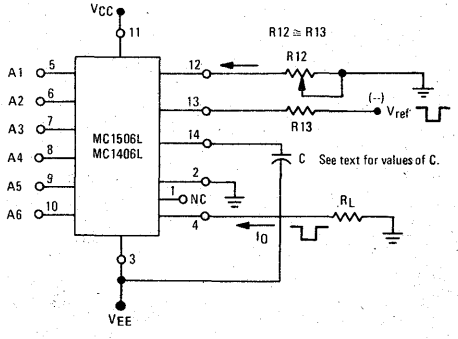
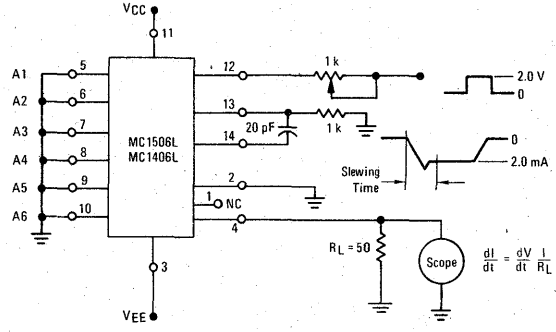


FIGURE 8 – REFERENCE CURRENT SLEW RATE MEASUREMENT TEST CIRCUIT



TEST CIRCUITS and TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – TRANSIENT RESPONSE

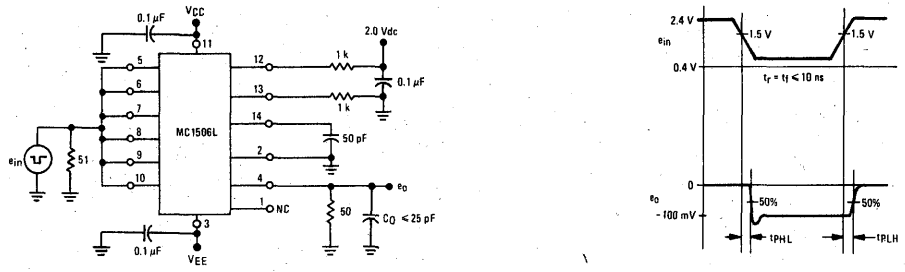


FIGURE 10 – RELATIVE ACCURACY TEST CIRCUIT

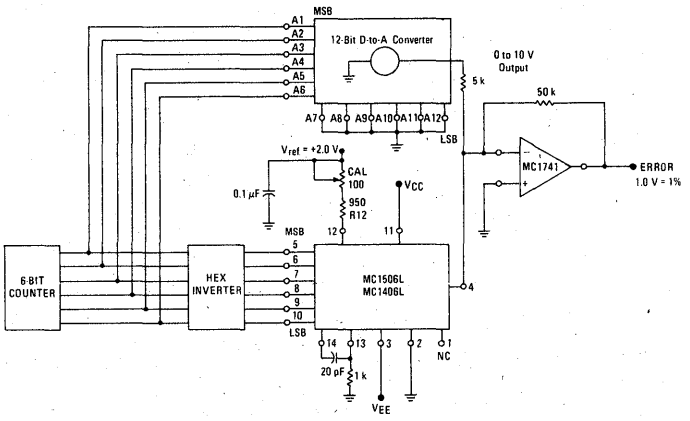


FIGURE 11 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE

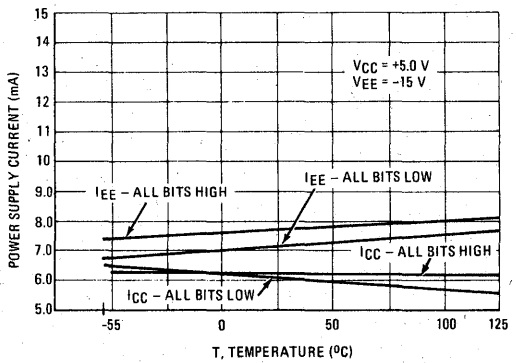
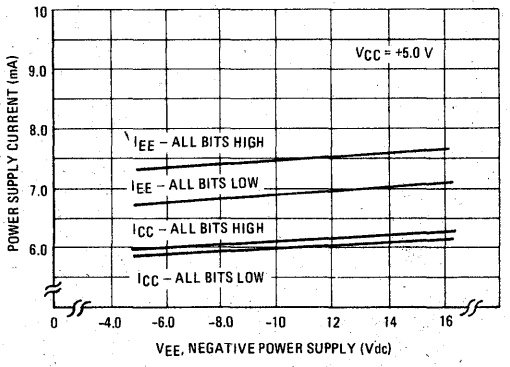


FIGURE 12 – TYPICAL POWER SUPPLY CURRENT versus V_{EE}



TYPICAL CHARACTERISTICS (continued)

FIGURE 13 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

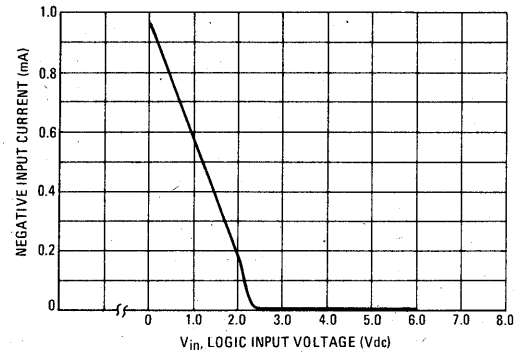


FIGURE 14 – MSB TRANSFER CHARACTERISTICS versus TEMPERATURE (MSB IS "WORST CASE")

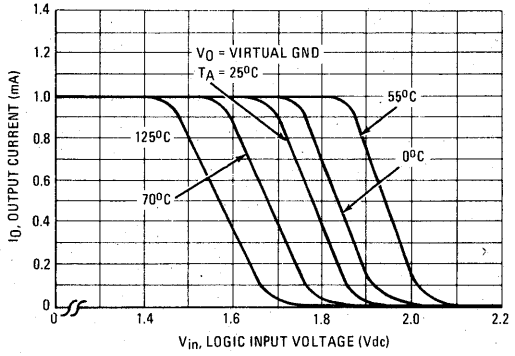
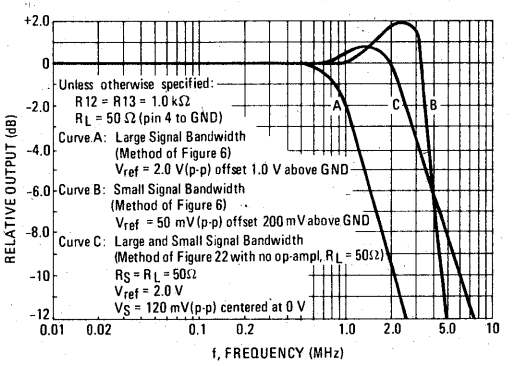


FIGURE 15 – REFERENCE INPUT FREQUENCY RESPONSE



GENERAL INFORMATION

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages below -6.0 volts, due to the increased voltage drop across the 400-ohm resistors in the reference current amplifier.

Output Voltage Compliance

The MC1506L current switches have been designed for high-speed operation and as a result have a restricted output voltage range, as shown in Figures 4 and 5. When a current switch is turned "off", the follower emitter is near ground and a positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington amplifier is one diode voltage below ground; thus a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

For example, at +25°C the allowable voltage compliance on Pin 4 to maintain six-bit accuracy is +0.1 to -0.3 Volts. With a full scale output current of 2.0 mA, the maximum resistor value that can be connected from Pin 4 to ground is 150 ohms.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1506L is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current.

The best temperature performance is achieved with a -6.0 V supply and a reference voltage of -3.0 volts. These conditions match the voltage across the NPN current source pair in the reference amplifier at the lowest possible voltage, matching and optimizing the output impedance of the pair.

The MC1506L/MC1406L is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.969 mA. This corresponds to a reference amplifier output current drive to the ladder of 2.0 mA, with the loss of one LSB = 31 μA that is the ladder remainder shunted to ground. The input current to Pin 12 has a guaranteed current range value of between 1.9 to 2.1 mA, allowing

5

some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 10. The 12-bit converter is calibrated for a full scale output current of 1.969 mA. This is an optional step since the MC1506L accuracy is essentially the same between 1.5 to 2.5 mA. Then the MC1506L full scale current is trimmed to the same value with R12 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 6-bit D-to-A converters may not be used to construct a 12-bit accurate D-to-A converter. 12-bit accuracy implies a total error of ±1/2 of one part in 4096, or ±0.012%, which is more accurate than the ±0.78% specification provided by the MC1506L.

Multiplying Accuracy

The MC1506L may be used in the multiplying mode with six-bit accuracy when the reference current is varied over a range of 64:1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions these six amplifiers can contribute a total of 6.0 μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 60 μA to 4.0 mA, the 6.0 μA contributes an error of 0.1 LSB. This is well within six-bit accuracy.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1506L is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

Settling Time

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a high-to-low transition for all bits. This time is typically 150 ns to within ±1/2 LSB, while the turn "off" is typically under 50 ns.

The slowest single switch is the least significant bit, which turns "on" and settles in 50 ns and turns "off" in 30 ns. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 150 ns may be realized.

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at Pin 12 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I12, must always flow into Pin 12 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6. The reference voltage source supplies the full current I12. Compensation is accomplished by Miller feedback from Pin 14 to Pin 13. This compensation method yields the best slew rate, typically better than 2.0 mA/μs, and is independent of the value of R12. R13 must be used to establish the proper impedance for compensation at Pin 13. For bipolar reference signals, as in the multiplying mode, R13 can be tied to a negative voltage corresponding to the minimum input level. Another method is shown in Figure 22.

It is possible to eliminate R13 with only a small sacrifice in accuracy and temperature drift. For instance when high-speed operation is not needed, a capacitor is connected from pin 14 to V_{EE}. The capacitor value must be increased when R12 is made larger to maintain a proper phase margin. For R12 values of 1.0, 2.5, and 5.0 kilohms, minimum capacitor values are 50, 125, and 250 pF.

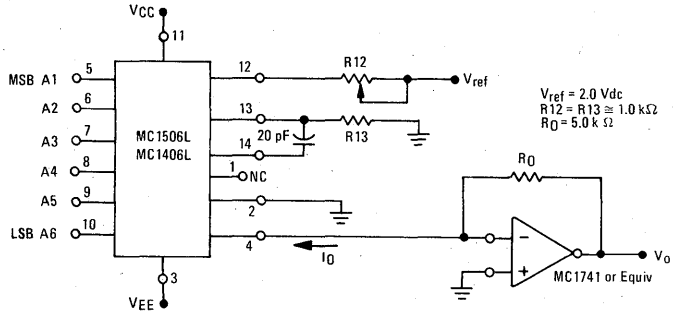
Connections for a negative reference voltage are shown in Figure 7. A high input impedance is the advantage of this method, but Miller feedback cannot be used because it feeds the input signal around the PNP directly into the high impedance node, causing slewing problems and high frequency peaking. Compensation involves a capacitor to V_{EE} on Pin 14, using the values of the previous paragraph. The negative reference voltage must be at least 3.0 V above V_{EE}. Bipolar input signals may be handled by connecting R12 to a positive reference voltage equal to the peak positive input level at Pin 13.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0 V logic supply is not recommended as a reference voltage. If a well regulated 5.0 V supply which drives logic is to be used as the reference, R12 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 μF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between Pin 12 and ground.

If Pin 12 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, thus decreasing the overall bandwidth.

APPLICATIONS INFORMATION

FIGURE 16 – OUTPUT CURRENT VOLTAGE CONVERSION



V_{ref} = 2.0 Vdc
R12 = R13 ≅ 1.0 kΩ
R_O = 5.0 k Ω

Theoretical V_O

$$V_O = \frac{V_{ref}}{R12}(R_O)\left(\frac{\bar{A}1}{2} + \frac{\bar{A}2}{4} + \frac{\bar{A}3}{8} + \frac{\bar{A}4}{16} + \frac{\bar{A}5}{32} + \frac{\bar{A}6}{64}\right) = K\,R_O\left\{\bar{A}\right\}$$

Adjust R_{ref} so that V_O with all digital inputs at low level is equal to 9.844 volts.

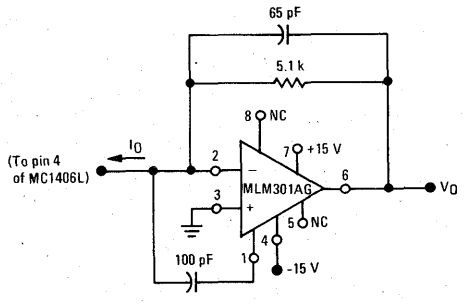
$$V_O = \frac{2\,V}{1\,K}(5\,K)\left(\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}\right) = 10\,V\left(\frac{63}{64}\right) = 9.844\,V$$

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1506L at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

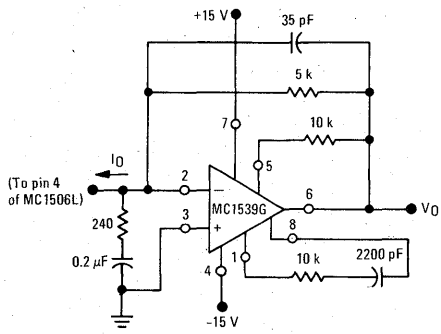
The following circuit shows how the MLM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 μs.

FIGURE 17

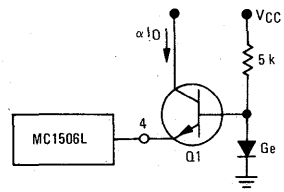


An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 μs. See Motorola Application Note AN-459 for more details on this concept.

FIGURE 18



The positive voltage range may be extended by cascoding the output with a high beta common base transistor, Q1, as shown.



The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing.

APPLICATIONS INFORMATION (continued)

Combined Output Amplifier and Voltage Reference

For many of its applications the MC1506L requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current, see Figure 19. Instead of powering the MC1723G from a single positive voltage supply, it uses a negative bias as well. Although the reference voltage of the MC1723G is then developed with respect to that negative voltage it appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its output amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

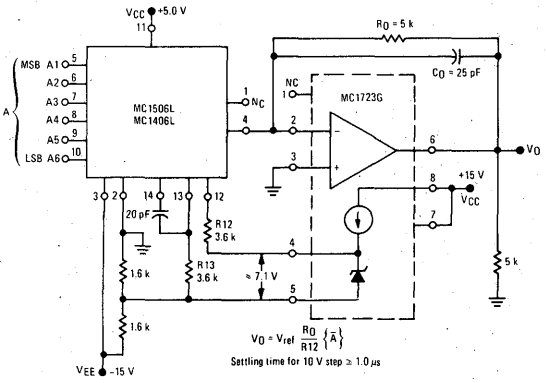
Since ±15 V and +5.0 V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

Full scale output may be increased to as much as 32 volts by increasing R_O and raising the +15 V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. C_O may be decreased to maintain the same R_OC_O product if maximum speed is desired.

Programmable Power Supply

The circuit of Figure 19 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to +6.3 volts in 0.1-volt increments, ±0.05 volt; or 0 to 31.5 volts in 0.5-volt increments, ±0.25 volt.

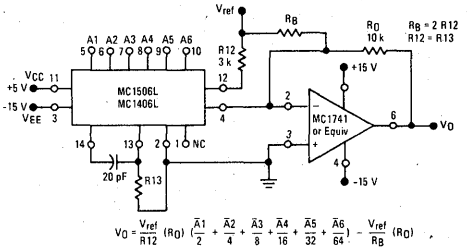
FIGURE 19 – COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



Bipolar or Negative Output Voltage

The circuit of Figure 20 is a variation from the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction. For example, if approximately 1.0 mA is used a bipolar output signal results which may be described as a 6-bit "1's" complement offset binary. V_{ref} may be used as this auxiliary reference. Note that R_O has been doubled to 10 kilohms because of the anticipated 20 V (p-p) output range.

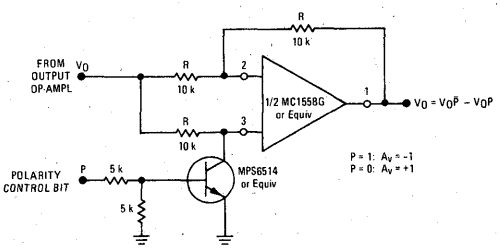
FIGURE 20 – BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT



Polarity Switching Circuit, 6-Bit Magnitude Plus Sign D-to-A Converter

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 21, gives 6-bits magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and -1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 21 – POLARITY SWITCHING CIRCUIT (6-Bit Magnitude Plus Sign D-to-A Converter)



APPLICATIONS INFORMATION (continued)

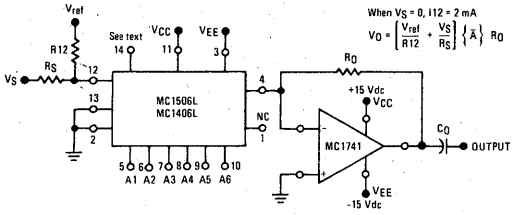
Programmable Gain Amplifier or Digital Attenuator

When used in the multiplying mode the MC1506L can be applied as a digital attenuator. See Figure 22. One advantage of this technique is that if R_S = 50 ohms, no compensation capacitor is needed and a wide large signal bandwidth is achieved. The small and large signal bandwidths are now identical and are shown in Figure 15.

The best frequency response is obtained by not allowing I_{12} to reach zero. R_S can be set for a ±1.0 mA variation in relation to I_{12}. I_{12} can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word that makes ac coupling necessary.

FIGURE 22 – PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT



Panel Meter Readout

The MC1506L can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R12 or V_{ref}.

FIGURE 23 – PANEL METER READOUT CIRCUIT

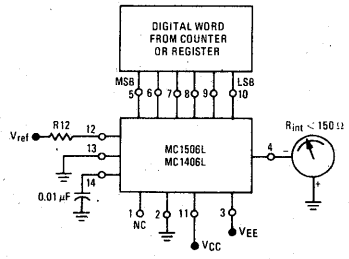
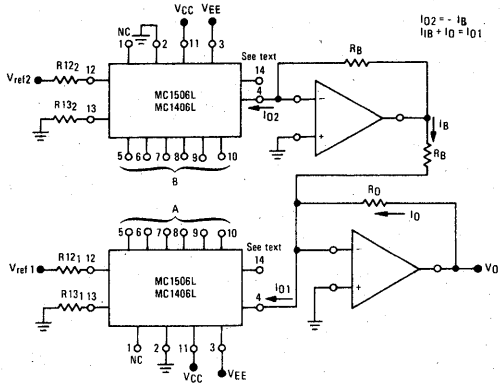


FIGURE 24 – DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION

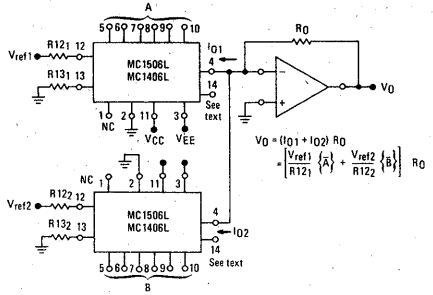


This digital subtraction application is useful for indicating when one digital word is approaching another in value. More information is available than with a digital comparator.

Bipolar inputs can be accepted by using any of the previously described methods, or applied differentially to $R12_1$ and $R12_2$ or $R13_1$ and $R13_2$. V_O will be a bipolar signal defined by the above equation. Note that the circuit shown accepts bipolar differential signals but does not have a negative common-mode range. A very useful method is to connect $R12_1$ and $R12_2$ to a positive reference higher than the most positive input, and drive $R13_1$ and $R13_2$. This yields high input impedance, bipolar differential and common-mode range. The compensation depends on the input method used, as shown in previous sections.

APPLICATIONS INFORMATION (continued)

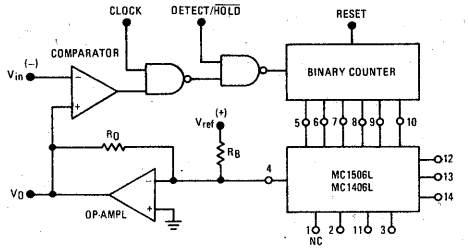
FIGURE 25 – DIGITAL SUMMING and CHARACTER GENERATION



In a character generation system one MC1506L circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke. The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke. Note that this approach does not result in a 12-bit D-to-A converter (see Accuracy Section).

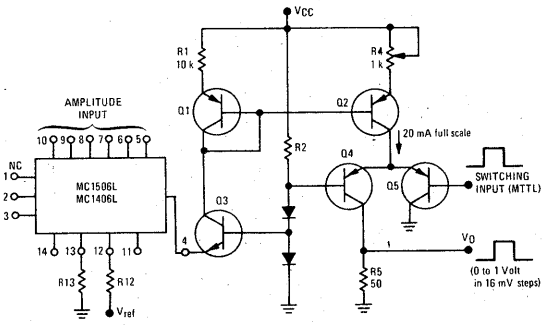
FIGURE 26 – PEAK DETECTING SAMPLE and HOLD

(Features infinite hold time and optional digital output.)



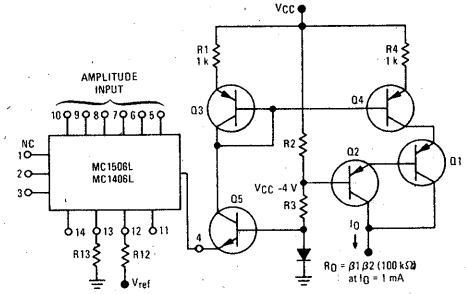
Positive peaks may be detected by inserting a hex inverter between the counter and MC1506L, reversing the comparator inputs, and connecting the output amplifier for unipolar operation.

FIGURE 27 – PROGRAMMABLE PULSE GENERATOR



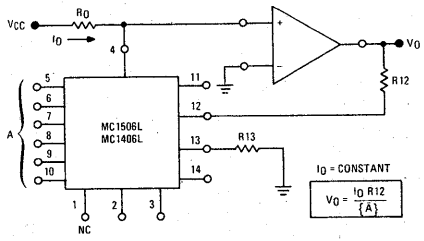
Fast rise and fall times require the use of high speed switching transistors for the differential pair, Q4 and Q5. Linear ramps and sine waves may be generated by the appropriate reference input.

FIGURE 28 – PROGRAMMABLE CONSTANT CURRENT SOURCE



Current pulses, ramps, staircases, and sine waves may be generated by the appropriate digital and reference inputs. This circuit is especially useful in curve tracer applications.

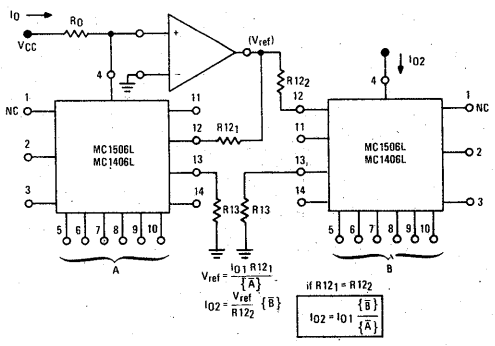
FIGURE 29 – ANALOG DIVISION BY DIGITAL WORD



This circuit yields the inverse of a digital word scaled by a constant. For minimum error over the range of operation, I_O can be set at 62 μA so that I_{12} will have a maximum value of 3.938 mA for a digital bit input configuration of 111110.

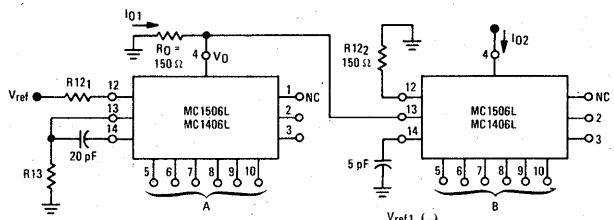
Compensation is necessary for loop stability and depends on the type of operational amplifier used. If a standard 1.0 MHz operational amplifier is employed, it should be overcompensated when possible. If this cannot be done, the reference amplifier can furnish the dominant pole with extra Miller feedback from pin 14 to 13. If the MC1723 or another wideband amplifier is used, the reference amplifier should always be overcompensated.

FIGURE 30 – ANALOG QUOTIENT OF TWO DIGITAL WORDS



APPLICATIONS INFORMATION (continued)

FIGURE 31 – ANALOG PRODUCT OF TWO DIGITAL WORDS (High-Speed Operation)



$$V_O = I_{O1} R_O = \frac{V_{ref1}}{R12_1} \{\bar{A}\} R_O$$

$$I_{O2} = \frac{\{\bar{B}\} I_{O1}}{R12_2}$$

$$= \frac{\{\bar{B}\}}{R12_2} \left[R_O \left(\frac{V_{ref1}}{R12_1} \right) \{\bar{A}\} \right]$$

since $R_O = R12_2$ and $K = V_{ref}/R12_1$

$$I_{O2} = K\{\bar{A}\}\{\bar{B}\}$$

K can be an analog variable.

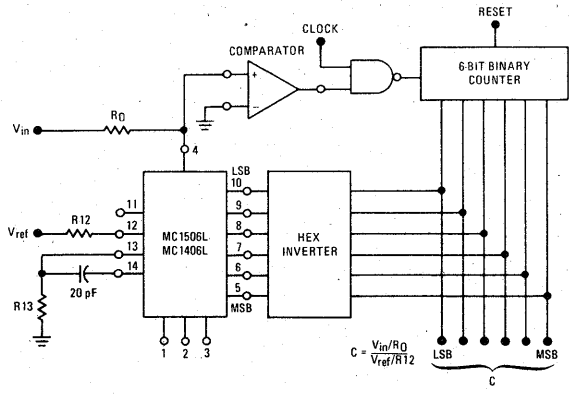
Two Digit BCD Conversion

MC1506L parts which meet the specification for 7-bit accuracy can be used for the most significant word when building a two digit BCD D-to-A or A-to-D converter. If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten.

5

FIGURE 32 – DIGITAL QUOTIENT of TWO ANALOG VARIABLES or ANALOG-TO-DIGITAL CONVERSION

The circuit shown is a simple counter-ramp converter. An UP/DOWN counter and dual threshold comparator can be used to provide faster operation and continuous conversion.



ORDERING INFORMATION

Device	Temperature Range	Package
MC1408L6	0°C to +75°C	Ceramic DIP
MC1408L7	0°C to +75°C	Ceramic DIP
MC1408L8	0°C to +75°C	Ceramic DIP
MC1408P6	0°C to +75°C	Plastic DIP
MC1408P7	0°C to +75°C	Plastic DIP
MC1408P8	0°C to +75°C	Plastic DIP
MC1508L8	−55°C to +125°C	Ceramic DIP

MC1408
MC1508

Specifications and Applications Information

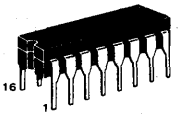
EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

. . . designed for use where the output current is a linear product of an eight-bit digital word and an analog input voltage.

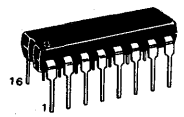
- Eight-Bit Accuracy Available in Both Temperature Ranges
  Relative Accuracy: ±0.19% Error maximum
  (MC1408L8, MC1408P8, MC1508L8)
- Seven and Six-Bit Accuracy Available with MC1408 Designated by 7 or 6 Suffix after Package Suffix
- Fast Settling Time — 300 ns typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible
- Output Voltage Swing — +0.4 V to -5.0 V
- High-Speed Multiplying Input
  Slew Rate 4.0 mA/μs
- Standard Supply Voltages: +5.0 V and -5.0 V to -15 V

EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

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FIGURE 1 — D-to-A TRANSFER CHARACTERISTICS

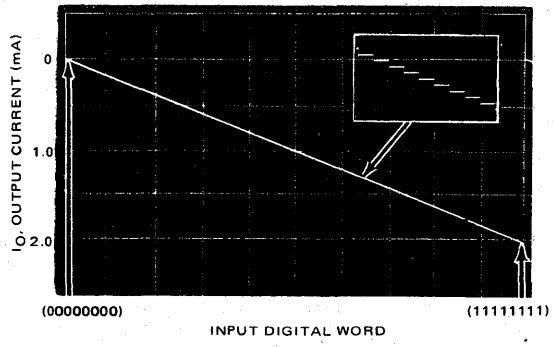
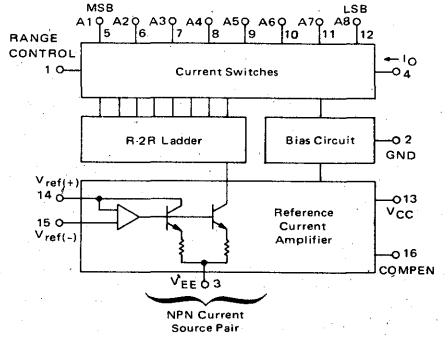


FIGURE 2 — BLOCK DIAGRAM



TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 2 1/2 Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+5.5 -16.5	Vdc
Digital Input Voltage	V_5 thru V_{12}	0 to +5.5	Vdc
Applied Output Voltage	V_O	+0.5,-5.2	Vdc
Reference Current	I_{14}	5.0	mA
Reference Amplifier Inputs	V_{14},V_{15}	V_{CC},V_{EE}	Vdc
Operating Temperature Range MC1508 MC1408 Series	T_A	 -55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

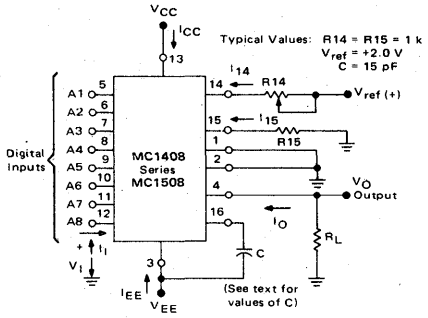
ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -15 Vdc, $\frac{V_{ref}}{R14}$ = 2.0 mA, MC1508L8: T_A = -55°C to +125°C. MC1408L Series: T_A = 0 to +75°C unless otherwise noted. All digital inputs at high logic level.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O) MC1508L8, MC1408L8, MC1408P8 MC1408P7, MC1408L7, See Note 1 MC1408P6, MC1408L6, See Note 1	4	E_r	 – – –	 – – –	 ±0.19 ±0.39 ±0.78	%
Settling Time to within ±1/2 LSB [includes t_{PLH}] (T_A=+25°C) See Note 2	5	t_S	–	300	–	ns
Propagation Delay Time T_A = +25°C	5	t_{PLH},t_{PHL}	–	30	100	ns
Output Full Scale Current Drift		TCI_O	–	-20	–	PPM/°C
Digital Input Logic Levels (MSB) High Level, Logic "1" Low Level, Logic "0"	3	 V_{IH} V_{IL}	 2.0 –	 – –	 – 0.8	Vdc
Digital Input Current (MSB) High Level, V_{IH} = 5.0 V Low Level, V_{IL} = 0.8 V	3	 I_{IH} I_{IL}	 – –	 0 -0.4	 0.04 -0.8	mA
Reference Input Bias Current (Pin 15)	3	I_{15}	–	-1.0	-5.0	μA
Output Current Range V_{EE} = -5.0 V V_{EE} = -15 V, T_A = 25°C	3	I_{OR}	 0 0	 2.0 2.0	 2.1 4.2	mA
Output Current V_{ref} = 2.000 V, R14 = 1000 Ω	3	I_O	 1.9	 1.99	 2.1	mA
Output Current (All bits low)	3	$I_{O(min)}$	–	0	4.0	μA
Output Voltage Compliance ($E_r \leq$ 0.19% at T_A = +25°C) Pin 1 grounded Pin 1 open, V_{EE} below -10 V	3	V_O	 – –	 – –	 -0.55, +0.4 -5.0, +0.4	Vdc
Reference Current Slew Rate	6	SR I_{ref}	–	4.0	–	mA/μs
Output Current Power Supply Sensitivity		PSRR(–)	–	0.5	2.7	μA/V
Power Supply Current (All bits low)	3	I_{CC} I_{EE}	– –	+13.5 -7.5	+22 -13	mA
Power Supply Voltage Range (T_A = +25°C)	3	V_{CCR} V_{EER}	+4.5 -4.5	+5.0 -15	+5.5 -16.5	Vdc
Power Dissipation All bits low V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc All bits high V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc	3	P_D	 – – – –	 105 190 90 160	 170 305 – –	mW

Note 1. All current switches are tested to guarantee at least 50% of rated output current.
Note 2. All bits switched.

TEST CIRCUITS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT



V_I and I_I apply to inputs A1 thru A8

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left\{\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right\}$$

where $K \cong \frac{V_{ref}}{R14}$,

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

FIGURE 4 – RELATIVE ACCURACY TEST CIRCUIT

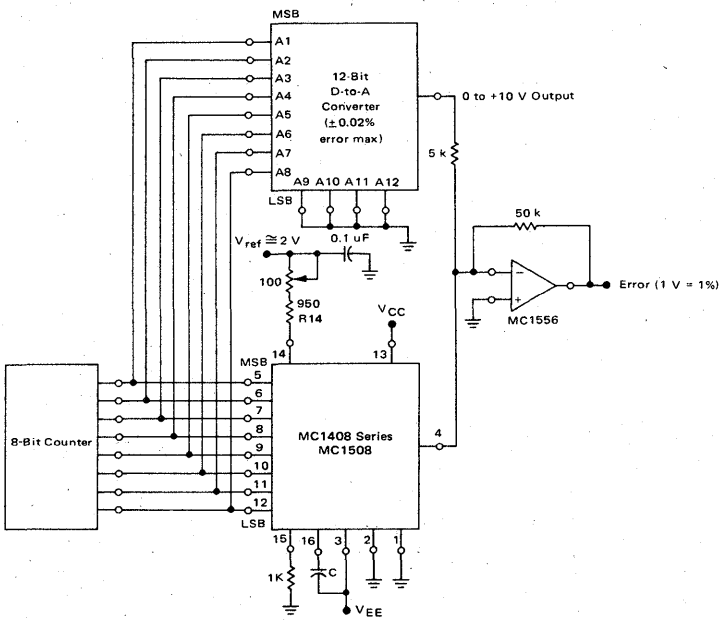
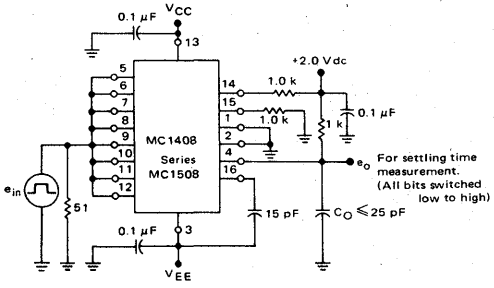
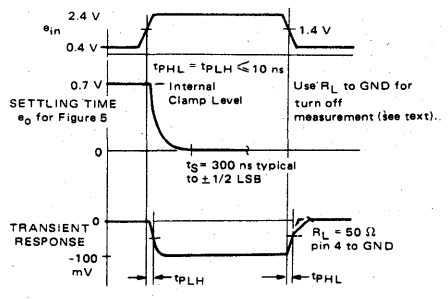


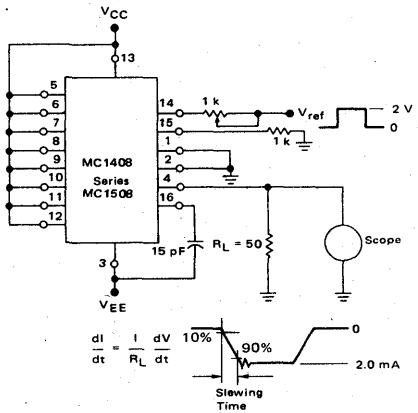
FIGURE 5 – TRANSIENT RESPONSE and SETTLING TIME





TEST CIRCUITS (continued)

FIGURE 6 – REFERENCE CURRENT SLEW RATE MEASUREMENT



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

FIGURE 7 – POSITIVE V_{ref}

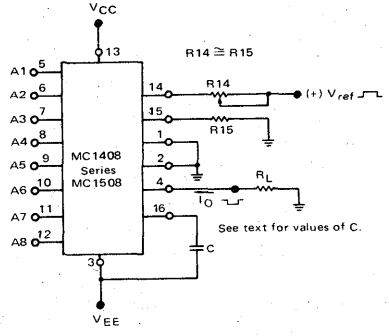


FIGURE 8 – NEGATIVE V_{ref}

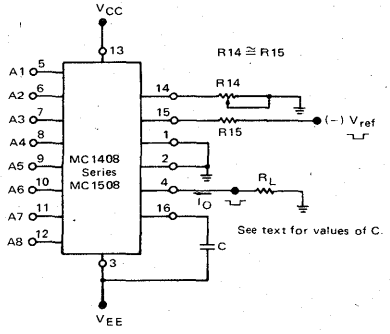


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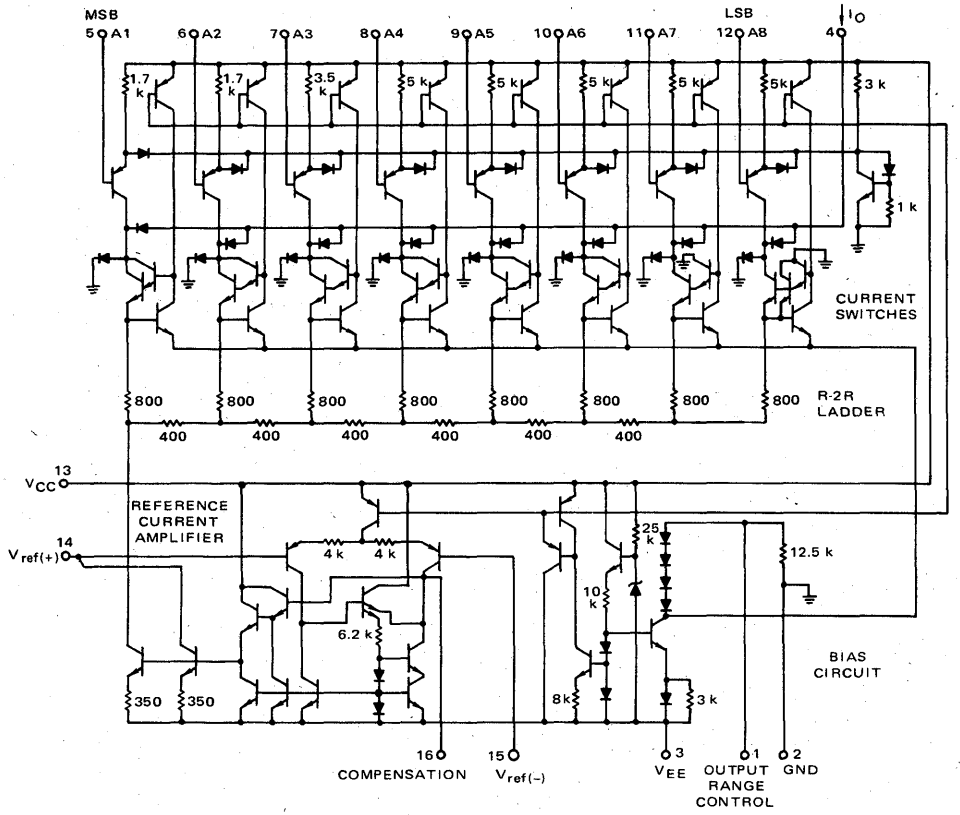
FIGURE 9 – MC1408, MC1508 SERIES EQUIVALENT CIRCUIT SCHEMATIC

DIGITAL INPUTS



CIRCUIT DESCRIPTION

The MC1408 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component. The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

GENERAL INFORMATION

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I14, must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 7. The reference voltage source supplies the full current I14. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift. Another method for bipolar inputs is shown in Figure 25.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1.0, 2.5 and 5.0 kilohms, minimum capacitor values are 15, 37, and 75 pF. The capacitor should be tied to V_{EE} as this increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in Figure 8. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0-volts above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0-V logic supply is not recommended as a reference voltage. If a well regulated 5.0-V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 μF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.55 to +0.4 volts at +25°C, due to the current switching methods employed in the MC1408. When a current switch is turned "off", the positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is one diode voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC1408 may be extended to -5.0 V volts by opening the circuit at pin 1. The negative supply voltage must be more negative than -10 volts. Using a full scale current of 1.992 mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance, but a 2.5-kilohm load increases "worst case" settling time to 1.2 μs (when all bits are switched on). Refer to the subsequent text section on Settling Time for more details on output loading.

If a power supply value between -5.0 V and -10 V is desired, a voltage of between 0 and -5.0 V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages typically more negative than -8.0 volts, due to the increased voltage drop across the 350-ohm resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1408 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC1408 has a very low full scale current drift with temperature.

The MC1408/MC1508 Series is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0 mA, with the loss of one LSB = 8.0 μA which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 4. The 12-bit converter is calibrated for a full scale output current of 1.992 mA. This is an optional step since the MC1408 accuracy is essentially the same between 1.5 and 2.5 mA. Then the MC1408 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65, 536, or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the MC1408x8.

Multiplying Accuracy

The MC1408 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions, these eight amplifiers can contribute a total of 1.6 μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 16 μA to 4.0 mA, the 1.6 μA contributes an error of 0.1 LSB. This is well within eight-bit accuracy referenced to 4.0 mA.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1408 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

GENERAL INFORMATION (Continued)

Settling Time

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a low-to-high transition for all bits. This time is typically 300 ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100 ns. These times apply when $R_L \leqslant 500$ ohms and $C_O \leqslant 25$ pF.

The slowest single switch is the least significant bit, which turns "on" and settles in 250 ns and turns "off" in 80 ns. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 300 ns may be realized. Bit A7 turns "on" in 200 ns and "off" in 80 ns, while bit A6 turns "on" in 150 ns and "off" in 80 ns.

The test circuit of Figure 5 requires a smaller voltage swing for the current switches due to internal voltage clamping in the MC-1408. A 1.0-kilohm load resistor from pin 4 to ground gives a typical settling time of 400 ns. Thus, it is voltage swing and not the output RC time constant that determines settling time for most applications.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

TYPICAL CHARACTERISTICS

(V_{CC} = +5.0 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

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FIGURE 10 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

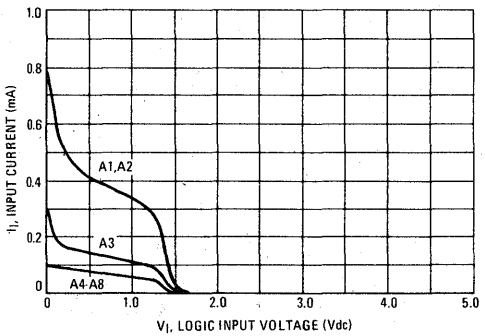


FIGURE 11 – TRANSFER CHARACTERISTIC versus TEMPERATURE
(A5 thru A8 thresholds lie within range for A1 thru A4)

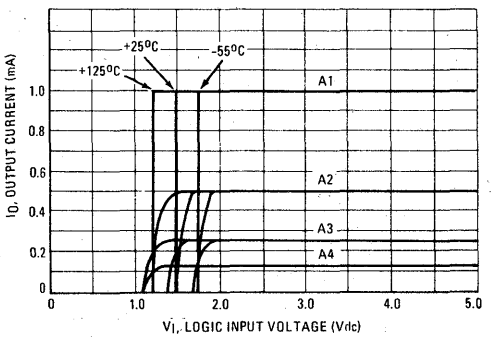


FIGURE 12 – OUTPUT CURRENT versus OUTPUT VOLTAGE
(See text for pin 1 restrictions)

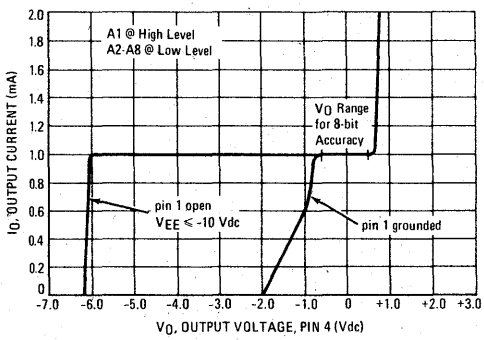
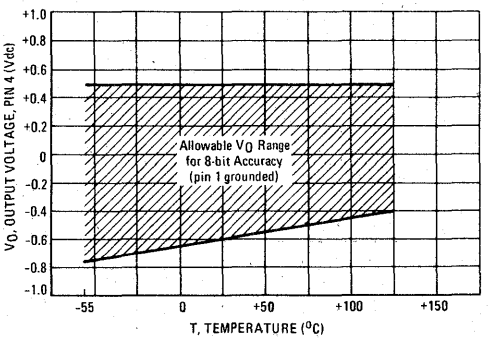


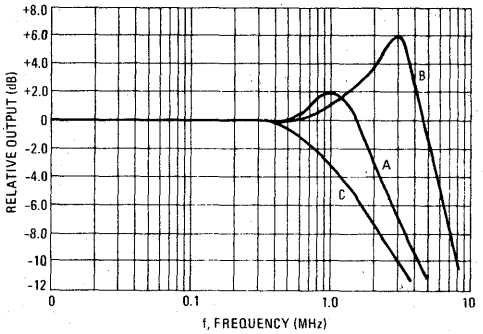
FIGURE 13 – OUTPUT VOLTAGE versus TEMPERATURE
(Negative range with pin 1 open is -5.0 Vdc over full temperature range)



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 14 – REFERENCE INPUT FREQUENCY RESPONSE



Unless otherwise specified:

R14 = R15 = 1.0 kΩ
C = 15 pF, pin 16 to V_{EE}
R_L = 50 Ω, pin 4 to GND

Curve A: Large Signal Bandwidth
Method of Figure 7
V_{ref} = 2.0 V(p-p) offset 1.0 V above GND

Curve B: Small Signal Bandwidth
Method of Figure 7 R_L = 250 Ω
V_{ref} = 50 mV(p-p) offset 200 mV above GND

Curve C: Large and Small Signal Bandwidth
Method of Figure 25 (no op-ampl, R_L = 50 Ω)
R_S = 50 Ω
V_{ref} = 2.0 V
V_S = 100 mV(p-p) centered at 0 V

FIGURE 15 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE (all bits low)

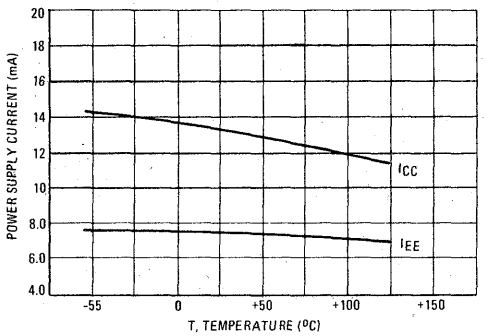
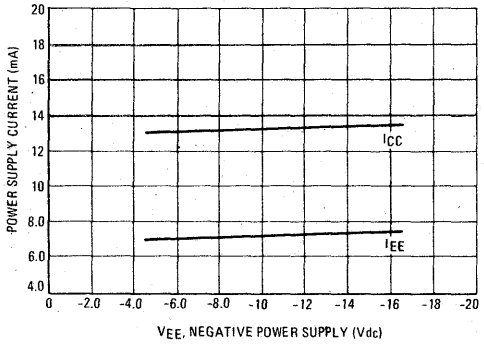
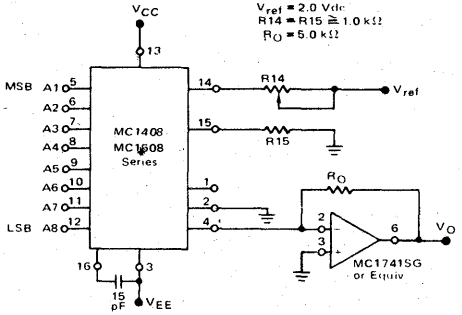


FIGURE 16 – TYPICAL POWER SUPPLY CURRENT versus V_{EE} (all bits low)



APPLICATIONS INFORMATION

FIGURE 17 – OUTPUT CURRENT TO VOLTAGE CONVERSION



Theoretical V_O

$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R14 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

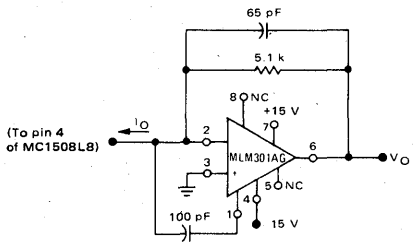
APPLICATIONS INFORMATION (continued)

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1408 at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

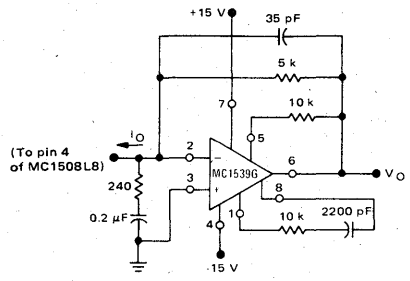
The following circuit shows how the MLM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 μs.

FIGURE 18



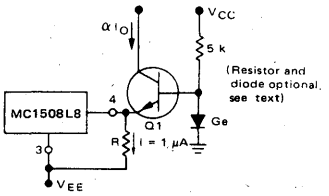
An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 μs. See Motorola Application Note AN-459 for more details on this concept.

FIGURE 19



The positive voltage range may be extended by cascading the output with a high beta common base transistor, Q1, as shown.

FIGURE 20 – EXTENDING POSITIVE VOLTAGE RANGE



The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. If pin 1 is left open, the transistor base may be grounded, eliminating both the resistor and the diode. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing, because pin 4 is held at a constant voltage. The resistor (R) to V_{EE} maintains the transistor emitter voltage when all bits are "off" and insures fast turn-on of the least significant bit.

Combined Output Amplifier and Voltage Reference

For many of its applications the MC1408 requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current. See Figure 21. The MC1723G uses both a positive and negative power supply. The reference voltage of the MC1723G is then developed with respect to the negative voltage and appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its output amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

Since ±15 V and +5.0 V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

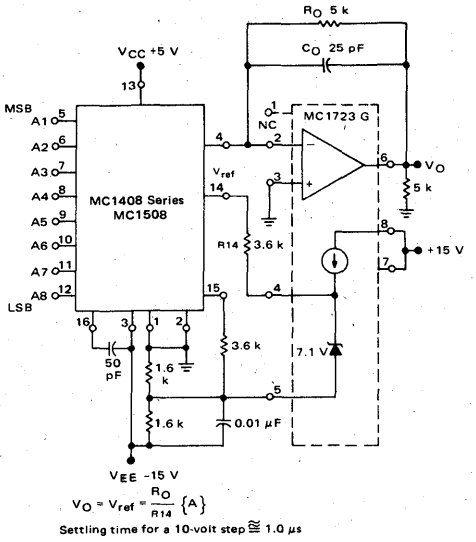
Full scale output may be increased to as much as 32 volts by increasing R_O and raising the +15 V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. C_O may be decreased to maintain the same R_OC_O product if maximum speed is desired.

APPLICATIONS INFORMATION (continued)

Programmable Power Supply

The circuit of Figure 21 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to +25.5 volts in 0.1-volt increments, ±0.05 volt; or 0 to 5.1 volts in 20 mV increments, ±10 mV.

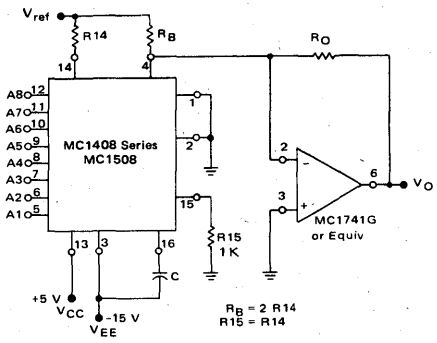
FIGURE 21 – COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



$$V_O = V_{ref} = \frac{R_O}{R14}\{A\}$$

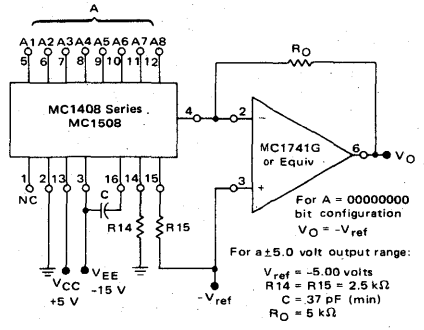
Settling time for a 10-volt step ≅ 1.0 µs

FIGURE 22 – BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT



$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]-\frac{V_{ref}}{R_B}(R_O)$$

FIGURE 23 – BIPOLAR OR INVERTED NEGATIVE OUTPUT VOLTAGE CIRCUIT



Bipolar or Negative Output Voltage

The circuit of Figure 22 is a variation from the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction. For example, if approximately 1.0 mA is used a bipolar output signal results which may be described as a 8-bit "1's" complement offset binary. V_{ref} may be used as this auxiliary reference. Note that R_O has been doubled to 10 kilohms because of the anticipated 20 V(p-p) output range.

Decrease R_O to 2.5 kΩ for a 0 to -5.0-volt output range. This application provides somewhat lower speed, as previously discussed in the Output Voltage Range section of the General Information.

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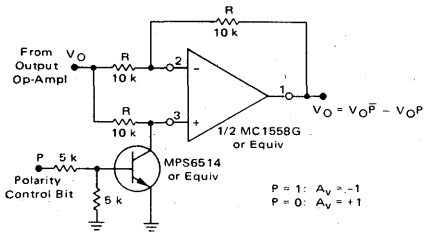
APPLICATIONS INFORMATION (continued)

Polarity Switching Circuit, 8-Bit Magnitude Plus Sign D-to-A Converter

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 24 gives 8-bit magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and -1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 24 – POLARITY SWITCHING CIRCUIT
(8-Bit Magnitude Plus Sign D-to-A Converter)



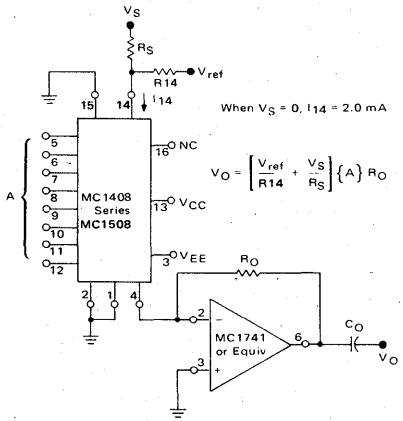
Programmable Gain Amplifier or Digital Attenuator

When used in the multiplying mode the MC1408 can be applied as a digital attenuator. See Figure 25. One advantage of this technique is that if R_S = 50 ohms, no compensation capacitor is needed. The small and large signal bandwidths are now identical and are shown in Figure 14.

The best frequency response is obtained by not allowing I_{14} to reach zero. However, the high impedance node, pin 16, is clamped to prevent saturation and insure fast recovery when the current through R14 goes to zero. R_S can be set for a ±1.0 mA variation in relation to I_{14}. I_{14} can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word which makes ac coupling necessary.

FIGURE 25 – PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT



Panel Meter Readout

The MC1408 can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R14 or V_{ref}.

FIGURE 26 – PANEL METER READOUT CIRCUIT

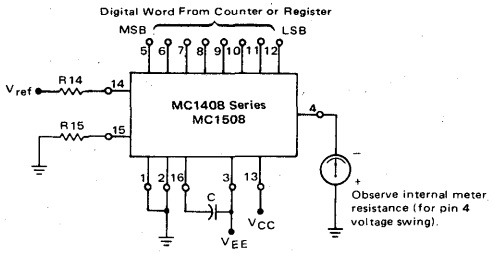
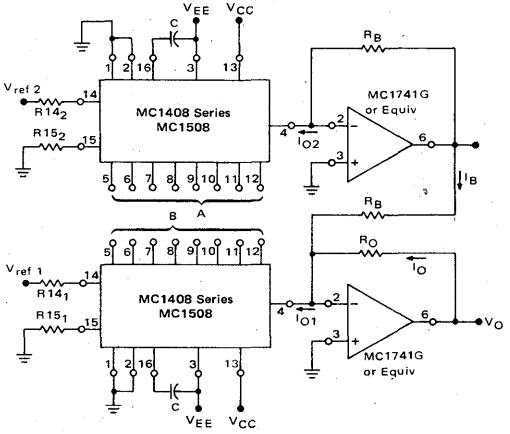


FIGURE 27 – DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION



$I_O = I_{O1} - I_{O2} = \frac{V_{ref\,1}}{R14_1}\{A\} \quad \frac{V_{ref\,2}}{R14_2}\{B\} \qquad I_{O2} = -I_B$

$I_B + I_O = I_{O1}$

Digital Subtraction:

Let $\frac{V_{ref\,1}}{R14_1} = \frac{V_{ref\,2}}{R14_2}$

Programmable Amplifier:
Connect Digital Inputs so A = B

$$V_O = \frac{V_{ref\,1}}{R14_1} R_O [\{A\} - \{B\}]$$

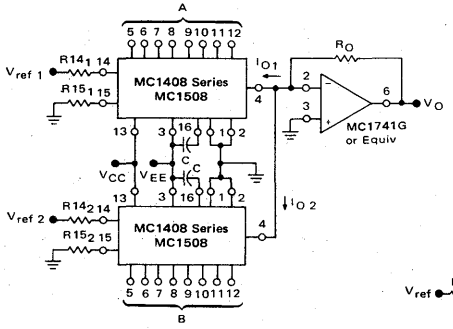
$$V_O = \{A\}\left[\frac{V_{ref\,1}}{R14_1} - \frac{V_{ref\,2}}{R14_2}\right]$$

APPLICATIONS INFORMATION (continued)

This digital subtraction application is useful for indicating when one digital word is approaching another in value. More information is available than with a digital comparator.

Bipolar inputs can be accepted by using any of the previously described methods, or applied differentially to $R14_1$ and $R14_2$ or $R15_1$ and $R15_2$. V_O will be a bipolar signal defined by the above equation. Note that the circuit shown accepts bipolar differential signals but does not have a negative common-mode range. A very useful method is to connect $R14_1$ and $R14_2$ to a positive reference higher than the most positive input, and drive $R15_1$ and $R15_2$. This yields high input impedance, bipolar differential and common-mode range.

FIGURE 28 – DIGITAL SUMMING and CHARACTER GENERATION



$$V_O = (I_{O\,1} + I_{O\,2})\ R_O$$

$$V_O = \left[\frac{V_{ref\ 1}}{R14_1}\{A\} + \frac{V_{ref\ 2}}{R14_2}\{B\}\right] R_O$$

In a character generation system one MC1408 circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke. The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke. Note that this approach does not result in a 16-bit D-to-A converter (see Accuracy Section).

FIGURE 29 – POSITIVE PEAK DETECTING SAMPLE and HOLD
(Features indefinite hold time and optional digital output.)

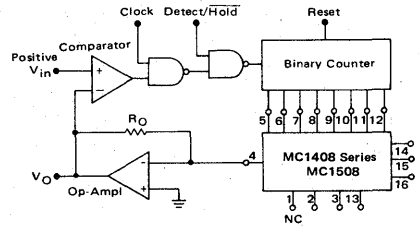
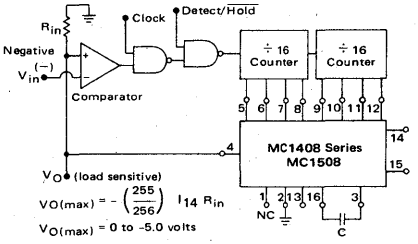


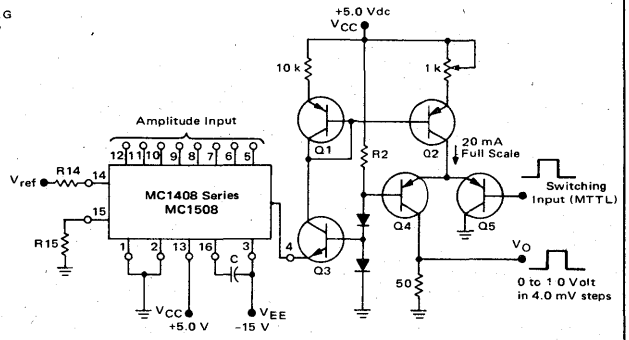
FIGURE 30 – NEGATIVE PEAK DETECTING SAMPLE AND HOLD



$$V_{O(max)} = -\left(\frac{255}{256}\right) I_{14}\ R_{in}$$

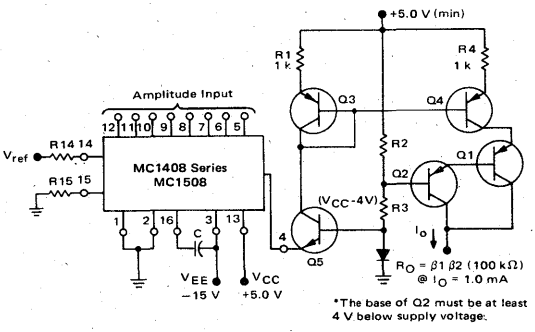
$V_{O(max)}$ = 0 to -5.0 volts

FIGURE 31 – PROGRAMMABLE PULSE GENERATION



Fast rise and fall times require the use of high-speed switching transistors for the differential pair, Q4 and Q5. Linear ramps and sine waves may be generated by the appropriate reference input.

FIGURE 32 – PROGRAMMABLE CONSTANT CURRENT SOURCE



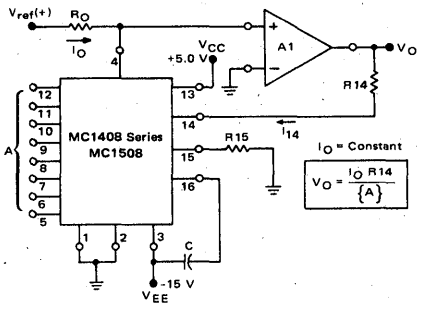
*The base of Q2 must be at least 4 V below supply voltage.

Current pulses, ramps, staircases, and sine waves may be generated by the appropriate digital and reference inputs. This circuit is especially useful in curve tracer applications.

5

APPLICATIONS INFORMATION (continued)

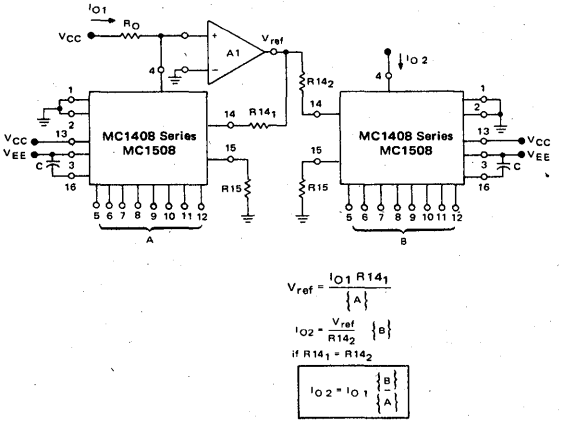
FIGURE 33 – ANALOG DIVISION BY DIGITAL WORD



This circuit yields the inverse of a digital word scaled by a constant. For minimum error over the range of operation, I_O can be set at 16 μA so that I_{14} will have a maximum value of 3.984 mA for a digital bit input configuration of 00000001.

Compensation is necessary for loop stability and depends on the type of operational amplifier used. If a standard 1.0 MHz operational amplifier is employed, it should be overcompensated when possible. If the MC1723 or another wideband amplifier is used, the reference amplifier should always be overcompensated.

FIGURE 34 – ANALOG QUOTIENT OF TWO DIGITAL WORDS



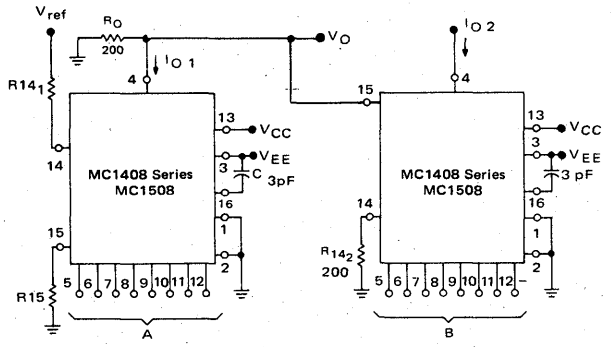
$$V_{ref} = \frac{I_{O1} R14_1}{\{A\}}$$

$$I_{O2} = \frac{V_{ref}}{R14_2} \{B\}$$

if $R14_1 = R14_2$

$$I_{O2} = I_{O1} \frac{\{B\}}{\{A\}}$$

FIGURE 35 – ANALOG PRODUCT OF TWO DIGITAL WORDS
(High-Speed Operation)



$$V_O = -I_{O1} R_O = \frac{V_{ref}}{R14_1} \{A\} R_O$$

$$I_{O2} = \frac{\{B\} |V_O|}{R14_2} = \frac{\{B\}}{R14_2} \left[R_O \left(\frac{V_{ref}}{R14_1} \right) \{A\} \right]$$

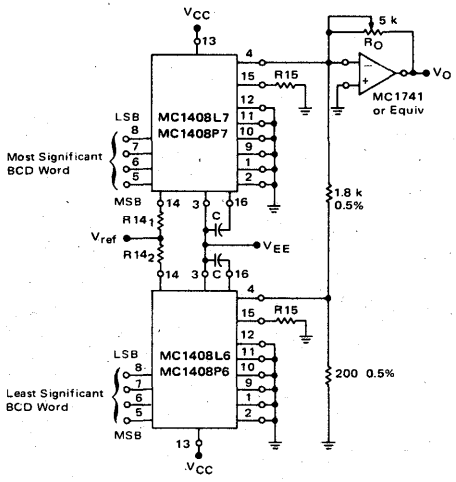
Since $R_O = R14_2$ and $K = \frac{V_{ref}}{R14_1}$

$$I_{O2} = K \{A\} \{B\}$$

K can be an analog variable.

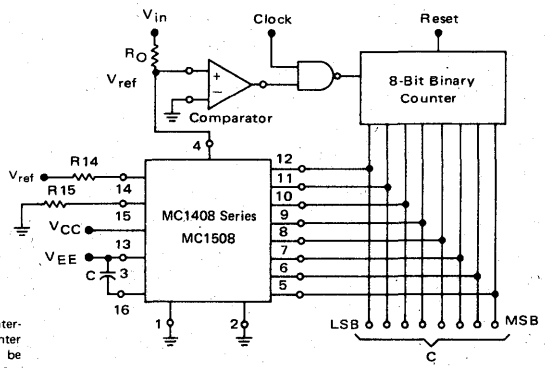
APPLICATIONS INFORMATION (continued)

FIGURE 36 – TWO-DIGIT BCD CONVERSION



Two 8-bit, D-to-A converters can be used to build a two digit BCD D-to-A or A-to-D converter. If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten and thus an MC1408L6 may be used for the least significant word.

FIGURE 37 – DIGITAL QUOTIENT OF TWO ANALOG VARIABLES or ANALOG-TO-DIGITAL CONVERSION



$$C = \frac{V_{in}/R_O}{V_{ref}/R14}$$

The circuit shown is a simple counter-ramp converter. An UP/DOWN counter and dual threshold comparator can be used to provide faster operation and continuous conversion.

MC1411 (ULN2001A)
MC1412 (ULN2002A)
MC1413 (ULN2003A)
MC1416 (ULN2004A)

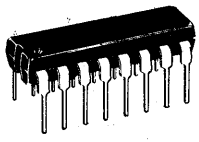
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

The seven NPN Darlington connected transistors in these arrays are well suited for driving lamps, relays or printer hammers in a variety of industrial and consumer applications. Their high breakdown voltage and internal suppression diodes insure freedom from problems associated with inductive loads. Peak inrush currents to 600 mA permit them to drive incandescent lamps.

The MC1411 device is a general-purpose array for use with DTL, TTL, PMOS or CMOS Logic. The MC1412 contains a zener diode, and resistor in series with the input to limit input current for use with 14 to 25 Volt PMOS Logic. The MC1413 with a 2.7 kΩ series input resistor is well-suited for systems utilizing 5 Volt TTL or CMOS Logic. The MC1416 uses a series 10.5 kΩ resistor and is useful in 8–18 Volt MOS systems.

PERIPHERAL DRIVER ARRAYS

SILICON MONOLITHIC INTEGRATED CIRCUITS



P OR PW SUFFIX
PLASTIC PACKAGE
CASE 648

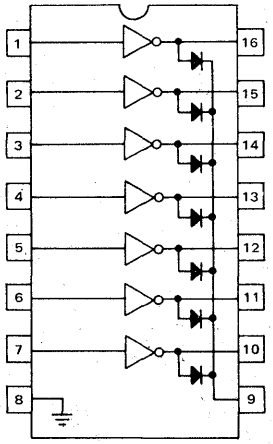
5

MAXIMUM RATINGS (T_A = 25°C and rating apply to any one device in the package unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50*	V
Input Voltage (Except MC1411)	V_I	30	V
Collector Current – Continuous	I_C	500	mA
Base Current – Continuous	I_B	25	mA
Operating Ambient Temperature Range	T_A	0 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Junction Temperature	T_J	150	°C

Maximum Package Power Dissipation (See Thermal Information Section)
*Higher voltage selection available. See your local representative.

PIN CONNECTIONS



DEVICE CROSS-REFERENCE LISTING

9665 – SN75476 – ULN2001A – order MC1411P or PW
9666 – SN75477 – ULN2002A – order MC1412P or PW
9667 – SN75478 – ULN2003A – order MC1413P or PW
9668 – – ULN2004A – order MC1416P or PW

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Leakage Current		I_{CEX}				μA
*(V_O = 50 V, T_A = +70°C)	All Types		–	–	100	
*(V_O = 50 V, T_A = +70°C, V_I = 6.0 V)	MC1412		–	–	500	
*(V_O = 50 V, T_A = +70°C, V_I = 1.0 V)	MC1416		–	–	500	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				V
(I_C = 350 mA, I_B = 500 μA)			–	1.1	1.6	
(I_C = 200 mA, I_B = 350 μA)			–	0.95	1.3	
(I_C = 100 mA, I_B = 250 μA)			–	0.85	1.1	
Input Current – On Condition		$I_{I(on)}$				mA
(V_I = 17 V)	MC1412		–	0.85	1.3	
(V_I = 3.85 V)	MC1413		–	0.93	1.35	
(V_I = 5.0 V)	MC1416		–	0.35	0.5	
(V_I = 12 V)	MC1416		–	1.0	1.45	
Input Voltage – On Condition		$V_{I(on)}$				V
(V_{CE} = 2.0 V, I_C = 300 mA)	MC1412		–	–	13	
(V_{CE} = 2.0 V, I_C = 200 mA)	MC1413		–	–	2.4	
(V_{CE} = 2.0 V, I_C = 250 mA)	MC1413		–	–	2.7	
(V_{CE} = 2.0 V, I_C = 300 mA)	MC1413		–	–	3.0	
(V_{CE} = 2.0 V, I_C = 125 mA)	MC1416		–	–	5.0	
(V_{CE} = 2.0 V, I_C = 200 mA)	MC1416		–	–	6.0	
(V_{CE} = 2.0 V, I_C = 275 mA)	MC1416		–	–	7.0	
(V_{CE} = 2.0 V, I_C = 350 mA)	MC1416		–	–	8.0	
Input Current – Off Condition (I_C = 500 μA, T_A = +70°C)		$I_{I(off)}$	50	100	–	μA
DC Current Gain (V_{CE} = 2.0 V, I_C = 350 mA)	MC1411	h_{FE}	1000	–	–	–
Input Capacitance		C_I	–	15	30	pF
Turn-On Delay Time (50% E_I to 50% E_O)		t_{on}	–	1.0	5.0	μs
Turn-Off Delay Time (50% E_I to 50% E_O)		t_{off}	–	1.0	5.0	μs
Clamp Diode Leakage Current (V_R = 50 V)		I_R	–	–	50	μA
Clamp Diode Forward Voltage (I_F = 350 mA)		V_F	–	1.5	2.0	V

*Higher voltage selections available, contact your local representative.

TYPICAL PERFORMANCE CURVES – T_A = 25°C

FIGURE 1 – OUTPUT CURRENT versus INPUT VOLTAGE

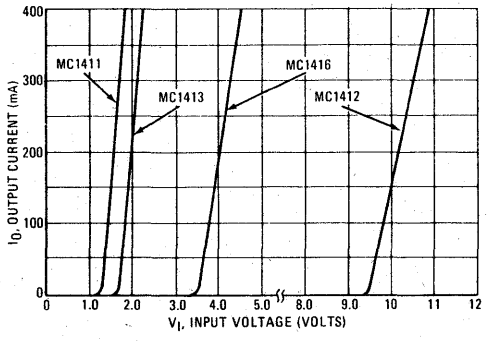
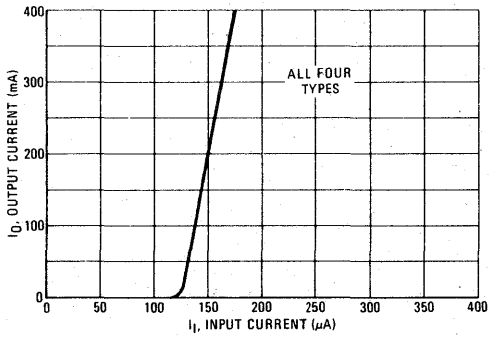


FIGURE 2 – OUTPUT CURRENT versus INPUT CURRENT



TYPICAL CHARACTERISTIC CURVES – T_A = 25°C (continued)

FIGURE 3 – TYPICAL OUTPUT CHARACTERISTICS

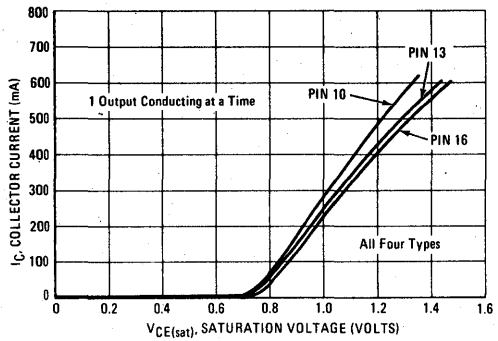


FIGURE 4 – INPUT CHARACTERISTICS – MC1412

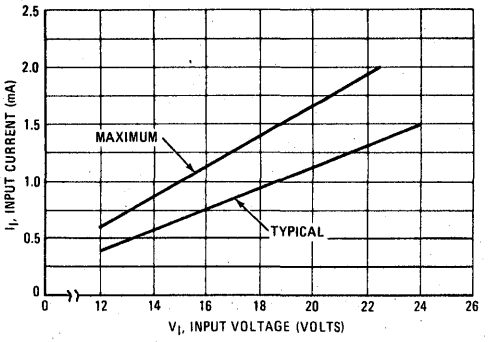


FIGURE 5 – INPUT CHARACTERISTICS – MC1413

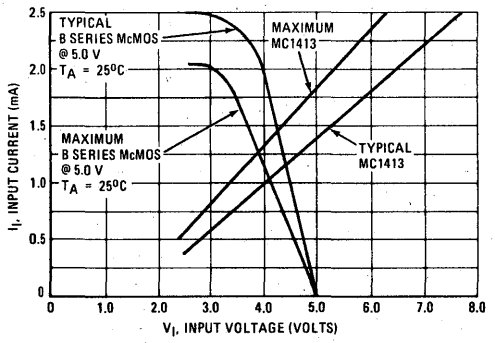
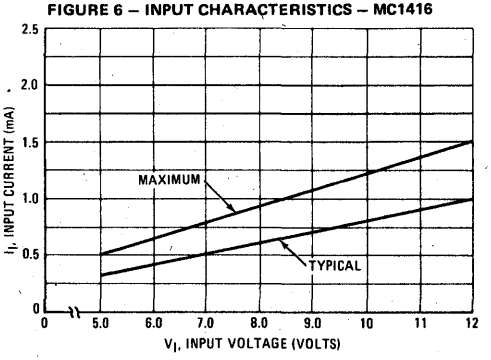
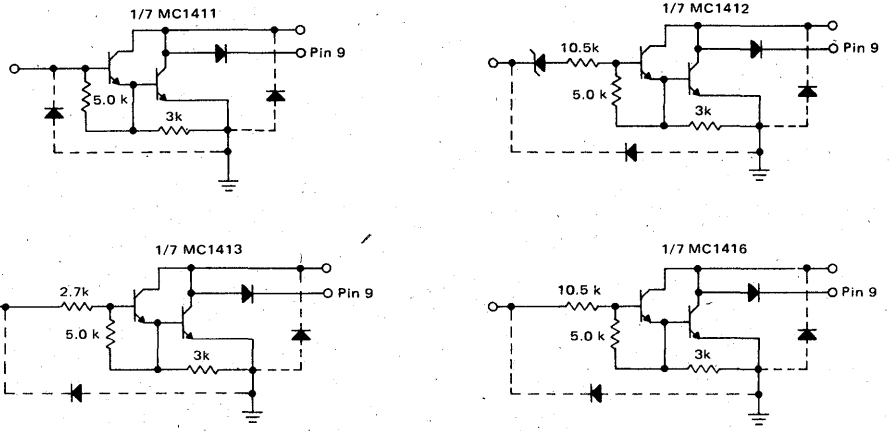


FIGURE 6 – INPUT CHARACTERISTICS – MC1416



REPRESENTATIVE CIRCUIT SCHEMATICS



ORDERING INFORMATION

Device	Temperature Range	Package
MC1440G	0°C to +75°C	Metal Can
MC1440L	0°C to +75°C	Ceramic DIP
MC1540G	−55°C to +125°C	Metal Can
MC1540L	−55°C to +125°C	Ceramic DIP

MC1440
MC1540

CORE MEMORY SENSE AMPLIFIER

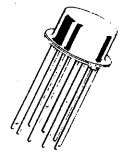
SILICON MONOLITHIC INTEGRATED CIRCUIT

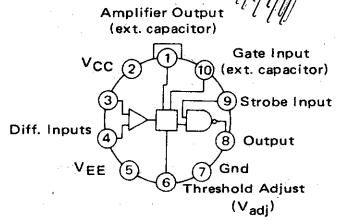
SENSE AMPLIFIER

. . . consisting of a wideband differential amplifier, a dc restoration circuit which also incorporates facilities to externally adjust the threshold, and an MDTL output gate which is strobed from saturated logic. It is designed to detect bipolar differential signals derived by a core memory with cycle times as low as 0.5 μs.

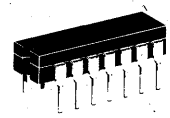
- Differential Threshold Characteristics:
  - Adjustable Threshold — 10-25 mV
  - Nominal Threshold — 17 mV @ V_{adj} = 6.0 V
  - Input Offset Voltage — 1.0 mV typical
  - Threshold Drift — −10 μV/°C typical
- Fast Response Time — 20 ns typical
- Short Recovery Time :
  - 50 ns max @ V_i = 1.8 V Common Mode
  - 50 ns max @ V_o = 400 mV Differential Mode

G SUFFIX
CASE 603B

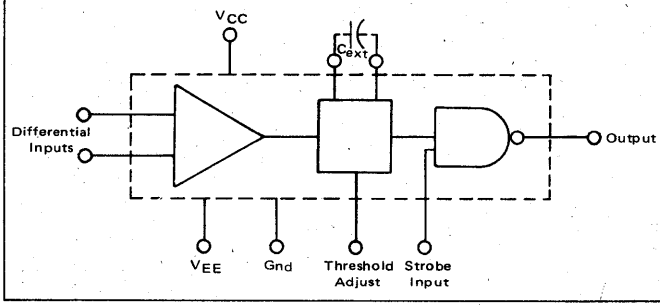




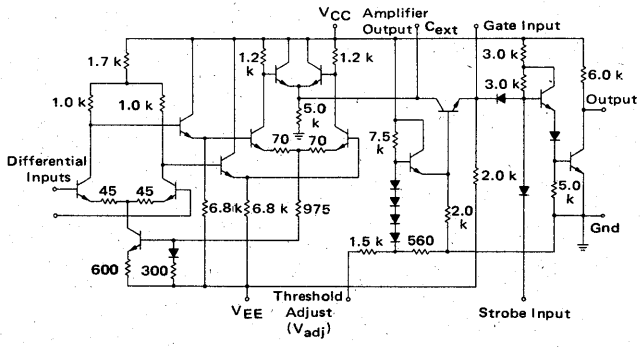
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

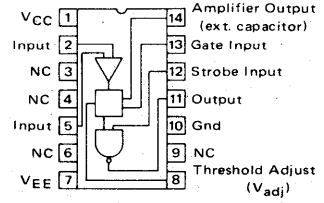


MC1540/MC1440 BLOCK DIAGRAM



REPRESENTATIVE CIRCUIT SCHEMATIC





5

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+10 -10	Vdc
Differential Input Voltage Range	V_{IDR}	±5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Output Load Current	I_L	25	mA
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above 25°C		4.6	mW/°C
Flat Package		500	mW
Derate above 25°C		3.3	mW/°C
Plastic and Ceramic DIP		625	mW
Derate above 25°C		5.0	mW/°C
Operating Ambient Temperature Range	T_A		
MC1540		0 to 75	°C
MC1440		-55 to 125	°C
Storage Temperature Range	T_{stg}	-65 to 150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, T_A = 25°C, V_{CC} = +6.0 Vdc ±1.0%, V_{EE} = -6.0 Vdc ±1% and C_{ext} = 0.01 μF)

Characteristic	Symbol	MC1540 Min	MC1540 Typ	MC1540 Max	MC1440 Min	MC1440 Typ	MC1440 Max	Unit
Input Threshold Voltage	V_{th}							mV
(V_{adj} = -6.0 V, T_A = 25°C)		14	17	20	12	17	24	
(V_{adj} = -6.0 V, T_A = T_{low}*)		12	17	24	10	17	30	
(V_{adj} = -6.0 V, T_A = T_{high}*)		12	17	22	10	17	30	
Input Offset Voltage	V_{IO}	–	1.0	5.0	–	1.0	6.0	mV
Input Bias Current	I_{IB}							μA
(T_A = 25°C)		–	7.5	50	–	7.5	75	
(T_A = T_{high} to T_{low})		–	–	100	–	–	100	
Input Offset Current	I_{IO}	–	2.0	10	–	2.0	15	μA
Output Voltage– High Logic State	V_{OH}	5.9	–	–	5.8	–	–	Vdc
Output Voltage – Low Logic State	V_{OL}							mV
(I_{OL} = 6.0 mA, $V_{IH(G)}$ = 6.0 V)		–	–	350	–	–	400	
(T_A = T_{high})		–	–	400	–	–	450	
Amplifier Voltage Gain	A_v	–	85	–	–	85	–	V/V
(V_i = 15 mV peak)								
Strobe Input Current – Low Logic State	$I_{IL(S)}$	–	–	1.2	–	–	1.5	mA
($V_{IL(S)}$ = 0 V)								
Strobe Input Current – High Logic State	$I_{IH(S)}$							μA
($V_{IH(S)}$ = 5.0 V)		–	–	2.0	–	–	5.0	
($V_{IH(S)}$ = 6.0 V, T_A = T_{high})		–	–	25	–	–	30	
Power Consumption	P_C	–	120	180	–	120	250	mW

*T_{low} = -55°C for MC1540, 0°C for MC1440
T_{high} = 125°C for MC1540, 75°C for MC1440

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 6.0 V, V_{EE} = -6.0 V, T_A = 25°C, C_{ext} = 0.01 μF.)

Characteristic	Symbol	MC1540 Min	MC1540 Typ	MC1540 Max	MC1440 Min	MC1440 Typ	MC1440 Max	Unit
Propagation Delay Time from Differential Input to Amplifier Output	$t_{PLH(A)}$	–	10	15	–	10	20	ns
Propagation Delay Time from Differential Input to Low Logic State Output	$t_{PHL(A)}$	–	20	30	–	20	50	ns
Propagation Delay Time from Strobe Input to Low Logic State Output	$t_{PHL(S)}$	–	10	15	–	10	30	ns
Differential Mode Recovery Time	$t_{R(DM)}$	–	20	50	–	20	90	ns
Common-Mode Recovery Time	$t_{R(CM)}$	–	20	50	–	20	60	ns

FIGURE 1 – THRESHOLD VOLTAGE TEST CIRCUIT AND WAVEFORMS

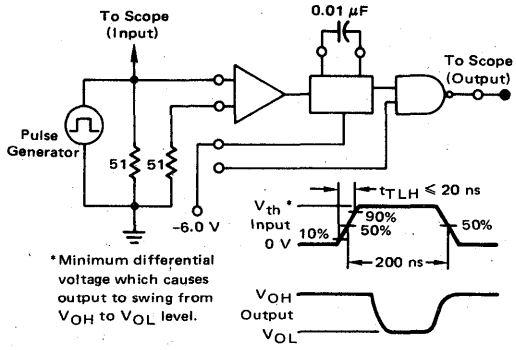


FIGURE 2 – AMPLIFIER VOLTAGE GAIN TEST CIRCUIT AND WAVEFORMS

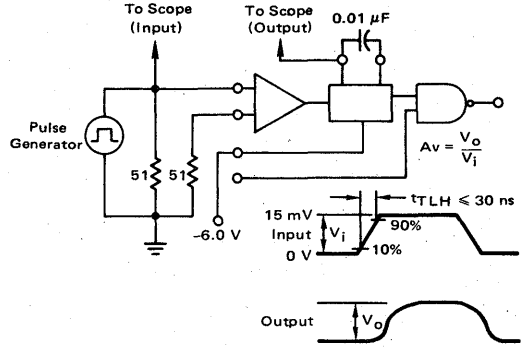


FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DIFFERENTIAL INPUTS TO AMPLIFIER AND GATE OUTPUTS

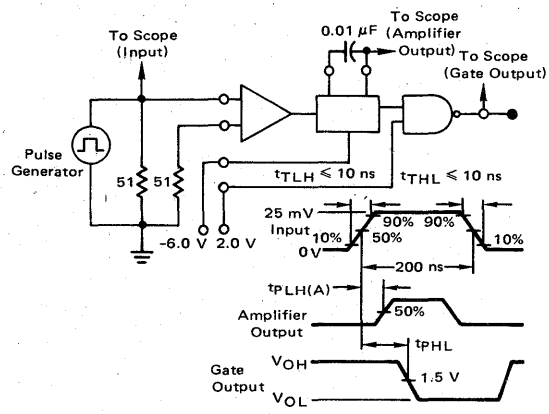


FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM STROBE INPUT TO OUTPUT

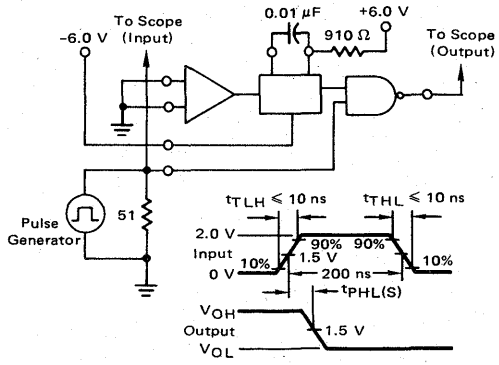


FIGURE 5 – TEST CIRCUIT AND WAVEFORMS FOR DIFFERENTIAL MODE RECOVERY TIME

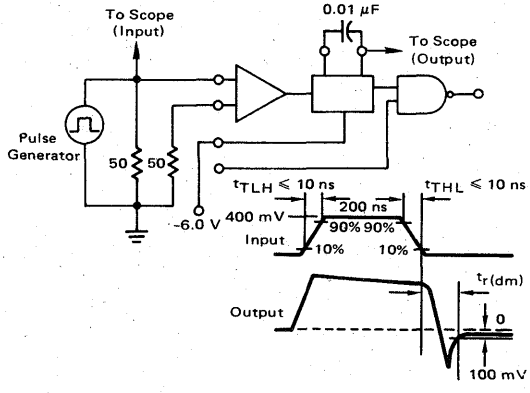
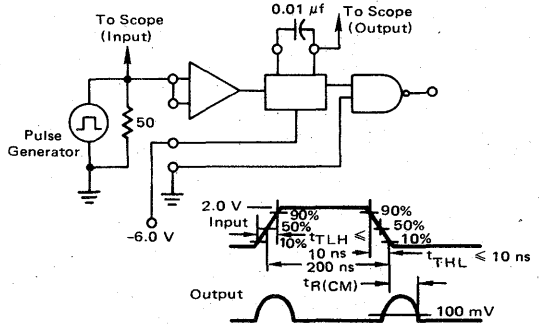


FIGURE 6 – TEST CIRCUIT AND WAVEFORMS FOR COMMON-MODE RECOVERY TIME



NOTE: The output shown is representative of that obtained, however, the two pulse amplitudes may not be equal or even present. Input Pulse width equals 200 ns, f = 1.0 MHz.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1444F	0°C to +75°C	Ceramic Flat
MC1444L	0°C to +75°C	Ceramic DIP
MC1544F	−55°C to +125°C	Ceramic Flat
MC1544L	−55°C to +125°C	Ceramic DIP

MC1444
MC1544

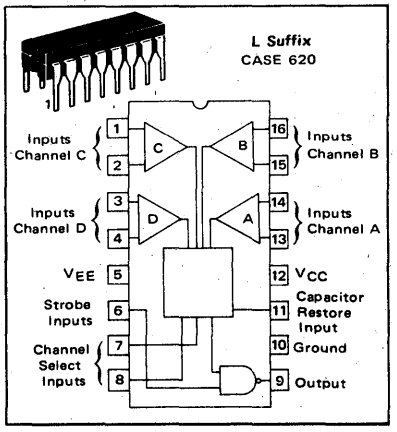
HIGH-SPEED, LOW THRESHOLD SENSE AMPLIFIERS

The MC1544 and MC1444 are high-speed quad sense amplifiers for use with plated wire, thin film or other memory systems requiring very low threshold sensitivity and narrow pulse widths. Both devices feature internal capacitive coupling to reduce the effects of voltage offsets.

- Threshold Level — 1.5 mV (Typ), 100 ns Rectangular Pulse
- Decoded Input Channel Selection
- Output Strobe Capability
- DC Level Restore Gate on Internal Capacitors Eliminates Repetition Rate Limitations

AC-COUPLED FOUR-CHANNEL SENSE AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



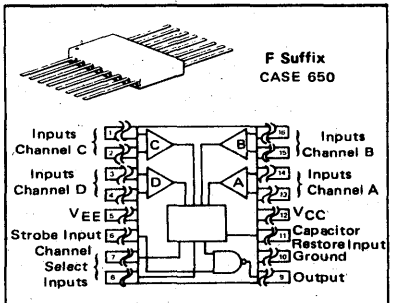
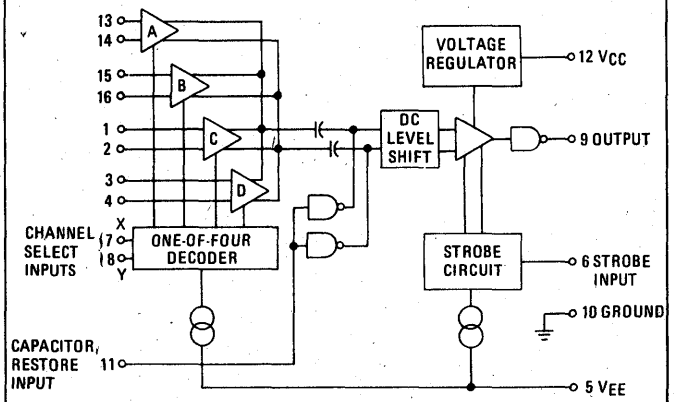


FIGURE 1 — BLOCK DIAGRAM



TRUTH TABLES

Channel Select		
Pin 7(X)	Pin 8(Y)	Channel Selected
H	H	A
L	H	B
H	L	C
L	L	D

H = high level (steady state, $V_I \geq V_{IH(min)}$ or $V_{ID} > V_{th}$
L = low level (steady state), $V_I \leq V_{IL(max)}$ or $V_{ID} < V_{th}$
X = irrelevant (any input, including transitions)
⌐ = transition from low level to high level
⌐¬ = low-level output pulse

Inputs				Output
Strobe	Capacitor Restore	Differential Input *Channel A	Channel Selects	
L	X	X	X X	H
X	H	X	X X	H
X	X	X	L X	H
X	X	X	X L	H
H	L	H	H ⌐	⌐¬
H	L	H	⌐ H	⌐¬
⌐	L	H	H H	⌐¬

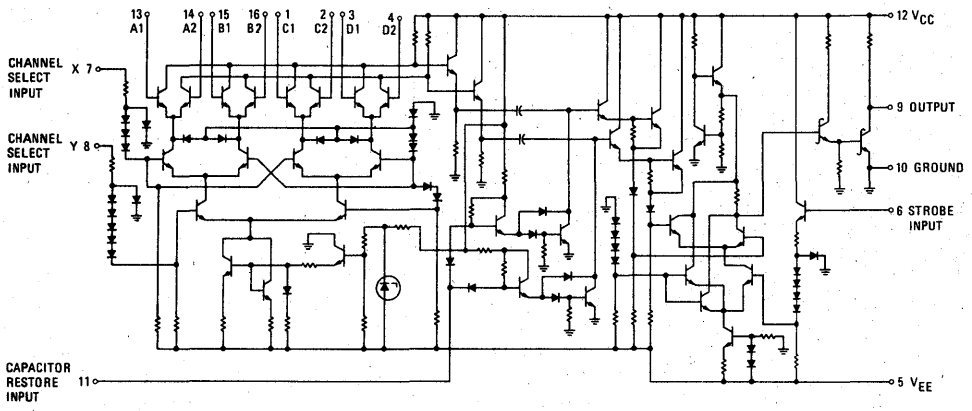
*Channel A used as an example, other channels function similarly. See channel select table.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted).

Rating		Symbol	Value	Unit
Power Supply Voltages(1)		V_{CC} V_{EE}	+7.0 -8.0	Vdc
Input Common-Mode Voltage Range		V_{ICR}	+5.0, -6.0	Vdc
Input Differential-Mode Voltage Range(2)		V_{IDR}	+5.0, -6.0	Vdc
Input Capacitor Restore, Channel Select, and Strobe Voltage		$V_{I(CR)}$ $V_{I(CS)}$ $V_{I(S)}$	+5.5	Vdc
Power Dissipation (Package Limitation) Derate above T_A = 25°C		P_D	1.0 6.7	Watt mW/°C
Operating Ambient Temperature Range	MC1544 MC1444	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C
Operating Junction Temperature		T_J	+175	°C

(1) All voltage values, except differential voltages, are with respect to the network ground terminal.
(2) Differential input voltages are at A1 with respect to A2, and similarly B1 to B2, C1 to C2, and D1 to D2.

FIGURE 2 – EQUIVALENT CIRCUIT SCHEMATIC



RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	4.75 -5.7	5.0 -6.0	5.25 -6.30	V
Input Common-Mode Current	I_{IC}	– –	– –	200 -10	μA
Input Differential Current	I_{ID}	–	–	200	μA

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for 4.75 V ≤ V_{CC} ≤ 5.25 V, -5.7 V ≥ V_{EE} ≥ -6.3 V, T_A = 25°C.)

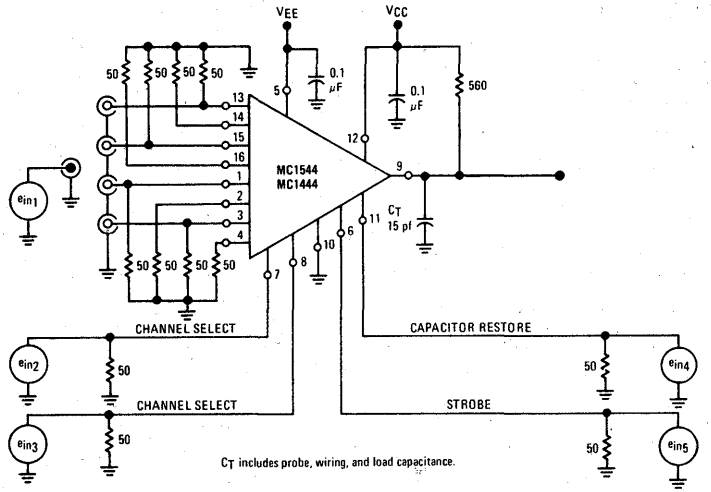
Characteristic	Symbol	MC1544 Min	MC1544 Typ	MC1544 Max	MC1444 Min	MC1444 Typ	MC1444 Max	Unit
Input Threshold Voltage (Figure 4) (V_{CC} = 5.0 V, V_{EE} = -6.0 V, T_A = T_{high} to T_{low}) (1)	V_{th}	0.5	1.0	1.5	0.3	1.0	2.3	mV
Input Bias Current (Selected Channel)	I_{IB}	–	20	50	–	20	50	μA
Input Offset Current (Selected Channel)	I_{IO}	–	1.0	10	–	1.0	10	μA
Channel Select Input Current-High Logic State, ($V_{IH(CS)}$ = 3.5 V)	$I_{IH(CS)}$	–	–	2.6	–	–	2.6	mA
Channel Select Input Current - Low Logic State, ($V_{IL(CS)}$ = 0 V)	$I_{IL(CS)}$	–	–	1.0	–	–	1.0	mA
Capacitor Restore Input Current - High Logic State, ($V_{IH(CR)}$ = 3.5 V)	$I_{IH(CR)}$	–	–	10	–	–	10	μA
Capacitor Restore Input Current-Low Logic State, ($V_{IL(CR)}$ = 0 V)	$I_{IL(CR)}$	–	–	-3.5	–	–	-3.5	mA
Strobe Input Current-High Logic State, ($V_{IH(S)}$ = 3.5 V)	$I_{IH(S)}$	–	–	200	–	–	200	μA
Strobe Input Current-Low Logic State ($V_{IL(S)}$ = 0 V)	$I_{IL(S)}$	–	–	200	–	–	200	μA
Channel Select Input Voltage-Low Logic State	$V_{IL(CS)}$	–	–	0.7	–	–	0.7	V
Channel Select Input Voltage-High Logic State	$V_{IH(CS)}$	2.1	–	–	2.1	–	–	V
Capacitor Restore Input Voltage-Low Logic State	$V_{IL(CR)}$	–	–	0.8	–	–	0.8	V
Capacitor Restore Input Voltage-High Logic State	$V_{IH(CR)}$	2.0	–	–	2.0	–	–	V
Strobe Input Voltage-Low Logic State	$V_{IL(S)}$	–	–	0.8	–	–	0.8	V
Strobe Input Voltage-High Logic State	$V_{IH(S)}$	2.0	–	–	2.0	–	–	V
Input Common-Mode Voltage Range	V_{ICR+} V_{ICR-}	– –	4.7 -6.0	– –	– –	4.7 -6.0	– –	V
Input Differential Voltage Range	V_{IDR}	–	±3.7	–	–	±3.7	–	V
Output Voltage-Low Logic State (I_{OL} = 10 mA)	V_{OL}	– –	– –	0.5 0.4	– –	– –	0.5 0.4	V
Output Voltage-High Logic State (I_{OH} = -400 μA)	V_{OH}	2.4	–	–	2.4	–	–	V
Positive Power Supply Current	I_{CC}	–	–	30	–	–	30	mA
Negative Power Supply Current	I_{EE}	–	–	30	–	–	30	mA

SWITCHING CHARACTERISTICS (unless otherwise noted, T_A = 25°C, V_{CC} = 5.0 V, V_{EE} = -6.0 V)

Characteristic	Symbol	MC1544 Min	MC1544 Typ	MC1544 Max	MC1444 Min	MC1444 Typ	MC1444 Max	Unit
Propagation Delay Time Differential Inputs to High Logic State Output	$t_{PLH(D)}$	–	40	–	–	40	–	ns
Propagation Delay Time Differential Input to Low Logic State Output	$t_{PHL(D)}$	–	18	25	–	18	25	ns
Propagation Delay Time Strobe Input to High Logic State Output	$t_{PLH(S)}$	–	30	–	–	30	–	ns
Propagation Delay Time Strobe Input to Low Logic State Output	$t_{PHL(S)}$	–	18	25	–	18	25	ns
Lead Time from Channel Select Input to Application of Differential Input Voltage	$t_{L(CS)}$	–	45	–	–	45	–	ns
Lead Time from Application of a 50 mV Offset Signal to Application of the Capacitor Restore Signal	$t_{L(CRO)}$	–	15	–	–	15	–	ns
Lead Time from Application of Strobe Input to Application of Differential Input Signal	$t_{L(S)}$	–	10	–	–	10	–	ns
Lead Time from Application of Capacitor Restore Signal to Application of Differential Input Signal	$t_{L(CR)}$	–	10	–	–	10	–	ns
Common-Mode Recovery Time (e_{in1} = +2.0 V) (e_{in1} = -2.0 V)	 t_{CMR+} t_{CMR-}	 – –	 50 50	 – –	 – –	 50 50	 – –	ns
Differential-Mode Recovery Time (e_{in1} = +1.0 V) (e_{in1} = -1.0 V)	 t_{DMR+} t_{DMR-}	 – –	 65 65	 – –	 – –	 65 65	 – –	ns

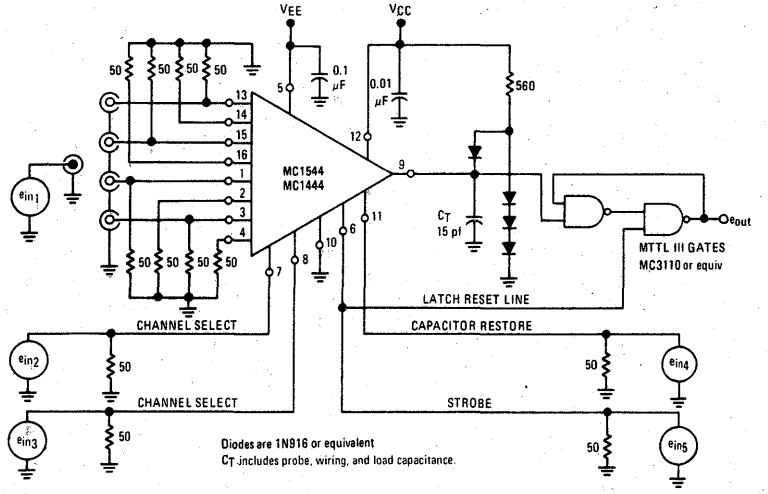
(1) T_{high} = 125°C for MC1544, 75°C for MC1444.
T_{low} = -55°C for MC1544, 0°C for MC1444.

FIGURE 3 – THRESHOLD VOLTAGE TEST CIRCUIT



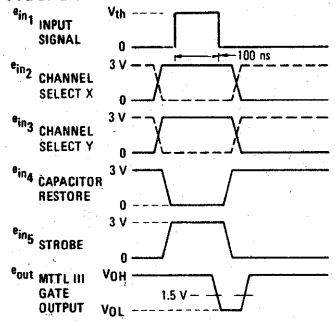
CT includes probe, wiring, and load capacitance.

FIGURE 4 – SWITCHING CHARACTERISTICS TEST CIRCUIT



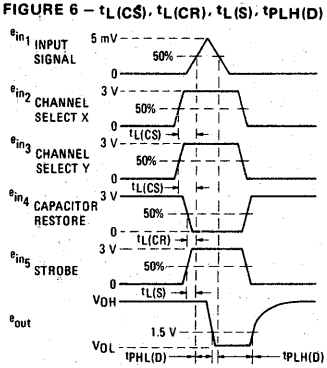
Diodes are 1N916 or equivalent
CT includes probe, wiring, and load capacitance.

FIGURE 5 – THRESHOLD VOLTAGE TEST



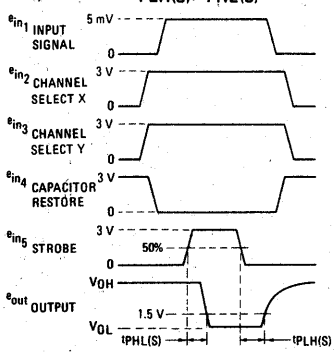
NOTE: e_{in_2} and e_{in_3} to be normal or inverted (dotted line) as necessary to select desired channel. For $e_{in_1} - e_{in_5}$ $\left.\begin{matrix}t_{TLH}\\t_{THL}\end{matrix}\right\} \leq 10$ ns

FIGURE 6 – $t_{L(CS)}$, $t_{L(CR)}$, $t_{L(S)}$, $t_{PLH(D)}$



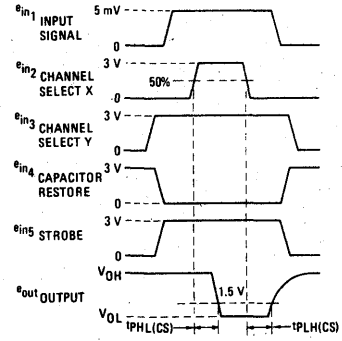
NOTE: $e_{in_2} - e_{in_5}$ $\left.\begin{matrix}t_{TLH}\\t_{THL}\end{matrix}\right\} \leq 10$ ns

FIGURE 7 – $t_{PLH(S)}$, $t_{PHL(S)}$



NOTE: $e_{in_1} - e_{in_2}$ $\left.\begin{matrix}t_{TLH}\\t_{THL}\end{matrix}\right\} \leq 10$ ns

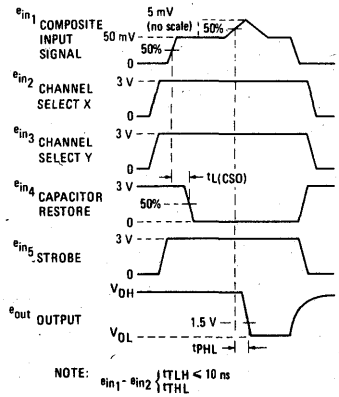
FIGURE 8 – $t_{PLH(CS)}$, $t_{PHL(CS)}$



NOTE: To test other channel select input, reverse e_{in_2} and e_{in_3}.

$e_{in_1} - e_{in_5}$ $\begin{cases} t_{TLH} \\ t_{THL} \end{cases} \leq 10$ ns

FIGURE 9 – $t_{L(CRO)}$



NOTE: $e_{in_1} - e_{in_2}$ $\begin{cases} t_{TLH} \\ t_{THL} \end{cases} \leq 10$ ns

DEFINITIONS

V_{OH}	Output Voltage – High Logic State
V_{OL}	Output Voltage – Low Logic State
$V_{IH(S)}$	The minimum high-level voltage at the strobe input which will allow normal operation during the threshold test
$V_{IL(S)}$	The maximum low-level voltage at the strobe input which will result in V_{OH} at the output regardless of input signals
V_{th}	The minimum input signal (e_{in_1}) required to drive the MTTL III gates to obtain the e_o waveform shown in Figure 5
V_{ICM+}	The maximum common-mode input voltage that will not saturate the amplifier
V_{ICM-}	The minimum common-mode input voltage that will not break down the amplifier
$V_{IH(CR)}$	The minimum high-level voltage at the capacitor restore input required to insure that the capacitors are clamped i.e., the input threshold voltage is greater than 10 mV
$V_{IL(CR)}$	The maximum low-level voltage at the capacitor restore input which will allow normal operation during the threshold test
$V_{IH(CS)}$	The minimum high-level voltage at a channel select input required to insure that the total of the base currents of all unselected inputs is less than 1.0 μA
$V_{IL(CS)}$	The maximum low-level voltage at a channel select input required to insure that the total of the base currents of all unselected inputs is less than 1.0 μA
V_{ID}	The maximum differential-mode input voltage that will not saturate the amplifier
I_{OH}	Output Source Current – High Logic State
I_{OL}	Output Sink Current - Low Logic State
$I_{IH(S)}$	The current into the strobe input when the input is at a high-level of 3.5 volts
$I_{IL(S)}$	The current into the strobe input when the input is at a low-level of 0 volts
$t_{CMR\pm}$	The minimum time between the 50% level of the trailing edge of a + or - 2 volt common-mode signal (t_{TLH}, $t_{THL} \leq 15$ ns) and the 50% level of the leading edge of a 5 mV input pulse when the capacitor restore and strobe inputs are used in a normal manner as shown in Figure 22
$t_{L(CRO)}$	The minimum time between the 50% level of the leading edge of a 50 mV input offset signal and the 50% level of the leading edge of the capacitor restore pulse as shown in Figure 9
$t_{L(CR)}$	The minimum time between the 50% level of the leading edge of the capacitor restore signal and the 50% level of the leading edge of a 5 mV input signal as shown in Figure 6
$t_{L(CS)}$	The minimum time between the 50% level of the leading edge of the channel select and the 50% level of the leading edge of a 5 mV input signal as shown in Figure 6
$t_{PLH(CS)}$	The delay time from the 50% level of the trailing edge of the channel select signal to the 1.5 volt level of the positive edge of the output when the input to the selected channel is held at the "1" level as shown in Figure 8
$t_{PHL(CS)}$	The delay time from the 50% level of the leading edge of the channel select signal to the 1.5 volt level of the negative edge of the output when the input to the selected channel is held at the "1" level as shown in Figure 8
$t_{DMR\pm}$	The minimum time between the 50% level of the trailing edge of a + or - 1 volt differential-mode signal (t_{TLH}, $t_{THL} \leq 15$ ns) and the 50% level of the leading edge of a 5 mV input pulse when the capacitor restore and strobe inputs are used in a normal manner as shown in Figure 23
$t_{PLH(D)}$	The delay time from the 50% level of the trailing edge of a 5 mV input signal to the 1.5 volt level of the positive edge of the output as shown in Figure 6
$t_{PHL(D)}$	The delay time from the 50% level of the leading edge of a 5 mV input signal to the 1.5 volt level of the negative edge of the output as shown in Figure 6
$t_{L(S)}$	The minimum time between the 50% level of the leading edge of the strobe and the 50% level of the leading edge of the input signal as shown in Figure 6
$t_{PLH(S)}$	The delay time from the 50% level of the trailing edge of the strobe to the 1.5 volt level of the positive edge of the output when the input is held at the High Logic Level as shown in Figure 7
$t_{PHL(S)}$	The delay time from the 50% level of the leading edge of the strobe to the 1.5 volt level of the negative edge of the output when the input is held at the High Logic Level as shown in Figure 7
$I_{IH(CS)}$	The current into the channel select input when the input is at a high-level of 3.5 volts
$I_{IH(CR)}$	The current out of the capacitor restore input when the input is at a low-level of 0 volts
$I_{IL(CS)}$	The input current to a channel select input when that input is at a high-level of 3.5 volts
$I_{IL(CR)}$	The current into a channel select input when the input is at a low-level of 0 volts

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

FIGURE 10 – THRESHOLD VOLTAGE versus TEMPERATURE

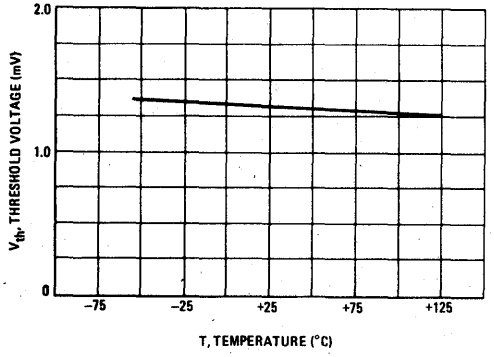


FIGURE 11 – THRESHOLD VOLTAGE versus POWER SUPPLIES

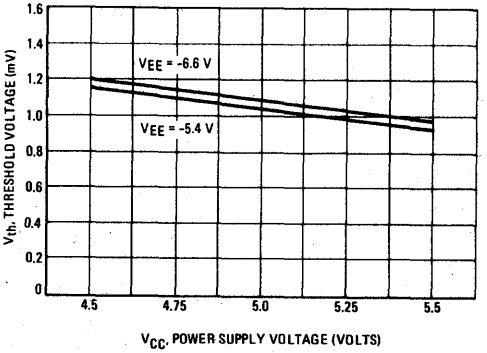


FIGURE 12 – THRESHOLD versus INPUT OFFSET VOLTAGE

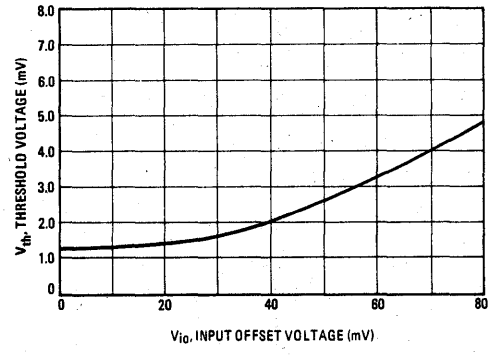


FIGURE 13 – THRESHOLD VOLTAGE versus PULSE WIDTH

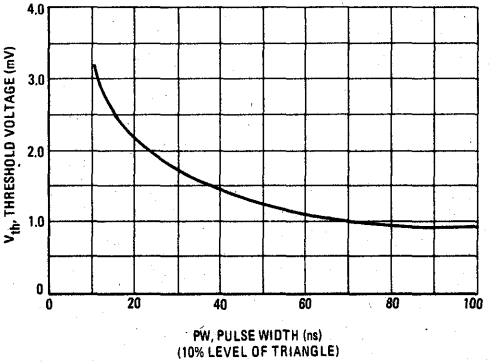


FIGURE 14 – OUTPUT VOLTAGE versus CURRENT and TEMPERATURE

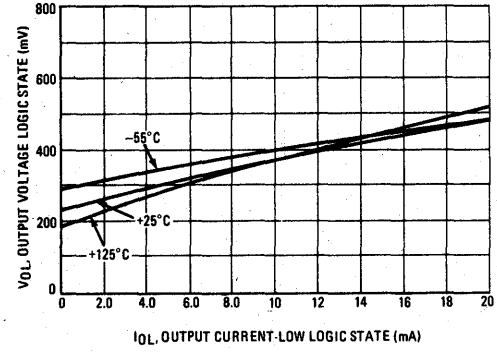
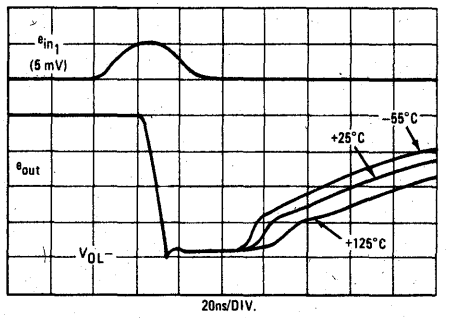


FIGURE 15 – SENSE AMPLIFIER RESPONSE versus TEMPERATURE (See Figure 3 and 6)



TYPICAL CHARACTERISTICS (continued)

FIGURE 16 – INPUT IMPEDANCE versus FREQUENCY

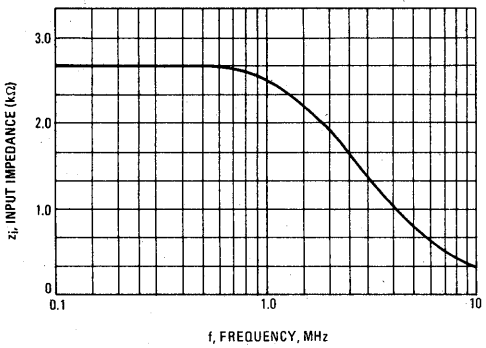


FIGURE 17 – CAPACITOR RESTORE TIME versus INPUT OFFSET VOLTAGE

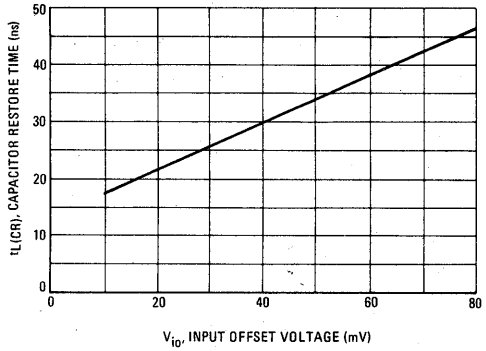


FIGURE 18 – AMPLIFIER INPUT TO OUTPUT TRANSFER CHARACTERISTIC

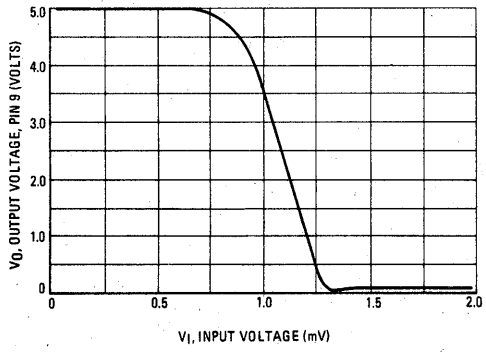


FIGURE 19 – STROBE TO OUTPUT TRANSFER CHARACTERISTICS

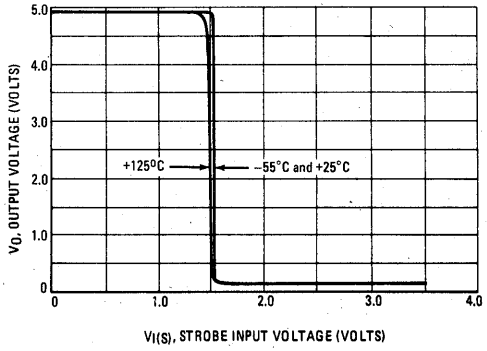


FIGURE 20 – CHANNEL SELECT X to OUTPUT TRANSFER CHARACTERISTICS

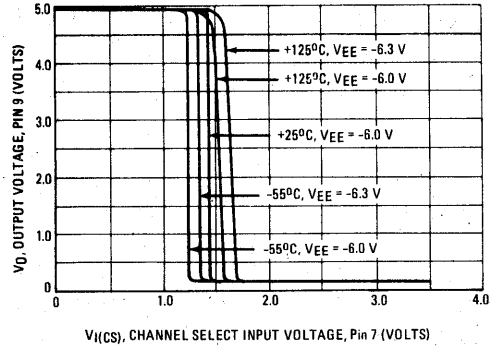


FIGURE 21 – CHANNEL SELECT Y to OUTPUT TRANSFER CHARACTERISTICS

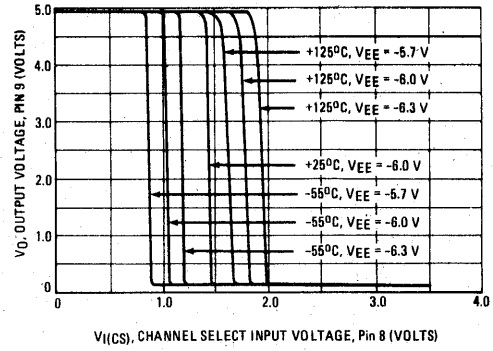


FIGURE 22 – COMMON-MODE CHARACTERISTICS

Note: The 5mV Input Signal (Differential) is superimposed on the Common-Mode Input and is shown separately for reference only.

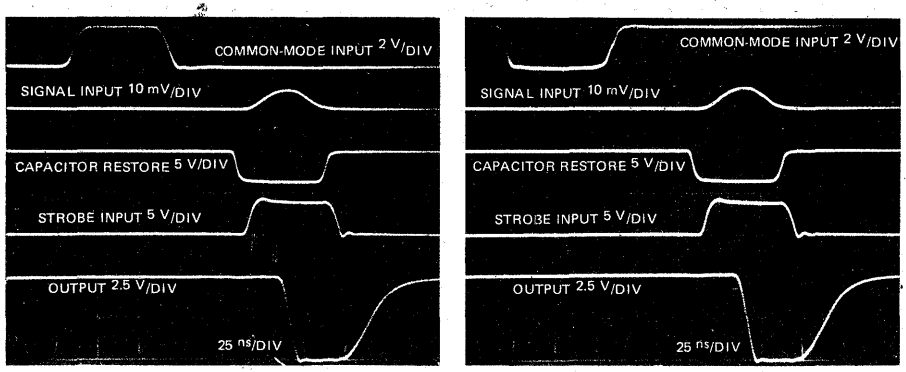
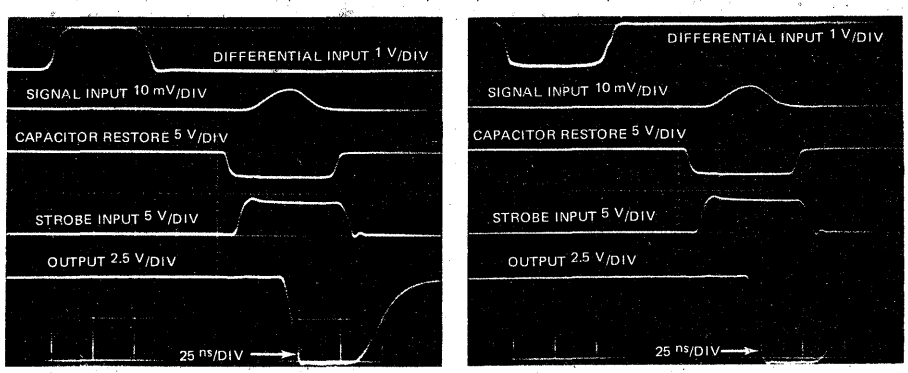


FIGURE 23 – DIFFERENTIAL-MODE CHARACTERISTICS

Note: The 5mV Input Signal is superimposed on the Differential Input and is shown separately for reference only.



5

MC1472

Product Preview

DUAL PERIPHERAL-HIGH-VOLTAGE POSITIVE "NAND" DRIVER*

The dual driver consists of a pair of PNP-buffered Schottky AND gates connected to the bases of a pair of high-voltage NPN transistors. They are similar to the MC75452 drivers but with the added advantages of: 1) 70 Volt capability 2) output suppression diodes and 3) PNP buffered inputs for MOS compatibility. These features make the MC1472 ideal for mating MOS logic or microprocessors to lamps, relays, printer hammers and incandescent displays.

- 300 mA Output Capability (each transistor)
- 70 Vdc Breakdown Voltage
- Internal Output Clamp Diode
- Low Input Loading for MOS Compatibility (PNP buffered)

CROSS REFERENCE
UDN-5712 – SN75475 – MC1472

MAXIMUM RATINGS (T_A = 25°C, Note 1).

Rating	Value	Unit
Supply Voltage	7.0	Volts
Input Voltage	5.5	Volts
Output Voltage	80	Volts
Clamp Voltage	80	Volts
Output Current (Continuous)	300	mA
Operating Junction Temperature Ceramic Package Plastic Package	 +175 +150	°C
Storage Temperature Range	-65 to +150	°C

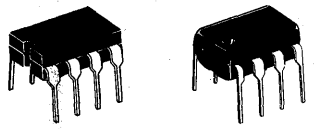
Note 1: "Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	Volts
Operating Ambient Temperature	T_A	0	70	°C
Output Voltage	V_O	V_{CC}	70	Volts
Clamp Voltage	V_C	V_O	70	Volts

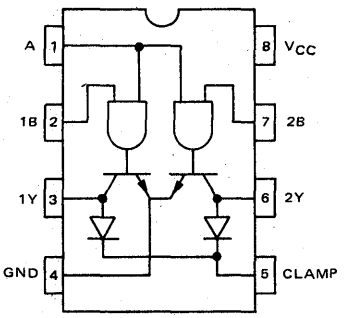
This is advance information and specifications are subject to change without notice.

DUAL PERIPHERAL POSITIVE "NAND" DRIVER
MONOLITHIC SILICON INTEGRATED CIRCUITS



U SUFFIX
CERAMIC PACKAGE
CASE 693

P1 SUFFIX
PLASTIC PACKAGE
CASE 626



Positive Logic: Y=AB*

TRUTH TABLE

A	B	Y
L	L	H ("OFF" STATE)
L	H	H ("OFF" STATE)
H	L	H ("OFF" STATE)
H	H	L ("ON" STATE)

H = Logic One
L = Logic Zero

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1472U	–	0 to +70°C	Ceramic DIP
MC1472P1	–	0 to +70°C	Plastic DIP

ELECTRICAL CHARACTERISTICS Unless otherwise noted min/max limits apply accross the 0°C to 70°C temperature range with 4.5 V ± V_{CC} ± 5.5 V. All typical values are for T_A = 25°C, V_{CC} = 5 Volts.

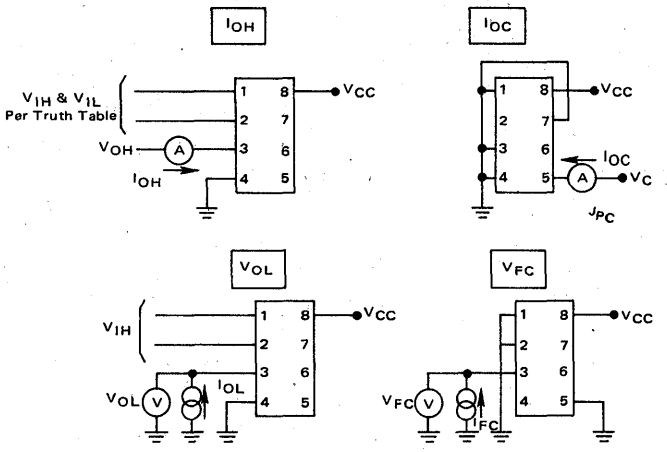
Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – High Logic State	V_{IH}	2.0	–	5.5	Vdc
Input Voltage – Low Logic State	V_{IL}	0	–	0.8	Vdc
Input Current – Low Logic State (V_{IL} = 0.4V) A Input B Input	I_{IL}	–	–	 -0.3 -0.15	mA
Input Current – High Logic State (V_{IH} = 2.4V) A input B Input (V_{IH} = 5.5V) A Input B Input	I_{IH}	 – – – –	 – – – –	 40 20 200 100	 µA
Input Clamp Voltage (I_{IC} = -12mA)	V_{IC}	–	–	-1.5	V
Output Leakage Current – High Logic State (V_O = 70V, See test Figure)	I_{OH}	–	–	100	µA
Output Voltage – Low Logic State (I_{OL} = 100 mA) (I_{OL} = 300 mA)	V_{OL}	– –	– –	0.4 0.7	V
Output Clamp Diode Leakage Current (V_C = 70V, See test Figure)	I_{OC}	–	–	100	µA
Output Clamp Forward Voltage (I_{FC} = 300 mA See test Figure)	V_{FC}	–	–	1.7	V
Power Supply Current (All Inputs at V_{IH}) (All Inputs at V_{IL})	I_{CC}	– –	– –	15 70	mA

NOTE: All currents into device pins are shown as positive, out of device pins as negative. All voltages referenced to ground unless otherwise noted.

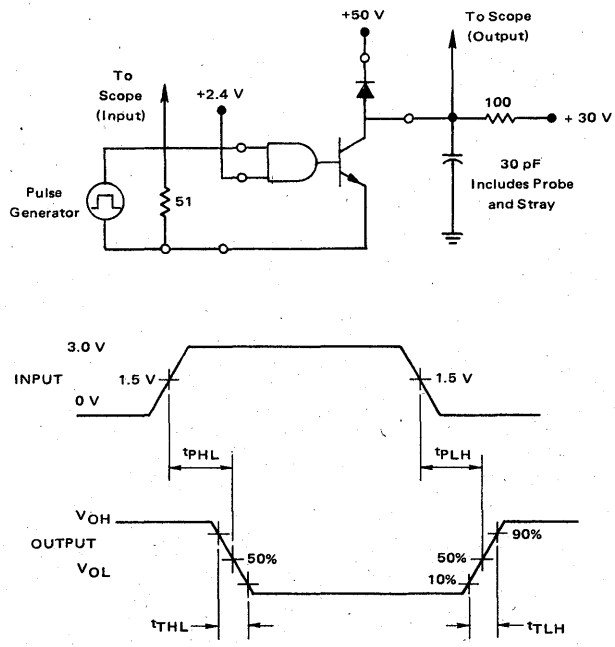
SWITCHING CHARACTERISTICS V_{CC} = 5.0V, T_A = 25°C

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time Output High to Low Output Low to High	 t_{PHL} t_{PLH}	 – –	 – –	 1.0 0.75	µs
Output Transition Time Output High to Low Output Low to High	 t_{THL} t_{TLH}	 – –	 – –	 0.1 0.1	µs

TEST CIRCUITS



SWITCHING TEST CIRCUIT AND WAVEFORM



ORDERING INFORMATION

Device	Temperature Range	Package
MC1488L	0°C to +75°C	Ceramic DIP

MC1488

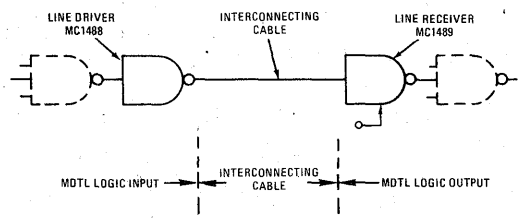
QUAD LINE DRIVER

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

Features:

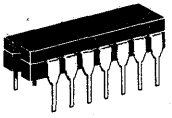
- Current Limited Output
  ±10 mA typ
- Power-Off Source Impedance
  300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola MDTL and MTTL Logic Families

TYPICAL APPLICATION

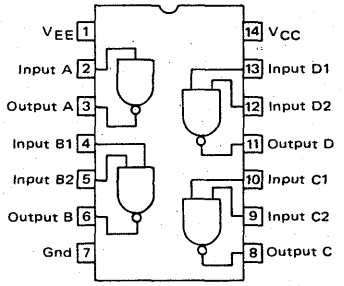


QUAD MDTL LINE DRIVER
RS-232C
SILICON MONOLITHIC
INTEGRATED CIRCUIT

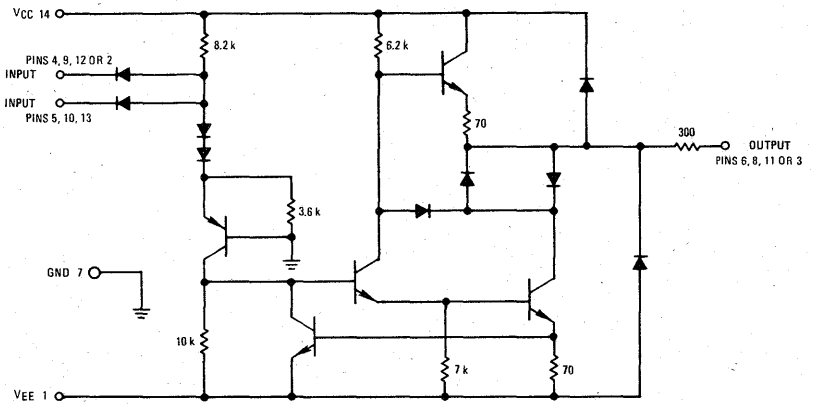
L Suffix
CERAMIC PACKAGE
CASE 632
TO-116



PIN CONNECTIONS



CIRCUIT SCHEMATIC
(1/4 OF CIRCUIT SHOWN)



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+15 -15	Vdc
Input Voltage Range	V_{IR}	$-15 \leq V_{IR} \leq 7.0$	Vdc
Output Signal Voltage	V_O	±15	Vdc
Power Derating (Package Limitation, Ceramic and Plastic Dual-In-Line Package) Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +9.0 ± 1% Vdc, V_{EE} = -9.0 ± 1% Vdc, T_A = 0 to +75°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Current — Low Logic State (V_{IL} = 0)	1	I_{IL}	–	1.0	1.6	mA
Input Current — High Logic State (V_{IH} = 5.0 V)	1	I_{IH}	–	–	10	µA
Output Voltage — High Logic State	2	V_{OH}				Vdc
(V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = -9.0 Vdc)			+6.0	+7.0	–	
(V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = -13.2 Vdc)			+9.0	+10.5	–	
Output Voltage — Low Logic State	2	V_{OL}				Vdc
(V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = -9.0 Vdc)			-6.0	-7.0	–	
(V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = -13.2 Vdc)			-9.0	-10.5	–	
Positive Output Short-Circuit Current (1)	3	I_{OS+}	+6.0	+10	+12	mA
Negative Output Short-Circuit Current (1)	3	I_{OS-}	-6.0	-10	-12	mA
Output Resistance (V_{CC} = V_{EE} = 0, $\lvert V_O \rvert$ = ±2.0 V)	4	r_o	300	–	–	Ohms
Positive Supply Current (R_l = ∞)	5	I_{CC}				mA
(V_{IH} = 1.9 Vdc, V_{CC} = +9.0 Vdc)			–	+15	+20	
(V_{IL} = 0.8 Vdc, V_{CC} = +9.0 Vdc)			–	+4.5	+6.0	
(V_{IH} = 1.9 Vdc, V_{CC} = +12 Vdc)			–	+19	+25	
(V_{IL} = 0.8 Vdc, V_{CC} = +12 Vdc)			–	+5.5	+7.0	
(V_{IH} = 1.9 Vdc, V_{CC} = +15 Vdc)			–	–	+34	
(V_{IL} = 0.8 Vdc, V_{CC} = +15 Vdc)			–	–	+12	
Negative Supply Current (R_L = ∞)	5	I_{EE}				
(V_{IH} = 1.9 Vdc, V_{EE} = -9.0 Vdc)			–	-13	-17	mA
(V_{IL} = 0.8 Vdc, V_{EE} = -9.0 Vdc)			–	–	-15	µA
(V_{IH} = 1.9 Vdc, V_{EE} = -12 Vdc)			–	-18	-23	mA
(V_{IL} = 0.8 Vdc, V_{EE} = -12 Vdc)			–	–	-15	µA
(V_{IH} = 1.9 Vdc, V_{EE} = -15 Vdc)			–	–	-34	mA
(V_{IL} = 0.8 Vdc, V_{EE} = -15 Vdc)			–	–	-2.5	mA
Power Consumption		P_C				mW
(V_{CC} = 9.0 Vdc, V_{EE} = -9.0 Vdc)			–	–	333	
(V_{CC} = 12 Vdc, V_{EE} = -12 Vdc)			–	–	576	

SWITCHING CHARACTERISTICS (V_{CC} = +9.0 ± 1% Vdc, V_{EE} = -9.0 ± 1% Vdc, T_A = +25°C.)

Propagation Delay Time (z_l = 3.0 k and 15 pF)	6	t_{PLH}	–	275	350	ns
Fall Time (z_l = 3.0 k and 15 pF)	6	t_{THL}	–	45	75	ns
Propagation Delay Time (z_l = 3.0 k and 15 pF)	6	t_{PHL}	–	110	175	ns
Rise Time (z_l = 3.0 k and 15 pF)	6	t_{TLH}	–	55	100	ns

(1) Maximum Package Power Dissipation may be exceeded if all outputs are shorted simultaneously.

CHARACTERISTIC DEFINITIONS

FIGURE 1 – INPUT CURRENT

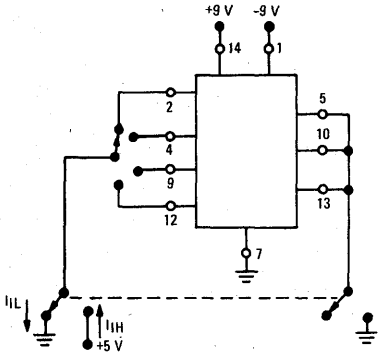


FIGURE 2 – OUTPUT VOLTAGE

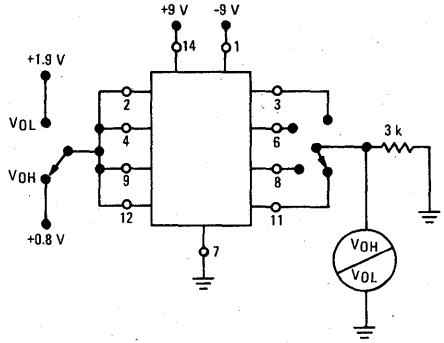


FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

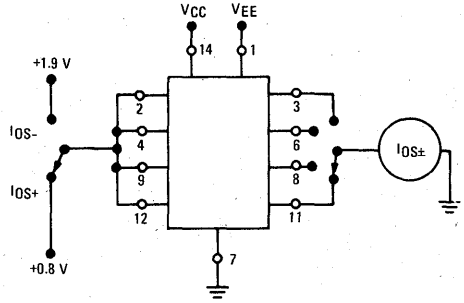


FIGURE 4 – OUTPUT RESISTANCE (POWER-OFF)

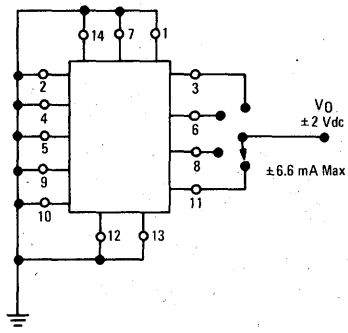


FIGURE 5 – POWER-SUPPLY CURRENTS

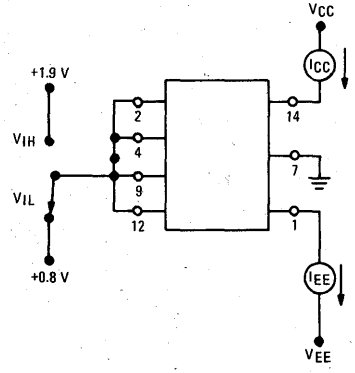
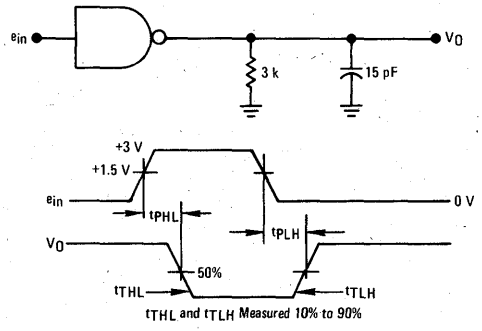


FIGURE 6 – SWITCHING RESPONSE



TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 7 – TRANSFER CHARACTERISTICS versus POWER-SUPPLY VOLTAGE

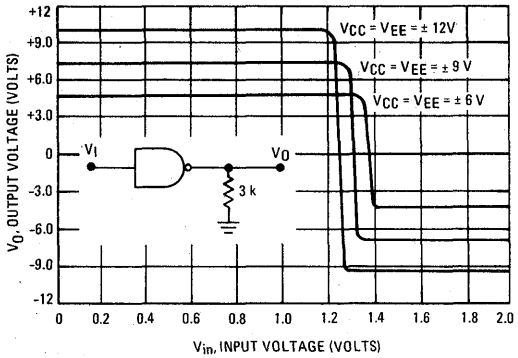


FIGURE 8 – SHORT-CIRCUIT OUTPUT CURRENT versus TEMPERATURE

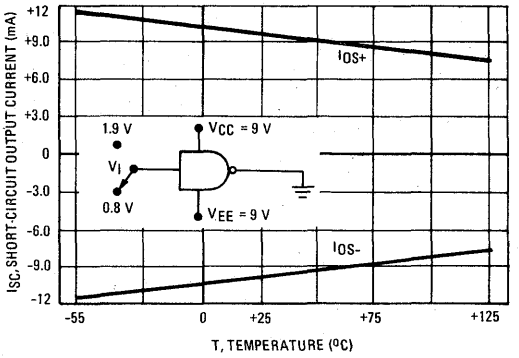


FIGURE 9 – OUTPUT SLEW RATE versus LOAD CAPACITANCE

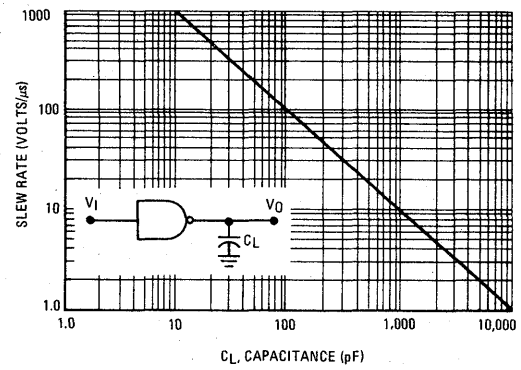


FIGURE 10 – OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS

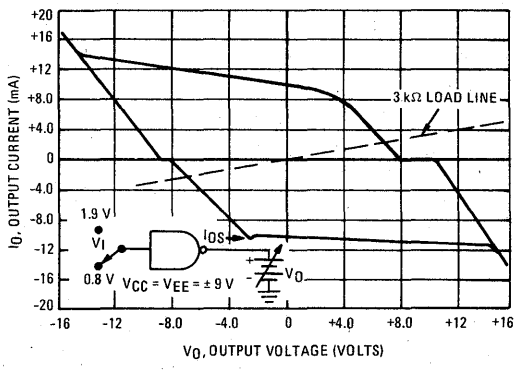
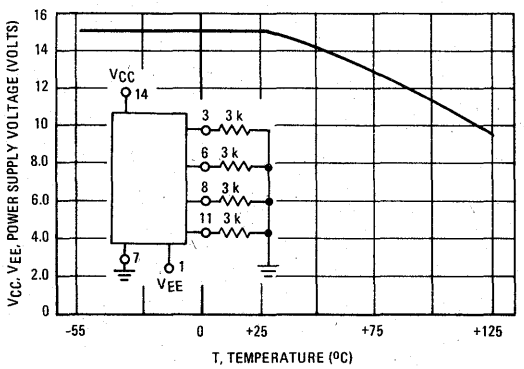


FIGURE 11 – MAXIMUM OPERATING TEMPERATURE versus POWER-SUPPLY VOLTAGE



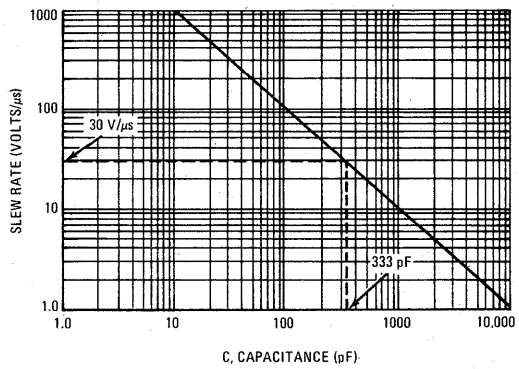
APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) has released the RS232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

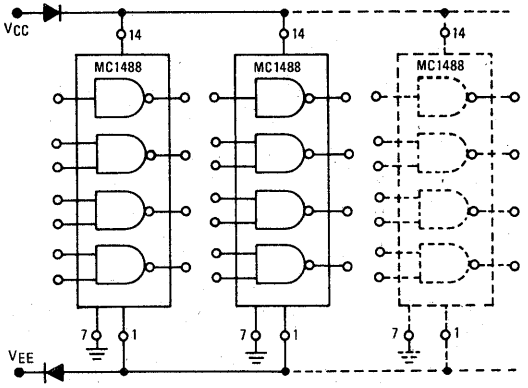
The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330-pF capacitor on each output will guarantee a worst case slew rate of 30 volts per microsecond.

FIGURE 12 – SLEW RATE versus CAPACITANCE FOR I_{SC} = 10 mA



The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15-volt, 500-mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V_{CC} \geq 9.0$ V; $V_{EE} \leq -9.0$ V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300-ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±25-volt limits specified in the earlier Standard RS232B.) The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 volts stated above.

FIGURE 13 – POWER-SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS



The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting – this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488 used as a DTL to MOS translator where the high-level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power-Supply Range – as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately -2.5 volts to the minimum specified -15 volts. The MC1488 will drive the output to within 2 volts of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving RS232C lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.

FIGURE 14 – MDTL/MTTL-TO-MOS TRANSLATOR

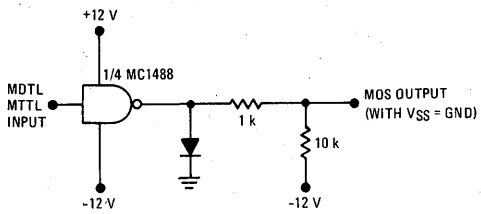
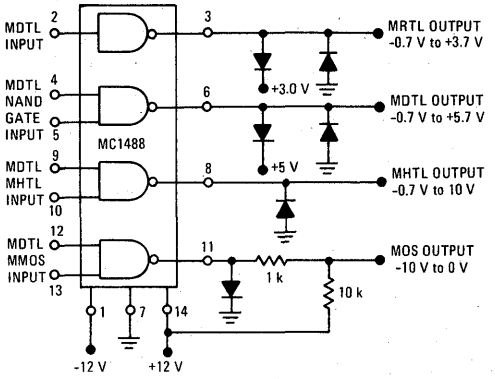


FIGURE 15 – LOGIC TRANSLATOR APPLICATIONS



5

ORDERING INFORMATION

Device	Temperature Range	Package
MC1489L	0°C to +75°C	Ceramic DIP
MC1489AL	0°C to +75°C	Ceramic DIP

MC1489L
MC1489AL

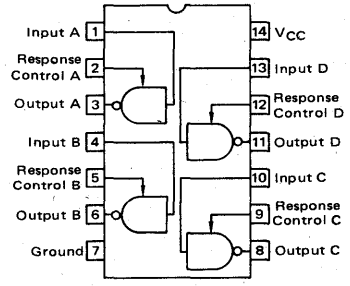
QUAD LINE RECEIVERS

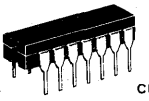
The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

- Input Resistance – 3.0 k to 7.0 kilohms
- Input Signal Range – ±30 Volts
- Input Threshold Hysteresis Built In
- Response Control
  a) Logic Threshold Shifting
  b) Input Noise Filtering

QUAD MDTL LINE RECEIVERS RS-232C

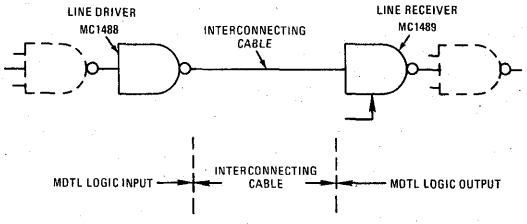
SILICON MONOLITHIC INTEGRATED CIRCUIT



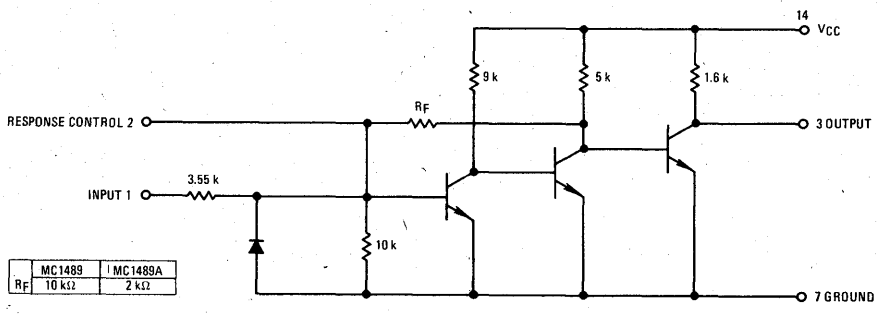


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

TYPICAL APPLICATION



CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



	MC1489	MC1489A
RF	10 kΩ	2 kΩ

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Input Voltage Range	V_{IR}	±30	Vdc
Output Load Current	I_L	20	mA
Power Dissipation (Package Limitation, Ceramic and Plastic Dual In-Line Package) Derate above T_A = +25°C	P_D $1/\theta_{JA}$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +175	°C

5

ELECTRICAL CHARACTERISTICS (Response control pin is open.) (V_{CC} = +5.0 Vdc ±1%, T_A = 0 to +75°C unless otherwise noted)

Characteristics		Figure	Symbol	Min	Typ	Max	Unit
Positive Input Current	(V_{IH} = +25 Vdc) (V_{IH} = +3.0 Vdc)	1	I_{IH}	3.6 0.43	– –	8.3 –	mA
Negative Input Current	(V_{IL} = -25 Vdc) (V_{IL} = -3.0 Vdc)	1	I_{IL}	-3.6 -0.43	– –	-8.3 –	mA
Input Turn-On Threshold Voltage (T_A = +25°C, $V_{OL} \leq$ 0.45 V)	MC1489 MC1489A	2	V_{IHL}	1.0 1.75	– 1.95	1.5 2.25	Vdc
Input Turn-Off Threshold Voltage (T_A = +25°C, $V_{OH} \geq$ 2.5 V, I_L = -0.5 mA)	MC1489 MC1489A	2	V_{ILH}	0.75 0.75	– 0.8	1.25 1.25	Vdc
Output Voltage High	(V_{IH} = 0.75 V, I_L = -0.5 mA) (Input Open Circuit, I_L = -0.5 mA)	2	V_{OH}	2.6 2.6	4.0 4.0	5.0 5.0	Vdc
Output Voltage Low	(V_{IL} = 3.0 V, I_L = 10 mA)	2	V_{OL}	–	0.2	0.45	Vdc
Output Short-Circuit Current		3	I_{OS}	–	3.0	–	mA
Power Supply Current	(V_{IH}= +5.0 Vdc)	4	I_{CC}	–	20	26	mA
Power Consumption	(V_{IH}= +5.0 Vdc)	4	P_C	–	100	130	mW

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 1%, T_A = +25°C)

Propagation Delay Time	(R_L = 3.9 kΩ)	5	t_{PLH}	–	25	85	ns
Rise Time	(R_L = 3.9 kΩ)	5	t_{TLH}	–	120	175	ns
Propagation Delay Time	(R_L = 390 Ω)	5	t_{PHL}	–	25	50	ns
Fall Time	(R_L = 390 Ω)	5	t_{THL}	–	10	20	ns

TEST CIRCUITS

FIGURE 1 – INPUT CURRENT

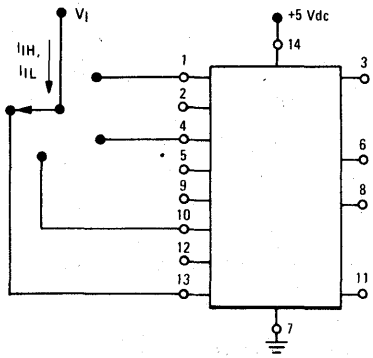


FIGURE 2 – OUTPUT VOLTAGE and INPUT THRESHOLD VOLTAGE

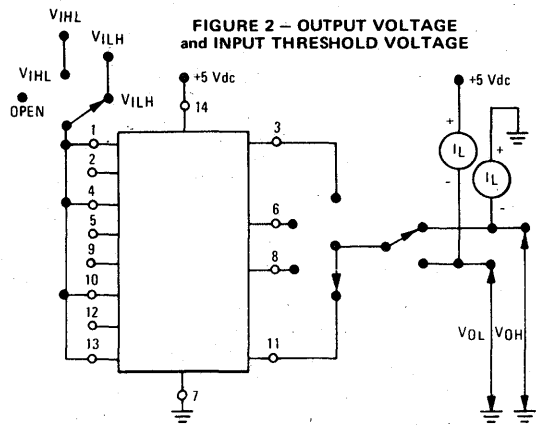


FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

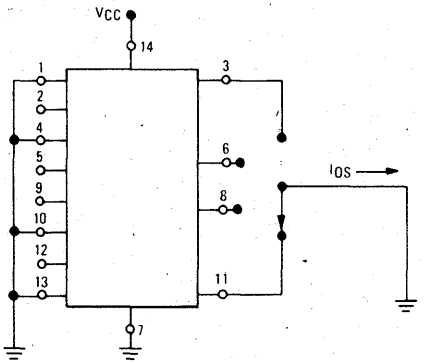


FIGURE 4 – POWER-SUPPLY CURRENT

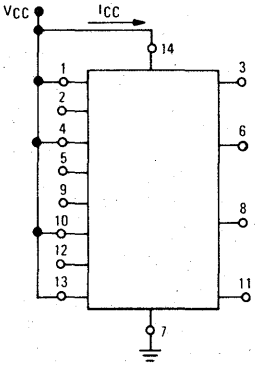
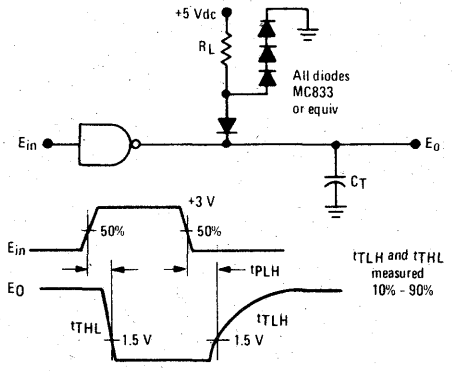
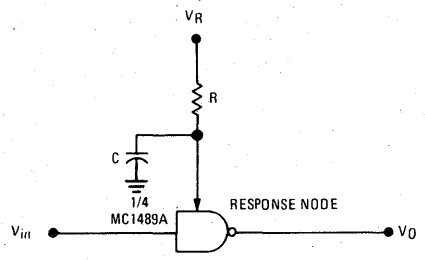


FIGURE 5 – SWITCHING RESPONSE



CT = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances

FIGURE 6 – RESPONSE CONTROL NODE



C, capacitor is for noise filtering.
R, resistor is for threshold shifting.

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TYPICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 7 – INPUT CURRENT

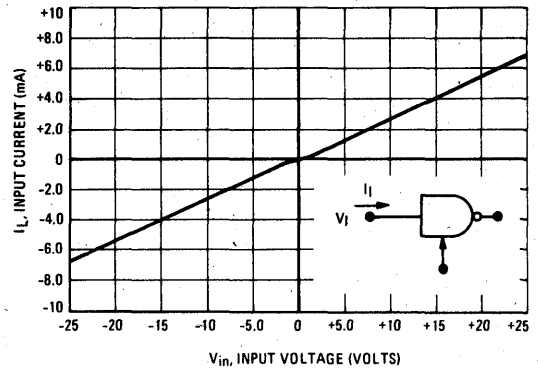


FIGURE 8 – MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

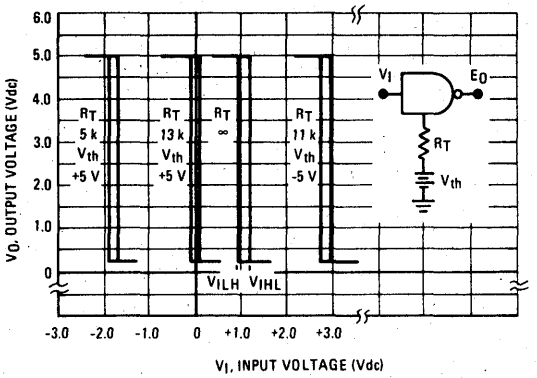


FIGURE 9 – MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

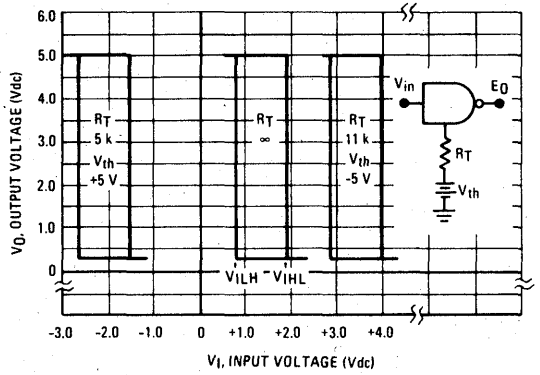


FIGURE 10 – INPUT THRESHOLD VOLTAGE versus TEMPERATURE

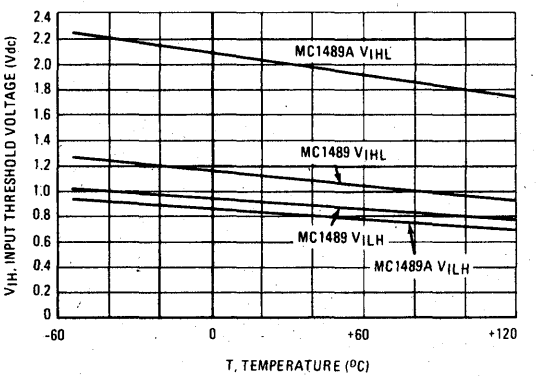
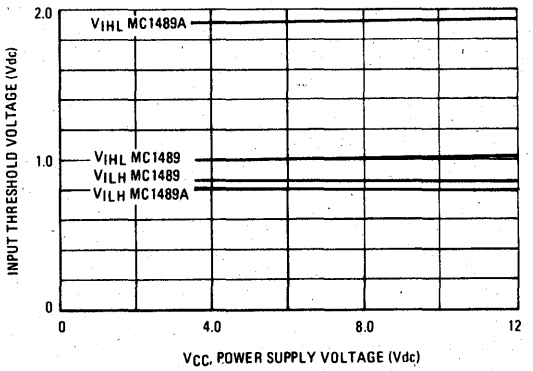


FIGURE 11 – INPUT THRESHOLD versus POWER-SUPPLY VOLTAGE



APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE} (Ref. Sect. 2.4).

The receiver shall detect a voltage between -3.0 and -25 volts as a logic "1" and inputs between +3.0 and +25 volts as a logic "0" (Ref. Sect. 2.3). On some interchange leads, an open circuit or power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or logic "1" (Ref. Sect. 2.5). For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 volts and turn-off of 1.0 volt for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 volts and turn-off of 0.8 volt for typically 1.15 volts of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power-supply. Figures 6, 8 and 9 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high-energy noise pulses. Figures 12 and 13 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 14)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 15 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

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FIGURE 12 – TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

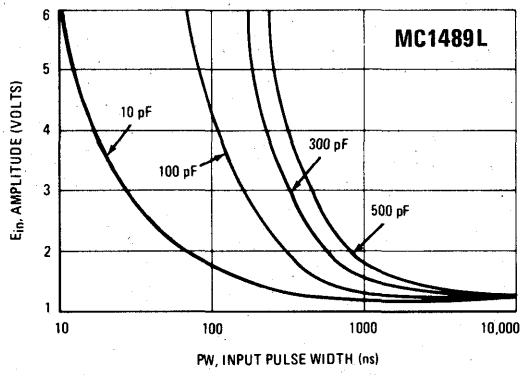
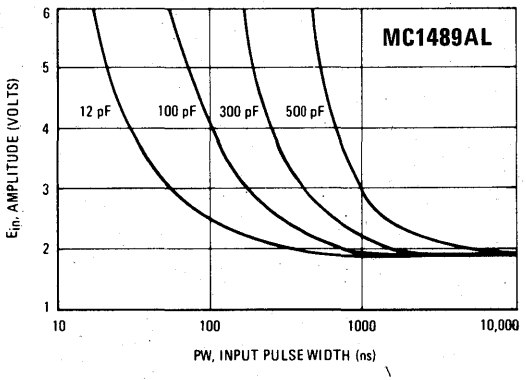


FIGURE 13 – TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND



APPLICATIONS INFORMATION (continued)

FIGURE 14 – TYPICAL TRANSLATOR APPLICATION – MOS TO DTL OR TTL

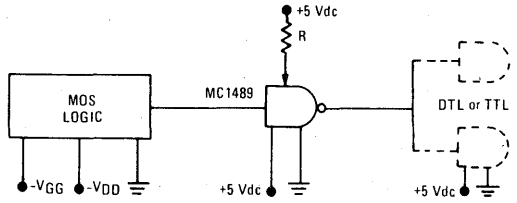
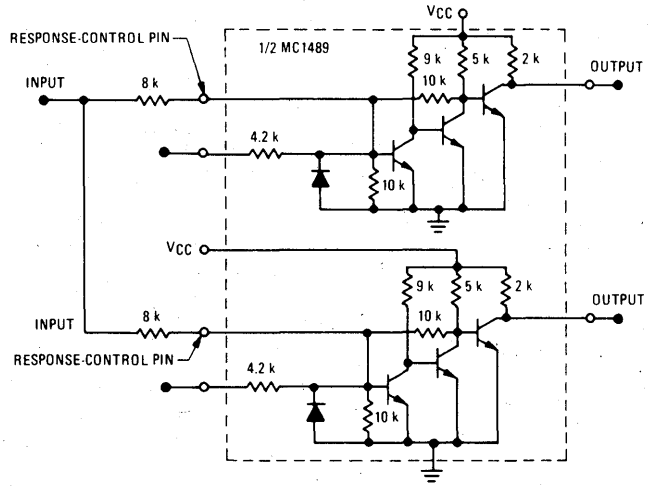


FIGURE 15 – TYPICAL PARALLELING OF TWO MC1489,A RECEIVERS TO MEET RS-232C



5

XC26S10
XC26S11

Product Preview

QUAD OPEN-COLLECTOR BUS TRANSCEIVERS

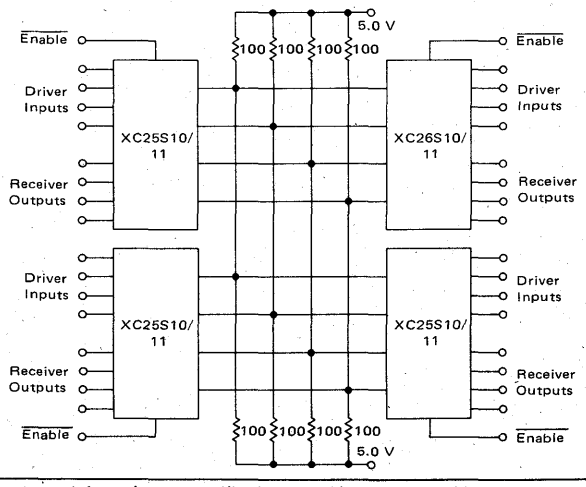
These quad transceivers are designed to mate Schottky TTL or NMOS logic to a low impedance bus. The $\overline{\text{Enable}}$ and Driver inputs are PNP buffered to ensure low input loading. The Driver (Bus) output is open-collector and can sink up to 100 mA at 0.8 V, thus the bus can drive impedances as low as 100 Ω. The receiver output is active pull-up and can drive ten Schottky TTL loads.

An active-low $\overline{\text{Enable}}$ controls all four drivers allowing the outputs of different device drivers to be connected together for party-line operation. The line can be terminated at both ends and still give considerable noise margin at the receiver. Typical receiver threshold is 2.0 V.

Advanced Schottky processing is utilized to assure fast propagation delay times. Two ground pins are provided to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both ground pins should be tied to the ground bus external to the package.

- Driver Can Sink 100 mA at 0.8 V (Max)
- PNP Inputs for Low-Logic Loading
- Typical Driver Delay = 10 ns
- Typical Receiver Delay = 10 ns
- Schottky Processing for High Speed
- Inverting Driver – XC26S10
  Non-Inverting – XC26S11

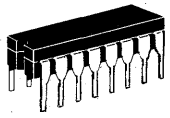
TYPICAL APPLICATION



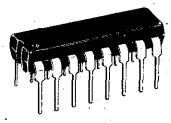
This is advance information and specifications are subject to change without notice.

QUAD OPEN-COLLECTOR BUS TRANSCEIVERS

SCHOTTKY
SILICON MONOLITHIC
INTEGRATED CIRCUIT

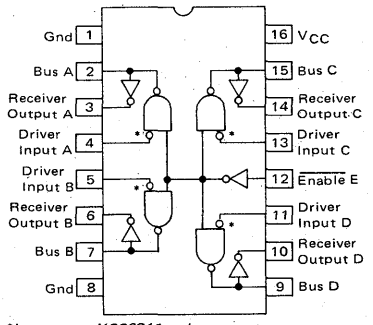


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



*Inverter on XC26S11 only.

TRUTH TABLE

Enable	Driver Input	Bus 26S10	Bus 26S11	Receiver Output
L	L	H	L	L
L	H	L	H	H
H	X	Y	Y	Y

L = Low Logic State
H = High Logic State
X = Irrelevant
Y = Assumes condition controlled by other elements on the bus

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MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	Vdc
Input Voltage	V_I	-0.5 to +5.5	Vdc
Input Current	I_I	-3.0 to +5.0	mA
Output Voltage — High Impedance State	$V_{O\ (Hi\text{-}z)}$	-0.5 to V_{CC}	V
Output Current—Bus	$I_{O(B)}$	200	mA
Output Current—Receiver	$I_{O(R)}$	30	mA
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

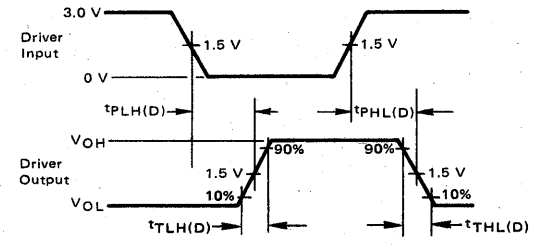
ELECTRICAL CHARACTERISTICS (Unless otherwise noted V_{CC} = 4.75 to 5.25 V and T_A = 0 to +70°C. Typical values measured at V_{CC} = 5.0 V and T_A = 25°C.)

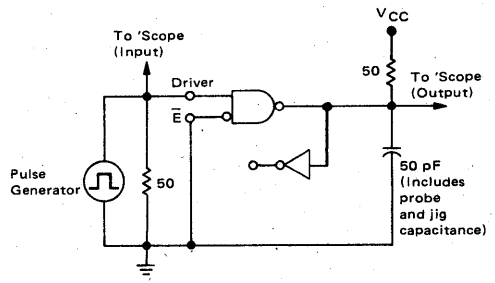
Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State (Driver and $\overline{\text{Enable}}$ Inputs)	V_{IL}	—	—	0.8	V
Input Voltage — High Logic State (Driver and $\overline{\text{Enable}}$ Inputs)	V_{IH}	2.0	—	—	V
Input Clamp Voltage (Driver and Enable Inputs) (I_{IC} = -18 mA)	V_{IC}	—	—	-1.2	V
Input Current — Low Logic State (V_{IL} = 0.4 V) ($\overline{\text{Enable}}$ Input) (Driver Inputs)	I_{IL}	 — —	 — —	 -0.36 -0.54	mA
Input Current — High Logic State (V_{IH} = 2.7 V) ($\overline{\text{Enable}}$ Input) (Driver Inputs)	I_{IH}	 — —	 — —	 20 30	μA
Input Current — Maximum Voltage (V_{IH1} = 5.5 V) ($\overline{\text{Enable}}$ or Driver Inputs)	I_{IH1}	—	—	100	μA
Driver Output Voltage — Low Logic State (I_{OL} = 40 mA) (I_{OL} = 70 mA) (I_{OL} = 100 mA)	$V_{OL(D)}$	 — — —	 0.33 0.42 0.51	 0.5 0.7 0.8	V
Driver (Bus) Leakage Current (V_{OH} = 4.5 V) (V_{OL} = 0.8 V)	$I_{O(D)}$	 — —	 — —	 100 -50	μA
Driver (Bus) Leakage Current (V_{CC} = 0 V, V_{OH} = 4.5 V)	$I_{O1(D)}$	—	—	100	μA
Receiver Input High Threshold ($V_{IH(\overline{E})}$ = 2.4 V)	$V_{TH(R)}$	2.25	2.0	—	V
Receiver Input Low Threshold ($V_{IH(\overline{E})}$ = 2.4 V)	$V_{TL(R)}$	—	2.0	1.75	V
Receiver Output Voltage — Low Logic State (I_{OL} = 20 mA)	$V_{OL(R)}$	—	—	0.5	V
Receiver Output Voltage — High Logic State (I_{OH} = -1.0 mA)	$V_{OH(R)}$	2.7	3.4	—	V
Receiver Output Short-Circuit Current	$I_{OS(R)}$	-18	—	-60	mA
Power Supply Current — Output Low State ($V_{IL(\overline{E})}$ = 0 V) XC26S10 XC26S11	I_{CC}	 — —	 45 —	 70 80	mA

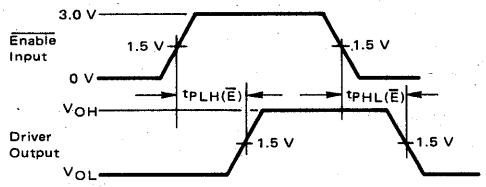
SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

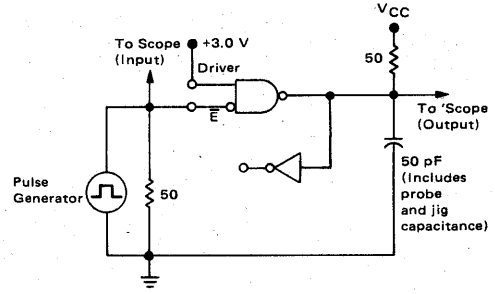
Characteristic	Symbol	XC26S10 Min	XC26S10 Typ	XC26S10 Max	XC26S11 Min	XC26S11 Typ	XC26S11 Max	Unit
Propagation Delay Time Driver Input to Output	$t_{PLH(D)}$	–	–	15	–	–	19	ns
	$t_{PHL(D)}$	–	–	15	–	–	19	
Propagation Delay Time Enable Input to Output	$t_{PLH(\overline{E})}$	–	–	18	–	–	20	ns
	$t_{PHL(\overline{E})}$	–	–	18	–		20	
Propagation Delay Time Bus to Receiver Output	$t_{PLH(R)}$	–	–	15	–	–	15	ns
	$t_{PHL(R)}$	–	–	15	–	–	15	
Rise and Fall Time of Driver Output	$t_{TLH(D)}$	4.0	–	–	4.0	–	–	ns
	$t_{THL(D)}$	2.0	–	–	2.0	–	–	

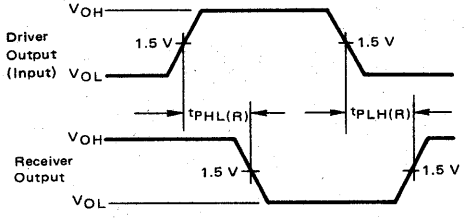
SWITCHING WAVEFORMS AND CIRCUITS

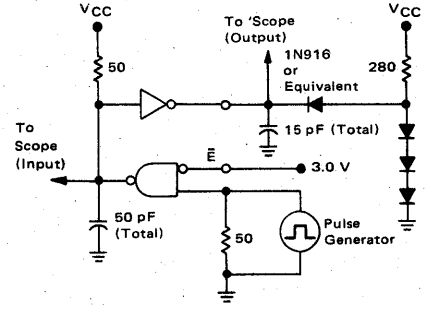












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MC3232A

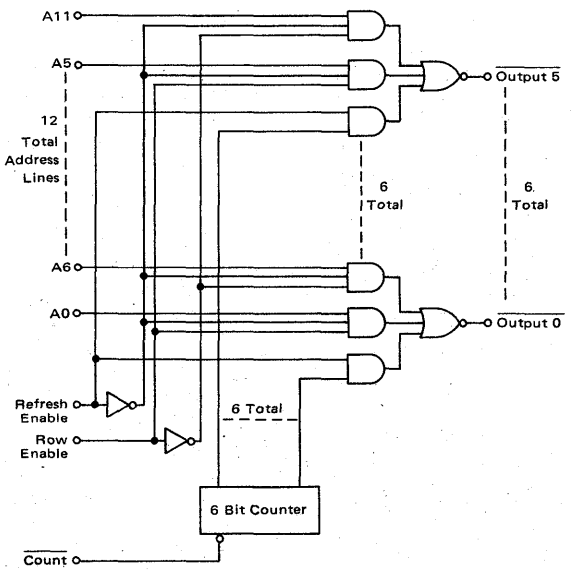
Advance Information

MEMORY ADDRESS MULTIPLEXER

The Motorola MC3232A is an address multiplexer and refresh counter for 16 pin 4K dynamic RAMs that require a 64 cycle refresh. It multiplexes twelve system address bits to the six input address pins of the memory device. The MC3232A also contains a 6 bit refresh counter that is clocked externally to generate the 64 sequential addresses required for refresh. The high performance of the MC3232A will enhance the high speed of the fast N-channel RAMs such as the MCM6604.

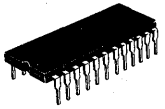
- Simplifies 16 Pin 4K Dynamic Memory Design
- Reduces Package Count
- 6 Bit Binary Counter for 64 Refresh Address
- Multiplexing: Row Address/Column Address/Refresh Address
- High Input Impedance for Minimum Loading of Bus:
  I_F = 0.25 mA Max
- Schottky TTL for High Performance Address Input to Output Delay
  t_{pd} = 20 ns @ C_L = 250 pF
- Second Source to Intel 3232
  (Detect Zero Function Not Included)

LOGIC DIAGRAM



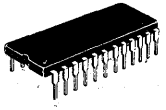
MEMORY ADDRESS MULTIPLEXER AND REFRESH ADDRESS COUNTER

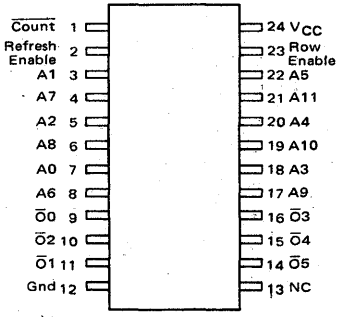
SCHOTTKY SILICON MONOLITHIC INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 623

P SUFFIX
PLASTIC PACKAGE
CASE 649





Note: A0 Through A5 Are Row Addresses
A6 Through A11 Are Column Addresses

TRUTH TABLE AND DEFINITIONS

Refresh Enable	Row Enable	Output
H	X	Refresh Address (From Internal Counter)
L	H	Row Address (A0 through A5)
L	L	Column Address (A6 through A11)

$\overline{\text{Count}}$ – Advances Internal Refresh Counter

ORDERING INFORMATION

Device	Temperature Range	Package
MC3232AL	0 to 75°C	Ceramic DIP
MC3232AP	0 to 75°C	Plastic DIP

This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_I	-0.5 to +7.0	V
Output Voltage	V_O	-0.5 to +7.0	V
Output Current	I_O	100	mA
Operating Ambient Temperature	T_A	0 to +75	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	°C

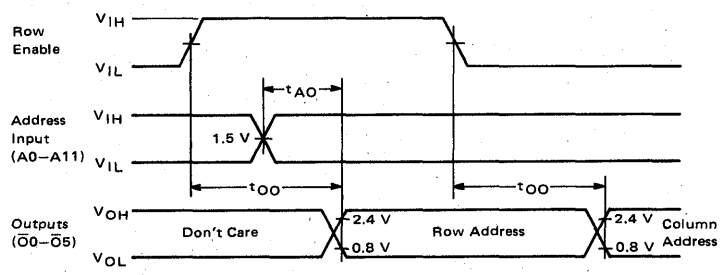
ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Min/Max values apply with 4.5 V ≤ V_{CC} ≤ 5.5 V, 0°C ≤ T_A ≤ 75°C; typical values apply with V_{CC} = 5.0 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current, Low Logic State (V_{IL} = 0.45 V)	I_{IL}	–	-0.04	-0.25	mA
Input Current, High Logic State (V_{IH} = 5.5 V)	I_{IH}	–	–	10	μA
Input Voltage, Low Logic State	V_{IL}	–	–	0.8	V
Input Voltage, High Logic State	V_{IH}	2.0	–	–	V
Output Voltage, Low Logic State (I_{OL} = 5.0 mA)	V_{OL}	–	0.25	0.4	V
Output Voltage, High Logic State (I_{OH} = -1.0 mA)	V_{OH}	2.8	4.0	–	V
Input Clamp Voltage (I_{IC} = -12 mA)	V_{IC}	–	-0.8	-1.5	V
Power Supply Current (V_{CC} = 5.5 V)	I_{CC}	–	100	150	mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, Min/Max values apply with 4.5 V ≤ V_{CC} ≤ 5.5 V, 0°C ≤ T_A ≤ 75°C; typical values apply with V_{CC} = 5.0 V, T_A = 25°C.)

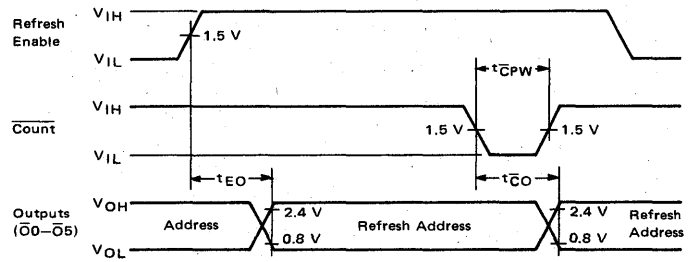
Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times					
Address Input to Output	t_{AO}				ns
(Load = 1 TTL, C_L = 250 pF)		–	16	25	
(Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)		–	6.0	9.0	
Row Enable to Output	t_{OO}				ns
(Load = 1 TTL, C_L = 250 pF)		12	28	41	
(Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)		7.0	12	18	
Refresh Enable to Output	t_{EO}				ns
(Load = 1 TTL, C_L = 250 pF)		12	30	45	
(Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)		7.0	14	20	
$\overline{\text{Count}}$ to Output	$t_{\overline{CO}}$				ns
(Load = 1 TTL, C_L = 250 pF)		20	55	80	
(Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)		15	40	60	

FIGURE 1 – AC WAVEFORMS with MCM6604 NORMAL CYCLE

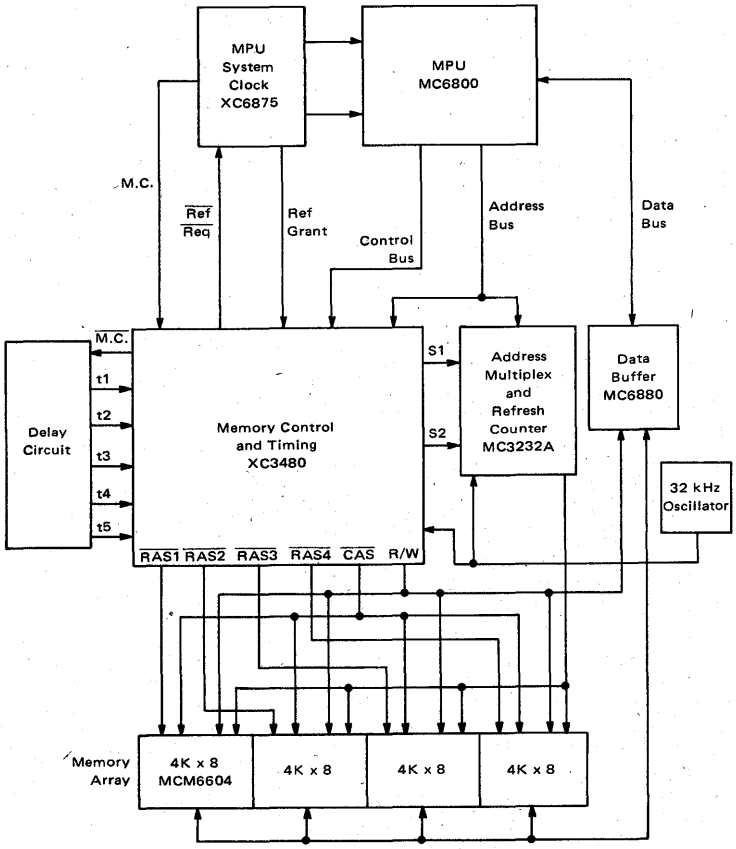


Refresh Enable – Low Logic State

FIGURE 2 – REFRESH CYCLE



TYPICAL APPLICATION
16K X 8-BIT MEMORY SYSTEM FOR M6800 MPU



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ORDERING INFORMATION

Device	Temperature Range	Package
MC3245L	0°C to +75°C	Ceramic DIP
MC3245P	0°C to +75°C	Plastic DIP

MC3245

QUAD TTL TO MOS DRIVER

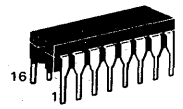
This high-speed driver is intended as a clock (high-level) driver for 22 pin and 18 pin dynamic NMOS RAMs. It is designed to operate on nominal +5 V and +12 V power supplies.

The channel control logic is organized so that all four drivers may be deactivated for STANDBY operation, or single driver may be activated for READ/WRITE operation or all four drivers may be activated for REFRESH operation.

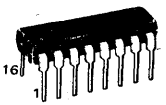
- Control Logic Optimized for Use in MOS RAM Systems
- Output Voltages Compatible with Many Popular MOS RAMs
- TTL and DTL Compatible Inputs
  High-Speed Switching
- Interchangeable with 3245.

GATE CONTROLLED FOUR CHANNEL MOS CLOCK DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

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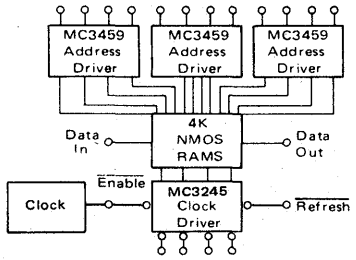
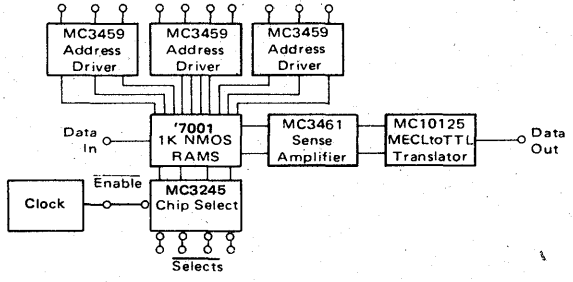
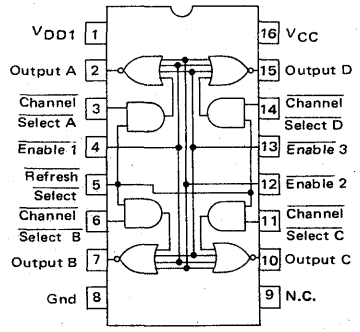
TYPICAL APPLICATION WITH 4K NMOS RAM IN TTL SYSTEM



TYPICAL APPLICATION WITH '7001 RAM AND TTL SYSTEMS



PIN CONNECTIONS



TRUTH TABLE

Inputs					Output
Control			Address		
Enable 1	Enable 2	Enable 3	Channel Select	Refresh Select	
H	I	I	I	I	L
I	H	I	I	I	L
I	I	H	I	I	L
I	I	I	H	H	L
L	L	L	L	I	H
L	L	L	I	L	H

H = High Logic State
L = Low Logic State
I = Irrelevant

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{DD}	-0.5 to +7.0 -0.5 to +14	Vdc Vdc
Output Voltage	V_O	-1.0 to V_{DD} +1.0	Vdc
Input Voltage	V_I	-1.0 to V_{DD}	Vdc
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{DD}	4.75 11.4	5.0 12	5.25 12.6	Vdc Vdc
Operating Ambient Temperature Range	T_A	0	–	75	°C

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ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply over recommended power supply and temperature conditions. Typical values measured at T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage – High Logic State (V_{IL} = 0.8 V, I_{OH} = -1.0 mA)	V_{OH}	V_{DD} - 0.5	–	–	Vdc
Output Clamp Voltage – High Logic State (I_{OH} = 5.0 mA, V_{IL} = 0 V)	V_{OHC}	–	–	V_{DD} + 1.0	Vdc
Output Voltage – Low Logic State (V_{IH} = 2.0 V, I_{OL} = 5.0 mA)	V_{OL}	–	–	0.45	Vdc
Output Clamp Voltage – Low Logic State (V_{IH} = 5.0 V, I_{OL} -5.0 mA)	V_{OLC}	-1.0	–	–	Vdc
Input Voltage – High Logic State	V_{IH}	2.0	–	–	Vdc
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	Vdc
Input Clamp Voltage (I_{IC} = -5.0 mA)	V_{IC}	–	–	-1.0	Vdc
Input Current – High Logic State (V_I = 5.0 V) Channel Select Inputs Refresh Select and Enable Inputs	I_{IH}	 – –	 – –	 10 40	μA
Input Current – Low Logic State (V_{IL} = 0.45 V) Channel Select Inputs Refresh Select and Enable Inputs	I_{IL}	 – –	 – –	 -0.25 -1.0	μA
Power Supply Current – Output High Logic State (V_{CC} = 5.25 V, V_{IL} = 0 V, I_{OH} = 0 mA, V_{DD} = 12.6 V)	I_{CCH} I_{DDH}	– –	23 19	30 26	mA
Power Supply Current – Output Low Logic State (V_{CC} = 5.25, V_{IH} = 5.0 V, I_{OL} = 0 mA, V_{DD} = 12.6 V)	I_{CCL} I_{DDL}	– –	29 12	39 15	mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, these specifications apply over recommended power supply and temperature conditions. Typical values measured at +25°C.)

Characteristic	Symbol	Min (1)	Typ (2)	Max (3)	Unit
Delay Time					ns
Output High to Low Level (R_S = 0 Ω)	t_{DHL}	3.0	7.0	–	
Output Low to High Level (R_S = 0 Ω)	t_{DLH}	5.0	11	–	
Transition Time					ns
Output High to Low Level (R_S = 20 Ω)	t_{THL}	10	17	25	
Output Low to High Level (R_S = 20 Ω)	t_{TLH}	10	17	25	
Propagation Delay Time					ns
Output High to Low Level (R_S = 0 Ω)	t_{PHL}	–	18	32	
Output Low to High Level (R_S = 0 Ω)	t_{PLH1}	–	20	32	
(R_S = 20 Ω)	t_{PLH2}	–	27	38	

(1) C_L = 150 pF
(2) C_L = 200 pF
(3) C_L = 250 pF

CAPACITANCE* (Unless otherwise specified, T_A = +25°C, f = 1.0 MHz, V_I = 2.0 V, and V_{CC} = 0 V.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance Channel Select Inputs	$C_{in}(\overline{CS})$	–	5.0	8.0	pF
Input Capacitance Refresh or Enable Inputs	$C_{in}(\overline{E})$	–	8.0	12	pF

*Periodically sampled, but not 100% tested.

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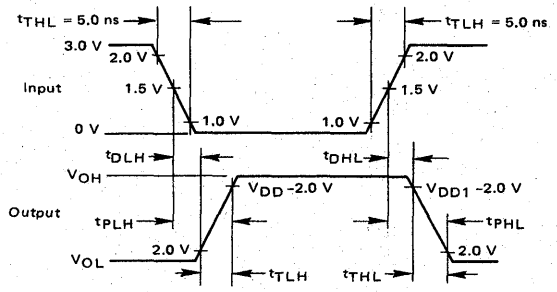
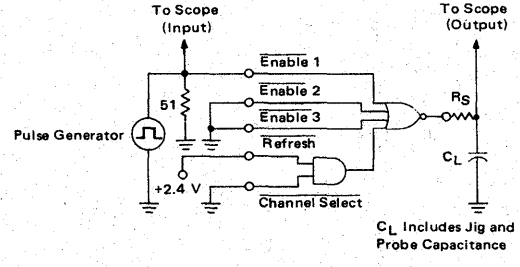
FIGURE 1 – SWITCHING TEST WAVEFORMS



Input Pulse Characteristics
PRR = 1 MHz
PW = 500 ns
$t_{TLH} = t_{THL}$ = 5.0 ns

FIGURE 2 – SWITCHING TEST CIRCUIT



C_L Includes Jig and Probe Capacitance

ORDERING INFORMATION

Device	Temperature Range	Package
MC3408L	0°C to +70°C	Ceramic DIP

MC3408

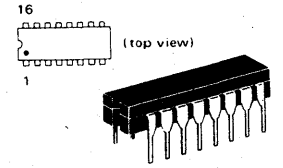
LOW-COST EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

. . . designed for use where the output current is a linear product of an eight-bit digital word and an analog input voltage.

- Relative Accuracy: ±0.5% Error Maximum
- Low Price Allows Use of a D/A in Many New Applications
- Monotonicity Guaranteed to 8 Bits
- Fast Settling Time – 300 ns typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible
- Output Voltage Swing – +0.4 V to -5.0 V
- High-Speed Multiplying Input Slew Rate 4.0 mA/μs
- Standard Supply Voltages: +5.0 V and -5.0 V to -15 V

EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620

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FIGURE 1 – D-to-A TRANSFER CHARACTERISTICS

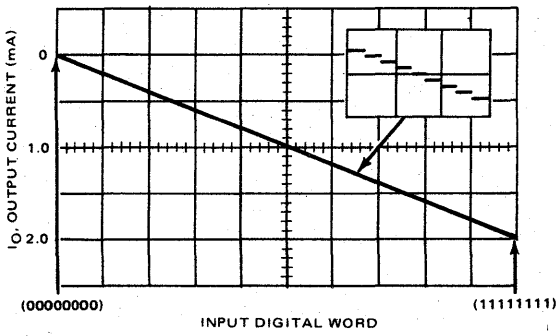
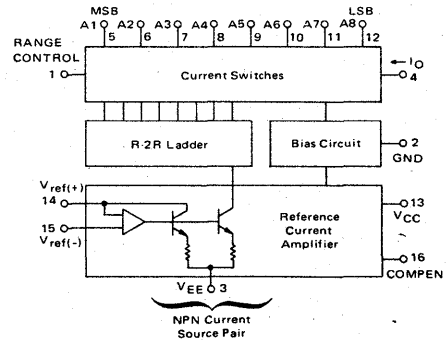


FIGURE 2 – BLOCK DIAGRAM



TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 2 1/2 Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -16.5	Vdc
Digital Input Voltage	V_5 thru V_{12}	0 to +15	Vdc
Applied Output Voltage	V_O	+0.5,-5.2	Vdc
Reference Current	I_{14}	5.0	mA
Reference Amplifier Inputs	V_{14},V_{15}	V_{CC},V_{EE}	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature	T_J	+175	°C

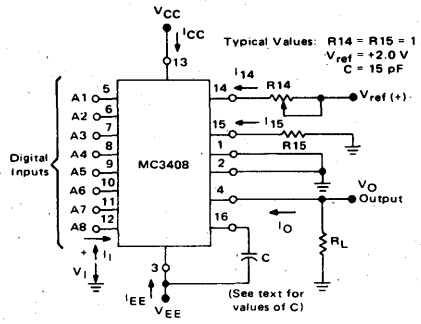
ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -15 Vdc, $\frac{V_{ref}}{R14}$ = 2.0 mA, T_A = 0 to +70°C unless otherwise noted. All digital inputs at high logic level.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O) Note 1	4	E_r	–	–	±0.5	%
Monotonicity See Multiplying Accuracy on Page 6	–	–	Guaranteed to 8 bits			–
Settling Time to within ±0.5% of Full Scale [includes t_{PLH}] (T_A=+25°C)See Note 2	5	t_S	–	300	–	ns
Propagation Delay Time T_A = +25°C	5	t_{PLH},t_{PHL}	–	30	100	ns
Output Full Scale Current Drift		TCI_O	–	-30	–	PPM/°C
Digital Input Logic Levels (MSB) High Level, Logic "1" Low Level, Logic "0"	3	 V_{IH} V_{IL}	 2.0 –	 – –	 – 0.8	Vdc
Digital Input Current (MSB) High Level, V_{IH} = 5.0 V Low Level, V_{IL} = 0.8 V	3	 I_{IH} I_{IL}	 – –	 0 -0.4	 0.04 -0.8	mA
Reference Input Bias Current (Pin 15)	3	I_{15}	–	-1.0	-5.0	μA
Output Current Range V_{EE} = -5.0 V V_{EE} = -15 V (T_A = 25°C)	3	I_{OR}	 0 0	 2.0 2.0	 2.1 4.2	mA
Output Current V_{ref} = 2.000 V, R14 = 1000 Ω	3	I_O	 1.9	 1.99	 2.1	mA
Output Current (All bits low)	3	$I_{O(min)}$	–	0	4.0	μA
Output Voltage Compliance ($E_r \leq$ 0.5% at T_A = +25°C) Pin 1 grounded Pin 1 open, V_{EE} below -10 V	3	V_O	 – –	 – –	 -0.5, +0.4 -5.0, +0.4	Vdc
Reference Current Slew Rate	6	SR I_{ref}	–	4.0	–	mA/μs
Output Current Power Supply Sensitivity		PSRR(–)	–	0.5	4.0	μA/V
Power Supply Current (All bits low)	3	I_{CC} I_{EE}	– –	+13.5 -7.5	+22 -13	mA
Power Supply Voltage Range (T_A = +25°C)	3	V_{CCR} V_{EER}	+4.5 -4.5	+5.0 -15	+5.5 -16.5	Vdc
Power Consumption All bits low V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc All bits high V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc	3	P_C	 – – – –	 105 190 90 160	 170 305 – –	mW

Note 1. For devices with greater accuracy, see MC1508 Series data sheet.
Note 2. All bits switched.

TEST CIRCUITS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT



V_I and I_I apply to inputs A1 thru A8

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left\{\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right\}$$

where $K \cong \frac{V_{ref}}{R14}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

FIGURE 4 – RELATIVE ACCURACY TEST CIRCUIT

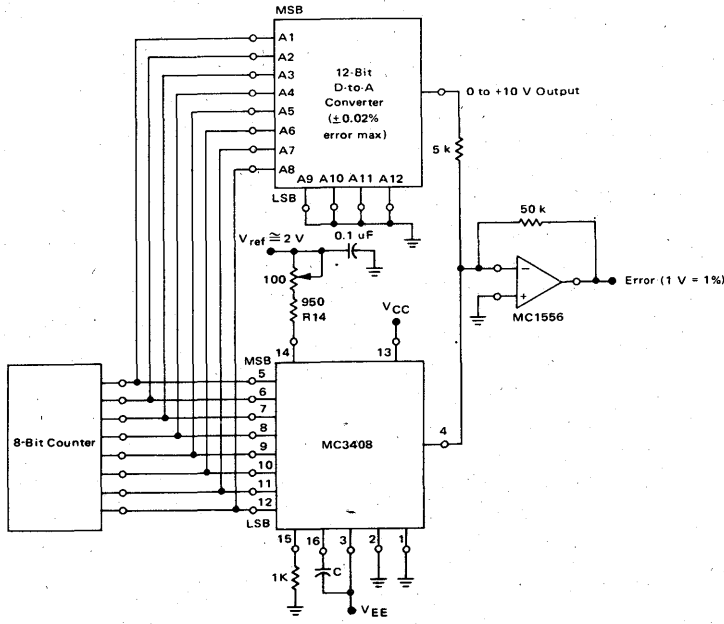
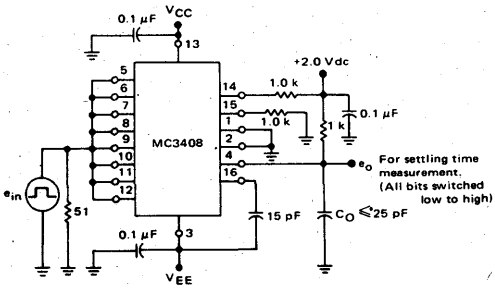
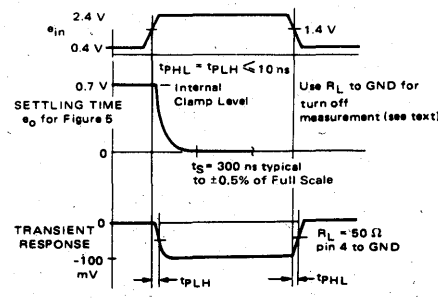


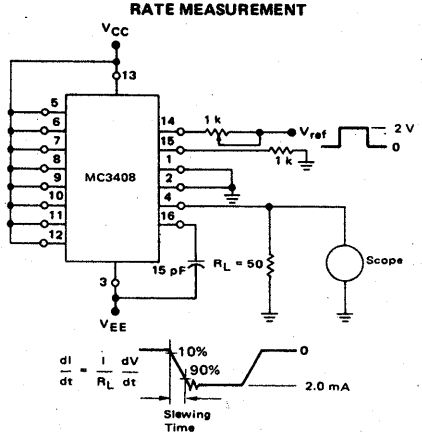
FIGURE 5 – TRANSIENT RESPONSE and SETTLING TIME





TEST CIRCUITS (continued)

FIGURE 6 – REFERENCE CURRENT SLEW RATE MEASUREMENT



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

FIGURE 7 – POSITIVE V_{ref}

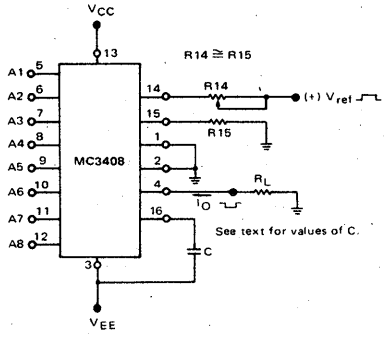


FIGURE 8 – NEGATIVE V_{ref}

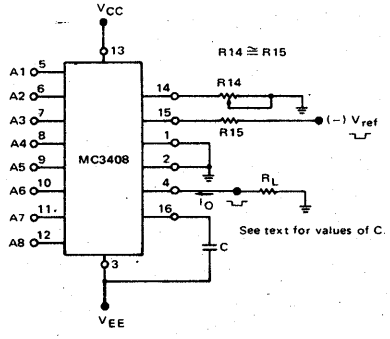
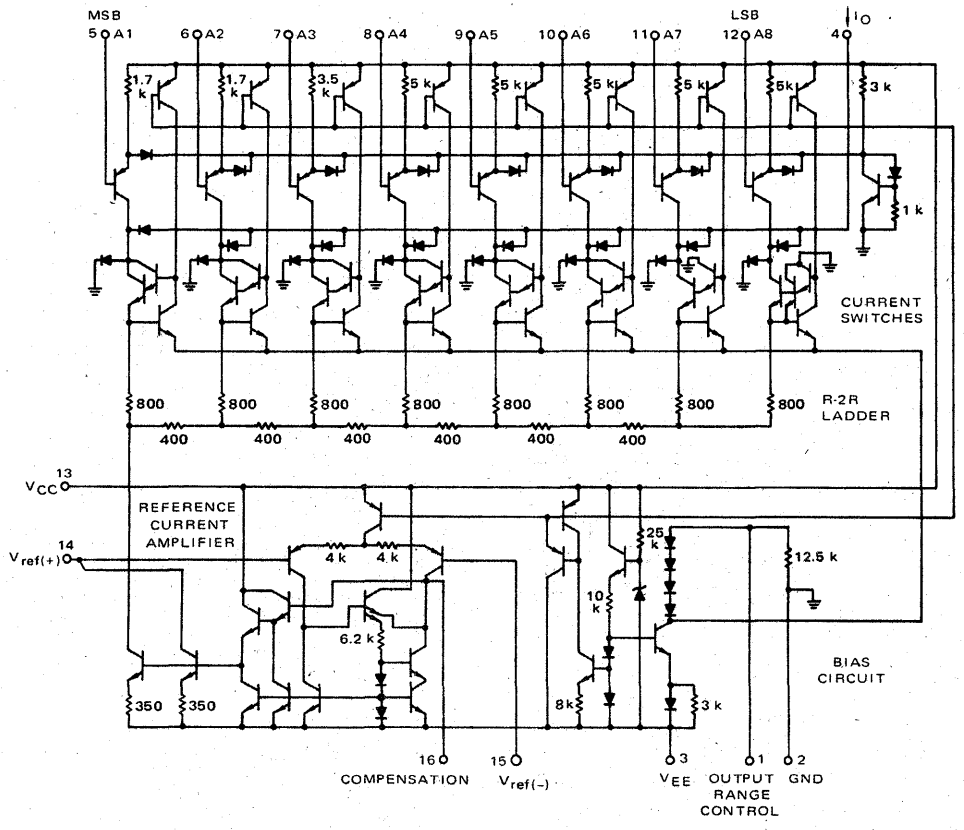


FIGURE 9 – MC3408 EQUIVALENT CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC3408 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component. The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

GENERAL INFORMATION

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I14, must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 7. The reference voltage source supplies the full current I14. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1.0, 2.5 and 5.0 kilohms, minimum capacitor values are 15, 37, and 75 pF. The capacitor should be tied to V_{EE} as this increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in Figure 8. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0-volts above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0-V logic supply is not recommended as a reference voltage. If a well regulated 5.0-V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 μF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.5 to +0.4 volts at +25°C, due to the current switching methods employed in the MC3408. When a current switch is turned "off", the positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is one diode voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC3408 may be extended to -5.0 V volts by opening the circuit at pin 1. The negative supply voltage must be more negative than -10 volts. Using a full scale current of 1.992 mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance, but a 2.5-kilohm load increases "worst case" settling time to 1.2 μs (when all bits are switched on). Refer to the subsequent text section on Settling Time for more details on output loading.

If a power supply value between -5.0 V and -10 V is desired, a voltage of between 0 and -5.0 V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages typically more negative than -8.0 volts, due to the increased voltage drop across the 350-ohm resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC3408 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC3408 has a very low full scale current drift with temperature.

The MC3408 is guaranteed accurate to within ±0.5% at +25°C at a full scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0 mA, with the loss of one LSB = 8.0 μA which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 4. The 12-bit converter is calibrated for a full scale output current of 1.992 mA. This is an optional step since the MC3408 accuracy is essentially the same between 1.5 and 2.5 mA. Then the MC3408 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65, 536, or ±0.00076%, which is much more accurate than the ±0.5% specification provided by the MC3408.

Multiplying Accuracy

The MC3408 may be used in the multiplying mode with good accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions, these eight amplifiers can contribute a total of 1.6 μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 16 μA to 2.0 mA, the 1.6 μA contributes an error of 0.2 LSB with respect to the 2.0 mA.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC3408 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 2.0 mA.

ORDERING INFORMATION

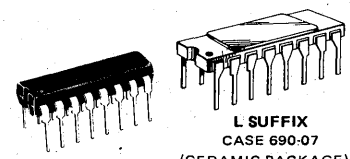
Device	Temperature Range	Package
MC3410L	0°C to +70°C	Ceramic DIP
MC3410P	0°C to +70°C	Plastic DIP
MC3410CL	0°C to +70°C	Ceramic DIP
MC3410CP	0°C to +70°C	Plastic DIP
MC3510L	−55°C to +125°C	Ceramic DIP

MC3410
MC3510 MC3410C

LASER TRIMMED

TEN BIT, MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
CASE 648-03
(PLASTIC PACKAGE)
(MC3410, MC3410C ONLY)

L SUFFIX
CASE 690-07
(CERAMIC PACKAGE)

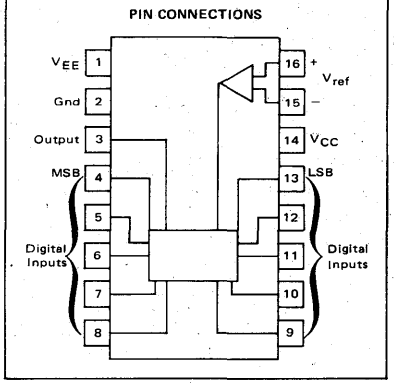
Specifications and Applications Information

TEN BIT D TO A CONVERTER

The MC3410 series devices are low-cost, high-accuracy monolithic D/A converter subsystems. Like their MC1408 series predecessors, they provide the logic controlled current switches, the R-2R resistor ladder network and output termination networks. The output buffer amplifier and reference voltage have been omitted from the circuit to allow greatest system speed, flexibiliby and lowest cost. This device is useful in industrial control and microprocessor based systems.

- Relative Accuracy – ±0.05% Error Maximum (MC3510 and MC3410)
- Fast Settling Time – 250 ns Typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible (from 5 to 15 V CMOS)
- Output Voltage Swing – +0.2 V to −2.5 V
- High Speed Multiplying Input Slew Rate – 20 mA/μs
- Standard Supply Voltages – +5 V and – 15 V
- All Categories Guaranteed Monotonic
- Reference Amplifier Internally Compensated

PIN CONNECTIONS



TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 3-Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Speech Compression and Expansion
- Sample Data Systems

FIGURE 1 – D-to-A TRANSFER CHARACTERISTICS

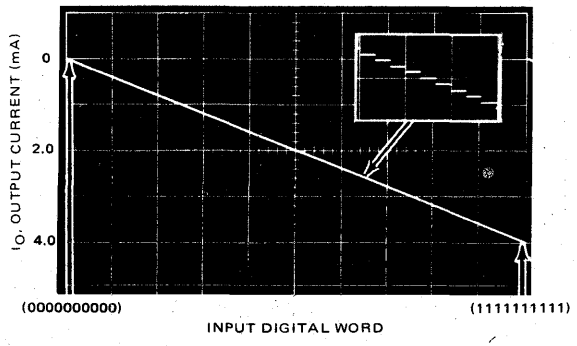
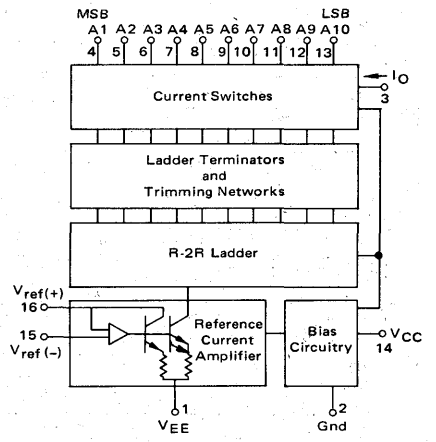


FIGURE 2 – TEN-BIT D/A CONVERTER BLOCK DIAGRAM



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 −18	Vdc
Digital Input Voltage	V_I	+15	Vdc
Applied Output Voltage	V_O	+0.7,-5.0	Vdc
Reference Current	$I_{REF(16)}$	2.5	mA
Reference Amplifier Inputs	V_{REF}	V_{CC}, V_{EE}	Vdc
Reference Amplifier Differential Inputs	$V_{REF(D)}$	0.7	Vdc
Operating Temperature Range MC3510 MC3410,C	T_A	 −55 to +125 0 to +70	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = −15 Vdc, $\frac{V_{ref}}{R16}$ = 2.0 mA, MC3510 T_A = −55°C to +125°C.
MC3410 Series: T_A = 0 to +70°C unless otherwise noted. All digital inputs at high logic level.)

Characteristic	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O) T_A = 25°C MC3510 MC3410 MC3410C	E_r	 – – –	 – – –	 ±0.05 ±0.05 ±0.1	%
Relative Accuracy Temperature Drift (Relative to Full Scale I_O)	TCE_r	–	2.5	–	PPM/°C
Monotonicity (T_A = 25°C)	–	Monotonic to 10 Bits			–
Settling Time to within ±1/2 LSB (T_A = 25°C) (All Bits Low to High)	t_S	–	250	–	ns
Propagation Delay Time T_A = +25°C	t_{PLH} t_{PHL}	– –	35 20	– –	ns
Output Full Scale Current Drift	TCI_O	–	−20	–	PPM/°C
Digital Input Logic Levels (All Bits) High Level, Logic "1" Low Level, Logic "0"	 V_{IH} V_{IL}	 2.0 –	 – –	 – 0.8	Vdc
Digital Input Current (All Bits) High Level, V_{IH} = 5.5V Low Level, V_{IL} = 0.8V	 I_{IH} I_{IL}	 – –	 – 0.05	 0.04 0.4	mA
Reference Input Bias Current (Pin 15)	$I_{REF(15)}$	–	−1.0	−5.0	μA
Output Current Range	I_{OR}	0	4.0	5.0	mA
Output Current V_{ref} = 2.000 V, R_{16} = 1000 Ω	I_O	3.8	3.996	4.2	mA
Output Current (All bits low) MC3510, MC3410 MC3410C	$I_{O(min)}$	– –	0 0	2.0 4.0	μA
Output Voltage Compliance (T_A 25°C) E_r ≤ 0.05% relative to FS – MC3510, MC3410 E_r ≤ 0.10% relative to FS – MC3410C	V_O	–	–	 -2.5,+0.2 -2.5,+0.2	Vdc
Reference Amplifier Slew Rate	SR I_{ref}	–	20	–	mA/μs
Reference Amplifier Settling Time (0 to 4.0 mA, ±0.1%)	STI_{REF}	–	2.0	–	μs
Output Current Power Supply Sensitivity MC3510, MC3410 MC3410C	PSRR(–)	– –	0.003 0.003	0.01 0.02	%/%
Output Capacitance (V_O = 0)	C_O	–	25	–	pF
Digital Input Capacitance (All Bits, Inputs High)	C_I	–	4.0	–	pF
Power Supply Current (All Bits low)	I_{CC} I_{EE}	– –	+10 −11.4	+18 −20	mA
Power Supply Voltage Range (T_A = +25°C)	V_{CCR} V_{EER}	+4.75 -14.25	+5.0 −15	+5.25 −15.75	Vdc
Power Consumption All Bits low All Bits high	P_C	 – –	 220 200	 380 –	mW

TEST CIRCUITS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUITS

V_I and I_I apply to inputs A1 thru A10

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left(\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}+\frac{A9}{512}+\frac{A10}{1024}\right)$$

where $K \cong \frac{2V_{ref}}{R16}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

Typical Values:
R15 = R16 = 1 k
V_{ref} (+) = +2.0 V
V_{ref} (–) = Gnd
I_O = 4.0 mA

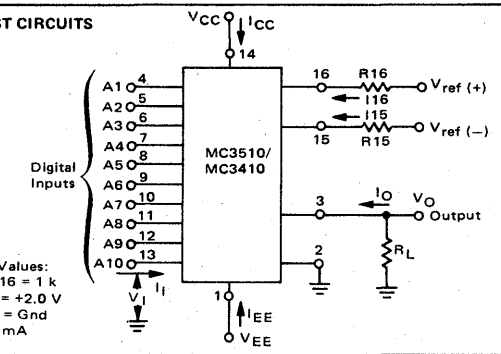


FIGURE 4 – RELATIVE ACCURACY TEST CIRCUIT

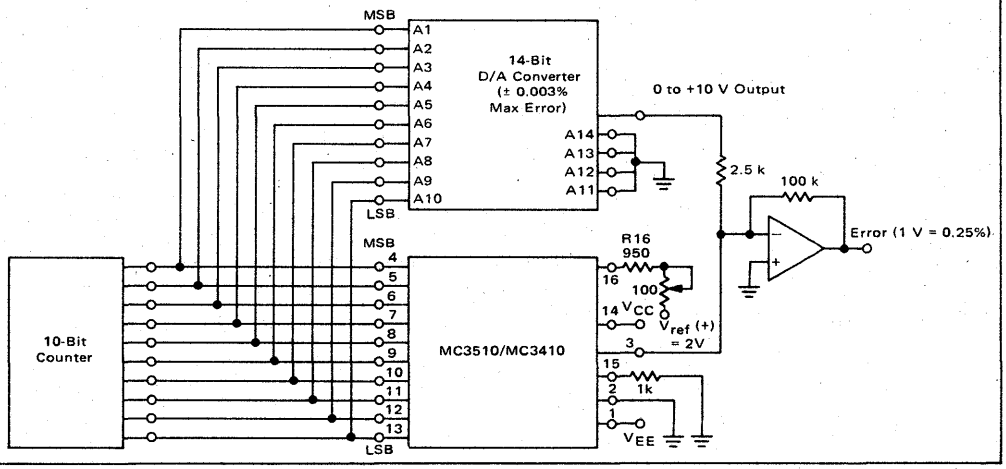
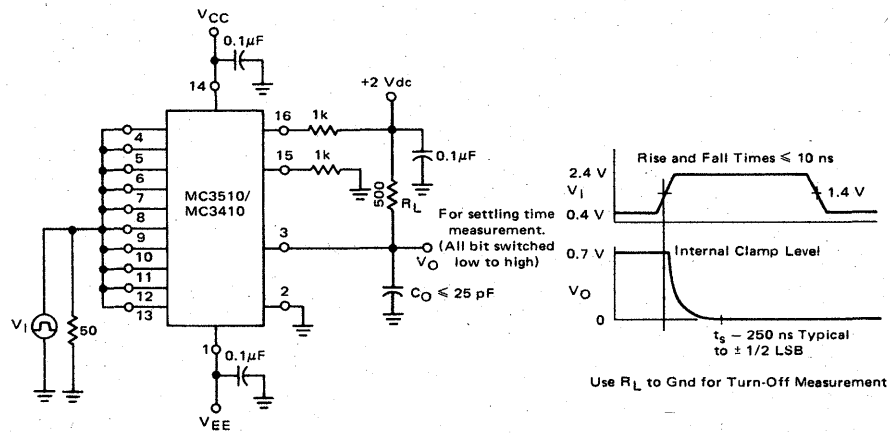


FIGURE 5 – SETTLING TIME



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TEST CIRCUITS (Continued)

FIGURE 6 – PROPAGATION DELAY TIME

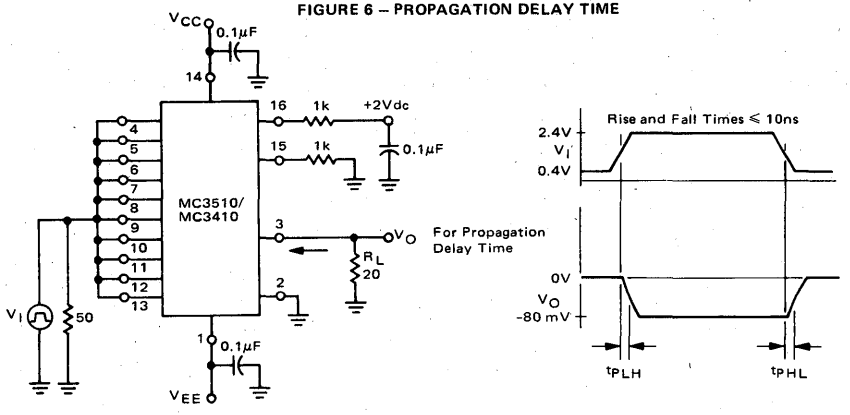


FIGURE 7 – REFERENCE AMPLIFIER SETTLING TIME AND SLEW RATE

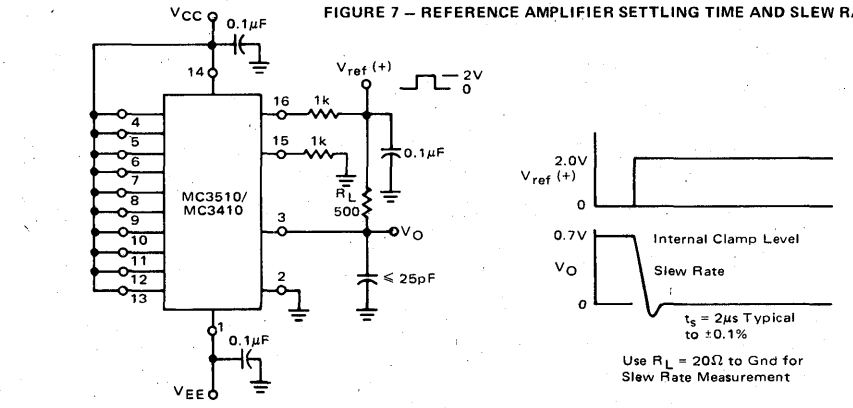


FIGURE 8 – POSITIVE V_{ref}

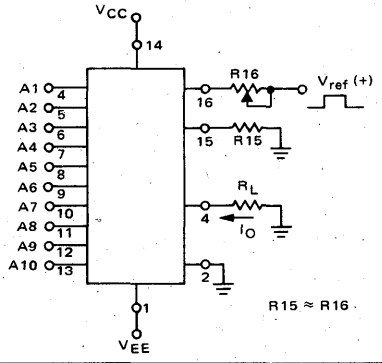
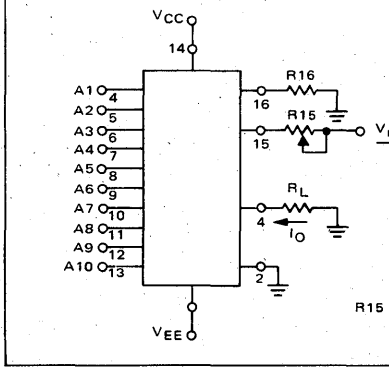


FIGURE 9 – NEGATIVE V_{ref}



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

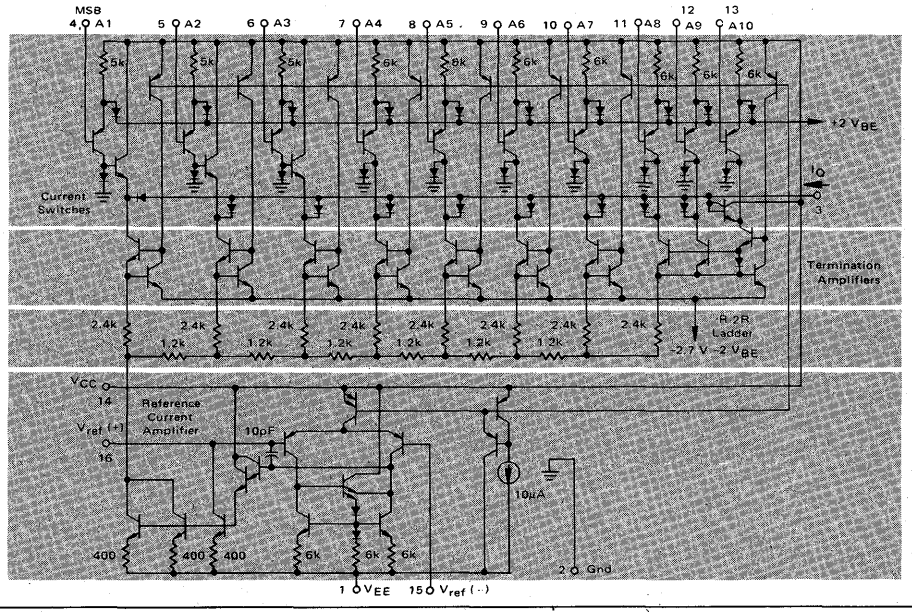
Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst-case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

FIGURE 10 – MC3410 10-BIT D/A CONVERTER EQUIVALENT CIRCUIT



CIRCUIT DESCRIPTION

The MC3410 consists of a reference current amplifier, a diffused R-2R ladder, a laser trimming network, and ten high-speed current switches. The trimming method employed makes it possible to improve the linearity attainable with modern diffusion technology by as much as a factor of ten so that a highly linear part results. The trim is performed by cutting aluminum links arranged to give incremental variations in voltage at the ladder termination amplifiers (See Figure 10). This yields a highly stable trim with no increase in fabrication complexity.

The switches are non-inverting in operation, so that a high state on an input turns on the specific component of output current. The switches use current steering for speed, and interface the R-2R ladder through unity gain feedback termination amplifiers, which provide low impedance terminations of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the current switches. The three least-significant bit switches derive their current through emitter scaling from the last leg of the ladder. The remaining current, equal to one LSB, is shunted to V_{CC} at the LSB switch. Therefore, the maximum output current is 1023/1024 of the reference amplifier current, or nominally 3.996 mA for a 2.000 mA reference input current.

GENERAL INFORMATION

Reference Amplifier

The reference amplifier allows the user to provide a voltage and a resistor to Pin 16 to convert the reference voltage to a current. A current mirror doubles this reference current and feeds it to the R-2R ladder. Thus for a reference voltage of 2.0 Volts and 1 kΩ resistor tied to Pin 16, the full-scale current is approximately 4.0 mA. The reference input current, I16, must flow into Pin 16 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 8. The reference voltage source supplies the full current I16. For bipolar refererence signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The reference amplifier is internally compensated with a 10 pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R16 and reference voltages which supply 2.0 mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0 mA. As R16 increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0 MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R16 = 1.0 kΩ, and settling time is ≈ 10 μs. The reference amplifier phase margin decreases as the current source value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5 mA for stability.

A negative reference voltage may be used if R16 is grounded and the reference voltage is applied to R15 as shown in Figure 9. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3 Volts above the V_{EE} supply for proper operation. Bipolar input signals may be handled by connecting R16 to a positive voltage equal to the peak positive input level at Pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5-V logic supply is not recommended as a reference voltage. If a well regulated 5.0-V supply, which drives logic, is to be used as the reference, R16 should be decoupled by connecting it to the +5.0 V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1 μF capacitor to ground.

Output Voltage Range

The voltage on Pin 3 is restricted to a range of −2.5 V to +0.2 V due to the current switching methods employed in the MC3410. When a current switch is turned off, the positive voltage at the output terminal can turn on the output diode and increase the output current. When a current switch is on, the negative output voltage range is restricted to the point at which the low current device of the termination amplifier Darlington begins to saturate, resulting in a decrease in output current.

The output voltage compliance is guaranteed at 25°C. Note from Figure 14 that the output compliance of the MC3410 is nearly constant over temperature.

Accuracy

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full scale current. The relative accuracy of the MC3410 is fairly constant over temperature due to the excellent temperature tracking, of the diffused resistors. The full scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the MC3410 has a low full scale current drift with temperature.

The MC3510 and MC3410 are guaranteed accurate to within ±1/2 LSB at 25°C and at a full scale current of 3.996 mA. Input reference current to Pin 16 is guaranteed to be between 1.9 and 2.1 mA to produce a full scale output current of 3.996 mA. The relative accuracy test circuit is shown in Figure 4. The 14 bit D/A converter is calibrated for a full scale output of 3.996 mA. This is an optional step as the relative accuracy of the MC3410 is nearly constant between 3 mA and 5 mA full scale current. The MC3410 is calibrated at full scale with the 14-bit reference D/A by adjusting R16 until the error voltage goes to zero. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored on a peak detector.

Monotonicity

The MC3510, MC3410 and MC3410C are all guaranteed to be monotonic at room temperature. This guarantees that for every increase in the input digital word, the output current either remains the same or increases, but never decreases. The MC3510 and MC3410 are typically monotonic over their respective temperature ranges. In the multiplying mode (when the reference current is varied), monotonicity is typically maintained for all values of input reference current above 0.5 mA.

Settling Time

The worst case switching condition occurs when all bits are switched "on," which corresponds to a low-to-high transition for all bits. This time is typically 250 ns for the output to settle to within ± 1/2 LSB for 10-bit accuracy, and 200 ns for 8-bit accuracy. The turn-off time is typically 120 ns. These times apply when the output swing is limited to a small (< 0.7 Volt) swing and the external output capacitance is under 25 pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

The slowest switches are bit A10 (LSB) and bit A9, which turn on and settle in typically 200 ns, and turn off in 100 ns.

In the test circuit of Figure 5, the output voltage is internally clamped in the MC3410 at about 0.7 Volts above ground. The output is thus limited to a 0.7 Volt swing. If a load resistor of 625 Ohms is connected to ground, allowing the output to swing to −2.5 Volts, the settling time increases to 1.5 μs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing, and minimum scope lead length are all necessary.

MC3510 TERMINOLOGY

RELATIVE ACCURACY — Maximum output deviation from the straight line connecting zero and full scale, expressed as a percentage of full scale.

RELATIVE ACCURACY DRIFT — The average change in linearity error that will occur with a change in ambient temperature, expressed in parts per million of full scale per degree C.

MONOTONICITY — For every increase in the input digital word, the output current either remains the same or increases.

SETTLING TIME — The elapsed time from the input transition until the output has settled within an error band about its final value.

OUTPUT FULL SCALE CURRENT DRIFT — The average change in full scale current between 25°C and either temperature extreme, expressed in parts per million of full scale per degree C.

REFERENCE AMPLIFIER SLEW RATE — The maximum rate of change of the full scale output current expressed in milliamperes per microsecond.

OUTPUT VOLTAGE COMPLIANCE — The maximum voltage that can be applied to the output pin so that the specified change in output current is not exceeded.

POWER SUPPLY SENSITIVITY — The change in full scale current caused by a change in V_{EE}, expressed as a percent of full scale current per percent change in V_{EE}.

TYPICAL CHARACTERISTICS

FIGURE 11 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

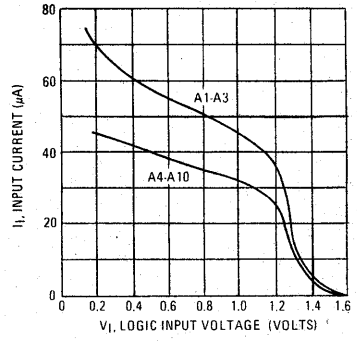


FIGURE 12 – TRANSFER CHARACTERISTIC versus TEMPERATURE

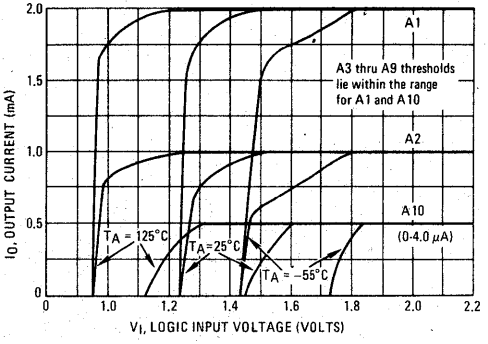


FIGURE 13 – OUTPUT CURRENT versus OUTPUT VOLTAGE (Output Compliance)

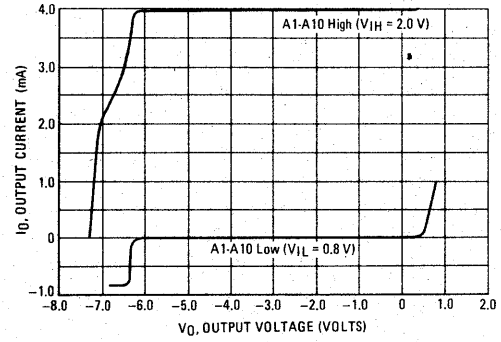


FIGURE 14 – MAXIMUM OUTPUT VOLTAGE versus TEMPERATURE

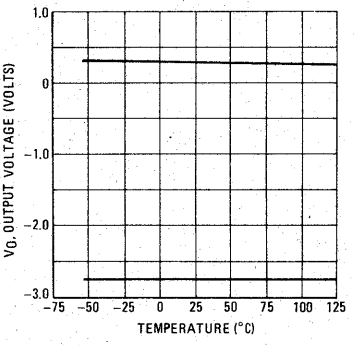


FIGURE 15 – REFERENCE AMPLIFIER FREQUENCY RESPONSE

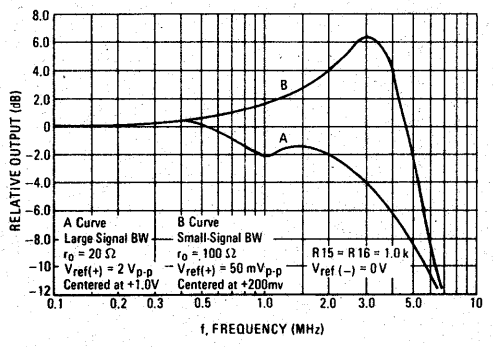
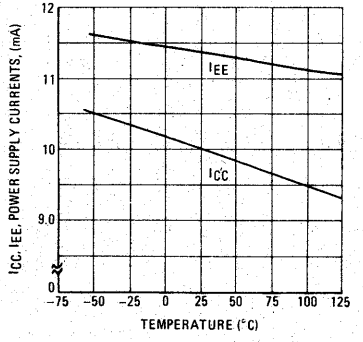


FIGURE 16 – TYPICAL POWER SUPPLY CURRENTS versus TEMPERATURE



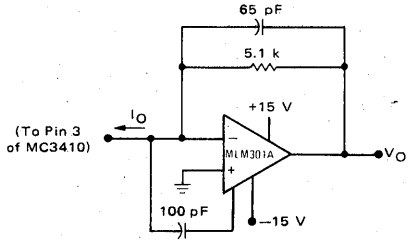
APPLICATIONS INFORMATION

Voltage outputs are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC3410 at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

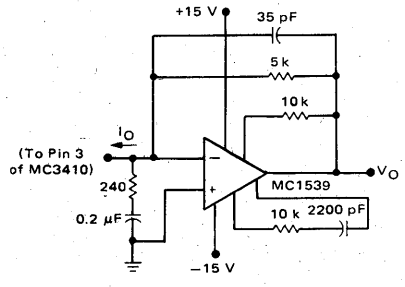
The following circuit shows how the MLM301A can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 μs.

FIGURE 17



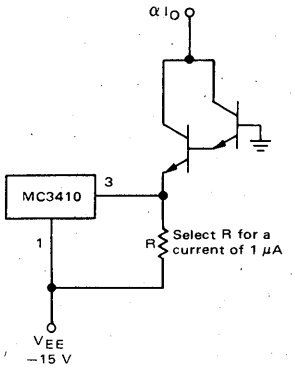
An alternative method is to use the MC1539 and input compensation. Response of this circuit is also on the order of 2.0 μs. See Motorola Application Note AN-459 for more details on this concept.

FIGURE 18



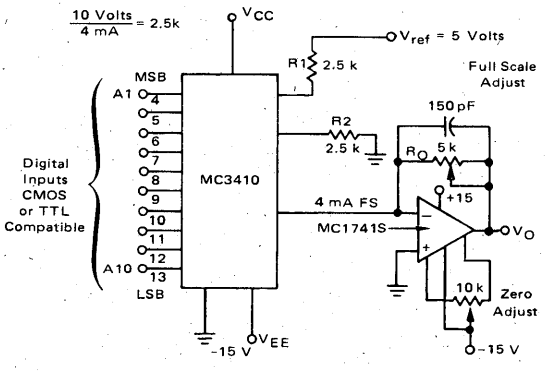
The positive voltage range may be extended by cascading the output with a high beta common base transistor, Q1, as shown.

FIGURE 19 – EXTENDING POSITIVE VOLTAGE RANGE



The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing, because Pin 3 is held at a constant voltage. The resistor (R) to V_{EE} maintains the transistor emitter voltage when all bits are "off" and insures fast turn-on of the least significant bit.

FIGURE 20 – OUTPUT CURRENT TO VOLTAGE CONVERSION



$$V_O = \frac{2R_0}{R_1} V_{ref} \left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256} + \frac{A9}{512} + \frac{A10}{1024}\right]$$

for 10 volt fullscale calibration

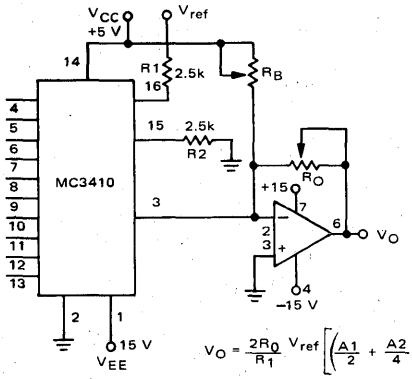
$$V_O = \frac{2(2.5\ k)}{2.5\ k}\ 5\ Volts\left[\frac{1023}{1024}\right] \qquad V_O = 10\ Volts\ [0.9990]$$

APPLICATIONS INFORMATION (Continued)

Bipolar or Negative Output Voltage

The circuit in Figure 21 is a variation of the standard output voltage circuit in Figure 20. A negative or offset binary output may be obtained by sourcing current from the reference into the output through R_B. If R_B allows 2 mA (R_B=2.5 kΩ from 5 Volts) then 1000000000 input will generate zero output voltage.

FIGURE 21 – OFFSET BINARY OR BIPOLAR DAC



For Offset Binary Output From +5 V to −5 V

$R_O \cong 2.5\ k\Omega$

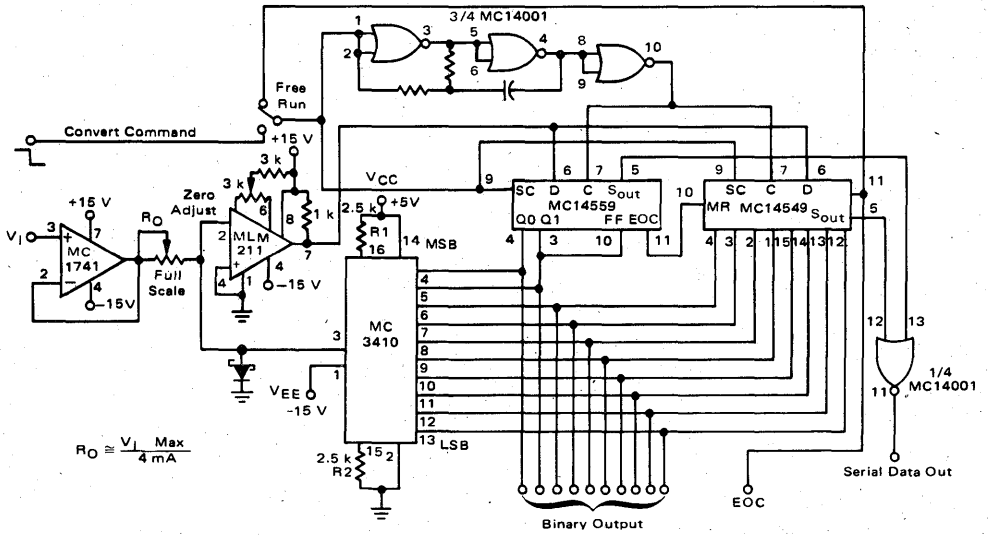
$R_B \cong 2.5\ k\Omega$

$$V_O = \frac{2R_O}{R_1} V_{ref}\left[\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256} + \frac{A9}{512} + \frac{A10}{1024}\right) - \frac{2R_I}{R_B}\right]$$

Successive Approximation A to D

The fastest and most efficient means of A to D conversion using D to A convertors is successive approximation (SA). Similar in appearance to staircase devices, the SA converter is capable of 100 times faster conversions for a 10-bit result. A complete 10-bit SA converter using MC3410 and MC14559/49 successive approximation registers is shown in Figure 22. The complexity which results in higher conversion speeds is contained in the MC14559/49 registers. Quite simply, the register compares the DAC output resulting from activating each bit with the input voltage. This is done starting with most significant bit and after 10 comparisons generates the 10-bit binary output representing that input. The accuracy of the conversion is fixed by the accuracy of the MC3410 and is not dependent on tolerances of the other components. An EOC outout is available and can be used to latch the parallel output or to synchronize the serial output which is also available. For more details on SA converters, see AN-716.

FIGURE 22 – SUCCESSIVE APPROXIMATION CONVERTER USING MC3410



APPLICATIONS INFORMATION (Continued)

Staircase A to D

If high conversion speed is not required, a staircase A to D convertor can be built for somewhat lower cost. A complete staircase A/D convertor is shown in Figure 23. Here the complicated SA registers are replaced with simple binary counters. With an input voltage applied, the binary counter is reset by the convert command pulse and the begin accumulating counts. The DAC output steps upward until the comparator detects that the input is equal to the DAC output. The counters are disabled and the conversion result is held at the output until the circuit is reset by the convert command input.

One advantage of staircase convertors is the ease with which BCD outputs may be obtained. Figure 24 shows a 3-digit panel meter using the staircase technique and an MC14553 3-decade counter. The circuit function is similar to Figure 23 but Multiplexed BCD output is available from the MC14553 counters. Parallel BCD may be obtained with equal ease using the MC14518 two decade CMOS counters.

In both these staircase designs the system accuracy is determined by the specified accuracy of the MC3410.

FIGURE 23 – 10-BIT STAIRCASE A to D USING MC3410

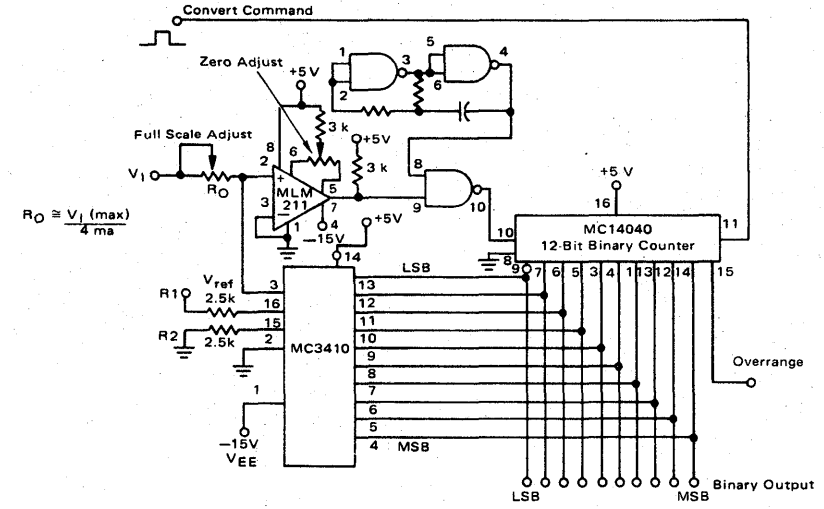
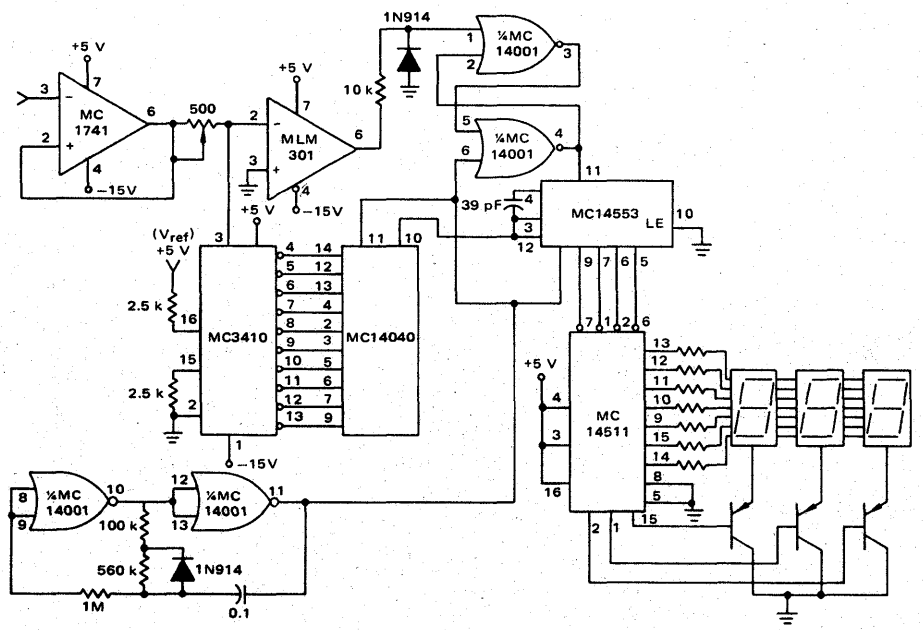
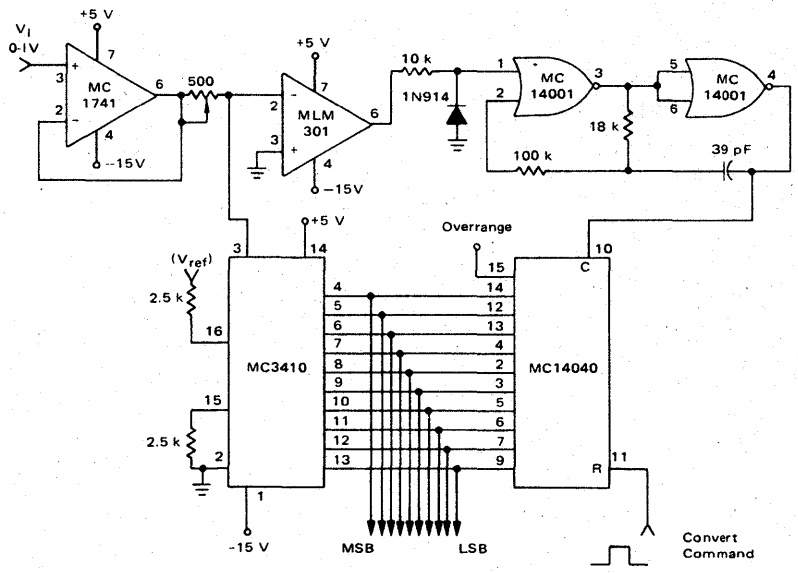


FIGURE 24 – 3-DIGIT DVM USING MC3410



APPLICATIONS INFORMATION (Continued)

FIGURE 25 – ALTERNATE APPROACH STAIRCASE A TO D



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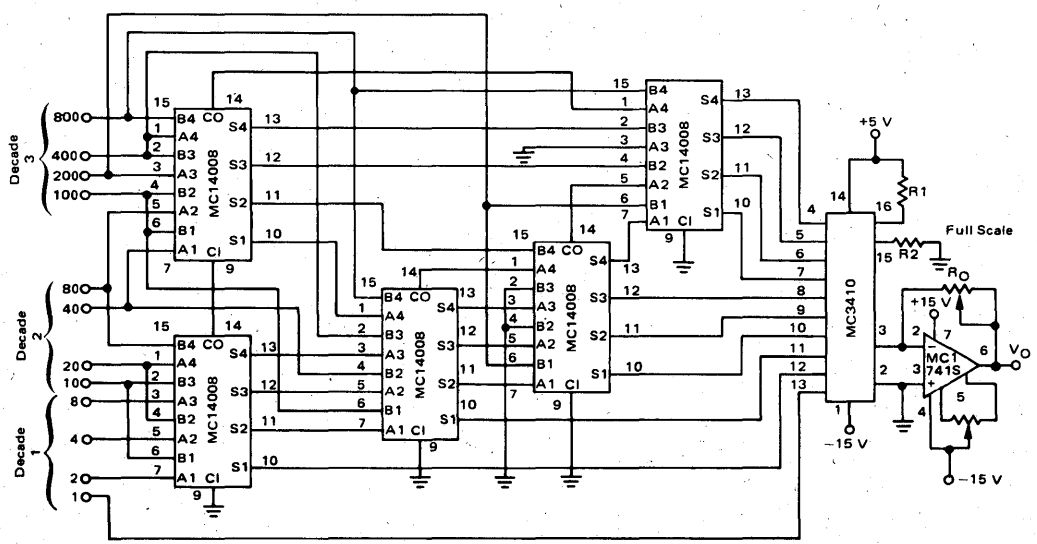
APPLICATIONS INFORMATION (Continued)

BCD D to A Converter

BCD output A to D conversions are most easily accomplished by accumulating the digital results in two different counters, but that concept does not extend to BCD Dto A techniques. Using the circuit in Figure 26 a three-digit BCD number can be converted to a 10-bit accurate voltage. The MC14008's perform the combinational BCD-to-Binary conversion. The accuracy of this circuit is also solely dependent on the accuracy of the MC3410.

FIGURE 26 – 3-DECADE BCD DAC



ORDERING INFORMATION

Device	Temperature Range	Package
MC3416L	0°C to +70°C	Ceramic DIP
MC3416P	0°C to +70°C	Plastic DIP

MC3416

Specifications and Applications Information

4 x 4 x 2 CROSSPOINT SWITCH

4 x 4 x 2 CROSSPOINT SWITCH

DIELECTRICALLY ISOLATED MONOLITHIC INTEGRATED CIRCUIT

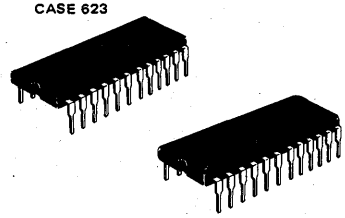
The MC3416 consists of a pair of 4 x 4 matrices of dielectrically isolated SCR's, triggered by a common selection matrix. The device is intended for switching analog signals in communication systems. The use of dielectric isolation processing provides excellent crosstalk isolation while maintaining minimal insertion loss.

The selection array consists of PNP transistors with the input thresholds compatible with either McMOS or MTTL logic families.

The MC3416 is a monolithic pin-for-pin replacement for the discontinued MCBH7601 hybrid device.

- Low Series Resistance – r_{on} = 6.0 Ohms (Typ) @ I_{AK} = 20 mA
- High Series Resistance – r_{off} = 100 MΩ (Min)
- Pin Compatible with MCBH7601 or RC4444
- High Breakdown Voltage – 30 V (Typ)
- Selection Matrix Compatible with TTL or CMOS Logic Levels
- Dielectric Isolation Insures Low Crosstalk and Low Insertion Loss

L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 649

5

FIGURE 1 – REPRESENTATIVE CELL SCHEMATIC
(Repeated 16 Times)

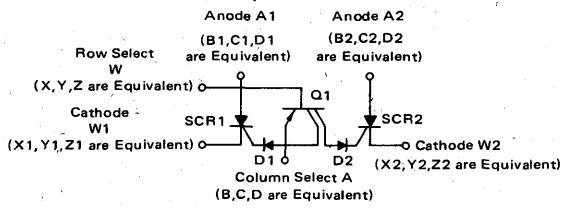
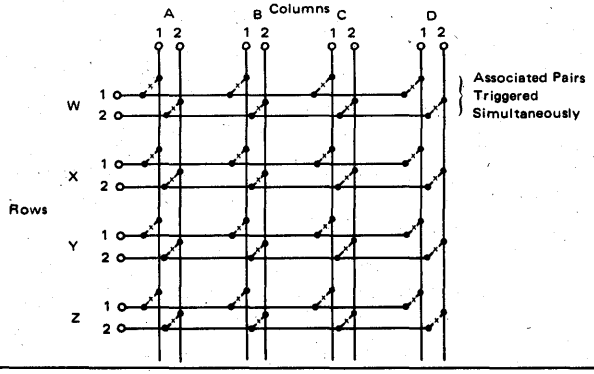
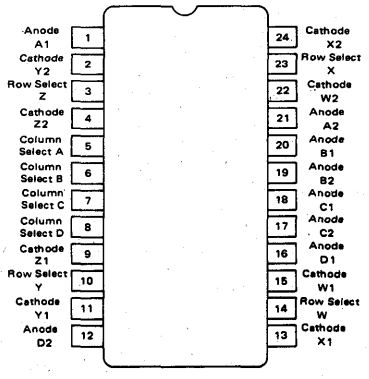


FIGURE 2 – MATRIX CONFIGURATION AND NOMENCLATURE
(X Indicates a Possible Connection)



PIN CONNECTIONS



MAXIMUM RATINGS (Unless otherwise noted, $T_A = 25^oC$)

Rating	Symbol	Value	Unit
Anode-Cathode Current – Continuous (only one SCR at a time)	I_{AK}	150	mA
Enable Current	I_{En}	10	mA
Operating Ambient Temperature Range	T_A	0 to +70	^oC
Storage Temperature Range	T_{stg}	-65 to +150	^oC
Junction Temperature Range	T_J	150^oC	^oC

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $T_A = 0$ to 70^oC)

Characteristic	Symbol	Min	Max	Unit
Anode Cathode Breakdown Voltage ($I_{AK} = 25\mu A$)	BV_{AK}	25	–	Vdc
Cathode-Anode Breakdown Voltage ($I_{KA} = 25\mu A$)	BV_{KA}	25	–	Vdc
Base-Cathode Breakdown Voltage ($I_{BK} = 25\mu A$)	BV_{BK}	25	–	Vdc
Cathode-Base Breakdown Voltage ($I_{KB} = 25\mu A$)	BV_{KB}	25	–	Vdc
Base-Emitter Breakdown Voltage ($I_{BE} = 25\mu A$)	BV_{BE}	25	–	Vdc
Emitter-Cathode Breakdown Voltage ($I_{EK} = 25\mu A$)	BV_{EK}	25	–	Vdc
OFF State Resistance ($V_{AK} = 10$ V)	r_{off}	100	–	MΩ
Dynamic ON Resistance (Center Current = 10 mA) (See Figure 8) (Center Current = 20 mA)	r_{on}	 4.0 2.0	 12 10	Ω
Holding Current (See Figure 10)	I_H	0.7	3.0	mA
Enable Current ($V_{BE} = 1.5$ V) (See Figure 7)	I_{En}	4.0	–	mA
Anode-Cathode ON Voltage ($I_{AK} = 10$ mA) ($I_{AK} = 20$ mA)	V_{AK}	 – –	 1.0 1.1	V
Gate Sharing Current Ratio @ Cathodes (Under Select Conditions with Anodes Open) (See Figure 3)	G_{Sh}	0.8	1.25	mA/mA
Inhibit Voltage ($V_B = 3.0$ V) (See Figure 9)	V_{inh}	–	0.3	V
Inhibit Current ($V_B = 3.0$ V) (See Figure 9)	I_{inh}	–	0.1	mA
OFF State Capacitance ($V_{AK} = 0$ V) (See Figure 6)	C_{off}	–	2.0	pF
Turn-ON Time (See Figure 4)	t_{on}	–	1.0	μs
Minimum Voltage Ramp (Which Could Fire the SCR Under Transient Conditions)	dv/dt	800	–	V/μs

FIGURE 3 – TEST CIRCUIT

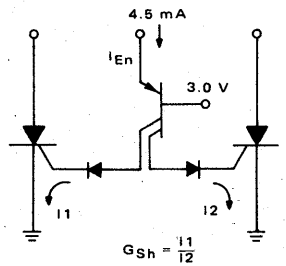


FIGURE 4 – TEST CIRCUIT FOR dv/dt AND t_{on}

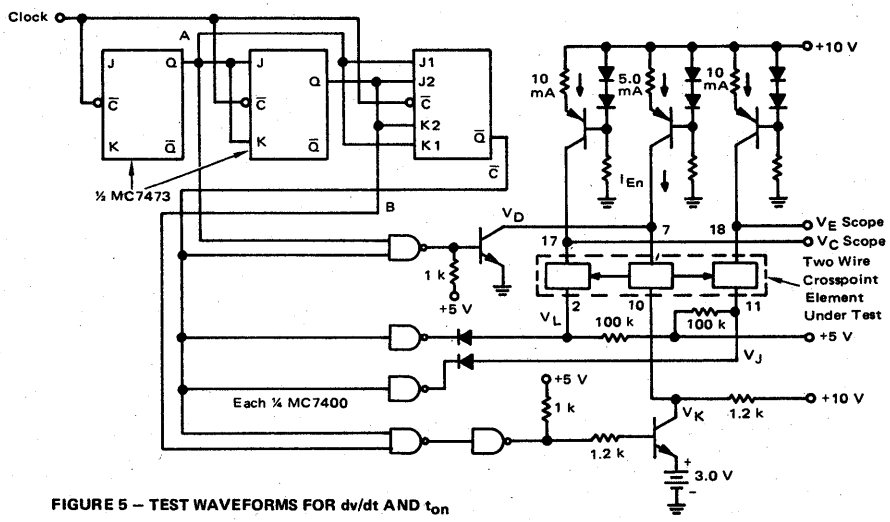


FIGURE 5 – TEST WAVEFORMS FOR dv/dt AND t_{on}

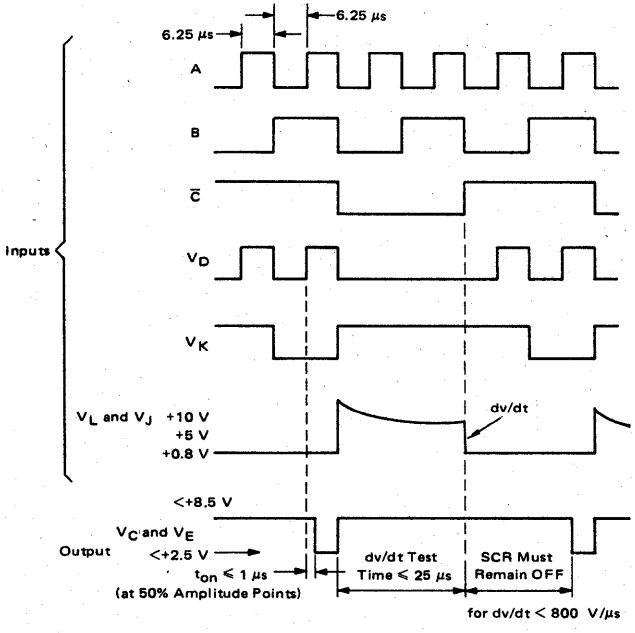


FIGURE 6 – TEST CIRCUIT FOR OFF-STATE CAPACITANCE

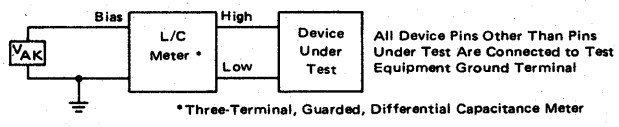


FIGURE 7 – ENABLE CURRENT (Both SCR's Must Turn On)

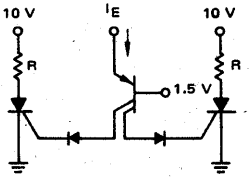


FIGURE 8 – THE CROSSPOINT SCR I-V CHARACTERISTIC (I_G = 0)

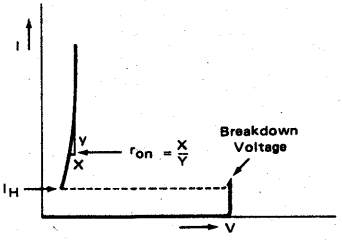
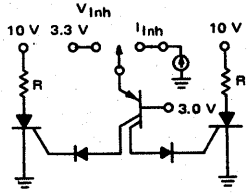


FIGURE 9 – INHIBIT VOLTAGE AND INHIBIT CURRENT (Both SCR's Must Remain OFF)



TYPICAL CHARACTERISTICS

FIGURE 10 – HOLDING CURRENT versus AMBIENT TEMPERATURE

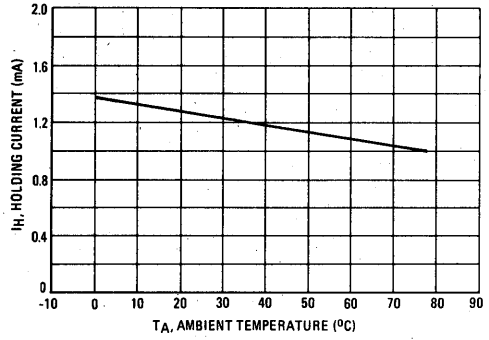


FIGURE 11 – ANODE-CATHODE ON VOLTAGE versus CURRENT AND TEMPERATURE

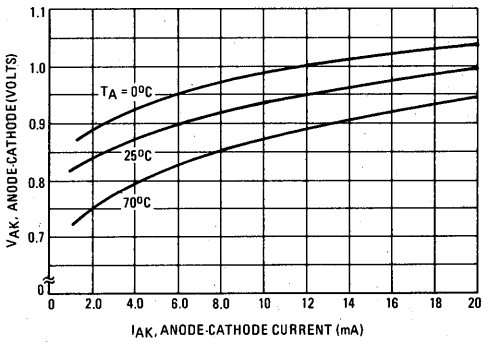


FIGURE 12 – DIFFERENCE IN ANODE-CATHODE ON VOLTAGE (Between Associate Pairs of SCR's) versus ANODE-CATHODE CURRENT

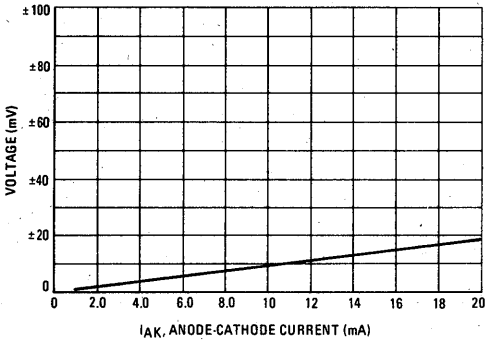


FIGURE 13 – OFF-STATE CAPACITANCE versus ANODE-CATHODE VOLTAGE

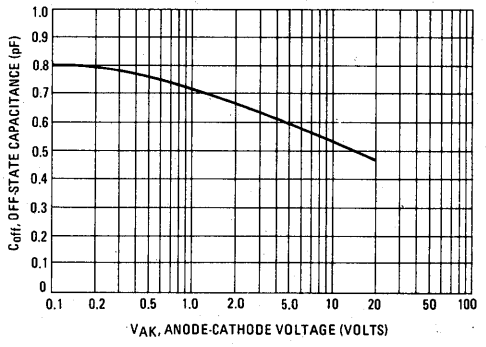


FIGURE 14 – DYNAMIC ON RESISTANCE versus ANODE-CATHODE CURRENT

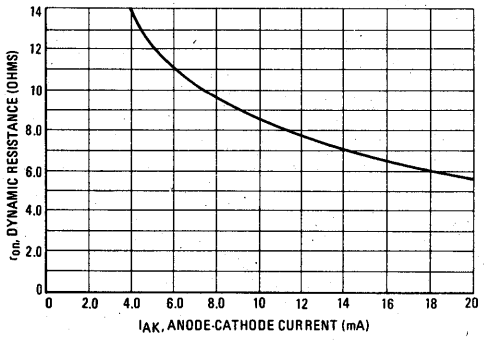


FIGURE 15 – DYNAMIC ON RESISTANCE versus AMBIENT TEMPERATURE

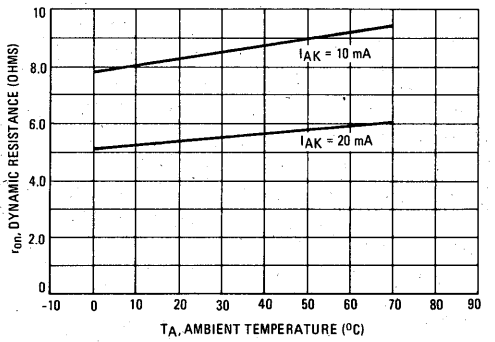


FIGURE 16 – FEEDTHROUGH versus SIGNAL FREQUENCY

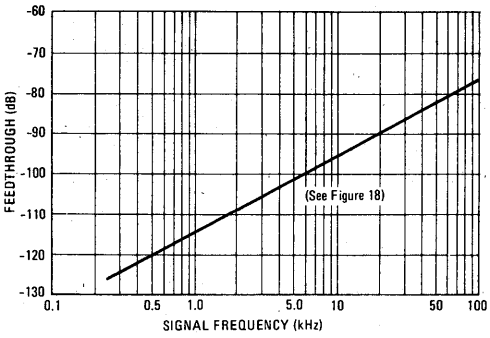


FIGURE 17 – CROSSTALK versus SIGNAL FREQUENCY

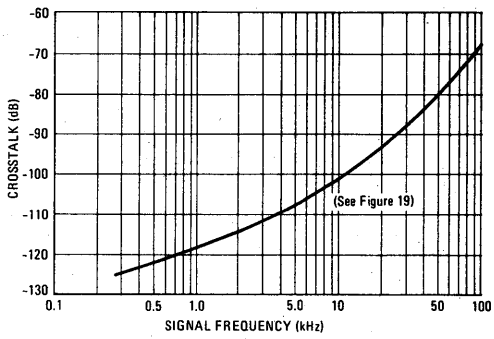
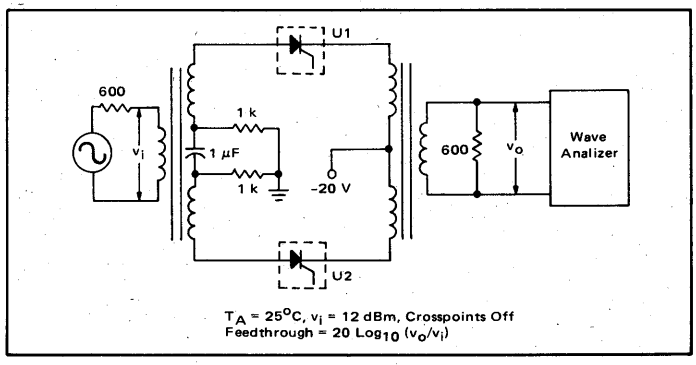
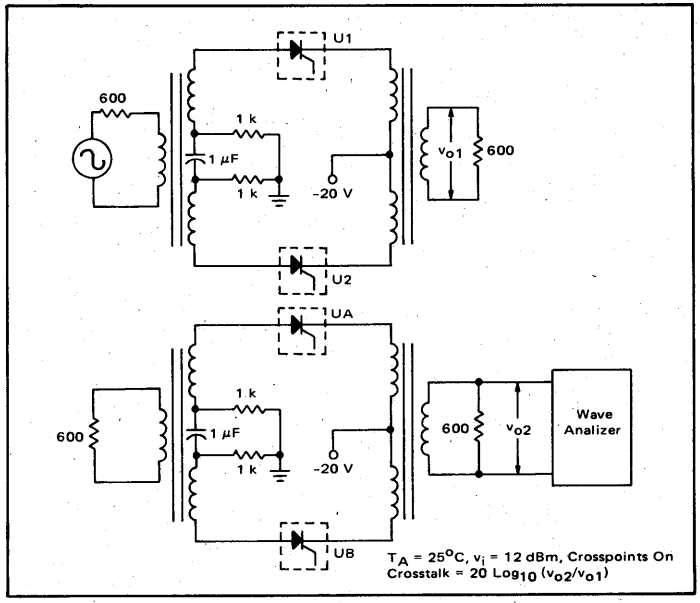


FIGURE 18 – TEST CIRCUIT FOR FEEDTHROUGH versus FREQUENCY



$T_A = 25^oC$, v_i = 12 dBm, Crosspoints Off
Feedthrough = 20 Log_{10} (v_o/v_i)

FIGURE 19 – TEST CIRCUIT FOR CROSSTALK versus FREQUENCY



$T_A = 25^oC$, v_i = 12 dBm, Crosspoints On
Crosstalk = 20 Log_{10} (v_{o2}/v_{o1})

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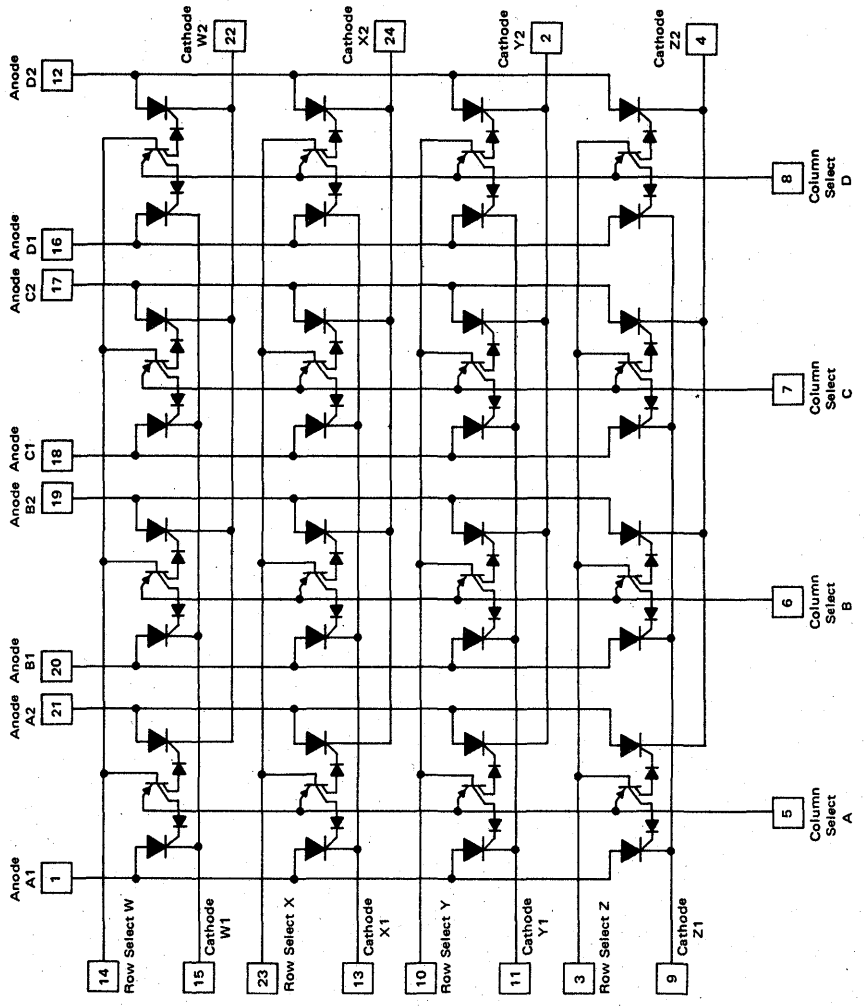
FIGURE 20 – REPRESENTATIVE SCHEMATIC DIAGRAM



TELEPHONE APPLICATION OF THE CROSSPOINT SWITCH

The MC3416 crosspoint switch is designed to provide a low-loss analog switching element for telephony signals. It can be addressed and controlled from standard binary decoders and is CMOS compatible. With proper system organization the MC3416 can significantly reduce the size and cost of existing crosspoint matrices.

SIGNAL PATH CONSIDERATIONS

The MC3416 is a balanced 4 x 4 2-wire crosspoint array. It is ideal for balanced transmission systems, but may be applied effectively in a number of single ended applications. Multiple chips may be interconnected to form larger crosspoint arrays. The major design constraint in using SCR crosspoints is that a forward dc current must be maintained through the SCR to retain an ac signal path. This requires that each subscriber-input to the array be capable of sourcing dc current as well as its ac signal. With each subscriber acting as a dc source, each trunk output then acts as a current sink. The instrument-to-trunk connection in Figure 21 shows this configuration. However, with each subscriber acting as a dc source, some method of interconnecting them without a trunk must be provided. Such a local or intercom termination is shown in Figure 22. Here both subscribers source dc current and exchange ac signals. The central current sink accepts current from both subscribers while the high output impedance of the current sink does not disturb the system.

These configurations are system compatible. The dc

FIGURE 21 – INSTRUMENT-TO-TRUNK CONNECTION

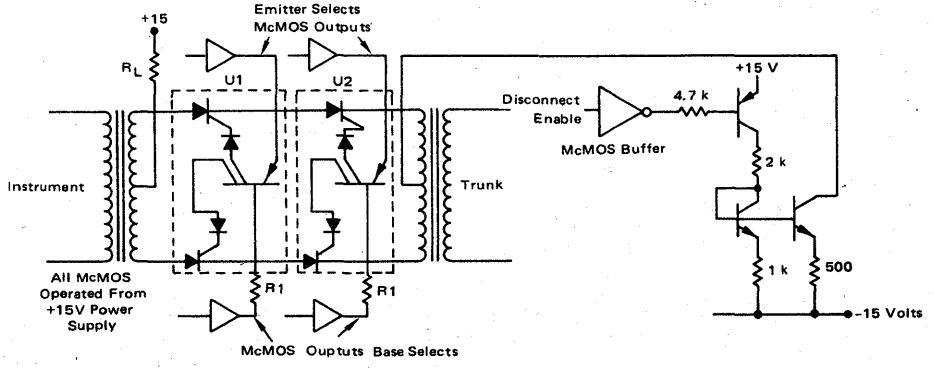
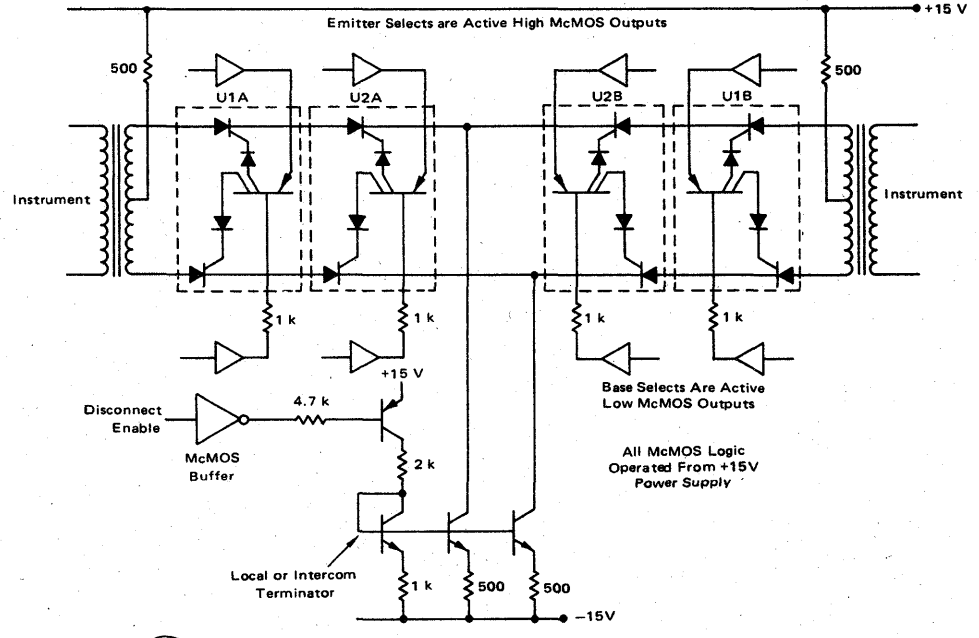


FIGURE 22 – TYPICAL INSTRUMENT TO INSTRUMENT CONNECTION

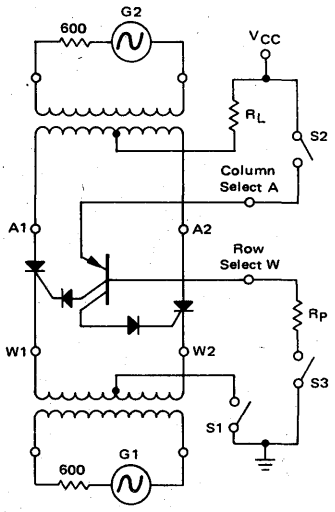


current restriction is not a restriction in the design of an efficient crosspoint array. Because of the current sink terminations, a signal path may use differing numbers of crosspoints in any connection or in two sides of the same connection further relaxing restrictions in array design.

Figure 23 demonstrates circuit operation. S1, S2, and S3 are open. The Crosspoint SCR's are off as they have no gate drive or dc current path through S1. By closing S2 and S3, gate drive is provided, but the SCR's still remain off as there is no dc current path to hold them on. Close S1 and the circuit is enabled, but with S2 and S3 off there is still no signal path. Closing S2 and S3 with S1 closed – current is injected into both gates and they switch on. DC current through R_L splits around the center-tapped winding and flows through each SCR, back through the lower winding and through S1 to ground. If S2 and S3 are opened, that current path still remains and the SCRs remain on. If an ac signal is injected at either G1 or G2, it will be transmitted to the other signal port with negligible loss in the SCR's. To disconnect the ac signal path the SCR's must be commutated off. By opening S1 the dc current path is interrupted and the SCR's switch off. The ac signal path is disconnected. With S1 closed the circuit is enabled and may be addressed again from S2 and S3. This circuit demonstrates a balanced transmission configuration. The transmission characteristics of the SCR's simulate a relay contact in that the ac signal does not incur a contact voltage drop across the crosspoint. The memory characteristics of the crosspoint are demonstrated by the selective application of S1, S2, and S3.

The selection of R_L is governed by the power supply voltage and the desired dc current. If 10 mA is to flow through each SCR then R_L must pass 20 mA. Thus, $(V_{CC} - V_{AK})/R_L = 20$ mA. The selection of R_P is governed by the characteristics for crosspoint turn on. Adequate enable current must be injected into the column select and R_P should drop at least 1.5 Volts. The PNP transistor has a typical gain of one. Thus, R_P should pass at least 2 mA to provide 4 mA column select current.

FIGURE 23– CROSSPOINT OPERATION DEMONSTRATION CIRCUIT



S1	S2	S3	LINE CONDITION
ON	X	OFF	Enabled, Not Connected
ON	OFF	X	Enabled, Not Connected
ON	ON	ON	Addressed and Connected
ON	X	X	G1 Connected to G2
OFF	X	X	Disconnected.
X = irrelevant			

ADDRESSING CONSIDERATIONS

The MC3416 crosspoint switch is addressed by selecting and turning on the PNP transistor that controls the SCR pair desired. The drive requirements of the MC3416 can be met with standard McMOS outputs. A particular crosspoint is addressed by putting a logical "1" on the emitter and a logical "0" on the base of the appropriate transistor. A resistor in the base circuit of the transistor is required to limit the current and must also drop 1.5 Volts to assure forward bias of the two diodes in the collector circuits. The gate current required for SCR turn on is 1 mA typically. The McMOS one-of-n decoders listed in Table I provide both active high and active low outputs and are well suited for standard addressing organizations. The major design constraint in organizing the addressing structure is that any signal path which is to be addressed must create a dc path from a source to a sink. If that path requires two crosspoints they must be addressed simultaneously. Of course, once the path is selected, the addressing hardware is free to initiate other signal paths. To meet the dc path

APPLICATIONS INFORMATION (continued)

requirement, crosspoint arrays should be designed in blocks such that any given dc path requires only one crosspoint per block. A signal path, however, may still use two crosspoints in the same block by sequentially addressing two dc paths to the same terminator. For example, the left or right pairs of crosspoints in Figure 22 must be addressed simultaneously but the left pair may be addressed in sequence after addressing the right pair. This is not a difficult constraint to meet and it does not require unnecessary addressing hardware.

TABLE I

	Active High Outputs	Active Low Outputs
Dual Binary to 1 of 4	MC14555	MC14556
4-bit latch/4 to 16	MC14514	MC14515
BCD to Decimal Decode	MC14028	

See Application Note AN-760 for additional applications suggestions.

DISCONNECT TECHNIQUES

Since the crosspoint switch maintains signal paths by keeping dc currents through active SCR's, disconnects are easily accomplished by interrupting the dc current path. This can be done anywhere in the circuit, but if the disconnect is done at the terminator then all signal paths established to that terminator are broken simultaneously. In both Figures 21 and 22 this is done by turning off the current sink circuit with a McMOS buffer gate. MC14049 or MC14050 buffers will drive the transistor switch. Once a disconnect is completed, the terminator may be re-enabled and used for another call. Usage of the terminators may be easily monitored with optoelectronic couplers in the collectors of the current sinks without disturbing transmission characteristics.

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THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

MC3417
MC3418

Advance Information

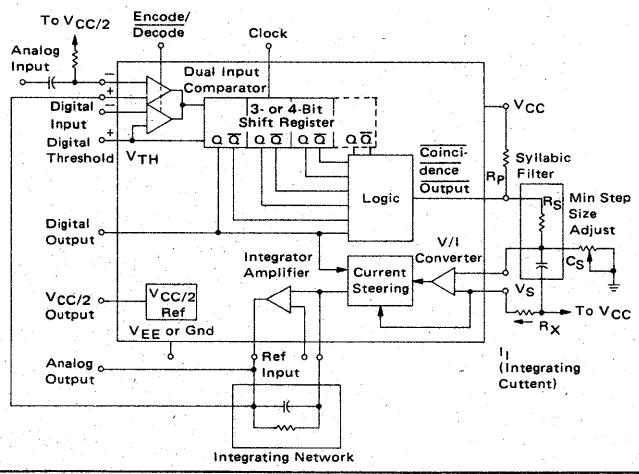
CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

- Encode and Decode Functions on the Same Chip with a Digital Input for Selection
- Utilization of Compatible I^2L – Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($\frac{V_{CC}}{2}$ reference provided on chip)
- MC3417 Has a 3 Bit Algorithm (General Communications)
- MC3418 Has a 4 Bit Algorithm (Commercial Telephone)

External Components Required:

- Integrating Network – Typically 1 ms Time Constant
- Syllabic Filter – Typically 5 ms Time Constant
- "Minimum Step Size Adjust" Resistor
- Gain Control Resistor
- Analog Input Capacitor and Resistor for Level Shifting if Input Signal Is Not Centered at $\frac{V_{CC}}{2}$

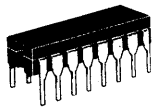
CVSD BLOCK DIAGRAM INCLUDING EXTERNAL COMPONENTS



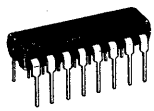
This is advance information and specifications are subject to change without notice.

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

LASER-TRIMMED INTEGRATED CIRCUIT

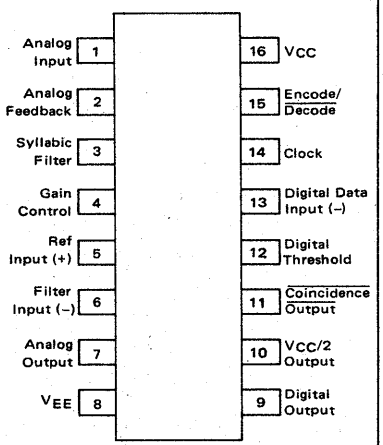


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



ORDERING INFORMATION

Temperature Range (All Types) = 0 to +70°C	
Device	**Package**
MC3417L	Ceramic DIP
MC3418L	Ceramic DIP
MC3417P	Plastic DIP
MC3418P	Plastic DIP

Note: MC3517 to be offered later in 1977.

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MAXIMUM RATINGS (All voltages referenced to V_{EE}, $T_A = 25^oC$ unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.4 to +18	Vdc
Differential Analog Input Voltage	V_{ID}	±6.0	Vdc
Digital Threshold Voltage	V_{TH}	-0.4 to V_{CC}	Vdc
Logic Input Voltage (Clock, Data, Encode/$\overline{\text{Decode}}$)	V_{Logic}	-0.4 to +18	Vdc
Coincidence Output Voltage	$V_{O(con)}$	-0.4 to +18	Vdc
Syllabic Filter Input Voltage	$V_{I(Syl)}$	-0.4 to V_{CC}	Vdc
Gain Control Input Voltage	$V_{I(GC)}$	-0.4 to V_{CC}	Vdc
Reference Input Voltage	$V_{I(Ref)}$	$\frac{V_{CC}}{2}$ -1.0 to +18	Vdc
$\frac{V_{CC}}{2}$ Output Current	I_O	-25	mA

TARGET ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, V_{EE} = Gnd, $T_A = 25^oC$ unless otherwise noted.)

Characteristic	Symbol	MC3417			MC3418			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage Range	V_{CCR}	4.75	12	16.5	4.75	12	16.5	Vdc
Power Supply Current (Idle Channel)	I_{CC}							mA
(V_{CC} = 5.0 V)		–	3.0	5.0	–	3.0	5.0	
(V_{CC} = 15 V)		–	4.0	10	–	4.0	10	
Clock Rate	SR	–	16 k	200 k	–	38 k	200 k	Samples/s
Integrating Current Range	I_{IR}							mA
($V_{CC} \leq$ 6.0 V)		0.01	–	1.5	0.01	–	1.5	
($V_{CC} \geq$ 6.0 V)		0.01	–	3.0	0.01	–	3.0	
Analog Input Range	V_I							Vdc
(4.75 V ≤ V_{CC} ≤ 15 V)		1.3	–	V_{CC} -1.3	1.3	–	V_{CC}-1.3	
Analog Output Range	V_O							Vdc
(4.75 V ≤ V_{CC} ≤ 15 V)		1.3	–	V_{CC}-1.3	1.3	–	V_{CC}-1.3	
Input Bias Currents	I_{IB}							µA
(Comparator in Active Region: $V_{pin\ 1} = V_{pin\ 10}$)								
(Analog Input)		–	0.3	1.5	–	0.3	1.5	
(Analog Feedback)		–	0.3	1.5	–	0.3	1.5	
(Syllabic Filter Input)		–	0.05	0.2	–	0.05	0.2	
(Reference Input)		–	-0.05	-0.15	–	-0.05	-0.15	
Input Offset Current (Comparator in Active Region: $V_{pin\ 1} = V_{pin\ 10}$) (Analog Input/Analog Feedback)	I_{IO}	–	0.1	0.4	–	0.1	0.3	µA
Input Offset Voltages	V_{IO}							mV
(Input Voltage Converter)		–	2.0	6.0	–	2.0	6.0	
(Integrator Amplifier)		–	1.0	4.0	–	1.0	4.0	
Transductance	gm							A/V
(Input V/I Converter (0 to 3.0 mA))		0.2	0.3	–	0.2	0.3	–	
(Integrator Amplifier (0 to ±5.0 mA))		1.0	2.0	–	1.0	2.5	–	
Propagation Delay Times								µs
(Clock Trigger to Digital Output)	t_{PLH}	–	1.5	2.5	–	1.5	2.5	
(Trigger Falling Edge, V_{CC} to +0.4 V)	t_{PHL}	–	1.0	2.5	–	1.0	2.5	
(Clock Trigger to Coincidence Output)	t_{PLH}	–	2.0	4.0	–	2.0	4.0	
(Trigger Falling Edge, V_{CC} to +0.4)	t_{PHL}	–	2.0	4.0	–	2.0	4.0	
(Clock Trigger to Ramp Reversal) (Trigger Falling Edge, V_{CC} to 0.4 V; I_{Ramp} = 100 µA)	tp	–	1.0	–	–	1.0	–	
Coincidence Output Voltage – Low Logic State ($I_{OL(Con)} \leq$ 3.0 mA)	$V_{OL(Con)}$	–	–	0.25	–	–	0.25	Vdc
Applied Digital Threshold Voltage Range	$V_{IR(th)}$	+1.2	–	V_{CC}-2.0	+1.2	–	V_{CC} - 2.0	Vdc

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ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	MC3417 Min	MC3417 Typ	MC3417 Max	MC3418 Min	MC3418 Typ	MC3418 Max	Unit
Digital Threshold Input Current ($1.2\ V \leq V_{th} \leq V_{CC} = 2.0\ V$)	$I_{IL(th)}$							μA
(V_{IL} applied to pins 13, 14 and 15)		–	–	5.0	–	–	5.0	
(V_{IH} applied to pins 13, 14 and 15)		–	-10	-50	–	-10	-50	
Maximum Integrator Output Current	$I_{OL(Int)}$	±5.0	–	–	±5.0	–	–	mA
$\frac{V_{CC}}{2}$ Generator Maximum Output Current	I_O	-10	–	–	-10	–	–	mA
$\frac{V_{CC}}{2}$ Generator Output Impedance (0 to +10 mA)	z_o	–	3.0	5.0	–	3.0	5.0	Ω
$\frac{V_{CC}}{2}$ Generator Error	ϵ_r	–	–	±2.0	–	–	±2.0	%
Logic Input Voltage								Vdc
(Low Logic State)	V_{IL}	Gnd	–	V_{th} - 0.4	Gnd	–	V_{th} - 0.4	
(High Logic State)	V_{IH}	V_{th}+0.4	–	+18	V_{th}+0.4	–	+18	
Total Loop Offset Voltage (Note 1)	ΣV_O							mV
(I_I = 33 μA, V_{CC} = 5.0 V)		–	±3.0	±7.0	–	–	–	
(I_I = 12 μA, V_{CC} = 12 V)		–	–	±2.0	–	±1.0	±2.0	
Digital Output Current								mA
(Low Logic State ($V_{OL} \leq 0.4\ V$))	I_{OL}	3.6	5.0	–	3.6	5.0	–	
(High Logic State ($V_{OH} \geq V_{CC} - 1.0\ V$))	I_{OH}	-0.35	-1.0	–	-0.35	-1.0	–	
Syllabic Filter Applied Voltage	$V_{I(Syl)}$	+3.0	–	V_{CC}	+3.0	–	V_{CC}	Vdc
Integrator Output Current								μA
(Gain Control Input Current = 12 μA)								
(Low Logic State Output)	$I_{OL(Int)}$	8.0	10	11.5	8.0	10	11.5	
(High Logic State Output)	$I_{OH(Int)}$	-11.5	-10	-8.0	-11.5	-10	-8.0	
(Gain Control Input Current = 3.0 mA)								mA
(Low Logic State Output)	$I_{OL(Int)}$	2.77	2.9	3.05	2.77	2.9	3.05	
(High Logic State Output)	$I_{OH(Int)}$	-3.05	-2.9	-2.77	-3.05	-2.9	-2.77	
Integrator Output Current Matching (Note 2) ($I_{Gain\ Control}$ = 1.5 mA)	I_{IO}	–	–	±2.0	–	–	±2.0	%
Input Current – Low Logic State (V_{IL} = 0 V)	I_{IL}	–	–	–	–	–	–	–
Input Current – High Logic State (V_{IH} = 18 V)	I_{IH}							μA
(Digital Data Input)		–	–	+5.0	–	–	+5.0	
(Clock Input)		–	–	+5.0	–	–	+5.0	
(Encode/$\overline{\text{Decode}}$ Input)		–	–	+5.0	–	–	+5.0	
Input Current – Low Logic State (V_{IL} = 0 V)	I_{IL}							μA
(Digital Data Input)		–	–	-10	–	–	-10	
(Clock Input)		–	–	-360	–	–	-360	
(Encode/$\overline{\text{Decode}}$ Input)		–	–	-36	–	–	-36	
(Clock Input, V_{IL} = 0.4 V)		–	–	-36	–	–	-36	

Note:

1. Total Loop Offset is defined as the summation of the offsets of the integrator amplifier and the analog comparator plus the effect of the integrator amplifier's bias currents flowing through 10 k input resistors and the effect of the mismatch in the positive and negative integrator currents. This mismatch causes an additional dc voltage drop in the 10 k integrator resistor. Idle channel performance is guaranteed if this total loop offset is less than one-half of the change in integrator output voltage during one clock cycle (ramp step size). Laser trimming techniques are utilized to ensure good idle channel performance.
2. The output current matching is observed with the circuit of Figure 4 by connecting pins 9 and 13 together, tieing pin 15 to a logic low level, setting up 1.5 mA into the gain control input and measuring the average voltage at pin 7 with respect to pin 10.

DEFINITIONS AND FUNCTION OF PINS

Pin 1 – Analog Input

This is the inverting comparator input where the voice signal is applied. It may be ac or dc coupled depending on the application. If the voice signal is to be level shifted to the internal reference voltage, then a bias resistor between pins 1 and 10 is used. The resistor is used to establish the reference as the new dc average of the ac coupled signal.

Pin 2 – Analog Feedback

This is the non-inverting input to the analog signal comparator within the IC. In an encoder application it should be connected to the analog output of the encoder circuit. This may be pin 7 or a low pass filter output connected to pin 7. In a decode circuit pin 2 is not used and may be tied to $V_{CC}/2$ on pin 10, ground or left open.

The analog input comparator has bias currents of 1.5 μA max, thus the driving impedances of pin 1 and 2 should be nearly equal to avoid disturbing the idle channel characteristics of the encoder.

Pin 3 – Syllabic Filter

This is the point at which the syllabic filter voltage is returned to the IC in order to control the integrator step size. It is an NPN input to an op amp. The syllabic filter consists of an RC product between pins 11 and 3. Typical values of 6 ms to 50 ms are used in voice codecs.

Pin 4 – Gain Control Input

The syllabic filter voltage appears across C_S of the syllabic filter and is the voltage between V_{CC} and pin 3. The active voltage to current (V to I) operational amplifier in the MC3417/18 drives pin 4 to the same voltage. Thus the current injected in the integrator is the syllabic filter voltage divided by the R_X resistance. The R_X resistor is then varied to adjust the loop gain of the codec and is connected to pin 4.

Pin 5 – Reference Input

This pin is the noninverting input of the integrator output. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as pin 1 and is commonly tied to the reference of pin 10. In a decoder application, it may be connected to signal ground, the reference, or any dc level within the common-mode range of the integrating op amp. It is a PNP input with a bias current of −0.15 μA maximum.

Pin 6 – Filter Input

This inverting op amp input is used to connect the integrator external components. Single integration systems require a 0.1 μF and 10 kΩ resistor between pins 6 and 7. Multipole configurations will have different circuitry, but the resistance between pins 6 and 7 should always be between 5 kΩ and 15 kΩ to maintain good idle channel characteristics.

Pin 7 – Analog Output

This is the integrator op amp output. It is capable of driving a 600-ohm load referenced to $\frac{V_{CC}}{2}$ to +6 dBm and can otherwise be treated as an op amp output. Pins 5, 6, and 7 provide full access to the integrator op amp for designing integration filter networks.

Pin 8 – V_{EE}

The MC3417/18 are designed to work in either single or dual power supply applications. Pin 8 is always connected to the most negative supply, which will be ground in a single supply system.

Pin 9 – Digital Output

The digital output provides the results of the delta modulator's conversion. It swings between V_{CC} and V_{EE} and is CMOS or TTL compatible. Pin 9 is inverting with respect to pin 1 and non-inverting with respect to pin 2. It is clocked on the falling edge of pin 14.

Pin 10 – $V_{CC}/2$ Output

An internal low impedance mid-supply reference is provided for use of the MC3417/18 in single supply applications. The internal regulator is a current source and must be loaded with a resistor to insure its sinking capability. If a +6 dBmo signal is expected across a 600 ohm input bias resistor, then pin 10 must sink 2.2 V/600Ω = 3.66 mA. This is only possible if pin 10 sources 3.66 mA into a resistor normally and will source only the difference under peak load. The reference load resistor is chosen accordingly. A 0.1 μF bypass capacitor from pin 10 to V_{EE} is also recommended. The $V_{CC}/2$ reference is capable of sourcing 10 mA and can be used as a reference elsewhere in the system circuitry.

Pin 11 – $\overline{\text{Coincidence Output}}$

The duty cycle of this pin is proportional to the voltage across C_S. The coincidence output will be low whenever the content of the internal shift register is all 1's or all 0's. In the MC3417 the register is 3 bits long while the MC3418 contains a 4 bit register. Pin 11 is an open collector of an NPN device and requires a pull-up resistor. If the syllabic filter is to have equal charge and discharge time constants, the value of R_p should be much less than R_S. In systems requiring different charge and discharge constants, the charging constant is R_SC_S while the decaying constant is $(R_S+R_p)C_S$. Thus longer decays are easily achieveable. The NPN device should not be required to sink more than 3 mA in any configuration.

5

DEFINITIONS AND FUNCTIONS OF PINS (CONT)

Pin 12 – Digital Threshold

This input sets the switching threshold in pins 13, 14, and 15. It is intended to aid in interfacing different logic families without external parts. Often it is connected to the $V_{CC}/2$ reference for CMOS interface or can be biased two diode drops above V_{EE} for TTL interface.

Pin 13 – Digital Data Input

In a decode application, the digital data stream is inputed through pin 13. In an encoder it may be unused or may be used to transmit signaling message under the control of pin 15. It is an inverting input with respect to pin 9. When pins 9 and 15 are connected, a toggle flip-flop is formed and a forced idle channel pattern can be transmitted. If pin 9 is connected to pin 11, a non 50% repetitive pattern can be transmitted and integrated at the receive end without diverging the integrator output to saturation. An MC3417 will produce a 001 pattern and the MC3418 will produce a 0001 pattern.

Pin 14 – Clock Input

The clock input determines the data rate of the codec circuit. A 32k bit rate requires a 32 kHz clock. The switching threshold of the clock input is set by pin 12. The shift register circuit toggles on the falling edge of the clock input.

Pin 15 – Encode /$\overline{\text{Decode}}$

This pin controls the connection of the analog input comparator and the digital input comparator to the internal shift register. If high, the result of the analog comparison will be clocked into the register on the falling edge at pin 14. If low, the digital input state will be entered. This allows use of the IC as an encoder-decoder or simplex codec without external parts. Furthermore, it allows non-voice patterns to be forced onto the transmission line through pin 13 in an encoder.

Pin 16 – V_{CC}

The power supply range of the MC3417/18 is from 5 to 15 volts between pin V_{CC} and V_{EE}. Guaranteed loop offset of the MC3417 is tested at 5 volts while the specification on the MC3418 is tested at 12 volts.

5

FIGURE 1 – BLOCK DIAGRAM OF THE CVSD ENCODER

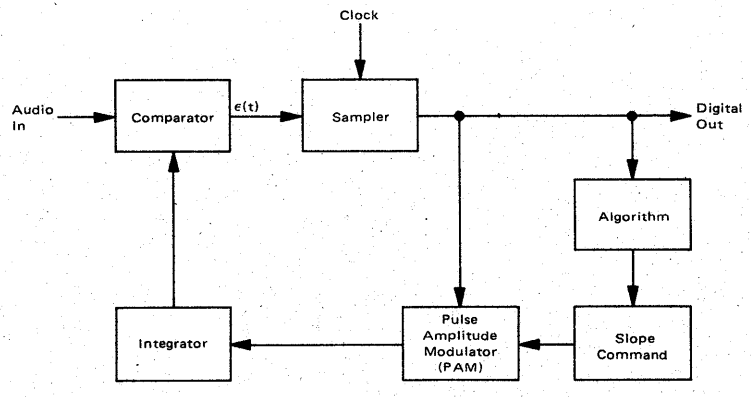


FIGURE 2 – CVDS WAVEFORMS

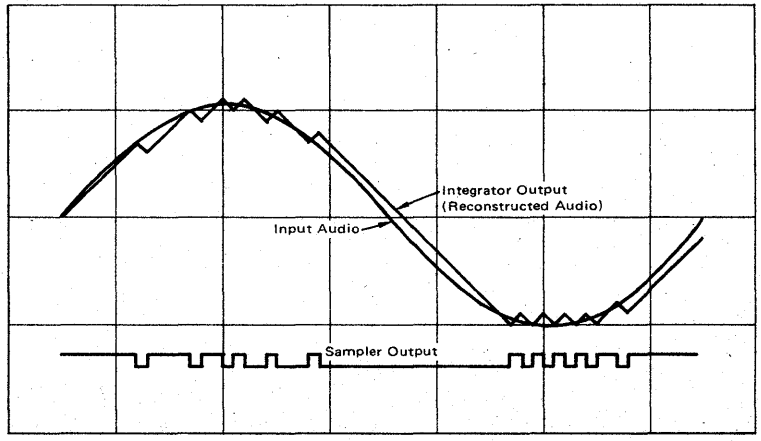


FIGURE 3 – BLOCK DIAGRAM OF THE CVSD DECODER

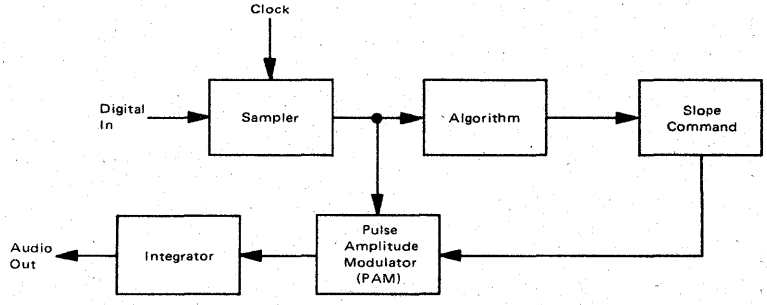
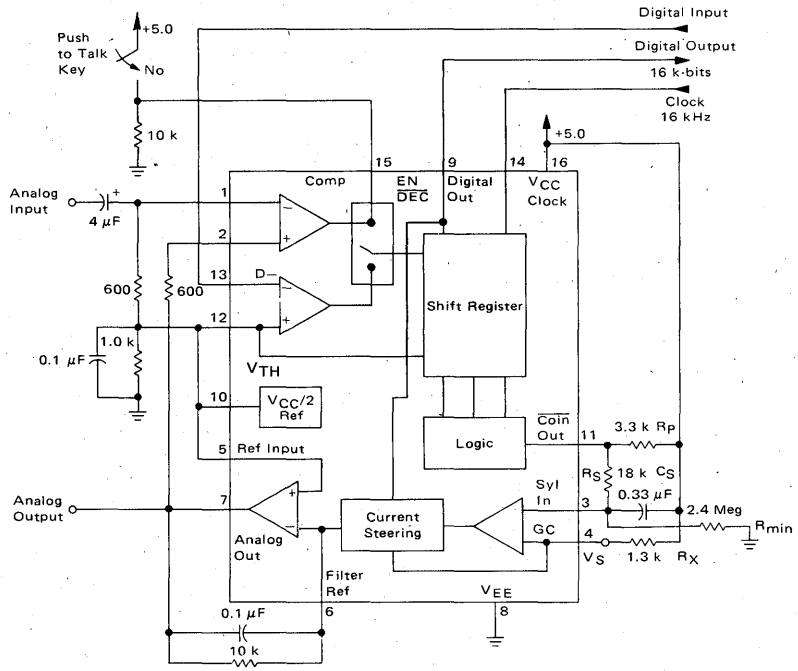


FIGURE 4 – 16 kHz SIMPLEX VOICE CODEC

(Using MC3417, Single Pole Companding and Single Integration)



CIRCUIT DESCRIPTION

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission and multiplexing, switching and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not meet the communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economically efficient means of digitizing analog inputs for transmission.

The Delta Modulator

The innermost control loop of a CVSD converter is a simple delta modulator. A block diagram CVSD Encoder is shown in Figure 1. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the integrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked so as to produce a synchronous and band limited digital bit stream.

If the clocked serial bit stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting locations tracks the input signal, the remove receiver reproduces the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise, if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4 kHz and clock rates from 8 k and up are possible. Thus the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to zero and receive restart begins without framing when the receiver reacquires. Similarly a delta modulator is tolerant of sporatic bit errors. Figure 2 shows the delta modulator waveforms while Figure 3 shows the corresponding CVSD decoder block diagram.

CIRCUIT DESCRIPTION (CONT)

The Companding Algorithm

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be band limited and amplitude limited. The frequency limitations are governed by the nyquist rate while the amplitude capabilities are set by the gain of the integrator.

The frequency limits are bounded on the upper end; that is for any input bandwidth there exists a clock frequency larger than that bandwidth which will transmit the signal with a specific noise level. However, the amplitude limits are bounded on both upper and lower ends. For a signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth the additional circuitry increases the delta modulator's dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is usually 3 or 4 bits long depending on the application. The accepted CVSD algorithm simply monitors the contents of shift register and indicates if it contains all 1's or 0's. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single pole low pass filter. The voltage output of this syllabic filter controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

The simplicity of the all ones, all zeros algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that is provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus a measure of the average input level is what is needed.

The algorithm is repeated in the receiver and thus the level data is recovered in the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If a CVSD encoder is played into a basic delta modulator, the output of the delta modulator will reflect the shape of the input signal but all of the output will be at an equal level. Thus the algorithm at the output is needed to restore the level variations. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing a voice input in a manner which is especially convenient for digital communications requirements.

CVSD DESIGN CONSIDERATIONS

A simple CVSD encoder using the MC3417 or MC3418 is shown in Figure 4. These ICs are general purpose CVSD building blocks which allow the system designer to tailor the encoders transmission characteristics to the application. Thus, the achievable transmission capabilities are constrained by the fundamental limitations of delta modulation and the design of encoder parameters. The performance is not dictated by the internal configuration of the MC3417 and MC3418. There are seven design considerations involved in designing these basic CVSD building blocks into a specific codec application.

These are listed below:

1. Selection of clock rate
2. Required number of shift register bits
3. Selection of loop gain
4. Selection of minimum step size
5. Design of integration filter transfer function
6. Design of syllabic filter transfer function
7. Design of low pass filter at the receiver

The circuit in Figure 4 is the most basic CVSD circuit possible. For many applications in secure radio or other intelligible voice channel requirements it is entirely sufficient. In this circuit, items 5 and 6 are reduced to their simplest form. The syllabic and integration filters are both single pole networks. The selection of items 1 through 4 govern the codec performance.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\,(Typ)}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst-case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient

ORDERING INFORMATION

Device	Temperature Range	Package
MC3437L	0°C to +70°C	Ceramic DIP
MC3437P	0°C to +70°C	Plastic DIP

MC3437

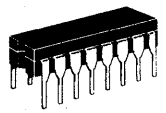
HEX BUS RECEIVER WITH INPUT HYSTERESIS

These high-speed bus receivers are useful in bus organized data transmission systems employing terminated 120 Ω lines. The receivers feature input hysteresis to obtain improved noise immunity. The receivers low input current requirement allows up to 27 driver/receiver pairs to share a common bus. A pair of Disable Inputs are provided. These Disable Inputs along with the receiver outputs are MTTL compatible.

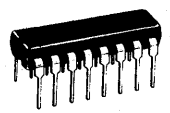
- Built in receiver hysteresis
- Receiver input threshold is not affected by temperature
- Propagation delay time – 20 ns (Typ)
- Direct Replacement for DS8837

HEX BUS RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

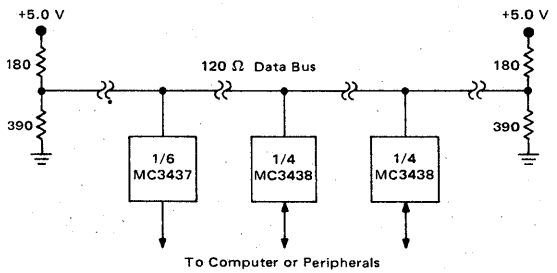


L SUFFIX
CERAMIC PACKAGE
CASE 620

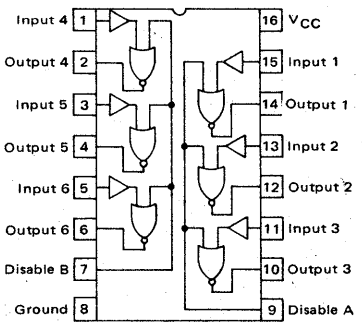


P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 – TYPICAL APPLICATION



PIN CONNECTIONS



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation Derate above 25°C	P_D	625 3.85	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

Input	Disable	Output
O	L	H
O	H	L
I	L	L
I	H	L

O = < 1.05 V
I = > 2.5 V
H = High Logic State
L = Low Logic State

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for $0 \leq T_A \leq 70^{\circ}C$ and $4.75\ V \leq V_{CC} \leq 5.25\ V$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Receiver Input Threshold Voltage — High Logic State ($V_{I(DA)} = 0.8\ V$, $I_{OL} = 16\ mA$, $V_{OL} \leq 0.4\ V$)	$V_{ILH(R)}$	1.80	2.25	2.50	V
Receiver Input Threshold Voltage — Low Logic State ($V_{I(DA)} = 0.8\ V$, $I_{OH} = -400\ \mu A$, $V_{OH} \geq 2.4\ V$)	$V_{IHL(R)}$	1.05	1.30	1.55	V
Receiver Input Current ($V_{I(R)} = 4.0\ V$, $V_{CC} = 5.25\ V$) ($V_{I(R)} = 4.0\ V$, $V_{CC} = 0\ V$)	$I_{I(R)}$	 – –	 15 1.0	 50 50	μA
Disable Input Voltage — High Logic State ($V_{I(R)} = 0.5\ V$, $V_{OL} \leq 0.4\ V$, $I_{OL} = 16\ mA$)	$V_{IH(DA)}$	2.0	–	–	V
Disable Input Voltage — Low Logic State ($V_{I(R)} = 0.5\ V$, $V_{OH} \geq 2.4\ V$, $I_{OH} = -400\ \mu A$)	$V_{IL(DA)}$	–	–	0.8	V
Output Voltage — High Logic State ($V_{I(R)} = 0.5\ V$, $V_{IL(DA)} = 0.8\ V$, $I_{OH} = -400\ \mu A$)	V_{OH}	2.4	–	–	V
Output Voltage — Low Logic State ($V_{I(R)} = 4.0\ V$, $V_{IL(DA)} = 0.8\ V$, $I_{OL} = 16\ mA$)	V_{OL}	–	0.25	0.4	V
Disable Input Current — High Logic State ($V_{IH(DA)} = 2.4\ V$) ($V_{IH(DA)} = 5.5\ V$)	$I_{IH(DA)}$	 – –	 – –	 80 2.0	 μA mA
Disable Input Current — Low Logic State ($V_{I(R)} = 4.0\ V$, $V_{IL(DA)} = 0.4\ V$)	$I_{IL(DA)}$	–	–	-3.2	mA
Output Short Circuit Current ($V_{I(R)} = 0.5\ V$, $V_{IL(DA)} = 0\ V$, $V_{CC} = 5.25\ V$)	I_{OS}	-18	–	-55	mA
Power Supply Current ($V_{I(R)} = 0.5\ V$, $V_{IL(DA)} = 0\ V$)	I_{CC}	–	45	65	mA
Input Clamp Diode Voltage ($I_{I(R)} = -12\ mA$, $I_{I(DA)} = -12\ mA$,	V_I	–	-1.0	-1.5	V

SWITCHING CHARACTERISTICS ($T_A = 25^{\circ}C$, $V_{CC} = 5.0\ V$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Receiver Input to High Logic State Output	$t_{PLH(R)}$	–	20	30	ns
Propagation Delay Time from Receiver Input to Low Logic State Output	$t_{PHL(R)}$	–	18	30	ns
Propagation Delay Time from Disable Input to High Logic State Output	$t_{PLH(DA)}$	–	9.0	15	ns
Propagation Delay Time from Disable Input to Low Logic State Output	$t_{PHL(DA)}$	–	4.0	12	ns

FIGURE 2 – SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

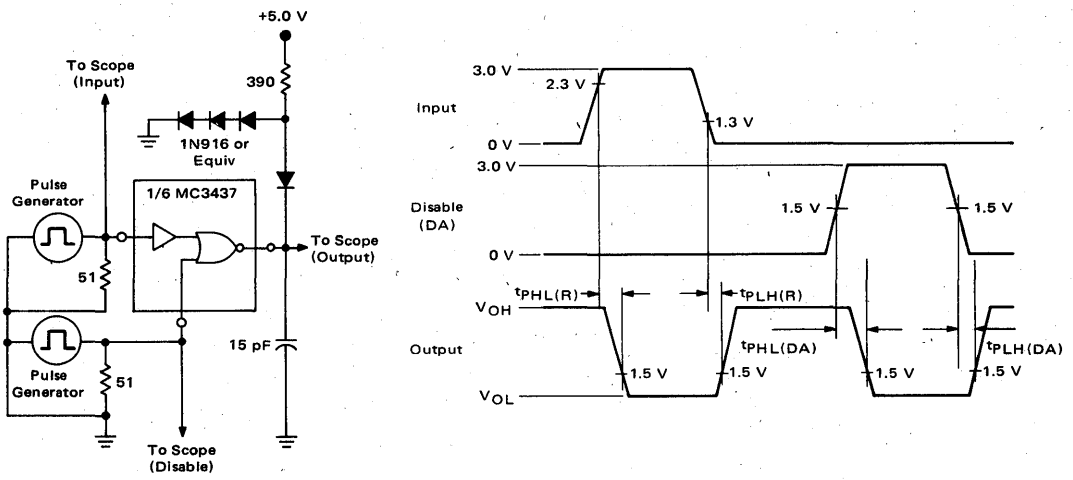
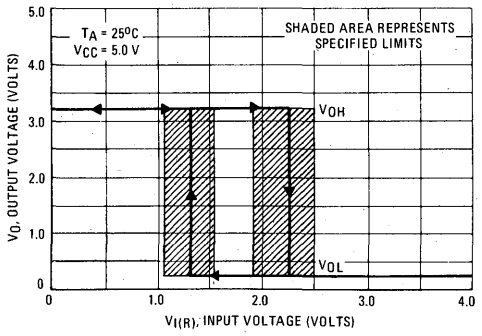
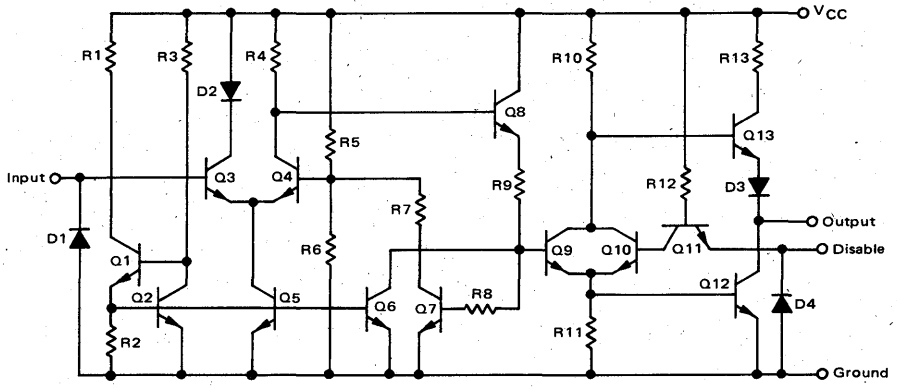


FIGURE 3 – TYPICAL HYSTERESIS



REPRESENTATIVE CIRCUIT SCHEMATIC
(1/6 Shown)



ORDERING INFORMATION

Device	Temperature Range	Package
MC3438L	0°C to +70°C	Ceramic DIP
MC3438P	0°C to +70°C	Plastic DIP

MC3438

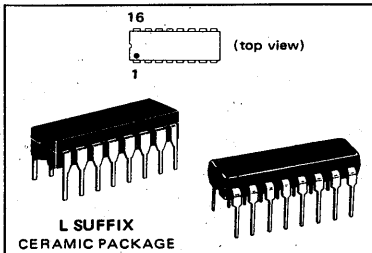
QUAD BUS TRANSCEIVER

Consists of four pair of drivers and receivers with the output of each driver connected to the input of its mating receiver. These devices are intended for use in bus organized data transmission system employing terminated 120 Ω lines. The receivers feature hysteresis to improve noise immunity. A disable function consisting of a two-input NOR gate is provided to control all four drivers.

- Receiver input threshold is not affected by temperature
- Receiver input hysteresis – 1.0 V (Typ)
- Open collector driver outputs allow wire-OR
- MTTL compatible receiver outputs and disable and driver inputs
- Driver propagation delay – 20 ns
- Receiver propagation delay – 20 ns
- Direct replacement for DS8838

QUAD BUS TRANSCEIVER

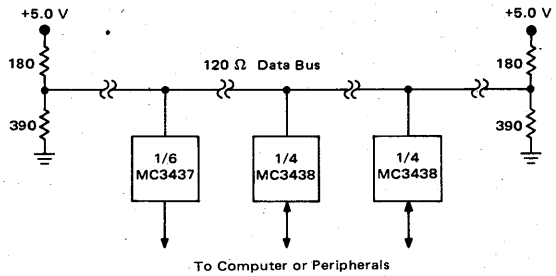
SILICON MONOLITHIC INTEGRATED CIRCUIT



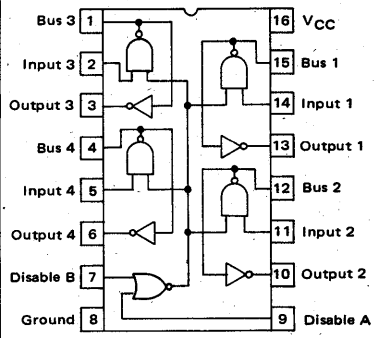
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 – TYPICAL APPLICATION



PIN CONNECTIONS



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	Vdc
Input and Output Voltage	V_O, V_I	5.5	Vdc
Power Dissipation Derate above 25°C	P_D	625 3.85	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLES

DRIVER SECTION

Disable 1	Disable 2	Input	Bus
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	H

RECEIVER SECTION

Bus	Output
$V_{IH(R)} > 2.5$ V	L
$V_{IL(R)} < 1.05$ V	H

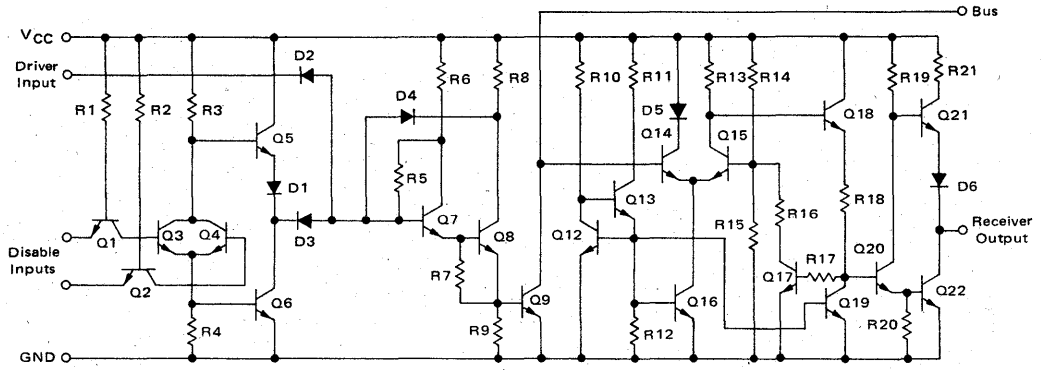
Where:
L = Low Logic State
H = High Logic State

5

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for $0 \leq T_A \leq 70^oC$ and $4.75 \leq V_{CC} \leq 5.25$ V.)

Characteristic	Symbol	Min	Typ	Max	Unit
Disable Input Voltage – High Logic State ($V_{IH(D)}$ = 2.0 V, $V_{IH(BUS)}$ = 4.0 V, $I_{BUS} < 100\ \mu A$)	$V_{IH(DA)}$	2.0	–	–	V
Disable Input Voltage – Low Logic State ($V_{IH(D)}$ = 2.0 V, $V_{IL(BUS)} \leq 0.7$ V, I_{BUS} = 50 mA)	$V_{IL(DA)}$	–	–	0.8	V
Driver Input Voltage – High Logic State ($V_{IL(DA)}$ = 0.8 V, I_{BUS} = 50 mA, $V_{IL(BUS)} \leq 0.7$ V)	$V_{IH(D)}$	2.0	–	–	V
Driver Input Voltage – Low Logic State ($V_{IL(DA)}$ = 0.8 V, $V_{IH(BUS)}$ = 4.0 V, $I_{BUS} < 100\ \mu A$)	$V_{IL(D)}$	–	–	0.8	V
Receiver Input Threshold Voltage – High Logic State ($V_{IL(D)}$ = 0.8 V, $I_{OL(R)}$ = 16 mA, $V_{OL(R)} \leq 0.4$ V)	$V_{ILH(R)}$	1.80	2.25	2.50	V
Receiver Input Threshold Voltage – Low Logic State ($V_{IL(D)}$ = 0.8 V, $I_{OH(R)}$ = -400 μA, $V_{OH(R)} \geq 2.4$ V)	$V_{IHL(R)}$	1.05	1.30	1.55	V
Disable Input Current – High Logic State ($V_{IH(D)}$ = 2.4 V, $V_{IH(DA)}$ = 2.4 V) ($V_{IH(D)}$ = 5.5 V, $V_{IH(DA)}$ = 5.5 V)	$I_{IH(DA)}$	– –	– –	40 1.0	μA mA
Driver Input Current – High Logic State ($V_{IH(DA)}$ = 2.4 V, $V_{IH(D)}$ = 2.4 V) ($V_{IH(DA)}$ = 5.5 V, $V_{IH(D)}$ = 5.5 V)	$I_{IH(D)}$	– –	– –	40 1.0	μA mA
Disable Input Current – Low Logic State ($V_{IL(DA)}$ = 0.4 V, $V_{IL(D)}$ = 0.4 V)	$I_{IL(DA)}$	–	–	-1.6	mA
Driver Input Current – Low Logic State ($V_{IL(D)}$ = 0.4 V, $V_{IL(DA)}$ = 0.4 V)	$I_{IL(D)}$	–	–	-1.6	mA
Bus Current ($V_{IL(DA)}$ = 0.8 V, $V_{IL(D)}$ = 0.8, $V_{IH(BUS)}$ = 4.0 V) (V_{CC} = 5.25 V) (V_{CC} = 0 V)	I_{BUS}	 – –	 20 2.0	 100 100	μA
Bus Voltage – Low Logic State ($V_{IL(DA)}$ = 0.8 V, $V_{IH(D)}$ = 2.0 V, I_{BUS} = 50 mA)	$V_{L(BUS)}$	–	0.4	0.7	V
Receiver Output Voltage – High Logic State ($V_{IL(DA)}$ = 0.8 V, $V_{IL(D)}$ = 0.8 V, $V_{IL(BUS)}$ = 0.5 V, $I_{OH(R)}$ = -400 μA)	$V_{OH(R)}$	2.4	–	–	V
Receiver Output Voltage – Low Logic State ($V_{IL(DA)}$ = 0.8 V, $V_{IL(D)}$ = 0.8 V, $V_{IH(BUS)}$ = 4.0 V, $I_{OL(R)}$ = 16 mA)	$V_{OL(R)}$	–	0.25	0.4	V
Receiver Output Short Circuit Current ($V_{IL(DA)}$ = 0.8 V, $V_{IL(D)}$ = 0.8 V, $V_{IL(BUS)}$ = 0.5 V, V_{CC} = 5.25 V)	$I_{OS(R)}$	-18	–	-55	mA
Power Supply Current ($V_{IL(DA)}$ = 0 V, $V_{IH(D)}$ = 2.0 V)	I_{CC}	–	50	70	mA
Input Clamp Diode Voltage ($I_{I(DA)} = I_{I(D)} = I_{BUS}$ = -12 mA)	V_I	–	-1.0	-1.5	V

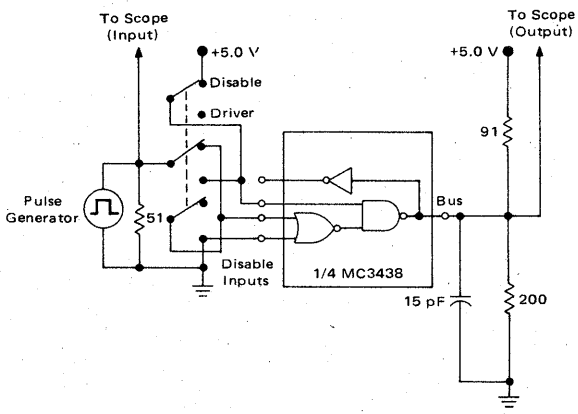
REPRESENTATIVE CIRCUIT SCHEMATIC
(1/4 Shown)



SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Disable Input to High Logic Level Output	$t_{PLH(DA)}$	–	19	27	ns
Propagation Delay Time from Disable Input to Low Logic Level Output	$t_{PHL(DA)}$	–	15	27	ns
Propagation Delay Time from Driver Input to High Logic Level Output	$t_{PLH(D)}$	–	17	25	ns
Propagation Delay Time from Driver Input to Low Logic Level Output	$t_{PHL(D)}$	–	9.0	20	ns
Propagation Delay Time from Bus Input to High Logic Level Output	$t_{PLH(R)}$	–	20	30	ns
Propagation Delay Time from Bus Input to Low Logic Level Output	$t_{PHL(R)}$	–	18	30	ns

FIGURE 2 – DRIVER AND DISABLE TEST CIRCUIT AND WAVEFORMS



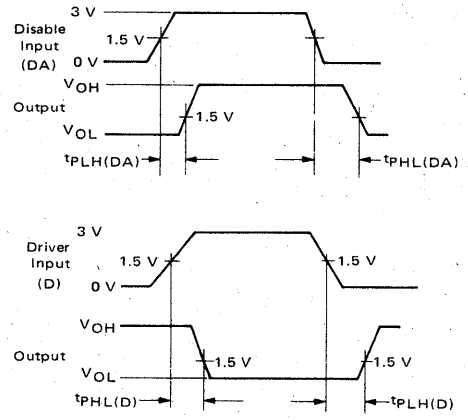
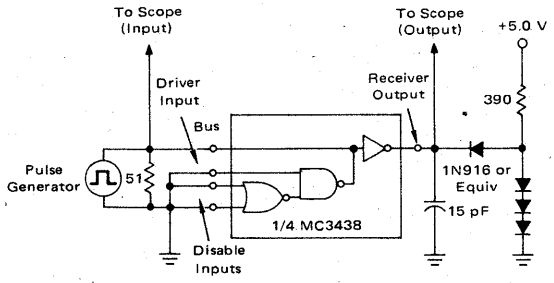


FIGURE 3 – RECEIVER TEST CIRCUIT AND WAVEFORM



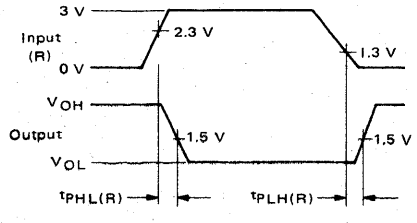
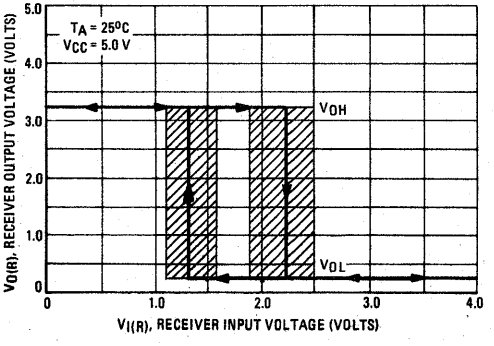


FIGURE 4 – TYPICAL RECEIVER HYSTERESIS



5

ORDERING INFORMATION

Device	Temperature Range	Package
MC3440P	0°C to +70°C	Plastic DIP
MC3441P	0°C to +70°C	Plastic DIP
MC3443P	0°C to +70°C	Plastic DIP

MC3440
MC3441
MC3443

QUAD INTERFACE BUS TRANSCEIVERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

QUAD GENERAL PURPOSE INTERFACE BUS (G.P.I.B.) TRANSCEIVERS

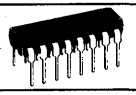
The MC3440, MC3441, MC3443 are quad bus transceivers intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. These transceivers allow the bidirectional flow of digital data and commands between the various instruments. Each of the transceiver versions provides four open-collector drivers and four receivers featuring input hysteresis.

The MC3440 version consists of three drivers controlled by a common Enable input and a single driver without an Enable input. Termination resistors are provided in the device.

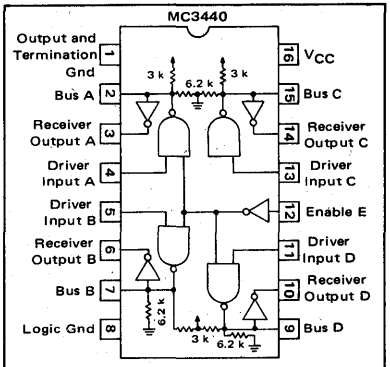
The MC3441 differs in that all four drivers are controlled by the Common Enable Input. Again, the termination resistors are provided.

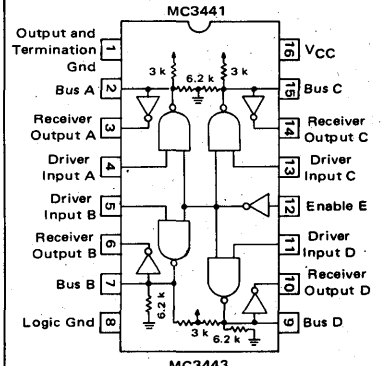
The MC3443 is identical to the MC3441 except that the termination resistors have been omitted. As such it is pin compatible, and functionally equivalent to the SN75138. It does offer the advantage of receiver input hysteresis.

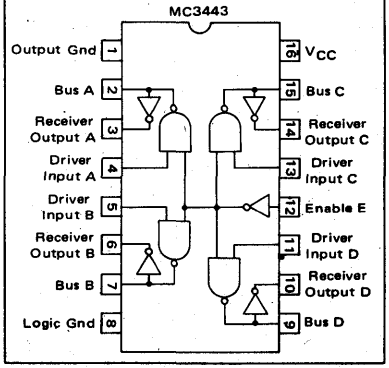
- Receiver Input Hysteresis Provides Excellent Noise Rejection.
- Open-Collector Driver Outputs Permit Wire-OR Connection.
- Tailored to Meet the Proposed Standards Set by the IEEE and IEC Committees on Instrument Interface (488-1975).
- Termination Resistors Provided (except MC3443 version).
- Provides Electrical Compatibility with Hewlett Packard Interface Bus (HP-1B).



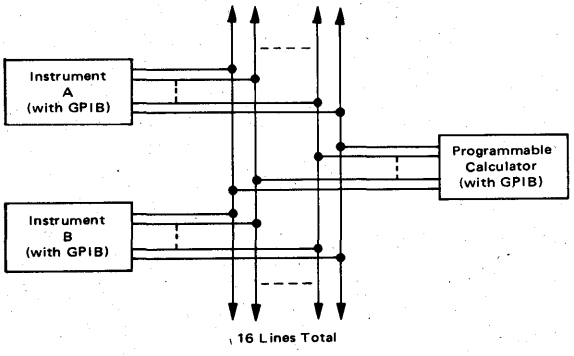
P SUFFIX
PLASTIC PACKAGE
CASE 648







TYPICAL APPLICATION – G.P.I.B. MEASUREMENT SYSTEM



5

MAXIMUM RATINGS (T_A 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Power Dissipation (Package Limitation) Derate above 25°C	P_D	830 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 4.75 V ≤ V_{CC} ≤ 5.25 V and 0 ≤ T_A ≤ 70°C, typical values are at T_A = 25°C; V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Input Voltage – High Logic State	$V_{IH(D)}$	2.0	–	–	V
Input Voltage – Low Logic State	$V_{IL(D)}$	–	–	0.8	V
Input Current – High Logic State (V_{IH} = 2.4 V)	$I_{IH(D)}$	–	–	40	μA
Input Current – Low Logic State (V_{IL} = 0.4 V, V_{CC} = 5.0 V, T_A = 25°C)	$I_{IL(D)}$	–	–	-1.6	mA
Input Clamp Voltage (I_{IC} = -12 mA)	$V_{IC(D)}$	–	–	-1.5	V
Output Voltage – High Logic State (1) ($V_{IH(S)}$ = 2.4 V or $V_{IL(D)}$ = 0.8 V)	$V_{OH(D)}$	2.6	–	–	V
Output Voltage – Low Logic State ($V_{IH(S)}$ = 2.0 V, $V_{IL(E)}$ = 0.8 V, $I_{OL(D)}$ = 48 mA) ($V_{IH(D)}$ = 2.0 V, $V_{IL(E)}$ = 0.8 V, $I_{OL(D)}$ = 100 mA)	$V_{OL(D)}$	 – –	 – –	 0.4 0.80	V
Output Leakage Current – MC3443 Only ($V_{IH(E)}$ = 2.0 V or $V_{IL(D)}$ = 0.8 V)	$I_{OH(D)}$	–	–	250	μA
RECEIVER PORTION					
Input Hysteresis	–	400	550	–	mV
Input Threshold Voltage – Low to High Output Logic State (V_{CC} = 5.0 V, T_A = 25°C)	$V_{ILH(R)}$	0.6	–	1.1	V
Input Threshold Voltage – High to Low Output Logic State (V_{CC} = 5.0 V, T_A = 25°C)	$V_{IHL(R)}$	1.5	–	–	V
Output Voltage – High Logic State ($V_{IL(R)}$ = 0.8 V, $I_{OH(R)}$ = -400 μA)	$V_{OH(R)}$	2.4	–	–	V
Output Voltage – Low Logic State ($V_{IH(R)}$ = 2.0 V, $I_{OL(R)}$ = 16 mA)	$V_{OL(R)}$	–	–	0.4	V
Output Short-Circuit Current ($V_{IL(R)}$ = 0.8 V) (Only one output may be shorted at a time)	$I_{OS(R)}$	-20	–	-55	mA
BUS TERMINATION PORTION (Does not apply to MC3443 version)					
Bus Divider Voltage ($V_{IL(D)}$ = 0 V)	$V_{(BUS)}$	2.6	3.3	3.75	V
Bus Short-Circuit Current ($V_{IL(D)}$ = 0 V, $V_{(BUS)}$ = 0 V)	$I_{OS(BUS)}$	1.25	–	2.08	mA
TOTAL DEVICE POWER CONSUMPTION					
Power Supply Current ($V_{IH(D)}$ = 2.4 V, $V_{IL(E)}$ = 0 V)	I_{CC}	–	56	75	mA

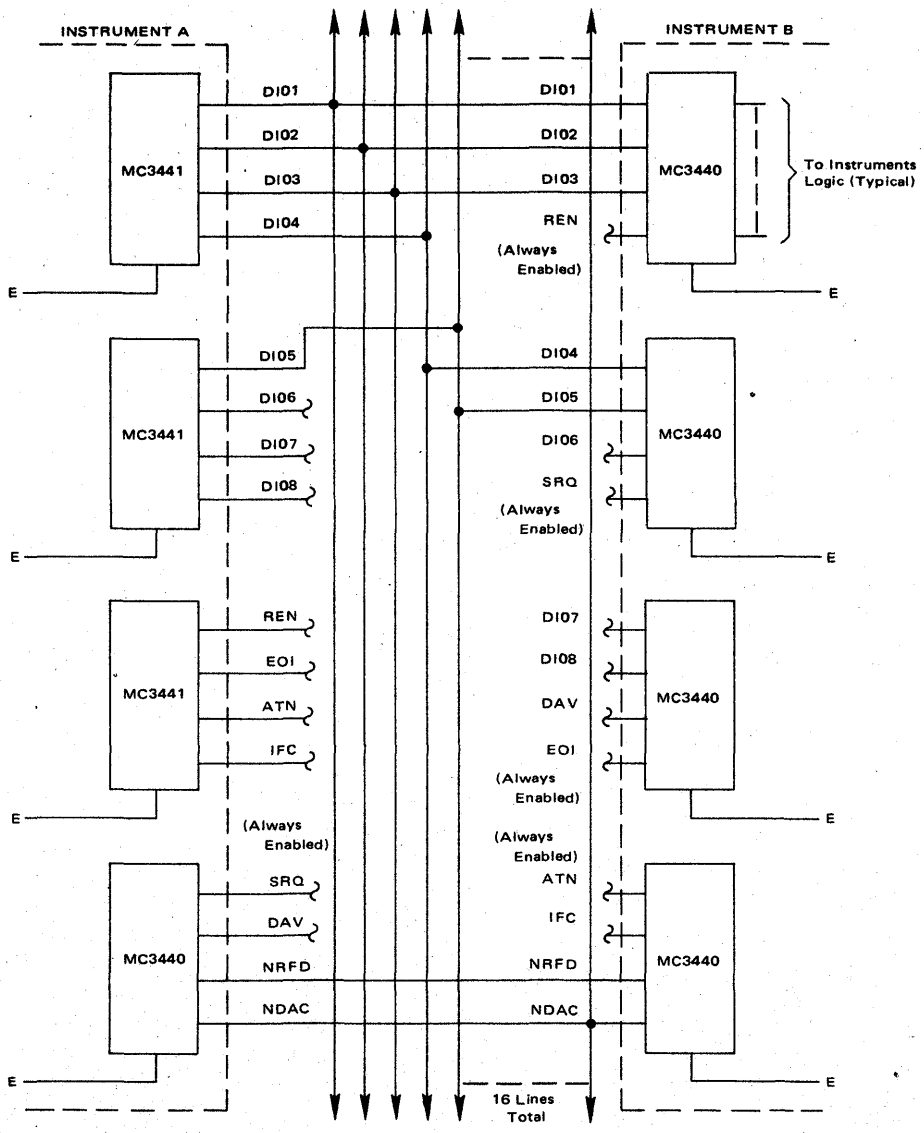
SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Symbol	MC3440, 3441			MC3443			Unit
		Min	Typ	Max	Min	Typ	Max	
DRIVER PORTION								
Propagation Delay Time from Driver Input to Low Logic State Bus Output	$t_{PHL(D)}$	–	13	30	–	13	25	ns
Propagation Delay Time from Driver Input to High Logic State Bus Output	$t_{PLH(D)}$	–	17	30	–	17	25	ns
Propagation Delay Time from Enable Input to Low Logic State Bus Output	$t_{PHL(E)}$	–	25	40	–	25	32	ns
Propagation Delay Time from Enable Input to High Logic State Bus Output	$t_{PLH(E)}$	–	25	40	–	25	32	ns
RECEIVER PORTION								
Propagation Delay Time from Bus Input to High Logic State Receiver Output	$t_{PLH(R)}$	–	15	30	–	15	22	ns
Propagation Delay Time from Bus Input to Low Logic State Receiver Output	$t_{PHL(R)}$	–	15	30	–	15	22	ns

(1) 1 3.0 k resistor from the bus terminal to V_{CC} required on the MC3443 version.

5

GENERAL PURPOSE INTERFACE BUS APPLICATION



G.P.I.B. SIGNALS:

8 Line Data Bus: DI01 – DI08

5 General Interrupt Transfer Control Bus:
- REN – Remote Enable
- SRQ – Service Request
- EOI – End or Identify
- ATN – Attention
- IFC – Interface Clear

3 Data Byte Transfer Control Bus
- DAV – Data Valid
- NRFD – Not Ready for Data
- NDAC – Not Data Accepted

16 Total Signal Lines

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER INPUT (BUS) TO OUTPUT

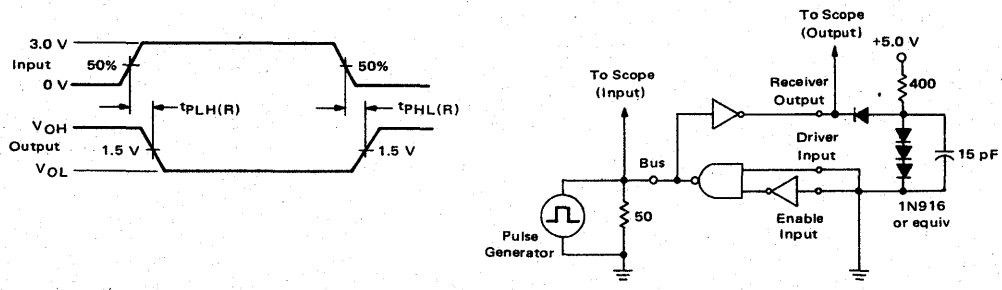


FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER AND COMMON ENABLE INPUTS TO OUTPUT (BUS)

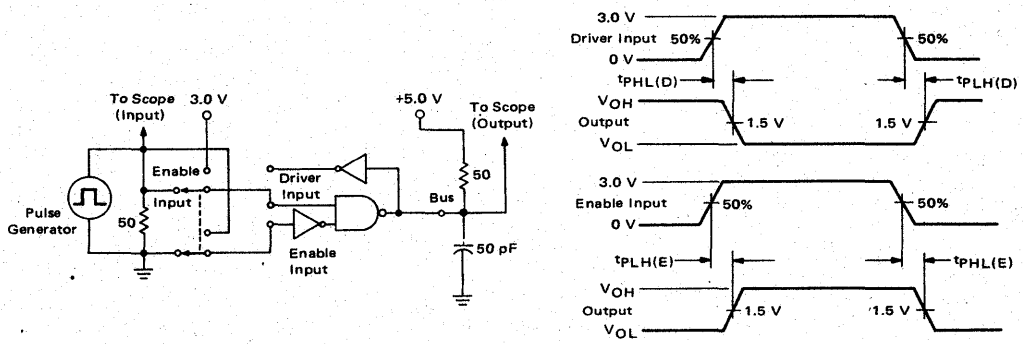


FIGURE 3 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

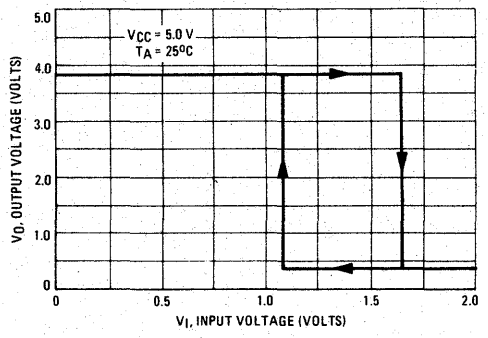
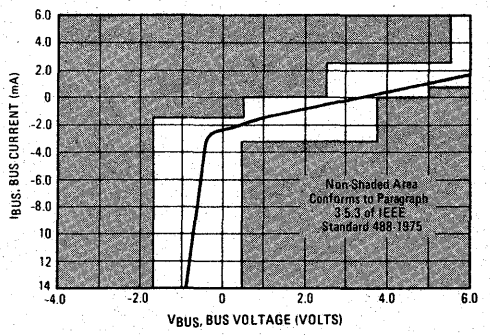


FIGURE 4 – TYPICAL BUS LOAD LINE



5

ORDERING INFORMATION

Device	Temperature Range	Package
MC3446	0°C to +70°C	Plastic DIP

MC3446

QUAD GENERAL PURPOSE INTERFACE BUS (G.P.I.B.) TRANSCEIVER

The MC3446 is a quad bus transceiver intended for usage in instruments and programmable calculators equipped for interconnection into complete measurement systems. This transceiver allows the bidirectional flow of digital data and commands between the various instruments. The transceiver provides four open-collector drivers and four receivers featuring hysteresis.

- Tailored to Meet the IEEE Standard 488-1975 (Digital Interface for Programmable Instrumentation) and the Proposed IEC Standard on Instrument Interface
- Provides Electrical Compatibility with Hewlett Packard Interface Bus. (HP-IB)
- MOS Compatible with High Impedance Inputs
- Driver Output Guaranteed Off During Power Up/Power Down
- Low Power – Average Power Supply Current = 12 mA
- Termination Resistors Provided

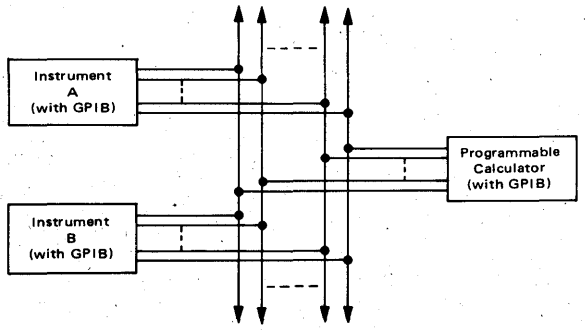
QUAD INTERFACE BUS TRANSCEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

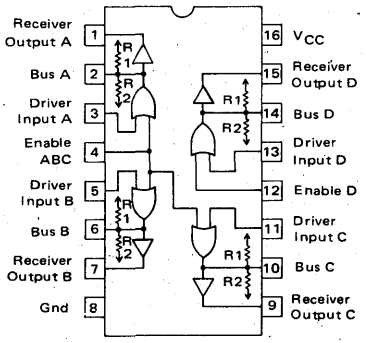
P SUFFIX
PLASTIC PACKAGE
CASE 648

5

TYPICAL MEASUREMENT SYSTEM APPLICATION



PIN CONNECTIONS



R1 = 2.4 k
R2 = 5.0 k

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 4.75 V ≤ V_{CC} ≤ 5.25 V and 0 ≤ T_A ≤ 70°C, typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Input Voltage – High Logic State	$V_{IH(D)}$	2.0	–	–	V
Input Voltage – Low Logic State	$V_{IL(D)}$	–	–	0.8	V
Input Current – High Logic State (V_{IH} = 2.4 V)	$I_{IH(D)}$	–	5.0	20	μA
Input Current – Low Logic State (V_{IL} = 0.4 V, V_{CC} = 5.0 V, T_A = 25°C)	$I_{IL(D)}$	–	0.2	0.36	mA
Input Clamp Voltage (I_{IC} = -12 mA)	$V_{IC(D)}$	–	–	-1.5	V
Output Voltage – High Logic State (1) ($V_{IH(S)}$ = 2.4 V or $V_{IH(D)}$ = 2.0 V)	$V_{OH(D)}$	2.5	3.3	3.7	V
Output Voltage – Low Logic State ($V_{IL(S)}$ = 0.8 V, $V_{IL(D)}$ = 0.8 V, $I_{OL(D)}$ = 48 mA)	$V_{OL(D)}$	–	–	0.4	
Input Breakdown Current ($V_{I(D)}$ = 5.5 V)	$I_{IB(D)}$	–	–	1.0	mA
RECEIVER PORTION					
Input Hysteresis	–	400	900	–	mV
Input Threshold Voltage – Low to High Output Logic State	$V_{ILH(R)}$	–	1.78	2.0	V
Input Threshold Voltage – High to Low Output Logic State	$V_{IHL(R)}$	0.6	0.88	–	V
Output Voltage – High Logic State ($V_{IH(R)}$ = 2.0 V, $I_{OH(R)}$ = -400 μA)	$V_{OH(R)}$	2.4	–	–	V
Output Voltage – Low Logic State ($V_{IL(R)}$ = 0.8 V, $I_{OL(R)}$ = 8.0 mA)	$V_{OL(R)}$	–	–	0.4	V
Output Short-Circuit Current ($V_{IH(R)}$ = 2.0 V) (Only one output may be shorted at a time)	$I_{OS(R)}$	4.0	–	14	mA
BUS LOAD CHARACTERISTICS					
Bus Voltage ($V_{IH(E)}$ = 2.4 V)	$V_{(BUS)}$	2.5	3.3	3.7	V
(I_{BUS} = -12 mA)		–	–	-1.5	
Bus Current ($V_{IH(O)}$ = 2.4 V, V_{BUS} ≥ 5.0 V)	$I_{(BUS)}$	0.7	–	–	mA
($V_{IH(D)}$ = 2.4 V, V_{BUS} = 0.4 V)		-1.3	–	-3.2	
(V_{BUS} ≤ 5.5 V)		–	–	2.5	
TOTAL DEVICE POWER CONSUMPTION					
Power Supply Current	I_{CC}	–	12	19	mA
(All Drivers OFF)		–	32	39	
(All Drivers ON)					

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER PORTION					
Propagation Delay Time from Driver Input to Low Logic State Bus Output	$t_{PHL(D)}$	–	34	50	ns
Propagation Delay Time from Driver Input to High Logic State Bus Output	$t_{PLH(D)}$	–	17	40	ns
Propagation Delay Time from Enable Input to Low Logic State Bus Output	$t_{PHL(E)}$	–	39	50	ns
Propagation Delay Time from Enable Input to High Logic State Bus Output	$t_{PLH(E)}$	–	32	50	ns
RECEIVER PORTION					
Propagation Delay Time from Bus Input to High Logic State Receiver Output	$t_{PLH(R)}$	–	37	50	ns
Propagation Delay Time from Bus Input to Low Logic State Receiver Output	$t_{PHL(R)}$	–	22	40	ns

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER INPUT (BUS) TO OUTPUT

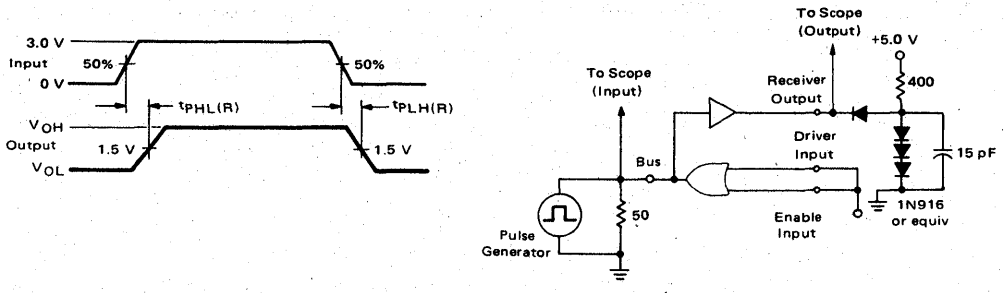


FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER AND COMMON ENABLE INPUTS TO OUTPUT (BUS)

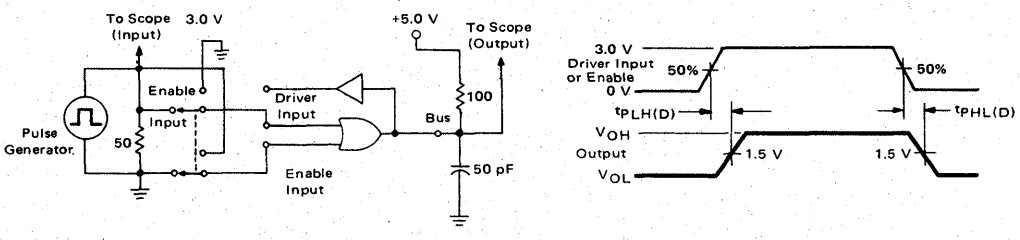


FIGURE 3 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

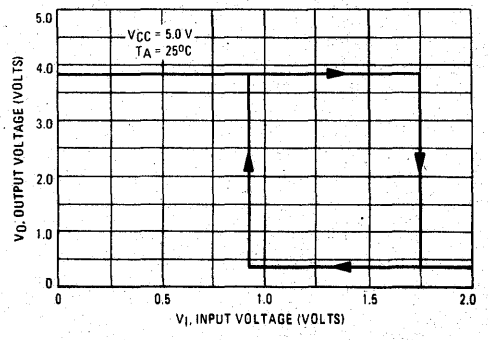
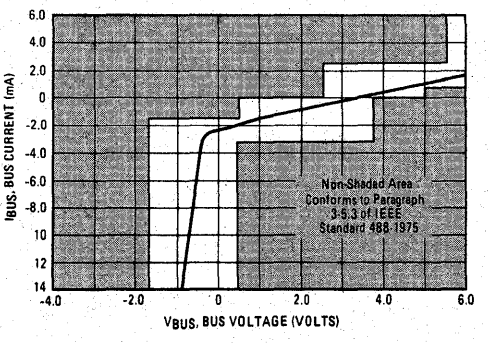


FIGURE 4 – TYPICAL BUS LOAD LINE



XC3448

Product Preview

BIDIRECTIONAL INSTRUMENTATION BUS (HP-IB) TRANSCEIVER

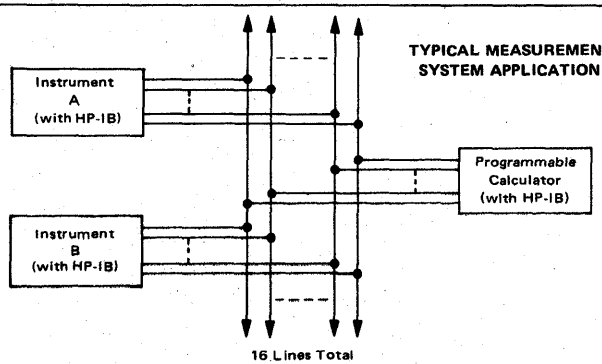
This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1975 often referred to as HP-IB). The required bus termination is internally provided.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by its corresponding Send/Receive input with the disabled output of the pair forced to a high impedance state. An additional option allows the driver outputs to be operated in an open collector or active pull-up configuration. The receivers have input hysteresis to improve on noise margin and their input loading follows the bus standard specifications.

- Four Independent Driver/Receiver Pairs
- Three State Outputs
- High Impedance Inputs – I_{IH} = 40 μA (Typ)
- Receiver Hysteresis – 650 mV (Typ)
- Fast Propagation Times – 20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output Option
- Power Up/Power Down Protection (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power Is Removed From Device
- Required Termination Characteristics Provided

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

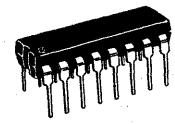


TYPICAL MEASUREMENT SYSTEM APPLICATION

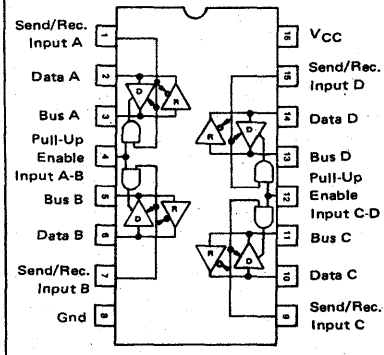
This is advance information and specifications are subject to change without notice.

QUAD THREE-STATE BUS TRANSCEIVER WITH TERMINATION NETWORKS

Silicon Monolithic Integrated Circuit



CASE 648
P SUFFIX
PLASTIC PACKAGE



TRUTH TABLE

Send/Rec.	Enable	Info. Flow	Comments
0	X	Bus → Data	–
1	1	Data → Bus	Active Pull-Up
1	0	Data → Bus	Open Col.

X = Don't Care

5

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 4.75 V ≤ V_{CC} ≤ 5.25 V and 0 ≤ T_A ≤ 70°C, typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
Bus Voltage					
(Bus Pin Open) ($V_{I(S/R)}$ = 0.8 V	$V_{(BUS)}$	2.5	3.3	3.7	V
(I_{BUS}) = -12 mA)	$V_{IC(BUS)}$	–	-0.5	-1.5	V
Bus Current	$I_{(BUS)}$				mA
($V_{(BUS)}$ ≥ 5.5 V)		0.7	–	2.5	
($V_{(BUS)}$ = 0.4 V)		-1.3	–	-3.2	
(V_{CC} = 0 V, 0 V ≤ $V_{(BUS)}$ ≤ 5.25 V)		–	–	-0.04	
Receiver Input Hysteresis ($V_{I(S/R)}$ = 0.4 V)	–	400	650	–	mV
Receiver Input Threshold					V
($V_{I(S/R)}$ = 0.4 V, Low to High)	$V_{ILH(R)}$	–	1.75	2.0	
($V_{I(S/R)}$ = 0.4 V, High to Low)	$V_{IHL(R)}$	0.8	1.1	–	
Receiver Output Voltage – High Logic State ($V_{I(S/R)}$ = 0.4 V, $I_{OH(R)}$ = -400 μA; $V_{(BUS)}$ = 2.0 V)	$V_{OH(R)}$	2.7	–	–	V
Receiver Output Voltage – Low Logic State ($V_{I(S/R)}$ = 0.4 V, $I_{OL(R)}$ = 16 mA, $V_{(BUS)}$ = 0.8 V)	$V_{OL(R)}$	–	–	0.4	V
Receiver Output Short Circuit Current ($V_{I(S/R)}$ = 0.4 V, $V_{(BUS)}$ = 2.0 V)	$I_{OS(R)}$	-20	–	-55	mA
Driver Input Voltage – High Logic State ($V_{I(S/R)}$ = 2.0 V)	$V_{IH(D)}$	2.0	–	–	V
Driver Input Voltage – Low Logic State ($V_{I(S/R)}$ = 2.0 V)	$V_{IL(D)}$	–	–	0.8	V
Driver Input Current	$I_{I(D)}$				μA
($V_{I(S/R)}$ = 2.0 V, 0.4 V ≤ $V_{I(D)}$ ≤ 4.5 V)		-40	–	40	
($V_{I(S/R)}$ = 2.0 V, 0.4 V ≤ $V_{I(D)}$ = 5.5 V)		–	–	2000	
Driver Input Clamp Voltage ($V_{I(S/R)}$ = 2.0 V, $I_{IC(D)}$ = -18 mA)	$V_{IC(D)}$	–	-0.5	-1.5	V
Driver Output Voltage – High Logic State ($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V, I_{OH} = -5.2 mA)	$V_{OH(D)}$	2.5	3.8	–	V
Driver Output Voltage – Low Logic State ($V_{I(S/R)}$ = 2.0 V, $I_{OL(D)}$ = 48 mA)	$V_{OL(D)}$	–	–	0.4	V
Output Short-Circuit Current ($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V)	$I_{OS(D)}$	-20	–	-55	mA
Power Supply Current	I_{CC}				mA
(Listening Mode – All Receivers On)		–	65	90	
(Talking Mode – All Drivers On)		–	95	120	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay of Driver					ns
(Output Low to High)	$t_{PLH(D)}$	–	13	25	
(Output High to Low)	$t_{PHL(D)}$	–	26	35	
Propagation Delay of Receiver					ns
(Output Low to High)	$t_{PLH(R)}$	–	23	35	
(Output High to Low)	$t_{PHL(R)}$	–	21	35	
Propagation Delay Time – R/W to Data					ns
Logic High to Third State	$t_{PHZ(R)}$	–	20	–	
Third State to Logic High	$t_{PZH(R)}$	–	7.0	–	
Logic Low to Third State	$t_{PLZ(R)}$	–	30	–	
Third State to Logic Low	$t_{PZL(R)}$	–	20	–	
Propagation Delay Time – R/W to Bus					ns
Logic High to Third State	$t_{PHZ(D)}$	–	20	–	
Third State to Logic High	$t_{PZH(D)}$	–	20	–	
Logic Low to Third State	$t_{PLZ(D)}$	–	40	–	
Third State to Logic Low	$t_{PZL(D)}$	–	25	–	

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

FIGURE 1 – BUS INPUT TO DATA OUTPUT (RECEIVER)

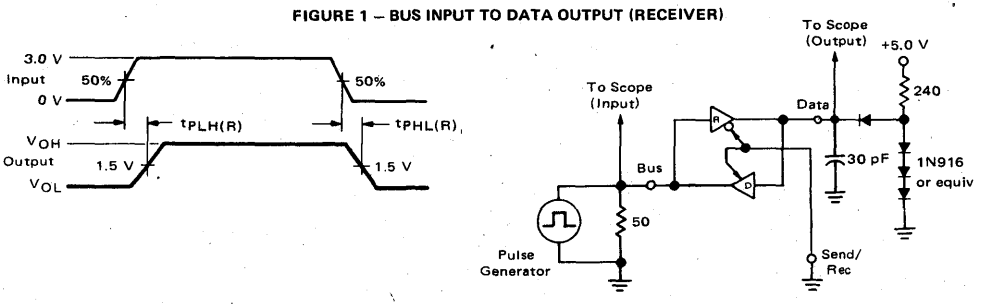


FIGURE 2 – DATA INPUT TO BUS OUTPUT (DRIVER)

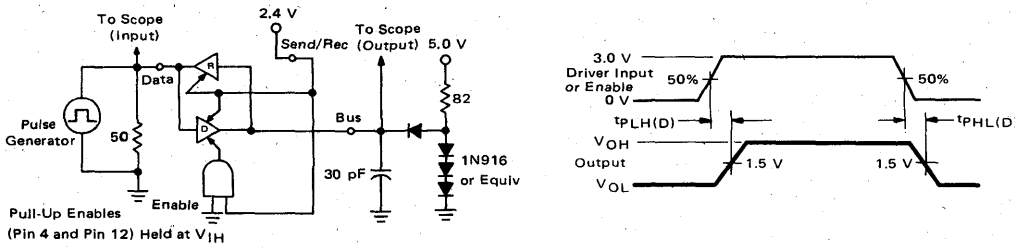


FIGURE 3 – SEND/RECEIVE INPUT TO BUS OUTPUT (DRIVER)

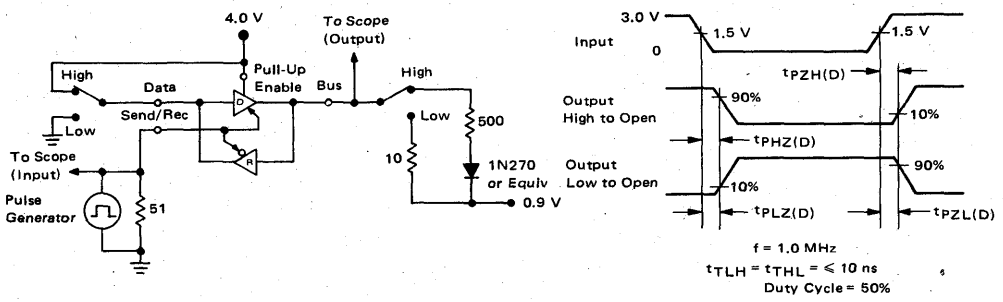


FIGURE 4 – SEND/RECEIVE INPUT TO DATA OUTPUT (RECEIVER)

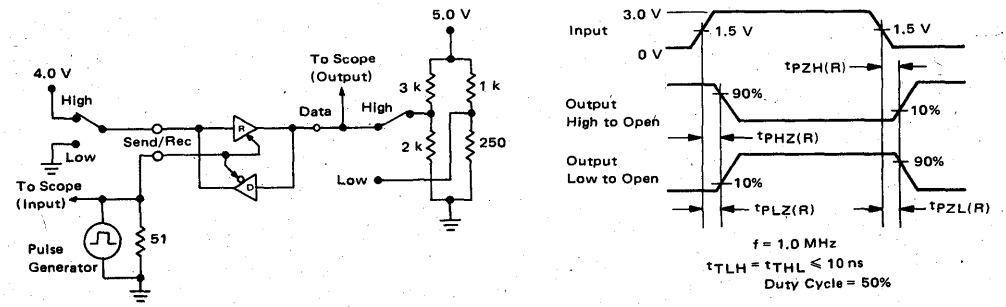


FIGURE 5 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

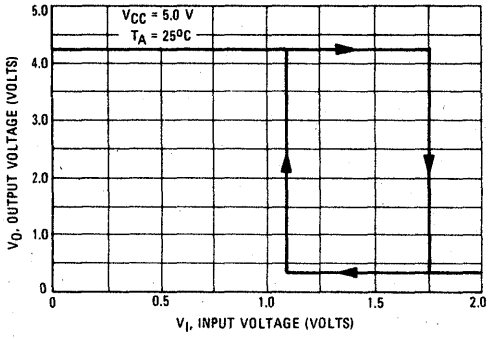
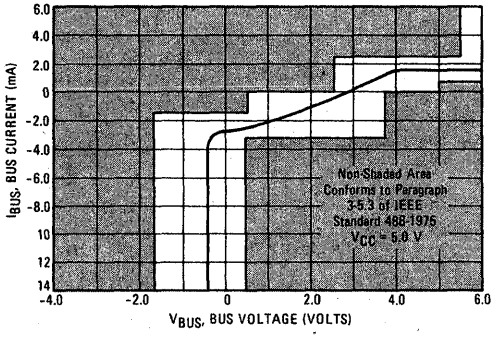


FIGURE 6 – TYPICAL BUS LOAD LINE



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

ORDERING INFORMATION

Device	Temperature Range	Package
MC3450L	0°C to +70°C	Ceramic DIP
MC3450P	0°C to +70°C	Plastic DIP
MC3452L	0°C to +70°C	Ceramic DIP
MC3552P	0°C to +70°C	Plastic DIP

MC3450
MC3452

Specifications and Applications Information

QUAD LINE RECEIVERS
WITH COMMON THREE-STATE
STROBE INPUT

SILICON MONOLITHIC
INTEGRATED CIRCUITS

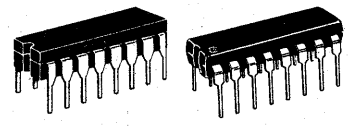
QUAD MTTL COMPATIBLE LINE RECEIVERS

The MC3450 features four MC75107 type active pullup line receivers with the addition of a common three-state strobe input. When the strobe input is at a logic zero, each receiver output state is determined by the differential voltage across its respective inputs. With the strobe high, the receiver outputs are in the high impedance state.

The MC3452 is the same as the MC3450 except that the outputs are open collector which permits the implied "AND" function.

The strobe input on both devices is buffered to present a strobe loading factor of only one for all four receivers and inverted to provide best compatability with standard decoder devices.

- Receiver Performance Identical to the Popular MC75107/MC75108 Series
- Four Independent Receivers with Common Strobe Input
- Implied "AND" Capability with Open Collector Outputs
- Useful as a Quad 1103 type Memory Sense Amplifier



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

CONNECTION DIAGRAM

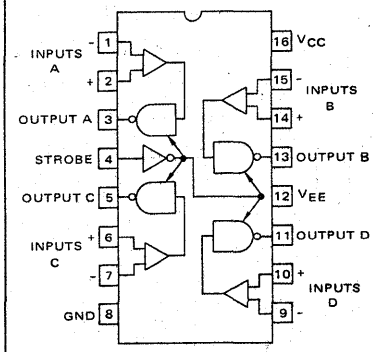
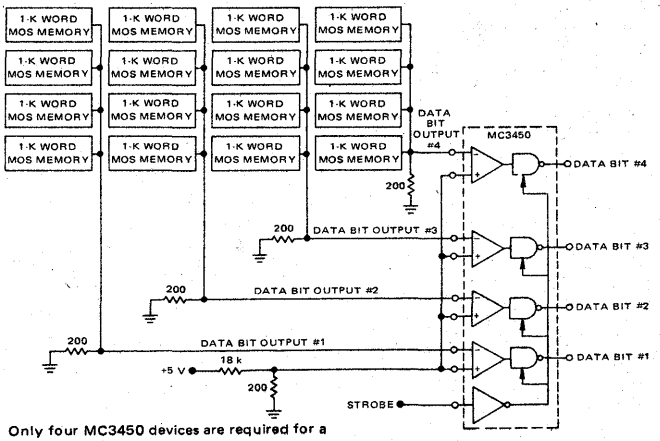


FIGURE 1 – A TYPICAL MOS MEMORY SENSING APPLICATION FOR A 4-K WORD BY 4-BIT MEMORY ARRANGEMENT EMPLOYING 1103 TYPE MEMORY DEVICES



Only four MC3450 devices are required for a 4-k word by 16-bit memory system.

TRUTH TABLE

INPUT	STROBE	OUTPUT MC3450	OUTPUT MC3452
$V_{ID} \geq$ +25 mV	L	H	Off
	H	Z	Off
-25 mV $\leq V_{ID} \leq$ +25 mV	L	I	I
	H	Z	Off
$V_{ID} \leq$ -25 mV	L	L	L
	H	Z	Off

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
I = Indeterminate State

5

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±7.0	Vdc
Differential-Mode Input Signal Voltage Range	V_{IDR}	±6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T_A = +25°C Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 1000 6.6 1000 6.6	 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Vdc
Output Load Current	I_{OL}	–	–	16	mA
Differential-Mode Input Voltage Range	V_{IDR}	-5.0	–	+5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	-3.0	–	+3.0	Vdc
Input Voltage Range (any input to Ground)	V_{IR}	-5.0	–	+3.0	Vdc

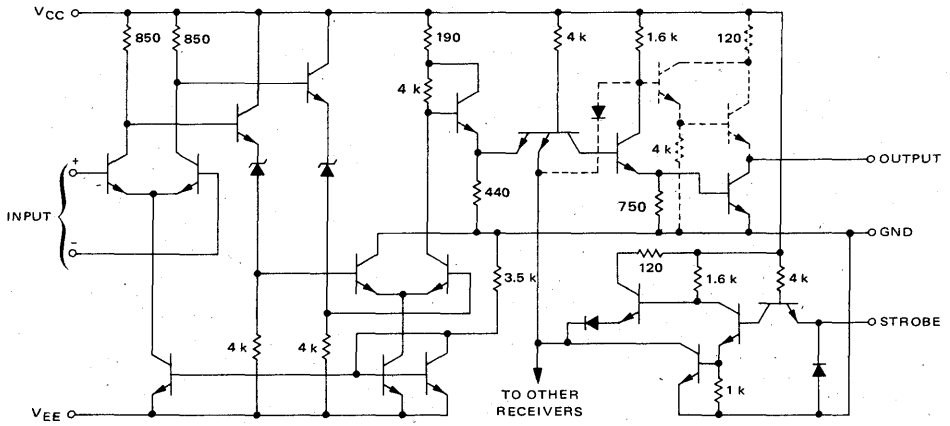
ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Fig.	MC3450			MC3452			Unit
			Min	Typ	Max	Min	Typ	Max	
High Level Input Current to Receiver Input	$I_{IH(I)}$	7	–	–	75	–	–	75	μA
Low Level Input Current to Receiver Input	$I_{IL(I)}$	8	–	–	-10	–	–	-10	μA
High Level Input Current to Strobe Input $V_{IH(S)}$ = +2.4 V $V_{IH(S)}$ = +5.25 V	$I_{IH(S)}$	5	 – –	 – –	 40 1.0	 – –	 – –	 40 1.0	 μA mA
Low Level Input Current to Strobe Input $V_{IH(S)}$ = +0.4 V	$I_{IL(S)}$	5	–	–	-1.6	–	–	-1.6	mA
High Level Output Voltage	V_{OH}	3	2.4	–	–	–	–	–	Vdc
High Level Output Leakage Current	I_{CEX}	3	–	–	–	–	–	250	μA
Low Level Output Voltage	V_{OL}	3	–	–	0.4	–	–	0.4	Vdc
Short-Circuit Output Current	I_{OS}	6	-18	–	-70	–	–	–	mA
Output Disable Leakage Current	I_{off}	9	–	–	40	–	–	–	μA
High Logic Level Supply Current from V_{CC}	I_{CCH}	4	–	45	60	–	45	60	mA
High Logic Level Supply Current from V_{EE}	I_{EEH}	4	–	-17	-30	–	-17	-30	mA

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Fig.	MC3450			MC3452			Unit
			Min	Typ	Max	Min	Typ	Max	
High to Low Logic Level Propagation Delay Time (Differential Inputs)	$t_{PHL(D)}$	10	–	–	25	–	–	25	ns
Low to High Logic Level Propagation Delay Time (Differential Inputs)	$t_{PLH(D)}$	10	–	–	25	–	–	25	ns
Open State to High Logic Level Propagation Delay Time (Strobe)	$t_{PZH(S)}$	11	–	–	21	–	–	–	ns
High Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PHZ(S)}$	11	–	–	18	–	–	–	ns
Open State to Low Logic Level Propagation Delay Time (Strobe)	$t_{PZL(S)}$	11	–	–	27	–	–	–	ns
Low Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PLZ(S)}$	11	–	–	29	–	–	–	ns
High Logic to Low Logic Level Propagation Delay Time (Strobe)	$t_{PHL(S)}$	12	–	–	–	–	–	25	ns
Low Logic to High Logic Level Propagation Delay Time (Strobe)	$t_{PLH(S)}$	12	–	–	–	–	–	25	ns

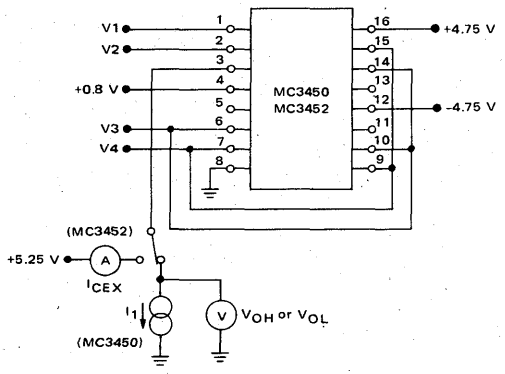
FIGURE 2 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



Dashed components apply to the MC3450 circuit only.

TEST CIRCUITS

FIGURE 3 – I_{CEX}, V_{OH}, AND V_{OL}



TEST TABLE

	V1		V2		V3		V4		
	MC3450*	MC3452	MC3450	MC3452	MC3450	MC3452	MC3450	MC3452	I1
V_{OH}	+2.975 V	–	+3.0 V	–	+3.0 V	–	GND	–	+0.4 mA
	-3.0 V	–	-2.975 V	–	GND	–	-3.0 V	–	
I_{CEX}	–	+2.975 V	–	+3.0 V	–	+3.0 V	–	GND	–
	–	-3.0 V	–	-2.975 V	–	GND	–	-3.0 V	–
V_{OL}	+3.0 V	+3.0 V	+2.975 V	+2.975 V	GND	GND	+3.0 V	+3.0 V	-16 mA
	-2.975 V	-2.975 V	-3.0 V	-3.0 V	-3.0 V	-3.0 V	GND	GND	

Channel A shown under test. Other channels are tested similarly.

FIGURE 4 – I_{CCH} AND I_{EEH}

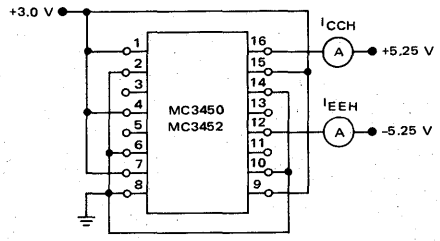
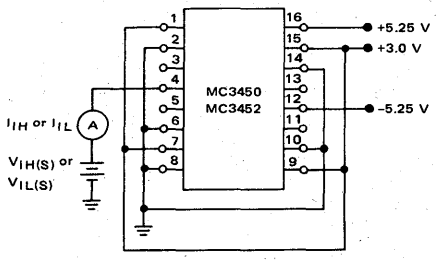
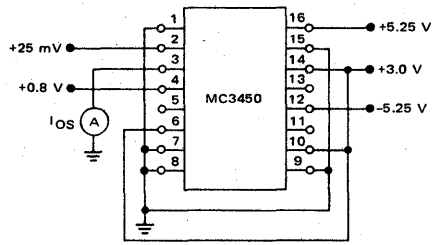


FIGURE 5 – $I_{IH(S)}$ AND $I_{IL(S)}$



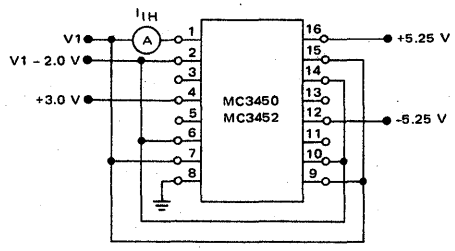
TEST CIRCUITS (continued)

FIGURE 6 – I_{OS}



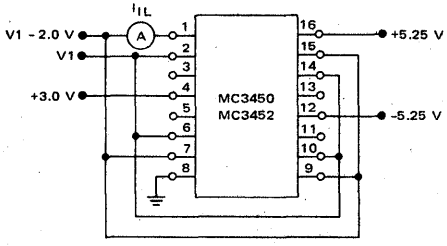
Channel A shown under test, other channels are tested similarly. Only one output shorted at a time.

FIGURE 7 – I_{IH}



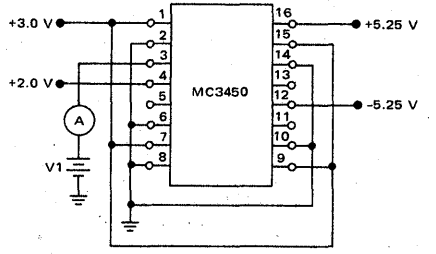
Channel A(–) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0 V to –3.0 V.

FIGURE 8 – I_{IL}



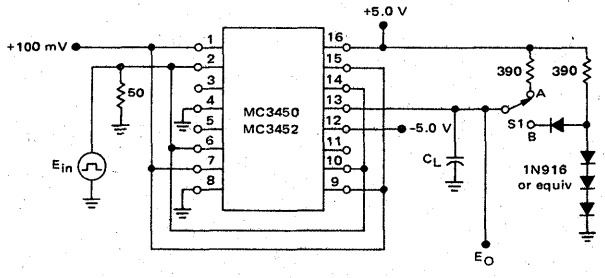
Channel A(–) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0 V to –3.0 V.

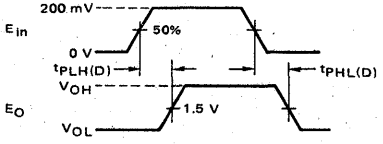
FIGURE 9 – I_{off}



Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4 V and +2.4 V.

FIGURE 10 – RECEIVER PROPAGATION DELAY $t_{PLH(D)}$ AND $t_{PHL(D)}$





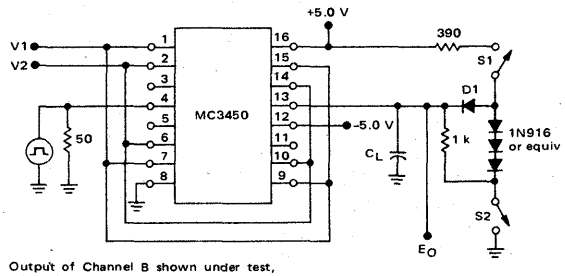
Output of Channel B shown under test, other channels are tested similarly.

S1 at "A" for MC3452
S1 at "B" for MC3450
C_L = 15 pF total for MC3452
C_L = 50 pF total for MC3450

E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leqslant 10$ ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

TEST CIRCUITS (continued)

FIGURE 11 – STROBE PROPAGATION DELAY TIMES $t_{PLZ(S)}$ $t_{PZL(S)}$ $t_{PHZ(S)}$ and $t_{PZH(S)}$



Output of Channel B shown under test, other channels are tested similarly.

	V1	V2	S1	S2	C_L
$t_{PLZ(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{PZL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHZ(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{PZH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leqslant 10$ ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

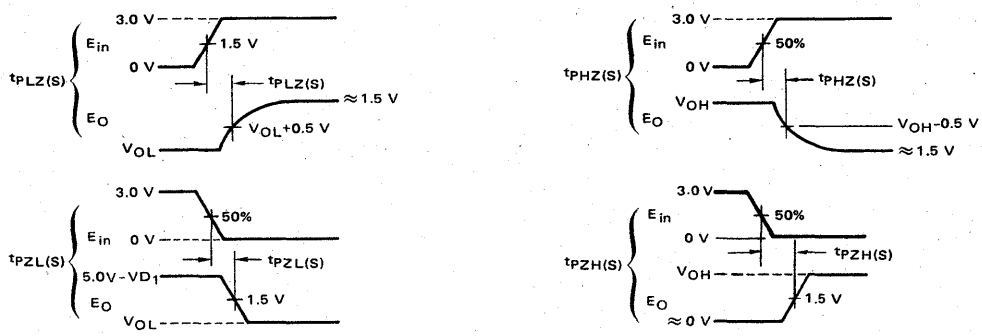
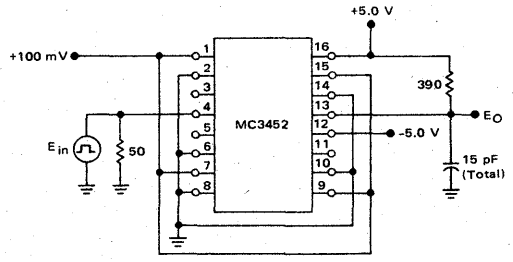
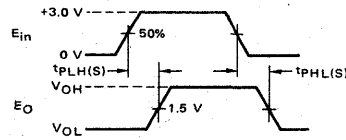


FIGURE 12 – STROBE PROPAGATION DELAY $t_{PLH(S)}$ AND $t_{PHL(S)}$



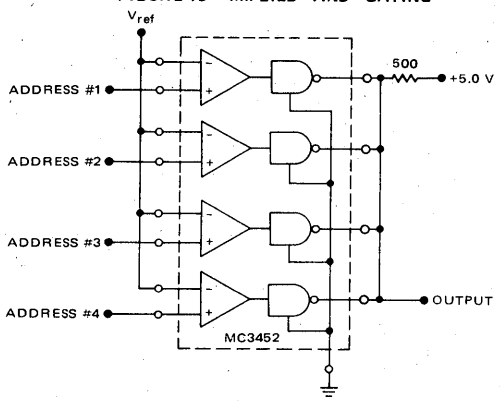
Output of Channel B shown under test, other channels are tested similarly.



E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leqslant 10$ ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

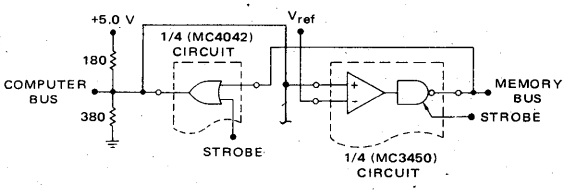
APPLICATIONS INFORMATION

FIGURE 13 – IMPLIED "AND" GATING



The MC3452 can be used for address decoding as illustrated above. All outputs of the MC3452 are tied together through a common resistor to +5.0 volts. In this configuration the MC3452 provides the "AND" function. All addresses have to be true before the output will go high. This scheme eliminates the need for an "AND" gate and enhances speed throughput for address decoding.

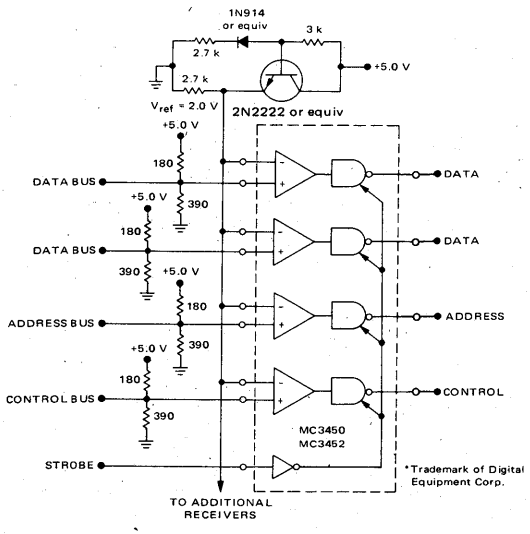
FIGURE 14 – BIDIRECTIONAL DATA TRANSMISSION



The three-state capability of the MC3450 permits bidirectional data transmission as illustrated.

5

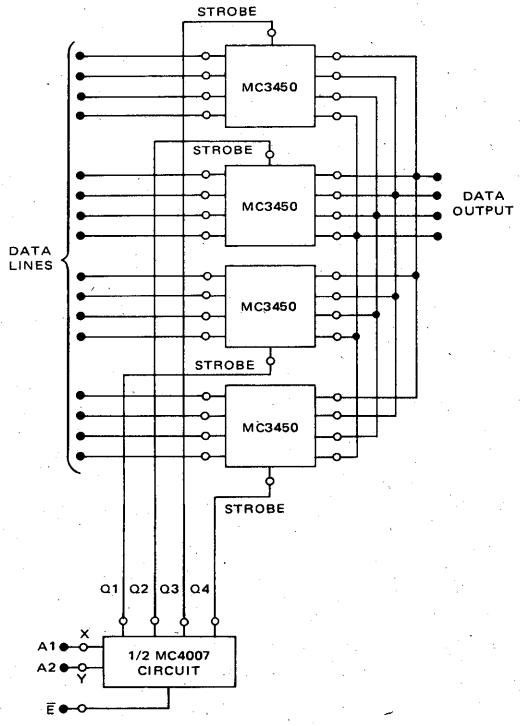
FIGURE 15 – SINGLE-ENDED UNI-BUS* LINE RECEIVER APPLICATION FOR MINICOMPUTERS



*Trademark of Digital Equipment Corp.

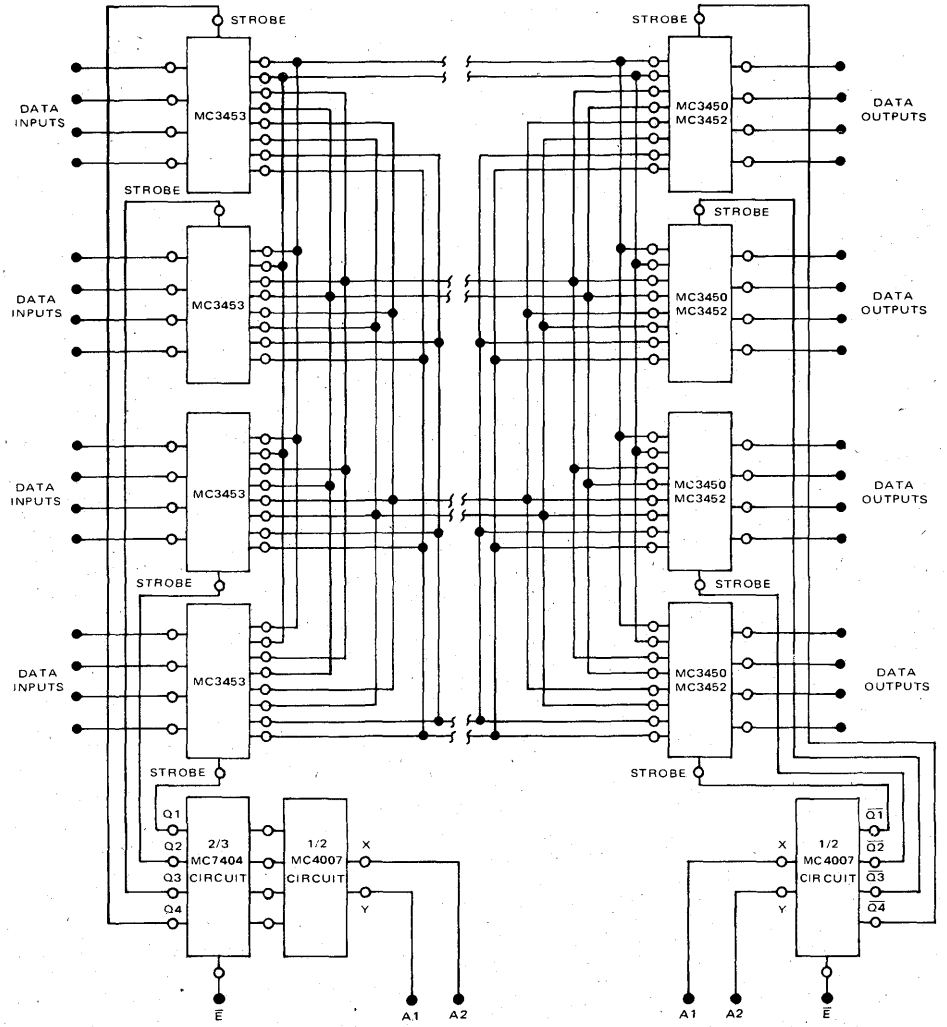
The MC3450/3452 can be used for single-ended as well as differential line receiving. For single-ended line receiver applications, such as are encountered in minicomputers, the configuration shown in Figure 15 can be used. The voltage source, which generates V_{ref}, should be designed so that the V_{ref} voltage is halfway between V_{OH}(min) and V_{OL}(max). The maximum input overdrive required to guarantee a given logic state is extremely small, 25 mV maximum. This low-input overdrive enhances differential noise immunity. Also the high-input impedance of the line receiver permits many receivers to be placed on a single line with minimum load effects.

FIGURE 16 – WIRED "OR" DATA SELECTION USING THREE-STATE LOGIC



APPLICATIONS INFORMATION (continued)

FIGURE 17 – PARTY-LINE DATA TRANSMISSION SYSTEM WITH MULTIPLEX DECODING



ORDERING INFORMATION

Device	Temperature Range	Package
MC3453L	0°C to +70°C	Ceramic DIP
MC3453P	0°C to +70°C	Plastic DIP

MC3453

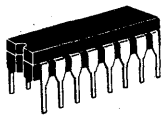
QUAD LINE DRIVER WITH COMMON INHIBIT INPUT

SILICON MONOLITHIC INTEGRATED CIRCUIT

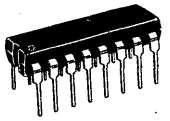
MTTL COMPATIBLE QUAD LINE DRIVER

The MC3453 features four MC75110 type line drivers with a common inhibit input. When the inhibit input is high, a constant output current is switched between each pair of output terminals in response to the logic level at that channel's input. When the inhibit is low, all channel outputs are nonconductive (transistors biased to cut-off). This minimizes loading in party-line systems where a large number of drivers share the same line.

- Four Independent Drivers with Common Inhibit Input
- -3.0 Volts Output Common-Mode Voltage Over Entire Operating Range
- Improved Driver Design Exceeds Performance of Popular MC75110

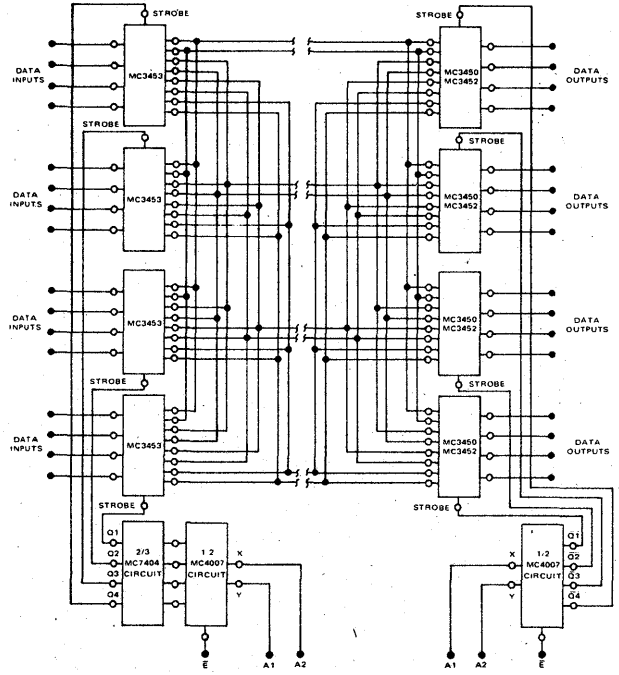


L SUFFIX
CERAMIC PACKAGE
CASE 620

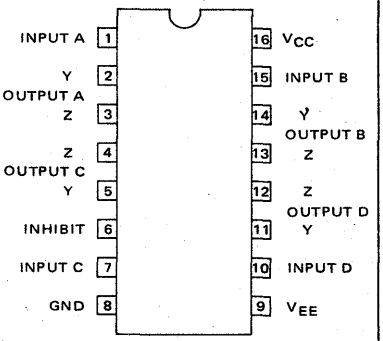


P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 – PARTY-LINE DATA TRANSMISSION SYSTEM WITH MULTIPLEX DECODING



CONNECTION DIAGRAM



TRUTH TABLE
(positive logic)

LOGIC INPUT	INHIBIT INPUT	OUTPUT CURRENT Z	OUTPUT CURRENT Y
H	H	On	Off
L	H	Off	On
H	L	Off	Off
L	L	Off	Off

L = Low Logic Level
H = High Logic Level

5

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Volts
Logic and Inhibitor Input Voltages	V_{in}	5.5	Volts
Common-Mode Output Voltage Range	V_{OCR}	-5.0 to +12	Volts
Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above T_A = +25°C	P_D	 1000 6.6	 mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range Plastic and Ceramic Dual In-Line Packages	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (See Notes 1 and 2.)

Characteristic	Symbol	Min	Nom	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Volts
Common-Mode Output Voltage Range Positive Negative	V_{OCR}	 0 0	 – –	 +10 -3.0	Volts

Note 1. These voltage values are in respect to the ground terminal.
Note 2. When not using all four channels, unused outputs must be grounded.

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DEFINITIONS OF INPUT LOGIC LEVELS*

Characteristic	Symbol	Min	Max	Unit
High-Level Input Voltage (at any input)	V_{IH}	2.0	5.5	Volts
Low-Level Input Voltage (at any input)	V_{IL}	0	0.8	Volts

*The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic##	Symbol	Min	Typ#	Max	Unit
High-Level Input Current (Logic Inputs) (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = V_{CC} Max)	I_{IH_L}	 – –	 – –	 40 1.0	 µA mA
Low-Level Input Current (Logic Inputs) (V_{CC} = Max, V_{EE} = Max, V_{IL_L} = 0.4 V)	I_{IL_L}	–	–	-1.6	mA
High-Level Input Current (Inhibit Input) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)	I_{IH_I}	 – –	 – –	 40 1.0	 µA mA
Low-Level Input Current (Inhibit Input) (V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)	I_{IL_I}	–	–	-1.6	mA
Output Current ("on" state) (V_{CC} = Max, V_{EE} = Max) (V_{CC} = Min, V_{EE} = Min)	$I_{O(on)}$	 – 6.5	 11 11	 15 –	mA
Output Current ("off" state) (V_{CC} = Min, V_{EE} = Min)	$I_{O(off)}$	–	5.0	100	µA
Supply Current from V_{CC} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{CC(on)}$	–	35	50	mA
Supply Current from V_{EE} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{EE(on)}$	–	65	90	mA
Supply Current from V_{CC} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{CC(off)}$	–	35	50	mA
Supply Current from V_{EE} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{EE(off)}$	–	25	40	mA

#All typical values are at V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.
##For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.
Ground unused inputs and outputs.

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Logic Input to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_L}	–	9.0	15	ns
	t_{PHL_L}	–	9.0	15	
Propagation Delay Time from Inhibit Input to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_I}	–	16	25	ns
	t_{PHL_I}	–	20	25	

FIGURE 2 – LOGIC INPUT TO OUTPUTS PROPAGATION DELAY TIME WAVEFORMS

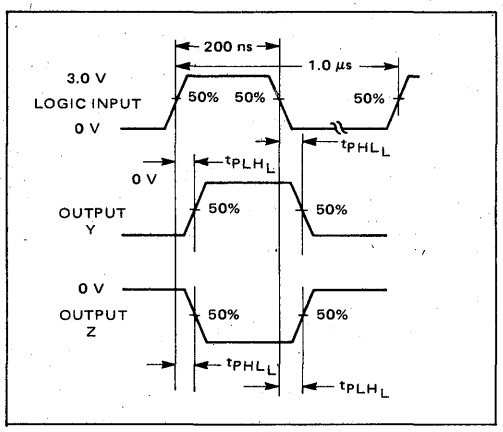
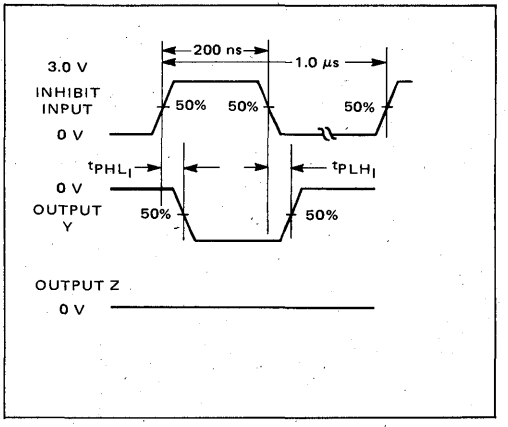
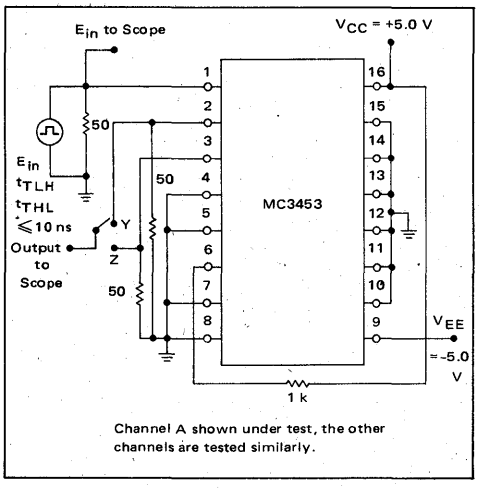


FIGURE 3 – INHIBIT INPUT TO OUTPUTS PROPAGATION DELAY TIME WAVEFORMS



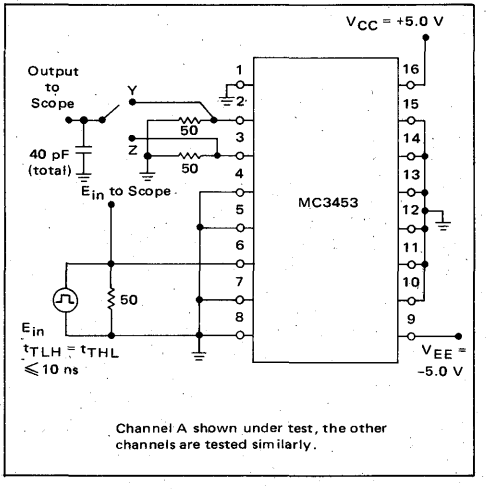
TEST CIRCUITS

FIGURE 4 – LOGIC INPUT TO OUTPUT PROPAGATION DELAY TIME TEST CIRCUIT



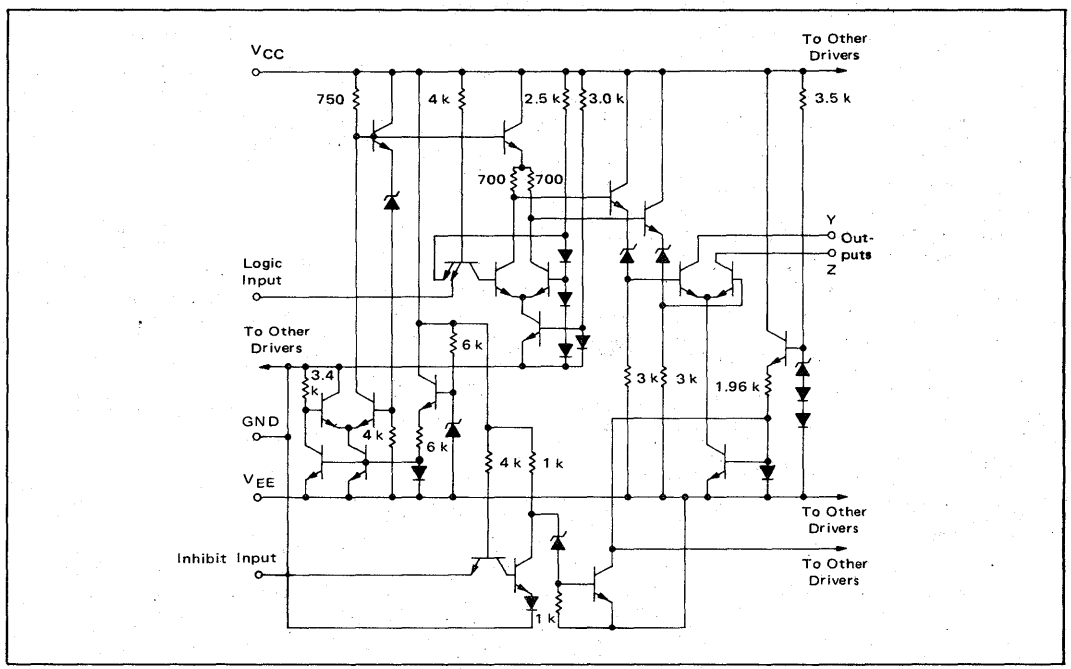
Channel A shown under test, the other channels are tested similarly.

FIGURE 5 – INHIBIT INPUT TO OUTPUT PROPAGATION DELAY TIME TEST CIRCUIT



Channel A shown under test, the other channels are tested similarly.

FIGURE 6 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



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ORDERING INFORMATION

Device	Temperature Range	Package
MC3459L	0°C to +70°C	Ceramic DIP
MC3459P	0°C to +70°C	Plastic DIP

MC3459

Specifications and Applications Information

QUAD NMOS MEMORY ADDRESS DRIVER

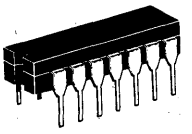
The MC3459 is designed for high-speed driving of the highly capacitive Address select inputs for NMOS Memories. It is also useful in numerous applications requiring a high-current MTTL NAND gate. It is pin-compatible with the popular MC7400 Quad NAND gate.

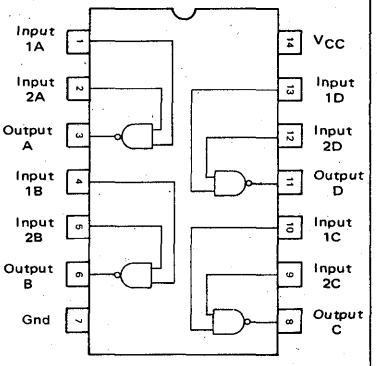
- Fast Propagation Delay Time — 20 ns Typical with 360 pF Load
- Output Voltages Compatible with NMOS Memories
- Inputs Compatible in MTTL and MDTL Logic Families
- Output Loading Factor — 50

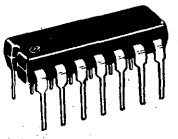
QUAD NMOS ADDRESS LINE DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

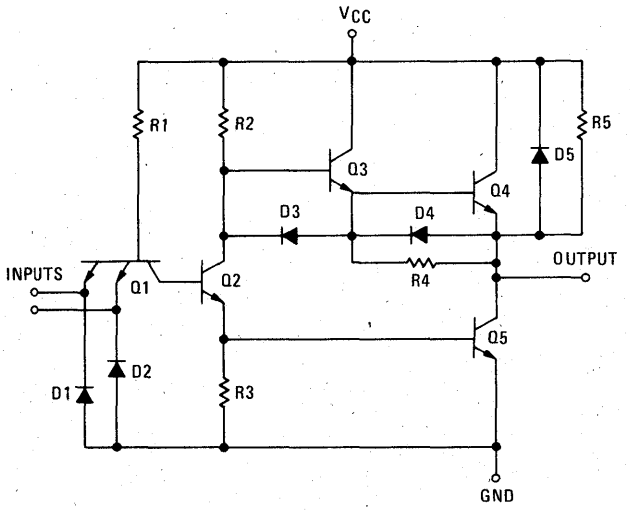




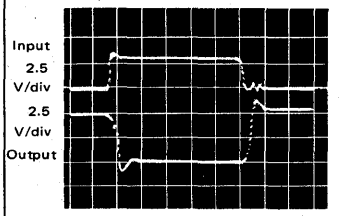


P SUFFIX
PLASTIC PACKAGE
CASE 646

REPRESENTATIVE CIRCUIT SCHEMATIC
(1/4 of Circuit Shown)



TYPICAL OPERATION



V_{CC} = 5.0 V, T_A = 25°C, 50 ns/div, C_L = 360 pF, R_S = 0 Ω

5

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.5	Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation (Package Limitation			
Ceramic Package @ T_A = 25°C	P_D	1000	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Plastic Package @ T_A = 25°C	P_D	830	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Ceramic Package @ T_C = 25°C	P_D	3.0	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	20	mW/°C
Plastic Package @ T_C = 25°C	P_D	1.8	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	14	mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	
Storage Temperature Range	T_{stg}	-65 to +150	°C

5

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 4.75 V ≤ V_{CC} ≤ 5.25 V and 0 ≤ T_A ≤ 70°C)

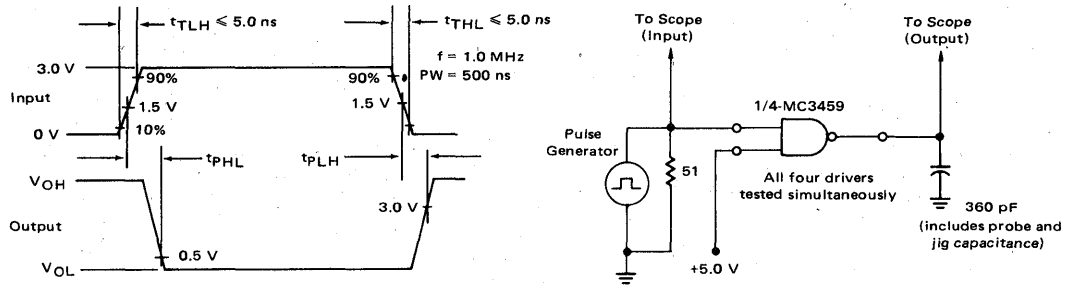
Characteristic	Symbol	Min	Typ (1)	Max	Unit
Input Voltage — High Logic State	V_{IH}	2.0	–	–	V
Input Voltage — Low Logic State	V_{IL}	–	–	0.8	V
Input Current — High Logic State					
(V_{CC} = 5.25 V, V_{IH} = 2.4 V)	I_{IH1}	–	–	80	μA
(V_{CC} = 5.25 V, V_{IH} = 5.5 V)	I_{IH2}	–	–	2.0	mA
Input Current — Low Logic State (V_{CC} = 5.25 V, V_{IL} = 0.4 V)	I_{IL}	–	–	-3.6	mA
Input Clamp Voltage (I_{IC} = -12 mA)	V_{IC}	–	–	-1.5	V
Output Voltage — High Logic State					V
(V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OH} = -640 μA)	V_{OH1}	3.2	–	–	
(V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OH} = -2.0 mA)	V_{OH2}	2.4	–	–	
Output Clamp Voltage (V_{CC} = 5.25 V, V_{IL} = 0 V, I_{OC} = 5.0 mA)	V_{OC}	–	5.8	6.75	V
Output Voltage — Low Logic State					V
(V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OL} = 640 μA)	V_{OL1}	–	–	0.3	
(V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OL} = 80 mA)	V_{OL2}	–	–	0.7	
Power Supply Current — Outputs High Logic State (V_{CC} = 5.25 V, V_{IL} = 0 V)	I_{CCH}	–	12	18	mA
Power Supply Current — Outputs Low Logic State (V_{CC} = 5.25 V, V_{IH} = 5.0 V)	I_{CCL}	–	85	122	mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V, T_A = 25°C, C_L = 360 pF)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — High to Low Logic State	t_{PHL}	–	21	32	ns
Propagation Delay Time — Low to High Logic State	t_{PLH}	–	16	26	ns

(1) Typical values measured at T_A = 25°C, V_{CC} = 5.0 V.

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES



TYPICAL PREFORMANCE CURVES

FIGURE 2 – POWER CONSUMPTION versus OPERATING FREQUENCY

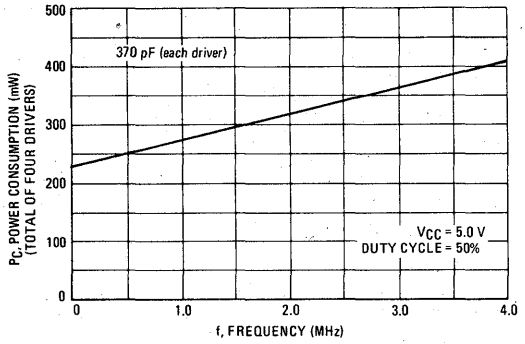


FIGURE 3 – OUTPUT VOLTAGE – HIGH LOGIC STATE versus OUTPUT CURRENT

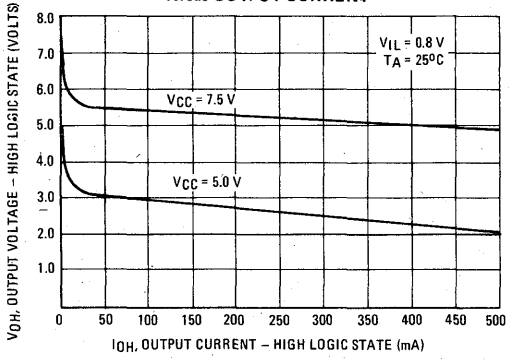


FIGURE 4 – OUTPUT VOLTAGE – HIGH LOGIC STATE versus OUTPUT CURRENT (Expanded Scale)

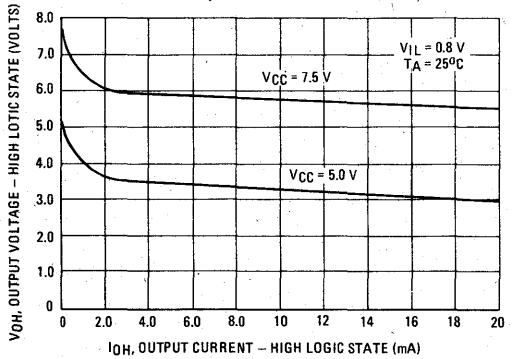
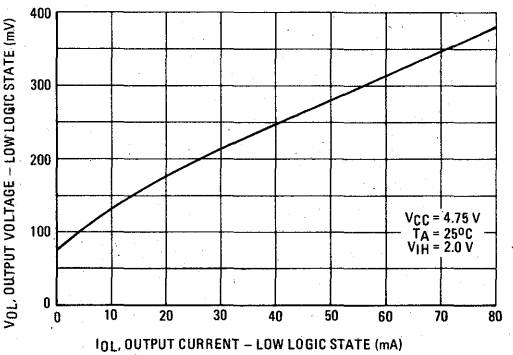


FIGURE 5 – OUTPUT VOLTAGE – LOW LOGIC STATE versus OUTPUT CURRENT



APPLICATIONS SUGGESTIONS

A majority of the new N-Channel MOS memories have TTL logic compatible inputs that exhibit extremely low input current and capacitance (typically 5 pF to 10 pF). However, in a typical memory system (Figure 6) where some of the inputs such as Address lines have to be common, the total parallel input capacitance can be over 300 pF. Standard TTL logic gates have insufficient current drive capability to rapidly switch a high capacitive load; a high speed buffer, such as the MC3459, is required.

A considerable amount of noise can be generated during switching due to the high speed and high current drive capability of the MC3459. The high capacitive discharge current during the high to low transition, plus current spikes can result in a considerable amount of noise being generated on the ground lead. Current spikes are due to both the upper and lower output drive transistors being on for a short period of time during switching. This causes a very low impedance path between V_{CC} and ground.

In order to minimize the effects of these currents, the following layout rules should be followed:

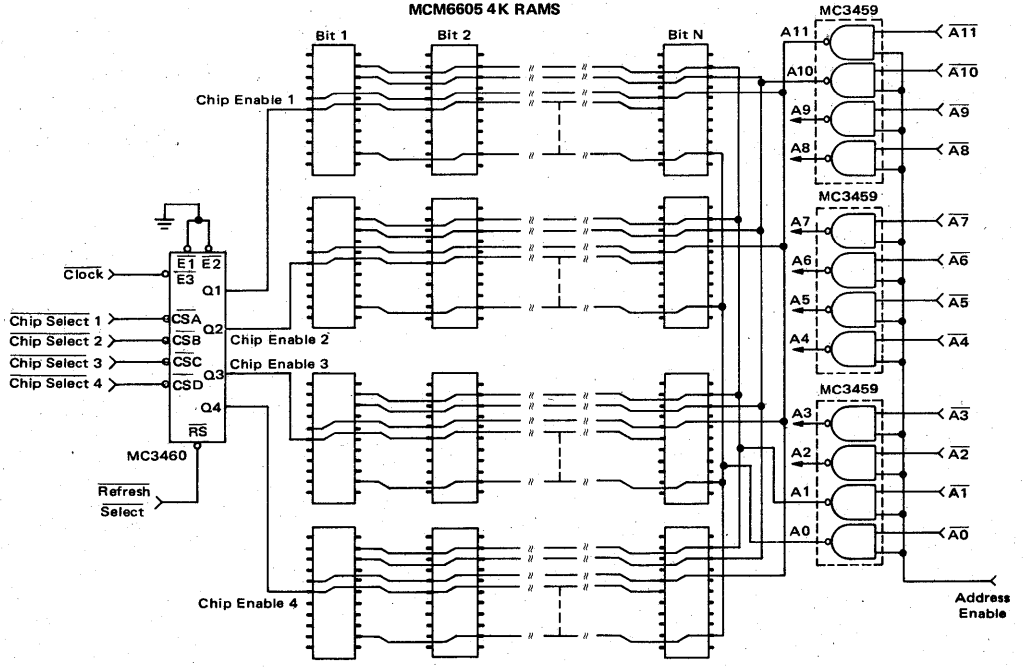
1. The V_{CC} supply pin of each package should be bypassed with a low inductance 0.01 μF capacitor. The 0.01 μF capacitor will sustain the high surge currents required during switching.
2. There is a large amount of current out of the ground node during switching – the noise seen at this node will be proportional to the ground impedance. The impedance of the ground bus can be reduced by increasing its width. At least a 50 mil ground width is recommended.

Some of the NMOS memories with TTL logic compatible inputs do not actually meet the TTL logic level requirements in the input high state voltage (V_{IH}). There are N-Channel MOS memories with a V_{IH} minimum ranging from 2.4 V to 4.0 V. The MC3459 can directly interface with those N-Channel memories having a V_{IH} minimum of 3.0 V. The higher driver output levels can be accomplished by adding a pull-up resistor to V_{CC} or by increasing the V_{CC} voltage. There are some N-Channel MOS memories, such as the MCM7001, that have a supply requirement of 7.5 V. The high maximum supply voltage rating of the MC3459 can accommodate a 7.5 V V_{CC} supply without affecting its input TTL logic compatibility. Figure 4 gives the typical V_{OH} versus I_{OH} characteristics for both V_{CC} = 5.0 V and V_{CC} = 7.5 V. An expanded output characteristic curve of Figure 4 is illustrated in Figure 5.

The MC3459 can be used in a variety of applications including, high fan-out buffer (drives 50 standard TTL loads) and low impedance transmission line driver.

5

FIGURE 6 – TYPICAL APPLICATION
16K X N Memory System Employing MCM6605 4K RAMS



4N MCM6605 RAMS

ORDERING INFORMATION

Device	Temperature Range	Package
MC3460L	0°C to +70°C	Ceramic DIP
MC3460P	0°C to +70°C	Plastic DIP
MC3466L	0°C to +70°C	Ceramic DIP
MC3466P	0°C to +70°C	Plastic DIP

MC3460
MC3466

Specifications and Applications Information

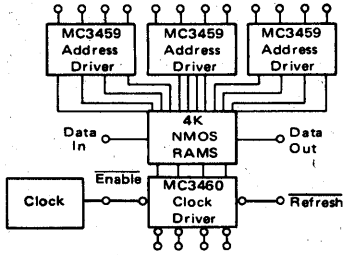
QUAD NMOS MEMORY CLOCK DRIVERS WITH REFRESH SELECT LOGIC

The MC3460 and MC3466 are quad drivers for use with high-level clock lines in NMOS RAM systems. The MC3460 version is specified for 4K memory applications with a V_{DD1} power supply voltages to +13 V. The MC3466 version is specified for mating with the MCM7001A 1K RAM and is guaranteed with a supply voltage V_{DD1} to 18 V. Both versions may be used with the V_{DD2} pin connected to a separate supply > V_{DD1} to increase the high logic state output voltage.

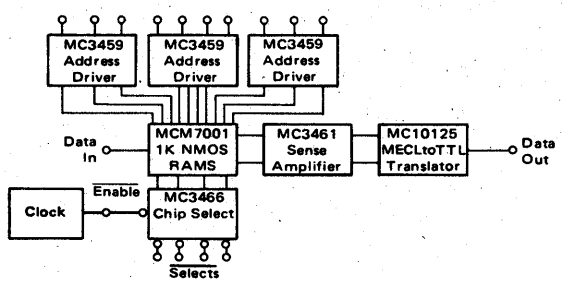
The channel control logic is organized so that all four drivers may be deactivated for STANDBY operation, or single driver may be activated for READ/WRITE operation or all four drivers may be activated for REFRESH operation.

- Control Logic Optimized for Use in MOS RAM Systems
- High Speed Switching
- V_{DD1} and V_{DD2} Variable Over Wide Range of Voltage to 18 and 22 V Respectively (MC3466)
- Output Voltages Compatible with Many Popular MOS RAMs
- MTTL and MDTL Compatible Inputs

TYPICAL APPLICATION WITH 4K NMOS RAM IN TTL SYSTEM (See Figure 17 for Details)

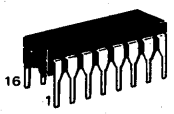


TYPICAL APPLICATION WITH MCM7001 1K RAM AND TTL SYSTEMS (See Figures 22, 23 for Details)

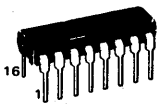


GATE CONTROLLED FOUR CHANNEL MOS CLOCK DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

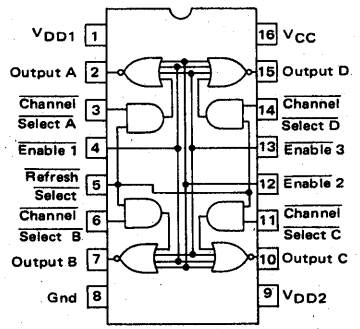


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



TRUTH TABLE

Inputs					Output
Control			Address		
Enable 1	Enable 2	Enable 3	Channel Select	Refresh Select	
H	I	I	I	I	L
I	H	I	I	I	L
I	I	H	I	I	L
I	I	I	H	I	L
L	L	L	L	H	H
L	L	L	I	L	H

H = High Logic State
L = Low Logic State
I = Irrelevant

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}	+7.0	Vdc
MC3460	V_{DD1}	+14	Vdc
MC3466		+19	
MC3460	V_{DD2}	+18	Vdc
MC3466		+23	
Input Voltage	V_I	+5.5	Vdc
Power Dissipation (Package Limitation)			
Ceramic Package @ T_A = 25°C	P_D	1000	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Plastic Package @ T_A = 25°C	P_D	830	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Ceramic Package @ T_C = 25°C	P_D	3.0	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	20	mW/°C
Plastic Package @ T_C = 25°C	P_D	1.8	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	14	mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	MC3460 Min	MC3460 Typ	MC3460 Max	MC3466 Min	MC3466 Typ	MC3466 Max	Unit
Power Supply Voltages	V_{CC}	4.75	5.0	5.25	4.75	5.0	5.25	Vdc
	V_{DD1}	4.75	–	13	4.75	–	18	Vdc
	V_{DD2}	V_{DD1}	–	17	V_{DD1}	–	22	Vdc
(Note 1)	V_{DD2}-V_{DD1}	0	–	10	0	–	10	Vdc
Operating Ambient Temperature Range	T_A	0	–	70	0	–	70	°C

Note 1: Not to Exceed Maximum Recommended Operating Voltages

ELECTRICAL CHARACTERISTICS *(Unless otherwise noted, these specifications apply over recommended power supply and temperature ranges. Typical values measured at T_A = 25°C)*

Characteristic	Symbol	MC3460 Min	MC3460 Typ	MC3460 Max	MC3466 Min	MC3466 Typ	MC3466 Max	Unit
Output Voltage – High Logic State (V_{DD2} = V_{DD1} + 3.0 V, V_{IL} = 0.8 V)	V_{OH1}							Vdc
I_{OH} = -2.0 mA		V_{DD1}-1.0	V_{DD1}-0.8	–	–	–	–	
I_{OH} = -40 mA		–	–	–	V_{DD1}-1.3	V_{DD1}-1.1		
Output Voltage – High Logic State (V_{DD2} = V_{DD1}, V_{IL} = 0.8 V) (See Applications Section of Data Sheet)	V_{OH2}							Vdc
I_{OH} = -100 μA		V_{DD1}-1.0	V_{DD1}-0.8	–	–	–	–	
I_{OH} = -40 mA		–	–	–	V_{DD1}-2.5	V_{DD1}-1.6	–	
Output Voltage – Low Logic State (V_{IH} = 2.0 V, I_{OL} = +10 mA)	V_{OL1}	–	–	0.35	–	–	0.35	Vdc
Output Voltage – Low Logic State (V_{IH} = 2.0 V, I_{OL} = 40 mA)	V_{OL2}							Vdc
11 V ≤ V_{DD2} ≤ 17 V		–	–	0.55	–	–	–	
11 V ≤ V_{DD2} ≤ 22 V		–	–	–	–	–	0.55	

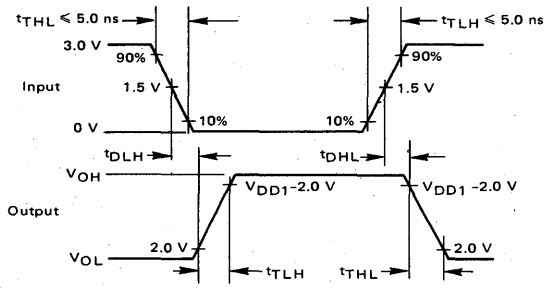
ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply over recommended power supply and temperature ranges. Typical values measured at $T_A = 25^oC$)

Characteristic	Symbol	MC3460			MC3466			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Clamp Voltage (V_{IL} = 0 V, I_{OC} = 5.0 mA)	V_{OC}	–	–	V_{DD1}+ 1.0	–	–	V_{DD1}+ 1.0	Vdc
Input Voltage – High Logic State	V_{IH}	2.0	–	–	2.0	–	–	Vdc
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	–	–	0.8	Vdc
Input Clamp Voltage (I_{IC} = -12 mA)	V_{IC}	–	–	-1.5	–	–	-1.5	Vdc
Input Current – High Logic State (V_I = 5.0 V)	I_{IH}							μA
Channel Select Inputs		–	–	20	–	–	20	
Refresh Select and Enable Inputs		–	–	80	–	–	80	
Input Current – Low Logic State (V_{IL} = 0.4 V)	I_{IL}							mA
Channel Select Inputs		–	–	-1.6	–	–	-1.6	
Refresh Select and Enable Inputs		–	–	-6.4	–	–	-6.4	
Power Supply Current – Output – High Logic State (V_{CC} = 5.25 V, V_{IL} = 0V, I_{OH} = 0 mA, MC3460 V_{DD1} = 13 V, V_{DD2} = 17 V, MC3466 V_{DD1} = 18 V, V_{DD2} = 22 V)	I_{CCH}	–	–	28	–	–	28	mA
	I_{DD1HP}	–	–	0.5	–	–	0.5	
	I_{DD1HN}	–	–	-6.0	–	–	-6.0	
	I_{DD2H}	–	–	6.0	–	–	6.0	
Power Supply Current – Output – Low Logic State (V_{CC} = +5.25, V_{IH} = 5.0 V, I_{OL} = 0 mA, MC3460 V_{DD1} = 13 V, V_{DD2} = 17 V, MC3466 V_{DD1} = 18 V, V_{DD2} = 22 V)	I_{CCL}	–	–	48	–	–	48	mA
	I_{DD1L}	–	–	2.0	–	–	2.0	
	I_{DD2L}	–	–	23	–	–	30	
Power Supply Current – Output – High Logic State (V_{CC} = +5.25 V, V_{IL} = 0 V, I_{OH} = 0 mA, MC3460 V_{DD1} = V_{DD2} = 13 V, MC3466 V_{DD1} = V_{DD2} = 18 V)	I_{DD1H}	–	–	0.5	–	–	0.5	mA
	I_{DD2H}	–	–	0.5	–	–	0.5	

SWITCHING CHARACTERISTICS ($T_A = 25^oC$, V_{CC} = 5.0 V; MC3460 : $V_{DD1} = V_{DD2}$ = 12 V, C_L = 480 pF; MC3466 : $V_{DD1} = V_{DD2}$ = 17 V, V_{DD} = 15 V, C_L = 480 pF)

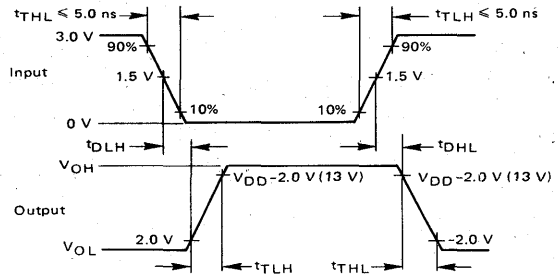
Characteristic	Symbol	MC3460			MC3466			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time – READ/WRITE Mode								ns
Output High to Low Level	t_{DHL1}	–	15	24	–	15	24	
Output Low to High Level	t_{DLH1}	–	15	23	–	15	23	
Transition Time – READ/WRITE Mode								ns
Output High to Low Level	t_{THL1}	–	14	23	–	15	24	
Output Low to High Level	t_{TLH1}	–	14	23	–	15	24	
Propagation Delay Time – REFRESH Mode								ns
Output High to Low Level	t_{DHL2}	–	20	35	–	–	–	
Output Low to High Level	t_{DLH2}	–	16	27	–	–	–	
Transition Time – REFRESH Mode								ns
Output High to Low Level	t_{THL2}	–	20	36	–	–	–	
Output Low to High Level	t_{TLH2}	–	16	27	–	–	–	

FIGURE 1 – SWITCHING TEST WAVEFORMS – MC3460



Input Pulse Characteristics
PRR = 1 MHz READ/WRITE Mode
PRR = 100 kHz REFRESH Mode
PW = 500 ns
$t_{TLH} = t_{THL} \leq 5.0$ ns

FIGURE 2 – SWITCHING TEST WAVEFORMS – MC3466



Input Pulse Characteristics
PRR = 1 MHz, READ/WRITE Mode
PW = 500 ns
$t_{TLH} = t_{THL} \leq 5.0$ ns

FIGURE 3 – SWITCHING TEST CIRCUIT FOR READ/WRITE MODE – MC3460

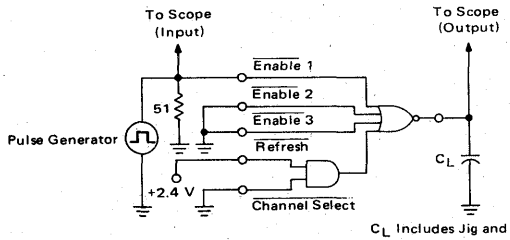


FIGURE 4 – SWITCHING TEST CIRCUIT FOR REFRESH MODE – MC3460

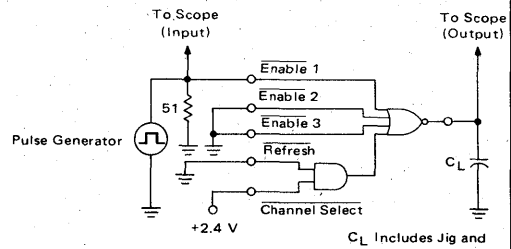


FIGURE 5 – SWITCHING TEST CIRCUIT FOR READ/WRITE MODE – MC3466

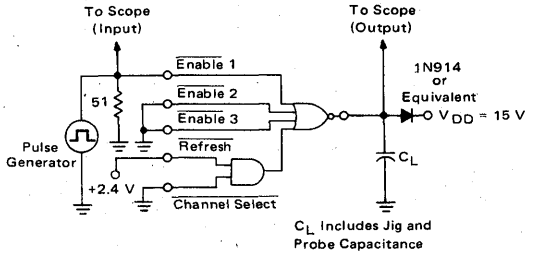
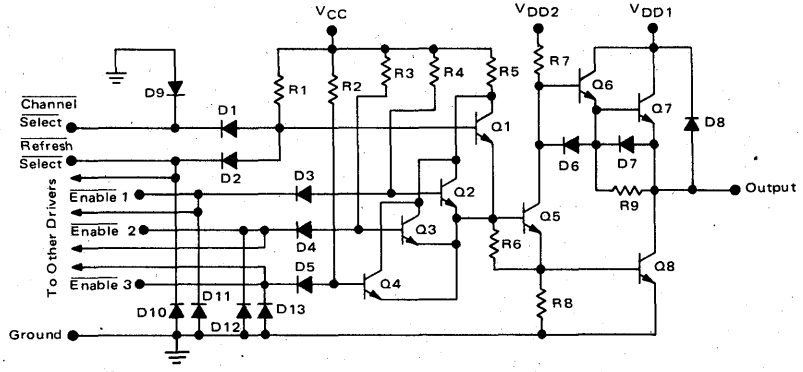


FIGURE 6 – REPRESENTATIVE CIRCUIT SCHEMATIC (1/4 of Circuit Shown)



TYPICAL PERFORMANCE CURVES

FIGURE 7 – DELAY TIMES versus LOAD CAPACITANCE (READ/WRITE MODE)

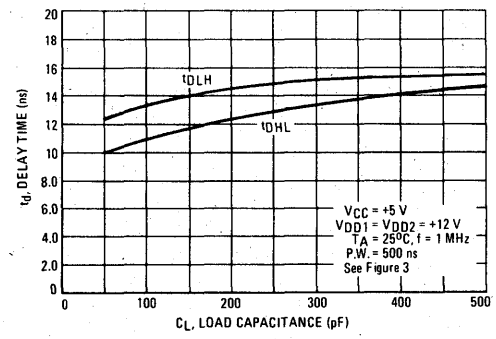
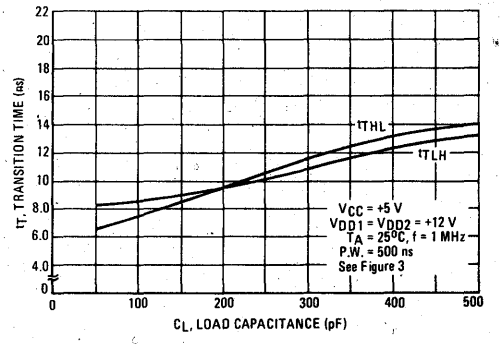


FIGURE 8 – TRANSITION TIMES versus LOAD CAPACITANCE (READ/WRITE MODE)



TYPICAL PERFORMANCE CURVES

FIGURE 9 – DELAY TIMES versus LOAD CAPACITANCE (REFRESH MODE)

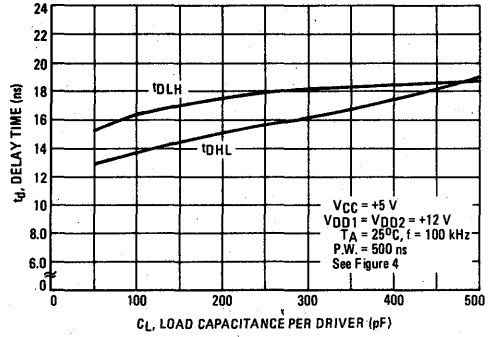


FIGURE 10 – TRANSITION TIMES versus LOAD CAPACITANCE (REFRESH MODE)

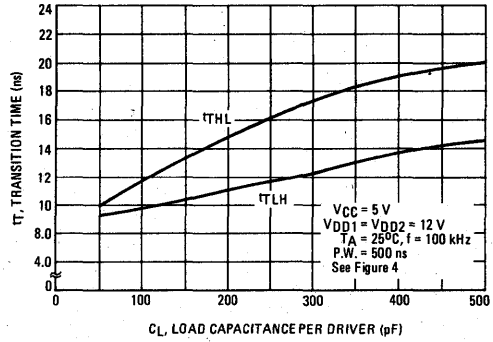


FIGURE 11 – SWITCHING TIMES versus TEMPERATURE (READ/WRITE MODE)

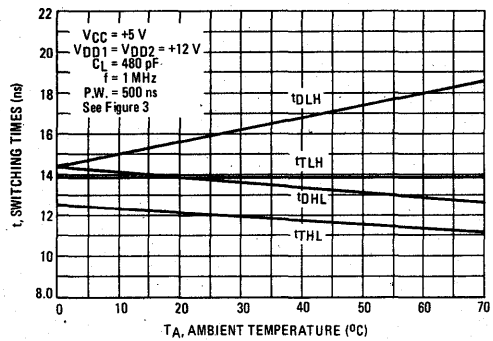


FIGURE 12 – SWITCHING TIMES versus TEMPERATURE (REFRESH MODE)

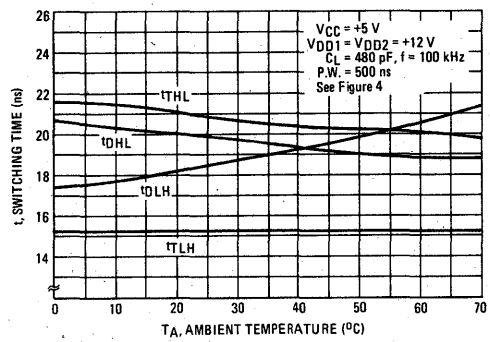


FIGURE 13 – POWER DISSIPATION versus FREQUENCY

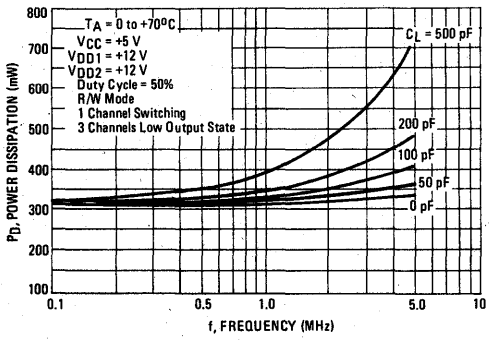
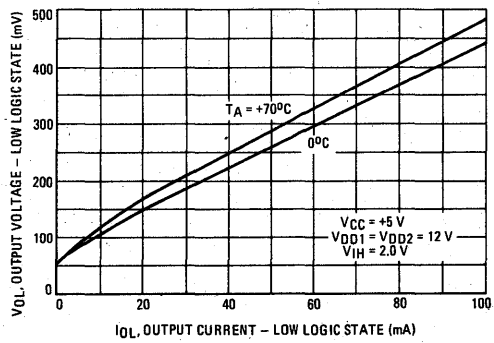


FIGURE 14 – OUTPUT VOLTAGE – LOW LOGIC STATE versus OUTPUT CURRENT



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TYPICAL PERFORMANCE CURVES

FIGURE 15 – OUTPUT VOLTAGE – HIGH LOGIC OUTPUT STATE versus OUTPUT CURRENT

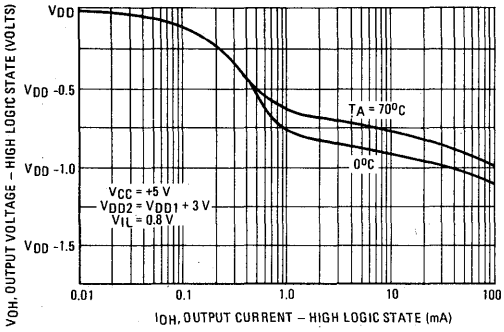

FIGURE 16 – OUTPUT VOLTAGE – HIGH LOGIC STATE versus OUTPUT CURRENT

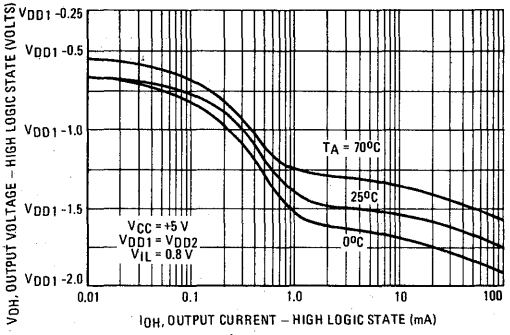

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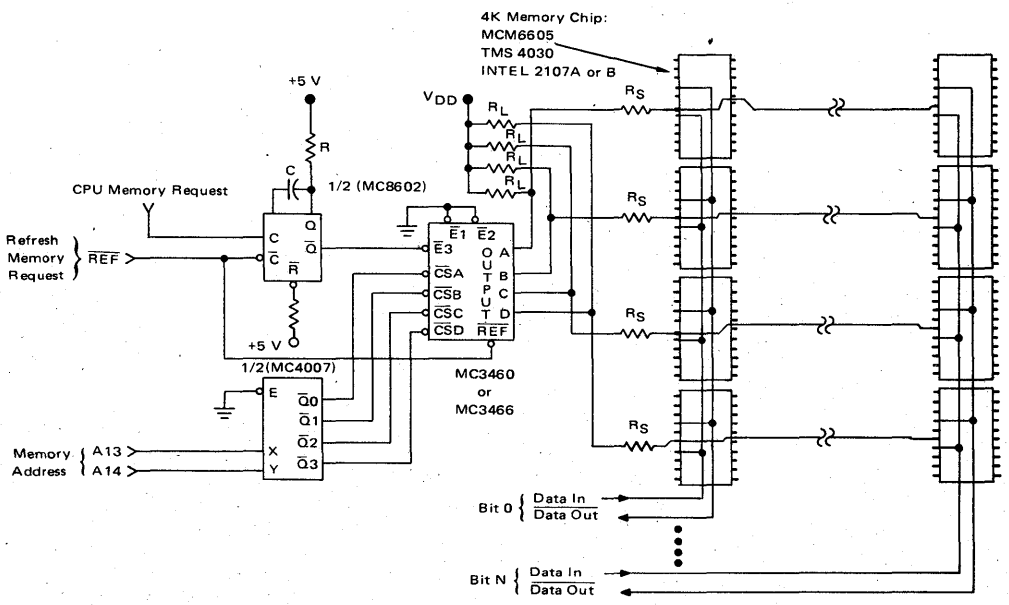
FIGURE 17 – TYPICAL 16K WORD BY N BIT MEMORY ARRAY



APPLICATIONS INFORMATION

The MC3460 and MC3466 are designed specifically for dynamic N-Channel MOS random access memories (RAM's) that require a single high-voltage clock. The unique design and electrical characteristics of these clock drivers will enhance the performance, as well as reduce the cost, of dynamic MOS RAM systems.

Dynamic N-Channel MOS RAM's that require a high voltage clock have extremely low standby power when the clock is in the logic "0" state (Gnd). To take advantage of this low-power mode, the memory system should be partitioned such that only the memory chips of a selected word receive a clock signal (see memory system in Figure 17). However, to reduce the amount of time spent refreshing the memory system, all memory chips of the system should be clocked for each refresh cycle.

The logic necessary to accomplish this desirable system feature has been incorporated in the clock drivers. Note from the block diagram and the truth table (on the front page of this data sheet) that the selection of a clock driver is dependent on the logic state of the $\overline{\text{REFRESH}}$ and $\overline{\text{CHANNEL SELECT}}$ inputs. All four drivers are selected when the $\overline{\text{REFRESH SELECT}}$ input (Pin 5) is at a logic "0" state. However, when the $\overline{\text{REFRESH SELECT}}$ input is at a logic "1" state, only those drivers that have their respective $\overline{\text{CHANNEL SELECT}}$ inputs at a logic "0" state will be selected. The timing and clock driver output pulse width are controlled by a logic "0" signal applied to one of the three $\overline{\text{ENABLE}}$ inputs. The other two $\overline{\text{ENABLE}}$ inputs allow the memory system to be expanded without additional address decoding.

Figure 17 illustrates one possible clock driver configuration that can be employed to drive a 16K word memory system comprised of 4K dynamic MOS RAM's. The MC4007 is a one-of-four decoder that decodes the memory address sent from the CPU. Since the decoder outputs drive the clock driver $\overline{\text{SELECT}}$ inputs, only one of the four clock drivers will be selected. The timing and clock driver output pulse width can be accomplished with a simple one-shot (MC8602). The $\overline{Q}$ output of the MC8602 drives an $\overline{\text{ENABLE}}$ input of the MC3460/MC3466 and the clock pulse width is determined by the RC component values.

For a memory refresh cycle, the $\overline{\text{REFRESH SELECT}}$ input of the MC3460/MC3466 is switched to a logic "0" state which will select all of the clock drivers as noted earlier. On the falling edge of the $\overline{\text{REFRESH SELECT}}$ signal, the one-shot is fired and at the same time all four clock drivers are selected for the refresh cycle since the $\overline{\text{REFRESH SELECT}}$ signal is in the zero state (See Figure 17). At the end of the refresh cycle, the $\overline{\text{REFRESH SELECT}}$ signal is switched to the logic "1" state and the memory system is set to accommodate another CPU memory request. The memory system access time will be enhanced with this scheme because no additional gating is required to accommodate the refresh cycle.

SYSTEM CONSIDERATIONS

Bypass and Layout – A considerable amount of noise can be generated during switching due to the high speed and high current drive capability of these drivers. The high charge or discharge current spikes during transitions can result in a considerable amount of noise being generated on the ground and V_{DD1} leads. These current spikes are primarily due to capacitive load current. However, there is an additional component to the total current spike which is due to both the upper and lower output driver transistors conducting for a short period of time during switching. This causes a low impedance path between the V_{DD1} supply and ground during part of the transition time.

In order to minimize the effects of these surge currents, the following layout rules should be followed:

1. The V_{DD1} supply pin of each package should be bypassed with a low inductance 0.1 μF capacitor. The 0.1 μF capacitor will sustain the high surge currents required during switching.
2. The surge current that flows out of the driver ground pin during switching will generate noise. This noise will be proportional to the ground impedance at the ground pin. To insure minimum ground noise, the ground path to this pin should be as wide as possible. At least a 50 mil to 100 mil ground line is recommended.

Fanout Considerations – In a memory system, the number of memory CHIP ENABLE inputs that can be driven by a single clock driver will depend on the input capacitance and the input leakage current required at a specified minimum logic "1" state (V_{CEH}). Since the memory CHIP ENABLE input capacitance will affect the clock transition times, the total parallel input capacitance should not exceed that value which will cause the clock driver transition times to be slower than those specified for the memory. For a majority of the 4K RAM's, the chip enable input capacitance is less than 40 pF. With a 30 pF loading, each driver of this device can drive up to sixteen 4K memory chips.

Although the input leakage current of each memory CHIP ENABLE is extremely small, the total leakage current of the CHIP ENABLE inputs when paralleled in a memory system can exceed the output current of the clock driver in the high output state (V_{OH}). With the MC3460/MC3466 there are two methods that can be employed to increase the output current. The MC3460/MC3466 has split high voltage power supplies (V_{DD1} and V_{DD2}) as noted in Figure 18. With $V_{DD1} = V_{DD2}$, the maximum output current, that guarantees a minimum V_{OH} of V_{DD1} -1.0 Volt, is -100 μA. However, the output current can be greatly increased if a voltage greater than V_{DD1} is applied to V_{DD2}. For $V_{DD2} = V_{DD1}$

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+3.0 Volts, I_{OH} can be increased to -2.0 mA for a V_{OH} minimum of V_{DD1} -1.0 Volt. For most 4K RAM's, this current is sufficient to drive to 200 memory chips. However, if a higher voltage is not available for V_{DD2} then the current can be increased by employing a pull-up resistor to V_{DD1}. The following formula can be used to determine what value of pull-up resistor is needed to meet a given fanout requirement.

$$R \leqslant \frac{V_{DD1} - V_{OH(min)}}{I_R} \quad (1)$$

where

$$I_R = N(I_{ICE}) - I_{OH} \quad (2)$$

I_{OH} is the clock driver output current for $V_{OH(min)} \geqslant V_{CEH(min)}$

I_{ICE} is the memory CHIP ENABLE input leakage current specification.

N is the number of CHIP ENABLE inputs to be driven by the clock driver.

For the memory system given in Figure 17, assume that each word has 16 bits. If the MCM6605 4K RAM were employed, then the pull-up resistor value would be calculated in the following manner.

From the MCM6605 Specifications;

$V_{CEH(min)} = V_{DD} - 1.0$ Volt @ $I_{ICE} = 10\ \mu A$.

From the MC3460 Specifications;

For $V_{DD1} = V_{DD2}$ the minimum V_{OH} is V_{DD1} - 1.0 Volt @ an $I_{OH} = 100\ \mu A$

Since the V_{OH} (min) required by the MCM6605 is V_{DD1} -1.0 Volt, equation (1) reduces to:

$$R \leqslant \frac{V_{DD1} - (V_{DD1} - 1.0\ Volt)}{I_R}$$

or

$$R \leqslant \frac{1.0\ Volt}{I_R} \quad (3)$$

From equation (2), since N = 16, I_R = 16 (10 μA) -100 μA = 60 μA. Substituting in this value of I_R into Equation (3) yields the following value for R:

$$R \leqslant \frac{1.0\ Volt}{60\ \mu A} = 16.6\ k$$

Overshoot — The finite inductance of the memory chip ENABLE line can cause the clock driver to overshoot during switching. With fast switching clock drivers, the overshoot can exceed the maximum logic levels specified for the CHIP ENABLE input. To insure that the overshoot voltage does not exceed the maximum CHIP ENABLE input ratings the following two techniques can be employed:

The simplest scheme is to place a damping resistor R_S in series with the clock line, (See Figure 17). The critical value of R_S can be calculated from the formula:

$$R_S \cong 2\sqrt{\frac{L_S}{C_L}} \quad (4)$$

where L_S is the clock line inductance and C_L is the load capacitance.

For most memory systems the value of R_S will range from 10 ohms to 50 ohms.

The series damping resistor will also affect the transition times of the damped output waveform. Thus, the maximum value that may be used for R_S will be determined by the maximum switching times specified for the CHIP ENABLE input. The following equation can be used to determine the maximum value of R_S.

$$t_T\ (max) \leqslant 2.2\ R_S\ C_L \quad (5)$$

In some high performance memory systems the switching times required may be too fast to accomodate the addition of a damping resistor. For these systems the overshoot can be limited by placing clamp diodes at the far end of the CHIP ENABLE line as noted in Figure 19. Fast recovery diodes are required to insure proper clamping on both the leading and trailing edges of the CLOCK pulse.

Power Considerations — Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the integrated circuit junction temperatures low. Electrical power dissipated in the integrated circuit is the source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature. The temperature increase depends on the amount of power dissipated in the circuit and on the thermal resistance between the heat source and the reference point. The basic formula for converting power dissipation into junction temperature is:

$$T_J = T_A + P_D\ (R_{\theta JC} + R_{\theta CA}) \quad (6)$$

or

$$T_J = T_A + P_D\ (R_{\theta JA}) \quad (7)$$

where

T_J = junction temperature
T_A = ambient temperature
P_D = power dissipation
$R_{\theta JC}$ = thermal resistance, junction to case
$R_{\theta CA}$ = thermal resistance, case to ambient
$R_{\theta JA}$ = thermal resistance, junction to ambient

The power dissipation of the device (P_D) is dependent on the following system requirements: frequency of operation, capacitive loading, output voltage swing, and duty cycle. The power dissipation as a function of capacitive loading and frequency can be obtained from Figure 13. The value found in Figure 13 should not yield a junction temperature, T_J, greater than T_J (max) at the maximum encountered ambient temperature. T_J (max) is specified for the integrated circuit packages in the maximum ratings section of this data sheet.

FIGURE 18 – SIMPLIFIED OUTPUT CONFIGURATION

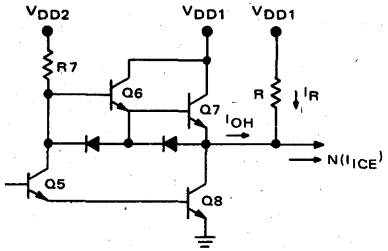
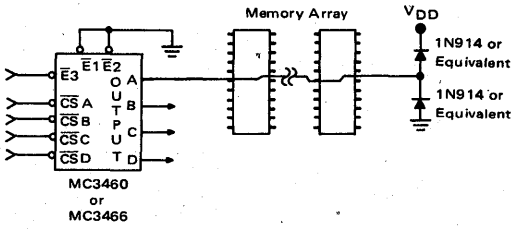


FIGURE 19 – APPLICATION OF CLAMPING DIODES TO LIMIT OVERSHOOT



THE MC3466 IN HIGH PERFORMANCE '7001 SYSTEMS

The MC3466 is specified to meet the more stringent driving requirements of high speed N-channel memories such as the MCM7001A. Figures 20 and 21 show photographs of oscilloscope waveforms for the MC3466 driving up to six MCM7001A memories. The memories were operated with a +15 Volt supply and the MC3466 used a +17 Volt supply tied to V_{DD1} and V_{DD2}. Two clamp diodes were used at the end of the line to clamp the overshoot as noted previously in Figure 19.

With this driver connection, where the V_{DD1} supply is at a higher voltage than the memory V_{DD} supply, the V_{DD1} and V_{DD} supplies should track each other within the following range $3.0\ V \geq V_{DD1} - V_{DD} \geq 1.5\ V$ to insure the minimum output V_{OH} level and to limit the amount of current the clamp diode has to sink during the clock high state period.

For the MC3466 driving two MCM7001A memories, Figure 20 shows the driver supplying about 250 mA peak current when the CHIP SELECT voltage switches from a "low" to "high", with a transition time of 15 ns (1.5 V to 13.5 V level) and a high to low transition time of only 8 ns. When driving four MCM7001A memories, the peak current reaches about 400 mA with a CHIP SELECT rise time of 22 ns.

Figure 21 shows that for a fanout of 6 memories, the transition time increases to 28 ns. The MC3461 (dual NMOS memory sense amplifier) is used to detect the data of the output memory and translate to MECL 10,000 levels. The use of the MC10125 will translate the MECL levels to TTL levels in only 5 ns. The total delay from the 50% level of the falling clock edge at the MC3466 input to the 50% point at the data output of the MC10125 is only 62 ns when driving two memories and 67 ns for four memories.

Figure 22 shows the logic diagram for building a 32K x 1 memory board with TTL interface and MCM7001A memories using a multiplex approach. Addresses A0 to A9 and the D_{IN} signals go to all the memory devices. The address bits A10 and A11 are used to select 1 of 4 rows (WRITE ENABLE lines) when writing into the memory. The addresses, A12, A13, and A14 are decoded using the MC3466 to drive the CHIP SELECT lines. Only two MC3466's are required. Each driver in the MC3466 drives the CHIP SELECT line connected to four memories. During a read operation, the data from 4 of the 32 memories are latched into the MC3461. Addresses A10 and A11 are used to select which one of the four memories is to be read on the DATA OUT line. This configuration is especially useful in interweaving of fast, large memory systems so that the data can be read out consecutively in one CPU cycle time.

A 4K x 18 memory board is shown in Figure 23 with TTL interface using a more straightforward approach. Only six MC3466's are required to drive the CHIP SELECT lines. The memory can be expanded to 256K words by using two 1-of-8 decoders on the control board and connecting the outputs to the proper BOARD ENABLE.

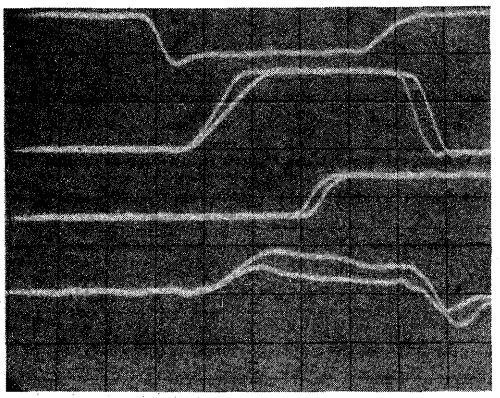
FIGURE 20 – CURRENT AND VOLTAGE CHARACTERISTICS FOR THE MC3460 DRIVER DRIVING 2 AND 4 MCM7001A MEMORIES

$\overline{\text{ENABLE}}$ 1 Input to MC3466 (5 V/Div)

CHIP SELECT voltage with a loading of 2, and 4. MCM7001A memories driven by an MC3466 driver. (10 V/Div.)

DATA OUT of the MC10125 (5 V/Div)

CHIP SELECT current out of the MC3466 driver (500 mA/Div.)



(20 ns/Div.)

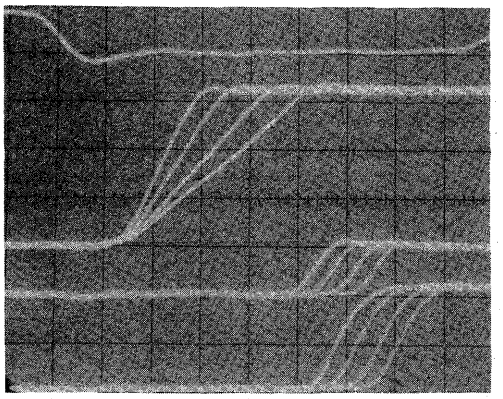
FIGURE 21 – RISE TIME AND ACCESS TIME VARIATIONS FOR AN MC3466 DRIVER DRIVING 1,2,4, AND 6 MCM7001A MEMORIES

$\overline{\text{ENABLE}}$ 1 INPUT to MC3466 (5 V/Div)

CHIP SELECT voltage with a loading of 1,2,4 and 6, MCM7001A memories driven by an MC3466 driver (5 V/Div.)

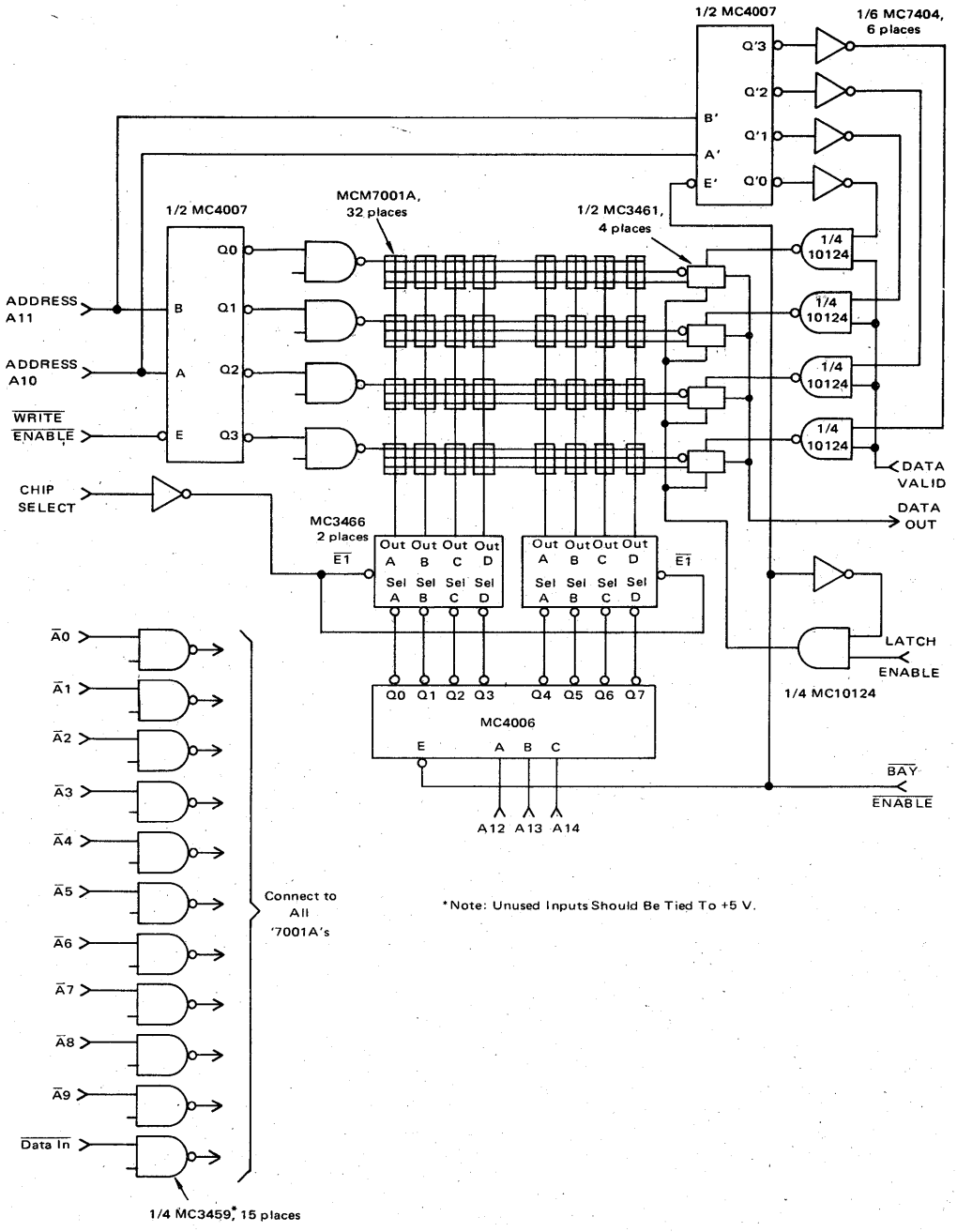
DATA OUT of the MC3461 (1 V/Div)

DATA OUT of the MC10125 (2 V/Div)



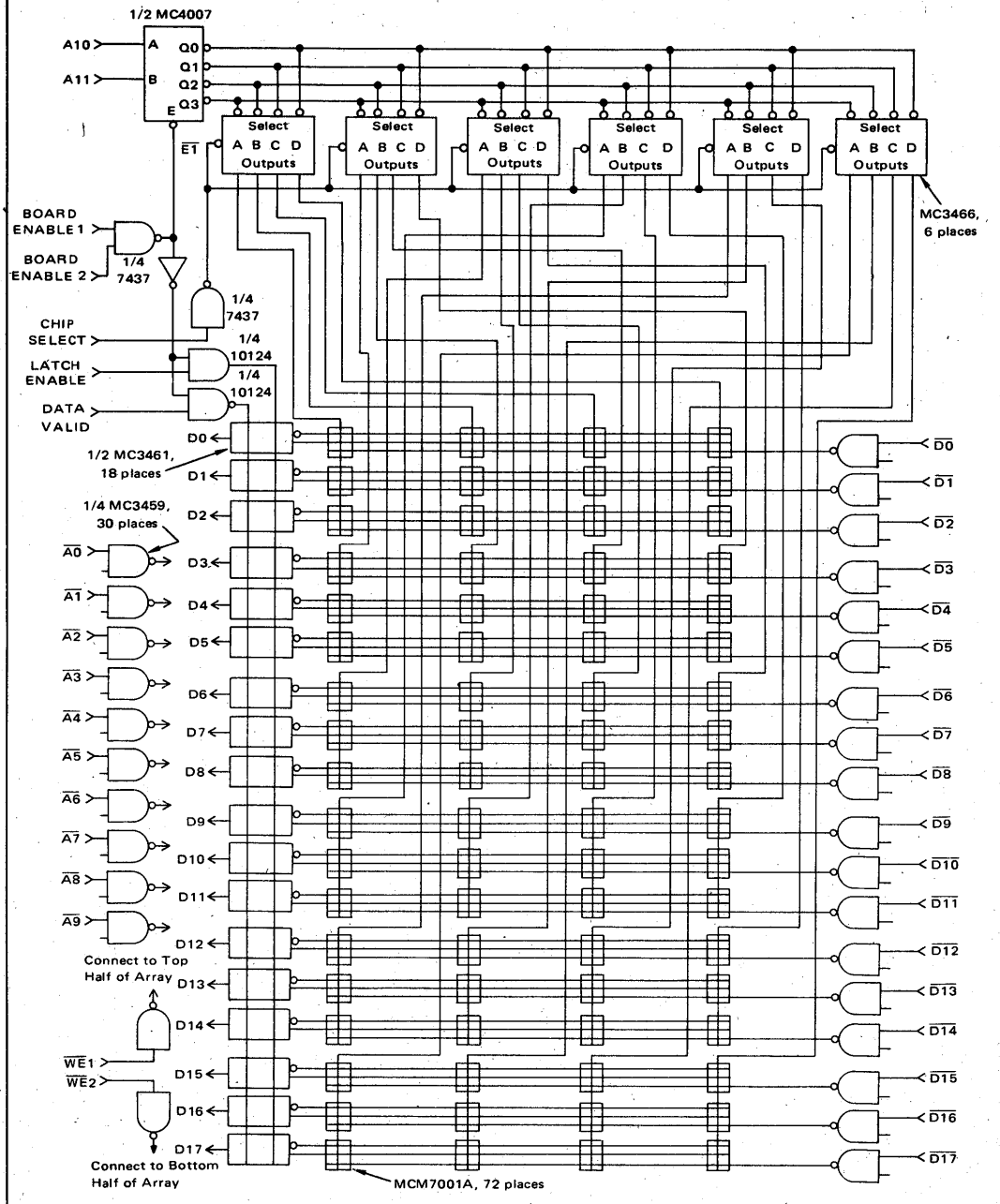
(10 ns/Div)

FIGURE 22 – 32K x 1 MEMORY BOARD
(TTL INTERFACE)



*Note: Unused Inputs Should Be Tied To +5 V.

FIGURE 23 – 4K x 18 MEMORY BOARD (TTL INTERFACE)



ORDERING INFORMATION

Device	Temperature Range	Package
MC3461L	0°C to +75°C	Ceramic DIP

MC3461

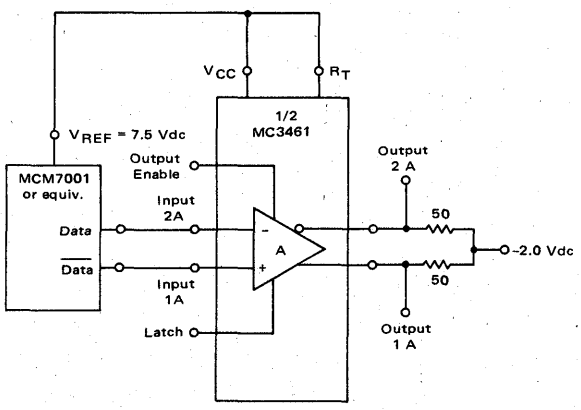
HIGH-SPEED NMOS/MECL SENSE AMPLIFIER

The MC3461 is a dual current sense amplifier with MECL 10,000 compatible control inputs and open emitter complementary outputs. The device is designed for use with Motorola MCM7001 or Intel 2105 NMOS 1K RAMs. A common latch input retains information in the amplifier at the time of latch closure. Separate channel output enables are provided to force the outputs to predetermined states until amplifier information exchange is desired.

When the latch input goes to a logic "0" the outputs are locked in their present state unless the output enable is at, goes to, logic "1". In this event, the Output 1 and Output 2 remain at, or go to, logic "0" and logic "1" respectively.

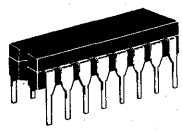
- Complete NMOS Sense Amplifier — No External Components Required
- Minimum Propagation Delay —
  Amplifier Response - 5.0 ns Typ
  Enable Response - 2.5 ns Typ
  Latch Response - 1.0 ns Typ
- Power Supplies Compatible With MCM7001/MECL10,000 Systems
- Amplifier Input Termination Voltage Range from Gnd to V_{REF} Supply on MCM7001

APPLICATION WITH MCM7001 MEMORY



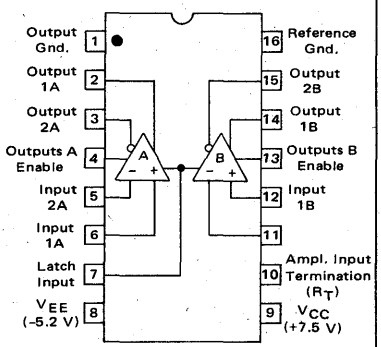
DUAL NMOS MEMORY SENSE AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN CONNECTIONS



TRUTH TABLE
for latch input at logic 1

Input	Output Enable	Output 1	Output 2
I(1) ≥ -200 μA	0	0	1
I(2) = 0 μA	1	0	1
I(1) = 0 μA	0	1	0
I(2) ≥ 200 μA	1	0	1

Negative Currents Defined as Flowing into Device Pin.

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MAXIMUM RATINGS (Unless otherwise noted, $T_A = 25^oC$)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	8.5 -6.0	V V
Termination Voltage	V_T	0 to V_{CC}	–
Operating Ambient Temperature Range	T_A	0 to 75	^oC
Package Power Dissipation Still Air Derate above 25^oC Transverse Air flow ⩾ 500 linear fpm Derate above 25^oC	P_D	 1000 6.7 2000 13.3	 mW mW/^oC mW mW/^oC

ELECTRICAL CHARACTERISTICS

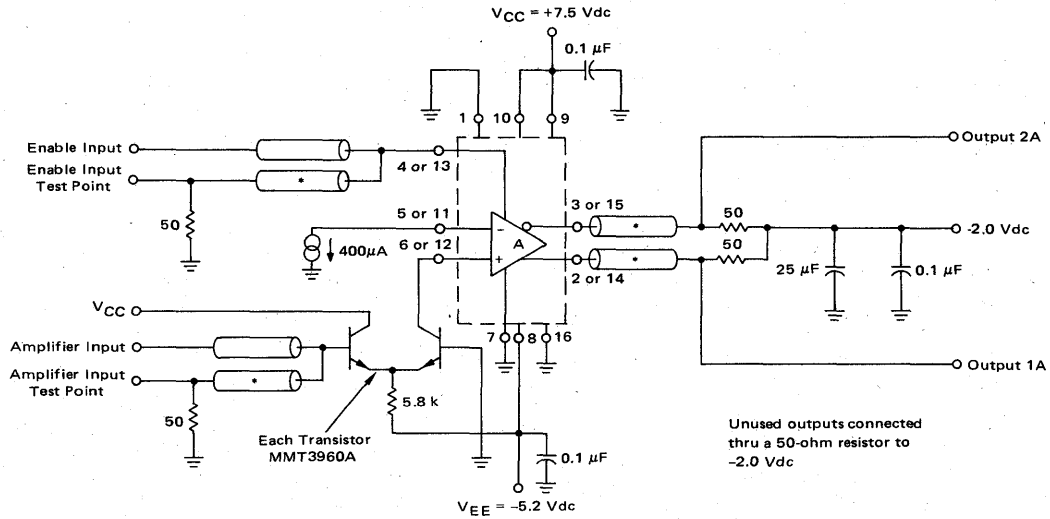
This device has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one sense amplifier. The other half is tested in the same manner.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) I_{sense}	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{CC}	V_{EE}
0^oC	⩾200μA	-0.850	-1.870	-1.155	-1.485	+7.5	-5.2
25^oC	⩾200μA	-0.810	-1.850	-1.105	-1.475	+7.5	-5.2
75^oC	⩾200μA	-0.720	-1.830	-1.045	-1.445	+7.5	-5.2

Characteristic	Symbol	Pin Under Test	MC3461 Test Limits 0^oC Min	0^oC Max	$+25^oC$ Min	$+25^oC$ Typ	$+25^oC$ Max	75^oC Min	75^oC Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: I_{sense}	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{CC}	V_{EE}	Gnd
Power Supply Drain Current	I_{CC}	9	–	–	–	40	50	–	–	mAdc	6,12	–	–	–	–	9, 10	8	1, 16
	I_{EE}	8	–	–	–	-50	-60	–	–	mAdc	6,12	–	–	–	–	9, 10	8	1, 16
Input Current	I_{inH}	4	–	–	–	–	500	–	–	μAdc	5, 11	4	–	–	–	9, 10	8	1, 16
		7	–	–	–	–	500	–	–	μAdc	5, 11	7	–	–	–	9, 10	8	1, 16
	I_{inL}	4	–	–	0.1	–	–	–	–	μAdc	5, 11	–	4	–	–	9, 10	8	1, 16
		7	–	–	0.1	–	–	–	–	μAdc	5, 11	–	7	–	–	9, 10	8	1, 16
Logic "1" Output Voltage	V_{OH}	3	-1.010	-0.850	-0.960	–	-0.810	-0.900	-0.720	Vdc	6	7	–	–	–	9, 10	8	1, 16
		2	↓	↓	↓	–	↓	↓	↓	↓	5	7	–	–	–	↓	↓	↓
		3	↓	↓	↓	–	↓	↓	↓	↓	5	7, 4	–	–	–	↓	↓	↓
Logic "0" Output Voltage	V_{OL}	3	-1.870	-1.660	-1.850	–	-1.650	-1.830	-1.620	Vdc	5	7	–	–	–	9, 10	8	1, 16
		2	↓	↓	↓	–	↓	↓	↓	↓	6	7	–	–	–	↓	↓	↓
		2	↓	↓	↓	–	↓	↓	↓	↓	5	7, 4	–	–	–	↓	↓	↓
Logic "1" Threshold Voltage	V_{OHA}	3	-1.030	–	-0.980	–	–	-0.920	–	Vdc	6	–	–	7	4	9, 10	8	1, 16
		2	↓	–	↓	–	–	↓	–	↓	5	–	–	7	4	↓	↓	↓
		3	↓	–	↓	–	–	↓	–	↓	5	–	–	4,7	–	↓	↓	↓
Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.640	–	–	-1.630	–	-1.600	Vdc	5	–	–	7	4	9, 10	8	1, 16
		2	–	↓	–	–	↓	–	↓	↓	6	–	–	7	4	↓	↓	↓
		2	–	↓	–	–	↓	–	↓	↓	5	–	–	4,7	–	↓	↓	↓
Switching Times (50-ohm load)														Pulse In	Pulse Out			
Propagation Delay Amplifier	t_{--}	2	–	–	–	5.0	10.0	–	–	ns	–	–	–	6	2	9, 10	8	1, 16
	t_{++}	2	–	–	–	↓	↓	–	–	↓	–	–	–	↓	2	↓	↓	↓
	t_{-+}	3	–	–	–	↓	↓	–	–	↓	–	–	–	↓	3	↓	↓	↓
	t_{+-}	3	–	–	–	↓	↓	–	–	↓	–	–	–	↓	3	↓	↓	↓
Enable	t_{--}	3	–	–	–	2.5	5.0	–	–	ns	–	–	–	4	3	9, 10	8	1, 16
	t_{++}	3	–	–	–	↓	↓	–	–	↓	–	–	–	↓	3	↓	↓	↓
	t_{-+}	2	–	–	–	↓	↓	–	–	↓	–	–	–	↓	2	↓	↓	↓
	t_{+-}	2	–	–	–	↓	↓	–	–	↓	–	–	–	↓	2	↓	↓	↓

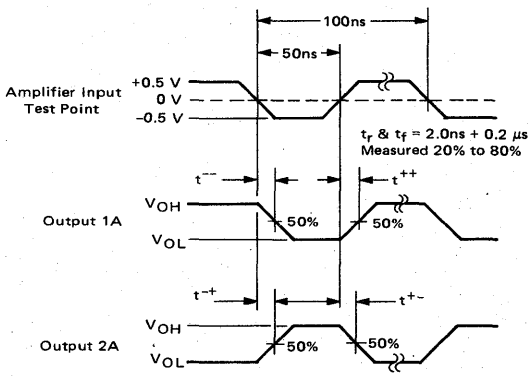
*Negative currents are defined as currents leaving the device.

FIGURE 1 – SWITCHING RESPONSE TEST CIRCUIT AND WAVEFORMS @ 25°C
(Other Section Tested Similarly)



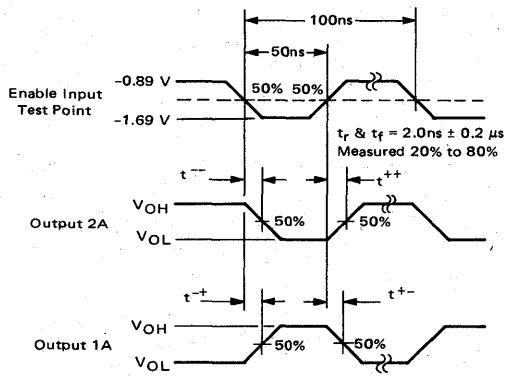
*Denotes equal lengths of 50-ohm coaxial cable. Wire length should be ⩽ 1/4" from test point to pin or BNC connector.

Amplifier Response Waveforms



Enable input held at -1.69 Vdc for Amplifier Response Tests.

Enable Response Waveforms



Amplifier input held at +0.5 Vdc for Enable Response Tests.

FIGURE 2 – 32K x 2 MEMORY BOARD (MECL SYSTEM)

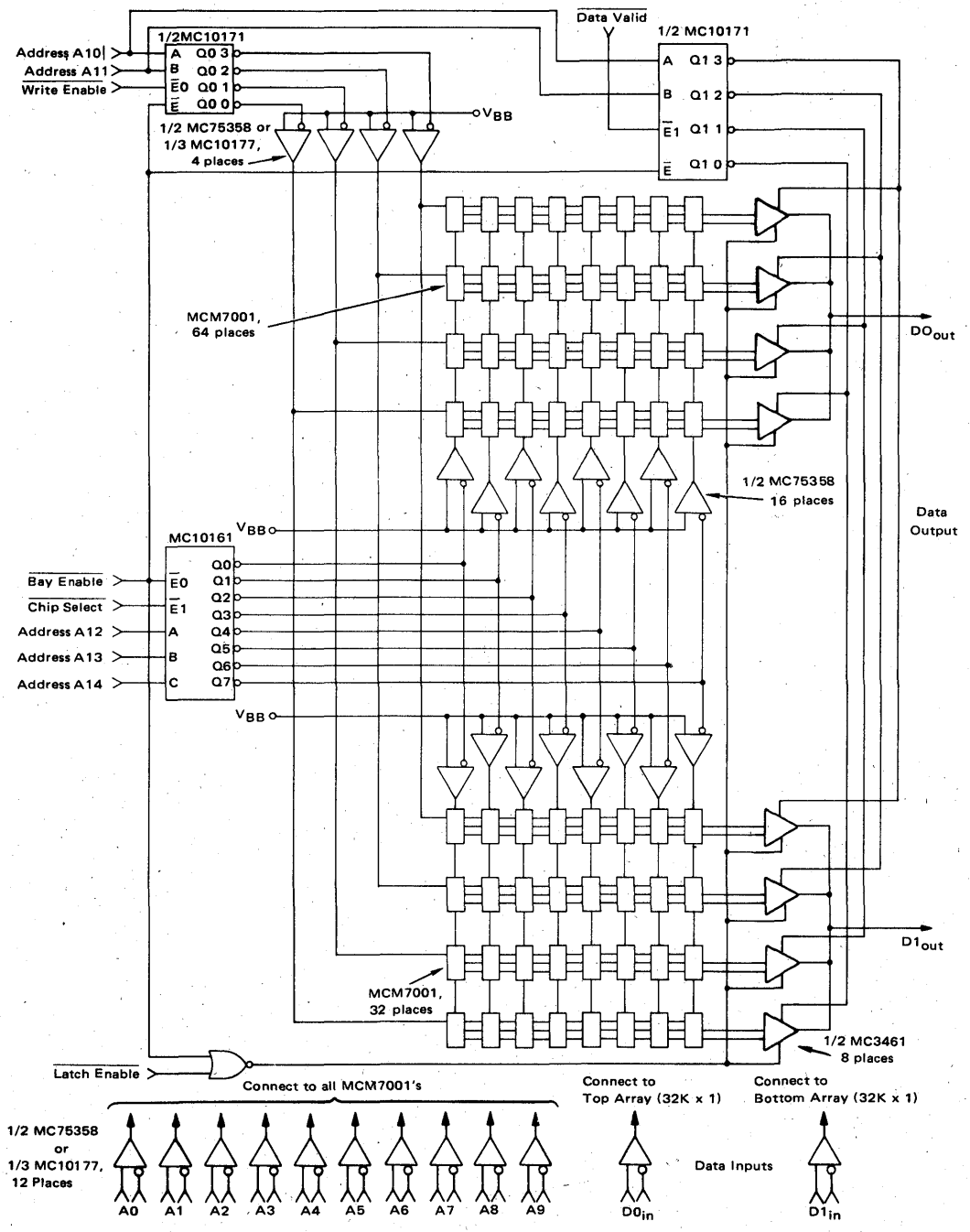
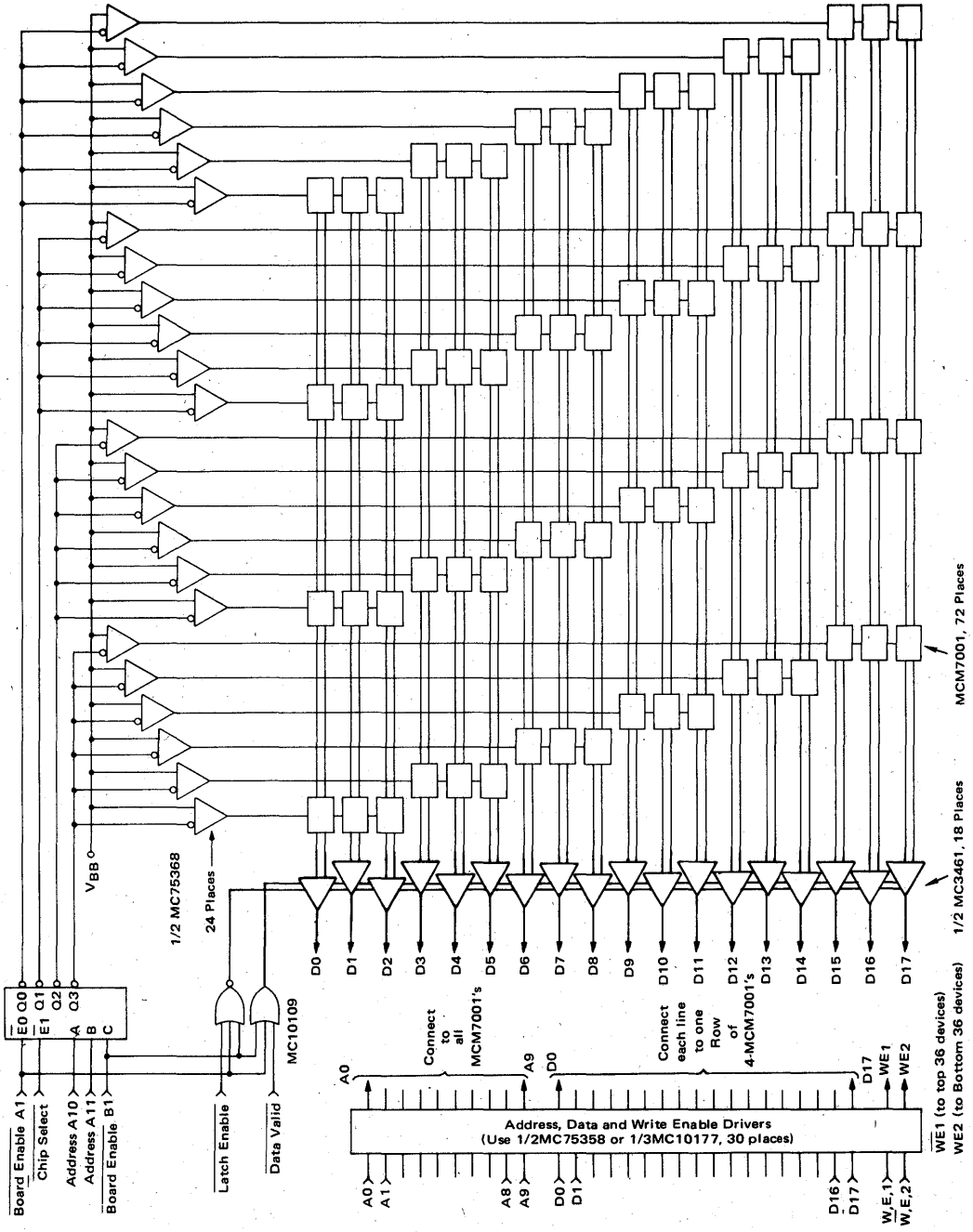


FIGURE 3 – 4K x 18 MEMORY BOARD (MECL SYSTEM)



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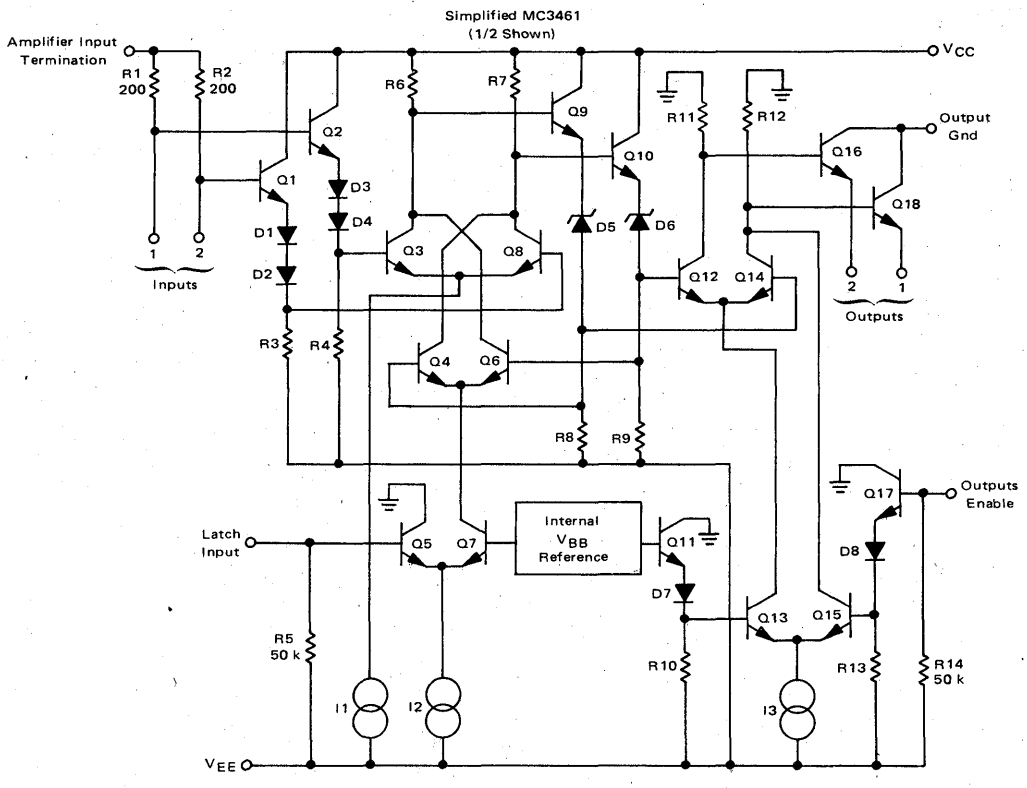
REPRESENTATIVE CIRCUIT SCHEMATIC



ORDERING INFORMATION

Device	Temperature Range	Package
MC3467L	0°C to +70°C	Ceramic DIP
MC3467P	0°C to +70°C	Plastic DIP

MC3467

TRIPLE WIDEBAND PREAMPLIFIER WITH ELECTRONIC GAIN CONTROL (EGC)

The MC3467 provides three independent preamplifiers with individual electronic gain control in a single 18-pin package. Each preamplifier has differential inputs and outputs allowing operation in completely balanced systems. The device is optimized for use in 9-track magnetic tape memory systems where low noise and low distortion are paramount objectives.

The electronic gain control allows each amplifier's gain to be set anywhere from essentially zero to a maximum of approximately 100 V/V.

The MC3467 is intended to mate with the MC3468 read amplifier to provide the entire magnetic tape read function.

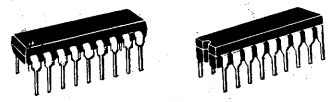
- Wide Bandwidth – 15 MHz (Typ)
- Individual Electronic Gain Control
- Differential Input/Output

TRIPLE MAGNETIC TAPE MEMORY PREAMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 701

L SUFFIX
CERAMIC PACKAGE
CASE 726



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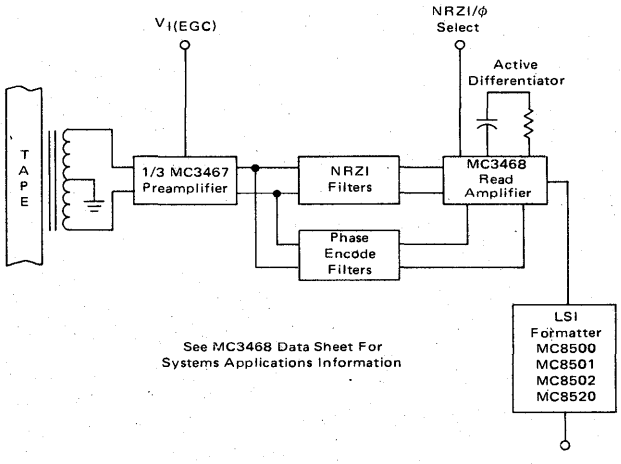
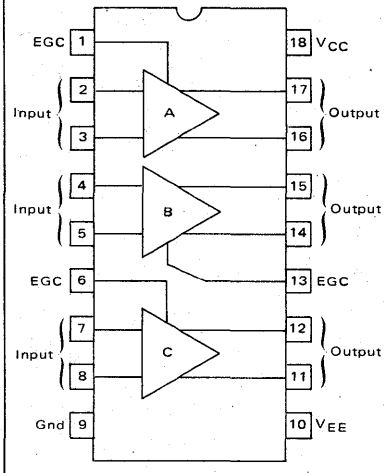
TYPICAL APPLICATION
HIGH PERFORMANCE 9-TRACK OPEN REEL TAPE SYSTEM





MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages Positive Supply Voltage Negative Supply Voltage	 V_{CC} V_{EE}	 6.0 −9.0	V
EGC Voltages (Pins 1, 6 and 13)	$V_{I(EGC)}$	−5.0 to V_{CC}	V
Input Differential Voltage	V_{ID}	±5.0	V
Input Common-Mode Voltage	V_{IC}	±5.0	V
Amplifier Output Short Circuit Duration (to Ground)	t_s	10	s
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = −6.0 V, T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range Positive Supply Voltage Negative Supply Voltage Operating EGC Voltage	 V_{CCR} V_{EER} $V_{I(EGC)}$	 4.75 −5.5 0	 5.0 −6.0 –	 5.25 −7.0 V_{CC}	 V V V
Differential Voltage Gain (Balanced) ($V_{I(EGC)}$ = 0, e_i = 25 mVp-p) (See Figure 1)	A_{VD}	85	100	115	V/V
Differential Voltage Gain ($V_{I(EGC)}$ = V_{CC})	A_{VD}	–	0.5	2.0	V/V
Maximum Input Differential Voltage (Balanced) (T_A = 25°C)	V_{IDR}	0.2	–	–	V_{pp}
Output Voltage Swing (Balanced) (Figure 1) (e_i = 200 mVp-p)	V_{OR}	6.0	8.0	–	V_{pp}
Input Common-Mode Range	V_{ICR}	±1.5	±2.0	–	V
Differential Output Offset Voltage (T_A = 25°C)	V_{OOD}	–	500	–	mV
Common-Mode Output Offset Voltage (T_A = 25°C)	V_{OOC}	–	500	–	mV
Common Mode Rejection Ratio (Figure 2) $V_{I(EGC)}$ = 0, V_{CM} = 1.0 V_{pp} (f = 100 kHz) (f = 1.0 MHz)	CMRR	 60 40	 100 100	 – –	dB
Small-Signal Bandwidth (Figure 1) (−3.0 dB, e_i = 1.0 mVp-p, T_A = 25°C)	BW	10	15	–	MHz
Input Bias Current	I_{IB}	–	5.0	15	μA
Output Sink Current (Figure 5)	I_{OS}	1.0	1.4	–	mA
Differential Noise Voltage Referred to Input (Figure 3) ($V_{I(EGC)}$ = 0, R_S = 50 Ω, BW = 10 Hz to 1.0 MHz, T_A = 25°C)	e_n	–	3.5	–	μV_{RMS}
Positive Power Supply Current (Figure 4)	I_{CC}	–	30	40	mA
Negative Power Supply Current (Figure 4)	I_{EE}	–	−30	−40	mA
Input Resistance (T_A = 25°C)	r_i	12	25	–	kΩ
Input Capacitance (T_A = 25°C)	C_i	–	2.0	–	pF
Output Resistance (Unbalanced) (T_A = 25°C)	r_o	–	30	–	Ohms

FIGURE 1 – DIFFERENTIAL VOLTAGE GAIN, BANDWIDTH AND OUTPUT VOLTAGE SWING TEST CIRCUIT
(Channel A under test, other channels tested similarly)

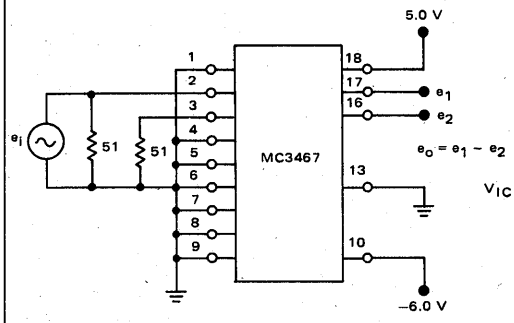


FIGURE 2 – COMMON-MODE REJECTION RATIO
(Channel A under test, other amplifiers tested similarly)

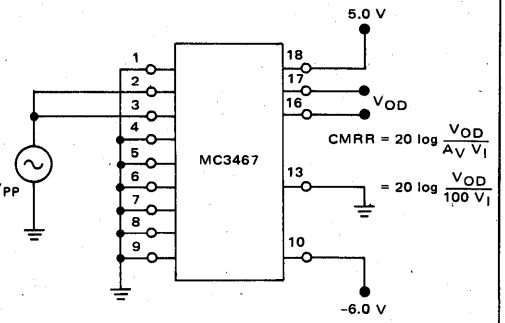


FIGURE 3 – DIFFERENTIAL NOISE VOLTAGE REFERRED TO THE INPUT

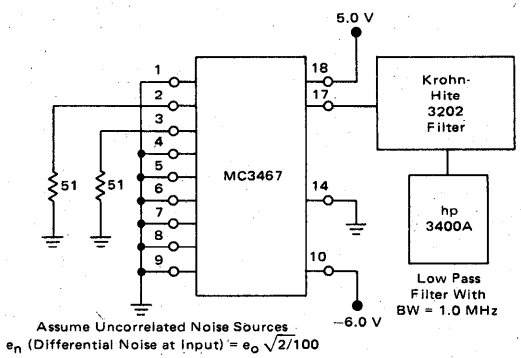


FIGURE 4 – POWER SUPPLY CURRENT TEST CIRCUIT

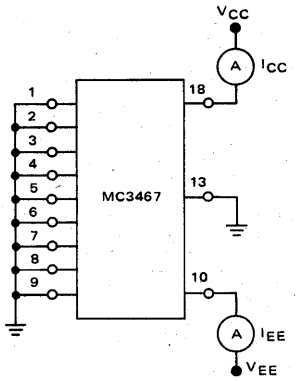


FIGURE 5 – OUTPUT SINK CURRENT TEST CIRCUIT
(Channel A under test, other channels tested similarly)

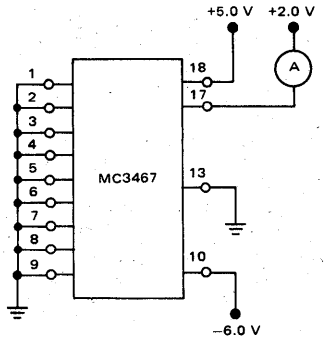
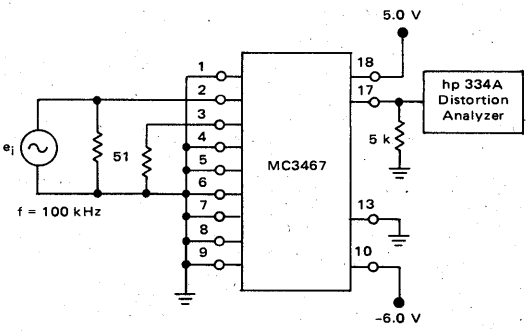


FIGURE 6 – TOTAL HARMONIC DISTORTION TEST CIRCUIT
(Channel A under test, other channels tested similarly)



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TYPICAL CHARACTERISTICS
(V_{CC} = 5.0 V, V_{EE} = -6.0 V, T_A = 25° unless otherwise noted)

FIGURE 7 – TOTAL HARMONIC DISTORTION (THD) versus INPUT VOLTAGE

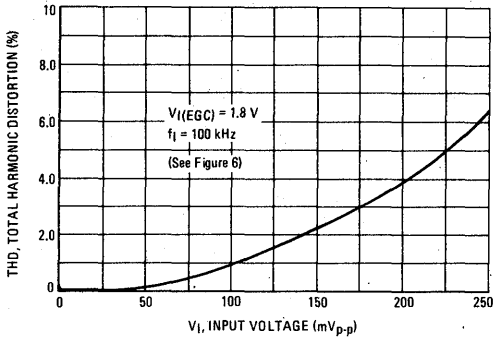


FIGURE 8 – NORMALIZED VOLTAGE GAIN versus FREQUENCY

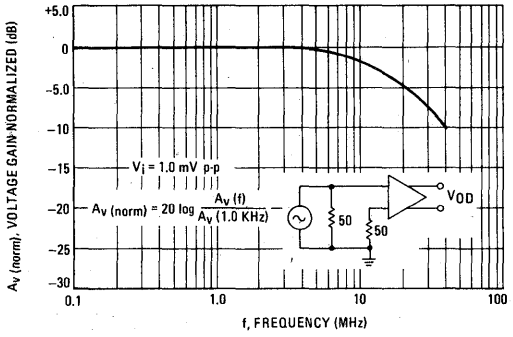


FIGURE 9 – NORMALIZED VOLTAGE GAIN versus AMBIENT TEMPERATURE

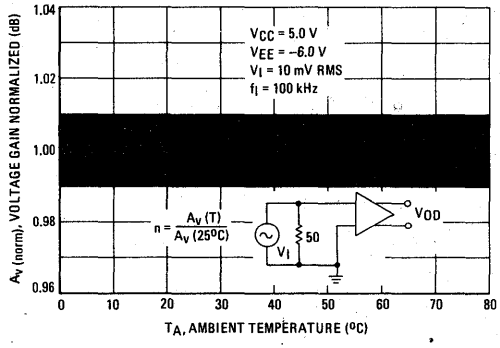


FIGURE 10 – NORMALIZED POSITIVE POWER SUPPLY CURRENT versus POSITIVE POWER SUPPLY VOLTAGE

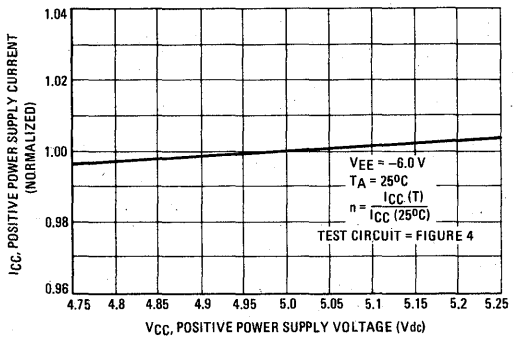


FIGURE 11 – NORMALIZED NEGATIVE POWER SUPPLY CURRENT versus NEGATIVE POWER SUPPLY VOLTAGE

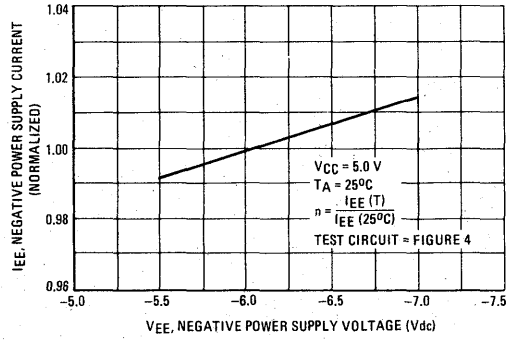


FIGURE 12 – NORMALIZED POWER SUPPLY CURRENTS versus AMBIENT TEMPERATURE

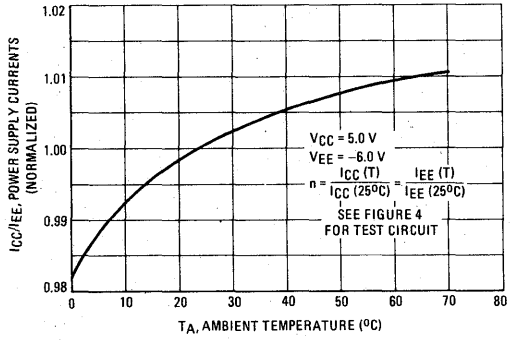


FIGURE 13 – DIFFERENTIAL VOLTAGE GAIN versus ELECTRONIC GAIN CONTROL VOLTAGE ($V_{I(EGC)}$)

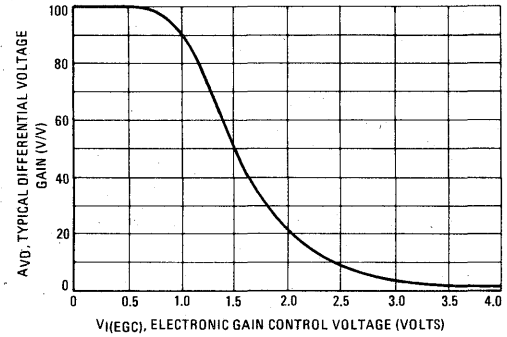


FIGURE 14 – COMMON-MODE REJECTION RATIO (CMRR) versus FREQUENCY

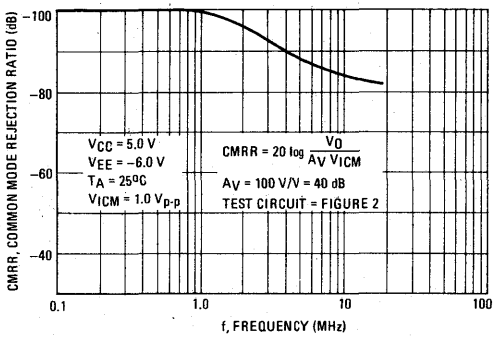


FIGURE 15 – PHASE SHIFT versus FREQUENCY

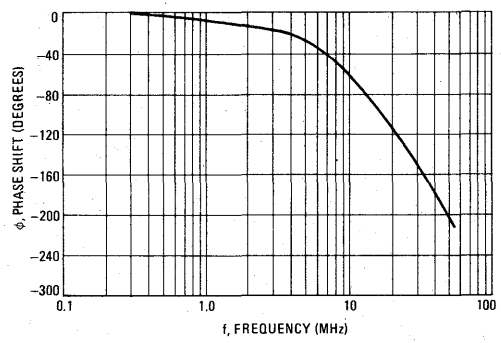
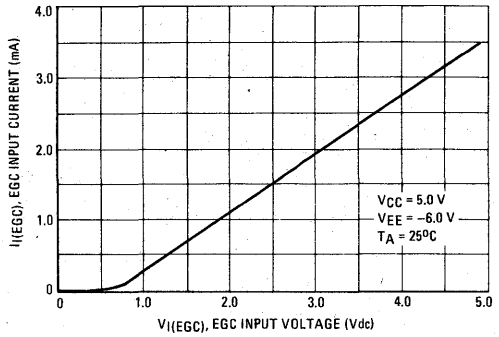
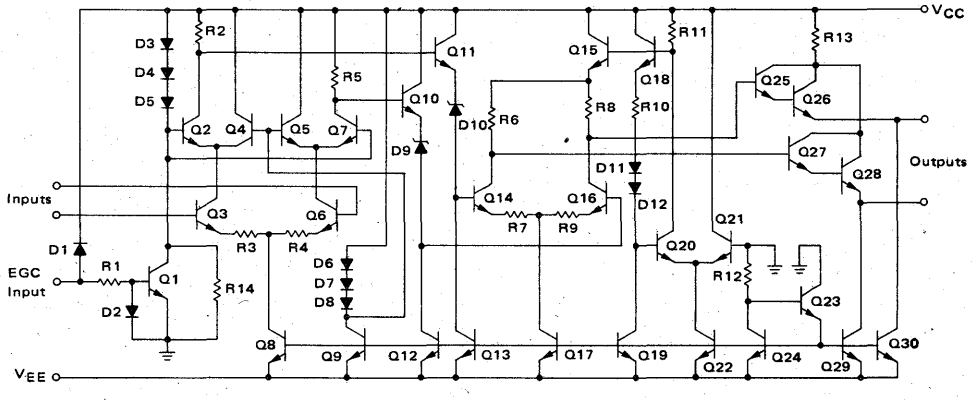


FIGURE 16 – TYPICAL EGC INPUT CURRENT versus EGC INPUT VOLTAGE



REPRESENTATIVE CIRCUIT SCHEMATIC

1/3 MC3467



ORDERING INFORMATION

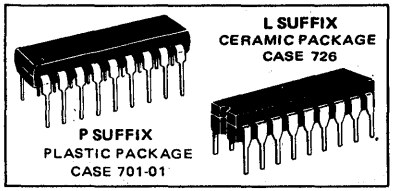
Device	Temperature Range	Package
MC3468L	0°C to +70°C	Ceramic DIP
MC3468P	0°C to +70°C	Plastic DIP

MC3468

Specifications and Applications Information

MAGNETIC TAPE MEMORY READ AMPLIFIER

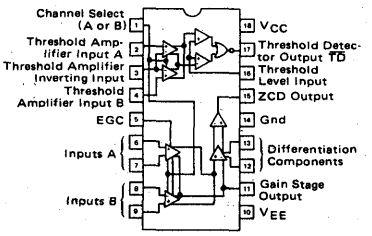
SILICON MONOLITHIC INTEGRATED CIRCUIT



LSI MAGNETIC MEMORY READ SUBSYSTEM

The MC3468 READ Subsystem when used with the MC3467 triple preamplifier provides the interface between magnetic tape heads and digital logic. This system is well suited for open-reel and cartridge magnetic tape systems. The MC3468 performs peak detection, and threshold detection functions as required for NRZI, Phase-Encoded or Group-Encoded recording formats. The device consists of: 1) Input Multiplex function, 2) Gain Stage with Electronic Gain Control (EGC), 3) Active Differentiation Amplifier, 4) Zero Crossing Detector (ZCD), 5) Threshold Detector Amplifier with Multiplexed Inputs and 6) Threshold Detector.

- Complete READ Function in One LSI Device
- Two Pair of Differential Inputs Allow Logically Controlled Selection of Input Filter or Tape Head Configuration
- Low Recovered Error Rate
- Input/Outputs are Low Power Schottky TTL Compatible



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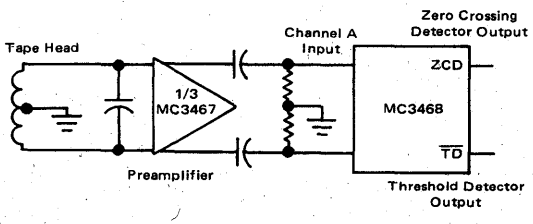
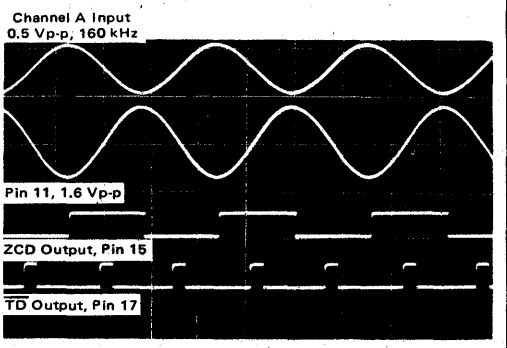
MC3468 TYPICAL APPLICATION AND WAVEFORMS





MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages			
Positive Supply Voltage	V_{CC}	+7.0	V
Negative Supply Voltage	V_{EE}	−8.0	V
Pin Voltages			
EGC Voltage (Pin 5)	$V_{I(EGC)}$	−5.0 to +7.0	V
Threshold Voltage (Pin 16)	$V_{I(T)}$	+1.0 to −3.5	V
ZCD Output (Pin 15)	$V_{O(ZCD)}$	+7.0	V
Channel Select A/B Input (Pin 1)	$V_{I(CS)}$	+7.0 to −2.0	V
Threshold Output $\overline{TD}$ (Pin 17)	$V_{O(\overline{TD})}$	+7.0	V
Differential Input Voltage			
Threshold Amplifier	$V_{ID(T)}$	±5.0	V
Gain Amplifier	V_{ID}	±5.0	V

MAXIMUM RATINGS (continued)

Rating	Symbol	Value	Unit
Common Mode Input Voltage			
Threshold Amplifier	$V_{IC(T)}$	±5.0	V
Gain Amplifier	V_{IC}	±5.0	V
Amplifier Output Short Circuit Duration (To Ground, Pin 11)	t_S	10	s
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = −6.0 V, T_A = 0 to +70°C unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
TOTAL DEVICE						
Power Supply Voltage Range @ T_A = 25°C						
Positive Supply Voltage		V_{CCR}	4.75	5.0	5.25	V
Negative Supply Voltage		V_{EER}	−5.5	−6.0	−7.0	V
Positive Supply Current	7	I_{CC}	–	35	45	mA
Negative Supply Current	7	I_{EE}	–	30	45	mA
Channel Select Input Voltage — Low Logic State		$V_{IL(CS)}$	–	–	0.8	V
Channel Select Input Voltage — High Logic State		$V_{IH(CS)}$	2.0	–	–	V
Channel Select Input Current — Low Logic State ($V_{IL(CS)}$ = 0, V_{CC} = 5.25 V)	6	$I_{IL(CS)}$	–	–	−100	μA
Channel Select Input Current — High Logic State ($V_{IH(CS)}$ = V_{CC} = 5.25 V)	6	$I_{IH(CS)}$	–	–	10	μA
GAIN AMPLIFIER SECTION						
Voltage Gain (Unbalanced) (e_i = 10 mV_{p-p})	1	A_V	6.5	7.5	8.5	V/V
Voltage Gain (Unbalanced) ($V_{I(EGC)}$ = V_{CC}, e_i = 800 mV_{p-p})	1	A_{VS}	–	0.05	0.1	V/V
Operating EGC Voltage Range		$V_{IR(EGC)}$	0	–	5.25	V
Maximum Differential Input Voltage (T_A = 25°C)		V_{IDR}	0.8	–	–	Vpp
Common Mode Rejection Ratio ($V_{I(EGC)}$ = 0, V_{CM} = 1.0 Vpp, f = 100 kHz, T_A = 25°C)	3	CMRR	40	80	–	dB
Bandwidth (−3.0 dB, T_A = 25°C)	1	BW	–	15	–	MHz
Input Resistance		r_i	30	60	–	kΩ
Channel Isolation (f = 100 kHz)			40	60	–	dB
Input Bias Current	4	I_{IB}	–	5.0	15	μA
Input Common Mode Voltage Range		V_{ICR}	±1.0	±1.5	–	V
Output Resistance (Pin 11) (T_A = 25°C)		r_o	–	15	30	Ohms
Output Sink Current (Pin 11)	5	I_{OS-}	1.2	2.1	–	mA
Output Voltage Swing (Pin 11)	1	V_{OR}	2.25	3.0	–	Vpp
Output Offset Voltage (T_A = 25°C)		V_{OO}	–	±400	–	mV

5

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = −6.0 V, T_A = 0 to +70°C unless otherwise noted) (Continued)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
ACTIVE DIFFERENTIATOR SECTION						
Timing Distortion (I = 1.0 mA, A = 1.5 Vpp, f = 100 kHz, T_A = 25°C)	12		–	1.0	3.0	%
Zero Cross Detector – High Level Output Current (V_{OH} = 5.5 V)	8	$I_{OH(ZCD)}$	–	–	150	μA
Zero Cross Detector – Low Level Output (I_{OL} = 8.0 mA)	9	$V_{OL(ZCD)}$	–	–	0.45	V
Differentiator Output Sink Current (Pins 12 and 13)	5	$I_{O(D)}$	1.0	1.4	–	mA
Differentiator Output Resistance (Unbalanced) (T_A = 25°C)		$r_{o(D)}$	–	20	–	Ohms
THRESHOLD AMPLIFIER SECTION						
Differential Voltage Gain		A_{VD}	8.5	10	11.5	V/V
Maximum Differential Input Voltage Without Distortion (T_A = 25°C)		$V_{IDR(T)}$	–	–	400	mVpp
Maximum Differential Input Voltage Before Timing Shift (T_A = 25°C)		$V_{IDR(T)}$	–	–	1.4	Vpp
Maximum Threshold Voltage (Linear Operation)		$V_{IR(T)}$	–	–	−1.0	V
Threshold Voltage Required to Disable Threshold Comparators ($V_{\overline{TD}}$ > 2.5 V, T_A = 25°C)		$V_{I(T)}$	–	−2.0	−2.5	V
Bandwidth (−3.0 dB, T_A = 25°C)		BW	–	15	–	MHz
Input Resistance		$r_{i(INT)}$	25	50	–	kΩ
Threshold Amplifier Bias Current		$I_{IB(T)}$	–	5.0	15	μA
Channel Isolation Ratio (f = 100 kHz)			40	60	–	dB
Threshold Detector Output Voltage – Low Logic State (I_{OL} = 8.0 mA, Pin 17)	10	$V_{OL(T)}$	–	–	0.45	V
Threshold Detector Output Current – High Logic State (V_{OH} = 5.5 V, Pin 17)	11	$I_{OL(T)}$	–	–	150	μA
Threshold Voltage Input Current (Pin 16)		I_{THC}	–	25	50	μA

DESCRIPTION OF FUNCTION

Input Multiplex – Input multiplexing allows logic-controlled (TTL compatible) selection of either of a pair of differential gain stages. Two separate tracks or one track processed through different filter networks for different recording formats can be selected (e.g., Phase Encoded/NRZI, Group-Coded/PE).

Gain Stage – The gain stage is controlled by Electronic Gain Control (EGC) and differential outputs are provided for the active differentiator and a single output is available for the threshold function. The EGC range is from essentially zero to 7.5 (unbalanced).

Active Differentiation – Active differentiation requires minimum external passive component count. The procedure for selecting component values insures linear operation and optimum zero-crossing detector performance for excellent noise rejection.

Zero Crossing Detector (ZCD) – The zero-crossing detector generates an output transition corresponding to the peak of the incoming signal to the MC3468. Careful attention has been paid to avoid timing distortion between the outputs of the active differentiator and the inputs of the zero crossing comparator. The output is open collector Schottky TTL.

Threshold Amplifier and Detector – The gain stage output is ac coupled or differentiated into the Threshold Amplifier multiplexer. This allows logic-controlled (TTL compatible) selection of either of a pair of single-ended to differential gain stages. Thus, the possibility of selecting between a differentiated or straight capacitive coupled signal for thresholding. The select line is the same as for the Gain Stage multiplexing. The unbalanced gain of the threshold amplifier is 5. An inverting input is available for balancing the input signal to minimize the effects of offset current. The differential outputs of the threshold amplifier are compared to an external threshold in the threshold comparators. An output signal is provided whenever the signal exceeds the threshold setting in the positive or negative direction. The output is open collector Schottky TTL.

The versatility of the MC3468 facilitates the design of dual mode (NRZI/PE, Group/PE) tape drives with the ability of dynamically switch gain, active differentiator components, and thresholds for different recording speeds or interchanged tapes.

MC3468 BLOCK SCHEMATIC

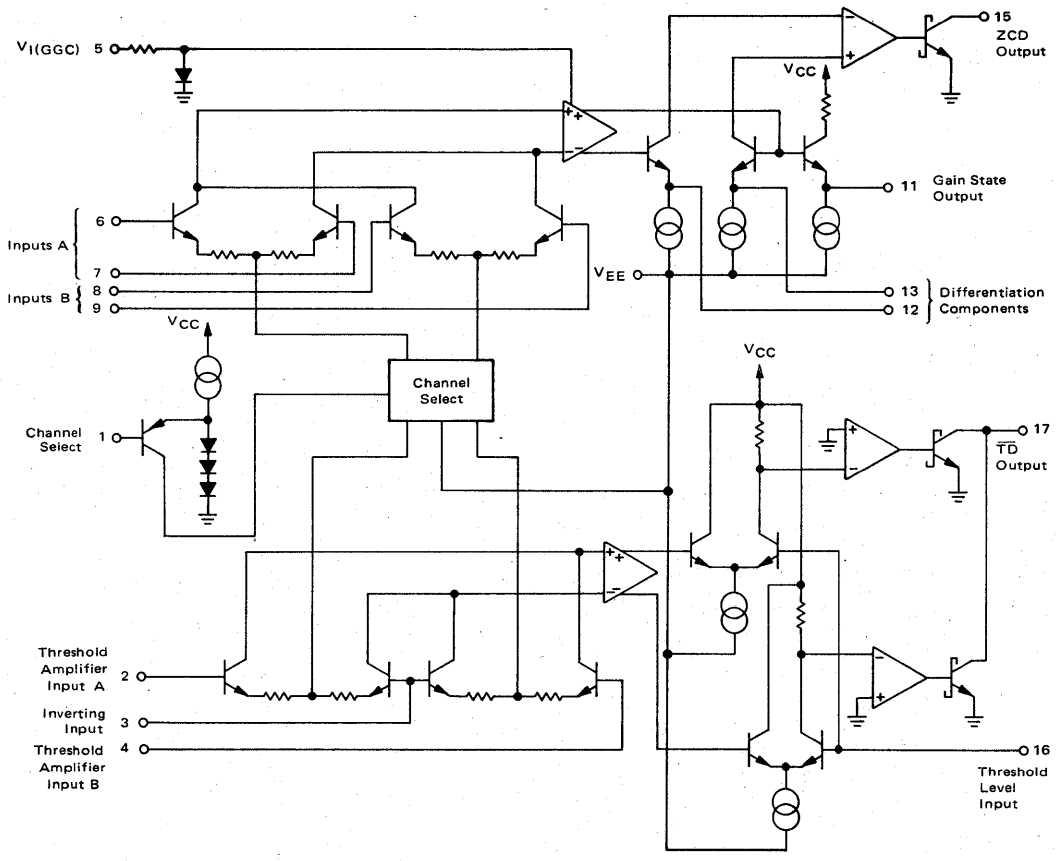


FIGURE 1 – VOLTAGE GAIN, BANDWIDTH AND OUTPUT VOLTAGE SWING

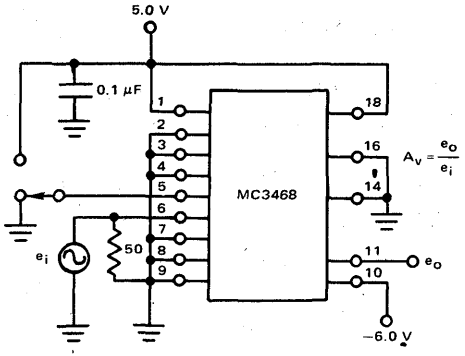


FIGURE 2 – CHANNEL ISOLATION RATIO

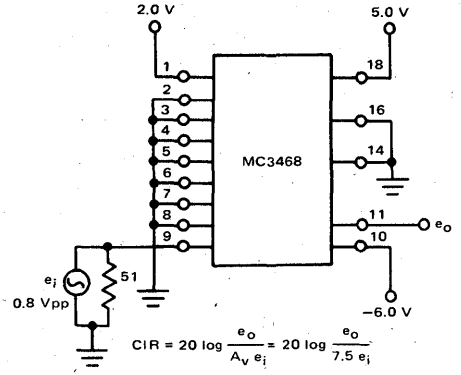


FIGURE 3 – COMMON MODE REJECTION RATIO (CMRR)

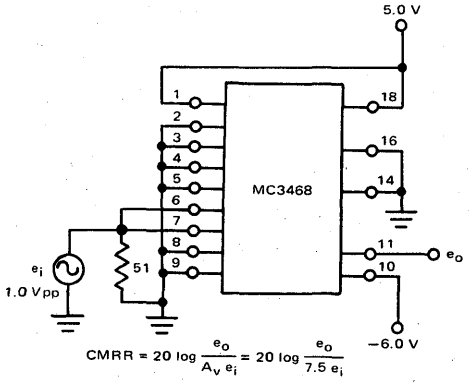


FIGURE 4 – INPUT BIAS CURRENT TEST CIRCUIT

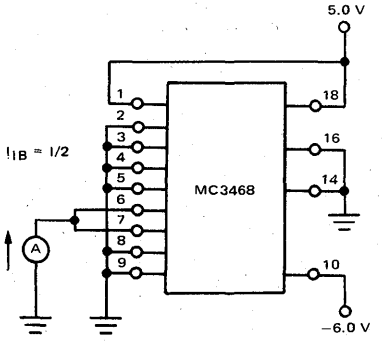


FIGURE 5 – OUTPUT SINK CURRENT AND DIFFERENTIATOR OUTPUT SINK CURRENT TEST CIRCUIT

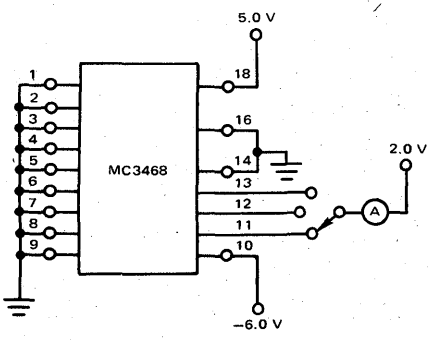


FIGURE 6 – CHANNEL SELECT INPUT CURRENT TEST CIRCUIT

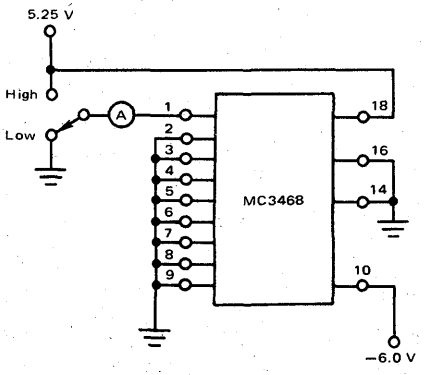


FIGURE 7 – POSITIVE AND NEGATIVE SUPPLY CURRENT TEST CIRCUIT

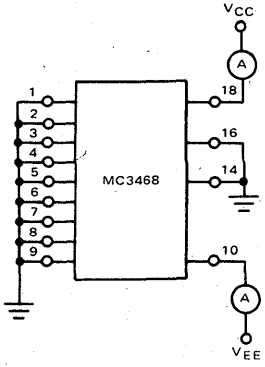


FIGURE 8 – ZERO CROSS DETECTOR OUTPUT CURRENT HIGH LOGIC STATE TEST CIRCUIT

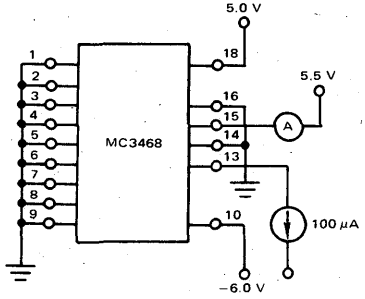


FIGURE 9 – ZERO CROSSING DETECTOR OUTPUT VOLTAGE LOW LOGIC STATE TEST CIRCUIT

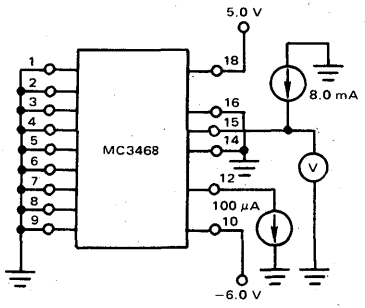


FIGURE 10 – THRESHOLD DETECTOR OUTPUT VOLTAGE – LOW LOGIC STATE TEST CIRCUIT

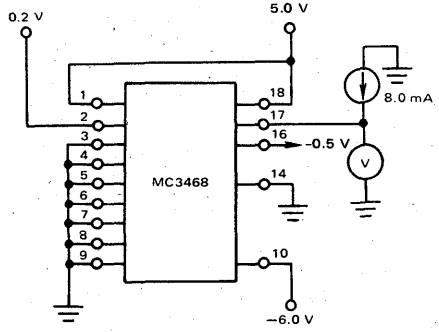


FIGURE 11 – THRESHOLD DETECTOR OUTPUT CURRENT – HIGH LOGIC STATE TEST CIRCUIT

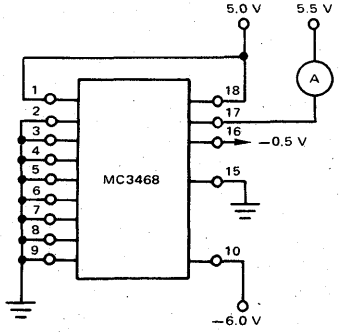
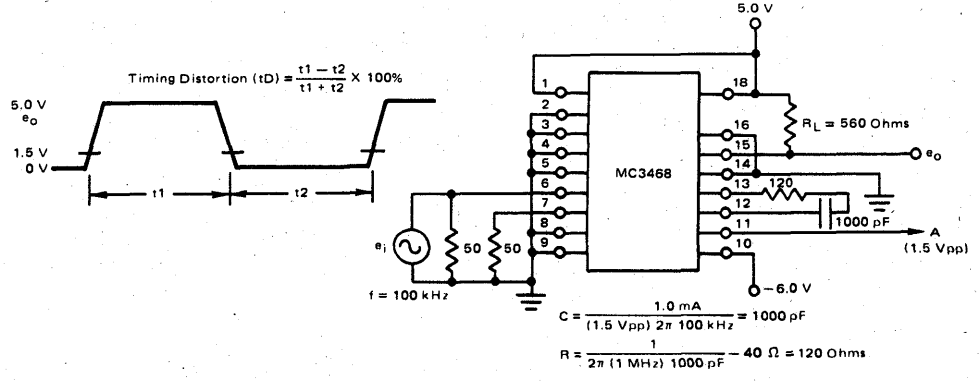


FIGURE 12 – TIMING DISTORTION $T_A = 25^oC$



TYPICAL PERFORMANCE CURVES

FIGURE 13 – NEGATIVE POWER SUPPLY CURRENT versus NEGATIVE POWER SUPPLY VOLTAGE

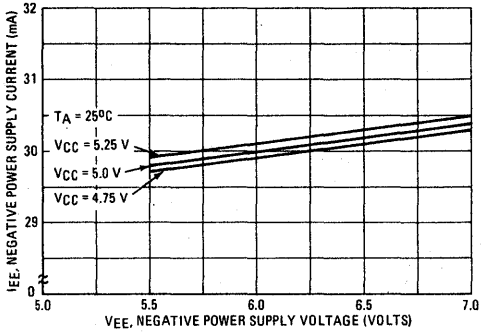


FIGURE 14 – NORMALIZED VOLTAGE GAIN versus EGC INPUT VOLTAGE

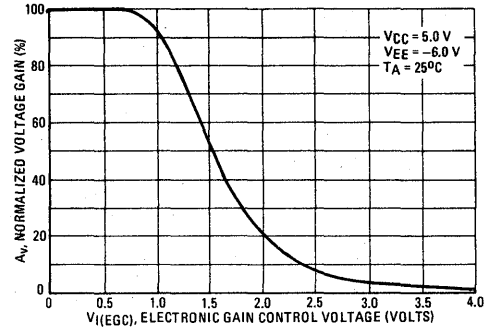


FIGURE 15 – ELECTRONIC GAIN CONTROL INPUT CURRENT versus VOLTAGE

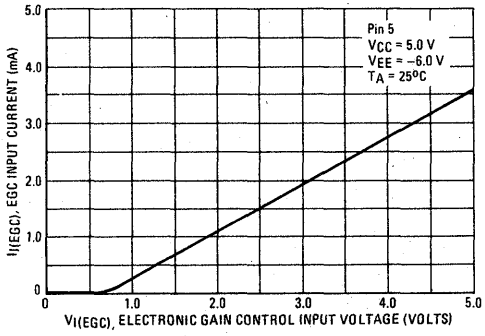


FIGURE 16 – CHANNEL ISOLATION RATIO versus FREQUENCY

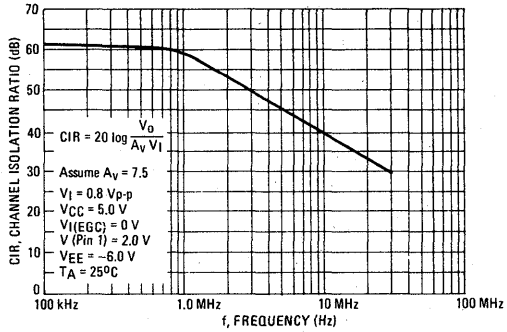


FIGURE 17 – PHASE versus FREQUENCY Gain Amplifier Inputs to Active Differentiator (Pins 6, 7 to 12, 13)

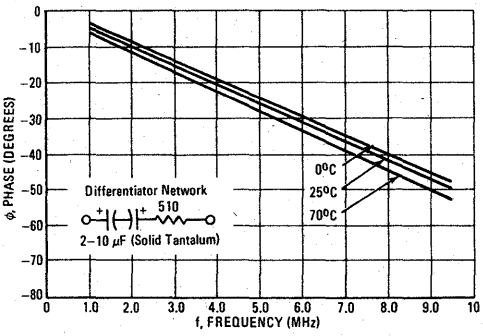
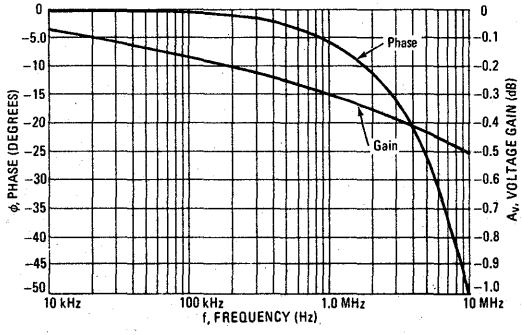


FIGURE 18 – GAIN AND PHASE versus FREQUENCY FROM Pins 6, 7 to Pins 12, 13



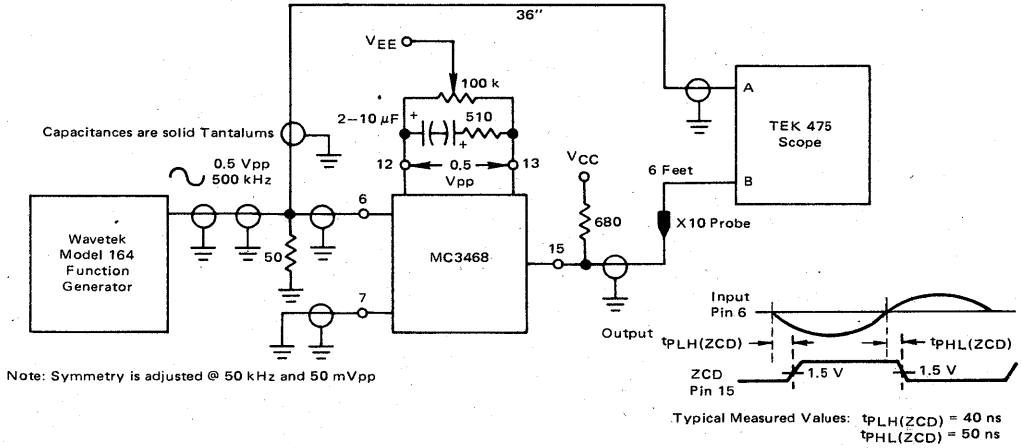
SYSTEM PARAMETERS

The following system parameters are characteristic of not only the device but external component values and circuit layout. Detailed test circuits and measured parameters are provided only as a guide to expected system performance. These parameters are not readily measureable on a production volume basis.

FIGURE 19 – TEST CIRCUIT FOR MEASURING PROPAGATION DELAYS

From Gain Stage Input to Zero Crossing Detector Output

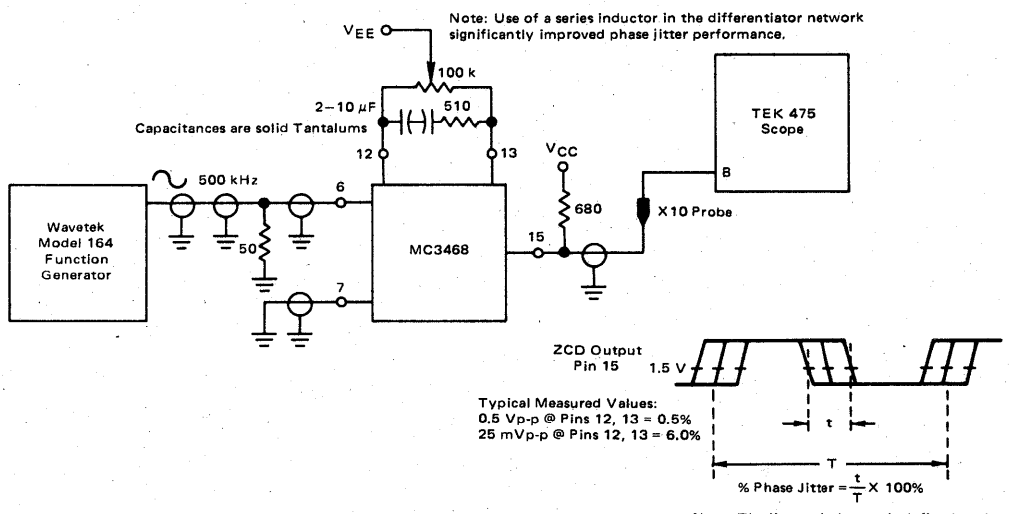
(Pin 6 to Pin 15) (Subtract 8 ns from measurement for probe and cable delays)



Note: Symmetry is adjusted @ 50 kHz and 50 mVpp

Typical Measured Values: $t_{PLH(ZCD)}$ = 40 ns
$t_{PHL(ZCD)}$ = 50 ns

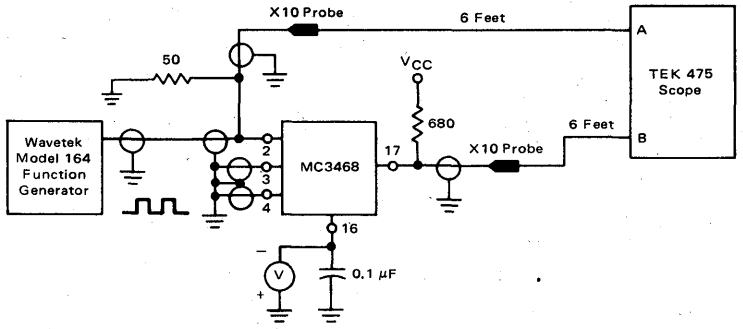
FIGURE 20 – TEST SETUP FOR MEASURING PHASE JITTER

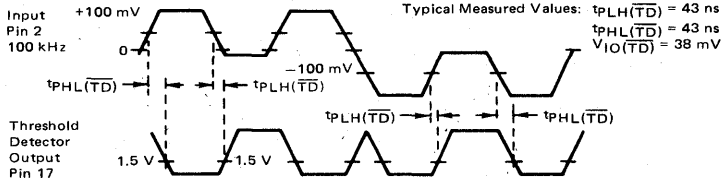


Typical Measured Values:
0.5 Vp-p @ Pins 12, 13 = 0.5%
25 mVp-p @ Pins 12, 13 = 6.0%

Note: The jitter window, t, is defined as the 3 σ points on a Gussion curve.

FIGURE 21 – TEST SETUP FOR THRESHOLD AMPLIFIER DELAY AND THRESHOLD COMPARATOR EQUIVALENT OFFSET MEASUREMENTS





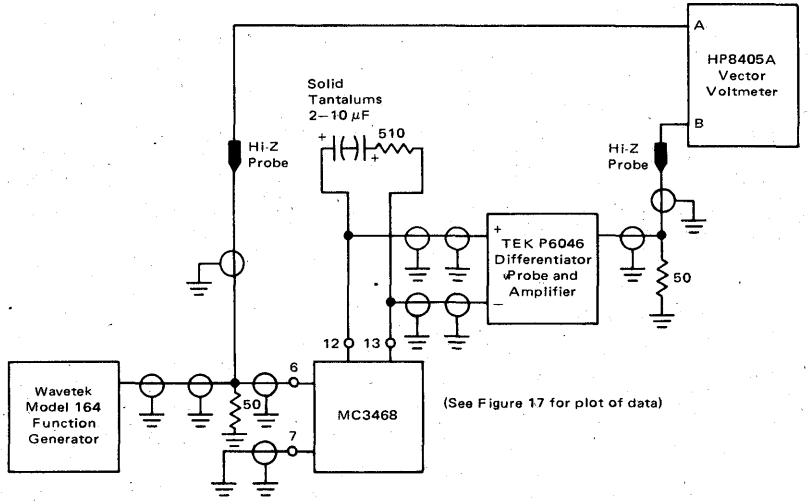
Typical Measured Values: $t_{PLH(\overline{TD})}$ = 43 ns, $t_{PHL(\overline{TD})}$ = 43 ns, $V_{IO(\overline{TD})}$ = 38 mV

Note: For Delay measurements, V is fixed at −250 mV; for equivalent comparator offset voltage measurements, V is adjusted until Pin 17 goes low. The voltage, V, is the equivalent offset, $V_{IO(\overline{TD})}$.

Note: Some compensation is possible using a resistor from Pin 3 to ground.

FIGURE 22 – TEST SETUP FOR GAIN AND PHASE versus FREQUENCY (1 MHz to 10 MHz) FROM INPUT TO DIFFERENTIATOR (Pin 6, 7 to Pin 12, 13)

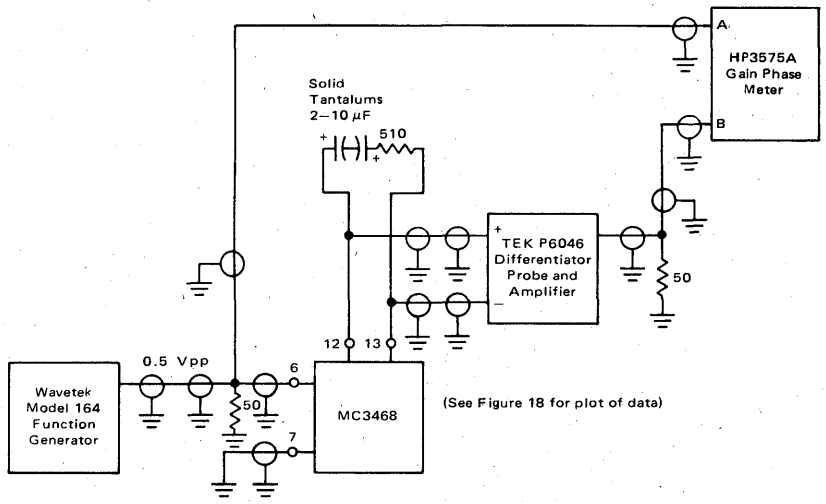
Actual Test Measurements (Calibrate Instrumentation for Phase Compensation)



(See Figure 17 for plot of data)

FIGURE 23 – TEST SETUP FOR GAIN AND PHASE versus FREQUENCY (5 kHz to 1 MHz) FROM INPUT TO DIFFERENTIATOR (Pin 6, 7 to Pin 12, 13)

Actual Test Measurements (Calibrate Instrumentation for Phase Compensation)



DESIGN SUGGESTIONS

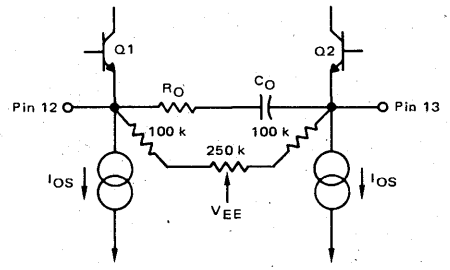
I Gain Stage Bias Current

One must consider supplying 15 μA of bias current to the Gain Stage when designing a filter network. A good design value for the equivalent resistance from each input leg to ground is 5 kΩ.

II Adjusting Peak Shift to Zero (See Figure 24)

The worst peak shift observed on the ZCD output occurs for the smallest slew rate provided by the Active Differentiator at the ZCD inputs. In Turn, the Active Differentiator produces the smallest slew rate when the gain-bandwidth product applied at its inputs is the smallest. Current source, resistors, and diode imbalances will exhibit the maximum peak shift under this condition. Using the resistor network shown, these imbalances are adjusted out for the worst case condition.

FIGURE 24 – PEAK SHIFT NETWORK



Note: The 100 kΩ resistors should be close to the IC to suppress noise.

MC3468 APPLICATIONS INFORMATION

MC3468 For NRZI Encoded Magnetic Tape

NRZI Encoding was one of the first popular recording formats and is formalized as an American National Standard for the purpose of facilitating the interchange of magnetic tapes. Although the Phase-Encoded format is now more widely accepted than NRZI, vast libraries of NRZI tapes still exist. Computers will be reading these tapes for years to come, and in some cases, re-writing them in phase-encoded format. Thus, the ability of the tape drive electronics to read both NRZI and PE tapes is a feature often sought in new designs.

For NRZI recording, the magnetic surface of the tape is magnetized to saturation in one direction or the other each time a logical "1" is to be recorded. The magnetization remains unchanged for a logical "0". The resulting signal from the read head for a typical NRZI data stream is shown in Figure 25. The NRZI data stream consists of a continuum of Fourier components up to a maximum frequency of $5f_H$, where f_H is numerically equal to one-half the maximum flux changes per second (FCPS). For long strings of zeroes, the lowest Fourier component could theoretically be near dc, but on a typical tape a long interval with no "1's" is not allowed. Consequently, most of the energy in the pulse train is around f_H and its harmonics (up to the fifth). A suitable corner frequency for ac coupling from the preamplifier is 60 Hz, although for high speed systems it could be considerably higher (1/10 fH). The -3 dB frequency of a low pass filter is usually placed at a frequency greater than f_H. In most systems, this low pass filter must do more than provide a roll-off for high-frequency transients. It also equalizes the read amplifier chain and differentiation network for linear phase versus frequency response. Once the transfer function of this equalization filter is known, it may be incorporated either as part of the ac coupling between the preamplifier and amplifier or as part of the differentiation network.

The American National Standard specifies that NRZI be recorded at 800 BPI (Bits Per Inch) on open reel magnetic tape. Typical read/write tape speeds range from 12.5 to 300 IPS (Inches Per Second). Examples 1 and 4 show MC3468 NRZI designs.

MC3468 For Phase-Encoded (PE) Magnetic Tape

Of the numerous methods for encoding digital data on magnetic tape, phase encoding is currently most popular. As shown in Figure 25, data is represented by transitions occurring in the middle of a "data cell". A low-to-high flux transition (toward the magnetization level representing erased tape) is defined as a logical "one" and a high-to-low transition is defined as a logical "zero". For consecutive "one's" or "zero's" phase transitions are introduced as needed at the "data cell" borders. Phase transitions are not required when the encoded data consists of "one-zero" patterns.

The read head signal resulting from mixed data streams consists of two fundamental frequencies, f_H and f_L which represent most of the harmonic content (with some energy at harmonics up to the fifth). These are numerically equal to $\frac{FCPI}{2} \times IPS$ and $\frac{FCPI \times IPS}{4}$ (where FCPI is maximum flux changes per inch and IPS is tape speed in inches per second). In high-speed, low-level systems, the amplitude of these read head signals is only a few millivolts and conditioning with a preamplifier such as the MC3467 followed by a passive bandpass filter is required. The bandpass characteristic sets the lower −3 dB frequency below f_L and the upper −3 dB frequency above f_H. In most systems, the bandpass filter must do more than filter out noise. The low-pass portion also equalizes the read amplifier chain and differentiation network for a linear phase versus frequency response. Once the transfer function of this equalization filter is known, it may be incorporated as part of the filter between the preamplifier and amplifier or as part of the differentiation network.

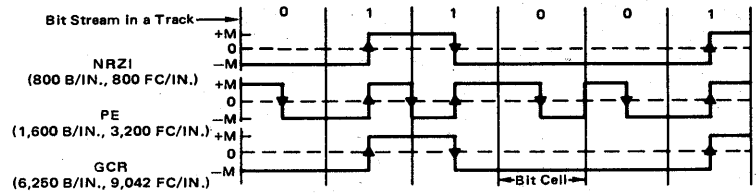
The American National Standard specifies that PE data be recorded at 1600 BPI (Bits Per Inch) on open reel magnetic tape. Typical read/write tape speeds range from 6.25 to 200 IPS (Inches Per Second). Cartridges use 1600 BPI and have tape speeds of 30 IPS for read/write. Examples 2, 3, and 4 show MC3468 designs for PE systems.

MC3468 For Group Code Recorded (GCR) Magnetic Tape

Basically, Group-Coded Recording (GCR) is a high density recording scheme which uses the NRZI convention for "1's" and "0's", but adds the restriction that flux changes occur at least once in every three bit cells (Figure 25). The read head signal resulting from mixed data streams consists primarily of Fourier components from f_L to $3f_L = f_H$ and their harmonics up to the fifth. The frequencies f_L and f_H are numerically equal to $\frac{FCPI \times IPS}{2}$ and $\frac{FCPI \times IPS}{6}$, respectively (where FCPI is maximum flux changes per inch and IPS is tape speed in inches per second). The amplitude of the read head signals is only a few millivolts or less and conditioning with a preamplifier such as the MC3467 followed by a passive bandpass filter is required. The bandpass characteristic sets the lower −3 dB frequency below f_L and the upper −3 dB frequency above f_H. The bandpass filter must do more than filter out noise. The low pass portion equalizes the read amplifier chain and differentiation network for linear phase versus frequency response. Once the transfer function of this equalization filter is known, it may be incorporated as part of the filter between the preamplifier and amplifier or as part of the differentiation network.

The proposed American National Standard specifies that GCR data be recorded at 9042 FCPI (Flux Changes Per Inch). Because of the data format, the usable data density is 6250 BPI rather than 9042 BPI. The "6250 BPI" is a throughput specification and should not be used in read amplifier calculations. The original GCR concept was intended for high speed drives (200 IPS). However, it is also being applied to lower speed (125 IPS) systems. Examples 5 and 6 illustrate the use of the MC3468 in GCR systems.

FIGURE 25 – MOST POPULAR MAGNETIC TAPE RECORDING FORMATS



CIRCUIT OPERATION

(See Figure 26 for component wiring and Figures 27 and 28 for Timing Diagrams)

The operation of the MC3468 is similar for NRZI, PE, and GCR data formats. The preamplifier and filtered signal is applied differentially to either Channel A or B Gain Stages. The Gain Stage output differentially feeds an Active Differentiator and a single-ended output is available for straight capacitive or differentiated (active or passive) coupling into either Channel A or B inputs to the Threshold Amplifier.

For the circuit configuration shown, the Active Differentiator output leads the input by almost 90°. The Active Differentiator output is applied to a Zero-Crossing Detector, which goes low for positive levels and high for negative levels, changing state at the zero crossings. The Threshold Circuit amplifies the Gain Stage output and compares positive and negative signals to a threshold level. When the level is exceeded, the $\overline{TD}$ output is low. From the waveforms, it is seen that the ZCD output makes a transition approximately in the middle of the period when $\overline{TD}$ is low. Wiring ZCD "anded" with TD to the set input and $\overline{ZCD}$ "anded" with TD to the "reset" input of the R-S type flip-flop reconstructs the data stream encoded on the tape. This circuit works for zero clip (zero threshold) operation, but has the disadvantage that timing distortion results from capacitive loading. Digital circuits for reconstructing the data stream which utilize pipe-line delays to overcome capacitive loading timing distortion are shown in Figure 29.

FIGURE 26 – TYPICAL MC3468 COMPONENT HOOKUP

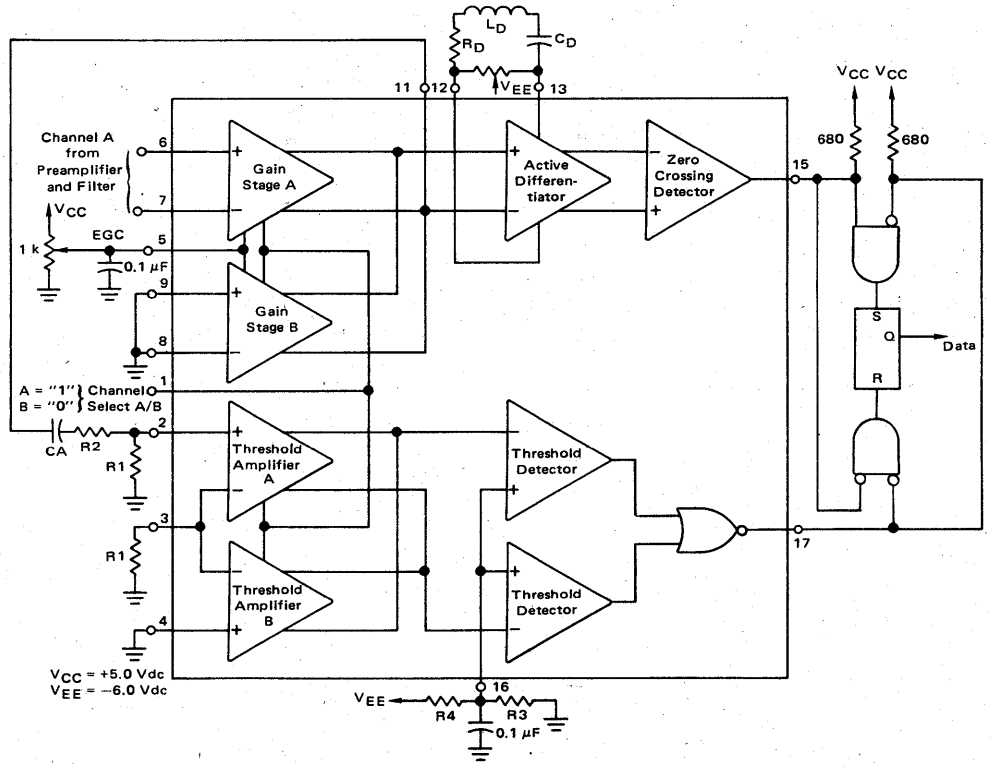


FIGURE 27 – WAVEFORMS SHOWING MC3468 OPERATION FOR NRZI DATA

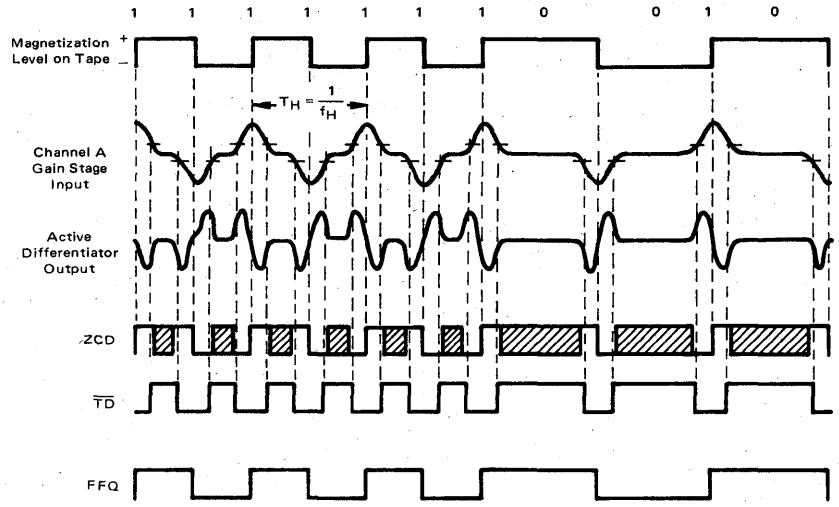


FIGURE 28 – TIMING DIAGRAM WAVEFORMS SHOWING MC3468 OPERATION FOR PHASE-ENCODED DATA

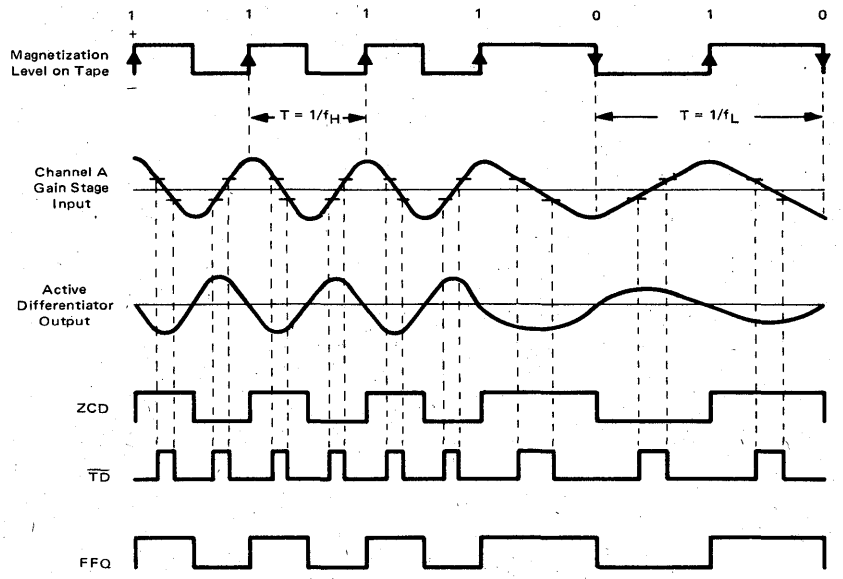
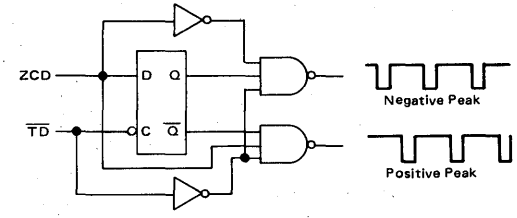
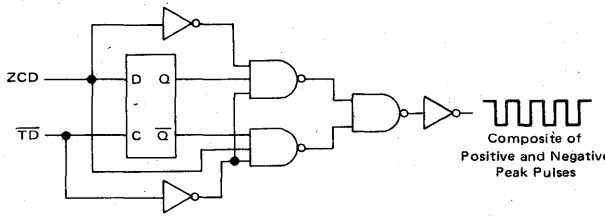


FIGURE 29 – OTHER DIGITAL CIRCUITS FOR RECONSTRUCTING DATA STREAMS FROM THE MC3468

1) Dual Output Circuit (Pipeline Delay for Negative Edge Must Be the Same for Both Outputs)



2) Single Output Circuit (Operation Independent of Capacitive Loading Effects on Delays)



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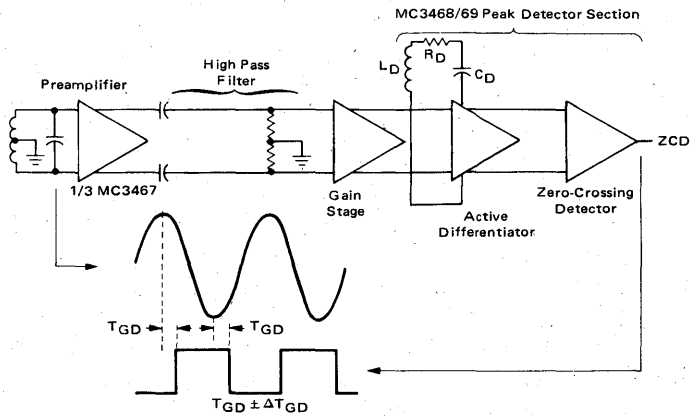
Group Delay Distortion

The ultimate purpose of the magnetic read amplifier chain in Figure 30 is to produce a digital signal with transitions corresponding to the peaks of a read head signal. Because the active and passive elements in the chain exhibit phase characteristics, there will be a "pipe-line" delay between peaks at the read head and the digital output from the zero-crossing detector. Variations in this delay with frequency or amplitudes cause timing distortion which translates directly into increasing error rates. The primary consideration in the read chain implementation is to equalize the read chain for almost flat delay over the frequencies and amplitudes of required operation. Figure 30 depicts one of several possible read chain configurations which can be equalized for best-flat time delay performance.

The determination of the component values is relatively straight forward provided the active elements have negligible phase characteristics in the frequency range of operation. Below 1 MHz, the MC3467/MC3468 read chain active elements have negligible phase characteristics. Although phase effects start showing above 1 MHz, phase versus frequency is linear (constant time delay) as shown in Figure 17 for the MC3468 Gain Stage.

Other read chain configurations have a band-pass filter between the preamplifier and Gain Stage. It is possible to move some of the poles of the filter into the active differentiator. The technique suggested in Figure 30 transfers poles into the active differentiator to minimize component count. The insertion loss of the technique is also less than an equalization filter ahead of the READ amplifier.

FIGURE 30 – GROUP DELAY DISTORTION THROUGH READ CHAIN

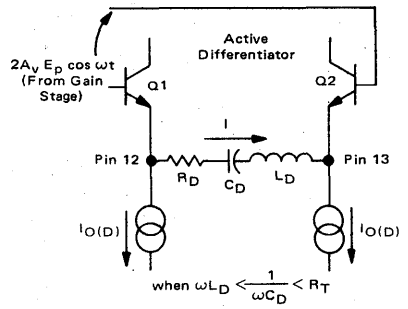


Determining R_D, C_D, and L_D For the Active Differentiator

For the equalized read chain shown in Figure 30, C_D, R_D and L_D are determined respectively in that order. The phase characteristics of the active elements are assumed to be negligible.

An active differentiator is formed by R_D, C_D and L_D coupling the emitters of a differential amplifier having current sources I_{OD} in each leg. If a differential voltage $A_V E_p \cos \omega t$ is applied to the Active Differentiator, the resulting current through R_D and C_D is:

$$I = \frac{2A_V E_p}{\sqrt{R_T^2 + \left(\frac{1}{\omega C_D} + \omega L_D\right)^2}} \cos\left\{\omega t - \arctan\left(\frac{-1/\omega C_D}{R_T}\right)\right\}$$



$I \cong 2A_V E_p C_D \omega \sin \omega t$

where $2A_V E_p$ is the product of the differential input to the Gain Stage E_p and its unbalanced gain, A_V.
where R_T is the total of R_D and the output impedances of Q1 and Q2. The combined output impedances of Q1 and Q2 is 40 Ohms.

This condition is approximated for $\frac{1}{R_T C_D} = \omega_C = 3\omega_H$ (where ω_H is the maximum applied frequency of appreciable Fourier content).

The peak value of I (i.e., $2A_V E_p C_D \omega$) is important. As I approaches $I_{O(D)}$, the transistor Q2 turns off and the waveform at Pin 12 distorts. The circuit no longer behaves as a differentiator and peak distortion results.

For best zero crossing detector performance, it is essential that I be maximized. A design value of I which results in good noise performance and minimum peak shift is 900 microamperes.[1]

$$I = 2A_V E_p C_D \omega = 900 \times 10^{-6}$$

Rearranging the equation for I,

$$C_D = \frac{900 \times 10^{-6}}{2A_V E_p \omega}$$

Also, solving $\omega_C = \frac{1}{R_T C_D}$ for R_T,

$$R_T = \frac{1}{\omega_C C_D}$$

Assuming the output impedance of Q1 and Q2 combined is 40 Ohms,

$$R_D = \frac{1}{\omega_C C_D} - 40$$

where $\omega_C = 3\omega_H$.

As shown in Table 1, the addition of an inductor, L_D, significantly improves phase linearity versus frequency as well as providing a roll off for high frequency noise. This optimum solution requires the following relationships:

$$\frac{2}{R_T C_D} = \frac{R_T}{L_D}$$

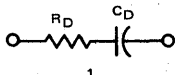
rearranging,

$$L_D = \frac{R_T^2 C_D}{2}$$

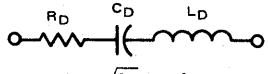
[1] For optimum zero-crossing detector performance, dI/dt should be as large as possible at zero-crossing.

Motorola guarantees a minimum $I_{O(D)}$ of 1.0 mA.

TABLE 1 – PHASE LINEARITY (CONSTANT TIME DELAY) PERFORMANCE FOR RC versus RLC ACTIVE DIFFERENTIATOR NETWORK



$\omega_C = \frac{1}{R_D C_D} = 3\omega_H$



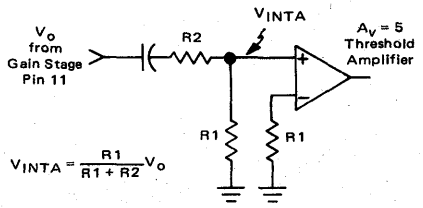
$\omega_n = \frac{\sqrt{2}}{R_D C_D} = \frac{1}{\sqrt{LC}}$

$\frac{\omega}{\omega_C}$	θ	$\Delta\theta$	$\frac{\omega}{\omega_n}$	θ	$\Delta\theta$
1.0	+45.00		1.0	0	
0.9	+48.01	+3.01	0.9	+8.49	+8.49
0.8	+51.34	+3.33	0.8	+17.65	+9.16
0.7	+55.01	+3.67	0.7	+27.26	+9.61
0.6	+59.04	+4.03	0.6	+37.03	+9.77
0.5	+63.43	+4.39	0.5	+46.69	+9.66
0.4	+68.20	+4.77	0.4	+56.04	+9.35
0.3	+73.30	+5.10	0.3	+65.00	+8.96
0.2	+78.69	+5.39	0.2	+73.58	+8.58
0.1	+84.29	+5.60	0.1	+81.87	+8.29

Threshold Considerations

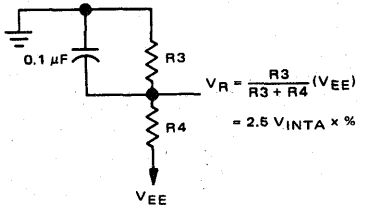
The threshold circuitry is used in read after write systems to insure that good data was written, to set up gain during an ID burst, and sometimes to indicate a minimum signal voltage for invalid data. Optimum thresholding requires a large swing at the threshold amplifier inputs. A good design value for V_{INTA} is 1.0 Vp-p, and should not exceed 1.4 Vp-p. If it does, a timing shift results. Internal clipping is provided for all signals greater than 400 mVp-p. The distortion resulting from clipping has no effect on thresholding because only peaks are clipped.

As shown in Figure 26, the Gain Stage output at Pin 11 is ac coupled to the threshold amplifier so that voltage offsets do not influence thresholding. An attenuator, R1/R2, is often required in the ac coupling networks because the gain stage output is between 1.6 Vp-p and 2.4 Vp-p for optimum zero-crossing-detector performance.



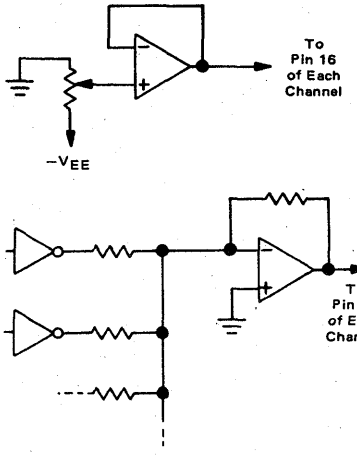
The magnitude of R1 should be less than 5 kΩ to minimize the effects of Threshold Amplifier Bias current (I_{THA} = 15 μA). Also, R1 + R2 must be greater than 3 kΩ because the minimum output sink current (I_{OS}) of the Gain Stage is 1.5 mA. A resistance equal to R1 should be wired to ground from the – leg of the Threshold Amplifier (minimize offset bias current effects).

Note that only the selected amplifier input contributes to bias current. Each output of the Threshold Amplifier is 5 V_{INTA}, and is applied to its resepctive Threshold comparator. Each comparator sees 2.5 V_{INTA}. Thresholding is based on a percentage of the nominal voltage applied to the comparators, 2.5 V_{INTA}. Both positive and negative references are derived from V_{EE} as follows:



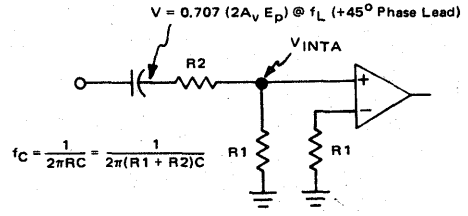
R3 should be less than 1 kΩ to minimize the effects of Threshold Comparator Bias Current (I_{THC} = 50 μA). A 0.1 μF decoupling capacitor is required for transients.

The following circuits are useful for multi-channel and/or dynamic threshold switching applications.



Base Line Shift in PE Systems

In phase-encoded recording, the read signal may not make symmetrical transitions about the zero bias level. A lower amplitude signal with a low frequency component is often superimposed. Although a highpass filter attenuates some of this component, its frequency is often close to the –3 dB frequency of the filter and may be only –6 dB down from signal amplitudes. This baseline shift has no adverse effects on the performance of the Active Differentiator. However, the Threshold Detector is sensitive to the unequal signal peaks. Signal-to-noise ratio can be improved by performing a passive differentiation into the Threshold Amplifier. With the corner frequency, f_C, placed at f_L, the f_L signal is attenuated –3 dB; the $f_H = 2f_L$ signal is for all practical purposes unattenuated. Figure 31 shows the 45° phase lead introduced by passive differentiation. Note that this technique is not directly applicable to high thresholds because the ZCD transitions fall outside the thresholding window. However, the threshold window can be delayed to overcome this drawback.



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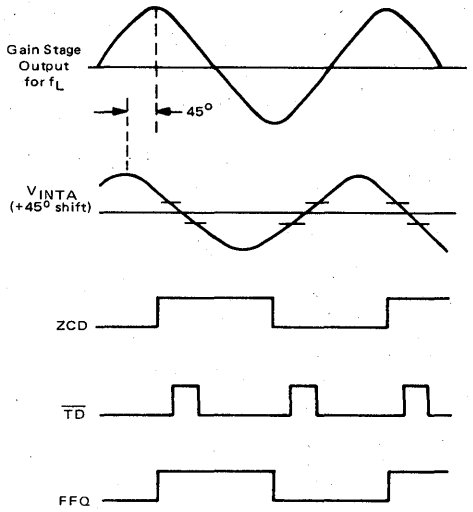
The design of the attenuator, R1/R2, follows as described previously. Example 3 shows a typical application of passive differentiation to overcome base-line shift.

FIGURE 31 – RESULTING OPERATION FOR PASSIVE DIFFERENTIATION INTO THRESHOLD AMPLIFIER



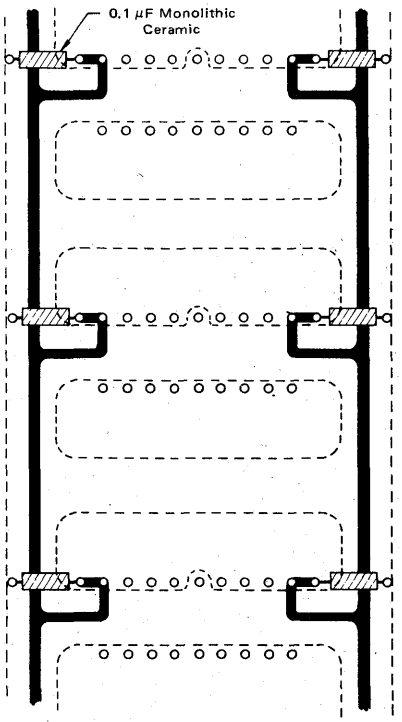
Board Layout and Testing Considerations

An LSI package has many input/output pins in close proximity, some carrying high level signals and others low level signals. As carefully as the on-chip isolation of the devices connected to these pins is implemented by the manufacturer, the coupling of signals or noise between external wires is under the control of the end-user who designs the integrated circuit into a piece of equipment. The designer should be familiar with the following layout procedures which will optimize the performance of the device. See Figure 32.

1. Build all circuits on printed circuit boards (including breadboards). Transmission line theory for flat conductors in a plane quite convincingly proves that coupling is far less than for round conductors in 3-dimensions.
2. Use a ground plane under the IC and over as much of the printed circuit board surface as possible without exceeding practical limits.
3. Avoid signal runs under the IC, also avoid parallel runs of 1 inch or greater on the opposite or same side of board.
4. Use monolithic ceramic 0.1 μF capacitors for decoupling power supply transients. One from V_{CC} to ground and one from V_{EE} to ground for each IC package. Keep lead lengths to ¼ inch or less and place in close proximity to the IC.
5. Keep all signal runs as short as possible. The lead on Pin 15 will radiate and can couple back into the active differentiator. This will result in excessive phase jitter. The tell-tale behavior is a ringing at Pin 11 corresponding to the transitions at Pin 15. To overcome this coupling problem, keep the lead on Pin 15 short and isolated from the other Input/Output lines to the MC3468. Preferably, put it over or next to a ground plane. For long distance runs, use a twisted pair or coaxial cable.

When evaluating the device for phase jitter and frequency response, a special test jig should be designed to reduce ground loops and coupling caused by instrumentation. Instrumentation test set-ups must be calibrated at each test frequency and differential equipment utilized where required. A valid evaluation of the performance of any read amplifier chain requires considerable care and thought.

FIGURE 32 – POWER AND GROUND DISTRIBUTION FOR MC3468 PRINTED CIRCUIT BOARD LAYOUT



Note: Dotted Lines Outline Ground Plane on Back Side of Printed Circuit Board

EXAMPLES

Example #1 (See Figure 26 for Component Hookup)

Tape Drive Type: Open Reel
Encoding: NRZI
Recording Density: 800 BPI (800 FCPI)
Tape Speed: 200 IPS
Signal into Gain Stage

$$E_{pp} = 0.3 \text{ to } 0.6 \text{ Vp-p @ } 80 \text{ kHz}$$

Threshold: 25% of minimum voltage peaks

The voltage from the Gain Stage is designed for 1.6 Vp-p at Pin 11.

$$\frac{1.6}{0.6} = A_V = 2.7$$

Set the EGC for a gain of 2.7, unbalanced.

The maximum p-p voltage to the Threshold Amplifier, V_{INTA}, is designed for 1 Volt. The required attenuation factor is $\frac{1}{1.6}$.

$$\frac{V_{INTA}}{V_O} = \frac{R1}{R1 + R2} = \frac{1}{1.6}$$

$R1 + R2 \geq 3\ k\Omega$ and $R1 \leq 5\ k\Omega$ (See text)

These constraints are satisfied when $R1 = 4.7\ k\Omega$ and $R2 = 3\ k\Omega$. This is an optimum solution for a minimum coupling capacitor value.

Now consider the minimum voltage applied to the Threshold Amplifier

$$V_{INTA(MIN)} = \frac{1}{1.6} \times 2.7 \times 0.3 = 0.5 \text{ Vp-p.}$$

The threshold comparator reference voltage, V_R, is set at 25% of $2.5 V_{INTA(MIN)}$

$$V_R \approx 0.25 \times 2.5 \times 0.5 \cong 300 \text{ mV}$$

$$-300 \times 10^{-3} = \frac{R3}{R3 + R4}(-6)$$

$R3 \leq 1\ k\Omega$ (See text)

Let $R3 = 470\ \Omega$; then $R4 \cong 10\ k\Omega$

The values of R_D and C_D are determined from the equations given in the text.

$$C_D = \frac{900 \times 10^{-6}}{2A_V E_p \omega} = \frac{900 \times 10^{-6}}{A_V E_{pp} \omega}$$

$$= \frac{900 \times 10^{-6}}{2.7 \times 0.6 \times 2\pi \times 80 \times 10^3}$$

$$C_D \cong 1000 \text{ pF}$$

Assume $f_C = 3f$

$$R_D = \frac{1}{\omega C C_D} - 40 = \frac{1}{2\pi \times 3 \times 80 \times 10^3 \times 10^{-9}} - 40$$

$$R_D = 670 - 40 \cong 600\ \Omega$$

$$L_D = \frac{R_T^2 C_D}{2} = \frac{(670)^2 \times 10^{-9}}{2} = 224\ \mu H$$

Example #2 (See Figure 26 for Component Hookup)

Tape Drive Type: Open Reel
Encoding: Phase-Encoded
Recording Density: 1600 BPI (3200 FCPI)
Tape Speed: 200 IPS
Signal Into Gain Stage

$$E_{pp} = 0.2 \text{ Vp-p @ } 320 \text{ kHz}$$
$$0.4 \text{ Vp-p @ } 160 \text{ kHz}$$

Threshold: 25% of minimum voltage peaks

The voltage from the Gain Stage is designed for 1.6 Vp-p at Pin 11.

$$\frac{1.6}{0.4} = A_V = 4$$

Set the EGC for a gain of 4, unbalanced.

The maximum p-p voltage to the Threshold Amplifier, V_{INTA}, is designed for 1 Volt. The required attenuation factor is $\frac{1}{1.6}$.

$$\frac{V_{INTA}}{V_O} = \frac{R1}{R1 + R2} = \frac{1}{1.6}$$

$R1 + R2 \geq 3\ k\Omega$ and $R1 \leq 5\ k\Omega$ (See text)

These constraints are satisfied when $R1 \cong 4.7\ k\Omega$ and $R2 \cong 3\ k\Omega$. This is an optimum solution for a minimum coupling capacitor value. Now consider the minimum voltage applied to the Threshold Amplifier.

$$V_{INTA(MIN)} = \frac{1}{1.6} \times 4 \times 0.2 = 0.5 \text{ Vp-p}$$

The threshold comparator reference voltage, V_R, is set at 25% of $2.5 V_{INTA(MIN)}$

$$V_R = 0.25 \times 2.5 \times 0.5 \cong 300 \text{ mV}$$

$$-300 \times 10^{-3} = \frac{R3}{R3 + R4}(-6)$$

$R3 \leq 1\ k\Omega$ (See text)

Let $R3 = 470\ \Omega$; then $R4 \cong 10\ k\Omega$

The values of R_D and C_D are determined from the equations given in the text.

$$C_D = \frac{900 \times 10^{-6}}{2A_V E_{pp}} = \frac{900 \times 10^{-6}}{A_V E_p} = \frac{900 \times 10^{-6}}{4 \times 0.4 \times 2\pi \times 160 \times 10^3}$$

$$C_D \cong 560 \text{ pF}$$

Assume $f_C = 3f_H$

$$R_D = \frac{1}{W_C C_D} - 40$$

$$= \frac{1}{2\pi \times 3 \times 320 \times 10^3 \times 5.6 \times 10^{-10}} - 40$$

$$R_D = 295 \text{ ohms} - 40 \cong 250\ \Omega$$

$$L_D = \frac{R_T^2 C_D}{2} = \frac{(295)^2 \times 560 \times 10^{-12}}{2} = 24\ \mu H$$

Example #3 (See Figure 26 for Component Hookup)

Same as Example #2, but consider base-line shift.

In addition to ac coupling between the Gain Stage and Threshold, a passive differentiation is performed to attenuate the lower frequencies producing base-line shift. This improves signal-to-noise ratio. The corner frequency is chosen at $f_L = 160$ kHz where the attenuation is 0.707 (−3 dB) and the phase angle is +45°.

$$f_L = \frac{1}{2\pi C (R1 + R2)} = 160 \times 10^3$$

For $C = 200$ pF

$$R1 + R2 \cong 5\ k\Omega$$

Now $\frac{R1}{R1 + R2} = \frac{1}{1.6 \times 0.707} = 0.9$

Let $R1 = 4.7\ k\Omega$, then $R2 = 470\ \Omega$

Example #4 (See Figure 33 for Component Hookup)

Tape Drive Type: Open Reel
Encoding: Dual Mode (Phase-Encoded/NRZI)
Recording Density: 1600 BPI (3200 FCPI) for PE mode and 800 BPI (800 FCPI) for NRZI mode
Tape Speed: 200 IPS
Signal Into Gain Stage

Same as Examples 1 and 2

Threshold: 25% of minimum voltage peaks

NOTE: Consider base-line shift for PE mode.

This tape drive performs either the NRZI or the PE functions of Examples #1 and #3, under control of the SEL A/B line. Using the Gain Stage and Threshold Amplifier Channel A, Channel B inputs, the hook-up for a single track is implemented as shown in Figure 33. Note that an electronic switch is required for Gain switching when the mode is changed. This particular design did not require the threshold voltage to be switched, although in a typical system it probably would be.

It is necessary to electronically switch differentiator components. A low impedance MOSFET switch is shown.

Example #5 (See Figure 26 for Component Hookup)

Tape Drive Type: Open Reel
Encoding: Group Code
Recording Density: 6250 BPI, 9042 FCPI
Tape Speed: 200 IPS
Signal Into Gain Stage

E_{pp} = 0.1 Vp-p @ 900 kHz = f_H

E_{pp} = 0.3 Vp-p @ 300 kHz = f_L

Considerations for setting Gain Stage EGC, coupling (passive differentiation for base-line shift or straight ac) into the Threshold Amplifier, and Threshold setting are similar to the previous examples. For Group-coded data the EGC setting can be electronically locked during the ID burst in conjunction with Threshold setting. (See Figure 34.)

Values for C_D and R_D

$$C_D = \frac{900 \times 10^{-6}}{2A_v E_p \omega}$$

$$= \frac{900 \times 10^{-6}}{A_v E_{pp} \omega} = \frac{900 \times 10^{-6}}{5.3 \times 0.3 \times 2\pi \times 300 \times 10^3}$$

$C_D \cong 300$ pF

Assume $f_C = 3f_H$

$$R_D = \frac{1}{\omega_C C_D} - 40 = \frac{1}{2\pi \times 3 \times 900 \times 10^3 \times 300 \times 10^{-12}} - 40$$

$R_D = 200 - 40 = 160$ Ohms

$$L_D = \frac{R_T^2 C_D}{2} = \frac{(200)^2 \times 300 \times 10^{-12}}{2} = 6\ \mu H$$

Example #6 (See Figure 26 for Component Hookup)

Same as Example #5 except 125 IPS tape speed.

Signal Into Gain Stage

E_{pp} = 0.3 Vp-p @ 565 kHz

E_{pp} = 0.6 Vp-p @ 188 kHz

C_D = 300 pF, R_D = 250 Ω

L_D = 12.6 μH

FIGURE 33 – MC3468 COMPONENT HOOKUP FOR DUAL MODE PE/NRZI EXAMPLE #4

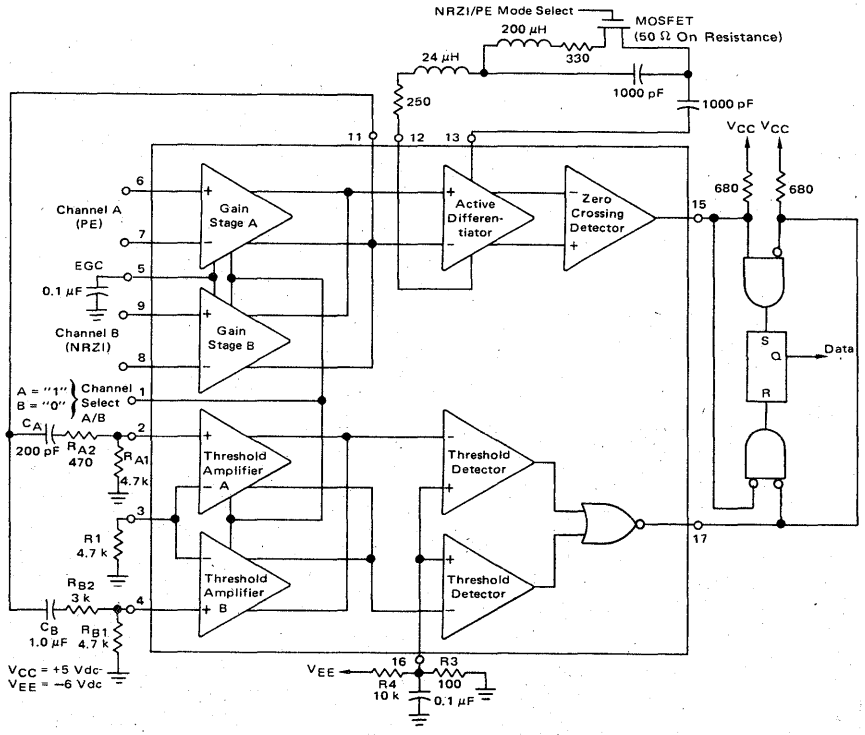
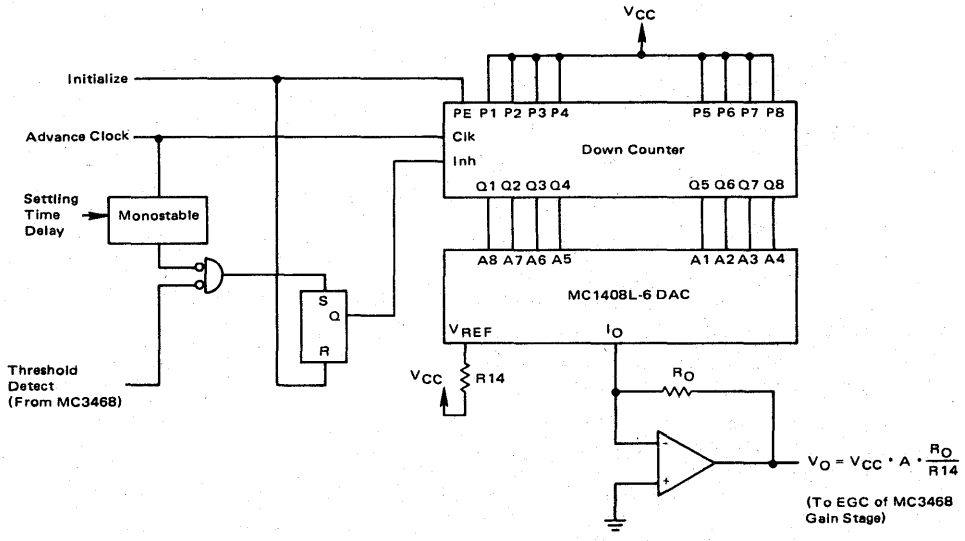


FIGURE 34 – APPLICATIONS CIRCUITS

Digital Attenuator for Setting MC3468 Gain Stage Automatically During ID Burst



5

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\ (Typ)}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst-case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient

XC3480

Product Preview

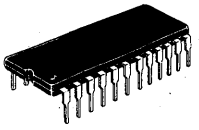
16 PIN 4K DYNAMIC MEMORY CONTROLLER

The memory controller chip is designed to greatly simplify the interface logic required to control the popular 16 pin 4K dynamic NMOS RAM in a microprocessor system such as the MC6800. The controller will generate, on command from the microprocessor, the proper timing signals required to successfully transfer data to the microprocessor from the NMOS memories. The controller, in conjunction with a 32 kHz oscillator, will also generate the necessary signals required to insure that the dynamic memories are refreshed for the retention of data.

- Greatly simplify the MPU – dynamic memory interface.
- Reduce package count.
- CHIP ENABLE for expansion to larger WORD CAPACITY.
- Generate 1 of 4 $\overline{RAS}$ signals for an optimum 16K memory system.
- High input impedance for minimum loading of MPU bus.
- Schottky TTL technology for high performance.
- Upward compatible with future 16K X 1 bit memories.

MEMORY CONTROLLER CIRCUIT

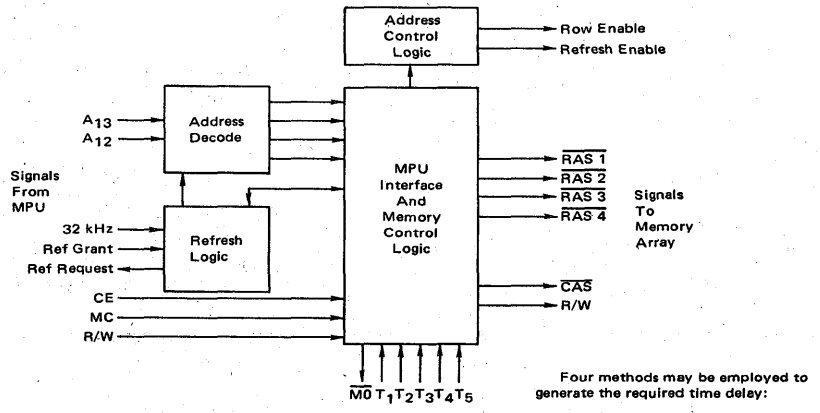
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 649

5

BLOCK DIAGRAM



Four methods may be employed to generate the required time delay:

1) One shots
2) High frequency counters
3) High frequency shift registers
4) Delay lines

This is advance information and specifications are subject to change without notice.

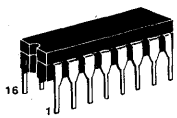
MC3486

QUAD RS-422/423 LINE RECEIVER

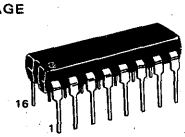
Motorola's Quad RS-422/3 Receiver features four independent receiver chains which comply with EIA Standards for the Electrical Characteristics of Balanced/Unbalanced Voltage Digital Interface Circuits. Receiver outputs are 74LS compatible, three-state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms. A summary of MC3486 features include:

- Four Independent Receiver Chains
- Three-State Outputs
- High Impedance Output Control Inputs (PIA Compatible)
- Internal Hysteresis – 100 mV (Typ)
- Fast Propagation Times – 25 ns (Typ)
- TTL Compatible
- Single 5 V Supply Voltage

QUAD RS-422/3 LINE RECEIVER WITH THREE-STATE OUTPUTS



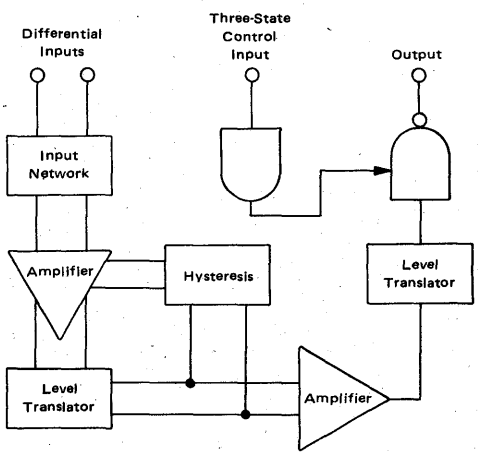
L SUFFIX
CERAMIC PACKAGE
CASE 620



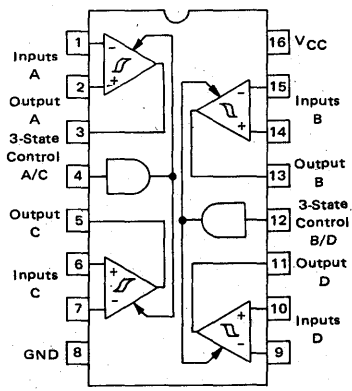
P SUFFIX
PLASTIC PACKAGE
CASE 648

5

RECEIVER CHAIN BLOCK DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION		
DEVICE	TEMPERATURE RANGE	PACKAGE
MC3486L	0 to +70°C	Ceramic DIP
MC3486P	0 to +70°C	Plastic DIP

ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Common Mode Voltage	V_{ICM}	±15	Vdc
Input Differential Voltage	V_{ID}	±15	Vdc
Three-State Control Input Voltage	V_I	8.0	Vdc
Output Sink Current	I_O	50	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Input Common Mode Voltage Range	V_{ICR}	-7.0 to +7.0	Vdc
Input Differential Voltage Range	V_{IDR}	6.0	Vdc

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for $T_A = 25°C$, $V_{CC} = 5.0$ V and $V_{IC} = 0$ V. See Note 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State (Three-State Control)	V_{IH}	2.0	–	–	V
Input Voltage — Low Logic State (Three-State Control)	V_{IL}	–	–	0.8	V
Differential Input Threshold Voltage ($-7.0\ V \leq V_{IC} \leq 7.0\ V$, $V_{IH(3C)} = 2.0$ V) ($I_O = 0.4$ mA, $V_{OH} \geq 2.7$ V) ($I_O = 8.0$ mA, $V_{OL} \geq 0.5$ V)	$V_{TH(D)}$	 – –	 0.05 -0.05	 0.2 -0.2	V
Input Bias Current ($V_{CC} = 0$ V or 5.25) (Other Inputs at 0 V) ($V_I = -10$ V) ($V_I = -3.0$ V) ($V_I = +3.0$ V) ($V_I = +10$ V)	$I_{IB(D)}$	 – – – –	 – – – –	 -3.25 -1.50 +1.50 +3.25	mA
Input Balance ($-7.0\ V \leq V_{IC} \leq 7.0\ V$, $V_{IH(3C)} = 2.0$ V, See Note 3) ($I_O = 0.4$ mA, $V_{ID} = 0.4$ V) ($I_O = 8.0$ mA, $V_{ID} = 0.4$ V)		 2.7 –	 – –	 – 0.5	V
Output Third State Leakage Current ($V_{I(D)} = +3.0$ V, $V_{IL(3C)} = 0.8$ V, $V_{OL} = 0.5$ V) ($V_{I(D)} = -3.0$ V, $V_{IL(3C)} = 0.8$ V, $V_{OH} = 2.7$ V)	I_{OZ}	 – –	 – –	 -40 40	μA
Output Short-Circuit Current ($V_{I(D)} = 3.0$ V, $V_{IH(3C)} = 2.0$ V, $V_O = 0$ V, See Note 2)	I_{OS}	-15	–	-100	mA
Input Current — Low Logic State (Three-State Control) ($V_{IH(3S)} = 0.5$ V)	I_{IL}	–	–	-100	μA
Input Current — High Logic State (Three-State Control) ($V_{IH(3S)} = 2.7$ V) ($V_{IH(3S)} = 5.25$ V)	I_{IH}	 – –	 – –	 20 100	μA
Input Clamp Diode Voltage (Three-State Control) ($I_{C(3S)} = -10$ mA)	V_{IC}	–	–	-1.5	V
Power Supply Current ($V_{IL(3S)} = 0$ V)	I_{CC}	–	–	80	mA

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Differential Inputs to Output					ns
(Output High to Low)	$t_{PHL(D)}$	–	20	–	
(Output Low to High)	$t_{PLH(D)}$	–	25	–	
Propagation Delay time — Three-State Control to Output					ns
(Output Low to Third State)	t_{PLZ}	–	23	–	
(Output High to Third State)	t_{PHZ}	–	25	–	
(Output Third State to High)	t_{PZH}	–	18	–	
(Output Third State to Low)	t_{PZL}	–	20	–	

NOTES:
1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Only one output at a time should be shorted.
3. Refer to EIA RS-422/3 for exact conditions.

FIGURE 1 — SWITCHING TEST CIRCUIT AND WAVEFORMS

Propagation Delay Differential Input to Output

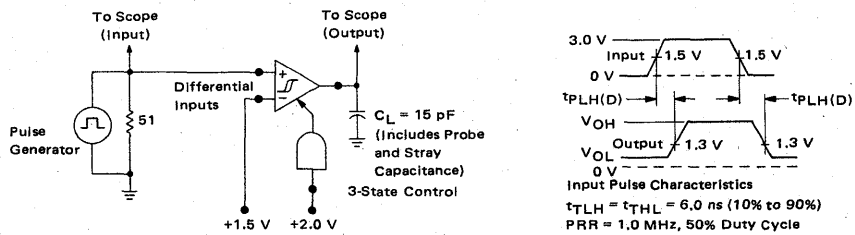
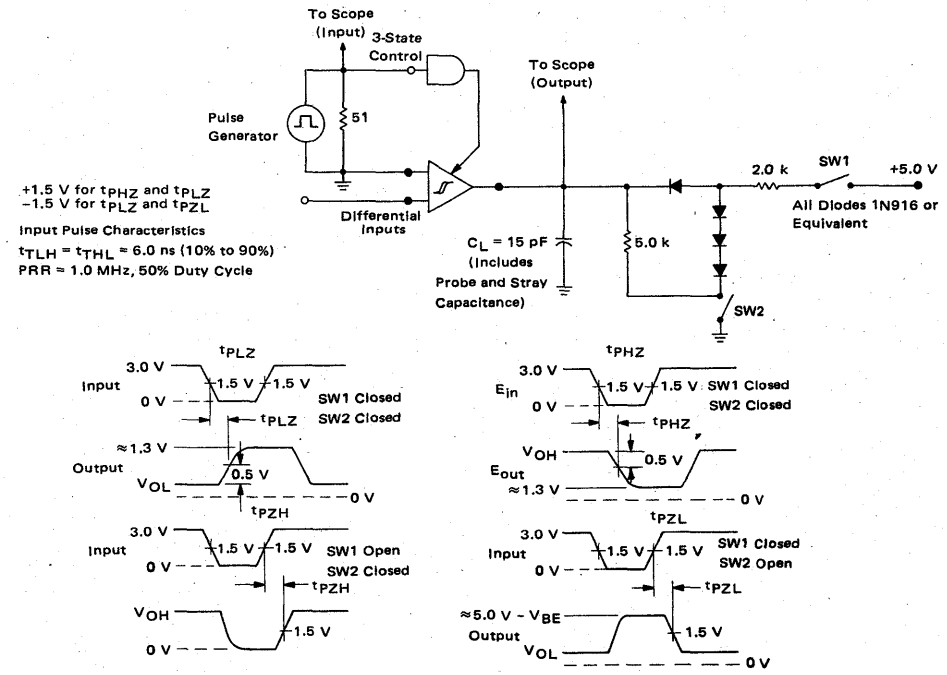


FIGURE 2 — PROPAGATION DELAY THREE-STATE CONTROL INPUT TO OUTPUT



XC3487

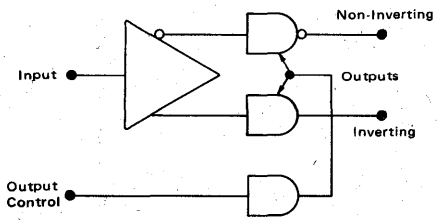
Product Preview

QUAD LINE DRIVER WITH THREE-STATE OUTPUTS

Motorola's Quad RS-422 Driver features four independent driver chains which comply with EIA Standards for the Electrical Characteristics of Balanced Voltage Digital Interface Circuits. The outputs are three-state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down. A summary of MC3487 features include:

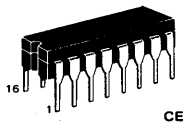
- Four Independent Driver Chains
- Three-State Outputs
- PNP High Impedance Inputs (PIA Compatible)
- Power Up/Down Protection
- Fast Propagation Times (Typ 15 ns)
- TTL Compatible
- Single 5 V Supply Voltage
- Output Rise and Fall Times Less Than 20 ns
- Equivalent to DS 3487

DRIVER BLOCK DIAGRAM

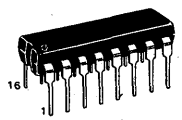


QUAD RS-422 LINE DRIVER WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC INTEGRATED CIRCUIT

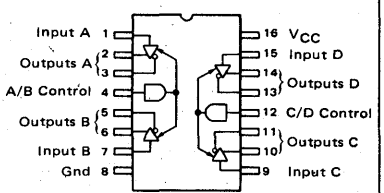


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



TRUTH TABLE

Input	Control Input	Non-Inverter Output	Inverter Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

This is advance information and specifications are subject to change without notice.

*ABSOLUTE MAXIMUM RATINGS			
Rating	**Symbol**	**Value**	**Unit**
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range Ceramic Package Plastic Package	T_J	 175 150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

*"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Table of Electrical Characteristics" provides conditions for actual device operation.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply 4.75 V ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 70°C. Typical values measured at V_{CC} = 5.0 V, and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State	V_{IL}	–	–	0.8	Vdc
Input Voltage — High Logic State	V_{IH}	2.0	–	–	Vdc
Input Current — Low Logic State (V_{IL} = 0.5 V)	I_{IL}	–	–	-200	μA
Input Current — High Logic State (V_{IH} = 2.4 V) (V_{IH} = 5.5 V)	I_{IH}	 – –	 – –	 -50 -50	μA
Input Clamp Voltage (I_{IC} = -12 mA)	V_{IC}	–	–	-1.5	V
Output Voltage — Low Logic State (I_{OL} = 48 mA)	V_{OL}	–	–	0.5	V
Output Voltage — High Logic State (I_{OH} = -10 mA) (I_{OH} = -50 mA)	V_{OH}	2.5 2.0	–	–	V
Output Short-Circuit Current (V_{IH} = 2.0 V) [2]	I_{OS}	-50	–	-150	mA
Output Leakage Current — Hi-Z State V_{IL} = 0.4 V, $V_{IL(Z)}$ = 0.8 V) V_{IH} = 2.4 V, $V_{IL(Z)}$ = 0.8 V)	$I_{OL(Z)}$	 – –	 – –	 ±100 ±100	μA
Output Leakage Current — Power OFF (V_{OH} = 6.0 V, V_{CC} = 0 V) (V_{OL} = -0.25 V, V_{CC} = 0 V)	$I_{OL(off)}$	 – –	 – –	 +100 -100	μA
Output Offset Voltage 1	V_{OS}	–	–	±0.4	V
Output Differential Voltage 1	V_T	2.0	–	–	V
Output Differential Voltage Difference 1	$V_T - \overline{V}_T$	–	–	±0.4	V
Power Supply Current	I_{CC}	–	–	95	mA

1. See EIA Specification RS-422 for exact test conditions.
2. Only one putput may be shorted at a time.

5

ORDERING INFORMATION

Device	Temperature Range	Package
MC3490P	0°C to +70°C	Plastic DIP
MC3494P	0°C to +70°C	Plastic DIP

MC3490 MC3494

ANODE (DIGIT) DRIVERS FOR GAS-DISCHARGE DISPLAYS

SILICON MONOLITHIC INTEGRATED CIRCUIT

SEVEN-DIGIT GAS-DISCHARGE DISPLAY DRIVERS

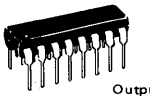
Seven channel digit (anode) drivers, the MC3490 and MC3494 are specifically conceived to be used with high-voltage, gas-discharge numeric displays such as the Burroughs' Panaplex®, Beckman (Sperry) Cherry, or Diacon displays.

The MC3490 version is configured such that a high logic level input causes the driver to turn on while the MC3494 requires a low logic level to turn the drivers on. Both devices are designed to mate with the MC3491 cathode (segment) driver.

With a low input current requirement of only 300 μA typically, these devices are compatible with popular MOS chips.

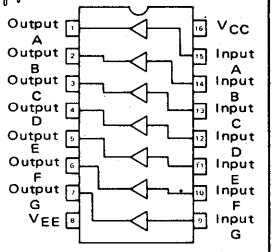
Minimum breakdown voltage is specified at 48 V and output drive current capability is typically 30 mA per channel.

- High Breakdown Voltage – 55 V Typical
- Low Input Current for MOS Compatibility
- Available with Either Active High or Active Low Inputs
- Operable from Either Positive or Negative Supply Voltages
- Input Clamp Diodes on MC3494 Version for DC Restoration
- Internal Pull-down Resistors

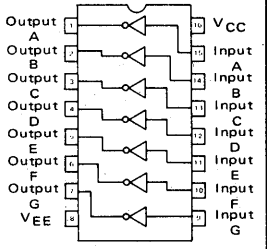


P SUFFIX
PLASTIC
PACKAGE
CASE 648

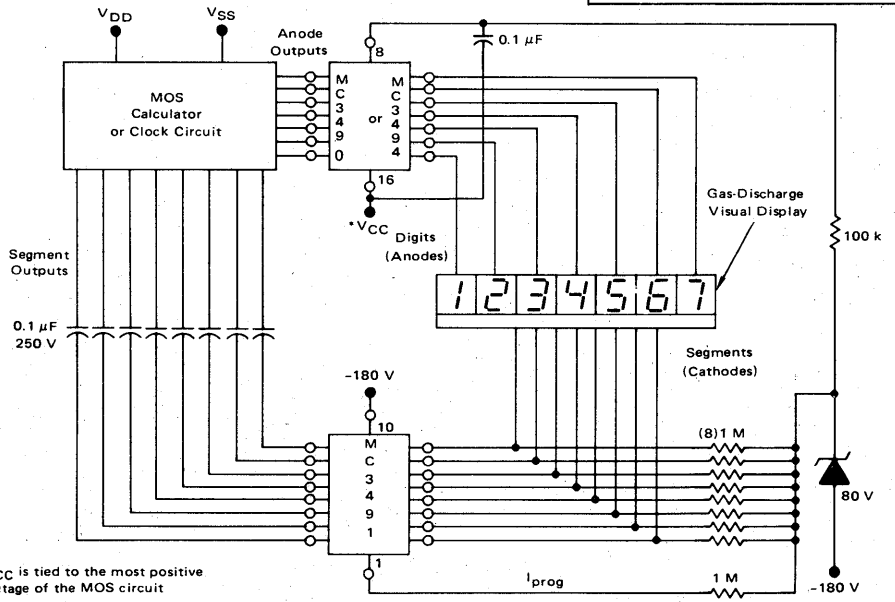
PIN CONNECTIONS
MC3490



MC3494



TYPICAL APPLICATION
WITH CAPACITIVE LEVEL SHIFT TO CATHODE DRIVER



*VCC is tied to the most positive voltage of the MOS circuit

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MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Negative Supply Voltage (Current Limited to -5 mA)	V_{EE}	-60	Vdc
Negative Supply Current	I_{EE}	-5.0	mAdc
Input Voltage	V_I	V_{CC}-20, V_{CC}	Vdc
Output Current (V_O = -5 V)	I_O	-50	mAdc
Package Power Dissipation Derate above 25°C	P_D	830 6.7	mW mW/°C
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = Gnd V_{EE} = -50 V, unless otherwise noted.)

Characteristic	Symbol	MC3490			MC3494			Unit
		Min	Typ	Max	Min	Typ	Max	
Substrate Breakdown Voltage Pin 16, V_{CC} = Gnd Pin 8 connected to -60 V thru 5 kΩ	$V_{S(BR)}$	-48	-55	–	-48	-55	–	Vdc
Input Current – On State V_I = 0.0 V (See Figure 4) V_I = -7.0 V (See Figure 3)	$I_{I(on)}$	– –	250 –	450 –	– –	– -200	– -350	μA
Input Current – Off State V_I = -15 V V_I = 0.0 V	$I_{I(off)}$	– –	<-1.0 –	-45 –	– –	– <1.0	– 45	μA
Input Voltage – Off State V_O = V_{EE} (See Figures 3 and 4)	$V_{I(off)}$	-5.0	–	–	–	–	-2.0	Vdc
Input Voltage – On State V_O = V_{CC}-5.0 V (See Figures 3 and 4)	$V_{I(on)}$	–	–	-2.0	-5.0	–	–	Vdc
Output Voltage – Off State V_I = 0.0 V V_I = -7.0 V	$V_{O(off)}$	– V_{EE} + 5.0	– V_{EE}	– –	V_{EE} + 5.0 –	V_{EE} –	– –	Vdc
Output Voltage – On State I_O = -20 mA, V_I = 0.0 V I_O = -20 mA, V_I = -7.0 V	$V_{O(on)}$	-3.5 –	-2.5 –	– –	– -5.0	– -3.5	– –	Vdc

5

SYSTEM DISCUSSION

The MC3491 and MC3490/MC3494 high voltage driver system is designed such that it can be floated and any point in the system may be tied to circuit ground. In a MOS system, normally either the ground pin on the MC3491 is tied to the most negative MOS voltage; or the V_{CC} pin on the MC3490/MC3494 is connected to the most positive MOS voltage. In the electrical characteristics table, this V_{CC} voltage is assumed to be 0.0 volts.

The MC3490/MC3494 provides its own internal voltage reference when a current (-100 μA to -5 mA) is drawn at the V_{EE} pin (Pin 8). This can be provided by connecting a resistor from Pin 8 to the high voltage reference on the cathode driver or any other voltage more negative than V_{CC} -60 V. This voltage (Pin 8) is approximately -55 V and provides a reference for the pull-down function for each channel.

5

TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 1 – SUBSTRATE CURRENT versus SUBSTRATE VOLTAGE

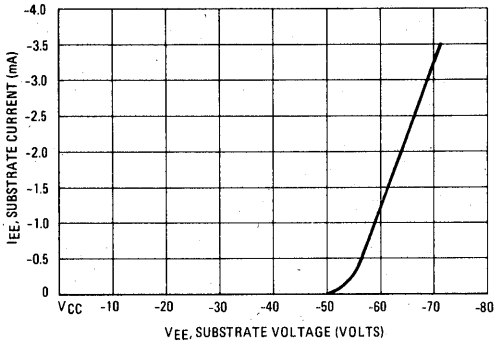


FIGURE 2 – PERMISSIBLE OPERATING RANGE

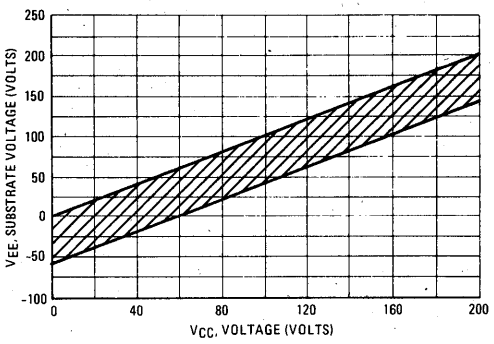


FIGURE 3 – OUTPUT VOLTAGE and INPUT CURRENT versus INPUT VOLTAGE

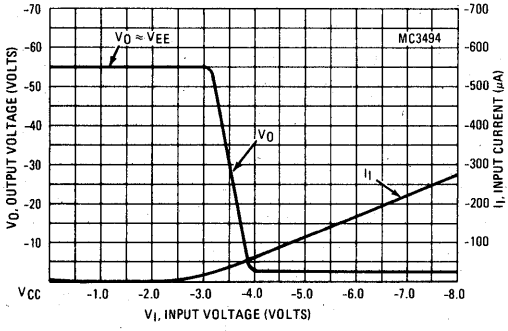
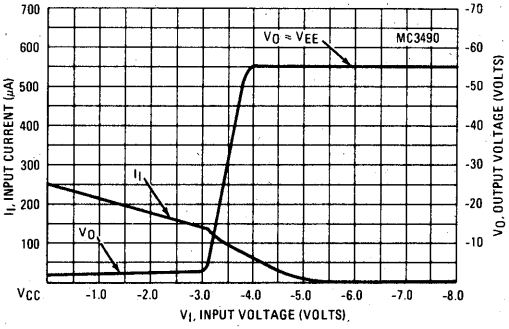
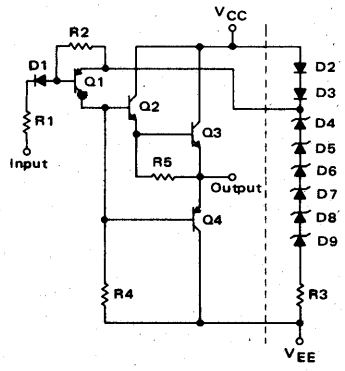


FIGURE 4 – INPUT CURRENT and OUTPUT VOLTAGE versus INPUT VOLTAGE

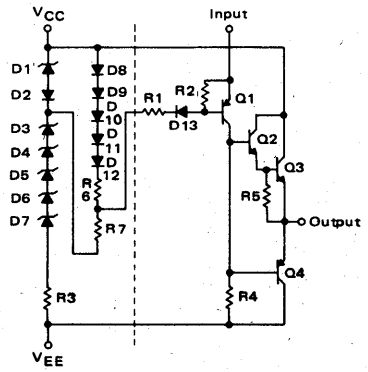


REPRESENTATIVE CIRCUIT SCHEMATIC (1/7 Shown)

MC3494



MC3490



12-DIGIT McMOS GAS DISCHARGE DISPLAY

When the number of digits for a gas discharge display system is greater than the number of segment drivers, it is generally more economical to level translate down to the cathode segments than to translate up to the digit anodes. An example of this technique is shown in the 12 digit display system where the display anodes and cathodes are referenced to ground and -180 V respectively.

The positive logic CMOS address circuits are powered by -10 V (V_{DD} = 0, V_{SS} = -10 V) with the MC14558 decoder outputs capacitor-coupled to the MC3491 Segment Drivers and the scan circuit directly-coupled to the MC3490 Anode Drivers. Thus, only eight capacitors (seven segments, one decimal point) are required as compared to 12 capacitors, if the strobed digit drivers were ac coupled.

The MC3491 has input clamp diodes allowing for dc restoration of the segment address pulse. This high voltage driver (80 V) also features programmable segment current by the selection of a single external resistor.

The MC3490 Anode Drivers are selected by the positive going output of the digit scan circuit. (If the scan circuit outputs were negative going, the low logic level input MC3494 Anode Driver should be used.) The internal zener diode string of the MC3490 references the off drivers (and display anodes) to -50 V without the need of pull-down resistors.

Digit scanning for this example is derived from two cascaded MC14022 Octal Counter/Drivers. The 12 sequenced output pulses are achieved by resetting the counters with the second counter Q7 output. In addition to driving the two MC3490s, the counter output should also control the system multiplexer (not shown) to properly synchronize the entire display system.

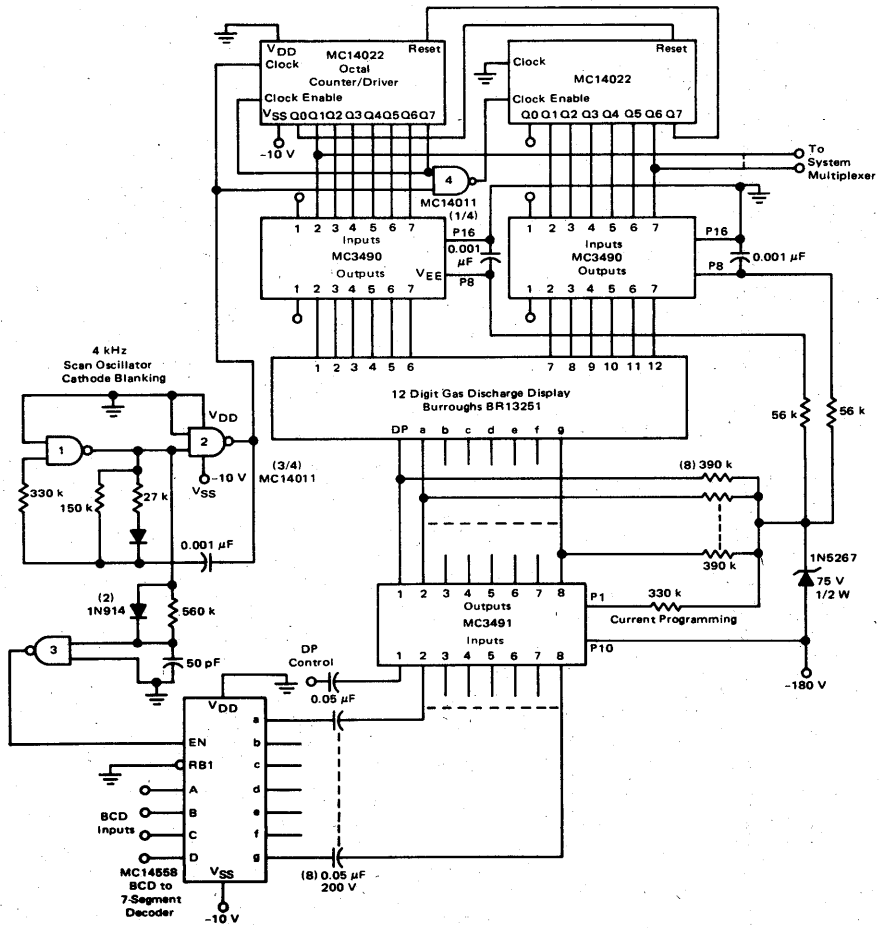
The MC14558 BCD-to-Seven Segment Decoder has an Enable input which readily provides for display cathode blanking. For the illustrated display, the cathode drivers should be turned off prior to anode switching and maintained off for some period after the next anode is strobed.

This cathode blanking overlap is derived by trailing edge time delaying the Gate 1 output of the non-symmetric 4 kHz scan oscillator with the integrated network and inverter Gate 3.

The high voltage power supply rise and fall times should be greater than the charge time of the coupling capacitors to prevent large transients from possible degrading the interface electronics.

For this example, power supply rise and fall time of 50 ms minimum will suffice.

FIGURE 5 – 12-DIGIT McMOS GAS DISCHARGE DISPLAY SYSTEM



3-1/2 DIGIT VOLTMETER

This specific application provides a 3-1/2 digit DVM utilizing the MC1505 dual ramp subsystem and CMOS MC14435 digital subsystem. Interfacing between low voltage logic ICs and the higher voltage gas discharge displays requires level translation or shifting. The method described for the 3-1/2 Digit DVM uses directly coupled high voltage (200 V) transistors to translate upward to the **MC3494 Anode Drivers.** Three of the transistors comprising the MPQ7042 high voltage quad transistor are used for this function. These transistors, connected in a common-base, constant-current configuration, are turned on by the negative going digit select output pulses of the MC14435. The current of approximately 330 μA is compatible with 200 μA typical input current of the MC3494 and the sink current capability of the MC14435.

The CMOS MC14558 BCD-to-Seven Segment Decoder has the capability of directly driving the MC3491 Segment Driver. Cathode blanking is accomplished by taking the clock signal from Pin 4 of the MC14435 (approximately 50% duty cycle) and tying it to the Enable input of the MC14458. The display segment current is increased accordingly to 1.1 mA (manufacturers maximum specified current equals 1.25 mA) for this relatively large cathode blanking period.

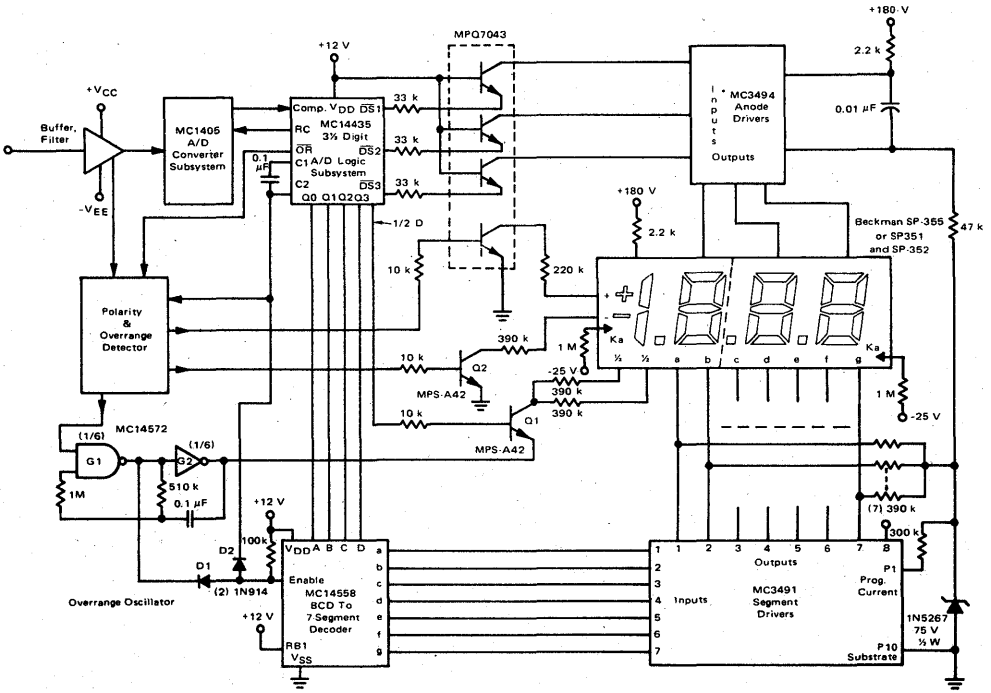
The positive and negative polarity signs are direct driven by the fourth transistor of the MPQ7043 and MPS-A42 transistor, Q2, respectively. Their dc segment currents are scaled to produce the same brightness as the multiplexed digits.

The 1/2 digit segments are driven by transistor Q1. Its emitter is normally referenced to ground through MC14572 Inverter G2, the output inverter of the Overrange Oscillator.

When an overrange situation occurs, the oscillator is enabled, thus causing the display to flash at the oscillator rate (approximately 8 Hz). This is accomplished by blanking the 1/2 digit through Q1 and the multiplexed digits through diode D1 to the decoder enable input.

See the MC1405 and MC14435 data sheets for more details of DVM system.

FIGURE 6 – 3-½ DIGIT DIGITAL VOLTMETER



12-HOUR CLOCK WITH GAS DISCHARGE DISPLAYS

The MC3491 cathode driver and MC3494 anode driver, greatly simplify the interfacing of a clock chip (MOSTEK MK50250) to a gas discharge clock display (Burroughs CD60733-CM).

The MK50250 has a 6 digit clock display with multiplexed 7 segment outputs. The MC3491 cathode drivers switch each display cathode between ground (on condition) and +75 Volts (off condition) with current limiting for the display provided via the current programming pin on the MC3491. The +75 Volt reference is obtained from a 75-Volt zener diode, Z1, R1, and a 50-Volt zener diode internal to the MC3494 anode driver.

The programming current is reduced during the time when the "two seconds" indicator digits are ON, to reduce the current through these smaller digits of the display. Four diodes attached to each of the "hours" and "minutes" digits, provide a voltage of +180 Volts across the 680 kΩ resistor. During the "seconds" digits display time, the voltage is reduced to +130 Volts, thus reducing the programming current.

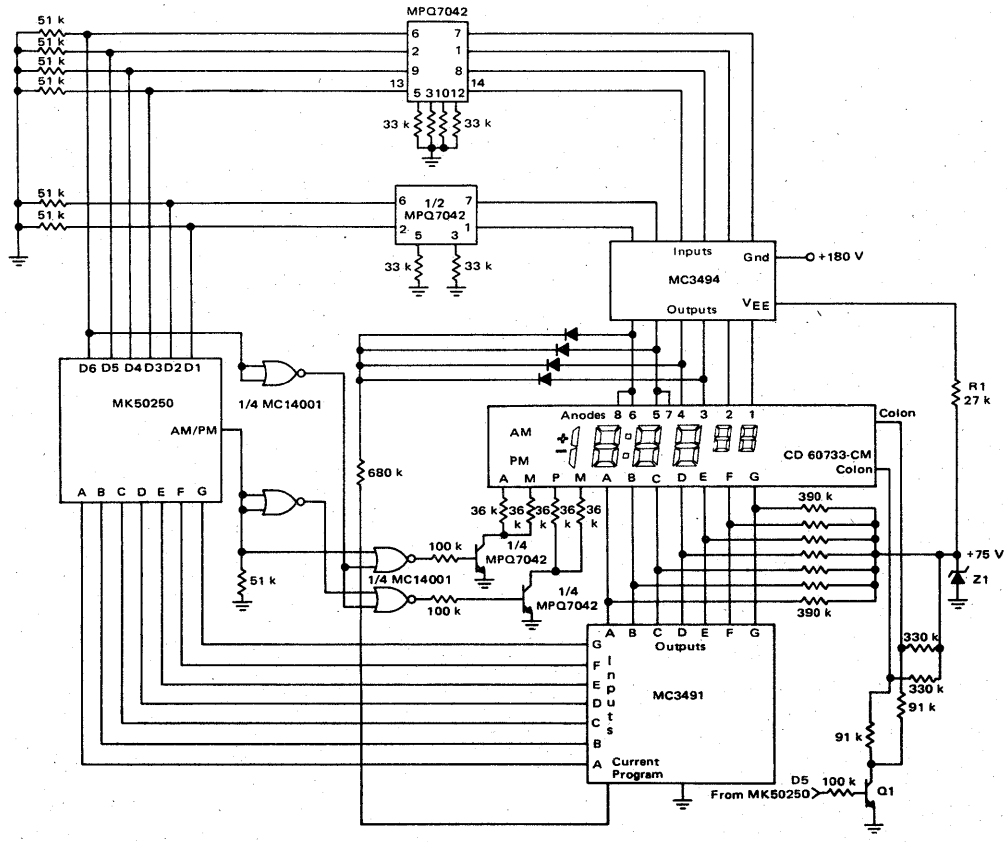
The anodes for each of the six digits are switched between the +180 Volt positive supply and +130 Volts via the MC3494 anode drivers. Inter-digit blanking is provided in the anode circuits. Level translation from the clock chip output to the input to the MC3494 uses two MPQ7042 quad high voltage transistor packages operating in an emitter follower current source mode. Each current source turns on one of the MC3494 drivers by sinking 300 μA to ground for the proper "on" digit.

The AM/PM clock output is in the high state when PM is indicated and has a 85% duty cycle corresponding to each anode on time. A MC14001 Quad NOR Gate decodes this output to turn on the appropriate AM or PM indicator during the D6 digit. These Gates control the AM/PM display indicators with the remaining MPQ7042 high voltage transistors which were not used in anode selection.

The colon separating hours and minutes is switched on during the units of hours digit on time. The colon cathodes are switched from +75 Volts to ground via T1 during the D5 digit time while the anodes are switched between +180 and +130 Volts.

Further information concerning operation or technical specifications on the MOSTEK clock chip, MK50250, and the Burroughs clock display, CD60733-CM is obtainable from the manufacturers.

FIGURE 7 – 12 HOUR CLOCK WITH GAS DISCHARGE DISPLAY SYSTEM



MC3491
MC3492

EIGHT-SEGMENT VISUAL DISPLAY DRIVERS

The MC3491 and MC3492 are eight-segment cathode drivers for use with gas-discharge displays, such as the Burroughs' Panaplex®, Beckman, Cherry or Diacon types. Both devices are directly compatible with MOS logic outputs due to their low 300 μA input current requirement.

All eight driver output currents are simultaneously programmable by selection of a single external resistor. As programmed, all eight currents match to within typically 1% of each other.

Both devices provide dc restoration. The units are specified for a minimum breakdown voltage of 80 V.

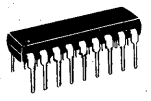
The MC3492 device is made for larger and higher intensity displays requiring higher segment current.

- High Breakdown Voltage – 80 V Min*
- Drives Seven Cathode Segments plus Decimal Point
- All Currents Simultaneously Programmable with One Resistor
- MC3491 is Pin-for-Pin and Functionally Equivalent to DM8889
- Output Current/Programming Current Ratio –
  Typically 4.5:1 for MC3491
  9:1 for MC3492
- Companion with MC3490 and MC3494 Anode Drivers
- MC3492 Provides Increased Output Current for High Intensity Displays

*Higher Voltage Selection Available

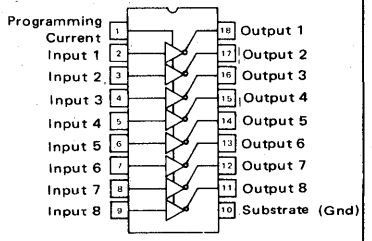
SEGMENT DRIVERS FOR GAS-DISCHARGE DISPLAYS

SILICON MONOLITHIC INTEGRATED CIRCUIT



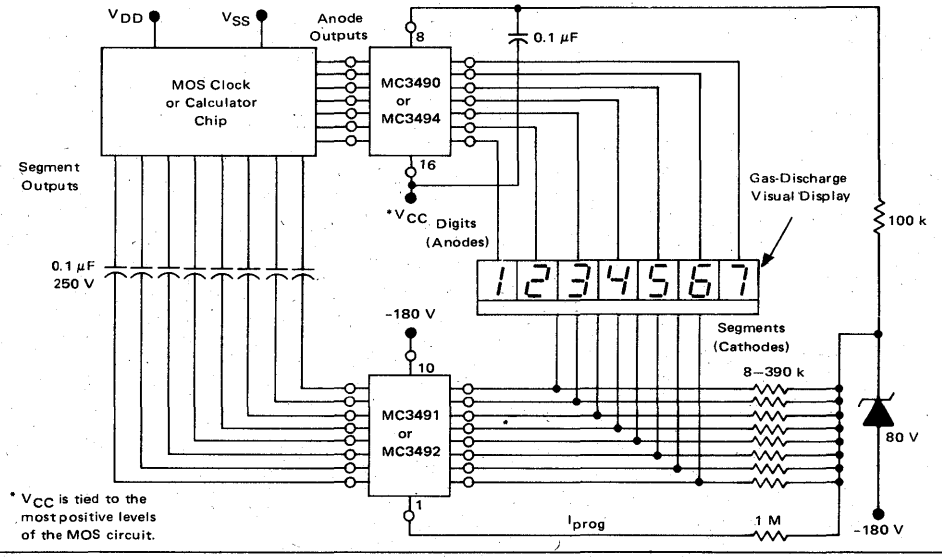
P SUFFIX
PLASTIC PACKAGE
CASE 701

PIN CONNECTIONS



ORDERING INFORMATION		
DEVICE	TEMPERATURE RANGE	PACKAGE
MC3491P	0 to +70°C	Plastic DIP
MC3492P	0 to +70°C	Plastic DIP

FIGURE 1 – TYPICAL CALCULATOR APPLICATION WITH CAPACITIVE LEVEL SHIFT AND ANODE DRIVER



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MAXIMUM RATINGS (Unless otherwise noted, $T_A = 25^oC$)

Rating	Symbol	Value	Unit
Output OFF Voltage (Current Limited to 0.5 mA)	$V_{O(off)}$	95	V
Output ON Voltage (Current Limtied to 2.0 mA)	$V_{O(on)}$	50	V
Input Voltage	V_I	20	V
Programming Current MC3491 MC3492	I_{prog}	 400 2500	μA
Junction Temperature	T_J	150	^oC
Operating Ambient Temperature Range	T_A	0 to 70	^oC
Storage Temperature Range	T_{stg}	-65 to +150	^oC

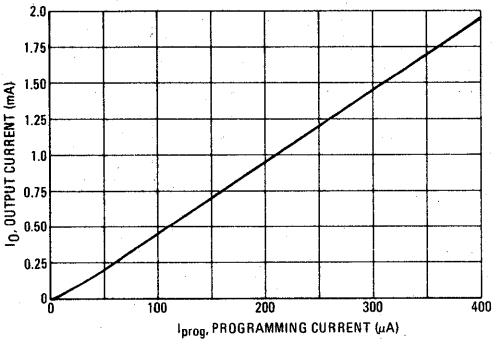
ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $V_{CC} \leq 80$ V, $T_A = 25^oC$, Pin 10 = Gnd. All voltages with respect to Gnd.)

Characteristic	Symbol	MC3491			MC3492			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Current (V_{IH} = 7.0 V)	I_{IH}	200	300	400	200	300	400	μA
Input Clamp Voltage (I_{IC} = -1.0 mA)	V_{IC}	–	–	-1.0	–	–	-1.0	V
Input OFF Voltage	V_{IL}	1.0	1.5	–	1.0	1.5	–	V
Input ON Voltage	V_{IH}	–	2.4	3.5	–	2.4	3.5	V
Output OFF Current (V_{IL} = 0 V, $V_O = V_{CC}$)	$I_{O(off)}$	–	–	5.0	–	–	5.0	μA
Output ON Current	$I_{O(on)}$							μA
(I_{prog} = 100 μA)		400	450	500	–	–	–	
(I_{prog} = 350 μA)		1450	1650	1850	–	–	–	
(I_{prog} = 300 μA)		–	–	–	1.3	1.6	1.9	mA
(I_{prog} = 500 μA)		–	–	–	3.75	4.5	5.25	
Output Current Matching (All eight outputs)	ΔI_O	–	≤ 1	≤ 10	–	≤ 1	≤ 10	%
Output OFF Voltage	$V_{O(off)}$							V
(I_{prog} = 100 μA, R_L = 1.0 MΩ, V_{IL} = 0 V)		V_{CC}-5.0	V_{CC}	–	–	–	–	
(I_{prog} = 300 μA, R_L = 1.0 MΩ, V_{IL} = 0 V)		–	–	–	V_{CC}-5.0	V_{CC}	–	
Output ON Voltage (I_{prog} = 100 μA, R_L = 1.0 MΩ, V_{IH} = 7.0 V)	$V_{O(on)}$	–	3.0	5.0	–	–	–	V
Output Saturation Voltage (I_{prog} = 300 μA, R_L = 1.0 MΩ, V_{IH} = 7.0 V)	$V_{O(sat)}$	–	–	–	–	3.0	5.0	V
Output Voltage Compliance Range	$V_{OR(on)}$							V
(I_{prog} = 100 μA, $I_{O(on)}$ = 450 μA, V_{IH} = 7.0 V) (See Figure 3)		5.0	–	50	–	–	–	
(I_{prog} = 300 μA, $I_{O(on)}$ = 2.8 mA, V_{IH} = 7.0 V) (See Figure 3)		–	–	–	5.0	–	50	

TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 2 – OUTPUT CURRENT versus PROGRAMMING CURRENT (T_A = 25°C)

MC3491



MC3492

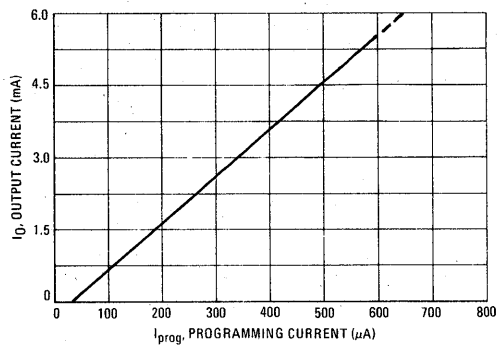
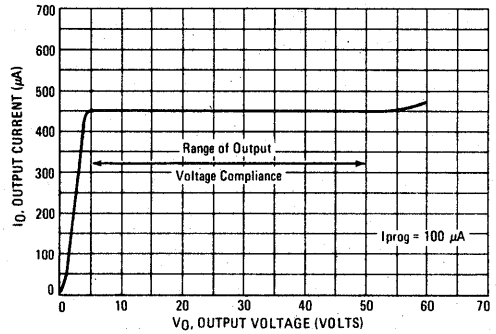


FIGURE 3 – OUTPUT CURRENT versus OUTPUT VOLTAGE (V_{IH} = 7.0 V, T_A = 25°C)

MC3491



MC3492

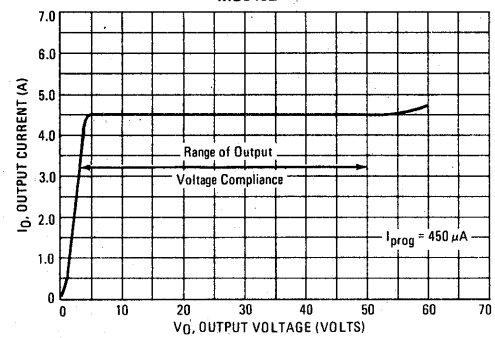
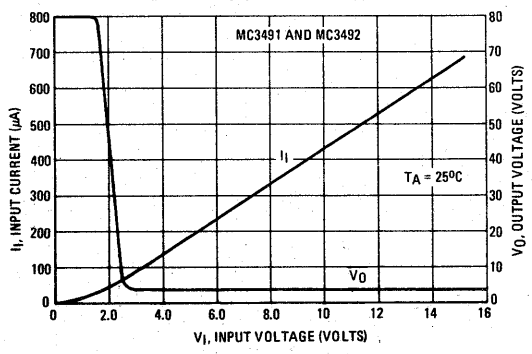


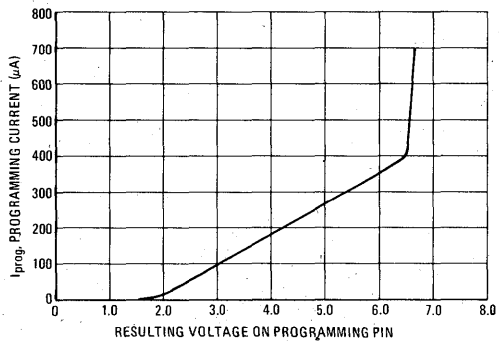
FIGURE 4 – TYPICAL INPUT CURRENT AND OUTPUT VOLTAGE versus INPUT VOLTAGE



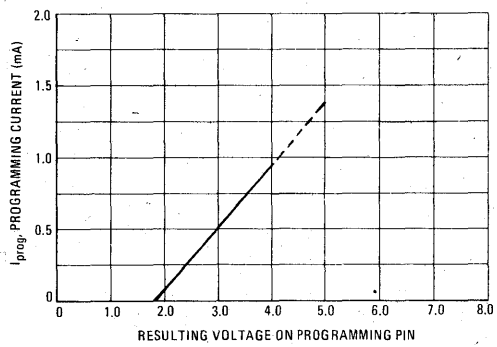
TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 5 – TYPICAL PROGRAMMING CURRENT versus VOLTAGE ON PROGRAMMING PIN (T_A = 25°C)

MC3491



MC3492



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

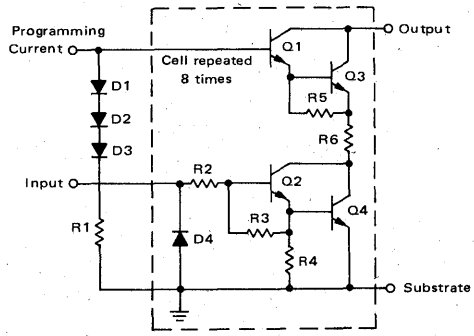
Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

REPRESENTATIVE CIRCUIT SCHEMATIC



12-DIGIT McMOS GAS DISCHARGE DISPLAY

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The MC3490P Anode Drivers are selected by the positive going output of the digit scan circuit. (If the scan circuit outputs were negative going, the low logic level input MC3494P Anode Driver should be used.) The internal zener diode string of the MC3490P references the off drivers (and display anodes) to -50 V without the need of pull-down resistors.

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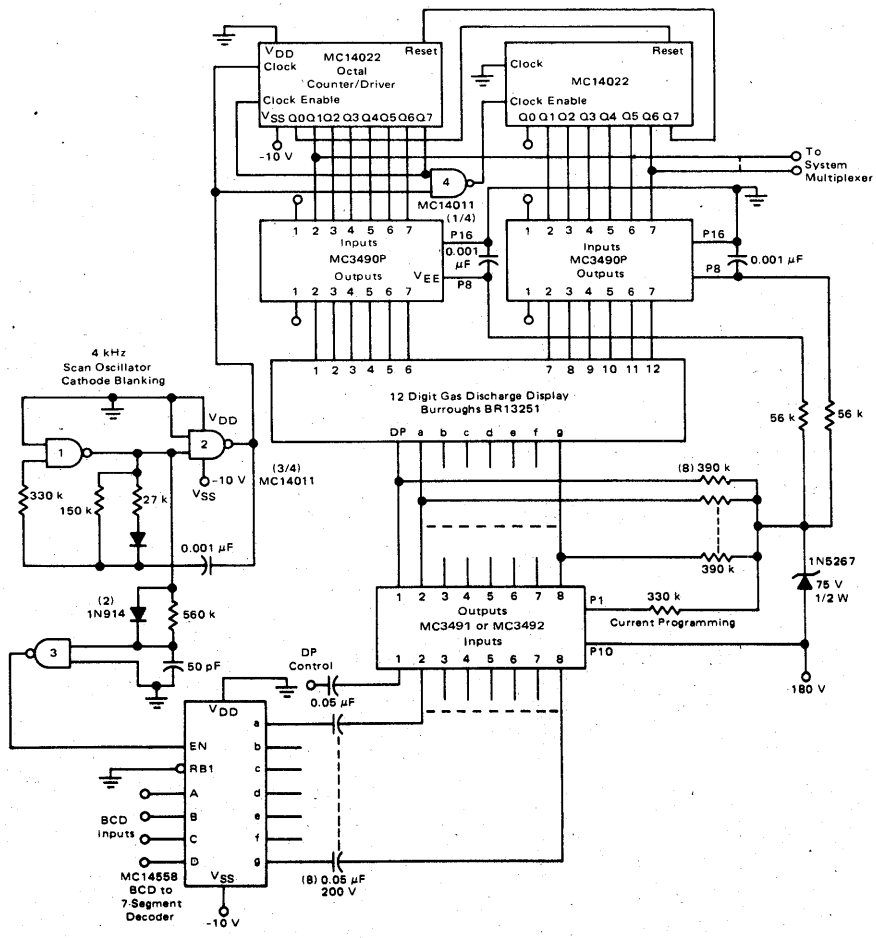
The high voltage power supply rise and fall times should be greater than the charge time of the coupling capacitors to prevent large transients from possible degrading the interface electronics.

For this example, power supply rise and fall time of 50 ms minimum will suffice.

FIGURE 6 – 12-DIGIT McMOS GAS DISCHARGE DISPLAY SYSTEM



3-1/2 DIGIT VOLTMETER

This specific application provides a 3-1/2 digit DVM utilizing the MC1505 dual ramp subsystem and CMOS MC14435 digital subsystem. Interfacing between low voltage logic ICs and the higher voltage gas discharge displays requires level translation or shifting. The method described for the 3-1/2 Digit DVM uses directly coupled high voltage (200 V) transistors to translate upward to the MC3494 Anode Drivers[1]. Three of the transistors comprising the MPQ7042 high voltage quad transistor are used for this function. These transistors, connected in a common-base, constant-current configuration, are turned on by the negative going digit select output pulses of the MC14435. The current of approximately 330 μA is compatible with 200 μA typical input current of the MC3494 and the sink current capability of the MC14435.

The CMOS MC14558 BCD-to-Seven Segment Decoder has the capability of directly driving the MC3491 or MC3492 Segment Drivers. Cathode blanking is accomplished by taking the clock signal from Pin 4 of the MC14435 (approximately 50% duty cycle) and tying it to the Enable input of the MC14458. The display segment current is increased accordingly to 1.1 mA (manufacturers maximum specified current equals 1.25 mA) for this relatively large cathode blanking period.

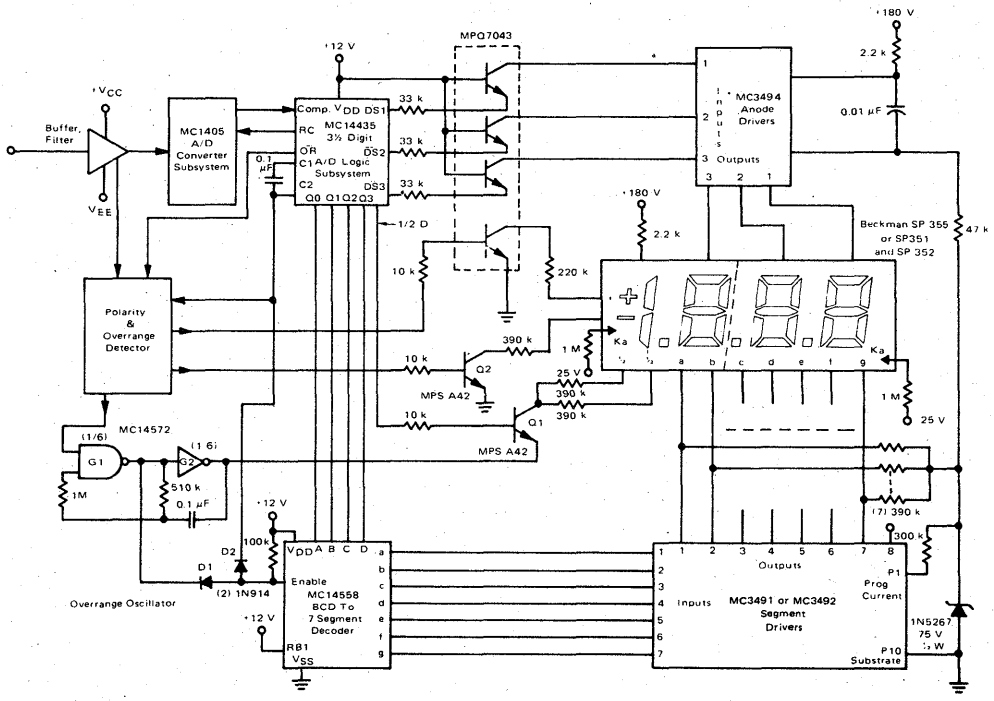
The positive and negative polarity signs are direct driven by the fourth transistor of the MPQ7043 and MPS-A42 transistor, Q2, respectively. Their dc segment currents are scaled to produce the same brightness as the multiplexed digits.

The 1/2 digit segments are driven by transistor Q1. Its emitter is normally referenced to ground through MC14572 Inverter G2, the output inverter of the Overrange Oscillator.

When an overrange situation occurs, the oscillator is enabled, thus causing the display to flash at the oscillator rate (approximately 8 Hz). This is accomplished by blanking the 1/2 digit through Q1 and the multiplexed digits through diode D1 to the decoder enable input.

See the MC1405 and MC14435 data sheets for more details of DVM system.

FIGURE 7 – 3-½ DIGIT DIGITAL VOLTMETER



12-HOUR CLOCK WITH GAS DISCHARGE DISPLAYS

The MC3491 or MC3492 cathode drivers and MC3494P anode driver, greatly simplify the interfacing of a clock chip (MOSTEK MK50250) to a gas discharge clock display (Burroughs CD60733-CM).

The MK50250 has a 6 digit clock display with multiplexed 7 segment outputs. The MC3491 cathode drivers switch each display cathode between ground (on condition) and +75 Volts (off condition) with current limiting for the display provided via the current programming pin on the **MC3491 or MC3492. The +75 Volt reference is obtained from a 75-Volt zener diode, Z1, R1, and a 50-Volt zener diode internal to the MC3494P anode driver.**

The programming current is reduced during the time when the "two seconds" indicator digits are ON, to reduce the current through these smaller digits of the display. Four diodes attached to each of the "hours" and "minutes" digits, provide a voltage of +180 Volts across the 680 kΩ resistor. During the "seconds" digits display time, the voltage is reduced to +130 Volts, thus reducing the programming current.

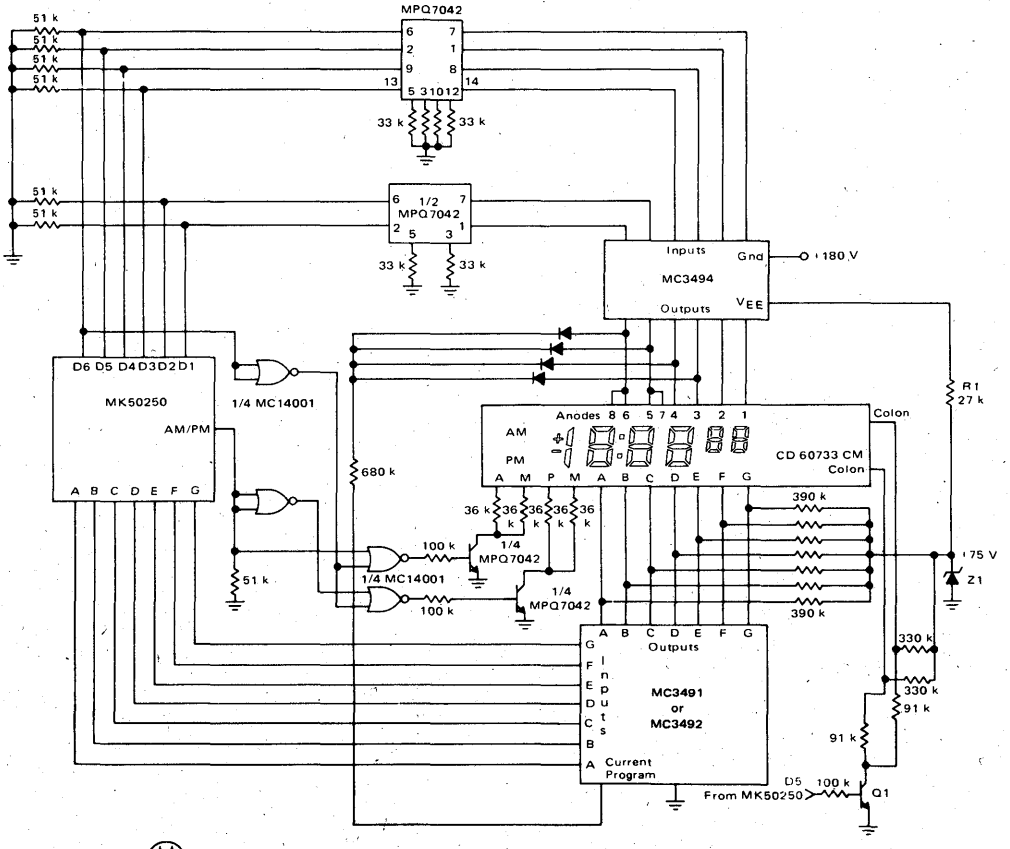
The anodes for each of the six digits are switched between the +180 Volt positive supply and +130 Volts via the MC3494P anode drivers. Inter-digit blanking is provided in the anode circuits. Level translation from the clock chip output to the input to the MC3494P uses two MPQ7042 quad high voltage transistor packages operating in an emitter follower current source mode. Each current source turns on one of the MC3494P drivers by sinking 300 μA to ground for the proper "on" digit.

The AM/PM clock output is in the high state when PM is indicated and has a 85% duty cycle corresponding to each anode on time. A MC14001 Quad NOR Gate decodes this output to turn on the appropriate AM or PM indicator during the D6 digit. These Gates control the AM/PM display indicators with the remaining MPQ7042 high voltage transistors which were not used in anode selection.

The colon separating hours and minutes is switched on during the units of hours digit on time. The colon cathodes are switched from +75 Volts to ground via T1 during the D5 digit time while the anodes are switched between +180 and +130 Volts.

Further information concerning operation or technical specifications on the MOSTEK clock chip, MK50250, and the Burroughs clock display, CD60733-CM is obtainable from the manufacturers.

FIGURE 8 – 12-HOUR CLOCK WITH GAS DISCHARGE DISPLAY SYSTEM



XC6875

Product Preview

M6800 CLOCK GENERATOR

Intended to supply the non-overlapping $\phi 1$ and $\phi 2$ clock signals required by the microprocessor. Both the oscillator and high capacitance driver elements are included along with numerous other logic accessory functions for easy system expansion.

Schottky technology is employed for high speed and PNP-buffered inputs are employed for NMOS compatibility. A single +5 V power supply, and a crystal or RC network for frequency determination are required. The Plastic-packaged version lists for $3.49 at 100–up.

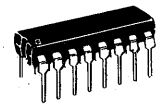
MPU CLOCK GENERATOR

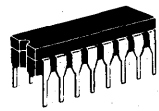
- 4xfo
- 2xfo — A free running oscillator at four times (two times) the MPU's clock rate useful for a system sync signal.
- $\overline{\text{DMA/REF REQ}}$ — An asynchronous input used to freeze the MPU clocks in the $\phi 1$ high, $\phi 2$ low state for dynamic memory refresh or cycle steal DMA (Direct Memory Access).
- DMA/REF GRANT — A synchronous output used to synchronize the refresh or DMA operation to the MPU.
- MEMORY READY — An asynchronous input used to freeze the MPU clocks in the $\phi 1$ low, $\phi 2$ high state for slow memory interface.
- MPU $\phi 1$
MPU $\phi 2$ — Capable of driving the $\phi 1$ and $\phi 2$ inputs on two MC6800's.
- BUS $\phi 2$ — An output nominally in phase with MPU $\phi 2$ having MC8T26 type drive capability which follows MPU $\phi 2$.
- MEMORY CLOCK — An output nominally in phase with MPU $\phi 2$ having MC8T26 type drive capability which free runs during a refresh request cycle.
- $\overline{\text{SYSTEM RESET}}$ — A Schmidt trigger input for attaching a capacitor to ground (power on reset) and/or a switch to ground (reset switch). Internal resistor to V_{CC}.
- $\overline{\text{RESET}}$ — An output to the MPU and I/O devices.
- X1, X2 — Provision to attach a series resonant crystal or RC network.
- EXT IN — Allows driving by an external TTL signal to synchronize the MPU to an external system.

MC6800 TWO PHASE CLOCK GENERATOR/DRIVER

SCHOTTKY MONOLITHIC INTEGRATED CIRCUITS

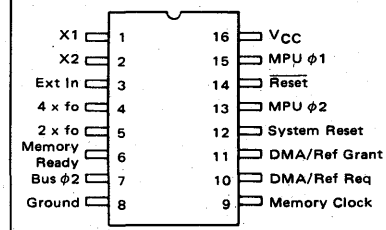
P SUFFIX
PLASTIC PACKAGE
CASE 648





L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN CONNECTIONS



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This is advance information and specifications are subject to change without notice.

MC6880A
MC8T26A

This device may be ordered under either of the above type numbers.

QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the −48 mA driver and −20 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

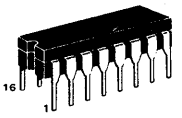
The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of 200 μA at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

The MC8T26A is identical to the NE8T26A and it operates from a single +5 V supply.

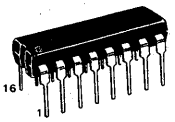
- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible Wtih M6800 Family Microprocessor

5

QUAD THREE-STATE
BUS TRANSCEIVER

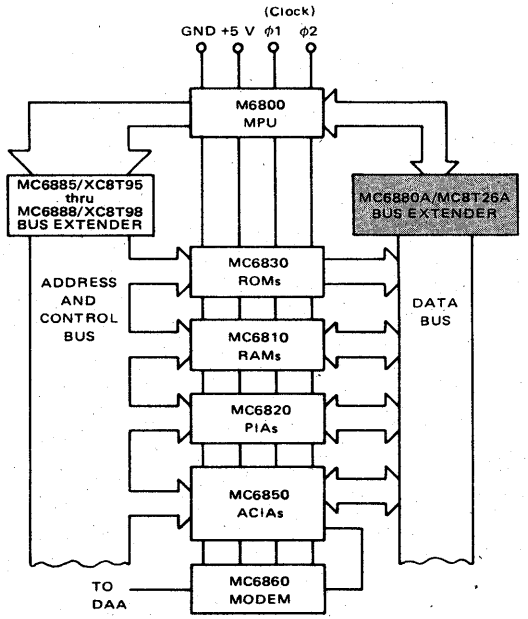


L SUFFIX
CERAMIC PACKAGE
CASE 620

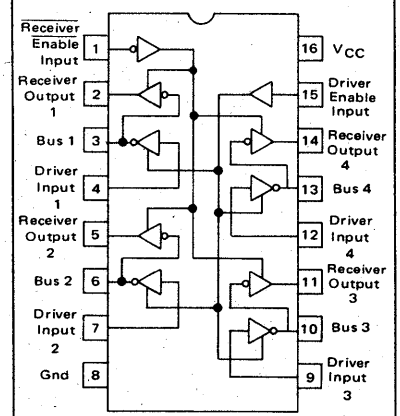


P SUFFIX
PLASTIC PACKAGE
CASE 648

MICROPROCESSOR BUS EXTENDER APPLICATION



PIN CONNECTIONS — MC6880A MC8T26A



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC8T26AL	MC6880AL	0 to +75°C	Ceramic DIP
MC8T26AP	MC6880AP	0 to +75°C	Plastic DIP

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless Otherwise Noted Specifications Apply 4.75 V ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 75°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current — Low Logic State					
(Receiver Enable Input, $V_{IL(RE)}$ = 0.4 V)	$I_{IL(\overline{RE})}$	–	–	-200	μA
(Driver Enable Input, $V_{IL(DE)}$ = 0.4 V)	$I_{IL(DE)}$	–	–	-200	
(Driver Input, $V_{IL(D)}$ = 0.4 V)	$I_{IL(D)}$	–	–	-200	
(Bus (Receiver) Input, $V_{IL(B)}$ = 0.4 V)	$I_{IL(B)}$	–	–	-200	
Input Disabled Current — Low Logic State (Driver Input, $V_{IL(D)}$ = 0.4 V)	$I_{IL(D)\ DIS}$	–	–	-25	μA
Input Current-High Logic State					
(Receiver Enable Input, $V_{IH(RE)}$ = 5.25 V)	$I_{IH(\overline{RE})}$	–	–	25	μA
(Driver Enable Input, $V_{IH(DE)}$ = 5.25 V)	$I_{IH(DE)}$	–	–	25	
(Driver Input, $V_{IH(D)}$ = 5.25 V)	$I_{IH(D)}$	–	–	25	
Input Voltage — Low Logic State					
(Receiver Enable Input)	$V_{IL(\overline{RE})}$	–	–	0.85	V
(Driver Enable Input	$V_{IL(DE)}$	–	–	0.85	
(Driver Input)	$V_{IL(D)}$	–	–	0.85	
(Receiver Input)	$V_{IL(B)}$	–	–	0.85	
Input Voltage — High Logic State					
(Receiver Enable Input)	$V_{IH(\overline{RE})}$	2.0	–	–	V
(Driver Enable Input)	$V_{IH(DE)}$	2.0	–	–	
(Driver Input)	$V_{IH(D)}$	2.0	–	–	
(Receiver Input)	$V_{IH(B)}$	2.0	–	–	
Output Voltage — Low Logic State					
(Bus Driver) Output, $I_{OL(B)}$ = 48 mA)	$V_{OL(B)}$	–	–	0.5	V
(Receiver Output, $I_{OL(R)}$ = 20 mA)	$V_{OL(R)}$	–	–	0.5	
Output Voltage — High Logic State					
(Bus (Driver) Output, $I_{OH(B)}$ = −10 mA)	$V_{OH(B)}$	2.4	3.1	–	V
(Receiver Output, $I_{OH(R)}$ = −2.0 mA)	$V_{OH(R)}$	2.4	3.1	–	
(Receiver Output, $I_{OH(R)}$ = −100μA, V_{CC} = 5.0 V)		3.5	–	–	
Output Disabled Leakage Current — High Logic State					
(Bus Driver) Output, $V_{OH(B)}$ = 2.4 V)	$I_{OHL(B)}$	–	–	100	μA
(Receiver Output, $V_{OH(R)}$ = 2.4 V)	$I_{OHL(R)}$	–	–	100	
Output Disabled Leakage Current — Low Logic State					
(Bus Output, $V_{OL(B)}$ = 0.5 V)	$I_{OLL(B)}$	–	–	−100	μA
(Receiver Output, $V_{OL(R)}$ = 0.5 V)	$I_{OLL(R)}$	–	–	−100	
Input Clamp Voltage					
(Driver Enable Input $I_{ID(DE)}$ = −12 mA)	$V_{IC(DE)}$	–	–	-1.0	V
(Receiver Enable Input $I_{IC(RE)}$ = +12 mA)	$V_{IC(RE)}$	–	–	-1.0	
(Driver Input $I_{IC(D)}$ = −12 mA)	$V_{IC(D)}$	–	–	-1.0	
Output Short-Circuit Current, V_{CC} = 5.25 V (1)					
(Bus (Driver) Output)	$I_{OS(B)}$	-50	–	-150	mA
(Receiver Output)	$I_{OS(R)}$	-30	–	-75	
Power Supply Current (V_{CC} = 5.25 V)	I_{CC}	–	–	87	mA

(1) Only one output may be short-circuited at a time.

SWITCHING CHARACTERISTICS (Unless otherwise noted, specifications apply at $T_A = 25^oC$ and $V_{CC} = 5.0$ V)

Characteristic	Symbol	Figure	Min	Max	Unit
Propagation Delay Time from Receiver (Bus) Input to High Logic State Receiver Output	$t_{PLH(R)}$	1	–	14	ns
Propagation Delay Time from Receiver (Bus) Input to Low Logic State Receiver Output	$t_{PHL(R)}$	1	–	14	ns
Propagation Delay Time from Driver Input to High Logic State Driver (Bus) Output	$t_{PLH(D)}$	2	–	14	ns
Propagation Delay Time from Driver Input to Low Logic State Driver (Bus) Output	$t_{PHL(D)}$	2	–	14	ns
Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to High Impedance (Open) Logic State Receiver Output	$t_{PLZ(RE)}$	3	–	15	ns
Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to Low Logic Level Receiver Output	$t_{PZL(RE)}$	3	–	20	ns
Propagation Delay Time from Driver Enable Input to High Impedance Logic State Driver (Bus) Output	$t_{PLZ(DE)}$	4	–	20	ns
Propagation Delay Time from Driver Enable Input to Low Logic State Driver (Bus) Output	$t_{PZL(DE)}$	4	–	25	ns

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FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT, $t_{PLH(R)}$, $t_{PHL(R)}$

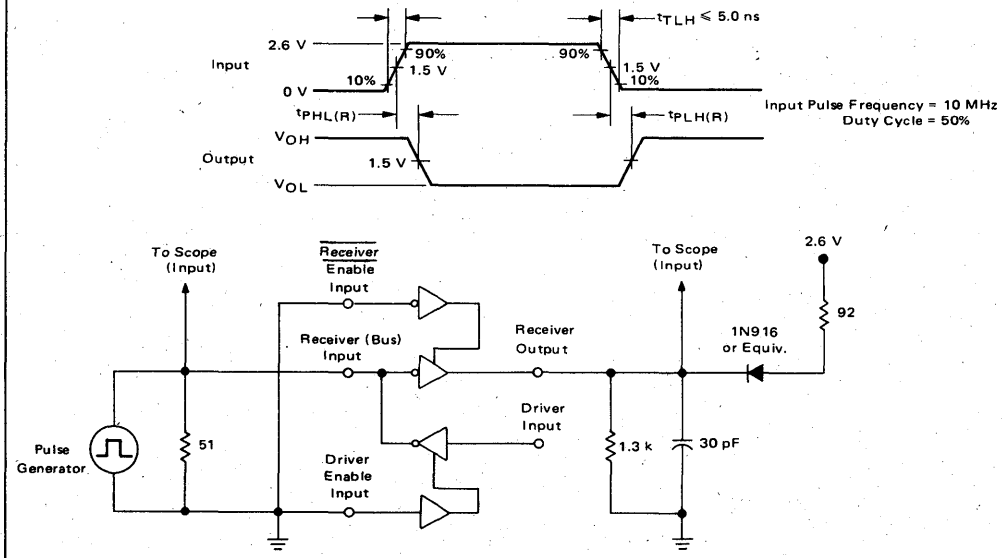

FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PHL(D)}$

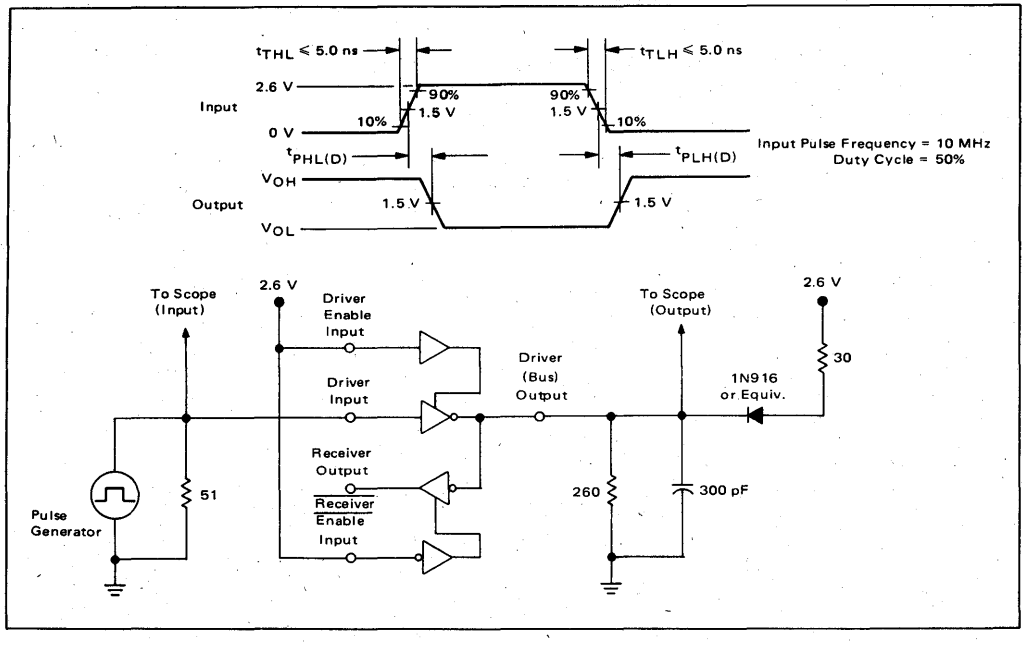

FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLZ(RE)}$, AND $t_{PZL(RE)}$

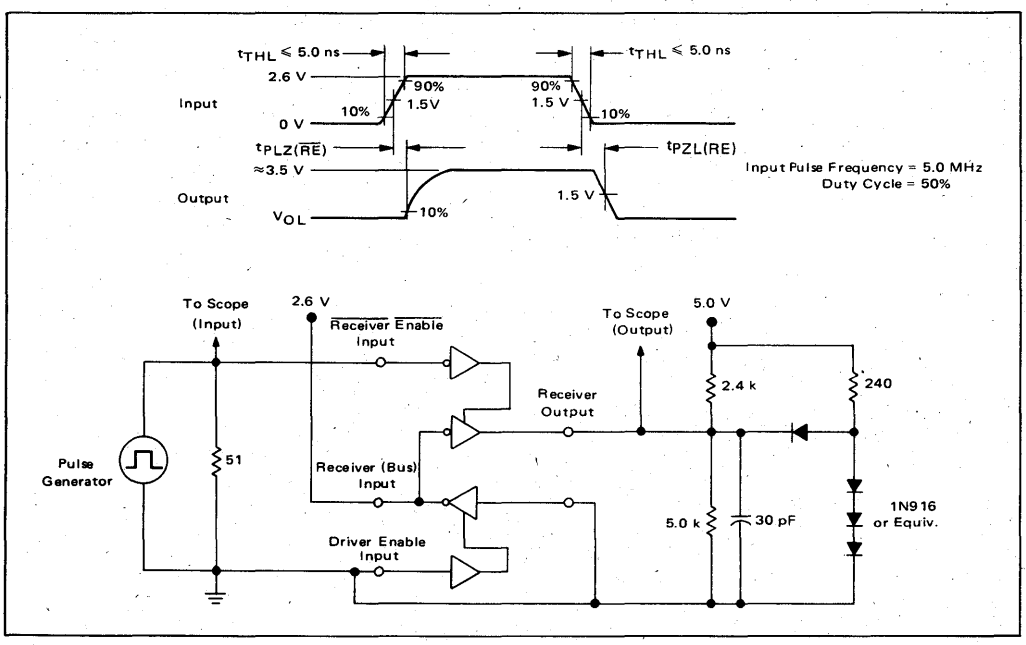

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FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT, $t_{PLO(DE)}$ AND $t_{POL(DE)}$

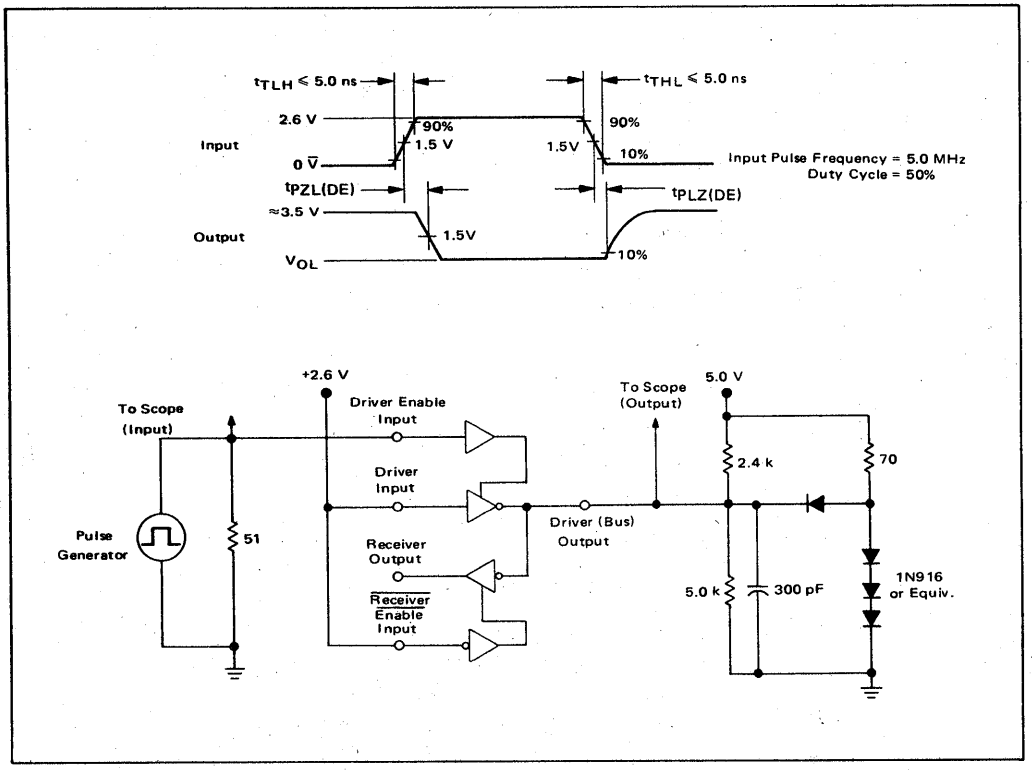
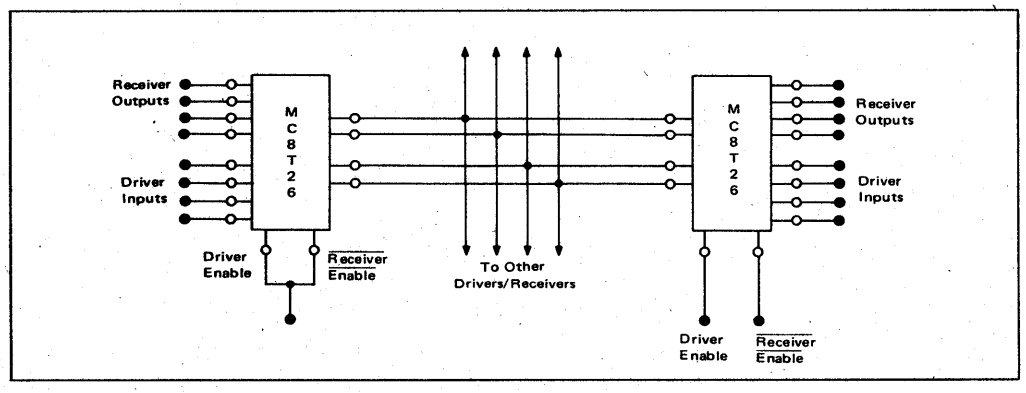


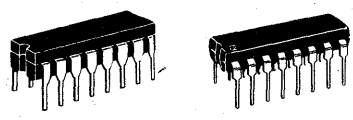
FIGURE 5 – BI-DIRECTIONAL BUS APPLICATIONS



MC6881
MC3449

This device may be ordered under either of the above type numbers.

BI-DIRECTIONAL BUS EXTENDER/SWITCH



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

5

TRIPLE BI-DIRECTIONAL BUS SWITCH

The MC6881/3449 is a three channel, non-inverting, bi-directional Bus Extender. It is designed to allow the bi-directional exchange of TTL level digital information between a selected pair of ports in a three port network. All three ports of each channel may be forced to a high impedance condition through that channel's $\overline{\text{Enable}}$ input.

Port pair selection and listener/talker status for the three channels is determined through the Control and Select inputs. All inputs are PNP buffered, M6800 Family compatible, and protected with Schottky-Barrier diode clamps to suppress undershoot voltages.

A summary of MC6881/3449 features include:

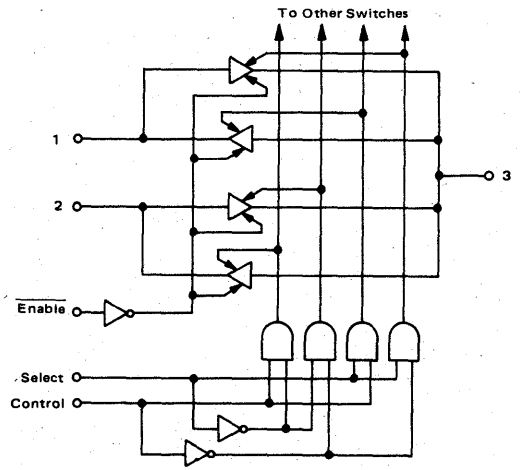
- Three Channels
- Noninverting Data Exchange
- Bi-Directional Operation
- Active Pull-Up with Three-State Capability
- High Impedance Inputs
- TTL Compatible
- High Speed Schottky Technology
- Single Power Supply

TRUTH TABLE

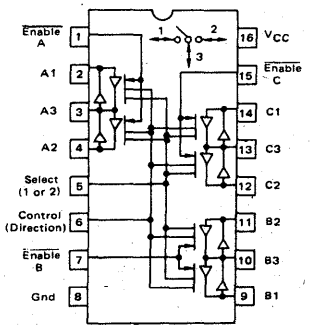
$\overline{\text{Enable}}$	Select	Control	Data Flow
0	0	0	2→3
0	0	1	3→2
0	1	0	1→3
0	1	1	3→1
1	X	X	High Impedance

X - Don't Care

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC3449L	MC6881L	0 to +70°C	Ceramic DIP
MC3449P	MC6881P	0 to +70°C	Plastic DIP

ELECTRICAL CHARACTERISTICS ($4.75\ V \leq V_{CC} \leq 5.25\ V, 0^{\circ}C \leq T_A \leq 70^{\circ}C$)

Characteristic	Symbol	Min	Max	Unit
Input Current – Low Logic State (V_{IL} = 0.4 V)	I_{IL}	–	–200	μA
Input Current – High Logic State	I_{IH}			μA
(V_{IH} = 2.7 V)		–	40	
(V_{IH} = 5.25 V)		–	100	
Input Voltage – Low Logic State	V_{IL}	0.8	–	V
Input Voltage – High Logic State	V_{IH}	–	2.0	V
Output Voltage – Low Logic State	V_{OL}			V
(I_{OL} = 8.0 mA)		–	0.5	
(I_{OL} = 16 mA)		–	0.6	
Output Voltage – High Logic State (I_{OH} = –1.0 mA)	V_{OH}	2.4	–	V
Output Disabled Current	I_{OD}			μA
(V_{OH} = 2.7 V)		–	25	
(V_{OL} = 0.4 V)		–	-40	
Power Supply Current	I_{CC}	–	50	mA

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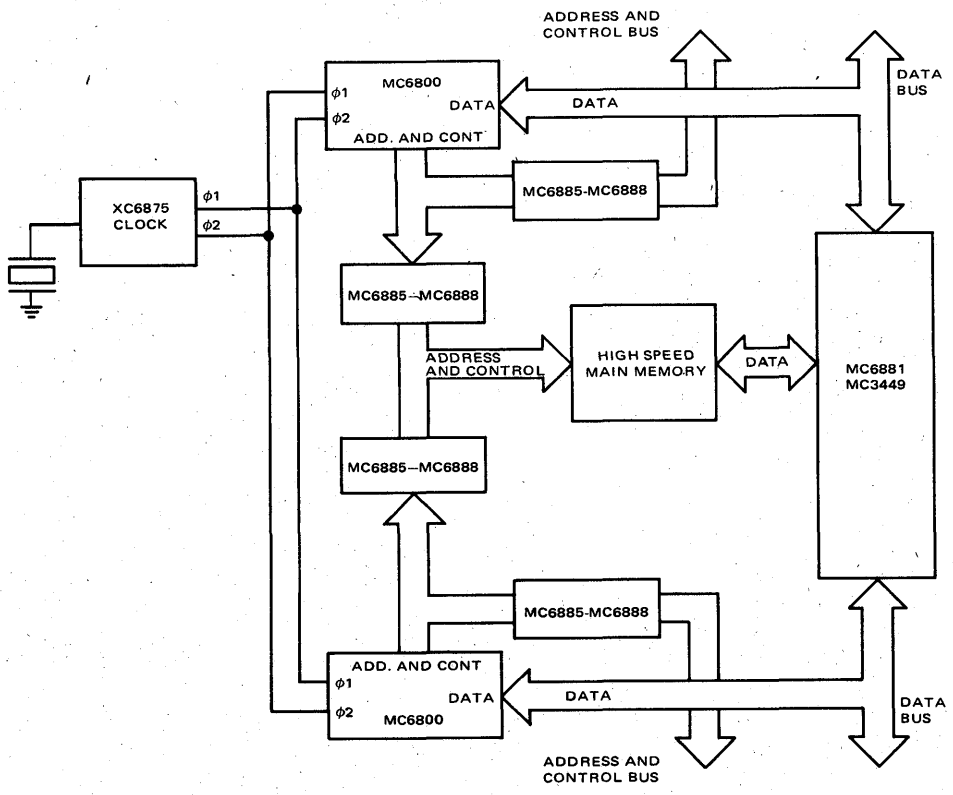
Two MPUs SHARING a Common Main-Memory



MC6885/MC8T95
MC6886/MC8T96
MC6887/MC8T97
MC6888/MC8T98

This device may be ordered under either of the above type numbers.

Advance Information

HEX THREE-STATE BUFFER INVERTERS

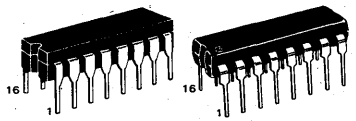
This series of devices combines four features usually found desirable in bus oriented systems. These features are: 1) – high impedance logic inputs insure that these devices do not seriously load the bus, 2) – three-state logic configuration allows buffers not being utilized to be effectively removed from the bus, 3) Schottky technology allows high-speed operation and 4) High-impedance output state maintained during power up/down.

The devices differ in that the non-inverting MC8T95/MC6885 and inverting MC8T96/MC6886 provide a two-input Enable which controls all six buffers, while the non-inverting MC8T97/MC6887 and inverting MC8T98/MC6888 provide two Enable inputs – one controlling four buffers and the other controlling the remaining two buffers.

The units are well-suited for Address buffers on the M6800 or similar microprocessor application.

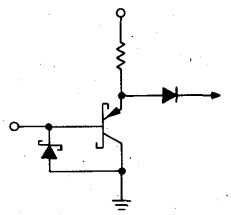
- High Speed – 8.0 ns (Typ)
- Three-State Logic Configuration
- Single +5 V Power Supply Requirement
- Compatible with 74S Logic or M6800 Microprocessor Systems
- High Impedance PNP Inputs Assure Minimal Loading of the Bus

HEX THREE-STATE BUFFER/INVERTERS

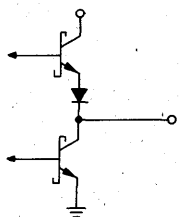


CASE 620 CASE 648

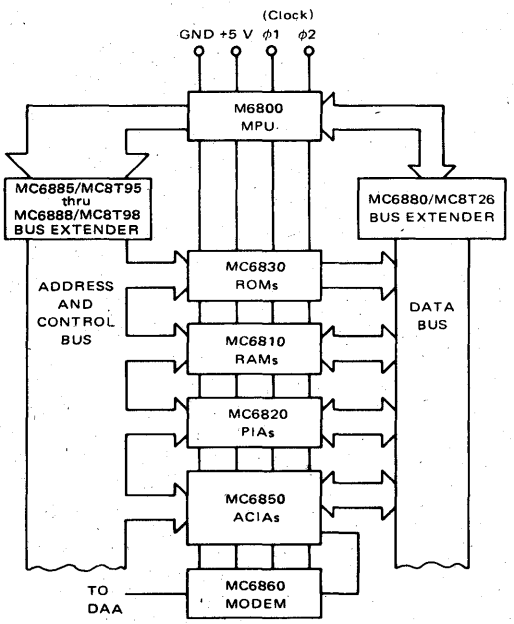
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT



MICROPROCESSOR BUS EXTENDER APPLICATION



ORDERING INFORMATION

(Temperature Range for the following devices = 0 to +75°C)

DEVICE	ALTERNATE	PACKAGE
MC6885L	MC8T95L	Ceramic DIP
MC6886L	MC8T96L	Ceramic DIP
MC6887L	MC8T97L	Ceramic DIP
MC6888L	MC8T98L	Ceramic DIP
MC6885P	MC8T95P	Plastic DIP
MC6886P	MC8T96P	Plastic DIP
MC6887P	MC8T97P	Plastic DIP
MC6888P	MC8T98P	Plastic DIP

This is advance information and specifications are subject to change without notice.

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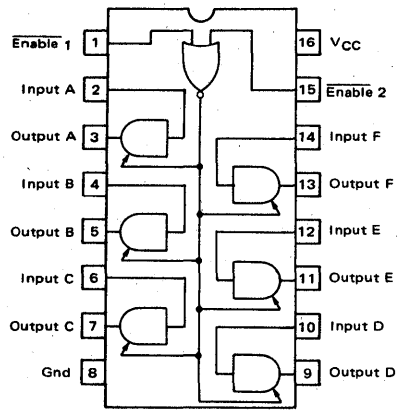
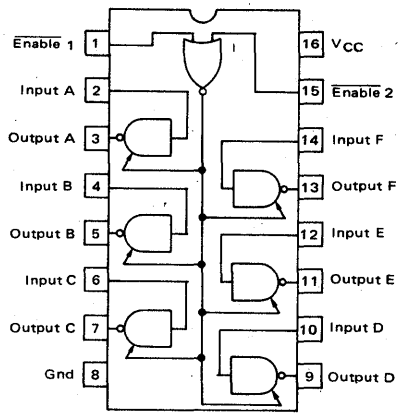
PIN CONNECTIONS AND TRUTH TABLES

MC6885/MC8T95



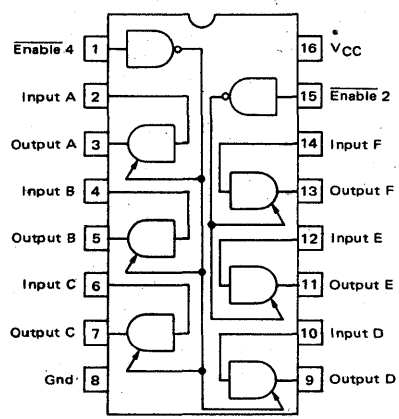
Enable 2	Enable 1	Input	Output
L	L	L	L
L	L	H	H
L	H	X	Z
H	L	X	Z
H	H	X	Z

MC6886/MC8T96



Enable 2	Enable 1	Input	Output
L	L	L	H
L	L	H	L
L	H	X	Z
H	L	X	Z
H	H	X	Z

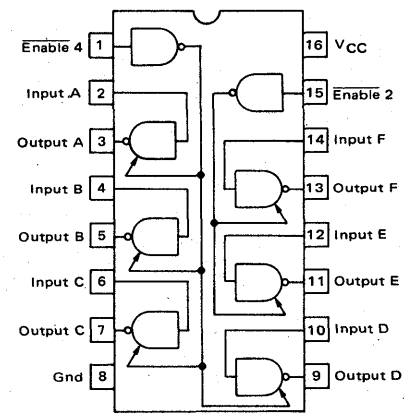
MC6887/MC8T97



Enable	Input	Output
L	L	L
L	H	H
H	X	Z

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
X = Irrelevant

MC6888/MC8T98



Enable	Input	Output
L	L	H
L	H	L
H	X	Z

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 150 175	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $0^{o}C \leq T_A \leq 75^{o}C$ and $4.75\ V \leq V_{CC} \leq 5.25\ V$)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – High Logic State (V_{CC} = 4.75 V, T_A = 25°C)	V_{IH}	2.0	–	–	V
Input Voltage – Low Logic State (V_{CC} = 4.75 V, T_A = 25°C)	V_{IL}	–	–	0.8	V
Input Current – High Logic State (V_{CC} = 5.25 V, V_{IH} = 2.4 V)	I_{IH}	–	–	40	μA
Input Current – Low Logic State (V_{CC} = 5.25 V, V_{IL} = 0.5 V, $V_{IL(\overline{E})}$ = 0.5 V)	I_{IL}	–	–	-400	μA
Input Current – High Impedance State (V_{CC} = 5.25 V, $V_{IL(I)}$ = 0.5 V, $V_{IH(\overline{E})}$ = 2.0 V)	$I_{IH(\overline{E})}$	–	–	-40	μA
Output Voltage – High Logic State (V_{CC} = 4.75 V, I_{OH} = -5.2 mA)	V_{OH}	2.4	–	–	V
Output Voltage – Low Logic State (I_{OL} = 48 mA)	V_{OL}	–	–	0.5	V
Output Current – High Impedance State (V_{CC} = 5.25 V, V_{OH} = 2.4 V) (V_{CC} = 5.25 V, V_{OL} = 0.5 V)	I_{OZ}	– –	– –	40 -40	μA
Output Short-Circuit Current (V_{CC} = 5.25 V, V_O = 0) (only one output can be shorted at a time)	I_{OS}	-40	-80	-115	mA
Power Supply Current (V_{CC} = 5.25 V) MC8T95, MC8T97, MC6885, MC6887 MC8T96, MC8T98, MC6886, MC6888	I_{CC}	– –	65 59	98 89	mA
Input Clamp Voltage (V_{CC} = 4.75 V, I_{IC} = -12 mA)	V_{IC}	–	–	-1.5	V
Output V_{CC} Clamp Voltage (V_{CC} = 0, I_{OC} = 12 mA)	V_{OC}	–	–	1.5	V
Output Gnd Clamp Voltage (V_{CC} = 0, I_{OC} = -12 mA)	V_{OC}	–	–	-1.5	V
Input Voltage (I_I = 1.0 mA)	V_I	5.5	–	–	V

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC8T95/97 MC6885/87 Min	MC8T95/97 MC6885/87 Typ	MC8T95/97 MC6885/87 Max	MC8T96/98 MC6886/88 Min	MC8T96/98 MC6886/88 Typ	MC8T96/98 MC6886/88 Min	Unit
Propagation Delay Time – High to Low State	t_{PHL}							ns
(C_L = 50 pF)		3.0	–	12	4.0	–	11	
(C_L = 250 pF)		–	16	–	–	15	–	
(C_L = 375 pF)		–	20	–	–	18	–	
(C_L = 500 pF)		–	23	–	–	22	–	
Propagation Delay Time – Low to High State	t_{PLH}							ns
(C_L = 50 pF)		3.0	–	13	3.0	–	10	
(C_L = 250 pF)		–	25	–	–	22	–	
(C_L = 375 pF)		–	33	–	–		–	
(C_L = 500 pF)		–	42	–	–	35	–	
Transition Time – High to Low State	t_{THL}							ns
(C_L = 250 pF)		–	10	–	–	10	–	
(C_L = 375 pF)		–	11	–	–	13	–	
(C_L = 500 pF)		–	14	–	–	15	–	
Transition Time – Low to High State	t_{TLH}							ns
(C_L = 250 pF)		–	32	–	–	28	–	
(C_L = 375 pF)		–	42	–	–	38	–	
(C_L = 500 pF)		–	60	–	–	53	–	

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SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC8T95/97 MC6885/87 Min	Typ	Max	MC8T96/98 MC6886/88 Min	Typ	Min	Unit
Propagation Delay Time – High State to Third State (C_L = 5.0 pF)	$t_{PHZ(\overline{E})}$	3.0	–	10	3.0	–	10	ns
Propagation Delay Time – Low State to Third State (C_L = 5.0 pF)	$t_{PLZ(\overline{E})}$	3.0	–	12	5.0	–	16	ns
Propagation Delay Time – Third State to High State (C_L = 50 pF)	$t_{PZH(\overline{E})}$	8.0	–	25	7.0	–	22	ns
Propagation Delay Time – Third State to Low State (C_L = 50 pF)	$t_{PZL(\overline{E})}$	12	–	25	11	–	24	ns

FIGURE 1 – TEST CIRCUIT FOR SWITCHING CHARACTERISTICS

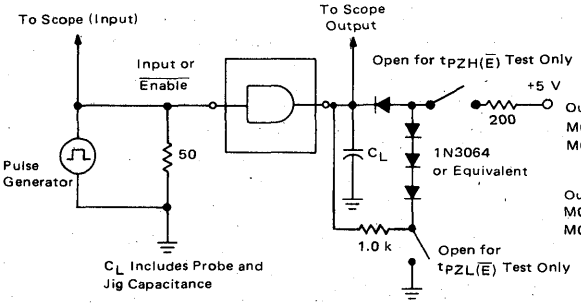


FIGURE 2 – WAVEFORMS FOR PROPAGATION DELAY TIMES INPUT TO OUTPUT

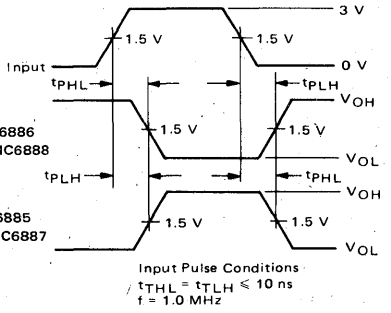
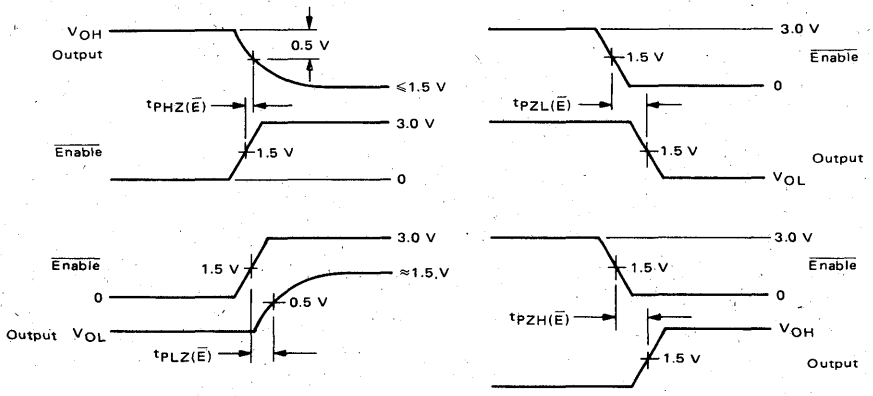
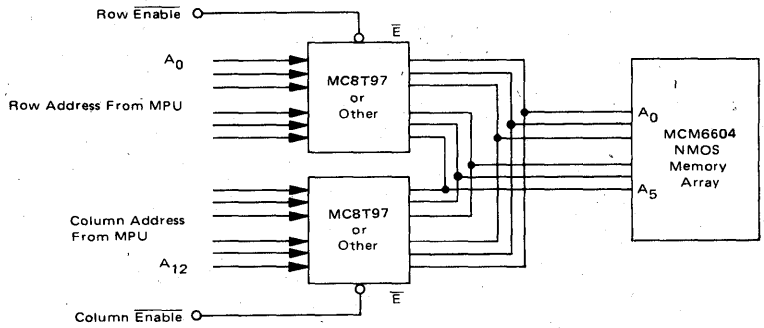


FIGURE 3 – WAVEFORMS FOR PROPAGATION DELAY TIMES – $\overline{\text{ENABLE}}$ TO OUTPUT



H = High-Logic State, L = Low-Logic State, Z = High Impedance State

FIGURE 4 – ADDRESS MULTIPLEXER FOR 16-PIN 4K NMOS MEMORY



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THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

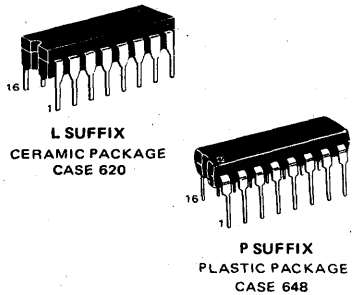
T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

MC6889
MC8T28

This device may be ordered under either of the above type numbers.

NON-INVERTING BUS TRANSCEIVER



NON-INVERTING QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the -48 mA driver and -20 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of 200 μA at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

Propagation delay times for the driver portion are 17 ns maximum while the receiver portion runs 17 ns for t_{PHL} and 17 ns for t_{PLH}. The MC8T28 is identical to the NE8T28 and it operates from a single +5 V supply.

- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible with M6800 Family Microprocessor
- Non-Inverting

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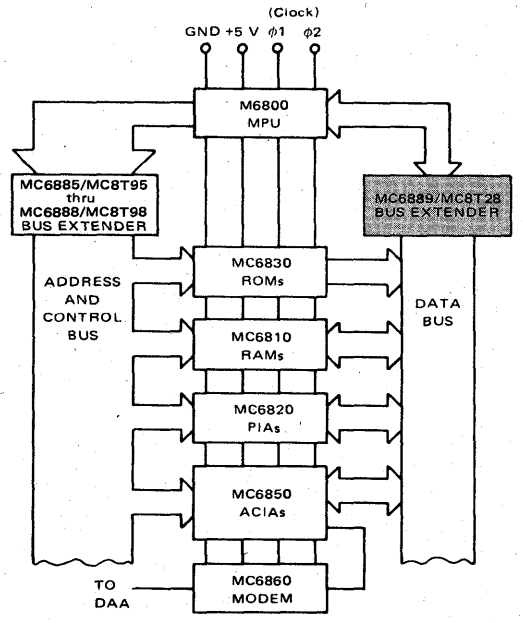
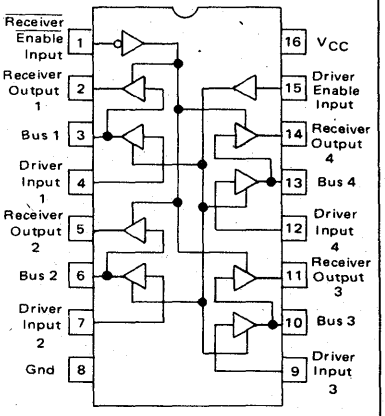
MICROPROCESSOR BUS EXTENDER APPLICATION



PIN CONNECTIONS – MC6889 MC8T28



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC8T28L	MC6889L	0 to +75°C	Ceramic DIP
MC8T28P	MC6889P	0 to +75°C	Plastic DIP

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless Otherwise Noted Specifications Apply 4.75 V ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 75°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current — Low Logic State					
(Receiver Enable Input, $V_{IL(\overline{RE})}$ = 0.4 V)	$I_{IL(\overline{RE})}$	–	–	-200	μA
(Driver Enable Input, $V_{IL(DE)}$ = 0.4 V)	$I_{IL(DE)}$	–	–	-200	
(Driver Input, $V_{IL(D)}$ = 0.4 V)	$I_{IL(D)}$	–	–	-200	
(Bus (Receiver) Input, $V_{IL(B)}$ = 0.4 V)	$I_{IL(B)}$	–	–	-200	
Input Disabled Current — Low Logic State					
(Driver Input, $V_{IL(D)}$ = 0.4 V)	$I_{IL(D)\ DIS}$	–	–	-25	μA
Input Current-High Logic State					
(Receiver Enable Input, $V_{IH(\overline{RE})}$ = 5.25 V)	$I_{IH(\overline{RE})}$	–	–	25	μA
(Driver Enable Input, $V_{IH(DE)}$ = 5.25 V)	$I_{IH(DE)}$	–	–	25	
(Driver Input, $V_{IH(D)}$ = 5.25 V)	$I_{IH(D)}$	–	–	25	
Input Voltage — Low Logic State					
(Receiver Enable Input)	$V_{IL(\overline{RE})}$	–	–	0.85	V
(Driver Enable Input	$V_{IL(DE)}$	–	–	0.85	
(Driver Input)	$V_{IL(D)}$	–	–	0.85	
(Receiver Input)	$V_{IL(B)}$	–	–	0.85	
Input Voltage — High Logic State					
(Receiver Enable Input)	$V_{IH(\overline{RE})}$	2.0	–	–	V
(Driver Enable Input)	$V_{IH(DE)}$	2.0	–	–	
(Driver Input)	$V_{IH(D)}$	2.0	–	–	
(Receiver Input)	$V_{IH(B)}$	3.0	–	–	
Output Voltage — Low Logic State					
(Bus Driver) Output, $I_{OL(B)}$ = 48 mA)	$V_{OL(B)}$	–	–	0.5	V
(Receiver Output, $I_{OL(R)}$ = 20 mA)	$V_{OL(R)}$	–	–	0.5	
Output Voltage — High Logic State					
(Bus (Driver) Output, $I_{OH(B)}$ = −10 mA)	$V_{OH(B)}$	2.4	3.1	–	V
(Receiver Output, $I_{OH(R)}$ = −2.0 mA)	$V_{OH(R)}$	2.4	3.1	–	
(Receiver Output, $I_{OH(R)}$ = −100μA, V_{CC} = 5.0 V)		3.5	–	–	
Output Disabled Leakage Current — High Logic State					
(Bus Driver) Output, $V_{OH(B)}$ = 2.4 V)	$I_{OHL(B)}$	–	–	100	μA
(Receiver Output, $V_{OH(R)}$ = 2.4 V)	$I_{OHL(R)}$	–	–	100	
Output Disabled Leakage Current — Low Logic State					
(Bus Output, $V_{OL(B)}$ = 0.5 V)	$I_{OLL(R)}$	–	–	−100	μA
(Receiver Output, $V_{OL(R)}$ = 0.5 V)	$I_{OLL(R)}$	–	–	−100	
Input Clamp Voltage					
(Driver Enable Input $I_{ID(DE)}$ = −12 mA)	$V_{IC(DE)}$	–	–	-1.0	V
(Receiver Enable Input $I_{IC(RE)}$ = −12 mA)	$V_{IC(RE)}$	–	–	-1.0	
(Driver Input $I_{IC(D)}$ = −12 mA)	$V_{IC(D)}$	–	–	-1.0	
Output Short-Circuit Current, V_{CC} = 5.25 V (1)					
(Bus (Driver) Output)	$I_{OS(B)}$	-50	–	-150	mA
(Receiver Output)	$I_{OS(R)}$	-30	–	-75	
Power Supply Current (V_{CC} = 5.25 V)	I_{CC}	–	–	110	mA

(1) Only one output may be short-circuited at a time.

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V and T_A = 25°C)

Characteristic	Symbol	Min	Max	Unit
Propagation Delay Time—Receiver (C_L = 30 pF)	$t_{PLH(R)}$ $t_{PHL(R)}$	–	17	ns
Propagation Delay Time—Driver (C_L = 300 pF)	$t_{PLH(D)}$ $t_{PHL(D)}$	–	17	ns
Propagation Delay Time—Enables (C_L = 30 pF)	$t_{PZL(R)}$ $t_{PLZ(R)}$	– –	23 18	ns
(C_L = 300 pF)	$t_{PZL(D)}$ $t_{PLZ(D)}$	– –	28 23	

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ORDERING INFORMATION

Device	Temperature Range	Package
MC5524L	−55°C to +125°C	Ceramic DIP
MC5525L	−55°C to +125°C	Ceramic DIP
MC7524L	0°C to +70°C	Ceramic DIP
MC7524P	0°C to +70°C	Plastic DIP
MC7525L	0°C to +70°C	Ceramic DIP
MC7525P	0°C to +70°C	Plastic DIP

MC7524 MC5524
MC7525 MC5525

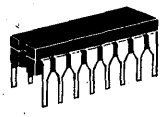
DUAL SENSE AMPLIFIERS

This dual sense amplifier is designed for use with high-speed memory systems. Low level pulses originating in the memory are converted to logic levels compatible with MDTL and MTTL circuits.

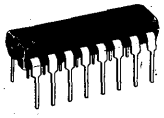
- Adjustable Threshold Voltage Levels
- High-Speed, Fast Recovery Time
- Time and Amplitude Signal Discrimination
- High dc Logic Noise Margin
  1.0 Volt typ
- Good Fan-Out Capability
- Independent Strobing
- Separate Logic Outputs

DUAL HIGH-SPEED SENSE AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648
(MC7524 and MC7525 Only)

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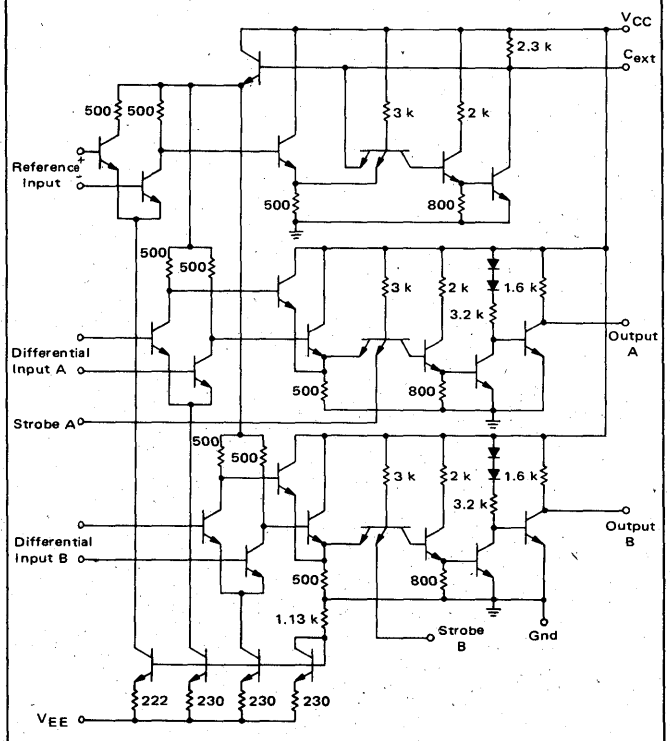
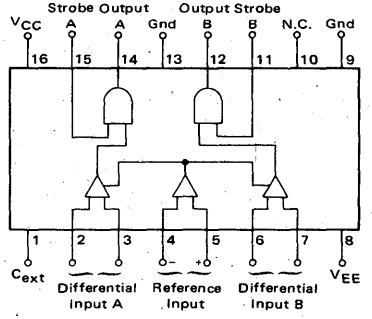
SCHEMATIC DIAGRAM



PIN CONNECTIONS



TRUTH TABLE

Differential Input	Strobe Input	Output
0	L	L
1	L	L
0	H	L
1	H	H

Where:

H = High Logic State
L = Low Logic State
0 = $V_{in} < V_{TH}$
1 = $V_{in} > V_{TH}$

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC} V_{EE}	+7.0 -7.0	Vdc Vdc
Differential Input Voltages		V_{in} or V_{ref}	±5.0	Vdc
Power Dissipation Derate above T_A = +25°C		P_D	575 3.85	mW mW/°C
Operating Ambient Temperature Range	MC5524, MC5525 MC7524, MC7525	T_A	-55 to +125 0 to +70	°C
Storage Temperature Range		T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = T_{high} to T_{low} unless otherwise noted.)

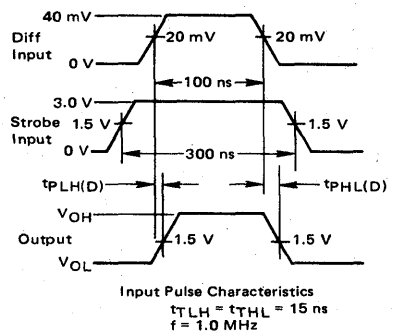
Characteristic			Symbol	Min	Typ	Max	Unit
Input Threshold Voltage			V_{th}				mV
(V_{ref} = 15 mV)	MC5524, MC7524	T_A = 0 to 70°C		11	15	19	
	MC5525, MC7525			8.0	15	22	
(V_{ref} = 40 mV)	MC5524, MC7524			36	40	44	
	MC5525, MC7525			33	40	47	
(V_{ref} = 15 mV)	MC5524	T_A = -55°C to 0°C and T_A = 70°C to 125°C		10	15	20	
	MC5525	T_A = -55°C to 0°C and T_A = 70°C to 125°C		8.0	15	22	
(V_{ref} = 40 mV)	MC5524	T_A = -55°C to 0°C and T_A = 70°C to 125°C		35	40	45	
	MC5525	T_A = -55°C to 0°C and T_A = 70°C to 125°C		33	40	47	
Input Common-Mode Firing Voltage (V_{ref} = 20 mV, $V_{IH(S)}$ = 5.0 V)			V_{ICF}	–	±3.0	–	Volts
Input Bias Current (V_{CC} = 5.25 V, V_{EE} = -5.25 V, T_A = -55°C to 0°C) MC5524,MC5525 (V_{CC} = 5.25 V, V_{EE} = -5.25 V, T_A = 0°C to T_{high}) MC7524,MC7525			I_{IB}	 – –	 – 30	 100 75	μA
Input Offset Current (V_{CC} = 5.25 V, V_{EE} = -5.25 V)			I_{IO}	–	0.5	–	μA
Differential Input Impedance (f = 1.0 kHz)			z_{id}	–	2.0	–	k ohms
Strobe Input Voltage – High Logic State			$V_{IH(S)}$	2.0	–	–	Volts
Strobe Input Voltage – Low Logic State			$V_{IL(S)}$	–	–	0.8	Volt
Strobe Input Current – Low Logic State ($V_{IL(S)}$ = 0.4 V)			$I_{IL(S)}$	–	-1.0	-1.6	mA
Strobe Input Current – High Logic State ($V_{IH(S)}$ = 2.4 V) ($V_{IH(S)}$ = 5.25 V)			$I_{IH(S)}$	 – –	 – –	 40 1.0	 μA mA
Output Voltage – High Logic State (V_{CC} = 4.75 V, V_{EE} = -4.75 V, I_{OH} = -400 μA)			V_{OH}	2.4	3.9	–	Volts
Output Voltage – Low Logic State (V_{CC} = 4.75 V, V_{EE} = -4.75 V, I_{OL} = 16 mA)			V_{OL}	–	0.25	0.4	Volt
Short-Circuit Output Current (V_{CC} = 5.25 V, V_{EE} = -5.25 V)			I_{OS}	2.1	–	3.5	mA
Power Supply Currents (V_{CC} = 5.25 V, V_{EE} = -5.25 V, T_A = 25°C)			 I_{CC} I_{EE}	 – –	 25 -15	 40 -20	mA

*T_{high} = 125°C for MC5524 and MC5525
T_{high} = 70°C for MC7524 and MC7525
T_{low} = -55°C for MC5524 and MC5525
T_{low} = 0°C for MC7524 and MC7525

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = -5.0 V, T_A = 25°C unless otherwise noted.)

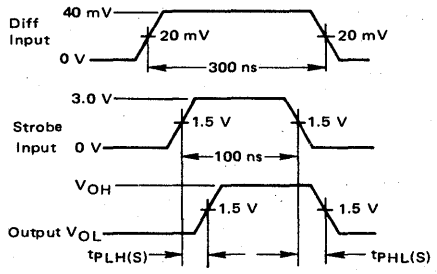
Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Differential Input to Output	$t_{PLH(D)}$ $t_{PHL(D)}$	– –	15 40	40 –	ns
Propagation Delay Time — Strobe Input to Output	$t_{PLH(S)}$ $t_{PHL(S)}$	– –	15 35	30 –	ns
Differential-Mode Input Overload Recovery Time	$t_{OR(DM)}$	–	20	–	ns
Common-Mode Input Overload Recovery Time	$t_{OR(CM)}$	–	20	–	ns
Minimum Cycle Time	$t_{C(min)}$	–	200	–	ns

PROPAGATION DELAY TIME — DIFFERENTIAL INPUT to OUTPUT

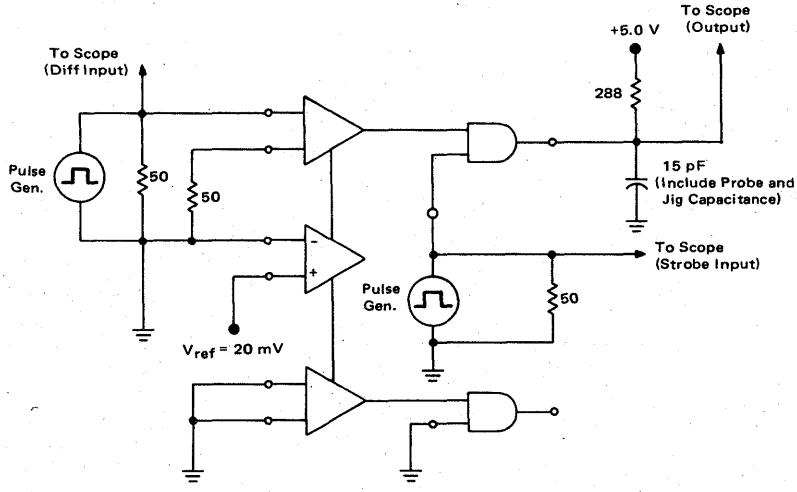


Input Pulse Characteristics
$t_{TLH} = t_{THL}$ = 15 ns
f = 1.0 MHz

PROPAGATION DELAY TIME STROBE INPUT to OUTPUT



PROPAGATION DELAY TIMES TEST CIRCUIT



ORDERING INFORMATION

Device	Temperature Range	Package
MC5528L	−55°C to +125°C	Ceramic DIP
MC5529L	−55°C to +125°C	Ceramic DIP
MC7528L	0°C to +70°C	Ceramic DIP
MC7528P	0°C to +70°C	Plastic DIP
MC7529L	0°C to +70°C	Ceramic DIP
MC7529P	0°C to +70°C	Plastic DIP

MC7528 MC5528
MC7529 MC5529

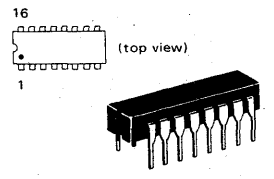
MONOLITHIC DUAL SENSE AMPLIFIERS WITH PREAMPLIFIER TEST POINTS

This dual sense amplifier is designed for use with high-speed memory systems. Low level pulses originating in the memory are converted to logic levels compatible with MDTL and MTTL circuits. External preamplifier test points provide for very accurate timing of the strobe with the input signal.

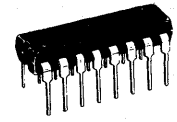
- Adjustable Threshold Voltage Levels
- High-Speed, Fast Recovery Time
- Time and Amplitude Signal Discrimination
- High dc Logic Noise Margin
  1.0 Volt typ
- Good Fan-Out Capability
- Independent Strobing
- Separate Logic Outputs
- Test Points Available for Accurate Strobe Timing

DUAL HIGH-SPEED SENSE AMPLIFIER WITH PREAMPLIFIER TEST POINTS

MONOLITHIC SILICON INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648
(MC7528 and MC7529 only)

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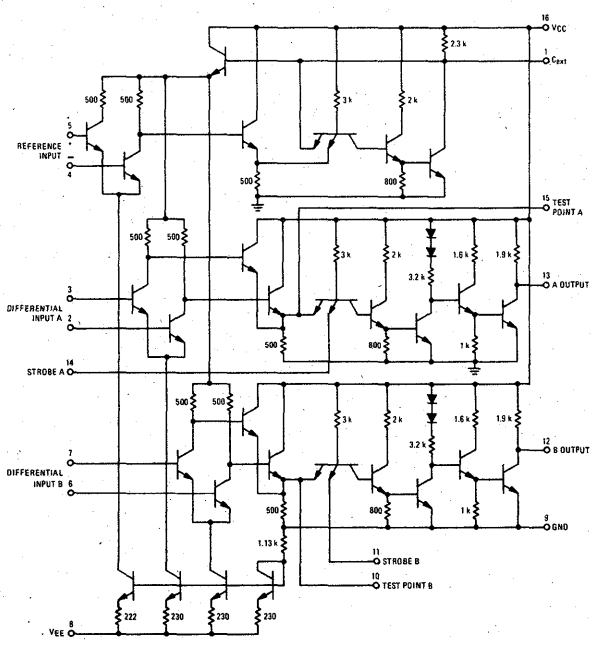
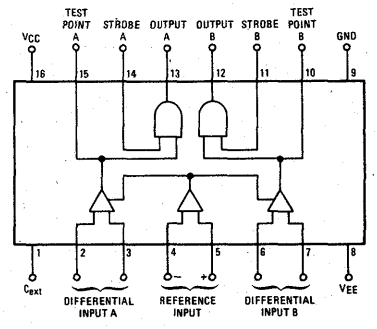
SCHEMATIC DIAGRAM





MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Units
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Vdc Vdc
Differential Input Voltages	V_{in} or V_{ref}	±5.0	Vdc
Power Dissipation Derate above T_A = +25°C	P_D	575 3.85	mW mW/°C
Operating Temperature Range MC5528, MC5529 MC7528, MC7529	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V ±5%, V_{EE} = -5.0 V ±5%, T_A = T_{low}# to T_{high}# unless otherwise noted.)

Characteristic		Symbol	MC5528 ① # MC5529 Min	MC5528 ① # MC5529 Typ	MC5528 ① # MC5529 Max	MC7528 # MC7529 Min	MC7528 # MC7529 Typ	MC7528 # MC7529 Max	Unit
Differential Input Threshold Voltage (V_{inS} = +5.0 V, V_{ID} = ±V_{th})		V_{th}							mV
(V_{ref} = 15 mV, I_L = 16 mA, V_O <0.4 V)	MC5528,MC7528		10	15	–	11	15	–	
	MC5529,MC7529		8.0	–	–	8.0	–	–	
(V_{ref} = 40 mV, I_L = 16 mA, V_O <0.4 V)	MC5528,MC7528		35	40	–	36	40	–	
	MC5529,MC7529		33	–	–	33	–	–	
(V_{ref} = 15 mV, I_L = -400 µA, V_O >2.4 V)	MC5528,MC7528		–	15	20	–	15	19	
	MC5529,MC7529		–	–	22	–	–	22	
(V_{ref} = 40 mV, I_L = -400 µA, V_O >2.4 V)	MC5528,MC7528		–	40	45	–	40	44	
	MC5529,MC7529		–	–	47	–	–	47	
Differential and Reference Input Bias Current (V_{ID} = V_{ref} = 0V, V_{inS} = +5.25 V, V_S = ±5.25 V)		I_{IB}	–	30	100	–	30	75	µA
Differential Input Offset Current (V_{ID} = V_{ref} = 0 V, V_{inS} = +5.25 V, V_S = ±5.25 V)		I_{IOD}	–	0.5	–	–	0.5	–	µA
Input Voltage, Logic "1" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 2.0 V, I_L = 400 µA, V_S = ±4.75 V, V_O >2.4 V)		V_{in}"1"	2.0	–	–	2.0	–	–	V
Input Voltage, Logic "0" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 0.8 V, I_L = 16 mA, V_S = ±4.75 V, V_{OL} <0.4 V)		V_{in}"0"	–	–	0.8	–	–	0.8	V
Input Current, Logic "1" (V_{ID} = 0 V, V_{ref} = 20 mV, V_{inS} = 2.4 V, V_S = ±5.25 V)	MC5528,MC5529	I_{in}"1"	–	5.0	40	–	–	–	µA
(V_{ID} = 0 V, V_{ref} = 20 mV, V_{inS} = +5.25 V, V_S = ±5.25 V)	MC7528,MC7529		–	–	–	–	0.02	1.0	mA
Input Current, Logic "0" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 0.4 V, V_S = ±5.25 V)		I_{in}"0"	–	-1.0	-1.6	–	-1.0	-1.6	mA
Output Voltage, Logic "1" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 2.0 V, I_L = -400 µA, V_S = ±4.75 V)		V_O"1"	2.4	3.9	–	2.4	3.9	–	V
Output Voltage, Logic "0" (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 0.8 V, I_L = 16 mA, V_S = ±4.75 V)		V_O"0"	–	0.25	0.40	–	0.25	0.40	V
Short-Circuit Output Current (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = +5.25 V, V_S = ±5.25 V)		I_{OSC}	-2.1	-2.8	-3.5	-2.1	-2.8	-3.5	mA
V_{CC} Supply Current (V_{ID} = V_{inS} = 0 V, V_{ref} = 20 mV, V_S = ±5.25 V)		I_{CC}	–	29	40	–	29	40	mA
V_{EE} Supply Current (V_{ID} = V_{inS} = 0 V, V_{ref} = 20 mV, V_S = ±5.25 V)		I_{EE}	–	-13	-18	–	-13	-18	mA

① For 0°C ≤ T_A ≤ 70°C operation; electrical characteristics for MC5528 and MC5529 are guaranteed the same as MC7528 and MC7529 respectively.

T_{low} = -55°C for MC5528, MC5529, 0°C for MC7528, MC7529
T_{high} = +125°C for MC5528, MC5529; +70°C for MC7528, MC7529

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V ±5%, V_{EE} = -5.0 V ±5%, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC5528 MC5529			MC7528 MC7529			Unit
		Min	Typ	Max	Min	Typ	Max	
AC Common-Mode Input Firing Voltage (V_{ref} = 20 mV, V_{inS} = 5.0 V)	V_{CMF}	–	±2.5	–	–	±2.5	–	V
Propagation Delay Time, Differential Input to Logic "1" Output (V_{ref} = 20 mV)	t_{PLHD}	–	20	40	–	20	40	ns
Propagation Delay Time, Differential Input to Logic "0" Output (V_{ref} = 20 mV)	t_{PHLD}	–	28	–	–	28	–	ns
Propagation Delay Time, Strobe Input to Logic "1" Output (V_{ref} = 20 mV)	t_{PHLS}	–	10	30	–	10	30	ns
Propagation Delay Time, Strobe Input to Logic "0" Output (V_{ref} = 20 mV)	t_{PHLS}	–	20	–	–	20	–	ns
Overload Recovery Time, Differential Input	t_{RD}	–	10	–	–	10	–	ns
Overload Recovery Time, Common-Mode Input	t_{RCM}	–	5.0	–	–	5.0	–	ns
Minimum Cycle Time	t(min)	–	200	–	–	200	–	ns

② Positive current is defined as current into the referenced pin.

③ Pin 1 to have ≥100 pF capacitor connected to ground.

④ Each test point to have ≤15 pF capacitive load to ground.

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ORDERING INFORMATION

Device	Temperature Range	Package
MC5534L	−55°C to +125°C	Ceramic DIP
MC5535L	−55°C to +125°C	Ceramic DIP
MC7534L	0°C to +70°C	Ceramic DIP
MC7534P	0°C to +70°C	Plastic DIP
MC7535L	0°C to +70°C	Ceramic DIP
MC7535P	0°C to +70°C	Plastic DIP

MC7534, MC5534
MC7535, MC5535

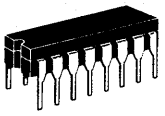
DUAL SENSE AMPLIFIERS WITH INVERTED OUTPUTS

This dual sense amplifier is designed for use with high-speed memory systems. Low level pulses originating in the memory are converted to logic levels compatible with MDTL and MTTL circuits. These circuits are identical to the MC7524 except that an additional stage has been added to each output gate to provide an inverted output.

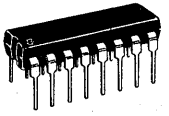
- Adjustable Threshold Voltage Levels
- High-Speed, Fast Recovery Time
- Time and Amplitude Signal Discrimination
- High dc Logic Noise Margin
  1.0 Volt typ
- Good Fan-Out Capability
- Independent Strobing
- Separate Logic Outputs
- Normally High Outputs Accomodate the Wired-OR of Several Sense Amplifiers

DUAL HIGH-SPEED SENSE AMPLIFIER WITH INVERTED OUTPUTS

SILICON MONOLITHIC INTEGRATED CIRCUIT

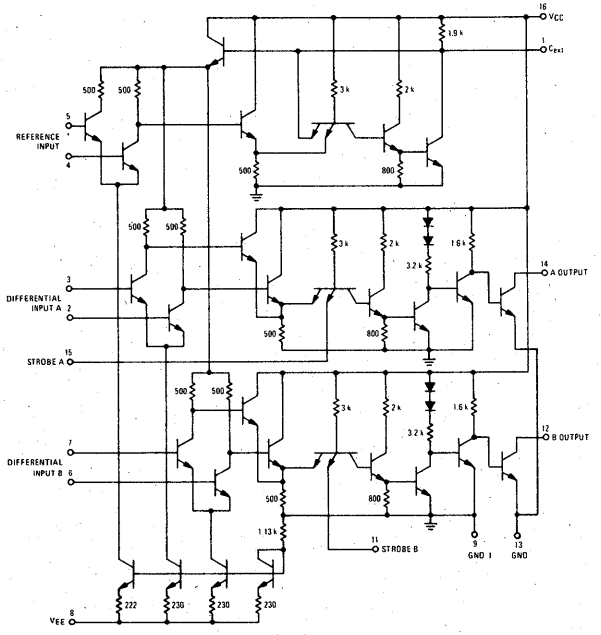


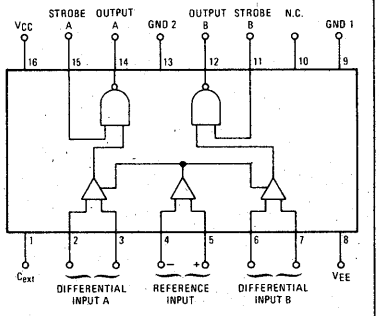
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

SCHEMATIC DIAGRAM





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DS 9225

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Units
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Vdc Vdc
Differential Input Voltages	V_{in} or V_{ref}	±5.0	Vdc
Power Dissipation Derate above T_A = +25°C	P_D	575 3.85	mW mW/°C
Operating Ambient Temperature Range MC5534, MC5535 MC7534, MC7535	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V ±5%, V_{EE} = -5.0 V ±5%, T_A = T_{low}# to T_{high}# unless otherwise noted.)

Characteristic		Symbol	MC5534 ① # MC5535 Min	MC5534 ① # MC5535 Typ	MC5534 ① # MC5535 Max	MC7534# MC7535 Min	MC7534# MC7535 Typ	MC7534# MC7535 Max	Unit
Differential Input Threshold Voltage (V_{inS} = +5.0 V, V_{ID} = ±V_{th})		V_{th}							mW
(V_{ref} = 15 mV, V_L = +5.25 V, I_L < 250 μA)	MC5534, MC7534		10	15	–	11	15	–	
	MC5535, MC7535		8.0	–	–	8.0	–	–	
(V_{ref} = 40 mV, V_L = +5.25 V, I_L < 250 μA)	MC5534, MC7534		35	40	–	36	40	–	
	MC5535, MC7535		33	–	–	33	–	–	
(V_{ref} = 15 mV, I_L = 20 mA, V_O = < 0.4 V)	MC5534, MC7534		–	15	20	–	15	19	
	MC5535, MC7535		–	–	22	–	–	22	
(V_{ref} = 40 mV, I_L = 200 mA, V_O = < 0.4 V)	MC5534, MC7534		–	40	45	–	40	44	
	MC5535, MC7535		–	–	47	–	–	47	
Differential Reference Input Bias Current (V_{ID} = V_{ref} = 0 V, V_{inS} = +5.25 V, V_S = ±5.25 V)		I_{IB}	–	30	100	–	30	75	μA
Differential Input Offset Current (V_{ID} = V_{ref} = 0 V, V_{inS} = +5.25 V, V_S = ±5.25 V)		I_{IOD}	–	0.5	–	–	0.5	–	μA
Input Voltage, Low Logic State (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 0.8 V, V_L = +5.25 V, V_S = ±4.75 V, I_L = < 250 μA)		V_{IL}	–	–	0.8	–	–	0.8	V
Input Voltage, High Logic State (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 2.0 V, I_L = 20 mA, V_S = ±4.75 V, V_O = < 0.4 V)		V_{IH}	2.0	–	–	2.0	–	–	V
Input Current, Low Logic State (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 0.4 V, V_S = ±5.25 V)		I_{IL}	–	-1.0	-1.6	–	-1.0	-1.6	mA
Input Current, High Logic State (V_{ID} = 0 V, V_{ref} = 20 mV, V_{inS} = 2.4 V, V_S = ±5.25 V)	MC5534, MC5535	I_{IH}	–	5.0	40	–	–	–	μA
	MC7534, MC7535		–	–	–	–	0.02	1.0	mA
Output Voltage, Low Logic State (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 2.0 V, I_L = 20 mA, V_S = ±4.75 V)		V_{OL}	–	0.25	0.40	–	0.25	0.40	V
Output Leakage Current (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 0.8 V, V_L = 5.25 V, V_S = ±4.75 V)		I_{OH}	–	0.01	250	–	0.01	250	μA
V_{CC} Supply Current (V_{ID} = V_{inS} = 0 V, V_{ref} = 20 mV, V_S = ±5.25 V)		I_{CC}	–	28	38	–	28	38	mA
V_{EE} Supply Current (V_{ID} = V_{inS} = 0 V, V_{ref} = 20 mV, V_S = ±5.25 V)		I_{EE}	–	-13	-18	–	-13	-18	mA

① For 0°C ≤ T_A ≤ 70°C operation, electrical characteristics for MC5534 and MC5535 are guaranteed the same as MC7534 and MC7535 respectively.

② Positive current is defined as current into the referenced pin.

③ Pin 1 to have ≥100 pF capacitor connected to ground.

T_{low} = -55°C for MC5534, MC5535, 0°C for MC7534, MC7535
T_{high} = +125°C for MC5534, MC5535, +70°C for MC7534, MC7535

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V ±5%, V_{EE} = -5.0 V ±5%, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC5534 MC5535 Min	MC5534 MC5535 Typ	MC5534 MC5535 Max	MC7534 MC7535 Min	MC7534 MC7535 Typ	MC7534 MC7535 Max	Unit
AC Common-Mode Input Firing Voltage (V_{ref} = 20 mV, V_{inS} = 5.0 V)	V_{CMF}	–	±2.5	–	–	±2.5	–	V
Propagation Delay Time, Differential Input to Logic "1" Output (V_{ref} = 20 mV)	t_{PLHD}	–	24	–	–	24	–	ns
Propagation Delay Time, Differential Input to Logic "0" Output (V_{ref} = 20 mV)	t_{PHLD}	–	20	40	–	20	40	ns
Propagation Delay Time, Strobe Input to Logic "1" Output (V_{ref} = 20 mV)	t_{PLHS}	–	16	–	–	16	–	ns
Propagation Delay Time, Strobe Input to Logic "0" Output (V_{ref} = 20 mV)	t_{PHLS}	–	10	30	–	10	30	ns
Overload Recovery Time, Differential Input	t_{RD}	–	10	–	–	10	–	ns
Overload Recovery Time, Common-Mode Input	t_{RCM}	–	5.0	–	–	5.0	–	ns
Minimum Cycle Time	t(min)	–	200	–	–	200	–	ns

ORDERING INFORMATION

Device	Temperature Range	Package
MC5538L	−55°C to +125°C	Ceramic DIP
MC5539L	−55°C to +125°C	Ceramic DIP
MC7538L	0°C to +70°C	Ceramic DIP
MC7538P	0°C to +70°C	Plastic DIP
MC7539L	0°C to +70°C	Ceramic DIP
MC7539P	0°C to +70°C	Plastic DIP

MC7538, MC5538
MC7539, MC5539

DUAL SENSE AMPLIFIERS WITH PREAMPLIFIER TEST POINTS AND INVERTED OUTPUTS

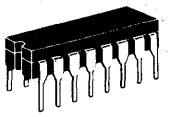
This dual sense amplifier is designed for use with high-speed memory systems. Low level pulses originating in the memory are converted to logic levels compatible with MDTL and MTTL circuits. These devices are identical to MC5528/MC7528 with the exception of the inverted outputs.

- Adjustable Threshold Voltage Levels
- High-Speed, Fast Recovery Time
- Time and Amplitude Signal Discrimination
- High dc Logic Noise Margin
  1.0 Volt typ
- Good Fan-Out Capability
- Independent Strobing
- Separate Logic Outputs
- Test Points Available for Strobe Timing
- Inverted Outputs to Accomodate Wired-OR Outputs of Several Sense Amplifiers

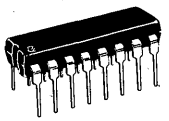
DUAL HIGH-SPEED SENSE AMPLIFIER

WITH
PREAMPLIFIER TEST POINTS
AND
INVERTED OUTPUTS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

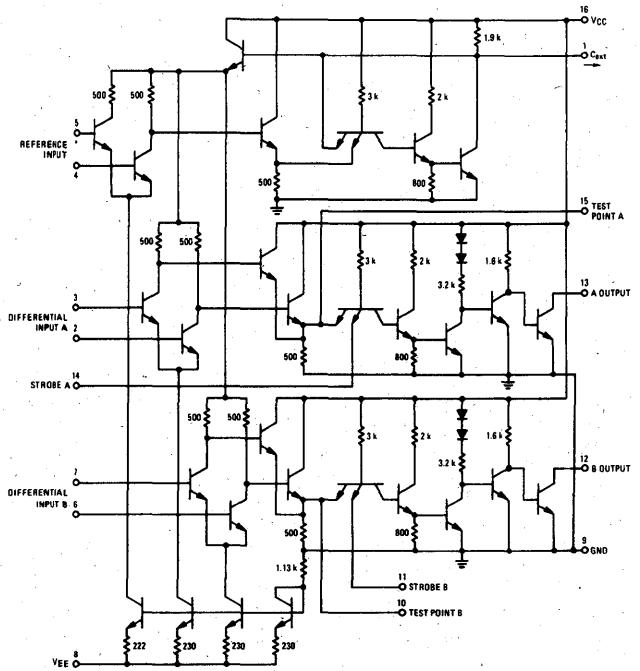


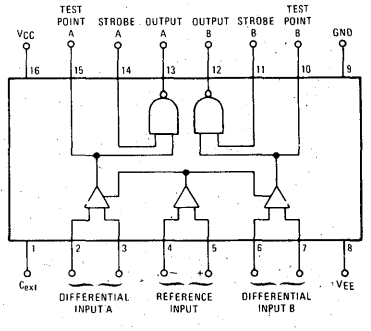
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648
(MC7538 and MC7539 only)

SCHEMATIC DIAGRAM





MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Units
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Vdc Vdc
Differential Input Voltages	V_{in} or V_{ref}	±5.0	Vdc
Power Dissipation Derate above T_A = +25°C	P_D	575 3.85	mW mW/°C
Operating Ambient Temperature Range MC5538, MC5539 MC7538, MC7539	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V ±5%, V_{EE} = -5.0 V ±5%, T_A = T_{low}# to T_{high}# unless otherwise noted.)

Characteristic	Symbol	MC5538 ① # MC5539 Min	MC5538 ① # MC5539 Typ	MC5538 ① # MC5539 Max	MC7538 # MC7539 Min	MC7538 # MC7539 Typ	MC7538 # MC7539 Max	Unit
Differential Input Threshold Voltage (V_{inS} = +5.0 V, V_{ID} = ±V_{th})	V_{th}							mV
(V_{ref} = 15 mV, V_L = +5.25 V, I_L < 250 μA) MC5538, MC7538		10	15	–	11	15	–	
MC5539, MC7539		8.0	–	–	8.0	–	–	
(V_{ref} = 40 mV, V_L = +5.25 V, I_L < 250 μA) MC5538, MC7538		35	40	–	36	40	–	
MC5539, MC7539		33	–	–	33	–	–	
(V_{ref} = 15 mV, I_L = 120 mA, V_L < 0.4 V) MC5538, MC7538		–	15	20	–	15	19	
MC5539, MC7539		–	–	22	–	–	22	
(V_{ref} = 40 mV, I_L = +20 mA, V_L < 0.4 V) MC5538, MC7538		–	40	45	–	40	44	
MC5539, MC7539		–	–	47	–	–	47	
Differential and Reference Input Bias Current (V_{ID} = V_{ref} = 0 V, V_{inS} = +5.25 V, V_S = ±5.25 V)	I_{IB}	–	30	100	–	30	75	μA
Differential Input Offset Current (V_{ID} = V_{ref} = 0 V, V_{inS} = +5.25 V, V_S = ±5.25 V)	I_{IOD}	–	0.5	–	–	0.5	–	μA
Input Voltage, High Logic State (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = +2.0 V, I_L = 20 mA; V_S = ±4.75 V, V_L < 0.4 V)	V_{IH}	2.0	–	–	2.0	–	–	V
Input Voltage, Low Logic State (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = +0.8 V, V_L = +5.25 V, V_S = ±4.75 V, I_L < 250 μA)	V_{IL}	–	–	0.8	–	–	0.8	V
Input Current, High Logic State (V_{ID} = 0 V, V_{ref} = 20 mV, V_{inS} = 2.4 V, V_S = ±5.25 V) MC5538, MC5539	I_{IH}	–	5.0	40	–	–	–	μA
(V_{ID} = 0 V, V_{ref} = 20 mV, V_{inS} = +5.25 V, MC7538, MC7539		–	–	–	–	0.02	1.0	mA
V_S = ±5.25 V)								
Input Current, Low Logic State (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 0.4 V, V_S = ±5.25 V)	I_{IL}	–	-1.0	-1.6	–	-1.0	-1.6	mA
Output Voltage, Low Logic State (V_{ID} = 40 mV, V_{ref} = 20 mV, V_{inS} = 2.0 V, I_L = 20 mA, V_S = ±4.75 V)	V_{OH}	–	0.25	0.40	–	0.25	0.40	V
V_{CC} Supply Current (V_{ID} = V_{inS} = 0 V, V_{ref} = 20 mV, V_S = ±5.25 V)	I_{CC}	–	28	38	–	28	38	mA
V_{EE} Supply Current (V_{ID} = V_{inS} = 0 V, V_S = ±5.25 V)	I_{EE}	–	-13	-18	–	-13	-18	mA

① For 0°C ≤ T_A ≤ 70°C operation, electrical characteristics for MC5538 and MC5539 are guaranteed the same as MC7538 and MC7539 respectively.

T_{low} = -55°C for MC5538, MC5539; 0°C for MC7538, MC7539
T_{high} = +125°C for MC5538, MC5539; +70°C for MC7538, MC7539

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V ±5%, V_{EE} = -5.0 V ±5%, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC5538 MC5539 Min	MC5538 MC5539 Typ	MC5538 MC5539 Max	MC7538 MC7539 Min	MC7538 MC7539 Typ	MC7538 MC7539 Max	Unit
AC Common-Mode Input Firing Voltage (V_{ref} = 20 mV, V_{inS} = 5.0 V)	V_{CMF}	–	±2.5	–	–	±2.5	–	V
Propagation Delay Time, Differential Input to Logic "1" Output (V_{ref} = 20 mV)	t_{PLHD}	–	24	–	–	24	–	ns
Propagation Delay Time, Differential Input to Logic "0" Output (V_{ref} = 20 mV)	t_{PHLD}	–	28	40	–	20	40	ns
Propagation Delay Time, Strobe Input to Logic "1" Output (V_{ref} = 20 mV)	t_{PHLS}	–	16	–	–	16	–	ns
Propagation Delay Time, Strobe Input to Logic "0" Output (V_{ref} = 20 mV)	t_{PHLS}	–	10	30	–	10	30	ns
Overload Recovery Time, Differential Input	t_{RD}	–	10	–	–	10	–	ns
Overload Recovery Time, Common-Mode Input	t_{RCM}	–	5.0	–	–	5.0	–	ns
Minimum Cycle Time	*t(min)*	–	200	–	–	200	–	ns

② Positive current is defined as current into the referenced pin.

③ Pin 1 to have ≥100 pF capacitor connected to ground.

④ Each test point to have ≤15 pF capacitive load to ground.

ORDERING INFORMATION

Device	Temperature Range	Package
MC8T13L	0°C to +75°C	Ceramic DIP
MC8T13P	0°C to +75°C	Plastic DIP
MC8T23L	0°C to +75°C	Ceramic DIP
MC8T23P	0°C to +75°C	Plastic DIP

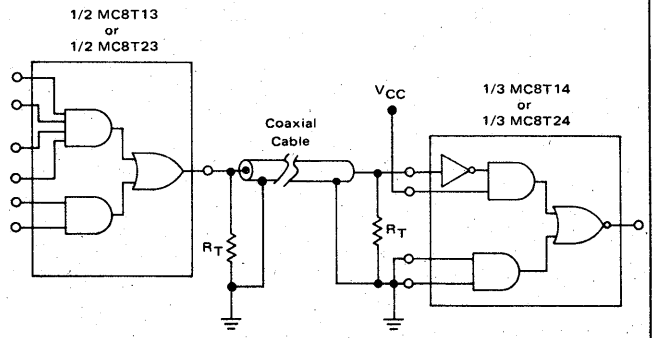
MC8T13
MC8T23

DUAL LINE DRIVERS

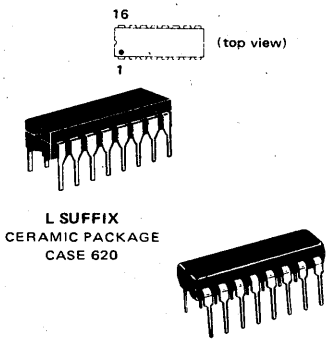
The MC8T13 and MC8T23 are designed to drive transmission lines with impedances of 50 Ω to 500 Ω. The MC8T23 specifically meets all of the input/output requirements of the IBM System 360/System 370 specifications (IBM Specification GA 22-6974-0).

- High Output Drive Capability –
  I_O = -75 mA (Min) @ V_O = 2.4 V – MC8T13
  I_O = -59.3 mA (Min) @ V_O = 3.11 V – MC8T23
- High Speed Operation –
  $t_{PLH} = t_{PHL}$ = 20 ns (Max) with 50 Ω Load
- MTTL and MDTL Compatible Inputs
- Uncommitted Emitter Output Structures Permit Party-Line Operation
- Designed to Operate with MC8T14 or MC8T24 Line Receivers
- Outputs are Short-Circuit Protected
- Equivalent to SN75121 and SN75123 Respectively.

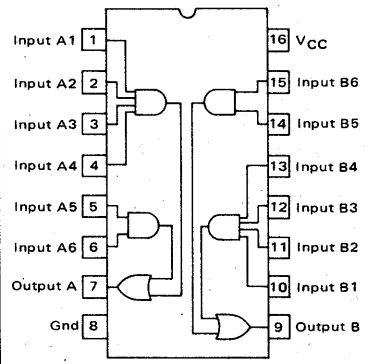
TYPICAL APPLICATION



DUAL LINE DRIVERS
SILICON MONOLITHIC INTEGRATED CIRCUIT



PIN CONNECTIONS



TRUTH TABLE

Inputs						Output
1	2	3	4	5	6	
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Combinations						L

H = High Logic State
L = Low Logic State
X = Irrelevant

5

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Output Voltage	V_O	7.0	Vdc
Power Dissipation @ T_A = +25°C Derate above 25°C	P_D	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 4.75 V ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 75°C)

Characteristics	Symbol	MC8T13 Min	MC8T13 Typ	MC8T13 Max	MC8T23 Min	MC8T23 Typ	MC8T23 Max	Unit
Input Voltage — Low Logic State	V_{IL}	–	–	0.8	–	–	0.8	V
Input Voltage — High Logic State	V_{IH}	2.0	–	–	2.0	–	–	V
Input Current — Low Logic State (V_{IL} = 0.4 V)	I_{IL}	-0.1	–	-1.6	-0.1	–	-1.6	mA
Input Current — High Logic State (V_{IH} = 4.5 V)	I_{IH1}	–	–	40	–	–	40	μA
(V_{IH} = 5.5 V, V_{CC} = 5.0 V)	I_{IH2}	–	–	10	–	–	10	mA
Input Clamp Voltage (I_I = -12 mA, V_{CC} = 5.0 V)	$V_{I(clamp)}$	–	–	-1.5	–	–	-1.5	V
Output Voltage — High Logic State (V_{IH} = 2.0 V, I_{OH} = -75 mA)	V_{OH1}	2.4	–	–	–	–	–	V
(V_{CC} = 5.0 V, V_{IH} = 2.0 V, I_{OH} = -59.3 mA) (T_A = 25°C)	V_{OH2}	– –	– –	– –	2.9 3.11	– –	– –	V
Output Current — High Logic State (V_{IH} = 4.5 V, V_{CC} = 5.0 V, V_O = 2.0 V, T_A = 25°C)	I_{OH}	-100	–	-250	-100	–	-250	mA
Output Current — Low Logic State (V_{IL} = 0.8 V, V_O = 0.4 V)	I_{OL1}	–	–	-800	–	–	–	μA
(V_{IL} = 0.8 V, V_O = 0.15 V)	I_{OL2}	–	–	–	–	–	-240	μA
Output Reverse Leakage Current — Low Logic State (V_{IL} = 0 V, V_O = 3.0 V)	I_{OR1}	–	–	80	–	–	–	μA
(V_{IL} = 0 V, V_O = 3.0 V, V_{CC} = 0 V)	I_{OR2}	–	–	500	–	–	40	μA
Output Short-Circuit Current (V_{IH} = 4.5 V, V_{CC} = 5.0 V, V_O = 0 V, T_A = 25°C)	I_{OS}	–	–	-30	–	–	-30	mA
Power Supply Currents (I_O = 0 mA) Outputs — Low Logic State, V_{IL} = 0.8 V	I_{CCL}	–	–	60	–	–	60	mA
Outputs — High Logic State, V_{IH} = 2.0 V	I_{CCH}	–	–	28	–	–	28	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.) Figure 1

Characteristic	Symbol	MC8T13 Min	MC8T13 Typ	MC8T13 Max	MC8T23 Min	MC8T23 Typ	MC8T23 Max	Unit
Propagation Delay Time — Low to High Level Output	t_{PLH}							ns
(R_L = 37 Ω, C_L = 15 pF)		–	11	20	–	–	–	
(R_L = 37 Ω, C_L = 1000 pF)		–	22	50	–	–	–	
(R_L = 50 Ω, C_L = 15 pF)		–	–	–	–	12	20	
(R_L = 50 Ω, C_L = 100 pF)		–	–	–	–	20	35	
Propagation Delay Time — High to Low Level Output	t_{PHL}							ns
(R_L = 37 Ω, C_L = 15 pF)		–	8.0	20	–	–	–	
(R_L = 37 Ω, C_L = 1000 pF)		–	20	50	–	–	–	
(R_L = 50 Ω, C_L = 15 pF)		–	–	–	–	12	20	
(R_L = 50 Ω, C_L = 100 pF)		–	–	–	–	15	25	

FIGURE 1 – SWITCHING TEST CIRCUIT AND WAVEFORMS

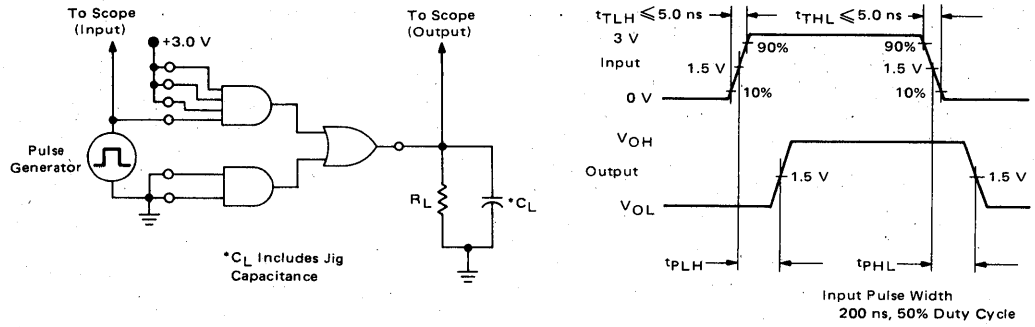


FIGURE 2 – REPRESENTATIVE SCHEMATIC DIAGRAM
(1/2 Shown)

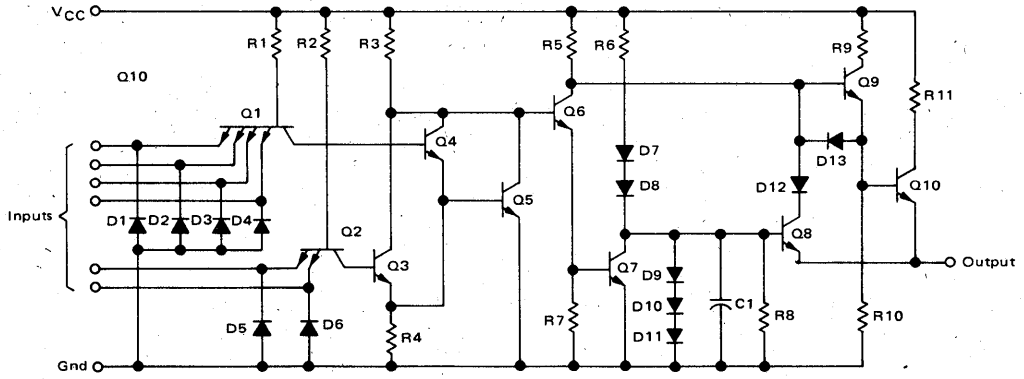
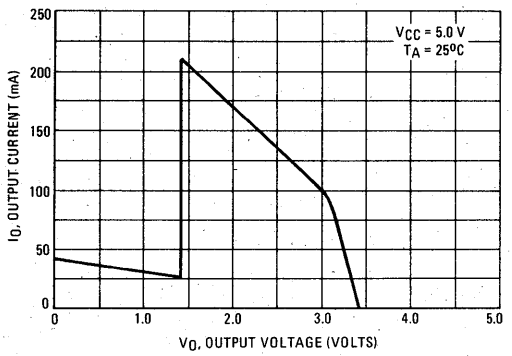


FIGURE 3 – TYPICAL OUTPUT CURRENT
versus OUTPUT VOLTAGE



ORDERING INFORMATION

Device	Temperature Range	Package
MC8T14L	0°C to +75°C	Ceramic DIP
MC8T14P	0°C to +75°C	Plastic DIP
MC8T24L	0°C to +75°C	Ceramic DIP
MC8T24P	0°C to +75°C	Plastic DIP

MC8T14
MC8T24

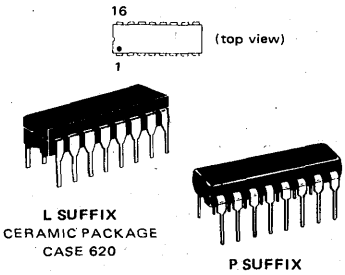
TRIPLE LINE RECEIVERS WITH HYSTERESIS

. . . specifically designed to meet the input/output specifications for IBM 360/370 Systems (IBM specification GA 22-6974-0). Each receiver incorporates hysteresis to provide high noise immunity and also high input impedance to minimize loading on the related driver.

- Each Channel Can Be Independently Strobed
- High Speed – $t_{PLH} = t_{PHL} = 20$ ns
- Input Gating Provided on Each Line
- Operates on a Single +5.0 V Power Supply
- Fully Compatible with MTTL or MDTL Logic Systems
- Input Hysteresis Results in High Noise Immunity

TRIPLE LINE RECEIVERS WITH HYSTERESIS

SILICON MONOLITHIC INTEGRATED CIRCUIT

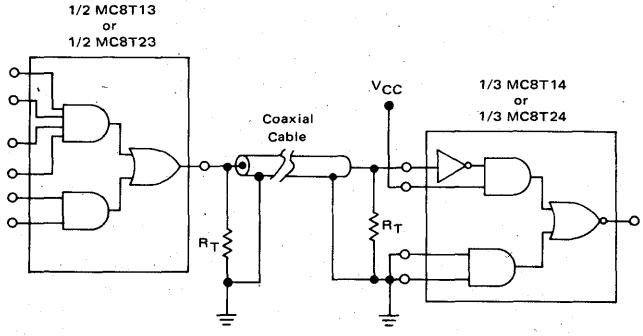


L SUFFIX
CERAMIC PACKAGE
CASE 620

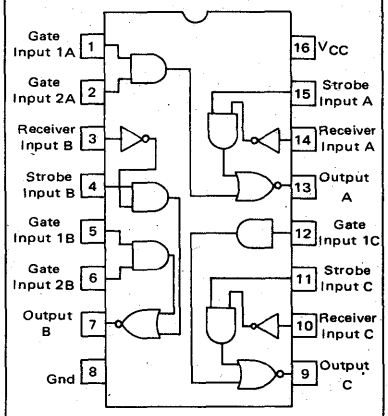
P SUFFIX
PLASTIC PACKAGE
CASE 648

5

TYPICAL APPLICATION



PIN CONNECTIONS



TRUTH TABLE

Inputs				Output
Receiver	Strobe	Gate 1	Gate 2	
X	X	H	H	L
L	H	X	X	L
H	X	L	X	H
X	L	L	X	H
H	X	X	L	H
X	L	X	L	H

Where:
L = Low Logic State
H = High Logic State
X = Don't Care

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Receiver Input Voltage (V_{CC} = 0)	$V_{I(R)}$	7.0 6.0	Vdc
Strobe or Gate Input Voltage	$V_{I(S) \text{ or } (G)}$	5.5	Vdc
Output Voltage	V_O	7.0	Vdc
Output Current	I_O	±100	mA
Power Dissipation (Package Limitation) Ceramic Package Derate above 25°C	P_D	 1000 6.7	 mW mW/°C
Plastic Package Derate above 25°C		830 6.7	mW mW/°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 4.75 ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 75°C)

Characteristic	Symbol	MC8T14 Min	MC8T14 Typ	MC8T14 Max	MC8T24 Min	MC8T24 Typ	MC8T24 Max	Unit
Gate or Strobe Input Voltage – High Logic State	$V_{IH(G) \text{ or } (S)}$	2.0	–	–	2.0	–	–	V
Gate or Strobe Input Voltage – Low Logic State	$V_{IL(G) \text{ or } (S)}$	–	–	0.8	–	–	0.8	V
Receiver Input Voltage – High Logic State	$V_{IH(R)}$	2.0	–	–	1.7	–	–	Vdc
Receiver Input Voltage – Low Logic State	$V_{IL(R)}$	–	–	0.8	–	–	0.7	Vdc
Receiver Input Hysteresis (1) (V_{CC} = 5.0 V, T_A = 25°C, $V_{IL(G)}$ = 0, $V_{IH(S)}$ = 4.5 V)	$V_{H(R)}$	0.3	0.5	–	0.2	0.4	–	V
Input Clamp Voltage (V_{CC} = 5.0 V, T_A = 25°C, I_I = -12 mA) (Strobe or Gate Inputs)	$V_{IC(G) \text{ or } (S)}$	–	–	1.5	–	–	1.5	V
Input Breakdown Voltage (V_{CC} = 5.0 V, I_I = 10 mA) (Strobe or Gate Inputs)	$V_{I(G) \text{ or } (S)}$	5.5	–	–	5.5	–	–	V
Receiver Input Current – High Logic State ($V_{IH(R)}$ = 3.8 V) ($V_{IH(R)}$ = 3.11 V) ($V_{IH(R)}$ = 7.0 V) ($V_{IH(R)}$ = 6.0 V, V_{CC} = 0 V)	$I_{IH(R)}$	 – – – –	 – – – –	 0.17 – – –	 – – – –	 – – – –	 – 0.17 5.0 5.0	mA
Gate or Strobe Input Current – High Logic State ($V_{IH(S)}$ = 4.5 V, $V_{IH(R)}$ = 3.11 V) ($V_{IH(G)}$ = 4.5 V)	$I_{IH(G) \text{ or } (S)}$	 – –	 – –	 40 40	 – –	 – –	 40 40	μA
Gate or Strobe Input Current – Low Logic State ($V_{IL(G) \text{ or } (S)}$ = 0.4 V, $V_{IL(R)}$ = 0 V)	$I_{IL(G) \text{ or } (S)}$	-0.1	–	-1.6	-0.1	–	-1.6	mA
Output Voltage – High Logic State ($V_{IH(R)}$ = 2.0 V, $V_{IH(S)}$ = 2.0 V, $V_{IL(G)}$ = 0.8 V, I_{OH} = -800 μA) ($V_{IH(R)}$ = 0.8 V, $V_{IL(S)}$ = 0.8 V, $V_{IL(G)}$ = 0.8 V, I_{OH} = -800 μA) ($V_{IH(R)}$ = 1.7 V, $V_{IH(S)}$ = 2.0 V, $V_{IL(G)}$ = 0.8 V, I_{OH} = -800 μA) ($V_{IH(R)}$ = 0.7 V, $V_{IL(S)}$ = 0.8 V, $V_{IL(G)}$ = 0.8 V, I_{OH} = -800 μA)	V_{OH}	 2.6 2.6 – –	 3.5 3.5 – –	 – – – –	 – – 2.6 2.6	 – – 3.4 3.4	 – – – –	V
Output Voltage – Low Logic State ($V_{IL(R)}$ = 0.8 V, $V_{IH(S)}$ = 2.0 V, $V_{IL(G)}$ = 0.8 V, I_{OL} = 16 mA) ($V_{IL(R)}$ = 0.8 V, $V_{IL(S)}$ = 0.8 V, $V_{IH(G)}$ = 2.0 V, I_{OL} = 16 mA) ($V_{IL(R)}$ = 0.7 V, $V_{IH(S)}$ = 2.0 V, $V_{IL(G)}$ = 0.8 V, I_{OL} = 16 mA) ($V_{IL(R)}$ = 0.7 V, $V_{IL(S)}$ = 0.8 V, $V_{IH(G)}$ = 2.0 V, I_{OL} = 16 mA)	V_{OL}	 – – – –	 – – – –	 0.4 0.4 – –	 – – – –	 – – – –	 – – 0.4 0.4	V
Output Short-Circuit Current (2) ($V_{IH(R)}$ = 3.8 V, $V_{IL(G)}$ = 0 V, $V_{IL(S)}$ = 0, V_{CC} = 5.0 V, T_A = 25°C) ($V_{IH(R)}$ = 3.11 V, $V_{IL(G)}$ = 0 V, $V_{IL(S)}$ = 0 V, V_{CC} = 5.0 V, T_A = 25°C)	I_{OS}	 -50 –	 – –	 -100 –	 – -50	 – –	 – -100	mA
Power Supply Current (V_{CC} = 5.25 V, T_A = 25°C)	I_{CC}	–	60	72	–	60	72	mA

(1) The Input Hysteresis is defined as the difference the input voltage at which the output begins to go from the high logic state to the low logic state and the input voltage which causes the output to begin to go from the low logic state to the high logic state.

(2) Only one output may be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Parameter	Symbol	MC8T14, MC8T24			Unit
		Min	Typ	Max	
Propagation Delay Time – Receiver Input to High Logic State Output	$t_{PLH(R)}$	–	20	30	ns
Propagation Delay Time Receiver Input to Low Logic State Output	$t_{PHL(R)}$	–	20	30	ns
Propagation Delay Time Strobe Input to High Logic State Output	$t_{PLH(S)}$	–	–	–	ns
Propagation Delay Time Strobe Input to Low Logic State Output	$t_{PHL(S)}$	–	–	–	ns
Propagation Delay Time Gate Input to High Logic State Output	$t_{PLH(G)}$	–	–	–	ns
Propagation Delay Time Gate Input to Low Logic State Output	$t_{PHL(G)}$	–	–	–	ns

FIGURE 1 – RECEIVER PROPAGATION DELAY TIMES $t_{PLH(R)}$ and $t_{PHL(R)}$ TEST CIRCUIT AND WAVEFORMS

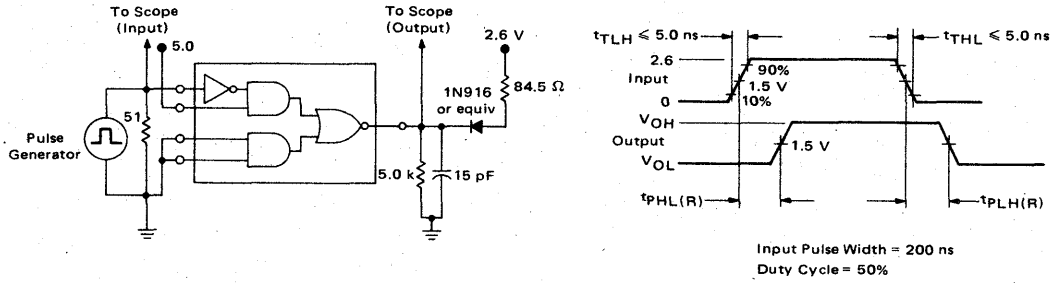


FIGURE 2 – GATE AND STROBE PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS

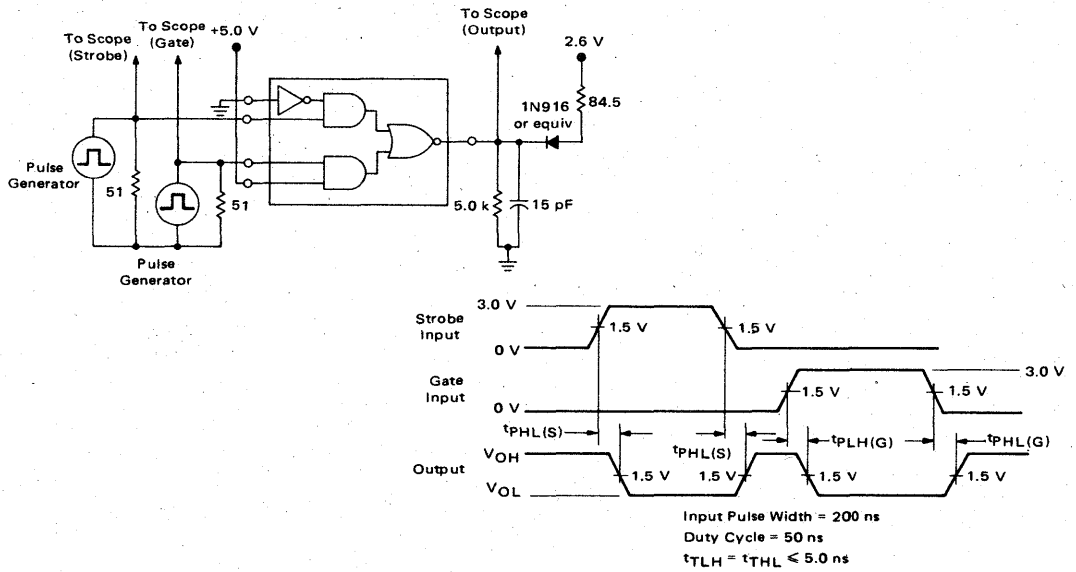


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FIGURE 3 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTIC

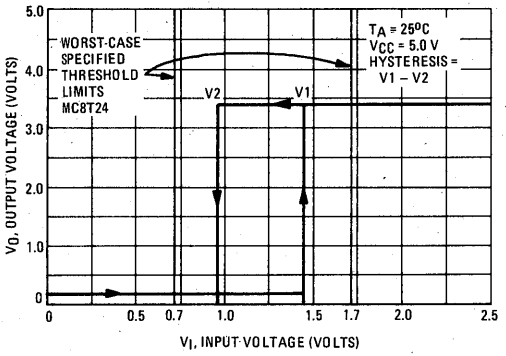
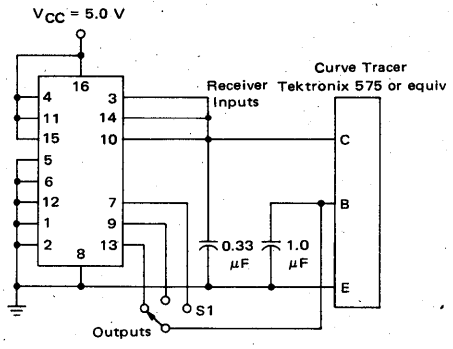
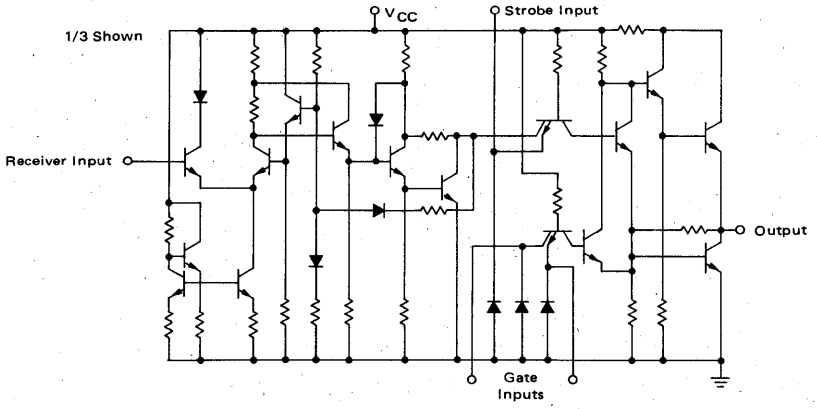


FIGURE 4 – HYSTERESIS TEST CIRCUIT



REPRESENTATIVE CIRCUIT SCHEMATIC



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ORDERING INFORMATION

Device	Temperature Range	Package
MC55107L	−55°C to +125°C	Ceramic DIP
MC55108L	−55°C to +125°C	Ceramic DIP
MC75107L	0°C to +70°C	Ceramic DIP
MC75107P	0°C to +70°C	Plastic DIP
MC75108L	0°C to +70°C	Ceramic DIP
MC75108P	0°C to +70°C	Plastic DIP

MC75107 MC55107
MC75108 MC55108

DUAL LINE RECEIVERS

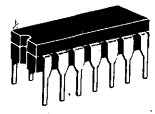
The MC55107/MC75107 and MC55108/MC75108 are MTTL compatible dual line receivers featuring independent channels with common voltage supply and ground terminals. The MC55107/MC75107 circuit features an active pull-up (totem-pole) output. The MC55108/MC75108 circuit features an open-collector output configuration that permits the Wired-OR logic connection with similar outputs (such as the MC5401/MC7401 MTTL gate or additional MC55108/MC75108 receivers). Thus a level of logic is implemented without extra delay.

The MC55107/MC75107 and MC55108/MC75108 circuits are designed to detect input signals of greater than 25 millivolts amplitude and convert the polarity of the signal into appropriate MTTL compatible output logic levels.

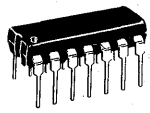
- High Common-Mode Rejection Ratio
- High Input Impedance
- High Input Sensitivity
- Differential Input Common-Mode Voltage Range of ±3.0 V
- Differential Input Common-Mode Voltage of More Than ±15 V Using External Attenuator
- Strobe Inputs for Receiver Selection
- Gate Inputs for Logic Versatility
- MTTL or MDTL Drive Capability
- High DC Noise Margins

DUAL LINE RECEIVERS

SILICON MONOLITHIC INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



P SUFFIX
PLASTIC PACKAGE
CASE 646

(MC75107 MC75108 only)

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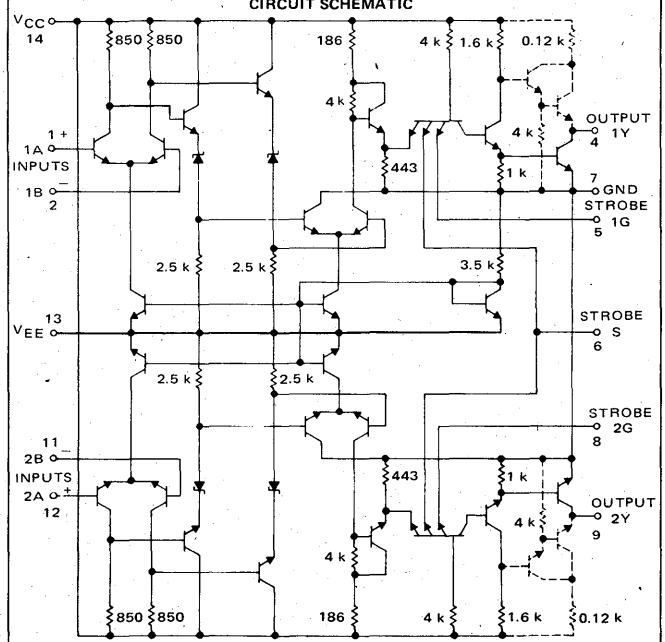
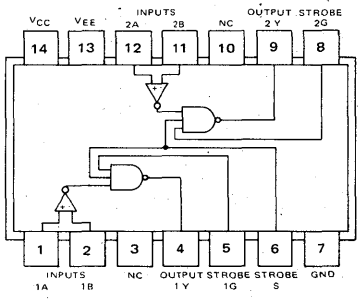
CIRCUIT SCHEMATIC



Components shown with dashed lines are applicable to the MC55107 and MC75107 only.



TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 25$ mV	L or H	L or H	H
	L or H	L	H
−25 mV ≤ V_{ID} ≤ 25 mV	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

MAXIMUM RATINGS ($T_A = T_{low}$* to T_{high}* unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+7.0 -7.0	Vdc
Differential-Mode Input Signal Voltage Range	V_{ID}	±6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Power Dissipation (Package Limitation) Plastic and Ceramic Dual-In-Line Packages Derate above T_A = +25°C	P_D	 625 3.85	 mW mW/°C
Operating Ambient Temperature Range MC55107, MC55108 MC75107, MC75108	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	MC55107, MC55108 Min	Typ	Max	MC75107, MC75108 Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.5 -4.5	+5.0 -5.0	+5.5 -5.5	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Vdc
Output Sink Current	I_{OS}	–	–	-16	–	–	-16	mA
Differential-Mode Input Voltage Range	V_{IDR}	-5.0	–	+5.0	-5.0	–	±5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	-3.0	–	+3.0	-3.0	–	+3.0	Vdc
Input Voltage Range, any differential input to ground	V_{IR}	-5.0	–	+3.0	-5.0	–	+3.0	Vdc
Operating Temperature Range	T_A	-55	–	+125	0	–	+70	°C

DEFINITIONS OF INPUT LOGIC LEVELS

Characteristic	Symbol	Test Fig.	Min	Max	Unit
High-Level Input Voltage (between differential inputs)	V_{IDH}	1	0.025	5.0	Vdc
Low-Level Input Voltage (between differential inputs)	V_{IDL}	1	-5.0†	-0.025	Vdc
High-Level Input Voltage (at strobe inputs)	$V_{IH(S)}$	3	2.0	5.5	Vdc
Low-Level Input Voltage (at strobe inputs)	$V_{IL(S)}$	3	0	0.8	Vdc

†The algebraic convention, where the most positive limit is designated maximum, is used with Low-Level Input Voltage Level (V_{IDL})

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ELECTRICAL CHARACTERISTICS ($T_A = T_{low}$* to T_{high}* unless otherwise noted)

Characteristic	Symbol	Test Fig.	MC55107,MC75107 Min	Typ #	Max	MC55108,MC75108 Min	Typ #	Max	Unit
High-Level Input Current to 1A or 2A Input (V_{CC} = Max, V_{EE} = Max, V_{ID} = 0.5 V, V_{IC} = -3.0 V to +3.0 V) ‡	I_{IH}	2	–	30	75	–	30	75	µA
Low-Level Input Current to 1A or 2A Input (V_{CC} = Max, V_{EE} = Max, V_{ID} = -2.0 V, V_{IC} = -3.0 V to +3.0 V) ‡	I_{IL}	2	–	–	-10	–	–	-10	µA
High-Level Input Current to 1G or 2G Input (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = 2.4 V)‡ (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = V_{CC} Max)‡	I_{IH}	4	– –	– –	40 1.0	– –	– –	40 1.0	µA mA
Low-Level Input Current to 1G or 2G Input (V_{CC} = Max, V_{EE} = Max, $V_{IL(S)}$ = 0.4 V)‡	I_{IL}	4	–	–	-1.6	–	–	-1.6	mA
High-Level Input Current to S Input (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = 2.4 V)‡ (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = V_{CC} Max)‡	I_{IH}	4	– –	– –	80 2.0	– –	– –	80 2.0	µA mA
Low-Level Input Current to S Input (V_{CC} = Max, V_{EE} = Max, $V_{IL(S)}$ = 0.4 V)‡	I_{IL}	4	–	–	-3.2	–	–	-3.2	mA
High-Level Output Voltage (V_{CC} = Min, V_{EE} = Min, I_{load} = -400 µA, V_{IC} = -3.0 V to +3.0 V)‡	V_{OH}	3	2.4	–	–	–	–	–	V
Low-Level Output Voltage (V_{CC} = Min, V_{EE} = Min, I_{sink} = 16 mA V_{IC} = -3.0 V to +3.0 V)‡	V_{OL}	3	–	–	0.4	–	–	0.4	V
High-Level Leakage Current (V_{CC} = Min, V_{EE} = Min, V_{OH} = V_{CC} Max)‡	I_{CEX}	3	–	–	–	–	–	250	µA
Short-Circuit Output Current # # (V_{CC} = Max, V_{EE} = Max)‡	I_{OSC}	5	-18	–	-70	–	–	–	mA
High Logic Level Supply Current from V_{CC} (V_{CC} = Max, V_{EE} = Max, V_{ID} = 25 mV, T_A = +25°C) ‡	I_{CCH}	6	–	18	30	–	18	30	mA
High Logic Level Supply Current from V_{EE} (V_{CC} = Max, V_{EE} = Max, V_{ID} = 25 mV, T_A = +25°C)‡	I_{EEH}	6	0	-8.4	-15	0	8.4	-15	mA

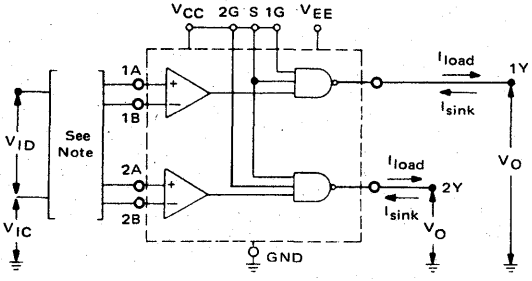
‡For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.
#All typical values are at V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.
#Not more than one output should be shorted at a time.
*T_{low} = 55°C for MC55107 and MC55108, T_{high} = +125°C for MC55107 and MC55108
= 0 for MC75107 and MC75108 = +70°C for MC75107 and MC75108

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C)

Characteristic	Symbol	Test Fig.	MC55107,MC75107 Min	MC55107,MC75107 Typ	MC55107,MC75107 Max	MC55108,MC75108 Min	MC55108,MC75108 Typ	MC55108,MC75108 Max	Unit
Propagation Delay Time, low-to-high level from differential inputs A and B to output (R_L = 390 Ω, C_L = 50 pF) (R_L = 390 Ω, C_L = 15 pF)	$t_{PLH(D)}$	7	 – –	 17 –	 25 –	 – –	 – 19	 – 25	ns
Propagation Delay Time, high-to-low level from differential inputs A and B to output (R_L = 390 Ω, C_L = 50 pF) (R_L = 390 Ω, C_L = 15 pF)	$t_{PHL(D)}$	7	 – –	 17 –	 25 –	 – –	 – 19	 – 25	ns
Propagation Delay Time, low-to-high level, from strobe input G or S to output (R_L = 390 Ω, C_L = 50 pF) (R_L = 390 Ω, C_L = 15 pF)	$t_{PLH(S)}$	7	 – –	 10 –	 15 –	 – –	 – 13	 – 20	ns
Propagation Delay Time, high-to-low level, from strobe input G or S to output (R_L = 390 Ω, C_L = 50 pF) (R_L = 390 Ω, C_L = 15 pF)	$t_{PHL(S)}$	7	 – –	 8.0 –	 15 –	 – –	 – 13	 – 20	ns

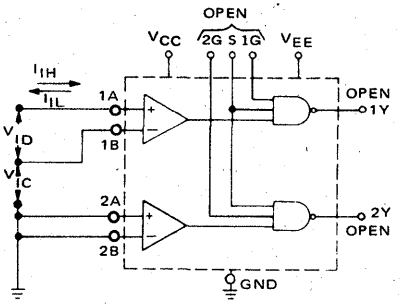
TEST CIRCUITS

FIGURE 1 – V_{IDH} and V_{IDL}



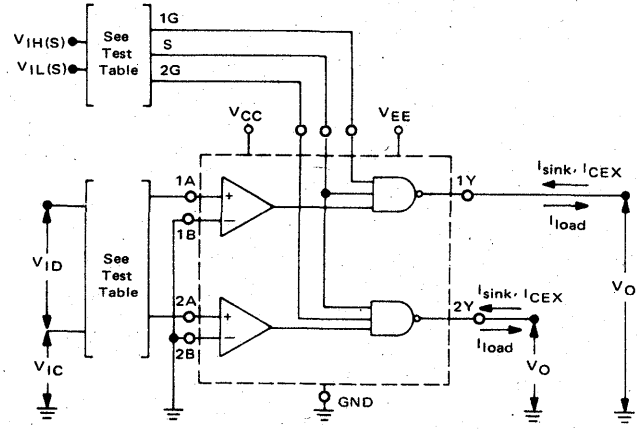
NOTE: When testing one channel, the inputs of the other channel are grounded.

FIGURE 2 – I_{IH} and I_{IL}



NOTE: Each pair of differential inputs is tested separately. The inputs of the other pair are grounded

FIGURE 3 – $V_{IH(S)}$, $V_{IL(S)}$, V_{OH}, V_{OL}, and I_{OH}



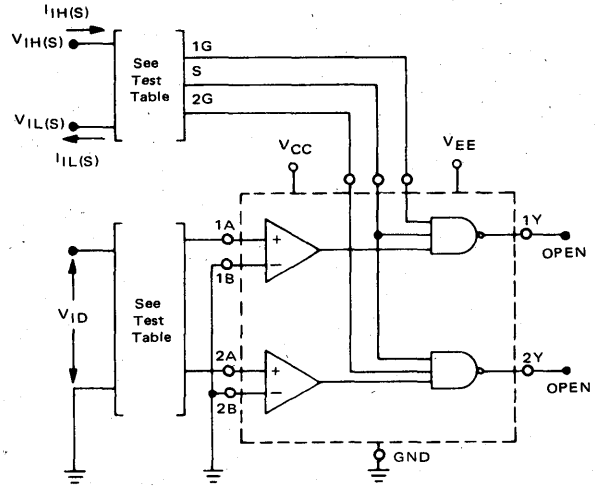
TEST TABLE

MC55107 MC75107	MC55108 MC75108	V_{ID}	STROBE 1G or 2G	STROBE S
TEST		APPLY		
V_{OH}	I_{CEX}	+25 mV	$V_{IH(S)}$	$V_{IH(S)}$
V_{OH}	I_{CEX}	-25 mV	$V_{IL(S)}$	$V_{IH(S)}$
V_{OH}	I_{CEX}	-25 mV	$V_{IH(S)}$	$V_{IL(S)}$
V_{OL}	V_{OL}	-25 mV	$V_{IH(S)}$	$V_{IH(S)}$

NOTES: 1. V_{IC} = -3.0 V to +3.0 V.
2. When testing one channel, the inputs of the other channel should be grounded.

TEST CIRCUITS (continued)

FIGURE 4 – $I_{IH(G)}$, $I_{IL(G)}$, $I_{IH(S)}$, and $I_{IL(S)}$



TEST	INPUT 1A	INPUT 2A	STROBE 1G	STROBE S	STROBE 2G
I_{IH} at Strobe 1G	+25 mV	Gnd	$V_{IH(S)}$	Gnd	Gnd
I_{IH} at Strobe 2G	Gnd	+25 mV	Gnd	Gnd	$V_{IH(S)}$
I_{IH} at Strobe S	+25 mV	+25 mV	Gnd	$V_{IH(S)}$	Gnd
I_{IL} at Strobe 1G	-25 mV	Gnd	$V_{IL(S)}$	4.5 V	Gnd
I_{IL} at Strobe 2G	Gnd	-25 mV	Gnd	4.5 V	$V_{IL(S)}$
I_{IL} at Strobe S	-25 mV	-25 mV	4.5 V	$V_{IL(S)}$	4.5 V

FIGURE 5 – I_{OS}

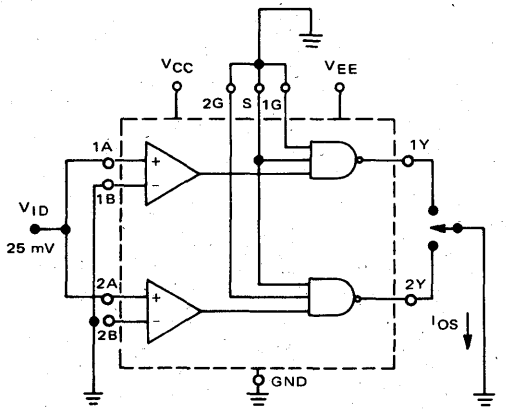
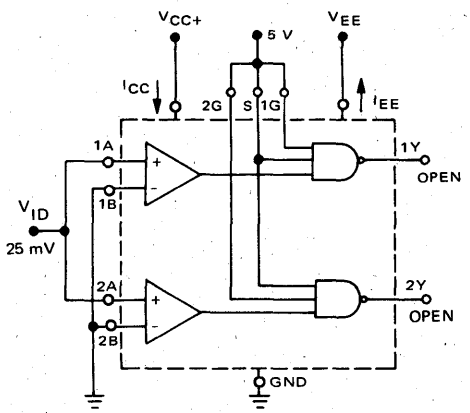


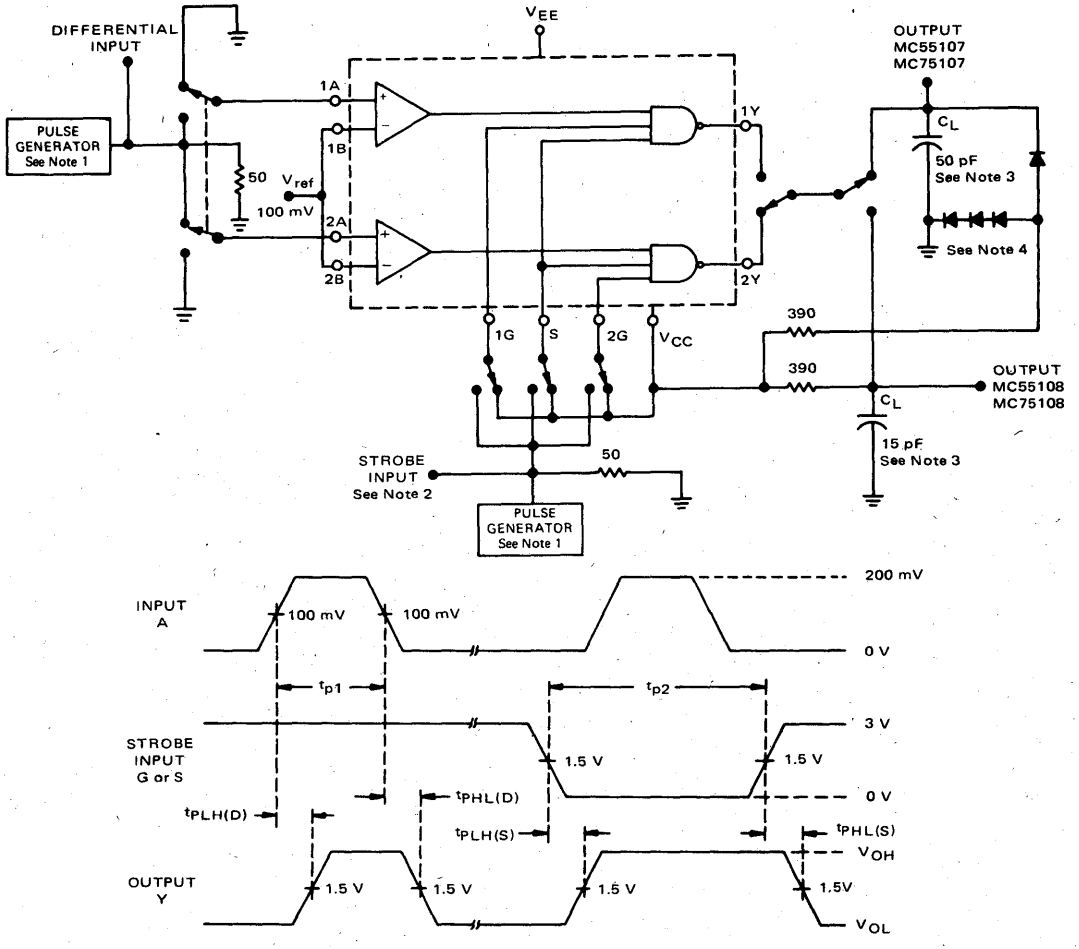
FIGURE 6 – I_{CC} and I_{EE}



NOTES: 1. Each channel is tested separately.
2. Not more than one output should be tested at one time.

TEST CIRCUITS (continued)

FIGURE 7 – PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS

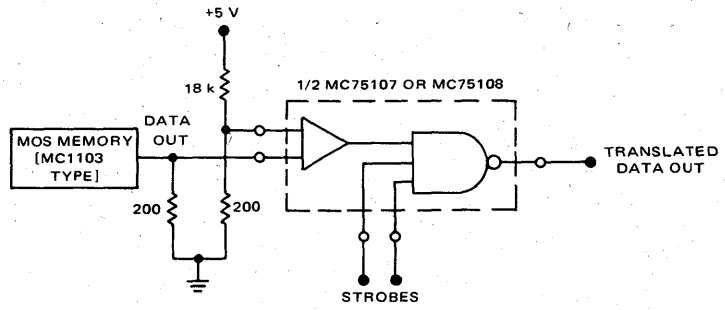


NOTES: 1. The pulse generators have the following characteristics: $z_o = 50\ \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{p1} = 500$ ns, PRR = 1 MHz $t_{p2} = 1$ ms, PRR = 500 kHz.

2. Strobe input pulse is applied to Strobe 1G when Inputs 1A-1B are being tested, to Strobe S when Inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916 or equivalent.

TYPICAL APPLICATION

FIGURE 8 – MOS-TO-TTL TRANSLATOR



ORDERING INFORMATION

Device	Temperature Range	Package
MC75110L	0°C to +70°C	Ceramic DIP
MC75110P	0°C to +70°C	Plastic DIP

MC75110

DUAL LINE DRIVER

The MC75110 dual line driver features independent channels with common voltage supply and ground terminals. Each driver circuit provides a constant output current that switches to either of two output terminals subject to the appropriate logic levels at the input terminals. Output current can be switched "off" (inhibited) by appropriate logic levels at the inhibit inputs. Output current is nominally 12 mA.

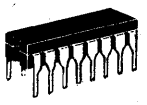
The inhibit feature permits use in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included to increase driver-logic versatility. With output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading occurs when the driver is used in a party-line system with other drivers. Output impedance of the driver in inhibited mode is very high (the output impedance of a transistor biased to cutoff).

All driver outputs have a common-mode voltage range of -3.0 volts to +10 volts, allowing common-mode voltage on the line without affecting driver performance.

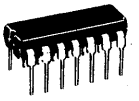
- Insensitive to Supply Variations Over the Entire Operating Range
- MTTL Input Compatibility
- Current-Mode Output (12 mA typical)
- High Output Impedance
- High Common-Mode Output Voltage Range (-3.0 V to +10 V)
- Inhibitor Available for Driver Selection

DUAL LINE DRIVER

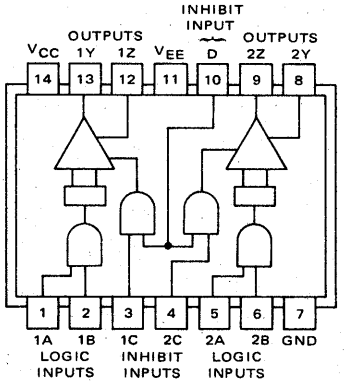
SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632
(TO-116)



P SUFFIX
PLASTIC PACKAGE
CASE 646



TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the "on" state.
High output represents the "off" state.

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Ratings	Symbol	Value	Unit
Power Supply Voltages (See Note 1)	V_{CC} V_{EE}	+7.0 -7.0	Volts
Logic and Inhibitor Input Voltages (See Note 1)	V_{in}	5.5	Volts
Common-Mode Output Voltage Range (See Note 1)	V_{OCR}	-5.0 to +12	Volts
Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above T_A = +25°C	P_D	 1000 3.85	 mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range Ceramic Dual In-Line Package Plastic Dual In-Line Package	T_{stg}	 -65 to +150 -65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (See Notes 1 and 2.)

Characteristic	Symbol	Min	Nom	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Volts
Common-Mode Output Voltage Range Positive Negative	V_{OCR}	 0 0	 – –	 +10 -3.0	Volts

Note 1. These voltage values are in respect to the ground terminal.
Note 2. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

DEFINITIONS OF INPUT LOGIC LEVELS*

Characteristic	Symbol	Test Fig.	Min	Max	Unit
High-Level Input Voltage (at any input)	V_{IH}	1,2	2.0	5.5	Volts
Low-Level Input Voltage (at any input)	V_{IL}	1,2	0	0.8	Volts

* The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic # #	Symbol	Test Fig.	MC75110 Min	MC75110 Typ #	MC75110 Max	Unit
High-Level Input Current to 1A, 1B, 2A or 2B	I_{IH_L}	1				
(V_{CC} = Max, V_{EE} = Max, V_{IH_L} = 2.4 V)#			–	–	40	μA
(V_{CC} = Max, V_{EE} = Max, V_{IH_L} = V_{CC} Max)			–	–	1.0	mA
Low-Level Input Current to 1A, 1B, 2A or 2B	I_{IL_L}	1				mA
(V_{CC} = Max, V_{EE} = Max, V_{IL_L} = 0.4 V)			–	–	-3.0	
High-Level Input Current into 1C or 2C	I_{IH_I}	2				
(V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V)			–	–	40	μA
(V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)			–	–	1.0	mA
Low-Level Input Current into 1C or 2C	I_{IL_I}	2				mA
(V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)			–	–	-3.0	
High-Level Input Current into D	I_{IH_I}	2				
(V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V)			–	–	80	μA
(V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)			–	–	2.0	mA
Low-Level Input Current into D	I_{IL_I}	2				mA
(V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)			–	–	-6.0	
Output Current ("on" state)	$I_{O(on)}$	3				mA
(V_{CC} = Max, V_{EE} = Max)			–	12	15	
(V_{CC} = Min, V_{EE} = Min)			6.5	–	–	
Output Current ("off" state)	$I_{O(off)}$	3				μA
(V_{CC} = Min, V_{EE} = Min)			–		100	
Supply Current from V_{CC} (with driver enabled)	$I_{CC(on)}$	4				mA
(V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)			–	28	35	
Supply Current from V_{EE} (with driver enabled)	$I_{EE(on)}$	4				mA
(V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)			–	-41	-50	
Supply Current from V_{CC} (with driver inhibited)	$I_{CC(off)}$	4				mA
(V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)			–	21	–	
Supply Current from V_{EE} (with driver inhibited)	$I_{EE(off)}$	4				mA
(V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)			–	-17	–	

#All typical values are at V_{CC} = +5.0 V, V_{EE} = -5.0 V.

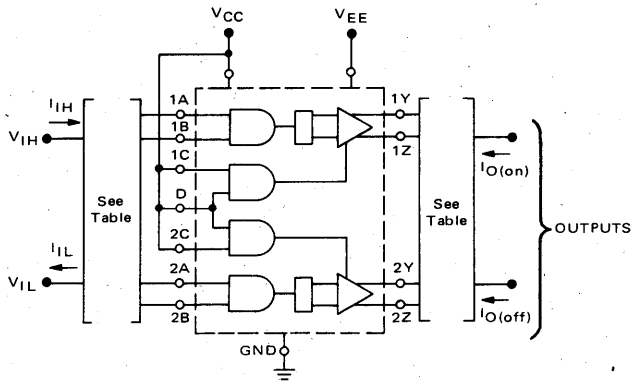
##For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time from Logic Input A or B to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)		5				ns
	t_{PLH_L}		–	9.0	15	
	t_{PHL_L}		–	9.0	15	
Propagation Delay Time from Inhibitor Input C or D to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)		5				ns
	t_{PLH_I}		–	16	25	
	t_{PHL_I}		–	13	25	

TEST CIRCUITS

FIGURE 1 – V_{IH}, V_{IL}, I_{IH}, and I_{IL}

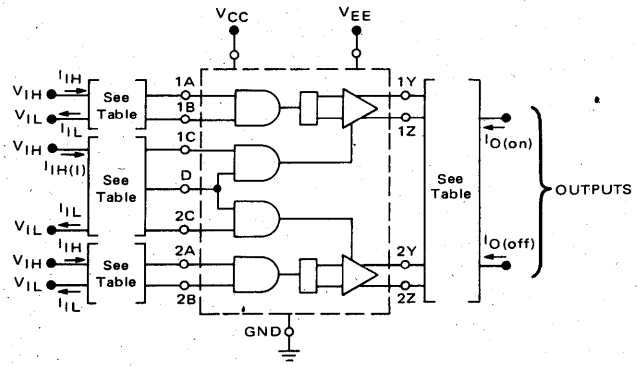


TEST TABLE

TEST AT ANY LOGIC INPUT	LOGIC INPUTS NOT UNDER TEST	ALL INHIBITOR INPUTS	OUTPUT 1Y or 2Y	OUTPUT 1Z or 2Z
V_{IH_L}	Open	V_{IH_I}	H (See Note 1)	L (See Note 1)
V_{IL_L}	V_{CC}	V_{IH_I}	L (See Note 1)	H (See Note 1)
I_{IH_L}	4.5 V	V_{IH_I}	Gnd	Gnd
I_{IL_L}	Gnd	V_{IH_I}	Gnd	Gnd

NOTES: 1. Low output represents the "on" state, high output represents the "off" state.
2. Each input is tested separately.
3. Arrows indicate actual direction of current flow.

FIGURE 2 – V_{IH}, V_{IL}, I_{IH}, I_{IL}

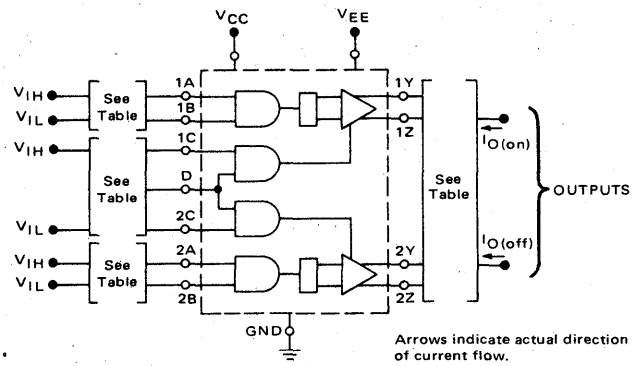


TEST TABLE

TEST AT ANY INHIBITOR INPUT	ALL LOGIC INPUTS	INHIBITOR INPUTS NOT UNDER TEST	OUTPUT 1Y or 2Y	OUTPUT 1Z or 2Z
V_{IH_I}	V_{IH_L}	Open	H(See Note 1)	L(See Note 1)
	V_{IL_L}	Open	L(See Note 1)	H(See Note 1)
V_{IL_I}	V_{IH_L}	V_{CC}	H(See Note 1)	H(See Note 1)
	V_{IL_L}	V_{CC}	H(See Note 1)	H(See Note 1)
I_{IH_I}	Gnd	4.5 V	Gnd	Gnd
I_{IL_I}	Gnd	Gnd	Gnd	Gnd

TEST CIRCUITS (continued)

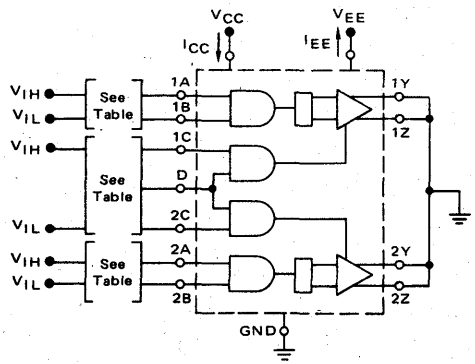
FIGURE 3– $I_{O(on)}$ and $I_{O(off)}$



TEST TABLE

TEST (Ground all output pins not under test.)		LOGIC INPUTS 1A or 2A	LOGIC INPUTS 1B or 2B	INHIBITOR INPUTS 1C or 2C	INHIBITOR INPUTS D
$I_{O(on)}$	at output 1Y or 2Y	V_{IL}	V_{IL}	V_{IH}	V_{IH}
		V_{IL}	V_{IH}		
		V_{IH}	V_{IL}		
$I_{O(on)}$	at output 1Z or 2Z	V_{IH}	V_{IH}	V_{IH}	V_{IH}
$I_{O(off)}$	at output 1Y or 2Y	V_{IH}	V_{IH}	V_{IH}	V_{IH}
$I_{O(off)}$	at output 1Z or 2Z	V_{IL}	V_{IL}	V_{IH}	V_{IH}
		V_{IL}	V_{IH}		
		V_{IH}	V_{IL}		
$I_{O(off)}$	at output 1Y, 2Y, 1Z, or 2Z	Either state	Either state	V_{IL}	V_{IL}
				V_{IL}	V_{IH}
				V_{IH}	V_{IL}

FIGURE 4 – I_{CC} and I_{EE}

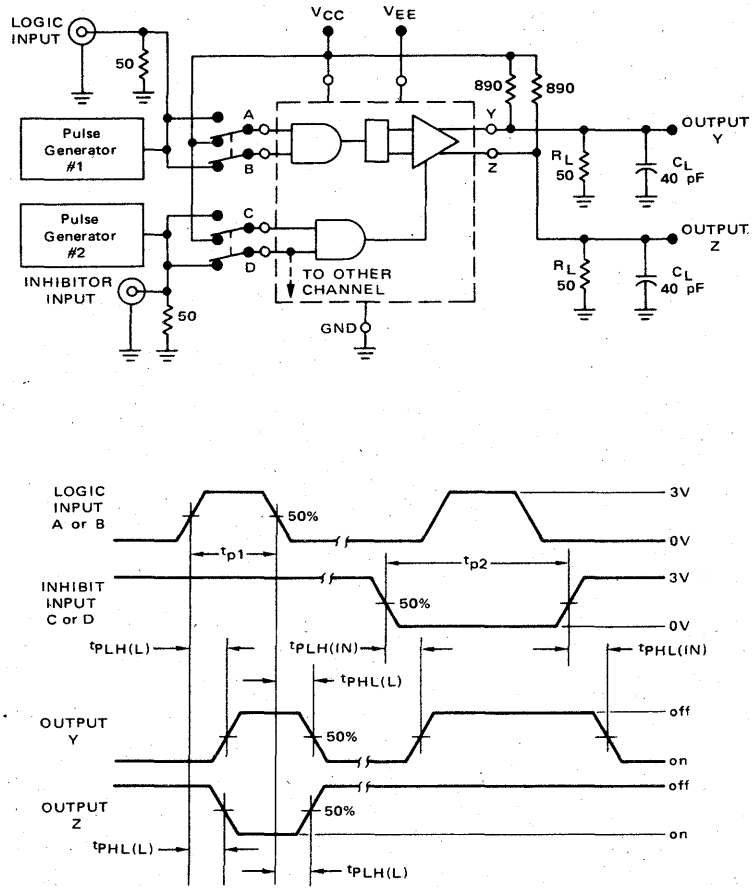


TEST TABLE

TEST		ALL LOGIC INPUTS	ALL INHIBITOR INPUTS
$I_{CC(on)}$	Driver enabled	V_{IL}	V_{IH}
$I_{EE(on)}$	Driver enabled	V_{IL}	V_{IH}
$I_{CC(off)}$	Driver inhibited	V_{IL}	V_{IL}
$I_{EE(off)}$	Driver inhibited	V_{IL}	V_{IL}

TEST CIRCUITS (continued)

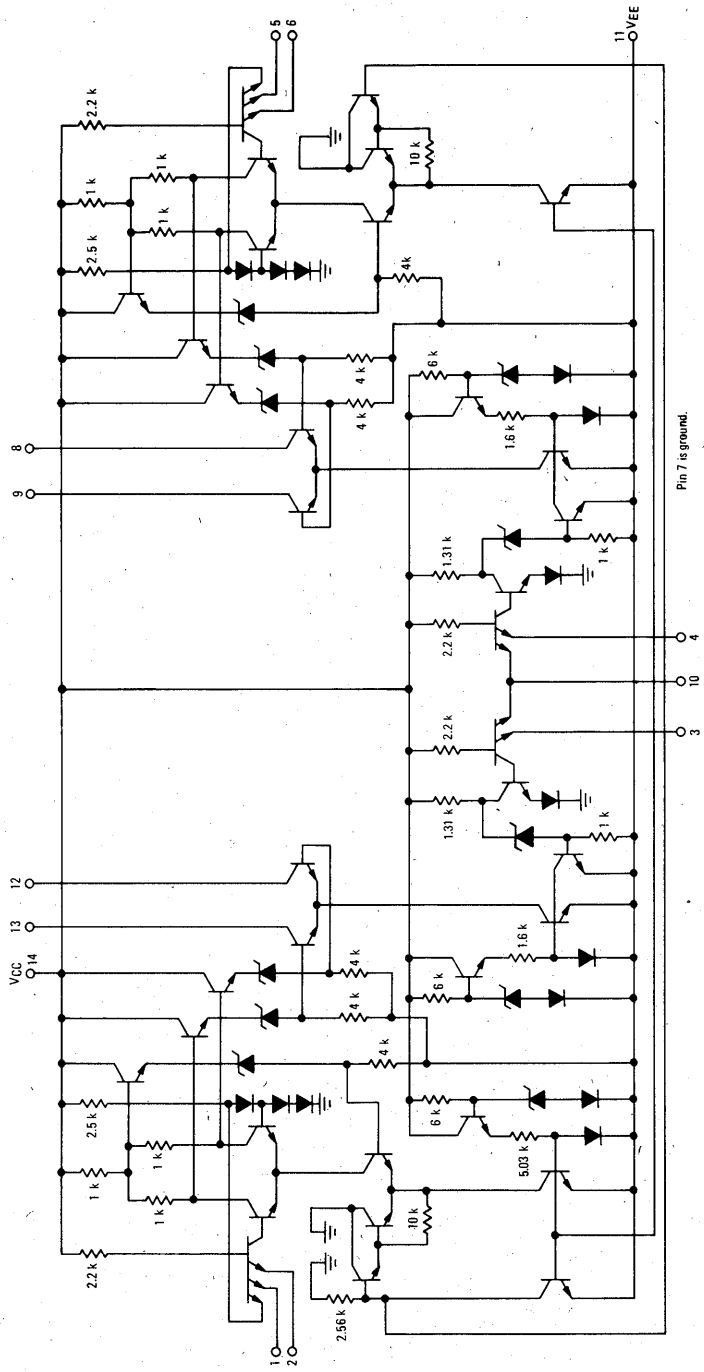
FIGURE 5 – PROPAGATION DELAY TIMES TEST CIRCUIT AND WAVEFORMS



NOTES: 1. The pulse generators have the following characteristics: $z_o = 50\ \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{p1} = 500$ ns, PRR = 1 MHz, $t_{p2} = 1$ ms, PRR = 500 kHz.
2. C_L includes probe and jig capacitance.
3. For simplicity, only one channel and the inhibitor connections are shown.

5

CIRCUIT DIAGRAM



ORDERING INFORMATION

Device	Temperature Range	Package
MC75140P1	0°C to +70°C	Plastic DIP

MC75140

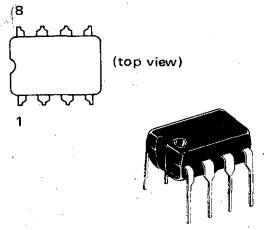
DUAL LINE RECEIVER

The MC75140P1 is a dual line receiver with common Strobe and Reference inputs. The Reference voltage is externally applied. This voltage may range from 1.5 to 3.5 volts, thus allowing for adjustment of maximum noise immunity in a given system design. The MC75140P1 is intended for use as a single-ended receiver in MTTL systems. Use in a party-line (bus-organized) system is aided by the low input current of the receiver.

- Single +5.0-Volts Power Supply
- ±100-mV Sensitivity
- Low Input Current
- MTTL Compatible Outputs
- Adjustable Reference Voltage
- Common Output Strobe

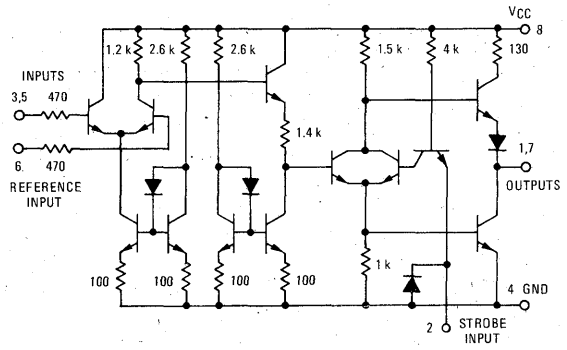
DUAL LINE RECEIVER

MONOLITHIC SILICON INTEGRATED CIRCUIT

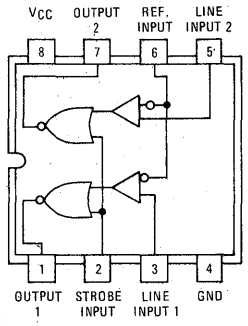


PLASTIC PACKAGE
CASE 626

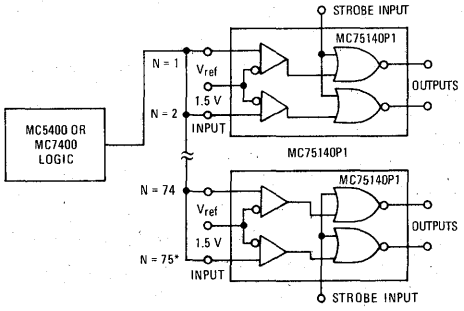
CIRCUIT SCHEMATIC
(1/2 Circuit Shown)



PIN CONNECTIONS



TYPICAL APPLICATION
HIGH FAN-OUT FROM A STANDARD MTTL GATE



*Most MC5400/MC7400 devices are capable of maintaining a 2.4-volt level under loads up to 7.5 mA.

FUNCTION TABLE

LINE INPUT	STROBE	OUTPUT
V_{ref} − 100 mV	L	H
V_{ref} + 100 mV	X	L
X	H	L

Positive Logic
H = High Level, L = Low Level,
X = Nonsignificant

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MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	Volts
Reference Voltage	V_{ref}	5.5	Volts
Line Input Voltage (with respect to Ground)	$V_{I(L)}$	-2.0 to +5.5	Volts
Line Input Voltage (with respect to V_{ref})	$V_{I(L)}$-V_{ref}	±5.0	Volts
Strobe Input Voltage	$V_{I(S)}$	5.5	Volts
Power Dissipation (Package Limitation) Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 830 6.6	 mW mW/°C
Operating Temperature Range (Ambient)	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Nom	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts
Reference Voltage Range	$V_{ref\ R}$	1.5	–	3.5	Volts
Input Voltage Range (Line or Strobe)	V_{IR}	0	–	5.5	Volts
Operating Ambient Temperature Range	T_A	0	–	+70	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±10%, V_{ref} = 1.5 to 3.5 V, T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ*	Max	Unit
High-Level Line Input Voltage	$V_{IH(L)}$	V_{ref} + 100	–	–	mV
Low-Level Line Input Voltage	$V_{IL(L)}$	–	–	V_{ref} - 100	mV
High-Level Strobe Input Voltage	$V_{IH(S)}$	2.0	–	–	Volts
Low-Level Strobe Input Voltage	$V_{IL(S)}$	–	–	0.8	Volt
High-Level Output Voltage $V_{IL(L)}$ = V_{ref} - 100 mV, $V_{IL(S)}$ = 0.8 V, I_{OH} = -400 µA	V_{OH}	 2.4	 –	 –	Volts
Low-Level Output Voltage $V_{IH(L)}$ = V_{ref} + 100 mV, $V_{IL(S)}$ = 0.8 V, I_{OL} = 16 mA $V_{IL(L)}$ = V_{ref} - 100 mV, $V_{IH(S)}$ = 2.0 V, I_{OL} = 16 mA	V_{OL}	 – –	 – –	 0.4 0.4	Volt
Strobe Input Clamp Voltage $I_{I(S)}$ = -12 mA	$V_{I(S)}$	 –	 –	 -1.5	Volts
Strobe Input Current (at max Input Voltage) $V_{I(S)}$ = 5.5 V	$I_{I(S)}$	 –	 –	 2.0	mA
High-Level Input Currents Strobe ($V_{I(S)}$ = 2.4 V) Line ($V_{I(L)}$ = V_{CC}, V_{ref} = 1.5 V) Reference (V_{ref} = 3.5 V, $V_{I(L)}$ = 1.5 V)	 $I_{IH(S)}$ $I_{IH(L)}$ $I_{IH(ref)}$	 – – –	 – 35 70	 80 100 200	µA
Low-Level Input Currents Strobe ($V_{I(S)}$ = 0.4 V) Line ($V_{I(L)}$ = 0 V, V_{ref} = 1.5 V) Reference (V_{ref} = 0 V, $V_{I(L)}$ = 1.5 V)	 $I_{IL(S)}$ $I_{IL(L)}$ $I_{IL(ref)}$	 – – –	 – – –	 -3.2 -10 -20	 mA µA µA
Short-Circuit Output Current** V_{CC} = 5.5 V	I_{OS}	 -18	 –	 -55	mA
Supply Current (output high) $V_{I(S)}$ = 0 V, $V_{I(L)}$ = V_{ref} - 100 mV	I_{CCH}	 –	 18	 30	mA
Supply Current (output low) $V_{I(S)}$ = 0 V, $V_{I(L)}$ = V_{ref} + 100 mV	I_{CCL}	 –	 20	 35	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, V_{ref} = 2.5 V, C_L = 15 pF, R_L = 400 Ω, T_A = +25°C unless otherwise noted.)
See Figure 1.

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time (low-to-high level output from Line input)	$t_{PLH(L)}$	–	22	35	ns
Propagation Delay Time (high-to-low level output from Line input)	$t_{PHL(L)}$	–	22	30	ns
Propagation Delay Time (low-to-high level output from Strobe input)	$t_{PLH(S)}$	–	12	22	ns
Propagation Delay Time (high-to-low level output from Strobe input)	$t_{PHL(S)}$	–	8.0	15	ns

*All typical values are at V_{CC} = 5.0 V, T_A = +25°C.
**Only one output should be shorted at a time.

FIGURE 1 – SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

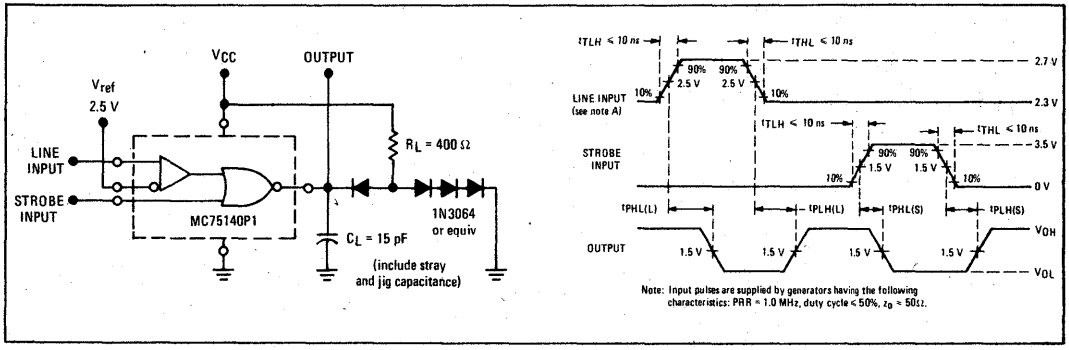

FIGURE 2 – OUTPUT VOLTAGE versus LINE INPUT VOLTAGE

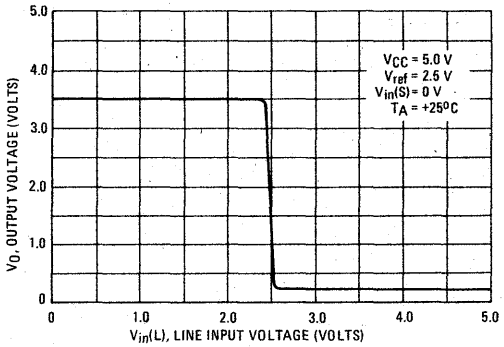

FIGURE 3 – SCHMITT TRIGGER

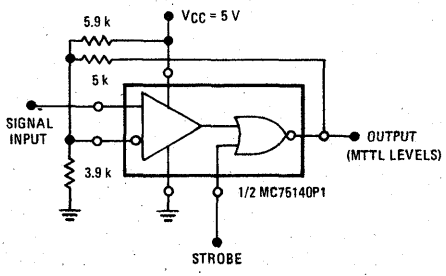

FIGURE 4 – TRANSFER CHARACTERISTICS FOR SCHMITT TRIGGER

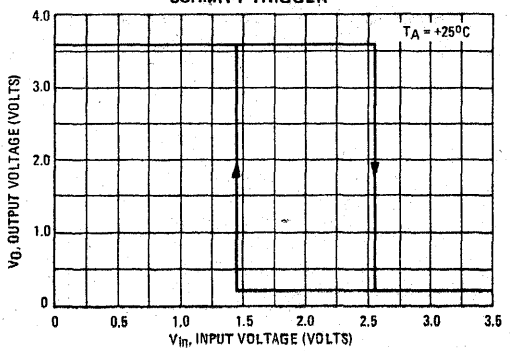

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FIGURE 5 – GATED OSCILLATOR

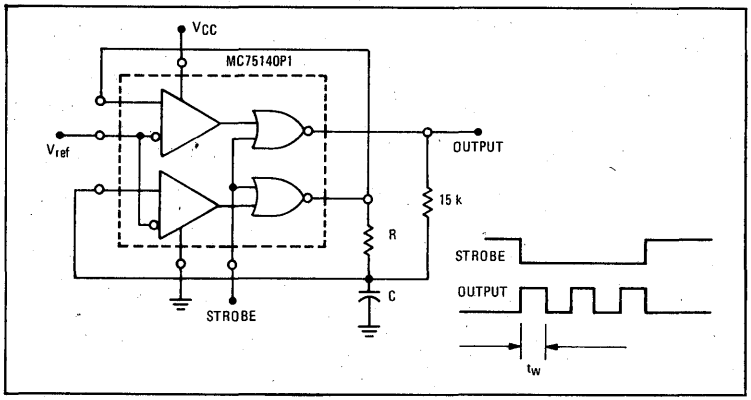


FIGURE 6 – GATE OSCILLATOR FREQUENCY versus RC TIME CONSTANT

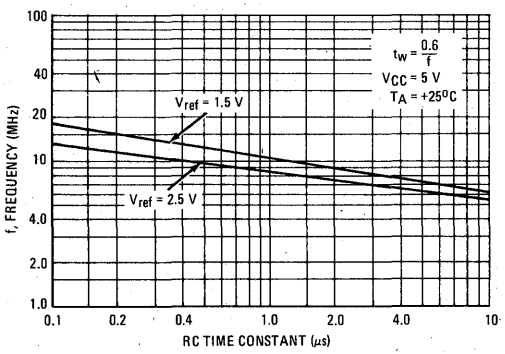
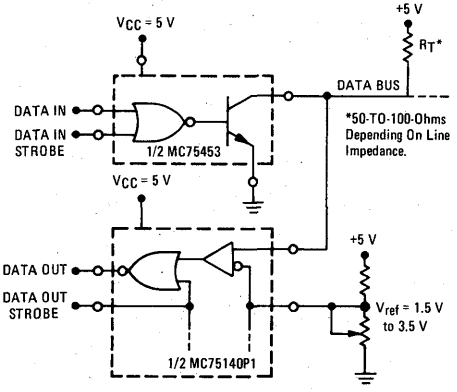


FIGURE 7 – DUAL BUS TRANSCEIVER



ORDERING INFORMATION

Device	Temperature Range	Package
MC55325F	−55°C to +125°C	Ceramic Flat
MC55325L	−55°C to +125°C	Ceramic DIP
MC75325F	0°C to +70°C	Ceramic Flat
MC75325L	0°C to +70°C	Ceramic DIP
MC75325P	0°C to +70°C	Plastic DIP

MC75325
MC55325

Specifications and Applications Information

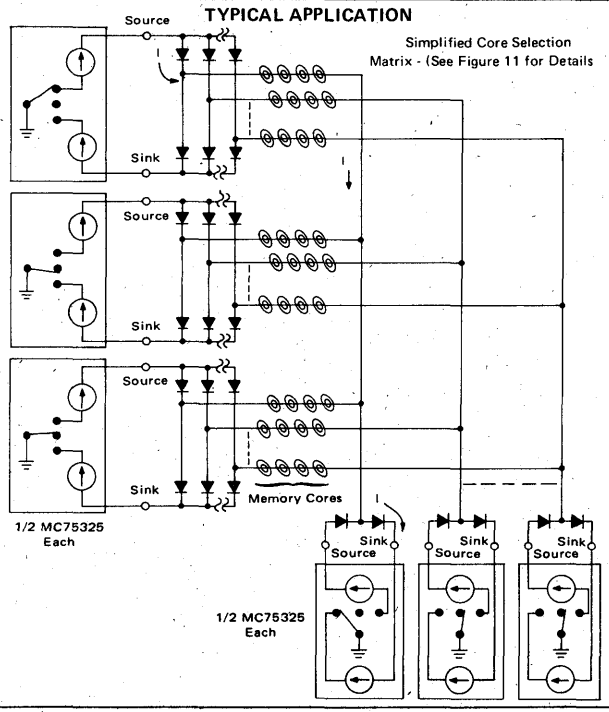
DUAL MEMORY DRIVER

The MC55325/75325 is a monolithic integrated circuit memory driver with logic inputs, and is designed for use with magnetic memories.

The device contains two 600-mA source-switch pairs and two 600-mA sink-switch pairs. Source selection is determined by one of two logic inputs, and source turn-on is determined by the source strobe. Likewise, sink selection is determined by one of two logic inputs, and sink turn-on is determined by the sink strobe. With this arrangement selection of one of the four switches provides turn-on with minimum time skew of the output current rise.

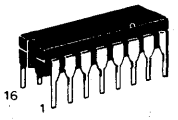
- 600-mA Output Capability
- Fast Switching Times
- Input Clamp Diodes
- Dual Sink and Dual Source Outputs
- MDTL and MTTL Compatibility
- 24-Volt Output Capability

TYPICAL APPLICATION

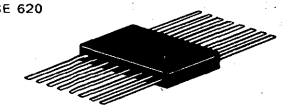


DUAL MEMORY DRIVER

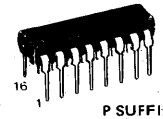
SILICON MONOLITHIC INTEGRATED CIRCUIT



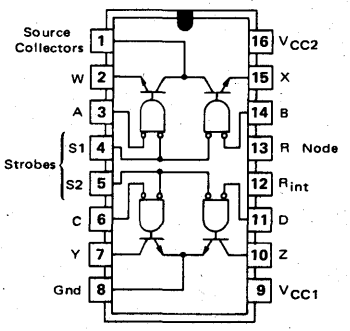
L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650



P SUFFIX
PLASTIC PACKAGE
CASE 648
(MC75325 only)



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MAXIMUM RATINGS (T_A = 25° unless otherwise noted)

Rating	Symbol	Value	Unit
Supply Voltage (Note 1)	V_{CC1} V_{CC2}	7.0 25	Vdc Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation (Package Limitation) Ceramic and Plastic Packages Derate above T_A = +25°C	P_D	 1.0 6.6	 W mW/°C
Operating Ambient Temperature Range MC55325 MC75325	T_A	 -55 to +125 0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1. Voltage values are with respect to the network ground terminal.

TRUTH TABLE

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	On	Off	Off	Off
H	L	X	X	L	H	Off	On	Off	Off
X	X	L	H	H	L	Off	Off	On	Off
X	X	H	L	H	L	Off	Off	Off	On
X	X	X	X	H	H	Off	Off	Off	Off
H	H	H	H	X	X	Off	Off	Off	Off

H = high level, L = low level, X = irrelevant

NOTE: Not more than one output is to be on at any one time.

ELECTRICAL CHARACTERISTICS ($T_A = T_{low}$ to T_{high} unless otherwise noted(1))

Characteristic	Symbol	MC55325 Min	MC55325 Typ(2)	MC55325 Max	MC75325 Min	MC75325 Typ(2)	MC75325 Max	Unit
Input Voltage – High Logic State	V_{IH}	2.0	–	–	2.0	–	–	V
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	–	–	0.8	V
Input Clamp Voltage (V_{CC1} = 4.5 V, V_{CC2} = 24 V, I_I = -10 mA, T_A = 25°C)	V_I	–	-1.3	-1.7	–	-1.3	-1.7	V
Output Current – Off State (V_{CC1} = 4.5 V, V_{CC2} = 24 V) $T_A = T_{low}$ to T_{high}	I_{off}	–	–	500	–	–	200	μA
T_A = 25°C		–	3.0	150	–	3.0	200	
Output Voltage – High Logic State (V_{CC1} = 4.5 V, V_{CC2} = 24 V, I_O = 0)	V_{OH}	19	23	–	19	23	–	V
Saturation Voltage(3)	V_{sat}							V
Source Outputs (V_{CC1} = 4.5 V, V_{CC2} = 15 V, $I_{source} \approx$ -600 mA, R_L = 24 ohms, Note 4) $T_A = T_{low}$ to T_{high}		–	–	0.9	–	–	0.9	
T_A = 25°C		–	0.43	0.7	–	0.43	0.75	
Sink Outputs (V_{CC1} = 4.5 V, V_{CC2} = 15 V, $I_{sink} \approx$ 600 mA, R_L = 24 ohms, Note 4) $T_A = T_{low}$ to T_{high}		–	–	0.9	–	–	0.9	
T_A = 25°C		–	0.43	0.7	–	0.43	0.75	
Input Current at Maximum Input Voltage (V_{CC1} = 5.5 V, V_{CC2} = 24 V, V_I = 5.5 V)	I_I							mA
Address Inputs		–	–	1.0	–	–	1.0	
Strobe Inputs		–	–	2.0	–	–	2.0	
Input Current – High Logic State (V_{CC1} = 5.5 V, V_{CC2} = 24 V, V_I = 2.4 V)	I_{IH}							μA
Address Inputs		–	3.0	40	–	3.0	40	
Strobe Inputs		–	6.0	80	–	6.0	80	
Input Current – Low Logic State (V_{CC1} = 5.5 V, V_{CC2} = 24 V, V_I = 0.4 V)	I_{IL}							mA
Address Inputs		–	-1.0	-1.6	–	-1.0	-1.6	
Strobe Inputs		–	-2.0	-3.2	–	-2.0	-3.2	
Supply Current – Output Condition Off (V_{CC1} = 5.5 V, V_{CC2} = 24 V, T_A = 25°C)	$I_{CC(off)}$							mA
From V_{CC1}		–	14	22	–	14	22	
From V_{CC2}		–	7.5	20	–	7.5	20	
Supply Current from V_{CC1}, Either Sink "On" (V_{CC1} = 5.5 V, V_{CC2} = 24 V, I_{sink} = 50 mA, T_A = 25°C)	I_{CC1}	–	55	70	–	55	70	mA
Supply Current from V_{CC2}, Either Source "On" (V_{CC1} = 5.5 V, V_{CC2} = 24 V, I_{source} = -50 mA, T_A = 25°C)	I_{CC2}	–	32	50	–	32	50	mA

(1) T_{low} = -55°C for MC55325, 0°C for MC75325
T_{high} = +125°C for MC55325, +70°C for MC75325

(2) All typical values are at T_A = 25°C

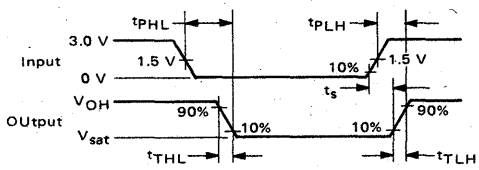
(3) Not more than one output is to be "on" at any one time.

(4) Saturation voltage must be measured using pulse techniques: Pulse Width = 200 μs, Duty Cycle ≤ 2%

SWITCHING CHARACTERISTICS (V_{CC1} = 5.0 V, C_L = 25 pF, T_A = 25°C)

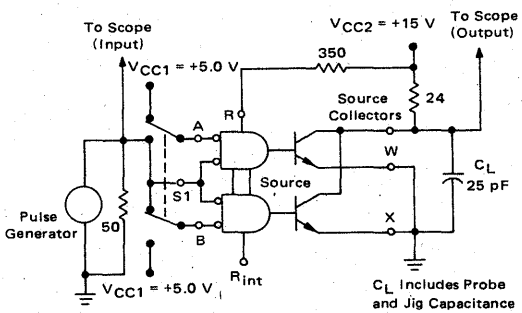
Characteristics		Symbol	MC55325/MC75325 Min	Typ	Max	Unit
Propagation Delay Time to Source Collectors (V_{CC2} = 15 V, R_L = 24 ohms)	Low-to-High Level	t_{PLH}	–	25	50	ns
	High-to-Low Level	t_{PHL}	–	25	50	ns
Transition Time (V_{CC2} = 20 V, R_L = 1 k ohms)	Low-to-High Level	t_{TLH}	–	55	–	ns
	High-to-Low Level	t_{THL}	–	7.0	–	ns
Propagation Delay Time to Sink Outputs (V_{CC2} = 15 V, R_L = 24 ohms)	Low-to-High Level	t_{PLH}	–	20	45	ns
	High-to-Low Level	t_{PHL}	–	20	45	ns
Transition Time (V_{CC2} = 15 V, R_L = 24 ohms)	Low-to-High Level Output	t_{TLH}	–	7.0	15	ns
	High-to-Low Level Output	t_{THL}	–	9.0	20	ns
Storage Time to Sink Outputs (V_{CC2} = 15 V, R_L = 24 ohms)		t_s	–	15	30	ns

FIGURE 1 – SWITCHING TIMES TO SOURCE COLLECTORS AND SINK OUTPUTS



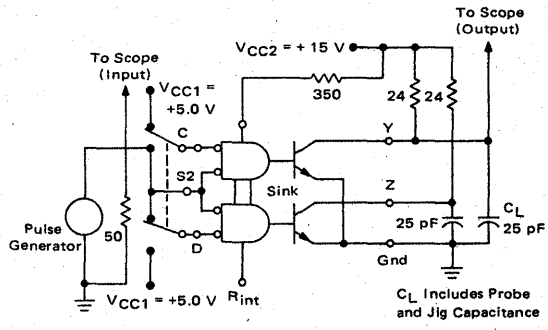
Input Pulse Characteristics:
z_o = 50Ω, Pulse Width = 200 ns,
$t_{TLH} = t_{THL} \leq$ 10 ns, Duty Cycle ≤ 1%

FIGURE 2 – PROPAGATION TIME TO SOURCE COLLECTORS



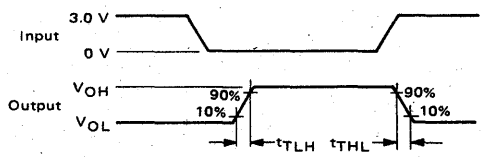
Source W Shown Under Test

FIGURE 3 – PROPAGATION TIME, TRANSITION TIME AND STORAGE TIME TO SINK OUTPUTS



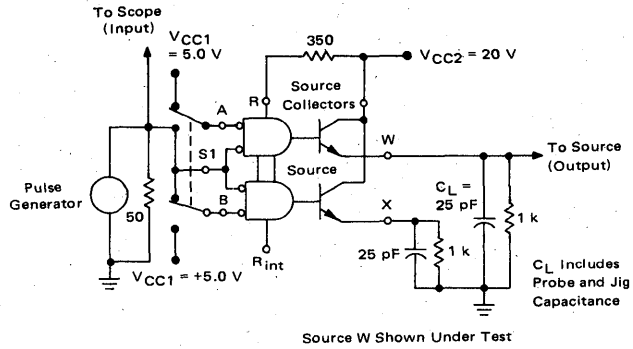
Sink Y Shown Under Test

FIGURE 4 – SWITCHING TIMES ON SOURCE OUTPUTS (See Figure 5)



Input Pulse Characteristics:
$t_{THL} = t_{TLH} \leq$ 10 ns, Duty Cycle ≤ 1%
Pulse Width = 200 ns

FIGURE 5 – TRANSITION TIME ON SOURCE OUTPUTS



Source W Shown Under Test

TYPICAL PERFORMANCE CURVES

FIGURE 6 – SOURCE COLLECTOR CURRENT (Off-State) versus AMBIENT TEMPERATURE

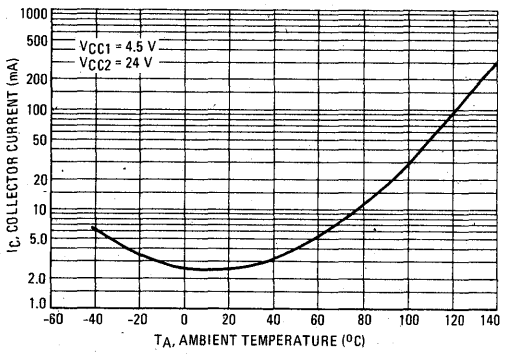


FIGURE 7 – SINK OUTPUT VOLTAGE-HIGH STATE V_{OH} versus AMBIENT TEMPERATURE

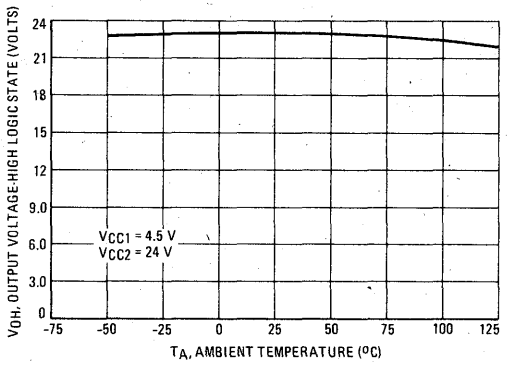


FIGURE 8 – SOURCE OR SINK SATURATION VOLTAGE versus AMBIENT TEMPERATURE

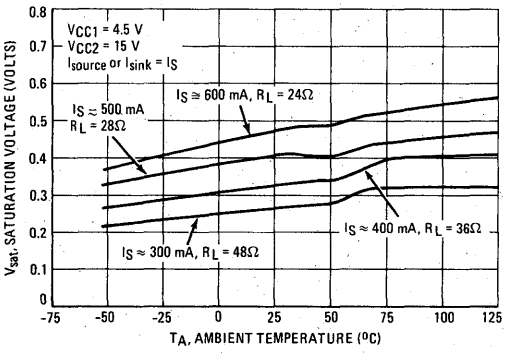
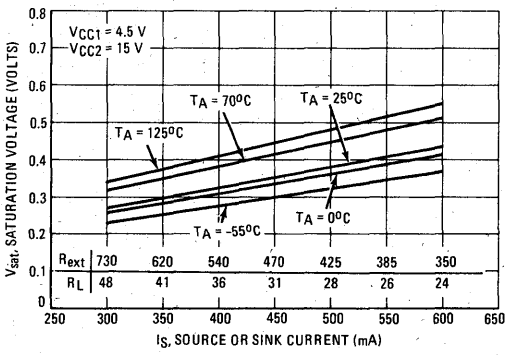


FIGURE 9 – SOURCE OR SINK SATURATION VOLTAGE versus SOURCE OR SINK CURRENT



APPLICATIONS INFORMATION

BASE DRIVE RESISTOR

An internal 575 Ω resistor connected between the V_{CC2} and the R_{int} terminals is provided in the MC55325/75325 to supply sufficient base drive for source currents to 375 mA at V_{CC2} of 15 Volts or 600 mA at V_{CC2} of 24 Volts. Connecting the R node to the R_{int} node selects this internal resistor. If source currents greater than 375 mA are required, the R_{int} node should be left open and an appropriate resistor connected between V_{CC2} and the R node. This method allows source base drive currents regulated to typically within ± 5%. This has an added advantage of removing the power dissipated in the resistor from the IC package, allowing the device to source greater currents at a given junction temperature.

The value of the required external resistor in a particular memory application may be computed using the following equation:

$$R_{ext} = \frac{16\,(V_{CC2\ min} - V_S - 2.2)}{I_L - 1.6\,(V_{CC2\ min} - V_S - 2.9)} \qquad (1)$$

Where: R_{ext} = kΩ.
V_S = the source output voltage referred to ground.
I_L = mA.

During the load current pulse the power dissipated in the resistor, R_{ext} is

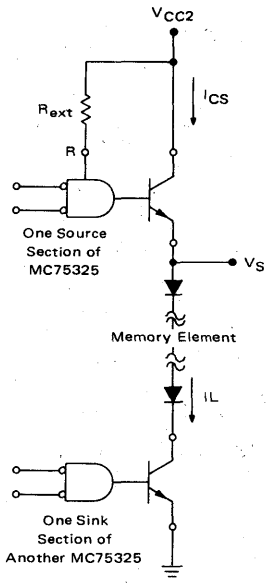
$$P_{R_{ext}} \approx \frac{I_L\,(V_{CC2\ min} - V_S - 2)}{16} \qquad (2)$$

Where: $P_{R_{ext}}$ = mW.

The source collector current I_{CS} is approximately 94% of total load current, I_L. The remaining current flows in the base of the source transistor through the external resistor R_{ext} or the source gate. See Figure 10 for added details.

An internal pull-up resistor in parallel with a clamping diode to V_{CC2} is provided at each sind-output collector to protect against voltage surges generated by switching reduction loads.

FIGURE 10 – TYPICAL CIRCUIT USED FOR R_{ext} CALCULATION



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SELECTION MATRIX

The combination of current source and sink pairs within the MC75325 is often utilized to implement a selection matrix for core memory systems. A typical, simplified system is shown in Figure 11.

The selection of any particular line (line 7, for example) is made by activating a particular, unique combination of two source/sink pairs. For an example, with the Mode Select input high and $\overline{B1}$ low, current source X of #1 MC75325 will be activated. This selects lines 4-7. When input C4 goes low, on #4 MC75325, current will flow through line 7 from source X (of device #1) to sink Y of device #4.

Changing the logic state of device #1 to input $\overline{D1}$ low, device #4 to input $\overline{A4}$ low, and applying a low to the Mode Select input, reverses the direction of the current in line 7 with the #1 MC75325 sinking the current and the #4 device sourcing it.

Drive line inductance and capacitance only limits the number of drive lines a source/sink pair can drive and thus the size of a matrix possible.

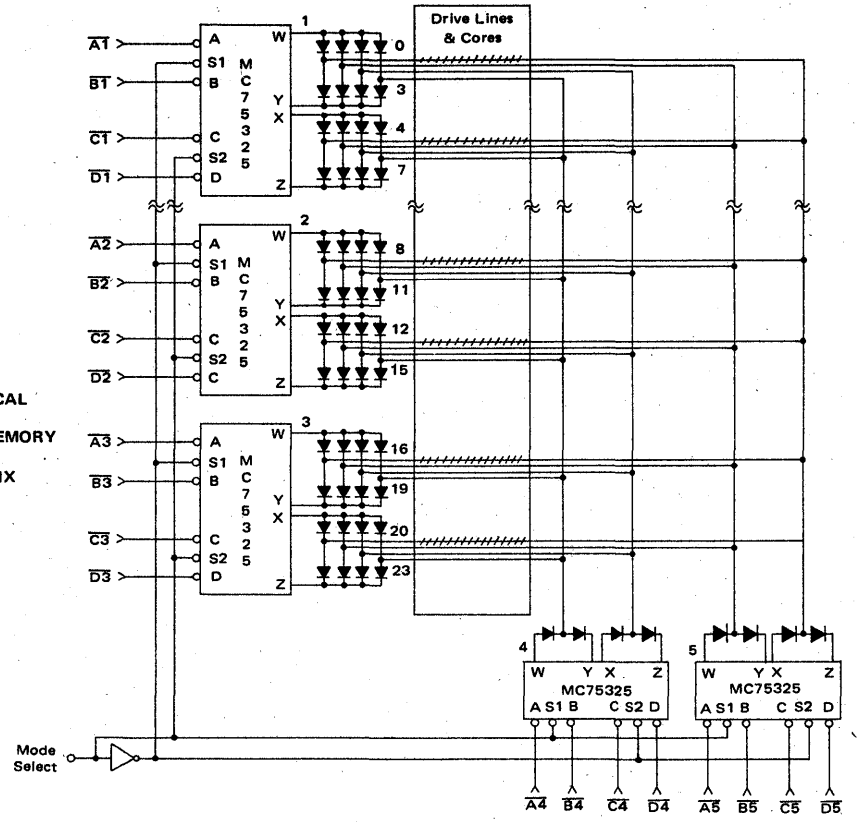

FIGURE 11 – TYPICAL APPLICATION - CORE MEMORY SELECTION MATRIX

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ORDERING INFORMATION

Device	Temperature Range	Package
MC75365L	0°C to +70°C	Ceramic DIP
MC75365P	0°C to +70°C	Plastic DIP

MC75365

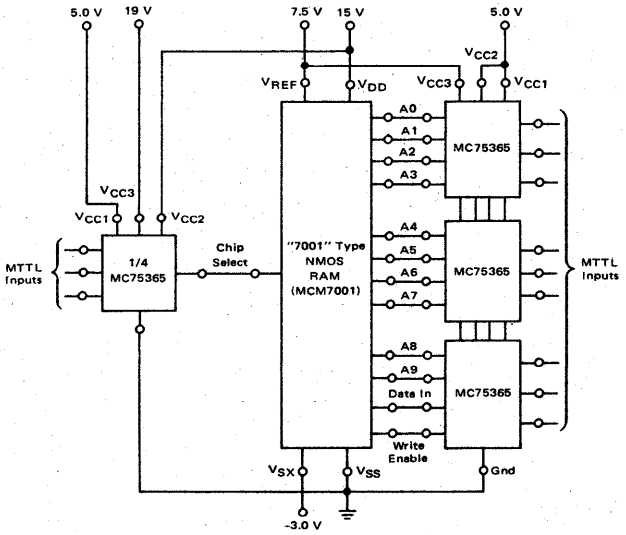
Specifications and Applications Information

QUAD MOS CLOCK DRIVER
OR HIGH-VOLTAGE, HIGH-CURRENT NAND DRIVER

The MC75365 is intended for driving the highly capacitive Address, Control and Timing inputs on a variety of MOS RAMs such as the "1103" and "7001" types. It is designed to operate from the MTTL 5.0 V power supply and the V_{SS} and V_{BB} power supplies used with the memories in most applications. Operation is recommended at $V_{CC3} \simeq V_{CC2} + 3$ V, but the part is useable over a wide latitude of supply voltages. V_{CC2} may be tied directly to V_{CC3} in many conditions.

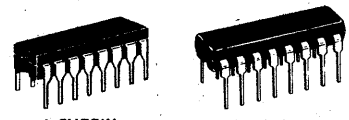
- Pin Compatible with Intel 3207 and Interchangeable with T. I. SN75365
- MTTL and MDTL Compatible, Diode-Clamped Inputs
- Two Common Enable Inputs per Gate Pair
- Low Standby Power Consumption Transient
- Capable of Driving High Capacitive Loads
- Fast Switching Operation

TYPICAL APPLICATION
with "7001" Type 1 K RAM



QUAD MOS CLOCK DRIVER

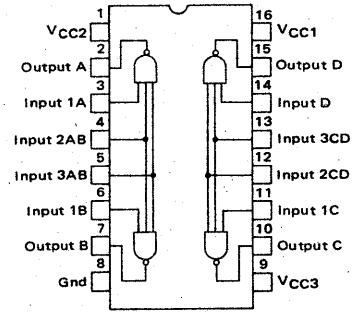
SILICON MONOLITHIC INTEGRATED CIRCUITS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



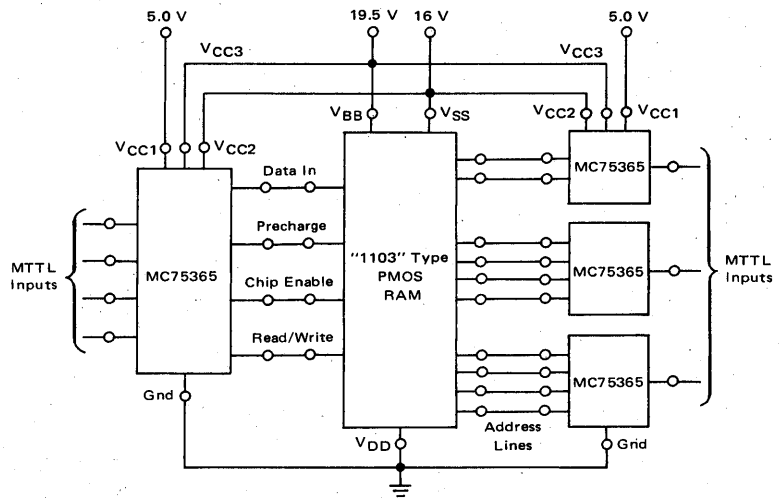
TRUTH TABLE

INPUT			OUTPUT
1	2	3	
H	H	H	L
L	I	I	H
I	L	I	H
I	I	L	H

Where:
H = High Logic State
L = Low Logic State
I = Irrelevant

5

TYPICAL APPLICATION
with "1103" Type 1 K RAM



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MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC1} V_{CC2} V_{CC3}	-0.5 to 7.0 -0.5 to 25 -0.5 to 30	V
Input Voltage	V_I	5.5	V
Input Differential Voltage (see Note 1)	V_{ID}	5.5	V
Power Dissipation (Package Limitation)			
Ceramic Package @ T_A = 25°C	P_D	1000	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Plastic Package @ T_A = 25°C	P_D	830	mW
Derate above T_A = 25°C	$1/R_{\theta JA}$	6.6	mW/°C
Ceramic Package @ T_C = 25°C	P_D	3.0	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	20	mW/°C
Plastic Package @ T_C = 25°C	P_D	1.8	Watts
Derate above T_C = 25°C	$1/R_{\theta JC}$	14	mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Junction Temperature	T_J		°C
Ceramic Package		175	
Plastic Package		150	
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1. This is the differential voltage between any two inputs to any single gate.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC1}	4.75	5.0	5.25	V
	V_{CC2}	4.75	20	24	
	V_{CC3}	V_{CC2}	24	28	
Difference between V_{CC3} and V_{CC2}	V_{CC3}-V_{CC2}	0	4.0	10	V
Operating Temperature Range	T_A	0	–	70	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted $T_A = 25^oC$, $V_{CC1} = 5.0$ V, $V_{CC2} = 20$ V, $V_{CC3} = 24$ V, $C_L = 200$ pF, $R_D = 24\Omega$, See Figures 1 and 2.)

Characteristic	Symbol	Min	Typ*	Max	Unit
Input Voltage – High Logic State	V_{IH}	2.0	–	–	V
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	V
Input Clamp Voltage ($I_{IC} = -12$ mA)	V_{IC}	–	–	1.5	V
Input Current – Maximum Input Voltage ($V_{IH} = 5.5$ V)	I_{IH1}	–	–	1.0	mA
Input Current – High Logic State	I_{IH2}				μA
(V_{IH} (1) = 2.4 V)		–	–	40	
(V_{IH} (2) or V_{IH} (3) = 2.4 V)		–	–	80	
Input Current – Low Logic State	I_{IL}				mA
(V_{IL} (1) = 0.4 V)		–	-1.0	-1.6	
(V_{IL} (2) or V_{IL} (3) = 0.4 V)		–	-2.0	-3.2	
Output Voltage – High Logic State					V
($V_{CC3} = V_{CC2} + 3.0$ V, $V_{IL} = 0.8$ V, $I_{OH} = -100$ μA)	V_{OH1}	V_{CC2} -0.3	V_{CC2} -0.1	–	
($V_{CC3} = V_{CC2} + 3.0$ V, $V_{IL} = 0.8$ V, $I_{OH} = -10$ mA)	V_{OH2}	V_{CC2} -1.2	V_{CC2} -0.9	–	
($V_{CC3} = V_{CC2}$, $V_{IL} = 0.8$ V, $I_{OH} = -50$ μA)	V_{OH3}	V_{CC2} -1.0	V_{CC2} -0.7	–	
($V_{CC3} = V_{CC2}$, $V_{IL} = 0.8$ V, $I_{OH} = -10$ mA)	V_{OH4}	V_{CC2} -2.3	V_{CC2} -1.8	–	
Output Clamp Voltage ($V_{IL} = 0$ V, $I_{OC} = 20$ mA)	V_{OC}	–	–	V_{CC2} +1.5	V
Output Voltage – Low Logic State					V
($V_{IH} = 2.0$ V, $I_{OL} = 10$ mA)	V_{OL1}	–	0.15	0.3	
($15 \text{ V} \leqslant V_{CC3} \leqslant 28$ V, $V_{IH} = 2.0$ V, $I_{OL} = 40$ mA)	V_{OL2}	–	0.25	0.5	
Power Supply Currents – Outputs High Logic State					mA
($V_{CC1} = 5.25$ V, $V_{CC2} = 24$ V, $V_{CC3} = 28$ V,	$I_{CC1(H)}$	–	4.0	8.0	
$V_{IL} = 0$ V, $I_{OH} = 0$ mA)	$I_{CC2(H)}$	–	-2.2	-3.2/+0.25	
	$I_{CC3(H)}$	–	2.2	3.5	
($V_{CC1} = 5.25$ V, $V_{CC2} = 24$ V, $V_{CC3} = 24$ V	$I_{CC2(H)}$	–	–	0.25	
$V_{IL} = 0$ V, $I_{OH} = 0$ mA)	$I_{CC3(H)}$	–	–	0.5	
Power Supply Currents – Output Low Logic State					mA
($V_{CC1} = 5.25$ V, $V_{CC2} = 24$ V, $V_{CC3} = 28$ V	$I_{CC1(L)}$	–	31	47	
$V_{IH} = 5.0$ V, $I_{OL} = 0$ mA)	$I_{CC2(L)}$	–	–	2.5	
	$I_{CC3(L)}$	–	16	25	
Power Supply Currents – Standby Condition					mA
($V_{CC1} = 0$ V, $V_{CC2} = 24$ V, $V_{CC3} = 24$ V	$I_{CC2(S)}$	–	–	0.25	
$V_{IH} = 5.0$ V, $I_{OL} = 0$ mA)	$I_{CC3(S)}$	–	–	0.5	

*Typical Values at 25^oC, $V_{CC1} = 5.0$ V, $V_{CC2} = 20$ V and $V_{CC3} = 24$ V

SWITCHING CHARACTERISTICS (Unless otherwise noted $T_A = 25^oC$, $V_{CC1} = 5.0$ V, $V_{CC2} = 20$ V, $V_{CC3} = 24$ V, $C_L = 200$ pF, $R_D = 24\Omega$, See Figures 1 and 2.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time, Low to High State Output	t_{PLH}	10	31	48	ns
Propagation Delay Time, High to Low State Output	t_{PHL}	10	30	46	
Delay Time, Low to High State Output	t_{DLH}	–	11	20	ns
Delay Time, High to Low State Output	t_{DHL}	–	10	18	
Transition Time, Low to High State Output	t_{TLH}	–	20	33	ns
Transition Time, High to Low State Output	t_{THL}	–	20	33	

5

FIGURE 1 – SWITCHING CHARACTERISTIC TEST CIRCUIT

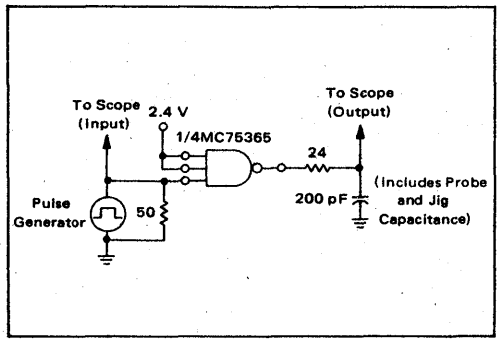
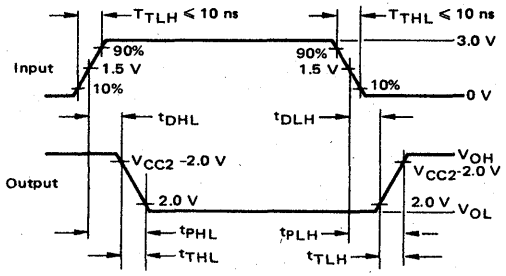


FIGURE 2 – SWITCHING CHARACTERISTICS WAVEFORMS



Input Pulse Characteristics:
PRR = 1.0 MHz, PW = 500 ns, $t_{TLH} = t_{THL} \leq 10$ ns

TYPICAL PERFORMANCE CURVES

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FIGURE 3 – OUTPUT VOLTAGE – HIGH LOGIC STATE versus OUTPUT CURRENT

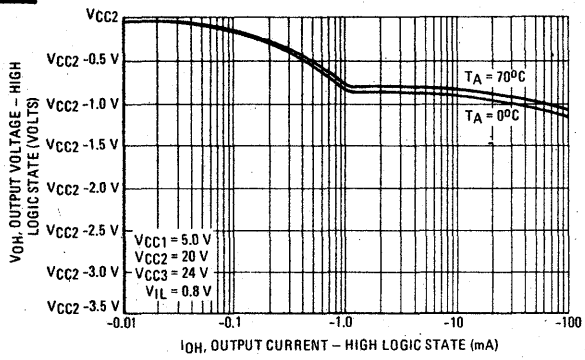


FIGURE 4 – OUTPUT VOLTAGE – HIGH LOGIC STATE versus OUTPUT CURRENT

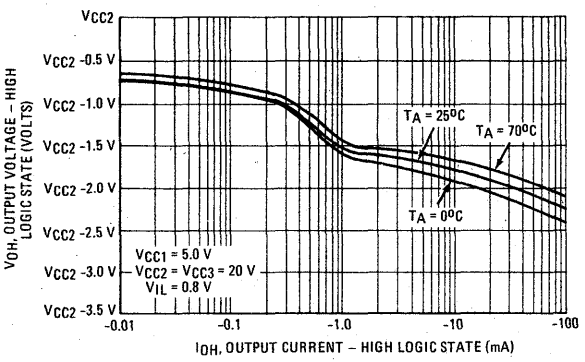


FIGURE 5 – OUTPUT VOLTAGE – LOW LOGIC STATE versus OUTPUT CURRENT

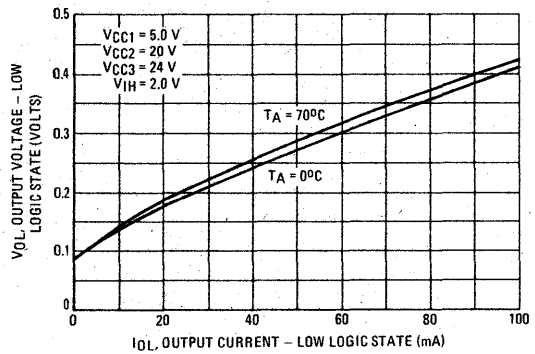
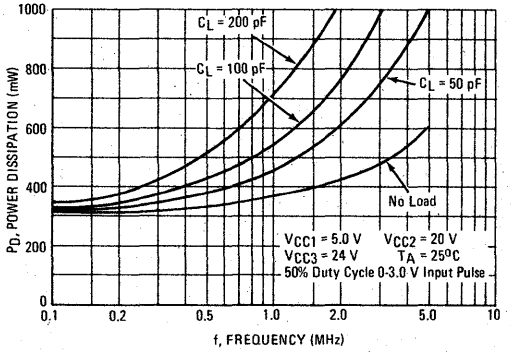


FIGURE 6 – TOTAL POWER DISSIPATION versus FREQUENCY (All Four Drivers)



TYPICAL PERFORMANCE CURVES

FIGURE 7 – PROPAGATION DELAY TIME – LOW TO HIGH STATE OUTPUT versus AMBIENT TEMPERATURE

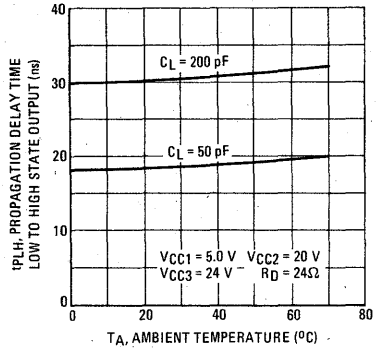


FIGURE 8 – PROPAGATION DELAY TIME – HIGH TO LOW STATE OUTPUT versus AMBIENT TEMPERATURE

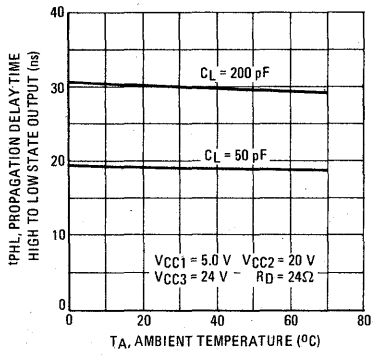


FIGURE 9 – PROPAGATION DELAY TIME – LOW TO HIGH STATE OUTPUT versus V_{CC2} SUPPLY VOLTAGE

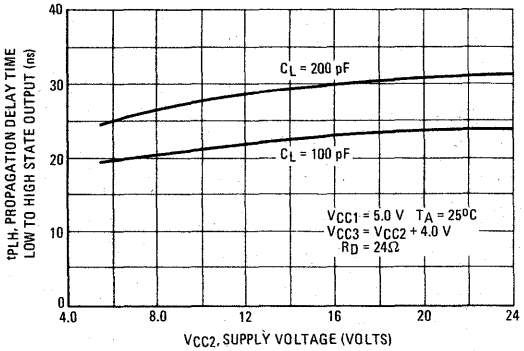


FIGURE 10 – PROPAGATION DELAY TIME – HIGH TO LOW STATE OUTPUT versus V_{CC2} SUPPLY VOLTAGE

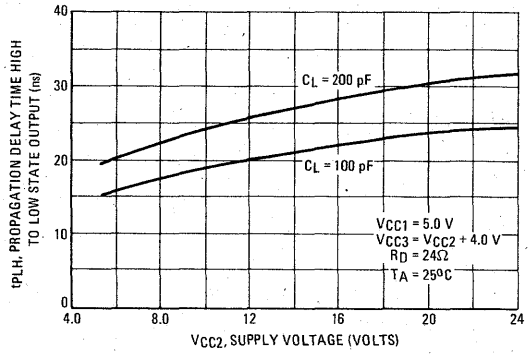


FIGURE 11 – PROPAGATION DELAY TIME – LOW TO HIGH LOGIC STATE versus LOAD CAPACITANCE

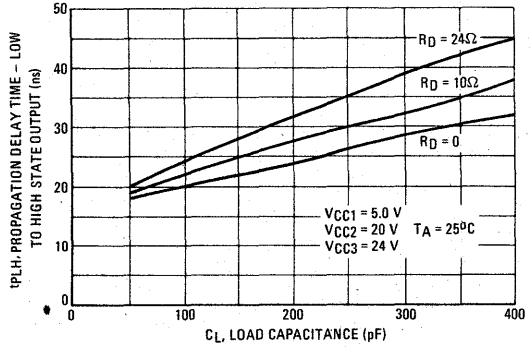
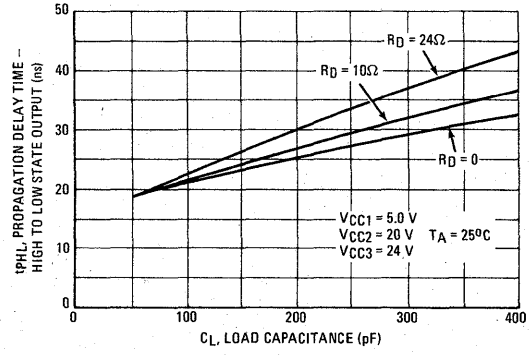


FIGURE 12 – PROPAGATION DELAY TIME – HIGH TO LOW STATE OUTPUT versus LOAD CAPACITANCE



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APPLICATIONS SUGGESTIONS

POWER CONSIDERATIONS

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the integrated circuit junction temperatures low. Electrical power dissipated in the integrated circuit is the source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature. The temperature increase depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point. The basic formula for converting power dissipation into junction temperature is:

$$T_J = T_A + P_D\ (R_{\theta JC} + R_{\theta CA}) \quad (1)$$

or

$$T_J = T_A + P_D\ (R_{\theta JA}) \quad (2)$$

where

T_J = junction temperature
T_A = ambient temperature
P_D = power dissipation
$R_{\theta JC}$ = thermal resistance, junction to case
$R_{\theta CA}$ = thermal resistance, case to ambient
$R_{\theta JA}$ = thermal resistance, junction to ambient.

Power Dissipation for the MC75365 MOS Clock Driver:

The power dissipation of the device (P_D) is dependent on the following system requirements: frequency of operation, capacitive loading, output voltage swing, and duty cycle. The variation of power dissipation with frequency and load capacitance for the MC75365 is illustrated in Figure 6. The power dissipation, when substituted into equation (2), should not yield a junction temperature, T_J, greater than T_J(max) at the maximum encountered ambient temperature. T_J(max) is specified for two integrated circuit packages in the maximum ratings section of this data sheet.

With these maximum junction temperature values, the maximum permissible power dissipation at a given ambient temperature may be determined. This can be done with equations (1) and (2) and the maximum thermal resistance values given in Table 1 shown on the following page.

TABLE 1 – THERMAL CHARACTERISTICS OF "L" AND "P" PACKAGES

PACKAGE TYPE (Mounted in Socket)	$R_{\theta JA}$ (°C/W) Still Air		$R_{\theta JC}$ (°C/W) Still Air	
	MAX	TYP	MAX	TYP
"L" (Ceramic Package)	150	100	50	27
"P" (Plastic Package)	150	100	70	40

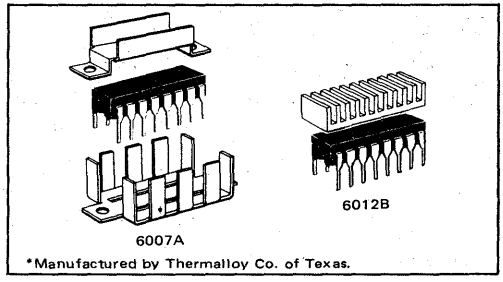
If the power dissipation determined by a given system produces a junction temperature in excess of the recommended maximum rating for a given package type, something must be done to reduce the junction temperature.

There are two methods of lowering the junction temperature without changing the system requirements. First, the ambient temperature may be reduced sufficiently to bring T_J to an acceptable value. Secondly, the $R_{\theta CA}$ term can be reduced. Lowering the $R_{\theta CA}$ term can be accomplished by increasing the surface area of the package with the addition of a heat sink or by blowing air across the package to promote improved heat dissipation.

Heat Sink Considerations:

Heat sinks come in a wide variety of sizes and shapes that will accomodate almost any IC package made. Some of these heat sinks are illustrated in Figure 13.

FIGURE 13 – THERMALLOY* HEAT SINKS



*Manufactured by Thermalloy Co. of Texas.

From Table 1, $R_{\theta JA}$(max) for the ceramic package with no heat sink and in a still air environment is 150°C/W.

For the following example the Thermalloy 6012B type heat sink, or equivalent, is chosen. With this heat sink, the $R_{\theta CA}$ for natural convection from Figure 14 is 44°C/W. From Table 1 $R_{\theta JC}$(max) = 50°C/W for the ceramic package. Therefore, the new $R_{\theta JA}$(max) with the 6012B heat sink added becomes:

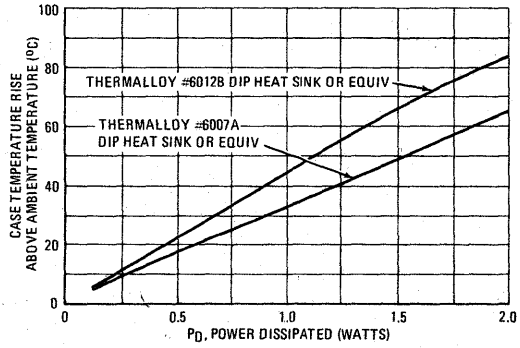
$R_{\theta JA}$(max) = 50°C/W + 44°C/W = 94°C/W.

Thus the addition of the heat sink has reduced $R_{\theta JA}$ (max) from 150°C/W down to 94°C/W. With the heat sink, the maximum power dissipation by equation (2) at T_A = +70°C is:

$$P_D = \frac{175^\circ C - 70^\circ C}{+94^\circ C/W} = 1.11 \text{ watts.}$$

This gives approximately a 60% increase in maximum power dissipation over the power dissipation which is allowable with no heat sink.

FIGURE 14 – CASE TEMPERATURE RISE ABOVE AMBIENT versus POWER DISSIPATED USING NATURAL CONVECTION



Forced Air Considerations:

As illustrated in Figure 15, forced air can be employed to reduce the $R_{\theta JA}$ term. Note, however, that this curve is expressed in terms of typical $R_{\theta JA}$ rather than maximum $R_{\theta JA}$. Maximum $R_{\theta JA}$ can be determined in the following manner:

From Table 1 the following information is known:

(a) $R_{\theta JA}$(typ) = 100°C/W

(b) $R_{\theta JC}$(typ) = 27°C/W

Since:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad (3)$$

Then:

$$R_{\theta CA} = R_{\theta JA} - R_{\theta JC} \quad (4)$$

Therefore, in still air

$R_{\theta CA}$(typ) = 100°C/W - 27°C/W = 73°C/W

From Curve 1 of Figure 14 at 500 LFPM and equation (4),

$R_{\theta CA}$(typ) = 53°C/W - 27°C/W = 26°C/W.

Thus $R_{\theta CA}$(typ) has changed from 73°C/W (still air) to 26°C/W (500 LFPM), which is a decrease in typical $R_{\theta CA}$ by a ratio of 1:2.8. Since the typical value of $R_{\theta CA}$ was reduced by a ratio of 1:2.8, $R_{\theta CA}$(max) of 100°C/W should also decrease by a ratio of 1:2.8.

This yields an $R_{\theta CA}$(max) at 500 LFPM of 36°C/W. Therefore, from equation (3):

$R_{\theta JA}$(max) = 50°C/W + 36°C/W = 86°C/W.

Therefore the maximum allowable power dissipation at 500 LFPM and T_A = +70°C is from equation (2):

$$P_D = \frac{175^\circ C - 70^\circ C}{86^\circ C/W} = 1.2 \text{ watts.}$$

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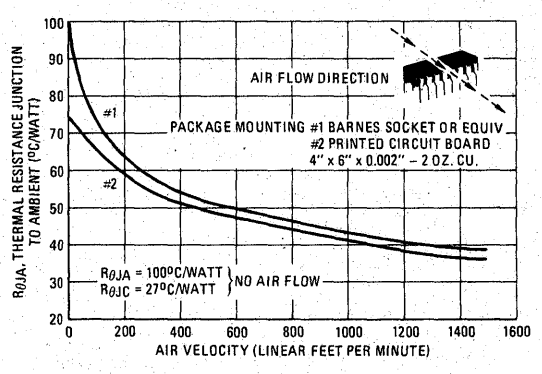
FIGURE 15 – TYPICAL THERMAL RESISTANCE ($R_{\theta JA}$) OF "L" PACKAGE versus AIR VELOCITY



Heat Sink and Forced Air Combined:

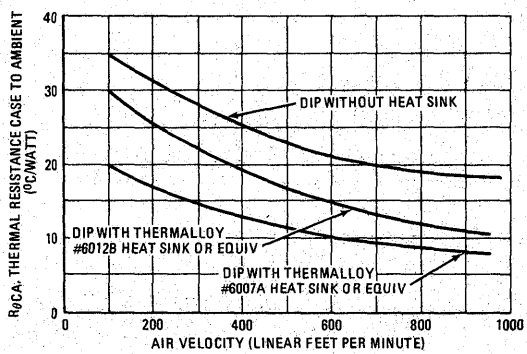
Some heat sink manufacturers provide data and curves of $R_{\theta CA}$ for still air and forced air such as illustrated in Figure 16. For example the 6012B heat sink has an $R_{\theta CA}$ = 17°C/W at 500 LFPM as noted in Figure 15. From equation (3):

Max $R_{\theta JA}$ = 50°C/W + 17°C/W = 67°C/W

From equation (2) at T_A = +70°C

$$P_D = \frac{175^\circ C - 70^\circ C}{67^\circ C/W} = 1.57 \text{ watts.}$$

FIGURE 16 – THERMAL RESISTANCE $R_{\theta CA}$ versus AIR VELOCITY



Note from Table 1 and Figure 15 that if the 16-pin ceramic package is mounted directly to the PC board (2 oz. cu. underneath), that typical $R_{\theta JA}$ is considerably less than for socket mount with still air and no heat sink. The following procedure can be employed to determine the maximum power dissipation for this condition.

Given data from Table 1:

typical $R_{\theta JA}$ = 100°C/W

typical $R_{\theta JC}$ = 27°C/W

From Curve 2 of Figure 15, $R_{\theta JA}$(typ) is 75°C/W for a PC mount and no air flow. Then the typical $R_{\theta CA}$ is 75°C/W – 27°C/W = 48°C/W. From Table 1 the typical value of $R_{\theta CA}$ for socket mount is 100°C/W – 27°C/W = 73°C/W. This shows that the PC board mount results in a decrease in typical $R_{\theta CA}$ by a ratio of 1:1.5 below the typical value of $R_{\theta CA}$ in a socket mount. Therefore, the maximum value of socket mount $R_{\theta CA}$ of 100°C/W should also decrease by a ratio of 1:1.5 when the device is mounted in a PC board. The maximum $R_{\theta CA}$ becomes:

$$R_{\theta CA} = \frac{100^\circ C/W}{1.5} = 66^\circ C/W \text{ for PC board mount}$$

Therefore the maximum $R_{\theta JA}$ for a PC mount is from equation (3).

$R_{\theta JA}$ = 50°C/W + 66°C/W = 116°C/W.

With maximum $R_{\theta JA}$ known, the maximum power dissipation can be found. If T_A = 70°C then from equation (2) the maximum power dissipation may be found to be 905 mW.

In most cases, heat sink manufacturer's publish only $R_{\theta CA}$ socket mount data. Although data for PC mounting is generally not available, this should present no problem. Note in Figure 15 that an air flow greater than 250 LFPM yields a socket mount $R_{\theta JA}$ approximately 6% greater than for a PC mount. Therefore, the socket mount data can be used for a PC mount with a slightly greater safety factor. Also it should be noted that thermal resistance measurements can vary widely. These measurement variations are due to the dependency of $R_{\theta CA}$ of the type environment and measurement techniques employed. For example, $R_{\theta CA}$ would be greater for an integrated circuit mounted on a PC board with little or no ground plane versus one with a substantial ground plane. Therefore, if the maximum calculated junction temperature is on the border line of being too high for a given system application, then thermal resistance measurements should be done on the system to be absolutely certain that the maximum junction temperature is not exceeded.

ORDERING INFORMATION

Device	Temperature Range	Package
MC75358L	0°C to +70°C	Ceramic DIP
MC75358P	0°C to +70°C	Plastic DIP
MC75368L	0°C to +70°C	Ceramic DIP
MC75368P	0°C to +70°C	Plastic DIP

MC75368
MC75358

Specifications and Applications Information

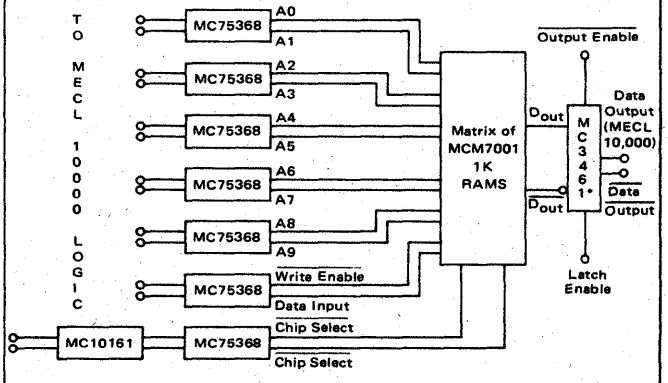
DUAL MECL-to-MOS DRIVERS

The MC75368 and MC75358 are dual MECL-to-MOS driver and interface circuits. The devices accept standard MECL 10,000 and IBM grounded-reference ECL input signals and create high-current and high-voltage output levels suitable for driving MOS circuits. Specifically, they may be used to drive address, control, and timing inputs for several types of MOS RAMs including high-speed MCM7001 1K NMOS RAM. The devices may also be used as MECL-to-MTTL translators.

These two devices differ in that the MC75368 is optimized for higher voltage capability and the MC75358 version is made to operate at somewhat reduced maximum voltages.

- Dual MECL-to-MOS Driver
- Dual MECL-to-MTTL Driver
- Versatile Interface Circuit for Use Between MECL and High-Current, High-Voltage Systems

FIGURE 1 – TYPICAL APPLICATION WITH MCM7001 1K NMOS RAM
(See Figure 8 and 9 for details)

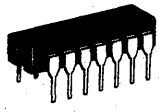


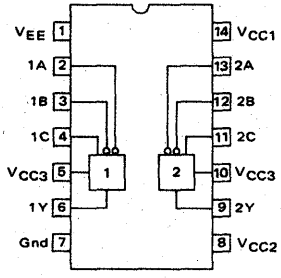
*MC3461 Dual Sense Amplifier to be announced 1st Quarter 1975.

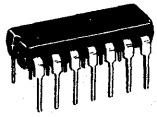
DUAL MECL-to-MOS DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116







P SUFFIX
PLASTIC PACKAGE
CASE 646

FUNCTION TABLE

Input Voltage Conditions		Output
Differential	Logic Level	
(More positive of A or B) –C	A B C	Y
($V_{ID} \geq 150$ mV)	L H L H L H H H L	L
(–150 mV ≤ V_{ID} ≤ 150 mV)	X X X	Indeterminate
($V_{ID} \leq$ –150 mV)	L L H	H

H = high logic level, L = low logic level,
X = irrelevant

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MAXIMUM RATINGS (Unless otherwise noted, voltages measured with respect to GND terminals, $T_A = 25^oC$.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC1}	-0.5 to 7.0	Vdc
MC75368 MC75358	V_{CC2}	-0.5 to 22 -0.5 to 18	Vdc
MC75368 MC75358	V_{CC3}	-0.5 to 30 -0.5 to 24	Vdc
	V_{EE}	-8.0 to 0.5	Vdc
Most Negative of V_{CC1}, V_{CC2}, or V_{CC3} with respect to V_{EE}	–	-0.5	Vdc
Input Voltage	V_I	-8.0 to 0.5	Vdc
Inter-Input Voltage(1)	–	5.5	Vdc
Most negative Input Voltage with respect to V_{EE}	$V_I - V_{EE}$	-5.0	Vdc
Power Dissipation (Package Limitation)			
Ceramic Package @ $T_A = 25^oC$	P_D	1000	mW
Derate above $T_A = 25^oC$	$1/R_{\theta JA}$	6.6	mW/°C
Plastic Package @ $T_A = 25^oC$	P_D	830	mW
Derate above $T_A = 25^oC$	$1/R_{\theta JA}$	6.6	mW/°C
Ceramic Package @ $T_C = 25^oC$	P_D	3.0	Watts
Derate above $T_C = 25^oC$	$1/R_{\theta JC}$	20	mW/°C
Plastic Package @ $T_C = 25^oC$	P_D	1.8	Watts
Derate above $T_C = 25^oC$	$1/R_{\theta JC}$	14	mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	-65 to 150	°C

(1) With respect to any pair of inputs to either of the input gates.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	MC75358			MC75368			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltages	V_{CC1}	4.75	5.0	5.25	4.75	5.0	5.25	V
	V_{CC2}	4.75	16	18	4.75	20	22	V
	V_{CC3}	V_{CC2}	20	22	V_{CC2}	24	28	V
	$V_{CC3} - V_{CC2}$	0	4.0	10	0	4.0	10	V
	V_{EE}	-4.68	-5.2	-5.72	-4.68	-5.2	-5.72	V
Operating Ambient Temperature Range	T_A	0	–	70	0	–	70	°C
DEFINITION OF INPUT LOGIC LEVELS								
Input Voltage – High Logic State (Any Input) (1)	V_{IH}	-1.5	–	-0.7	-1.5	–	-0.7	V
Input Voltage – Low Logic State (Any Input) (1)	V_{IL}	V_{EE}	–	V_{IH}-150	V_{EE}	–	V_{IH}-150	mV
Input Differential Voltage – High Logic State (2)	V_{IDH}	150	–	–	150	–	–	mV
Input Differential Voltage – Low Logic State (2)	V_{IDL}	-150	–	–	-150	–	–	mV

(1) The definition of these Logic Levels use Algebraic System of notation.

(2) The input differential voltage is measured from the more positive inverting input (A or B) with respect to the non-inverting input (C) of the same gate.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply over recommended power supply and temperature ranges. Typical values measured at V_{CC1} = 5.0 V, V_{EE} = -5.2 V, T_A = 25°C and V_{CC2} = 20, V_{CC3} = 24 V for MC75368 and V_{CC2} = 16, V_{CC3} = 20 V for MC75358.

Characteristic	Symbol	MC75358 Min	MC75358 Typ	MC75358 Max	MC75368 Min	MC75368 Typ	MC75368 Max	Unit
Output Voltage — High Logic State								V
(V_{CC3} = V_{CC2} + 3.0 V, V_{IDL} = -150 mV, I_{OH} = -100 μA)	V_{OH1}	V_{CC2} - 0.3	V_{CC2} - 0.1	—	V_{CC2} - 0.3	V_{CC2} - 0.1	—	
(V_{CC3} = V_{CC2} + 3.0 V, V_{IDL} = -150 mV, I_{OH} = -10 mA)	V_{OH2}	V_{CC2} - 1.2	V_{CC2} - 0.9	—	V_{CC2} - 1.2	V_{CC2} - 0.9	—	
(V_{CC3} = V_{CC2}, V_{IDL} = -150 mV, I_{OH} = -50 μA)	V_{OH3}	V_{CC2} - 1.0	V_{CC2} - 0.7	—	V_{CC2} - 1.0	V_{CC2} - 0.7	—	
(V_{CC3} = V_{CC2}, V_{IDL} = -150 mV, I_{OH} = -10 mA)	V_{OH4}	V_{CC2} - 2.3	V_{CC2} - 1.8	—	V_{CC2} - 2.3	V_{CC2} - 1.8	—	
Output Voltage — Low Logic State								V
(V_{IDH} = 150 mV, I_{OL} = 10 mA)	V_{OL1}	—	0.15	0.3	—	0.15	0.3	
(V_{IDH} = 150 mV, I_{OL} = 30 mA)	V_{OL2}							
10 V ≤ V_{CC3} ≤ 22 V		—	0.2	0.4	—	—	—	
10 V ≤ V_{CC2} ≤ 28 V		—	—	—	—	0.2	0.4	
Output Clamp Voltage (V_{IDH} = 500 mV, I_{OC} = 20 mA)	V_{OC}	—	—	V_{CC2}+1.5 V	—	—	V_{CC2}+1.5 V	V
Input Current — High Logic State (V_{EE} = -5.72 V, V_{IL} = -5.72 V, V_{IH} = -0.7 V)	I_{IH}	—	300	800	—	300	800	μA
Input Current — Low Logic State								μA
(V_{IH} = -0.7 V, V_{IL} = -2.0 V)	I_{IL1}	—	—	-10	—	—	-10	
(V_{EE} = -5.72 V, V_{IH} = -0.7 V, V_{IL} = -5.72 V)	I_{IL2}	—	—	-100	—	—	-100	
Power Supply Current — Both Outputs High Logic State (V_{CC} = 5.25 V, V_{EE} = -5.72 V, $V_{IL(A)}$ and (B) = -2.0 V, $V_{IH(C)}$ = -0.7 V, I_{OH} = 0)								
MC75368 — V_{CC2} = 22 V, V_{CC3} = 26 V	$I_{CC1(H)}$	—	21	38	—	21	38	mA
MC75358 — V_{CC2} = 18 V, V_{CC3} = 22 V	$I_{CC2(H)}$	—	-1.1	+0.25 -1.6	—	-1.1	+0.25 -1.6	mA
	$I_{CC3(H)}$	—	0.6	1.0	—	0.6	1.0	mA
	$I_{EE(H)}$	—	-21	-38	—	-21	-38	mA
Power Supply Current — Both Outputs Low Logic State (V_{CC1} = 5.25 V, V_{EE} = -5.72 V, $V_{IH(A)}$ and (B) = -0.7 V, $V_{IL(C)}$ = -2.0 V, I_{OL} = 0)								
MC75368 — V_{CC2} = 22 V, V_{CC3} = 28 V	$I_{CC1(L)}$	—	13	24	—	13	24	mA
MC75358 — V_{CC2} = 18 V, V_{CC3} = 22 V	$I_{CC2(L)}$	—	0.5	1.0	—	0.5	1.0	mA
	$I_{CC3(L)}$	—	3.0	5.7	—	4.0	7.0	mA
	$I_{EE(L)}$	—	-21	-38	—	-21	-38	mA
Power Supply Current — Both Outputs High Logic State (V_{CC1} = 5.25 V, V_{EE} = -5.72 V, $V_{IL(A)}$ and (B) = -2.0 V, $V_{IH(C)}$ = -0.7 V, I_{OL} = 0)								
MC75368 — V_{CC2} = 22 V, V_{CC3} = 22 V	$I_{CC2(H)}$	—	—	0.25	—	—	0.25	mA
MC75358 — V_{CC2} = 18 V V_{CC3} = 18 V	$I_{CC3(H)}$	—	—	0.25	—	—	0.25	mA
Power Supply Current — Stand By Condition (V_{CC1} = 0 V, V_{EE} = 0 V, $V_{IH(A)}$ and (B) = -0.7 V, $V_{IL(C)}$ = -2.0 V, I_{OL} = 0)								
MC75368 — V_{CC2} = 22 V, V_{CC3} = 22 V	$I_{CC2(S)}$	—	—	0.25	—	—	0.25	mA
MC75358 — V_{CC2} = 18 V, V_{CC3} = 18 V	$I_{CC3(S)}$	—	—	0.25	—	—	0.25	mA

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SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC1} = 5.0 V, V_{EE} = -5.2 V, T_A = 25°C and V_{CC2} = 20 V for MC75368 and V_{CC2} = 16 V for MC75358)

Characteristic	Symbol	MC75358 Min	MC75358 Typ	MC75358 Max	MC78368 Min	MC78368 Typ	MC78368 Max	Unit
Delay Time – Low to High Output Logic Level	t_{DLH}							ns
(V_{CC3} = 24 V)		–	–	–	–	12	24	
(V_{CC3} = 20 V)		–	13	24	–	13	25	
(V_{CC3} = 16 V)		–	14	26	–	–	–	
Delay Time – High to Low Output Logic Level	t_{DHL}							ns
(V_{CC3} = 24 V)		–	–	–	–	13	24	
(V_{CC3} = 20 V)		–	13	24	–	15	26	
(V_{CC3} = 16 V)		–	15	26	–	–	–	
Transition Time, Low-to-High Output Logic Level	t_{TLH}							ns
(V_{CC3} = 24 V)		–	–	–	–	19	30	
(V_{CC3} = 20 V)		–	17	29	–	20	30	
(V_{CC3} = 16 V)		–	18	30	–	–	–	
Transition Time, High-to-Low Output Logic Level	t_{THL}							ns
(V_{CC3} = 24 V)		–	–	–	–	20	33	
(V_{CC3} = 20 V)		–	17	29	–	18	30	
(V_{CC3} = 16 V)		–	16	29	–	–	–	
Propagation Delay Time, Low-to-High Logic Level	t_{PLH}							ns
(V_{CC3} = 24 V)		–	–	–	–	31	54	
(V_{CC3} = 20 V)		–	30	53	–	33	55	
(V_{CC3} = 16 V)		–	32	56	–	–	–	
Propagation Delay Time, High-to-Low Logic Level	t_{PHL}							ns
(V_{CC3} = 24 V)		–	–	–	–	33	57	
(V_{CC3} = 20 V)		–	30	53	–	33	56	
(V_{CC3} = 16 V)		–	31	55	–	–	–	

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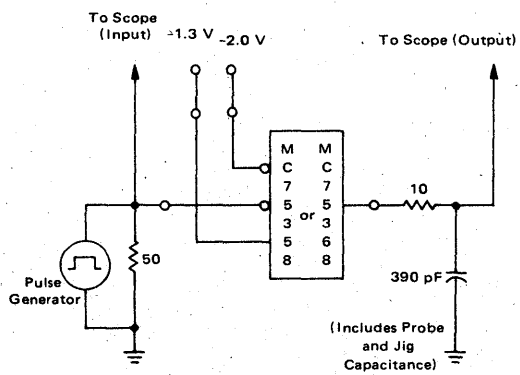
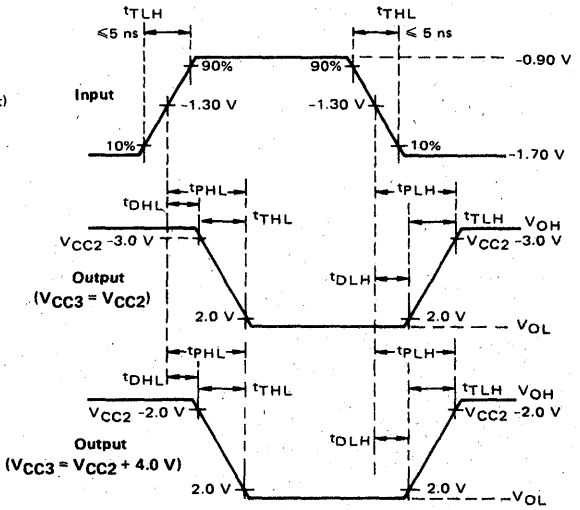
FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



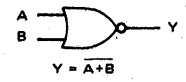
The pulse generator has the following characteristics:
PRR = 1 MHz. $z_o \approx 50\ \Omega$.
Duty Cycle = 50%

FIGURE 3 – SWITCHING TIMES WAVEFORM



APPLICATIONS INFORMATION
MODES OF OPERATION

FIGURE 4 – POSITIVE-NOR GATE

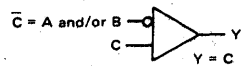


FUNCTION TABLE

CONFIGURATION	INPUTS A	B	C	OUTPUT Y
C at V_{BB}	L	L	V_{BB}	H
	H	X	V_{BB}	L
	X	H	V_{BB}	L

H – High Level, L – Low Level, X – Irrelevant
V_{BB} – Reference Supply voltage for MECL 10,000.

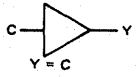
FIGURE 5 – DIFFERENTIAL MECL LINE RECEIVER



FUNCTION TABLE

CONFIGURATION	INPUTS A	B	C	OUTPUT Y
A and B connected together	H	H	L	L
	L	L	H	H
A not used but connected low	L	H	L	L
	L	L	H	H
B not used but connected low	H	L	L	L
	L	L	H	H

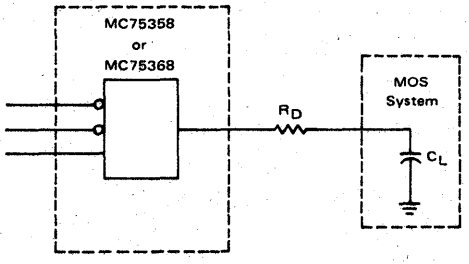
FIGURE 6 – NON-INVERTING GATE



FUNCTION TABLE

CONFIGURATION	INPUTS A	B	C	OUTPUT Y
A and B at V_{BB}	V_{BB}	V_{BB}	L	L
	V_{BB}	V_{BB}	H	H
A at V_{BB}, B connected low	V_{BB}	L	L	L
	V_{BB}	L	H	H
B at V_{BB}, A connected low	L	V_{BB}	L	L
	L	V_{BB}	H	H

FIGURE 7 – USE OF DAMPING RESISTOR TO REDUCE OR ELIMINATE OUTPUT TRANSIENT OVERSHOOT IN CERTAIN MC75358 AND MC75368 APPLICATIONS



Note: $R_D \approx 10\Omega$ to 30Ω (optional)

The MC75368 and MC75358 are identical except that the MC75368 version has been selected for slightly higher voltage capability. The two devices are interchangeable in most applications. Both can operate over a wide range of V_{CC2} and V_{CC3} supply voltages.

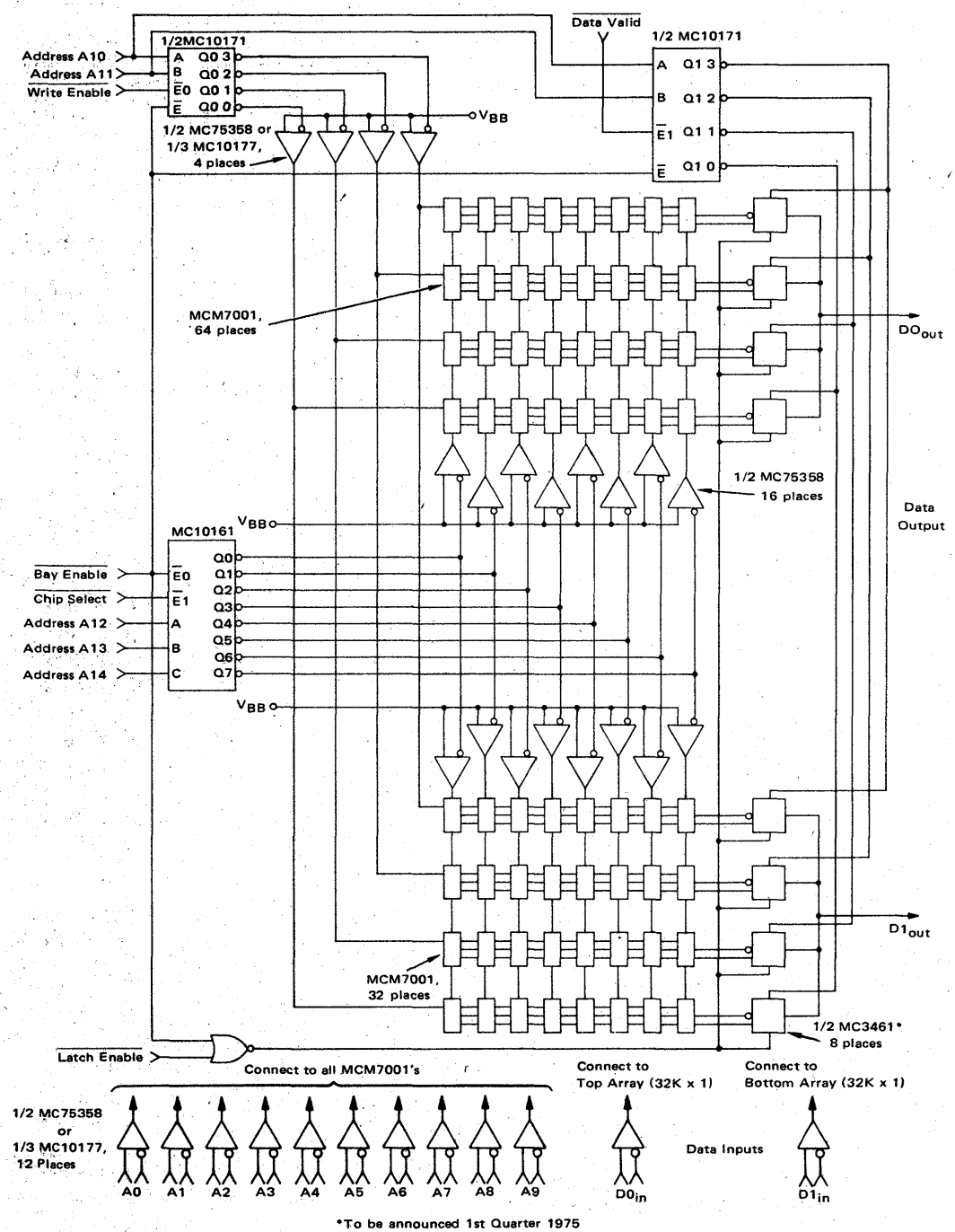
The need for four separate power supplies V_{CC1}, V_{CC2}, V_{CC3} and V_{EE} can be avoided in many cases by tying V_{CC2} to V_{CC3}. However, performance advantages can be obtained by connecting either one or both V_{CC3} pins to an additional power supply of higher voltage than V_{CC2}. Both V_{CC3} pins do not have to be held at the same voltage. For MECL-to-TTL level converter applications both V_{CC2} and V_{CC3} are generally connected to a +5.0 V power source.

By providing two out-of-phase (A and B) inputs and one in-phase (C) input, each gate can be used as positive NOR, or as a inverting or non-inverting gate. This flexibility is achieved by connecting an externally supplied MECL 10,000 Series reference supply voltage (V_{BB}) to the appropriate input as shown in Figures 4 thru 6. An unused out-of-phase input should be tied low or connected to the other out-of-phase input of the same gate. The required V_{BB} voltage source may be obtained from MECL 10,000 Series devices such as the MC10115 line receiver, or by connecting the output of a MECL 10,000 gate, like the MC10102, to the respective out-of-phase inputs (as an example connect pins 4 and 5 to 2 of the MC10102 to obtain a V_{BB} reference voltage).

When driven differentially, the MC75368 and MC75358 may be used as a differential MECL line receiver, without the need for the V_{BB} reference voltage.

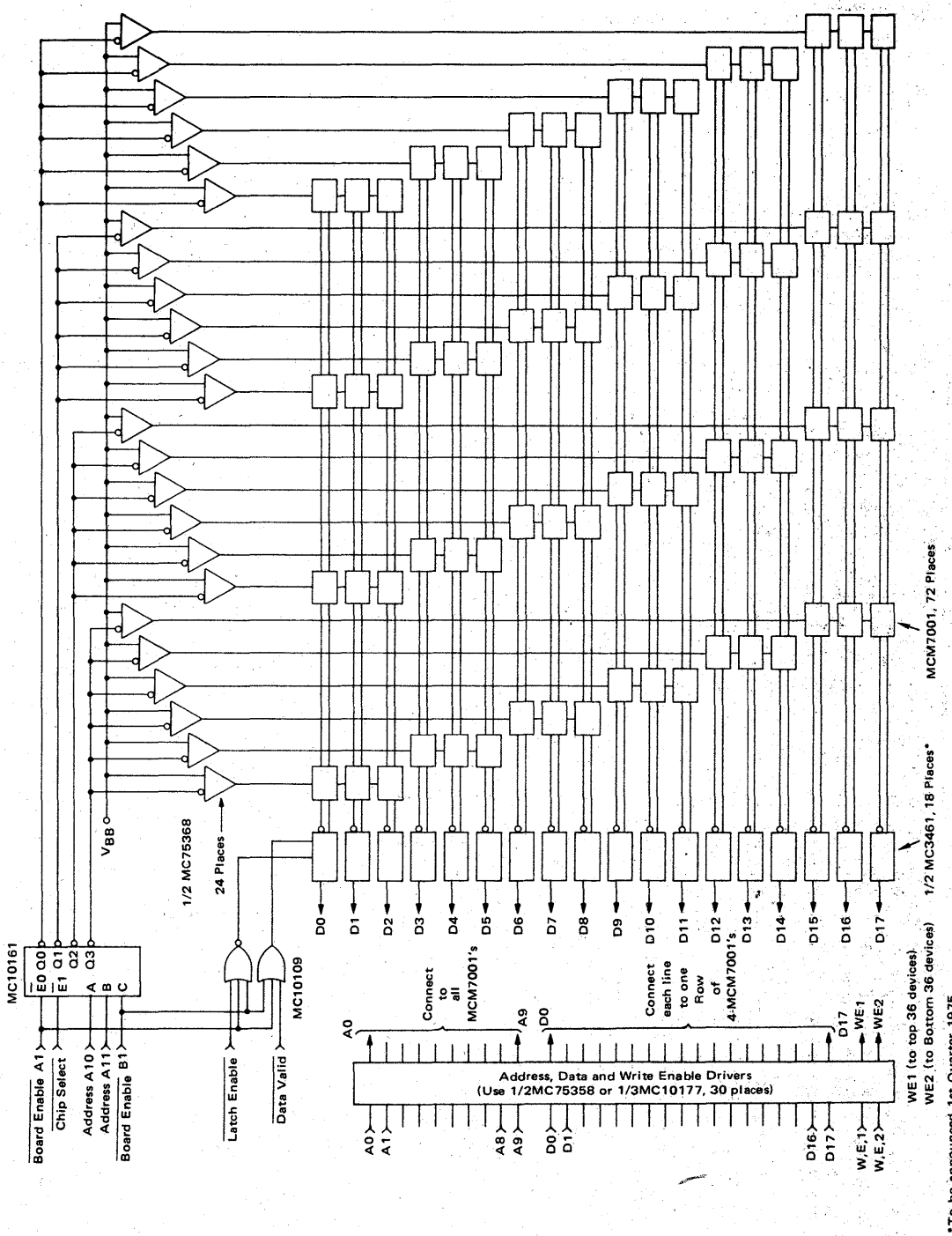
Undesirable output transient overshoot due to load or wiring inductance and the fast switching speeds of the MC75368 and MC75358 can be eliminated or reduced by adding a small amount of series resistance. The value of this damping resistance is dependent on specific load characteristics and switching speed but typical values lie in the range of 10 to 30 ohms. This is illustrated in Figure 7.

FIGURE 8 – 32K x 2 MEMORY BOARD (MECL SYSTEM)



*To be announced 1st Quarter 1975

FIGURE 9 – 4K x 18 MEMORY BOARD (MECL SYSTEM)



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ORDERING INFORMATION

Device	Temperature Range	Package
MC75450L	0°C to +70°C	Ceramic DIP
MC75450P	0°C to +70°C	Plastic DIP

MC75450

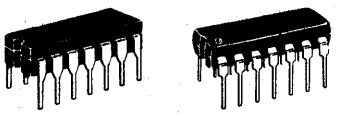
DUAL PERIPHERAL POSITIVE "AND" DRIVER

The MC75450 is a versatile device designed for use as a general-purpose dual interface circuit in MDTL and MTTL type systems. This device features two standard MTTL gates and two noncommitted, high-current, high-voltage NPN transistors. Typical applications include relay and lamp drivers, power drivers, MOS and memory drivers.

- MDTL and MTTL Compatibility
- 300 mA Output Current Drive Capability (each transistor)
- Separate Gate and Output Transistor for Maximum Design Flexibility
- High Output Breakdown Voltage: V_{CER} = 30 Volts minimum

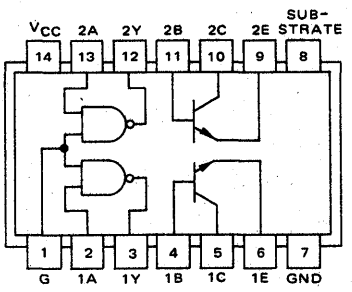
DUAL PERIPHERAL POSITIVE "AND" DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUITS



L SUFFIX CERAMIC PACKAGE CASE 632 (TO-116)

P SUFFIX PLASTIC PACKAGE CASE 646



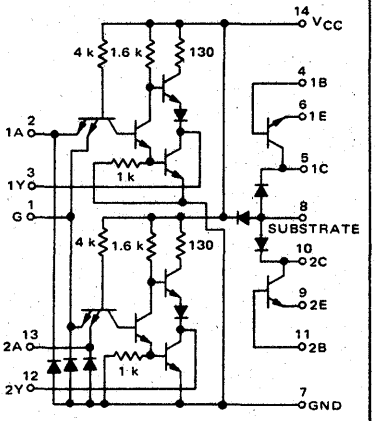
Positive Logic: Y = $\overline{AG}$ (gate only)
C = AG (gate and transistor)

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage (See Note 1)	V_{CC}	+7.0	Vdc
Input Voltage (See Note 1)	V_{in}	5.5	Vdc
V_{CC}-to-Substrate Voltage		35	Vdc
Collector-to-Substrate Voltage		35	Vdc
Collector-Base Voltage	V_{CB}	35	Vdc
Collector-Emitter Voltage (See Note 2)	V_{CE}	30	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current (continuous) (See Note 3)		300	mA
Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above T_A = +25°C	P_D	 830 6.6	 mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 ohms.
3. Both halves of these dual circuits may conduct the rated current simultaneously.

CIRCUIT SCHEMATIC



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RECOMMENDED OPERATING CONDITIONS (See Note 4)

Characteristic	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc

Note 4. The substrate, pin 8, must always be at the most negative device voltage for proper operation.

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic		Symbol	Test Fig.	Min	Typ*	Max	Unit
MTTL GATES							
High-Level Input Voltage		V_{IH}	1	2.0	–	–	Vdc
Low-Level Input Voltage		V_{IL}	2	–	–	0.8	Vdc
High-Level Output Voltage (V_{CC} = 4.5 V, V_{IL} = 0.8 V, I_{OH} = -400 μA)		V_{OH}	2	2.4	3.3	–	Vdc
Low-Level Output Voltage (V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OL} = 16 mA)		V_{OL}	1	–	0.22	0.4	Vdc
High-Level Input Current		I_{IH}	3				
(V_{CC} = 5.25 V, V_{in} = 2.4 V)	Input A			–	–	40	μA
	Input G			–	–	80	
(V_{CC} = 5.25 V, V_{in} = 5.5 V)	Input A			–	–	1.0	mA
	Input G			–	–	2.0	
Low-Level Input Current		I_{IL}	4				mA
(V_{CC} = 5.25 V, V_{in} = 0.4 V)	Input A			–	–	-1.6	
	Input G			–	–	-3.2	
Short-Circuit Output Current** (V_{CC} = 5.25 V)		I_{OS}	5	-18	–	-55	mA
Supply Current			6				mA
High-Level Output (V_{CC} = 5.25 V, V_{in} = 0)		I_{CCH}		–	2.0	4.0	
Low-Level Output (V_{CC} = 5.25 V, V_{in} = 5.0 V)		I_{CCL}		–	6.0	11	
Input Clamp Voltage (V_{CC} = 4.75 V, I_{in} = -12 mA)		V_{in}	4	–	–	-1.5	V

OUTPUT TRANSISTORS

Characteristic	Symbol	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage (I_C = 100 μA, I_E = 0)	V_{CBO}	35	–	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 100 μA, R_{BE} = 500 ohms)	V_{CER}	30	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μA, I_C = 0)	V_{EBO}	5.0	–	–	Vdc
Static Forward Transfer Ratio (See Note 5)	h_{FE}				
(V_{CE} = 3.0 V, I_C = 100 mA, T_A = +25°C)		25	–	–	
(V_{CE} = 3.0 V, I_C = 300 mA, T_A = +25°C)		30	–	–	
(V_{CE} = 3.0 V, I_C = 100 mA, T_A = 0°C)		20	–	–	
(V_{CE} = 3.0 V, I_C = 300 mA, T_A = 0°C)		25	–	–	
Base-Emitter Voltage (See Note 5)	V_{BE}				Vdc
(I_B = 10 mA, I_C = 100 mA)		–	0.85	1.0	
(I_B = 30 mA, I_C = 300 mA)		–	1.05	1.2	
Collector-Emitter Saturation Voltage (See Note 5)	$V_{CE(sat)}$				Vdc
(I_B = 10 mA, I_C = 100 mA)		–	0.25	0.4	
(I_B = 30 mA, I_C = 300 mA)		–	0.5	0.7	

Note 5. These parameters must be measured using pulse techniques; t_w = 300 μs, duty cycle ≤ 2%.
*All typical values at V_{CC} = 5.0 V, T_A = +25°C.
**Not more than one output should be shorted at a time.

5

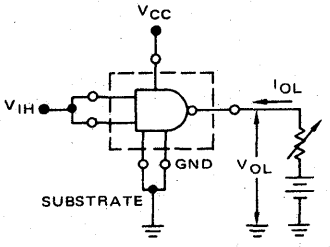
SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
MTTL GATES						
Propagation Delay Time (C_L = 15 pF, R_L = 400 ohms)		7				ns
Low-to-High-Level Output	t_{PLH}		–	14	–	
High-to-Low-Level Output	t_{PHL}		–	6.0	–	
OUTPUT TRANSISTORS ‡						
Switching Times (I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = -40 mA, $V_{BE(off)}$ = -1.0 V, C_L = 15 pF, R_L = 50 ohms)		8				ns
Delay Time	t_d		–	9.0	–	
Rise Time	t_r		–	11	–	
Storage Time	t_s		–	14	–	
Fall Time	t_f		–	8.0	–	
GATES AND TRANSISTORS COMBINED #						
Propagation Delay Time (I_C = 200 mA, C_L = 15 pF, R_L = 50 ohms)		9				ns
Low-to-High-Level Output	t_{PLH}		–	21	–	
High-to-Low Level Output	t_{PHL}		–	16	–	
Transition Time# (I_C = 200 mA, C_L = 15 pF, R_L = 50 ohms)		9				ns
Low-to-High-Level Output	t_{TLH}		–	7.0	–	
High-to-Low-Level Output	t_{THL}		–	8.0	–	

#Voltage and current values are nominal; exact values vary slightly with transistors parameters.

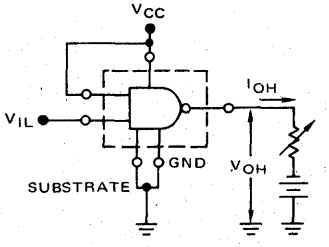
DC TEST CIRCUITS FOR MTTL GATES

FIGURE 1 – V_{IH}, V_{OL}



Both inputs are tested simultaneously.

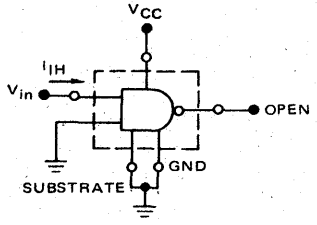
FIGURE 2 – V_{IL}, V_{OH}



Each input is tested separately.

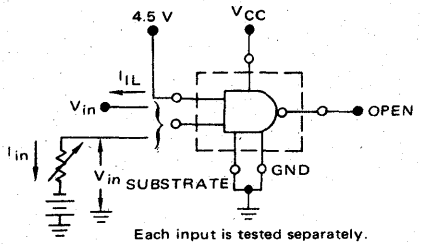
(Arrows indicate actual direction of current flow. Current into a terminal is a positive value.)

FIGURE 3 – I_{IH}



Each input is tested separately.

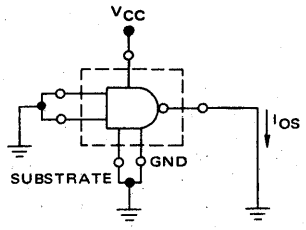
FIGURE 4 – I_{IL}, V_{in}



Each input is tested separately.

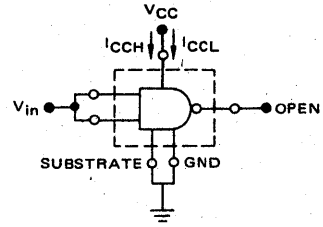
DC TEST CIRCUITS FOR MTTL GATES (continued)

FIGURE 5 – I_{OS}



Each gate is tested separately

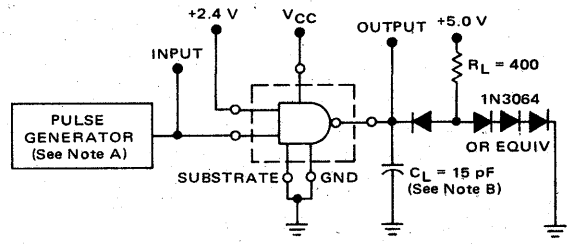
FIGURE 6 – I_{CCH}, I_{CCL}



Both gates are tested simultaneously.

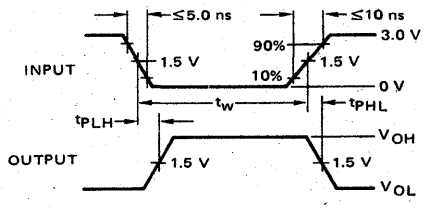
(Arrows indicate actual direction of current flow. Current into a terminal is a positive value.)

FIGURE 7 – PROPAGATION DELAY TIMES, EACH GATE



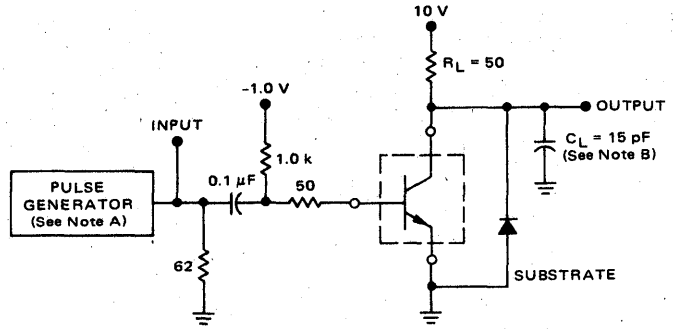
NOTES: A. The pulse generator has the following characteristics: $t_w = 0.5\ \mu s$, PRR = 1.0 MHz, $z_o \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS



TEST CIRCUITS (continued)

FIGURE 8 – SWITCHING TIMES, EACH TRANSISTOR



NOTES: A. The pulse generator has the following characteristics: t_w = 0.3 μs, duty cycle ≤ 1%, $z_o \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS

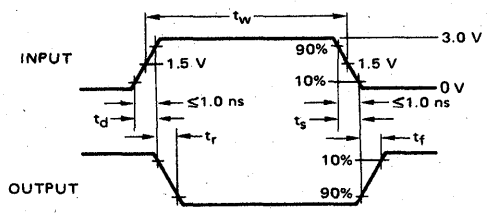
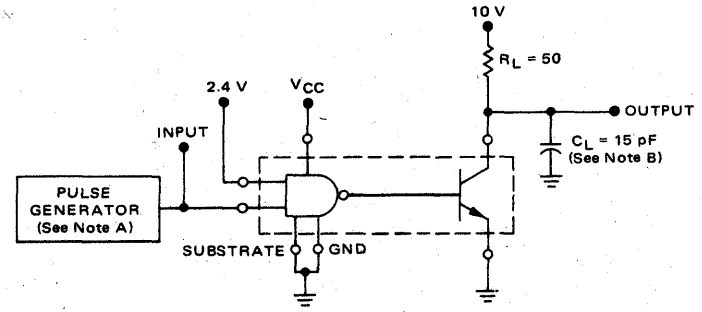
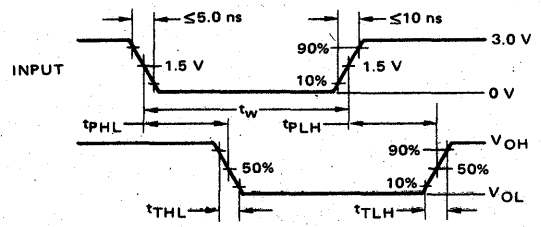


FIGURE 9 – SWITCHING TIMES, GATE AND TRANSISTOR



NOTES: A. The pulse generator has the following characteristics: t_w = 0.5 μs, PRR = 1.0 MHz, $z_o \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC75451P	SN75451BP	0°C to +70°C	Plastic DIP
MC75451U	—	0°C to +70°C	Ceramic DIP
MC75452P	SN75452BP	0°C to +70°C	Plastic DIP
MC75452U	—	0°C to +70°C	Ceramic DIP
MC75453P	SN75453BP	0°C to +70°C	Plastic DIP
MC75453U	—	0°C to +70°C	Ceramic DIP
MC75454P	SN75454BP	0°C to +70°C	Plastic DIP
MC75454U	—	0°C to +70°C	Ceramic DIP

MC75451
MC75452
MC75453
MC75454

DUAL PERIPHERAL DRIVERS

These versatile devices are useful for interfacing digital logic to industrial electronic systems. They are useful as lamp drivers, relay drivers, logic buffers, line drivers, or MOS drivers.

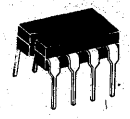
Each of these devices consists of a pair of MTTL gates with the output of each gate internally connected to the base of a transistor.

MC75451 provides the AND function
MC75452 provides the NAND function
MC75453 provides the OR function
MC75454 provides the NOR function

- 300 mA Output Current Capability
- Output Breakdown Voltage — 30 V Min
- MTTL compatible Inputs

DUAL PERIPHERAL DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUITS

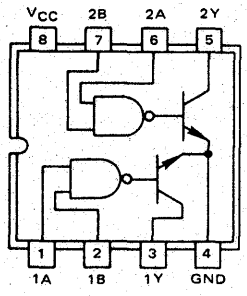


U SUFFIX
CERAMIC PACKAGE
CASE 693

P SUFFIX
PLASTIC PACKAGE
CASE 626

5

MC75451 — Positive AND



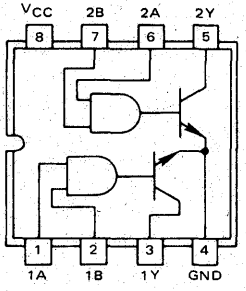
Positive Logic: Y = AB

TRUTH TABLE

A	B	Y
L	L	L ("on" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	H ("off" state)

H = high level, L = low level.

MC75452 — Positive NAND



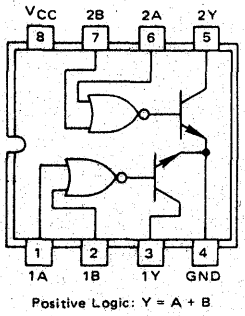
Positive Logic: Y = $\overline{AB}$

TRUTH TABLE

A	B	Y
L	L	H ("off" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	L ("on" state)

H = high level, L = low level

MC75453 — Positive OR



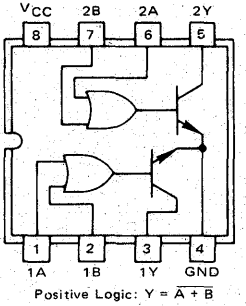
Positive Logic: Y = A + B

TRUTH TABLE

A	B	Y
L	L	L ("on" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	H ("off" state)

H = high level, L = low level

MC75454 — Positive NOR



Positive Logic: Y = $\overline{A + B}$

TRUTH TABLE

A	B	Y
L	L	H ("off" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	L ("on" state)

H = high level, L = low level.

MAXIMUM RATINGS (T_A = 0°C to 70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage(1)	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Interemitter Voltage(2)	–	5.5	Vdc
Output Voltage(3)	V_O	30	Vdc
Output Current(4)	I_O	300	mA
Power Dissipation @ T_A = 25°C Derate above T_A = +25°C	P_D	830 6.6	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

(1) Voltage values are with respect to network ground terminal.
(2) This is the voltage between two emitters of a multiple-emitter transistor.
(3) This is the maximum voltage which should be applied to any output when it is in the "off" state.
(4) Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for 4.75 ≥ V_{CC} ≥ 5.25 V and 0°C ≤ T_A ≤ 70°C)

Characteristic		Figure	Symbol	Min	Typ (1)	Max	Unit
Input Voltage – High Logic State		1,2	V_{IH}	2.0	–	–	Vdc
Input Voltage – Low Logic State		1,2	V_{IL}	–	–	0.8	Vdc
Input Clamp Voltage (V_{CC} = 4.75 V, I_I = -12 mA)		4	V_I	–	-1.2	-1.5	Vdc
Output Current – High Logic State (V_{CC} = 4.75 V, V_{OH} = 30 V, V_{IH} = 2.0 V) (V_{CC} = 4.75 V, V_{OH} = 30 V, V_{IL} = 0.8 V)	MC75451, MC75453 MC75452, MC75454	2	I_{OH}	–	–	100	μA
Output Voltage – Low Logic State (V_{CC} = 4.75 V, V_{IL} = 0.8 V) (V_{CC} = 4.75 V, V_{IH} = 2.0 V) (I_{OL} = 100 mA) (I_{OL} = 300 mA)	 MC75451, MC75453 MC75452, MC75454 	1	V_{OL}	 – –	 0.25 0.5	 0.4 0.7	Vdc
Input Current – High Logic State (V_{CC} = 5.25 V, V_I = 2.4 V) (V_{CC} = 5.25 V, V_I = 5.5 V)		3	I_{IH}	 – –	 – –	 40 1.0	 μA mA
Input Current – Low Logic State (V_{CC} = 5.25 V, V_I = 0.4 V)		4	I_{IL}	–	-1.0	-1.6	mA
Power Supply Current – Output High Logic State (V_{CC} = 5.25 V, V_I = 5.0 V) (V_{CC} = 5.25 V, V_I = 0) (V_{CC} = 5.25 V, V_I = 5.0 V) (V_{CC} = 5.25 V, V_I = 0)	 MC75451 MC75452 MC75453 MC75454	5	I_{CCH}	 – – – –	 7.0 11 8.0 13	 11 14 11 17	mA
Power Supply Current – Output Low Logic State (V_{CC} = 5.25 V, V_I = 0) (V_{CC} = 5.25 V, V_I = 5.0 V) (V_{CC} = 5.25 V, V_I = 0) (V_{CC} = 5.25 V, V_I = 5.0 V)	 MC75451 MC75452 MC75453 MC75454	5	I_{CCL}	 – – – –	 52 56 54 61	 65 71 68 79	mA

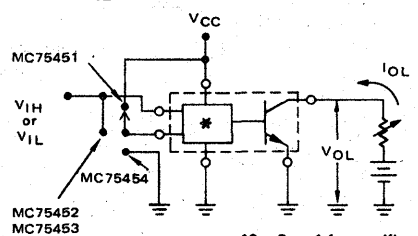
(1) Typical Values Measured with V_{CC} = 5.0 V, T_A = 25°C.

TEST CIRCUITS

(Current into terminal is shown as a positive value.
Arrows indicate actual direction of current flow.)

FIGURE 1 – V_{OL}

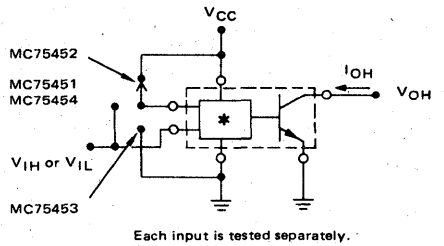
V_{IH} – MC75452 and MC75454
V_{IL} – MC75451 and MC75453



*See Page 1 for specific gate type.

FIGURE 2 – I_{OH}

V_{IH} – MC75451 and MC75453
V_{IL} – MC75452 and MC75454



Each input is tested separately.

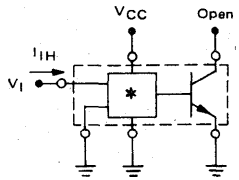
SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time ($I_O \approx 200$ mA, C_L = 15 pF, R_L = 50 ohms)						
MC75451						
Low-to-High-Level Output	t_{PLH}	6	–	17	–	ns
High-to-Low-Level Output	t_{PHL}		–	18	–	
MC75452						
Low-to-High-Level Output	t_{PLH}	6	–	18	–	ns
High-to-Low-Level Output	t_{PHL}		–	16	–	
MC75453						
Low-to-High-Level Output	t_{PLH}	6	–	15	–	ns
High-to-Low-Level Output	t_{PHL}		–	17	–	
MC75454						
Low-to-High-Level Output	t_{PLH}	6	–	25	–	ns
High-to-Low-Level Output	t_{PHL}		–	19	–	
Transition Time ($I_O \approx 200$ mA, C_L = 15 pF, R_L = 50 ohms)						
MC75451						
Low-to-High-Level Output	t_{TLH}	6	–	6.0	–	ns
High-to-Low-Level Output	t_{THL}		–	11	–	
MC75452						
Low-to-High-Level Output	t_{TLH}	6	–	8.0	–	ns
High-to-Low-Level Output	t_{THL}		–	9.0	–	
MC75453						
Low-to-High-Level Output	t_{TLH}	6	–	5.0	–	ns
High-to-Low-Level Output	t_{THL}		–	8.0	–	
MC75454						
Low-to-High-Level Output	t_{TLH}	6	–	5.0	–	ns
High-to-Low-Level Output	t_{THL}		–	8.0	–	

5

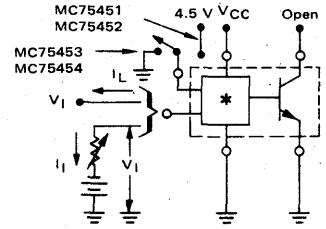
TEST CIRCUITS (Continued)
(Current into terminal is shown as a positive value.
Arrows indicate actual direction of current flow.)

FIGURE 3 – I_{IH} (ALL DEVICE TYPES)



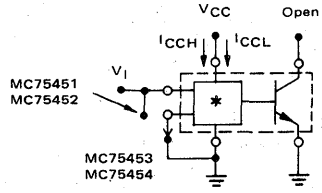
Each input is tested separately.

FIGURE 4 – I_{IL}, V_I (ALL DEVICE TYPES)



Each input is tested separately.

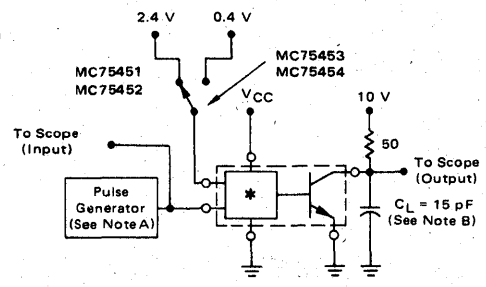
FIGURE 5 – I_{CCH}, I_{CCL} (ALL DEVICE TYPES)



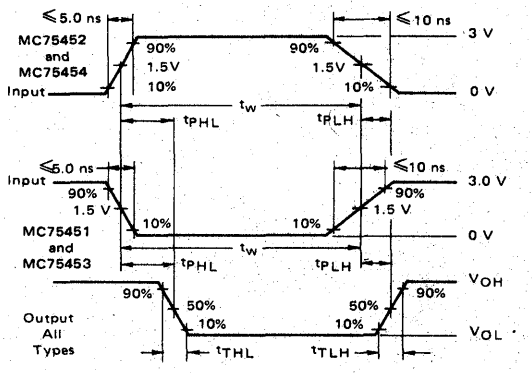
*See page 1 for specific gate type.

Both gates are tested simultaneously.

FIGURE 6 – SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



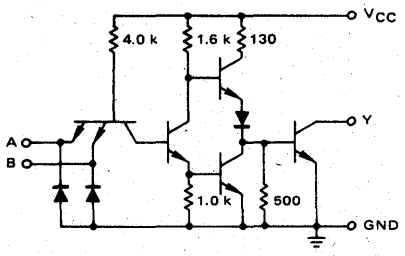
NOTES: A. Pulse generator characteristics: t_w = 0.5 μs, PRR = 1.0 MHz, $z_o \approx 50\ \Omega$.
B. C_L includes probe and test fixture capacitance.



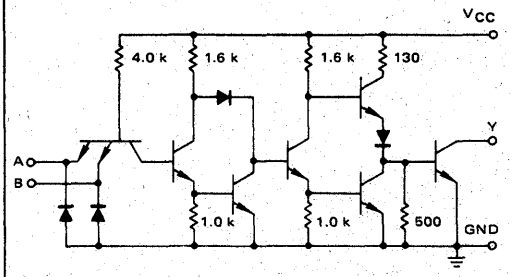
REPRESENTATIVE SCHEMATIC DIAGRAMS

(1/2 Circuits Shown)

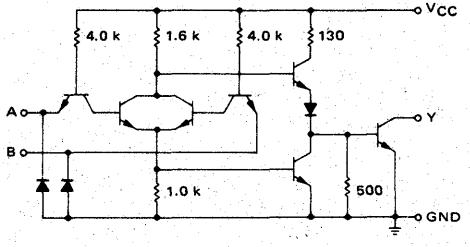
MC75451



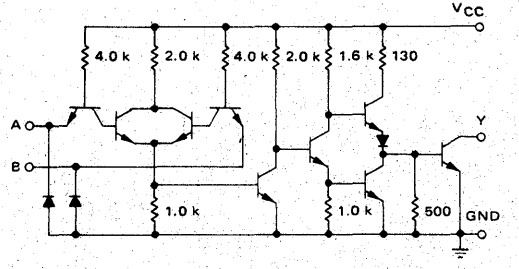
MC75452



MC75453



MC75454



ORDERING INFORMATION

Device	Temperature Range	Package
MC75461P	0°C to +70°C	Plastic DIP
MC75461U	0°C to +70°C	Ceramic DIP
MC75462P	0°C to +70°C	Plastic DIP
MC75462U	0°C to +70°C	Ceramic DIP
MC75463P	0°C to +70°C	Plastic DIP
MC75463U	0°C to +70°C	Ceramic DIP
MC75464P	0°C to +70°C	Plastic DIP
MC75464U	0°C to +70°C	Ceramic DIP

MC75461
MC75462
MC75463
MC75464

DUAL HIGH-VOLTAGE PERIPHERAL DRIVERS

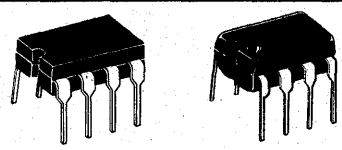
The MC75461 thru MC75464 series is similar to the MC75451 thru MC75454 series peripheral drivers; however, the MC75461 series features greater voltage capability allowing operation with higher output voltages or with inductive loads. These devices are useful as lamp drivers, relay drivers, logic buffers, line drivers, or MOS drivers.

Each of these devices consists of a pair of MTTL gates with the output of each gate internally connected to the base of a transistor.

MC75461 provides the AND function
MC75462 provides the NAND function
MC75463 provides the OR function
MC75464 provides the NOR function

- 300 mA Output Current Capability
- No Output Latch-up at 30 V
- MTTL compatible Inputs

DUAL HIGH-VOLTAGE PERIPHERAL DRIVERS
SILICON MONOLITHIC INTEGRATED CIRCUITS

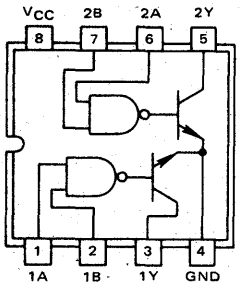


U SUFFIX
CERAMIC PACKAGE
CASE 693

P SUFFIX
PLASTIC PACKAGE
CASE 626

5

MC75461 – Positive AND



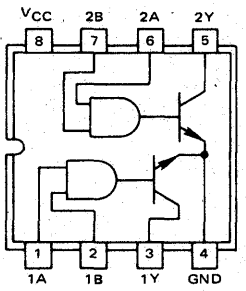
Positive Logic: Y = AB

TRUTH TABLE

A	B	Y
L	L	L ("on" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	H ("off" state)

H = high level, L = low level.

MC75462 – Positive NAND



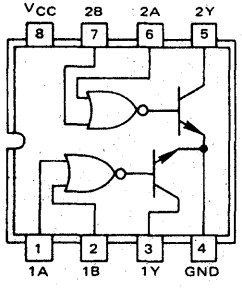
Positive Logic: Y = $\overline{AB}$

TRUTH TABLE

A	B	Y
L	L	H ("off" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	L ("on" state)

H = high level, L = low level

MC75463 – Positive OR



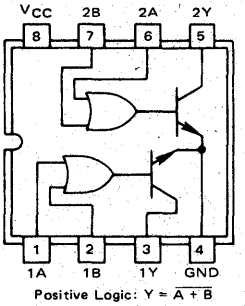
Positive Logic: Y = A + B

TRUTH TABLE

A	B	Y
L	L	L ("on" state)
L	H	H ("off" state)
H	L	H ("off" state)
H	H	H ("off" state)

H = high level, L = low level

MC75464 – Positive NOR



Positive Logic: Y = $\overline{A + B}$

TRUTH TABLE

A	B	Y
L	L	H ("off" state)
L	H	L ("on" state)
H	L	L ("on" state)
H	H	L ("on" state)

H = high level, L = low level.

MAXIMUM RATINGS (T_A = 0°C to 70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage(1)	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Interemitter Voltage(2)	–	5.5	Vdc
Output Voltage(3)	V_O	35	Vdc
Output Current(4)	I_O	300	mA
Power Dissipation @ T_A = 25°C Derate above T_A = +25°C	P_D	830 6.6	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

(1) Voltage values are with respect to network ground terminal.
(2) This is the voltage between two emitters of a multiple-emitter transistor.
(3) This is the maximum voltage which should be applied to any output when it is in the "off" state.
(4) Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for 4.75 ≥ V_{CC} ≥ 5.25 V and 0°C ≤ T_A ≤ 70°C)

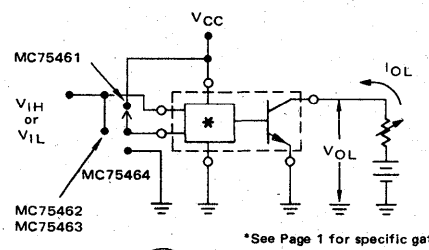
Characteristic		Figure	Symbol	Min	Typ(1)	Max	Unit
Input Voltage – High Logic State		1,2	V_{IH}	2.0	–	–	Vdc
Input Voltage – Low Logic State		1,2	V_{IL}	–	–	0.8	Vdc
Input Clamp Voltage (V_{CC} = 4.75 V, I_I = -12 mA)		4	V_I	–	-1.2	-1.5	Vdc
Output Current – High Logic State (V_{CC} = 4.75 V, V_{OH} = 35 V, V_{IH} = 2.0 V) (V_{CC} = 4.75 V, V_{OH} = 35 V, V_{IL} = 0.8 V)	 MC75461, MC75463 MC75462, MC75464	2	I_{OH}	–	–	100	μA
Output Voltage – Low Logic State (V_{CC} = 4.75 V, V_{IL} = 0.8 V) (V_{CC} = 4.75 V, V_{IH} = 2.0 V) I_{OL} = 100 mA I_{OL} = 300 mA	 MC75461, MC75463 MC75462, MC75464	1	V_{OL}	 – –	 0.15 0.35	 0.4 0.7	Vdc
Input Current – High Logic State (V_{CC} = 5.25 V, V_I = 2.4 V) (V_{CC} = 5.25 V, V_I = 5.5 V)		3	I_{IH}	 – –	 – –	 40 1.0	 μA mA
Input Current – Low Logic State (V_{CC} = 5.25 V, V_I = 0.4 V)		4	I_{IL}	–	-1.0	-1.6	mA
Power Supply Current – Output High Logic State (V_{CC} = 5.25 V, V_{IH} = 5.0 V) (V_{CC} = 5.25 V, V_{IL} = 0) (V_{CC} = 5.25 V, V_{IH} = 5.0 V) (V_{CC} = 5.25 V, V_{IL} = 0)	 MC75461 MC75462 MC75463 MC75464	5	I_{CCH}	 – – – –	 8.0 13 8.0 14	 11 17 11 19	mA
Power Supply Current – Output Low Logic State (V_{CC} = 5.25 V, V_{IL} = 0) (V_{CC} = 5.25 V, V_{IH} = 5.0 V) (V_{CC} = 5.25 V, V_{IL} = 0) (V_{CC} = 5.25 V, V_{IH} = 5.0 V)	 MC75461 MC75462 MC75463 MC75464	5	I_{CCL}	 – – – –	 61 65 63 72	 76 76 76 85	mA

(1) Typical Values Measured with V_{CC} = 5.0 V, T_A = 25°C

TEST CIRCUITS

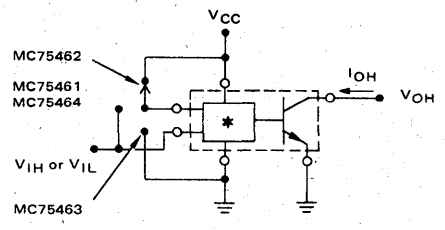
(Current into terminal is shown as a positive value.
Arrows indicate actual direction of current flow.)

FIGURE 1 – V_{OL}
V_{IH} – MC75462 and MC75464
V_{IL} – MC75461 and MC75463



*See Page 1 for specific gate type.

FIGURE 2 – I_{OH},
V_{IH} – MC75461 and MC75463
V_{IL} – MC75462 and MC75464



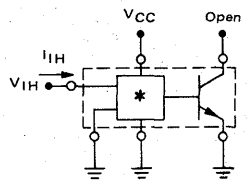
Each input is tested separately.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time ($I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 ohms)						
MC75461						
Low-to-High-Level Output	t_{PLH}	6	–	45	55	ns
High-to-Low-Level Output	t_{PHL}		–	30	40	
MC75462						
Low-to-High-Level Output	t_{PLH}	6	–	50	65	ns
High-to-Low-Level Output	t_{PHL}		–	40	50	
MC75463						
Low-to-High-Level Output	t_{PLH}	6	–	45	55	ns
High-to-Low-Level Output	t_{PHL}		–	30	40	
MC75464						
Low-to-High-Level Output	t_{PLH}	6	–	50	65	ns
High-to-Low-Level Output	t_{PHL}		–	40	50	
Transition Time ($I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 ohms)						
MC75461						
Low-to-High-Level Output	t_{TLH}	6	–	8.0	20	ns
High-to-Low-Level Output	t_{THL}		–	10	20	
MC75462						
Low-to-High-Level Output	t_{TLH}	6	–	12	25	ns
High-to-Low-Level Output	t_{THL}		–	15	20	
MC75463						
Low-to-High-Level Output	t_{TLH}	6	–	8.0	25	ns
High-to-Low-Level Output	t_{THL}		–	10	25	
MC75464						
Low-to-High-Level Output	t_{TLH}	6	–	12	20	ns
High-to-Low-Level Output	t_{THL}		–	15	20	
Output Voltage – High Logic Level after Switching (Latch-up Test) (V_S = 30 V $I_O \approx$ 300 mA)	V_{OH}	7	V_S-10	–	–	mV

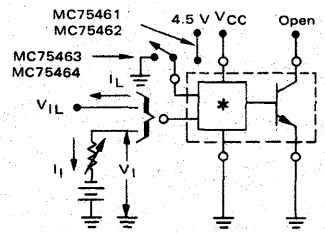
TEST CIRCUITS (Continued)
(Current into terminal is shown as a positive value.
Arrows indicate actual direction of current flow.)

FIGURE 3 – I_{IH} (ALL DEVICE TYPES)



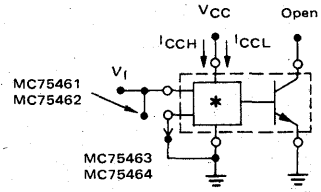
Each input is tested separately.

FIGURE 4 – I_{IL}, V_I (ALL DEVICE TYPES)



Each input is tested separately.

FIGURE 5 – I_{CCH}, I_{CCL} (ALL DEVICE TYPES)

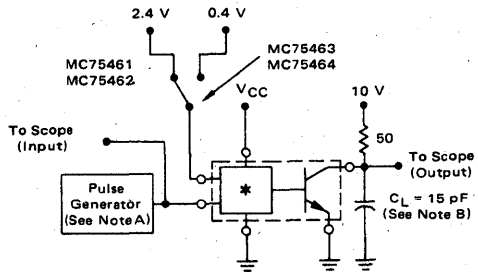


*See page 1 for specific gate type.

Both gates are tested simultaneously.

5

FIGURE 6 – SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



NOTES: A. Pulse generator characteristics: $t_w = 0.5\ \mu s$, PRR = 1.0 MHz, $z_o \approx 50\ \Omega$
B. C_L includes probe and test fixture capacitance.

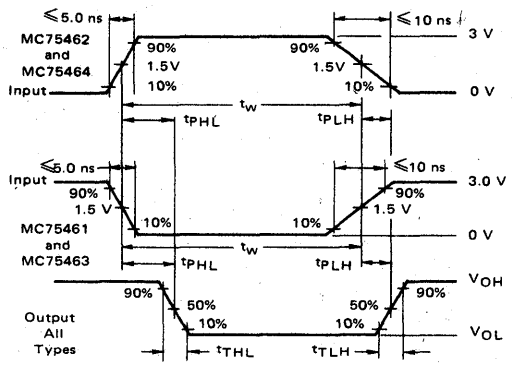
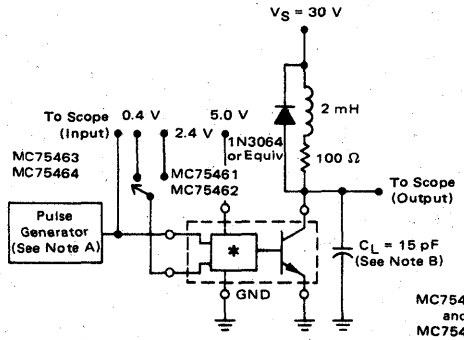
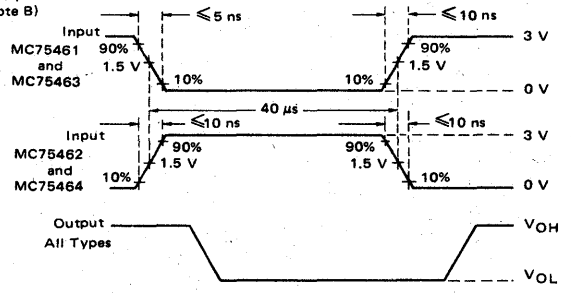


FIGURE 7 – OUTPUT VOLTAGE AFTER SWITCHING TEST CIRCUIT AND WAVEFORMS (LATCH-UP TEST)



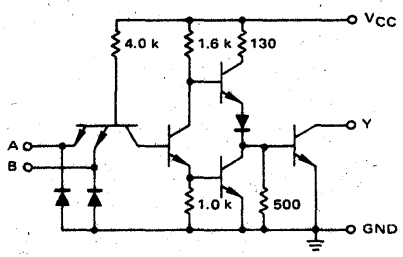
*See Page 1 for specific gate type.



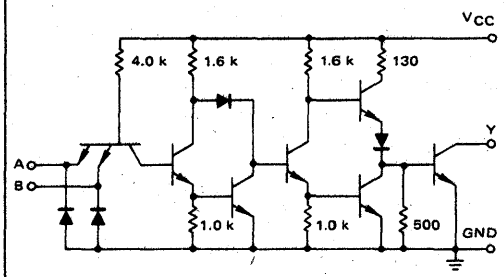
NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out} = 50\ \Omega$
B. C_L includes probe and jig capacitance.

REPRESENTATIVE SCHEMATIC DIAGRAMS
(1/2 Circuits Shown)

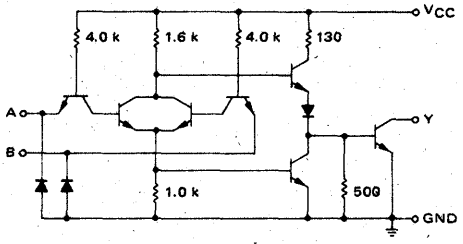
MC75461



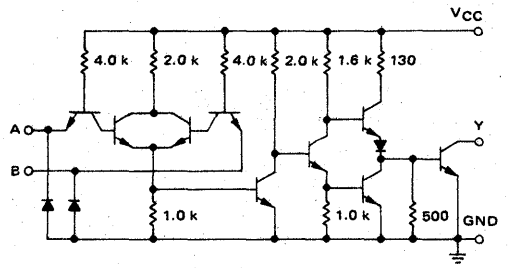
MC75462



MC75463



MC75464



ORDERING INFORMATION

Device	Temperature Range	Package
MC75491P	0°C to +70°C	Plastic DIP
MC75492P	0°C to +70°C	Plastic DIP

MC75491
MC75492

Specifications and Applications Information

MULTIPLE
LIGHT-EMITTING DIODE (LED)
DRIVERS

SILICON MONOLITHIC
INTEGRATED CIRCUITS

QUAD LED SEGMENT DRIVER – MC75491
HEX LED DIGIT DRIVER – MC75492

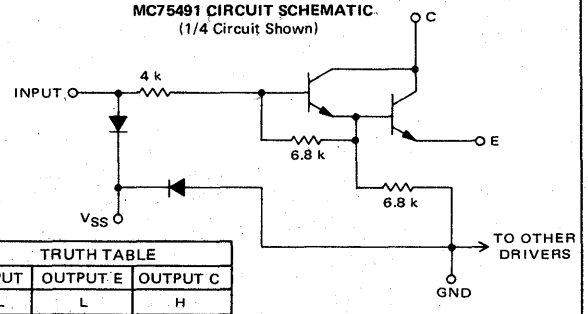
The MC75491 and MC75492 are designed to interface MOS logic to common cathode light-emitting diode readouts in serially addressed multi-digit displays. Using a segment address and digit scan LED drive method in a time multiplexing system results in a minimizing of the number of required drivers.

- Low Input Current Requirement for MOS Compatibility
- Low Standby Power Drain
- Source or Sink Current Capability of 50 mA for MC75491
- Sink Current Capability of 250 mA for MC75492
- Four High-Gain Darlington Drivers in a Single Package – MC75491
- Six High-Gain Darlington Drivers in a Single Package – MC75492

P SUFFIX
PLASTIC PACKAGE
CASE 646

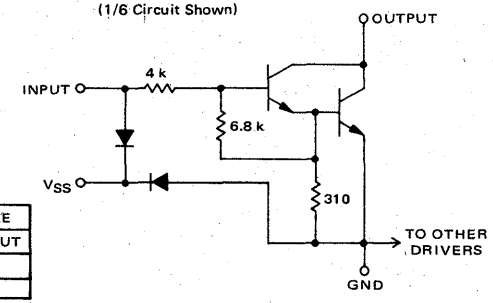
5

MC75491 CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



TRUTH TABLE		
INPUT	OUTPUT E	OUTPUT C
L	L	H
H	H	L

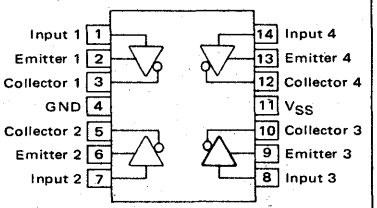
MC75492 CIRCUIT SCHEMATIC
(1/6 Circuit Shown)



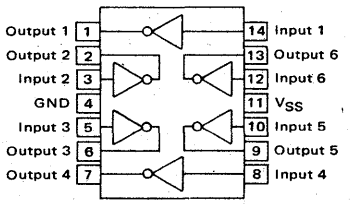
TRUTH TABLE	
INPUT	OUTPUT
L	H
H	L

CONNECTION DIAGRAMS

MC75491



MC75492



MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value		Unit
		MC75491	MC75492	
Bias Supply Voltage (See Note 1)	V_{SS}	10	10	Vdc
Input Voltage (See Note 2)	V_{in}	-5.0 to V_{SS}	-5.0 to V_{SS}	Vdc
Collector Voltage (See Note 3)	V_C	10	10	Vdc
Collector-to-Emitter Voltage	V_{CE}	10	–	Vdc
Collector-to-Input Voltage	V_{CI}	10	10	Vdc
Emitter Voltage ($V_{in} \geq 5.0$ Vdc)	V_E	10	–	Vdc
Emitter-to-Input Voltage	V_{EI}	5.0	–	Vdc
Continuous Collector Current (Each Collector) (All Collectors)	I_C	50 200	250 600	mA mA
Power Dissipation (Package Limitation) Ceramic and Plastic Dual In-Line Packages Derate above T_A = +25°C	P_D	 830 6.6		 mW mW/°C
Operating Temperature Range	T_A	0 to +70		°C
Storage Temperature Range	T_{stg}	-65 to +150		°C

Note 1. V_{SS} terminal voltage is with respect to any other device terminal.

Note 2. With the exception of the inputs, the GND terminal must always be the most negative device voltage for proper operation.

Note 3. Voltage values are with respect to GND terminal unless otherwise noted.

ELECTRICAL CHARACTERISTICS (V_{SS} = 10 Vdc, T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	MC75491			MC75492			Unit
		Min	Typ	Max	Min	Typ	Max	
Low-Level Collector-to-Emitter Voltage (V_{in} = 8.5 V thru 1.0 kΩ, I_{OL} = 50 mA, V_E = 5.0 V) T_A = +25°C T_A = 0 to +70°C	V_{CEL}	 – –	 0.9 –	 1.2 1.5	 – –	 – –	 – –	Vdc
High-Level Collector Current V_{CH} = 10 V, V_E = 0, I_{in} = 40 μA V_{CH} = 10 V, V_E = 0, V_{in} = 0.7 V	I_{CH}	 – –	 – –	 100 100	 – –	 – –	 – –	μA
Low-Level Output Voltage (V_{in} = 6.5 V thru 1.0 kΩ, I_{OL} = 250 mA) T_A = +25°C T_A = 0 to +70°C	V_{OL}	 – –	 – –	 – –	 – –	 0.9 –	 1.2 1.5	Vdc
High-Level Output Current V_{OH} = 10 V, I_{in} = 40 μA V_{OH} = 10 V, V_{in} = 0.5 V	I_{OH}	 – –	 – –	 – –	 – –	 – –	 200 200	μA
Input Current at Maximum Input Voltage V_{in} = 10 V, I_{OL} = 20 mA	I_{in}	–	2.2	3.3	–	2.2	3.3	mA
Emitter Current – Reverse Bias I_C = 0, V_{in} = 0, V_E = 5.0 V	I_{ER}	–	–	100	–	–	–	μA
Bias Supply Current (V_{SS} = 10 V)	I_{SS}	–	–	1.0	–	–	1.0	mA

SWITCHING CHARACTERISTICS (V_{SS} = 7.5 V, T_A = +25°C unless otherwise noted.)

Propagation Delay Time, High-to-Low Level R_L = 200 Ω, V_{IH} = 4.5 V, C_L = 15 pF, V_E = 0 R_L = 39 Ω, V_{IH} = 7.5 V, C_L = 15 pF	t_{PHL}	 – –	 20* –	 – –	 – –	 – 40	 – –	ns
Propagation Delay Time, Low-to-High Level C_L = 15 pF, V_E = 0, R_L = 200 Ω, V_{IH} = 4.5 Vdc C_L = 15 pF, R_L = 39 Ω, V_{IH} = 7.5 Vdc	t_{PLH}	 – –	 40* –	 – –	 – –	 – 80	 – –	ns

*To collector output.

TYPICAL CHARACTERISTICS

(V_{SS} = +10 Vdc, T_A = +25°C unless otherwise noted.)

MC75491

FIGURE 1 – COLLECTOR CURRENT versus INPUT VOLTAGE

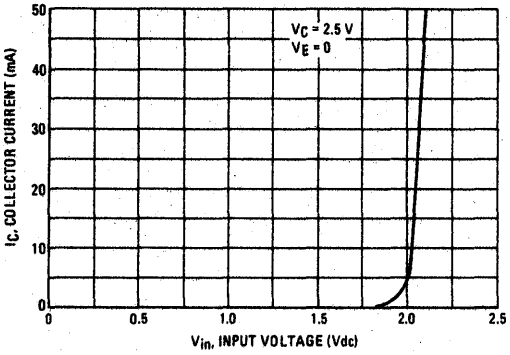


FIGURE 3 – COLLECTOR CURRENT versus INPUT CURRENT

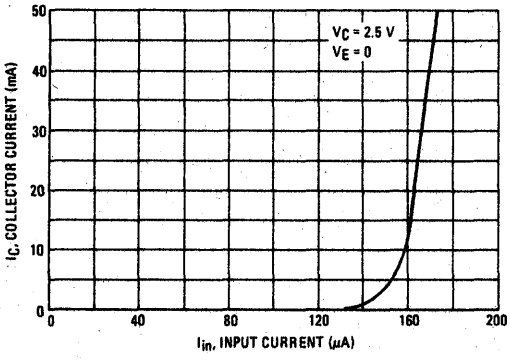
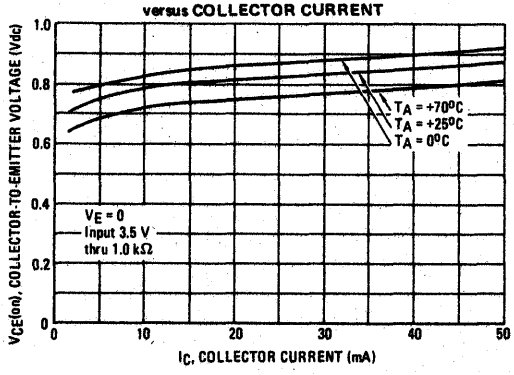


FIGURE 5 – COLLECTOR-TO-EMITTER VOLTAGE (ON) versus COLLECTOR CURRENT



MC75492

FIGURE 2 – OUTPUT CURRENT versus INPUT VOLTAGE

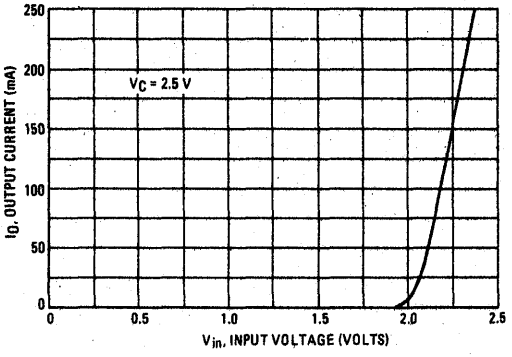


FIGURE 4 – OUTPUT CURRENT versus INPUT CURRENT

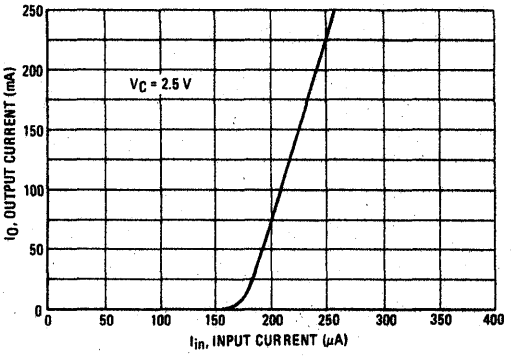
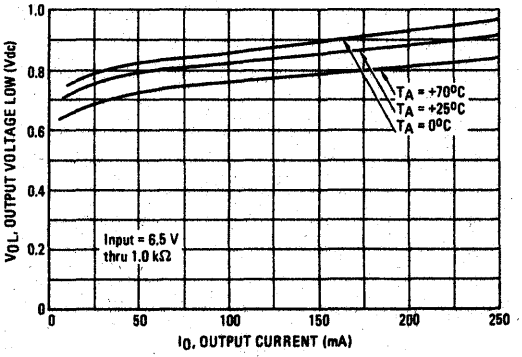


FIGURE 6 – OUTPUT VOLTAGE LOW versus OUTPUT CURRENT



5

TYPICAL CHARACTERISTICS and SWITCHING TIME CIRCUITS

FIGURE 7 – MC75491/MC75492 INPUT CURRENT versus INPUT VOLTAGE

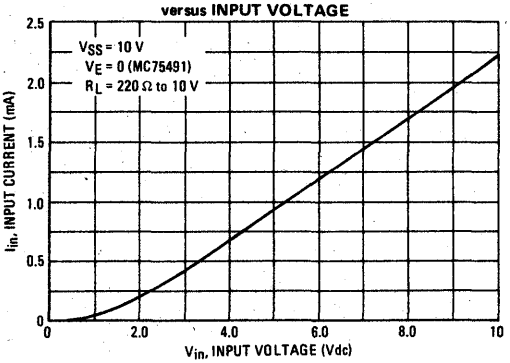


FIGURE 8 – MC75491 SWITCHING CIRCUIT

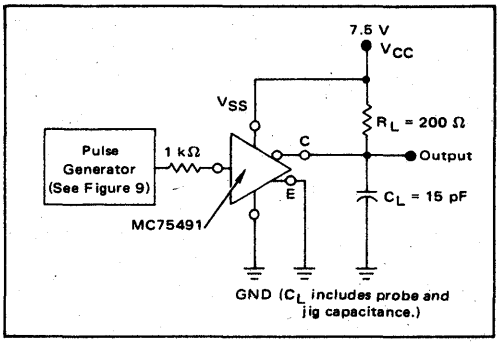


FIGURE 9 – SWITCHING WAVEFORM DEFINITIONS

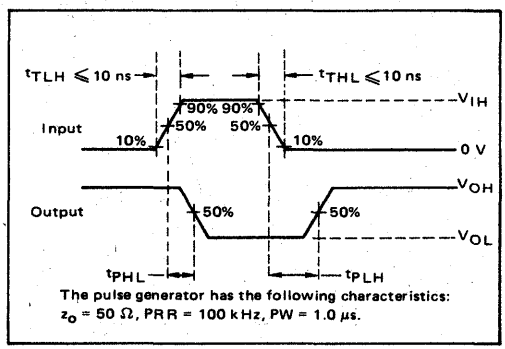
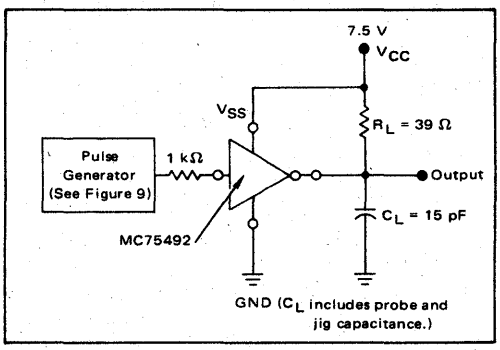


FIGURE 10 – MC75492 SWITCHING CIRCUIT



TYPICAL APPLICATIONS

FIGURE 11 – QUAD-OR-HEX RELAY DRIVER

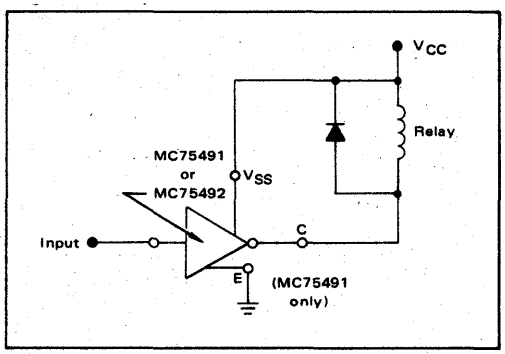
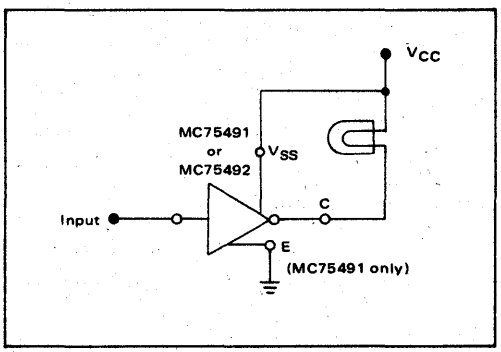


FIGURE 12 – QUAD-OR-HEX LAMP DRIVER



5

TYPICAL APPLICATIONS (continued)

FIGURE 13 – MOS-TO-MTTL LEVEL TRANSLATOR

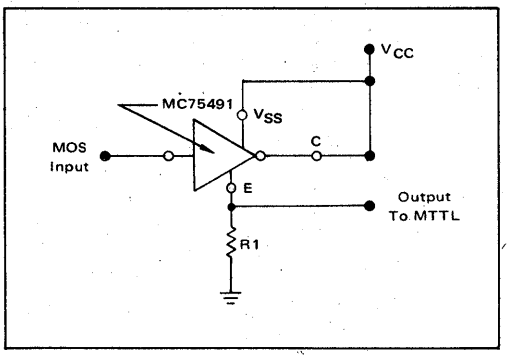


FIGURE 14 – QUAD HIGH-CURRENT NPN TRANSISTOR DRIVER

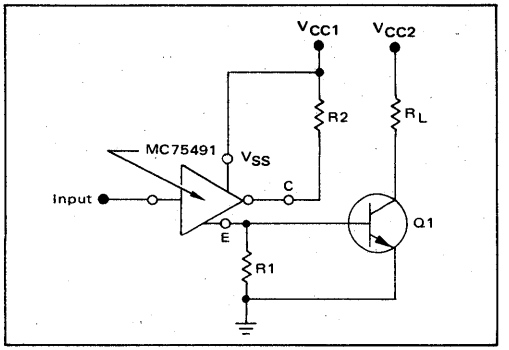


FIGURE 15 – QUAD-OR-HEX HIGH-CURRENT PNP TRANSISTOR DRIVER

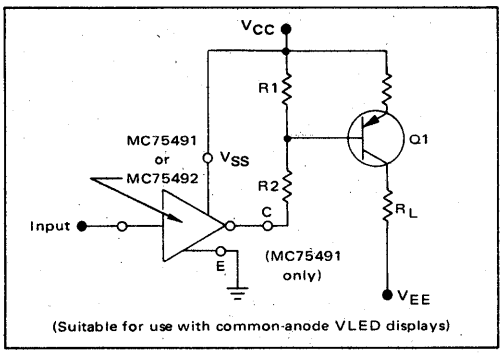


FIGURE 16 – BASE-EMITTER SELECT TRANSISTOR DRIVER

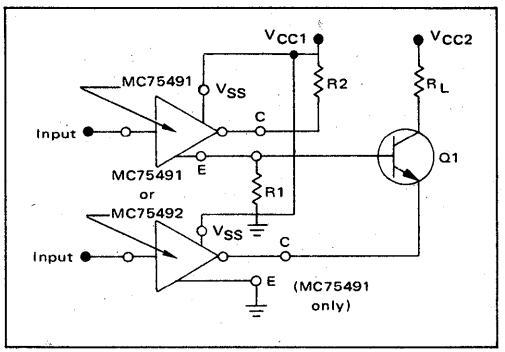
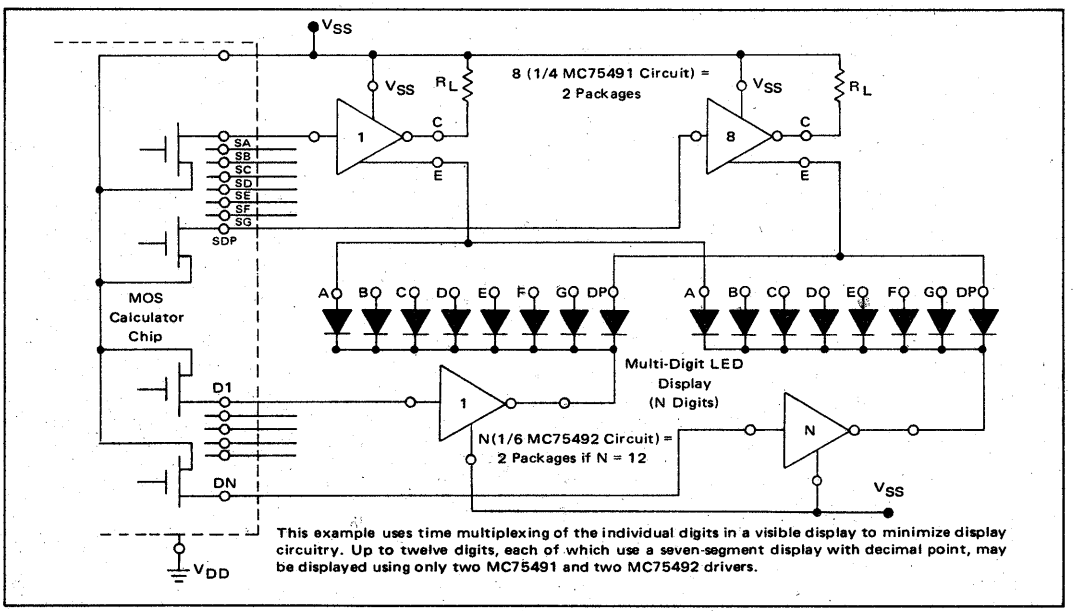


FIGURE 17 – MOS CALCULATOR CHIP-TO-LED INTERFACE CIRCUIT



TYPICAL APPLICATIONS (continued)

FIGURE 18 – STROBED "NOR" DRIVER

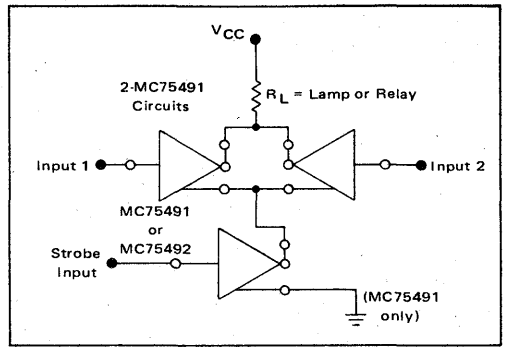
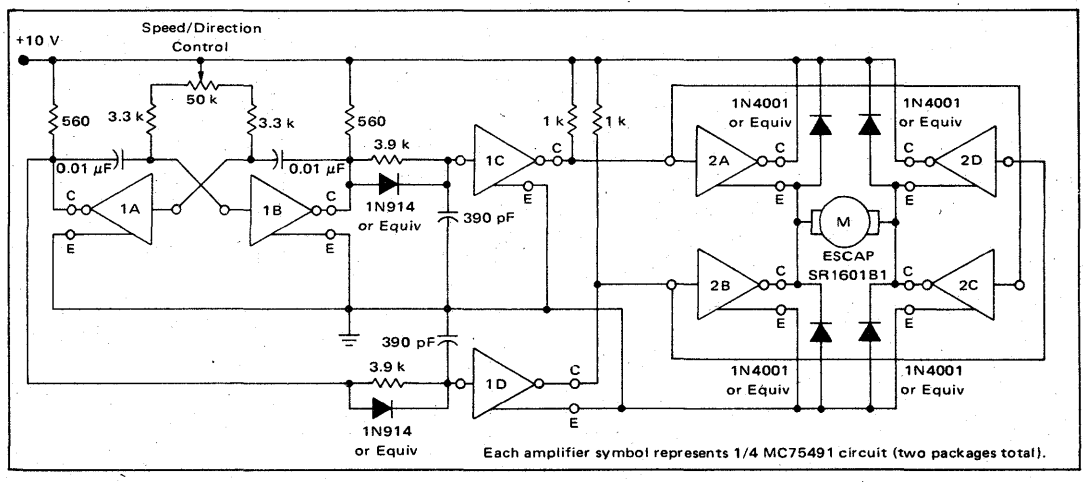


FIGURE 19 – DC MOTOR SPEED/DIRECTION CONTROL CIRCUIT



5

ORDERING INFORMATION

Device	Temperature Range	Package
MCC1486	0°C to +70°C	Chip Only
MCC1487	0°C to +70°C	Chip Only

MCC1486
MCC1487

Advance Information

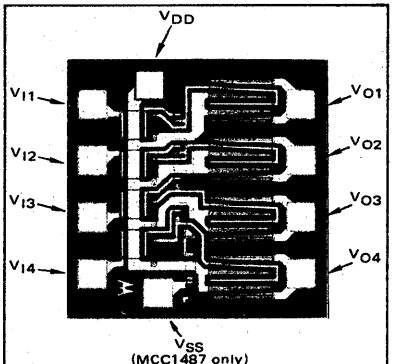
QUAD LED DIGIT DRIVERS

The MCC1486/MCC1487 consists of four (4) medium current (70 mA) CMOS compatible digit drivers. Each circuit has been specially designed for use with digital watch display applications employing demand display CMOS watch circuits, or other applications requiring CMOS or equivalent input compatibility. Both are designed to serve as digit drivers for driving 4-digit common cathode LED watch displays. Each driver serves as a current sink for a particular digit cathode, providing convenient time multiplex operation. The time-multiplexed display system allows a single driver to serve as a current sink for all segments of a particular digit, resulting in a significant decrease in interface circuit requirements.

The MCC1487 differs from the MCC1486 in that a two-stage high-gain driver circuit is used. The increased gain of the MCC1487 circuit permits operation with very low output current CMOS watch circuits. Also, the MCC1487's improved input threshold (approximately 2 V_{BE}) provides greater immunity to characteristic CMOS output leakage currents. Together, the increased gain and improved input threshold allows use of relaxed watch chip specifications and a more stable, noise free operation.

QUAD LED DIGIT DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUITS



(MCC1487 only)

Available in Chip Form Only

-1 Suffix Indicates Multiples of 10

-2 Suffix Indicates Multiples of 100

MCC1487 Metal Pattern Shown. Pad Locations Same For Both Devices.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{SS}	5.0	V
Input Voltage	V_I	5.0	V
Output Voltage	V_O	5.0	V
Output Current	I_O	100	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 – 1/4 of MCC1486

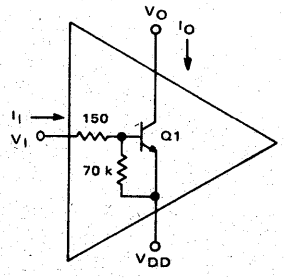
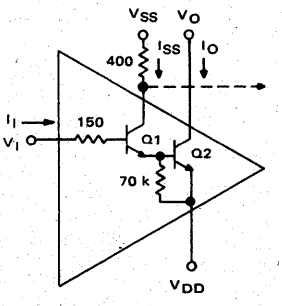
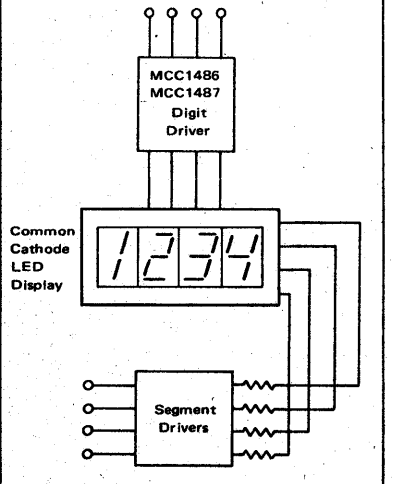


FIGURE 2 – 1/4 of MCC1487





TYPICAL APPLICATION

CROSS REFERENCE

BOMAR BD5030 – MCC1486

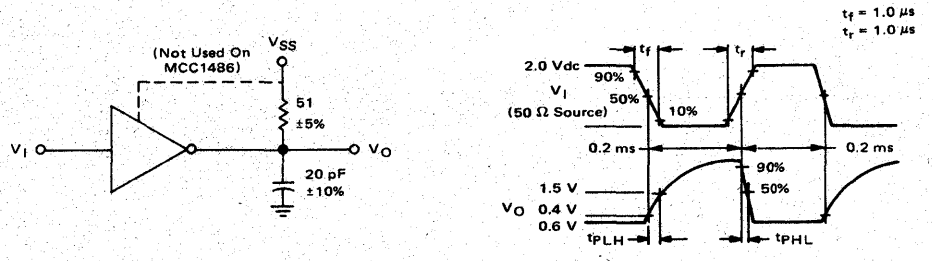
BOMAR BD5031 – MCC1487

This is advance information and specifications are subject to change without notice.

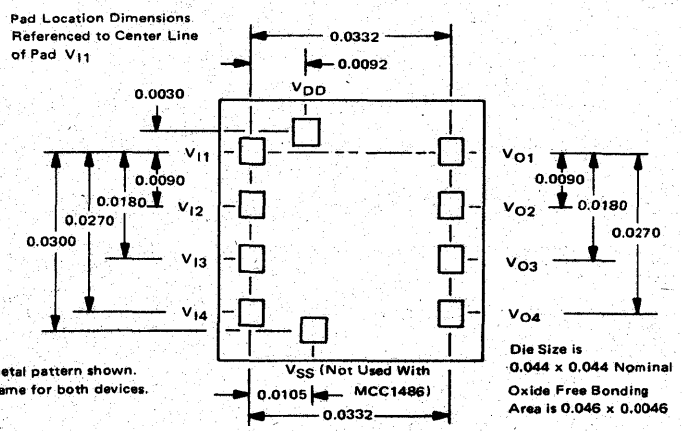
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	MCC1486 Min	MCC1486 Max	MCC1487 Min	MCC1487 Max	Unit
Output Voltage – Low Logic State	V_{OL}					Vdc
(V_I = 1.2 V, I_O = 70 mA)		–	0.4	–	–	
(I_I = 840 μA, I_O = 56 mA)		–	0.4	–	–	
(V_I = 2.0 V) I_O = 70 mA, V_{SS} = 3.0 V)		–	–	–	0.4	
Output Current – High Logic State	I_{OH}					μA
(Total of all Outputs)						
(V_I = 0.2 V, V_O = 3.0 V)		–	1.0	–	–	
(V_I = 0.2 V, V_O = V_{SS} = 3.0 V)		–	–	–	1.0	
Input Current – On State	$I_{I(on)}$					μA
(V_I = 1.2 V)		840	–	–	–	
(V_I = 2.0 V)		–	–	300	–	
Input Current – Off State	$I_{I(off)}$					
(V_I = 0.2 V)		–	20	–	–	μA
(V_I = 0.5 V)		–	–	–	200	nA
Power Supply Current	I_{SS}					mA
(V_I = 2.0 V, I_O = 70 mA, V_{SS} = 3.0 V)		–	–	–	7.0	
Propagation Delay Time						
Low to High State Output	t_{PLH}	–	10	–	10	μs
High to Low State Output	t_{PHL}	–	10	–	10	μs

FIGURE 3 – SWITCHING TEST CIRCUIT AND WAVEFORMS
(For Reference Only)



CHIP OUTLINE DIMENSIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MMH0026G	−55°C to +125°C	Metal Can
MMH0026L	−55°C to +125°C	Ceramic DIP
MMH0026U	−55°C to +125°C	Ceramic DIP
MMH0026CG	0°C to +70°C	Metal Can
MMH0026CL	0°C to +70°C	Ceramic DIP
MMH0026CP1	0°C to +70°C	Plastic DIP
MMH0026CU	0°C to +70°C	Ceramic DIP

MMH0026
MMH0026C

Specifications and Applications Information

DUAL MOS CLOCK DRIVER

. . . designed for high-speed driving of highly capacitive loads in a MOS system.

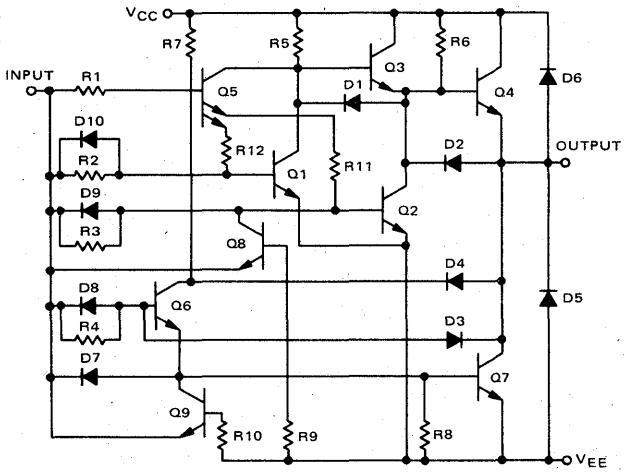
- Fast Transition Times – 20 ns with 1000 pF Load
- High Output Swing – 20 Volts
- High Output Current Drive – ±1.5 Amperes
- High Repetition Rate – 5.0 to 10 MHz Depending on Load
- MTTL and MDTL Compatible Inputs
- Low Power Consumption when in MOS "0" State – 2.0 mW
- +5.0-Volt Operation for N-Channel MOS Compatibility

DUAL MOS CLOCK DRIVER

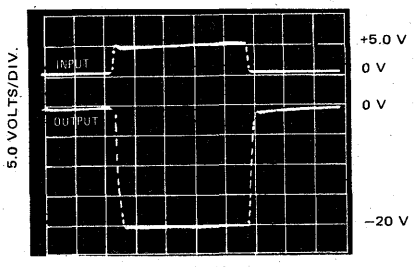
SILICON MONOLITHIC INTEGRATED CIRCUIT

5

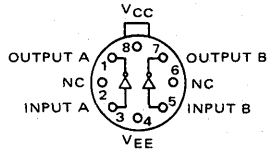
FIGURE 1 – CIRCUIT SCHEMATIC (1/2 CIRCUIT SHOWN)



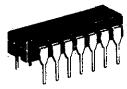
TYPICAL OPERATION
(R_S = 10 Ω, $C_L = C_{in}$ = 1000 pF, f = 1.0 MHz, PW = 500 ns, V_{CC} = 0 V, V_{EE} = −20 V)



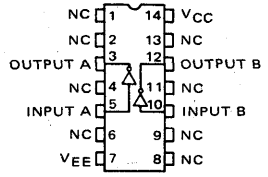
G SUFFIX
METAL PACKAGE
CASE 601-02
TO-99



(Top View)



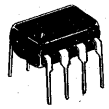
L SUFFIX
CERAMIC PACKAGE
CASE 632-02
TO-116

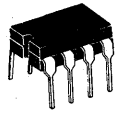


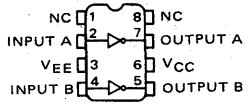
(Top View)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MMH0026C Only)

U SUFFIX
CERAMIC PACKAGE
CASE 693







(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value			Unit
Differential Supply Voltage	V_{CC}-V_{EE}	+22			Vdc
Input Current	I_I	+100			mA
Input Voltage	V_I	V_{EE} + 5.5			Vdc
Peak Output Current	I_{Opk}	±1.5			A
Junction Temperature	T_J	+175	+175	+150	°C
Operating Ambient Temperature Range	T_A	G	U,L	P1	°C
MMH0026		-55 to +125	-55 to +125	–	
MMH0026C		0 to +70	0 to +70	0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC}-V_{EE} = 10 V to 20 V, C_L = 1000 pF, T_A = -55 to +125°C for MMH0026 and 0 to +70°C for MMH0026C for min and max values; T_A = +25°C for all typical values unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Logic "1" Level Input Voltage $V_O = V_{EE}$ + 1.0 Vdc		V_{IH}	V_{EE} + 2.0	V_{EE} + 1.5	–	Vdc
Logic "1" Level Input Current $V_I - V_{EE}$ = 2.4 Vdc, $V_O = V_{EE}$ + 1.0 Vdc		I_{IH}	–	10	15	mA
Logic "0" Level Input Voltage $V_O = V_{CC}$ -1.0 Vdc		V_{IL}	–	V_{EE} + 0.6	V_{EE} + 0.4	Vdc
Logic "0" Level Input Current $V_I - V_{EE}$ = 0 Vdc, $V_O = V_{CC}$ -1.0 Vdc		I_{IL}	–	-0.005	-10	μA
Logic "0" Level Output Voltage		V_{OH}				Vdc
V_{CC} = +5.0 Vdc, V_{EE} = -12 Vdc, V_I = -11.6 Vdc			4.0	4.3	–	
$V_I - V_{EE}$ = 0.4 Vdc			V_{CC} -1.0	V_{CC} -0.7	–	
Logic "1" Level Output Voltage		V_{OL}				Vdc
V_{CC} = +5.0 Vdc, V_{EE} = -12 Vdc, V_I = -9.6 Vdc			–	-11.5	-11	
$V_I - V_{EE}$ = 2.4 Vdc			–	V_{EE} + 0.5	V_{EE} + 1.0	
"On" Supply Current V_{CC}-V_{EE} = 20 Vdc, $V_I - V_{EE}$ = 2.4 Vdc		I_{CCL}	–	30	40	mA
"Off" Supply Current	MMH0026C	I_{CCH}	–	10	100	μA
V_{CC}-V_{EE} = 20 Vdc, $V_I - V_{EE}$ = 0 V	MMH0026		–	–	500	

SWITCHING CHARACTERISTICS (V_{CC}-V_{EE} = 10 V to 20 V, C_L = 1000 pF, T_A = 25°C)

Propagation Time						
High to Low	(Figure 2)	t_{PHL}	5.0	7.5	12	ns
	(Figure 3)		–	11	–	
Low to High	(Figure 2)	t_{PLH}	5.0	12	15	
	(Figure 3)		–	13	–	
Transition Time (High to Low)		t_{THL}				ns
V_{CC}-V_{EE} = 20 Vdc, C_L = 250 pF	(Figure 2)		–	12	–	
V_{CC}-V_{EE} = 20 Vdc, C_L = 500 pF	(Figure 2)		–	15	18	
	(Figure 3)		–	30	40	
V_{CC}-V_{EE} = 20 Vdc, C_L = 1000 pF	(Figure 2)		–	20	35	
	(Figure 3)		–	36	50	
Transition Time (Low to High)		t_{TLH}				ns
V_{CC}-V_{EE} = 20 Vdc, C_L = 250 pF	(Figure 2)		–	10	–	
V_{CC}-V_{EE} = 20 Vdc, C_L = 500 pF	(Figure 2)		–	12	16	
	(Figure 3)		–	28	35	
V_{CC} -V_{EE} = 20 Vdc, C_L = 1000 pF	(Figure 2)		–	17	25	
	(Figure 3)		–	31	40	

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TEST CIRCUIT

FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS

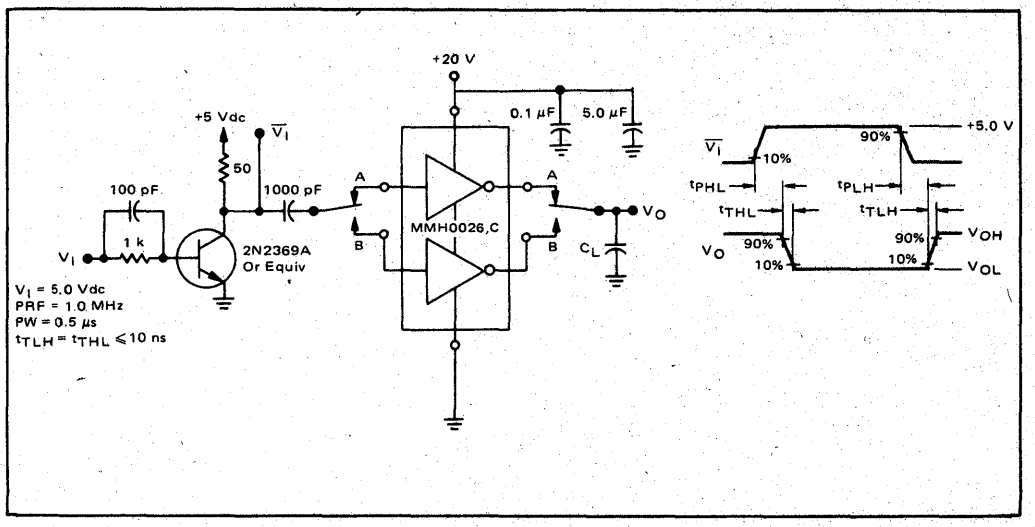
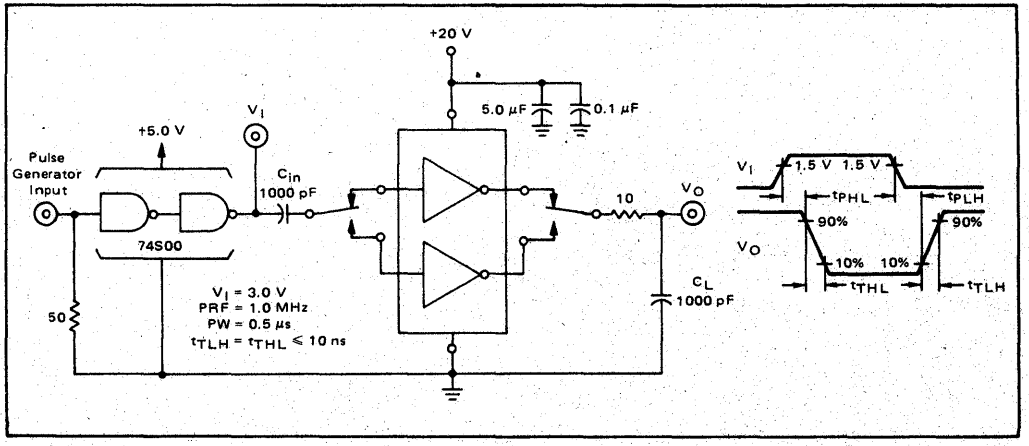


FIGURE 3 – AC TEST CIRCUIT AND WAVEFORMS



TYPICAL CHARACTERISTICS

(V_{CC} = + 20 V, V_{EE} = 0 V, T_A = +25°C unless otherwise noted.)

FIGURE 4 – INPUT CURRENT versus INPUT VOLTAGE

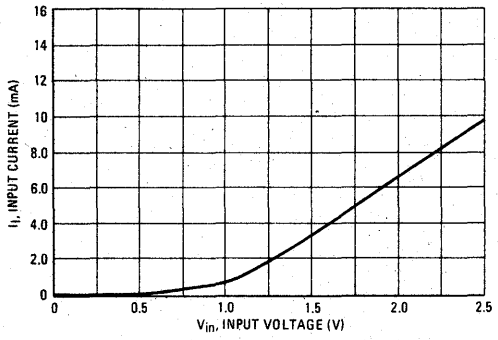


FIGURE 5 – SUPPLY CURRENT versus TEMPERATURE

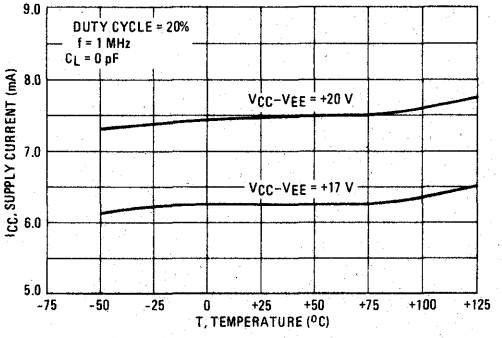


FIGURE 6 – OPTIMUM INPUT CAPACITANCE versus OUTPUT PULSE WIDTH

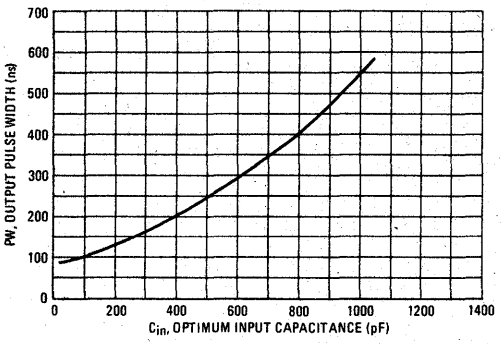


FIGURE 7 – TRANSITION TIMES versus LOAD CAPACITANCE

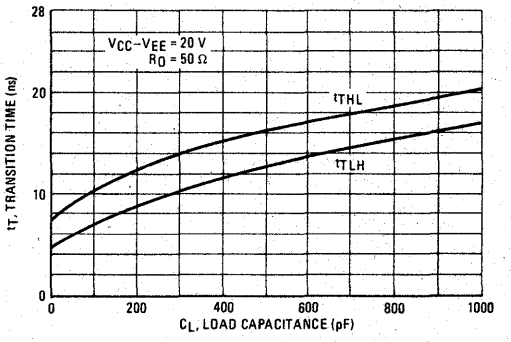


FIGURE 8 – PROPAGATION DELAY TIMES versus TEMPERATURE

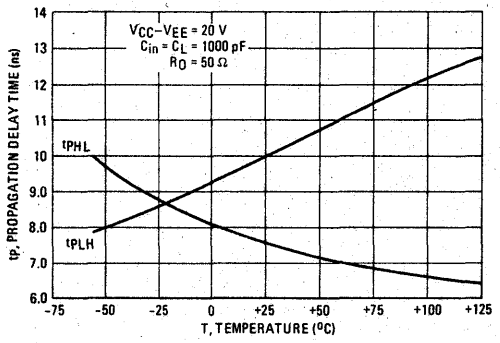
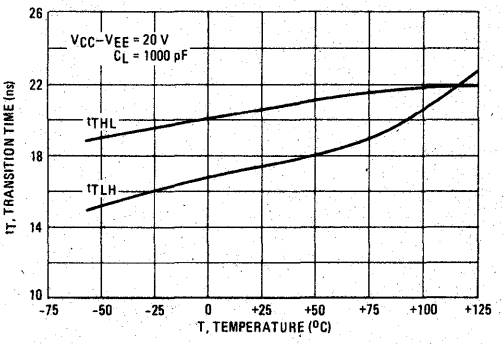


FIGURE 9 – TRANSITION TIMES versus TEMPERATURE



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TYPICAL CHARACTISTICS (continued)

(V_{CC} = + 20 V, V_{EE} = 0 V, T_A = +25°C unless otherwise noted.)

FIGURE 10 – TRANSITION TIME versus TEMPERATURE FOR +5 VOLT DC-COUPLED OPERATION (See Figure 4.)

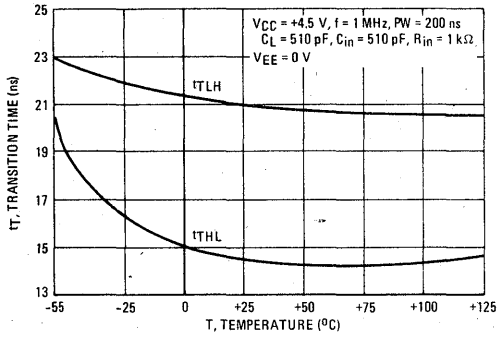


FIGURE 11 – PROPAGATION DELAY TIME versus TEMPERATURE FOR +5 VOLT DC-COUPLED OPERATION (See Figure 4.)

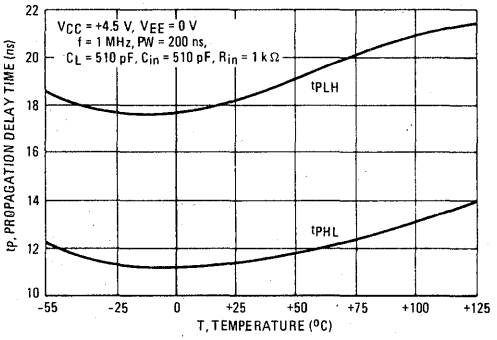


FIGURE 12 – DC-COUPLED SWITCHING RESPONSE versus R_{in} (See Figure 4.)

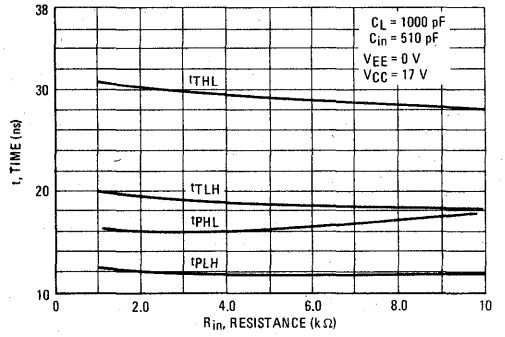


FIGURE 13 – DC-COUPLED SWITCHING versus C_{in} (See Figure 4.)

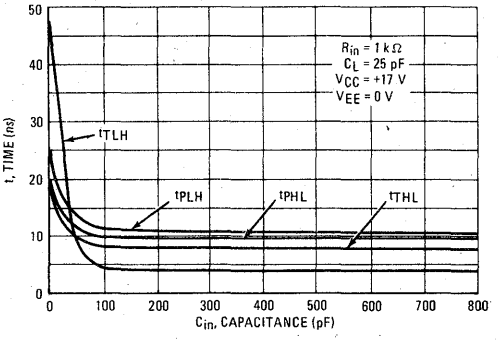


FIGURE 14 – MAXIMUM DC POWER DISSIPATION versus DUTY CYCLE (SINGLE DRIVER)

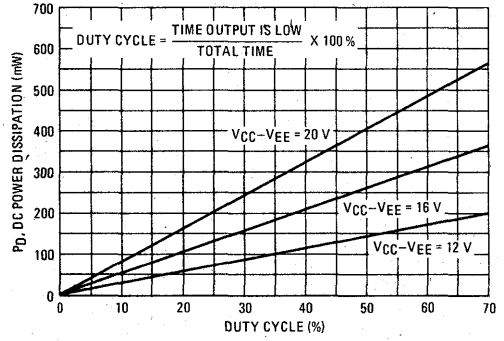
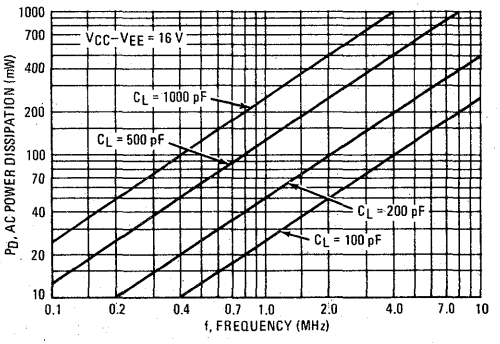


FIGURE 15 – AC POWER DISSIPATION versus FREQUENCY (SINGLE DRIVER)



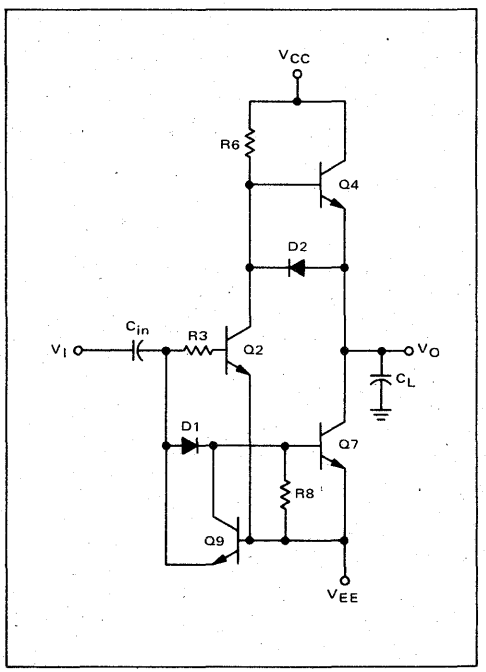
APPLICATIONS INFORMATION

OPERATION OF THE MMH0026

The simplified schematic diagram of MMH0026, shown in Figure 16, is useful in explaining the operation of the device. Figure 16 illustrates that as the input voltage level goes high, diode D1 provides an 0.7-volt "dead zone" thus ensuring that Q2 is turned "on" and Q4 is turned "off" before Q7 is turned "on". This prevents undesirable "current spiking" from the power supply, which would occur if Q7 and Q4 were allowed to be "on" simultaneously for an instant of time. Diode D2 prevents "zenering" of Q4 and provides an initial discharge path for the output capacitive load by way of Q2.

As the input voltage level goes low, the stored charge in Q2 is used advantageously to keep Q2 "on" and Q4 "off" until Q7 is "off". Again undesirable "current spiking" is prevented. Due to the external capacitor, the input side of C_{in} goes negative with respect to V_{EE} causing Q9 to conduct momentarily thus assuring rapid turn "off" of Q7.

FIGURE 16 – SIMPLIFIED SCHEMATIC DIAGRAM
(Ref.: Figure 1)



The complete circuit, Figure 1, basically creates Darlington devices of transistors Q7, Q4 and Q2 in the simplified circuit of Figure 16. Note in Figure 1 that when the input goes negative with respect to V_{EE}, diodes D7 through D10 turn "on" assuring faster turn "off" of transistors Q1, Q2, Q6 and Q7. Resistor R6 insures that the output will charge to within one V_{BE} voltage drop of the V_{CC} supply.

SYSTEM CONSIDERATIONS

Overshoot:

In most system applications the output waveform of the MMH0026 will "overshoot" to some degree. However, "overshoot" can be eliminated or reduced by placing a damping resistor in series with the output. The amount of resistance required is given by: $R_S = 2\sqrt{L/C_L}$ where L is the inductance of the line and C_L is the load capacitance. In most cases a series of damping resistor in the range of 10-to-50 ohms will be sufficient. The damping resistor also affects the transition times of the outputs. The speed reduction is given by the formula:

$t_{THL} \approx t_{TLH} = 2.2\ R_S\ C_L$ (R_S is the damping resistor).

Crosstalk:

The MMH0026 is sensitive to crosstalk when the output voltage level is high ($V_O \approx V_{CC}$). With the output in the high voltage level state, Q3 and Q4 are essentially turned "off". Therefore, negative-going crosstalk will pull the output down until Q4 turns "on" sufficiently to pull the output back towards V_{CC}. This problem can be minimized by placing a "bleeding" resistor from the output to ground. The "bleeding" resistor should be of sufficient size so that Q4 conducts only a few milliamperes. Thus, when noise is coupled, Q4 is already "on" and the line is quickly clamped by Q4. Also note that in Figure 1 D6 clamps the output one diode-voltage drop above V_{CC} for positive-going crosstalk.

Power Supply Decoupling:

The decoupling of V_{CC} and V_{EE} is essential in most systems. Sufficient capacitive decoupling is required to supply the peak surge currents during switching. At least a 0.1-μF to 1.0-μF low inductive capacitor should be placed as close to each driver package as the layout will permit.

Input Driving:

For those applications requiring split power supplies ($V_{EE} < GND$), ac coupling, as illustrated in Figure23, should be employed. Selection of the input capacitor size is determined by the desired output pulse width. Maximum performance is attained when the voltage at

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APPLICATIONS INFORMATION (continued)

the input of the MMH0026 discharges to just above the device's threshold voltage (about 1.5 V). Figure 6 shows optimum values for C_{in} versus the desired output pulse width. The value for C_{in} may be roughly predicted by:

$$C_{in} \doteq (2 \times 10^{-3})\ (PW_O). \qquad (1)$$

For an output pulse width of 500 ns, the optimum value for C_{in} is:

$$C_{in} = (2 \times 10^{-3})\ (500 \times 10^{-9}) = 1000\ pF.$$

If single supply operation is required (V_{EE} = GND), then dc coupling as illustrated in Figure 24 can be employed. For maximum switching performance, a speed-up capacitor should be employed with dc coupling. Figures 12 and 13 show typical switching characteristics for various values of input resistance and capacitance.

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POWER CONSIDERATIONS

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the integrated circuit junction temperatures low. Electrical power dissipated in the integrated circuit is the source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature. The temperature increase depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point. The basic formula for converting power dissipation into junction temperature is:

$$T_J = T_A + P_D\ (R_{\theta JC} + R_{\theta CA}) \qquad (2)$$

or

$$T_J = T_A + P_D\ (R_{\theta JA}) \qquad (3)$$

where

T_J = junction temperature
T_A = ambient temperature
P_D = power dissipation
$R_{\theta JC}$ = thermal resistance, junction to case
$R_{\theta CA}$ = thermal resistance, case to ambient
$R_{\theta JA}$ = thermal resistance, junction to ambient.

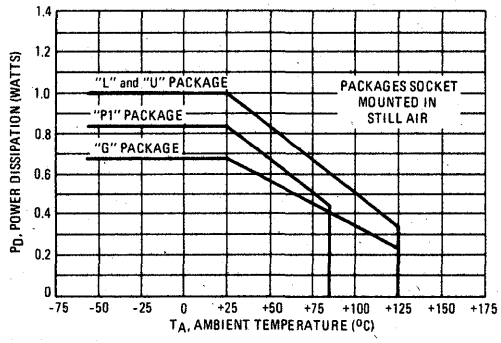
Power Dissipation for the MMH0026 MOS Clock Driver:

The power dissipation of the device (P_D) is dependent on the following system requirements: frequency of operation, capacitive loading, output voltage swing, and duty cycle. This power dissipation, when substituted into equation (3), should not yield a junction temperature, T_J, greater than T_J(max) at the maximum encountered ambient temperature. T_J(max) is specified for three integrated circuit packages in the maximum ratings section of this data sheet.

TABLE 1 – THERMAL CHARACTERISTICS OF "G", "L", "P1", AND "U" PACKAGES

PACKAGE TYPE (Mounted in Socket)	$R_{\theta JA}$ (°C/W) Still Air		$R_{\theta JC}$ (°C/W) Still Air	
	MAX	TYP	MAX	TYP
"G" (Metal Package)	220	175	70	40
"L" (Ceramic Package)	150	100	50	27
"P1" (Plastic Package)	150	100	70	40
"U" (Ceramic Package)	150	100	50	27

FIGURE 17 – MAXIMUM POWER DISSIPATION versus AMBIENT TEMPERATURE (As related to package)



With these maximum junction temperature values, the maximum permissible power dissipation at a given ambient temperature may be determined. This can be done with equations (2) or (3) and the maximum thermal resistance values given in Table 1 or alternately, by using the curves plotted in Figure 17. If, however, the power dissipation determined by a given system produces a calculated junction temperature in excess of the recommended maximum rating for a given package type, something must be done to reduce the junction temperature.

There are two methods of lowering the junction temperature without changing the system requirements. First, the ambient temperature may be reduced sufficiently to bring T_J to an acceptable value. Secondly, the $R_{\theta CA}$ term can be reduced. Lowering the $R_{\theta CA}$ term can be accomplished by increasing the surface area of the package with the addition of a heat sink or by blowing air across the package to promote improved heat dissipation.

APPLICATIONS INFORMATION (continued)

The following examples illustrate the thermal considerations necessary to increase the power capability of the MMH0026.

Assume that the ceramic package is to be used at a maximum ambient temperature (T_A) of +70°C. From Table 1: $R_{\theta JA(max)}$ = 150°C/watt, and from the maximum rating section of the data sheet: $T_J(max)$ = +175°C. Substituting the above values into equation (3) yields a maximum allowable power dissipation of 0.7 watts. Note that this same value may be read from Figure 17. Also note that this power dissipation value is for the device mounted in a socket.

Next, the maximum power consumed for a given system application must be determined. The power dissipation of the MOS clock driver is conveniently divided into dc and ac components. The dc power dissipation is given by:

$$P_{dc} = (V_{CC} - V_{EE}) \times (I_{CCL}) \times (\text{Duty Cycle}) \qquad (4)$$

$$\text{where } I_{CCL} = 40\ \text{mA}\ (\frac{V_{CC} - V_{EE}}{20\ \text{V}}).$$

Note that Figure 14 is a plot of equation (4) for three values of (V_{CC}–V_{EE}). For this example, suppose that the MOS clock driver is to be operated with V_{CC} = +16 V and V_{EE} = GND and with a 50% duty cycle. From equation (4) or Figure 14, the dc power dissipation (per driver) may be found to be 256 mW. If both drivers within the package are used in an identical way, the total dc power is 512 mW. Since the maximum total allowable power dissipation is 700 mW, the maximum ac power that can be dissipated for this example becomes:

$$P_{ac} = 0.7 - 0.512 = 188\ \text{mW}$$

The ac power for each driver is given by:

$$P_{ac} = (V_{CC} - V_{EE})^2 \times f \times C_L \qquad (5)$$

where f = frequency of operation

C_L = load capacitance (including all strays and wiring).

Figure 16 gives the maximum ac power dissipation versus switching frequency for various capacitive loads with V_{CC} = 16 V and V_{EE} = GND. Under the above conditions, and with the aid of Figure 15, the safe operating area beneath Curve A of Figure 18 can be generated.

Since both drivers have a maximum ac power dissipation of 188 mW, the maximum ac power per driver becomes 94 mW. A horizontal line intersecting all the capacitance load lines at the 94 mW level of Figure 15 will yield the maximum frequency of operation for each of the capacitive loads at the specified power level. By using the previous formulas and constants, a new safe operating area can be generated for any output voltage swing and duty cycle desired.

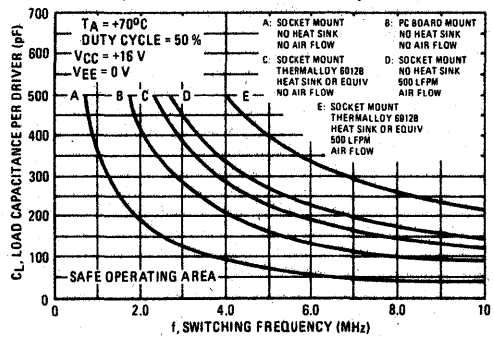
Note from Figure 18, that with highly capacitive loads, the maximum switching frequency is very low. The switching frequency can be increased by varying the following factors:

(a) decrease T_A
(b) decrease the duty cycle
(c) lower package thermal resistance ($R_{\theta JA}$)

In most cases conditions (a) and (b) are fixed due to system requirements. This leaves only the thermal resistance $R_{\theta JA}$ that can be varied.

Note from equation (2) that the thermal resistance is comprised of two parts. One is the junction-to-case thermal resistance ($R_{\theta JC}$) and the other is the case-to-ambient thermal resistance ($R_{\theta CA}$). Since the factor $R_{\theta JC}$ is a function of the die size and type of bonding employed, it cannot be varied. However, the $R_{\theta CA}$ term can be changed as previously discussed, see Page 7.

FIGURE 18 – LOAD CAPACITANCE versus FREQUENCY FOR "L" PACKAGE ONLY
(Both drivers used in identical way)



Heat Sink Considerations:

Heat sinks come in a wide variety of sizes and shapes that will accomodate almost any IC package made. Some of these heat sinks are illustrated in Figure 19. In the previous example, with the ceramic package, no heat sink and in a still air environment, $R_{\theta JA(max)}$ was 150°C/W.

For the following example the Thermalloy 6012B type heat sink, or equivalent, is chosen. With this heat sink, the $R_{\theta CA}$ for natural convection from Figure 20 is 44°C/W. From Table 1 $R_{\theta JC(max)}$ = 50°C/W for the ceramic

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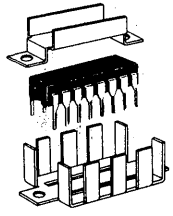
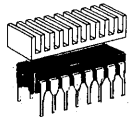
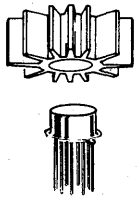
APPLICATIONS INFORMATION (continued)

FIGURE 19 – THERMALLOY* HEAT SINKS


6007A


6012B


2230-5

*Manufactured by Thermalloy Co. of Texas.

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package. Therefore, the new $R_{\theta JA}$(max) with the 6012B heat sink added becomes:

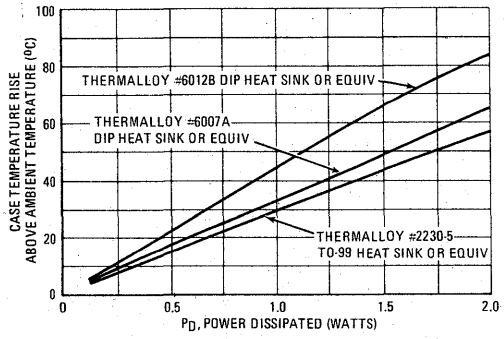
$R_{\theta JA(max)} = 50^oC/W + 44^oC/W = 94^oC/W.$

Thus the addition of the heat sink has reduced $R_{\theta JA}$(max) from 150°C/W down to 94°C/W. With the heat sink, the maximum power dissipation by equation (3) at T_A = +70°C is:

$$P_D = \frac{175^oC - 70^oC}{94^oC/W} = 1.11 \text{ watts.}$$

This gives approximately a 58% increase in maximum power dissipation. The safe operating area under Curve C of Figure 18 can now be generated as before with the aid of Figure 15 and equation (5).

FIGURE 20 – CASE TEMPERATURE RISE ABOVE AMBIENT versus POWER DISSIPATED USING NATURAL CONVECTION



Forced Air Considerations:

As illustrated in Figure 21, forced air can be employed to reduce the $R_{\theta JA}$ term. Note, however, that this curve is expressed in terms of typical $R_{\theta JA}$ rather than maximum $R_{\theta JA}$. Maximum $R_{\theta JA}$ can be determined in the following manner:

From Table 1 the following information is known:

(a) $R_{\theta JA(typ)} = 100^o$ C/W
(b) $R_{\theta JC(typ)} = 27^o$ C/W

Since:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad (6)$$

Then:

$$R_{\theta CA} = R_{\theta JA} - R_{\theta JC} \quad (7)$$

Therefore, in still air

$R_{\theta CA(typ)} = 100^oC/W - 27^oC/W = 73^oC/W$

From Curve 1 of Figure 21 at 500 LFPM and equation (7),

$R_{\theta CA(typ)} = 53^oC/W - 27^oC/W = 26^oC/W.$

Thus $R_{\theta CA}$(typ) has changed from 73°C/W (still air) to 26°C/W (500 LFPM), which is a decrease in typical $R_{\theta CA}$ by a ratio of 1:2.8. Since the typical value of $R_{\theta CA}$ was reduced by a ratio of 1:2.8, $R_{\theta CA}$(max) of 100°C/W should also decrease by a ratio of 1:2.8.

This yields an $R_{\theta CA(max)}$ at 500 LFPM of 36°C/W.

Therefore, from equation (6):

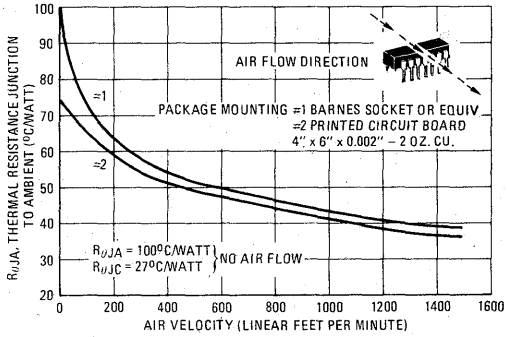
$R_{\theta JA(max)} = 50^oC/W + 36^oC/W = 86^oC/W.$

Therefore the maximum allowable power dissipation at 500 LFPM and T_A = +70°C is from equation (3):

$$P_D = \frac{175^oC - 70^oC}{+86^oC/W} = 1.2 \text{ watts.}$$

APPLICATIONS INFORMATION (continued)

FIGURE 21 – TYPICAL THERMAL RESISTANCE ($R_{\theta JA}$) OF "L" PACKAGE versus AIR VELOCITY



As with the previous examples, the dc power at 50% duty cycle is subtracted from the maximum allowable device dissipation (P_D) to obtain a maximum P_{ac}. The safe operating area under Curve D of Figure 18 can now be generated from Figure 15 and equation (5).

Heat Sink and Forced Air Combined:

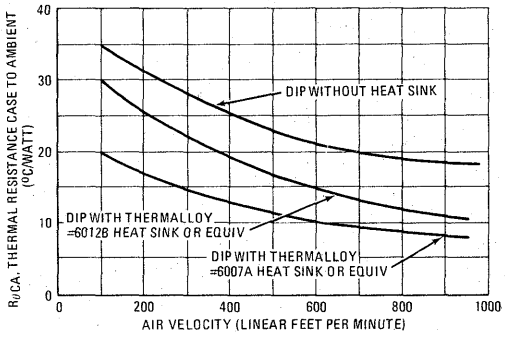
Some heat sink manufacturers provide data and curves of $R_{\theta CA}$ for still air and forced air such as illustrated in Figure 22. For example the 6012B heat sink has an $R_{\theta CA}$ = 17°C/W at 500 LFPM as noted in Figure 22. From equation (6):

$$\text{Max } R_{\theta JA} = 50^{\circ}C/W + 17^{\circ}C/W = 67^{\circ}C/W$$

From equation (3) at T_A = +70°C

$$P_D = \frac{175^{\circ}C - 70^{\circ}C}{67^{\circ}C/W} = 1.57 \text{ watts.}$$

FIGURE 22 – THERMAL RESISTANCE $R_{\theta CA}$ versus AIR VELOCITY



As before this yields a safe operating area under Curve E in Figure 18.

Note from Table 1 and Figure 21 that if the 14-pin ceramic package is mounted directly to the PC board (2 oz. cu. underneath), that typical $R_{\theta JA}$ is considerably less than for socket mount with still air and no heat sink. The following procedure can be employed to determine a safe operating area for this condition.

Given data from Table 1:

$$\text{typical } R_{\theta JA} = 100^{\circ}C/W$$
$$\text{typical } R_{\theta JC} = 27^{\circ}C/W$$

From Curve 2 of Figure 21, $R_{\theta JA}$(typ) is 75°C/W for a PC mount and no air flow. Then the typical $R_{\theta CA}$ is 75°C/W – 27°C/W = 48°C/W. From Table 1 the typical value of $R_{\theta CA}$ for socket mount is 100°C/W – 27°C/W = 73°C/W. This shows that the PC board mount results in a decrease in typical $R_{\theta CA}$ by a ratio of 1:1.5 below the typical value of $R_{\theta CA}$ in a socket mount. Therefore, the maximum value of socket mount $R_{\theta CA}$ of 100°C/W should also decrease by a ratio of 1:1.5 when the device is mounted in a PC board. The maximum $R_{\theta CA}$ becomes:

$$R_{\theta CA} = \frac{100^{\circ}C/W}{1.5} = 66^{\circ}C/W \text{ for PC board mount}$$

Therefore the maximum $R_{\theta JA}$ for a PC mount is from equation (6).

$$R_{\theta JA} = 50^{\circ}C/W + 66^{\circ}C/W = 116^{\circ}C/W.$$

With maximum $R_{\theta JA}$ known, the maximum power dissipation can be found and the safe operating area determined as before. See Curve B in Figure 18.

CONCLUSION

In most cases, heat sink manufacturer's publish only $R_{\theta CA}$ socket mount data. Although $R_{\theta CA}$ data for PC mounting is generally not available, this should present no problem. Note in Figure 21 that an air flow greater than 250 LFPM yields a socket mount $R_{\theta JA}$ approximately 6% greater than for a PC mount. Therefore, the socket mount data can be used for a PC mount with a slightly greater safety factor. Also it should be noted that thermal resistance measurements can vary widely. These measurement variations are due to the dependency of $R_{\theta CA}$ on the type environment and measurement techniques employed. For example, $R_{\theta CA}$ would be greater for an integrated circuit mounted on a PC board with little or no ground plane versus one with a substantial ground plane. Therefore, if the maximum calculated junction temperature is on the border line of being too high for a given system application, then thermal resistance measurements should be done on the system to be absolutely certain that the maximum junction temperature is not exceeded.

5

TYPICAL APPLICATIONS

FIGURE 23 – AC-COUPLED MOS CLOCK DRIVER

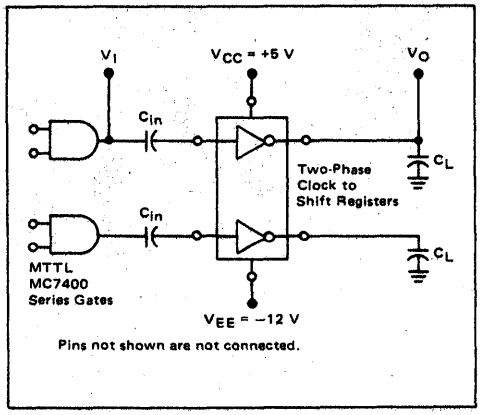
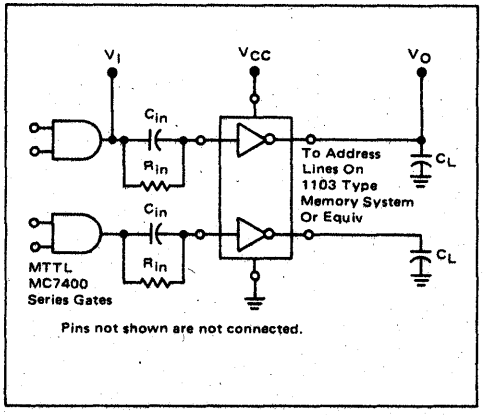
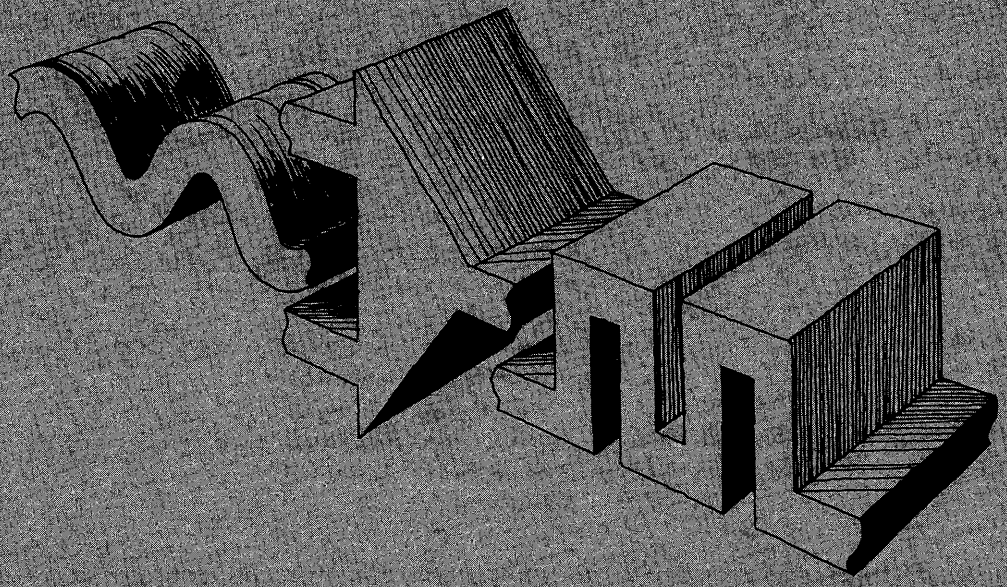


FIGURE 24 – DC-COUPLED RAM MEMORY ADDRESS OR PRECHARGE DRIVER (POSITIVE-SUPPLY ONLY)





Voltage Comparators / Chapter 6

VOLTAGE COMPARATORS

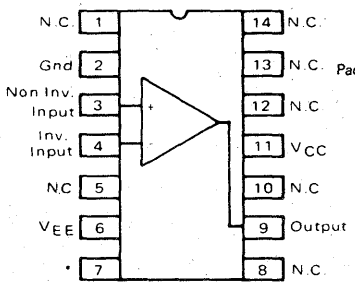
Temperature Range 0 to 70°C	Temperature Range -55 to 125°C	Other		Page
MC1414	MC1514	—	Dual MC1710 Differential Comparator	6-5
MC1710C	MC1710	—	Differential Comparator	6-9
MC1711C	MC1711	—	Dual Differential Comparator	6-13
—	—	MC3302	Quad Comparator	6-17
XC3411	—	—	Dual Comparator	6-21
MC3430-33	—	—	High-Speed Quad Comparators	6-23
MLM311	MLM111	MLM211	High-Performance Comparator	6-31
MLM339	MLM139	MLM239	Quad Comparator (Single Supply)	6-35
MLM339A	MLM139A	MLM239A	Quad Comparator (Single Supply)	6-39
—	—	MLM2901	Quad Comparator	6-43

VOLTAGE COMPARATORS

General Purpose Comparators

. . . for detecting the polarity relationship between two analog levels and giving a corresponding TTL output.

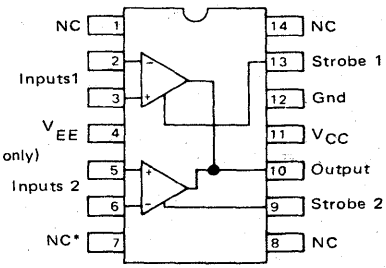
MC1710 – T_A = -55 to 125°C
MC1710C – T_A = 0 to 70°C
Single comparators



*Connected to pin 6 via the substrate on some plastic units.

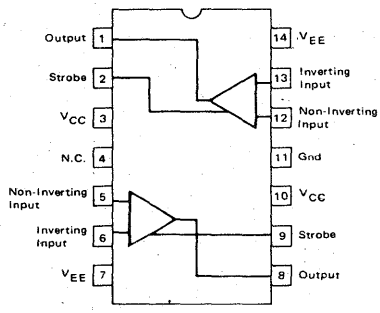
Packages:
G Suffix – Case 601
F Suffix – Case 606
L Suffix – Case 632
P Suffix – Case 646 (for MC1710C, MC1711C only)

MC1711 – T_A = -55 to 125°C
MC1711C – T_A = 0 to 70°C
Dual comparators with strobes and wire-ORed outputs



*Connected to pin 4 via the substrate on some plastic units.

MC1514 – T_A = -55 to 125°C
MC1414 – T_A = 0 to 70°C
Dual comparators with strobes.



Packages:
F Suffix – Case 607
L Suffix – Case 632
P Suffix – Case 646 (MC1414 only)

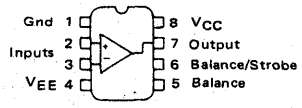
Device Number	V_{IO} mV Max	I_{IB} µA Max	A_{VOL} V/V Min
MC1710C	5.0	25	1000
MC1710	2.0	20	1250
MC1711C	5.0	100	700
MC1711	3.5	75	700
MC1514	2.0	20	1250
MC1414	5.0	25	1000

6

Precision Comparators

. . . featuring low input loading, high voltage gain, and a choice of either dual or single positive power supply operation.

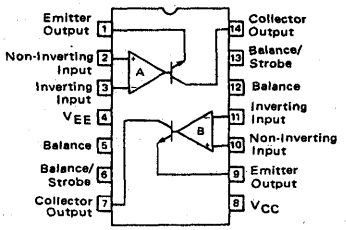
MLM111 – T_A = -55 to 125°C
MLM211 – T_A = -25 to 85°C
MLM311 – T_A = 0 to 70°C
Single comparators; high gain, high input impedance; strobe and balance inputs provided.



Packages:
G Suffix – Case 601
F Suffix – Case 606
L Suffix – Case 632
P1 Suffix – Case 626 (MLM311 only)

MC3411 – T_A = 0 to 70°C
Dual 311-type comparator.

Packages:
L Suffix – Case 632
P Suffix – Case 646



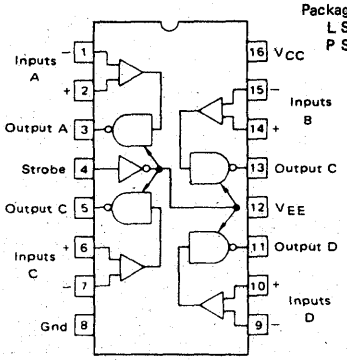
Device Number	V_{IO} mV Max	I_{IB} nA Max	V_{OL} @ I_{OL} = 50 mA Volts Max
MLM111	3.0	100	1.5
MLM211	3.0	100	1.5
MLM311	7.5	250	1.5
MC3411	7.5	250	1.5

Quad Comparators . . . for applications requiring multiple comparators.

MC3430
MC3431 } – High-speed quad comparators with three-state Enable common to all four devices; ±5 volt supply; T_A = 0 to 70°C.

MC3432
MC3433 } – Quad comparators with open collector outputs, common strobe input; ±5 volt supply; T_A = 0 to 70°C.

Packages:
L Suffix – Case 620
P Suffix – Case 648



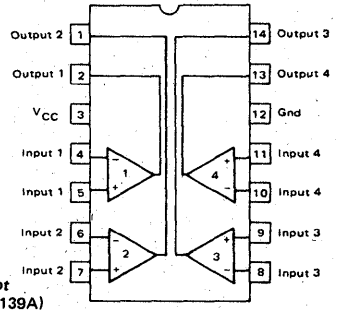
Device Number	V_{IS} mV Max	I_{IB} µA Max	t_{PHL} ns Max
MC3430	±6.0	20	45
MC3431	±10	20	45
MC3432	±6.0	20	50
MC3433	±10	20	50

MLM139
MLM139A } – T_A = -55 to 125°C

MC3302
MLM239
MLM239A } – T_A = -40 to 85°C

MLM339
MLM339A } – T_A = 0 to 70°C

Single supply voltage comparators.



Packages:
L Suffix – Case 632
P Suffix – Case 646 (For all devices *except* MLM139, MLM139A)

Device Number	V_{IO} @ 25°C mV Max	I_{IB} @ 25°C nA Max	I_{sink} @ V_{OL} = 500 mV mA Min	V_{OL} @ I_{OL} = 2.0 mA* @ I_{OL} = 4.0 mA mV Max
MC3302	20	1000	–	400*
MLM139	5.0	100	6.0	500
MLM139A	2.0	100	6.0	500
MLM239	5.0	250	6.0	500
MLM239A	2.0	250	6.0	500
MLM339	5.0	250	6.0	500
MLM339A	2.0	250	6.0	500

ORDERING INFORMATION

Device	Temperature Range	Package
MC1414L	0°C to +75°C	Ceramic DIP
MC1414P	0°C to +75°C	Plastic DIP
MC1514L	−55°C to +125°C	Ceramic DIP

MC1414
MC1514

DUAL DIFFERENTIAL VOLTAGE COMPARATOR

. . . designed for use in level detection, low-level sensing, and memory applications.

- Two Separate Outputs
- Strobe Capability
- High Output Sink Current
  2.8 mA Minimum (Each Comparator) for MC1514
  1.6 mA minimum (Each Comparator) for MC1414
- Differential Input Characteristics
  Input Offset Voltage = 1.0 mV for MC1514
  = 1.5 mV for MC1414
  Offset Voltage Drift = 3.0 μV/°C for MC1514
  = 5.0 μV/°C for MC1414
- Short Propagation Delay Time — 40 ns typical
- Output Compatible with All Saturating Logic Forms
  V_O = +3.2 V to -0.5 V typical

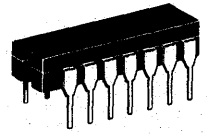
DUAL DIFFERENTIAL COMPARATOR

(DUAL MC1710)

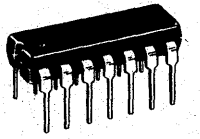
MONOLITHIC SILICON INTEGRATED CIRCUIT

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+14 -7.0	Vdc
Differential Mode Input Voltage Range	V_{IDR}	±5.0	Vdc
Common Mode Input Voltage Range	V_{ICR}	±7.0	Vdc
Peak Load Current	I_L	10	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		1000	mW
Derate above T_A = 25°C		6.0	mW/°C
Ceramic Flat Package		500	mW
Derate above T_A = 25°C		3.3	mW/°C
Plastic Dual In-Line Package		625	mW
Derate above T_A = 25°C		5.0	mW/°C
Operating Temperature Range MC1514 MC1414	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

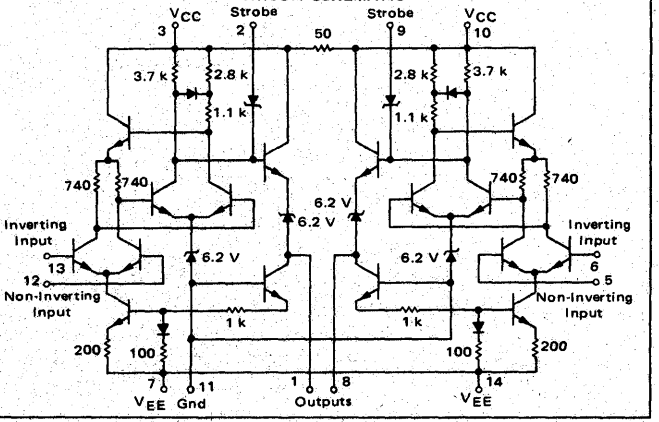


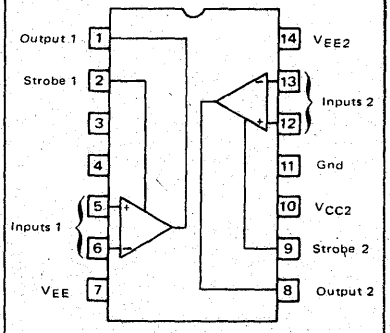
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1414 only)

CIRCUIT SCHEMATIC





6

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, V_{EE} = -6 Vdc, T_A = 25°C unless otherwise noted.) (Each Comparator)

Characteristic	Symbol	MC1514 Min	MC1514 Typ	MC1514 Max	MC1414 Min	MC1414 Typ	MC1414 Max	Unit
Input Offset Voltage	V_{IO}							mVdc
(V_O = 1.4 Vdc, T_A = 25°C)		–	1.0	2.0	–	1.5	5.0	
(V_O = 1.8 Vdc, T_A = T_{low}*)		–	–	3.0	–	–	6.5	
(V_O = 1.0 Vdc, T_A = T_{high}*)		–	–	3.0	–	–	6.5	
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	3.0	–	–	5.0	–	μV/°C
Input Offset Current	I_{IO}							μAdc
(V_O = 1.4 Vdc, T_A = 25°C)		–	1.0	3.0	–	1.0	5.0	
(V_O = 1.8 Vdc, T_A = T_{low})		–	–	7.0	–	–	7.5	
(V_O = 1.0 Vdc, T_A = T_{high})		–	–	3.0	–	–	7.5	
Input Bias Current	I_{IB}							μAdc
(V_O = 1.4 Vdc, T_A = 25°C)		–	12	20	–	15	25	
(V_O = 1.8 Vdc, T_A = T_{low})		–	–	45	–	18	40	
(V_O = 1.0 Vdc, T_A = T_{high})		–	–	20	–	–	40	
Open Loop Voltage Gain	A_{vol}							V/V
(T_A = 25°C)		1250	1700	–	1000	1500	–	
(T_A = T_{low} to T_{high})		1000	–	–	800	–	–	
Output Resistance	R_O	–	200	–	–	200	–	ohms
Differential Voltage Range	V_{IDR}	±5.0	–	–	±5.0	–	–	Vdc
High Level Output Voltage ($V_{ID} \geq 5.0$ mV, $0 \leq I_O \leq 5.0$ mA)	V_{OH}	2.5	3.2	4.0	2.5	3.2	4.0	Vdc
Low Level Output Voltage	V_{OL}							Vdc
($V_{ID} \geq -5.0$ mV, I_{OS} = 2.8 mA)		-1.0	-0.5	0	–	–	–	
($V_{ID} \geq -5.0$ mV, I_{OS} = 1.6 mA)		–	–	–	-1.0	-0.5	0	
Output Sink Current ($V_{ID} \geq -5.0$ mV, $V_{OL} \leq 0.4$ V, T_A = T_{low} to T_{high})	I_{OS}	2.8	3.4	–	1.6	2.5	–	mAdc
Input Common Mode Voltage Range (V_{EE} = -7.0 Vdc)	V_{ICR}	±5.0	–	–	±5.0	–	–	Vdc
Common-Mode Rejection Ratio (V_{EE} = -7.0 Vdc, $R_S \leq 200\ \Omega$)	CMRR	80	100	–	70	100	–	dB
Strobe Low Level Current (V_{IL} = 0)	I_{IL}	–	–	2.5	–	–	2.5	mA
Strobe High Level Current (V_{IH} = 5.0 Vdc)	I_{IH}	–	–	1.0	–	–	1.0	μA
Strobe Disable Voltage ($V_{OL} \leq 0.4$ Vdc)	V_{IL}	–	–	0.4	–	–	0.4	Vdc
Strobe Enable Voltage ($V_{OH} \geq 2.4$ Vdc)	V_{IH}	3.5	–	6.0	3.5	–	6.0	Vdc
Propagation Delay Time (Figure 1)	t_{PLH}	–	20	–	–	20	–	ns
	t_{PHL}	–	40	–	–	40	–	
Strobe Response Time (Figure 2)	t_{so}	–	15	–	–	15	–	ns
	t_{sr}	–	6.0	–	–	6.0	–	
Total Power Supply Current, Both Comparators	I_{CC}	–	12.8	18	–	12.8	18	mAdc
($V_O \leq 0$)	I_{EE}	–	11	14	–	11	14	
Total Power Consumption, Both Comparators	P_D	–	230	300	–	230	300	mW

*T_{low} = -55°C for MC1514, 0°C for MC1414
T_{high} = +125°C for MC1514, +75°C for MC1414

FIGURE 1 – PROPAGATION DELAY TIME

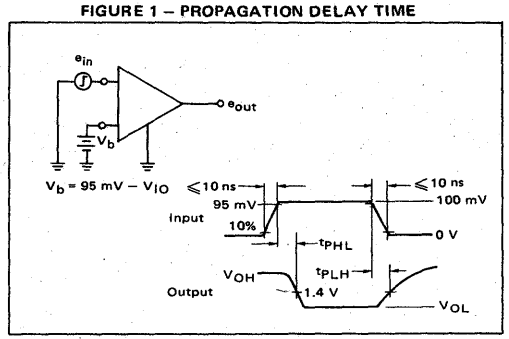
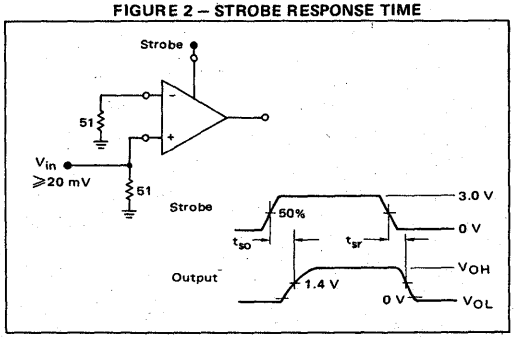


FIGURE 2 – STROBE RESPONSE TIME



TYPICAL CHARACTERISTICS

(Each Comparator)

FIGURE 3 – VOLTAGE TRANSFER CHARACTERISTICS

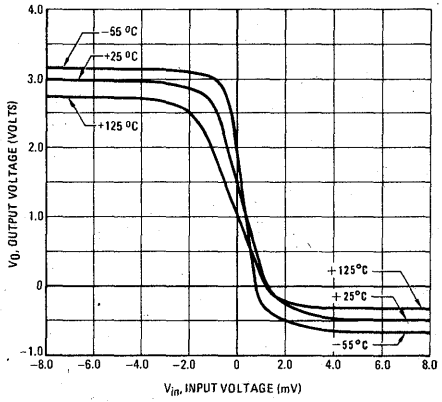


FIGURE 4 – INPUT OFFSET VOLTAGE versus TEMPERATURE

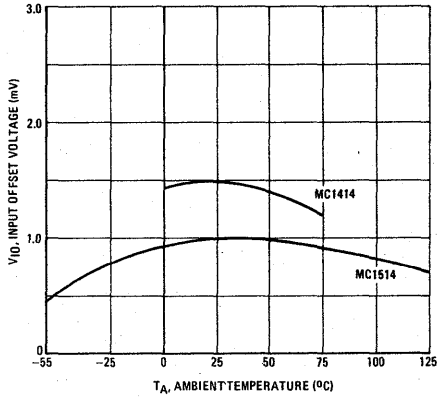


FIGURE 5 – INPUT OFFSET CURRENT versus TEMPERATURE

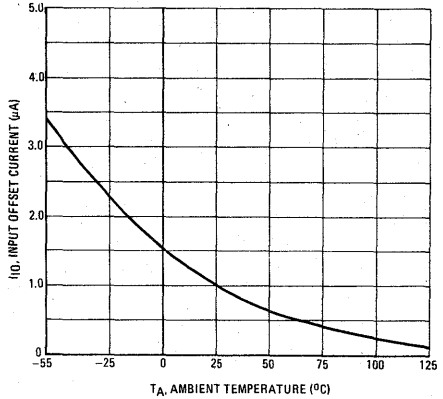


FIGURE 6 – INPUT BIAS CURRENT versus TEMPERATURE

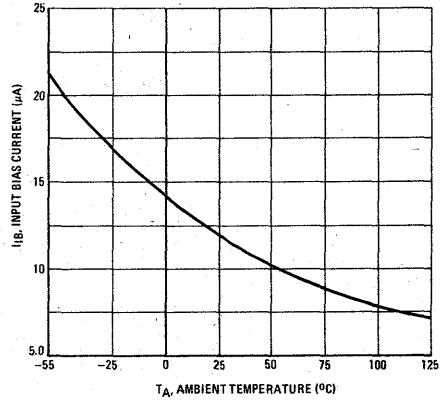


FIGURE 7 – GAIN VARIATION WITH POWER SUPPLY VOLTAGE

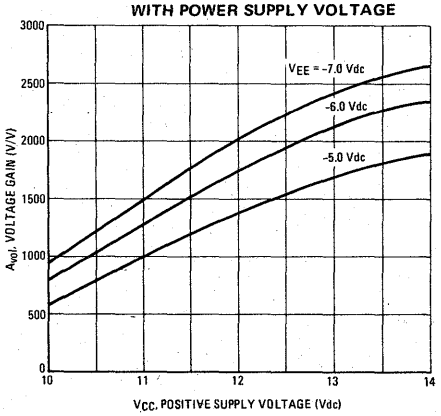


FIGURE 8 – VOLTAGE GAIN versus TEMPERATURE

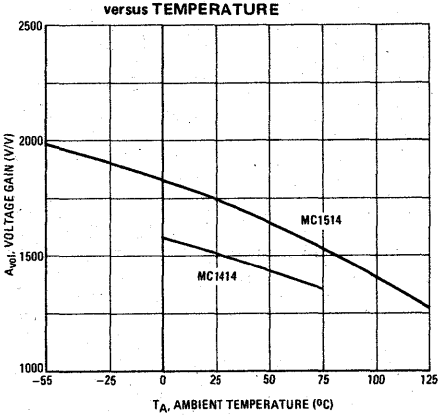


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FIGURE 9 – RESPONSE TIME

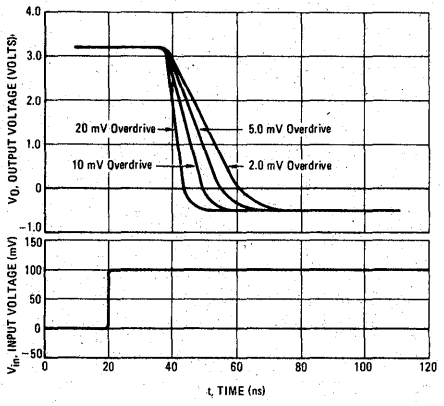


FIGURE 10 – POWER DISSIPATION versus TEMPERATURE

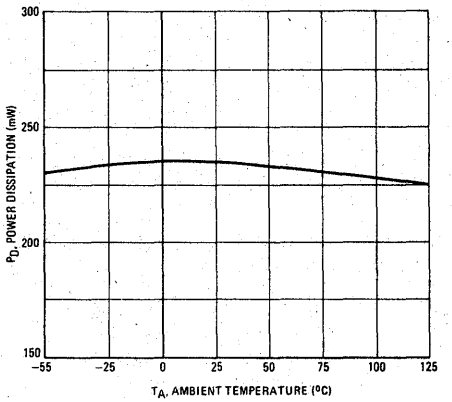


FIGURE 11 – RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

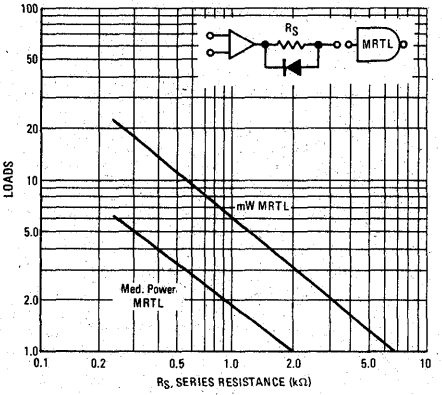


FIGURE 12 – SINK CURRENT versus TEMPERATURE

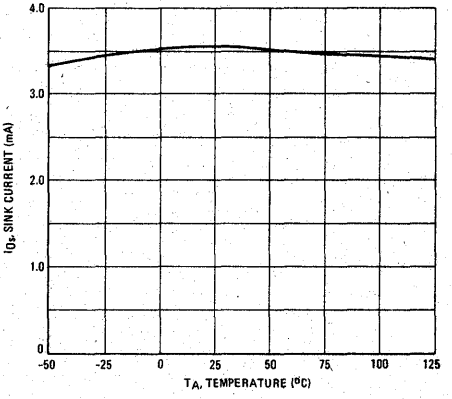
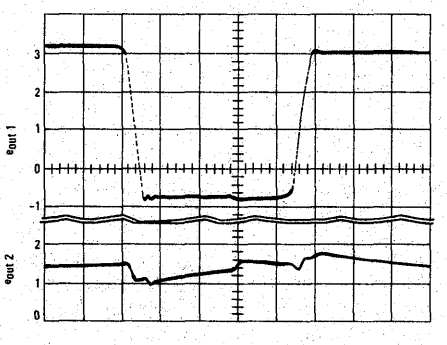
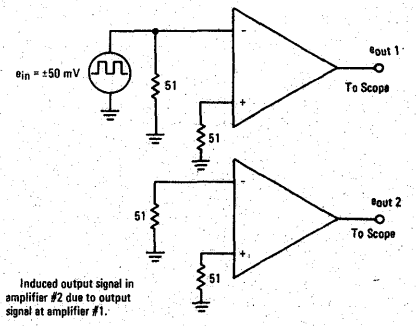


FIGURE 13 – CROSSTALK†





†Worst case condition shown – no load.

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1710F	—	−55°C to +125°C	Ceramic Flat
MC1710G	—	−55°C to +125°C	Metal Can
MC1710L	—	−55°C to +125°C	Ceramic DIP
MC1710CF	—	0°C to +75°C	Ceramic Flat
MC1710CG	LM710CH, μA710HC	0°C to +75°C	Metal Can
MC1710CP	—	0°C to +75°C	Plastic DIP
MC1710CL	—	0°C to +75°C	Ceramic DIP

MC1710
MC1710C

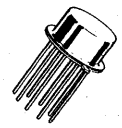
DIFFERENTIAL VOLTAGE COMPARATORS

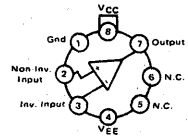
. . . designed for use in level detection, low-level sensing, and memory applications.

- Differential Input Characteristics –
  Input Offset Voltage = 1.0 mV – MC1710
  = 1.5 mV – MC1710C
  Offset Voltage Drift = 3.0 μV/°C – MC1710
  = 5.0 μV/°C – MC1710C
- Fast Response Time – 40 ns
- Output Compatible with all Saturating Logic Forms –
  V_O = +3.2 V to -0.5 V (Typ)
- Low Output Impedance – 200 Ohms

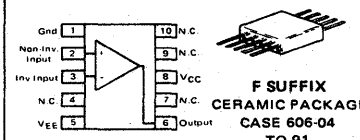
DIFFERENTIAL COMPARATORS

MONOLITHIC SILICON INTEGRATED CIRCUIT

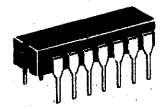




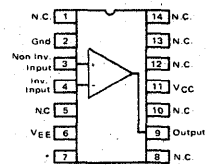
G SUFFIX
METAL PACKAGE
CASE 601



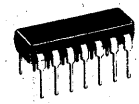
F SUFFIX
CERAMIC PACKAGE
CASE 606-04
TO-91



L SUFFIX
CERAMIC PACKAGE
CASE 632-02
TO-116



*Connected to pin 6 via the substrate on some plastic units.

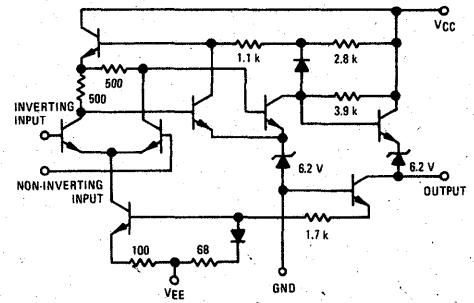


P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1710C Only)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating		Symbol	Value	Unit
Power Supply Voltage		$V_{CC(max)}$ $V_{EE(max)}$	+14 -7.0	Vdc Vdc
Differential Input Signal Voltage		V_{ID}	±5.0	Volts
Common Mode Input Swing Voltage		V_{ICR}	±7.0	Volts
Peak Load Current		I_L	10	mA
Power Dissipation (Package Limitations) Metal Package Derate above T_A = +25°C Flat Package Derate above T_A = +25°C Ceramic Dual In-Line Package Derate above T_A = +25°C		P_D	 680 4.6 500 3.3 625 5.0	 mW mW/°C mW mW/°C mW mW/°C
Operating Temperature Range	MC1710 MC1710C	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Offset Voltage		V_{IO}				mVdc
(V_O = 1.4 Vdc, T_A = +25°C)	MC1710		–	1.0	2.0	
	MC1710C		–	1.0	5.0	
(V_O = 1.8 Vdc, T_A = -55°C)	MC1710		–	–	3.0	
(V_O = 1.0 Vdc, T_A = +125°C	MC1710		–	–	3.0	
(V_O = 1.5 Vdc, T_A = 0°C)	MC1710C		–	–	6.5	
(V_O = 1.2 Vdc, T_A = +75°C)	MC1710C		–	–	6.5	
Temperature Coefficient of Input Offset Voltage		$\Delta V_{IO}/\Delta T$	–	3.0	–	μV/°C
Input Offset Current		I_{IO}				μAdc
(V_O = 1.4 Vdc, T_A = +25°C)	MC1710		–	1.0	3.0	
	MC1710C		–	1.0	5.0	
(V_O = 1.8 Vdc, T_A = -55°C)	MC1710		–	–	7.0	
(V_O = 1.0 Vdc, T_A = +125°C)	MC1710		–	–	3.0	
(V_O = 1.5 Vdc, T_A = 0°C)	MC1710C		–	–	7.5	
(V_O = 1.2 Vdc, T_A = +75°C)	MC1710C		–	–	7.5	
Input Bias Current		I_{IB}				μAdc
(V_O = 1.4 Vdc, T_A = +25°C)	MC1710		–	12	20	
	MC1710C		–	12	25	
(V_O = 1.8 Vdc, T_A = -55°C)	MC1710		–	–	45	
(V_O = 1.0 Vdc, T_A = +125°C)	MC1710		–	–	20	
(V_O = 1.5 Vdc, T_A = 0°C)	MC1710C		–	–	40	
(V_O = 1.2 Vdc, T_A = +75°C)	MC1710C		–	–	40	
Voltage Gain		A_{vol}				V/V
(T_A = +25°C)	MC1710		1250	1700	–	
	MC1710C		1000	1700	–	
(T_A = T_{low} to T_{high}) (1)	MC1710		1000	–	–	
	MC1710C		800	–	–	
Output Resistance		r_o	–	200	–	Ohms
Differential Voltage Range		V_{ID}	±5.0	–	–	Vdc
Positive Output Voltage ($V_{ID} \geq 5.0$ mV, $0 \leq I_O \leq 5.0$ mA)		V_{OH}	2.5	3.2	4.0	Vdc
Negative Output Voltage ($V_{ID} \geq -5.0$ mV)		V_{OL}	-1.0	-0.5	0	Vdc
Output Sink Current		I_{Os}				mAdc
($V_{ID} \geq -5.0$ mV, $V_O \leq 0$)	MC1710		2.0	2.5	–	
	MC1710C		1.6	2.5	–	
($V_{ID} \geq -5.0$ mV, $V_O \geq 0$, $T_A = T_{low}$)	MC1710		1.0	2.0	–	
	MC1710C		0.5	–	–	
Input Common-Mode Voltage Range (V_{EE} = -7.0 Vdc)		V_{ICR}	±5.0	–	–	Volts
Common-Mode Rejection Ratio		C_{MRR}				dB
(V_{EE} = -7.0 Vdc, $R_S \leq 200$ Ohms)	MC1710		80	100	–	
	MC1710C		70	100	–	
Propagation Delay Time for Positive and Negative Going Input Pulse		t_p	–	40	–	ns
Power Supply Current						mAdc
($V_O \leq 0$)		I_{D^+}	–	6.4	9.0	
		I_{D^-}	–	5.5	7.0	
Power Consumption		P_D	–	115	150	mW

(1) T_{low} = -55°C for MC1710, 0°C for MC1710C
T_{high} = +125°C for MC1710, +75°C for MC1710C

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

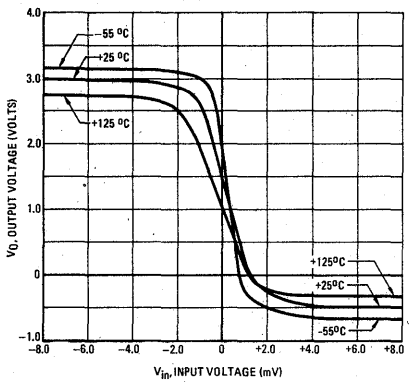


FIGURE 2 – INPUT OFFSET VOLTAGE versus TEMPERATURE

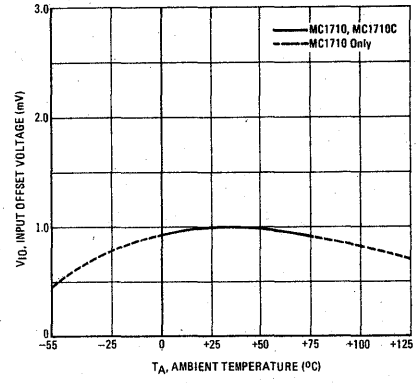


FIGURE 3 – INPUT OFFSET CURRENT versus TEMPERATURE

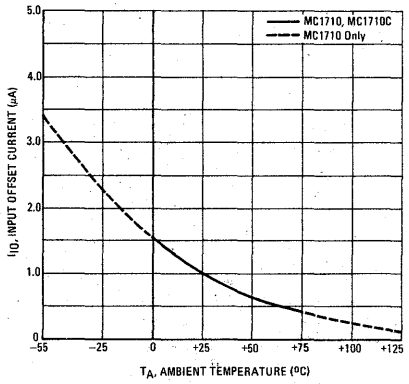


FIGURE 4 – INPUT BIAS CURRENT versus TEMPERATURE

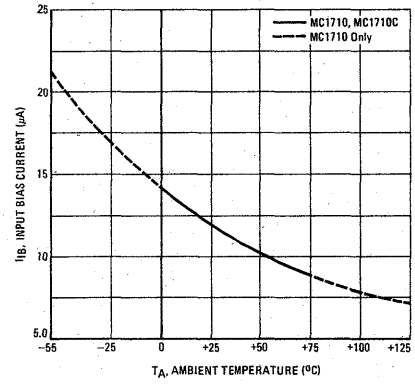


FIGURE 5 – GAIN VARIATION WITH POWER SUPPLY VOLTAGE

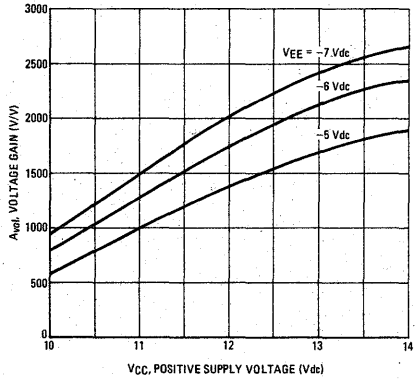


FIGURE 6 – VOLTAGE GAIN versus TEMPERATURE

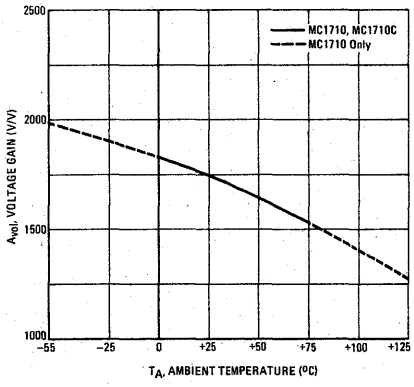


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FIGURE 7 – RESPONSE TIME

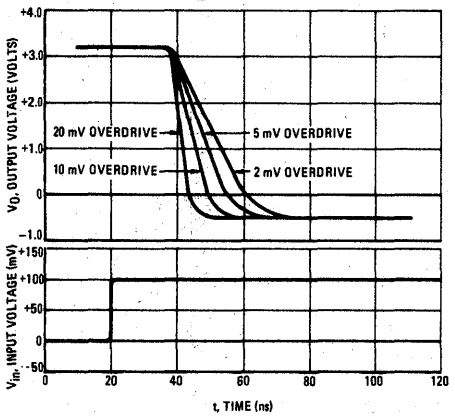


FIGURE 8 – POWER DISSIPATION versus TEMPERATURE

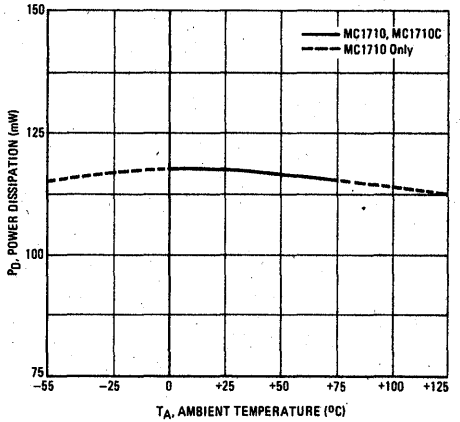
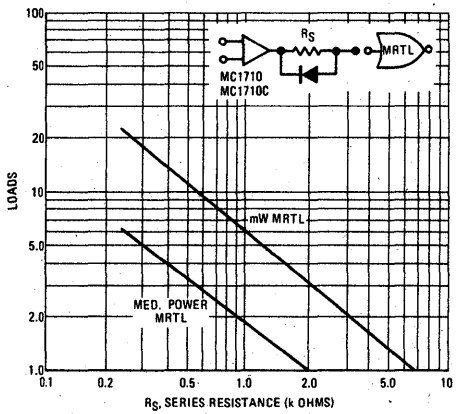
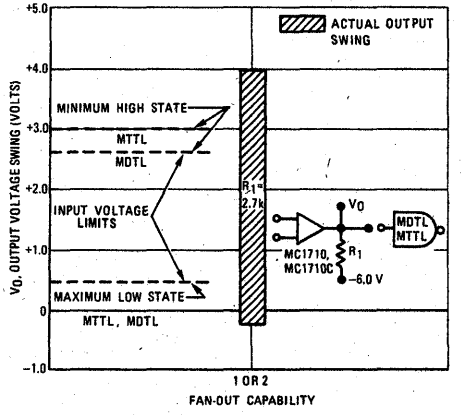


FIGURE 9 – RECOMMENDED SERIES RESISTANCE versus MRTL* LOADS



*Trademark of Motorola, Inc

FIGURE 10 – FAN-OUT CAPABILITY WITH MDTL* OR MTTL* OUTPUT SWING



6

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1711CG	LM711CH,μA711HG	0°C to +75°C	Metal Can
MC1711G	—	−55°C to +125°C	Metal Can
MC1711CL	—	0°C to +75°C	Ceramic DIP
MC1711L	—	−55°C to +125°C	Ceramic DIP
MC1711CF	—	0°C to +75°C	Ceramic Flat
MC1711F	—	−55°C to +125°C	Ceramic Flat
MC1711CP	—	0°C to +75°C	Plastic DIP

MC1711
MC1711C

DUAL DIFFERENTIAL VOLTAGE COMPARATOR

. . . designed for use in level detection, low-level sensing, and memory applications.

Typical Characteristics:

- Differential Input
  - Input Offset Voltage = 1.0 mV
  - Offset Voltage Drift = 5.0 μV/°C
- Fast Response Time — 40 ns
- Output Compatible with All Saturating Logic Forms
  - V_{out} = +4.5 V to -0.5 V typical
- Low Output Impedance — 200 ohms

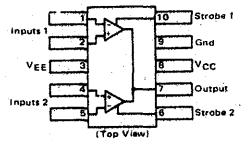
DUAL DIFFERENTIAL COMPARATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

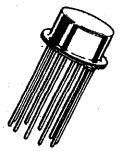
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

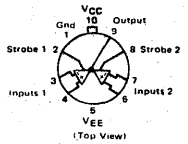
Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC} V_{EE}	+14 -7.0	Vdc
Differential Input Signal Voltage		V_{IDR}	±5.0	Volts
Common-Mode Input Swing Voltage		V_{ICR}	±7.0	Volts
Peak Load Current		I_L	50	mA
Power Dissipation (package limitation)		P_D		
Metal Package			680	mW
Derate above T_A = +25°C			4.6	mW/°C
Flat Ceramic Package			500	mW
Derate above T_A = +25°C			3.3	mW/°C
Ceramic and Plastic Dual In-Line Packages			625	mW
Derate above T_A = +25°C			5.0	mW/°C
Operating Temperature Range	MC1711 MC1711C	T_A	-55 to +125 0 to +75	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

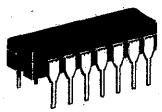


G SUFFIX
METAL PACKAGE
CASE 603
TO-100

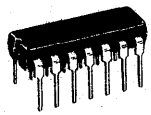


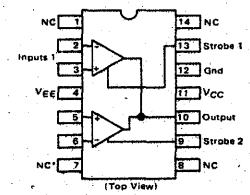


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



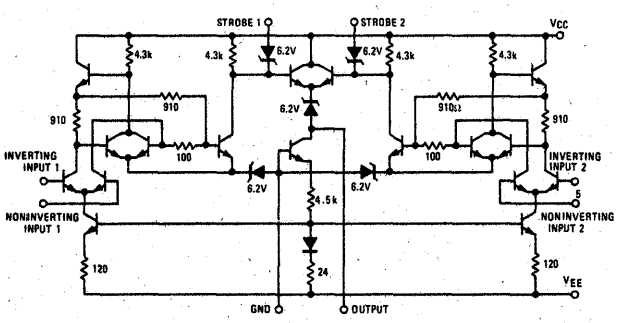
P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1711C only)





*Connected to pin 4 via the substrate on some plastic units.

CIRCUIT SCHEMATIC



6

ELECTRICAL CHARACTERISTICS (each comparator) (V_{CC} = +12 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MC1711 Min	MC1711 Typ	MC1711 Max	MC1711C Min	MC1711C Typ	MC1711C Max	Unit
Input Offset Voltage	V_{IO}							mVdc
(V_{ICR} = 0 Vdc, T_A = +25°C)		–	1.0	3.5	–	1.0	5.0	
($V_{ICR} \neq$ 0 Vdc, T_A = +25°C)		–	1.0	5.0	–	1.0	7.5	
(V_{ICR} = 0 Vdc, T_A = T_{low} to T_{high}*)		–	–	4.5	–	–	6.0	
($V_{ICR} \neq$ 0 Vdc, T_A = T_{low} to T_{high})		–	–	6.0	–	–	10	
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	5.0	–	–	5.0	–	μV/°C
Input Offset Current	I_{IO}							μAdc
(V_O = 1.4 Vdc, T_A = +25°C)		–	0.5	10	–	0.5	15	
(V_O = 1.8 Vdc, T_A = -55°C)		–	–	20	–	–	–	
(V_O = 1.5 Vdc, T_A = 0°C)		–	–	–	–	–	25	
(V_O = 1.0 Vdc, T_A = +125°C)		–	–	20	–	–	–	
(V_O = 1.2 Vdc, T_A = +75°C)		–	–	–	–	–	25	
Input Bias Current	I_{IB}							μAdc
(V_O = 1.4 Vdc, T_A = +25°C)		–	25	75	–	25	100	
(V_O = 1.8 Vdc, T_A = -55°C)		–	–	150	–	–	–	
(V_O = 1.5 Vdc, T_A = 0°C)		–	–	–	–	–	150	
(V_O = 1.0 Vdc, T_A = +125°C)		–	–	150	–	–	–	
(V_O = 1.2 Vdc, T_A = +75°C)		–	–	–	–	–	150	
Voltage Gain	A_{vol}							V/V
(T_A = +25°C)		700	1500	–	700	1500	–	
(T_A = T_{low} to T_{high})		500	–	–	500	–	–	
Output Resistance	R_O	–	200	–	–	200	–	ohms
Differential Voltage Range	V_{IDR}	±5.0	–	–	±5.0	–	–	Vdc
High Level Output Voltage ($V_{ID} \geq$ 10 mVdc, 0 ≤ I_O ≤ 5.0 mA)	V_{OH}	2.5	3.2	5.0	2.5	3.2	5.0	Vdc
Low Level Output Voltage ($V_{ID} \geq$ -10 mVdc)	V_{OL}	-1.0	-0.5	0	-1.0	-0.5	0	Vdc
Strobed Output Level ($V_{strobe} \leq$ 0.3 Vdc)	$V_{OL(st)}$	-1.0	–	0	-1.0	–	0	Vdc
Output Sink Current ($V_{in} \geq$ -10 mV, $V_O \geq$ 0)	I_{Os}	0.5	0.8	–	0.5	0.8	–	mAdc
Strobe Current (V_{strobe} = 100 mVdc)	I_{st}	–	1.2	2.5	–	1.2	2.5	mAdc
Input Common-Mode Range (V_{EE} = -7.0 Vdc)	V_{ICR}	±5.0	–	–	±5.0	–	–	Volts
Response Time (V_b = 5.0 mV + V_{IO})	t_R	–	40	–	–	40	–	ns
Strobe Release Time	t_{SR}	–	12	–	–	12	–	ns
Power Supply Current	I_{CC}	–	8.6	–	–	8.6	–	mAdc
($V_O \leq$ 0 Vdc)	I_{EE}	–	3.9	–	–	3.9	–	
Power Consumption		–	130	200	–	130	200	mW

*T_{low} = -55°C for MC1711, 0°C for MC1711C
T_{high} = +125°C for MC1711, +75°C for MC1711C

TYPICAL CHARACTERISTICS

FIGURE 1 – VOLTAGE TRANSFER CHARACTERISTICS

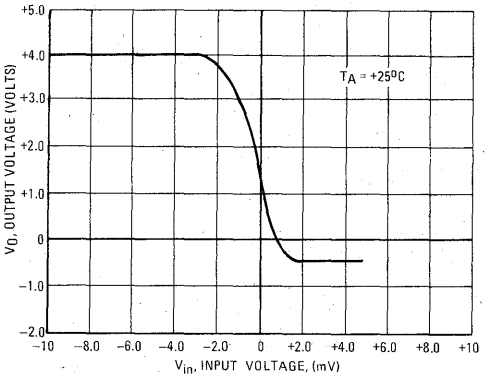


FIGURE 2 – INPUT BIAS CURRENT versus TEMPERATURE

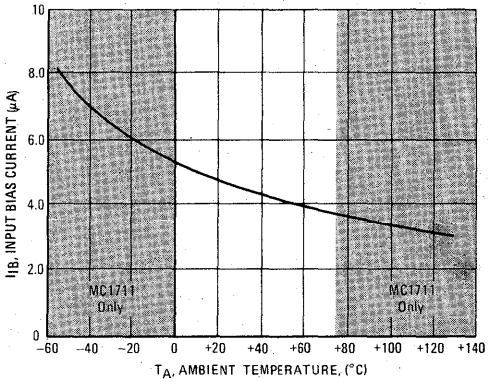


FIGURE 3 – VOLTAGE GAIN versus TEMPERATURE

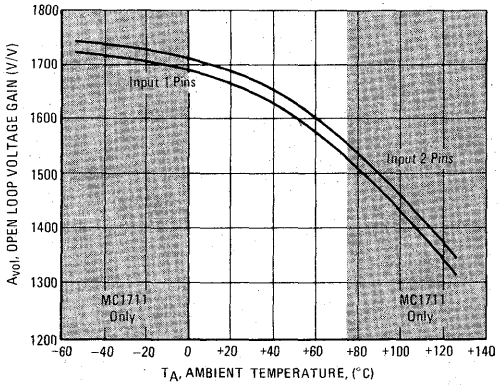


FIGURE 4 – RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

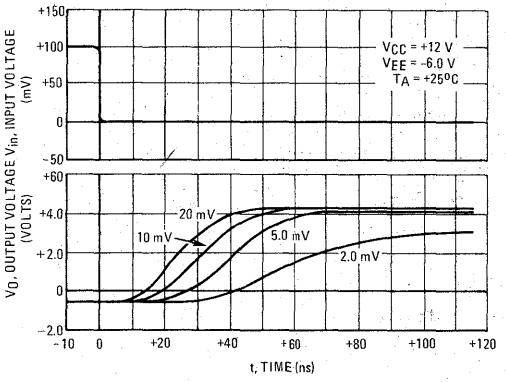


FIGURE 5 – VOLTAGE GAIN VARIATION WITH POWER SUPPLY VOLTAGE

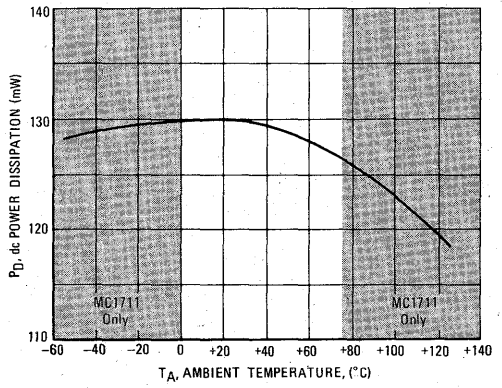


FIGURE 6 – STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES

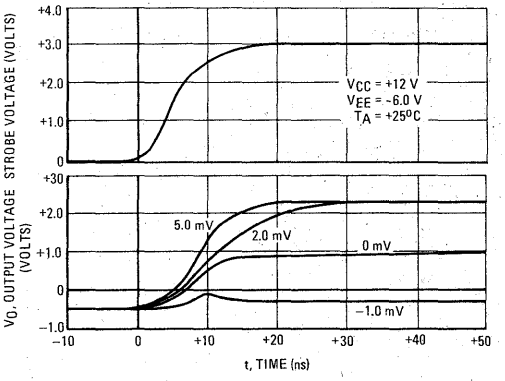


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FIGURE 7 – COMMON-MODE PULSE RESPONSE

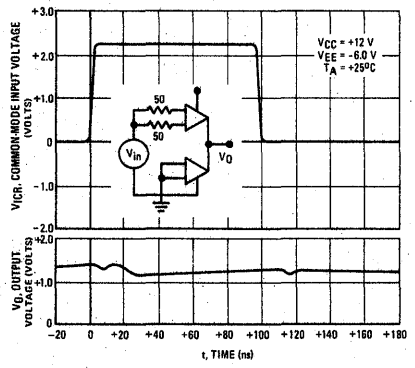


FIGURE 8 – OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING

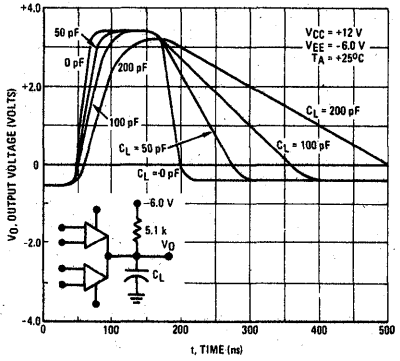


FIGURE 9 – RECOMMENDED SERIES RESISTANCE versus MRTL LOADS

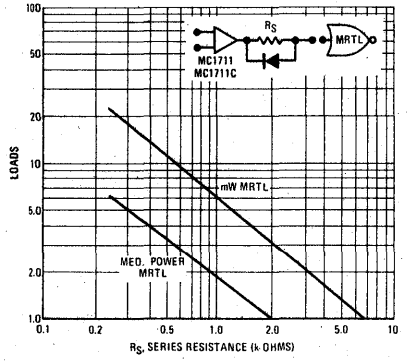
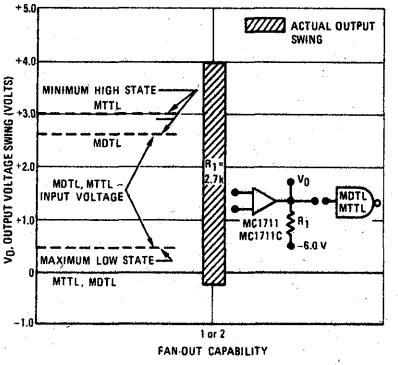


FIGURE 10 – FAN-OUT CAPABILITY WITH MDTL OR MTTL OUTPUT SWING



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ORDERING INFORMATION

Device	Temperature Range	Package
MC3302L	−55°C to +125°C	Ceramic DIP
MC3302P	−40°C to +85°C	Plastic DIP

MC3302P

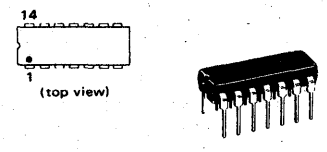
QUAD SINGLE-SUPPLY COMPARATOR

These comparators are designed specifically for single positive-power-supply Consumer Automotive and Industrial electronic applications. Each MC3302P contains four independent comparators – suiting it ideally for usages requiring high density and low-cost.

- Wide Operating Temperature Range – -40 to +85°C
- Single-Supply Operation – +2.0 to +28 Vdc
- Differential Input Voltage = $\pm V_{CC}$
- Compare Voltages at Ground Potential
- MTTL Compatible
- Low Current Drain – 700 μA typical @ V_{CC} +5.0 to +28 Vdc
- Outputs can be Connected to Give the Implied AND Function

QUAD COMPARATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Range	V_{CC}	+2.0 to +28	Vdc
Output Sink Current (See Note 1)	I_O	20	mA
Differential Input Voltage	V_{IDR}	$\pm V_{CC}$	Vdc
Common-Mode Input Voltage Range (See Note 2)	V_{ICR}	-0.3 to +V_{CC}	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	625 5.0	mW mW/°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Note 1. Requires an external resistor, R_L, to limit current below maximum rating.

Note 2. If either (+) or (−) inputs of any comparator go more than several tenths of a volt below ground, a parasitic transistor turns "on" causing high input current and possible faulty outputs.

FIGURE 1 – EQUIVALENT CIRCUIT

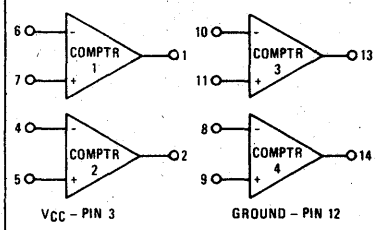
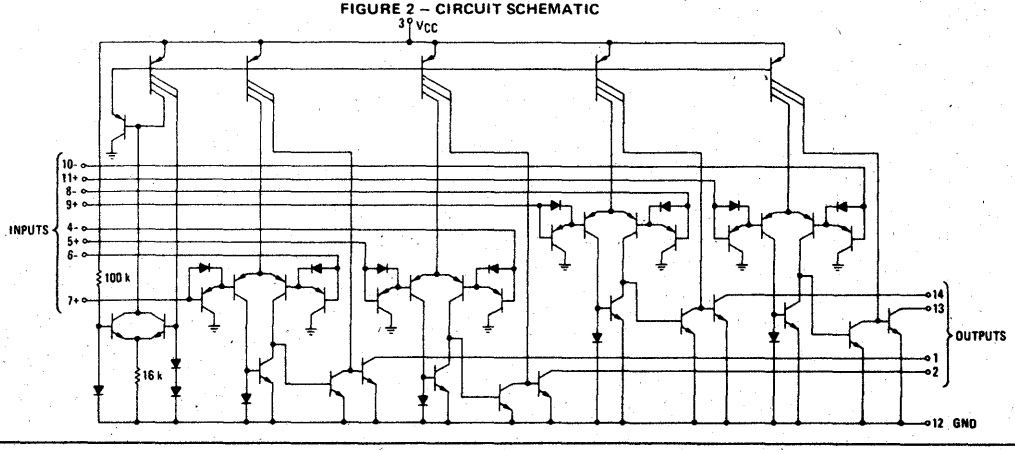


FIGURE 2 – CIRCUIT SCHEMATIC



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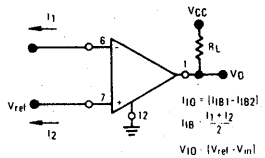
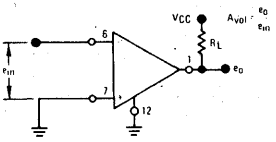
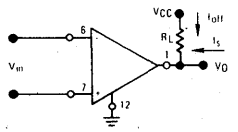
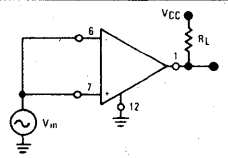
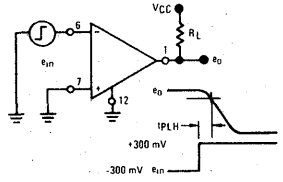
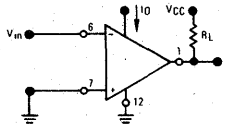
ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

Characteristic Definitions (1/4 Circuit Shown)	Characteristic	Symbol	Min	Typ	Max	Unit
	Input Offset Voltage (V_{ref} = 1.2 Vdc) (T_A = +25°C) (T_A = -40 to +85°C)	V_{IO}	– –	3.0 –	20 40	mVdc
	Input Offset Current	I_{IO}	–	3.0	–	nAdc
	Input Bias Current (T_A = +25°C) (T_A = -40 to +85°C)	I_{IB}	– –	30 –	500 1000	nAdc
	Voltage Gain (T_A = +25°C, R_L = 15 kΩ)	A_{vol}	2,000	30,000	–	V/V
	Transconductance	gm	–	2.0	–	mhos
	Input Differential Voltage Range	V_{IDR}	±V_{CC}	–	–	Vdc
	Output Leakage Current (Output Voltage High)	I_{OL}	–	–	1.0	μAdc
	Output Voltage - Low Logic State (I_s = 2.0 mA, V_{CC} = +5.0 to +28 Vdc)	V_{OL}	–	150	400	mVdc
	Output Sink Current (V_{CC} = +5.0 Vdc) (T_A = +25°C; V_{OL} = 400 mV) (T_A = -40 to +85°C, V_{OL} = 800 mV)	I_{sink}	– 2.0	6.0 –	– –	mAdc
	Input Common-Mode Voltage Range (V_{CC} = +28 Vdc)	V_{ICR}	0-26	–	–	Volts
	Common-Mode Rejection Ratio	CMRR	–	60	–	dB
	Propagation Delay Time For Positive and Negative-Going Input Pulse	$t_{PHL/LH}$	–	2.0	–	μs
	Slew Rate (R_L = 15 kΩ)	SR	– –	200 50	– –	V/μs
	Power Supply Current (Total of four comparators) (I_s = 0, V_{CC} = +5.0 to +28 Vdc)	I_{CC} I_{EE}	–	0.7	1.5	mAdc

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TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

FIGURE 3 – INPUT OFFSET VOLTAGE

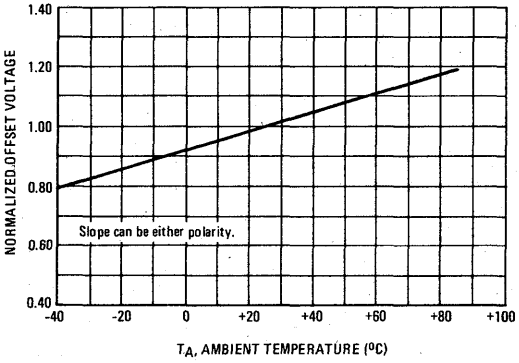


FIGURE 4 – OFFSET BIAS CURRENT

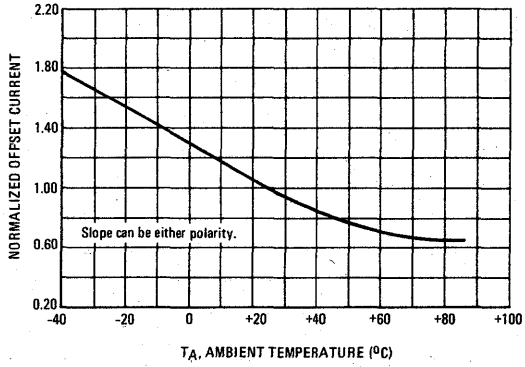
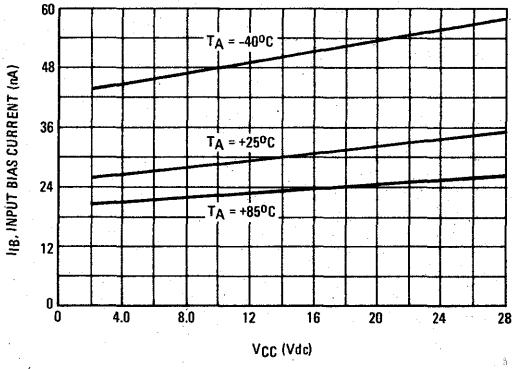


FIGURE 5 – INPUT BIAS CURRENT



TYPICAL APPLICATIONS

FIGURE 6 – FREE-RUNNING SQUARE-WAVE OSCILLATOR

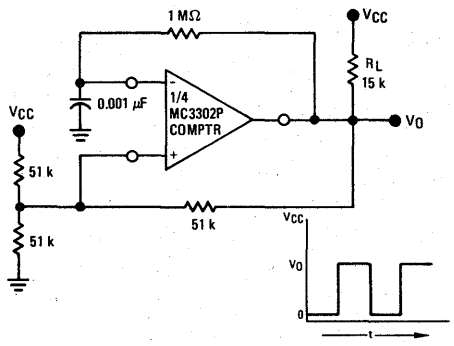
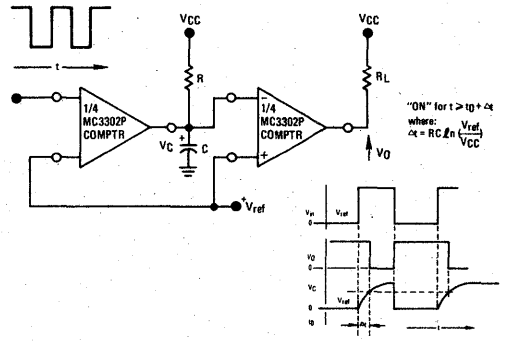
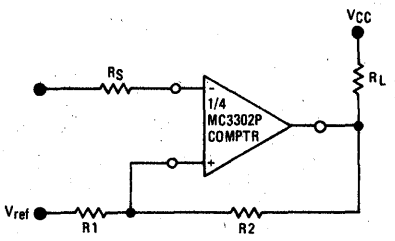


FIGURE 7 – TIME DELAY GENERATOR



TYPICAL APPLICATIONS (continued)

FIGURE 8 – COMPARATOR WITH HYSTERESIS

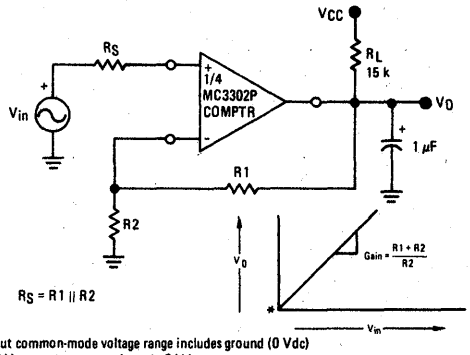


$R_S = R1 \parallel R2$

$$V_{th1} = V_{ref} + \frac{(V_{CC} - V_{ref})\,R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{ref} - \frac{(V_{ref} - V_O\ \text{Low})\,R1}{R1 + R2 + R_L}$$

FIGURE 9 – THE COMPARATOR AS AN OPERATIONAL AMPLIFIER



$R_S = R1 \parallel R2$

*Input common-mode voltage range includes ground (0 Vdc) and V_O can go to approximately 0 Vdc.

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XC3411

Product Preview

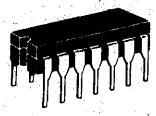
DUAL '111 TYPE COMPARATOR

The MC3411 single/split power supply comparators are dual versions of popular MLM111 series single comparators. These versatile devices feature low input currents and low offsets. Outputs can sink currents up to 50 mA.

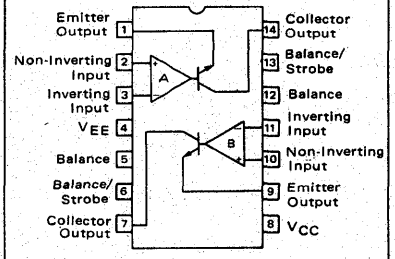
DUAL HIGH PERFORMANCE VOLTAGE COMPARATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

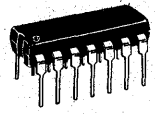
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



PIN CONNECTIONS



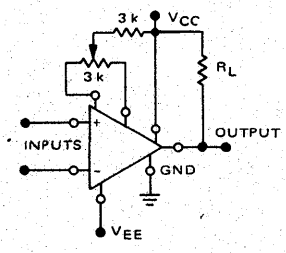
P SUFFIX
PLASTIC PACKAGE
CASE 646



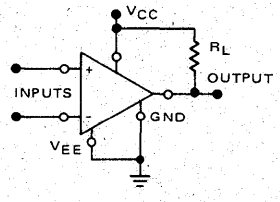
Pin compatible to LH2111 Series. (Move XC3511 back in socket to leave pins 1 and 16 open.)

SUGGESTED COMPARATOR DESIGN CONFIGURATIONS

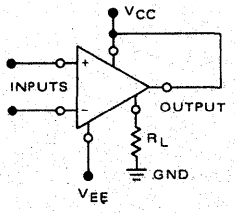
SPLIT POWER-SUPPLY with OFFSET BALANCE



SINGLE SUPPLY

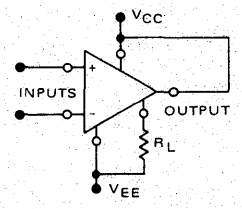


GROUND-REFERRED LOAD



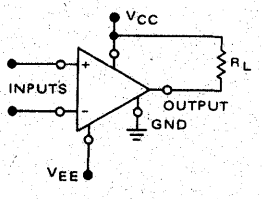
Input polarity is reversed when GND pin is used as an output.

LOAD REFERRED to NEGATIVE SUPPLY

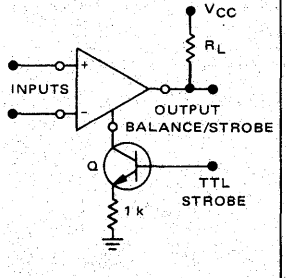


Input polarity is reversed when GND pin is used as an output.

LOAD REFERRED to POSITIVE SUPPLY



STROBE CAPABILITY



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Total Supply Voltage	V_{CC} + $\|V_{EE}\|$	36	Vdc
Output to Negative Supply Voltage	V_O - V_{EE}	40	Vdc
Ground to Negative Supply Voltage	V_{EE}	30	Vdc
Input Differential Voltage	V_{ID}	±30	Vdc
Input Voltage (1)	V_{in}	±15	Vdc
Power Dissipation Plastic and Ceramic Packages Derate above T_A = +25°C	P_D	 625 5.0	 mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (2) $R_S \leq 50$ kΩ, T_A = +25°C $R_S \leq 50$ kΩ, 0°C ≤ T_A ≤ 70°C	$\|V_{IO}\|$	 – –	 2.0 –	 7.5 10	mV
Input Offset Current (2) T_A = +25°C 0°C ≤ T_A ≤ 70°C	$\|I_{IO}\|$	 – –	 6.0 –	 50 70	nA
Input Bias Current T_A = +25°C 0°C ≤ T_A ≤ 70°C	I_{IB}	 – –	 100 –	 250 300	nA
Voltage Gain	A_V	–	200	–	V/mV
Response Time (3)	t_{TLH}	–	200	–	ns
Saturation Voltage T_A = +25°C, $V_{ID} \leq$ -10 mV, I_O = 50 mA 0°C, ≤ T_A ≤ 70°C, $V_{CC} \geq$ 4.5 V, V_{EE} = 0, $V_{ID} \leq$ -10 mV, $I_{sink} \leq$ 8.0 mA	V_{OL}	 – –	 0.75 0.23	 1.5 0.4	V
Strobe "On" Current	I_S	–	3.0	–	mA
Output Leakage Current T_A = +25°C, $V_{ID} \geq$ 10 mV, V_O = 35 V	I_{OL}	–	0.2	50	nA
Input Voltage Range 0°C ≤ T_A ≤ 70°C	V_{IR}	–	±14	–	V
Positive Supply Current	I_{CC}	–	7.0	10	mA
Negative Supply Current	I_{EE}	–	-5.0	-8.0	mA

Notes:
1. This rating applies for ±15-volt supplies. The positive input voltage limit is 30 volts above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 volts below the positive supply, whichever is less.
2. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0-mA load. Thus, these parameters define an error band and take into account the "worst-case" effects of voltage gain and input impedance.
3. The response time specified is for a 100-mV input step with 5.0-mV overdrive.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section
T_A = Maximum Desired Operating Ambient Temperature
$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

ORDERING INFORMATION

Device	Temperature Range	Package
MC3430L	0°C to +70°C	Ceramic DIP
MC3430P	0°C to +70°C	Plastic DIP
MC3431L	0°C to +70°C	Ceramic DIP
MC3431P	0°C to +70°C	Plastic DIP
MC3432L	0°C to +70°C	Ceramic DIP
MC3432P	0°C to +70°C	Plastic DIP
MC3433L	0°C to +70°C	Ceramic DIP
MC3433P	0°C to +70°C	Plastic DIP

MC3430 thru MC3433

QUAD HIGH-SPEED VOLTAGE COMPARATORS

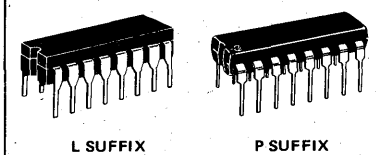
SILICON MONOLITHIC INTEGRATED CIRCUITS

QUAD DIFFERENTIAL VOLTAGE COMPARATOR/SENSE AMPLIFIERS

The MC3430 thru MC3433 high-speed comparators are ideal for application as sense amplifiers in MOS memory systems. They are specified in a unique way which combines the effects of input offset voltage, input offset current, voltage gain, temperature variations and input common-mode range into a single functional parameter. This parameter, called Input Sensitivity, specifies a minimum differential input voltage which will guarantee a given logic state. Four variations are offered in the comparator series.

The MC3430 and MC3431 versions feature a three-state strobe input common to all four channels which can be used to place the four outputs in a high-impedance state. These two devices use active-pull-up MTTL compatible outputs. The MC3432 and MC3433 are open-collector types which permit the implied AND connection. The MC3430 and MC3432 versions are specified for a ±7.0 mV input sensitivity over the 0 to 70°C temperature range, while the MC3431 and MC3433 are specified for ±12 mV.

- Propagation Delay Time – 40 ns
- Outputs Specified for a Fanout of 10 (MC7400 type loads)
- Specified for all conditions of ±5% Power Supply Variations, Operating Temperature Range, Input Common-Mode Voltage Swing from -3.0 V to 3.0 V, and $R_S \leq 200$ ohms.



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

CONNECTION DIAGRAM

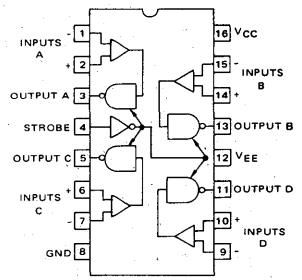
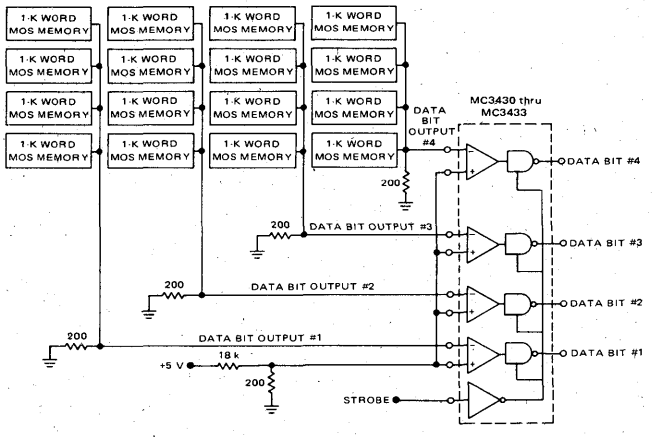


FIGURE 1 – A TYPICAL MOS MEMORY SENSING APPLICATION FOR A 4-K WORD BY 4-BIT MEMORY ARRANGEMENT EMPLOYING 1103 TYPE MEMORY DEVICES



Only four devices are required for a 4-k word by 16-bit memory system.

TRUTH TABLE
MC3430 and MC3432

Input	Strobe	Output	Device
$V_{ID} \geq 7.0$ mV, T_A = 0 to 70°C	L	H	MC3430
	H	Z	
	L	Off	MC3432
	H	Off	
-7.0 mV ≤ V_{ID} ≤ 7.0 mV, T_A = 0 to 70°C	L	I	MC3430
	H	Z	
	L	I	MC3432
	H	Off	
$V_{ID} \leq$ -7.0 mV, T_A = 0 to 70°C	L	L	MC3430
	H	Z	
	L	On	MC3432
	H	Off	

TRUTH TABLE
MC3431 and MC3433

Input	Strobe	Output	Device
$V_{ID} \geq 12$ mV, T_A = 0 to 70°C	L	H	MC3431
	H	Z	
	L	Off	MC3433
	H	Off	
-12 mV ≤ V_{ID} ≤ +12 mV, T_A = 0 to 70°C	L	I	MC3431
	H	Z	
	L	I	MC3433
	H	Off	
$V_{ID} \leq$ -12 mV, T_A = 0 to 70°C	L	L	MC3431
	H	Z	
	L	On	MC3433
	H	Off	

L = Low Logic State Z = Third (High Impedance)
H = High Logic State I = Indeterminate State
RS ≤ 200 Ω

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MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±7.0	Vdc
Differential Mode Input Signal Voltage Range	V_{IDR}	±6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Output Voltage (MC3432 — 33 versions)	V_O	+7.0	Vdc
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Vdc
Output Load Current	I_{OL}	–	–	16	mA
Differential-Mode Input Voltage Range	V_{IDR}	-5.0	–	+5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	-3.0	–	+3.0	Vdc
Input Voltage Range (any input to Ground)	V_{IR}	-5.0	–	+3.0	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = 0°C to +70°C unless otherwise noted.)
Typical Values are Measured at T_A = 25°C

Characteristic	Symbol	MC3430, MC3431 Min	MC3430, MC3431 Typ	MC3430, MC3431 Max	MC3432, MC3433 Min	MC3432, MC3433 Typ	MC3432, MC3433 Max	Unit
Input Sensitivity (See Discussion on Page 3) ($R_S \leq 200$ Ohms)	V_{IS}							mV
(Common Mode Voltage Range = -3.0 V ≤ V_{in} ≤ 3.0 V) 4.75 ≤ V_{CC} ≤ 5.25 V, -4.75 ≥ V_{EE} ≥ -5.25 V, T_A = 25°C								
MC3430, MC3432		–	–	±6.0	–	–	±6.0	
MC3431, MC3433		–	–	±10	–	–	±10	
(Common Mode Voltage Range = -3.0 V ≤ V_{in} ≤ 3.0 V) 4.75 ≤ V_{CC} ≤ 5.25 V, -4.75 ≥ V_{EE} ≥ -5.25 V, T_A = 0 to 70°C								
MC3430, MC3432		–	–	±7.0	–	–	±7.0	
MC3431, MC3433		–	–	±12	–	–	±12	
Input Offset Voltage ($R_S \leq 200$ Ohms)	V_{IO}	–	2.0	–	–	2.0	–	mV
Input Bias Current (V_{CC} = 5.25 V, V_{EE} = -5.25 V)	I_{IB}							µA
MC3430, MC3432		–	–	20	–	–	20	
MC3431, MC3433		–	–	20	–	–	20	
Input Offset Current	I_{IO}	–	1.0	–	–	1.0	–	µA
Voltage Gain	A_{vol}	–	1200	–	–	1200	–	V/V
Strobe Input Voltage (Low State)	$V_{IL(S)}$	–	–	0.8	–	–	0.8	V
Strobe Input Voltage (High State)	$V_{IH(S)}$	2.0	–	–	2.0	–	–	V
Strobe Current (Low State) (V_{CC} = 5.25 V, V_{EE} = -5.25 V, V_{in} = 0.4 V)	$I_{IL(S)}$	–	–	-1.6	–	–	-1.6	mA
Strobe Current (High State)	$I_{IH(S)}$							
(V_{CC} = 5.25 V, V_{EE} = -5.25 V, V_{in} = 2.4 V)		–	–	40	–	–	40	µA
(V_{CC} = 5.25 V, V_{EE} = -5.25 V, V_{in} = 5.25 V)		–	–	1.0	–	–	1.0	mA
Output Voltage (High State) (I_O = -400 µA, V_{CC} = 4.75 V, V_{EE} = -4.75 V)	V_{OH}	2.4	–	–	–	–	–	V
Output Voltage (Low State) (I_O = 16 mA, V_{CC} = 4.75 V, V_{EE} = 4.75 V)	V_{OL}	–	–	0.4	–	–	0.4	V
Output Leakage Current (V_{CC} = 4.75 V, V_{EE} = -4.75 V, V_O = 5.25 V)	I_{CEX}	–	–	–	–	–	250	µA
Output Current Short Circuit (V_{CC} = 5.25 V, V_{EE} = -5.25 V)	I_{os}	-18	–	-70	–	–	–	mA
Output Disable Leakage Current (V_{CC} = 5.25 V, V_{EE} = -5.25 V)	I_{off}	–	–	40	–	–	–	µA
High Logic Level Supply Currents (V_{CC} = 5.25 V, V_{EE} = -5.25 V)	I_{CC} I_{EE}	– –	45 -17	60 -30	– –	45 -17	60 -30	mA mA

A UNIQUE FUNCTIONAL PARAMETER FOR COMPARATORS

A unique approach is used in specifying the MC3430-33 quad comparators. Previously, comparators have been specified as linear devices with common operational amplifier type parameters such as voltage gain (A_{VOL}), input offset voltage (V_{IO}), input offset current (I_{IO}) and common-mode rejection ratio (CMRR). This is true despite the fact that most comparators are seldom operated in their linear region because it is difficult to hold a high gain comparator in this narrow region. Comparators are normally used to "detect" when an unknown voltage level exceeds a given reference voltage.

The most desirable comparator parameter is what minimum differential input voltage is required at the comparator's input terminals to guarantee a given output logic state. This new and important parameter has been called input sensitivity (V_{IS}) and is analagous to the input threshold voltage specification on a core memory sense amplifier. The input sensitivity specification includes the effects of voltage gain, input offset voltage and input offset current and eliminates the need for specifying these three parameters.

In order to make this parameter as inclusive as possible on the MC3430-33 series quad comparators, the input sensitivity is specified within the following conditions:

Commercial Temperature Range — 0 to 70°C
Power Supply Variations — ±5% (all conditions)
Input Source Resistance — ≤200 Ohms
Common-Mode Voltage Range — -3.0 V to +3.0 V

Note: Typical values have been included on the omitted parameters for applications where the offset voltages are externally nulled.

Voltage gain is defined as the ratio of the resulting ΔV_O to a change in the V_{IDR} using conditions at which the V_{IO} and I_{IO} are nulled. Thus, for worst case MTTL logic levels, the required output voltage change is 2.0 V (V_{OH}min − V_{OL}max = 2.4 V − 0.4 V). If 2.0 mV are required at the input terminals to induce this change in logic state, the voltage gain would be 1000 V/V.

Gain however is not the only factor affecting the logic transition. Normally input offset voltages, that are not externally nulled, can add an appreciable error that drastically overshadows the comparator gain. Therefore, the 2.0 mV for example, required to cause the logic transition is often masked. An input offset voltage of up to 7.5 mV might be required to reach the linear region. A further consideration is the input offset current of up to ±10 μA flowing through the matched 200-Ohm source resistors at the input terminals which can create an additional error of ±2.0 mV. In order to determine a worst case input sensitivity, it must be assumed that minimum specified gain and maximum specified offset voltage and current conditions exist. Also it must be assumed that these three factors are cumulative, requiring a worst case input of:

Logic Transition = 2.0 mV
V_{IO} = 7.5 mV
I_{IO} of ±10 μA thru 200-Ohm resistor = 2.0 mV

Therefore, 2 + 7.5 + 2 = 11.5 mV.

The effects of power supply voltage variations, temperature changes and common-mode input voltage conditions have not been considered, as they are not present in the gain and offset specifications on most comparators.

Thus, the input sensitivity specification greatly reduces the effort required in determining the worst case differential voltage required by a given comparator type.

Table I compares the worst case input sensitivity of three popular comparator types at both room temperature and over the specified commercial temperature range (0 to 70°C). This sensitivity was computed from the specified voltage gain, offset voltage and offset current limits.

TABLE I — WORST CASE COMPARISONS

	T_A = 25°C						T_A = 0 to 70°C					
Type Number	V_{IO} mV Max	A_{vol}* V/V Typ	Differential Input Voltage Required for 3.0 V Output Change	I_{IO} R_S = 200 Ω μA Max	Error Voltage Generated Into 200 Ω Source Resistors	Total Sensitivity mV	V_{IO} mV Max	A_{vol}* V/V Typ	Differential Input Voltage Required for 3.0 V Output Change	I_{IO} R_S = 200 Ω μA Max	Error Voltage Generated Into 200 Ω Source Resistors	Total Sensitivity mV
MC3430, MC3432	—	—	—	—	—	6.0	—	—	—	—	—	7.0
MC3431, MC3433	—	—	—	—	—	10	—	—	—	—	—	12
MC1711C	5.0	1500	2.0 mV	15	3.0 mV	10	5.0	1000	3.0 mV	25	5.0 mV	13
MLM311	7.5	200 k	0.015 mV	6.0**	0.0012 mV	7.516	10	100 k	0.030 mV	70**	0.014 mV	10.04

*Typical values given, as minimum gain not always specified.
**I_{IO} measured in nA

FIGURE 2 — GUARANTEED OUTPUT STATE versus DIFFERENTIAL INPUT VOLTAGE

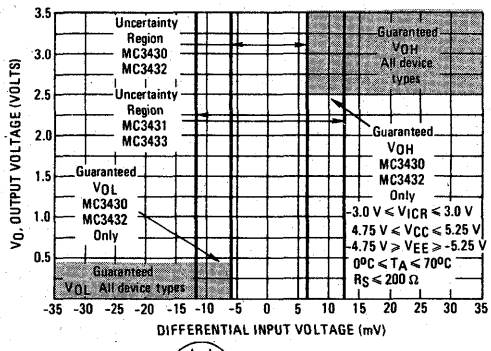
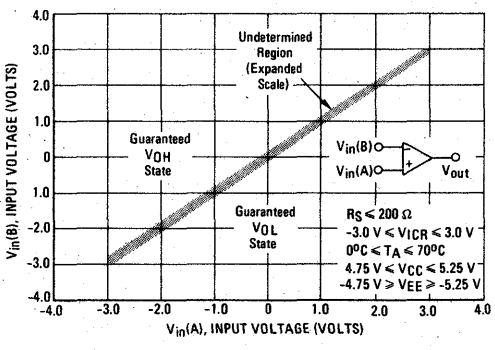


FIGURE 3 — GUARANTEED OUTPUT STATE versus INPUT VOLTAGE

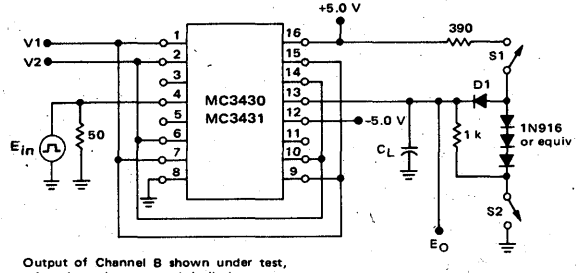


SWITCHING CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Fig.	MC3430, MC3431			MC3432, MC3433			Unit
			Min	Typ	Max	Min	Typ	Max	
High to Low Logic Level Propagation Delay Time (Differential Inputs) 5.0 mV + V_{IS}	$t_{PHL(D)}$	6,8-11	–	20	45	–	27	50	ns
Low to High Logic Level Propagation Delay Time (Differential Inputs) 5.0 mV + V_{IS}	$t_{PLH(D)}$	6,8-11	–	33	55	–	40	65	ns
Open State to High Logic Level Propagation Delay Time (Strobe)	$t_{PZH(S)}$	4	–	–	35	–	–	–	ns
High Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PHZ(S)}$	4	–	–	35	–	–	–	ns
Open State to Low Logic Level Propagation Delay Time (Strobe)	$t_{PZL(S)}$	4	–	–	40	–	–	–	ns
Low Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PLZ(S)}$	4	–	–	35	–	–	–	ns
High Logic to Low Logic Level Propagation Delay Time (Strobe)	$t_{PHL(S)}$	5	–	–	–	–	–	40	ns
Low Logic to High Logic Level Propagation Delay Time (Strobe)	$t_{PLH(S)}$	5	–	–	–	–	–	35	ns

TEST CIRCUITS

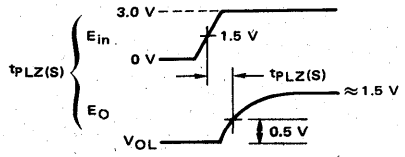
FIGURE 4 – STROBE PROPAGATION DELAY TIMES $t_{PLZ(S)}$, $t_{PZL(S)}$, $t_{PHZ(S)}$, and $t_{PZH(S)}$

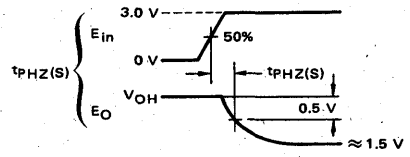


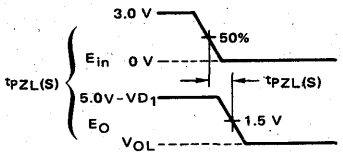
Output of Channel B shown under test, other channels are tested similarly.

	V1	V2	S1	S2	C_L
$t_{PLZ(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{PZL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHZ(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{PZH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{in} waveform characteristics:
t_{TLH} and t_{THL} ≤ 10 ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%







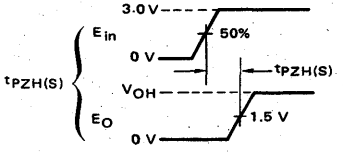
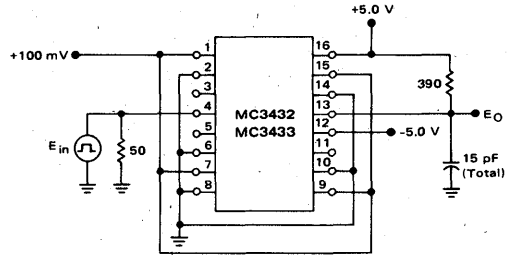
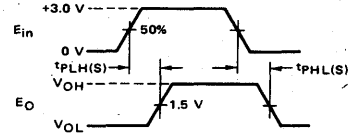


FIGURE 5 – STROBE PROPAGATION DELAY $t_{PLH(S)}$ AND $t_{PHL(S)}$

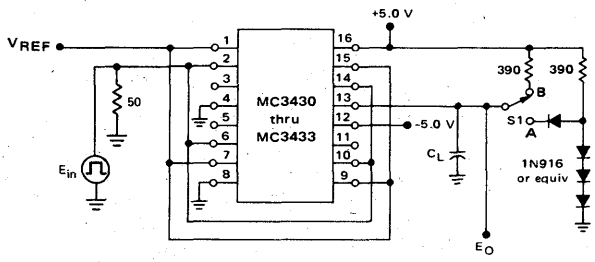


Output of Channel B shown under test, other channels are tested similarly.



E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

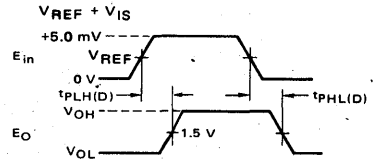
FIGURE 6 – DIFFERENTIAL INPUT PROPAGATION DELAY $t_{PLH(D)}$ AND $t_{PHL(D)}$



Output of Channel B shown under test, other channels are tested similarly.

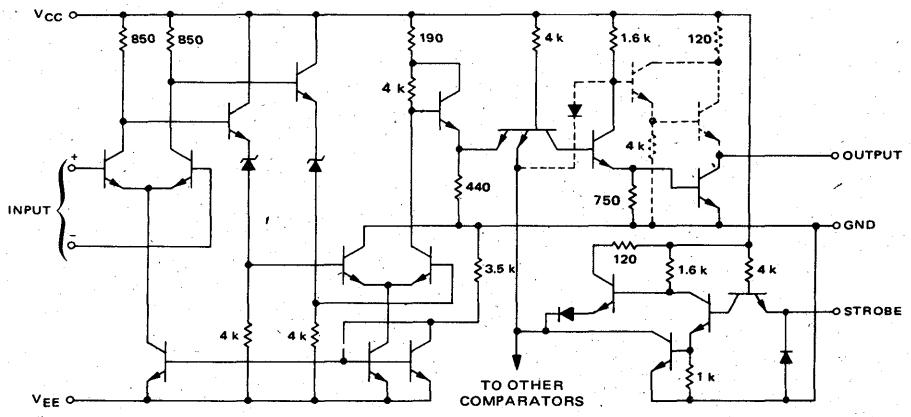
S1 at "A" for MC3430, MC3431
S1 at "B" for MC3432, MC3433
C_L = 50 pF total for MC3430, MC3431
C_L = 15 pF total for MC3432, MC3433

Device	V_{REF} mV
MC3430	11
MC3431	15
MC3432	11
MC3433	15



E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

FIGURE 7 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



Dashed components apply to the MC3430 and MC3431 circuits only.

TYPICAL PERFORMANCE CURVES

RESPONSE TIME versus OVERDRIVE – MC3430, MC3431

FIGURE 8 – OUTPUT LOW TO HIGH

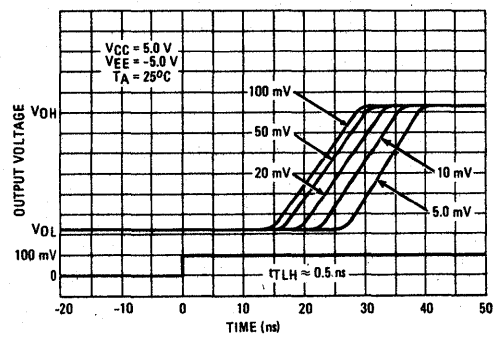
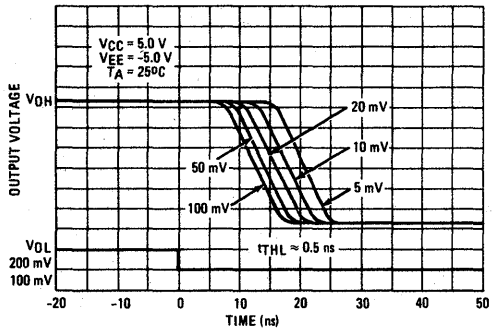


FIGURE 9 – OUTPUT HIGH TO LOW



RESPONSE TIME versus OVERDRIVE – MC3432, MC3433

FIGURE 10 – OUTPUT LOW TO HIGH

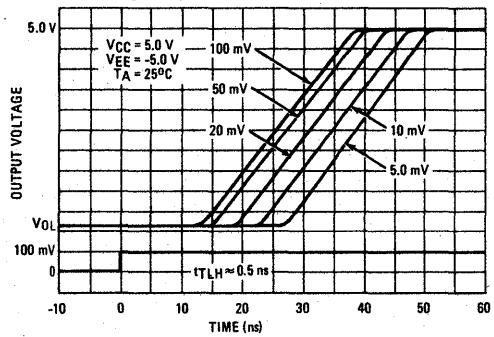


FIGURE 11 – OUTPUT HIGH TO LOW

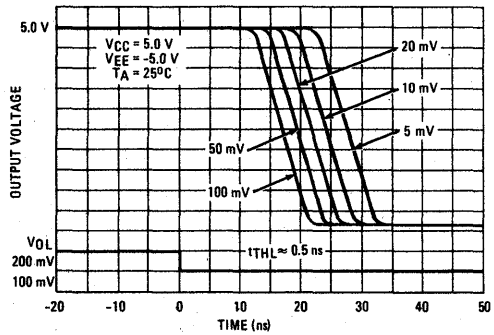


FIGURE 12 – AVERAGE INPUT OFFSET VOLTAGE versus TEMPERATURE

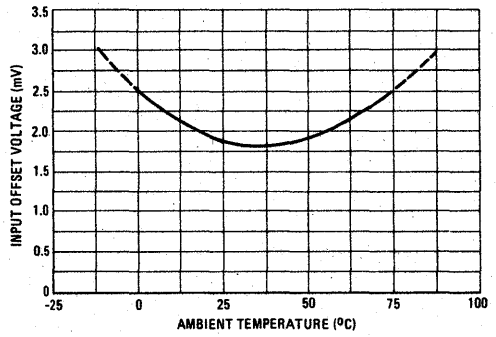
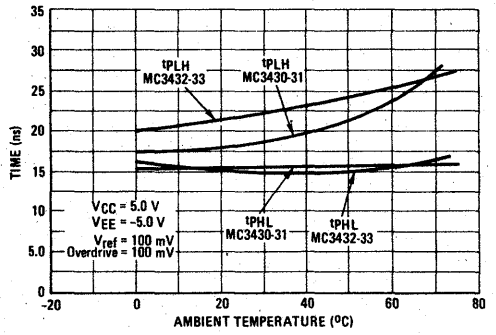


FIGURE 13 – RESPONSE TIME versus TEMPERATURE



6

APPLICATIONS INFORMATION

FIGURE 14 – 4-BIT PARALLEL A/D CONVERTER

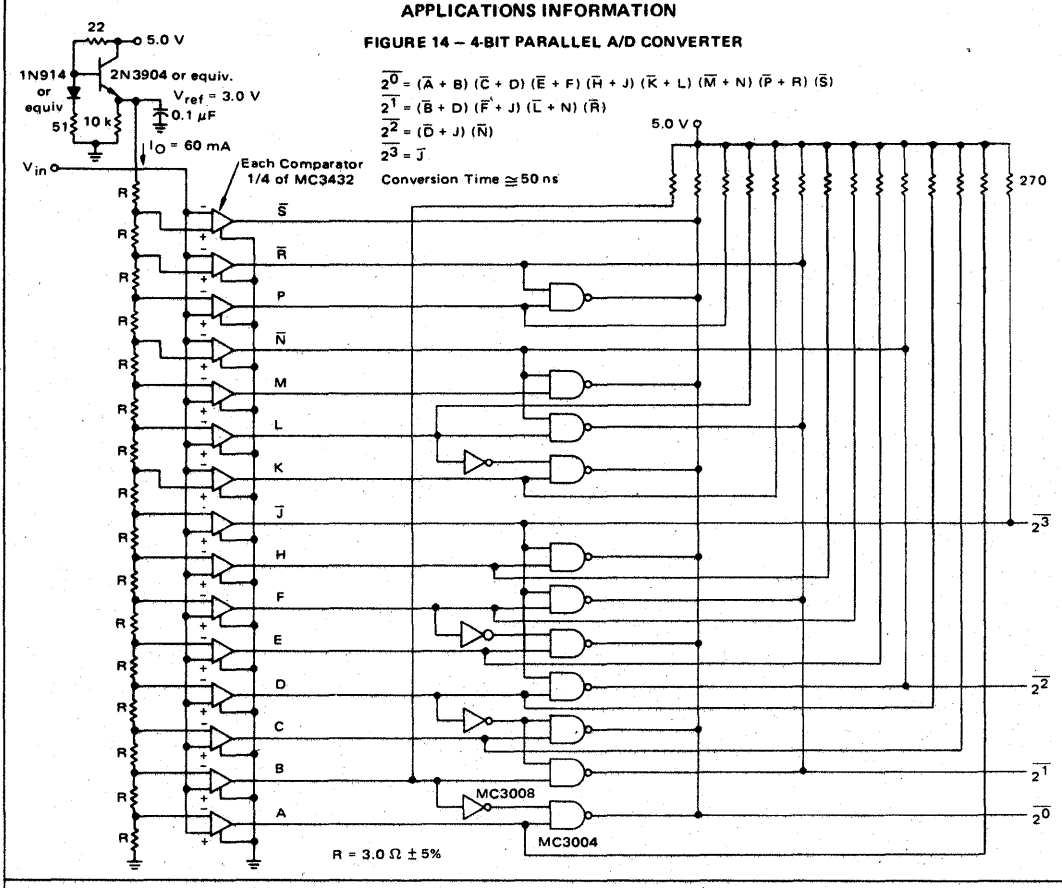


FIGURE 15 – LEVEL DETECTOR WITH HYSTERESIS

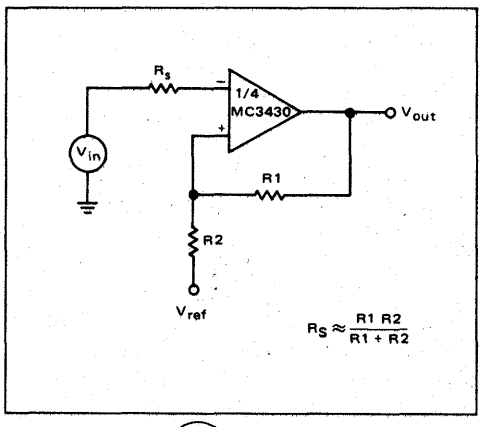
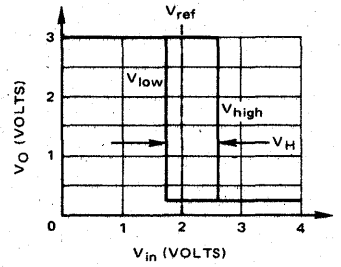


FIGURE 16 – TRANSFER CHARACTERISTICS AND EQUATIONS FOR FIGURE 15



$$V_{high} = V_{ref} + \frac{R2\ [V_{O(max)} - V_{REF}]}{R1 + R2}$$

$$V_{low} = V_{ref} + \frac{R2\ [V_{O(min)} - V_{REF}]}{R1 + R2}$$

Hysteresis Loop (V_h)

$$V_h = V_{high} - V_{low} = \frac{R2}{R1 + R2}\ [V_{O(max)} - V_{O(min)}]$$

FIGURE 17 – DOUBLE ENDED LIMIT DETECTOR

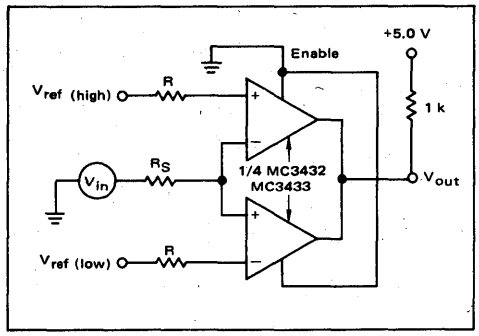
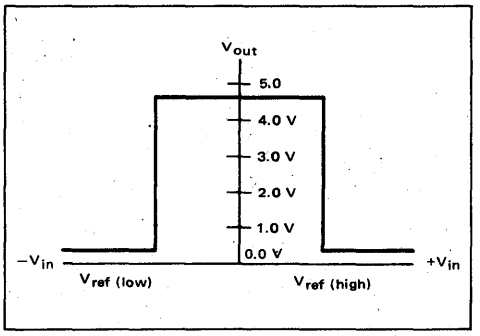


FIGURE 18 – VOLTAGE TRANSFER FUNCTION



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MLM311G	LM311H	0°C to +70°C	Metal Can
MLM311P1	LM311N	0°C to +70°C	Plastic DIP
MLM311L,U	—	0°C to +70°C	Ceramic DIP
MLM311F	—	0°C to +70°C	Ceramic Flat
MLM211G	—	−25°C to +85°C	Metal Can
MLM211L,U	—	−25°C to +85°C	Ceramic DIP
MLM211F	—	−25°C to +85°C	Ceramic Flat
MLM111G	—	−55°C to +125°C	Metal Can
MLM111L,U	—	−55°C to +125°C	Ceramic DIP
MLM111F	—	−55°C to +125°C	Ceramic Flat

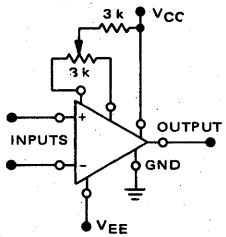
MLM111
MLM211
MLM311

HIGHLY FLEXIBLE VOLTAGE COMPARATORS

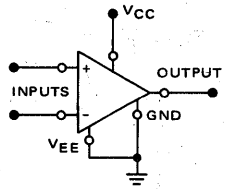
The ability to operate from a single power supply of 5.0 to 30 volts or ±15-volt split supplies, as commonly used with operational amplifiers, makes the MLM111/MLM211/MLM311 a truly versatile comparator. Moreover, the inputs of the device can be isolated from system ground while the output can drive loads referenced either to ground, the V_{CC} or the V_{EE} supply. This flexibility makes it possible to drive MDTL, MRTL, MTTL, or MOS logic. The output can also switch voltages to 50 volts at currents to 50 mA. Thus the MLM111/MLM211/MLM311 can be used to drive relays, lamps or solenoids.

SUGGESTED COMPARATOR DESIGN CONFIGURATIONS

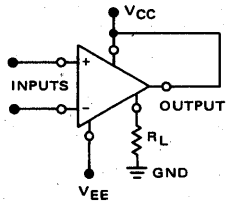
SPLIT POWER-SUPPLY with OFFSET BALANCE



SINGLE SUPPLY

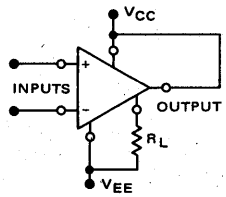


GROUND-REFERRED LOAD



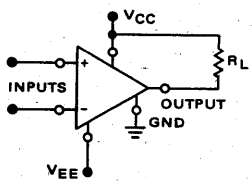
Input polarity is reversed when GND pin is used as an output.

LOAD REFERRED to NEGATIVE SUPPLY

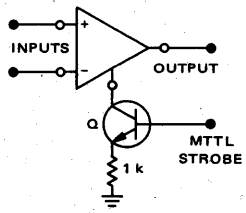


Input polarity is reversed when GND pin is used as an output.

LOAD REFERRED to POSITIVE SUPPLY



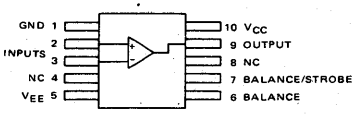
STROBE CAPABILITY



HIGH PERFORMANCE VOLTAGE COMPARATORS

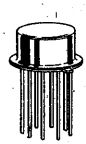
SILICON MONOLITHIC INTEGRATED CIRCUIT

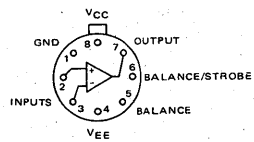
F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91



(Top View)

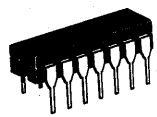
G SUFFIX
METAL PACKAGE
CASE 601

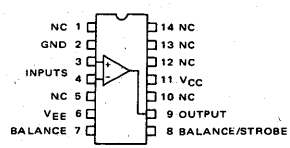




(Top View)

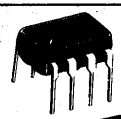
L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



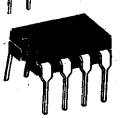


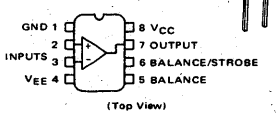
(Top View)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MLM311 Only)



U SUFFIX
CERAMIC PACKAGE
CASE 693





(Top View)

6

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value		Unit
		MLM111 MLM211	MLM311	
Total Supply Voltage	$V_{CC} + \lvert V_{EE}\rvert$	36	36	Vdc
Output to Negative Supply Voltage	$V_O - V_{EE}$	50	40	Vdc
Ground to Negative Supply Voltage	V_{EE}	30	30	Vdc
Differential Input Voltage	V_{ID}	±30	±30	Vdc
Input Voltage (See Note 1)	V_{in}	±15	±15	Vdc
Power Dissipation (Pkg. Limitation)	P_D			
Metal Package		680		mW
Derate above T_A = +25°C		4.6		mW/°C
Flat Package		500		mW
Derate above T_A = +25°C		3.3		mW/°C
Plastic* and Ceramic Dual In-Line Packages		625		mW
Derate above T_A = +25°C		5.0		mW/°C
Operating Temperatures Range	T_A			°C
MLM111		-55 to +125	–	
MLM211		-25 to +85	–	
MLM311		–	0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

*MLM311P1 only is available in the plastic dual in-line package.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	MLM111 MLM211			MLM311			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (See Note 2.)	$\lvert V_{IO}\rvert$							mV
$R_S \leq 50\ k\Omega$, T_A = +25°C		–	0.7	3.0	–	2.0	7.5	
$R_S \leq 50\ k\Omega$, $T_{low}^* \leq T_A \leq T_{high}^*$		–	–	4.0	–	–	10	
Input Offset Current (See Note 2.)	$\lvert I_{IO}\rvert$							nA
T_A = +25°C		–	4.0	10	–	6.0	50	
$T_{low} \leq T_A \leq T_{high}$		–	–	20	–	–	70	
Input Bias Current	I_{IB}							nA
T_A = +25°C		–	60	100	–	100	250	
$T_{low} \leq T_A \leq T_{high}$		–	–	150	–	–	300	
Voltage Gain	A_V	–	200	–	–	200	–	V/mV
Response Time (See Note 3.)	t_{TLH}	–	200	–	–	200	–	ns
Saturation Voltage	V_{OL}							V
T_A = +25°C, $V_{ID} \leq -5.0$ mV, I_O = 50 mA		–	0.75	1.5	–	–	–	
$V_{ID} \leq -10$ mV, I_O = 50 mA		–	–	–	–	0.75	1.5	
$T_{low} \leq T_A \leq T_{high}$, $V_{CC} \geq 4.5$ V, V_{EE} = 0								
$V_{ID} \leq -6.0$ mV, $I_{sink} \leq 8.0$ mA		–	0.23	0.4	–	–	–	
$V_{ID} \leq -10$ mV, $I_{sink} \leq 8.0$ mA		–	–	–	–	0.23	0.4	
Strobe "On" Current	I_S	–	3.0	–	–	3.0	–	mA
Output Leakage Current	I_{OL}							
T_A = +25°C, $V_{ID} \geq 5.0$ mV, V_O = 35 V		–	0.2	10	–	–	–	nA
$V_{ID} \geq 10$ mV, V_O = 35 V		–	–	–	–	0.2	50	nA
$T_{low} \leq T_A \leq T_{high}$, $V_{ID} \geq 5.0$ mV, V_O = 35 V		–	0.1	0.5	–	–	–	μA
Input Voltage Range	V_{IR}							V
$T_{low} \leq T_A \leq T_{high}$		–	±14	–	–	±14	–	
Positive Supply Current	I_{CC}	–	+5.1	+6.0	–	+5.1	+7.5	mA
Negative Supply Current	I_{EE}	–	-4.1	-5.0	–	-4.1	-5.0	mA

*T_{low} = -55°C for MLM111 = -25°C for MLM211 = 0 for MLM311

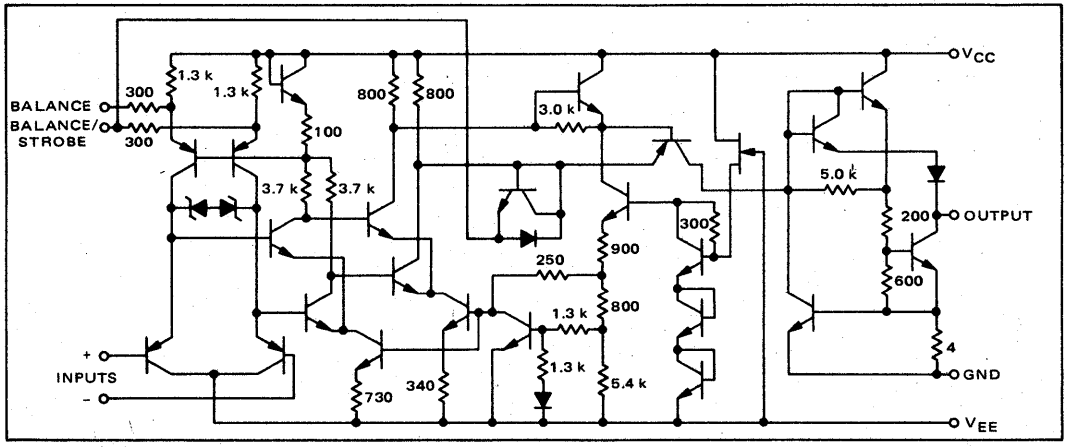
T_{high} = +125°C for MLM111 = +85°C for MLM211 = +70°C for MLM311

Note 1. This rating applies for ±15-volt supplies. The positive input voltage limit is 30 volts above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 volts below the positive supply, whichever is less.

Note 2. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0-mA load. Thus, these parameters define an error band and take into account the "worst case" effects of voltage gain and input impedance.

Note 3. The response time specified is for a 100-mV input step with 5.0-mV overdrive.

FIGURE 1 – CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

FIGURE 2 – INPUT BIAS CURRENT and INPUT OFFSET CURRENT versus TEMPERATURE

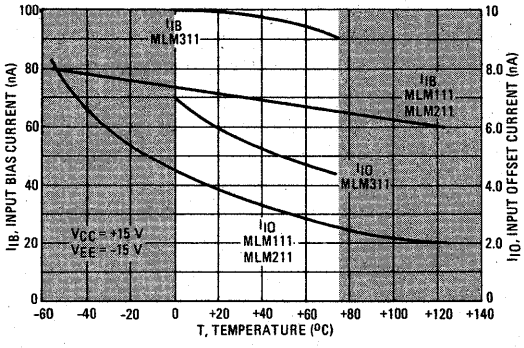


FIGURE 3 – COMMON-MODE LIMITS versus TEMPERATURE

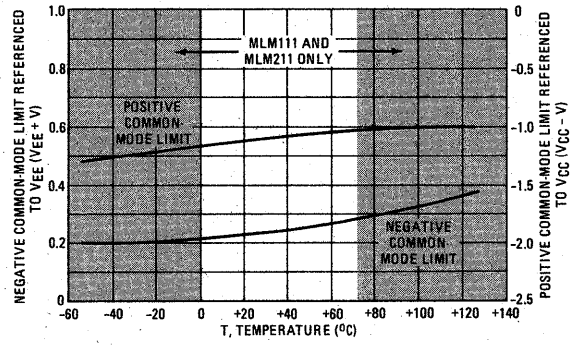


FIGURE 4 – OUTPUT SATURATION VOLTAGE versus OUTPUT CURRENT

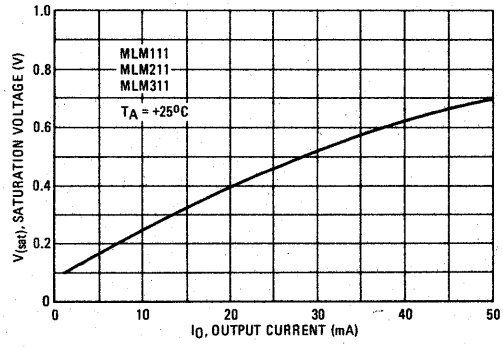
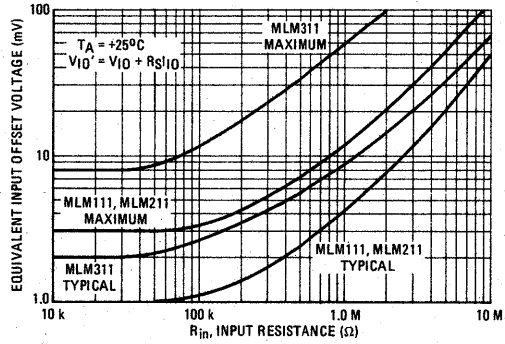


FIGURE 5 – EQUIVALENT OFFSET ERROR versus INPUT RESISTANCE



6

APPLICATIONS INFORMATION

FIGURE 6 – ZERO-CROSSING DETECTOR DRIVING MOS LOGIC

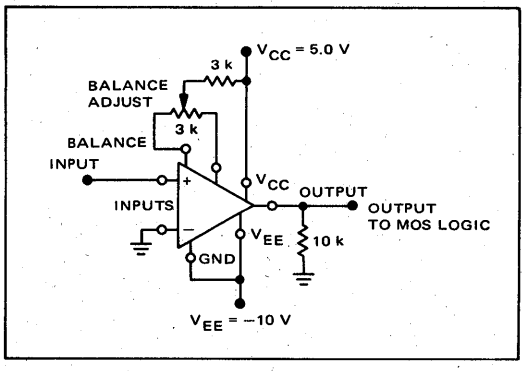
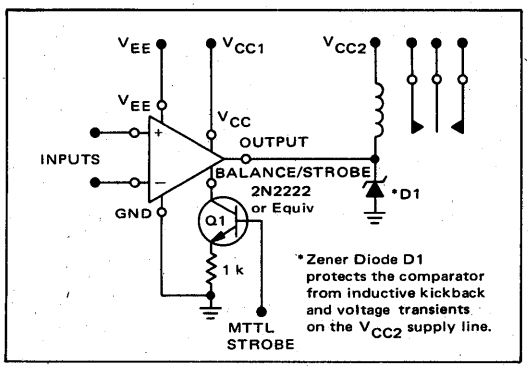


FIGURE 7 – RELAY DRIVER WITH STROBE CAPABILITY



6

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MLM139L	—	−55°C to +125°C	Ceramic DIP
MLM239L	—	−40°C to +85°C	Ceramic DIP
MLM239P	—	−40°C to +85°C	Plastic DIP
MLM339L	—	0°C to +70°C	Ceramic DIP
MLM339P	LM339N	0°C to +70°C	Plastic DIP

MLM139
MLM239
MLM339

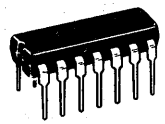
QUAD SINGLE-SUPPLY COMPARATORS

These comparators are designed for use in level detection, low-level sensing and memory applications in Consumer Automotive and Industrial electronic applications.

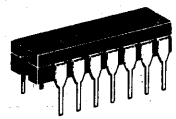
- Power Supply Options —
  Single Supply = 2.0 to 36 Vdc
  Split Supplies = ±1.0 −±18 Vdc
- Wide Operating Temperature Range — −55 to +125°C
- Low Supply Current Drain — 2.0 mA (Max)
- Low Input Biasing Current — 25 nA (Typ)
- Low Input Offset Voltage — 5.0 mV (Max)
- TTL and CMOS Compatible

QUAD COMPARATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646
(MLM239 and MLM339 only)



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +36	Vdc
Output Sink Current	I_{sink}	20	mA
Power Dissipation @ T_A = 25°C	P_D		
Ceramic Package		1.25	Watts
Derate above 25°C		10	mW/°C
Plastic Package		1.25	Watts
Derate above 25°C		10	mW/°C
Operating Ambient Temperature Range	T_A		°C
MLM139		-55 to +125	
MLM239		-40 to +85	
MLM339		0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN CONNECTIONS

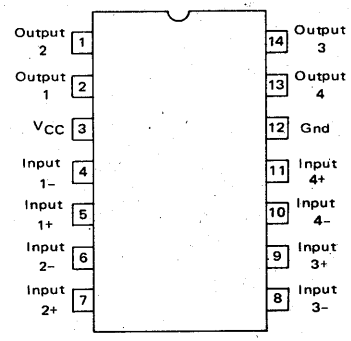
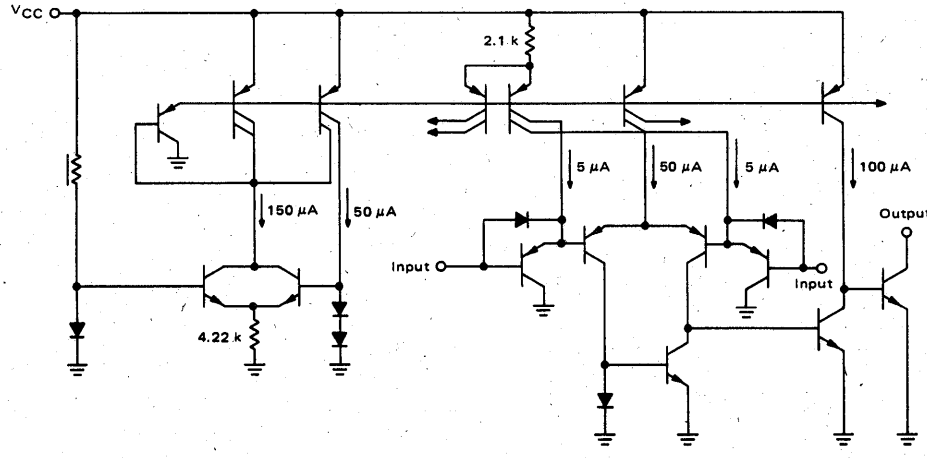


FIGURE 1 — CIRCUIT SCHEMATIC (Diagram shown is for 1 comparator)



ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = 25°C unless otherwise noted.)

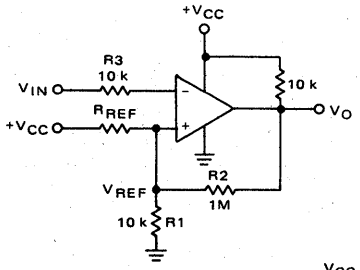
Characteristic	Symbol	MLM139			MLM239			MLM339			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_{ref} = 1.4 Vdc, V_O = 1.4 Vdc, R_S = 0)	V_{IO}	–	±2.0	±5.0	–	±2.0	±5.0	–	±2.0	±5.0	mVdc
Input Offset Current	I_{IO}	–	±3.0	±25	–	±5.0	±50	–	±5.0	±50	nA
Input Bias Current	I_{IB}	–	25	100	–	25	250	–	25	250	nA
Input Common Mode Voltage Range (Note 1)	V_{ICR}	0	–	V_{CC} -1.5	0	–	V_{CC} -1.5	0	–	V_{CC} -1.5	V
Supply Current (R_L = ∞)	I_{CC} I_{EE}	–	0.8	2.0	–	0.8	2.0	–	0.8	2.0	mA
Response Time (Note 2) (V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ)	–	–	1.3	–	–	1.3	–	–	1.3	–	μs
Output Sink Current ($V_{I(-)}$ ≥ +1.0 Vdc, $V_{I(+)}$ = 0, V_O ≤ +1.5 Vdc) ($V_{I(-)}$ ≥ +1.0 Vdc, $V_{I(+)}$ = 0, V_O ≤ 500 mVdc)	I_{sink}	6.0 6.0	16 –	– –	6.0 6.0	16 –	– –	6.0 6.0	16 –	– –	mA
Saturation Voltage ($V_{I(-)}$ ≥ +1.0 Vdc, $V_{I(+)}$ = 0, I_{sink} ≤ 4.0 mAdc) ($V_{I(-)}$ ≥ +1.0 Vdc, $V_{I(+)}$ = 0, I_{sink} ≤ 6.0 mAdc)	V_{sat}	– –	– –	500 500	– –	– –	500 500	– –	– –	500 500	mV
Voltage Gain (V_{CC} = 15 V) (R_L ≥15 kΩ)	A_V	–	200	–	–	200	–	–	200	–	k
Output Leakage Current ($V_{I(+)}$ ≥ +1.0 Vdc, $V_{I(-)}$ = 0, V_O = 5.0 Vdc)	I_{OL}	–	0.1	–	–	0.1	–	–	0.1	–	μA

PERFORMANCE CHARACTERISTICS – Guaranteed Over Temperature Range (V_{CC} = +5.0 Vdc)

Characteristic	Symbol	-55 to +125°C			-40°C to +85°C			0° to 70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_{ref} = +1.4 Vdc, V_O = 1.4 Vdc, R_S = 0)	V_{IO}	–	–	± 9.0	–	–	± 9.0	–	–	± 9.0	mV
Input Offset Current	I_{IO}	–	–	±100	–	–	±150	–	–	±150	nA
Input Bias Current	I_{IB}	–	–	300	–	–	400	–	–	400	nA
Input Common Mode Voltage Range	V_{ICR}	0	–	V_{CC} -2.0	0	–	V_{CC} -2.0	0	–	V_{CC} -2.0	Vdc
Saturation Voltage ($V_{I(-)}$ ≥ 1.0 Vdc, $V_{I(+)}$ = 0, I_{sink} ≤ 4.0 mAdc)	V_{sat}	–	–	700	–	–	700	–	–	700	mV
Output Leakage Current ($V_{I(+)}$ ≥ 1.0 Vdc, $V_{I(-)}$ = 0, V_O = 30 Vdc)	I_{OL}	–	–	1.0	–	–	1.0	–	–	1.0	μA
Input Differential Voltage (All V_I ≥ 0 Vdc)	V_{ID}	–	–	36	–	–	36	–	–	36	Vdc

Notes 1. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 300 mV. The upper end of the common-mode voltage range is V_{CC} -1.5 V, but either or both inputs can go to +30 Vdc without damage.
2. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger signals, 300 ns is typical.

FIGURE 2 – INVERTING COMPARATOR WITH HYSTERESIS

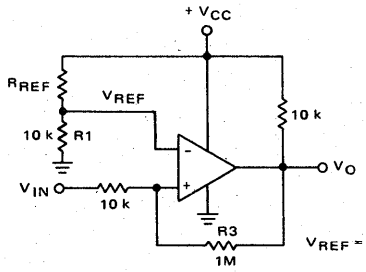


$$V_{REF} \approx \frac{V_{CC}\,R1}{R_{REF} + R1}$$

$$R3 \simeq R1 \,//\, R_{REF} \,//\, R1$$

$$V_H = \frac{R1 // R_{REF}}{R1 // R_{REF} + R2} \quad (V_{Omax} - V_{Omin})$$

FIGURE 3 – NON-INVERTING COMPARATOR WITH HYSTERESIS



$$V_{REF} = \frac{V_{CC}\,R1}{R_{REF} + R1}$$

$$R2 \approx R1 // R_{REF}$$

Amount of Hysteresis V_M

$$V_H = \frac{R2}{R2 + R3} \quad (V_{Omax} - V_{Omin})$$

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

FIGURE 4 – INPUT OFFSET VOLTAGE

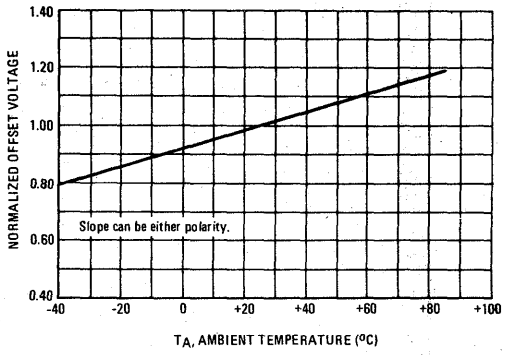


FIGURE 5 – INPUT BIAS CURRENT

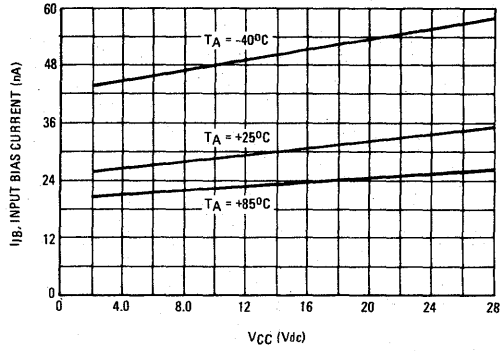


FIGURE 6 – OFFSET BIAS CURRENT

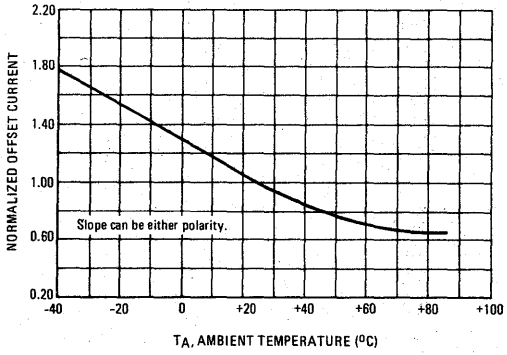


FIGURE 7 – OUTPUT CURRENT versus OUTPUT VOLTAGE

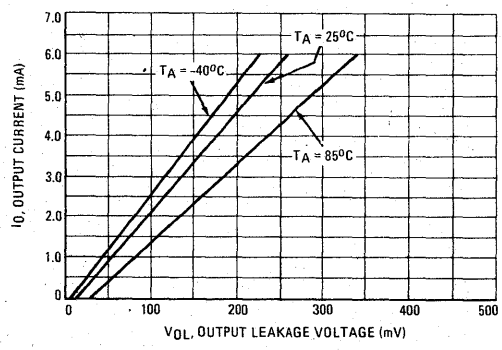
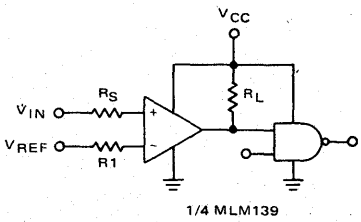


FIGURE 8 – DRIVING LOGIC

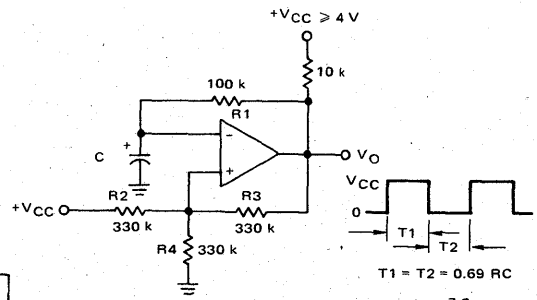


R_S = Source Resistance

$R1 \simeq R_S$

LOGIC	DEVICE	V_{CC} Volts	R_L kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5	10

FIGURE 9 – SQUAREWAVE OSCILLATOR



T1 = T2 = 0.69 RC

$f \approx \frac{7.2}{C(\mu F)}$

R2 = R3 = R4

R1 ≈ R2//R3//R4

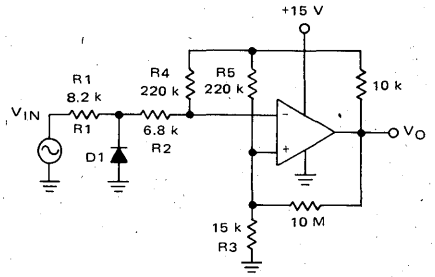
APPLICATIONS INFORMATION

The MLM139, MLM239 and MLM339 are quad comparators having high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors <10 kΩ should be used. The addition of positive feedback (<10 mV) is also recommended.

It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's input voltages. More negative than -300 mV should not be used.

FIGURE 10 – ZERO CROSSING DETECTOR (Single Supply)



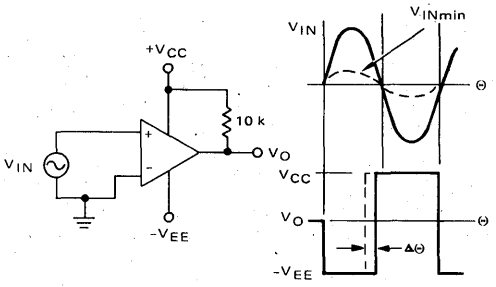
D1 prevents input from going negative by more than 0.6 V.

$R1 + R2 = R3$

$R3 \leq \frac{R5}{10}$ for small error in zero crossing

FIGURE 11 – ZERO CROSSING DETECTOR (Split Supplies)

$V_{INmin} \approx 0.4$ V peak for 1% phase distortion ($\Delta\Theta$).



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MLM139AL	—	−55°C to +125°C	Ceramic DIP
MLM239AL	—	−40°C to +85°C	Ceramic DIP
MLM239AP	—	−40°C to +85°C	Plastic DIP
MLM339AL	—	0°C to +70°C	Ceramic DIP
MLM339AP	LM339AN	0°C to +70°C	Plastic DIP

MLM139A
MLM239A
MLM339A

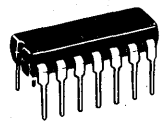
QUAD SINGLE-SUPPLY COMPARATORS

These comparators are designed for use in level detection, low-level sensing and memory applications in Consumer Automotive and Industrial electronic applications.

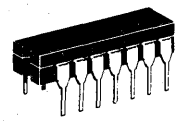
- Power Supply Options –
  Single Supply = 2.0 to 36 Vdc
  Split Supplies = ±1.0 −±18 Vdc
- Wide Operating Temperature Range – −55 to +125°C
- Low Supply Current Drain – 2.0 mA (Max)
- Low Input Biasing Current – 25 nA (Typ)
- Low Input Offset Voltage – 2.0 mV (Max)
- TTL and CMOS Compatible

QUAD COMPARATORS

SILICON MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646
(MLM239A and
MLM339A only)



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +36	Vdc
Output Sink Current	I_{sink}	20	mA
Power Dissipation @ T_A = 25°C	P_D		
Ceramic Package		1.25	Watts
Derate above 25°C		10	mW/°C
Plastic Package		1.25	Watts
Derate above 25°C		10	mW/°C
Operating Ambient Temperature Range	T_A		°C
MLM139A		-55 to +125	
MLM239A		-40 to +85	
MLM339A		0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN CONNECTIONS

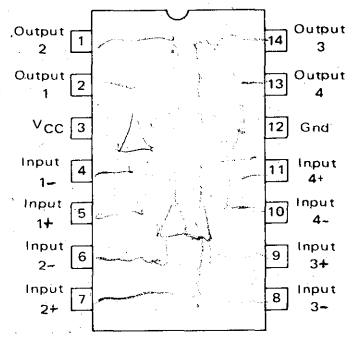
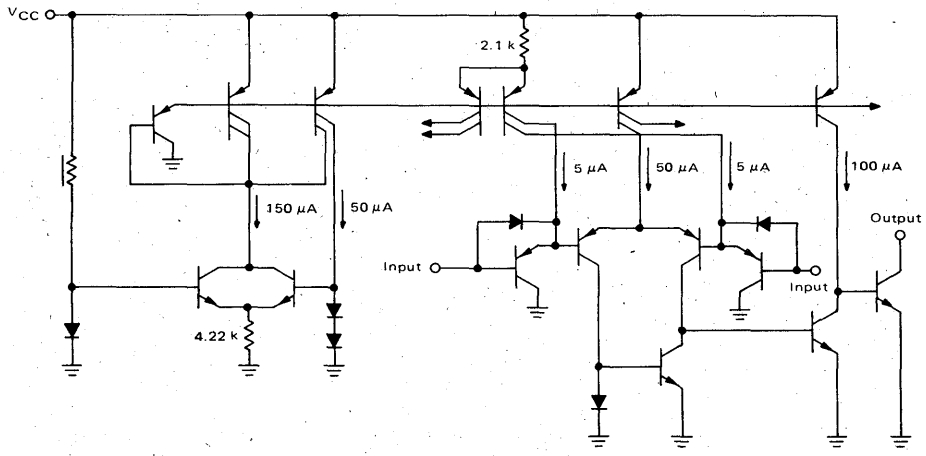


FIGURE 1 – CIRCUIT SCHEMATIC (Diagram shown is for 1 comparator)



ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = 25°C unless otherwise noted.)

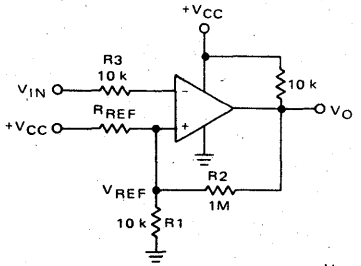
Characteristic	Symbol	MLM139A			MLM239A			MLM339A			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_{ref} = 1.4 Vdc, V_O = 1.4 Vdc, R_S = 0)	V_{IO}	–	±1.0	±2.0	–	±1.0	±2.0	–	±1.0	±2.0	mVdc
Input Offset Current	I_{IO}	–	±3.0	±25	–	±5.0	±50	–	±5.0	±50	nA
Input Bias Current	I_{IB}	–	25	100	–	25	250	–	25	250	nA
Input Common Mode Voltage Range (Note 1)	V_{ICR}	0	–	V_{CC} -1.5	0	–	V_{CC} -1.5	0	–	V_{CC} -1.5	V
Supply Current (R_L = ∞)	I_{CC} / I_{EE}	–	0.8	2.0	–	0.8	2.0	–	0.8	2.0	mA
Response Time (Note 2) (V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ)	–	–	1.3	–	–	1.3	–	–	1.3	–	μs
Output Sink Current ($V_{I(-)}$ ≥ +1.0 Vdc, $V_{I(+)}$ = 0, V_O ≤ +1.5 Vdc) ($V_{I(-)}$ ≥ +1.0 Vdc, $V_{I(+)}$ = 0, V_O ≤ 500 mVdc)	I_{sink}	 6.0 6.0	 16 –	 – –	 6.0 6.0	 16 –	 – –	 6.0 6.0	 16 –	 – –	mA
Saturation Voltage ($V_{I(-)}$ ≥ +1.0 Vdc, $V_{I(+)}$ = 0, I_{sink} ≤ 4.0 mAdc) ($V_{I(-)}$ ≥ +1.0 Vdc, $V_{I(+)}$ = 0, I_{sink} ≤ 6.0 mAdc)	V_{sat}	 – –	 – –	 500 500	 – –	 – –	 500 500	 – –	 – –	 500 500	mV
Voltage Gain (V_{CC} = 15 V) (R_L ≥15 kΩ)	A_V	50	200	–	50	200	–	50	200	–	k
Output Leakage Current ($V_{I(+)}$ ≥ +1.0 Vdc, $V_{I(-)}$ = 0, V_O = 5.0 Vdc)	I_{OL}	–	0.1	–	–	0.1	–	–	0.1	–	μA

PERFORMANCE CHARACTERISTICS – Guaranteed Over Temperature Range (V_{CC} = +5.0 Vdc)

Characteristic	Symbol	-55 to +125°C			-40°C to +85°C			0° to 70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_{ref} = +1.4 Vdc, V_O = 1.4 Vdc, R_S = 0)	V_{IO}	–	–	± 4.0	–	–	± 4.0	–	–	± 4.0	mV
Input Offset Current	I_{IO}	–	–	±100	–	–	±150	–	–	±150	nA
Input Bias Current	I_{IB}	–	–	300	–	–	400	–	–	400	nA
Input Common Mode Voltage Range	V_{ICR}	0	–	V_{CC} -2.0	0	–	V_{CC} -2.0	0	–	V_{CC} -2.0	Vdc
Saturation Voltage ($V_{I(-)}$ ≥ 1.0 Vdc, $V_{I(+)}$ = 0, I_{sink} ≤ 4.0 mAdc)	V_{sat}	–	–	700	–	–	700	–	–	700	mV
Output Leakage Current ($V_{I(+)}$ ≥ 1.0 Vdc, $V_{I(-)}$ = 0, V_O = 30 Vdc)	I_{OL}	–	–	1.0	–	–	1.0	–	–	1.0	μA
Input Differential Voltage (All V_I ≥ 0 Vdc)	V_{ID}	–	–	36	–	–	36	–	–	36	Vdc

Notes 1. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 300 mV. The upper end of the common-mode voltage range is V_{CC} -1.5 V, but either or both inputs can go to +30 Vdc without damage.
2. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger signals, 300 ns is typical.

FIGURE 2 – INVERTING COMPARATOR WITH HYSTERESIS

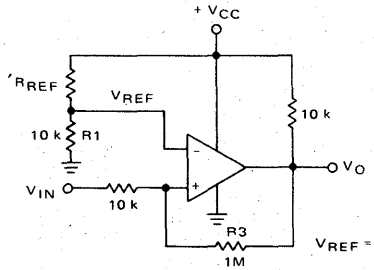


$$V_{REF} \approx \frac{V_{CC}\,R1}{R_{REF} + R1}$$

$$R3 \approx R1 \,//\, R_{REF} \,//\, R1$$

$$V_H = \frac{R1 // R_{REF}}{R1 // R_{REF} + R2} \quad (V_{Omax} - V_{Omin})$$

FIGURE 3 – NON-INVERTING COMPARATOR WITH HYSTERESIS



$$V_{REF} = \frac{V_{CC}\,R1}{R_{REF} + R1}$$

$$R2 \approx R1 // R_{REF}$$

Amount of Hysteresis V_M

$$V_H = \frac{R2}{R2 + R3} \quad (V_{Omax} - V_{Omin})$$

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

FIGURE 4 – INPUT OFFSET VOLTAGE

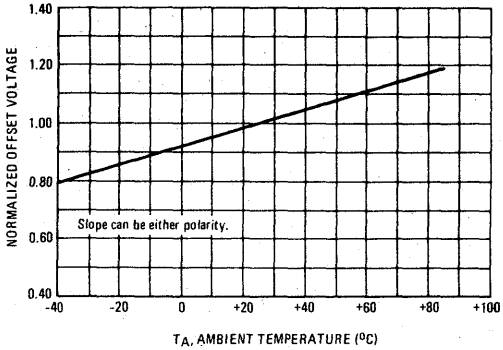


FIGURE 5 – INPUT BIAS CURRENT

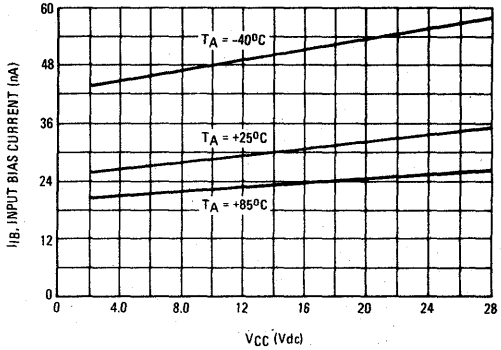


FIGURE 6 – OFFSET BIAS CURRENT

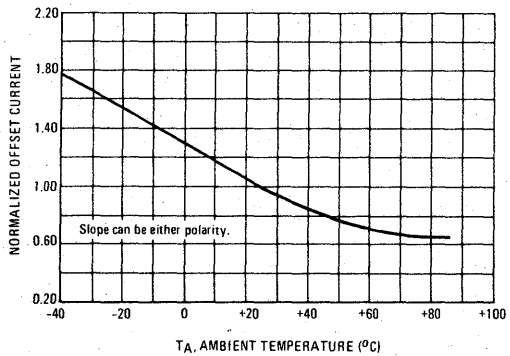


FIGURE 7 – OUTPUT CURRENT versus OUTPUT VOLTAGE

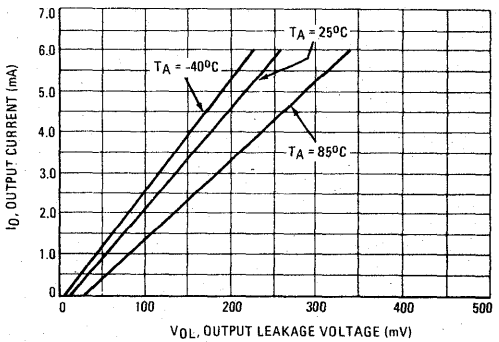
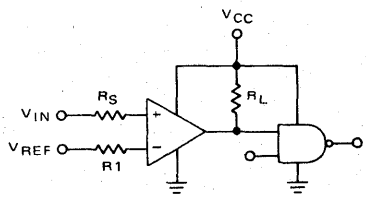


FIGURE 8 – DRIVING LOGIC

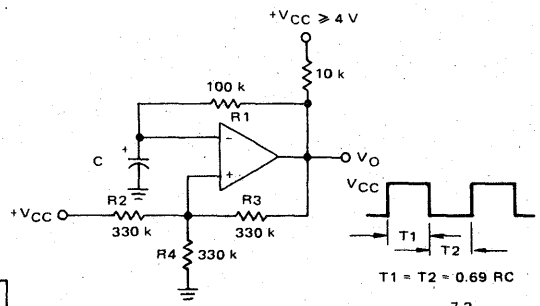


R_S = Source Resistance

$R1 \simeq R_S$

LOGIC	DEVICE	V_{CC} Volts	R_L kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5	10

FIGURE 9 – SQUAREWAVE OSCILLATOR



T1 = T2 = 0.69 RC

$f \approx \frac{7.2}{C\,(\mu F)}$

R2 = R3 = R4

R1 ≈ R2//R3//R4

6

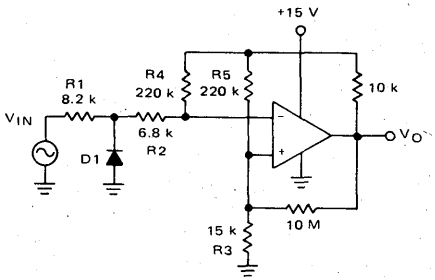
APPLICATIONS INFORMATION

The MLM139A, MLM239A and MLM339A are quad comparators having high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors <10 kΩ should be used. The addition of positive feedback (<10 mV) is also recommended.

It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's input voltages. More negative than -300 mV should not be used.

FIGURE 10 – ZERO CROSSING DETECTOR (Single Supply)



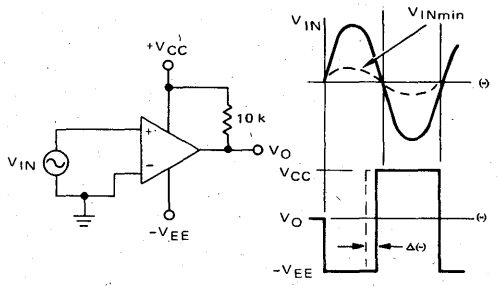
D1 prevents input from going negative by more than 0.6 V.

$R1 + R2 = R3$

$R3 \leq \frac{R5}{10}$ for small error in zero crossing

FIGURE 11 – ZERO CROSSING DETECTOR (Split Supplies)

$V_{INmin} \approx 0.4$ V peak for 1% phase distortion ($\Delta\Theta$).



ORDERING INFORMATION

Device	Temperature Range	Package
MLM2901P	−40°C to +85°C	Plastic DIP

MLM2901

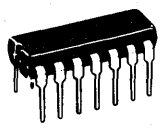
QUAD SINGLE-SUPPLY COMPARATOR

This comparator is designed for use in level detection, low-level sensing and memory applications in Consumer Automotive and Industrial electronic applications.

- Power Supply Options –
  Single Supply = 2.0 to 36 Vdc
  Split Supplies = ±1.0 to ±18 Vdc
- Wide Operating Temperature Range – -40 to +85°C
- Low Supply Current Drain – 2.0 mA (Max)
- Low Input Biasing Current – 25 nA (Typ)
- Low Input Offset Voltage – 2.0 mV (Max)
- TTL and CMOS Compatible

QUAD COMPARATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +36	Vdc
Output Sink Current	I_{sink}	20	mA
Power Dissipation @ T_A = 25°C Plastic Package Derate above 25°C	P_D	 1.25 10	 Watts mW/°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

PIN CONNECTIONS

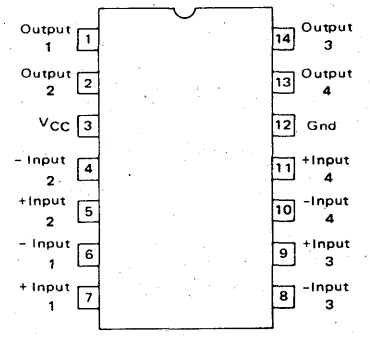


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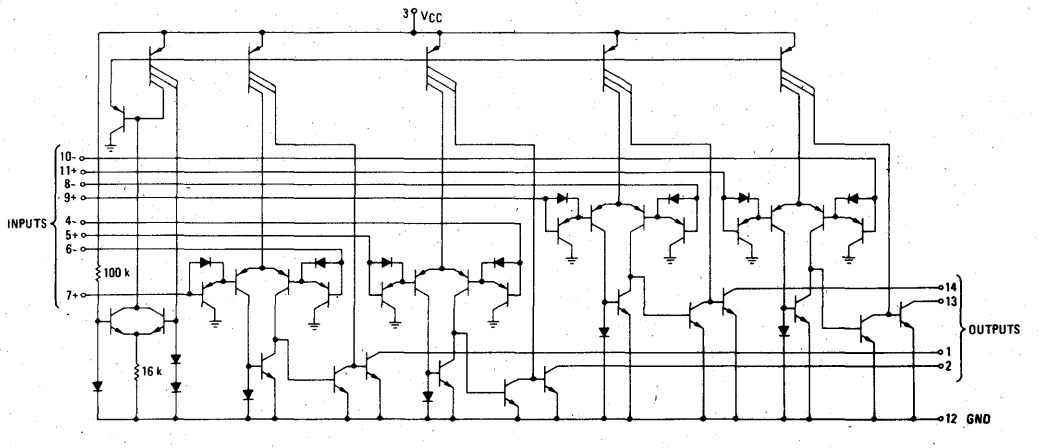
FIGURE 1 – CIRCUIT SCHEMATIC



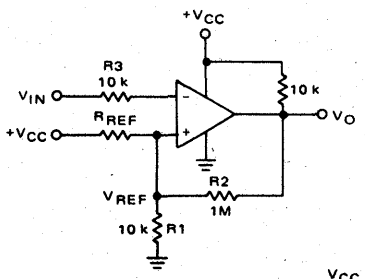
ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{ref} = 1.4 Vdc, V_O = 1.4 Vdc, R_S = 0)	V_{IO}	–	2.0	7.0	mVdc
Input Offset Current	I_{IO}	–	±5.0	±50	nA
Input Bias Current	I_{IB}	–	25	250	nA
Input Common Mode Voltage Range (Note 1)	V_{ICR}	0	–	V_{CC} -1.5	V
Supply Current (R_L = ∞)	I_{CC} I_{EE}	–	0.8	2.0	mA
Response Time (Note 2) (V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ)	–	–	1.3	–	μs
Output Sink Current ($V_{I(-)} \geq$ +1.0 Vdc, $V_{I(+)}$ = 0, $V_O \leq$ +1.5 Vdc)	I_{sink}	6.0	16	–	mA
Saturation Voltage ($V_{I(-)} \geq$ +1.0 Vdc, $V_{I(+)}$ = 0, I_{sink} = 3.0 mAdc)	V_{sat}	–	–	400	mV
Output Leakage Current ($V_{I(+)} \geq$ +1.0 Vdc, $V_{I(-)}$ = 0, V_O = 5.0 Vdc)	I_{OL}	–	0.1	–	μA

Notes 1. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 300 mV. The upper end of the common-mode voltage range is V_{CC} -1.5 V, but either or both inputs can go to +30 Vdc without damage.
2. The response time specified is for a 100 mV input step with 5 mV overdrive. For large signals, 300 ns is typical.

6

FIGURE 2 – INVERTING COMPARATOR WITH HYSTERESIS

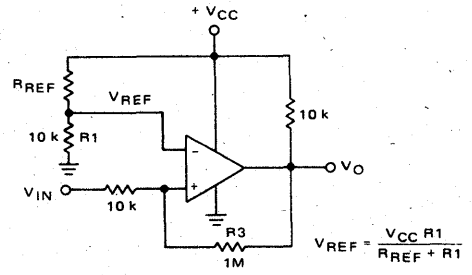


$$V_{REF} \approx \frac{V_{CC}\,R1}{R_{REF} + R1}$$

$$R3 \approx R1 \,//\, R_{REF} \,//\, R1$$

$$V_H = \frac{R1 // R_{REF}}{R1 // R_{REF} + R2} \quad (V_{Omax} - V_{Omin})$$

FIGURE 3 – NON-INVERTING COMPARATOR WITH HYSTERESIS



$$V_{REF} = \frac{V_{CC}\,R1}{R_{REF} + R1}$$

$$R2 \approx R1 // R_{REF}$$

Amount of Hysteresis V_M

$$V_H = \frac{R2}{R2 + R3} \quad (V_{Omax} - V_{Omin})$$

TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 4 – INPUT OFFSET VOLTAGE

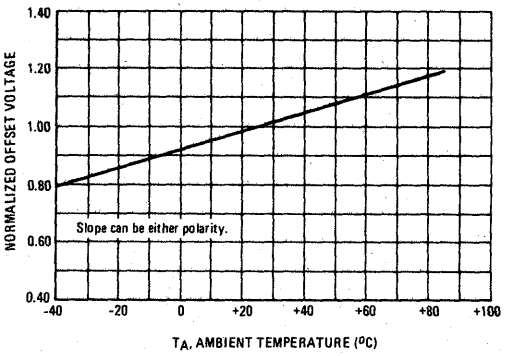


FIGURE 5 – INPUT BIAS CURRENT

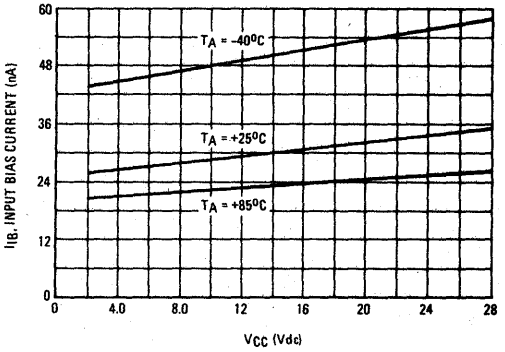


FIGURE 6 – OFFSET BIAS CURRENT

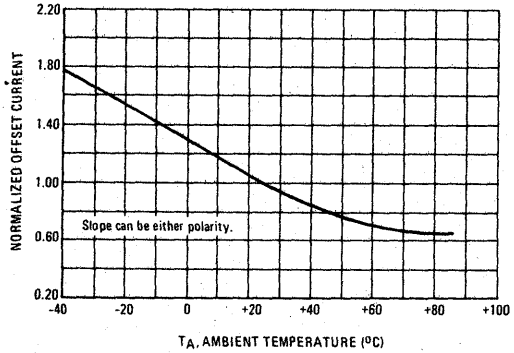


FIGURE 7 – OUTPUT CURRENT versus OUTPUT VOLTAGE

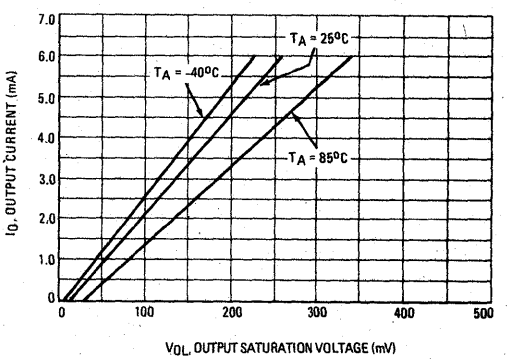
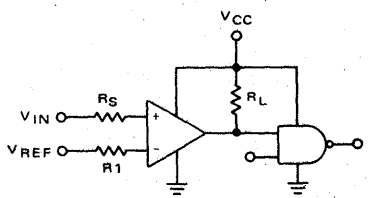


FIGURE 8 – DRIVING LOGIC



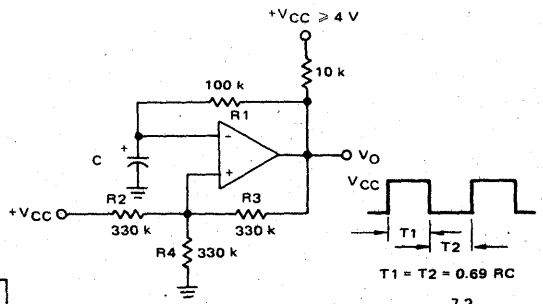
1/4 MLM2901P

R_S = Source Resistance

$R1 \approx R_S$

LOGIC	DEVICE	V_{CC} Volts	R_L kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5	10

FIGURE 9 – SQUAREWAVE OSCILLATOR



T1 = T2 = 0.69 RC

$f \approx \frac{7.2}{C(\mu F)}$

R2 = R3 = R4

R1 ≈ R2//R3//R4

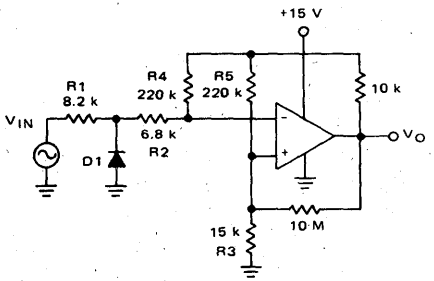
APPLICATIONS INFORMATION

The MLM2901P is a quad comparator having high gain, wide bandwidth characteristics. This gives the device oscillator tendencies if the outputs capacitively couple to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors <10 kΩ should not be used. The addition of positive feedback (<10 mV) is also recommended

It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's input voltages. More negative than -300 mV should not be used.

FIGURE 10 – ZERO CROSSING DETECTOR
(Single Supply)



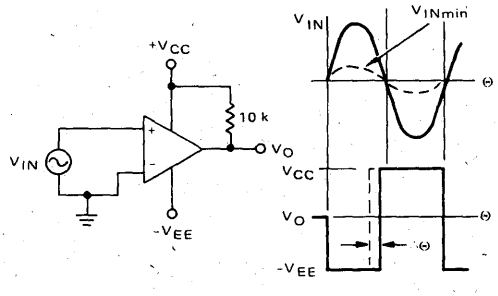
D1 prevents input from going negative by more than 0.6 V.

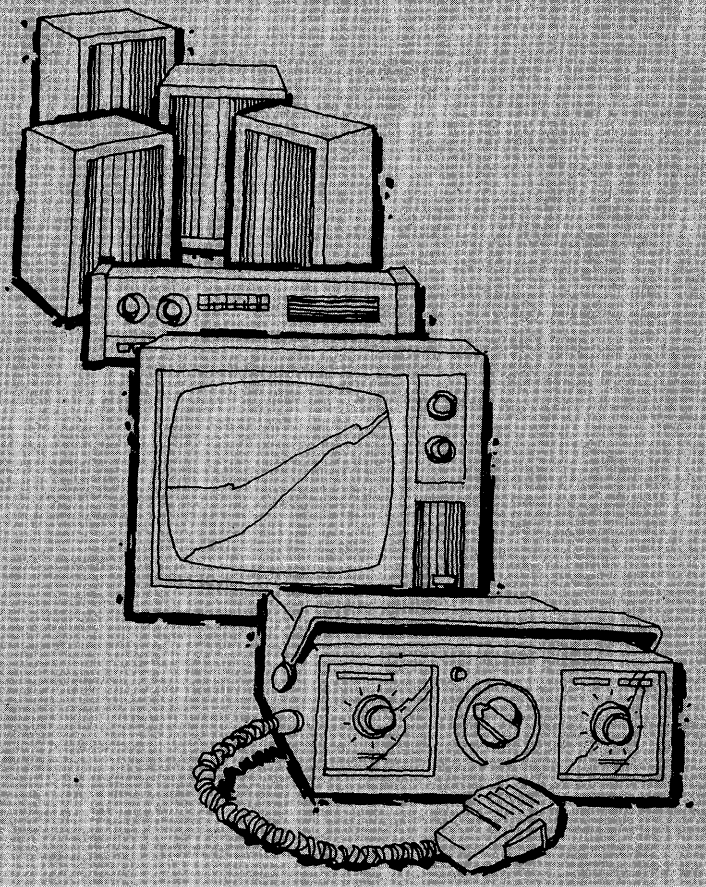
$R1 + R2 = R3$

$R3 \leq \frac{R5}{10}$ for small error in zero crossing

FIGURE 11 – ZERO CROSSING DETECTOR
(Split Supplies)

$V_{INmin} \approx 0.4$ V peak for 1% phase distortion ($\Delta\Theta$).





Consumer Circuits / Chapter 7

CONSUMER CIRCUITS

Circuits for Consumer Applications

. . . reflecting Motorola's continuing commitment to semiconductor products necessary for consumer system designs. This tabulation is arranged to simplify first-order selection of consumer integrated circuit devices that satisfy the primary functions for Television, Audio, Radio, Citizens Band, Automotive and Organ applications.

TELEVISION CIRCUITS

SOUND

Function	Features	Case	Type
Sound IF, Detector, Limiter, Audio Preamplifier	80 μV, 3dB Limiting Sensitivity, 3.5 V(RMS) Output, Sufficient for Single Transistor Output Stage	646,647	MC1351
Sound IF Detector	Interchangeable with ULN2111A	646,647	MC1357
Sound IF Detector, dc Volume Control, Preamplifier	Excellent AMR, Interchangeable with CA3065	646,647	MC1358
Sound IF, Low Pass Filter, Detector, dc Volume Control, Pre-Amplifier, Power Amplifier	Complete TV Sound System 100 μV 3 dB Limiting Sensitivity 4 Watts Output, V_{CC} = 24V, R_L = 16 Ω	722A	TDA1190Z

VIDEO

1st and 2nd Video IF Amplifier	IF Gain @ 45 MHz—60 dB Type AGC Range—70 dB min	626	MC1349
	IF Gain @ 45 MHz—46 dB typ, AGC Range—60 dB min	626	MC1350
1st and 2nd Video IF, AGC Keyer and Amplifier	IF Gain @ 45 MHz—53 dB typ, AGC Range—65 dB min, "Forward AGC" Provided for Tuner	646,647	MC1352
3rd IF, Video Detector, Video Buffer, and AFC Buffer	Low-Level Detection Low Harmonic Generation Zero Signal dc Output Voltage of 7.0 to 8.2 V	626	MC1330A1
	Same as MC1330A1 except zero signal dc output voltage of 7.8 to 9.0 V	626	MC1330A2
3rd IF, Video Detector, Sound IF Detector, and Sync Separator	Low-Level Detection, Separate Sound Detector, Differential Inputs	646	MC1331
AGC Keyer, AGC Amplifier, Noise Gate, Sync Separator	High-Quality Noise Gate, One IF AGC Output and Two Tuner AGC Outputs, Adjustable AGC Delay	646	MC1344
Automatic Fine Tuning	High Gain AFT System, Interchangeable with CA3064	646	MC1364

CHROMA

Chroma IF Amplifier and Subcarrier System	Includes Complete Chroma IF, AGC, dc Gain and Tint Controls, Injection Locked Oscillator. Low Peripheral Parts Count	646	MC1398
Chroma IF Amplifier and Subcarrier System (PLL)	Includes Complete Chroma IF, AGC, dc Chroma and Hue Controls, Phase Locked Loop (PLL) Oscillator, Color Killer Threshold Adjustment.	648	MC1399
Dual Chroma Demodulators	Dual Doubly Balanced Demodulator with RGB Matrix and Chroma Driver Stages	646	MC1324
	Dual Doubly Balanced Demodulator with RGB Output Matrix and PAL Switch	646,647	MC1327
Triple Chroma Demodulator	Triple Doubly Balanced Demodulator with Adjustable Output Matrix, Contains Three Independent Demodulators.	648	MC1323

DEFLECTION

Function	Features	Case	Type
Horizontal Processor	Includes Phase-Detector, Oscillator and Predriver: Linear Balanced Phase Detector Adjustable dc Loop Gain	626	MC1391
	Same as MC1391 except designed to accept negative sawtooth sync pulse	626	MC1394
Vertical Processor	Includes Oscillator and Complementary Driver, Low Thermal Drift, Retrace Pulse for Effective Blanking	648	MC1393

AUDIO CIRCUITS

PREAMPLIFIERS

Function	V_{CC} Vdc Max	A_{vol} dB Min	THD % Typ	z_o Ohms Typ	Case	Type
Dual Preamplifier	±15	80	0.1	100	646	MC1303

DRIVERS

Function	V_{CC} Vdc Max	Drive Current mA	A_{vol} dB	Case	Type
Class B Audio Drivers	35	150 peak	89 typ	626	MC3320
	20	150 peak	87 typ	626	MC3321
	25	50 max	—	646	MC1385

POWER AMPLIFIERS

Function	P_O Watts	V_{CC} Vdc Max	c_{in} @ rated P_O mV Typ	I_D mA Typ	R_L Ohms	Case	Type
Audio Power Amplifiers	0.5	12	3.0	4.0	8.0	626	MC1306
	0.25	12	3.0	3.0	16	626	MC3360
	4.0	18	22.0	12	4.0	722	MC1384

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RADIO CIRCUITS

IF AMPLIFIERS

Function	Gain @ 10.7 MHz dB Typ	3 dB Limiting @ 10.7 MHz mV (RMS) typ	AMR dB Typ	Recovered Audio Output f = ±75 kHz mV (RMS)	Power Supply Volts Max	Case	Type
IF Amplifier	58	0.175	60	690	18	626	MC1350
Limiting FM-IF Amplifier	-	0.600	45	480	18	646, 647	MC1355
Limiting IF Ampl/Quadrature Detector with Built-In Regulator	-	0.4	42	450	16	646	MC1356
Limiting IF Ampl/Quad Detector	53	0.4	45	480	16	646, 647	MC1357
IF Amplifier, Limiter, Detector, Audio Preamplifier	21	0.25	55	625	16	646	MC1375
IF Amplifier	42	60	50	500	18	626	MC3310

DECODERS

Function	Channel Separation dB Typ	THD % Typ	Stereo—Indicator Lamp Driver mA Max	Features	Case	Type
FM Multiplex Stereo Decoder	40	0.3	75	Coilless Operation	646	MC1310
Four Channel SQ† Decoders	45	0.1	-	V_{CC} = 20 Vdc nom	646	MC1312
Four Channel SQ† Gain and Balance Control	-	-	-	Master Volume Control and LF/RF, LB/RB, E/B Balance Control	648	MC1314
Four Channel SQ† Logic Circuit	-	-	-	Interface with MC1314 and MC1312 to increase F/B Separation and Supply Gain and Balance Control to MC1314.	648	MC1315

†Trademark of Columbia Broadcasting System, Inc.

ORGAN CIRCUITS

FREQUENCY DIVIDER

Function	V_{CC} Range Vdc	f_{Tog} MHz Typ	V_{OH} Vdc Min	Case	Type
7-Stage Divider	6-16	1.0	12.0/15.0	646	MC1302

ATTENUATOR

Function	V_{CC} Range Vdc	THD % Typ	A_V dB Typ	Attenuation Range dB Typ	Case	Type
Electronic Attenuator	9.0 to 18	0.6	13	90	626	MC3340

AUTOMOTIVE CIRCUITS

OPERATIONAL AMPLIFIER

Function	V_{CC} Range Vdc	A_{VOL} V/V Min	I_{IB} A Max	Unity Gain Bandwidth MHz Typ	Case	Type
Quad Operational Amplifier	4.0—28	1000	0.3	4.0	646	MC3301

COMPARATORS

Function	V_{CC} Range Vdc	V_{IO} mV Max	I_{IO} nA Max	I_{IB} na Max	Sink Current mA Typ	Case	Type
Quad Comparators	2.0—28	±20		500	6.0	646, 632	MC3302
	2.0—36	±7.0	±50	250	16.0	646	MLM2901
		±5.0				646, 632	MLM239
		±2.0				646, 632	MLM239A

VOLTAGE REGULATOR

Function	Features	Case	Type
Automotive Voltage Regulator	Designed for use with NPN Darlington Overvoltage Protection "Open Sense" Shut Down Selectable Temperature Coefficient	646	MC3325

ELECTRONIC IGNITION

Function	Features	Case	Type
Electronic Ignition Circuit	Designed for use in High Energy-Variable Dwell Electronic Ignition Systems with Variable Reluctance Sensors. Dwell and Spark Energy are Externally Adjustable.	646	MC3333

TRANSISTOR ARRAYS

GENERAL PURPOSE

Function	I_{C} (max) mA	V_{CEO} Volts Max	V_{CBO} Volts Max	V_{EBO} Volts Max	Case	Type
One Differentially connected pair and Three Isolated Transistors	50	15	20	5.0	646	MC3346 MC3386
One Differentially Connected Pair with Associated Constant Current Transistor	50	20	20	5.0	626	MC3330

SPECIAL FUNCTIONS

Function	Features	Case	Type
Emitter-Coupled Astable Multivibrator	Useful as DC-DC Converter, Power Regulator or Multivibrator. Toggle Freq = 100 kHz (typ).	626	MC3380
Phase Lock Loop	Contains Voltage Controlled Oscillator and Double Balanced Phase Detector	646	MLM565
Frequency to Voltage Converter	Frequency Doubling for Low Output Ripple Programmable Threshold and Hysteresis	646	MC3315
Dual Frequency to Voltage Converters	Frequency Doubling for Low Output Ripple Programmable Threshold and Hysteresis Two Independent Channels	648	MC3316
	Same as MC3316 . . . Plus Fail Check Indication for Open Sensor High and Low Select Outputs	701	MC3317
Programmable Frequency Switch	Wide Input Frequency Range (10 Hz to 100 kHz) Adjustable Hysteresis Wide Supply Operating Range (7 to 24V)	646, 632	MC3344

CITIZENS BAND CIRCUITS

SYNTHESIZER

Function	Features	Case	Type
Phase Lock Loop Frequency Synthesizer	Requires only One Crystal to Generate All Transmit and Receive Frequencies Can be used with Binary Coded Switch Designed for Double or Single Conversions Receivers	724	MC3390

CONTROLLER

Remote Controller and Display Driver	Designed for use with a Push Button Switch for Incremental up/down Channel Selection of the MC3390 Provides Display Drive Current	724	MC3391

MC1302

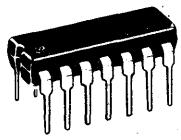
7-STAGE DIVIDER

This monolithic circuit is designed for use as a frequency divider in electronic organs. It contains 7 flip-flops with all inputs and outputs externally accessible.

- Wide Operating Voltage Range – 6.0 to 16 Volts
- Regulated Supply Not Required
- Maximum Design Flexibility – Allows for Two to Seven-Stage Cascades

7-STAGE DIVIDER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

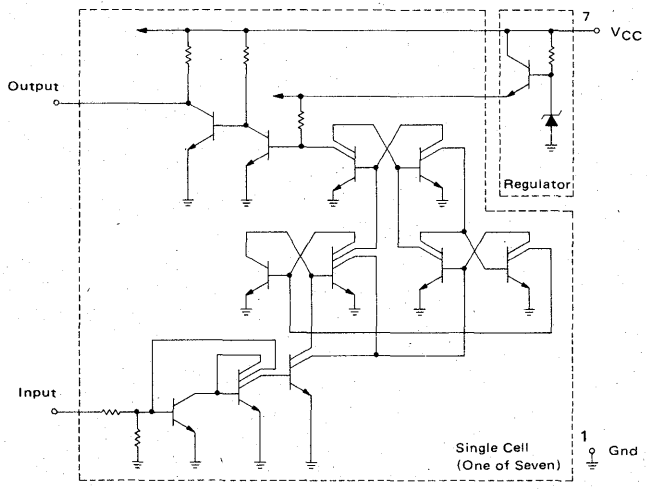


P SUFFIX
PLASTIC PACKAGE
CASE 646

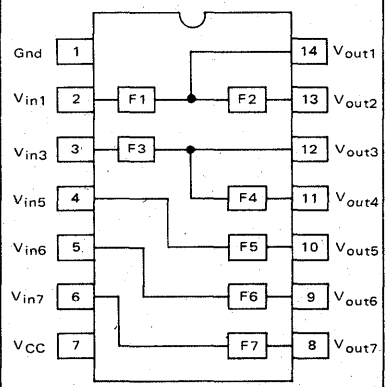
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Volts
Power Supply Voltage	19	Vdc
Output Sinking Current	10	mA
Negative Input Voltage	0.5	Vdc
Junction Temperature	150	°C
Operating Temperature Range	0 to +75	°C

FIGURE 1 – CIRCUIT SCHEMATIC



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC1302P	0 to +75	Plastic DIP

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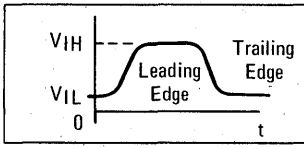
ELECTRICAL CHARACTERISTICS (V_{CC} = 16 Vdc, V_{in} = 4.0 V, Square Pulse, f = 10 kHz, 50% Duty Cycle, t_{PHL} = 1.0 V/μs, T_A = +25°C, unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Operating Power Supply Voltage	6.0	—	16	Vdc
Toggle Frequency	—	1.0	—	MHz
Output Voltage (High) Pins 8, 9, 10, 11, & 13				Vdc
(V_{CC} = 6.0 Vdc)	5.5	—	—	
(V_{CC} = 16 Vdc)	15.0	—	—	
Output Voltage (High) Pins 12 & 14				Vdc
(V_{CC} = 6.0 Vdc)	4.5	—	—	
(V_{CC} = 16 Vdc)	12	—	—	
Operating Drain Current				mAdc
(V_{CC} = 16 Vdc)	—	26	—	
Output Sinking Current				mAdc
(V_O < 0.5 Vdc)	—	10	—	
Rise Time	—	100	—	ns
Propagation Delay	—	700	—	ns
Fall Time	—	50	—	ns
Input Resistance	10	—	—	kΩ
Output Resistance (Output High)	—	—	5.0	kΩ

INPUT PULSE REQUIREMENTS



Characteristic	Min	Max	Unit
Pulse Magnitude	+4.0	—	Volts
Zero Level	—	+1.0	Volts
Leading Edge	No Requirement		
Trailing Edge dv/dt	-1.0	—	$\frac{\text{Volts}}{\text{ms}}$

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\,(Typ)}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst-case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient

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ORDERING INFORMATION

Device	Temperature Range	Package
MC1303P	0°C to +75°C	Plastic DIP

MC1303

DUAL STEREO PREAMPLIFIER

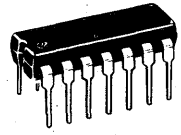
. . . designed for amplifying low-level stereo audio signals with two preamplifiers built into a single monolithic semiconductor.

Each Preamplifier Features:

- Large Output Voltage Swing – 4.0 V (RMS) Min
- High Open-Loop Voltage Gain = 6000 min
- Channel Separation = 60 dB min at 10 kHz
- Short-Circuit-Proof Design

DUAL STEREO PREAMPLIFIER INTEGRATED CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

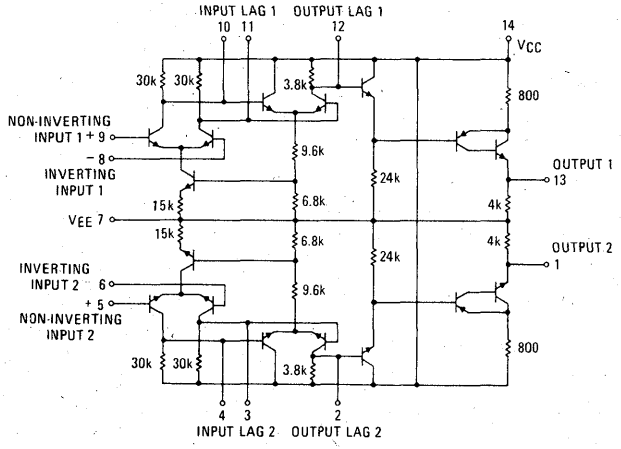


P SUFFIX
PLASTIC PACKAGE
CASE 646

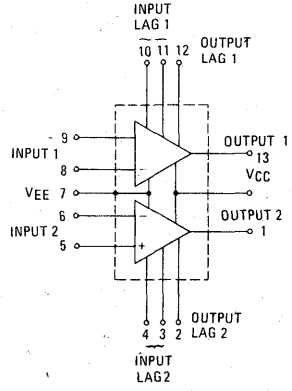
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	+15 -15	Vdc
Junction Temperature	+150	°C
Operating Ambient Temperature Range	0 to +75	°C

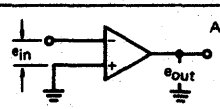
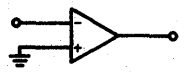
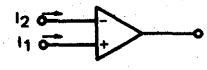
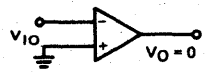
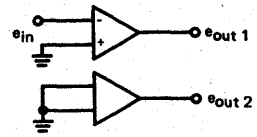
CIRCUIT SCHEMATIC



EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (Each Preamplifier) (V_{CC} = +13 Vdc, V_{EE} = -13 Vdc, T_A = +25°C unless otherwise noted).

Characteristic Definitions (linear operations)	Characteristic	Min	Typ	Max	Unit
	Open Loop Voltage Gain	6,000	10,000	–	V/V
	Output Voltage Swing (R_L = 10 kΩ)	4.0	5.5	–	V(RMS)
	Input Bias Current $I_{IB} = \frac{I_1+I_2}{2}$	–	1.0	10	μA
	Input Offset Current ($I_{IO} = I_1 - I_2$)	–	0.2	0.4	μA
	Input Offset Voltage	–	1.5	10	mV
	DC Power Dissipation (Power Supply = ±13 V, V_O = 0)	–	–	400	mW
	Channel Separation (f = 10 kHz)	60	70	–	dB

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

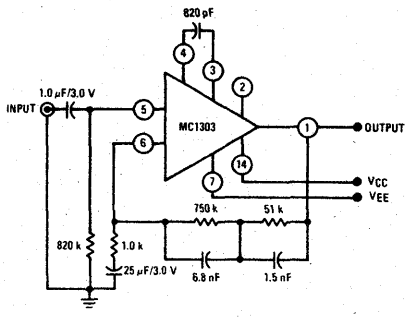
$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

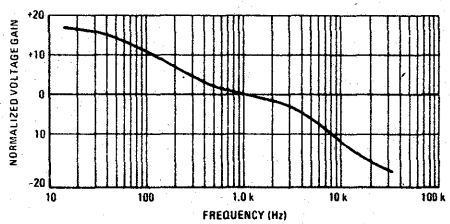
T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

TYPICAL PREAMPLIFIER APPLICATIONS

FIGURE 1 – MAGNETIC PHONO PLAYBACK PREAMPLIFIER/RIAA EQUALIZED



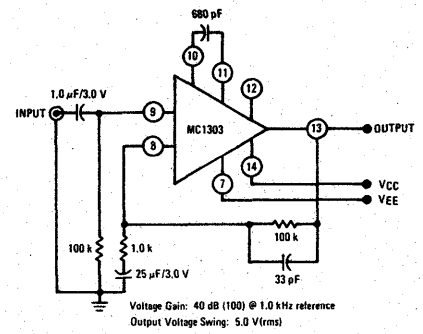


TYPICAL PERFORMANCE CHARACTERISTICS

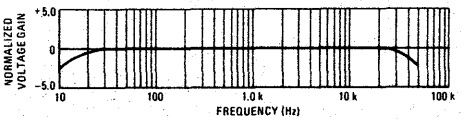
Voltage Gain	34 dB (50)@ 1.0 kHz
Input Overload Point	100 mVRMS @ 1.0 kHz
Output Voltage Swing	5.0 VRMS @ 1.0 kHz @ 0.1% THD.
Output Noise Level	Better Than 70 dB Below 10 mV Phono Input (Input Shorted)

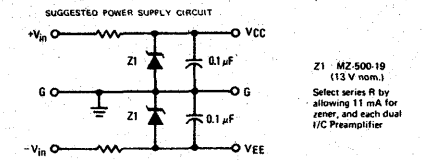
Pins not shown are not connected.

FIGURE 2 – BROAD BAND AUDIO AMPLIFIER



Voltage Gain: 40 dB (100) @ 1.0 kHz reference
Output Voltage Swing: 5.0 V(rms)

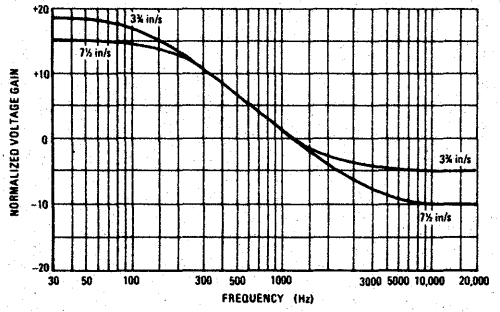


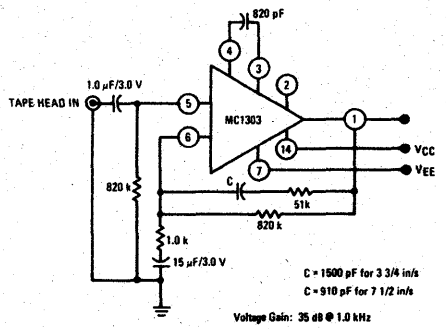


Z1 MZ-500-19 (13 V nom.)
Select series R by allowing 11 mA for zener, and each dual I/C Preamplifier

Pins not shown are not connected.

FIGURE 3 – NAB TAPE HEAD EQUALIZATION





C = 1500 pF for 3 3/4 in/s
C = 910 pF for 7 1/2 in/s

Voltage Gain: 35 dB @ 1.0 kHz
Output Voltage Swing: 5.0 V(RMS)

Pins not shown are not connected.

FIGURE 4 – POWER DISSIPATION versus SUPPLY VOLTAGE

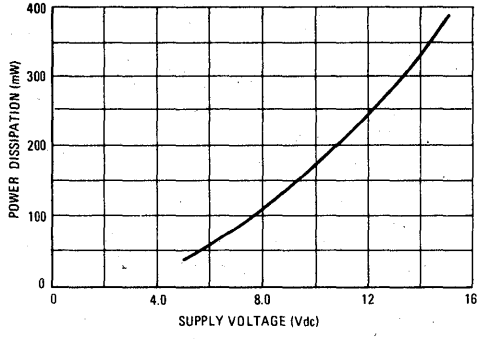


FIGURE 5 – OUTPUT LINEARITY

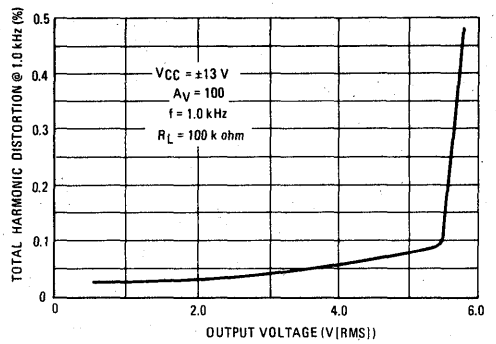
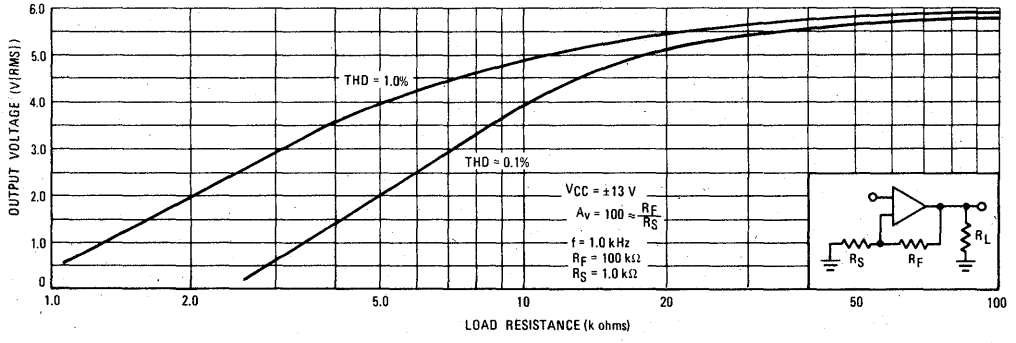


FIGURE 6 – INFLUENCE OF OUTPUT LOADING



NOISE CHARACTERISTICS

FIGURE 7A– INFLUENCE OF SOURCE RESISTANCE & BANDWIDTH

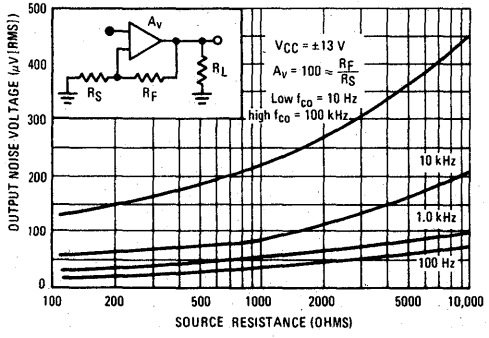
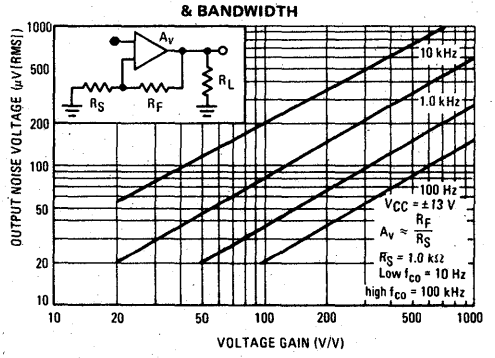


FIGURE 7B – INFLUENCE OF VOLTAGE GAIN & BANDWIDTH



ORDERING INFORMATION

Device	Temperature Range	Package
MC1306P	0°C to +75°C	Plastic DIP

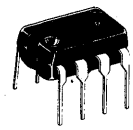
MC1306

1/2-WATT AUDIO AMPLIFIER

The MC1306P is a monolithic complementary power amplifier and preamplifier designed to deliver 1/2-Watt into a loudspeaker with a 3.0 mV(rms) typical input. Gain and bandwidth are externally adjustable. Typical applications include portable AM-FM radios, tape recorder, phonographs, and intercoms.

- 1/2-Watt Power Output (9.0 Vdc Supply, 8-Ohm Load)
- High Overall Gain – 3.0 mV(rms) Sensitivity for 1/2-Watt Output
- Low Zero-Signal Current Drain – 4.0 mAdc @ 9.0 V typ
- Low Distortion – 0.5% at 250 mW typ

1/2-WATT AUDIO AMPLIFIER



PLASTIC PACKAGE
CASE 626

TYPICAL APPLICATIONS

FIGURE 1 – AM-FM RADIO, AUDIO SECTION

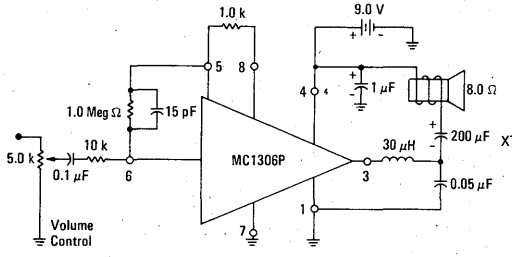
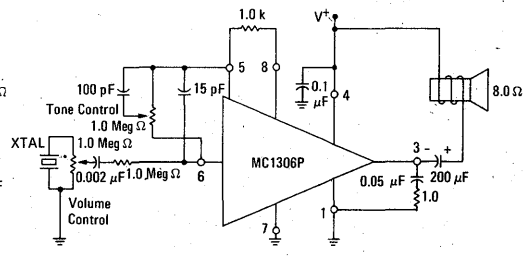
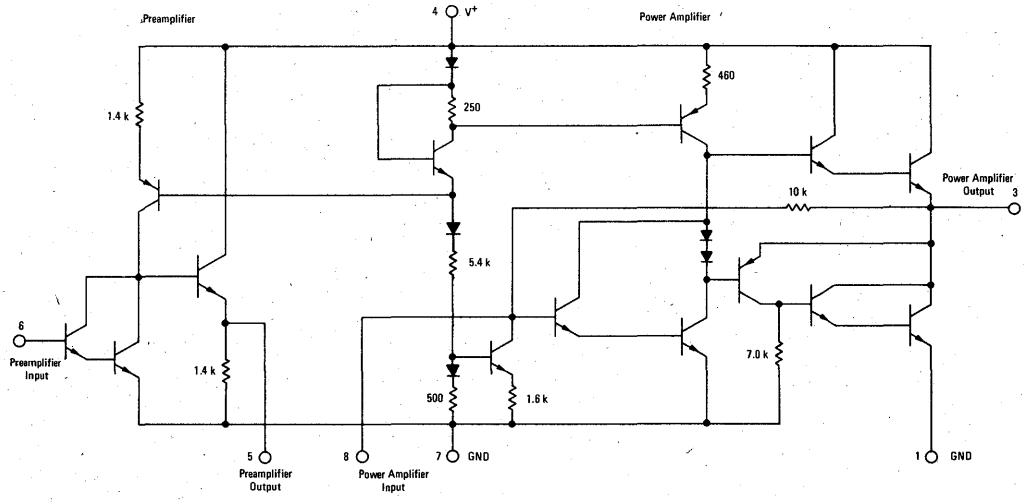


FIGURE 2 – PHONOGRAPH AMPLIFIER (CERAMIC CARTRIDGE)



CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	12	Vdc
Load Current	I_L	400	mAdc
Power Dissipation (Package Limitation) T_A = +25°C Derate above T_A = +25°C	P_D $1/\theta J_A$	625 5.0	mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = 9.0 V, R_L = 8.0 ohms, f = 1.0 kHz, (using test circuit of Figure 3), T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Open Loop Voltage Gain Pre-amplifier R_L = 1.0 k ohm Power-amplifier R_L = 16 ohms	A_{VOL}	 – –	 270 360	 – –	V/V
Sensitivity (P_o = 500 mW)	S	–	3.0	–	mV(rms)
Output Impedance (Power-amplifier)	Z_o	–	0.5	–	Ohm
Signal to Noise Ratio (P_o = 150 mW, f = 300 Hz to 10 kHz)	S/N	–	55	–	dB
Total Harmonic Distortion (P_o = 250 mW)	THD	–	0.5	–	%
Quiescent Output Voltage	V_o	–	$V^+/2$	–	Vdc
Output Power (THD ≤ 10%)	P_o	 500	 570	–	mW
Current Drain (zero signal)	I_D	–	4.0	–	mA
Power Dissipation (zero signal)	P_D	–	36	–	mW

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FIGURE 3 – TEST CIRCUIT

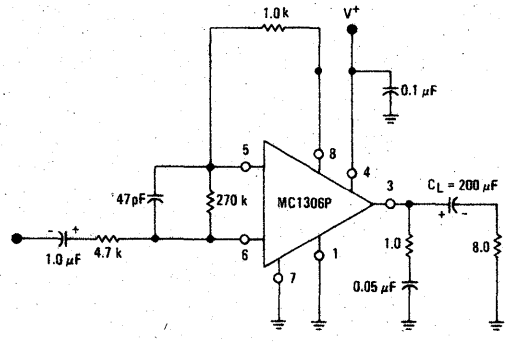
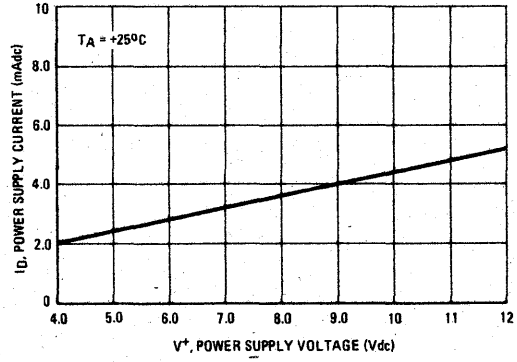


FIGURE 4 – ZERO SIGNAL BIAS CURRENT



TYPICAL CHARACTERISTICS

(V^+ = 9.0 V, f = 1.0 kHz, T_A = +25°C unless otherwise noted)

FIGURE 5 – EFFICIENCY

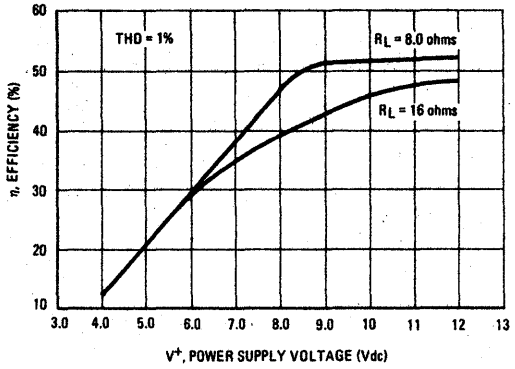


FIGURE 6 – OUTPUT POWER

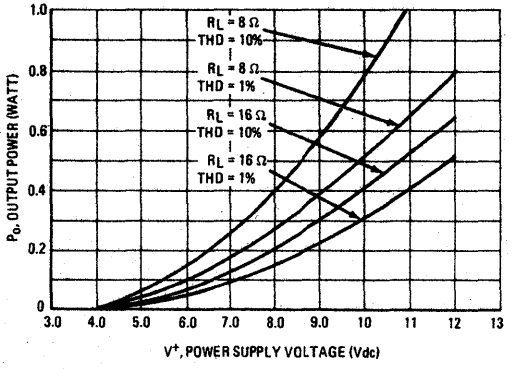


FIGURE 7 – TOTAL HARMONIC DISTORTION

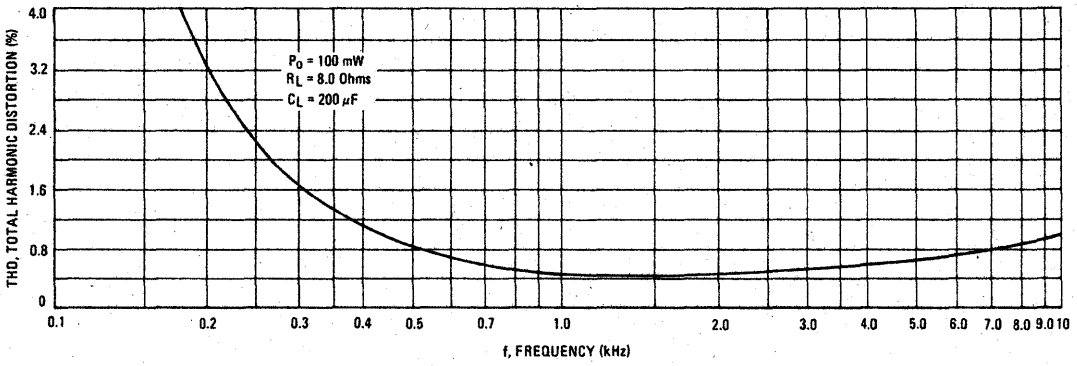


FIGURE 8 – EFFECT OF BATTERY AGING ON LOW-LEVEL DISTORTION

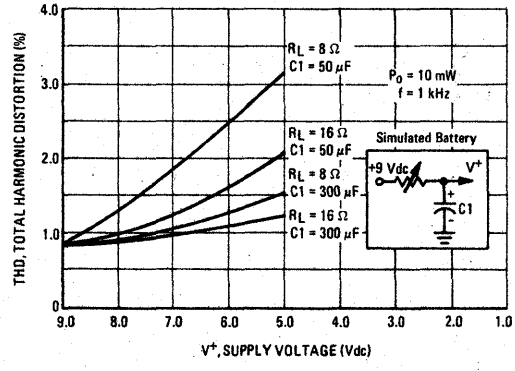


FIGURE 9 – DISTORTION

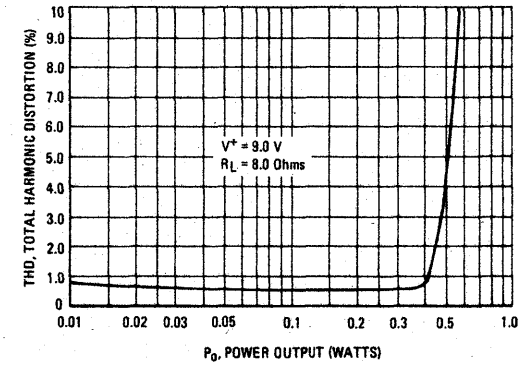


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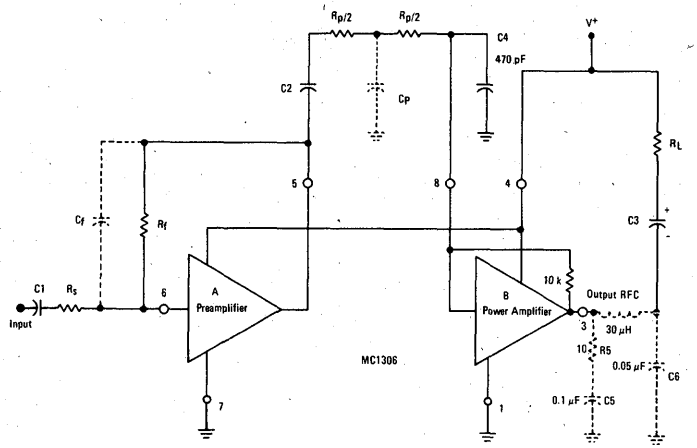
FIGURE 10 – TYPICAL CIRCUIT CONNECTION



DESIGN CONSIDERATIONS

The MC1306P provides the designer with a means to control preamplifier gain, power amplifier gain, input impedance, and frequency response. The following relationships will serve as guides.

1. Gain

The Preamplifier Stage Voltage Gain is:

$$A_{V_A} \approx \frac{R_f}{R_s}$$

and is limited only by the open-loop gain (270 V/V). For good preamplifier dc stability R_f should be no larger than 1.0-megohm.

The Power Amplifier Voltage Gain is controlled in a similar manner where:

$$A_{V_B} \approx \frac{10\ k}{R_p}$$

The 10-k ohm feedback resistor is provided in the integrated circuit.

Recommended values of R_p range from 500-ohms to 3.3-k ohms. The low end is limited primarily by low-level distortion and the upper end is limited due to the voltage drive capabilities of the pre-amplifier. (A resistor can be added in the dc feedback loop, from pin 6 to ground, to increase this drive). The Overall Voltage Gain, then, is:

$$A_{VT} = \frac{R_f\ 10\ k}{R_s\ R_p}$$

2. Input Impedance

The Preamplifier Input Impedance is:

$$Z_{in\,A} \approx R_s$$

and the Power Amplifier Input Impedance is:

$$Z_{in\,B} \approx R_p$$

3. Frequency Response

The low frequency response is controlled by the cumulative effect of the series coupling capacitors C1, C2, and C3. High-frequency response can be determined by the feedback capacitor, C_f, and the −3.0 dB point occurs when

$$X_{C_f} = R_f$$

Additional high frequency roll-off and noise reduction can be achieved by placing a capacitor from the center point of R_p to ground as shown in Figure 10.

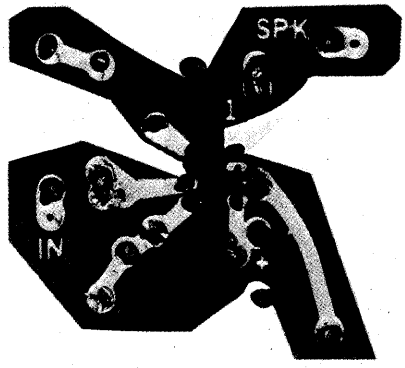
Capacitor C4 and the RC network shown in dotted lines may be needed to prevent high frequency parasitic oscillations. The RF choke, shown in series with the output, and capacitor C6 are used to prevent the high-frequency components in a large-signal clipped audio output waveform from radiating into the RF or IF sections of a radio (Figure 10).

4. Battery Operation

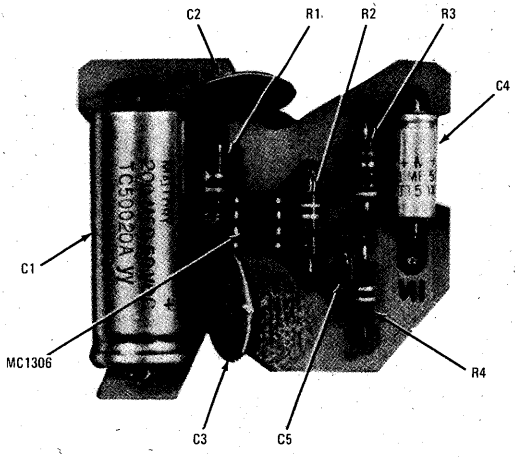
The increase of battery resistance with age has two undesirable effects on circuit performance. One effect is the increasing of amplifier distortion at low signal levels. This is readily corrected by increasing the size of the filter capacitor placed across the battery (as shown in Figure 8; a 300-μF filter capacitor gives distortions at low-tonal levels that are comparable to the "stiff" supply). The second effect of supply impedance is a lowering of power output capability for steady signals. This condition is not correctable, but is of questionable importance for music and voice signals.

5. Application Examples: (1) The audio section of the AM-FM radio (Figure 1) is adjusted for a preamplifier gain of 100 with an input impedance of 10-k ohms. The power amplifier gain is set at 10, which gives an overall voltage gain of 1000. The bandwidth has been set at 10-kHz. (2) The phono amplifier (Figure 2) is designed for a preamplifier gain of unity and a power amplifier gain of 10. The input impedance is 1.0-megohm. An adjustable treble control is provided within the feedback loop.

TYPICAL PRINTED CIRCUIT BOARD LAYOUT



LOCATION OF COMPONENTS



See Figure 3 for schematic diagram.

PARTS LIST

Component	Value
C1	200 μF
C2	0.1 μF
C3	0.05 μF
C4	1.0 μF
C5	47 pF
R1	1 ohm
R2	1 k ohm
R3	4.7 k ohms
R4	270 k ohms
MC1306	–
PC Board	–

ORDERING INFORMATION

Device	Temperature Range	Package
MC1310P	−40°C to +85°C	Plastic DIP

MC1310

Specifications and Applications Information

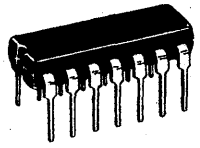
FM STEREO DEMODULATOR

. . . a monolithic device designed for use in solid-state stereo receivers.

- Requires no Inductors
- Low External Part Count
- Only Oscillator Frequency Adjustment Necessary
- Integral Stereo/Monaural Switch 75 mA Lamp Driving Capability
- Wide Dynamic Range: 0.5–2.8 V(p-p) Composite Input Signal
- Wide Supply Range: 8–14 Vdc
- Excellent Channel Separation Maintained Over Entire Audio Frequency Range
- Low Distortion: Typically 0.3% THD at 560 mV (RMS) Composite Input Signal
- Excellent SCA Rejection

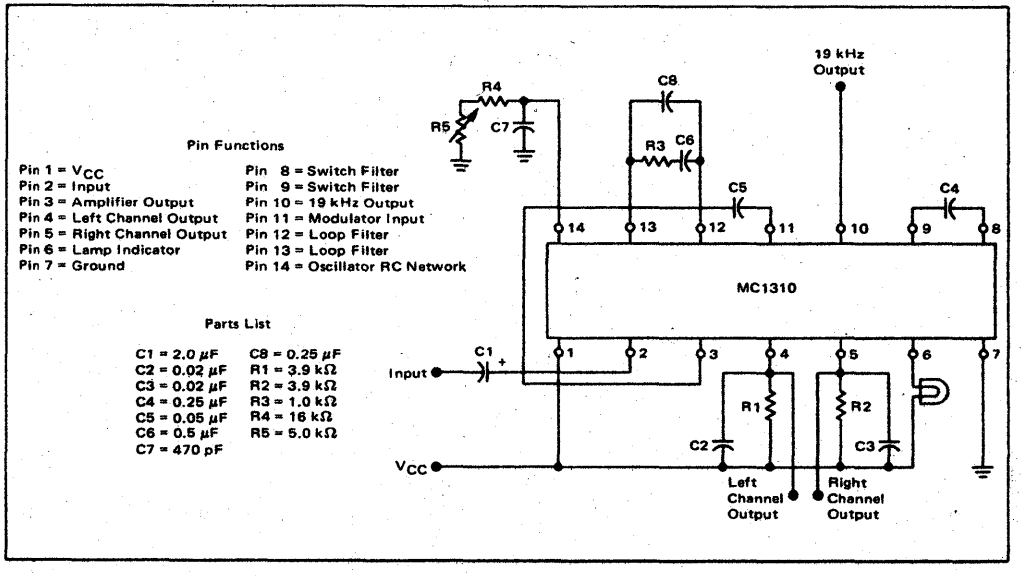
FM STEREO DEMODULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



CASE 646

FIGURE 1 – TYPICAL APPLICATION AND TEST CIRCUIT



MAXIMUM RATINGS (T_A = +25° unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	14	Volts
Lamp Current	75	mA
Power Dissipation (Package limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS Unless otherwise noted; V_{CC} = +12 Vdc, T_A = +25°C, 560 mV(RMS) (2.8 $V_{[p-p]}$) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 100 mV(RMS) pilot level (10%), using circuit of Figure 1.

Characteristic	Min	Typ	Max	Unit
Maximum Standard Composite Input Signal (0.5% THD)	2.8	–	–	$V_{(p-p)}$
Maximum Monaural Input Signal (1.0% THD)	2.8	–	–	$V_{(p-p)}$
Input Impedance	20	50	–	kΩ
Stereo Channel Separation	30	40	–	dB
Audio Output Voltage (desired channel)	–	485	–	mV(RMS)
Monaural Channel Balance (pilot tone "off")	–	–	1.5	dB
Total Harmonic Distortion	–	0.3	–	%
Ultrasonic Frequency Rejection 19 kHz 38 kHz	– –	34.4 45	– –	dB
Inherent SC A Rejection (f = 67 kHz; 9.0 kHz beat note measured with 1.0 kHz modulation "off")	–	75	–	dB
Stereo Switch Level 19 kHz input level for lamp "on" 19 kHz input level for lamp "off"	 – 5.0	 – –	 20 –	mV(RMS)
Capture Range (permissible tuning error of internal oscillator, reference circuit values of Figure 1)	–	±3.5	–	%
Current Drain (lamp "off")	–	13	–	mAdc

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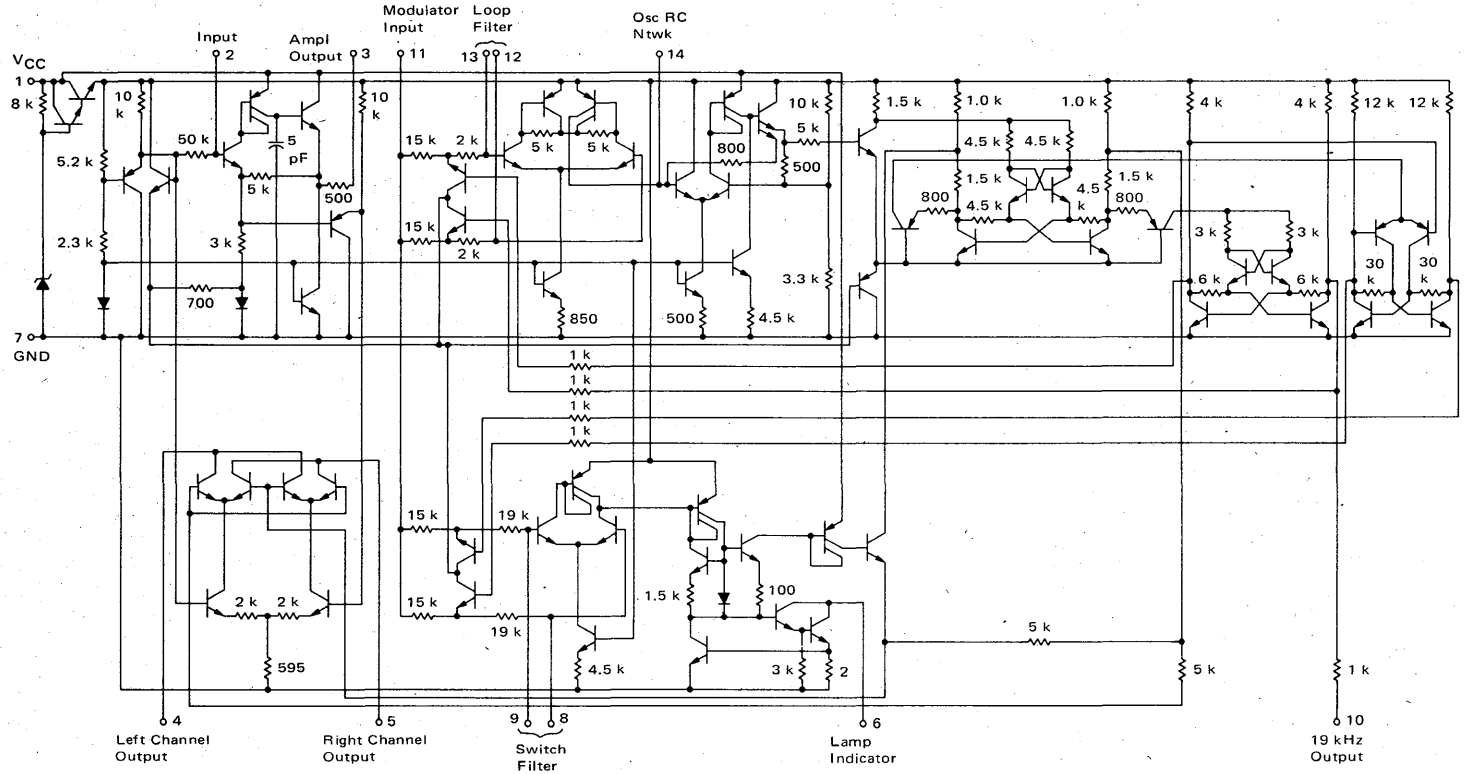
FIGURE 2 – CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

Unless otherwise noted: V_{CC} = +12 Vdc, T_A = +25°C; 560 mV(RMS) (2.8 $V_{[p-p]}$) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 100 mV(RMS) pilot level (10%), using circuit of Figure 1.

FIGURE 3 – CHANNEL SEPARATION versus COMPOSITE INPUT LEVEL

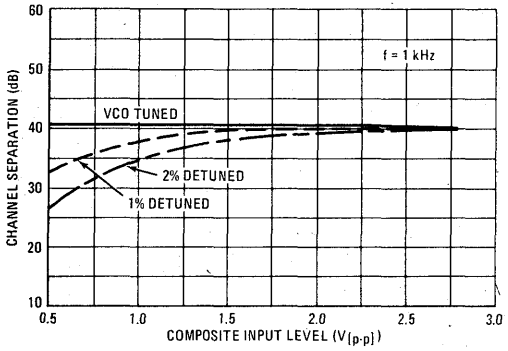


FIGURE 4 – CHANNEL SEPARATION versus FREQUENCY

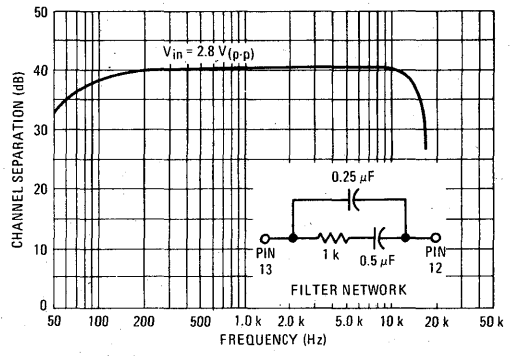


FIGURE 5 – CHANNEL SEPARATION versus VCO FREE-RUNNING FREQUENCY

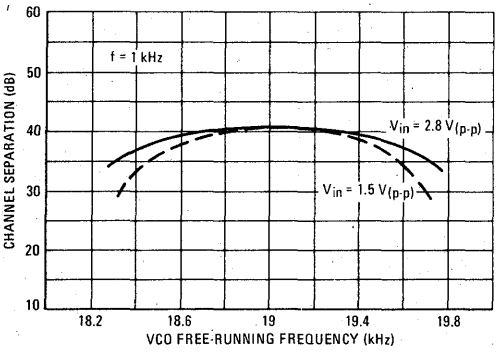


FIGURE 6 – CHANNEL SEPARATION versus SUPPLY VOLTAGE

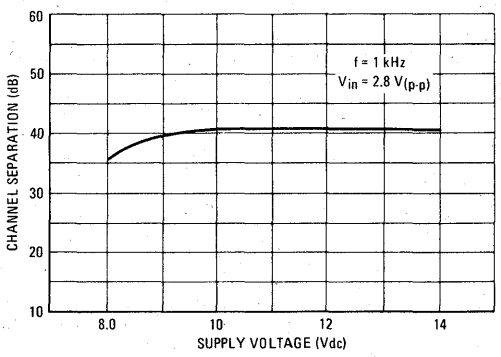


FIGURE 7 – THD versus COMPOSITE INPUT LEVEL*

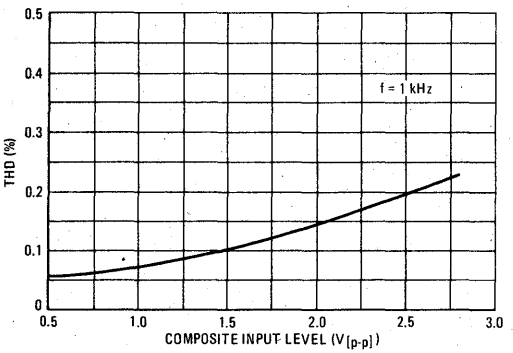
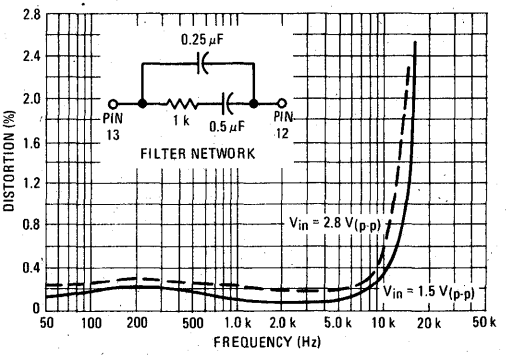


FIGURE 8 – DISTORTION versus FREQUENCY*



*Measured with Low Pass Filter (BW = 15 kHz).

7

TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – DISTORTION versus FREQUENCY*

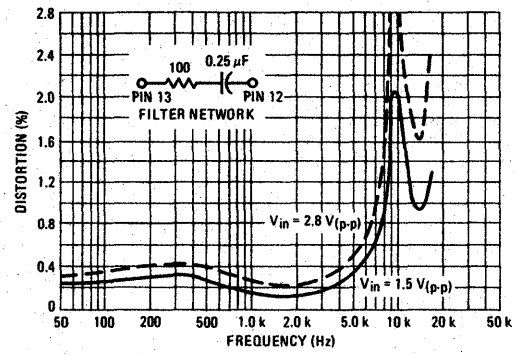


FIGURE 10 – VCO FREE-RUNNING FREQUENCY versus TEMPERATURE

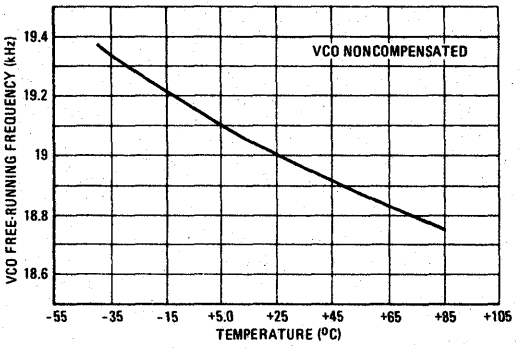
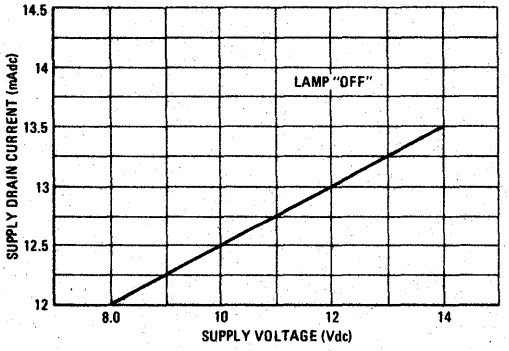


FIGURE 11 – CURRENT DRAIN versus SUPPLY VOLTAGE



*Measured with Low Pass Filter (BW = 15 kHz)

FIGURE 12 – PILOT LEVEL REQUIRED FOR VCO LOCKUP versus VCO FREE-RUNNING FREQUENCY

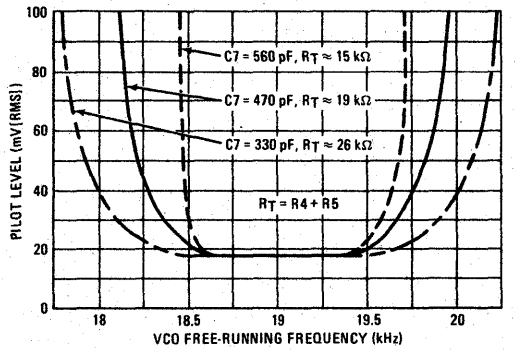
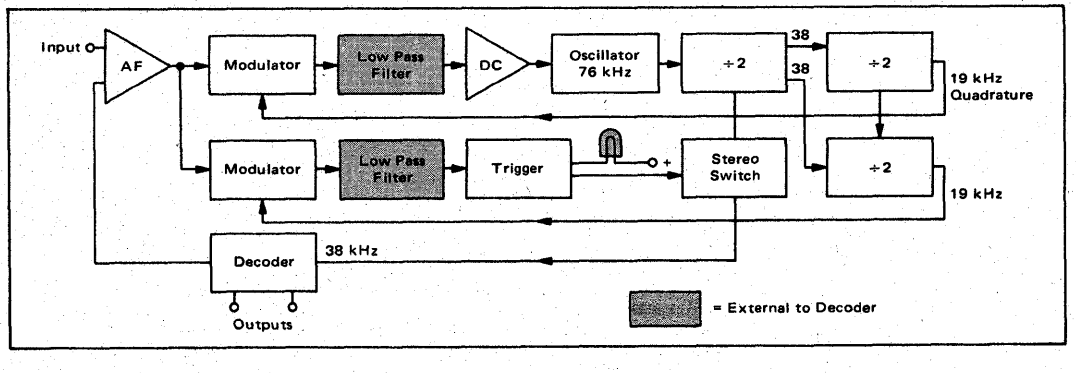


FIGURE 13 – SYSTEM BLOCK DIAGRAM



CIRCUIT OPERATION

Figure 13, on the previous page, shows the system block diagram. The upper line, comprising the 38-kHz regeneration loop operates as follows: the internal oscillator running at 76-kHz and feeding through two divider stages returns a 19-kHz signal to the input modulator. There the returned signal is multiplied with the incoming signal so that when a 19-kHz pilot tone is received a dc component is produced. The dc component is extracted by the low pass filter and used to control the frequency of the internal oscillator which consequently becomes phase-locked to the pilot tone. With the oscillator phase-locked to the pilot the 38-kHz output from the first divider is in the correct phase for decoding a stereo signal. The decoder is essentially another modulator in which the incoming signal is multiplied by the regenerated 38-kHz signal. The regenerated 38-kHz signal is fed to the stereo decoder via an internal switch, which closes when a sufficiently large 19 kHz pilot tone is received.

The 19-kHz signal returned to the 38-kHz regeneration loop modulator is in quadrature with the 19-kHz pilot tone when the loop is locked. With the third divider state appropriately connected, a 19-kHz signal in phase with the pilot tone is generated. This is multiplied with the incoming signal in the stereo switch modulator yielding a dc component proportional to the pilot tone amplitude. This component after filtering is applied to the trigger circuit which activates both the stereo switch and an indicator lamp.

APPLICATIONS INFORMATION

(Component numbers refer to Figure 1)

External Component Functions and Values

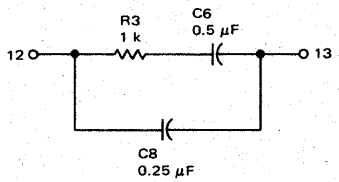
C1 — Input coupling capacitor; 2.0 μF is recommended but a lower value is permissible if reduced separation at low frequencies is acceptable.

R1, R2, C2, C3 — See Maximum Load Resistance section.

C4 — Filter capacitor for stereo switch level detector; time constant is C4 x 53 kilohms ±30%, maximum dc voltage appearing across C4 is 0.25 V (pin 8 positive) at 100 mV(RMS) pilot level. The signal voltage across C4 is negligible.

C5 — See Phase Compensation section.

R3, C6, C8 — Phase-locked loop filter components; the following network is recommended:



When less performance is required a simpler network consisting of R3 = 100 ohms and C6 = 0.25 μF may be used (omit C8). See Figure 9.

R4, R5, C7 — Oscillator timing network; recommended values:

C7 = 470 pF	1%
R4 = 16 kΩ	1%
R5 = 5 kΩ	Preset

These values give ±3.5% typical capture range. Capture range may be increased by reducing C7 and increasing R4, R5 proportionally but at the cost of increasing beat-note distortion (due to oscillator-phase jitter) at high-signal levels. See Figure 12.

Stereo Lamp — Nominal rating up to 75 mA at 12 V; the circuit includes surge limiting which restricts cold-lamp current to approximately 250 mA.

19-kHz Output — A buffer output providing a 3.0-V_{pk} square wave at 19 kHz is available at pin 10. A frequency counter may be connected to this point to measure the oscillator free-running frequency for alignment. See Alignment section.

External Monaural/Stereo Switching

If it is desired to maintain the circuit in monaural mode, the following procedure must be followed. First, the stereo switch must be disabled to prevent false lamp triggering. This can be accomplished by connecting pin 8 negative or pin 9 positive by 0.3 volt. Pin 8 may be grounded directly if desired. Note that the voltage across C4 increases to approximately 2 volts with pin 9 positive when pin 8 is grounded.

Second, the 76-kHz oscillator must be killed to prevent interference when on AM. This can be accomplished by connecting pin 14 to ground via a current limiting resistor (3.3 kilohms is recommended).

Phase Compensation/IF Roll-off Compensation

Phase-shifts in the circuit cause the regenerated 38-kHz sub-carrier to lead the original 38 kHz by approximately 2^{o}. The coupling capacitor C5 generates an

APPLICATIONS INFORMATION (continued)

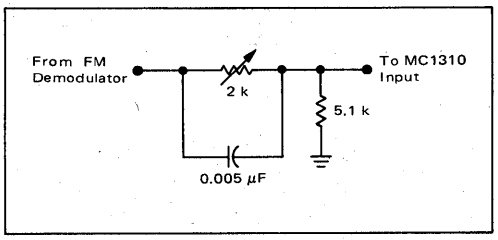
additional lead of 3.5° (for C5 = 0.05 μF) giving a total lead of 5.5°.

The circuit is so designed that phase lag may be generated by adding a capacitor from pin 3 to ground. The source resistance at this point is 500 ohms. A capacitance of 820 pF compensates the 5.5° phase lead: increase above this value causes the regenerated subcarrier to lag the original. However, a 5.5° phase error if left noncompensated will not degrade separation appreciably.

Note that these phase shifts occur within the phase-locked loop and affect only the regenerated 38-kHz sub-carrier: the circuit causes no significant phase or amplitude variation in the actual stereo signal prior to decoding.

Most IF amplifiers have a frequency response that limits separation to a value significantly lower than the capability of the MC1310. For example, if the response produces a 1-dB roll-off at 38 kHz, the separation will be limited to about 32 dB. This error can be compensated by using an RC lead network as shown in Figure 14. The exact values will be determined by the IF amplifier design. However, the values shown in Figure 14 are suitable for use with the MC1357 and MC1375 IF amplifiers.

FIGURE 14 – IF COMPENSATION NETWORK



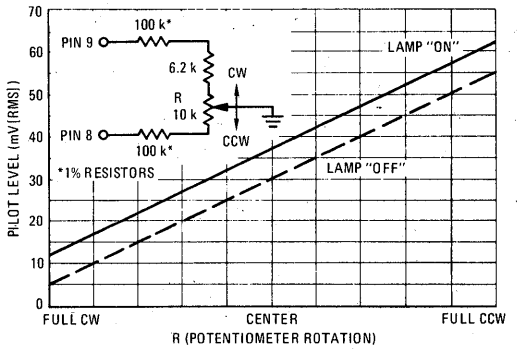
Voltage Control Oscillator Compensation

Figure 10 illustrates noncompensated Oscillator Drift versus temperature. The recommended T_C of the R4, R5, C7 combination is -300 PPM. This will hold the oscillator drift to approximately ±1% over a temperature range of -40 to +85°C. Allowing ±2% for aging of the timing components acceptable performance is still obtained.

Lamp Sensitivity

It may be desirable in some cases, to change the lamp sensitivity due to differing signal levels produced by various FM detectors. The lamp sensitivity can be changed by making use of the external circuit shown. Typical sensitivities versus potentiometer rotation are also shown in Figure 15.

FIGURE 15 – PILOT SENSITIVITY versus POTENTIOMETER ROTATION



Alignment Procedure

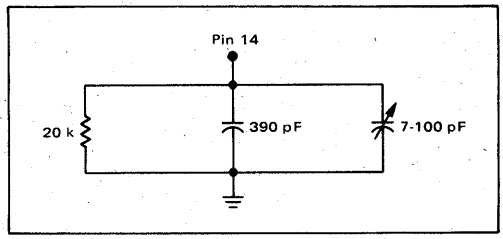
The optimum alignment procedure, with no input signal applied, is to adjust R5 until 19.00 kHz is read at pin 10 on the frequency counter.

Another procedure requiring no equipment, other than the receiver itself, will result in separation of within a few dB of optimum. This latter method is merely to tune the receiver to a stereo broadcast and adjust R5 until the pilot lamp turns "on". To find the center of the lock-in range, rotate the potentiometer back and forth until the center of the lamp "on" range is found. This completes the alignment.

Alternate Timing Network

The alternate timing network shown, incorporating a trimmer capacitor rather than a potentiometer, may be used if desired. Again, to provide correct temperature compensation, the temperature coefficient of the timing network must be approximately -300 PPM.

FIGURE 16

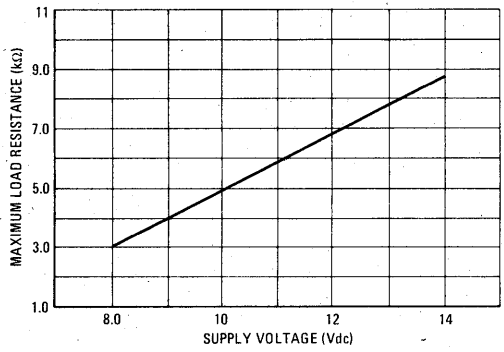


Maximum Load Resistance

The curve shown gives absolute maximum load resistance values versus supply voltage used for full-signal handling capability. With desired load resistance choose C2, C3 capacitors to provide standard 75 μs de-emphasis.

APPLICATIONS INFORMATION (continued)

FIGURE 17 – MAXIMUM LOAD RESISTANCE versus SUPPLY VOLTAGE



Audio Output

The ratio $G = \frac{\text{p-p audio output (one-channel)}}{\text{p-p input signal}}$ for different types of input is as follows:

	INPUT
Single-Channel Composite Signal	Monaural Signal
0.45	0.5

These figures are for 3.9-kilohm load resistors and for low-audio frequencies where de-emphasis roll-off is insignificant.

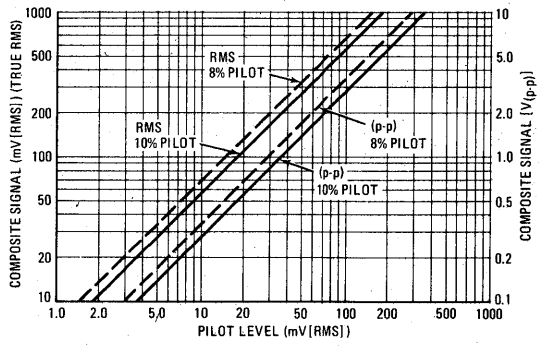
Capture Range versus Timing Components

The capture range can be changed to some extent by use of different timing components. Typical values are shown in Figure 12.

Composite Signal

Due to confusion concerning the measurement of the stereo composite signal, a curve showing both RMS and p-p composite levels versus pilot level follows, see Figure 18.

FIGURE 18 – COMPOSITE LEVEL versus PILOT (L or R Modulation Only)



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ORDERING INFORMATION

Device	Temperature Range	Package
MC1312P	0°C to +70°C	Plastic DIP
MC1314P	0°C to +70°C	Plastic DIP
MC1315P	0°C to +70°C	Plastic DIP

MC1312P
MC1314P
MC1315P

FOUR CHANNEL SQ LOGIC DECODER SYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT

CBS SQ* LOGIC DECODER SYSTEM

. . . a matrix system designed to decode SQ encoded program material into four separate channels. This system conforms to specifications for decoding quadraphonic records produced by the largest record companies in the world.

MC1312P - DECODER

. . . consists of two high input impedance preamplifiers which are fed with left total, L_T, and right total, R_T, signals. The preamplifiers each feed two all-phase networks which generate two L_T signals in quadrature and two R_T signals in quadrature. The four signals are matrixed to yield left front, left back, right front, and right back signals (L_F', L_B', R_F', R_B').

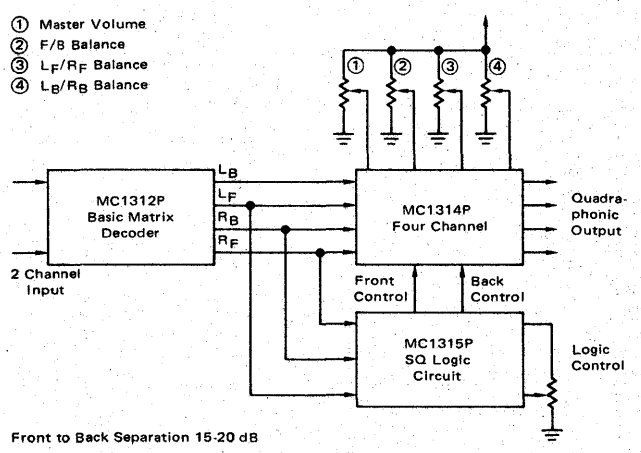
MC1314P - VOLTAGE CONTROLLED ATTENUATOR

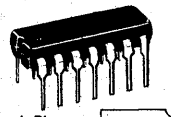
. . . a gain control and balance adjustment unit for use with any quadraphonic system. It has four channels whose gain can be varied by an external dc voltage. In addition, the relative gain between channels can be set by 3 external dc voltages. Thus with four variable resistors the master volume L_F/R_F, L_B/R_B and F/B balance may be controlled.

MC1315P - LOGIC CIRCUIT

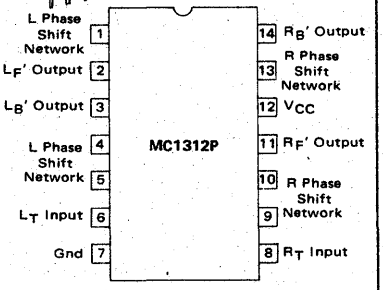
. . . provides the basic logic function to enhance the front to back separation in the CBS SQ four channel decoding system. This device is designed to interface with the MC1312 decoder and MC1314. The MC1315 provides dc logic enhancement control signals which extends the performance of the basic SQ system to the levels desired for top-of-the-line systems.

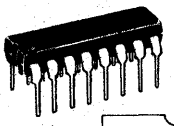
FIGURE 1 – SQ LOGIC DECODER SYSTEM



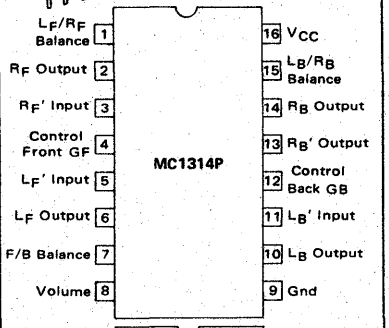


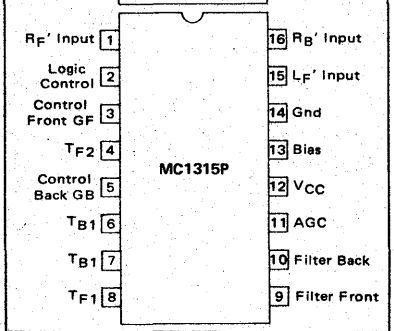
P SUFFIX
PLASTIC PACKAGE
CASE 646





P SUFFIX
PLASTIC PACKAGE
CASE 648





*Trademark of CBS Inc.

MC1312P • CBS SQ DECODER UNIT

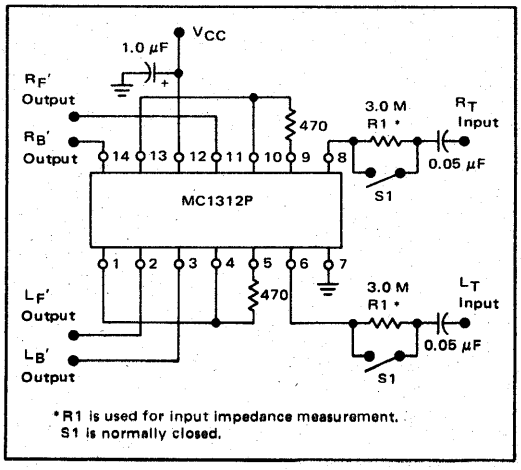
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	25	Vdc
Power Dissipation @ T_A = 25°C Derate above +25°C	750 6.7	mW mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, V_{in} = 0.5 V(RMS) @ 1 kHz, T_A = +25°C unless otherwise noted.)

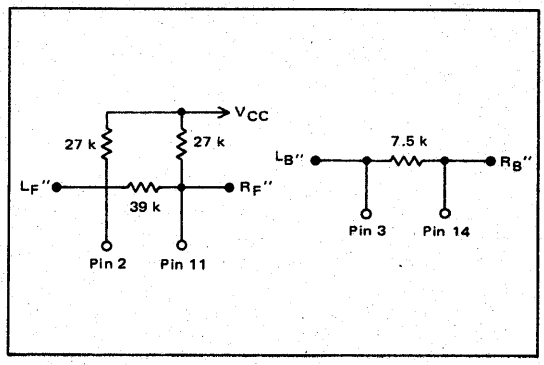
Characteristic	Min	Typ	Max	Unit
Supply Current Drain	11	16	21	mA
Input Impedance	1.8	3.0	–	MΩ
Output Impedance	–	5.0	–	kΩ
Channel Balance (L_F/R_F)	-1.0	0	+1.0	dB
Voltage Gain L_F/L_T or R_F/R_T	-1.0	0	+1.0	dB
Relative Voltage Gain L_B'/L_F', R_B'/L_F', L_B'/R_F', R_B'/R_F' L_F' measurements made with L_T input, R_F' measurements made with R_T input.	-2.0	-3.0	-4.0	dB
Maximum Input Voltage for 1%THD at Output R_T or L_T	2.0	–	–	V(RMS)
Total Harmonic Distortion R_T or L_T	–	0.1	–	%
Signal to Noise Ratio (Short-Circuit Input V_O = 0.5 V(RMS) with Output Noise Referenced to Output Voltage, V_O) (BW = 20 Hz to 20 kHz)	–	80	–	dB

FIGURE 2 – MC1312P TEST CIRCUIT



*R1 is used for input impedance measurement.
S1 is normally closed.

FIGURE 3 – EIA STANDARD BLEND

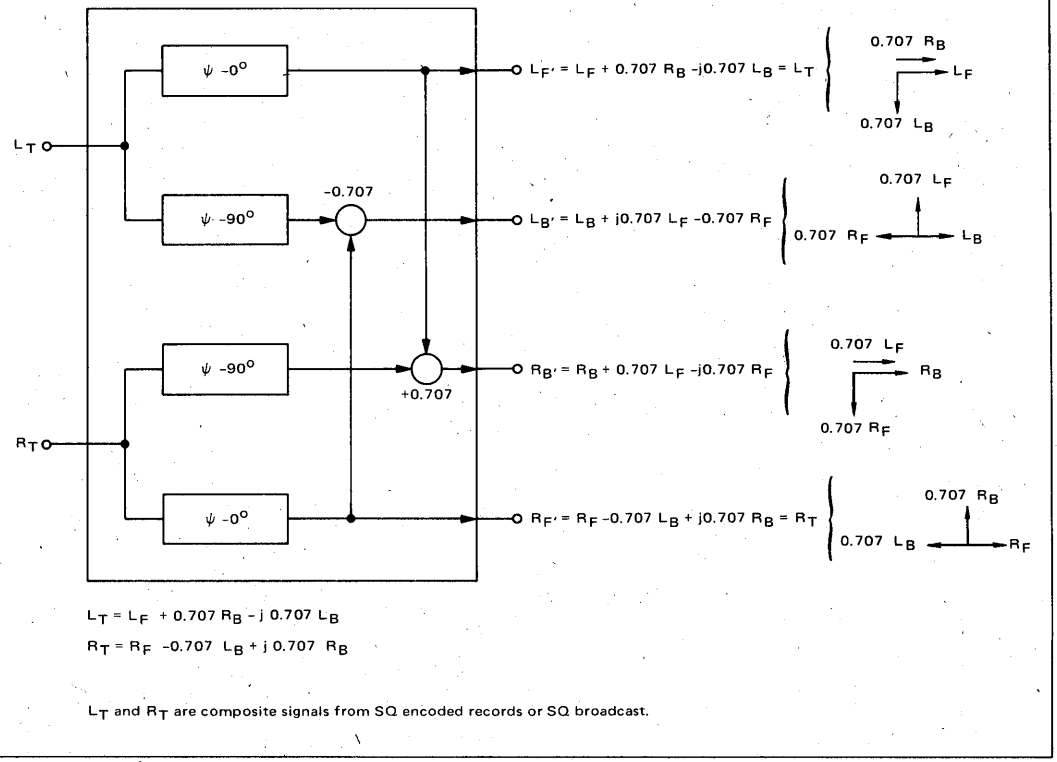


Note: In applications where tone arm pick-up is connected directly to the MC1312P inputs, a 300 k resistor should be inserted in series with R_T (Pin 8), and L_T (Pin 6) inputs.

MC1312P • CBS SQ DECODER UNIT

APPLICATIONS INFORMATION

FIGURE 4 – DECODING PROCESS DIAGRAM



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The decoding process is shown schematically in Figure 4. The MC1312P circuits that perform this function consists of two preamplifiers which are fed with left total, L_T, and right total, R_T, signals. The preamplifiers each feed two all-pass* networks that are used to generate two L_T signals in quadrature and two R_T signals in quadrature. The four signals are matrixed to yield left-front, left-back, right-front, and right-back signals (L_F', L_B', R_F', R_B').

The all-pass networks are of the Wein bridge form with the resistive arms realized in the integrated circuit and the RC arms formed by external components. The values shown in Figure 1 are for a 100-Hz to 10-kHz bandwidth and a phase ripple of ±8.5° on a 90° phase difference.

It is generally desirable to enhance center-front to center-back separation. This is accomplished by connecting a resistor between pins 2 and 11 (front outputs) and a resistor between pins 3 and 14 (back outputs). For a 10% front channel blending† and a 40% back channel blending†, 47 kilohms between pins 2 and 11 and 7.5 kilohms between pins 3 and 14 is required and results in the following equations:

$$^{\dagger}R_F'' = 0.912\ L_T + 0.088\ R_T$$
$$L_F'' = 0.912\ R_T + 0.088\ L_T$$
$$R_B'' = \frac{\sqrt{2}}{2}\left[0.714\ (JR_T - L_T) + 0.286\ (R_T - JL_T)\right]$$
$$L_B'' = \frac{\sqrt{2}}{2}\left[0.714\ (JL_T - R_T) + 0.286\ (L_T - JR_T)\right]$$

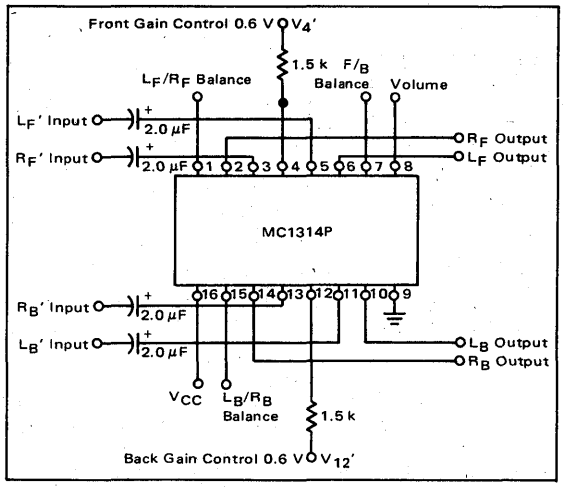
To meet the EIA matrix standards with 10/40 blend use the circuit of Figure 5, which results in the following equations:

$$R_F'' = 0.772\ (0.995\ R_T + 0.0972\ L_T)$$
$$L_F'' = 0.772\ (0.995\ L_T + 0.0972\ R_T)$$
$$R_B'' = \frac{\sqrt{2}}{2}\ (0.769)\ \left[0.928\ (JR_T - L_T) + 0.372\ (R_T - JL_T)\right]$$
$$L_B'' = \frac{\sqrt{2}}{2}\ (0.769)\ \left[0.928\ (JL_T - R_T) + 0.372\ (L_T - JR_T)\right]$$

*An all-pass network produces phase shift without amplitude variations.

MC1314P • GAIN CONTROL AND BALANCE ADJUSTMENT UNIT

FIGURE 5 – MC1314P TEST CIRCUIT



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	28	Vdc
Input Voltage Swing	±6.0	V_{pp}
Volume Control Range	-0.3 to +8.0	V
Balance Control Voltage	-4.0 to +10	V
Output Current Sinking (dc)	0	mA
Output Current Sourcing (dc)	1.0	mA
Power Dissipation @ T_A = +25°C Derate above +25°C	750 6.7	mW mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 V, $V_4' = V_{12}'$ = 0.60 Vdc, T_A = +25°C, V_{IN} = 1.0 V(rms) @ 1.0 kHz, balance control pins open, unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Maximum Gain (V_8 = 6 V)	-1.0	1.0	+3.0	dB
Minimum Gain (V_8 = 0 V)	-60	–	–	dB
Gain Spread @ Gain = Max	–	1.0	3.0	dB
@ Gain = -20 dB	–	–	3.0	dB
@ Gain = -40 dB	–	–	3.0	dB
Signal Handling (THD < 1%)	1.3	–	–	Vrms
Signal Handling ($V_4' = V_{12}'$ = 0.42 Vdc balance controls set for max gain in channel undertest) THD < 1%)	0.4	–	–	Vrms
Total Harmonic Distortion (V_{in} = 0.4 Vrms, max gain)	–	0.2	–	%
Signal/Noise Ratio (20 Hz - 15 kHz Bandwidth) Note 1. V_{IN} = 0.4 Vrms (ref)	–	80	–	dB
Channel Separation Note 2	–	60	–	dB
Balance Control Range – 20 dB gain V_8 = 6.0 V (≈Max Gain)	–	20	–	dB
V_8 = 3.0 V (≈ 6.0 dB Gain)	18	26	–	
V_8 = 1.0 V (≈ 20 dB Gain)	–	32	–	
Gain Enhancement ($V_4' = V_{12}'$ = 0.42 Vdc compared to $V_4' = V_8'$ = 0.60 Vdc)	2.0	–	4.0	dB
Gain Reduction ($V_4' = V_{12}'$ = 1.86 Vdc compared to $V_4' = V_{12}'$ = 0.60 Vdc)	7.0	–	11	dB
Gain Reduction ($V_4' = V_{12}'$ = 3.12 Vdc compared to $V_4' = V_{12}'$ = 0.60 Vdc, V_{CC} = 25 Vdc)	–	14	–	dB
Supply Current (max gain) (V_{IN} = 0 V)	–	19	25	mA
(min gain) (V_{IN} > 0 V)	–	9.0	15	mA
Input Impedance	–	13	–	kΩ
Output Impedance	–	2.0	–	kΩ
Control Current I_4 or I_{12}	–	-20	–	µA
Balance Control Reference Voltage (relative to V_{CC})				
L_F/R_F & L_B/R_B Controls (V_{1q}/V_{CC} & V_{15q}/V_{CC})	–	15	–	%
F/B Control (V_{7q}/V_{CC})	–	13	–	%
Intermodulation Distortion (f_1 = 7 kHz, f_2 = 60 Hz)	–	0.6	–	%

Note 1: All Inputs ac shorted
Note 2: Input to 3-Channels driven, 4th Channel open.

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MC1314P • TYPICAL CHARACTERISTICS

FIGURE 6 – ATTENUATION versus CONTROL VOLTAGE

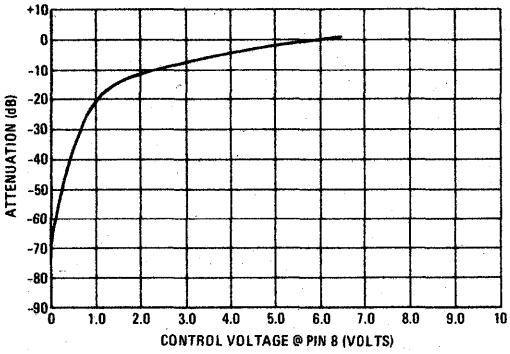
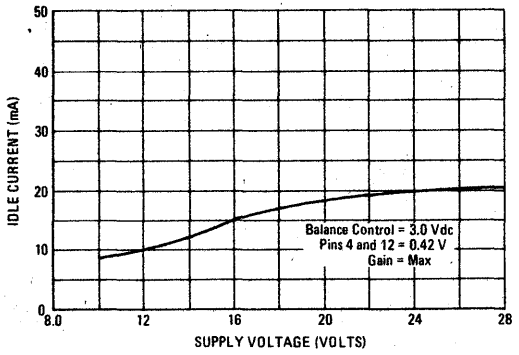


FIGURE 7 – IDLE CURRENT versus SUPPLY VOLTAGE



DISTORTION CHARACTERISTICS

FIGURE 8 – TOTAL HARMONIC DISTORTION versus ATTENUATION

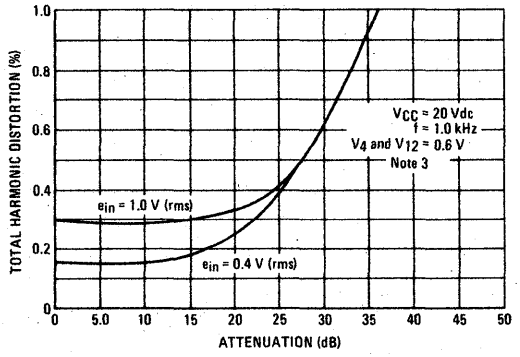


FIGURE 9 – INTERMODULATION DISTORTION versus INPUT VOLTAGE

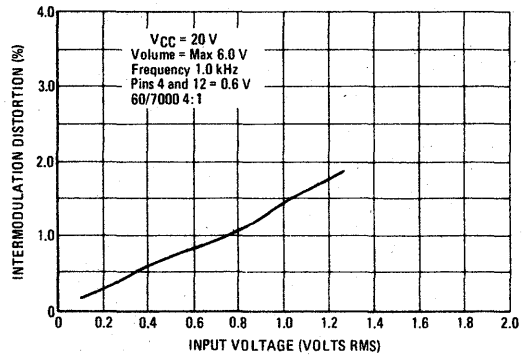


FIGURE 10 – TOTAL HARMONIC DISTORTION versus INPUT VOLTAGE

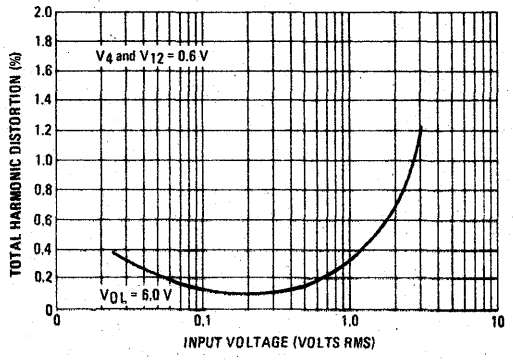
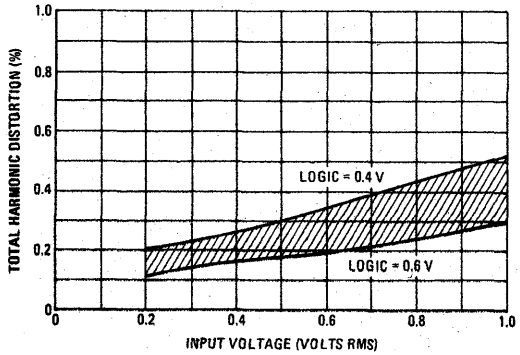


FIGURE 11 – LOGIC VOLTAGE EFFECTS ON TOTAL HARMONIC DISTORTION



Note 3: Major component of THD beyond 20 dB attenuation is noise.

MC1315P • DC LOGIC ENHANCEMENT CONTROL UNIT

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Supply Voltage (Note 1)	25	V
Input Signal Voltage	±4.0	Vpk
Bias Terminal Current	±2.0	mA
Output Current	±2.0	mA
Power Dissipation @ T_A = 25°C Derate above +25°C	750 6.7	mW mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 20 Vdc, Logic Control = 50%, V_{IN} = 0.5 Vrms, f = 2.0 kHz, unless otherwise noted, Note 1).

Characteristic	Min	Typ	Max	Unit
Supply Current (Pin 12) @ V_{IN} = 0	–	7.0	13	mA
@ V_{IN} = 1.4 Vrms	–	15	–	mA
Input Resistance @ Pin 1, 15, 16	–	20	–	kΩ
Output Resistance @ Pin 3, 5	–	1.5	–	kΩ
Paraphase Filter Resistance @ Pin 9, 10	–	4.0	–	kΩ
Front-Back Logic Discharge Resistance @ Pin 7, 8	–	5.0	–	kΩ
Bias Voltage (10 k to ground) @ Pin 13	–	1.4	–	Vdc
Logic Control Input Current @ Pin 2 ($V_2 = V_{13}$ or V_2 = 0)	–	±0.5	–	mA
Quiescent Input Voltage (V_{IN} = 0) @ Pin 1, 15, 16	–	7.0	–	Vdc
Quiescent Output Voltage (V_{IN} = 0)	0.48	–	0.72	Vdc
Quiescent Output Offset (V_{IN} = 0)	–	±0.02	±0.1	Vdc
Relative Output Change				
Front output with L_B or R_B inputs or back output with L_F or R_F inputs	2.1 7.5	2.8 9.0	5.0 14	V/V dB
Back output with C_F input	1.9 5.5	2.5 8.0	3.5 11	V/V dB
Front output with L_F, C_F or R_F inputs or back output with L_B, or R_B input	0.8 2.2	0.67 3.5	0.56 5.0	V/V dB
AGC Leveling - V_{IN} = 1.4 Vrms to V_{IN} = 50 mVrms (Note 2) Figure 8 (AGC1, AGC2)	–	1.0	3.0	dB
Quiescent Output Voltage at Max Logic (S_1 in Position 1, Figure 12) (V_{IN} = 0, $V_2 = V_{13}$)	0.45	–	0.83	Vdc
Max Logic Relative Output Change ($V_2 = V_{13}$)				
Front output with L_B or R_B inputs or back outputs with L_F, C_F or R_F inputs	– –	5.0 14	– –	V/V dB
Front output with L_F, C_F or R_F inputs or back outputs with L_B or R_B inputs	– –	0.67 3.5	– –	V/V dB

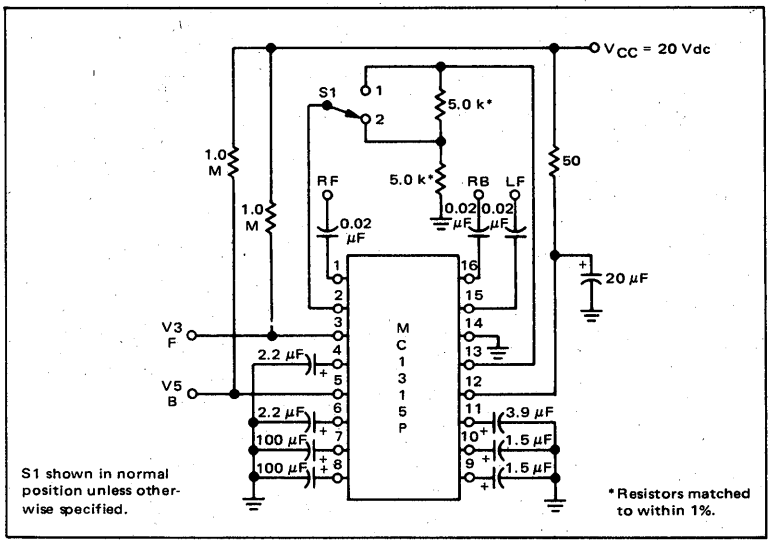
Note 1: When testing with well regulated supplies, current should be limited to 25 mA.

Note 2: For example, this is the decrease in the back control voltage, V_5 with a right front input signal as this signal is varied from 1.4 Vrms to 50 mVrms.

7

MC1315P • DC LOGIC ENHANCEMENT CONTROL UNIT

FIGURE 12 – MC1315P TEST CIRCUIT



7

TABLE 1 – DEFINITION OF INPUT SIGNALS: (f = 2.0 kHz)

V_I Name	Signal Description	Apply To Pin	V_I Name	Signal Description	Apply To Pin
RF	0.5 V rms /0° 0.35 V rms /−90° (1)	1 16 15	CF	0.35 V rms /0° 0.35 V rms /−45° 0.35 V rms /0°	1 16 15
LF	(1) 0.35 V rms /0° 0.5 V rms /0°	1 16 15			
LB	0.35 V rms /180° (1) 0.35 V rms /−90°	1 16 15	AGC1	(1) 1.0 V rms /−90° 1.4 V rms /0°	15 16 1
RB	0.35 V rms /90° 0.5 V rms /0° 0.35 V rms /0°	1 16 15	AGC2	(1) 35 mV rms /−90° 50 mV rms /0°	15 16 1

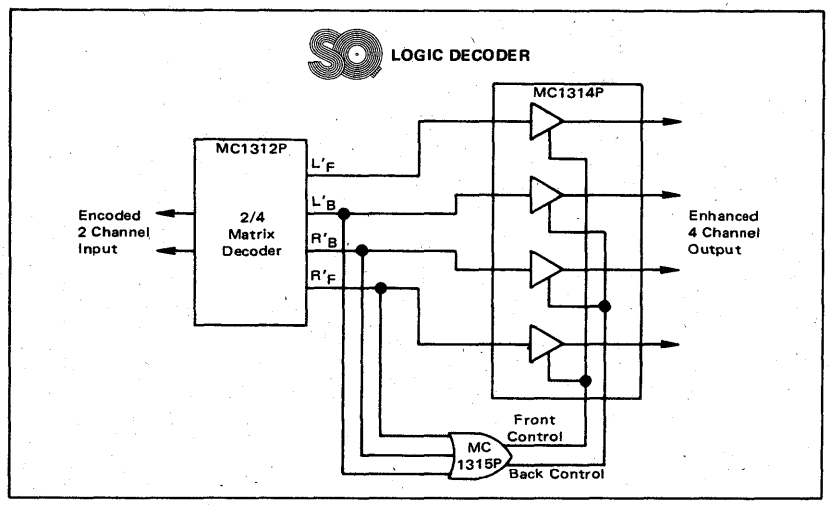
(1) All unused inputs shall be ac grounded.
(2) This signal not used at present.

MC1315P • DC LOGIC ENHANCEMENT CONTROL UNIT

WHY LOGIC?

Enhances front to back separation from 6 dB to 20 dB.

Front-to-back separation of SQ material can be enhanced by the MC1315 logic circuit which detects the presence of dominant front or back signals and adjusts the front-back gain relationship of the MC1314P to enhance the relative gain of the dominant channels.



Front and back control voltages (from the MC1315P) are connected to the MC1314P. Although the relative gains of the front and back channels are altered with these control signals, they vary in a complementary manner to maintain constant power output from the MC1314P.

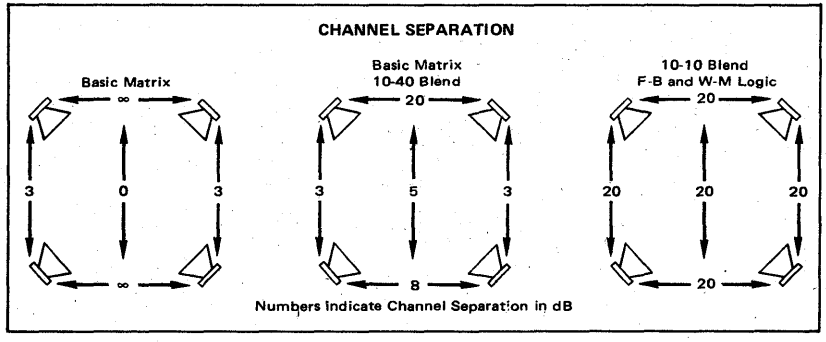
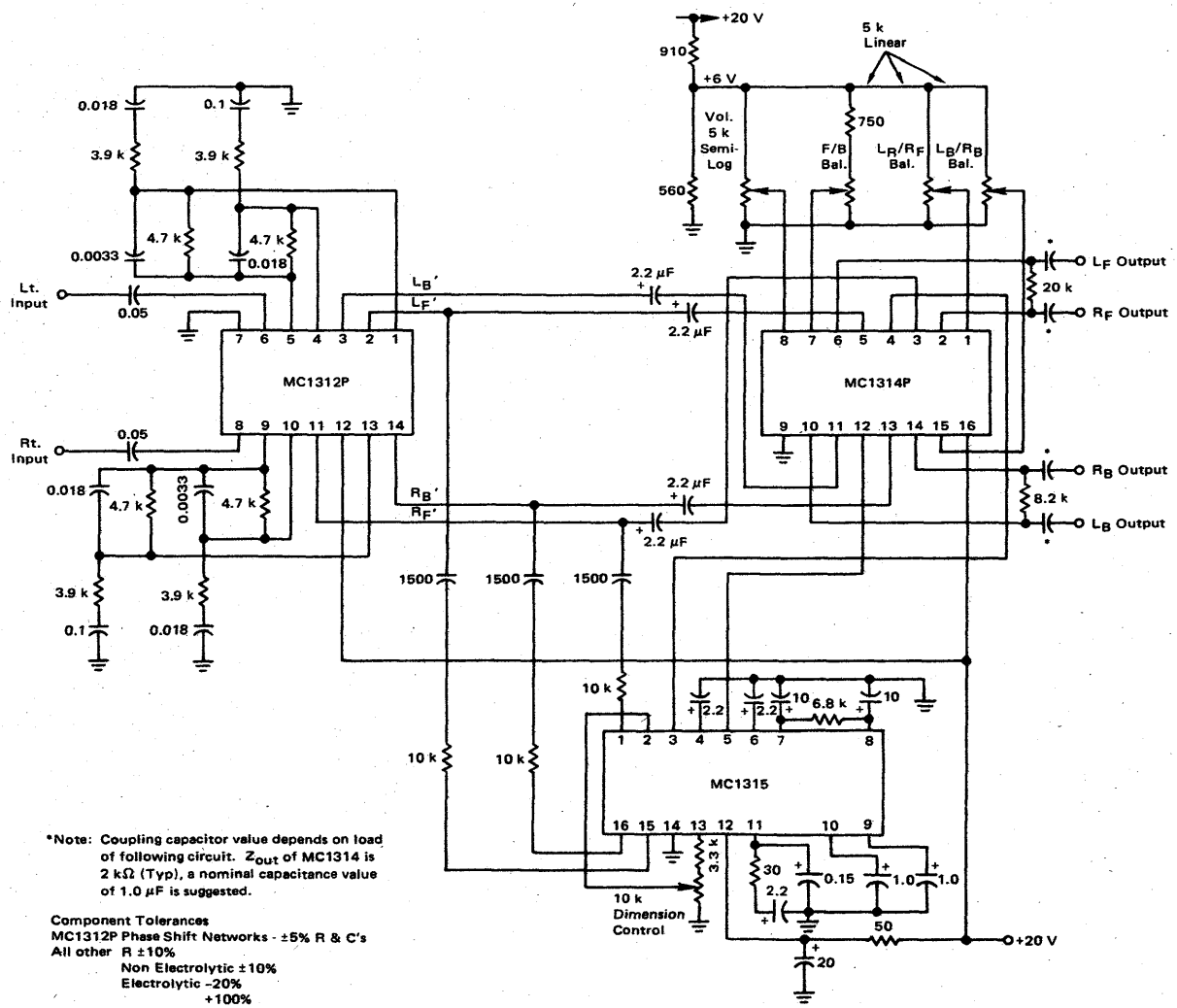


FIGURE 13 – CBS SQ LOGIC SYSTEM (L1a)

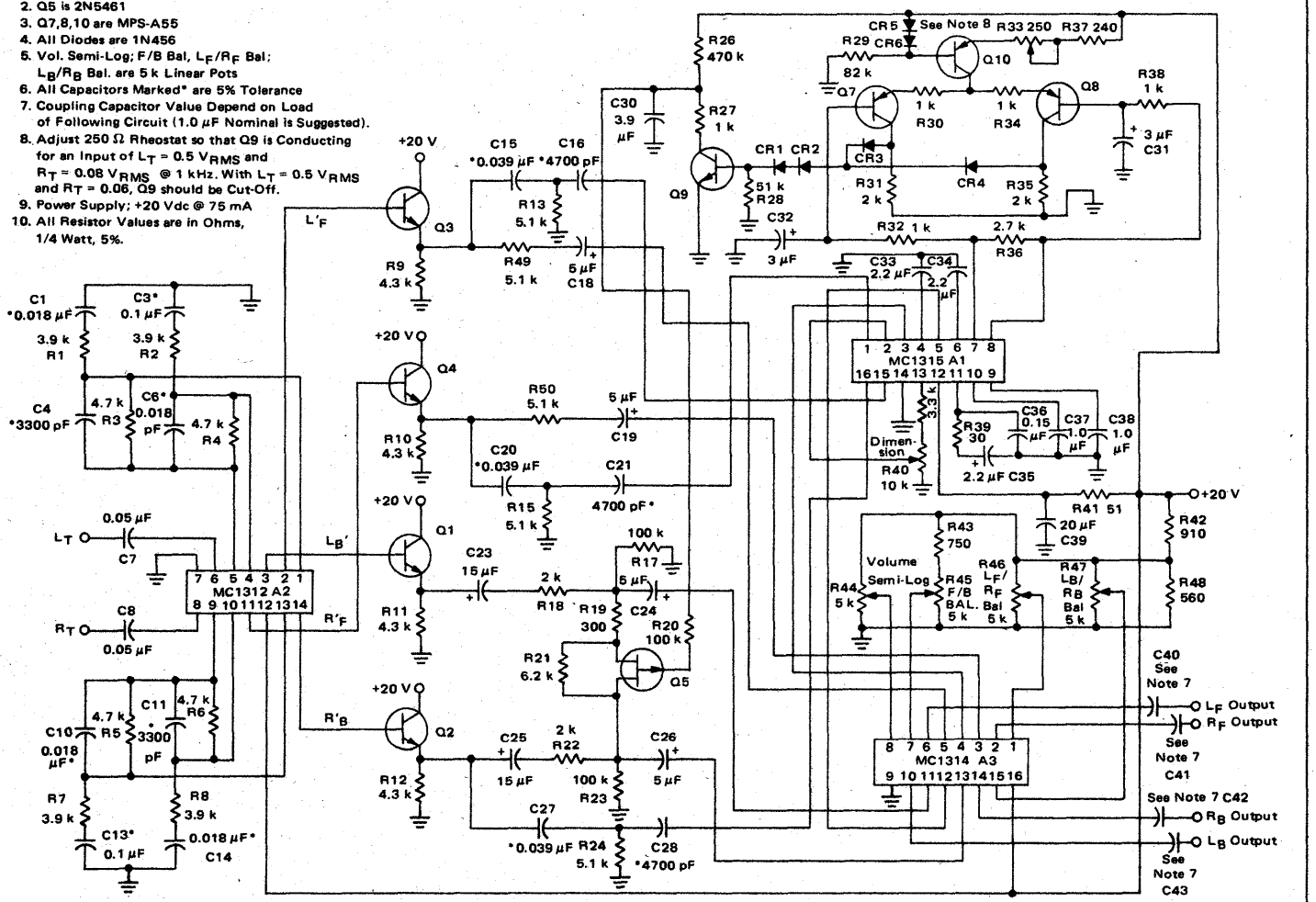


*Note: Coupling capacitor value depends on load of following circuit. Z_{out} of MC1314 is 2 kΩ (Typ), a nominal capacitance value of 1.0 μF is suggested.

Component Tolerances
MC1312P Phase Shift Networks - ±5% R & C's
All other R ±10%
Non Electrolytic ±10%
Electrolytic -20%
+100%

NOTES: (Unless otherwise specified)
1. Q1,2,3,4,9 are MPS-A18
2. Q5 is 2N5461
3. Q7,8,10 are MPS-A55
4. All Diodes are 1N456
5. Vol. Semi-Log; F/B Bal, L_F/R_F Bal; L_B/R_B Bal. are 5 k Linear Pots
6. All Capacitors Marked* are 5% Tolerance
7. Coupling Capacitor Value Depend on Load of Following Circuit (1.0 μF Nominal is Suggested).
8. Adjust 250 Ω Rheostat so that Q9 is Conducting for an Input of L_T = 0.5 V_{RMS} and R_T = 0.08 V_{RMS} @ 1 kHz. With L_T = 0.5 V_{RMS} and R_T = 0.06, Q9 should be Cut-Off.
9. Power Supply; +20 Vdc @ 75 mA
10. All Resistor Values are in Ohms, 1/4 Watt, 5%.

FIGURE 14 – CBS LOGIC SYSTEM WITH VARIABLE BLEND (L2a)



TYPICAL SYSTEM PERFORMANCE CHARACTERISTICS (MC1312P, MC1314P, MC1315P)

Power Supply Requirements:	60 mA (L1a), 75 mA (L2a) @ 20 V
Nominal Signal Level:	0.5 V
Maximum Input Voltage:	1.9 V
Input Impedance:	2 MΩ
Output Impedance:	2 kΩ
Total Harmonic Distortion:	0.2% at nominal input
at 1 Hz	1.0% at maximum input
Voltage Gain (at quiescent):	1.0
4 Channel Volume Control	Range - 70 dB
	Tracking - within 3 dB
4 Channel Balance Control:	-35 dB at -20 dB gain

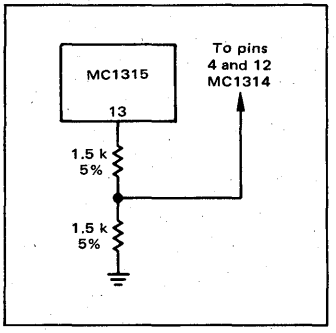
NOTES

MC1314P

1. If volume control is not used, connect Pin 8 to +6.0 V.
2. If balance controls are not used, open Pins 1, 7 and 15.
3. L_F/R_F and L_B/R_B balance controls can be ganged by connecting Pins 1 and 15.
4. Signal handling capability is reduced at maximum logic (20 dB front to back separation) unless V_{CC} = 25 V on MC1314.

MC1315P

1. The logic control will provide enhancement of front to back separation from 6 dB typical to 20 dB max (15 dB typical at the recommended operating level of 50% control).
2. To defeat the logic use the circuit connections as shown on right.



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SYSTEM CHARACTERISTICS

FIGURE 15 – GAIN versus F/B BALANCE

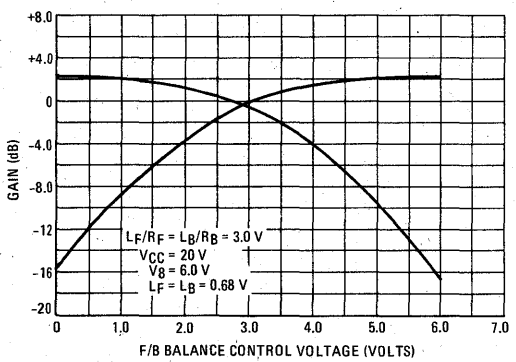
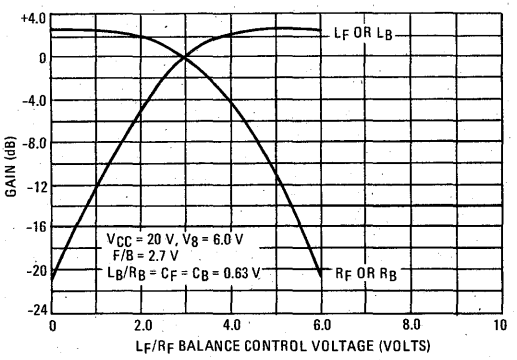


FIGURE 16 – GAIN versus L_F/R_F BALANCE CONTROL



Signal Definitions for Total System

Test signals shall have the following relative phase and amplitude characteristics.

Source Location	Input Signals	
	L_T	R_T
L_F	1	0
C_F	.71	.71
R_F	0	1
L_B	$.71/-90^o$	$.71/180^o$
R_B	.71	$.71/90^o$

Where L_F is left front, R_B is right back, C_F is center front, etc.

1. System Tests: MC1312P, MC1314P, MC1315P
   a) L_F source - connect signal to L_T input, ac ground R_T input of MC1312P.
   b) R_F source - apply signal to R_T, ac ground L_T.
   c) C_F source - apply equal signals to L_T and R_T inputs.

   NOTES: Balance control inputs of MC1314 may be opened for convenience or set for perfect balance with C_F and C_B inputs; set logic control to 50%: Max signal should be limited to 1.6 Vrms L_T or R_T: MC1314P outputs give system performance, typically 15 dB front back separation for corners, 12 dB for center front, center back.

2. Logic Circuit Tests: MC1315P
   a) L_F source - apply $L_F' = \sqrt{2}\,R_B'$, $R_F' = 0$; dc voltage at Pin 3 should decrease by 3 dB, at Pin 5 should increase by 9 dB.
   b) R_B source - apply $R_F' = \sqrt{2}\,R_B'$, $R_F' = 0$; dc voltage at Pin 3 should increase by 9 dB, at Pin 5 should decrease by 3 dB.

3. Voltage Controlled Amplifier Tests: MC1314P
   a) Volume control - with balance controls open or balanced, gain should be +0.5 dB at 6 V on Pin 8 and less than -60 dB at 0 V.
   b) Balance controls - with balance controls at Pins 1 and 15 at 15% of supply and Pin 7 at 13% of supply, system is nominally balanced. Taking Pin 1 to ground should increase L_F gain by 3 dB and decrease R_F gain by greater than 12 dB at maximum volume and 30 dB at lower volume levels.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1323P	0°C to +75°C	Plastic DIP
MC1323PW	0°C to +75°C	Heat Spreader Plastic DIP

MC1323P
MC1323PW

TRIPLE DOUBLY BALANCED CHROMA DEMODULATOR WITH ADJUSTABLE OUTPUT MATRIX

. . . designed for use in solid-state color television receivers. May be used in any conventional color picture tube application.

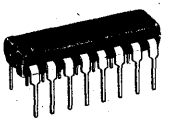
For next generation single-gun color picture tube applications, the MC1323P/PW features three independent demodulators with each gain adjustable with no change to dc output levels.

The MC1323PW package is suited for higher power, higher ambient temperature applications.

- Low Differential Output DC Offset Voltage – < 500 mV (Max)
- Complete Freedom in Choice of Demodulation Axes
- High Blue Output Voltage Swing – 10 V(p-p) (Typ)
- Guaranteed Chroma Sensitivity – 450 mV(p-p) (Max)
- Brightness Input Provided
- Blanking Input Provided
- Circuit Regulated – 16 to 22 V Operating Window
- Power Dissipation @ T_A = 25°C – P_D = 2.2 W – MC1323PW = 1.25 W – MC1323P

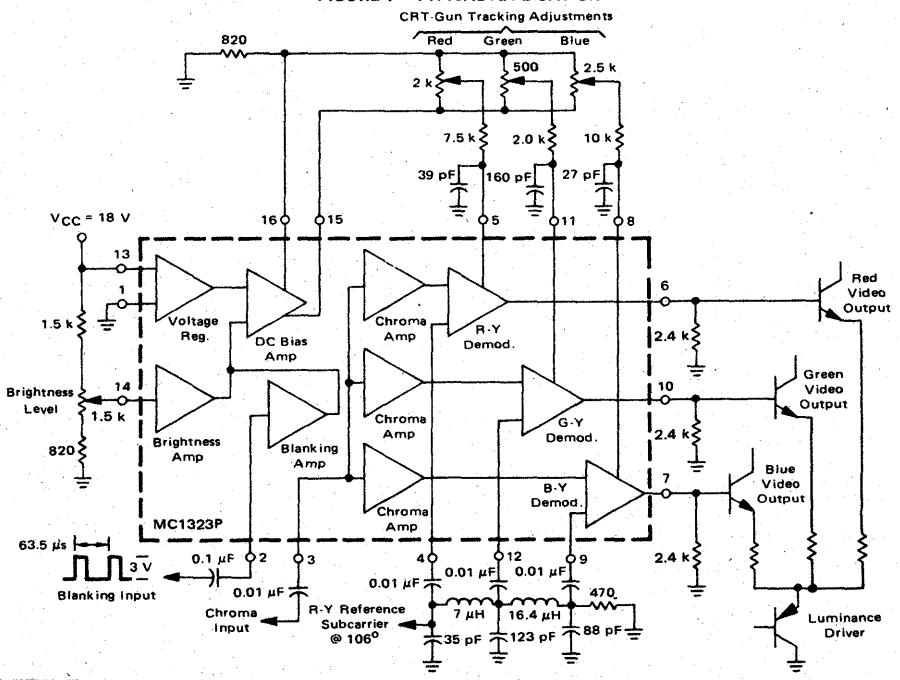
TRIPLE DOUBLY BALANCED CHROMA DEMODULATOR WITH ADJUSTABLE OUTPUT MATRIX

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 648

FIGURE 1 – TYPICAL APPLICATION



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	MC1323P	MC1323PW	Unit
Power Supply Voltage	22		Vdc
Blanking Signal Input Voltage	6.0		V(p-p)
Minimum Load Resistance (Pins 6,7,10)	2.2		kΩ
Brightness Input Range – Max Min	10.7 4.5		Vdc
Operating Ambient Temperature Range	0 to +75		°C
Storage Temperature Range	-65 to +150		°C
Power Dissipation @ T_A = 25°C Derate above +25°C	1.25 10	2.2 17	W mW/°C

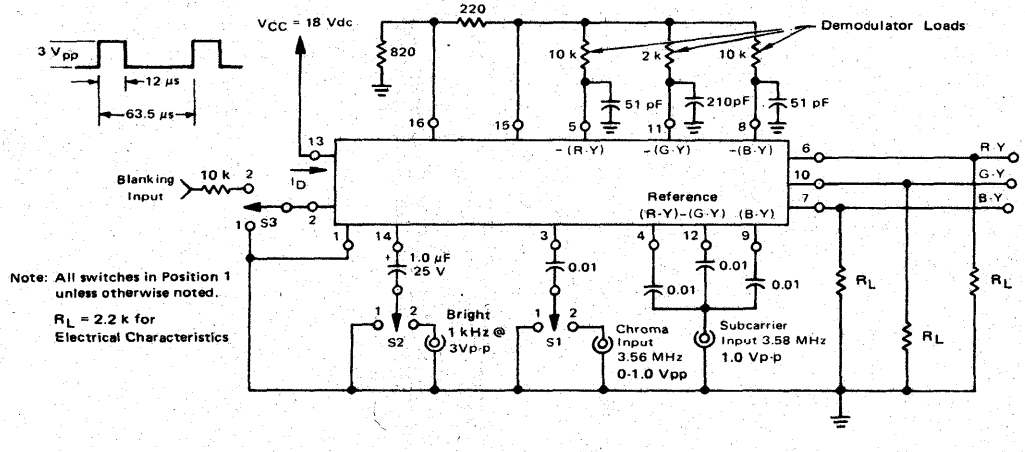
THERMAL CHARACTERISTICS

Characteristic	Max	Unit
Thermal Resistance, Junction to Ambient MC1323PW	59	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = +18 Vdc, R_L = 2.2 kΩ, V_{REF} = 1.0 V(p-p), T_A = +25°C unless otherwise noted.)

Characteristic	Pin No.	Min	Typ	Max	Unit
STATIC CHARACTERISTICS (Figure 2) S1, S2, and S3 in Position 1)					
Quiescent Input Current From Supply	13	–	37	–	mA
Quiescent Output Voltage	6,7,10	9.8	10.8	11.8	Vdc
Differential Output Voltage	6-7,7-10,6-10	–	200	500	mVdc
Differential Voltage	15,16	1.5	1.65	–	Vdc
Pin 15 Output Voltage	15	10.6	11.3	12	Vdc
DYNAMIC CHARACTERISTICS (Figure 2)					
Chroma Input Voltage (Pin 6 Output = 5 V(p-p) S1 in Position 2)	3	–	0.35	0.45	V(p-p)
Detected Output Voltage (Pin 6 Output = 5 V(p-p) S1 in Position 2	7 10	4.6 0.92	5.0 1.0	5.4 1.08	V(p-p) V(p-p)
Blanking Output Voltage (S3 in Position 2)	6,7,10	5.2	5.4	5.6	V(p-p)
Maximum Output Voltage Swing (S1 in Position 2)	6	–	10	–	V(p-p)
Brightness Output Swing (S2 in Position 2)	6,7,10	2.9	–	–	V(p-p)

FIGURE 2 – TEST CIRCUIT WITH REFERENCE INPUT SIGNAL
(Quiescent Current, DC Output Voltage, Difference Voltage)



CIRCUIT DESCRIPTION

The MC1323P is a doubly balanced chroma demodulator that offers several novel features. Three separate independent demodulator sections are used to obtain the (R-Y), (B-Y) and (G-Y) outputs allowing complete freedom in the choice of demodulation axes and individual demodulator conversion gain.

The (R-Y) demodulator is shown in Figure 10 (both (B-Y) and (G-Y) are similar), and is a conventional doubly balanced circuit. The chroma input, which is common to all three demodulators, is applied at Pin 3 to the balanced pair Q15, Q16, which are evenly dividing the 1 mA bias current from the current source Q14. The upper switching pairs Q17, Q18, Q19 and Q20 are driven with approximately 1 Vpp of reference subcarrier applied at Pin 4. If the subcarrier at Pin 4 has a relative angle of 109°, then the output from the switching pairs will be the desired (R-Y) signal. Similarly, for the (B-Y) demodulator, the reference phase at Pin 9 is approximately 3°. To avoid unnecessarily wide phase shift networks to provide the 256° reference phase for the (G-Y) demodulator, the chroma input is phase reversed and the reference angle becomes 76° at Pin 12.

The demodulator is unique in the manner in which the demodulated signals are connected to the output pins. Instead of feeding load resistors returned to the supply voltage rail, the collectors of Q17, Q19 are coupled to the current mirror Q21, Q22, Q23. At balance, with no chroma input signal, Q17, Q19 current (mirrored in Q23) matches Q18, Q20 and the net current at Pin 5 is zero. If a load resistor is connected from Pin 5 to some convenient voltage source, the base of Q25 will be at that voltage regardless of the size of load resistor. Therefore, the conversion gain of the demodulator (defined by the size of the resistor at Pin 5) can be easily changed, yet changes in gain do not result in a change of the dc voltage level at the demodulator output (Pin 6). The ability to change gain, together with a complete choice of demodulation axes, allows the designer to compensate for non-standard CRT phosphors, different color temperatures, and allows easy implementation of automatic hue or color level control circuits.

In order to provide temperature stability of the output dc levels, a reference voltage for the load resistors (Pins 5, 8, and 11) is supplied at Pin 15 with a nominally zero TC. Since the demodulator output dc levels are defined by the voltage source to which the load resistors are returned, another voltage source is provided at Pin 16 and is approximately 1.5 volts lower than Pin 15. Returning the load resistors to the wiper arms of potentiometers connected between Pins 15 and 16 will allow the output dc level of each demodulator to be changed independently over a 1.5 V range. If the potentiometers have a comparatively low resistance compared to the load resistors, negligible change in ac gain will occur with wiper arm rotation and the dc shift can be used to help set up the picture tube grey scale tracking. The voltage source at Pin 16 is obtained by providing a temperature compensated current in Q5 emitter load. This current is "mirrored" in Q8, producing the 1.5 V difference between the bases of Q11 and Q12.

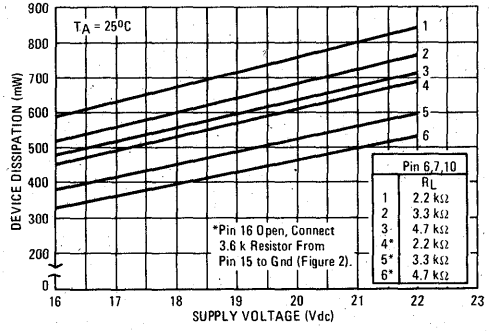
The brightness input at Pin 14 allows the dc output level of all three demodulators to be changed and is a convenient point for a brightness control or brightness range/brightness limiter function.

Output blanking during retrace is achieved by applying a +3 V pulse at Pin 2 (Q13 base). The outputs become clamped to Q2 emitter voltage preventing the demodulator upper pairs from becoming saturated during blanking and giving a very well defined blanking pulse amplitude.

TYPICAL DESIGN CHARACTERISTICS (V_{CC} = +18 Vdc, R_L = 2.2 kΩ, V_{REF} = 1.0 V(p-p), T_A = +25°C)

Characteristic	Pin No.	Min	Typ	Max	Unit
Output Voltage Temperature Coefficient (Reference Input Voltage = 1.0 V(p-p), T_A = +25 to +75°C)	6,7,10	–	1.5	–	mV/°C
Chroma Input Voltage	3	–	1.8	–	Vdc
Reference Input Voltage	4,9,12	–	3.2	–	Vdc
Brightness Input Voltage	14	–	9.2	–	Vdc
Differential Blanking Output Voltage (S3 in Position 2)	6-7,7-10,6-10	–	200	–	mV(p-p)

FIGURE 3 – POWER DISSIPATION CHARACTERISTICS



TYPICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted. Refer to Figure 2 except where noted.)

FIGURE 4 – DEMODULATOR GAIN LINEARITY AND TOTAL HARMONIC DISTORTION CHARACTERISTICS

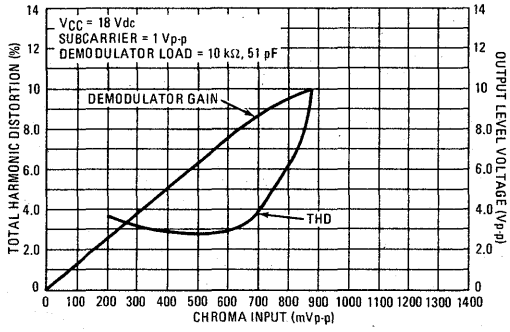


FIGURE 5 – CHROMA BANDWIDTH

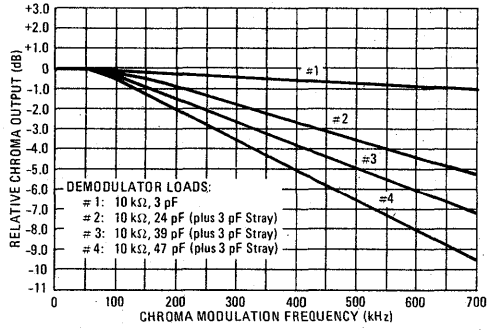


FIGURE 6 – DETECTED OUTPUT VOLTAGE

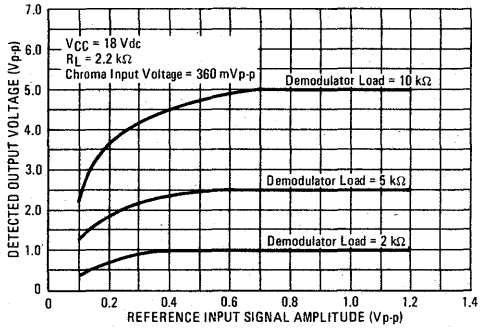


FIGURE 7 – DETECTED OUTPUT VOLTAGE versus SUPPLY VOLTAGE

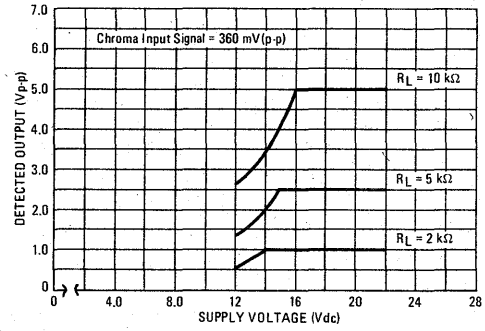


FIGURE 8 – DC OUTPUT VOLTAGE versus LUMINANCE INPUT

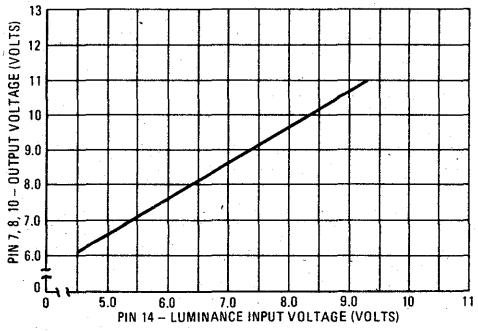
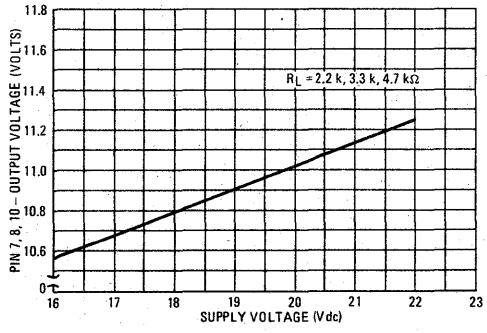


FIGURE 9 – DC OUTPUT VOLTAGE versus SUPPLY VOLTAGE



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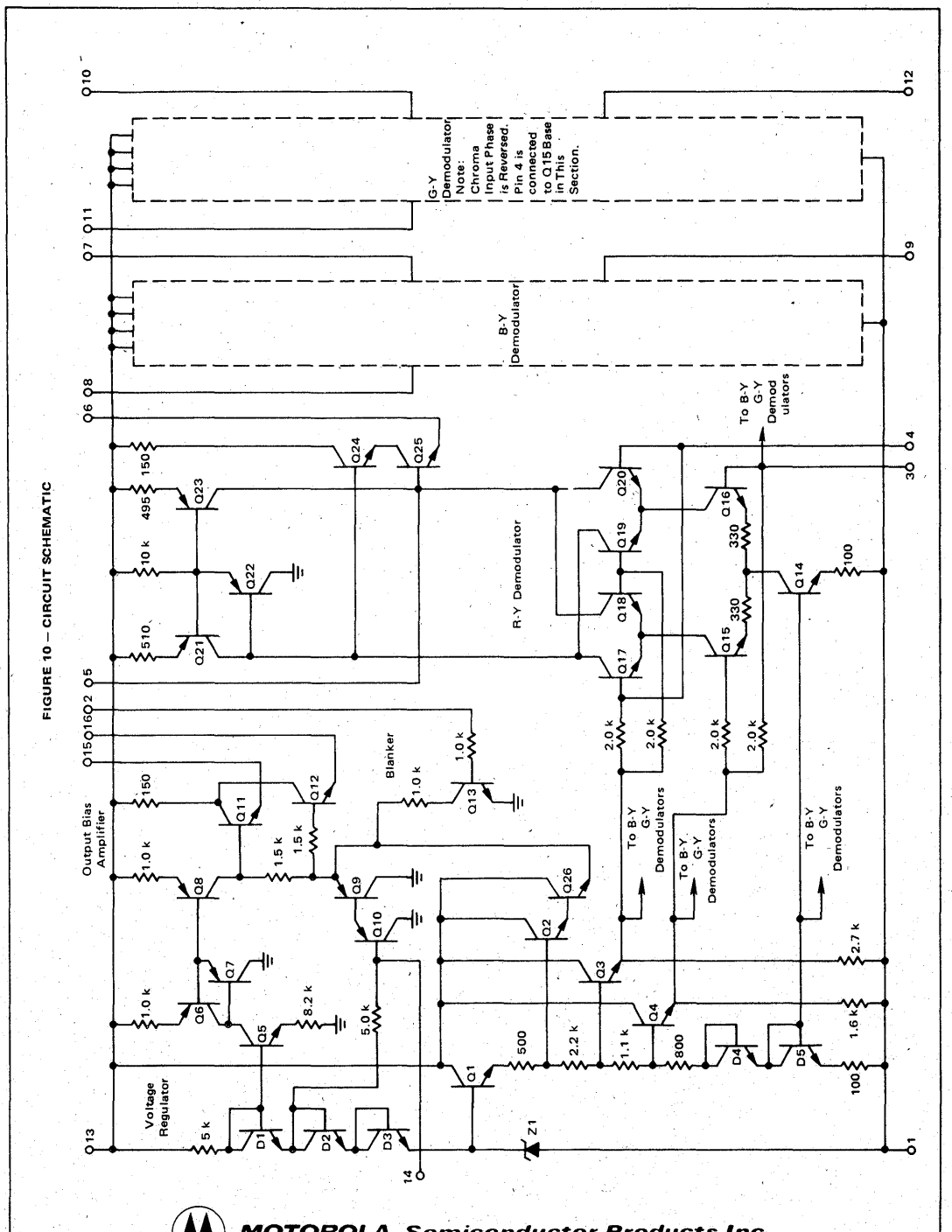


FIGURE 10 – CIRCUIT SCHEMATIC

ORDERING INFORMATION

Device	Temperature Range	Package
MC1324P	0°C to +75°C	Plastic DIP

MC1324

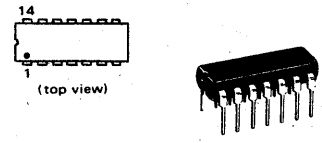
DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH R G B MATRIX AND CHROMA DRIVER STAGES

. . . a monolithic device designed for use in solid-state color television receivers.

- Luminance Input Provided
- Good Chroma Sensitivity – 0.36 Vp-p Input for 5 Vp-p Output
- Low Differential Output DC Offset Voltage – 0.6 V max
- DC Temperature Stability – 3 mV/°C typ
- Negligible Change in Output Voltage Swing and Varying 3.58-MHz Reference Input Signal
- High Ripple Rejection Achieved with MOS Filter Capacitors
- High Blue Output Voltage Swing – 10 V(p-p) typ
- Blanking Input Provided
- Improved MC1326
- Short-Circuit Protected Outputs

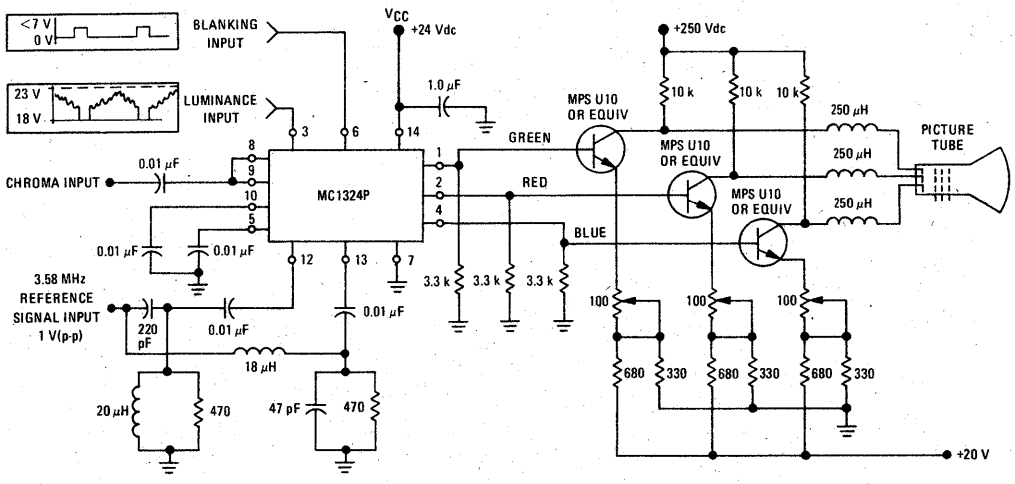
DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH R G B OUTPUT MATRIX

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

FIGURE 1 – MC1324 TYPICAL APPLICATION



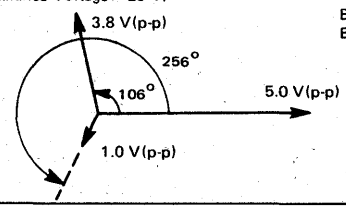
A typical application is given above to indicate the requirements and output functions of this chroma demodulator.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Chroma Signal Input Voltage	5.0	V(pk)
Reference Signal Input Voltage	5.0	V(pk)
Minimum Load Resistance	2.2	k ohms
Luminance Input Voltage	12	V(p-p)
Blanking Input Voltage	7.0	V(p-p)
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, V_{ref} = 1.0 V(p-p), R_L = 3.3 k ohms, T_A = +25°C unless otherwise noted.)

Characteristic	Pin No.	Min	Typ	Max	Unit
STATIC CHARACTERISTICS (See Figure 2.)					
Quiescent Output Voltage	1,2,4	14.3	15	16.3	Vdc
Quiescent Input Current (R_L = ∞) (R_L = 3.3 k ohms)		 – 16.5	 6.0 19	 – 25.5	mA
Reference Input dc Voltage	5,12,13	–	6.8	–	Vdc
Chroma Input dc Voltage	8,9,10	–	3.6	–	Vdc
Differential Output Voltage	1,2,4	–	0.3	0.6	Vdc
Output Temperature Coefficient (Reference Input Voltage = 1.0 V(p-p), +25° to +65°C)	1,2,4	–	3.0	–	mV/°C
DYNAMIC CHARACTERISTICS (See Figure 3.)					
Detected Output Voltage (See Note 1.) +(B-Y) -(B-Y)	4	 4.0 4.0	 5.0 5.0	 – –	V(pk)
Chroma Input Voltage (B-Y Output = 5.0 V[p-p]) (See Note 2.)	8	–	0.36	0.7	V(p-p)
Luminance Input Resistance	3	100	–	–	kΩ
Luminance Gain From Pin 3 to Outputs (@ dc) (@ 5.0 MHz)	1,2,4	 – –	 0.95 0.5	 – –	–
Blanking Input Resistance 1.0 Vdc 0 Vdc	6	 – –	 1.1 75	 – –	kΩ
Detected Output Voltage (Adjust B-Y Output to 5.0 V(p-p), Luminance Voltage = 23 V) G-Y Output R-Y Output	4 1 2	 0.75 3.5	 1.0 3.8	 1.25 4.2	V(p-p)
Relative Output Phase (B-Y Output = 5.0 V(p-p), Luminance Voltage = 23 V) B-Y to R-Y Output B-Y to G-Y Output	 4,2 4,1	 101 248	 106 256	 111 264	Degrees
Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage)	1,2,4	–	100	500	mV(p-p)
Residual Carrier and Harmonics Output Voltage (with Input Signal Voltage, normal Reference Signal Voltage and B-Y Output = 5.0 V[p-p])	1,2,4	–	–	1.0	V(p-p)
Reference Input Resistance	12,13	–	2.0	–	kΩ
Reference Input Capacitance	12,13	–	6.0	–	pF
Chroma Input Resistance	9,10	–	2.0	–	kΩ
Chroma Input Capacitance	9,10	–	2.0	–	pF



NOTES:

1. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 1.2 V(p-p).
2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5 V(p-p). The Chroma Input Voltage at this point should be equal to or less than 0.7 V(p-p).

TEST CIRCUITS

(V_{CC} = 24 Vdc, R_L = 3.3 Kilohms, T_A = +25°C unless otherwise noted.)

FIGURE 2 – DC OUTPUT VOLTAGE TEST CIRCUIT WITH NORMAL REFERENCE INPUT VOLTAGE (B, R, AND G)

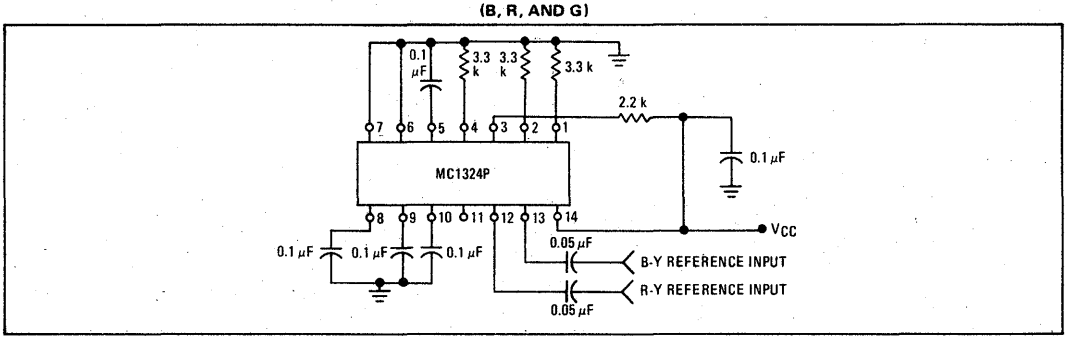
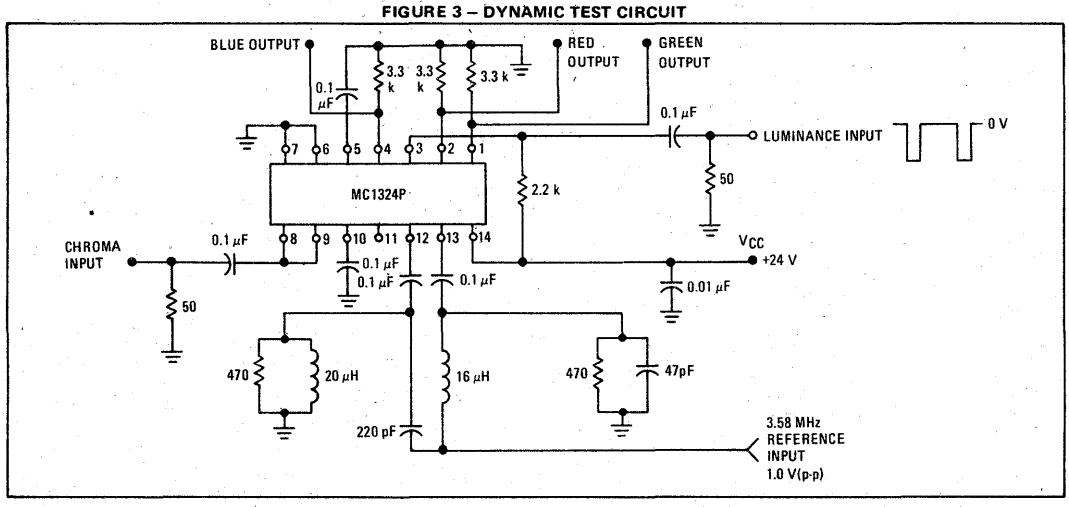


FIGURE 3 – DYNAMIC TEST CIRCUIT



TYPICAL CHARACTERISTICS

FIGURE 4 – DETECTED OUTPUT VOLTAGE
(Test Circuit of Figure 3)

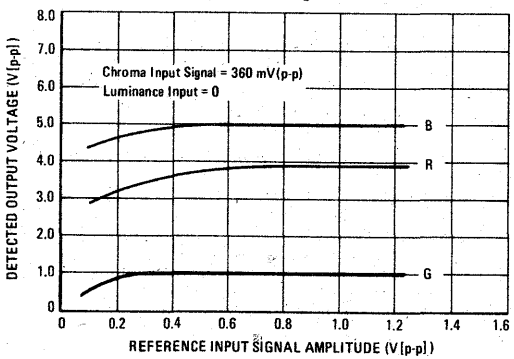


FIGURE 5 – POWER DISSIPATION

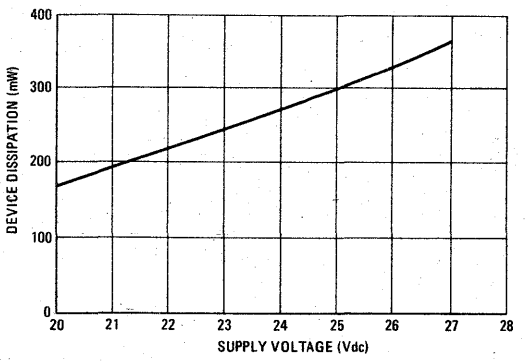
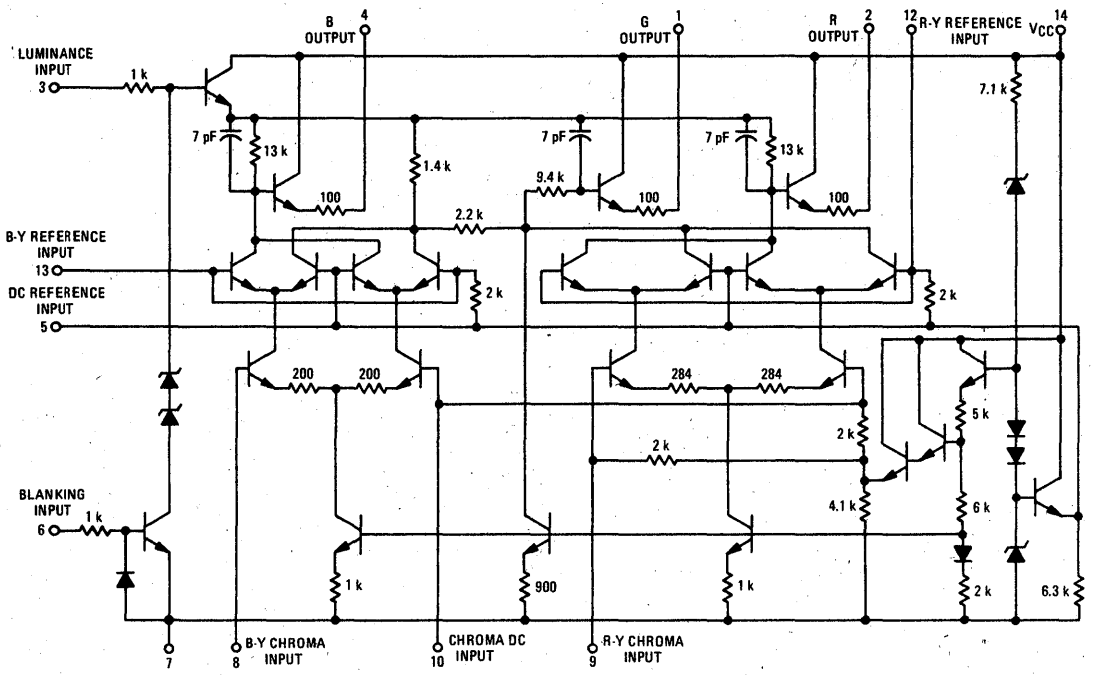


FIGURE 6 – CIRCUIT SCHEMATIC



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ORDERING INFORMATION

Device	Temperature Range	Package
MC1327P	−20°C to +75°C	Plastic DIP
MC1327PQ	−20°C to +75°C	Plastic

MC1327

DUAL DOUBLY BALANCED CHROMA DEMODULATOR WITH RGB MATRIX, PAL SWITCH, AND CHROMA DRIVER STAGES

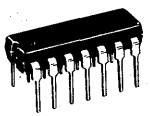
. . . a monolithic device designed for use in solid-state color television receivers.

- Good Chroma Sensitivity — 0.28 Vp-p Input Typical for 5.0 Vp-p Output
- Low Differential Output DC Offset Voltage — 0.6 V Maximum
- Differential DC Temperature Stability — 0.7 mV/°C
- High Blue Output Voltage Swing — 10 Vp-p Typical
- Blanking Input Provided
- Luminance Bandwidth Greater than 5.0 MHz

DUAL DOUBLY BALANCED CHROMA DEMODULATOR with RGB OUTPUT MATRIX AND PAL SWITCH

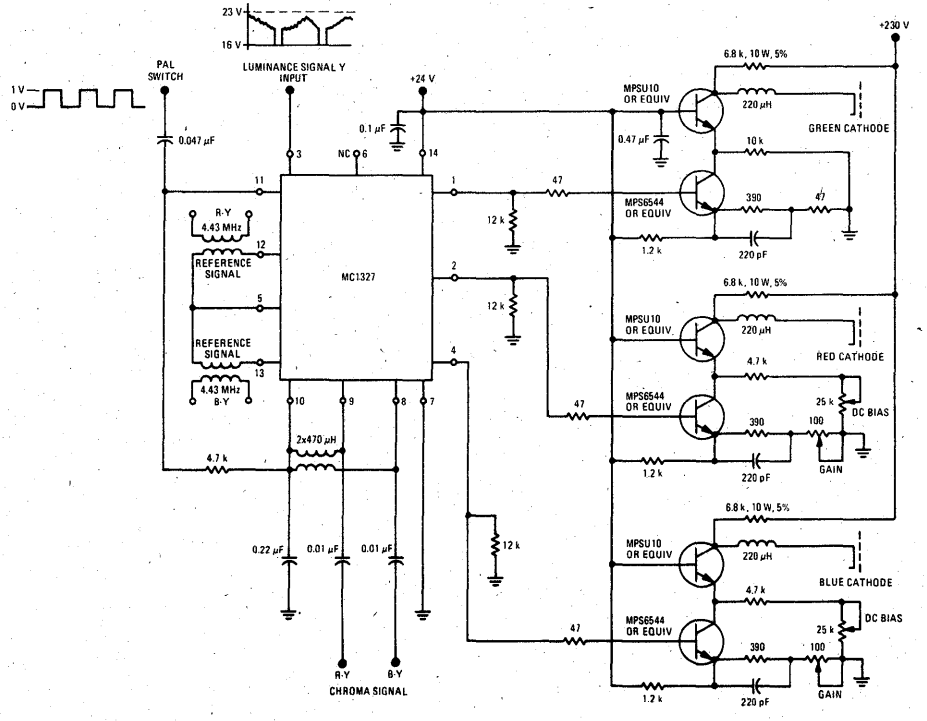
SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 646



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 — TYPICAL APPLICATION CIRCUIT



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Chroma Signal Input Voltage	5.0	Vpk
Reference Signal Input Voltage	5.0	Vpk
Minimum Load Resistance	3.0	k ohms
Luminance Input Voltage	12	Vp-p
Blanking Input Voltage	7.0	Vp-p
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, R_L = 3.3 k ohms, T_A = +25°C unless otherwise noted)

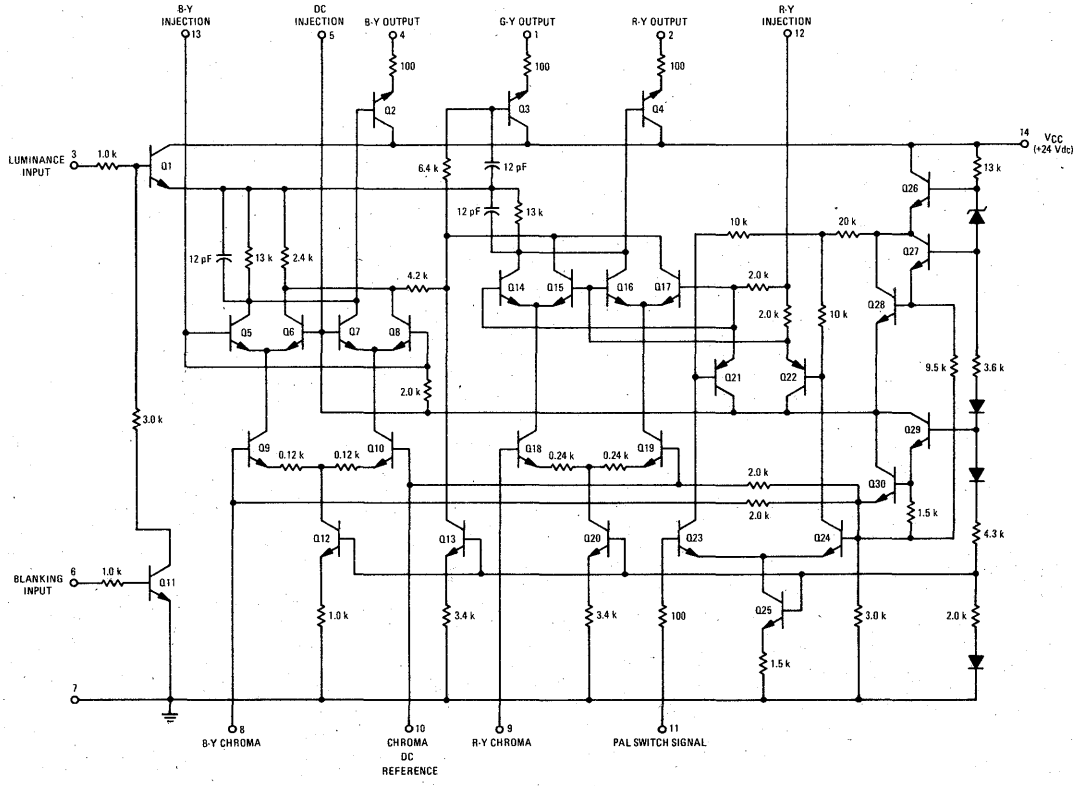
Characteristic	Pin No.	Min	Typ	Max	Unit
STATIC CHARACTERISTICS					
Quiescent Output Voltage (See Figure 2)	1,2,4	13.2	14.5	15.8	Vdc
Quiescent Input Current from Supply (Figure 2) (R_L = ∞) (R_L = 3.3 k ohms)		 – 16	 7.5 19	 – 26	mA
Reference Input DC Voltage (Figure 2)	5,12,13	–	6.2	–	Vdc
Chroma Reference Input DC Voltage (Figure 2)	8,9,10	–	3.4	–	Vdc
Differential Output Voltage (See Note 1 and Figure 2)	1,2,4	–	0.3	0.6	Vdc
Differential Output Voltage Temperature Coefficient (See Note 1 and Figure 2) (+25°C to +65°C)	1,2,4	–	0.7	–	mV/°C
Output Voltage Temperature Coefficient (See Note 1 and Figure 2) (+25°C to +65°C)	1,2,4	–	+0.5	±5.0	mV/°C

DYNAMIC CHARACTERISTICS (V_{CC} = 24 Vdc, R_L = 3.3 k ohms, Reference Input Voltage = 1.0 Vp-p, T_A = +25°C unless otherwise noted)

Blue Output Voltage Swing (See Note 2 and Figure 3)	4	8.0	10	–	Vp-p
Chroma Input Voltage (B Output = 5.0 Vp-p) (See Note 3 and Figure 3)	8	–	280	550	mVp-p
Luminance Input Resistance	3	100	–	–	kΩ
Luminance Gain From Pin 3 to Outputs (@ dc) (@ 5.0 MHz, reference at 100 kHz)	1,2,4	 – –	 0.95 -1.8	 – –	– dB
Differential Luminance Gain, RGB Outputs (@ 5.0 MHz)		–	0.3	–	dB
Blanking Input Resistance (1.0 Vdc) (0 Vdc)	6	 – –	 1.1 75	 – –	kΩ
Detected Output Voltage (Adjust B Output to 5.0 Vp-p, Luminance Voltage = 23 V) (See Note 4) G Output R Output	4 1 2	 1.4 2.5	 1.8 2.9	 2.2 3.3	Vp-p
PAL Switch Operating Voltage Range (7.8 kHz Square Wave)	11	0.3	–	3.0	Vp-p
R-Y Output dc Offset with PAL Switch Operation		–	–	100	mVdc
Demodulator Unbalance Voltage (no Chroma Input Voltage and normal Reference Signal Input Voltage)	1,2,4	–	200	300	mVp-p
Residual Carrier and Harmonics Output Voltage (with Input Signal Voltage, normal Reference Signal Voltage and B Output = 5.0 Vp-p)	1,2,4	–	0.6	1.0	Vp-p
Reference Input Resistance (Chroma Input = 0)	12,13	–	2.0	–	kΩ
Reference Input Capacitance (Chroma Input = 0)	12,13	–	6.0	–	pF
Chroma Input Resistance	8,9,10	–	2.0	–	kΩ
Chroma Input Capacitance	8,9,10	–	2.0	–	pF

NOTES: 1. Chroma Input Signal Voltage = 0 and normal Reference Input Signal Voltage = 1.0 Vp-p.
2. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage to 1.2 Vp-p.
3. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5.0 Vp-p.
4. With normal Reference Input Signal Voltage, adjust Chroma Input Signal Voltage until the Blue Output Voltage = 5.0 Vp-p. At this point, the Red and Green voltages will fall within the specified limits.

MC1327 CHROMA DEMODULATOR (PAL)



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TEST CIRCUITS

(V_{CC} = 24 Vdc, R_L = 3.3 kilohms, T_A = +25°C unless otherwise noted)

FIGURE 2 – DC OUTPUT VOLTAGE TEST CIRCUIT WITH NORMAL REFERENCE INPUT VOLTAGE (B, R, AND G)

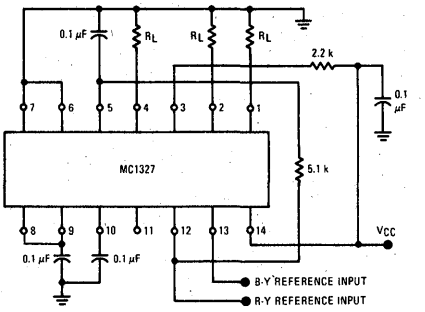
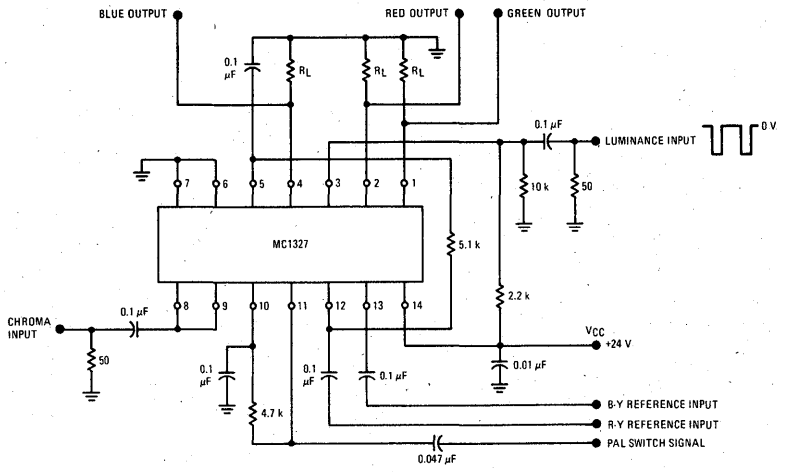


FIGURE 3 – DYNAMIC TEST CIRCUIT



ORDERING INFORMATION

Device	Temperature Range	Package
MC1330A1P	0°C to +75°C	Plastic DIP
MC1330A2P	0°C to +75°C	Plastic DIP

MC1330A1P
MC1330A2P

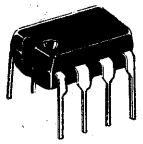
LOW-LEVEL VIDEO DETECTOR

. . . an integrated circuit featuring very linear video characteristics and wide bandwidth. Designed for color and monochrome television receivers, replacing the third IF, detector, video buffer and AFC buffer.

- Conversion Gain – 33 dB (Typ)
- Excellent Differential Phase and Gain
- High Rejection of IF Carrier Feedthrough
- High Video Output – 8.0 V(p-p)
- Fully Balanced Detector
- Output Temperature Compensated
- Improved Versions of the MC1330P

LOW-LEVEL VIDEO DETECTOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

CIRCUIT DESCRIPTION

The MC1330A video detector is a fully balanced multiplier detector circuit that has linear amplitude and phase characteristics. The signal is divided into two channels, one a linear amplifier and the other a limiting amplifier that provides the switching carrier for the detector.

The switching carrier has a buffered output for use in providing the AFT function.

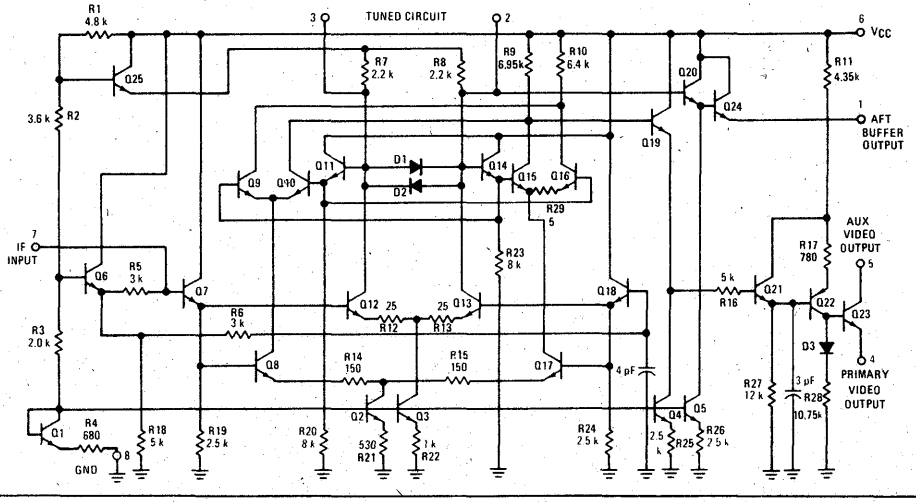
The video amplifier output is an improved design that reduces the differential gain and phase distortion associated with previous video output systems. The output is wide band, > 8.0 MHz, with normal negative polarity. A separate narrow bandwidth, positive video output is also provided.

OUTPUT VOLTAGE SELECTION

The MC1330A1P is identical to the MC1330A2P with the following exception:

	ZERO SIGNAL DC OUTPUT VOLTAGE
MC1330A1P	7.0 to 8.2 Vdc
MC1330A2P	7.8 to 9.0 Vdc

FIGURE 1 – CIRCUIT SCHEMATIC



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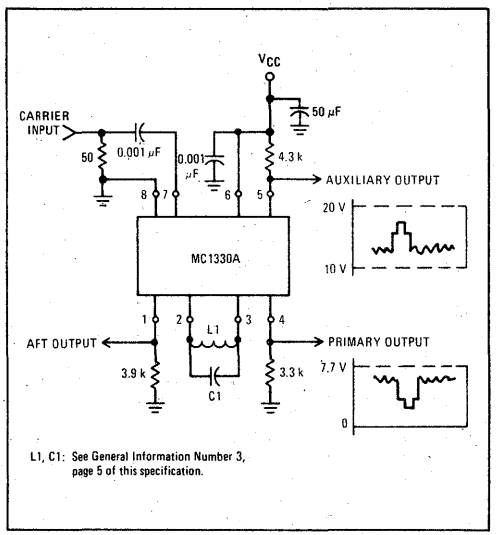
MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage	24	Vdc
DC Video Output Current	5.0	mAdc
DC AFT Output Current	2.0	mAdc
Junction Temperature	150	°C
Operating Ambient Temperature Range	0 to 75	°C
Storage Temperature Range	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, Q = 40, fc = 45.75 MHz, T_A = +25°C unless otherwise noted)

Characteristic		Pin	Min	Typ	Max	Unit
Zero Signal dc Output Voltage	MC1330A1P	4	7.0	–	8.2	Vdc
	MC1330A2P	4	7.8	–	9.0	Vdc
Supply Current		5, 6	11	17.5	20	mA
Maximum Signal dc Output Voltage		4	–	0	0.5	Vdc
Conversion Gain for 1.0 Vp-p Output (30% Modulation)		7	25	36	65	mVrms
AFT Buffer Output at Carrier Frequency		1	300	475	650	mVp-p

FIGURE 2 – TEST FIXTURE CIRCUIT



L1, C1: See General Information Number 3, page 5 of this specification.

FIGURE 3 – INPUT ADMITTANCE

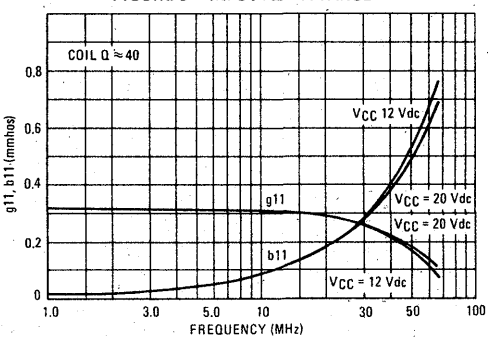
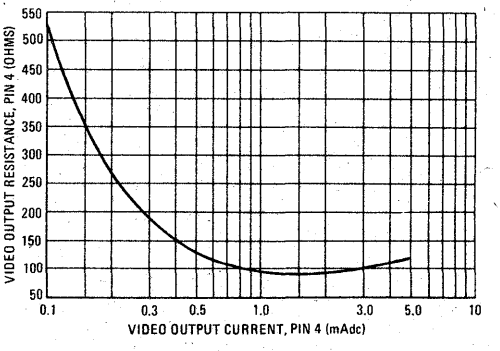


FIGURE 4 – VIDEO DETECTOR OUTPUT RESISTANCE



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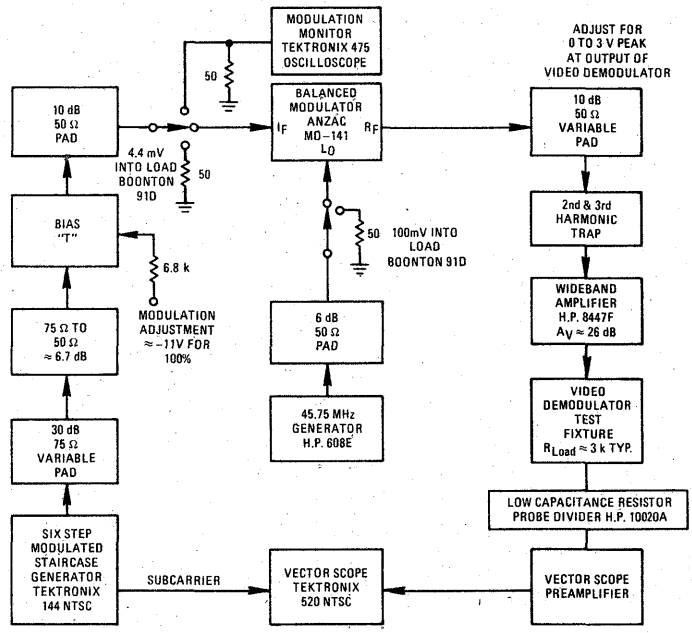
DESIGN CHARACTERISTICS (V_{CC} = +20 Vdc, Q = 40, f_c = 45.75 MHz, T_A = +25°C unless otherwise noted)

Characteristic	Pin	Typ	Unit
Input Resistance Input Capacitance	7 7	4.9 1.5	kΩ pF
Internal Resistance (Across Tuned Circuit) Internal Capacitance (Across Tuned Circuit)	2, 3 2, 3	4.4 1.0	kΩ pF
Negative Video Output Bandwidth (Figure 10) Positive Video Output Bandwidth (Figure 10)	4 5	10.8 2.2	MHz MHz
Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6 Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6	4 4	7.0 4.0	Degrees %
Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ	4 4	8.0 6.0	Degrees %
920 kHz Beat Output (dB Below 100% Modulated Video, See Figure 11) 45.75 MHz = Reference 42.17 MHz = - 6 dB 41.25 MHz = -20 dB	4	−38	dB
Video Output Resistance @ 1 MHz, 2 mA	4	94	Ω
Input Overload (Carrier Level at Input to Caused Detector Output, Pin 4, To Go Positive 0.1 Vdc From Ground.) V_{CC} = 12 Vdc V_{CC} = 15 Vdc V_{CC} = 20 Vdc V_{CC} = 24 Vdc	7	2.0 2.6 3.6 4.6	Volts
Power Supply Voltage Range	5	10 to 24	Volts

FIGURE 5 –DIFFERENTIAL PHASE AND GAIN TEST SET UP



TYPICAL CHARACTERISTICS

(V_{CC} = +20 Vdc, T_A = +25°C Unless Otherwise Noted)

FIGURE 6 – OUTPUT VOLTAGE TRANSFER FUNCTION

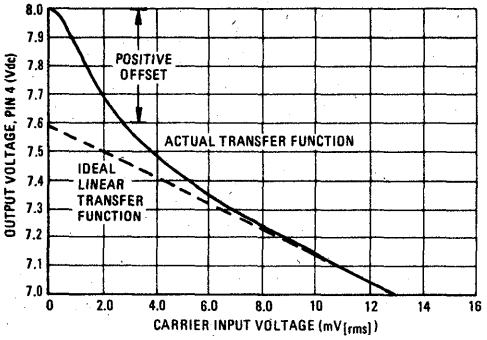


FIGURE 7 – OUTPUT VOLTAGE TRANSFER FUNCTION

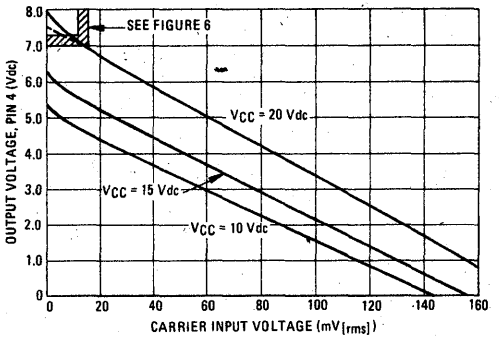


FIGURE 8 – OUTPUT VOLTAGE, SUPPLY CURRENT

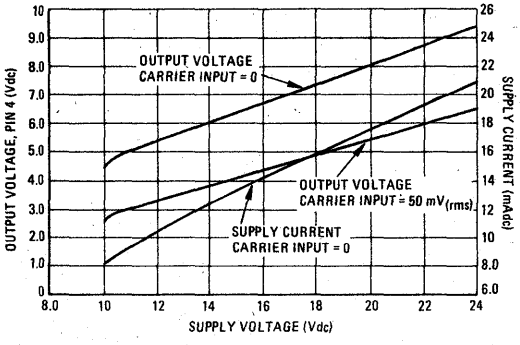


FIGURE 9 – AFT LIMITING

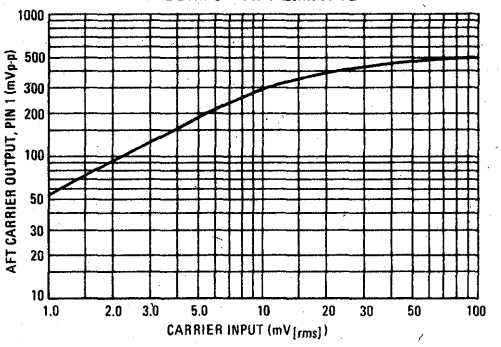


FIGURE 10 – VIDEO OUTPUT RESPONSE

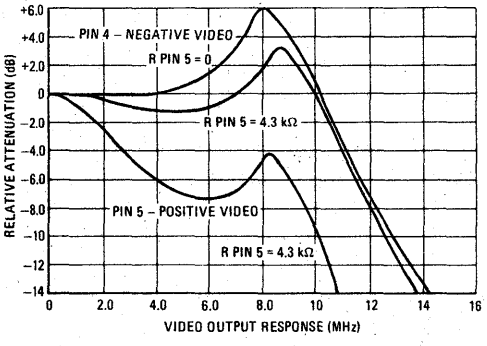
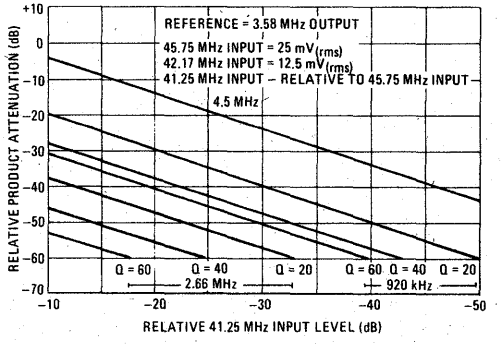


FIGURE 11 – VIDEO OUTPUT PRODUCTS



7

TV-IF Amplifier Information

A very compact high performance IF amplifier constructed as shown in Figure 14 minimizes the number of overall components and alignment adjustments. It can be readily combined with normal tuners and input tuning-trapping circuitry to provide the performance demanded of high quality receivers. This configuration will provide approximately 93 dB voltage gain and can accomodate the usual low impedance input network or, if desired, can take advantage of an impedance step-up from tuner to MC1349P input.

The burden of selectivity, formerly found between the third IF and detector, must now be placed at the interstage. The nominal 3 volt peak-to-peak output can be varied from 0 to 7.0 V with excellent linearity and freedom from spurious output products.

Alignment is most easily accomplished with an AM generator, set at a carrier frequency of 45.75 MHz, modulated with a video frequency sweep. This provides the proper realistic conditions necessary to operate to low-level detector (LLD). The detector tank is first adjusted for maximum detected dc (with a CW input), next, the video sweep modulation is applied and the interstage and input circuits aligned, step by step, as in a standard IF amplifier.

Note: A normal IF sweep generator, essentially an FM generator, will not serve properly without modification. The LLD tank attempts to "follow" the sweep input frequency, and results in variations of switching amplitude in the detector. Hence, the apparent overall response becomes modified by the response of the LLD tank, which a real signal doesn't do.

This effect can be prevented by resistively adding a 45.75 MHz CW signal to the output of the sweep generator approximately 3 dB greater than the sweep amplitude. See Figures 12 and 13 below. For a more detailed description of the MC1330AP see application note AN-545.

MC1330A General Information

The MC1330A offers the designer a new approach to an old problem. Now linear detection can be performed at much lower power signal levels than possible with a detector diode.

Offering a number of distinct advantages, its easy implementation should meet with ready acceptance for television designs. Some specific features and information on systems design with this device are given below:

1. The device provides excellent linearity of output versus input, as shown in Figures 6 and 7. These graphs also show that video peak-to-peak amplitude (ac) does not change with supply voltage variation. (Slopes are parallel. Visualize a given variation of input CW and use the figure as a transfer function.)

2. The dc output level does change linearly with supply voltage shown in Figure 8. This can be accommodated by regulating the supply or by referencing the subsequent video amplifier to the same power supply.

3. The choice of Q for the tuned circuit of pins 2 and 3 is not critical. The higher the Q, the better the rejection of 920 kHz products but the more critical the tuning accuracy required. See Figure 11. Values of Q from 20 to 50 are recommended. (Note the internal resistance.)

4. A video output with positive-going sync is available at pin 5 if required. This signal has a higher output impedance than pin 4 so it must be handled with greater care. If not used, pin 5 may be connected directly to the supply voltage (pin 6).The video response will be altered somewhat. See Figure 10.

5. An AFT output (pin1) provides 460 mV of IF carrier output, sufficient voltage to drive an AFT ratio detector, with only one additional stage.

6. AGC lockout can occur if the input signal presented in the MC1330A is greater than that shown in the input overload section of the design characteristics shown on Page 3. If these values are exceeded, the turns ratio between the primary and secondary of T_1 should be increased. Another solution to the problem is to use an input clamp diode D_1 shown in Figure 14.

7. The total I.F. noise figure at high gain reductions can be improved by reflecting $\approx$ 1 k source impedance to the input of the MC1330AP. This will cause some loss in overall IF voltage gain.

FIGURE 12 – BYPASS DISPLAYED BY CONVENTIONAL SWEEP

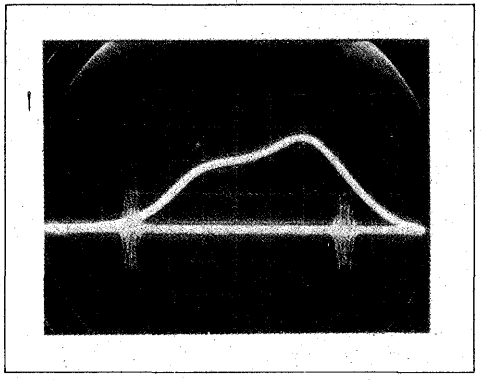
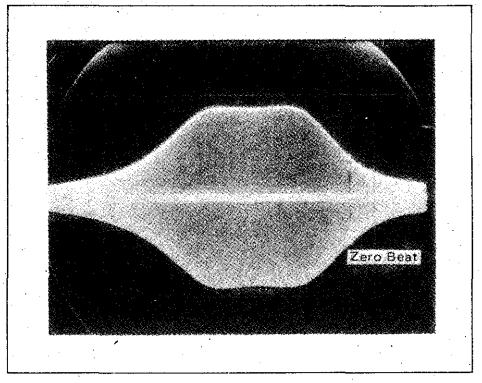
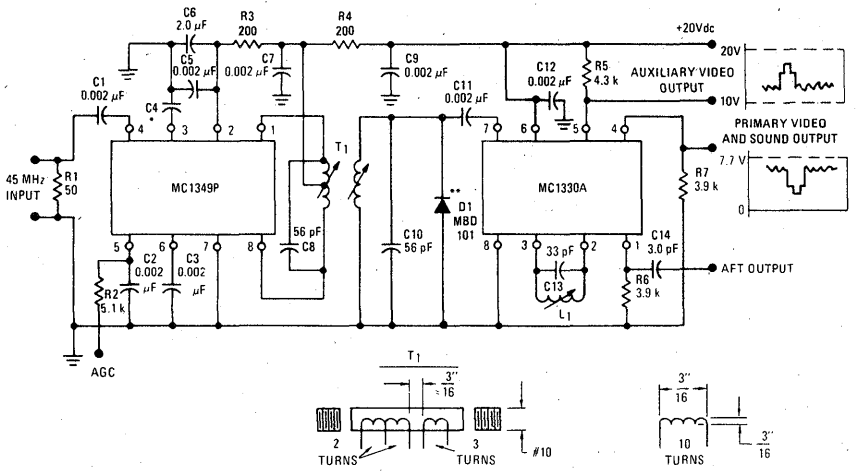


FIGURE 13 – BYPASS DISPLAY WITH THE ADDITION OF CARRIER INJECTION



7

FIGURE 14 – TYPICAL APPLICATION OF MC1349P VIDEO IF AMPLIFIER and MC1330A LOW-LEVEL VIDEO DETECTOR CIRCUIT



All windings 22 AWG tinned nylon acetate wire tuned with Coilcraft #61 slugs, size 10–32, or equivalent

L_1 wound with 26 AWG tinned nylon acetate wire tuned by distorting winding.

*See Note 1 (page 3), and C4, Parts List (page 4) for this specification on the MC1349P Data Sheet.

**See Input Overload Section of the Design Characteristics Page 3, and General Information, Page 5, Note 6.

FIGURE 15 – PRINTED CIRCUIT BOARD PARTS LAYOUT

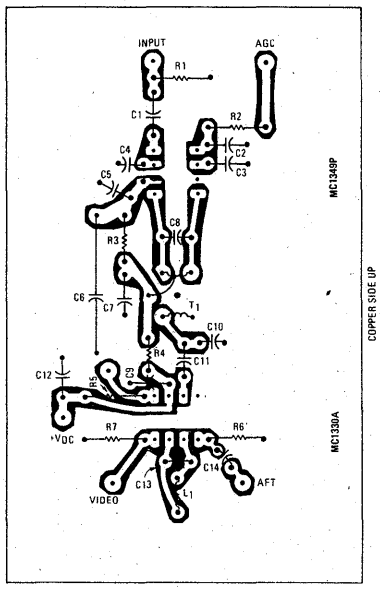
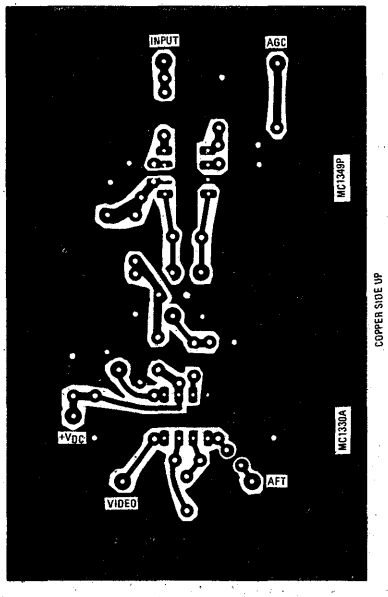


FIGURE 16 – PRINTED CIRCUIT BOARD LAYOUT



7

ORDERING INFORMATION

Device	Temperature Range	Package
MC1331P	0°C to +75°C	Plastic DIP

MC1331P

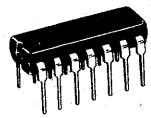
LOW-LEVEL VIDEO DETECTOR

. . . an integrated circuit featuring very linear video characteristics and wide bandwidth. Designed for color and monochrome television receivers, replacing the third IF, detector, video buffer, AFC buffer, sound IF detector, and sync separator.

- Conversion Gain – 34 dB typical
- Video Frequency Response at 8.0 MHz < 3.0 dB
- Input of 36 mV Produces 3.0 V (p-p) Output
- High Video Output – 6.0 V (p-p)
- Fully Balanced Detector
- Separate Sound Detector
- Differential Inputs

LOW-LEVEL VIDEO DETECTOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

CIRCUIT DESCRIPTION

The MC1331 video detector is a fully balanced multiplier detector circuit that has linear amplitude and phase characteristics. The signal is divided into two channels, one a linear amplifier and the other a limiting amplifier that provides the switching carrier for the detector. The input signal level is sensed by an overload protection circuit and clamps the video output amplifier, preventing AGC system lock out.

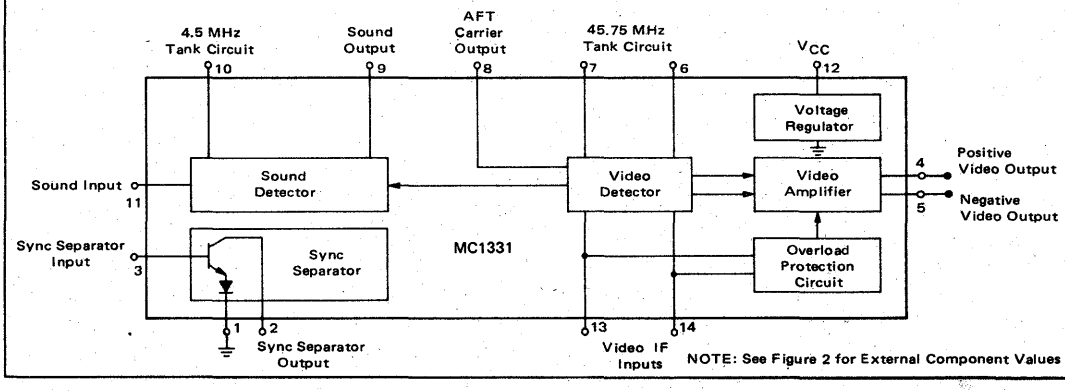
The switching carrier is also used in the sound detector, converting the 41.25 MHz sound carrier into the 4.5 MHz IF frequency. The sound detector has a tuned 4.5 MHz tank circuit to develop the narrow band sound carrier output.

The switching carrier has a buffered output for use in providing the AFT function.

The video amplifier output is an improved all NPN design that reduces the differential gain and phase distortion associated with previous video output systems. The output is wide band, > 8.0 MHz, with normal negative polarity. A separate, narrow bandwidth, positive video output is also provided. Internal regulation maintains the video output dc reference essentially independent of supply voltage variations and reduces the variation in the absolute value of the reference level.

The circuit includes an inexpensive sync separator circuit.

FIGURE 1 – MC1331P BLOCK DIAGRAM



NOTE: See Figure 2 for External Component Values

7

MAXIMUM RATINGS

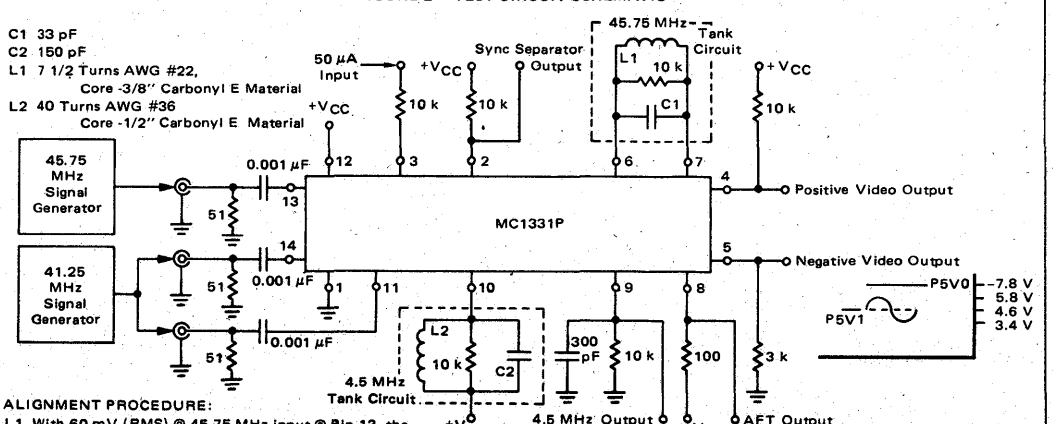
Rating	Value	Unit
Power Supply Voltage	15	Vdc
Input Voltage	2.0	V(RMS)
Maximum DC Video Output Current	5.0	mAdc
Maximum DC Sync Separator Current (Pin 2)	4.0	mAdc
Power Dissipation @ $T_A = 25^oC$ Derate above 25^oC	1.2 10	Watts $mW/^oC$
Operating Ambient Temperature Range	0 to 75	^oC
Storage Temperature Range	-65 to +150	^oC

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, Q = 20, f_C = 45 MHz, $T_A = 25^oC$ unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage Range	–	10.5	–	15	Vdc
Supply Current Range (Zero Signal Input)	12	26	30	34	mA
Zero Signal dc Output Voltage (Figures 3, 4)	5	6.8	7.8	8.8	Vdc
Video Output Transfer Gain (Figure 3) ($V_{Pin\ 13}$ = 60 mV(rms) @ 45.75 MHz)	5	2.0	3.0	–	Vdc
High Frequency Video Output Voltage Swing (@ 4.5 MHz) ($V_{Pin\ 13}$ = 60 mV(rms) @ 45.75 MHz), ($V_{Pin\ 14}$ = 30 mV(rms) @ 41.25 MHz)	5	1.6	2.4	–	V(p-p)
RF Rejection ($V_{Pin\ 13}$ = 60 mV(rms) @ 45.75 MHz)	5	–	150	450	mV(p-p)
Maximum Signal Output (V_2, See Figure 3)	5	–	–	100	mVdc
Available Positive Video Output Swing ($V_{Pin\ 12} - V_{Pin\ 4}$)	4,12	8.0	10.5	–	V(p-p)
AFT Output Voltage Swing	8	75	150	–	mVdc
Transfer Function Negative Offset Voltage (Figure 4) (V_{in} = 0 to 5 mV)	5	–	–	100	mVdc
4.5 MHz Sound Detector Conversion Gain (BW = 200 kHz) ($V_{Pin\ 13}$ = 60 mV(rms) @ 45.75 MHz), ($V_{Pin\ 11}$ = 5 mV(rms) @ 41.25 MHz)	9	35	50	–	mV(rms)
Sync Separator Leakage ($V_{CC} - V_{Pin\ 2}$, R_L = 10 kΩ, Pin 3 Open)	2	–	–	10	μAdc
Sync Separator Voltage Swing ($V_{CC} - V_{Pin\ 2}$, $I_{Pin\ 3}$ = 50 μA)	2	10	–	–	Vp-p

7

FIGURE 2 – TEST CIRCUIT SCHEMATIC



ALIGNMENT PROCEDURE:

L1 With 60 mV (RMS) @ 45.75 MHz input @ Pin 13, the output of Pin 5 is monitored and L1 core is adjusted for minimum dc @ Pin 5. This is equivalent to maximizing the video output (ΔP5V).

L2 With 60 mV (RMS) @ 45.75 MHz input at Pin 13, and 5 mV(RMS) @ 41.25 MHz @ Pin 11, the ac output voltage on Pin 9 is monitored. L2 core is adjusted for maximum 4.5 MHz output @ Pin 9.

DESIGN CHARACTERISTICS (V_{CC} = +12 Vdc, Q = 20, f_C = 45 MHz, T_A = 25°C unless otherwise noted.)

Characteristic	Pin	Typ	Unit
Input Resistance Input Capacitance	13,14 13,14	3.0 3.0	kΩ pF
Input Resistance Input Capacitance	11 11	3.0 3.0	kΩ pF
Internal Resistance (Across Tuned Circuit) Internal Capacitance (Across Tuned Circuit)	6,7 6,7	5.0 4.0	kΩ pF
Video Output Resistance @ 4.5 MHz	5	25	Ω
Sound Detector Output Resistance	9	100	Ω
Negative Video Output Bandwidth (Figure 7)	5	8.0	MHz
Positive Video Output Bandwidth (Figure 7)	4	3.0	MHz
Differential Gain @ 3.58 MHz Differential Phase @ 3.58 MHz	5 5	5.0 5.0	% Degrees
920 kHz Beat Output (Below 100% Modulated Video) (1) (45.75 MHz = Reference) (42.17 MHz = -6.0 dB) (41.25 MHz = -20 dB)	5	36	dB
Video Output Supply Rejection (d Pin 5 V_O/d V_{CC})	—	20	dB
Carrier Rejection (Sound Channel)	9	-20	dB
Modulation Rejection in AFT Output (2) (1 kHz Sideband)	—	30	dB

(1) Undesired beat product between 42.17 MHz subcarrier (-6 dB) and the 41.25 MHz soundcarrier (-20 dB) relative to the 3.58 MHz output. Carrier levels are relative to the 45.75 MHz carrier.
(2) Residual at 90% double sideband modulated at 1 kHz on 45.75 MHz video carrier.

TYPICAL OUTPUT CHARACTERISTICS

FIGURE 3 – OUTPUT VOLTAGE TRANSFER FUNCTION

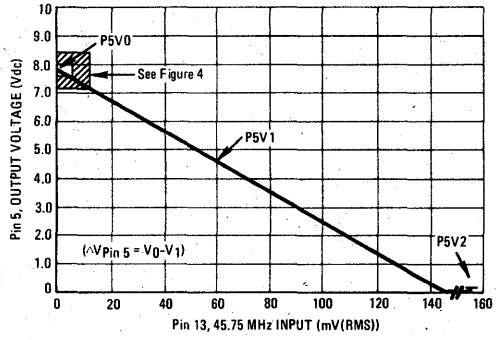
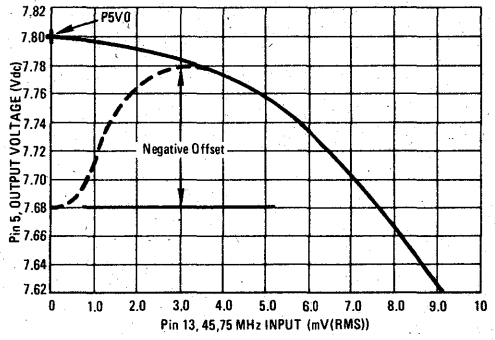


FIGURE 4 – OUTPUT VOLTAGE TRANSFER FUNCTION



TYPICAL CHARACTERISTICS

FIGURE 5 – SOUND DETECTOR OUTPUT versus Pin 13 VOLTAGE

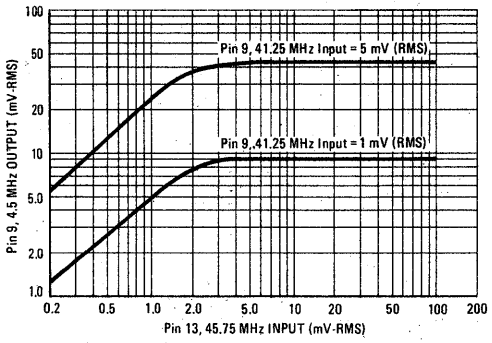


FIGURE 6 – SOUND DETECTOR OUTPUT versus Pin 11 VOLTAGE

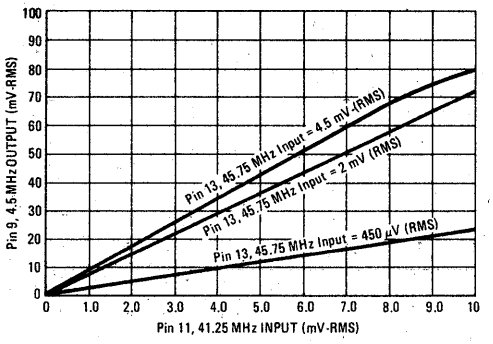


FIGURE 7 – VIDEO OUTPUT RESPONSE

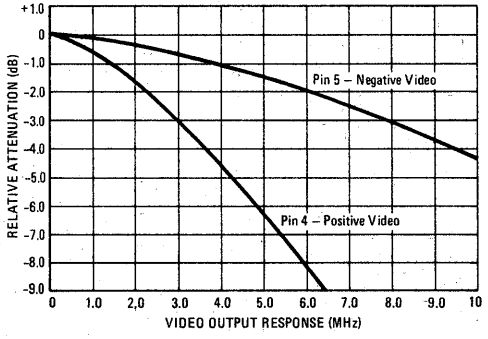


FIGURE 8 – VIDEO OUTPUT PRODUCTS

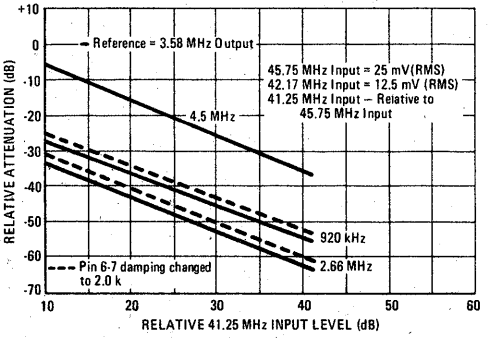
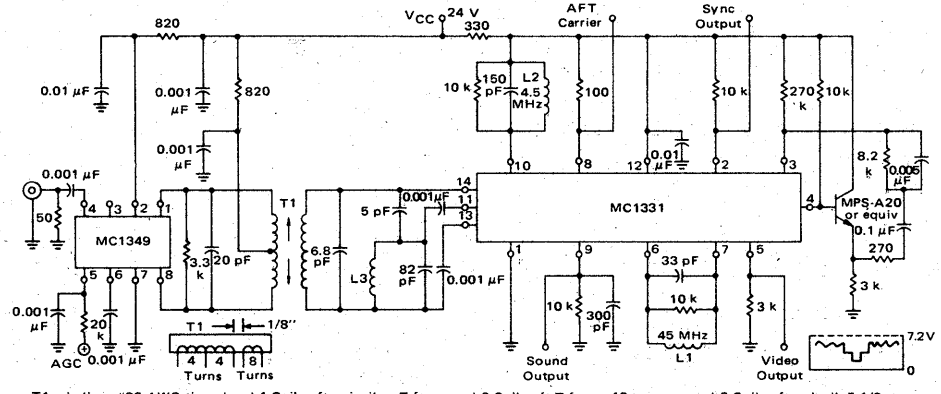


FIGURE 9 – VIDEO IF APPLICATION CIRCUIT



APPLICATION INFORMATION

(For further information, see AN-751)

The video IF amplifier shown in Figure 9 provides excellent system performance required in TV receivers. Typical L-C input selectivity and trapping network may be added or the selectivity element could be a block filter. The system shown has a gain in the video channel of 85 dB, measured from the input of the MC1349. The unique interstage shown eliminates the previous performance trade-off between adequate 41.25 MHz rejection in the video channel and sufficient 4.5 MHz detection for good sound performance. Figure 4 shows the interstage response of double tuned transformer T1 and the 41.25 MHz take-off circuit. The 41.25 MHz rejection in the video channel is 10 dB. With a total sound carrier attenuation of 26 dB in the video channel, the 920 kHz rejection of the MC1331 is in excess of 40 dB. The output from the sound detector is greater than 5 millivolts, sufficient to maintain the sound IF system in hard limiting.

The alignment of the system is similar to that previously used in the MC1330 operation. A signal, comprised of a 45.75 MHz carrier, modulated with video sweep information, provides the simplest alignment. The detector coil, L1, is peaked for maximum detected dc with the unmodulated carrier. Then the video sweep modulation is applied and the interstage and possible input circuits are aligned. The 41.25 MHz trap coil, L3, is then adjusted temporarily for minimum 41.25 MHz. The output of the sound detector is then monitored (Figure 5). The 4.5 MHz coil, L2, is aligned for maximum output. The trap coil, L3, can then be optimized for maximum 4.5 MHz output.

Note: A normal IF sweep generator, essentially an FM generator, will not serve properly without modification. The detector tank attempts to "follow" the sweep input frequency, and results in variations of the switching carrier amplitude in the detector. Hence, the apparent overall response becomes modified by the response of the detector tank circuit. This does not occur when a normal video IF signal is applied, as a true fixed carrier is available to "lock" the detector tank circuit.

This effect can be prevented by resistively adding a 45.75 MHz CW signal to the output of the sweep generator at approximately 6 dB greater than the sweep amplitude.

The circuit described in Figure 12 is capable of providing the high performance required of quality TV receivers. The sound IF carrier (41.25 MHz) is separated from the video IF information early in the system, avoiding intermodulation in the video channel and any degradation of the sound noise figure performance. The signal is recombined in the MC1331 for normal intercarrier demodulation. The separate 41.25 MHz amplifier has 40 dB voltage gain, sufficient for driving the sound detector, which provides at least 5 millivolts of 4.5 MHz with normal picture carrier to sound carrier ratios. The L3 circuit Q is approximately 20 (see Figure 12), narrowing slightly at maximum gain; this requires alignment of this sound amplifier at maximum gain.

The video channel incorporates the MC1352, which includes the AGC function. The AGC for the sound amplifier is derived from Pin 14 of the MC1352. In set partitioning which includes a separate AGC-sync circuit (jungle) the amplifier could be the MC1349. The circuit shown has 80 dB gain, including the block filter insertion loss of 15 dB. The video response, shown in Figure 14, is mainly determined by the bandpass filter; which could be an acoustic surface wave filter as shown, a block L-C filter, or a discrete component L-C network. The pre-amplifier is included to improve the noise figure of the system, and to provide isolation of the 41.25 MHz trap from the block filtering. The interstage is broad tuned with fixed chokes. Since the system includes high attenuation of the 41.25 MHz, the detector coil (L10) could be heavily damped, i.e., Rd = 2 kΩ, allowing for the possibility of pre-tuning the detector coil. This will show a slight degradation of beat product rejection as shown in Figure 4. The detector alignment is the same as described.

7

FIGURE 10 – VIDEO CHANNEL OUTPUT – PIN 5

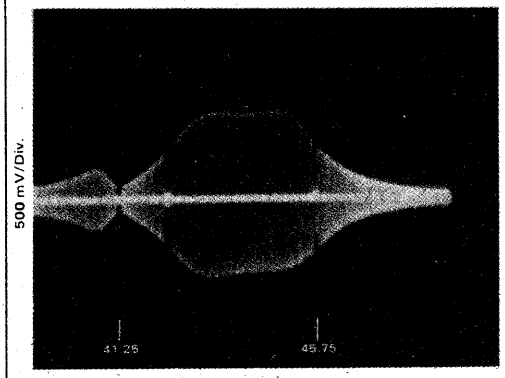


FIGURE 11 – SOUND CHANNEL OUTPUT – PIN 9

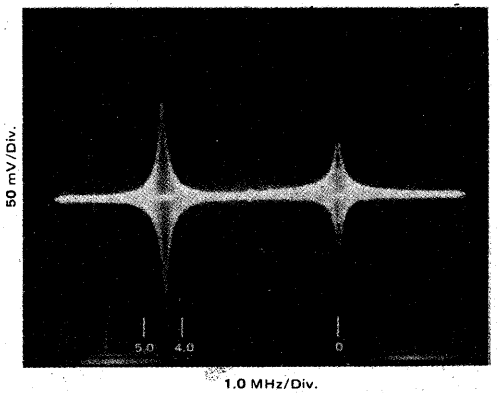
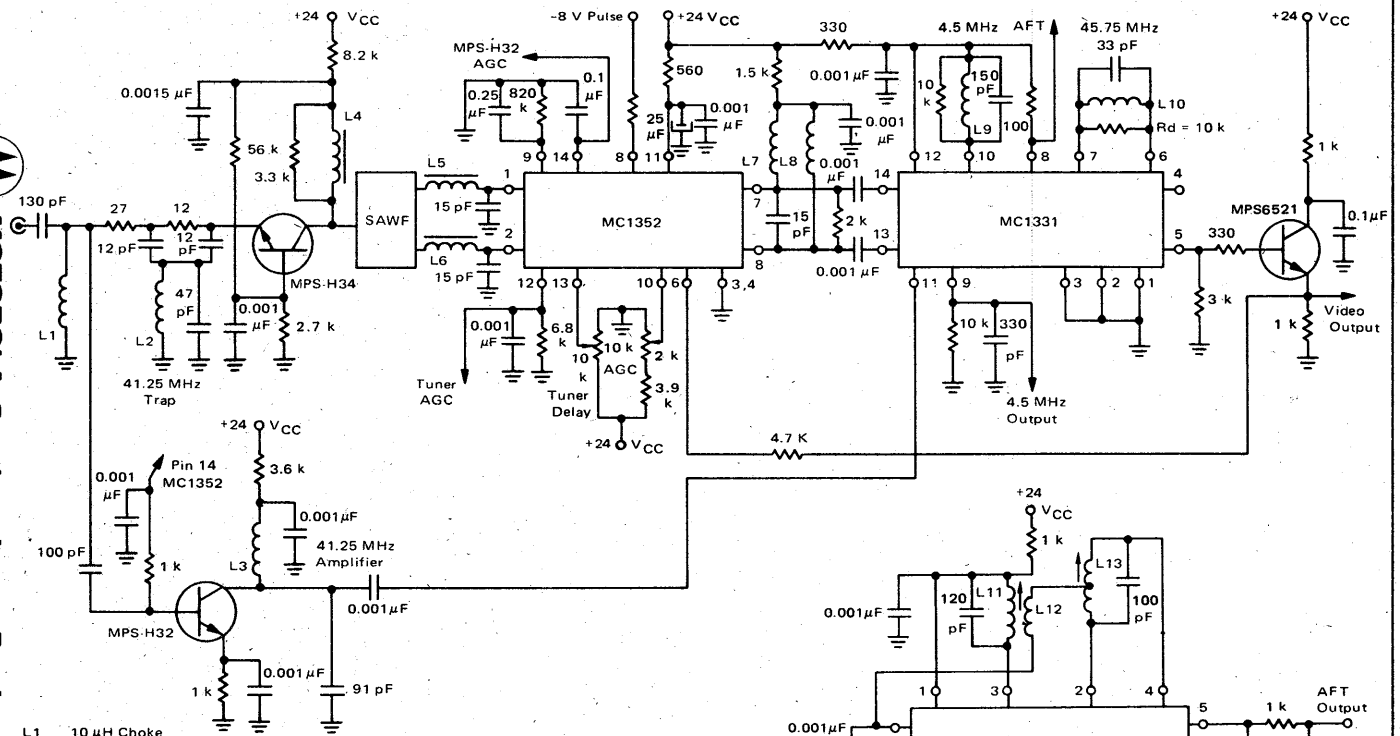


FIGURE 12 – APPLICATION CIRCUIT USING MC1352



L1 10 μH Choke

L2 9½ Turns, AWG #18 Copper Wire
PAUL SMITH CO Coil Form SK308
3/8" 10-32 Core · Carbonyl J Material

L3 4½ Turns, AWG #22 Copper Wire
PAUL SMITH CO. Coil Form SK478
3/8" 10-32 Core – Carbonyl E Material

L4 21 Turns, AWG #36 Copper Wire Over 3.3 kΩ Resistor, 1/2 W

L5, L6 0.47 μH Choke

L7, L8 8 Turns, Center Tapped, Air Core
AWG #36 Single Cell Copper Wire

L9 40 Turns, AWG #36 Copper Wire
PAUL SMITH CO. Coil Form EF186
3/8" 10-32 Core – Corbonyl E Material

L10 7½ Turns, AWG #22 Copper Wire
PAUL SMITH CO. Coil Form SK-478
3/8" 10-32 Core – Carbonyl E Material

L11 31/6 Turns, AWG #20 Copper Wire
COILCRAFT T-Form [Start at Pin 3(MC1364)]
3/8" 10-32 Core – Carbonyl T Material

L12 21/3 Turns, AWG #20 Copper Wire
Over Bottom End of L11 [Finish at Pin 9 (MC1364)]
3/8" 10-32 Core – Carbonyl T Material

L13 3 1/6 Turns, AWG #20 Copper Wire
Center Tapped.
3/8" 10-32 Core – Carbonyl T Material

FIGURE 13 – SOUND CHANNEL OUTPUT

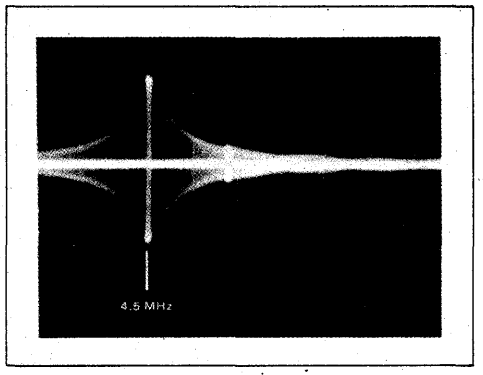


FIGURE 14 – VIDEO CHANNEL OUTPUT

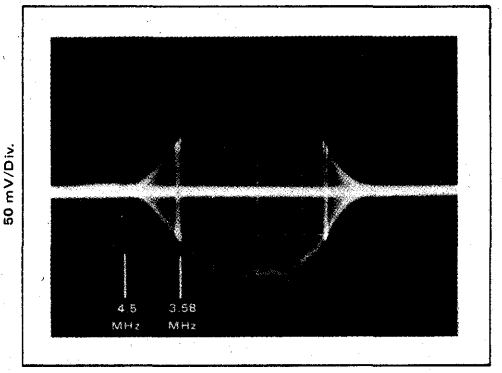
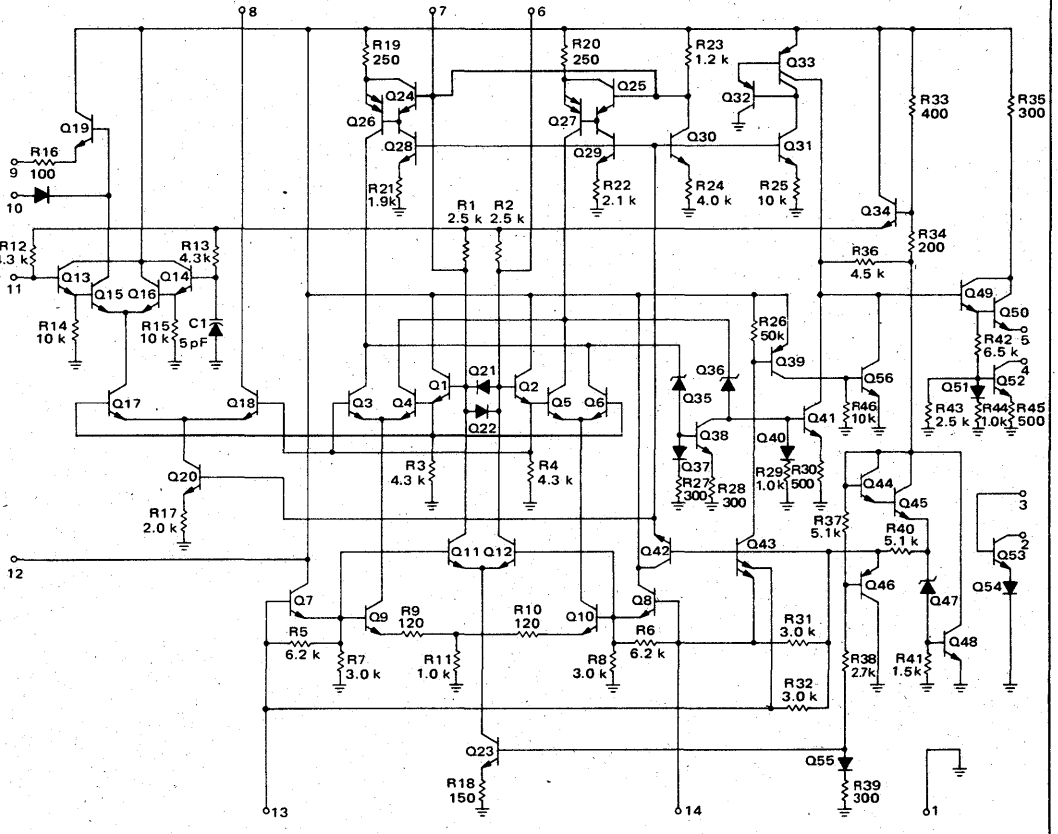


FIGURE 15 – CIRCUIT SCHEMATIC



ORDERING INFORMATION

Device	Temperature Range	Package
MC1344P	0°C to +70°C	Plastic DIP

MC1344

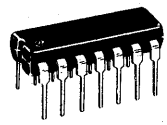
TV SIGNAL PROCESSOR

. . . a monolithic TV circuit with sync separator, advanced noise inversion, AGC comparator, and versatile RF AGC delay amplifier for use in color or monochrome TV receivers.

- Video Internally Delayed for Total Noise Inversion
- Low Impedance, Noise Cancelled Sync Output
- Refined AGC Gate
- Small IF AGC Output Change During RF AGC Interval
- Positive and Negative Going RF AGC Outputs
- Noise Threshold May Be Externally Adjusted
- Time Constants for Sync Separator Externally Chosen
- Stabilized for ±10% Supply Variations

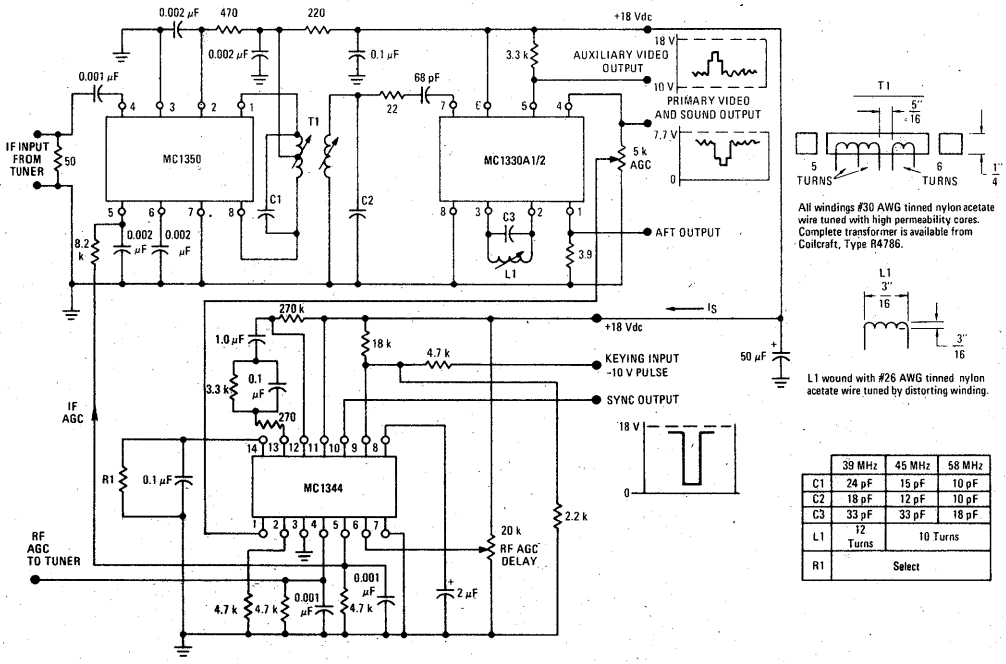
TV SIGNAL PROCESSOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646

FIGURE 1 – TYPICAL MC1344 APPLICATION CIRCUIT



	39 MHz	45 MHz	58 MHz
C1	24 pF	15 pF	10 pF
C2	18 pF	12 pF	10 pF
C3	33 pF	33 pF	18 pF
L1	12 Turns	10 Turns	
R1	Select		

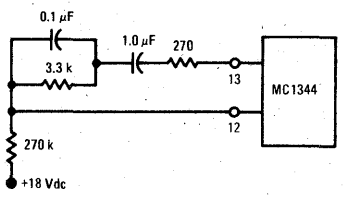
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage (Pin 11)	+22	Vdc
Video Input Voltage (Pin 1)	+10	Vdc
Negative RF AGC Supply Voltage (Pin 3)	-10	Vdc
Gating Voltage (Pin 9)	15	Vp-p
Sync Separator Drive Voltage (Pin 12)	7.0	Vp-p
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +70	°C
Storage Temperature Range	-55 to +150	°C

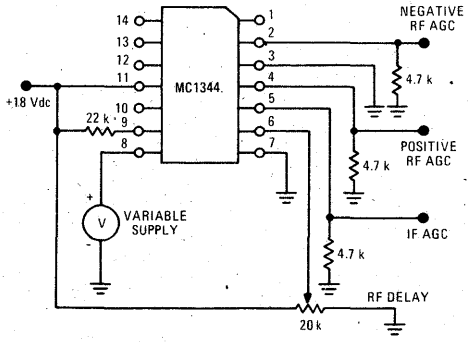
ELECTRICAL CHARACTERISTICS (V_{CC} = +18 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Sync Tip dc Level of Input Signal	3.4	3.9	4.2	Vdc
Temperature Coefficient of Sync Tip (Input)	–	–	1.0	mV/°C
Sync Output Amplitude	–	16	–	Vp-p
Sync Output Impedance	–	–	100	Ohms
Sync Tip to Noise Threshold Separation (Input)	0.45	0.7	0.95	Vdc
IF AGC Voltage Change During RF Interval	–	0.10	0.5	Vdc
Peak AGC Charge Current	–	15	–	mAdc
Peak AGC Discharge Current	–	0.9	–	mAdc
IF AGC Voltage Range	9.0	–	–	Vdc
Positive RF AGC Voltage Range	–	10	–	Vdc
Positive RF AGC Minimum Voltage	0.5	1.5	2.0	Vdc
Negative RF AGC Voltage Range	–	10	–	Vdc
Negative RF AGC Maximum Voltage	9.0	10.2	12	Vdc
Total Supply Current, I_S (Circuit of Figure 1)	–	22	–	mAdc

NORMAL SYNC SEPARATION NETWORK



TEST CIRCUIT FOR AGC AMPLIFIER MEASUREMENTS



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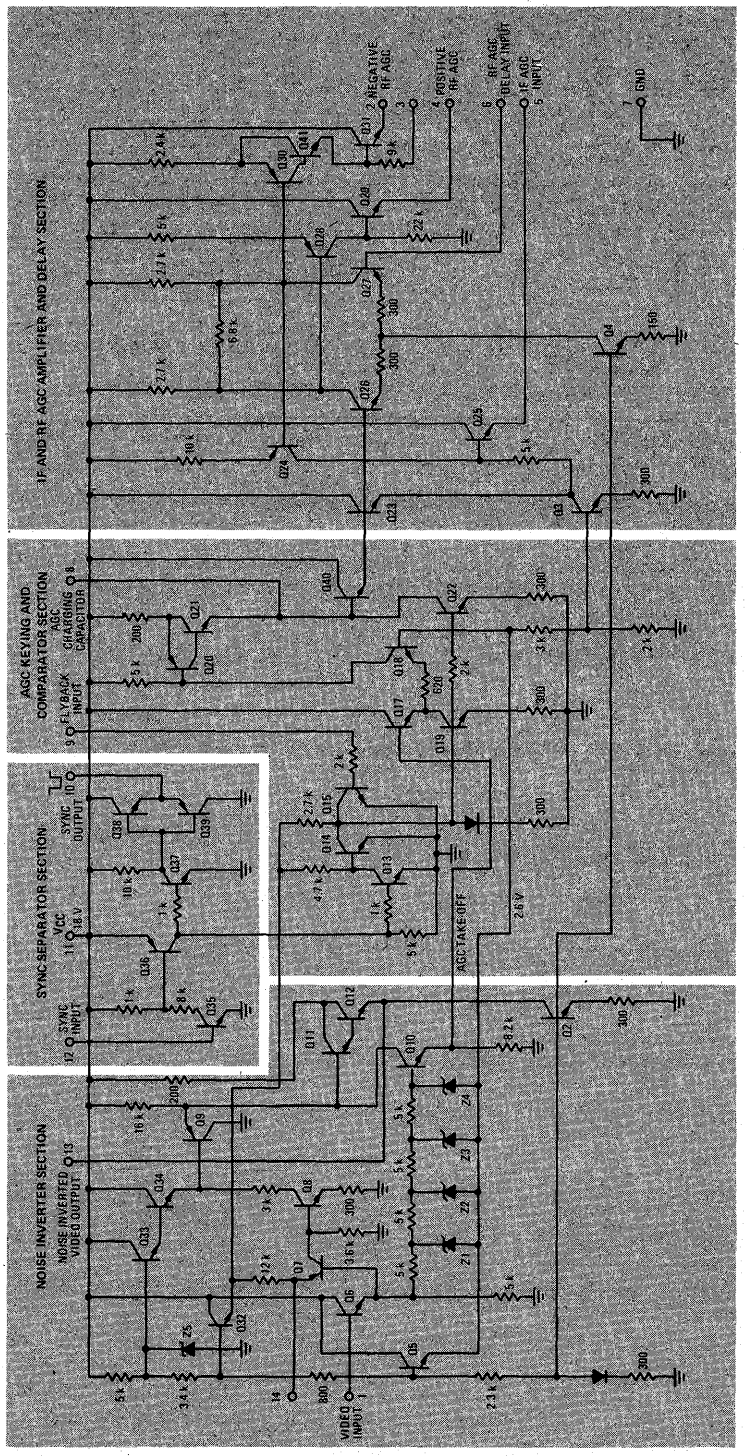
CIRCUIT SCHEMATIC



ORDERING INFORMATION

Device	Temperature Range	Package
MC1349P	0°C to +70°C	Plastic DIP

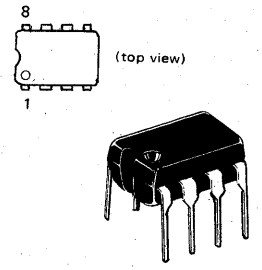
MC1349P

IF AMPLIFIER

. . . an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and television applications over the temperature range 0 to +70°C.

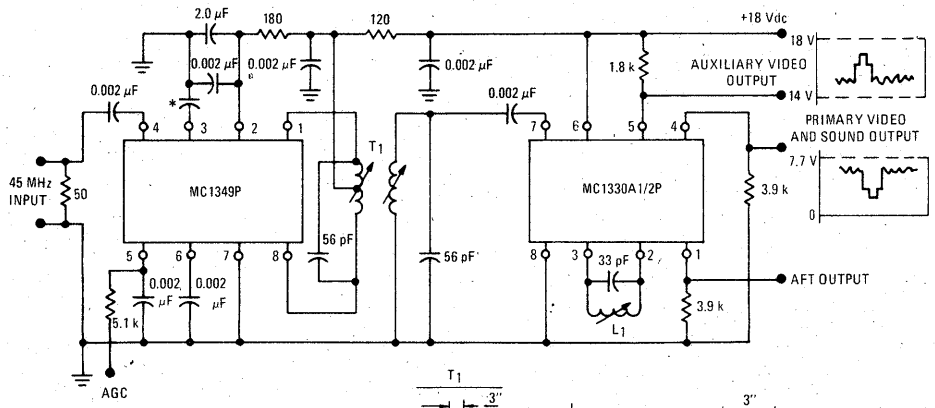
- Power Gain – 60 dB typ at 45 MHz (pin 3 open)
  – 56 dB typ at 58 MHz (pin 3 open)
  – 61 dB typ at 45 MHz (pin 3 bypassed)
  – 59 dB typ at 58 MHz (pin 3 bypassed)
- AGC Range – 80 dB typ, dc to 45 MHz
- High Output Impedance
- Low Reverse Transfer Admittance
- 15-Volt Operation, Single-Polarity Power Supply
- Improved Noise Figure versus AGC

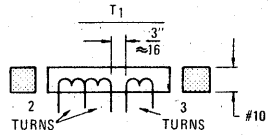
IF AMPLIFIER
SILICON MONOLITHIC INTEGRATED CIRCUIT

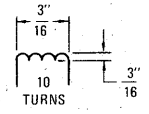


PLASTIC PACKAGE
CASE 626

FIGURE 1 – TYPICAL APPLICATION OF MC1349P VIDEO IF AMPLIFIER and MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT







All windings #22 AWG tinned nylon acetate wire tuned with Coilcraft #61 slugs, size 10-32, or equivalent.

L1 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

*See Note 1 (page 3), and C4, Parts List (page 4) of this specification.

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted).

Rating	Value	Unit
Power Supply Voltage (V_{CC1})	+18	Vdc
Output Supply Voltage (V_{CC2})	+18	Vdc
AGC Supply Voltage	$\leq V_{CC1}$ (pin 2)	Vdc
Differential Input Voltage	5.0	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

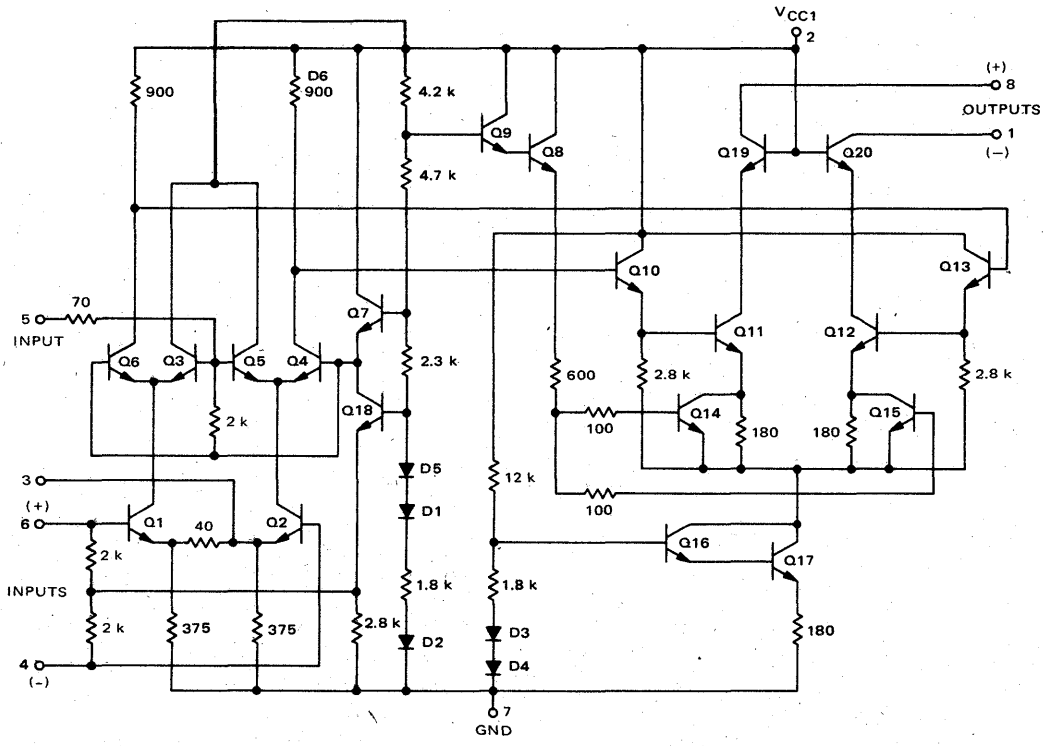
ELECTRICAL CHARACTERISTICS (V_{CC1} = +12 Vdc [pin 2], V_{CC2} = +15 Vdc [pins 1 and 8], T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
AGC Range, 45 MHz (5.0 V to 7.5 V) (Figure 3)	70	80	–	dB
Power Gain (Pin 5 grounded via 5.1 kΩ resistor, input pin 4) f = 45 MHz, BW (3 dB) = 4.5 MHz, Tuned Input, pin 3 open Untuned Input, pin 3 bypassed f = 58 MHz, BΩ (3 dB) = 4.5 MHz, Tuned Input, pin 3 open Untuned Input, pin 3 bypassed	 52 – – –	 60 61 56 59	 – – – –	dB
Maximum Differential Output Voltage Swing	–	6.0	–	Vp-p
Output Stage Current (pins 1 and 8)	–	9.0	–	mA
Amplifier Current (pin 2)	–	15	20	mAdc
Power Dissipation	–	315	400	mW
Noise Figure f = 45 MHz, Tuned Input, pin 3 open, Gain Reduction = 15 dB	–	8.5	–	dB

DESIGN PARAMETERS (V_{CC1} = +12 Vdc, [pin 2], V_{CC2} = +15 Vdc, [pins 1 and 8], T_A = +25°C unless otherwise noted.)

Parameter	Symbol	Frequency		Unit
		45 MHz	58 MHz	
Single-Ended Input Admittance, input pin 4, AGC min Pin 3 open Pin 3 open Pin 3 bypassed Pin 3 bypassed	 g11 b11 g11 b11	 0.74 1.9 4.1 6.5	 0.95 2.4 5.4 6.9	mmhos
Differential Output Admittance, AGC max	 g22 b22	 5.5 270	 8.3 360	μmhos
Reverse Transfer Admittance (magnitude)		1.5	2.0	μmhos
Forward Transfer Admittance Magnitude, pin 3 open Angle (0 dB AGC), pin 3 open Magnitude, pin 3 bypassed Angle (0 dB AGC), pin 3 bypassed		 520 100 1020 120	 400 130 800 400	 mmhos degrees mmhos degrees
Single-Ended Input Capacitance, AGC min Pin 3 open Pin 3 bypassed		 6.8 2.3	 6.7 20	pF
Differential Output Capacitance (AGC max)		1.0	1.0	pF

FIGURE 2 – CIRCUIT SCHEMATIC



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GENERAL INFORMATION

The MC1349P is an improved version of the MC1350P. Featuring higher gain, a lower noise figure, and greater AGC range; in addition, an emitter of the input amplifier is available for bypassing. This provides a low input impedance with good gain, useful for untuned input configurations.

Both input and output IF amplifier sections are gain-controlled in the MC1349P, with the input amplifier also serving as an AGC amplifier for the output section. During the initial part of AGC gain reduction, the gain of the input amplifier decreases only a few dB while the output section decreases 15 dB; further AGC acts upon the input section. Although the gain reduction curve was taken with 5.1 kilohms at pin 5, higher series resistance can be used to reduce the voltage and temperature sensitivity of the AGC. Pin 5 currents are shown on the AGC curve, see Figure 10.

In use, it is important to bypass pin 2, both for IF frequencies and for low frequencies, (as shown in the test circuits). This is due to the dual function of the input amplifier. If replacing MC-1350P take precaution not to ground pin 3, (not used in the MC1350P). Due to the significantly higher gain of the MC1349P, extra care in layout should be exercised.

NOTE 1: The references to bypasses at pin 3 do not give specific values (C4, see Figures 1 and 4). In all cases, measurements were taken with a bypass at a standard value as near as possible to series resonance. The values are dependent on test frequency and circuit layout. Fully bypassing pin 3 reduces the input signal handling capability before distortion from over 100 mV(RMS) to approximately 25 mV(RMS). C4 = 0.002 μF at f = 45 MHz is a typical value for printed circuit applications.

TEST CIRCUITS

FIGURE 3 – TUNED INPUT
(PIN 3 OPEN)

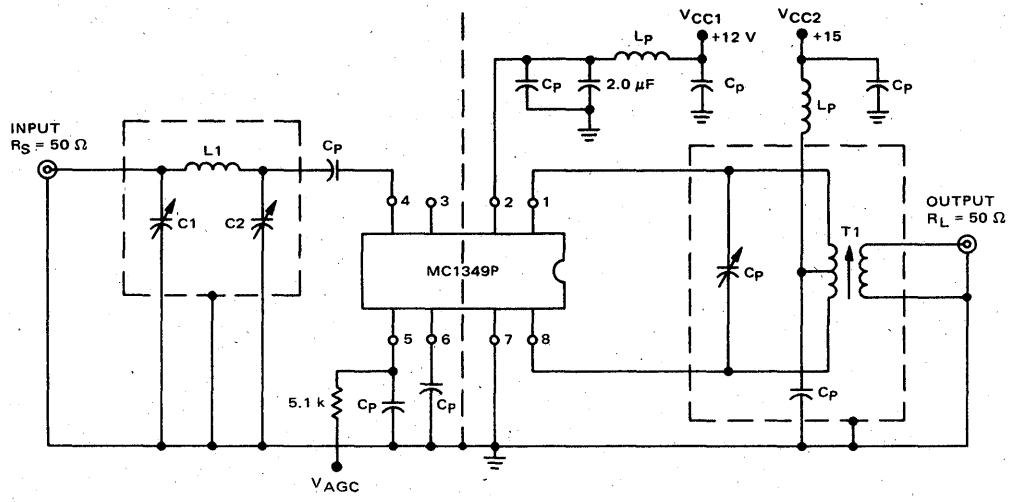
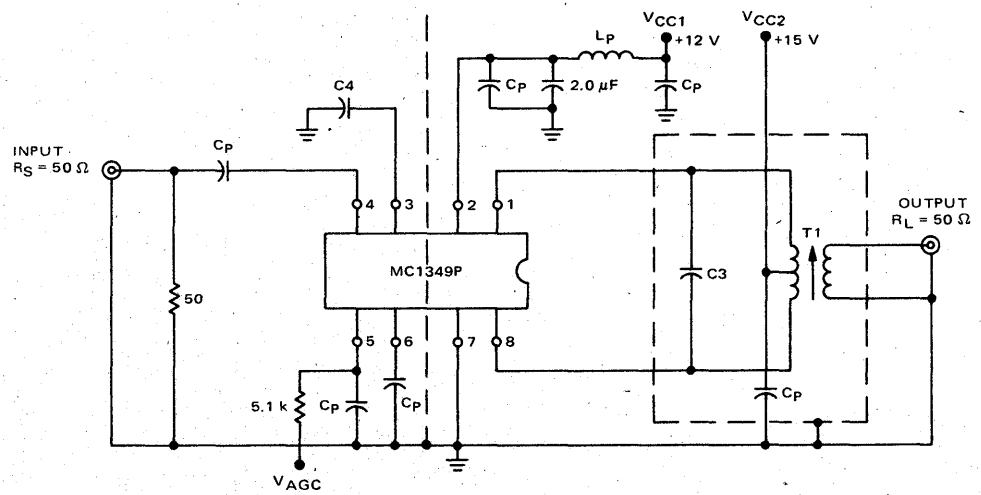


FIGURE 4 – UNTUNED INPUT
(PIN 3 BYPASSED TO GROUND)



PARTS LIST

COMPONENT	45 MHz	58 MHz
C1	8-60 pF	50-100 pF
C2	3-35 pF	3-35 pF
C3	1-7.0 pF	1-7.0 pF
C4	82-470 pF	82-470 pF
C_P	0.0015 μF	0.001 μF
L1	0.84 μH	0.33 μH
L_P	10 μH	10 μH

T1 Primary 14 turns center-tapped
Secondary 2½ turns (45 MHz tuned input pin #3 open) 1½ turns (all other fixtures) wound over primary
Wire: #26 AWG tinned nylon acetate wound on 1/4" diameter coil form
Core: Arnold Type TH, 1/2" long or equivalent.

TYPICAL CHARACTERISTICS

FIGURE 5 – SINGLE-ENDED INPUT ADMITTANCE (PIN 3 OPEN)

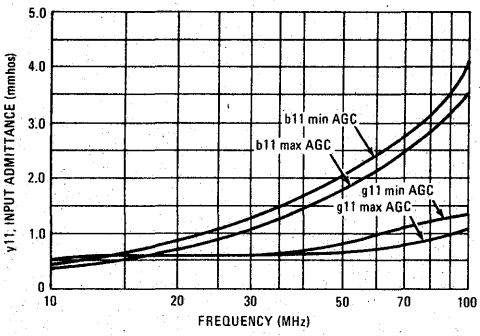


FIGURE 6 – SINGLE-ENDED INPUT ADMITTANCE (PIN 3 BYPASSED TO GROUND)

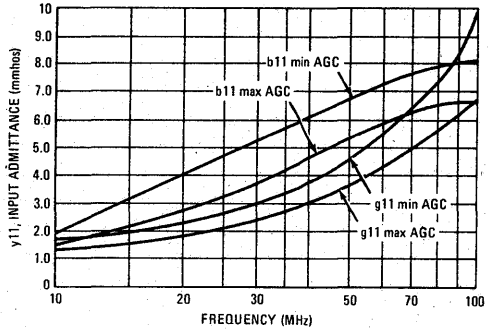


FIGURE 7 – SINGLE-ENDED FORWARD TRANSFER ADMITTANCE

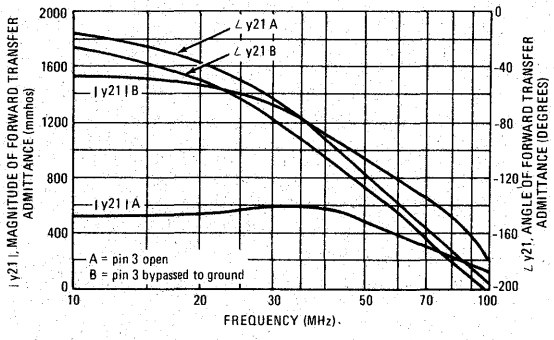


FIGURE 8 – DIFFERENTIAL OUTPUT ADMITTANCE (MAXIMUM AGC)

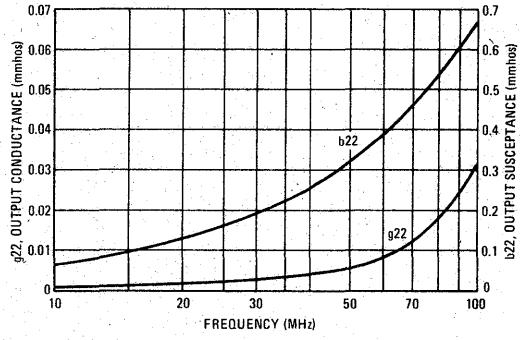


FIGURE 9 – NOISE FIGURE

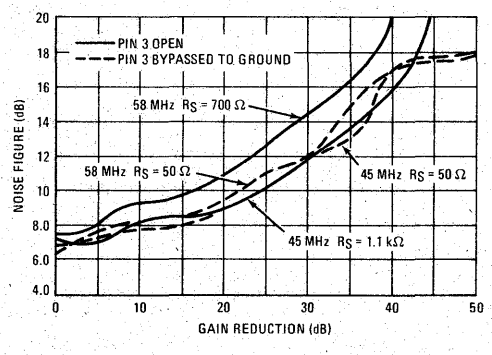
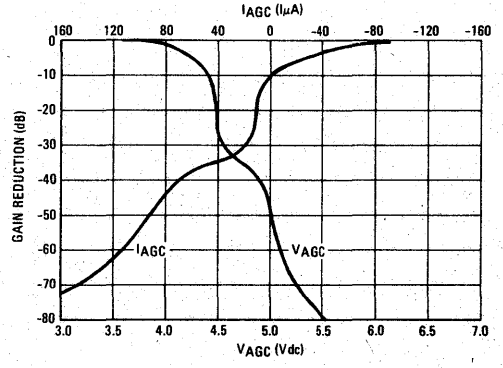


FIGURE 10 – GAIN REDUCTION



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ORDERING INFORMATION

Device	Temperature Range	Package
MC1350P	0°C to +75°C	Plastic DIP

MC1350

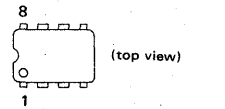
MONOLITHIC IF AMPLIFIER

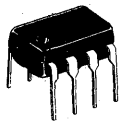
. . . an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and TV over the temperature range 0 to +75°C. The MC1352 is similar in design but has a keyed-AGC amplifier as an integral part of the same chip.

- Power Gain – 50 dB typ at 45 MHz,
  – 48 dB typ at 58 MHz
- AGC Range – 60 dB min, dc to 45 MHz
- Nearly Constant Input and Output Admittance Over the Entire AGC Range
- y_{21} Constant (-3.0 dB) to 90 MHz
- Low Reverse Transfer Admittance – << 1.0 μmho typ
- 12-Volt Operation, Single-Polarity Power Supply

IF AMPLIFIER

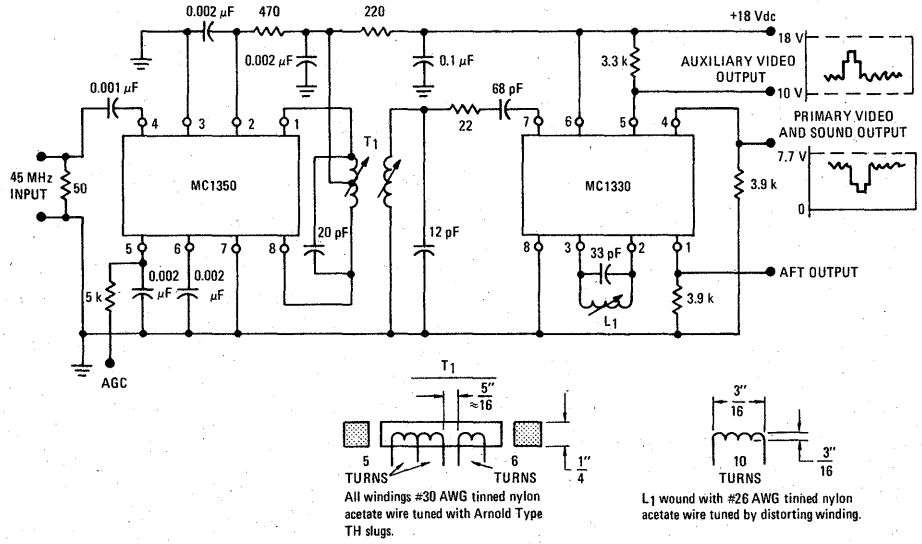
MONOLITHIC SILICON INTEGRATED CIRCUIT





PLASTIC PACKAGE
CASE 626

FIGURE 1 – TYPICAL MC1350 VIDEO IF AMPLIFIER and MC1330 LOW-LEVEL VIDEO DETECTOR CIRCUIT



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+18	Vdc
Output Supply Voltage	V_1, V_8	+18	Vdc
AGC Supply Voltage	V_{AGC}	V^+	Vdc
Differential Input Voltage	V_{in}	5.0	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above 25°C	P_D	 625 5.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C

ELECTRICAL CHARACTERISTICS (V^+ = +12 Vdc; T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
AGC Range, 45 MHz (5.0 V to 7.0 V) (Figure 1)		60	68	–	dB
Power Gain (Pin 5 grounded via a 5.1 kΩ resistor)	A_p				dB
f = 58 MHz, BW = 4.5 MHz } See Figure 5		–	48	–	
f = 45 MHz, BW = 4.5 MHz } See Figure 5		46	50	–	
f = 10.7 MHz, BW = 350 kHz } See Figure 6		–	58	–	
f = 455 kHz, BW = 20 kHz } See Figure 6		–	62	–	
Maximum Differential Voltage Swing	V_o				V_{p-p}
0 dB AGC		–	20	–	
-30 dB AGC		–	8.0	–	
Output Stage Current (Pins 1 and 8)	$I_1 + I_8$	–	5.6	–	mA
Total Supply Current (Pins 1, 2 and 8)	I_S	–	14	17	mAdc
Power Dissipation	P_D	–	168	204	mW

DESIGN PARAMETERS, Typical Values (V^+ = +12 Vdc, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Frequency				Unit
		455 kHz	10.7 MHz	45 MHz	58 MHz	
Single-Ended Input Admittance	g_{11} b_{11}	0.31 0.022	0.36 0.50	0.39 2.30	0.5 2.75	mmhos
Input Admittance Variations with AGC (0 to 60 dB)	Δg_{11} Δb_{11}	– –	– –	60 0	– –	μmhos
Differential Output Admittance	g_{22} b_{22}	4.0 3.0	4.4 110	30 390	60 510	μmhos
Output Admittance Variations with AGC (0 to 60 dB)	Δg_{22} Δb_{22}	– –	– –	4.0 90	– –	μmhos
Reverse Transfer Admittance (Magnitude)	$\lvert y_{12} \rvert$	$\ll$1.0	$\ll$1.0	$\ll$1.0	$\ll$1.0	μmho
Forward Transfer Admittance						
Magnitude	$\lvert y_{21} \rvert$	160	160	200	180	mmhos
Angle (0 dB AGC)	$< y_{21}$	-5.0	-20	-80	-105	degrees
Angle (-30 dB AGC)	$< y_{21}$	-3.0	-18	-69	-90	degrees
Single-Ended Input Capacitance	C_{in}	7.2	7.2	7.4	7.6	pF
Differential Output Capacitance	C_o	1.2	1.2	1.3	1.6	pF

FIGURE 2 – TYPICAL GAIN REDUCTION
(Figures 5 and 6)

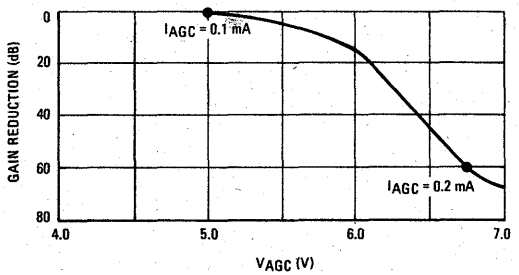
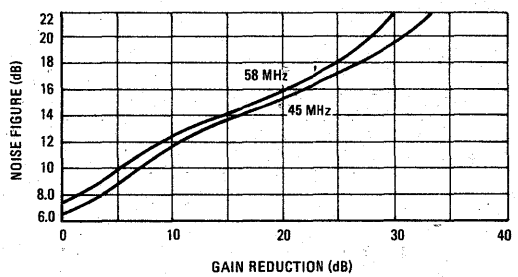


FIGURE 3 – NOISE FIGURE
(Figure 5)



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GENERAL OPERATING INFORMATION

The input amplifiers (Q1 and Q2) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac) with identical results. Terminals 4 and 6 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q4 and Q5 causing these transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q3 and Q6. The output amplifiers are supplied from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant. Collector voltage for the output amplifier must be supplied through a center-tapped tuning coil to Pins 1 and 8. The 12-volt supply (V^+) at Pin 2 may be used for this purpose, but output admittance remains more nearly constant if a separate 15-volt supply (V^{++}) is used, because the base voltage on the output amplifier varies with AGC bias.

FIGURE 4 – CIRCUIT SCHEMATIC

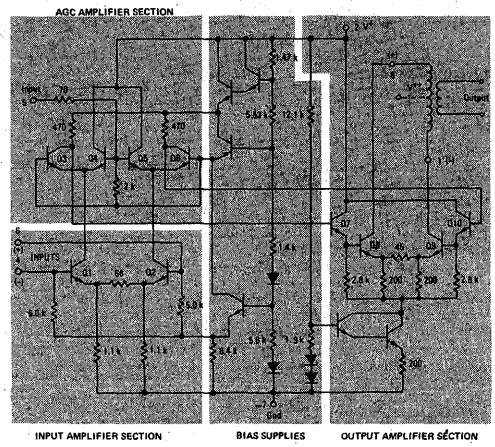
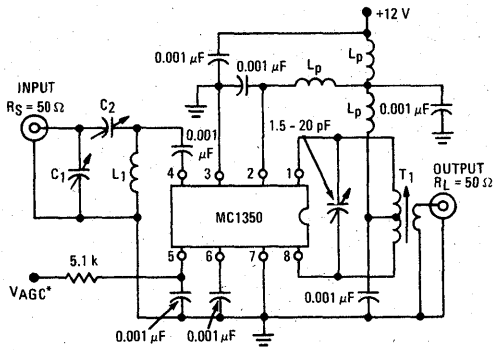


FIGURE 5 – POWER GAIN, AGC and NOISE FIGURE TEST CIRCUIT (45 MHz and 58 MHz)

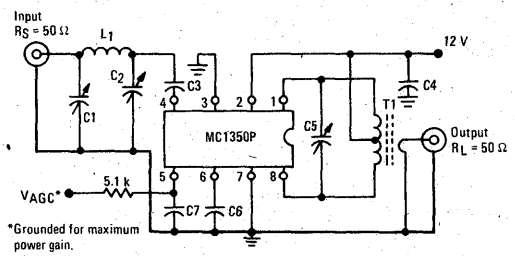


*Connect to ground for maximum power gain test.
All power-supply chokes (L_p), are self-resonate at input frequency. $L_p \geq 20$ kΩ
See Figure 10 for frequency response curve.

L_1 @ 45 MHz = 7 1/4 Turns on a 1/4" coil form.
@ 58 MHz = 6 Turns on a 1/4" coil form
T_1 Primary Winding = 18 Turns on a 1/4" coil form, center-tapped
Secondary Winding = 2 Turns centered over Primary Winding @ 45 MHz
= 1 Turn @ 58 MHz
Slug = Arnold TH Material 1/2" Long

	45 MHz		58 MHz	
L_1	0.4 μH	Q ≥ 100	0.3 μH	Q ≥ 100
T_1	1.3 -3.4 μH	Q ≥ 100 @ 2 μH	1.2 -3.8 μH	Q ≥ 100 @ 2 μH
C_1	50 - 160 pF		8 - 60 pF	
C_2	8 - 60 pF		3 - 35 pF	

FIGURE 6 – POWER GAIN and AGC TEST CIRCUIT (455 kHz and 10.7 MHz)



*Grounded for maximum power gain.

Note 1. Primary: 120 μH (center-tapped)
Q_u = 140 at 455 kHz
Primary: Secondary turns ratio ≈ 13

Note 2. Primary: 6.0 μH
Primary winding = 24 turns #36 AWG (close-wound on 1/4" dia. form)
Core = Arnold Type TH or equiv.
Secondary winding = 1-1/2 turns #36 AWG, 1/4" dia. (wound over center-tap)

	Frequency	
Component	455 kHz	10.7 MHz
C1	–	80–450 pF
C2	–	5.0–80 pF
C3	0.05 μF	0.001 μF
C4	0.05 μF	0.05 μF
C5	0.001 μF	36 pF
C6	0.05 μF	0.05 μF
C7	0.05 μF	0.05 μF
L1	–	4.6 μH
T1	Note 1	Note 2

TYPICAL CHARACTERISTICS

(V^+ = 12 V, T_A = +25°C)

FIGURE 7 – SINGLE-ENDED INPUT ADMITTANCE

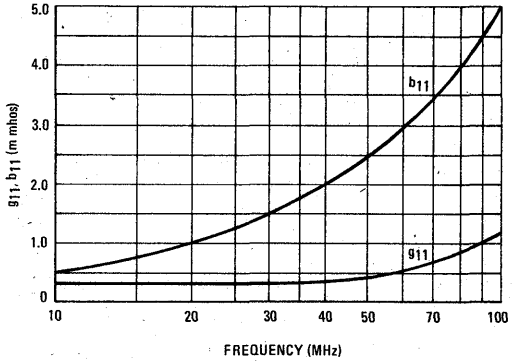


FIGURE 8 – FORWARD TRANSFER ADMITTANCE

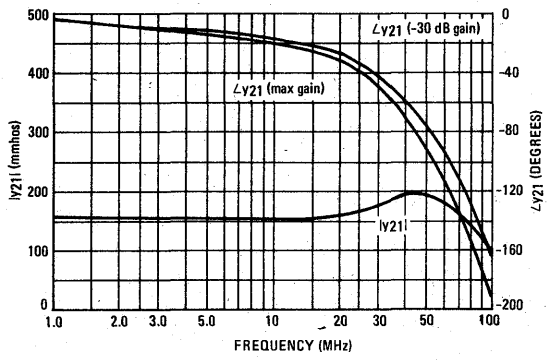


FIGURE 9 – DIFFERENTIAL OUTPUT ADMITTANCE

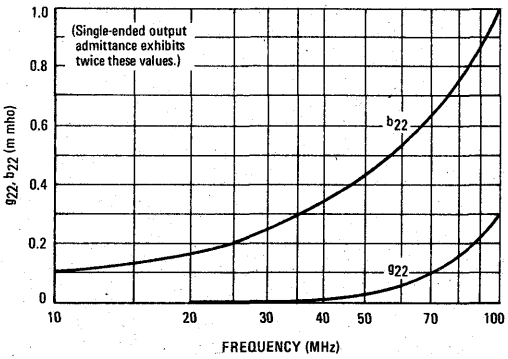


FIGURE 10 – TEST CIRCUIT RESPONSE CURVE (45 and 58 MHz)

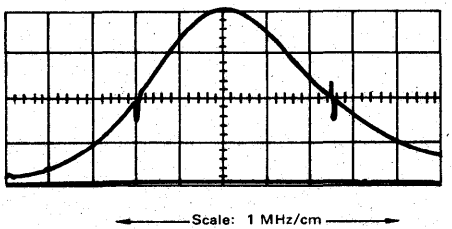
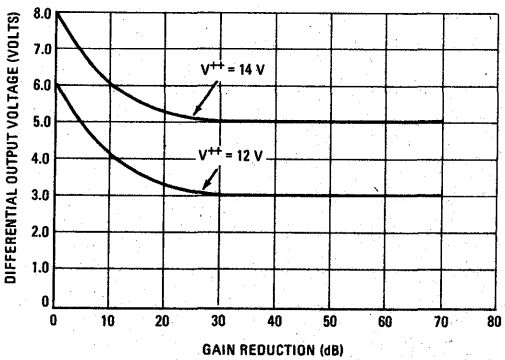


FIGURE 11 – DIFFERENTIAL OUTPUT VOLTAGE



For additional information see "A High-Performance Monolithic IF Amplifier Incorporating Electronic Gain Control", by W. R. Davis and J. E. Solomon, IEEE Journal on Solid State Circuits, December 1968.

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ORDERING INFORMATION

Device	Temperature Range	Package
MC1351P	0°C to +75°C	Plastic DIP
MC1351PQ	0°C to +75°C	Plastic

MC1351

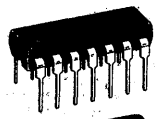
WIDE-BAND FM-AMPLIFIER; LIMITER, DETECTOR, AND AUDIO AMPLIFIER

. . . designed for IF limiting, detection, audio preamplifier and driver for the sound portion of a TV receiver.

- Excellent Limiting with 80 μV(rms) Input Signal typ
- Large Output-Voltage Swing – to 3.5 V(rms) typ
- High IF Voltage Gain – 65 dB typ
- Zener Power-Supply Regulation Built-In
- Short-Circuit Protection
- A Coincidence Discriminator that Requires Only One RLC Phase Shift Network
- Preamplifier to Drive a Single External-Transistor Class-A Audio-Output Stage

TV SOUND CIRCUIT

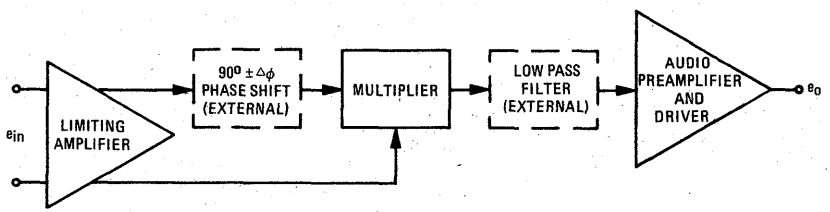
MONOLITHIC SILICON INTEGRATED CIRCUIT



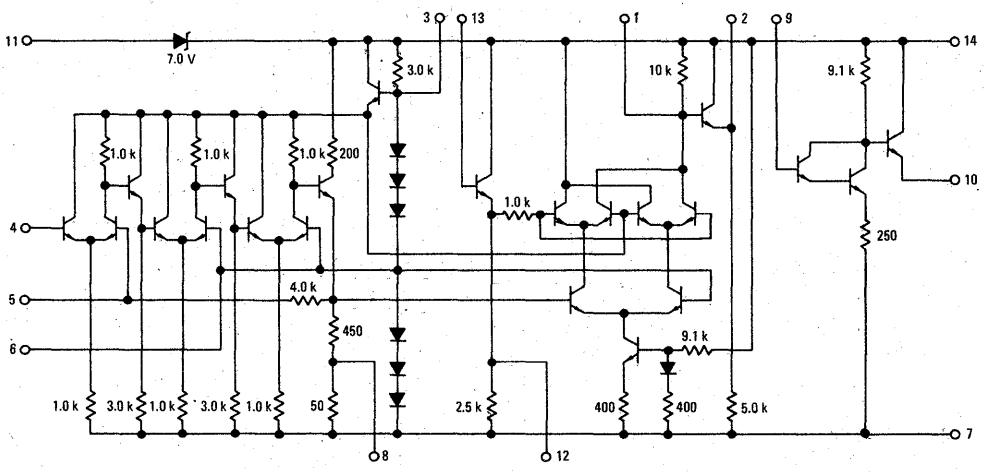
P SUFFIX
PLASTIC PACKAGE
CASE 646

PQ SUFFIX
PLASTIC PACKAGE
CASE 647

BLOCK DIAGRAM



CIRCUIT SCHEMATIC



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MAXIMUM RATINGS (T_A = +25° unless otherwise noted)

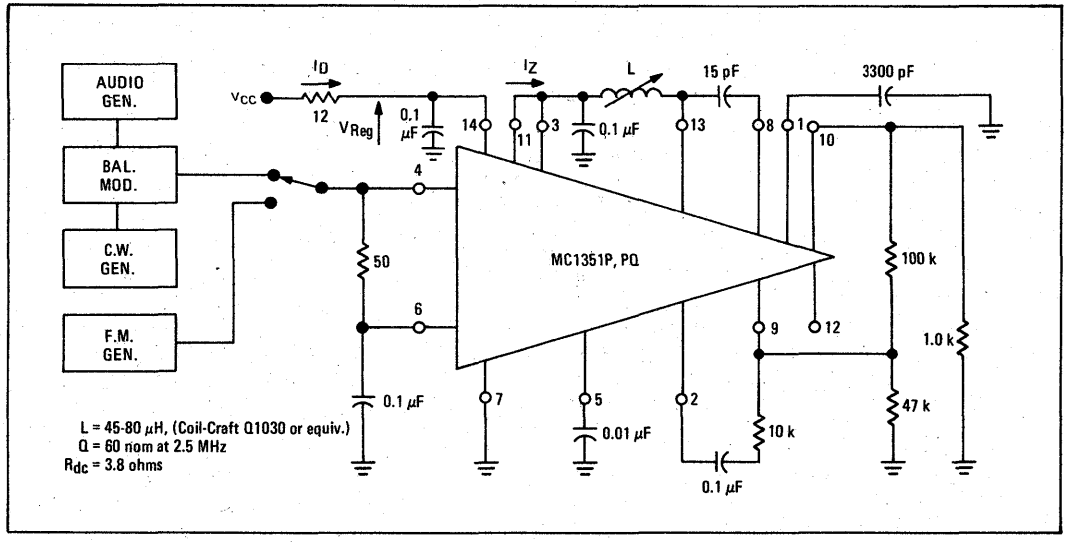
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+16	Vdc
Input Voltage	V_{in}	0.7	V(rms)
Power Dissipation (Package Limitation) Plastic Packages Derate above +25°C	 P_D $1/\theta_{JA}$	 625 5.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = +25°C, f = 4.5 MHz, Deviation = ±25 kHz unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Input Voltage (-3.0 dB Limiting)	–	80	160	μV(rms)
AM Rejection (V_{in} = 20 mV(rms), AM = 30%) (See Note 1) AMR = 20 log V_{OFM}/V_{OAM} { f = 4.5 MHz, Deviation = ±25 kHz, Q_L = 24 { f = 5.5 MHz, Deviation = ±50 kHz, Q_L = 30	 – –	 45 45	 – –	dB
Total Harmonic Distortion (Q_L = 24) (See Note 1) (7.5 kHz Deviation)	–	1.0	–	%
Maximum Undistorted Audio Output Voltage (Pin 10) (See Note 1) (Audio Gain Adjusted Externally) (Q = 24)	–	3.5	–	V(rms)
Recovered Audio (Pin 2) (See Note 1) (f = 4.5 MHz, Deviation = ±25 kHz, Q_L = 24) (f = 5.5 MHz, Deviation = ±50 kHz, Q_L = 30)	 0.35 –	 0.50 0.80	 – –	V(rms)
Audio Preamplifier Open Loop Gain	–	25	–	dB
IF Voltage Gain	–	65	–	dB
Parallel Input Resistance	–	9.0	–	kΩ
Parallel Input Capacitance	–	6.0	–	pF
Nominal Zener Voltage (I_Z = 5.0 mAdc)	–	11.6	–	Vdc
Power Supply Current (I_Z = 5.0 mAdc)	–	31	–	mAdc
Power Dissipation (I_Z = 5.0 mAdc)	–	300	375	mW

Note 1: Q_L is loaded circuit Q.

FIGURE 1 – TEST CIRCUIT (V_{CC} = +12 Vdc, T_A = +25°C)



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TYPICAL CHARACTERISTICS

FIGURE 2 – DETECTED AUDIO OUTPUT versus INPUT LEVEL @ f =4.5 MHz, ±25 kHz DEVIATION

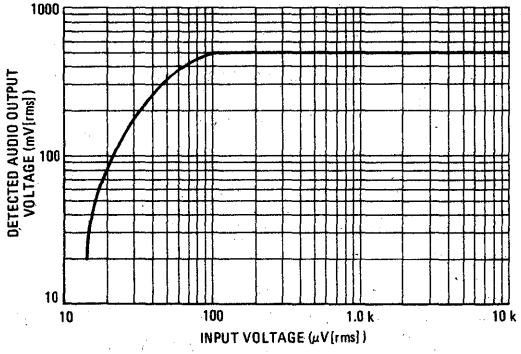

FIGURE 3 – DETECTED AUDIO OUTPUT versus INPUT LEVEL @ f = 5.5 MHz, ±50 kHz DEVIATION

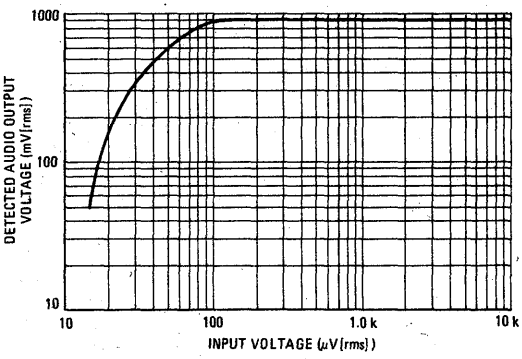

FIGURE 4 – DETECTOR "S" CURVE @ f = 4.5 MHz, BW = 200 kHz, Q = 24

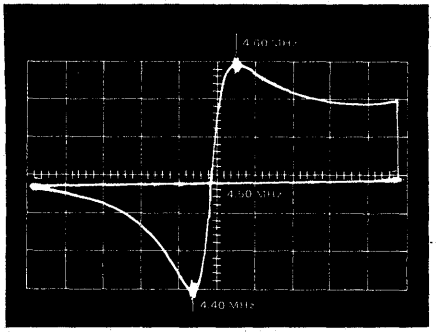

FIGURE 5 – DETECTOR "S" CURVE @ f = 5.5 MHz, BW = 220 kHz, Q = 30

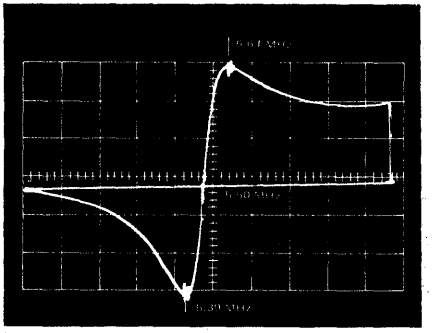

FIGURE 6 – IF VOLTAGE GAIN versus FREQUENCY

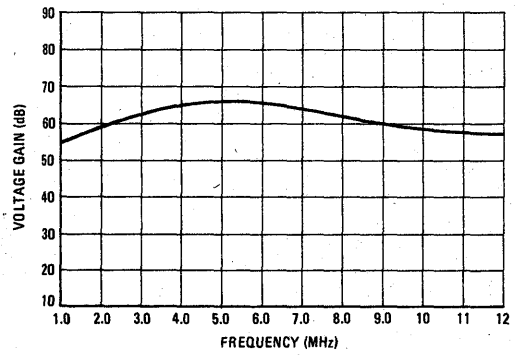

FIGURE 7 – AM REJECTION

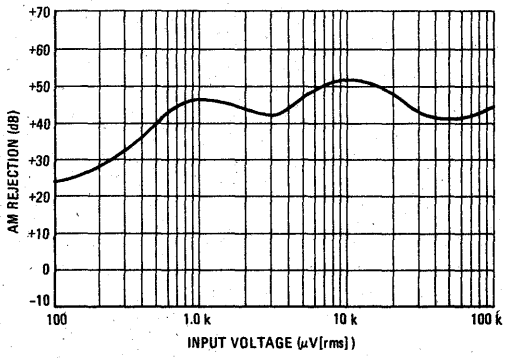

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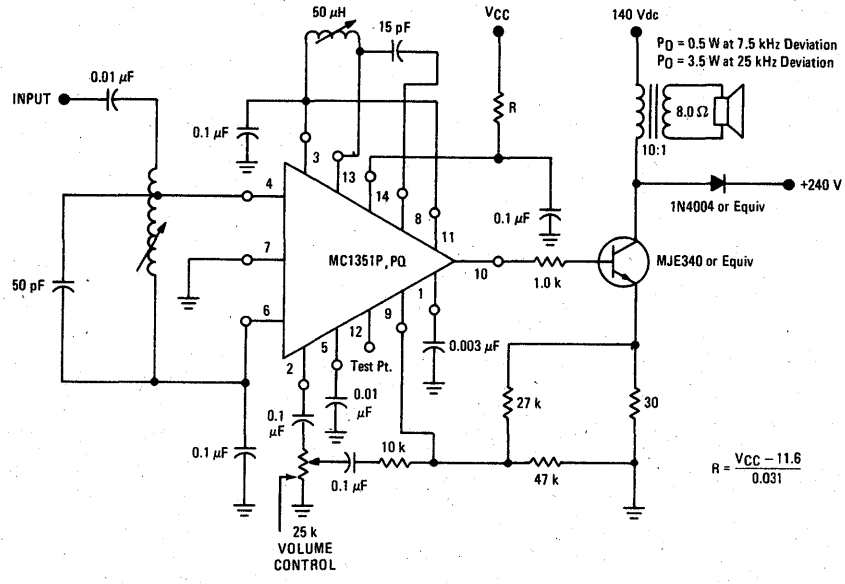
FIGURE 8 – 4.5 MHz TYPICAL APPLICATION



7

ORDERING INFORMATION

Device	Temperature Range	Package
MC1352P	0°C to +70°C	Plastic DIP
MC1352PQ	0°C to +70°C	Plastic

MC1352

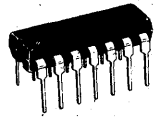
TV VIDEO IF AMPLIFIER WITH AGC AND KEYER CIRCUIT

. . . a monolithic IF amplifier with a complete gated wide-range AGC system for use as the 1st and 2nd IF stages and AGC keyer and amplifier in color or monochrome TV receivers.

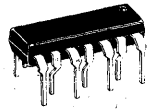
- Power Gain at 45 MHz, 52 dB typ
- Extremely Low Reverse-Transfer Admittance – << 1.0 μmho typ
- Nearly Constant Input and Output Admittance Over AGC Range
- Single-Polarity Power-Supply Operation
- High-Gain Gated AGC System for Either Positive or Negative-Going Video Signals
- Control Signal Available for Delayed AGC of Tuner

TV VIDEO IF AMPLIFIER WITH AGC AND KEYER CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

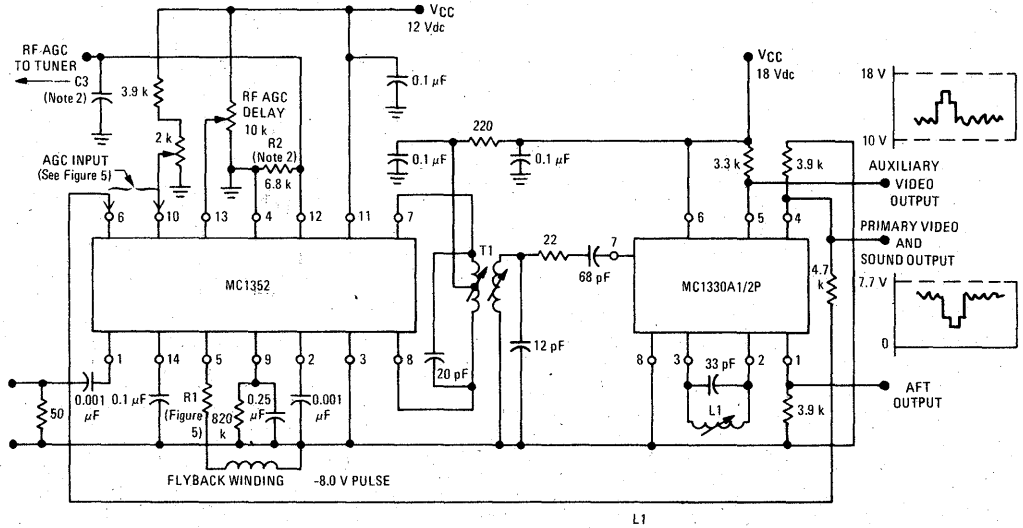


P SUFFIX
PLASTIC PACKAGE
CASE 646

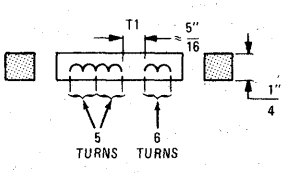


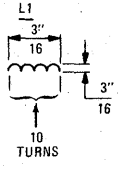
PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – TYPICAL VIDEO IF AMPLIFIER APPLICATION



All windings #30 AWG tinned nylon acetate wire tuned with Arnold Type TH slugs.





Wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

MAXIMUM RATINGS (Voltages referenced to pin 4, ground; T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply (Pin 11)	+18	Vdc
Output Supply (Pins 7 and 8)	+18	Vdc
Signal Input Voltage (Pin 1 or 2, other pin ac grounded)	10	V_{p-p}
AGC Input Voltage (Pin 6 or 10, other pin ac grounded)	+6.0	Vdc
Gating Voltage, Pin 5	+10, -20	Vdc
Power Dissipation Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, Voltages referenced to pin 4, ground; T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
AGC Range	–	75	–	dB
Power Gain f = 35 MHz or 45 MHz f = 58 MHz	 – –	 52 50	 – –	dB
Maximum Differential Output Voltage Swing 0 dB AGC -30 dB AGC	 – –	 16.8 8.4	 – –	V_{p-p}
Voltage Range for RF-AGC at Pin 12 Maximum Minimum	 – –	 7.0 0.2	 – –	Vdc
IF Gain Change Over RF-AGC Range	–	10	–	dB
Output Stage Current ($I_7 + I_8$)	–	5.7	–	mAdc
Total Supply Current ($I_7 + I_8 + I_{11}$)	–	27	31	mAdc
Total Power Dissipation	–	325	370	mW

DESIGN PARAMETERS, TYPICAL VALUES (V_{CC} = 12 Vdc, T_A = +25°C unless otherwise noted.)

Parameters	Symbol	f = 35 MHz	f = 45 MHz	f = 58 MHz	Unit
Single-Ended Input Admittance	g_{11} b_{11}	0.55 2.25	0.70 2.80	1.1 3.75	mmhos
Input Admittance Variations with AGC (0 to 60 dB)	Δg_{11} Δb_{11}	50 0	60 0	– –	μmhos
Differential Output Admittance	g_{22} b_{22}	20 430	40 570	75 780	μmhos
Output Admittance Variations with AGC (0 to 60 dB)	Δg_{22} Δb_{22}	3.0 80	4.0 100	– –	μmhos
Reverse Transfer Admittance	$\lvert y_{12} \rvert$	$\ll$1.0	$\ll$1.0	$\ll$1.0	μmho
Forward Transfer Admittance Magnitude Angle (0 dB AGC) Angle (-30 dB AGC)	 $\lvert y_{12} \rvert$ $\angle y_{21}$ $\angle y_{21}$	 260 -73 -52	 240 -100 -72	 210 -135 -96	 mmhos degrees
Single-Ended Input Capacitance	–	9.5	10	10.5	pF
Differential Output Capacitance	–	2.0	2.0	2.5	pF

7

FIGURE 2 – CIRCUIT SCHEMATIC

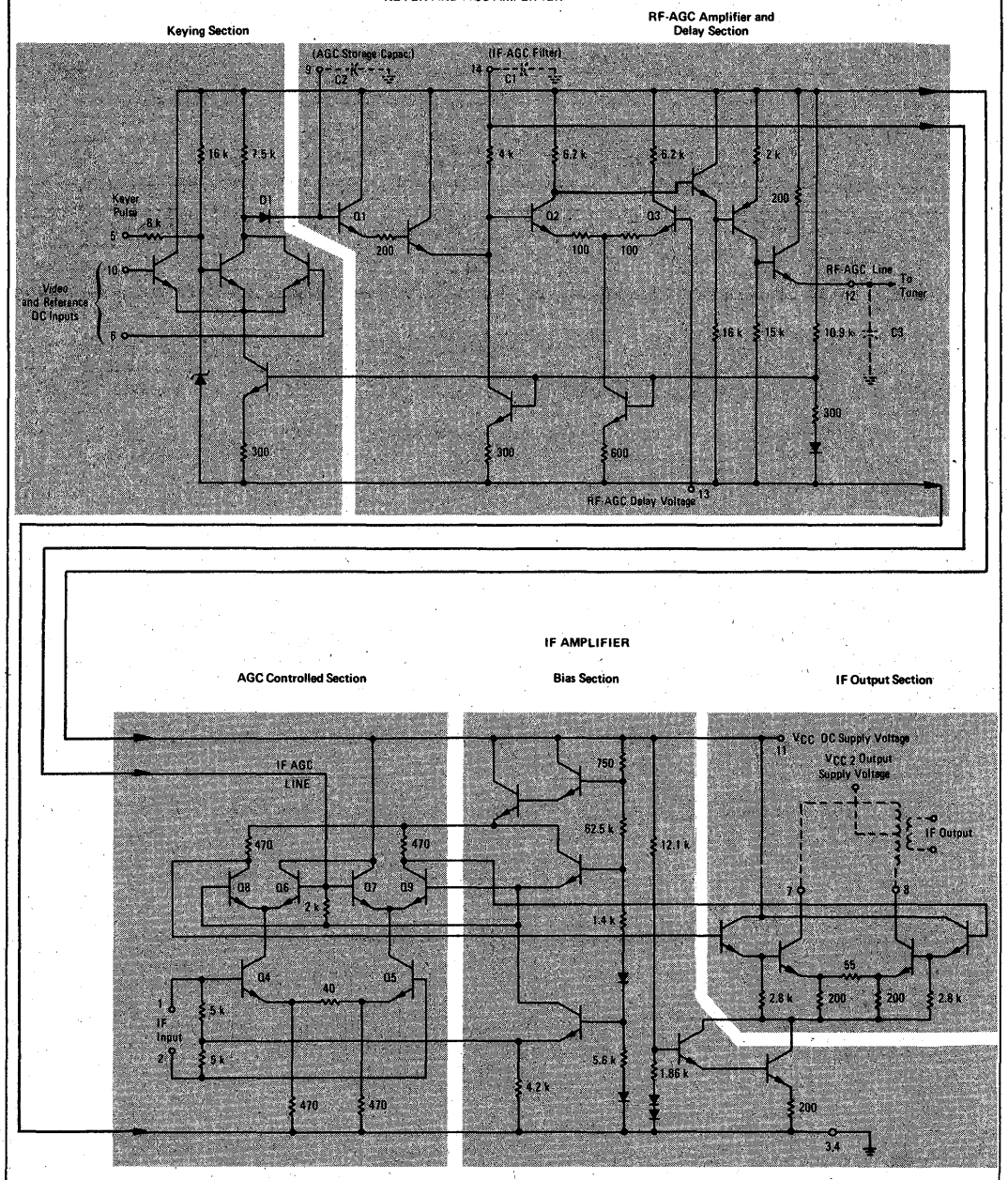


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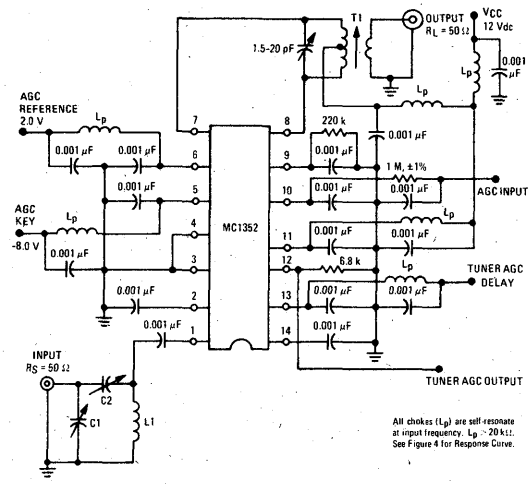
FIGURE 3 – POWER GAIN, AGC AND NOISE TEST CIRCUIT



	35 and 45 MHz		58 MHz	
L1	0.4 μH	Q > 100	0.3 μH	Q > 100
T1	1.3-3.4 μH	Q > 100 @ 2 μH	1.2-3.8 μH	Q > 100 @ 2 μH
C1	48-100 pF		40-80 pF	
C2	8-60 pF		12-45 pF	

L1 and T1 = #26 AWG Tinned Nylon Acetate Wire.

L1 @ 35 or 45 MHz = 7-1/4 Turns on a 1/4" coil form
@ 58 MHz = 6 Turns on a 1/4" coil form
T1 Primary Winding = 18 Turns on a 1/4" coil form
Secondary Winding = 2 Turns Wound Evenly over Primary Winding for 35 or 45 MHz and 1 Turn for 58 MHz
Slug = Arnold TH Material 1/2" long

GENERAL OPERATING INFORMATION

The MC1352 consists of an AGC section and an IF signal amplifier (Figure 2) subdivided into different functions as indicated by the illustration.

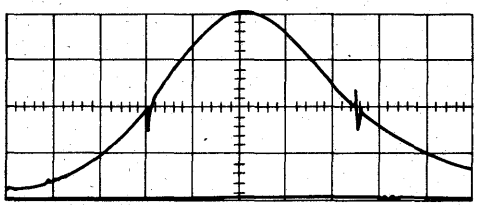
A gating pulse, a reference level, and a composite video signal are required for proper operation of the AGC section. Either positive or negative-going video may be used; necessary connections and signal levels are shown in Figure 1. The essential difference is that the video is fed into Pin 10 and the AGC reference level is applied to Pin 6 for a video signal with positive-going sync while the input connections are reversed for negative-going sync.

The action of the gating section is such that the proper voltage, V_C, is maintained across the external capacitor, C2, for a particular video level and dc reference setting. The voltage V_C, is the result of the charge delivered through D1 and the charge drained by Q1. The charge delivered occurs during the time of the gating pulse, and its magnitude is determined by the amplitude of the video signal relative to the dc reference level. The voltage V_C is delivered via the IF-AGC amplifier and applied to the variable gain stage of the IF signal amplifier and is also applied to the RF-AGC amplifier, where it is compared to the fixed RF-AGC delay voltage reference by the differential amplifier, Q2 and Q3. The following stages amplify the output signal of Q2 and shift the dc levels causing the RF-AGC voltage to vary.

The input amplifiers (Q4 and Q5) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for ac). Terminals 1 and 2 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q6 and Q7 causing those transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q8 and Q9. The output amplifiers are fed from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant.

FIGURE 4 – TEST CIRCUIT RESPONSE CURVE (45 and 58 MHz)



Scale: 1 MHz/cm

NOTES:

1. The 12-V supply must have a low ac impedance to prevent low-frequency instability in the RF-AGC loop. This can be achieved by a 12-V zener diode and a large decoupling capacitor. (5 μF).
2. Choices of C1, C2 and C3 depend somewhat on the set designers' preference concerning AGC stability versus AGC recovery speed. Typical values are C1 = 0.1 μF, C2 = 0.25 μF, C3 = 10 μF.
3. To set a fixed IF-AGC operating point (e.g., for receiver alignment) connect a 22 kΩ resistor from pin 9 to pin 11 to give minimum gain, then bias pin 14 to give the correct operating point using a 200 kΩ variable resistor to ground.
4. Although the unit will normally be operating with a very high power gain, the pin configuration has been carefully chosen so that shielding between input and output terminals will not normally be necessary even when a standard socket is used.

FIGURE 5 – TYPICAL AGC APPLICATION CHART

Video Polarity	Pin 6 Voltage	Pin 10 Voltage	Pin 5 R1 (Ω)
Negative-Going Sync.	5.5 / 2.0 / 0	Adj. 1.0–4.0 Vdc Nom 2.0 V	0
Positive-Going Sync.	Adj. 1.0–8.0 Vdc Nom 4.5 V	4.5 / 0	3.9 k

TYPICAL CHARACTERISTICS

(V_{CC} = +12 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 6 – SINGLE-ENDED INPUT ADMITTANCE

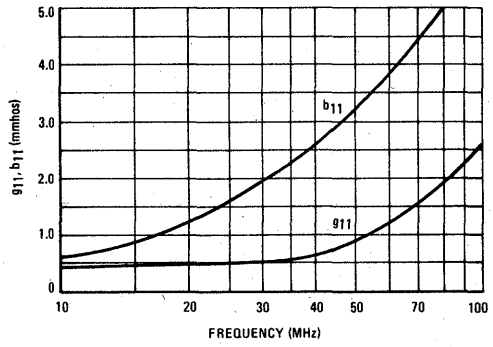


FIGURE 7 – DIFFERENTIAL OUTPUT ADMITTANCE

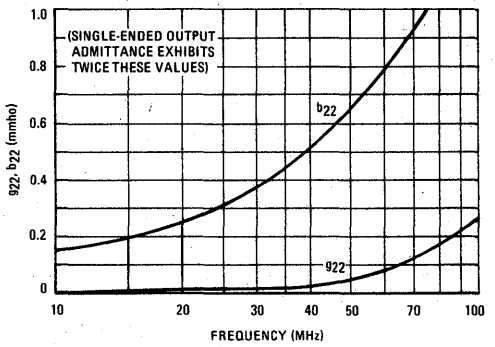


FIGURE 8 – FORWARD TRANSFER ADMITTANCE

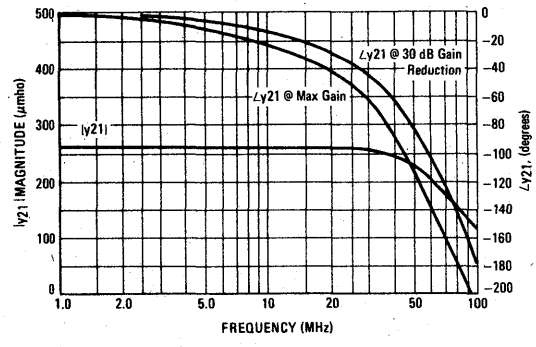


FIGURE 9 – DIFFERENTIAL OUTPUT VOLTAGE

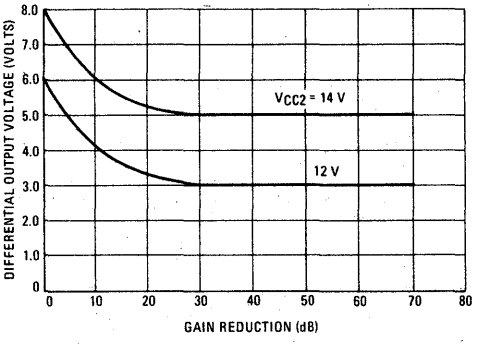


FIGURE 10 – AGC CHARACTERISTICS

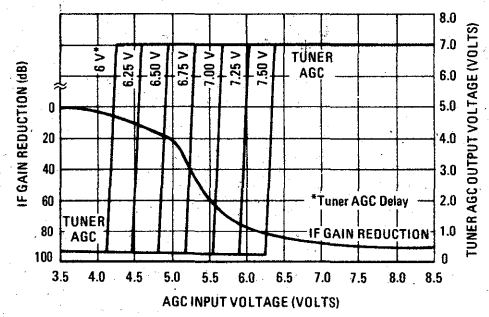
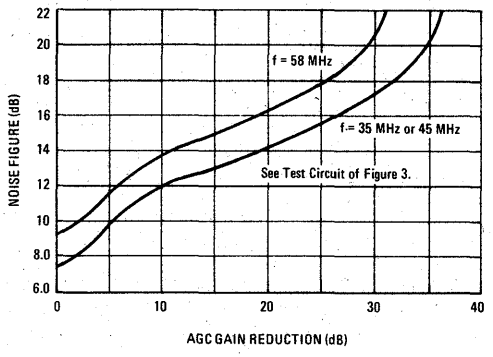


FIGURE 11 – TYPICAL NOISE FIGURE



ORDERING INFORMATION

Device	Temperature Range	Package
MC1355P	0°C to +75°C	Plastic DIP
MC1355PQ	0°C to +75°C	Plastic

MC1355

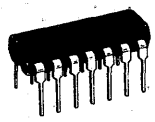
BALANCED FOUR-STAGE HIGH-GAIN FM/IF AMPLIFIER

. . . designed for use with Foster-Seeley discriminator or ratio detector in high quality FM systems.

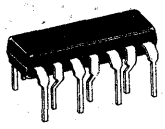
- High AM Rejection (60 dB typ)
- Wide Range of Supply Voltages (8 to 18 Vdc)
- Low Distortion (0.5% typ)

LIMITING FM IF AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

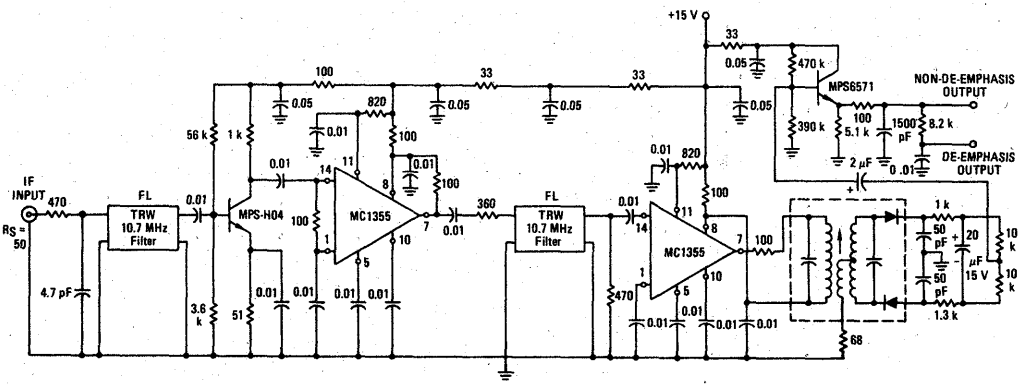


P SUFFIX
PLASTIC PACKAGE
CASE 646



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – DUAL MC1355 FM IF APPLICATION



*All other pins grounded
T-Ratio Detector (input impedance ≅ 1.5 k) G.I. #36231 or equivalent

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

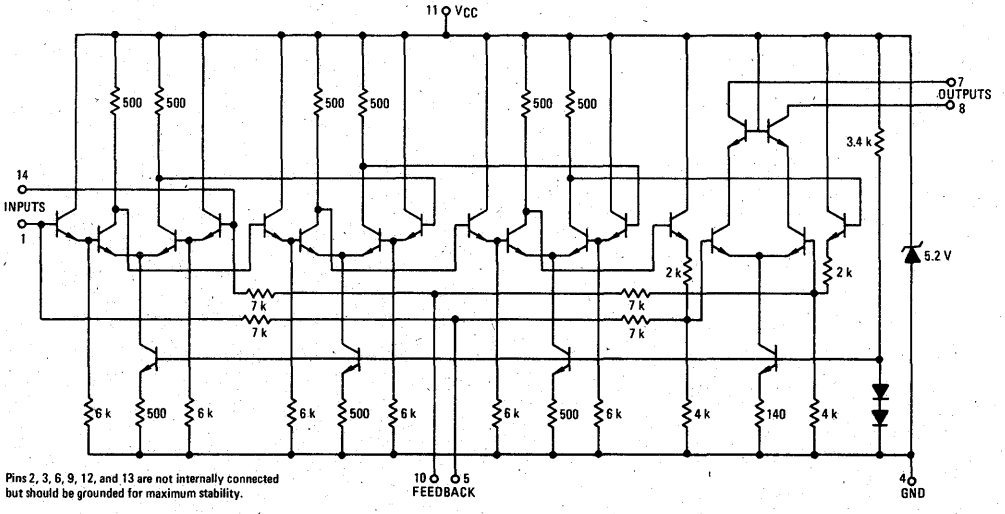
Rating	Value	Unit
Output Voltage (pins 7 & 8)	40	Vdc
Supply Current to pin 11	20	mA
Input Signal Voltage (single-ended)	5.0	Vp-p
Input Signal Voltage (differential)	10	Vp-p
Power Dissipation (package limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 Vdc, f = 10.7 MHz, T_A = +25°C)

Characteristic		Min	Typ	Max	Units
Power Supply Voltage Range		8.0	15	18	Vdc
Total Circuit Current		–	16	–	mAdc
Total Output Stage Current		–	4.2	–	mA
Device Dissipation		–	125	–	mW
Internal Zener Voltage		–	5.2	–	Vdc
Input Signal for 3 dB Limiting		–	175	250	μV(rms)
Output Current Swing		3.5	4.2	5.0	mA p-p
AM Rejection (10 mv to 1.0 v (rms) input, FM @ 100%, AM @ 80%, Foster Seeley detector)		–	60	–	dB
Admittance Parameters	Y_{11}	–	120 + j320	–	μmhos
	Y_{12}	–	j0.6	–	μmho
	Y_{21}	–	8 + j5.9	–	mhos
	Y_{22}	–	15 + j230	–	μmhos

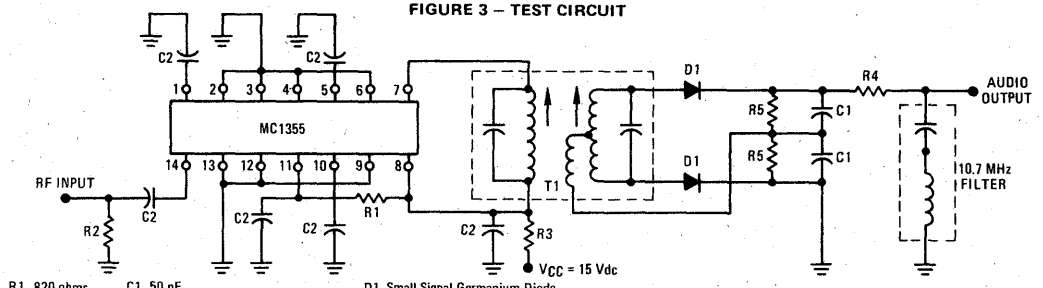
7

FIGURE 2 – CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

FIGURE 3 – TEST CIRCUIT



R1 820 ohms
R2 50 ohms
R3 100 ohms
R4 5 kilohms
R5 12 kilohms

C1 50 pF
C2 0.01 μF
T1 10.7 MHz Foster-Seeley Discriminator, Primary Impedance = 3.9 k, Peak-to-Peak Separation = 600 kHz

D1 Small Signal Germanium Diode (1N542 or equiv)

Specifications are given for a Foster-Seeley discriminator. Improved AM rejection at low signal levels can be obtained with a ratio detector.

For optimum circuit stability it is important to ground pins 2, 3, 4, 6, 9, 12, and 13.

FIGURE 4 – AM REJECTION TEST BLOCK DIAGRAM

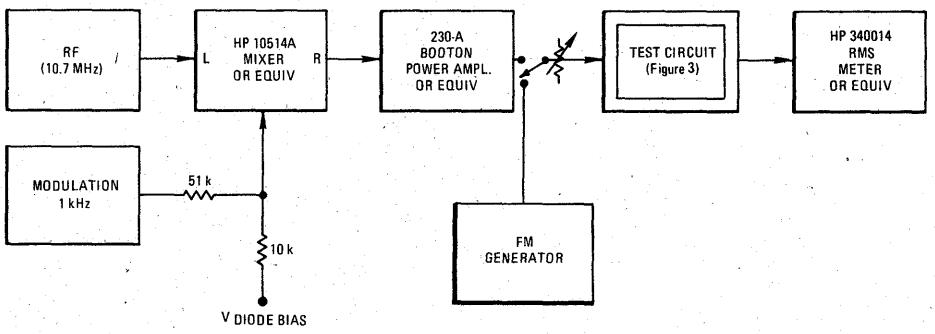


FIGURE 5 – LIMITING

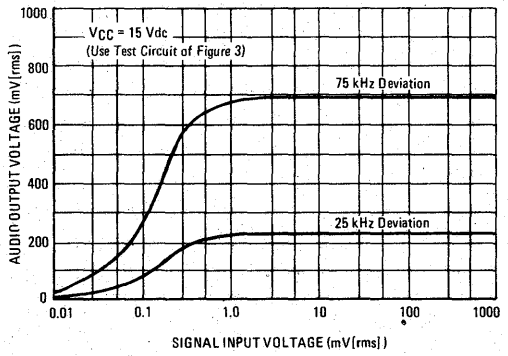
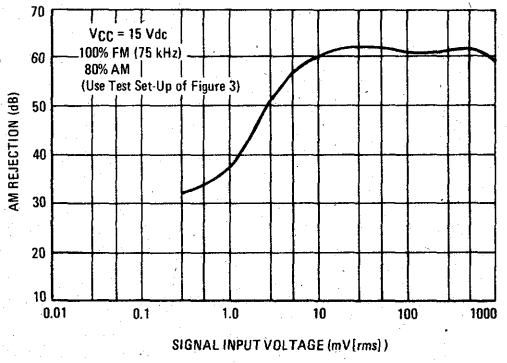


FIGURE 6 – AM REJECTION



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TYPICAL CHARACTERISTICS (continued)

FIGURE 7 – OUTPUT DISTORTION

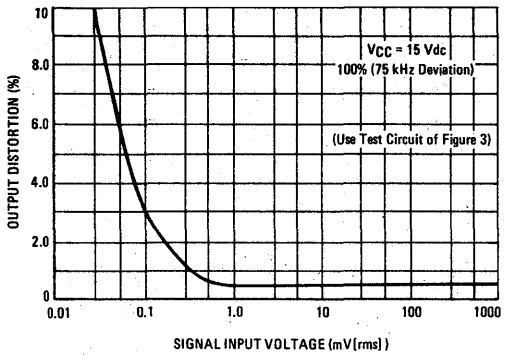


FIGURE 8 – SIGNAL-TO-NOISE RATIO SIGNAL

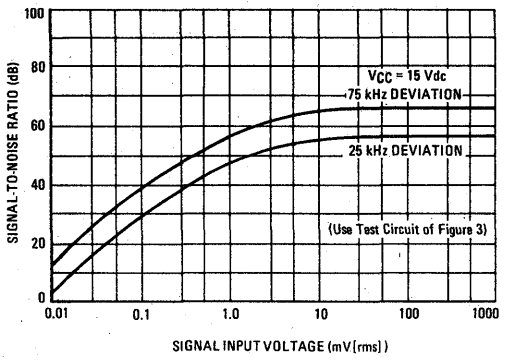
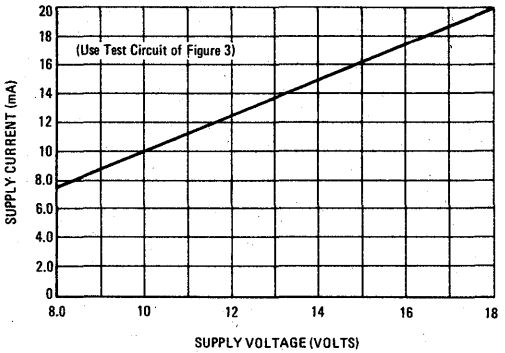


FIGURE 9 – TOTAL SUPPLY CURRENT



7

ORDERING INFORMATION

Device	Temperature Range	Package
MC1356P	−25°C to +85°C	Plastic DIP

MC1356P

FM DETECTOR AND LIMITER

SILICON MONOLITHIC INTEGRATED CIRCUITS

FM DETECTOR AND LIMITER

. . . includes a limiting amplifier, a quadrature discriminator, and a voltage regulator; and is designed primarily for FM receiver applications. It is similar to the MC1357 and includes built-in regulation capable of supplying 20 mA to external circuitry.

Features:

- Good Line and Load Regulation
- Low Harmonic Distortion
- Single Tuning Coil Design
- Direct Replacement for ULN2136

P SUFFIX
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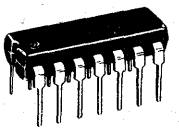
CASE 646



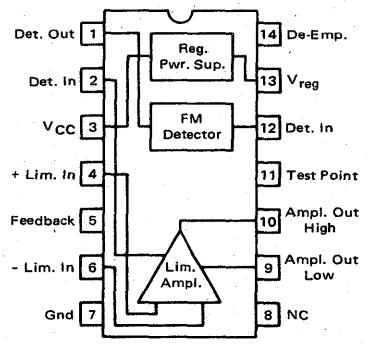
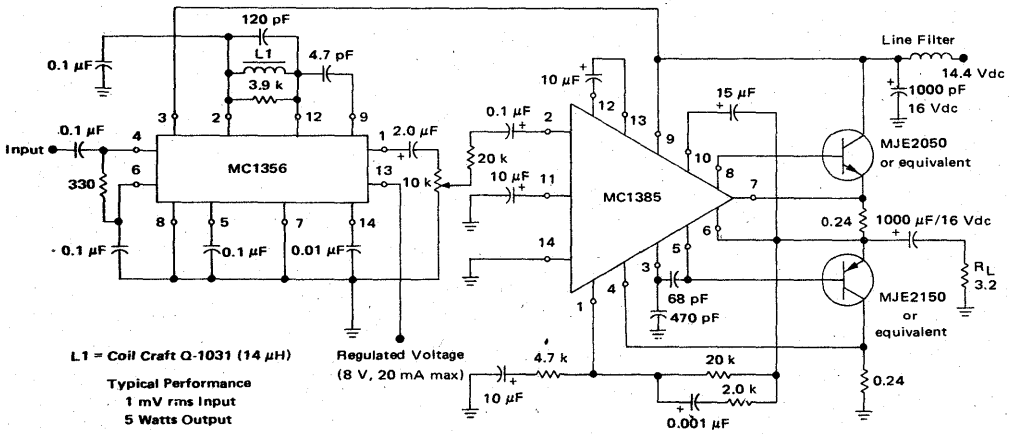


FIGURE 1 – TYPICAL AUTOMOTIVE APPLICATIONS CIRCUIT



7

MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage	+16	Vdc
Power Dissipation @ T_A = +25°C (Package Limitation) Derate above 25°C	1.0 7.7	W mW/°C
Operating Temperature Range	-25 to +85	°C
Storage Temperature Range	-65 to +150	°C
Regulator Load (Pin 13)	20	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = 25°C unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Recommended Operating Voltage	3	10	–	16	Vdc
Drain Current	3	14	16	19	mA
Amplifier Input Reference Voltage	6	1.3	1.4	1.5	Vdc
Detector Input Reference Voltage	2	3.3	3.5	3.7	Vdc
Detector Output Voltage	1	3.0	3.8	4.6	Vdc
Amplifier Input Resistance	4	–	15	–	kΩ
Amplifier Input Capacitance	4	–	7.0	–	pF
Amplfier Output Resistance	10	–	90	–	Ohms
De-Emphasis Resistance	14	7.0	8.8	10.5	kΩ
Temperature Sensitivity of Power Supply	13	–	+0.2	–	mV/°C
Temperature Sensitivity of Output Voltage	1	–	+0.3	–	mV/°C
Regulation Voltage	13	7.9	8.1	8.3	Vdc

DYNAMIC CHARACTERISTICS (FM Modulation Frequency = 1.0 kHz, T_A = 25°C)
(V_{CC} = 12 Vdc, f_o = 10.7 MHz, f = ±75 kHz)

Characteristic	Pin	Min	Typ	Max	Unit
AM Rejection (V_{IN} = 10 mVrms)	1	36	42	–	dB
Input Limiting Threshold Voltage (-3 dB, V_{IN} @ 10 mVrms)	4	–	400	500	μV(RMS)
Recovered Audio Output Voltage (V_{IN} = 10 mV(rms)	1	350	450	550	mV(RMS)
Output Distortion (V_{IN} = 10 mVrms)	1	–	1.0	2.0	%
Signal to Noise (V_{IN} = 10 mV rms)	1	–	70	–	dB

7

FIGURE 2 – MC1356P TEST CIRCUIT

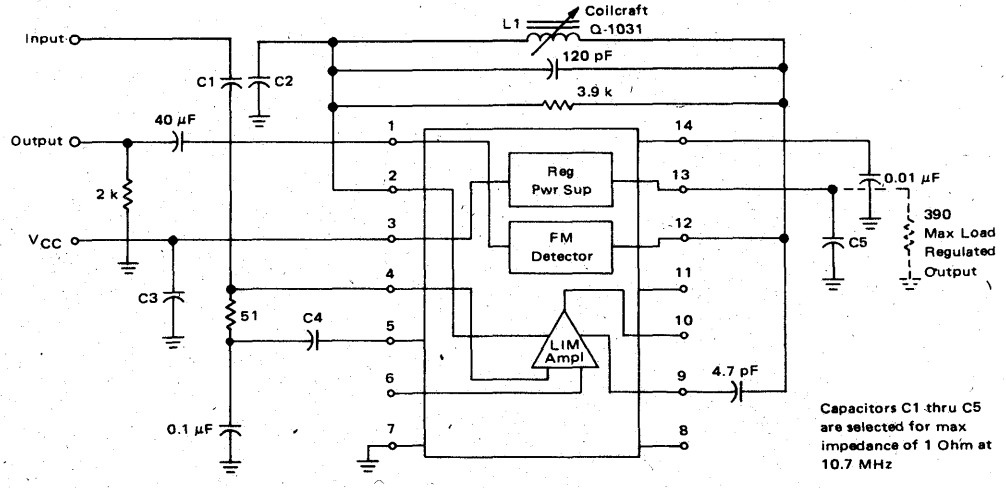


FIGURE 3 – AM REJECTION

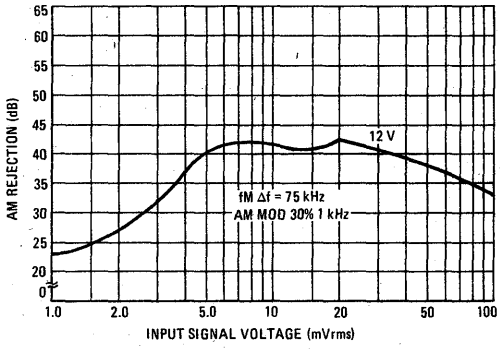


FIGURE 4 – SIGNAL-TO-NOISE RATIO

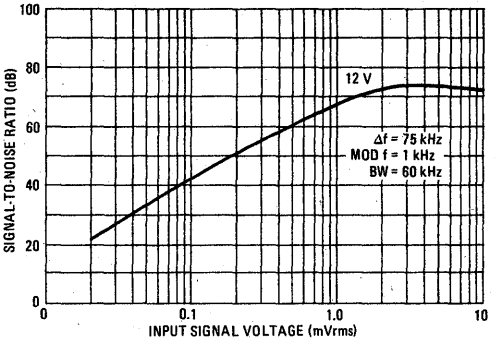


FIGURE 5 – RECOVERED AUDIO OUTPUT versus SIGNAL INPUT VOLTAGE

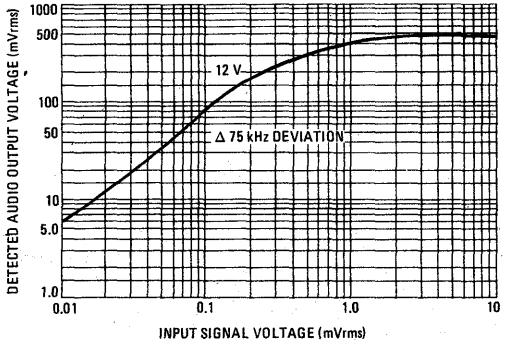


FIGURE 6 – REGULATED VOLTAGE versus SUPPLY VOLTAGE

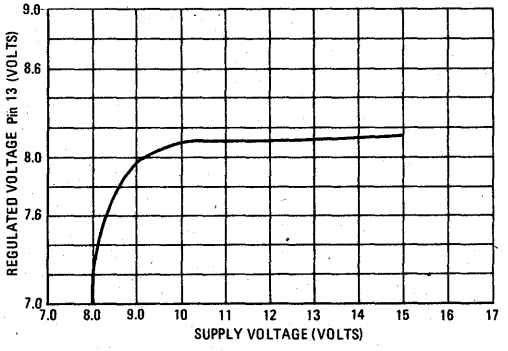


FIGURE 7 – DETECTOR TRANSFER CHARACTERISTIC

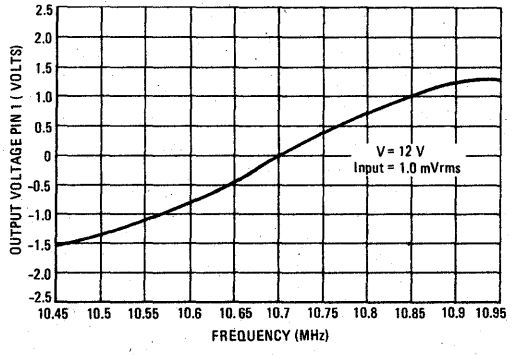


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FIGURE 8 – TYPICAL FM RADIO RECEIVER BLOCK DIAGRAM USING MC1356P

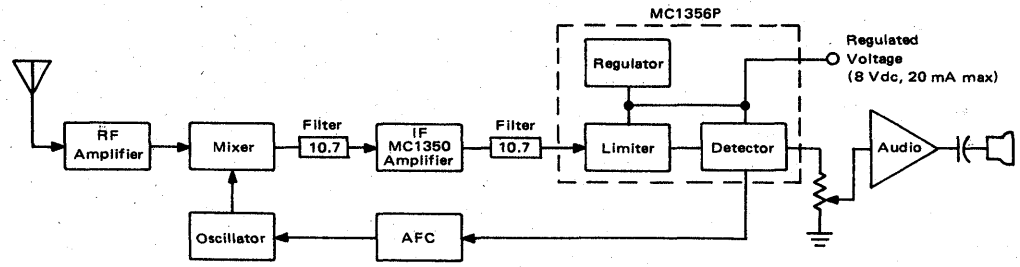
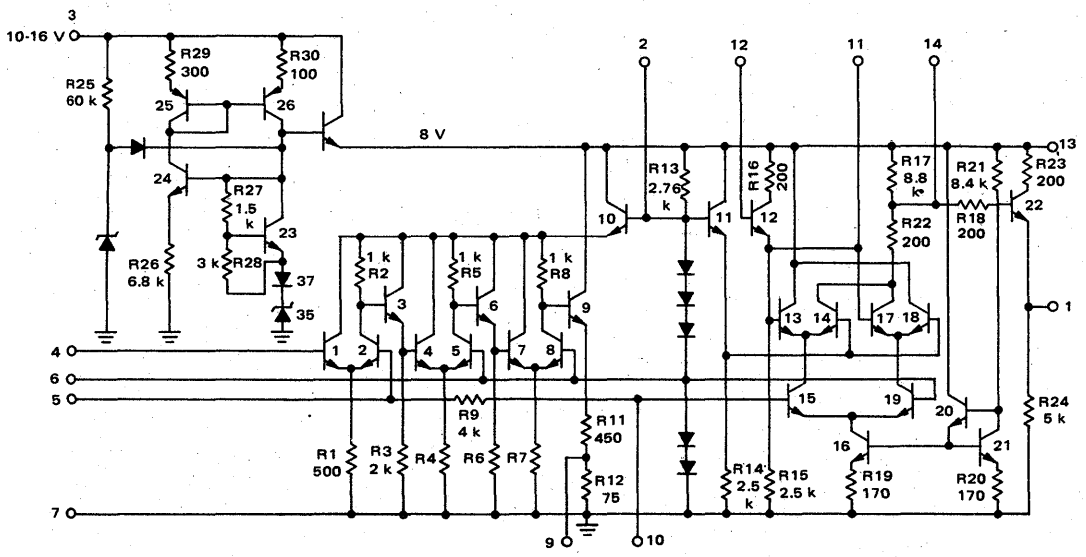


FIGURE 9 – MC1356P TEST CIRCUIT SCHEMATIC



ORDERING INFORMATION

Device	Temperature Range	Package
MC1357P	0°C to +75°C	Plastic DIP
MC1357PQ	0°C to +75°C	Plastic

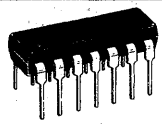
MC1357

TV SOUND IF OR FM IF AMPLIFIER WITH QUADRATURE DETECTOR

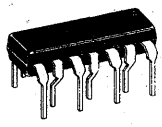
- A Direct Replacement for the ULN2111A
- Greatly Simplified FM Demodulator Alignment
- Excellent Performance at V_{CC} = 8.0 Vdc

IF AMPLIFIER AND QUADRATURE DETECTOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

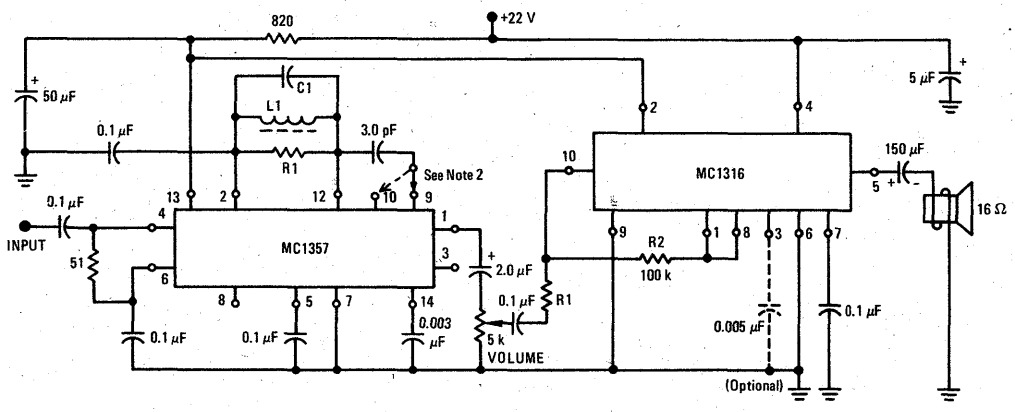


P SUFFIX
PLASTIC PACKAGE
CASE 646



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 – TV TYPICAL APPLICATION CIRCUIT



Typical Performance:
2 Watts Output
2% Distortion
250 μV Sensitivity (3 dB Lim.)

C1 = 120 pF
L1 = 14 μH
R1 = 20 kΩ
Q = 30

7

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	16	Vdc
Input Voltage (Pin 4)	3.5	V_p
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic		Pin	Min	Typ	Max	Units
Drain Current	V_{CC} = 8 V V_{CC} = 12 V	13	10 –	12 15	19 21	mA
Amplifier Input Reference Voltage		6	–	1.45	–	Vdc
Detector Input Reference Voltage		2	–	3.65	–	Vdc
Amplifier High Level Output Voltage		10	1.25	1.45	1.65	Vdc
Amplifier Low Level Output Voltage		9	–	0.145	0.2	Vdc
Detector Output Voltage	V_{CC} = 8 V V_{CC} = 12 V	1	– –	3.7 5.4	– –	Vdc
Amplifier Input Resistance		4	–	5.0	–	kΩ
Amplifier Input Capacitance		4	–	11	–	pF
Detector Input Resistance		12	–	70	–	kΩ
Detector Input Capacitance		12	–	2.7	–	pF
Amplifier Output Resistance		10	–	60	–	ohms
Detector Output Resistance		1	–	200	–	ohms
De-Emphasis Resistance		14	–	8.8	–	kΩ

DYNAMIC CHARACTERISTICS (FM Modulation Freq. = 1.0 kHz, Source Resistance = 50 ohms, T_A = +25°C for all tests.)

(V_{CC} = 12 Vdc, f_o = 4.5 MHz, Δf = ±25 kHz, Peak Separation = 150 kHz)

Characteristics	Pin	Min	Typ	Max	Units
Amplifier Voltage Gain ($V_{in} \leq 50\ \mu V$[rms])	10	–	60	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	36	–	dB
Input Limiting Threshold Voltage	4	–	250	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	0.72	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	3	–	%

(V_{CC} = 12 Vdc, f_o = 5.5 MHz, Δf = ±50 kHz, Peak Separation = 260 kHz)

Amplifier Voltage Gain ($V_{in} \leq 50\ \mu V$[rms])	10	–	60	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	40	–	dB
Input Limiting Threshold Voltage	4	–	250	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	1.2	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	5	–	%

(V_{CC} = 8.0 Vdc, f_o = 10.7 MHz, Δf = ±75 kHz, Peak Separation = 550 kHz)

Amplifier Voltage Gain ($V_{in} \leq 50\ \mu V$[rms])	10	–	53	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	37	–	dB
Input Limiting Threshold Voltage	4	–	600	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	0.30	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	1.4	–	%

(V_{CC} = 12 Vdc, f_o = 10.7 MHz, Δf = ±75 kHz, Peak Separation = 550 kHz)

Amplifier Voltage Gain ($V_{in} \leq 50\ \mu V$[rms])	10	–	53	–	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	–	45	–	dB
Input Limiting Threshold Voltage	4	–	600	–	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	–	0.48	–	V(rms)
Output Distortion (V_{in} = 10 mV[rms])	1	–	1.4	–	%

*100% FM, 30% AM Modulation

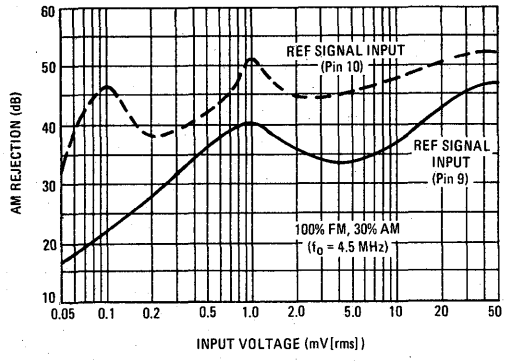
TYPICAL CHARACTERISTICS

(V_{CC} = 12 V, T_A = +25°C unless otherwise noted)

(Use Test Circuit of Figure 13)

(f_o = 4.5 MHz)

FIGURE 2 – AM REJECTION



(f_o = 5.5 MHz)

FIGURE 3 – AM REJECTION

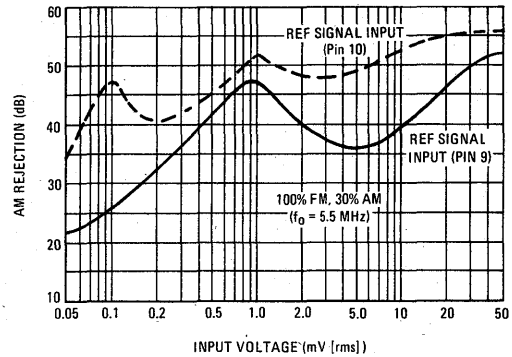


FIGURE 4 – DETECTED AUDIO OUTPUT

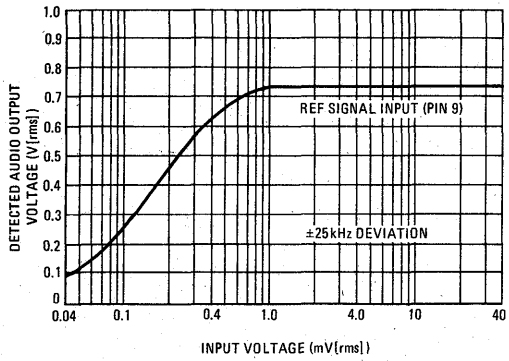


FIGURE 5 – DETECTED AUDIO OUTPUT

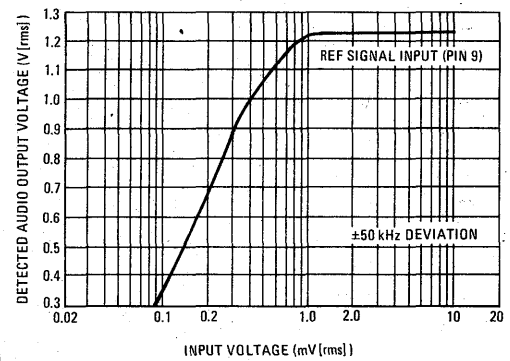


FIGURE 6 – DETECTOR TRANSFER CHARACTERISTIC

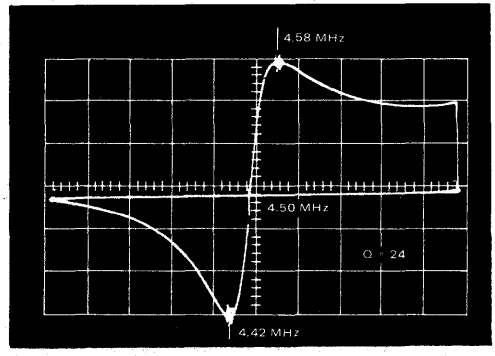
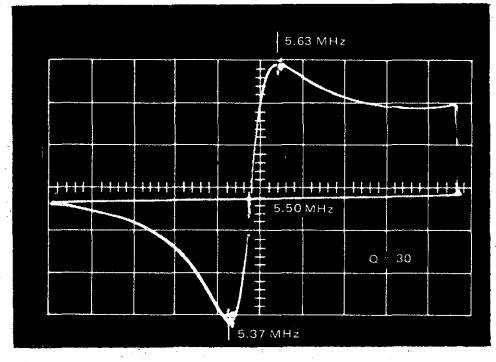


FIGURE 7 – DETECTOR TRANSFER CHARACTERISTIC



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TYPICAL CHARACTERISTICS (continued)

(f_o = 10.7 MHz, T_A = +25°C unless otherwise noted.)

(Use Test Circuit of Figure 13)

FIGURE 8 – AM REJECTION

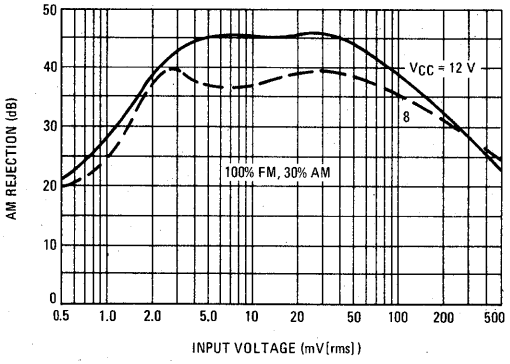


FIGURE 9 – AFC VOLTAGE DRIFT (1.0 mV INPUT CARRIER @ 10.7 MHz)

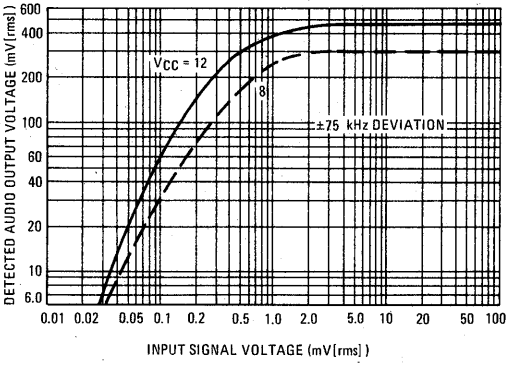


FIGURE 10 – LIMITING

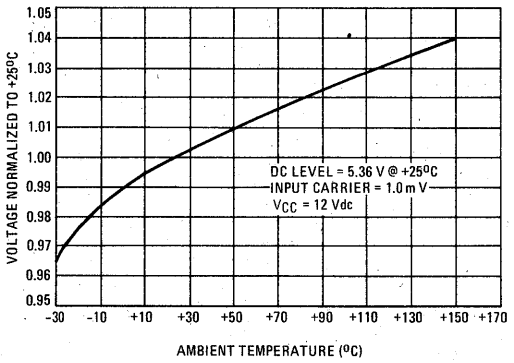


FIGURE 11 – SIGNAL-TO-NOISE RATIO

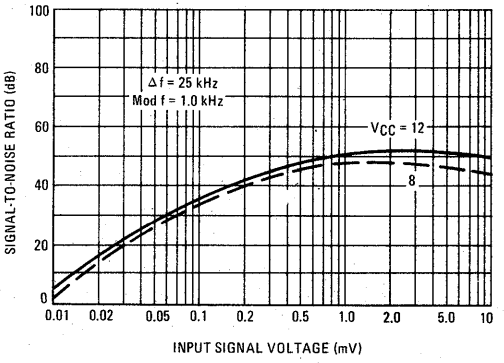


FIGURE 12 – DETECTOR TRANSFER CHARACTERISTIC

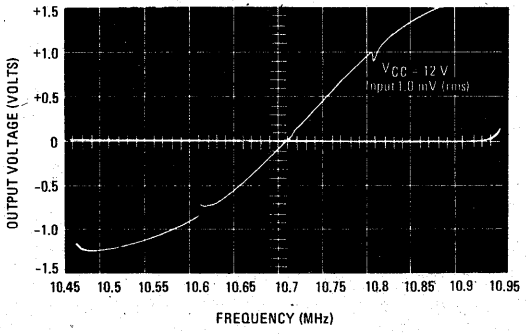
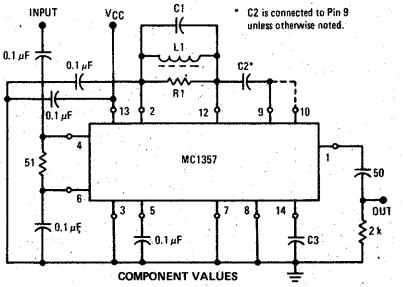


FIGURE 13 – TEST CIRCUIT



COMPONENT VALUES

f	L1	C1	R1	Q(R1, L1)	C2	C3
MHz	μH	pF	kΩ		pF	μF
4.5	14	120	20	30	3.0	0.003
5.5	8.0	100	20	30	3.0	0.003
10.7	2.0	120	3.9	30	4.7	0.01

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FIGURE 14 – FM RADIO TYPICAL APPLICATION CIRCUIT

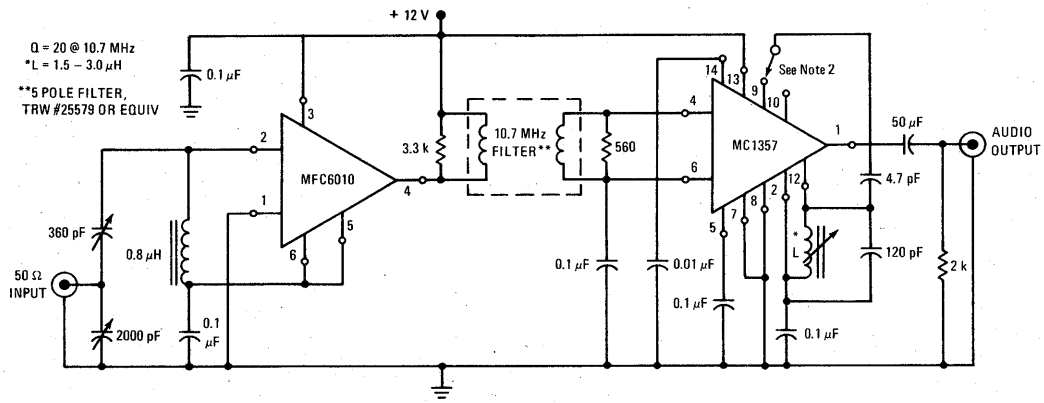
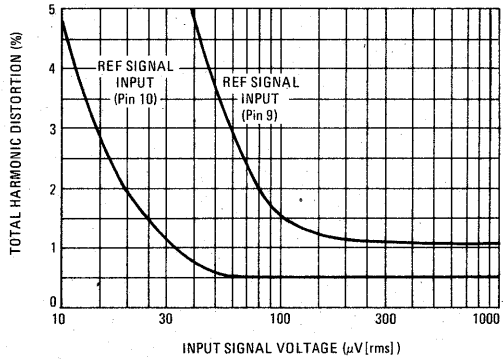


FIGURE 15 – OUTPUT DISTORTION



Note 1:
Information shown in Figures 15, 16, and 17 was obtained using the circuit of Figure 14.

Note 2:
Optional input to the quadrature coil may be from either pin 9 or pin 10 in the applications shown. Pin 9 has commonly been used on this type of part to avoid overload with various tuning techniques. For this reason, pin 9 is used in tests on the preceding pages (except as noted). However, a significant improvement of limiting sensitivity can be obtained using pin 10, see Figure 17, and no overload problems have been incurred with this tuned circuit configuration.

FIGURE 16 – SIGNAL-TO-NOISE RATIO

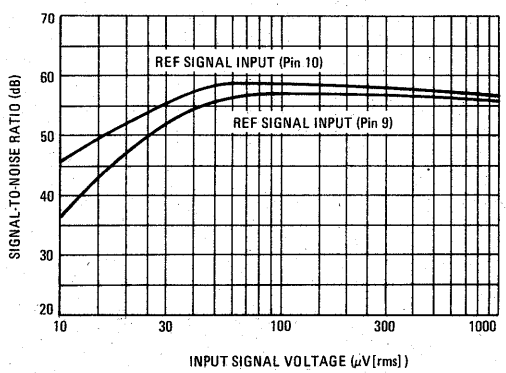


FIGURE 17 – RECOVERED AUDIO OUTPUT

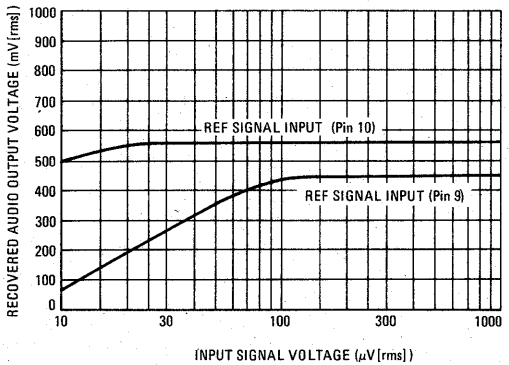


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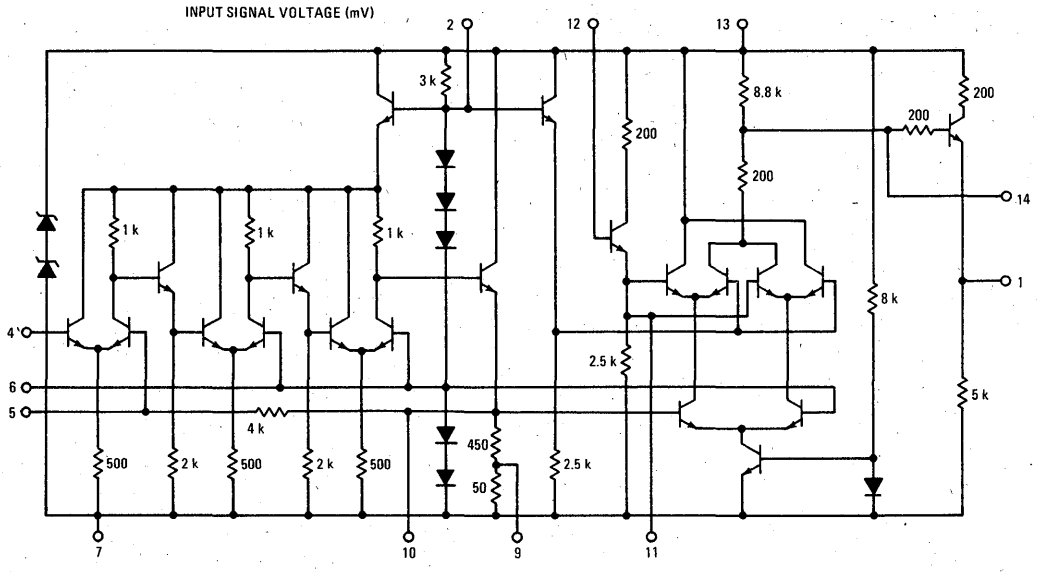
FIGURE 18 – CIRCUIT SCHEMATIC



7

ORDERING INFORMATION

Device	Temperature Range	Package
MC1358P	−20°C to +75°C	Plastic DIP
MC1358PQ	−20°C to +75°C	Plastic

MC1358

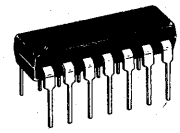
TV SOUND IF AMPLIFIER

. . . a versatile monolithic device incorporating IF limiting, detection, electronic attenuation, audio amplifier, and audio driver capabilities.

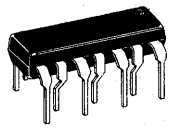
- Direct Replacement for the CA3065
- Differential Peak Detector Requiring a Single Tuned Circuit
- Electronic Attenuator Replaces Conventional ac Volume Control — Range > 60 dB
- Excellent AM Rejection @ 4.5 and 5.5 MHz
- High Stability
- Low Harmonic Distortion
- Audio Drive Capability — 6.0 mAp-p
- Minimum Undesirable Output Signal @ Maximum Attenuation

IF AMPLIFIER, LIMITER, FM DETECTOR, AUDIO DRIVER, ELECTRONIC ATTENUATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

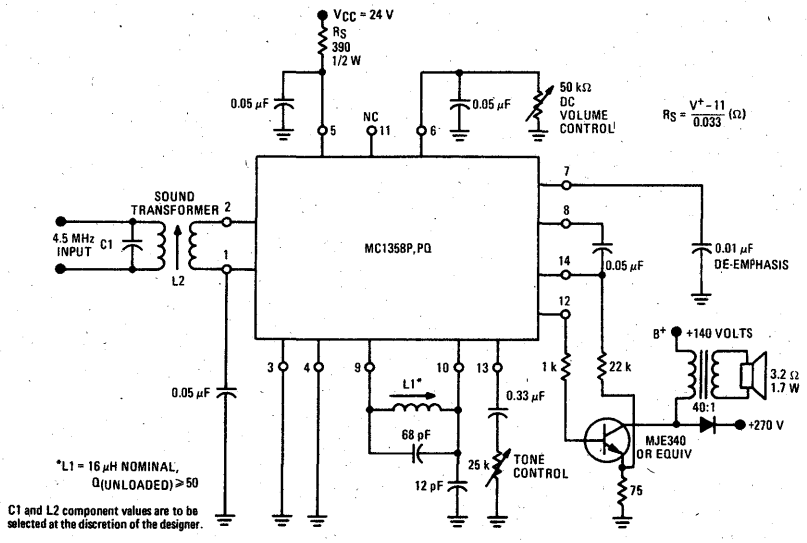


P SUFFIX
PLASTIC PACKAGE
CASE 646



PQ SUFFIX
PLASTIC PACKAGE
CASE 647

FIGURE 1 — TYPICAL TV APPLICATION CIRCUIT



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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Input Signal Voltage (Pins 1 and 2)	±3.0	Vdc
Power Supply Current	50	mA
Power Dissipation (Package Limitation) Plastic Packages Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C unless otherwise noted).

Characteristic	Pin	Min	Typ	Max	Unit
Regulated Voltage	5	10.3	11	12.2	Vdc
DC Supply Current (V^+ = 9 Vdc, R_S = 0)	5	10	16	24	mA
Quiescent Output Voltage	12	–	5.1	–	Vdc

DYNAMIC CHARACTERISTICS (V_{CC} = 24 Vdc, T_A = +25°C unless otherwise noted).

Characteristic	Min	Typ	Max	Unit
IF AMPLIFIER AND DETECTOR				
f_o = 4.5 MHz, Δf = ±25 kHz				
AM Rejection* (V_{in} = 10 mV [rms])	40	51	–	dB
Input Limiting Threshold Voltage	–	200	400	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	0.5	0.70	–	V(rms)
Output Distortion (V_{in} = 10 mV [rms])	–	0.4	2.0	%
f_o = 5.5 MHz, Δf = ±50 kHz				
AM Rejection* (V_{in} = 10 mV [rms])	40	53	–	dB
Input Limiting Threshold Voltage	–	200	400	μV(rms)
Recovered Audio Output Voltage (V_{in} = 10 mV [rms])	0.5	0.91	–	V(rms)
Output Distortion (V_{in} = 10 mV [rms])	–	0.9	–	%
Input Impedance Components (f = 4.5 MHz, measurement between pins 1 and 2) Parallel Input Resistance Parallel Input Capacitance	 – –	 17 4.0	 – –	 kΩ pF
Output Impedance Components (f = 4.5 MHz, measurement between pin 9 and GND) Parallel Output Resistance Parallel Output Capacitance	 – –	 3.25 3.6	 – –	 kΩ pF
Output Resistance, Detector Pin 7 Pin 8	 – –	 7.5 250	 – –	 kΩ Ω
ATTENUATOR				
Volume Reduction Range (See Figure 8) (dc Volume Control = ∞)	60	–	–	dB
Maximum Undesirable Signal (See Note 1) (dc Volume Control = ∞)	–	0.07	1.0	mV
AUDIO AMPLIFIER				
Voltage Gain (V_{in} = 0.1 V(rms), f = 400 Hz)	17.5	20	–	dB
Total Harmonic Distortion (V_o = 2.0 V(rms), f = 400 Hz)	–	2.0	–	%
Output Voltage (THD = 5%, f = 400 Hz)	2.0	3.0	–	V(rms)
Input Resistance (f = 400 Hz)	–	70	–	kΩ
Output Resistance (f = 400 Hz)	–	270	–	Ω

*100% FM, 30% AM Modulation.

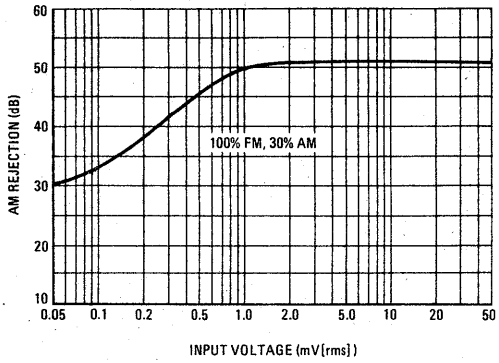
Note 1. Undesirable signal is measured at pin 8 when volume control is set for minimum output.

TYPICAL CHARACTERISTICS

(V_{CC} = 24 Vdc, T_A = +25°C unless otherwise noted)

(f_o = 4.5 MHz)

FIGURE 2 – AM REJECTION



(f_o = 5.5 MHz)

FIGURE 3 – AM REJECTION

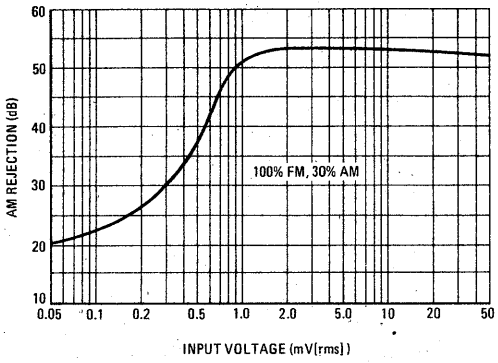


FIGURE 4 – DETECTED AUDIO OUTPUT

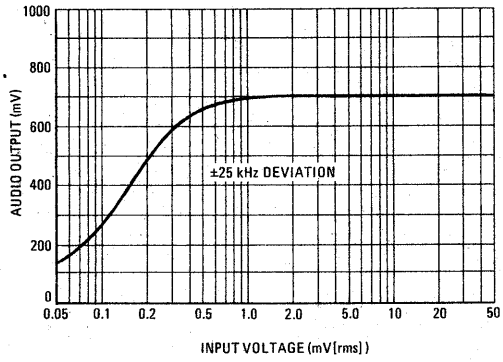


FIGURE 5 – DETECTED AUDIO OUTPUT

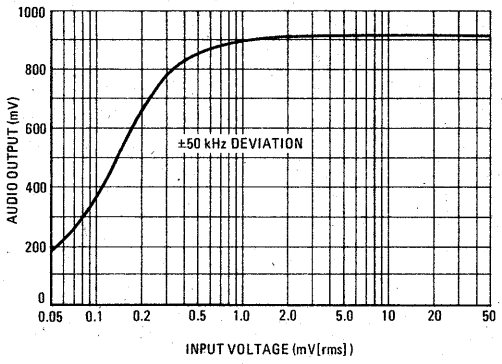


FIGURE 6 – IF AMPLIFIER AND DETECTOR THD

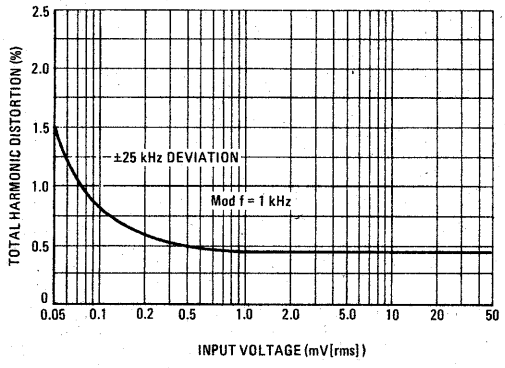
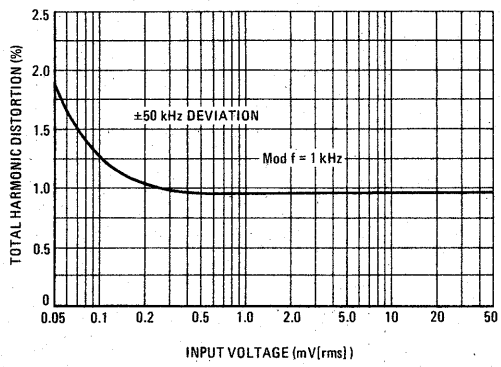


FIGURE 7 – IF AMPLIFIER AND DETECTOR THD



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TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – GAIN REDUCTION OF ATTENUATOR

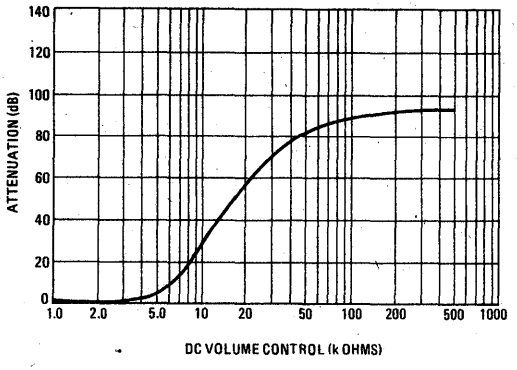


FIGURE 9 – AUDIO AMPLIFIER THD

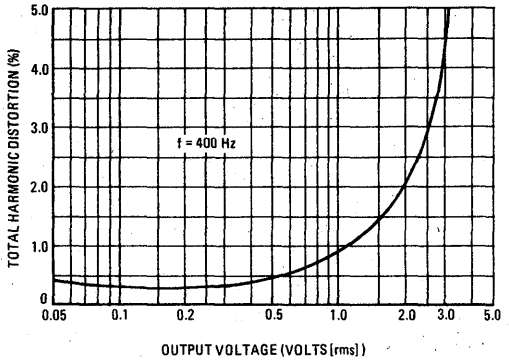


FIGURE 10 – IF FREQUENCY RESPONSE

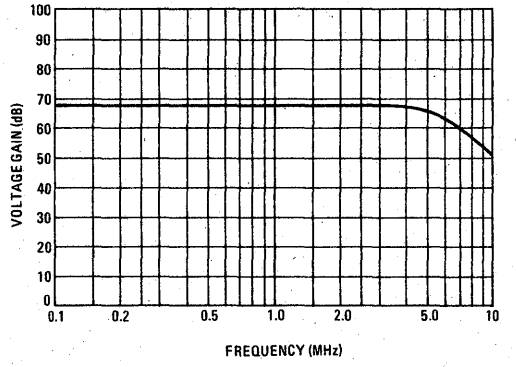


FIGURE 11 – IF FREQUENCY RESPONSE TEST CIRCUIT

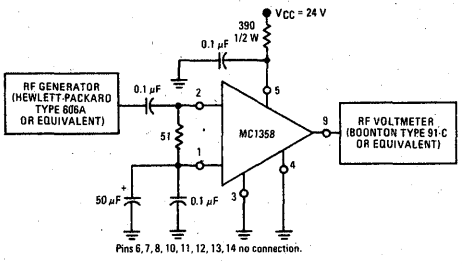


FIGURE 12 – AM REJECTION, DETECTED AUDIO, THD, ATTENUATION TEST CIRCUIT

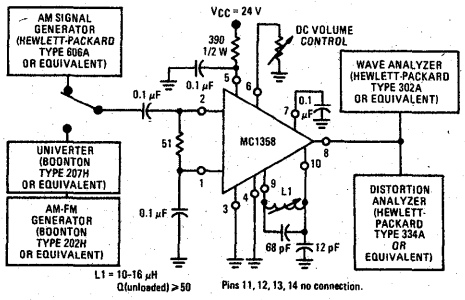


FIGURE 13 – AUDIO VOLTAGE GAIN, AUDIO THD TEST CIRCUIT

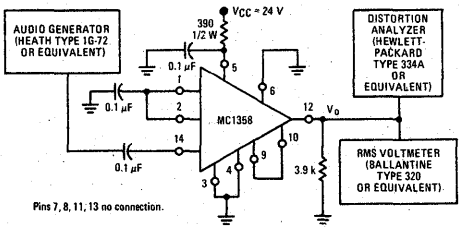
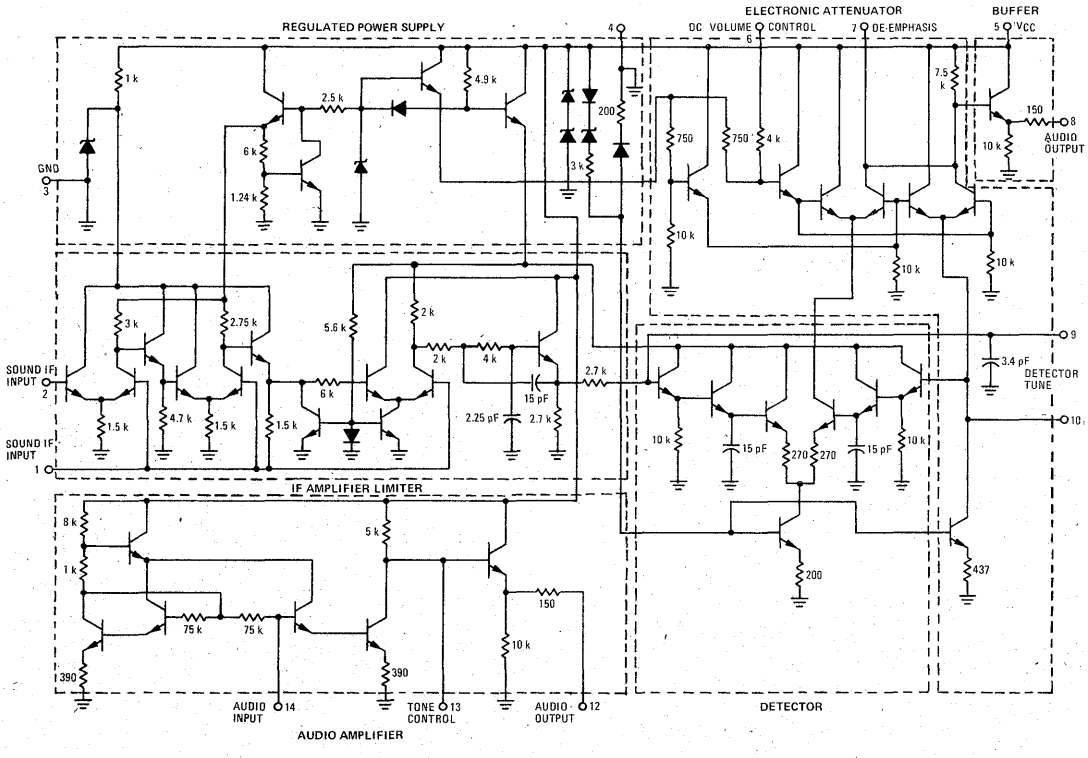


FIGURE 14 – CIRCUIT SCHEMATIC



7

ORDERING INFORMATION

Device	Temperature Range	Package
MC1364P	0°C to +75°C	Plastic DIP

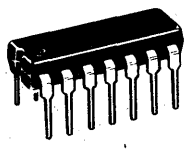
MC1364

TV AUTOMATIC FREQUENCY CONTROL

- High Gain Amplifier – 18 mV Input for Full Output
- Direct Replacement for the CA3064
- Also Available in the 14-Lead Dual In-Line Package

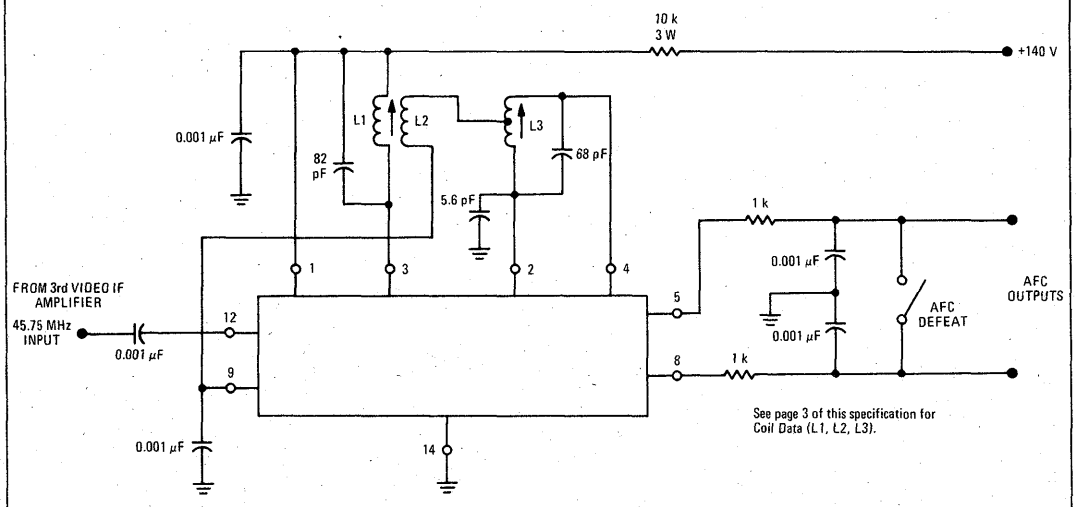
AUTOMATIC FREQUENCY CONTROL

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
CASE 646
PLASTIC PACKAGE

FIGURE 1 – TYPICAL APPLICATION CIRCUIT



See page 3 of this specification for Coil Data (L1, L2, L3).

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	MC1364P	Unit
Input Signal Voltage (Pin 12 to 14)	+2.0, -10	Vdc
Output Collector Voltage (Pins 3 and 14)	20	Volts
Power Dissipation (Package Limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range	0 to +75	°C
Storage Temperature Range	-65 to +125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +30 Vdc, T_A = +25°C, see Test Circuit of Figure 4 unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Total Device Dissipation	–	140	–	mW
Total Supply Current	–	12	–	mA
Current Drain, Total (Reduce V_{CC} so that V10 = 10.5 Vdc)	4.0	6.5	9.5	mA
Zener Regulating Voltage	10.9	11.8	12.8	V
Quiescent Current to Pin 3	1.0	2.0	4.0	mA
Quiescent Voltage at Pin 5 or Pin 8	5.0	6.6	8.0	V
Output Offset Voltage (Pin 5 to Pin 8)	-1.0	0	+1.0	V

DESIGN PARAMETERS, TYPICAL VALUES (V_{CC} = +30 Vdc, R_S = 1.5 k, f = 45.75 MHz)

Parameter	Symbol	Typ	Unit
Input Admittance	y_{11}	0.4 + j1	mmho
Reverse Transfer Admittance	y_{12}	0 + j3.4	μmho
Forward Transfer Admittance	y_{21}	110 + j140	mmhos
Output Admittance (Pin 3)	y_{22}	0.02 + j1	mmho

7

TYPICAL CHARACTERISTICS

(See Test Circuit of Figure 2)

FIGURE 2 – TYPICAL NARROW BAND DYNAMIC CHARACTERISTICS

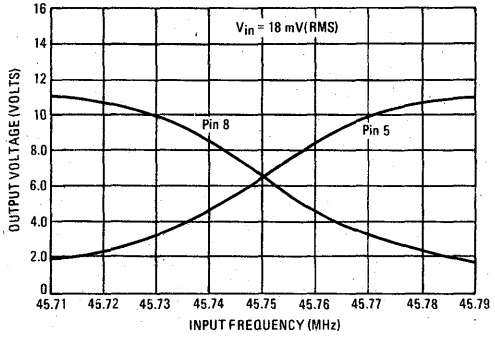


FIGURE 3 – TYPICAL WIDE BAND DYNAMIC CHARACTERISTICS

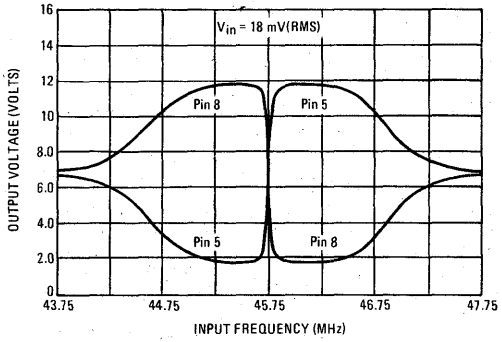
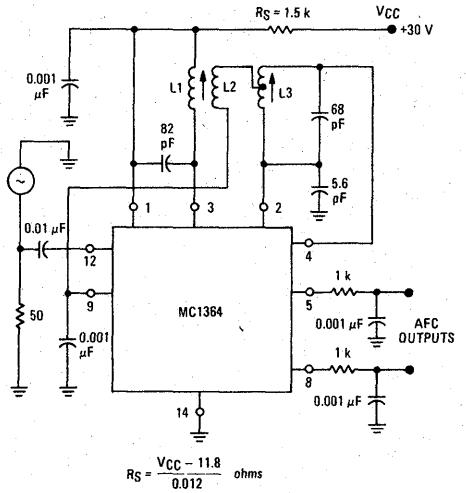


FIGURE 4 – TEST CIRCUIT



COIL DATA FOR DISCRIMINATOR WINDINGS FOR FIGURES 1 AND 4

L1 – Discriminator Primary: 3-1/6 turns; AWG #20 enamel-covered wire – close-wound, at bottom of coil form. Inductance of L1 = 0.165 μH; Q_O = 120 at f_O = 45.75 MHz.

Start winding at Terminal #6; finish at Terminal #1. See Notes below.

L2 – Tertiary Windings: 2-1/6 turns; AWG #20 enamel-covered wire – close-wound over bottom end of L1.

Start winding at Terminal #3; finish at Terminal #4. See Notes below.

L3 – Discriminator Secondary: 3-1/2 turns; AWG #20 enamel-covered wire, center-tapped, space wound at bottom of coil form.

Start winding at Terminal #2; finish at Terminal #5, connect center tap to Terminal #7. See Notes below.

Notes:
1. Coil Forms; Cylindrical; -0.30" Dia. Max.
2. Tuning Core: 0.250" Dia. x 0.37" Length.
   Material: Carbinal J or equivalent.
3. Coil Form Base: See drawing below.
4. End of coil nearest terminal board to be designated the winding start end.
5. Mount the coils 3/4" apart, center to center.

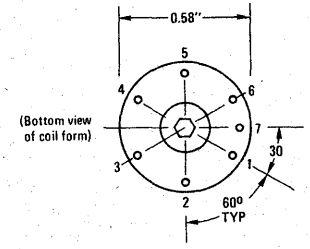


FIGURE 5 – CIRCUIT SCHEMATIC

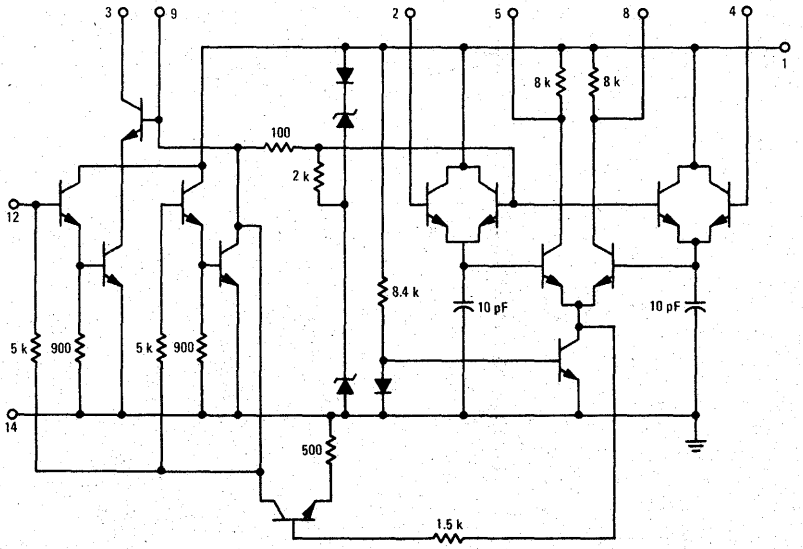
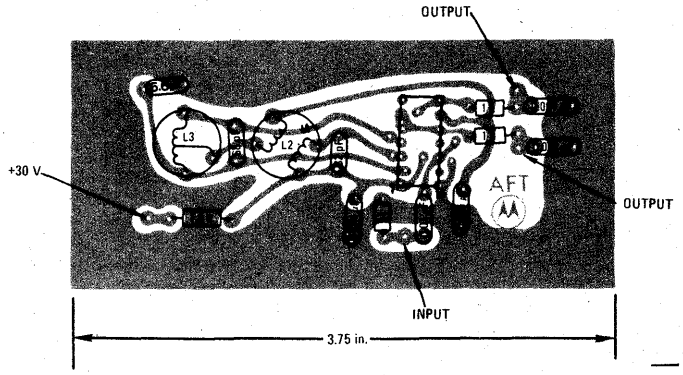


FIGURE 6 – PRINTED CIRCUIT BOARD AND PARTS ARRANGEMENT
(Copper Side)



7

ORDERING INFORMATION

Device	Temperature Range	Package
MC1375P	−40°C to +85°C	Plastic DIP

MC1375P

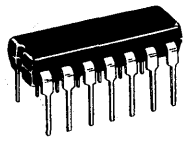
FM IF AMPLIFIER, LIMITER, FM DETECTOR, AND AUDIO PREAMPLIFIER

. . . a monolithic device designed for use in solid-state FM receivers.

- Excellent Sensitivity: Input Limiting Voltage (Knee) = 250 μV typical
- Excellent AM Rejection: 55 dB typical at 10.7 MHz
- Internal Zener Diode Regulation for the IF Amplifier Section
- Low Harmonic Distortion
- Differential Peak Detection: Permits Simplified Single-Coil Tuning
- Audio Preamplifier Voltage Gain: 21 dB typical
- Minimum Number of External Parts Required
- Direct Replacement for CA3075

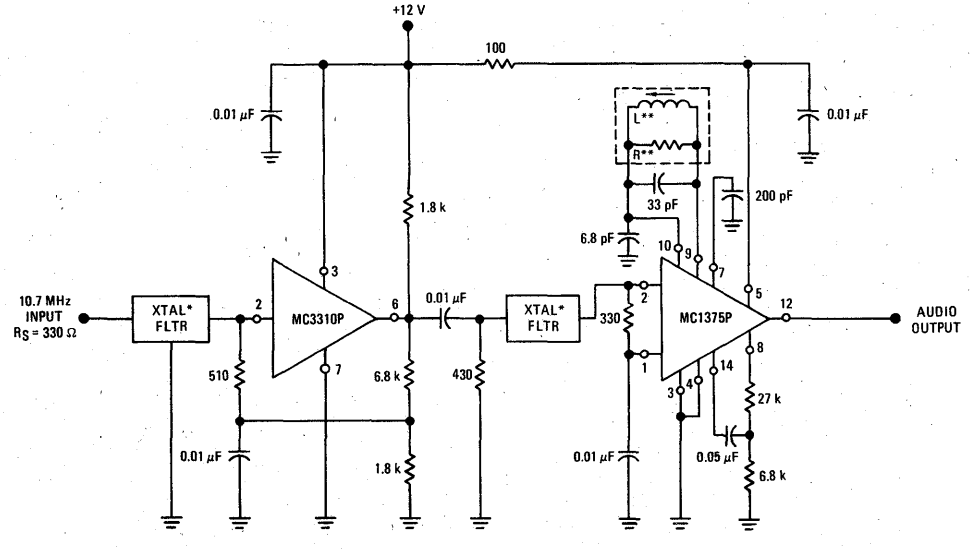
FM IF AMPLIFIER, LIMITER, FM DETECTOR AND AUDIO PREAMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

FIGURE 1 – TYPICAL FM APPLICATION



*10.7 MHz Filter; Vernitron FM-4 or equivalent
**L = 6.0 μH nom
Adjust R for $Q_L \approx 55$

Pins not shown are not connected.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	+16	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +11.2 Vdc, V_{EE} = Gnd, T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Current Drain	–	19	29	mA
DC Voltage at pin 8 (V_{in} = 0)	–	5.4	–	Vdc
Amplifier Input Resistance (V_{in} = 20 mV, 10.7 MHz)	–	5.0	–	kΩ
Amplifier Input Capacitance (V_{in} = 20 mV, 10.7 MHz)	–	5.0	–	pF

DYNAMIC CHARACTERISTICS (V_{CC} = +11.2 Vdc, V_{EE} = Gnd, f_{mod} = 1.0 kHz, T_A = +25°C unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
IF AMPLIFIER AND DETECTOR (f_O = 10.7 MHz, Δf = ± 75 kHz)				
AM Rejection* (V_{in} = 10 mV)	–	55	–	dB
Input Limiting Threshold Voltage	–	250	600	μV(RMS)
Recovered Audio Output Voltage	500	625	–	mV(RMS)
Output Distortion (V_{in} = 10 mV[RMS])	–	0.75	–	%
Signal-to-Noise Ratio (V_{in} = 1.0 mV)	–	68	–	dB
AUDIO AMPLIFIER (Audio Test Frequency; f = 1.0 kHz)				
Voltage Gain (V_{in} = 100 mV)	–	21	–	dB
Total Harmonic Distortion (V_O = 2.0 V[RMS])	–	1.2	–	%
Input Impedance (pin 14)	–	100	–	kΩ

*100% FM, 30% AM Signal

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TYPICAL CHARACTERISTICS

(All measurements at T_A = +25°C, V_{CC} = 11.2 V; see test circuits of Figure 9 and 10.)

FIGURE 2 – AM REJECTION

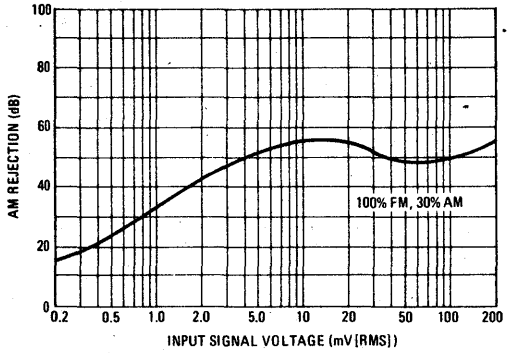


FIGURE 3 – RECOVERED AUDIO OUTPUT

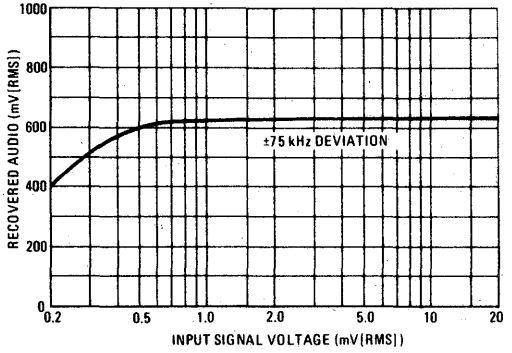


FIGURE 4 – IF AMPLIFIER AND DETECTOR THD

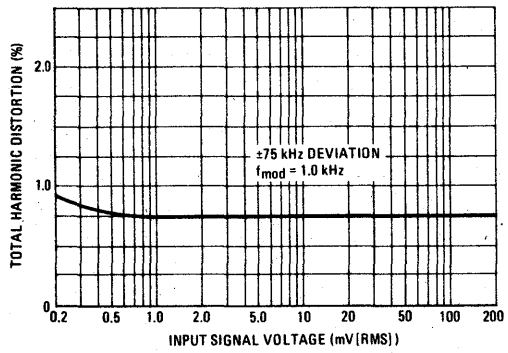


FIGURE 5 – SIGNAL TO NOISE

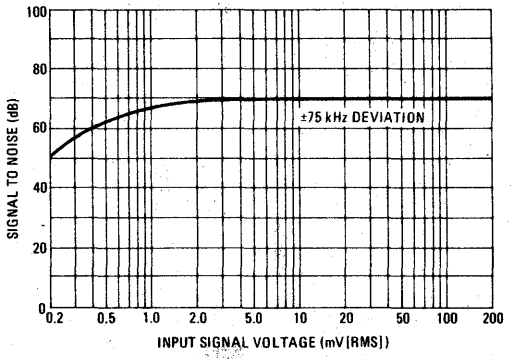


FIGURE 6 – AUDIO AMPLIFIER THD

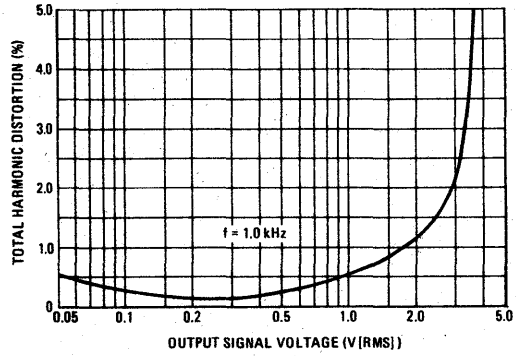


FIGURE 7 – CURRENT DRAIN versus SUPPLY VOLTAGE

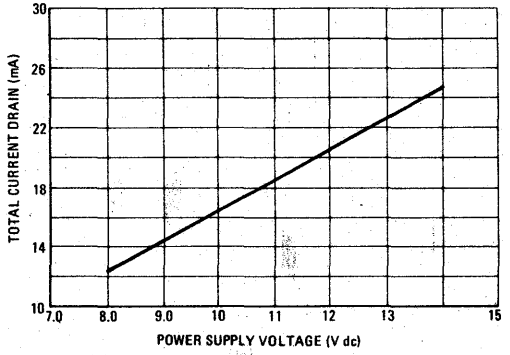


FIGURE 8 – CIRCUIT SCHEMATIC

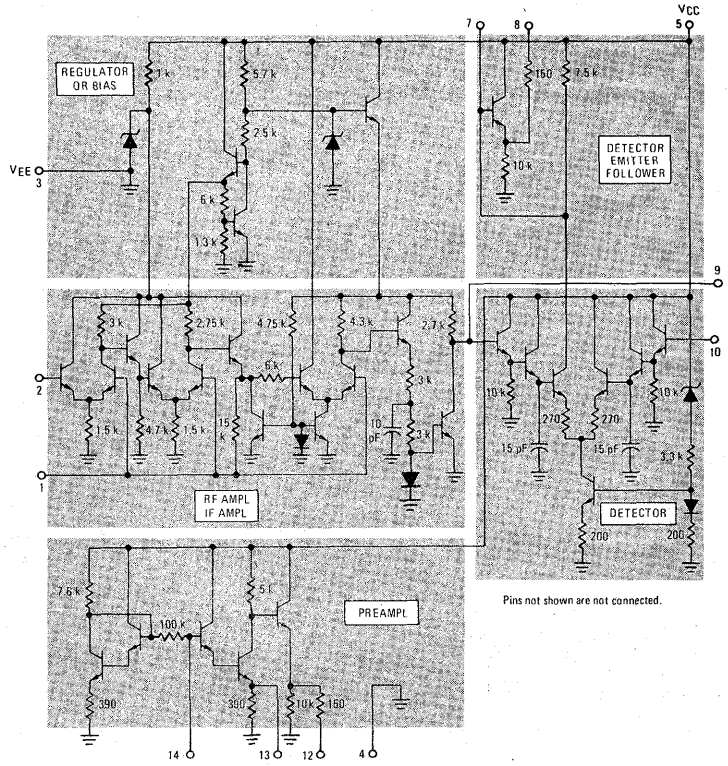


FIGURE 9 – AM REJECTION, THD, RECOVERED AUDIO, AND S/N TEST CIRCUIT

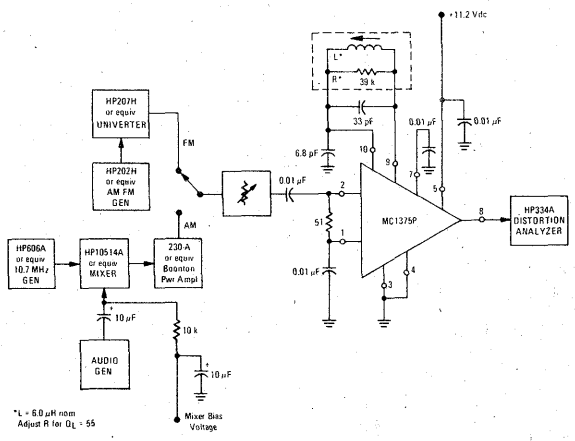
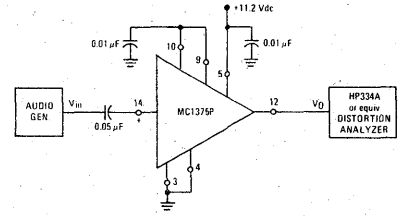


FIGURE 10 – AUDIO VOLTAGE GAIN AND THD TEST CIRCUIT



7

MC1384

Advance Information

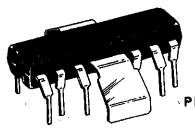
5-WATT AUDIO POWER AMPLIFIER

The MC1384 is a monolithic integrated circuit intended for use as a low frequency class B amplifier. It provides 5 watts typical of audio power output at 16 volts and 4 ohms, 4 watts typical at 14.4 volts and 4 ohms, 2 watts typical at 9 volts and 4 ohms, and works with a wide range of supply voltages (4 to 20 volts).

- Thermal Shutdown
- Wide Supply Voltage Range (4 to 20 Volts)
- High Current Capability
- "Angel" Power Package

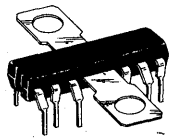
5-WATT AUDIO POWER AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



PQ SUFFIX
PLASTIC PACKAGE
CASE 722A

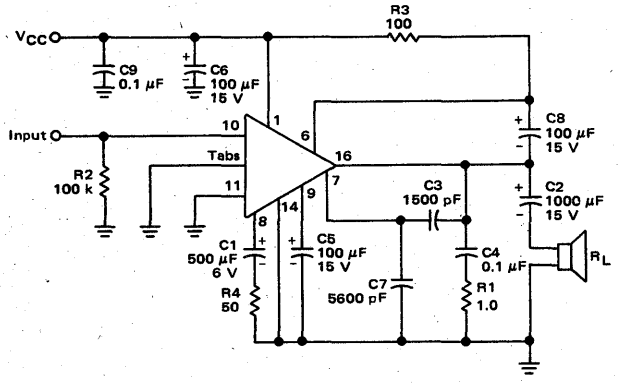
PQM SUFFIX
PLASTIC PACKAGE
CASE 722



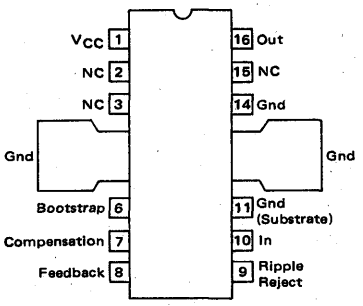
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	20	V
Output Peak Current (Non-Repetitive)	I_O	3.5	A
Output Current (Repetitive)	I_O	2.5	A
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Temperature Range	T_A	0 to +70	°C

FIGURE 1 – TYPICAL APPLICATION CIRCUIT



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC1384PQ	0 to +70°C	Plastic
MC1384PQM	0 to +70°C	Plastic

This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_{CC} = 14.4 Vdc, R_L = 4.0 Ω, f = 1.0 kHz, T_A = 25°C unless otherwise noted, see Figure 1 test circuit.)

Characteristic	Symbol	Min	Typ	Max	Unit
Quiescent Drain Current (e_{in} = 0)	I_D	–	12	20	mA
Quiescent Output Voltage (e_{in} = 0)	V_O	–	7.4	–	V
Bias Current	I_b	–	0.4	–	μA
Power Output (10% Distortion)	P_o				W
V_{CC} = 16 V		–	5.0	–	
V_{CC} = 14.4 V		–	4.0	–	
V_{CC} = 9.0 V		–	2.0	–	
Sensitivity, Input Voltage (P_O = 4.0 watts)	e_{in}				mV
R_f = 56 Ω		–	50	–	
R_f = 22 Ω		–	22	–	
Input Resistance	r_i	–	5.0	–	MΩ
Frequency Response (–3.0 dB)	f_B				Hz
C_3 = 820 pF		–	40-20,000	–	
C_3 = 1500 pF		–	40-10,000	–	
Distortion (P_o = 50 mW to 1.0 W)	d	–	0.4	–	%
Open-Loop Voltage Gain	A_{VOL}	–	80	–	dB
Closed-Loop Voltage Gain	A_{VCL}	–	38	–	dB
Equivalent Input Noise (R_S = 0, Bandpass = 20 Hz to 20 kHz)	e_n	–	2.0	–	μV
Power Supply Rejection Ratio (f_{ripple} = 1.0 kHz)	PSRR	–	38	–	dB

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ORDERING INFORMATION

Device	Temperature Range	Package
MC1385P	−40°C to +85°C	Plastic DIP

MC1385

CLASS B AUDIO DRIVER

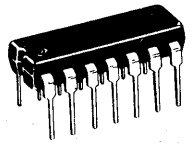
The MC1385 Class B Audio Driver is ideal for low voltage single-supply audio driver applications as found in consumer and industrial electronics.

Along with excellent audio reproduction, care has been taken to design in features significant to the automotive radio such as short circuit protection, supply line transient protection (commonly called "load dump"). Because of the current limiting shut down circuit, the requirement for a large heat sink has been significantly reduced.

- Internal Power Supply Transient Protection
- Built-In Programmable Short-Circuit Current Limiting
- Reduced Heat Sink Requirement
- Excellent Power-Supply Ripple Rejection – 35 dB Typ
- Typical Operation from 9.0 Vdc to 16 Vdc
- Excellent Sensitivity – 4.0 mV (Typ) for 1 W
- 5-Watt Driving Capability

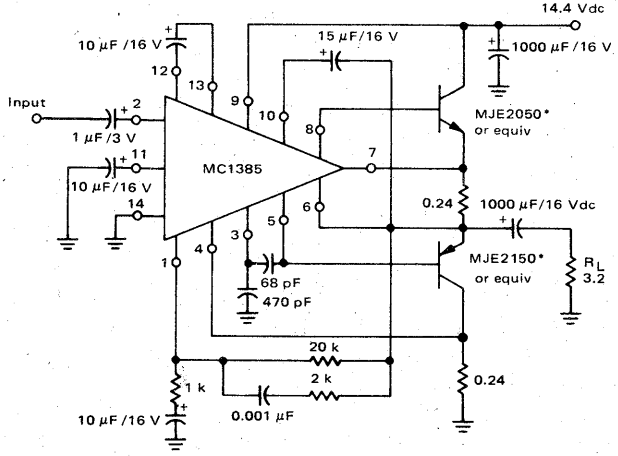
CLASS B AUDIO DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

FIGURE 1 – TYPICAL APPLICATION CIRCUIT



*For idle current considerations, power transistors used with the MC1385 driver require $V_{BE(on)}$ @ I_C = 50 mA, 0.65 V-0.69 V, V_{CE} = 5.0 Vdc, T_C = 25°C.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

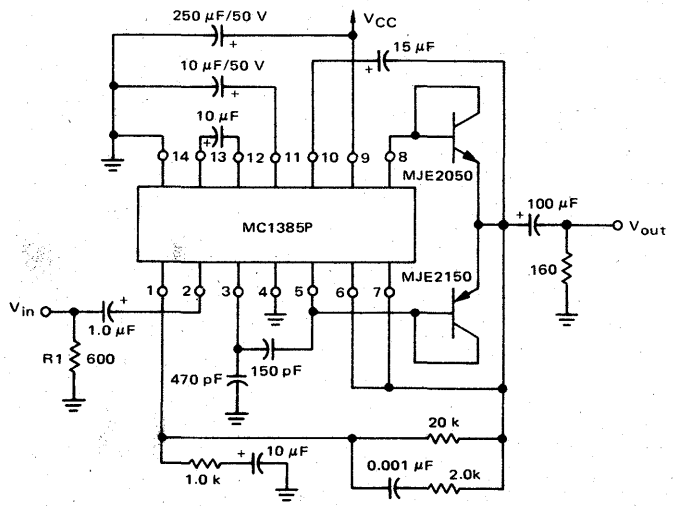
Rating	Value	Unit
Power Supply Voltage — Steady State Transients of 50 ms or less (1)	25 40	Vdc
Maximum Sink or Source Current Pin 5 or 8	50	mA
Power Dissipation (Package Limitation) @ T_A = 25°C Derate Above +25°C	625 5.0	mW mW/°C
Operating Ambient Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 14.4 Vdc, R_L = 3.2 ohms, f = 1.0 kHz, T_A = +25°C unless otherwise noted.)

Characteristic	Figure	Min	Typ	Max	Unit
Voltage Gain (V_{in} = 10 mVRMS, V_{CC} = 14.4 Vdc, R2 = 160 Ω, f = 1.0 kHz)	2	400	–	–	Vdc
Total Harmonic Distortion (V_{out} = 4.0 VRMS, R2 = 160 Ω, f = 1.0 kHz)	2	–	–	5.0	%
Power Supply Overvoltage Shutdown (1)	–	–	22	–	Vdc
Drain Current	2	–	10	–	mA
Power Output (THD = 10%)	1	–	6.7	–	W
Input Sensitivity Voltage (P_O = 1.0 W)	1	–	4.0	–	mV(RMS)
Total Harmonic Distortion (P_O = 1.0 W)	1	–	0.5	–	%
Output Noise (BW = 50 Hz to 6.0 kHz, Input Shorted)	1	–	2.0	–	mV(RMS)
Power-Supply Rejection (Ripple = 1.0 V(p-p) @ f = 1.0 kHz)	2	–	35	–	dB
Input Impedance	–	–	5.0	–	kΩ
Efficiency @ 5-Watts	1	–	69	–	%
Recommended Heat Sink Temperature Coefficient for Output Device Mounting (Figure 15)	1	–	6.0	–	°C/W

(1) These specifications were developed to meet typical automotive load dump requirements.

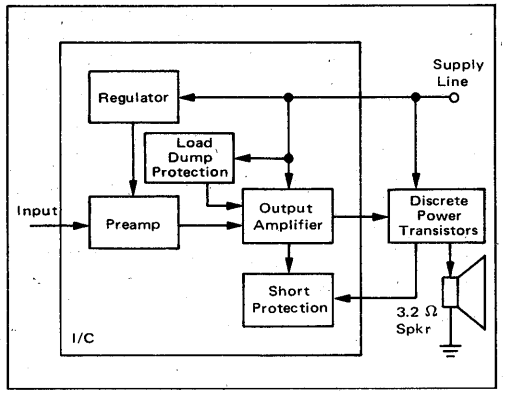
FIGURE 2 – TEST CIRCUIT



CIRCUIT DESCRIPTION

The total system is shown in Figure 3. The signal path consists of two closed-loop blocks: the preamplifier and the output amplifier. This configuration allows improved ripple rejection and a faster turn-on time than with a single closed-loop system. The two principal fault modes of overvoltage and overcurrent are avoided by the "load dump" and "short circuit" blocks respectively. The regulator provides the preamplifier with immunity to the noise injected on the supply line.

FIGURE 3 – SYSTEM BLOCK DIAGRAM



The regulator circuitry is shown in Figure 5. Noise voltage on the supply line is attenuated by the RC filter network of R1 + R2 and C1. The preamplifier supply line noise is further attenuated by the ratio of R3 to the small signal impedance of Z1 which is about 40 Ω. The noise injected at the base of S1 is determined by the ratio of R14 to the impedance on the base of S1.

The output impedance of Q5 is small compared to C2 and the input impedance of S1 is large, so the impedance at the base of S1 is C2 in parallel with R15.

The preamplifier is a two stage amplifier with localized feedback. Device Q2 provides bias for the first gain stage Q3 which is directly coupled to the second gain stage Q4. The output device Q5 is an emitter follower with feedback provided by R11.

The output amplifier is a differential amplifier driving a Darlington, common-emitter stage.

The short circuit protection is provided by Q10 and Q12 in conjunction with two external resistors. The value of the external resistor is set by the choice of desired output peak current and Equation 1.

$$R_E = \frac{V_{BE(on)}\ Q10 \text{ or } Q12}{I_P} \qquad (1)$$

where I_P = desired output peak current

$V_{BE(on)}$ = 720 mV at 25°C

R_E = value of current limit resistor

Load dump protection, illustrated in Figure 5, is provided by three zener diodes, Z2, Z3 and Z4 and Q9. When the supply voltage exceeds the combined breakdown voltage of the three zener diodes (22 V typically) and the turn-on voltage of Q9, the base of Q15 and the collector of Q11 are pulled to the saturation voltage of Q9 or less than one volt. This completely turns off both external discrete devices which places them in a BV_{CER} condition. With R26 across the base-emitter junction of the MJE2050, the device will remain off and unharmed as long as the transient voltage excursion is below 40 volts.

PERFORMANCE OF PROTECTION CIRCUITS

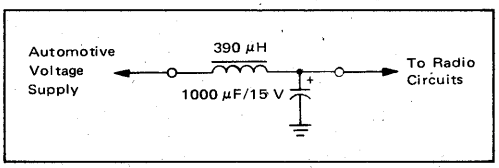
The MC1385 incorporates shut down circuits to prevent destruction of the MC1385 and outputs under these conditions.

As was shown in Figure 5, the supply line transient voltage shutdown circuit is a function of zener diodes Z2, Z3, Z4. The circuit shuts down the outputs for voltages on Pin 9 of 22.0 Vdc (typically).

The current limiting is adjustable by means of the resistors in the emitter of the MJE2050 and the collector of the MJE2150. Equation 1 may be used to select these resistors given the limit of peak output current, I_P, desired.

The selection of these resistors and consequently the short circuit current determines the amount of heat sinking required for the output devices. For example, with the resistors selected in the application circuit of Figure 1, the I_P is approximately 3.0 A with an average current of about 1.1 A. This circuit requires a heat sink of about 6.0°C/watt on the combined output devices to provide short circuit protection at V_{supply} of 14.4 Vdc and T_A = 25°C. It is suggested that the user measure the heat being developed in the output devices under his required short circuit test to make certain the output device T_{Jmax} of 150°C is not being exceeded.

FIGURE 4 – CONVENTIONAL A-LINE FILTERING



SUPPLY LINE FILTERING (ALTERNATOR WHINE)

Figure 4 represents the conventional method of filtering the automotive supply line.

The combination of the choke and 1000 μF capacitor attenuated the voltage transients (primarily alternator whine) on the A-line to a point where they are inaudible at the speaker output. However, the A-line choke represents a bulky, expensive component at a time when reduction of radio size is an important design goal.

Also due to its placement in series with the output devices, the impedance of the choke provides an undesirable voltage drop and therefore a reduction in audio power output.

Figure 6 illustrates a suggested A-line filtering scheme for use with the MC1385.

Experiments regarding alternator whine indicate that the 10 Ω series resistor and the existing 1000 μF A-line

FIGURE 5 – TOTAL SYSTEM SCHEMATIC

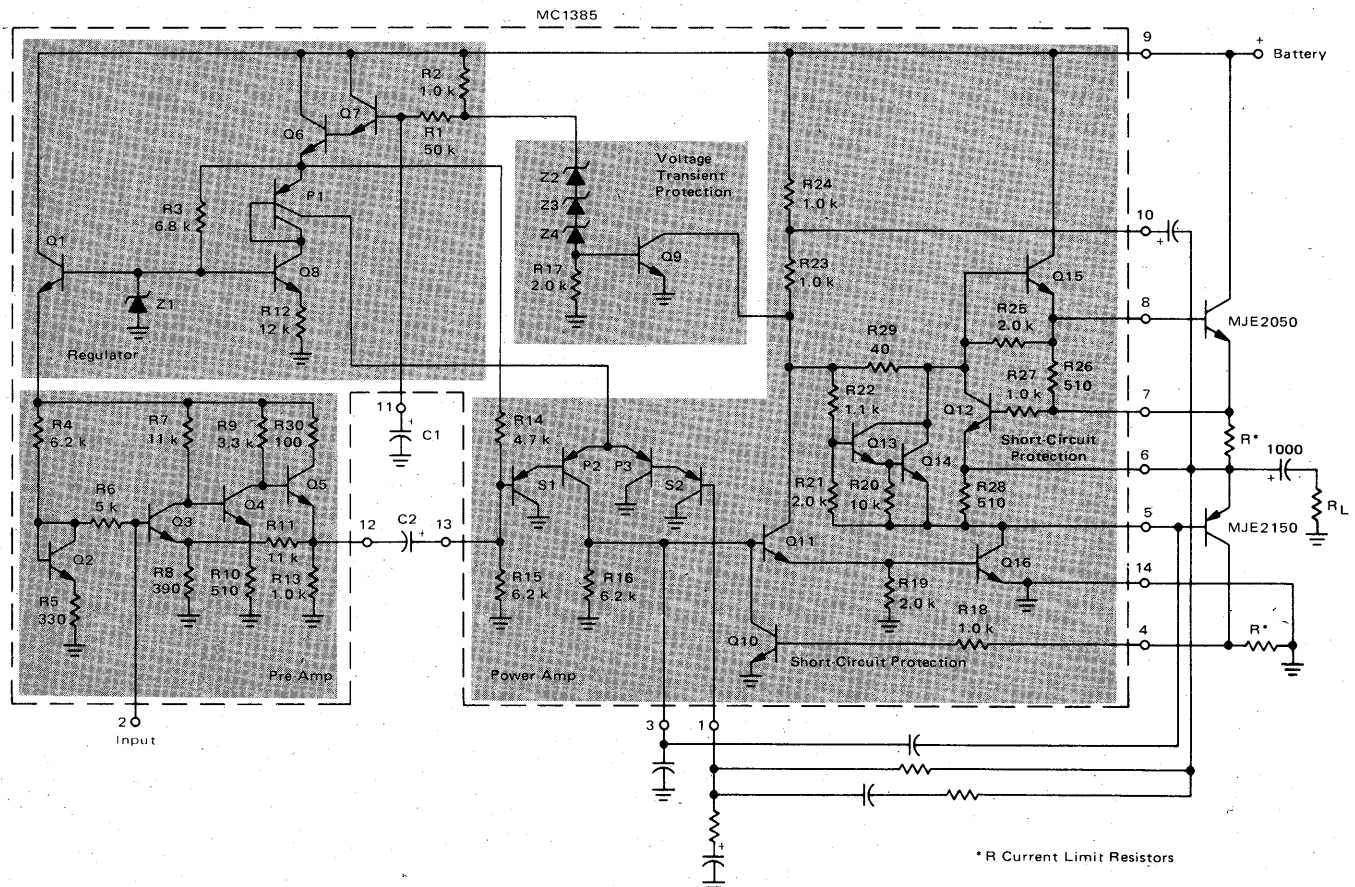
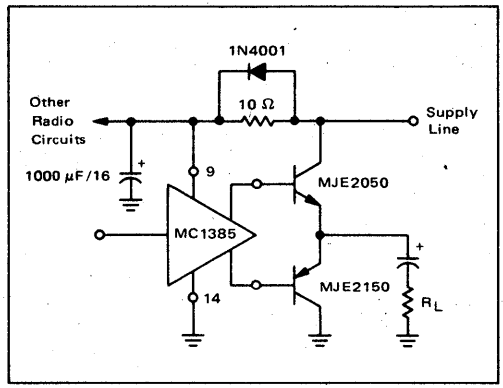


FIGURE 6 – SUGGESTED A-LINE FILTERING WITH MC1385



electrolytic are effective in attenuating alternator whine. The diode is included to permit the load dump portion of the I/C to be connected directly to the A-line and thus remove the time delay associated with the 10 Ω/1000 μF circuit. The diode is necessary if load dump protection is required.

PERFORMANCE AND APPLICATION INFORMATION

The following section covers performance characteristics and application information on the MC1385/MJE2050/MJE2150.

Figure 1 illustrates the typical circuit configuration that was used to generate the performance curves and data shown in Figures 7 thru 14. Performance measurements were made at 14.4 V; however, the test circuit in Figure 1 will operate satisfactorily over the automotive voltage range of 9-16 Vdc.

7

FIGURE 7 – TOTAL HARMONIC DISTORTION versus POWER OUTPUT

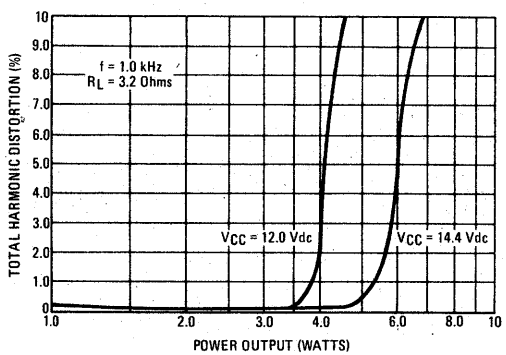


FIGURE 8 – POWER OUTPUT versus SUPPLY VOLTAGE

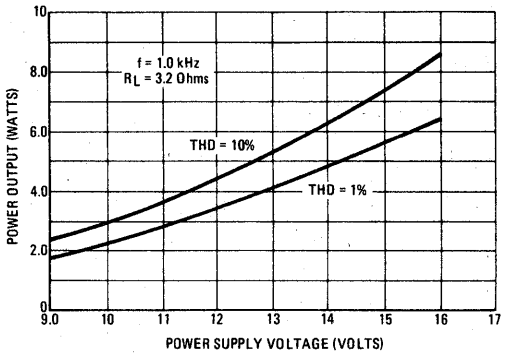


FIGURE 9 – POWER OUTPUT versus FREQUENCY @ 10% TOTAL HARMONIC DISTORTION

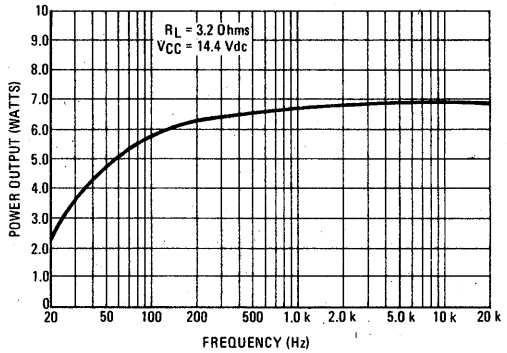


FIGURE 10 – TOTAL HARMONIC DISTORTION versus FREQUENCY @ 1.0 WATT OUTPUT

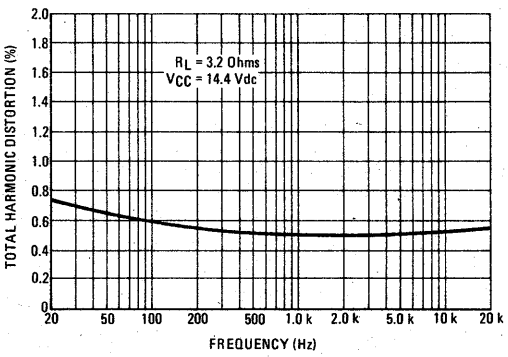


FIGURE 11 – POWER OUTPUT versus AMBIENT TEMPERATURE

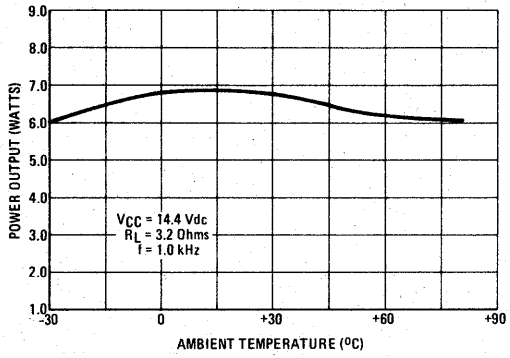


FIGURE 12 – IDLE CURRENT versus AMBIENT TEMPERATURE

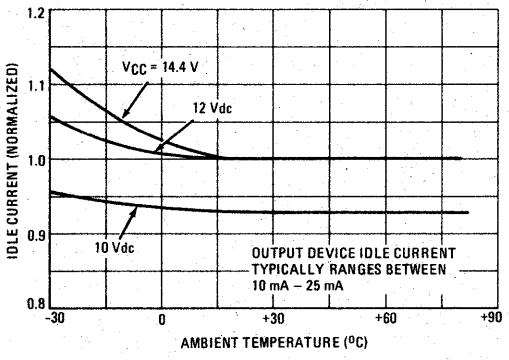


FIGURE 13 – POWER OUTPUT versus LOAD RESISTANCE @ 10% TOTAL HARMONIC DISTORTION

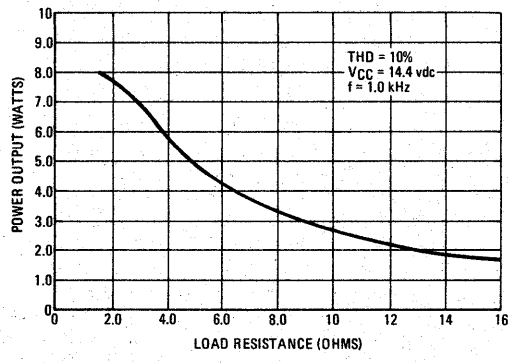


FIGURE 14 – POWER SUPPLY REJECTION versus POWER SUPPLY RIPPLE FREQUENCY

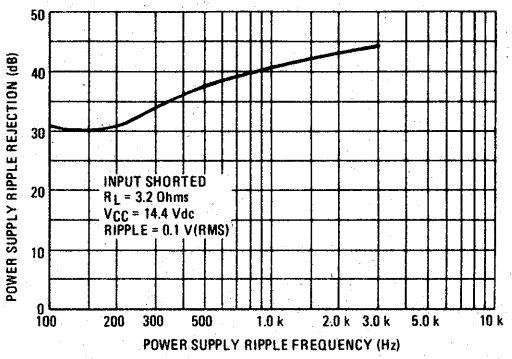
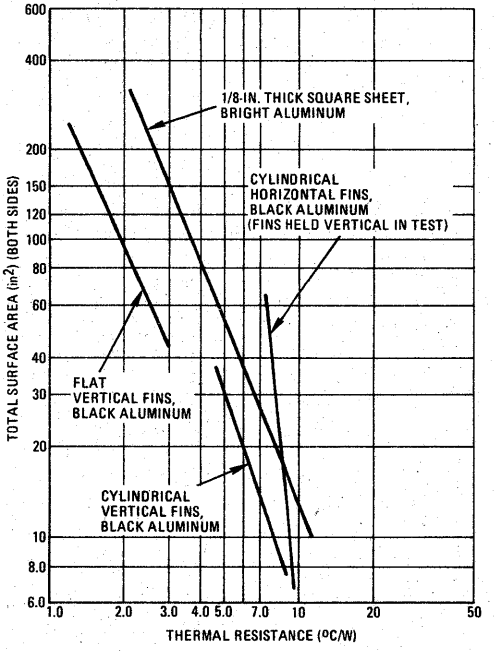


FIGURE 15 – CALCULATING TOTAL SURFACE AREA OF FABRICATED HEAT SINK FROM REQUIRED VALUE OF THERMAL RESISTANCE



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ORDERING INFORMATION

Device	Temperature Range	Package
MC1391P	0°C to +75°C	Plastic DIP
MC1394P	0°C to +75°C	Plastic DIP

MC1391P
MC1394P

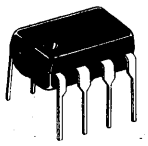
TV HORIZONTAL PROCESSOR

. . . low-level horizontal sections including phase detector, oscillator and pre-driver — a device designed for use in all types of television receivers.

- Internal Shunt Regulator
- Preset Hold Control Capability
- ±300 Hz Typical Pull-In
- Linear Balanced Phase Detector
- Variable Output Duty Cycle for Driving Tube or Transistor
- Low Thermal Frequency Drift
- Small Static Phase Error
- Adjustable dc Loop Gain
- MC1391P — Positive Flyback Inputs
- MC1394P — Negative Flyback Inputs

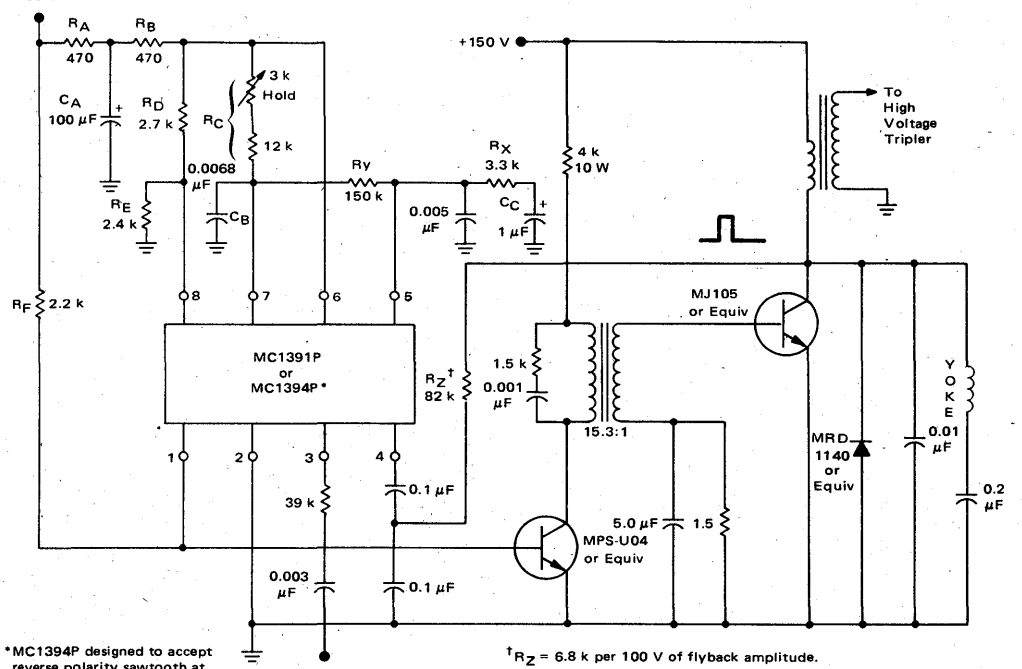
TV HORIZONTAL PROCESSOR

MONOLITHIC SILICON INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 626

FIGURE 1 – TYPICAL APPLICATION CIRCUIT



*MC1394P designed to accept reverse polarity sawtooth at Pin 4 if sync pulse not derived from MJ105 collector.

†R_Z = 6.8 k per 100 V of flyback amplitude.

-20 V Sync

This circuit has an oscillator pull-in range of ±300 Hz, a noise bandwidth of 320 Hz, and a damping factor of 0.8.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Supply Current	40	mAdc
Output Voltage	40	Vdc
Output Current	30	mAdc
Sync Input Voltage (Pin 3)	5.0	$V_{(p-p)}$
Flyback Input Voltage (Pin 4)	5.0	$V_{(p-p)}$
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted.) (See Test Circuit of Figure 2, all switches in position 1.)

Characteristic	Min	Typ	Max	Unit
Regulated Voltage (Pin 6)	8.0	8.6	9.0	Vdc
Supply Current (Pin 6)	–	20	–	mAdc
Collector-Emitter Saturation Voltage (Output Transistor Q1 in Figure 6) (I_C = 20 mA, Pin 1) Vdc	–	0.15	0.25	Vdc
Voltage (Pin 4)	–	2.0	–	Vdc
Oscillator Pull-in Range (Adjust R_H in Figure 2)	–	±300	–	Hz
Oscillator Hold-in Range (Adjust R_H in Figure 2)	–	±900	–	Hz
Static Phase Error (Δf = 300 Hz)	–	0.5	–	μs
Free-running Frequency Supply Dependance (S1 in position 2)	–	±3.0	–	Hz/Vdc
Phase Detector Leakage (Pin 5) (All switches in position 2)	–	–	±1.0	μA
Sync Input Voltage (Pin 3)	2.0	–	5.0	V(p-p)
Sawtooth Input Voltage (Pin 4)	1.0	–	3.0	V(p-p)

7

TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 2 – TEST CIRCUIT

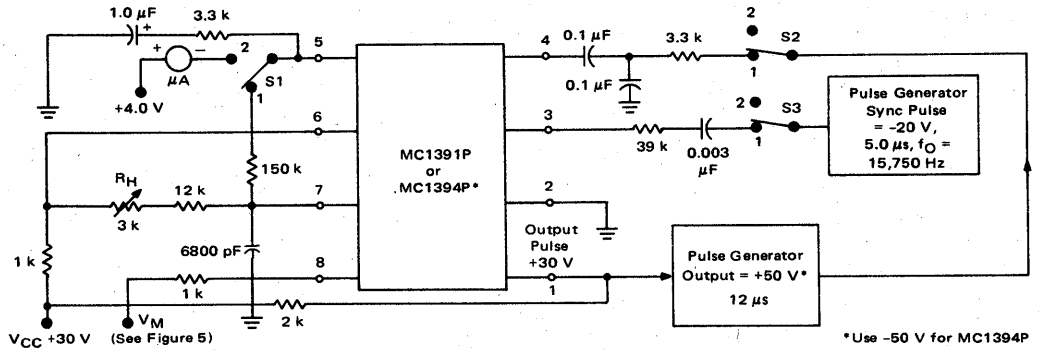


FIGURE 3 – FREQUENCY versus TEMPERATURE

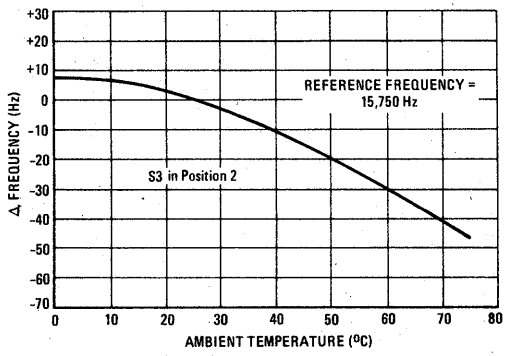


FIGURE 4 – FREQUENCY DRIFT versus WARM-UP TIME

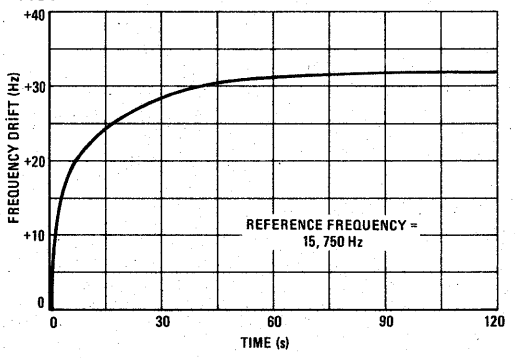


FIGURE 5 – MARK-SPACE RATIO

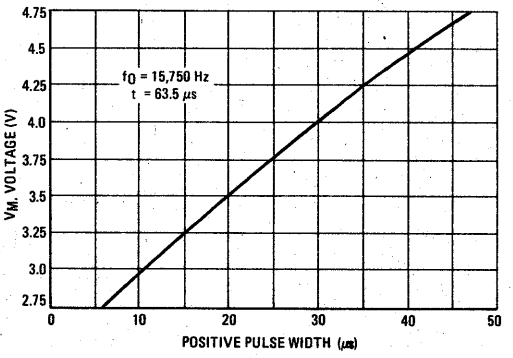
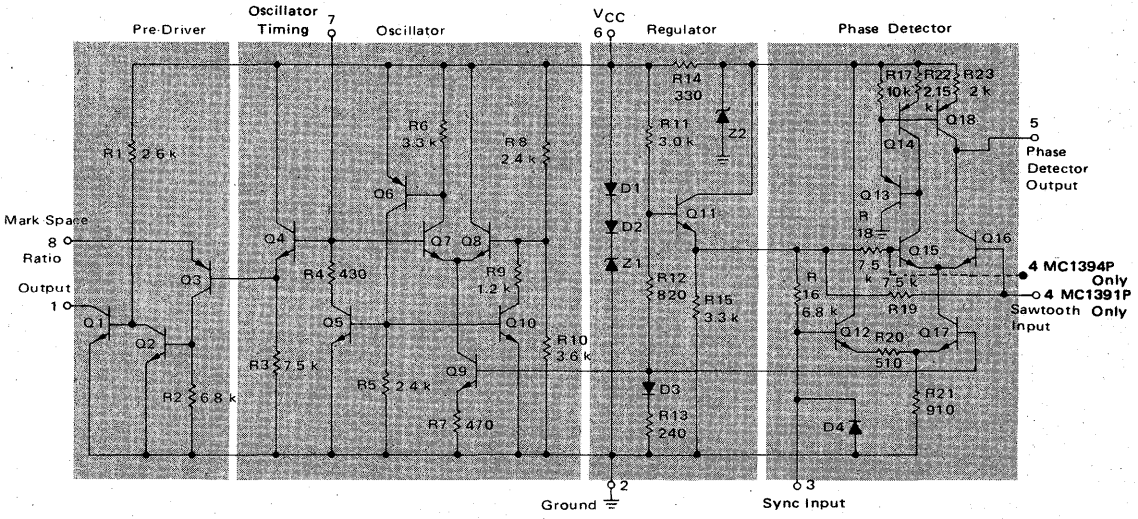


FIGURE 6 – CIRCUIT SCHEMATIC



CIRCUIT OPERATION

The MC1391P and MC1394P contain the oscillator, phase detector and predriver sections needed for a television horizontal APC loop.

The oscillator is an RC type with one pin (Pin 7) used to control the timing. The basic operation can be explained easily. If it is assumed that Q7 is initially off, then the capacitor connected from Pin 7 to ground will be charged by an external resistor (R_C) connected to Pin 6. As soon as the voltage at Pin 7 exceeds the potential set at the base of Q8 by resistors R8 and R10, Q7 will turn on and Q6 will supply base current to Q5 and Q10. Transistor Q10 will set a new, lower potential at the base of Q8 determined by R8, R9 and R10. Then, transistor Q5 will discharge the capacitor through R4 until the base bias of Q7 falls below that of Q8, at which time Q7 will turn off and the cycle repeats.

The sawtooth generated at the base of Q4 will appear across R3 and turn off Q3 whenever it exceeds the bias set on Pin 8. By adjusting the potential at Pin 8, the duty cycle (MSR) at the predriver output pin (Pin 1) can be changed to accommodate either tube or transistor horizontal output stages.

The phase detector is isolated from the remainder of the circuit by R14 and Z2. The phase detector consists of the comparator Q15, Q16 and the gated current source Q17. Negative going sync pulses at Pin 3 turn off Q12 and the current division between Q15 and Q16 will be determined by the phase relationship of the sync and the sawtooth waveform at Pin 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents will flow in the collectors of Q15 and Q16 each for half the sync pulse period. The current in Q15 is turned around by Q18 so that there is no net output current at Pin 5 for balanced conditions. When a phase offset occurs, current will flow either in or out of Pin 5. This pin is connected via an external low-pass filter to Pin 7, thus controlling the oscillator.

Shunt regulation for the circuit is obtained with a zero temperature coefficient from the series combination of D1, D2 and Z1.

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APPLICATION INFORMATION

Although it is an integrated circuit, the MC1391P and MC1394P have all the flexibility of a conventional discrete component horizontal APC loop.

The internal temperature compensated voltage regulator allows a wide supply voltage variation to be tolerated, enabling operation from nonregulated power supplies. A minimum value for supply current into Pin 6 to maintain zener regulation is about 18 mA. Allowing 2mA for the external dividers

$$R_A + R_B = \frac{V_{nonreg(min)} - 8.8}{20 \times 10^{-3}}$$

Components R_A, R_B and C_A are used for ripple rejection. If the supply voltage ripple is expected to be less than 100 mV (for a 30 Volt supply) then R_A and R_B can be combined and C_A omitted.

The output pulse width can be varied from 6 μs to 48 μs by changing the voltage at Pin 8 (see Figure 5). However, care should be taken to keep the lead lengths to Pin 8 as short as possible to prevent ringing which can result in erroneous output pulses at Pin 1. The parallel impedance of R_D and R_E should be close to 1 kΩ to ensure stable pulse widths.

For 15 mA drive at saturation

$$R_F = \frac{V_{nonreg} - 0.3}{15 \times 10^{-3}}$$

The oscillator free-running frequency is set by R_C and C_B connected to Pin 7. For values of $R_C \gg R_{discharge}$ (R4 in Figure 6), a useful approximation for the free-running frequency is

$$f_O = \frac{1}{0.6\, R_C C_B}$$

Proper choice of R_C and C_B will give a wide range of oscillator frequencies – operation at 31.5 kHz for count-down circuits is possible for example. As long as the product $R_C C_B \approx 10^{-4}$ many combinations of values of R_C and C_B will satisfy the free-running frequency requirement of 15.734 kHz. However, the sensitivity of the oscillator (β) to control-current from the phase detector is directly dependent on the magnitude of R_C, and this provides a convenient method of adjusting the dc loop gain (fc).

For a given phase detector sensitivity (μ) = 1.60×10^{-4} A/rad

$$fc = \mu\beta \text{ and } \beta = 3.15 \times R_C \text{ Hz/mA}$$

Increasing R_C will raise the dc loop gain and reduce the static phase error (S.P.E.) for a given frequency offset. Secondary effects are to increase the natural resonant frequency of the loop (ω_n) and give a wider pull-in range from an out-of-lock condition. The loop will also tend to be underdamped with fast pull-in times, producing good airplane flutter performance. However, as the loop becomes more underdamped impulse noise can cause shock excitation of the loop. Unlimited increase in the dc loop gain will also raise the noise bandwidth excessively causing horizontal jitter with thermal noise. Once the dc loop gain has been selected for adequate S.P.E. performance, the loop filter can be used to produce the balance between other desirable characteristics. Damping of the loop is achieved most directly by changing the resistor R_X with respect to R_Y which modifies the ac/dc gain ratio (m) of the loop. Lowering this ratio will reduce the pull-in range and noise bandwidth (fnn). (Note: very large values of R_Y will limit the control capability of the phase detector with a corresponding reduction in hold-in range).

Static phasing can be adjusted simply by adding a small resistor between the flyback pulse integrating capacitor and ground. The sync coupling capacitor should not be too small or it can charge during the vertical pulse and this may result in picture bends at the top of the CRT.

NOTE:

In adjusting the loop parameters, the following equations may prove useful:

$$f_{nn} = \frac{1 + \chi^2 T\omega_c}{4\chi T} \qquad \chi = \frac{R_X}{R_Y}$$

$$\omega_n = \sqrt{\frac{\omega_c}{(1+\chi)\,T}} \qquad \omega_c = 2\pi fc$$

$$T = R_Y C_C$$

$$K = \frac{\chi^2 T\omega_c}{4}$$

where:

K = loop damping coefficient

7

MC1393

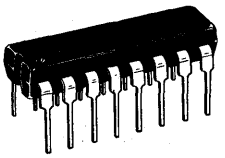
TV VERTICAL PROCESSOR

. . . designed for universal use in black and white as well as large-screen color television receivers.

- Injection Locked Oscillator
- Greater Than 12 Hz Injection
- Low Thermal Drift
- Eliminates Centering Control
- Independent Vertical Hold and Size Controls
- Scan Current Independent of Yoke Variations
- Retrace Pulse for Effective Blanking
- Linear Sawtooth Amplification

TV VERTICAL PROCESSOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

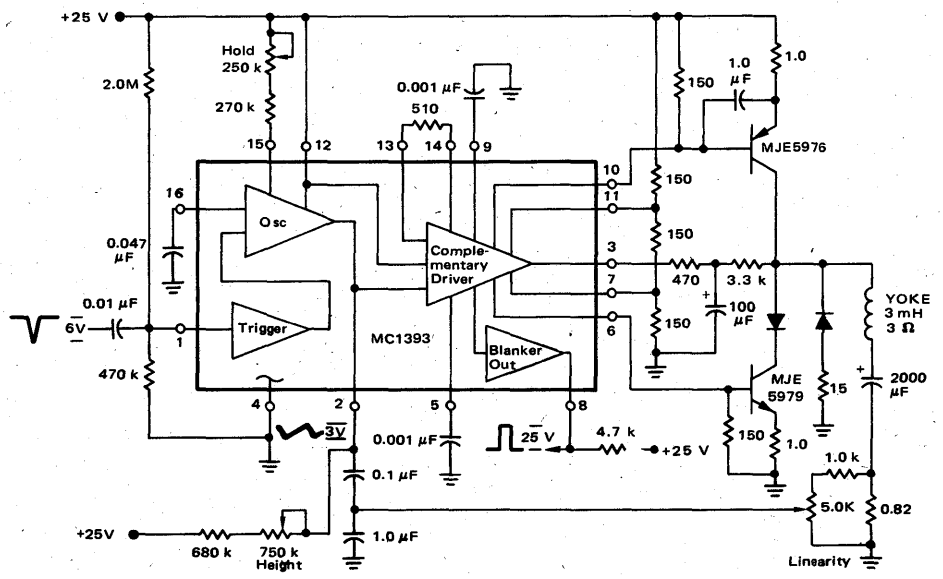


PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

Device	Temperature Range	Package
MC1393	0 to +70°C	Plastic DIP

FIGURE 1 – TYPICAL APPLICATION CIRCUIT



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage	30	Vdc
Junction Temperature	150	°C
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +25 V, T_A = +25°C) (Figure 1)

Characteristic	Typ	Unit
Supply Drain(1)	525	mAdc
Oscillator Frequency (Pin 16)	60	Hz
Oscillator Supply Sensitivity	0.3	Hz/V
Oscillator Drift	130	PPM/°C
Oscillator Injection (Pull-In)	12	Hz
Driver Input Sawtooth Amplitude (Pin 2)	3.0	$V_{(p-p)}$
Output Current (Yoke)	3.0	$A_{(p-p)}$
Scan Non-Linearity	8.0	%

Note 1: Total Current Includes Current in Circuit External to the IC.

CIRCUIT DESCRIPTION

7

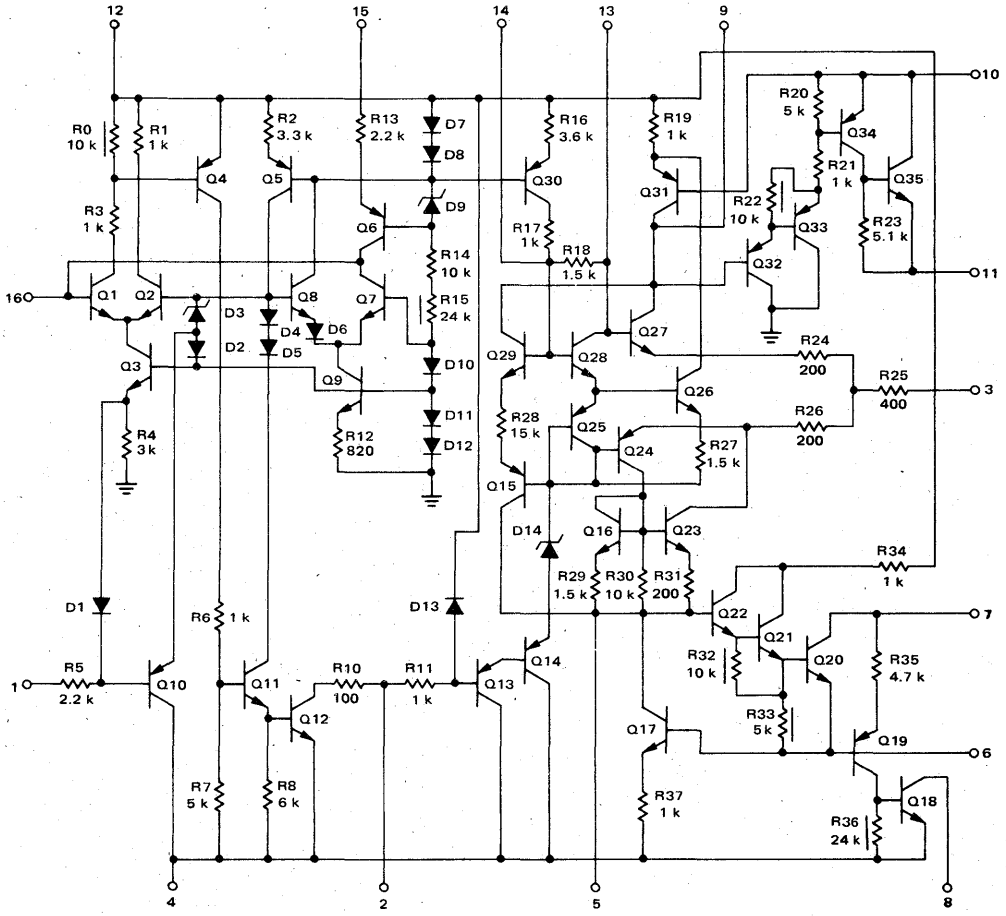
Oscillator

The oscillator employs two differential amplifiers (Q1, Q2, and Q7, Q8). A capacitor at Pin 16 is charged by a current source Q6 until it reaches a voltage that turns on Q1. Q7 is turned on by Q1 providing a discharge path for the voltage stored at Pin 16. Q12 is on during the same period as Q1, and provides a discharge path for a ramp generated at Pin 2. Q1 stays on until the capacitor voltage is discharged to a level that turns Q7 off. A negative sync pulse at Pin 1 turns Q10 on and increases the oscillator frequency by lowering the Q1 switching voltage.

Complementary Driver

A sawtooth generated at Pin 2 is level shifted to the driver inputs Q24 and Q27. Q17 and an NPN output transistor at Pin 6 are a current driver function for one-half of the output. Q20 acts as a current amplifier providing base current for the NPN output transistor. The current gain between Q20 and the output transistor is inversely proportional to the resistance ratio of R37 and the output emitter resistor. 1.0 mA of current through R37 will produce 1.0 A through a 1.0 ohm output-emitter resistor, thus providing a gain of 1000. Q20, Q31 and a PNP output transistor at Pin 10 are a second current driver function, making up the other half of the complementary output. Q35 provides base current for the output. The maximum amount of base current drive is determined by the current in the voltage divider on Pins 7 and 11. Pin 3 is a return path for the dc and provides for automatic centering. Pin 8 is the collector output of Q18 providing a positive blanking pulse.

FIGURE 2 – CIRCUIT SCHEMATIC



ORDERING INFORMATION

Device	Temperature Range	Package
MC1398P	−20°C to +75°C	Plastic DIP

MC1398

TV COLOR PROCESSING CIRCUIT

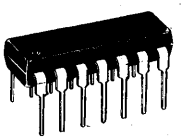
. . . a chroma IF amplifier with automatic chroma control, color killer, dc chroma control, and injection lock reference system followed by dc hue control.

MC1398P is a monolithic device designed for use in solid-state color television receivers.

- Minimum Number of External Components
- DC Control of Both Chroma Amplitude and Hue Shift
- Crystal-Controlled Internal Feedback Oscillator
- Built-in Noise Immunity
- Schmitt Trigger Color Killer
- Automatic Chroma Control
- Internal Burst Gate and Gate Pulse Shaping Circuit
- High Oscillator Lock-in Sensitivity
- Built-in Supply Regulation

TV COLOR PROCESSING CIRCUIT

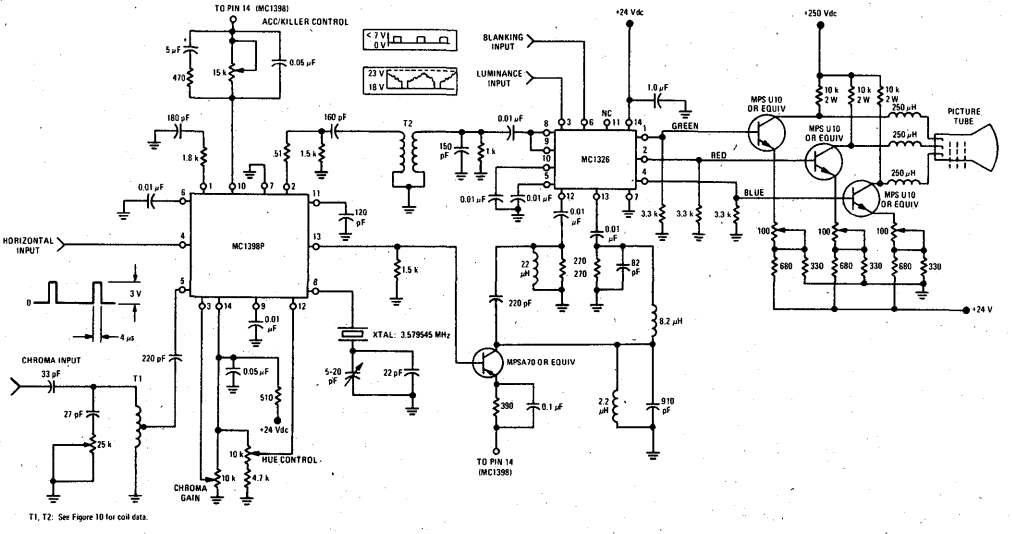
SILICON MONOLITHIC INTEGRATED CIRCUIT



PLASTIC PACKAGE
CASE 646

7

FIGURE 1 – TYPICAL CHROMA APPLICATIONS CIRCUIT
(MC1398P, MC1326 and MPSU10)



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

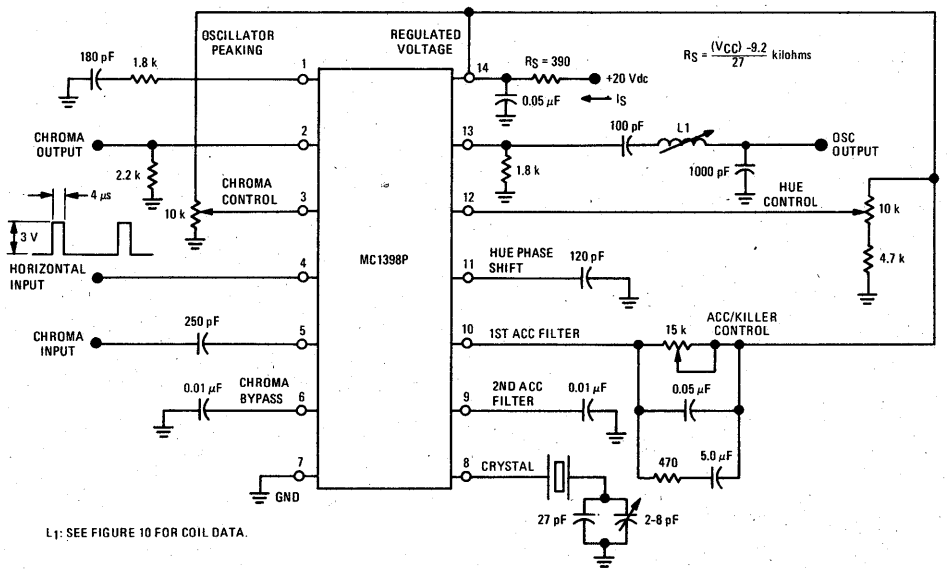
Rating	Value	Unit
Power Supply Current	35	mAdc
Horizontal Pulse Input Current	250	μA Peak
Power Dissipation (package limitation) Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	-20 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, R_S = 390 ohms, T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Regulated Voltage (I_S = 35 mA) (I_S = 27 mA)	9.0 –	9.6 9.2	11.5 –	Vdc
Maximum Undistorted Chroma Output, See Note 1, $E_{(pin\ 3)} = E_{(pin\ 14)}$	0.8	1.75	–	V(p-p)
Maximum Chroma Gain $E_{(pin\ 3)} = E_{(pin\ 14)}$, See Note 1	34	40	–	dB
Automatic Chroma Control Range (ACC) -3.0 dB down from maximum undistorted output, see Note 1	–	19	–	dB
Chroma Burst Level to Kill, See Note 1	–	1.4	–	mV(p-p)
Manual Chroma Gain Control Range ($\Delta V_{(pin\ 3)}$) ($V_{(pin\ 14)}$ to 0 Vdc)	50	60	–	dB
Chroma Input Resistance	–	2.3	–	k ohms
Chroma Input Capacitance	–	13	–	pF
Chroma Output Impedance	–	15	–	ohms
Horizontal Input Pulse	2.2	3.0	4.0	Vp
Oscillator Output	100	–	–	mV(RMS)
Oscillator Output Impedance	–	15	–	ohms
Hue Control Range ($\Delta V_{(pin\ 12)}$) ($V_{(pin\ 14)}$ to 4.3 Vdc)	100	126	–	degrees
Oscillator Pull-In Range	1200	–	–	Hz
Oscillator Noise Bandwidth (f_N)	–	900	–	Hz
Static Phase Error with Oscillator Detuning 25 mV(p-p) Burst Amplitude 2.0 mV(p-p) Burst Amplitude	– –	0.20 0.25	– –	degrees/Hz

Note 1: With 5.0 mV(p-p) burst input at pin 5 set $E_{(pin\ 10)}$ to just "unkill".

FIGURE 2 – MC1398P TEST CIRCUIT



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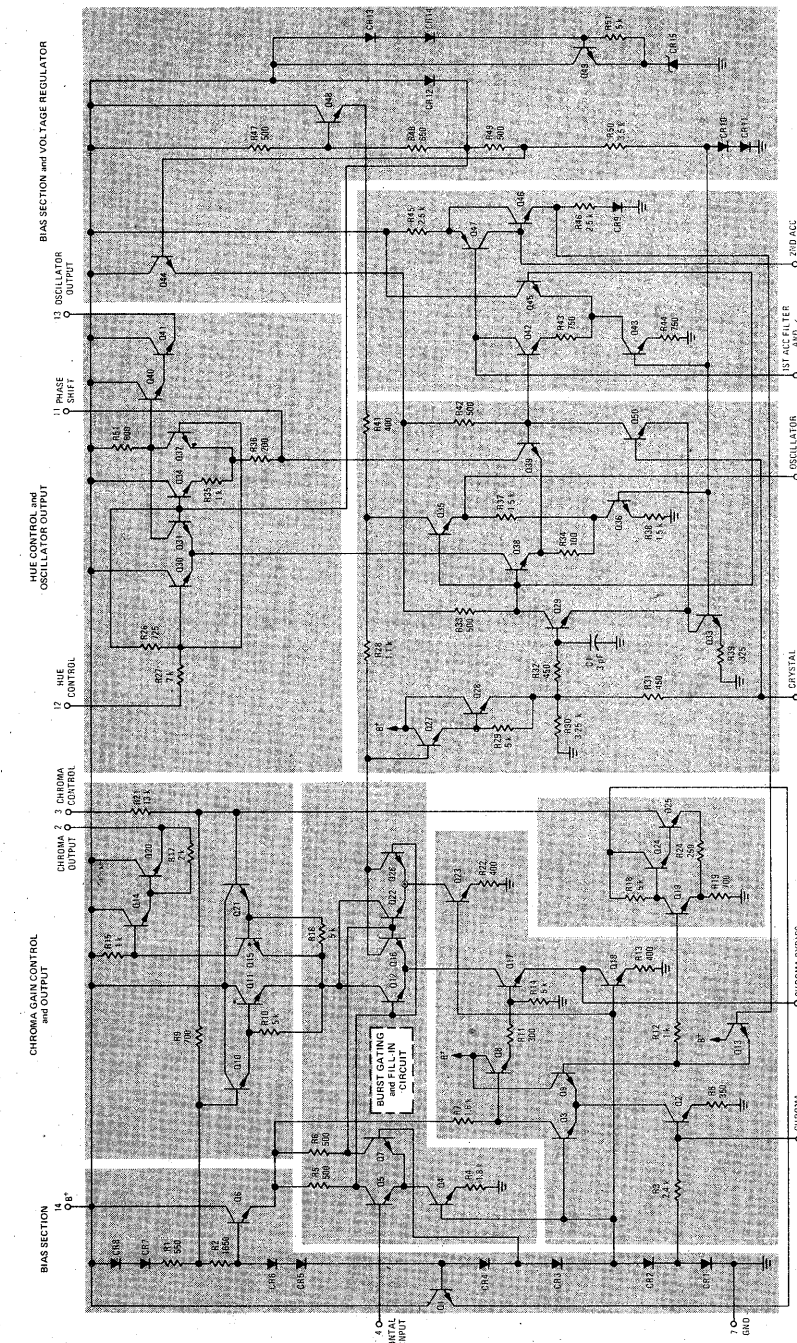

FIGURE 3 – MC1398 CIRCUIT SCHEMATIC

7

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted)

(Figures 4 through 9, See Test Circuit of Figure 2.)

FIGURE 4 – INPUT/OUTPUT CHARACTERISTICS

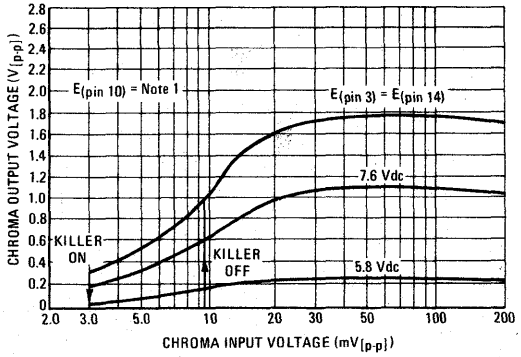

FIGURE 5 – REGULATED VOLTAGE

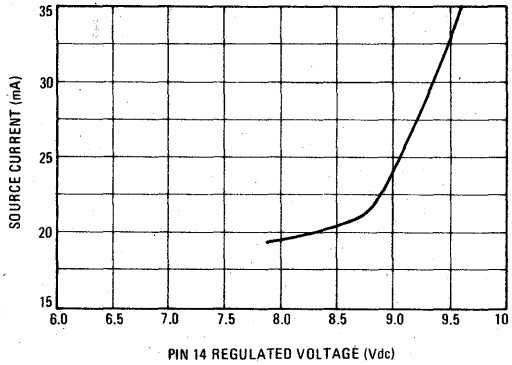

FIGURE 6 – HUE CONTROL OPERATION

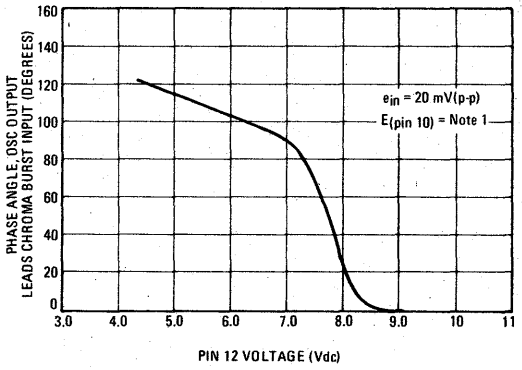

FIGURE 7 – OSCILLATOR OUTPUT versus PIN 12 VOLTAGE

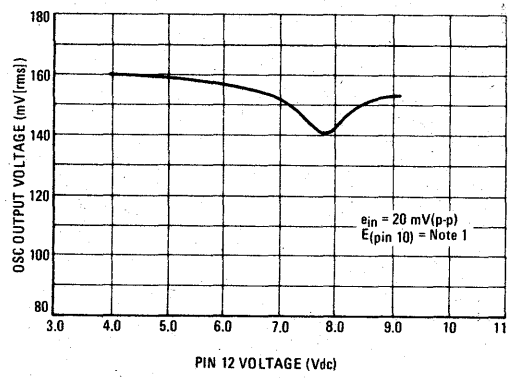

FIGURE 8 – STATIC PHASE ERROR

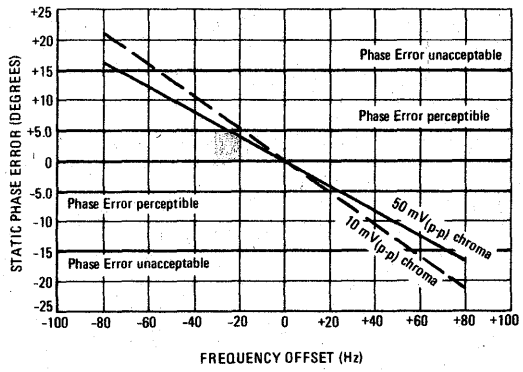

FIGURE 9 – TEMPERATURE STABILITY of the MC1398 OSCILLATOR

(I/C only subjected to temperature change)

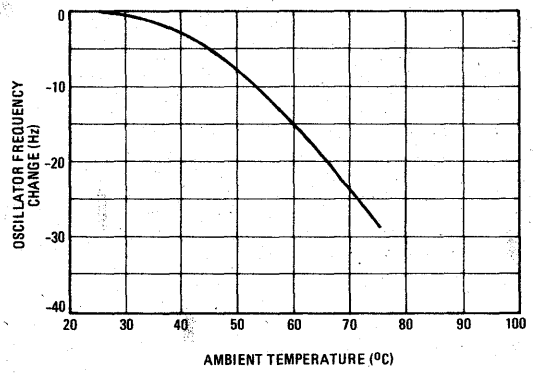

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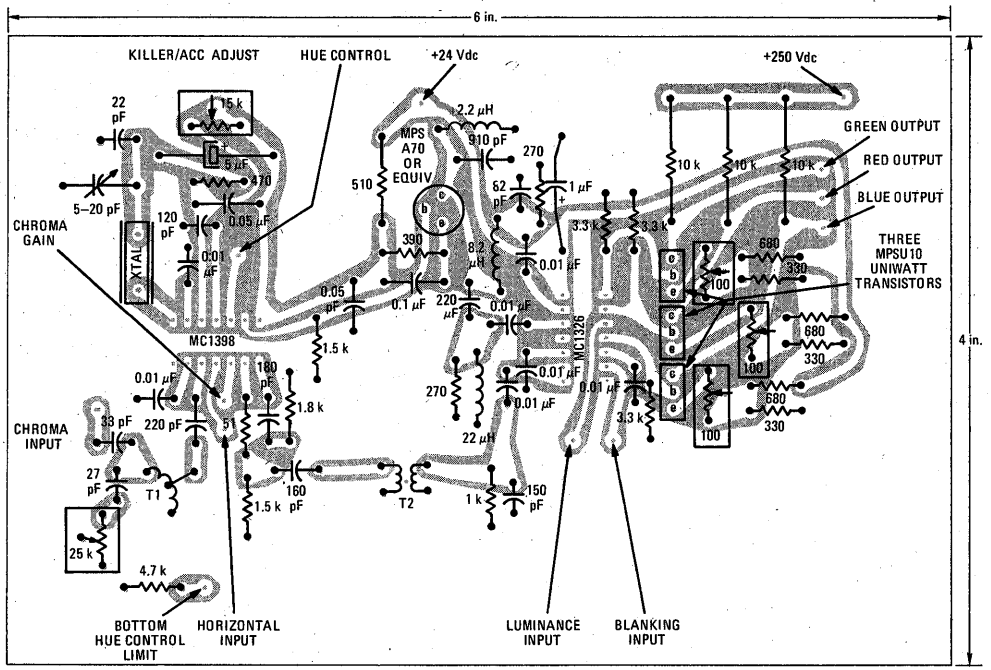
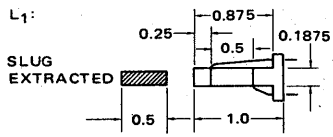
FIGURE 10 – PRINTED CIRCUIT LAYOUT OF MC1398P, MC1326, and MPSU 10 TRANSISTORS



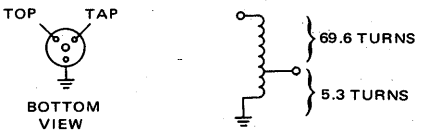
NOTES:
All resistors are 1/4 W unless otherwise noted.
(Copper Side Shown)

L_1:



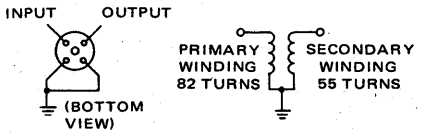
L_1: 80 TURNS OF STANDARD #38 AWG HEAVY POLYTHERMALEZ WIRE.

T_1:



COILCRAFT FORM #10-32 OR EQUIV
UNIVERSAL AWG #36 WIRE OR EQUIV
L = 26 μH

T_2:



COILCRAFT FORM #10-32 OR EQUIV
UNIVERSAL AWG #36 WIRE OR EQUIV
L_P = 12 μH primary winding
L_S = 8.8 μH secondary winding
K = 0.4

This coil data is intended as an aid only. It is expected that many designers will want to use other approaches.

MC1398P APPLICATIONS INFORMATION

MC1398P is a multifunction circuit with considerable gain associated with the chroma amplifier and oscillator sections. It is important to the circuit layout utilizing the MC1398P that the chroma amplifier, oscillator, and oscillator output/hue section grounds are separated from each other. Ground loop problems will interfere with oscillation stability and lock-up if this precaution is not observed.

Care must be exercised to avoid coupling from the oscillator output to the crystal circuitry connected to pin 8. Stray coupling of these two points can result in excessive oscillator shift; or in some cases, oscillator drop-out during adjustment of the hue control.

A suitable circuit layout for the MC1398P is shown in Figure 10.

An adjustable capacitor (1.5–20 pF in parallel with a fixed 22 pF capacitor) is shown in series with the 3.58 MHz crystal. This capacitor is used to adjust the oscillator exactly on frequency, and ensures excellent oscillator lock-up. However, acceptable oscillator performance can be obtained with a fixed value of capacitance (this value is dependent on the designers' choice of crystals).

MC1398P CIRCUIT DESCRIPTION

The MC1398P is capable of providing the entire color processing function between the second detector and the demodulator for television color receivers.

A band pass filter from the second detector provides a 50 mV (p-p) signal (for a saturated color bar pattern) at the input to the first chroma amplifier stage (Q_2, Q_3, Q_8, Q_9). Because of Q_2 emitter load resistor the input impedance is determined primarily by the bias resistor (R_3) and is about 2.3 kilohms. Since Q_2 is the current source for the differential pair (Q_3 and Q_9), the chroma information will pass to the load resistor (R_7) and then to the second chroma amplifier (Q_{17}). To avoid overload of Q_{17}, the maximum gain to Q_{17} base is only X3 and by varying the bias at the base of Q_9 it is possible to reduce the stage gain by 23 dB without signal distortion; the signal being "dumped" by Q_9 collector into the supply. Since this automatic chroma control action will vary the dc bias at Q_{17} base the emitter load of Q_{17} is the current source Q_{18}, maintaining the dc operating current. Q_{18} collector is bypassed externally to prevent ac signal attenuation.

During picture scan time, the chroma signal passes through the output level control amplifier (Q_{10}, Q_{11}, Q_{15}, Q_{21}). By changing the bias on Q_{11} and Q_{15} bases the signal can either pass to the output pin 2 or be "dumped" into the supply through Q_{11}. The use of buffer stages Q_{10} and Q_{21} prevent distortion at low-signal levels and the control range is better than 70 dB. The signal output is also buffered by Q_{14} and Q_{20}, thus providing a low impedance drive of up to 2.0 V (p-p) to the demodulator, with an overall gain between pins 5 and 2 of 40 dB. To enable the chroma signal output to reach the amplifiers from Q_{17} collector, Q_{12} is held in conduction by Q_5 which in the absence of any input on pin 4 is not conducting. This high collector voltage also holds Q_{26} in conduction, clamping the input to the burst channel and preventing chroma information reaching the oscillator. During picture retrace time, a positive-going 4.0 µs pulse from the line sweep transformer will turn Q_5 "on" and Q_7 "off". When Q_5 collector goes low, Q_{12} will become "cut-off" preventing the burst signal at Q_{17} collector from reaching the output pin 2. At the same time, Q_{26} turns "off" opening the burst channel. The high collector voltage of Q_7 turns on Q_{16} and Q_{22}. Q_{16} passes the burst signal from Q_{17} collector to the subcarrier regenerator and Q_{22} "fills-in" for Q_{12} during the gate period to prevent a dc shift in the pin 2 output voltage.

The gated burst signal is applied to the oscillator through Q_{27} and Q_{28}. Q_{29}, Q_{50} and Q_{35} together with Q_{27} and Q_{28} form an injection locked oscillator circuit. At series resonance of the crystal connected to pin 8 the impedance of pin 8 is very low, thereby reducing the 3.579545 MHz carrier level at the base of Q_{50}. The signal at the base of Q_{29} is not reduced but the output voltages in R_{33} and R_{42} will change. Any signals outside the response band of the crystal will appear equally at Q_{50} and Q_{29} bases and be suppressed in the output by the differential amplifier common-mode rejection ratio (about 40 dB). To maintain oscillation, a feedback signal with the correct phase is passed by Q_{35} back to the input of Q_{27}. Careful control of the resistor ratios ensures that Q_{29} and Q_{50} are operated linearly with about 350 mV (p-p) at R_{33} and R_{42}, due to self oscillation. A burst signal as low as 2.0 mV (p-p) at the chroma input is sufficient to cause the oscillator to lock to the reference phase and frequency.

As the burst amplitude increases, the level at Q_{29} and Q_{50} collectors changes and this shift is used to provide the automatic chroma control function. Q_{42} and Q_{45} form a modified differential amplifier and with zero offset bias Q_{45} conducts most of the current from Q_{43}. As an increasing burst level swings Q_{29} and Q_{50} collectors, the current from Q_{43} is shunted into Q_{42}. At a point predetermined by the setting of the automatic chroma control connected to pin 10, the composite lateral PNP of Q_{47} and Q_{46} will be biased into conduction. This amplifier has a gain of unity and a filter capacitor (connected to Q_{46} base) prevents any tendency to oscillations. Diode CR_9 provides thermal compensation to ensure a steady color-killer threshold point. The increasing current through Q_{13} emitter is used to control Q_9 base, attenuating the input signal as the burst amplitude increases. The current from Q_{13} also keeps Q_{19} in saturation. When the input signal becomes too small for satisfactory color rendition, Q_{13} current falls and Q_{19} comes out of saturation. This means Q_{25} will saturate, clamping Q_{21} base and "killing" the chroma output stage. R_{24} in the Schmitt trigger circuit ensures that the color-killer will have hysteresis to prevent fluttering between "on" and "off" states.

The oscillator output voltages at R_{33} and R_{42} are used to drive Q_{38} and Q_{39} into limiting so that as the burst amplitude increases the oscillator activity to around 700 mV (p-p), there will be no change in the oscillator output amplitude at pin 13. Q_{38} and Q_{39} are used as current sources with a 180° phase difference for the differential pairs Q_{30} and Q_{31}, Q_{34} and Q_{37}. A small capacitor attached externally to Q_{39} collector adjusts the total phase difference to 135°. Since the signal appearing in the load resistor R_{51} will be the vector sum of Q_{31} and Q_{37} signals, varying the base bias of Q_{30} and Q_{34} will change the oscillator output phase over the 135° range. Q_{40} and Q_{41} buffer the oscillator output providing a low impedance drive at pin 13 for the demodulator.

To minimize crosstalk between the burst and chroma channels, separate bias chains are used. Further, the oscillator bias chain is zener regulated to prevent phase shifts in the reference output with power-supply variations.

MC1399

Advance Information

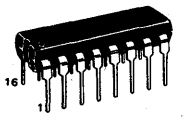
TV COLOR PROCESSING CIRCUIT

The MC1399 contains a chroma IF amplifier with automatic chroma control, color killer, linear dc chroma control, and a phase lock loop subcarrier regenerator system followed by a dc hue control.

- High Gain Automatic Chroma Control (ACC)
- High Gain Phase Lock Loop Subcarrier Regenerator System
- Color Killer with Externally Defined Threshold
- Critical Design Parameters Externally Adjustable
- Linear dc Chroma Control
- DC Hue Control with Well Defined Range and Center
- Internal Gating for Color Burst
- Built-In Supply Regulator
- Compatible with Most Existing Demodulators

TV COLOR PROCESSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

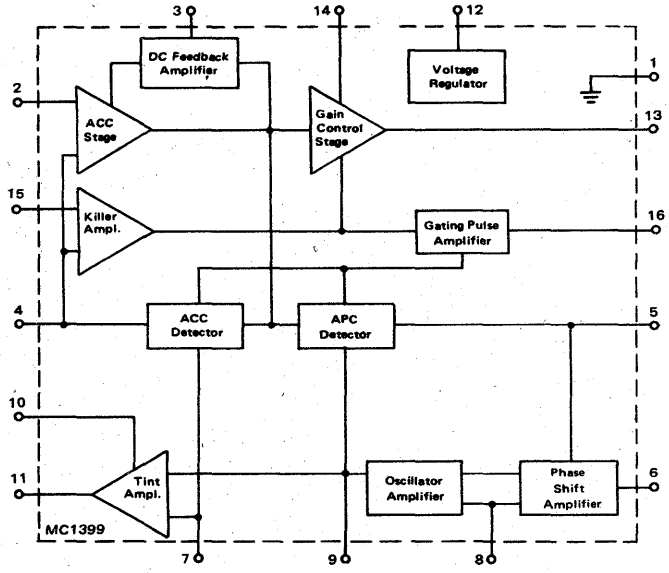


P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

Device	Temperature Range	Package
MC1399P	-20 to +75°C	Plastic DIP

FIGURE 1– MC1399 BLOCK DIAGRAM



This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Current	60	mA
Horizontal Pulse Input Current	4.2	mA
Minimum Load Resistance (Pins 11, 13)	2.7	kΩ
Junction Temperature	150	°C
Operating Ambient Temperature Range	-20 to +75	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS See Test Circuit, Figure 5. (All Switches in Position 1 Unless Otherwise Noted.)

Characteristic	Min	Typ	Max	Unit
Regulated Voltage (V_C) (Pin 12)	–	12.6	–	Vdc
Load Regulation (Pin 12) (V_{CC} from +22 V to +26 V)	–	100	–	mVdc
APC Set Up Voltage (R2)	0.61	–	0.81	$\%V_{CC}$
ACC Set Up Voltage (R1)	0.57	–	0.79	$\%V_{CC}$
Chroma Control Output Voltage				
(S1 Position 2)	–	1.25	–	Vp-p
(S1 Position 3)	–	625	–	mVp-p
(S1 Position 4)	–	12	–	mVp-p
Oscillator Output				
(S2 Position 2)	–	2.2	–	Vp-p
(S2 Position 1)	–	1.6	–	Vp-p
(S2 Position 3)	–	2.2	–	Vp-p
Oscillator Output Phase (Referred to Chroma Output Pin 13)				
(S2 Position 1)	–	231	–	Deg.
(S2 Position 2)	–	185	–	Deg.
(S2 Position 3)	–	268	–	Deg.
Static Phase Error (SPE) with Oscillator Detuned	–	0.02	–	Degrees/Hz
Automatic Chroma Control (ACC)				
Chroma Output for Input of:				
+6.0 dB (360 mVp-p Burst)	–	2.65	–	Vp-p
-14 dB (36 mVp-p Burst)	–	2.1	–	Vp-p
Chroma Output Voltage (Pin 13) for Input of -20 dB (Killer On) (18 mVp-p Burst @ Pin 2)	–	10	–	mVp-p

TYPICAL DESIGN CHARACTERISTICS (Figure 5)

Characteristic		Typ	Unit
Input Impedance	Pin 2	2.0 2.0	kΩ pF
	Pin 7	10 2.0	kΩ pF
	Pin 9	10 2.0	kΩ pF
Output Impedance Pins 6, 11, 13		50	Ω
Oscillator Drift with Temperature (Device Only)		0.7	PPM/°C
Oscillator Δf with V_{CC}		+20	Hz/Volt
Chroma Output Level Drift with Temperature (Device Only, 25 to 75°C)		10	%
Chroma Output Level Sensitivity to V_{CC} (Device Only)		2.0	%/Volt
Pull-In Range		±500	Hz
Noise Bandwidth (f_{nn})		150	Hz
Oscillator Control Sensitivity (β)		1.2	Hz/mV
APC Phase Detector Sensitivity (μ)		42	mV/Degree

FIGURE 2 – ACC CHARACTERISTICS

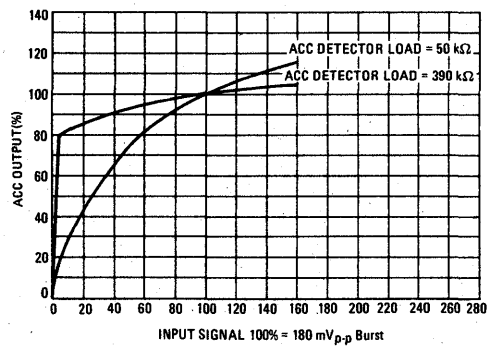


FIGURE 3 – GAIN CONTROL CHARACTERISTICS

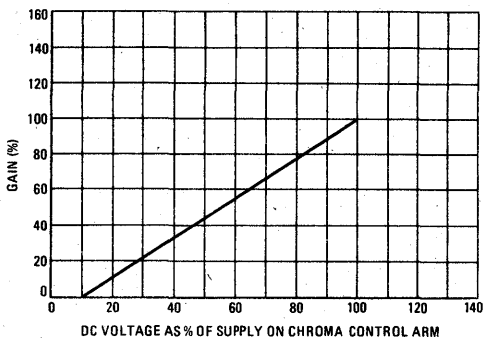


FIGURE 4 – TINT CONTROL CHARACTERISTICS

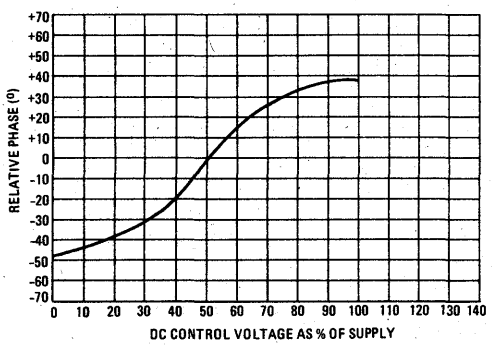


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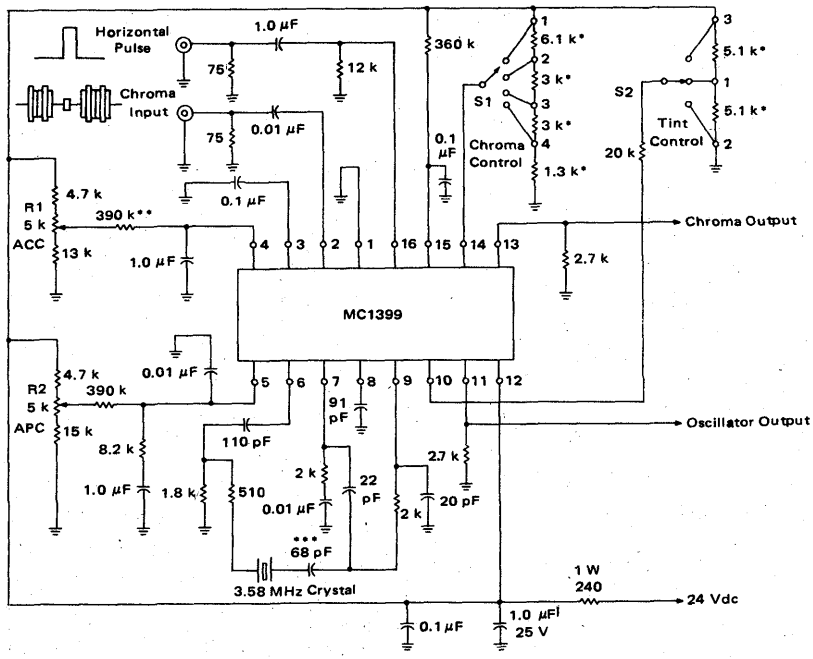
FIGURE 5 – DYNAMIC CHARACTERISTIC TEST CIRCUIT



Set-Up: Apply 6 μs, 15.734 kHz Horizontal Pulse 3 Vp-p, Centered on Burst.
Adjust APC Control for 3.579545 MHz with No Chroma Input.
Apply NTSC 75% Bar Chart, (Luminance, Sync and Set-up Removed)
and Adjust ACC Control for 2.5 Vp-p Red Bar at Chroma Output.

*1% Resistor Tolerance
**Determines ACC loop gain, see Figure 2.
***Value determined by crystal.

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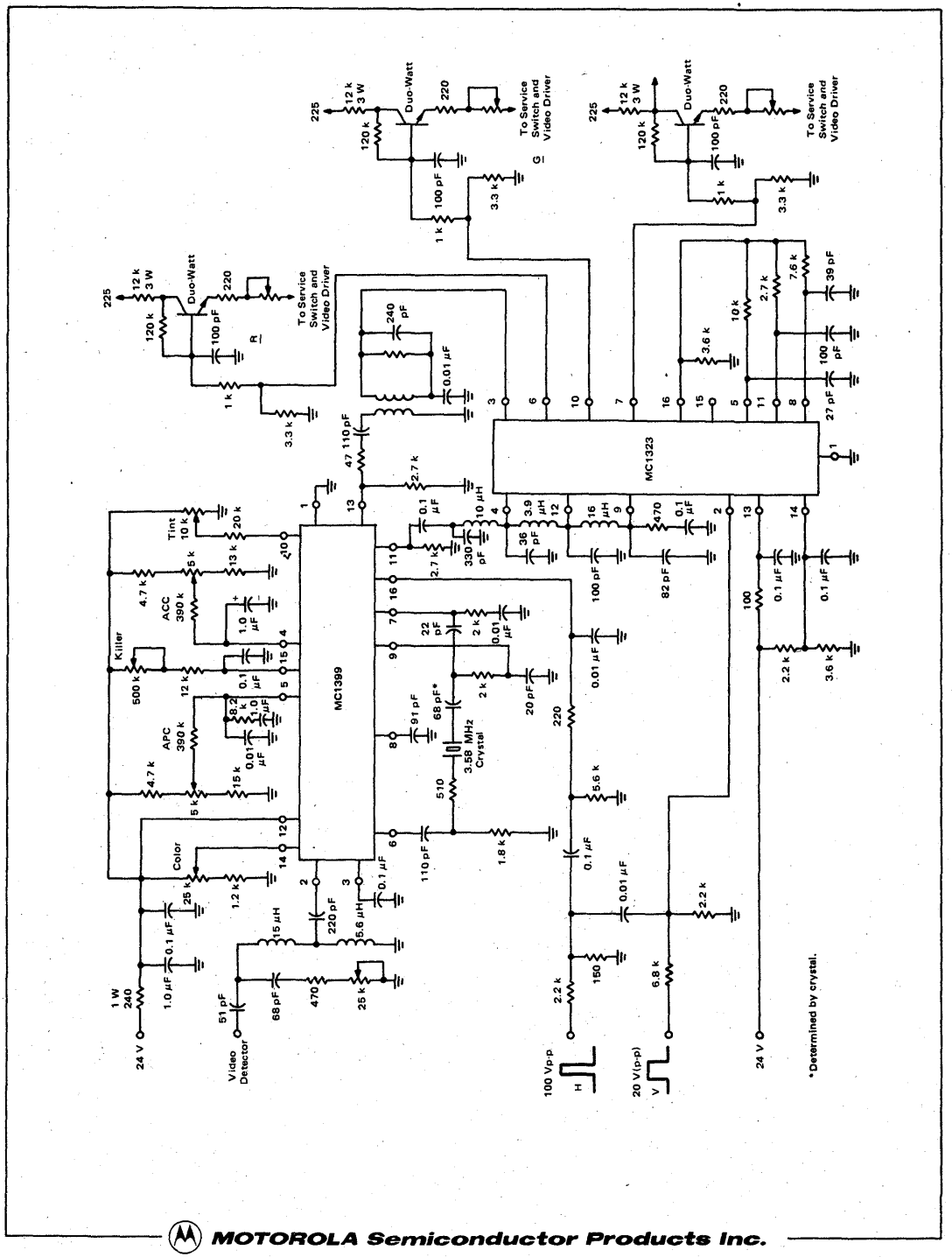

MC1399
MC1323
Duo-Watt
To Service Switch and Video Driver
Tint
ACC
APC
Killer
Color
3.58 MHz Crystal
Video Detector
24 V
100 Vp-p
20 V(p-p)
*Determined by crystal.

ORDERING INFORMATION

Device	Temperature Range	Package
MC3310P	0°C to +75°C	Plastic DIP

MC3310P

WIDE-BAND AMPLIFIER

. . . designed for FM/IF and low-level audio applications.

- High Audio Gain – 60 dB minimum
- Useful as a Microphone Amplifier and in Tape Recorders and Cassettes
- Excellent Performance as a 10.7 MHz FM/IF Amplifier
- High Transconductance (g_m) Ideally Suited to Low Impedance Ceramic Filters
- Formerly MFC4010A in Case 206A Package

WIDE-BAND AMPLIFIER

SILICON MONOLITHIC FUNCTIONAL CIRCUIT

CASE 626-03

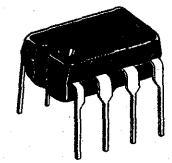


FIGURE 1 – FM/IF AMPLIFIER

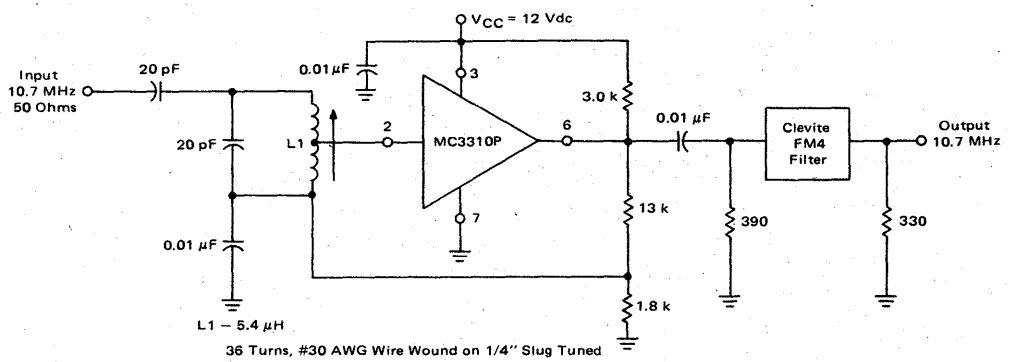
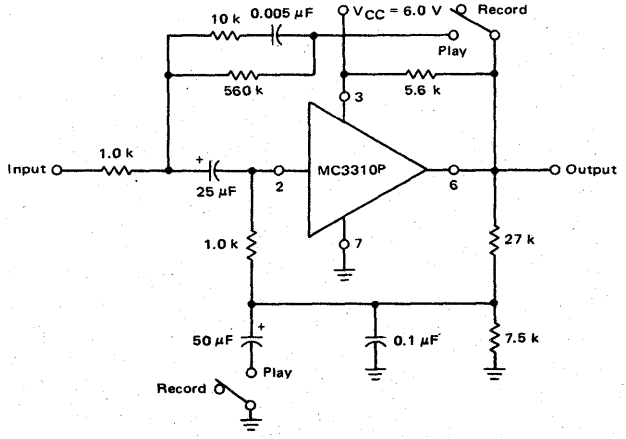


FIGURE 2 – RECORD/PLAY PREAMPLIFIER FOR CASSETTE AND PORTABLE TAPE RECORDERS



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MAXIMUM RATINGS (T_A = 25°C unless otherwise noted).

Rating	Value	Unit
Power Supply Voltage	21	Vdc
Power Dissipation @ T_A = 25°C (Package Limitation)	1.2	Watts
Derate above 25°C	10	mW/°C
Operating Ambient Temperature Range	0 to +75	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, T_A = 25°C unless otherwise noted).

Characteristic		Min	Typ	Max	Unit
Open Loop Voltage Gain (Figure 3) (f = 1.0 kHz)		60	68	–	dB
h Parameters(1) (f = 1.0 kHz)	h_{11}	–	1.0	–	k ohms
	h_{12}	–	10^{-6}	–	–
	h_{21}	–	1000	–	–
	h_{22}	–	10^{-5}	–	mhos
Output Noise Voltage (Figure 3) (BW = 20 Hz to 20 kHz, R_S = 1.0 k ohms)		–	3.0	–	mV(RMS)
		–	3.0	–	
Current Drain		–	3.0	–	mA

HIGH FREQUENCY CHARACTERISTICS (V_{CC} = 12 Vdc, f = 10.7 MHz, T_A = 25°C unless otherwise noted).

Power Gain (Figure 1) (e_{in} = 0.1 mVRMS)		–	42	–	dB
Noise Figure (Figure 1) ($R_S \approx$ 740 Ohms)		–	6.0	–	dB
y Parameters(1) (f = 10.7 MHz, I_2 = 2.0 mA)	y_{11}	–	1.3 + j1.5	–	mmhos
	y_{12}	–	-3.4 + j8.1	–	μmhos
	y_{21}	–	-0.33 + j0.68	–	mho
	y_{22}	–	120 + j0	–	μmhos

(1) Device only, without external passive components.

FIGURE 3 – AUDIO TEST CIRCUIT

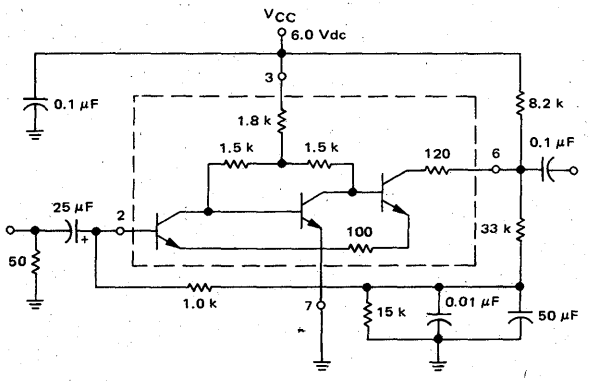
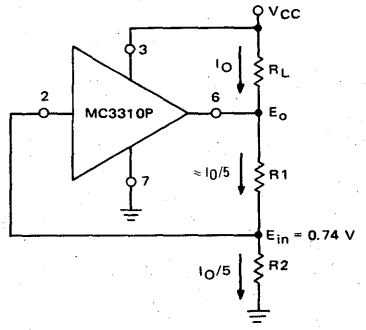


FIGURE 4 – BIASING RECOMMENDATIONS



Select: V_{CC}, E_o, and I_O
Solve for: $R_L = (V_{CC} - E_o)/I_O$
Let: $R2 = 5(0.74)/I_O$
Then: $R1 = R2\,(E_o - 0.74)/0.74$

TYPICAL CHARACTERISTICS

AUDIO PERFORMANCE CHARACTERISTICS (for Test Circuit Figure 3)

FIGURE 5 – VOLTAGE GAIN versus FREQUENCY

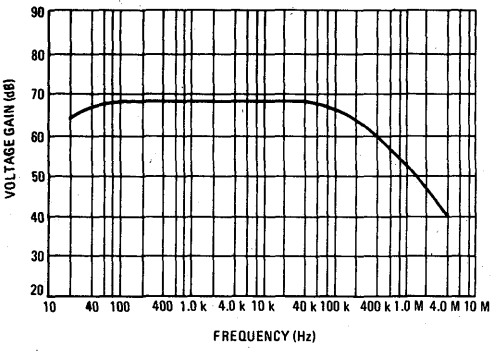
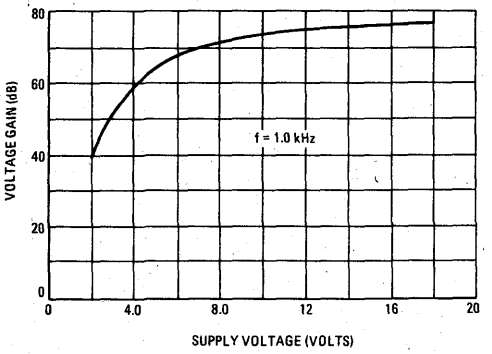


FIGURE 6 – VOLTAGE GAIN versus POWER SUPPLY



*TAPE PREAMPLIFIER PERFORMANCE (for Circuit Figure 2)

FIGURE 7 – RECORD VOLTAGE GAIN versus FREQUENCY

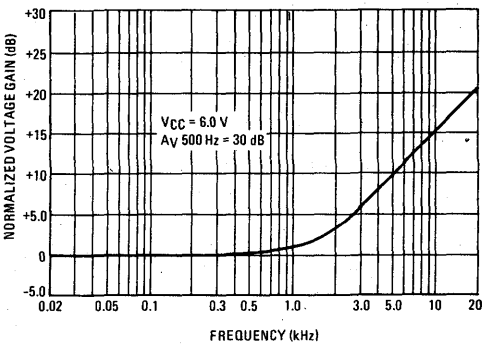
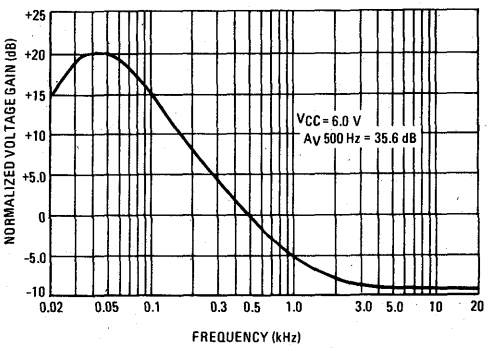


FIGURE 8 – PLAYBACK VOLTAGE GAIN versus FREQUENCY



Note:

The record/playback characteristics shown in Figures 8 and 9 were taken with the preamplifier driven by a 50 ohm source. The curves are typical of a desired response for the preamplifier; however, every type of tape recording and playback head is different and this circuit will not necessarily satisfy all requirements. No particular tape head was used as a basis for circuit design. The circuit is only an example showing the equalization network configuration.

The ideal preamplifier will have an input impedance approximately 10 times the highest impedance of the tape head and every preamplifier circuit must be designed using a test tape to verify the response of the design.

10.7 MHz y PARAMETERS

FIGURE 9 – INPUT ADMITTANCE

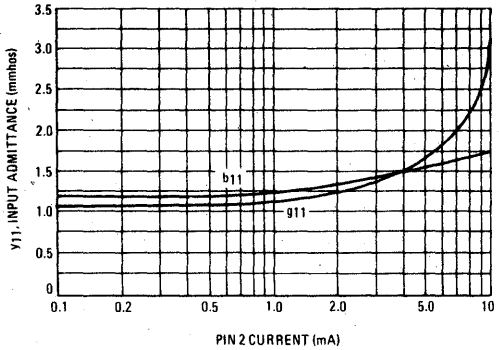


FIGURE 10 – REVERSE TRANSFER ADMITTANCE

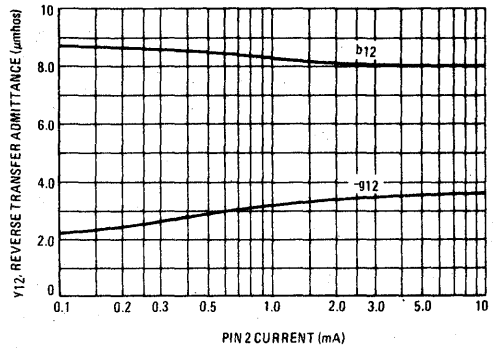


FIGURE 11 – FORWARD TRANSFER ADMITTANCE

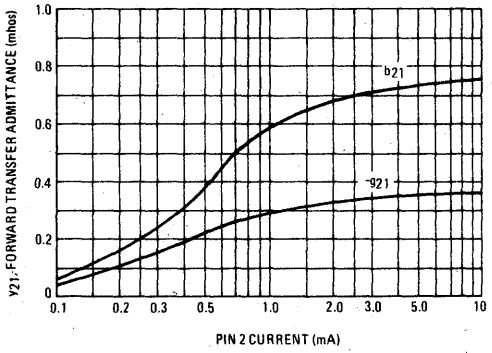
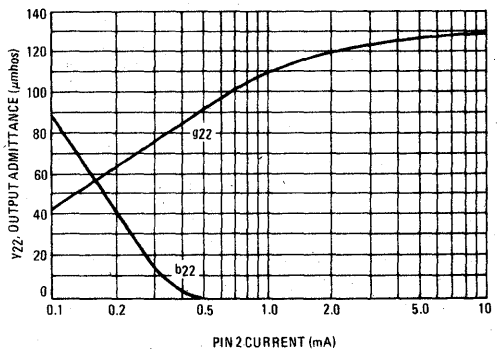


FIGURE 12 – OUTPUT ADMITTANCE



10.7 MHz PERFORMANCE
(Circuit of Figure 1)

FIGURE 13 – POWER GAIN versus SUPPLY VOLTAGE

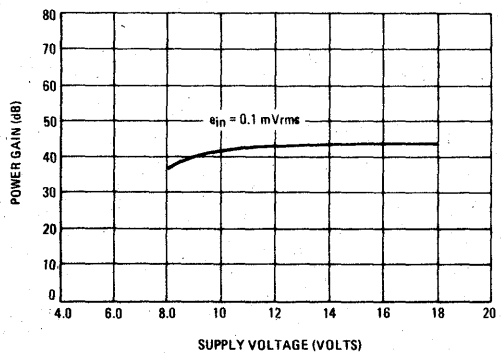
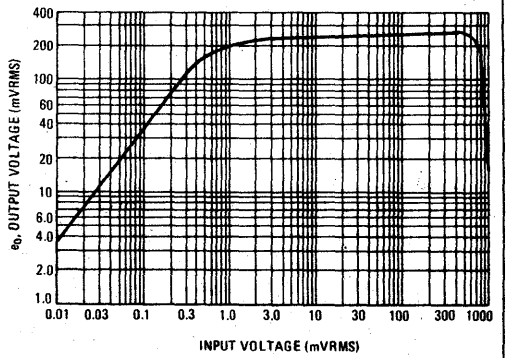


FIGURE 14 – VOLTAGE TRANSFER CHARACTERISTIC



ORDERING INFORMATION

Device	Temperature Range	Package
XC3315P	−40°C to +85°C	Plastic DIP

XC3315

Advance Information

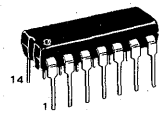
FREQUENCY-TO-VOLTAGE CONVERTER

This monolithic frequency-to-voltage converter uses a frequency doubling technique prior to integration in order to provide a low output ripple.

- Threshold and hysteresis of input comparator programmed with single external resistor
- Pulse-width programmed with external capacitor
- Output voltage proportional to supply voltage
- Zero frequency output voltage provided for use as reference

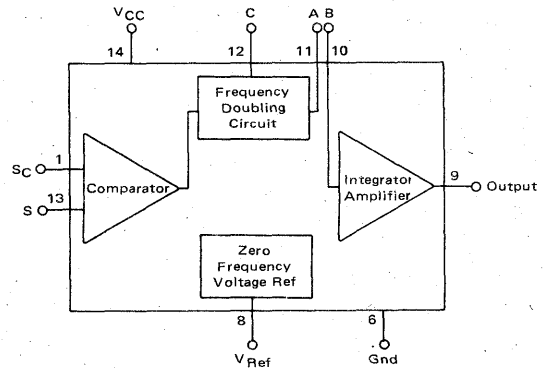
FREQUENCY-TO-VOLTAGE CONVERTER

MONOLITHIC SILICON INTEGRATED CIRCUIT

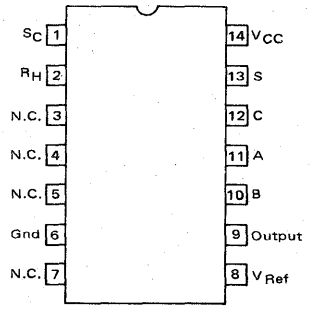


PLASTIC PACKAGE
CASE 646

BLOCK DIAGRAM



PIN CONNECTIONS



7

This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Voltage Range	V_{CC}	6.0 to 16	Vdc
Voltage at R_H Pin	V_{RH}	4.0	Vdc
Sensor Input Voltage	V_{IN}	24	Vdc
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 9.0 Vdc, V_{RH} = +1.0 Vdc, T_A = +25°C unless otherwise noted)

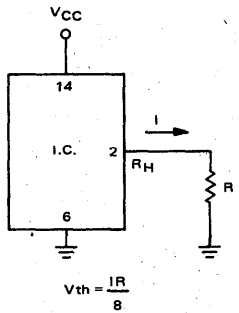
Characteristic	Symbol	Min	Typ	Max	Unit
Current Drain	I_D	–	–	16	mA
Amplifier (Norton Type)					
Open Loop Voltage Gain	A_{VOL}	–	66	–	dB
Input Bias Current	I_{IB}	–	–	200	nA
Output Current					
Source Capability	I_{source}	2.0	–	–	mA
Sink Capability	I_{sink}	0.3	–	–	mA
Output Voltage					
High Voltage	V_{OH}	V_{CC}-1.5	–	–	Vdc
Low Voltage	V_{OL}	–	–	0.4	Vdc
Unity Gain Bandwidth	BW	–	2.0	–	MHz
Phase Margin	θM	–	70	–	degree
Zero Frequency Reference Voltage					
Reference Voltage	V_{Ref}	500	600	700	mV
Current Sink Capability	I_{sink}	1.0	–	–	mA
Current Source Capability	I_{source}	1.0	–	–	mA
Reference Matching to Integrator Amplifier	$V_{Ref(offset)}$	–	10	–	mV

CIRCUIT INFORMATION

INPUT SPECIFICATIONS

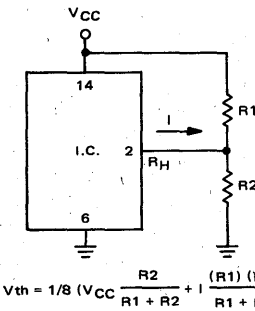
Threshold of Input Comparator

The trip point of the input comparator is programmed by adjusting the voltage at the terminal R_H. This threshold is symmetric about the zero signal level and can be determined with the design equation: Vth = $VR_H/8$. A 50 μA ± 30% current source is provided at terminal R_H such that the thresholds can be programmed with a single resistor to ground. If greater accuracy is desired, the voltage at terminal R_H can be forced with a resistor divider to a reference voltage such as a regulated supply. For proper circuit operation, the threshold should be greater than ±50 mV, but less than ±500 mV corresponding to programming voltages of 400 mV to 4.0 volts at terminal R_H. The options for programming the input threshold are illustrated below.



$$Vth = \frac{IR}{8}$$

I = 50 μA ± 30%



$$Vth = 1/8 \left(V_{CC} \frac{R2}{R1 + R2} + I \frac{(R1)(R2)}{R1 + R2}\right)$$

Maximum Input Amplitude at Pin 13

To avoid false failure indication during the peak swing of the sensor signal, the voltage at Pin 13 must remain at least one volt above ground and one volt below V_{CC}. This implies that the peak sensor amplitude be less than ½ V_{CC}-1 volts. To accomplish this the input filter, RS-CS, should be adjusted accordingly.

To avoid damage to the IC the voltage at the input Terminals S, and SC should not swing more than 16 volts above their ½ V_{CC} bias level. External resistors should guarantee that the clamp current sourced by the IC at S1 or S2 does not exceed 1.0 mA.

TIMING CIRCUIT SPECIFICATION

The voltage on the capacitor at terminals (Pin 12) are ramped upward and downward to produce pulses of current for integration at twice the input signal frequencies. The pulse widths can be adjusted by adjusting the capacitor using the relationship:

$$\text{Pulse width} \approx \frac{210\ \mu s}{0.003\ \mu F} = 70\ \text{ms}/\mu F$$

To avoid saturating the converter at high frequencies the pulse widths should be less than $\frac{1}{2f_{max}}$ where f_{max} equals the maximum input signal frequency.

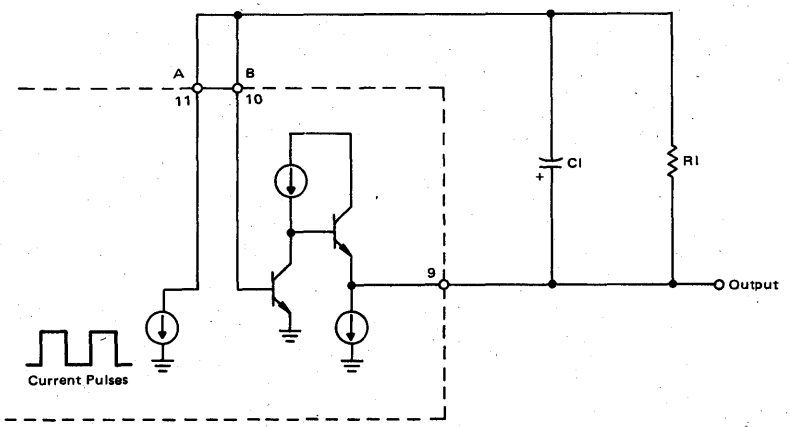
ONE POLE INTEGRATOR DESIGN

To obtain a single pole at the frequency Wo an external resistor and capacitor should be connected as shown in Figure 1.

After adjusting the gain of the converter with the resistor RI (RI ≅ 100 kΩ), the capacitor CI should be chosen such that:

$$Wo = \frac{1}{RI\ CI}$$

FIGURE 1 – ONE POLE INTEGRATOR



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TWO POLE INTEGRATOR DESIGN

To obtain two real and equal poles at the frequency Wo using the circuit shown in Figure 2 proceed as follows:

1. Set integrator gain with resistor R4 (R4 ≅ 100 kΩ).
2. Choose R3 and C2 from the equation:

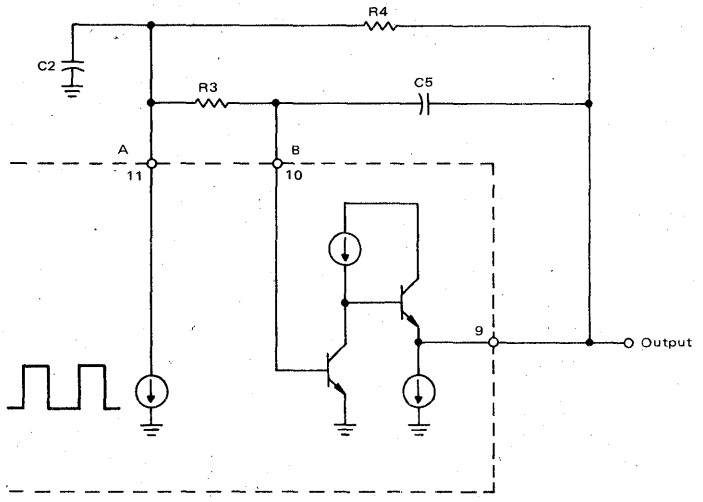
$$Wo = \frac{R3 + R4}{2\,(R3)\,(R4)\,(C2)}$$

Note: Let R3 ≤ 5.0 kΩ to avoid saturating the current source at terminal A.

3. For real and equal poles let:

$$C5 = \frac{4\,(R3)\,(R4)\,(C2)}{(R3 + R4)^2}$$

FIGURE 2 – TWO POLE INTEGRATOR



ACCURACY SPECIFICATIONS

The tachometer has been designed to provide accurate frequency trip points when used with the comparator circuit shown in Figure 3.

For this purpose the tach output must be described by the equation:

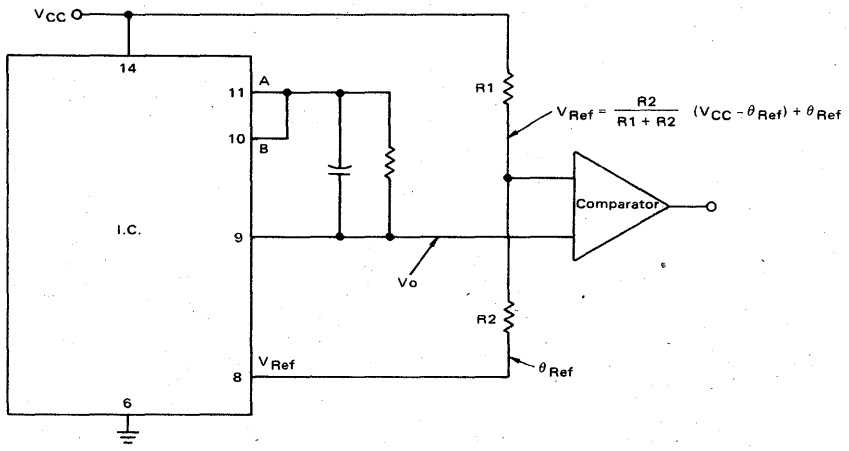
$$Vo = K\,(V_{CC} - \theta_{Ref})\,f + \theta_{Ref}$$

where K = converter gain constant
f = frequency of sensor signal

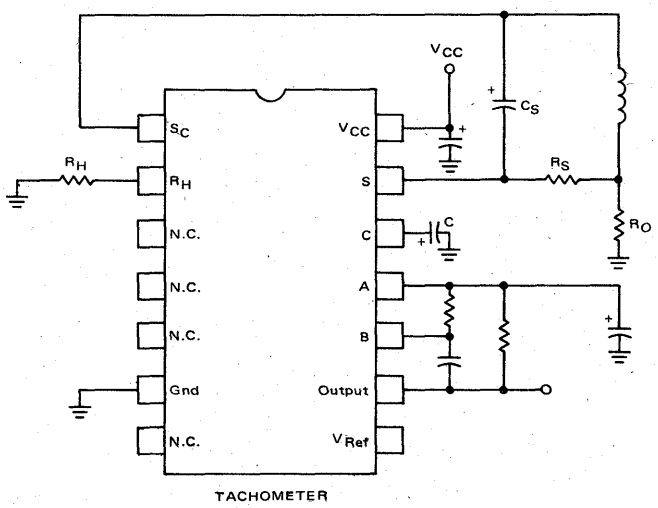
The accuracy and linearity of the converter can be determined by how well the tach characteristics fit this equation. Using measured values of Vo, V_{CC}, θ_{Ref}, and f the gain constant K can be calculated at various operating points. The converter accuracy can be expressed as the percent change in K due to supply voltage, temperature, and frequency variations. The following tolerances are typical.

Variation in gain with supply voltage (average for 6.0 V to 16 V operation)	+0.5%/Volt
Variation in gain with frequency (linearity from 50 Hz to 2.0 kHz)	±1%
Variation in gain with temperature (-40°C to +85°C)	±1%

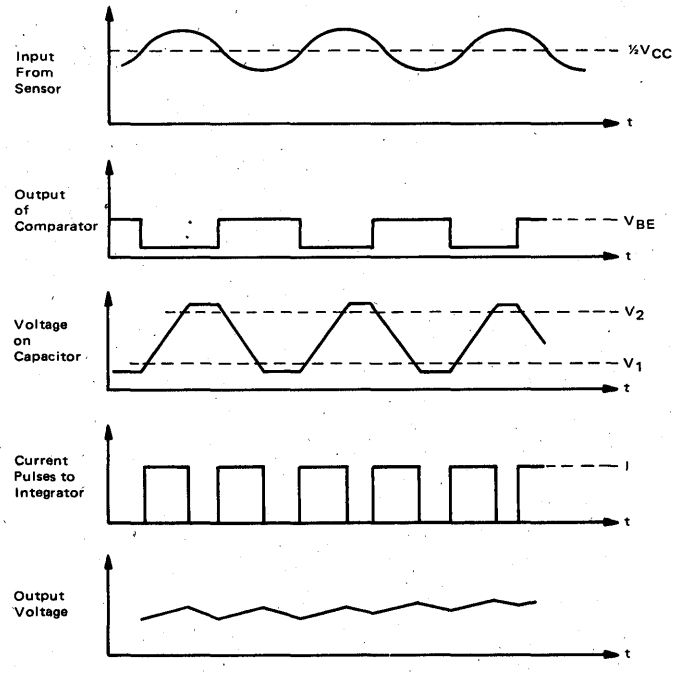
FIGURE 3 – COMPARATOR CIRCUIT FOR ACCURATE FREQUENCY TRIP POINTS



TYPICAL APPLICATION



TYPICAL CIRCUIT WAVEFORMS



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

7

ORDERING INFORMATION

Device	Temperature Range	Package
XC3316P	-40 to +85°C	Plastic DIP
XC3317P	-40 to +85°C	Plastic DIP

XC3316
XC3317

Advance Information

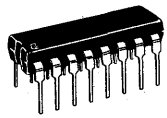
DUAL FREQUENCY-TO-VOLTAGE CONVERTER

This monolithic dual frequency-to-voltage converter uses a frequency doubling technique prior to integration in order to provide a low output ripple. High select, low select and fail indication outputs are available with the XC3317 only.

- Two independent channels
- Threshold and hysteresis of input comparators programmed for both channels with single external resistor
- Pulse-width programmed with external capacitor for each channel
- Output voltages proportional to supply voltages
- Zero frequency output voltage provided for use as reference
- Fail check indication for open sensor (XC3317 only)
- Hi and low select outputs with less than 100 mV offset from actual output voltage (XC3317 only)

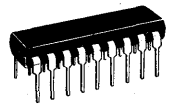
DUAL FREQUENCY-TO-VOLTAGE CONVERTER

MONOLITHIC SILICON INTEGRATED CIRCUIT

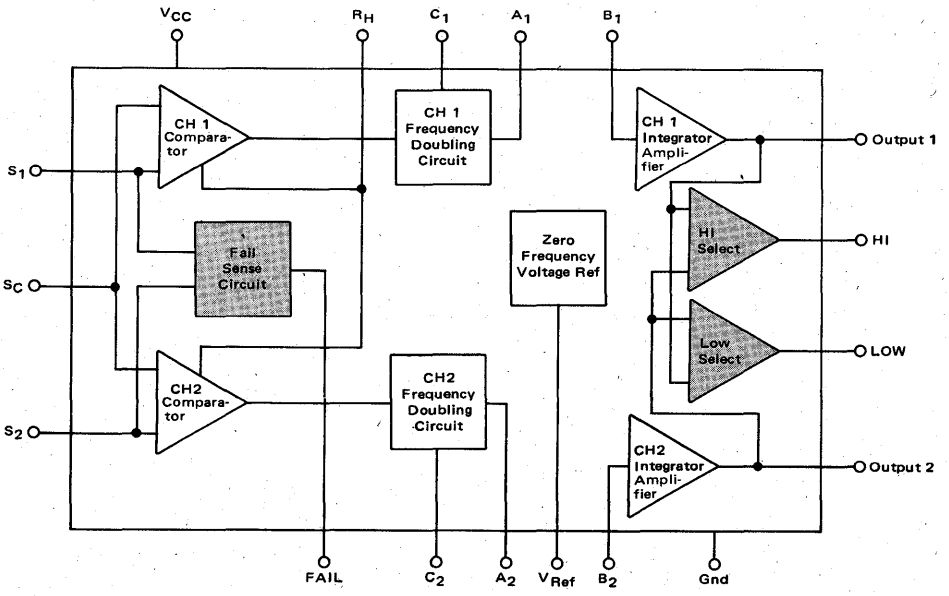


XC3316
P SUFFIX
PLASTIC PACKAGE
CASE 648

XC3317
P SUFFIX
PLASTIC PACKAGE
CASE 701



BLOCK DIAGRAM



Shaded Areas Are Included With The XC3317 Only

This is advance information and specifications are subject to change without notice.

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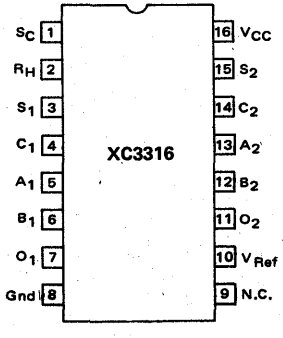
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

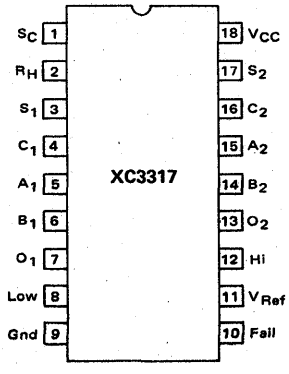
Rating	Symbol	Value	Unit
Operating Voltage Range	V_{CC}	6.0 to 16	Vdc
Voltage at R_H Pin	V_{RH}	4.0	Vdc
Sensor Input Voltage	V_{IN}	24	Vdc
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +9.0 Vdc, V_{RH} = +1.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Current Drain	I_D	–	–	16	mA
Amplifiers (Norton Type)					
Open Loop Voltage Gain	A_{VOL}	–	66	–	dB
Input Bias Current	I_{IB}	–	–	200	nA
Output Current					
Source Capability	I_{source}	2.0	–	–	mA
Sink Capability	I_{sink}	0.3	–	–	mA
Output Voltage					
High Voltage	V_{OH}	V_{CC}-1.5	–	–	Vdc
Low Voltage	V_{OL}	–	–	0.4	Vdc
Unity Gain Bandwidth	BW	–	2.0	–	MHz
Phase Margin	θM	–	70	–	degree
Output Terminal Specifications					
Hi Select Output					
Offset From High Channel Output	V_{IO}	–	–	100	mV
Current Source Capability	I_{source}	2.0	–	–	mA
Current Sinking Capability	I_{sink}	0.3	–	–	mA
Lo-Select Output					
Offset From Lower Channel Output	V_{IO}	–	–	100	mV
Current Source Capability	I_{source}	2.0	–	–	mA
Current Sink Capability	I_{sink}	0.3	–	–	mA
Failure Indication Output					
Failure Indication Resistance	R_{FAIL}	–	1.0	–	MΩ
Normal Resistance	R_{norm}	–	50	–	ohms
Current Sink Capability	I_{sink}	–	2.0	–	mA
Zero Frequency Reference Voltage					
Reference Voltage	V_{Ref}	500	600	700	mV
Current Sink Capability	I_{sink}	1.0	–	–	mA
Current Source Capability	I_{source}	1.0	–	–	mA
Reference Matching to Integrator Amplifiers	$V_{Ref(offset)}$	–	10	–	mV

PIN CONNECTIONS



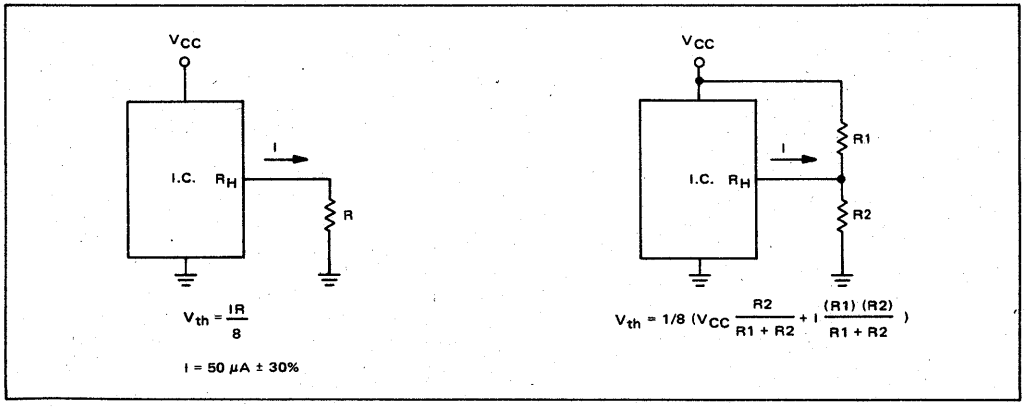


CIRCUIT INFORMATION

INPUT SPECIFICATIONS

Thresholds of Input Comparators

The trip points of the input comparators are programmed for both channels by adjusting the voltage at the terminal R_H. These thresholds are symmetric about the zero signal level and can be determined with the design equation: $V_{th} = V_{RH}/8$. A 50 μA ± 30% current source is provided at terminal RH such that the thresholds can be programmed with a single resistor to ground. If greater accuracy is desired, the voltage at terminal R_H can be forced with a resistor divider to a reference voltage such as a regulated supply. For proper circuit operation, the thresholds should be greater than ± 50 mV, but less than ± 500 mV corresponding to programming voltages of 400 mV to 4.0 volts at terminal RH. The options for programming the input thresholds are illustrated below:



Maximum Input Amplitude at S1 and S2

To avoid false failure indication during the peak swing of the sensor signal, the voltage at terminals S1 and S2 must remain at least one volt above ground and one volt below V_{CC}. This implies that the peak sensor amplitude be less than ½ V_{CC}-1.0 volts. To accomplish this the input filters, RS1-CS1 and RS2-CS2, should be adjusted accordingly.

To avoid damage to the IC the voltage at the input terminals S1, S2, and SC should not swing more than 16 volts above their ½ V_{CC} bias level. The fail check circuit will not allow S1 or S2 to go below ground, but external resistors should guarantee that the clamp current sourced by the IC at S1 or S2 does not exceed 1.0 mA.

SENSOR FAILURE CHECK SPECIFICATIONS

Open Sensor Check

Resistors R01 and R02 pull S1 and S2 respectively to ground if a sensor opens. This trips a fail check comparator on the IC and drives the FAIL terminal output to its high state (high impedance). Let R01, R01 $\leq$ 200 kΩ.

TIMING CIRCUIT SPECIFICATION

The voltages on the capacitors at terminals C1 and C2 are ramped upward and downward to produce pulses of current for integration at twice the input signal frequencies. The pulse widths can be adjusted by adjusting the capacitors using the relationship:

$$\text{Pulse width} \cong \frac{210\,\mu s}{0.003\,\mu F} = 70\ \text{ms}/\mu F$$

To avoid saturating the tach at high frequencies the pulse widths should be less than $\frac{1}{2\,f_{max}}$ where f_{max} equals the maximum input signal frequency.

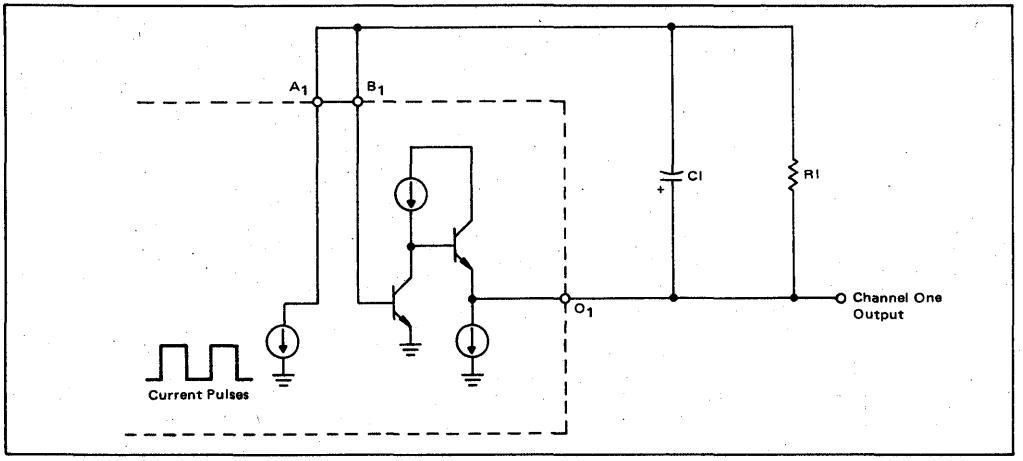
7

ONE POLE INTEGRATOR DESIGN

To obtain a single pole at the frequency Wo, an external resistor and capacitor should be connected as shown below.

After adjusting the gain of the tach with the resistor R_I ($R_I \cong 100\ k\Omega$), the capacitor C_I should be chosen such that:

$$Wo = \frac{1}{R_I C_I}$$



TWO POLE INTEGRATOR DESIGN

To obtain two real and equal poles at the frequency Wo using the circuit shown below proceed as follows:

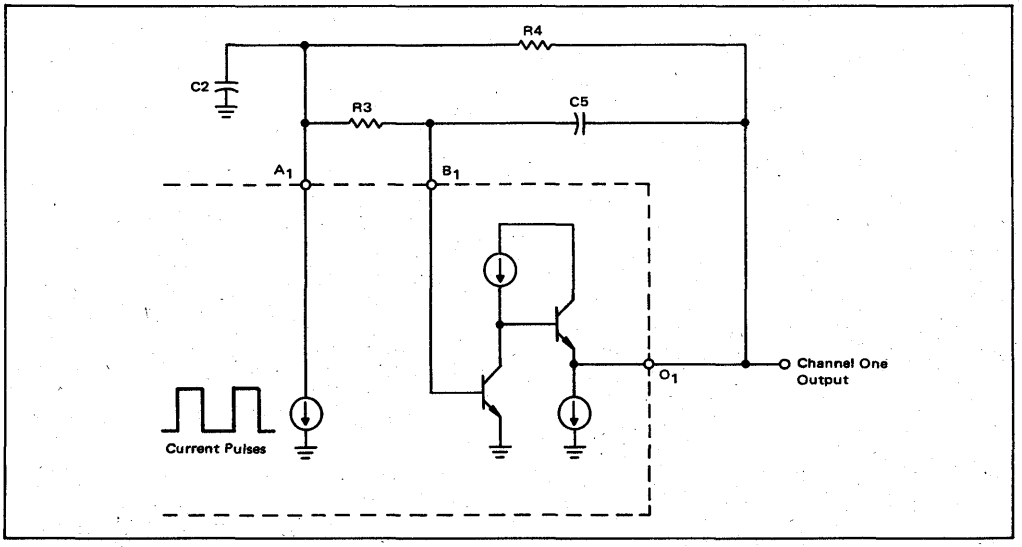
1. Set integrator gain with resistor R4 ($R4 \cong 100\ k\Omega$).
2. Choose R3 and C2 from the equation:

$$Wo = \frac{R3 + R4}{2(R3)(R4)(C2)}$$

Note: Let $R3 \leqslant 5.0\ k\Omega$ to avoid saturating the current source at terminal A.

3. For real and equal poles let:

$$C5 = \frac{4(R3)(R4)(C2)}{(R3 + R4)^2}$$



7

ACCURACY SPECIFICATIONS

The tachometer has been designed to provide accurate frequency trip points when used with the comparator circuit shown below.
For this purpose the tach output must be described by the equation:

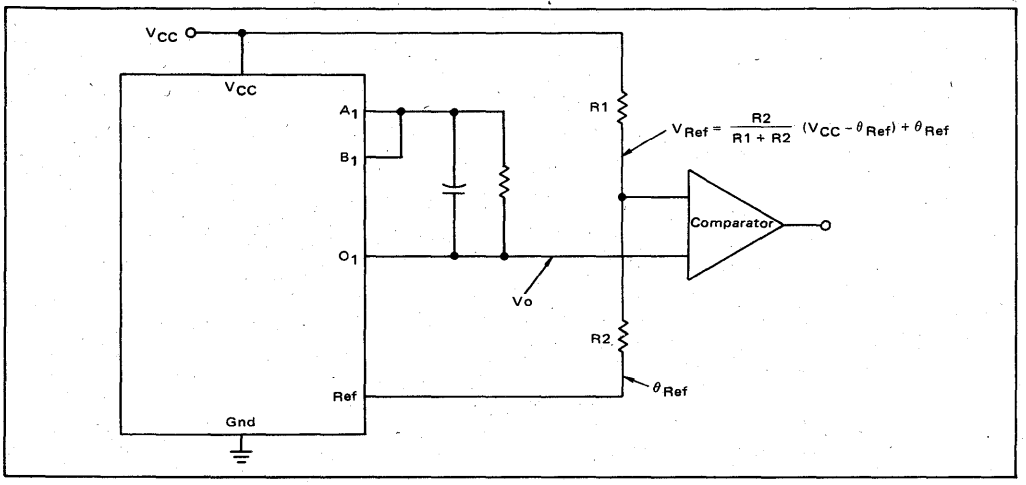
$$Vo = K\,(V_{CC} - \theta_{Ref})\,f + \theta_{Ref}$$

where K = tachometer gain constant
f = frequency of sensor signal

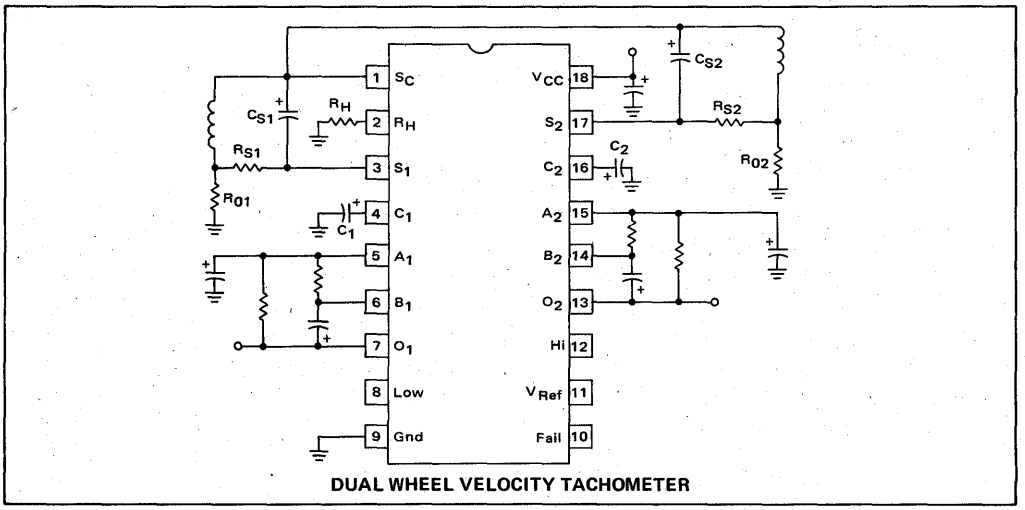
The accuracy and linearity of the tach can be determined by how well the tach characteristics fit this equation. Using measured values of Vo, V_{CC}, θ_{Ref}, and f the gain constant K can be calculated at various operating points. The tachometer accuracy can be expressed as the percent change in K due to supply voltage, temperature, and frequency variations. The following tolerances are typical.

Variation in gain with supply voltage (average for 6.0 V to 16 V operation)	+0.5%/Volt
Variation in gain with frequency (linearity from 50 Hz to 2.0 kHz)	±1%
Variation in gain with temperature (-40°C to +85°C)	±1%

COMPARATOR CIRCUIT FOR ACCURATE FREQUENCY TRIP POINTS

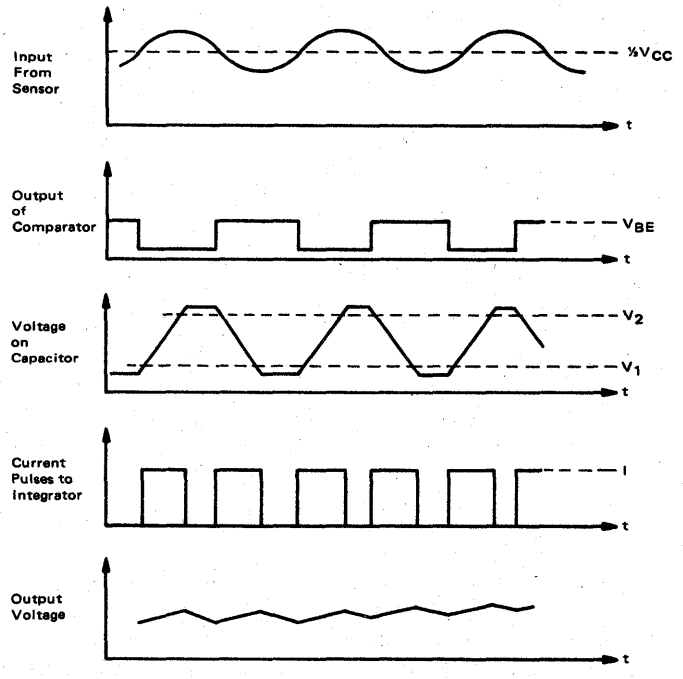


TYPICAL APPLICATION



DUAL WHEEL VELOCITY TACHOMETER

TYPICAL CIRCUIT WAVEFORMS



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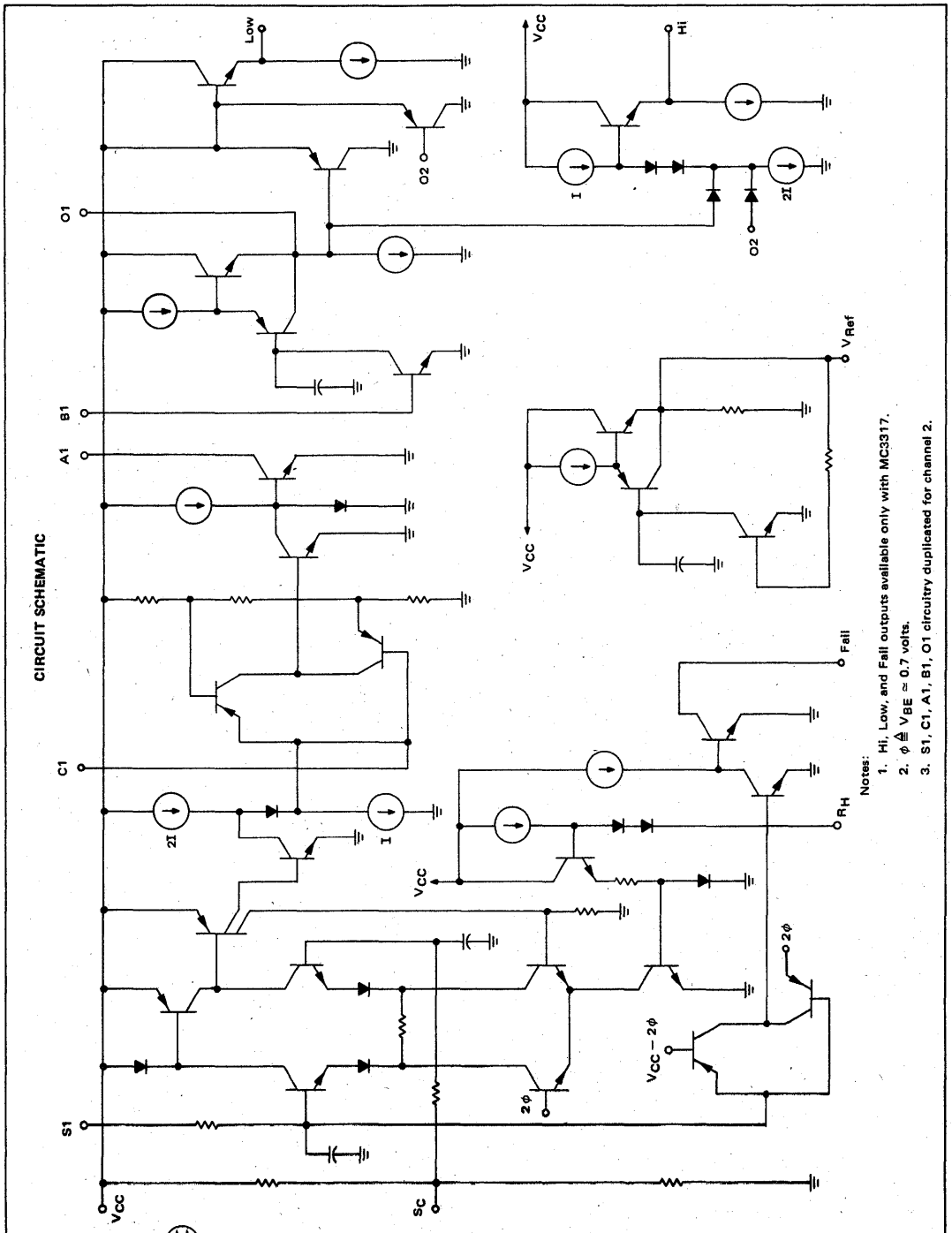

CIRCUIT SCHEMATIC
Low
Hi
O1
O2
B1
A1
C1
S1
VCC
SC
VRef
Fail
RH
2I
I
2ϕ
VCC – 2ϕ
Notes:
1. Hi, Low, and Fail outputs available only with MC3317.
2. ϕ ≙ VBE ≃ 0.7 volts.
3. S1, C1, A1, B1, O1 circuitry duplicated for channel 2.

ORDERING INFORMATION

Device	Temperature Range	Package
MC3320P	−10°C to +75°C	Plastic DIP
MC3321P	−10°C to +75°C	Plastic DIP

MC3320P
MC3321P

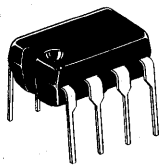
CLASS B AUDIO DRIVERS

. . . designed as preamplifiers and driver circuits for complementary output transistors.

- Driver for Auto Radios — and up to 10-Watt Amplifiers
- High Gain — 7.0 mV for 1.0 Watt, R_L = 3.2 Ohms
- High Input Impedance — 500-Kilohm Capability
- Output Biasing Diodes Included
- No Special h_{FE} Matching of Outputs Required
- Formerly MFC8020A and MFC8021A in Case 644A Package

CLASS B AUDIO DRIVERS

SILICON MONOLITHIC FUNCTIONAL CIRCUITS



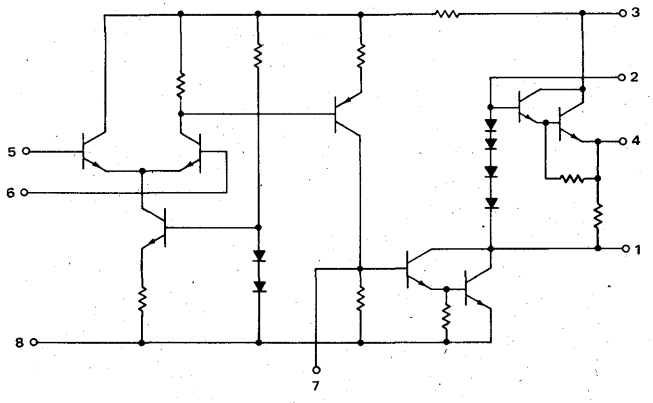
PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	MC3320P	MC3321P	Unit
Power Supply Voltage	V_{CC}	35	20	Vdc
Peak Output Current (Pins 4 and 1)	I_P	150		mA
Operating Ambient Temperature Range	T_A	-10 to +75		°C
Storage Temperature Range	T_{stg}	-55 to +125		°C
Junction Temperature	T_J	150		°C

7

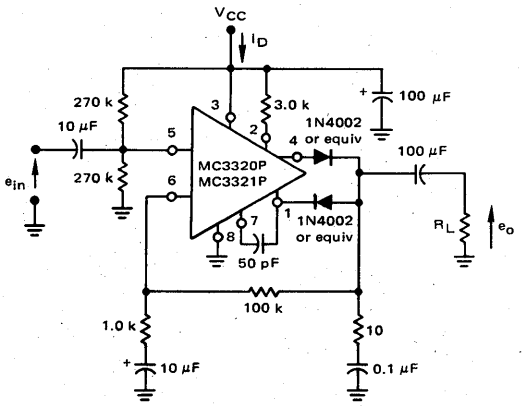
FIGURE 1 — CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted) (See Figure 2)

Characteristic		Min	Typ	Max	Unit
Drain Current (e_{in} = 0)					mA
(V_{CC} = 30 Vdc)	MC3320P	–	10	30	
(V_{CC} = 14 Vdc)	MC3321P	–	7.0	30	
Sensitivity (P_O = 1.0 Watt, f = 1.0 kHz)					mV
(e_o = 8.95 V(RMS), R_L = 165 Ω)	MC3320P	–	89	112	
(e_o = 3.2 V(RMS), R_L = 65 Ω)	MC3321P	–	32	40	
Total Harmonic Distortion (f = 1.0 kHz)					%
(V_{CC} = 30 V, e_o = 8.95 V(RMS), R_L = 165 Ω)	MC3320P	–	0.7	5.0	
(V_{CC} = 14 V, e_o = 3.2 V(RMS), R_L = 65 Ω)	MC3321P	–	1.0	5.0	
Open-Loop Gain					dB
(V_{CC} = 30 V, R_L = 165 Ω)	MC3320P	–	89	–	
(V_{CC} = 14 V, R_L = 65 Ω)	MC3321P	–	87	–	
Ripple Rejection (f = 60 Hz, A_V = 100, e_{in} = 0, Power Supply Ripple = 1.0 V(RMS)		–	27	–	dB
Equivalent Input Noise (e_{in} = 0, R_S = 1.0 kΩ, BW = 100 Hz – 10 Hz)		–	18	–	μV
Quiescent Output Voltage (e_{in} = 0)					Vdc
(V_{CC} = 30 V)	MC3320P	–	15	–	
(V_{CC} = 14 V)	MC3321P	–	7.0	–	

FIGURE 2 – TEST CIRCUIT



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

TYPICAL AUTO RADIO AUDIO APPLICATIONS and CHARACTERISTICS

(T_A = +25° unless otherwise noted.)

FIGURE 3 – APPLICATION CIRCUIT FOR MC3321P*

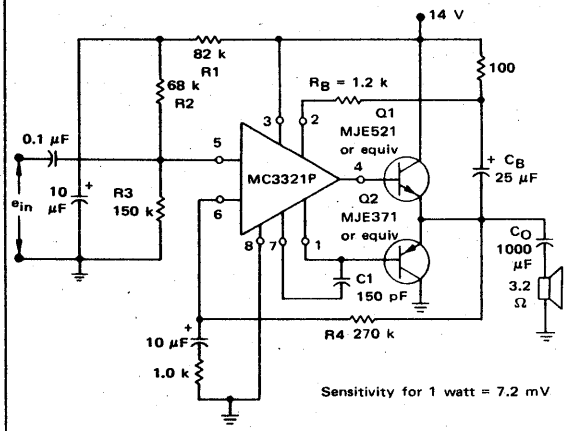


FIGURE 4–TOTAL HARMONIC DISTORTION versus OUTPUT POWER

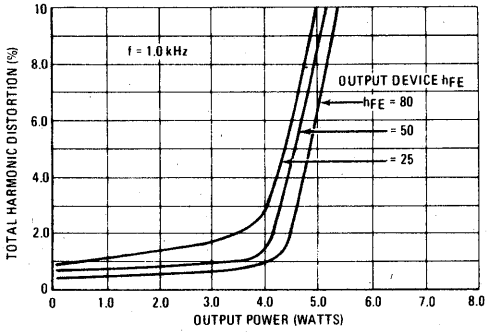


FIGURE 5 – TOTAL HARMONIC DISTORTION versus FREQUENCY

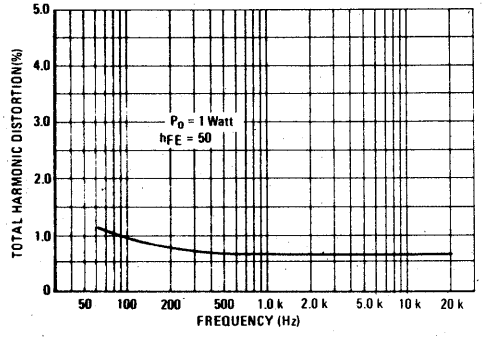
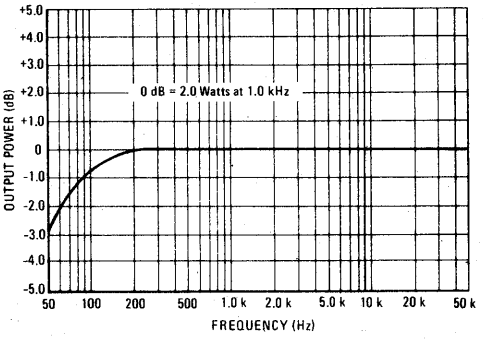


FIGURE 6 – FREQUENCY RESPONSE



APPLICATIONS INFORMATION for MC3321P (AUTO RADIO AUDIO)

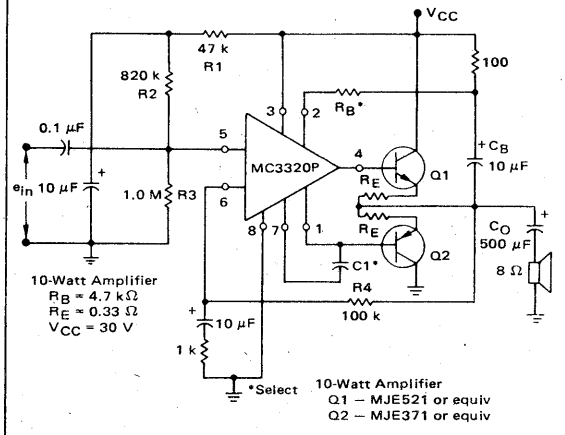
The MC3321P combines all the voltage gain required for an automotive radio audio amplifier into one package reducing the circuit-board area requirement. The circuit shown in Figure 3 has an input sensitivity of approximately 7.2 millivolts for a one-watt output. Sensitivity can be adjusted by changing the value of R_4. The circuit performance is a function of the output device h_{FE}, as shown in Figure 4. Figure 4 can be used to determine the minimum h_{FE} of the output transistors. The bandwidth of the amplifier is determined by the capacitor, C_1. If C_1 is increased to 390 pF the high frequency 3.0 dB point is typically 20 kHz.

* Differences may be found in idle current when matching this device to various output transistor types. It is suggested that a 10k potentiometer be placed between Pins 1 and 4 in series with a 100 Ohm resistor. This will allow for a reduction in quiescent current. Care should be taken not to allow the idle current to fall below 1 mA to avoid crossover distortion.

TYPICAL 10-WATT AMPLIFIER APPLICATION AND CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 7 – APPLICATION CIRCUIT*



(Select C1 to provide desired bandwidth.
C1 = 47 pF minimum)

FIGURE 8 – TOTAL HARMONIC DISTORTION versus OUTPUT POWER

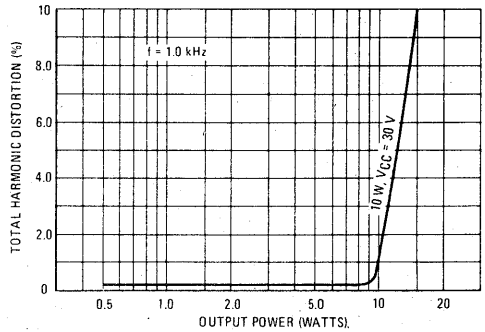


FIGURE 9 – TOTAL HARMONIC DISTORTION versus FREQUENCY

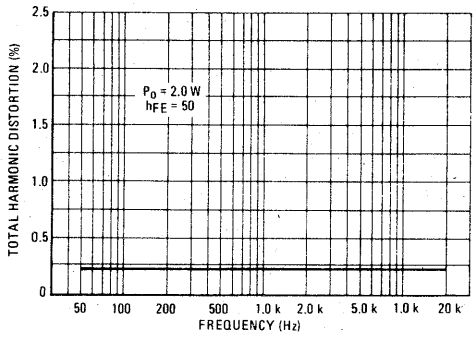
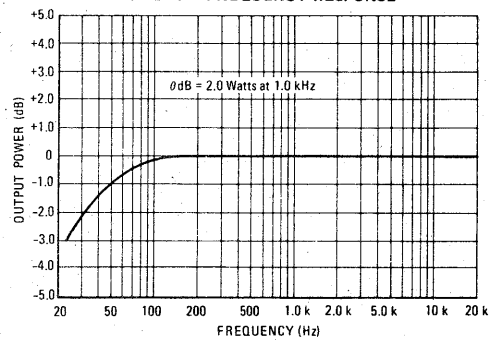


FIGURE 10 – FREQUENCY RESPONSE



APPLICATIONS INFORMATION for MC3320P
(10 Watt Amplifiers)

The MC3320P is a high-voltage device capable of driving 10 Watt audio amplifiers. The gain of the circuit shown in Figure 7 changes when the value of R4 is varied and the bandwidth is determined by C1. Emitter resistors are required at the higher voltages used for 10 Watt audio amplifiers to provide thermal stability. The value of R_E is a function of the heatsink thermal resistance and supply voltage. The heatsink requirements for operation at +65°C (with both devices mounted on the same heatsink) is about 14°C/W for the 10-Watt amplifier. If the maximum ambient operating temperature is reduced then the heatsink can be reduced in size as calculated by

$$\theta SA = \frac{T_J - (\theta JS)\, P_D - T_A}{P_D}$$

where

θSA = Heatsink thermal resistance

T_J = Maximum junction operating temperature

θJS = Junction to heatsink thermal resistance (includes all surface interface components for thermal resistance such as the insulating washer)

P_D = Maximum power dissipation of transistors (This occurs at about 60% of maximum output power) 6.0 W for 10 W, 7.2 W for 12 W

T_A = Maximum ambient temperature

* Differences may be found in idle current when matching this device to various output transistor types. It is suggested that a 10k potentiometer be placed between Pins 1 and 4 in series with a 100 Ohm resistor. This will allow for a reduction in quiescent current. Care should be taken not to allow the idle current to fall below 1 mA to avoid crossover distortion.

7

MC3325

Advance Information

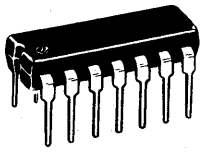
AUTOMOTIVE VOLTAGE REGULATOR

. . . designed for use in conjunction with an NPN Darlington transistor in a floating field alternator charging system.

- Overvoltage Protection
- Shut-Down on Loss of Battery Sense
- Selectable Temperature Coefficient
- Available in Chip Form for Hybrid Assembly

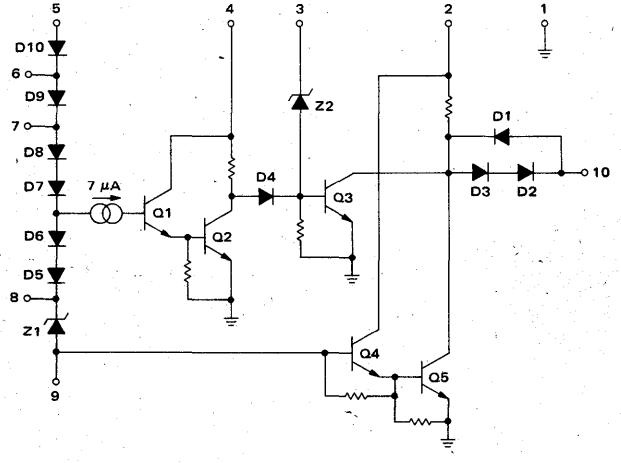
AUTOMOTIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

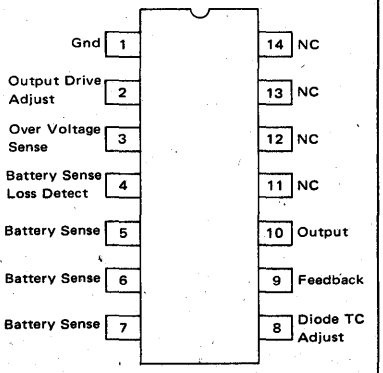


P SUFFIX
PLASTIC PACKAGE
CASE 646
TO-116

CIRCUIT SCHEMATIC



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC3325P	-40 to +85°C	Plastic DIP

7

This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Current Into Pins 5, 6, and 7	$I_{5,6,or\ 7}$	50	mA
Current Into Pin 3	I_3	20	mA
Current Into Pin 4	I_4	20	mA
Current Into Pin 2	I_2	120	mA
Current Into Pin 8	I_8	50	mA
Current Into Pin 9	I_9	50	mA
Current Into Pin 10	I_{10}	50	mA
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
Diode TC Adjust: Threshold Voltage on Pin 8 (Figure 1)	V_8	7.9	–	8.8	V
Battery Sense: Threshold Voltage on Pin 5 (Figure 1)	V_5	11.8	–	13.3	V
Battery Sense: Threshold Voltage on Pin 6 (Figure 1)	V_6	11.1	–	12.6	V
Battery Sense: Threshold Voltage on Pin 7 (Figure 1)	V_7	10.5	–	11.8	V
Battery Sense Loss Detect: Threshold Current Into Pin 4 (Figure 2)	I_4	–	–	400	μA
Battery Sense Loss Detect: Threshold Voltage at Pin 4 ($I_4 \leq 400$ μA, Figure 2)	V_4	1.3	–	1.7	V
Overvoltage Sense: Threshold Current Into Pin 3 (Figure 2)	I_3	–	–	400	μA
Overvoltage Sense: Threshold Voltage at Pin 3 ($I_3 \leq 400$ μA, Figure 2)	V_3	6.7	–	9.0	V
Output Drive Adjust: Voltage Drop from Pin 2 to Pin 10 (I_2 = 10 mA, Figure 3)	V_2	1.9	–	2.4	V
Low State Output Voltage at Pin 10 (I_3 = 12 mA, I_2 = 120 mA, Figure 4)	V_{10}	–	–	0.7	V

7

TEST CIRCUITS

FIGURE 1

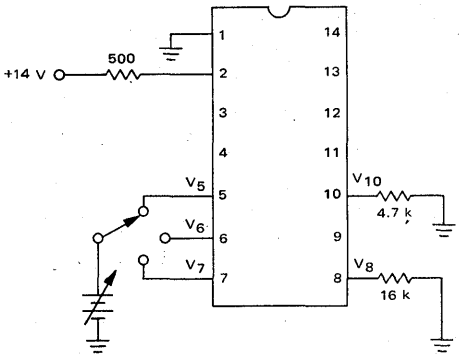


FIGURE 2

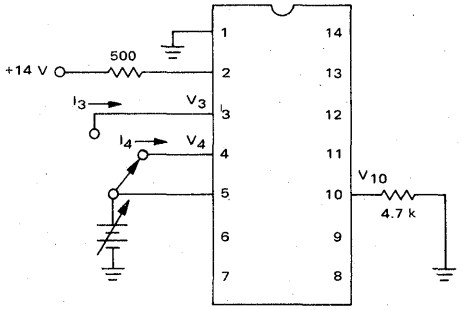


FIGURE 3

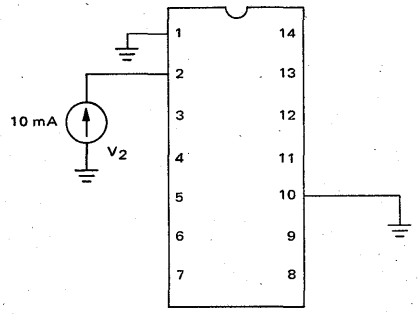
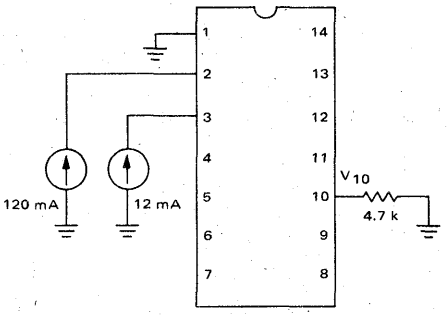
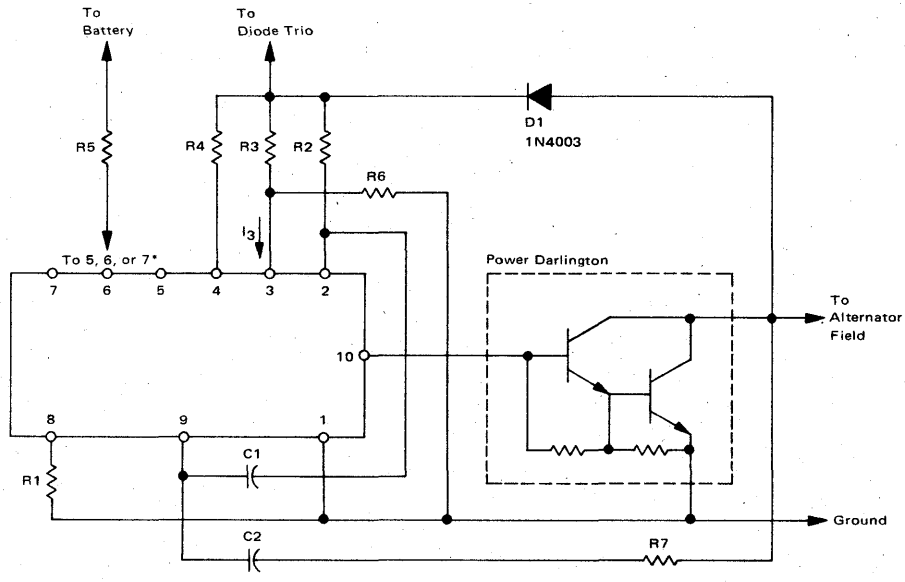


FIGURE 4



7

FIGURE 5 – APPLICATION CIRCUIT



*Note: The temperature coefficient of the battery voltage sense terminal is determined by the number of diodes used in the diode string (i.e., whether Pin 5, 6, or 7 is used). The approximate temperature coefficient for a diode at 1.0 mA is -2.0 mV/°C, and for a zener diode it is +3.0 mV/°C. Counting from ground (see circuit schematic) we have -2.0 mV for Q5, -2.0 mV for Q4, +3.0 mV for Z1, -8.0 mV for D5 thru D8, and an additional -2.0 mV each for D9 and D10 if used. The total temperature coefficient can be varied from approximately -9.0 mV/°C to -13 mV/°C depending on the number of the diodes in the diode string that are utilized.

APPLICATIONS CIRCUIT INFORMATION

(See Figure 5)

R1 Determines the temperature coefficient by setting the value of current in the diode string. As the value of R1 decreases, so does the effective TC. R1 should be chosen so that the current in the diode string is between 0.5 mA and 1.0 mA.

R5 This resistor determines the V_{reg} voltage as defined by the following equation:

$$V_{reg} = \left(1 + \frac{R5}{R1}\right) 8.4 + \left(n + \frac{R5}{5k}\right) (0.7)$$

n = number of diodes used in diode string
$(4 \leqslant n \leqslant 6)$

R4 Used as a current limiting resistor on Pin 4 in case of an open battery voltage sense lead.

R3 Used as a current limiting resistor on Pin 3 in case of overvoltage at the diode trio. Voltage at Pin 3 will run approximately 7.5 volts. R3 should be chosen so that the current (I_3) at maximum overvoltage is between 2.0 mA and 6.0 mA.

R2 This resistor determines the output drive current. Refer to specifications for the darlington driver and select the value for R2 that will provide enough drive to the output when the diode trio voltage is at a minimum.

$$I_{Drive} \cong \frac{V_{min} - 2.8\ V}{R2 + 50\ \Omega}$$

R6 This resistor in conjunction with R3 is used to set the maximum overvoltage.

$$\text{Maximum overvoltage} \cong \frac{R3 + R6}{R6} \quad (7.5)$$

R7 Used for compensation (Approximately 3.0 kΩ)

C1, C2 Used for compensation (Approximately 0.01 μF)

7

ORDERING INFORMATION

Device	Temperature Range	Package
MC3330P	0°C to +75°C	Plastic DIP

MC3330

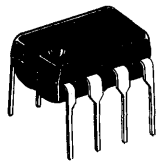
DIFFERENTIAL/CASCODE AMPLIFIER

. . . designed for applications requiring differential or cascode amplifiers.

- Extremely Flexible Amplifier
- Diode Available for Biasing
- Economical 8-Pin Dual In-Line Package
- Formerly MFC8030 In Case 644A Package

DIFFERENTIAL/CASCODE AMPLIFIER

SILICON MONOLITHIC FUNCTIONAL CIRCUIT



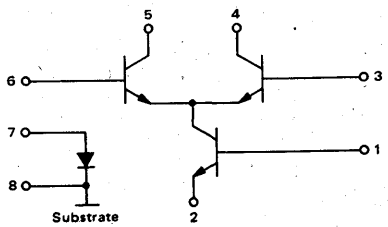
P SUFFIX
PLASTIC PACKAGE
CASE 626-03

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

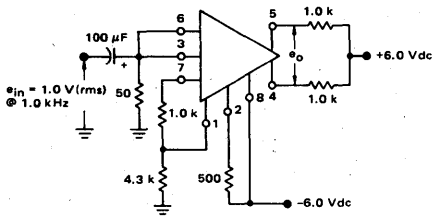
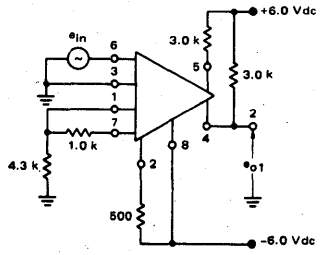
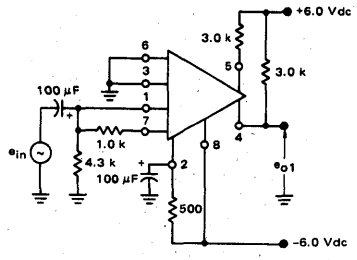
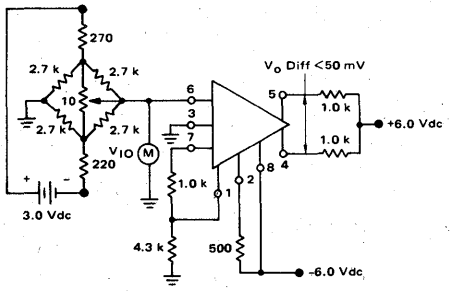
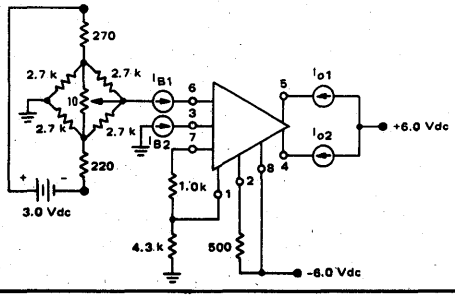
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	Vdc
Input Differential Voltage	V_I	±5.0	Vdc
Power Dissipation @ T_A = 25°C (Package Limitation)	P_D	1.2	Watts
Derate above 25°C	$1/R_{\theta JA}$	10	mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C

7

FIGURE 1 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Circuit	Characteristic	Symbol	Min	Typ	Max	Unit
	AC Common-Mode Rejection $e_{4-5} = e_o$ $CMR = 20 \log \frac{(e_{in})}{(e_o)}$	CMR_{AC}	–	35	–	dB
	Differential-Mode Voltage Gain A_V Diff = $20 \log \frac{(e_{o1})}{(e_{in})}$ (e_{in} = 1.0 kHz, 1.0 mV[rms]) (e_{in} = 10 MHz, 1.0 mV[rms]) (e_{in} = 50 MHz, 1.0 mV[rms])	$A_{V(dif)}$	 – – –	 32 26 10	 – – –	dB
	Cascode-Mode Voltage Gain A_V Cascode = $20 \log \frac{(e_{o1})}{(e_{in})}$ (e_{in} = 1.0 kHz, 1.0 mV[rms]) (e_{in} = 10 MHz, 1.0 mV[rms]) (e_{in} = 50 MHz, 1.0 mV[rms])	$A_{V(cscd)}$	 – – –	 36 31.5 15	 – – –	dB
	Input Offset Voltage	V_{IO}	–	5.0	10	mV
	DC Current Gain Match (I_{o1} = I_{o2})	$\frac{h_{FE1}}{h_{FE2}}$	0.8	–	1.25	–

MC3333

VARI-DWELL IGNITION CIRCUIT

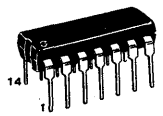
. . . designed for use in conjunction with a flux averaging sensor and a high energy ignition coil to provide regulated current pulses to the coil from information supplied by the sensor.

- Wide Supply Voltage Operating Range (4 to 24 V)
- Externally Adjustable Overvoltage Shutdown
- Externally Adjustable Dwell Time and Spark Energy
- Extremely Stable Output Current Pulses
- Variable Input Threshold Compensates for Low Supply Voltage Conditions
- Low Static Current Drain
- Also Available in Flip-Chip (MCCF3333) and Standard Chip (MCC3333) Form

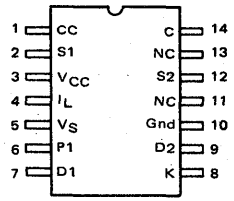
VARI-DWELL IGNITION CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 646



PIN CONNECTIONS

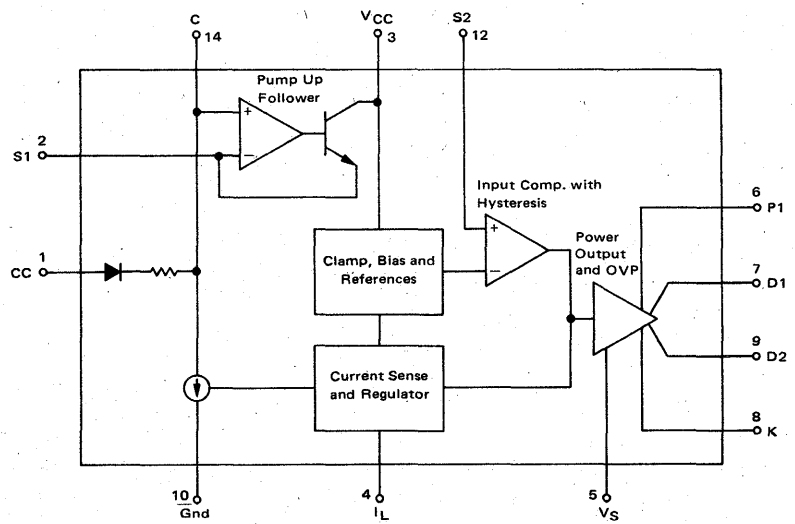


ORDERING INFORMATION

Device	Temperature Range	Package
MC3333P	-40 to +85	Plastic DIP

7

FIGURE 1 – BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage Steady State (Through 400 Ω, see Fig. 2) Transients of 300 ms or less	V_{CC}	24 90	Vdc
Peak Output Sink Current Transients of 300 ms or less	$I_{S(PEAK)}$	 1.3	A
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 14.5 V, T_A = 25°C unless otherwise specified; Figure 2.)

Characteristic	Symbol	Pin(s) Under Test	S1	S2	S3	S4	S5	S6	Min	Typ	Max	Unit
Current Drain	I_D	3	A	A	A	A	A	A	8.0	15	25	mA
Pre-Driver On	V_{P1}	6	A	A	A	A	A	A	–	.90	2.0	V
D1, D2 Output On	$V_{D1, D2}$	7&9	A	A	A	A	A	A	–	110	500	mV
Kelvin Contact	V_K	8	A	A	A	A	A	A	–	40	200	mV
CC Charge Circuit	V1	1	B	A	A	A	A	E	700	800	900	mV
S1 Follower	V_{S1}	2	A	B	A	A	A	C	1.4	1.6	1.8	V
C Clamp High	V_c	14	A	A	A	A	A	D	–	8.4	8.8	V
S2 Turn On (measure V_{S2} ramp value at P1 switch point.)	V_{S2}	12	A	A	A	A	B	A	1.6	1.9	2.1	V
Overvoltage Protection	V_S	5	A	A	A	B	C	A	8.0	9.1	10	V
Current Limit Trip	V_{IL}	4	A	A	B	A	C	B	150	180	220	mV

FIGURE 2 – TEST CIRCUIT

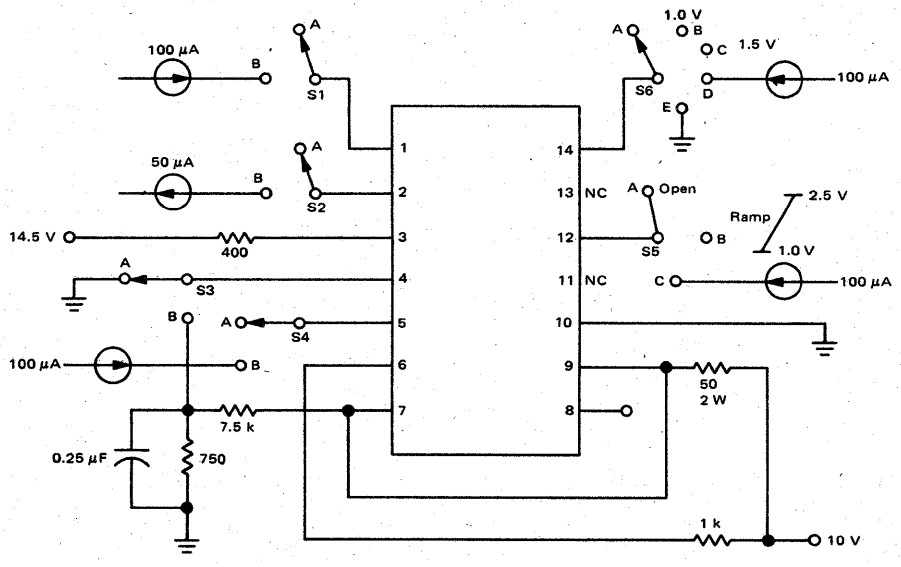
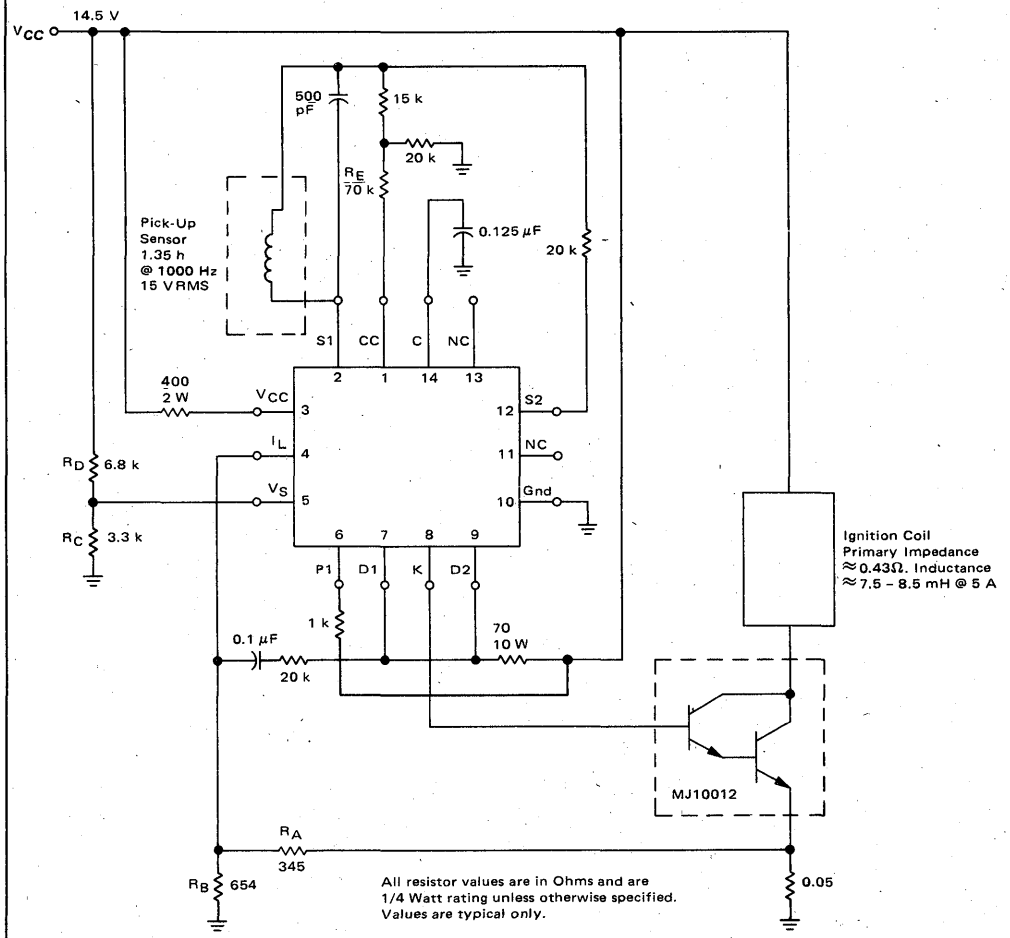


FIGURE 3 – TYPICAL APPLICATION CIRCUIT



Notes:

1. The ratio of R_A to R_B controls the ignition coil regulated current:

$$I_{COIL} \approx 3.6 \left(\frac{R_A + R_B}{R_B}\right) \qquad R_A + R_B \approx 1\ k\Omega$$

2. The ratio of R_D to R_C sets the over-voltage shutdown point with respect to B+.

$$B+_{overvoltage} \approx 8 \left(\frac{R_C + R_D}{R_C}\right) \qquad R_C + R_D \approx 10\ k\Omega$$

3. R_E is active region dwell control. R_E = 70 kΩ results in output current limit time of approximately 10% at 1000 RPM (with respect to one distributor cycle in an 8 cylinder engine). Values less than 70 kΩ lengthen this limit time and values higher shorten this limit time.
4. The 0.1 µF capacitor at pin 4 may be eliminated and stability maintained. A readjustment of the R_A and R_B resistors will be required.

ORDERING INFORMATION

Device	Temperature Range	Package
MC3340P	0°C to +75°C	Plastic DIP

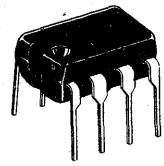
MC3340P

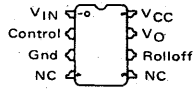
ELECTRONIC ATTENUATOR

- Designed for use in:
  - DC Operated Volume Control
  - Compression and Expansion Amplifier Applications
- Controlled by DC Voltage or External Variable Resistor
- Economical 8-Pin Dual In-Line Package
- Formerly MFC6040 in Case 643A Package

ELECTRONIC ATTENUATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT



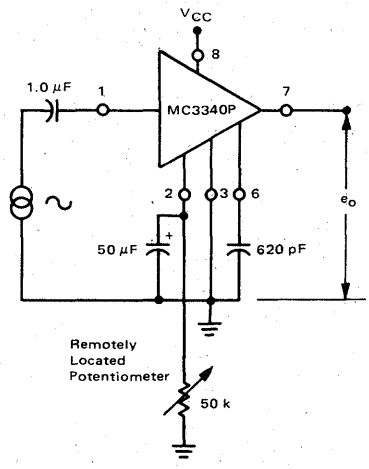


PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	20	Vdc
Power Dissipation @ T_A = 25°C Derate above T_A = 25°C	1.2 10	Watts mW/°C
Operating Ambient Temperature Range	0 to +75	°C

FIGURE 1 – TYPICAL DC "REMOTE" VOLUME CONTROL



7

ELECTRICAL CHARACTERISTICS (e_{in} = 100 mV (RMS), f = 1.0 kHz, R1 = 0, V_{CC} = 16 Vdc, T_A = +25°C unless otherwise noted.)

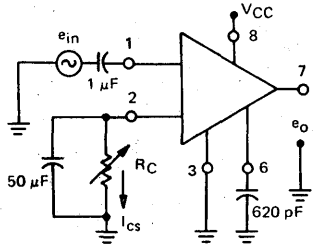
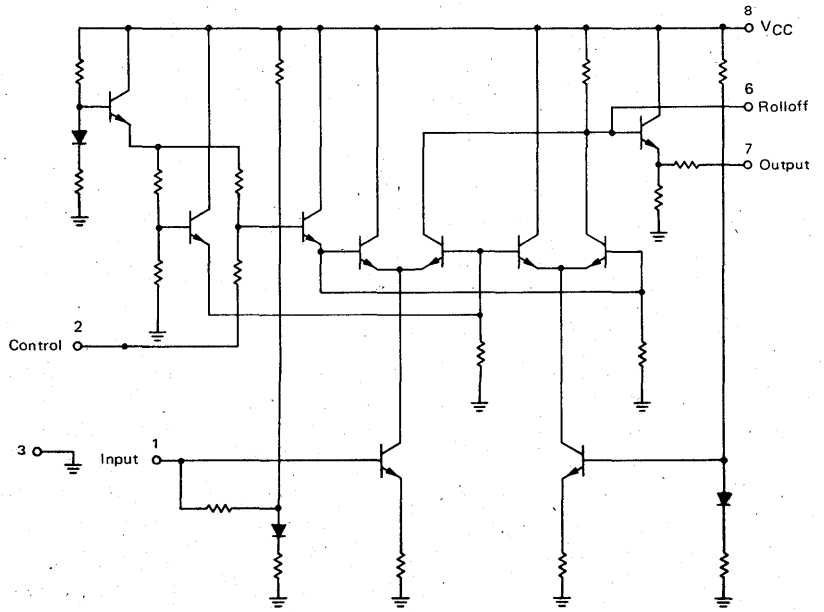
Circuit	Characteristic	Min	Typ	Max	Unit
	Operating Power Supply Voltage	9.0	–	18	Vdc
	Control Terminal Sink Current (e_{in} = 0)	–	–	2.0	mAdc
	Maximum Input Voltage	–	–	0.5	V(RMS)
	Voltage Gain	11	13	–	dB
	Attenuation Range (R_C = 33 k ohms)	70	90	–	dB
	Total Harmonic Distortion (Pin 2 Gnd) (e_{in} = 100 mV (RMS), $e_o = A_V \times e_{in}$)	–	0.6	1.0	%

FIGURE 2 – CIRCUIT SCHEMATIC



TYPICAL ELECTRICAL CHARACTERISTICS

(V_{CC} = 16 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3 – ATTENUATION versus DC CONTROL VOLTAGE

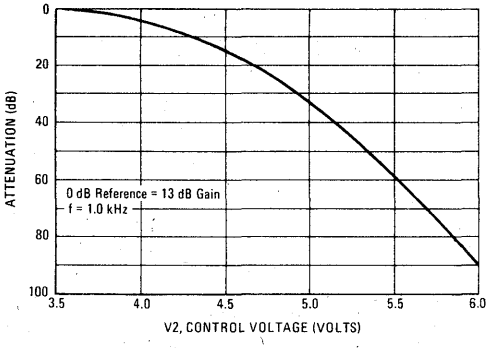


FIGURE 4 – ATTENUATION versus CONTROL RESISTOR

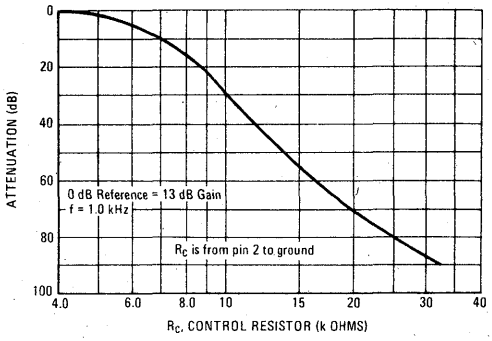


FIGURE 5 – FREQUENCY RESPONSE

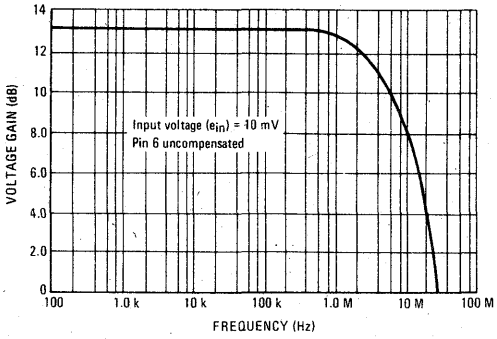


FIGURE 6 – OUTPUT VOLTAGE SWING

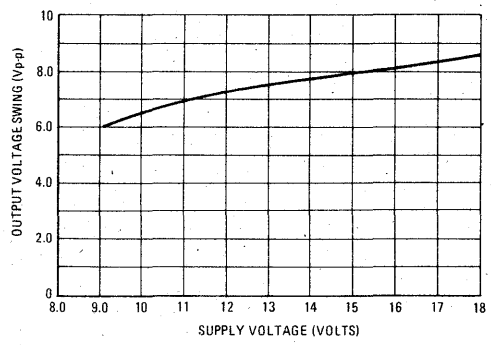
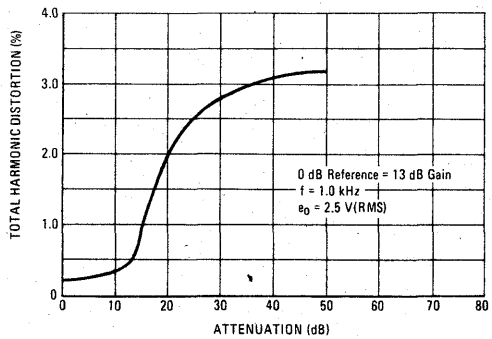


FIGURE 7 – TOTAL HARMONIC DISTORTION



ORDERING INFORMATION

Device	Temperature Range	Package
MC3346P	−40°C to +85°C	Plastic DIP
MC3386P	−40°C to +85°C	Plastic DIP

MC3346
MC3386

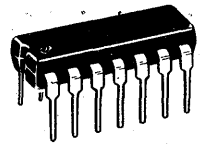
ONE DIFFERENTIALLY-CONNECTED PAIR AND THREE ISOLATED TRANSISTOR ARRAY

The MC3346 and MC3386 are designed for general-purpose, low power applications for consumer and industrial designs.

- Guaranteed Base-Emitter Voltage Matching
- Operating Current Range Specified – 10 μA to 10 mA
- Five General-Purpose Transistors in One Package

GENERAL-PURPOSE TRANSISTOR ARRAY

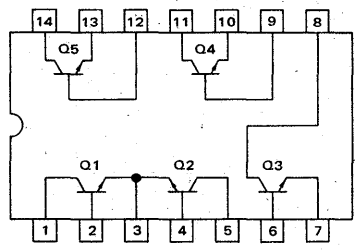
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector-Substrate Voltage	V_{CIO}	20	Vdc
Collector Current – Continuous	I_C	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C Derate Each Transistor @ 25°C	P_D	1.2 10 300	Watts mW/°C mW/°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	MC3346P			MC3386P			Unit
		Min	Typ	Max	Min	Typ	Max	
STATIC CHARACTERISTICS								
Collector-Base Breakdown Voltage (I_C = 10 μAdc)	BV_{CBO}	20	60	–	20	60	–	Vdc
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc)	BV_{CEO}	15	–	–	15	–	–	Vdc
Collector-Substrate Breakdown Voltage (I_C = 10 μA)	BV_{CIO}	20	60	–	20	60	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc)	BV_{EBO}	5.0	7.0	–	5.0	7.0	–	Vdc
Collector-Base Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	–	–	40	–	–	100	nAdc
DC Current Gain	h_{FE}							–
(I_C = 10 mAdc, V_{CE} = 3.0 Vdc)		–	140	–	–	–	–	
(I_C = 1.0 mAdc, V_{CE} = 3.0 Vdc)		40	130	–	40	130	–	
(I_C = 10 μAdc, V_{CE} = 3.0 Vdc)		–	60	–	–	–	–	
Base-Emitter Voltage	V_{BE}							Vdc
(V_{CE} = 3.0 Vdc, I_E = 1.0 mAdc)		–	0.72	–	–	0.72	–	
(V_{CE} = 3.0 Vdc, I_E = 10 mAdc)		–	0.80	–	–	0.80	–	
Input Offset Current for Matched Pair Q1 and Q2 (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	$\lvert I_{IO1} - I_{IO2} \rvert$	–	0.3	2.0	–	0.3	–	μAdc
Magnitude of Input Offset Voltage (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	–	–	0.5	5.0	–	0.5	–	mVdc
Temperature Coefficient of Base-Emitter Voltage (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	$\frac{\Delta V_{BE}}{\Delta T}$	–	-1.9	–	–	-1.9	–	mV/°C
Temperature Coefficient	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	–	1.0	–	–	1.0	–	μV/°C
Collector-Emitter Cutoff Current (V_{CE} = 10 Vdc, I_B = 0)	I_{CEO}	–	–	0.5	–	–	5.0	μAdc
DYNAMIC CHARACTERISTICS								
Low Frequency Noise Figure (V_{CE} = 3.0 Vdc, I_C = 100 μAdc, R_S = 1.0 kΩ, f = 1.0 kHz)	NF	–	3.25	–	–	3.25	–	dB
Forward Current Transfer Ratio (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	h_{FE}	–	110	–	–	110	–	–
Short-Circuit Input Impedance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{ie}	–	3.5	–	–	3.5	–	kΩ
Open-Circuit Output Impedance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{oe}	–	15.6	–	–	15.6	–	μmhos
Reverse Voltage Transfer Ratio (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{re}	–	1.8	–	–	1.8	–	$x10^{-4}$
Forward Transfer Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{fe}	–	31–j1.5	–	–	31–j1.5	–	–
Input Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{ie}	–	0.3+j0.04	–	–	0.3+j0.04	–	–
Output Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{oe}	–	0.001+j0.03	–	–	0.001+j0.03	–	–
Current-Gain — Bandwidth Product (V_{CE} = 3.0 Vdc, I_C = 3.0 mAdc)	f_T	300	550	–	–	550	–	MHz
Emitter-Base Capacitance (V_{EB} = 3.0 Vdc, I_E = 0)	C_{eb}	–	0.6	–	–	0.6	–	pF
Collector-Base Capacitance (V_{CB} = 3.0 Vdc, I_C = 0)	C_{cb}	–	0.58	–	–	0.58	–	pF
Collector-Substrate Capacitance (V_{CS} = 3.0 Vdc, I_C = 0)	C_{CI}	–	2.8	–	–	2.8	–	pF

TYPICAL CHARACTERISTICS

FIGURE 1 – COLLECTOR CUTOFF CURRENT versus TEMPERATURE (Each Transistor)

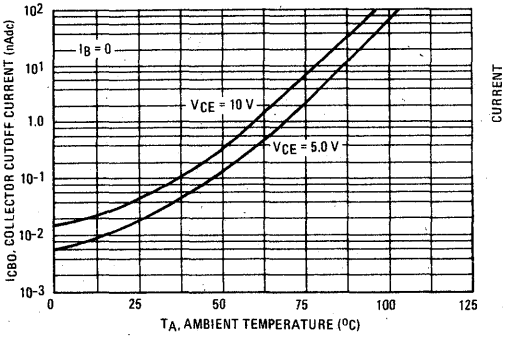


FIGURE 2 – COLLECTOR CUTOFF CURRENT versus TEMPERATURE (Each Transistor)

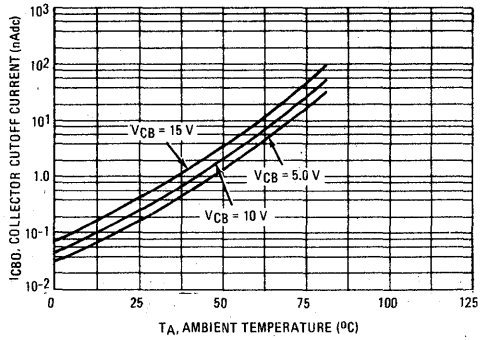


FIGURE 3 – INPUT OFFSET CHARACTERISTICS FOR Q1 and Q2

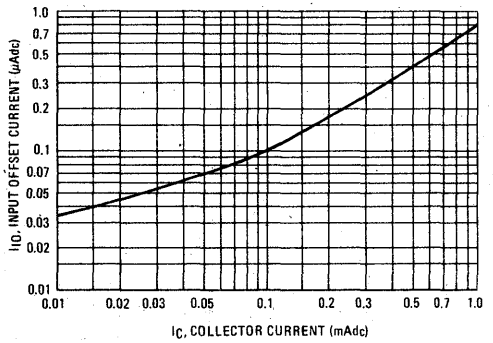


FIGURE 4 – BASE-EMITTER AND INPUT OFFSET VOLTAGE CHARACTERISTICS

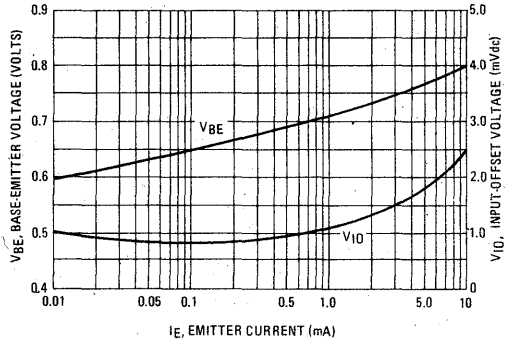
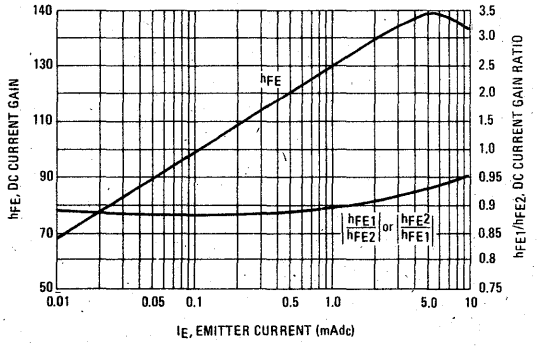


FIGURE 5 – DC CURRENT GAIN



ORDERING INFORMATION

Device	Temperature Range	Package
MC3360P	−10°C to +75°C	Plastic DIP

MC3360P

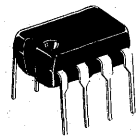
1/4-WATT AUDIO AMPLIFIER

. . . designed for the output stage of battery-powered portable radios.

- 250 mW of Audio Output Power
- Low Standby Current – 3.5 mA typical
- Low Harmonic Distortion
- Reduces Component Count in Portable Radios
- Formerly MFC4000B Packaged in Plastic Case 206A.

1/4-WATT AUDIO AMPLIFIER

SILICON MONOLITHIC
FUNCTIONAL CIRCUIT

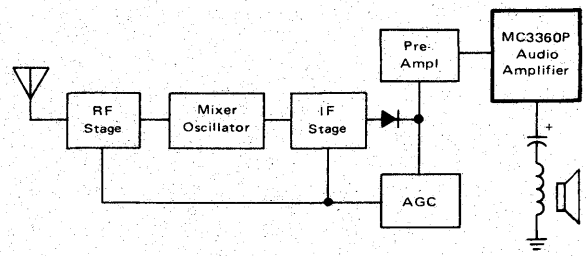


PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	12	Vdc
Power Dissipation (Package Limitation) Derate above T_A = +25°C	1.2 10	Watts mW/°C
Operating Ambient Temperature Range	-10 to +75	°C

TYPICAL APPLICATION



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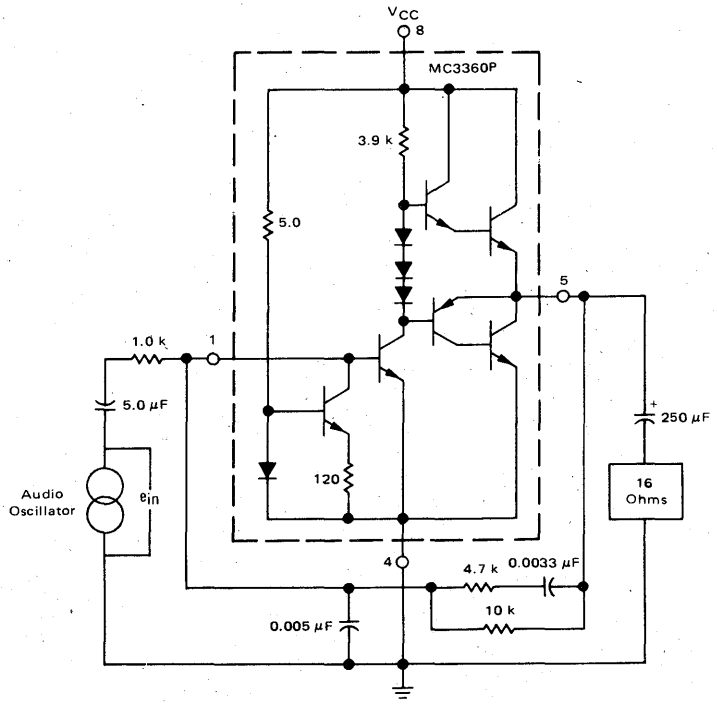
ELECTRICAL CHARACTERISTICS* (V_{CC} = 9.0 Vdc, R_L = 16 Ohms, T_A = +25°C unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Zero Signal Current Drain	–	3.0	5.0	mAdc
Sensitivity P_O = 250 mW(RMS)	–	–	240	mV(RMS)
Output Power Total Harmonic Distortion ≤ 10%	250	350	–	mW(RMS)
Total Harmonic Distortion P_O = 50 mW(RMS) P_O = 50 mW(RMS), V_{CC} = 6.0 Vdc	– –	0.7 4.5	– –	%

*As measured in test circuit shown in Figure 1.

FIGURE 1 – TEST CIRCUIT



TOTAL HARMONIC DISTORTION versus OUTPUT POWER

FIGURE 2 – V_{CC} = 9.0 Vdc

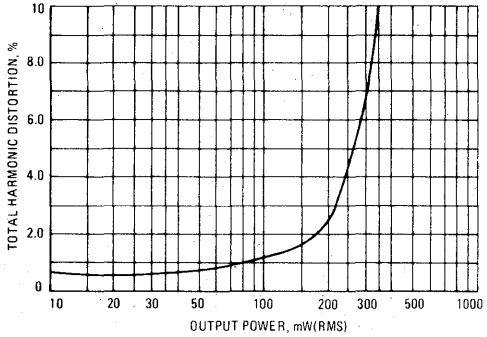


FIGURE 3 – V_{CC} = 6.0 Vdc

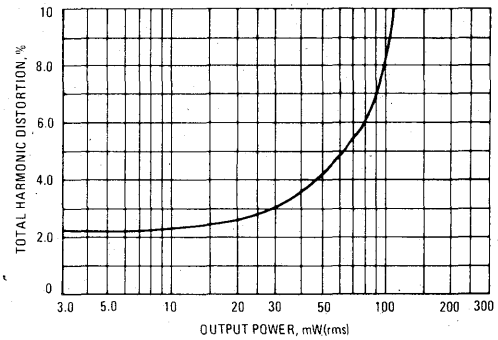


FIGURE 4 – CURRENT DRAIN versus OUTPUT POWER

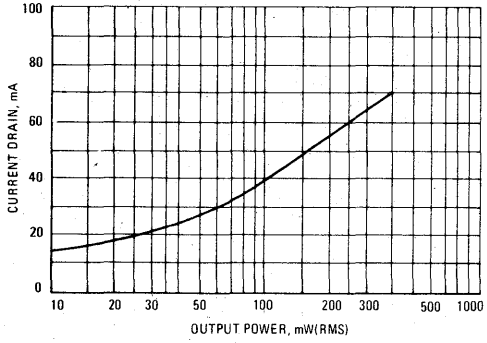


FIGURE 5 – TOTAL HARMONIC DISTORTION versus SUPPLY VOLTAGE

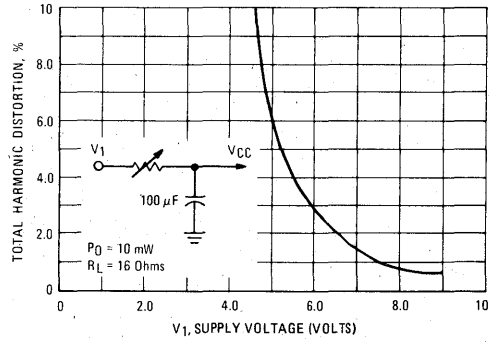
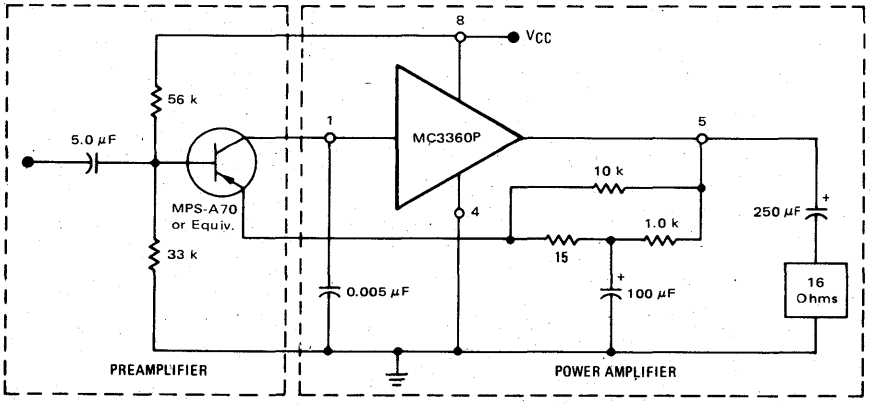


FIGURE 6 – TYPICAL CIRCUIT APPLICATION



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ORDERING INFORMATION

Device	Temperature Range	Package
MC3380P	0°C to +75°C	Plastic DIP

MC3380P

EMITTER COUPLED
ASTABLE
MULTIVIBRATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT

EMITTER COUPLED ASTABLE MULTIVIBRATOR
With Programmable Pulse Width and Current-Controlled Pulse Repetition Rate

The MC3380P is a monolithic device designed for use as a general building block in control and power supply applications.

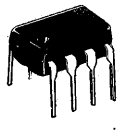
Its extremely flexible design makes it useful in dc-dc converter applications and power supply regulator circuits. Its fixed pulse width, variable frequency mode of operation makes it useful in switching regulator applications with either fixed or variable loads. This device is capable of stepping up (Figures 5 and 9) or stepping down (Figure 14) dc input voltages, and can produce regulated multiple output dc voltages of either positive or negative polarity (Figure 14).

This device can also be used as a frequency source when configured as a multivibrator.

As a DC-DC Converter –
Differential Line Regulation (Figure 9) –
= 1 V (Max) @ V_{CC} = 3 to 7.5 V

As a Power Regulator –
Load Regulation (Figure 5) –
0.2% (Typ) @ P_D = 1 to 3 Watts

As a Multivibrator –
High Toggle Frequency = 100 kHz (Typ)



PLASTIC PACKAGE
CASE 626

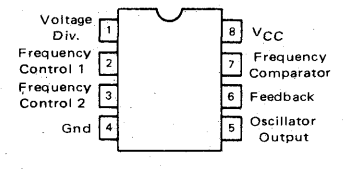


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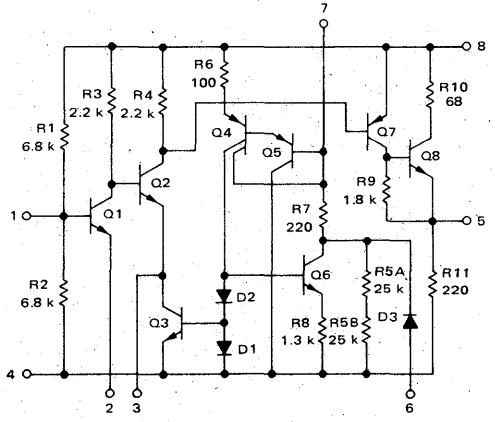
FIGURE 1 – CIRCUIT SCHEMATIC



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Output Current - Pin 8	I_O	100	mA
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 3.0	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 Vdc, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
EMITTER-COUPLED ASTABLE MULTIVIBRATOR					
Rise Time (C = 0.0034 μF, R1 = R2 = 10 kΩ, f = 100 kHz, Figure 4)	t_r	–	12	–	ns
Fall Time (C = 0.0034 μF, R1 = R2 = 10 kΩ, f = 100 kHz, Figure 4)	t_f	–	45	–	ns
Toggle Frequency (C = 0.002 μF, R1 = R2 = 10 k, Figures 2, 3, 4)	–	–	100	–	kHz
3-WATT REGULATOR					
Power Efficiency (Figure 5) (V_O = 200 Vdc @ 15 mAdc)	–	–	60	–	%
Load Regulation (Figure 5) (P_{out} < 3.0 W)	Reg_{load}	–	0.2	–	%
Line Regulation (Figure 5) (V_{CC} = 4.0 -6.0 Vdc)	Reg_{line}	–	0.3	–	%
Output Voltage (Figure 5)	V_O	–	200	–	V
Output Current (Figure 5)	I_O	–	15	–	mA
Supply Voltage (Figure 5)	V_{CC}	3.0	–	10	V
Supply Current (Figure 6) (I_{FB} = 0, R_L = ∞)	I_D	–	20	30	mA
Output Voltage High (Figure 6) (I_O = 2.0 mA, I_{FB} = 250 μA) (I_O = 25 mA, I_{FB} = 250 μA)	V_{OH}	 2.4 1.2	 3.5 1.5	 – –	V
Output Voltage Low (Figure 6) (I_O = -1.0 mA, I_{FB} = 600 μA)	V_{OL}	–	150	300	mV
Rise Time (Figure 7)	t_r	–	12	–	ns
On Time (Figure 7)	t_{on}	–	20	–	μs
Fall Time (Figure 7)	t_f	–	45	–	ns
Off Time (Figure 7)	t_{off}	–	20	–	μs
DC - DC CONVERTER					
Zener Bias Current (Figure 10) (V_{CC} = 5.0 Vdc, V_O > 2.4 Vdc) (V_{CC} = 5.0 Vdc, V_O < 0.4 Vdc)	 I_{FB1} I_{FB2}	 – 600	 – –	 250 –	 μA μA
Output Current (Figure 11) (V_{CC} = 5.0 Vdc)	I_{OH}	25	35	–	mA
Output Resistance (Figure 12) (V_{CC} = 5.0 Vdc, I_O = -1.0 mA)	r_o	150	220	300	Ω
Shutdown Voltage (Figure 13) (V_O < 0.5 V)	V_{CC}	–	–	1.6	V
Supply Voltage (Figure 9)		3.0	–	7.0	V
Differential Line Regulation (Figure 9) (ΔV_{CC} = 3.0 to 7.0 Vdc)	ΔV_{reg}	-1.0	–	+1.0	V
Feedback Voltage (Figure 9) (V_{CC} = 5.0 Vdc)	V_F	0.6	–	1.1	V
Voltage Efficiency (Figure 9) (V_{CC} = 5.0 Vdc, Eff(%) = $(V_{out}^2/(3.3\ k)\ (I_{CC})(V_{CC})$)	–	40	–	–	%

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FIGURE 2 – TYPICAL CAPACITANCE versus FREQUENCY

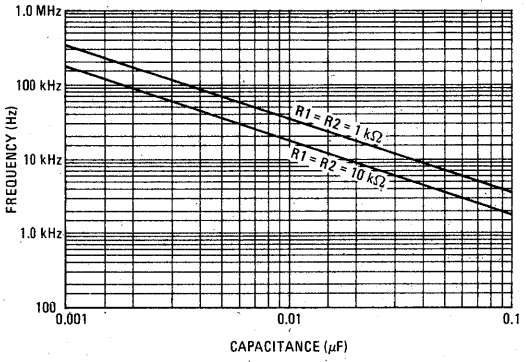


FIGURE 3 – TYPICAL DUTY CYCLE and FREQUENCY CHARACTERISTICS

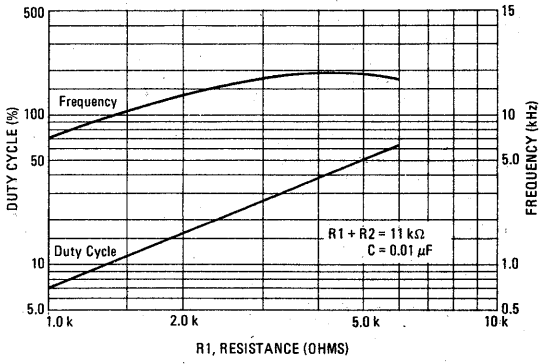


FIGURE 4 – ASTABLE MULTIVIBRATOR TEST CIRCUIT

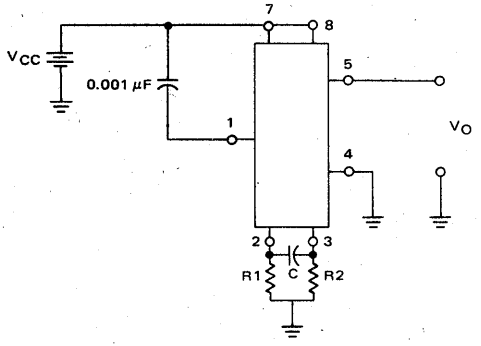
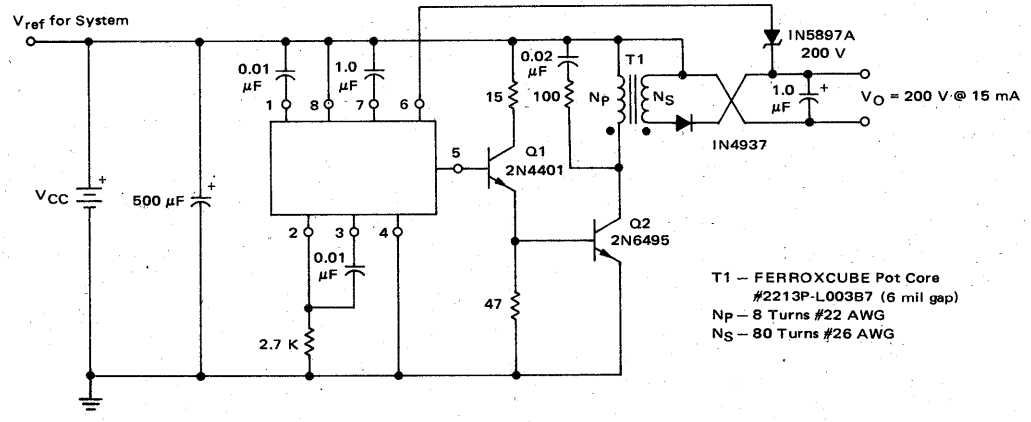


FIGURE 5 – 3-WATT SWITCHING REGULATOR APPLICATION CIRCUIT



3-Watt Switching Regulator - converts 5 V to 200 V for gas discharge displays such as Burroughs Panaplex and Beckman.

FIGURE 6 – STATIC TEST CIRCUIT

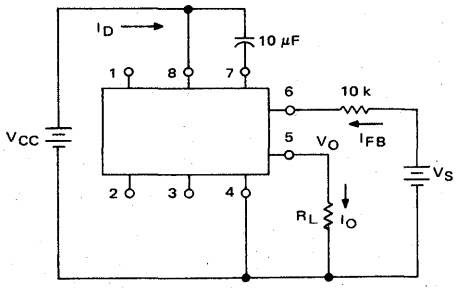


FIGURE 7 – DYNAMIC TEST CIRCUIT

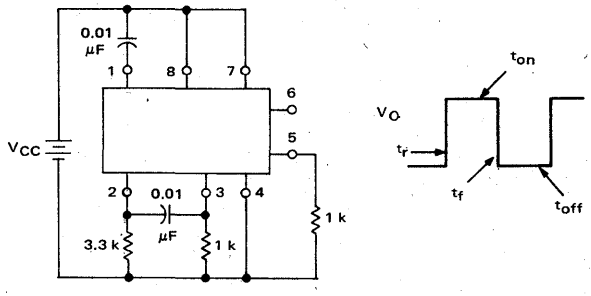


FIGURE 8 – SWITCHING WAVEFORMS AT Q2

Collector Current and Voltage Waveforms of 2N6495 (Q2) From Figure 5

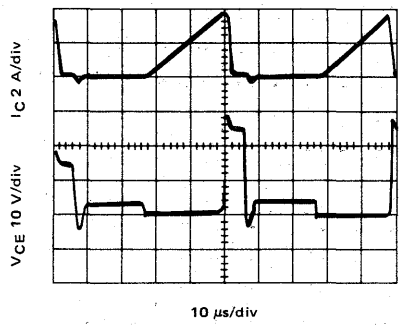
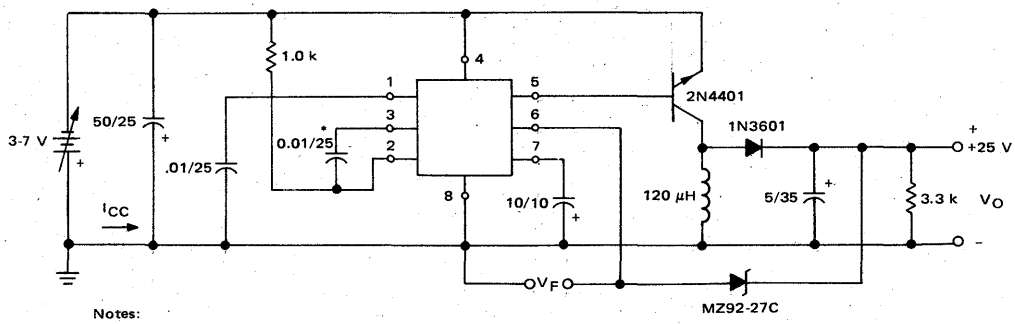


FIGURE 9 – TYPICAL APPLICATION IN 3 - 25 V DC-DC CONVERTER CONFIGURATION



Notes:
1. All resistor values in ohms, ± 1%, 1/4 W
2. All capacitor values in μF, = 20%, except * ± 5%.
3. All inductors ± 4%.

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DC - DC CONVERTER TEST CIRCUITS

FIGURE 10 – ZENER BIAS CURRENT TEST

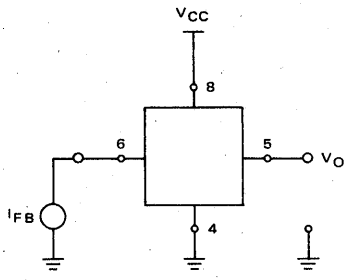


FIGURE 11 – OUTPUT CURRENT TEST

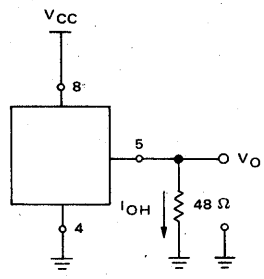
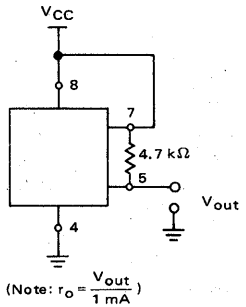


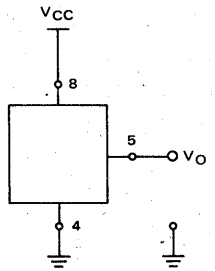
FIGURE 12 – OUTPUT RESISTANCE TEST



(Note: $r_o = \frac{V_{out}}{1\ mA}$)

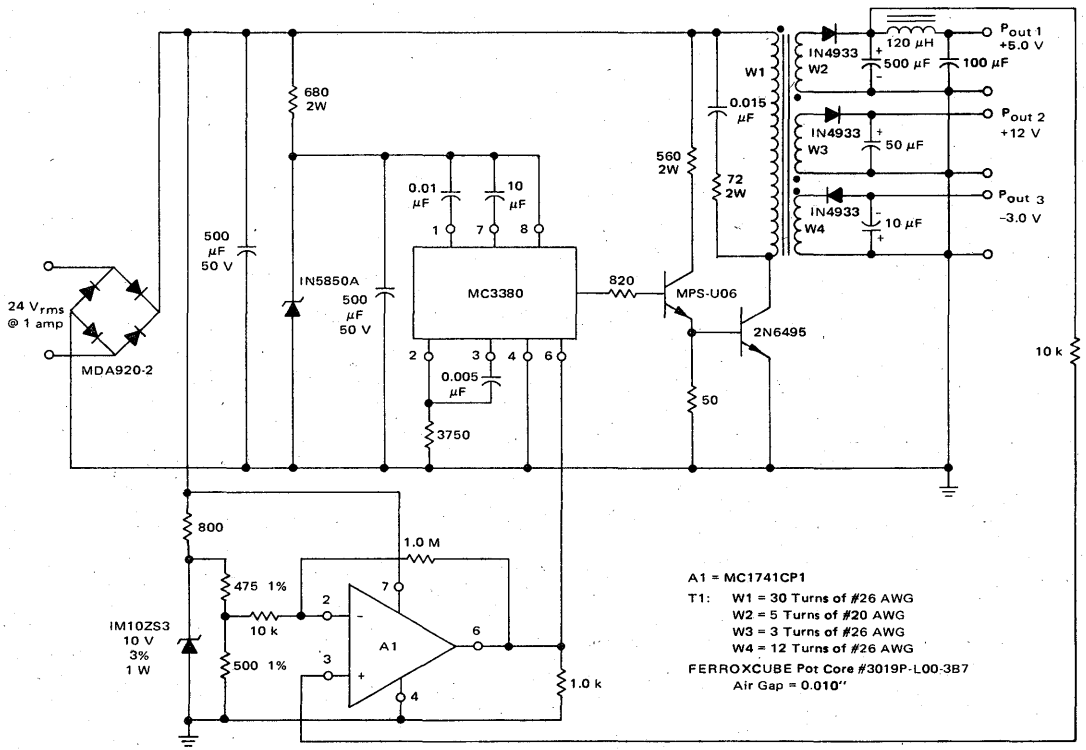
FIGURE 13 – SHUTDOWN VOLTAGE AND TEST

(NOTE: Decrease V_{CC} until $V_O < 0.5$ V)



7

FIGURE 14 – TYPICAL APPLICATION AS MULTIPLE OUTPUT SWITCHING REGULATOR FOR USE WITH MPU'S



TYPICAL PERFORMANCE
P_{out1} = 4 Watts
(V_O = 5 V ± 5%)
5 V Ripple Component = 50 mV
(120 Hz + 20 kHz)
P_{out2} = 600 mW
(V_O = 12 V ± 10%)
P_{out3} = 3 mW
(V_O = –3 V ± 10%)

7

MC3390

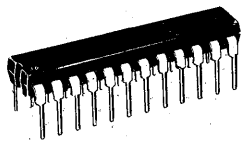
Product Preview

PHASE LOCKED LOOP FREQUENCY SYNTHESIZER

The MC3390 is a phase locked loop frequency synthesizer designed specifically for single crystal, Class-D citizen band radio applications. By utilizing recently developed circuit techniques, the IC incorporates high speed and high density logic in combination with standard linear functions and is processed with the same techniques and materials common to the Motorola low-cost consumer linear IC line.

- Developed Specifically for Class-D Citizen Band Radio Applications
- Targeted for Low Cost, High Volume Requirements
- Directly Compatible with the New 40 Channel Frequency Allocation
- Requires Only One Crystal to Generate All Transmit and Receive Frequencies
- Compatible with the MC3391 Remote Controller and Display Driver
- A Low-Cost Binary Coded Switch Can Be Used Directly for Channel Selection
- Compatible with Digital Display Techniques
- Linear Compatible I^2L Is Utilized for Optimum Cost Effectiveness
- Designed for Double or Single Conversion Receivers

PHASE LOCKED LOOP FREQUENCY SYNTHESIZER FOR CITIZEN'S BAND RADIO

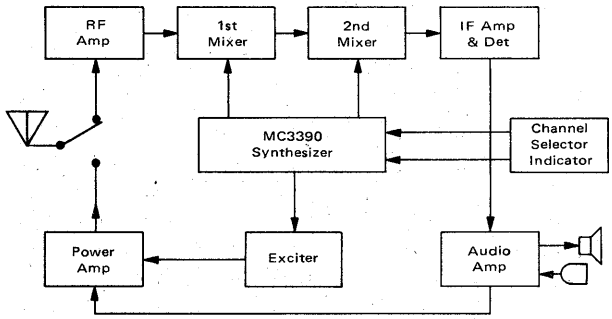


P SUFFIX
PLASTIC PACKAGE
CASE 724

ORDERING INFORMATION

Device	Temperature Range	Package
MC3390P	-40 to +85	Plastic DIP

CB RADIO USING MC3390 SYNTHESIZER



This is advance information and specifications are subject to change without notice.

MC3391

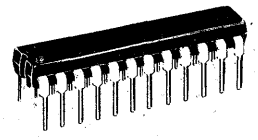
Product Preview

REMOTE CONTROLLER AND DISPLAY DRIVER FOR CITIZEN'S BAND RADIO

The MC3391 is a remote controller and display driver IC designed to be used in conjunction with the MC3390 frequency synthesizer for Class-D citizen's band radio applications.

The MC3391 provides the user the capability of incremental stepping from one channel to another by merely engaging a push button switch. Last channel memory is provided during power switch off conditions. The IC also provides the decoding and drive required by seven-segment light emitting diode or liquid crystal displays for channel number indication. It is fully compatible with the new 40 channel frequency allocation.

REMOTE CONTROLLER
AND
DISPLAY DRIVER
FOR
CITIZEN'S BAND RADIO



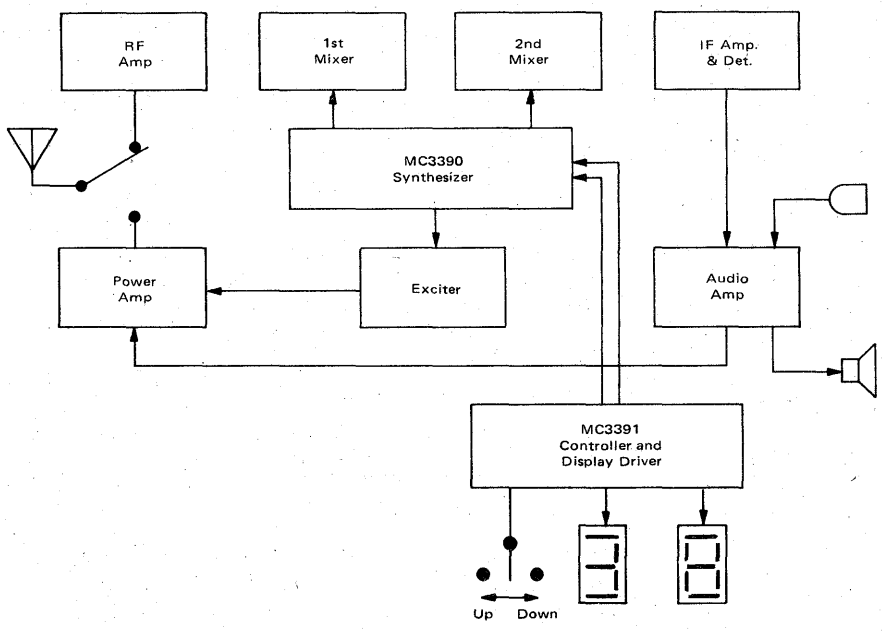
P SUFFIX
PLASTIC PACKAGE
CASE 724

ORDERING INFORMATION

Device	Temperature Range	Package
MC3391P	–40 to +85	Plastic DIP

TYPICAL APPLICATION

40 Channel CB Transceiver with remote and manual control capability and LED/LCD display



7

This is advance information and specifications are subject to change without notice.

TDA1190Z

Advance Information

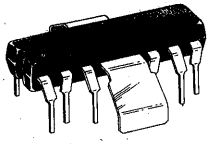
TV SOUND SYSTEM

The TDA1190Z 4.0 watt sound system is designed for television and related applications. Functions performed by this circuit include: IF Limiting, IF amplifier, low pass filter, FM detector, DC volume control, audio preamplifier, and audio power amplifier.

- 4.0 Watts Output Power
  (V_{CC} = 24 V, R_L = 16 Ω)
- Linear Volume Control
- High AM Rejection
- Low Harmonic Distortion
- High Sensitivity

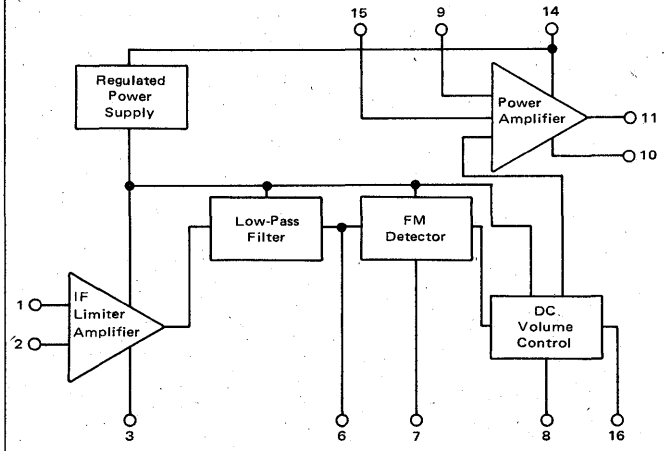
TV SOUND SYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT

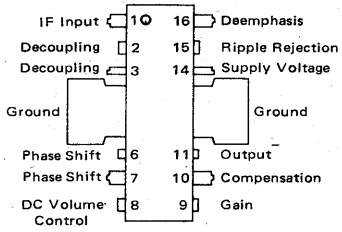


PLASTIC PACKAGE
CASE 722A

BLOCK DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
TDA1190Z	0 to +75°C	Plastic

This is advance information and specifications are subject to change without notice.

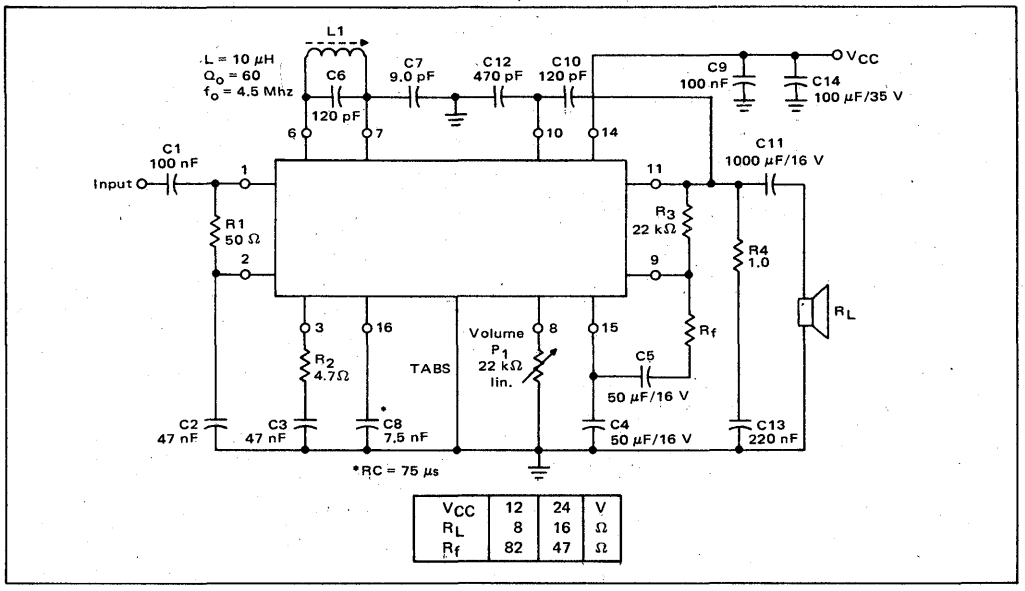
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	9.0 to 28	V
Input Signal Voltage	V_I	1.0	V
Output Peak Current (Non-repetitive) (Repetitive)	I_o	2.0 1.5	A
Operating Temperature Range	T_A	0 to +75	°C
Junction Temperature	T_J	150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 V, f_o = 4.5 MHz, Δf = ±25 kHz, T_A = 25°C unless otherwise noted.

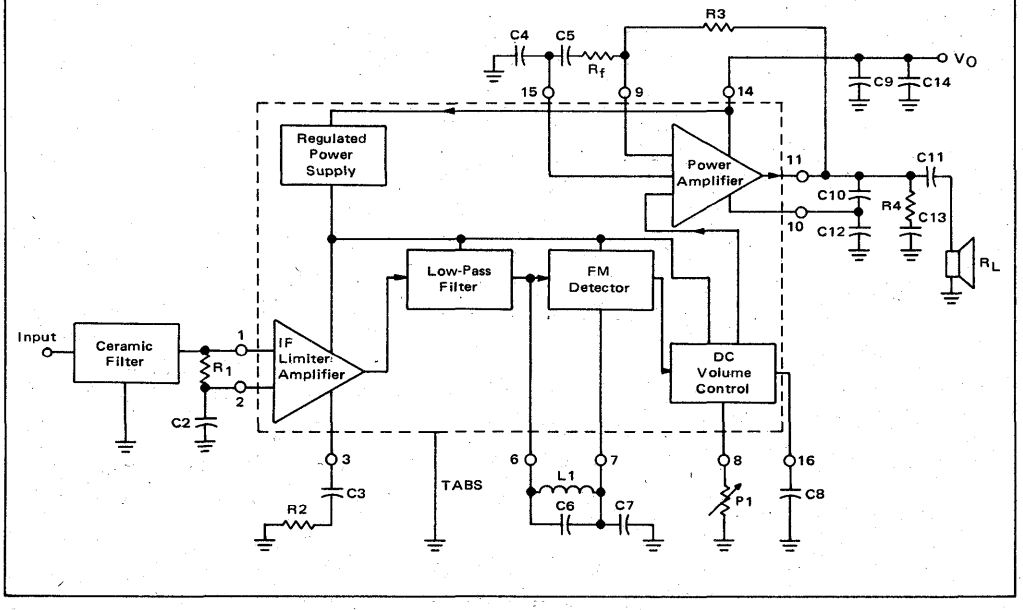
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Quiescent Output Voltage (pin 11)	V_O				V
V_{CC} = 24 V		11	12	13	
V_{CC} = 12 V		5.1	6.0	6.9	
Quiescent Drain Current	I_D				mA
(P1 = 22 kΩ)					
V_{CC} = 24 V		11	22	35	
V_{CC} = 12 V		–	19	–	
Output Power	P_O				W
(d = 10%, f_m = 400 Hz)					
V_{CC} = 24 V, R_L = 16 Ω		–	4.2	–	
V_{CC} = 12 V, R_L = 8.0 Ω		–	1.5	–	
(d = 2%, f_m = 400 Hz)					
V_{CC} = 24 V, R_L = 16 Ω		–	3.5	–	
V_{CC} = 12 V, R_L = 8.0 Ω		–	1.4	–	
Input Limiting Threshold Voltage (-3.0 dB) at pin 1 Δf = ±7.5 kHz, f_m = 400 Hz, P_1 = 0	V_I	–	40	100	μV
Distortion	d				%
(P_O = 50 mW, f_m = 400 Hz, Δf = ±7.5 kHz)					
V_{CC} = 24 V, R_L = 16 Ω		–	0.75	–	
V_{CC} = 12 V, R_L = 8.0 Ω		–	1.0	–	
Frequency Response of Audio Amplifier (-3.0 dB)	B				Hz
(R_L = 16 Ω, C_{10} = 120 pF, C_{12} = 470 pF, P_1 = 22 kΩ)					
R_f = 82 Ω		–	70 to 12 k	–	
R_f = 47 Ω		–	70 to 7.0 k	–	
Recovered Audio Voltage (pin 16) (V_I ≥ 1 mV, f_m = 400 Hz, Δf = ±7.5 kHz, P_1 = 0)	V_o	–	120	–	mV
Amplitude Modulation Rejection (V_I ≥ 1.0 mV, f_m = 400 Hz, m = 30%)	AMR	–	55	–	dB
Signal and Noise to Noise Ratio (V_I ≥ 1.0 mV, V_o = 4.0 V, f_m = 400 Hz)	$\frac{S+N}{N}$	50	65	–	dB
External Feedback Resistance (between pins 9 and 10)	R_f	–	–	22	kΩ
Input Resistance (pin 1) (V_I = 1.0 mV)	r_i	–	30	–	kΩ
Input Capacitance (pin 1) (V_I = 1.0 mV)	C_i	–	5.0	–	pF
Power Supply Rejection Ratio (R_L = 4.0 Ω, f_{ripple} = 100 Hz, P1 = 22 kΩ)	PSRR	–	46	–	dB
DC Volume Control Attenuation (P1 = 12 kΩ)	–	–	90	–	dB

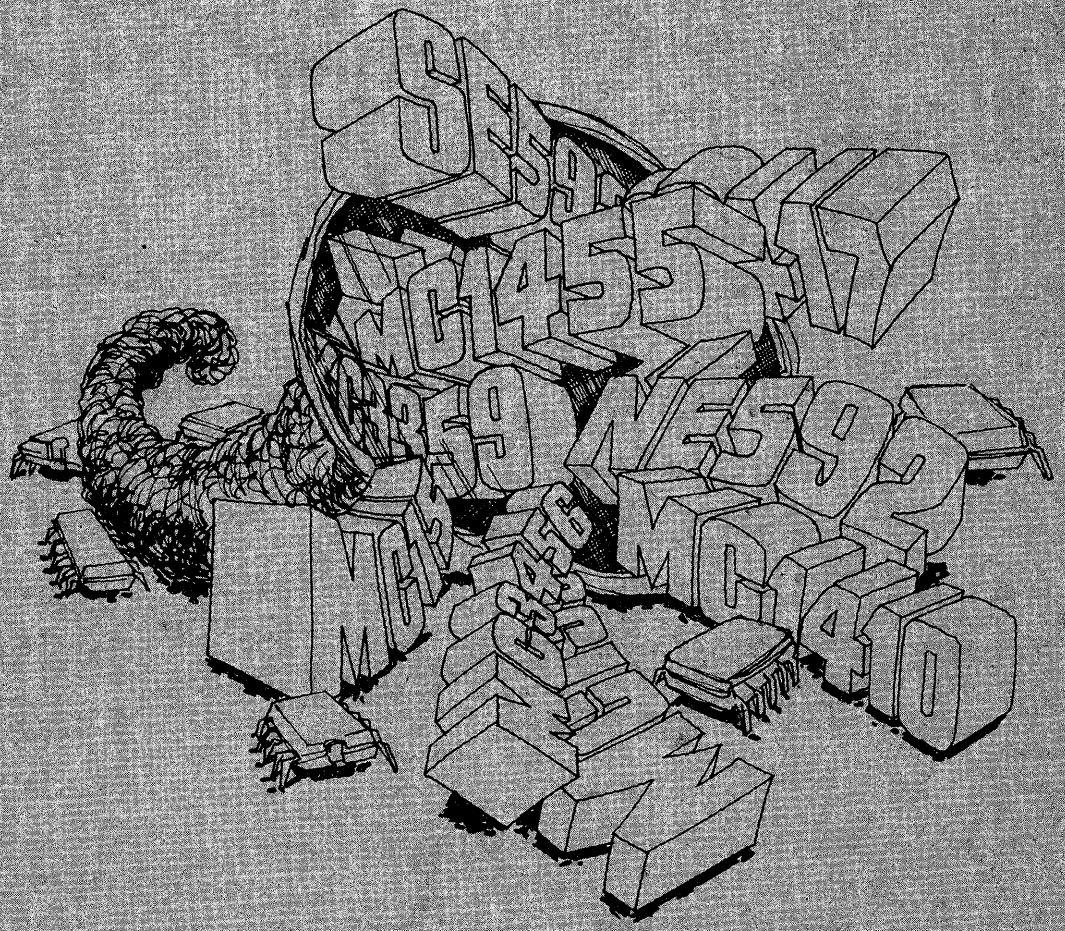
TEST CIRCUIT



V_{CC}	12	24	V
R_L	8	16	Ω
R_f	82	47	Ω

TYPICAL CIRCUIT CONFIGURATION





Other Linear Circuits / Chapter 8

OTHER LINEAR CIRCUITS

High Frequency Amplifiers

A variety of high-frequency circuits with features ranging from low-cost simplicity to multi-function versatility marks Motorola's line of integrated RF/IF amplifiers. Devices described here are intended for industrial and cummunications applications. For devices especially dedicated to consumer products, i.e., TV and entertainment radio, see page 7-3.

NON-AGC AMPLIFIERS

SE/NE592 — Differential Two Stage Video Amplifiers

A monolithic, two state differential output, wide-band video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems.

MC1733/MC1733C — Video Amplifier

Differential input and output amplifier provides three fixed gain options with bandwidth to 120 MHz. External resistor permits any gain setting from 10 to 400 v/v. Extremely fast rise time (2.5 ns typ) and propagation delay time (3.6 ns typ) makes this unit particularly useful as pulse amplifier in tape, drum, or disc memory read applications.

MC1552/MC1553 — Low Distortion Amplifier

Extremely high performance amplifier with internal series feedback for stable voltage gain and low distortion. Temperature compensation stablizes operating point. Has selectable gain option and well characterized data that permits accurate response shaping. Useful for critical applications such as wideband linear amplifiers or fast-rise pulse amplifiers.

MC1510/MC1410 — General-Purpose Differential Amplifier

Differential amplifier with flat response to 40 MHz. Provides excellent performance and simple design for most video and communications purposes.

AGC AMPLIFIERS

MC1550 — Low Cost Building Block

Single-stage cascade connected amplifier with delayed AGC characteristics, for operation at frequencies to 100 MHz. Has typical power gain of 25 dB @ 60 MHz.

MC1545/MC1445 — Gated 2-Channel Input

Differential input and output amplifier with gated 2-channel input for a wide variety of switching purposes. Typical 75 MHz bandwidth makes it suitable for high-frequency applications such as video switching, FSK circuits, multiplexers, etc. Gating circuit is useful for AGC control.

MC1590 — Wide-Band General Purpose

Has differential inputs and outputs with unneutralized power gain as high as 35 dB typical at 100 MHz in tuned amplifier service. Effective AGC voltage range from 5 to 7 volts for a 30 dB gain reduction.

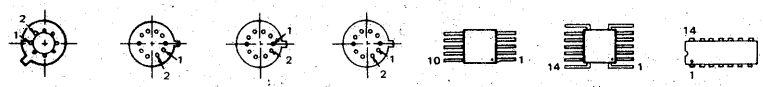
ELECTRICAL SPECIFICATIONS
AGC AMPLIFIERS

Operating Temperature Range		A_V dB	Band width MHz	V_{CC}/V_{EE} Vdc	Case
-55 to +125°C	0 to +75°C				
MC1550	—	22 Min	22	+6/–	602B,606
MC1590	—	44 Typ @ 10 4 Typ @ 100		+12/–	601
MC1545	MC1445	19 Typ @ 75		+5/–5	602A,607 632

NON AGC AMPLIFIERS

MC1733	MC1733C	52 @ 40 40 90 20 120	+6/–6	603,632
MC1510	MC1410	40 40	+6/–6	601
MC1553	—	46 @ 35 52 15	+6/–6	602B
MC1552	—	34 @ 40 40 @ 35	+6/–6	602B
SE592	NE592	55 @ 40 45 @ 90	+6/–6	603,632

PACKAGE STYLES



CASE	601	602A	602B	603	606	607	632
MATERIAL	Metal	Metal	Metal	Metal	Ceramic	Ceramic	Ceramic
SUFFIX after type number	G	G	G	G	F	F	L

8

Special Purpose Circuits

The linear-integrated-circuits listed in this section were developed by Motorola for the system design engineer to fill special-purpose requirements. Temperature ranges and package availability are tailored to provide price/performance versatility.

LINEAR FOUR-QUADRANT MULTIPLIERS

MC1594/1494

This device is designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

The MC1594/MC1494 is a variable transconductance multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power-supply rejection.

MC1595/MC1495

Similar to the MC1594/1494, but without internal level shift and voltage regulator circuits.

BALANCED MODULATOR-DEMODULATOR

MC1596/MC1496

Designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection and chopper applications.

TIMING CIRCUITS

MC1555/MC1455/MC1422

These devices are highly stable timing circuits capable of producing accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits. Timing from Microseconds through Hours.

The MC1422 has variable threshold level, adjustable externally.

	Timing Error (typ)
MC1555	0.5%
MC1455	1.0%
MC1422	1.0%

MC3556/MC3456

Dual Version of the MC1555/MC1455

Operating Temperature Range		
-55 to +125°C	0 to +70°C	Case
MC1554	MC1454	602B
MC1555		601, 693
	MC1455	601, 626, 693
MC1594	MC1494	620
MC1595	MC1495	632
MC1596		602A, 632
	MC1496	602A, 632, 646
	MC1422	601, 626
MC3505		632
	MC3405	632, 646
MC3556		632
	MC3456	632, 646
MC3523		693
	MC3423	626, 693
	MC3426	632
	MC3370	626

GROUND FAULT INTERRUPTED CIRCUITS

MC3426

(Latching)

This circuit provides ground fault and grounded neutral protection for 120 VAC, 15 and 20 Amp. lines. Useful in wall socket and circuit breaker applications.

- Trip Times in Accordance with U.L.
- High Noise Immunity
- Resistance to False Tripping
- Minimum Trip Leakage Current-5 ± mA
- Trips for Neutral Gnd. Resistance > 2

8

OVERVOLTAGE PROTECTION CIRCUIT

MC3423/MC3523

Protects sensitive electronic circuitry from over voltage conditions by short circuiting the supply current when an overvoltage occurs. This causes circuit breaker to trip or fuse to open.

- Adjustable Threshold Voltage
- Adjustable Energy Threshold
- Remote Activation
- Activation Indication

POWER CONTROL CIRCUITS

MC3370

Electronic switch for triac triggering applications. Features zero-crossing detector to eliminate RFI, differential input with dual sensor inputs, input open and short protection, and built-in regulator permitting AC line operation.

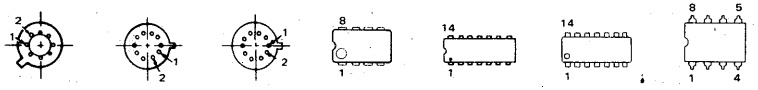
MONOLITHIC DUAL OP AMP-DUAL COMPARATOR

MC3505/MC3405

This device contains two differential input operational amplifiers and two comparators each set capable of single supply operation. This operational amplifier-comparator circuit will find its applications as a general purpose product for automotive circuits and as an industrial "building block".

- Op Amp Equivalent in Performance to MC3403
- Comparator Similar in Performance to MLM339
- Op Amps are Internally Frequency Compensated
- Supply Operation 3.0 Volts to 36.0 Volts
- Dual Supply Operation also Available

PACKAGE STYLES



CASE	601	602A	602B	626	632	646	693
MATERIAL	Metal	Metal	Metal	Plastic	Ceramic	Plastic	Ceramic
SUFFIX after type number	G	G	G	P or P1	L	P	U

8

ORDERING INFORMATION

Device	Temperature Range	Package
MC1410G	0°C to +75°C	Metal Can
MC1510G	−55°C to +125°C	Metal Can

MC1410
MC1510

WIDEBAND VIDEO AMPLIFIER

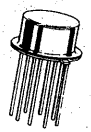
. . . designed for use as a high-frequency differential amplifier with operating characteristics that provide a flat frequency response from dc to 40 MHz.

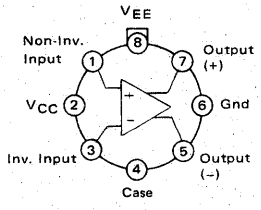
- High Gain Characteristics
  A_V = 93 typ
- Wide Bandwidth — dc to 40 MHz typ
- Large Output Voltage Swing
  4.5 Vp-p typical @ ±6.0 V Supply
- Low Output Distortion
  THD ≤ 1.5% typ

VIDEO AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

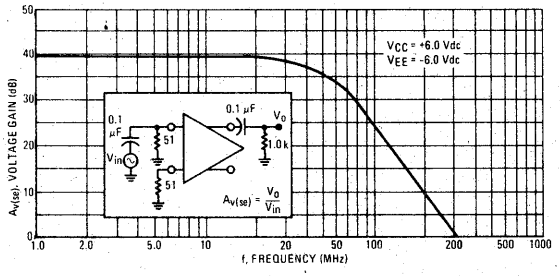
G SUFFIX
METAL PACKAGE
CASE 601





(Top View)

FIGURE 1 — VOLTAGE GAIN versus FREQUENCY



REPRESENTATIVE CIRCUIT SCHEMATIC

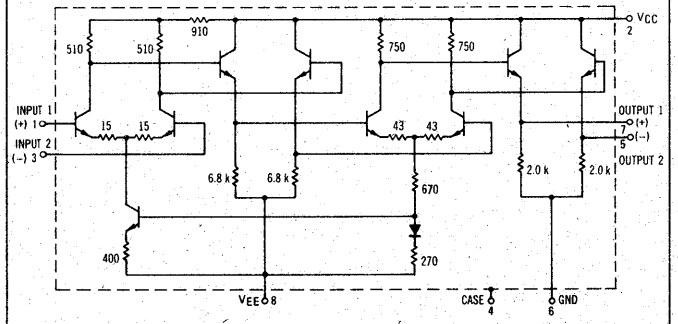
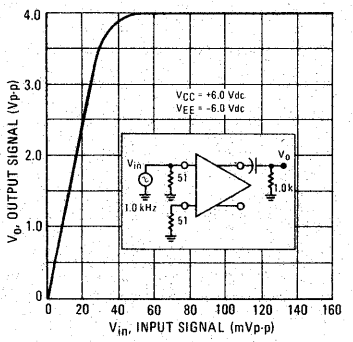


FIGURE 2 — LIMITING CHARACTERISTICS @ 1.0 kHz



8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+8.0 -8.0	Vdc
Differential Input Voltage Range	V_{IDR}	±5.0	Volts
Common Mode Input Voltage Range	V_{ICR}	±6.0	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	t_s	5.0	s
Power Dissipation (Package Limitation) Metal Can Derate above T_A = +25°C	P_D	 680 4.6	 mW mW/°C
Operating Temperature Range MC1410 MC1510	T_A	 0 to +75 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, R_L = 5.0 kΩ, T_A = +25°C unless otherwise noted.)

		MC1510			MC1410			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Single Ended Voltage Gain	$A_{v(se)}$	75	93	110	60	90	120	V/V
Output Impedance (f = 20 kHz)	Z_o	–	35	–	–	35	–	Ω
Input Impedance (f = 20 kHz)	Z_i	–	6.0	–	–	6.0	–	kΩ
Bandwidth (-3.0 dB)	BW	–	40	–	–	40	–	MHz
Output Voltage Swing (Single Ended) (f = 100 kHz)	V_o	–	4.0	–	–	4.0	–	Vp-p
Single Ended Output Distortion (e_{in} < 0.2% Distortion)	THD	–	1.5	5.0	–	2.0	–	%
Input Common Mode Voltage Range	V_{ICR}	–	±1.0	–	–	±1.0	–	V
Common Mode Voltage Gain (V_{in} = 0.3 V rms, f = 100 kHz)	AV_{CM}	-30	-45	–	-20	-40	–	dB
Common Mode Rejection Ratio	CMRR	–	85	–	–	85	–	dB
Input Bias Current $\left(I_{IB}=\frac{I_1+I_2}{2}\right)$, Differential Output = 0	I_{IB}	–	20	80	–	50	100	μA
Input Offset Current ($I_{IO} = I_1 - I_2$)	I_{IO}	–	3.0	20	–	5.0	30	μA
Output Offset Voltage Differential Mode (V_{in} = 0) Common Mode (Differential Output = 0)	$V_{OO(DM)}$ $V_{OO(CM)}$	– 2.6	0.5 3.1	1.3 3.5	– 2.0	0.5 3.0	2.0 4.0	Vdc
Step Response	t_{THL} t_{PHL}, t_{PLH} t_{TLH}	– – –	9.0 9.0 9.0	12 – 12	– – –	10 9.0 10	15 – 15	ns
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, T_A = T_{low}* to T_{high}**) ($R_S \leq$ 10 k Ω, T_A = T_{low} to T_{high})	$\Delta V_{IO}/\Delta T$	– –	±3.0 ±6.0	– –	– –	±3.0 ±6.0	– –	μV/°C
DC Power Consumption (Power Supply = ±6.0 V)	V_C	–	150	220	–	165	220	mW
Equivalent Average Input Noise Voltage (f = 10 Hz to 500 kHz, R_S = 0)	V_n	–	5.0	–	–	5.0	–	μV

*T_{low} = 0°C for MC1410 or −55°C for MC1510

**T_{high} = +75°C for MC1410 or +125°C for MC1510

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TYPICAL CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 3
POWER DISSIPATION versus SUPPLY VOLTAGE

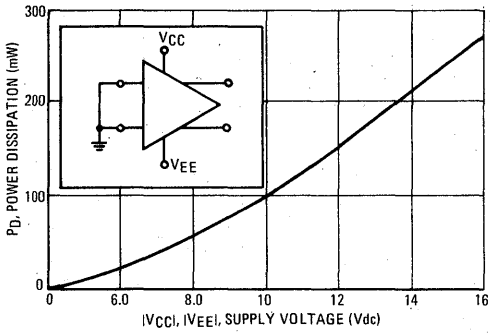


FIGURE 4
VOLTAGE GAIN versus SUPPLY VOLTAGE

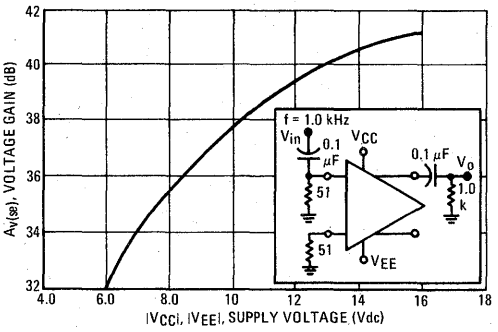


FIGURE 5
VOLTAGE GAIN versus TEMPERATURE

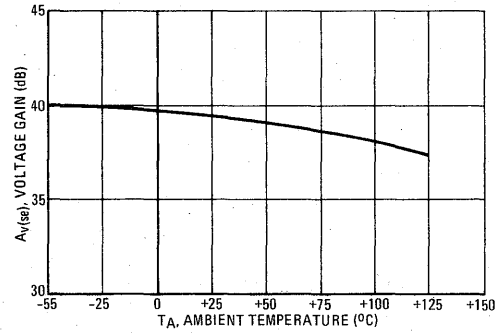


FIGURE 6
DC OUTPUT VOLTAGE versus TEMPERATURE

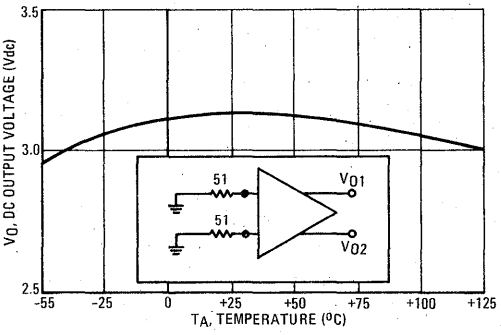


FIGURE 7
INPUT BIAS CURRENT versus TEMPERATURE

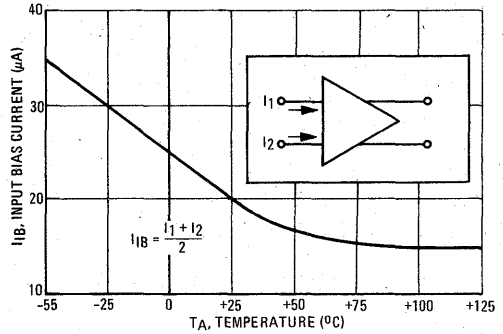
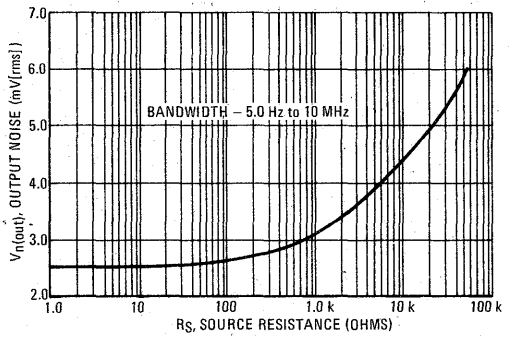


FIGURE 8
OUTPUT NOISE VOLTAGE versus SOURCE IMPEDANCE



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TYPICAL CHARACTERISTICS

FIGURE 9
LIMITING CHARACTERISTICS @ 30 MHz

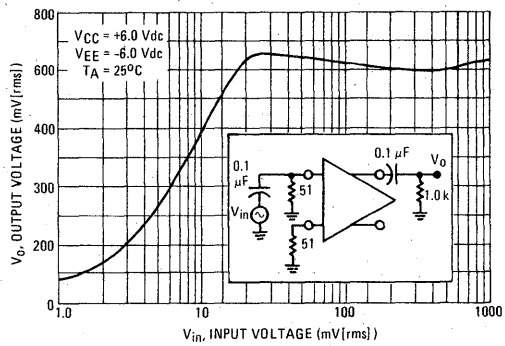
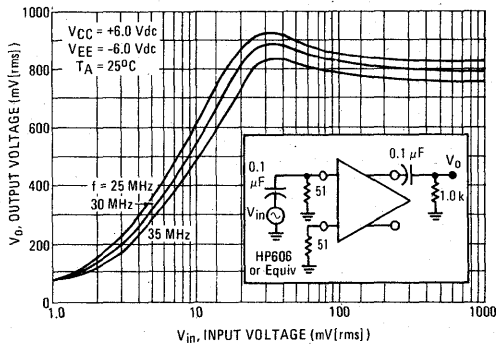


FIGURE 10
LIMITING CHARACTERISTICS versus FREQUENCY



TYPICAL APPLICATIONS

FIGURE 11
ENVELOPE DETECTOR

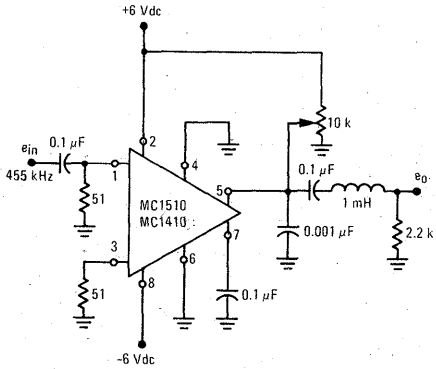


FIGURE 12
SINGLE STAGE WIDEBAND AMPLIFIER

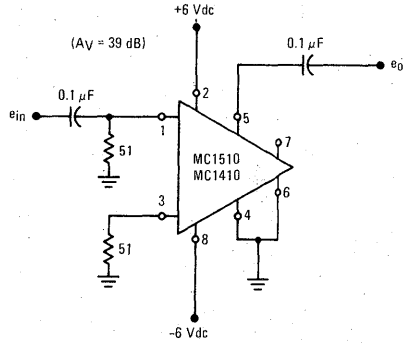
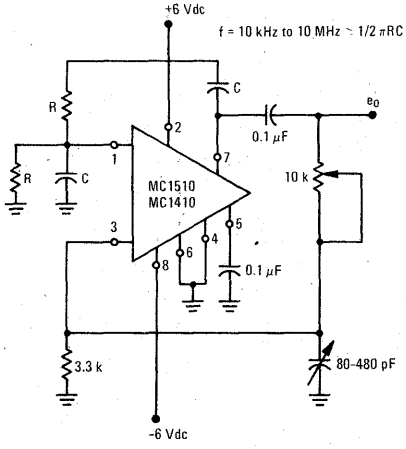


FIGURE 13
WEIN BRIDGE OSCILLATOR



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MC1422

Specifications and Applications Information

MONOLITHIC TIMING CIRCUIT WITH EXTERNALLY ADJUSTABLE THRESHOLD LEVEL

The MC1422 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Useable as a Differential Comparator Timer
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output

TYPICAL APPLICATIONS

- Time Delay Generation
- Precision Timing
- Missing Pulse Detection
- Sequential Timing
- Pulse Generation
- Pulse Width Modulation
- Linear Sweep Generation
- Pulse Shaping
- Pulse Position Modulation

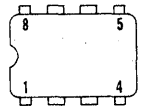
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+16	Vdc
Discharge Current (Pin 7)	I_7	200	mA
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Plastic Dual In-Line Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Temperature Range (Ambient)	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

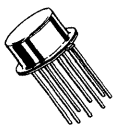
TIMING CIRCUIT WITH ADJUSTABLE THRESHOLD

MONOLITHIC SILICON INTEGRATED CIRCUIT

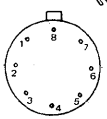
P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(Top View)



1. Ground
2. Trigger
3. Output
4. Reset
5. Variable Threshold Reference
6. Threshold
7. Discharge
8. V_{CC}



G SUFFIX
METAL PACKAGE
CASE 601
TO-99



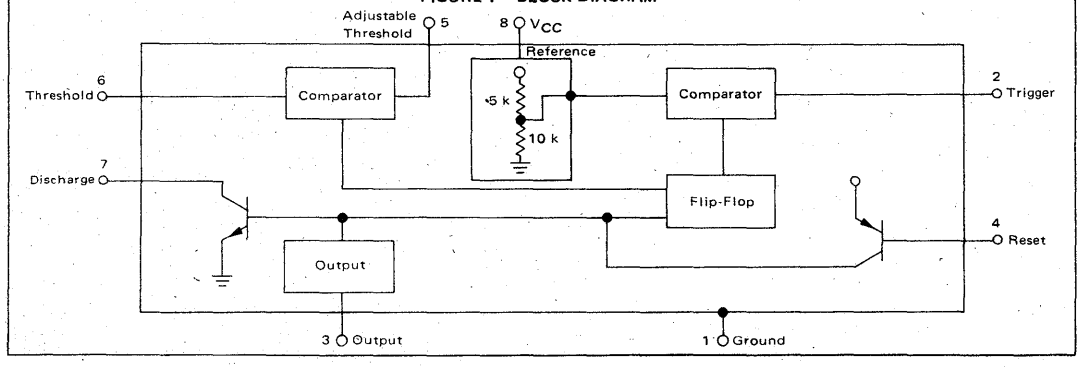
(Top View)

1. Ground
2. Trigger
3. Output
4. Reset
5. Variable Threshold Reference
6. Threshold
7. Discharge
8. V_{CC}

ORDERING INFORMATION

Type	Temperature Range	Package
MC1422G	0 to +70°C	Metal Can
MCC1422P1	0 to +70°C	Plastic DIP

FIGURE 1 – BLOCK DIAGRAM



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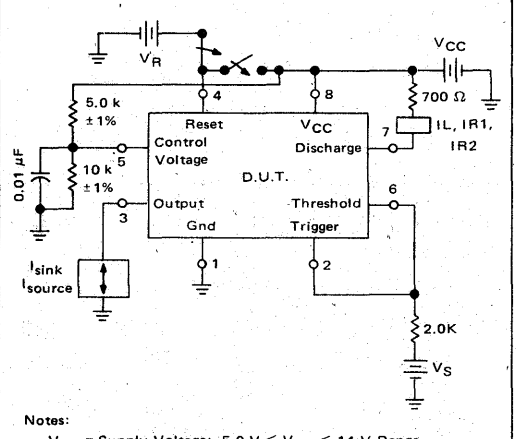
ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +14 V unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	–	14	V
Supply Current	I_D				mA
V_{CC} = 5.0 V, R_L = ∞		–	3.0	6.0	
V_{CC} = 14 V, R_L = ∞		–	10	15	
Low State (Note 1)					
Timing Error (Note 2)					
R_A, R_B = 1.0 kΩ to 100 kΩ					
Initial Accuracy C = 0.1 μF		–	1.0	–	%
Drift with Temperature		–	50	–	PPM/°C
Drift with Supply Voltage		–	0.01	–	%/Volt
Threshold Voltage (Figure 2)	V_{th}	–	2/3	–	xV_{CC}
Trigger Voltage	V_T				V
V_{CC} = 14 V		–	5.0	–	
V_{CC} = 5.0 V		–	1.67	–	
Trigger Current	I_T	–	0.5	–	μA
Discharge Leakage Current	I_{dis}	–	–	250	nA
Reset Current	I_R	–	0.1	–	mA
Threshold Current (Note 3)	I_{th}	–	–	1.0	μA
Output Voltage Low	V_{OL}				V
(V_{CC} = 14 V)					
I_{sink} = 10 mA		–	0.1	0.35	
I_{sink} = 50 mA		–	0.4	1.0	
I_{sink} = 100 mA		–	2.0	3.5	
I_{sink} = 200 mA		–	2.5	–	
Output Voltage High	V_{OH}				V
(I_{source} = 25 mA)					
V_{CC} = 14 V		12.75	13.3	–	
V_{CC} = 5.0 V		2.75	3.3	–	
Rise Time of Output	t_{OLH}	–	100	–	ns
Fall Time of Output	t_{OHL}	–	100	–	ns

NOTES:

1. Supply current when output is high is typically 1.0 mA less.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 14 V.
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 megohms.

FIGURE 2 – DC TEST CIRCUIT



Notes:

V_{CC} = Supply Voltage: 5.0 V ≤ V_{CC} ≤ 14 V Range

V_S = Switching Voltage: 1.4 V ≤ V_S ≤ 11.0 V Range

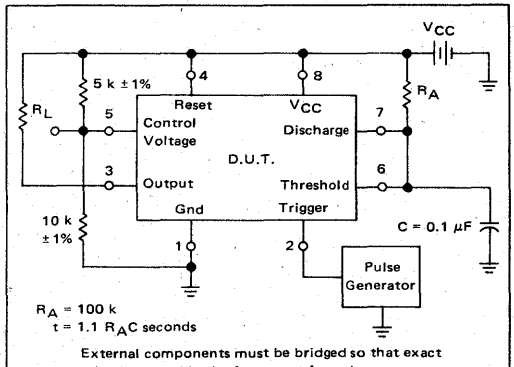
When V_S ≥ 2/3 V_{CC}, V_O is low ≅ 0 at R_L = ∞

When V_S ≤ 1/3 V_{CC}, V_O is high ≅ V_{CC} at R_L = ∞

V_R = Reset Voltage: V_R = 0.4 V or 1.0 V during Reset Test

During other tests, Pin 4 tied to V_{CC}.

FIGURE 3 – AC TEST CIRCUIT



R_A = 100 k

t = 1.1 R_AC seconds

External components must be bridged so that exact values are used in the frequency formula.

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TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 4 – TRIGGER PULSE WIDTH

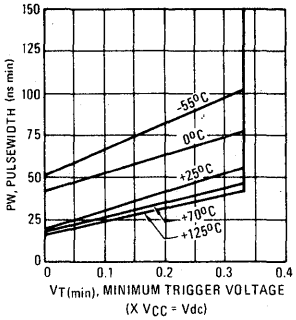

FIGURE 5 – SUPPLY CURRENT

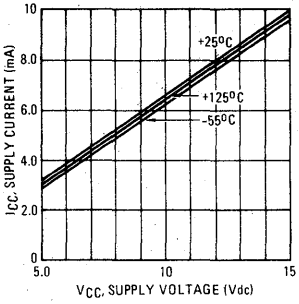

FIGURE 6 – HIGH OUTPUT VOLTAGE

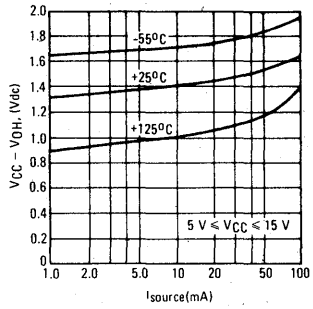

FIGURE 7 – LOW OUTPUT VOLTAGE @ V_{CC} = 5.0 Vdc

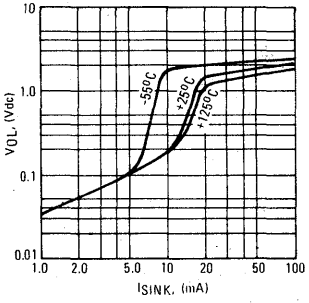

FIGURE 8 – LOW OUTPUT VOLTAGE @ V_{CC} = 10 Vdc

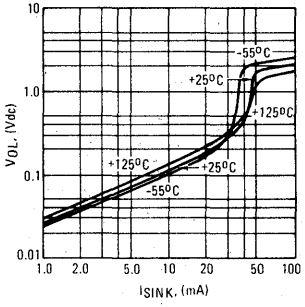

FIGURE 9 – LOW OUTPUT VOLTAGE @ V_{CC} = 15 Vdc

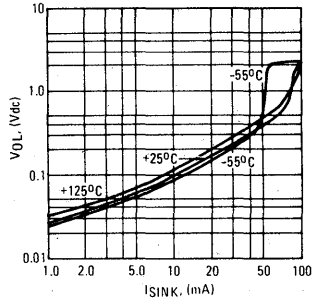

FIGURE 10 – DELAY TIME *versus* SUPPLY VOLTAGE

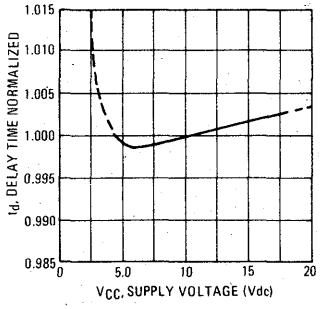

FIGURE 11 – DELAY TIME *versus* TEMPERATURE

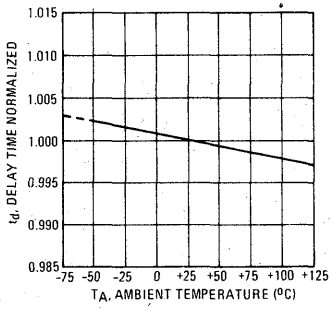

FIGURE 12 – PROPAGATION DELAY *versus* TRIGGER VOLTAGE

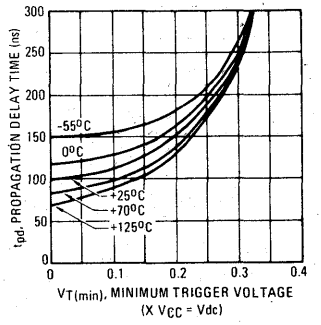

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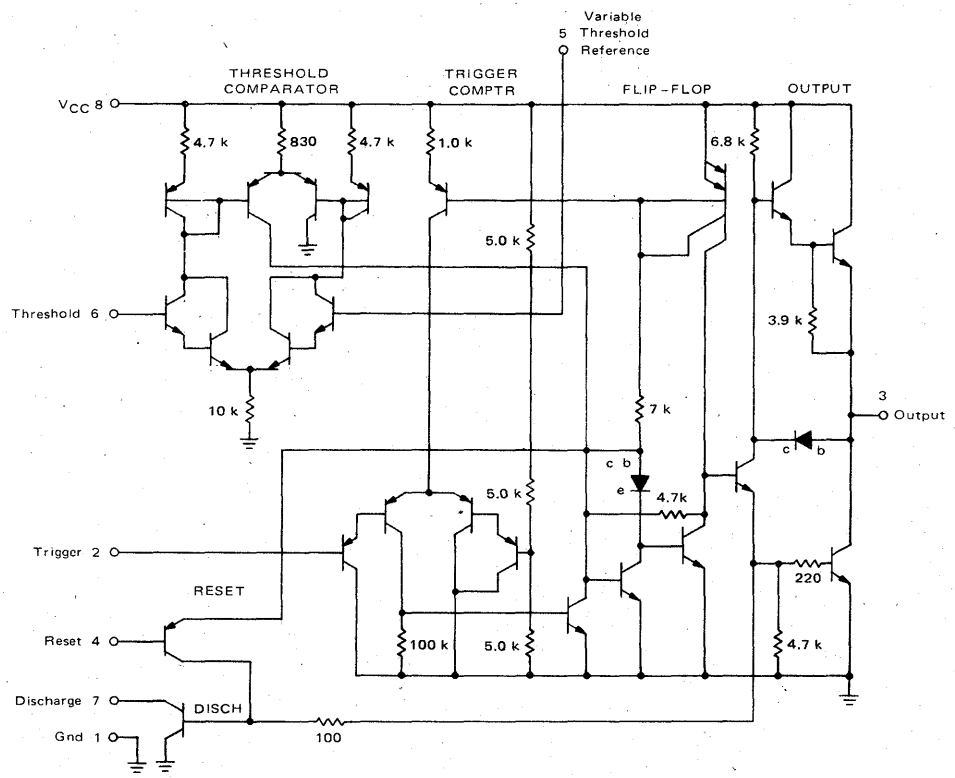
FIGURE 13 – CIRCUIT SCHEMATIC CONTROL VOLTAGE



GENERAL INFORMATION

The MC1422 is a monolithic timing circuit similar in performance and function to the MC1455 timer. It can be used in both the astable and monostable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are offered. The reference voltage of the trigger comparator is a fixed ratio of the supply voltage while the reference voltage of the threshold comparator is completely adjustable.

The MC1422 offers a completely independent variable threshold terminal. This feature allows it to be used as a modulation terminal as well as a synchronization terminal giving an additional degree of freedom in circuit design. The reference voltage pin (pin 5) for the threshold comparator is completely adjustable.

A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain low. The reset pin should be tied to the supply voltage when not in use.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below 1/3 V_{CC} the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches the external reference voltage the threshold comparator resets the flip-flop. This discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A C$. Various combinations of R and C and their associated times are shown in Figure 15. The trigger pulse width must be less than the timing period.

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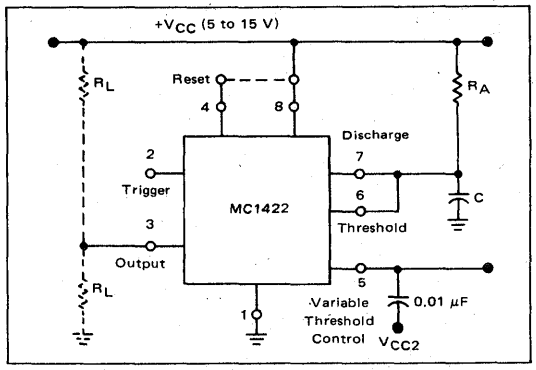
FIGURE 14 – MONOSTABLE CIRCUIT



APPLICATIONS INFORMATION

In general, the MC1422 can be used in any application where the MC1455/NE555 is currently being used as long as an external reference is supplied. (Refer to MC1455 data sheet for these applications.) The applications listed below are unique to the MC1422 and its design.

Zero Crossing Cycler

This circuit (see Figure 15) is most useful where it is necessary to cycle a thyristor at some frequency and duty cycle at line zero crossing only. This cycling at zero crossing only will reduce EMI, and current surges if capacitive loads are used.

Circuit Description

In order to have exact zero crossing cycling a phase shift network (R3)(C2) is used. Diodes C_{R1} and C_{R2} limit the line voltage to V- and V+. This limited line voltage, which appears somewhat like a square wave, is used as a sync pulse when differentiated by C1 and attenuated to 1/3 by R1 and R2. Cycle time is dependent on R4 and C3. The duty cycle is set by potentiometer R4.

It should be noted that this zero crossing cycler is intended for low frequency cycling, much lower than the line frequency used.

$$T_{cycle} = 0.69\ (R4)(C3) \text{ or } f_{cycle} = \frac{1.44}{(R4)(C3)}$$

FIGURE 15 – ZERO CROSSING CYCLER

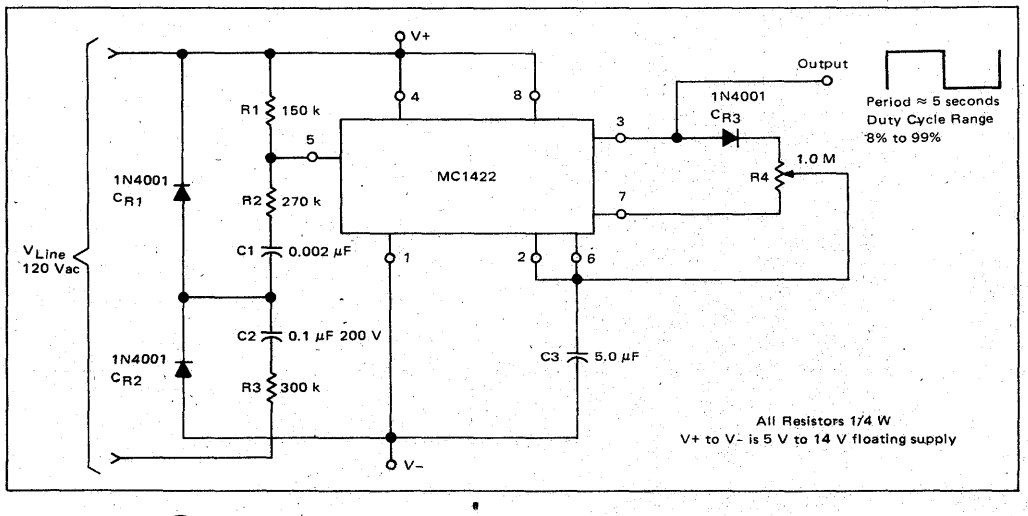


FIGURE 16 – PULSE WIDTH MODULATOR

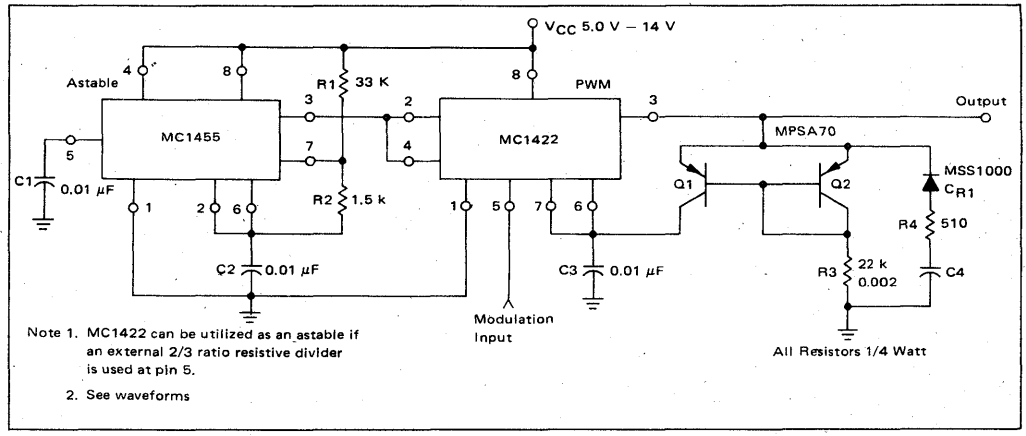
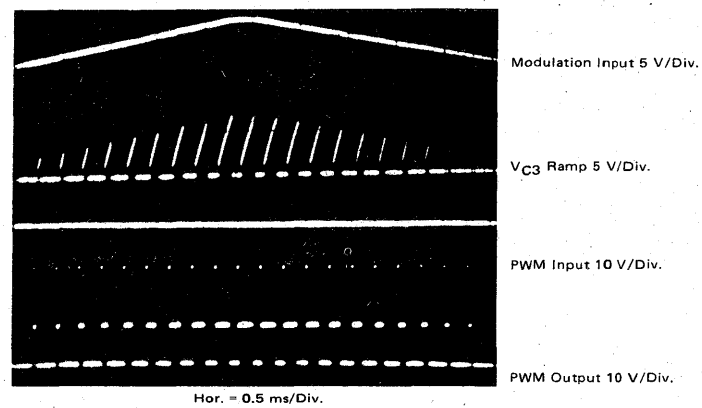


FIGURE 17 – PULSE WIDTH MODULATOR WAVEFORMS



Pulse Width Modulator

The MC1422 is used as a pulse width modulator (PWM) with the MC1455 being utilized as an astable. The MC1422 can be used as an astable in place of the MC1455 if an external reference of approximately 2/3 V_{CC} is used at Pin 5.

The transistors Q1 and Q2 are configured as a current mirror to provide a linear voltage ramp across C3. This constant current scheme attributes a relatively linear transfer characteristic for the pulse width modulator.

Several considerations must be made when using this circuit.

1. The minimum duty cycle out is limited to the complement of the input signal. (i.e., a 95% duty cycle astable driving the PWM will give a minimum duty cycle output of ≃ 5%.)

   The maximum duty cycle out will also be limited to the maximum duty cycle in.

2. For the astable frequency:

$$f = 1/T = \frac{1.44}{(R_1 + 2R_2)C}$$

3. Duty cycle (D.C.) for the astable:

$$DC = \frac{R_2}{R_1 + 2R_2}$$

For best results the charge time of C3 in the pulse width modulator should be equal to the period of the astable.

$$\frac{I_{Q1}}{C3\,(V_{CC} - 1)} = f_{in} = \frac{1}{T_{C3}} \quad I_{Q1} \simeq I_{Q2} = \frac{V_{CC} - V_{BE}}{R3}$$

V_{CC} = 10 V linearity typically 3% modulation input from 2 volts to 8 volts.

8

Voltage Controlled Oscillator

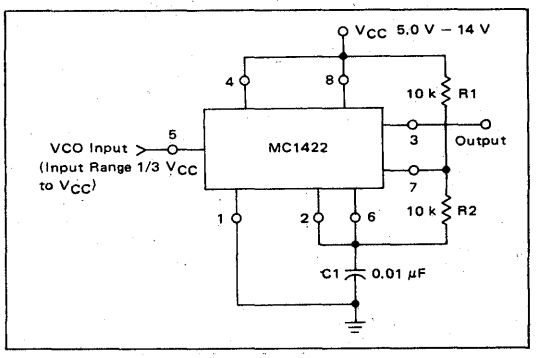
The VCO circuit, which has a nonlinear transfer characteristic will operate satisfactorily up to 200 kHz. The VCO input range is effective from 1/3 V_{CC} to V_{CC} - 2 V, with the highest control voltage producing the lowest output frequency. The equation for the frequency is:

$$f_{out} \simeq \frac{1}{\ln\left(1-\frac{V5-1/3\,V_{CC}}{2/3\,V_{CC}}\right)(R1+R2)C1+\ln\left(\frac{V5-1/3\,V_{CC}}{V5}\right)R2C1}$$

V5 = VCO input control voltage

It should be noted that, the output duty cycle will vary somewhat over the VCO input control range.

FIGURE 18 – VOLTAGE CONTROLLED OSCILLATOR



Comparator with Time Out

The MC1422 is used as a comparator with the capability of a timing output pulse when the inverting input (Pin 6) is ⩾ the non-inverting input (Pin 5). The frequency of the pulses for the values of R2 and C1 as shown in Figure 19 is approximately 2.0 Hz, and the pulse width 0.3 ms, f_p = frequency of pulses while Pin 6 voltage is above voltage at Pin 5.

The function of R1 is to limit di/dt, when charging C1.

$$f_p \simeq \frac{1}{R2C1} \text{ or } T_p \simeq R2C1 \ .$$

FIGURE 19

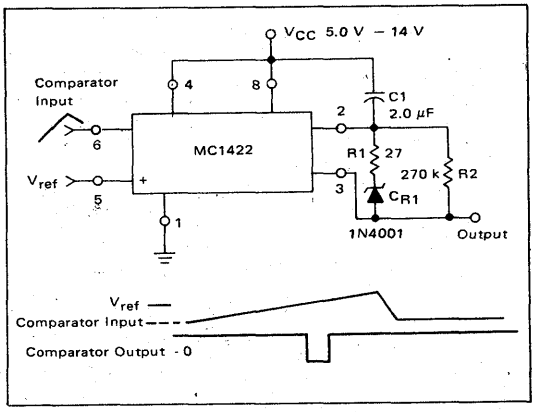
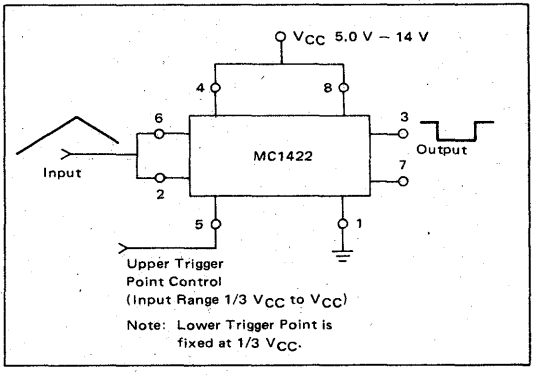


FIGURE 20



Schmitt Trigger

The MC1422 is very useful as a Schmitt Trigger as shown in Figure 20. The lower trigger point is fixed at 1/3 V_{CC}, but the upper trigger point is adjustable by means of Pin 5 from 1/3 V_{CC} to slightly less than V_{CC}. The Schmitt trigger will operate with input frequencies up to 50 kHz.

8

ORDERING INFORMATION

Device	Temperature Range	Package
MC1438R	0°C to +70°C	Metal Power
MC1538R	−55°C to +125°C	Metal Power

MC1438R
MC1538R

POWER BOOSTER

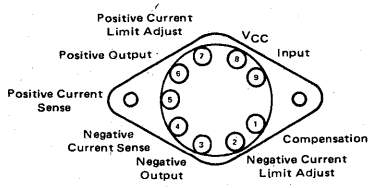
The MC1538/MC1438 is designed as a high current gain amplifier (70 dB), with unity voltage gain that can deliver load currents up to ±300 mAdc. This device is ideally suited to follow an operational amplifier (such as MC1556/MC1456) for driving low impedance loads and improving the overall circuit performance.

- High Input Impedance — 0.4 Meg-Ohm typ — when driving the MC1538/MC1438, the gain of an operational amplifier will approach the unloaded open-loop gain. Internal power dissipation of the operational amplifier will be independent of output voltage and therefore thermal drift will be reduced.
- Large Power Bandwidth — 1.5 MHz typ — considerably better than present operational amplifiers. Bandwidth and slew rate will be limited by the operational amplifier, not the MC1538/MC1438.
- Low Output Impedance — 10 Ohms typ — allows the MC1538/MC1438 to drive a capacitive load with greatly reduced phase shift compared with an operational amplifier. Output voltage swing capability is much increased when driving small load impedances.
- Adjustable Current Limit — ±5.0 mAdc to ±300 mAdc
- Excellent Power-Supply Rejection — 1.0 mV/V typ
- Current Gain — 3000 typ

OPERATIONAL AMPLIFIERS POWER BOOSTER

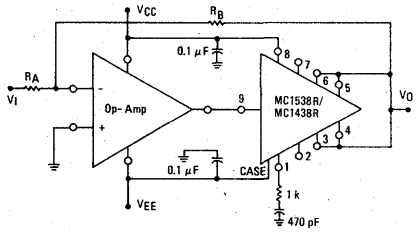
SILICON MONOLITHIC INTEGRATED CIRCUIT

R SUFFIX
CASE 614

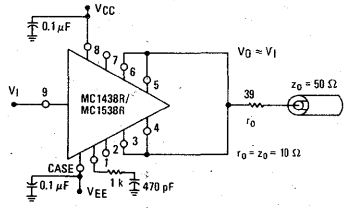


TYPICAL APPLICATIONS

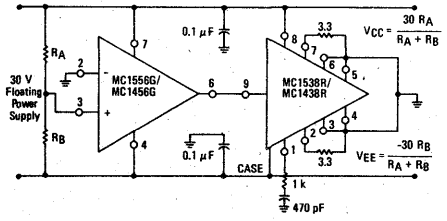
OPERATIONAL AMPLIFIER BOOST CIRCUIT



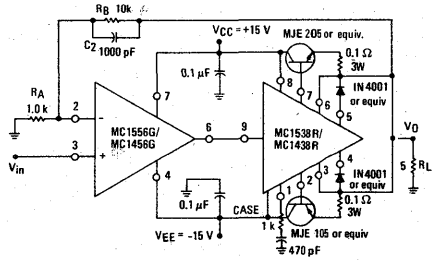
DIGITAL OR ANALOG LINE DRIVER



POWER SUPPLY SPLITTER



SERVO/POWER AMPLIFIER



Under some conditions of circuit layout and loading, the MC1538R/MC1438R will oscillate when driven into current limiting. Oscillation during positive current limiting can usually be suppressed by placing a 0.02 μF capacitor between Pins 7 and 5. Oscillations during negative current limit can usually be suppressed by placing a 0.02 μF capacitor between Pins 1 and 2. 100 Ohms in series with this capacitor will reduce any cross-over distortion occurring when driving extremely low impedance loads.

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MAXIMUM RATINGS (T_C = +25°C unless otherwise noted.)

Rating	Symbol	MC1538R	MC1438R	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 -22	+18 -18	Vdc
Input Voltage Swing	$\|V_{in}\|$	V_{CC} or V_{EE}		Vdc
Load Current	I_L	350		mAdc
Power Dissipation @ T_A = +25°C Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	3.0 24		Watts mW/°C
Power Dissipation @ T_C = +25°C Derate above T_C = +25°C	P_D $1/R_{\theta JC}$	17.5 140		Watts mW/°C
Operating Ambient Temperature Range MC1438R MC1538R	T_A	0 to + 70 -55 to +125		°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	41.6	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	7.15	°C/W

ELECTRICAL CHARACTERISTICS

(R_L = 300 ohms, T_C = +25°C unless otherwise noted.)

				MC1538R 5.0 V ≤ V_{CC} = $\|V_{EE}\|$ ≤ 20 V			MC1438R V_{CC} = +15 V, V_{EE} = -15 V			
Characteristic (Linear Operation)	**Fig**	**Note**	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Voltage Gain (f = 1.0 kHz)	1	–	A_V	0.9	0.95	1.0	0.85	0.95	1.0	V/V
Current Gain ($A_I = \Delta I_O/\Delta I_I$)	1	–	A_I	–	3000	–	–	3000	–	A/A
Output Impedance (f = 1.0 kHz)	1	–	z_o	–	10	–	–	10	–	Ohms
Input Impedance (f = 1.0 kHz)	1	–	z_i	–	400	–	–	400	–	k ohms
Output Voltage Swing (See Note 3)	1	3	V_O	±12	±13	–	±11	±12	–	Vdc
Input Bias Current	2	–	I_{IB}	–	60	200	–	60	300	μAdc
Output Offset Voltage	2	1	V_{OO}	–	25	150	–	25	200	mVdc
Small Signal Bandwidth (R_L = 300 ohms) (V_I = 0 Vdc, V_I = 100 mV[rms])	1	–	BW	–	8.0	–	–	8.0	–	MHz
Power Bandwidth (See Note 3) (V_O = 20 V_{p-p}, THD = 5%)	1	–	BW_P	–	1.5	–	–	1.5	–	MHz
Total Harmonic Distortion (Note 3) (f = 1.0 kHz, V_O = 20 V_{p-p})	1	–	THD	–	0.5	–	–	0.5	–	%
Output Short-Circuit Current (R1 = R2 = ∞) (R1 = R2 = 3.3. ohms) Adjustable Range	 3 3 4,5	 2	I_{OS}	 75 – –	 95 300 5.0 to 300	 125 – –	 65 – –	 95 300 5.0 to 300	 140 – –	mAdc
Power Supply Sensitivity (V_{EE} constant) (V_{CC} constant)	2	–	PSRR	 – –	 1.0 1.0	 – –	 – –	 1.0 1.0	 – –	mV/V
Power Supply Current (R_L ∞, V_I = 0)	2	–	I_{CC} I_{EE}	4.5	6.0	10	2.5	6.0	15	mAdc
Power Dissipation (See Note 3) (R_L ∞, V_I = 0)	2	3	P_C	150	180	300	75	180	450	mW

Note 1. Output offset Voltage is the quiescent dc output voltage with the input grounded.

Note 2. Short-Circuit Current, I_{SC}, is adjustable by varying R1, R2, R3 and R4. The positive current limit is set by R1 or R3, and the negative current limit is set by R2 or R4. See Figures 4 and 5 for curves of short-circuit current versus R1, R2, R3 and R4.

Note 3. V_{CC} = +15 V, V_{EE} = -15 V.

TEST CIRCUITS

FIGURE 1

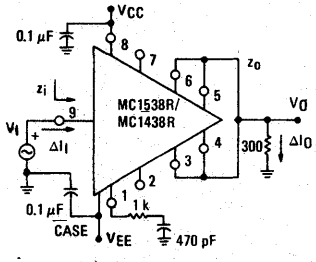


FIGURE 2

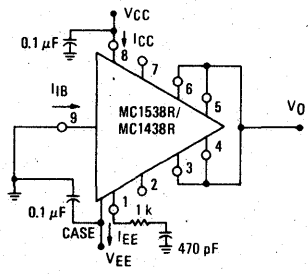
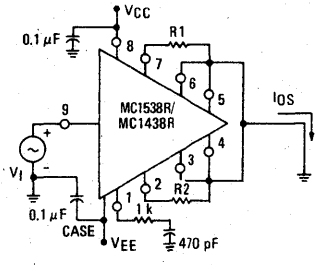
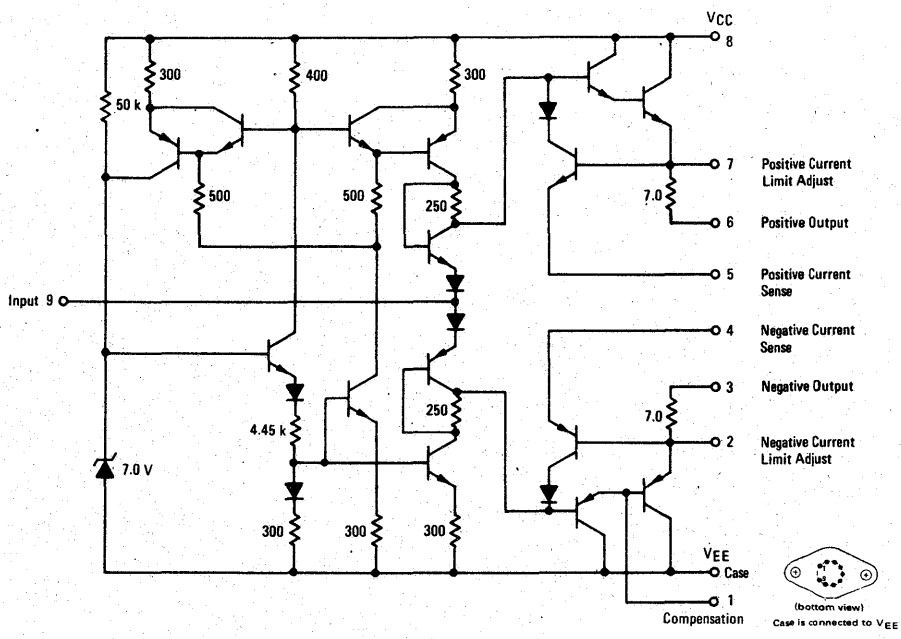


FIGURE 3



CIRCUIT SCHEMATIC



TYPICAL CHARACTERISTICS

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 4 – SHORT-CIRCUIT CURRENT versus R1 OR R2 (100 mA to 300 mA)

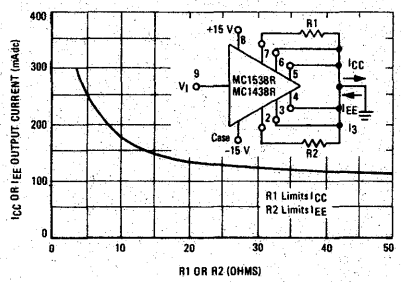
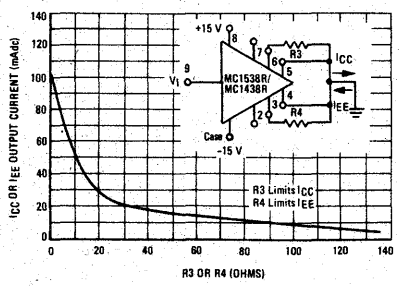


FIGURE 5 – SHORT-CIRCUIT CURRENT versus R3 OR R4 (5.0 mA to 100 mA)



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TYPICAL CHARACTERISTICS (continued)

FIGURE 6 – POWER SUPPLY CURRENT versus SHUNT RESISTANCE

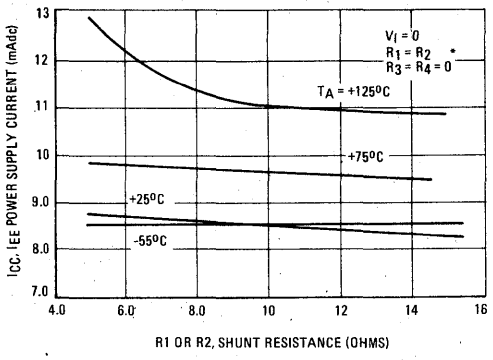


FIGURE 7 – SMALL SIGNAL GAIN AND PHASE RESPONSE

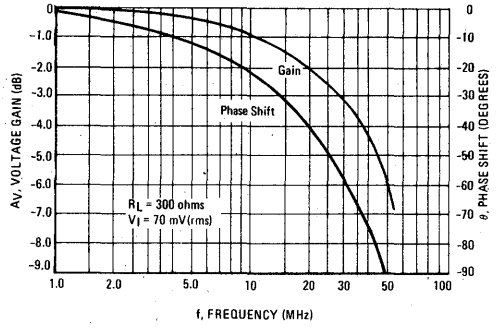


FIGURE 8 – POSITIVE OUTPUT VOLTAGE SWING versus LOAD CURRENT

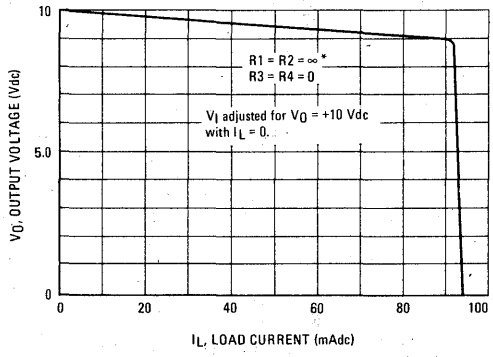


FIGURE 9 – NEGATIVE OUTPUT VOLTAGE SWING versus LOAD CURRENT

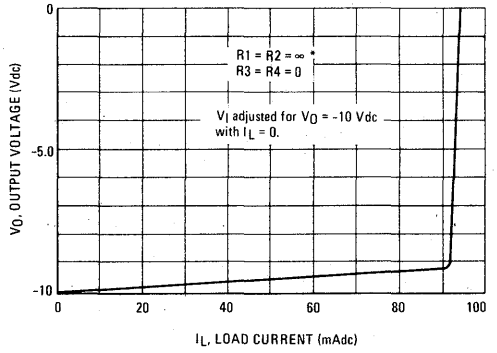


FIGURE 10 – OUTPUT OFFSET VOLTAGE versus TEMPERATURE

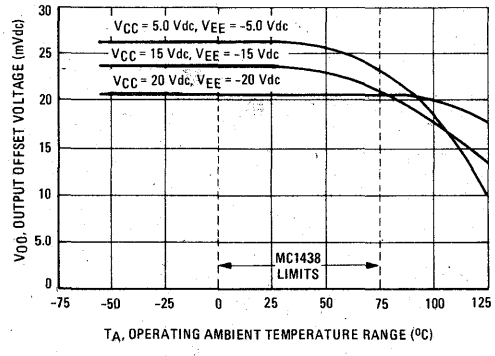
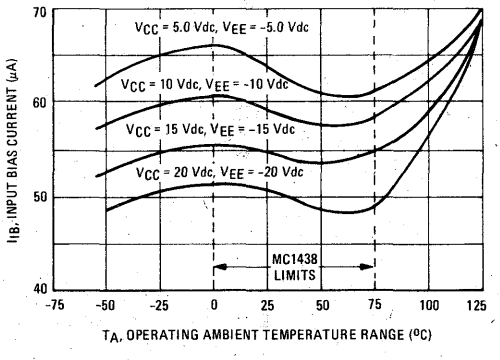


FIGURE 11 – INPUT BIAS CURRENT versus TEMPERATURE



*See figures 4 and 5 for definition of R1, R2,R3, and R4.

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +15 Vdc, V_{EE} = -15 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 12 – PULSE RESPONSE CHARACTERISTICS

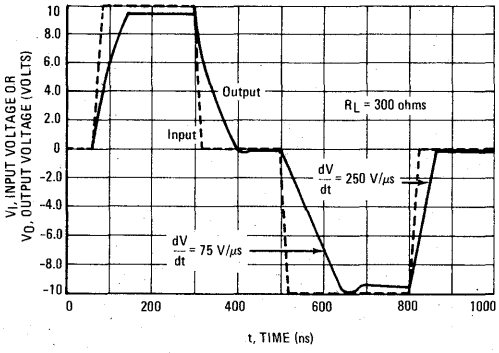
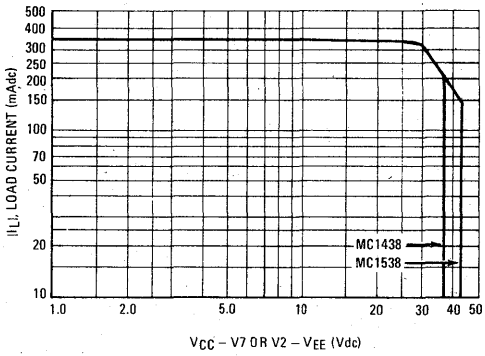


FIGURE 13 – DC SAFE OPERATING AREA



TYPICAL APPLICATIONS

FIGURE 14 – NON-INVERTING AC POWER AMPLIFIER

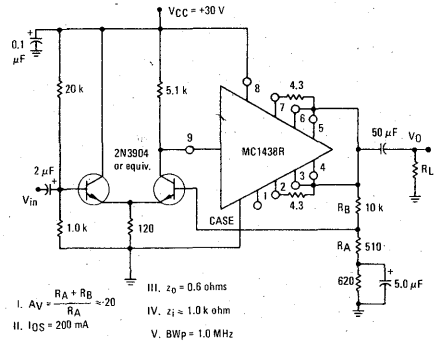


FIGURE 15 – NON-INVERTING POWER AMPLIFIER

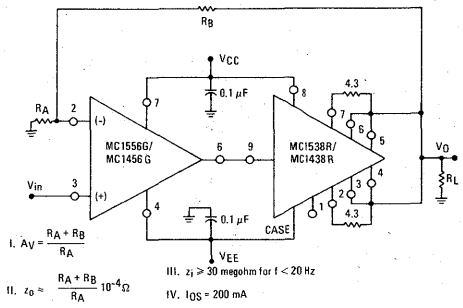


FIGURE 16 – NON-INVERTING VOLTAGE FOLLOWER

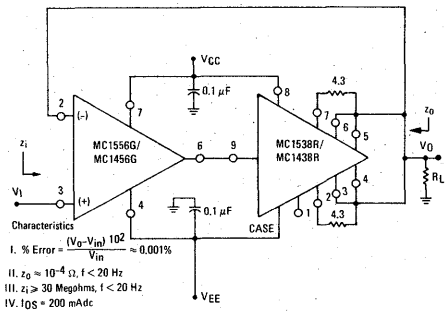
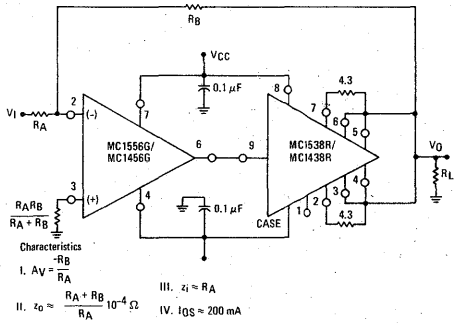


FIGURE 17 – INVERTING POWER AMPLIFIER



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TYPICAL APPLICATIONS (continued)

FIGURE 18 – PROGRAMMABLE VOLTAGE SOURCE

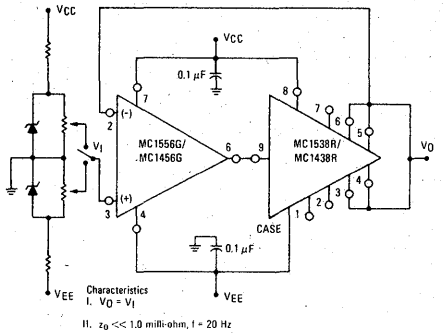


FIGURE 19 – CONSTANT CURRENT SOURCE OR TRANSCONDUCTANCE AMPLIFIER

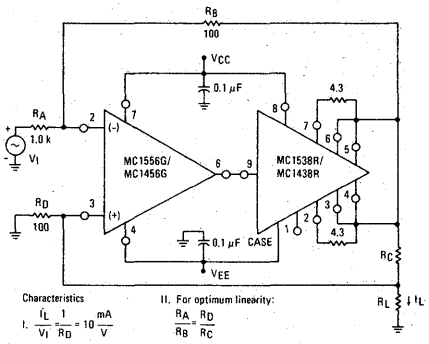


FIGURE 20 – SIGNAL DISTRIBUTION

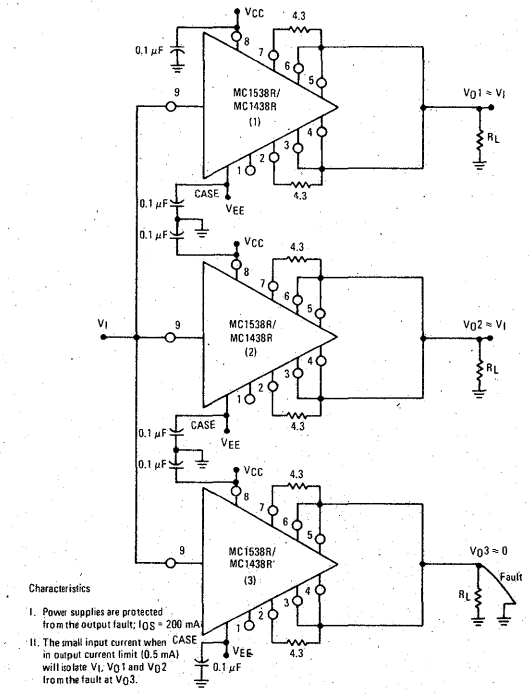


FIGURE 21 – ASTABLE MULTIVIBRATOR

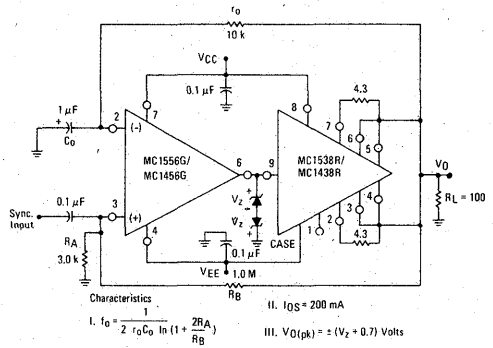
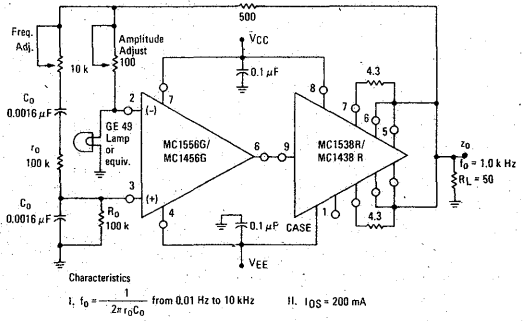


FIGURE 22 – WIEN BRIDGE OSCILLATOR



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ORDERING INFORMATION

Device	Temperature Range	Package
MC1445F	0°C to +75°C	Ceramic Flat
MC1445G	0°C to +75°C	Metal Can
MC1445L	0°C to +75°C	Ceramic DIP
MC1545F	−55°C to +125°C	Ceramic Flat
MC1545G	−55°C to +125°C	Metal Can
MC1545L	−55°C to +125°C	Ceramic DIP

MC1445
MC1545

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

. . . designed for use as a general-purpose gated wideband-amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier. See Application Notes AN475 and AN491 for design details.

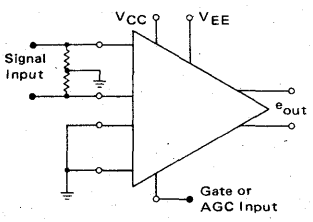
- Large Bandwidth; 50 MHz typical
- Channel-Select Time of 20 ns typical
- Differential Inputs and Differential Output

GATE CONTROLLED TWO-CHANNEL-INPUT WIDEBAND AMPLIFIER

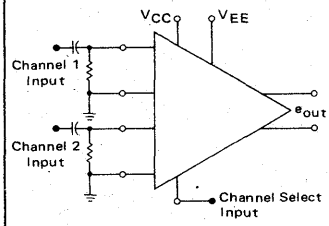
SILICON MONOLITHIC INTEGRATED CIRCUIT

TYPICAL APPLICATIONS

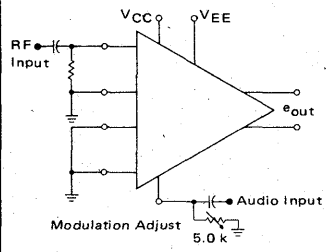
VIDEO SWITCH OR DIFFERENTIAL AMPLIFIER WITH AGC



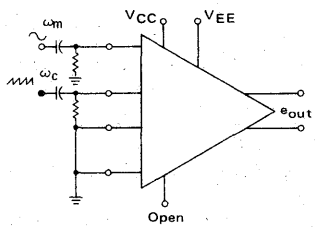
MULTIPLEX OR FSK



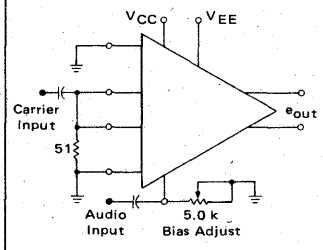
AMPLITUDE MODULATOR



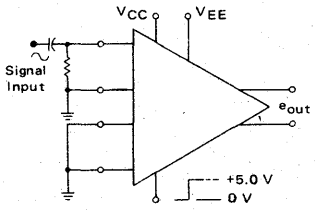
PULSE-WIDTH MODULATOR

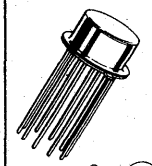


BALANCED MODULATOR

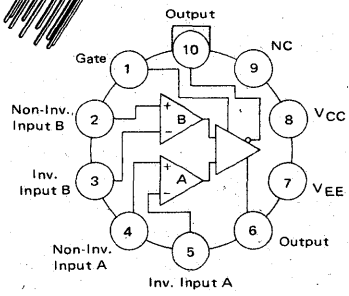


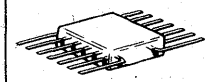
ANALOG SWITCH



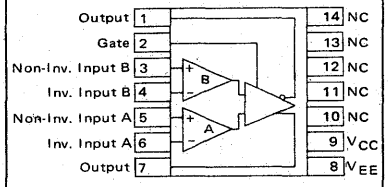


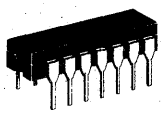
G SUFFIX
METAL PACKAGE
CASE 602A



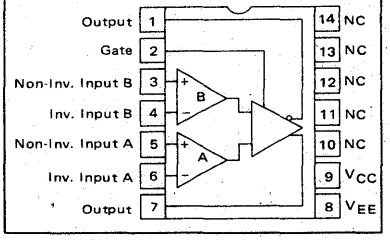


F SUFFIX
CERAMIC PACKAGE
CASE 607





L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116



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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+12 -12	Vdc Vdc
Input Differential Voltage Range	V_{IDR}	±5.0	Volts
Load Current	I_L	25	mA
Power Dissipation (Package Limitation) Flat Package Derate above T_A = +25°C Ceramic Dual In-Line Package Derate above T_A = +25°C Metal Can Derate above T_A = +25°C	P_D	 500 3.3 625 5.0 680 4.6	 mW mW/°C mW mW/°C mW mW/°C
Operating Ambient Temperature Range MC1445 MC1545	T_A	0 to +75 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = 5.0 Vdc, at T_A = +25°C, specifications apply to both input channels unless otherwise noted.)

Characteristic	Fig. No.	Symbol	MC1545 Min	MC1545 Typ	MC1545 Max	MC1445 Min	MC1445 Typ	MC1445 Max	Unit
Single-Ended Voltage Gain	1,12	A_{vs}	16	19	21	16	19.5	23	dB
Bandwidth	1,12	BW	45	50	–	–	50	–	MHz
Input Impedance (f = 50 kHz)	5,14	z_i	4.0	10	–	3.0	10	–	k ohms
Output Impedance (f = 50 kHz)	6,15	z_o	–	25	–	–	25	–	Ohms
Output Differential Voltage Range (R_L = 1.0 k ohm, f = 50 kHz)	4,13	V_{ODR}	1.5	2.5	–	1.5	2.5	–	Vp-p
Input Bias Current	16	I_{IB}	–	15	25	–	15	30	μAdc
Input Offset Current	16	I_{IO}	–	2.0	–	–	2.0	–	μAdc
Input Offset Voltage	17	V_{IO}	–	1.0	5.0	–	–	7.5	mVdc
Quiescent Output dc Level	17	V_O	–	0.2	–	–	0.2	–	Vdc
Output dc Level Change (Gate Input Voltage Change: +5.0 V to 0 V)	17	ΔV_O	–	±15	–	–	±15	–	mV
Common-Mode Rejection Ratio (f = 50 kHz)	9,18	CMRR	–	85	–	–	85	–	dB
Input Common-Mode Voltage Range	18	V_{ICR}	–	±2.5	–	–	±2.5	–	Vp
Gate Characteristics Gate Input Voltage – Low Logic State (Note 1) Gate Input Voltage – High Logic State (Note 2)	8	$V_{IL(G)}$ $V_{IH(G)}$	0.45 –	0.70 1.5	– 2.2	0.2 –	0.4 1.3	– 3.0	Vdc
Gate Input Current – Low Logic State ($V_{IL(G)}$ = 0 V)	18	$I_{IL(G)}$	–	–	2.5	–	–	4.0	mA
Gate Input Current – High Logic State ($V_{IH(G)}$ = +5.0 V)	18	$I_{IH(G)}$	–	–	2.0	–	–	4.0	μA
Step Response (e_{in} = 20 mV)	19	t_{PLH} t_{PHL} t_{TLH} t_{THL}	– – – –	6.5 6.3 6.5 7.0	10 10 15 15	– – – –	6.5 6.3 6.5 7.0	– – – –	ns
Wideband Input Noise (5.0 Hz – 10 MHz, R_S = 50 ohms)	10,20	e_n	–	25	–	–	25	–	μV(rms)
DC Power Consumption	11,20	P_C	–	70	110	–	70	150	mW

Note 1. $V_{IL(G)}$ is the gate voltage which results in channel A gain of unity or less and channel B gain of 16 dB or greater.
Note 2. $V_{IH(G)}$ is the gate voltage which results in channel B gain of unity or less and channel A gain of 16 dB or greater.

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FIGURE 1 – SINGLE-ENDED VOLTAGE GAIN versus FREQUENCY

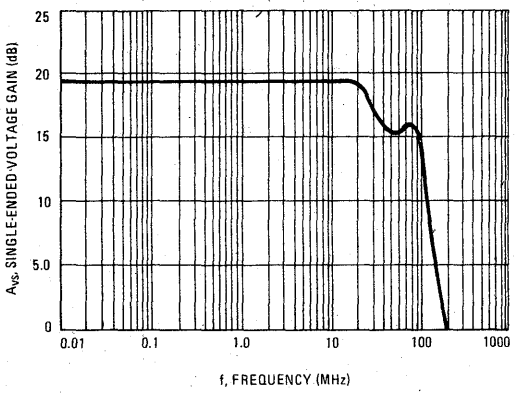

FIGURE 2 – SINGLE-ENDED VOLTAGE GAIN versus TEMPERATURE

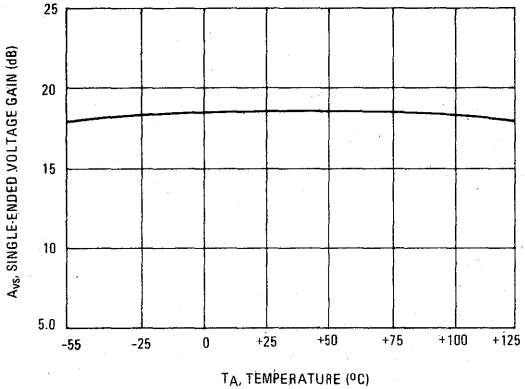

FIGURE 3 – VOLTAGE GAIN versus POWER SUPPLY VOLTAGES

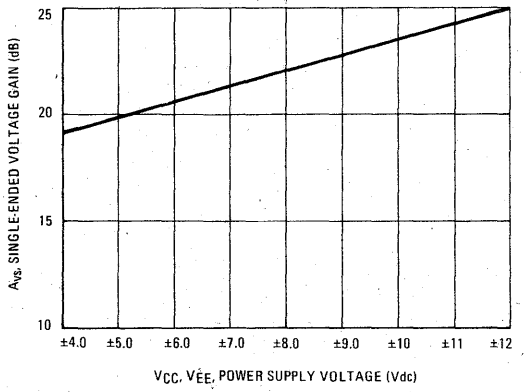

FIGURE 4 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

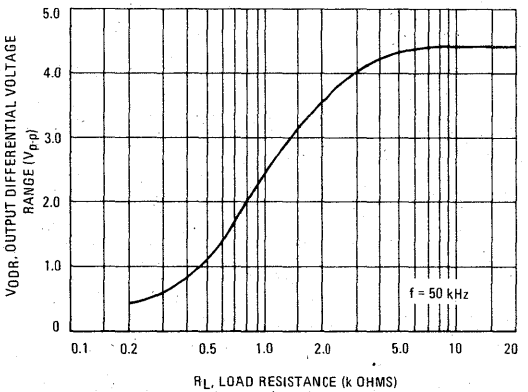

FIGURE 5 – INPUT C_P AND R_P versus FREQUENCY (BOTH CHANNELS)

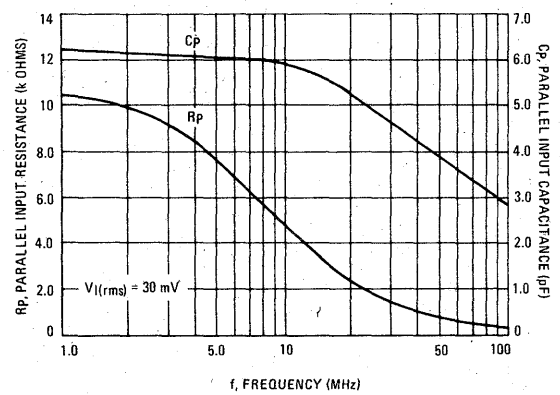

FIGURE 6 – OUTPUT IMPEDANCE versus FREQUENCY

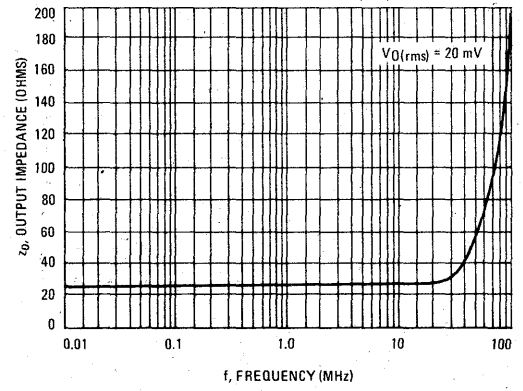

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FIGURE 7 – CHANNEL SEPARATION versus FREQUENCY

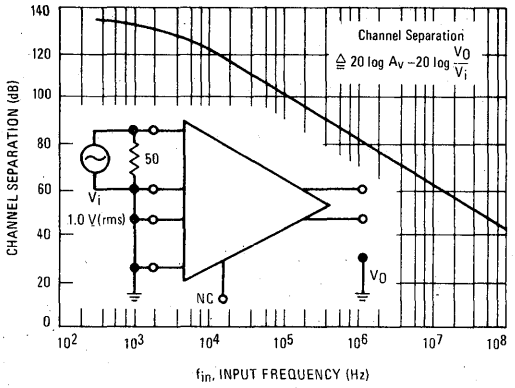

FIGURE 8 – GATE CHARACTERISTICS

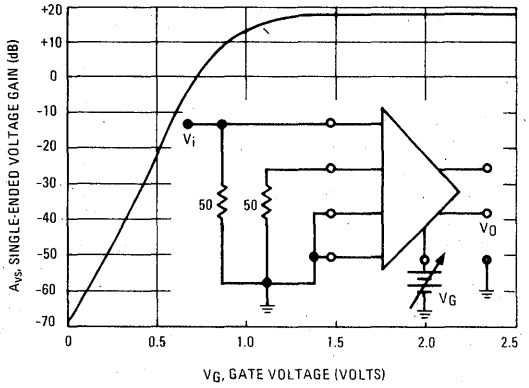

FIGURE 9 – COMMON MODE REJECTION RATIO versus FREQUENCY

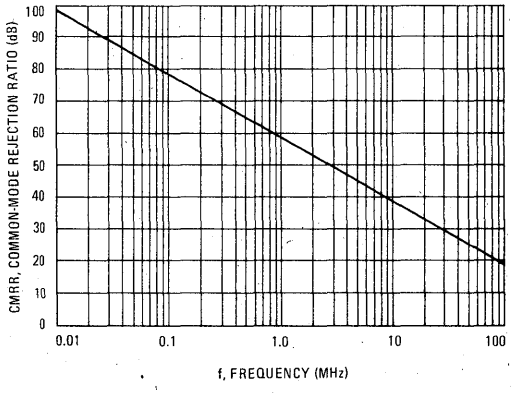

FIGURE 10 – INPUT WIDEBAND NOISE versus SOURCE RESISTANCE

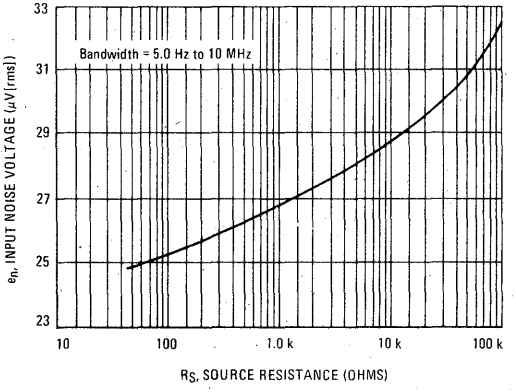

FIGURE 11 – CIRCUIT SCHEMATIC

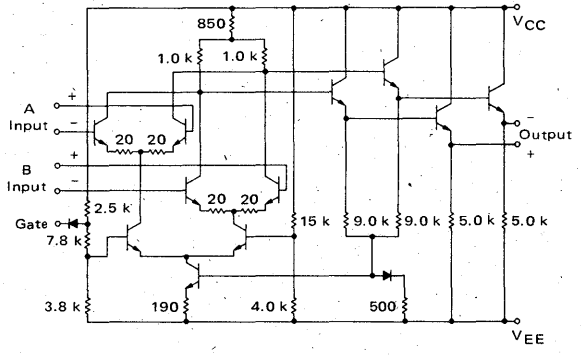

FIGURE 12 – SINGLE-ENDED VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT

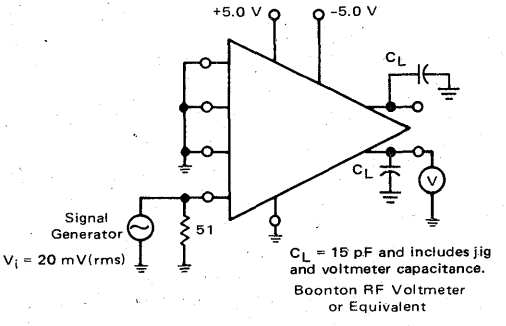

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FIGURE 13 – OUTPUT VOLTAGE SWING TEST CIRCUIT

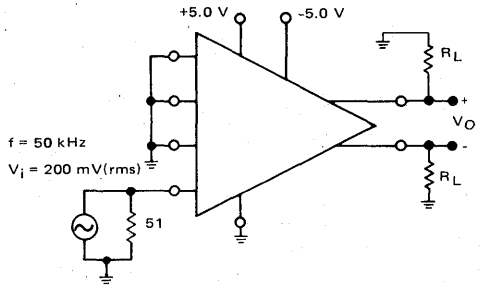

FIGURE 14 – INPUT IMPEDANCE TEST CIRCUIT

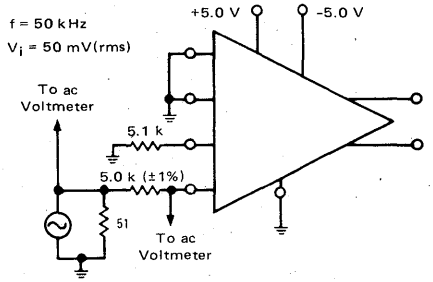

FIGURE 15 – OUTPUT IMPEDANCE TEST CIRCUIT

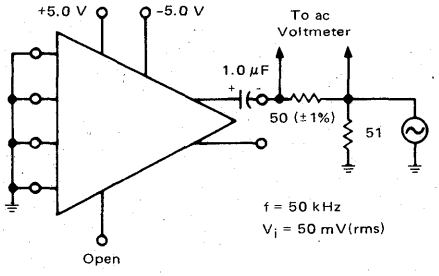

FIGURE 16 – INPUT BIAS CURRENT AND INPUT OFFSET CURRENT TEST CIRCUIT

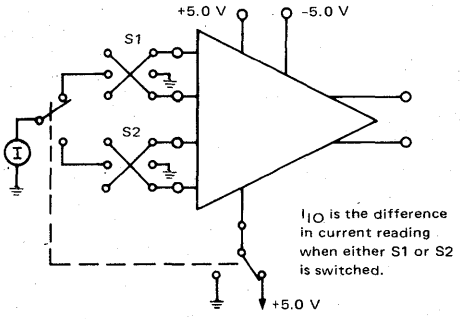

FIGURE 17 – INPUT OFFSET VOLTAGE AND QUIESCENT OUTPUT LEVEL TEST CIRCUIT

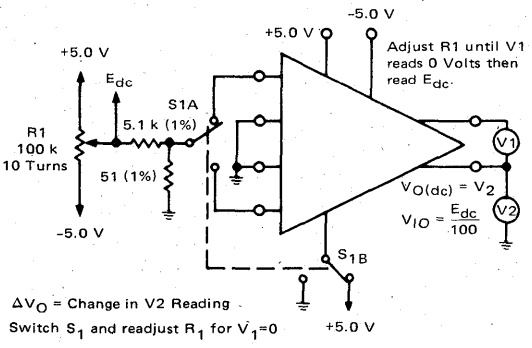

FIGURE 18 – GATE CURRENT (HIGH AND LOW), COMMON-MODE REJECTION AND COMMON-MODE INPUT RANGE TEST CIRCUIT

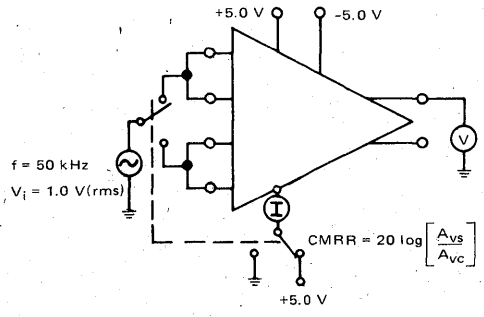

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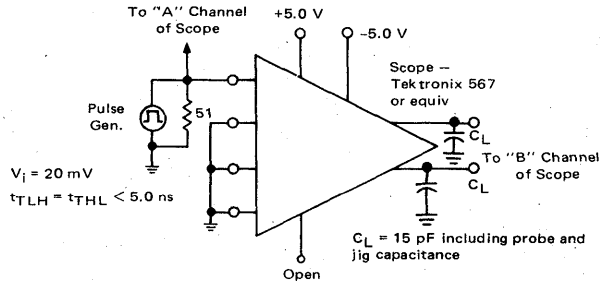
FIGURE 19 – PROPAGATION DELAY AND RISE AND FALL TIMES TEST CIRCUIT



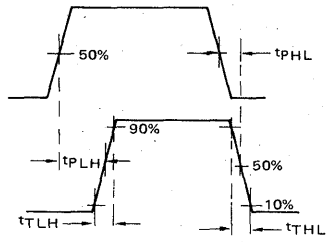


FIGURE 20 – POWER DISSIPATION AND WIDEBAND INPUT NOISE TEST CIRCUIT

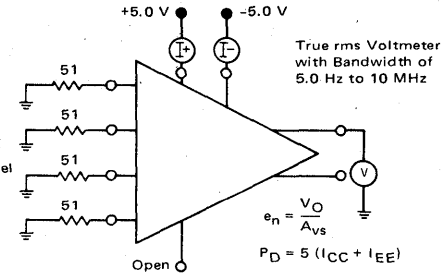
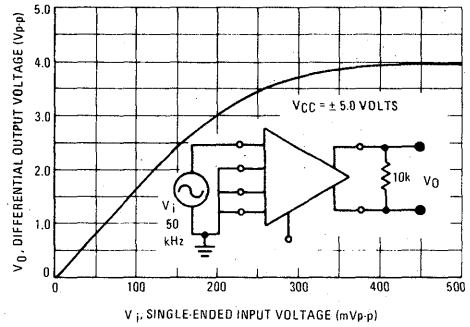


FIGURE 21 – LIMITING CHARACTERISTIC



8

ORDERING INFORMATION

Device	Temperature Range	Package
MC1550F	−55°C to +125°C	Ceramic Flat
MC1550G	−55°C to +125°C	Metal Can

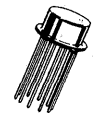
MC1550

RF – IF AMPLIFIER
SILICON MONOLITHIC
INTEGRATED CIRCUIT

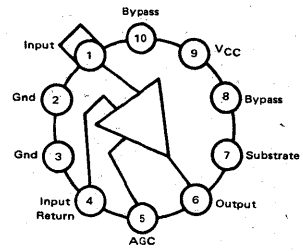
RF – IF AMPLIFIER

. . . a versatile, common-emitter, common-base cascode circuit for use in communications applications. See Application Note AN-215A for additional information.

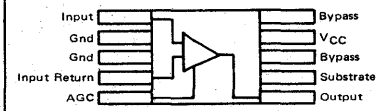
- Constant Input Impedance over entire AGC range
- Extremely Low y_{12} – 4.3 μmhos at 60 MHz
- High Power Gain – 30 dB @ 60 MHz (0.5 MHz BW)
- Good Noise Figure – 5 dB @ 60 MHz



G SUFFIX
METAL PACKAGE
CASE 603B



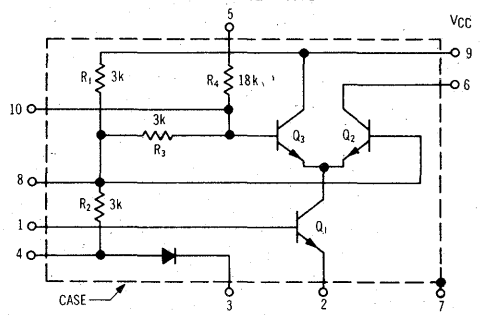
F SUFFIX
CERAMIC PACKAGE
CASE 606-04
TO-91



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 9	V_{CC}	20	Vdc
AGC Supply Voltage	V_{AGC}	20	Vdc
Input Differential Voltage, Pin 1 to Pin 4 (R_S = 500 ohms)	V_{ID}	±5.0	V(rms)
Power Dissipation (Package Limitation) Metal Can Derate above T_A = +25°C Flat Package Derate above T_A = +25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Ambient Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC1550 is built with monolithic fabrication techniques utilizing diffused resistors and small-geometry transistors. Excellent AGC performance is obtained by shunting the signal through the AGC transistor Q_3 maintaining the operating point of the input transistor Q_1. This keeps the input impedance constant over the entire AGC range.

The amplifier is intended to be used in a common-emitter, common-base configuration (Q_1 and Q_2) with Q_3 acting as an AGC transistor. The input signal is applied between pins 1 and 4, where pin 4 is ac-coupled to ground. DC source resistance between pins 1 and 4 should be small (less than 100 ohms). Pins 2 and 3 should be connected together and grounded. Pins 8 and 10 should be bypassed to ground. The positive supply voltage is applied at pin 9 and at higher frequencies, pin 9 should also be bypassed to ground. The output is taken between pins 6 and 9. The substrate is connected to pin 7 and should be grounded. AGC voltage is applied to pin 5.

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ELECTRICAL CHARACTERISTICS (V^+ = +6 Vdc, T_A = +25°C)

Characteristic	Conditions	Figure	Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS							
Output Voltage	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	V_O	3.80 5.90	– –	4.65 6.00	Vdc
Test Voltage	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	V8	2.85 3.25	– –	3.40 3.80	Vdc
Supply Drain Current	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	I_D	– –	– –	2.2 2.5	mAdc
AGC Supply Drain Current	V_{AGC} = 0 Vdc V_{AGC} = +6 Vdc	1	I_{AGC}	– –	– –	-0.2 0.18	mAdc
SMALL-SIGNAL CHARACTERISTICS							
Small-Signal Voltage Gain	f = 500 kHz	2	A_V	22	–	29	dB
Bandwidth	-3.0 dB	2	BW	22	–	–	MHz
Transducer Power Gain	f = 60 MHz, BW = 6 MHz f = 100 MHz, BW = 6 MHz	3	A_P	– –	25 21	– –	dB

TYPICAL CHARACTERISTICS

(V_{CC} = 6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 1 – DC CHARACTERISTICS TEST CIRCUIT

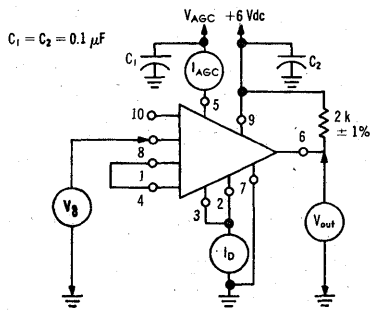


FIGURE 2 – VOLTAGE GAIN AND BANDWIDTH TEST CIRCUIT

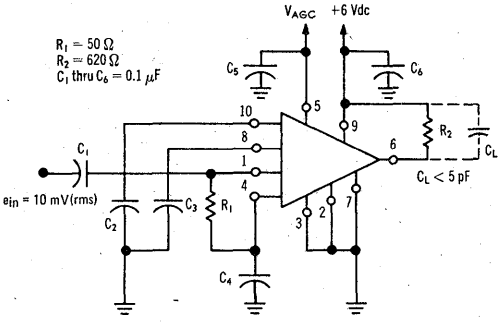


FIGURE 3 – POWER GAIN TEST CIRCUIT @ 60 MHz

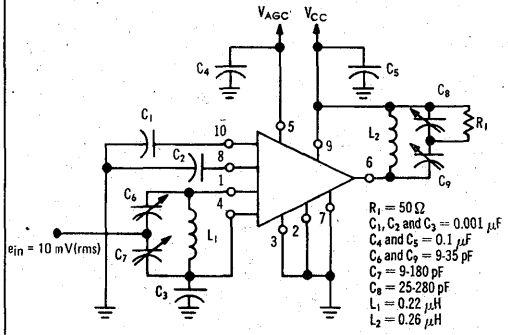
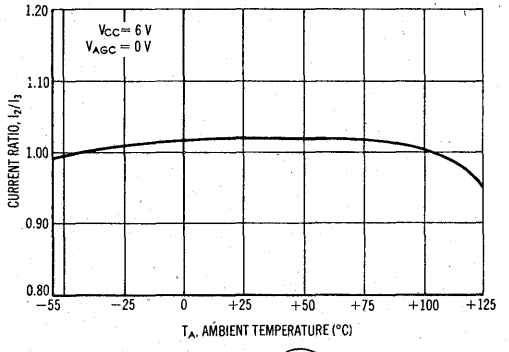


FIGURE 4 – DRAIN CURRENT TEMPERATURE CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

FIGURE 5 – INPUT RESISTANCE AND CAPACITANCE versus FREQUENCY

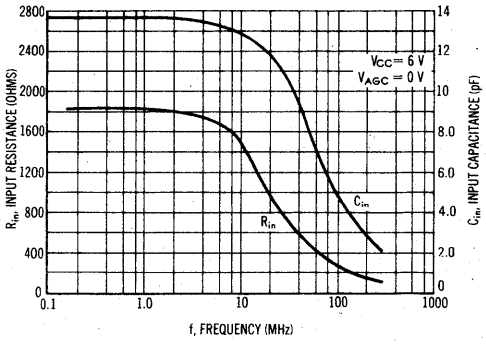


FIGURE 6 – INPUT RESISTANCE AND CAPACITANCE versus AGC VOLTAGE

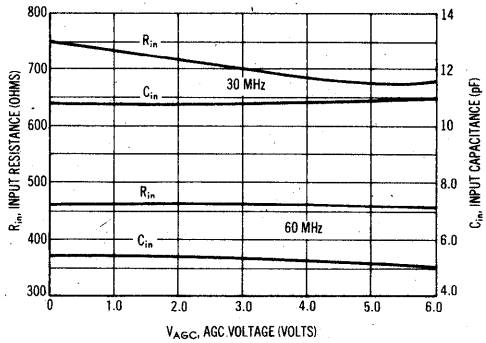


FIGURE 7 – OUTPUT RESISTANCE AND CAPACITANCE versus FREQUENCY

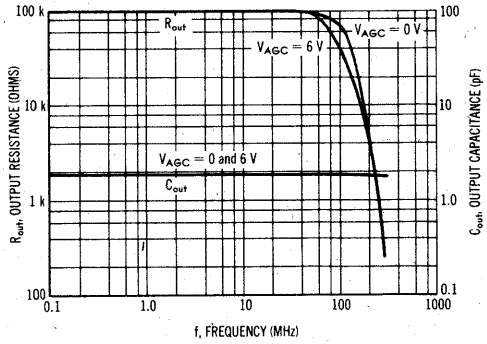


FIGURE 8 – OUTPUT RESISTANCE AND CAPACITANCE versus AGC VOLTAGE

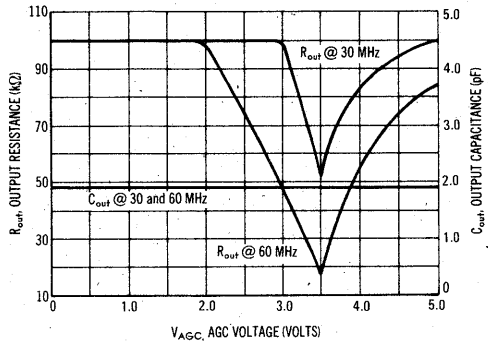


FIGURE 9 – MAXIMUM TRANSDUCER POWER GAIN versus FREQUENCY

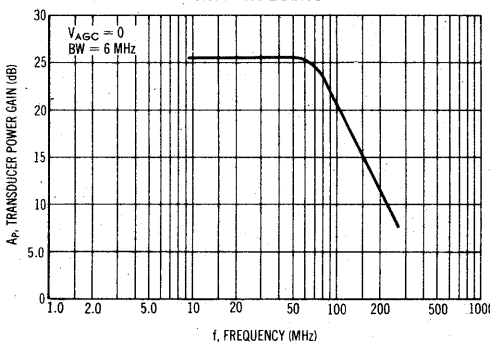
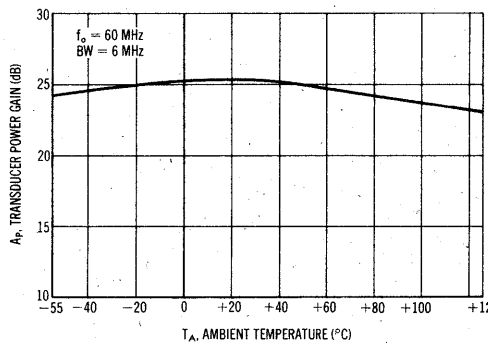


FIGURE 10 – TRANSDUCER POWER GAIN versus TEMPERATURE



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TYPICAL CHARACTERISTICS (continued)

FIGURE 11 – TRANSDUCER POWER BANDWIDTH versus AGC VOLTAGE

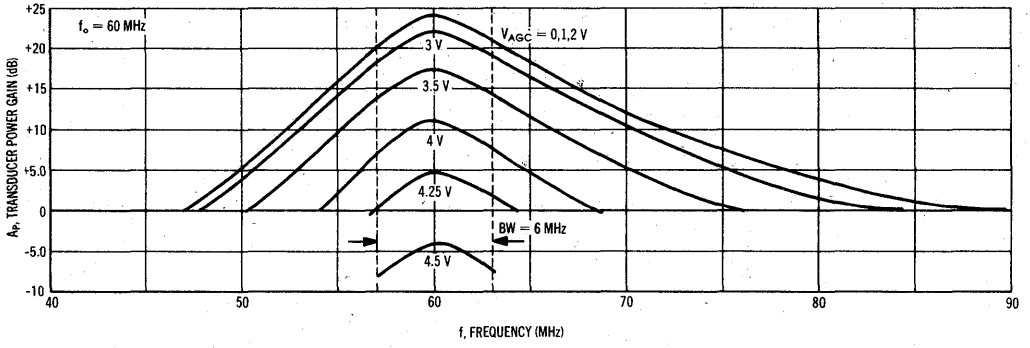


FIGURE 12 – NOISE FIGURE AND OPTIMUM SOURCE RESISTANCE versus FREQUENCY

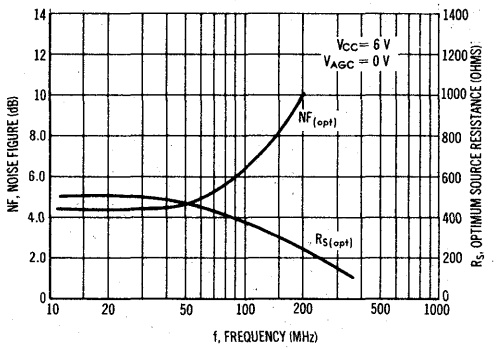


FIGURE 13 – NOISE FIGURE versus SOURCE RESISTANCE

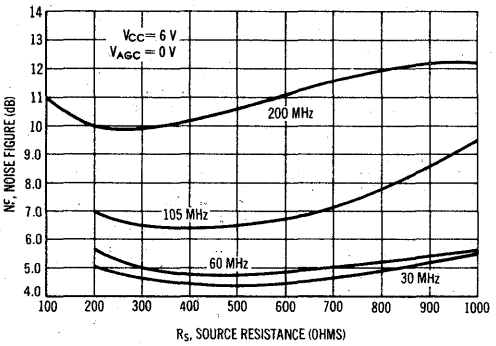


FIGURE 14 – y_{21}, FORWARD-TRANSFER ADMITTANCE versus FREQUENCY

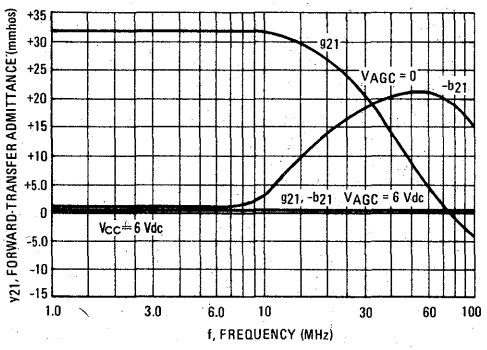
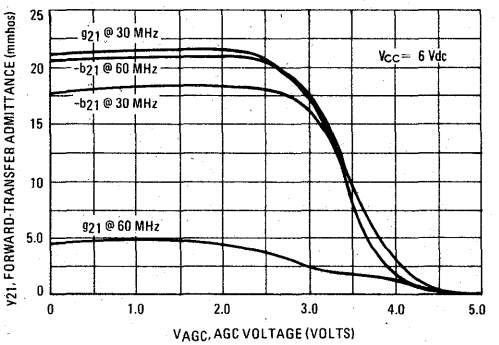


FIGURE 15 – y_{21}, FORWARD-TRANSFER ADMITTANCE versus AGC VOLTAGE



TYPICAL CHARACTERISTICS

(V_{CC} = 6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 16 – y_{12}, REVERSE TRANSFER-ADMITTANCE versus FREQUENCY

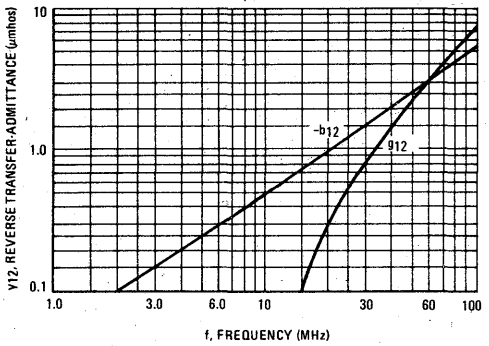
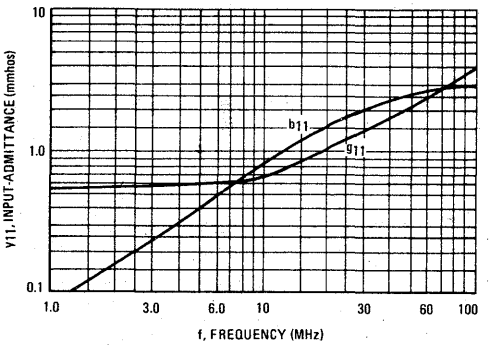


FIGURE 17 – y_{11}, INPUT-ADMITTANCE versus FREQUENCY



The y_{12} shown in Figure 16 illustrates the extremely low feedback of the MC1550 with no contribution from the external mounting circuitry. However, in many cases the external circuitry may contribute as much or more to the total feedback than does the MC1550.

To perform more accurate design calculations of gain, stability, and input - output impedances it is recommended that the designer first determine the total feedback of device plus circuitry.

This can be done in one of two ways:

(1) Measure the total y_{12} or s_{12} of the MC1550 installed in its mounting circuitry, or

(2) Measure the y_{12} of the circuitry alone (without the MC1550 installed) and add the circuit y_{12} to the y_{12} for the MC1550 given in Figure 16.

FIGURE 19 – s_{11} AND s_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT

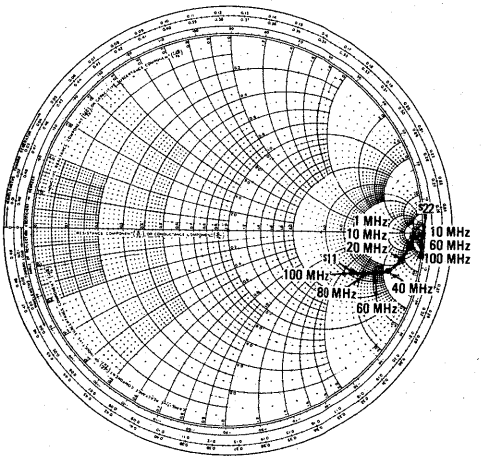
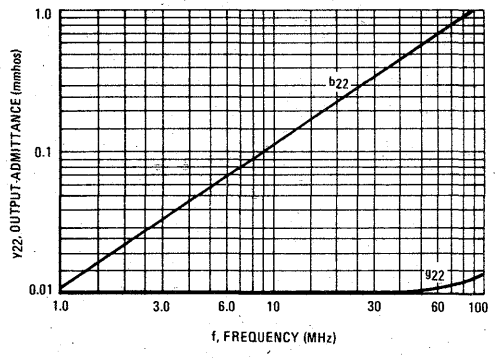


FIGURE 18 – y_{22}, OUTPUT-ADMITTANCE versus FREQUENCY



8

TYPICAL CHARACTERISTICS (continued)

(V_{CC} = 6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 20 – s_{11}, INPUT REFLECTION COEFFICIENT versus FREQUENCY

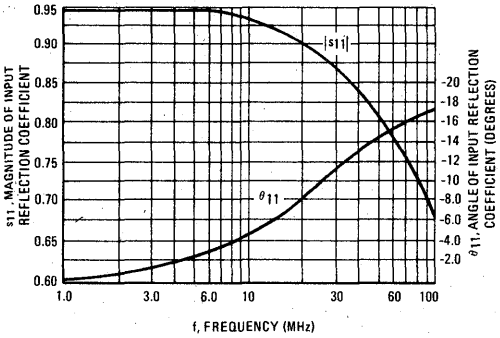


FIGURE 21 – s_{22}, OUTPUT REFLECTION COEFFICIENT versus FREQUENCY

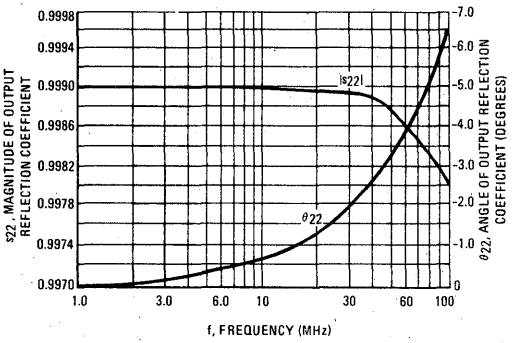


FIGURE 22 – s_{21}, FORWARD TRANSMISSION COEFFICIENT (GAIN)

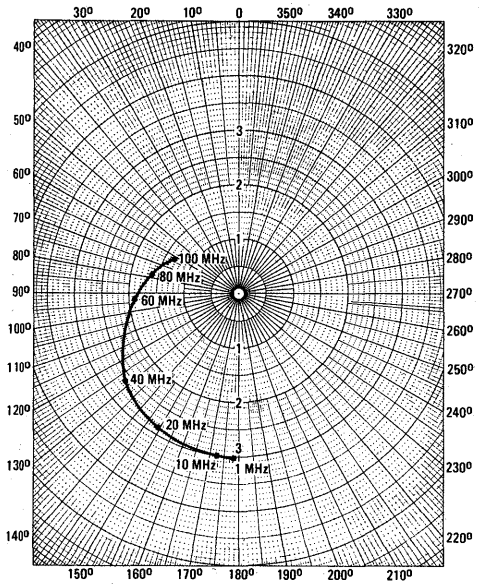
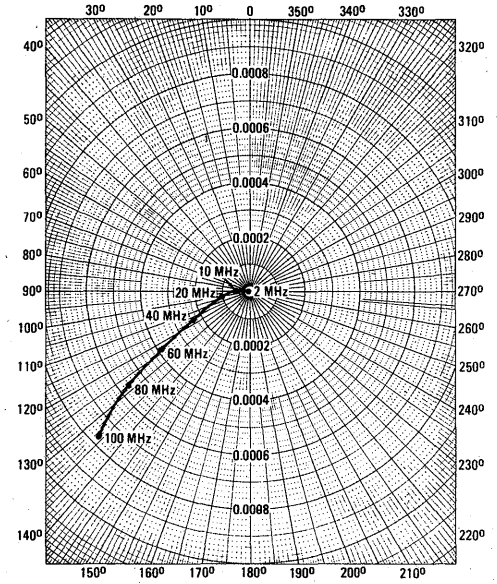


FIGURE 23 – s_{12}, REVERSE TRANSMISSION COEFFICIENT (FEEDBACK)



8

ORDERING INFORMATION

Device	Temperature Range	Package
MC1552G	−55°C to +125°C	Metal Can
MC1553G	−55°C to +125°C	Metal Can

MC1552G
MC1553G

VIDEO AMPLIFIERS

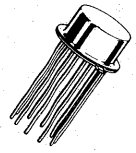
These devices consist of a three-stage, direct-coupled, common-emitter cascade incorporating series feedback to achieve stable voltage gain, low distortion, and wide bandwidth. They employ a temperature-compensated dc feedback loop to stabilize the operating point and a current-biased emitter follower output and are intended for use as either wide-band linear amplifiers or as fast rise pulse amplifiers.

- High Gain – 34 dB ± 1 dB (MC1552)
  52 dB ± 1 dB (MC1553)
- Wide Bandwidth – 40 MHz (MC1552)
  35 MHz (MC1553)
- Low Distortion – 0.2% at 200 kHz
- Low Temperature Drift – ±0.002 dB/°C

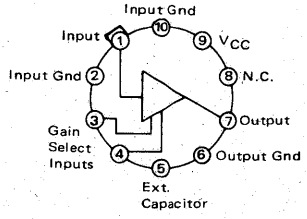
HIGH FREQUENCY VIDEO AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

CASE 603B
METAL PACKAGE



PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage, Pin 9	V_{CC}	9.0	Vdc
Input Differential Voltage, Pin 1 to Pin 2 (R_S = 500 ohms)	V_{ID}	1.0	V(rms)
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6	mW mW/°C
Operating Ambient Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

REPRESENTATIVE CIRCUIT SCHEMATICS

FIGURE 1 – MC1552 (LOW GAIN)

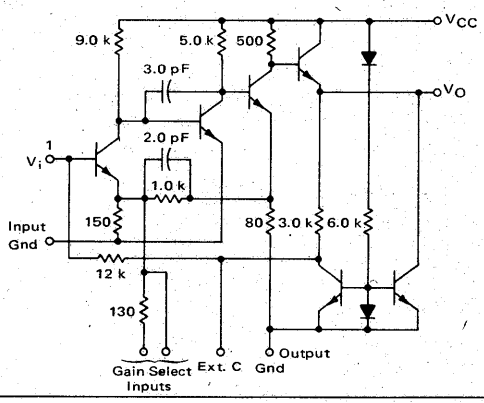
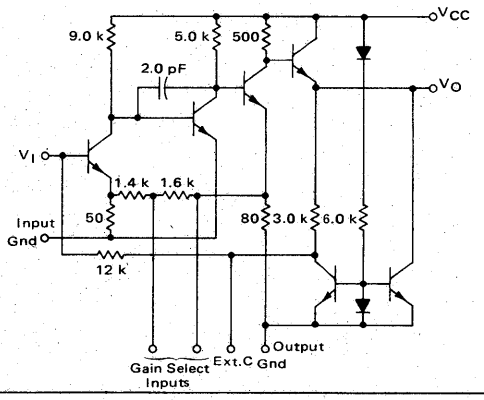


FIGURE 2 – MC1553 (HIGH GAIN)



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ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $T_A = 25^oC$, $V_{CC} = 6.0$ V and specification applies for all Gain Selection options.

Characteristic	Test Figure	Symbol	MC1552G Min	MC1552G Typ	MC1552G Max	MC1553G Min	MC1553G Typ	MC1553G Max	Unit
Voltage Gain	3	A_V							V/V
(Gain Option = 50)			44	50	56	–	–	–	
(Gain Option = 100)			87	100	113	–	–	–	
(Gain Option = 200)			–	–	–	175	200	225	
(Gain Option = 400)			–	–	–	350	400	450	
$-55^oC \leq T_A \leq 125^oC$									
(Gain Option = 50)			42	–	58	–	–	–	
(Gain Option = 100)			83	–	117	–	–	–	
(Gain Option = 200)			–	–	–	171	–	230	
(Gain Option = 400)			–	–	–	342	–	461	
Voltage Gain Variation ($-55^oC \leq T_A \leq 125^oC$)	3	ΔA_V	–	±0.2	–	–	±0.2	–	dB
Small-Signal Bandwidth	3,6	BW							MHz
(Gain Option = 50)			21	40	–	–	–	–	
(Gain Option = 100)			17	35	–	–	–	–	
(Gain Option = 200)			–	–	–	17	35	–	
(Gain Option = 400)			–	–	–	7.5	15	–	
Input Impedance ($f = 100$ kHz, $R_L = 1.0$ kΩ)		z_i	7.0	10	–	7.0	10	–	kΩ
Output Impedance ($f = 100$ kHz, $R_S = 50$ Ω)		z_o	–	16	50	–	16	50	Ω
DC Output Voltage	3	V_O	2.5	2.9	3.2	2.5	2.9	3.2	Vdc
($-55^oC \leq T_A \leq 125^oC$)			2.3	–	3.4	2.4	–	3.3	
DC Output Voltage Variation ($-55^oC \leq T_A \leq 125^oC$)	3	ΔV_O	–	±0.05	–	–	±0.05	–	Vdc
Output Voltage Range ($z_L \leq 1.0$ kΩ, $C_i = 100$ mV rms) ($-55^oC \leq T_A \leq 125^oC$)	3	V_{OR}	3.6	4.2	–	3.6 3.4	4.2	–	V p-p
Power Supply Current	–	I_{CC}	–	12.5	20	–	12.5	20	mA
($-55^oC \leq T_A \leq 125^oC$)			–	–	24	–	–	23	
Propagation Delay Time	3,4	t_{PHL}							ns
(Gain Option = 50)			–	8.0	–	–	–	–	
(Gain Option = 100)			–	9.0	–	–	–	–	
(Gain Option = 200)			–	–	–	–	10	–	
(Gain Option = 400)			–	–	–	–	25	–	
Transition (Rise) Time	3,4	t_{THL}							ns
(Gain Option = 50)			–	9.0	16	–	–	–	
(Gain Option = 100)			–	12	20	–	–	–	
(Gain Option = 200)			–	–	–	–	11	20	
(Gain Option = 400)			–	–	–	–	30	45	
Overshoot	3,4	$100 V_{OS}/V_P$	–	5.0	–	–	5.0	–	%
Noise Figure ($R_S = 400$ Ω, $f_o = 30$ MHz,BW = 3.0 MHz) (See Figure 14)	–	NF	–	3.0	–	–	3.0	–	dB
Total Harmonic Distortion ($V_o = 2.0$ V p-p, $f = 200$ kHz, $R_L = 1.0$ kΩ)	–	THD	–	0.2	–	–	0.2	–	%

NOTES

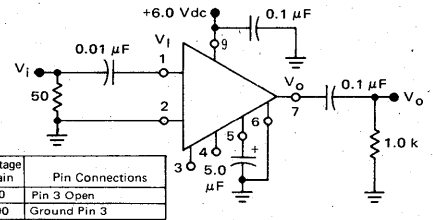
1. Ground Pin 6 as close to package as possible to minimize overshoot. Best results are usually obtained by directly grounding the package.
2. If large input and output coupling capacitors are used, place a shield between them to avoid input-output coupling.
3. A high-frequency capacitor must always be used to by-pass the power supply. This capacitor should be as close to the circuit as possible.
4. Voltage gain can be adjusted to any value between 50 and 3000 by connecting an external resistor from Pin 4 to ground on MC1552, or from Pin 3 to ground on MC1553, as shown in Figure 8. Under these conditions, the following equations must be used to determine C1 and C2 rather than the circuits shown in Figure 5.

Fig. 5b $C1 = \dfrac{1}{2\pi f_c(1.7 \times 10^4)}$ Farads; $C2 = 8\,C1(V_o/V_i)$ Farads

Fig. 5c $C1 = \dfrac{V_o/V_i}{2\pi f_c(1.5 \times 10^4)}$ Farads

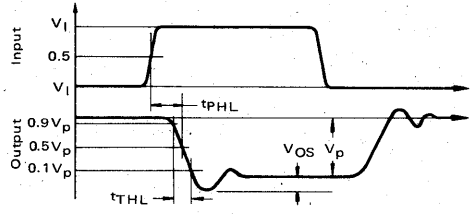
Fig. 5d $C2 = \dfrac{V_o/V_i}{2\pi f_c(3 \times 10^3)}$ Farads

FIGURE 3 – TEST CIRCUIT



Type	Voltage Gain	Pin Connections
MC1552	50	Pin 3 Open
	100	Ground Pin 3
MC1553	200	Connect Pin 3 to Pin 4
	400	Pins 3 and 4 Open

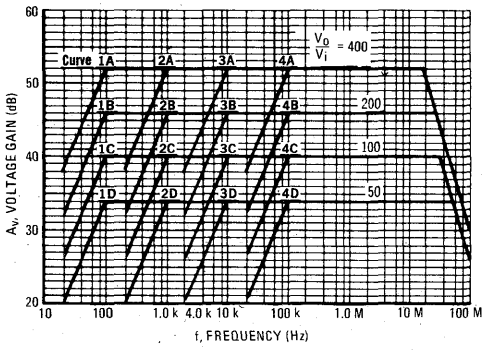
FIGURE 4 – PULSE RESPONSE DEFINITIONS



TYPICAL CHARACTERISTICS

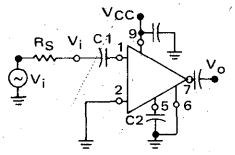
$T_A = +25^oC$

FIGURE 5a – FREQUENCY RESPONSE



TEST CIRCUITS FOR FREQUENCY RESPONSE

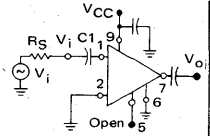
FIGURE 5b – CAPACITIVE COUPLED INPUT ($R_s < 5\ k\Omega$)



Curve No.	C1 (μF)	C2 (μF)
1A	0.1	250
1B	0.1	150
1C	0.1	70
1D	0.1	40

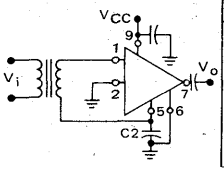
Curve No.	C1 (μF)	C2 (μF)
2A	0.01	30
2B	0.01	18
2C	0.01	8.0
2D	0.01	4.0
	(pF)	
3A	1000	3.0
3B	1000	1.8
3C	1000	0.8
3D	1000	0.4
4A	100	0.3
4B	100	0.18
4C	100	0.08
4D	100	0.04

FIGURE 5c – CAPACITIVE COUPLED INPUT ($R_s < 500\ \Omega$)



Curve No.	C1 (μF)	Curve No.	C1 (μF)
1A	20	3A	0.4
1B	10	3B	0.2
1C	7.0	3C	0.1
1D	3.0	3D	0.06
2A	3.0	4A	0.04
2B	1.0	4B	0.02
2C	0.8	4C	0.01
2D	0.5	4D	0.007

FIGURE 5d – TRANSFORMER COUPLED INPUT



Curve No.	C2 (μF)	Curve No.	C1 (μF)
1A	200	3A	2.0
1B	100	3B	1.0
1C	70	3C	0.7
1D	30	3D	0.3
2A	20	4A	0.2
2B	10	4B	0.1
2C	7.0	4C	0.07
2D	3.0	4D	0.03

FIGURE 6 – VOLTAGE GAIN versus FREQUENCY

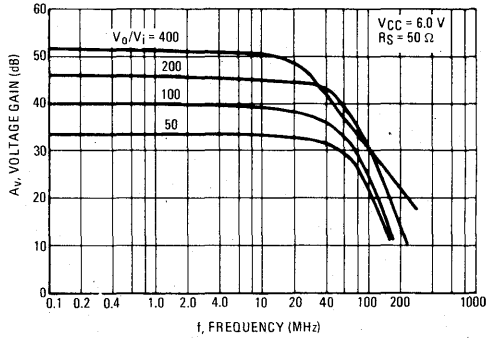


FIGURE 7 – MAXIMUM NEGATIVE SWING SLEW RATE versus LOAD CAPACITANCE

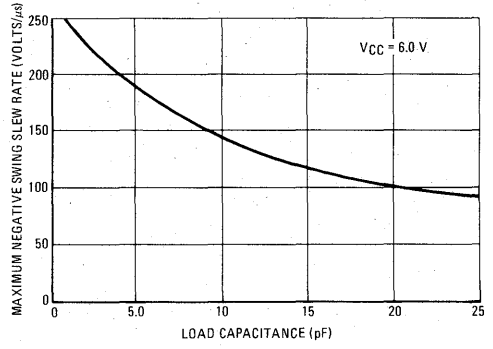
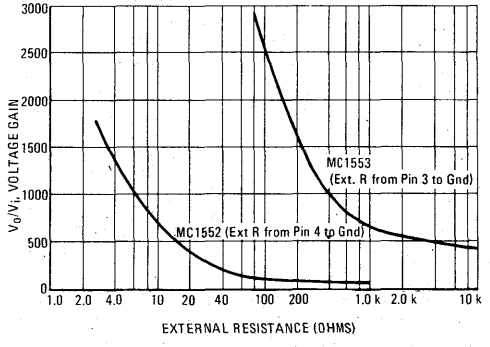


FIGURE 8 – VOLTAGE GAIN ADJUSTMENT BY USE OF EXTERNAL RESISTOR



8

INPUT ADMITTANCE

(V_{CC} = 6.0 Vdc, R_L = 1.0 kΩ, T_A = +25°C)

FIGURE 9 – GAIN = 50

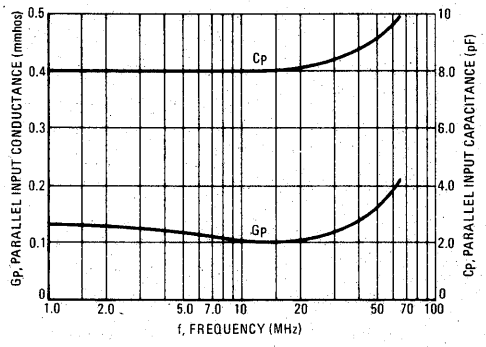


FIGURE 10 – GAIN = 100

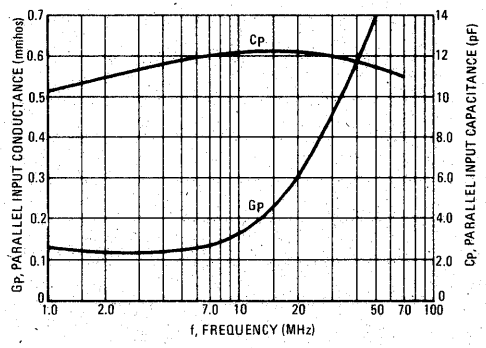


FIGURE 11 – GAIN = 200

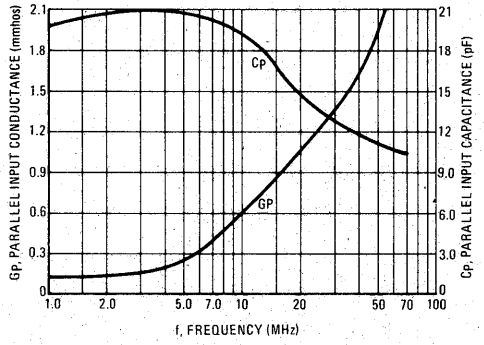


FIGURE 12 – GAIN = 400

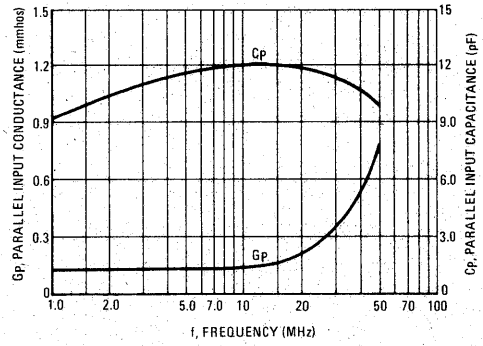


FIGURE 13 – OUTPUT IMPEDANCE versus FREQUENCY

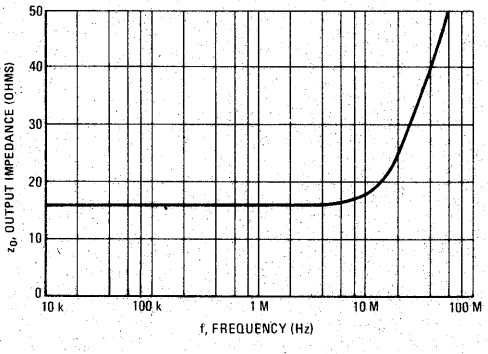
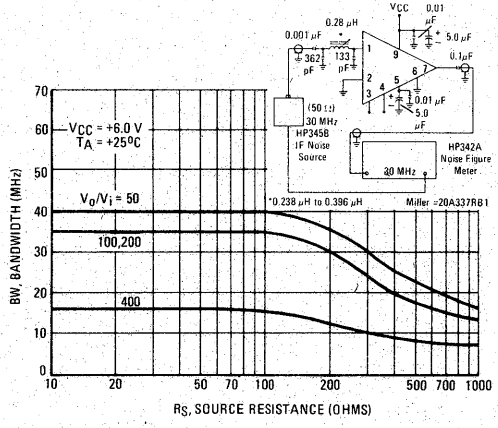


FIGURE 14 – BANDWIDTH versus SOURCE RESISTANCE



8

ORDERING INFORMATION

Device	Temperature Range	Package
MC1454G	0°C to +70°C	Metal Can
MC1554G	−55°C to +125°C	Metal Can

MC1454G
MC1554G

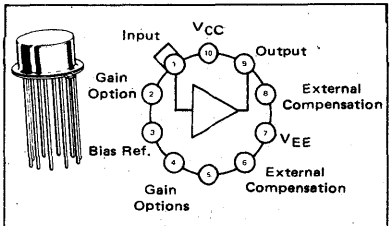
1-WATT POWER AMPLIFIERS

. . . designed to amplify signals to 300-kHz with 1-Watt delivered to a direct coupled or capacitively coupled load.

- Low Total Harmonic Distortion — 0.4% (Typ) @ 1 Watt
- Low Output Impedance — 0.2 Ohm
- Excellent Gain — Temperature Stability

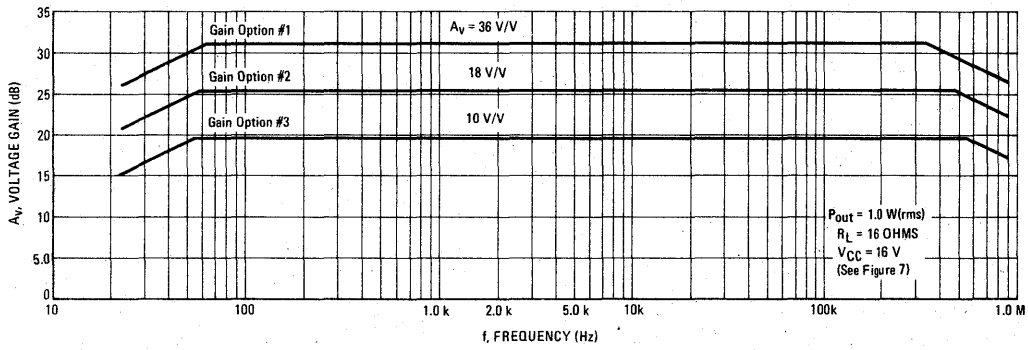
1-WATT POWER AMPLIFIER INTEGRATED CIRCUIT

SILICON MONOLITHIC
EPITAXIAL PASSIVATED

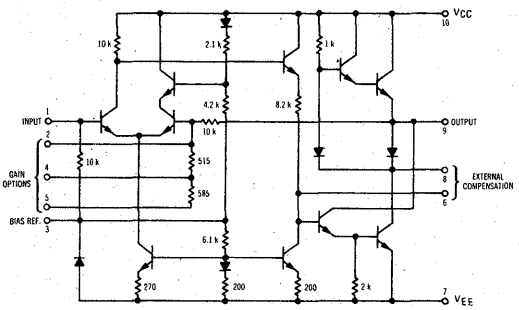


G SUFFIX
CASE 603B

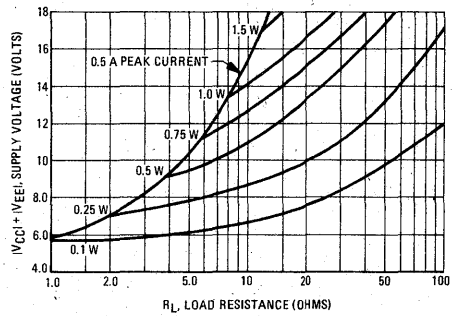
VOLTAGE GAIN versus FREQUENCY (R_L = 16 OHMS)



CIRCUIT SCHEMATIC



MAXIMUM AVAILABLE OUTPUT POWER (SINE WAVE)



8

ELECTRICAL CHARACTERISTICS (T_C = +25°C unless otherwise noted)
Frequency compensation shown in Figures 6 and 7.

Characteristic	Figure	R_L (Ohms)	Gain Option*	Symbol	MC1554 (-55 to +125°C) Min	MC1554 Typ	MC1554 Max	MC1454 (0 to +70°C) Min	MC1454 Typ	MC1454 Max	Unit
Output Power (for e_{out}<5.0% THD)	1	16	–	P_{out}	1.0	1.1	–	–	1.0	–	Watt
Power Dissipation (@ P_{out} = 1.0 W)	1	16	–	P_D	–	0.9	1.2	–	0.9	–	Watt
Voltage Gain	1	16	10	A_v	8.0	10	12	–	10	–	V/V
		16	18		–	18	–	–	18	–	
		16	36		–	36	–	–	36	–	
Input Impedance	1	–	10	z_{in}	7.0	10	–	3.0	10	–	kΩ
Output Impedance	1	–	10	z_o	–	0.2	–	–	0.4	–	Ω
Power Bandwidth (for e_{out}<5.0% THD)	2	16	10	BW	–	270	–	–	270	–	kHz
		16	18		–	250	–	–	250	–	
		16	36		–	210	–	–	210	–	
Total Harmonic Distortion (for e_{in}<0.05% THD, f = 20 Hz to 20 kHz)	2			THD							%
P_{out} = 1.0 Watt (sinewave)		16	10		–	0.4	–	–	0.4	–	
P_{out} = 0.1 Watt (sinewave)		16	10		–	0.5	–	–	0.5	–	
Zero Signal Current Drain	3	∞	–	I_D	–	11	15	–	11	20	mAdc
Output Noise Voltage	3	16	10	V_n	–	0.3	–	–	0.3	–	mV(rms)
Output Quiescent Voltage (Split Supply Operation)	4	16	–	V_o (dc)	–	±10	±30	–	±10	–	mVdc
Positive Supply Sensitivity (V_{EE} constant)	5	∞	–	S^+	–	-40	–	–	-40	–	mV/V
Negative Supply Sensitivity (V_{CC} constant)	5	∞	–	S^-	–	-40	–	–	-40	–	mV/V

*To obtain the voltage gain characteristic desired, use the following pin connections:

Voltage Gain	Pin Connection
10	Pins 2 and 4 open, Pin 5 to ac ground
18	Pins 2 and 5 open, Pin 4 to ac ground
36	Pin 2 connected to Pin 5, Pin 4 to ac ground

Characteristic Definitions
(Linear Operation)

FIGURE 1

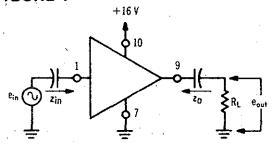


FIGURE 2

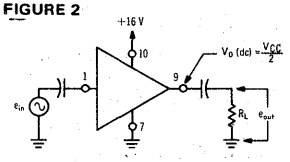
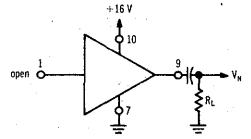


FIGURE 3



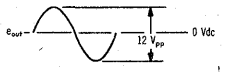


FIGURE 4

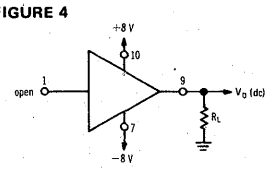
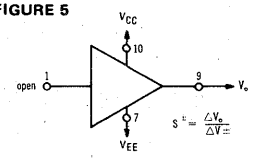


FIGURE 5



MAXIMUM RATINGS (T_C = +25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Total Power Supply Voltage		$\|V_{CC}\| + \|V_{EE}\|$	18	Vdc
Peak Load Current		I_{out}	0.5	Ampere
Audio Output Power		P_{out}	1.8	Watts
Power Dissipation (package limitation) T_A = +25°C Derate above 25°C T_C = +25°C Derate above 25°C		 P_D $1/\theta J_A$ P_D $1/\theta J_C$	 600 4.8 1.8 14.4	 mW mW/°C Watts mW/°C
Operating Temperature Range	MC1454 MC1554	T_A	0 to +70 -55 to +125	°C
Storage Temperature Range		T_{stg}	-55 to +150	°C

TYPICAL CONNECTIONS

FIGURE 6 – SPLIT SUPPLY OPERATION VOLTAGE GAIN (A_V) = 10, $f_{LOW} \approx 25$ Hz

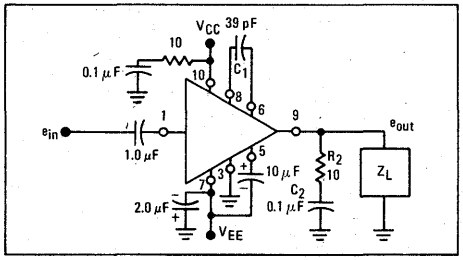
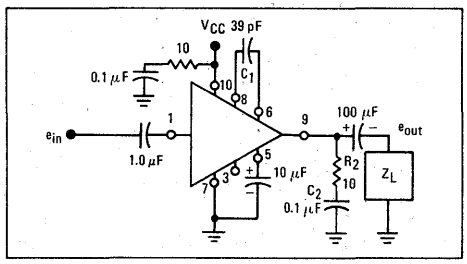


FIGURE 7 – SINGLE SUPPLY OPERATION VOLTAGE GAIN (A_V) = 10, $f_{LOW} \approx 100$ Hz



RECOMMENDED OPERATING CONDITIONS

In order to avoid local VHF instability, the following set of rules must be adhered to:

1. An R-C stabilizing network (0.1 μF in series with 10 ohms) should be placed directly from pin 9 to ground, as shown in Figures 6 and 7, using short leads, to eliminate local VHF instability caused by lead inductance to the load.
2. Excessive lead inductance from the V_{CC} supply to pin 10 can cause high frequency instability. To prevent this, the V_{CC} by-pass capacitor should be connected with short leads from the V_{CC} pin to ground. If this capacitor is remotely located a series R-C network (0.1 μF and 10 ohms) should be used directly from pin 10 to ground as shown in Figures 6 and 7.
3. Lead lengths from the external components to pins 7, 9, and 10 of the package should be as short as possible to insure good VHF grounding for these points.

Due to the large bandwidth of the amplifier, coupling must be avoided between the output and input leads. This can be assured by either (a) use of short leads which are well isolated, (b) narrow-banding the overall amplifier by placing a capacitor from pin 1 to ground to form a low-pass filter in combination with the source impedance, or (c) use of a shielded input cable. In applications which require upper band-edge control the input low-pass filter is recommended.

TYPICAL CHARACTERISTICS

FIGURE 8 – TOTAL HARMONIC DISTORTION versus LOAD RESISTANCE

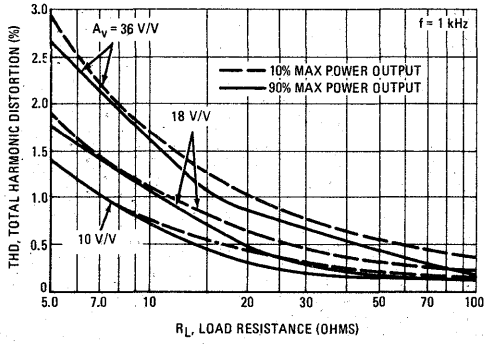
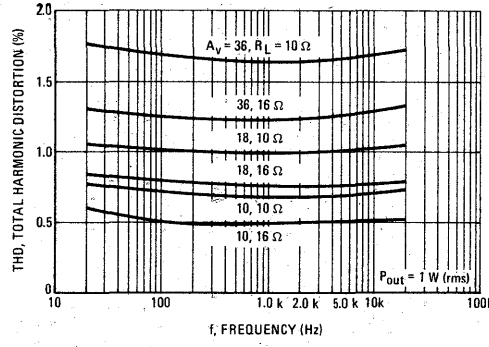


FIGURE 9 – TOTAL HARMONIC DISTORTION versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

FIGURE 10 – VOLTAGE GAIN versus TEMPERATURE

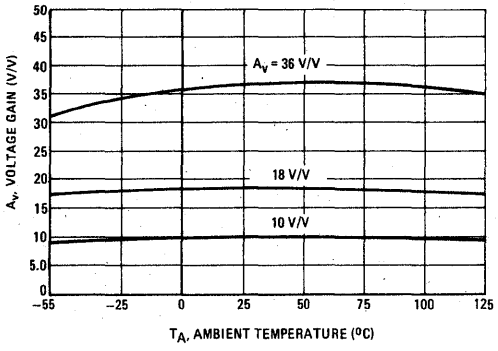


FIGURE 11 – OUTPUT VOLTAGE CHANGE

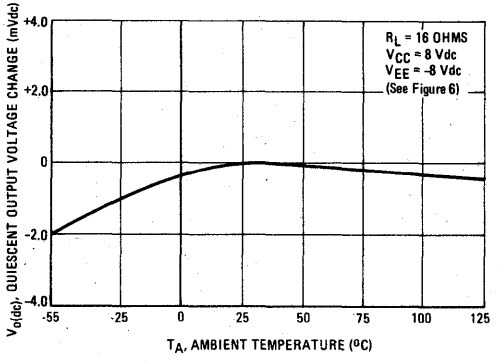


FIGURE 12 – VOLTAGE GAIN versus FREQUENCY ($R_L = \infty$)

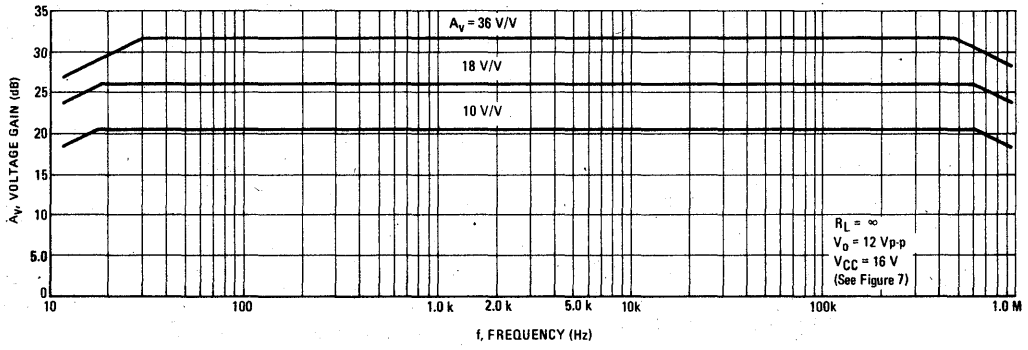
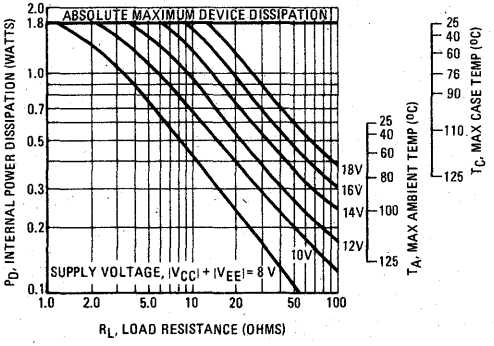


FIGURE 13 – MAXIMUM DEVICE DISSIPATION (SINE WAVE)



8

ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1455G	—	0°C to +70°C	Metal Can
MC1455P1	NE555V	0°C to +70°C	Plastic DIP
MC1455U	—	0°C to +70°C	Ceramic DIP
MC1555G	—	−55°C to +125°C	Metal Can
MC1555U	—	−55°C to +125°C	Ceramic DIP

MC1455
MC1555

Specifications and Applications Information

TIMING CIRCUIT

The MC1555/MC1455 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE555/SE555 Timers
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output

FIGURE 1 – 22-SECOND SOLID-STATE TIME DELAY RELAY CIRCUIT

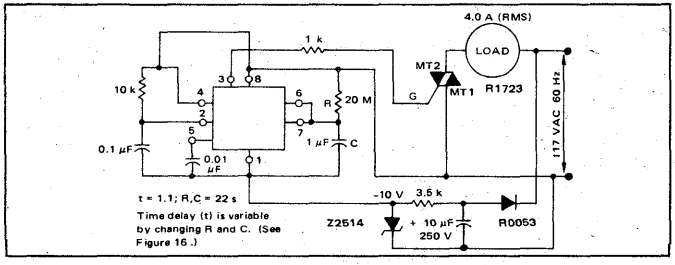
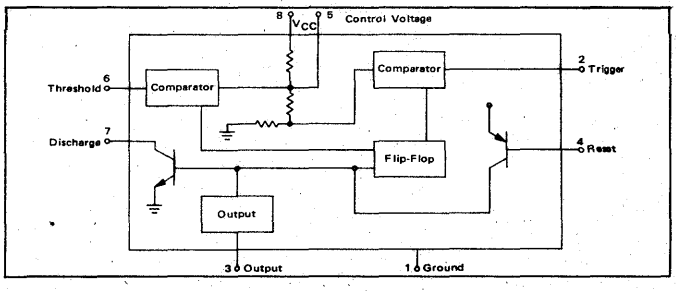


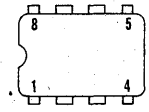
FIGURE 2 – BLOCK DIAGRAM



TIMING CIRCUIT

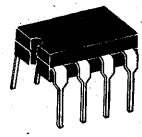
SILICON MONOLITHIC INTEGRATED CIRCUIT

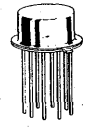
P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(Top View)
(MC1455P1 only)



1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

U SUFFIX
CERAMIC PACKAGE
CASE 693





G SUFFIX
METAL PACKAGE
CASE 601

(Top View)

1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

TYPICAL APPLICATIONS

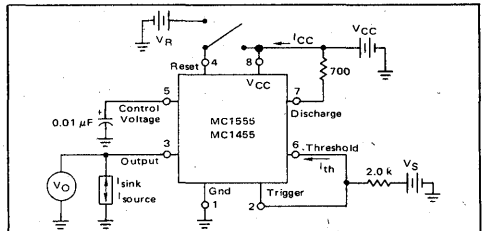
- Time Delay Generation
- Sequential Timing
- Linear Sweep Generation
- Precision Timing
- Pulse Generation
- Pulse Shaping
- Missing Pulse Detection
- Pulse Width Modulation
- Pulse Position Modulation

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current (Pin 7)	I_7	200	mA
Power Dissipation (Package Limitation)	P_D		
Metal Can		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Plastic Dual In-Line Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Temperature Range (Ambient) MC1555	T_A	-55 to +125	°C
MC1455		0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 3 – GENERAL TEST CIRCUIT



Test Circuit for Measuring dc Parameters:
(to set output and measure parameters)
a). When $V_S \geq 2/3\ V_{CC}$, V_O is low.
b). When $V_S \leq 1/3\ V_{CC}$, V_O is high.
c). When V_O is low, pin 7 sinks current. To test for Reset, set V_O, high, apply Reset voltage, and test for current flowing into pin 7. When Reset is not in use, it should be tied to V_{CC}.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +15 V unless otherwise noted.)

Characteristics	Symbol	MC1555			MC1455			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	–	18	4.5	–	16	V
Supply Current	I_{CC}							mA
V_{CC} = 5.0 V, R_L = ∞		–	3.0	5.0	–	3.0	6.0	
V_{CC} = 15 V, R_L = ∞		–	10	12	–	10	15	
Low State, (Note 1)								
Timing Error (Note 2)								
R = 1.0 kΩ to 100 kΩ								
Initial Accuracy C = 0.1 μF		–	0.5	2.0	–	1.0	–	%
Drift with Temperature		–	30	100	–	50	–	PPM/°C
Drift with Supply Voltage		–	0.05	0.20	–	0.10	–	%/Volt
Threshold Voltage	V_{th}	–	2/3	–	–	2/3	–	xV_{CC}
Trigger Voltage	V_T							V
V_{CC} = 15 V		4.8	5.0	5.2	–	5.0	–	
V_{CC} = 5.0 V		1.45	1.67	1.9	–	1.67	–	
Trigger Current	I_T	–	0.5	–	–	0.5	–	μA
Reset Voltage	V_R	0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current	I_R	–	0.1	–	–	0.1	–	mA
Threshold Current (Note 3)	I_{th}	–	0.1	0.25	–	0.1	0.25	μA
Control Voltage Level	V_{CL}							V
V_{CC} = 15 V		9.6	10	10.4	9.0	10	11	
V_{CC} = 5.0 V		2.9	3.33	3.8	2.6	3.33	4.0	
Output Voltage Low	V_{OL}							
(V_{CC} = 15 V)								V
I_{sink} = 10 mA		–	0.1	0.15	–	0.1	0.25	
I_{sink} = 50 mA		–	0.4	0.5	–	0.4	0.75	
I_{sink} = 100 mA		–	2.0	2.2	–	2.0	2.5	
I_{sink} = 200 mA		–	2.5	–	–	2.5	–	
(V_{CC} = 5.0 V)								
I_{sink} = 8.0 mA		–	0.1	0.25	–	–	–	
I_{sink} = 5.0 mA		–	–	–	–	0.25	0.35	
Output Voltage High	V_{OH}							V
(I_{source} = 200 mA)								
V_{CC} = 15 V		–	12.5	–	–	12.5	–	
(I_{source} = 100 mA)								
V_{CC} = 15 V		13	13.3	–	12.75	13.3	–	
V_{CC} = 5.0 V		3.0	3.3	–	2.75	3.3	–	
Rise Time of Output	t_{OLH}	–	100	–	–	100	–	ns
Fall Time of Output	t_{OHL}	–	100	–	–	100	–	ns

NOTES:
1. Supply current when output is high is typically 1.0 mA less.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
   Monostable mode
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 megohms.

TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 4 – TRIGGER PULSE WIDTH

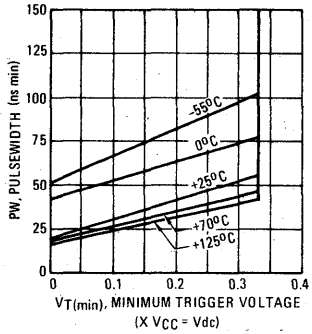


FIGURE 5 – SUPPLY CURRENT

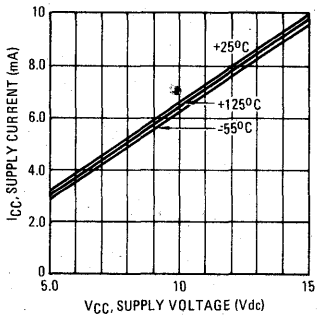


FIGURE 6 – HIGH OUTPUT VOLTAGE

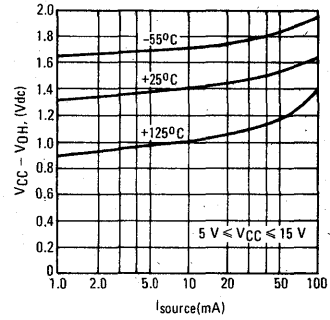


FIGURE 7 – LOW OUTPUT VOLTAGE @ V_{CC} = 5.0 Vdc

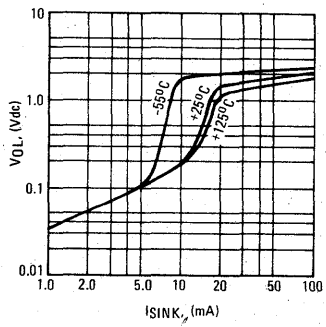


FIGURE 8 – LOW OUTPUT VOLTAGE @ V_{CC} = 10 Vdc

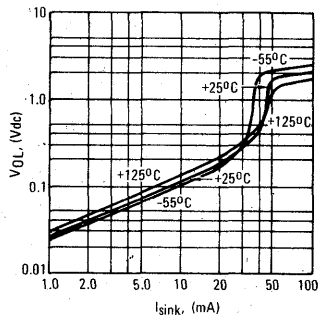


FIGURE 9 – LOW OUTPUT VOLTAGE @ V_{CC} = 15 Vdc

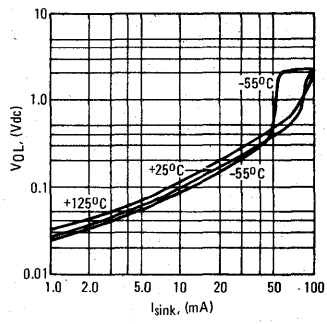


FIGURE 10 – DELAY TIME versus SUPPLY VOLTAGE

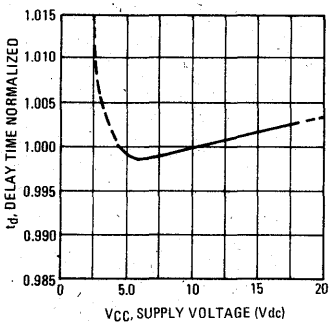


FIGURE 11 – DELAY TIME versus TEMPERATURE

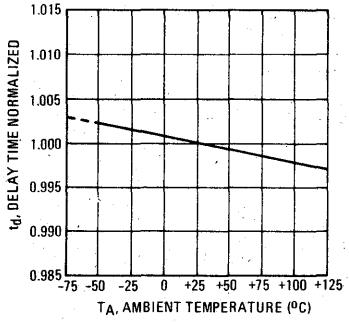
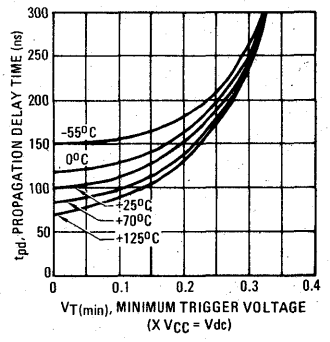


FIGURE 12 – PROPAGATION DELAY versus TRIGGER VOLTAGE



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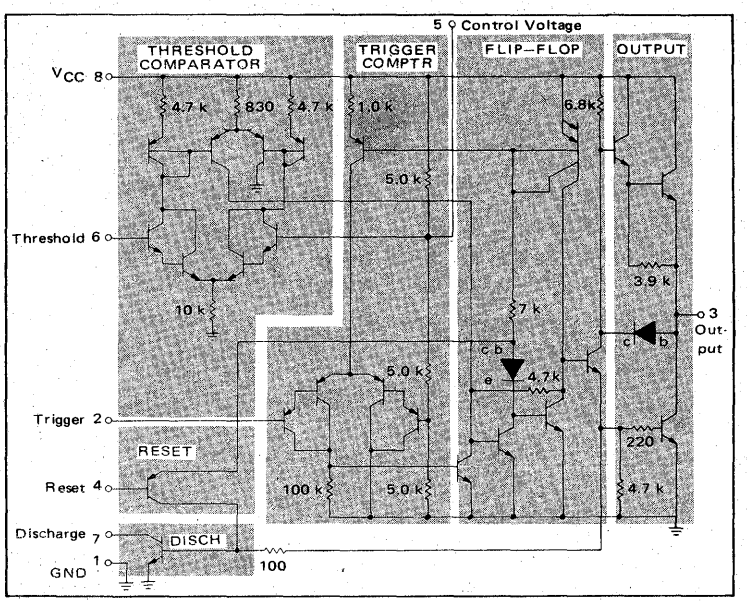


FIGURE 13 – REPRESENTATIVE CIRCUIT SCHEMATIC

GENERAL OPERATION

The MC1555 is a monolithic timing circuit which uses as its timing elements an external resistor – capacitor network. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

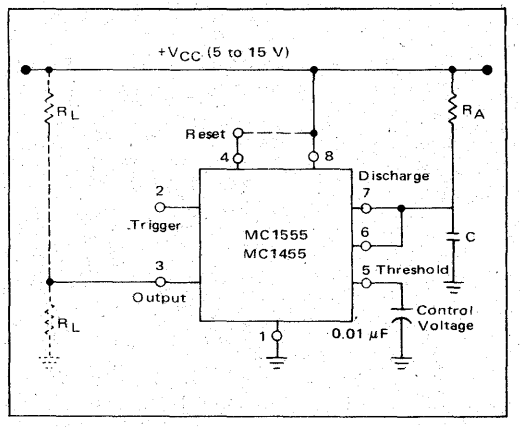
A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

8

Monostable Mode

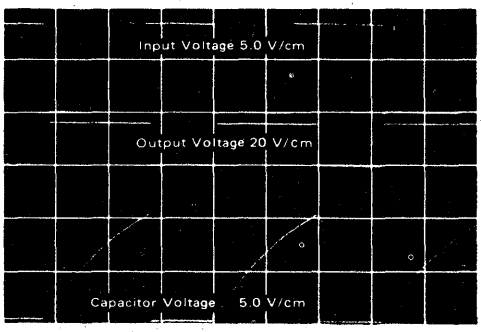
In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below 1/3 V_{CC} the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V_{CC} the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

FIGURE 14 – MONOSTABLE CIRCUIT



GENERAL OPERATION (continued)

FIGURE 15 – MONOSTABLE WAVEFORMS



t = 50 μs/cm

(R_A = 10 kΩ, C = 0.01 μF, R_L = 1.0 kΩ, V_{CC} = 15 V)

FIGURE 16 – TIME DELAY

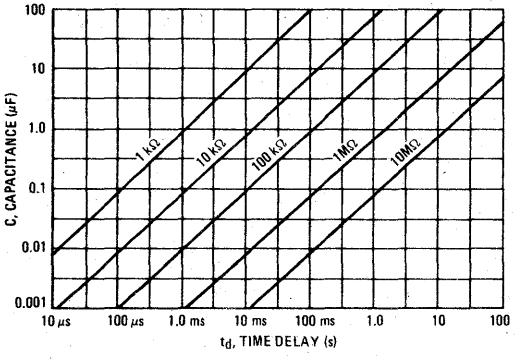


FIGURE 17 – ASTABLE CIRCUIT

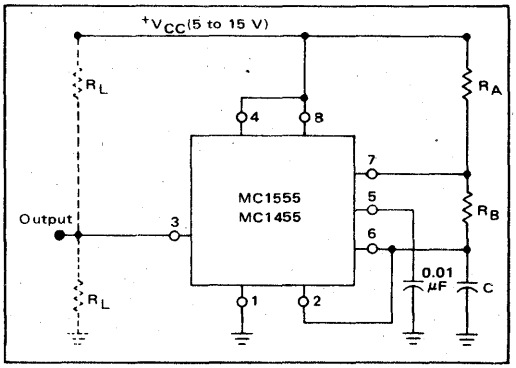
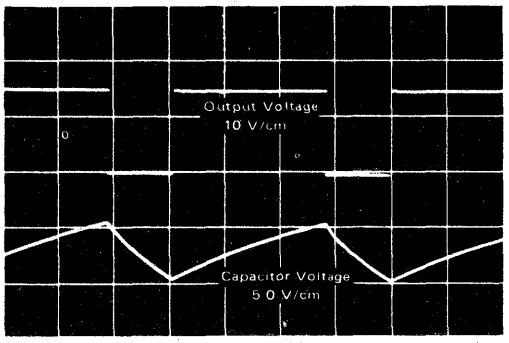


FIGURE 18 – ASTABLE WAVEFORMS



t = 20 μs/cm

(R_A = 5.1 kΩ, C = 0.01 μF, R_L = 1.0 kΩ;
R_B = 3.9 kΩ, V_{CC} = 15 V)

Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 V_{CC} and 2/3 V_{CC}. See Figure 17.

The external capacitor charges to 2/3 V_{CC} through R_A and R_B and discharges to 1/3 V_{CC} through R_B. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by: $t_1 = 0.695\,(R_A+R_B)\,C$

The discharge time (output low) by: $t_2 = 0.695\,(R_B)\,C$

Thus the total period is given by: $T = t_1 + t_2 = 0.695\,(R_A+2R_B)\,C$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A+2R_B)\,C}$

and may be easily found as shown in Figure 19.

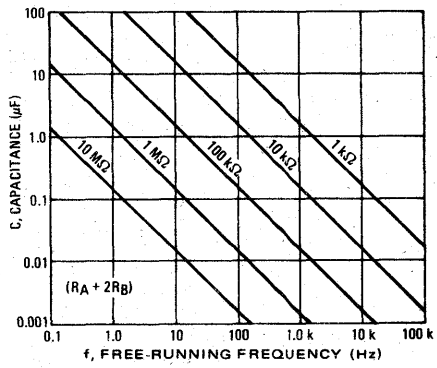
The duty cycle is given by: $DC = \frac{R_B}{R_A+2R_B}$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geq \frac{V_{CC}\,(Vdc)}{I_7\,(A)} \geq \frac{V_{CC}\,(Vdc)}{0.2}$$

FIGURE 19 – FREE-RUNNING FREQUENCY



8

APPLICATIONS INFORMATION

Linear Voltage Ramp

In the monostable mode, the resistor can be replaced by a constant current source to provide a linear ramp voltage. The capacitor still charges from 0 to 2/3 V_{CC}. The linear ramp time is given by $t = \frac{2}{3} \frac{V_{CC}}{I}$

where $I = \frac{V_{CC} - V_B - V_{BE}}{R_E}$. If V_B is much larger than V_{BE}, then t can be made independent of V_{CC}.

Missing Pulse Detector

The timer can be used to produce an output when an input pulse fails to occur within the delay of the timer. To accomplish this, set the time delay to be slightly longer than the time between successive input pulses. The timing cycle is then continuously reset by the input pulse train until a change in frequency or a missing pulse allows completion of the timing cycle, causing a change in the output level.

FIGURE 20 – LINEAR VOLTAGE SWEEP CIRCUIT

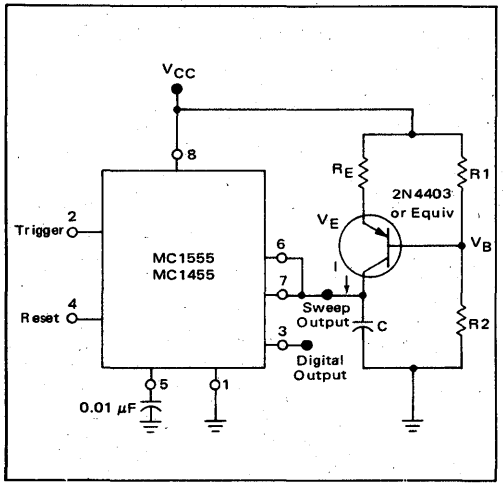


FIGURE 22

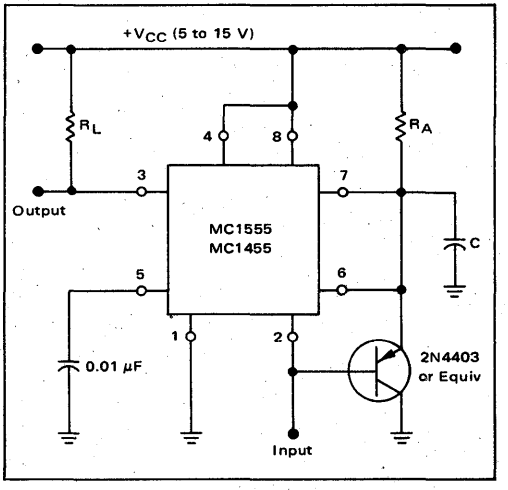
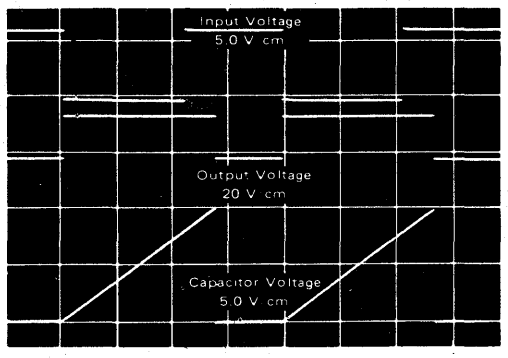
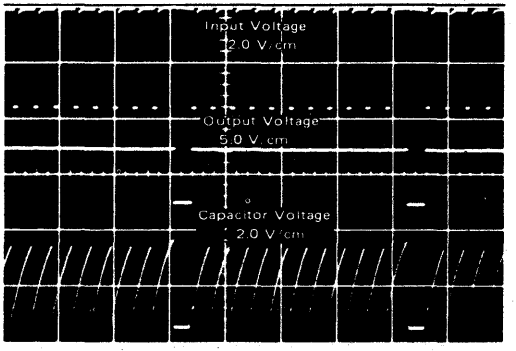


FIGURE 21 – LINEAR VOLTAGE RAMP WAVEFORMS
(R_E = 10 kΩ, R2 = 100 kΩ, R1 = 39 kΩ, C = 0.01 μF, V_{CC} = 15 V)



t = 100 μs/cm

FIGURE 23 – MISSING PULSE DETECTOR WAVEFORMS
(R_A = 2.0 kΩ, R_L = 1.0 kΩ, C = 0.1 μF, V_{CC} = 15 V)



t = 500 μs/cm

APPLICATIONS INFORMATION (continued)

Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at pin 5. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

FIGURE 24

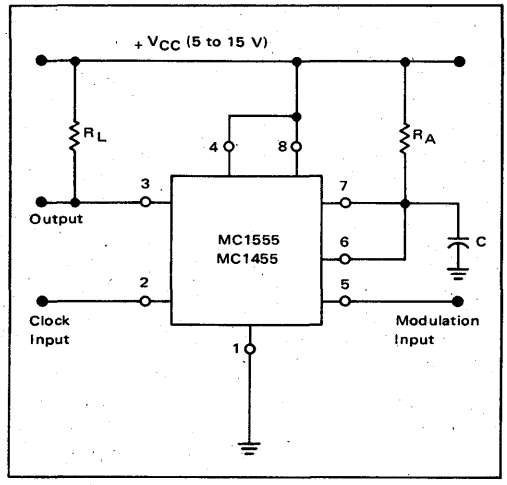
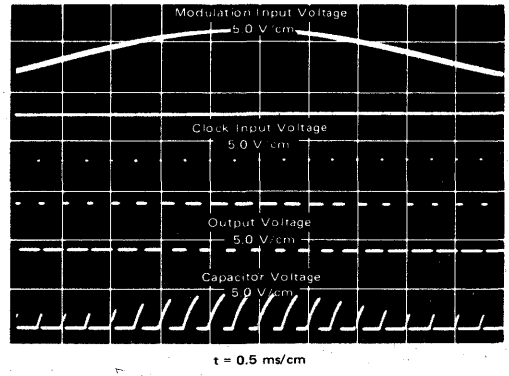


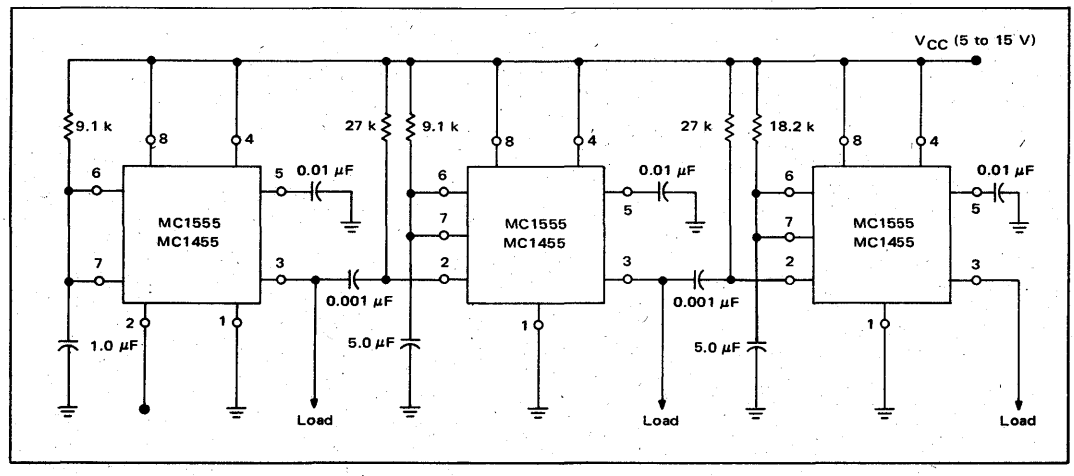
FIGURE 25 – PULSE WIDTH MODULATION WAVEFORMS
(R_A = 10 kΩ, C = 0.02 μF, V_{CC} = 15 V)



Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 26 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

FIGURE 26



8

MC1464

Product Preview

3.0 AMPERE NPN POWER DARLINGTON DRIVER

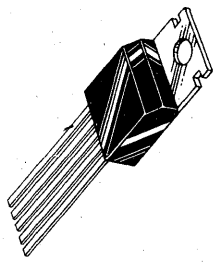
. . . designed for use as an output device in complementary general purpose amplifier applications.

The MC1464 can also be used for driving lamps, relays, or printer hammers in a variety of industrial and consumer applications.

- High DC Current Gain
  h_{FE} = 2000 (Min) @ I_C = 3.0 A
- Can Be Voltage or Current Driven
- High Collector-Emitter Breakdown Voltage
  BV_{CEO} = 80 V (Min) @ I_C = 100 mA
- Includes Current Limit Control

NPN
POWER DARLINGTON
DRIVER

SILICON MONOLITHIC
INTEGRATED CIRCUIT



1. Emitter
2. Current Drive (Base)
3. Current Limit Control
4. Voltage Drive
5. Collector

CIRCUIT SCHEMATIC

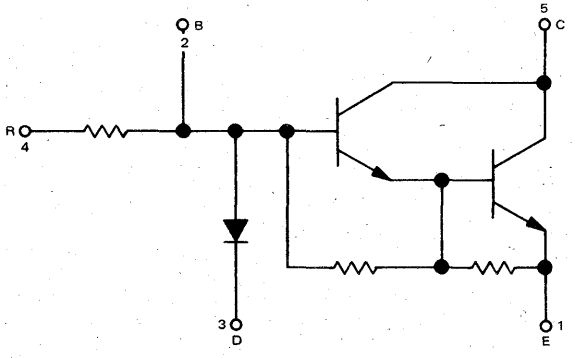
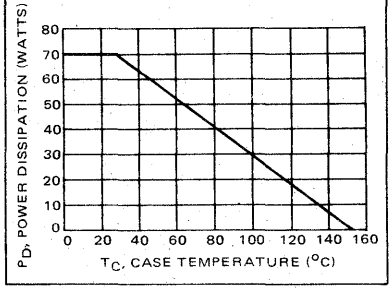


FIGURE 1 – POWER DERATING



ORDERING INFORMATION

Device	Temperature Range	Package
MC1464P	0 to +125°C	Plastic

This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	80	Vdc
Collector-Base Voltage	V_{CB}	80	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current	I_C	3.0	Adc
Base Current	I_B	0.1	Adc
Total Device Dissipation @ $T_C = 25^oC$ Derate above 25^oC	P_D	70 0.56	Watts $W/^oC$
Operating Junction Temperature Range	T_J	-55 to +150	^oC
Storage Temperature Range	T_{stg}	-55 to +150	^oC
Operating Ambient Temperature Range	T_A	0 to +70	^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.8	$^oC/W$
Thermal Resistance, Juction to Ambient	θ_{JA}	50	$^oC/W$

ELECTRICAL CHARACTERISTICS ($T_A = 25^oC$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Diode Breakdown Voltage (I = 1.0 mA)	B_V	5.0	–	–	Vdc
Diode Forward Voltage (I_F = 5.0 mA) (I_F = 0.5 mA)	V_F	 0.7 0.64	 – –	 0.8 0.76	Vdc
Input Resistor	R_{in}	1400	–	1800	Ω
Input Resistor Dissipation	P_D	100	–	–	mW
Collector-Emitter Breakdown Voltage (I_C = 100 mA, I_B = 0)	BV_{CEO}	65	–	–	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0)	I_{CEO}	–	–	500	μAdc
Collector Cutoff Current (V_{CB} = 80 V, I_E = 0, $T_A = 25^oC$) (V_{CB} = 80 V, I_E = 0, $T_A = 100^oC$)	I_{CBO}	 – –	 – –	 0.2 2.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	–	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 3.0 Adc, V_{CE} = 3.0 V)	h_{FE}	1500	–	7000	–
Collector-Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 12 mAdc)	$V_{CE(sat)}$	–	–	2.5	Vdc
Base-Emitter On Voltage(1)	$V_{BE(on)}$	1.7	–	1.9	–
DYNAMIC CHARACTERISTICS					
Small-Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)	h_{fe}	1.0	–	–	–

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

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ORDERING INFORMATION

Device	Temperature Range	Package
MC1590F	−55°C to +125°C	Ceramic Flat
MC1590G	−55°C to +125°C	Metal Can

MC1590

RF/IF/AUDIO AMPLIFIER

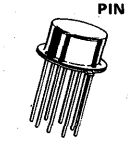
. . . an integrated circuit featuring wide-range AGC for use in RF/IF amplifiers and audio amplifiers over the temperature range, - 55 to +125°C. See Motorola Application Note AN-513 for design details.

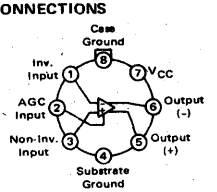
- High Power Gain – 50 dB typ at 10 MHz
  45 dB typ at 60 MHz
  35 dB typ at 100 MHz
- Wide-Range AGC – 60 dB min, dc to 60 MHz
- Low Reverse Transfer Admittance – <10 μmhos typ at 60 MHz
- 6.0 to 15-Volt Operation, Single-Polarity Power Supply

WIDEBAND AMPLIFIER WITH AGC

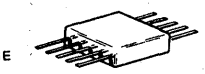
SILICON MONOLITHIC INTEGRATED CIRCUIT

PIN CONNECTIONS





G SUFFIX
METAL PACKAGE
CASE 601
TO-99



F SUFFIX
CERAMIC PACKAGE
CASE 606

(Same Pin Connections as Above)

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol*	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Output Supply	V_O	+18	Vdc
AGC Supply	V_I (AGC)	V_{CC}	Vdc
Differential Input Voltage	V_I	5.0	Vdc
Operating Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+175	°C

ADMITTANCE PARAMETERS (V_{CC} = +12 Vdc, T_A = +25°C)

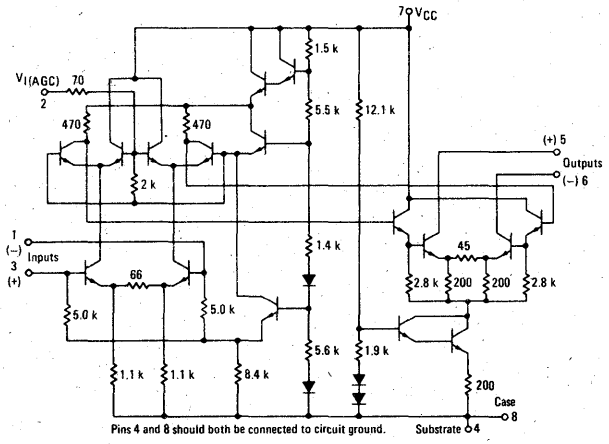
Parameter	Symbol	f = MHz Typ 30	f = MHz Typ 60	Unit
Single-Ended Input Admittance	g_{11} b_{11}	0.4 1.2	0.75 3.4	mmhos
Single-Ended Output Admittance	g_{22} b_{22}	0.05 0.50	0.1 1.0	mmho
Forward Transfer Admittance (Pin 1 to Pin 5)	$\lvert Y_{21}\rvert$ θ_{21}	150 −45	150 −105	mmhos degrees
Reverse Transfer Admittance*	g_{12} b_{12}	−0 -5.0	−0 −10	μmhos

*The value of Reverse Transfer Admittance includes the feedback admittance of the test circuit used in the measurement. The total feedback capacitance (including test circuit) is 0.025 pF and is a more practical value for design calculations than the internal feedback of the device alone. (See Figure 10.)

SCATTERING PARAMETERS (V_{CC} = +12 Vdc, T_A = +25°C, Z_o = 50 Ω)

Parameter	Symbol	f = MHz Typ 30	f = MHz Typ 60	Unit
Input Reflection Coefficient	S_{11} θ_{11}	0.95 -7.3	0.93 −16	– degrees
Output Reflection Coefficient	S_{22} θ_{22}	0.99 -3.0	0.98 −5.5	– degrees
Forward Transmission Coefficient	S_{21} θ_{21}	16.8 128	14.7 64.3	– degrees
Reverse Transmission Coefficient	S_{12} θ_{12}	0.00048 84.9	0.00092 79.2	– degrees

REPRESENTATIVE CIRCUIT SCHEMATIC



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ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, f = 60 MHz, BW = 1.0 MHz, T_A = −55°C to 125°C unless otherwise noted)

Characteristic	Symbol	MC1590 Min	MC1590 Typ	MC1590 Max	Unit
AGC Range					
($V_{I\ (AGC)}$ = 5.0 V to 7.0 V)	–	58	–	–	dB
($V_{I\ (AGC)}$ = 5.0 V to 7.0 V, T_A = 25°C)		60	68	–	
Single-Ended Power Gain (Figure 24)	G_p	37	–	–	dB
(T_A = 25°C)		40	45		
Noise Figure					
(R_s optimized for best NF) (T_A = 25°C)	NF	–	6.0	7.0	dB
Output Voltage Swing (Pin 5)					
Differential Output (Figure 25)	V_{ODR}				
(0 dB AGC)		10	–	–	Vpp
(0 dB AGC, T_A = 25°C)		13	14	–	
(−30 dB AGC)		4.0	–	–	
(−30 dB AGC, T_A = 25°C)		6.6	6.0	–	
Single-Ended Output (Figure 24)	V_{OCR}				Vpp
(0 dB AGC)		5.0	–	–	
(0 dB AGC, T_A = 25°C)		6.5	7.0	–	
(−30 dB AGC)		2.0	–	–	
(−30 dB AGC, T_A = 25°C)		2.5	3.0	–	
Output Stage Current	I_O				
(Sum of Pins 5 and 6)		3.5	–	8.0	mA
(T_A = 25°C)		4.0	5.6	7.5	
Output Current Matching					
(Magnitude of Difference of Output Currents) (T_A = 25°C)	ΔI_O	–	0.7	–	mA
Power Supply Current					
(V_O = 0 V)	I_{CC}	–	–	20	mA
(V_O = 0 V, T_A = 25°C)		–	14	17	
Power Consumption					
(V_I = 0 V)	P_C	–	–	240	mW
(V_I = 0 V, T_A = 25°C)		–	168	200	

FIGURE 1 – UNNEUTRALIZED POWER GAIN versus FREQUENCY
(Tuned Amplifier, See Figure 24)

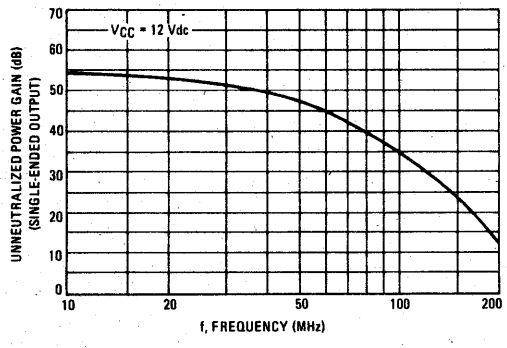
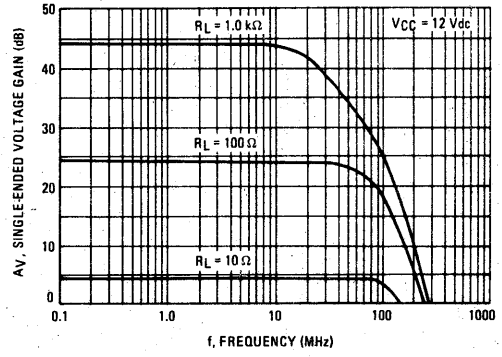


FIGURE 2 – VOLTAGE GAIN versus FREQUENCY
(Video Amplifier, See Figure 26)



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TYPICAL CHARACTERISTICS

($V_{I\ (AGC)}$ = 0, V_{CC} = 12 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 3 – DYNAMIC RANGE: OUTPUT VOLTAGE versus INPUT VOLTAGE (Video Amplifier, See Figure 26)

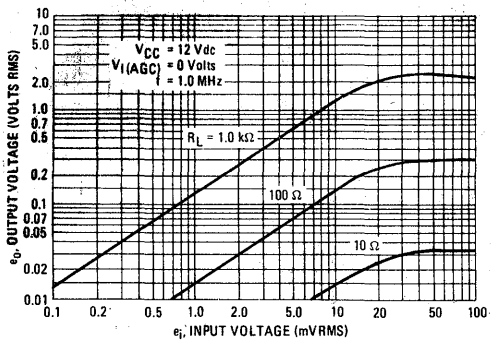


FIGURE 4 – VOLTAGE GAIN versus FREQUENCY (Video Amplifier, See Figure 26)

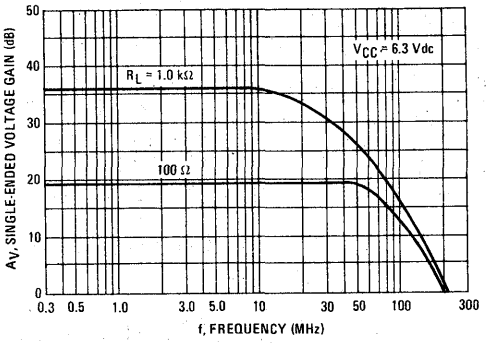


FIGURE 5 – VOLTAGE GAIN AND SUPPLY CURRENT versus SUPPLY VOLTAGE (Video Amplifier, See Figure 26)

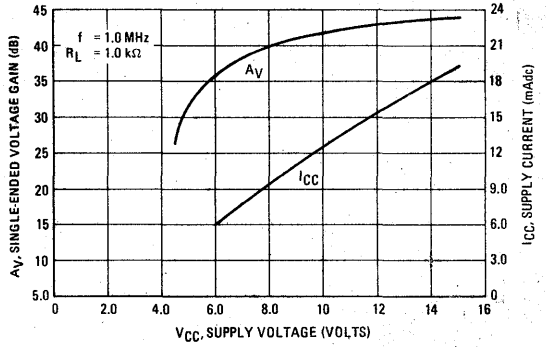


FIGURE 6 – TYPICAL GAIN REDUCTION versus AGC VOLTAGE

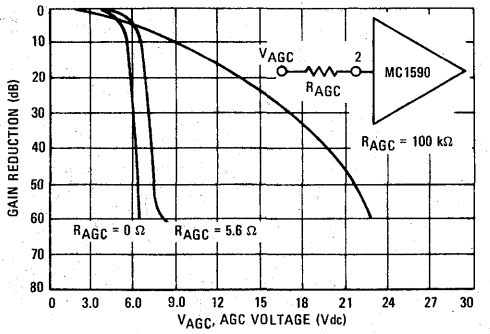


FIGURE 7 – TYPICAL GAIN REDUCTION versus AGC CURRENT

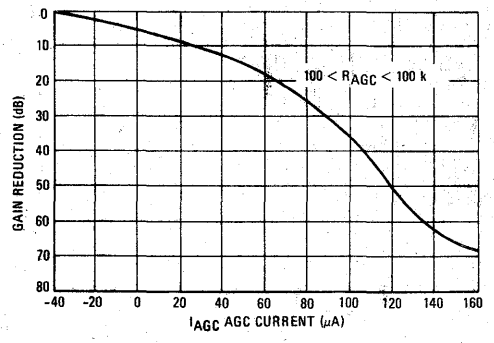
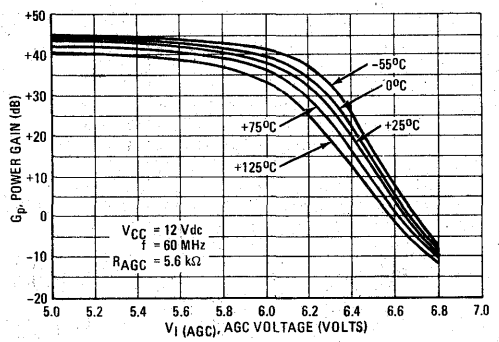


FIGURE 8 – FIXED TUNED POWER GAIN REDUCTION versus TEMPERATURE (See Test Circuit, Figure 24)



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TYPICAL CHARACTERISTICS (continued)

FIGURE 9 – POWER GAIN versus SUPPLY VOLTAGE
(See Test Circuit, Figure 24)

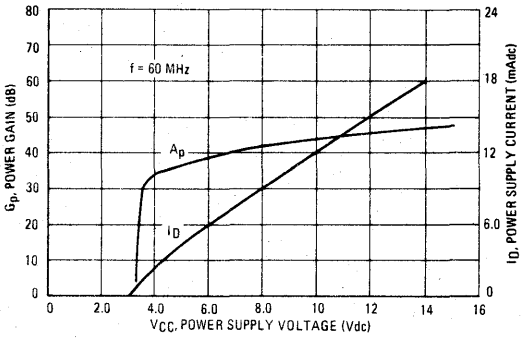


FIGURE 10 – REVERSE TRANSFER ADMITTANCE versus FREQUENCY (See Parameter Table, Page 1)

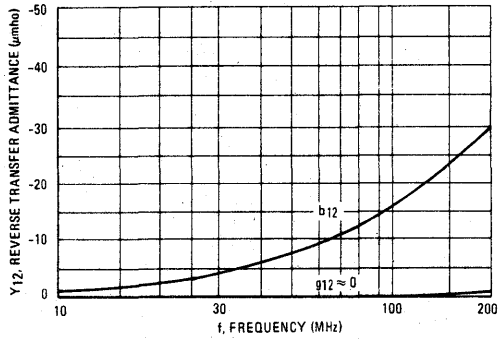


FIGURE 11 – NOISE FIGURE versus FREQUENCY

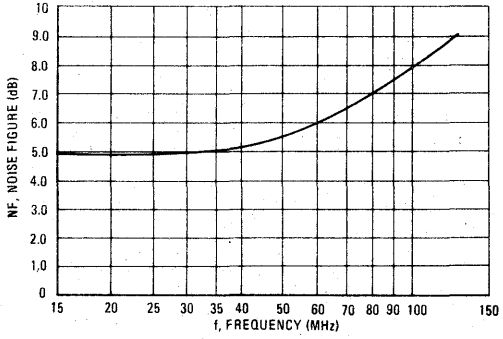


FIGURE 12 – NOISE FIGURE versus SOURCE RESISTANCE

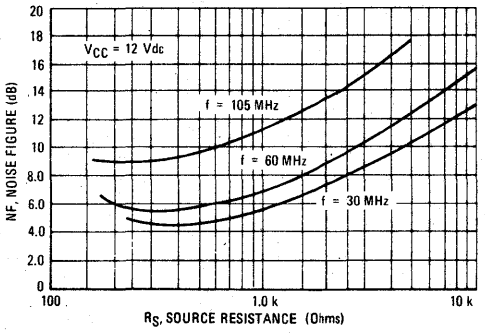
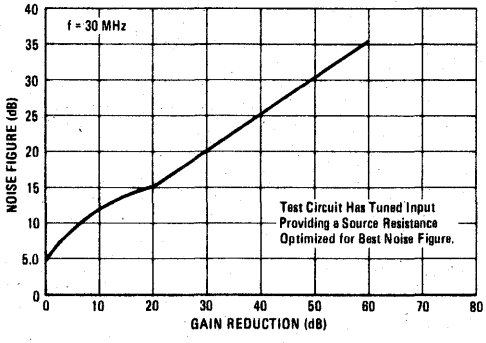


FIGURE 13 – NOISE FIGURE versus AGC GAIN REDUCTION



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TYPICAL CHARACTERISTICS (continued)

FIGURE 14 – SINGLE-ENDED OUTPUT ADMITTANCE

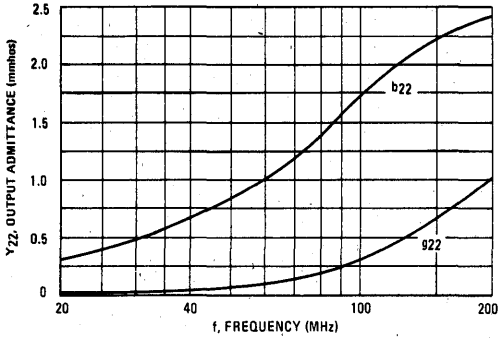


FIGURE 15 – SINGLE-ENDED INPUT ADMITTANCE

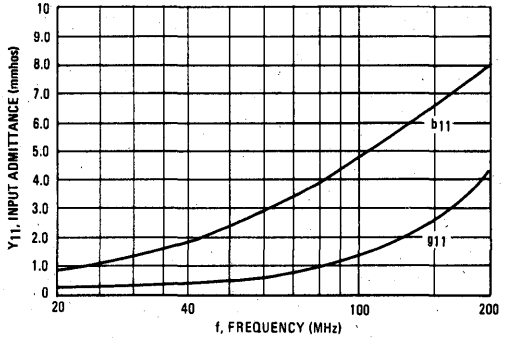


FIGURE 16 – HARMONIC DISTORTION versus AGC GAIN REDUCTION FOR AM CARRIER (For Test Circuit, See Figure 17)

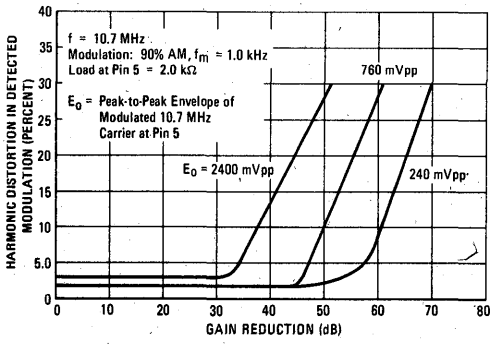


FIGURE 17 – 10.7-MHz AMPLIFIER
Gain ≃ 55 dB, BW ≃ 100 kHz

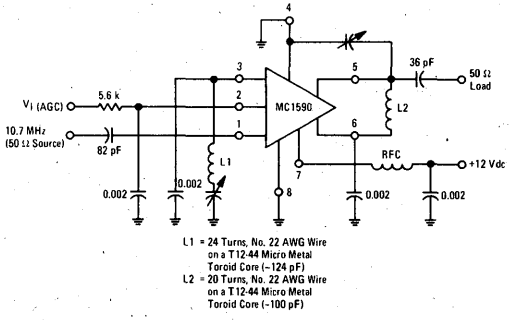


FIGURE 18 – Y_{21}, FORWARD TRANSFER ADMITTANCE RECTANGULAR FORM

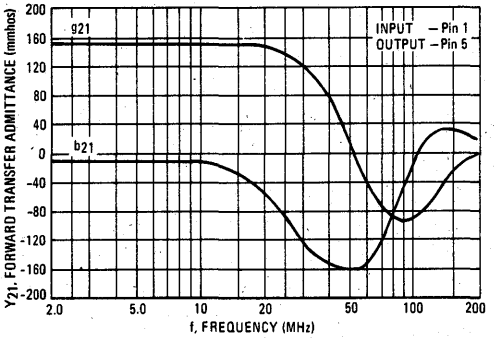
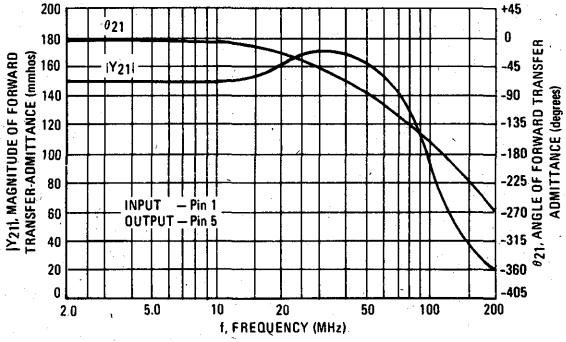


FIGURE 19 – Y_{21}, FORWARD TRANSFER ADMITTANCE POLAR FORM



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TYPICAL CHARACTERISTICS (continued)

FIGURE 20 – S_{11} AND S_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT

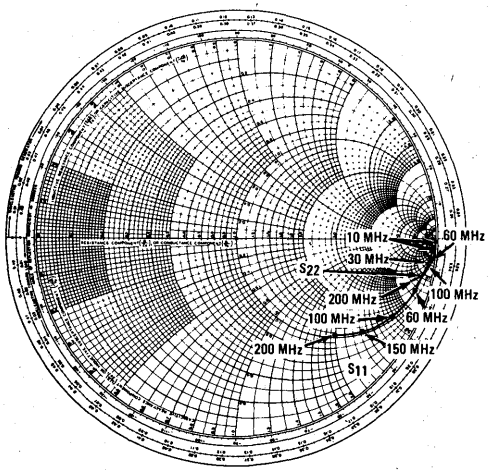


FIGURE 21 – S_{11} AND S_{22}, INPUT AND OUTPUT REFLECTION COEFFICIENT

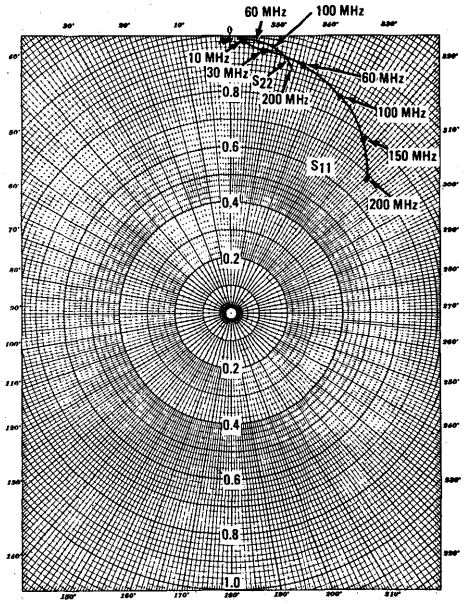


FIGURE 22 – S_{21}, FORWARD TRANSMISSION COEFFICIENT (GAIN)

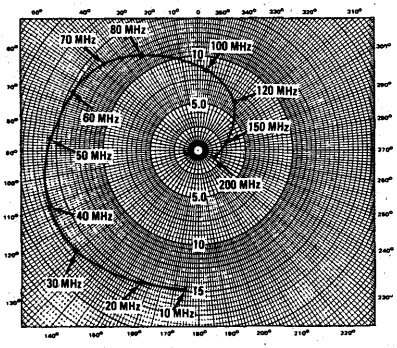
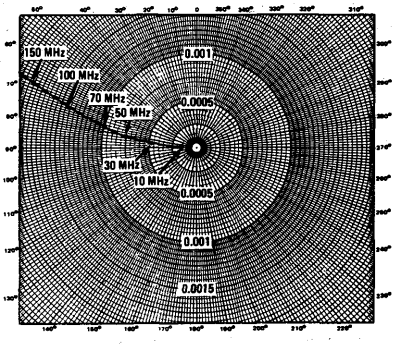


FIGURE 23 – S_{12}, REVERSE TRANSMISSION COEFFICIENT (FEEDBACK)



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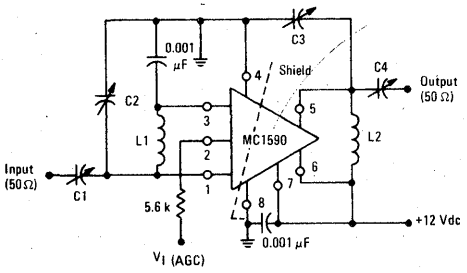
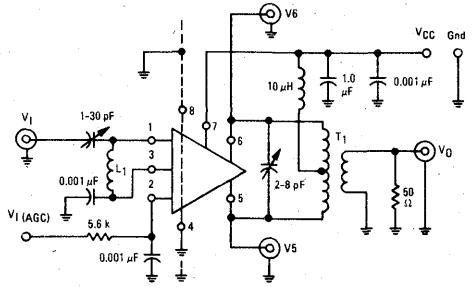
TYPICAL APPLICATIONS

FIGURE 24 – 60-MHz POWER GAIN TEST CIRCUIT



L1 = 7 Turns, #20 AWG Wire, 5/16" Dia., 5/8" Long
L2 = 6 Turns, #14 AWG Wire, 9/16" Dia., 3/4" Long
C1,C2,C3 = (1-30) pF
C4 = (1-10) pF

FIGURE 25 – DIFFERENTIAL OUTPUT VOLTAGE SWING, (V5, V6) (60 MHz)



L1: 7 Turns, # 22 AWG Wire on 5/16" Dia. Form, 5/8" Long
T1: Close Wound Over 1/4" Form
Primary Winding = 16 Turns # 26 AWG, Center Tapped
Secondary Winding = 2 Turns # 26 AWG.

FIGURE 26 – VIDEO AMPLIFIER

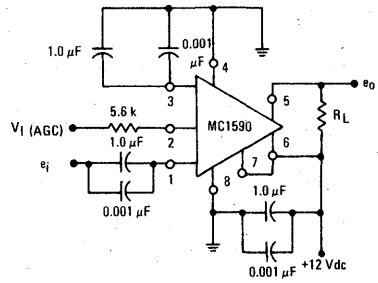
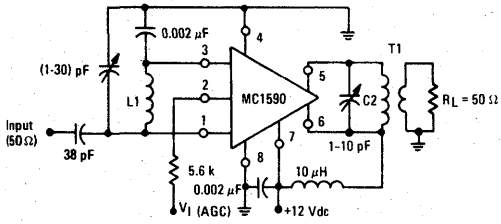
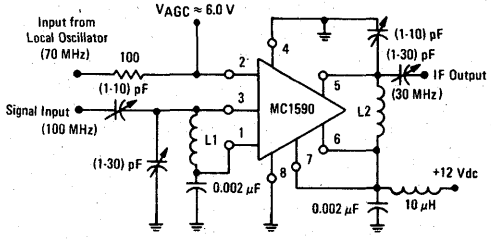


FIGURE 27 – 30-MHz AMPLIFIER (Power Gain = 50 dB, BW ≈ 1.0 MHz)



L1 = 12 Turns #22 AWG Wire on a Toroid Core, (T37-6 Micro Metal or Equiv)
T1: Primary = 17 Turns #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)
Secondary = 2 Turns #20 AWG Wire

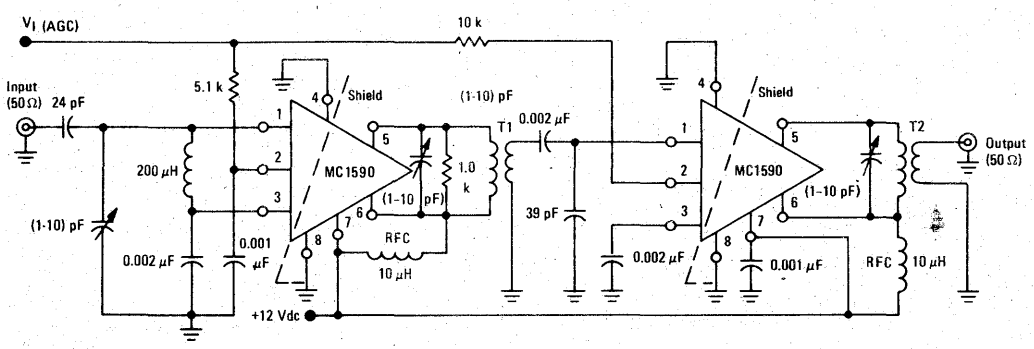
FIGURE 28 – 100-MHz MIXER



L1 = 5 Turns, #16 AWG Wire, 1/4" ID, 5/8" Long
L2 = 16 Turns, #20 AWG Wire on a Toroid Core, (T44-6 Micro Metal or Equiv)

TYPICAL APPLICATIONS (continued)

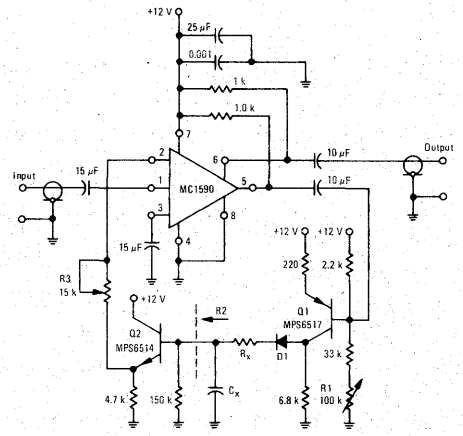
FIGURE 29 – TWO-STAGE 60 MHz IF AMPLIFIER (Power Gain ≈ 80 dB, BW ≈ 1.5 MHz)



T1: Primary Winding = 15 Turns, #22 AWG Wire, 1/4" ID Air Core
Secondary Winding = 4 Turns, #22 AWG Wire,
Coefficient of Coupling ≈ 1.0

T2: Primary Winding = 10 Turns, #22 AWG Wire, 1/4" ID Air Core
Secondary Winding = 2 Turns, #22 AWG Wire,
Coefficient of Coupling ≈ 1.0

FIGURE 30 – SPEECH COMPRESSOR



DESCRIPTION OF SPEECH COMPRESSOR

The amplifier drives the base of a PNP MPS6517 operating common-emitter with a voltage gain of approximately 20. The control R1 varies the quiescent Q point of this transistor so that varying amounts of signal exceed the level V_r. Diode D1 rectifies the positive peaks of Q1's output only when these peaks are greater than $V_r \simeq 7.0$ Volts. The resulting output is filtered by C_x, R_x.

R_x controls the charging time constant or attack time. C_x is involved in both charge and discharge. R2 (the 150 kΩ and input resistance of the emitter-follower Q2) controls the decay time. Making the decay long and attack short is accomplished by making R_x small and R2 large. (A Darlington emitter-follower may be needed if extremely slow decay times are required.)

The emitter-follower Q2 drives the AGC Pin 2 of the MC1590 and reduces the gain. R3 controls the slope of signal compression. The following graph details performance with R3 set to 15 kΩ.

FIGURE 31 – OUTPUT VOLTAGE versus INPUT VOLTAGE

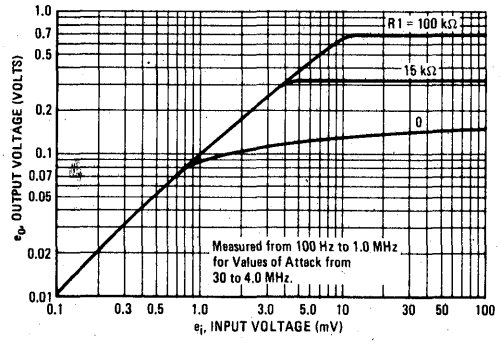


TABLE I – DISTORTION versus FREQUENCY

FREQUENCY	DISTORTION		DISTORTION	
	10 mV e_i	100 mV e_i	10 mV e_i	100 mV e_i
100 Hz	3.5%	12%	15%	27%
300 Hz	2%	10%	6%	20%
1.0 kHz	1.5%	8%	3%	9%
10 kHz	1.5%	8%	1%	3%
100 kHz	1.5%	8%	1%	3%

Decay = 300 ms
Attack = 20 ms

C_X = 7.5 μF
R_X = 0 (Short)

Decay = 20 ms
Attack = 3 ms

C_X = 0.68 μF
R_X = 1.5 kΩ

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\,(Typ)}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst-case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient

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ORDERING INFORMATION

Device	Temperature Range	Package
MC1494L	0°C to +70°C	Ceramic DIP
MC1594L	−55°C to +125°C	Ceramic DIP

MC1494L
MC1594L

Specifications and Applications Information

MONOLITHIC FOUR-QUADRANT MULTIPLIER

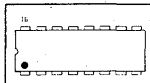
. . . designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

The MC1594/1494 is a variable transconductance multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power-supply rejection.

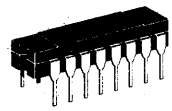
- Operates With ±15 V Supplies
- Excellent Linearity – Maximum Error (X or Y): ± 0.5% (MC1594)
  ± 1.0% (MC1494)
- Wide Input Voltage Range – ±10 volts
- Adjustable Scale Factor, K (0.1 nominal)
- Single-Ended Output Referenced to Ground
- Simplified Offset Adjust Circuitry
- Frequency Response (3 dB Small-Signal) – 1.0 MHz
- Power Supply Sensitivity – 30 mV/V typical

LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

MONOLITHIC SILICON EPITAXIAL PASSIVATED

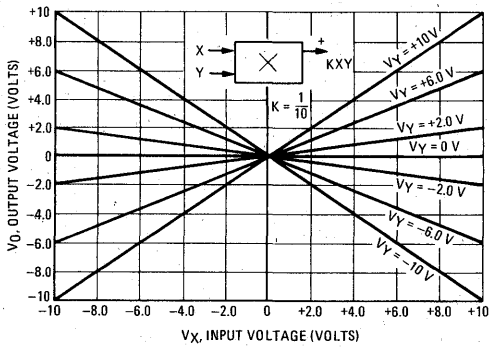


(top view)

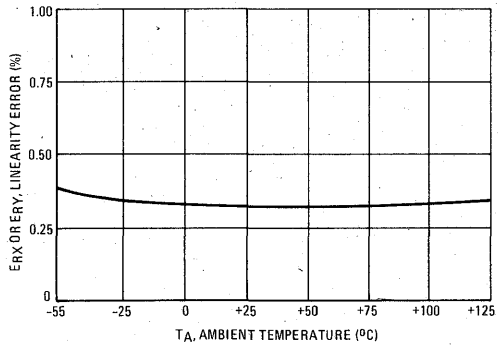


CERAMIC PACKAGE
CASE 620

FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC



TYPICAL LINEARITY ERROR versus TEMPERATURE



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CONTENTS

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+18	Vdc
	V^-	-18	
Differential Input Signal	V_9-V_6	$\pm \lvert 6+I_1 R_Y \rvert < 30$	Vdc
	$V_{10}-V_{13}$	$\pm \lvert 6+I_1 R_X \rvert < 30$	
Common-Mode Input Voltage			Vdc
$V_{CMY} = V_9 = V_6$	V_{CMY}	±11.5	
$V_{CMX} = V_{10} = V_{13}$	V_{CMX}	±11.5	
Power Dissipation (Package Limitation)			
T_A = +25°C	P_D	750	mW
Derate above T_A = +25°C	$1/\theta_{JA}$	5.0	mW/°C
Operating Temperature Range	T_A		°C
MC1594		-55 to +125	
MC1494		0 to + 70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V^+ = +15 V, V^- = -15 V, T_A = +25°C, R1 = 16 kΩ, R_X = 30 kΩ, R_Y = 62 kΩ, R_L = 47 kΩ, unless otherwise noted)

Characteristic	Fig.	Symbol	MC1594 Min	MC1594 Typ	MC1594 Max	MC1494 Min	MC1494 Typ	MC1494 Max	Unit
Linearity	1	E_{RX} or E_{RY}							%
Output error in Percent of full scale									
-10 V<V_X<+10 V (V_Y = ±10 V)									
-10 V<V_Y<+10 V (V_X = ±10 V)									
T_A = +25°C			–	± 0.3	± 0.5	–	± 0.5	± 1.0	
$T_A = T_{high}$ ①			–	–	± 0.8	–	–	± 1.3	
$T_A = T_{low}$ ②			–	–	± 0.8	–	–	± 1.3	
Input	2,3,4								
Voltage Range ($V_X = V_Y = V_{in}$)		V_{in}	±10	–	–	±10	–	–	V_{pk}
Resistance (X or Y Input)		R_{in}	–	300	–	–	300	–	MΩ
Offset Voltage (X Input) (Note 1)		$\lvert V_{iox} \rvert$	–	0.1	1.6	–	0.2	2.5	V
(Y Input) (Note 1)		$\lvert V_{ioy} \rvert$	–	0.4	1.6	–	0.8	2.5	
Bias Current (X or Y Input)		I_b	–	0.5	1.5	–	1.0	2.5	μA
Offset Current (X or Y Input)		$\lvert I_{io} \rvert$	–	28	150	–	50	400	nA
Output	3,4								
Voltage Swing Capability		V_o	±10	–	–	±10	–	–	V_{pk}
Impedance		R_o	–	850	–	–	850	–	kΩ
Offset Voltage (Note 1)		$\lvert V_{oo} \rvert$	–	0.8	1.6	–	1.2	2.5	V
Offset Current (Note 1)		$\lvert I_{oo} \rvert$	–	17	34	–	25	52	μA
Temperature Stability (Drift)									
$T_A = T_{high}$ to T_{low}									
Output Offset (X = 0, Y = 0) Voltage		$\lvert TCV_{oo} \rvert$	–	1.3	–	–	1.3	–	mV/°C
Current		$\lvert TCI_{oo} \rvert$	–	27	–	–	27	–	nA/°C
X Input Offset (Y = 0)		$\lvert TCV_{iox} \rvert$	–	0.3	–	–	0.3	–	mV/°C
Y Input Offset (X = 0)		$\lvert TCV_{ioy} \rvert$	–	1.5	–	–	1.5	–	
Scale Factor		$\lvert TCK \rvert$	–	0.07	–	–	0.07	–	%/°C
Total dc Accuracy Drift (X = 10, Y = 10)		$\lvert TCE \rvert$	–	0.09	–	–	0.09	–	
Dynamic Response	5								
Small Signal (3 dB) X		$BW_{3\,dB}(X)$	–	0.8	–	–	0.8	–	MHz
Y		$BW_{3\,dB}(Y)$	–	1.0	–	–	1.0	–	
Power Bandwidth (47 k)		P_{BW}	–	440	–	–	440	–	kHz
3° Relative Phase Shift		$f\phi$	–	240	–	–	240	–	
1% Absolute Error		$f\theta$	–	30	–	–	30	–	
Common Mode	6								
Input Swing (X or Y)		CMV	±10.5	–	–	±10.5	–	–	V_{pk}
Gain (X or Y)		A_{CM}	–	-65	–	–	-65	–	dB
Power Supply	7								
Current		I_d^+	–	6.0	9.0	–	6.0	12	mAdc
		I_d^-	–	6.5	9.0	–	6.5	12	
Quiescent Power Dissipation		P_d	–	185	260	–	185	350	mW
Sensitivity		S^+	–	13	50	–	13	100	mV/V
		S^-	–	30	100	–	30	200	
Regulated Offset Adjust Voltages	7								
Positive		V_R^+	+3.5	+4.3	+5.0	+3.5	+4.3	+5.0	Vdc
Negative		V_R^-	-3.5	-4.3	-5.0	-3.5	-4.3	-5.0	
Temperature Coefficient (V_R^+ or V_R^-)		TCV_R	–	0.03	–	–	0.03	–	mV/°C
Power Supply Sensitivity (V_R^+ or V_R^-)		S_R^+, S_R^-	–	0.6	–	–	0.6	–	mV/V

Note 1: Offsets can be adjusted to zero with external potentiometers.

① T_{high} = +125°C for MC1594, + 70°C for MC1494 ② T_{low} = -55°C for MC1594, 0°C for MC1494

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TEST CIRCUITS

FIGURE 1 – LINEARITY

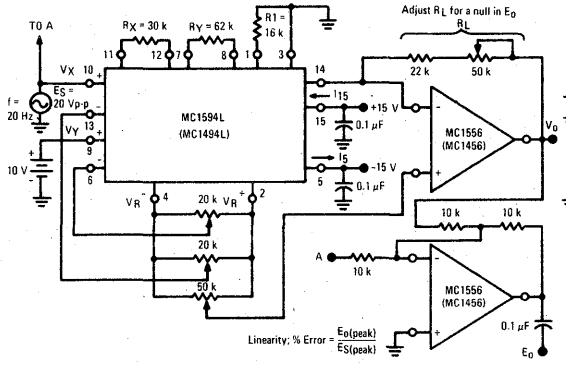


FIGURE 2 – INPUT RESISTANCE

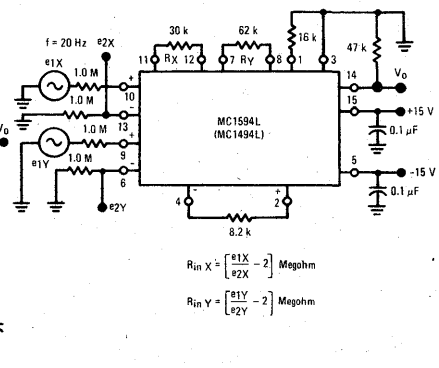


FIGURE 3 – OFFSET VOLTAGES, GAIN

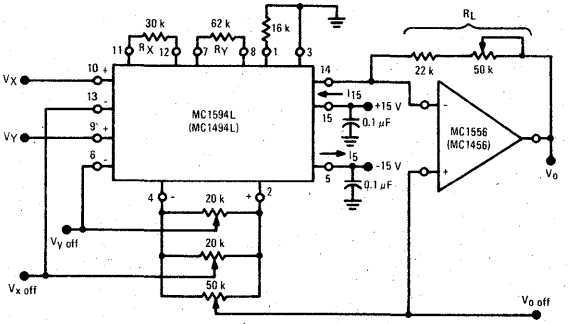


FIGURE 4 – INPUT BIAS CURRENT/INPUT OFFSET CURRENT, OUTPUT RESISTANCE

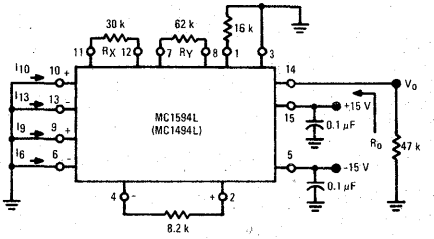


FIGURE 5 – FREQUENCY RESPONSE

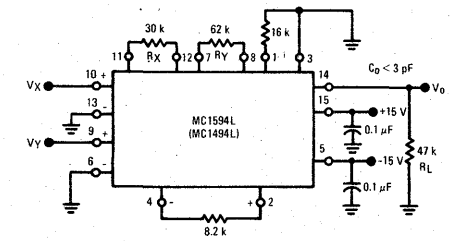


FIGURE 6 – COMMON-MODE

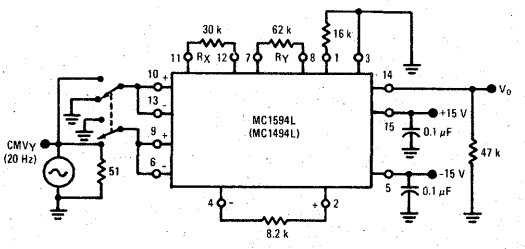


FIGURE 7 – POWER-SUPPLY SENSITIVITY

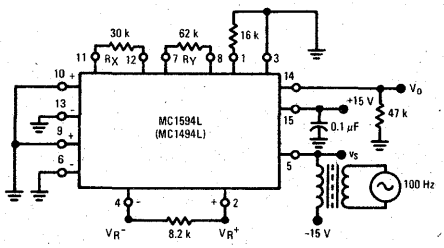
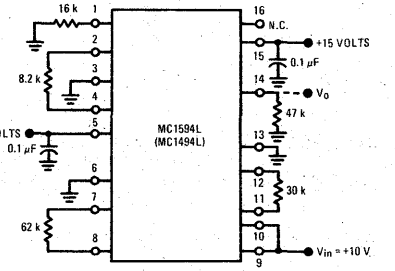


FIGURE 8 – BURN-IN



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TYPICAL CHARACTERISTICS

(Unless otherwise noted, $V^+ = +15$ V, $V^- = -15$ V, R1 = 16 kΩ, $R_X = 30$ kΩ, $R_Y = 62$ kΩ, $R_L = 47$ kΩ, $T_A = +25^oC$)

FIGURE 9 – FREQUENCY RESPONSE OF Y INPUT versus LOAD RESISTANCE

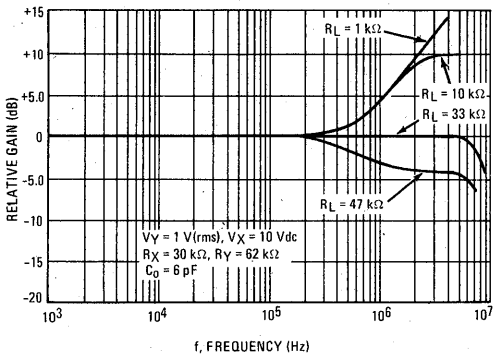


FIGURE 10 – FREQUENCY RESPONSE OF X INPUT versus LOAD RESISTANCE

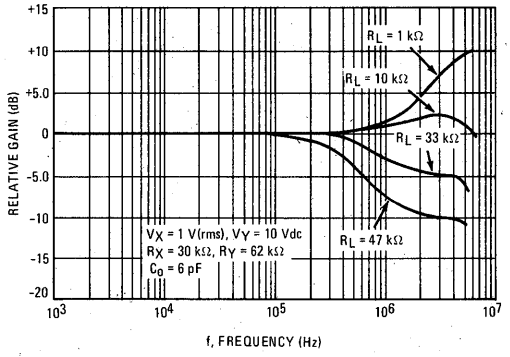


FIGURE 11 – LARGE SIGNAL VOLTAGE versus FREQUENCY

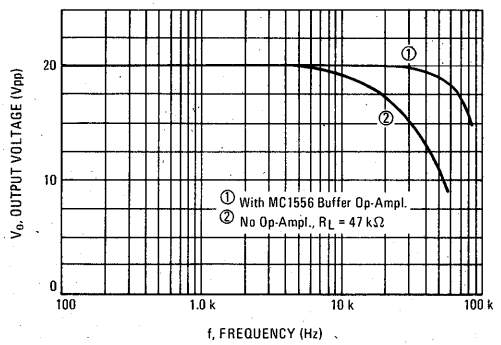


FIGURE 12 – LINEARITY versus R_X OR R_Y WITH K = 1/10

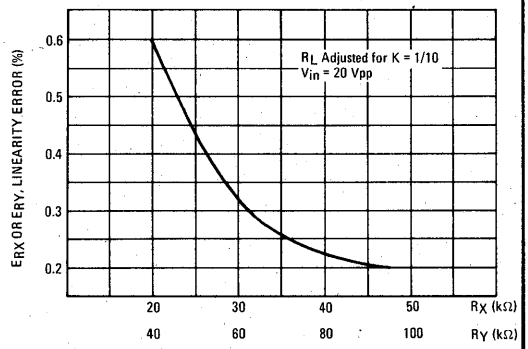


FIGURE 13 – LINEARITY versus R_X OR R_Y WITH K = 1

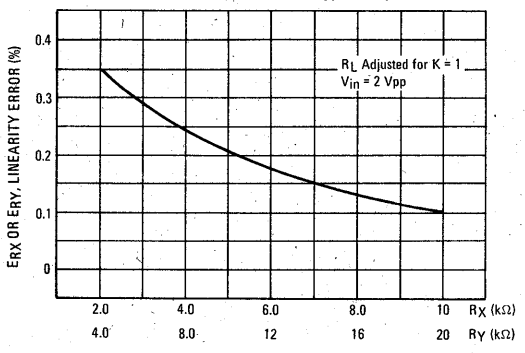
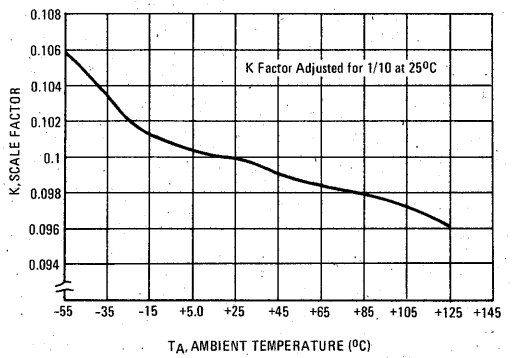


FIGURE 14 – SCALE FACTOR (K) versus TEMPERATURE



8

GENERAL INFORMATION

1. CIRCUIT DESCRIPTION

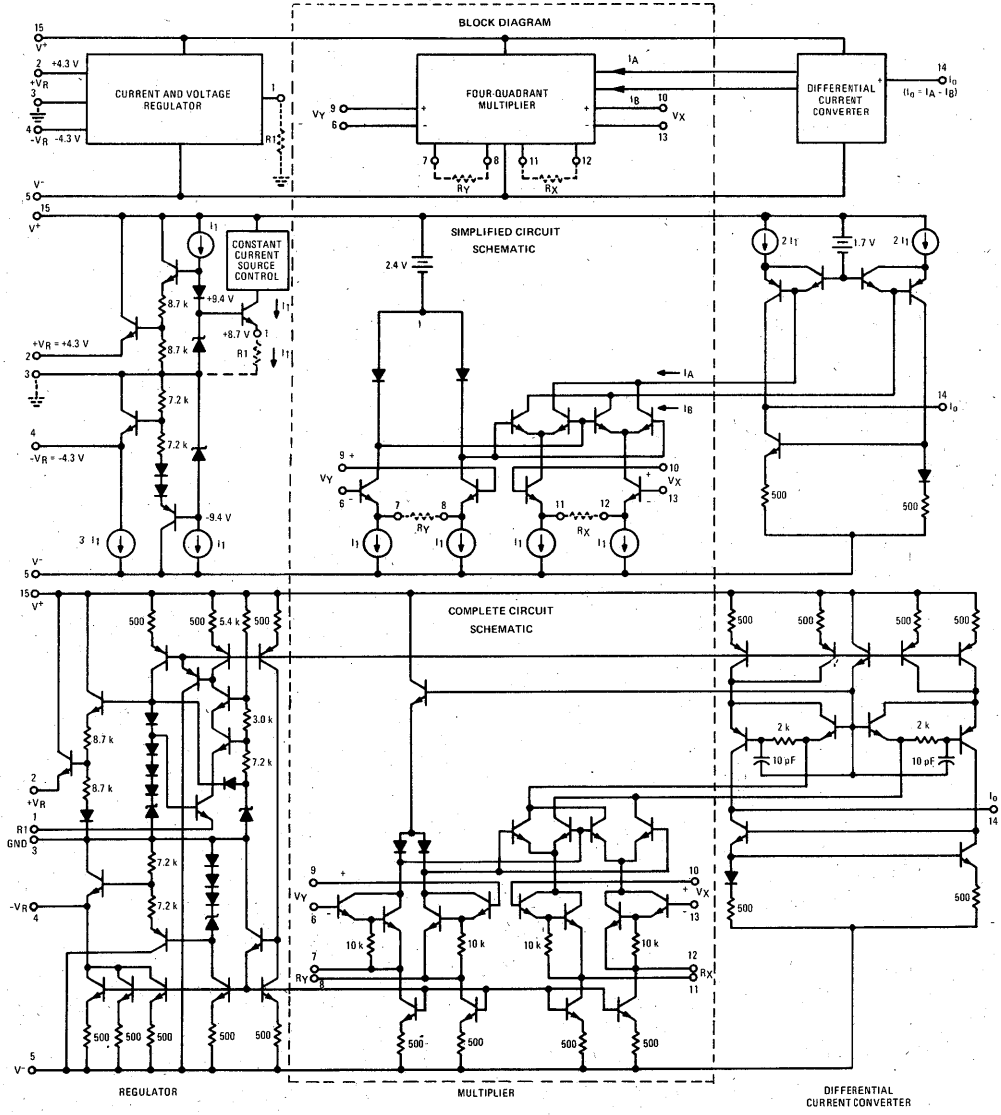
1.1 Introduction

The MC1594 is a monolithic, four-quadrant multiplier that operates on the principle of variable transconductance. It features a single-ended current output referenced to ground and provides two complementary regulated voltages for use with the offset adjust circuits to virtually eliminate sensitivity of the offset voltage nulls to changes in supply voltage.

As shown in Figure 15, the MC1594 consists of a multiplier proper and associated peripheral circuitry to provide these features.

FIGURE 15

(Recommended External Circuitry is Depicted With Dotted Lines)



1.2 Regulator (Figure 15)

The regulator biases the entire MC1594 circuit making it essentially independent of supply variation. It also provides two convenient regulated supply voltages which can be used in the offset adjust circuitry. The regulated output voltage at pin 2 is approximately +4.3 V while the regulated voltage at pin 4 is approximately -4.3 V. For optimum temperature stability of these regulated voltages, it is recommended that $|I_2| = |I_4| = 1.0$ mA (equivalent load of 8.6 kΩ). As will be shown later, there will normally be two 20 k-ohm potentiometers and one 50 k-ohm potentiometer connected between pins 2 and 4.

The regulator also establishes a constant current reference that controls all of the constant current sources in the MC1594. Note that all current sources are related to current I_1 which is determined by R1. For best temperature performance, R1 should be 16 kΩ so that $I_1 \approx 0.5$ mA for all applications.

1.3 Multiplier (Figure 15)

The multiplier section of the MC1594 (center section of Figure 15) is nearly identical to the MC1595 and is discussed in detail in Application Note AN-489, "Analysis and Basic Operation of the MC1595". The result of this analysis is that the differential output current of the multiplier is given by:

$$I_A - I_B = \Delta I \approx \frac{2V_X V_Y}{R_X R_Y I_1}$$

Therefore, the output is proportional to the product of the two input voltages.

1.4 Differential Current Converter (Figure 15)

This portion of the circuitry converts the differential output current (I_A-I_B) of the multiplier to a single-ended output current (I_o):

$$I_o = I_A - I_B$$

or

$$I_o = \frac{2V_X V_Y}{R_X R_Y I_1}$$

The output current can be easily converted to an output voltage by placing a load resistor R_L from the output (pin 14) to ground (Figure 17) or by using an op-ampl. as a current-to-voltage converter (Figure 16). The result in both circuits is that the output voltage is given by:

$$V_o = \frac{2R_L V_X V_Y}{R_X R_Y I_1} = KV_X V_Y$$

where K (scale factor) $= \frac{2R_L}{R_X R_Y I_1}$

2. DC OPERATION

2.1 Selection of External Components

For low frequency operation the circuit of Figure 16 is recommended. For this circuit, $R_X = 30$ kΩ, $R_Y = 62$ kΩ, R1 = 16 kΩ and hence $I_1 \approx 0.5$ mA. Therefore, to set the scale factor, K, equal to 1/10, the value of R_L can be calculated to be:

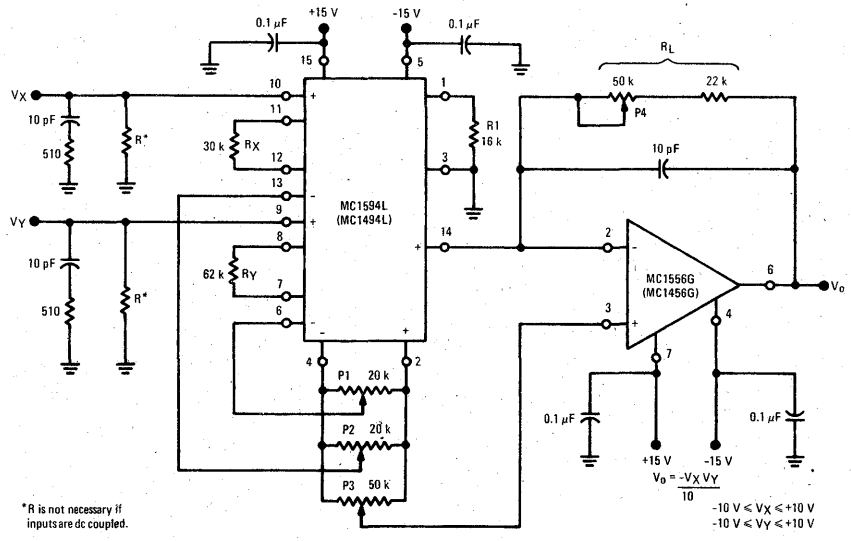
$$K = \frac{1}{10} = \frac{2R_L}{R_X R_Y I_1}$$

or $$R_L = \frac{R_X R_Y I_1}{(2)(10)} = \frac{(30\text{ k})(62\text{ k})(0.5\text{ mA})}{20}$$

$$R_L = 46.5\text{ k}$$

Thus, a reasonable accuracy in scale factor can be achieved by making R_L a fixed 47 kΩ resistor. However, if it is desired

FIGURE 16 – TYPICAL MULTIPLIER CONNECTION



that the scale factor be exact, R_L can be comprised of a fixed resistor and a potentiometer as shown in Figure 16. It should be pointed out that there is nothing magic about setting the scale factor to 1/10. This is merely a convenient factor to use if the V_X and V_Y input voltages are expected to be large, say ±10 V. Obviously with $V_X = V_Y = 10$ V and a scale factor of unity, the device could not hope to provide a 100 V output, so the scale factor is set to 1/10 and provides an output scaled down by a factor of ten. For many applications it may be desirable to set K = 1/2 or K = 1 or even K = 100. This can be accomplished by adjusting R_X, R_Y and R_L appropriately.

The selection of R_L is arbitrary and can be chosen after resistors R_X and R_Y are found. Note in Figure 16 that R_Y is 62 kΩ while R_X is 30 kΩ. The reason for this is that the "Y" side of the multiplier exhibits a second order non-linearity whereas the "X" side exhibits a simple non-linearity. By making the R_Y resistor approximately twice the value of the R_X resistor, the linearity on both the "X" and "Y" sides are made equal. The selection of the R_X and R_Y resistor values is dependent upon the expected amplitude of V_X and V_Y inputs. To maintain a specified linearity, resistors R_X and R_Y should be selected according to the following equations:

$$R_X \geq 3\ V_X \text{ (max) in k}\Omega \text{ when } V_X \text{ is in volts}$$

$$R_Y \geq 6\ V_Y \text{ (max) in k}\Omega \text{ when } V_Y \text{ is in volts}$$

For example, if the maximum input on the "X" side is ±1 volt, resistor R_X can be selected to be 3 kΩ. If the maximum input on the "Y" side is also ±1 volt, then resistor R_Y can be selected to be 6 kΩ (6.2 kΩ nominal value). If a scale factor of K = 10 is desired, the load resistor is found to be 47 kΩ. In this example, the multiplier provides a gain of 20 dB.

2.2 Operational Amplifier Selection

The operational amplifier connection in Figure 16 is a simple but extremely accurate current-to-voltage converter. The output current of the multiplier flows through the feedback resistor R_L to provide a low impedance output voltage from the op-ampl. Since the offset current and bias currents of the op-ampl. will cause errors in the output voltage, particularly with temperature, one with very low bias and offset currents is recommended. The MC1556/MC1456 or MC1741/MC1741C are excellent choices for this application.

Since the MC1594 is capable of operation at much higher frequencies than the op-ampl., the frequency characteristics of the circuit in Figure 16 will be primarily dependent upon the op-ampl.

2.3 Stability

The current-to-voltage converter mode is a most demanding application for an operational amplifier. Loop gain is at its maximum and the feedback resistor in conjunction with stray or input capacitance at the multiplier output adds additional phase shift. It may therefore be necessary to add (particularly in the case of internally compensated op-ampls.) a small feedback capacitor to reduce loop gain at the higher frequencies. A value of 10 pF in parallel with R_L should be adequate to insure stability over production and temperature variations, etc.

An externally compensated op-ampl. might be employed using slightly heavier compensation than that recommended for unity-gain operation.

2.4 Offset Adjustment

The non-inverting input of the op-ampl. provides a convenient point to adjust the output offset voltage. By connecting this point to the wiper arm of a potentiometer (P3), the output offset voltage can be adjusted to zero (see offset and scale factor adjustment procedure).

The input offset adjustment potentiometers, P1 and P2 will be necessary for most applications where it is desirable to take advantage of the multiplier's excellent linearity characteristics. Depending upon the particular application, some of the potentiometers can be omitted (see Figures 17, 19, 22, 24 and 25).

2.5 Offset and Scale Factor Adjustment Procedure

The adjustment procedure for the circuit of Figure 16 is:

A. X Input Offset
   (a) connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 9)
   (b) connect "X" input (pin 10) to ground
   (c) adjust X-offset potentiometer, P2 for an ac null at the output

B. Y Input Offset
   (a) connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 10)
   (b) connect "Y" input (pin 9) to ground
   (c) adjust Y-offset potentiometer, P1 for an ac null at the output

C. Output Offset
   (a) connect both "X" and "Y" inputs to ground
   (b) adjust output offset potentiometer, P3, until the output voltage V_O, is zero volts dc

D. Scale Factor
   (a) apply +10 Vdc to both the "X" and "Y" inputs
   (b) adjust P4 to achieve -10.00 V at the output
   (c) apply -10 Vdc to both "X" and "Y" inputs and check for V_O = -10.00 V

E. Repeat steps A through D as necessary.

The ability to accurately adjust the MC1594 is dependent on the offset adjust potentiometers. Potentiometers should be of the "infinite" resolution type rather than wirewound. Fine adjustments in balanced-modulator applications may require two potentiometers to provide "coarse" and "fine" adjustment. Potentiometers should have low temperature coefficients and be free from backlash.

2.6 Temperature Stability

While the MC1594 provides excellent performance in itself, overall performance depends to a large degree on the quality of the external components. Previous discussion shows the direct dependence on R_X, R_Y, and R_L and indirect dependence on R1 (through I_1). Any circuit subjected to temperature variations should be evaluated with these effects in mind.

2.7 Bias Currents

The MC1594 multiplier, like most linear IC's, requires a dc bias current into its input terminals. The device cannot be capacitively coupled at the input without regard for this bias current. If inputs V_X and V_Y are able to supply the small bias current ($\approx 0.5\ \mu A$) resistors, R (Figure 16) can be omitted. If the MC1594 is used in an ac mode of operation and capacitive coupling is used the value of resistor R can be any reasonable value up to 100 kΩ. For minimum noise and optimum temperature performance, the value of resistor R should be as low as practical.

2.8 Parasitic Oscillation

When long leads are used on the inputs, oscillation may occur. In this event, an RC parasitic suppression network similar to the ones shown in Figure 16 should be connected directly to each input using short leads. The purpose of the network

is to reduce the "Q" of the source-tuned circuits which cause the oscillation.

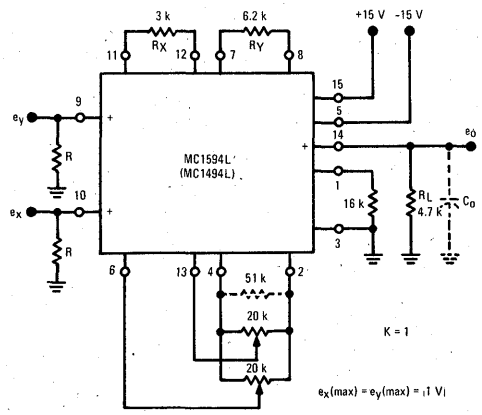
Inability to adjust the circuit to within the specified accuracy may be an indication of oscillation.

3. AC OPERATION

3.1 General

For ac operation, such as balanced modulation, frequency doubler, AGC, etc., the op-ampl. will usually be omitted as well as the output offset adjust potentiometer. The output offset adjust potentiometer is omitted since the output will normally be ac-coupled and the dc voltage at the output is of no concern providing it is close enough to zero volts that it will not cause clipping in the output waveform. Figure 17

FIGURE 17 – WIDEBAND MULTIPLIER



shows a typical ac multiplier circuit with a scale factor K≈1. Again, resistor R_X and R_Y are chosen as outlined in the previous section, with R_L chosen to provide the required scale factor.

The offset voltage then existing at the output will be equal to the offset current times the load resistance. The output offset current of the MC1594 is typically 17 μA and 35 μA maximum. Thus, the maximum output offset would be about 160 mV.

3.2 Bandwidth

The bandwidth of the MC1594 is primarily determined by two factors. First, the dominant pole will be determined by the load resistor and the stray capacitance at the output terminal. For the circuit shown in Figure 17, assuming a total output capacitance (C_o) of 10 pF, the 3 dB bandwidth would be approximately 3.4 MHz. If the load resistor were 47 kΩ, the bandwidth would be approximately 340 kHz.

Secondly, a "zero" is present in the frequency response characteristic for both the "X" and "Y" inputs which causes the output signal to rise in amplitude at a 6 dB/octave slope at frequencies beyond the breakpoint of the "zero". The "zero" is caused by the parasitic and substrate capacitance which is related to resistors R_X and R_Y and the transistors associated with them. The effect of these transmission "zeros" is seen in Figures 9 and 10. The reason for this increase in gain is due to the bypassing of R_X and R_Y at high frequencies. Since the R_Y resistor is approximately twice the value of the R_X resistor, the zero associated with the "Y" input will occur at approximately one octave below the zero associated with the "X" input. For R_X = 30 kΩ and R_Y = 62 kΩ, the zeros occur at 1.5 MHz for the "X" input and 700 kHz for the "Y" input. These two measured breakpoints correspond to a shunt capacitance of about 3.5 pF. Thus, for the circuit of Figure 17, the "X" input zero and "Y" input zero will be at approximately 15 MHz and 7 MHz respectively.

It should be noted that the MC1594 multiplies in the time domain, hence, its frequency response is found by means of complex convolution in the frequency (Laplace) domain. This means that if the "X" input does not involve a frequency, it is not necessary to consider the "X" side frequency response in the output product. Likewise, for the "Y" side. Thus, for applications such as a wideband linear AGC amplifier which has a dc voltage as one input, the multiplier frequency response has one zero and one pole. For applications which involve an ac voltage on both the "X" and "Y" side, such as a balanced modulator, the product voltage response will have two zeros and one pole, hence, peaking may be present in the output.

From this brief discussion, it is evident that for ac applications; (1) the value of resistors R_X, R_Y and R_L should be kept as small as possible to achieve maximum frequency response, and (2) it is possible to select a load resistor R_L such that the dominant pole (R_L, C_o) cancels the input zero (R_X, 3.5 pF or R_Y, 3.5 pF) to give a flat amplitude characteristic with frequency. This is shown in Figures 9 and 10. Examination of the frequency characteristics of the "X" and "Y" inputs will demonstrate that for wideband amplifier applications, the best tradeoff with frequency response and gain is achieved by using the "Y" input for the ac signal.

For ac applications requiring bandwidths greater than those specified for the MC1594, two other devices are recommended. For modulator-demodulator applications, the MC1596 may be used up to 100 MHz. For wideband multiplier applications, the MC1595 (using small collector loads and ac coupling) can be used.

3.3 Slew-Rate

The MC1594 multiplier is not slew-rate limited in the ordinary sense that an op-ampl. is. Since all the signals in the multiplier are currents and not voltages, there is no charging and discharging of stray capacitors and thus no limitations beyond the normal device limitations. However, it should be noted that the quiescent current in the output transistors is 0.5 mA and thus the maximum rate of change of the output voltage is limited by the output load capacitance by the simple equation:

$$\text{Slew-Rate } \frac{\Delta V_o}{\Delta T} = \frac{I_o}{C}$$

Thus, if C_o is 10 pF, the maximum slew-rate would be:

$$\frac{\Delta V_o}{\Delta T} = \frac{0.5 \times 10^{-3}}{10 \times 10^{-12}} = 50 \text{ V}/\mu\text{s}$$

This can be improved if necessary by addition of an emitter-follower or other type of buffer.

3.4 Phase-Vector Error

All multipliers are subject to an error which is known as the phase-vector error. This error is a phase error only and does not contribute an amplitude error per se. The phase-vector

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error is best explained by an example. If the "X" input is described in vector notation as

$$X = A \angle 0^o$$

and the "Y" input is described as

$$Y = B \angle 0^o$$

then the output product would be expected to be

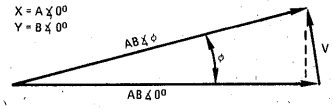
$$V_o = AB \angle 0^o \text{ (see Figure 18)}$$

However, due to a relative phase shift between the "X" and "Y" channels, the output product will be given by

$$V_o = AB \angle \phi$$

Notice that the magnitude is correct but the phase angle of the product is in error. The vector, V, associated with this error is the "phase-vector error". The startling fact about the phase-vector error is that it occurs and accumulates much more rapidly than the amplitude error associated with frequency response. In fact, a relative phase shift of only 0.57° will result in a 1% phase-vector error. For most applications, this error is meaningless. If phase of the output product is not important, then neither is the phase-vector error. If phase is important, such as in the case of double sideband modulation or demodulation, then a 1% phase-vector error will represent a 1% amplitude error at the phase angle of interest.

FIGURE 18 – PHASE-VECTOR ERROR



3.5 Circuit Layout

If wideband operation is desired, careful circuit layout must be observed. Stray capacitance across R_X and R_Y should be avoided to minimize peaking (caused by a zero created by the parallel RC circuit).

4. DC APPLICATIONS

4.1 Squaring Circuit

If the two inputs are connected together, the resultant function is squaring:

$$V_o = KV^2$$

where K is the scale factor (see Figure 19).

However, a more careful look at the multiplier's defining equation will provide some useful information. The output voltage, without initial offset adjustments is given by:

$$V_o = K(V_x + V_{iox} - V_{x\,off})(V_y + V_{ioy} - V_{y\,off}) + V_{oo}$$

(See "Definitions" for an explanation of terms).

With $V_x = V_y = V$ (squaring) and defining

$$\epsilon_x = V_{iox} - V_{x\,off}$$

$$\epsilon_y = V_{ioy} - V_{y\,off}$$

The output voltage equation becomes

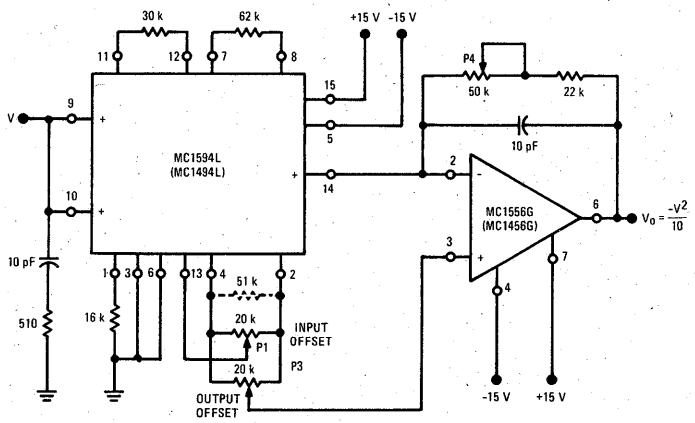
$$V_o = K V_x^2 + KV_x(\epsilon_x + \epsilon_y) + K\epsilon_x\epsilon_y + V_{oo}$$

This shows that all error terms can be eliminated with only three adjustment potentiometers, eliminating one of the input offset adjustments. For instance, if the "X" input offset adjustment is eliminated, ϵ_x is determined by the internal offset, V_{iox}, but ϵ_y is adjustable to the extent that the $(\epsilon_x + \epsilon_y)$ term can be zeroed. Then the output offset adjustment is used to adjust the V_{oo} term and thus zero the remaining error terms. An ac procedure for nulling with three adjustments is:

A. AC Procedure:

1. Connect oscillator (1 kHz, 15 Vpp) to input
2. Monitor output at 2 kHz with tuned voltmeter and adjust P4 for desired gain (Be sure to peak response of voltmeter)
3. Tune voltmeter to 1 kHz and adjust P1 for a minimum output voltage
4. Ground input and adjust P3 (output offset) for zero volts dc out
5. Repeat steps 1 through 4 as necessary.

FIGURE 19 – MC1594 SQUARING CIRCUIT



B. DC Procedure:

1. Set $V_X = V_Y = 0$ V and adjust P3 (output offset potentiometer) such that $V_o = 0.0$ Vdc
2. Set $V_X = V_Y = 1.0$ V and adjust P1 (Y input offset potentiometer) such that the output voltage is -0.100 volts
3. Set $V_X = V_Y = 10$ Vdc and adjust P4 (load resistor) such that the output voltage is -10.00 volts
4. Set $V_X = V_Y = -10$ Vdc and check that $V_O = -10$V Repeat steps 1 through 4 as necessary.

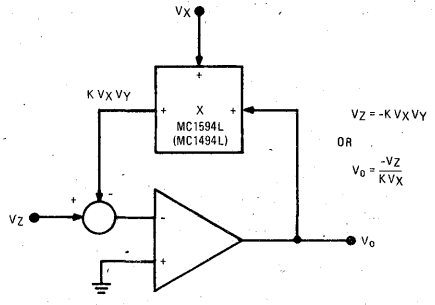
4.2 Divide

Divide circuits warrant a special discussion as a result of their special problems. Classic feedback theory teaches that if a multiplier is used as a feedback element in an operational amplifier circuit, the divide function results. Figure 20 illustrates the theoretical simplicity of such an approach and a practical realization is shown in Figure 21.

The characteristic "failure" mode of the divide circuit is latch-up. One way it can occur is if V_X is allowed to go negative or, in some cases, if V_X approaches zero.

Figure 20 illustrates why this is so. For $V_X > 0$ the transfer function through the multiplier is non-inverting. Its output is fed to the inverting input of the op-ampl. Thus, operation is in the negative feedback mode and the circuit is dc stable. Should V_X change polarity, the transfer function through the multiplier becomes inverting, the amplifier has positive feedback and latch-up results. The problem resulting from

FIGURE 20 – BASIC DIVIDE CIRCUIT USING MULTIPLIER



V_X being near zero is a result of the transfer through the multiplier being near zero. The op-ampl. is then operating with a very high closed loop gain and error voltages can thus become effective in causing latch-up.

The other mode of latch-up results from the output voltage of the op-ampl. exceeding the rated common-mode input voltage of the multiplier. The input stage of the multiplier becomes saturated, phase reversal results, and the circuit is latched up. The circuit of Figure 21 protects against this happening by clamping the output swing of the op-ampl. to approximately ±10.7 volts. Five-percent tolerance, 10-volt zeners are used to assure adequate output swing but still limit the output voltage of the op-ampl. from exceeding the common-mode input range of the MC1594.

Setting up the divide circuit for reasonably accurate operation is somewhat different from the procedure for the multiplier itself. One approach, however, is to break the feedback loop, null out the multiplier circuit, and then close the loop.

A simpler approach, since it does not involve breaking the loop (thus making it more practical on a production basis), is:

1. Set $V_Z = 0$ volts and adjust the output offset potentiometer (P3) until the output voltage (V_o) remains at some (not necessarily zero) constant value as V_X is varied between +1.0 volt and +10 volts.
2. Maintain V_Z at 0 volts, set V_X at +10 volts and adjust the Y input offset potentiometer (P1) until $V_o = 0$ volts.
3. With $V_X = V_Z$, adjust the X input offset potentiometer (P2) *until the output voltage remains at some* (not necessarily -10 volts) constant value as $V_Z = V_X$ is varied between +1.0 volt and +10 volts.
4. Maintain $V_X = V_Z$ and adjust the scale factor potentiometer (R_L) until the average value of V_o is -10 volts as $V_Z = V_X$ is varied between +1.0 volt and +10 volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

Users of the divide circuit should be aware that the accuracy to be expected decreases in direct proportion to the denomi-

FIGURE 21 – PRACTICAL DIVIDE CIRCUIT

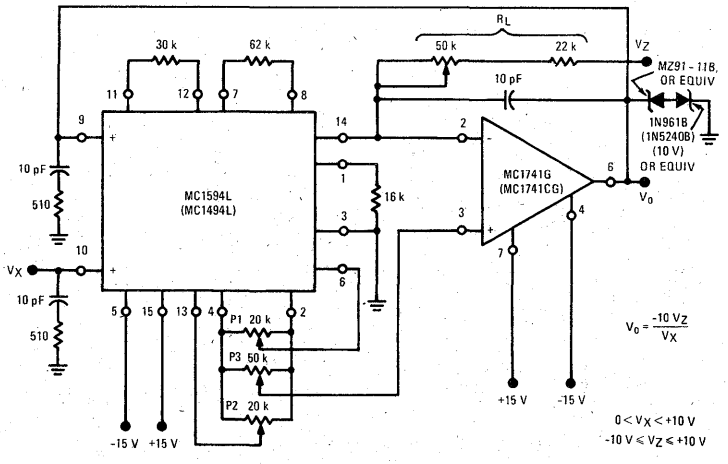
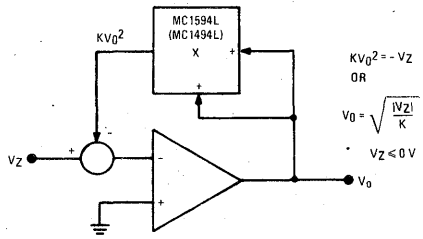


FIGURE 22 – BASIC SQUARE ROOT CIRCUIT



nator voltage. As a result, if V_X is set to 10 volts and 0.5% accuracy is available, then 5% accuracy can be expected when V_X is only 1 volt.

In accordance with an earlier statement, V_X may have only one polarity, positive, while V_Z may be either polarity.

4.3 Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together results in the square root function as indicated in Figure 22. This circuit too may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 23) protects against accidental latch-up.

This circuit too, may be adjusted in the closed-loop mode:

1. Set V_Z = -0.01 Vdc and adjust P3 (output offset) for V_O = 0.316 Vdc.
2. Set V_Z to -0.9 Vdc and adjust P2 ("X" adjust) for V_O = +3 Vdc.
3. Set V_Z to -10 Vdc and adjust P4 (gain adjust) for V_O = +10 Vdc.

Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

Note: Operation near zero volts input may prove very inaccurate, hence, it may not be possible to adjust V_O to 0 but rather only to within 100 to 400 mV of zero.

5. AC APPLICATIONS

5.1 Wideband Amplifier With Linear AGC

If one input to the MC1594 is a dc voltage and a signal voltage is applied to the other input, the amplitude of the output signal can be controlled in a linear fashion by varying the dc voltage. Hence, the multiplier can function as a dc coupled, wideband amplifier with linear AGC control.

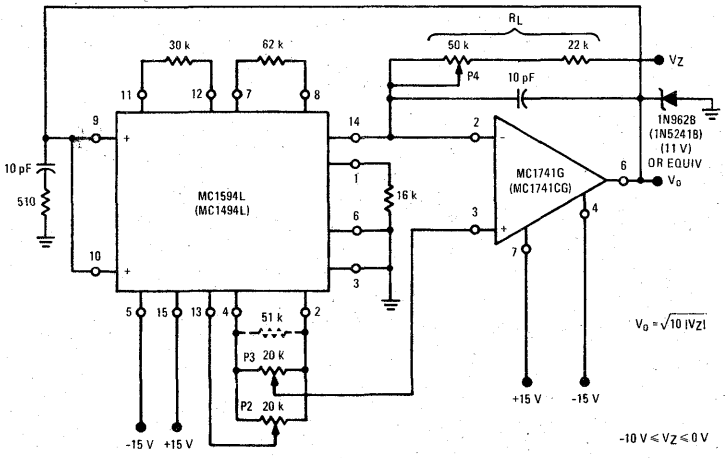
In addition to the advantage of Linear AGC control, the multiplier has three other distinct advantages over most other types of AGC systems. First, the AGC dynamic range is theoretically infinite. This stems from the basic fact that with zero volts dc applied to the AGC, the output will be zero regardless of the input. In practice, the dynamic range is limited by the ability to adjust the input offset adjust potentiometers. By using cermet multi-turn potentiometers, a dynamic range of 80 dB can be obtained. The second advantage of the multiplier is that variation of the AGC voltage has no effect on the signal handling capability of the signal port, nor does it alter the input impedance of the signal port. This feature is particularly important in AGC systems which are phase sensitive. A third advantage of the multiplier is that the output-voltage-swing capability and output impedance are unchanged with variations in AGC voltage.

The circuit of Figure 24 demonstrates the linear AGC amplifier. The amplifier can handle 1 V(rms) and exhibits a gain of approximately 20 dB. It is AGC'd through a 60 dB dynamic range with the application of an AGC voltage from 0 Vdc to 1 Vdc. The bandwidth of the amplifier is determined by the load resistor and output stray capacitance. For this reason, an emitter-follower buffer has been added to extend the bandwidth in excess of 1 MHz.

5.2 Balanced Modulator

When two-time variant signals are used as inputs, the result-

FIGURE 23 – SQUARE ROOT CIRCUIT



ing output is suppressed-carrier double-sideband modulation. In terms of sinusoidal inputs, this can be seen in the following equation:

$$V_o = K(e_1 \cos\omega_m t)(e_2 \cos\omega_c t)$$

where ω_m is the modulation frequency and ω_c is the carrier frequency. This equation can be expanded to show the suppressed carrier or balanced modulation:

$$V_o = \frac{Ke_1e_2}{2}[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

Unlike many modulation schemes, which are non-linear in nature, the modulation which takes place when using the MC1594 is linear. This means that for two sinusoidal inputs, the output will contain only two frequencies, the sum and difference, as seen in the above equation. There will be no spectrum centered about the second harmonic of the carrier, or any multiple of the carrier. For this reason, the filter requirements of a modulation system are reduced to the minimum. Figure 25 shows the MC1594 configuration to perform this function.

FIGURE 25 – BALANCED MODULATOR

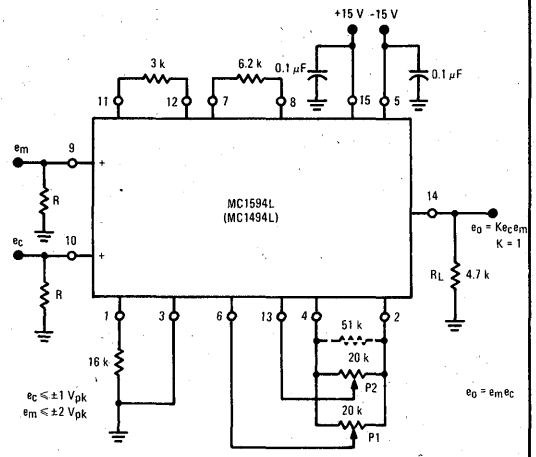
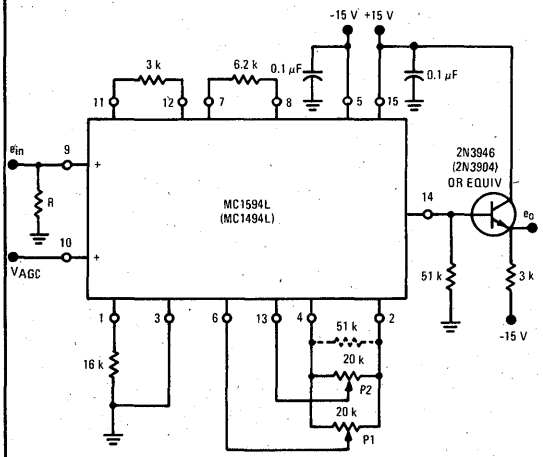


FIGURE 24 – WIDEBAND AMPLIFIER WITH LINEAR AGC



Notice that the resistor values for R_X, R_Y, and R_L have been modified. This has been done primarily to increase the bandwidth by lowering the output impedance of the MC1594 and then lowering R_X and R_Y to achieve a gain of 1. The e_c can be as large as 1 volt peak and e_m as high as 2 volts peak. No output offset adjust is employed since we are *interested only in the ac output components.*

The input R's are used to supply bias current to the multiplier inputs as well as provide matching input impedance. The output frequency range of this configuration is determined by the 4.7 k ohm output impedance and capacitive loading. Assuming a 6 pF load, the small-signal bandwidth is 5.5 MHz.

The circuit of Figure 25 will provide a typical carrier rejection of ≥70 dB from 10 kHz to 1.5 MHz.

The adjustment procedure for this circuit is quite simple.

(1) Place the carrier signal at pin 10. With no signal applied to pin 9, adjust potentiometer P1 such that an ac null is obtained at the output.

(2) Place a modulation signal at pin 9. With no signal applied to pin 10, adjust potentiometer P2 such that an ac null is obtained at the output.

Again, the ability to make careful adjustment of these offsets will be a function of the type of potentiometers used for P1 and P2. Multiple turn cermet type potentiometers are recommended.

5.3 Frequency Doubler

If for Figure 25 both inputs are identical;

$$e_m = e_c = E\cos\omega t$$

Then the output is given by

$$e_o = e_m e_c = E^2\cos^2\omega t$$

which reduces to

$$e_o = \frac{E^2}{2}(1 + \cos 2\omega t)$$

This equation states that the output will consist of a dc term equal to one half the peak voltage squared and the second harmonic of the input frequency. Thus, the circuit acts as a frequency doubler. Two facts about this circuit are worthy of note. First, the second harmonic of the input frequency is the only frequency appearing at the output. The fundamental does not appear. Second, if the input is sinusoidal, the output will be sinusoidal and requires no filtering.

The circuit of Figure 25 can be used as a frequency doubler with input frequencies in excess of 2 MHz.

5.4 Amplitude Modulator

The circuit of Figure 25 is also easily used as an amplitude modulator. This is accomplished by simply varying the input offset adjust potentiometer (P1) associated with the modu-

lation input. This procedure places a dc offset on the modulation input of the multiplier such that the carrier still passes thru the multiplier when the modulating signal is zero. The result is amplitude modulation. This is easily seen by examining the basic mathematical expression for amplitude modulation given below. For the case under discussion, with K = 1,

$$e_o = (E + E_m \cos\omega_m t)\,(E_c \cos\omega_c t)$$

where E is the dc input offset adjust voltage. This expression can be written as:

$$e_o = E_o\,[1 + M\cos\omega_c t]\,\cos\omega_c t$$

where $E_o = EE_c$

and $M = \dfrac{E_m}{E}$ = modulation index

This is the standard equation for amplitude modulation. From this, it is easy to see that 100% modulation can be achieved by adjusting the input offset adjust voltage to be exactly equal to the peak value of the modulation, E_m. This is done by observing the output waveform and adjusting the input offset potentiometer, P1, until the output exhibits the familiar amplitude modulation waveform.

5.5 Phase Detector

If the circuit of Figure 25 has as its inputs two signals of identical frequency but having a relative phase shift the output will be a dc signal which is directly proportional to the cosine of phase difference as well as the double frequency term.

$$e_c = E_c \cos\omega_c t$$

$$e_m = E_m \cos(\omega_c t + \phi)$$

$$e_o = e_c e_m = E_c E_m \cos\omega_c t \cos(\omega_c t + \phi)$$

or $$e_o = \frac{E_c E_m}{2}\,[\cos\phi + \cos(2\omega_c t + \phi)]$$

The addition of a simple low pass filter to the output (which eliminates the second cosine term) and return of R_L to an offset adjustment potentiometer will result in a dc output voltage which is proportional to the cosine of the phase difference. Hence, the circuit functions as a synchronous detector.

6. DEFINITIONS OF SPECIFICATIONS

Because of the unique nature of a multiplier, i.e., two inputs and one output, operating specifications are difficult to define and interpret. Indeed the same specification may be defined in several completely different ways depending upon which manufacturer is doing the defining. In order to clear up some of this mystery, the following definitions and examples are presented.

6.1 Multiplier Transfer Function

The output of the multiplier may be expressed by this equation:

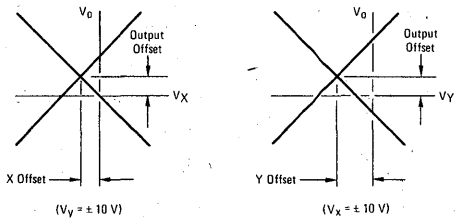
$$V_o = K\,(V_x \pm V_{iox} - V_{x\,off})\,(V_y \pm V_{ioy} - V_{y\,off}) \pm V_{oo} \quad (1)$$

where K = scale factor (see 6.5)

V_x = "x" input voltage
V_y = "y" input voltage
V_{iox} = "x" input offset voltage
V_{ioy} = "y" input offset voltage
$V_{x\,off}$ = "x" input offset adjust voltage
$V_{y\,off}$ = "y" input offset adjust voltage
V_{oo} = output offset voltage

The voltage transfer characteristic below indicates "X", "Y" and output offset voltages.

FIGURE 26



6.2 Linearity

Linearity is defined to be the maximum deviation of output voltage from a straight line transfer function. It is expressed as a percentage of full-scale output and is measured for V_x and V_y separately either using an "X-Y" plotter (and checking the deviation from a straight line) or by using the method shown in Figure 1. The latter method nulls the output signal with the input signal, resulting in distortion components proportional to the linearity.

Example: 0.35% linearity means

$$V_o = \frac{V_x V_y}{10} \pm (0.0035)\,(10\ \text{volts})$$

6.3 Input Offset Voltage

The input offset voltage is defined from Equation (1). It is measured for V_x and V_y separately and is defined to be that dc input offset adjust voltage ("x" or "y") that will result in minimum ac output when ac (5 Vpp, 1 kHz) is applied to the other input ("y" or "x" respectively). From Equation (1) we have:

$$V_{o(ac)} = K\,(0 \pm V_{iox} - V_{x\,off})\,(\sin\omega t)$$

adjust $V_{x\,off}$ so that $(\pm V_{iox} - V_{x\,off}) = 0$.

6.4 Output Offset Current and Voltage

Output offset current (I_{oo}) is the dc current flowing in the output lead when $V_x = V_y = 0$ and "X" and "Y" offset voltages are adjusted to zero.

Output offset voltage (V_{oo}) is:

$$V_{oo} = I_{oo} R_L$$

where R_L is the load resistance.

Note: Output offset voltage is defined by many manufacturers with all inputs at zero but without adjusting "X" and "Y" offset voltages to zero. Thus it includes input offset terms, an output offset term and a scale factor term.

6.5 Scale Factor

Scale factor is the K term in Equation (1). It determines the "gain" of the multiplier and is expressed approximately by the following equation.

$$K = \frac{2R_L}{R_x R_y I_1} \text{ where } R_x \text{ and } R_y \gg \frac{kT}{qI_1}$$

and I_1 is the current out of pin 1.

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6.6 Total DC Accuracy

The total dc accuracy of a multiplier is defined as error in multiplier output with dc (±10 Vdc) applied to both inputs. It is expressed as a percent of full scale. Accuracy is not specified for the MC1594 because error terms can be nulled by the user.

6.7 Temperature Stability (Drift)

Each term defined above will have a finite drift with temperature. The temperature specifications are obtained by re-adjusting the multiplier offsets and scale factor at each new temperature (see previous definitions and the adjustment procedure) and noting the change.

Assume inputs are grounded and initial offset voltages have been adjusted to zero. Then output voltage drift is given by:

$$\triangle V_O = \pm[K \pm K\ (TCK)\ (\triangle T)\ ][\ (TCV_{iox})\ (\triangle T)\ ][\ (TCV_{ioy})\ (\triangle T)\ ] \pm (TCV_{oo})\ (\triangle T)$$

6.8 Total DC Accuracy Drift

This is the temperature drift in output voltage with 10 volts applied to each input. The output is adjusted to 10 volts at $T_A = +25^oC$. Assuming initial offset voltages have been adjusted to zero at $T_A = +25^oC$, then:

$$V_O = [K \pm K\ (TCK)\ (\triangle T)\ ][10 \pm (TCV_{iox})\ (\triangle T)\ ][10 \pm (TCV_{ioy})\ (\triangle T)\ ] \pm (TCV_{oo})\ (\triangle T)$$

6.9 Power Supply Rejection

Variation in power supply voltages will cause undesired variation of the output voltage. It is measured by superimposing a 1-volt, 100-Hz signal on each supply (±15 V) with each input grounded. The resulting change in the output is expressed in mV/V.

6.10 Output Voltage Swing

Output voltage swing capability is the maximum output voltage swing (without clipping) into a resistive load (note output offset is adjusted to zero).

If an op-ampl. is used, the multiplier output becomes a virtual ground — the swing is then determined by the scale factor and the op-ampl. selected.

GENERAL INFORMATION INDEX

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ORDERING INFORMATION

Device	Temperature Range	Package
MC1495L	0°C to +70°C	Ceramic DIP
MC1595L	−55°C to +125°C	Ceramic DIP

MC1495L
MC1595L

Specifications and Applications Information

WIDEBAND MONOLITHIC FOUR-QUADRANT MULTIPLIER

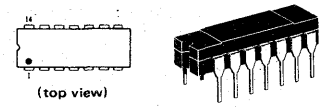
. . . designed for uses where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

*When used with an operational amplifier.

- Wide Bandwidth
- Excellent Linearity – 1% max Error on X-Input, 2% max Error on Y-Input – MC1595L
- Excellent Linearity – 2% max Error on X-Input, 4% max Error on Y-Input – MC1495L
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range – ± 10 Volts
- ± 15 Volt Operation

LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

MONOLITHIC SILICON
EPITAXIAL PASSIVATED



CERAMIC PACKAGE
CASE 632
TO-116

FIGURE 1 – FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC

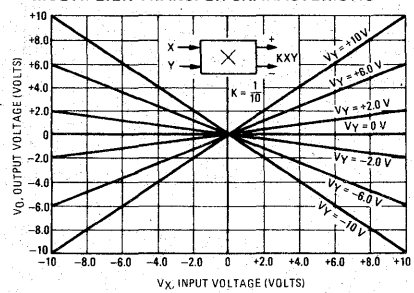


FIGURE 2 – TRANSCONDUCTANCE BANDWIDTH

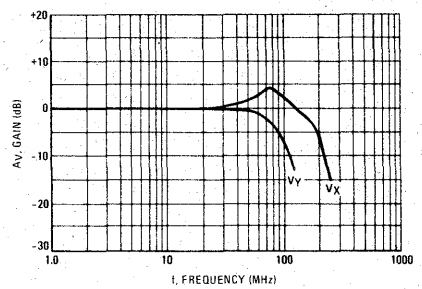
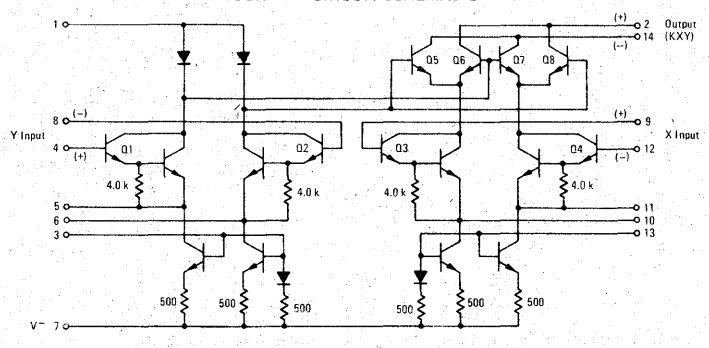


FIGURE 3 – CIRCUIT SCHEMATIC



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ELECTRICAL CHARACTERISTICS ($V^+ = +32V$, $V^- = -15$ V, $T_A = +25^oC$, $I_3 = I_{13} = 1$ mA, $R_X = R_Y = 15$ kΩ, $R_L = 11$ kΩ unless otherwise noted)

Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Linearity: Output Error in Percent of Full Scale:		5					%
$T_A = +25^oC$							
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)	MC1495		E_{RX}	–	± 1.0	± 2.0	
	MC1595			–	± 0.5	± 1.0	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)	MC1495		E_{RY}	–	± 2.0	± 4.0	
	MC1595			–	± 1.0	± 2.0	
$T_A = 0$ to $+70^oC$	MC1495						
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)			E_{RX}	–	± 1.5	–	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)			E_{RY}	–	± 3.0	–	
$T_A = -55^oC$ to $+125^oC$	MC1595						
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)			E_{RX}	–	± 0.75	–	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)			E_{RY}	–	± 1.50	–	
Squaring Mode Error: Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment		5	E_{SQ}				%
$T_A = +25^oC$	MC1495			–	± 0.75	–	
	MC1595			–	± 0.5	–	
$T_A = 0$ to $+70^oC$	MC1495			–	± 1.0	–	
$T_A = -55^oC$ to $+125^oC$	MC1595			–	± 0.75	–	
Scale Factor (Adjustable) $(K = \frac{2R_L}{I_3 R_X R_Y})$		–	K	–	0.1	–	–
Input Resistance (f = 20 Hz)	MC1495	7	R_{INX}	–	20	–	MegOhms
	MC1595			–	35	–	
	MC1495		R_{INY}	–	20	–	
	MC1595			–	35	–	
Differential Output Resistance (f = 20 Hz)		8	R_o	–	300	–	k Ohms
Input Bias Current $I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$	MC1495	6	I_{bx}	–	2.0	12	μA
	MC1595			–	2.0	8.0	
	MC1495		I_{by}	–	2.0	12	
	MC1595			–	2.0	8.0	
Input Offset Current							
$\lvert I_9 - I_{12} \rvert$	MC1495	6	$\lvert I_{iox} \rvert$	–	0.4	2.0	μA
	MC1595			–	0.2	1.0	
$\lvert I_4 - I_8 \rvert$	MC1495		$\lvert I_{iov} \rvert$	–	0.4	2.0	
	MC1595			–	0.2	1.0	
Average Temperature Coefficient of Input Offset Current		6	$\lvert TC_{Iio} \rvert$				nA/°C
($T_A = 0$ to $+70^oC$)	MC1495			–	2.0	–	
($T_A = -55^oC$ to $+125^oC$)	MC1595			–	2.0	–	
Output Offset Current $\lvert I_{14} - I_2 \rvert$		6	$\lvert I_{oo} \rvert$				μA
	MC1495			–	20	100	
	MC1595			–	10	50	
Average Temperature Coefficient of Output Offset Current		6	$\lvert TC_{Ioo} \rvert$				nA/°C
($T_A = 0$ to $+70^oC$)	MC1495			–	1.0	–	
($T_A = -55^oC$ to $+125^oC$)	MC1595			–	1.0	–	
Frequency Response							
3.0 dB Bandwidth, $R_L = 11$ kΩ		9,10	BW_{3dB}	–	3.0	–	MHz
3.0 dB Bandwidth, $R_L = 50$ Ω (Transconductance Bandwidth)			$T_{BW3\,dB}$	–	80	–	MHz
3° Relative Phase Shift Between V_X and V_Y			f_ϕ	–	750	–	kHz
1% Absolute Error Due to Input-Output Phase Shift			f_θ	–	30	–	kHz
Common Mode Input Swing (Either Input)		11	CMV				Vdc
	MC1495			±10.5	±12	–	
	MC1595			±11.5	±13	–	
Common Mode Gain (Either Input)		11	A_{CM}				dB
	MC1495			-40	-50	–	
	MC1595			-50	-60	–	
Common Mode Quiescent Output Voltage		12	V_{o1}	–	21	–	Vdc
			V_{o2}	–	21	–	
Differential Output Voltage Swing Capability		9	V_o	–	±14	–	V_{peak}
Power Supply Sensitivity		12	S^+	–	5.0	–	mV/V
			S^-	–	10	–	
Power Supply Current		12	I_7	–	6.0	7.0	mA
DC Power Dissipation		12	P_D	–	135	170	mW

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage (V_2–V_1, V_{14}–V_1, V_1–V_9, V_1–V_{12}, V_1–V_4, V_1–V_8, V_{12}–V_7, V_9–V_7, V_8–V_7, V_4–V_7)	ΔV	30	Vdc
Differential Input Signal	V_{12}–V_9 V_4–V_8	±(6+I_{13} R_X) ±(6+I_3 R_Y)	Vdc Vdc
Maximum Bias Current	I_3 I_{13}	10 10	mA
Power Dissipation (Package Limitation) Ceramic Package Derate above T_A = +25°C	P_D	 750 5.0	 mW mW/°C
Operating Temperature Range MC1495 MC1595	T_A	 0 to +70 -55 to +125	°C °C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TEST CIRCUITS

FIGURE 4 – LINEARITY (USING NULL TECHNIQUE)

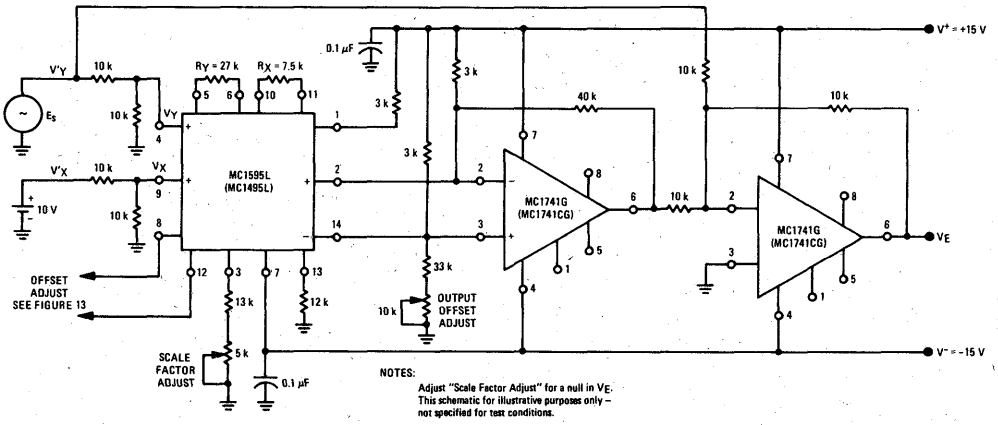
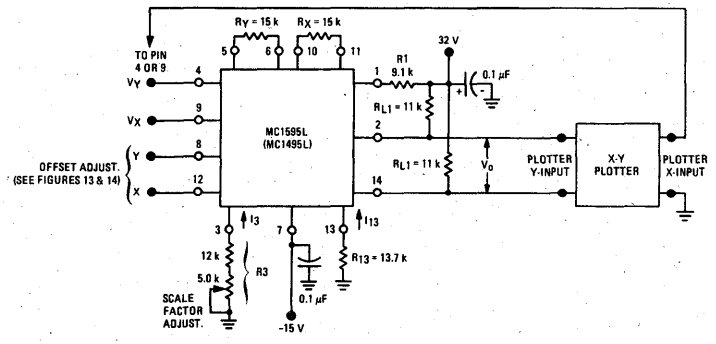


FIGURE 5 – LINEARITY (USING X-Y PLOTTER TECHNIQUE)



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TEST CIRCUITS (continued)

FIGURE 6 – INPUT AND OUTPUT CURRENT

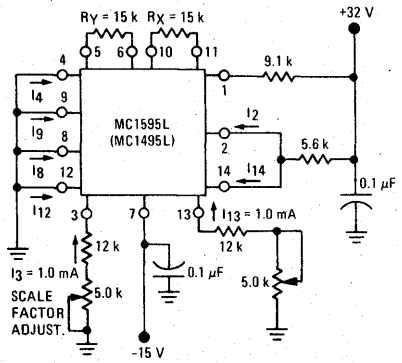


FIGURE 7 – INPUT RESISTANCE

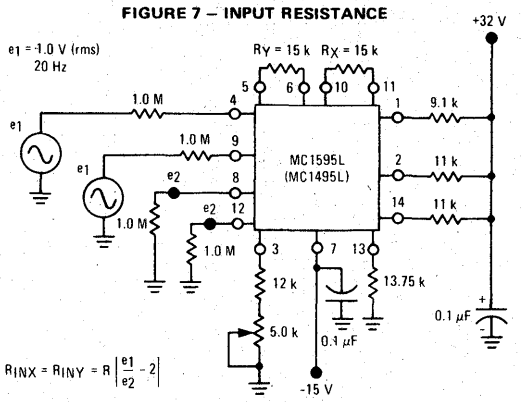


FIGURE 8 – OUTPUT RESISTANCE

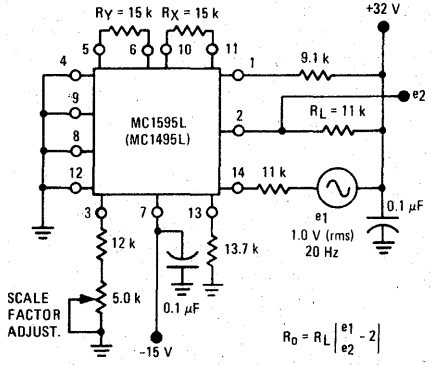


FIGURE 9 – BANDWIDTH (R_L = 11 kΩ)

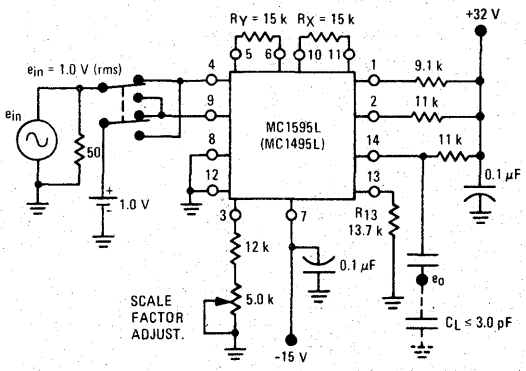


FIGURE 10 – BANDWIDTH (R_L = 50 Ω)

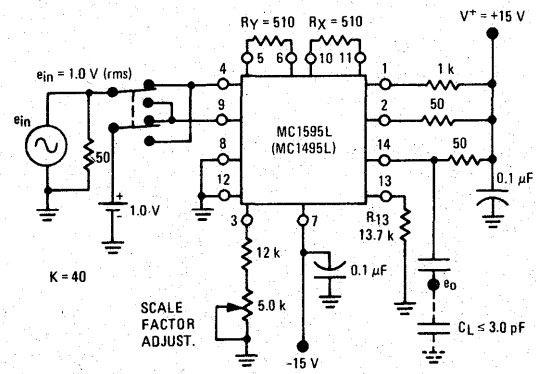
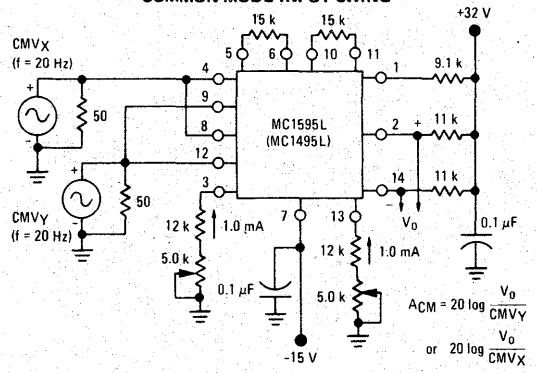


FIGURE 11 – COMMON-MODE GAIN and COMMON-MODE INPUT SWING



TEST CIRCUITS (continued)

FIGURE 12 – POWER SUPPLY SENSITIVITY

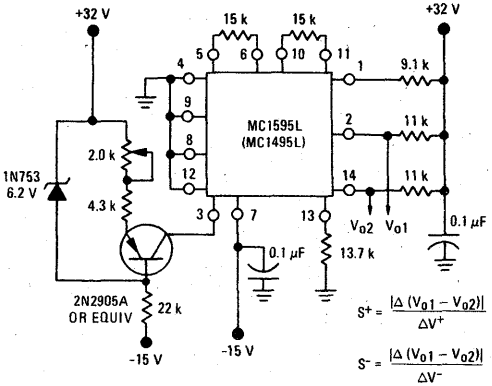
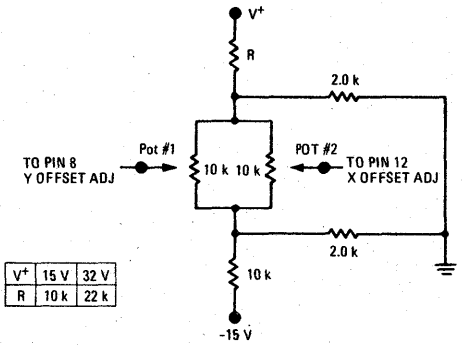
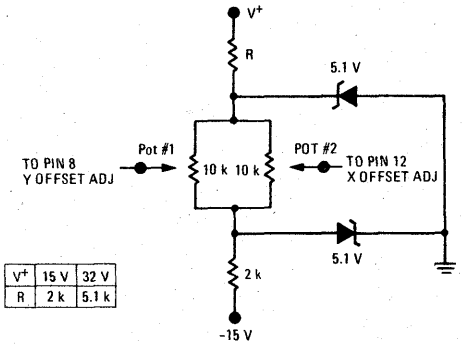


FIGURE 13 – OFFSET ADJUST CIRCUIT



V^+	15 V	32 V
R	10 k	22 k

FIGURE 14 – OFFSET ADJUST CIRCUIT (ALTERNATE)



V^+	15 V	32 V
R	2 k	5.1 k

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TYPICAL CHARACTERISTICS

FIGURE 15 – LINEARITY versus TEMPERATURE

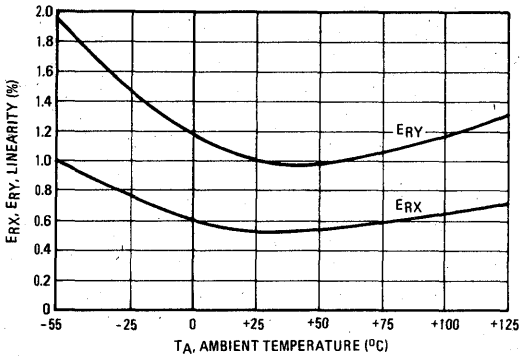

FIGURE 16 – SCALE FACTOR versus TEMPERATURE

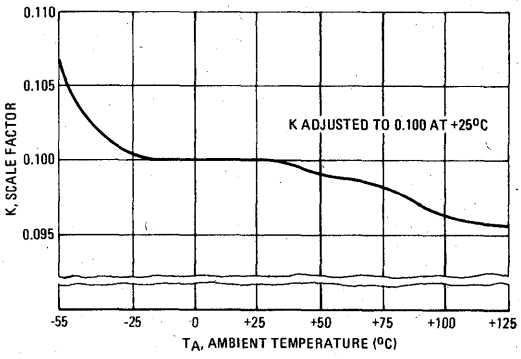

FIGURE 17 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

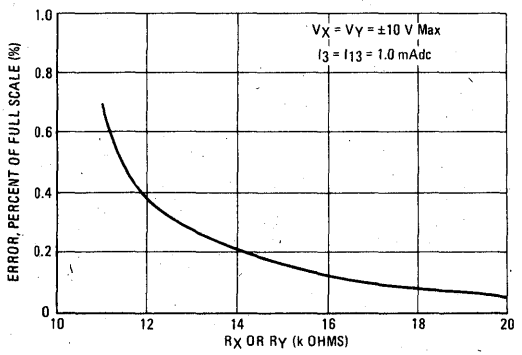

FIGURE 18 – ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER

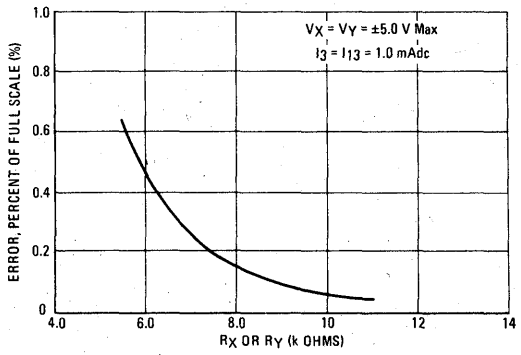

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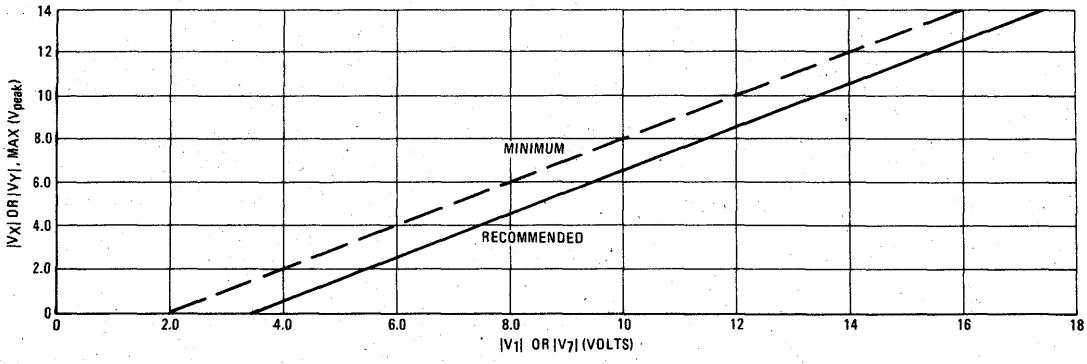
FIGURE 19 – MAXIMUM ALLOWABLE INPUT VOLTAGE versus VOLTAGE AT PIN 1 OR PIN 7



OPERATION AND APPLICATIONS INFORMATION

1. Theory of Operation

The MC1595 (MC1495) is a monolithic, four-quadrant multiplier which operates on the principle of variable transconductance. The detailed theory of operation is covered in Application Note AN-489, Analysis and Basic Operation of the MC1595. The result of this analysis is that the differential output current of the multiplier is given by

$$I_A - I_B = \Delta I = \frac{2V_XV_Y}{R_XR_YI_3}$$

where I_A and I_B are the currents into pins 14 and 2, respectively, and V_X and V_Y are the X and Y input voltages at the multiplier input terminals.

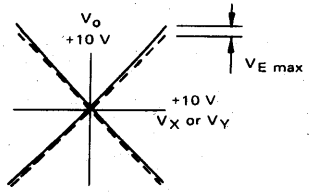
2. Design Considerations

2.1 General

The MC1595 (MC1495) permits the designer to tailor the multiplier to a specific application by proper selection of external components. External components may be selected to optimize a given parameter (e.g. bandwidth) which may in turn restrict another parameter (e.g. maximum output voltage swing). Each important parameter is discussed in detail in the following paragraphs.

2.1.1 Linearity, Output Error, E_{RX} or E_{RY}

Linearity error is defined as the maximum deviation of output voltage from a straight line transfer function. It is expressed as error in percent of full scale (see figure below).



For example, if the maximum deviation, $V_{E(max)}$, is ±100 mV and the full scale output is 10 volts, then the percentage error is

$$E_R = \frac{V_{E(max)}}{V_{o(max)}} \times 100 = \frac{100 \times 10^{-3}}{10} \times 100 = \pm 1.0\%.$$

Linearity error may be measured by either of the following methods:

1. Using an X – Y plotter with the circuit shown in Figure 5, obtain plots for X and Y similar to the one shown above.
2. Use the circuit of Figure 4. This method nulls the level shifted output of the multiplier with the original input. The peak output of the null operational amplifier will be equal to the error voltage, $V_{E(max)}$.

One source of linearity error can arise from large signal nonlinearity in the X and Y-input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough so that nonlinear base-emitter voltage variation can be ignored. Figures 17 and 18 show the error expected from this source as a function of the values of R_X and R_Y with an operating current of 1.0 mA in each side of the differential amplifiers (i.e., $I_3 = I_{13} = 1.0$ mA).

2.1.2 3 dB-Bandwidth and Phase Shift

Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, low value load resistors and/or a wideband operational amplifier should be used. Stray output capacitance will depend to a large extent on circuit layout.

Phase shift in the multiplier circuit results from two sources: phase shift common to both X and Y channels (due to the load resistor-output capacitance pole mentioned above) and relative phase shift between X and Y channels (due to differences in transadmittance in the X and Y channels). If the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between V_X and V_Y results in a vector error of 5%.

2.1.3 Maximum Input Voltage

$V_{X(max)}$, $V_{Y(max)}$ maximum input voltages must be such that:

$$V_{X(max)} < I_{13} R_Y$$

$$V_{Y(max)} < I_3 R_Y.$$

Exceeding this value will drive one side of the input amplifier to "cutoff" and cause non-linear operation.

Currents I_3 and I_{13} are chosen at a convenient value (observing power dissipation limitation) between 0.5 mA and 2.0 mA, approximately 1.0 mA. Then R_X and R_Y can be determined by considering the input signal handling requirements.

For $V_{X(max)} = V_{Y(max)} = 10$ volts;

$$R_X = R_Y > \frac{10\ V}{1.0\ mA} = 10\ k\Omega.$$

The equation $I_A - I_B = \dfrac{2V_XV_Y}{R_XR_YI_3}$

is derived from $I_A - I_B = \dfrac{2V_XV_Y}{(R_X + \frac{2kT}{qI_{13}})(R_Y + \frac{2kT}{qI_3})I_3}$

with the assumption $R_X \gg \frac{2kT}{qI_{13}}$ and $R_Y \gg \frac{2kT}{qI_3}$.

At $T_A = +25°C$ and $I_{13} = I_3 = 1$ mA,

$$\frac{2kT}{qI_{13}} = \frac{2kT}{qI_3} = 52\ \Omega.$$

Therefore, with $R_X = R_Y = 10\ k\Omega$ the above assumption is valid. Reference to Figure 19 will indicate limitations of $V_{X(max)}$ or $V_{Y(max)}$ due to V_1 and V_7. Exceeding these limits will cause saturation or "cutoff" of the input transistors. See Step 4 of Section 3 (General Design Procedure) for further details.

2.1.4 Maximum Output Voltage Swing

The maximum output voltage swing is dependent upon the factors mentioned below and upon the particular circuit being considered.

For Figure 20 the maximum output swing is dependent upon V^+ for positive swing and upon the voltage at pin 1 for negative swing. The potential at pin 1 determines the quiescent level for transistors Q_5, Q_6, Q_7, and Q_8. This potential

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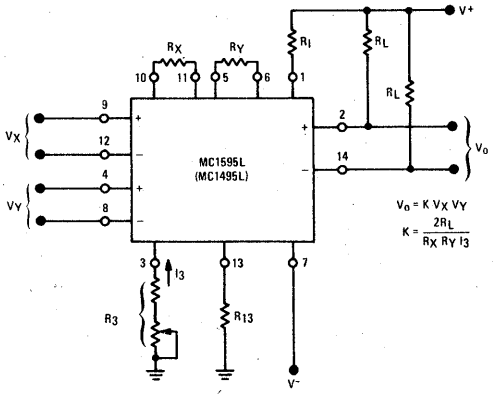
OPERATION AND APPLICATIONS INFORMATION (continued)

should be related so that negative swing at pins 2 or 14 does not saturate those transistors. See Section 3 for further information regarding selection of these potentials.

FIGURE 20 – BASIC MULTIPLIER



If an operational amplifier is used for level shift, as shown in Figure 21, the output swing (of the multiplier) is greatly reduced. See Section 3 for further details.

3. General Design Procedure

Selection of component values is best demonstrated by the following example: assume resistive dividers are used at the X and Y inputs to limit the maximum multiplier input to ±5.0 volts ($V_X = V_{Y\,[max]}$) for a ±10-volt input ($V_X' = V_Y'_{[max]}$). (See Figure 21). If an overall scale factor of 1/10 is desired, then

$$V_o = \frac{V_X' V_Y'}{10} = \frac{(2V_X)(2V_Y)}{10} = 4/10\ V_X V_Y .$$

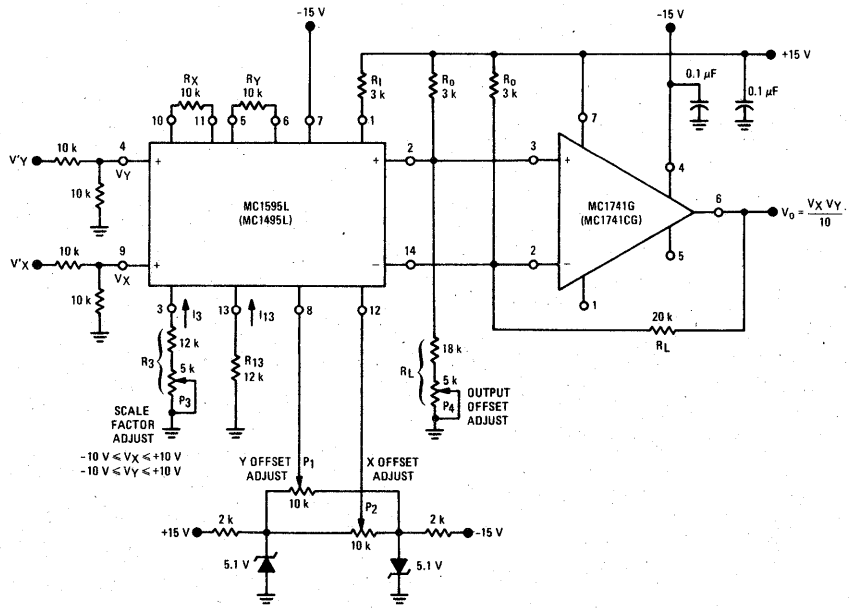
Therefore, K = 4/10 for the multiplier (excluding the divider network).

Step 1. The first step is to select current I_3 and current I_{13}. There are no restrictions on the selection of either of these currents except the power dissipation of the device. I_3 and I_{13} will normally be one or two milliamperes. Further, I_3 does not have to be equal to I_{13}, and there is normally no need to make them different. For this example, let

$$I_3 = I_{13} = 1\ mA.$$

To set currents I_3 and I_{13} to the desired value, it is only necessary to connect a resistor between pin 13 and ground, and between pin 3 and ground. From the schematic shown in Figure 3,

FIGURE 21 – MULTIPLIER WITH OP-AMP. LEVEL SHIFT



OPERATION AND APPLICATIONS INFORMATION (continued)

it can be seen that the resistor values necessary are given by:

$$R_{13} + 500\ \Omega = \frac{|V^-| - 0.7\ V}{I_{13}}$$

$$R_3 + 500\ \Omega = \frac{|V^-| - 0.7\ V}{I_3}$$

Let $V^- = -15$ V

Then $R_{13} + 500 = \frac{14.3\ V}{1\ mA}$ or $R_{13} = 13.8\ k\Omega$

Let $R_{13} = 12\ k\Omega$

Similarly, $R_3 = 13.8\ k\Omega$

Let $R_3 = 15\ k\Omega$

However, for applications which require an accurate scale factor, the adjustment of R_3 and consequently, I_3, offers a convenient method of making a final trim of the scale factor. For this reason, as shown in Figure 21, resistor R_3 is shown as a fixed resistor in series with a potentiometer.

For applications not requiring an exact scale factor (balanced modulator, frequency doubler, AGC amplifier, etc.), pins 3 and 13 can be connected together and a single resistor from pin 3 to ground can be used. In this case, the single resistor would have a value of one-half the above calculated value for R_{13}.

Step 2. The next step is to select R_X and R_Y. To insure that the input transistors will always be active, the following conditions should be met:

$$\frac{V_X}{R_X} < I_{13} \qquad \frac{V_Y}{R_Y} < I_3.$$

A good rule of thumb is to make $I_3 R_Y \geq 1.5\ V_{Y(max)}$ and $I_{13} R_X \geq 1.5\ V_{X(max)}$.

The larger the $I_3 R_Y$ and $I_{13} R_X$ product in relation to V_Y and V_X respectively, the more accurate the multiplier will be (see Figures 17 and 18).

Let $R_X = R_Y = 10\ k\Omega$

Then $I_3 R_Y = 10$ V

$I_{13} R_X = 10$ V

since $V_{X(max)} = V_{Y(max)} = 5.0$ volts the value of $R_X = R_Y = 10\ k\Omega$ is sufficient.

Step 3. Now that R_X, R_Y and I_3 have been chosen, R_L can be determined:

$$K = \frac{2R_L}{R_X R_Y I_3} = \frac{4}{10}$$

$$\text{or} \quad \frac{(2)\ (R_L)}{(10\ k)\ (10\ k)\ (1\ mA)} = \frac{4}{10}$$

Thus $R_L = 20\ k\Omega$.

Step 4. To determine what power-supply voltage is necessary for this application, attention must be given to the circuit schematic shown in Figure 3. From the circuit schematic it can be seen that in order to maintain transistors Q_1, Q_2, Q_3 and Q_4 in an active region when the maximum input voltages are applied ($V_X' = V_Y' = 10$ V or $V_X = 5.0$ V, $V_Y = 5.0$ V), their respective collector voltage should be at least a few tenths of a volt higher than the maximum input voltage. It should also be noticed that the collector voltage of transistors Q_3 and Q_4 are at a potential which is two diode-drops below the voltage at pin 1. Thus, the voltage at pin 1 should be about two volts higher than the maximum input voltage. Therefore, to handle +5.0 volts at the inputs, the voltage at pin 1 must be at least +7.0 volts. Let $V_1 = 9.0$ Vdc.

Since the current following into pin 1 is always equal to $2I_3$, the voltage at pin 1 can be set by placing a resistor, R_1 from pin 1 to the positive supply:

$$R_1 = \frac{V^+ - V_1}{2I_3}$$

Let $V^+ = +15$ V

Then $R_1 = \frac{15\ V - 9\ V}{(2)\ (1\ mA)}$

$R_1 = 3\ k\Omega$.

Note that the voltage at the base of transistors Q_5, Q_6, Q_7 and Q_8 is one diode-drop below the voltage at pin 1. Thus, in order that these transistors stay active, the voltage at pins 2 and 14 should be approximately halfway between the voltage at pin 1 and the positive-supply voltage. For this example, the voltage at pins 2 and 14 should be approximately 11 volts.

Step 5. Level Shifting

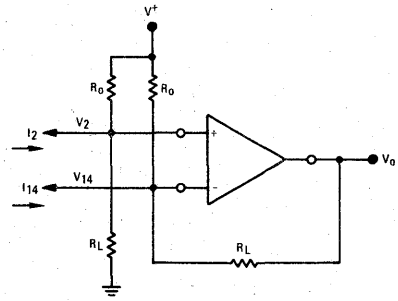
For dc applications, such as the multiply, divide and square-root functions, it is usually desirable to convert the differential output to a single-ended output voltage referenced to ground. The circuit shown in Figure 22 performs this function. It can be shown that the output voltage of this circuit is given by:

$$V_o = (I_2 - I_{14})\ R_L$$

And since $I_A - I_B = I_2 - I_{14} = \frac{2I_X I_Y}{I_3} = \frac{2\ V_X V_Y}{I_3 R_X R_Y}$

Then $V_o = \frac{2R_L V_X' V_Y'}{4R_X R_Y I_3}$ where $V_X' V_Y'$ is the voltage at the input to the voltage dividers.

FIGURE 22 – LEVEL SHIFT CIRCUIT



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OPERATION AND APPLICATIONS INFORMATION (continued)

The choice of an operational amplifier for this application should have low bias currents, low offset current, and a high common-mode input voltage range as well as a high common-mode rejection ratio. The MC1556, and MC1741 operational amplifiers meet these requirements.

Referring to Figure 21, the level shift components will be determined. When $V_X = V_Y = 0$, the currents I_2 and I_{14} will be equal to I_{13}. In Step 3, R_L was found to be 20 kΩ and in Step 4, V_2 and V_{14} were found to be approximately 11 volts. From this information, R_o can be found easily from the following equation (neglecting the operational amplifiers bias current):

$$\frac{V_2}{R_L} + I_{13} = \frac{V^+ - V_2}{R_o}$$

And for this example, $\frac{11\ V}{20\ k\Omega} + 1\ mA = \frac{15\ V - 11\ V}{R_o}$

Solving for R_o, $R_o = 2.6\ k\Omega$

Thus, select $R_o = 3.0\ k\Omega$

For $R_o = 3.0\ k\Omega$, the voltage at pins 2 and 14 is calculated to be

$$V_2 = V_{14} = 10.4\ volts.$$

The linearity of this circuit (Figure 21) is likely to be as good or better than the circuit of Figure 5. Further improvements are possible as shown in Figure 23 where R_Y has been increased substantially to improve the Y linearity, and R_X decreased somewhat so as not to materially affect the X linearity, this avoids increasing R_L significantly in order to maintain a K of 0.1.

The versatility of the MC1595 (MC1495) allows the user to to optimize its performance for various input and output signal levels.

4. Offset and Scale Factor Adjustment

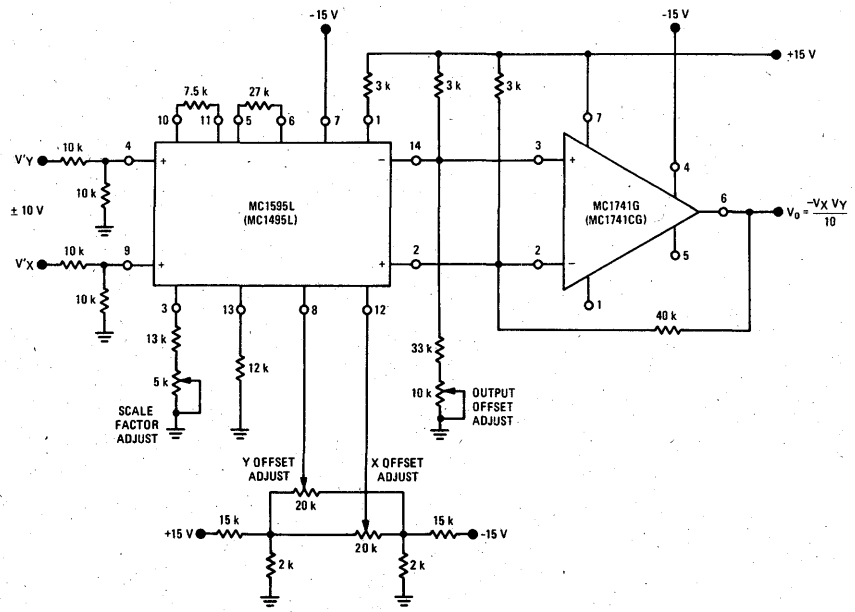
4.1 Offset Voltages

Within the monolithic multiplier (Figure 3) transistor base-emitter junctions are typically matched within 1 mV and resistors are typically matched within 2%. Even with this careful matching, an output error can occur. This output error is comprised of X-input offset voltage, Y-input offset voltage, and output-offset voltage. These errors can be adjusted to zero with the techniques shown in Figure 21. Offset terms can be shown analytically by the transfer function:

$$V_o = K(V_X \pm V_{IOX} \pm V_{X\,off})(V_Y \pm V_{IOY} \pm V_{Y\,off}) \pm V_{oo} \quad (1)$$

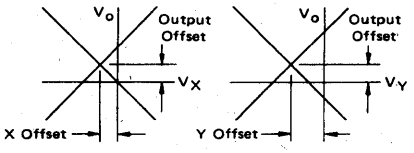
Where K = scale factor
V_X = X input voltage
V_Y = Y input voltage
V_{IOX} = X input offset voltage
V_{IOY} = Y input offset voltage
$V_{X\,off}$ = X input offset adjust voltage
$V_{Y\,off}$ = Y input offset adjust voltage
V_{oo} = output offset voltage.

FIGURE 23 – MULTIPLIER WITH IMPROVED LINEARITY



OPERATION AND APPLICATIONS INFORMATION (continued)

X, Y and Output Offset Voltages



For most dc applications, all three offset adjust potentiometers (P_1, P_2, P_4) will be necessary. One or more offset adjust potentiometers can be eliminated for ac applications (See Figures 28, 29, 30, 31).

If well regulated supply voltages are available, the offset adjust circuit of Figure 13 is recommended. Otherwise, the circuit of Figure 14 will greatly reduce the sensitivity to power supply changes.

4.2 Scale Factor

The scale factor, K, is set by P_3(Figure 21). P_3 varies I_3 which inversely controls the scale factor K. It should be noted that current I_3 is one-half the current through R_1. R_1 sets the bias level for Q_5, Q_6, Q_7, and Q_8 (See Figure 3). Therefore, to be sure that these devices remain active under all conditions of input and output swing, care should be exercised in adjusting P_3 over wide voltage ranges (see Section 3, General Design Procedure).

4.3 Adjustment Procedures

The following adjustment procedure should be used to null the offsets and set the scale factor for the multiply mode of operation. (See Figure 21)

1. X Input Offset
   (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "Y" input (pin 4)
   (b) Connect "X" input (pin 9) to ground
   (c) Adjust X offset potentiometer, P_2, for an ac null at the output
2. Y Input Offset
   (a) Connect oscillator (1 kHz, 5 Vpp sinewave) to the "X" input (pin 9).
   (b) Connect "Y" input (pin 4) to ground
   (c) Adjust "Y" offset potentiometer, P_1, for an ac null at the output
3. Output Offset
   (a) Connect both "X" and "Y" inputs to ground
   (b) Adjust output offset potentiometer, P_4, until the output voltage V_o is zero volts dc
4. Scale Factor
   (a) Apply +10 Vdc to both the "X" and "Y" inputs
   (b) Adjust P_3 to achieve + 10.00 V at the output.
5. Repeat steps 1 through 4 as necessary.

The ability to accurately adjust the MC1595 (MC1495) depends upon the characteristics of potentiometers P_1 through P_4. Multi-turn, infinite resolution potentiometers with low-temperature coefficients are recommended.

5. DC Applications

5.1 Multiply

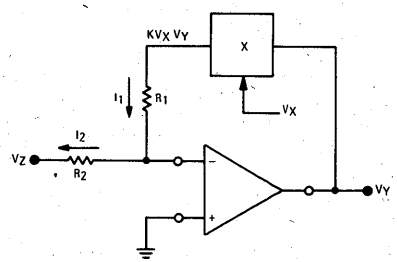
The circuit shown in Figure 21 may be used to multiply signals from dc to 100 kHz. Input levels to the actual multiplier are 5.0 V (max). With resistive voltage dividers the maximum could be very large — however, for this application two-to-one dividers have been used so that the maximum input level is 10 V. The maximum output level has also been designed for 10 V (max).

5.2 Squaring Circuit

If the two inputs are tied together, the resultant function is squaring; that is $V_o = KV^2$ where K is the scale factor. Note that all error terms can be eliminated with only three adjustment potentiometers, thus eliminating one of the input offset adjustments. Procedures for nulling with adjustments are given as follows:

1. AC Procedure:
   (a) Connect oscillator (1 kHz, 15 Vpp) to input
   (b) Monitor output at 2 kHz with tuned voltmeter and adjust P_3 for desired gain (be sure to peak response of the voltmeter)
   (c) Tune voltmeter to 1 kHz and adjust P_1 for a minimum output voltage
   (d) Ground input and adjust P_4 (output offset) for zero volts dc output
   (e) Repeat steps a through d as necessary.
2. DC Procedure:
   (a) Set $V_X = V_Y = 0$ V and adjust P_4 (output offset potentiometer) such that $V_o = 0.0$ Vdc
   (b) Set $V_X = V_Y = 1.0$ V and adjust P_1 (Y input offset potentiometer) such that the output voltage is +0.100 volts
   (c) Set $V_X = V_Y = 10$ Vdc and adjust P_3 such that the output voltage is +10.00 volts
   (d) Set $V_X = V_Y = -10$ Vdc. Repeat steps a through d as necessary.

FIGURE 24 – BASIC DIVIDE CIRCUIT



5.3 Divide Circuit

Consider the circuit shown in Figure 24 in which the multiplier is placed in the feedback path of an operational amplifier. For this configuration, the operational amplifier will maintain a "virtual ground" at the inverting (–) input. Assuming that the bias current of the operational amplifier is negligible, then $I_1 = I_2$ and

$$\frac{KV_XV_Y}{R1} = \frac{-V_Z}{R2} \quad (1)$$

Solving for V_Y,

$$V_Y = \frac{-R1}{R2}\frac{1}{K}\frac{V_Z}{V_X}. \quad (2)$$

If R1 = R2

$$V_Y = \frac{-V_Z}{KV_X} \quad (3)$$

If R1 = KR2

$$V_Y = \frac{-V_Z}{V_X}. \quad (4)$$

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OPERATION AND APPLICATIONS INFORMATION (continued)

Hence, the output voltage is the ratio of V_Z to V_X and provides a divide function. This analysis is, of course, the ideal condition. If the multiplier error is taken into account, the output voltage is found to be

$$V_Y = -\left[\frac{R1}{R2\,K}\right]\frac{V_Z}{V_X} + \frac{\Delta E}{K V_X}, \quad (5)$$

where ΔE is the error voltage at the output of the multiplier. From this equation, it is seen that divide accuracy is strongly dependent upon the accuracy at which the multiplier can be set, particularly at small values of V_Y. For example, assume that R1 = R2, and K = 1/10. For these conditions the output of the divide circuit is given by:

$$V_Y = \frac{-10\,V_Z}{V_X} + \frac{10\,\Delta E}{V_X}. \quad (6)$$

From equation 6, it is seen that only when V_X = 10 V is the error voltage of the divide circuit as low as the error of the multiply circuit. For example, when V_X is small, (0.1 volt) the error voltage of the divide circuit can be expected to be a hundred times the error of the basic multiplier circuit.

In terms of percentage error,

$$\text{percentage error} = \frac{\text{error}}{\text{actual}} \times 100\%$$

or from equation (5),

$$P.E._D = \frac{\frac{\Delta E}{K V_X}}{\left[\frac{R1}{R2\,K}\right]\frac{V_Z}{V_X}} = \left[\frac{R2}{R1}\right]\frac{\Delta E}{V_Z}. \quad (7)$$

From equation 7, the percentage error is inversely related to voltage V_Z (i.e., for increasing values of V_Z, the percentage error decreases).

A circuit that performs the divide function is shown in Figure 25.

Two things should be emphasized concerning Figure 25.

1. The input voltage (V'_X) must be greater than zero and must be positive. This insures that the current out of pin 2 of the multiplier will always be in a direction compatible with the polarity of V_Z.
2. Pins 2 and 14 of the multiplier have been interchanged in respect to the operational amplifiers input terminals. In this instance, Figure 25 differs from the circuit connection shown in Figure 21; necessitated to insure negative feedback around the loop.

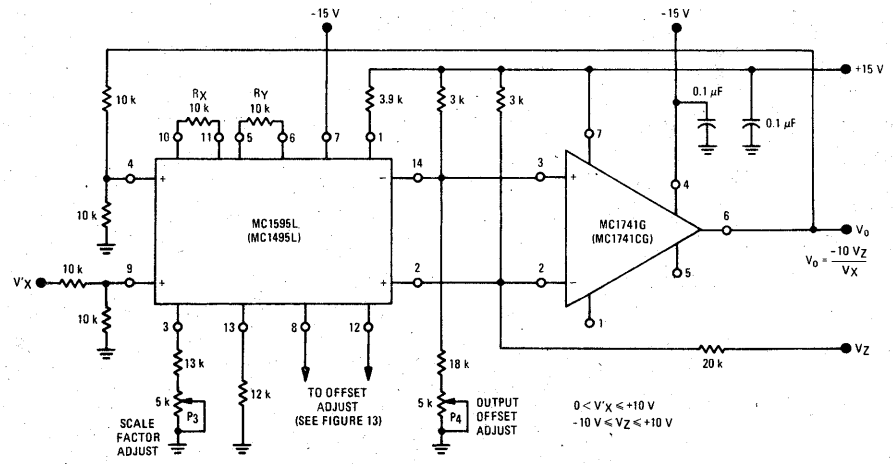
A Suggested Adjustment Procedure for the Divide Circuit

1. Set V_Z = 0 volts and adjust the output offset potentiometer (P_4) until the output voltage (V_o) remains at some (not necessarily zero) constant value as V_X' is varied between +1.0 volt and +10 volts.
2. Keep V_Z at 0 volts, set V_X' at +10 volts and adjust the Y input offset potentiometer (P_1) until V_o = 0 volts.
3. Let $V_X' = V_Z$ and adjust the X input offset potentiometer (P_2) until the output voltage remains at some (not necessarily - 10 volts) constant value as $V_Z = V_X'$ is varied between +1.0 and +10 volts.
4. Keep $V_X' = V_Z$ and adjust the scale factor potentiometer (P_3) until the average value of V_o is - 10 volts as $V_Z = V_X'$ is varied between +1.0 volt and +10 volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

5.4 Square Root

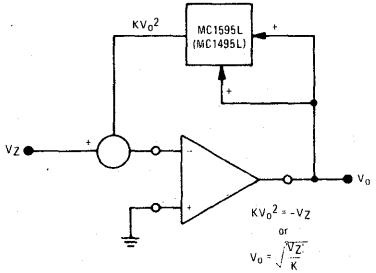
A special case of the divide circuit in which the two inputs to the multiplier are connected together is the square root function

FIGURE 25 – DIVIDE CIRCUIT



OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 26 – BASIC SQUARE ROOT CIRCUIT



as indicated in Figure 26. This circuit may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 27) protects against accidental latch-up.

This circuit also may be adjusted in the closed-loop mode as follows:

1. Set V_Z to -0.01 volts and adjust P_4 (output offset) for V_o = +0.316 volts, being careful to approach the output from the positive side to preclude the effect of the output diode clamping.
2. Set V_Z to -0.9 volts and adjust P_2 (X adjust) for V_o = +3.0 volts.
3. Set V_Z to -10 volts and adjust P_3 (scale factor adjust) for V_o = +10 volts.
4. Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

6. AC Applications

The applications that follow demonstrate the versatility of the monolithic multiplier. If a potted multiplier is used for these cases, the results generally would not be as good because the potted units have circuits that, although they optimize dc multiplication operation, can hinder ac applications.

6.1 Frequency doubling often is done with a diode where the fundamental plus a series of harmonics are generated. However, extensive filtering is required to obtain the desired harmonic, and the second harmonic obtained under this technique usually is small in magnitude and requires amplification.

When a multiplier is used to double frequency the second harmonic is obtained directly, except for a dc term, which can be removed with ac coupling.

$$e_o = KE^2 \cos^2 \omega t$$

$$e_o = \frac{KE^2}{2}(1 + \cos 2\omega t).$$

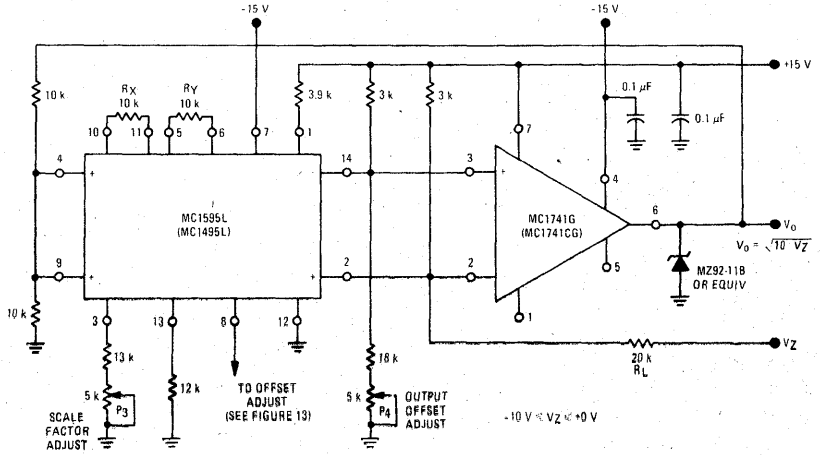
A potted multiplier can be used to obtain the double frequency component, but frequency would be limited by its internal level-shift amplifier. In the monolithic units, the amplifier is omitted.

In a typical doubler circuit, conventional ± 15-volt supplies are used. An input dynamic range of 5.0 volts peak-to-peak is allowed. The circuit generates wave-forms that are double frequency; less than 1% distortion is encountered without filtering. The configuration has been successfully used in excess of 200 kHz; reducing the scale factor by decreasing the load resistors can further expand the bandwidth.

A slightly modified version of the MC1595 (MC1495) – the MC1596 (MC1496) – has been successfully used as a doubler to obtain 400 MHz. (See Figure 28.)

6.2 Figure 29 represents an application for the monolithic multiplier as a balanced modulator. Here, the audio input signal is 1.6 kHz and the carrier is 40 kHz.

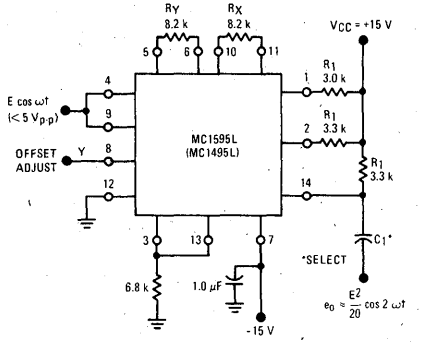
FIGURE 27 – SQUARE ROOT CIRCUIT



8

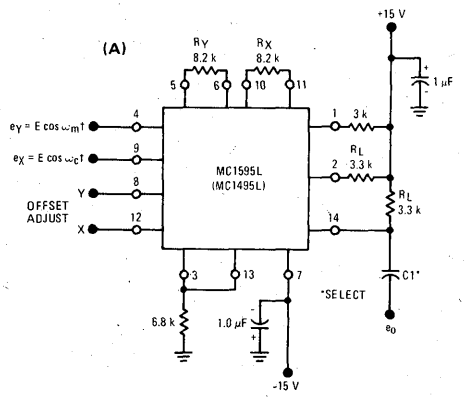
OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 28 – FREQUENCY DOUBLER

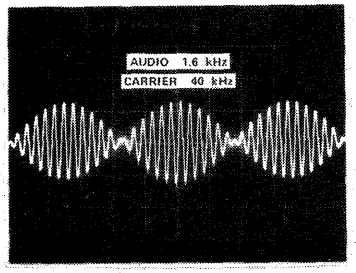


When two equal cosine waves are applied to X and Y, the result is a wave shape of twice the input frequency. For this example the input was a 10 kHz signal, output was 20 kHz.

FIGURE 29 – BALANCED MODULATOR



(B)



The defining equation for balanced modulation is

$$K(E_m \cos \omega_m t)(E_c \cos \omega_c t) =$$

$$\frac{KE_cE_m}{2}[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

where ω_c is the carrier frequency, ω_m is the modulator frequency and K is the multiplier gain constant.

AC coupling at the output eliminates the need for level translation or an operational amplifier; a higher operating frequency results.

A problem common to communications is to extract the intelligence from single-sideband received signal. The ssb signal is of the form

$$e_{ssb} = A \cos(\omega_c + \omega_m)t$$

and if multiplied by the appropriate carrier waveform, cos $\omega_c t$,

$$e_{ssb}e_{carrier} = \frac{AK}{2}[\cos(2\omega_c + \omega_m)t + \cos(\omega_c)t].$$

If the frequency of the band-limited carrier signal, ω_c, is ascertained in advance the designer can insert a low-pass filter and obtain the (AK/2) (cos $\omega_c t$) term with ease. He also can use an operational amplifier for a combination level shift-active filter, as an external component. But in potted multipliers, even if the frequency range can be covered, the operational amplifier is inside and not accessible, so the user must accept the level shifting provided, and still add a low-pass filter.

6.3 Amplitude Modulation

The multiplier performs amplitude modulation, similar to balanced modulation, when a dc term is added to the modulating signal with the Y offset adjust potentiometer. (See Figure 30.)

Here, the identity is

$$E_m(1 + m \cos \omega_m t)E_c \cos \omega_c t = KE_mE_c \cos \omega_c t +$$

$$\frac{KE_mE_cm}{2}[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

where m indicates the degree of modulation. Since m is adjustable, via potentiometer P_1, 100% modulation is possible. Without extensive tweaking, 96% modulation may be obtained where ω_c and ω_m are the same as in the balanced-modulator example.

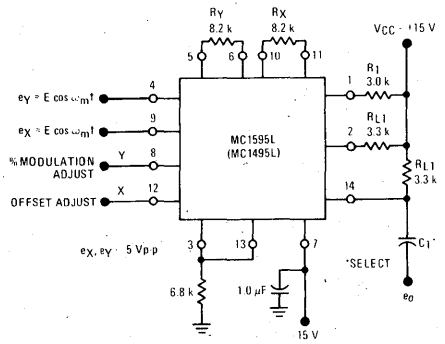
6.4 Linear Gain Control

To obtain linear gain control, the designer can feed to one of the two MC1595 (MC1495) inputs a signal that will vary the unit's gain. The following example demonstrates the feasibility of this application. Suppose a 200 kHz sine wave, 1.0 volt peak-to-peak, is the signal to which a gain control will be added. The dynamic range of the control voltage V_C is 0 to +1.0 volt. These must be ascertained and the proper values of R_X and R_Y can be selected for optimum performance. For the 200-kHz operating frequency, load resistors of 100 ohms were chosen to broaden the operating bandwidth of the multiplier, but gain was sacrificed. It may be made up with an amplifier operating at the appropriate frequency. (See Figure 31.)

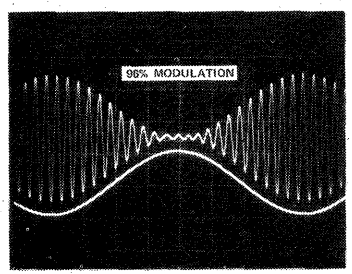
8

OPERATION AND APPLICATIONS INFORMATION (continued)

FIGURE 30 – AMPLITUDE MODULATION



(B)



The signal is applied to the unit's Y input. Since the total input range is limited to 1.0 volt p-p, a 2.0-volt swing, a current source of 2.0 mA and an R_Y value of 1.0 kilohm is chosen. This takes best advantage of the dynamic range and insures *linear operation in the Y-channel.*

Since the X input varies between 0 and +1.0 volt, the current source selected was 1.0 mA and the R_X value chosen was 2.0 kilohms. This also insures linear operation over the X input dynamic range.

Choosing $R_L = 100$ assures wide-bandwidth operation. Hence, the scale factor for this configuration is

$$K = \frac{R_L}{R_X R_Y I_3}$$

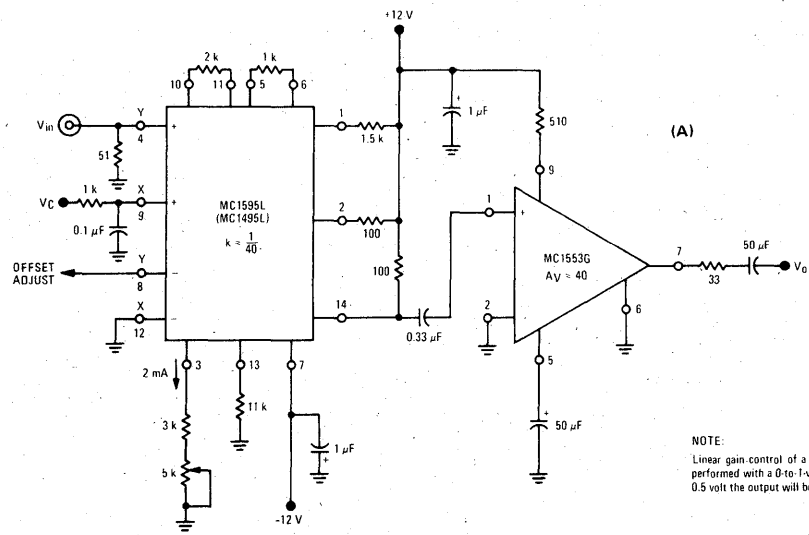
$$= \frac{100}{(2\text{ k})(1\text{ k})(2 \times 10^{+3})}\ V^{-1}$$

$$= \frac{1}{40}\ V^{-1}.$$

The 2 in the numerator of the equation is missing in this scale-factor expression because the output is single-ended and ac coupled.

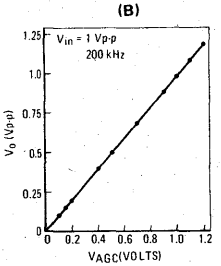
To recover the gain, an MC1552 video amplifier with a gain of 40 is used. An operational amplifier also could have been used with frequency compensation to allow a gain of 40 at 200 kHz. The MC1539 operational amplifier can be tailored for this use; and the MC1520 operational amplifier does it directly.

FIGURE 31 – LINEAR GAIN CONTROL



(A)

(B)



NOTE:
Linear gain control of a 1-volt peak-to-peak signal is performed with a 0-to-1-volt control voltage. If V_C is 0.5 volt the output will be 0.5 volt p-p.

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OPERATIONS AND APPLICATIONS INFORMATION INDEX

ORDERING INFORMATION

Device	Temperature Range	Package
MC1496G	0°C to +70°C	Metal Can
MC1496L	0°C to +70°C	Ceramic DIP
MC1496P	0°C to +70°C	Plastic DIP
MC1596G	−55°C to +125°C	Metal Can
MC1596L	−55°C to +125°C	Ceramic DIP

MC1496
MC1596

BALANCED MODULATOR – DEMODULATOR

. . . designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN-531 for additional design information.

- Excellent Carrier Suppression – 65 dB typ @ 0.5 MHz
  – 50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common-Mode Rejection – 85 dB typ

BALANCED MODULATOR – DEMODULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

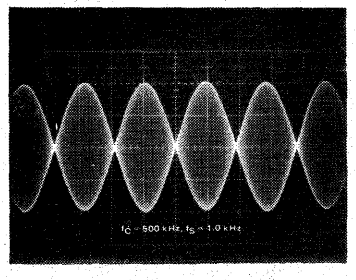


FIGURE 1 – SUPPRESSED-CARRIER OUTPUT WAVEFORM

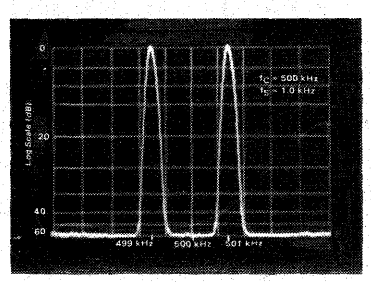


FIGURE 2 – SUPPRESSED-CARRIER SPECTRUM

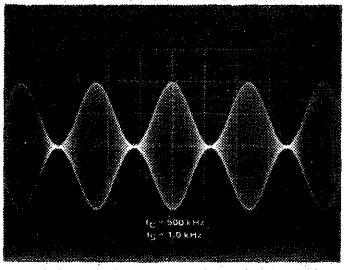
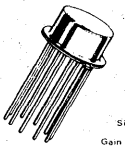
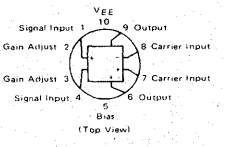
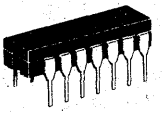


FIGURE 3 – AMPLITUDE-MODULATION OUTPUT WAVEFORM



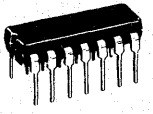
G SUFFIX
METAL PACKAGE
CASE 603





L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1496 only)



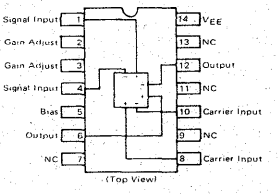
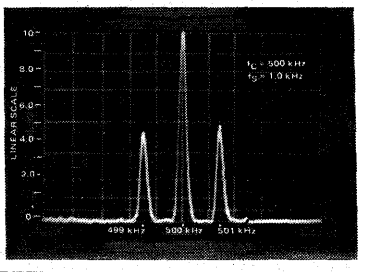


FIGURE 4 – AMPLITUDE-MODULATION SPECTRUM



8

MAXIMUM RATINGS* (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage ($V_6 - V_7$, $V_8 - V_1$, $V_9 - V_7$, $V_9 - V_8$, $V_7 - V_4$, $V_7 - V_1$, $V_8 - V_4$, $V_6 - V_8$, $V_2 - V_5$, $V_3 - V_5$)	ΔV	30	Vdc
Differential Input Signal	$V_7 - V_8$ $V_4 - V_1$	+5.0 $\pm(5+I_5R_e)$	Vdc
Maximum Bias Current	I_5	10	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In-Line Package		575	mW
Derate above T_A = +25°C		3.85	mW/°C
Metal Package		680	mW
Derate above T_A = +25°C		4.6	mW/°C
Operating Temperature Range	T_A		°C
MC1496		0 to +70	
MC1596		-55 to +125	
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS* (V_{CC} = +12 Vdc, V_{EE} = -8.0 Vdc, I_5 = 1.0 mAdc, R_L = 3.9 kΩ, R_e = 1.0 kΩ, T_A = +25°C unless otherwise noted) (All input and output characteristics are single-ended unless otherwise noted.)

Characteristic	Fig	Note	Symbol	MC1596 Min	MC1596 Typ	MC1596 Max	MC1496 Min	MC1496 Typ	MC1496 Max	Unit
Carrier Feedthrough	5	1	V_{CFT}							μV(rms)
V_C = 60 mV(rms) sine wave and f_C = 1.0 kHz				–	40	–	–	40	–	
offset adjusted to zero f_C = 10 MHz				–	140	–	–	140	–	
V_C = 300 mVp-p square wave:										mV(rms)
offset adjusted to zero f_C = 1.0 kHz				–	0.04	0.2	–	0.04	0.4	
offset not adjusted f_C = 1.0 kHz				–	20	100	–	20	200	
Carrier Suppression	5	2	V_{CS}							dB
f_S = 10 kHz, 300 mV(rms)										
f_C = 500 kHz, 60 mV(rms) sine wave				50	65	–	40	65	–	
f_C = 10 MHz, 60 mV(rms) sine wave				–	50	–	–	50	–	k
Transadmittance Bandwidth (Magnitude) (R_L = 50 ohms)	8	8	BW_{3dB}							MHz
Carrier Input Port, V_C = 60 mV(rms) sine wave				–	300	–	–	300	–	
f_S = 1.0 kHz, 300 mV(rms) sine wave										
Signal Input Port, V_S = 300 mV(rms) sine wave				–	80	–	–	80	–	
$\lvert V_C \rvert$ = 0.5 Vdc										
Signal Gain	10	3	A_{VS}	2.5	3.5	–	2.5	3.5	–	V/V
V_S = 100 mV(rms), f = 1.0 kHz; $\lvert V_C \rvert$ = 0.5 Vdc										
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz	6	–								
Parallel Input Resistance			r_{ip}	–	200	–	–	200	–	kΩ
Parallel Input Capacitance			c_{ip}	–	2.0	–	–	2.0	–	pF
Single-Ended Output Impedance, f = 10 MHz	6	–								
Parallel Output Resistance			r_{op}	–	40	–	–	40	–	kΩ
Parallel Output Capacitance			c_{op}	–	5.0	–	–	5.0	–	pF
Input Bias Current	7	–								μA
$I_{bS} = \frac{I_1 + I_4}{2}$; $I_{bC} = \frac{I_7 + I_8}{2}$			I_{bS}	–	12	25	–	12	30	
			I_{bC}	–	12	25	–	12	30	
Input Offset Current	7	–								μA
$I_{ioS} = I_1 - I_4$; $I_{ioC} = I_7 - I_8$			$\lvert I_{ioS} \rvert$	–	0.7	5.0	–	0.7	7.0	
			$\lvert I_{ioC} \rvert$	–	0.7	5.0	–	0.7	7.0	
Average Temperature Coefficient of Input Offset Current (T_A = -55°C to +125°C)	7	–	$\lvert TC_{Iio} \rvert$	–	2.0	–	–	2.0	–	nA/°C
Output Offset Current ($I_6 - I_9$)	7	–	$\lvert I_{oo} \rvert$	–	14	50	–	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = -55°C to +125°C)	7	–	$\lvert TC_{Ioo} \rvert$	–	90	–	–	90	–	nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz	9	4	CMV	–	5.0	–	–	5.0	–	Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz, $\lvert V_C \rvert$ = 0.5 Vdc	9	–	ACM	–	-85	–	–	-85	–	dB
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)	10	–	V_o	–	8.0	–	–	8.0	–	Vdc
Differential Output Voltage Swing Capability	10	–	V_{out}	–	8.0	–	–	8.0	–	Vp-p
Power Supply Current	7	6								mAdc
$I_6 + I_9$			I_{CC}	–	2.0	3.0	–	2.0	4.0	
I_{10}			I_{EE}	–	3.0	4.0	–	3.0	5.0	
DC Power Dissipation	7	5	P_D	–	33	–	–	33	–	mW

* Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

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GENERAL OPERATING INFORMATION *

Note 1 – Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R_1 of Figure 5).

Note 2 – Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1596 has been characterized with a 60 mV(rms) sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair – or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude (see Note 3 and Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Note 3 – Signal Gain and Maximum Input Level

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \text{ where } r_e = \frac{26\text{ mV}}{I_5\text{ (mA)}}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I_5

$$V_S \leq I_5 R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 10, V_S corresponds to a maximum value of 1 volt peak.

Note 4 – Common-Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen (see Note 6).

Note 5 – Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming $V_9 = V_6$, $I_5 = I_6 = I_9$ and ignoring base current, $P_D = 2\,I_5\,(V_6 - V_{10}) + I_5\,(V_5 - V_{10})$ where subscripts refer to pin numbers.

Note 6 – Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions. See Note 3 for R_e equation.

A. Operating Current

The internal bias currents are set by the conditions at pin 5. Assume:

$$I_5 = I_6 = I_9$$

$$I_B \ll I_C \text{ for all transistors}$$

then:

$$R_5 = \frac{V^- - \phi}{I_5} - 500\ \Omega \quad \text{where: } R_5 \text{ is the resistor between pin 5 and ground}$$
$$\phi = 0.75\text{ V at } T_A = +25^\circ C$$

The MC1596 has been characterized for the condition I_5 = 1.0 mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_6 = V_9 = V^+ - I_5 R_L$$

Note 7 – Biasing

The MC1596 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$30\text{ Vdc} \geq [(V_6, V_9) - (V_7, V_8)] \geq 2\text{ Vdc}$$

$$30\text{ Vdc} \geq [(V_7, V_8) - (V_1, V_4)] \geq 2.7\text{ Vdc}$$

$$30\text{ Vdc} \geq [(V_1, V_4) - (V_5)] \geq 2.7\text{ Vdc}$$

The foregoing conditions are based on the following approximations:

$$V_6 = V_9, \quad V_7 = V_8, \quad V_1 = V_4$$

Bias currents flowing into pins 1, 4, 7, and 8 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Note 8 – Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$Y_{21C} = \left.\frac{i_o\text{ (each sideband)}}{v_s\text{ (signal)}}\right| V_o = 0$$

Signal transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$Y_{21S} = \left.\frac{i_o\text{ (signal)}}{v_s\text{ (signal)}}\right| V_C = 0.5\text{ Vdc}, V_o = 0$$

*Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

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Note 9 – Coupling and Bypass Capacitors C_1 and C_2

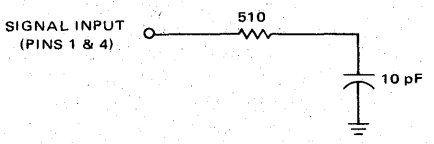
Capacitors C_1 and C_2 (Figure 5) should be selected for a reactance of less than 5.0 ohms at the carrier frequency.

Note 10 – Output Signal, V_o

The output signal is taken from pins 6 and 9, either balanced or single-ended. Figure 12 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single-ended output connection.

Note 11 – Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.



An alternate method for low-frequency applications is to insert a 1 k-ohm resistor in series with the inputs, pins 1 and 4. In this case input current drift may cause serious degradation of carrier suppression.

TEST CIRCUITS

FIGURE 5 – CARRIER REJECTION AND SUPPRESSION

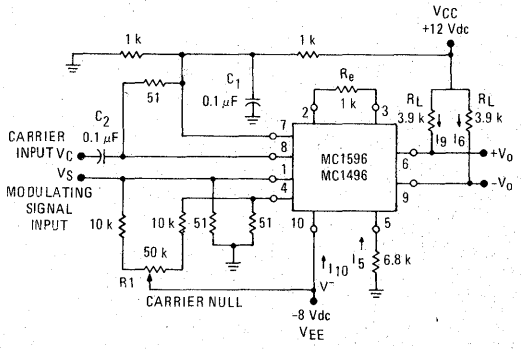


FIGURE 6 – INPUT-OUTPUT IMPEDANCE

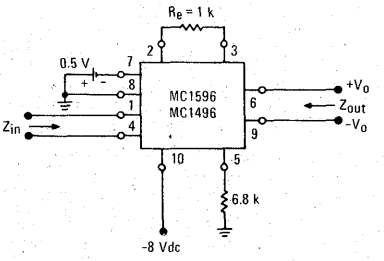


FIGURE 7 – BIAS AND OFFSET CURRENTS

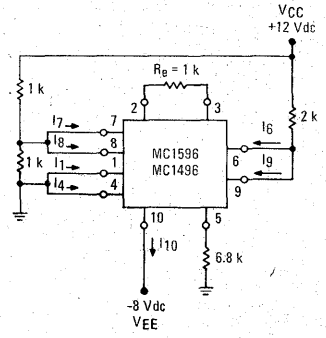
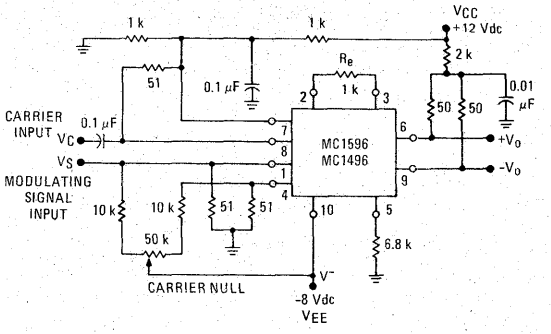


FIGURE 8 – TRANSCONDUCTANCE BANDWIDTH



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

TEST CIRCUITS (continued)

FIGURE 9 – COMMON-MODE GAIN

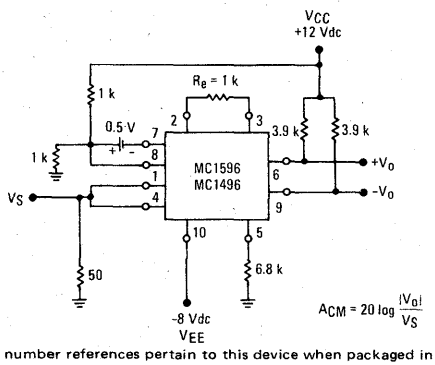
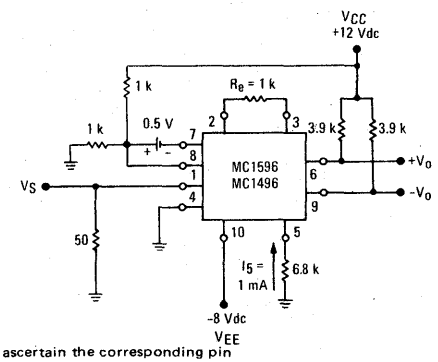


FIGURE 10 – SIGNAL GAIN AND OUTPUT SWING



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 11 – SIDEBAND OUTPUT versus CARRIER LEVELS

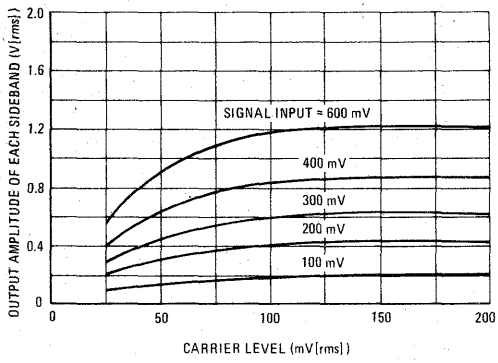


FIGURE 12 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT RESISTANCE versus FREQUENCY

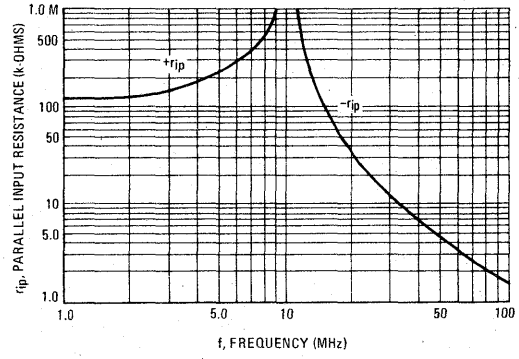


FIGURE 13 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

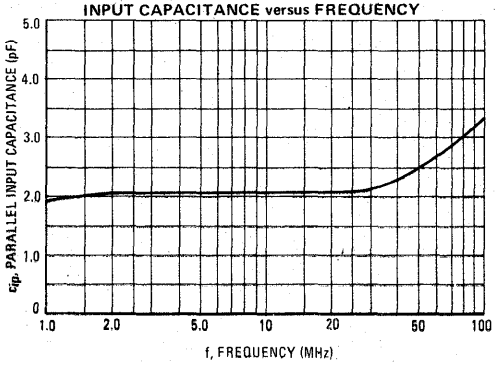
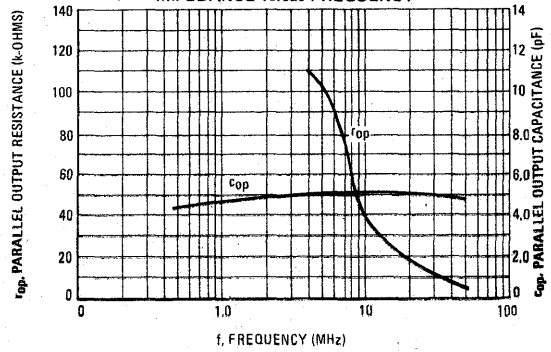


FIGURE 14 – SINGLE-ENDED OUTPUT IMPEDANCE versus FREQUENCY



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TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 15 – SIDEBAND AND SIGNAL PORT TRANSADMITTANCES versus FREQUENCY

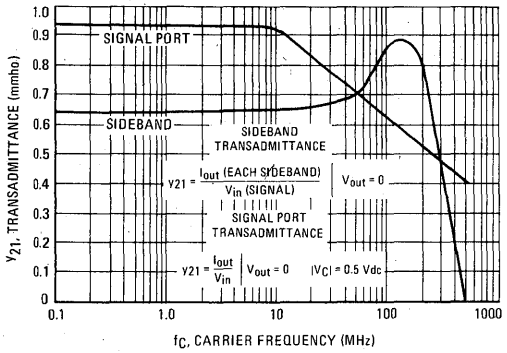


FIGURE 16 – CARRIER SUPPRESSION versus TEMPERATURE

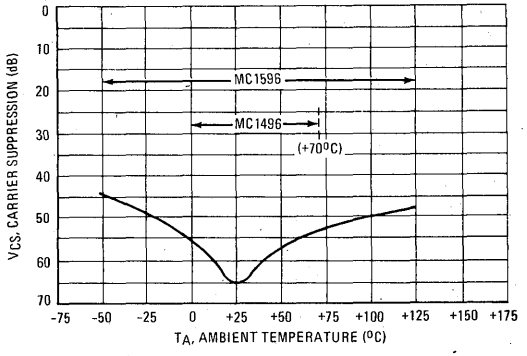


FIGURE 17 – SIGNAL-PORT FREQUENCY RESPONSE

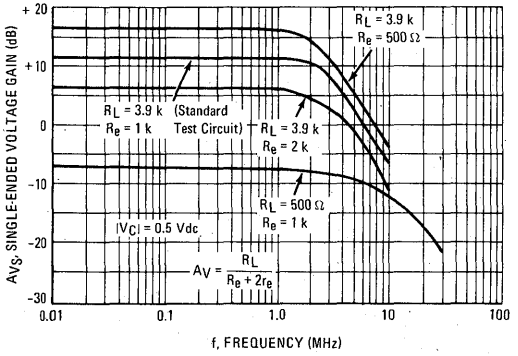


FIGURE 18 – CARRIER SUPPRESSION versus FREQUENCY

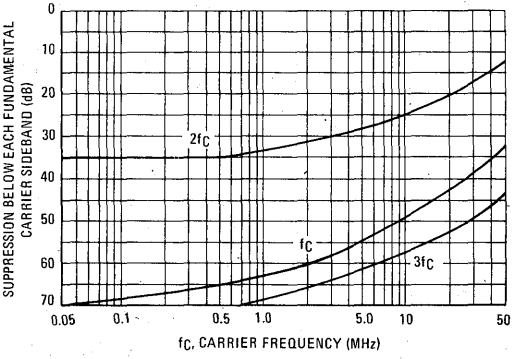


FIGURE 19 – CARRIER FEEDTHROUGH versus FREQUENCY

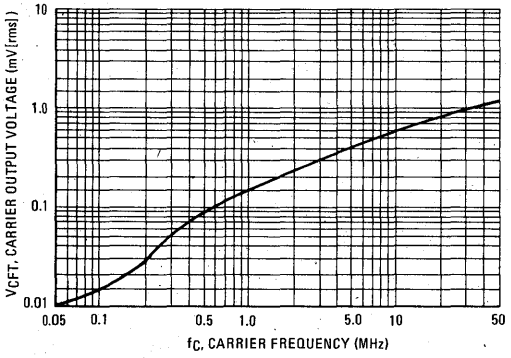
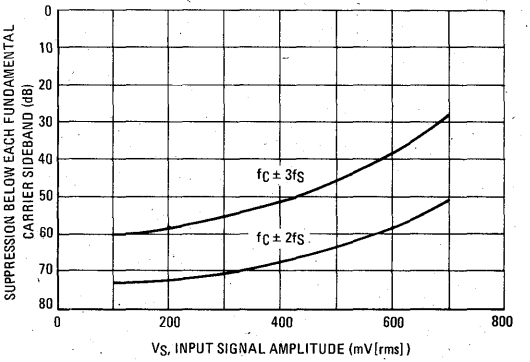


FIGURE 20 – SIDEBAND HARMONIC SUPPRESSION versus INPUT SIGNAL LEVEL



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TYPICAL CHARACTERISTICS (continued)

FIGURE 21 – SUPPRESSION OF CARRIER HARMONIC SIDEBANDS versus CARRIER FREQUENCY

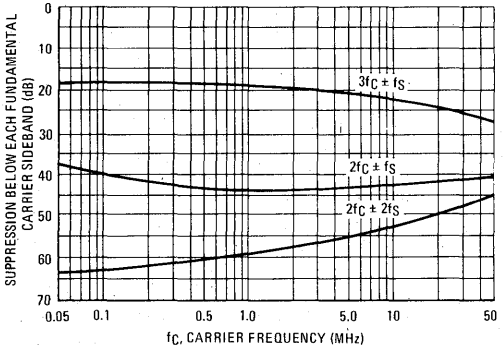
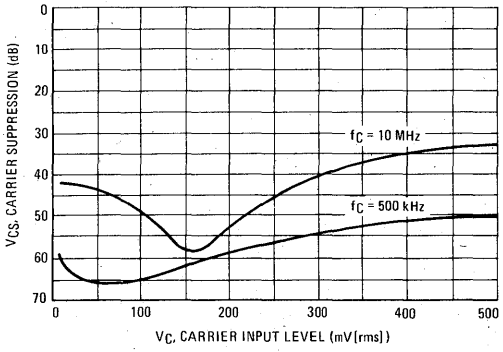


FIGURE 22 – CARRIER SUPPRESSION versus CARRIER INPUT LEVEL



OPERATIONS INFORMATION

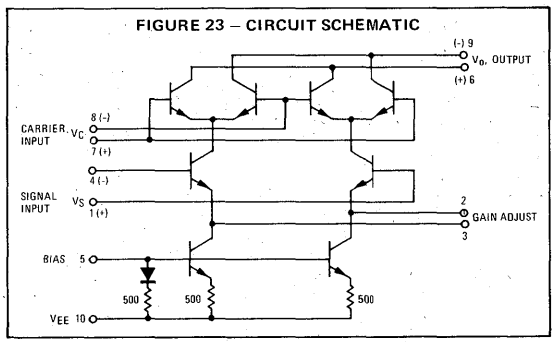
The MC1596/MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

FIGURE 23 – CIRCUIT SCHEMATIC



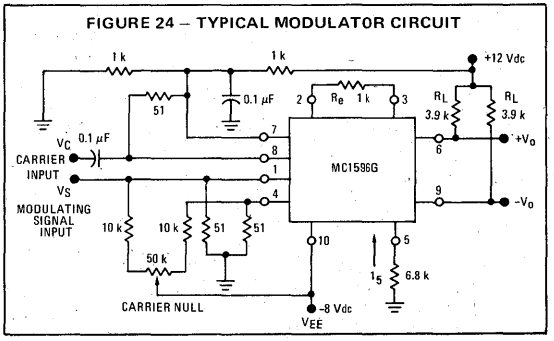
Signal Levels

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

FIGURE 24 – TYPICAL MODULATOR CIRCUIT



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

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OPERATIONS INFORMATION (continued)

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$V = (I_5)(R_E) \text{ volts peak.}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.

FIGURE 25 – TABLE 1
VOLTAGE GAIN AND OUTPUT FREQUENCIES

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level dc	$\frac{R_L V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$	f_M
High-level dc	$\frac{R_L}{R_E + 2r_e}$	f_M
Low-level ac	$\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High-level ac	$\frac{0.637 R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$, . . .

The gain from the modulating signal input port to the output is the MC1596/MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1596/MC1496 for a low-level modulating signal input and the following carrier input conditions:

1) Low-level dc
2) High-level dc
3) Low-level ac
4) High-level ac

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

NOTES:
1. Low-level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. R_E = Emitter resistance between pins 2 and 3.
6. r_e = Transistor dynamic emitter resistance, at +25°C;

$$r_e \approx \frac{26 \text{ mV}}{I_5 \text{ (mA)}}$$

7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26 \text{ mV at room temperature}$$

APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1596/MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1596/MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single +12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

8

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1596/MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μF capacitors on pins 7 and 8 should be increased to 1.0 μF. Also, the output filter at pin 9 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1596/MC1496, the emitter resistance between pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

APPLICATIONS INFORMATION (continued)

Doubly Balanced Mixer

The MC1596/MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Figure 30 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1596/MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1596/MC1496 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1596/MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1596/MC1496 will then provide an output which is a function of the input signal frequency.

Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

TYPICAL APPLICATIONS

FIGURE 26 – BALANCED MODULATOR
(+12 Vdc SINGLE SUPPLY)

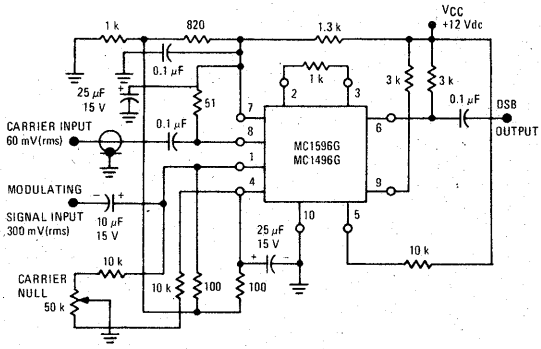


FIGURE 27 – BALANCED MODULATOR-DEMODULATOR

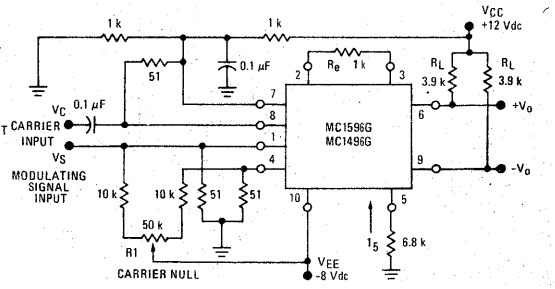


FIGURE 28 – AM MODULATOR CIRCUIT

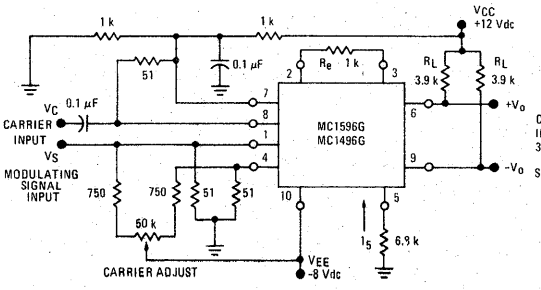
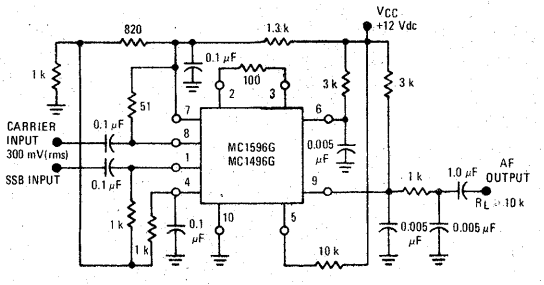


FIGURE 29 – PRODUCT DETECTOR
(+12 Vdc SINGLE SUPPLY)



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TYPICAL APPLICATIONS (continued)

FIGURE 30 – DOUBLY BALANCED MIXER
(BROADBAND INPUTS, 9.0 MHz TUNED OUTPUT)

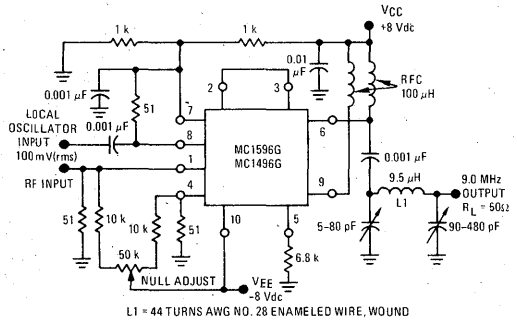


FIGURE 31 – LOW-FREQUENCY DOUBLER

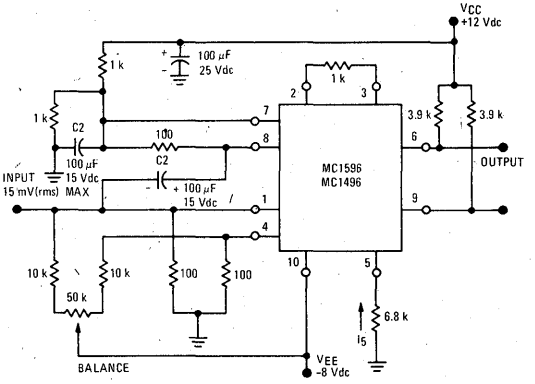
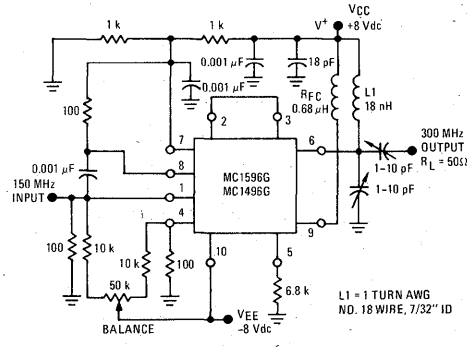
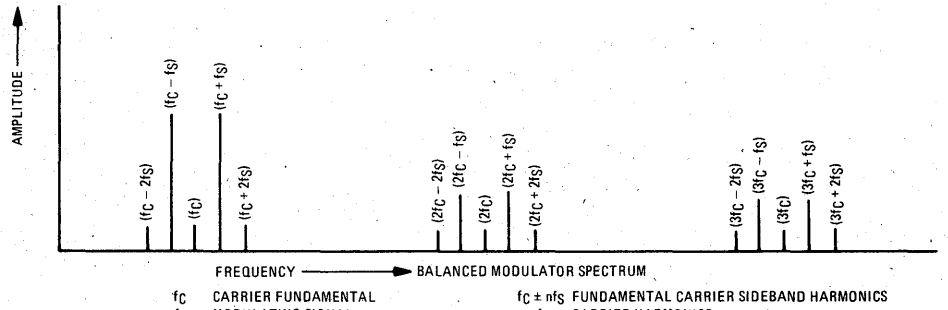


FIGURE 32 – 150 to 300 MHz DOUBLER



DEFINITIONS



f_C	CARRIER FUNDAMENTAL	$f_C \pm nf_S$	FUNDAMENTAL CARRIER SIDEBAND HARMONICS
f_S	MODULATING SIGNAL	nf_C	CARRIER HARMONICS
$f_C \pm f_S$	FUNDAMENTAL CARRIER SIDEBANDS	$nf_C \pm nf_S$	CARRIER HARMONIC SIDEBANDS

Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic or ceramic packaged devices refer to the first page of this specification sheet.

ORDERING INFORMATION

Device	Temperature Range	Package
MC1733G	−55°C to +125°C	Metal Can
MC1733L	−55°C to +125°C	Ceramic DIP
MC1733CG	0°C to +70°C	Metal Can
MC1733CL	0°C to +70°C	Ceramic DIP
MC1733CP	0°C to +70°C	Plastic DIP

MC1733
MC1733C

DIFFERENTIAL VIDEO AMPLIFIER

. . . a wideband amplifier with differential input and differential output. Gain is fixed at 10, 100, or 400 without external components or, with the addition of one external resistor, gain becomes adjustable from 10 to 400.

- Bandwidth – 120 MHz typical @ A_{vd} = 10
- Rise Time – 2.5 ns typical @ A_{vd} = 10
- Propagation Delay Time – 3.6 ns typical @ A_{vd} = 10

DIFFERENTIAL VIDEO WIDEBAND AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

FIGURE 1 – BASIC CIRCUIT

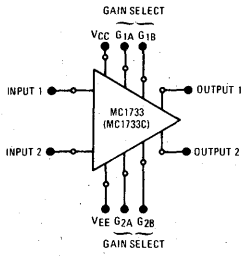


FIGURE 2 – VOLTAGE GAIN ADJUST CIRCUIT

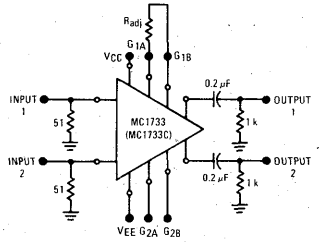
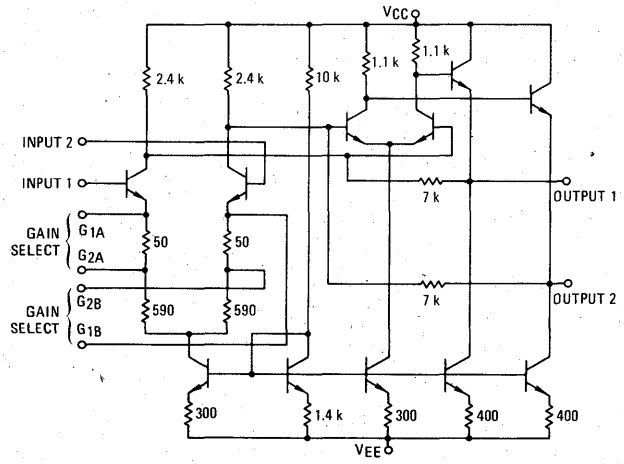
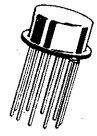
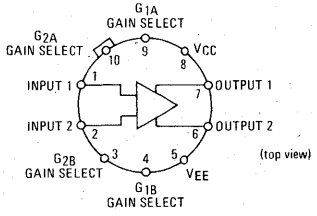


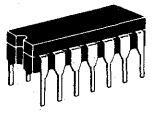
FIGURE 3 – EQUIVALENT CIRCUIT SCHEMATIC



G SUFFIX
METAL PACKAGE
CASE 603
TO-100

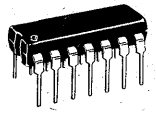


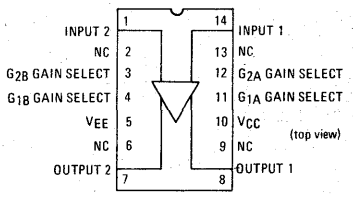




L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P SUFFIX
PLASTIC PACKAGE
CASE 646





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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+8.0 -8.0	Volts
Differential Input Voltage	V_{in}	±5.0	Volts
Common-Mode Input Voltage	V_{ICM}	±6.0	Volts
Output Current	I_O	10	mA
Internal Power Dissipation (Note 1) Metal Can Package Ceramic Dual In-Line Package	P_D	 500 500	mW
Operating Temperature Range MC1733C MC1733	T_A	0 to +70 -55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, at T_A = +25°C unless otherwise noted.)

		MC1733			MC1733C			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Differential Voltage Gain								V/V
Gain 1 (Note 2)	A_{vd}	300	400	500	250	400	600	
Gain 2 (Note 3)		90	100	110	80	100	120	
Gain 3 (Note 4)		9.0	10	11	8.0	10	12	
Bandwidth (R_s = 50 Ω)	BW							MHz
Gain 1		–	40	–	–	40	–	
Gain 2		–	90	–	–	90	–	
Gain 3		–	120	–	–	120	–	
Rise Time (R_s = 50 Ω, V_O = 1 Vp-p)	t_{TLH}							ns
Gain 1	t_{THL}	–	10.5	–	–	10.5	–	
Gain 2		–	4.5	10	–	4.5	12	
Gain 3		–	2.5	–	–	2.5	–	
Propagation Delay (R_s = 50 Ω, V_O = 1 Vp-p)	t_{PLH}							ns
Gain 1	t_{PHL}	–	7.5	–	–	7.5	–	
Gain 2		–	6.0	10	–	6.0	10	
Gain 3		–	3.6	–	–	3.6	–	
Input Resistance	R_{in}							kΩ
Gain 1		–	4.0	–	–	4.0	–	
Gain 2		20	30	–	10	30	–	
Gain 3		–	250	–	–	250	–	
Input Capacitance (Gain 2)	C_{in}	–	2.0	–	–	2.0	–	pF
Input Offset Current (Gain 3)	$\|I_{IO}\|$	–	0.4	3.0	–	0.4	5.0	μA
Input Bias Current (Gain 3)	I_{IB}	–	9.0	20	–	9.0	30	μA
Input Noise Voltage (R_s = 50 Ω, BW = 1 kHz to 10 MHz)	V_n	–	12	–	–	12	–	μV(rms)
Input Voltage Range (Gain 2)	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio	CMRR							dB
Gain 2 (V_{CM} = ±1 V, f ≤ 100 kHz)		60	86	–	60	86	–	
Gain 2 (V_{CM} = ±1 V, f = 5 MHz)		–	60	–	–	60	–	
Supply Voltage Rejection Ratio	PSRR							dB
Gain 2 (ΔV_s = ±0.5 V)		50	70	–	50	70	–	
Output Offset Voltage	V_{OO}							V
Gain 1		–	0.6	1.5	–	0.6	1.5	
Gain 2 and Gain 3		–	0.35	1.0	–	0.35	1.5	
Output Common-Mode Voltage (Gain3)	V_{CMO}	2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing (Gain 2)	V_O	3.0	4.0	–	3.0	4.0	–	Vp-p
Output Sink Current (Gain 2)	I_O	2.5	3.6	–	2.5	3.6	–	mA
Output Resistance	R_{out}	–	20	–	–	20	–	Ω
Power Supply Current (Gain 2)	I_D	–	18	24	–	18	24	mA

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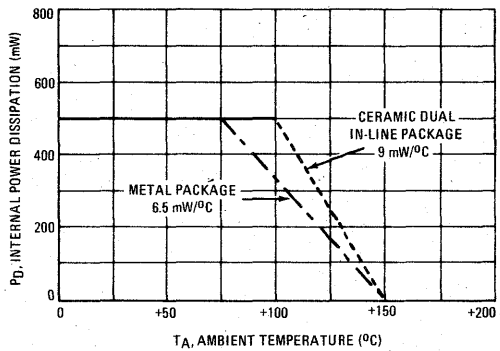
ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, at $T_A = T_{high}$ to T_{low} unless otherwise noted.)*

Characteristic	Symbol	MC1733 Min	MC1733 Typ	MC1733 Max	MC1733C Min	MC1733C Typ	MC1733C Max	Units
Differential Voltage Gain	A_{vd}							V/V
Gain 1 (Note 2)		200	–	600	250	–	600	
Gain 2 (Note 3)		80	–	120	80	–	120	
Gain 3 (Note 4)		8.0	–	12	8.0	–	12	
Input Resistance Gain 2	R_{in}	8.0	–	–	8.0	–	–	kΩ
Input Offset Current (Gain 3)	$\|I_{IO}\|$	–	–	5.0	–	–	6.0	μA
Input Bias Current (Gain 3)	I_{IB}	–	–	40	–	–	40	μA
Input Voltage Range (Gain 2)	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio Gain 2 (V_{CM} = ±1 V, f ≤ 100 kHz)	CMRR	50	–	–	50	–	–	dB
Supply Voltage Rejection Ratio Gain 2 (ΔV_s = ±0.5 V)	PSRR	50	–	–	50	–	–	dB
Output Offset Voltage	V_{OO}							V
Gain 1		–	–	1.5	–	–	1.5	
Gain 2 and Gain 3		–	–	1.2	–	–	1.5	
Output Voltage Swing (Gain 2)	V_O	2.5	–	–	2.5	–	–	Vp-p
Output Sink Current (Gain 2)	I_O	2.2	–	–	2.5	–	–	mA
Power Supply Current (Gain 2)	I_D	–	–	27	–	–	27	mA

*T_{low} = 0°C for MC1733C, -55°C for MC1733
T_{high} = +70°C for MC1733C, +125°C for MC1733.

FIGURE 4 – MAXIMUM ALLOWABLE POWER DISSIPATION



NOTES

Note 1: Derate metal package at 6.5 mW/°C for operation at ambient temperatures above 75°C and dual in-line package at 9 mW/°C for operation at ambient temperatures above 100°C (see Figure 4). If operation at high ambient temperatures is required (MC1733) a heatsink may be necessary to limit maximum junction temperature to 150°C. Thermal resistance, junction-to-case, for the metal package is 69.4°C per Watt.
Note 2: Gain Select pins G_{1A} and G_{1B} connected together.
Note 3: Gain Select pins G_{2A} and G_{2B} connected together.
Note 4: All Gain Select pins open.

TYPICAL CHARACTERISTICS

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 5 – SUPPLY CURRENT versus TEMPERATURE

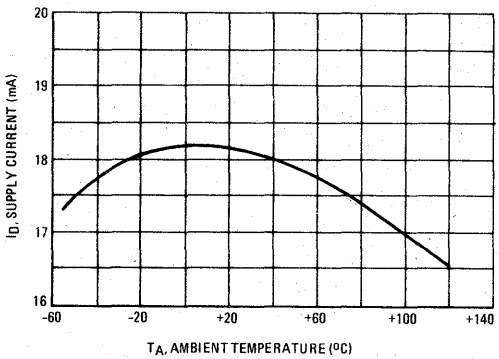
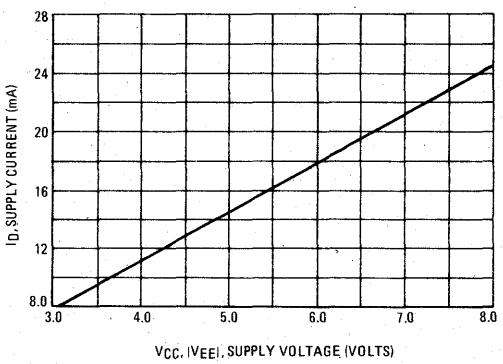


FIGURE 6 – SUPPLY CURRENT versus SUPPLY VOLTAGE



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TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +6.0 Vdc, V_{EE} = –6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 7 – GAIN versus TEMPERATURE

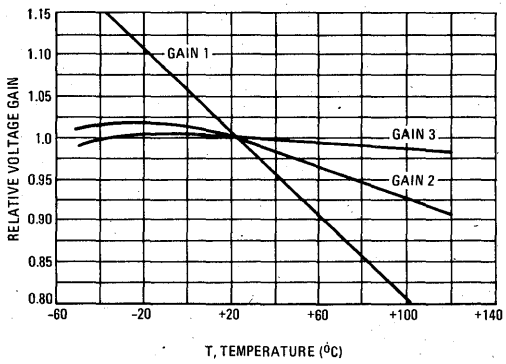


FIGURE 8 – GAIN versus FREQUENCY

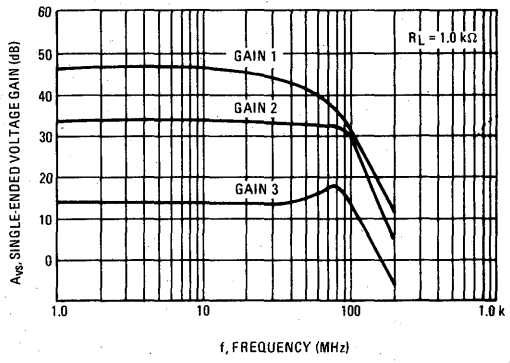


FIGURE 9 – GAIN versus SUPPLY VOLTAGE

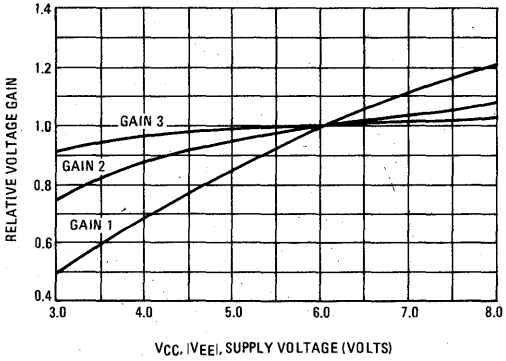


FIGURE 10 – GAIN versus R_{ADJUST}

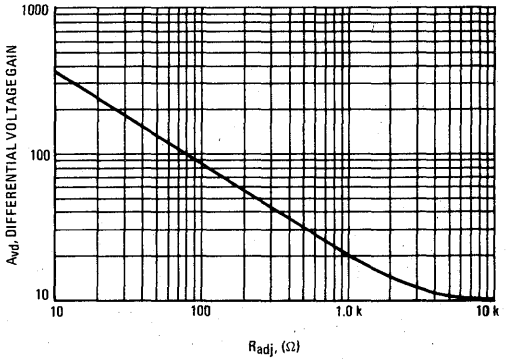


FIGURE 11 – GAIN versus FREQUENCY and SUPPLY VOLTAGE

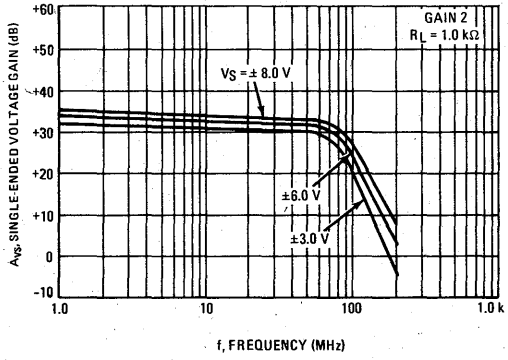
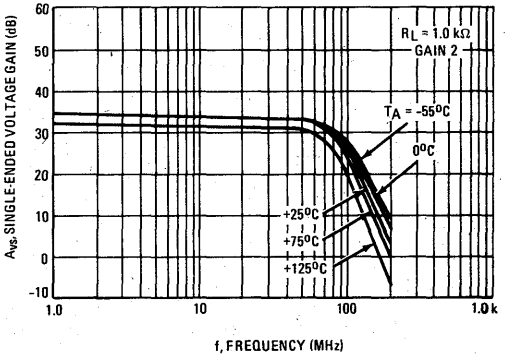


FIGURE 12 – GAIN versus FREQUENCY and TEMPERATURE



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TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 13 – PULSE RESPONSE versus GAIN

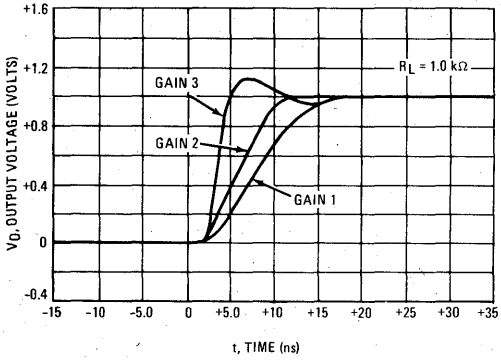


FIGURE 14 – PULSE RESPONSE versus SUPPLY VOLTAGE

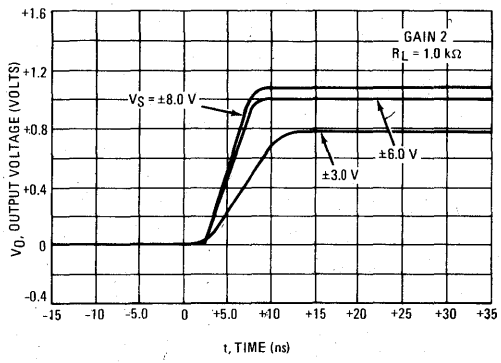


FIGURE 15 – PULSE RESPONSE versus TEMPERATURE

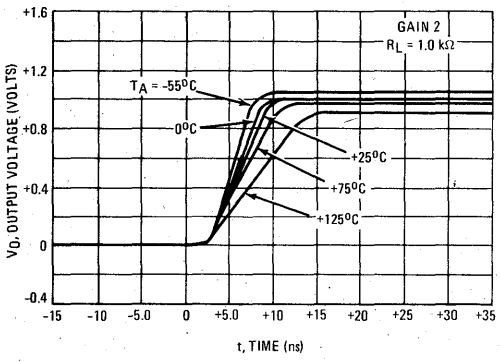


FIGURE 16 – DIFFERENTIAL OVERDRIVE RECOVERY TIME

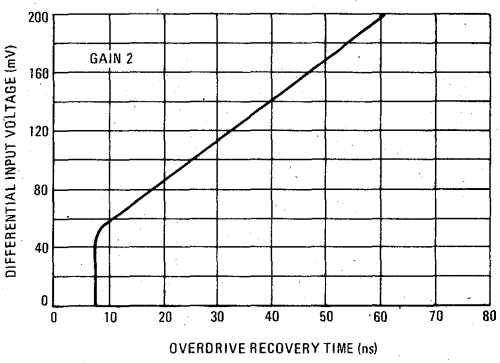


FIGURE 17 – PHASE SHIFT versus FREQUENCY

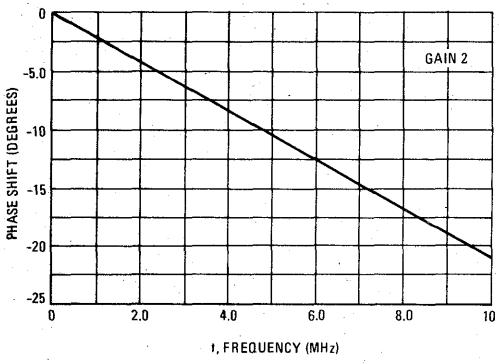
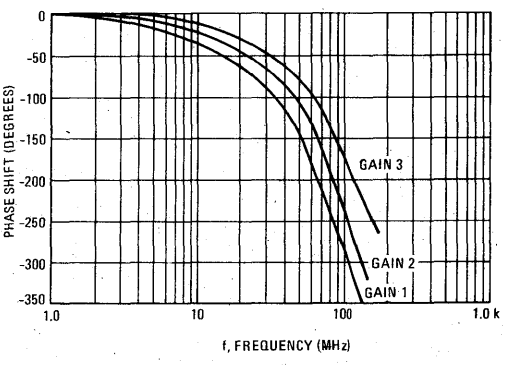


FIGURE 18 – PHASE SHIFT versus FREQUENCY



8

TYPICAL CHARACTERISTICS (Continued)

(V_{CC} = +6.0 Vdc, V_{EE} = -6.0 Vdc, T_A = +25°C unless otherwise noted.)

FIGURE 19 – INPUT RESISTANCE versus TEMPERATURE

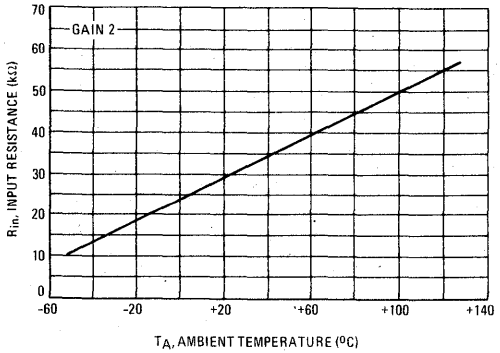


FIGURE 20 – INPUT NOISE VOLTAGE

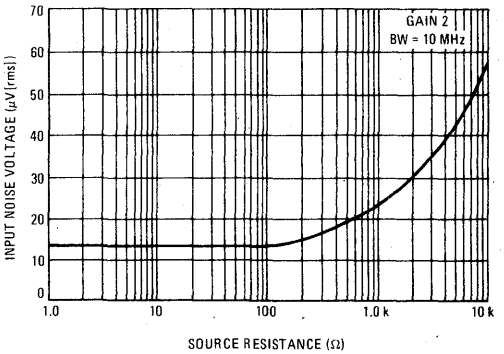


FIGURE 21 – OUTPUT VOLTAGE SWING and SINK CURRENT versus SUPPLY VOLTAGE

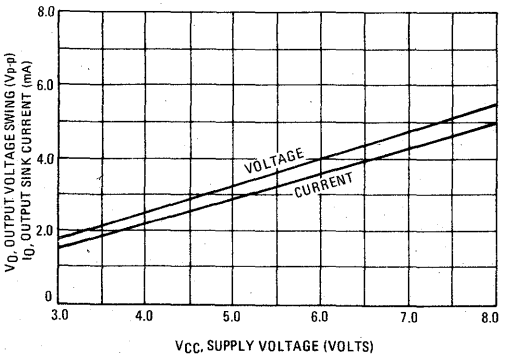


FIGURE 22 – OUTPUT VOLTAGE SWING versus LOAD RESISTANCE

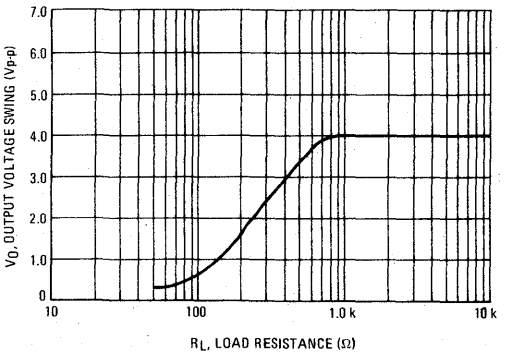


FIGURE 23 – OUTPUT VOLTAGE SWING versus FREQUENCY

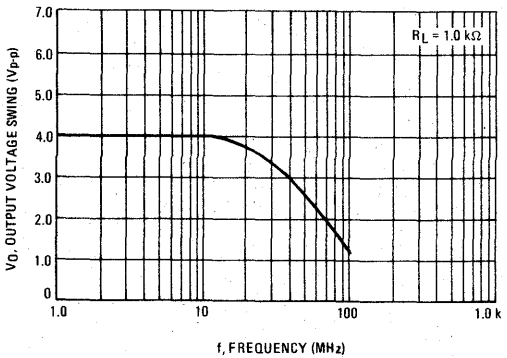
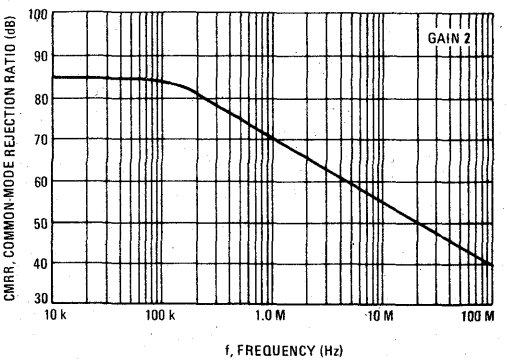


FIGURE 24 – COMMON-MODE REJECTION RATIO



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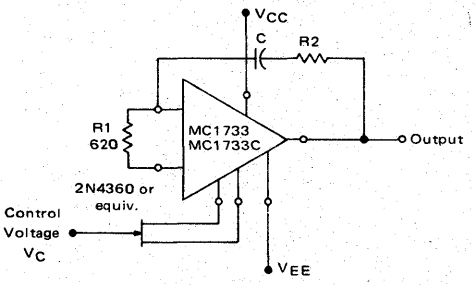
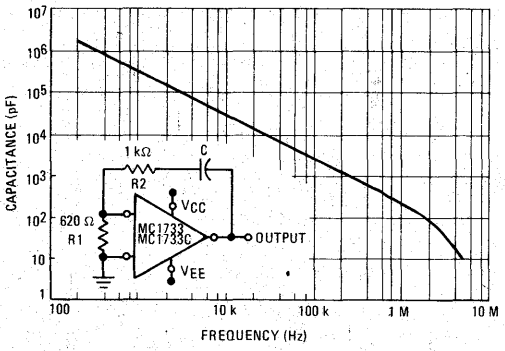
APPLICATIONS INFORMATION

FIGURE 25 – VOLTAGE CONTROLLED OSCILLATOR



By changing the voltage V_C the gain will vary over a range of 10 to 400. This will give a frequency variation about the value set by the capacitor and shown in Figure 26.

FIGURE 26 – OSCILLATOR FREQUENCY FOR VARIOUS CAPACITOR VALUES



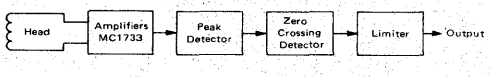
TAPE, DRUM OR DISC MEMORY READ AMPLIFIERS

The first of several methods to be discussed is shown in Figure 27. This block diagram describes a simple Read circuit with no threshold circuitry. Each block represents a basic function that must be performed by the Read circuit. The first block, referred to as "amplfiication", increases the level of the signal available from the Read head to a level adequate to drive the peak detector. Obviously, these signal levels will vary depending on factors such as tape speed, whether the system used is disc or tape, and the type of head and the circuitry used. For a representative tape system, levels of 7 to 25 mV for the signal from the Read head and 2 V for the signal to the peak detector are typical. These signal levels are "peak-to-peak" unless otherwise specified. On the basis of the signal levels mentioned above, the overall amplification required is 38 to 49 dB.

How the overall gain requirement is implemented will depend somewhat on the system used. For instance, a tape cassette system with variable tape speed may utilize a first stage for gain and a second stage primarily for gain control. Thus, a typical circuit would utilize 35 dB in the first stage and 10 to 15 dB in the second stage.

Devices suitable for use as amplifiers fall into one of two categories, operational amplifiers or wideband video amplifiers. Lower speed equipment with low transfer rates commonly uses low cost operational amplifiers. Examples of these are the MC1741, MC1458, MC1709, and MLM301. Equipment requiring higher transfer rates, such as disc systems normally use wideband amplifiers such as the MC1733. The actual cross-over point where wideband amplifiers are used exclusively varies with equipment design. For purposes of comparison, the MLM301 has slightly less than a 40 dB open-loop gain at 100 kHz; the MC1741, a compensated op-amp, has approximately 20 dB open loop gain at 100 kHz; the MC1733 has approximately 33 dB of gain out to 100 MHz (depending on gain option and loading).

FIGURE 27 – TYPICAL READ CIRCUIT (METHOD 1)



There are a number of ways to implement the peak detector function. However, the simplest and most widely used method is a passive differentiator that generates "zero-crossings" for each of the data peaks in the Read signal.

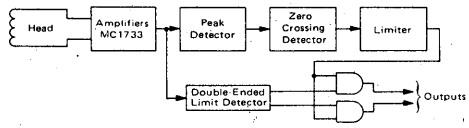
The actual circuitry used to differentiate the Read signal varies from a differential LC type in disc systems to a simple RC type in reel and cassette systems. Either type, of course, attenuates the signal by an amount depending on the circuit used and system specifications. A good approximation of attenuation using the RC type is 20 dB. Thus, the 2 V signal going into the differentiator is reduced to 200 mV.

The next block in Figure 27 to be discussed is the zero-crossing detector. In most cases detection of the zero-crossings is combined with the limiter. These functions serve to generate a TTL compatible pulse waveform with "edges" corresponding to zero-crossings. For low transfer rates, the circuit often used consists of an operational amplifier with series or shunt limiting. For higher transfer rates (greater than 100K B/S) comparators are used.

The method described above is often modified to include threshold sensing. In Figure 28, the function called "double-ended, limit-detector" enables the output NAND gate when either the negative or positive data peaks of the Read signal exceed a predetermined threshold. This function can be implemented in either of two ways. One method first rectifies the signal before it is applied to a comparator with a set threshold. The other method utilizes two comparators, one comparator for positive-going peaks and the other for negative-going peaks. These comparator outputs are then combined in the output logic gates.

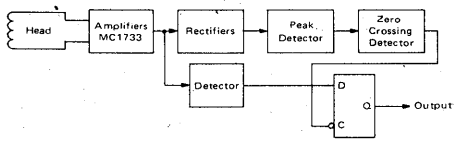
APPLICATIONS INFORMATION (continued)

FIGURE 28 – READ CIRCUIT (METHOD 2)



Another common technique is shown in Figure 29. The branch labeled rectifiers, peak detector, etc., provides a clock transition of the D flip-flop that corresponds to the peak of both the positive and negative-going data peaks. This branch may include threshold circuitry prior to the peak detector. The detector in the lower path detects whether the signal peaks are positive or negative and feeds this data to the flip-flop. This detector can be implemented using a comparator with pre-set threshold.

FIGURE 29 – READ CIRCUIT (METHOD 3)

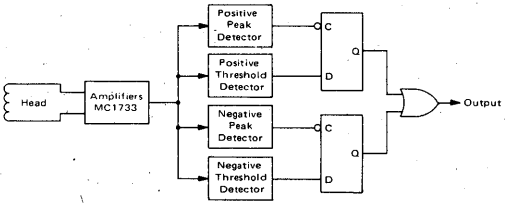


The technique shown in Figure 30 uses separate circuits with threshold provisions for both negative and positive peaks. The peak detectors and threshold detectors may be implemented with two comparators and two passive differentiators.

Each of the methods shown offer certain intrinsic advantages or disadvantages. The overall decision as to which method to use however often involves other important considerations. These could include cost and system requirements or circuitry other than simply the Read circuitry. For instance, if cost is the predominate overall factor, then approach one may be the only feasible alternative.

Method four was included as a design example because it illustrates several unique advantages. First, it uses threshold sensing to reduce noise peak errors. Second, it may be implemented using only integrated circuits. Third, it offers separate, direct threshold sensing for both positive and negative peaks.

FIGURE 30 – READ CIRCUIT (Method 4)



8

ORDERING INFORMATION

Device	Temperature Range	Package
MC3344L	−40°C to +85°C	Ceramic DIP
MC3344P	−40°C to +85°C	Plastic DIP

MC3344

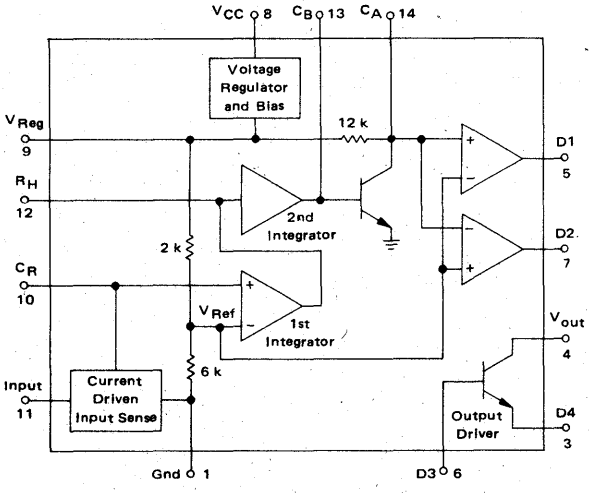
Advance Information

PROGRAMMABLE FREQUENCY SWITCH WITH ADJUSTABLE HYSTERESIS

The MC3344 is a general purpose programmable frequency switch designed for use in systems where a load must be switched on or off at a predetermined frequency. Switch frequency is determined by an external resistor (R_R) and capacitor (C_R). Hysteresis is adjustable and determined by an external resistor (R_H).

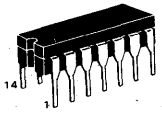
- Isolated Driver Transistor
- Complementary Outputs
- Adjustable Hysteresis
- Wide Supply Operating Range (7 to 24 Volts)
- Wide Input Frequency Range (10 Hz to 100 kHz)
- Internal Regulator
- Ideal for Automotive and Industrial Applications

FIGURE 1 – CIRCUIT BLOCK DIAGRAM

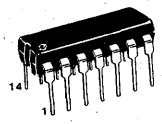


PROGRAMMABLE FREQUENCY SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT

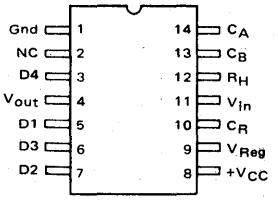


L SUFFIX
CERAMIC PACKAGE
CASE 632
TO - 116



P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



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This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply	V_{CC}	24	Vdc
Peak Input Current	I_I	10	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +15 Vdc unless otherwise specified)

Characteristic	Test Ckts	Symbol	Min	Typ	Max	Unit
Supply Current	2	I_D	–	2.5	4.0	mA
Trigger Reset Voltage	3					Vdc
I_{in} = 200 μA		V_{CR1}	0.25	–	–	
I_{in} = 600 μA		V_{CR2}	–	–	0.25	
Regulator Output Voltage	4	V_{Reg}	4.0	4.5	5.0	Vdc
Threshold Output Voltage $V_{TCR} = V_{CR}/V_{Reg}$	5	V_{TCR}	0.739	0.750	0.761	V/V
Hysteresis Sink Current	6	I_H	100	400	–	μA
Second Comparator Output	7					
D1 Leakage		I_{D1L}	–	–	100	nA
D2 Source		I_{D2S}	100	250	–	μA
D1 Source		I_{D1S}	100	200	–	μA
D2 Leakage		I_{D2L}	–	–	100	nA
Output Driver Gain I_C = 5.0 mA	8	h_{FE1}	50	100	–	–
Output Driver Voltage Standoff I_D = 5.0 mA	9	BV_{CEO}	25	30	–	Vdc
Integrator Transistor Gain $h_{FE2} = \Delta I_C/\Delta I_B$, I_{C1} = 0.4 mA, I_{C2} = 0.6 mA	10	h_{FE2}	50	200	300	–

8

TEST CIRCUITS

FIGURE 2 – SUPPLY CURRENT

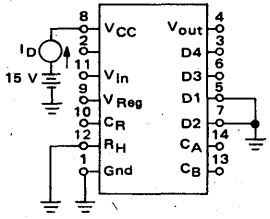
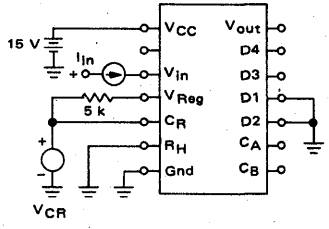


FIGURE 3 – TRIGGER RESET VOLTAGE



I_{in} = 200 μA, $V_{CR} \geq 0.25$ V
I_{in} = 600 μA, $V_{CR} \leq 0.25$ V

FIGURE 4 – REGULATOR OUTPUT VOLTAGE

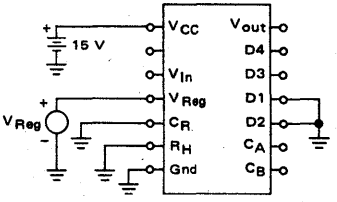
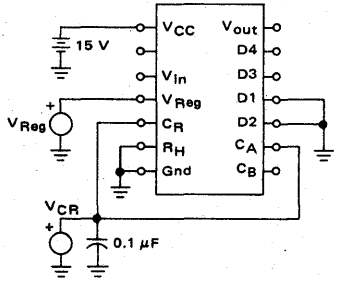


FIGURE 5 – THRESHOLD VOLTAGE RATIO



$V_{TCR} = V_{CR}/V_{Reg}$

FIGURE 6 – HYSTERESIS SINK CURRENT

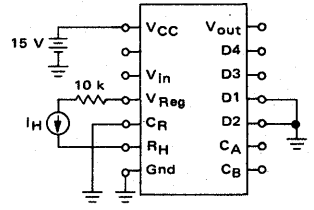
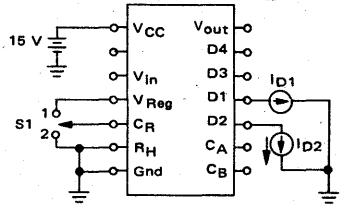


FIGURE 7 – I_{D1L}/I_{D2S}, I_{D2L}/I_{D1S}



I_{D1L}/I_{D2S} – S1 in position 1
I_{D2L}/I_{D1S} – S1 in position 2

FIGURE 8 – OUTPUT DRIVER GAIN

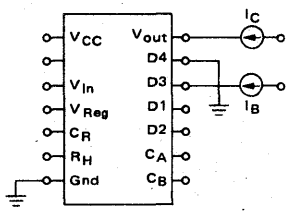


FIGURE 9 – BV_{CEO} OF OUTPUT TRANSISTOR

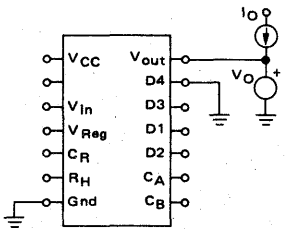
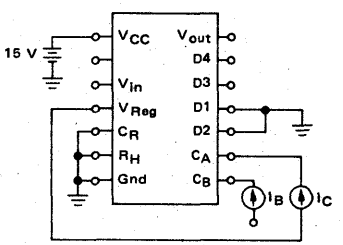


FIGURE 10 – INTEGRATOR TRANSISTOR GAIN



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APPLICATIONS INFORMATION

The voltage regulator and bias section provides the proper biasing and regulated supply voltage to the integrated circuit.

A square wave, when applied to the RC differentiator, provides input current pulses to the IC. The input circuit discharges and clamps, for a predetermined time, the voltage across capacitor C_R. This establishes the initial ramp voltage (V_{sat}) and allows initiation of a new voltage ramp after each positive transistion of the input waveform.

The voltage, V_{CR}, ramps from V_{sat} to the final value, V_{Reg}, charging through R_R.

If V_{CR} is never allowed to reach V_{Ref} due to quick reset pulses, the second integrator amplifier will not be activated, and capacitor C_{AB} is allowed to charge through the 12 kΩ resistor until V_{CA} is greater than V_{Ref}. At this point, D1 will switch ON and D2 will switch OFF. By connecting either D1 or D2 to the D3 drive pin, the output drive transistor may be either switched ON or OFF at the switch point.

If V_{CR} is allowed to ramp above V_{Ref} before being reset, the second integrator amplifier is driven ON which discharges and resets capacitor C_{AB} keeping V_{CA} low with respect to V_{Ref}.

V_{CA} will always be low with respect to V_{Ref} if the time from reset C_R to $V_{CR} = V_{Ref}$ is less than the time from reset C_{AB} to $V_{CA} = V_{Ref}$.

Resistor R_H provides hysteresis around the switch point (i.e., frequency to switch the output driver ON, when connected to the D1 terminal, is higher than the frequency required to switch the output driver OFF). If no hysteresis is desired then the R_H resistor should be omitted and pin 12 grounded.

Circuit Equations:

The first integrator time constant is
$T1 = R_H \parallel R_R\, C_R$. If R_H is omitted then
$T1 = R_R\, C_R$.

The second integrator time constant is
$T2 = (12\text{ k})\,(h_{FE2})\,(C_{AB})$.

$$f1 = \text{Switch Point frequency} \cong \frac{1}{1.39\, R_R\, C_R}$$

$$f2 = \text{Hysteresis Switch Point frequency} \approx \frac{1}{R_R \parallel R_H\, C_R \ln\left[\frac{R_H}{0.25\, R_H - 0.75\, R_R}\right]}$$

FIGURE 11 – TYPICAL APPLICATION

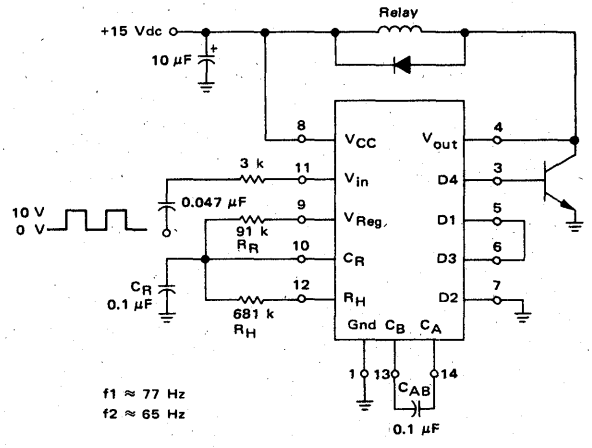
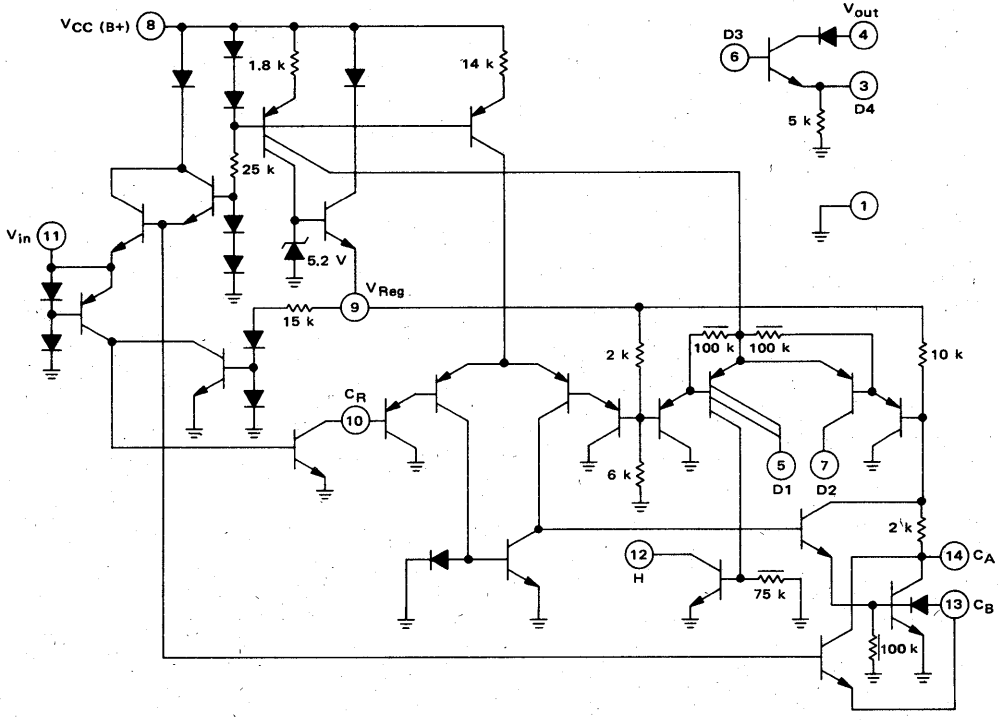


FIGURE 12 – CIRCUIT SCHEMATIC



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

8

ORDERING INFORMATION

Device	Temperature Range	Package
MC3370P	−10°C to +75°C	Plastic DIP

MC3370P

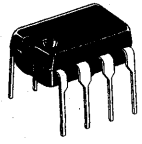
ZERO VOLTAGE SWITCH

. . . designed for use in ac power switching applications with output drive capable of triggering triacs. Other operational features include; (1) a built-in voltage regulator that allows direct ac line operation, (2) a differential input with dual sensor inputs capable of testing the condition of two external sensors and controlling the gate pulse to a triac accordingly; (hysteresis or proportional control to this section may be added if desired) (3) sensor input "open and short" protection; this insures that the triac will never be turned "on" if either of the inputs are shorted or opened (4) a zero crossing detector that synchronizes the triac gate pulses with the zero crossing of the ac line voltage. This eliminates radio frequency interference (RFI) when used with resistive loads.

- Heater Controls
- Photo Controls
- Threshold Detector
- Lamp Driver
- Valve Control
- On-Off Power Controls
- Relay Driver
- Flasher Control
- Formerly MFC8070 in Case 644A Package

ZERO VOLTAGE SWITCH

SILICON MONOLITHIC
FUNCTIONAL CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 626

FIGURE 1 – CIRCUIT SCHEMATIC

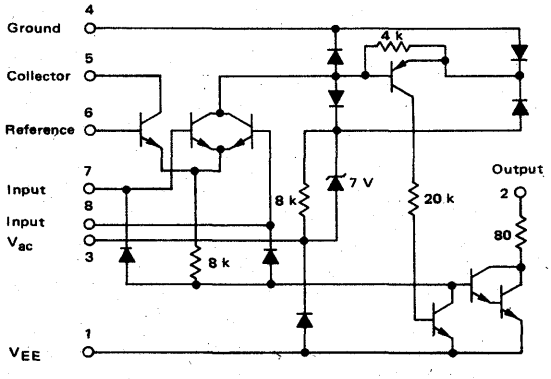


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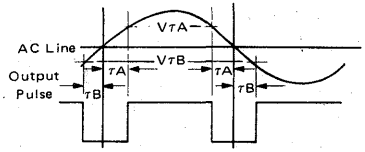
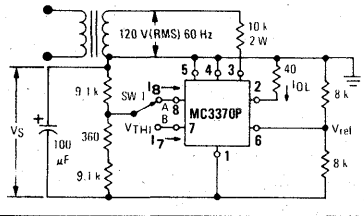
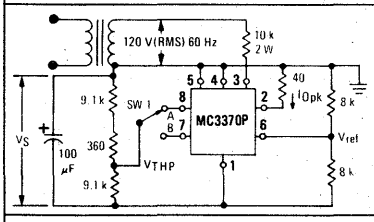
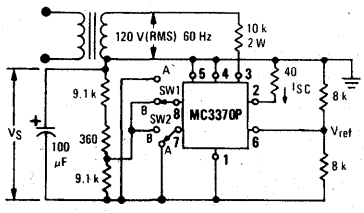
FIGURE 2 – OUTPUT PULSE DEFINITION



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
DC Voltage	V_{4-1}	15	Vdc
DC Voltage	V_{5-1}	15	Vdc
DC Voltage	V_{2-1}	15	Vdc
Peak Supply Current	I_3	35	mA
Power Dissipation Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	1.2 10	Watts mW/°C
Operating Ambient Temperature Range	T_A	-10 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted.)

Characteristic Definitions	Characteristic	Symbol	Min	Typ	Max	Unit
	V_S with Inhibit Output (Sw 1: A or B)	V_{SIO}	–	9.0	11	Vdc
	Output Leakage Current (Sw 1: A or B)	I_{OL}	–	5.0	100	μA
	Input Current 8 (Sw 1: A)	I_8	–	5.0	15	μA
	Input Current 7 (Sw 1: B)	I_7	–	5.0	15	μA
	Inhibit Threshold Voltage (Sw 1: A or B)	V_{THI}	V_{ref} +100 mV	V_{ref} +10 mV	–	Vdc
	V_S with Pulse Output (Sw 1: A or B)	V_{SPO}	6.0	8.5	–	Vdc
	Peak Output Current (Sw 1: A or B)	I_{Opk}	50	80	–	mA
	Pulse Threshold Voltage (Sw 1: A or B)	V_{THP}	–	V_{ref} -10 mV	V_{ref} -100 mV	Vdc
	Output Pulse Width (Sw 1: A or B, See Figure 2)	τA, τB VτA, VτB	–	70 ±4.5	– –	μs V
	Output Current With Input Short (Sw 1: B; Sw 2: A) (Sw 1: A; Sw 2: B)	I_{SC}	– –	5.0 5.0	100 100	μA

TEST CIRCUIT AND TYPICAL CHARACTERISTICS

FIGURE 3 – CIRCUIT WITH INCREASED PULSE WIDTH AND TRIAC DRIVER TO CONTROL HIGH-CURRENT SCR's

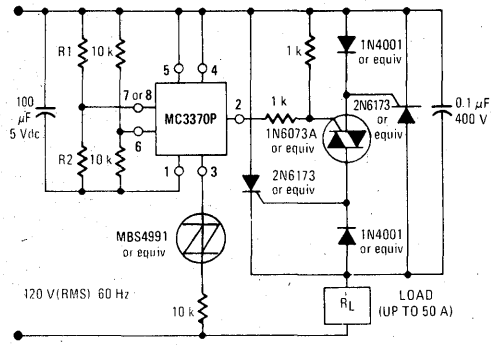
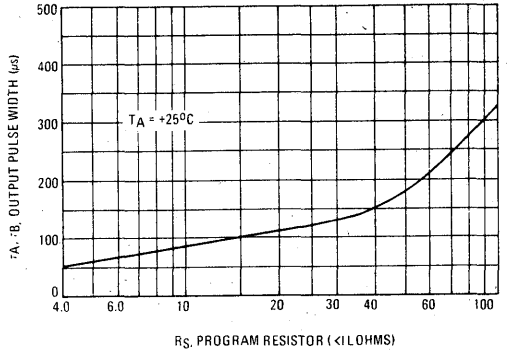
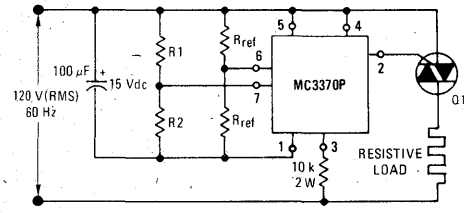


FIGURE 4 – OUTPUT PULSE WIDTH versus SOURCE RESISTANCE (See Figure 6.)



TYPICAL ZERO VOLTAGE SWITCH APPLICATIONS FOR TRIAC CONTROL

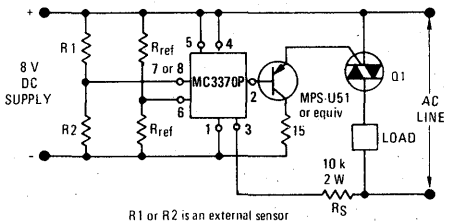
FIGURE 5 – TRIAC CONTROL CIRCUIT



R1 or R2 is an external sensor

Basic triac trigger circuit utilizing the zero crossing detector and the input comparator to control triacs with gate current requirements to 500 mA.

FIGURE 6 – TRIAC CONTROL CIRCUIT WITH CURRENT BOOST UTILIZING DC SUPPLY



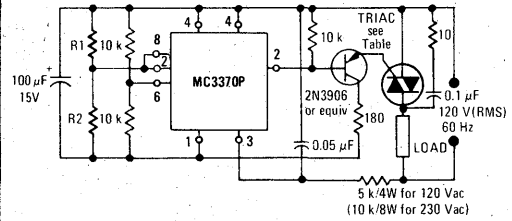
R1 or R2 is an external sensor

Basic dc trigger application using the input comparator to control a PNP capable of furnishing gate drive of approximately 0.5 A.

Suggested circuit to vary output pulse width by value of R_S (See Figure 4).

R2 must be the external sensor for the internal short and open protection to be operative.

FIGURE 7 – TRIAC CONTROL CIRCUIT WITH CURRENT BOOST UTILIZING AC SUPPLY

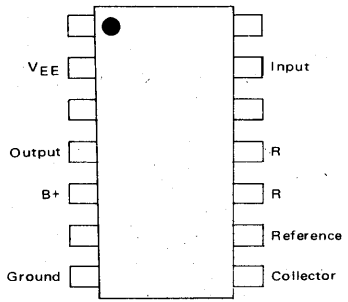


Zero crossing triac control circuit for gate current requirements to 100 mA.

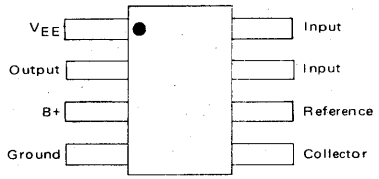
Recommended Motorola triacs for use in circuit.

Maximum Continuous Current (A [RMS])	Triac Family	Case No.
10	2N6151/2N6153 2N6346A/2N6349A	90 (Plastic) 221-024 (Plastic)
10	2N6139/2N6144	86, 250
25	2N6157/2N6165	174, 175, 235
40	2N5441/2N5446	237, 238, 239

PIN COMPARISON OF MC3370P AND GEL300F1 (PA424/CA3059)



GEL300F1/CA3059



MC3370

8

MC3405
MC3505

Advance Information

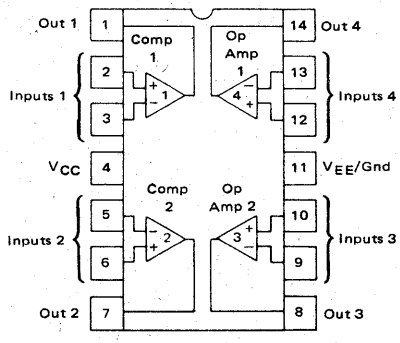
DUAL OPERATIONAL AMPLIFIER AND DUAL COMPARATOR

The MC3405/3505 contains two differential-input operational amplifiers and two comparators, each set capable of single supply operation. This operational amplifier-comparator circuit, better known as the "Operator" will find its applications as a general purpose product for automotive circuits and as an industrial building block.

The MC3405 is specified over the commercial operating temperature range of 0 to +70°C while the MC3505 is specified over the military operating range of -55 to +125°C.

- Operational Amplifiers Equivalent in Performance to MC3403
- Comparators Similar in Performance to MLM339
- Operational Amplifiers are Internally Frequency Compensated
- Supply Operation – 3.0 Volts to 36 Volts
- Dual Supply Operation also Available

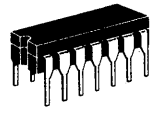
PIN CONNECTIONS



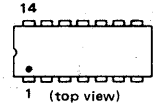
This is advance information and specifications are subject to change without notice.

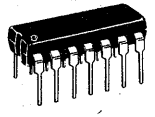
DUAL OPERATIONAL AMPLIFIER AND DUAL VOTAGE COMPARATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116





P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

Device	Temperature Range	Package
MC3405L	0 to +70°C	Ceramic DIP
MC3405P	0 to +70°C	Plastic DIP
MC3505L	-55 to +125°C	Ceramic DIP

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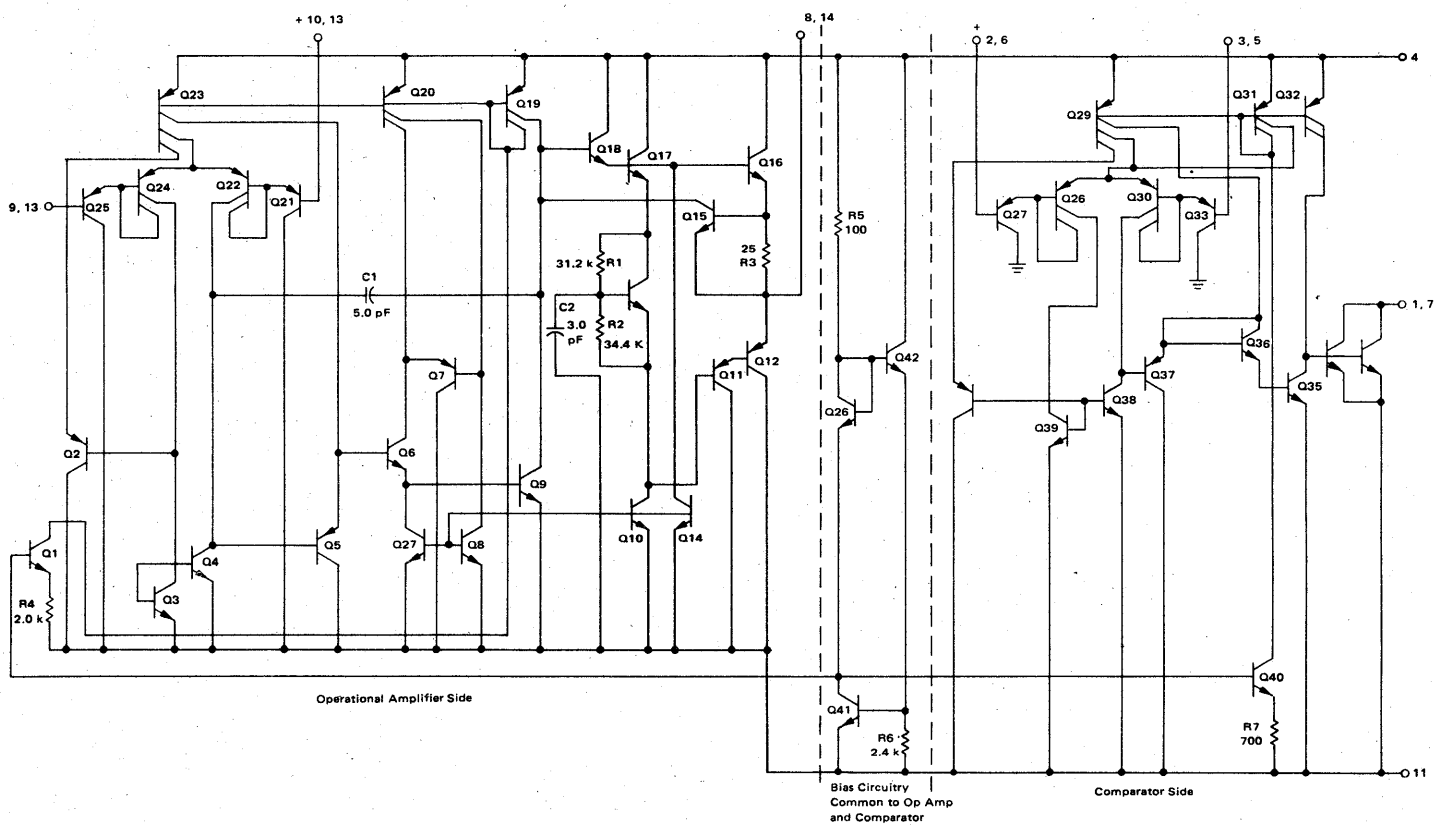
CIRCUIT SCHEMATIC
(1/2 OF CIRCUIT SHOWN)



OPERATIONAL AMPLIFIER SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{CC} V_{EE}	36 +18 −18	Vdc
Input Differential Voltage Range	V_{IDR}	±30	Vdc
Input Common Mode Voltage Range	V_{ICR}	±15	Vdc
Operating Ambient Temperature Range — MC3505 MC3405	T_A	−55 to +125 0 to +70	°C
Storage Temperature Range — Ceramic Package Plastic Package	T_{stg}	−65 to +150 −55 to +125	°C
Operating Junction Temperature Range — Ceramic Package Plastic Package	T_J	175 150	°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	100	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC3505 Min	MC3505 Typ	MC3505 Max	MC3405 Min	MC3405 Typ	MC3405 Max	Unit
Input Offset Voltage ($T_A = T_{low}$ to T_{high})(1)	V_{IO}	— —	2.0 —	5.0 6.0	— —	2.0 —	10 12	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	—	15	—	—	15	—	μV/°C
Input Offset Current ($T_A = T_{low}$ to T_{high})(1)	I_{IO}	— —	— —	50 200	— —	— —	50 200	nA
Input Bias Current ($T_A = T_{low}$ to T_{high})(1)	I_{IB}	— —	200 300	500 1500	— —	200 —	500 800	nA
Large Signal Open Loop Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ) ($T_A = T_{low}$ to T_{high})(1)	A_{VOL}	 50 25	 200 100	 — —	 20 15	 200 —	 — —	V/mV
Power Supply Current (2)	I_{CC} I_{EE}	— —	2.8 2.8	4.0 4.0	— —	2.8 2.8	7.0 7.0	mA mA
Common Mode Rejection Ratio	CMRR	70	90	—	70	90	—	dB
Power Supply Rejection Ratio	PSRR+	—	30	150	—	30	—	dB
Output Voltage (R_L = 10 kΩ) (R_L = 2.0 kΩ) (R_L = 2.0 kΩ, $T_A = T_{low}$ to T_{high})(1)	V_O	 ±12 ±10 ±10	 ±13.5 ±13.0 —	 — — —	 ±12 ±10 ±10	 ±13.5 ±13.0 —	 — — —	Vdc
Input Common Mode Voltage Range	V_{ICR}	+13 − V_{EE}	—	—	+13 − V_{EE}	—	—	Vdc
Output Short-Circuit Current	I_{OS}	±10	±30	±45	±10	±20	±45	mA
Phase Margin	ϕm	—	60	—	—	60	—	°C
Small-Signal Bandwidth (A_V = 1, R_L = 10 kΩ, V_O = 50 mV)	BW	—	1.0	—	—	1.0	—	MHz
Power Bandwidth (A_V = 1, R_L = 2.0 kΩ, V_O = 20 V (p-p), THD = 5%)	BW_P	—	9.0	—	—	9.0	—	kHz
Rise Time	t_{TLH}	—	0.35	—	—	0.35	—	μs
Fall Time	t_{THL}	—	0.35	—	—	0.35	—	μs
Overshoot (A_V = 1, R_L = 10 kΩ, V_O = 50 mV)	OS	—	20	—	—	20	—	%
Slew Rate	SR	—	0.6	—	—	0.6	—	V/μs

(continued)

8

OPERATIONAL AMPLIFIER SECTION (continued)

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC3505			MC3405			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	mV
Input Offset Current	I_{IO}	–	30	50	–	30	50	nA
Input Bias Current	I_{IB}	–	-200	-500	–	-200	-500	nA
Large-Signal Open-Loop Voltage Gain (R_L = 2.0 kΩ)	A_{VOL}	20	200	–	20	200	–	V/mV
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	μV/V
Output Voltage Range (3) (R_L = 10 kΩ, V_{CC} = 5.0 V) (R_L = 10 kΩ, 5.0 V ≤ V_{CC} ≤ 30 V)	V_{OR}	3.3 V_{CC} - 1.7	3.5 V_{CC} - 1.5	– –	3.3 V_{CC} - 1.7	3.5 V_{CC} - 1.5	– –	Vp-p
Power Supply Current(4)	I_{CC}	–	2.5	4.0	–	2.5	7.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	–	–	-120	–	–	-120	–	dB

(1) T_{low} = -55°C for MC3505 T_{high} = +125°C for MC3505
= 0°C for MC3405 = +70°C for MC3405

(2) For Operational Amplifier and Comparator

(3) Output will swing to ground.

(4) Not to exceed miximum package power dissipation.

8

COMPARATOR SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	36	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to +35	Vdc
Sink Current	I_{sink}	20	mA
Operating Ambient Temperature Range — MC3503 MC3405	T_A	-55 to +125 0 to +70	°C
Storage Temperature Range — Ceramic Package Plastic Package	T_{stg}	-65 to +150 -55 to +125	°C
Operating Junction Temperature Range — Ceramic Package Plastic Package	T_J	175 150	°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	100	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC3505 Min	MC3505 Typ	MC3505 Max	MC3405 Min	MC3405 Typ	MC3405 Max	Unit
Input Offset Voltage (T_A = T_{low} to T_{high}) (1), (3)	V_{IO}	– –	2.0 –	5.0 9.0	– –	2.0 –	10 12	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	15	–	–	15	–	μV/°C
Input Offset Current (T_A = T_{low} to T_{high}) (1)	I_{IO}	– –	50 –	75 150	– –	50 –	100 200	nA
Input Bias Current (T_A = T_{low} to T_{high}) (1)	I_{IB}	– –	25 –	500 1500	– –	25 –	500 800	nA
Large-Signal Open Loop Voltage Gain (R_L = 15 kΩ)	A_{VOL}	–	200	–	–	200	–	V/mV
Input Common Mode Voltage Range (T_A = T_{low} to T_{high}) (1)	V_{ICR}	0 0	V_{CC} - 1.5 V_{CC} - 1.7	V_{CC} - 1.7 V_{CC} - 2.0	0 0	V_{CC} - 1.5 V_{CC} - 1.7	V_{CC} - 1.7 V_{CC} - 2.0	V
Input Differential Voltage (All $V_{in} \geq 0$ Vdc)	V_{ID}	–	–	36	–	–	36	V
Sink Current (V_{in} (-) ≥ 1.0 Vdc, V_{in} (+) = 0, $V_O \leq$ 1.5 V)	I_{sink}	6.0	16	–	6.0	16	–	mA
Saturation Voltage (V_{in} (-) = 1.0 Vdc, V_{in} (+) = 0, $I_{sink} \leq$ 4.0 mAdc) (T_A = T_{low} to T_{high}) (1)	V_{sat}	– –	250 –	500 700	– –	250 –	500 700	mV
Output Leakage Current (V_{in} (+) ≥ 1.0 Vdc, V_{in} (-) = 0, V_O = 5.0 Vdc) (T_A = T_{low} to T_{high}) (1)	I_{OL}	– –	0.1 0.1	1.0 1.0	– –	0.1 0.1	1.0 1.0	μA
Large-Signal Response	–	–	300	–	–	300	–	ns
Response Time (2) (V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ)	–	–	1.3	–	–	1.3	–	μs
Low Level Output Voltage (V_{in} (+) = 0 V, V_{in} (-) = 1.0 V, I_{sink} = 4.0 mA) (T_A = T_{low} to T_{high}) (1)	V_{OL}	– –	– –	500 700	– –	– –	500 700	mV

(1) T_{low} = -55°C for MC3505 = 0°C for MC3405 T_{high} = +125°C for MC3505 = +70°C for MC3405

(2) The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals 300 ns is typical.

(3) $V_O \cong$ 1.4 V, R_S = 0 Ω with V+ from 5.0 Vdc to 30 Vdc, and over the input common mode range 0 to V+ -1.7 V.

MC3423
MC3523

Advance Information

OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

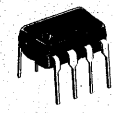
These overvoltage protection circuits (OVP) protect sensitive electronic circuitry from overvoltage transients or regulator failures when used in conjunction with an external "crowbar" SCR. They sense the overvoltage condition and quickly "crowbar" or short circuit the supply, forcing the supply into current limiting or opening the fuse or circuit breaker.

The protection voltage threshold is adjustable and the MC3423/3523 can be programmed for minimum duration of overvoltage condition before tripping, thus supplying noise immunity.

OVERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

PI SUFFIX
PLASTIC PACKAGE
CASE 626

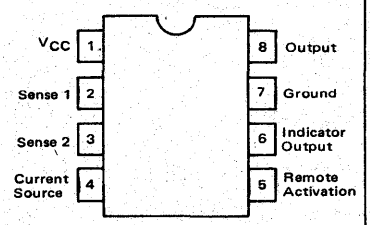


U SUFFIX
CERAMIC PACKAGE
CASE 693

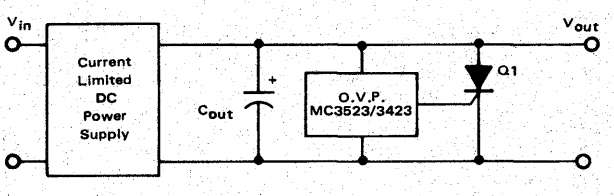
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Differential Power Supply Voltage	V_{CC}-V_{EE}	45	Vdc
Sense Voltage (1)	$V_{Sense\ 1}$	6.8	Vdc
Sense Voltage (2)	$V_{Sense\ 2}$	6.8	Vdc
Remote Activation Input Voltage	V_{act}	7.0	Vdc
Output Current	I_O	300	mA
Operating Ambient Temperature Range MC3423 MC3523	T_A	 0 to +70 –55 to +125	°C
Operating Junction Temperature Range Plastic Package Ceramic Package	T_J	 150 175	°C

PIN CONNECTIONS



TYPICAL APPLICATION



NOTE: A 2N6504 or equivalent is suggested for Q1.

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC3423P1	0 to +70°C	Plastic DIP
MC3423U	0 to +70°C	Ceramic DIP
MC3523U	–55 to +125°C	Ceramic DIP

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This is advance information and specifications are subject to change without notice.

ELECTRICAL CHARACTERISTICS ($V_{CC} - V_{EE} = 5.0$ V, $T_{low} < T_J < T_{high}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}	4.5	–	36	Vdc
Output Voltage	V_O	–	3.0	–	Vdc
Indication Output Current (V_{OL} = 0.4 V)	$I_{O(Ind)}$	–	10	–	mA
Reference Voltage (T_A = 25°C)	V_{ref}	–	2.6	–	Vdc
Temperature Coefficient of Reference Voltage	TCV_{ref}	–	0.08	–	%/°C
Remote Activation Input Current (V_{IH} = 2.0 V)	$I_{in(Ind)}$	–	0.1	–	mA
Source Current	I_{source}	–	0.22	–	mA
Output Current Risetime (T_A = 25°C)	t_r	–	400	–	mA/μs
Propagation Delay (T_A = 25°C)	t_{pd}	–	0.5	–	μs
Supply Current	I_D	–	5.0	–	mA

T_{low} = −55°C for MC3523
= 0°C for MC3423

T_{high} = +125°C for MC3523 and MC3423

FIGURE 1 – BLOCK DIAGRAM

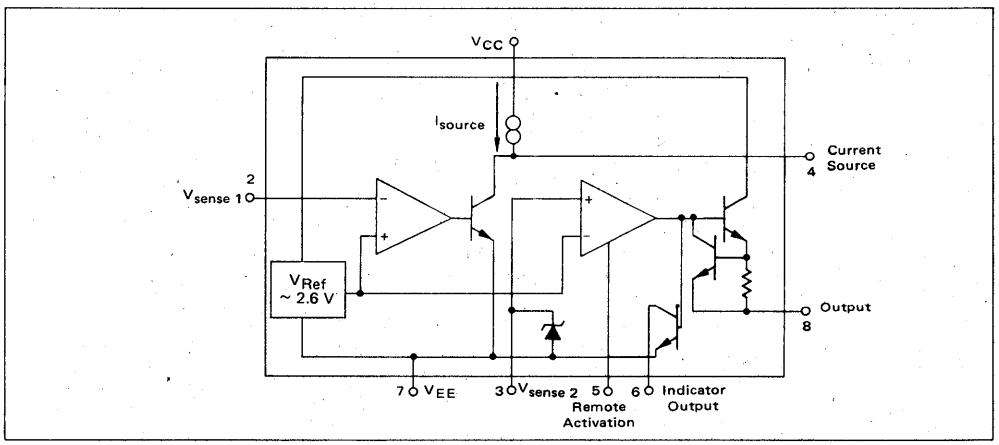
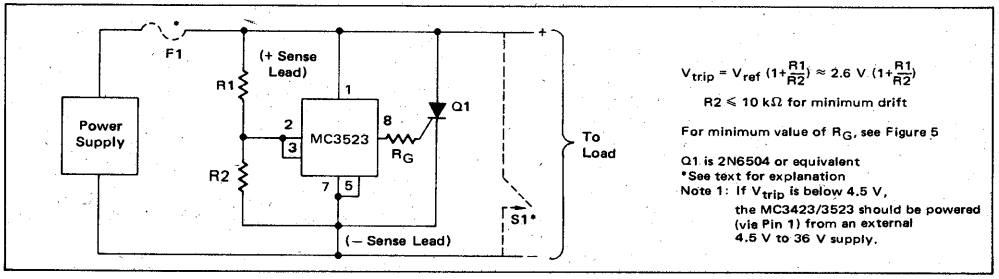


FIGURE 2A – BASIC CIRCUIT CONFIGURATION
for $V_{ref} \leq V_{trip} \leq 36$ V



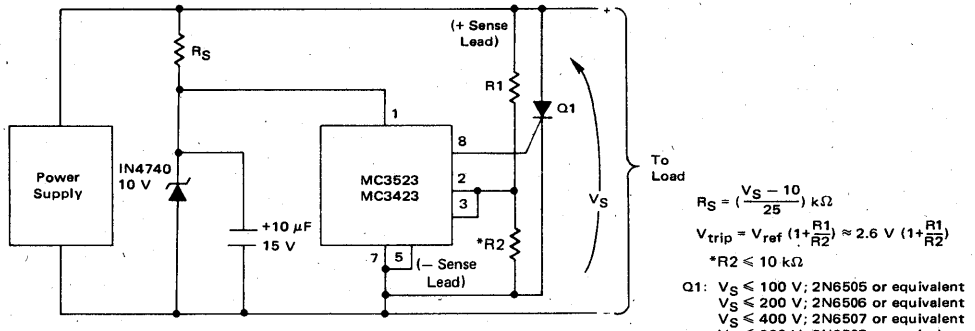
$V_{trip} = V_{ref}\left(1+\frac{R1}{R2}\right) \approx 2.6\ V\left(1+\frac{R1}{R2}\right)$

$R2 \leq 10\ k\Omega$ for minimum drift

For minimum value of R_G, see Figure 5

Q1 is 2N6504 or equivalent
*See text for explanation
Note 1: If V_{trip} is below 4.5 V, the MC3423/3523 should be powered (via Pin 1) from an external 4.5 V to 36 V supply.

FIGURE 2B – CIRCUIT CONFIGURATION FOR SUPPLY VOLTAGE ABOVE 36 V



APPLICATIONS INFORMATION

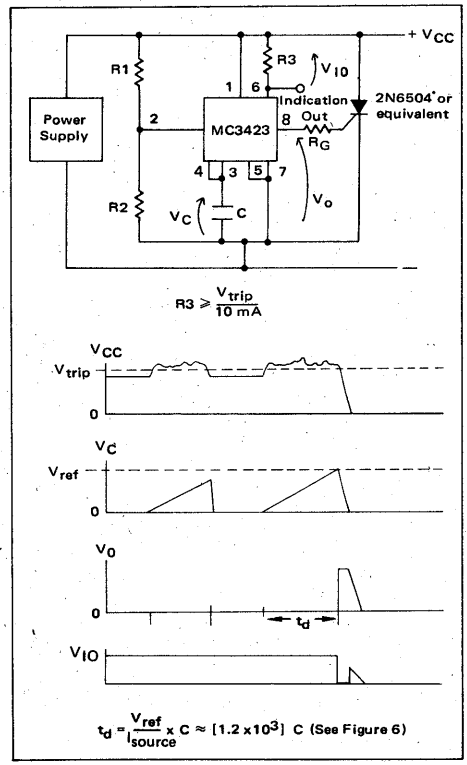
Basic Circuit Configuration

The basic circuit configuration of the MC3423/3523 OVP is shown in Figure 2A for trip voltages from 2.5 V to 36 V, and in Figure 2B for trip voltages above 36 V. In this circuit, the voltage sensing inputs of both internal amplifiers are tied together for sensing the overvoltage condition. The shortest possible propagation delay is obtained with this configuration. The threshold or trip voltage at which the MC3423/3523 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R1 and R2. Their values can be determined by the equation given in Figures 2A and 2B, or by the graph shown in Figure 4. The minimum value of the gate current limiting resistor, R_G, is given in Figure 5. Using this value of R_G, the SCR, Q1, will receive the greatest gate current possible without damaging the MC3423/3523. If lower output currents are required, R_G can be increased in value. The switch, S1, shown in Figure 2A may be used to reset the SCR crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current-limited supply is used, a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

Configuration for Programmable Minimum Duration of Overvoltage Condition Before Tripping

In many instances, the MC3423/3523 OVP will be used in a noise environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423/3523 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 3 is used. In this configuration, a capacitor is connected from Pin 3 to V_{EE}. The value of this capacitor determines the minimum duration of the overvoltage condition which is necessary to trip the OVP.

FIGURE 3 – BASIC CONFIGURATION FOR PROGRAMMABLE DURATION OF OVERVOLTAGE CONDITION BEFORE TRIP



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The value of C can be found from Figure 6. The circuit operates in the following manner: When V_{CC} rises above the trip point set by R1 and R2, an internal current source begins charging the capacitor, C, connected to Pin 3. If the overvoltage condition remains present long enough for the capacitor voltage, V_C, to reach V_{ref}, the output is activated. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate ≅ 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

Additional Features

1. Activation Indication Output

An additional output for use as an indicator of OVP activation is provided by the MC3423/3523. This output is an open collector transistor which saturates when the OVP is activated. It will remain in a saturated state until the SCR crowbar pulls the supply voltage, V_{CC}, below 4.5 V as in Figure 3. This output can be used to clock an edge triggered flip-flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heat-sinking requirements for the crowbar SCR.

2. Remote Activation Input

Another feature of the MC3423/3523 is its remote activation input, Pin 5. If the voltage on this CMOS/TTL compatible input is held below 0.7 V, the MC3423/3523 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present. This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the activation indication output of one MC3423/3523 can be used to activate another MC3423/3523 if a single transistor inverter is used to interface the former's indication output to the latter's remote activation input.

FIGURE 4 – R1 versus TRIP VOLTAGE

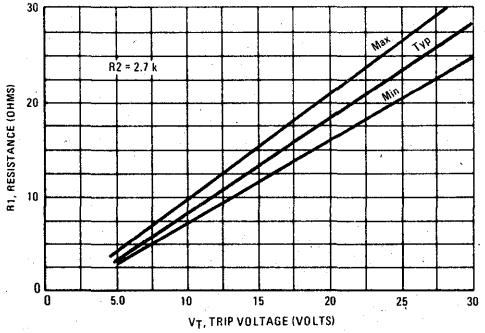


FIGURE 5 – MINIMUM R_G versus SUPPLY VOLTAGE

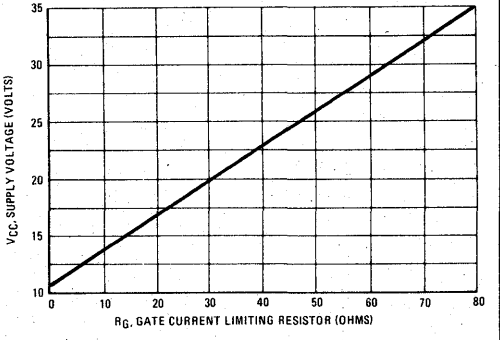
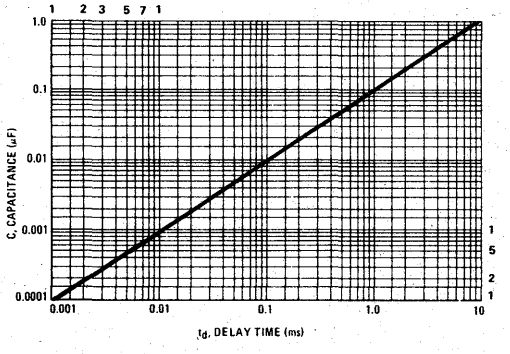


FIGURE 6 – CAPACITANCE versus MINIMUM OVERVOLTAGE DURATION



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MC3426

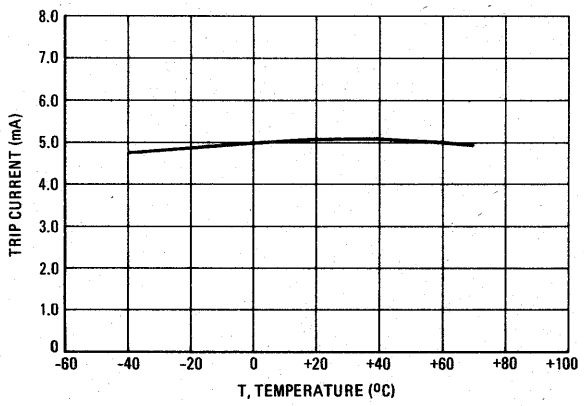
Advance Information

GROUND FAULT INTERRUPTER SUBSYSTEM (Latching)

The MC3426 is designed to provide ground fault and grounded neutral protection for 120 Vac, 15 and 20 ampere lines.

- Minimum number of external components
- Includes full wave bridge
- Designed for use with inexpensive ferrite cores or low permeability differential transfers
- Will operate properly if "hot" and neutral input wires are reversed
- Designed to be used in systems meeting UL943 specifications for Class A Ground Fault Circuit Interrupters
- Trips at a minimum leakage current of 5 mA ±1 mA over a temperature range of -40°C to +70°C and line voltage variations from 102 V to 132 V. Also trips for a neutral grounding resistance less than 2 Ω.
- Trip times are in accordance with UL curve
- High noise immunity and resistance to false tripping

FIGURE 1 – TYPICAL TRIP CURRENT THRESHOLD versus TEMPERATURE



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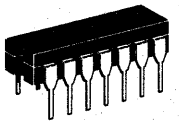
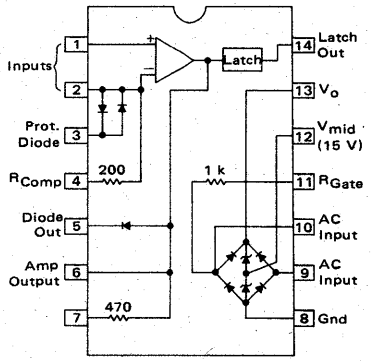
GROUND FAULT INTERRUPTER SUBSYSTEM

MONOLITHIC SILICON INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC3426L	-40 to +70°C	Ceramic DIP

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MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Current through pins 9 and 10 (T_A = 70°C)	I_{IN}	20	mA RMS
Thermal Resistance, Junction to Air	θ_{JA}	100	°C/W
Operating Ambient Temperature Range	T_A	-40 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Maximum Operating Junction Temperature	T_J	125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OPERATIONAL AMPLIFIER SECTION					
Input Offset Voltage	V_{IO}	–	3.0	–	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	15	–	μV/°C
Input Offset Current	I_{IO}	–	30	–	nA
Input Bias Current	I_{IB}	–	300	–	nA
Large Signal Open Loop Voltage Gain	A_{VOL+}	15	–	–	V/mV
Power Supply Current (V_O set to 25 V, Latch OFF, 2.7 MΩ from pin 2 to pin 5, Note 4)	I_D	–	1.4	2.25	mA
Power Supply Current (V_O Set to 25 V, Latch ON, pin 14 tied to pin 13, Note 6)	I_D (L_{on})	–	–	9.0	mA
Power Supply Rejection Ratio	PSRR±	60	–	–	dB
Output Quiescent Voltage of Operational Amplifier minus V_{mid} (2.7 MΩ from pin 2 to pin 5, Notes 2 and 5)	$V_6 - V_{mid}$	-2.0	–	1.0	V
REGULATOR/BRIDGE SECTION					
Power Supply Output Voltage (Note 1)	V_O	27.5	29.9	32.3	V
LATCH/TRIGGER SECTION					
Latch Trigger Voltage (Notes 2 and 7)	V_6 (L_{on}) -V_{mid}	6.7	7.4	8.1	V
Latch Trigger Current (Note 8)	I_I(L_{on})	–	50	–	μA
Output Drive Current @ V14 = 1.0 V (T_A = -40°C, Note 3)	I_{14} (L_{on})	0.5	–	–	mA
Output Drive Voltage with Latch Off (Note 9)	V_{14} (L_{off})	–	–	0.05	V
Power Supply Voltage to Turn Off Latch (Note 10)	V_O (L_{off})	0.2	2.0	3.0	V

DEFINITION OF TERMS

Note:

1. POWER SUPPLY OUTPUT VOLTAGE – V_O

This is the voltage between pins 13 and 8 that is set up by the zener string with the latch turned off and a current of 17 mAdc (approximately the maximum peak current from the ac line with a 10 kΩ 5% dropping resistor) is flowing between the pins.

2. MIDPOINT VOLTAGE – V_{mid}

This is the voltage at the midpoint of the zener string–between pins 12 and 8–with 17 mAdc flowing and the latch turned off.

3. OUTPUT DRIVE CURRENT – $I_{14}(L_{on})$

This is the current sourced from pin 14 with the latch on and the gate resistor (R_{Gate}, 1 kΩ) connected (pin 11 shorted to pin 14).

4. POWER SUPPLY CURRENT, LATCH OFF – I_D

This is the power supply drain current of the operational amplifier section with the latch turned off, a 2.7 MΩ resistor between pins 2 and 5, and V_O set to 25

V so that no current goes through the zener string. I_D max assures proper quiescent operation of the operational amplifier.

5. OUTPUT QUIESCENT VOLTAGE – V_6

This is the quiescent output voltage of the operational amplifier with a 2.7 MΩ resistor between pins 2 and 5. The $V_6 - V_{mid}$ specification assures proper trip threshold with specified V_{IO} and I_{IB}.

6. POWER SUPPLY CURRENT, LATCH ON – $I_D(L_{on})$

This is the power supply drain current of the operational amplifier section and the latch section with the latch turned on, V_O set to 25 V, pin 14 tied to pin 13, R_{Gate} not connected, and the ac line polarity such that the SCR cannot fire. $I_D(L_{on})$ max assures the latch remaining latched before the SCR fires.

7. LATCH TRIGGER VOLTAGE – $V_6(L_{on})$

This is the threshold voltage between pins 6 and 8 at which the latch turns on and pin 14 begins sourcing current.

8. LATCH TRIGGER CURRENT – $I_I(L_{on})$

This is the threshold current through resistor R11 (5 kΩ) at which the latch turns on and pin 14 begins sourcing current.

9. OUTPUT DRIVE VOLTAGE, LATCH OFF – $V_{14}(L_{off})$

This is the voltage between pins 14 and 10 with the latch off, R_{Gate} connected (pin 11 shorted to pin 14), and 17 mAdc flowing between pins 9 and 10. $V_{14}(L_{off})$ max assures that the SCR will not be turned on when the latch is off.

10. POWER SUPPLY VOLTAGE TO TURN OFF LATCH – $V_O(L_{off})$

This is the voltage to which pin 13 must be dropped after the latch has been turned on to turn the latch off and cause pin 14 to stop sourcing current.

CIRCUIT SCHEMATIC

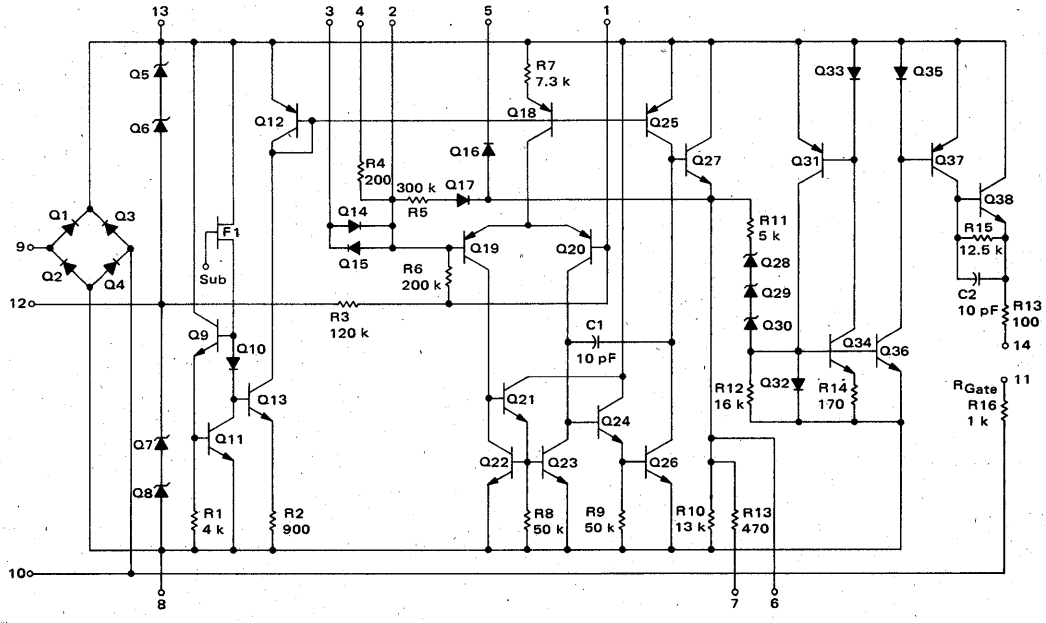
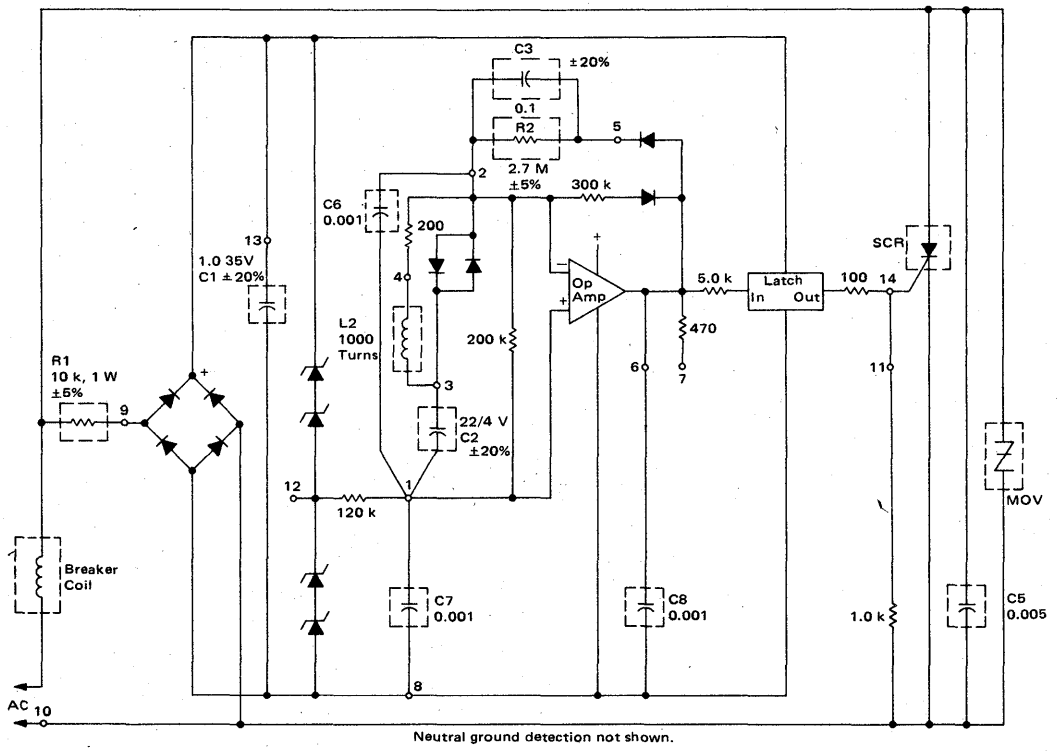


FIGURE 2 – BLOCK DIAGRAM
(External Components within dotted lines)



CIRCUIT OPERATION

Circuit operation is best understood by referring to the complete block diagram in Figure 2.

Power Supply

The circuit is powered from the ac line through the breaker coil and R1 (an external 10 k ohm dropping resistor) to pins 9 and 10, which are connected to the internal full wave bridge rectifier. Four on-chip zeners clamp the dc output voltage between pins 13 and 8 to about 30 V, and an external capacitor (C1) filters this voltage. During normal quiescent operation less than 10 mA is drawn through the breaker coil, which is not enough to energize it.

Operational Amplifier Biasing

The operational amplifier has two feedback paths, depending on whether its output is more positive or more negative than its inputs. The dc gain is relatively small, less than 15 when the output swings up and about 1.5 when the output swings down. The non-inverting input to the op amp is tied to the midpoint of the zener string through a 120 k ohm resistor, and therefore the

quiescent output voltage of the op amp is approximately that voltage, about 15 volts. A 200 k ohm internal resistor between the inputs provides a path for bias current from the inverting input terminal and helps set the dc feedback. It also provides a discharge path for C2 after high level faults to make reset quicker.

Fault Sensing and Breaker Tripping

If a ground fault occurs, the imbalance of current in the two ac primary wires of L2 will generate a signal in the secondary. This signal is ac coupled through an external 22 μF capacitor (C2) to the inputs of the op amp. An external 0.1 μF capacitor (C3) acts as an integrating capacitor; it charges up slightly more each time that the signal causes the op amp to swing positive (i.e., every other half cycle of the ac line). When the signal polarity reverses and the op amp swings down, the only discharge path for C3 is through the external set resistor (R2). With a 5 mA ground fault it takes about 2 seconds for C3 to integrate up so that the positive swings of the op amp become larger and larger until they reach a "steady state" value of about 7 V above the quiescent output voltage of the op amp and increase no further. This is just the threshold voltage of the latch, which turns it on and causes pin 14 to be pulled toward the positive supply voltage and turns on the SCR. When the SCR is turned on, enough current is drawn through the breaker coil to energize it and cause the breaker to disconnect power from the load side of the ac line. (The breaker is a mechanically latching type and it must be mechanically reset to reapply power to the load side of the ac line.)

The purpose of the feedback on negative swings of the output of the op amp is to equalize positive and negative swings so that coupling capacitor C2 does not charge up and drive the output one way or the other.

If the line side black and white wires to the GFI system are reversed such that the black is now the neutral and the white is now the hot wire, the result is that the signal at the output of the op amp is not the correct phase to fire the SCR since the SCR is a half-wave device connected across the line. However, the latch takes care of this problem by turning on and staying on until the SCR can fire during the next half-cycle of the ac line.

High Faults

The purpose of the 120 k ohm internal resistor between pins 12 and 1 is to reduce the trip time at higher fault currents. As the fault current increases, the voltage drop across this resistor increases and since the output of the op amp follows the voltage at the non-inverting input this means that C3 will integrate less and therefore the trip time will be faster.

The on-chip protection diodes across the sense coil serve two purposes, but only during extremely high fault currents. First, they prevent C2 from charging to a large voltage during this condition which would make the reset or the return to quiescent operation slow. Second, they prevent excessive voltage from "zenering" or otherwise damaging junctions on the circuit.

Use of Ferrites or Low-Permeability Torroids

The sense coil in this circuit is looking into a relatively low impedance (i.e., the impedance between the two inputs to the op amp), which is the feedback resistance divided by the open loop gain of the op amp (an impedance of a few hundred ohms) in series with a 22 μF capacitor and a 200 ohm resistor. As long as this loading resistance is low compared to the secondary reactance of the torroid, the transformer acts as a current transformer and the output remains constant with changes in core permeability. Therefore, ferrite cores or other low permeability cores may be used as long as these conditions are met. The purpose of the 200 ohm on-chip resistor is to counteract the tendency for the circuit to become more sensitive at low temperatures with ferrite cores due to the reduction in secondary inductance with the reduction in core permeability.

Noise, DV/DT, and Transient Protection

External 0.001 μF capacitors C6, C7, and C8 have been added to increase the circuit's resistance to false tripping due to noise spikes. The internal 1 k ohm resistor from gate to anode and the external 0.005 μF capacitor C5 from anode to cathode of the SCR reduce the SCR's sensitivity to DV/DT turn on. The purpose of the MOV (metal oxide varistor) is to absorb energy from very high voltage line transients to prevent damage to the IC or SCR.

Latching Characteristics (Auxiliary Switch Requirements)

Note that this device requires a third pole or auxiliary contact on the breaker when used in a wall socket application. This is because the latch remains latched when the circuit is tripped and would continue to energize the breaker coil. Note also that a single contact breaker may be used in circuit breaker applications when line side "hot" and when neutral wires cannot be reversed.

Grounded Neutral Detection Methods

Figures 3 and 4 are schematics for wall socket applications showing the different methods of grounded neutral detection.

Figure 3 is the 60 Hz method; the high-μ core is connected across the line and acts as a 60 Hz source for both black and white wires. If the neutral is grounded (load white essentially connected to line white, or if line wires are reversed and load black essentially connected to line black) this 60 Hz signal is coupled to the 1000 turn sense coil and the circuit trips just as it does with a ground fault.

Figure 4 is the external oscillator method of grounded neutral detection. A 2 to 4 kHz signal is fed into the left ferrite coil and this signal is sourced for both the black and white wires. If the neutral is grounded this signal is coupled to the 1000 turn sense coil and the circuit trips just as with the previous method except that the signal is now the 2 to 4 kHz supplied by the external oscillator.

FIGURE 3 – GROUNDED NEUTRAL DETECTION USING A 60 Hz TRANSFORMER

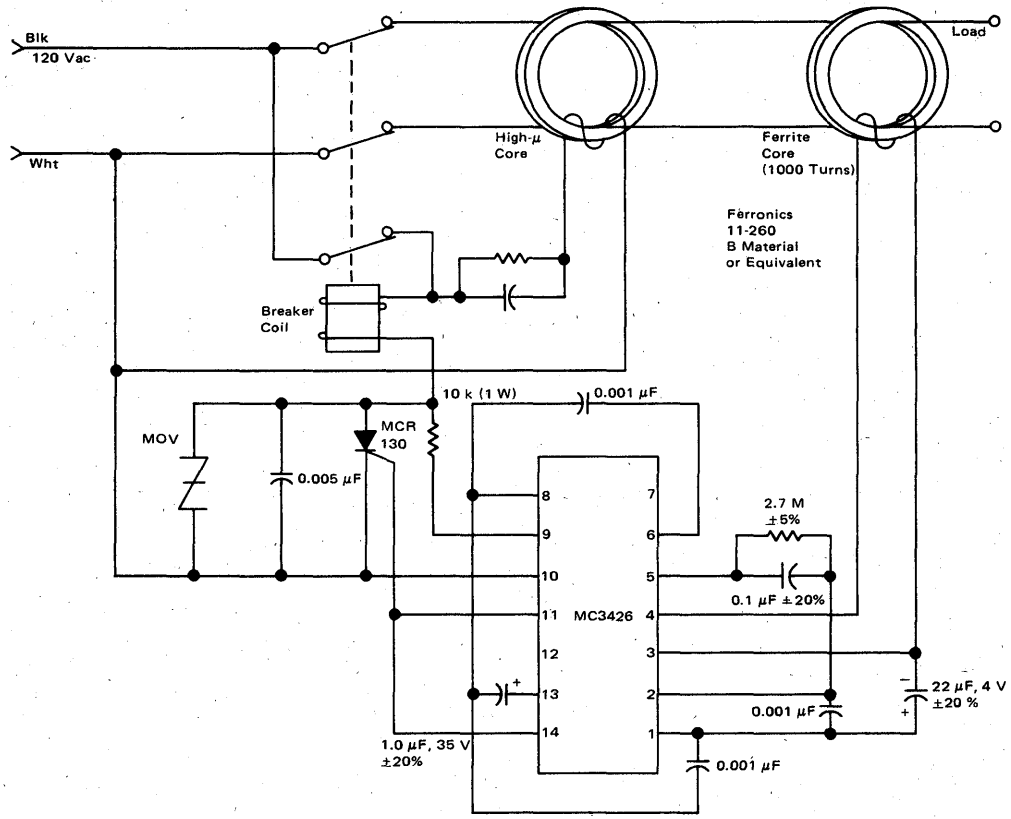


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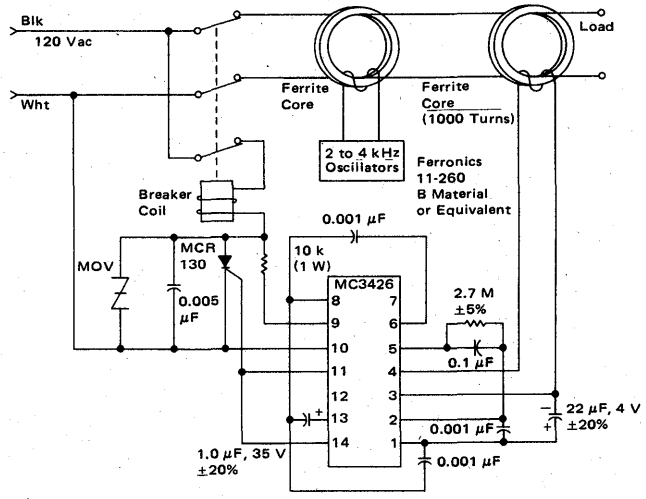
FIGURE 4 – GROUNDED NEUTRAL DETECTION USING AN EXTERNAL OSCILLATOR



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\,(Typ)}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst-case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}(Typ)$ = Typical Thermal Resistance Junction to Ambient

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ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC3456L	—	0°C to +70°C	Ceramic DIP
MC3456P	NE556A	0°C to +70°C	Plastic DIP
MC3556L	—	−55°C to +125°C	Ceramic DIP

MC3456
MC3556

Specifications and Applications Information

DUAL TIMING CIRCUIT

The MC3556/MC3456 dual timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor per timer. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor per timer. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE556/SE556 Timers
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output
- Dual Version of the Popular MC1555/MC1455 Timer

FIGURE 1 – 22-SECOND SOLID-STATE TIME DELAY RELAY CIRCUIT

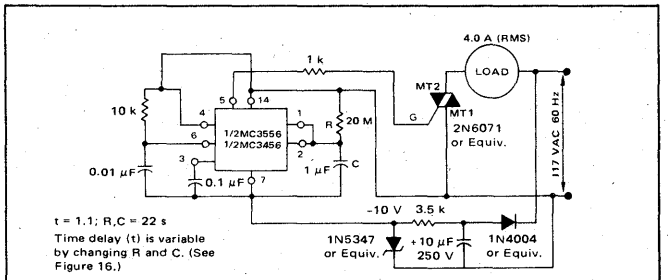
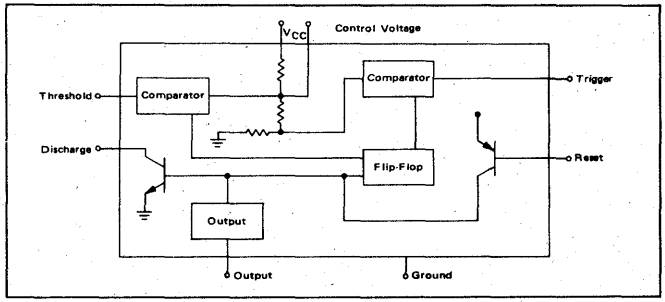
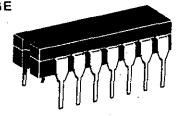


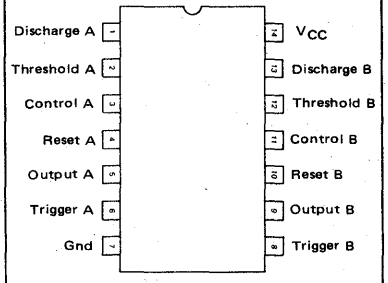
FIGURE 2 – BLOCK DIAGRAM (1/2 SHOWN)



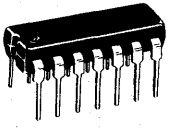
DUAL
TIMING CIRCUIT
SILICON MONOLITHIC
INTEGRATED CIRCUIT

L SUFFIX
CERAMIC PACKAGE
CASE 632-02
TO-116





P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC3456 only)



TYPICAL APPLICATIONS

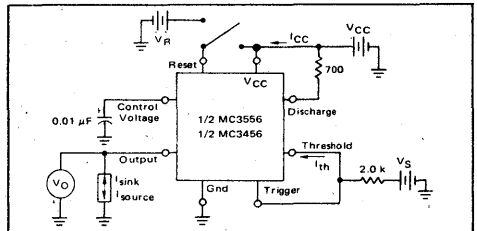
- Time Delay Generation
- Sequential Timing
- Linear Sweep Generation
- Precision Timing
- Pulse Generation
- Pulse Shaping
- Missing Pulse Detection
- Pulse Width Modulation
- Pulse Position Modulation

8

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current	I_{dis}	200	mA
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual-In-Line Package		1000	mW
Derate above T_A = +25°C		6.6	mW/°C
Plastic Dual In-Line Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
Operating Ambient Temperature Range MC3556	T_A	-55 to +125	°C
MC3456		0 to +70	
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 3 – GENERAL TEST CIRCUIT



Test Circuit for Measuring dc Parameters:
(to set output and measure parameters)
a. When $V_S \geq 2/3\ V_{CC}$, V_O is low.
b. When $V_S \leq 1/3\ V_{CC}$, V_O is high.
c. When V_O is low, pin 7 sinks current. To test for Reset, set V_O high, apply Reset voltage, and test for current flowing into discharge pin. When Reset is not in use, it should be tied to V_{CC}.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +15 V unless otherwise noted.)

Characteristics	Symbol	MC3556 Min	MC3556 Typ	MC3556 Max	MC3456 Min	MC3456 Typ	MC3456 Max	Unit
Supply Voltage	V_{CC}	4.5	–	18	4.5	–	16	V
Supply Current (Per timer, double for both halfs)	I_{CC}							mA
V_{CC} = 5.0 V, R_L = ∞		–	3.0	5.0	–	3.0	6.0	
V_{CC} = 15 V, R_L = ∞		–	10	11	–	10	14	
Low State, (Note 1)								
Timing Error (Note 2)								
Monostable Mode								
R_A = 2.0 kΩ to 100 kΩ								
Initial Accuracy C = 0.1 μF		–	0.5	1.5	–	0.75	–	%
Drift with Temperature		–	30	100	–	50	–	PPM/°C
Drift with Supply Voltage		–	0.15	0.2	–	0.1	–	%/Volt
Astable Mode								
R_A = R_B = 2.0 kΩ to 100 kΩ								
C = 0.01 μF								
Initial Accuracy		–	1.5	–	–	2.25	–	%
Drift with Temperature		–	90	–	–	150	–	PPM/°C
Drift with Supply Voltage		–	0.15	–	–	0.3	–	%/Volt
Threshold Voltage	V_{th}	–	2/3	–	–	2/3	–	xV_{CC}
Trigger Voltage	V_T							V
V_{CC} = 15 V		4.8	5.0	5.2	–	5.0	–	
V_{CC} = 5.0 V		1.45	1.67	1.9	–	1.67	–	
Trigger Current	I_T	–	0.5	–	–	0.5	–	μA
Reset Voltage	V_R	0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current	I_R	–	0.1	–	–	0.1	–	mA
Threshold Current (Note 3)	I_{th}	–	0.03	0.1	–	0.03	0.1	μA
Control Voltage Level	V_{CL}							V
V_{CC} = 15 V		9.6	10	10.4	9.0	10	11	
V_{CC} = 5.0 V		2.9	3.33	3.8	2.6	3.33	4.0	
Output Voltage Low	V_{OL}							V
(V_{CC} = 15 V)								
I_{sink} = 10 mA		–	0.1	0.15	–	0.1	0.25	
I_{sink} = 50 mA		–	0.4	0.5	–	0.4	0.75	
I_{sink} = 100 mA		–	2.0	2.25	–	2.0	2.75	
I_{sink} = 200 mA		–	2.5	–	–	2.5	–	
(V_{CC} = 5.0 V)								
I_{sink} = 8.0 mA		–	0.1	0.25	–	–	–	
I_{sink} = 5.0 mA		–	–	–	–	0.25	0.35	
Output Voltage High	V_{OH}							V
(I_{source} = 200 mA)								
V_{CC} = 15 V		–	12.5	–	–	12.5	–	
(I_{source} = 100 mA)								
V_{CC} = 15 V		13	13.3	–	12.75	13.3	–	
V_{CC} = 5.0 V		3.0	3.3	–	2.75	3.3	–	
Toggle Rate (Figures 17, 19)								
R_A = 3.3 kΩ, R_B = 6.8 kΩ, C = 0.003 μF	–	–	100	–	–	100	–	kHz
Discharge Leakage Current	I_{dis}	–	20	100	–	20	100	nA
Rise Time of Output	t_{OLH}	–	100	–	–	100	–	ns
Fall Time of Output	t_{OHL}	–	100	–	–	100	–	ns
Matching Characteristics Between Sections (Monostable)								
Initial Timing Accuracy		–	0.05	0.1	–	0.1	0.2	%
Timing Drift with Temperature		–	±10	–	–	±10	–	ppm/°C
Drift with Supply Voltage		–	0.1	0.2	–	0.2	0.5	%/V

NOTES: 1. Supply current when output is high is typically 2.0 mA less.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 megohms.

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TYPICAL CHARACTERISTICS
(T_A = +25°C unless otherwise noted.)

FIGURE 4 – TRIGGER PULSE WIDTH

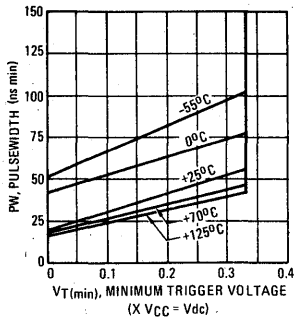


FIGURE 5 – SUPPLY CURRENT

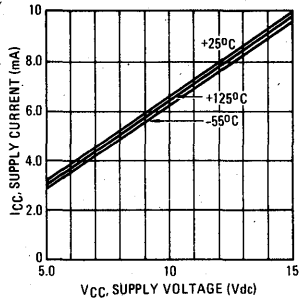


FIGURE 6 – HIGH OUTPUT VOLTAGE

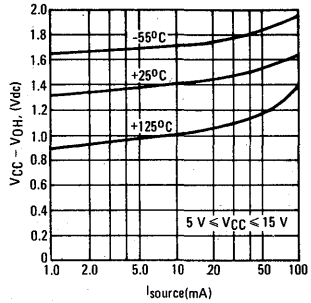


FIGURE 7 – LOW OUTPUT VOLTAGE @ V_{CC} = 5.0 Vdc

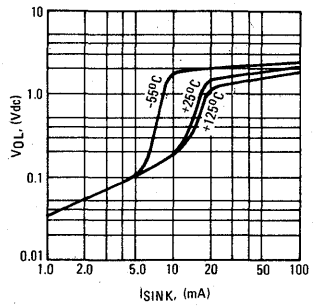


FIGURE 8 – LOW OUTPUT VOLTAGE @ V_{CC} = 10 Vdc

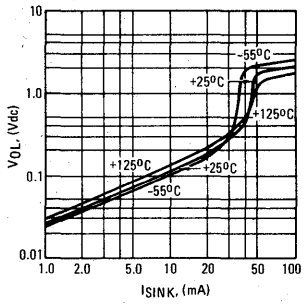


FIGURE 9 – LOW OUTPUT VOLTAGE @ V_{CC} = 15 Vdc

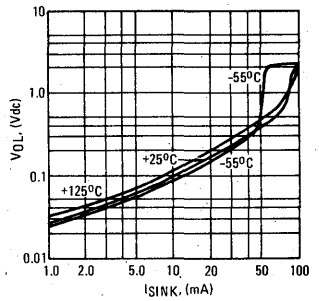


FIGURE 10 – DELAY TIME versus SUPPLY VOLTAGE

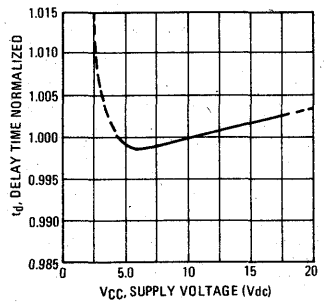


FIGURE 11 – DELAY TIME versus TEMPERATURE

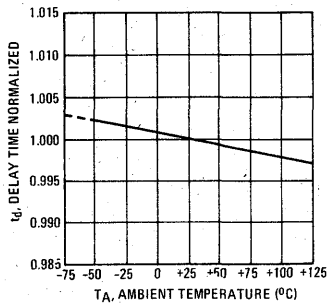
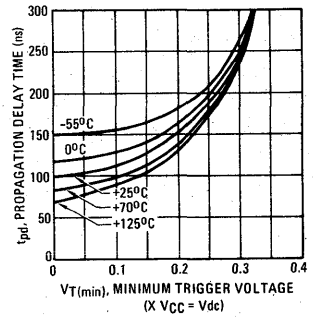


FIGURE 12 – PROPAGATION DELAY versus TRIGGER VOLTAGE



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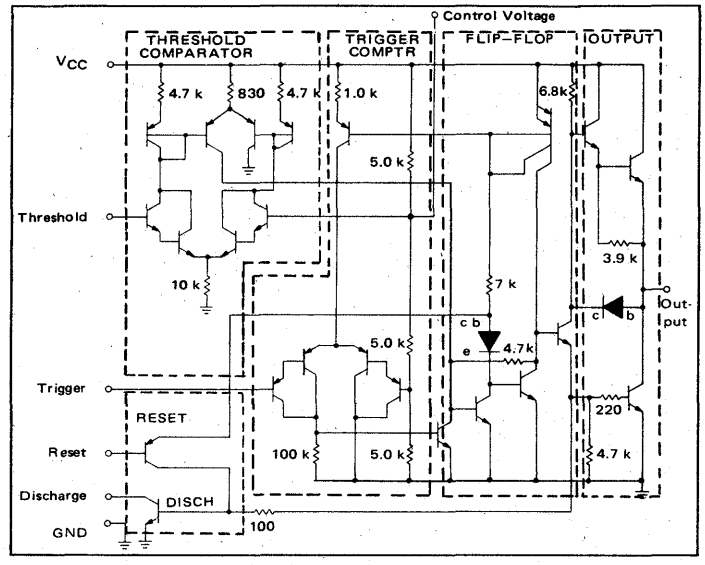


FIGURE 13 – 1/2 REPRESENTATIVE CIRCUIT SCHEMATIC

GENERAL OPERATION

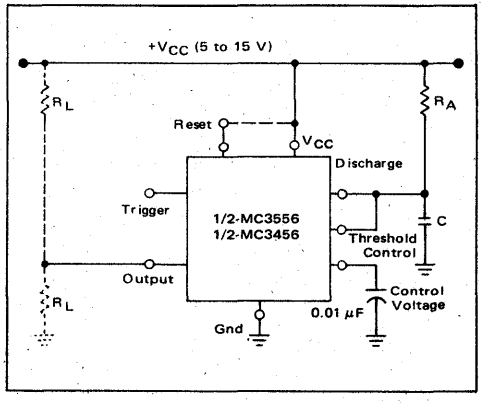
The MC3556 is a dual timing circuit which uses as its timing elements an external resistor – capacitor network. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below 1/3 V_{CC} the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V_{CC} the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

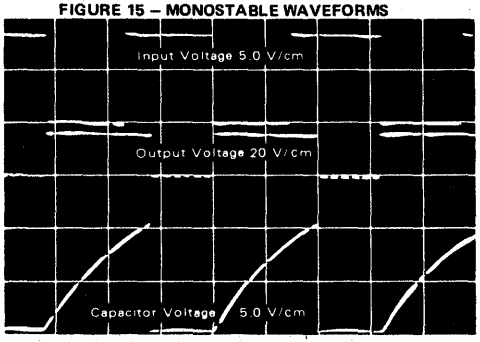
FIGURE 14 – MONOSTABLE CIRCUIT



8

GENERAL OPERATION (continued)

FIGURE 15 – MONOSTABLE WAVEFORMS



t = 50 μs/cm
(R_A = 10 kΩ, C = 0.01 μF, R_L = 1.0 kΩ, V_{CC} = 15 V)

FIGURE 16 – TIME DELAY

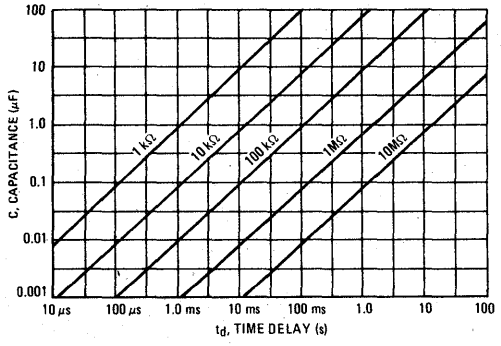


FIGURE 17 – ASTABLE CIRCUIT

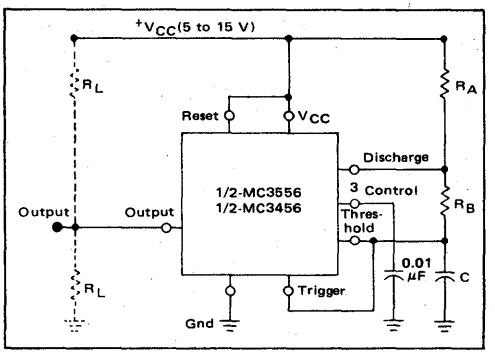
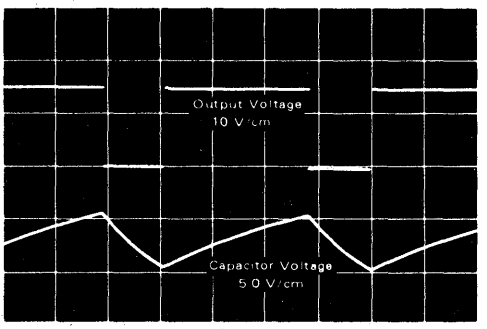


FIGURE 18 – ASTABLE WAVEFORMS



t = 20 μs/cm
(R_A = 5.1 kΩ, C = 0.01 μF, R_L = 1.0 kΩ;
R_B = 3.9 kΩ, V_{CC} = 15 V)

Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 V_{CC} and 2/3 V_{CC}. See Figure 17.

The external capacitor charges to 2/3 V_{CC} through R_A and R_B and discharges to 1/3 V_{CC} through R_B. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by: $t_1 = 0.695 (R_A+R_B) C$

The discharge time (output low) by: $t_2 = 0.695 (R_B) C$

Thus the total period is given by: $T = t_1 + t_2 = 0.695 (R_A+2R_B) C$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A+2R_B) C}$

and may be easily found as shown in Figure 19.

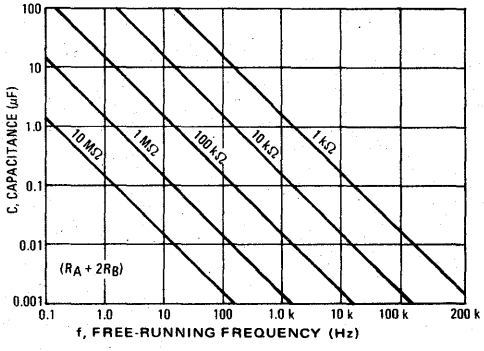
The duty cycle is given by: $DC = \frac{R_B}{R_A+2R_B}$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geq \frac{V_{CC}\ (Vdc)}{I_7\ (A)} \geq \frac{V_{CC}\ (Vdc)}{0.2}$$

FIGURE 19 – FREE-RUNNING FREQUENCY



8

APPLICATIONS INFORMATION

TONE BURST GENERATOR

For a tone burst generator the first timer is used as a monostable and determines the tone duration when triggered by a positive pulse at Pin 6. The second timer is enabled by the high output of the monostable. It is connected as an astable and determines the frequency of the tone.

DUAL ASTABLE MULTIVIBRATOR

This dual astable multivibrator provides versatility not available with single timer circuits. The duty cycle can be adjusted from 5% to 95%. The two outputs provide two phase clock signals often required in digital systems. It can also be inhibited by use of either reset terminal.

FIGURE 20 – TONE BURST GENERATOR

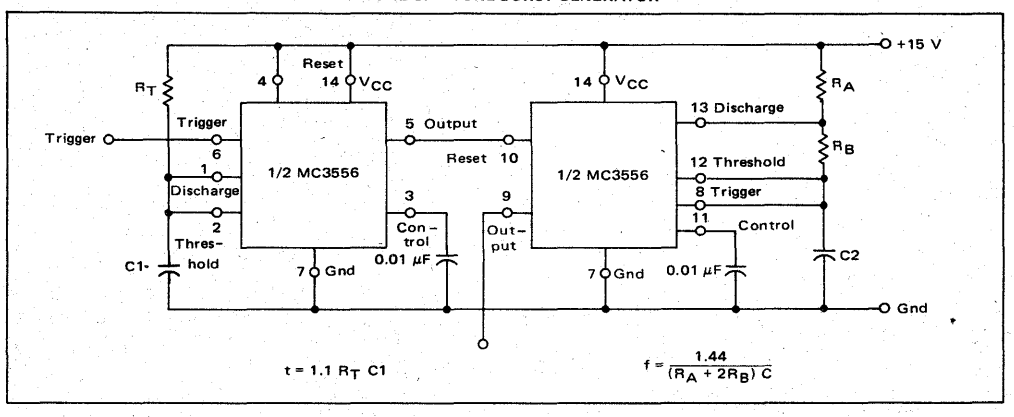
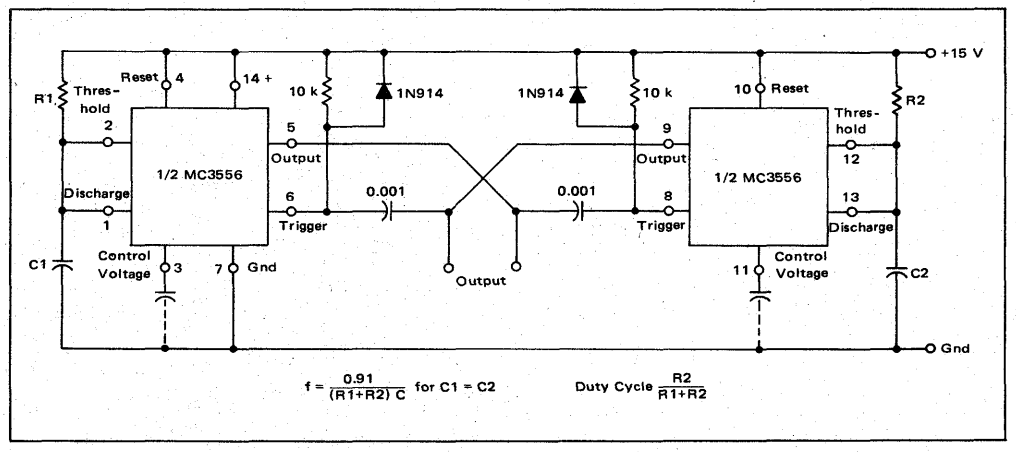


FIGURE 21 – DUAL ASTABLE MULTIVIBRATOR



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APPLICATIONS INFORMATION (continued)

Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at pin 3. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

FIGURE 22

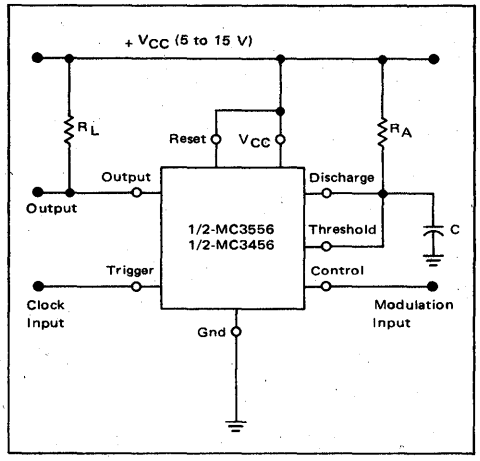
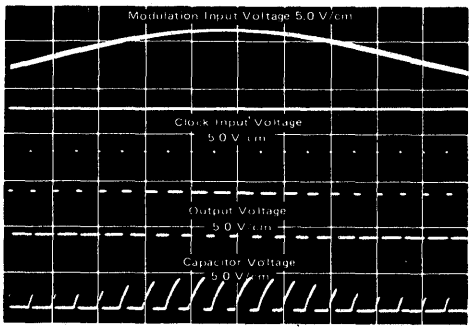


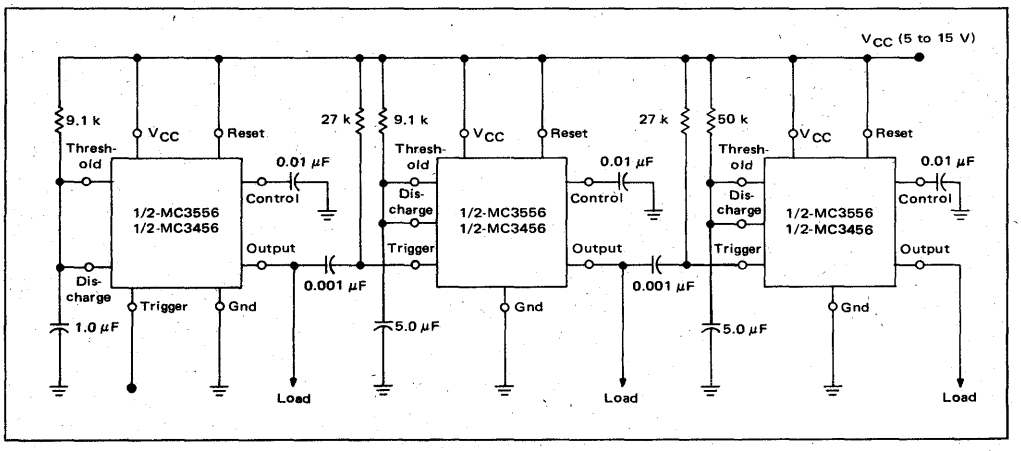
FIGURE 23 – PULSE WIDTH MODULATION WAVEFORMS
(R_A = 10 kΩ, C = 0.02 μF, V_{CC} = 15 V)



Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 24 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

FIGURE 24



ORDERING INFORMATION

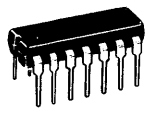
Device	Alternate	Temperature Range	Package
MLM565CP	NE565A	0°C to +70°C	Plastic DIP

MLM565C

PHASE-LOCKED LOOP
SILICON MONOLITHIC
INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE

CASE 646



PHASE-LOCKED LOOP

The MLM565C is designed for general-purpose phase-locked loop applications to 500 kHz.

- Stable Center Frequency – 200 ppm/°C (Typ)
- Flexible Power Supply Range – ±5 to ±12 Volts with Small Frequency Drift – 100 ppm/% (Typ)
- Low Total Harmonic Distortion of Demodulator Output – 1.5% (Max)
- Linear Triangle Wave Output – 0.5% (Typ)
- TTL, DTL Compatible Inputs and Outputs
- Adjustable Hold In Range – ±1% to >±60%.

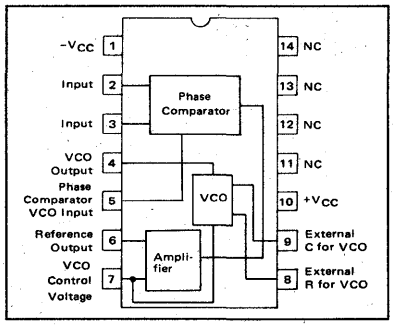
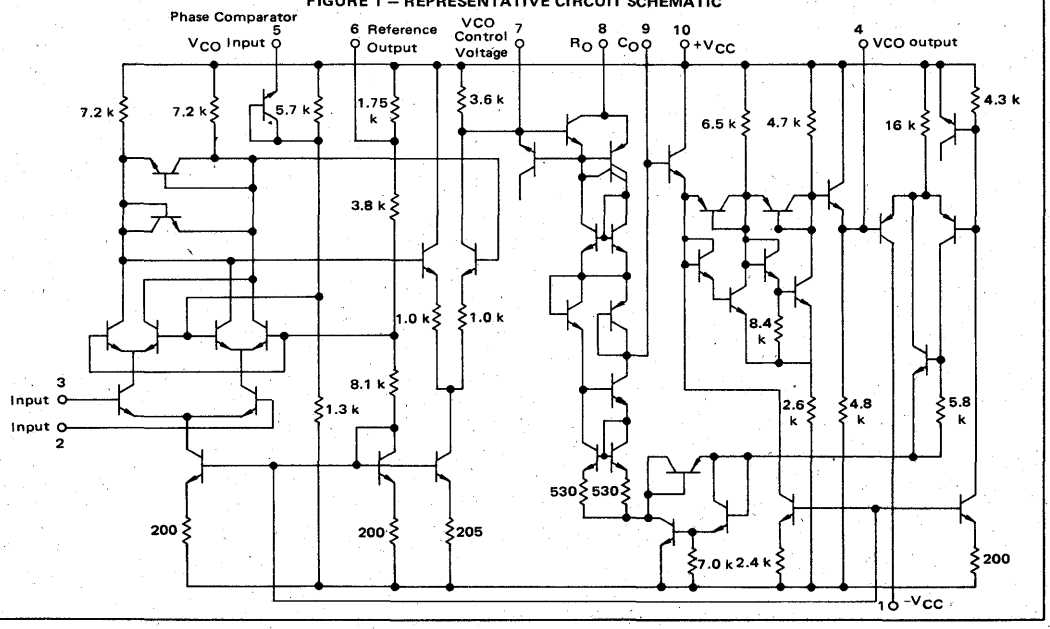


FIGURE 1 – REPRESENTATIVE CIRCUIT SCHEMATIC



8

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	±12	Vdc
Power Dissipation (Package Limitation) Derate above 25°C	P_D	825 6.6	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Test Circuit Figure 2, T_A = 25°C, V_{CC} = ±6.0 Vdc unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Power Supply Current	–	8.0	12.5	mA
Input Impedance (Pins 2, 3) -4.0 V < V2, V3 < 0 V	–	5.0	–	kΩ
Input Level Required for Tracking f_o = 10 kHz, ±10% Frequency Deviation	10	–	–	mVrms
VCO Maximum Operating Frequency C_o = 2.7 pF	–	500	–	kHz
Operating Frequency Temperature Coefficient	–	200	–	ppm/°C
Frequency Drift with Supply Voltage	–	200	–	ppm/%
Triangle Wave Ouptut Voltage	2.0	2.4	3.0	Vp-p
Triangle Wave Output Linearity	–	0.5	–	%
Square Wave Output Level	4.7	5.4	–	Vp-p
VCO Output Impedance (Pin 4)	–	5.0	–	kΩ
Square Wave Duty Cycle	40	50	60	%
Square Wave Rise Time	–	20	–	ns
Square Wave Fall Time	–	50	–	ns
Output Current Sink (Pin 4)	0.6	1.0	–	mA
VCO Sensitivity	–	6600	–	Hz/V
Demodulated Output Voltage (Pin 7) f_o = 10 kHz, ±10% Frequency Deviation	200	300	–	mVp-p
Total Harmonic Distortion f_o = 10 kHz, ±10% Frequency Deviation	–	0.2	1.5	%
Output Impedance (Pin 7)	–	3.5	–	kΩ
DC Output Voltage Level (Pin 7)	4.0	4.5	5.0	V
Output Offset Voltage (Input = 0) /V7-V6/	–	50	200	mV
Temperature Drift of /V7-V6/	–	500	–	μV/°C
AM Rejection	–	40	–	dB
Phase Detector Sensitivity K_D	–	0.68	–	V/radian

FIGURE 2 – TEST CIRCUIT SCHEMATIC

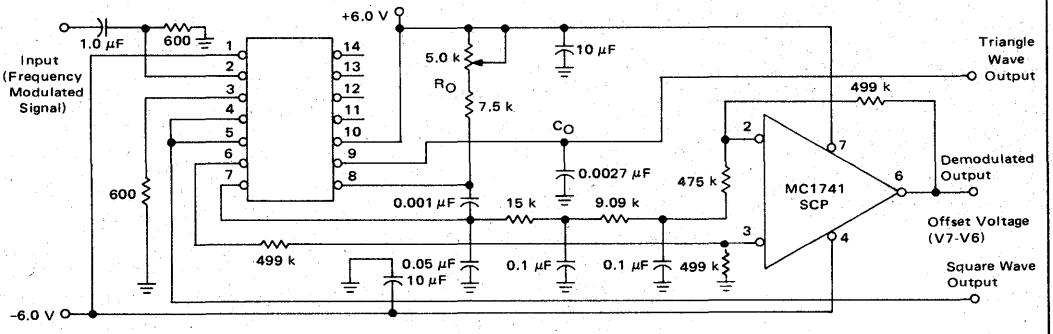


FIGURE 3 – POWER SUPPLY CHARACTERISTICS

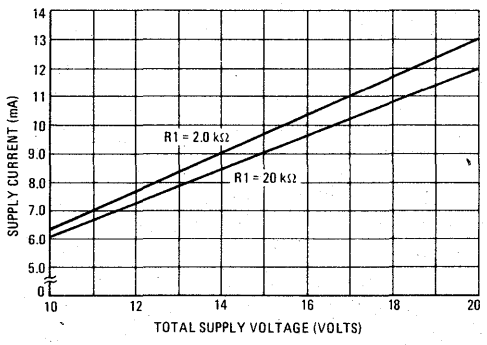


FIGURE 4 – VCO CONVERSION GAIN

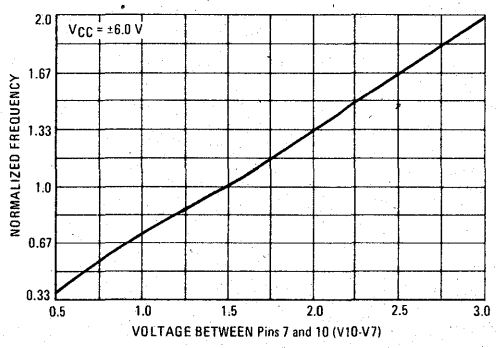


FIGURE 5 – LOCK RANGE versus INPUT VOLTAGE

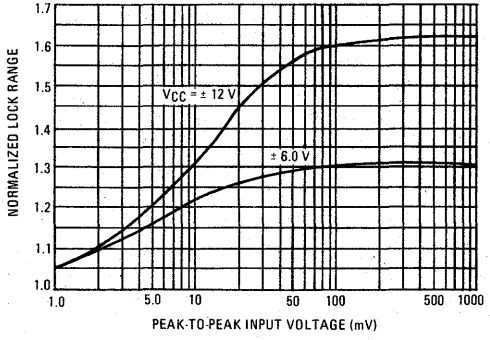


FIGURE 6 – OSCILLATOR OUTPUT WAVEFORMS

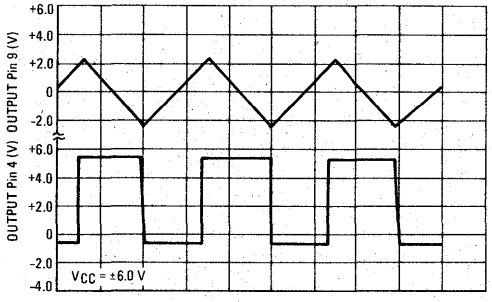


FIGURE 7 – LOCK RANGE
(As a Function of Gain Setting Resistance)

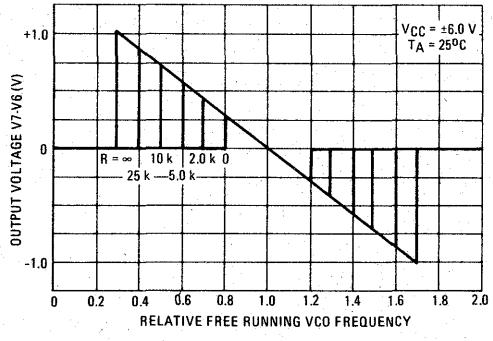
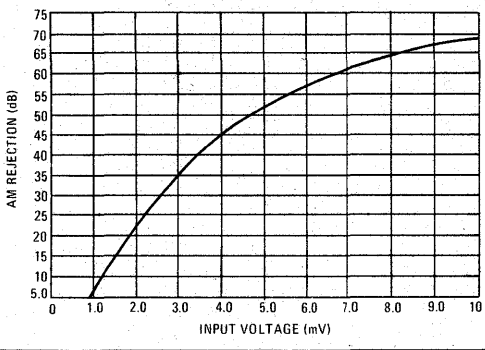


FIGURE 8 – AM REJECTION CHARACTERISTICS



GENERAL APPLICATIONS INFORMATION

The following formulas are useful when designing with the MLM565C:

1. Center Frequency – $f_o \approx \frac{1}{3.7\, R_O C_O}$

   Where: f_o is the frequency of the VCO without input signal. For R_O, C_O circuit location see Figure 2.

2. Loop Gain – $K_O K_D A$

   Definitions:

   K_O – VCO Conversion Gain – the conversion factor between VCO frequency and control voltage.

   $K_O = 4.12\, f_o$ (units are in radians/sec/volt)

   Example: for VCO Sensitivity @ 10 kHz (in Hz/volt)

   $$K_O = \frac{4.12 \times 10^4}{2\pi \text{ radians}} = 6600 \text{ Hz/Volt}$$

   K_D – Phase Detector Gain Factor – the conversion factor between the phase detector output voltage and the phase difference between input and VCO signals. Units are in volts/radian.

   $$K_D = \frac{8.1 \bullet A}{V_{CC}}$$

   Where: A = f(R6 to R7)

   Hence: $K_D = \frac{8.1}{V_{CC}}$ [f(R6-R7)]

   Where: V_{CC} is total system supply voltage, f(R6-R7) is internal amplifier gain (See Figure 9). V_{CC} - total supply voltage to the circuit.

3. Lock Range – $f_L = \pm \frac{8 f_o}{V_{CC}}$

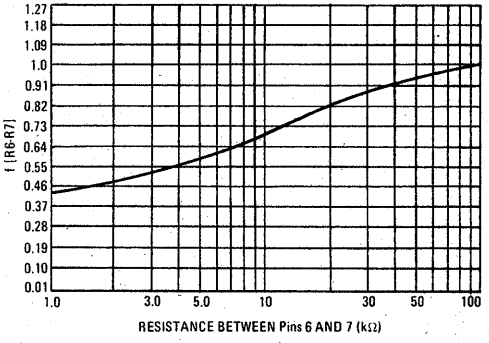
   Where: f_L is the range of frequencies in the area of f_o over which the VCO, once locked to the input signal, will remain locked.

4. Capture Range – $f_c \approx \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$

   Where: f_c is that range of frequencies around f_o over which the loop will acquire lock with an input signal initially starting out of lock.

   (τ = Time Constant at Pin 7)

FIGURE 9 – INTERNAL AMPLIFIER GAIN CHARACTERISTICS



8

NE592
SE592

Advance Information

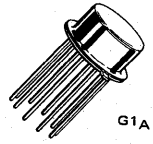
VIDEO AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

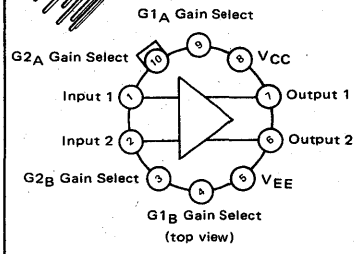
DIFFERENTIAL TWO-STAGE VIDEO AMPLIFIER

The SE/NE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed to that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems. The 592 is a pin-for-pin replacement for the MC1733.

- 120 MHz Bandwidth
- Adjustable Gains From 0 to 400
- Adjustable Pass Band
- No Frequency Compensation Required

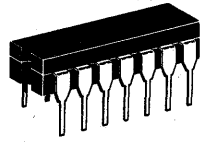


G SUFFIX
METAL PACKAGE
CASE 603

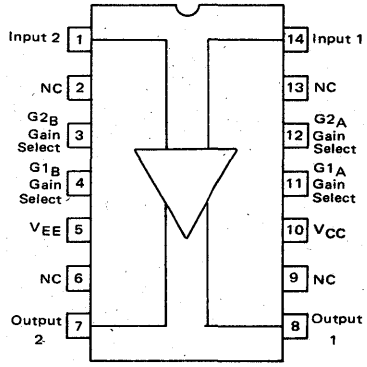


(top view)

Pin 5 connected to case

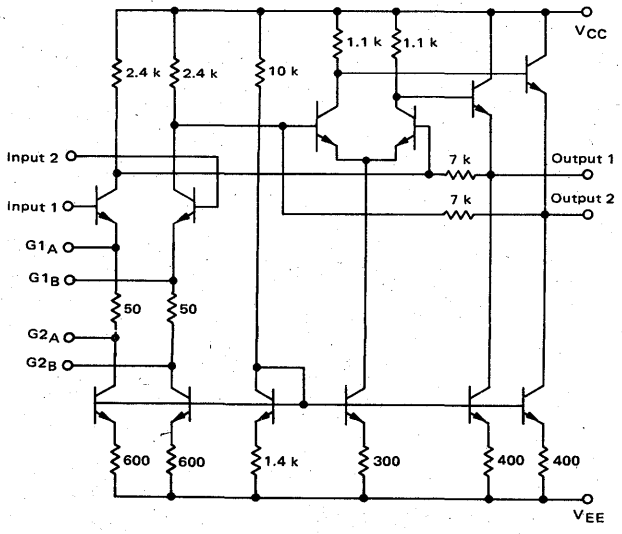


L SUFFIX
CERAMIC PACKAGE
CASE 632



(top view)

CIRCUIT SCHEMATIC



ORDERING INFORMATION

Device	Temperature Range	Package
NE592L	0 to 70°C	Ceramic DIP
NE592G	0 to 70°C	Metal Can
SE592L	-50 to +125°C	Ceramic DIP
SE592G	-55 to +125°C	Metal Can

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This is advance information and specifications are subject to change without notice.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+8.0 −8.0	Volts
Differential Input Voltages	V_{ID}	±5.0	Volts
Common-Mode Input Voltage	V_{IC}	±6.0	Volts
Output Current	I_o	10	mA
Operating Ambient Temperature Range SE592 NE592	T_A	 −55 to +125 0 to +70	°C
Operating Junction Temperature Range	T_J	175	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 V, V_{EE} = −6.0 V, V_{CM} = 0, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	SE592 Min	SE592 Typ	SE592 Max	NE592 Min	NE592 Typ	NE592 Max	Units
Differential Voltage Gain								V/V
(Gain 1, R_L = 2 kΩ Note 1)	A_{vd}	300	400	500	250	400	600	
(Gain 2, V_{out} = 3 Vp-p Note 2)		90	100	110	80	100	120	
Bandwidth	BW							MHz
(Gain 1, Note 1)		–	40	–	–	40	–	
(Gain 1, Note 2)		–	90	–	–	90	–	
Rise Time								ns
(Gain 1, V_o = 1 Vp-p, Note 1)	t_{TLH}	–	10.5	–	–	10.5	–	
(Gain 2, V_o = 1 Vp-p, Note 2)	t_{THL}	–	4.5	10	–	4.5	12	
Propagation Delay								ns
(Gain 1, V_o = 1 Vp-p, Note 1)	t_{PLH}	–	7.5	–	–	7.5	–	
(Gain 2, V_o = 1 Vp-p, Note 2)	t_{PHL}	–	6.0	10	–	6.0	10	
Input Resistance	R_{in}							kΩ
(Gain 1, Note 1)		–	4.0	–	–	4.0	–	
(Gain 2, Note 2)		20	30	–	10	30	–	
Input Capacitance								
(Gain 2, Note 2)	C_{in}	–	2.0	–	–	2.0	–	pF
Input Offset Current	I_{IO}	–	0.4	3.0	–	0.4	5.0	μA
Input Bias Current	I_{IB}	–	9.0	20	–	9.0	30	μA
Input Noise Voltage (BW = 1 kHz to 10 MHz)	V_n	–	12	–	–	12	–	μV(rms)
Input Voltage Range	V_{in}	±1.0	–	–	±1.0	–	–	V
Common-Mode Rejection Ratio	CMRR							dB
(Gain 2, V_{CM} = ±1 V, f ≤ 100 kHz)		60	86	–	60	86	–	
(Gain 2, V_{CM} = ±1 V, f = 5 MHz)		–	60	–	–	60	–	
Supply Voltage Rejection Ratio	PSRR							dB
(Gain 2, Δ V_s = ±0.5 V)		50	70	–	50	70	–	
Output Offset Voltage	V_{oo}							V
(Gain 3, R_L = ∞, Note 3)		–	0.35	0.75	–	0.35	0.75	
Output Common-Mode Voltage	V_{CMO}							V
(R_L = ∞)		2.4	2.9	3.4	2.4	2.9	3.4	
Output Voltage Swing	V_o							Vp-p
(R_L = 2k)		3.0	4.0	–	3.0	4.0	–	
Output Resistance	r_o	–	20	–	–	20	–	Ω
Power Supply Current	I_D							mA
(R_L = ∞)		–	18	24	–	18	24	

Note 1. Gain select pins $G1_A$ and $G1_B$ connected together.

Note 2. Gain select pins $G2_A$ and $G2_B$ connected together.

Note 3. All gain select pins open.

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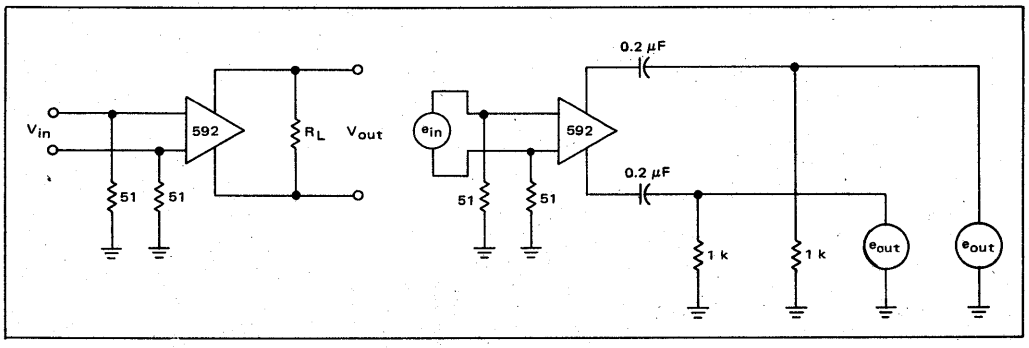
GENERAL TEST CIRCUITS



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

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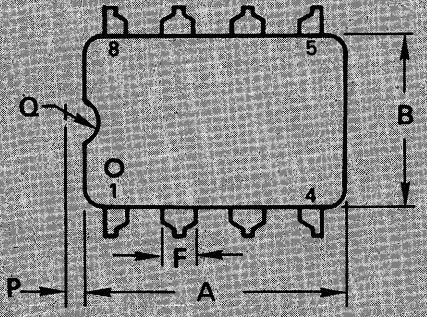
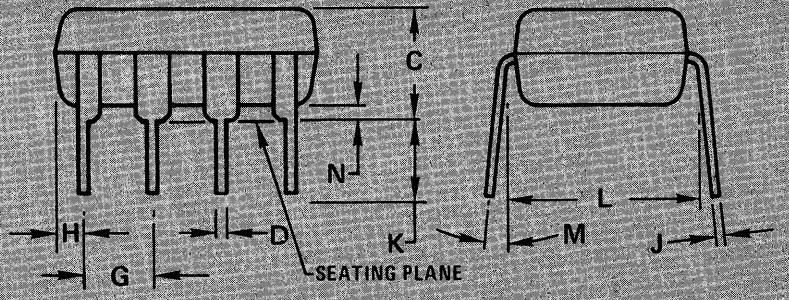
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	0.76	0.020	0.030
P	0.13	0.38	0.005	0.015
Q	0.76	1.02	0.030	0.040





Package Information and Mounting Hardware / Chapter 9

CASE OUTLINE DIMENSIONS

The packaging availability for each device type is indicated on the individual data sheets and the Selector Guide. All of the outline dimensions for the packages are given in this section. Outline dimensions for non-encapsulated standard linear device chips and flip-chip devices are found in the Chips Data Book.

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section. See individual data sheets for $T_{J(max)}$ information.

T_A = Maximum Desired Operating Ambient Temperature

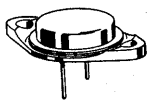
$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

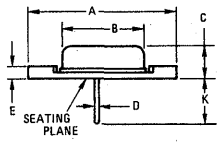
CASE 11 (TO-3)

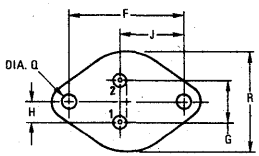
Metal Package

$R_{\theta JA}$ = 45° C/W(Typ)

$R_{\theta JC}$ = 5.5° C/W(Typ)





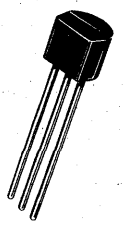


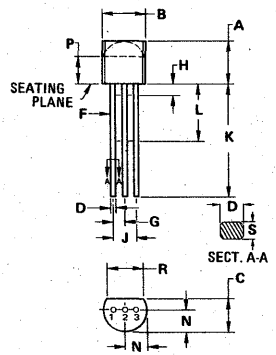
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 29 (TO-92)

Plastic Transistor

$R_{\theta JA}$ = 200° C/W





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

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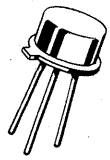
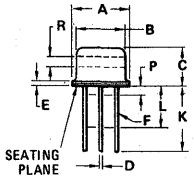
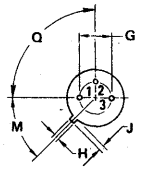
CASE 79 (TO-39)

Metal Package

$R_{\theta JA}$ = 185° C/W(Typ)







DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.89	9.40	0.350	0.370
B	8.00	8.51	0.315	0.335
C	6.10	6.60	0.240	0.260
D	0.406	0.533	0.016	0.021
E	0.229	3.18	0.009	0.125
F	0.406	0.483	0.016	0.019
G	4.83	5.33	0.190	0.210
H	0.711	0.864	0.028	0.034
J	0.737	1.02	0.029	0.040
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° NOM		45° NOM	
P	–	1.27	–	0.050
Q	90° NOM		90° NOM	
R	2.54	–	0.100	–

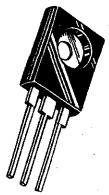
All JEDEC dimensions and notes apply.

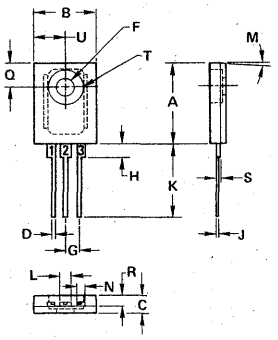
CASE 199

Plastic Package

$R_{\theta JA}$ = 65° C/W

$R_{\theta JC}$ = 5.0° C/W





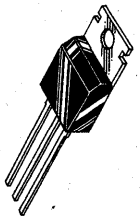
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.08	16.33	0.633	0.643
B	12.57	12.83	0.495	0.505
C	3.18	3.43	0.125	0.135
D	0.51	0.76	0.020	0.030
F	3.61	3.86	0.142	0.152
G	2.54 BSC		0.100 BSC	
H	2.67	2.92	0.105	0.115
J	0.43	0.69	0.017	0.027
K	14.73	14.99	0.580	0.590
L	2.16	2.41	0.085	0.095
M	3° TYP		3° TYP	
N	1.47	1.73	0.058	0.068
Q	4.78	5.03	0.188	0.198
R	1.91	2.16	0.075	0.085
S	0.81	0.86	0.032	0.034
T	6.99	7.24	0.275	0.285
U	6.22	6.48	0.245	0.255

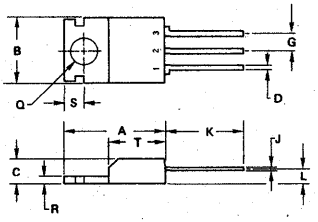
1. DIM "G" IS TO CENTER LINE OF LEADS.

CASE 313 (TO-220 Type)

Plastic Power

$R_{\theta JA}$ = 65° C/W (Typ)





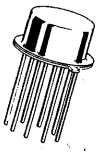
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.49	15.88	0.610	0.625
B	9.65	10.67	0.380	0.420
C	4.06	4.83	0.160	0.190
D	0.51	1.02	0.020	0.040
G	2.29	2.79	0.090	0.110
J	0.38	0.64	0.015	0.025
K	12.70	–	0.500	–
L	2.03	2.92	0.080	0.115
Q	3.53	3.73	0.139	0.147
R	0.89	1.40	0.035	0.055
R	9.02	9.40	0.355	0.370
S	2.54	3.05	0.100	0.120
T	9.02	9.39	0.355	0.370

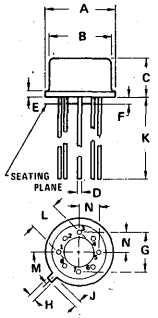
9

CASE 601

Metal Package

$R_{\theta JA}$ = 160° C/W(Typ)



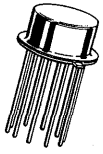


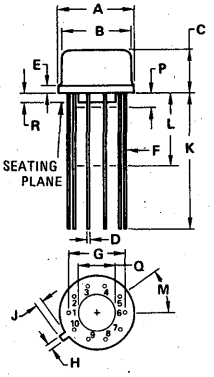
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.40	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.41	0.48	0.016	0.019
E	0.25	1.02	0.010	0.040
F	0.25	1.02	0.010	0.040
G	5.08 BSC		0.200 BSC	
H	0.71	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	–	0.500	–
L	3.05	4.06	0.120	0.160
M	45° BSC		45° BSC	
N	2.41	2.67	0.095	0.105

CASE 603B

Metal Can

$R_{\theta JA}$ = 160° C/W

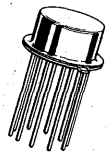


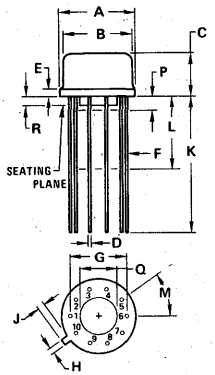


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	4.70	0.165	0.185
D	0.407	0.533	0.016	0.021
E	–	1.02	–	0.040
F	0.406	0.483	0.016	0.019
G	5.84 BSC		0.230 BSC	
H	0.712	0.864	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	–	0.500	–
L	6.35	12.70	0.250	0.500
M	36° BSC		36° BSC	
P	–	1.27	–	0.050
Q	3.56	4.06	0.140	0.160
R	0.254	1.02	0.010	0.040

CASE 603C (TO-100 Type)

$R_{\theta JA}$ = 150° C/W(Typ)





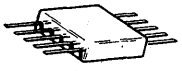
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.51	0.305	0.335
C	4.19	6.73	0.165	0.265
D	0.407	0.533	0.016	0.021
E	–	1.02	–	0.040
F	0.406	0.483	0.016	0.019
G	5.84 BSC		0.230 BSC	
H	0.712	0.864	0.028	0.034
J	0.737	1.14	0.029	0.045
K	12.70	–	0.500	–
L	6.35	12.70	0.250	0.500
M	36° BSC		36° BSC	
P	–	1.27	–	0.050
Q	3.56	4.06	0.140	0.160
R	0.254	1.02	0.010	0.040

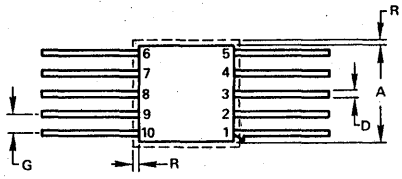
9

CASE 606 (TO-91)

Ceramic Package

$R_{\theta JA}$ = 165° C/W(Typ)

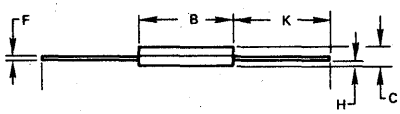




DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	6.10	7.36	0.240	0.290
B	6.10	6.60	0.240	0.260
C	0.762	1.77	0.030	0.070
D	0.254	0.482	0.010	0.019
F	0.077	0.152	0.003	0.006
G	1.15	1.39	0.045	0.055
H	0.127	0.889	0.005	0.035
K	1.78	–	0.070	–
R	–	0.381	–	0.015

All JEDEC dimensions and notes apply

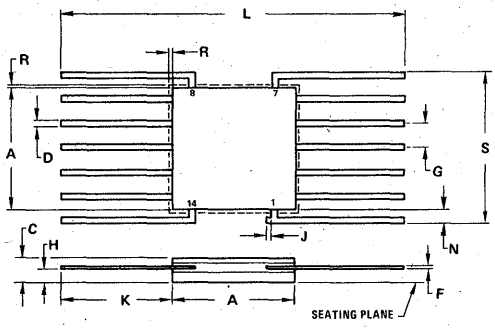
NOTE:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION (AT BODY)



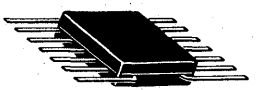
CASE 607 (TO-86 Type)

Ceramic Package

$R_{\theta JA}$ = 165° C/W(Typ)



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	6.10	6.60	0.240	0.260
C	0.76	1.78	0.030	0.070
D	0.33	0.48	0.013	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.30	0.89	0.012	0.035
J	–	0.38	–	0.015
K	6.35	9.40	0.250	0.370
L	18.80	–	0.740	–
N	0.25	–	0.010	–
R	–	0.38	–	0.015
S	7.62	8.38	0.300	0.330

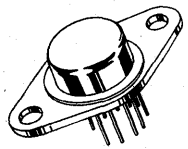


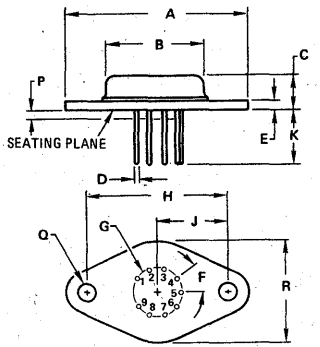
CASE 614 (TO-66 Type)

Metal Package

$R_{\theta JA}$ = 35° C/W(Typ)

$R_{\theta JC}$ = 6° C/W(Typ)





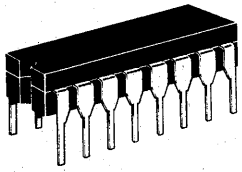
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	–	31.80	–	1.252
B	11.94	12.70	0.470	0.500
C	6.35	8.64	0.250	0.340
D	0.71	0.81	0.028	0.032
E	1.27	1.90	0.050	0.075
F	36° BSC		36° BSC	
G	8.26 BSC		0.325 BSC	
H	24.33	24.43	0.958	0.962
J	12.17	12.22	0.479	0.481
K	9.14	–	0.360	–
P	1.40 BSC		0.055 BSC	
Q	3.61	3.86	0.142	0.152
R	–	17.78	–	0.700

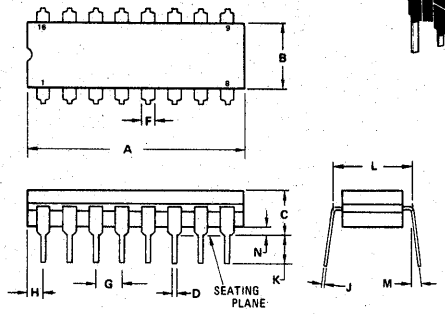
9

CASE 620

Ceramic Package

$R_{\theta JA}$ = 100° C/W(Typ)





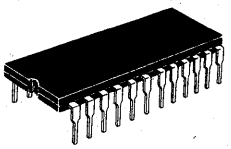
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	0.30	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

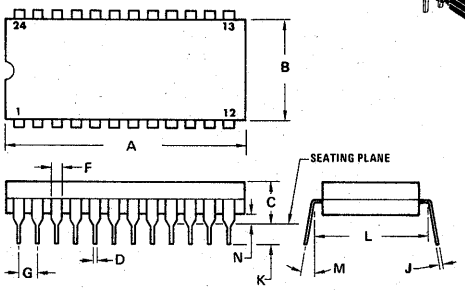
NOTES:
1 LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION'
2 PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT'
3 DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL'

CASE 623

Ceramic Package

$R_{\theta JA}$ = 53° C/W(Typ)





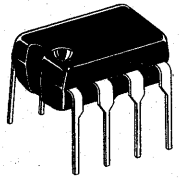
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

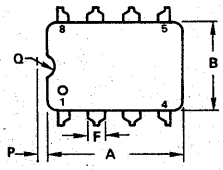
NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

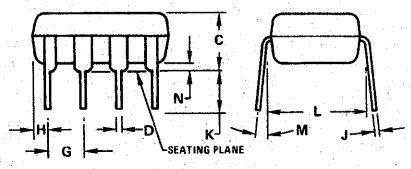
CASE 626

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)







DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	0.76	0.020	0.030
P	0.13	0.38	0.005	0.015
Q	0.76	1.02	0.030	0.040

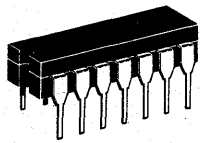
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

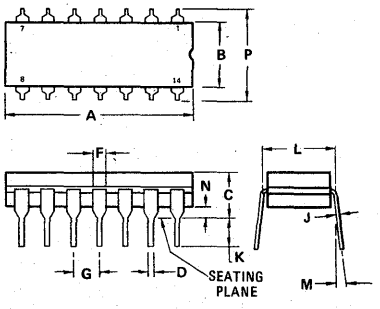
9

CASE 632 (TO-116)

Ceramic Package

$R_{\theta JA}$ = 100° C/W(Typ)





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

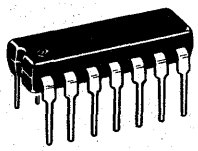
All JEDEC dimensions and notes apply.

DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

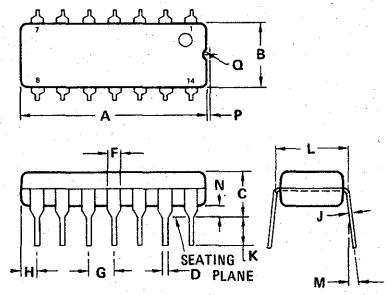
CASE 646

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

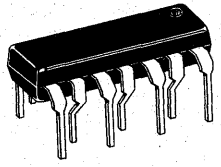


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

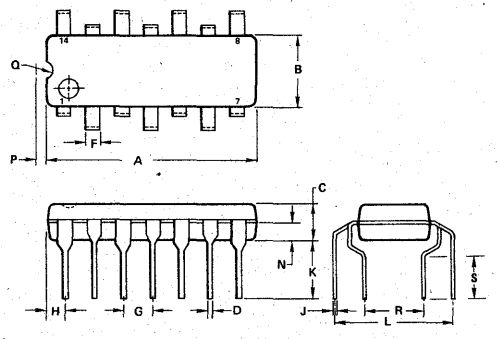
CASE 647

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)



NOTE:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION



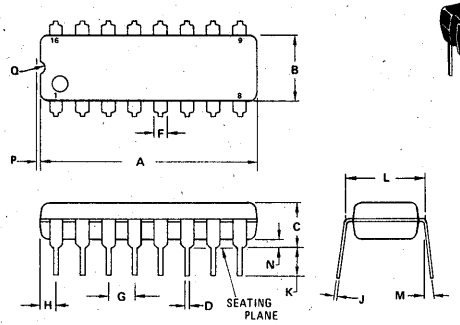
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	3.30	3.81	0.130	0.150
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.79	4.06	0.110	0.0160
L	9.52	10.92	0.375	0.430
N	1.02	1.52	0.040	0.060
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030
R	4.70	5.97	0.185	0.235
S	2.54	3.43	0.100	0.135

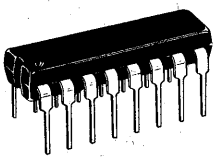
9

CASE 648

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)





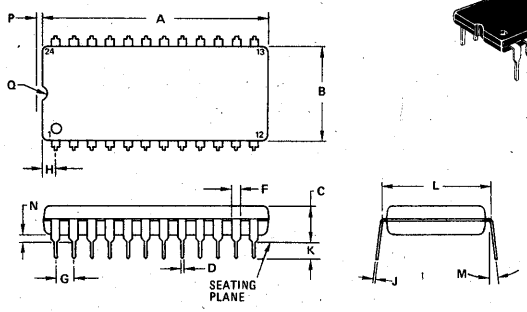
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

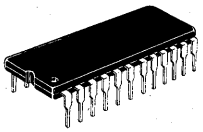
NOTE:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

CASE 649

Plastic Package

$R_{\theta JA}$ = 90° C/W(Typ)





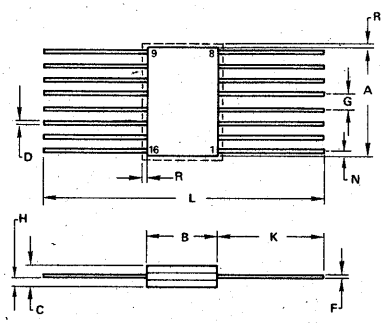
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

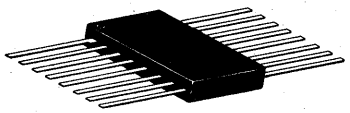
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

CASE 650

Ceramic Package

$R_{\theta JA}$ = 140° C/W(Typ)





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.22	6.60	0.245	0.260
C	1.52	2.03	0.060	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	–	0.745	–
N	–	0.51	–	0.020
R	–	0.38	–	0.015

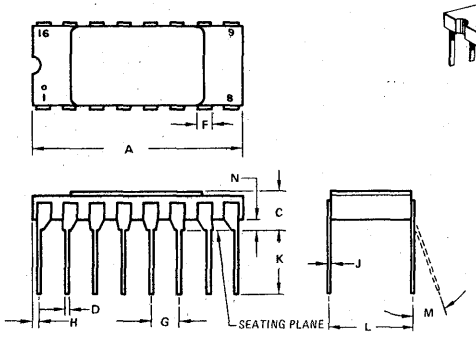
NOTES:
1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

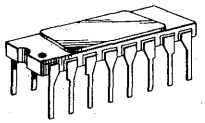
9

CASE 690

Ceramic Package

$R_{\theta JA}$ = 100° C/W(Typ)





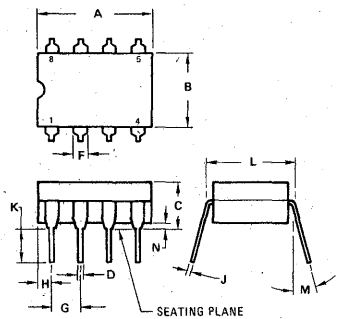
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.23	0.740	0.757
C	2.67	3.94	0.105	0.155
D	0.41	0.51	0.016	0.020
F	1.14	1.40	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	0.51	0.71	0.020	0.028
J	0.20	0.31	0.008	0.012
K	3.56	4.83	0.140	0.190
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.64	1.14	0.025	0.045

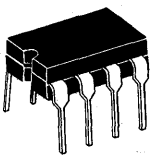
NOTE
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.

CASE 693

Ceramic Package

$R_{\theta JA}$ = 100° C/W(Typ)





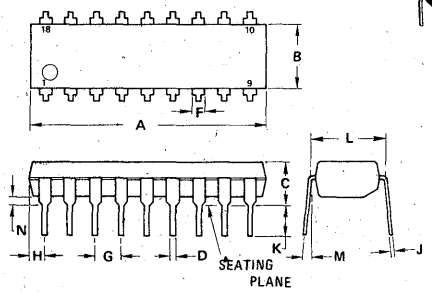
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

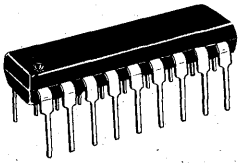
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

CASE 701

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)





NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUM OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "G").
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

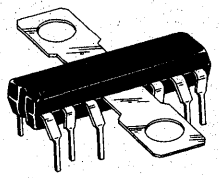
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.11	23.88	0.910	0.940
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

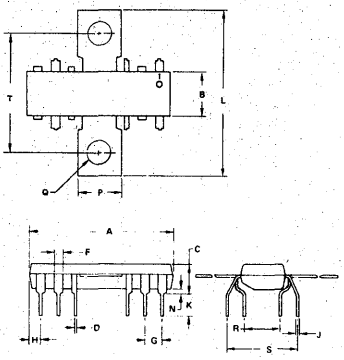
9

CASE 722

Plastic Package

$R_{\theta JA}$ = 60° C/W(Typ)



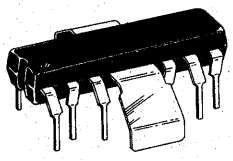


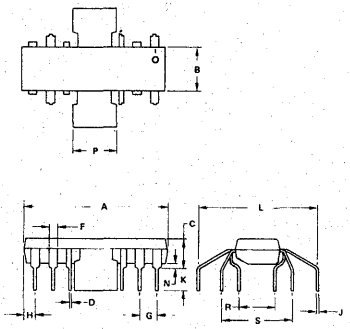
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.43	0.56	0.017	0.022
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.32	1.83	0.052	0.072
J	0.33	0.46	0.013	0.018
K	2.92	3.43	0.115	0.135
L	25.15	27.94	0.990	1.100
N	0.51	1.02	0.020	0.040
P	6.27	6.53	0.247	0.257
Q	3.48	3.73	0.137	0.147
R	4.83	5.33	0.190	0.210
S	9.91	10.41	0.390	0.410
T	16.26	16.76	0.640	0.660

CASE 722A

Plastic Package

$R_{\theta JA}$ = 60° C/W(Typ)



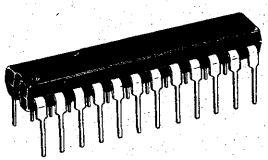


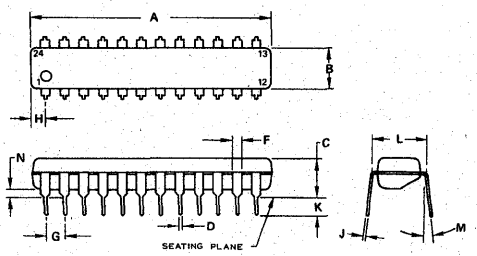
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.43	0.56	0.017	0.022
F	1.02	1.52	0.040	0.060
G	2.41	2.67	0.095	0.105
H	1.32	1.83	0.052	0.072
J	0.33	0.46	0.013	0.018
K	2.92	3.43	0.115	0.135
L	16.94	17.45	0.667	0.687
N	0.51	1.02	0.020	0.040
P	6.27	6.53	0.247	0.257
R	4.83	5.33	0.190	0.210
S	9.91	10.41	0.390	0.410

CASE 724

Plastic Package

$R_{\theta JA}$ = 100° C/W(Typ)





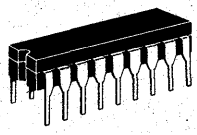
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.13	1.230	1.265
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.60	2.11	0.063	0.083
J	0.18	0.30	0.007	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040

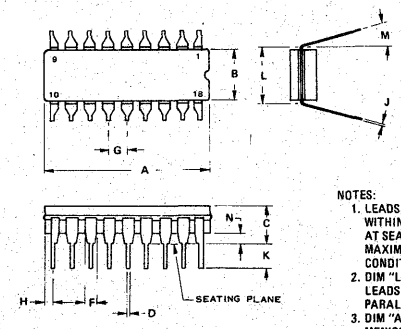
NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM D).

CASE 726

Ceramic Package

$R_{\theta JA}$ = 100° C/W(Typ)





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.35	23.11	0.880	0.910
B	6.63	7.24	0.261	0.285
C	–	5.08	–	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.76	1.02	0.030	0.040
J	0.13	0.38	0.005	0.015
K	–	4.44	–	0.175
L	7.37	8.00	0.290	0.315
M	0°	15°	0°	15°
N	0.51	0.76	0.020	0.030

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.

9

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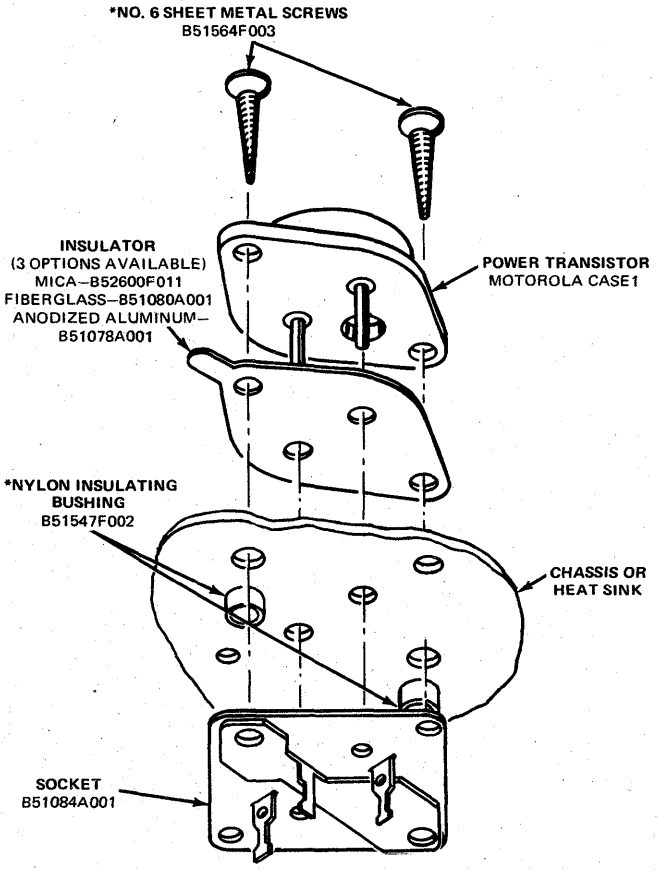
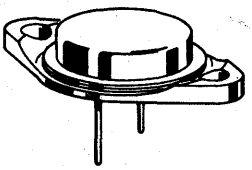
MOUNTING HARDWARE TO-3

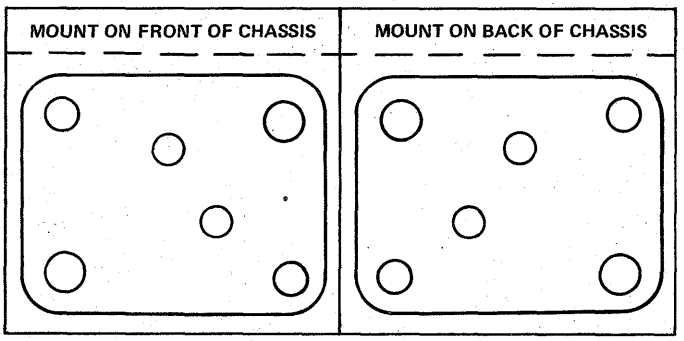


*Longer screws (not available from Motorola) and multiple bushings may be required for thick chassis or heat sink.

This hardware is applicable to the following packages.



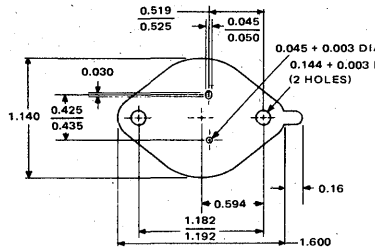
CASE 1 (TO-3)
CASE 3
CASE 11A
CASE 11 (TO-3)
CASE 12
CASE 54
CASE 197



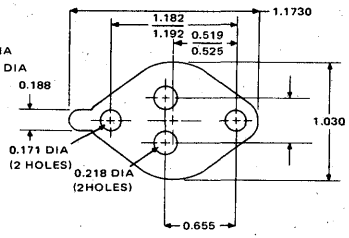
FRONT TEMPLATE
B51087A001

BACK TEMPLATE
B51087A002

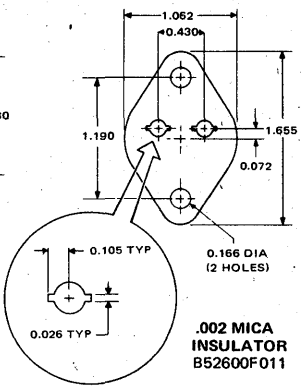
9



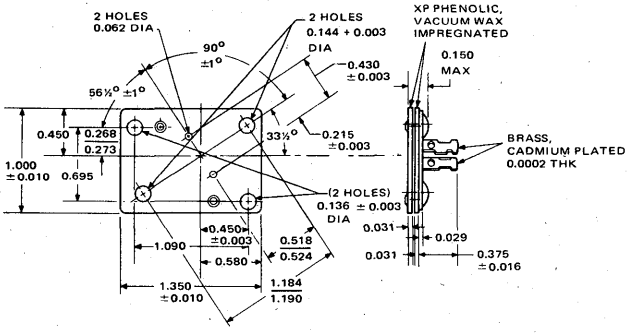
0.003 TEFLON-COATED FIBERGLASS INSULATOR
B51080A001



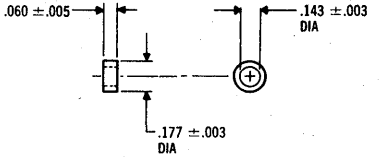
.020 ALUMINUM INSULATOR
B51078A001



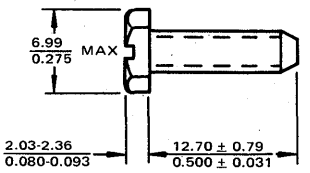
.002 MICA INSULATOR
B52600F011

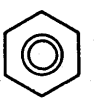


TRANSISTOR SOCKET
B51084A001

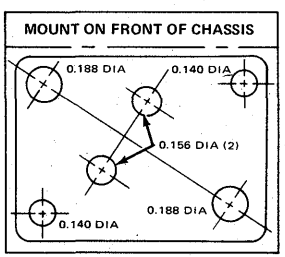


NYLON INSULATING BUSHING
B51547F002

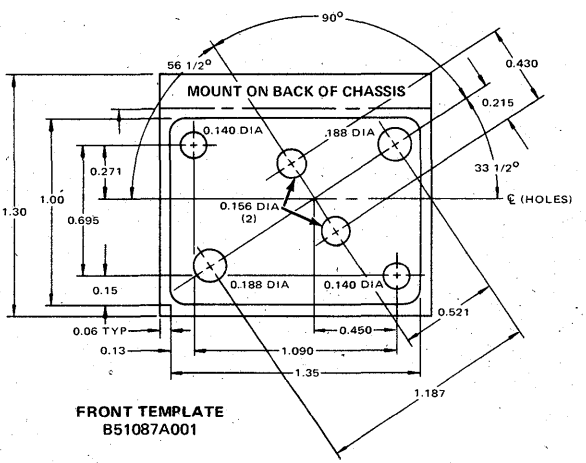




NO. 6 SHEET METAL SCREW
B51564F003



BACK TEMPLATE
B51087A002



FRONT TEMPLATE
B51087A001

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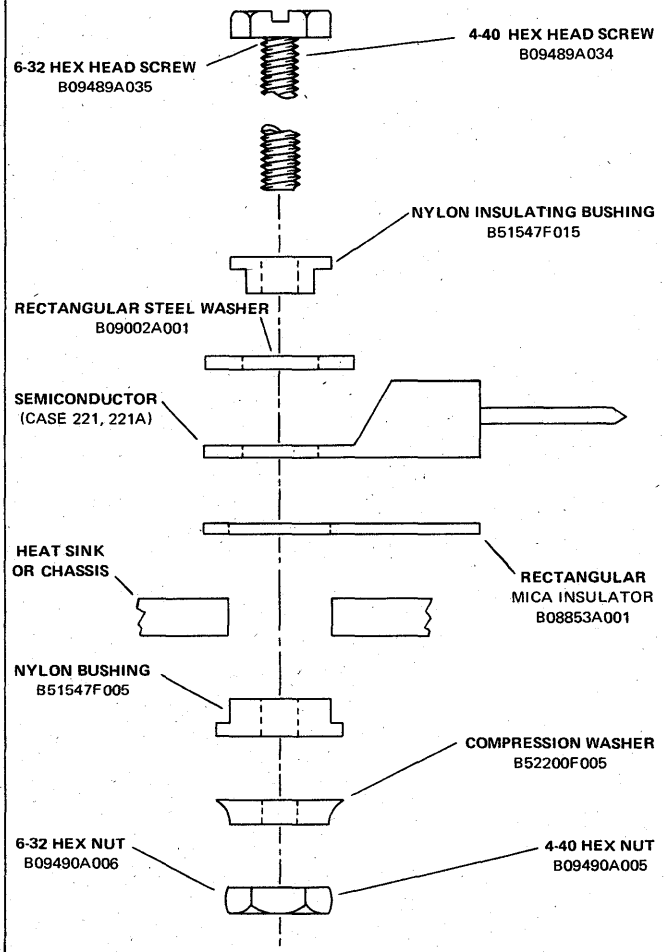
MOUNTING HARDWARE TO-220AB

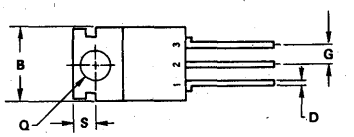
Part numbers in this column for **NON-INSULATED MOUNTING**

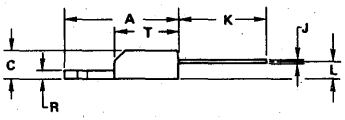
Part numbers in this column for **INSULATED MOUNTING**

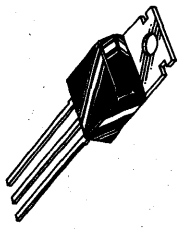


TORQUE REQUIREMENTS

INSULATED 0.68 N-M (6 IN-LBS) MAX
NON-INSULATED 0.9 N-M (8 IN-LBS) MAX







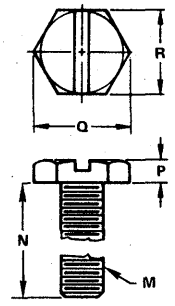
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.49	15.88	0.610	0.625
B	9.65	10.67	0.380	0.420
C	4.06	4.83	0.160	0.190
D	0.51	1.02	0.020	0.040
G	2.29	2.79	0.090	0.110
J	0.38	0.64	0.015	0.025
K	12.70	--	0.500	--
L	2.03	2.92	0.080	0.115
Q	3.53	3.73	0.139	0.147
R	0.89	1.40	0.035	0.055
R	9.02	9.40	0.355	0.370
S	2.54	3.05	0.100	0.120
T	9.02	9.39	0.355	0.370

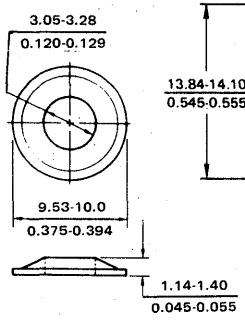
CASE 313-01
TO-220 Type

9

(DIMENSION — MILLIMETER / INCH)

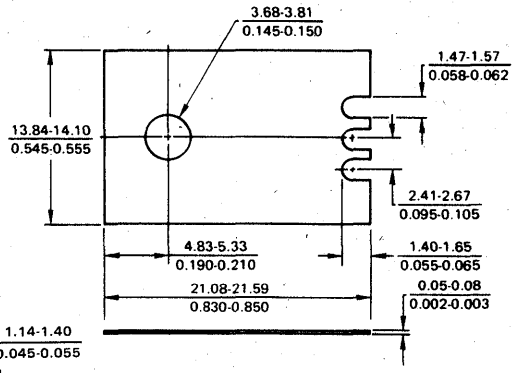
HEX HEAD SCREW
CARBON STEEL
CADMIUM-PLATED



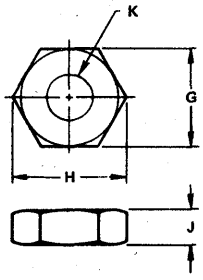


STEEL COMPRESSION WASHER
B52200F005

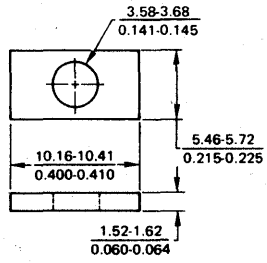
MICA INSULATOR
B08853A001



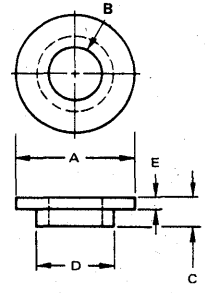
HEX NUT
CARBON STEEL
CADMIUM-PLATED



RECTANGULAR STEEL WASHER
B09002A001



NYLON INSULATING BUSHING



DIMENSIONS — MILLIMETER (INCH)

NYLON BUSHING

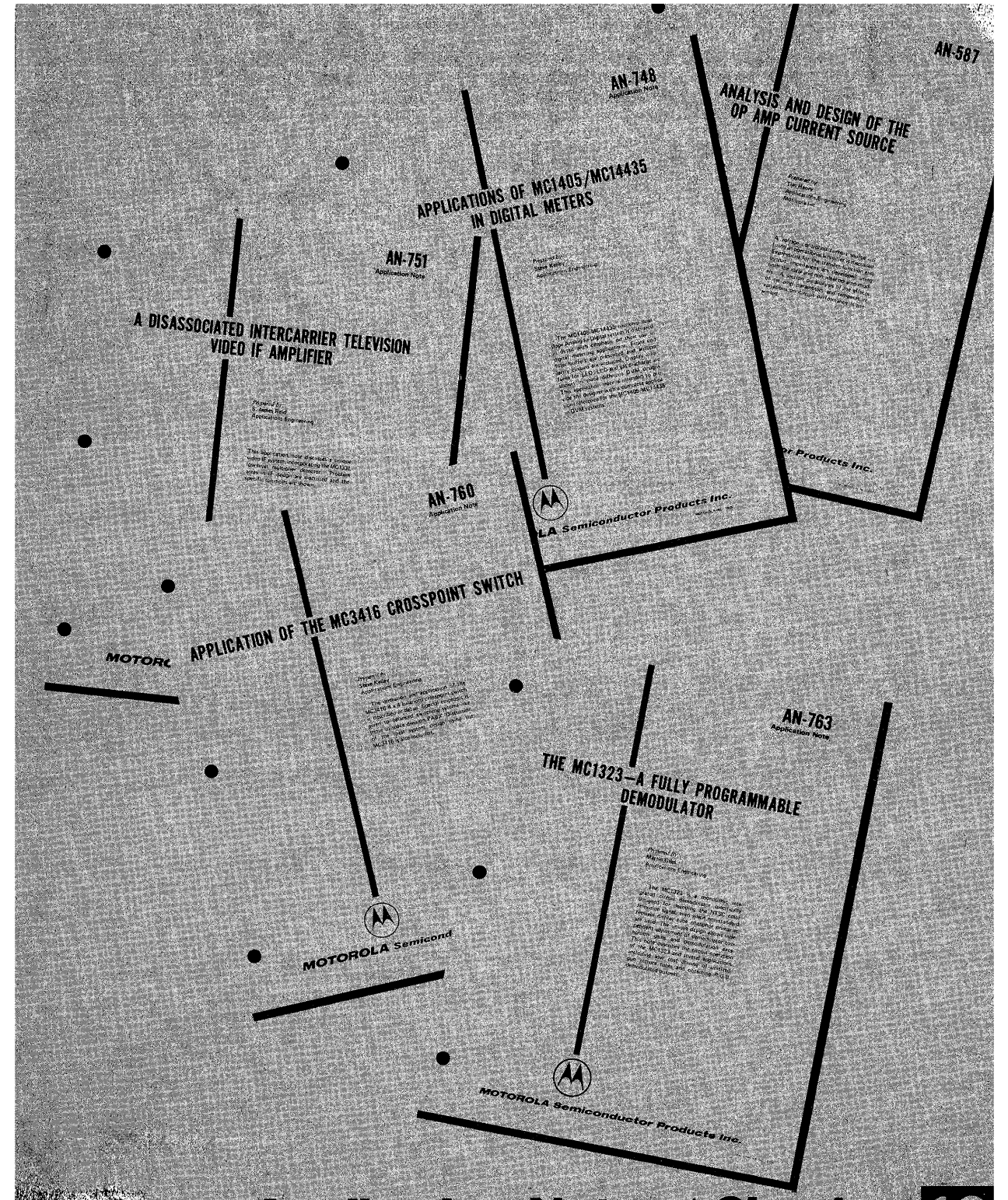
PART NO.	DIM A	DIM B	DIM C	DIM D	DIM E
B51547F005	9.40-9.65 (0.370-0.380)	3.84-4.09 (0.151-0.161)	2.16-2.41 (0.085-0.095	6.10-6.35 (0.240-0.250)	1.02-1.27 (0.040-0.050)
B51547F015	5.59-6.10 (0.220-0.240)	3.05-3.15 (0.120-0.124)	1.57-1.68 (0.062-0.066)	3.56-3.66 (0.140-0.144)	0.51-0.64 (0.020.0.025)

HEX NUT

TYPE	PART NO.	DIM G	DIM H	DIM J	DIM K
4-40	B09490A005	6.12-6.35 (0.241-0.250)	6.98-7.34 (0.275-0.289)	2.21-2.49 (0.087-0.098)	2.84 NOM (0.112 NOM)
6-32	B09490A006	7.67-7.92 (0.302-0.312)	8.74-9.17 (0.344-0.361)	2.59-2.90 (0.102-0.114)	3.50 NOM (0.138 NOM)

HEX HEAD SCREW

TYPE	PART NO.	DIM M	DIM P	DIM Q	DIM R
4-40	B09484A034	0.112-40	1.24-1.52 (0.049-0.060)	5.13 MIN (0.202 MIN)	4.60-4.75 (0.181-0.187)
6-32	B09484A035	0.138-32	2.03-2.36 (0.080-0.093)	6.91 MIN (0.272 MIN)	6.20-6.35 (0.244-0.250)



Application Notes / Chapter 10

APPLICATION NOTE ABSTRACTS

The application notes listed in this section have been prepared to acquaint the circuits and systems engineer with Motorola Linear integrated circuits and their applications. To obtain copies of the notes, simply list the AN number or numbers and send your request on your company letterhead to: Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036.

AN-204A The MC1530, MC1531 Integrated Operational Amplifiers

Two new high performance monolithic operational amplifiers feature exceptionally high input impedance and high open loop gain. This note describes the function of each stage in the circuit, methods of frequency compensating and DC biasing. Four applications are discussed: a summing circuit, an integrator, a DC comparator, and transfer function simulation.

AN-245A An Integrated Core Memory Sense Amplifier

This application note discusses core memories and related design considerations for a sense amplifier. Performance and environmental specifications for the amplifier design are carefully established so that the circuit will work with any computer using core memories. The final circuit design is then analyzed and measured performance is discussed. The amplifier features a small uncertainty region (6 mV max), adjustable voltage gain, and fast cycle time (0.5 μs).

AN-261A Transistor Logarithmic Conversion Using an Operational Amplifier

The design of a log amplifier using a common base transistor configuration as the feedback element of an integrated circuit operational amplifier circuit is discussed in this application note. Six decades of logarithmic conversion are obtained with less than 1% error of output voltage. The possible causes of error are discussed followed by two applications: direct multiplication of two numbers, and solution of the equation $Z = X^n$.

AN-273A More Value out of Integrated Operational Amplifier Data Sheets

The operational amplifier is rapidly becoming a basic building block in present day solid state electronic systems. The purpose of this application note is to provide a better understanding of the open loop characteristics of the amplifier and their significance to overall circuit operation. Also, each parameter is defined and reviewed with respect to closed loop considerations. The importance of loop gain stability and bandwidth is discussed at length. Input offset circuits are also reviewed with respect to closed loop operation.

AN-290B Mounting Procedure for, and Thermal Aspects of, Thermopad Plastic Power Devices

Many Motorola power devices are now available in the Plastic Thermopad packages. Three package types are presently available. This application note provides information concerning the handling and mounting of these packages, as well as information on some thermal aspects.

AN-401 The MC1554 One-Watt Monolithic Integrated Circuit Power Amplifier

This application note discusses four different applications for the MC1554, along with a circuit description including DC characteristics, frequency response, and distortion. A section of the note is also devoted to package power dissipation calculations including the use of the curves on the power amplifier data sheet.

AN-403 Single Power Supply Operation of IC Op Amps

A split zener biasing technique that permits use of the MC1530/1531, MC1533, and MC1709 operational amplifiers and their restricted temperature counterparts MC1430/1431, MC1433 and MC1709C from a single power supply voltage is discussed in detail. General circuit considerations as well as specific AC and DC device considerations are outlined to minimize operating and design problems.

AN-404 A Wideband Monolithic Video Amplifier

This note describes the basic principles of AC and DC operation of the MC1552G and MC1553G, characteristics obtained as a function of the device operating modes, and typical circuit applications.

AN-407 A General Purpose IC Differential Output Operational Amplifier

This application note discusses four different applications for the MC1520 and a complete description of the device itself. The final sections of the note discuss such topics as operation from single and split power supplies, frequency compensation, and various feedback schemes.

AN-411 The MC1535 Monolithic Dual Op Amp

This note discusses two dual operational amplifier applications and an input compensation scheme for fast slew rate for the MC1535. A complete AC and DC circuit analysis is presented in addition to many of the pertinent electrical characteristics and how they might affect the system performance.

AN-421 Semiconductor Noise Figure Considerations

A summary of many of the important noise figure considerations related with the design of low noise amplifiers is presented. The basic fundamentals involving noise, noise figure, and noise figure-frequency characteristics are then discussed with the emphasis on characteristics common to all semiconductors. A brief introduction is made to various

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methods of data sheet presentation of noise figure and a summary is given for the various methods of measurement. A discussion of low noise circuit design, utilizing many of the previously discussed considerations, is included.

AN-439 MC1539 Op Amp and its Applications

This application note discusses the MC1539, a second generation operational amplifier. The general use and operation of the amplifier is discussed with special mention made of improved operation over that of its first generation predecessor—the 709 type amplifier.

In addition to the detailed discussion on the DC and AC operation of the device, considerable emphasis is placed on operational performance. Many applications are offered to demonstrate the device capability, including a high frequency feed-forward scheme, and a source follower application.

AN-459 A Simple Technique for Extending Op Amp Power Bandwidth

The design of fast response amplifiers is presented without the use of "tricky" compensation procedures.

AN-460 Using Transient Response to Determine Operational Amplifier Stability

Analysis and an example are given for a technique that evaluates the stability of any particular feedback amplifier configuration by analyzing its response to a step-function input.

AN-471 Analog-to-Digital Conversion Techniques

The subject of analog-to-digital conversion and many of the techniques that can be used to accomplish it are discussed. The paper is written in general terms from a system point of view and is intended to assist the reader in determining which conversion technique is best suited for a given application.

AN-473 A Monolithic High-Power Series Voltage Regulator

This note discusses MC1560/MC1561 voltage regulator in terms of internal operation, development of these circuits, and how they are advantageously used in supply fabrication.

AN-474 The MC1541—A Gated Dual-Channel Sense Amplifier for Core Memories

The MC1541 sense amplifier can provide many magnetic core memory systems with lower system cycle times and a lower package count than with previous sense amplifiers. Circuit operation, design considerations, interface problems and typical applications are discussed.

AN-475 Using the MC1545—A Monolithic, Gated-Video Amplifier

Because of the unique design of the MC1545, this amplifier can be used as a gated video amplifier, sense amplifier, amplitude modulator, frequency shift keyer, balanced modulator, pulse amplifier, and many other applications. This note describes the AC and DC operation of the circuit and presents applications of the device as a video switch, amplitude modulator, balanced modulator, pulse amplifier, and others.

AN-489 Analysis and Basic Operation of the MC1595

The MC1595 monolithic linear four-quadrant multiplier is discussed. The equations for the analysis are given along with performance that is characteristic of the device. A few basic applications are given to assist the designer in system design.

AN-491 Gated Video Amplifier Applications The MC1545

This application note reviews the basic operation of the MC1545 and discusses some of the more popular applications for the MC1545. Included are several modulator types, temperature compensation of the active gate, AGC, gated oscillators, FSK systems, and single supply operation.

AN-498 Voltage and Current Boost Techniques Using The MC1560-61

The stability requirements for the current boosted MC1560-61 are discussed. Both internal and external compensation techniques are shown, along with heat-sink design information and typical circuits, including a self-oscillating switching regulator, and a voltage boost circuit.

AN-499 Shutdown Techniques for the MC1560-61/69 Monolithic Voltage Regulators

This note discusses the many ways one can use the shutdown control for the MC1560 Monolithic Voltage Regulator. These include logic control, short circuit detection, over voltage detection, junction temperature control, and thermal feedback. Also discussed, are current foldback and methods of restarting automatically from the shutdown state. The techniques discussed apply equally to the MC1560, MC1561, and MC1569 positive voltage regulators.

AN-513 A High Gain Integrated Circuit RF-IF Amplifier with Wide Range AGC

This note describes the operation and application of the MC1590G, a monolithic RF-IF amplifier. Included are several applications for IF amplifiers, a mixer, video amplifiers, single and two-stage RF amplifiers.

AN-522 The MC1556 Operational Amplifier and its Applications

This application note discusses the MC1556, a second generation, internally compensated monolithic operational amplifier. Particular emphasis is placed on its distinct advantages over the early 709-type amplifier and the more recent 741-type amplifier.

Along with a description of its operation this note presents a discussion on various applications of the MC1556, highlighting its capabilities, and points out its characteristics so the reader may make effective use of the device.

AN-531 MC1596 Balanced Modulator

The MC1596 monolithic circuit is a highly versatile communications building block. In this note, both theoretical and practical information are given to aid the designer in the use of this part. Applications include modulators for AM, SSB, and suppressed carrier AM; demodulators for the previously mentioned modulation forms; frequency doublers and HF/VHF double balanced mixers.

AN-533 Semiconductors for Plated-Wire Memories

An introduction to the operation and electrical characteristics of plated-wire memories is provided in conjunction with the applications of semiconductors that interface with the plated-wire memories.

Devices discussed include drivers, sense amplifiers, and decoders. Memory organization and memory-related semiconductor applications are also mentioned.

AN-543A Integrated Circuit IF Amplifiers for AM/FM and FM Radios

This application note discusses the design and performance of four IF amplifiers using integrated circuits. The IF amplifiers discussed include a high performance circuit, a circuit utilizing a quadrature detector, a composite AM/FM circuit, and an economy model for use with an external discriminator.

AN-545 Television Video IF Amplifier Using Integrated Circuits

This applications note considers the requirements of the video IF amplifier section of a television receiver, and gives working circuit schematics using integrated circuits which have been specifically designed for consumer oriented products. The integrated circuits used are the MC1350, MC1352, MC1353 and the MC1330.

AN-547 A High-Speed Dual Differential Comparator, The MC1514

This application note discusses a few of the many uses for the MC1514 dual comparator. Many applications such as sense amplifiers, multivibrators, and peak level detectors are presented.

AN-553 A New Generation of Integrated Avionic Synthesizers

The need to generate signals of a multitude of different frequencies for avionic systems has resulted in complex solutions in the past. With the introduction of certain standard product integrated circuits, frequency synthesis using digital phase locked loop techniques presents a more practical solution. Several different types of servo phase locked loop systems are discussed and a practical design example is given. Results of design examples are presented along with possible applications.

AN-557 Analog-to-Digital Cyclic Converter

The A/D cyclic converter discussed in this note provides medium speed (1-5μs/ bit) and medium accuracy (7 or 8 bits) operation. A Cyclic converter uses the successive approximation technique in which an unknown analog input voltage is successively compared to a reference voltage to determine each bit of the digital output.

AN-559 Simple RAMP A/D Converter

A simple single ramp A/D converter which incorporates a calibration cycle to insure an accuracy of 12 bits is discussed. The circuit uses standard ICs and requires only one precision part—the reference voltage used in the calibration. This converter is useful in a number of instrumentation and measurement applications.

AN-564 An ADF Frequency Synthesizer Utilizing Phase Locked-Loop Integrated Circuits

This application note describes an IC phase locked-loop frequency synthesizer suitable for the local osciallator function in aircraft Automatic Direction Finder (ADF) equipment.

AN-587 Analysis and Design of the Op Amp Current Source

A voltage controlled current source utilizing an operational amplifier is discussed. Expressions for the transfer function and output impedances are developed using both the ideal and non-ideal op amp models. A section on analysis of the effects of op amp parameters and temperature variations on circuit performance is presented.

AN-588 A 20 kHz, 1kW Line Operated Inverter

This report describes a 1 kilowatt ultrasonic inverter for use in 208-volt, line-operated, computer main-frame power supply systems. This particular design has an output capability of 5 Volts at 200 Amperes.

AN-589 Generate Custom Waveforms Digitally

A method of generating custom waveforms using IC counters, a read-only memory, and a new monolithic D/A Converter is described. Performance of a prototype model is noted as well as possible applications.

AN-590 Servo Motor Drive Amplifiers

The design of transformerless, AC servo amplifiers using power darlington transistors and IC op amps are discussed. Two types of power amplifiers are illustrated, one using single +28 Volt power supply, the second using high voltage transistors in complementary configuration for operating directly off the line.

Four different op amp preamplifiers and 90 phase shifters are also described.

AN-594 A Frequency Synthesizer for Aircraft Automatic Direction Finding Systems

This report describes a phase locked loop frequency synthesizer suitable as the local oscillator in an ADF system. The synthesizer is designed for receivers using a 455 kHz IF system. Motorola application note AN-564 describes a similar system for receivers using a 10.7 MHz IF.

AN-597 Power Control Using the Zero Voltage Switch

This application note discusses the advantages of zero-voltage switching using the Motorola MFC8070. A temperature control circuit is shown which demonstrates the design flexibility of CMOS and optical-coupler combinations.

AN-599 Mounting Techniques For Metal Packaged Power Semiconductors

For cooler, more reliable operation, proper mounting procedures must be followed if the interface thermal resistance between the semiconductor package and heat sink is to be minimized. Discussed are aspects of preparing the mounting surface, using thermal compounds, and fastening techniques. Typical interface thermal resistance is given for a number of packages.

AN-702 High Speed Digital-To-Analog and Analog-To-Digital Techniques

A brief overview of some of the more popular techniques for accomplishing D/A and A/D techniques. In particular those techniques which lead themselves to high speed conversion.

AN-703 Designing Digitally-Controlled Power Supplies

This application note shows two design approaches; a basic low voltage supply using an inexpensive MC1723 voltage regulator and a high current, high voltage, supply using the MC1466 floating regulator with optoelectronic isolation. Various circuit options are shown to allow the designer maximum flexibility in any application.

AN-705 Pulse Width Modulation for Small DC Motor Control

This application note explains the use of modern pulse width modulation techniques as an efficient and economical solution to small DC motor control. Several practical circuit design approaches using discrete, operational amplifier and integrated circuit devices are described and illustrated.

AN-710 Communication System Transmission Losses

This report shows the derivation of the equations used to calculate the insertion loss associated with various component parts of a communications channel. The combinations of components form a system whose overall loss may not be equal to the sum of the losses of the various parts.

AN-711 The Recovery of Recorded Digital Information in Drum, Disk and Tape Systems

The use of magnetic recording techniques has long been an important means of sorting digital information, as evidenced by the wide variety of equipment currently in use. Representative systems utilize drums, disks and tape as the recording medium.

All three techniques share the common problem of recovering the recorded digital information. The analog signal obtained by passing the recording medium by a magnetic sensor (Read Head) must be converted to a suitable digital format.

This application note reviews the general problem and discusses a number of specific circuit approaches.

AN-713 Binary D/A Converters can Provide BCD-Coded Conversion

This note describes the application and use of integrated circuit D/A converters for use in providing a BCD-coded conversion. The technique is illustrated using a 2-1/2 digit digital voltmeter.

AN-714 A Personalized Heart-Rate Monitor with Digital Readout

Using the micropower operational amplifier MC1776 and CMOS digital integrated circuits, entirely self-contained portable electro-medical monitoring equipment can be built. This note details the construction of a heart-rate monitor giving a digital indication, beat-by-beat.

AN-716 A/D Conversion Series – Part V Successive Approximation A/D Conversion

Recent advances in integrated circuit design and technology have resulted in reduced cost of high performance successive approximation analog to digital converters. This note describes and illustrates two examples of how modern IC components have changed this well known technique.

AN-717 Battery Powered 5-MHz Frequency Counter

This application note describes a battery-powered 5-MHz frequency counter using the McMOS logic family for low-power operation. The basic counter is optimized, at a 12-volt supply for maximum performance with a linear input-signal conditioner. Several options are discussed which optimize the basic counter for minimum power dissipation. These options include a CMOS input signal-conditioner and multiplexed LED displays.

AN-719 A New Approach to Switching Regulators

This article describes a 24-Volt, 3-Ampere switching mode supply. It operates at 20 kHz from a 120 Vac line with an overall efficiency of 70%. New techniques are used to shape the load line. The control portion uses a quad comparator and an opto coupler and features short circuit protection.

AN-720 Interfacing with MECL 10,000

This article describes some of the MECL circuits used to interface with signals not meeting MECL input or output requirements. The characteristics of these circuits such as; input impedance, output drive, gain, and bandwidth allow the system designer to use these parts to optimize his system. MECL interface circuits overcome a problem area of many system designs, which is the efficient coupling on non-compatible signals.

AN-732A A Non-Volatile Microprocessor Memory Using 4K N-Channel MOS RAMs

NMOS semiconductor technology has made inroads into high density/high performance circuit design. The one-chip microprocessor, Random Access Memories, and Read Only Memories, are changing system implementation from random logic designs to software and firmware programmable microcomputing systems. Such systems frequently require relatively

large amounts of memory.

This paper describes the design of an 8192-byte non-volatile Random Access Memory system using the MCM6605 4K x 1 RAM. The system is designed to work with the Motorola MC6800, an 8-bit microprocessor.

AN-737 Switched Mode Power Supplies – Highlighting A 5-V, 40-A Inverter Design

This application note identifies the features of various regulator circuits that are in use today in AC to DC power supplies. The note also illustrates how these circuits may be used as complementary building blocks in a system design. Primary emphasis is on switched mode regulators because they fill the present need for energy and space savings.

A complete 5-V, 40-A line operated inverter supply is described in detail including design procedures for the magnetic components. The inverter itself is a "state-of-the-art" design which features CMOS logic, high voltage power transistors, Schottky rectifiers and an opto-electronic coupler. It operates with a full load efficiency of 80% at a frequency of 20 kHz.

AN-739 A Synthetic Spectrum Tuning System for TV

A tuning system is described which uses a complete spectrum of TV channel markers to achieve precise tuning to any channel.

AN-741 Interface Considerations for Numeric Display Systems

This application note describes several methods of multiplexing multi-digit, seven-segment displays. The logic devices illustrated are primarily CMOS with two examples describing TTL. The displays discussed are liquid crystal, LED, gas discharge, incandescent and fluorescent. How to interface between the logic and these displays, and what the interface considerations are, are described in detail.

AN-744 A Phase-Locked Loop Tuning System for Television

This note describes a frequency domain tuning system which utilizes direct digital countdown of the varactor tuner's local oscillator to obtain the proper local oscillator frequency for the channel number selected. The system features direct channel access with equal ease of tuning and an exact channel readout for all VHF and UHF channels.

AN-746 A 3½ Digit DVM Using an Integrated Circuit Dual Ramp System

This application note describes the design of a 3½-digit DVM (digital voltmeter) using the MC1405 and the MC14435 dual ramp A/D system. The performance criteria is that of a lab quality DVM with both 3½-digit resolution and accuracy while still retaining a low cost and low parts count instrument. Features of the DVM include circuitry for a high impedance input, autopolarity and overrange indication.

AN-748 Applications of MC1405/MC14435 In Digital Meters

The MC1405/MC14435 two chip dual slope Analog-to-Digital system is discussed in detail with emphasis on their use in digital metering applications. Front end filter/buffers are presented and autopolarity circuits are included. Display interfaces for LED, LCD and gas discharge are shown in three different DVM designs. This application note is intended to provide the designer with a complete applications reference for the MC1405/MC14435 in DVM systems.

AN-751 A Disassociated Intercarrier Television Video IF Amplifier

This application note discusses a unique video IF system, incorporating the MC1331, low-level multiplier detector. Problem areas in IF design are discussed and the specific solutions are shown.

AN-752 An 80-Watt Switching Regulator for CATV and Industrial Applications

This application note describes a 24-Volt, 3-Ampere switching, regulated power supply that operates above 18 kHz from a 40-to 60-Volt, 60-Hz square wave source (CATV power line from a ferroresonant transformer) or a dc standby source with input output isolation. The control circuit consists of a dual operational amplifier and a linear integrated circuit timer which are used to vary the on time of a new high-speed power transistor. The circuit provides good efficiency, good regulation, low output ripple and incorporates input and output voltage over shutdown protection.

AN-757 Analog-to-Digital Conversion Techniques with the MC6800 Microprocessor System

This application note describes several analog-to-digital conversion systems implemented with the M6800 microprocessor and external linear and digital IC's. Systems consisting of an 8- and 10-bit successive approximation approach, as well as dual ramp techniques of 3½-and 4½-digit BCD and 12-bit binary, are shown with flow diagrams, source programs and hardware schematics. System tradeoffs of the various schemes and programs for binary-to-BCD and BCD-to-7 segment code are discussed.

AN-760

The operation and application of the MC3416 4 x 4 balanced crosspoint switch is described in detail. Special emphasis is given to balanced switching systems like those in space division PABX. Discussion of the total system design using the MC3416 is also included.

AN-761

This note describes video amplifier design considerations for unitized gun and conventional picture tubes. Some unique design techniques are discussed

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taking advantage of Motorola's MC1323 chroma demodulator. Finally, design objectives of video amplifiers are discussed.

AN-763

The MC1323 is a monolithic integrated circuit demodulator specifically designed for decoding the NTSC color television signal, even when non-standard receiver display tube phosphor primaries are used. The unique design allows independent adjustment of demodulator conversion gains and demodulation axes. This note describes the circuit operation of the MC1323 and several applications including low cost driving of unitized gun picture tubes and obtaining R-G-B demodulated outputs.

AN-765

This note describes a technique of measurement of the IF contribution and ways of minimization of the IF noise. An IF design, following these procedures, is described to meet the desired noise performance.

Engineering Bulletin ABSTRACTS

EB-13 Switching Regulators Head 'Em Off At The Series Pass

In EB-13, you'll find a switching regulator design. From a line which can fluctuate from 100 to 140 Vac, it's capable of providing a regulated 24 Vdc to a load varying from 1.5 to 3.0 amperes.

EB-14 Simple Linear Voltage Sweep Uses The MC1555 Timer

EB-14 shows how the MC1555 timer can be used with five simple external components to make a linear voltage sweep useful in ramp, deflection and function generator designs.

EB-20 Multiplier/Op Amp Circuit Detects True RMS

Two op amps and two multipliers are used in the circuit described by EB-20 to obtain the true rms of an input voltage ranging from 2 to 10 Vpk.

EB-21 DAC Key To Inexpensive 2-2/3 Digit Voltmeter

EB-21 presents an idea for the core of an economical 2-2/3 digit voltmeter. Built around Motorola's MC1408 8-bit D/A converter, the meter can measure to 2.55 V in 10 mV steps.

EB-24 Input Buffer Circuits For The MC1505 Dual Ramp A-to-D Converter Subsystem

Several bipolar op amp buffers of medium-high impedance are described in this bulletin. It also discusses FET input op amp buffers providing high impedance and temperature drift under 1 mV over the O°C to 50°C range.

EB-35 Autopolarity Circuits For The MC1405 Dual-Slope A/D Converter System

Engineering Bulletin EB-35 provides three input stage designs, each of which will provide the autopolarity function for the unipolar MC1405 A/D converter subsystem.

EB-36 4-1/2 Digit DVM System Using The MC1505 Dual-Slope Converter

The circuits required for implementing a 4-1/2 digit DVM based on the MC1505 dual slope A-to-D converter are presented in EB-36. With this design, a 4-1/2 digit accurate system with excellent environmental stability is possible.

EB-43 A 9-1/2 Digit Gas Discharge Display System With Leading Zero Suppression

The 9-1/2 digit multiplexed gas discharge display system described in EB-43 was designed for use in a 1.2 GHz frequency counter. The display system features leading zero blanking and constant current segment drives. Its logic supply is +5 V.

EB-50 Build This Simple, Battery-Powered 3-1/2 Digit DVM From Standard Parts

EB-50 describes a simple, battery-powered 3-1/2 digit DVM capable of measuring up to 20 volts that can be built from readily obtained standard parts. Sufficient information is provided to construct the circuit including schematic, PC board layout, parts list and calibration instructions.

EB-51 Successive Approximation BCD A/D Converter

A successive approximation A/D converter in which a digital-to-analog converter in a feedback loop produces a BCD digital output from an analog input is described in EB-51.

EB-52 Control Your Switching Regulator With The MC3380 Astable Multivibrator

Engineering Bulletin EB-52 describes the operation and characteristics of the MC3380 astable multivibrator and details the design of a 200 volt switching regulator circuit for gas discharge displays using this device as the control element.

EB-55 Battery-Powered 3-1/2 Digit Multimeter

Using the information provided in EB-55, a battery-powered 3-1/2 digit multimeter can be built and packaged in a pocket calculator case. The bulletin discusses the theory of design and describes the basic meter, buffer and autopolarity circuit, multimeter functions, choice of batteries and packaging in detail. Layouts for the two PC boards, a complete parts list and calibration procedures are also given.

EB-57 An Economical FM Transmitter Voice Processor from a Single IC

An MC3401 Quad OP-Amp is used as a Microphone/Modulation interface in an FM transmitter.

EB-58 Analog Data Acquisition Network for Digital Processing Using the MC1405-MC14435 A/D System

An MC1405-MC14435 combination is used to form a dual-slope A/D converter for analog data acquisition.

EB-64 Bus Transceivers For The General Purpose Interface Bus (GPIB)

This bulletin discusses the use of the MC3440, 41, 43, and 46 general purpose interface bus (GPIB) transceivers. Also included are an introduction to the GPIB, a description of the hardware required for a GPIB-equipped instrument, GPIB bus electrical characteristics, and the IEEE 488 standard for GPIB.

EB-65 Switchmode Power Supply

This bulletin describes a line-operated 5 V, 50 A, 20 kHz switching power supply intended for use as a logic supply in computer and industrial applications. It has a constant current limiting, inrush surge current limiting, and a soft-start feature to prevent output voltage overshoots during start-up.