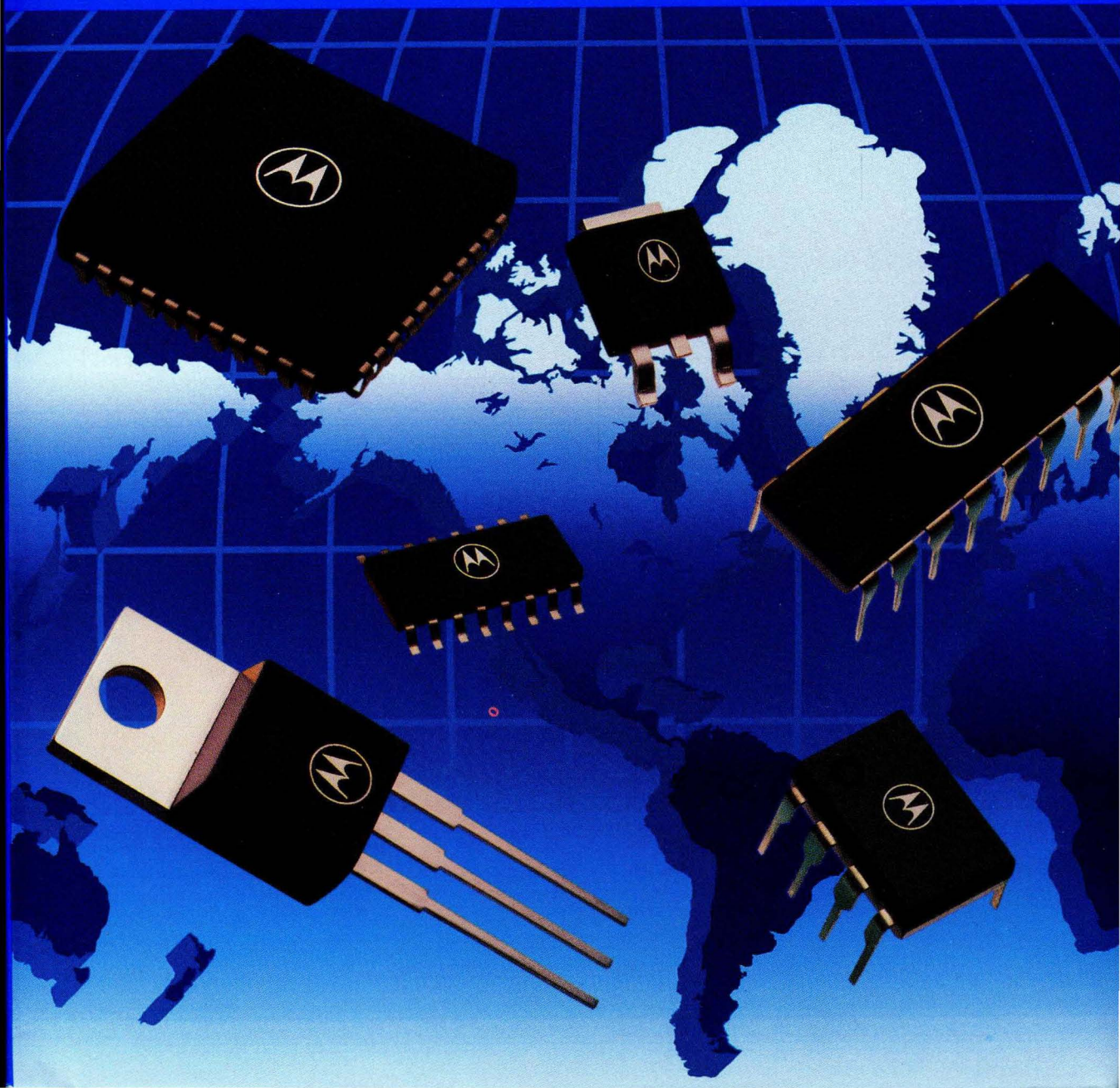
MOTOROLA

DL128/D
REV 4

Linear/Interface ICs

Device Data

Vol. I



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TDA1524A
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New Product Literature (Referenced)

AN1046
AN1077
AN1122
AN1203
AN1510

MOTOROLA

LINEAR/INTERFACE ICs DEVICE DATA

This publication presents technical information for the broad line of Linear and Interface Integrated Circuit products. Complete device specifications are provided in the form of **Data Sheets** which are categorized by product type into ten chapters for easy reference. **Selector Guides** by product family are provided in the beginning of each Chapter to enable quick comparisons of performance characteristics. A **Cross Reference** chapter lists Motorola nearest replacement and functional equivalent part numbers for other industry products.

A chapter is provided to illustrate **Package Outline** and includes information on Surface Mount Devices (SMD).

Additionally, chapters are provided with information on **Quality** program concepts, high-reliability processing, and abstracts of available **Technical Literature**.

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.

Series H
First Printing

Printed in U.S.A.

New Product Literature

Chapter 2 has an addendum providing applications information on operational amplifiers.

The applications information which formerly appeared in the *Motorola Linear/Switchmode Voltage Regulator Handbook* (HB206) is now included as an addendum to Chapter 3.

An addendum covering RF applications information has been added to Chapter 8.

The Surface Mount Technology in Chapter 12 has been expanded to include Multiple Package Quantity (MPQ) information for surface mount and TO-92 packages shipped in Tape and Reel or Ammo Pack Styles. Mechanical Polarization drawings for the TO-92 (TO-226AA) in tape and reel plus the ammo pack styles have also been added to Chapter 12.

Data Classification

Product Preview

This heading on a data sheet indicates that the device is in the formative stages or in design (under development). The disclaimer at the bottom of the first page reads: "This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice."

Advance Information

This heading on a data sheet indicates that the device is in sampling, pre-production, or first production stages. The disclaimer at the bottom of the first page reads: "This document contains information on a new product. Specifications and information herein are subject to change without notice."

Fully Released

A fully released data sheet contains neither a classification heading nor a disclaimer at the bottom of the first page. This document contains information on a product in full production. Guaranteed limits will not be changed without written notice to your local Motorola Semiconductor Sales Office.

Index and Cross Reference

In Brief . . .

Motorola linear and interface integrated circuits cover a much broader range of products than the traditional op amps, regulators and consumer-image associated with linear suppliers. Linear circuit technology currently influences the design and architecture of equipment for all major markets. As with other integrated circuit technologies, linear circuit design techniques and processes have been continually refined and updated to meet the needs of these diversified markets.

Operational amplifiers have utilized JFET inputs for improved performance, plus innovative design and trimming concepts have evolved for improved high performance and precision characteristics. In linear power ICs, basic voltage regulators have been refined to include higher current levels and more precise three-terminal fixed and adjustable voltages. The power area continues to expand into switching regulators, power supply control and supervisory circuits, and motor controllers.

Linear designs also offer a wide array of line drivers, receivers and transceivers for many of the EIA, European, IEEE and IBM interface standards. Peripheral drivers for a variety of devices are also offered. In addition to these key interface functions, a variety of magnetic and semiconductor memory read, write, sense and RAM control circuits are also available.

In data conversion, the original A-D and D-A converters have been augmented with high performance video speed and multiplying designs. Linear circuit technology has also provided precision low voltage references for use in data conversion and other low temperature drift applications.

A host of special purpose linear devices have also been developed. These circuits find applications in telecommications, radio, television, automotive, RF communications, and data transmission. These products have reduced the cost of RF communications, and have provided capabilities in telecommunications which make the telephone line convenient for both voice and data communications. Linear developments have also reduced the many discrete components formerly required for consumer functions to a few IC packages, and have made significant contributions to the rapidly growing market for electronics in automotive applications.

The table of contents provides a perspective of the many markets served by linear/interface ICs and of Motorola's involvement in these areas.

Alphanumeric Index

Alphanumeric Index (continued)

*See *Telecommunication Device Data* (DL136)

Alphanumeric Index (continued)

*See *Telecommunication Device Data* (DL136)

Alphanumeric Index (continued)

Cross Reference

The following table represents a cross reference guide for all of Analog devices which are manufactured by Motorola. Where the Motorola part number differs from the industry part number, the Motorola device is a "form, fit and function" replacement for the industry part number. However, some differences in characteristics and/or specifications may exist.

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
55110DM		MC75S110L
75107ADC	MC75107L	
75107APC	MC75107P	
75107BDC		MC75107L
75107BPC		MC75107P
75108ADC	MC75108L	
75108APC	MC75108P	
75108BDC		MC75108L
75108BPC		MC75108P
75110DC	MC75S110L	
75110PC	MC75S110P	
75207DC		MC75107L
75207PC		MC75108P
75208DC		MC75108L
75208PC		MC75108P
8216		MC8T26AL
9614DC		MC75S110L
9614DM		MC75S110L
9615DC		MC75108L
9616CDC		MC1488L
9616DM		MC1488L
90616EDC		MC1488L
9617DC		MC1489AL
9620DC		MC75S110L
9620DM		MC75S110L
9621DC		MC75108L
9627DC		MC1489AL
9627DM		MC1489AL
9636AT	MC3488AP	
9637T		MC3486P
9638T		MC3487P
9640DC	MC26S10L	
9640PC	MC26S10P	
9665DC	MC1411L	
9665PC	MC1411P	
9666DC	MC1412L	
9666PC	MC1412P	
9667DC	MC1413L	
9667PC	MC1413P	
9668DC	MC1416L	
9668PC	MC1416P	
AD1403AN		MC1403AU
AD1508-8D	MC1508L8	
AD530		MC1595L
AD531		MC1595L
AD532L		MC1595L
AD580J		MC1403U
AD580K		MC1403P1
AD580M		MC1403AP1
AD580S		MC1503U
AD580T		MC1503AU
AD589J		LM385Z-1.2
AD589K		LM385Z-1.2
AD589L		LM385Z-1.2
AD589M		LM385BZ-1.2
ADDAC-08CQ	DAC-08CQ	
ADDAC-08ED	DAC-08EQ	

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
ADDAC-08HD	DAC-08HQ	
AM107	LM111J	
AM201AD		LM201AN
AM201D		LM201AN
AM26LS30D	AM26LS30D	
AM26LS30L	AM26LS30L	
AM26ALS30P	AM26LS30P	
AM26LS31CJ	AM26LS31PC	
AM26LS31CN	AM26LS31PC	
AM26LS31DS	AM26LS31DS	
AM26LS31P	AM26LS31P	
AM26LS32ACJ	AM26LS32D	
AM26LS32ACN	AM26LS32APC	
AM26LS32PC	AM26LS32PC	
AM26LS32P	AM26LS32PC	
AM26LS33DC		MC3486L
AM26LS33PC		MC3486P
AM26S10DC	MC26S10L	
AM301AD		LM301AJ
AM301D		LM301AJ
AM311D	LM311J-8	
AM723DC	MC1723CL	
AM723DM	MC1723L	
AM723P	MC1723CP	
AM741DC		MC1741CU
AM741DM		MC1741U
AM747DC	MC1747CL	
AM747DM	MC1747L	
AN5150		MC34129P
AN5151		MC13001P
CA081AE		TL081ACP
CA081AS		TL081ACJG
CA081CS		TL081CJG
CA081E		TL081CP
CA081S		TL081MJG
CA082AE		TL082ACP
CA082AS		TL082ACJG
CA082CS		TL082CJG
CA082E		TL082CP
CA082S		TL082MJG
CA084AE		TL084ACN
CA084E		TL084CN
CA084S		TL084MJ
CA1391E	MC1391P	
CA139AG	LM139AJ	
CA139G	LM139J	
CA1458S	MC1458CP1	
CA1558S		MC1558U
CA239AE	LM239AN	
CA239AG	LM239AJ	
CA239E	LM239N	
CA239G	LM239J	
CA3026		CA3054
CA3045F		MC3346P
CA3045		MC3346P
CA3046	MC3346P	
CA3048		MC3301P

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
CA3052		MC3301P
CA3054	CA3054	
CA3058		CA3059
CA3059	CA3059	
CA3079	CA3079	
CA3085AF		MC1723L
CA3086F		MC3346P
CA308AS	LM308N	
CA3091D		MC1594L
CA3136A		MC3346P
CA3146D		CA3146D
CA3146		MC3346P
CA3201E		TDA3301B
CA3210E		MC13001P
CA3217E		TDA3301B
CA3302E	MC3302N	
CA339AE	LM339AN	
CA339AG	LM339AJ	
CA339E	LM339N	
CA339G	LM339J	
CA3401E	MC3401P	
CA723CE	MC1723CP	
CA723E	MC1723L	
CA741CS	MC1741CP1	
CA741S	MC1741U	
CA747CE	MC1747CL	
CA747CF	MC1747CL	
CA747E	MC1747L	
CA747F	MC1747L	
CA748CS	MC1748CP1	
CS2842AD	UC2842BD1	
CS2843AD	UC2843BD1	
CS2844D	UC2844BD1	
CS2845D	UC2845BD1	
CS3471	MC3471P	
CS3842AD	UC3842BD1	
CS3843AD	UC3843DB1	
CS3844D	UC3844BD1	
CS3845D	UC3845BD1	
D8216		MC8T26AL
D8226		MC8T26L
DAC-08CD	DAC-08CD	
DAC-08CN		DAC-08CP
DAC-08CP	DAC-08CP	
DAC08CQ	DAC-08CQ	
DAC-08ED	DAC-08ED	
DAC-08EN		DAC-08EP
DAC-08EP	DAC-08EP	
DAC-08EQ	DAC-08EQ	
DAC-08HN		DAC-08HP
DAC-08HP	DAC-08HP	
DAC-08HQ	DAC-08HQ	
DAC0800LCJ	DAC-08EQ	
DAC0800LCN	DAC-08EP	
DAC0801LCJ	DAC-08CQ	
DAC0801LCN	DAC-08CP	
DAC0802LCJ	DAC-08HQ	
DAC0802LCN	DAC-08HP	
DAC0808LCJ	MC1408L8	
DAC0808LCN	MC1408P8	
DAC0808LD	MC1508L8	

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
DM7822J		MC1489AL
DM7837J		MC3437L
DM8822J		MC1489AL
DM8822N		MC1489AP
DM8837N	MC3437P	
DS1488J	MC1488L	
DS1488N	MC1488P	
DS1489AJ	MC1489AL	
DS1489AN	MC1489AP	
DS1489J	MC1489L	
DS1489N	MC1489P	
DS26LS31N	AM26LS31P	
DS26LS32N	AM26LS32P	
DS26S10CJ	MC26S10L	
DS26S10CN	MC26S10P	
DS3486J	MC3486L	
DS3486N	MC3486P	
DS3487J	MC3487L	
DS3487N	MC3487P	
DS3612H		MC1472U
DS3612N		MC1472P1
DS3632H	MC1472U	
DS3632J	MC1472U	
DS3632N	MC1472P1	
DS3650J	MC3450L	
DS3650N	MC3450P	
DS3651J	MC3430L	
DS3651N	MC3430P	
DS3652J	MC3452L	
DS3652N	MC3452P	
DS3653J	MC3432L	
DS3653N	MC3432P	
DS55107W		MC75107L
DS55110J		MC75S110L
DS75107J	MC75107L	
DS75107N	MC75107P	
DS75108J	MC75108L	
DS75108N	MC75108P	
DS75110J	MC75S110L	
DS75110N	MC75S110P	
DS75207J		MC75107L
DS75207N		MC75107P
DS75208J		MC75108L
DS75208N		MC74108P
DS7837J		MC3437L
DS7837W		MC3437L
DS8834J		MC8T26AL
DS8834N		MC8T26AP
DS8835J		MC8T26AL
DS8835N		MC8T26AP
DS8837J	MC3437L	
DS8837N	MC3437P	
DS8922A		MC34051P
DS8923A		MC34050P
DS9636ACN	MC3488AP1	
ICL741CLNPA		MC1741CP1
ICL741CLNTY		MC1741CP1
ICL8001CTZ		LM111J
ICL8001MTZ		LM111J
ICL8008CPA		LM301AN
ICL8808CTY		LM301AN

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
ICL8013A		MC1594L
ICL8013B		MC1594L
ICL8013C		MC1594L
ICL8017CTW		LM301AN
ICL8017MTW		LM301AN
ICL8069CCZR		LM384BZ-1.2
ICL8069DCZR		LM385BZ-1,2
IP33063N	MC33063AP1	
IP34060AN	MC34060AP	
IP34063N	MC34063AP1	
IP35063J	MC35063AU	
IP3525AJ	SG3525AJ	
IP3525AN	SG3525AN	
IP3526J	SG3526J	
IP3526N	SG3526N	
IP3527AJ	SG3527AJ	
IP3527AN	SG3527AN	
IP494ACJ		TL594IN
IP494ACN		TL594CN
IP494AJ		TL594MJ
ITT3710		MC1391P
ITT652	MC1411P	
ITT654	MC1412P	
ITT656	MC1413P	
L144AP		LM324N
L201	MC1411P	
L202	MC1412P	
L203	MC1413P	
L387		MC33267
L583		MC3484S2
LF347BN	LF347BN	
LF347N	LF347N	
LF351AN		MC34001AP
LF351BN		MC34001BP
LF351N	LF351N	
LF352D		LF355J
LF353AN	MC34002AP	
LF353BN	MC34002BP	
LF353D	LF353D	
LF353N	LF353N	
LF356BJ	LF356BJ	
LF356BN		LF356J
LF356JG		LF356J
LF356J	LF356J	
LF356N		LF356J
LF356P		LF356J
LF357BJ	LF357BJ	
LD357BN		LF357BJ
LD357JG		LF357J
LF357J	LF357J	
LF357N		LF357J
LF357P		LF357J
LF411CD	LF411CD	
LF411CH		MC34001AG
LF412CD	LF411CD	
LF412CH		MC34002AG
LF441CD	LF441CD	
LF441CN	LF441CN	
LF442CD	LF442CD	
LF442CN	LF442CN	

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
LF444CD	LF444CD	
LF444CN	LF444CN	
LF351AN		MC34001AP
LM101AJ-14		LM101AJ
LM101AJG	LM101AJ	
LM101AJ	LM101AJ	
LM101D		LM101AJ
LM101J-14		LM101AJ
LM1035		TCA5550
LM107L	MC1741L	
LM111J-8	LM111J-8	
LM111JG	LM111J-8	
LM11CLN	LM11CLN	
LM11CN	LM11CN	
LM124AD		LM124J
LM124AJ		LM124J
LM124J	LM124J	
LM124N	LM124N	
LM139AJ	LM139AJ	
LM139J	LM139J	
LM139N	MC1391P	
LM1408J8		MC1408L8
LM1408N8		MC1408P8
LM1489AN	MC1489AP	
LM1489J	MC1489L	
LM1489N	MC1489P	
LM1496J	MC1496L	
LM1496N	MC1496P	
LM149J		MC4741L
LM158JG		LM158J
LM158J	LM158J	
LM1558J	MC1558U	
LM1596J	MC1596L	
LM163J		MC3450L
LM1849A		MC3484S2
LM1889		MC1374P
LM1900D		MC3301P
LM1981		MC13020P
LM201AD	LM201AD	
LM201AJ-14		LM201AJ
LM201AJG	LM201AJ	
LM201AJ	LM201AJ	
LM201AN	LM201AN	
LM201AP		LM201AN
LM201J-14		LM201AJ
LM201J	LM201AJ	
LM211D	LM211D	
LM211J-8	LM211J-8	
LM211JG	LM211J-8	
LM211M	LM211D	
LM212H		MC1456U
LM224AF		LM224J
LM224AJ		LM224J
LM224D	LM224D	
LM224J	LM224J	
LM224M	LM224D	
LM224N	LM224N	
LM239AJ	LM239AJ	
LM239AN	LM239AN	
LM239D	LM239D	

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
LM239J	LM239J	
LM239M	LM239D	
LM239N	LM239N	
LM240LAZ-12		MC78L12ACP
LM240LAZ-15		MC78L15ACP
LM240LAZ-18		MC78L18ACP
LM240LAZ-24		MC78L24ACP
LM240LAZ-5.0		MC78L05ACP
LM204LAZ-6.0		MC78L05ACP
LM240LAZ-8.0		MC78L08ACP
LM248J	LM248J	
LM248N	LM248N	
LM249J		MC4741L
LM249N		MC4741P
LM258D	LM258D	
LM258J	LM258J	
LM258M	LM258D	
LM258N	LM258N	
LM285Z-1.2	LM258Z-1.2	
LM285Z-2.5	LM258Z-2.5	
LM2900N	LM2900N	
LM2901D	LM2901D	
LM2901M	LM2901D	
LM2901N	LM2901N	
LM2902D	LM2902D	
LM2902J	LM2902J	
LM2902M	LM2902D	
LM2902N	LM2902N	
LM2903D	LM2903D	
LM2903M	LM2903D	
LM2903N	LM2903N	
LM2903P	LM2903N	
LM2904J	LM2904J	
LM2904M	LM2904D	
LM2904N	LM2904N	
LM2905N		MC1455P1
LM2931ACT	LM2931ACT	
LM2931AD-5.0	LM2931AD-5.0	
LM2931AT-5.0	LM2931AT-5.0	
LM2931AZ-5.0	LM2931AZ-5.0	
LM2931CD	LM2931CD	
LM2931CM	LM2931CD	
LM2931CT	LM2931CT	
LM2931D-5.0	LM2931D-5.0	
LM2931D	LM2931D	
LM2931T-5.0	LM2931T-5.0	
LM2931Z-5.0	LM2931Z-5.0	
LM2935T	MC2935T	
LM293D	LM293D	
LM301AD	LM301AD	
LM301AJG	LM301AJ	
LM301AJ	LM301AJ	
LM301AM	LM301AD	
LM301AN	LM301AN	
LM301AP		LM301AN
LM3026		CA3054
LM3045		MC3346P
LM3046N	MC3346P	
LM3054	CA3054	
LM307N	LM307N	
LM307P		LM307N

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
LM3089		MC3356P
LM311D	LM311D	
LM311J-8	LM311J-8	
LM331JG	LM311J-8	
LM311M	LM311D	
LM311N-14		LM311J-8
LM311N	LM311N	
LM311P	LM311N	
LM3146A		MC3346P
LM3146		MC3346P
LM317KC	LM317T	
LM317KD		LM317T
LM317LD	LM317LD	
LM317LZ	LM317LZ	
LM317MP		LM317MT
LM317P		LM317T
LM317T	LM317T	
LM3189		MC3356P
LM320LZ-12		MC79L12ACP
LM320LZ-15		MC79L15ACP
LM320LZ-5.0		MC79L05ACP
LM320MP-12		MC7912CT
LM320MP-15		MC7915CT
LM320MP-18		MC7918CT
LM320MP-24		MC7924CT
LM320MP-5.0		MC7905CT
LM320MP-5.2		MC7905.2CT
LM320MP-6.0		MC7906CT
LM320MP-8.0		MC7908CT
LM320T-12		MC7912CT
LM320T-15		MC7915CT
LM320T-5.0		MC7905CT
LM320T-5.2		MC7905.2CT
LM322N		MC1455P1
LM323AT	LM323AT	
LM323T	LM323T	
LM324AD	LM324AD	
LM324AJ		LM324J
LM324AN	LM324AN	
LM324D	LM324D	
LM324J	LM324J	
LM324M	LM324D	
LM324N	LM324N	
LM325AN		MC1468L
LM325N		MC1468L
LM326N		MC1468L
LM328AN		MC1468L
LM328N		MC1468L
LM3301N	MC3301L	
LM3302J	MC3302L	
LM3302N	MC3302P	
LM337MP		LM337MT
LM337MT	LM337MT	
LM337T	LM337T	
LM339AD	LM339AD	
LM339AJ	LM339AJ	
LM339AM	LM339AD	
LM339AN	LM339AN	
LM339D	LM339D	
LM339J	LM339J	
LM339N	LM339N	

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
LM339P		LM339N
LM3401N	MC3401P	
LM340AT-12	LM340AT-12	
LM340AT-15	LM340AT-15	
LM340AT-5.0	LM340AT-5.0	
LM340KC-12	LM340T-12	
LM340KC-15	LM340T-15	
LM340LAZ-12		MC78L12ACP
LM340LAZ-18		MC78L18ACP
LM340LAZ-24		MC78L24ACP
LM340LAZ-5.0		MC78L05ACP
LM340LAZ-8.0		MC78L08ACP
LM340T-12	LM340T-12	
LM340T-15	LM340T-15	
LM340T-18	LM340T-18	
LM340T-24	LM340T-24	
LM340T-5.0	LM340T-5.0	
LM340T-6.0	LM340T-6.0	
LM340T-8.0	LM340T-8.0	
LM341P-12		MC78M12CT
LM341P-15		MC78M15CT
LM341P-18		MC78M18CT
LM341P-24		MC78M24CT
LM341P-5.0		MC78M05CT
LM341P-6.0		MC78M06CT
LM341P-8.0		MC78M08CT
LM342P-12		MC78M12CT
LM342P-15		MC78M15CT
LM342P-18		MC78M18CT
LM342P-24		MC78M24CT
LM342P-5.0		MC78M05CT
LM342P-6.0		MC78M06CT
LM342P-8.0		MC78M08CT
LM348D	LM348D	
LM348J	LM348J	
LM348M	LM348D	
LM348N	LM348N	
LM349J		MC4741CL
LM349N		MC4741CP
LM350T	LM350T	
LM358AN		LM358N
LM358D	LM358D	
LM358JG	LM358J	
LM358J	LM358J	
LM358M	LM358D	
LM358N	LM358N	
LM363AJ		MC3450L
LM363AN		MC3450P
LM363J		MC3450L
LM363N		MC3450P
LM385BZ-1.2	LM385BZ-1.2	
LM385BZ-2.5	LM385BZ-2.5	
LM385D-1.2	LM385D-1.2	
LM385D-2.5	LM385D-2.5	
LM385M-1.2	LM385D-1.2	
LM385M-2.5	LM385D-2.5	
LM385Z-1.2	LM385Z-1.2	
LM385Z-2.5	LM385Z-2.5	
LM386N		MC34119P
LM3900D	LM3900D	
LM3900J	LM3900J	

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
LM3900N	LM3900N	
LM3905N		MC1455P1
LM393AN	LM393AN	
LM393D	LM393D	
LM393JG		LM393N
LM393M	LM393D	
LM393N	LM393N	
LM4250CN		MC1776CP1
LM55109J		MC75S110L
LM55110J		MC75S110L
LM555CN	MC1455P1	
LM556CD	MC3456L	
LM556CJ	MC3456L	
LM556CN	MC3456P	
LM556L	MC3456L	
LM703LN		MC1350P
LM723CD	MC1723CL	
LM723CJ	MC1723CL	
LM723CN	MC1723CP	
LM723J	MC1723L	
LM741CD	MC1741CL	
LM741CJ-14	MC1741CL	
LM741EJ		MC1741CU
LM741EN		MC1741CP1
LM747CD	MC1747CL	
LM748CN	MC1748CP1	
LM75107AN	MC75107P	
LM75108AJ	MC75108L	
LM75108AN	MC75108P	
LM75110J	MC75S110L	
LM75110N	MC75S110P	
LM75207L		MC75107L
LM75207N		MC75107P
LM75208J		MC75108L
LM75208N		MC75108P
LM7805CT	MC7805CT	
LM7812CT	MC7812CT	
LM7815CT	MC7815CT	
LM78L05ACZ	MC78L05ACP	
LM78L05CZ	MC78L05CP	
LM78L08ACZ	MC78L08ACP	
LM78L08CZ	MC78L08CP	
LM78L12ACZ	MC78L12ACP	
LM78L12CZ	MC78L12CP	
LM78L15ACZ	MC78L15ACP	
LM78L15CZ	MC78L15CP	
LM78L18ACZ	MC78L18ACP	
LM78L18CZ	MC78L18CP	
LM78L24ACZ	MC78L24ACP	
LM78L24CZ	MC78L24CP	
LM78M06CP		MC78M05CT
LM78M12CP		MC78M12CT
LM78M15CP		MC78M15CT
LM7905CT	MC7905CT	
LM7912CT	MC7912CT	
LM7915CT	MC7915CT	
LM79L05ACZ	MC79L05ACP	
LM79L12ACZ	MC79L12ACP	
LM79L15ACZ	MC78L15ACP	
LM79M05CP		MC79M05CT
LM79M12CP		MC79M12CT

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
LM79M15CP		MC79M15CT
LM833D	LM833D	
LM833N	LM833N	
LM833P	LM833N	
LM837N		MC33079P
LMC6482D		MC33202D
LMC6482P		MC33202P
LMC6484D		MC33204D
LMC6484P		MC33204P
LT1083		MC34268
MB3759	TL494CN	
MP5531CP	MC1404U5	
MP5531DP	MC1404U5	
MP5532CP	MC1404U10	
MP5532DP	MC1404U10	
N5558F	MC1458U	
N5558V	MC1458P1	
N5595A	MC1495L	
N5595F	MC1495L	
N5596A	MC1496L	
N5723A		MC1723CP
N5741A		MC1741CP1
N5741V	MC1741CP1	
N5747A	MC1747CL	
N5747F	MC1747CL	
N8T15A		MC1488L
N8T15F		MC1488L
N8T16A		MC1489L
N8T26AB	MC8T26AP	
N8T26AE	MC8T26AL	
N8T26AJ	MC8T26AL	
N8T26AN	MC8T26AP	
N8T26B	MC8T26AP	
N8T26J	MC8T26AL	
N8T26N	MC8T26AP	
N8T37A	MC3437P	
N8T97B	MC8T97P	
N8T97F	MC8T97L	
N8T97N	MC8T97P	
N8T98B	MC8T98P	
N8T98F	MC8T98L	
N8T98N	MC8T98P	
NE550A		MC1723CP
NE555JG	MC1455U	
NE555D	MC1455D	
NE555V	MC1455P1	
NE556D	NE556D	
NE556F	MC3456L	
NE5561FE		MC34060AL
NE5561N		MC34060P
NE5234D		MC33204D
NE5234P		MC33204P
OP-01P		MC1436P1
PWM125CK	SG3525AJ	
RC1458DN	MC1458P1	
RC1488DC	MC1488L	
RC1489ADC	MC1489AL	
RC1489DC	MC1489L	
RC3302DB	MC3302P	
RC4136DP		MC3403P
RC4136D		MC3403L

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
RC4136J		MC3403L
RC4136N		MC3403P
RC4194DC		MC1468L
RC4195NB		MC1468L
RC4558DN	MC4558CP1	
RC4558JG	MC4558CU	
RC4458P	MC4558CP1	
RC723DB	MC1723CP	
RC723DC	MC1723CL	
RC723D	MC1723CL	
RC741DN	MC1741CP1	
RC747D	MC1747CL	
RC75107ADP	MC75107P	
RC75107AD	MC75107L	
RC75108ADP	MC75108P	
RC75108AD	MC75108L	
RC75109DP		MC75S110P
RC75109D		MC75S110L
RC75110DP	MC75S110P	
RC75110D	MC75S110L	
REF-01CJ		MC1404U10
REF-01CP	MC1404U10	
REF-01CZ	MC1404U10	
REF-01DJ		MC1404U10
REF-01DP	MC1404U10	
REF-01DZ	MC1404U10	
REF-02CJ		MC1404U5
REF-02CP	MC1404U5	
REF-02CZ	MC1404U5	
REF-02DJ		MC1404U5
REF-02DP	MC1404U5	
REF-02DZ	MC1404U5	
RM4136D		MC3503L
RM4136J		MC3503L
RM4194DC		MC1568L
RM4558D	MC4558U	
RM4558JG	MC4558U	
RM723DC	MC1723L	
RM723D	MC1723L	
RM741DP	MC1741L	
RM747D	MC1747L	
RV3301DB	MC3301P	
S5558E	MC1558U	
S5596F	MC1596L	
SA555N	MC1455BP1	
SAA1042A		SAA1042AV
SAA1042		SAA1042V
SG107J		MC1741L
SG107T		MC1741L
SG111D	LM111J	
SG124J	LM124J	
SG1402N		MC1594L
SG1402T		MC1594L
SG1436M	MC1436U	
SG1458M	MC1458P1	
SG1468J	MC1468L	
SG1468N		MC1468L
SG1495D	MC1495L	
SG1495N		MC1495L
SG1496D	MC1496L	
SG1496N	MC1496P	

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
SG1501AD		MC1568L
SG1501AJ		MC1568L
SG1501AJ	MC1568L	
SG1502D		MC1568L
SG1502J		MC1568L
SG1502N		MC1568L
SG1503T		MC1503U
SG1503Y		MC1503U
SG1524J		TL494MJ
SG1568J	MC1568L	
SG1595D	MC1595L	
SG1596D	MC1596L	
SG201AM	LM201AN	
SG201AN		LM201AN
SG201M	LM201AN	
SG201N		LM201AN
SG211D	LM211J-8	
SG211M	LM211J-8	
SG224J	LM224J	
SG224N	LM224N	
SG2402N		MC1494L
SG2402T		MC1494L
SG2501AD		MC1468L
SG2501D	MC1468L	
SG2501J		MC1468L
SG2501N		MC1468L
SG2502J		MC1468L
SG2502N		MC1468L
SG2503M		MC1403AU
SG2503T		MC1403AU
SG2503Y		MC1403AU
SG300N		MC1723CP
SG301AM	LM301AN	
SG301AN		LM301AN
SG307J		LM307N
SG307M	LM307N	
SG307N		LM307N
SG308AM	LM308AN	
SG311D	LM311J	
SG311M	LM311N	
SG317P	LM317T	
SG317R		LM317T
SG324J	LM324J	
SG324N	LM324N	
SG337P	LM337T	
SG337R		LM337T
SG3402N		MC1494L
SG3402T		MC1494L
SG3423M		MC3423P1
SG3423Y		MC3423U
SG3501AD		MC1468L
SG3501AJ		MC1468L
SG3501AN		MC1468L
SG3501D		MC1468L
SG3501J		MC1468L
SG3501N		MC1468L
SG3502D		MC1468L
SG3502J		MC1468L
SG3502N		MC1468L
SG3503M		MC1403U
SG3503T		MC1403U

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
SG3503Y	MC1403U	
SG3523Y		MC3523U
SG3524J		TL494CJ
SG3525AJ	SG3525AJ	
SG3525AN	SG3525AN	
SG3526J	SG3526J	
SG3526N	SG3526N	
SG3527AJ	SG3527AJ	
SG3527AN	SG3527AN	
SG3561	MC34261	
SG4194CJ		MC1468L
SG4194J		MC1568L
SG4250CM		MC1775CP1
SG4501D	MC1468L	
SG4501J		MC1468L
SG4501N		MC1468L
SG555CM	MC1455P1	
SG556CJ		MC3456L
SG556CN	MC3456P	
SG556J	MC3456L	
SG723CD		MC1723CL
SG723CJ	MC1723CL	
SG723CN	MC1723CP	
SG723D		MC1723L
SG723J	MC1723L	
SG741CM	MC1741CP1	
SG747CJ	MC1747CL	
SG747CN	MC1747CP2	
SG747J	MC1747L	
SG748CD		MC1748CP1
SG748CM		MC1748CP1
SG748CN		MC1748CP1
SG777CN		LM308AN
SG7805ACP	MC7805ACT	
SG7805ACR		MC7805ACT
SG7805ACT		MC7805ACT
SG7805CP	MC7805CT	
SG7806ACP	MC7806ACT	
SG7806ACR		MC7806ACT
SG7806ACT		MC7806ACT
SG7806CP	MC7806CT	
SG7806CR		MC7806CT
SG7808ACP	MC7808ACT	
SG7808ACT		MC7808ACT
SG7808CP	MC7808CT	
SG7808CR		MC7808CT
SG7812ACP	MC7812ACT	
SG7812ACR		MC7812ACT
SG7812ACT		MC7812ACT
SG7812CP	MC7812CT	
SG7812CR		MC7812CT
SG7815ACP	MC7815ACT	
SG7815ACR		MC7815ACT
SG7815ACT		MC7815ACT
SG7815CP	MC7815CT	
SG7815CR		MC7815CT
SG7815CT		MC7815CT
SG7818ACP	MC7818ACT	
SG7818ACR		MC7818ACT
SG7818ACT		MC7818ACT
SG7818CP	MC7818CT	

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
SG7818CR		MC7818CT
SG7824ACP	MC7824ACT	
SG7824ACR		MC7824ACT
SG7824ACT		MC7824ACT
SG7824CP	MC7824CT	
SG7824CR		MC7824CT
SG7905.2CP	MC7905.2CT	
SG7905.2CR		MC7905.2CT
SG7905.2CT		MC7905.2CT
SG7905ACP	MC7905ACT	
SG7905ACR		MC7905ACT
SG7905ACT		MC7905ACT
SG7905CP	MC7905CT	
SG7905CR		MC7905CT
SG7905CT		MC7905CT
SG7908CP	MC7908CT	
SG7908CR		MC7908CT
SG7908CT		MC7908CT
SG7912ACP	MC7912ACT	
SG7912ACR		MC7912ACT
SG7912ACT		MC7912ACT
SG7912CP	MC7912CT	
SG7912CR		MC7912CT
SG7912CT		MC7912CT
SG7915ACP	MC7915ACT	
SG7915ACR		MC7915ACT
SG7915ACT		MC7915ACT
SG7915CP	MC7915CT	
SG7915CR		MC7915CT
SG7915CT		MC7915CT
SG7918CP	MC7918CT	
SH8090FM		MC1508L8
SN75107AJ	MC75107L	
SN75107AN	MC75107P	
SN75107BJ		MC75107L
SN75107BN		MC75107P
SN75108AJ	MC75108L	
SN75108AN	MC75108P	
SN75108BJ		MC75108L
SN75108BN		MC75108P
SN75110AJ	MC75S110L	
SN75110AN	MC75S110P	
SN75121J		MC3481/5L
SN75121N		MC3481/5P
SN75125N		MC3481/5L
SN75126J		MC3481/5L
SN75126N		MC3481/5P
SN75150J		MC1488L
SN75150N		MC1488P
SN75154J		MC1489L
SN75154N		MC1489P
SN75160J		MC3447L
SN75160N		MC3447P/P3
SN75172N	MC75172BP	
SN75173J	SN75173J	
SN75173N	SN75173N	
SN75174N	MC75174BP	
SN75175J	SN75175J	
SN75175N	SN75175N	
SN75188J	MC1488L	
SN75188N	MC1488P	

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
SN75189AJ	MC1489AL	
SN75189AN	MC1489AP	
SN75189J	MC1489L	
SN75189N	MC1489P	
SN75207J		MC75107L
SN75207N		MC75107P
SN75208J		MC75108L
SN75208N		MC75108P
SN75251N		MC3471P
SN75466J	MC1411L	
SN75466N	MC1411P	
SN75467J	MC1412L	
SN75467N	MC1412P	
SN75468J	MC1413L	
SN75468N	MC1413P	
SN75475JG	MC1472U	
SN75475P	MC1472P1	
SN76514N	MC1496P	
SN76591P	MC1391P	
SN76600P	MC1350P	
SSS140BA-8Z	MC1408L8	
SSS150BA-8Z	MC1508L8	
SSS201AP	LM201AN	
SSS301AP	LM301AN	
SSS747BP		MC1747L
SSS747CP		MC1747CL
SSS747GP		MC1747L
SSS747P		MC1747L
TA7179P	MC1468L	
TA7504P	MC1741CP1	
TA7506P	LM301AN	
TA75071P		MC34001P
TA75072P		MC34002P
TA75074F		MC34004P
TA75339F	LM339D	
TA75339P	LM339N	
TA75358CF	LM358D	
TA75358CP	LM358N	
TA75393F	LM393D	
TA75393P	LM393N	
TA75458F	MC1458D	
TA75458P	MC1458CP1	
TA75558P	MC4558CP1	
TA7555F	MC1455D	
TA7555P	MC1455P1	
TA75902F	LM324D	
TA76494P		TL494IN
TA78005AP	MC7805CT	
TA78006AP	MC7806CT	
TA78008AP	MC7808CT	
TA78012AP	MC7812CT	
TA78015AP	MC7815CT	
TA78018AP	MC7818CT	
TA78024AP	MC7824CT	
TA78L005AP		MC78L05ACP
TA78L005P		MC78L05CP
TA78L008AP		MC78L08ACP
TA78L008P		MC78L08CP
TA78L012AP		MC78L12ACP
TA78L012P		MC78L12CP
TA78L015AP		MC78L15ACP

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
TA78L015P		MC78L15CP
TA78L018AP		MC78L18ACP
TA78L018P		MC78L18CP
TA78L024AP		MC78L24ACP
TA78L024P		MC78L24CP
TA78M05P	MC78M05CT	
TA78M06P	MC78M06CT	
TA78M08P	MC78M08CT	
TA78M12P	MC78M12CT	
TA78M18P	MC78M18CT	
TA78M20P	MC78M20CT	
TA78M24P	MC78M24CT	
TA79005P	MC7905CT	
TA79006P	MC7906CT	
TA79008P	MC7908CT	
TA79012P	MC7912CT	
TA79015P	MC7915CT	
TA79018P	MC7918CT	
TA79024P	MC7924CT	
TA79L005P		MC79L05CP
TA79L012P		MC79L12P
TA79L015P		MC79L15P
TA79L018P		MC79L18P
TA79L024P		MC79L24P
TB920		MC1391P
TBA920S		MC1391P
TCA5600	TCA5600	
TCF5600	TCF5600	
TD62001P/AP	MC1411P	
TD62002P/AP	MC1412P	
TD62003P/AP	MC1413P	
TD62477P	MC1472P	
TD62479P	MC1374P	
TDA1085A	TDA1085A	
TDA1085C	TDA1085C	
TDA1085	TDA1085C	
TDA1185A	TDA1185A	
TDA3301B	TDA3301B	
TDA4817	MC34261	
TDC1048		MC10319P
TLC2272D		MC33202D
TLC2272P		MC33202P
TLC2274D		MC33204D
TLC2274P		MC33204P
TL022CJG		LM358J
TL022CP		LM358N
TL022MJG		LM158J
TL044CJ		LM324N
TL044MJ		LM124J
TL062ACP	TL062ACP	
TL062CD	TL062CD	
TL062CP	TL062CP	
TL062MJG	TL062MJG	
TL062VP	TL062VP	
TL064ACD	TL064ACD	
TL064ACN	TL064ACN	
TL064CD	TL064CD	
TL064CN	TL064CN	
TL064MJ	TL064MJ	
TL064VN	TL064VN	
TL071ACD	TL071ACD	

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
TL071ACJG	TL071ACJG	
TL071ACP	TL071ACP	
TL071CD	TL071CD	
TL071CJG	TL071CJG	
TL071CP	TL071CP	
TL071MJG	TL071MJG	
TL072ACD	TL072ACD	
TL072ACJG	TL072ACJG	
TL072ACP	TL072ACP	
TL072CD	TL072CD	
TL072CJG	TL072CJG	
TL072CP	TL072CP	
TL072MJG	TL072MJG	
TL074ACJ	TL074ACJ	
TL074ACN	TL074ACN	
TL074CJ	TL074CJ	
TL074CN	TL074CN	
TL074MJ	TL074MJ	
TL081ACD	TL081ACD	
TL081ACJG	TL081ACJG	
TL081ACP	TL081ACP	
TL081CD	TL081CD	
TL081CJG	TL081CJG	
TL081CP	TL081CP	
TL081MJG	TL081MJG	
TL082ACJG	TL082ACJG	
TL082ACP	TL082ACP	
TL082CD	TL082CD	
TL082CJG	TL082CJG	
TL082CP	TL082CP	
TL082MJG	TL082MJG	
TL084ACJ	TL084ACJ	
TL084ACN	TL084ACN	
TL084CJ	TL084CJ	
TL084CN	TL084CN	
TL084MJ	TL084MJ	
TL1431		TL431
TL431CD	TL431CD	
TL431CJG	TL431CJG	
TL431CLP	TL431CLP	
TL431CP	TL431CP	
TL431IJG	TL431IJG	
TL431ILP	TL431ILP	
TL431IP	TL431IP	
TL431MJG	TL431MJG	
TL494CJ	TL494CJ	
TL494CN	TL494CN	
TL494IJ	TL494IJ	
TL494IN	TL494IN	
TL494MJ	TL494MJ	
TL497CJ		MC34063AU
TL497CN		MC34063AP1
TL497MJ		MC35063AU
TL594CN	TL594CN	
TL594IN	TL594IN	
TL594MJ	TL594MJ	
TL780-05CKC	TL780-05CKC	
TL780-12CKC	TL780-12CKC	
TL780-15CKC	TL780-15CKC	
TL7805ACKC	MC7805ACT	
µA0802DC-1	MC1408L8	

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
µA0802DC-2	MC1408L8	
µA0802DC-3	MC1408L8	
µA0802DM-1	MC1508L8	
µA0802PC-1	MC1408P8	
µA0802PC-2	MC1408P8	
µA0802PC-3	MC1408P8	
µA101AD		LM101AJ
µA101AF		LM101AJ
µA101D		LM101AJ
µA101F		LM101AJ
µA1391PC	MC1391P	
µA1458CP	MC1458CP1	
µA1458CRC	MC1458CU	
µA1458CTC	MC1458CP1	
µA1458P	MC1458P1	
µA1458RC	MC1458U	
µA1458TC	MC1458P1	
µA201AD		LM201AJ
µA201AF		LM201AJ
µA201D		LM201AJ
µA201F		LM201AJ
µA2240DC		MC1455U
µA2240PC		MC1455P1
µA301AD		LM301AJ
µA301AT	LM301AN	
µA3026HM		CA3054
µA3045		MC3346P
µA3046DC	MC3346P	
µA3054DC	CA3054P	
µA307T	LM307N	
µA311T	LM311N	
µA317UC	LM317T	
µA3301P	MC3301P	
µA3302P	MC3302P	
µA3303P	MC3303P	
µA3401P	MC3401P	
µA3403D	MC3403L	
µA3403P	MC3403P	
µA4136DC		MC4741CL
µA4136DM		MC4741L
µA4136PC		MC4741CP
µA431AWC	TL431CP	
µA4558TC	MC4558CP1	
µA494DC	TL494CJ	
µA494DM	TL494MJ	
µA494PC	TL494CN	
µA555TC	MC1455P1	
µA556DC	MC3456L	
µA556PC	MC3456P	
µA723CF	MC1723CL	
µA723CJ	MC1723CL	
µA723CN	MC1723CP	
µA723DC	MC1723CL	
µA723DM	MC1723L	
µA723F	MC1723L	
µA723MJ	MC1723L	
µA723PC	MC1723CP	
µA734DC		LM311J
µA734DM		LM311J
µA741ADM		MC1741L
µA741CJG	MC1741CU	

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
µA741CP	MC1741CP1	
µA741MJG	MC1741U	
µA741RC	MC1741CU	
µA741RM	MC1741U	
µA742DC		CA3059
µA747ADM		MC1747L
µA747CN	MC1747CP2	
µA747DC	MC1747CL	
µA747DM	MC1747L	
µA747EDC	MC1747CL	
µA747MJ	MC1747L	
µA747PC	MC1747CP2	
µA748CP	MC1748CP1	
µA748TC	MC1748CP1	
µA757DC		MC1350P
µA757DM		MC1350P
µA775DC	LM339J	
µA775DM	LM339J	
µA775PC	LM339N	
µA776TC	MC1776CP1	
µA7805CKC	MC7805CT	
µA7805UC	MC7805CT	
µA7805UV	MC7805BT	
µA7806CKC	MC7806CT	
µA7806UC	MC7806CT	
µA7806UV	MC7806BT	
µA7808CKC	MC7808CT	
µA7808UC	MC7808CT	
µA7808UV	MC7808BT	
µA7812CKC	MC7812CT	
µA7812UC	MC7812CT	
µA7812UV	MC7812BT	
µA7815CKC	MC7815CT	
µA7815UC	MC7815CT	
µA7815UV	MC7815BT	
µA7818CKC	MC7818CT	
µA7818UC	MC7818CT	
µA7818UV	MC7818BT	
µA7824CKC	MC7824CT	
µA7824UC	MC7824CT	
µA7824UV	MC7824BT	
µA78GU1C		LM317T
µA78GUC		LM317T
µA78L05ACLP	MC78L05ACP	
µA78L05AWC		MC78L05ACP
µA78L05CLP	MC78L05CP	
µA78L05WC		MC78L05CP
µA78L08ACLP	MC78L08ACP	
µA78L08AWC		MC78L08ACP
µA78L08CLP	MC78L08CP	
µA78L12ACLP	MC78L12ACP	
µA78L12AWC		MC78L12ACP
µA78L12CLP	MC78L12CP	
µA78L12WC		MC78L12CP
µA78L15ACLP	MC78L15ACP	
µA78L15AWC		MC78L15ACP
µA78L15CLP	MC78L15CP	
µA78L15WC		MC78L15CP
µA78L18AWC		MC78L18ACP
µA78L24AWC	MC78L24ACP	
µA78M05CKC	M78M05CT	

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
µA78M05CKD		MC78M05CT
µA78M05UC	MC78M05CT	
µA78M06CKC	MC78M06CT	
µA78M06CKD		MC78M06CT
µA78M06UC	MC78M06CT	
µA78M08CKC	MC78M08CT	
µA78M08CKD		MC78M08CT
µA78M08UC	MC78M08CT	
µA78M12CKC	MC78M12CT	
µA78M12CKD		MC78M12CT
µA78M12UC	MC78M12CT	
µA78M15CKC	MC78M15CT	
µA78M15CKD		MC78M15CT
µA78M15UC	MC78M15CT	
µA78M18UC	MC78M18CT	
µA78M20CKC	MC78M20CT	
µA78M20CKD		MC78M20CT
µA78M20UC	MC78M20CT	
µA78M24CKC	MC78M24CT	
µA78M24CKD		MC78M24CT
µA78M24UC	MC78M24CT	
µA78MGT2C		LM317T
µA78MGU1C		LM317T
µA78MGUC		LM317MT
µA78S40DC	µA78S40DC	
µA78S40DM	µA78S40DM	
µA78S40PC	µA78S40PC	
µA78S40PV	µA78S40PV	
µA7905.2CKC	MC7905.2CT	
µA7905CKC	MC7905CT	
µA7905UC	MC7905CT	
µA7906CKC	MC7906CT	
µA7906UC	MC7906CT	
µA7908CKC	MC7908CT	
µA7912CKC	MC7912CT	
µA7912UC	MC7912CT	
µA7915CKC	MC7915CT	
µA7915UC	MC7915CT	
µA7918CKC	MC7918CT	
µA7918UC	MC7818CT	
µA7924CKC	MC7924CT	
µA7924UC	MC7924CT	
µA796DC	MC1496L	
µA796DM	MC1596L	
µA798RC	MC3458U	
µA798RM	MC3558U	
µA798TC	MC3458P1	
µA79L05AWC	MC79L05ACP	
µA79L05WC	MC79L05CP	
µA79L12AWC	MC79L12ACP	
µA79L12WC	MC79L12CP	
µA79L15AWC	MC79L15ACP	
µA79L15WC	MC79L15CP	
µA79M05AUC	MC79M05CT	
µA79M05CKC	MC79M05CT	
µA79M06AUC		MC7906CT
µA79M06CKC		MC7906CT
µA79M06UC		MC7906CT
µA79M08AUC		MC7908CT
µA79M08CKC		MC7908CT
µA79M08UC		MC7908CT

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
µA79M12AUC	MC79M12CT	
µA79M12CKC	MC79M12CT	
µA79M18AUC		MC7918CT
µA79M18UC		MC7918CT
µA79M24AUC		MC7924CT
µA79M24CKC		MC7924CT
µA79M24UC		MC7924CT
µA9636ATC	MC3488AP1	
UAA1016B	UAA1016B	
UC2842AD	UC2842AD	
UC2842AJ	UC2842AJ	
UC2842AN	UC2842AN	
UC2842BD	UC2842BD	
UC2842BN	UC2842BN	
UC2842D	UC2842AD	
UC2842N	UC2842AN	
UC2843AD	UC2843AD	
UC2843AJ	UC2843AJ	
UC2843AN	UC2843AN	
UC2843BD	UC2843BD	
UC2843BN	UC2843BN	
UC2843D	UC2843AD	
UC2843N	UC2843AN	
UC2844BD	UC2844BD	
UC2844BN	UC2844BN	
UC2844D	UC2844D	
UC2844J	UC2844J	
UC2844N	UC2844N	
UC2845BD	UC2845BD	
UC2845BN	UC2845BN	
UC2845D	UC2845D	
UC2845J	UC2845J	
UC2845N	UC2845N	
UC317T	LM317T	
UC337T	LM337T	
UC3525AJ	SG3525AJ	
UC3525AN	SG3525AN	
UC3526J	SG3526J	
UC3526N	SG3526N	
UC3527AJ	SG3527AJ	
UC3527AN	SG3527AN	
UC3823		MC34023
UC3825		MC34025
UC3842AD	UC3842AD	
UC3842AN	UC3842AN	
UC3842BD	UC3842BD	
UC3842BN	UC3842BN	
UC3842D	UC3842AD	
UC3842N	UC3842AN	
UC3843AD	UC3843AD	
UC3843AN	UC3843AN	
UC3843BD	UC3843BD	
UC3843BN	UC3843BN	
UC3843D	UC3843AD	
UC3843N	UC3843AN	
UC3844BD	UC3844BD	
UC3844BN	UC3844BN	
UC3844D	UC3844D	
UC3844J	UC3844J	
UC3844N	UC3844N	
UC3845BD	UC3845BD	

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
UC3845BN	UC3845BN	
UC3845D	UC3845D	
UC3845N	UC3845N	
UC494ACN		TL594CN
UC494AJ		TL594MJ
UC494CN		TL494CN
UC494J		TL494MJ
UCN5816A	MC34142	
UDN5712M	MC1472P1	
ULN2068BB	ULN2068B	
ULN2068NE	ULN2068B	
ULN2151H	MC1741CP1	
ULN2151M		MC1741CP1
ULN2747A		MC1747CL
ULN2801A	ULN2801A	
ULN2802A	ULN2802A	
ULN2803A	ULN2803A	
ULN2804A	ULN2804A	

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
ULN8126A	SG3526N	
ULN8126R	SG3526J	
ULQ8126R	SC3526J	
ULS2151M		MC1741CP1
ULS2157A		MC1558U
ULS2157H		MC1558U
ULX8161M		MC34060P
UPC1373		MC3373P
UPD6950C		MC10319P
UVC3101		MC10319P
XR082CN	TL082CJG	
XR082CP	TL082CP	
XR082M	TL082MJG	
XR084CN	TL084CJ	
XR084CP	TL084CN	
XR084M	TL084MJ	
XR3470A	MC3470AP	

Amplifiers and Comparators

In Brief . . .

For over two decades, Motorola has continually refined and updated integrated circuit technologies, analog circuit design techniques and processes in response to the needs of the marketplace. The enhanced performance of newer operational amplifiers and comparators has come through innovative application of these technologies, designs and processes. Some early designs are still available but are giving way to the new, higher performance operational amplifier and comparator circuits. Motorola has pioneered in JFET inputs, low temperature coefficient input stages, Miller loop compensation, all NPN output stages, dual-doublet frequency compensation and analog "in-the-package" trimming of resistors to produce superior high performance operational amplifiers and comparators, operating in many cases from a single supply with low input offset, low noise, low power, high output swing, high slew rate and high gain-bandwidth product at reasonable cost to the customer.

Present day operational amplifiers and comparators find applications in all market segments including motor controls, instrumentation, aerospace, automotive, telecommunications, medical, and consumer products.

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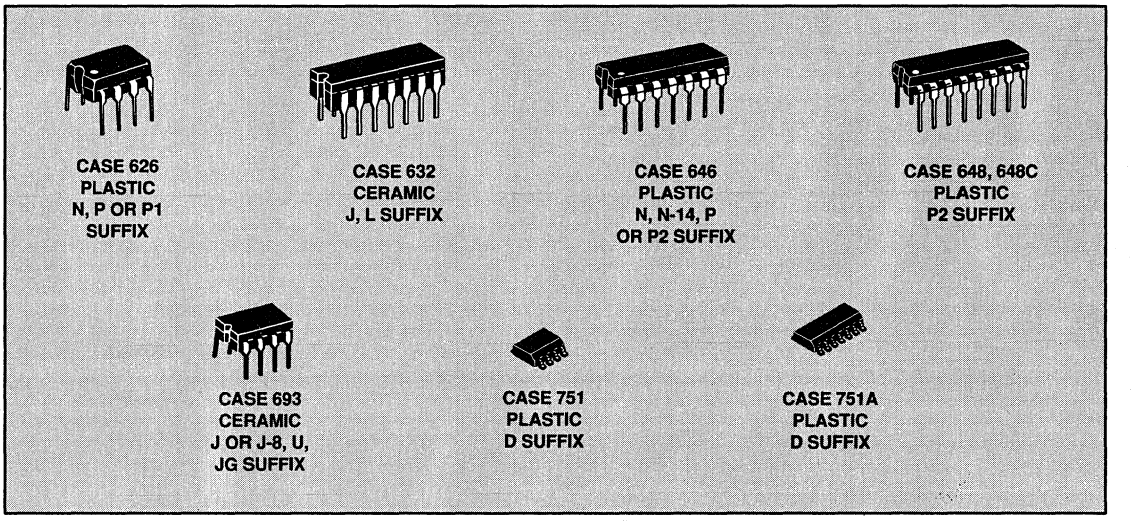


Operational Amplifiers

Motorola offers a broad line of bipolar operational amplifiers to meet a wide range of applications. From low-cost industry-standard types to high precision circuits, the span encompasses a large range of performance capabilities. These linear integrated circuits are available as single, dual and quad monolithic devices in a variety of temperature ranges and package styles. Most devices may be obtained in unencapsulated "chip" form as well. For price and delivery information on chips, please contact your Motorola Sales Representative or Distributor.

Single Operational Amplifiers

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	TC_{VIO} (μV/°C) Typ	I_{IO} (nA) Max	A_{vol} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/μs) Typ	Supply Voltage (V) Min	Supply Voltage (V) Max	Description	Suffix/ Package
Noncompensated											
Commercial Temperature Range (0°C to +70°C)											
LM301A	0.25	7.5	10	50	25	1.0	0.5	±3.0	±18	General Purpose	N/626, J/693
LM308A	7.0	0.5	5.0	1.0	80	1.0	0.3	±3.0	±18	Precision	N/626
MC1748C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	General Purpose	P1
Industrial Temperature Range (–25°C to +85°C)											
LM201A	0.075	2.0	10	10	50	1.0	0.5	±3.0	±22	General Purpose	N/626, J/693
Military Temperature Range (–55°C to +125°C)											
LM101A	0.075	2.0	10	10	50	1.0	0.5	±3.0	±22	General Purpose	J/693
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LF351	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/626
LF356	200 pA	10	5.0	50 pA	50	2.0	15	±5.0	±18	JFET Input	J/693
LF356B	100 pA	5.0	5.0	20 pA	50	5.0	12	±5.0	±22	JFET Input	J/693
LF357	200 pA	10	5.0	50 pA	50	3.0	75	±5.0	±18	Wideband FET Input	J/693
LF357B	100 pA	5.0	5.0	20 pA	50	20	50	±5.0	±22	JFET Input	J/693
LF411C	200 pA	2.0	10	100 pA	25	8.0	25	+5.0	±22	JFET Input, Low Offset, Low Drift	N/626, D/751
LF441C	100 pA	5.0	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power JFET Input	N/626
LM11C	100 pA	0.6	2.0	10 pA	250	1.0	0.3	±3.0	±20	Precision	N/626
LM11CL	200 pA	5.0	3.0	25 pA	50	1.0	0.3	±3.0	±20	Precision	N/626

Single Operational Amplifiers (continued)

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	TC_{VIO} (μV/°C) Typ	I_{IO} (nA) Max	A_{vol} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/μs) Typ	Supply Voltage (V) Min	Supply Voltage (V) Max	Description	Suffix/ Package
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LM307	0.25	7.5	10	50	25	1.0	0.5	±3.0	±18	General Purpose	N/626
MC1436	0.04	10	12	10	70	1.0	2.0	±15	±34	High Voltage	U
MC1741C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	General Purpose	P1, U
MC1776C	0.003	6.0	15	3.0	100	1.0	0.2	±1.2	±18	μPower, Programmable	P1, U
MC3476	0.05	6.0	15	25	50	1.0	0.2	±1.5	±18	Low Cost μPower, Programmable	P1, U
MC34001	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, U
MC34001B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, U
MC34071	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	P/626, U
MC34071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, U
MC34080	200 pA	1.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/626, U
MC34081	200 pA	1.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed JFET Input	P/626, U
MC34181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/626
TL071AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise JFET Input	P/626, JG
TL071C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise JFET Input	P/626, JG
TL081AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, JG
TL081C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, JG
Automotive Temperature Range (–40°C to +85°C)											
MC33071	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	P/626, U
MC33071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, U
MC33171	0.1	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power Single Supply	P/626
MC33181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/626
Extended Automotive Temperature Range (–40°C to +105°C)											
MC33201	200 nA	6.0	2.0	50	50	2.2	1.0	+1.8	+12	Low V Rail-to-Rail™	P/626, D/751
Military Temperature Range (–55°C to +125°C)											
MC1536	0.02	5.0	10	3.0	100	1.0	2.0	±15	±40	High Voltage	U
MC1741	0.5	5.0	15	200	50	1.0	0.5	±3.0	±22	General Purpose	U
MC1776	0.0075	5.0	15	3.0	200	1.0	0.2	±1.2	±18	μPower, Programmable	L
MC35001B	100 pA	5.0	10	50 pA	50	4.0	13	±5.0	±22	JFET Input	U
MC35071	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	U
MC35071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	U
MC35080	200 pA	1.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	U
MC35081	200 pA	1.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed JFET Input	U
MC35171	0.1	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power Single Supply	U
TL081M	200 pA	6.0	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	JG

Dual Operational Amplifiers

2

Internally Compensated

Commercial Temperature Range (0°C to +70°C)

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	TC_{VIO} (μV/°C) Typ	I_{IO} (nA) Max	A_{vol} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/μs) Typ	Supply Voltage (V) Min	Supply Voltage (V) Max	Description	Suffix/ Package
LF353	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/626
LF412C	200 pA	3.0	10	100 pA	25	4.0	13	+5.0	±18	JFET Input, Low Offset, Low Drift	N/626, D/751
LF442C	100 pA	5.0	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power JFET Input	N/626
LM358	0.25	6.0	7.0	50	25	1.0	0.6	±1.5 +3.0	±18 +36	Single Supply, Low Power Consumption	N/626, J/693
LM833	1.0	5.0	2.0	200	31.6	15	7.0	±2.5	±18	Low Noise, Audio	N/626
MC1458	0.5	6.0	10	200	20	1.1	0.8	±3.0	±18	Dual MC1741	P1, U
MC1458C	0.7	10	10	300	20	1.1	0.8	±3.0	±18	General Purpose	P1
MC1747C	0.5	6.0	10	200	25	1.0	0.5	±3.0	±18	Dual MC1741	L, P2
MC3458	0.5	10	7.0	50	20	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies Single Supply Low Crossover Distortion	P1, U
MC4558AC	0.5	5.0	10	200	50	2.8	1.6	±3.0	±22	High Frequency	P1
MC4558C	0.5	6.0	10	200	20	2.8	1.6	±3.0	±18	High Frequency	P1, U
MC34002	100 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	P/626
MC34002B	100 pA	5.0	10	70 pA	25	4.0	13	±5.0	±18	JFET Input	P/626
MC34072	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	P/626, U
MC34072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, U
MC34082	200 pA	3.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed JFET Input	P/626
MC34083	200 pA	3.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/626
MC34182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/626
TL062AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL062C	200 pA	15	10	200 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626
TL072AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise JFET Input	P/626, JG/693
TL072C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise JFET Input	P/626, JG/693
TL082AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, JG/693
TL082C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, JG/693

Industrial Temperature Range (–25°C to +85°C)

LM258	0.15	5.0	10	30	50	1.0	0.6	±1.5 +3.0	±18 +36	Split or Single Supply Op Amp	N/626, J/693

Automotive Temperature Range (–40°C to +85°C)

LM2904	0.25	7.0	7.0	50	100 typ	1.0	0.6	±1.5 +3.0	±13 +26	Split Supplies Single Supply	N/626, J/693
MC3358	5.0	8.0	10	75	20	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies Single Supply	P1/626
MC33072	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance,	P/626, U
MC33072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, U
MC33076	0.5	4.0	2.0	70	25	7.4	2.6	±2.0	±18	High Output Current	P1/626 P2/648C
MC33077	1.0	1.0	2.0	180	150	37	11	±2.5	±18	Low Noise	P/626
MC33078	750 nA	2.0	2.0	150	31.6	16	7.0	±5.0	±18	Low Noise	N/626
MC33102											
(Awake)	500 nA	2.0	1.0	6.0	50	4.0	1.0	±2.5	±18	Sleepmode™	P/626,
(Sleep)	50 nA	2.0	1.0	6.0	25	0.3	0.1	±2.5	±18	Micropower	D/751
MC33172	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power Single Supply	P/626
MC33178	0.5	3.0	2.0	50	50	5.0	2.0	±2.0	±18	High Output Current	P/626
MC33182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/626
MC33272	650 nA	1.0	0.56	25 nA	31.6	5.5	11.5	±1.5	±18	High Performance	P/626
MC33282	100 pA	200 μV	5.0	50 pA	50	30	12	±2.5	±18	Low Input Offset JFET	P/646
TL062V	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	P/626

Dual Operational Amplifiers (continued)

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	TC_{VIO} (μV/°C) Typ	I_{IO} (nA) Max	A_{VOL} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/μs) Typ	Supply Voltage (V) Min	Supply Voltage (V) Max	Description	Suffix/ Package
Extended Automotive Temperature Range (–40°C to +105°C)											
MC33202	200 nA	6.0	2.0	50	50	2.2	1.0	+1.8	+12	Low V Rail-to-Rail™	P/626, D/751
Extended Automotive Temperature Range (–40°C to +125°C)											
TCA0372	500 nA	15	20	50	30	1.1	1.4	+ 5.0	+ 36	Power Op Amp Single Supply	DP1/626 DP2/648
Military Temperature Range (–55°C to +125°C)											
LM158	0.15	5.0	10	30	50	1.0	0.6	± 1.5	± 18	Split Supplies	J/693
								+ 3.0	+ 36	Single Supply Low Power Consumption	
MC1558	0.5	5.0	10	200	50	1.1	0.8	± 3.0	± 22	Dual MC1741	U
MC1747	0.5	5.0	10	200	50	1.0	0.5	± 3.0	± 22	Dual MC1741	L
MC3558	0.5	5.0	10	50	50	1.0	0.6	± 1.5	± 18	Split Supplies	U
								+ 3.0	+ 36	Single Supply	
MC4558	0.5	5.0	10	200	50	2.8	1.6	± 3.0	± 22	High Frequency	U
MC35002	100 pA	10	10	100 pA	25	4.0	13	± 5.0	± 22	JFET Input	U
MC35002B	100 pA	5.0	10	50 pA	50	4.0	13	± 5.0	± 22	JFET Input	U
MC35072	0.5	5.0	10	75	25	4.5	10	+ 3.0	+ 44	High Performance,	U
MC35072A	500 nA	3.0	10	50	50	4.5	10	+ 3.0	+ 44	Single Supply	U
MC35172	0.1	4.5	10	20	50	1.8	2.1	+ 3.0	+ 44	Low Power Single Supply	U
TL062M	200 pA	6.0	10	100 pA	4.0	2.0	6.0	± 2.5	± 18	Low Power JFET Input	JG
TL072M	200 pA	6.0	10	50 pA	35	4.0	13	± 5.0	± 18	Low Noise JFET Input	JG
TL082M	200 pA	6.0	10	100 pA	25	4.0	13	± 5.0	± 18	JFET Input	JG

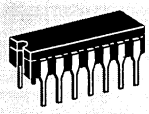
Quad Operational Amplifiers

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	TC_{VIO} (μV/°C) Typ	I_{IO} (nA) Max	A_{VOL} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/μs) Typ	Supply Voltage (V) Min	Supply Voltage (V) Max	Description	Suffix/ Package
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LF347	200 pA	10	10	100 pA	25	4.0	13	± 5.0	± 18	JFET Input	N/646
LF347B	200 pA	5.0	10	100 pA	50	4.0	13	± 5.0	± 18	JFET Input	N/646
LF444C	100 pA	10	10	50 pA	25	2.0	6.0	± 5.0	± 18	Low Power JFET Input	N/646
LM324	0.25	6.0	7.0	50	25	1.0	0.6	± 1.5	± 16	Low Power	J/632, N/646
								+ 3.0	+ 32	Consumption	
LM348	0.2	6.0	—	50	25	1.0	0.5	± 3.0	± 18	Quad MC1741	J/632, N/646
MC3401/ LM3900	0.3	—	—	—	1.0	5.0	0.6	± 1.5	± 18	Norton Input	J/632, N/646
								+ 3.0	+ 36		
MC3403	0.5	10	7.0	50	20	1.0	0.6	± 1.5	± 18	No Crossover	L, P/646
								+ 3.0	+ 36	Distortion	
MC4741C	0.5	6.0	15	200	20	1.0	0.5	± 3.0	± 18	Quad MC1741	L, P/646
MC34004	200 pA	10	10	100 pA	25	4.0	13	± 5.0	± 18	JFET Input	L, P/646
MC34004B	200 pA	5.0	10	100 pA	50	4.0	13	± 5.0	± 18	JFET Input	L, P/646
MC34074	0.5	5.0	10	75	25	4.5	10	+ 3.0	+ 44	High Performance,	L, P/646
MC34074A	500 nA	3.0	10	50	50	4.5	10	+ 3.0	+ 44	Single Supply	L, P/646
MC34084	200 pA	12	10	100 pA	25	8.0	30	± 5.0	± 22	High Speed JFET Input	P/646
MC34085	200 pA	12	10	100 pA	25	16	55	± 5.0	± 22	Decompensated	P/646
MC34184	0.1 nA	10	10	0.05	25	4.0	10	± 2.5	± 18	Low Power JFET Input	P/646
TL064AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	± 2.5	± 18	Low Power JFET Input	N/646
TL064C	200 pA	15	10	200 pA	4.0	2.0	6.0	± 2.5	± 18	Low Power JFET Input	N/646

Quad Operational Amplifiers (continued)

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	TC_{VIO} (μV/°C) Typ	I_{IO} (nA) Max	A_{VOL} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/μs) Typ	Supply Voltage (V) Min	Supply Voltage (V) Max	Description	Suffix/ Package
TL074AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise JFET Input	J/632, N/646
TL074C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise JFET Input	J/632, N/646
TL084AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	J/632, N/646
TL084C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	J/632, N/646
Industrial Temperature Range (–25°C to +85°C)											
LM224	0.15	5.0	7.0	30	50	1.0	0.6	±1.5 +3.0	±16 +32	Split Supplies Single Supply	J/632, N/646
LM248	0.2	6.0	—	50	25	1.0	0.5	±3.0	±18	Quad MC1741	J/632, N/646
Automotive Temperature Range (–40°C to +85°C)											
MC3301/ LM2900	0.3	—	—	—	1.0	4.0	0.6	±2.0 +4.0	±15 +28	Norton Input	P/646 N/646
LM2902	0.5	10	—	50	—	1.0	0.6	±1.5 +3.0	±13 +26	Differential Low Power	J/632, N/646
MC3303	0.5	8.0	10	75	20	1.0	0.6	±1.5 +3.0	±18 +36	Differential General Purpose	P/646
MC33074	0.5	4.5	10	75	25	4.5	10	+3.0	+44	High Performance, Single Supply	L, P/646
MC33074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	High Performance	L, P/646
MC33079	750 nA	2.5	2.0	150	31.6	9.0	7.0	±5.0	±18	Low Noise	N/646
MC33174	0.1	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power Single Supply	P/646
MC33179	0.5	3.0	2.0	50	50	5.0	2.0	±2.0	±18	High Output Current	P/646
MC33184	0.1 nA	10	10	0.05	25	4.0	10	±2.5	±18	Low Power JFET Input	P/646
MC33274	650 nA	1.0	0.56	25 nA	31.6	5.5	11.5	±1.5	±18	High Performance	P/646
MC33284	100 pA	2.0	5.0	50 pA	50	30	12	±2.5	±18	Low Input Offset JFET	P/646
TL064V	200 pA	9.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	N/646
Extended Automotive Temperature Range (–40°C to +105°C)											
MC33204	200 nA	6.0	2.0	50	50	2.2	1.0	+1.8	+12	Low V Rail-to-Rail™	P/646, D/751A
Telecommunications Temperature Range (–40°C to +85°C)											
MC143403	1.0 nA	30	—	200 pA	45 dB	0.8	1.5	4.75	12.6	CMOS Low Power, Drives Low-Impedance Loads	L, P/646
MC143404	1.0 nA	30	—	200 pA	60 dB	0.8	1.0	4.75	12.6	CMOS Very Low Power	L, P/646
Military Temperature Range (–55°C to +125°C)											
LM124	0.15	5.0	7.0	30	50	1.0	0.6	±1.5 +3.0	±16 +32	Low Power Consumption	J/632, N/646
MC3503	0.5	5.0	7.0	50	50	1.0	0.6	±1.5 +3.0	±18 +36	General Purpose, Low Power	L, P/646
MC4741	0.5	5.0	15	200	50	1.0	0.5	±3.0	±22	Quad MC1741	L
MC35004	100 pA	10	10	100 pA	25	4.0	13	±5.0	±22	JFET Input	L
MC35004B	100 pA	5.0	10	50 pA	50	4.0	13	±5.0	±22	JFET Input	L
MC35074	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance, Single Supply	L
MC35074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	High Performance	L
MC35084	200 pA	12	10	100 pA	25	8.0	30	±5.0	±22	High Speed JFET Input	L
MC35085	200 pA	12	10	100 pA	25	16	55	±5.0	±22	Decompensated	L
MC35174	0.1	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	L
TL064M	200 pA	9.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power JFET Input	J/632
TL074M	200 pA	9.0	10	50 pA	35	4.0	13	±5.0	±18	Low Noise JFET Input	J/632
TL084M	200 pA	9.0	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	J/632

CASE 626
PLASTIC
P SUFFIX



CASE 632
CERAMIC
F, L SUFFIX

CASE 751
PLASTIC
D SUFFIX

High Frequency Amplifiers

A variety of high frequency circuits with features ranging from low cost simplicity to multi-function versatility marks Motorola's line of integrated amplifiers. Devices described here are intended for industrial and communications applications. For devices especially dedicated to consumer products, i.e., TV and entertainment radio. (See the Consumer Electronics Circuits section.)

High-Frequency Amplifier Specifications

Operating Temperature Range			A_V (dB)	Bandwidth @ MHz	V_{CC}/V_{EE} (Vdc)		Suffix/ Package
–55° to +125°C	–40° to +85°C	0° to +70°C	Typ		Min	Max	
—	—	MC1350	50 50	45 45	+ 6.0	+ 18	P/626, D/751
—	MC1490	—	50 45 35	10 60 100	+ 6.0	+ 18	P/626
MC1545	—	MC1445	19	50	± 4.0	± 12	L/632

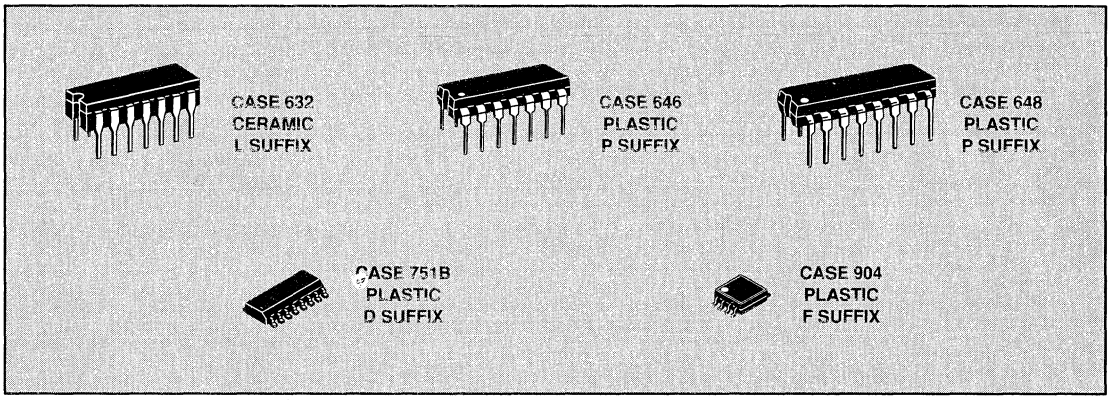
AGC Amplifiers

MC1490/1350 Family Wideband General Purpose Amplifiers

The MC1490 and MC1350 family are basic building blocks — AGC (Automatic Gain Controlled) RF/Video amplifiers. These parts are recommended for applications up through 70 MHz. The best high frequency performance may be obtained by using the physically smaller SOIC version (shorter leads) — MC1350D. There are currently no other RF ICs like these, because other manufacturers have dropped their copies. Applications include variable gain video and instrumentation amplifiers, IF (Intermediate Frequency) amplifiers for radio and TV receivers, and transmitter power output control. Many uses will be found in medical instrumentation, remote monitoring, video/graphics processing, and a variety of communications equipment. The family of parts using the same basic die (identical circuit with slightly different test parameters) is listed in the following table.

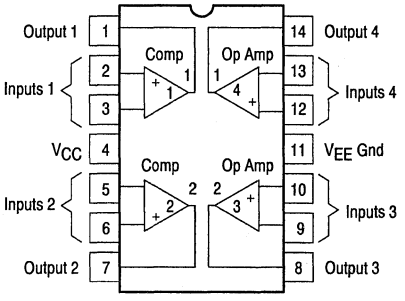
MC1545/1445 Gated 2-Channel Input

Differential input and output amplifier with gated 2-channel input provides for a wide variety of switching purposes. Typical 50 MHz bandwidth makes it suitable for high frequency applications such as video switching, FSK circuits, multiplexers, etc. Gating circuit is useful for AGC control.



Miscellaneous Amplifiers

Motorola provides several Bipolar and CMOS special purpose amplifiers which fill specific needs. These devices range from low power CMOS programmable amplifiers and comparators to variable-gain bipolar power amplifiers.



MC3405/MC3505 Dual Operational Amplifier and Dual Voltage Comparator

This device contains two differential input operational amplifiers and two comparators; each set capable of single supply operation. This operational amplifier/comparator circuit will find its applications as a general purpose product for automotive circuits and as an industrial "building block."

Bipolar

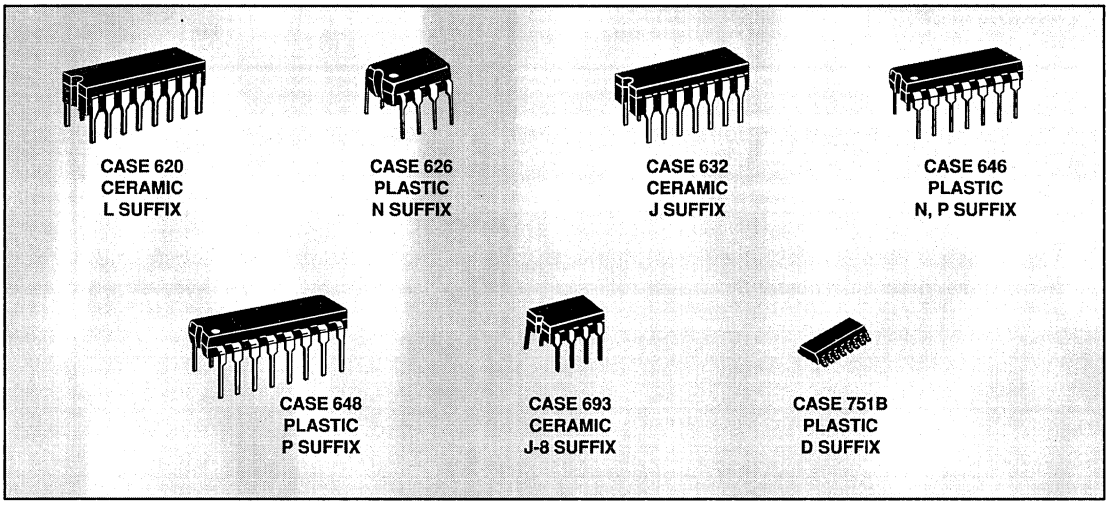
Device	I_{IB} (μA) Max	V_{IO} (mV) Max	I_{IO} (nA) Max	A_{VOL} (V/mV) Min	Response (μs) Typ	Supply Voltage		Suffix/ Package
						Single	Dual	
MC3405	0.5	10	50	20	1.3	3.0 to 36	± 1.5 to ± 18	L/632, P/646
MC3505	0.5	5.0	50	20	1.3	3.0 to 36	± 1.5 to ± 18	L/632

CMOS

MC14573 Quad Programmable Operational Amplifier
MC14576B/MC14577B Dual Video Amplifiers
MC14575 Dual Programmable Operational Amplifier and Dual Programmable Comparator

Function	Quantity Per Package	Single Supply Voltage Range	Dual Supply Voltage Range	Frequency Range	Device Number	Suffix/ Package
Operational Amplifiers	4	3.0 to 15 V	± 1.5 to ± 7.5 V	DC to 1.0 MHz	MC14573	D/751B, P/648
Video Amplifiers	2	5.0 to 12 V(1)	± 2.5 to ± 6 V(2)	Up to 10 MHz	MC14576B MC14577B	P/626, F/904
Operational Amplifiers and Comparators	2 and 2	3.0 to 15 V	± 1.5 to ± 7.5 V	DC to 1.0 MHz	MC14575	D/751B, P/648

(1)5.0 to 10 V for surface mount package
(2)± 2.5 to ± 5 V for surface mount package



Comparators

Single

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	I_{IO} (μA) Max	A_V (V/V) Typ	I_O (mA) Min	Response Time (ns)	Supply Voltage (V)	Description	Temperature Range (°C)	Suffix/ Package
Bipolar										
LM111	0.1	3.0	0.01	200 k	8.0	200	+ 15, – 15	With strobe, will operate	– 55 to + 125	J-8
LM211	0.1	3.0	0.01	200 k	8.0	200	+ 15, – 15	from single supply	– 25 to + 85	J-8
LM311	0.25	7.5	0.05	200 k	8.0	200	+ 15, – 15		0 to + 70	N/626, J-8
CMOS										
MC14578	1.0 pA	50	—	—	1.1	—	3.5 to 14	Requires only 10 μA from single-ended supply	– 30 to + 70	P/648 D/751B

Dual

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	I_{IO} (μA) Max	A_V (V/V) Typ	I_O (mA) Min	Response Time (ns)	Supply Voltage (V)	Description	Temperature Range (°C)	Suffix/ Package
Bipolar										
LM393	0.25	5.0	0.05	200 k	6.0	1300	± 1.5 to ± 18	Designed for single or split	0 to + 70	N/626
LM393A	0.25	2.0	0.05	200 k	6.0	1300	or	supply operation, input	0 to + 70	N/626
LM2903	0.25	7.0	0.05	200 k	6.0	1500	3.0 to 36	common mode includes ground (negative supply)	– 40 to + 85	N/626
MC3405	0.5	10	0.05	200 k	6.0	1300	± 1.5 to ± 7.5	This device contains 2 op	0 to + 70	L, P/646
MC3505	0.5	5.0	0.05	200 k	6.0	1300	or	amps and 2 comparators in	– 55 to + 125	L
							3.0 to 15	a single package		
CMOS										
MC14575	0.001	30	0.0001	2 k	3.0	1000	± 1.5 to ± 7.5	This device contains 2 op	– 40 to + 85	P/648
							or	amps and 2 comparators in		D/751B
							3.0 to 15	a single package		

2

Quad

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	I_{IO} (μA) Max	A_V (V/V) Typ	I_{IO} (mA) Min	Response Time (ns)	Supply Voltage (V)	Description	Temperature Range (°C)	Suffix/ Package
Bipolar										
LM139	0.1	5.0	0.025	200 k	6.0	1300	± 1.5 to ± 18	Designed for single or split	– 55 to + 125	J
LM139A	0.1	2.0	0.025	200 k	6.0	1300	or	supply operation, input	– 55 to + 125	J
LM239	0.25	5.0	0.05	200 k	6.0	1300	3.0 to 36	common mode includes	– 25 to + 85	J, N/646
LM239A	0.25	2.0	0.05	200 k	6.0	1300		ground (negative supply)	– 25 to + 85	J, N/646
LM339	0.25	5.0	0.05	200 k	6.0	1300			0 to + 70	J, N/646
LM339A	0.25	2.0	0.05	200 k	6.0	1300			0 to + 70	J, N/646
LM2901	0.25	7.0	0.05	100 k	6.0	1300			– 40 to + 85	N/646
MC3302	0.5	20	0.5	30 k	6.0	1300			– 40 to + 85	P/646
MC3430	40	6.0	1.0 Typ	1.2 k	16	33	+ 5.0, – 5.0	High speed comparator/	0 to + 70	L, P/648
MC3431	40	10	1.0 Typ	1.2 k	16	33	+ 5.0, – 5.0	sense-amplifier	0 to + 70	L, P/648
MC3432	40	6.0	1.0 Typ	1.2 k	16	40	+ 5.0, – 5.0		0 to + 70	L, P/648
MC3433	40	10	1.0 Typ	1.2 k	16	40	+ 5.0, – 5.0		0 to + 70	L, P/648
CMOS										
MC14574	0.001	30	0.0001	2.0 k	3.0	1000	± 1.5 to ± 7.5 or 3.0 to 15	Externally programmable power dissipation with 1 or 2 resistors	– 40 to + 85	P/648 D/751B

Amplifiers

Amplifiers

Comparators

ADDENDUM

RELATED APPLICATION NOTES

App Note	Title	Related Device
AN926, AR115	Techniques for Improving the Settling of a DAC and Op Amp Combination	**LF357, MC34084, MC34085, MC34087**
AN587	Analysis and Design of the Op Amp Current Source	**MC1741**

LF347
LF351
LF353

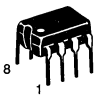
FAMILY OF JFET OPERATIONAL AMPLIFIERS

JFET Input Operational Amplifiers

These low cost JFET input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The JFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices.

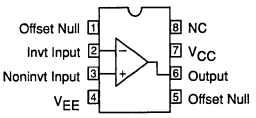
- Input Offset Voltage of 5.0 mV Max (LF347B)
- Low Input Bias Current: 50 pA
- Low Input Noise Voltage: 16 nV/$\sqrt{Hz}$
- Wide Gain Bandwidth: 4.0 MHz
- High Slew Rate: 13V/μs
- Low Supply Current: 1.8 mA per Amplifier
- High Input Impedance: 10^{12} Ω
- High Common Mode and Supply Voltage Rejection Ratios: 100 dB



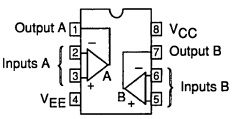
N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

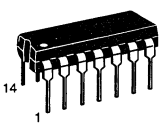
PIN CONNECTIONS



LF351
(Top View)

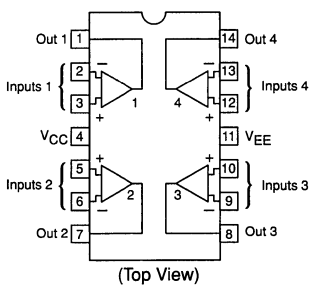


LF353
(Top View)



N SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+18 −18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Power Dissipation at T_A = +25°C Derate above T_A =+25°C	P_D $1/\theta_{JA}$	900 10	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range	T_J	115	°C
Storage Temperature Range	T_{stg}	− 65 to +150	°C

NOTES: 1. Unless otherwise specified, the absolute maximum negative input voltage is limited to the negative power supply.
2. Any amplifier output can be shorted to ground indefinitely. However, if more than one amplifier output is shorted simultaneously, maximum junction temperature rating may be exceeded.

ORDERING INFORMATION

Device	Function	Package
LF351D	Single	SO-8
LF351N	Single	Plastic DIP
LF353D	Dual	S0-8
LF353N	Dual	Plastic DIP
LF347BN	Quad	Plastic DIP
LF347N	Quad	Plastic DIP

2

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = – 15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	LF347B			LF347, LF351, LF353			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le 10$ k, V_{CM} = 0) T_A = +25°C 0°C ≤ T_A ≤ +70°C	V_{IO}	 — —	 1.0 —	 5.0 8.0	 — —	 5.0 —	 10 13	mV
Avg. Temperature Coefficient of Input Offset Voltage $R_S \le 10$ k, 0°C ≤ T_A ≤ +70°C	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	µV/°C
Input Offset Current (V_{CM} = 0, Note 3) T_A = +25°C 0°C ≤ T_A ≤ +70°C	I_{IO}	 — —	 25 —	 100 4.0	 — —	 25 —	 100 4.0	 pA nA
Input Bias Current (V_{CM} = 0, Note 3) T_A = +25°C 0°C ≤ T_A ≤ +70°C	I_{IB}	 — —	 50 —	 200 8.0	 — —	 50 —	 200 8.0	 pA nA
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Common Mode Input Voltage Range	V_{ICR}	±11	+15 –12	—	±11	+15 –12	—	V
Large-Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k) T_A = +25°C 0°C ≤ T_A ≤ +70°C	A_{VOL}	 50 25	 100 —	 — —	 25 15	 100 —	 — —	V/mV
Output Voltage Swing (R_L = 10 k)	V_O	±12	±14	—	±12	±14	—	V
Common Mode Rejection ($R_S \le 10$ k)	CMR	80	100	—	70	100	—	dB
Supply Voltage Rejection ($R_S \le 10$ k)	PSRR	80	100	—	70	100	—	dB
Supply Current LF347 LF351 LF353	I_D	 — — —	 7.2 — —	 11 — —	 — — —	 7.2 1.8 3.6	 11 3.4 6.5	mA
Slew Rate (A_V = +1)	SR	—	13	—	—	13	—	V/µs
Gain-Bandwidth Product	BWp	—	4.0	—	—	4.0	—	MHz
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1000 Hz)	e_n	—	24	—	—	24	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1000 Hz)	i_n	—	0.01	—	—	0.01	—	$pA/\sqrt{Hz}$
Channel Separation (LF347, LF353) 1.0 Hz ≤ f ≤ 20 kHz (Input Referred)	—	—	–120	—	—	–120	—	dB

For Typical Characteristic Performance Curves, refer to MC34001, 34002, 34004 data sheet.

NOTES: 3. Input bias currents of JFET input op amps approximately double for every 10°C rise in junction temperature. To maintain junction temperatures as close to ambient as is possible, pulse techniques are utilized during test.

LF356, LF356B, LF357*, LF357B*

MONOLITHIC JFET OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

Monolithic JFET Input Operational Amplifiers

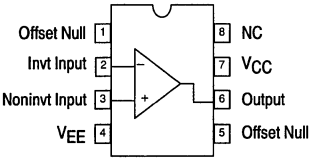
These internally compensated operational amplifiers incorporate highly matched JFET devices on the same chip with standard bipolar transistors. The JFET devices enhance the input characteristics of these operational amplifiers by more than an order of magnitude over conventional amplifiers.

This series of op amps combines the low current characteristics typical of FET amplifiers with the low initial offset voltage and offset voltage stability of bipolar amplifiers. Also, nulling the offset voltage does not degrade the drift or common mode rejection.

- Low Input Bias Current: 30 pA
- Low Input Offset Current: 3.0 pA
- Low Input Offset Voltage: 1.0 mV
- Temperature Compensation of Input Offset Voltage: 3.0 µV/°C
- Low Input Noise Current: 0.01 pA/$\sqrt{Hz}$
- High Input Impedance: $10^{12}\Omega$
- High Common Mode Rejection: 100 dB
- High DC Voltage Gain: 106 dB

J SUFFIX
CERAMIC PACKAGE
CASE 693

PIN CONNECTIONS



(Top View)

SERIES FEATURES

- LF356/356B: Wide Bandwidth
- LF357/357B: Wider Bandwidth Decompensated ($A_{V_{min}}$ = 5)

	LF356/356B	LF357/357B
Fast Setting Time to 0.01%	1.5 µs	1.5 µs
Fast Slew Rate	12 V/µs	50 V/µs
Wide Gain Bandwidth	5.0 MHz	20 MHz
Low Input Noise Voltage	12nV/$\sqrt{Hz}$	12nV/$\sqrt{Hz}$

APPLICATIONS

The LF series is suggested for all general purpose FET input amplifier requirements where precision and frequency response flexibility are of prime importance.

Specific applications include:

- Sample and Hold Circuits
- High Impedance Buffers
- Fast D/A and A/D Converters
- Precision High Speed Integrators
- Wideband, Low Noise, Low Drift Amplifiers

***NOTE:** The LF357/357B are designed for wider bandwidth applications. They are decompensated ($A_{V(min)}$ = 5).

ORDERING INFORMATION

Device	Temperature Range	Package
LF356BJ,J	0° to +70°C	Ceramic DIP
LF357BJ,J		Ceramic DIP

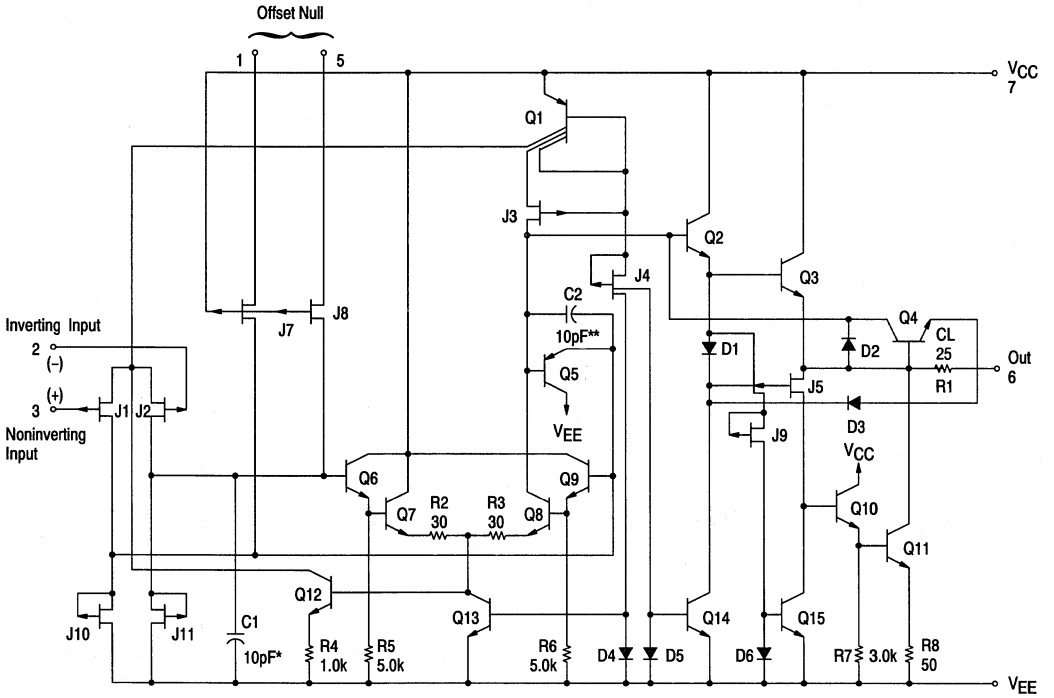
2

MAXIMUM RATINGS

Rating	Symbol	LF356B/357B	LF356/357	Unit
Supply Voltage	V_{CC} V_{EE}	+22 −22	+18 −18	V
Differential Input Voltage	V_{ID}	±40	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±20	±16	V
Output Short Circuit Duration	T_{SC}	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70		°C
Operating Junction Temperature	T_J	150		°C
Storage Temperature Range	T_{stg}	−65 to +150		°C

NOTE: 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

Circuit Schematic



*C1 = 5.0pF on LF357
**C2 = 2.0pF on LF357

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V to 20 V , V_{EE} = –15 V to –20 V for LF356B/357B; V_{CC} = +15 V, V_{EE} = –15 V for LF356/357; T_A = 0° to +70°C, unless otherwise noted.)

Characteristics	Symbol	LF356B/357B			LF356/357			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0) (T_A = 25°C) (Over Temperature)	V_{IO}	 — —	 3.0 —	 5.0 6.5	 — —	 3.0 —	 10 13	mV
Avg. Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω)	$\Delta V_{IO}/\Delta T$	—	5.0	—	—	5.0	—	µV/°C
Change in Average TC with V_{IO} Adjust (R_S = 50 Ω) (Note 2)	$\Delta TC/\Delta V_{IO}$	—	0.5	—	—	0.5	—	µV/°C per mV
Input Offset Current (V_{CM} = 0) (Note 3) (T_J = 25°C) ($T_J \leq$ 70°C)	I_{IO}	 — —	 3.0 —	 2.0 1.0	 — —	 3.0 —	 50 2.0	 pA nA
Input Bias Current (V_{CM} = 0) (Note 3) (T_J = 25°C) ($T_J \leq$ 70°C)	I_{IB}	 — —	 30 —	 100 5.0	 — —	 30 —	 200 8.0	 pA nA
Input Resistance (T_J = 25°C)	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k, V_{CC} = 15 V, V_{EE} = –15 V) (T_A = 25°C) (0°C ≤ $T_A \leq$ +70°C)	A_{VOL}	 50 25	 200 —	 — —	 25 15	 200 —	 — —	V/mV
Output Voltage Swing (V_{CC} = 15 V, V_{EE} = –15 V, R_L = 10 kΩ) (V_{CC} = 15 V, V_{EE} = –15 V, R_L = 2 kΩ)	V_O	 ±12 ±10	 ±13 ±12	 — —	 ±12 ±10	 ±13 ±12	 — —	V
Input Common Mode Voltage Range (V_{CC} = 15 V, V_{EE} = –15 V)	V_{ICR}	±11	+15.1 –12.0	—	±10	+15.1 –12.0		V
Common Mode Rejection	CMR	85	100	—	80	100	—	dB
Supply Voltage Rejection (Note 4)	PSR	85	100	—	80	100	—	dB
Supply Current (T_A = 25°C, V_{CC} = 15 V, V_{EE} = –15 V) LF356B/357B LF356/357	I_D	 — —	 5.0 —	 7.0 —	 — —	 — 5.0	 — 10	mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	LF356B/356			LF357B/357			Unit
		Min	Typ	Max	Min	Typ	Max	
Slew Rate (Note 5) (A_V = 1) LF356 (A_V = 5) LF357	SR	 7.5 —	 12 —	 — —	 — 30	 — 50	 — —	V/µs
Gain Bandwidth Product	GBW	—	5.0	—	—	20	—	MHz
Settling Time to 0.01% (Note 6)	t_s	—	1.5	—	—	1.5	—	µs
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 100 Hz) (R_S = 100 Ω, f = 1000 Hz)	e_n	 — —	 15 12	 — —	 — —	 15 12	 — —	nV/$\sqrt{Hz}$
Equivalent Input Noise Current (f = 100 Hz) (f = 1000 Hz)	i_n	 — —	 0.01 0.01	 — —	 — —	 0.01 0.01	 — —	pA/$\sqrt{Hz}$
Input Capacitance	C_i	—	3.0	—	—	3.0	—	pF

NOTES: 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.
2. The temperature coefficient of the adjusted input offset voltage changes only a small amount (0.5 µV/°C typically) for each mV of adjustment from its original unadjusted value. Common mode rejection and open-loop voltage gain are also unaffected by offset adjustment.
3. The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
4. Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.
5. The minimum slew rate limits apply for the LF356B and the LF357B, but do not apply for the LF356 or LF357.
6. Settling time is defined here, for a unity gain inverter connection using 2.0 k resistors for the LF356. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10 V step input is applied to the inverter. For the LF357, A_V = –5.0, the feedback resistor from output to input is 2.0 k and the output step is 10 V (see settling time test circuit).

Figure 1. Input Bias Current versus Case Temperature

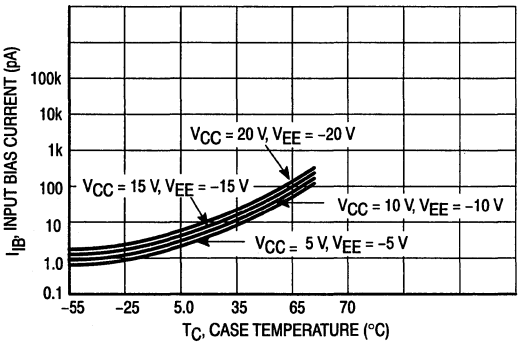


Figure 2. Input Bias Current versus Input Common Mode Voltage

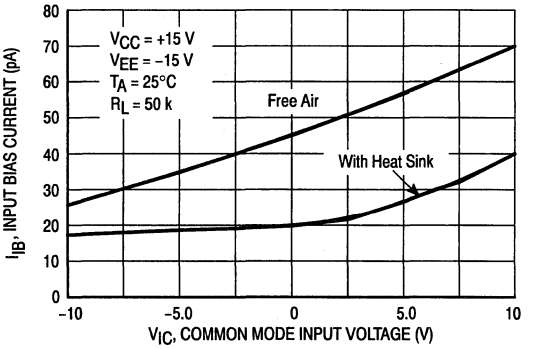


Figure 3. Output Voltage Swing versus Supply Voltage

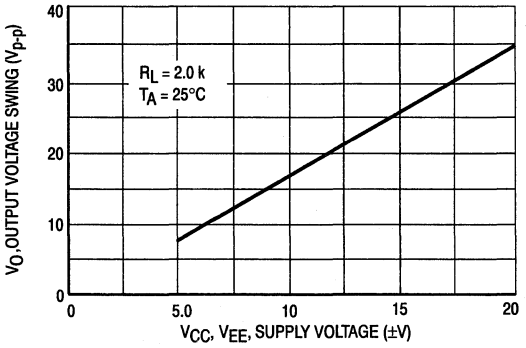


Figure 4. Supply Current versus Supply Voltage

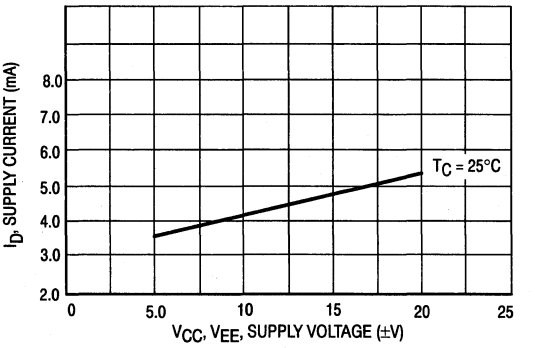


Figure 5. Negative Current Limit

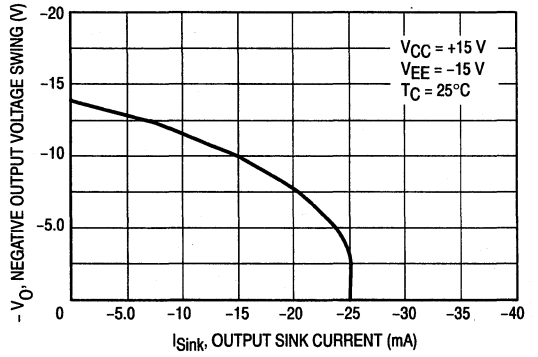


Figure 6. Positive Current Limit

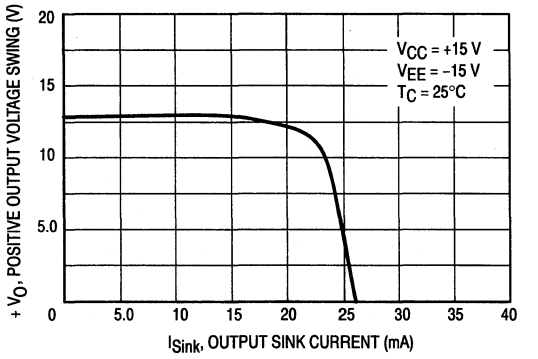


Figure 7. Positive Common Mode Input Voltage Limit

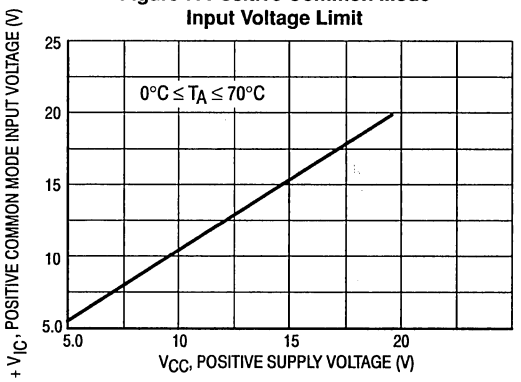


Figure 8. Negative Common Mode Input Voltage Limit

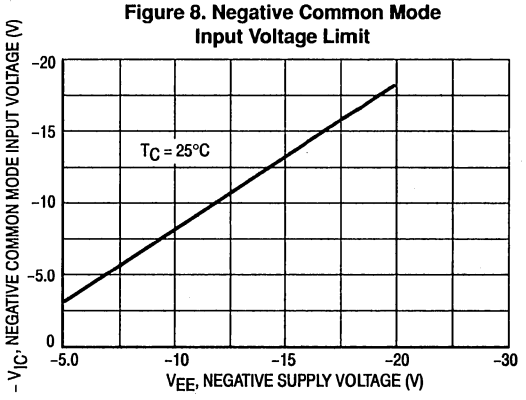


Figure 9. Open-Loop Voltage Gain

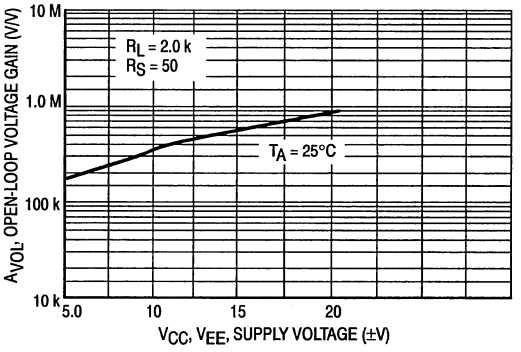


Figure 10. Output Voltage Swing versus Load Resistance

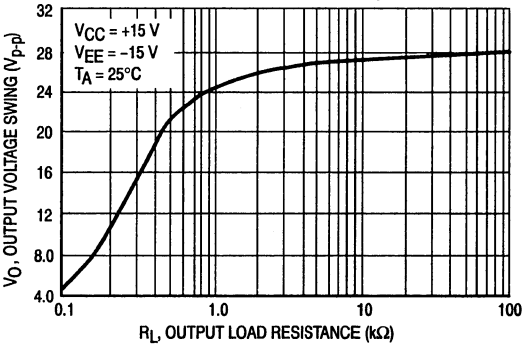


Figure 11. Gain Bandwidth Product (LF356 and LF357 Series)

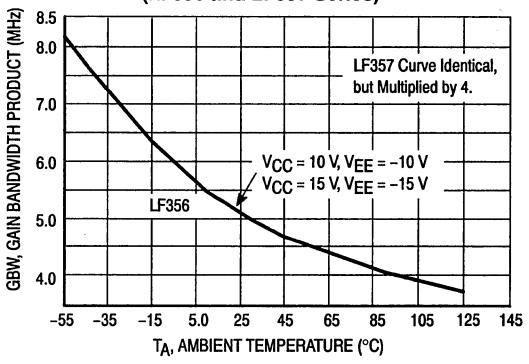


Figure 12. Inverter Settling Time (LF356 and LF357 Series)

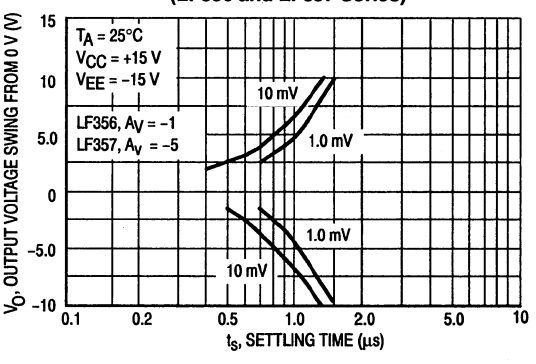


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Figure 13. Normalized Slew Rate

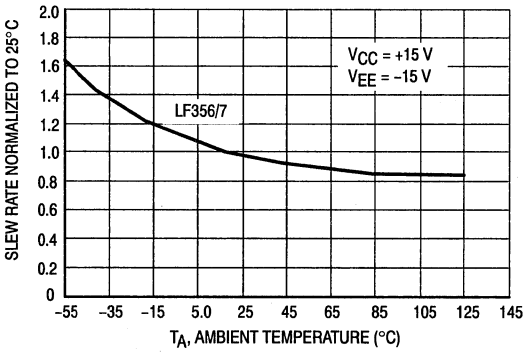


Figure 14. Open-Loop Frequency Response

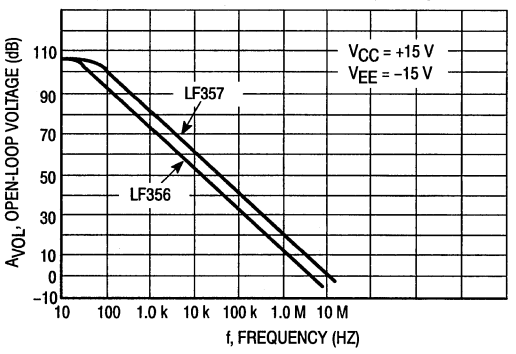


Figure 15. Bode Plot (LF356 Series)

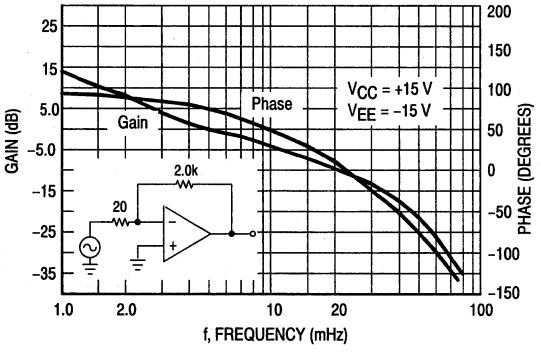


Figure 16. Output Impedance (LF356 Series)

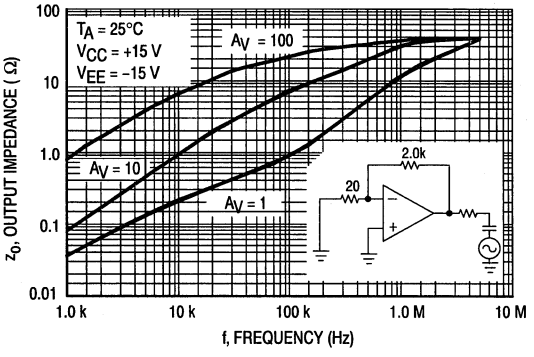


Figure 17. Bode Plot (LF357 Series)

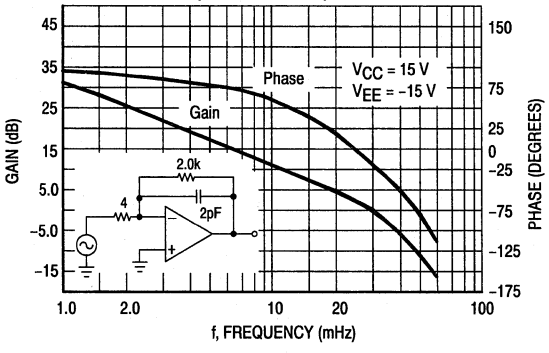


Figure 18. Output Impedance (LF357 Series)

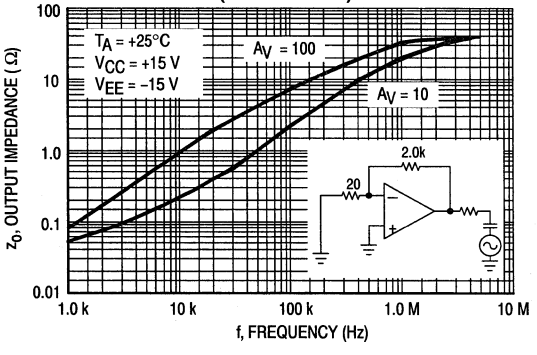


Figure 19. Common Mode Rejection Ratio

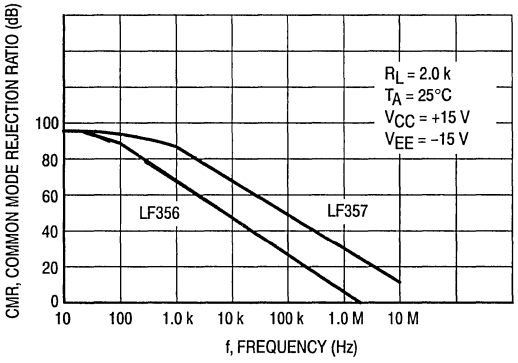


Figure 20. Undistorted Output Voltage Swing

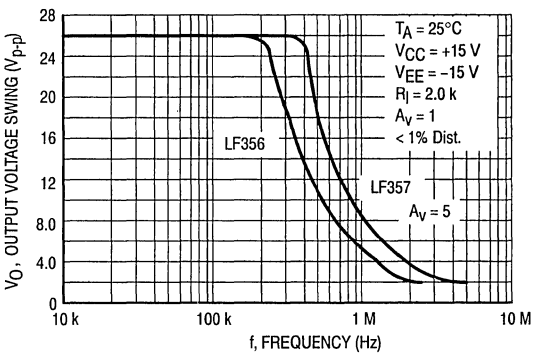


Figure 21. Power Supply Voltage Rejection Ratio

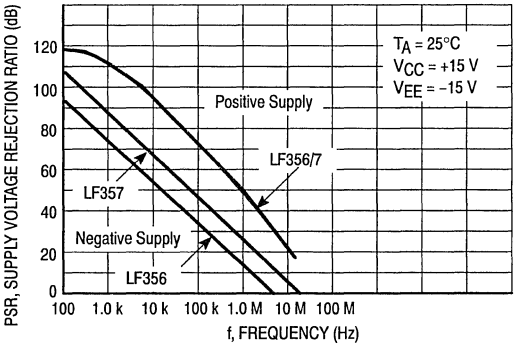


Figure 22. Equivalent Noise Voltage

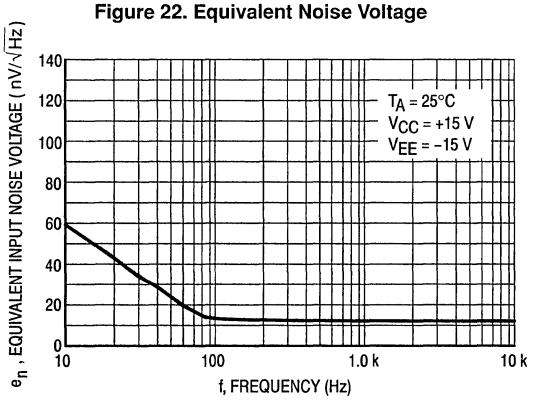
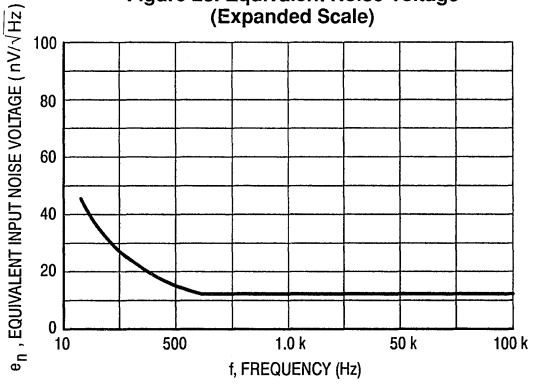
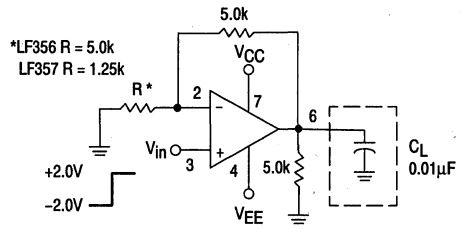


Figure 23. Equivalent Noise Voltage (Expanded Scale)



2

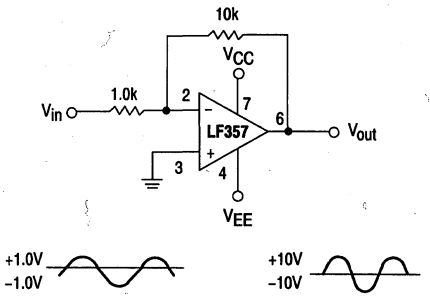
Figure 24. Driving Capacitive Loads



Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability.

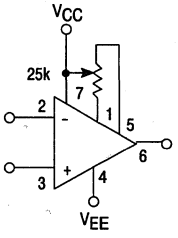
- $C_{L(max)} \cong 0.01\mu F$
- Overshoot $\leq$ 20%
- Settling time (t_s) $\cong$ 5.0 µs

Figure 25. Large Power Bandwidth Amplifier



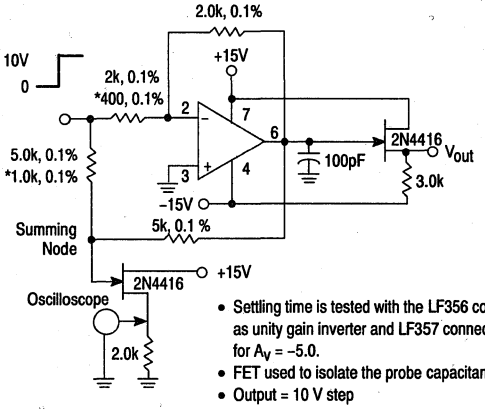
For distortion < 1% and a 20 Vp-p V_{out} swing, power bandwidth is 500 kHz.

Figure 26. Input Offset Voltage Adjustment



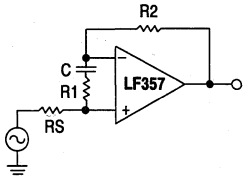
- V_{IO} is adjusted with a 25 k potentiometer
- The potentiometer wiper is connected to V_{CC}
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is $\approx$ 0.5 µV/°C/mV of adjustment.
- Typical overall drift: 5.0 µV/°C ±(0.5 µV/°C/mV of adjustment.)

Figure 27. Settling Time Test Circuit



- Settling time is tested with the LF356 connected as unity gain inverter and LF357 connected for A_V = -5.0.
- FET used to isolate the probe capacitance.
- Output = 10 V step
- A_V = -5.0 for LF357

Figure 28. Noninverting Unity Gain Operation



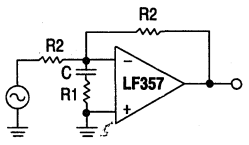
$$R1C \geq \frac{1}{(2\pi)\ (5.0\ MHz)}$$

$$R1 = \frac{R2 + R_S}{4}$$

$A_{V(DC)}$ = 1

$f_{-3dB} \approx$ 5.0 MHz

Figure 29. Inverting Unity Gain



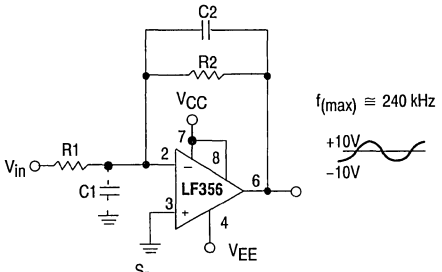
$$R1C \geq \frac{1}{(2\pi)\ (5.0\ MHz)}$$

$$R1 = \frac{R2}{4}$$

$A_{V(DC)}$ = -1

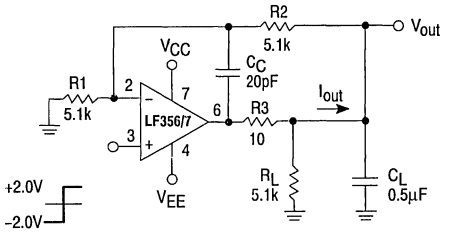
$f_{-3dB} \approx$ 5.0 MHz

Figure 30. Wide BW, Low Noise, Low Drift Amplifier



- Power BW: $f_{(max)} = \frac{S_r}{2\pi V_p} \cong 240\ kHz$
- Parasitic input capacitance (C1 ≅ 3.0 pF for LF356 and LF357 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

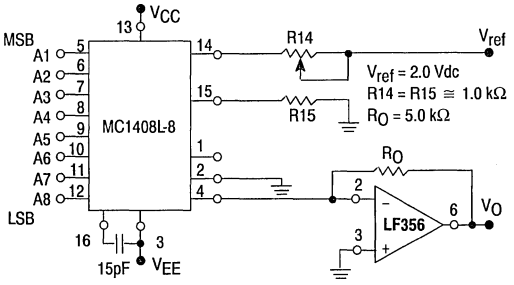
Figure 31. Isolating Large Capacitive Loads



- Overshoot 6%
- t_s = 10 µs
- When driving large C_L, the V_{out} slew rate is determined by C_L and $I_{out(max)}$:

$$\frac{\Delta V_{out}}{\Delta t} = \frac{I_{out}}{C_L} \cong \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s \text{ (with } C_L \text{ shown)}$$

Figure 32. 8-Bit D/A with Output Current to Voltage Conversion



Theoretical V_O

$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R14 or R_O so that V_O with all digital inputs at high level is equal to 9.961 V.

$$V_O = \frac{2.0\ V}{1.0\ k}(5.0\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

LF411C
LF412C

SINGLE/DUAL JFET OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

Low Offset, Low Drift JFET Input Operational Amplifier

Through innovative design concepts and precision matching this monolithic high speed JFET input operational amplifier family offers very low input offset voltage as well as low temperature coefficient of input offset voltage. The amplifier requires less than 3.4 mA per amplifier of supply current yet exhibits greater than 2.7 MHz of gain bandwidth product and more than 8.0 V/μs slew rate. Through the use of JFET inputs the amplifier has very low input bias currents and low input offset currents. The amplifier utilizes industry standard pinouts which afford the user the opportunity to directly upgrade circuit performance without the need for redesign.

The LF411C and LF412C are available in the industry standard plastic 8-pin DIP and SO-8 surface mount packages, and specified over the commercial temperature range.

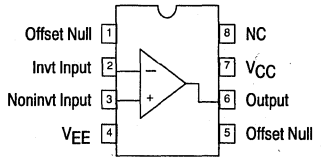
- Low Input Offset Voltage: 2.0 mV Max (Single)
  3.0 mV Max (Dual)
- Low T.C. of Input Offset Voltage: 10 μV/°C
- Low Input Offset Current: 20 pA
- Low Input Bias Current: 60 pA
- Low Input Noise Voltage: 18 nV/ $\sqrt{Hz}$
- Low Input Noise Current: 0.01 pA/ $\sqrt{Hz}$
- Low Total Harmonic Distortion: 0.05%
- Low Supply Current: 2.5 mA
- High Input Resistance: 10^{12} Ω
- Wide Gain Bandwidth: 8.0 MHz
- High Slew Rate: 25 V/μs (Typ)
- Fast Settling Time: 1.6 μs (to within 0.01%)

N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

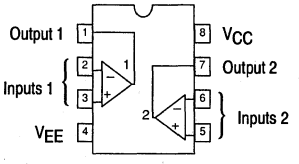
PIN CONNECTIONS

LF411C



(Single, Top View)

LF412C



(Dual, Top View)

ORDERING INFORMATION

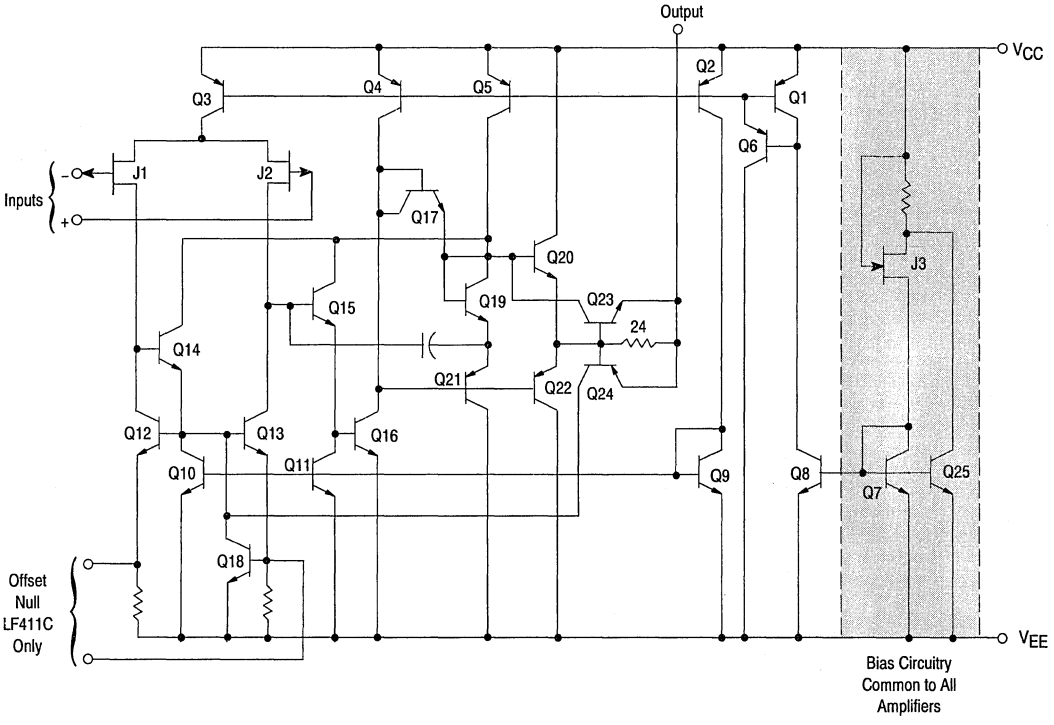
Device	Function	Test Temperature Range	Package
LF411CD LF411CN	Single	0° to +70°C	SO-8 Plastic DIP
LF412CD LF412CN	Dual		

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltages	V_{CC}, $\|V_{EE}\|$	+18	V
Input Differential Voltage Range (Note 1)	V_{IDR}	±30	V
Input Voltage Range (Note 1)	V_{IR}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Thermal Resistance (Junction-to-Ambient) LF411CN/412CN LF411CD/412CD	$R\theta_{JA}$	100 180	°C/W
Storage Temperature	T_{stg}	−60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.
3. Measured with V_{CC} and V_{EE} simultaneously varied.

Representative Circuit Schematic
(Each Amplifier)



2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 0° to 70°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 k Ω, V_{CM} = 0 V, V_O = 0 V)	$\|V_{IO}\|$				mV
LF411		—	0.5	2.0	
LF412		—	1.0	3.0	
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$				μV/°C
(R_S = 10 k Ω, V_{CM} = 0 V, V_O = 0 V)		—	10	—	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}				
LF411 T_A = 25°C		—	20	100	pA
T_A = 0° to 70°C		—	—	2.0	nA
LF412 T_A = 25°C		—	25	100	pA
T_A = 0° to 70°C		—	—	2.0	nA
Input Bias Current (V_{CM} = 0 V)	I_{IB}				
LF411 T_A = 25°C		—	0.6	200	pA
T_A = 0° to 70°C		—	—	4.0	nA
LF412 T_A = 25°C		—	0.5	200	pA
T_A = 0° to 70°C		—	—	4.0	nA
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k Ω)	A_{VOL}				V/mV
LF411 T_A = 25°C		25	80	—	
T_A = 0° to 70°C		15	—	—	
LF412 T_A = 25°C		25	150	—	
T_A = 0° to 70°C		15	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V, R_L = 10 kΩ)					V
LF411	V_O+	+12	+13.9	—	
	V_O-	—	−14.7	−12	
LF412	V_O+	+12	+14.0	—	
	V_O-	—	−14.0	−12	
Common Mode Input Voltage Range (V_O = 0 V)	V_{ICR}				V
LF411		+11	+14	−11	
		—	−14	—	
LF412		+11	+15	−11	
		—	−12	—	
Common Mode Rejection (V_{CM} = ±11 V, R_S ≤ 10 k Ω)	CMR				dB
LF411		70	90	—	
LF412		70	100	—	
Power Supply Rejection (Note 3)	PSR				dB
(V_{CC} V_{EE} = +15 V, −15 V to +5.0 V, −5.0 V)					
LF411		70	86	—	
LF412		70	100	—	
Power Supply Current (V_O = 0 V)	I_D				mA
LF411		—	2.5	3.4	
LF412		—	2.8	6.8	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 k Ω, A_V = +1.0)	SR				V/μs
LF411		8.0	25	—	
LF412		8.0	13	—	
Gain Bandwidth Product	GBW				MHz
LF411		2.7	8.0	—	
LF412		2.7	4.0	—	
Channel Separation (f = 1.0 Hz to 20 kHz, LF412)	CS	—	−120	—	dB
Differential Input Resistance (V_{CM} = 0 V)	R_{in}	—	10^{12}	—	kΩ
Equivalent Input Voltage Noise (R_S = 100 Ω, f = 1.0 kHz)	e_n				nV/√Hz
LF411		—	30	—	
LF412		—	25	—	
Equivalent Input Noise Current (f = 1.0 kHz)	i_n				pA/√Hz
LF411		—	0.01	—	
LF412		—	0.01	—	

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

LF441C
LF442C
LF444C

Low Power JFET Input Operational Amplifier

LOW POWER JFET INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

These JFET input operational amplifiers are designed for low power applications. They feature high input impedance, low input bias current and low input offset current. Advanced design techniques allow for higher slew rates, gain bandwidth products and output swing. The LF441C device provides for the external null adjustment of input offset voltage.

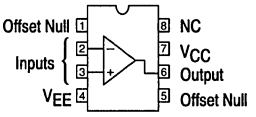
These devices are specified over the commercial temperature range. All are available in plastic dual in-line and SOIC packages.

- Low Supply Current: 200 µA/Amplifier
- Low Input Bias Current: 5.0 pA
- High Gain Bandwidth: 2.0 MHz
- High Slew Rate: 6.0 V/ µs
- High Input Impedance: 10^{12} Ω
- Large Output Voltage Swing: ±14 V
- Output Short Circuit Protection

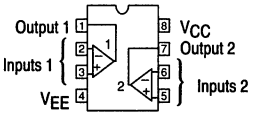
N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS

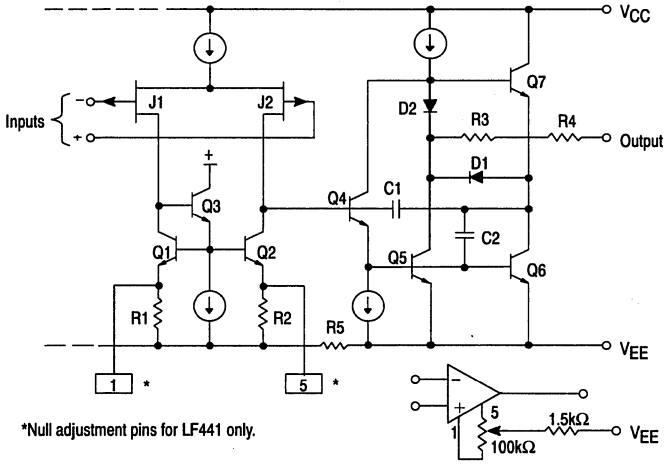


(Single, Top View)



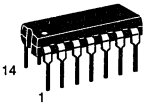
(Dual, Top View)

EQUIVALENT CIRCUIT SCHEMATIC (EACH AMPLIFIER)

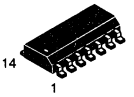


*Null adjustment pins for LF441 only.

LF441C input offset voltage null adjust circuit

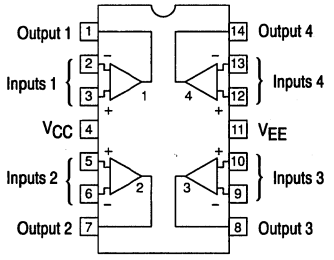


N SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Quad, Top View)

ORDERING INFORMATION

Device	Function	Tested Temperature Range	Package
LF441CD LF441CN	Single	0° to +70°C	SO-8 Plastic DIP
LF442CD LF442CN	Dual		SO-8 Plastic DIP
LF444CD LF444CN	Quad		SO-14 Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range (Note 1)	V_{IDR}	±30	V
Input Voltage Range (Notes 1 and 2)	V_{IR}	±15	V
Output Short Circuit Duration (Note 3)	t_{SC}	Indefinite	sec
Operating Junction Temperature (Note 3)	T_J	+150	°C
Storage Temperature Range	T_{stg}	–60 to +150	°C

NOTES: 1. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
2. The magnitude of the input voltage must never exceed the magnitude of the supply or 15 V, whichever is less.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See Figure 1.)

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 0° to 70°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 kΩ, V_O = 0 V)	V_{IO}				mV
Single: T_A = +25°C		—	3.0	5.0	
T_A = 0° to +70°C		—	—	7.5	
Dual: T_A = +25°C		—	3.0	5.0	
T_A = 0° to +70°C		—	—	7.5	
Quad: T_A = +25°C		—	3.0	10	
T_A = 0° to +70°C		—	—	12	
Average Temperature Coefficient of Offset Voltage (R_S = 10 kΩ, V_O = 0 V)	$\Delta V_{IO}/\Delta T$	—	10	—	µV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}				
T_A = +25°C		—	0.5	50	pA
T_A = 0° to +70°C		—	—	1.5	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}				
T_A = +25°C		—	3.0	100	pA
T_A = 0° to +70°C		—	—	3.0	nA
Common Mode Input Voltage Range (T_A = +25°C)	V_{ICR}	—	+14.5	+11	V
		–11	–12	—	
Large Signal Voltage Gain (V_O = ±10 V, R_L = 10 kΩ)	A_{VOL}				V/mV
T_A = +25°C		25	60	—	
T_A = 0° to +70°C		15	—	—	
Output Voltage Swing (R_L = 10 kΩ)	V_O+	+12	+14	—	V
	V_O-	—	–14	–12	
Common Mode Rejection ($R_S \leq$ 10 kΩ, $V_{CM} = V_{ICR}$, V_O = 0 V)	CMR	70	86	—	dB
Power Supply Rejection (R_S = 100 Ω, V_{CM} = 0 V, V_O = 0 V)	PSR	70	84	—	dB
Power Supply Current (No Load, V_O = 0 V)	I_D				µA
Single		—	200	250	
Dual		—	400	500	
Quad		—	800	1000	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 10 kΩ, C_L = 10 pF, A_V = +1.0)	SR	0.6	6.0	—	V/µs
Settling Time To within 10 mV	t_s	—	1.6	—	µs
(A_V = –1.0, R_L = 10 kΩ, V_O = 0 V to +10 V) To within 1.0 mV		—	2.2	—	
Gain Bandwidth Product (f = 200 kHz)	GBW	0.6	2.0	—	MHz
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	e_n	—	47	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	i_n	—	0.01	—	$pA/\sqrt{Hz}$
Input Resistance	R_i	—	10^{12}	—	Ω
Channel Separation (f = 1.0 Hz to 20 kHz)	CS	—	120	—	dB

Figure 1. Maximum Power Dissipation versus Temperature for Package Variations

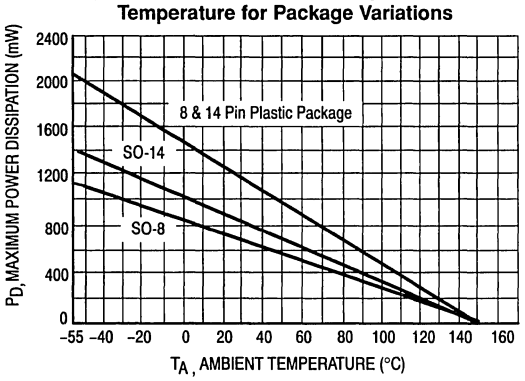


Figure 2. Input Bias Current versus Input Common Mode Voltage

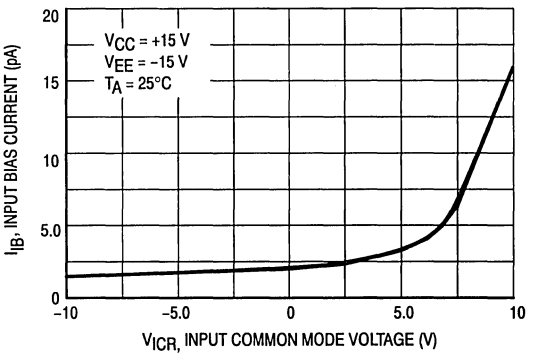


Figure 3. Input Bias Current versus Temperature

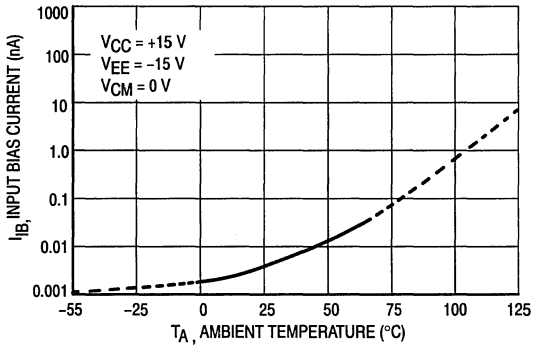


Figure 4. Supply Current versus Supply Voltage

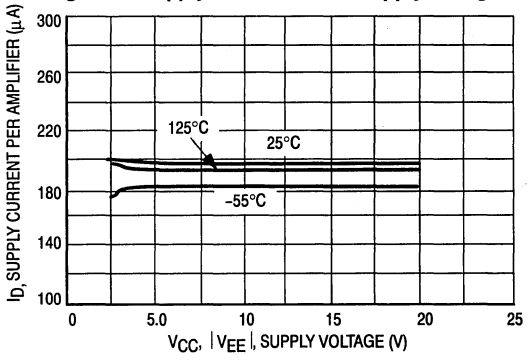


Figure 5. Positive Input Common Mode Voltage Range versus Positive Supply Voltage

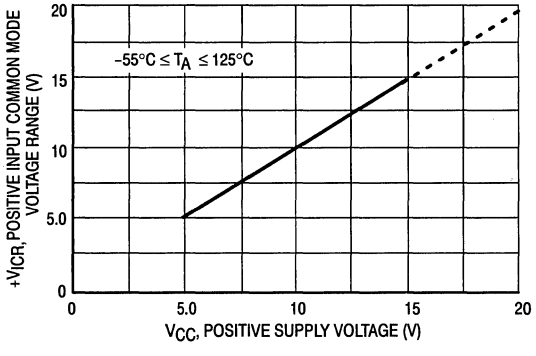


Figure 6. Negative Input Common Mode Voltage Range versus Negative Supply Voltage

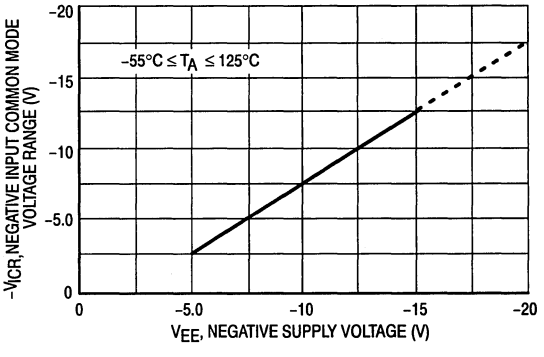


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Figure 7. Output Voltage versus Output Source Current

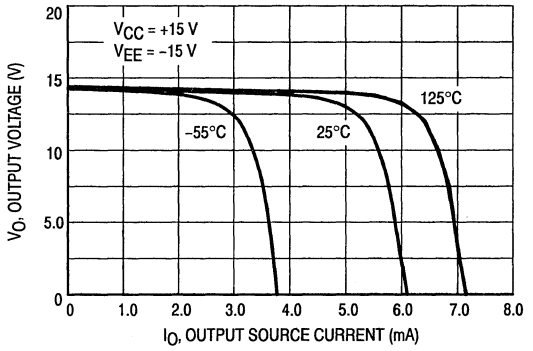

Figure 8. Output Voltage versus Output Sink Current

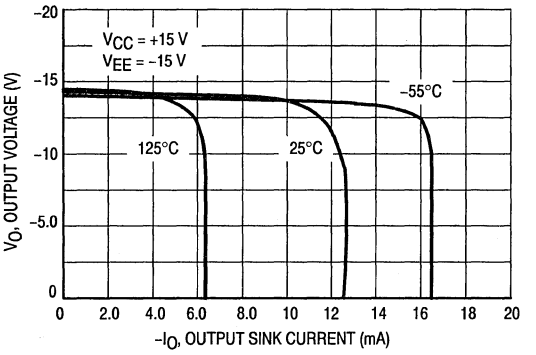

Figure 9. Output Voltage Swing versus Supply Voltage

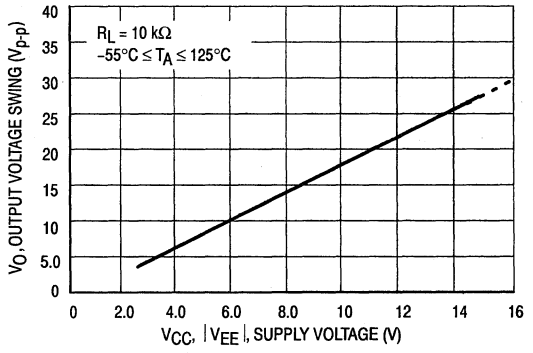

Figure 10. Output Voltage Swing versus Load Resistance

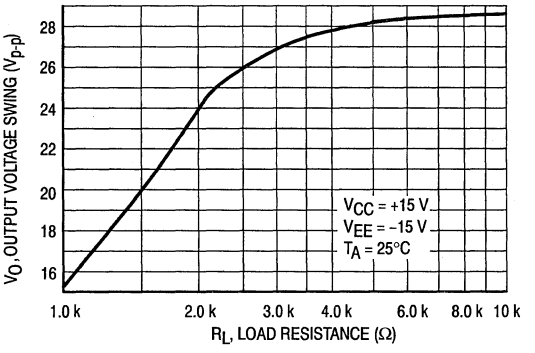

Figure 11. Normalized Gain Bandwidth Product versus Temperature

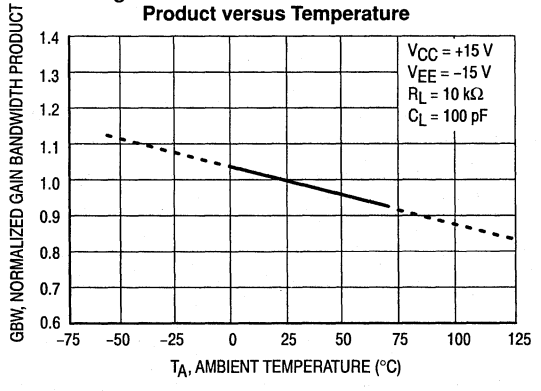

Figure 12. Open-Loop Voltage Gain and Phase versus Frequency

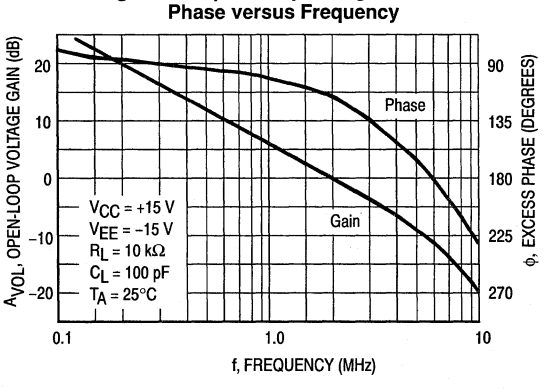

Figure 13. Slew Rate versus Temperature

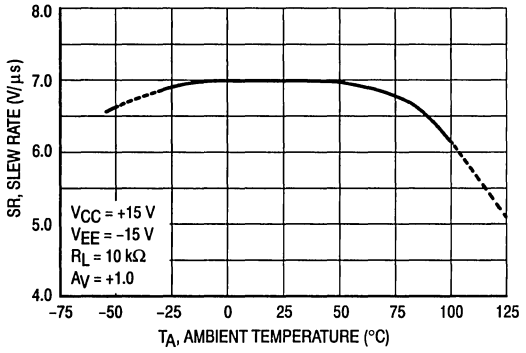

Figure 14. Total Output Distortion versus Frequency

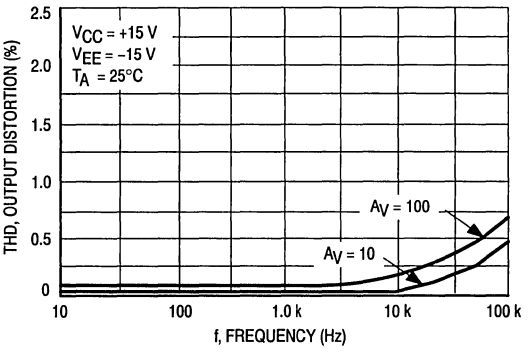

Figure 15. Output Voltage Swing versus Frequency

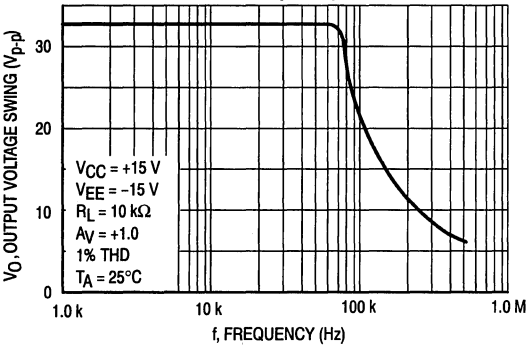

Figure 16. Open-Loop Voltage Gain versus Frequency

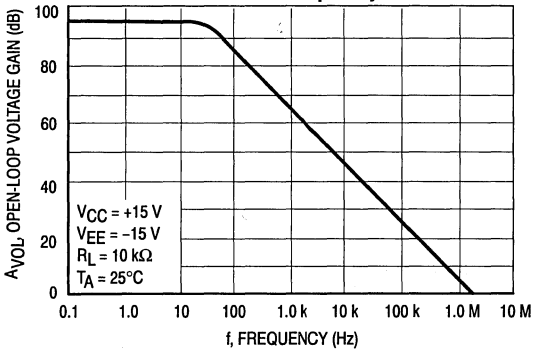

Figure 17. Common Mode Rejection versus Frequency

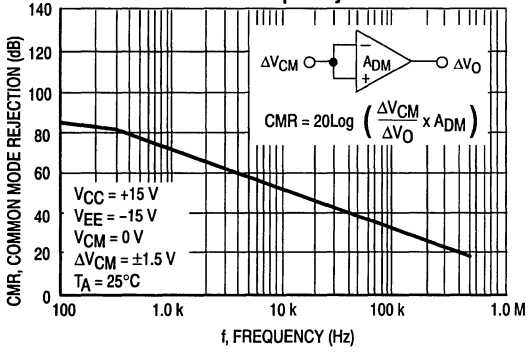

Figure 18. Power Supply Rejection versus Frequency

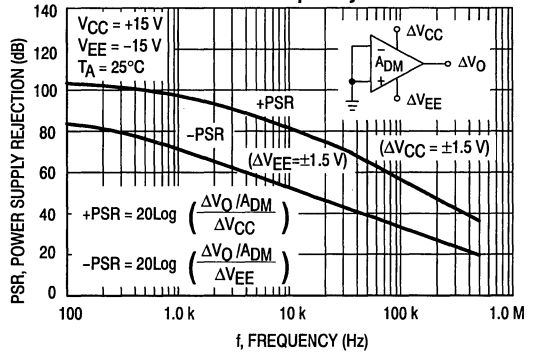

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Figure 19. Input Noise Voltage versus Frequency

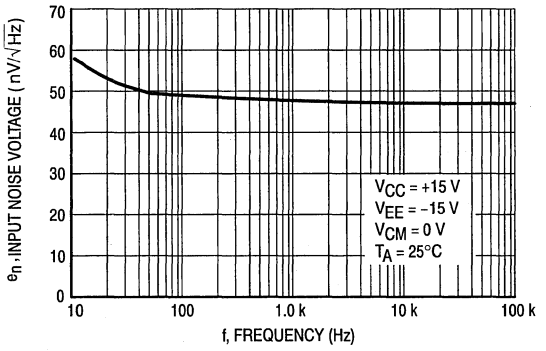


Figure 20. Open-Loop Voltage Gain versus Supply Voltage

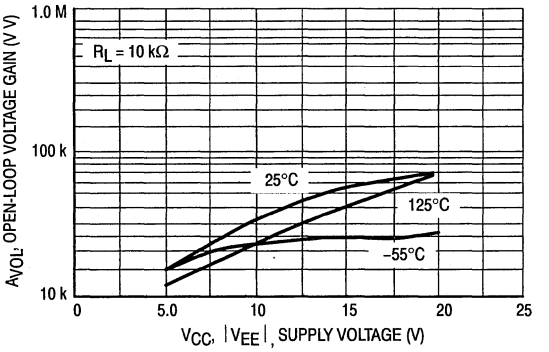


Figure 21. Output Impedance versus Frequency

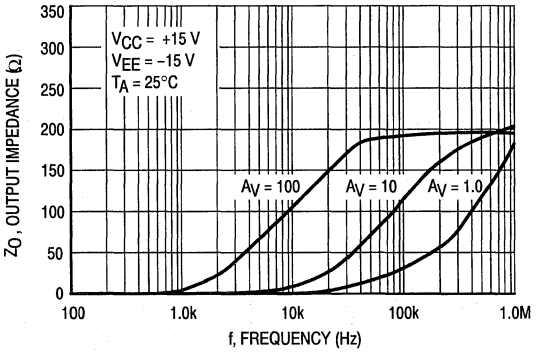
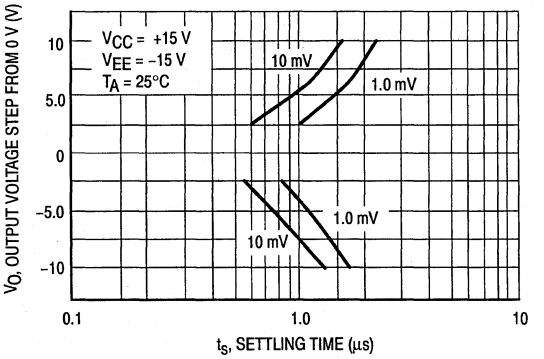


Figure 22. Inverter Settling Time



SMALL SIGNAL RESPONSE

Figure 23. Inverting

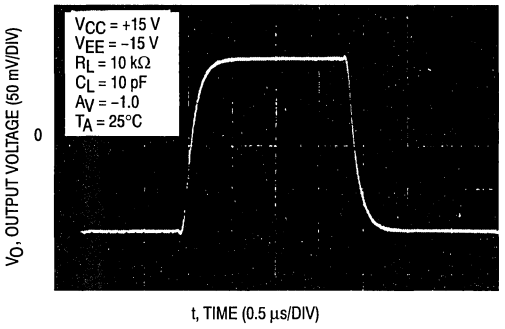
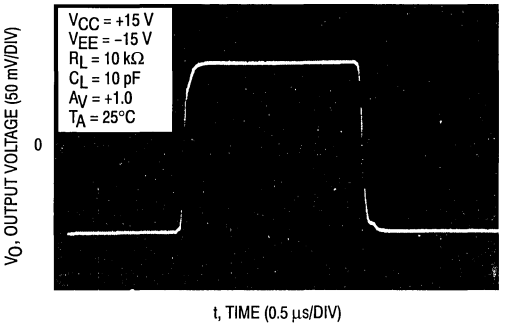


Figure 24. Noninverting



LARGE SIGNAL RESPONSE

Figure 25. Inverting

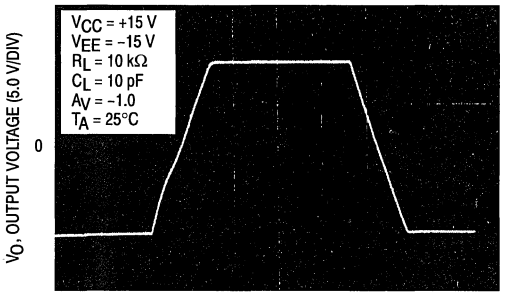
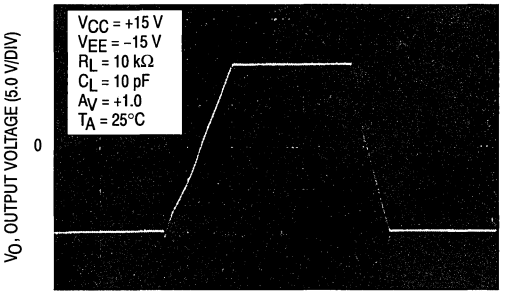


Figure 26. Noninverting



LM11C
LM11CL

2

Precision Operational Amplifiers

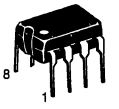
PRECISION OPERATIONAL AMPLIFIERS
SILICON MONOLITHIC INTEGRATED CIRCUIT

The LM11C is a precision, low drift operational amplifier providing the best features of existing FET and Bipolar op amps. Implementation of super gain transistors allows reduction of input bias currents by an order of magnitude over earlier devices such as the LM308A. Offset voltage and drift have also been reduced. Although bandwidth and slew rate are not as great as FET devices, input offset voltage, drift and bias current are inherently lower, particularly over temperature. Power consumption is also much lower, eliminating warm-up stabilization time in critical applications.

Offset balancing is provided, with the range determined by an external low resistance potentiometer. Compensation is provided internally, but external compensation can be added for improved stability when driving capacitive loads.

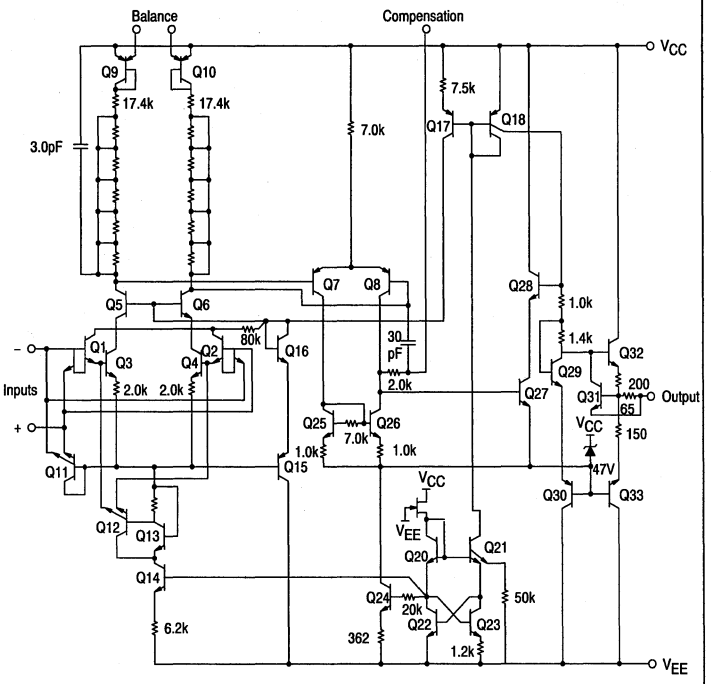
The precision characteristics of the LM11C make this device ideal for applications such as charge integrators, analog memories, electrometers, active filters, light meters and logarithmic amplifiers.

- Low Input Offset Voltage: 100 μV
- Low Input Bias Current: 17 pA
- Low Input Offset Current: 0.5 pA
- Low Input Offset Voltage Drift: 1.0 μV/°C
- Long-Term Stability: 10 μV/year
- High Common Mode Rejection: 130 dB

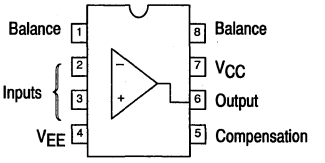


N SUFFIX
PLASTIC PACKAGE
CASE 626

Schematic Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM11CLN, CN	0° to +70°C	Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} to V_{EE}	40	Vdc
Differential Input Current (Note 1)	I_{ID}	±10	mA
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	
Power Dissipation (Note 3)	P_D	500	mW
Operating Junction Temperature	T_J	85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted [Note 4] .)

Characteristics	Symbol	LM11C			LM11CL			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	0.2	0.6	—	0.5	5.0	mV
T_{low} to T_{high}		—	—	0.8	—	—	6.0	
Input Offset Current	I_{IO}	—	1.0	10	—	4.0	25	pA
T_{low} to T_{high}		—	—	20	—	—	50	
Input Bias Current	I_{IB}	—	17	100	—	17	200	pA
T_{low} to T_{high}		—	—	150	—	—	300	
Input Resistance	r_i	—	10^{11}	—	—	10^{11}	—	Ω
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	—	2.0	5.0	—	3.0	—	μV/°C
T_{low} to T_{high}								
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$	—	10	—	—	50	—	fA/°C
T_{low} to T_{high}								
Input Bias Current Drift	$\Delta I_{IB}/\Delta T$	—	0.8	3.0	—	1.4	—	pA/°C
T_{low} to T_{high}								
Large Signal Voltage Gain	A_{VOL}							V/mV
V_S = ±15 V, V_{out} = ±12 V, I_{out} = ±2.0 mA		100	300	—	25	300	—	
T_{low} to T_{high} (Note 5)		50	—	—	15	—	—	
V_S = ±15 V, V_{out} = ±12 V, I_{out} = ±0.5 mA		250	1200	—	50	800	—	
T_{low} to T_{high}		100	—	—	30	—	—	
Common Mode Rejection	CMR							dB
V_S = ±15 V, −13 V ≤ V_{CM} ≤ 14 V		110	130	—	96	110	—	
V_S = ±15 V, −12.5 V ≤ V_{CM} ≤ 14 V,		100	—	—	90	—	—	
T_{low} to T_{high}								
Power Supply Rejection	PSR							dB
±2.5 V ≤ V_S ≤ ±20 V		100	118	—	84	100	—	
T_{low} to T_{high}		96	—	—	80	—	—	
Power Supply Current	I_D	—	0.3	0.8	—	0.3	0.8	mA
T_{low} to T_{high}		—	—	1.0	—	—	1.0	
Output Short Circuit Current	I_{SC}	—	±10	—	—	±10	—	mA
T_J = 150°C, Output Shorted to Ground								

NOTES: 1. The inputs are shunted by back-to-back diodes for over-voltage protection. Excessive current will flow if the input differential voltage is in excess of 1.0 V if no limiting resistance is used. Additionally, a 2.0 kΩ resistance in each input is suggested to prevent possible latch-up initiated by supply reversals.

2. The output is current limited when shorted to ground or any voltages less than the supplies. Continuous overloads will require package dissipation to be considered and heatsinking should be provided when necessary.

3. Devices must be derated based on package thermal resistance (see package outline dimensions).

4. These specifications apply for V_{EE} +2.0 V ≤ V_{CM} ≤ V_{CC} −1.0 V (V_{EE} +2.5 V ≤ V_{CM} ≤ V_{CC} −1.0 V for T_{low} to T_{high}) and ±2.5 V ≤ V_S ≤ ±20 V T_{low} to T_{high}: 0°C ≤ T_J ≤ +70°C for LM11C and LM11CL

5. V_{out} = ±11.5 V, all other conditions unchanged.

2

Figure 1. Input Bias Current versus Case Temperature

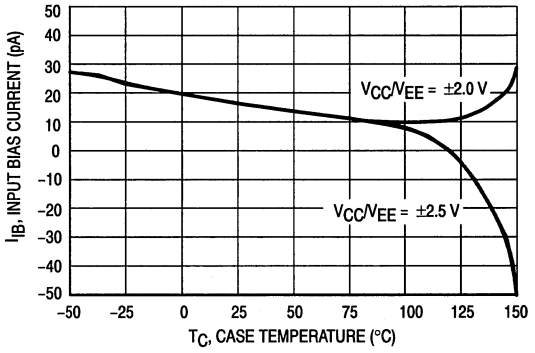


Figure 2. Input Offset Current versus Case Temperature

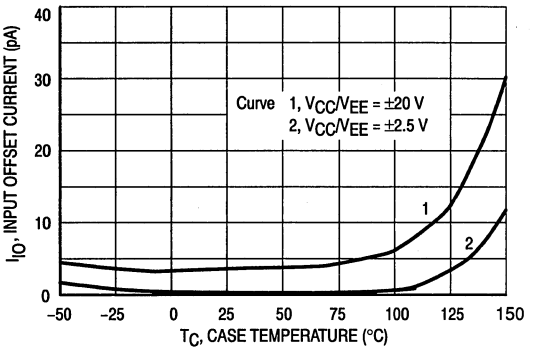


Figure 3. Temperature Coefficient of Input Offset Voltage versus Input Offset Voltage

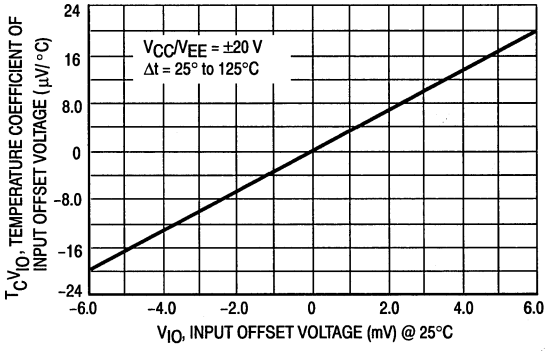


Figure 4. Spectral Noise Density

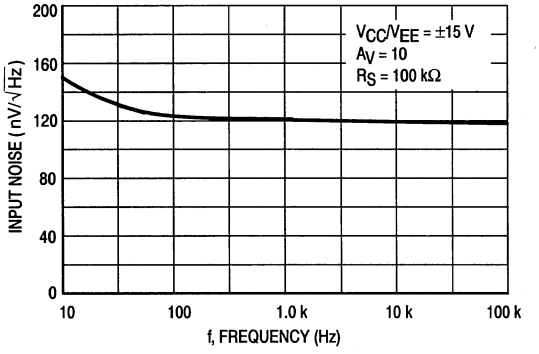


Figure 5. Common Mode Limits versus Temperature

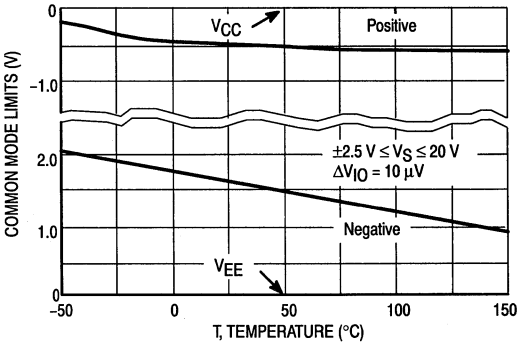


Figure 6. Common Mode Rejection and Slew Limit versus Frequency

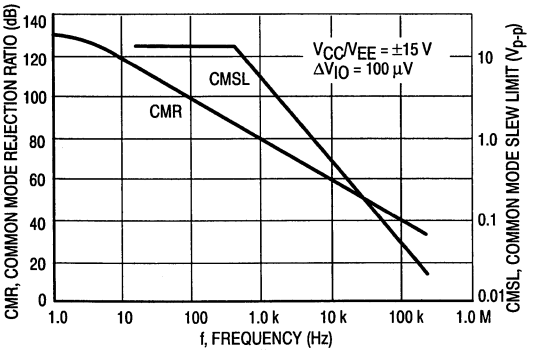


Figure 7. Open-Loop Voltage Gain versus Supply Voltage

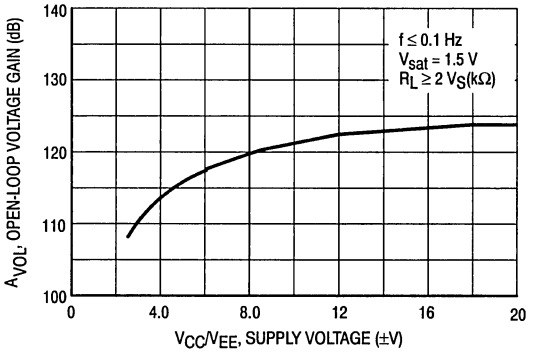


Figure 8. Output Saturation versus Load Current

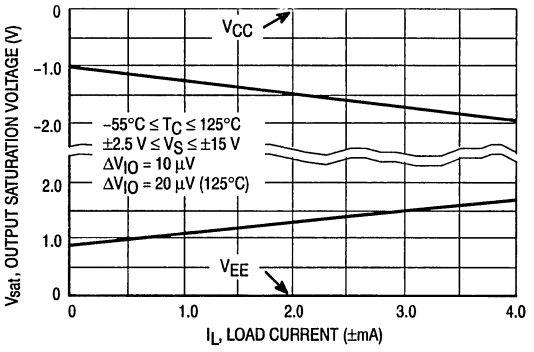


Figure 9. Power Supply Rejection Ratio versus Frequency

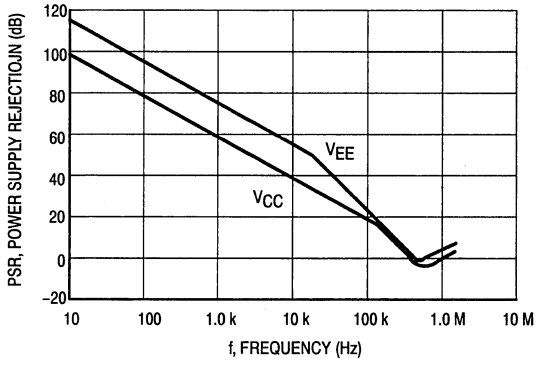


Figure 10. Supply Current versus Supply Voltage

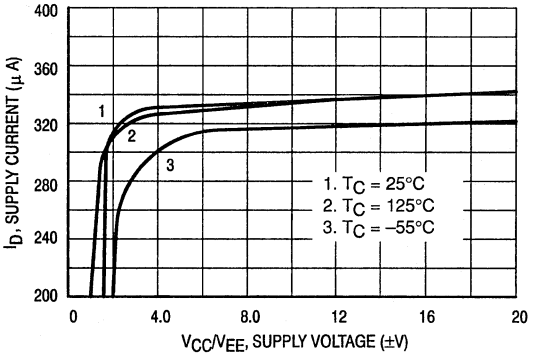


Figure 11. Open-Loop Voltage Gain and Phase versus Frequency

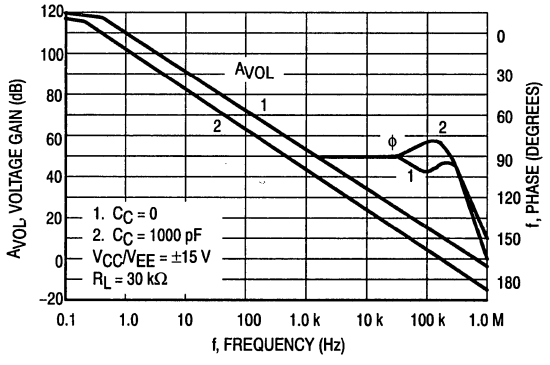
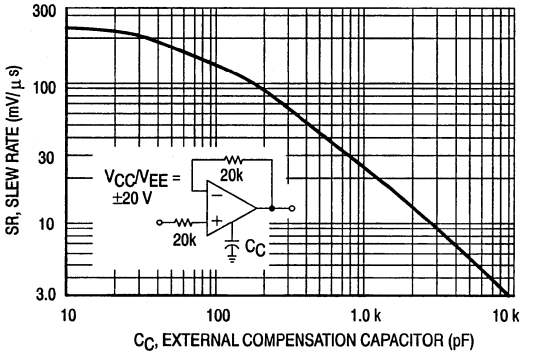
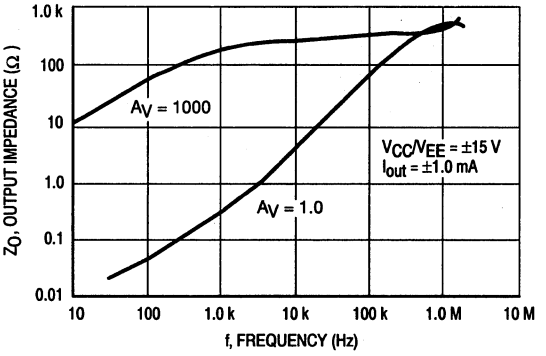


Figure 12. Slew Rate versus External Compensation Capacitor



2

Figure 13. Closed-Loop Output Impedance versus Frequency



APPLICATIONS INFORMATION

Due to the extremely low input bias currents of this device, it may be tempting to remove the bias current compensation resistor normally associated with a summing amplifier configuration. Direct connection of the inputs to a low impedance source or ground should be avoided when supply voltages greater than approximately 3.0 V are used. The potential problem involves reversal of one supply which can cause excessive current to flow in the second supply. Possible destruction of the IC could result if the second supply is not current limited to approximately 100 mA or if bypass capacitors greater than 1.0 µF are used in the supply bus.

Disconnecting one supply will generally cause reversal due to loading of the other supply within the IC and in external circuitry. Although the problem can usually be avoided by placing clamp diodes across the power supplies of each printed circuit board, a careful design will include sufficient resistance in the input leads to limit the current to 10 mA if the input leads are pulled to either supply by internal currents. This precaution is not limited to only the LM11C.

The LM11C is capable of resolving picoampere level signals. Leakage currents external to the IC can severely impair the performance of the device. It is important that high quality insulating materials such as teflon be employed. Proper cleaning to remove fluxes and other residues from printed circuit boards, sockets and the device package are necessary to minimize surface leakage.

When operating in high humidity environments or temperatures near 0°C, a surface coating is suggested to set up a moisture barrier.

Leakage effects on printed circuit boards can be reduced by encircling the inputs (both sides of pc board) with a conductive guard ring connected to a low impedance potential nearly the same as that of the inputs.

Guard ring electrical connections for common operational amplifier configurations are illustrated in Figure 14. Electrostatic shielding is suggested in high impedance circuits.

Error voltages in external circuitry can be generated by thermocouple effects. Dissimilar metals along with temperature gradients can set up an error voltage ranging in the hundreds of microvolts. Some of the best thermocouples are junctions of dissimilar metals made up of IC package pins and printed circuit boards. Problems can be avoided by keeping low level circuitry away from heat generating elements.

The LM11C is internally compensated, but external compensation can be added to improve stability, particularly when driving capacitive loads.

Figure 14. Guard Ring Electrical Connections for Common Amplifier Configurations

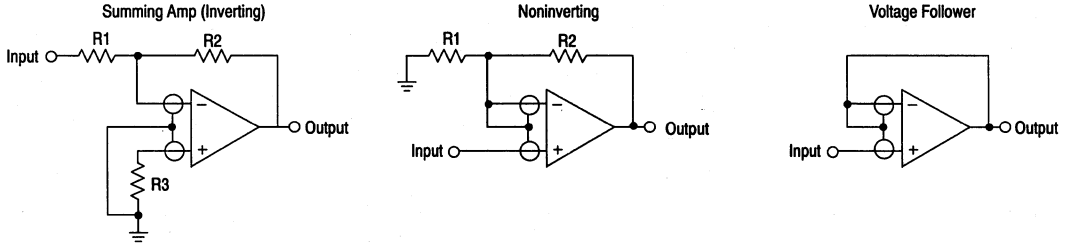
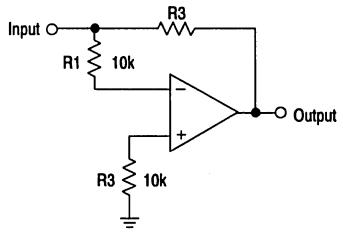
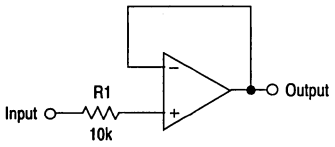


Figure 15. Input Protection for Summing (Inverting) Amplifier



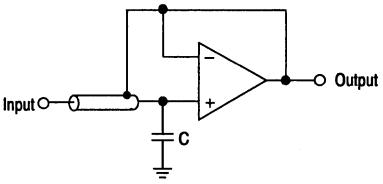
Current is limited by R1 in the event the input is connected to a low impedance source outside the common mode range of the device. Current is controlled by R2 if one supply reverses. R1 and R2 do not affect normal operation.

Figure 16. Input Protection for a Voltage Follower

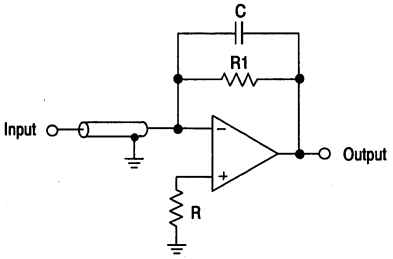


Input current is limited by R1 when the input exceeds supply voltage, power supply is turned off, or output is shorted.

Figure 17. Cable Boot Strapping and Input Shields

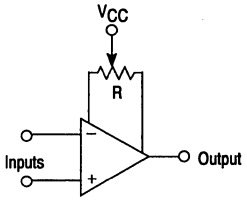


An input shield boot strapped in a voltage follower reduces input capacitance, leakage, and spurious voltages from cable flexing. A small capacitor from the input to ground will prevent any instability.



In a summing amplifier the input is at virtual ground. Therefore the shield can be grounded. A small feedback capacitor will insure stability.

Figure 18. Adjusting Input Offset Voltage with Balance Potentiometer



Minimum Adjustment Range (mV)	R (Ω)
±0.4	1.0 k
±1.0	3.0 k
±2.0	10 k
±5.0	100 k

Input offset voltage adjustment range is a function of the Balance Potentiometer Resistance as indicated by the table above. The potentiometer is connected between the two "Balance" pins.

LM101A
LM201A
LM301A

OPERATIONAL AMPLIFIER

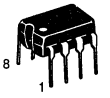
SILICON MONOLITHIC INTEGRATED CIRCUIT

Operational Amplifier

A general purpose operational amplifier that allows the user to choose the compensation capacitor best suited to his needs. With proper compensation, summing amplifier slew rates to 10 V/μs can be obtained.

- Low Input Offset Current: 20 nA Maximum OverTemperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short Circuit Protection
- Guaranteed Drift Characteristics

N SUFFIX
PLASTIC PACKAGE
CASE 626
(LM201A and LM301A)



J SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

Figure 1. Standard Compensation and Offset Balancing Circuit

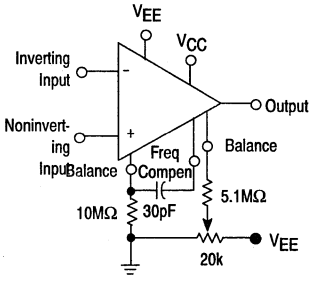
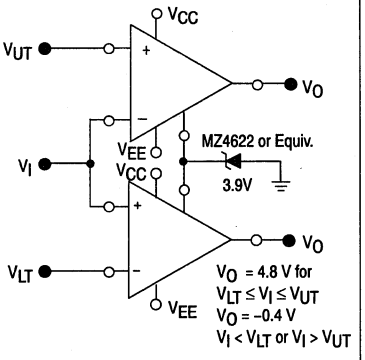
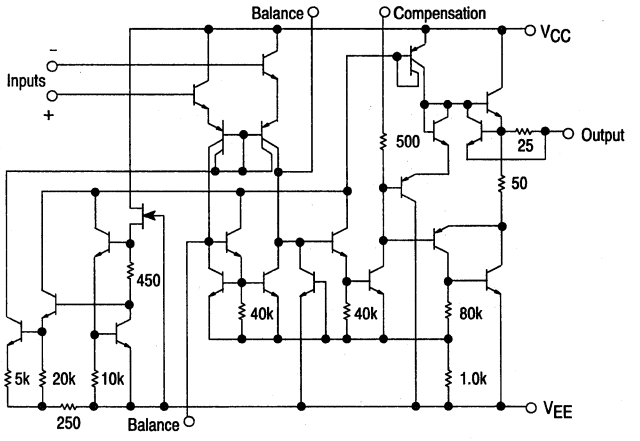


Figure 2. Double-Ended Limit Detctor

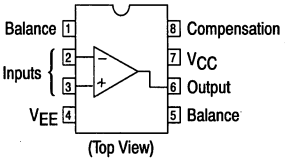


(Pins Not Shown Are Not Connected)

Figure 3. Representative Circuit Schematic



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
LM101AJ	−55° to +125°C	Ceramic DIP
LM201AD LM201AN LM201AJ	−25° to +85°C	SO-8 Plastic DIP Ceramic DIP
LM301AD LM301AN LM301AJ	0° to +70°C	SO-8 Plastic DIP Ceramic DIP

MAXIMUM RATINGS

Rating	Symbol	VALUE LM101A	VALUE LM201A	VALUE LM301A	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±22	±22	±18	Vdc
Input Differential Voltage	V_{ID}	←——— ±30 ———→			V
Input Common Mode Range (Note 1)	V_{ICR}	←——— ±15 ———→			V
Output Short Circuit Duration	t_{SC}	←——— Continuous ———→			
Power Dissipation (Package Limitation)	P_D				
Plastic Dual-In-Line Package (LM201A/		—	625	625	mW
Derate above T_A = +25°C 301A)		—	5.0	5.0	mW/°C
Ceramic Package (LM101A)		←——— 750 ———→			mW
Derate above 25°C		←——— 6.6 ———→			mW/°C
Operating Ambient Temperature Range	T_A	–55 to +125	–25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	←——— –65 to +150 ———→			°C

Note: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, unless otherwise noted.) Unless otherwise specified, these specifications apply for supply voltages from ±5.0 V to ±20 V for the LM101A and LM201A, and from ±5.0 V to ±15 V for the LM301A.

Characteristics	Symbol	LM101A LM201A Min	Typ	Max	LM301A Min	Typ	Max	Unit
Input Offset Voltage (R_S ≤ 50 kΩ)	V_{IO}	—	0.7	2.0	—	2.0	7.5	mV
Input Offset Current	I_{IO}	—	1.5	10	—	3.0	50	nA
Input Bias Current	I_{IB}	—	30	75	—	70	250	nA
Input Resistance	r_i	1.5	4.0	—	0.5	2.0	—	MΩ
Supply Current	I_{CC},I_{EE}							mA
V_{CC}/V_{EE} = ±20 V		—	1.8	3.0	—	—	—	
V_{CC}/V_{EE} = ±15 V		—	—	—	—	1.8	3.0	
Large Signal Voltage Gain (V_{CC}/V_{EE} = ±15 V, V_O = ±10 V, R_L > 2.0 kΩ)	A_V	50	160	—	25	160	—	V/mV
The following specifications apply over the operating temperature range.								
Input Offset Voltage (R_S ≤ 50 kΩ)	V_{IO}	—	—	3.0	—	—	10	mV
Input Offset Current	I_{IO}	—	—	20	—	—	70	nA
Avg Temperature Coefficient of Input Offset Voltage T_A(min) ≤ T_A ≤ T_A (max)	$\Delta V_{IO}/\Delta T$	—	3.0	15	—	6.0	30	µV/°C
Avg Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$							nA/°C
+25°C ≤ T_A ≤ T_A (max)		—	0.01	0.1	—	0.01	0.3	
T_A(min) ≤ T_A ≤ 25°C		—	0.02	0.2	—	0.02	0.6	
Input Bias Current	I_{IB}	—	—	100	—	—	300	nA
Large Signal Voltage Gain (V_{CC}/V_{EE} = ±15 V, V_O = ±10V, R_L > 2.0 kΩ)	A_{VOL}	25	—	—	15	—	—	V/mV
Input Voltage Range	V_{ICR}							V
V_{CC}/V_{EE} = ±20 V		–15	—	+15	—	—	—	
V_{CC}/V_{EE} = ±15 V		—	—	—	–12	—	+12	
Common Mode Rejection (R_S ≤ 50 kΩ)	CMR	80	96	—	70	90	—	dB
Supply Voltage Rejection (R_S ≤ 50 kΩ)	PSR	80	96	—	70	96	—	dB
Output Voltage Swing	V_O							V
(V_{CC}/V_{EE} = ±15 V, R_L = ±10 kΩ, R_L > 2.0 kΩ)		±12	±14	—	±12	±14	—	
		±10	±13	—	±10	±13	—	
Supply Currents (T_A = T_A(max), V_{CC}/V_{EE} = ±20 V)	I_{CC},I_{EE}	—	1.2	2.5	—	—	—	mA

2

Figure 4. Minimum Input Voltage Range

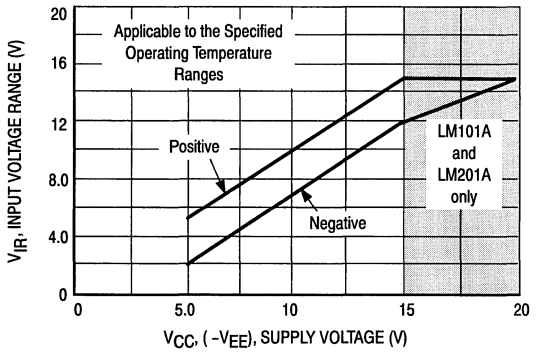


Figure 5. Minimum Output Voltage Swing

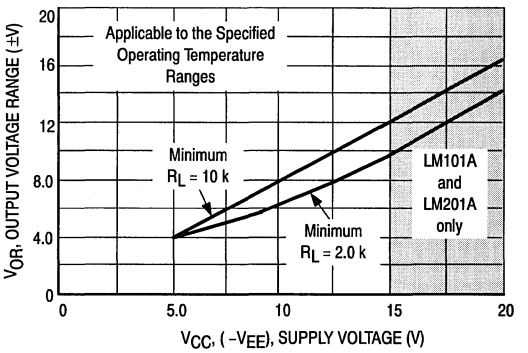


Figure 6. Minimum Voltage Gain

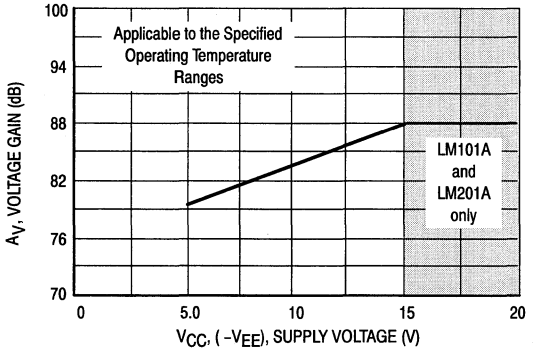


Figure 7. Typical Supply Currents

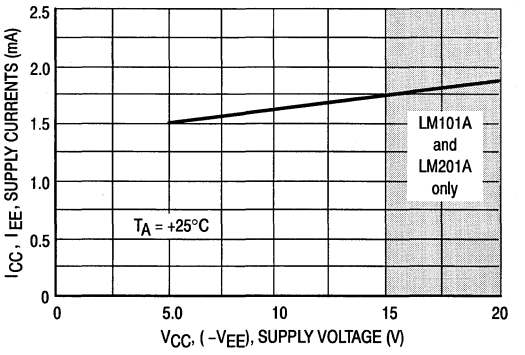


Figure 8. Open-Loop Frequency Response

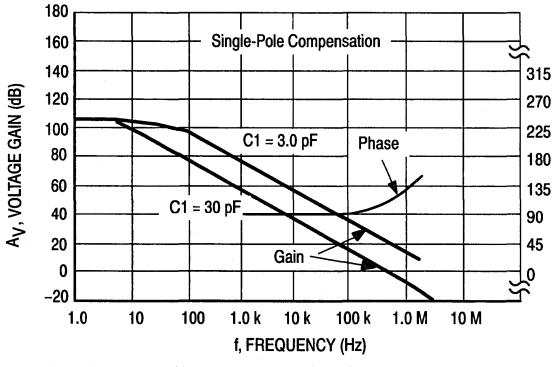


Figure 9. Large Signal Frequency Response

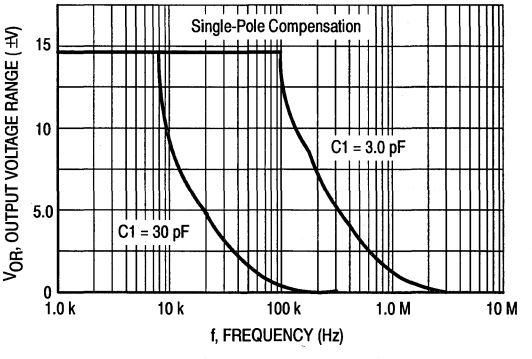


Figure 10. Voltage Follower Pulse Response

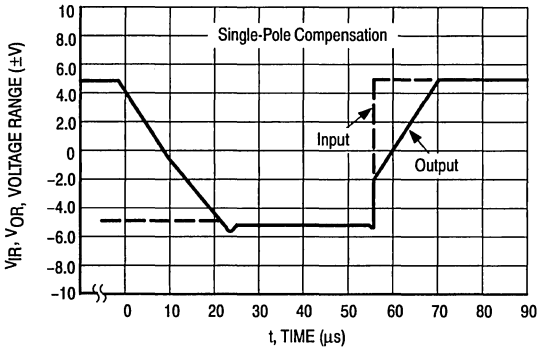


Figure 11. Open-Loop Frequency Response

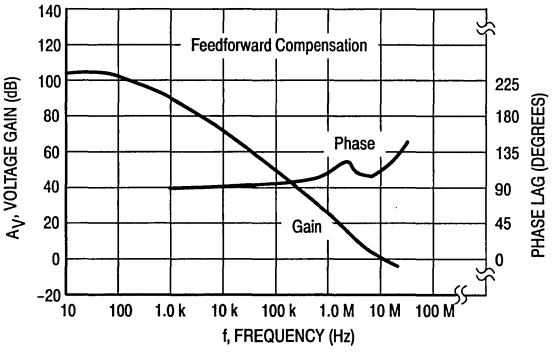


Figure 12. Large Signal Frequency Response

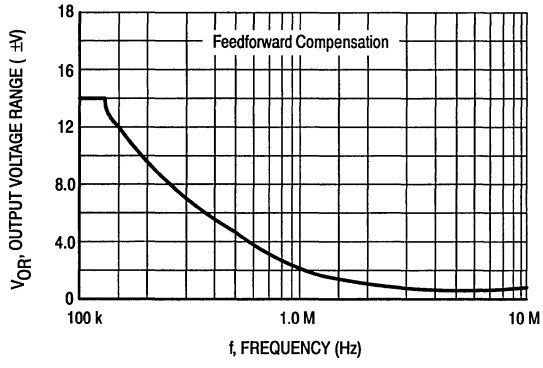


Figure 13. Inverter Pulse Response

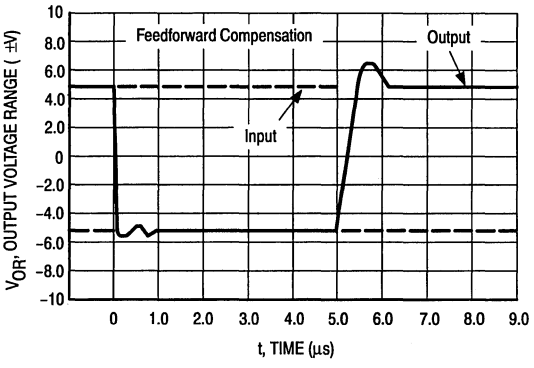


Figure 14. Single-Pole Compensation

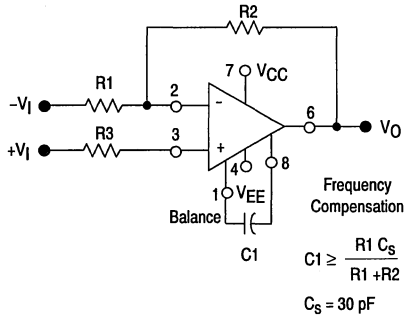
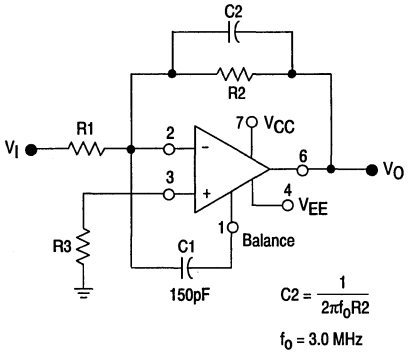


Figure 15. Feedforward Compensation



LM111
LM211
LM311

HIGH PERFORMANCE VOLTAGE COMPARATORS

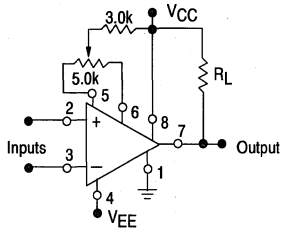
SILICON MONOLITHIC INTEGRATED CIRCUIT

Highly Flexible Voltage Comparators

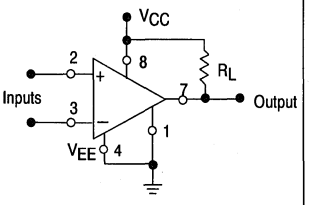
The ability to operate from a single power supply of 5.0 V to 30 V or ±15 V split supplies, as commonly used with operational amplifiers, makes the LM111/LM211/LM311 a truly versatile comparator. Moreover, the inputs of the device can be isolated from system ground while the output can drive loads referenced either to ground, the V_{CC} or the V_{EE} supply. This flexibility makes it possible to drive DTL, RTL, TTL, or MOS logic. The output can also switch voltages to 50 V at currents to 50 mA. Thus the LM111/LM211/LM311 can be used to drive relays, lamps or solenoids.

Typical Comparator Design Configurations

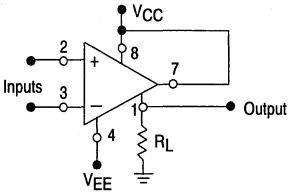
Split Power Supply with Offset Balance



Single Supply

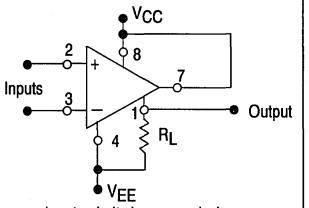


Ground-Referred Load



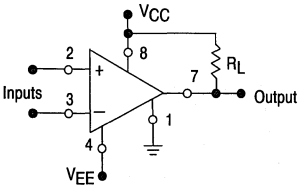
Input polarity is reversed when Gnd pin is used as an output.

Load Referred to Negative Supply

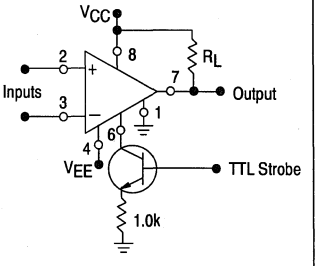


Input polarity is reversed when Gnd pin is used as an output.

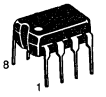
Load Referred to Positive Supply



Strobe Capability



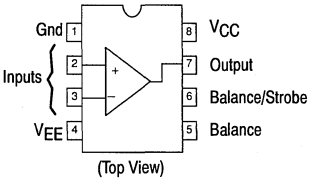
N SUFFIX
PLASTIC PACKAGE
CASE 626



J-8 SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
LM111J-8	–55° to +125°C	Ceramic DIP
LM211D LM211J-8	–25° to +85°C	SO-8 Ceramic DIP
LM311D LM311J-8 LM311N	0° to +70°C	SO-8 Ceramic DIP Plastic DIP

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	LM111/LM211	LM311	Unit
Total Supply Voltage	V_{CC} + $\|V_{EE}\|$	36	36	Vdc
Output to Negative Supply Voltage	V_O –V_{EE}	50	40	Vdc
Ground to Negative Supply Voltage	V_{EE}	30	30	Vdc
Input Differential Voltage	V_{ID}	±30	±30	Vdc
Input Voltage (Note 2)	V_{in}	±15	±15	Vdc
Voltage at Strobe Pin	—	V_{CC} to V_{CC}–5	V_{CC} to V_{CC}–5	Vdc
Power Dissipation and Thermal Characteristics Plastic and Ceramic Dual-In-Line Packages Derate Above T_A = +25°C	 P_D $1/\theta_{JA}$	 625 5.0		 mW mW/°C
Operating Ambient Temperature Range	T_A	 –55 to +125 –25 to +85 —	 — — 0 to +70	°C
Operating Junction Temperature	$T_{J(max)}$	+150	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted [Note 1].)

Characteristics	Symbol	LM111/LM211			LM311			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 3) $R_S \leq$ 50 kΩ, T_A = +25°C $R_S \leq$ 50 kΩ, $T_{low} \leq T_A \leq T_{high}$*	V_{IO}	 — —	 0.7 —	 3.0 4.0	 — —	 2.0 —	 7.5 10	mV
Input Offset Current (Note 3) T_A = +25°C $T_{low} \leq T_A \leq T_{high}$*	I_{IO}	— —	1.7 —	10 20	— —	1.7 —	50 70	nA
Input Bias Current T_A = +25°C $T_{low} \leq T_A \leq T_{high}$*	I_{IB}	— —	45 —	100 150	— —	45 —	250 300	nA
Voltage Gain	A_V	40	200	—	40	200	—	V/mV
Response Time (Note 4)		—	200	—	—	200	—	ns
Saturation Voltage $V_{ID} \leq$ –5.0 mV, I_O = 50 mA, T_A = 25°C $V_{ID} \leq$–10 mV, I_O = 50 mA, T_A = 25°C $V_{CC} \geq$ 4.5 V, V_{EE} = 0, $T_{low} \leq T_A \leq T_{high}$* $V_{ID} \geq$6.0 mV, $I_{sink} \leq$ 8.0 mA $V_{ID} \geq$10 mV, $I_{sink} \leq$ 8.0 mA	V_{OL}	 — — — —	 0.75 — 0.23 —	 1.5 — 0.4 —	 — — — —	 — 0.75 — 0.23	 — 1.5 — 0.4	V
Strobe "On" Current (Note 5)	I_S	—	3.0	—	—	3.0	—	mA
Output Leakage Current $V_{ID} \geq$ 5.0 mV, V_O= 35 V, T_A = 25°C, I_{strobe}= 3.0 mA $V_{ID} \geq$ 10 mV, V_O= 35 V, T_A = 25°C, I_{strobe}= 3.0 mA $V_{ID} \geq$ 5.0 mV, V_O= 35 V, $T_{low} \leq T_A \leq T_{high}$*		 — — —	 0.2 — 0.1	 10 — 0.5	 — — —	 — 0.2 —	 — 50 —	 nA nA µA
Input Voltage Range ($T_{low} \leq T_A \leq T_{high}$*)	V_{ICR}	–14.5	–14.7 to 13.8	+13.0	–14.5	–14.7 to 13.8	+13.0	V
Positive Supply Current	I_{CC}	—	+2.4	+6.0	—	+2.4	+7.5	mA
Negative Supply Current	I_{EE}	—	–1.3	–5.0	—	–1.3	–5.0	mA

* T_{low} = –55°C for LM111 = –25°C for LM211 = 0°C for LM311 T_{high} = +125°C for LM111 = +85°C for LM211 = +70°C for LM311

NOTES: 1. Offset voltage, offset current and bias current specifications apply for a supply voltage range from a single 5.0 V supply up to ±15 V supplies.

2. This rating applies for ±15 V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
3. The Offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the "worst case" effects of voltage gain and input impedance.
4. The response time specified is for a 100 mV input step with 5.0 mV overdrive.
5. Do not short the strobe pin to ground; it should be current driven at 3.0 mA to 5.0 mA.

2

Figure 1. Circuit Schematic

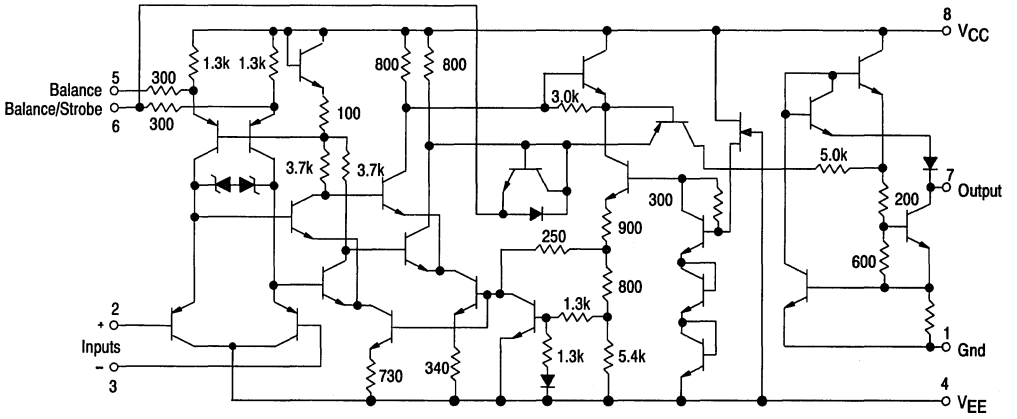


Figure 2. Input Bias Current versus Temperature

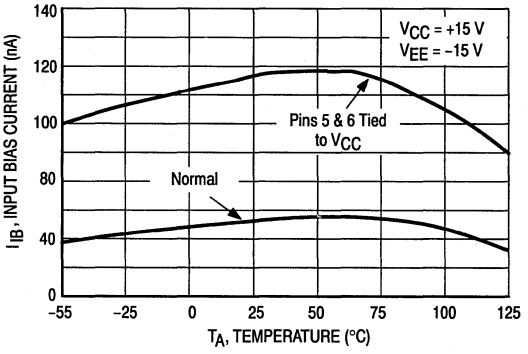


Figure 3. Input Offset Current versus Temperature

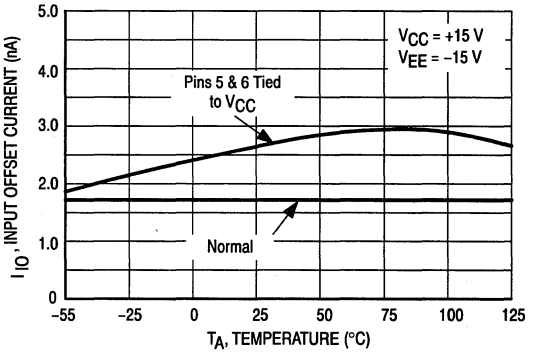


Figure 4. Input Bias Current versus Differential Input Voltage

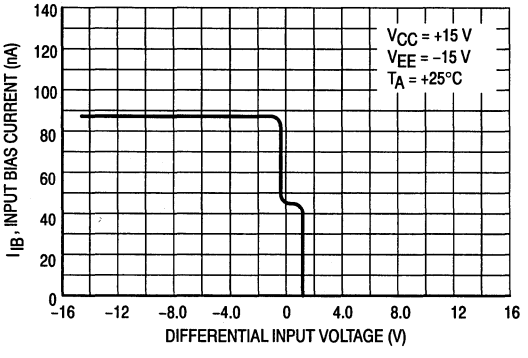


Figure 5. Common Mode Limits versus Temperature

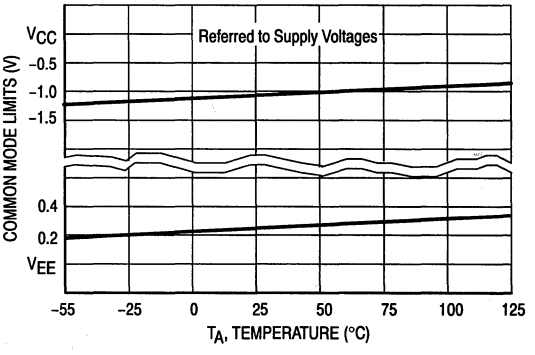


Figure 6. Response Time for Various Input Overdrives

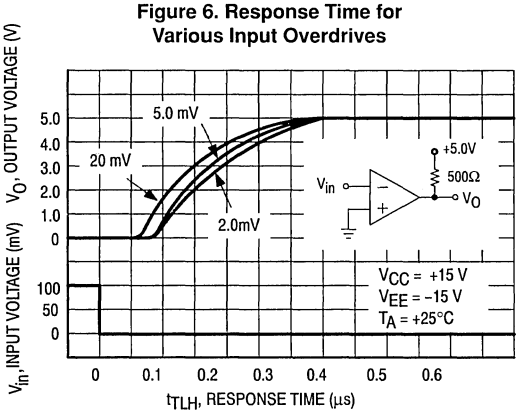


Figure 7. Response Time for Various Input Overdrives

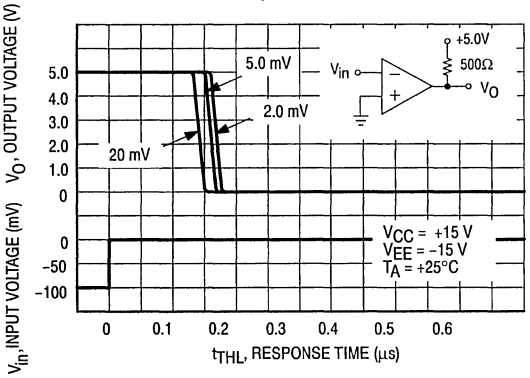


Figure 8. Response Time for Various Input Overdrives

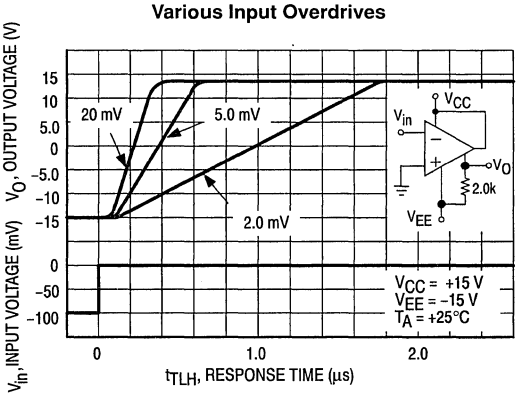


Figure 9. Response Time for Various Input Overdrives

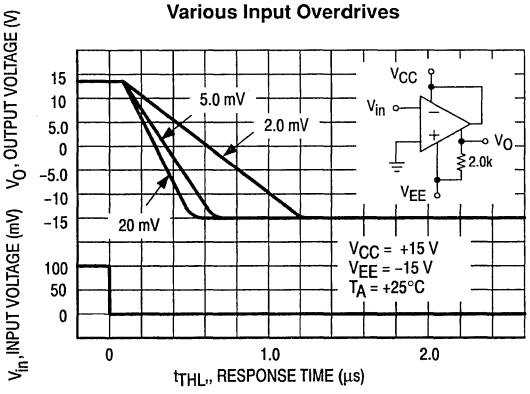


Figure 10. Output Short Circuit Current Characteristics and Power Dissipation

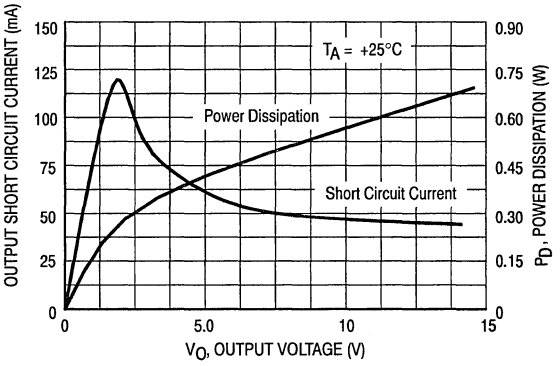
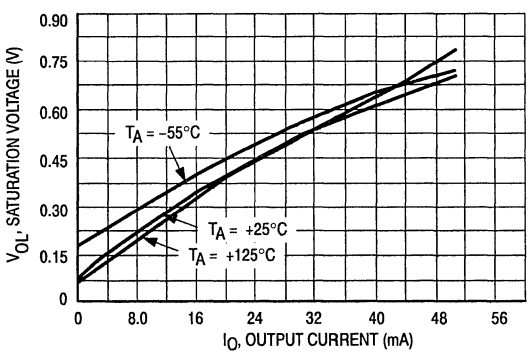


Figure 11. Output Saturation Voltage versus Output Current



2

Figure 12. Output Leakage Current versus Temperature

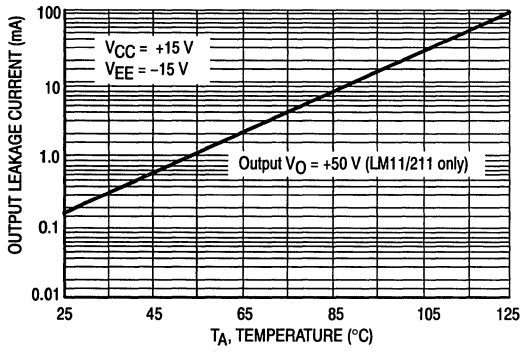


Figure 13. Power Supply Current versus Supply Voltage

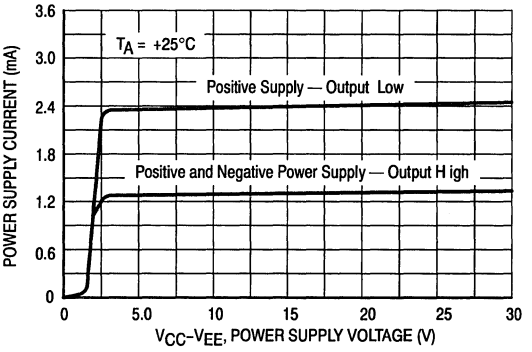
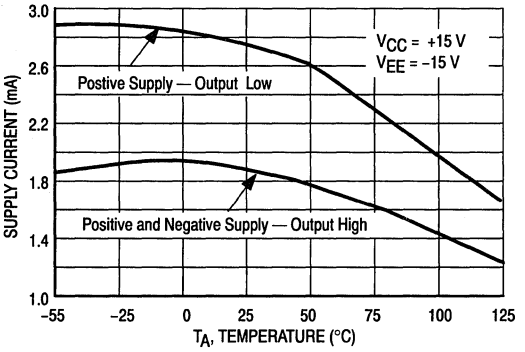


Figure 14. Power Supply Current versus Temperature



APPLICATIONS INFORMATION

Figure 15. Improved Method of Adding Hysteresis Without Applying Positive Feedback to the Inputs

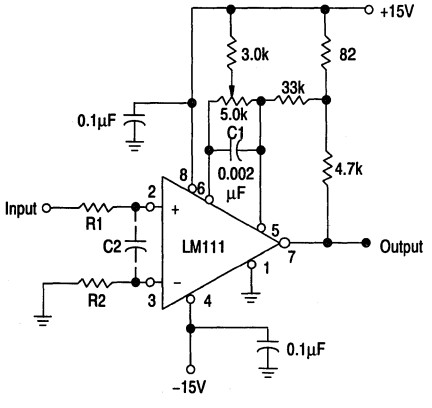
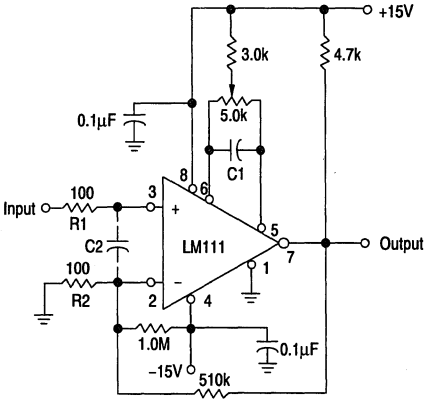


Figure 16. Conventional Technique for Adding Hysteresis



TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high speed comparator such as the LM111 is used with high speed input signals and low source impedances, the output response will normally be fast and stable, providing the power supplies have been bypassed (with 0.1 µF disc capacitors), and that the output signal is routed well away from the inputs (Pins 2 and 3) and also away from Pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1.0 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111 series. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 15.

The trim pins (Pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 µF capacitor (C1) between Pins 5 and 6 will minimize the susceptibility to ac coupling. A smaller capacitor is used if Pin 5 is used for positive feedback as in Figure 15.

Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor (C2) is connected directly across the input pins. When the signal source is applied through a resistive network, R1, it is usually advantageous to choose R2 of the same value, both for dc and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used with good results in comparator input circuitry, but inductive wirewound resistors should be avoided.

When comparator circuits use input resistors (e.g., summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words, there should be a very short lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R1 = 10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to dampen, Twisting these input leads tightly is the best alternative to placing resistors close to the comparator.

Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry (e.g., one side of a double layer printed circuit board). Ground, positive supply or negative supply foil should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any fast high-level signals (such as the output). If Pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located no more than a few inches away from the LM111, and a 0.01 µF capacitor should be installed across Pins 5 and 6. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between Pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111.

A standard procedure is to add hysteresis to a comparator to prevent oscillation, and to avoid excessive noise on the output. In the circuit of Figure 16, the feedback resistor of 510 kΩ from the output to the positive input will cause about 3.0 mV of hysteresis. However, if R2 is larger than 100 Ω, such as 50 kΩ, it would not be practical to simply increase the value of the positive feedback resistor proportionally above 510 kΩ to maintain the same amount of hysteresis.

When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of Figure 15 is ideal. The positive feedback is applied to Pin 5 (one of the offset adjustment pins). This will be sufficient to cause 1.0 mV to 2.0 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82 Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at Pin 5, so this feedback does not add to the offset voltage of the comparator. As much as 8.0 mV of offset voltage can be trimmed out, using the 5.0 kΩ pot and 3.0 kΩ resistor as shown.

Figure 17. Zero-Crossing Detector Driving CMOS Logic

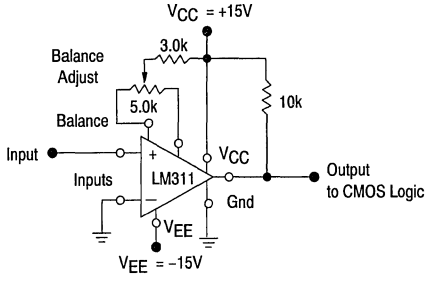
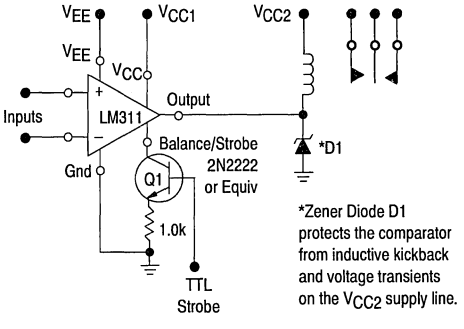


Figure 18. Relay Driver with Strobe Capability



LM124, LM224, LM324, LM324A, LM2902

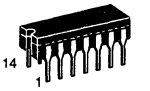
QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

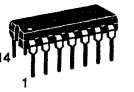
Quad Low Power Operational Amplifiers

The LM124 series are low-cost, quad operational amplifiers with true differential inputs. These have several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 V or as high as 32 V with quiescent currents about one fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuited Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V
- Low Input Bias Currents: 100 nA Max (LM324A)
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Industry Standard Pinouts
- ESD Clamps on the Inputs Increase Ruggedness without Affecting Device Operation



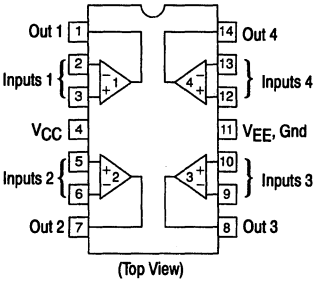
J SUFFIX
CERAMIC PACKAGE
CASE 632



N SUFFIX
PLASTIC PACKAGE
CASE 646
(LM224, LM324, LM2902 Only)

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	LM124 LM224 LM324,A	LM2902	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 32 ±16	 26 ±13	Vdc
Input Differential Voltage Range (1)	V_{IDR}	±32	±26	Vdc
Input Common Mode Voltage Range	V_{ICR}	–0.3 to 32	–0.3 to 26	Vdc
Output Short Circuit Duration	t_{SC}	Continuous		
Junction Temperature Ceramic Package Plastic Packages	T_J	 175 150		°C
Storage Temperature Range Ceramic Package Plastic Packages	T_{stg}	 –65 to +150 –55 to +125		°C
Operating Ambient Temperature Range	T_A	 –55 to +125 –25 to +85 0 to +70 —	 — — — –40 to +105	°C

NOTE: 1. Split Power Supplies.

ORDERING INFORMATION

Device	Temperature Range	Package
LM124J	–55° to +125°C	Ceramic DIP
LM2902D	–40° to +105°C	SO-14
LM2902N		Plastic DIP
LM2902J	–40° to +85°C	Ceramic DIP
LM224D	–25° to +85°C	SO-14
LM224J		Ceramic DIP
LM224N		Plastic DIP
LM324AD	0° to +70°C	SO-14
LM324AN		Plastic DIP
LM324D		SO-14
LM324J		Ceramic DIP
LM324N		Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = GND, T_A = 25°C, unless otherwise noted.)

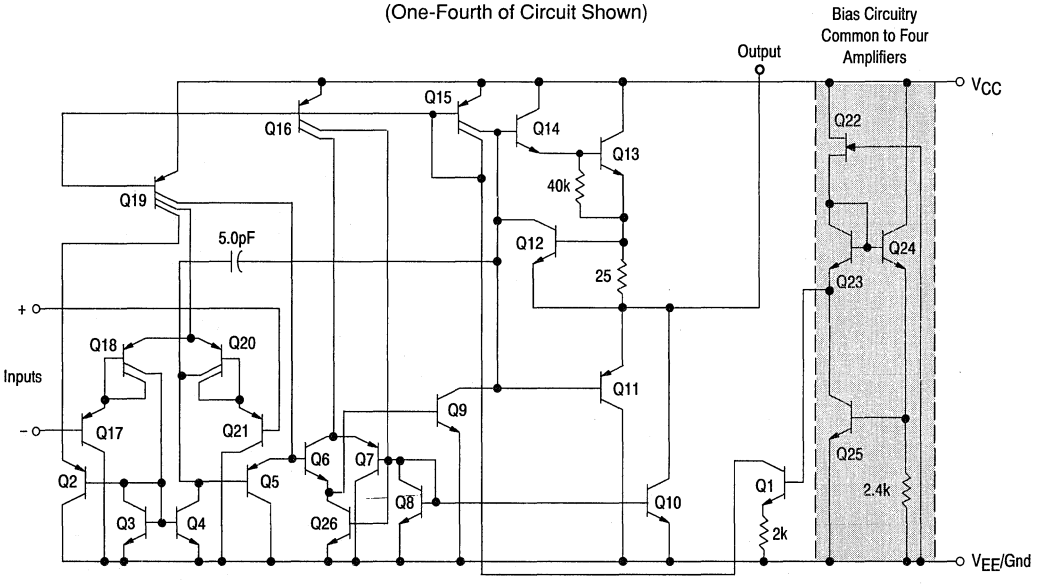
Characteristics	Symbol	LM124/LM224			LM324A			LM324			LM2902			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage V_{CC} = 5.0 V to 30 V (26 V for LM2902), V_{ICR} = 0 V to V_{CC} –1.7 V, V_O = 1.4 V, R_S = 0 Ω	V_{IO}													mV
T_A = 25°C		—	2.0	5.0	—	2.0	3.0	—	2.0	7.0	—	2.0	7.0	
T_A = T_{high} to T_{low} (Note 1)		—	—	7.0	—	—	5.0	—	—	9.0	—	—	10	
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low} (Note 1)	$\Delta V_{IO}/\Delta T$	—	7.0	—	—	7.0	30	—	7.0	—	—	7.0	—	μV/°C
Input Offset Current	I_{IO}	—	3.0	30	—	5.0	30	—	5.0	50	—	5.0	50	nA
T_A = T_{high} to T_{low} (Note 1)		—	—	100	—	—	75	—	—	150	—	—	200	
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low} (Note 1)	$\Delta I_{IO}/\Delta T$	—	10	—	—	10	300	—	10	—	—	10	—	pA/°C
Input Bias Current	I_{IB}	—	–90	–150	—	–45	–100	—	–90	–250	—	–90	–250	nA
T_A = T_{high} to T_{low} (Note 1)		—	—	–300	—	—	–200	—	—	–500	—	—	–500	
Input Common Mode Voltage Range (Note 2)	V_{ICR}													V
V_{CC} = 30 V (26 V for LM2902)		0	—	28.3	0	—	28.3	0	—	28.3	0	—	24.3	
V_{CC} = 30 V (26 V for LM2902), T_A = T_{high} to T_{low}		0	—	28	0	—	28	0	—	28	0	—	24	
Differential Input Voltage Range	V_{IDR}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	V
Large Signal Open-Loop Voltage Gain	A_{VOL}													V/mV
R_L = 2.0 kΩ, V_{CC} = 15 V, for Large V_O Swing,		50	100	—	25	100	—	25	100	—	25	100	—	
T_A = T_{high} to T_{low} (Note 1)		25	—	—	15	—	—	15	—	—	15	—	—	
Channel Separation 10 kHz ≤ f ≤ 20 kHz, Input Referenced	CS	—	–120	—	—	–120	—	—	–120	—	—	–120	—	dB
Common Mode Rejection R_S ≤ 10 kΩ	CMR	70	85	—	65	70	—	65	70	—	50	70	—	dB
Power Supply Rejection	PSR	65	100	—	65	100	—	65	100	—	50	100	—	dB
Output Voltage—High Limit (T_A = T_{high} to T_{low}) (Note 1)	V_{OH}													V
V_{CC} = 5.0 V, R_L = 2.0 kΩ, T_A = 25°C		3.3	3.5	—	3.3	3.5	—	3.3	3.5	—	3.3	3.5	—	
V_{CC} = 30 V (26 V for LM2902), R_L = 2.0 kΩ		26	—	—	26	—	—	26	—	—	22	—	—	
V_{CC} = 30 V (26 V for LM2902), R_L = 10 kΩ		27	28	—	27	28	—	27	28	—	23	24	—	
Output Voltage — Low Limit V_{CC} = 5.0 V, R_L = 10 kΩ, T_A = T_{high} to T_{low} (Note1)	V_{OL}	—	5.0	20	—	5.0	20	—	5.0	20	—	5.0	100	mV
Output Source Current (V_{ID} = +1.0 V, V_{CC} = 15 V)	I_{O+}													mA
T_A = 25°C		20	40	—	20	40	—	20	40	—	20	40	—	
T_A = T_{high} to T_{low} (Note 1)		10	20	—	10	20	—	10	20	—	10	20	—	
Output Sink Current	I_{O-}													mA
(V_{ID} = –1.0 V, V_{CC} = 15 V)														
T_A = 25°C		10	20	—	10	20	—	10	20	—	10	20	—	
T_A = T_{high} to T_{low} (Note 1)		5.0	8.0	—	5.0	8.0	—	5.0	8.0	—	5.0	8.0	—	
(V_{ID} = –1.0 V, V_O = 200 mV, T_A = 25°C)		12	50	—	12	50	—	12	50	—	—	—	—	μA
Output Short Circuit to Ground (Note 3)	I_{SC}	—	40	60	—	40	60	—	40	60	—	40	60	mA
Power Supply Current (T_A = T_{high} to T_{low}) (Note 1)	I_{CC}													mA
V_{CC} = 30 V (26 V for LM2902), V_O = 0 V, R_L = ∞		—	—	3.0	—	1.4	3.0	—	—	3.0	—	—	3.0	
V_{CC} = 5.0 V, V_O = 0 V, R_L = ∞		—	—	1.2	—	0.7	1.2	—	—	1.2	—	—	1.2	

NOTES: 1. T_{low} = –55°C for LM124 T_{high} = +125°C for LM124
= –25°C for LM224 = +85°C for LM224
= 0°C for LM324, A = +70°C for LM324,A
= –40°C for LM2902 = +105°C for LM2902

2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} –1.7 V.
3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

2

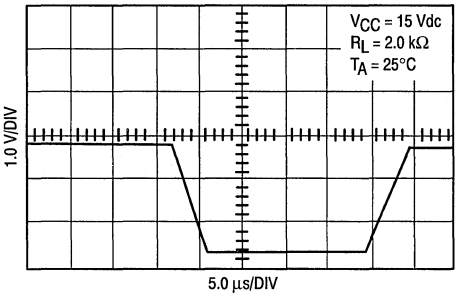
Representative Circuit Schematic
(One-Fourth of Circuit Shown)



CIRCUIT DESCRIPTION

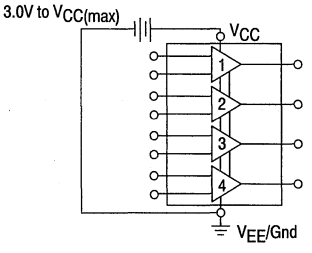
The LM124 series is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Large Signal Voltage Follower Response



Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

Single Supply



Split Supplies

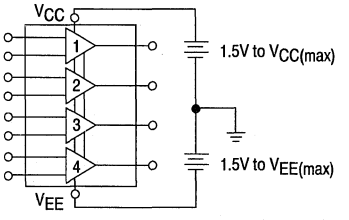


Figure 1. Input Voltage Range

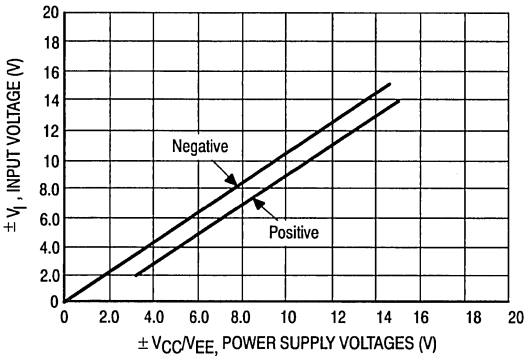


Figure 2. Open-Loop Frequency

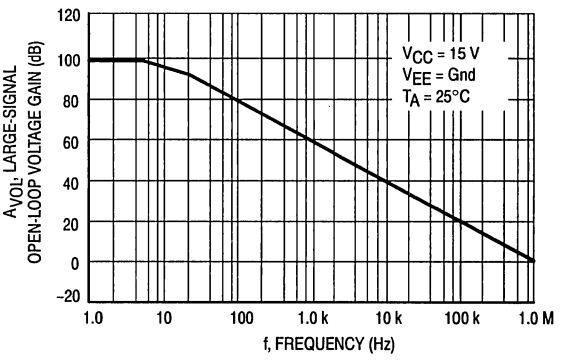


Figure 3. Large-Signal Frequency Response

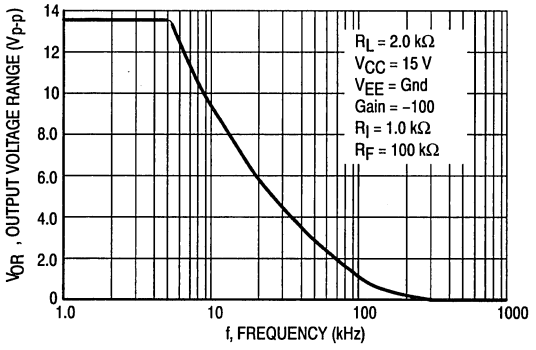


Figure 4. Small-Signal Voltage Follower Pulse Response (Noninverting)

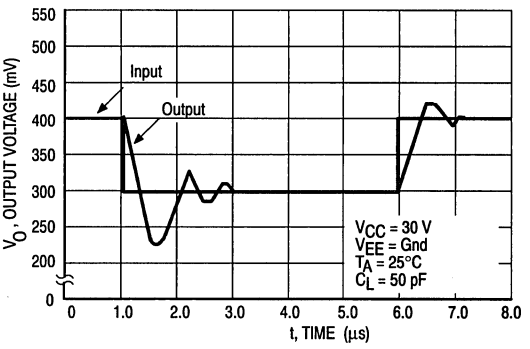


Figure 5. Power Supply Current versus Power Supply Voltage

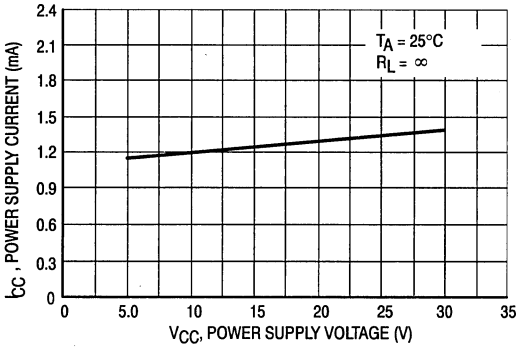
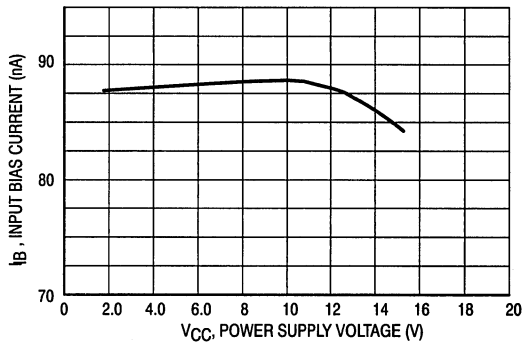
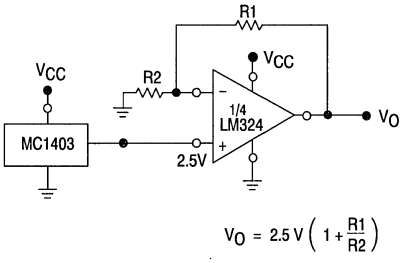


Figure 6. Input Bias Current versus Power Supply Voltage



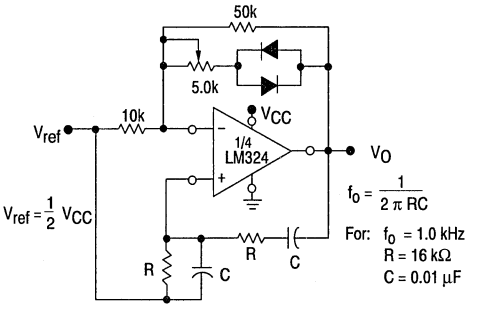
2

Figure 7. Voltage Reference



$$V_O = 2.5\,V\left(1 + \frac{R1}{R2}\right)$$

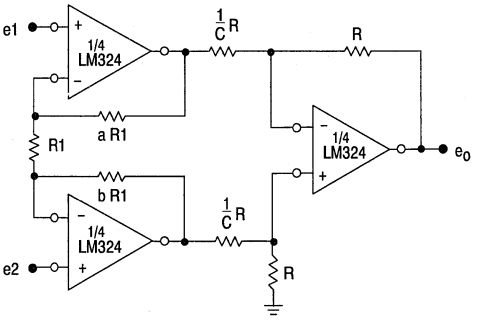
Figure 8. Wien Bridge Oscillator



$$f_o = \frac{1}{2\pi RC}$$

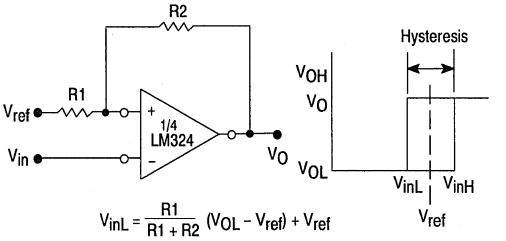
For: f_o = 1.0 kHz
R = 16 kΩ
C = 0.01 µF

Figure 9. High Impedance Differential Amplifier



$$e_o = C\,(1 + a + b)\,(e2 - e1)$$

Figure 10. Comparator with Hysteresis

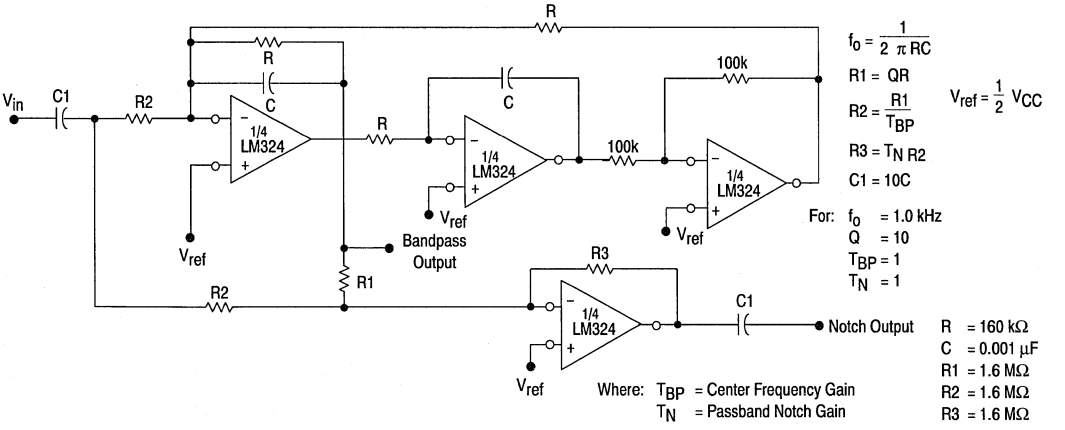


$$V_{inL} = \frac{R1}{R1 + R2}\,(V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2}\,(V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2}\,(V_{OH} - V_{OL})$$

Figure 11. Bi-Quad Filter



$$f_o = \frac{1}{2\pi RC}$$

R1 = QR

$$R2 = \frac{R1}{T_{BP}}$$

R3 = T_N R2

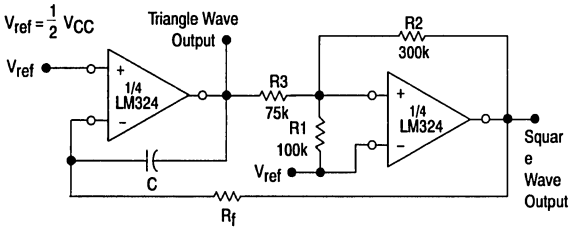
C1 = 10C

$$V_{ref} = \frac{1}{2}\,V_{CC}$$

For: f_o = 1.0 kHz
Q = 10
T_{BP} = 1
T_N = 1

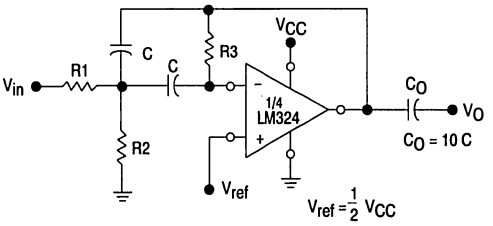
R = 160 kΩ
C = 0.001 µF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

Figure 12. Function Generator



$$f = \frac{R1 + R_C}{4 C R_f R1} \quad \text{if } R3 = \frac{R2\,R1}{R2 + R1}$$

Figure 13. Multiple Feedback Bandpass Filter



Given: f_0 = center frequency

$A(f_0)$ = gain at center frequency

Choose value f_0, C

Then:

$$R3 = \frac{Q}{\pi f_0 C}$$

$$R1 = \frac{R3}{2 A(f_0)}$$

$$R2 = \frac{R1\,R3}{4Q^2 R1 - R3}$$

For less than 10% error from operational amplifier,

$\frac{Q_0 f_0}{BW} < 0.1$ where f_0 and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

LM139,A LM239,A, LM2901, LM339,A, MC3302

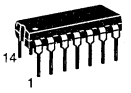
Quad Single Supply Comparators

These comparators are designed for use in level detection, low-level sensing and memory applications in consumer automotive and industrial electronic applications.

- Single or Split Supply Operation
- Low Input Bias Current: 25 nA (Typ)
- Low Input Offset Current: ±5.0 nA (Typ)
- Low Input Offset Voltage: ±1.0 mV (Typ) LM139A Series
- Input Common Mode Voltage Range to Gnd
- Low Output Saturation Voltage: 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible
- ESD Clamps on the Inputs Increase Reliability without Affecting Device Operation

QUAD COMPARATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT



N, P SUFFIX
PLASTIC PACKAGE
CASE 646

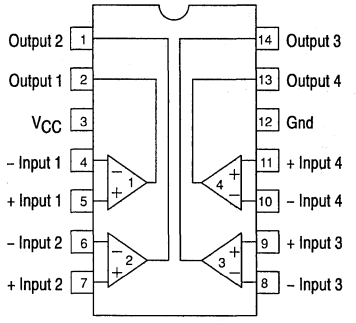
J, L SUFFIX
CERAMIC PACKAGE
CASE 632

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

MAXIMUM RATINGS

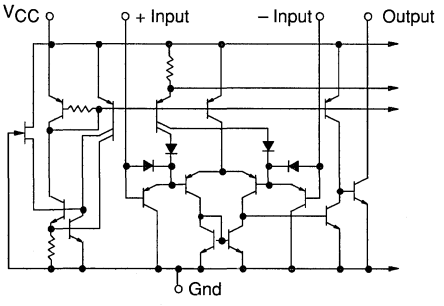
Rating	Symbol	Value	Unit
Power Supply Voltage LM139, A/LM239, A/LM339A/LM2901 MC3302	V_{CC}	 +36 or ±18 +30 or ±15	Vdc
Input Differential Voltage Range LM139, A/LM239, A/LM339, A/LM2901 MC3302	V_{IDR}	 36 30	Vdc
Input Common Mode Voltage Range	V_{ICMR}	−0.3 to V_{CC}	Vdc
Output Short Circuit to Ground (Note 1)	I_{SC}	Continuous	
Input Current (V_{in} < − 0.3 Vdc) (Note 2)	I_{in}	50	mA
Power Dissipation @ T_A = 25°C Ceramic Plastic Package Derate above 25°C	P_D	 1.0 8.0	 W mW/°C
Junction Temperature Ceramic & Metal Package Plastic Package	T_J	 175 150	°C
Operating Ambient Temperature Range LM139, A LM239, A MC3302 LM2901 LM339, A	T_A	 −55 to +125 −25 to +85 −40 to +85 −40 to +105 0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

PIN CONNECTIONS



(Top View)

Figure 1. Circuit Schematic



NOTE: Diagram shown is for 1 comparator.

ORDERING INFORMATION

Device	Temperature Range	Package
LM139J, AJ	−55° to +125°C	Ceramic DIP
LM239D, AD LM239J, AJ LM239N, AN	−25° to +85°C	SO-14 Ceramic DIP Plastic DIP
LM339D, AD LM339J, AJ LM339N, AN	0° to +70°C	SO-14 Ceramic DIP Plastic DIP
LM2901D LM2901N	−40° to +105°C	SO-14 Plastic DIP
MC3302L MC3302P	−40° to +85°C	Ceramic DIP Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = +25°C, unless otherwise noted)

Characteristics	Symbol	LM139A			LM239A/339A			LM139			LM239/339			LM2901			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	—	±1.0	±2.0	—	±1.0	±2.0	—	±2.0	±5.0	—	±2.0	±5.0	—	±2.0	±7.0	—	±3.0	±20	mVdc
Input Bias Current (Notes 4, 5) (Output in Linear Range)	I_{IB}	—	25	100	—	25	250	—	25	100	—	25	250	—	25	250	—	25	500	nA
Input Offset Current (Note 4)	I_{IO}	—	±3.0	±25	—	±5.0	±50	—	±3.0	±25	—	±5.0	±50	—	±5.0	±50	—	±3.0	±100	nA
Input Common Mode Voltage Range	V_{ICMR}	0	—	V_{CC} −1.5	0	—	V_{CC} −1.5	0	—	V_{CC} −1.5	0	—	V_{CC} −1.5	0	—	V_{CC} −1.5	0	—	V_{CC} −1.5	V
Supply Current R_L = ∞ (For All Comparators) R_L = ∞, V_{CC} = 30 Vdc	I_{CC}	— —	0.8 1.0	2.0 2.5	— —	0.8 1.0	2.0 2.5	— —	0.8 1.0	2.0 2.5	— —	0.8 1.0	2.0 2.5	— —	0.8 1.0	2.0 2.5	— —	0.8 1.0	2.0 2.5	mA
Voltage Gain R_L ≥ 15 kΩ, V_{CC} = 15 Vdc	A_{VOL}	50	200	—	50	200	—	—	200	—	—	200	—	25	100	—	2	30	—	V/mV
Large Signal Response Time V_I = TTL Logic Swing, V_{ref} = 1.4 Vdc, V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	—	—	300	—	—	300	—	—	300	—	—	300	—	—	300	—	—	300	—	ns
Response Time (Note 6) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	—	1.3	—	µs
Output Sink Current $V_I(-)$ ≥ +1.0 Vdc, $V_I(+)$ = 0, V_O ≤ 1.5 Vdc	I_{Sink}	6.0	16	—	6.0	16	—	6.0	16	—	6.0	16	—	6.0	16	—	6.0	16	—	mA
Saturation Voltage $V_I(-)$ ≥ +1.0 Vdc, $V_I(+)$ = 0, I_{sink} ≤ 4.0 mA	V_{sat}	—	130	400	—	130	400	—	130	400	—	130	400	—	130	400	—	130	500	mV
Output Leakage Current $V_I(+)$ ≥ +1.0 Vdc, $V_I(-)$ = 0, V_O = +5.0 Vdc	I_{OL}	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	—	nA

PERFORMANCE CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = T_{low} to T_{high} [Note 3])

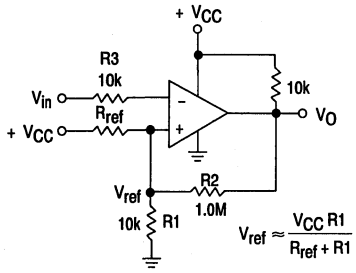
Characteristic	Symbol	LM139A			LM239A/339A			LM139			LM239/339			LM2901			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	—	—	±4.0	—	—	±4.0	—	—	±9.0	—	—	±9.0	—	—	±15	—	—	±40	mVdc
Input Bias Current (Notes 4, 5) (Output in Linear Range)	I_{IB}	—	—	300	—	—	400	—	—	300	—	—	400	—	—	500	—	—	1000	nA
Input Offset Current (Note 4)	I_{IO}	—	—	±100	—	—	±150	—	—	±100	—	—	±150	—	—	±200	—	—	±300	nA
Input Common Mode Voltage Range	V_{ICMR}	0	—	V_{CC} −2.0	0	—	V_{CC} −2.0	0	—	V_{CC} −2.0	0	—	V_{CC} −2.0	0	—	V_{CC} −2.0	0	—	V_{CC} −2.0	V
Saturation Voltage $V_I(-)$ ≥ +1.0 Vdc, $V_I(+)$ = 0, I_{sink} ≤ 4.0 mA	V_{sat}	—	—	700	—	—	700	—	—	700	—	—	700	—	—	700	—	—	700	mV
Output Leakage Current $V_I(+)$ ≥ +1.0 Vdc, $V_I(-)$ = 0, V_O = 30 Vdc	I_{OL}	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	µA
Differential Input Voltage All V_I ≥ 0 Vdc	V_{ID}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	Vdc

NOTES:

1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}. Output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. This magnitude of input current will only occur if the leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collectorbase junction becoming forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action which can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time that an input is driven negative. This will not destroy the device when limited to the max rating and normal output states will recover when the inputs become ≥ ground or negative supply.
3. (LM139/139A) T_{low} = −55°C, T_{high} = +125°C
   (LM239/239A) T_{low} = −25°C, T_{high} = +85°C
   (LM339/339A) T_{low} = 0°C, T_{high} = +70°C
   (MC3302) T_{low} = −40°C, T_{high} = +85°C
   (LM2901) T_{low} = −40°C, T_{high} = +105°C
4. At the output switch point, V_O ≈ 1.4 Vdc, R_S ≤ 100 Ω 5.0 Vdc ≤ V_{CC} ≤ 30 Vdc, with the inputs over the full common mode range (0 Vdc to V_{CC} −1.5 Vdc).
5. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
6. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.

2

Figure 2. Inverting Comparator with Hystersis



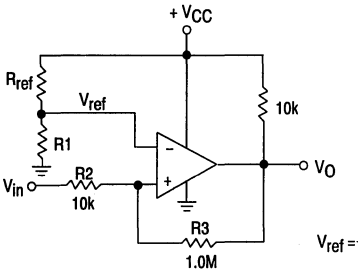
$$V_{ref} \approx \frac{V_{CC}\,R1}{R_{ref} + R1}$$

$$R3 \simeq R1 \,//\, R_{ref} \,//\, R2$$

$$V_H = \frac{R1 \,//\, R_{ref}}{R1 \,//\, R_{ref} + R2}\,[V_{O(max)} - V_{O(min)}]$$

$$R2 \gg R_{ref} \,//\, R1$$

Figure 3. Noninverting Comparator with Hysteresis



$$V_{ref} = \frac{V_{CC}\,R1}{R_{ref} + R1}$$

$$R2 \approx R1 \,//\, R_{ref}$$

Amount of Hysteresis V_H

$$V_H = \frac{R2}{R2 + R3}\,[(V_{O(max)} - V_{O(min)}]$$

Typical Characteristics

(V_{CC} = 1.5 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

Figure 4. Normalized Input Offset Voltage

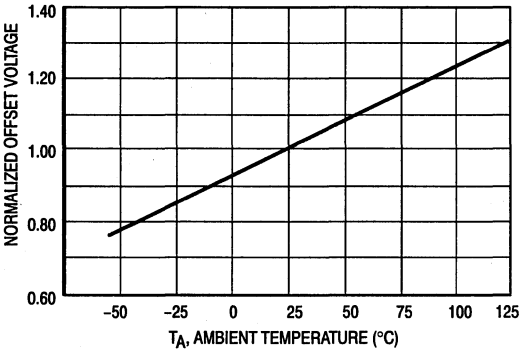


Figure 5. Input Bias Current

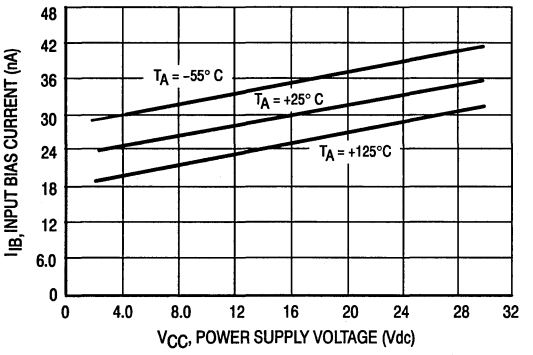


Figure 6. Output Sink Current versus Output Saturation Voltage

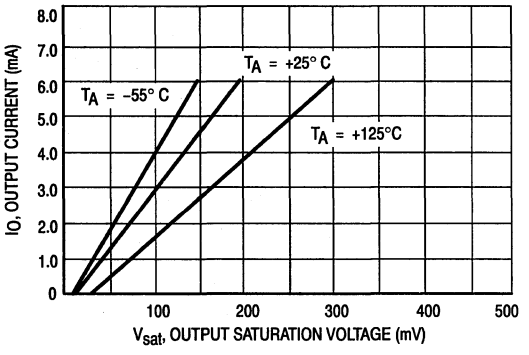
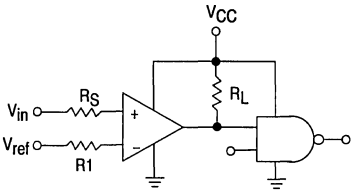


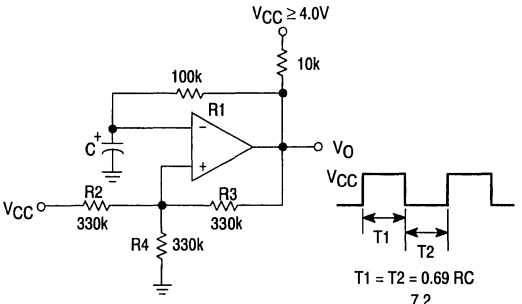
Figure 7. Driving Logic



RS = Source Resistance
R1 ≃ RS

Logic	Device	VCC (V)	RL kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5.0	10

Figure 8. Squarewave Oscillator



T1 = T2 = 0.69 RC

$f \approx \frac{7.2}{C(\mu F)}$

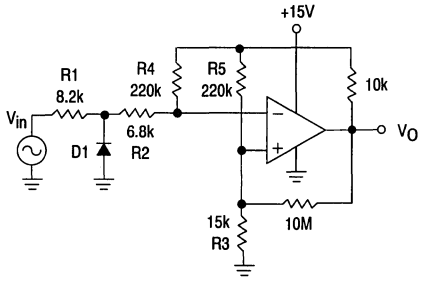
R2 = R3 = R4
R1 ≃ R2 // R3 // R4

APPLICATIONS INFORMATION

These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors < 10 kΩ should be used. The addition of positive feedback (< 10 mV) is also recommended. It is good design practice to ground all unused input pins.

Differential input voltages may be larger than supply voltages without damaging the comparator's inputs. Voltages more negative than –300 mV should not be used.

Figure 9. Zero Crossing Detector (Single Supply)



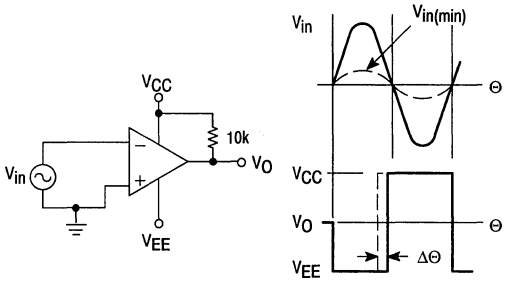
D1 prevents input from going negative by more than 0.6 V.

R1 + R2 = R3

$R3 \leq \frac{R5}{10}$ for small error in zero crossing

Figure 10. Zero Crossing Detector (Split Supplies)

$V_{in(min)} \approx 0.4$ V peak for 1% phase distortion (ΔΘ).



Dual Low Power Operational Amplifiers

LM158, LM258, LM358, LM2904

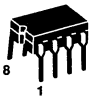
DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, 3) Single Supply or Split Supply operation and 4) pin outs compatible with the popular MC1558 dual operational amplifier. The LM158 Series is equivalent to one-half of an LM124.

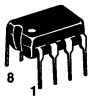
These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 V or as high as 32 V with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). the common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The Output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Single and Split Supply Operation
- Similar Performance to the Popular MC1558
- ESD Clamps on the Inputs Increase Ruggedness of the Device without Affecting Operation



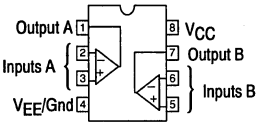
J SUFFIX
CERAMIC PACKAGE
CASE 693

N SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	LM158 LM258 LM358	LM2904	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 32 ±16	 26 ±13	Vdc
Input Differential Voltage Range (1)	V_{IDR}	±32	±26	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	–0.3 to 32	–0.3 to 26	Vdc
Output Short Circuit Duration	t_{SC}	Continuous		
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150		°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 –65 to +150 –55 to +125		°C
Operating Ambient Temperature Range LM158 LM258 LM358 LM2904	T_A	 –55 to +125 –25 to +85 0 to +70 —	 — — — –40 to +105	°C

NOTES: 1. Split Power Supplies.
2. For Supply Voltages less than 32 V for the LM158/258/358 and 26 V for the LM2904, the absolute maximum input voltage is equalt to the supply voltage
3. This input current will only exist when the voltage is negative at any of the input leads. Normal output states will reestablish when the input voltage returns to a voltage greater than –0.3 V.

ORDERING INFORMATION

Device	Temperature Range	Package
LM158J	–55° to +125°C	Ceramic DIP
LM2904D	–40° to +105°C	SO-8
LM2904N		Plastic DIP
LM2904J	–40° to +85°C	Ceramic DIP
LM258D	–25° to +85°C	SO-8
LM258J		Ceramic DIP
LM258N		Plastic DIP
LM358D	0° to +70°C	SO-8
LM358J		Ceramic DIP
LM358N		Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

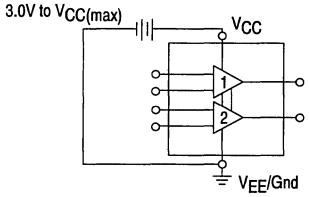
Characteristics	Symbol	LM158/LM258			LM358			LM2904			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage V_{CC} = 5.0 V to 30 V (26 V for LM2904), V_{IC} = 0 V to V_{CC} –1.7 V, $V_O \approx$ 14 V, R_S = 0 Ω T_A = 25°C $T_A = T_{high}$ to T_{low} (Note 1)	V_{IO}	 — —	 2.0 —	 5.0 7.0	 — —	 2.0 —	 7.0 9.0	 — —	 2.0 —	 7.0 10	mV
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{high}$ to T_{low} (Note 1)	$\Delta V_{IO}/\Delta T$	—	7.0	—	—	7.0	—	—	7.0	—	μV/°C
Input Offset Current $T_A = T_{high}$ to T_{low} (Note 1)	I_{IO}	— —	3.0 —	30 100	— —	5.0 —	50 150	— —	5.0 45	50 200	nA
Input Bias Current $T_A = T_{high}$ to T_{low} (Note 1)	I_{IB}	— —	–45 –50	–150 –300	— —	–45 –50	–250 –500	— —	–45 –50	–250 –500	
Average Temperature Coefficient of Input Offset Current $T_A = T_{high}$ to T_{low} (Note 1)	$\Delta I_{IO}/\Delta T$	—	10	—	—	10	—	—	10	—	pA/°C
Input Common Mode Voltage Range (Note 2) V_{CC} = 30 V (26 V for LM2904) V_{CC} = 30 V (26 V for LM2904), $T_A = T_{high}$ to T_{low}	V_{ICR}	 0 0	 — —	 28.3 28	 0 0	 — —	 28.3 28	 0 0	 — —	 24.3 24	V
Differential Input Voltage Range	V_{IDR}	—	—	V_{CC}	—	—	V_{CC}	—	—	V_{CC}	V
Large Signal Open-Loop Voltage Gain R_L = 2.0 kΩ, V_{CC} = 15 V, For Large V_O Swing, $T_A = T_{high}$ to T_{low} (Note 1)	A_{VOL}	 50 25	 100 —	 — —	 25 15	 100 —	 — —	 25 15	 100 —	 — —	V/mV
Channel Separation 1.0 kHz ≤ f ≤ 20 kHz, Input Referenced	CS	—	–120	—	—	–120	—	—	–120	—	dB
Common Mode Rejection R_S ≤ 10 kΩ	CMR	70	85	—	65	70	—	50	70	—	dB
Power Supply Rejection	PSR	65	100	—	65	100	—	50	100	—	dB
Output Voltage—High Limit ($T_A = T_{high}$ to T_{low}) (Note 1) V_{CC} = 50 V, R_L = 2.0 kΩ, T_A = 25°C V_{CC} = 30 V (26 V for LM2904), R_L = 2 kΩ V_{CC} = 30 V (26 V for LM2904), R_L = 10 kΩ	V_{OH}	 3.3 26 27	 3.5 — 28	 — — —	 3.3 26 27	 3.5 — 28	 — — —	 3.3 22 23	 3.5 — 24	 — — —	V
Output Voltage—Low Limit V_{CC} = 5.0 V, R_L = 10 kΩ, $T_A = T_{high}$ to T_{low} (Note 1)	V_{OL}	—	5.0	20	—	5.0	20	—	5.0	20	mV
Output Source Current V_{ID} = +1.0 V, V_{CC} = 15 V	I_{O+}	20	40	—	20	40	—	20	40	—	mA
Output Sink Current V_{ID} = –1.0 V, V_{CC} = 15 V V_{ID} = –1.0 V, V_O = 200 mV	I_{O-}	 10 12	 20 50	 — —	 10 12	 20 50	 — —	 10 —	 20 —	 — —	mA μA
Output Short Circuit to Ground (Note 3)	I_{SC}	—	40	60	—	40	60	—	40	60	mA
Power Supply Current ($T_A = T_{high}$ to T_{low}) (Note 1) V_{CC} = 30 V (26 V for LM2904), V_O = 0 V, R_L = ∞ V_{CC} = 5 V, V_O = 0 V, R_L = ∞	I_{CC}	 — —	 1.5 0.7	 3.0 1.2	 — —	 1.5 0.7	 3.0 1.2	 — —	 1.5 0.7	 3.0 1.2	mA

NOTES: 1. T_{low} = –55°C for LM158 T_{high} = +125°C for LM158
= –40°C for LM2904 = +105°C for LM2904
= –25°C for LM258 = +85°C for LM258
= 0°C for LM358 = +70°C for LM358

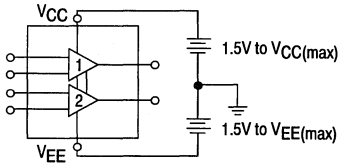
2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} –1.7 V.

3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Single Supply

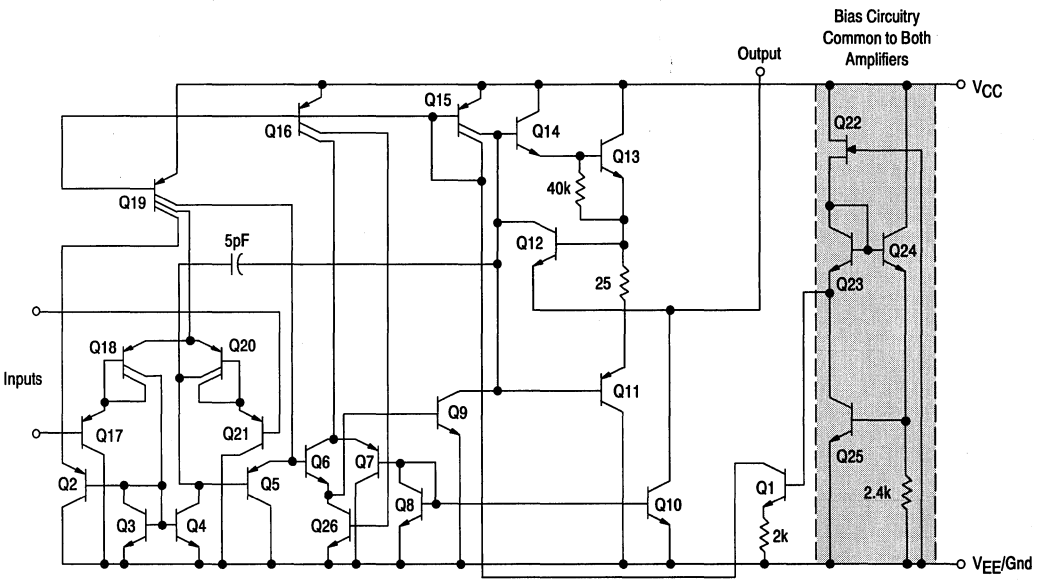


Split Supplies



2

Representative Circuit Schematic
(One-Half of Circuit Shown)



CIRCUIT DESCRIPTION

The LM158 series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

Large Signal Voltage Follower Response

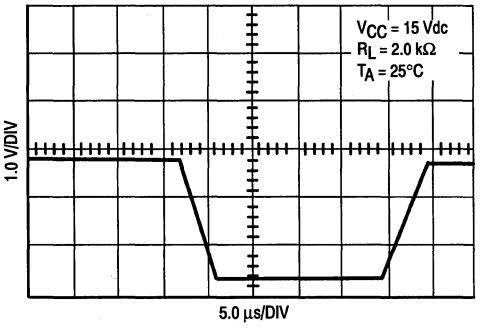


Figure 1. Input Voltage Range

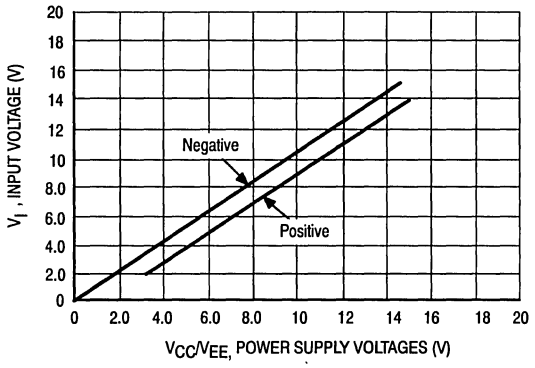


Figure 2. Large-Signal Open-Loop Voltage Gain

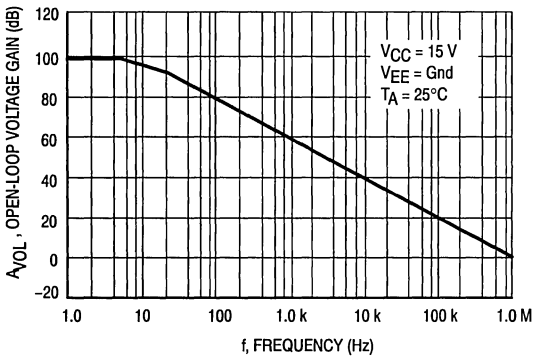


Figure 3. Large-Signal Frequency Response

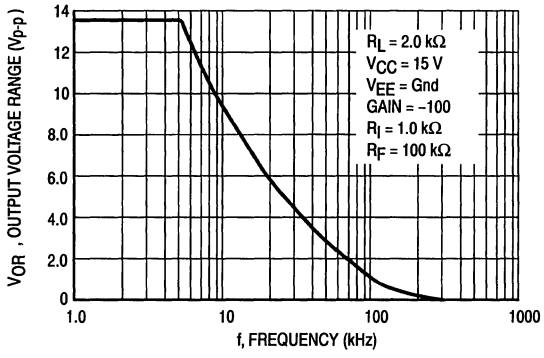


Figure 4. Small Signal Voltage Follower Pulse Response (Noninverting)

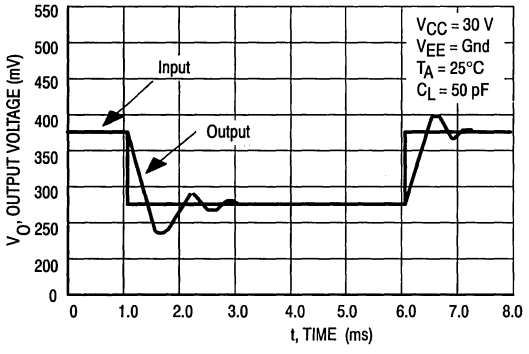


Figure 5. Power Supply Current versus Power Supply Voltage

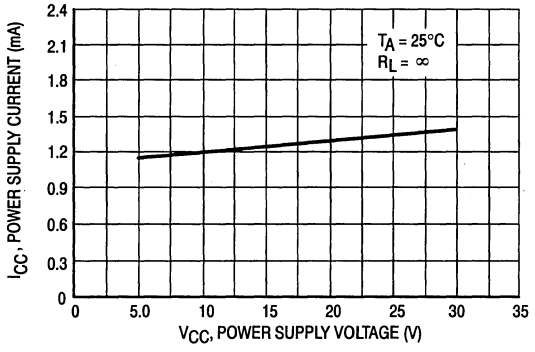


Figure 6. Input Bias Current versus Supply Voltage

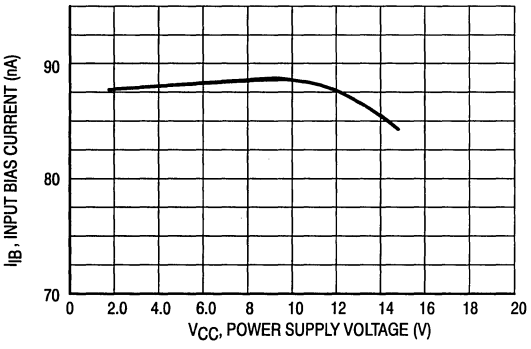


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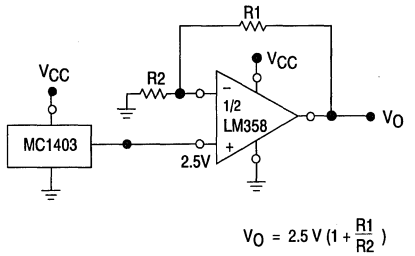
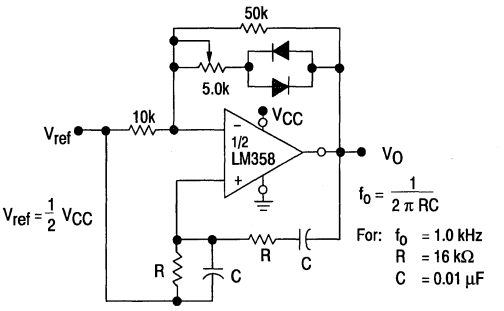
Figure 7. Voltage Reference



$$V_O = 2.5\,V\left(1 + \frac{R1}{R2}\right)$$

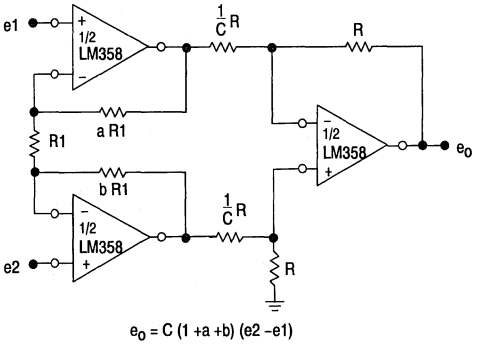
Figure 8. Wien Bridge Oscillator



$$f_o = \frac{1}{2\pi RC}$$

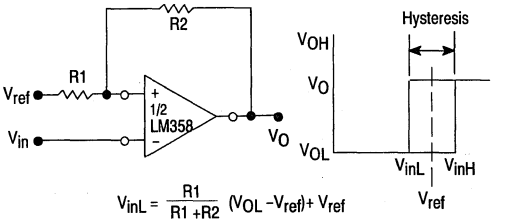
For: f_o = 1.0 kHz
R = 16 kΩ
C = 0.01 µF

Figure 9. High Impedance Differential Amplifier



$$e_o = C\,(1 + a + b)\,(e2 - e1)$$

Figure 10. Comparator with Hysteresis

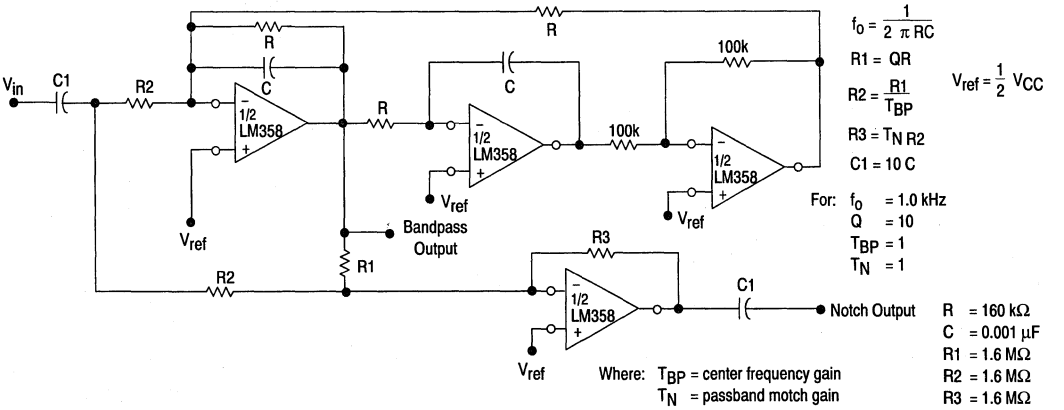


$$V_{inL} = \frac{R1}{R1 + R2}\,(V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2}\,(V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2}\,(V_{OH} - V_{OL})$$

Figure 11. Bi-Quad Filter



$$f_o = \frac{1}{2\pi RC}$$

R1 = QR

$$R2 = \frac{R1}{T_{BP}}$$

R3 = T_N R2

C1 = 10 C

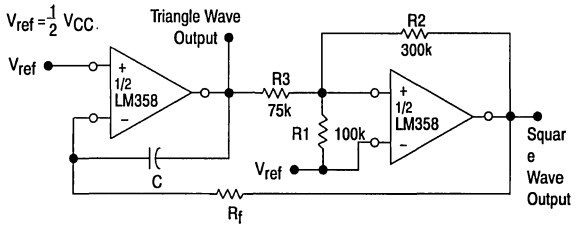
$$V_{ref} = \frac{1}{2}\,V_{CC}$$

For: f_o = 1.0 kHz
Q = 10
T_{BP} = 1
T_N = 1

R = 160 kΩ
C = 0.001 µF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

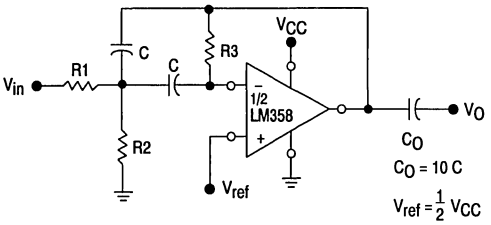
Where: T_{BP} = center frequency gain
T_N = passband motch gain

Figure 12. Function Generator



$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \quad \text{if, } R3 = \frac{R2\,R1}{R2 + R1}$$

Figure 13. Multiple Feedback Bandpass Filter



Given: f_0 = center frequency
$A(f_0)$ = gain at center frequency

Choose value f_0, C
Then:

$$R3 = \frac{Q}{\pi\, f_0\, C}$$

$$R1 = \frac{R3}{2\,A(f_0)}$$

$$R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

For less than 10% error from operational amplifier.

$$\frac{Q_0\, f_0}{BW} < 0.1$$ Where f_0 and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

LM348
LM248

DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

(Quad MC1741)
Operational Amplifiers

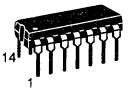
The LM348 series is a true quad MC1741. Integrated on a single monolithic chip are four independent, low power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single MC1741. Other features include input offset currents and input bias currents which are much less than the MC1741 industry standard.

The LM348 can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

- Each Amplifier is Functionally Equivalent to the MC1741
- Low Input Offset and Input Bias Currents
- Class AB Output Stage Eliminates Crossover Distortion
- Pin Compatible with MC3403 and LM324
- True Differential Inputs
- Internally Frequency Compensated
- Short Circuit Protection
- Low Power Supply Current (0.6 mA/Amplifier)

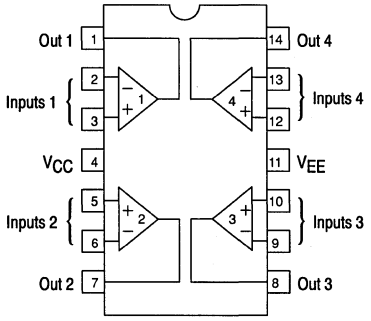
J SUFFIX
CERAMIC PACKAGE
CASE 632

N SUFFIX
PLASTIC PACKAGE
CASE 646



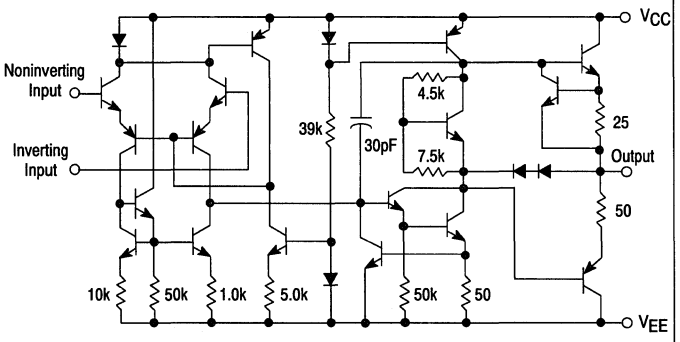
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Top View)

Equivalent Circuit Schematic
(1/4 of Circuit Shown)



ORDERING INFORMATION

Device	Temperature Range	Package
LM248J LM248N	–25° to +85°C	Ceramic DIP Plastic DIP
LM348D LM348J LM348N	0° to +70°C	SO-14 Ceramic DIP Plastic DIP

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value		Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 −18		Vdc
Input Differential Voltage	V_{ID}	±36		V
Input Common Mode Voltage	V_{ICM}	±18		V
Output Short Circuit Duration	t_{SC}	Continuous		
Operating Ambient Temperature Range	T_A	−25 to +85	0 to +70	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	−65 to +150 −55 to +125		°C
Junction Temperature Ceramic Package Plastic Package	T_J	175 150		°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le 10$ k)	V_{IO}	—	1.0	6.0	mV
Input Offset Current Input Bias Current	I_{IO} I_{IB}	— —	4.0 30	50 200	nA
Input Resistance	r_i	0.8	2.5	—	MΩ
Common Mode Input Voltage Range	V_{ICR}	±12	—	—	V
Large Signal Voltage Gain ($R_L \ge 2.0$ k, V_O = ±10 V)	A_{VOL}	25	160	—	V/mV
Channel Separation (f = 1.0 Hz to 20 kHz)	—	—	−120	—	dB
Common Mode Rejection ($R_S \le 10$ k)	CMR	70	90	—	dB
Supply Voltage Rejection ($R_S \le 10$ k)	PSR	77	96	—	
Output Voltage Swing ($R_L \ge 10$ k) ($R_L \ge 2$ k)	V_O	 ±12 ±10	 ±13 ±12	 — —	V
Output Short Circuit Current	I_{SC}	—	25	—	mA
Supply Current (All Amplifiers)	I_D	—	2.4	4.5	mA
Small Signal Bandwidth (A_V = 1)	BW	—	1.0	—	MHz
Phase Margin (A_V = 1)	ϕm	—	60	—	Degrees
Slew Rate (A_V = 1)	SR	—	0.5	—	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = *T_{high} to T_{low}, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le 10$ kΩ)	V_{IO}	—	—	7.5	mV
Input Offset Current LM248 LM348	I_{IO}	 — —	 — —	 125 100	nA
Input Bias Current LM248 LM348	I_{IB}	 — —	 — —	 500 400	
Common Mode Input Voltage Range	V_{ICR}	±12	—	—	V
Large Signal Voltage Gain ($R_L \ge 2$ k, V_O = ±10 V)	A_{VOL}	15	—	—	V/mV
Common Mode Rejection ($R_S \le 10$ k)	CMR	70	90	—	dB
Supply Voltage Rejection ($R_S \le 10$ k)	PSR	77	96	—	
Output Voltage Swing ($R_L \ge 10$ k) ($R_L \ge 2$ k)	V_O	 ±12 ±10	 ±13 ±12	 — —	V

* T_{high} = 85°C for LM248, and 70°C for LM348. T_{low} = −25°C for LM248, and 0°C for LM348.

NOTE: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted or the maximum junction temperature will be exceeded.

2

Figure 1. Power Bandwidth (Large Signal Swing versus Frequency)

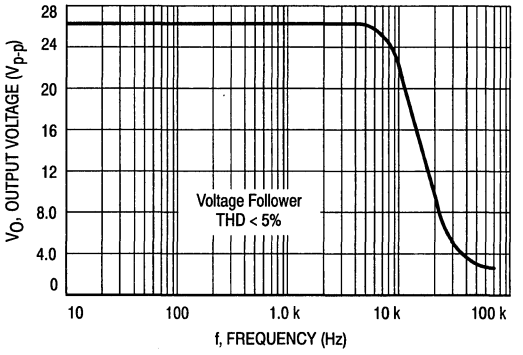


Figure 2. Open-Loop Frequency Response

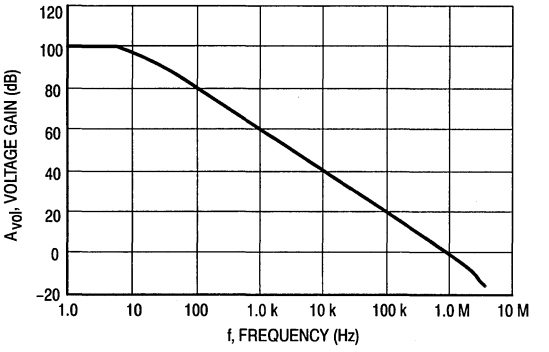


Figure 3. Positive Output Voltage Swing versus Load Resistance

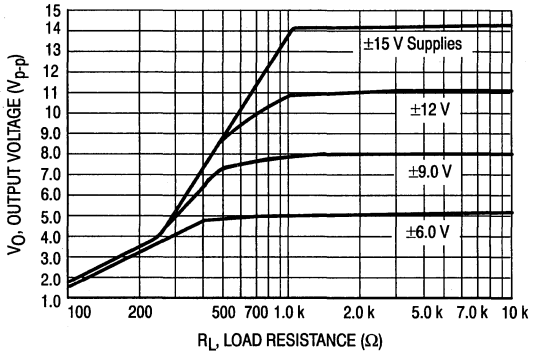


Figure 4. Negative Output Voltage Swing versus Load Resistance

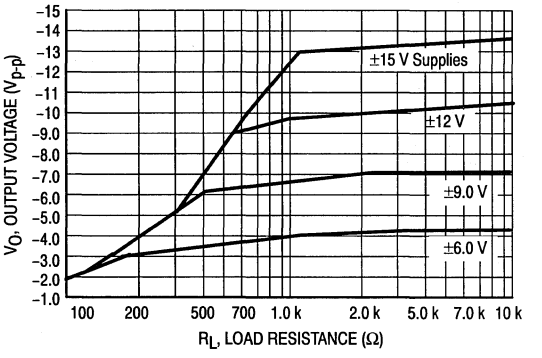


Figure 5. Output Voltage Swing versus Load Resistance (Single Supply Operation)

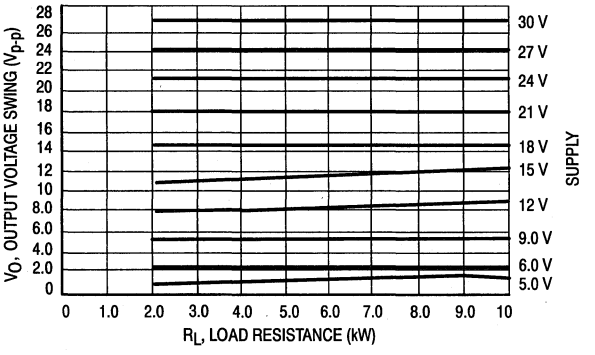


Figure 6. Noninverting Pulse Response

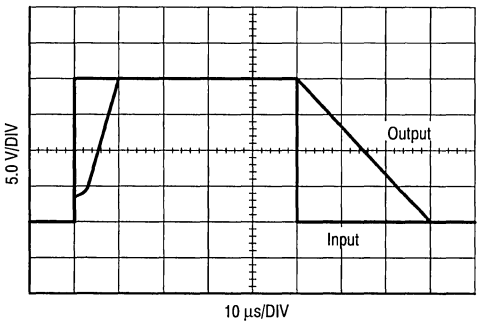
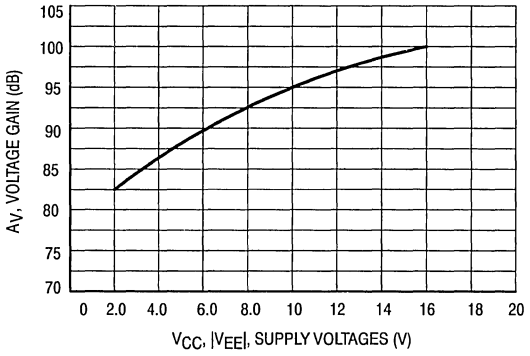
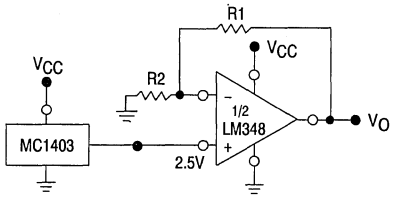


Figure 7. Open-Loop Voltage Gain versus Supply Voltage



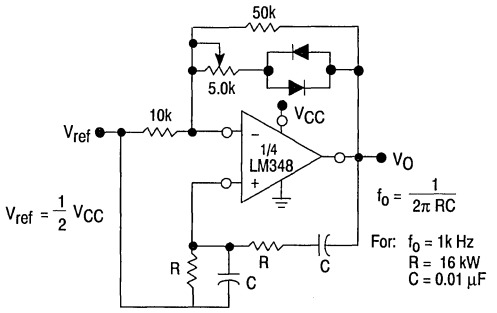
APPLICATIONS INFORMATION

Figure 8. Voltage Reference



$$V_O = 2.5\,V\left(1 + \frac{R1}{R2}\right)$$

Figure 9. Wien Bridge Oscillator

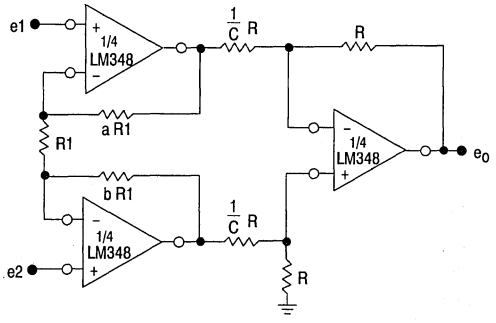


$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_o = \frac{1}{2\pi RC}$$

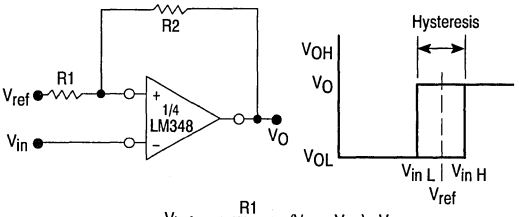
For: f_o = 1k Hz
R = 16 kW
C = 0.01 µF

Figure 10. High Impedance Differential Amplifier



$$e_o = C\,(1 + a + b)\,(e2 - e1)$$

Figure 11. Comparator with Hysteresis



$$V_{in\,L} = \frac{R1}{R1 + R2}\,(V_{OL} - V_{ref}) + V_{ref}$$

$$V_{in\,H} = \frac{R1}{R1 + R2}\,(V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2}\,(V_{OH} - V_{OL})$$

2

Figure 12. High Impedance Instrumentation Buffer/Filter

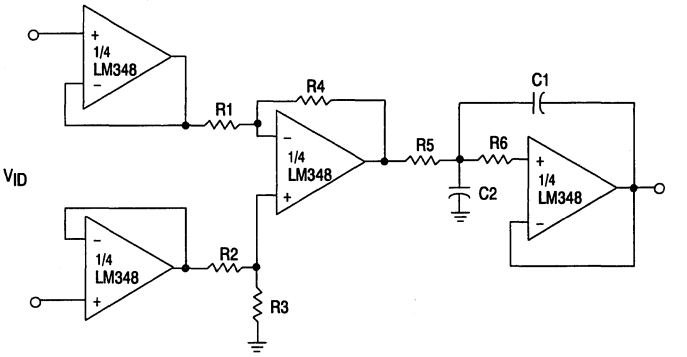


Figure 13. Function Generator

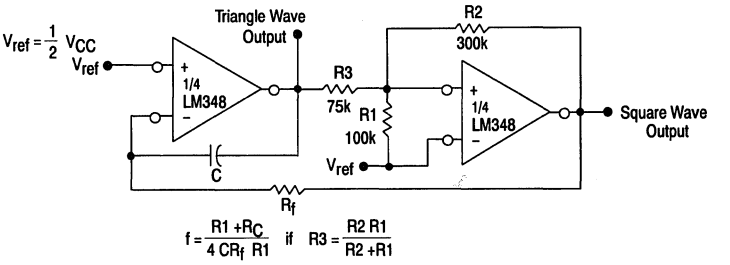


Figure 14. Bi-Quad Filter

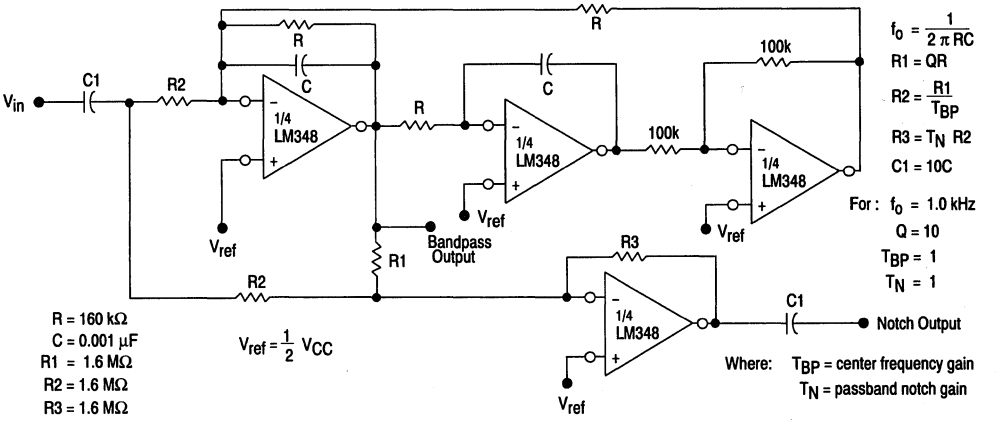
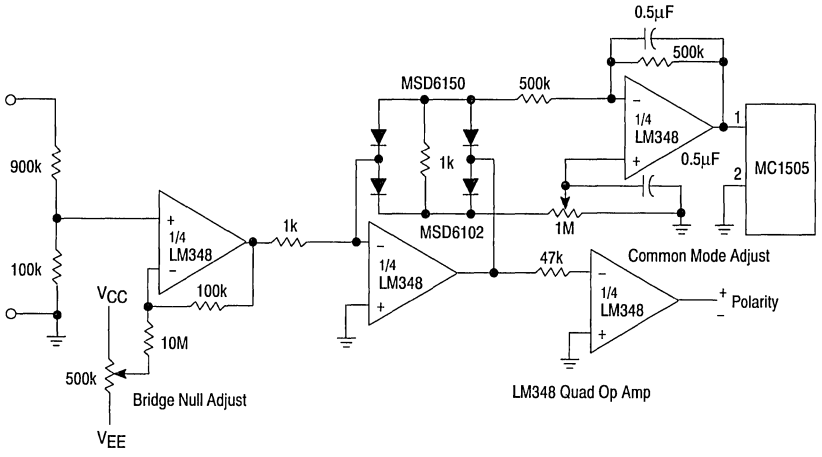


Figure 15. Absolute Value DVM Front End



LM393, A
LM293
LM2903

Low Offset Voltage Dual Comparators

SINGLE SUPPLY, LOW POWER DUAL COMPARATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

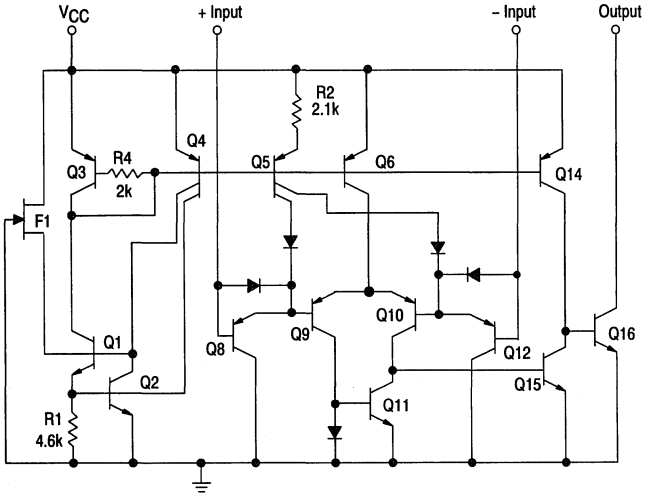
The LM393 series are dual independent precision voltage comparators capable of single or split supply operation. These devices are designed to permit a common mode range-to-ground level with single supply operation. Input offset voltage specifications as low as 2.0 mV make this device an excellent selection for many applications in consumer automotive, and industrial electronics.

- Wide Single-Supply Range: 2.0 Vdc to 36 Vdc
- Split-Supply Range: ±1.0 Vdc to ±18 Vdc
- Very Low Current Drain Independent of Supply Voltage: 0.4 mA
- Low Input Bias Current: 25 nA
- Low Input Offset Current: 5.0 nA
- Low Input Offset Voltage: 2.0 mV (max) LM393A
  5.0 mV (max) LM293/393
- Input Common Mode Range to Ground Level
- Differential Input Voltage Range Equal to Power Supply Voltage
- Output Voltage Compatible with DTL, ECL, TTL, MOS, and CMOS Logic Levels
- ESD Clamps on the Inputs Increase the Ruggedness of the Device without Affecting Performance

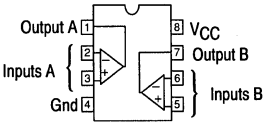
N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

Figure 1. Circuit Schematic
(Diagram shown is for 1 comparator)



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
LM293D	–25° to +85°C	SO-8
LM393D	0° to +70°C	SO-8
LM393AN,N		Plastic DIP
LM2903D	–40° to +105°C	SO-8
LM2903N		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	–0.3 to +36	Vdc
Input Current (2) (V_{in} < –0.3 Vdc)	I_{in}	50	mA
Output Short Circuit-to-Ground Output Sink Current (1)	I_{SC} I_{Sink}	Continuous 20	mA
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D $1/R_{\theta JA}$	570 5.7	mW mW/°C
Operating Ambient Temperature Range LM293 LM393, 393A LM2903	T_A	– –25 to +85 0 to +70 –40 to +105	°C
Maximum Operating Junction Temperature LM393, 393A, 2903 LM293	$T_{J(max)}$	 125 150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, $T_{low} \le T_A \le T_{high}$, unless otherwise noted.)*

Characteristics	Symbol	LM393A Min	LM393A Typ	LM393A Max	Unit
Input Offset Voltage (Note 3) T_A = 25°C $T_{low} \le T_A \le T_{high}$	V_{IO}	 — —	 ±1.0 —	 ±2.0 4.0	mV
Input Offset Current T_A = 25°C $T_{low} \le T_A \le T_{high}$	I_{IO}	 — —	 ±50 —	 ±50 ±150	nA
Input Bias Current (4) T_A = 25°C $T_{low} \le T_A \le T_{high}$	I_{IB}	 — —	 25 —	 250 400	nA
Input Common Mode Voltage Range (Note 5) T_A = 25°C $T_{low} \le T_A \le T_{high}$	V_{ICR}	 0 0	 — —	 V_{CC} –1.5 V_{CC} –2.0	V
Voltage Gain $R_L \ge 15$ kΩ, V_{CC} = 15 Vdc, T_A = 25°C	A_{VOL}	50	200	—	V/mV
Large Signal Response Time V_{in} = TTL Logic Swing, V_{ref} = 1.4 Vdc V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C	—	—	300	—	ns
Response Time (Note 6) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C	t_{TLH}	—	1.3	—	µs
Input Differential Voltage (7) All $V_{in} \ge$ Gnd or V– Supply (if used)	V_{ID}	—	—	V_{CC}	V
Output Sink Current $V_{in} \ge 1.0$ Vdc, V_{in+} = 0 Vdc, $V_O \le 1.5$ Vdc, T_A = 25°C	I_{Sink}	6.0	16	—	mA
Output Saturation Voltage $V_{in} \ge 1.0$ Vdc, V_{in+} = 0 Vdc, $I_{Sink} \le 4.0$ mA, T_A = 25°C $T_{low} \le T_A \le T_{high}$	V_{OL}	 — —	 150 —	 400 700	mV
Output Leakage Current $V_{in–}$ = 0 V, $V_{in+} \ge 1.0$ Vdc, V_O = 5.0 Vdc, T_A= 25°C $V_{in–}$ = 0 V, $V_{in+} \ge 1.0$ Vdc, V_O = 30 Vdc, $T_{low} \le T_A \le T_{high}$	I_{OL}	 — —	 0.1 —	 — 1.0	µA
Supply Current R_L = ∞ Both Comparators, T_A = 25°C R_L = ∞ Both Comparators, V_{CC} = 30 V	I_{CC}	 — —	 0.4 1.0	 1.0 2.5	mA

*LM293 T_{low} = –25°C, T_{high} = +85°C
LM393/393A T_{low} = 0°C, T_{high} = +70°C
LM2903 T_{low} = –40°C, T_{high} = +105°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, $T_{low} \le T_A \le T_{high}$, unless otherwise noted.)*

Characteristics	Symbol	LM293, LM393			LM2903			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 3)	V_{IO}							mV
T_A = 25°C		—	±1.0	±5.0	—	±2.0	±7.0	
$T_{low} \le T_A \le T_{high}$		—	—	9.0	—	9.0	15	
Input Offset Current	I_{IO}							nA
T_A = 25°C		—	±5.0	±50	—	±5.0	±50	
$T_{low} \le T_A \le T_{high}$		—	—	±150	—	±50	±200	
Input Bias Current (Note 4)	I_{IB}							nA
T_A = 25°C		—	25	250	—	25	250	
$T_{low} \le T_A \le T_{high}$		—	—	400	—	200	500	
Input Common Mode Voltage Range (Note 4)	V_{ICR}							V
T_A = 25°C		0	—	V_{CC} –1.5	0	—	V_{CC} –1.5	
$T_{low} \le T_A \le T_{high}$		0	—	V_{CC} –2.0	0	—	V_{CC} –2.0	
Voltage Gain	A_{VOL}	50	200	—	25	200	—	V/mV
$R_L \ge 15$ kΩ, V_{CC} = 15 Vdc, T_A = 25°C								
Large Signal Response Time	—	—	300	—	—	300	—	ns
V_{in} = TTL Logic Swing, V_{ref} = 1.4 Vdc								
V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C								
Response Time (Note 6)	t_{TLH}	—	1.3	—	—	1.5	—	µs
V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C								
Input Differential Voltage (Note 7)	V_{ID}	—	—	V_{CC}	—	—	V_{CC}	V
All $V_{in} \ge$ Gnd or V– Supply (if used)								
Output Sink Current	I_{Sink}	6.0	16	—	6.0	16	—	mA
$V_{in} \ge 1.0$ Vdc, V_{in+} = 0 Vdc, $V_O \le 1.5$ Vdc T_A = 25°C								
Output Saturation Voltage	V_{OL}							mV
$V_{in} \ge 1.0$ Vdc, V_{in+} = 0, $I_{Sink} \le 4.0$ mA, T_A = 25°C		—	150	400	—	—	400	
$T_{low} \le T_A \le T_{high}$		—	—	700	—	200	700	
Output Leakage Current	I_{OL}							nA
$V_{in–}$ = 0 V, $V_{in+} \ge 1.0$ Vdc, V_O = 5.0 Vdc, T_A = 25°C		—	0.1	—	—	0.1	—	
$V_{in–}$ = 0 V, $V_{in+} \ge 1.0$ Vdc, V_O = 30 Vdc,								
$T_{low} \le T_A \le T_{high}$		—	—	1000	—	—	1000	
Supply Current	I_{CC}							mA
R_L = ∞ Both Comparators, T_A = 25°C		—	0.4	1.0	—	0.4	1.0	
R_L = ∞ Both Comparators, V_{CC} = 30 V		—	—	2.5	—	—	2.5	

*LM293 T_{low} = –25°C, T_{high} = +85°C
LM393/393A T_{low} = 0°C, T_{high} = +70°C

NOTES: 1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}, output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. This magnitude of input current will only occur if the input leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector base junction becoming forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action on the IC chip. This phenomena can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time the input is driven negative. This will not destroy the device and normal output states will recover when the inputs become > –0.3 V of ground or negative supply.
3. At output switch point, $V_O \simeq 1.4$ Vdc, R_S = 0 Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the full input common mode range (0 V to V_{CC} = –1.5 V).
4. Due to the PNP transistor inputs, bias current will flow out of the inputs. This current is essentially constant, independent of the output state, therefore, no loading changes will exist on the input lines.
5. Input common mode of either input should not be permitted to go more than 0.3 V negative of ground or minus supply. The upper limit of common mode range is V_{CC} –1.5 V.
6. Response time is specified with a 100 mV step and 5.0 mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.
7. The comparator will exhibit proper output state if one of the inputs becomes greater than V_{CC}, the other input must remain within the common mode range. The low input state must not be less than –0.3 V of ground or minus supply.

LM293/393,A

Figure 2. Input Bias Current versus Power Supply Voltage

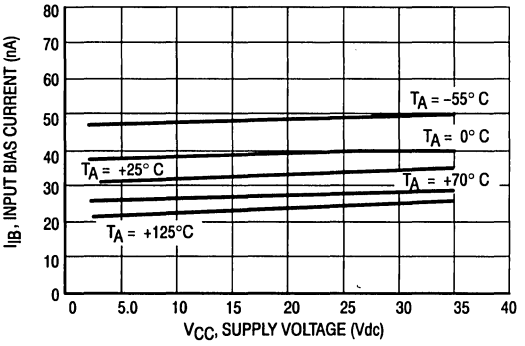


Figure 3. Output Saturation Voltage versus Output Sink Current

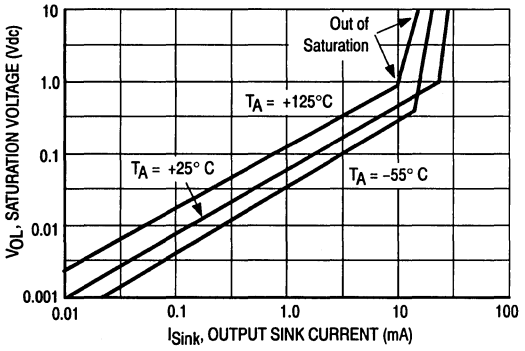
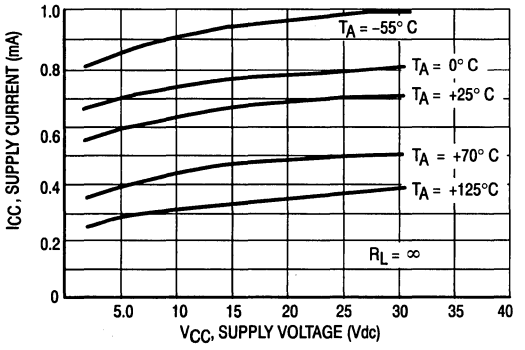


Figure 4. Power Supply Current versus Power Supply Voltage



LM2903

Figure 5. Input Bias Current versus Power Supply Voltage

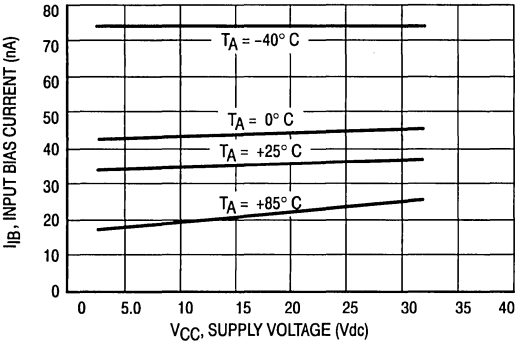


Figure 6. Output Saturation Voltage versus Output Sink Current

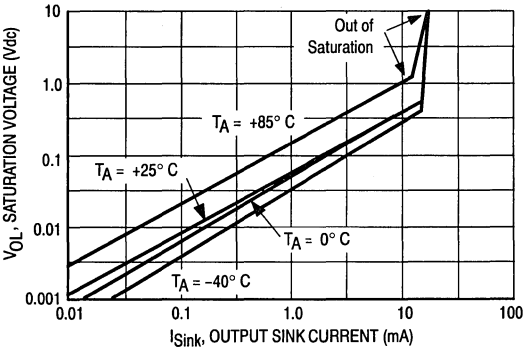
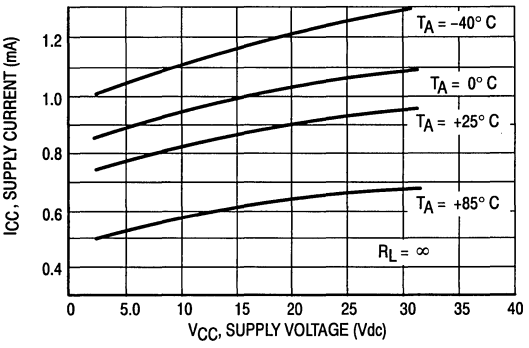


Figure 7. Power Supply Current versus Power Supply Voltage



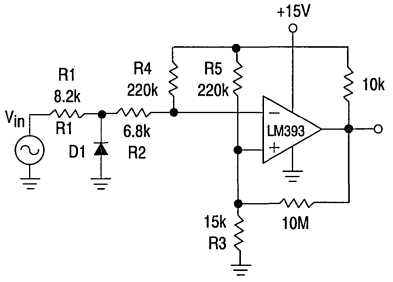
APPLICATIONS INFORMATION

These dual comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors <10 kΩ should be used.

The addition of positive feedback (<10 mV) is also recommended. It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than –0.3 V should not be used.

Figure 8. Zero Crossing Detector (Single Supply)

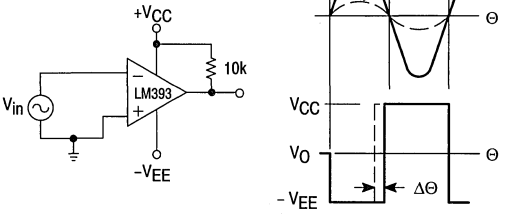


D1 prevents input from going negative by more than 0.6 V.

$$R1 + R2 = R3$$

$$R3 \leq \frac{R5}{10}$$ for small error in zero crossing.

Figure 9. Zero Crossing Detector (Split Supply)



$V_{in(min)} \approx 0.4$ V peak for 1% phase distortion ($\Delta\Theta$).

Figure 10. Free-Running Square-Wave Oscillator

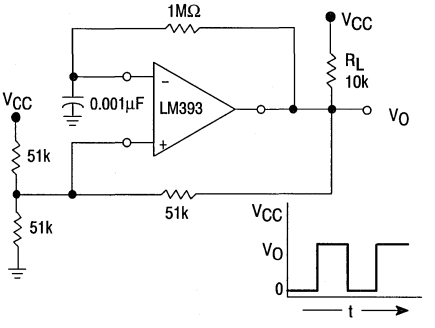
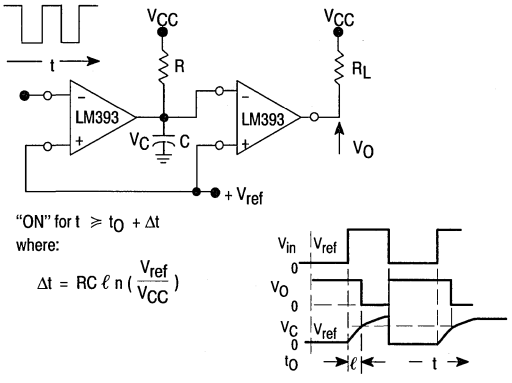


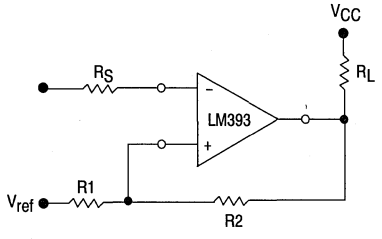
Figure 11. Time Delay Generator



"ON" for $t \geq t_O + \Delta t$
where:

$$\Delta t = RC\,\ell n\left(\frac{V_{ref}}{V_{CC}}\right)$$

Figure 12. Comparator with Hysteresis



$$R_S = R1 \,||\, R2$$

$$V_{th1} = V_{ref} + \frac{(V_{CC} - V_{ref})\ R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{ref} - \frac{(V_{ref} - V_{O\ Low})\ R1}{R1 + R2}$$

LM307

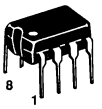
OPERATIONAL AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

Internally Compensated Monolithic Operational Amplifier

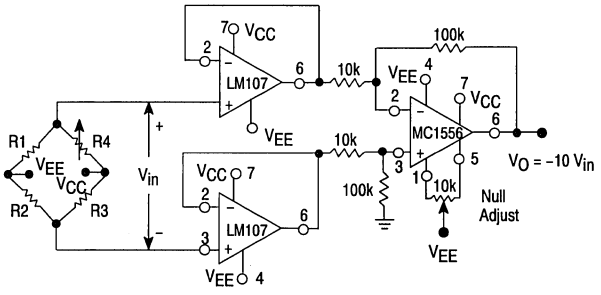
A general purpose operational amplifier well suited for applications requiring lower input currents than are available with the popular MC1741. These improved input characteristics permit greater accuracy in sample and hold circuits and long interval integrators.

- Internally Compensated
- Low Offset Voltage: 7.5 mV Max
- Low Input Offset Current: 50 nA Max
- Low Input Bias Current: 250 nA Max



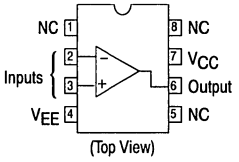
N SUFFIX
PLASTIC PACKAGE
CASE 626

Typical Application
High Impedance Bridge Amplifier



Pins not shown are not connected.

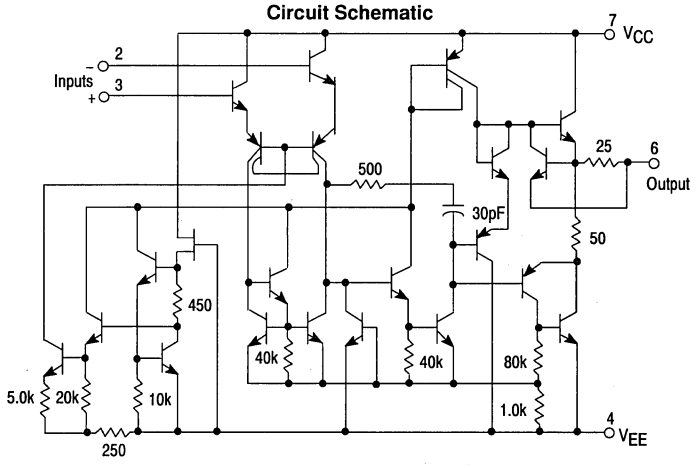
PIN CONNECTIONS



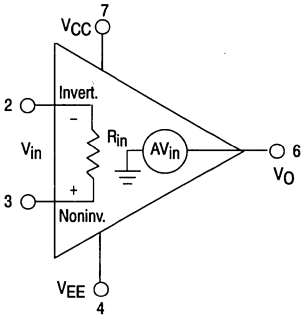
ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM307N	0° to+70°C	Plastic DIP

Circuit Schematic



Equivalent Circuit



Pins 1, 5, and 8 no connection.

2

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	LM307	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 −18	Vdc
Differential Input Signal Voltage	V_{ID}	±30	V
Common Mode Input Swing (Note 1)	V_{ICR}	±15	V
Output Short Circuit Duration	t_{SC}	Indefinite	
Power Dissipation (Package Limitation) (Note 2)	P_D	500	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, unless otherwise noted, see Note 3.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}				mV
$R_S \le 50$ kΩ, T_A = +25°C		—	2.0	7.5	
$R_S \le 50$ kΩ, $T_A = T_{low}$ to T_{high}		—	—	10	
Input Offset Current	I_{IO}				nA
T_A = +25°C		—	3.0	50	
$T_A = T_{low}$ to T_{high}		—	—	70	
Input Bias Current	I_{IB}				nA
T_A = +25°C		—	70	250	
$T_A = T_{low}$ to T_{high}		—	—	300	
Input Resistance	r_i	0.5	2.0	—	MΩ
Supply Current, V_S = ±15 V, T_A = +25°C	I_D	—	1.8	3.0	mA
Large Signal Voltage Gain	A_{VOL}				V/mV
V_S = ±15 V, V_O = ±10 V, R_L > 2.0 kΩ, T_A = +25°C		25	160	—	
V_S = ±15 V, V_O = ±10 V, R_L > 2.0 kΩ, $T_A = T_{low}$		15	—	—	
Average Temperature Coefficient of Input Offset Voltage, $T_{low} \le T_A \le T_{high}$	TCV_{IO}	—	6.0	30	µV/°C
Average Temperature Coefficient of Input Offset Current	TCI_{IO}				nA/°C
+25°C ≤ $T_A \le T_{high}$		—	0.01	0.3	
$T_{low} \le T_A$ ≤ +25°C		—	0.02	0.6	
Output Voltage Swing ($T_A = T_{low}$ to T_{high})	V_O				V
V_S = ±15 V, R_L = 10 kΩ		±12	±14	—	
R_L = 2.0 kΩ		±10	±13	—	
Input Voltage Range ($T_A = T_{low}$ to T_{high}) V_S = ±15 V	V_{ICR}	±12	—	—	V
Common Mode Rejection ($T_A = T_{low}$ to T_{high}) $R_S \le 50$ kΩ	CMR	70	90	—	dB
Supply Voltage Rejection ($T_A = T_{low}$ to T_{high}) $R_S \le 50$ kΩ	PSR	70	96	—	dB

NOTES: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. For operating at elevated temperatures, the device must be derated based on a maximum junction temperature of 100°C.
3. Unless otherwise noted, these specifications apply for: ±5.0 V ≤ V_{CC}/V_{EE} ≤ ±15 V, T_{low} = 0°C, T_{high} = +70°C.

Figure 1. Minimum Input Voltage Range

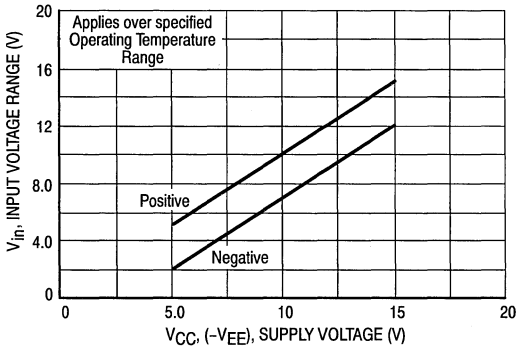


Figure 2. Minimum Output Voltage Swing

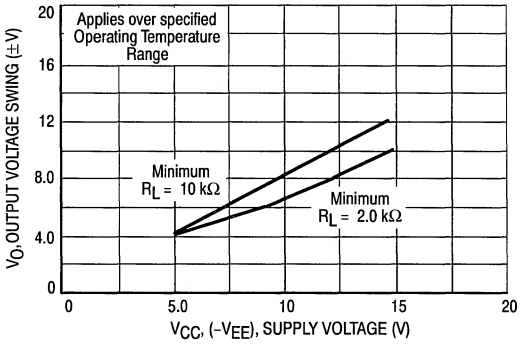


Figure 3. Minimum Voltage Gain

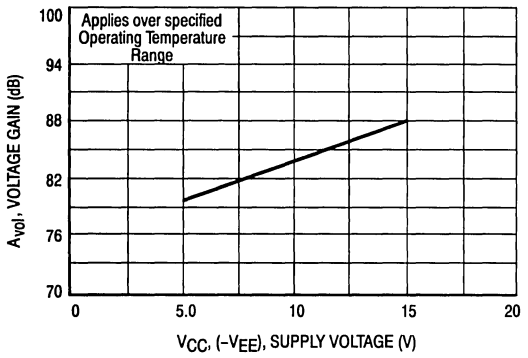


Figure 4. Typical Supply Currents

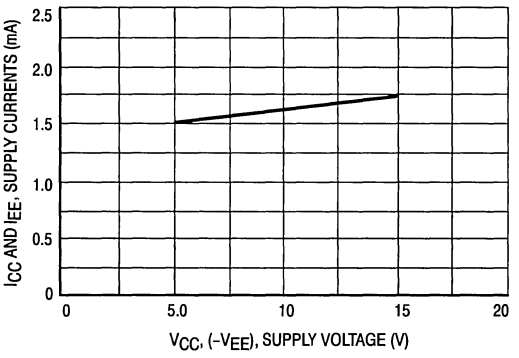


Figure 5. Open-Loop Frequency Response

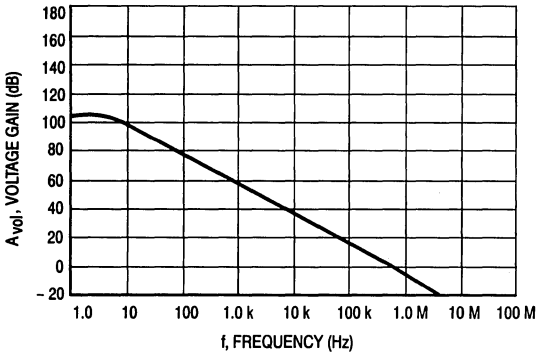


Figure 6. Large Signal Frequency Response

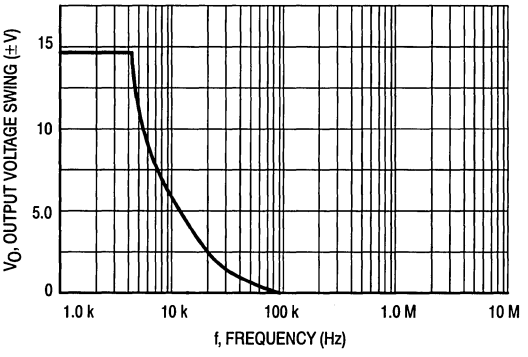
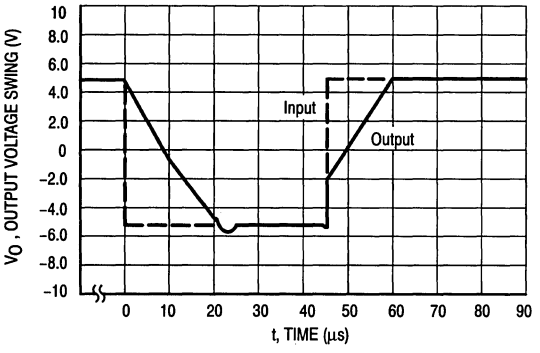


Figure 7. Voltage Follower Pulse Response



LM308A

SUPER GAIN OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

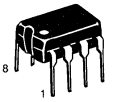
Precision Operational Amplifier

The LM308A operational amplifier provides high input impedance, low input offset and temperature drift, and low noise. These characteristics are made possible by use of a special Super Beta processing technology. This amplifier is particularly useful for applications where high accuracy and low drift performance are essential. In addition high speed performance may be improved by employing feedforward compensation techniques to maximize slew rate without compromising other performance criteria.

The LM308A offers extremely low input offset voltage and drift specifications allowing usage in even the most critical applications without external offset nulling.

- Operation from a Wide Range of Power Supply Voltages
- Low Input Bias and Offset Currents
- Low Input Offset Voltage and Guaranteed Offset Voltage Drift Performance
- High Input Impedance

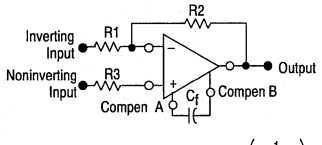
N SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

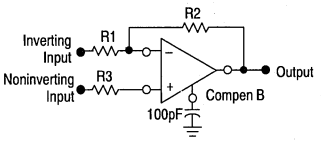
Frequency Compensation

Standard Compensation

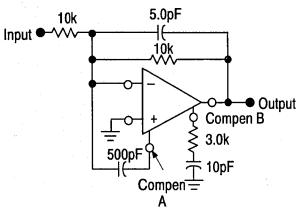


$$C_f \geq 30 \left(\frac{1}{1 + \frac{R2}{R1}}\right)$$

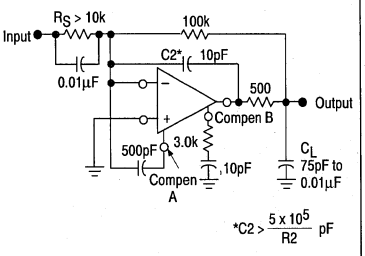
Modified Compensation



Standard Feedforward Compensation

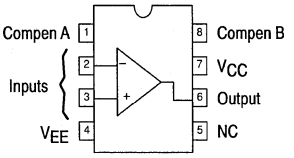


Feedforward Compensations for Decoupling Load Capacitance



$$*C2 > \frac{5 \times 10^5}{R2}\ pF$$

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
LM308AN LM308AD	0° to +70°C	Plastic DIP SO-8

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±18	Vdc
Input Voltage (See Note 1)	V_I	±15	V
Input Differential Current (See Note 2)	I_{ID}	±10	mA
Output Short Circuit Duration	t_{SC}	Indefinite	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+150	°C

Notes: 1. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1.0 V is applied between the inputs, unless some limiting resistance is used.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted these specifications apply for supply voltages of +5.0V ≤ V_{CC} ≤ +15 V and −5.0 V ≥ V_{EE} ≥ −15 V, T_A = +25°C.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	—	0.3	0.5	mV
Input Offset Current	I_{IO}	—	0.2	1.0	nA
Input Bias Current	I_{IB}	—	1.5	7.0	nA
Input Resistance	r_i	10	40	—	MΩ
Power Supply Currents (V_{CC} = +15 V, V_{EE} = −15 V)	I_{CC},I_{EE}	—	±0.3	±0.8	mA
Large Signal Voltage Gain (V_{CC} = +15 V, V_{EE} = −15 V, V_O = ±10 V, R_L ≥ 10 kΩ)	A_{VOL}	80	300	—	V/mV
The following specifications apply over the operating temperature range.					
Input Offset Voltage	V_{IO}	—	—	0.73	mV
Input Offset Current	I_{IO}	—	—	1.5	nA
Average Temperature Coefficient of Input Offset Voltage T_A (min) ≤ T_A ≤ T_A (max)	$\Delta V_{IO}/\Delta T$	—	1.0	5.0	µV/°C
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	—	2.0	10	pA/°C
Input Bias Current	I_{IB}	—	—	10	nA
Large Signal Voltage Gain (V_{CC} +15 V, V_{EE} = −15 V, V_O = ±10 V, R_L ≥ 10 kΩ)	A_{VOL}	60	—	—	V/mV
Input Voltage Range (V_{CC} = +15 V, V_{EE} = −15 V)	V_{ICR}	±14	—	—	V
Common Mode Rejection (R_S ≤ 50 kΩ)	CMR	96	110	—	dB
Supply Voltage Rejection (R_S ≤ 50 kΩ)	PSR	96	110	—	dB
Output Voltage Range (V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kΩ)	V_{OR}	±13	±14	—	V

2

Figure 1. Input Bias and Input Offset Currents

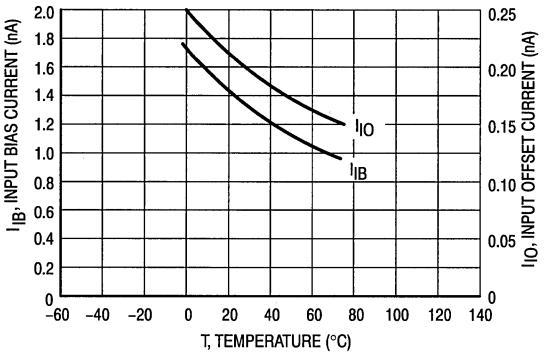


Figure 2. Maximum Equivalent Input Offset Voltage Error versus Input Resistance

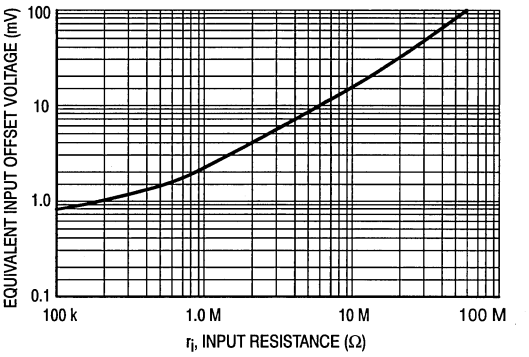


Figure 3. Voltage Gain versus Supply Voltages

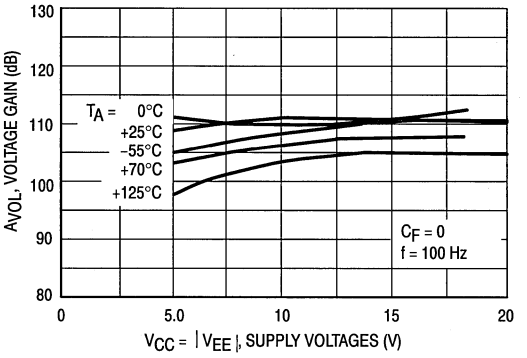


Figure 4. Power Supply Currents versus Power Supply Voltages

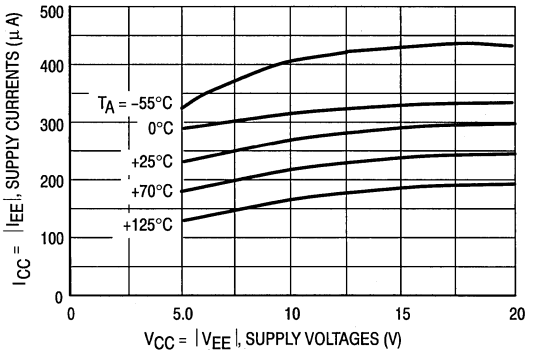


Figure 5. Open-Loop Frequency Response

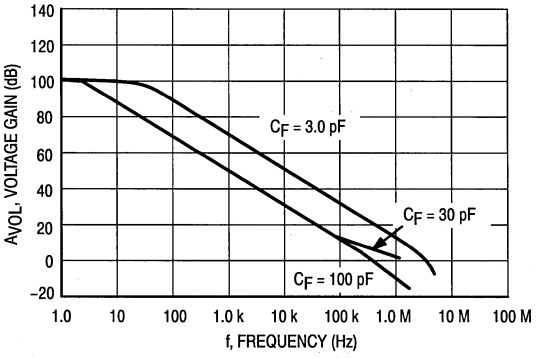
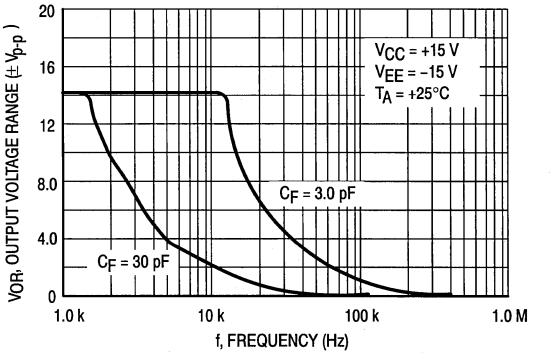


Figure 6. Large Signal Frequency Response



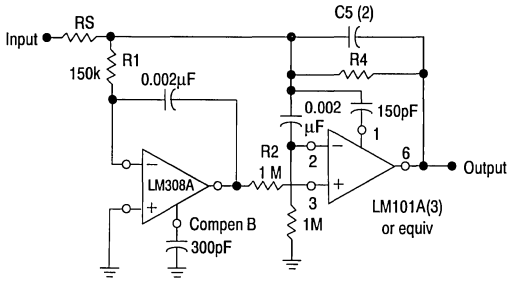
SUGGESTED DESIGN APPLICATIONS

INPUT GUARDING

Special care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the LM308A amplifier. Boards must be thoroughly cleaned with alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at +125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high voltage pins are then absorbed by the guard.

Figure 7. Fast (1) Summing Amplifier with Low Input Current

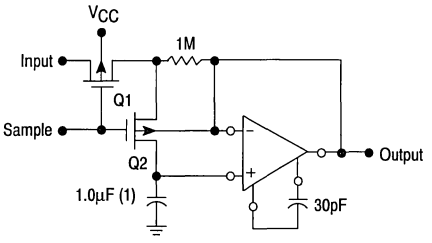


(1) Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10 V/µs

(2) $C5 = \frac{6 \times 10^{-8}}{R1}$

(3) In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

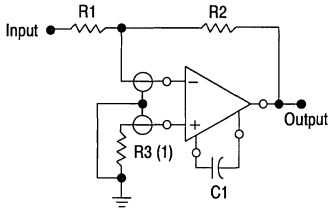
Figure 8. Sample and Hold



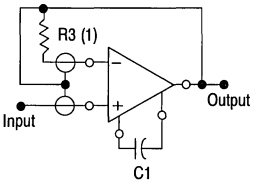
(1) Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

Figure 9. Connection of Input Guards

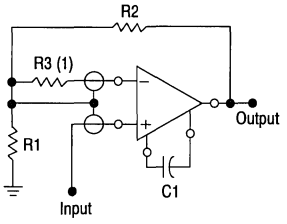
Inverting Amplifier



Follower



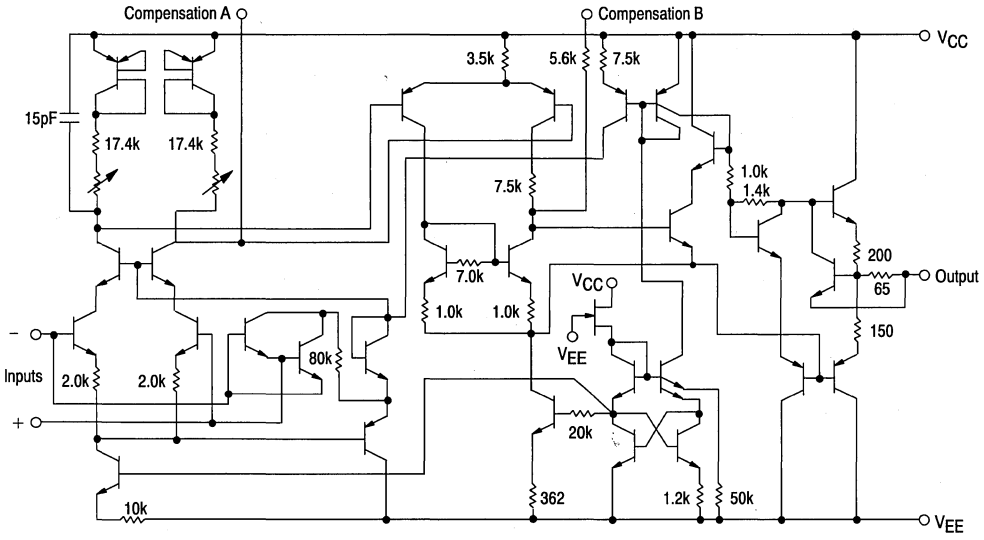
Noninverting Amplifier



(1) Used to compensate for large source resistances.

Note: $\frac{R1\ R2}{R1 + R2}$ must be an impedance.

Representative Circuit Schematic



LM833

Dual Low Noise, Audio Amplifier

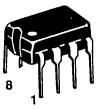
DUAL OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

The LM833 is a standard low-cost monolithic dual general-purpose operational amplifier employing Bipolar technology with innovative high- performance concepts for audio systems applications. With high frequency PNP transistors, the LM833 offers low voltage noise (4.5 nV/$\sqrt{Hz}$), 15 MHz gain bandwidth product, 7.0 V/μs slew rate, 0.3 mV input offset voltage with 2.0 μV/°C temperature coefficient of input offset voltage. The LM833 output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink AC frequency response.

The LM833 is specified over the automotive temperature range and is available in the plastic DIP and SO-8 packages (P and D suffixes). For an improved performance dual/quad version, see the MC33079 family.

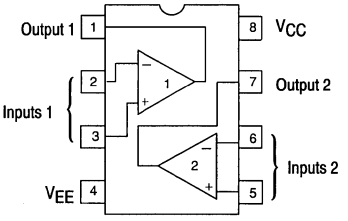
- Low Voltage Noise: 4.5 nV/$\sqrt{Hz}$
- High Gain Bandwidth Product: 15 MHz
- High Slew Rate: 7.0 V/μs
- Low Input Offset Voltage: 0.3 mV
- Low T.C. of Input Offset Voltage: 2.0 μV/°C
- Low Distortion: 0.002%
- Excellent Frequency Stability
- Dual Supply Operation



N SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	30(1)	V
Input Voltage Range	V_{IR}	±15(1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	–60 to +150	°C
Maximum Power Dissipation (Note 2)	P_D	500(3)	mW

NOTES: 1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (See power dissipation performance characteristic).
3. Maximum value at $T_A \leq 85°C$.

ORDERING INFORMATION

Device	Temperature Range	Package
LM833N	–40° to +85°C	Plastic DIP
LM833D		SO-8

2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_O = 0 V)	V_{IO}	—	0.3	5.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_O = 0 V, T_A = T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	—	2.0	—	μV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}	—	10	200	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}	—	300	1000	nA
Common Mode Input Voltage Range	V_{ICR}	— −12	+14 −14	+12 —	V
Large Signal Voltage Gain (R_L = 2.0 kΩ, V_O = ±10 V	A_{VOL}	90	110	—	dB
Output Voltage Swing: R_L = 2.0 kΩ, V_{ID} = 1.0 V R_L = 2.0 kΩ, V_{ID} = 1.0 V R_L = 10 kΩ, V_{ID} = 1.0 V R_L = 10 kΩ, V_{ID} = 1.0 V	 V_{O+} V_{O-} V_{O+} V_{O-}	 10 — 12 —	 13.7 −14.1 13.9 −14.7	 — −10 — −12	V
Common Mode Rejection (V_{in} = ±12 V)	CMR	80	100	—	dB
Power Supply Rejection (V_S = 15 V to 5.0 V, −15 V to −5.0 V)	PSR	80	115	—	dB
Power Supply Current (V_O = 0 V, Both Amplifiers)	I_D	—	4.0	8.0	mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, A_V = +1.0)	S_R	5.0	7.0	—	V/μs
Gain Bandwidth Product (f = 100 kHz)	GBW	10	15	—	MHz
Unity Gain Frequency (Open-Loop)	f_U	—	9.0	—	MHz
Unity Gain Phase Margin (Open-Loop)	θ_m	—	60	—	Deg
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	e_n	—	4.5	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	i_n	—	0.5	—	$pA/\sqrt{Hz}$
Power Bandwidth (V_O = 27 V_{p-p}, R_L = 2.0 kΩ, THD ≤ 1.0%)	BWP	—	120	—	kHz
Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	THD	—	0.002	—	%
Channel Separation (f = 20 Hz to 20 kHz)	C_S	—	−120	—	dB

Figure 1. Maximum Power Dissipation versus Temperature

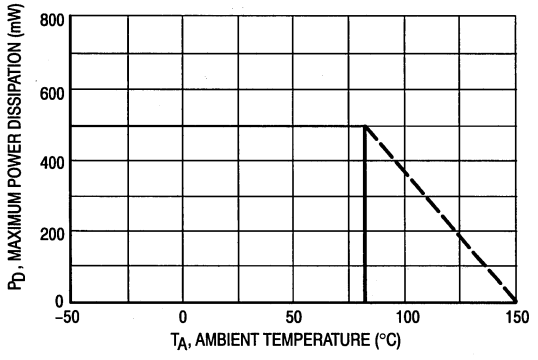


Figure 2. Input Bias Current versus Temperature

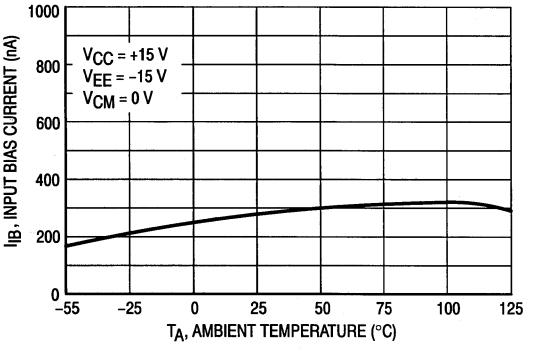


Figure 3. Input Bias Current versus Supply Voltage

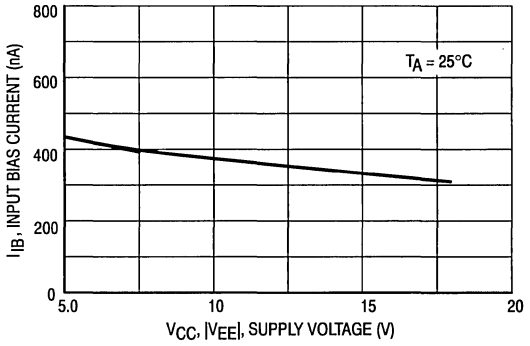


Figure 4. Supply Current versus Supply Voltage

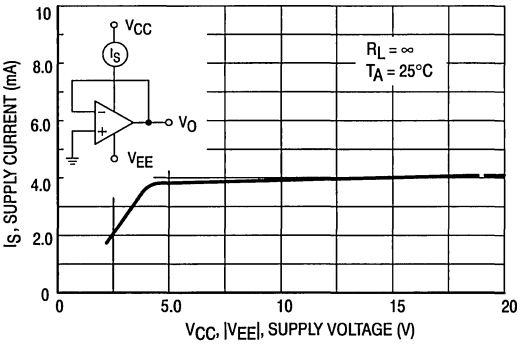


Figure 5. DC Voltage Gain versus Temperature

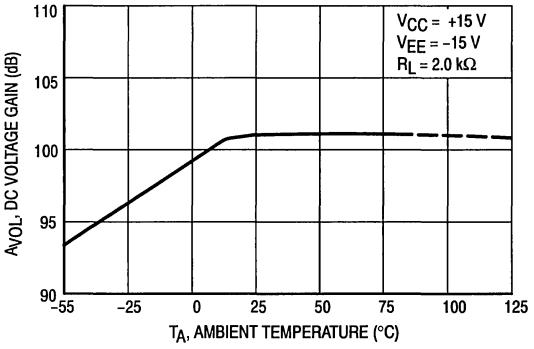


Figure 6. DC Voltage Gain versus Supply Voltage

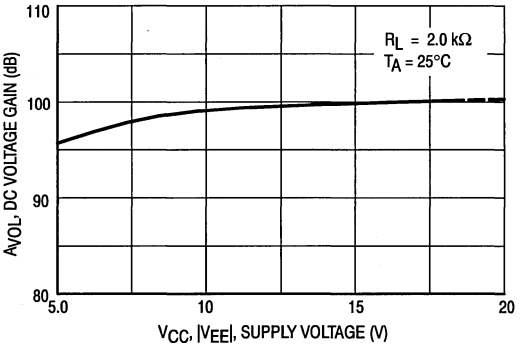


Figure 7. Open-Loop Voltage Gain and Phase versus Frequency

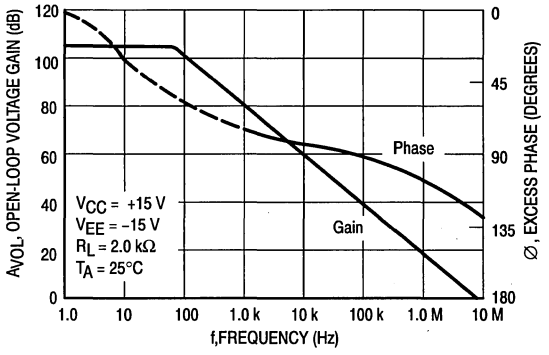


Figure 8. Gain Bandwidht Product versus Tmperature

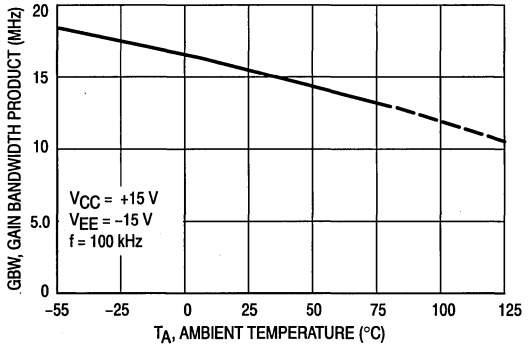


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Figure 9. Gain Bandwidth Product versus Supply Voltage

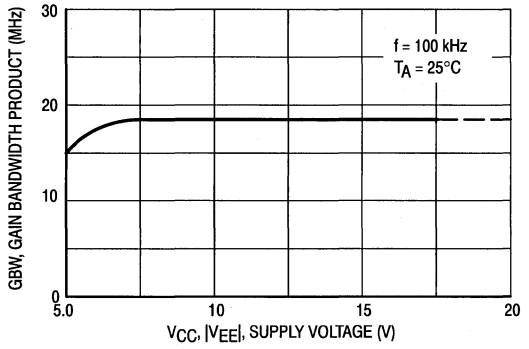


Figure 10. Slew Rate versus Temperature

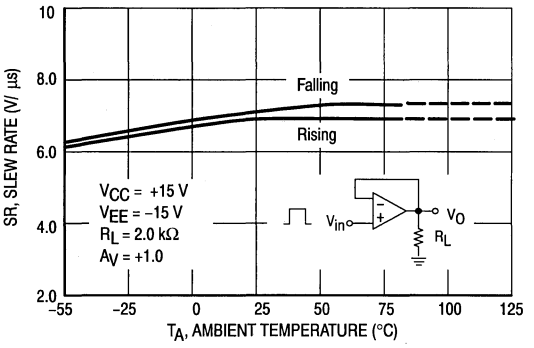


Figure 11. Slew Rate versus Supply Voltage

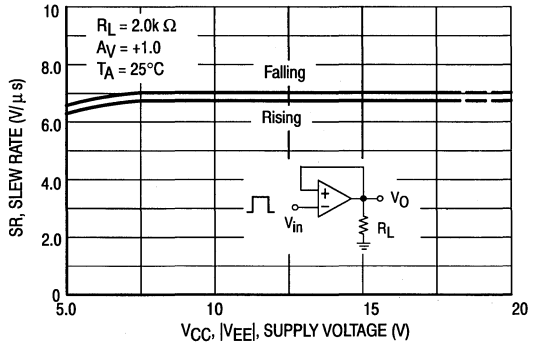


Figure 12. Output Voltage versus Frequency

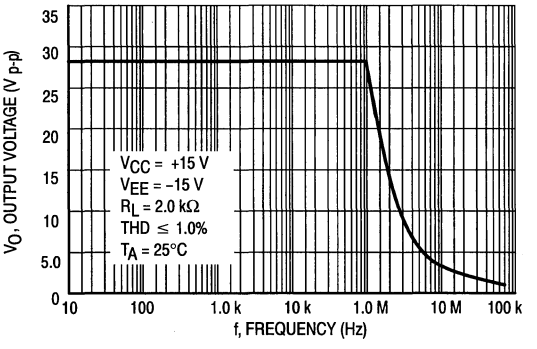


Figure 13. Maximum Output Voltage versus Supply Voltage

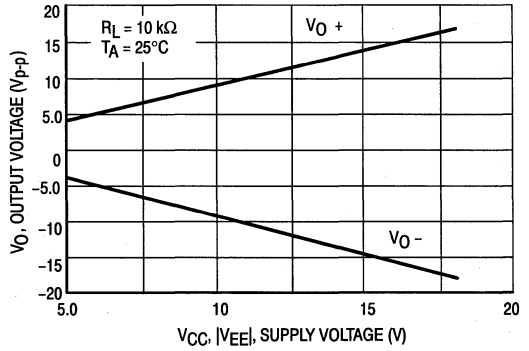


Figure 14. Output Saturation Voltage versus Temperature

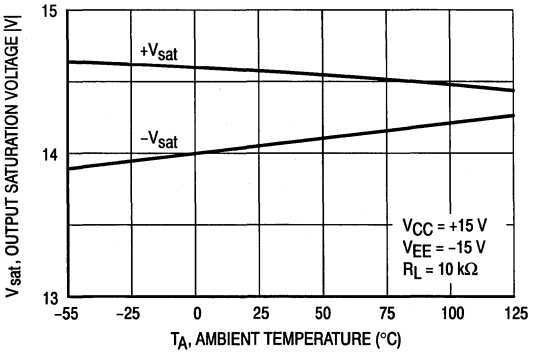


Figure 15. Power Supply Rejection versus Frequency

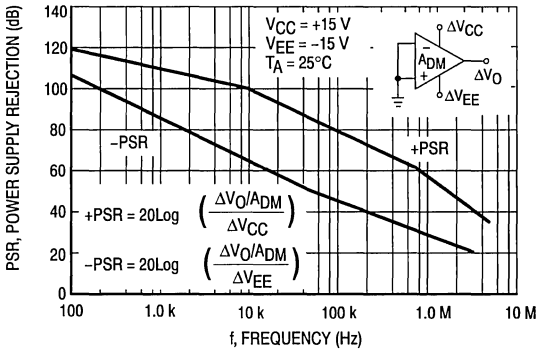


Figure 16. Common Mode Rejection versus Frequency

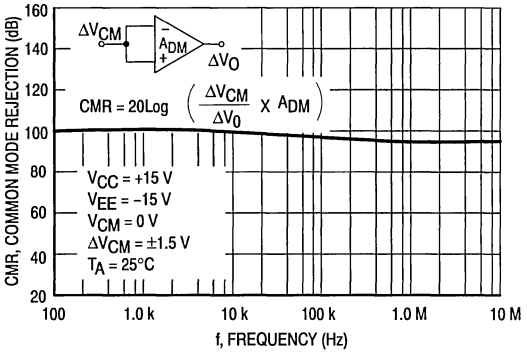


Figure 17. Total Harmonic Distortion versus Frequency

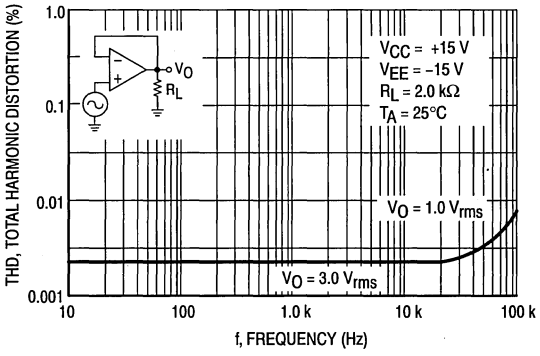


Figure 18. Input Referred Noise Voltage versus Frequency

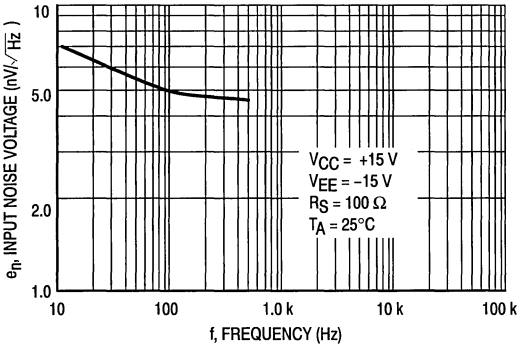


Figure 19. Input Referred Noise Current versus Frequency

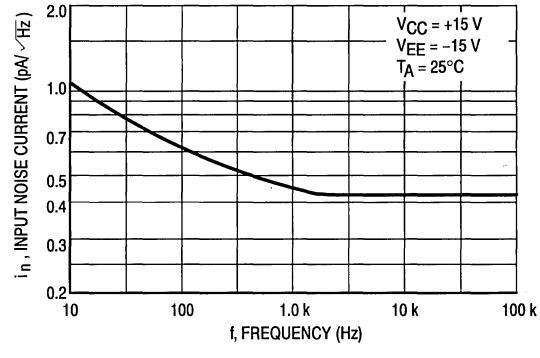


Figure 20. Input Referred Noise Voltage versus Source Resistance

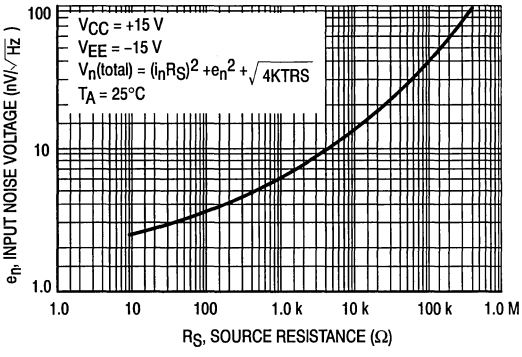


Figure 21. Inverting Amplifier

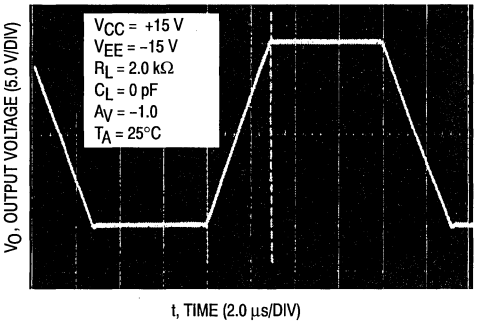


Figure 22. Noninverting Amplifier Slew Rate

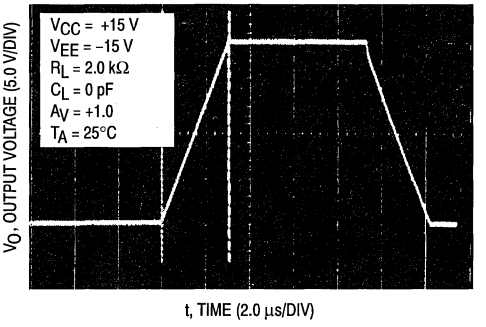
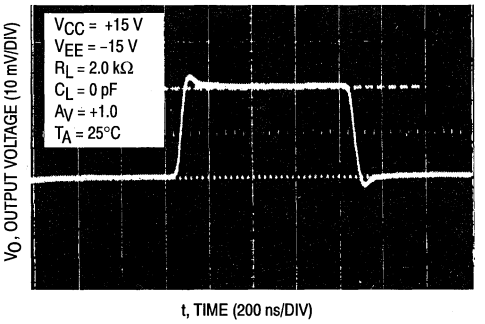


Figure 23. Noninverting Amplifier Overshoot



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1436,C
MC1536

High Voltage, Internally Compensated Operational Amplifier

OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC1436, C was designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- Maximum Supply Voltage: ±40 Vdc (MC1536)
- Output Voltage Swing:
  ±30 $V_{pk(min)}$ (V_{CC} = +36 V, V_{EE} = −36 V) (MC1536)
  ±22 $V_{pk(min)}$ (V_{CC} = +28 V, V_{EE} = −28 V)
- Input Bias Current: 20 nA max (MC1536)
- Input Offset Current: 3.0 nA max (MC1536)
- Fast Slew Rate: 2.0 V/μs typ
- Internally Compensated
- Offset Voltage Null Capability
- Input Overvoltage Protection
- A_{VOL}: 500,000 typ
- Characteristics Independent of Power Supply Voltages:
  (±5.0 Vdc to ±36 Vdc)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626

U SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

Figure 1. Differential Amplifier with ±20 V Common Mode Input Voltage Range

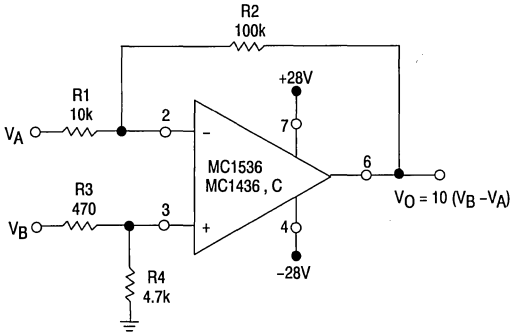
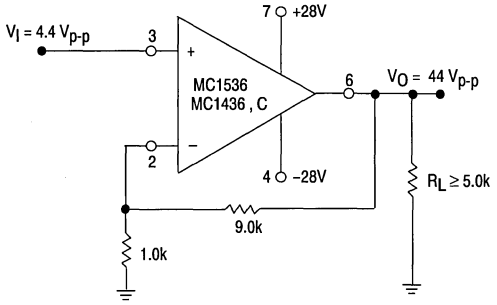
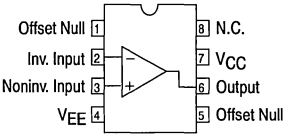


Figure 2. Typical Noninverting X10 Voltage Amplifier



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC1436CD,D	0° to +70°C	SO-8
MC1436P1,CP1		Plastic DIP
MC1436CU,U		Ceramic DIP
MC1536U	−55° to +125°C	Ceramic DIP

2

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	MC1536	MC1436	MC1436C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+40 –40	+34 –34	+30 –30	Vdc
Input Differential Voltage Range	V_{IDR}	Note 3			V
Input Common Mode Voltage Range	V_{ICR}	Note 3			V
Output Short Circuit Duration (V_{CC} = V_{EE} = 28 Vdc, V_O = 0)	t_{SC}	5.0			sec
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6			mW mW/°C
Operating Ambient Temperature Range	T_A	–55 to +125	0 to +70		°C
Storage Temperature Range	T_{stg}	–65 to +150			°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +28 V, V_{EE} = –28 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	MC1536 Min	MC1536 Typ	MC1536 Max	MC1436 Min	MC1436 Typ	MC1436 Max	MC1436C Min	MC1436C Typ	MC1436C Max	Unit
Input Bias Current T_A = +25°C T_A = T_{low} to T_{high} (See Note 1)	I_{IB}	 — —	 8.0 —	 20 35	 — —	 15 —	 40 55	 — —	 25 —	 90 —	nAdc
Input Offset Current T_A = +25°C T_A = +25°C to T_{high} T_A = T_{low} to +25°C	I_{IO}	 — — —	 1.0 — —	 3.0 4.5 7.0	 — — —	 5.0 — —	 10 14 14	 — — —	 10 — —	 25 — —	nAdc
Input Offset Voltage T_A = +25°C T_A = T_{low} to T_{high}	V_{IO}	 — —	 2.0 —	 5.0 7.0	 — —	 5.0 —	 10 14	 — —	 5.0 —	 12 —	mVdc
Differential Input Impedance (Open-loop, f ≤ 5.0 Hz) Parallel Input Resistance Parallel Input Capacitance	 rp Cp	 — —	 10 2.0	 — —	 — —	 10 2.0	 — —	 — —	 10 2.0	 — —	MΩ pF
Common Mode Input Impedance (f ≤ 5.0 Hz)	z_{ic}	—	250	—	—	250	—	—	250	—	MΩ
Input Common Mode Voltage Range	V_{ICR}	±24	±25	—	±22	±25	—	±18	±20	—	Vpk
Equivalent Input Noise Voltage (A_V = 100, R_S = 10 kΩ, f = 1.0 kHz, BW = 1.0 Hz)	e_n	—	50	—	—	50	—	—	50	—	$nV/(Hz)^{1/2}$
Common Mode Rejection (dc)	CMR	80	110	—	70	110	—	50	90	—	dB
Large Signal DC Open-Loop Voltage Gain (V_O = ±10 V, R_L = 100 kΩ) { T_A = +25°C { T_A = T_{low} to T_{high} (V_O = ±10 V, R_L = 10 kΩ, T_A = +25°C)	A_{VOL}	 100,000 50,000 —	 500,000 — 200,000	 — — —	 70,000 50,000 —	 500,000 — 200,000	 — — —	 50,000 — —	 500,000 — 200,000	 — — —	V/V
Power Bandwidth (Voltage Follower) (A_V = 1, R_L = 5.0 kΩ, THD ≤ 5%, V_O = 40 V_{p-p})	BWp	—	23	—	—	23	—	—	23	—	kHz
Unity Gain Crossover Frequency (Open-loop)	f_c	—	1.0	—	—	1.0	—	—	1.0	—	MHz
Phase Margin (Open-loop, Unity Gain)	ϕ_m	—	50	—	—	50	—	—	50	—	Degrees
Gain Margin	A_M	—	18	—	—	18	—	—	18	—	dB
Slew Rate (Unity Gain)	SR	—	2.0	—	—	2.0	—	—	2.0	—	V/μs
Output Impedance (f ≤ 5.0 Hz)	z_O	—	1.0	—	—	1.0	—	—	1.0	—	kΩ
Short Circuit Output Current	I_{SC}	—	±17	—	—	±17	—	—	±19	—	mAdc
Output Voltage Range (R_L = 5.0 kΩ) V_{CC} = +28 Vdc, V_{EE} = –28 Vdc V_{CC} = +36 Vdc, V_{EE} = –36 Vdc	V_O	 ±22 ±30	 ±23 ±32	 — —	 ±20 —	 ±22 —	 — —	 ±20 —	 ±22 —	 — —	V_{pk}
Power Supply Rejection V_{EE} = Constant, R_S ≤ 10 kΩ V_{CC} = Constant, R_S ≤ 10 kΩ	 PSR + PSR –	 — —	 15 15	 100 100	 — —	 35 35	 200 200	 — —	 50 50	 — —	μV/V
Power Supply Current (See Note 2)	I_{CC} I_{EE}	— —	2.2 2.2	4.0 4.0	— —	2.6 2.6	5.0 5.0	— —	2.6 2.6	5.0 5.0	mAdc
DC Quiescent Power Consumption (V_O = 0)	P_C	—	124	224	—	146	280	—	146	280	mW

NOTES: 1. T_{low} = 0°C for MC1436,C; –55°C for MC1536 T_{high} = +70°C for MC1436,C; +125°C for MC1536

2. V_{CC} = V_{EE} = 5.0 Vdc to 36 Vdc for MC1536
   V_{CC} = V_{EE} = 5.0 Vdc to 30 Vdc for MC1436
   V_{CC} = V_{EE} = 5.0 Vdc to 28 Vdc for MC1436C
3. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE} +3.0 V.

Figure 3. Low-Drift Sample and Hold

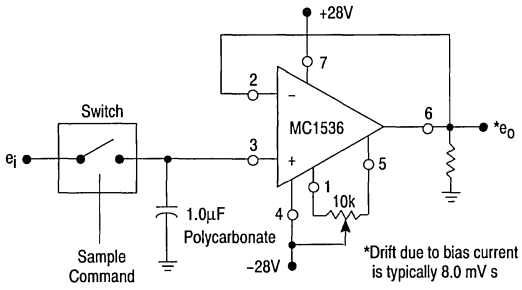


Figure 4. Power Bandwidth

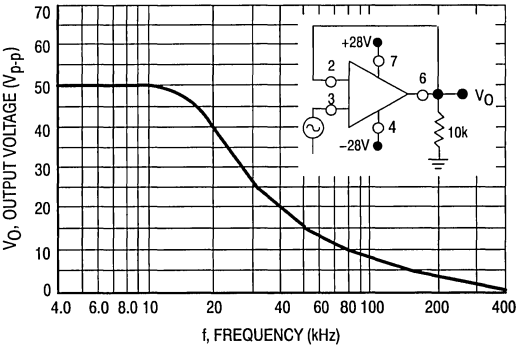


Figure 5. Peak Output Voltage Swing versus Power Supply Voltage

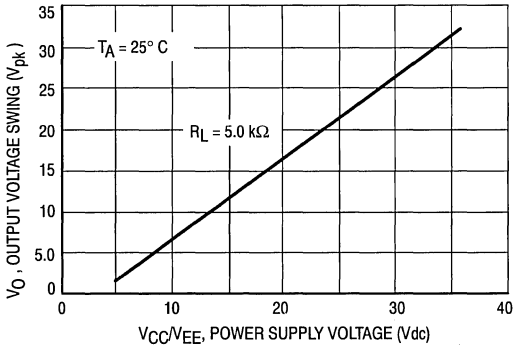


Figure 6. Open-Loop Frequency Response

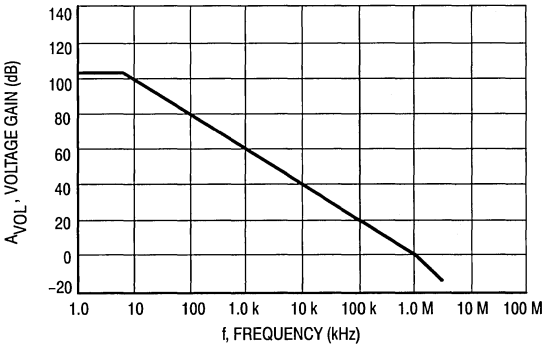


Figure 7. Output Short Circuit Current versus Temperature

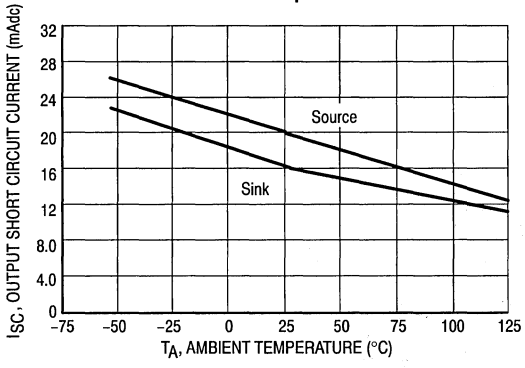
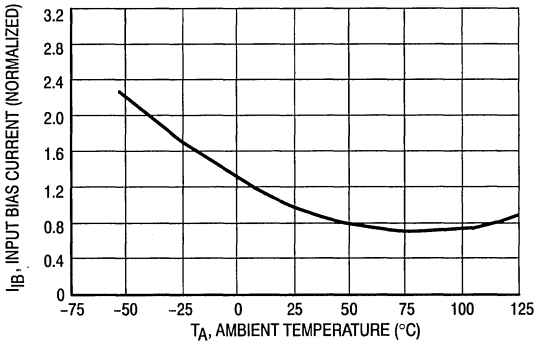


Figure 8. Input Bias Current versus Temperature



2

Figure 9. Inverting Feedback Model

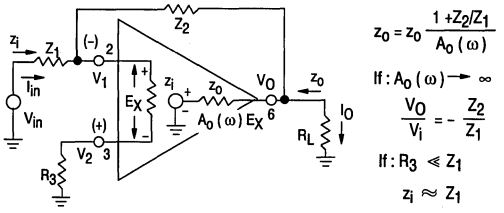


Figure 10. Noninverting Feedback Model

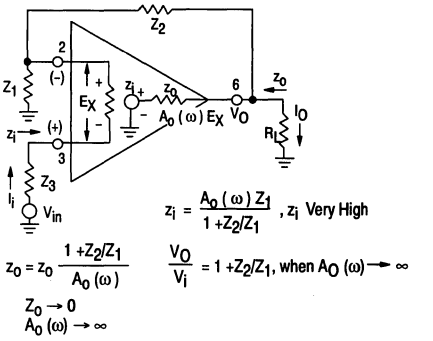


Figure 11. Audio Amplifier

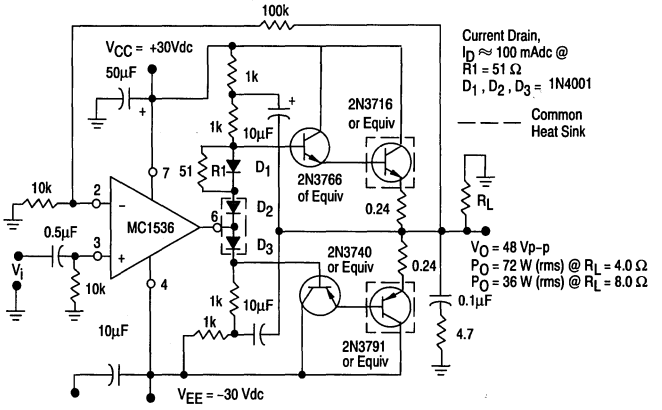


Figure 12. Voltage Controlled Current Source or Transconductance Amplifier with 0 V to 40 V Compliance

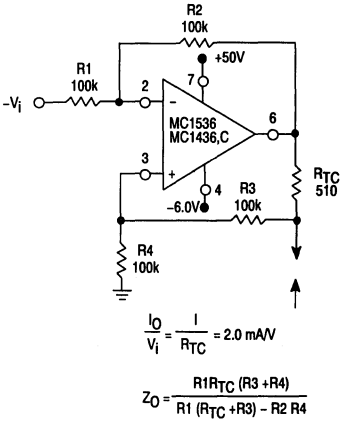


Figure 13. Representative Circuit Schematic

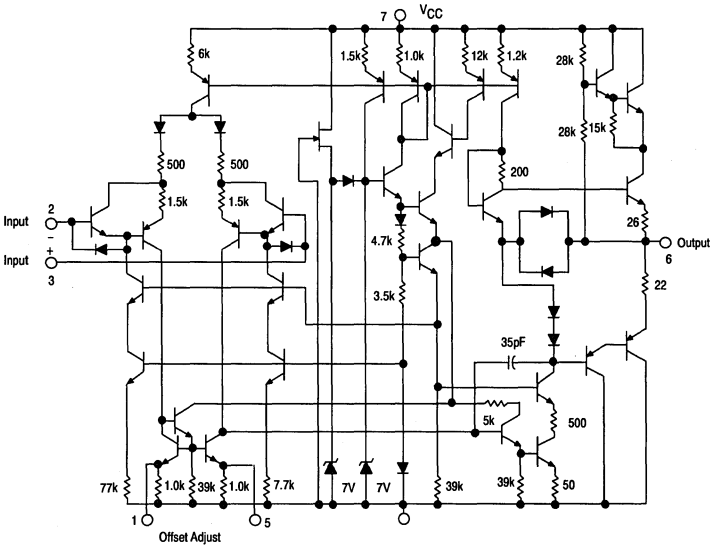
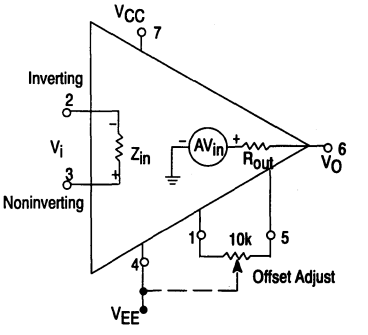


Figure 14. Equivalent Circuit



MC1445
MC1545

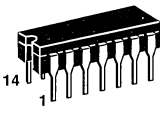
Gate Controlled Two Channel Input Wideband Amplifier

The MC1445/1545 was designed for use as a general purpose gated wideband amplifier, video switch, sense amplifier, multiplexer, modulator, FSK circuit, limiter, AGC circuit, or pulse amplifier.

- Large Bandwidth; 50 MHz Typical
- Channel Select Time of 20 ns Typical
- Differential Inputs and Differential Output

GATE CONTROLLED TWO CHANNEL INPUT WIDEBAND AMPLIFIER

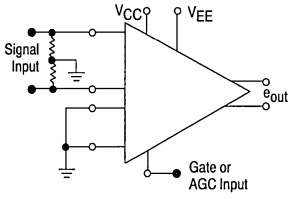
SILICON MONOLITHIC INTEGRATED CIRCUIT



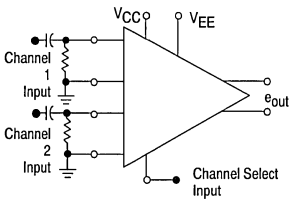
L SUFFIX
CERAMIC PACKAGE
CASE 632

Typical Applications

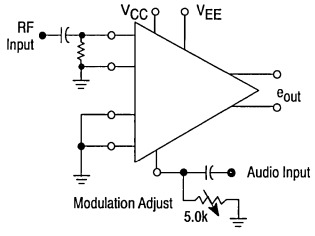
Video Switch or Differential Amplifier with AGC



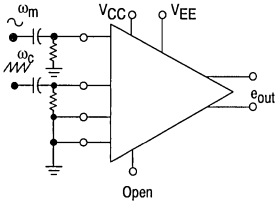
Multiplex or FSK



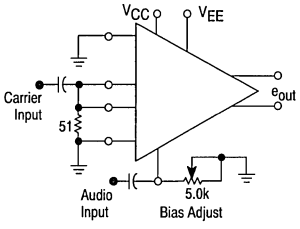
Amplitude Modulator



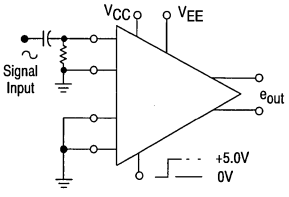
Pulse Width Modulator



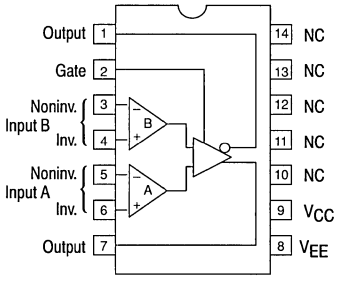
Balanced Modulator



Analog Switch



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
LM1445L	0° to +75°C	Ceramic DIP
LM1545L	−55° to +125°C	Ceramic DIP

2

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC} V_{EE}	+12 –12	Vdc
Input Differential Voltage Range		V_{IDR}	±5.0	V
Load Current		I_L	25	mA
Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T_A = +25°C		P_D	 625 5.0	 mW mW/°C
Operating Ambient Temperature Range	MC1445 MC1545	T_A	0 to +75 –55 to +125	°C
Storage Temperature Range		T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = –5.0 Vdc, @ T_A = +25°C, specifications apply to both input channels, unless otherwise noted.)

Characteristics	Fig. No.	Symbol	MC1545 Min	MC1545 Typ	MC1545 Max	MC1445 Min	MC1445 Typ	MC1445 Max	Unit
Single-Ended Voltage Gain	1, 12	A_{VS}	16	19	21	16	19.5	23	dB
Bandwidth	1, 12	BW	40	50	—	—	50	—	MHz
Input Impedance (f = 50 kHz)	5, 14	z_i	4.0	10	—	3.0	10	—	kΩ
Output Impedance (f = 50 kHz)	6, 15	z_o	—	25	—	—	25	—	Ω
Output Differential Voltage Range (R_L = 1.0 kΩ, f = 50 kHz)	4, 13	V_{ODR}	1.5	2.5	—	1.5	2.5	—	V_{p-p}
Input Bias Current	16	I_{IB}	—	15	25	—	15	30	μAdc
Input Offset Current	16	I_{IO}	—	2.0	—	—	2.0	—	μAdc
Input Offset Voltage	17	V_{IO}	—	1.0	5.0	—	—	7.5	mVdc
Quiescent Output dc Level	17	V_O	—	0.1	—	—	0.1	—	Vdc
Output dc Level Change (Gate Input Voltage Change: +5.0 V to 0 V)	17	ΔV_O	—	±15	—	—	±15	—	mV
Common Mode Rejection (f = 50 kHz)	9, 18	CMR	—	85	—	—	85	—	dB
Input Common Mode Voltage Range	18	V_{ICR}	—	±2.5	—	—	±2.5	—	V_{pk}
Gate Characteristics Gate Input Voltage – Low Logic State (Note 1) Gate Input Voltage – High Logic State (Note 2)	8	 $V_{IL(G)}$ $V_{IH(G)}$	 0.40 —	 0.70 1.5	 — 2.2	 0.2 —	 0.4 1.3	 — 3.0	Vdc
Gate Input Current – Low Logic State ($V_{IL(G)}$ = 0 V)	18	$I_{IL(G)}$	—	—	2.5	—	—	4.0	mA
Gate Input Current – High Logic State ($V_{IH(G)}$ = +5.0 V)	18	$I_{IH(G)}$	—	—	2.0	—	—	4.0	μA
Step Response (e_{in} = 20 mV)	19	t_{PLH} t_{PHL} t_{TLH} t_{THL}	— — — —	6.5 6.3 6.5 7.0	10 10 15 15	— — — —	6.5 6.3 6.5 7.0	— — — —	ns
Wideband Input Noise (5.0 Hz – 10 MHz, R_S = 50 Ω)	10, 20	e_n	—	25	—	—	25	—	μV(rms)
DC Power Consumption	11, 20	P_C	—	70	110	—	70	150	mW

NOTES: 1. $V_{IL(G)}$ is the gate voltage which results in channel A gain of unity or less and channel B gain of 16 dB or greater.
2. $V_{IH(G)}$ is the gate voltage which results in channel B gain of unity or less and channel A gain of 16 dB or greater.

Figure 1. Single-Ended Voltage Gain versus Frequency

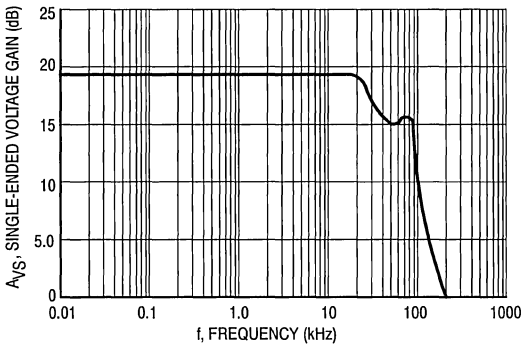


Figure 2. Single-Ended Voltage Gain versus Temperature

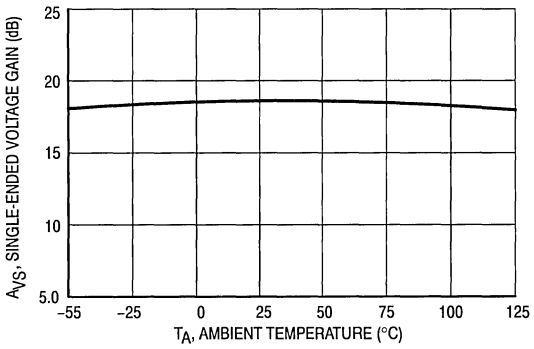


Figure 3. Voltage Gain versus Power Supply Voltages

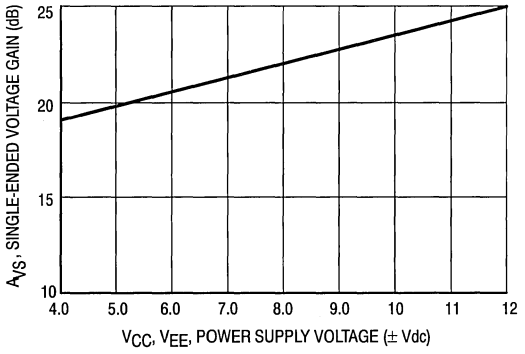


Figure 4. Output Voltage Swing versus Load Resistance

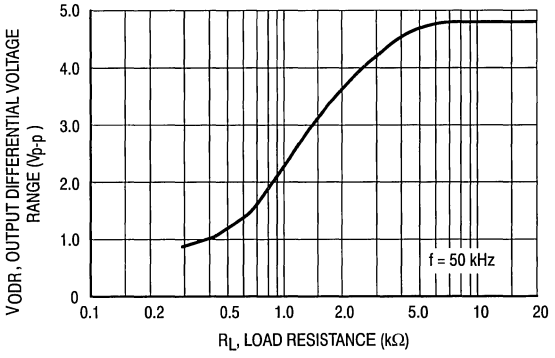


Figure 5. Input Cp and Rp versus Frequency (Both Channels)

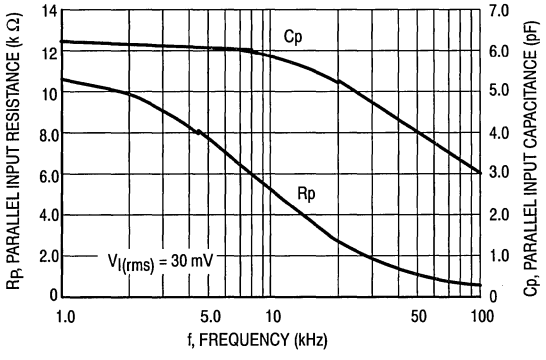
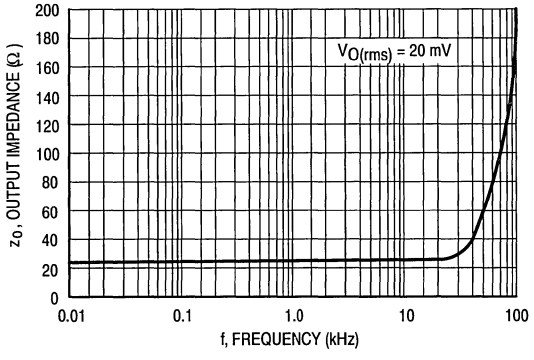


Figure 6. Output Impedance versus Frequency



2

Figure 7. Channel Separation versus Frequency

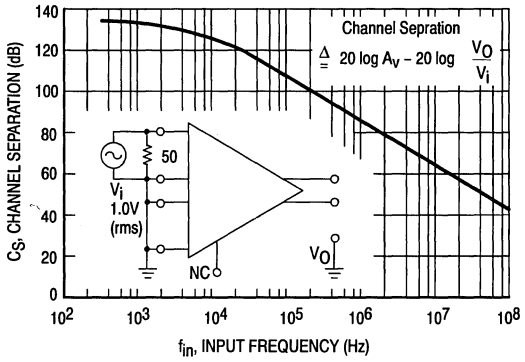


Figure 8. Gate Characteristics

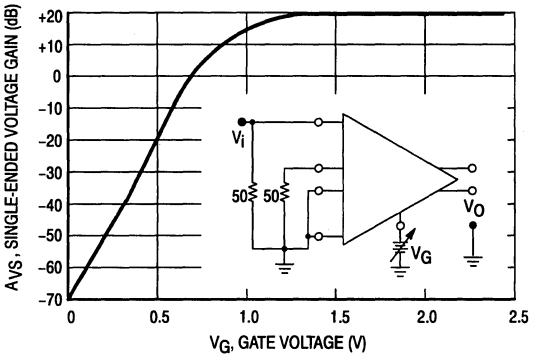


Figure 9. Common Mode Rejection Ratio versus Frequency

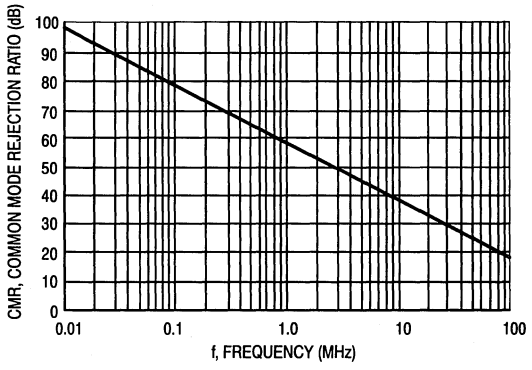


Figure 10. Input Wideband Noise versus Source Resistance

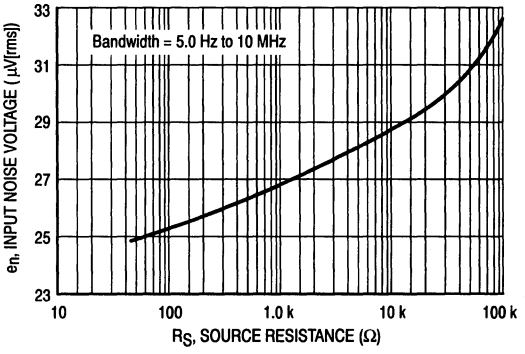


Figure 11. Circuit Schematic

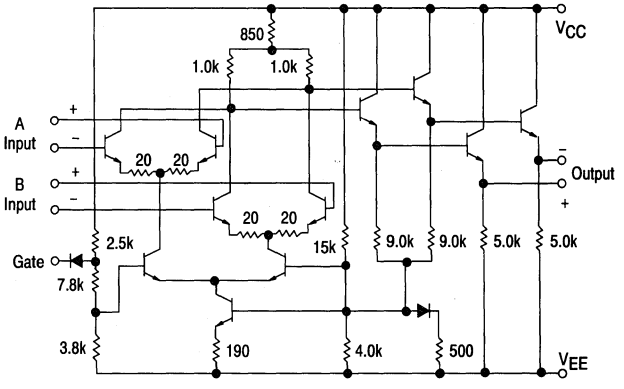


Figure 12. Single-Ended Voltage Gain and Bandwidth Test Circuit

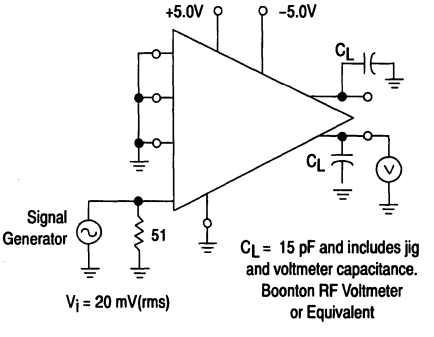


Figure 13. Output Voltage Swing Test Circuit

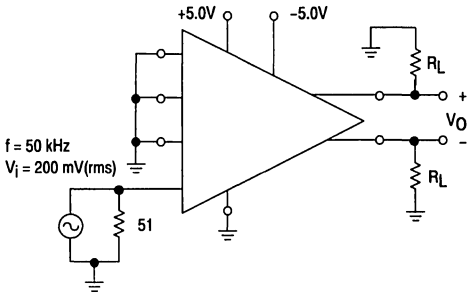


Figure 14. Input Impedance Test Circuit

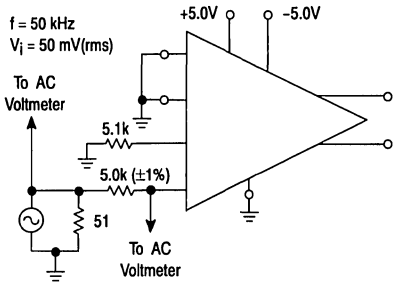


Figure 15. Output Impedance Test Circuit

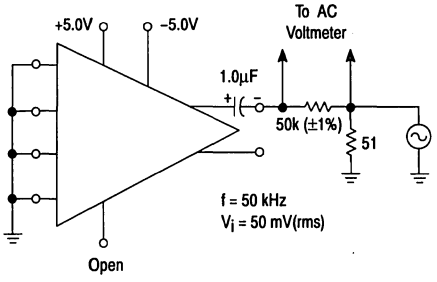


Figure 16. Input Bias Current and Input Offset Current Test Circuit

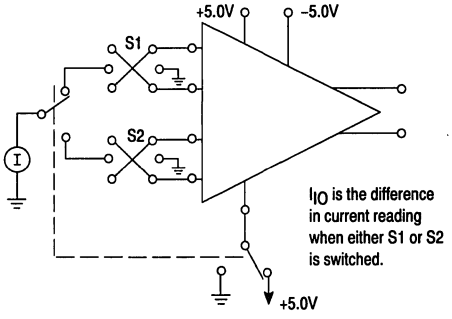


Figure 17. Input Offset Voltage and Quiescent Output Level Test Circuit

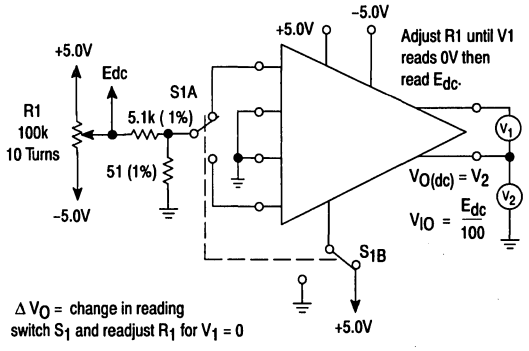


Figure 18. Gate Current (High and Low), Common Mode Rejection and Common Mode Input Range Test Circuit

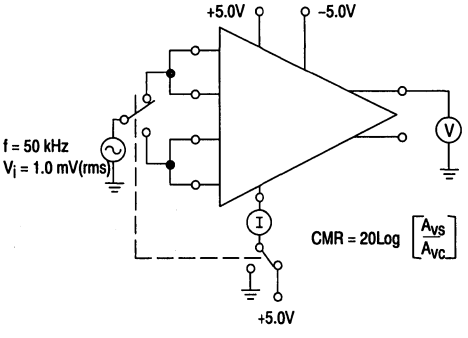


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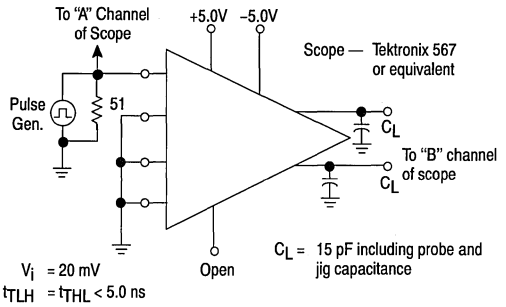
Figure 19. Propagation Delay, Rise and Fall Times Test Circuit



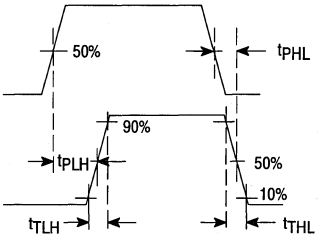


Figure 20. Power Dissipation and Wideband Input Noise Test Circuit

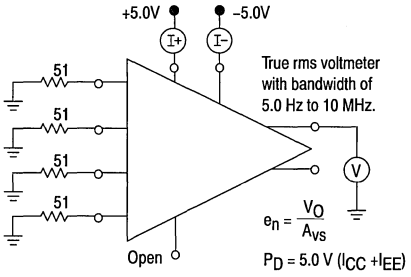
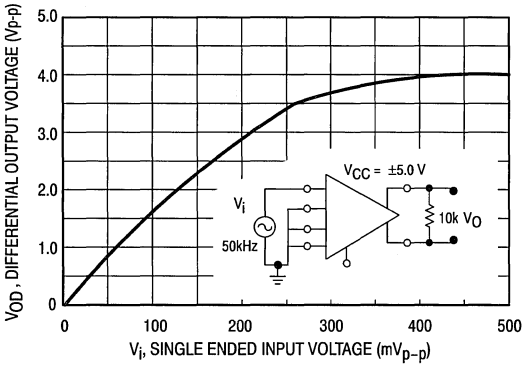


Figure 21. Limiting Characteristic



MC1458,C
MC1558

2

(DUAL MC1741)
DUAL
OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

(Dual MC1741)
Internally Compensated, High Performance Dual Operational Amplifiers

The MC1458/1558 was designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short Circuit Protection
- Wide Common Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch-Up

P1 SUFFIX
PLASTIC PACKAGE
CASE 626

U SUFFIX
CERAMIC PACKAGE
CASE 693

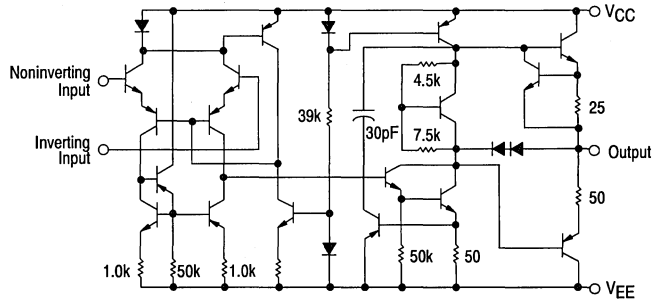
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

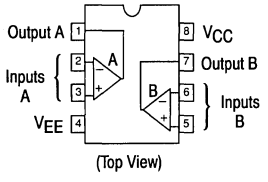
Rating	Symbol	MC1458	MC1558	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 −18	+22 −22	Vdc
Input Differential Voltage	V_{ID}	±30		V
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70	−55 to +125	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 −65 to +150 −55 to +125		°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150		°C

NOTES: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Supply voltage equal to or less than 15 V.

EQUIVALENT CIRCUIT SCHEMATIC



PIN CONNETIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC1458CD,D	0° to +70°C	SO-8
MC1458CP1,P1		Plastic DIP
MC1458CU,U		Ceramic DIP
MC1558U	−55° to +125°C	Ceramic DIP

2

ELECTRICAL CHARACTERISTICS — Note 1. (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le 10$ k)	V_{IO}	—	1.0	5.0	—	2.0	6.0	—	2.0	1.0	mV
Input Offset Current	I_{IO}	—	20	200	—	20	200	—	20	300	nA
Input Bias Current	I_{IB}	—	80	500	—	80	500	—	80	700	nA
Input Resistance	r_i	0.3	2.0	—	0.3	2.0	—	—	2.0	—	MΩ
Input Capacitance	C_i	—	1.4	—	—	1.4	—	—	1.4	—	pF
Offset Voltage Adjustment Range	V_{IOR}	—	±15	—	—	±15	—	—	±15	—	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	—	±12	±13	—	±11	±13	—	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k) (V_O = ±10 V, R_L = 10 k)	A_{VOL}	50 —	200 —	— —	20 —	200 —	— —	— 20	— 200	— —	V/mV
Output Resistance	r_o	—	75	—	—	75	—	—	75	—	Ω
Common Mode Rejection ($R_S \le 10$ k)	CMR	70	90	—	70	90	—	60	90	—	dB
Supply Voltage Rejection ($R_S \le 10$ k)	PSR	—	30	150	—	30	150	—	30	—	μV/V
Output Voltage Swing ($R_S \le 10$ k) ($R_S \le 2.0$ k)	V_O	±12 ±10	±14 ±13	— —	±12 ±10	±14 ±13	— —	±11 ±9.0	±14 ±13	— —	V
Output Short Circuit Current	I_{SC}	—	20	—	—	20	—	—	20	—	mA
Supply Currents (Both Amplifiers)	I_D	—	2.3	5.0	—	2.3	5.6	—	2.3	8.0	mA
Power Consumption	P_C	—	70	150	—	70	170	—	70	240	mW
Transient Response (Unity Gain) (V_I = 20 mV, $R_L \ge 2.0$ kΩ, $C_L \le 100$ pF) Rise Time (V_I = 20 mV, $R_L \ge 2.0$ kΩ, $C_L \le 100$ pF) Overshoot (V_I = 10 V, $R_L \ge 2.0$ kΩ, $C_L \le 100$ pF) Slew Rate	 t_{TLH} os SR	 — — —	 0.3 15 0.5	 — — —	 — — —	 0.3 15 0.5	 — — —	 — — —	 0.3 15 0.5	 — — —	 μs % V/μs

ELECTRICAL CHARACTERISTICS — Note 1. (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{high} to T_{low}, unless otherwise noted.)*

Characteristics	Symbol	MC1558			MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le 10$ kΩ)	V_{IO}	—	1.0	6.0	—	—	7.5	—	—	12	mV
Input Offset Current (T_A = 125°C) (T_A = −55°C) (T_A = 0° to +70°C)	I_{IO}	— — —	7.0 85 —	200 500 —	— — —	— — —	— — 300	— — —	— — —	— — 400	nA
Input Bias Current (T_A = 125°C) (T_A = −55°C) (T_A = 0° to +70°C)	I_{IB}	— — —	30 300 —	500 1500 —	— — —	— — —	— — 800	— — —	— — —	— — 1000	nA
Common Mode Input Voltage Range	V_{ICR}	±12	±13	—	—	—	—	—	—	—	V
Common Mode Rejection ($R_S \le 10$ k)	CMR	70	90		—	—	—	—	—	—	dB
Supply Voltage Rejection ($R_S \le 10$ k)	PSR	—	30	150	—	—	—	—	—	—	μV/V
Output Voltage Swing ($R_S \le 10$ k) ($R_S \le 2$ k)	V_O	±12 ±10	±14 ±13	— —	±12 ±10	±14 ±13	— —	— ±9.0	— ±13	— —	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2 k) (V_O = ±10 V, R_L = 10 k)	A_{VOL}	25 —	— —	— —	15 —	— —	— —	— 15	— —	— —	V/mV
Supply Currents (Both Amplifiers) (T_A = 125°C) (T_A = −55°C)	I_D	— —	— —	4.5 6.0	— —	— —	— —	— —	— —	— —	mA
Power Consumption (T_A = 125°C) (T_A = −55°C)	P_C	— —	— —	135 180	— —	— —	— —	— —	— —	— —	mW

*T_{low} = −55°C for MC1558 T_{high} = +125°C for MC1558
0°C for MC1458 +70°C for MC1458

NOTE: 1. Input pins of an unused amplifier must be grounded for split supply operation or biased at least 3.0 V above V_{EE} for single supply operation.

Figure 1. Burst Noise versus Source Resistance

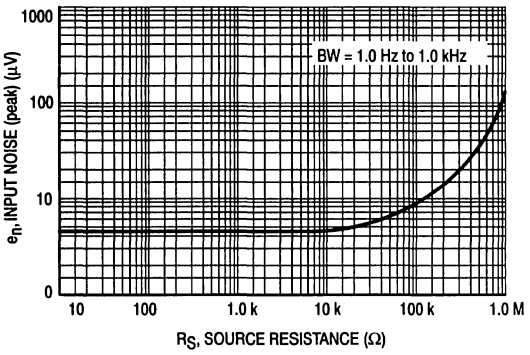


Figure 2. RMS Noise versus Source Resistance

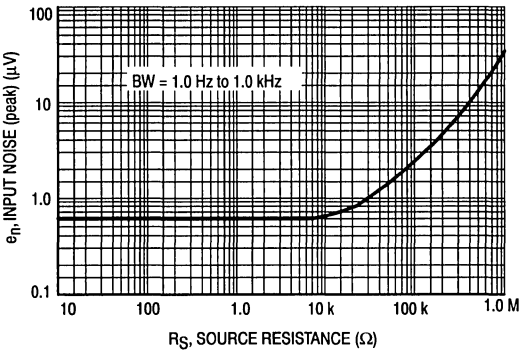


Figure 3. Output Noise versus Source Resistance

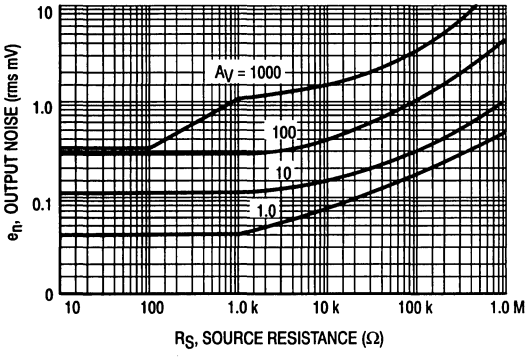


Figure 4. Spectral Noise Density

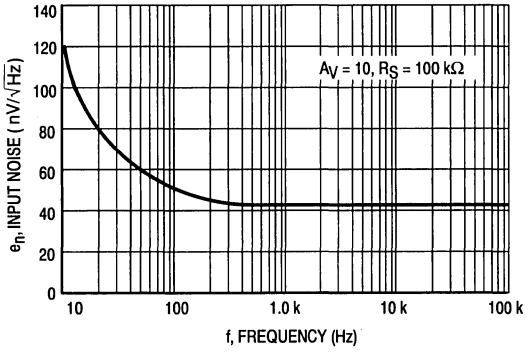
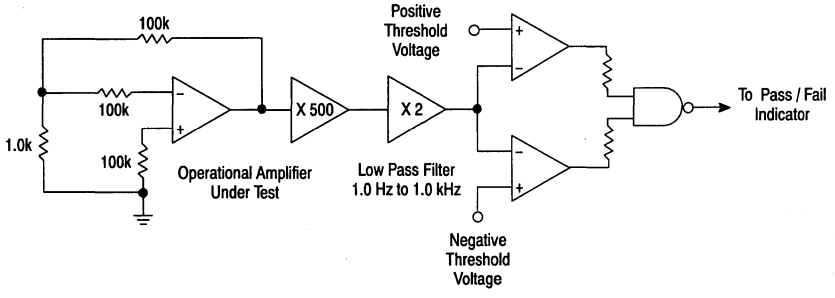


Figure 5. Burst Noise Test Circuit



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 sec and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier .

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Figure 6. Power Bandwidth (Large Signal Swing versus Frequency)

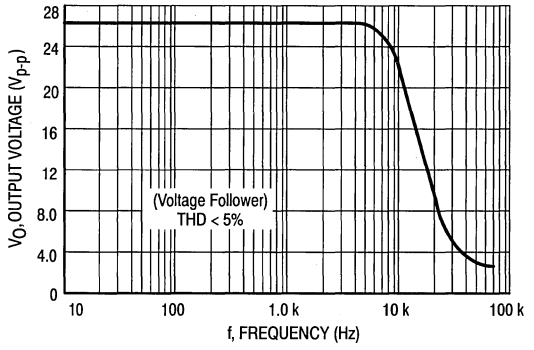


Figure 7. Open-Loop Freuqency Response

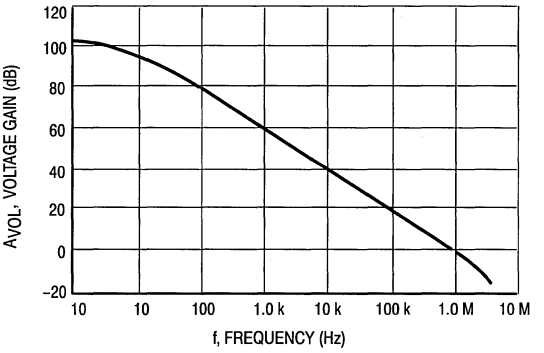


Figure 8. Positive Output Voltage Swing versus Load Resistance

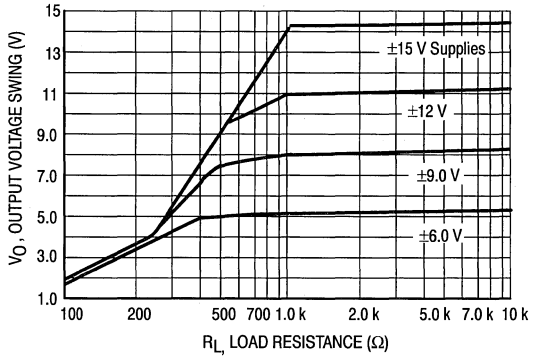


Figure 9. Negative Output Voltage Swing versus Load Resistance

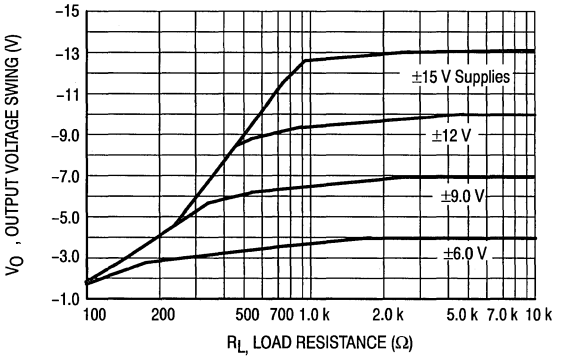


Figure 10. Output Voltage Swing versus Load Resistance (Single Supply Operation)

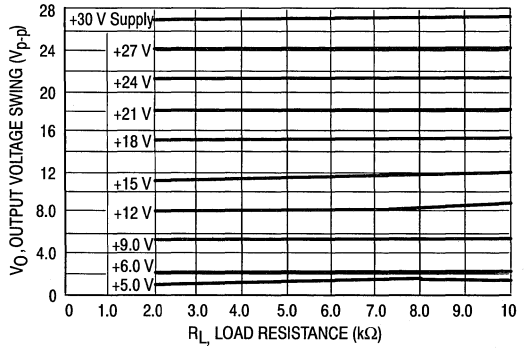


Figure 11. Single Supply Inverting Amplifier

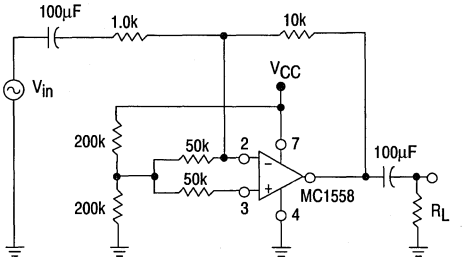


Figure 12. Noninverting Pulse Response

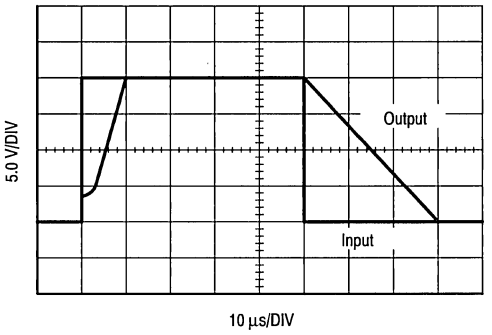


Figure 13. Transient Response Test Circuit

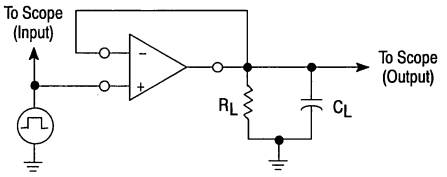
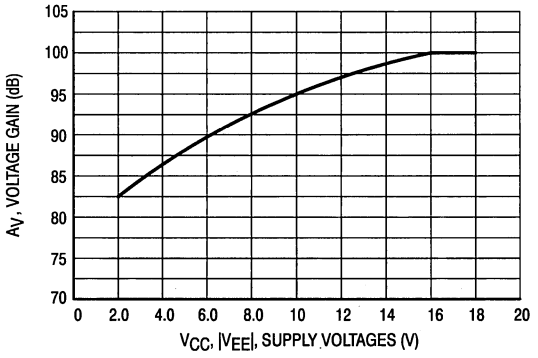


Figure 14. Open-Loop Voltage Gain versus Supply Voltage



MC1490P

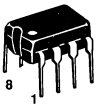
WIDEBAND AMPLIFIER WITH AGC

SILICON MONOLITHIC INTEGRATED CIRCUIT

RF/IF/Audio Amplifier

The MC1490P is an integrated circuit featuring wide-range AGC for use in RF/IF amplifiers and audio amplifiers over the temperature range, –40° to +85°C. See Motorola Applications Note AN513 for design details.

- High Power Gain: 50 dB Typ at 10 MHz
  45 dB Typ at 60 MHz
  35 dB Typ at 100 MHz
- Wide Range AGC: 60 dB Min, DC to 60 MHz
- 6.0 V to 15 V Operation, Single Polarity Supply
- See MC1350D for Surface Mount

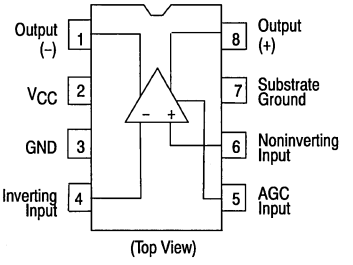


P SUFFIX
PLASTIC PACKAGE
CASE 626

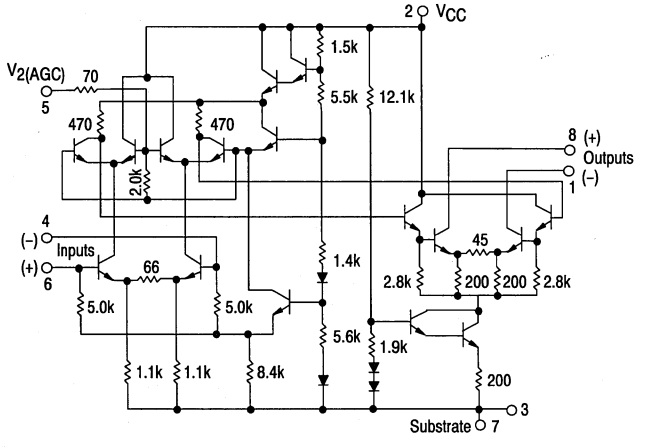
MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
AGC Supply	$V_{2(AGC)}$	V_{CC}	Vdc
Input Differential Voltage	V_{ID}	5.0	Vdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	+150	°C

PIN CONNECTIONS



Representative Circuit Schematic



Pins 3 and 7 should both be connected to circuit ground.

SCATTERING PARAMETERS
(V_{CC} = +12 Vdc, T_A = +25°C, Z_o = 50 Ω)

Parameter	Symbol	f = MHz Typ 30	f = MHz Typ 60	Unit
Input Reflection Coefficient	$\|S_{11}\|$ θ_{11}	0.95 –7.3	0.93 –16	— °
Output Reflection Coefficient	$\|S_{22}\|$ θ_{22}	0.99 –3.0	0.98 –5.5	— °
Forward Transmission Coefficient	$\|S_{21}\|$ θ_{21}	16.8 128	14.7 64.3	— °
Reverse Transmission Coefficient	S_{12} θ_{12}	0.00048 84.9	0.00092 79.2	— °

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, f = 60 MHz, BW = 1.0 MHz, T_A = 25°C)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Power Supply Current Drain	—	I_{CC}	—	—	17	mA
AGC Range (AGC) 5.0 V Min to 7.0 V Max	19	M_{AGC}	–60	—	—	dB
Output Stage Current (Sum of Pins 1 and 8)	—	I_O	4.0	—	7.5	mA
Single-Ended Power Gain R_S = R_L = 50 Ω	19	G_P	40	—	—	dB
Noise Figure R_S = 50 Ohms	19	NF	—	6.0	—	dB
Power Dissipation	—	P_D	—	168	204	mW

Figure 1. Unneutralized Power Gain versus Frequency (Tuned Amplifier, See Figure 19)

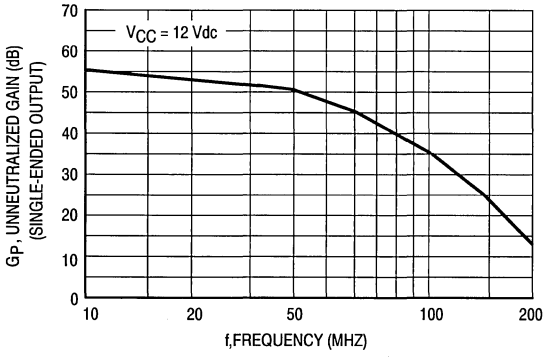


Figure 2. Voltage Gain versus Frequency (Video Amplifier, See Figure 21)

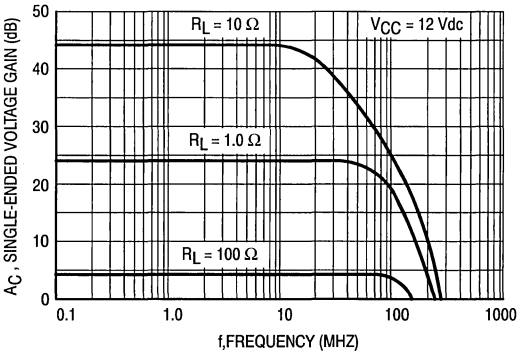


Figure 3. Dynamic Range: Output Voltage versus Input Voltage (Video Amplifier, See Figure 21)

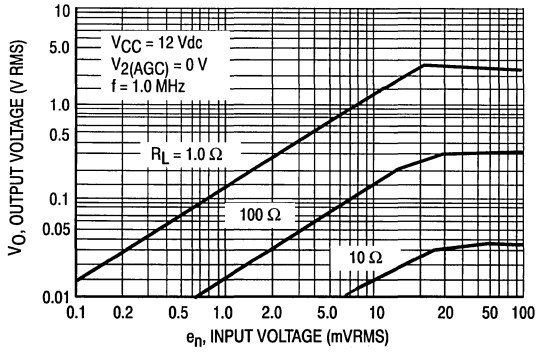
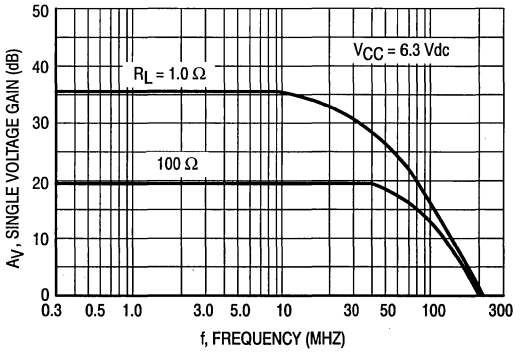


Figure 4. Voltage Gain versus Frequency (Video Amplifier, See Figure 21)



2

Figure 5. Voltage Gain and Supply Current versus Supply Voltage (Video Amplifier, See Figure 21)

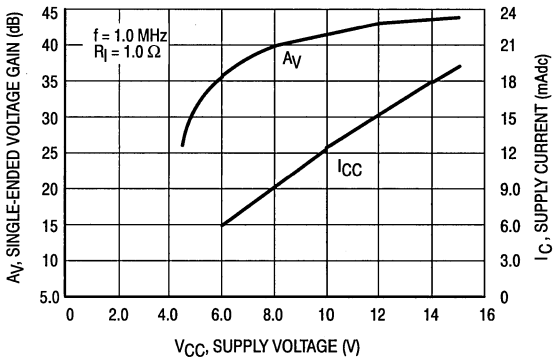


Figure 6. Typical Gain Reduction versus AGC Voltage

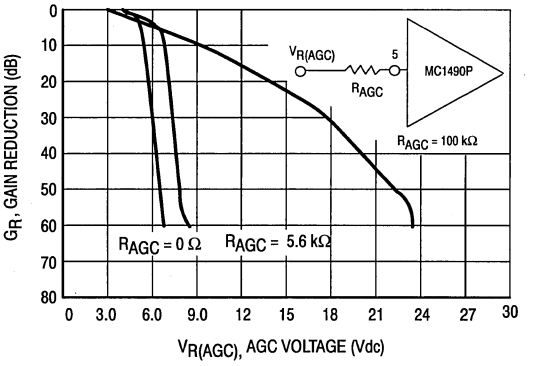


Figure 7. Typical Gain Reduction versus AGC Current

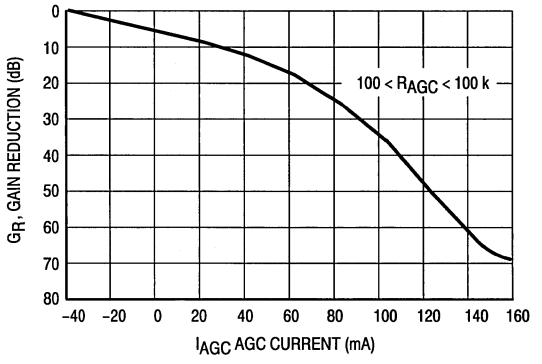


Figure 8. Fixed Tuned Power Gain Reduction versus Temperature (See Test Circuit, Figure 19)

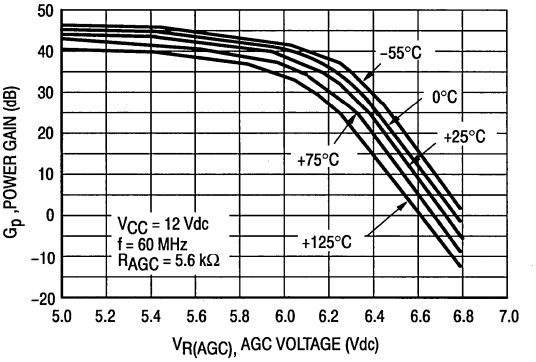


Figure 9. Power Gain versus Supply Voltage (See Test Circuit, Figure19)

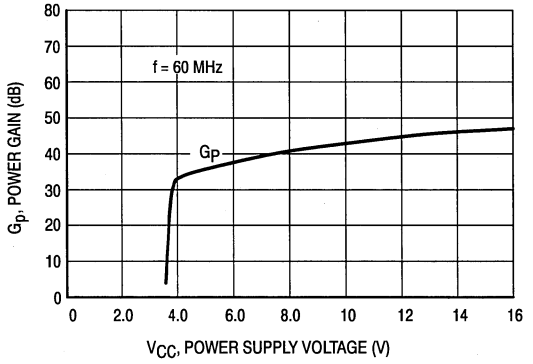


Figure 10. Noise Figure versus Frequency

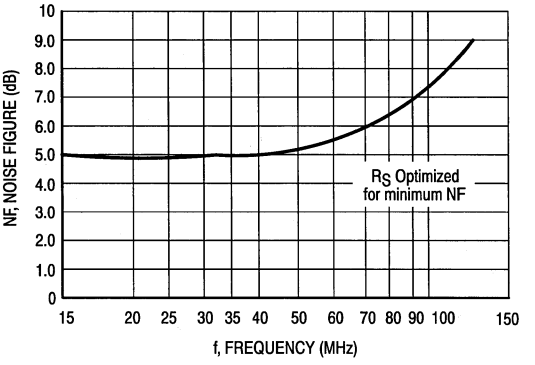


Figure 11. Noise Figure versus Source Resistance

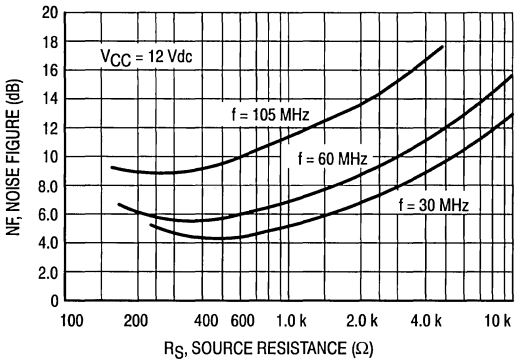


Figure 12. Noise Figure versus AGC Gain Reduction

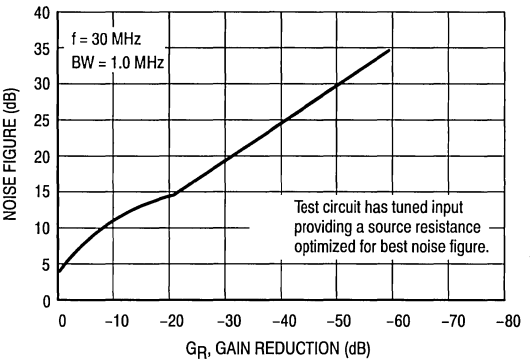


Figure 13. Harmonic Distortion versus AGC Gain Reduction for AM Carrier (For Test Circuit, See Figure 14)

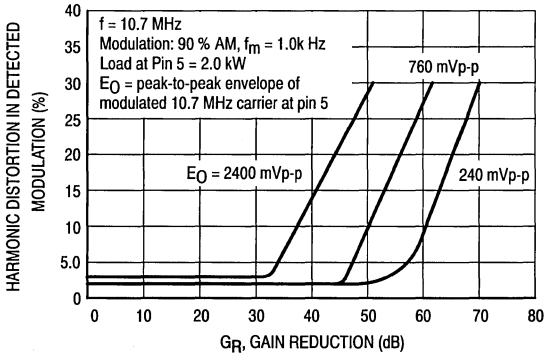
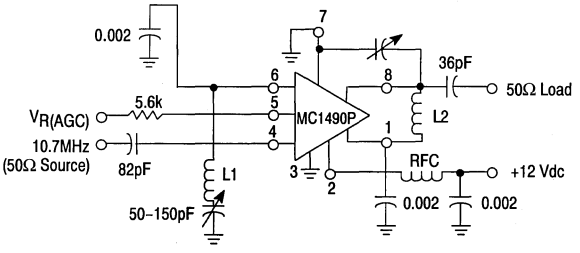


Figure 14. 10.7 MHz Amplifier Gain ≃ 55 dB, BW ≃ 100 kHz



L1 = 24 turns, #22 AWG wire on a T12-44 micro metal Toroid core (−124 pF)

L2 = 20 turns, #22 AWG wire on a T12-44 micro metal Toroid core (−100 pF)

2

Figure 15. S_{11} and S_{22}, Input and Output Reflection Coefficient

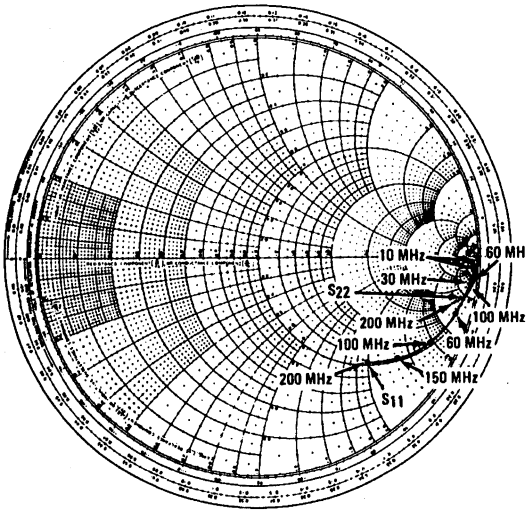


Figure 16. S_{11} and S_{22}, Input and Output Reflection Coefficient

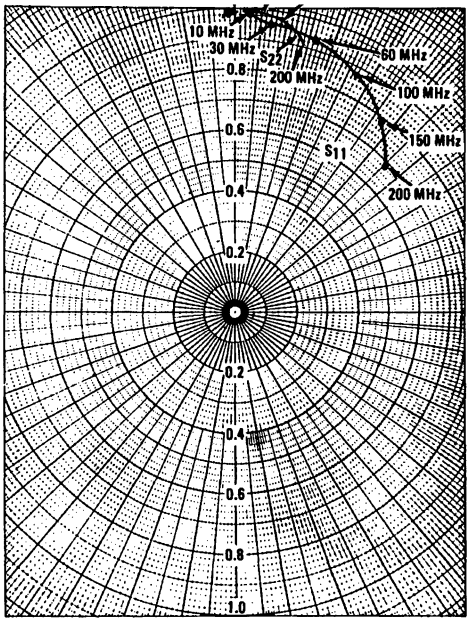


Figure 17. S_{21}, Forward Transmission Coefficient (Gain)

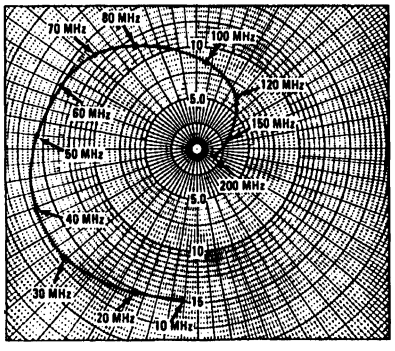


Figure 18. S_{12}, Reverse Transmission Coefficient (Feedback)

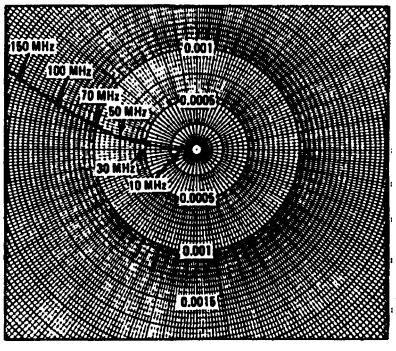


Figure 19. 60 MHz Power Gain Test Circuit

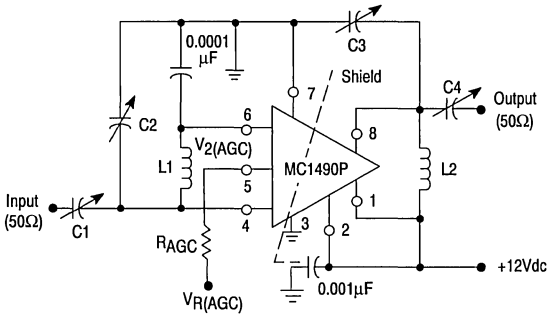


Figure 20. Procedure for Setup Using Figure 19

Test	e_{in}	$V_{2(AGC)}$	$R_{AGC}(k\Omega)$
M_{AGC}	2.23 mV (–40 dBm)	5.0 V to 7.0 V	0
G_P	1.0 mV (–47 dBm)	≤ 5.0	5.6
NF	1.0 mV (–47 dBm)	≤ 5.0	5.6

L1 = 7 turns, #20 AWG wire, 5/16″ Dia., 5/8″ long
L2 = 6 turns, #14 AWG wire, 9/16″ Dia., 3/4″ long

C1,C2,C3 = (1–30) pF
C4 = (1–10) pF

Figure 21. Video Amplifier

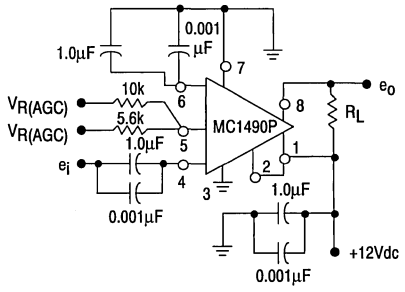
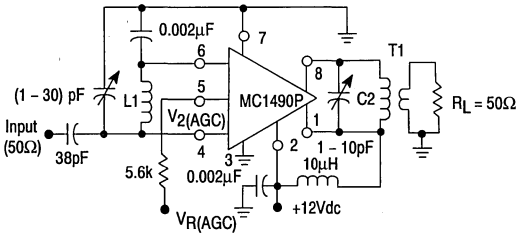
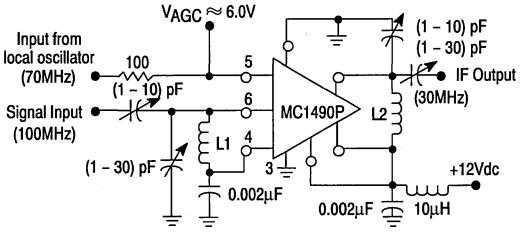


Figure 22. 30 MHz Amplifier (Power Gain = 50 dB, BW ≈ 1.0 MHz)



L1 = 12 turns, #22 AWG wire on a Toroid core, (T37-6 micro metal or equiv)
T1: Primary = 17 turns, #20 AWG wire on a Toroid core, (T44-6)
Secondary = 2 turns, #20 AWG wire

Figure 23. 100 MHz Mixer



L1 = 5 turns, #16 AWG wire, 1/4″, ID, 5/8″, long
L2 = 16 turns, #20 AWG wire on a Toroid core, (T44-6)

DESCRIPTION OF SPEECH COMPRESSOR

The amplifier drives the base of a PNP MPS6517 operating common-emitter with a voltage gain of approximately 20. The control R1 varies the quiescent Q point of this transistor so that varying amounts of signal exceed the level V_r. Diode D1 rectifies the positive peaks of Q1's output only when these peaks are greater than $V_r \approx 7.0$ V. The resulting output is filtered by C_X, R_X.

R_X controls the charging time constant or attack time. C_X is involved in both charge and discharge. R2 (the 150 kΩ and input resistance of the emitter-follower Q2) controls the decay time. Making the decay long and attack short is accomplished by making R_X small and R2 large. (A Darlington emitter-follower may be needed if extremely slow decay times are required.)

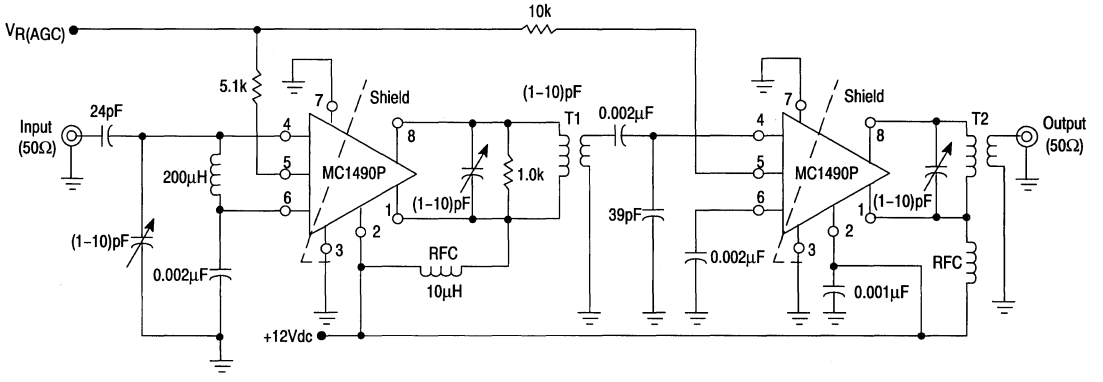
The emitter-follower Q2 drives the AGC Pin 5 of the MC1490P and reduces the gain. R3 controls the slope of signal compression.

Table 1. Distortion versus Frequency

Frequency	Distortion		Distortion	
	10 mV e_i	100 mV e_i	10 mV e_i	100 mV e_i
100 Hz	3.5%	12%	15%	27%
300 Hz	2%	10%	6%	20%
1.0 kHz	1.5%	8%	3%	9%
10 kHz	1.5%	8%	1%	3%
100 kHz	1.5%	8%	1%	3%
	Notes 1 and 2		Notes 3 and 4	

NOTES: (1) Decay = 300 ms
Attack = 20 ms
(2) C_X = 7.5 μF
R_X = 0 (Short)
(3) Decay = 20 ms
Attach = 3.0 ms
(4) C_X = 0.68 μF
R_X = 1.5 kΩ

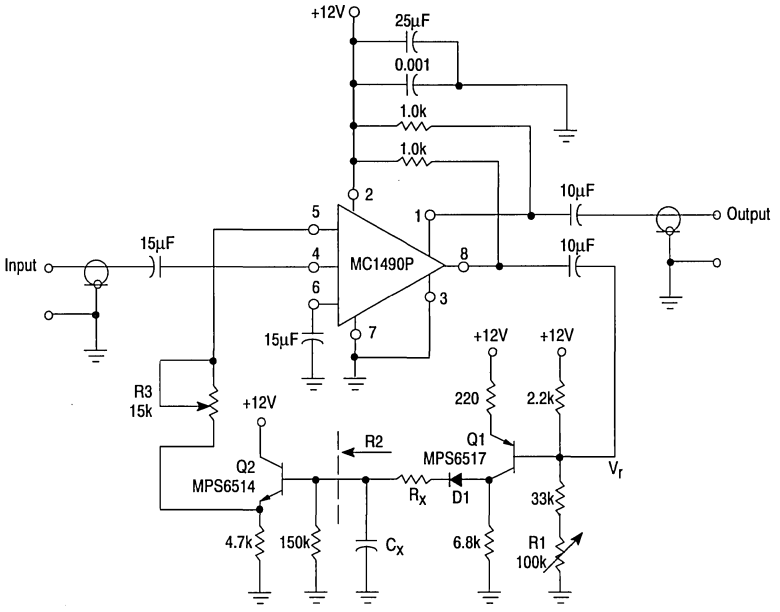
Figure 24. Two-Stage 60 MHz if Amplifier (Power Gain ≈ 80 dB, BW ≈ 1.5 MHz)



T1: Primary Winding = 15 turns, #22 AWG wire, 1/4″ ID Air Core
Secondary Winding = 4 turns, #22 AWG wire,
Coefficient of Coupling ≈ 1.0

T1: Primary Winding = 10 turns, #22 AWG wire, 1/4″ ID Air Core
Secondary Winding = 2 turns, #22 AWG wire,
Coefficient of Coupling ≈ 1.0

Figure 25. Speech Compressor



MC1733CB

DIFFERENTIAL VIDEO WIDEBAND AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

Differential Video Amplifier

The MC1733CB is a wideband amplifier with differential input and differential output. Gain is fixed at 10 V, 100 V, or 400 V without external components. With the addition of one external resistor, gain becomes adjustable from 10 V to 400 V.

- Bandwidth: 120 MHz Typical @ A_{vd} = 10
- Rise Time: 2.5 ns Typical @ A_{vd} = 10
- Propagation Delay Time: 3.6 ns Typical @ A_{vd} = 10

Figure 1. Basic Circuit

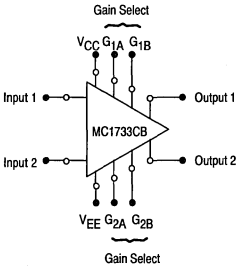


Figure 2. Voltage Gain Adjust Circuit

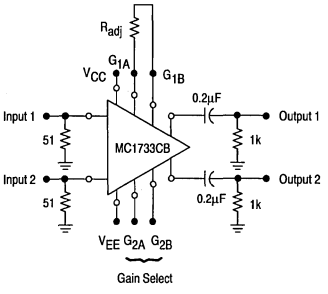
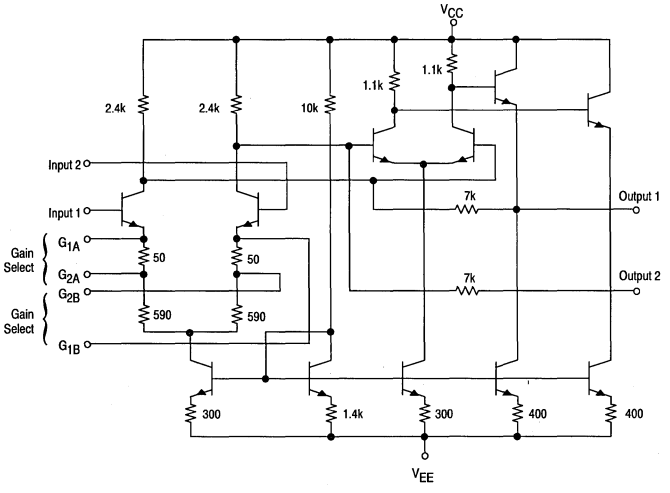
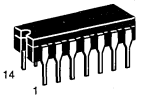


Figure 3. Equivalent Circuit Schematic

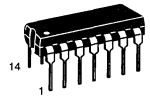


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

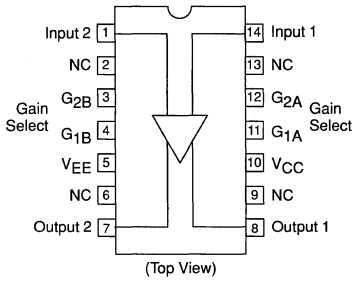
L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC1733CBD	0° to +70°C	SO-14
MC1733CBL		Plastic DIP
MC1733CBP		Ceramic DIP

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+8.0 –8.0	V
Differential Input Voltage	V_{in}	±5.0	V
Common Mode Input Voltage	V_{ICM}	±6.0	V
Output Current	I_O	10	mA
Internal Power Dissipation	P_D	500	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = –6.0 Vdc, @ +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Differential Voltage Gain	A_{vd}				V/V
Gain 1 (Note 2)		250	400	600	
Gain 2 (Note 3)		80	100	120	
Gain 3 (Note 4)		8.0	10	12	
Bandwidth (R_S = 50 Ω)	BW				MHz
Gain 1		—	40	—	
Gain 2		—	90	—	
Gain 3		—	120	—	
Rise Time (R_S = 50 Ω, V_O = 1.0 V_{p-p})	t_{TLH}				ns
Gain 1	t_{THL}	—	10.5	—	
Gain 2		—	4.5	—	
Gain 3		—	2.5	—	
Propagation Delay (R_S = 50 Ω, V_O = 1.0 V_{p-p})	t_{PLH}				ns
Gain 1	t_{PHL}	—	7.5	—	
Gain 2		—	6.0	—	
Gain 3		—	3.6	—	
Input Resistance	R_{in}				kΩ
Gain 1		—	4.0	—	
Gain 2		10	30	—	
Gain 3		—	250	—	
Input Capacitance (Gain 2)	C_{in}	—	2.0	—	pF
Input Offset Current (Gain 3)	$\|I_{IO}\|$	—	0.4	5.0	μA
Input Bias Current (Gain 3)	I_{IB}	—	9.0	30	μA
Input Noise Voltage (R_S = 50 Ω, BW = 1.0 kHz to 10 MHz)	V_n	—	12	—	μV(rms)
Input Voltage Range (Gain 2)	V_{in}	±1.0	—	—	V
Common Mode Rejection	CMR				dB
Gain 2 (V_{CM} = ±1.0 V, f ≤ 100 kHz)		60	86	—	
Gain 2 (V_{CM} = ±1.0 V, f = 5.0 MHz)		—	60	—	
Supply Voltage Rejection Gain 2 (Δ V_S = ±0.5 V)	PSR	50	70	—	dB
Output Offset Voltage	V_{OO}				V
Gain 1		—	0.6	2.0	
Gain 2 and Gain 3		—	0.35	1.5	
Output Common Mode Voltage (Gain 3)	V_{CMO}	2.4	2.9	3.4	V
Output Voltage Swing (Gain 2)	V_O	3.0	4.0	—	V_{p-p}
Output Sink Current (Gain 2)	I_{Sink}	2.5	3.6	—	mA
Output Resistance	R_{out}	—	20	—	Ω
Power Supply Current (Gain 2)	I_D	—	18	24	mA

2

ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 Vdc, V_{EE} = −6.0 Vdc, @ T_A = T_{high} to T_{low}, unless otherwise noted.)*

Characteristics	Symbol	Min	Typ	Max	Unit
Differential Voltage Gain	A_{VD}				V/V
Gain 1 (Note 2)		250	—	600	
Gain 2 (Note 3)		80	—	120	
Gain 3 (Note 4)		8.0	—	12	
Input Resistance Gain 2	R_{in}	8.0	—	—	kΩ
Input Offset Current (Gain 3)	$\|I_O\|$	—	—	6.0	μA
Input Bias Current (Gain 3)	I_{IB}	—	—	40	μA
Input Voltage Range (Gain 2)	V_{in}	±1.0	—	—	V
Common Mode Rejection Gain 2 (V_{CM} = ±1.0 V, f ≤ 100 kHz)	CMR	50	—	—	dB
Supply Voltage Rejection Gain 2 (Δ V_S = ±0.5 V)	PSR	50	—	—	dB
Output Offset Voltage	V_{OO}				V
Gain 1		—	—	1.5	
Gain 2 and Gain 3		—	—	1.5	
Output Voltage Swing (Gain 2)	V_O	2.5	—	—	V_{p-p}
Output Sink Current (Gain 2)	I_O	2.5	—	—	mA
Power Supply Current (Gain 2)	I_D	—	—	27	mA

*T_{low} = 0°C for MC1733. T_{high} = +70°C for MC1733C.

NOTES: 1. Derate dual-in-line package at 9.0 mW/°C for operation at ambient temperatures above 100°C (see Figure 4). If operation at high ambient temperatures is required a heatsink may be necessary to limit maximum junction temperature at 150°C.
2. Gain Select pins G_{1A} and G_{1B} connected together.
3. Gain Select pins G_{2A} and G_{2B} connected together.
4. All Gain Select pins open.

Figure 4. Maximum Allowable Power Dissipation

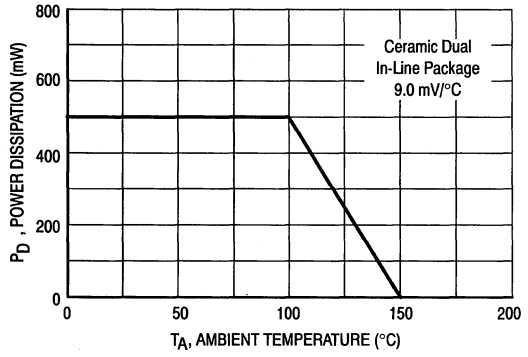


Figure 5. Supply Current versus Temperature

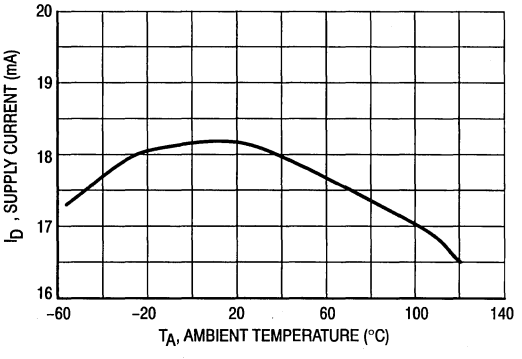


Figure 6. Supply Current versus Supply Voltage

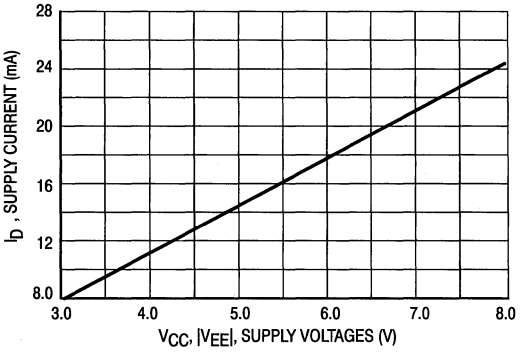


Figure 7. Gain versus Temperature

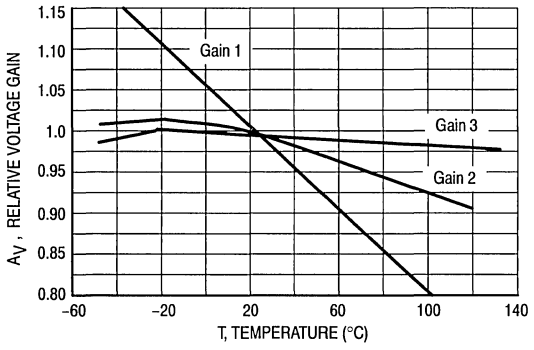


Figure 8. Gain versus Frequency

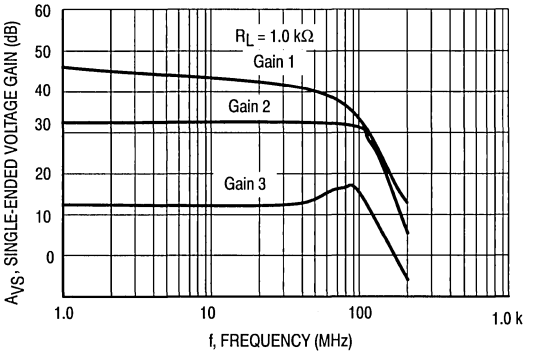


Figure 9. Gain versus Supply Voltage

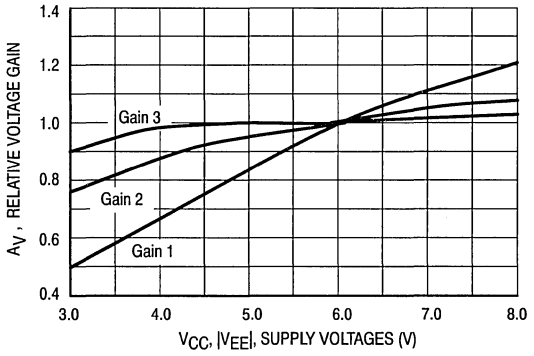


Figure 10. Gain versus R_{adjust}

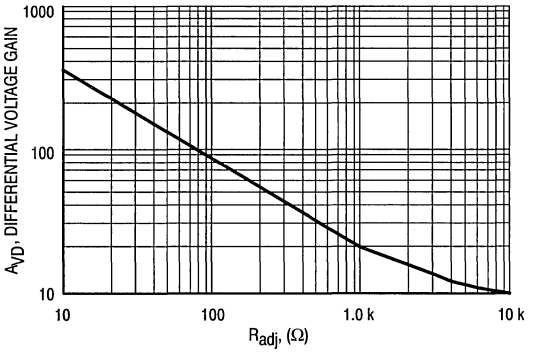


Figure 11. Gain versus Frequency and Supply Voltage

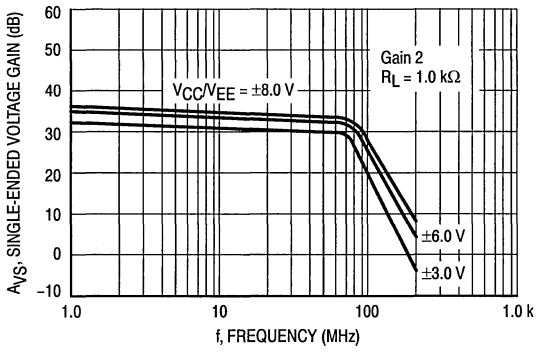
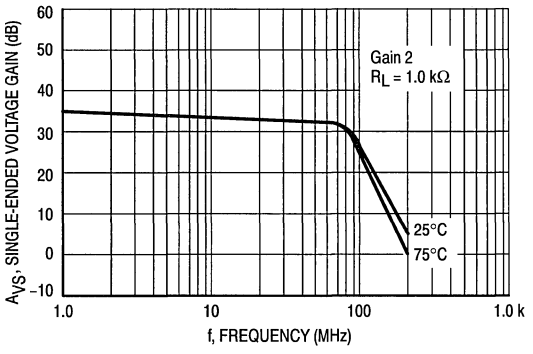


Figure 12. Gain versus Frequency and Temperature



2

Figure 13. Pulse Response versus Gain

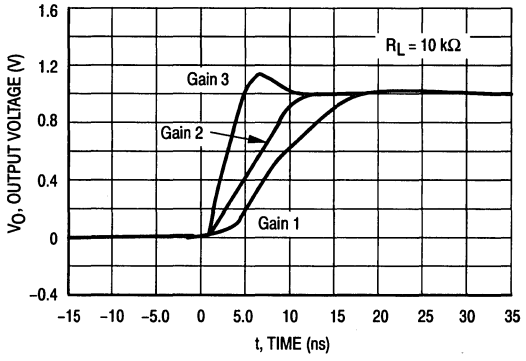


Figure 14. Pulse Response versus Supply Voltage

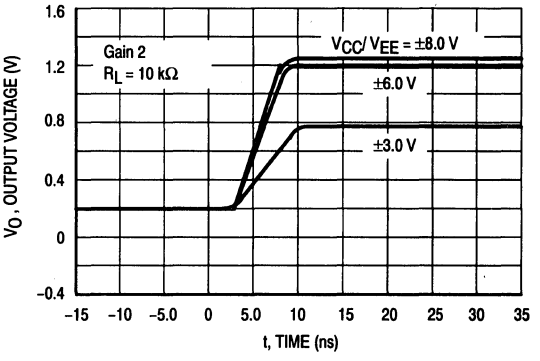


Figure 15. Pulse Response versus Temperature

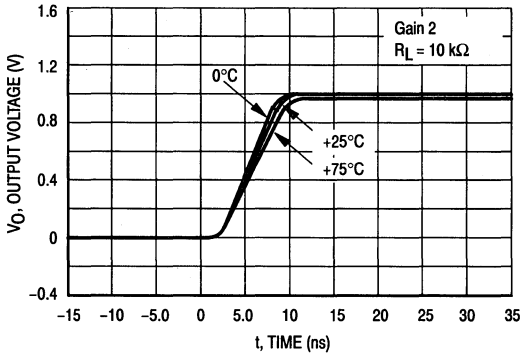


Figure 16. Differential Overdrive Recovery Time

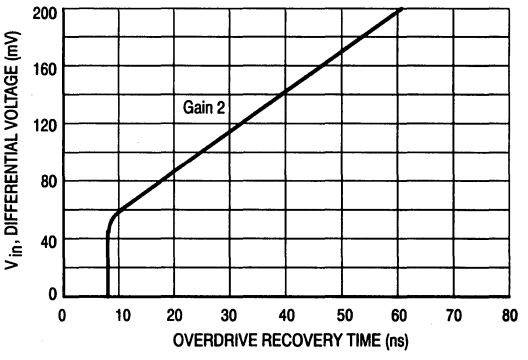


Figure 17. Phase Shift versus Frequency

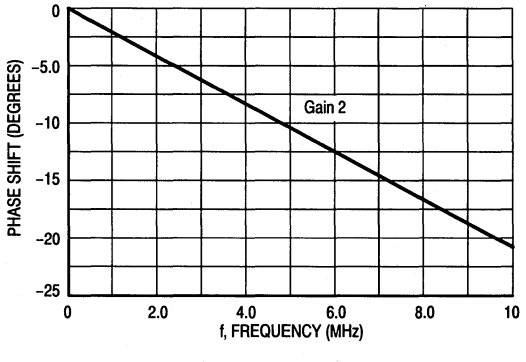


Figure 18. Phase Shift versus Frequency

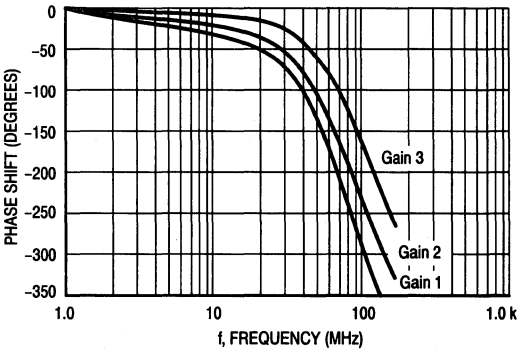


Figure 19. Input Resistance versus Temperature

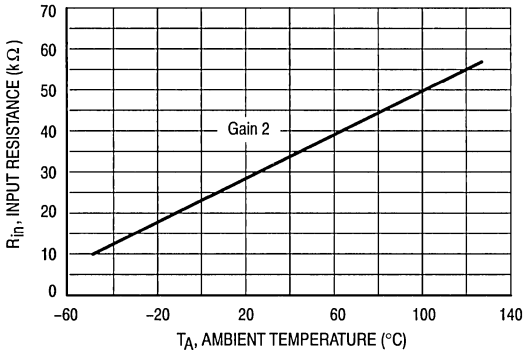


Figure 20. Input Noise Voltage

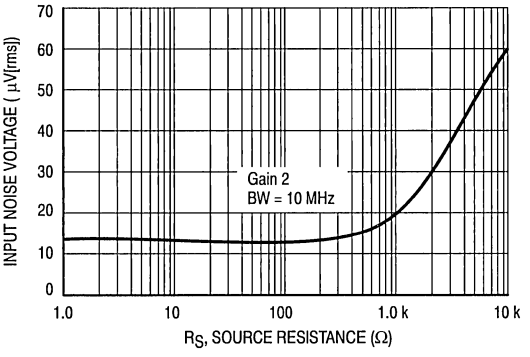


Figure 21. Output Voltage Swing and Sink Current versus Supply Voltage

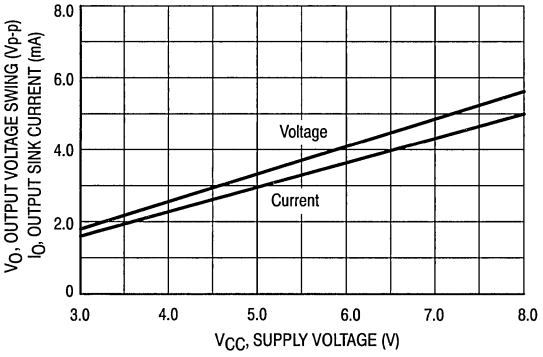


Figure 22. Output Voltage Swing versus Load Resistance

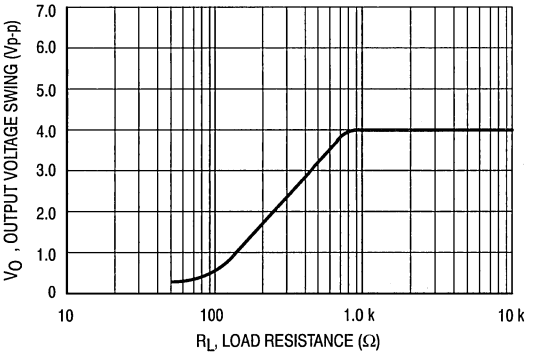


Figure 23. Output Voltage Swing versus Frequency

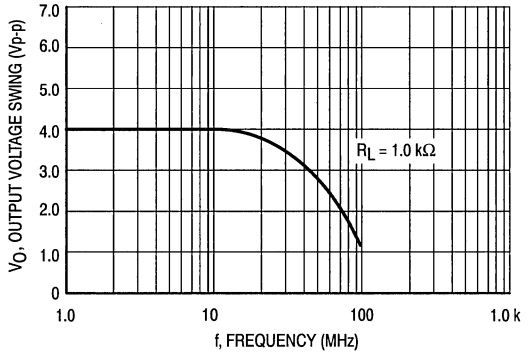


Figure 24. Common Mode Rejection Ratio

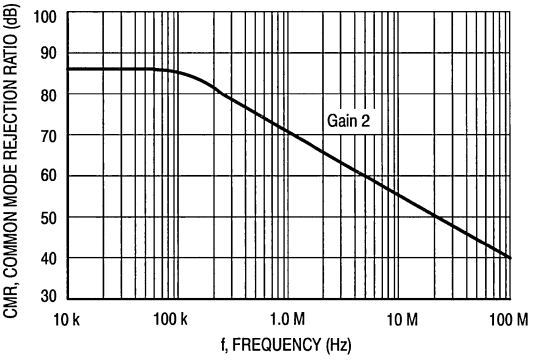
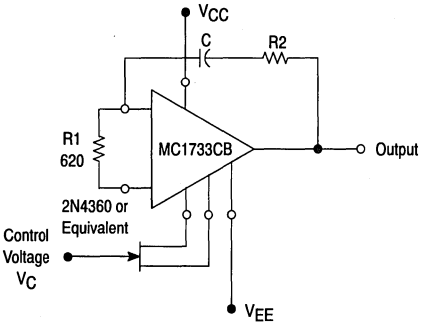
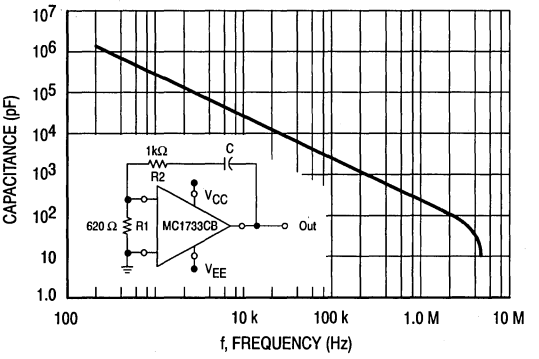


Figure 25. Voltage Controlled Oscillator



By changing the voltage V_C the gain will vary over a range of 10 V to 400 V. This will give a frequency variation about the value set by the capacitor and shown in Figure 26.

Figure 26. Oscillator Frequency for Various Capacitor Values



Tape, Drum or Disc Memory Read Amplifiers

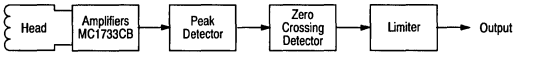
The first of several methods to be discussed is shown in Figure 27. This block diagram describes a simple Read circuit with no threshold circuitry. Each block represents a basic function that must be performed by the Read circuit. The first block, referred to as "amplification", increases the level of the signal available from the Read head to a level adequate to drive the Peak Detector. Obviously, these signal levels will vary depending on factors such as tape speed, whether the system used is disc or tape, and the type of head and the circuitry used. For a representative tape system, levels of 7.0 mV to 25 mV for the signal from the Read head and 2.0 V for the signal to the Peak Detector are typical. These signal levels are "peak-to-peak" unless otherwise specified. On the basis of the signal levels mentioned above, the overall amplification required is 38 dB to 49 dB.

How the overall gain requirement is implemented will depend somewhat on the system used. For instance, a tape cassette system with variable tape speed may utilize a first stage for gain and a second stage primarily for gain control. Thus, a typical circuit would utilize 35 dB in the first stage and 10 dB to 15 dB in the second stage.

Devices suitable for use as amplifiers fall into one of two categories, operational amplifiers or wideband video amplifiers. Lower speed equipment with low transfer rates commonly uses low cost operational amplifiers. Examples of these are the MC1741, MC1458, and MLM301. Equipment requiring higher transfer rates, such as disk systems normally use wideband amplifiers such as the MC1733CB. The actual crossover point where wideband amplifiers are used exclusively varies with equipment design. For purposes of comparison, the MLM301 has slightly less than a 40 dB open-loop gain at 100 kHz; the MC1741, a compensated op amp, has approximatley 20 dB open-loop gain at 100 kHz; the MC1733CB has approximately 33 dB of gain out to 100 MHz (depending on a gain option and loading).

There are a number of ways to implement the Peak Detector function. However, the simplest and most widely used method is a passive differentiator that generates "zero crossing" for each of the data peaks in the Read signal.

Figure 27. Typical Read Circuit (Method 1)

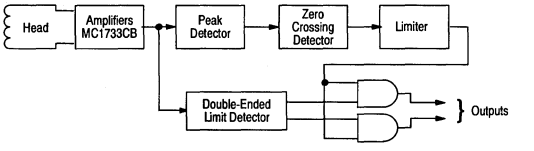


The actual circuitry used to differentiate the Read signal varies from a differential LC type in disc systems to a simple RC type in reel and cassette systems. Either type, of course, attenuates the signal by an amount depending on the circuit used and system specifications. A good approximation of attenuation using the RC type is 30 dB. Thus, the 2.0 V signal going into the differentiator is reduced to 200 mV.

The next block in Figure 27 to be discussed is the Zero Crossing Detector. In most cases detection of the zero crossings is combined with the limiter. These functions serve to generate a TTL compatible pulse waveform with "edges" corresponding to zero crossings. For low transfer rates, the circuit often used consists of an operational amplifier with series or shunt limiting. For higher transfer rates (greater than 100k B/S) comparators are used.

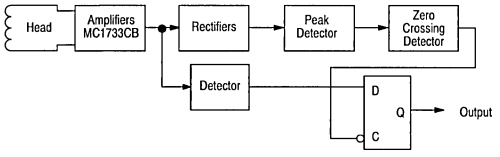
The method described above is often modified to include threshold sensing. In Figure 28, the function called Double Ended Limit Detector enables the output NAND gate when either the negative or positive data peaks of the Read signal exceed a predetermined threshold. This function can be implemented in either of two ways. One method first rectifies the signal before it is applied to a comparator with a set threshold. The other method utilizes two comparators, one comparator for positive-going peaks and the other for negative-going peaks. These comparator outputs are then combined in the output logic gates.

Figure 28. Read Circuit (Method 2)



Another common technique is shown in Figure 29. The branch labeled rectifiers, Peak Detector, etc., provides a clock transition of the D flip-flop that corresponds to the peak of both the positive and negative-going data peaks. This branch may include threshold circuitry prior to the Peak Detector. The detector in the lower path detects whether the signal peaks are positive or negative and feeds this data to the flip-flop. This detector can be implemented using a comparator with preset threshold.

Figure 29. Read Circuit (Method 3)

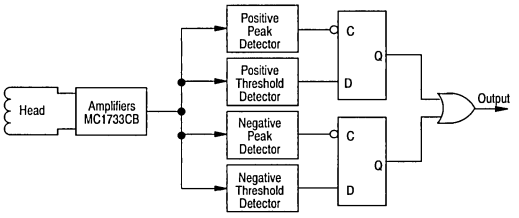


The technique shown in Figure 30 uses separate circuits with threshold provisions for both negative and positive peaks. The peak detectors and threshold detectors may be implemented with two comparators and two passive differentiators.

Each of the methods shown offer certain intrinsic advantages or disadvantages. The overall decision as to which method to use however often involves other important considerations. These could include cost and system requirements or circuitry other than simply the Read circuitry. For instance, if cost is the predominate overall factor, then Method 1 may be the only feasible alternative.

Method 4 was included as a design example because it illustrates several unique advantages. First, it uses threshold sensing to reduce noise peak errors. Second, it may be implemented using only integrated circuits. Third, it offers separate, direct threshold sensing for both positive and negative peaks.

Figure 30. Read Circuit (Method 4)



MC1741
MC1741C

OPERATIONAL AMPLIFIERS

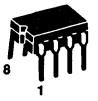
SILICON MONOLITHIC INTEGRATED CIRCUIT

Internally Compensated, High Performance Operational Amplifiers

The MC1741 and MC1741C were designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short Circuit Protection
- Offset Voltage Null Capability
- Wide Common Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch Up

P1 SUFFIX
PLASTIC PACKAGE
CASE 626



U SUFFIX
CERAMIC PACKAGE
CASE 693

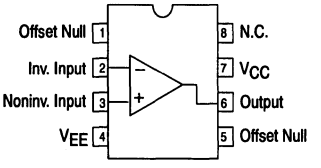
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	MC1741C	MC1741	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±18	±22	V_{dc}
Input Differential Voltage	V_{ID}	±30		V
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous		
Operating Ambient Temperature Range	T_A	0 to +70	–55 to +125	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 –65 to +150 –55 to +125		°C

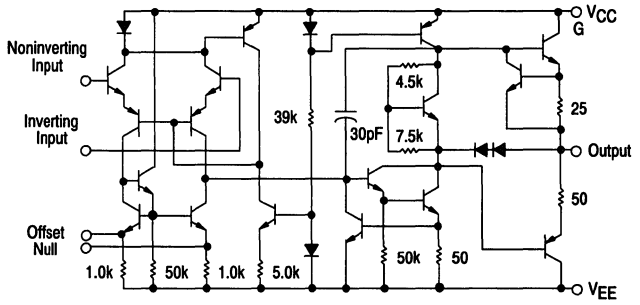
NOTES: 1. For supply voltages less than +15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Supply voltage equal to or less than 15 V.

PIN CONNECTIONS



(Top View)

Equivalent Circuit Schematic
(1/4 of Circuit Shown)



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1741CD	—	0° to +70°C	SO-8
MC1741CP1	LM741CN, µA741TC		Plastic DIP
MC1741CU	—		Ceramic DIP
MC1741U	—	–55° to +125°C	Ceramic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	MC1741			MC1741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le 10$ k)	V_{IO}	—	1.0	5.0	—	2.0	6.0	mV
Input Offset Current	I_{IO}	—	20	200	—	20	200	nA
Input Bias Current	I_{IB}	—	80	500	—	80	500	nA
Input Resistance	r_i	0.3	2.0	—	0.3	2.0	—	MΩ
Input Capacitance	C_i	—	1.4	—	—	1.4	—	pF
Offset Voltage Adjustment Range	V_{IOR}	—	±15	—	—	±15	—	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	—	±12	±13	—	V
Large Signal Voltage Gain (V_O = ±10 V, $R_L \ge 2.0$ k)	A_{VOL}	50	200	—	20	200	—	V/mV
Output Resistance	r_o	—	75	—	—	75	—	Ω
Common Mode Rejection ($R_S \le 10$ k)	CMR	70	90	—	70	90	—	dB
Supply Voltage Rejection ($R_S \le 10$ k)	PSR	75	—	—	75	—	—	dB
Output Voltage Swing	V_O							V
($R_L \ge 10$ k)		±12	±14	—	±12	±14	—	
($R_L \ge 2.0$ k)		±10	±13	—	±10	±13	—	
Output Short Circuit Current	I_{SC}	—	20	—	—	20	—	mA
Supply Current	I_D	—	1.7	2.8	—	1.7	2.8	mA
Power Consumption	P_C	—	50	85	—	50	85	mW
Transient Response (Unity Gain, Noninverting)								
(V_I = 20 mV, $R_L \ge 2.0$ k, $C_L \le 100$ pF) Rise Time	t_{TLH}	—	0.3	—	—	0.3	—	µs
(V_I = 20 mV, $R_L \ge 2.0$ k, $C_L \le 100$ pF) Overshoot	os	—	15	—	—	15	—	%
(V_I = 10 V, $R_L \ge 2.0$ k, $C_L \le 100$ pF) Slew Rate	SR	—	0.5	—	—	0.5	—	V/µs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high}, unless otherwise noted.)*

Characteristics	Symbol	MC1741			MC1741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le 10$ kΩ)	V_{IO}	—	1.0	6.0	—	—	7.5	mV
Input Offset Current	I_{IO}							nA
(T_A = +125°C)		—	7.0	200	—	—	—	
(T_A = −55°C)		—	85	500	—	—	—	
(T_A = 0° to +70°C)		—	—	—	—	—	300	
Input Bias Current	I_{IB}							nA
(T_A = +125°C)		—	30	500	—	—	—	
(T_A = −55°C)		—	300	1500	—	—	—	
(T_A = 0° to +70°C)		—	—	—	—	—	800	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	—	—	—	—	V
Common Mode Rejection ($R_S \le 10$ k)	CMR	70	90	—	—	—	—	dB
Supply Voltage Rejection ($R_S \le 10$ k)	PSR	75	—	—	75	—	—	dB
Output Voltage Swing	V_O							V
($R_L \ge 10$ k)		±12	±14	—	—	—	—	
($R_L \ge 2.0$ k)		±10	±13	—	±10	±13	—	
Large Signal Voltage Gain ($R_L \ge 2.0$ k, V_O = ±10 V)	A_{VOL}	25	—	—	15	—	—	V/mV
Supply Currents	I_D							mA
(T_A = +125°C)		—	1.5	2.5	—	—		
(T_A = −55°C)		—	2.0	3.3	—	—		
Power Consumption (T_A = +125°C)	P_C	—	45	75	—	—	—	mW
(T_A = −55°C)		—	60	100	—	—	—	

T_{high} = 125°C for MC1741, 70°C for MC1741C

* T_{low} = −55°C for MC1741, 0°C for MC1741C

2

Figure 1. Burst Noise versus Source Resistance

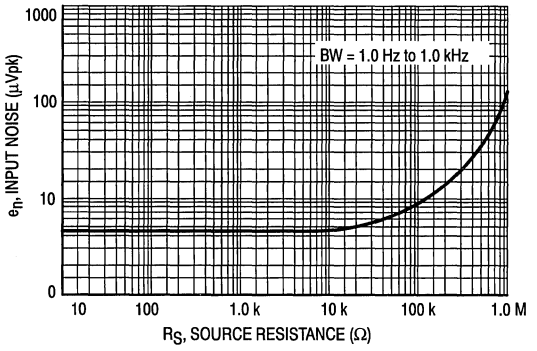


Figure 2. RMS Noise versus Source Resistance

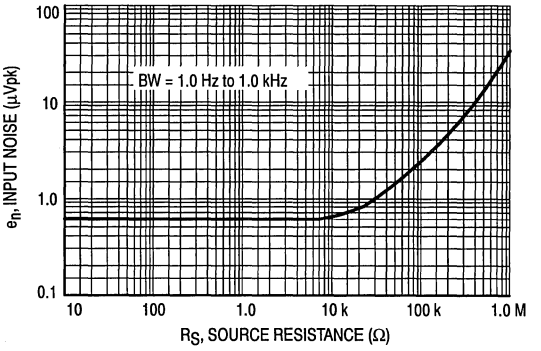


Figure 3. Output Noise versus Source Resistance

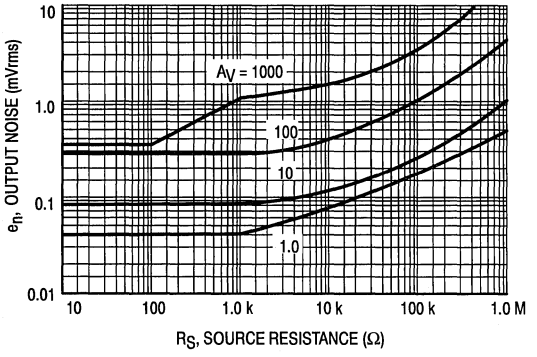


Figure 4. Spectral Noise Density

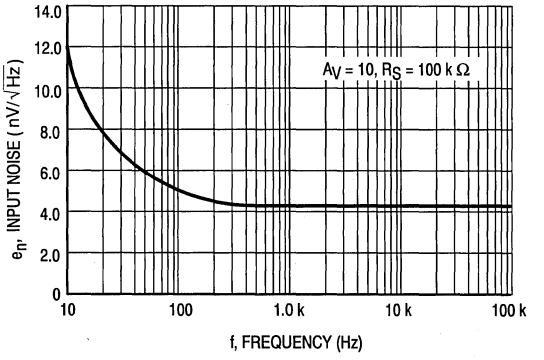
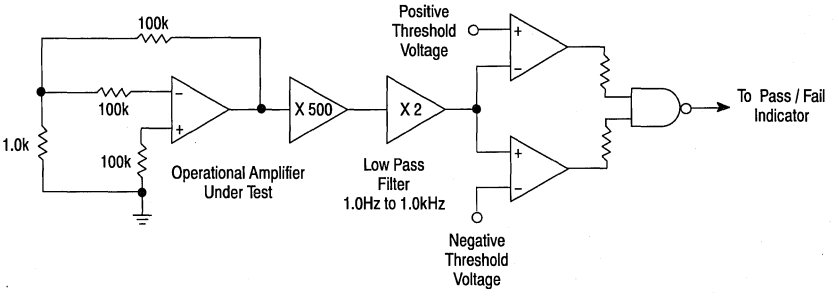


Figure 5. Burst Noise Test Circuit



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 sec and the 20 mV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier.

Figure 6. Power Bandwidth (Large Signal Swing versus Frequency)

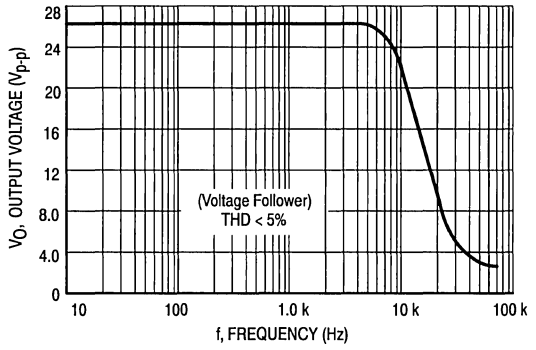


Figure 7. Open-Loop Freuqncy Response

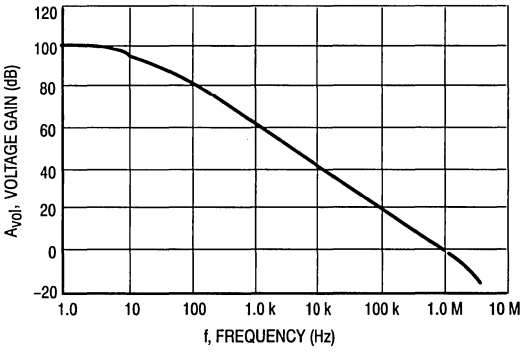


Figure 8. Positive Output Voltage Swing versus Load Resistance

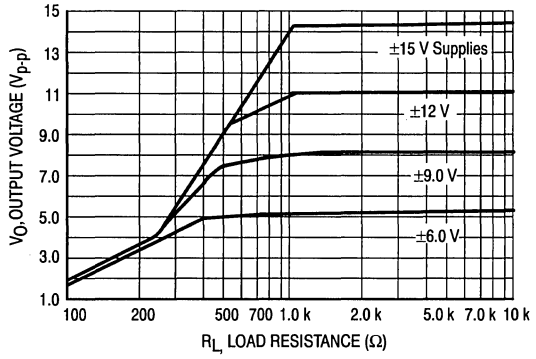


Figure 9. Negative Output Voltage Swing versus Load Resistance

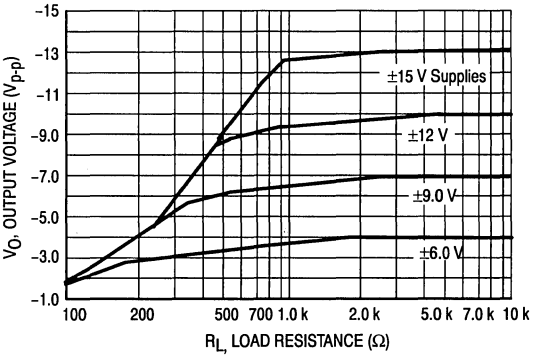


Figure 10. Output Voltage Swing versus Load Resistance (Single Supply Operation)

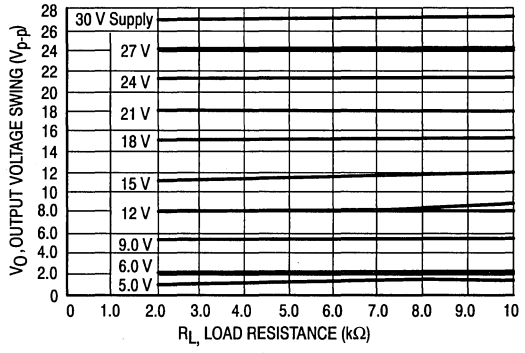


Figure 11. Single Supply Inverting Amplifier

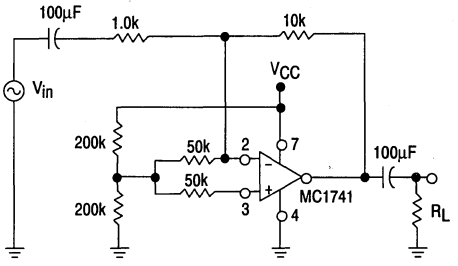


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Figure 12. Noninverting Pulse Response

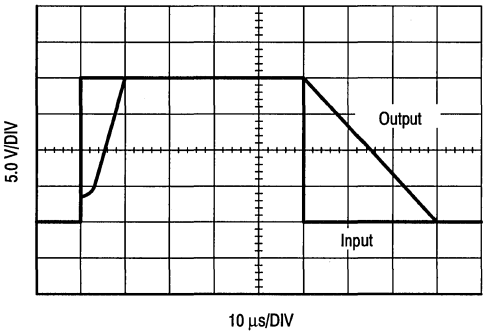


Figure 13. Transient Response Test Circuit

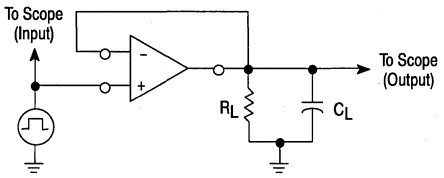
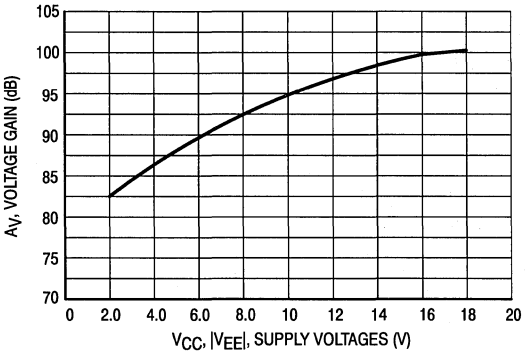


Figure 14. Open-Loop Voltage Gain versus Supply Voltage



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1747
MC1747C

(Dual MC1741)
Internally Compensated, High Performance Operational Amplifiers

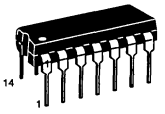
The MC1747 and MC1747C were designed for use as summing amplifiers, integrators, or amplifiers with operating characteristics as a function of the external feedback components. The MC1747L and MC1747CL are functionally and electrically equivalent to the μA747 and μA747C respectively.

- No Frequency Compensation Required
- Short Circuit Protection
- Wide Common Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Offset Voltage Null Capability

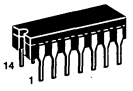
(DUAL MC1741)
DUAL
OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

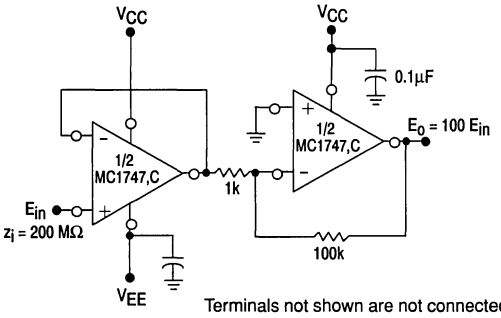


P2 SUFFIX
PLASTIC PACKAGE
CASE 646



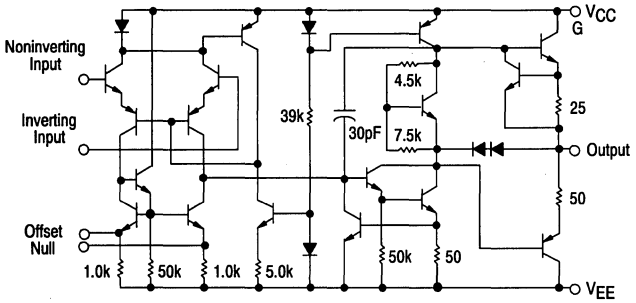
L SUFFIX
CERAMIC PACKAGE
CASE 632

Figure 1. High-Impedance, High-Gain Inverting Amplifier

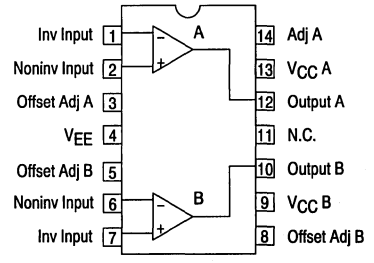


Terminals not shown are not connected

Figure 2. Circuit Schematic



PIN CONNECTIONS



VCCA and VCCB are not connected internally

ORDERING INFORMATION

Device	Temperature Range	Package
MC1747L	−55° to +125°C	Ceramic DIP
MC1747CD	0° to +70°C	SO-14
MC1747CL		Ceramic DIP
MC1747CP2		Plastic DIP

2

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

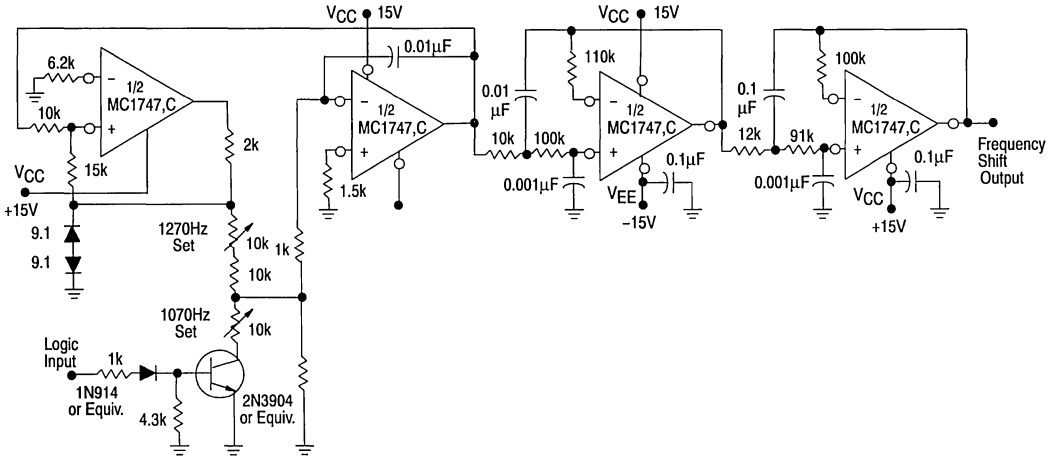
Rating	Symbol	MC1747	MC1747C	Unit
Power Supply Voltages	V_{CC} V_{EE}	+22 −22	+18 −18	Vdc
Differential Input Signal Voltages (Note 1)	V_{ID}	±30		V
Common Mode Input Swing Voltage (Note 2)	V_{ICR}	±15		V
Output Short Circuit Duration	t_{SC}	Continuous		
Voltage (Measurement between Offset Null and V_{EE})		±0.5		V
Operating Ambient Temperature Range	T_A	−55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	−65 to +150	°C
Junction Temperature Ceramic Package Plastic Package	T_J	175 150		°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	MC1747 Min	MC1747 Typ	MC1747 Max	MC1747C Min	MC1747C Typ	MC1747C Max	Unit
Input Bias Current T_A = +25°C T_A = T_{high} (Note 3) T_A = T_{low} (Note 3)	I_{IB}	 — — —	 80 30 300	 500 500 1500	 — — —	 80 30 30	 500 800 800	nAdc
Input Offset Current T_A = +25°C T_A = T_{high} T_A = T_{low}	I_{IO}	 — — —	 20 7.0 85	 200 200 500	 — — —	 20 7.0 7.0	 200 300 300	nAdc
Input Offset Current T_A = +25°C T_A = T_{low} to T_A = T_{high}	V_{IO}	 — —	 1.0 1.0	 5.0 6.0	 — —	 1.0 1.0	 6.0 7.5	mVdc
Offset Voltage Adjustment Range		—	±15	—	—	±15	—	mV
Differential Input Impedance (Open-loop, f = 20 Hz) Parallel Input Resistance Parallel Input Capacitance	 r_i C_i	 0.3 —	 2.0 1.4	 — —	 0.3 —	 2.0 1.4	 — —	 MΩ pF
Common Mode Input Voltage Swing T_{low} ≤ T_A ≤ T_{high}	V_{ICR}	 ±12	 ±13	 —	 ±12	 ±13	 —	V
Common Mode Rejection (R_S = 10 kΩ) T_{low} ≤ T_A ≤ T_{high}	CMR	 70	 90	 —	 70	 90	 —	dB
Open-Loop Voltage Gain T_A = +25°C T_A = T_{low} to T_A = T_{high} (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}	 50,000 25,000	 200,000 —	 — —	 25,000 15,000	 200,000 —	 — —	V
Transient Response (Unity Gain) (V_{in} = 20 mV, R_L = 2.0 kΩ, C_L ≤ 100 pF) Rise Time Overshoot Percentage	 t_{PLH}	 — —	 0.3 5.0	 — —	 — —	 0.3 5.0	 — —	 µs %
Slew Rate (Unity Gain)	SR	—	0.5	—	—	0.5	—	V/µs
Output Impedance	z_o	—	75	—	—	75	—	Ω
Short Circuit Output Current	I_{SC}	—	25	—	—	25	—	mAdc
Channel Separation		—	120	—	—	120	—	dB
Output Voltage Swing (T_{low} ≤ T_A ≤ T_{high}) R_L = 10 kΩ R_L = 2.0 kΩ	V_{OR}	 ±12 ±10	 ±14 ±13	 — —	 ±12 ±10	 ±14 ±13	 — —	Vpk
Power Supply Rejection (T_{low} to T_{high}) V_{EE} = Constant, R_S ≤ 10 kΩ V_{CC} = Constant, R_S ≤ 10 kΩ	 PSR+ PSR−	 75 75	 — —	 — —	 75 75	 — —	 — —	dB
Power Supply Current (each amplifier) T_A = +25°C T_A = T_{low} T_A = T_{high}	I_{CC},I_{EE}	 — — —	 1.7 2.0 1.5	 2.8 3.3 2.5	 — — —	 1.7 2.0 2.0	 2.8 3.3 3.3	mAdc
DC Power Consumption (each amplifier) T_A = +25°C T_A = T_{low} T_A = T_{high}	P_C	 — — —	 50 60 45	 85 100 75	 — — —	 50 60 60	 85 100 100	mW

NOTES: 1. For supply voltages of less than ±15 V, the maximum differential input voltage is equal to ±(V_{CC} +|V_{EE}|).
2. For supply voltages of less than ±15 V, the maximum input voltage is equal to the supply voltage (+V_{CC}, −|V_{EE}|).
3. T_{low} = 0°C for MC1747CL, −55°C for MC1747L; T_{high} = +70°C for MC1747CL, +125°C for MC1747L

Figure 3. Typical Frequency Shift Keyer Tone Generator Test Circuit



Terminals not shown are not connected.

Figure 4. Typical Frequency Shift Keyer Tone Generator

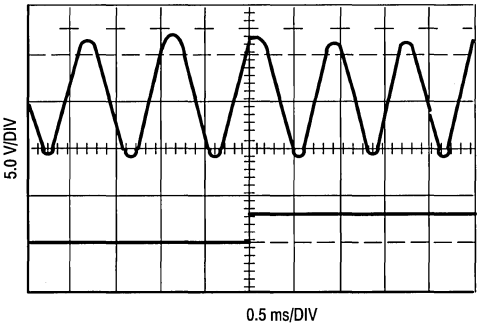


Figure 5. Open-Loop Voltage Gain versus Power-Supply Voltage

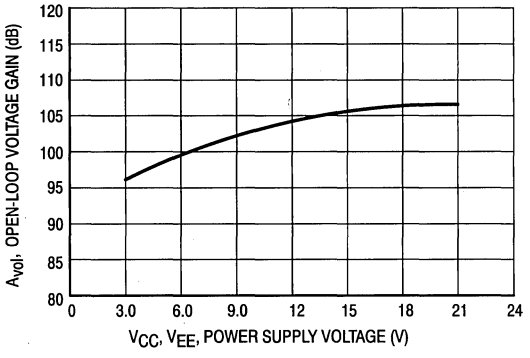


Figure 6. Open-Loop Frequency Response

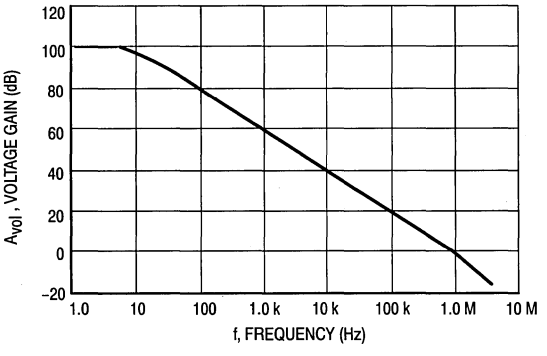


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Figure 7. Power Bandwidth (Large Signal Swing versus Frequency)

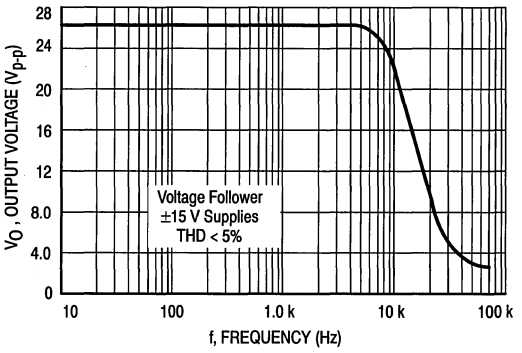


Figure 8. Power Consumption versus Power Supply Voltage

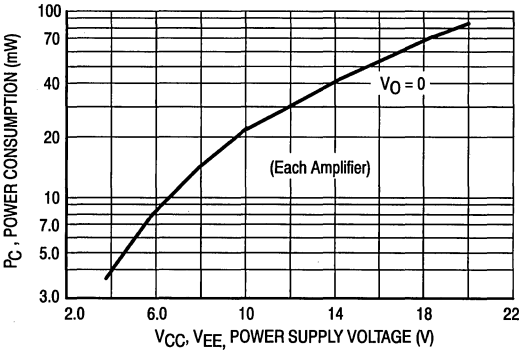


Figure 9. Output Voltage Swing versus Load Resistance

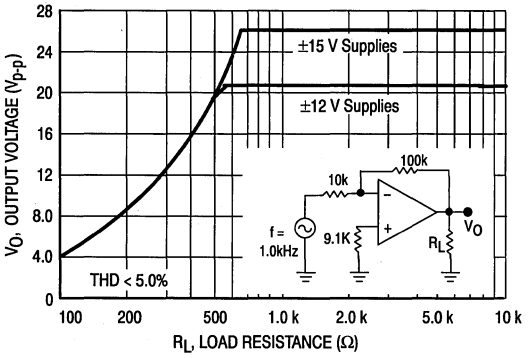
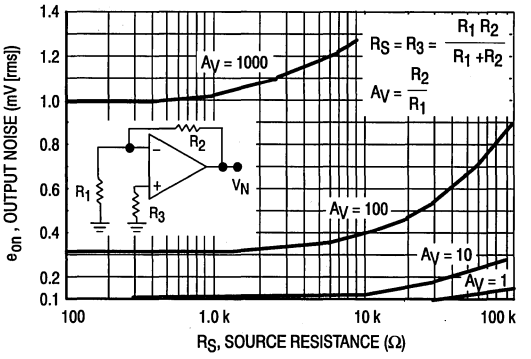


Figure 10. Output Noise versus Source Resistance



MC1748C

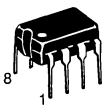
OPERATIONAL AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

High Performance Operational Amplifier

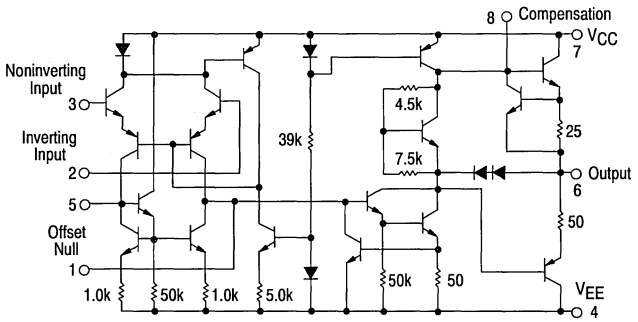
The MC1748 is designed for use as a summing amplifier, intergrator, or amplifier with operating characteristics as a function of the external feedback components.

- Noncompensated MC1741
- Single 30 pF Capacitor Compensation Requried For Unity Gain
- Short Circuit Protection
- Offset Voltage Null Capability
- Wide Common Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch Up

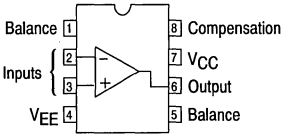


P1 SUFFIX
PLASTIC PACKAGE
CASE 626

Figure 1. Circuit Schematic



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC1748CP1	0° to +70°C	Plastic DIP

Typical Compensation Circuits

Figure 2. Offset Adjust and Frequency Compensation

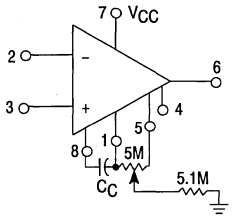


Figure 3. Single-Pole Compensation

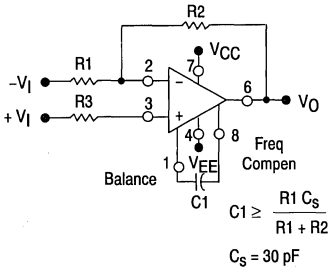
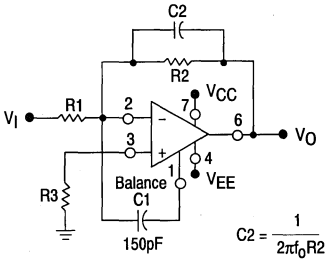


Figure 4. Feedforward Compensation



2

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 −18	Vdc
Differential Input Signal	V_{in}	±30	V
Common Mode Input Swing (Note 1)	V_{ICR}	±15	V
Output Short Circuit Duration	t_{SC}	Continuous	
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6	mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, V_{EE} = −15 V, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Bias Current T_A = +25°C T_A = T_{low} to T_{high} (Note 2)	I_{IB}	 — —	 0.08 —	 0.5 0.8	µAdc
Input Offset Current T_A = +25°C T_A = T_{low} to T_{high}	$\|I_{IO}\|$	 — —	 0.02 —	 0.2 0.3	µAdc
Input Offset Voltage ($R_S \leq 10$ k Ω) T_A = +25°C T_A = T_{low} to T_{high}	$\|V_{IO}\|$	 — —	 1.0 —	 6.0 7.5	mVdc
Differential Input Impedance (Open-Loop, f = 20 Hz) Parallel Input Resistance Parallel Input Capacitance	 R_P C_P	 0.3 —	 2.0 1.4	 — —	 MΩ pF
Common Mode Input Impedance (f 20 Hz)	z_{in}	—	200		MΩ
Common Mode Input Voltage Swing	V_{ICR}	±12	±13	—	V_{pk}
Common Mode Rejection (f = 100 Hz)	CMR	70	90	—	dB
Open-Loop Voltage Gain, (V_O = ±10 V, R_L = 2.0 kΩ) T_A = +25°C T_A = T_{low} to T_{high}	A_{vol}	 20,000 15,000	 200,000	 — —	V/V
Step Response (V_{in} = 20 mV, C_C = 30 pF, R_L = 2.0 kΩ, C_L = 100 pF) Rise Time Overshoot Slew Rate	 t_r dV_{out}/dt	 — — —	 0.3 5.0 0.8	 — — —	 µs % V/µs
Output Impedance (f = 20 Hz)	z_o	—	75	—	Ω
Short Circuit Output Current	I_{sc}	—	25	—	mAdc
Output Voltage Swing (R_L = 10 kΩ) R_L = 2 kΩ (T_A = T_{low} to T_{high})	V_O	±12 ±10	±14 ±13	— —	V_{pk}
Power Supply Sensitivity V_{EE} = constant, $R_S \leq 10$ kΩ V_{CC} = constant, $R_S \leq 10$ kΩ	 PSR+ PSR−	 75 75	 — —	 — —	dB
Power Supply Current	I_D + I_D −	— —	1.67 1.67	2.83 2.83	mAdc
DC Quiescent Power Dissipation (V_O = 0)	P_D	—	50	85	mW

NOTES: 1. For supply voltages of less than ±15 V, the Maximum Input Voltage Is equal to the Supply Voltage.
2. T_{low}: 0°C for MC1748C
T_{high}: +70°C for MC1748C

Figure 5. Minimum Input Voltage Range

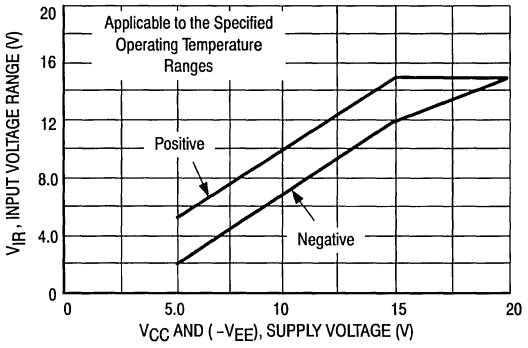


Figure 6. Minimum Output Voltage Swing

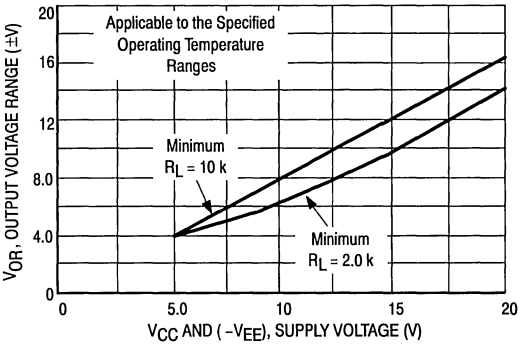


Figure 7. Minimum Voltage Gain

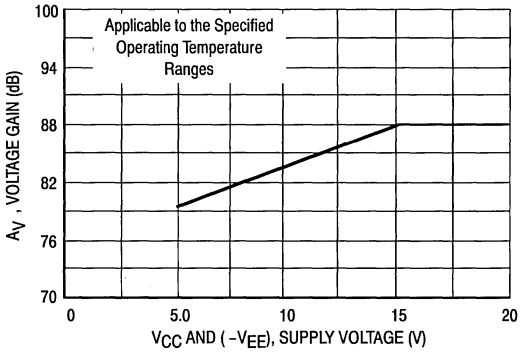


Figure 8. Typical Supply Currents

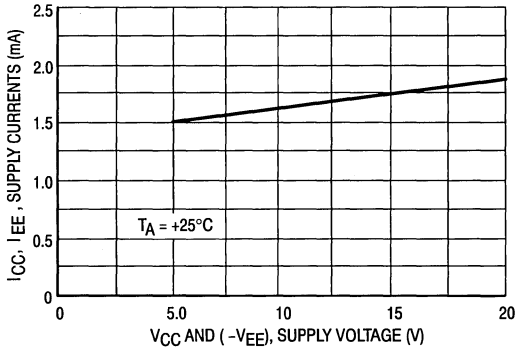


Figure 9. Open-Loop Frequency Response

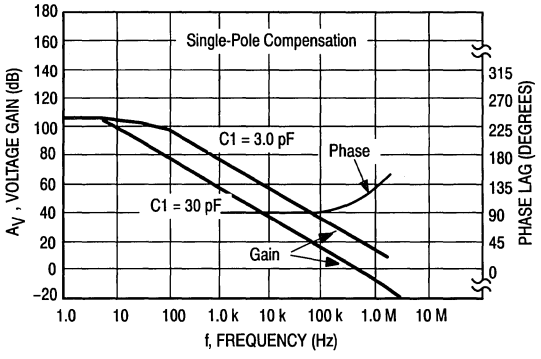
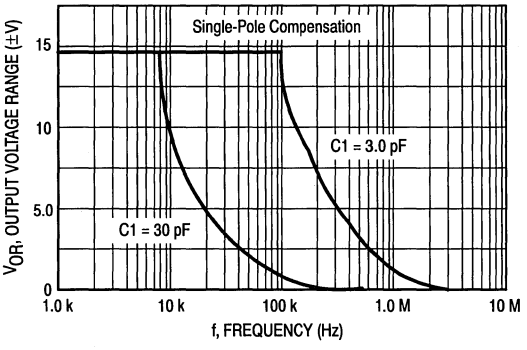


Figure 10. Large-Signal Frequency Response



2

Figure 11. Voltage Follower Pulse Response

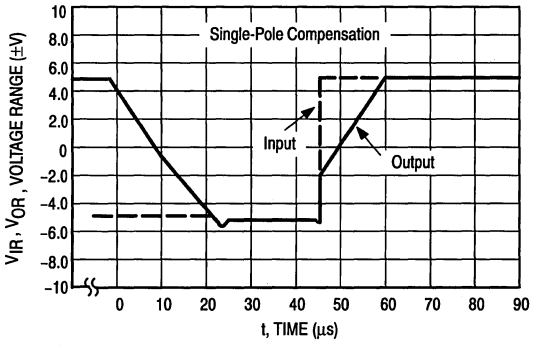


Figure 12. Open-Loop Frequency Response

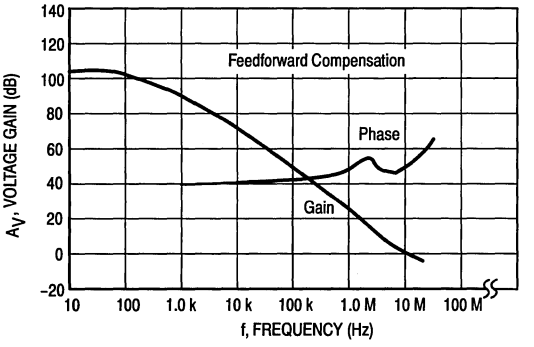


Figure 13. Large-Signal Frequency Response

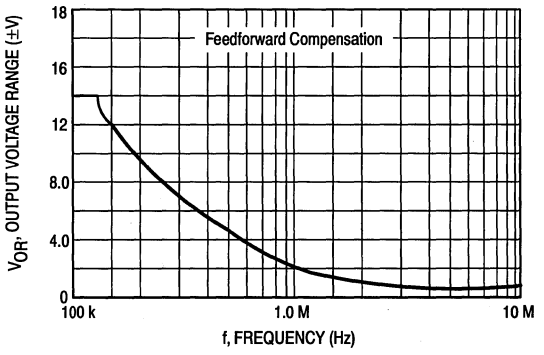
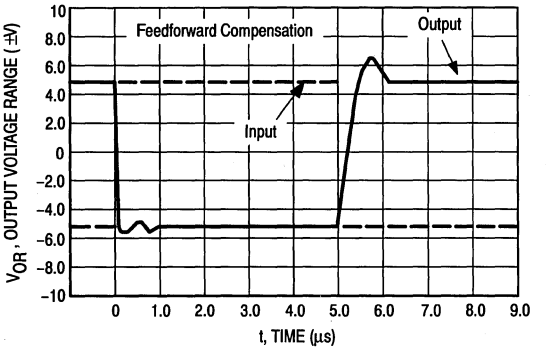


Figure 14. Inverter Pulse Response



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1776
MC1776C

PROGRAMMABLE OPERATIONAL AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

Micropower Programmable Operational Amplifier

This extremely versatile operational amplifier features low power consumption and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current and power consumption despite wide variations in operating power supply voltages.

- ±1.2 V to ±18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short Circuit Protection

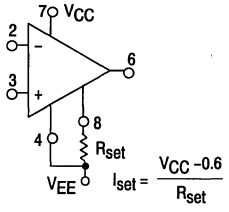
P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1776C Only)

U SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

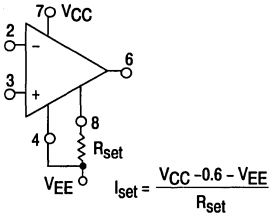
Resistive Programming
(See Figure 1)

R_{set} to Ground



Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 µA	I_{set} = 15 µA
±6.0 V	3.6 MΩ	360 kΩ
±10 V	6.2 MΩ	620 kΩ
±12 V	7.5 MΩ	750 kΩ
±15 V	10 MΩ	1.0 MΩ

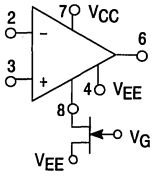
R_{set} to Negative Supply
(Recommended for supply voltage less than ±6.0 V)



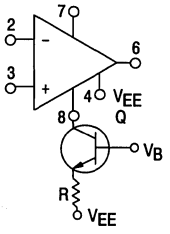
Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 µA	I_{set} = 15 µA
±1.5 V	1.6 MΩ	160 kΩ
±3.0 V	3.6 MΩ	360 kΩ
±6.0 V	7.5 MΩ	750 kΩ
±15 V	20 MΩ	2.0 MΩ

Active Programming

FET Current Source

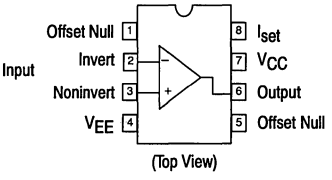


Bipolar Current Source



Pins not shown are not connected.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC1776U	–55° to +125°C	Ceramic DIP
MC1776CD	0° to +70°C	SO-8
MC1776CP1		Plastic DIP
MC1776CU		Ceramic DIP

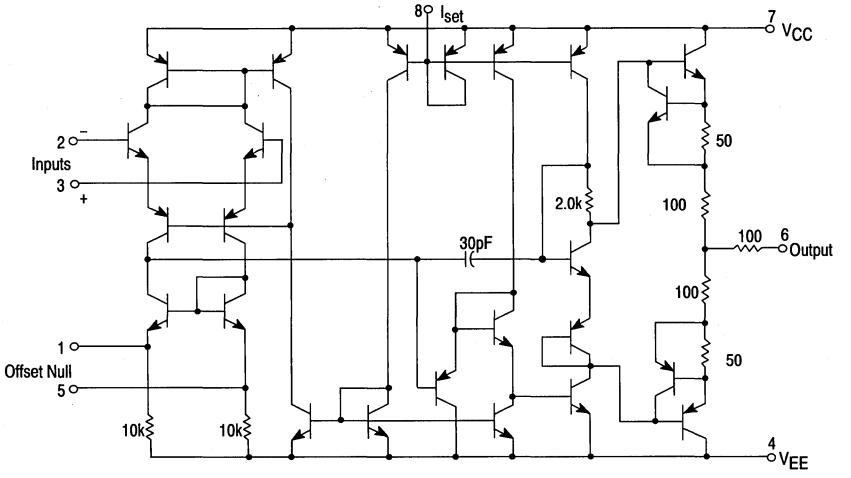
2

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

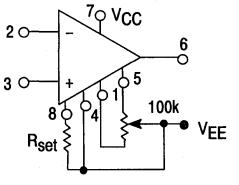
Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±18	Vdc
Differential Input Voltage	V_{ID}	±30	Vdc
Common Mode Input Voltage V_{CC} and $\|V_{EE}\|$ < 15 V V_{CC} and $\|V_{EE}\|$ ≥ 15 V	V_{ICM}	 V_{CC}, V_{EE} ±15	Vdc
Offset Null to V_{EE} Voltage	V_{off}–V_{EE}	±0.5	Vdc
Programming Current	I_{set}	500	μA
Programming Voltage (Voltage from I_{set} Terminal to Ground)	V_{set}	(V_{CC} –2.0 V) to V_{CC}	Vdc
Output Short Circuit Duration (Note 1)	t_{SC}	Indefinite	sec
Operating Temperature Range MC1776 MC1776C	T_A	 –55 to +125 0 to +70	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 –65 to +150 –55 to +125	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

NOTE 1. May be to ground or either Supply Voltage. Rating applies up to a case temperature of +125°C or ambient temperature of +70°C and $I_{set} \leq 30$ μA.

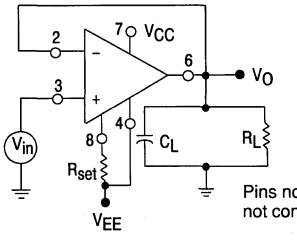
Equivalent Schematic Diagram



Voltage Offset Null Circuit



Transient Response Test Circuit



Pins not shown are not connected.

ELECTRICAL CHARACTERISTICS (V_{CC} = +3.0 V, V_{EE} = −3.0 V, I_{set} = 1.5 µA, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	MC1776 Min	MC1776 Typ	MC1776 Max	M1776C Min	M1776C Typ	M1776C Max	Unit
Input Offset Voltage ($R_S \le 10$ kΩ) T_A = +25°C $T_{low}^* \le T_A \le T_{high}^*$	V_{IO}	 — —	 2.0 —	 5.0 6.0	 — —	 2.0 —	 6.0 7.5	mV
Offset Voltage Adjustment Range	V_{IOR}	—	9.0	—	—	9.0	—	mV
Input Offset Current T_A = +25°C $T_A = T_{high}$ $T_A = T_{low}$	I_{IO}	 — — —	 0.7 — —	 3.0 5.0 10	 — — —	 0.7 — —	 6.0 6.0 10	nA
Input Bias Current T_A = +25°C $T_A = T_{high}$ $T_A = T_{low}$	I_{IB}	 — — —	 2.0 — —	 7.5 7.5 20	 — — —	 2.0 — —	 10 10 20	nA
Input Resistance	r_i	—	50	—	—	50	—	MΩ
Input Capacitance	c_i	—	2.0	—	—	2.0	—	pF
Input Voltage Range $T_{low} \le T_A \le T_{high}$	V_{ID}	 +1.0	 —	 —	 +1.0	 —	 —	V
Large Signal Voltage Gain $R_L \ge 75$ kΩ, $V_O = \pm 1.0$ V, T_A = +25°C $R_L \ge 75$ kΩ, $V_O = \pm 1.0$ V, $T_{low} \le T_A \le T_{high}$	A_{VOL}	 50 k 25 k	 200 k —	 — —	 25 k 25 k	 200 k —	 — —	V/V
Output Voltage Swing $R_L \ge 75$ kΩ, $T_{low} \le T_A \le T_{high}$	V_O	 ±2.0	 ±2.4	 —	 ±2.0	 ±2.4	 —	V
Output Resistance	r_o	—	5.0	—	—	5.0	—	kΩ
Output Short Circuit Current	I_{SC}	—	3.0	—	—	3.0	—	mA
Common Mode Rejection $R_S \le 10$ kΩ, $T_{low} \le T_A \le T_{high}$	CMR	 70	 86	 —	 70	 86	 —	dB
Supply Voltage Rejection Ratio $R_S \le 10$ kΩ, $T_{low} \le T_A \le T_{high}$	PSRR	 —	 25	 150	 —	 25	 200	µV/V
Supply Current T_A = +25°C $T_{low} \le T_A \le T_{high}$	I_{CC}, I_{EE}	 — —	 13 —	 20 25	 — —	 13 —	 20 25	µA
Power Dissipation T_A = +25°C $T_{low} \le T_A \le T_{high}$	P_D	 — —	 78 —	 120 150	 — —	 78 —	 120 150	µW
Transient Response (Unity Gain) V_{in} = 20 mV, $R_L \ge 5.0$ kΩ, C_L = 100 pF Rise Time Overshoot	 t_{TLH} OS	 — —	 3.0 0	 — —	 — —	 3.0 0	 — —	 µs %
Slew Rate ($R_L \ge 5.0$ kΩ)	S_R	—	0.03	—	—	0.03	—	V/µs

*T_{low} = −55°C for MC1776, 0°C for MC1776C T_{high} = +125°C for MC1776, +70°C for MC1776C

ELECTRICAL CHARACTERISTICS—continued (V_{CC} = +3.0 V, V_{EE} = −3.0 V, I_{set} = 15 μA, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	MC1776			MC1776C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le 10$ kΩ) T_A = +25°C $T_{low}^* \le T_A \le T_{high}^*$	V_{IO}	 — —	 2.0 —	 5.0 6.0	 — —	 2.0 —	 6.0 7.5	mV
Offset Voltage Adjustment Range	V_{IOR}	—	18	—	—	18	—	mV
Input Offset Current T_A = +25°C $T_A = T_{high}$ $T_A = T_{low}$	I_{IO}	 — — —	 2.0 — —	 15 15 40	 — — —	 2.0 — —	 25 25 40	nA
Input Bias Current T_A = +25°C $T_A = T_{high}$ $T_A = T_{low}$	I_{IB}	 — — —	 15 — —	 50 50 120	 — — —	 15 — —	 50 50 100	nA
Input Resistance	r_i	—	5.0	—	—	5.0	—	MΩ
Input Capacitance	c_i	—	2.0	—	—	2.0	—	pF
Input Voltage Range $T_{low} \le T_A \le T_{high}$	V_{ID}	 ±1.0	 —	 —	 ±1.0	 —	 —	V
Large Signal Voltage Gain $R_L \ge 5.0$ kΩ, V_O = ±1.0 V, T_A = +25°C $R_L \ge 5.0$ kΩ, V_O = ±1.0 V, $T_{low} \le T_A \le T_{high}$	A_{VOL}	 50 k 25 k	 200 k —	 — —	 25 k 25 k	 200 k —	 — —	V/V
Output Voltage Swing $R_L \ge 5.0$ kΩ, $T_{low} \le T_A \le T_{high}$	V_O	 ±1.9	 ±2.1	 —	 ±2.0	 ±2.1	 —	V
Output Resistance	r_o	—	1.0	—	—	1.0	—	kΩ
Output Short Circuit Current	I_{SC}	—	5.0	—	—	5.0	—	mA
Common Mode Rejection $R_S \le 10$ kΩ, $T_{low} \le T_A \le T_{high}$	CMR	 70	 86	 —	 70	 86	 —	dB
Supply Voltage Rejection Ratio $R_S \le 10$ kΩ, $T_{low} \le T_A \le T_{high}$	PSRR	 —	 25	 150	 —	 25	 200	μV/V
Supply Current T_A = +25°C $T_{low} \le T_A \le T_{high}$	I_{CC}, I_{EE}	 — —	 130 —	 160 180	 — —	 130 —	 170 180	μA
Power Dissipation T_A = +25°C $T_{low} \le T_A \le T_{high}$	P_D	 — —	 780 —	 960 1080	 — —	 780 —	 1020 1080	μW
Transient Response (Unity Gain) V_{in} = 20 mV, $R_L \ge 5.0$ kΩ, C_L = 100 pF Rise Time Overshoot	 t_{TLH} OS	 — —	 0.6 5.0	 — —	 — —	 0.6 5.0	 — —	 μs %
Slew Rate ($R_L \ge 5.0$ kΩ)	S_R	—	0.35	—	—	0.35	—	V/μs

ELECTRICAL CHARACTERISTICS—continued (V_{CC} = +15 V, V_{EE} = −15 V, I_{set} = 1.5 µA, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	MC1776			MC1776C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le 10$ kΩ)	V_{IO}							mV
T_A = +25°C		—	2.0	5.0	—	2.0	6.0	
$T_{low}^* \le T_A \le T_{high}^*$		—	—	6.0	—	—	7.5	
Offset Voltage Adjustment Range	V_{IOR}	—	9.0	—	—	9.0	—	mV
Input Offset Current	I_{IO}							nA
T_A = +25°C		—	0.7	3.0	—	0.7	6.0	
$T_A = T_{high}$		—	—	5.0	—	—	6.0	
$T_A = T_{low}$		—	—	10	—	—	10	
Input Bias Current	I_{IB}							nA
T_A = +25°C		—	2.0	7.5	—	2.0	10	
$T_A = T_{high}$		—	—	7.5	—	—	10	
$T_A = T_{low}$		—	—	20	—	—	20	
Input Resistance	r_i	—	50	—	—	50	—	MΩ
Input Capacitance	c_i	—	2.0	—	—	2.0	—	pF
Input Voltage Range	V_{ID}							V
$T_{low} \le T_A \le T_{high}$		±10	—	—	±10	—	—	
Large Signal Voltage Gain	A_{VOL}							V/V
$R_L \ge 75$ kΩ, V_O = ±10 V, T_A = +25°C		200 k	400 k	—	50 k	400 k	—	
$R_L \ge 75$ kΩ, V_O = ±10 V, $T_{low} \le T_A \le T_{high}$		100 k	—	—	50 k	—	—	
Output Voltage Swing	V_O							V
$R_L \ge 75$ kΩ, T_A = +25°C		±12	±14	—	±12	±14	—	
$R_L \ge 75$ kΩ, $T_{low} \le T_A \le T_{high}$		±10	—		±10	—		
Output Resistance	r_o	—	5.0	—	—	5.0	—	kΩ
Output Short Circuit Current	I_{SC}	—	3.0	—	—	3.0	—	mA
Common Mode Rejection	CMR							dB
$R_S \le 10$ kΩ, $T_{low} \le T_A \le T_{high}$		70	90	—	70	90	—	
Supply Voltage Rejection Ratio	PSRR							µV/V
$R_S \le 10$ kΩ, $T_{low} \le T_A \le T_{high}$		—	25	150	—	25	200	
Supply Current	I_{CC},I_{EE}							µA
T_A = +25°C		—	20	25	—	20	30	
$T_{low} \le T_A \le T_{high}$		—	—	30	—	—	35	
Power Dissipation	P_D							mW
T_A = +25°C		—	—	0.75	—	780	0.9	
$T_{low} \le T_A \le T_{high}$		—	—	0.9	—	—	1.05	
Transient Response (Unity Gain)								
V_{in} = 20 mV, $R_L \ge 5.0$ kΩ, C_L = 100 pF								
Rise Time	t_{TLH}	—	1.6	—	—	1.6	—	µs
Overshoot	OS	—	0	—	—	0	—	%
Slew Rate ($R_L \ge 5.0$ kΩ)	S_R	—	0.1	—	—	0.1	—	V/µs

*T_{low} = −55°C for MC1776
0°C for MC1776C

T_{high} = +125°C for MC1776
+70°C for MC1776C

2

ELECTRICAL CHARACTERISTICS—continued (V_{CC} = +15 V, V_{EE} = –15 V, I_{set} = 15 µA, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	MC1776			MC1776C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le 10$ kΩ) T_A = +25°C $T_{low}^* \le T_A \le T_{high}^*$	V_{IO}	 — —	 2.0 —	 5.0 6.0	 — —	 2.0 —	 6.0 7.5	mV
Offset Voltage Adjustment Range	V_{IOR}	—	18	—	—	18	—	mV
Input Offset Current T_A = +25°C $T_A = T_{high}$ $T_A = T_{low}$	I_{IO}	 — — —	 2.0 — —	 15 15 40	 — — —	 2.0 — —	 25 25 40	nA
Input Bias Current T_A = +25°C $T_A = T_{high}$ $T_A = T_{low}$	I_{IB}	 — — —	 15 — —	 50 50 120	 — — —	 15 — —	 50 50 100	nA
Input Resistance	r_i	—	5.0	—	—	5.0	—	MΩ
Input Capacitance	c_i	—	2.0	—	—	2.0	—	pF
Input Voltage Range $T_{low} \le T_A \le T_{high}$	V_{ID}	 ±10	 —	 —	 ±10	 —	 —	V
Large Signal Voltage Gain $R_L \ge 5.0$ kΩ, V_O = ±10 V, T_A = +25°C $R_L \ge 75$ kΩ, V_O = ±10 V, $T_{low} \le T_A \le T_{high}$	A_{VOL}	 100 k 75 k	 400 k —	 — —	 50 k 50 k	 400 k —	 — —	V/V
Output Voltage Swing $R_L \ge 5.0$ kΩ, T_A = +25°C $R_L \ge 75$ kΩ, $T_{low} \le T_A \le T_{high}$	V_O	 ±10 ±10	 ±13 —	 —	 ±10 ±10	 ±13 —	 —	V
Output Resistance	r_o	—	1.0	—	—	1.0	—	kΩ
Output Short Circuit Current	I_{SC}	—	12	—	—	12	—	mA
Common Mode Rejection $R_S \le 10$ kΩ, $T_{low} \le T_A \le T_{high}$	CMR	 70	 90	 —	 70	 90	 —	dB
Supply Voltage Rejection Ratio $R_S \le 10$ kΩ, $T_{low} \le T_A \le T_{high}$	PSRR	 —	 25	 150	 —	 25	 200	µV/V
Supply Current T_A = +25°C $T_{low} \le T_A \le T_{high}$	I_{CC}, I_{EE}	 — —	 160 —	 180 200	 — —	 160 —	 190 200	µA
Power Dissipation T_A = +25°C $T_{low} \le T_A \le T_{high}$	P_D	 — —	 — —	 5.4 6.0	 — —	 — —	 5.7 6.0	µW
Transient Response (Unity Gain) V_{in} = 20 mV, $R_L \ge 5.0$ kΩ, C_L = 100 pF Rise Time Overshoot	 t_{TLH} OS	 — —	 0.35 10	 — —	 — —	 0.35 10	 — —	 µs %
Slew Rate ($R_L \ge 5.0$ kΩ)	S_R	—	0.8	—	—	0.8	—	V/µs

Figure 1. Set Current versus Set Resistor

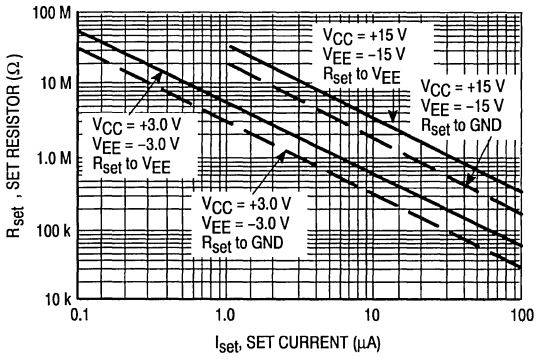


Figure 2. Positive Standby Supply Current versus Set Current

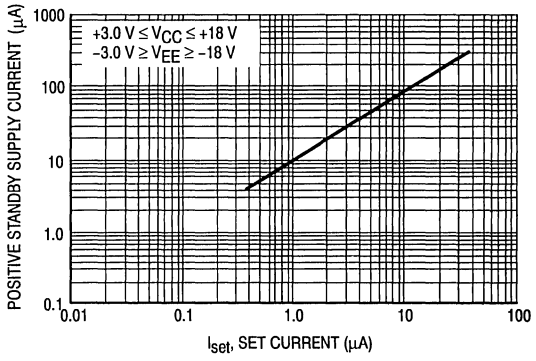


Figure 3. Open-Loop Gain versus Set Current

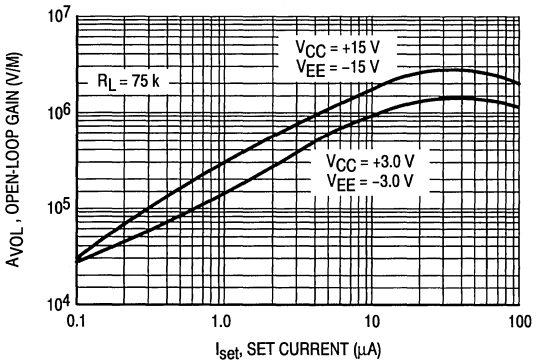


Figure 4. Input Bias Current versus Set Current

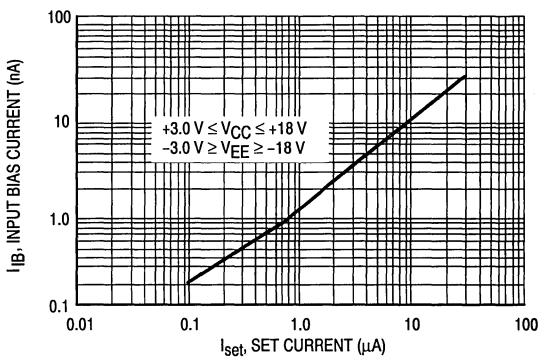


Figure 5. Input Bias Current versus Ambient Temperature

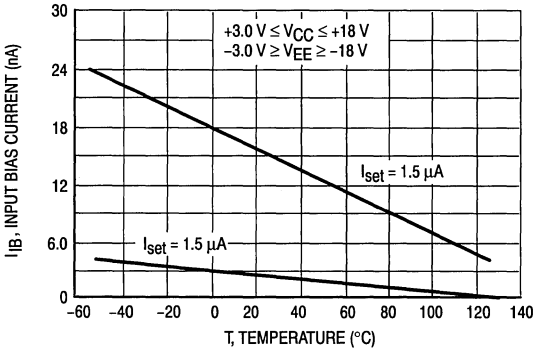
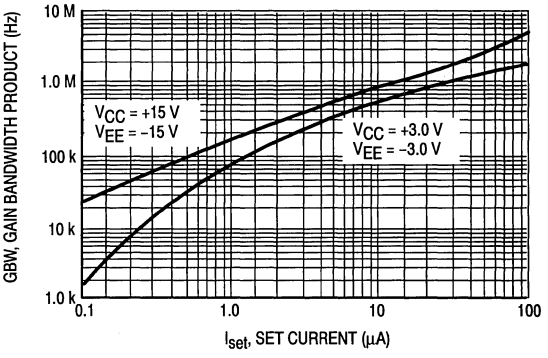


Figure 6. Gain Bandwidth Product versus Set Current



2

Figure 7. Output Voltage Swing versus Load Resistance

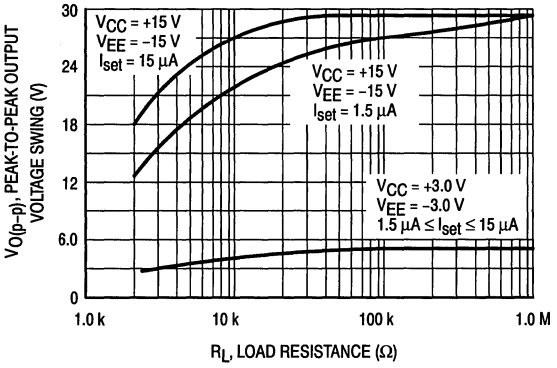


Figure 8. Supply Current versus Ambient Temperature

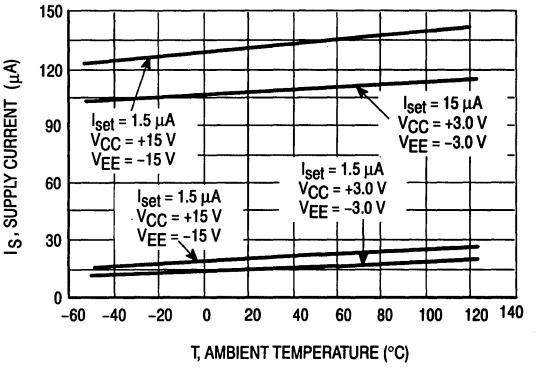


Figure 9. Output Voltage Swing versus Supply Voltage

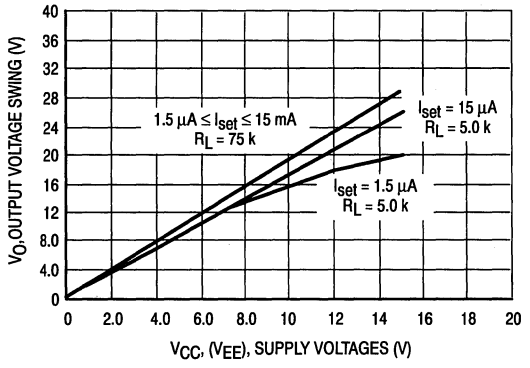


Figure 10. Slew Rate versus Set Current

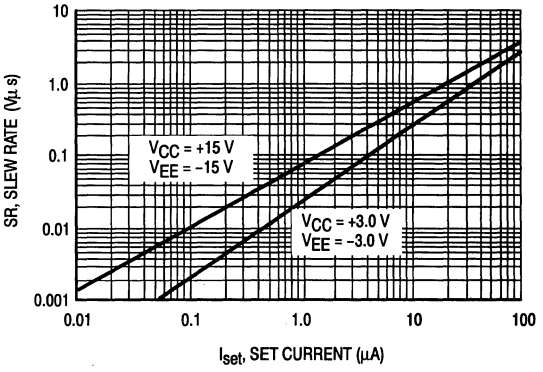


Figure 11. Input Noise Voltage versus Set Current

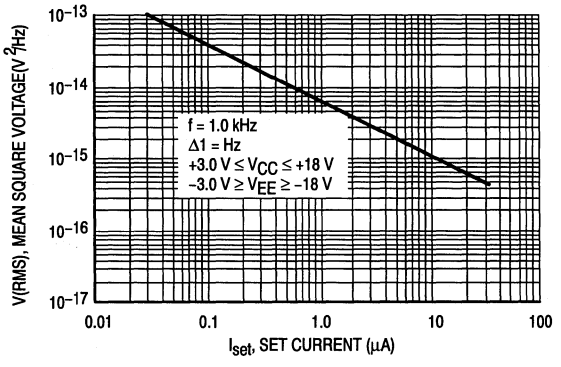


Figure 12. Optimum Source Resistance for Minimum Noise versus Set Current

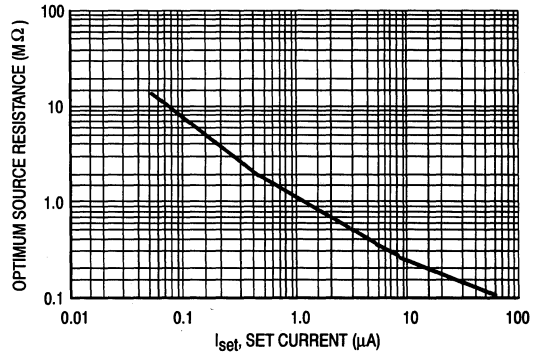
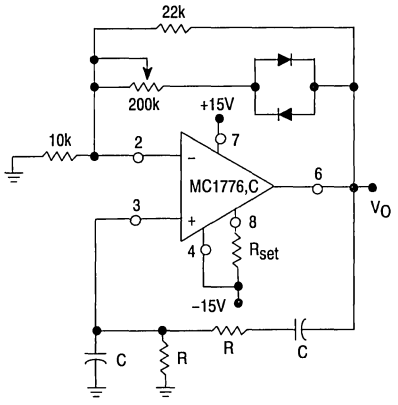


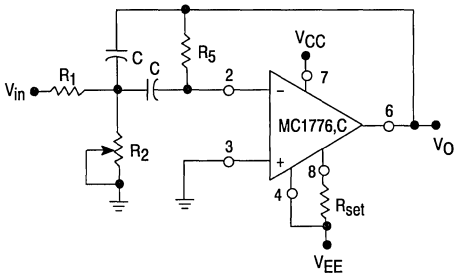
Figure 13. Wien Bridge Oscillator



$$f_o = \frac{1}{2\pi RC} \quad \text{(for } f_o = 1.0 \text{ kHz)}$$

R= 16 kΩ
C = 0.01 μF

Figure 14. Multiple Feedback Bandpass Filter



For a given:
fo = center frequency
A (fo) = Gain at center frequency
Q = quality factor

Choose a value for C, then

$$R_5 = \frac{Q}{\pi f_o C}$$

$$R_1 = \frac{R5}{2A\,(f_o)}$$

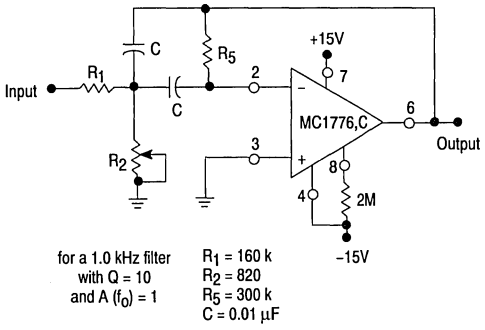
$$R_2 = \frac{R1,R5}{4Q^2\ R1\text{-}R5}$$

To obtain less than 10% error from the operational amplifier:

$$\frac{Q_O\, f_o}{GBW} \leq 0.1$$

where f_o and GBW are expressed in Hz. GBW is available from Figure 6 as a function of Set Current, I_{set}.

Figure 15. Multiple Feedback Bandpass Filter (1.0 kHz)



for a 1.0 kHz filter with Q = 10 and A (f_o) = 1

R_1 = 160 k
R_2 = 820
R_5 = 300 k
C = 0.01 μF

Figure 16. Gated Amplifier

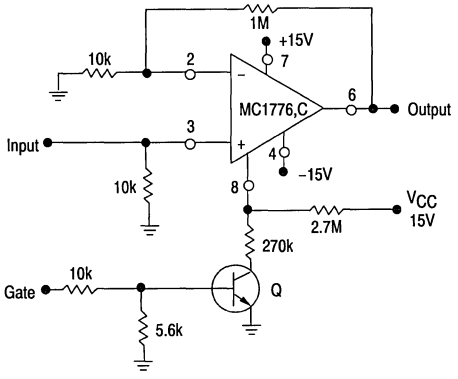
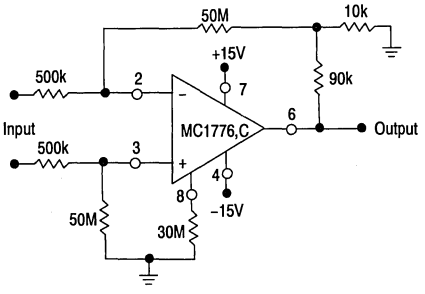


Figure 17. High Input Impedance Amplifier



MC3301 LM2900
MC3401 LM3900

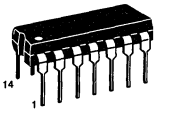
QUAD
OPERATIONAL AMPLIFIERS

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

Quad Single Supply Operational Amplifiers

These internally compensated Norton operational amplifiers are designed specifically for single positive power supply applications found in industrial control systems and automotive electronics. Each device contains four independent amplifiers — making it ideal for applications such as active filters, multi-channel amplifiers, tachometers, oscillators and other similar usage.

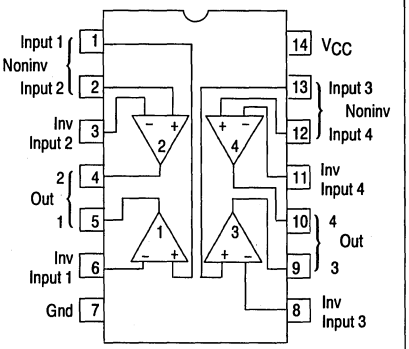
- Single Supply Operation
- Internally Compensated
- Wide Unity Gain Bandwidth: 4.0 MHz Typical
- Low Input Bias Current: 50 nA Typical
- High Open-Loop Gain: 1000 V/V Minimum
- Large Output Voltage Swing: (V_{CC} — 1) V_{p-p}



N, P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	LM2900/ LM3900	MC3301	MC3401	Unit
Supply Voltage	V_{CC}	+32	+28	+18	V
Input Current (I_{in} + or I_{in} −)	I_{in}	5.0			mA
Output Current	I_O	50			mA
Power Dissipation (T_A = +25°C) Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	625 5.0			mW mW/°C
Ambient Temperature Range LM2900 LM3900	T_A	 −40 to +85 0 to +70	 −40 to +85 	 0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150			°C

ORDERING INFORMATION

Device	Temperature Range	Package
LM3900D MC3401D	0° to +70°C	SO-14
LM3900N MC3401P	0° to +70°C	Plastic DIP
LM2900N MC3301P	−40° to +85°C	Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, R_L = 5.0 kΩ. T_A = +25°C [each amplifier], unless otherwise noted.)

Characteristics	Symbol	LM2900			LM3900			MC3301			MC3401			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Open-Loop Voltage Gain f = 100 Hz, R_L = 5.0 k $T_A = T_{low}$ to T_{high} (Notes 1, 2)	A_{VOL}	1.2 —	2.0 —	— —	1.2 —	2.0 —	— —	1.2 —	2.0 —	— —	1.2 0.8	2.0 —	— —	V/mV
Input Resistance (Inverting Input)	r_i	—	1.0	—	—	1.0	—	—	1.0	—	0.1	1.0	—	MΩ
Output Resistance	r_o	—	8.0	—	—	8.0	—	—	8.0	—	—	8.0	—	kΩ
Input Bias Current (Inverting Input) $T_A = T_{low}$ to T_{high} (Note 1)	I_{IB}	— —	50 —	200 —	— —	50 —	200 —	— —	50 —	300 —	— —	50 —	300 500	nA
Slew Rate (C_L = 100 pF, R_L = 2.0 k) Positive Output Swing Negative Output Swing	SR	— —	0.5 20	— —	— —	0.5 20	— —	— —	0.5 20	— —	— —	0.5 20	— —	V/μs
Unity Gain Bandwidth	BW	—	4.0	—	—	4.0	—	—	4.0	—	—	4.0	—	MHz
Output Voltage Swing (Note 7) V_{CC} = +15 V, R_L = 2.0 k V_{out} High (I_{in}^- = 0, I_{in}^+ = 0) V_{out} Low (I_{in}^- = 10 μA, I_{in}^+ = 0) V_{CC} = Maximum Rating, R_L = ∞ V_{out} High (I_{in}^- = 0, I_{in}^+ = 0)	 V_{OH} V_{OL} V_{OH}	 13.5 — —	 14.2 0.03 29.5	 — 0.2 —	 13.5 — —	 14.2 0.03 29.5	 — 0.2 —	 13.5 — —	 14.2 0.03 25.5	 — 0.2 —	 13.5 — —	 14.2 0.03 15.5	 — 0.2 —	V
Output Current Source Sink (Note 3) Low Level Output Current I_{in}^- = 5.0 μA, V_{OL} = 1.0 V	 I_{Source} I_{Sink} I_{OL}	 6.0 0.5 —	 10 0.87 5.0	 — — —	 6.0 0.5 —	 10 0.87 5.0	 — — —	 5.0 0.5 —	 10 0.87 5.0	 5.0 0.5 —	 5.0 0.5 —	 10 0.87 5.0	 — — —	mA
Supply Current (All Four Amplifiers) Noninverting Inputs Open Noninverting Inputs Grounded	 I_{DO} I_{DG}	 — —	 6.9 7.8	 10 14	 — —	 6.9 7.8	 10 14	 — —	 6.9 7.8	 10 14	 — —	 6.9 7.8	 10 14	mA
Power Supply Rejection (f = 100 Hz)	PSR	—	55	—	—	55	—	—	55	—	—	55	—	dB
Mirror Gain ($T_A = T_{low}$ to T_{high}; Notes 1, 4) I_{in}^+ = 20 μA I_{in}^+ = 200 μA	A_i	0.90 0.90	1.0 1.0	1.1 1.1	0.90 0.90	1.0 1.0	1.1 1.1	0.90 0.90	1.0 1.0	1.1 1.1	0.90 0.90	1.0 1.0	1.1 1.0	μA
Δ Mirror Gain ($T_A = T_{low}$ to T_{high}; Notes 1, 4) 20 μA ≤ I_{in}^+ ≤ 200 μA	ΔA_i	—	2.0	5.0	—	2.0	5.0	—	2.0	5.0	—	2.0	5.0	%
Mirror Current ($T_A = T_{low}$ to T_{high}; Notes 1, 5)		—	10	500	—	10	500	—	10	500	—	10	500	μA
Negative Input Current (Note 6)		—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	mA

NOTES: 1. T_{low} = −40°C for LM2900, MC3301 = 0°C for LM3900, MC3401 T_{high} = +85°C for LM290, MC3301 = +70°C for LM3900, MC3401

2. Open-Loop voltage gain is defined as voltage gain from the inverting input to the output.
3. Sink current is specified for linear operation. When the device is used as a comparator (non-linear operation) where the inverting input is overdriven, the sink current (low level output current) capability is typically 5.0 mA.
4. This specification indicates the current gain of the current mirror which is used as the noninverting input.
5. Input V_{BE} match between the noninverting and inverting inputs occurs for a mirror current (noninverting input current) of approximately 10 μA.
6. Clamp transistors are included to prevent the input voltages from swinging below ground more than approximately −0.3 V. The negative input currents that may result from large signal overdrive with capacitive input coupling must be limited externally to values of approximately 1.0 mA. If more than one of the input terminals are simultaneously driven negative, maximum currents are reduced. Common mode biasing can be used to prevent negative input voltages.
7. When used as a noninverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.

2

Figure 1. Open-Loop Voltage Gain versus Frequency

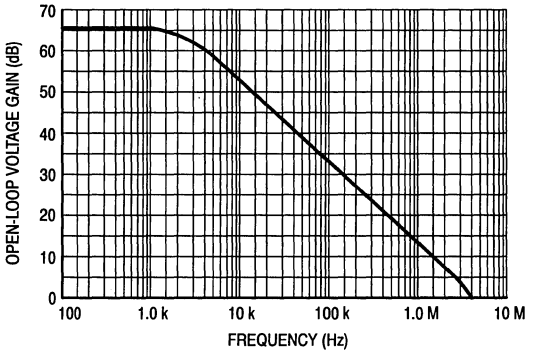


Figure 2. Open-Loop Voltage Gain versus Supply Voltage

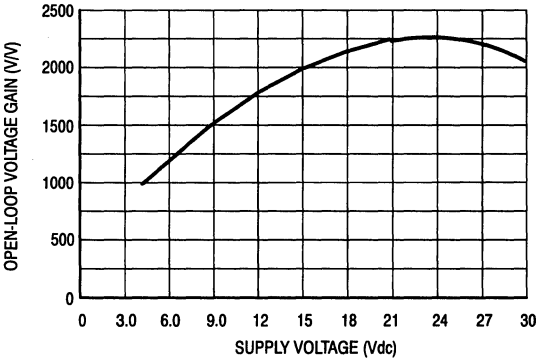


Figure 3. Output Resistance versus Frequency

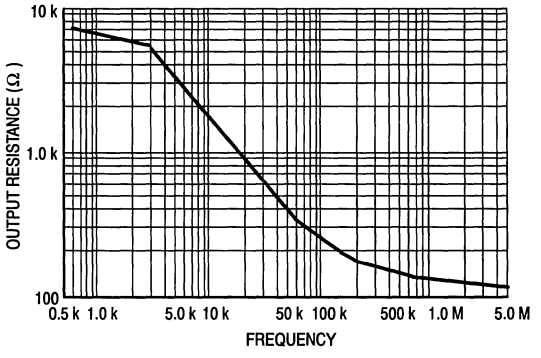


Figure 4. Supply Current versus Supply Voltage

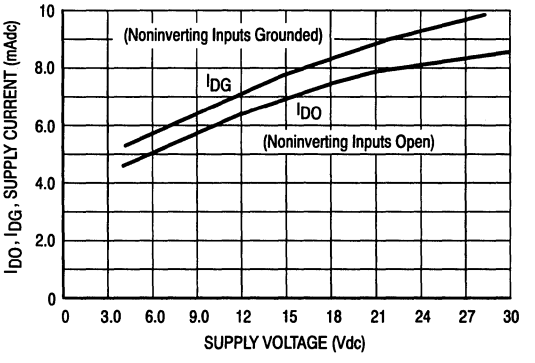


Figure 5. Linear Source Current versus Supply Voltage

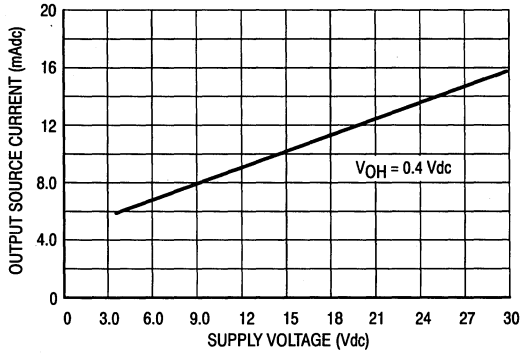
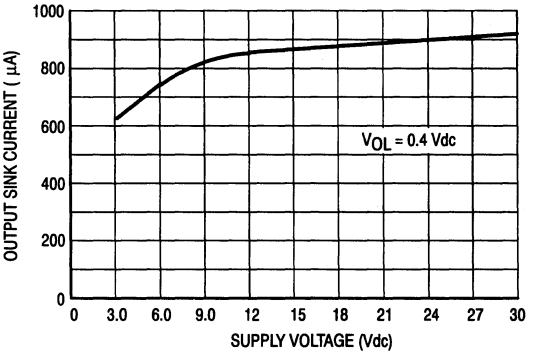


Figure 6. Linear Sink Current versus Supply Voltage

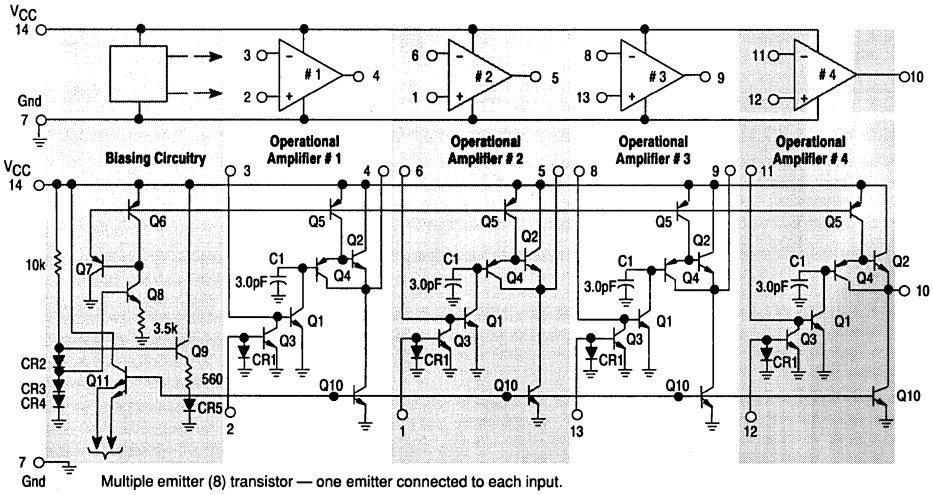


OPERATION AND APPLICATIONS

Basic Amplifier

The basic amplifier is the common emitter stage shown in Figures 7 and 8. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased Class A by the current source I_2. The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled linear operation at the output. The sink of the device can be forced to exceed the specified level by keeping the output dc voltage above ≈ 1.0 V resulting in an increase in the distortion appearing at the output. Closed-loop stability is maintained by an on-the-chip 3-pF capacitor shown in Figure 10 on the following page. No external compensation is required.

Figure 7. Block Diagram



Multiple emitter (8) transistor — one emitter connected to each input.

A noninverting input obtained by adding a current mirror as shown in Figure 9. Essentially all current which enters the noninverting input, $I_{in}+$, flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to $I_{in}+$. Since the alpha current gain of Q3 ≈ 1, its collector current is approximately equal to $I_{in}+$ also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the dc quiescent level at the output. Techniques for doing this are discussed in the "Normal Design Procedure" section.

Figure 8. A Basic Gain Stage

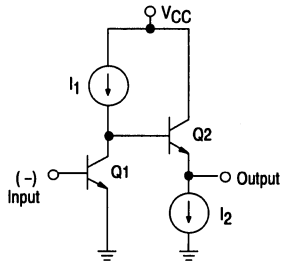
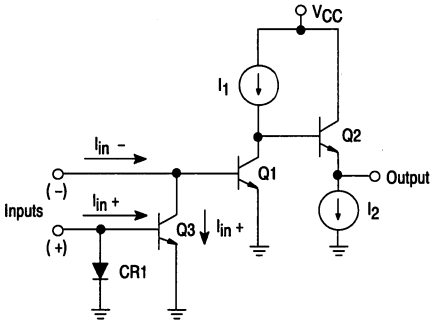


Figure 9. Obtaining A Noninverting Input



2

Biasing Circuitry

The circuitry common to all four amplifiers is shown in Figure 11. The purpose of this circuity is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, ect.) are set to the magnitude $V_{BE}/R1$ by transistor Q6. Transistor Q7 reduces base current loading. The voltage across resistor R_2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5 thus the current set is established by CR5 in all the NPN current sources (Q10, ect.). This technique results in current source magnitudes which are relatively independent of the supply voltage. Q11 (Figure 7) provides circuit protection from signals that are negative with respect to ground.

Figure 10. A Basic Operational Amplifier

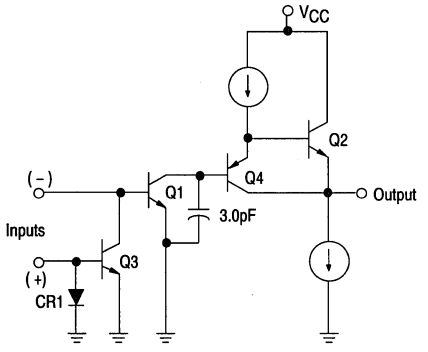
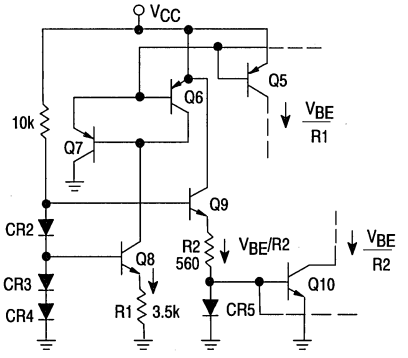


Figure 11. Biasing Circuitry



NORMAL DESIGN PROCEDURE

1. Output Q-Point Biasing
   A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing, as shown in Figures 12 and 13. The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 10 μA to 200 μA range.

   B. V_{CC} Reference Voltage (see Figures 12 and 13)
   The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor (R_r) allowing the input current, (I_{in}^+) to be within the range of 10 μA to 200 μA.

   Choosing the feedback resistor (R_f) to be equal to $^1/_2 R_r$ will now bias the amplifier output DC level to approximately $V_{CC}/2$. This allows the maximum dynamic range of the output voltage.

   C. Reference Voltage other than V_{CC} (see Figure 14)
   The biasing resistor (R_r) may be returned to a voltage(V_r) other than V_{CC}. By setting $R_f = R_r$, (still keeping I_{in} +between 10 μA and 200 μA) the output DC level will be equal to V_r. The expression for determining V_{Odc} is:

$$V_{Odc} = \frac{(A_i)(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r} A_i\right) \phi$$

   where ϕ is the V_{BE} drop of the input transistors (approximately 0.6 Vdc @ +25°C and assumed equal). A_i is the current mirror gain.

Figure 12. Inverting Amplifier

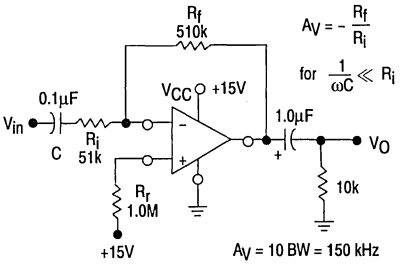
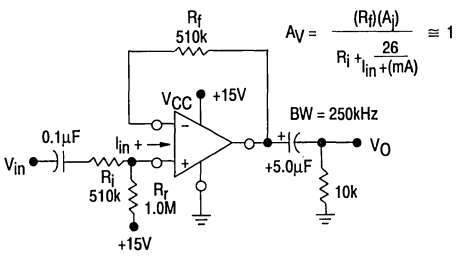


Figure 13. Noninverting Amplifier



2. Gain Determination

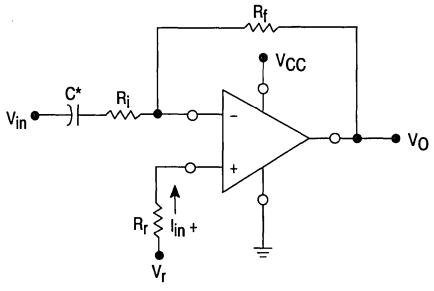
A. Inverting Amplifier

The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the dc bias and the output is normally capacitively coupled to eliminate the dc voltage across the load. Note that when the output is capacitively coupled to the load, the value of I_{sink} becomes a limitation with respect to the load driving capabilities of the device is direct coupled. In this configuration, the ac gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier:

$$A_V = \frac{R_f}{R_i}$$

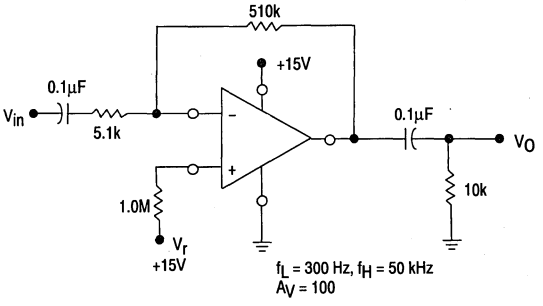
The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically be 400 kHz with 20 dB of closed-loop gain or 40 kHz with 40 dB of closed-loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed-loop gain intercepts the open-loop response curve. The inverting input capacity is typically 3.0 pF.

Figure 14. Inverting Amplifier with Arbitrary Reference



*Select for low frequency response.

Figure 15. Inverting Amplifier with $A_V = 100$ and $V_r = V_{CC}$



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B. Noninverting Amplifier

These devices may be used in the noninverting mode (see Figure 13). The amplifier gain in this configuration is subject to the current mirror gain. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_{in+}}$ Ω, where I_{in+} is input current in milliamperes. The noninverting AC gain expression is given by:

$$A_V = \frac{(R_f)(A_i)}{R_i + \frac{26}{I_{in+}(mA)}}$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For $R_f = 510\ k\Omega$ the bandwidth will be in excess of 200 kHz for noninverting of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the the input resistor is effectively isolated from the feedback loop.

Figure 16. Tachometer Circuit

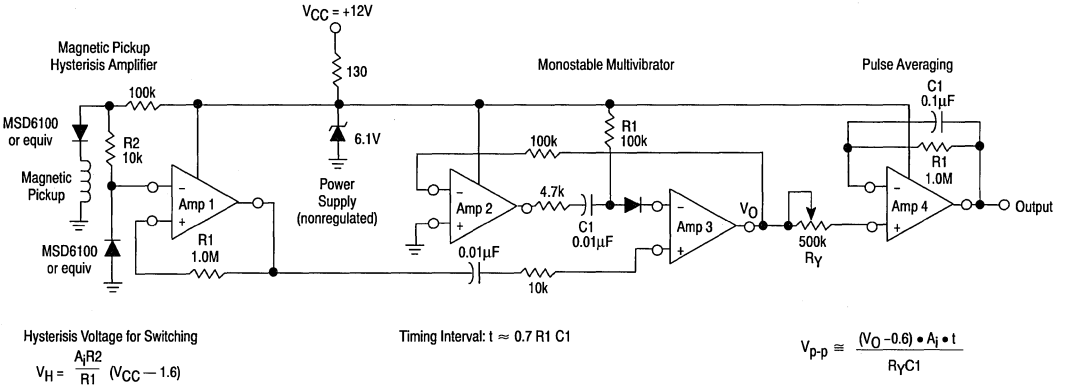
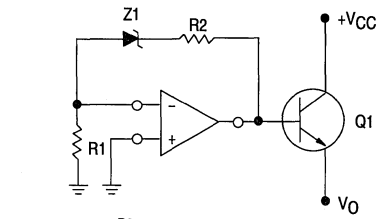


Figure 17. Voltage Regulator



Note: For positive T_C zeners R2 and R1 can be selected to give T_C output.

Figure 18. Logic "OR" Gate

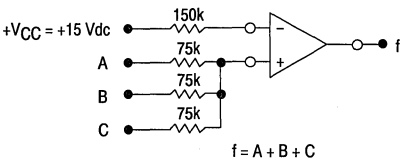


Figure 19. Logic "NAND" Gate (Large Fan-In)

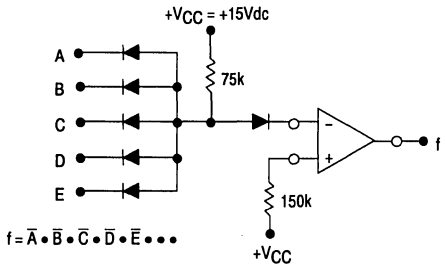


Figure 20. Logic "NOR" Gate

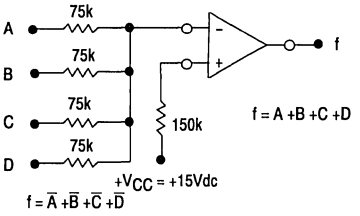


Figure 21. R-S Flip-Flop

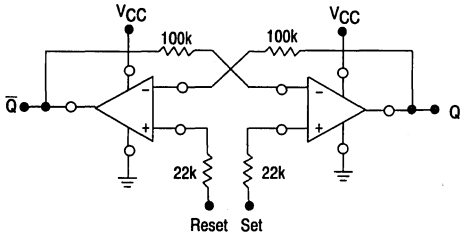


Figure 22. Astable Multivibrator

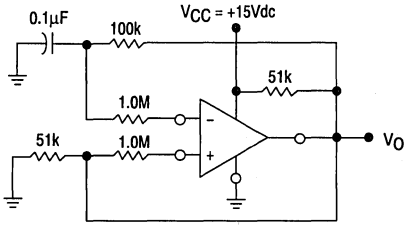


Figure 23. Positive-Edge Differentiator

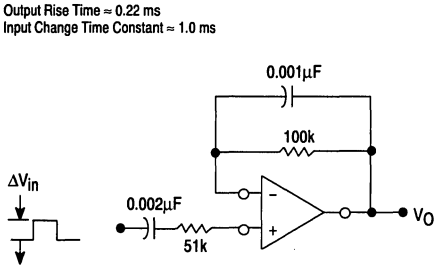


Figure 24. Negative-Edge Differentiator

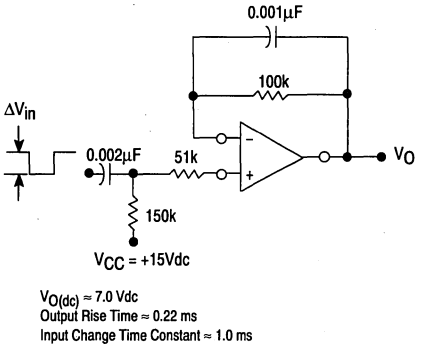


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Figure 25. Amplifier and Driver for a 50 Ω Line

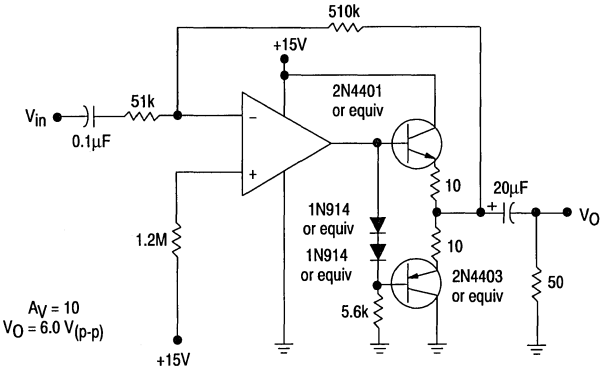


Figure 26. Basic Bandpass and Notch Filter

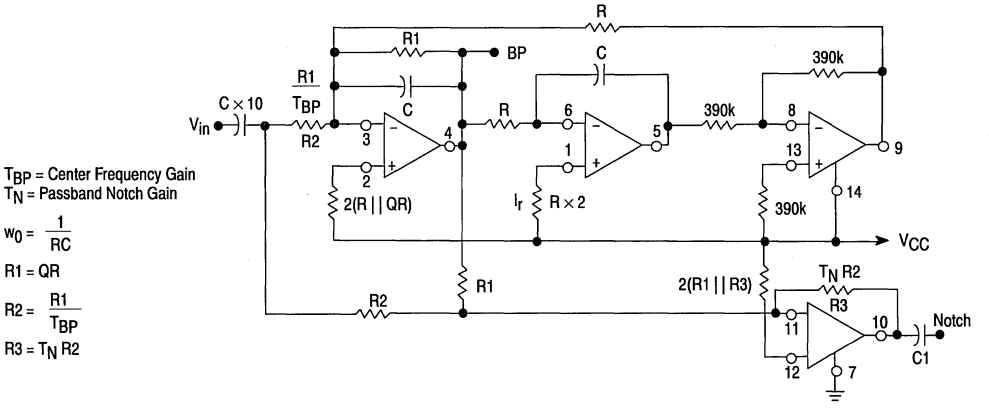


Figure 27. Bandpass and Notch Filter

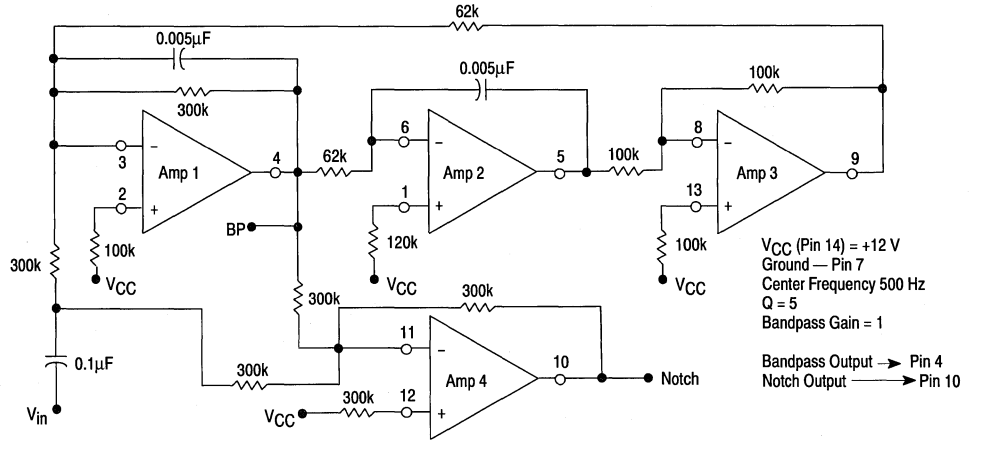
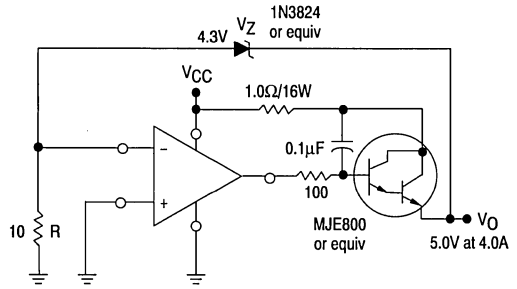


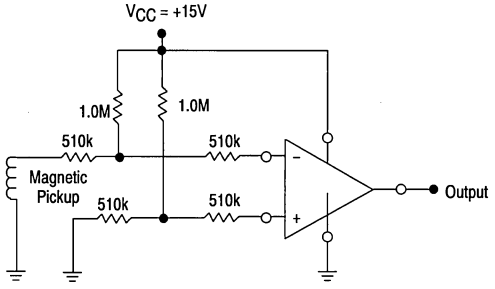
Figure 28. Voltage Regulator

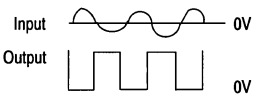


$V_O = V_Z + 0.6$ Vdc

NOTES:
1. R is used to bias the zener.
2. If the zener TC is positive, and equal in magnitude to the negative TC of the input to the operational amplifier (≈2.0 mV/°C), the output is zero-TC. A 7.0 V zener will give approximately zero-TC.

Figure 29. Zero Crossing Detector





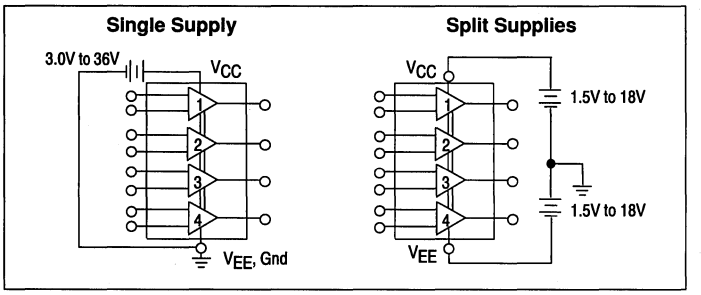
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2

Quad Low Power Operational Amplifiers

The MC3503 is a low cost, quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular MC1741. However, the MC3503 has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 V or as high as 36 V with quiescent currents about one third of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- Class AB Output Stage for Minimal Crossover Distortion
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 36 V
- Split Supply Operation: ±1.5 V to ±18 V
- Low Input Bias Currents: 500 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- Similar Performance to Popular MC1741
- Industry Standard Pinouts
- ESD Diodes Added for Increased Ruggedness



MAXIMUM RATINGS

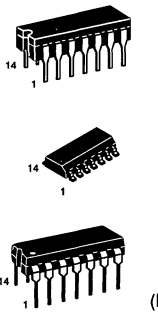
Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 36 ±18	Vdc
Input Differential Voltage Range (Note 1)	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range (Notes 1, 2)	V_{ICR}	±18	Vdc
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 –65 to +150 –55 to +125	°C
Operating Ambient Temperature Range MC3303 MC3403 MC3503	T_A	 0 to +70 –40 to +85 –55 to +125	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

NOTES: 1. Split power supplies.
2. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

MC3403
MC3503
MC3303

QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SILICON MONOLITH INTEGRATED CIRCUIT

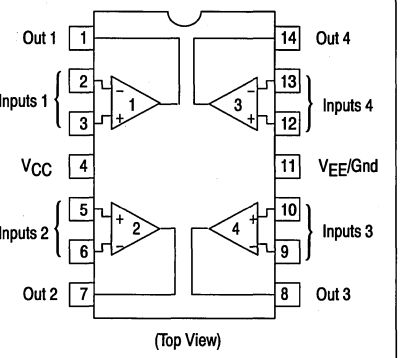


L SUFFIX
CERAMIC PACKAGE
CASE 632

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC3403 and MC3303 Only)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC3303D	–40° to +85°C	SO-14
MC3303L		Ceramic DIP
MC3303P		Plastic DIP
MC3403D	0° to +70°C	SO-14
MC3403L		Ceramic DIP
MC3403P		Plastic DIP
MC3503L	–55° to +125°C	Ceramic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V for MC3503, MC3403; V_{CC} = +14 V, V_{EE} = Gnd for MCC3303 T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	MC3503			MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $T_A = T_{high}$ to T_{low} (Note 1)	V_{IO}	— —	2.0 —	5.0 6.0	— —	2.0 —	10 12	— —	2.0 —	8.0 10	mV
Input Offset Current $T_A = T_{high}$ to T_{low}	I_{IO}	— —	30 —	50 200	— —	30 —	50 200	— —	30 —	75 250	nA
Large Signal Open-Loop Voltage Gain V_O = ±10 V, R_L = 2.0 kΩ $T_A = T_{high}$ to T_{low}	A_{VOL}	50 25	200 —	— —	20 15	200 —	— —	20 15	200 —	— —	V/mV
Input Bias Current $T_A = T_{high}$ to T_{low}	I_{IB}	— —	–200 –300	–500 –1500	— —	–200 —	–500 –800	— —	–200 —	–500 –1000	nA
Output Impedance f = 20 Hz	z_o	–	75	—	—	75	—	—	75	—	Ω
Input Impedance f = 20 Hz	z_i	0.3	1.0	—	0.3	1.0	—	0.3	1.0	—	MΩ
Output Voltage Range R_L = 10 kΩ R_L = 2.0 kΩ R_L = 2.0 kΩ, $T_A = T_{high}$ to T_{low}	V_O	±12 ±10 ±10	±13.5 ±13 —	— — —	±12 ±10 ±10	±13.5 ±13 —	— — —	±12 ±10 ±10	±12.5 ±12 —	— — —	V
Input Common Mode Voltage Range	V_{ICR}	+13 V $-V_{EE}$	+13.5 V $-V_{EE}$	—	+13 V $-V_{EE}$	+13 V $-V_{EE}$	—	+12 V $-V_{EE}$	+12.5 V $-V_{EE}$	—	V
Common Mode Rejection $R_S \leq$ 10 k Ω	CMR	70	90	—	70	90	—	70	90	—	dB
Power Supply Current (V_O = 0) $R_L = \infty$	I_{CC},I_{EE}	—	2.8	4.0	—	2.8	7.0	—	2.8	7.0	mA
Individual Output Short-Circuit Current (2)	I_{SC}	±10	±30	±45	±10	±20	±45	±10	±30	±45	mA
Positive Power Supply Rejection Ratio	PSRR+	—	30	150	—	30	150	—	30	150	µV/V
Negative Power Supply Rejection Ratio	PSRR–	—	30	150	—	30	150	—	30	150	µV/V
Average Temperature Coefficient of Input Offset Current $T_A = T_{high}$ to T_{low}	$\Delta I_{IO}/\Delta T$	—	50	—	—	50	—	—	50	—	pA/°C
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{high}$ to T_{low}	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	—	10	—	µV/°C
Power Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 20 V(p-p), THD = 5%	BWp	—	9.0	—	—	9.0	—	—	9.0	—	kHz
Small-Signal Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 50 mV	BW	—	1.0	—	—	1.0	—	—	1.0	—	MHz
Slew Rate A_V = 1, V_i = –10 V to +10 V	SR	—	0.6	—	—	0.6	—	—	0.6	—	V/µs
Rise Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{TLH}	—	0.35	—	—	0.35	—	—	0.35	—	µs
Fall Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{TLH}	—	0.35	—	—	0.35	—	—	0.35	—	µs
Overshoot A_V = 1, R_L = 10 kΩ, V_O = 50 mV	OS	—	20	—	—	20	—	—	20	—	%
Phase Margin A_V = 1, R_L = 2.0 kΩ, V_O = 200 pF	ϕm	—	60	—	—	60	—	—	60	—	Degrees
Crossover Distortion (V_{in} = 30 mVp-p, V_{out}= 2.0 Vp-p, f = 10 kHz)	—	—	1.0	—	—	1.0	—	—	1.0	—	%

NOTE: 1. T_{high} = 125°C for MC3503, 70°C for MC3403, 85°C for MC3303
T_{low} = –55°C for MC3503, 0°C for MC3403, –40°C for MC3303

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

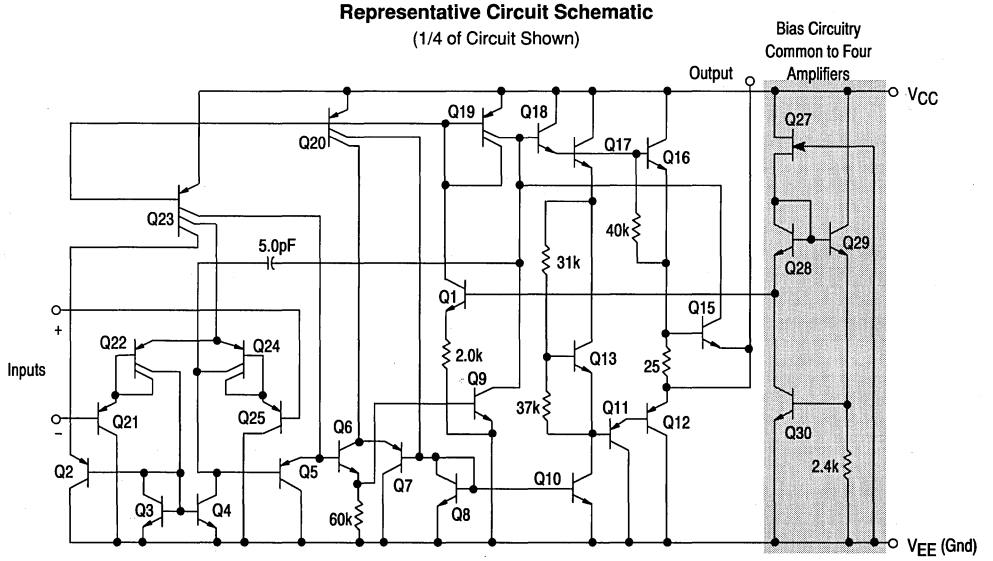
Characteristics	Symbol	MC3503			MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	2.0	5.0	—	2.0	10	—	—	10	mV
Input Offset Current	I_{IO}	—	30	50	—	30	50	—	—	75	nA
Input Bias Current	I_{IB}	—	–200	–500	—	–200	–500	—	—	–500	nA
Large Signal Open-Loop Voltage Gain R_L = 2.0 kΩ	A_{VOL}	10	200	—	10	200	—	10	200	—	V/mV
Power Supply Rejection Ratio	PSRR	—	—	150	—	—	150	—	—	150	µV/V
Output Voltage Range (3) R_L = 10 kΩ, V_{CC} = 5.0 V R_L = 10 kΩ, 5.0 ≤ V_{CC} ≤ 30 V	V_{OR}	3.3 V_{CC}–2.0	3.5 V_{CC}–1.7	— —	3.3 V_{CC}–2.0	3.5 V_{CC}–1.7	— —	3.3 V_{CC}–2.0	3.5 V_{CC}–1.7	— —	Vp-p
Power Supply Current	I_{CC}	—	2.5	4.0	—	2.5	7.0	—	2.5	7.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	CS	—	–120	—	—	–120	—	—	–120	—	dB

NOTES: 2. Not to exceed maximum package power dissipation.
3. Output will swing to ground with a 10 kΩ pull down resistor.

2

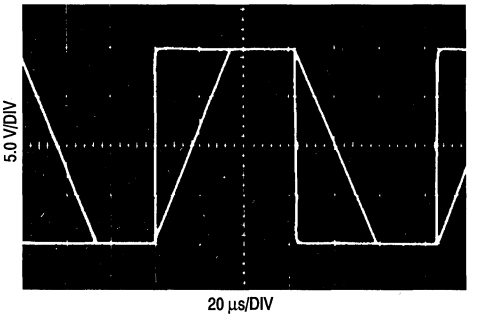
Representative Circuit Schematic

(1/4 of Circuit Shown)



CIRCUIT DESCRIPTION

Inverter Pulse Response



The MC3503/3403/3303 is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input device Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 an Q22. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because Class AB operation is utilized.

Each amplifier is biased from an internal voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

Figure 1. Sine Wave Response

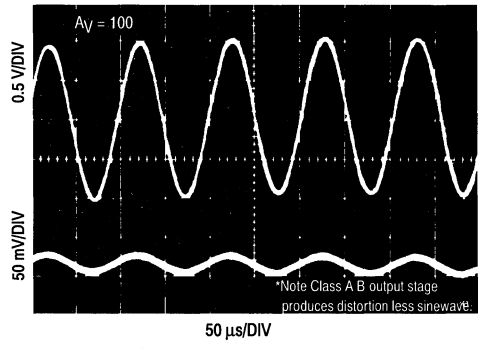


Figure 2. Open-Loop Frequency Response

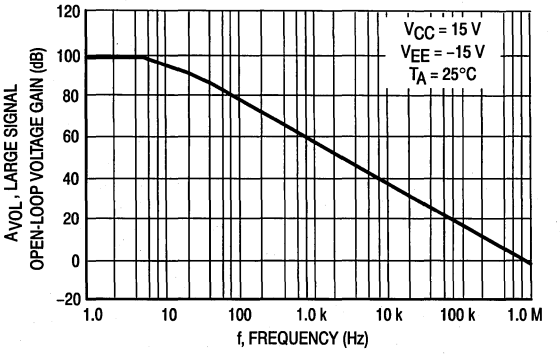


Figure 3. Power Bandwidth

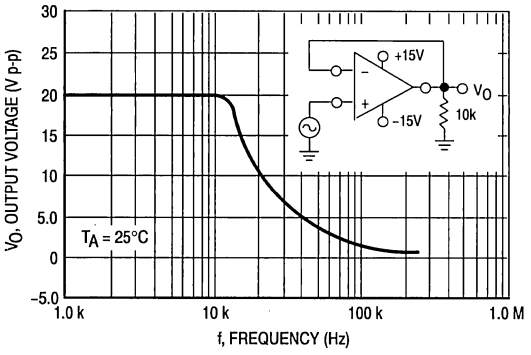


Figure 4. Output Swing versus Supply Voltage

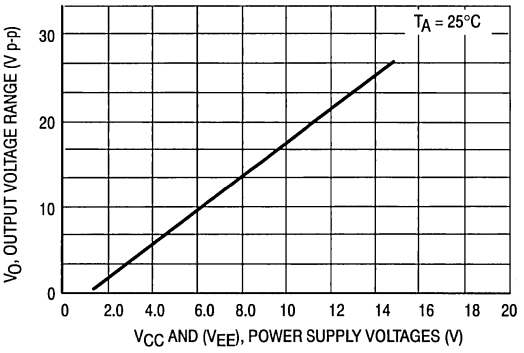


Figure 5. Input Bias Current versus Temperature

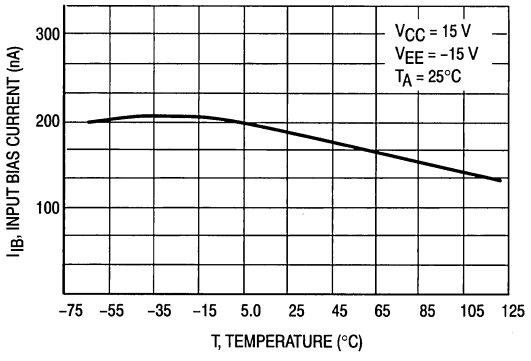


Figure 6. Input Bias Current versus Supply Voltage

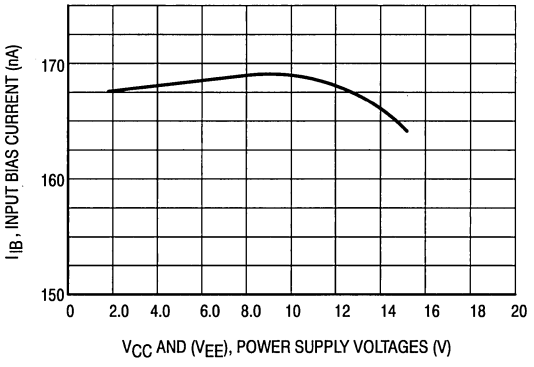


Figure 7. Voltage Reference

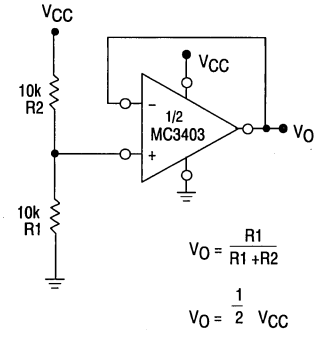
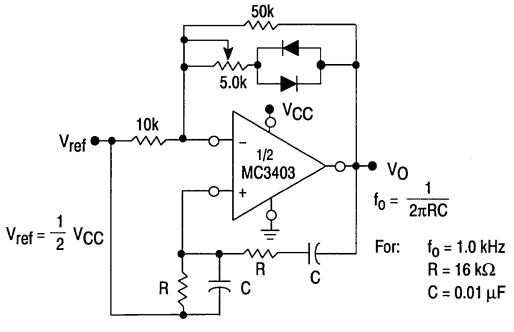


Figure 8. Wien Bridge Oscillator



2

Figure 9. High Impedance Differential Amplifier

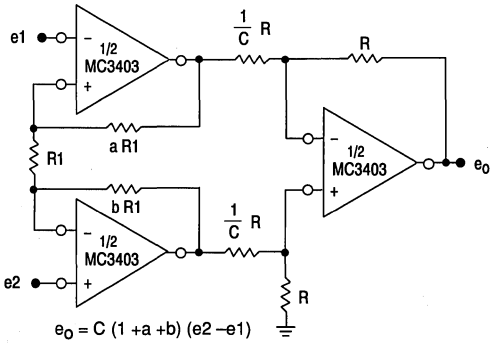


Figure 10. Comparator with Hysteresis

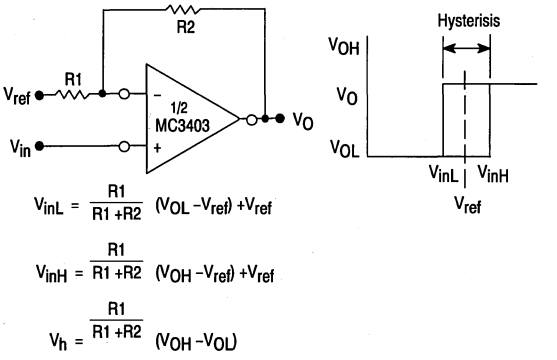
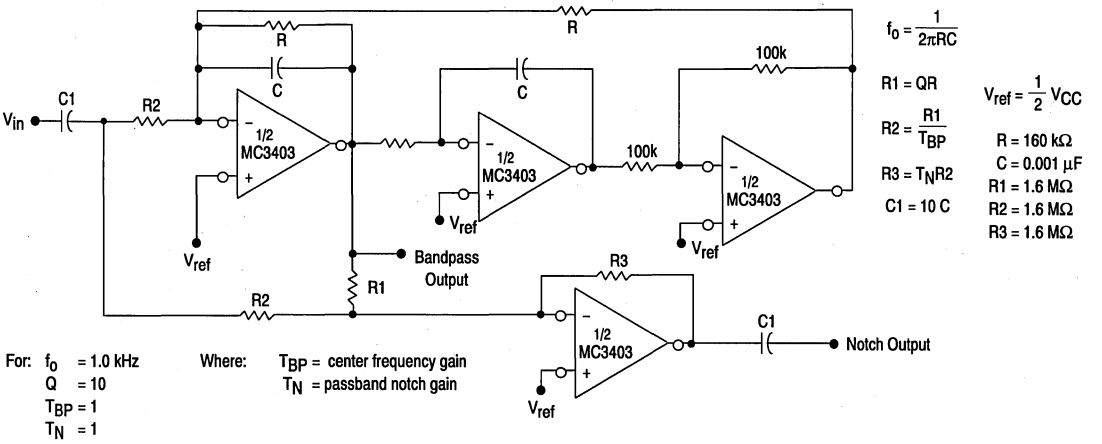


Figure 11. Bi-Quad Filter



For: f_0 = 1.0 kHz, Q = 10, T_{BP} = 1, T_N = 1

Where: T_{BP} = center frequency gain, T_N = passband notch gain

Figure 12. Function Generator

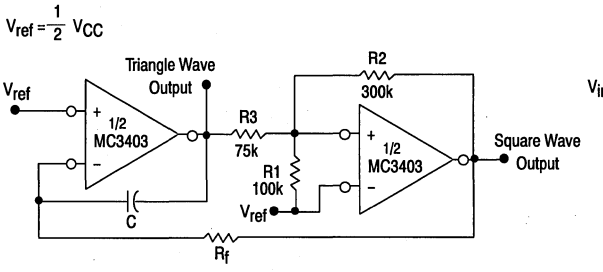
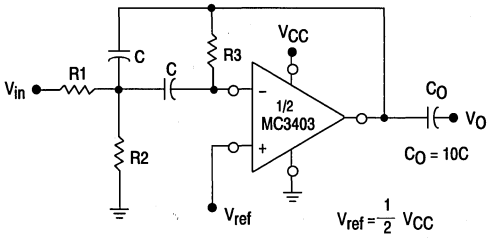


Figure 13. Multiple Feedback Bandpass Filter



Given: f_0 = center frequency

$A(f_0)$ = gain at center frequency

Choose value f_0, C

Then: $R3 = \frac{Q}{\pi f_0 C}$ $R1 = \frac{R3}{2A(f_0)}$ $R2 = \frac{R1\,R5}{4Q^2\,R1 - R5}$

For less than 10% error from operational amplifier $\frac{O_0 f_0}{BW} < 0.1$

where, f_0 and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

MC3405
MC3505

Dual Operational Amplifier and Dual Comparator

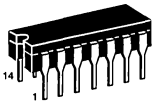
The MC3405/3505 contains two differential-input operational amplifiers and two comparators, each set capable of single supply operation. This operational amplifier-comparator circuit fulfills its applications as a general purpose product for automotive and consumer circuits as well as an industrial building block.

The MC3405 is specified over the commercial operating temperature range of 0° to +70°C, while the MC3505 is specified over the military operating range of –55° to +125°C.

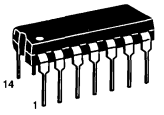
- Operational Amplifiers Equivalent in Performance to MC3403/3503
- Comparators Similar in Performance to LM339/139
- Single Supply Operation: 3.0 V to 36 V
- Split Supply Operation: ±1.5 V to ±18 V
- Low Supply Current Drain
- Operational Amplifiers are Internally Frequency Compensated
- Comparators TTL and CMOS Compatible

DUAL
OPERATIONAL AMPLIFIER/
DUAL VOLTAGE COMPARATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT

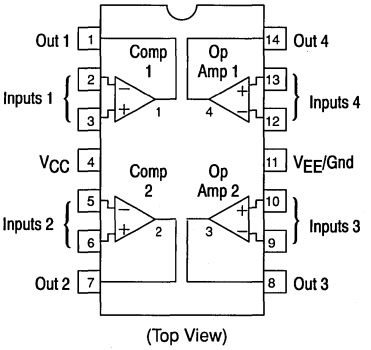


L SUFFIX
CERAMIC PACKAGE
CASE 632



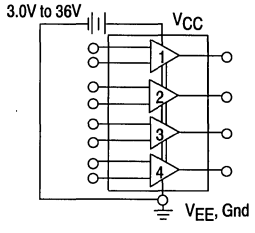
P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS

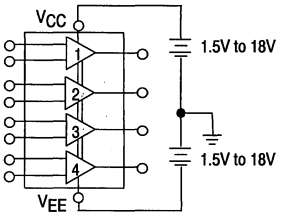


(Top View)

Single Supply



Split Supplies



ORDERING INFORMATION

Device	Temperature Range	Package
MC3405L	0° to +70°C	Ceramic DIP
MC3405P	0° to +70°C	Plastic DIP
MC3505L	–55° to +125°C	Ceramic DIP

2

OPERATIONAL AMPLIFIER SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage — Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	36 ±18	Vdc
Input Differential Voltage Range	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range	V_{ICR}	±18	Vdc
Operating Ambient Temperature Range — MC3505 MC3405	T_A	–55 to +125 0 to +70	°C
Storage Temperature Range — Ceramic Package Plastic Package	Tstg	–65 to +150 –55 to +125	°C
Operating Junction Temperature Range — Ceramic Package Plastic Package	T_J	175 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	MC3505 Min	MC3505 Typ	MC3505 Max	MC3405 Min	MC3405 Typ	MC3405 Max	Unit
Input Offset Voltage	V_{IO}	—	2.0	5.0	—	2.0	10	mV
Input Offset Current	I_{IO}	—	30	50	—	30	50	nA
Input Bias Current	I_{IB}	—	–200	–500	—	–200	–500	nA
Large-Signal, Open-Loop Voltage Gain (R_L = 2.0 kΩ)	A_{VOL}	20	200	—	20	200	—	V/mV
Power Supply Rejection	PSR	—	—	150	—	—	150	μV/V
Output Voltage Range (Note 1) (R_L = 10 kΩ, V_{CC} = 5.0 V) (R_L = 10 kΩ, 5.0 V ≤ V_{CC} ≤ 30 V)	V_{OR}	 3.3 V_{CC} –2.0	 3.5 V_{CC} –1.7	 — —	 3.3 V_{CC}–2.0	 3.5 V_{CC} –1.7	 — —	V_{p-p}
Power Supply Current (Notes 2 and 3)	I_{CC}	—	2.5	4.0	—	2.5	7.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	—	—	–120	—	—	–120	—	dB

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Input Offset Voltage (T_A = T_{low} + T_{high}) (Note 4)	V_{IO}	— —	2.0 —	5.0 6.0	— —	2.0 —	10 12	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	—	15	—	—	15	—	μV/°C
Input Offset Current (T_A = T_{low} to T_{high}) (Note 4)	I_{IO}	— —	— —	50 200	— —	— —	50 200	nA
Input Bias Current (T_A = T_{low} to T_{high}) (Note 4)	I_{IB}	— —	–200 –300	–500 –1500	— —	–200 —	–500 –800	nA
Input Common Mode Voltage Range	V_{ICR}	+13 –V_{EE}	—	—	+13 –V_{EE}	—	—	Vdc
Large Signal, Open-Loop Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ) (T_A = T_{low} to T_{high}) (Note 4)	A_{VOL}	 50 25	 200 100	 — —	 20 15	 200 100	 — —	V/mV
Common Mode Rejection	CMR	70	90	—	70	90	—	dB
Power Supply Rejection Ratio	PSRR	—	30	150	—	30	150	μV/V
Output Voltage (R_L = 10 kΩ) (R_L = 2.0 kΩ) (R_L = 2.0 kΩ, T_A = T_{low} to T_{high}) (Note 4)	V_O	 ±12 ±10 ±10	 ±13.5 ±13 —	 — — —	 ±12 ±10 ±10	 ±13.5 ±13 —	 — — —	Vdc
Output Short Circuit Current	I_{SC}	±10	±30	±45	±10	±20	±45	mA
Power Supply Current (Notes 2 and 3)	I_{CC}, I_{EE}	—	2.8	4.0	—	2.8	7.0	mA
Phase Margin	ϕm	—	60	—	—	60	—	Degrees
Small-Signal Bandwidth (A_V = 1, R_L = 10 kΩ, V_O = 50 mV)	BW	—	1.0	—	—	1.0	—	MHz
Power Bandwidth (A_V = 1, R_L = 2.0 kΩ, V_O = 20 V_{p-p}, THD = 5%)	BWp	—	9.0	—	—	9.0	—	kHz
Rise Time/Fall Time	t_{TLH}, t_{THL}	—	0.35	—	—	0.35	—	μs
Overshoot (A_V = 1, R_L = 10 kΩ, V_O = 50 mV)	OS	—	20	—	—	20	—	%
Slew Rate	SR	—	0.6	—	—	0.6	—	V/μs

NOTES: 1. Output will swing to groung.
2. Not to exceed maximum package power dissipation.
3. For Operational Amplifier and Comparator.
4. T_{low} = –55°C for MC3505 = 0°C for MC3405 T_{high} = +125°C for MC3505 = +70°C for MC3405

COMPARATOR SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage — Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	36 ±18	Vdc
Input Differential Voltage Range	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range	V_{ICR}	−0.3 to +36	Vdc
Sink Current	I_{Sink}	20	mA
Operating Ambient Temperature Range — MC3505 MC3405	T_A	−55 to +125 0 to +70	°C
Storage Temperature Range — Ceramic Package Plastic Package	Tstg	−65 to +150 −55 to +125	°C
Operating Junction Temperature Range — Ceramic Package Plastic Package	T_J	175 150	°C

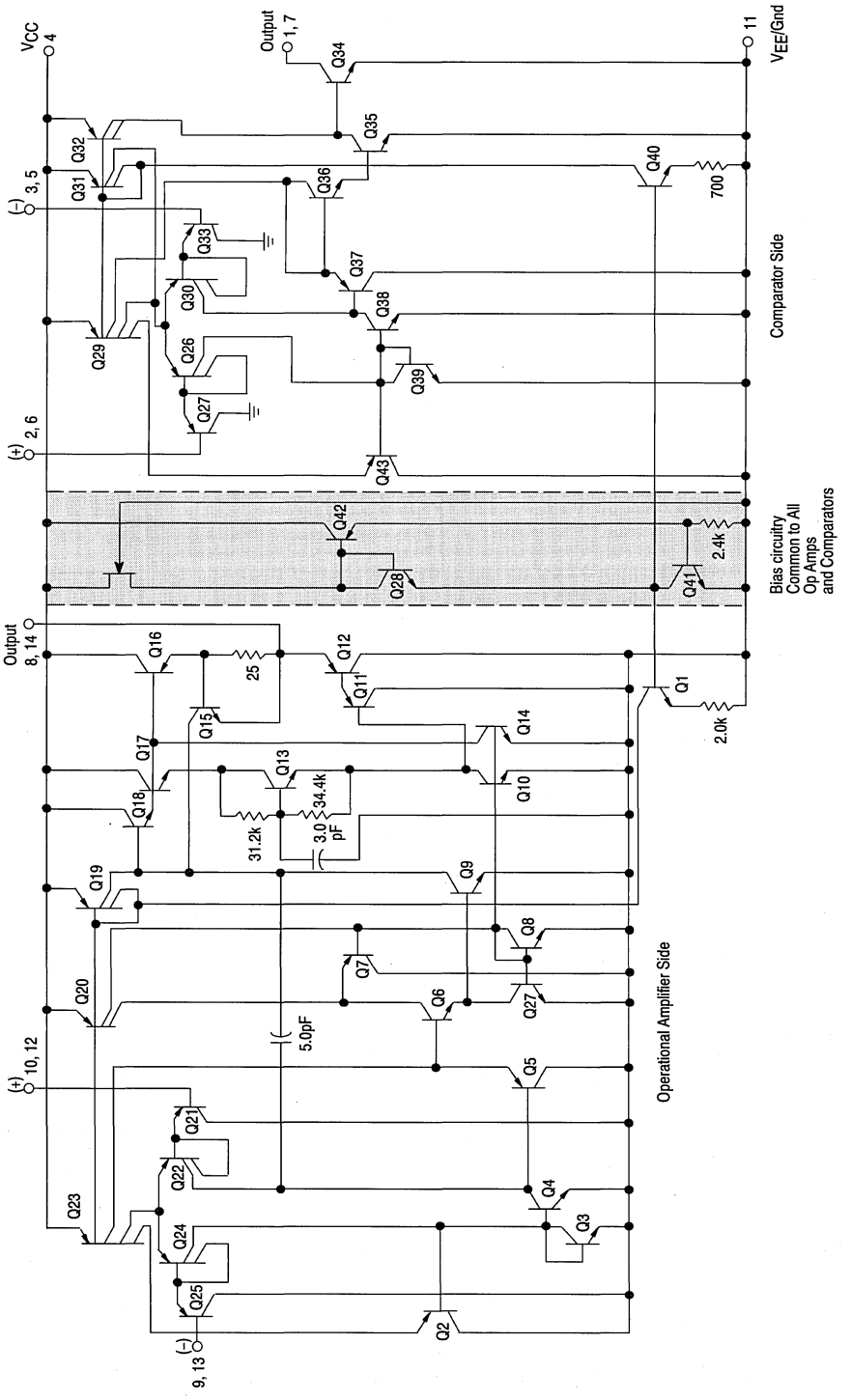
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	MC3505 Min	MC3505 Typ	MC3505 Max	MC3405 Min	MC3405 Typ	MC3405 Max	Unit
Input Offset Voltage (T_A = T_{low} to T_{high}) (Notes 1 and 2)	V_{IO}	— —	2.0 —	5.0 9.0	— —	2.0 —	10 12	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	—	15	—	—	15	—	µV/°C
Input Offset Current (T_A = T_{low} to T_{high}) (Note 1)	I_{IO}	— —	50 —	75 150	— —	50 —	100 200	nA
Input Bias Current (T_A = T_{low} to T_{high}) (Note 1)	I_{IB}	— —	−125 —	−500 −1500	— —	−125 —	−500 −800	nA
Input Common Mode Voltage Range (T_A = T_{low} to T_{high}) (Note 1)	V_{ICR}	0 0	V_{CC} −1.5 V_{CC} −1.7	V_{CC} −1.7 V_{CC} −2.0	0 0	V_{CC} −1.5 V_{CC} −1.7	V_{CC} −1.7 V_{CC} −2.0	Vp-p
Input Differential Voltage (All V_{in} ≥ 0 Vdc)	V_{ID}	—	—	36	—	—	36	V
Large-Signal, Open-Loop Voltage Gain (R_L = 15 kΩ)	A_{VOL}	—	200	—	—	200	—	V/mV
Output Sink Current ($-V_{in}$ ≥ 1.0 Vdc, $+V_{in}$ = 0, V_O ≤ 1.5 V)	I_{Sink}	6.0	16	—	6.0	16	—	mA
Low Level Output Voltage ($+V_{in}$ = 0 V, $-V_{in}$ = 1.0 V, I_{Sink} = 4.0 mA) (T_A = T_{low} to T_{high}) (Note 1)	V_{OL}	— —	350 —	500 700	— —	350 —	500 700	µA
Output Leakage Current ($+V_{in}$ ≥ 1.0 Vdc, $-V_{in}$ = 0, V_O = 5.0 Vdc) (T_A = T_{low} to T_{high}) (Note 1)	I_{OL}	— —	0.1 0.1	1.0 1.0	— —	0.1 0.1	1.0 1.0	µA
Large-Signal Response	—	—	300	—	—	300	—	ns
Response Time (Note 3) (V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ)	—	—	1.3	—	—	1.3	—	µs

NOTES: 1. T_{low} = −55°C for MC3505 T_{high} = +125°C for MC3505
= 0°C for MC3405 = +70°C for MC3405
2. V_O ≅ 1.4 V, R_S = 0 Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the input common mode range 0 to V_{CC} −1.7 V.
3. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals 300 ns is typical.

2

Circuit Schematic
(1/2 of Circuit Shown)



OPERATIONAL AMPLIFIER SECTION

Figure 1. Sine Wave Response

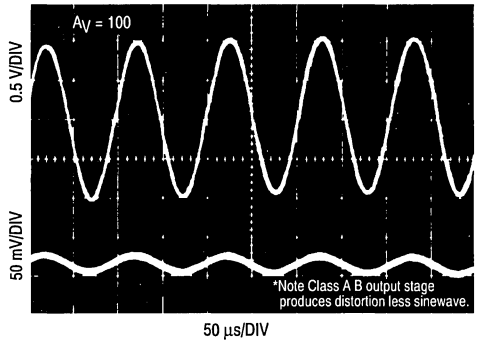


Figure 2. Open-Loop Frequency Response

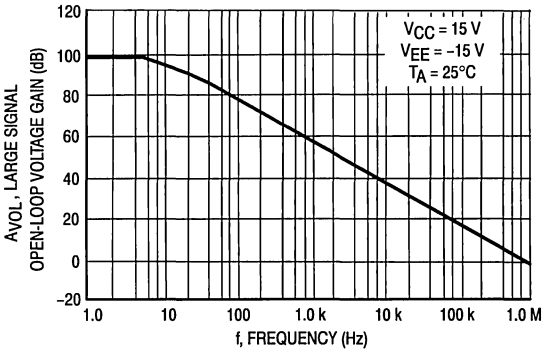


Figure 3. Power Bandwidth

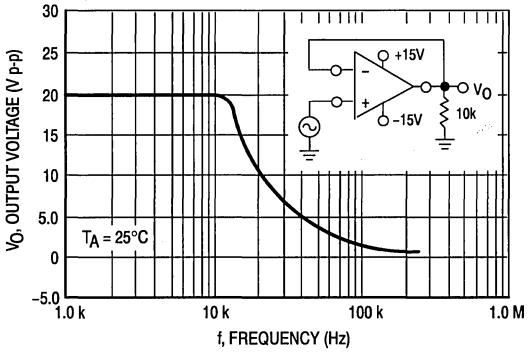


Figure 4. Output Swing versus Supply Voltage

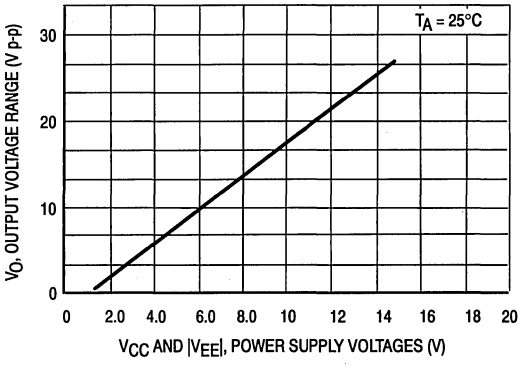


Figure 5. Input Bias Current versus Temperature

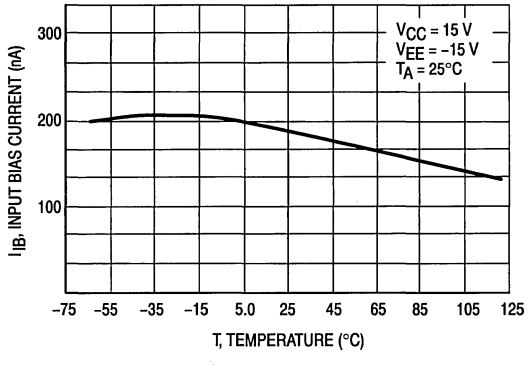
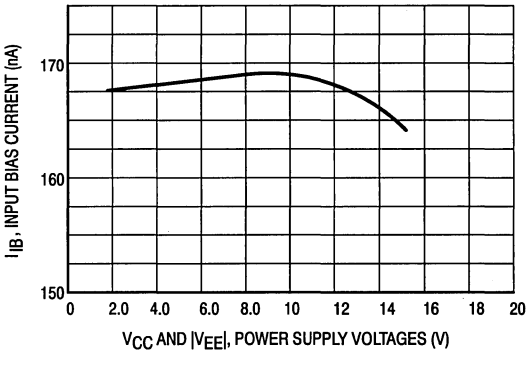


Figure 6. Input Bias Current versus Supply Voltage



COMPARATOR SECTION

Figure 7. Normalized Input Offset Voltage

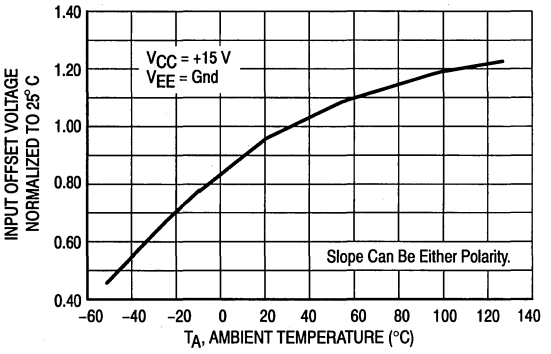


Figure 8. Input Bias Current

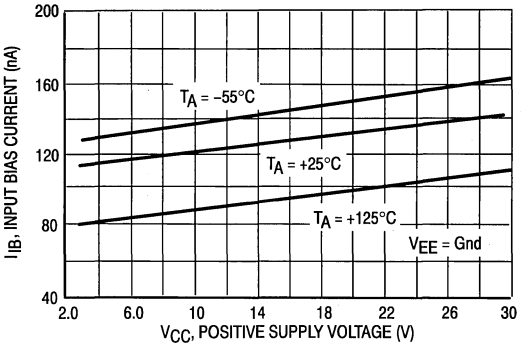


Figure 9. Normalized Input Offset Current

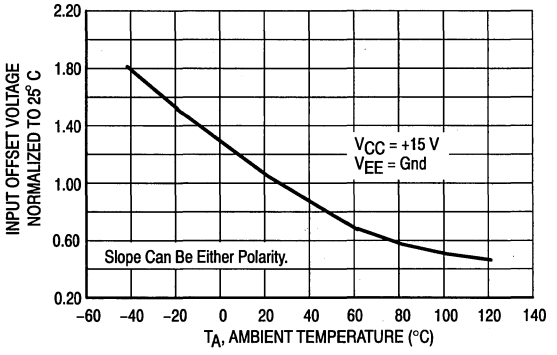


Figure 10. Output Sink Current versus Output Voltage

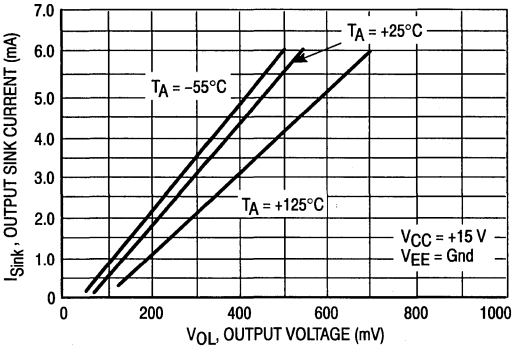
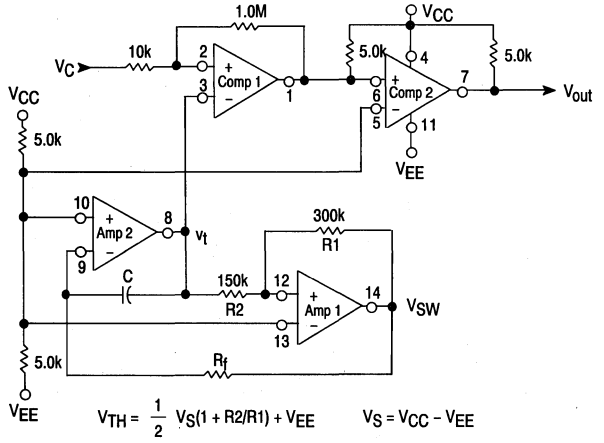


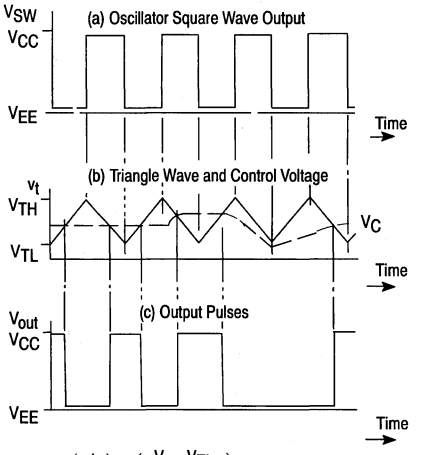
Figure 11. Pulse Width Modulator Schematic and Waveforms



$$V_{TH} = \frac{1}{2} V_S(1 + R2/R1) + V_{EE} \qquad V_S = V_{CC} - V_{EE}$$

$$V_{TL} = \frac{1}{2} V_S(1 - R2/R1) + V_{EE}$$

$$\text{Oscillator Frequency } f = \frac{R1}{4R_fCR2}$$



$$\text{Pulse Width} = \left(\frac{1}{f}\right)\left(\frac{V_C - V_{TL}}{V_{TH} - V_{TL}}\right) \text{ when: } V_{TL} < V_C < V_{TH}$$

$$\text{Duty Cycle in \%} = \left(\frac{V_C - V_{TL}}{V_{TH} - V_{TL}}\right)(100)$$

Figure 12. Window Comparator

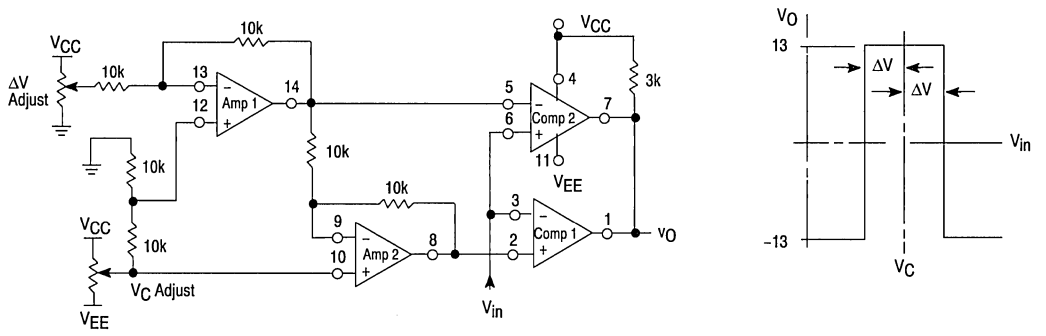
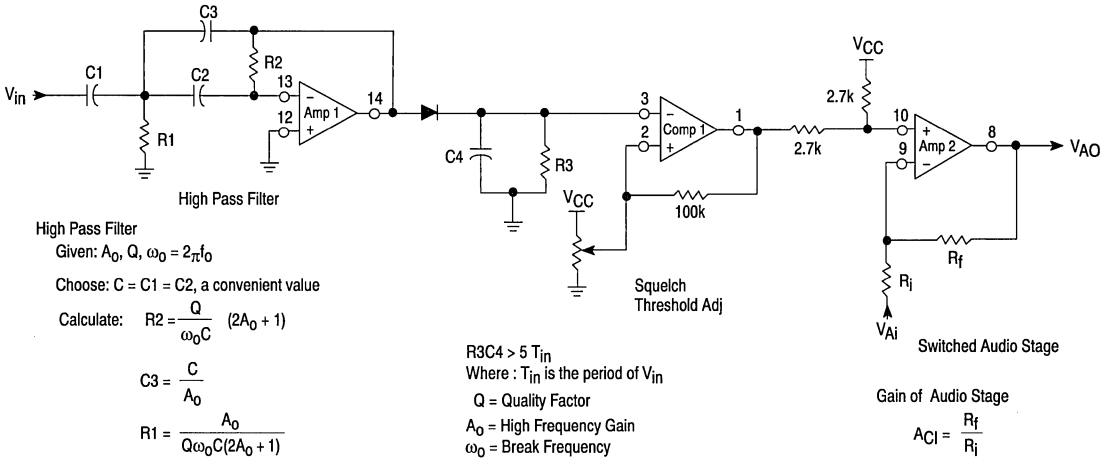


Figure 13. Squelch Circuit for AM or FM



High Pass Filter

Given: A_o, Q, $\omega_o = 2\pi f_o$

Choose: C = C1 = C2, a convenient value

Calculate: $R2 = \frac{Q}{\omega_o C} (2A_o + 1)$

$C3 = \frac{C}{A_o}$

$R1 = \frac{A_o}{Q\omega_o C(2A_o + 1)}$

$R3C4 > 5\ T_{in}$

Where : T_{in} is the period of V_{in}

Q = Quality Factor

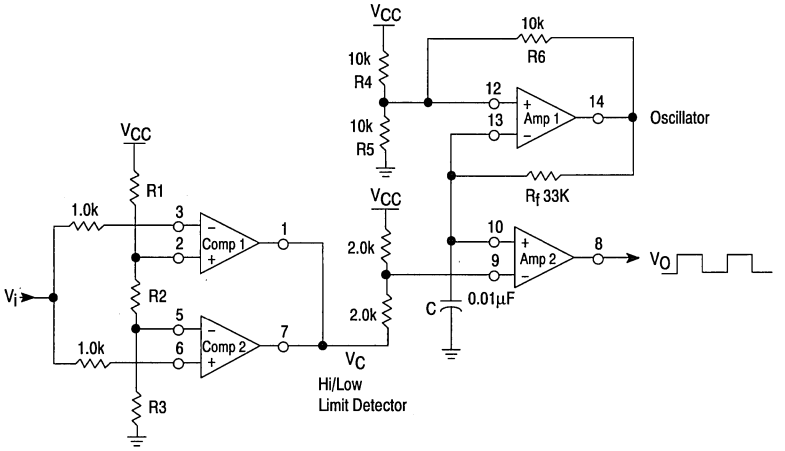
A_o = High Frequency Gain

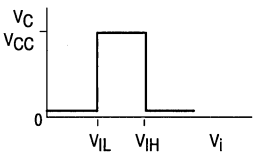
ω_o = Break Frequency

Gain of Audio Stage

$A_{CL} = \frac{R_f}{R_i}$

Figure 14. High/Low Limit Alarm





$V_{IL} = V_{CC} \frac{R3}{R1 + R2 + R3}$

$V_{IH} = V_{CC} \frac{R2 + R3}{R1 + R2 + R3}$

Oscillator

If R4 = R5 = R6

$f = 0.72/R_fC$

As shown, f = 2.2 kHz

V_O will oscillate if $V_{IH} < V_i$, or $V_{IL} > V_i$

V_O will be low if $V_{IL} < V_i < V_{IH}$

Figure 15. Zero Crossing Detector with Temperature Sensor

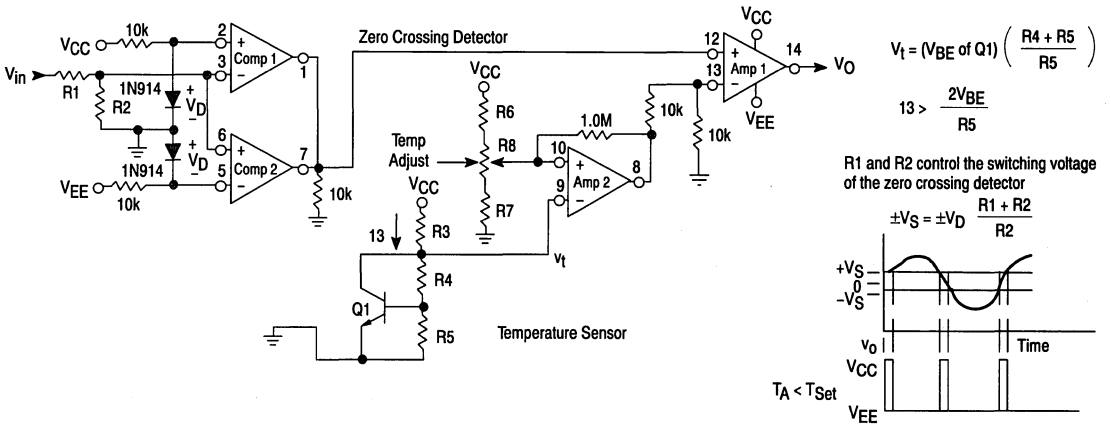
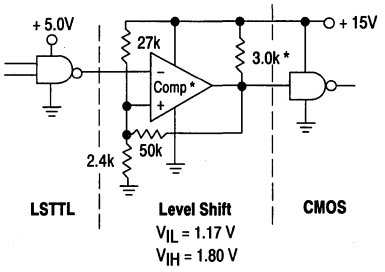
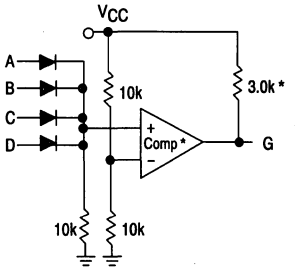


Figure 16. LSTTL to CMOS Interface with Hysteresis



*The same configuration may be used with an op amp if the 3.0 k resistor is removed.

Figure 17. NOR Gate



*The same configuration may be used with an op amp if the 3.0 k resistor is removed.

MC3430 thru MC3433

QUAD HIGH SPEED VOLTAGE COMPARATORS

Quad, Differential Voltage Comparator/Sense Amplifiers

The MC3430 thru MC3433 high speed comparators are ideal for applications as sense amplifiers in MOS memory systems. They are specified in a unique way which combines the effects of input offset voltage, input offset current, voltage gain, temperature variations and input common mode range into a single functional parameter. This parameter, called Input Sensitivity, specifies a minimum differential input voltage which will guarantee a given logic state. Four variations are offered in the comparator series.

The MC3430 and MC3431 versions feature a three-state strobe input common to all four channels which can be used to place the four outputs in a high impedance state. These two devices use active pull-up MTTL compatible outputs. The MC3432 and MC3433 are open-collector types which permit the implied AND connection. The MC3430 and MC3432 versions are specified for a ±7.0 mV input sensitivity over the 0° to 70°C temperature range, while the MC3431 and MC3433 are specified for ±12 mV.

- Propagation Delay Time: 40 ns
- Outputs Specified for a Fanout of 10 (MC7400 Type Loads)
- Specified for All Conditions of ±5% Power Supply Variations, Operating Temperature Range, Input Common Mode Voltage Swing from –3.0 V to 3.0 V, and $R_S \leq 200\ \Omega$.

L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS

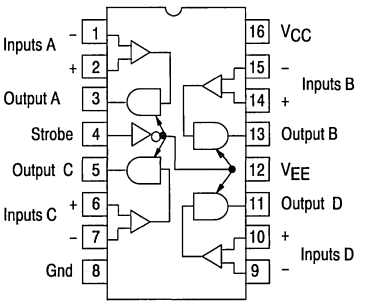
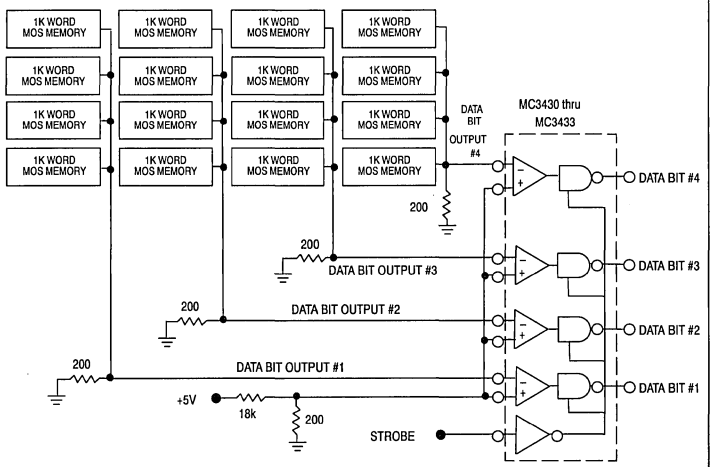


Figure 1. A Typical MOS Memory Sensing Application for a 4K Word by 4-Bit Memory Arrangement Employing 1103 Type Memory Devices



Only four devices are required for a 4k word by 4-bit memory system.

TRUTH TABLE

Input	Strobe	Output	Device
$V_{ID} \geq 7.0$ mV	L	H	MC3430
	H	Z	
$T_A = 0°$ to 70°C	L	Off	MC3432
	H	Off	
-7.0 mV $\leq V_{ID} \leq 7.0$ mV	L	I	MC3430
	H	Z	
$T_A = 0°$ to 70°C	L	I	MC3432
	H	Off	
$V_{ID} \leq -7.0$ mV	L	L	MC3430
	H	Z	
$T_A = 0°$ to 70°C	L	On	MC3432
	H	Off	
$V_{ID} \geq 12$ mV	L	H	MC3431
	H	Z	
$T_A = 0°$ to 70°C	L	Off	MC3433
	H	Off	
-12mV $\leq V_{ID} \leq +12$ mV	L	I	MC3431
	H	Z	
$T_A = 0°$ to 70°C	L	I	MC3433
	H	Off	
$V_{ID} \leq -12$ mV	L	L	MC3431
	H	Z	
$T_A = 0°$ to 70°C	L	On	MC3433
	H	Off	

L = Low Logic State Z = Third (High Impedance)
H = High Logic State I = Indeterminate State
$R_S \leq 200\ \Omega$

2

MAXIMUM RATINGS (T_A = 0° to +70°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±7.0	Vdc
Differential Mode Input Signal Voltage Range	V_{IDR}	±6.0	Vdc
Common Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Output Voltage (MC3432, MC3433)	V_O	±7.0	Vdc
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0° to +70°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	±4.75 –4.75	±5.0 –5.0	±5.25 –5.25	Vdc
Output Load Current	I_{OL}	—	—	16	mA
Differential Mode Input Voltage Range	V_{IDR}	–5.0	—	+5.0	Vdc
Common Mode Input Voltage Range	V_{ICR}	–3.0	—	+3.0	Vdc
Input Voltage Range (any input to Ground)	V_{IR}	–5.0	—	+3.0	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = –5.0 Vdc, T_A = 0° to +70°C, typical values are measured at T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	MC3430, MC3431 Min	MC3430, MC3431 Typ	MC3430, MC3431 Max	MC3432, MC3433 Min	MC3432, MC3433 Typ	MC3432, MC3433 Max	Unit
Input Sensitivity (See Discussion on Page 3) ($R_S \le 200\ \Omega$) (Common Mode Voltage Range = –3.0 V ≤ V_{in} ≤ 3.0 V) 4.75 ≤ V_{CC} ≤ 5.25 V, T_A = 25°C MC3430, MC3432 –4.75 ≥ V_{EE} ≥ –5.25 V, T_A = 25°C MC3431, MC3433 (Common Mode Voltage Range = –3.0 V ≤ V_{in} ≤ 3.0 V) 4.75 ≤ V_{CC} ≤ 5.25 V, T_A = 0° to 70°C MC3430, MC3432 –4.75 ≥ V_{EE} ≥ –5.25 V, T_A = 0° to 70°C MC3431, MC3433	V_{IS}	 — — — —	 — — — —	 ±6.0 ±10 ±7.0 ±12	 — — — —	 — — — —	 ±6.0 ±10 ±7.0 ±12	mV
Input Offset Voltage ($R_S \le 200\ \Omega$)	V_{IO}	—	2.0	—	—	2.0	—	mV
Input Bias Current (V_{CC} = 5.25 V, V_{EE} = –5.25 V) MC3430, MC3432 MC3431, MC3433	I_B	 — —	 20 20	 40 40	 — —	 20 20	 40 40	µA
Input Offset Current	I_{IO}	—	1.0	—	—	1.0	—	µA
Voltage Gain	A_{VOL}	—	1200	—	—	1200	—	V/V
Strobe Input Voltage (Low State)	$V_{IL(S)}$	—	—	0.8	—	—	0.8	V
Strobe Input Voltage (High State)	$V_{IH(S)}$	2.0	—	—	2.0	—	—	V
Strobe Current (Low State) (V_{CC} = 5.25 V, V_{EE} = –5.25 V, V_{in} = 0.4 V)	$I_{IL(S)}$	—	—	–1.6	—	—	–1.6	mA
Strobe Current (High State) (V_{CC} = 5.25 V, V_{EE} = –5.25 V, V_{in} = 2.4 V) (V_{CC} = 5.25 V, V_{EE} = –5.25 V, V_{in} = 5.25 V)	$I_{IH(S)}$	 — —	 — —	 40 1.0	 — —	 — —	 40 1.0	 µA mA
Output Voltage (High State) (I_O = –400 µA, V_{CC} = 4.75 V, V_{EE} = –4.75 V)	V_{OH}	2.4	—	—	—	—	—	V
Output Voltage (Low State) (I_O = 16 mA, V_{CC} = 4.75 V, V_{EE} = 4.75 V)	V_{OL}	—	—	0.4	—	—	0.4	V
Output Leakage Current (V_{CC} = 4.75 V, V_{EE} = –4.75 V, V_O = 5.25 V)	I_{CEX}	—	—	—	—	—	250	µA
Output Current Short Circuit (V_{CC} = 5.25 V, V_{EE} = –5.25 V)	I_{SC}	–18	—	–70	—	—	—	mA
Output Disable Leakage Current (V_{CC} = 5.25 V, V_{EE} = –5.25 V)	I_{off}	—	—	40	—	—	—	µA
High Logic Level Supply Currents (V_{CC} = 5.25 V, V_{EE} = –5.25 V)	I_{CC} I_{EE}	— —	+45 –17	+60 –30	— —	+45 –17	+60 –30	mA mA

A UNIQUE FUNCTIONAL PARAMETER FOR COMPARATORS

A unique approach is used in specifying the MC3430 to MC3433 quad comparators. Previously, comparators have been specified as linear devices with common operational amplifier type parameters such as voltage gain (A_{VOL}), input offset voltage (V_{IO}), input offset current (I_{IO}) and common mode rejection (CMR). This is true despite the fact that most comparators are seldom operated in their linear region because it is difficult to hold a high gain comparator in this narrow region. Comparators are normally used to "detect" when an unknown voltage level exceeds a given reference voltage.

The most desirable comparator parameter is what minimum differential input voltage is required at the comparator's input terminals to guarantee a given output logic state. This new and important parameter has been called input sensitivity (V_{IS}) and is analogous to the input threshold voltage specification on a core memory sense amplifier. The input sensitivity specification includes the effects of voltage gain, input offset voltage and input offset current and eliminates the need for specifying these three parameters.

In order to make this parameter as inclusive as possible on the MC3430 to MC3433 series quad comparators, the input sensitivity is specified within the following conditions:

Commercial temperature range: 0° to 70°C
Power supply variations: ±5% (all conditions)
Input source resistance: ≤ 200 Ω
Common mode voltage range: –3.0 V to +3.0 V

Note: Typical values have been included on the omitted parameters for applications where the offset voltages are externally nulled.

Voltage gain is defined as the ratio of the resulting ΔV_O to a change in the V_{IDR} using conditions at which the V_{IO} and I_{IO} are nulled. Thus, for worst case MTTL logic levels, the required output voltage change is 2.0 V [V_{OH}(min) — V_{OL}(max) = 2.4 V — 0.4 V]. If 2.0 mV are required at the input terminals to induce this change in logic state, the voltage gain would be 1000 V/V.

Gain, however, is not the only factor affecting the logic transition. Normally, input offset voltages, that are not externally nulled can add an appreciable error that drastically overshadows the comparator gain. Therefore, the 2.0 mV for example, required to cause the logic transition is often masked. An input offset voltage of up to 7.5 mV might be required to reach the linear region. A further consideration is the input offset current of up to ±10 μA flowing through the matched 200 Ω source resistors at the input terminals which can create an additional error of ±2.0 mV. In order to determine a worst case input sensitivity, it must be assumed that minimum specified gain and maximum specified offset voltage and current conditions exist. Also, it must be assumed that these three factors are cumulative, requiring a worst case input of:

Logic transition = 2.0 mV
V_{IO} = 7.5 mV
I_{IO} of ±10 μA thru 200 Ω resistor = 2.0 mV
Therefore, 2 +7.5 +2 = 11.5 mV.

The effects of power supply voltage variations, temperature changes and common mode input voltage conditions have not been considered, as they are not present in the gain and offset specifications on most comparators.

Thus, the input sensitivity specification greatly reduces the effort required in determining the worst case differential voltage required by a given comparator type.

Table I compares the worst case input sensitivity of three popular comparator types at both room temperature and over the specified commercial temperature range (0° to 70°C). This sensitivity was computed from the specified voltage gain, offset voltage and offset current limits.

Table 1. Worst Case Comparisons

Device	T_A = 25°C						T_A = 0° to 70°C					
	V_{IO} (mV) Max	A_{VOL}* V/V Typ	V_{ID} Required for 3.0 V Output Change	I_{IO} R_S = 200 Ω (μA) Max	Error Voltage Generated Into 200 Ω Source Resistors	Total Sensitivity (mV)	V_{IO} (mV) Max	A_{VOL}* V/V Typ	V_{ID} Required for 3.0 V Output Change	I_{IO} R_S = 200 Ω (μA) Max	Error Voltage Generated Into 200 Ω Source Resistors	Total Sensitivity (mV)
MC3430 MC3432	—	—	—	—	—	6.0	—	—	—	—	—	7.0
MC3431, MC3433	—	—	—	—	—	10	—	—	—	—	—	12
MC1711C	5.0	1500	2.0 mV	15	3.0 mV	10	5.0	1000	3.0 mV	25	5.0 mV	13
LM311	7.5	200 k	0.015 mV	6.0**	0.0012 mV	7.516	10	100 k	0.030 mV	70**	0.014 mV	10.04

* Typical values given, as minimum gain not always specified.

** I_{IO} measured in nA.

Figure 2. Guaranteed Output State versus Differential Input Voltage

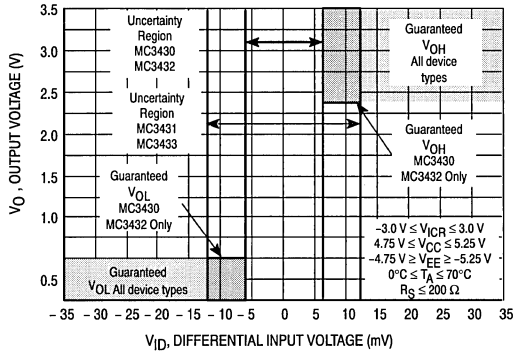
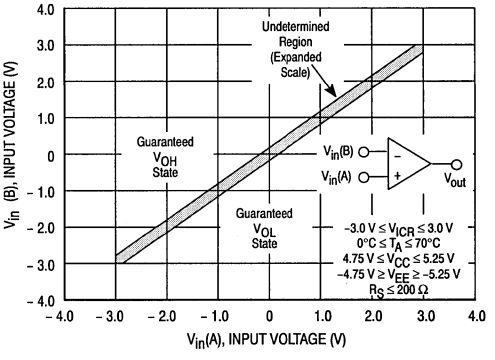


Figure 3. Guaranteed Output State versus Input Voltage

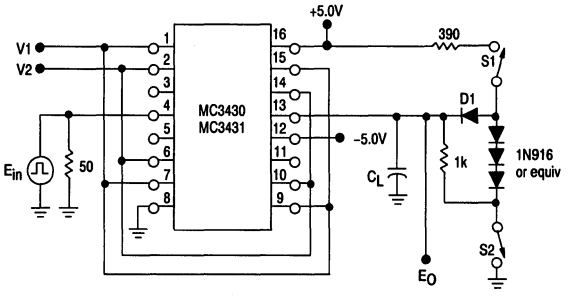


2

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = −5.0 Vdc, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Fig.	MC3430, MC3431			MC3432, MC3433			Unit
			Min	Typ	Max	Min	Typ	Max	
High to Low Logic Level Propagation Delay Time (Differential Inputs) 5.0 mV +V_{IS}	$t_{PHL(D)}$	6,8-11	—	20	45	—	27	50	ns
Low to High Logic Level Propagation Delay Time (Differential Inputs) 5.0 mV +V_{IS}	$t_{PLH(D)}$	6,8-11	—	33	55	—	40	65	ns
Open State to High Logic Level Propagation Delay Time (Strobe)	$t_{PZH(S)}$	4	—	—	35	—	—	—	ns
High Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PHZ(S)}$	4	—	—	35	—	—	—	ns
Open State to Low Logic Level Propagation Delay Time (Strobe)	$t_{PZL(S)}$	4	—	—	40	—	—	—	ns
Low Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PLZ(S)}$	4	—	—	35	—	—	—	ns
High Logic to Low Logic Level Propagation Delay Time (Strobe)	$t_{PHL(S)}$	5	—	—	—	—	—	40	ns
Low Logic to High Logic Level Propagation Delay Time (Strobe)	$t_{PLH(S)}$	5	—	—	—	—	—	35	ns

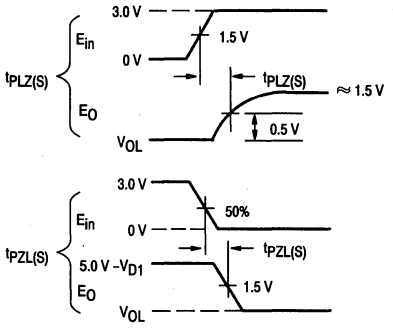
Figure 4. Strobe Propagation Delay Times $t_{PLZ(S)}$, $t_{PZL(S)}$, $t_{PHZ(S)}$, and $t_{PZH(S)}$



Output of Channel B shown under test, other channels are tested similarly.

	V1	V2	S1	S2	C_L
$t_{PLZ(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{PZL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHZ(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{PZH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{in} waveform characteristics.
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%



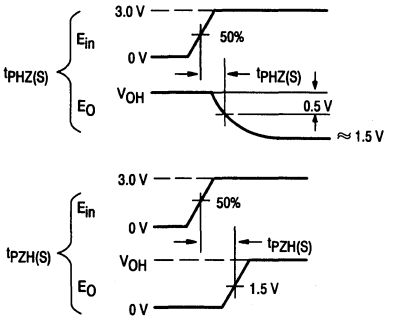
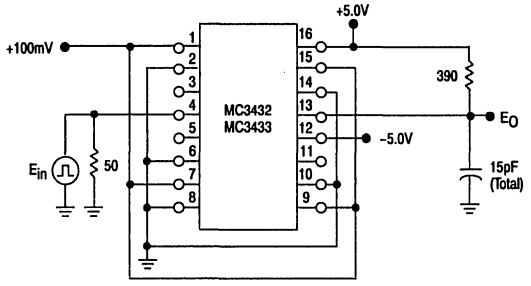
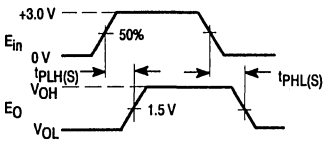


Figure 5. Strobe Propagation Delay $t_{PLH(S)}$ and $t_{PHL(S)}$

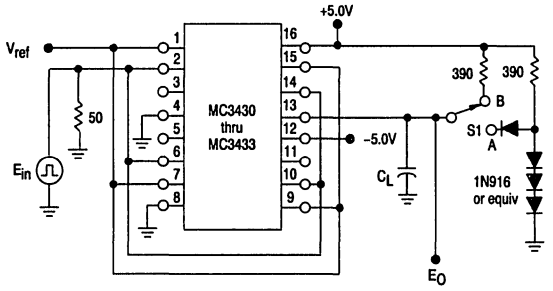


Output of Channel B shown under test, other channels are tested similarly.



E_{in} waveform characteristics.
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

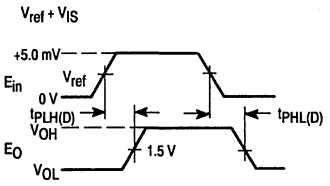
Figure 6. Differential Input Propagation Delay $t_{PLH(D)}$ and $t_{PHL(D)}$



Output of Channel B shown under test, other channels are tested similarly.

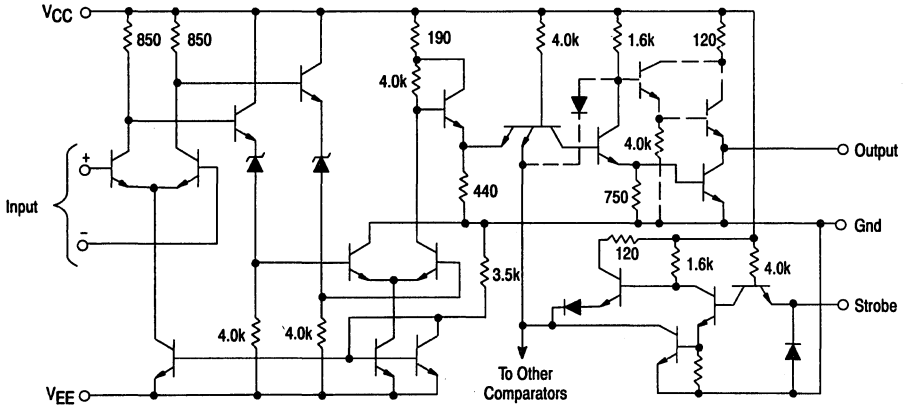
S1 at "A" for MC3430, MC3431
S1 at "B" for MC3432, MC3433
C_L = 50 pF total for MC3430, MC3431
C_L = 15 pF total for MC3432, MC3433

Device	V_{ref}
MC3430	11 mV
MC3431	15 mV
MC3432	11 mV
MC3433	15 mV



E_{in} waveform characteristics.
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

Figure 7. Circuit Schematic
(1/4 Circuit Shown)



Dashed components apply to the MC3430 and MC3431 circuits only.

Response Time versus Overdrive — MC3430, MC3431

Figure 8. Output Low-to-High

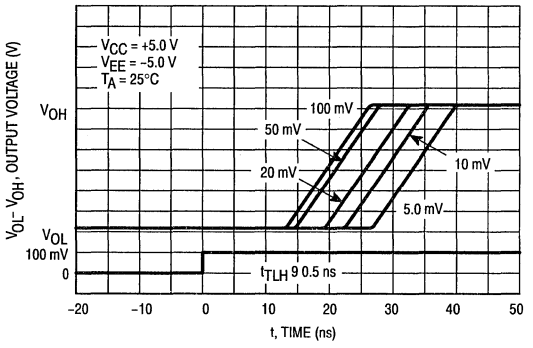
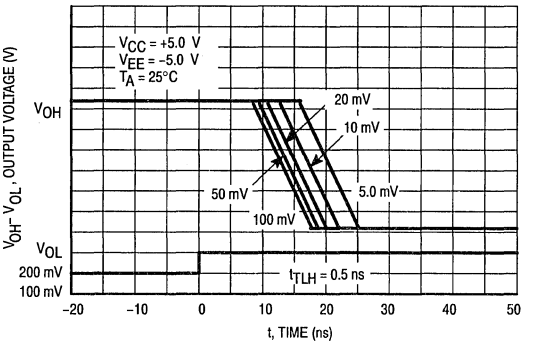


Figure 9. Output High-to-Low



Response Time versus Overdrive — MC3432, MC3433

Figure 10. Output Low-to-High

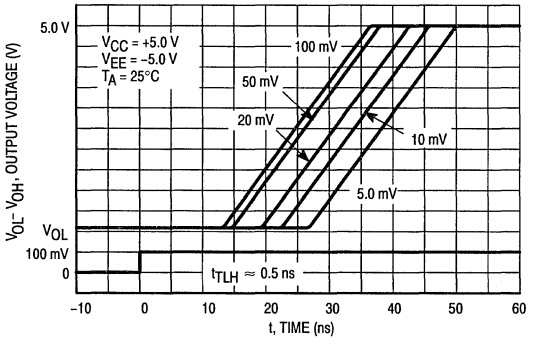


Figure 11. Output High-to-Low

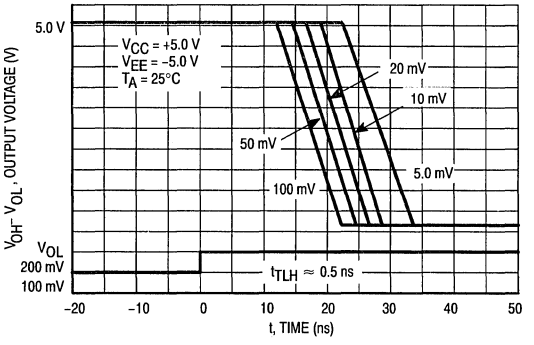


Figure 12. Average Input Offset Voltage versus Temperature

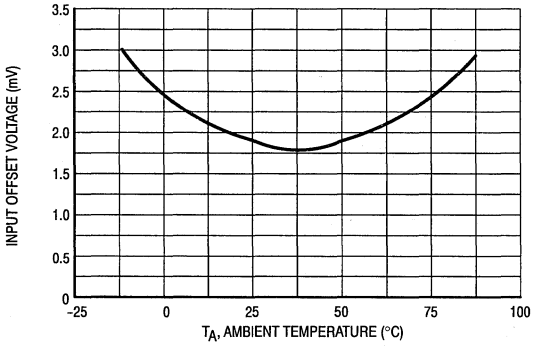


Figure 13. Response Time versus Temperature

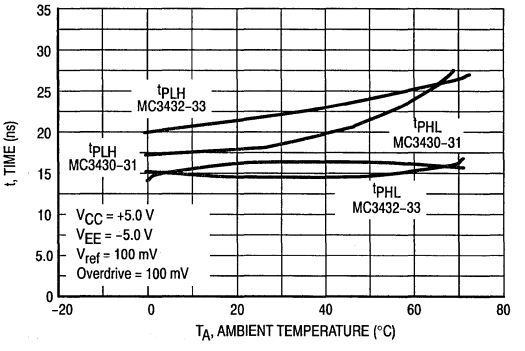
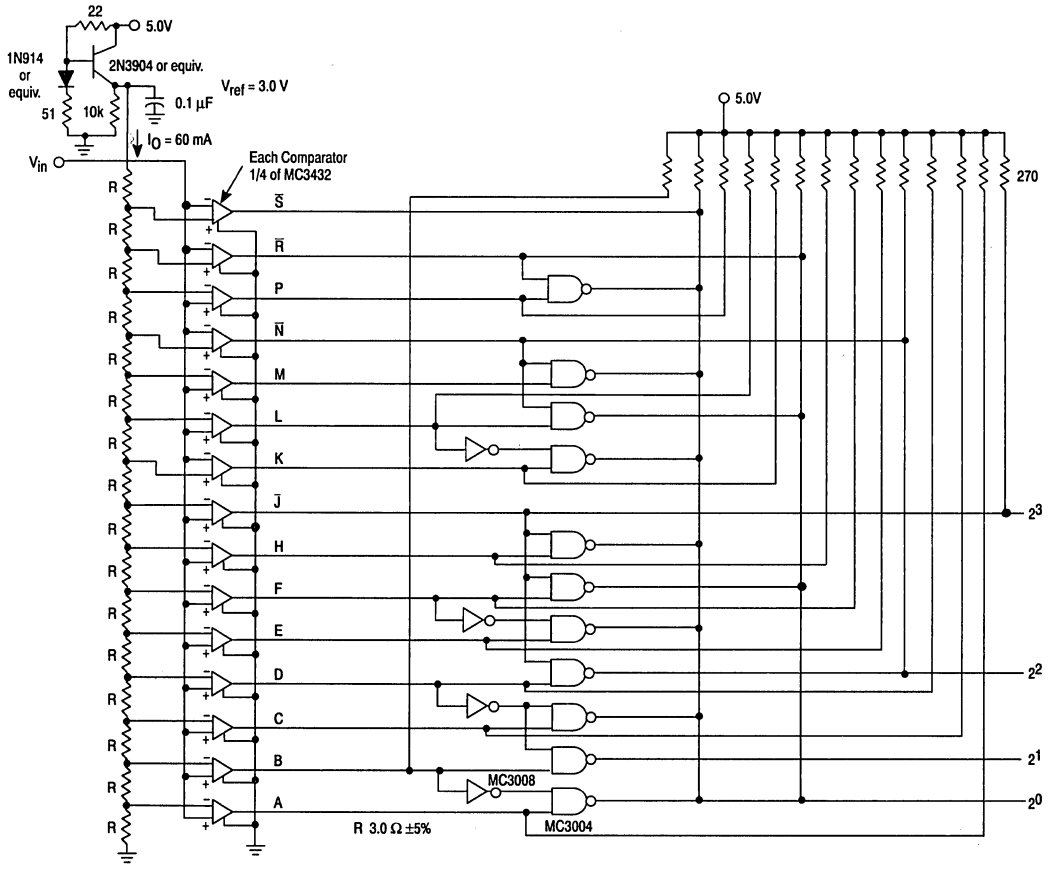


Figure 14. 4-Bit Parallel A/D Converter



$\overline{2^0} = (\overline{A}+B)(\overline{C}+D)(\overline{E}+F)(\overline{H}+J)(\overline{K}+L)(\overline{M}+N)(\overline{P}+R)(S)$

$\overline{2^1} = (\overline{B}+D)(\overline{F}+J)(\overline{L}+N)(\overline{R})$

$\overline{2^2} = (\overline{D}+J)(\overline{N})$

$\overline{2^3} = \overline{J}$

Conversion Time ≅ 50 ns

2

Figure 15. Level Detector with Hysteresis

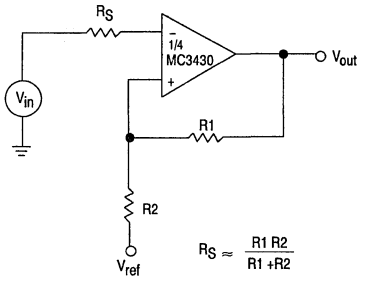
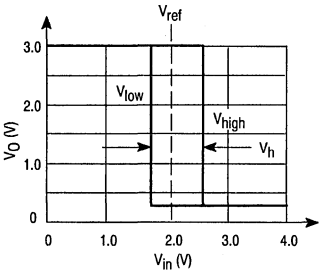


Figure 16. Transfer Characteristics and Equations for Figure 15



$$V_{high} = V_{ref} + \frac{R2\,[V_{O(max)} - V_{ref}]}{R1 + R2}$$

$$V_{low} = V_{ref} + \frac{R2\,[V_{O(min)} - V_{ref}]}{R1 + R2}$$

Hysteresis Loop (V_h):

$$V_h = V_{high} - V_{low} = \frac{R2}{R1 + R2}\,[V_{O(max)} - V_{O(min)}]$$

Figure 17. Double-Ended Limit Detector

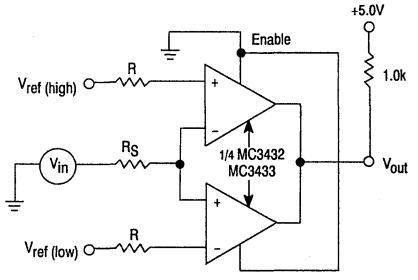
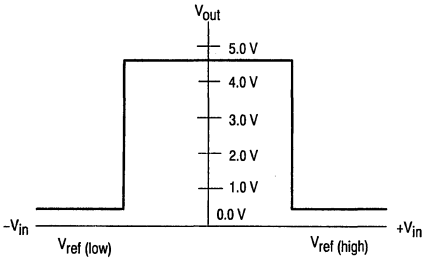


Figure 18. Voltage Transfer Function



MC3458
MC3558
MC3358

2

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

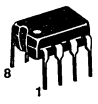
SILICON MONOLITHIC
INTEGRATED CIRCUIT

Dual, Low Power Operational Amplifiers

Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, 3) Single Supply or Split Supply operation and 4) pin outs compatible with the popular MC1558 dual operational amplifier. The MC3558 Series is equivalent to one-half of a MC3505.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 V or as high as 36 V with quiescent currents about one-fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 36 V
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Class AB Output Stage for Minimum Crossover Distortion
- Single and Split Supply Operations Available
- Similar Performance to the Popular MC1458/1558

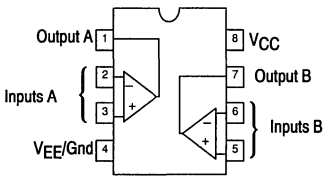


P1 SUFFIX
PLASTIC PACKAGE
CASE 626

U SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 36 ±18	Vdc
Input Differential Voltage Range (1)	V_{IDR}	±30	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	±15	Vdc
Junction Temperature Ceramic Package Plastice Package	T_J	 175 150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 –65 to +150 –55 to +125	°C
Operating Ambient Temperature Range MC3458 MC3558 MC3358	T_A	 0 to +70 –55 to +125 –40 to +85	°C

NOTES: 1. Split Power Supplies.
2. For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING INFORMATION

Device	Temperature Range	Package
MC3358P1	–40° to +85°C	Plastic DIP
MC3458D MC3458P1 MC3458U	0° to +70°C	SO-8 Plastic DIP Ceramic DIP
MC3558U	–55° to +125°C	Ceramic DIP

2

ELECTRICAL CHARACTERISTICS (For MC3558, MC3458, V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)
(For MC3358, V_{CC} = +14 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	MC3558			MC3458			MC3358			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $T_A = T_{high}$ to T_{low} (Note 1)	V_{IO}	— —	2.0 —	5.0 6.0	— —	2.0 —	10 12	— —	2.0 —	8.0 10	mV
Input Offset Current $T_A = T_{high}$ to T_{low}	I_{IO}	— —	30 —	50 200	— —	30 —	50 200	— —	30 —	75 250	nA
Large Signal Open-Loop Voltage Gain V_O = ±10 V, R_L = 2.0 kΩ, $T_A = T_{high}$ to T_{low}	A_{VOL}	 50 25	 200 300	 — —	 20 15	 200 —	 — —	 20 15	 200 —	 — —	V/mV
Input Bias Current $T_A = T_{high}$ to T_{low}	I_{IB}	— —	–200 –300	–500 –1500	— —	–200 —	–500 –800	— —	–200 —	–500 –1000	nA
Output Impedance f = 20 Hz	z_O	—	75	—	—	75	—	—	75	—	Ω
Input Impedance f = 20 Hz	z_I	0.3	1.0	—	0.3	1.0	—	0.3	1.0	—	MΩ
Output Voltage Range R_L = 10 kΩ R_L = 2.0 kΩ R_L = 2.0 kΩ, $T_A = T_{high}$ to T_{low}	V_{OR}	 ±12 ±10 ±10	 ±13.5 ±13 —	 — — —	 ±12 ±10 ±10	 ±13.5 ±13 —	 — — —	 12 10 10	 12.5 12 —	 — — —	V
Input Common Mode Voltage Range	V_{ICR}	+13 $-V_{EE}$	+13.5 $-V_{EE}$	—	+13 $-V_{EE}$	+13.5 $-V_{EE}$	—	+13 $-V_{EE}$	+13.5 $-V_{EE}$	—	V
Common Mode Rejection Ratio $R_S \leq 10$ kΩ	CMR	70	90	—	70	90	—	70	90	—	dB
Power Supply Current (V_O = 0) R_L = ∞	I_{CC}, I_{EE}	—	1.6	2.2	—	1.6	3.7	—	1.6	3.7	mA
Individual Output Short Circuit Current (Note 2)	I_{SC}	±10	±30	±45	±10	±20	±45	±10	±30	±45	mA
Positive Power Supply Rejection Ratio	PSRR+	—	30	150	—	30	150	—	30	150	μV/V
Negative Power Supply Rejection Ratio	PSRR–	—	30	150	—	30	150	—	—	—	μV/V
Average Temperature Coefficient of Input Offset Current $T_A = T_{high}$ to T_{low}	$\Delta I_{IO}/\Delta T$	—	50	—	—	50	—	—	50	—	pA/°C
Average Temperature Coefficient of Input Offset Current $T_A = T_{high}$ to T_{low}	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	—	10	—	μV/°C
Power Bandwidth A_V = 1, R_L = 2.0 kΩ, V_O = 20 V_{p-p}, THD = 5%	BWp	—	9.0	—	—	9.0	—	—	9.0	—	kHz
Small Signal Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 50 mV	BW	—	1.0	—	—	1.0	—	—	1.0	—	MHz
Slew Rate A_V = 1, V_I = –10 V to +10 V	SR	—	0.6	—	—	0.6	—	—	0.6	—	V/μs
Rise Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{TLH}	—	0.35	—	—	0.35	—	—	0.35	—	μs
Fall Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{THL}	—	0.35	—	—	0.35	—	—	0.35	—	μs
Overshoot A_V = 1, R_L = 10 kΩ, V_O = 50 mV	OS	—	20	—	—	20	—	—	20	—	%
Phase Margin A_V = 1, R_L = 2.0 kΩ, C_L = 200 pF	ϕm	—	60	—	—	60	—	—	60	—	Degrees
Crossover Distortion (V_{in} = 30 mVp-p, V_{out} = 2.0 Vp-p, f = 10 kHz)	—	—	1.0	—	—	1.0	—	—	1.0	—	%

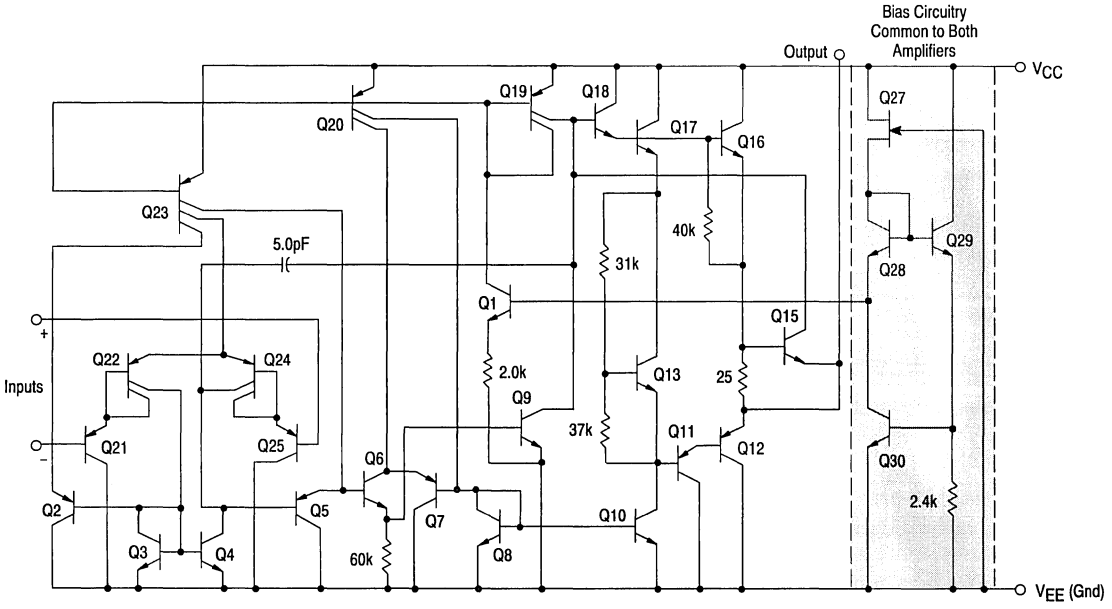
NOTES: 1. T_{high} = 125°C for MC3558, 70°C for MC3458, 85°C for MC3358 T_{low} = –55°C for MC3558, 0°C for MC3458, –40°C for MC3358
2. Not to exceed maximum package power dissipation.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

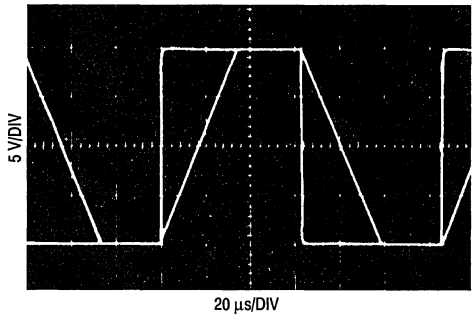
Characteristics	Symbol	MC3558			MC3458			MC3358			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	—	2.0	5.0	—	2.0	5.0	—	2.0	10	mV
Input Offset Current	I_{IO}	—	30	50	—	30	50	—	—	75	nA
Input Bias Current	I_{IB}	—	–200	–500	—	–200	–500	—	—	–500	nA
Large Signal Open-Loop Voltage Gain R_L = 2.0 kΩ,	A_{VOL}	20	200	—	20	200	—	20	200	—	V/mV
Power Supply Rejection Ratio	PSRR	—	—	150	—	—	150	—	—	150	μV/V
Output Voltage Range (Note 3) R_L = 10 kΩ, V_{CC} = 5.0 V R_L = 10 kΩ, 5.0 V ≤ V_{CC} ≤ 30 V	V_{OR}	 3.3 —	 3.5 V_{CC} –1.7	 — —	 3.3 —	 3.5 V_{CC} –1.7	 — —	 3.3 —	 3.5 V_{CC} –1.7	 — —	Vp-p
Power Supply Current	I_{CC}	—	2.5	4.0	—	2.5	7.0	—	2.5	4.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	CS	—	–120	—	—	–120	—	—	–120	—	dB

NOTES: 3. Output will swing to ground with a 10 kΩ pull down resistor.

Representative Circuit Schematic
(1/4 of Circuit Shown)



Inverter Pulse Response



CIRCUIT DESCRIPTION

The MC3558 Series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input Common Mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because Class AB operation is utilized.

Each amplifier is biased from an internal voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

2

Figure 1. Sine Wave Response

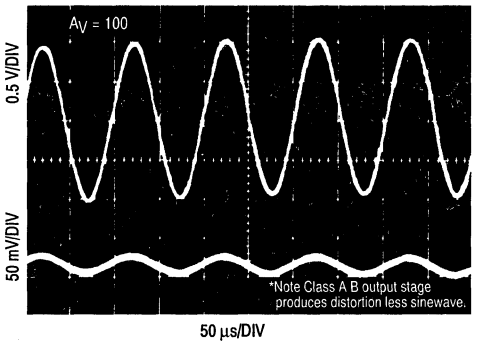


Figure 2. Open-Loop Frequency Response

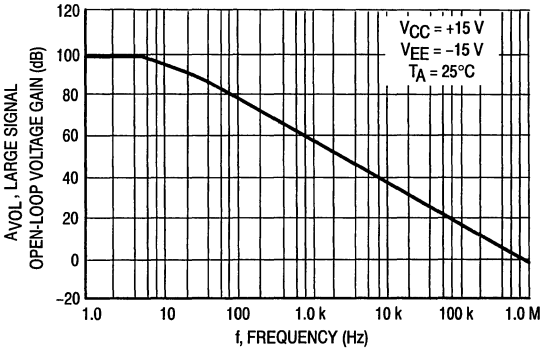


Figure 3. Power Bandwidth

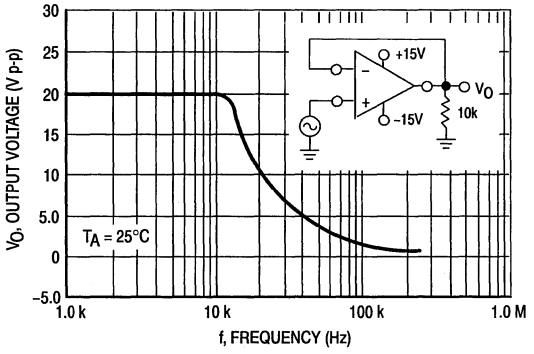


Figure 4. Output Swing versus Supply Voltage

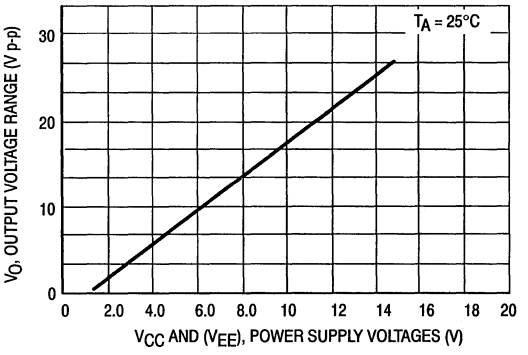


Figure 5. Input Bias Current versus Temperature

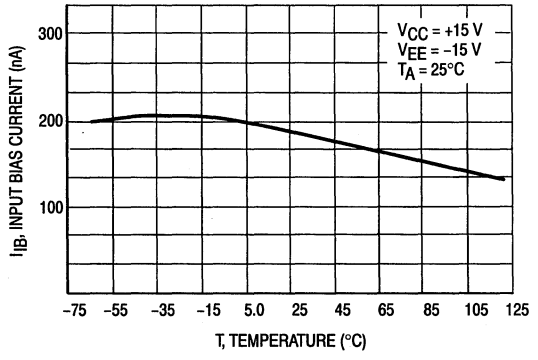


Figure 6. Input Bias Current versus Supply Voltage

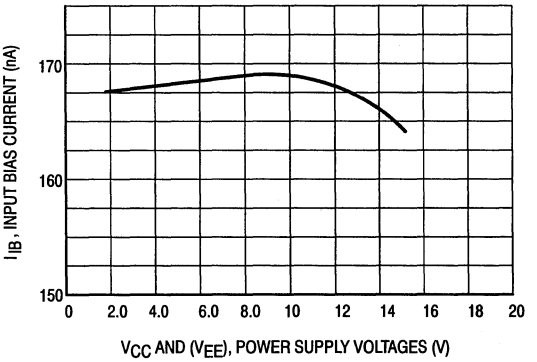


Figure 7. Voltage Reference

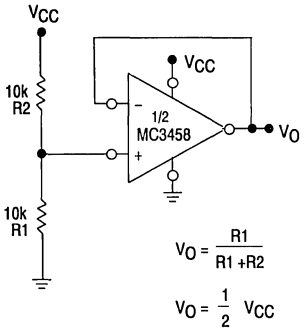


Figure 8. Wien Bridge Oscillator

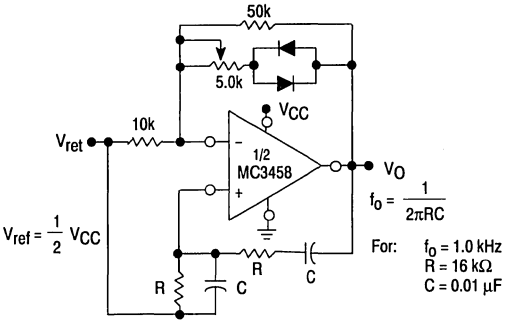


Figure 9. High Impedance Differential Amplifier

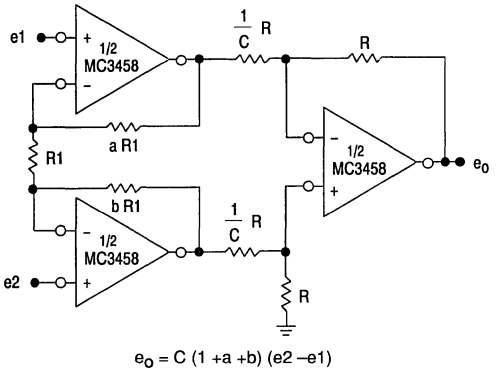


Figure 10. Comparator with Hysteresis

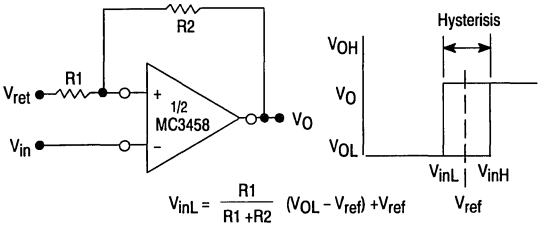


Figure 11. Bi-Quad Filter

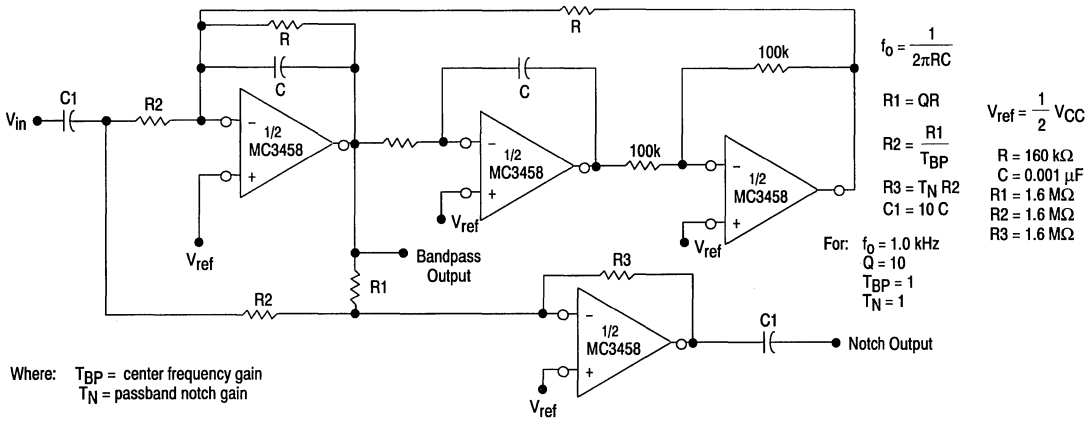
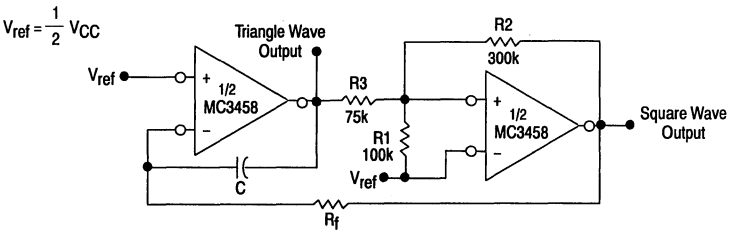
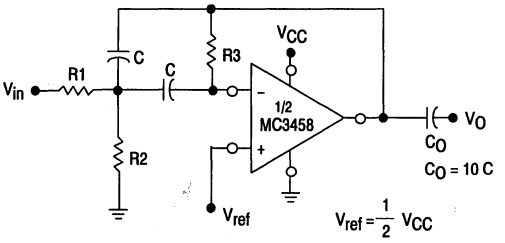


Figure 12. Function Generator



$$f = \frac{R1 + R_C}{4 C R_f R1} \quad \text{if,} \quad R3 = \frac{R2\ R1}{R2 + R1}$$

Figure 13. Multiple Feedback Bandpass Filter



Given: f_0 = center frequency

$A(f_0)$ = gain at center frequency

Choose value f_0, C.

Then: $R3 = \frac{Q}{\pi f_0 C}$ $\quad R1 = \frac{R3}{2 A(f_0)}$ $\quad R2 = \frac{R1\ R5}{4Q^2 R1 - R3}$

For less than 10% error from operational amplifier $\frac{Q_0 f_0}{BW} < 0.1$

where, f_0 and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

MC3476

2

Low Cost Programmable Operational Amplifier

The MC3476 is a low cost selection of the popular, industry standard MC1776 programmable operational amplifier. This extremely versatile operational amplifier features low power consumption and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current and power consumption despite wide variations in operating power supply voltages.

- ±6.0 V to ±18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short Circuit Protection

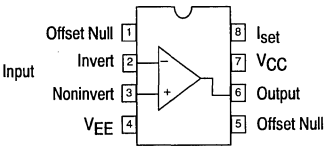
LOW COST PROGRAMMABLE OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

P1 SUFFIX
PLASTIC PACKAGE
CASE 626

U SUFFIX
CERAMIC PACKAGE
CASE 693

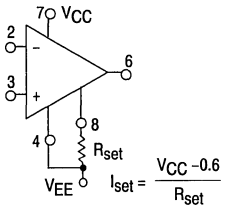
PIN CONNECTIONS



(Top View)

Resistive Programming
(See Figure 1)

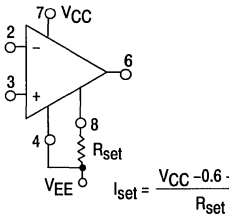
R_{set} to Ground



$$I_{set} = \frac{V_{CC} - 0.6}{R_{set}}$$

Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 µA	I_{set} = 15 µA
±6.0 V	3.6 MΩ	360 kΩ
±10 V	6.2 MΩ	620 kΩ
±12 V	7.5 MΩ	750 kΩ
±15 V	10 MΩ	1.0 MΩ

R_{set} to Negative Supply
(Recommended for supply voltage less than ±6.0 V)

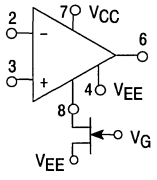


$$I_{set} = \frac{V_{CC} - 0.6 - V_{EE}}{R_{set}}$$

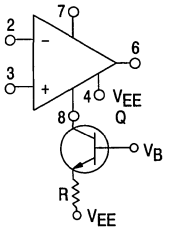
Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 µA	I_{set} = 15 µA
±1.5 V	1.6 MΩ	160 kΩ
±3.0 V	3.6 MΩ	360 kΩ
±6.0 V	7.5 MΩ	750 kΩ
±15 V	20 MΩ	2.0 MΩ

Active Programming

FET Current Source



Bipolar Current Source



Pins not shown are not connected.

ORDERING INFORMATION

Device	Temperature Range	Package
MC3476P1	0° to +70°C	Plastic DIP
MC3476U		Ceramic DIP

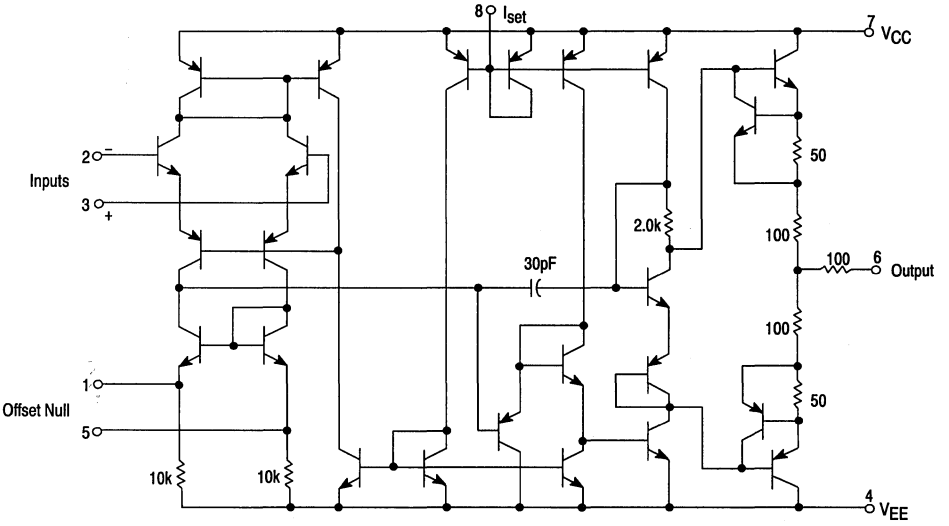
2

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

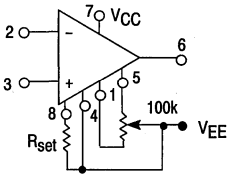
Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±18	Vdc
Input Differential Voltage Range	V_{IDR}	±30	Vdc
Input Common Mode Voltage Range	V_{ICR}	V_{CC}, V_{EE}	Vdc
Offset Null to V_{EE} Voltage	$V_{off} - V_{EE}$	±0.5	Vdc
Programming Current	I_{set}	200	μA
Programming Voltage (Voltage from I_{set} Terminal to Ground)	V_{set}	(V_{CC} – 0.6 V) to V_{CC}	Vdc
Output Short Circuit Duration (Note 1)	t_{SC}	Indefinite	sec
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range Metal and Ceramic Packages Plastic Package	T_{stg}	 – 65 to +150 – 55 ot +125	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

NOTE: 1. Short circuit to ground with $I_{set} \leq 15$ μA. Rating applies up to ambient temperature of +70°C.

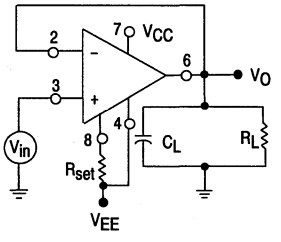
Equivalent Schematic Diagram



Voltage Offset Null Circuit



Transient Response Test Circuit



Pins not shown are not connected.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = – 15 V, I_{set} = 15 μA, T_A = +25°C, unless otherwise noted).

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset voltage ($R_S \le 10$ kΩ) T_A = +25°C 0°C ≤ T_A ≤ +70°C	V_{IO}	 — —	 2.0 —	 6.0 7.5	mV
Offset Voltage Adjustment Range	V_{IOR}	—	18	—	mV
Input Offset Current T_A = +25°C T_A = +70°C T_A = 0°C	I_{IO}	 — — —	 20 — —	 25 25 40	nA
Input Bias Current T_A = +25°C T_A = +70°C T_A = 0°C	I_{IB}	 — — —	 15 — —	 50 50 100	nA
Input Resistance	r_i	—	5.0	—	MΩ
Input Capacitance	C_i	—	2.0	—	pF
Input Common Mode Voltage Gain 0°C ≤ T_A ≤ +70°C	V_{ICR}	±10	—	—	V
Large Signal Voltage Gain $R_L \ge 10$ kΩ, V_O = ±10 V, T_A = +25°C $R_L \ge 10$ kΩ, V_O = ±10 V, 0°C ≤ T_A ≤ +70°C	A_{VOL}	 50 k 25 k	 400 k —	 — —	V/V
Output Voltage Range $R_L \ge 10$ kΩ, T_A = +25°C $R_L \ge 10$ kΩ, 0°C ≤ T_A ≤ +70°C	V_{OR}	 ±12 ±12	 ±13 —	 — —	V
Output Resistance	r_o	—	1.0	—	kΩ
Output Short Circuit Current	I_{SC}	—	12	—	mA
Common Mode Rejection $R_S \le 10$ kΩ, 0°C ≤ T_A ≤ +70°C	CMR	70	90	—	dB
Supply Voltage Rejection Ratio $R_S \le 10$ kΩ, 0°C ≤ T_A ≤ +70°C	PSRR	—	25	200	μV/V
Supply Current T_A = +25°C 0°C ≤ T_A ≤ +70°C	I_{CC}, I_{EE}	 — —	 160 —	 200 225	μA
Power Dissipation T_A = +25°C 0°C ≤ T_A ≤ +70°C	P_D	 — —	 4.8 —	 6.0 6.75	mW
Transient Response (Unity Gain) V_{in} = 20 mV, $R_L \ge 10$ kΩ, C_L = 100 pF Rise Time Overshoot	 t_{TLH} OS	 — —	 0.35 10	 — —	 μs %
Slew Rate ($R_L \ge 10$ kΩ)	SR	—	0.8	—	V/μs

Figure 1. Set Current versus Set Resistor

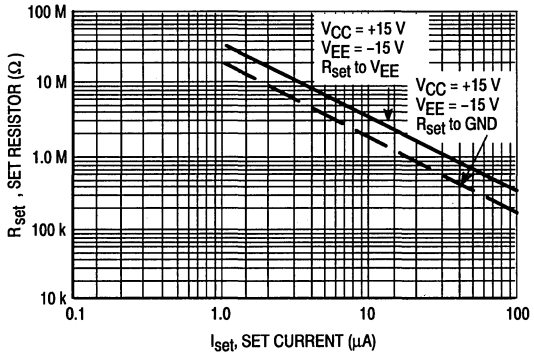


Figure 2. Positive Standby Supply Current versus Set Current

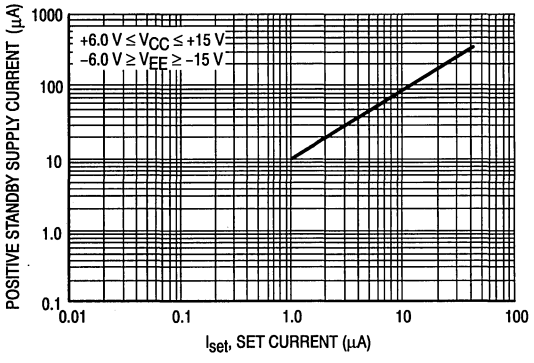


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Figure 3. Open-Loop versus Set Current

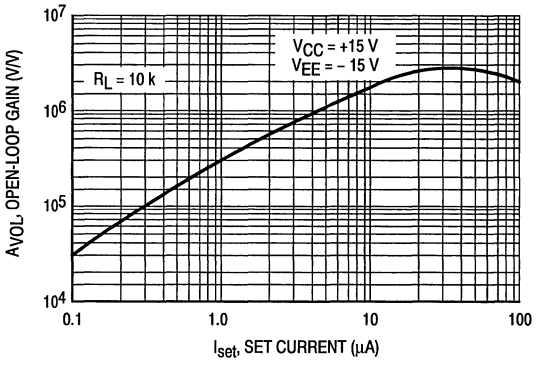


Figure 4. Input Bias Current versus Set Current

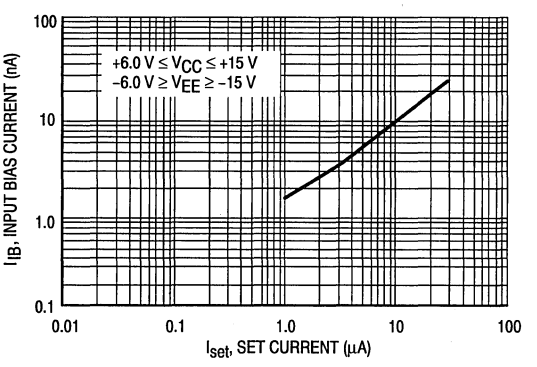


Figure 5. Slew Rate versus Set Current

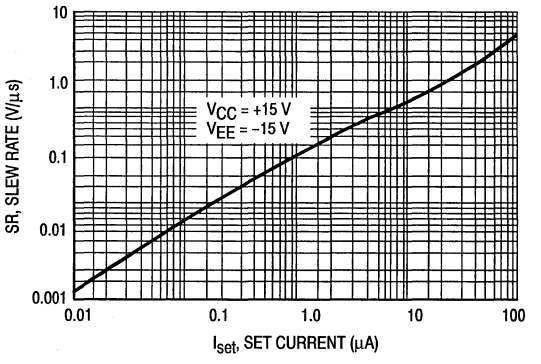


Figure 6. Gain Bandwidth Product versus Set Current

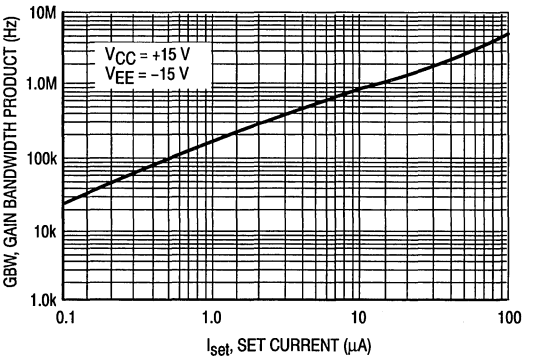


Figure 7. Output Voltage Swing versus Load Resistance

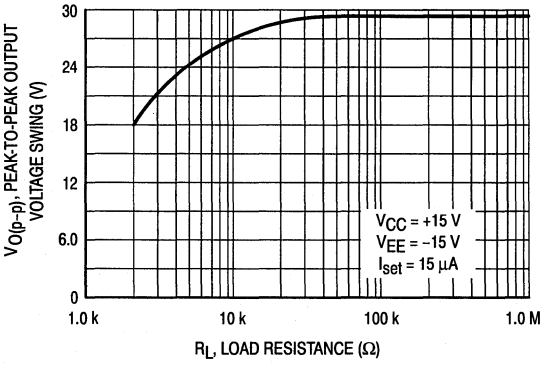
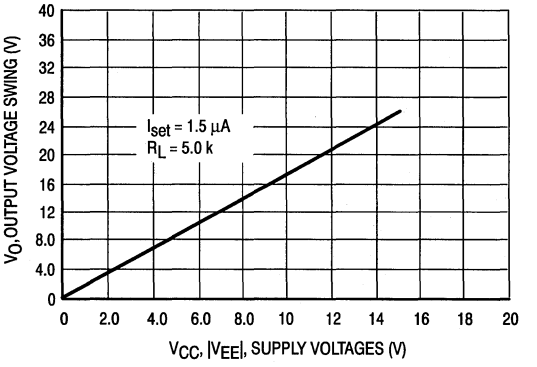


Figure 8. Output Voltage Swing versus Supply Voltage



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC4558, MC4558AC MC4558C

DUAL WIDE BANDWIDTH OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

Dual Wide Bandwidth Operational Amplifier

The MC4558, AC, and C combine all the outstanding features of the MC1458 and, in addition, possess three times the unity gain bandwidth of the industry standard.

- 2.5 MHz Unity Gain Bandwidth Guaranteed (MC4558 and MC4558AC)
- 2.0 MHz Unity Gain Bandwidth Guaranteed (MC4558C)
- Internally Compensated
- Short Circuit Protection
- Gain and Phase Match between Amplifiers
- Low Power Consumption

P1 SUFFIX
PLASTIC PACKAGE
CASE 626

U SUFFIX
CERAMIC PACKAGE
CASE 693

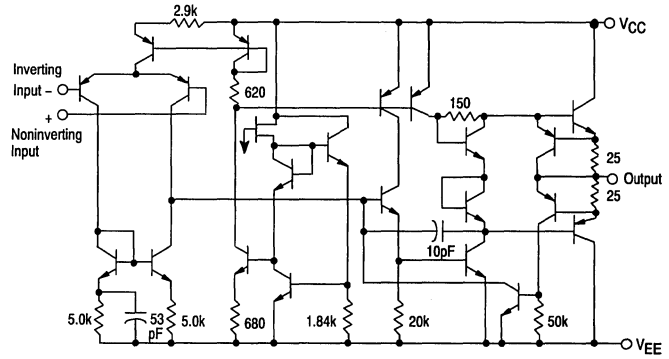
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

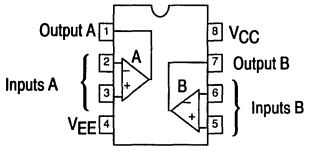
Rating	Symbol	MC4558 MC4558AC	MC4558C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 –22	+18 –18	Vdc
Input Differential Voltage	V_{ID}	±30		V
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous		
Ambient Temperature Range	T_A	–55 to +125 0 to +70		
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 –65 to +150 –55 to +125		°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150		°C

NOTES: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage
2. Short circuit may be to ground or either supply.

Equivalent Circuit Schematic
(1/2 of Circuit Shown)



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC4558U	–55° to +125°C	Ceramic DIP
MC4558CD	0° to +70°C	SO-8
MC4558ACP1, CP1		Plastic DIP
MC4558CU		Ceramic DIP

2

FREQUENCY CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C)

Characteristics	Symbol	MC4558, MC4558AC			MC4558C			Unit
		Min	Typ	Max	Min	Typ	Max	
Unity Gain Bandwidth	BW	2.5	2.8	—	2.0	2.8	—	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Input Offset Voltage ($R_S \le 10$ kΩ)	V_{IO}	—	1.0	5.0	—	2.0	6.0	mV
Input Offset Current	I_{IO}	—	20	200	—	20	200	nA
Input Bias Current (Note 1)	I_{IB}	—	80	500	—	80	500	nA
Input Resistance	r_i	0.3	2.0	—	0.3	2.0	—	MΩ
Input Capacitance	C_i	—	1.4	—	—	1.4	—	pF
Common Mode Input Voltage Range	V_{ICR}	±12	±13	—	±12	±13	—	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}	50	200	—	20	200	—	V/mV
Output Resistance	r_o	—	75	—	—	75	—	Ω
Common Mode Rejection ($R_S \le 10$ kΩ)	CMR	70	90	—	70	90	—	dB
Supply Voltage Rejection Ratio ($R_S \le 10$ kΩ)	PSRR	—	30	150	—	30	150	μV/V
Output Voltage Swing	V_O							V
($R_L \ge 10$ kΩ)		±12	±14	—	±12	±14	—	
($R_L \ge 2.0$ kΩ)		±10	±13	—	±10	±13	—	
Output Short Circuit Current	I_{SC}	10	20	40	10	20	40	mA
Supply Currents (Both Amplifiers)	I_D	—	2.3	5.0	—	2.3	5.6	mA
Power Consumption (Both Amplifiers)	P_C	—	70	150	—	70	170	mW
Transient Response (Unity Gain)								
(V_I = 20 mV, $R_L \ge 2.0$ kΩ, $C_L \le 100$ pF) Rise Time	t_{TLH}	—	0.3	—	—	0.3	—	μs
(V_I = 20 mV, $R_L \ge 2.0$ kΩ, $C_L \le 100$ pF) Overshoot	os	—	15	—	—	15	—	%
(V_I = 10 V, $R_L \ge 2.0$ kΩ, $C_L \le 100$ pF) Slew Rate	SR	1.5	1.6	—	1.0	1.6	—	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{high} to T_{low}, unless otherwise noted. See Note 2.)

Input Offset Voltage ($R_S \le 10$ kΩ)	V_{IO}	—	1.0	6.0	—	—	7.5	mV
Input Offset Current	I_{IO}							nA
(T_A = T_{high})		—	7.0	200	—	—	—	
(T_A = T_{low})		—	85	500	—	—	—	
(T_A = 0° to +70°C)		—	—	—	—	—	300	
Input Bias Current	I_{IB}							nA
(T_A = T_{high})		—	30	500	—	—	—	
(T_A = T_{low})		—	300	1500	—	—	—	
(T_A = 0° to +70°C)		—	—	—	—	—	800	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	—	—	—	—	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}	25	—	—	15	—	—	V/mV
Common Mode Rejection ($R_S \le 10$ kΩ)	CMR	70	90	—	—	—	—	dB
Supply Voltage Rejection Ratio ($R_S \le 10$ kΩ)	PSRR	—	30	150	—	—	—	μV/V
Output Voltage Swing	V_O							V
($R_L \ge 10$ kΩ)		±12	±14	—	±12	±14	—	
($R_L \ge 2.0$ kΩ)		±10	±13	—	±10	±13	—	
Supply Currents (Both Amplifiers)	I_D							mA
(T_A = T_{high})		—	—	4.5	—	—	5.0	
(T_A = T_{low})		—	—	6.0	—	—	6.7	
Power Consumption (Both Amplifiers)	P_C							mW
(T_A = T_{high})		—	—	135	—	—	150	
(T_A = T_{low})		—	—	180	—	—	200	

NOTES: 1. I_{IB} is out of the amplifier due to PNP input transistors.

2. T_{high} = +125°C for MC4558 T_{low} = −55°C for MC4558
= +70°C for MC4558C and MC4558AC = 0°C for MC4558C and MC4558AC.

Figure 1. Burst Noise versus Source Resistance

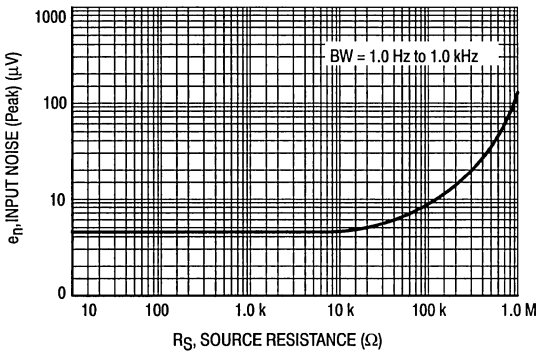


Figure 2. RMS Noise versus Source Resistance

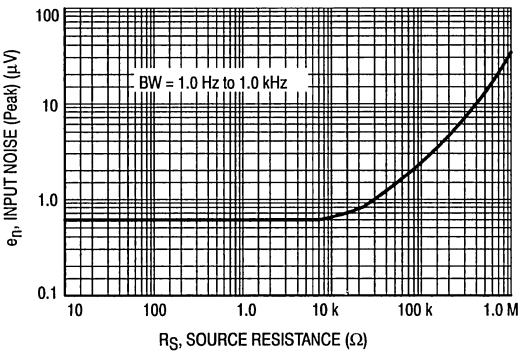


Figure 3. Output Noise versus Source Resistance

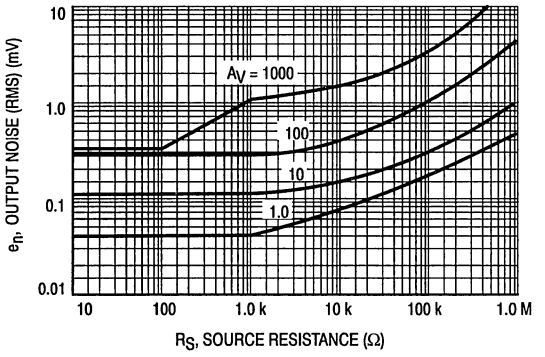


Figure 4. Spectral Noise Density

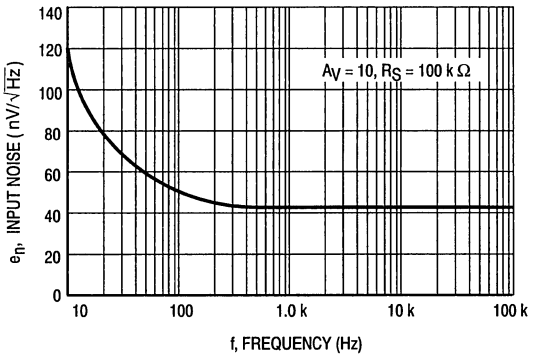
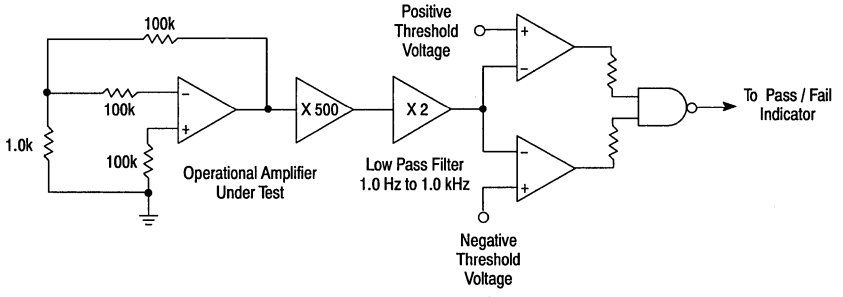


Figure 5. Burst Noise Test Circuit



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 sec and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed-loop gain factor of the operational amplifier.

2

Figure 6. Open-Loop Frequency Response

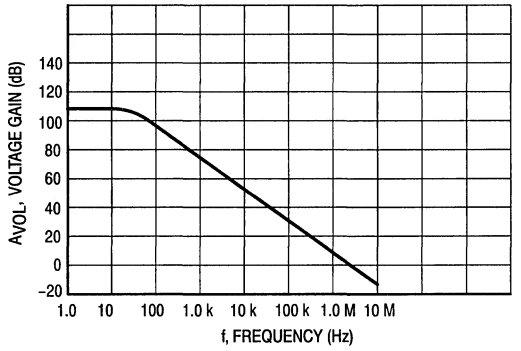


Figure 7. Phase Margin versus Frequency

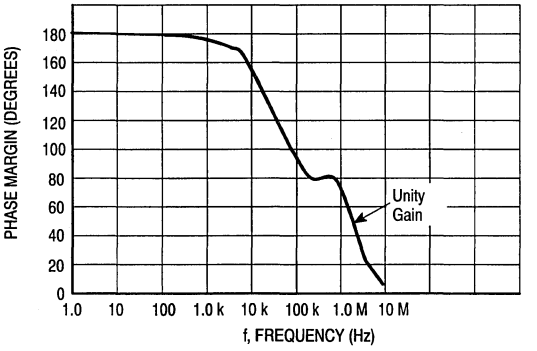


Figure 8. Positive Output Voltage Swing versus Load Resistance

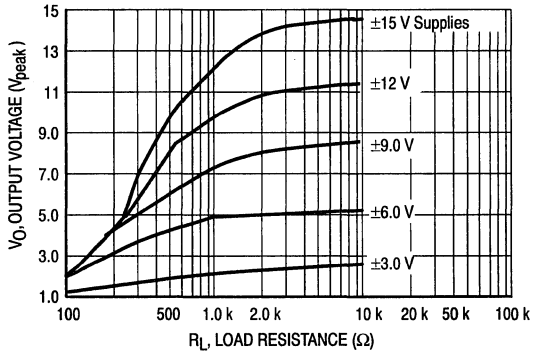


Figure 9. Negative Output Voltage Swing versus Load Resistance

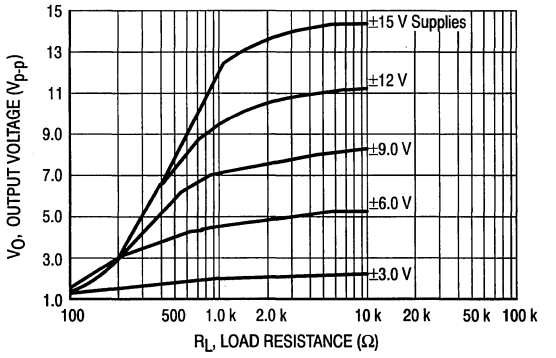


Figure 10. Power Bandwidth
(Large Signal Swing versus Frequency)

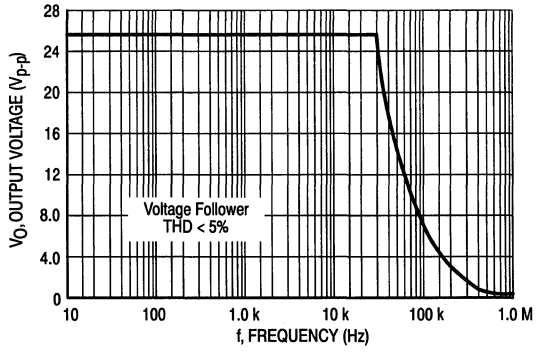
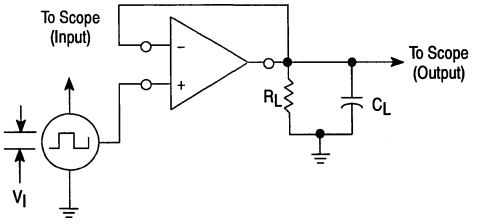


Figure 11. Transient Response Test Circuit



MC4741
MC4741C

(QUAD MC1741)
DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

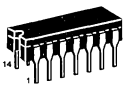
SILICON MONOLITHIC INTEGRATED CIRCUIT

(Quad MC1741)
Operational Amplifiers

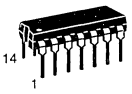
The MC4741,C is a true quad MC1741. Integrated on a single monolithic chip are four independent, low power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance.

The MC4741,C can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

- Each Amplifier is Functionally Equivalent to the MC1741
- Class AB Output Stage Eliminates Crossover Distortion
- True Differential Inputs
- Internally Frequency Compensated
- Short Circuit Protection
- Low Power Supply Current (0.6 mA/Amplifier)



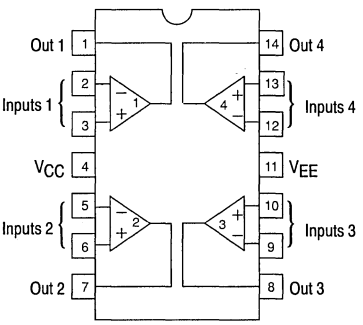
L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

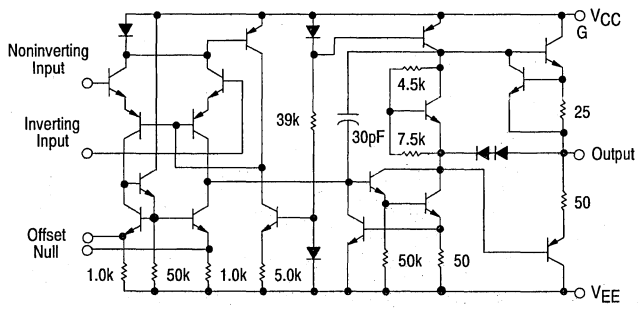
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Top View)

EQUIVALENT CIRCUIT SCHEMATIC
(1/4 of Circuit Shown)



ORDERING INFORMATION

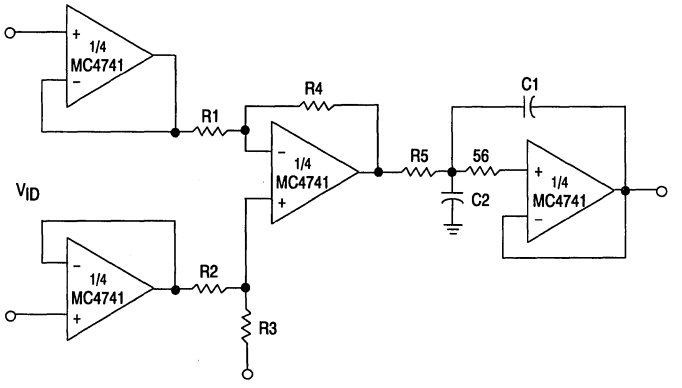
Device	Temperature Range	Package
MC4741L	–55° to +125°C	Ceramic DIP
MC4741CD MC4741CL MC4741CP	0° to +70°C	SO-14 Ceramic DIP Plastic DIP

2

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	MC4741	MC4741C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 −22	+18 −18	Vdc
Input Differential Voltage	V_{ID}	±44	±36	V
Input Common Mode Voltage	V_{ICM}	±22	±18	V
Output Short Circuit Duration	t_{SC}	Continuous		
Operating Ambient Temperature Range	T_A	−55 to +125	0 to +70	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 −65 to +150 −55 to +125		°C
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150		°C

High Impedance Instrumentation Buffer/Filter



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	MC4741			MC4741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ k)	V_{IO}	—	1.0	5.0	—	2.0	6.0	mV
Input Offset Current	I_{IO}	—	20	200	—	20	200	nA
Input Bias Current	I_{IB}	—	80	500	—	80	500	nA
Input Resistance	r_i	0.3	2.0	—	0.3	2.0	—	MΩ
Input Capacitance	C_i	—	1.4	—	—	1.4	—	pF
Offset Voltage Adjustment Range	V_{IOR}	—	±15	—	—	±15	—	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	—	±12	±13	—	V
Large Signal Voltage Gain (V_O = ±10 V, $R_L \geq 2.0$ k)	A_V	50	200	—	20	200	—	V/mV
Output Resistance	r_o	—	75	—	—	75	—	Ω
Common Mode Rejection ($R_S \leq 10$ k)	CMR	70	90	—	70	90	—	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	—	30	150	—	30	150	μV/V
Output Voltage Swing	V_O							V
($R_L \geq 10$ k)		±12	±14	—	±12	±14	—	
($R_L \geq 2$ k)		±10	±13	—	±10	±13	—	
Output Short Circuit Current	I_{SC}	—	20	—	—	20	—	mA
Supply Current — (All Amplifiers)	I_D	—	2.4	4.0	—	3.5	7.0	mA
Power Consumption (All Amplifiers)	P_C	—	72	120	—	105	210	mW
Transient Response (Unity Gain — Non-Inverting)								
(V_I = 20 mV, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Rise Time	t_{TLH}	—	0.3	—	—	0.3	—	μs
(V_I = 20 mV, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Overshoot	os	—	15	—	—	15	—	%
(V_I = 10 V, $R_L \geq 2$ kΩ, $C_L \leq 100$ pF) Slew Rate	SR	—	0.5	—	—	0.5	—	V/μs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = * T_{high} to T_{low}, unless otherwise noted.)

Characteristics	Symbol	MC4741			MC4741C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}	—	1.0	6.0	—	—	7.5	mV
Input Offset Current	I_{IO}							nA
(T_A = 125°C)		—	7.0	200	—	—	—	
(T_A = –55°C)		—	85	500	—	—	—	
(T_A = 0° to + 70°C)		—	—	—	—	—	300	
Input Bias Current	I_{IB}							nA
(T_A = 125°C)		—	30	500	—	—	—	
(T_A = –55°C)		—	300	1500	—	—	—	
(T_A = 0° to + 70°C)		—	—	—	—	—	800	
Common Mode Input Voltage Range	V_{ICR}	±12	±13	—	—	—	—	V
Large Signal Voltage Gain ($R_L \geq 2$k, V_{OUT} = ±10 V)	A_V	25	—	—	15	—	—	V/mV
Common Mode Rejection ($R_S \leq 10$ k)	CMR	70	90	—	—	—	—	dB
Supply Voltage Rejection Ratio ($R_S \leq 10$ k)	PSRR	—	30	150	—	—	—	μV/V
Output Voltage Swing	V_O							V
($R_L \geq 10$ k)		±12	±14	—	—	—	—	
($R_L \geq 2$ k)		±10	±13	—	±10	±13	—	
Supply Currents — (All Amplifiers)	I_D							mA
(T_A = 125°C)		—	2.4	3.4	—	—	—	
(T_A = –55°C)		—	3.6	5.0	—	—	—	
Power Consumption (T_A = +125°C)	P_C	—	72	102	—	—	—	mW
(T_A = –55°C)		—	108	150	—	—	—	

* T_{high} = 125°C for MC4741 and 70°C for MC4741C.
T_{low} = –55°C for MC4741 and 0°C for MC4741C.

2

Figure 1. Power Bandwidth (Large Signal Swing versus Frequency)

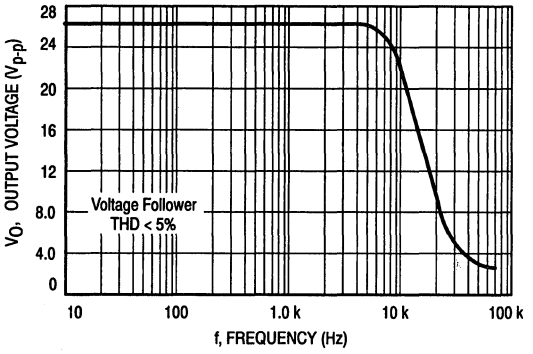


Figure 2. Open-Loop Frequency Response

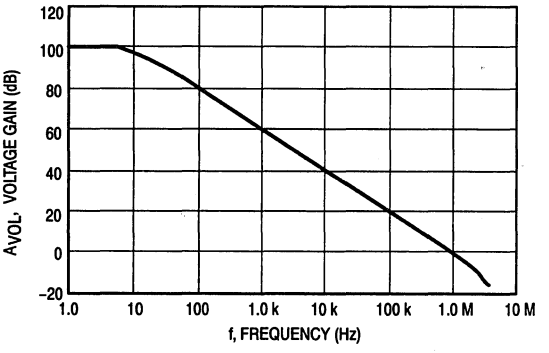


Figure 3. Positive Output Voltage Swing versus Load Resistance

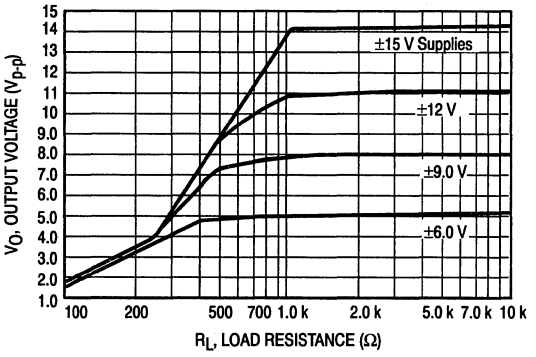


Figure 4. Negative Output Voltage Swing versus Load Resistance

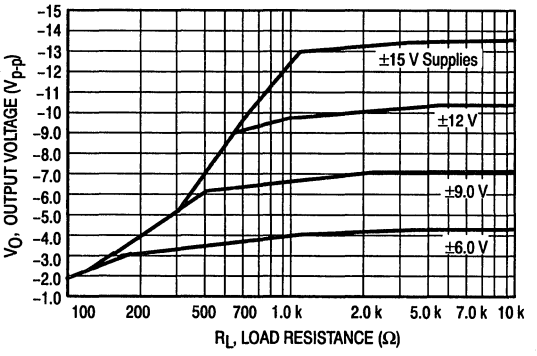


Figure 5. Output Voltage Swing versus Load Resistance (Single Supply Operation)

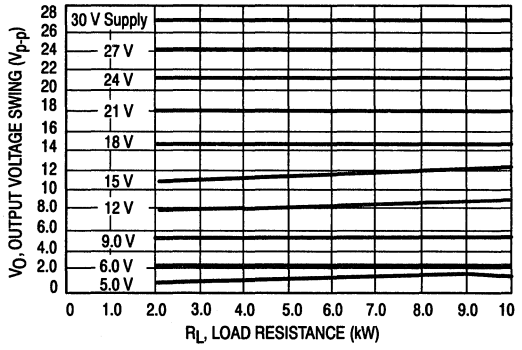


Figure 6. Noninverting Pulse Response

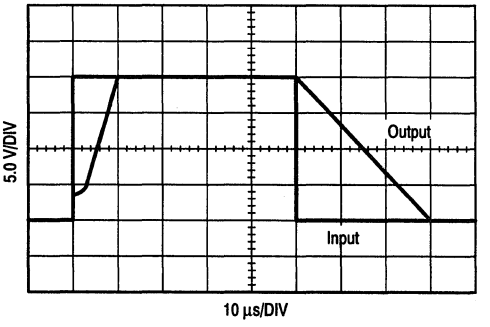


Figure 7. Bi-Quad Filter

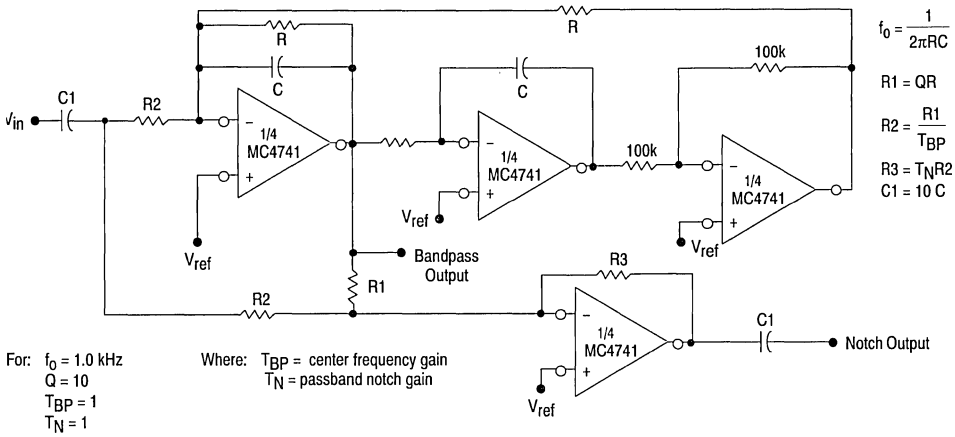


Figure 8. Open-Loop Voltage Gain versus Supply Voltage

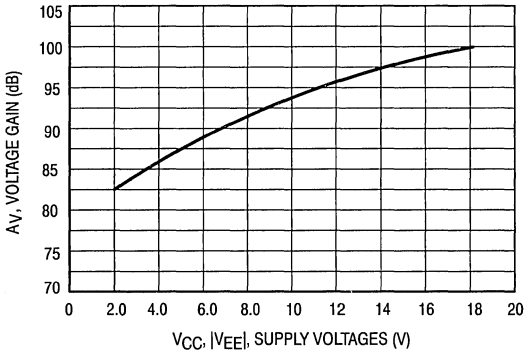


Figure 9. Transient Response Test Circuit

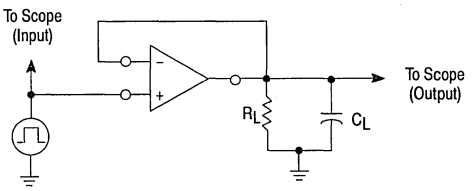
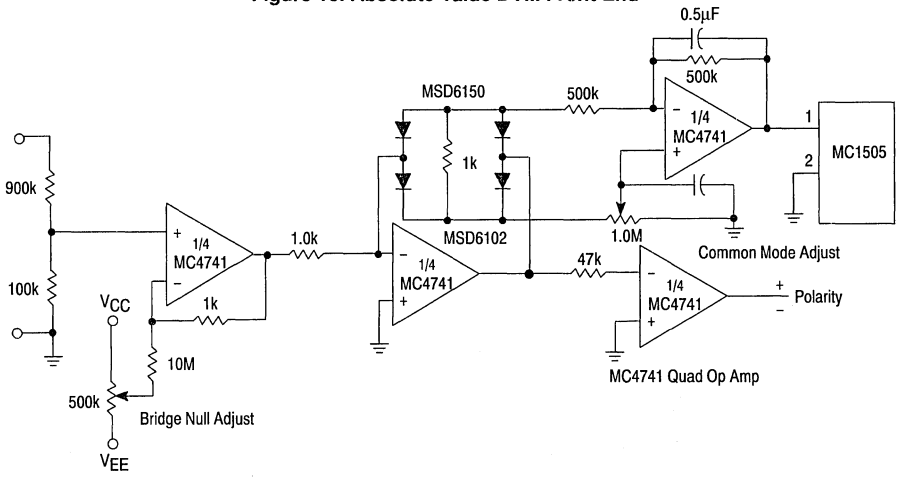


Figure 10. Absolute Value DVM Front End



MC33076

DUAL HIGH OUTPUT CURRENT OPERATIONAL AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

Advance Information

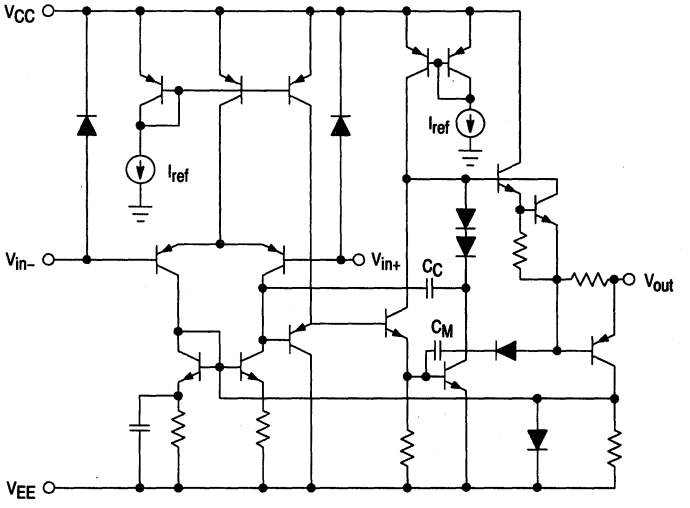
Dual High Output Current Low Power, Low Noise Bipolar Operational Amplifier

The MC33076 operational amplifier employs bipolar technology with innovative high performance concepts for audio and industrial applications. This device uses high frequency PNP input transistors to improve frequency response. In addition, the amplifier provides high output current drive capability while minimizing the drain current. The all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source and sink AC frequency performance.

The MC33076 is tested over the automotive temperature range and is available in an 8 pin SOIC package (D suffix) and in both the standard 8 pin DIP and 16 pin DIP packages for high power applications.

- 100 Ω Output Drive Capability
- Large Output Voltage Swing
- Low Total Harmonic Distortion
- High Gain Bandwidth: 7.4 MHz
- High Slew Rate: 2.6 V/μs
- Dual Supply Operation: ±2.0 V to ±18 V
- High Output Current: ISC = 250 mA typ
- Similar Performance to MC33178

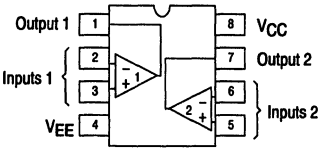
Equivalent Circuit Schematic
(Each Amplifier)



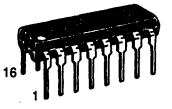
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626

PIN CONNECTIONS

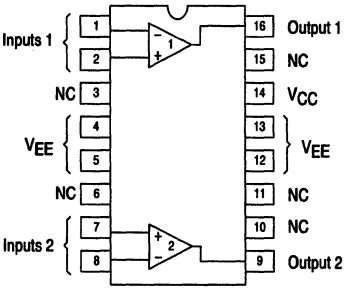


(8 Pin Pkg, Top View)



P2 SUFFIX
PLASTIC PACKAGE
CASE 648C
DIP (12+2+2)

PIN CONNECTIONS



(16 Pin Pkg, Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC33076D	−40° to 85°C	SO-8
MC33076P1		Plastic DIP
MC33076P2		Power Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Note 2)	V_{CC} to V_{EE}	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	5.0	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. **Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded** (see power dissipation performance characteristic, Figure 1. See applications section for further information.

DC ELECTRICAL CHARACTERICISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V) (V_S = ±2.5 V to ±15 V) T_A = +25°C T_A = –40° to +85°C	2	$\lvert V_{IO} \rvert$	 — —	 0.5 0.5	 4.0 5.0	mV
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω, V_{CM} = 0 V) T_A = –40° to +85°C		$\Delta V_{IO}/\Delta T$	 —	 2.0	 —	μV/°C
Input Bias Current (V_{CM} = 0 V) T_A = +25°C T_A = –40° to +85°C	3, 4	I_{IB}	 — —	 100 —	 500 600	nA
Input Offset Current (V_{CM} = 0 V) T_A = +25°C T_A = –40° to +85°C		$\lvert I_{IO} \rvert$	 — —	 5.0 —	 70 100	nA
Common Mode Input Voltage Range	5	V_{ICR}	–13	–14 +14	 13	V
Large Signal Voltage Gain (V_O = –10 V to +10 V) (T_A = +25°C) R_L = 100 Ω R_L = 600 Ω (T_A = –40° to +85°C) R_L = 600 Ω	6	A_{VOL}	 25 50 25	 — 200 —	 — — —	kV/V
Output Voltage Swing (V_{ID} = ±1.0 V) (V_{CC} = +15 V, V_{EE} = –15 V) R_L = 100 Ω R_L = 100 Ω R_L = 600 Ω R_L = 600 Ω (V_{CC} = +2.5 V, V_{EE} = –2.5 V) R_L = 100 Ω R_L = 100 Ω	7, 8, 9	 V_{O+} V_{O-} V_{O+} V_{O-} V_{O+} V_{O-}	 10 — 13 — 1.2 —	 +11.7 –11.7 +13.8 –13.8 +1.66 –1.74	 — –10 — –13 — –1.2	V
Common Mode Rejection (V_{in} = ±13 V)	10	CMR	80	116	—	dB
Power Supply Rejection (V_{CC}/V_{EE} = +15 V/–15 V, +5.0 V/–15 V, +15 V/–5.0 V)	11	PSR	 80	 120	 —	dB

DC ELECTRICAL CHARACTERICISTICS (V_{CC} = +15, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Output Short Circuit Current (V_{ID} = ±1.0 V Output to Gnd)	12, 13	I_{SC}				mA
(V_{CC} = +15 V, V_{EE} = −15 V)						
Source			190	+250	—	
Sink			—	−280	−215	
(V_{CC} = +2.5 V, V_{EE} = −2.5 V)						
Source			63	+94	—	
Sink			—	−80	−46	
Power Supply Current per Amplifier (V_O = 0 V)	14	I_D				mA
(V_S = ±2.5 V to ±15 V)						
T_A = +25°C			—	2.2	2.8	
T_A = −40° to +85°C			—	—	3.3	

AC ELECTRICAL CHARACTERICISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 100 Ω, C_L = 100 pF, A_V = +1)	15	SR	1.2	2.6	—	V/μs
Gain Bandwidth Product (f = 20 kHz)	16	GBW	4.0	7.4	—	MHz
Unity Gain Frequency (Open-Loop) (R_L = 600 Ω, C_L = 0 pF)	—	f_U	—	3.5	—	MHz
Gain Margin (R_L = 600 Ω, C_L = 0 pF)	19, 20	A_m	—	15	—	dB
Phase Margin (R_L = 600 Ω, C_L = 0 pF)	19, 20	$\varnothing_m$	—	52	—	Deg
Channel Separation (f = 100 Hz to 20 kHz)	21	CS	—	−120	—	dB
Power Bandwidth (V_O = 20 V_{p-p}, R_L = 600 Ω, THD ≤ 1%)	—	BW_p	—	32	—	kHz
Total Harmonic Distortion (R_L = 600 Ω, V_O = 2.0 V_{p-p}, A_V = +1)	22	THD				%
f = 1.0 kHz			—	0.0027	—	
f = 10 kHz			—	0.011	—	
f = 20 kHz			—	0.022	—	
Open-Loop Output Impedance (V_O = 0 V, f = 2.5 MHz, A_V = 10)	23	$\|Z_O\|$	—	75	—	Ω
Differential Input Resistance (V_{CM} = 0 V)	—	R_{in}	—	200	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)	—	C_{in}	—	10	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω)	24	e_n				nV/√Hz
f = 10 Hz			—	7.5		
f = 1.0 kHz			—	5.0	——	
Equivalent Input Noise Current	—	i_n				pA/√Hz
f = 10 Hz			—	0.33	—	
f = 1.0 kHz			—	0.15	—	

Figure 1. Maximum Power Dissipation versus Temperature

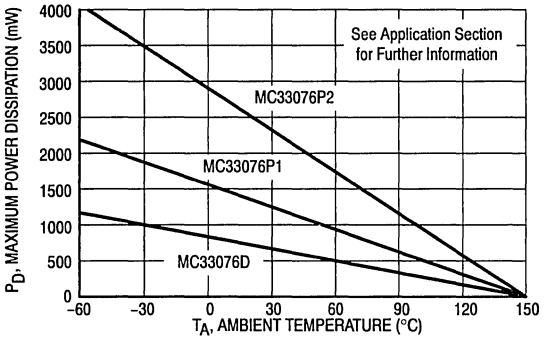


Figure 2. Distribution of Input Offset Voltage

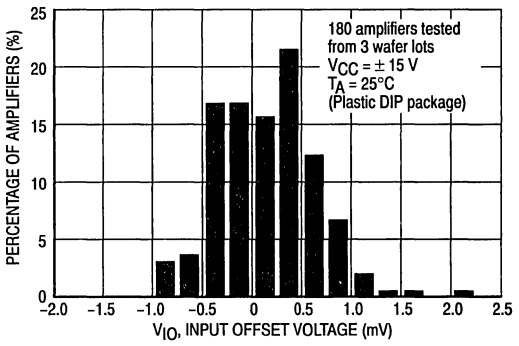


Figure 3. Input Bias Current versus Common Mode Voltage

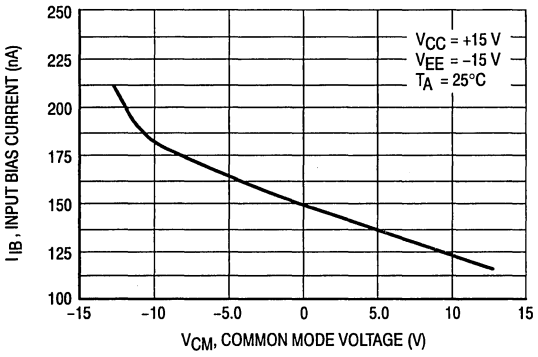


Figure 4. Input Bias Current versus Temperature

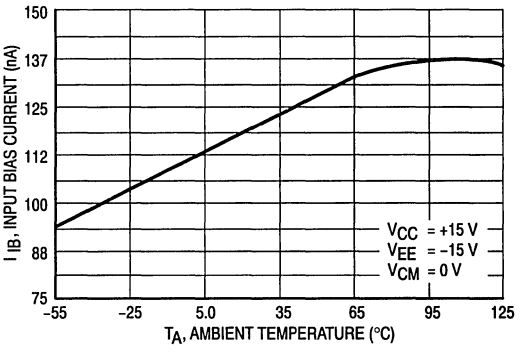


Figure 5. Input Common Mode Voltage Range versus Temperature

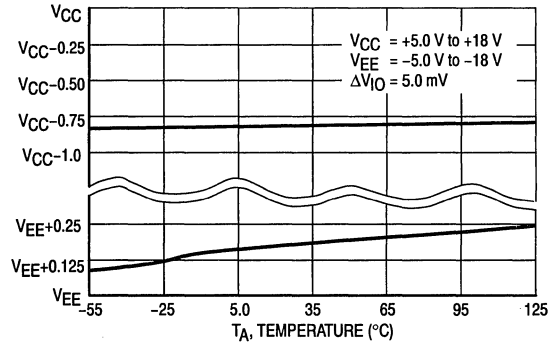
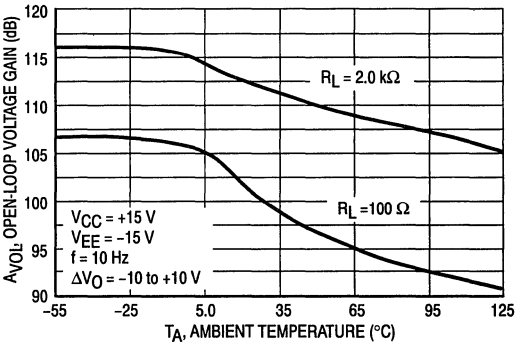


Figure 6. Open-Loop Voltage Gain versus Temperature



2

Figure 7. Output Voltage Swing versus Supply Voltage

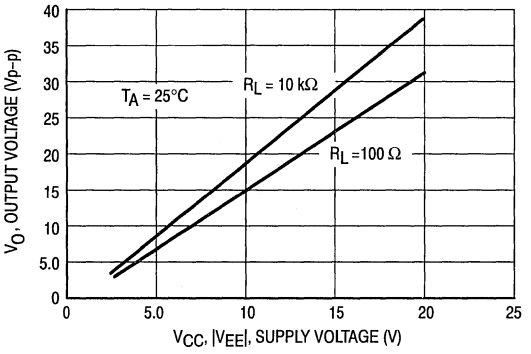


Figure 8. Maximum Peak-to-Peak Output Voltage Swing versus Load Resistance

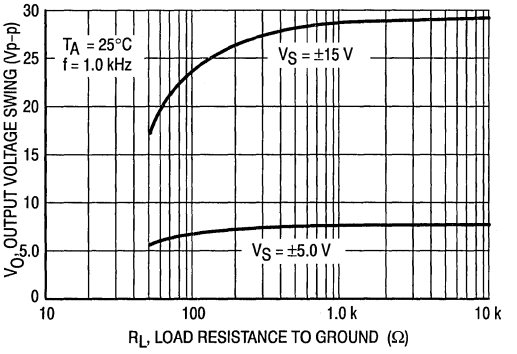


Figure 9. Output Voltage versus Frequency

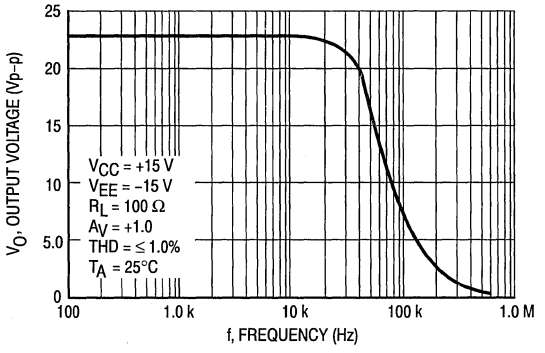


Figure 10. Common Mode Rejection versus Frequency Over Temperature

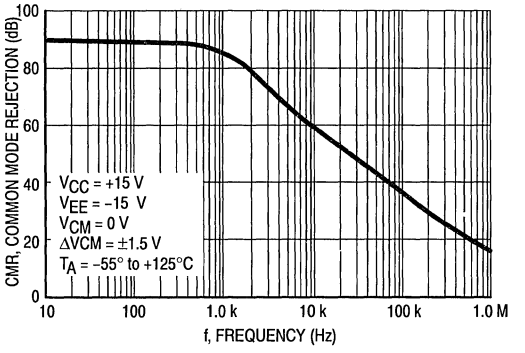


Figure 11. Power Supply Rejection versus Frequency Over Temperature

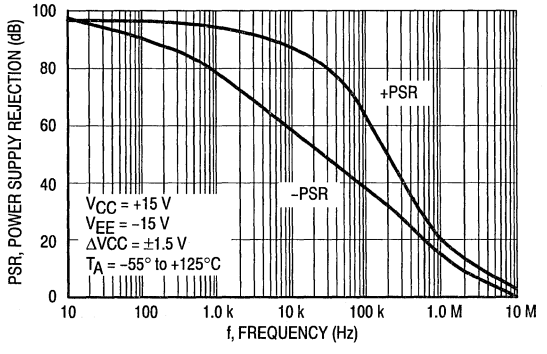


Figure 12. Output Short Circuit Current versus Output Voltage

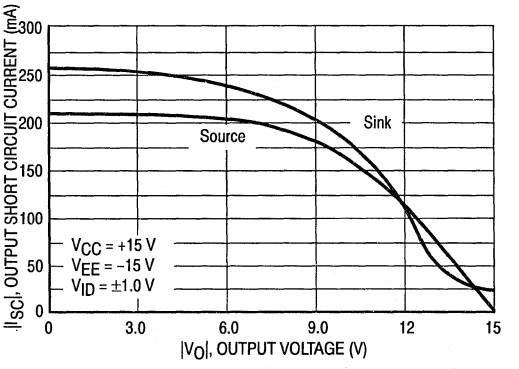


Figure 13. Output Short Circuit Current versus Temperature

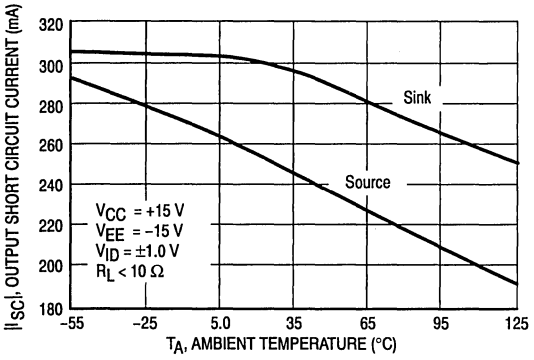


Figure 14. Supply Current versus Supply Voltage With No Load

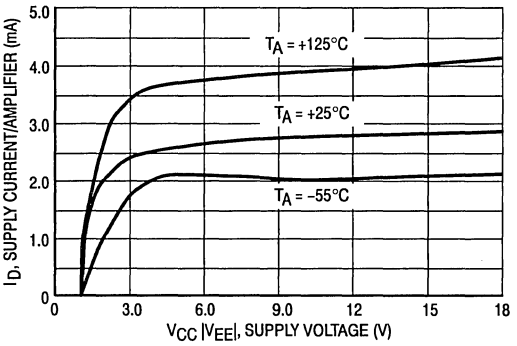


Figure 15. Slew Rate versus Temperature

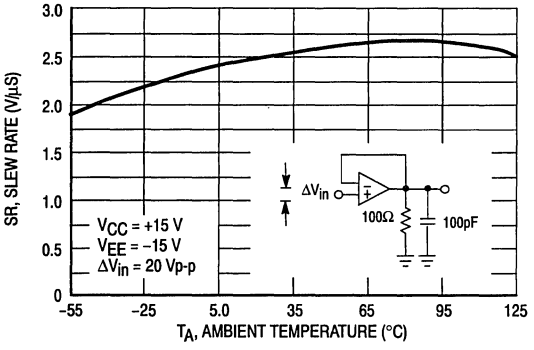


Figure 16. Gain Bandwidth Product versus Temperature

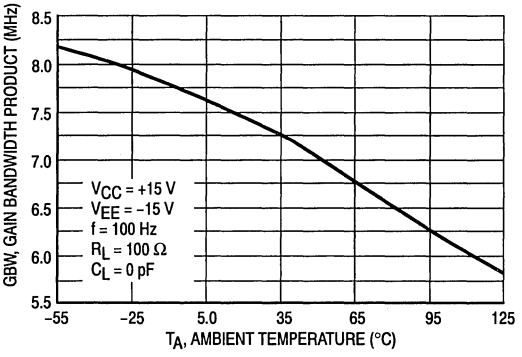


Figure 17. Voltage Gain and Phase versus Frequency

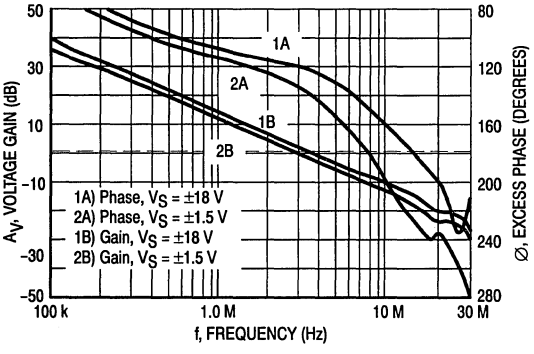
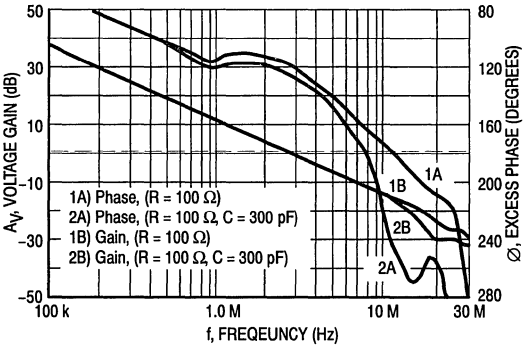


Figure 18. Voltage Gain and Phase versus Frequency



2

Figure 19. Phase Margin and Gain Margin versus Differential Source Resistance

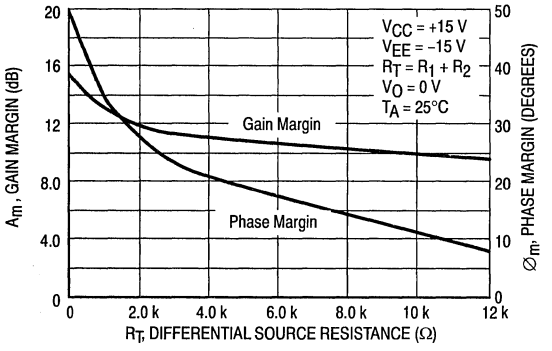


Figure 20. Open-Loop Gain Margin and Phase Margin versus Output Load Capacitance

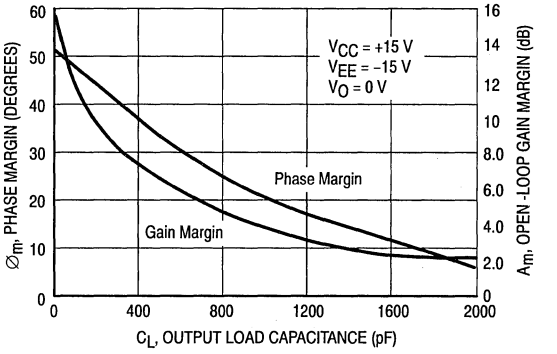


Figure 21. Channel Separation versus Frequency

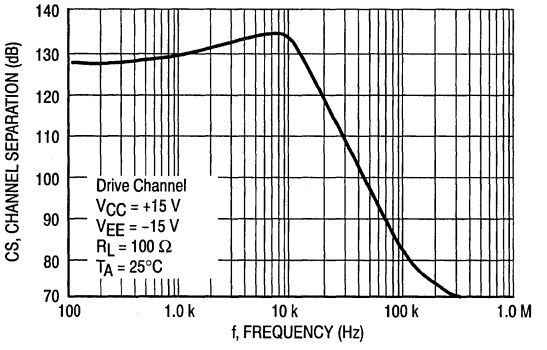


Figure 22. Total Harmonic Distortion versus Frequency

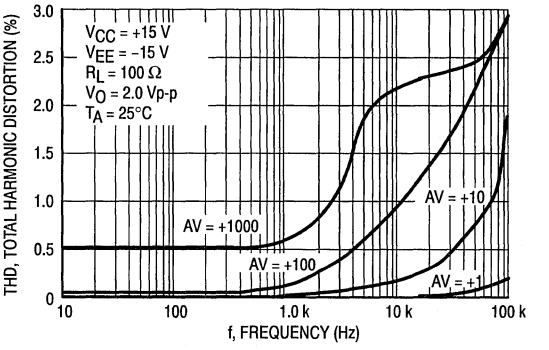


Figure 23. Output Impedance versus Frequency

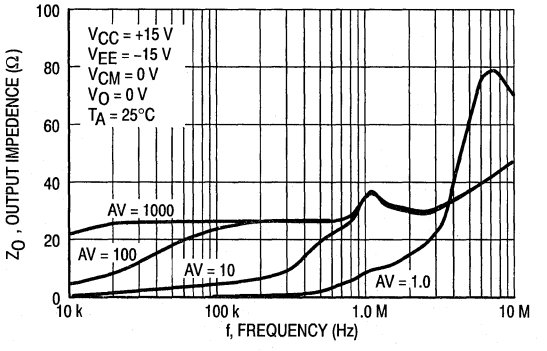


Figure 24. Input Referred Noise Voltage versus Frequency

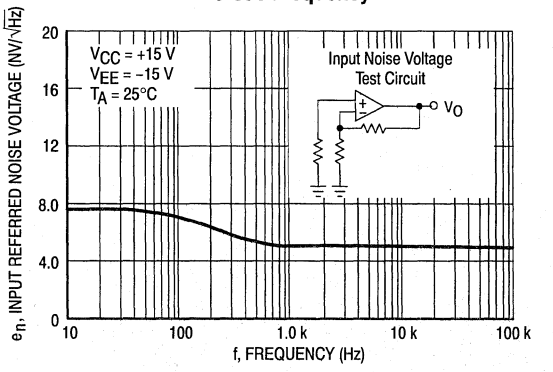


Figure 25. Percent Overshoot versus Load Capacitance

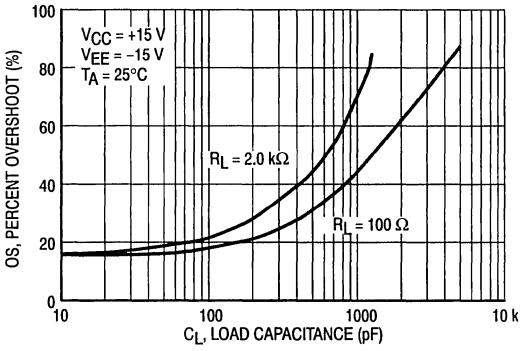
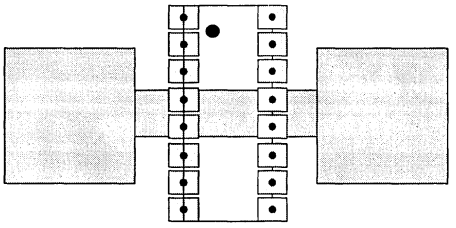


Figure 26. PC Board Heatsink Example



APPLICATIONS INFORMATION

The MC33076 dual operational amplifier is available in the standard 8 pin plastic dual-in-line (DIP) and surface mount packages, and also in a 16 pin batwing power package. To enhance the power dissipation capability of the power package, Pins 4, 5, 12, and 13 are tied together on the leadframe, giving it an ambient thermal resistance of 52°C/W typically, in still air. The junction to ambient thermal resistance ($R_{\theta JA}$) can be decreased further by using a copper pad on the printed circuit board (as shown in Figure 26) to draw the heat away from the package. *Care must be taken not to exceed the maximum junction temperature or damage to the device may occur.*

2

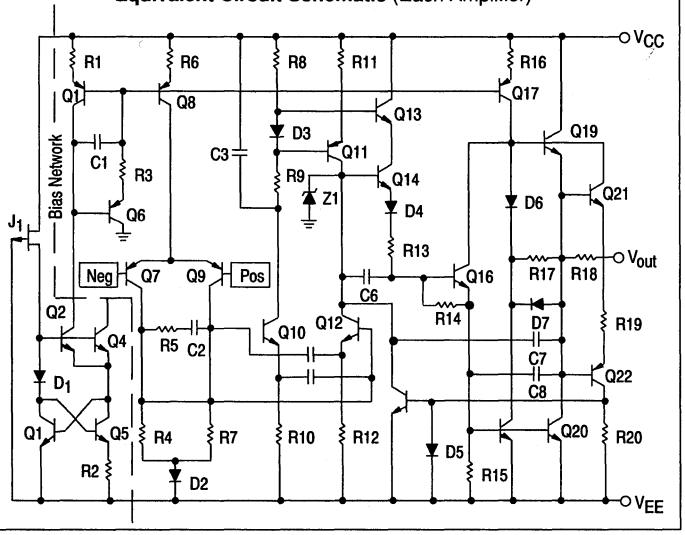
Dual, Low Noise Operational Amplifier

The MC33077 is a precision high quality, high frequency, low noise monolithic dual operational amplifier employing innovative bipolar design techniques. Precision matching coupled with a unique analog resistor trim technique is used to obtain low input offset voltages. Dual-doublet frequency compensation techniques are used to enhance the gain bandwidth product of the amplifier. In addition, the MC33077 offers low input noise voltage, low temperature coefficient of input offset voltage, high slew rate, high AC and DC open-loop voltage gain and low supply current drain. The all NPN transistor output stage exhibits no deadband cross-over distortion, large output voltage swing, excellent phase and gain margins, low open-loop output impedance and symmetrical source and sink AC frequency performance.

The MC33077 is tested over the automotive temperature range and is available in plastic DIP and SO-8 packages (P and D suffixes).

- Low Voltage Noise: 4.4 nV/$\sqrt{\text{Hz}}$ @ 1.0 kHz
- Low Input Offset Voltage: 0.2 mV
- Low TC of Input Offset voltage: 2.0 μV/°C
- High gain Bandwidth Product: 37 MHz @ 100 kHz
- High AC Voltage Gain: 370 @ 100 kHz
  1850 @ 20 kHz
- Unity Gain Stable: with Capacitance Loads to 500 pF
- High Slew Rate: 11 V/μs
- Low Total Harmonic Distortion: 0.007%
- Large Output Voltage Swing: +14 V to −14.7 V
- High DC Open-Loop Voltage Gain: 400 k (112 dB)
- High Common Mode Rejection: 107 dB
- Low Power Supply Drain Current: 3.5 mA
- Dual Supply Operation: ±2.5 V to ±18 V

Equivalent Circuit Schematic (Each Amplifier)



MC33077

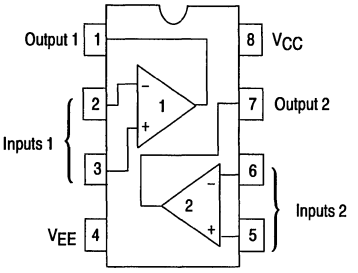
DUAL, LOW NOISE OPERATIONAL AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



(Dual, Top View)

ORDERING INFORMATION

Device	Ambient Test Temperature Range	Package
MC33077D	−40° to +85°C	SO-8
MC33077P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = –40° to +85°C	$\lvert V_{IO}\rvert$	 — —	 0.13 —	 1.0 1.5	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = –40° to +85°C	$\Delta V_{IO}/\Delta T$	—	2.0	—	µV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = –40° to +85°C	I_{IB}	 — —	 280 —	 1000 1200	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = –40° to +85°C	I_{IO}	 — —	 15 —	 180 240	nA
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	V_{ICR}	±13.5	±14	—	V
Large Signal Voltage Gain (V_O = ±1.0 V, R_L = 2.0 kΩ) T_A = +25°C T_A = –40° to +85°C	A_{VOL}	 150 k 125 k	 400 k —	 — —	V/V
Output voltage Swing (V_{ID} = ±1.0 V) R_L = 2.0 kΩ R_L = 2.0 kΩ R_L = 10 kΩ R_L = 10 kΩ	 V_{O+} V_{O-} V_{O+} V_{O-}	 +13.0 — +13.4 —	 +13.6 –14.1 +14.0 –14.7	 — –13.5 — –14.3	V
Common Mode Rejection (V_{in} = ±13 V)	CMR	85	107	—	dB
Power Supply Rejection (Note 3) V_{CC}/V_{EE} = +15 V/ –15 V to +5.0 V/ –5.0 V	PSR	80	90	—	dB
Output Short circuit current (V_{ID} = ±1.0 V, Output to Ground) Source Sink	I_{SC}	 +10 –20	 +26 –33	 +60 +60	mA
Power Supply Current (V_O = 0 V, All Amplifiers) T_A = +25°C T_A = –40° to +85°C	I_D	 — —	 3.5 —	 4.5 4.8	mA

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE} (See Applications Information).
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (See power dissipation performance characteristic, Figure 1).
3. Measured with V_{CC} and V_{EE} simultaneously varied.

2

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0)	SR	8.0	11	—	V/μs
Gain Bandwidth Product (f = 100 kHz)	GBW	25	37	—	MHz
AC Voltage Gain (R_L = 2.0 kΩ, V_O = 0 V) f = 100 kHz f = 20 kHz	A_{VO}	 — —	 370 1850	 — —	V/V
Unity Gain Frequency (Open-Loop)	f_U	—	7.5	—	MHz
Gain Margin (R_L = 2.0 kΩ, C_L = 10 pF)	A_m	—	10	—	dB
Phase Margin (R_L = 2.0 kΩ, C_L = 10 pF)	$\varnothing_m$	—	55	—	Degrees
Channel Separation (f = 20 Hz to 20 kHz, R_L = 2.0 kΩ, V_O = 10 V_{p-p})	CS	—	−120	—	dB
Power Bandwidth (V_O = 27$_{p-p}$, R_L = 2.0 kΩ, THD ≤ 1%)	BW_p	—	200	—	kHz
Distortion (R_L = 2.0 kΩ) A_V = +1.0, f = 20 Hz to 20 kHz V_O = 3.0 V_{rms} A_V = 2000, f = 20 kHz V_O = 2.0 V_{p-p} V_O = 10 V_{p-p} A_V = 4000, f = 100 kHz V_O = 2.0 V_{p-p} V_O = 10 V_{p-p}	THD	 — — — — —	 0.007 0.215 0.242 0.3.19 0.316	 — — — — —	%
Open-Loop Output Impedance (V_O = 0 V, f = f_U)	$\|Z_O\|$	—	36	—	Ω
Differential Input Resistance (V_{CM} = 0 V)	R_{IN}	—	270	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)	C_{IN}	—	15	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω) f = 10 Hz f = 1.0 kHz	e_n	 — —	 6.7 4.4	 — —	nV/√Hz
Equivalent Input Noise Current (F = 1.0 kHz) f = 10 Hz f = 1.0 kHz	i_n	 — —	 1.3 0.6	 — —	pA/√Hz

Figure 1. Maximum Power Dissipation versus Temperature

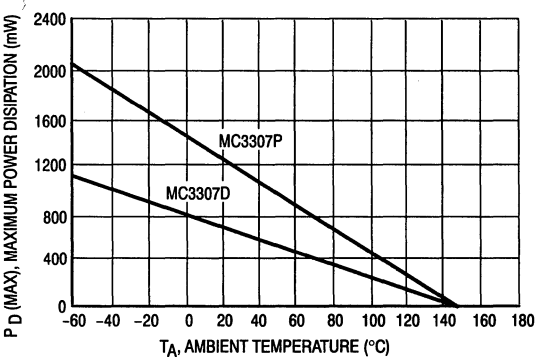


Figure 2. Input Bias Current versus Supply Voltage

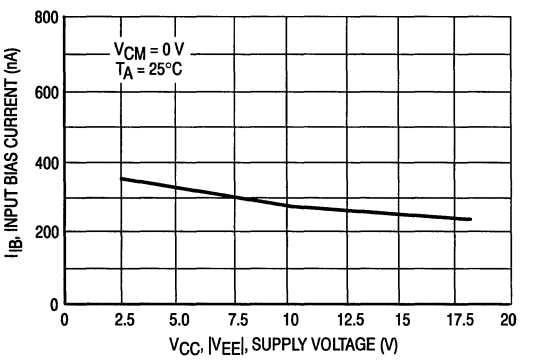


Figure 3. Input Bias Current versus Temperature

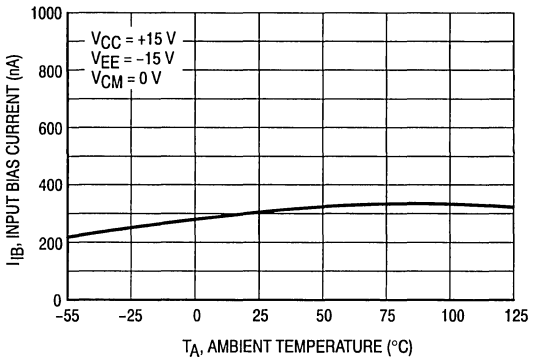


Figure 4. Input Offset Voltage versus Temperature

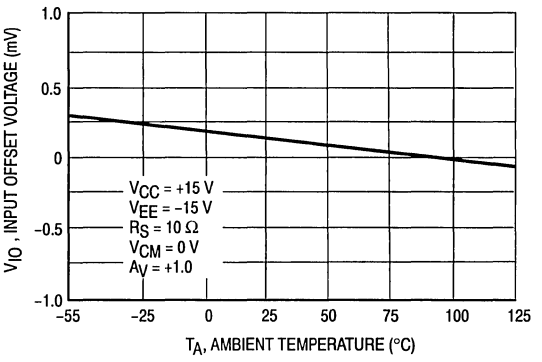


Figure 5. Input Bias Current versus Common Mode Voltage

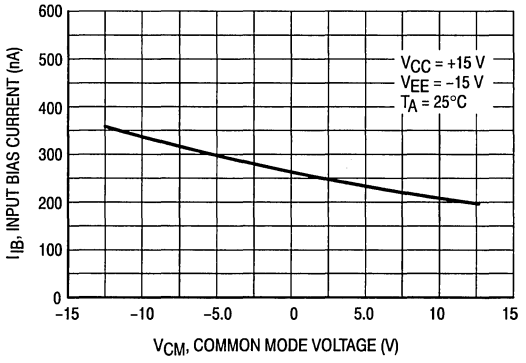


Figure 6. Input Common Mode Voltage Range versus Temperature

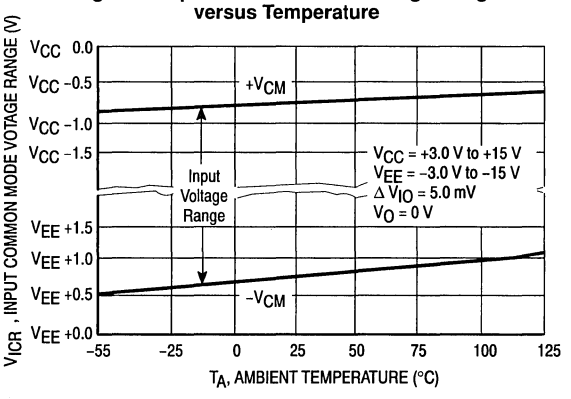


Figure 7. Output Saturation Voltage versus Load Resistance to Ground

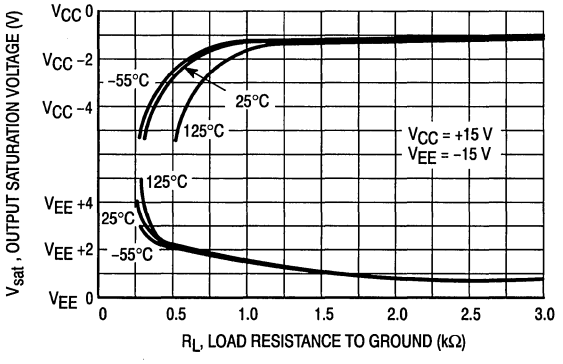


Figure 8. Output Short Circuit Current versus Temperature

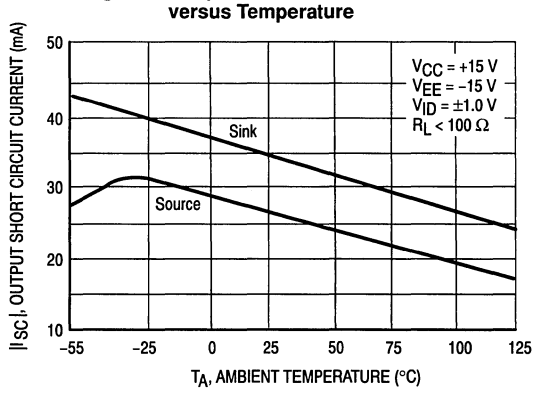


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Figure 9. Supply Current versus Temperature

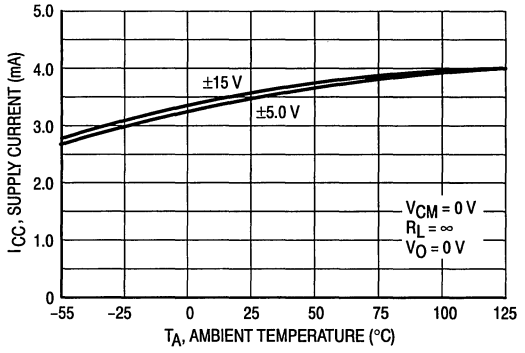

Figure 10. Common Mode Rejection versus Frequency

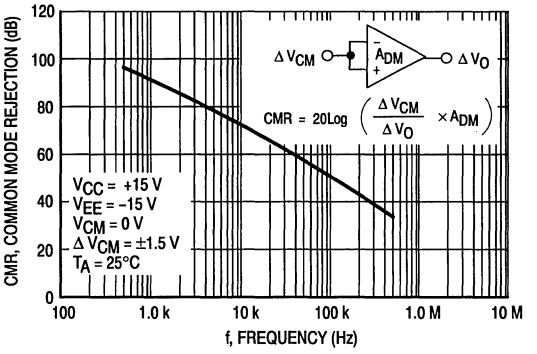

Figure 11. Power Supply Rejection versus Frequency

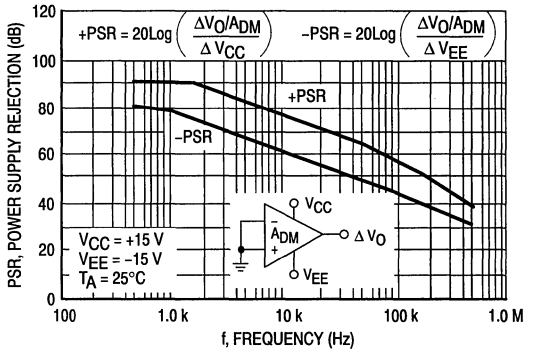

Figure 12. Gain Bandwidth Product versus Supply Voltage

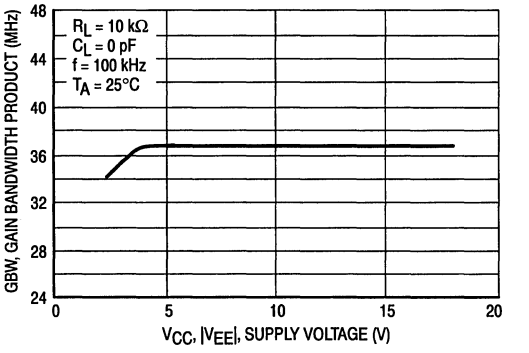

Figure 13. Gain Bandwidth Product versus Temperature

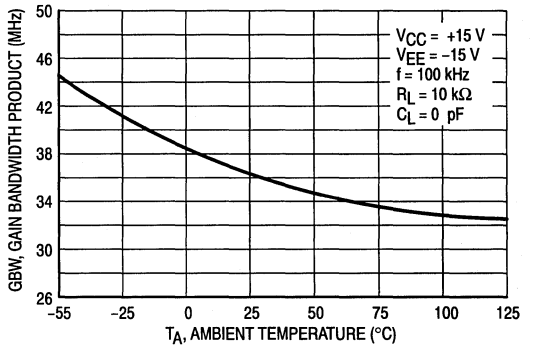

Figure 14. Maximum Output Voltage versus Supply Voltage

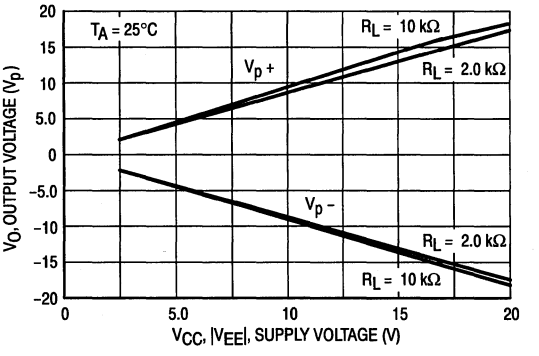

Figure 15. Output Voltage versus Frequency

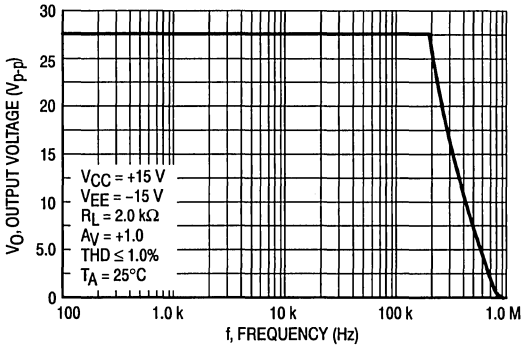

Figure 16. Open-Loop Voltage Gain versus Supply Voltage

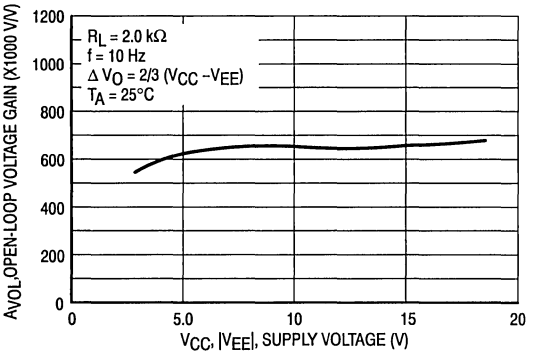

Figure 17. Open-Loop Voltage Gain versus Temperature

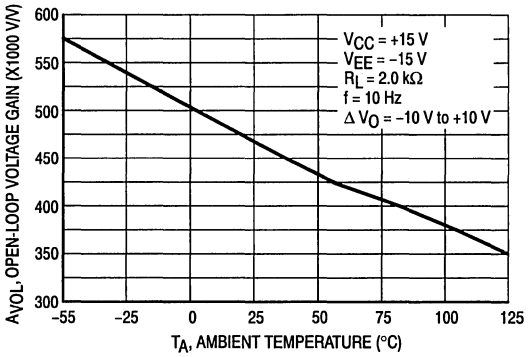

Figure 18. Output Impedance versus Frequency

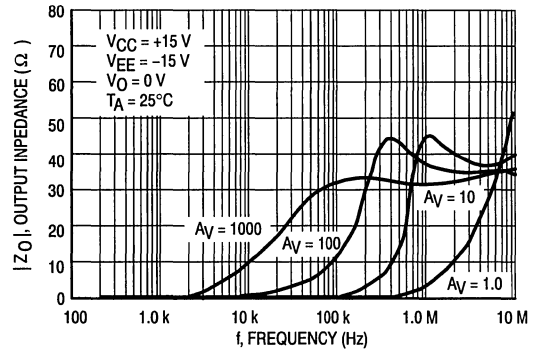

Figure 19. Channel Separation versus Frequency

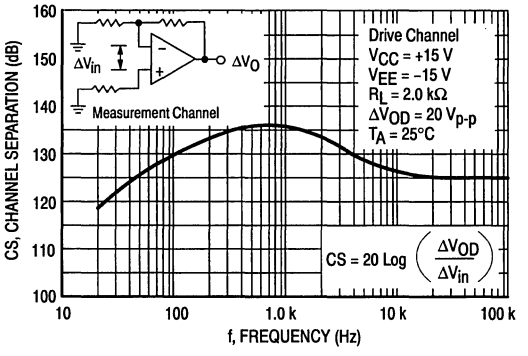

Figure 20. Total Harmonic Distortion versus Frequency

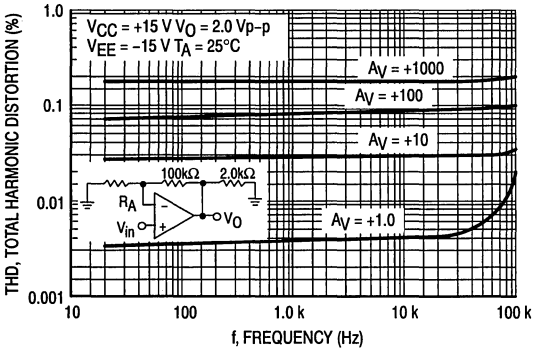

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Figure 21. Total Harmonic Distortion versus Frequency

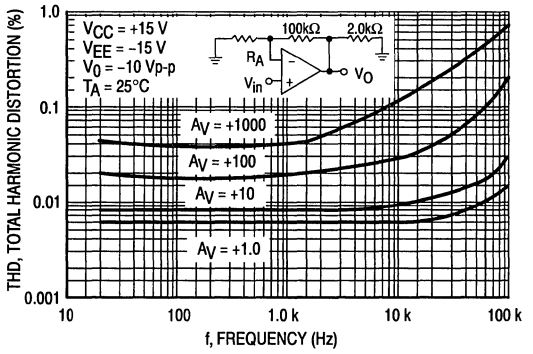

Figure 22. Total harmonic Distortion versus Output Voltage

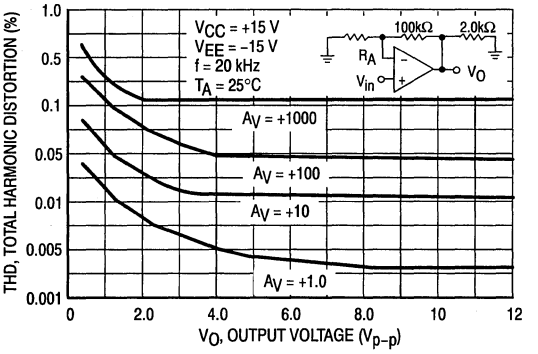

Figure 23. Slew Rate versus Supply Voltage

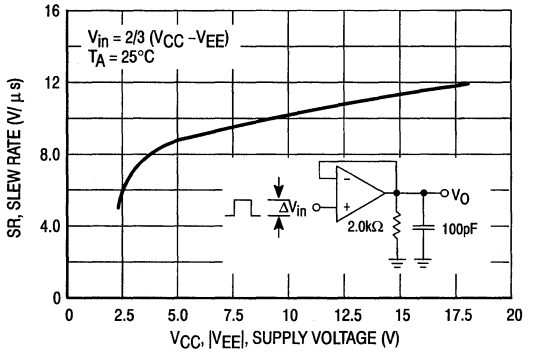

Figure 24. Slew Rate versus Temperature

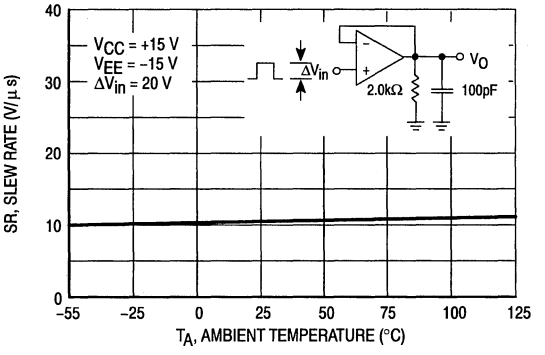

Figure 25. Voltage Gain and Phase versus Frequency

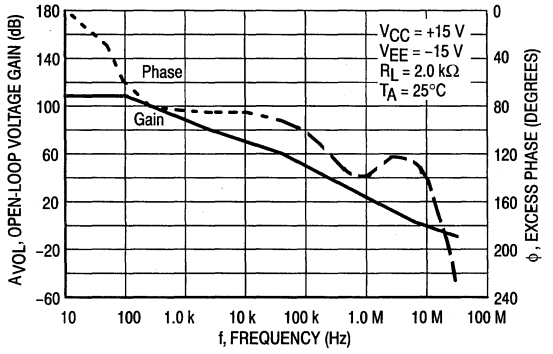

Figure 26. Open-Loop Gain Margin and Phase Margin versus Output Load Capacitance

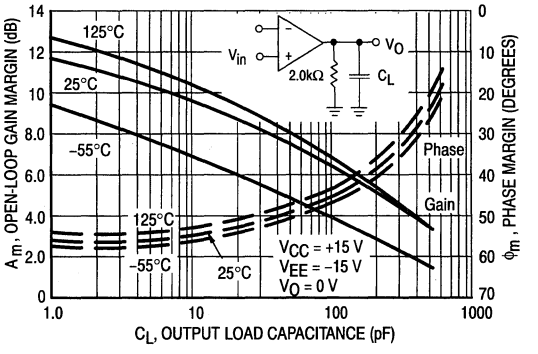

Figure 27. Phase Margin versus Output Voltage

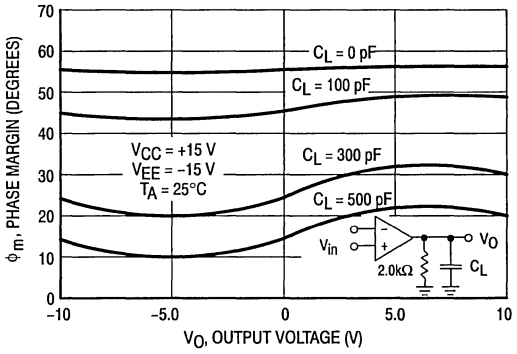

Figure 28. Overshoot versus Output Load Capacitance

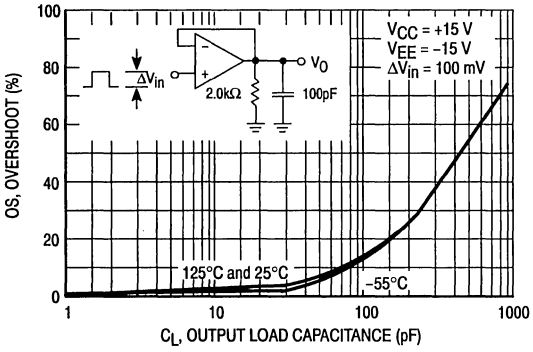

Figure 29. Input Referred Noise Voltage and Current versus Frequency

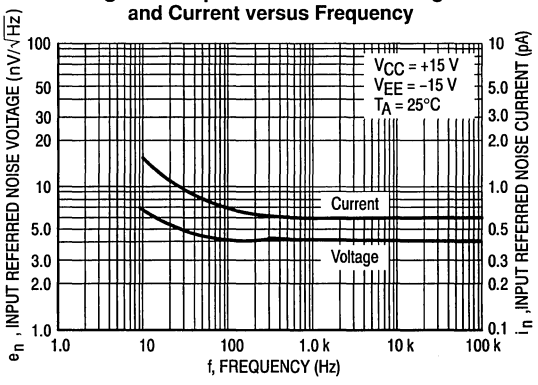

Figure 30. Total Input Referred Noise Voltage versus Source Resistant

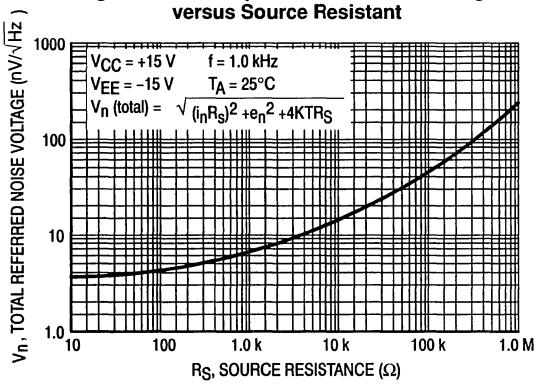

Figure 31. Phase Margin and Gain Margin versus Differential Source Resistance

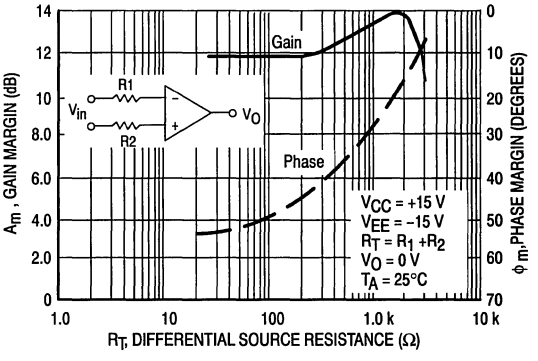

Figure 32. Inverting Amplifer Slew Rate

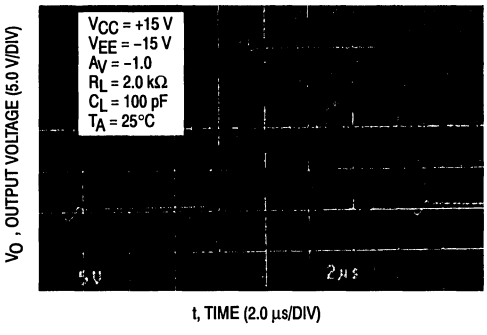

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Figure 33. Noninverting Amplifier Slew Rate

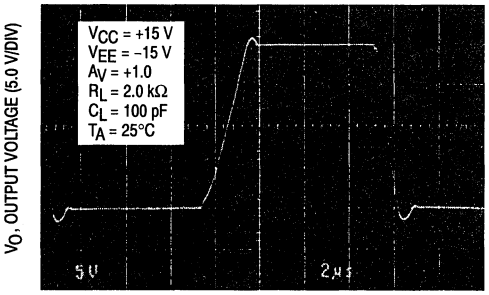


Figure 34. Noninverting Amplifier Overshoot

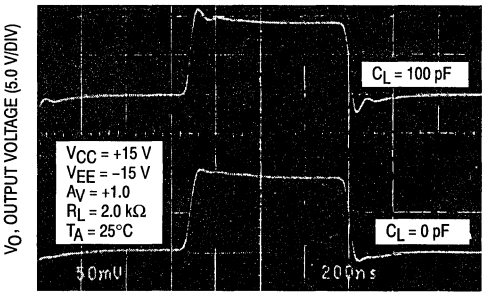
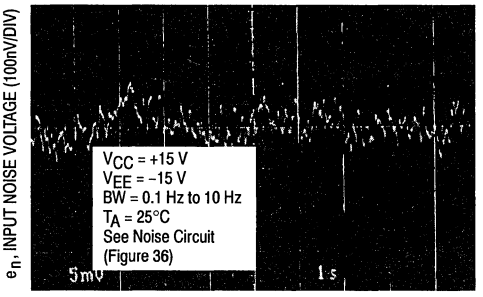


Figure 35. Low Frequency Noise Voltage versus Time



APPLICATIONS INFORMATION

The MC33077 is designed primarily for its low noise, low offset voltage, high gain bandwidth product and large output swing characteristics. Its outstanding high frequency gain/phase performance make it a very attractive amplifier for high quality preamps, instrumentation amps, active filters and other applications requiring precision quality characteristics.

The MC33077 utilizes high frequency lateral PNP input transistors in a low noise bipolar differential stage driving a compensated Miller integration amplifier. Dual-doublet frequency compensation techniques are used to enhance the gain bandwidth product. The output stage uses an all NPN transistor design which provides greater output voltage swing and improved frequency performance over more conventional stages by using both PNP and NPN transistors (Class AB). This combination produces an amplifier with superior characteristics.

Through precision component matching and innovative current mirror design, a lower than normal temperature coefficient of input offset voltage (2.0 μV/°C as opposed to 10 μV/°C), as well as low input offset voltage, is accomplished.

The minimum common mode input range is from 1.5 V below the positive rail (V_{CC}) to 1.5 V above the negative rail (V_{EE}). The inputs will typically common mode to within 1.0 V of both negative and positive rails though degradation in offset voltage and gain will be experienced as the common mode voltage nears either supply rail. In practice, though not recommended, the input voltage may exceed V_{CC} by approximately 30 V and decrease below the V_{EE} by approximately 0.6 V without causing permanent damage to the device. If the input voltage on either or both inputs is less than approximately 0.6 V, excessive current may flow, if not limited, causing permanent damage to the device.

The amplifier will not latch with input source currents up to 20 mA, though in practice, source currents should be limited to 5.0 mA so as to avoid any parametric damage to the device. If both inputs exceed V_{CC}, the output will be in the high state and phase reversal may occur. No phase reversal will occur if the voltage on one input is within the common mode range and the voltage on the other input exceeds V_{CC}. Phase reversal may occur if the input voltage on either or both inputs is less than 1.0 V above the negative rail. Phase reversal will be experienced if the voltage on either or both inputs is less than V_{EE}.

Through the use of dual-doublet frequency compensation techniques, the gain bandwidth product has been greatly enhanced over other amplifiers using the conventional single pole compensation. The phase an gain error of the amplifier remains low to higher frequencies for fixed amplifier gain configurations.

With the all NPN output stage, there is minimal swing loss to the supply rails, producing superior output swing, no crossover distortion and improved output phase symmetry with output voltage excursions. Output phase symmetry being the amplifiers ability to maintain a constant phase relation independent of its output voltage swing. Output phase symmetry degradation in the more conventional PNP and NPN transistor output stage was primarily due to the inherent cut-off frequency mismatch of the PNP and NPN transistors (typically 10 MHz and 300 MHz, respectively) used, causing considerable phase change to occur as the output voltage changes. By eliminating the PNP in the output, such phase change has been avoided and a very significant improvement in output phase symmetry as well as output swing has been accomplished.

The output swing improvement is most noticeable when operation is with lower supply voltages (typically 30% with ± 5.0 V supplies). With a 10 k load, the output of the amplifier can typically swing to within 1.0 V of the positive rail (V_{CC}), and to within 0.3 V of the negative rail (V_{EE}), producing a 28.7 V_{p-p} signal from ±15 V supplies. Output voltage swing can be further improved by using an output pull-up resistor referenced to the V_{CC}. Where output signals are referenced to the positive supply rail, the pull-up resistor will pull the output to V_{CC} during the positive swing and during the negative swing, the NPN output transistor collector will pull the output very near V_{EE}. This configuration will produce the maximum attainable output signal from given supply voltages. The value of load resistance used should be much less than any feedback resistance so as to avoid excess loading and allow easy pull-up of the output.

Output impedance of the amplifier is typically less than 50 Ω at frequencies less than the unity gain crossover frequency (see Figure 18). The amplifier is unity gain stable with output capacitance loads up to 500 pF at full output swing over the –55° to +125°C temperature range. Output phase symmetry is excellent with typically 4°C total phase change over a 20 V output excursion at 25°C with a 2.0 kΩ and 100 pF load. With a 2.0 kΩ resistive load and no capacitance loading the total phase change is approximately one degree for the same 20 V output excursion. With a 2.0 kΩ and 500 pF load at 125°C the total phase change is typically only 10°C for a 20 V output excursion (see Figure 27).

As with all amplifiers, care should be exercised so as to insure that one does not create a pole at the input of the amplifier which is near the closed-loop corner frequency. This becomes a greater concern when using high frequency amplifiers since it is very easy to create such a pole with relatively small values of resistance on the inputs. If this does

occur, the amplifier's phase will degrade severely causing the amplifier to become unstable. Effective source resistances, acting in conjunction with the input capacitance of the amplifier, should be kept to a minimum so as to avoid creating such a pole at the input (see Figure 31). There is minimal effect on stability where the created input pole is much greater than the closed-loop corner frequency. Where amplifier stability is affected as a result of a negative feedback resistor in conjunction with the amplifier's input capacitance, creating a pole near the closed-loop corner frequency, lead capacitor compensation techniques (lead capacitor in parallel with the feedback resistor) can be employed to improve stability. The feedback resistor and lead capacitor RC time constant should be larger than that of the uncompensated input pole frequency. Having a high resistance connected to the noninverting input of the amplifier can create a like instability problem. Compensation for this condition can be accomplished by adding a lead capacitor in parallel with the noninverting input resistor of such a value as to make the RC time constant larger than the RC time constant of the uncompensated input resistor acting in conjunction with the amplifiers input capacitance.

For optimum frequency performance and stability careful component placement and printed circuit board layout should be exercised. For example, long unshielded input or output leads may result in unwanted input output coupling. In order to reduce the input capacitance, the body of resistors connected to the input pins should be physically close to the input pins. This not only minimizes the input pole creation for optimum frequency response, but also minimizes extraneous signal "pickup" at this node. Power supplies should be decoupled with adequate capacitance as close as possible to the device supply pin.

In addition to amplifier stability considerations, input source resistance values should be low so as to take full advantage of the low noise characteristics of the amplifier. Thermal noise (Johnson Noise) of a resistor is generated by thermally-charged carriers randomly moving within the resistor creating a voltage. The rms thermal noise voltage in a resistor can be calculated from:

$$E_{nr} = \sqrt{4k\,TR \bullet BW}$$

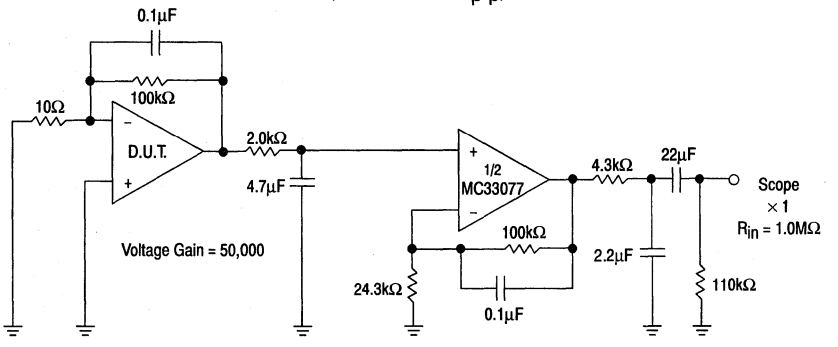
where:

k = Boltzmann's Constant ($1.38 \bullet 10^{-23}$ joules/k)
T = Kelvin temperature
R = Resistance in ohms
BW = Upper and lower frequency limit in Hertz.

By way of reference, a 1.0 kΩ resistor at 25°C, will produce a 4.0 $nV/\sqrt{Hz}$ of rms noise voltage. If this resistor is connected to the input of the amplifier, the noise voltage will be gained-up in accordance to the amplifier's gain configuration, For this reason the selection of input source resistance for low noise circuit applications warrants serious consideration. The total noise of the amplifier, as referred to its inputs, is typically only 4.4 $nV/\sqrt{Hz}$ at 1.0 kHz.

The output of any one amplifier is current limited and thus protected from a direct short to ground, However, under such conditions, it is important to not allow the amplifier to exceed the maximum junction temperature rating. Typically for ±15 V supplies, any one output can be shorted continuously to ground without exceeding the temperature rating.

Figure 36. Voltage Noise Test Circuit
(0.1 Hz to 10 Hz_{p-p})



Note: All capacitors are non-polarized.

MC33078
MC33079

Dual/Quad Low Noise Operational Amplifiers

DUAL/QUAD
LOW NOISE
OPERATIONAL AMPLIFIERS

The MC33078/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high performance concepts for quality audio and data signal processing applications. This family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input voltage noise with high gain bandwidth product and slew rate. The all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source and sink AC frequency performance.

The MC33078/9 family offers both dual and quad amplifier versions, tested over the automotive temperature range and available in the plastic DIP and SOIC packages (P and D suffixes).

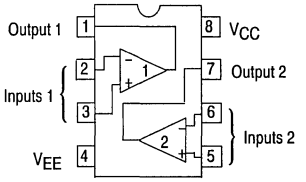
- Dual Supply Operation: ±18 V (Max)
- Low Voltage Noise: 4.5 nV/$\sqrt{Hz}$
- Low Input Offset Voltage: 0.15 mV
- Low T.C. of Input Offset Voltage: 2.0 μV/°C
- Low Total Harmonic Distortion: 0.002%
- High Gain Bandwidth Product: 16 MHz
- High Slew Rate: 7.0 V/μs
- High Open-Loop AC Gain: 800 @ 20 kHz
- Excellent Frequency Stability
- Large Output Voltage Swing: +14.1 V/ −14.6 V
- ESD Diodes Provided on the Inputs

DUAL

P SUFFIX
PLASTIC PACKAGE
CASE 626

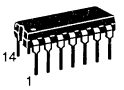
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS

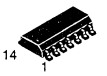


(Dual, Top View)

QUAD

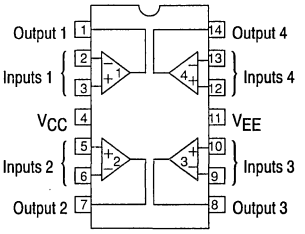


P SUFFIX
PLASTIC PACKAGE
CASE 646



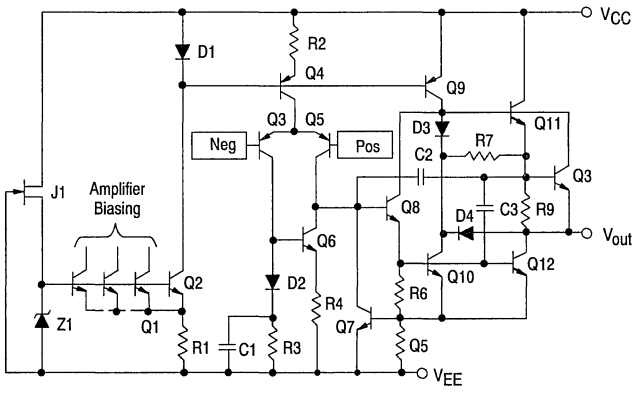
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Quad, Top View)

Equivalent Circuit Schematic
(Each Amplifier)



ORDERING INFORMATION

Device	Test Temperature Range	Package
MC33078D MC33078P	−40° to +85°C	SO-8 Plastic DIP
MC33079D MC33079P		SO-14 Plastic DIP

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).
3. Measured with V_{CC} and V_{EE} differentially varied simultaneously.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V)	$\|V_{IO}\|$				mV
(MC33078) T_A = +25°C		—	0.15	2.0	
T_A = −40° to +85°C		—	—	3.0	
(MC33079) T_A = +25°C		—	0.15	2.5	
T_A = −40° to +85°C		—	—	3.5	
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	—	2.0	—	μV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}				nA
T_A = +25°C		—	300	750	
T_A = −40° to +85°C		—	—	800	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}				nA
T_A = +25°C		—	25	150	
T_A = −40° to +85°C		—	—	175	
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	V_{ICR}	±13	±14	—	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}				dB
T_A = +25°C		90	110	—	
T_A = −40° to +85°C		85	—	—	
Output Voltage Swing (V_{ID} = ±1.0V)					V
R_L = 600 Ω	V_{O+}	—	+10.7	—	
R_L = 600 Ω	V_{O-}	—	−11.9	—	
R_L = 2.0 kΩ	V_{O+}	+13.2	+13.8	—	
R_L = 2.0 kΩ	V_{O-}	—	−13.7	−13.2	
R_L = 10 kΩ	V_{O+}	+13.5	+14.1	—	
R_L = 10 kΩ	V_{O-}	—	−14.6	−14	
Common Mode Rejection (V_{in} = ±13V)	CMR	80	100	—	dB
Power Supply Rejection (Note 3)	PSR	80	105	—	dB
V_{CC}/V_{EE} = +15 V/−15 V to +5.0 V/−5.0 V					
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground)	I_{SC}				mA
Source		+15	+29	—	
Sink		−20	−37	—	
Power Supply Current (V_O = 0 V, All Amplifiers)	I_D				mA
(MC33078) T_A = +25°C		—	4.1	5.0	
T_A = −40° to +85°C		—	—	5.5	
(MC33079) T_A = +25°C		—	8.4	10	
T_A = −40° to +85°C		—	—	11	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics		Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF A_V = +1.0)		SR	5.0	7.0	—	V/μs
Gain Bandwidth Product (f = 100 kHz)		GBW	10	16	—	MHz
Unity Gain Frequency (Open-Loop)		f_U	—	9.0	—	MHz
Gain Margin (R_L = 2.0 kΩ)	C_L = 0 pF C_L = 100 pF	A_m	— —	−11 −6.0	—	dB
Phase Margin (R_L = 2.0 kΩ)	C_L = 0 pF C_L = 100 pF	ϕ_m	— —	55 40	—	Degrees
Channel Separation (f = 20 Hz to 20 kHz)		CS	—	−120	—	dB
Power Bandwidth (V_O = 27 V_{p-p}, R_L = 2.0 kΩ, THD ≤ 1.0%)		BW_p	—	120	—	kHz
Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)		THD	—	0.002	—	%
Open-Loop Output Impedance (V_O = 0 V, f = 9.0 MHz)		$\|Z_O\|$	—	37	—	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{IN}	—	175	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{IN}	—	12	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)		e_n	—	4.5	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)		i_n	—	0.5	—	$pA/\sqrt{Hz}$

Figure 1. Maximum Power Dissipation versus Temperature

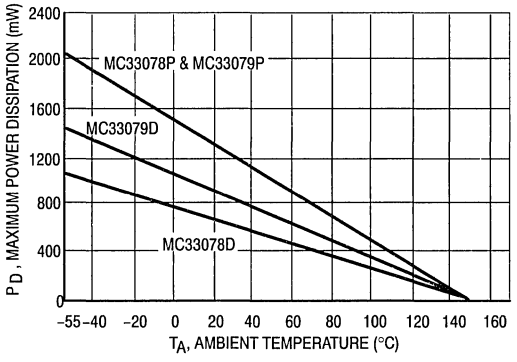


Figure 2. Input Bias Current versus Supply Voltage

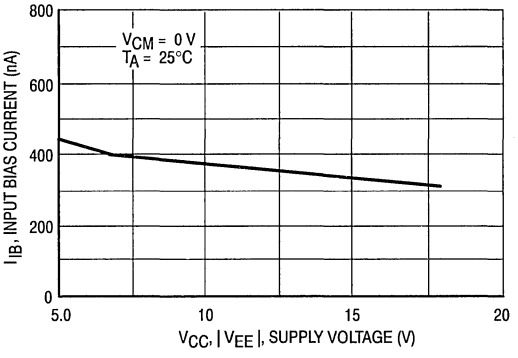


Figure 3. Input Bias Current versus Temperature

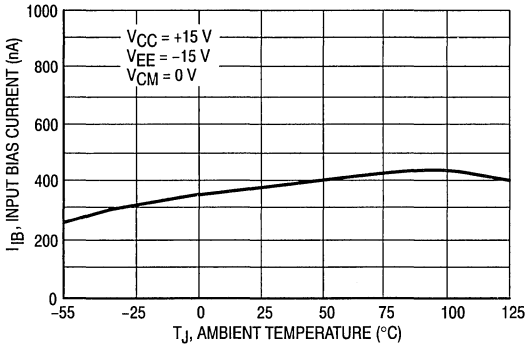


Figure 4. Input Offset Voltage versus Temperature

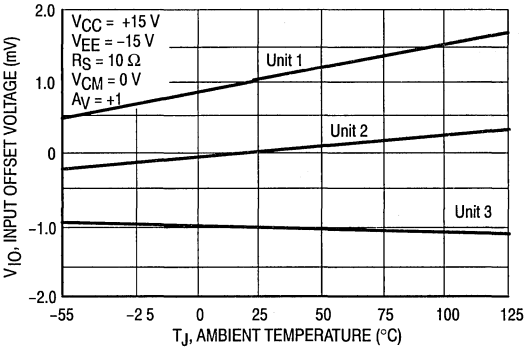


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Figure 5. Input Bias Current versus Common Mode Voltage

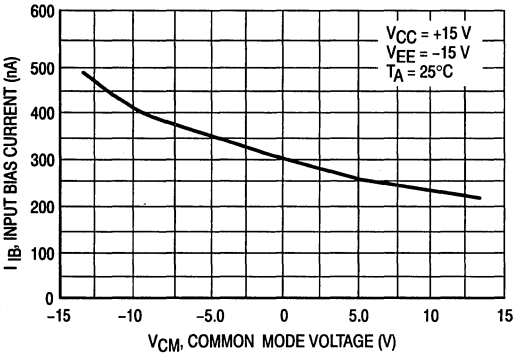


Figure 6. Input Common Mode Voltage Range versus Temperature

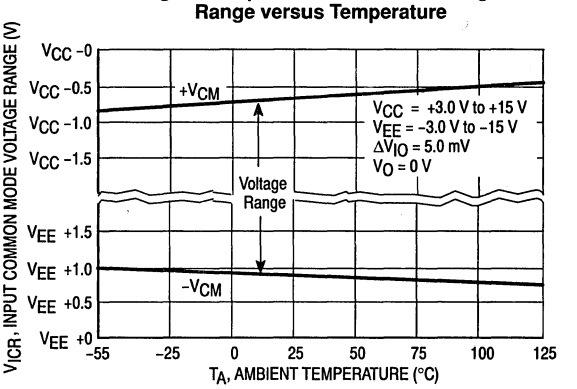


Figure 7. Output Saturation Voltage versus Load Resistance to Ground

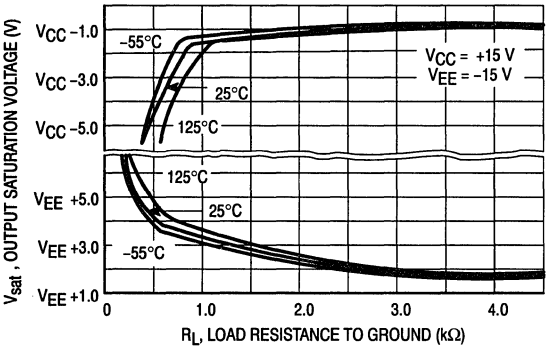


Figure 8. Output Short Circuit Current versus Temperature

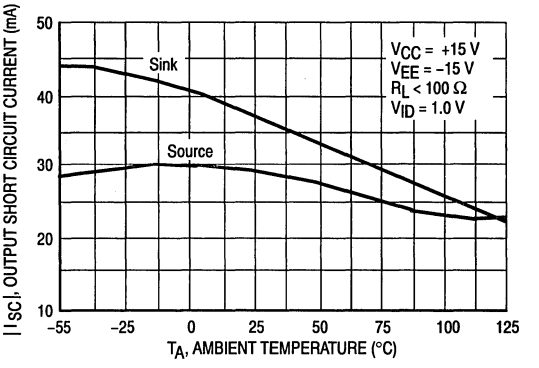


Figure 9. Supply Current versus Temperature

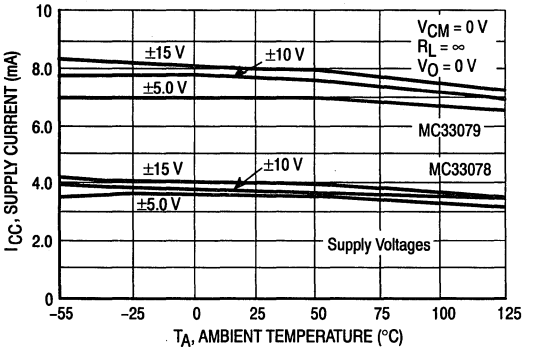


Figure 10. Common Mode Rejection versus Frequency

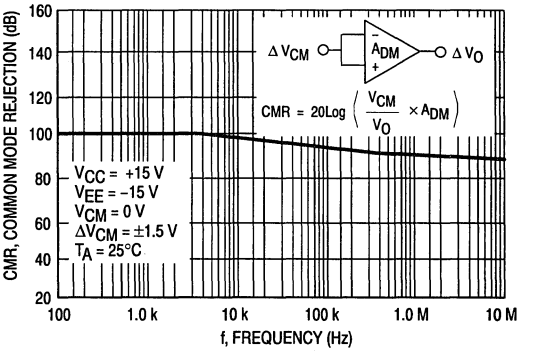


Figure 11. Power Supply Rejection versus Frequency

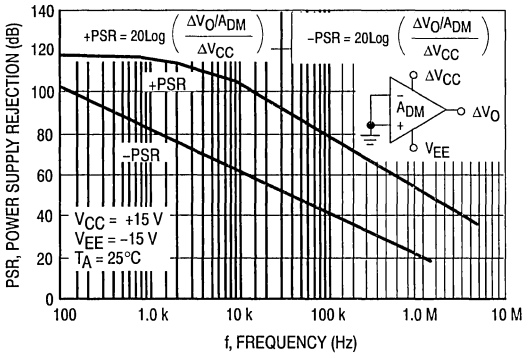


Figure 12. Gain Bandwidth Product versus Supply Voltage

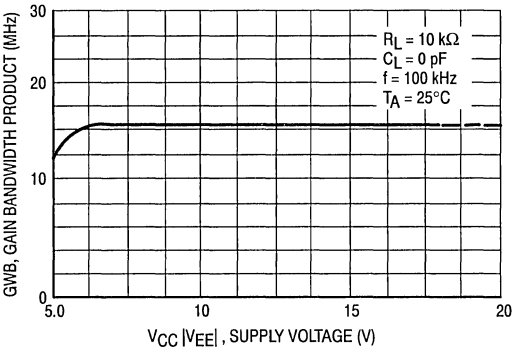


Figure 13. Gain Bandwidth Product versus Temperature

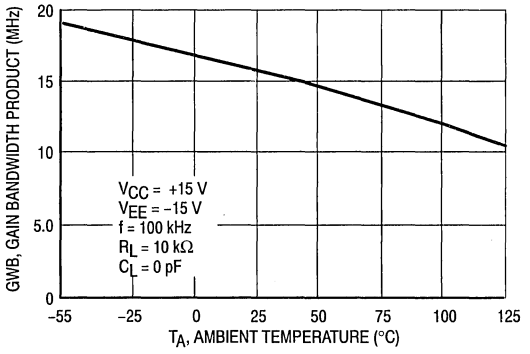


Figure 14. Maximum Output Voltage versus Supply Voltage

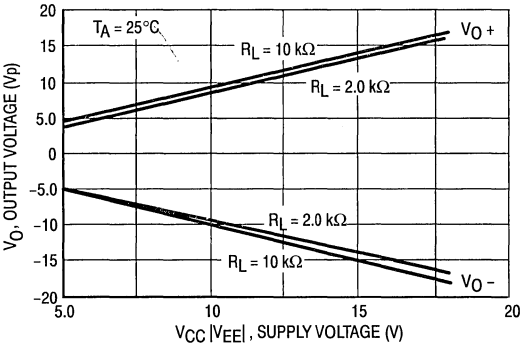


Figure 15. Output Voltage versus Frequency

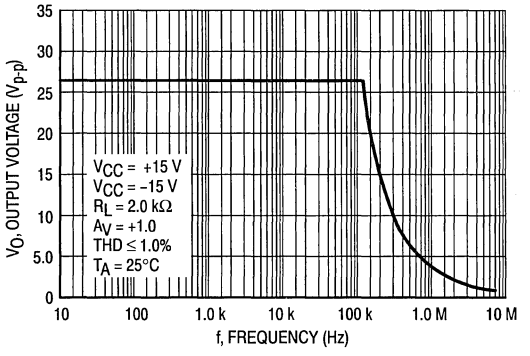
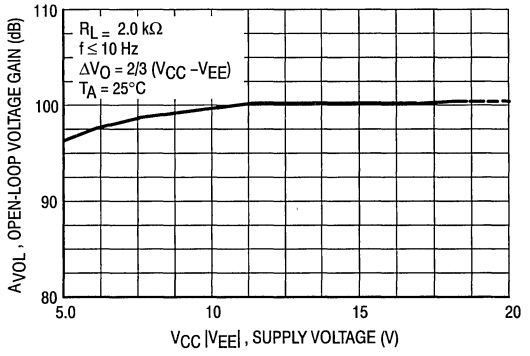


Figure 16. Open-Loop Voltage Gain versus Supply Voltage



2

Figure 17. Open-Loop Voltage Gain versus Temperature

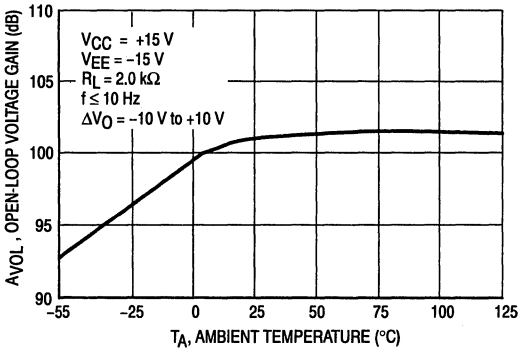


Figure 18. Output Impedance versus Frequency

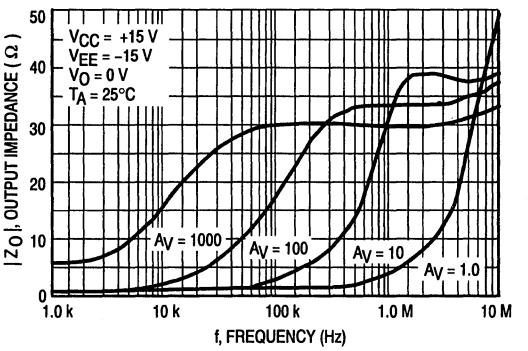


Figure 19. Channel Separation versus Frequency

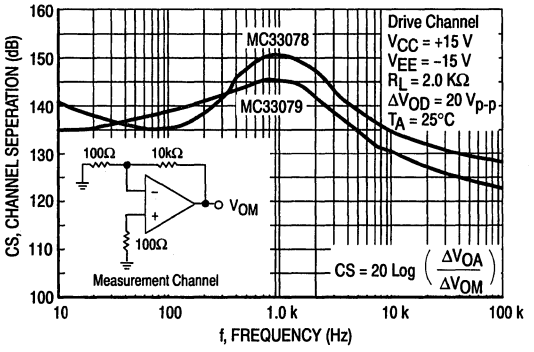


Figure 20. Total Harmonic Distortion versus Frequency

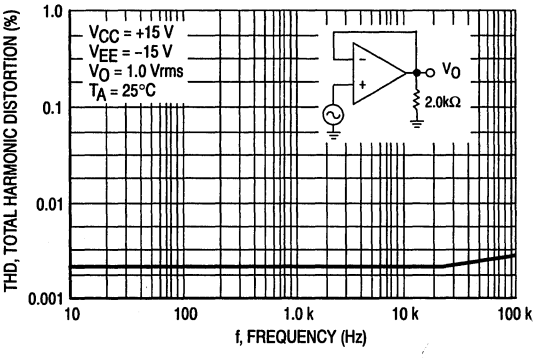


Figure 21. Total Harmonic Distortion versus Output Voltage

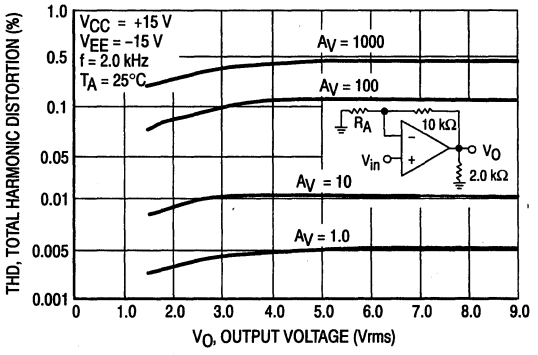


Figure 22. Slew Rate versus Supply Voltage

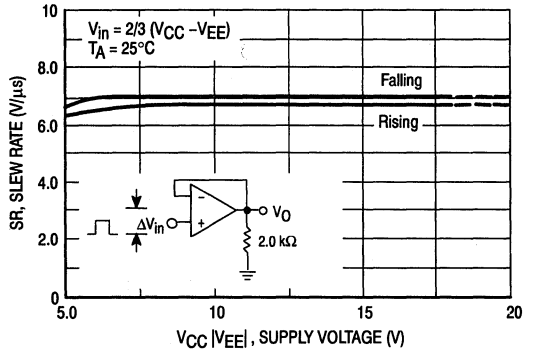


Figure 23. Slew Rate versus Temperature

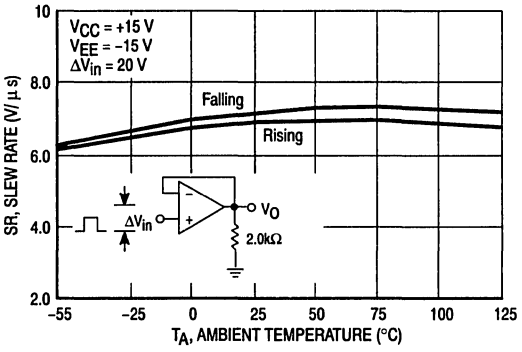


Figure 24. Voltage Gain and Phase versus Frequency

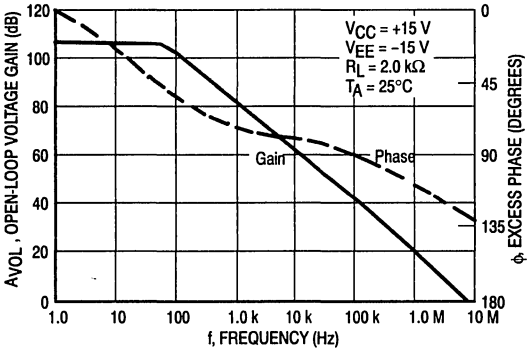


Figure 25. Open-Loop Gain Margin and Phase Margin versus Load Capacitance

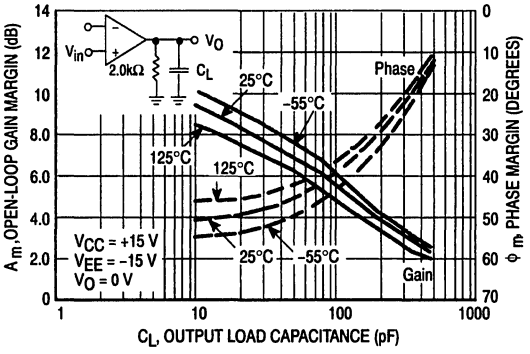


Figure 26. Overshoot versus Output Load Capacitance

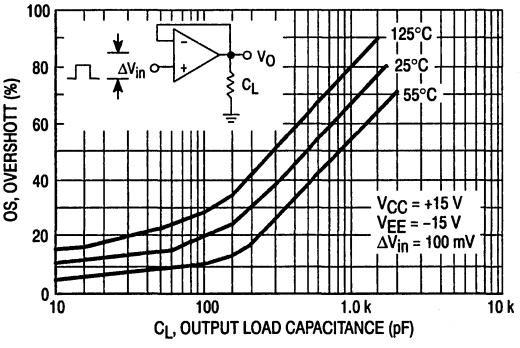


Figure 27. Input Referred Noise Voltage and Current versus Frequency

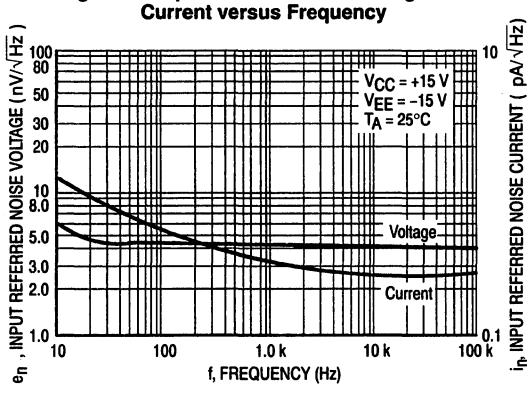
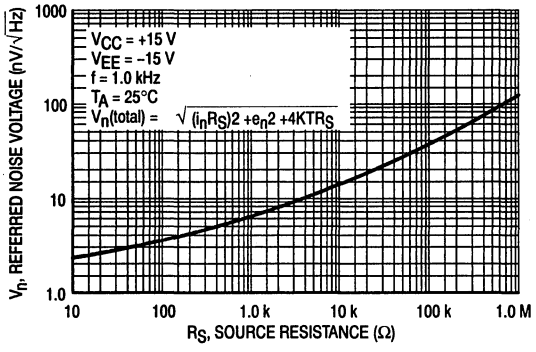


Figure 28. Total Input Referred Noise Voltage versus Source Resistnce



2

Figure 29. Phase Margin and Gain Margin versus Differential Source Resistance

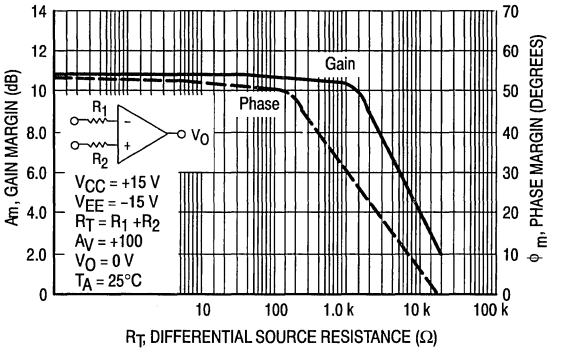


Figure 30. Inverting Amplifier Slew Rate

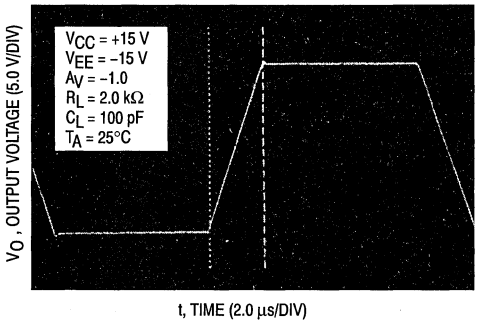


Figure 31. Noninverting Amplifier Slew Rate

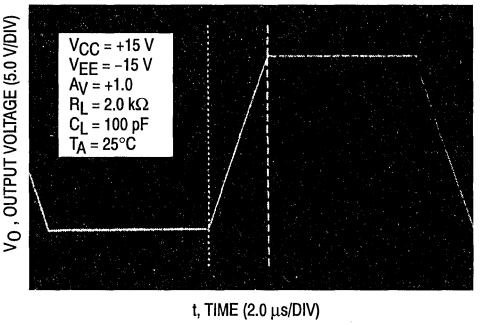


Figure 32. Noninverting Amplifier Overshoot

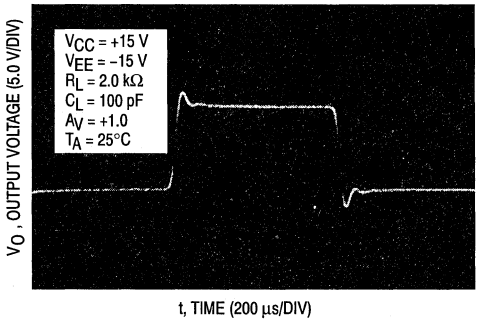


Figure 33. Low Frequency Noise Voltage versus Time

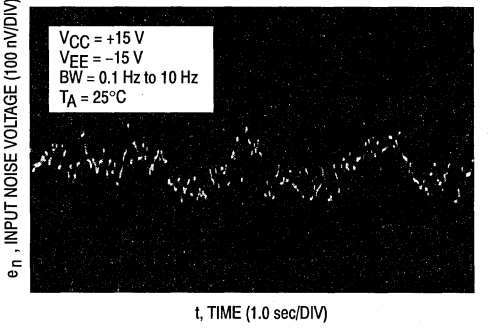
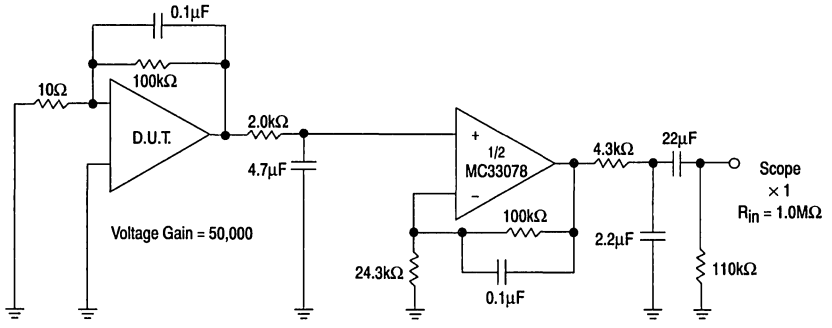


Figure 34. Voltage Noise Test Circuit
(0.1 Hz to 10 Hz_{p-p})



Note: All capacitors are non-polarized.

MC33102

DUAL SLEEP-MODE™ OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

Advance Information

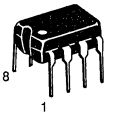
Sleep-Mode™ Two-State, Micropower Operational Amplifier

The MC33102 dual operational amplifier is an innovative design concept employing Sleep-Mode™ technology. Sleep-Mode amplifiers have two separate states, a sleepmode and an awakemode. In sleepmode, the amplifier is active and waiting for an input signal. When a signal is applied causing the amplifier to source or sink 160 μA (typically) to the load, it will automatically switch to the awakemode which offers higher slew rate, gain bandwidth, and drive capability.

- Two States: "Sleepmode" (Micropower) and "Awakemode" (High Performance)
- Switches from Sleepmode to Awakemode in 4.0 μs when Output Current Exceeds the Threshold Current (R_L = 600 Ω)
- Independent Sleepmode Function for Each Op Amp
- Standard Pinouts – No Additional Pins or Components Required
- Sleepmode State – Can Be Used in the Low Current Idle State as a Fully Functional Micropower Amplifier
- Automatic Return to Sleepmode when Output Current Drops Below Threshold
- No Deadband/Crossover Distortion; as Low as 1.0 Hz in the Awakemode
- Drop-in Replacement for Many Other Dual Op Amps
- ESD Clamps on Inputs Increase Reliability without Affecting Device Operation

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

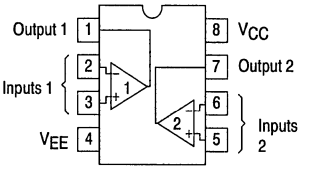
P SUFFIX
PLASTIC PACKAGE
CASE 626



TYPICAL SLEEPMODE/AWAKEMODE PERFORMANCE

Characteristic	Sleepmode (Typical)	Awakemode (Typical)	Unit
Low Current Drain	45	750	μA
Low Input Offset Voltage	0.15	0.15	mV
High Output Current Capability	0.15	50	mA
Low T.C. of Input Offset Voltage	1.0	1.0	μV/°C
High Gain Bandwidth (@20 kHz)	0.33	4.6	MHz
High Slew Rate	0.16	1.7	V/μs
Low Noise (@ 1.0 kHz)	28	9.0	$nV/\sqrt{Hz}$

PIN CONNECTIONS



(Dual Package,
Top View)

MAXIMUM RATINGS

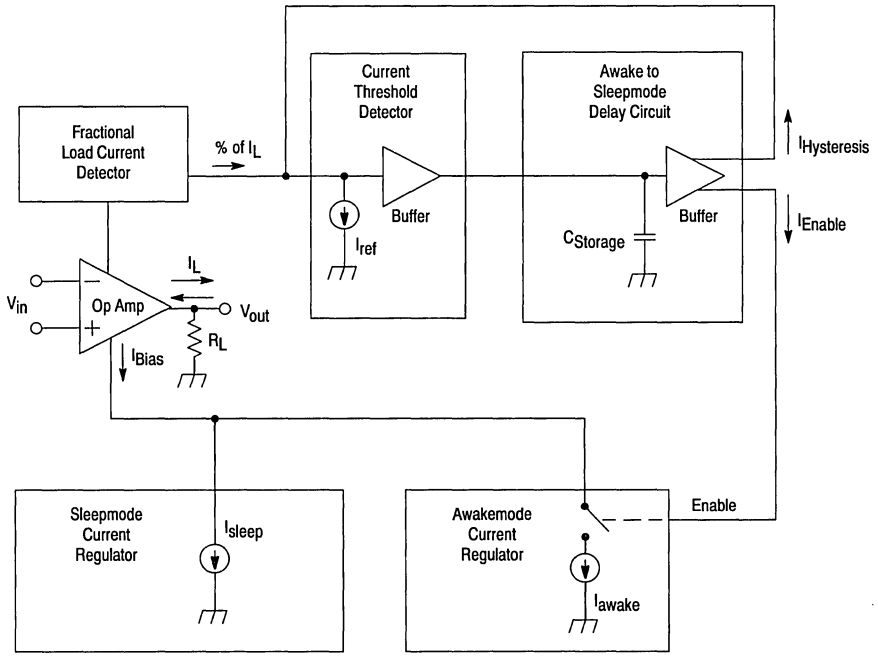
Ratings	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range Input Voltage Range	V_{IDR} V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	(Note 2)	sec
Maximum Junction Temperature Storage Temperature	T_J T_{stg}	+150 –65 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (refer to Figure 1).

ORDERING INFORMATION

Device	Temperature Range	Package
MC33102D	–40° to +85°C	SO-8
MC33102P		Plastic DIP

Simplified Block Diagram



DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	2	$\lvert V_{IO} \rvert$				mV
Sleepmode						
T_A = +25°C			—	0.15	2.0	
T_A = −40° to +85°C			—	—	3.0	
Awakemode						
T_A = +25°C			—	0.15	2.0	
T_A = −40° to +85°C			—	—	3.0	
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	3	$\Delta V_{IO}/\Delta T$				μV/°C
T_A = −40° to +85°C (Sleepmode and Awakemode)			—	1.0	—	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	4, 6	I_{IB}				nA
Sleepmode						
T_A = +25°C			—	8.0	50	
T_A = −40° to +85°C			—	—	60	
Awakemode						
T_A = +25°C			—	100	500	
T_A = −40° to +85°C			—	—	600	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	—	$\lvert I_{IO} \rvert$				nA
Sleepmode						
T_A = +25°C			—	0.5	5.0	
T_A = −40° to +85°C			—	—	6.0	
Awakemode						
T_A = +25°C			—	5.0	50	
T_A = −40° to +85°C			—	—	60	

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	5	V_{ICR}				V
Sleepmode and Awakemode			–13	–14.8	—	
			—	+14.2	+13	
Large Signal Voltage Gain	7	A_{VOL}				kV/V
Sleepmode (RL = 1.0 MΩ)						
T_A = +25°C			25	200	—	
T_A = –40° to +85°C			15	—	—	
Awakemode (V_O = ±10 V, R_L = 600 Ω)						
T_A = +25°C			50	700	—	
T_A = –40° to +85°C			25	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)	8, 9, 10					V
Sleepmode (V_{CC} = +15 V, V_{EE} = –15 V)						
R_L = 1.0 MΩ		V_{O+}	+13.5	+14.2	—	
R_L = 1.0 MΩ		V_{O-}	—	–14.2	–13.5	
Awakemode (V_{CC} = +15 V, V_{EE} = –15 V)						V
R_L = 600 Ω		V_{O+}	+12.5	+13.6	—	
R_L = 600 Ω		V_{O-}	—	–13.6	–12.5	
R_L = 2.0 kΩ		V_{O+}	+13.3	+14	—	
R_L = 2.0 kΩ		V_{O-}	—	–14	–13.3	
Awakemode (V_{CC} = +2.5 V, V_{EE} = –2.5 V)						
R_L = 600 Ω		V_{O+}	+1.1	+1.6	—	
R_L = 600 Ω		V_{O-}	—	–1.6	–1.1	
Common Mode Rejection (V_{CM} = ±13 V)	11	CMR				dB
Sleepmode and Awakemode			80	90	—	
Power Supply Rejection (V_{CC}/V_{EE} = +15 V/–15 V, 5.0 V/–15 V, +15 V/–5.0 V)	12	PSR				dB
Sleepmode and Awakemode			80	100	—	
Output Transition Current	13, 14					µA
Sleepmode to Awakemode (Source/Sink)		$\lvert I_{TH1} \rvert$				
(V_S = ±15 V)			200	160	—	
(V_S = ±2.5 V)			250	200	—	
Awakemode to Sleepmode (Source/Sink)		$\lvert I_{TH2} \rvert$				
(V_S = ±15 V)			—	142	90	
(V_S = ±2.5 V)			—	180	140	
Output Short Circuit Current (Awakemode) (V_{ID} = ±1.0 V, Output to Ground)	15, 16	$\lvert I_{SC} \rvert$				mA
Source			50	110	—	
Sink			50	110	—	
Power Supply Current (per Amplifier) (A_{CL} = 1, V_O = 0V)	17	I_D				µA
Sleepmode (V_S = ±15 V)						
T_A = +25°C			—	45	65	
T_A = –40° to +85°C			—	48	70	
Sleepmode (V_S = ±2.5 V)						
T_A = +25°C			—	38	65	
T_A = –40° to +85°C			—	42	—	
Awakemode (V_S = ±15 V)						
T_A = +25°C			—	750	800	
T_A = –40° to +85°C			—	800	900	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −5.0 V to +5.0 V, C_L = 50 pF, A_V = 1.0)	18	SR				V/μs
Sleepmode (R_L = 1.0 MΩ)			0.10	0.16	—	
Awakemode (R_L = 600 Ω)			1.0	1.7	—	
Gain Bandwidth Product	19	GBW				MHz
Sleepmode (f = 10 kHz)			0.25	0.33	—	
Awakemode (f = 20 kHz)			3.5	4.6	—	
Sleepmode to Awakemode Transition Time	20, 21	t_{tr1}				μs
(A_{CL} = 0.1, V_{in} = 0 V to +5.0 V)						
R_L = 600 Ω			—	4.0	—	
R_L = 10 kΩ			—	15	—	
Awakemode to Sleepmode Transition Time	22	t_{tr2}	—	1.5	—	sec
Unity Gain Frequency (Open-Loop)		f_U				kHz
Sleepmode (R_L = 100 kΩ, C_L = 0 pF)			—	200	—	
Awakemode (R_L = 600 Ω, C_L = 0 pF)			—	2500	—	
Gain Margin	23, 25	A_M				dB
Sleepmode (R_L = 100 kΩ, C_L = 0 pF)			—	13	—	
Awakemode (R_L = 600 Ω, C_L = 0 pF)			—	12	—	
Phase Margin	24, 26	$\varnothing_M$				Degrees
Sleepmode (R_L = 100 kΩ, C_L = 0 pF)			—	60	—	
Awakemode (R_L = 600 Ω, C_L = 0 pF)			—	60	—	
Channel Separation (f = 100 Hz to 20 kHz)	29	CS				dB
Sleepmode and Awakemode			—	120	—	
Power Bandwidth (Awakemode)		BW_P				kHz
(V_O = 10 V_{p-p}, R_L = 100 kΩ, THD ≤ 1%)			—	20	—	
Total Harmonic Distortion (V_O = 2.0 V_{p-p}, A_V = 1.0)	30	THD				%
Awakemode (R_L = 600 Ω)						
f = 1.0 kHz			—	0.005	—	
f = 10 kHz			—	0.016	—	
f = 20 kHz			—	0.031	—	
DC Output Impedence (V_O = 0 V, A_V = 10, I_Q = 10 μA)	31	R_O				Ω
Sleepmode			—	1.0 k	—	
Awakemode			—	96	—	
Differential Input Resistance (V_{CM} = 0 V)		R_{in}				MΩ
Sleepmode			—	1.3	—	
Awakemode			—	0.17	—	
Differential Input Capacitance (V_{CM} = 0 V)		C_{in}				pF
Sleepmode			—	0.4	—	
Awakemode			—	4.0	—	
Equivalent Input Noise Voltage (f = 1.0 kHz, R_S = 100 Ω)	32	e_n				nV/√Hz
Sleepmode			—	28	—	
Awakemode			—	9.0	—	
Equivalent Input Noise Current (f = 1.0 kHz)	33	i_n				pA/√Hz
Sleepmode			—	0.01	—	
Awakemode			—	0.05	—	

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Figure 1. Maximum Power Dissipation versus Temperature

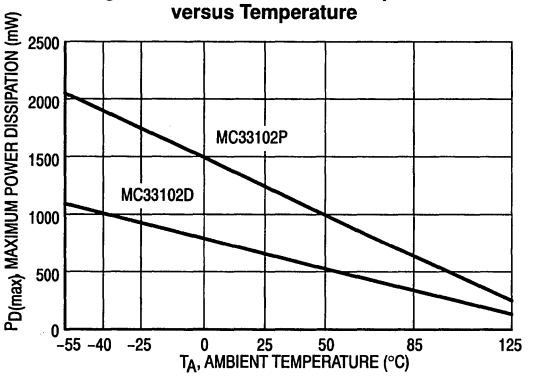

Figure 2. Distribution of Input Offset Voltage

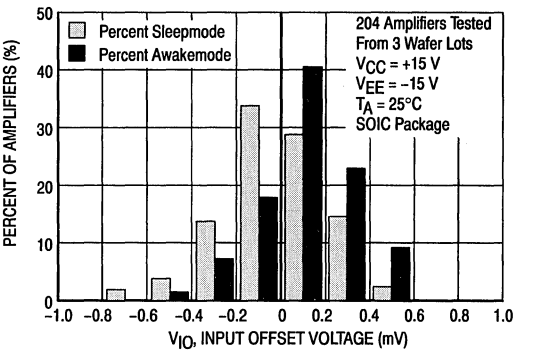

Figure 3. Input Offset Voltage Temperature Coefficient Distribution

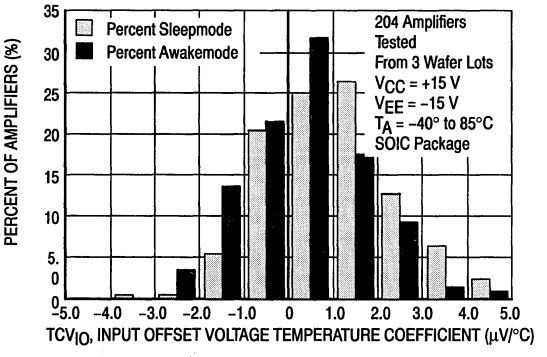

Figure 4. Input Bias Current versus Common Mode Input Voltage

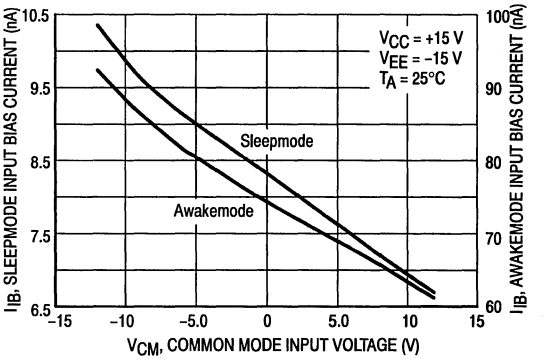

Figure 5. Input Common Mode Voltage Range versus Temperature

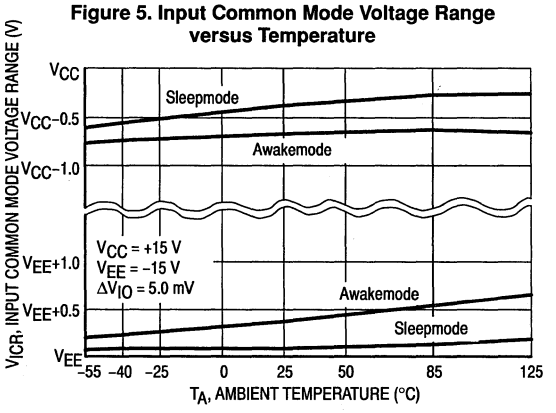

Figure 6. Input Bias Current versus Temperature

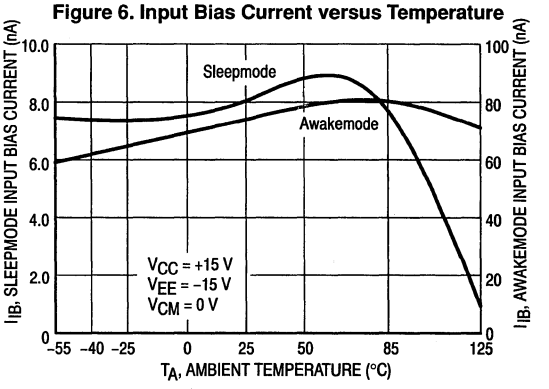

Figure 7. Open-Loop Voltage Gain versus Temperature

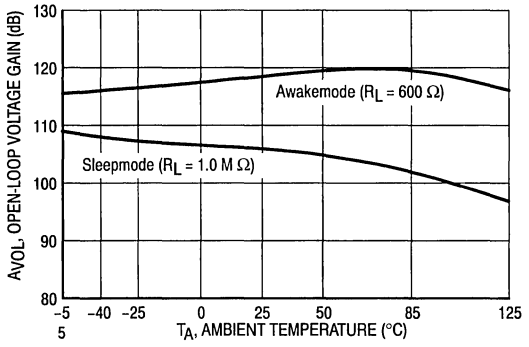

Figure 8. Output Voltage Swing versus Supply Voltage

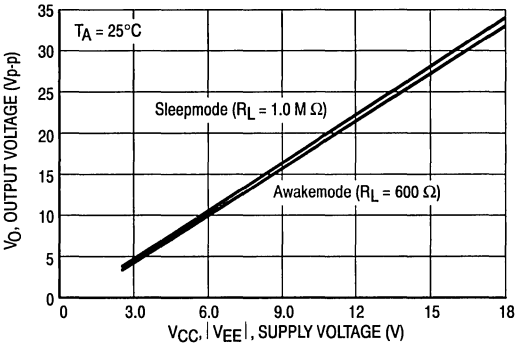

Figure 9. Output Voltage versus Frequency

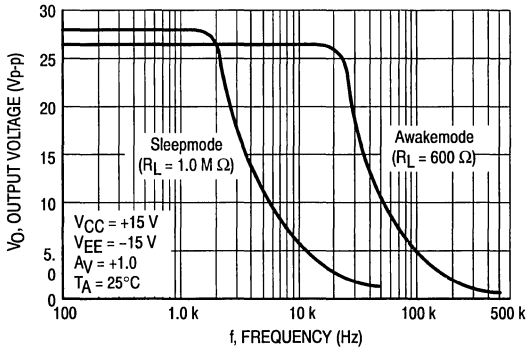

Figure 10. Maximum Peak-to-Peak Output Voltage Swing versus Load Resistance

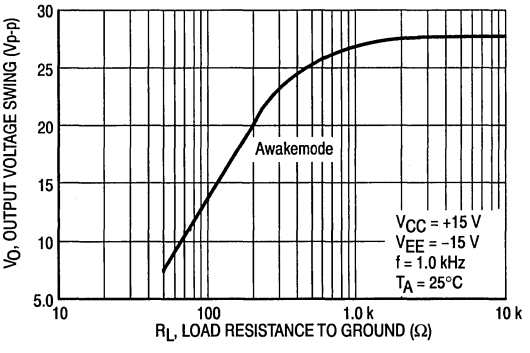

Figure 11. Common Mode Rejection versus Frequency

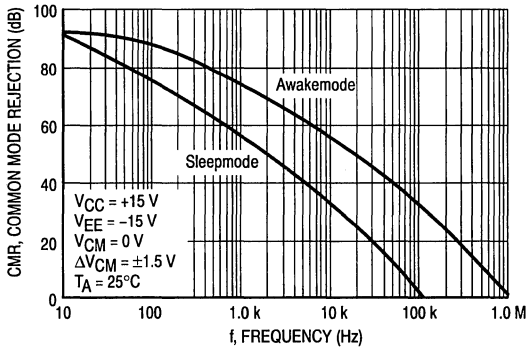

Figure 12. Power Supply Rejection versus Frequency

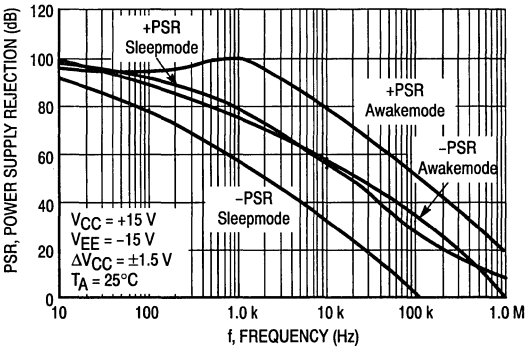

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Figure 13. Sleepmode to Awakemode Current Threshold versus Supply Voltage

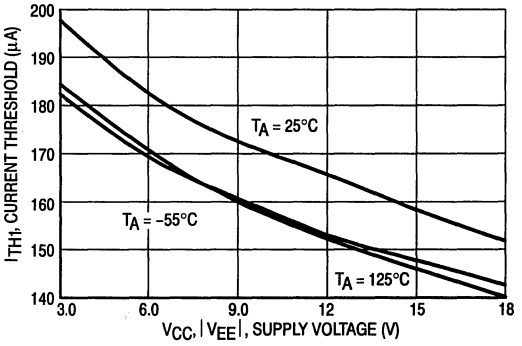

Figure 14. Awakemode to Sleepmode Current Threshold versus Supply Voltage

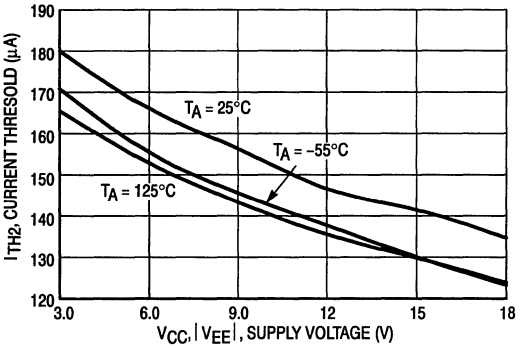

Figure 15. Output Short Circuit Current versus Output Voltage

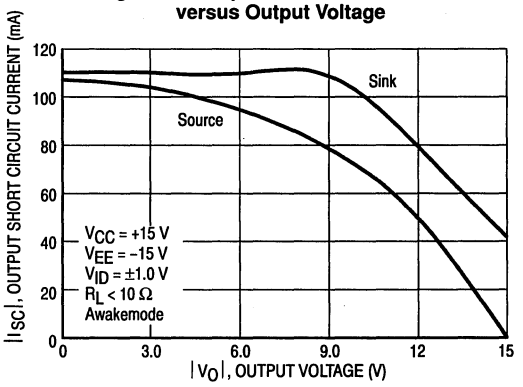

Figure 16. Output Short Ciruit Current versus Temperature

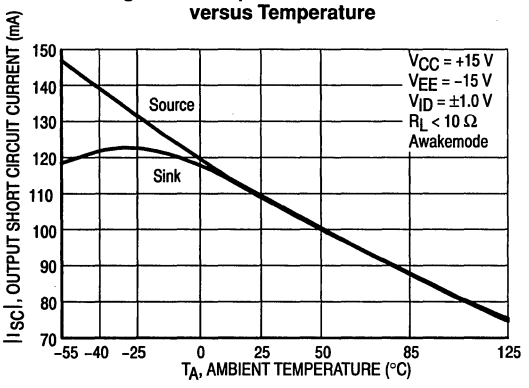

Figure 17. Power Supply Current Per Amplifier versus Temperature

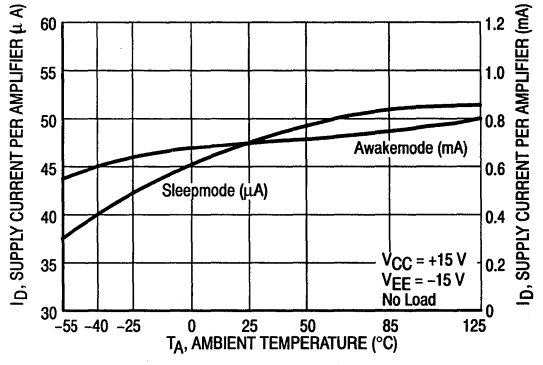

Figure 18. Slew Rate versus Temperature

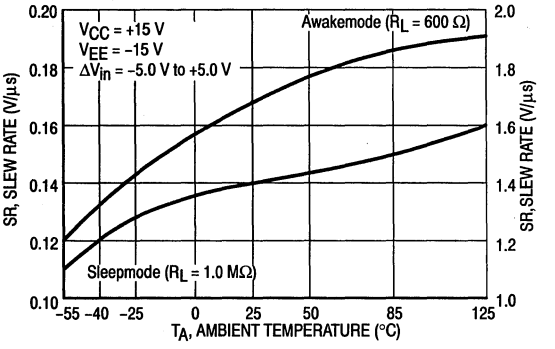

Figure 19. Gain Bandwidth Product versus Temperature

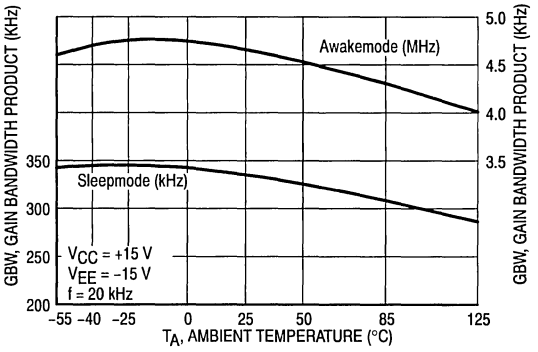

Figure 20. Sleepmode to Awakemode Transition Time

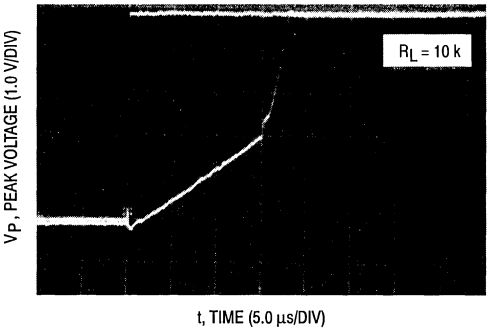

Figure 21. Sleepmode to Awakemode Transition Time

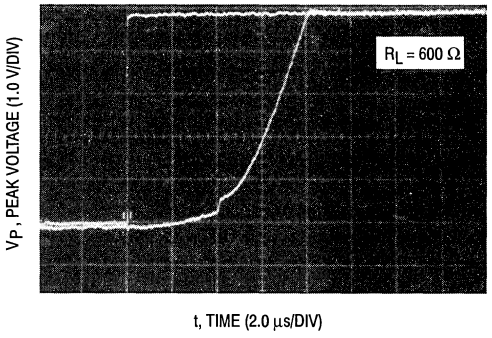

Figure 22. Awakemode to Sleepmode Transition Time versus Supply Voltage

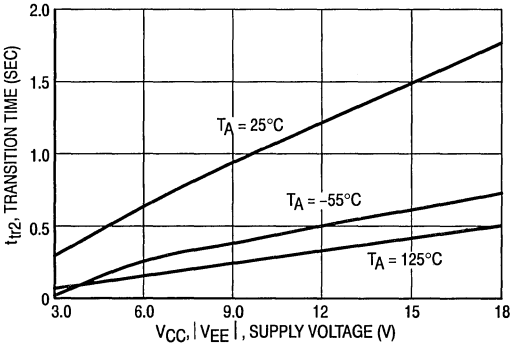

Figure 23. Gain Margin versus Differential Source Resistance

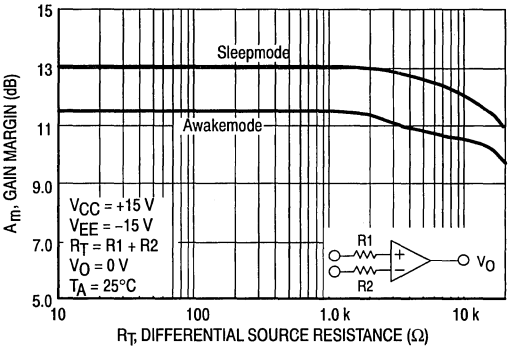

Figure 24. Phase Margin versus Differential Source Resistance

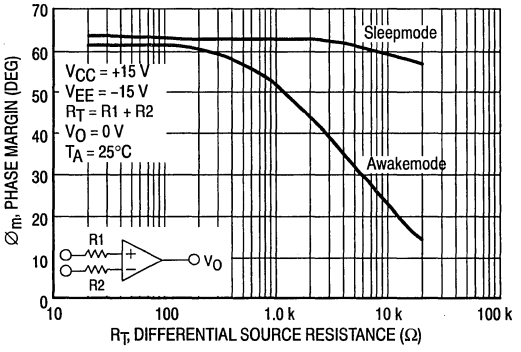

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Figure 25. Open-Loop Gain Margin versus Output Load Capacitance

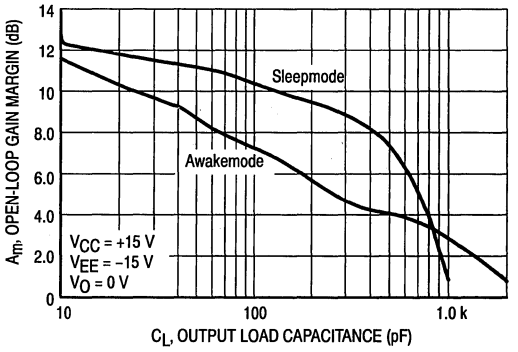

Figure 26. Phase Margin versus Output Load Capacitance

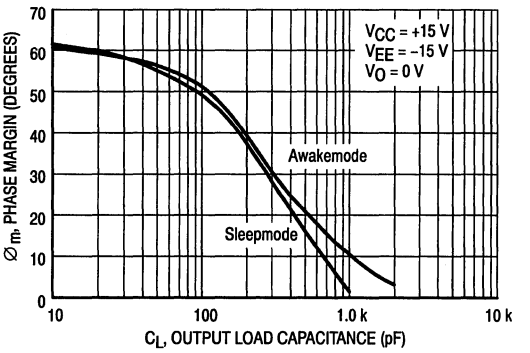

Figure 27. Sleepmode Voltage Gain and Phase versus Frequency

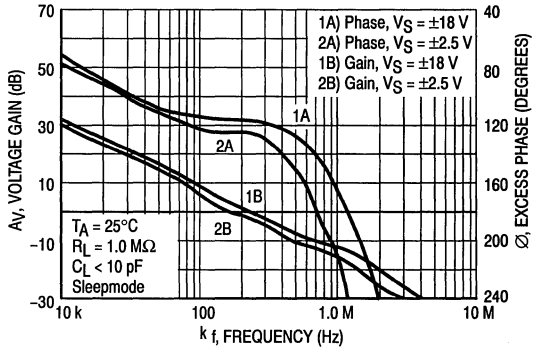

Figure 28. Awakemode Voltage Gain and Phase versus Frequency

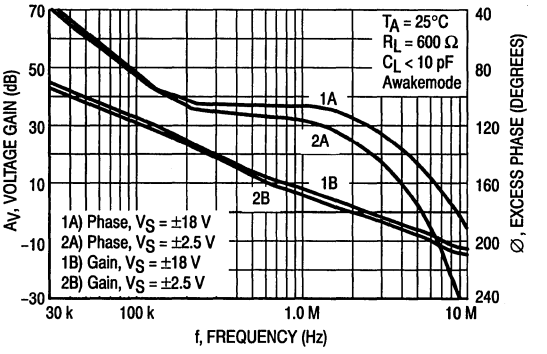

Figure 29. Channel Separation versus Frequency

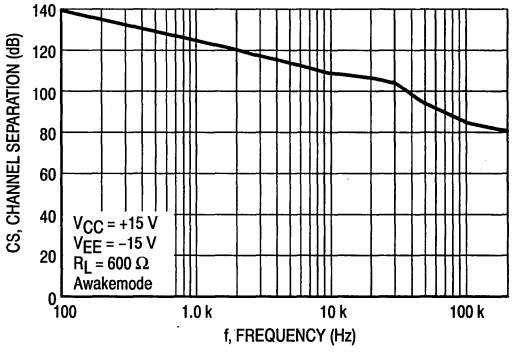

Figure 30. Total Harmonic Distortion versus Frequency

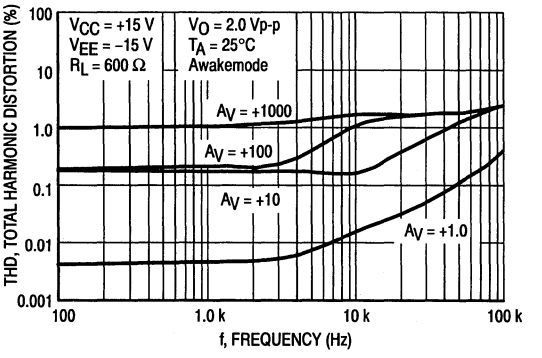

Figure 31. Awakemode Output Impedence versus Frequency

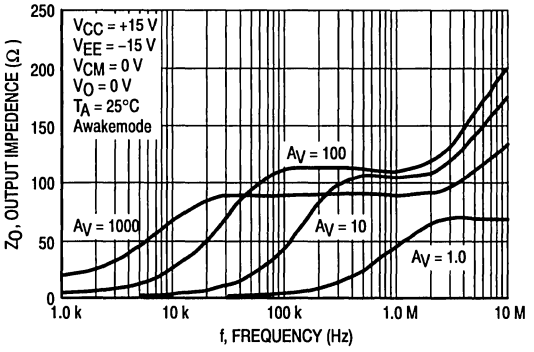

Figure 32. Input Referred Noise Voltage versus Frequency

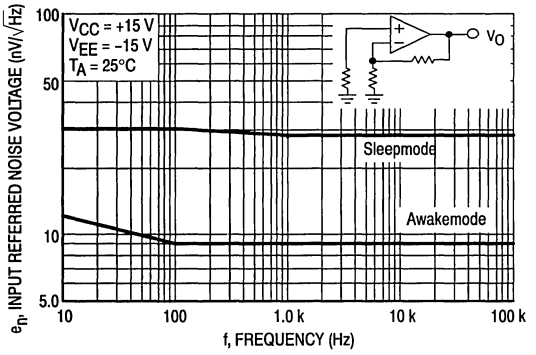

Figure 33. Current Noise versus Frequency

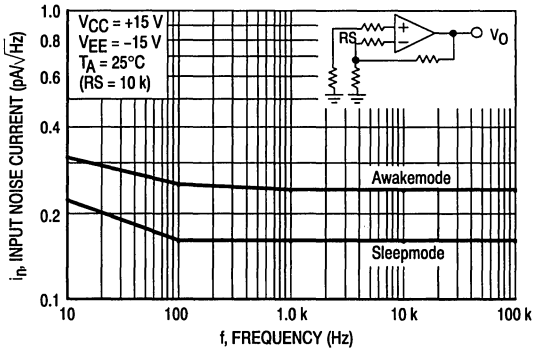

Figure 34. Percent Overshoot versus Load Capacitance

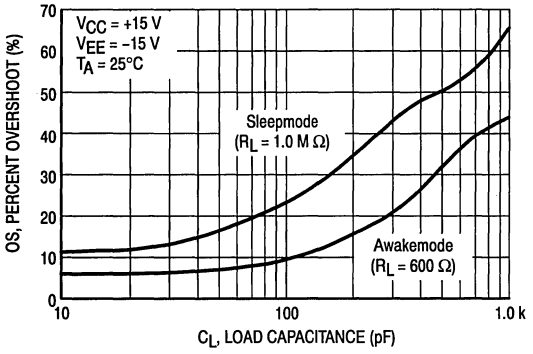

Figure 35. Sleepmode Large Signal Transient Response

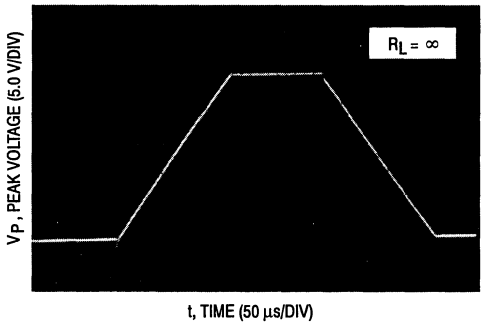

Figure 36. Awakemode Large Signal Transient Response

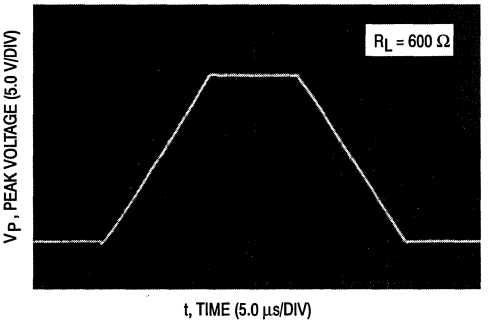

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Figure 37. Sleepmode Small Signal Transient Response

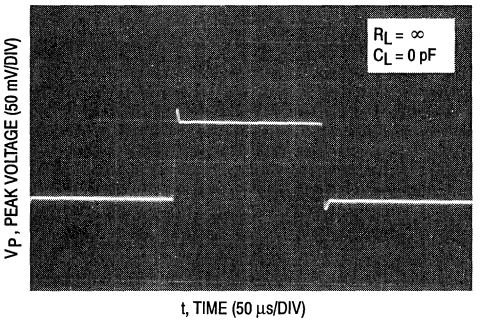
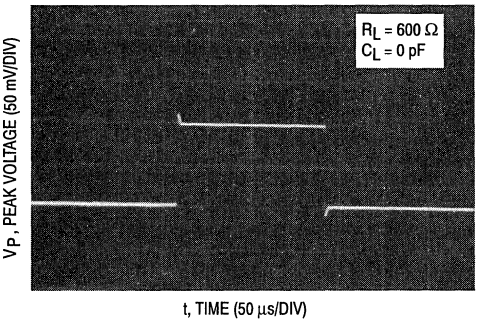


Figure 38. Awakemode Small Signal Transient Response



CIRCUIT INFORMATION

The MC33102 was designed primarily for applications where high performance (which requires higher current drain) is required only part of the time. The two-state feature of this op amp enables it to conserve power during idle times, yet to be powered up and ready for an input signal. Possible applications include laptop computers, automotive, cordless phones, baby monitors, and battery operated test equipment. Although most applications will require low power consumption, this device can be used in any application where better efficiency and higher performance is needed.

The Sleep-Mode™ amplifier has two states; a sleepmode and an awakemode. In the sleepmode state the amplifier is active and functions as a typical micropower op amp. When a signal is applied to the amplifier causing it to source or sink sufficient current (see Figure 13), the amplifier will automatically switch to the awakemode. See Figures 20 and 21 for transition times with 600 Ω and 10 kΩ loads.

The awakemode uses higher drain current to provide a high slew rate, gain bandwidth, and output current capability. In the awakemode, this amplifier can drive 27 Vp-p into a 600 Ω load with $V_S = \pm 15$ V.

An internal delay circuit is used to prevent the amplifier from returning to the sleepmode at every zero crossing. This delay circuit also eliminates the crossover distortion commonly found in micropower amplifiers. This amplifier can process frequencies as low as 1.0 Hz without the amplifier returning to sleepmode, depending on the load.

The first stage PNP differential amplifier provides low noise performance in both the sleep and awake modes, and an all NPN output stage provides symmetrical source and sink AC frequency response.

APPLICATIONS INFORMATION

The MC33102 will begin to function at power supply voltages as low as $V_S = \pm 1.0$ V at room temperature. (At this voltage, the output voltage swing will be limited to a few hundred millivolts). The input voltages must range between V_{CC} and V_{EE} supply voltages as shown in the maximum rating table. Specifically, **allowing the input to go more negative than 0.3 V below V_{EE} may cause product damage.** Also, exceeding the input common mode voltage range on either input may cause phase reversal, even if the inputs are between V_{CC} and V_{EE}.

When power is initially applied, the part may start to operate in the awakemode. This is because of the currents generated due to charging of internal capacitors. When this occurs and the sleepmode state is desired, the user will have to wait approximately 1.5 seconds before the device will switch back to the sleepmode. To prevent this from occurring, ramp the power supplies from 1.0 V to full supply. Notice that the device is more prone to switch into the awakemode when V_{EE} is adjusted than with a similar change in V_{CC}.

The amplifier is designed to switch from sleepmode to awakemode whenever the output current exceeds a preset current threshold (I_{TH}) of approximately 160 µA. As a result, the output switching threshold voltage (V_{ST}) is controlled by the output loading resistance (R_L). This loading can be a load resistor, feedback resistors, or both. Then:

$$V_{ST} = (160\ \mu A) * R_L$$

Large valued load resistors require a large output voltage to switch, but reduce unwanted transitions to the awakemode. For instance, in cases where the amplifier is connected with a large closed-loop gain (A_{CL}), the input offset voltage (V_{IO}) is multiplied by the gain at the output and could produce an output voltage exceeding V_{ST} with no input signal applied.

Small values of R_L allow rapid transition to the awakemode because most of the transition time is consumed slewing in the sleepmode until V_{ST} is reached (see Figures 20, 21). The output switching threshold voltage V_{ST} is higher for larger values of R_L, requiring the amplifier to slew longer in the slower sleepmode state before switching to the awakemode.

The transition time (t_{tr1}) required to switch from sleep to awake mode is:

$$t_{tr1} = t_D + I_{TH} (R_L/SR_{sleepmode})$$

where: t_D = Amplifier delay (<1.0 μs)
I_{TH} = Output threshold current for mode transition (160 μA)
R_L = Load resistance
$SR_{sleepmode}$ = Sleepmode slew rate (0.16 V/μs)

Although typically 160 μA, I_{TH} varies with supply voltage and temperature. In general, any current loading on the output which causes a current greater than I_{TH} to flow will switch the amplifier into the awakemode. This includes transition currents such as that generated by charging load capacitances. In fact, the maximum capacitance that can be driven while attempting to remain in the sleepmode is approximately 1000 pF.

$$C_{L(max)} = I_{TH}/SR_{sleepmode}$$
$$= 160\ \mu A/(0.16\ V/\mu s)$$
$$= 1000\ pF$$

Any electrical noise seen at the output of the MC33102 may also cause the device to transition to the awakemode. To minimize this problem, a resistor may be added in series with the output of the device (inserted as close to the device as possible) to isolate the op amp from both parasitic and load capacitance.

The awakemode to sleepmode transition time is controlled by an internal delay circuit, which is necessary to prevent the amplifier from going to sleep during every zero crossing. This time is a function of supply voltage and temperature as shown in Figure 22.

Gain bandwidth product (GBW) in both modes is an important system design consideration when using a sleepmode amplifier. The amplifier has been designed to obtain the maximum GBW in both modes. "Smooth" AC transitions between modes with no noticeable change in the amplitude of the output voltage waveform will occur as long as the closed-loop gains (A_{CL}) in both modes are substantially equal at the frequency of operation. For smooth AC transitions:

$$(A_{CLsleepmode})\ (BW) < GBW_{sleepmo}$$

where: $A_{CLsleepmode}$ = Closed-loop gain in the sleepmode
BW = The required system bandwidth or operating frequency

TESTING INFORMATION

To determine if the MC33102 is in the awakemode or the sleepmode, the power supply currents (I_{D+} and I_{D-}) must be measured. When the magnitude of **either** power supply current exceeds 400 μA the device is in the awakemode. When the magnitudes of both supply currents are less than 400 μA, the device is in the sleepmode. Since the total supply current is typically ten times higher in the awakemode than the sleepmode, the two states are easily distinguishable.

The measured value of I_{D+} equals the I_D of both devices (for a dual op amp) plus the output source current of device A and the output source current of device B. Similarly, the measured value of I_{D-} is equal to the I_{D-} of both devices plus the output sink current of each device. I_{out} is the sum of the currents caused by both the feedback loop and load resistance. The total I_{out} needs to be subtracted from the measured I_D to obtain the correct I_D of the dual op amp.

An accurate way to measure the awakemode I_{out} current on automatic test equipment is to remove the I_{out} current on both Channel A and B. Then measure the I_D values before the device goes back to the sleepmode state. The transition will take typically 1.5 seconds with ±15 V power supplies.

The large signal sleepmode testing in the characterization was accomplished with a 1.0 MΩ load resistor which ensured the device would remain in sleepmode despite large voltage swings.

MC33171, MC35171
MC33172, MC35172
MC33174, MC35174

Low Power, Single Supply Operational Amplifiers

Quality bipolar fabrication with innovative design concepts are employed for the MC33171/72/74, MC35171/72/74 series of monolithic operational amplifiers. These devices operate at 180 μA per amplifier and offer 1.8 MHz of gain bandwidth product and 2.1 V/μs slew rate without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage includes ground potential (V_{EE}). With a Darlington input stage, these devices exhibit high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33171/72/74, MC35171/72/74 are specified over the industrial/automotive or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in the plastic and ceramic DIP as well as the SOIC surface mount packages.

- Low Supply Current: 180 μA (Per Amplifier)
- Wide Supply Operating Range: 3.0 V to 44 V or ±1.5 V to ±22 V
- Wide Input Common Mode Range, Including Ground (V_{EE})
- Wide Bandwidth: 1.8 MHz
- High Slew Rate: 2.1 V/μs
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing: –14.2 V to +14.2 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 pF to 500 pF
- Low Total Harmonic Distortion: 0.03%
- Excellent Phase Margin: 60°C
- Excellent Gain Margin: 15 dB
- Output Short Circuit Protection
- ESD Diodes Provide Input Protection for Dual and Quad

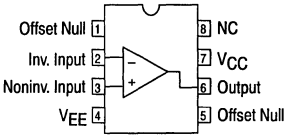
DUAL

P SUFFIX
PLASTIC PACKAGE
CASE 626

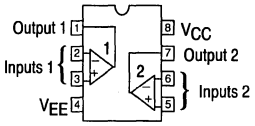
U SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS

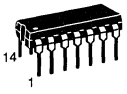


(Single, Top View)



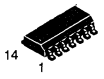
(Top View)

QUAD



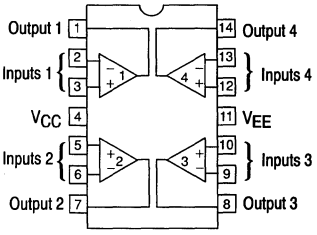
P SUFFIX
PLASTIC PACKAGE
CASE 646

U SUFFIX
CERAMIC PACKAGE
CASE 632



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

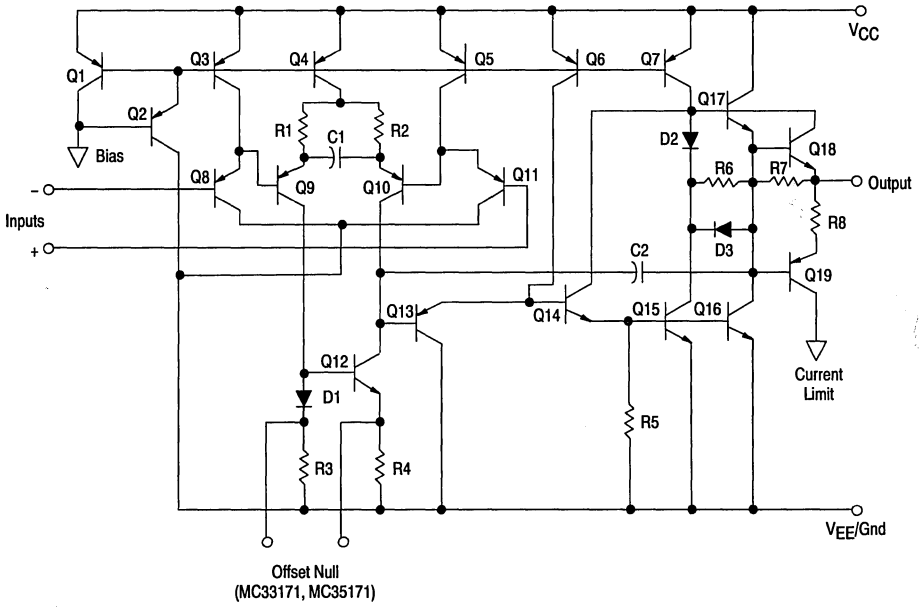
Op Amp Function	Device	Temperature Range	Package
Single	MC33171D	–40° to +85°C	SO-8
	MC35171U	–55° to +125°C	Ceramic DIP
	MC33171P	–40° to +85°C	Plastic DIP
Dual	MC33172D	–40° to +85°C	SO-8
	MC35172U	–55° to +125°C	Ceramic DIP
	MC33172P	–40° to +85°C	Plastic DIP
Quad	MC33174D	–40° to +85°C	SO-8
	MC35174L	–55° to +125°C	Ceramic DIP
	MC33174P	–40° to +85°C	Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}/V_{EE}	±22	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Ambient Temperature Range MC35171/MC35172/MC35174 MC33171/MC33172/MC33174	T_A	 –55 to +125 –40 to +85	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 –65 to +150 –55 to +125	°C

NOTES: 1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

Equivalent Circuit Schematic
(Each Amplifier)



2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L connected to ground, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} = 0 V)	V_{IO}				mV
V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C		—	2.0	4.5	
V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C		—	2.5	5.0	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high}		—	—	6.5	
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	10	—	μV/°C
Input Bias Current (V_{CM} = 0 V)	I_{IB}				nA
T_A = +25°C		—	20	100	
T_A = T_{low} to T_{high}		—	—	200	
Input Offset Current (V_{CM} = 0 V)	I_{IO}				nA
T_A = +25°C		—	5.0	20	
T_A = T_{low} to T_{high}		—	—	40	
Large Signal Voltage Gain (V_O = ±10 V< R_L = 10 k)	A_{VOL}				V/mV
T_A = +25°C		50	500	—	
T_A = T_{low} to T_{high}		25	—	—	
Output Voltage Swing	V_{OH}				V
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 10 k, T_A = +25°C		3.5	4.3	—	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = +25°C		13.6	14.2	—	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = T_{low} to T_{high}		13.3	—	—	
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 10 k, T_A = +25°C	V_{OL}	—	0.05	0.15	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = +25°C		—	−14.2	−13.6	
V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 k, T_A = T_{low} to T_{high}		—	—	−13.3	
Output Short Circuit (T_A = +25°C)	I_{SC}				mA
Input Overdrive = 1.0 V, Output to Ground					
Source		3.0	5.0	—	
Sink		15	27	—	
Input Common Mode Voltage Range	V_{ICR}				V
T_A = +25°C		V_{EE} to (V_{CC} −1.8)			
T_A = T_{low} to T_{high}		V_{EE} to (V_{CC} −2.2)			
Common Mode Rejection Ratio (R_S ≤ 10 k) T_A = +25°C	CMRR	80	90	—	dB
Power Supply Rejection Ratio (R_S = 100 Ω) T_A = +25°C	PSRR	80	100	—	dB
Power Supply Current (Per Amplifier)	I_D				μA
V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C		—	180	250	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C		—	220	250	
V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high}		—	—	300	

NOTES: 3. T_{low} = −55°C for MC35171/MC35172/MC35174
= −40°C for MC33171/MC33172/MC33174

T_{high} = +125°C for MC35171/MC35172/MC35174
= +85°C for MC33171/MC33172/MC33174

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L connected to ground, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 10 k, C_L = 100 pF) A_V +1 A_V −1	SR	 1.6 —	 2.1 2.1	 — —	V/μs
Gain Bandwidth Product (f = 100 kHz)	GBW	1.4	1.8	—	MHz
Power Bandwidth A_V = +1.0 R_L = 10 k, V_O = 20 V_{p-p}, THD = 5%	BWp	—	35	—	kHz
Phase Margin R_L = 10 k R_L = 10 k, C_L = 100 pF	ϕ_m	 — —	 60 45	 — —	Degrees
Gain Margin R_L = 10 k R_L = 10 k, C_L = 100 pF	A_m	 — —	 15 5.0	 — —	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	32	—	nV/√Hz
Equivalent Input Noise Current (f = 1.0 kHz)	I_n	—	0.2	—	pA/√Hz
Differential Input Resistance V_{cm} = 0 V	R_{in}	—	300	—	MΩ
Input Capacitance	C_i	—	0.8	—	pF
Total Harmonic Distortion A_V = +10, R_L = 10 k, 2.0 $V_{p-p} \le V_O \le$ 20 V_{p-p}, f = 10 kHz	THD	—	0.03	—	%
Channel Separation (f = 10 kHz)	CS	—	120	—	dB
Open-Loop Output Impedance (f = 1.0 MHz)	z_o	—	100	—	Ω

Figure 1. Input Common Mode Voltage Range versus Temperature

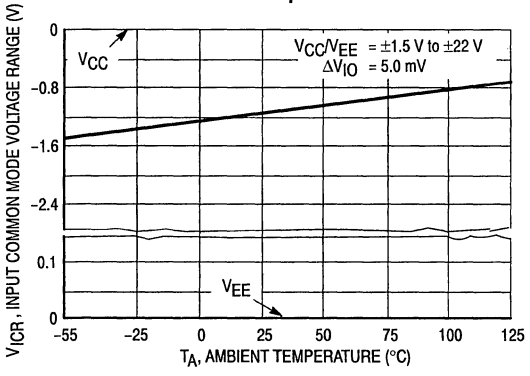
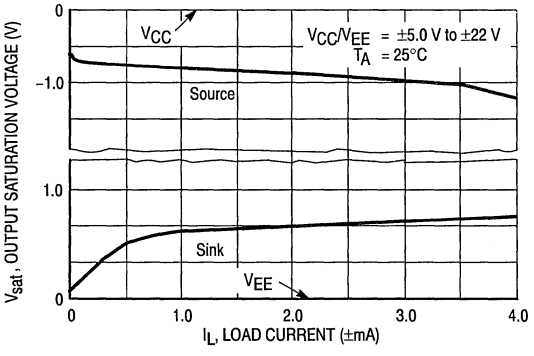


Figure 2. Split Supply Output Saturation versus Load Current



2

Figure 3. Open-Loop Voltage Gain and Phase versus Frequency

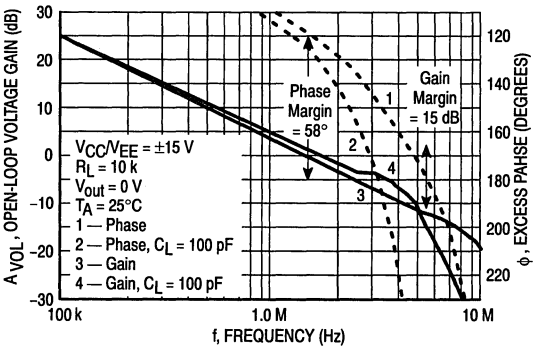


Figure 4. Phase Margin and Percent Overshoot versus Load Capacitance

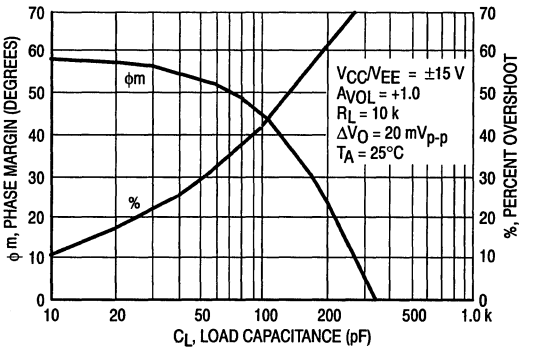


Figure 5. Normalized Gain Bandwidth Product and Slew Rate versus Temperature

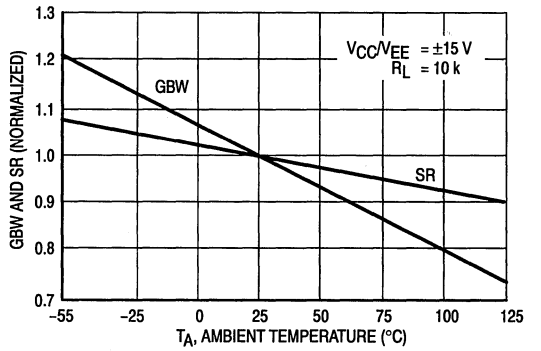


Figure 6. Small and Large Signal Transient Response

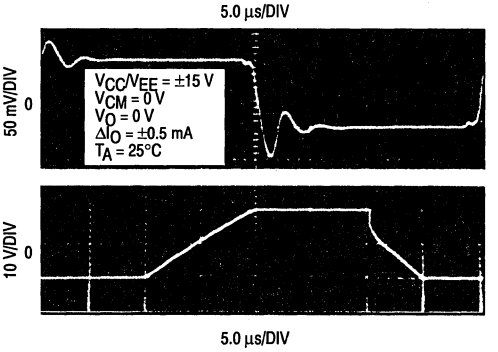


Figure 7. Output Impedance and Frequency

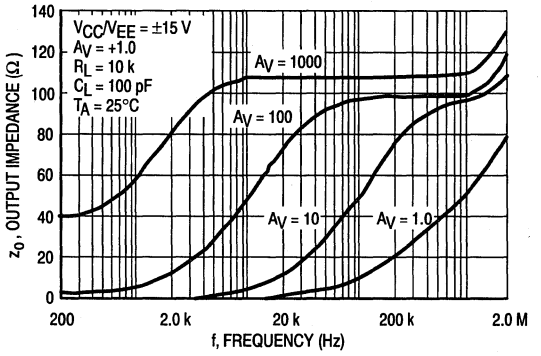
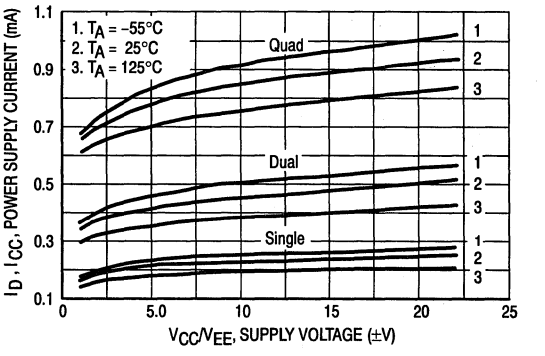


Figure 8. Supply Current versus Supply Voltage



APPLICATIONS INFORMATION
CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC33171/72/74 amplifier family is similar to low power op amp products utilizing JFET input devices, these amplifiers offer additional advantages as a result of the PNP transistor differential inputs and an all NPN transistor output stage.

Because the input common mode voltage range of this input stage includes the V_{EE} potential, single supply operation is feasible to as low as 3.0 V with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 V, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between V_{CC} and V_{EE} supply voltages as shown by the maximum rating table. In practice, although *not recommended,* the input voltages can exceed the V_{CC} voltage by approximately 3.0 V and decrease below the V_{EE} voltage by 0.3 V without causing product damage, although output phase reversal may occur. It is also possible to source up to 5.0 mA of current from V_{EE} through either inputs' clamping diode without damage or latching, but phase reversal may again occur. If at least one input is within the common mode input voltage range and the other input is within the maximum input voltage range, no phase reversal will occur. If both inputs exceed the upper common mode input voltage limit, the output will be forced to its lowest voltage state.

Since the input capacitance associated with the small geometry input device is substantially lower (0.8 pF) than that of a typical JFET (3.0 pF), the frequency response for a given input source resistance is greatly enhanced. This becomes evident in D-to-A current to voltage conversion applications where the feedback resistance can form a pole with the input capacitance of the op amp. This input pole creates a 2nd Order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DAC's). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 10 kΩ of feedback resistance, the MC33171/72/74 family can typically settle to within 1/2 LSB of 8 bits in 4.2 μs, and within 1/2 LSB of 12 bits in 4.8 μs for a 10 V step. In a standard inverting unity gain fast settling configuration, the symmetrical slew rate is typically ±2.1 V/μs. In the classic noninverting unity gain configuration the typical output positive slew rate is also 2.1 V/μs, and the corresponding negative slew rate will usually exceed the positive slew rate as a function of the fall time of the input waveform.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 kΩ load resistance can typically swing within 0.8 V of the positive rail (V_{CC}) and negative rail (V_{EE}), providing a 28.4 Vp-p swing from ±15 V supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q7, the V_{BE} of the NPN pull-up transistor Q17, and the voltage drop associated with the short circuit resistance, R5. For sink currents less than 0.4 mA, the negative swing is limited by the saturation voltage of the pull-down transistor Q15, and the voltage drop across R4 and R5. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of V_{EE}. For sink currents (> 0.4 mA), diode D3 clamps the voltage across R4. Thus the negative swing is limited by the saturation voltage of Q15, plus the forward diode drop of D3 (≈V_{EE} +1.0 V). Therefore an unprecedented peak-to-peak output voltage swing is possible for a given supply voltage as indicated by the output swing specifications.

If the load resistance is referenced to V_{CC} instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull-up capability.

Because the PNP output emitter-follower transistor has been eliminated, the MC33171/72/74 family offers a 15 mA minimum current sink capability, typically to an output voltage of (V_{EE} +1.8 V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for current switching applications.

In addition, the all NPN transistor output stage is inherently faster than PNP types, contributing to the bipolar amplifier's improved gain bandwidth product. The associated high frequency low output impedance (200 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 pF to 400 pF without oscillation in the noninverting unity gain configuration. The 60°C phase margin and 15 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The AC characteristics of the MC33171/72/74 family also allow excellent active filter capability, especially for low voltage single supply applications.

Although the single supply specification is defined at 5.0 V, these amplifiers are functional to at least 3.0 V @ 25°C. However slight changes in parametrics such as bandwidth, slew rate, and DC gain may occur.

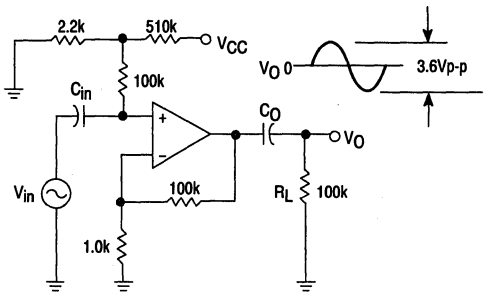
If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

As usual with most high frequency amplifiers, proper lead dress, component placement and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input/output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ±15 V supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

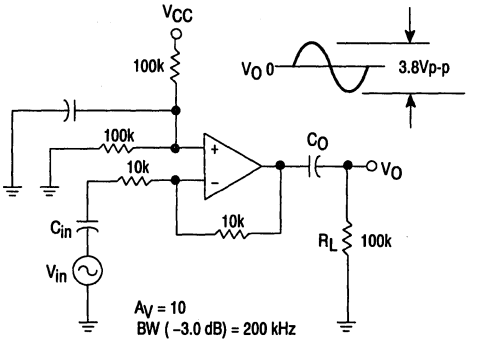
2

Figure 9. AC Coupled Noninverting Amplifier with Single +5.0 V Supply



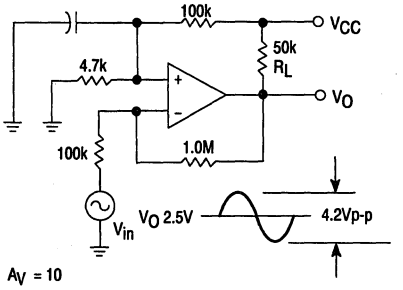
A_V = 101
BW (–3.0 dB) = 20 kHz

Figure 10. AC Coupled Inverting Amplifier with Single +5.0 V Supply



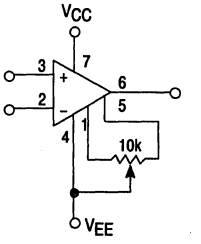
A_V = 10
BW (–3.0 dB) = 200 kHz

Figure 11. DC Coupled Inverting Amplifier Maximum Output Swing with Single +5.0 V Supply



A_V = 10
BW (–3.0 dB) = 200 kHz

Figure 12. Offset Nulling Circuit



Offset Nulling range is approximately ±80 mV with a 10 k potentiometer, MC33171/MC35171 only.

Figure 13. Active High-Q Notch Filter

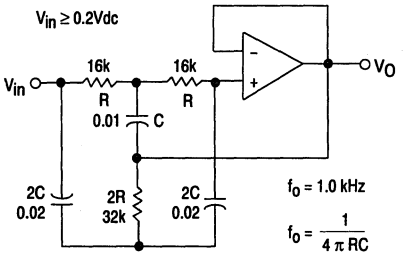
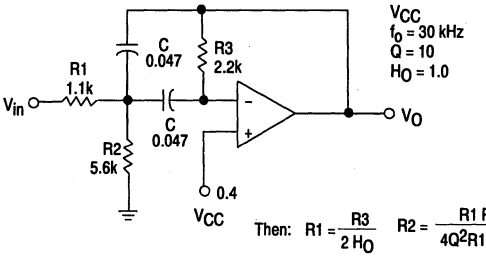


Figure 14. Active Bandpass Filter



Then: $R1 = \frac{R3}{2H_O}$ $R2 = \frac{R1\,R3}{4Q^2R1 - R3}$

Given f_0 = center frequency
A_0 = Gain at center frequency
Choose Value f_0, Q, A_0, C

$R3 = \frac{Q}{\pi f_0 C}$ $\frac{Q_0\ f_0}{GBW} < 0.1$

For less than 10% error for operational amplifier, where f_0 and GBW are expressed in Hz.

MC33178
MC33179

High Output Current Low Power, Low Noise Bipolar Operational Amplifiers

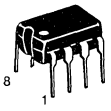
HIGH OUTPUT CURRENT LOW POWER, LOW NOISE OPERATIONAL AMPLIFIERS

The MC33178/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high performance concepts for quality audio and data signal processing applications. This device family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input offset voltage, noise and distortion. In addition, the amplifier provides high output current drive capability while consuming only 420 μA of drain current per amplifier. The NPN output stage used, exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open-loop high frequency output impedance, symmetrical source and sink AC frequency performance.

The MC33178/9 family offers both dual and quad amplifier versions, tested over the vehicular temperature range. These devices are available in DIP and SOIC packages.

- 600 Ω Output Drive Capability
- Large Output Voltage Swing
- Low Offset Voltage: 0.15 mV (Mean)
- Low T.C. of Input Offset Voltage: 2.0 μV/°C
- Low Total Harmonic Distortion: 0.0024% (@ 1.0 kHz w/600 Ω Load)
- High Gain Bandwidth: 5.0 MHz
- High Slew Rate: 2.0 V/μs
- Dual Supply Operation: ±2.0 V to ±18 V
- ESD Clamps on the Inputs Increase Ruggedness without Affecting Device Performance

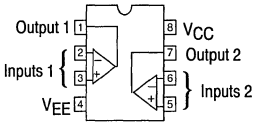
DUAL



P SUFFIX
PLASTIC PACKAGE
CASE 626

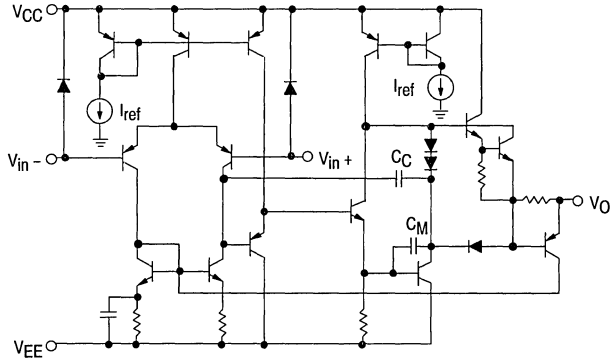
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS

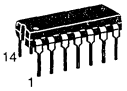


(Top View)

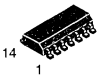
Equivalent Circuit Schematic (Each Amplifier)



QUAD

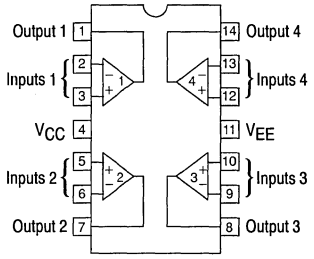


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Op Amp Function	Fully Compensated	Temperature Range	Package
Dual	MC33178D MC33178P	−40° to +85°C	SO-8 Plastic DIP
Quad	MC33179D MC33179P		SO-14 Plastic DIP

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	2	$\|V_{IO}\|$				mV
(V_{CC} = +2.5 V, V_{EE} = –2.5 V to V_{CC} = +15 V, V_{EE} = –15 V)						
T_A = +25°C			—	0.15	3.0	
T_A = –40° to +85°C			—	—	4.0	
Average Temperature Coefficient of Input Offset Voltage	2	$\Delta V_{IO}/\Delta T$				µV/°C
(R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)						
T_A = –40° to +85°C			—	2.0	—	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	3, 4	I_{IB}				nA
T_A = +25°C			—	100	500	
T_A = –40° to +85°C			—	—	600	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)		$\|I_{IO}\|$				nA
T_A = +25°C			—	5.0	50	
T_A = –40° to +85°C			—	—	60	
Common Mode Input Voltage Range	5	V_{ICR}	–13	–14	—	V
(ΔV_{IO} = 5.0 mV, V_O = 0 V)			—	+14	+13	
Large Signal Voltage Gain (V_O = –10 V to +10 V, R_L = 600 Ω)	6, 7	A_{VOL}				V/V
T_A = +25°C			50 k	200 k	—	
T_A = –40° to +85°C			25 k	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)	8, 9, 10					V
(V_{CC} = +15 V, V_{EE} = –15 V)						
R_L = 300 Ω		V_{O+}	—	+12	—	
R_L = 300 Ω		V_{O-}	—	–12	—	
R_L = 600 Ω		V_{O+}	+12	+13.6	—	
R_L = 600 Ω		V_{O-}	—	–13	–12	
R_L = 2.0 kΩ		V_{O+}	+13	+14	—	
R_L = 2.0 kΩ		V_{O-}	—	–13.8	–13	
(V_{CC} = +2.5 V, V_{EE} = –2.5 V)						
R_L = 600 Ω		V_{O+}	1.1	1.6	—	
R_L = 600 Ω		V_{O-}	—	–1.6	–1.1	
Common Mode Rejection (V_{in} = ±13 V)	11	CMR	80	110	—	dB
Power Supply Rejection	12	PSR	80	110	—	dB
V_{CC}/V_{EE} = +15 V/–15 V, +5.0 V/–15 V, +15 V/–5.0 V						
Output Short Circuit Current (V_{ID} = ±1.0 V, Output to Ground)	13, 14	I_{SC}				mA
Source (V_{CC} = 2.5 V to 15 V)			+50	+80	—	
Sink (V_{EE} = –2.5 V to –15 V)			–50	–100	—	
Power Supply Current (V_O = 0 V)	15	I_D				mA
(V_{CC} = 2.5 V, V_{EE} = –2.5 V to V_{CC} = +15 V, V_{EE} = –15 V)						
MC33178 (Dual)						
T_A = +25°C			—	—	1.4	
T_A = –40° to +85°C			—	—	1.6	
MC33179 (Quad)						
T_A = +25°C			—	1.7	2.4	
T_A = –40° to +85°C			—	—	2.6	

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See power dissipation performance characteristic, Figure 1.)

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0 V)	16, 31	SR	1.2	2.0	—	V/μs
Gain Bandwidth Product (f = 100 kHz)	17	GBW	2.5	5.0	—	MHz
AC Voltage Gain (R_L = 600 Ω, V_O = 0 V, f = 20 kHz)	18, 19	A_{VO}	—	50	—	dB
Unity Gain Frequency (Open-Loop) (R_L = 600 Ω, C_L = 0 pF)		f_U	—	3.0	—	MHz
Gain Margin (R_L = 600 Ω, C_L = 0 pF)	20, 22, 23	A_m	—	15	—	dB
Phase Margin (R_L = 600 Ω, C_L = 0 pF)	21, 22, 23	ϕ_m	—	60	—	Degrees
Channel Separation (f = 100 Hz to 20 kHz)	24	CS	—	−120	—	dB
Power Bandwidth (V_O = 20 V_{p-p}, R_L = 600 Ω, THD ≤ 1.0%)		BW_p	—	32	—	kHz
Distortion (R_L = 600 Ω,, V_O = 2.0 V_{p-p}, A_V = +1.0 V) (f = 1.0 kHz) (f = 10 kHz) (f = 20 kHz)	25	THD	 — — —	 0.0024 0.014 0.024	 — — —	%
Open-Loop Output Impedance (V_O = 0 V, f = 3.0 MHz, A_V = 10 V)	26	$\|Z_O\|$	—	150	—	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{IN}	—	200	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{IN}	—	10	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω,) f = 10 Hz f = 1.0 kHz	27	e_n	 — —	 8.0 7.5	 — —	nV/$\sqrt{Hz}$
Equivalent Input Noise Current f = 10 Hz f = 1.0 kHz	28	i_n	 — —	 0.33 0.15	 — —	pA/$\sqrt{Hz}$

Figure 1. Maximum Power Dissipation versus Temperature

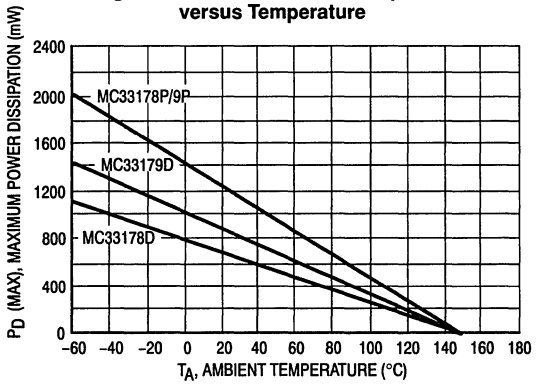
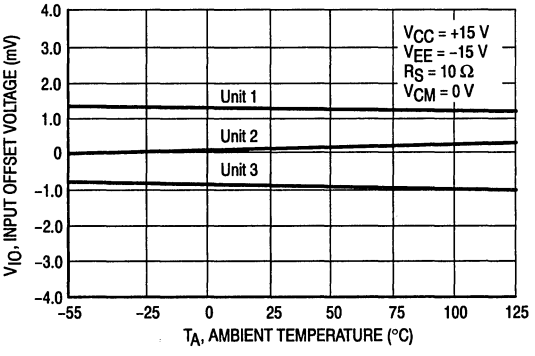


Figure 2. Input Offset Voltage versus Temperature for 3 Typical Units



2

Figure 3. Input Bias Current versus Common Mode Voltage

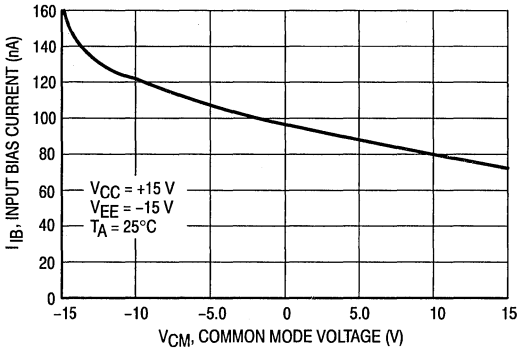


Figure 4. Input Bias Current versus Temperature

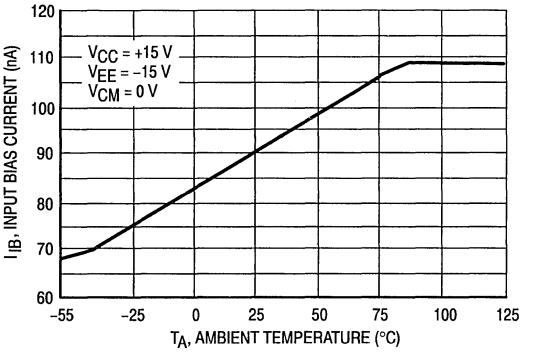


Figure 5. Input Common Mode Voltage Range versus Temperature

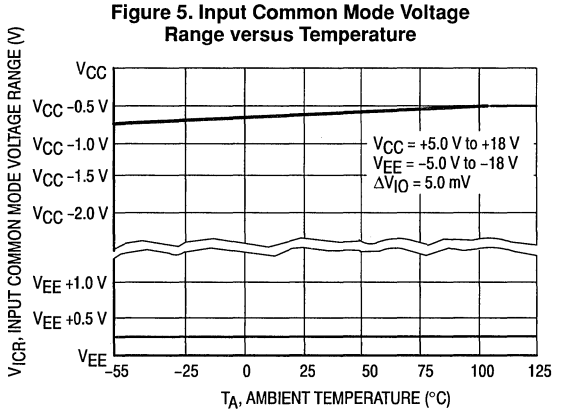


Figure 6. Open-Loop Voltage Gain versus Temperature

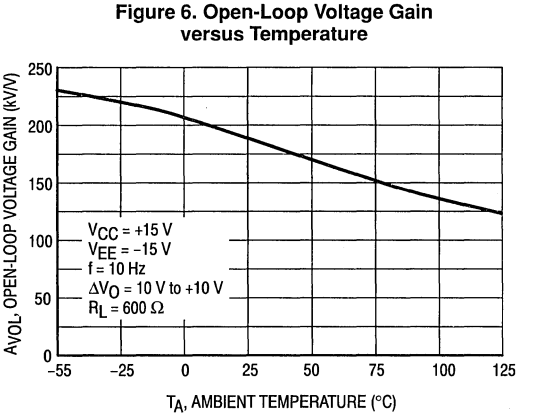


Figure 7. Voltage Gain and Phase versus Frequency

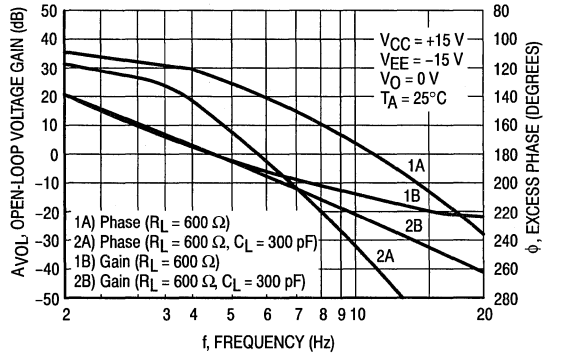


Figure 8. Output Voltage Swing versus Supply Voltage

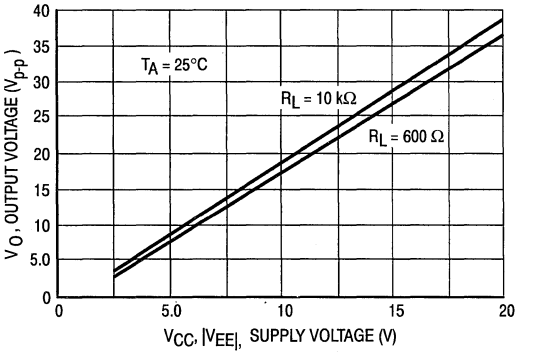


Figure 9. Output Saturation Voltage versus Load Current

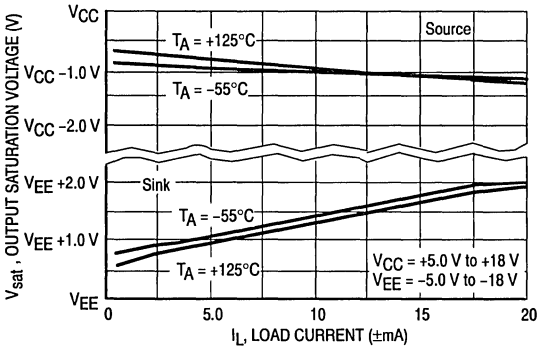


Figure 10. Output Voltage versus Frequency

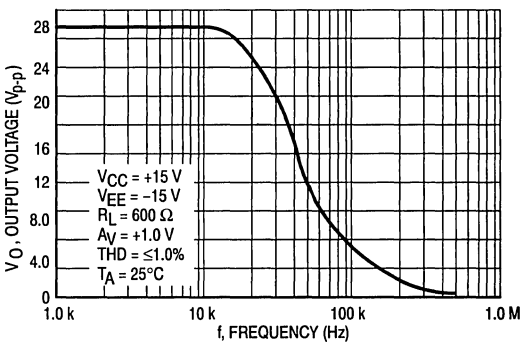


Figure 11. Common Mode Rejection versus Frequency Over Temperature

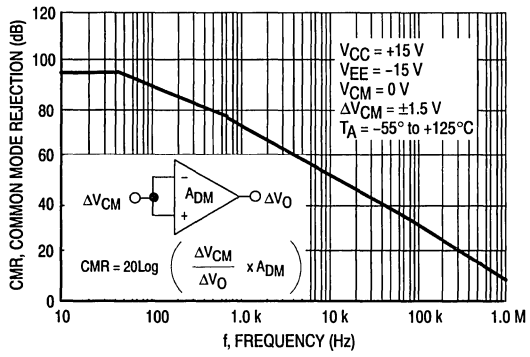


Figure 12. Power Supply Rejection versus Frequency Over Temperature

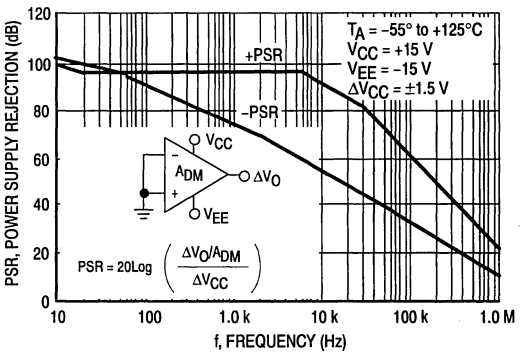


Figure 13. Output Short Circuit Current versus Output Voltage

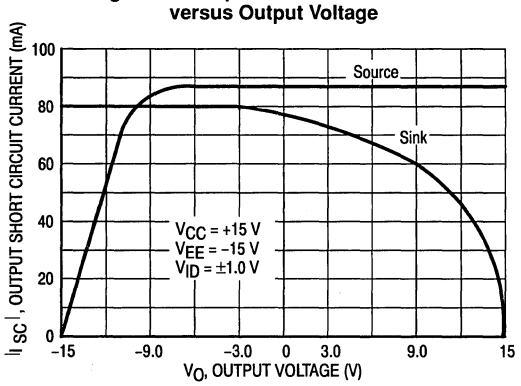


Figure 14. Output Short Circuit Current versus Temperature

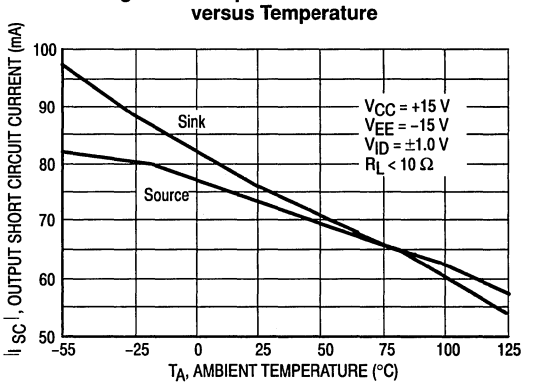


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Figure 15. Supply Current versus Supply Voltage with No Load

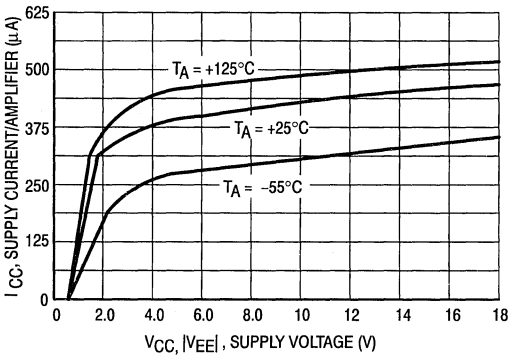

Figure 16. Normalized Slew Rate versus Temperature

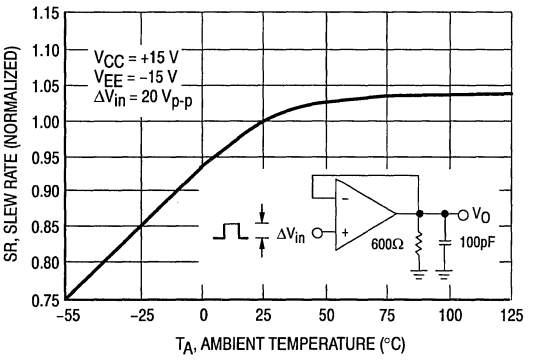

Figure 17. Gain Bandwidth Product versus Temperature

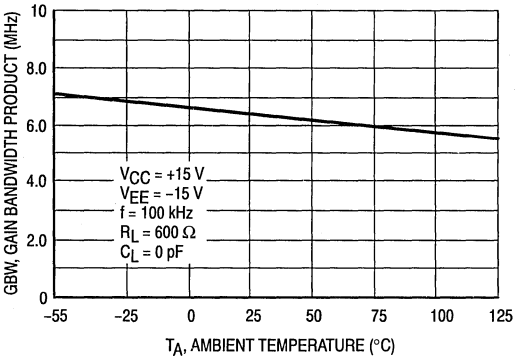

Figure 18. Voltage Gain and Phase versus Frequency

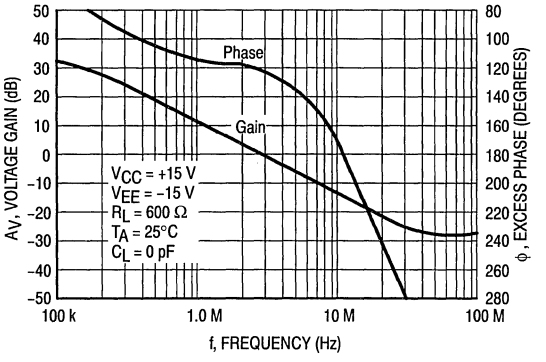

Figure 19. Voltage Gain and Phase versus Frequency

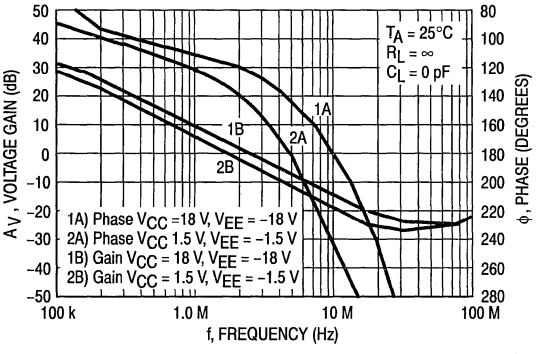

Figure 20. Open-Loop Gain Margin versus Temperature

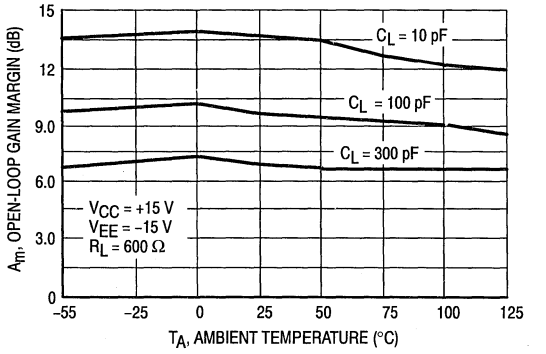

Figure 21. Phase Margin versus Temperature

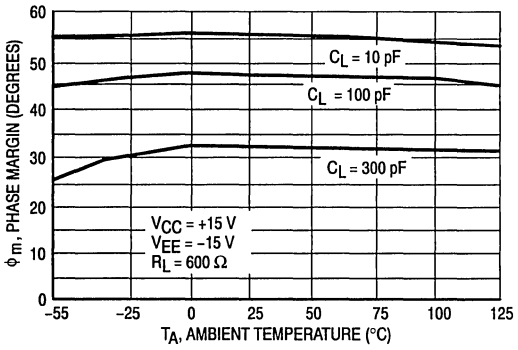

Figure 22. Phase Margin and Gain Margin versus Differential Source Resistance

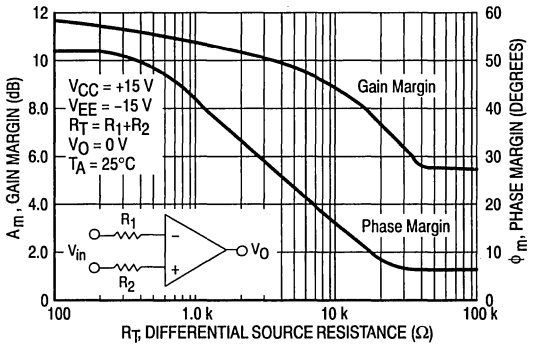

Figure 23. Open-Loop Gain Margin and Phase Margin versus Output Load Capacitance

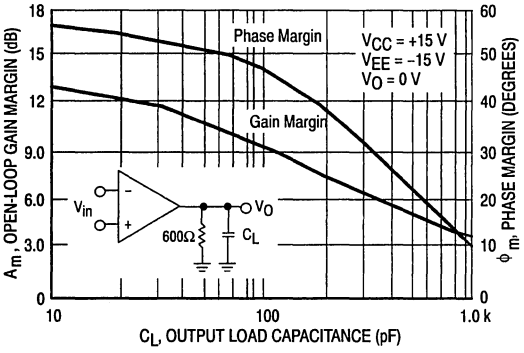

Figure 24. Channel Separation versus Frequency

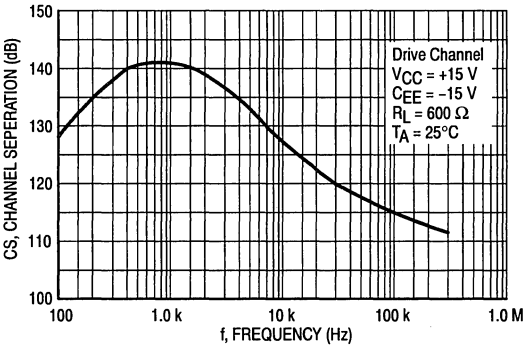

Figure 25. Total Harmonic Distortion versus Frequency

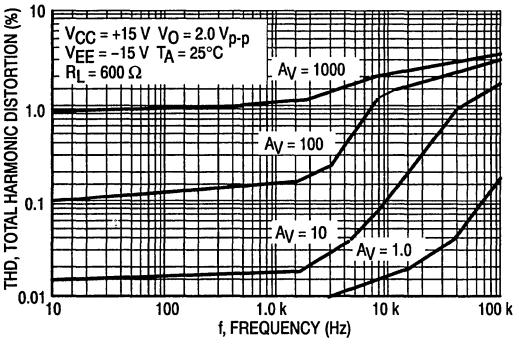

Figure 26. Output Impedance versus Frequency

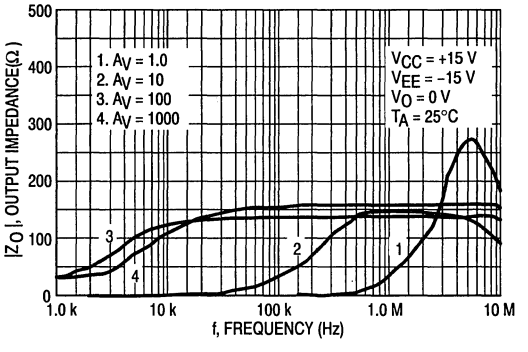

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Figure 27. Input Referred Noise Voltage versus Frequency

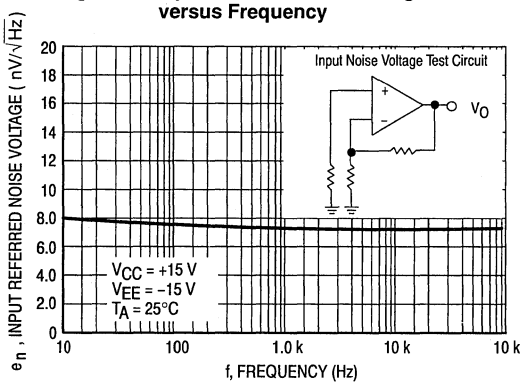


Figure 28. Input Referred Noise Current versus Frequency

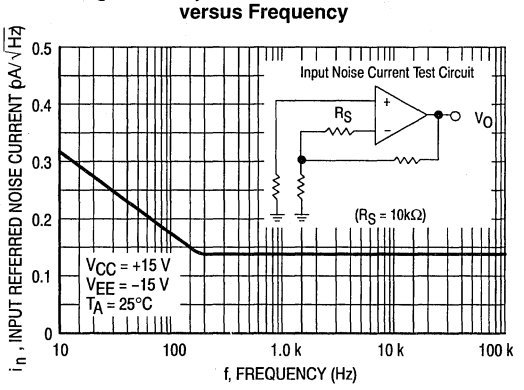


Figure 29. Percent Overshoot versus Load Capacitance

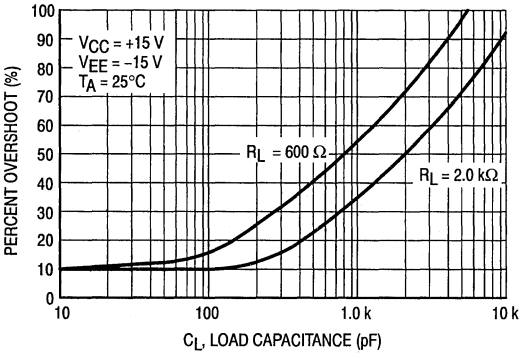


Figure 30. Noninverting Amplifier Slew Rate

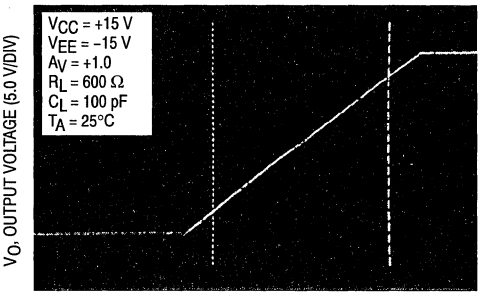


Figure 31. Small Signal Transient Response

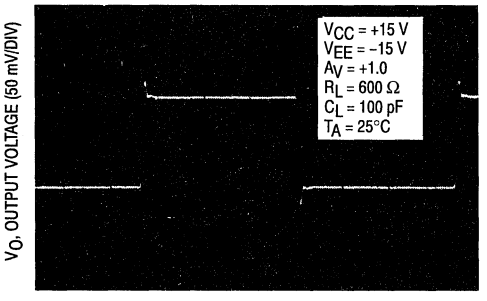


Figure 32. Large Signal Transient Response

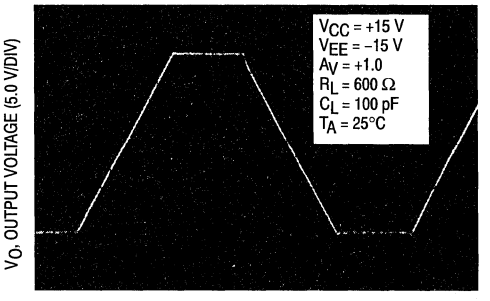
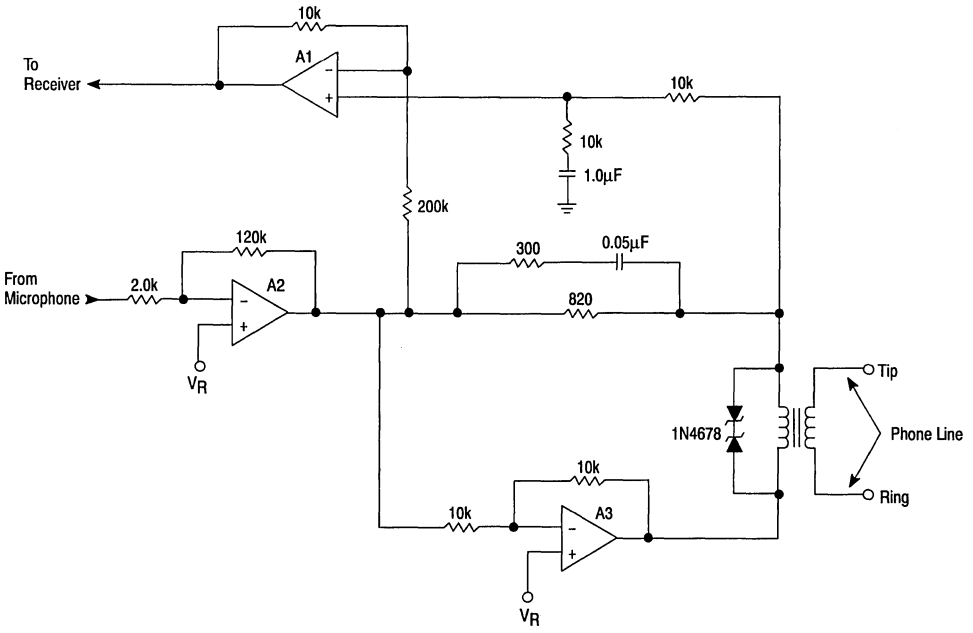


Figure 33. Telephone Line Interface Circuit



APPLICATION INFORMATION

This unique device uses a boosted output stage to combine a high output current with a drain current lower than similar bipolar input op amps. Its 60° phase margin and 15 dB gain margin ensure stability with up to 1000 pF of load capacitance (see Figure 23). The ability to drive a minimum 600 Ω load makes it particularly suitable for telecom applications. Note that in the sample circuit in Figure 33 both A2 and A3 are driving equivalent loads of approximately 600 Ω .

The low input offset voltage and moderately high slew rate and gain bandwidth product make it attractive for a variety of other applications. For example, although it is not single supply (the common mode input range does not include ground), it is specified at +5.0 V with a typical common mode rejection, of 110 dB. This makes it an excellent choice for use with digital circuits. The high common mode rejection, which is stable over temperature, coupled with a low noise figure and low distortion is an ideal op amp for audio circuits.

The output stage of the op amp is current limited and therefore has a certain amount of protection in the event of a short circuit. However, because of its high current output, it is especially important not to allow the device to exceed the maximum junction temperature, particularly with the MC33179 (quad op amp). Shorting more than one amplifier could easily exceed the junction temperature to the extent of causing permanent damage.

Stability

As usual with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input/output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole frequency for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supplying decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

Additional stability problems can be caused by high load capacitances and/or a high source resistance. Simple compensation schemes can be used to alleviate these effects.

If a high source of resistance is used (R1 > 1.0 kΩ), a compensation capacitor equal to or greater than the input capacitance of the op amp (10 pF) placed across the feedback resistor (see Figure 34) can be used to neutralize that pole and prevent outer loop oscillation. Since the closed loop transient response will be a function of that capacitance it is important to choose the optimum value for that capacitor. This can be determined by the following formula:

(1) $C_C = (1 + [R1/R2])^2 \bullet C_L (Z_O/R_2)$

where: Z_O is the output impedance of the op amp.

For moderately high capacitive loads (500 pF < C_L < 1500 pF) the addition of a compensation resistor on the order of 20 Ω between the output and the feedback loop will help to decrease miller loop oscillation (see Figure 35). For high capacitive loads (C_L > 1500 pF) a combined compensation scheme should be used (see Figure 36). Both the compensation resistor and the compensation capacitor affect the transient response and can be calculated for optimum performance. The value of C_C can be calculated using formula (1). The formula to calculate R_C is as follows:

(2) $R_C = Z_O \bullet R1/R2$

Figure 34. Compensation for High Source Impedance

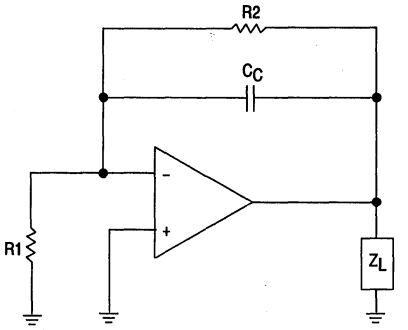


Figure 35. Compensation Circuit for Moderate Capacitve Loads

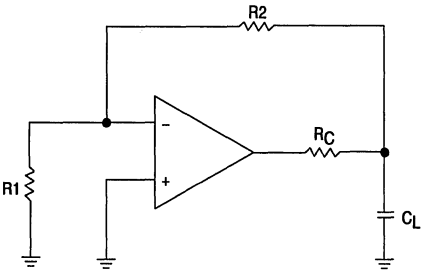
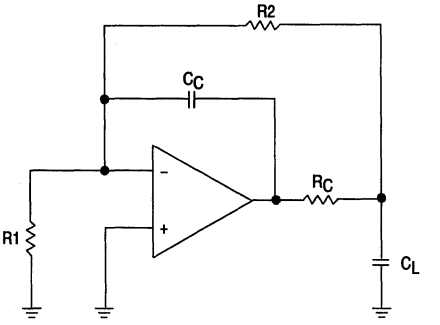


Figure 36. Compensation Circuit for High Capacitive Loads



MC33201
MC33202
MC33204

LOW VOLTAGE RAIL-TO-RAIL™ OPERATIONAL AMPLIFIERS

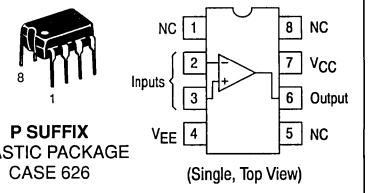
SILICON MONOLITHIC INTEGRATED CIRCUIT

Advance Information

Rail-to-Rail™ Operational Amplifiers

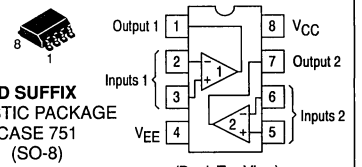
The MC33201/2/4 family of operational amplifiers provide rail-to-rail operation on both the input and output. The inputs can be driven as high as 200 mV beyond the supply rails without phase reversal on the outputs, and the output can swing within 50 mV of each rail. This rail-to-rail operation enables the user to make full use of the supply voltage range available. It is designed to work at very low supply voltages (± 0.9 V) yet can operate with a supply of up to +12 V and ground. Output current boosting techniques provide a high output current capability while keeping the drain current of the amplifier to a minimum. Also, the combination of low noise and distortion with a high slew rate and drive capability make this an ideal amplifier for audio applications.

- Low Voltage, Single Supply Operation (+1.8 V and Ground to +12 V and Ground)
- Input Voltage Range Includes both Supply Rails
- Output Voltage Swings within 50 mV of both Rails
- No Phase Reversal on the Output for Oven-driven Input Signals
- High Output Current (I_{SC} = 80 mA, Typ)
- Low Supply Current (I_D = 0.9 mA, Typ)
- 600 Ω Output Drive Capability
- Extended Operating Temperature Range (– 40° to +105°C)
- Typical Gain Bandwidth Product = 2.2 MHz



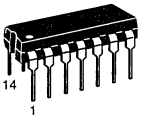
P SUFFIX
PLASTIC PACKAGE
CASE 626

(Single, Top View)



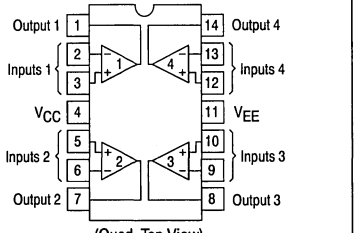
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

(Dual, Top View)



P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



(Quad, Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC33201P	– 40° to +105°C	Plastic DIP
MC33201D		SO-8
MC33202P		Plastic DIP
MC33202D		SO-8
MC33204P		Plastic DIP
MC33204D		SO-14

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	V_{CC} = 2.0 V	V_{CC} = 3.3 V	V_{CC} = 5.0 V	Unit
Input Offset Voltage V_{IO} (max) MC33201 MC33202 MC33204	 ± 8.0 ±10 ±12	 ± 8.0 ±10 ±12	 ± 6.0 ± 8.0 ±10	mV
Output Voltage Swing V_{OH} (R_L = 10 kΩ) V_{OL} (R_L = 10 kΩ)	 1.9 0.10	 3.15 0.15	 4.85 0.15	 V_{min} V_{max}
Power Supply Current per Amplifier (I_D)	1.125	1.125	1.125	mA

Specifications at V_{CC} = 3.3 V are guaranteed by the 2.0 V and 5.0 V tests. V_{EE} = Gnd.

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+13	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Common Mode Input Voltage Range (Note 2)	V_{CM}	V_{CC} + 0.5 V to V_{EE} – 0.5 V	V
Output Short Circuit Duration	t_s	(Note 3)	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	– 65 to +150	°C
Maximum Power Dissipation	P_D	(Note 3)	mW

NOTES: 1. The differential input voltage of each amplifier is limited by two internal parallel back-to-back diodes. For additional differential input voltage range, use current limiting resistors in series with the input pins.
2. The input common mode voltage range is limited by internal diodes connected from the inputs to both supply rails. Therefore, the voltage on either input must not exceed either supply rail by more than 500 mV.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See Figure 2)

DC ELECTRICAL CHARACTERISTICS (V_{CC} = + 5.0 V, V_{EE} = Ground, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} 0 V to 0.5 V, V_{CM} 1.0 V to 5.0 V)	3	$\|V_{IO}\|$				mV
(MC33201): T_A = + 25°C			—	—	6.0	
T_A = – 40° to +105°C			—	—	9.0	
(MC33202): T_A = + 25°C			—	—	8.0	
T_A = – 40° to +105°C			—	—	11	
(MC33204): T_A = + 25°C			—	—	10	
T_A = – 40° to +105°C			—	—	13	
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω)	4	$\Delta V_{IO}/\Delta T$				µV/°C
T_A = – 40° to +105°C			—	2.0	—	
Input Bias Current (V_{CM} = 0 V to 0.5 V, V_{CM} = 1.0 V to 5.0 V)	5, 6	$\|I_{IB}\|$				nA
T_A = + 25°C			—	80	200	
T_A = – 40° to +105°C			—	100	250	
Input Offset Current (V_{CM} = 0 V to 0.5 V, V_{CM} = 1.0 V to 5.0 V)	—	$\|I_{IO}\|$				nA
T_A = + 25°C			—	5.0	50	
T_A = – 40° to +105°C			—	10	100	
Common Mode Input Voltage Range	—	V_{ICR}	V_{EE}	—	V_{CC}	V
Large Signal Voltage Gain (V_{CC} = + 5.0 V, V_{EE} = – 5.0 V)	7	A_{VOL}				kV/V
R_L = 10 kΩ			50	300	—	
R_L = 600 Ω			25	250	—	
Output Voltage Swing (V_{ID} = ± 0.2 V)	8, 9, 10					V
R_L = 10 kΩ		V_{OH}	4.85	4.95	—	
R_L = 10 kΩ		V_{OL}	—	0.05	0.15	
R_L = 600 Ω		V_{OH}	4.75	4.85	—	
R_L = 600 Ω		V_{OL}	—	0.15	0.25	
Common Mode Rejection (V_{in} = 0 V to 5.0 V)	11	CMR	60	90	—	dB
Power Supply Rejection Ratio	12	PSRR				µV/V
V_{CC}/V_{EE} = 5.0 V/Gnd to 3.0 V/Gnd			500	25	—	
Output Short Circuit Current (Source and Sink)	13, 14	I_{SC}	50	80	—	mA
Power Supply Current per Amplifier (V_O = 0 V)	15	I_D				mA
T_A = – 40° to +105°C			—	0.9	1.125	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = + 5.0 V, V_{EE} = Ground, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_S = ± 2.5 V, V_O = – 2.0 V to + 2.0 V, R_L = 2.0 kΩ, A_V = +1.0)	16, 26	SR	0.5	1.0	—	V/μs
Gain Bandwidth Product (f = 100 kHz)	17	GBW	—	2.2	—	MHz
Gain Margin (R_L = 600 Ω, C_L = 0 pF)	20, 21, 22	A_M	—	12	—	dB
Phase Margin (R_L = 600 Ω, C_L = 0 pF)	20, 21, 22	ϕ_M	—	65	—	Deg
Channel Separation (f = 1.0 Hz to 20 kHz, A_V = 100)	23	CS	—	90	—	dB
Power Bandwidth (V_O = 4.0 V_{pp}, R_L = 600 Ω, THD ≤ 1 %)		BW_P	—	28	—	kHz
Total Harmonic Distortion (R_L = 600 Ω, V_O = 1.0 V_{pp}, A_V = 1.0) f = 1.0 kHz f = 10 kHz	24	THD	 — —	 0.002 0.008	 — —	%
Open-Loop Output Impedance (V_O = 0 V, f = 2.0 MHz, A_V = 10)		$\|Z_O\|$	—	100	—	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{in}	—	200	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{in}	—	8.0	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω) f = 10 Hz f = 1.0 kHz	25	e_n	 — —	 25 20	 — —	$\frac{nV}{\sqrt{Hz}}$
Equivalent Input Noise Current f = 10 Hz f = 1.0 kHz	25	i_n	 — —	 0.8 0.2	 — —	$\frac{pA}{\sqrt{Hz}}$

Figure 1. Equivalent Circuit Schematic (Each Amplifier)

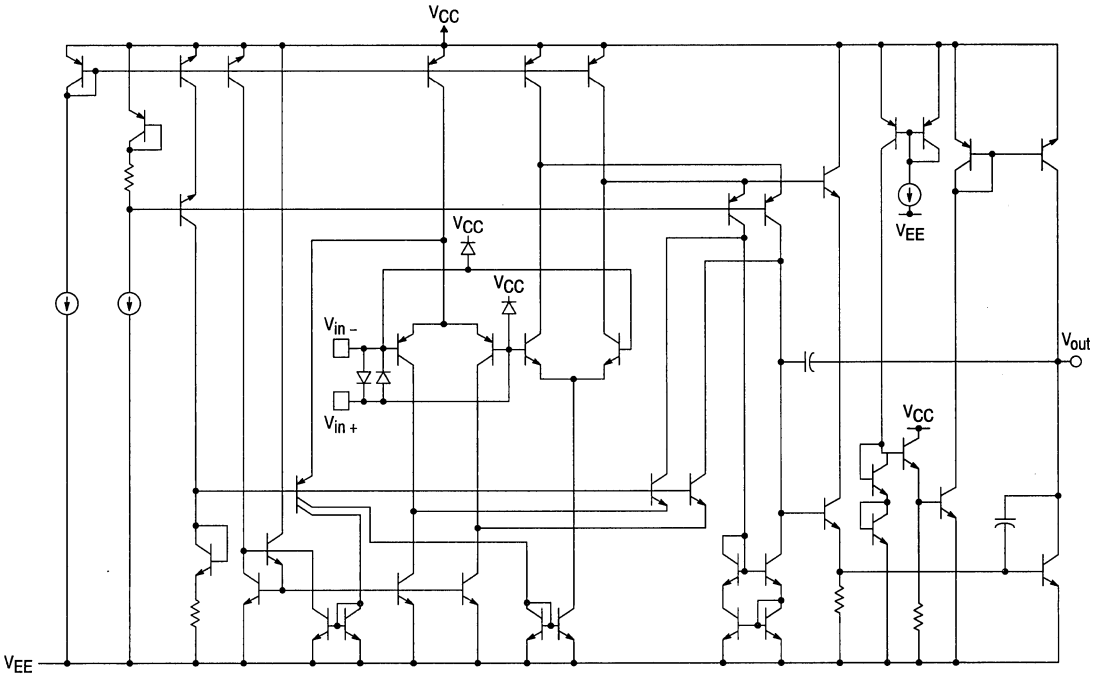


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Figure 2. Maximum Power Dissipation versus Temperature

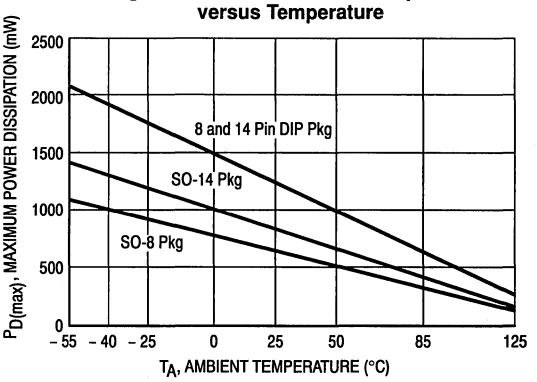


Figure 3. Input Offset Voltage Distribution

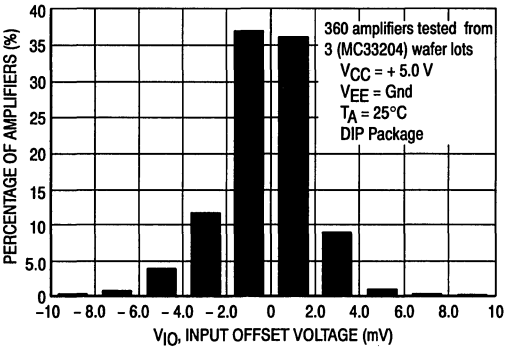


Figure 4. Input Offset Voltage Temperature Coefficient Distribution

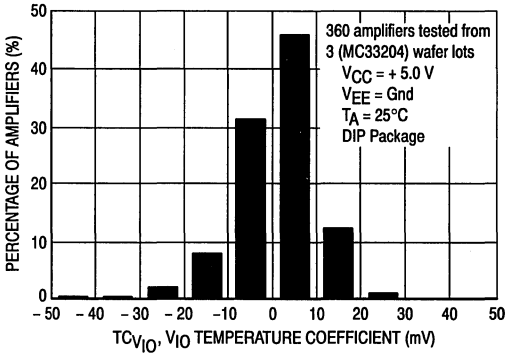


Figure 5. Input Bias Current versus Temperature

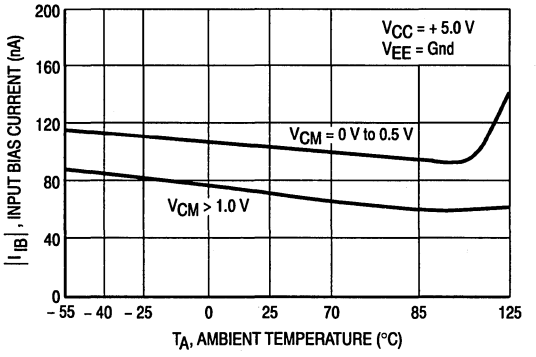


Figure 6. Input Bias Current versus Common Mode Voltage

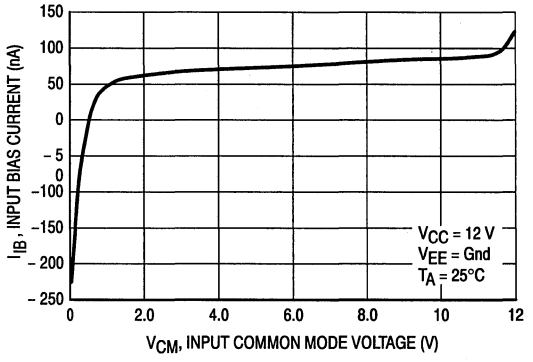


Figure 7. Open-Loop Voltage Gain versus Temperature

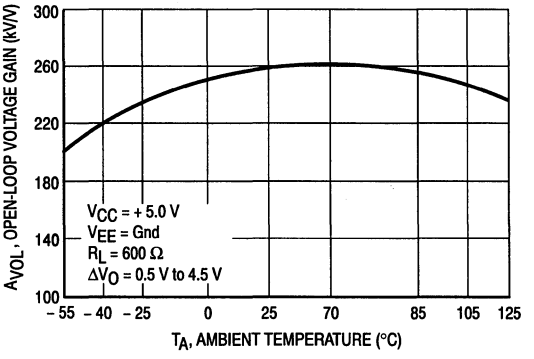


Figure 8. Output Voltage Swing versus Supply Voltage

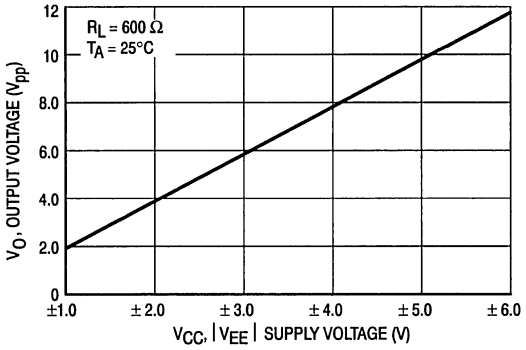


Figure 9. Output Saturation Voltage versus Load Current

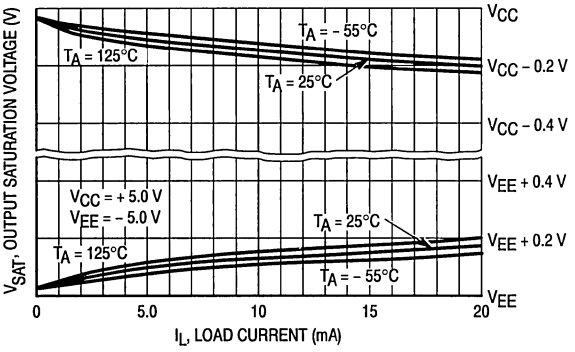


Figure 10. Output Voltage versus Frequency

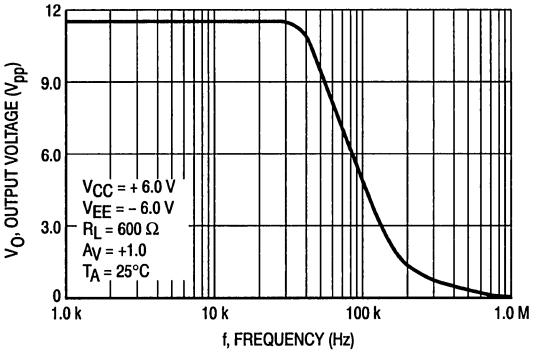


Figure 11. Common Mode Rejection versus Frequency

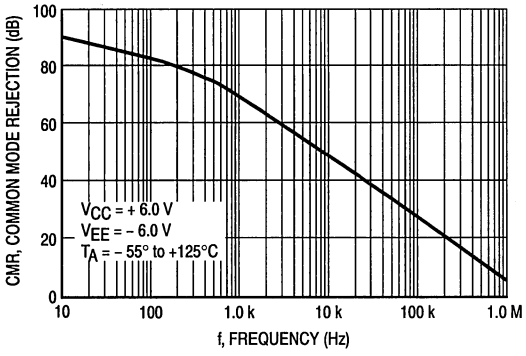


Figure 12. Power Supply Rejection versus Frequency

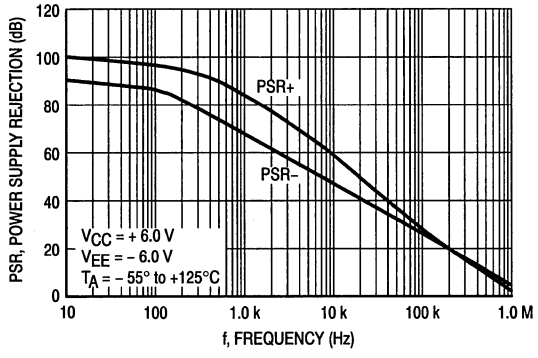
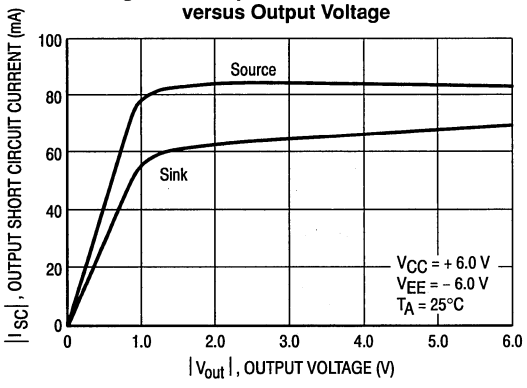


Figure 13. Output Short Circuit Current versus Output Voltage



2

Figure 14. Output Short Circuit Current versus Temperature

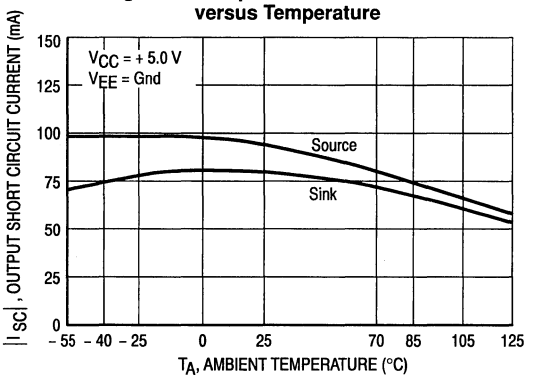


Figure 15. Supply Current per Amplifier versus Supply Voltage with No Load

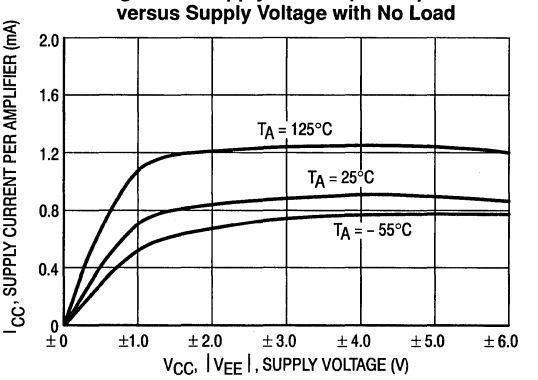


Figure 16. Slew Rate versus Temperature

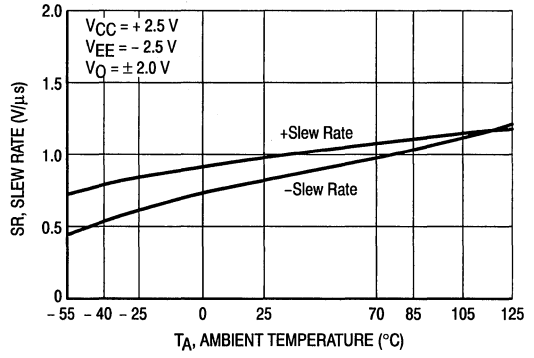


Figure 17. Gain Bandwidth Product versus Temperature

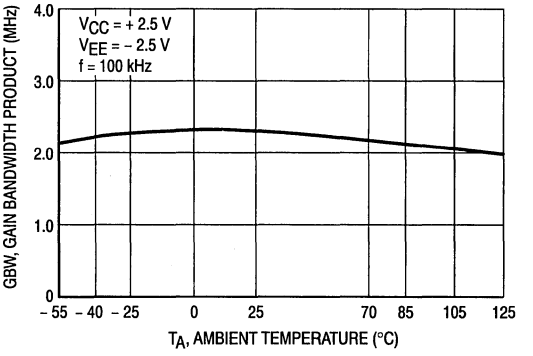


Figure 18. Voltage Gain and Phase versus Frequency

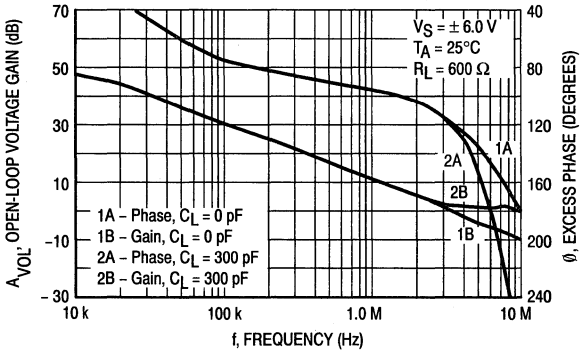


Figure 19. Voltage Gain and Phase versus Frequency

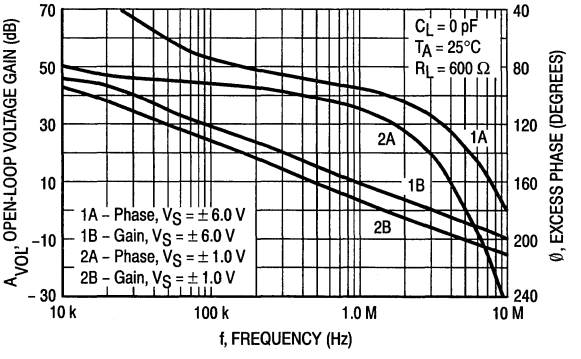


Figure 20. Gain and Phase Margin versus Temperature

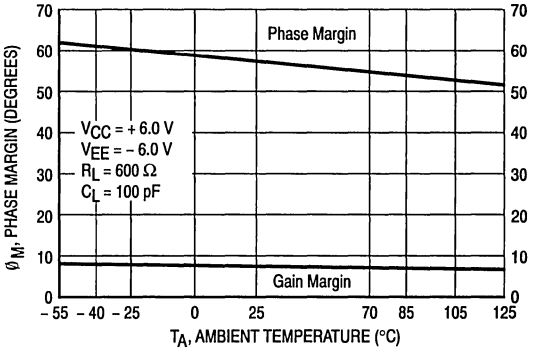


Figure 21. Gain and Phase Margin versus Differential Source Resistance

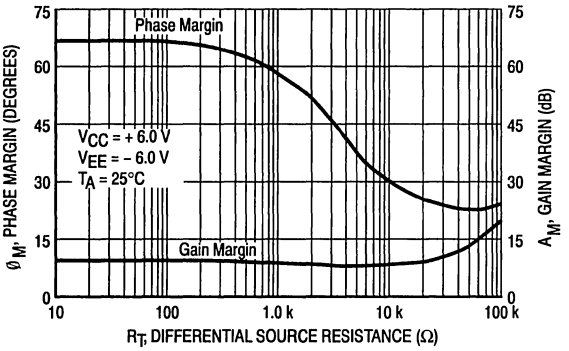


Figure 22. Gain and Phase Margin versus Capacitive Load

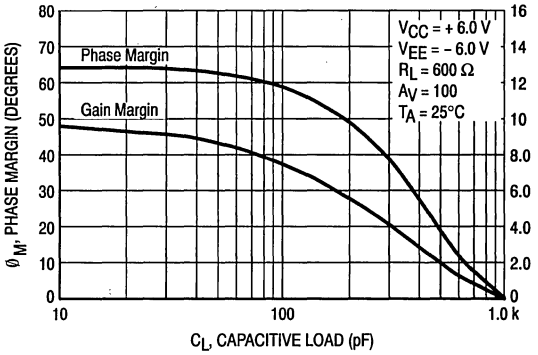


Figure 23. Channel Separation versus Frequency

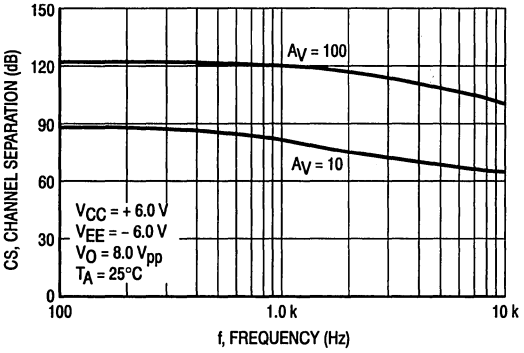


Figure 24. Total Harmonic Distortion versus Frequency

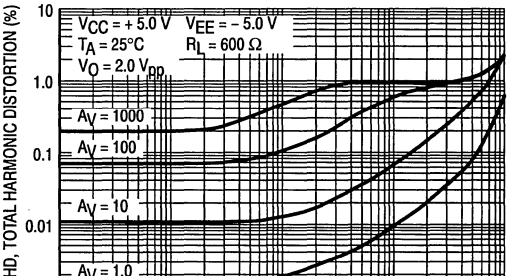
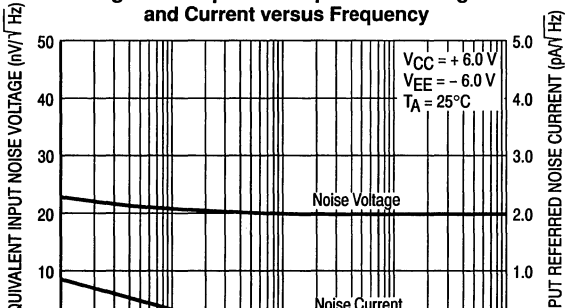


Figure 25. Equivalent Input Noise Voltage and Current versus Frequency



2

General Information

The MC33201/2/4 family of operational amplifiers are unique in their ability to swing rail-to-rail on both the input and the output with a completely bipolar design. This offers low noise, high output current capability and a wide common mode input voltage range even with low supply voltages. Operation is guaranteed over an extended temperature range and at supply voltages of 2.0 V, 3.3 V and 5.0 V and ground.

Since the common mode input voltage range extends from V_{CC} to V_{EE}, it can be operated with either single or split voltage supplies. The MC33201/2/4 are guaranteed not to latch or phase reverse over the entire common mode range, however, the inputs should not be allowed to exceed maximum ratings.

Circuit Information

Rail-to-rail performance is achieved at the input of the amplifiers by using parallel NPN-PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV greater than V_{EE}, the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents (see Figure 6). Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross-coupling techniques have been used to keep this change to a minimum.

In addition to its rail-to-rail performance, the output stage is current boosted to provide 80 mA of output current, enabling the op amp to drive 600 Ω loads. Because of this high output current capability, care should be taken not to exceed the 150°C maximum junction temperature.

Figure 26. Noninverting Amplifier Slew Rate

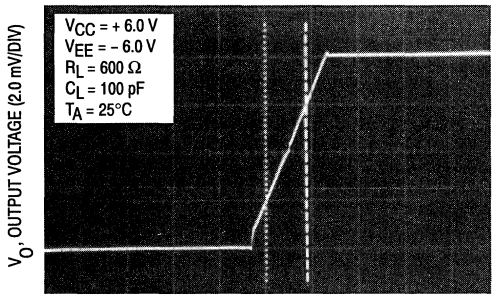


Figure 27. Small Signal Transient Response

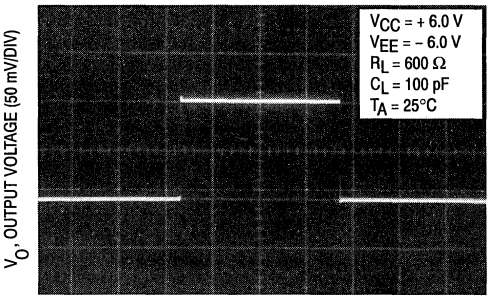
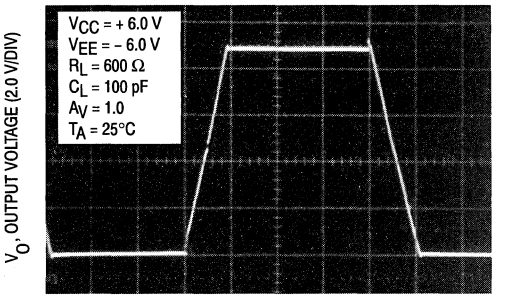


Figure 28. Large Signal Transient Response



MC33272
MC33274

HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

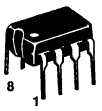
Single Supply, High Slew Rate Low Input Offset Voltage, Bipolar Operational Amplifiers

The MC33272/74 series of monolithic operational amplifiers are quality fabricated with innovative Bipolar design concepts. This dual and quad operational amplifier series incorporates Bipolar inputs along with a patented Zip-R-Trim element for input offset voltage reduction. The MC33272/74 series of operational amplifiers exhibits low input offset voltage and high gain bandwidth product. Dual-doublet frequency compensation is used to increase the slew rate while maintaining low input noise characteristics. Its all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, and an excellent phase and gain margin. It also provides a low open-loop high frequency output impedance with symmetrical source and sink AC frequency performance.

The MC33272/74 series is specified over –40° to +85°C and is available in the plastic DIP and SOIC surface mount packages (P and D suffixes).

- Input Offset Voltage Trimmed to 100 μV (Typ)
- Low Input Bias Current: 300 nA
- Low Input Offset Current: 3.0 nA
- High Input Resistance: 16 MΩ
- Low Noise: 18 nV/$\sqrt{\text{Hz}}$ @ 1.0 kHz
- High Gain Bandwidth Product: 24 MHz @ 100 kHz
- High Slew Rate: 10 V/μs
- Power Bandwidth: 160 kHz
- Excellent Frequency Stability
- Unity Gain Stable: w/Capacitance Loads to 500 pF
- Large Output Voltage Swing: +14.1 V/ –14.6 V
- Low Total Harmonic Distortion: 0.003%
- Power Supply Drain Current: 2.15 mA per Amplifier
- Single or Split Supply Operation: +3.0 V to +36 V or ±1.5 V to ±18 V
- ESD Diodes Provide Added Protection to the Inputs

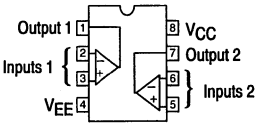
DUAL



P SUFFIX
PLASTIC PACKAGE
CASE 626

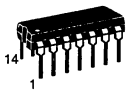
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS

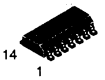


(Top View)

QUAD

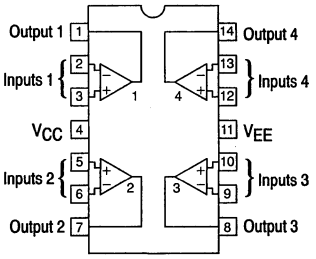


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Op Amp Function	Device	Specified Ambient Temperature Range	Package
Dual	MC33272D	–40° to +85°C	SO-8
	MC33272P		Plastic DIP
Quad	MC33274D		SO-14
	MC33274P		Plastic DIP

2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} to V_{EE}	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V)	3	$\|V_{IO}\|$				mV
(V_{CC} = +15 V, V_{EE} = –15 V)						
T_A = +25°C			—	0.1	1.0	
T_A = –40° to +85°C			—	—	1.8	
(V_{CC} = 5.0 V, V_{EE} = 0)						
T_A = +25°C			—	—	2.0	
Average Temperature Coefficient of Input Offset Voltage	3	$\Delta V_{IO}/\Delta T$				µV/°C
R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = –40° to +85°C			—	2.0	—	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	4, 5	I_{IB}				nA
T_A = +25°C			—	300	650	
T_A = –40° to +85°C			—	—	800	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)		$\|I_{IO}\|$				nA
T_A = +25°C			—	3.0	65	
T_A = –40° to +85°C			—	—	80	
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	6	V_{ICR}	V_{EE} to (V_{CC} –1.8)			V
T_A = +25°C						
Large Signal Voltage Gain (V_O = 0 V to 10 V, R_L = 2.0 kΩ)	7	A_{VOL}				dB
T_A = +25°C			90	100	—	
T_A = –40° to +85°C			86	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)	8, 9, 12					V
(V_{CC} = +15 V, V_{EE} = –15 V)						
R_L = 2.0 kΩ		V_{O+}	13.4	13.9	—	
R_L = 2.0 kΩ		V_{O-}	—	–13.9	–13.5	
R_L = 10 kΩ		V_{O+}	13.4	14	—	
R_L = 10 kΩ		V_{O-}	—	–14.7	–14.1	
(V_{CC} = 5.0 V, V_{EE} = 0 V)	10, 11					
R_L = 2.0 kΩ		V_{OL}	—	—	0.2	
R_L = 2.0 kΩ		V_{OH}	3.7	—	5.0	
Common Mode Rejection (V_{in} = +13.2 V to –15 V)	13	CMR	80	100	—	dB
Power Supply Rejection	14, 15	PSR				dB
V_{CC}/V_{EE} = +15 V/ –15 V, +5.0 V/ –15 V, +15 V/ –5.0 V			80	105	—	
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground)	16	I_{SC}				mA
Source			+25	+37	—	
Sink			–25	–37	—	
Power Supply Current Per Amplifier (V_O = 0 V)	17	I_{CC}				mA
(V_{CC} = +15 V, V_{EE} = –15 V)						
T_A = +25°C			—	2.15	2.75	
T_A = –40° to +85°C			—	—	3.0	
(V_{CC} = 5.0 V, V_{EE} = 0 V)						
T_A = +25°C			—	—	2.75	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0 V)	18, 33	SR	8.0	10	—	V/μs
Gain Bandwidth Product (f = 100 kHz)	19	GBW	17	24	—	MHz
AC Voltage Gain (R_L = 2.0 kΩ, V_O = 0 V, f = 20 kHz)	20, 21, 22	A_{VO}	—	65	—	dB
Unity Gain Frequency (Open-Loop)		f_U	—	5.5	—	MHz
Gain Margin (R_L = 2.0 kΩ, C_L = 0 pF)	23, 24, 26	A_m	—	12	—	dB
Phase Margin (R_L = 2.0 kΩ, C_L = 0 pF)	23, 25, 26	ϕ_m	—	55	—	Degrees
Channel Separation (f = 20 Hz to 20 kHz)	27	CS	—	−120	—	dB
Power Bandwidth (V_O = 20 V_{p-p}, R_L = 2.0 kΩ, THD ≤ 1.0%)		BW_P	—	160	—	kHz
Total Harmonic Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	28	THD	—	0.003	—	%
Open-Loop Output Impedance (V_O = 0 V, f = 6.0 MHz)	29	$\|Z_O\|$	—	35	—	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{IN}	—	16	—	MΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{IN}	—	3.0	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	30	e_n	—	18	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	31	i_n	—	0.5	—	$pA/\sqrt{Hz}$

Figure 1. Equivalent Circuit Schematic (Each Amplifier)

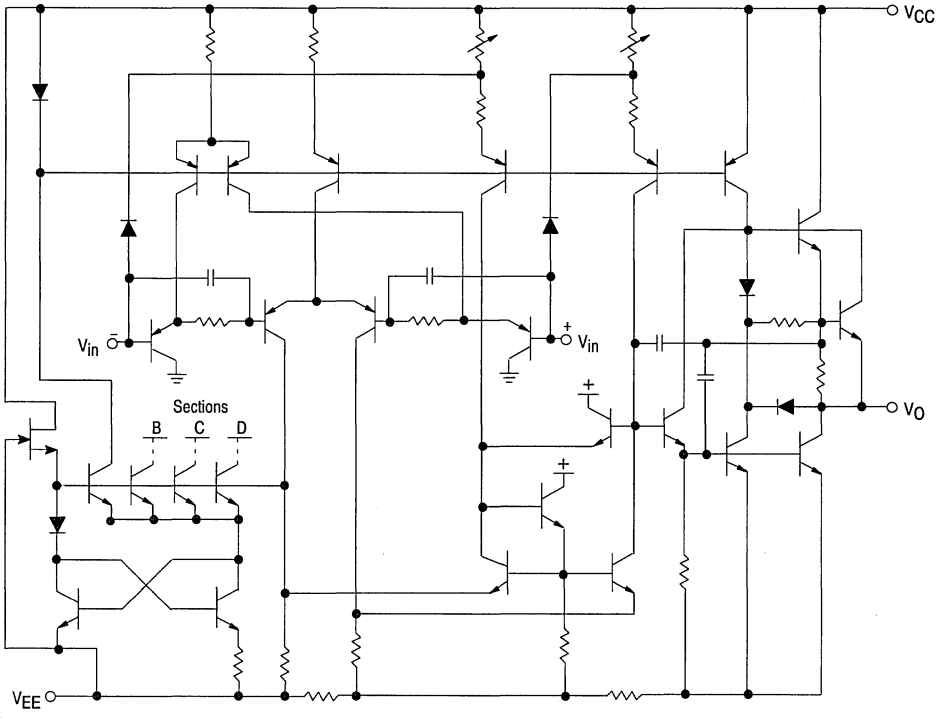


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Figure 2. Maximum Power Dissipation versus Temperature

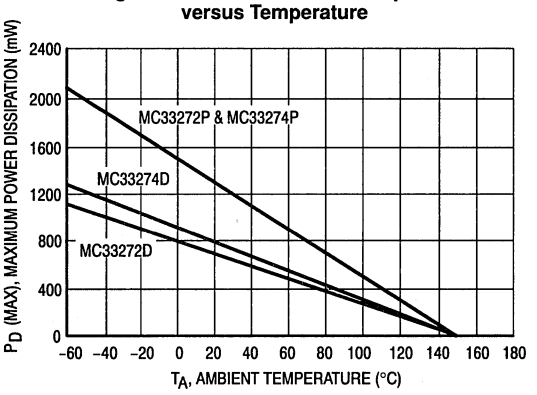

Figure 3. Input Offset Voltage versus Temperature for Typical Units

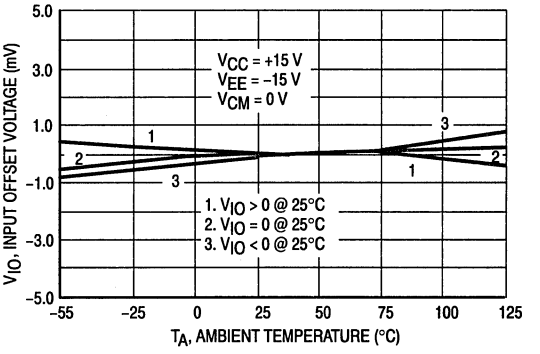

Figure 4. Input Bias Current versus Common Mode Voltage

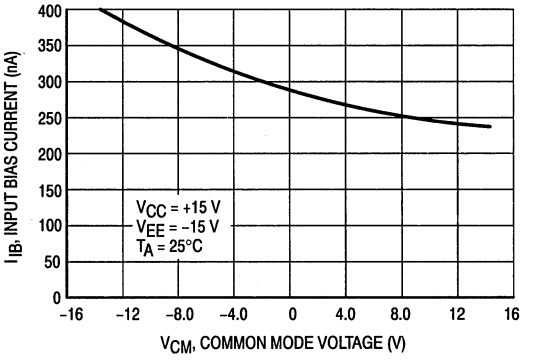

Figure 5. Input Bias Current versus Temperature

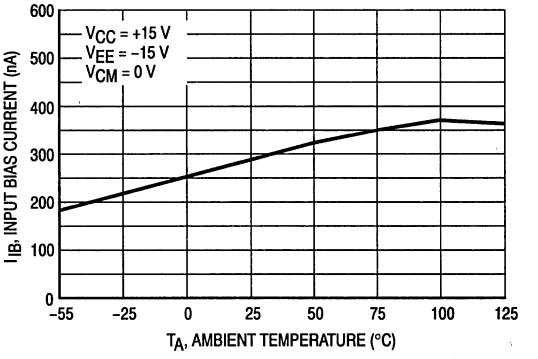

Figure 6. Input Common Mode Voltage Range versus Temperature

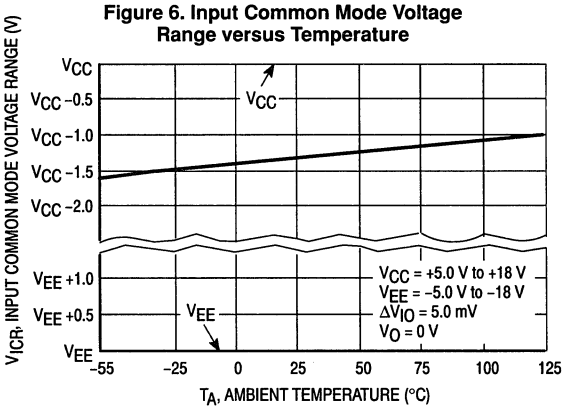

Figure 7. Open-Loop Voltage Gain versus Temperature

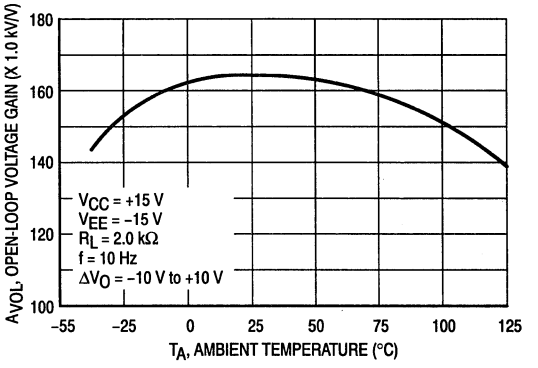

Figure 8. Split Supply Output Voltage Swing versus Supply Voltage

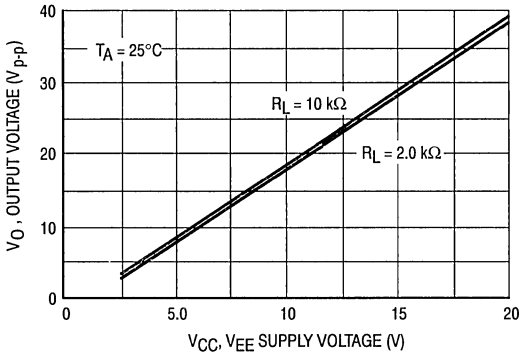

Figure 9. Split Supply Output Saturation Voltage versus Load Current

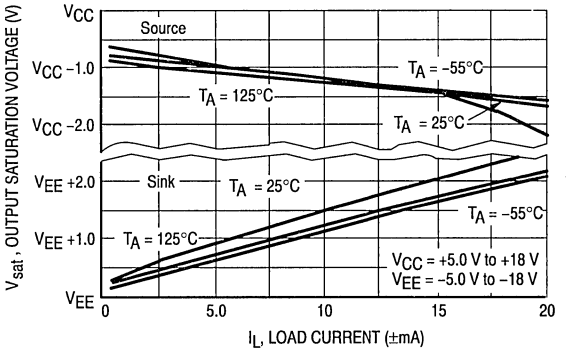

Figure 10. Single Supply Output Saturation Voltage versus Load Resistnce to Ground

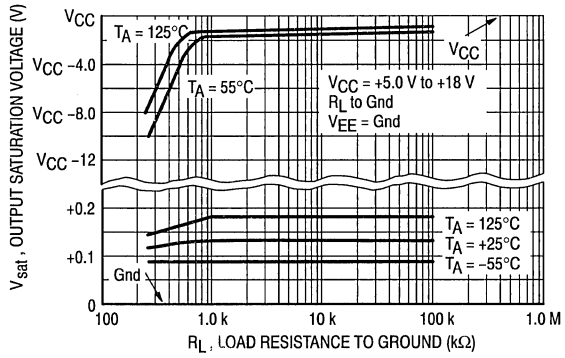

Figure 11. Single Supply Output Saturation Voltage versus Load Resistance to V_{CC}

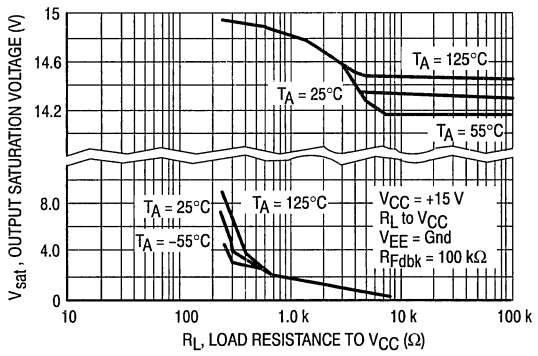

Figure 12. Output Voltage versus Frequency

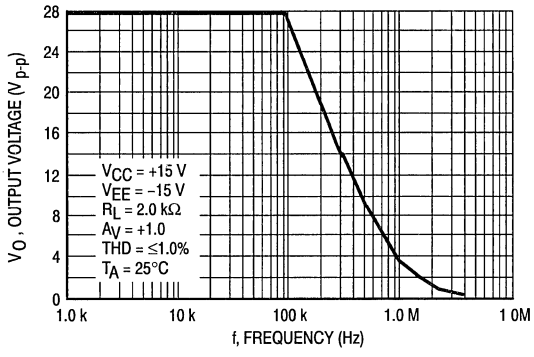

Figure 13. Common Mode Rejection versus Frequency

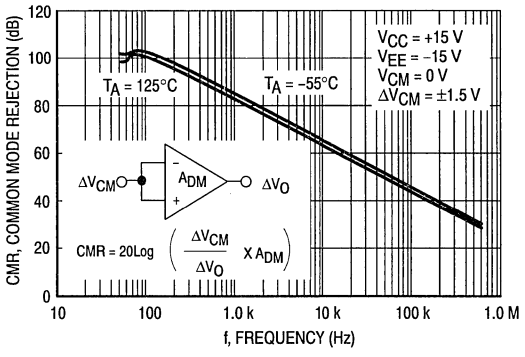

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Figure 14. Positive Power Supply Rejection versus Frequency

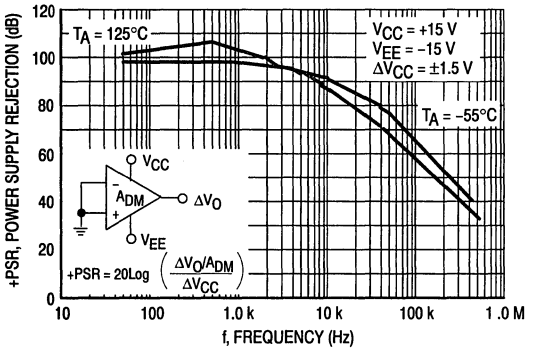

Figure 15. Negative Power Supply Rejection versus Frequency

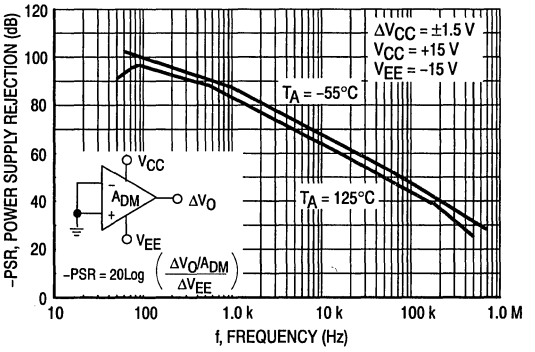

Figure 16. Output Short Circuit Current versus Temperature

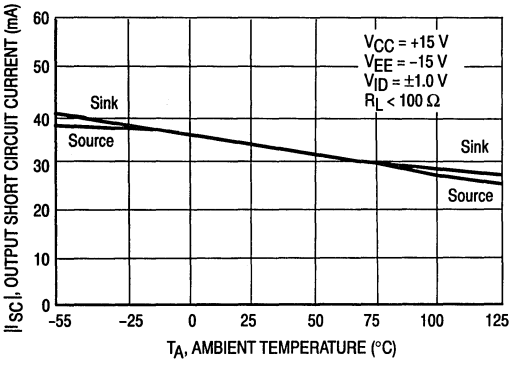

Figure 17. Supply Current versus Supply Voltage

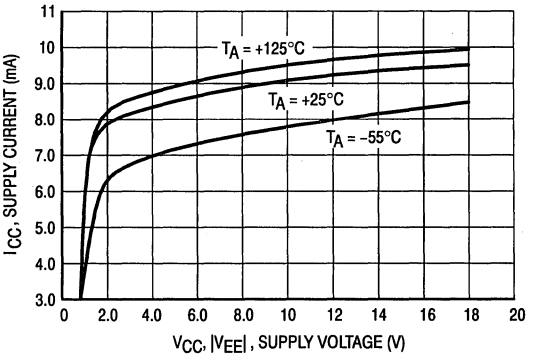

Figure 18. Normalized Slew Rate versus Temperature

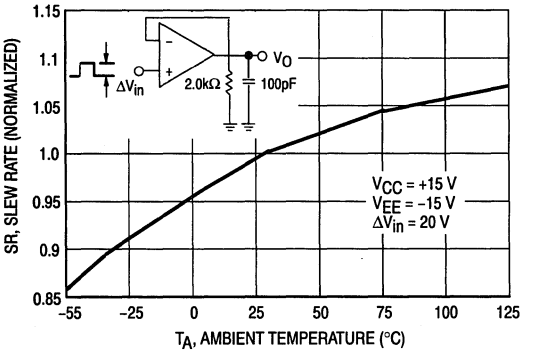

Figure 19. Gain Bandwidth Product versus Temperature

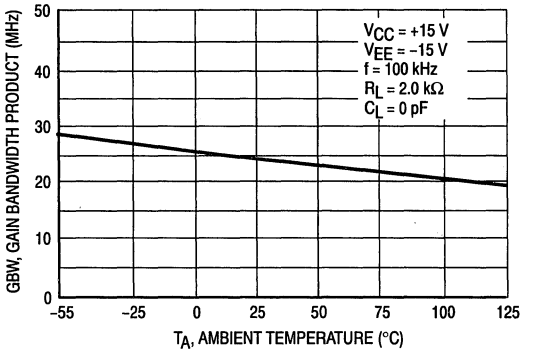

Figure 20. Voltage Gain and Phase versus Frequency

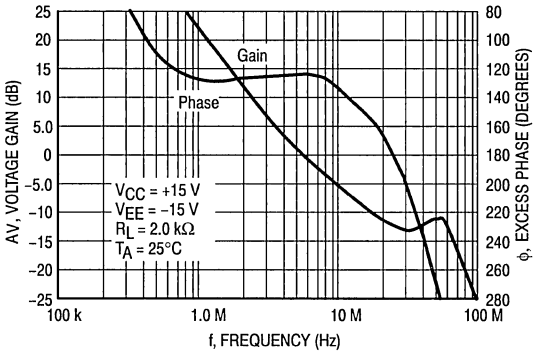

Figure 21. Gain and Phase versus Frequency

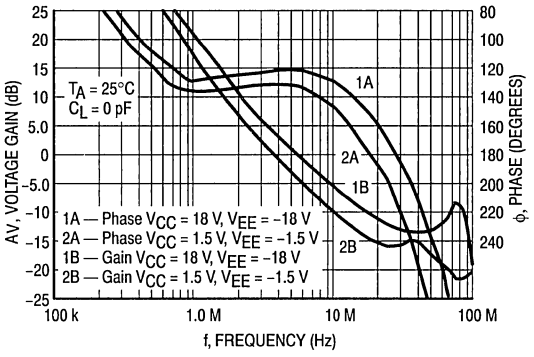

Figure 22. Open-Loop Voltage Gain and Phase versus Frequency

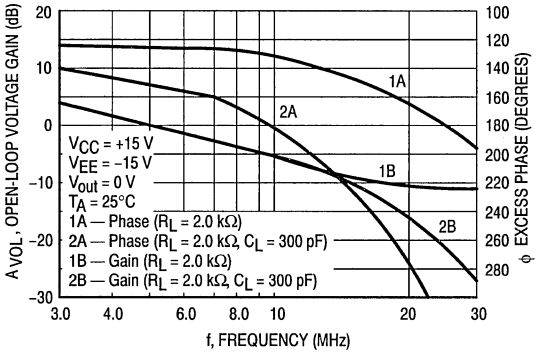

Figure 23. Open-Loop Gain Margin and Phase Margin versus Output Load Capacitance

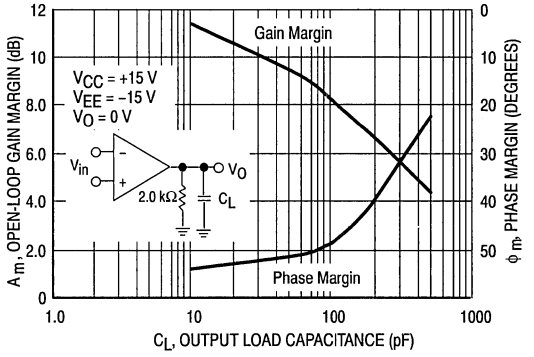

Figure 24. Open-Loop Gain Margin versus Temperature

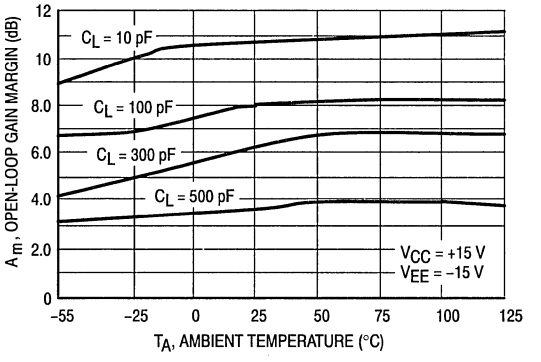

Figure 25. Phase Margin versus Temperature

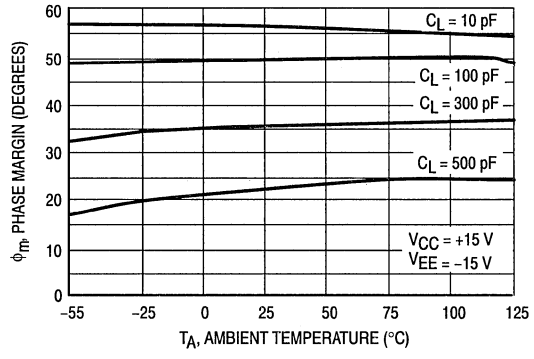

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Figure 26. Phase Margin and Gain Margin versus Differential Source Resistance

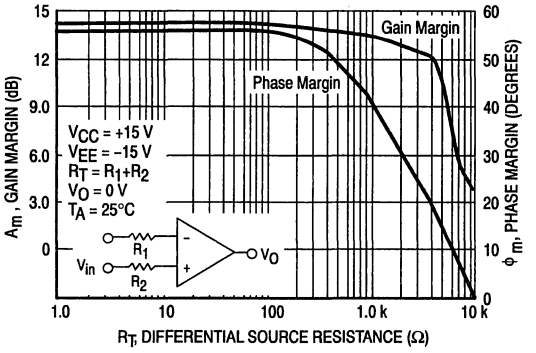


Figure 27. Channel Separation versus Frequency

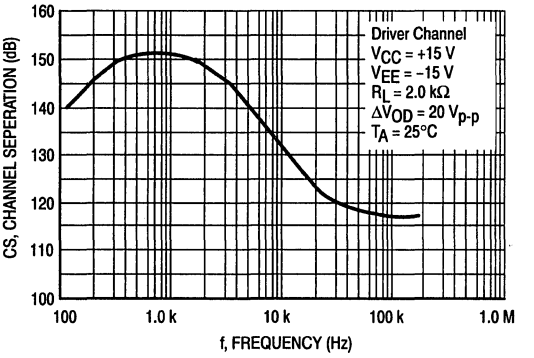


Figure 28. Total Harmonic Distortion versus Frequency

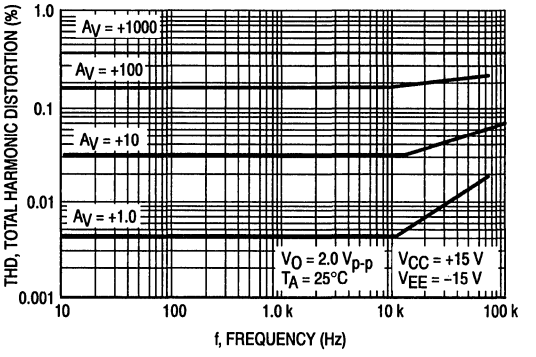


Figure 29. Output Impedance versus Frequency

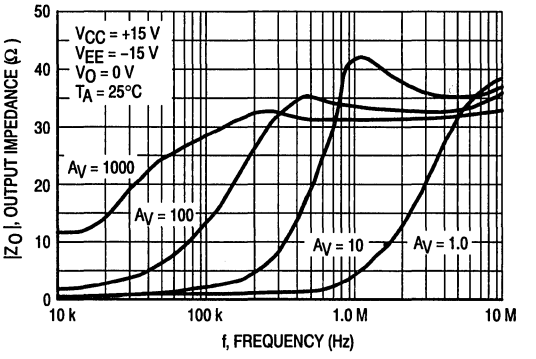


Figure 30. Input Referred Noise Voltage versus Frequency

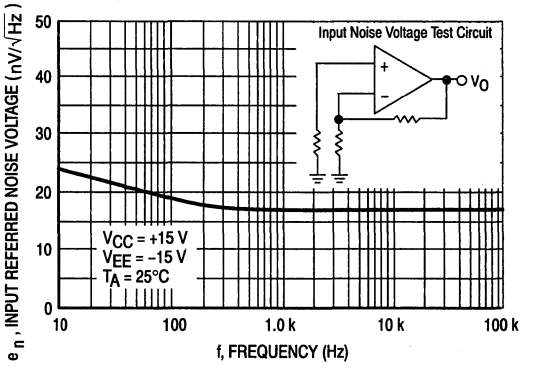


Figure 31. Input Referred Noise Current versus Frequency

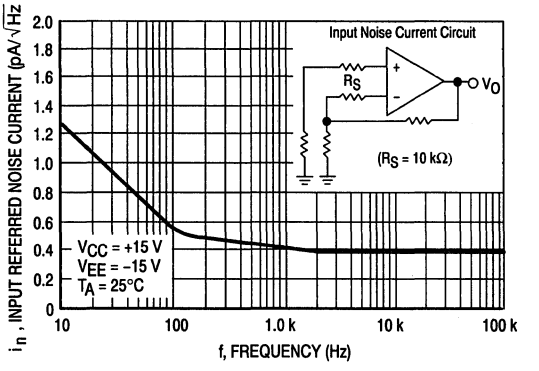


Figure 32. Percent Overshoot versus Load Capacitance

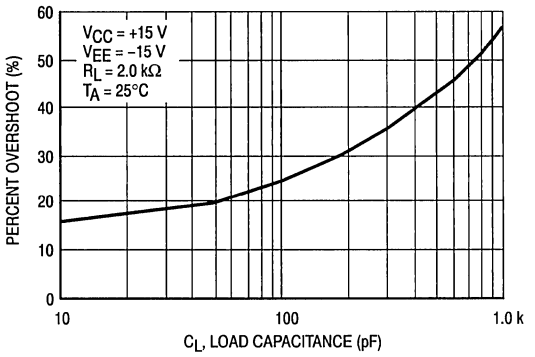


Figure 33. Noninverting Amplifier Slew Rate for the MC33274

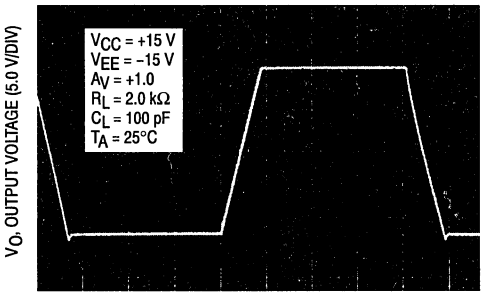


Figure 34. Noninverting Amplifier Overshoot for the MC33274

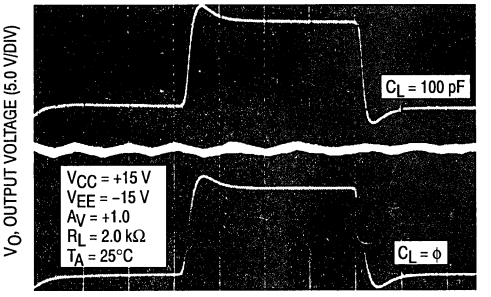


Figure 35. Small Signal Transient Response for MC33274

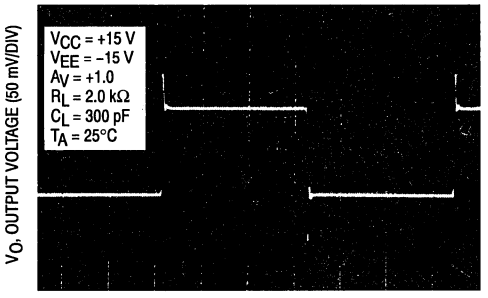
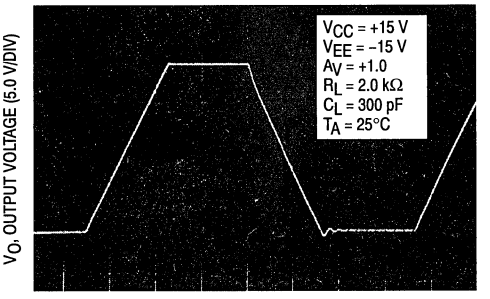


Figure 36. Large Signal Transient Response for MC33274



MC33282
MC33284

HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

Advance Information

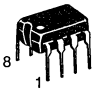
Low Input Offset, High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifiers

The MC33282/284 series of high performance operational amplifiers are quality fabricated with innovative bipolar and JFET design concepts. This dual and quad amplifier series incorporates JFET inputs along with a patented Zip-R-Trim element for input offset voltage reduction. These devices exhibit low input offset voltage, low input bias current, high gain bandwidth and high slew rate. Dual-doublet frequency compensation is incorporated to produce high quality phase/gain performance. In addition, the MC33282/284 series exhibit low input noise characteristics for JFET input amplifiers. Its all NPN output stage exhibits no deadband crossover distortion and a large output voltage swing. They also provide a low open-loop high frequency output impedance with symmetrical source and sink AC frequency performance.

The MC33282/284 series are specified over –40° to +85°C and are available in plastic DIP and SOIC surface mount packages (P and D suffixes).

- Low Input Offset Voltage: Trimmed to 200 μV
- Low Input Bias Current: 30 pA
- Low Input Offset Current: 6.0 pA
- High Input Resistance: 10^{12} Ω
- Low Noise: 18 nV $\sqrt{\text{Hz}}$ @ 1.0 kHz
- High Gain Bandwidth Products: 35 MHz @ 100 kHz
- High Slew Rate: 15 V/μs
- Power Bandwidth: 175 kHz
- Unity Gain Stable: w/Capacitance Loads to 300 pF
- Large Output Voltage Swing: +14.1 V/–14.6 V
- Low Total Harmonic Distortion: 0.003%
- Power Supply Drain Current: 2.15 mA per Amplifier
- Dual Supply Operation: ±2.5 V to ±18 V (Max)

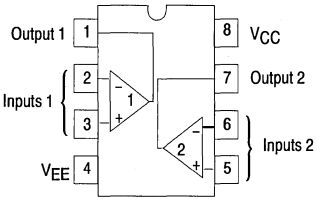
DUAL (MC33282)



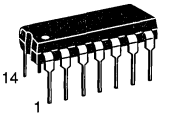
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP-8)

PIN CONNECTIONS



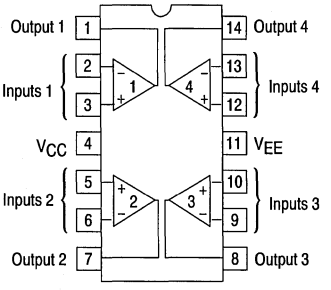
QUAD (MC33284)



P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



ORDERING INFORMATION

Op Amp Function	Device	Specified Ambient Temperature Range	Package
Dual	MC33282D	–40° to +85°C	SOP-8
	MC33282P		Plastic DIP
Quad	MC33284D		SO-14
	MC33284P		Plastic DIP

Zip-R-Trim is a registered trademark of Motorola Inc.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	– 60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See power dissipation performance characteristic, Figure 2.)

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Figure	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = –40° to +85°C	$\|V_{IO}\|$	3	 — —	 0.2 —	 2.0 4.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = T_{low} to T_{high}	$\|\Delta V_{IO}\|/\Delta T$	3	 —	 15	 —	μV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = –40° to +85°C	I_{IB}	4, 5	 –200 –2.0	 30 —	 200 2.0	 pA nA
Input Offset Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = –40° to +85°C	I_{IO}		 –100 –1.0	 6.0 —	 100 1.0	 pA nA
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	V_{ICR}	6	–11 —	–12 +14	— +11	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ) T_A = +25°C T_A = –40° to +85°C	A_{VOL}	7	 50 25	 200 —	 — —	V/mV
Output Voltage Swing (V_{ID} = ±1.0 V) R_L = 2.0 kΩ R_L = 2.0 kΩ R_L = 10 kΩ R_L = 10 kΩ	 V_{O+} V_{O-} V_{O+} V_{O-}	8, 9, 10	 13.2 — 13.7 —	 +13.7 –13.9 +14.1 –14.6	 — –13.2 — –14.3	V
Common Mode Rejection (V_{in} = ±11 V)	CMR	11	70	90	—	dB
Power Supply Rejection V_{CC}/V_{EE} = +15 V/–15 V, +5.0 V/–15 V, +15 V/–5.0 V	PSR	12	 75	 100	 —	dB
Output Short Circuit Current (V_{ID} = 1.0 V, output to ground) Source Sink	I_{SC}	13, 14	 15 —	 +21 –27	 — –15	mA
Power Supply Current (V_O = 0 V, per amplifier) T_A = +25°C T_A = –40° to +85°C	I_D	15	 — —	 2.15 —	 2.75 3.0	mA

2

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Figure	Min	Typ	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0)	SR	16, 28, 29	8.0	15	V/μs
Gain Bandwidth Product (f = 100 kHz)	GBW	17	20	35	MHz
AC Voltage Gain (R_L = 2.0 kΩ, V_O = 0 V, f = 20 kHz)	A_{VO}	18, 21	—	1750	V/V
Unity Gain Frequency (Open-Loop)	f_U		—	5.5	MHz
Gain Margin (R_L = 2.0 kΩ, C_L = 0 pF)	A_m	19, 20	—	15	dB
Phase Margin (R_L = 2.0 kΩ, C_L = 0 pF)	ϕ_m	19, 20	—	40	Degrees
Channel Separation (f = 20 Hz to 20 kHz)	CS	22	—	−120	dB
Power Bandwidth (V_O = 20 V_{p-p}, R_L = 2.0 kΩ, THD ≤ 1.0%)	BW_P		—	175	kHz
Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	THD	23	—	0.003	%
Open-Loop Output Impedance (V_O = 0 V, f = 9.0 MHz)	$\|Z_O\|$	24	—	37	Ω
Differential Input Resistance (V_{CM} = 0 V)	R_{IN}		—	10^{12}	Ω
Differential Input Capacitance (V_{CM} = 0 V)	C_{IN}		—	5.0	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	e_n	25	—	18	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	i_n		—	0.01	$pA/\sqrt{Hz}$

Figure 1. Equivalent Circuit Schematic
(Each Amplifier)

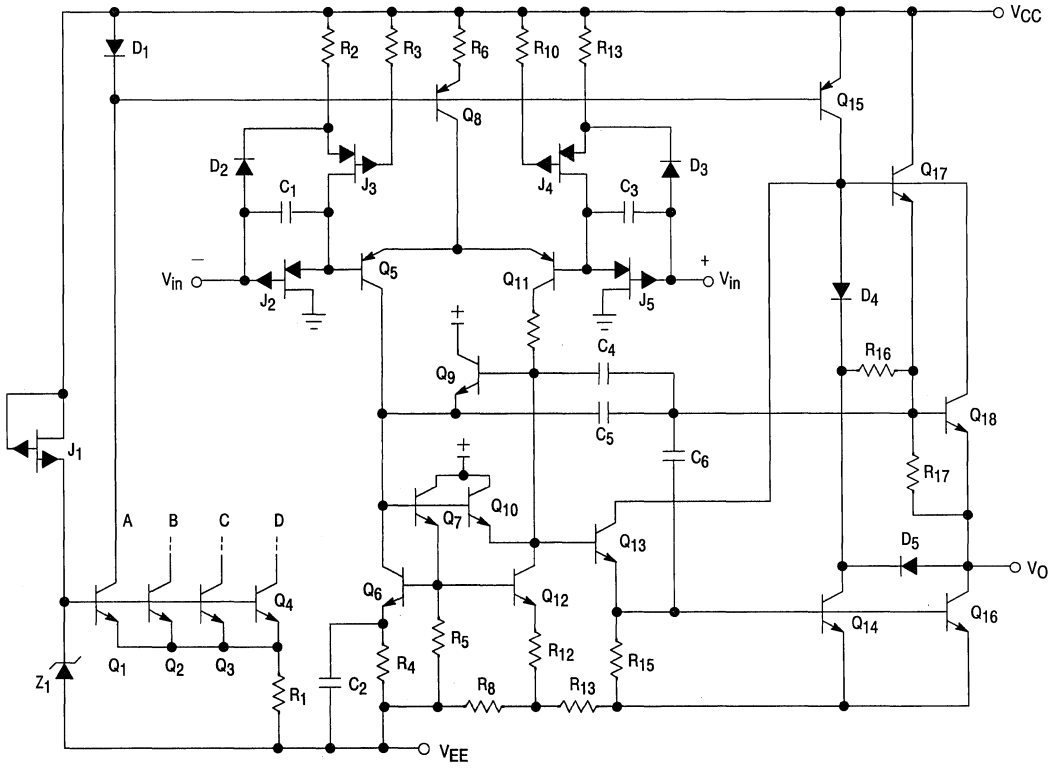


Figure 2. Maximum Power Dissipation versus Temperature

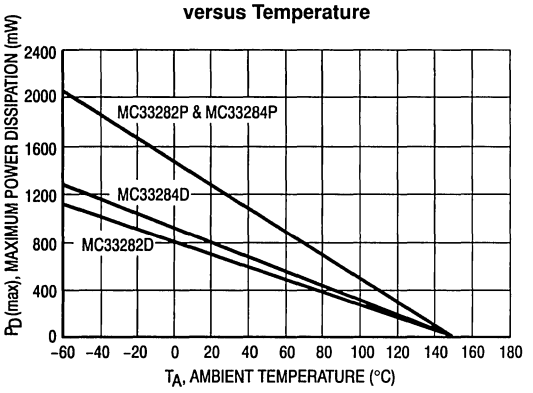


Figure 3. Input Offset Voltage versus Temperature for Typical Units

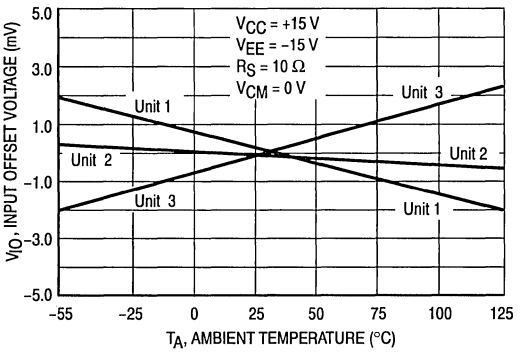


Figure 4. Input Bias Current versus Temperature

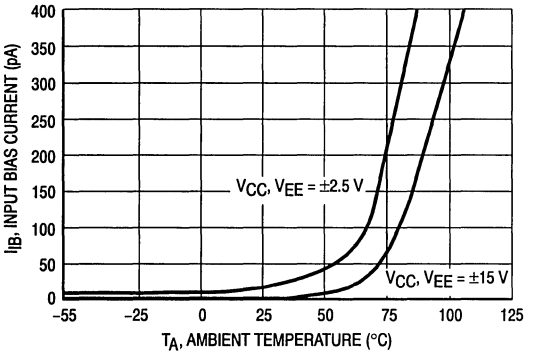


Figure 5. Input Bias Current versus Common Mode Voltage

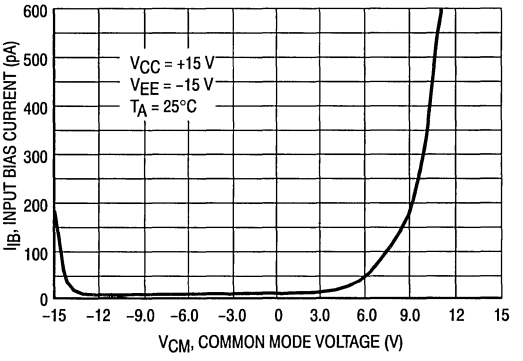


Figure 6. Input Common Mode Voltage Range versus Temperature

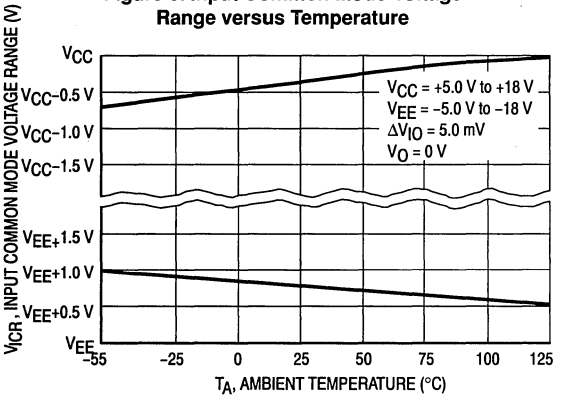
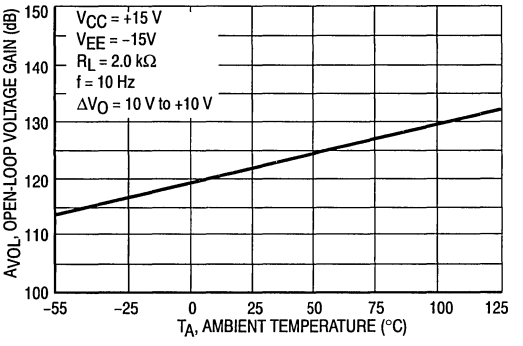


Figure 7. Open-Loop Voltage Gain versus Temperature



2

Figure 8. Output Voltage Swing versus Supply Voltage

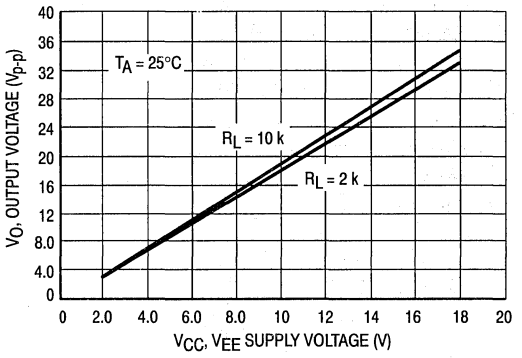


Figure 9. Output Voltage versus Frequency

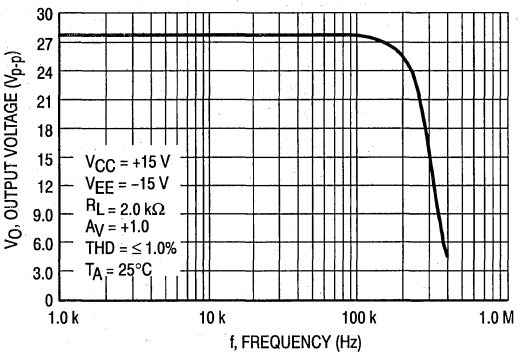


Figure 10. Output Saturation Voltage versus Load Current

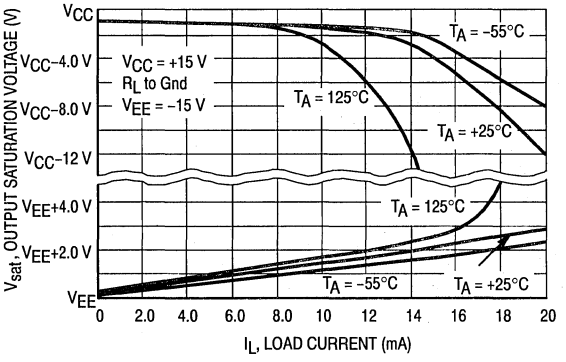


Figure 11. Common Mode Rejection versus Frequency

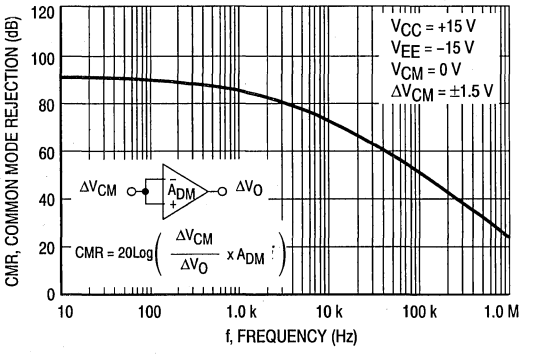


Figure 12. Positive Power Supply Rejection versus Frequency

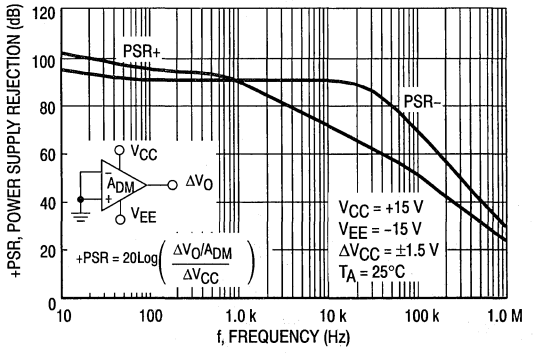


Figure 13. Output Short Circuit Source Current versus Temperature

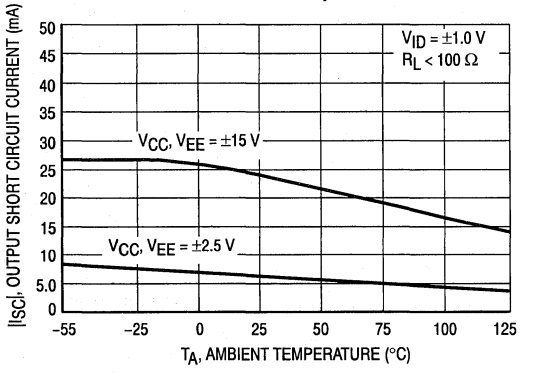


Figure 14. Output Short Circuit Sink Current versus Temperature

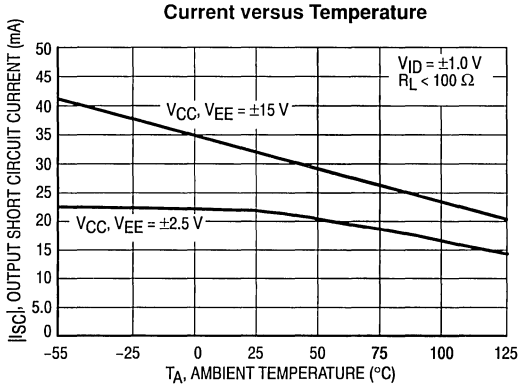


Figure 15. Power Supply Current versus Supply Voltage

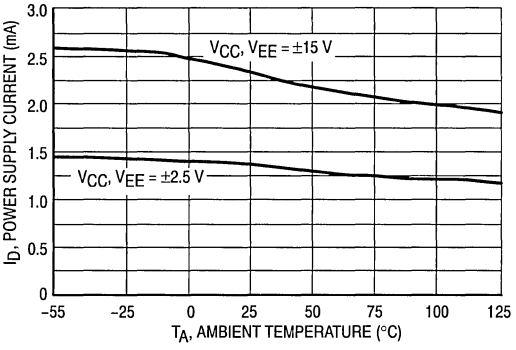


Figure 16. Slew Rate versus Temperature

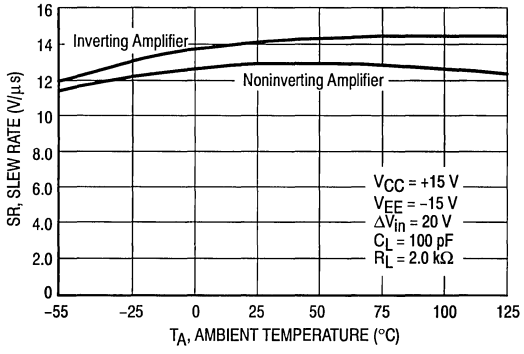


Figure 17. Gain Bandwidth Product versus Temperature

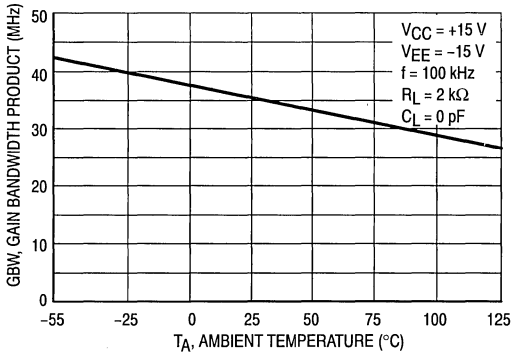


Figure 18. Gain and Phase versus Frequency

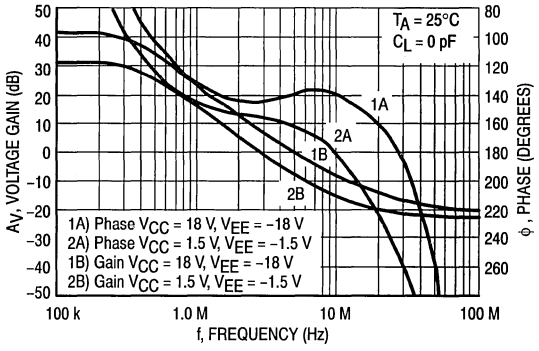
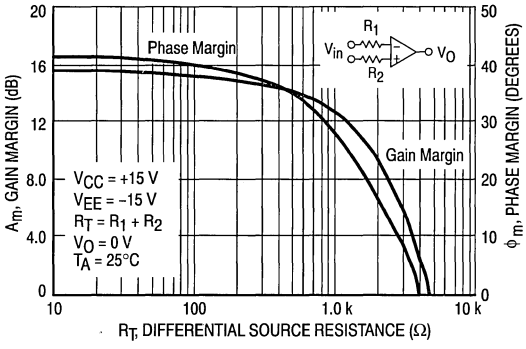


Figure 19. Phase Margin and Gain Margin versus Differential Source Resistance



2

Figure 20. Open-Loop Gain and Phase Margin versus Output Load Capacitance

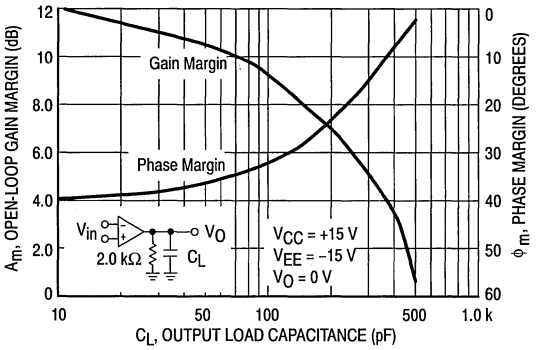


Figure 21. Gain and Phase versus Frequency

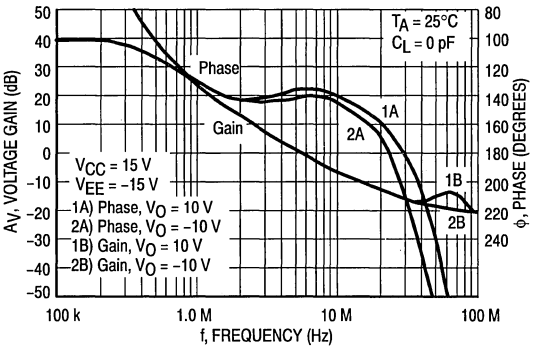


Figure 22. Channel Separation versus Frequency

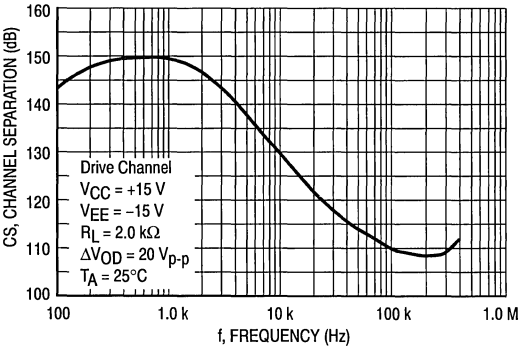


Figure 23. Total Harmonic Distortion versus Frequency

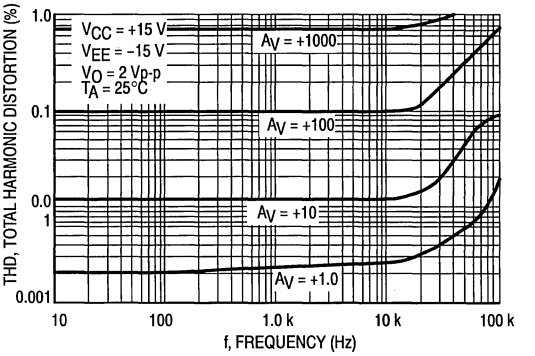


Figure 24. Output Impedance versus Frequency

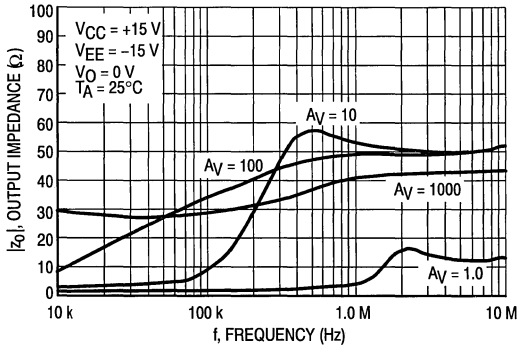


Figure 25. Input Referred Noise Voltage versus Frequency

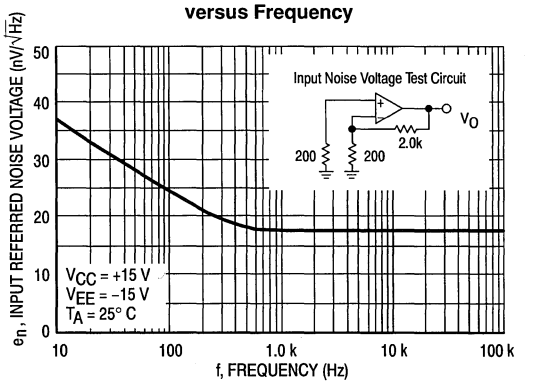


Figure 26. Percent Overshoot versus Load Capacitance

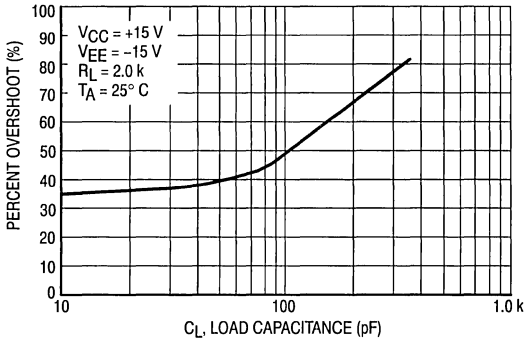


Figure 27. Noninverting Amplifier Overshoot

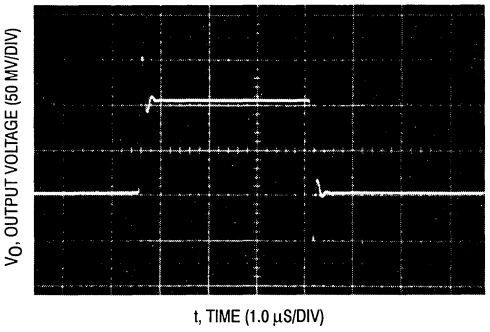


Figure 28. Noninverting Amplifier Slew Rate

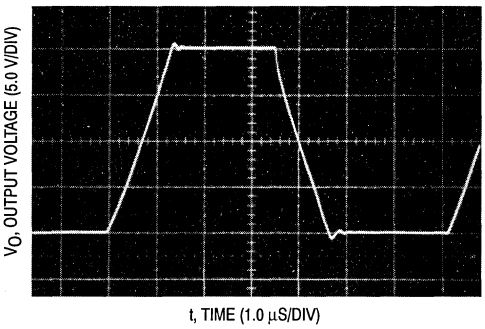
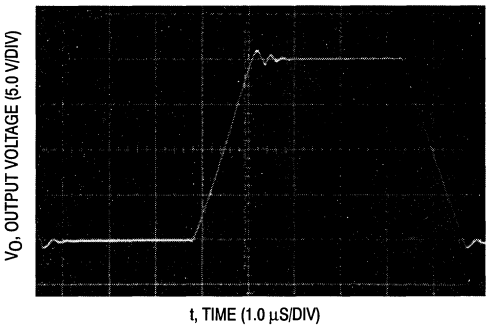


Figure 29. Inverting Amplifier Slew Rate



MC33304

QUAD SLEEP-MODE™ RAIL-TO-RAIL OPERATIONAL AMPLIFIER

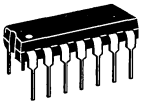
SILICON MONOLITHIC INTEGRATED CIRCUIT

Product Preview

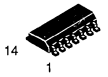
Rail-to-Rail, Sleep-Mode™ Two-State Operational Amplifier

The MC33304 quad operational amplifier provides rail-to-rail operation on both the input and output while incorporating the Sleep-Mode™ technology of the MC33102. In sleepmode, the amplifier is active and waiting for an input signal. When a signal is sensed on the input, it will automatically switch to the awakemode which offers higher slew rate, gain bandwidth, and drive capability. The output rail-to-rail operation enables the user to make full use of the supply voltage range available. It is designed to work at low supply voltages, yet can operate with a supply of up to +15 V and ground. The sleepmode function combined with a boosted output stage provide the highest possible output current capability while keeping the drain current of the amplifier to a minimum. Also, the combination of low noise and distortion with a high drive capability make this an ideal amplifier for audio applications.

- Two States: "Sleepmode" (Micropower) and "Awakemode" (High Performance)
- Automatically Changes Modes: No Additional Pins/Logic Required
- Independent Sleepmode Function for Each Op Amp
- Low Voltage, Single Supply Operation (+1.8 V, Ground to +15 V, and Ground)
- Input Voltage Range Includes Both Supply Rails
- Output Voltage Swings Within 50 mV of Both Rails
- No Phase Reversal on the Output for Overdriven Input Signals
- High Output Current
- Low Supply Current
- Low Noise
- 600 Ω Output Drive Capability
- ESD Clamps on Inputs Increase Reliability Without Affecting Device Operation

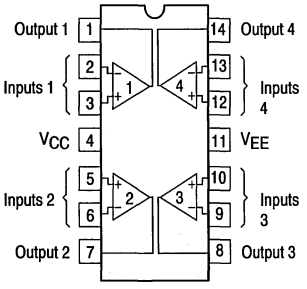


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+16	V
Input Differential Voltage Range	V_{IDR}	5.0	V
Input Voltage Range	V_{IR}	(See Note)	V
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	− 60 to +150	°C

NOTE: Either or both input voltages should not exceed V_{CC} or V_{EE}.

ORDERING INFORMATION

Device	Temperature Range	Package
MC33304D	− 40° to + 85°C	SO-14
MC33304P		Plastic DIP

MC34001, MC35001
MC34002, MC35002
MC34004, MC35004

JFET Input Operational Amplifiers

JFET INPUT OPERATIONAL AMPLIFIERS

These low cost JFET Input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

The Motorola BIFET family offers single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices. The MC35001/35002/35004 series are specified over the military operating temperature range of –55° to +125°C and the MC34001/34002/34004 series are specified from 0° to +70°C.

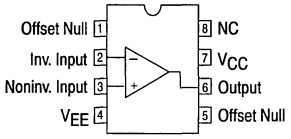
- Input Offset Voltage Options of 5.0 mV and 10 mV Maximum
- Low Input Bias Current: 40 pA
- Low Input Offset Current: 10 pA
- Wide Gain Bandwidth: 4.0 MHz
- High Slew Rate: 13 V/μs
- Low Supply Current: 1.4 mA per Amplifier
- High Input Impedance: $10^{12}\ \Omega$
- High Common Mode and Supply Voltage Rejection Ratios: 100 dB
- Industry Standard Pinouts

P SUFFIX
PLASTIC PACKAGE
CASE 626

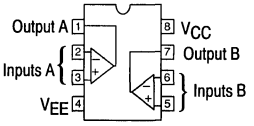
U SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

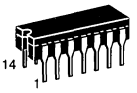
PIN CONNECTIONS



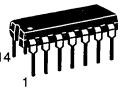
MC34001, MC35001 (Top View)



MC34002, MC35002 (Top View)

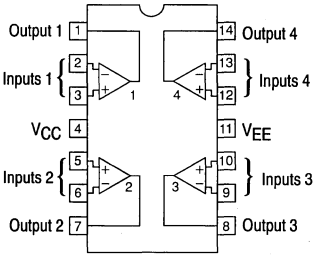


L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



MC34004, MC35004 (Top View)

ORDERING INFORMATION

Op Amp Function	Device	Temperature Range	Package
Single	MC34001BD, D	0° to+ 70°C	SO-8
	MC34001BP, P		Plastic DIP
	MC34001BU, U		Ceramic DIP
Dual	MC34002BD, D	0° to +70°C	SO-8
	MC34002BP, P		Plastic DIP
	MC35002BU, U	–55° to +125°C	Ceramic DIP
Quad	MC34004BL, L	0° to +70°C	Ceramic DIP
	MC34004BP, P		Plastic DIP
	MC35004BL, L	–55° to +125°C	Ceramic DIP

MAXIMUM RATINGS

Rating	Symbol	MC35001 MC35002 MC35004	MC34001 MC34002 MC34004	Unit
Supply Voltage	V_{CC}, V_{EE}	±22	±18	V
Differential Input Voltage (Note 1)	V_{ID}	±40	±30	V
Input Voltage Range	V_{IDR}	±20	±16	V
Open Short Circuit Duration	t_{SC}	Continuous		
Operating Ambient Temperature Range	T_A	–55 to +125	0 to +70	°C
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 150 —	 150 150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 –65 to +150 —	 –65 to +150 –55 to +125	°C

NOTES: 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	MC35001/35002/35004 Min	Typ	Max	MC34001/34002/34004 Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le 10$ k) MC3500XB, MC3400XB MC3500X, MC3400X	V_{IO}	 — —	 3.0 5.0	 5.0 10	 — —	 3.0 5.0	 5.0 10	mV
Average Temperature Coefficient of Input Offset Voltage $R_S \le 10$ k, $T_A = T_{low}$ to T_{high} (Note 2)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	µV/°C
Input Offset Current (V_{CM} = 0) (Note 3) MC3500XB, MC3400XB MC3500X, MC3400X	I_{IO}	 — —	 10 25	 50 100	 — —	 25 25	 100 100	pA
Input Bias Current (V_{CM} = 0) (Note 3) MC3500XB, MC3400XB MC3500X, MC3400X	I_{IB}	 — —	 40 50	 100 200	 — —	 50 50	 200 200	pA
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Common Mode Input Voltage Range	V_{ICR}	±11 —	+15 –12	— —	±11 —	+15 –12	— —	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k) MC3500XB, MC3400XB MC3500X, MC3400X	A_{VOL}	 50 25	 150 100	 — —	 50 25	 150 100	 — —	V/mV
Output Voltage Swing ($R_L \ge 10$ k) ($R_L \ge 2.0$ k)	V_O	 ±12 ±10	 ±14 ±13	 — —	 ±12 ±10	 ±14 ±13	 — —	V
Common Mode Rejection Ratio ($R_S \le 10$ k) MC3500XB, MC3400XB MC3500X, MC3400X	CMRR	 80 —	 100 —	 — —	 80 70	 100 100	 — —	dB
Supply Voltage Rejection Ratio ($R_S \le 10$ k) (Note 4) MC3500XB, MC3400XB MC3500X, MC3400X	PSRR	 80 70	 100 100	 — —	 80 70	 100 100	 — —	dB
Supply Current (Each Amplifier) MC3500XB, MC3400XB MC3500X, MC3400X	I_D	 — —	 1.4 1.4	 2.5 2.7	 — —	 1.4 1.4	 2.5 2.7	mA
Slew Rate (A_V = 1.0)	SR	—	13	—	—	13	—	V/µs
Gain-Bandwidth Product	GBW	—	4.0	—	—	4.0	—	MHz
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1000 Hz)	e_n	—	25	—	—	25	—	nV/$\sqrt{Hz}$
Equivalent Input Noise Current (f = 1000 Hz)	i_n	—	0.01	—	—	0.01	—	pA/$\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} [Note 2].)

Characteristics	Symbol	MC35001/35002/35004			MC34001/34002/34004			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S ≤ 10 k) MC3500XB, MC3400XB MC3500X, MC3400X	V_{IO}	 — —	 — —	 7.0 14	 — —	 — —	 7.0 13	mV
Input Offset Current (V_{CM} = 0) (Note 3) MC3500XB, MC3400XB MC3500X, MC3400X	I_{IO}	 — —	 — —	 40 40	 — —	 — —	 4.0 4.0	nA
Input Bias Current (V_{CM} = 0) (Note 3) MC3500XB, MC3400XB MC3500X, MC3400X	I_{IB}	 — —	 — —	 50 50	 — —	 — —	 8.0 8.0	nA
Common Mode Input Voltage Range	V_{ICR}	±11	—	—	±11	—	—	V
Large Signal (V_O = ±10 V, R_L = 2.0 k) MC3500XB, MC3400XB MC3500X, MC3400X	A_{VOL}	 25 15	 — —	 — —	 25 15	 — —	 — —	V/mV
Output Voltage Swing (R ≥ 10 k) (R ≥ 2.0 k)	V_O	 ±12 ±10	 — —	 — —	 ±12 ±10	 — —	 — —	V
Common Mode Rejection Ratio (R_S ≤ 10 k) MC3500XB, MC3400XB MC3500X, MC3400X	CMRR	 80 70	 — —	 — —	 80 70	 — —	 — —	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 k) (Note 4) MC3500XB, MC3400XB MC3500X, MC3400X	PSRR	 80 70	 — —	 — —	 80 70	 — —	 — —	dB
Supply Current (Each Amplifier) MC3500XB, MC3400XB MC3500X, MC3400X	I_D	 — —	 — —	 2.8 3.0	 — —	 — —	 2.8 3.0	mA

NOTES: 2. T_{low} = −55°C for MC35001/35001B, MC35002/35002B, MC35004/35004B; = 0°C for MC34001/34001B, MC34002/35002B, MC34004/34004B. T_{high} = +125°C for MC35001/35001B, MC35002/35002B, MC35004/35004B; = +70°C for MC34001/34001B, MC34002/35002B, MC34004/34004B.

3. The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heatsink is recommended if input bias current is to be kept to a minimum.
4. Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

2

Figure 1. Input Bias Current versus Temperature

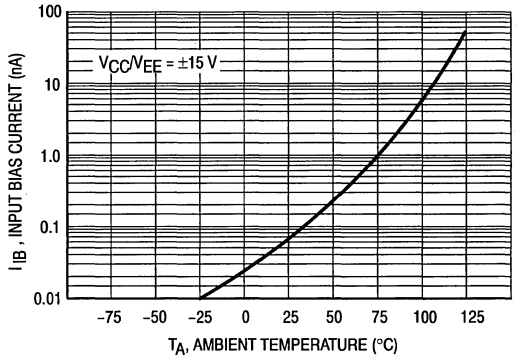


Figure 2. Output Voltage Swing versus Frequency

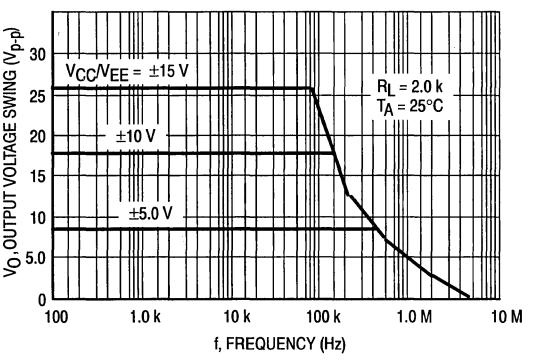


Figure 3. Output Voltage Swing versus Load Resistance

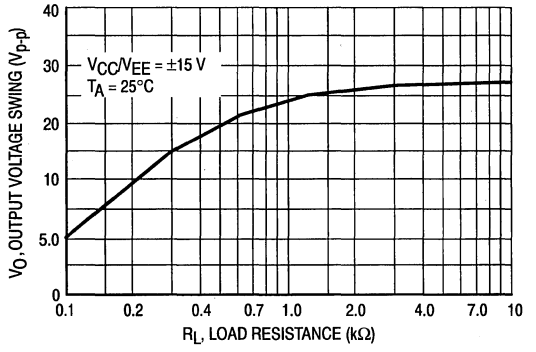


Figure 4. Output Voltage Swing versus Supply Voltage

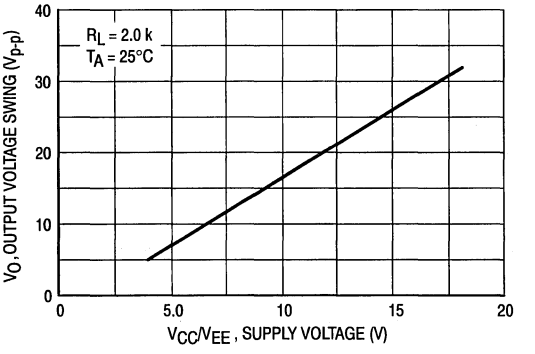


Figure 5. Output Voltage Swing versus Temperature

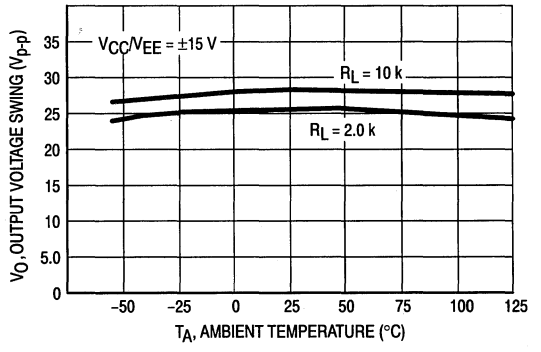


Figure 6. Supply Current per Amplifier versus Temperature

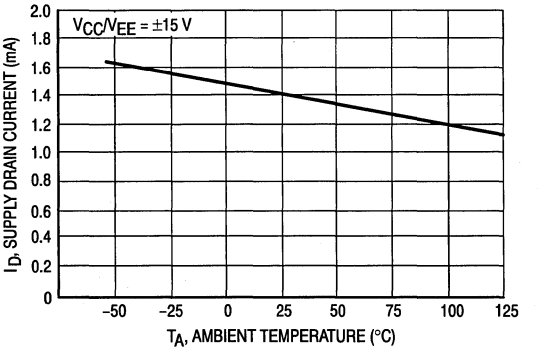


Figure 7. Large-Signal Voltage Gain and Phase Shift versus Frequency

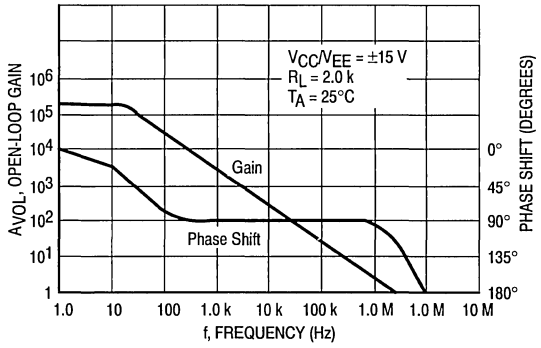


Figure 8. Large-Signal Voltage Gain versus Temperature

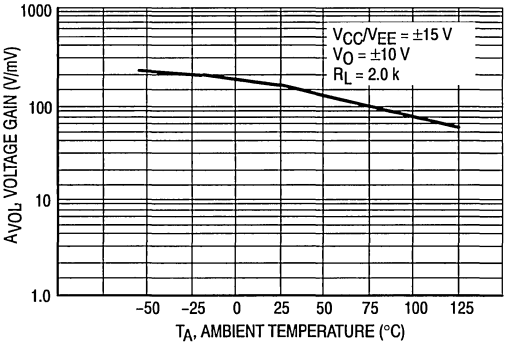


Figure 9. Normalized Slew Rate versus Temperature

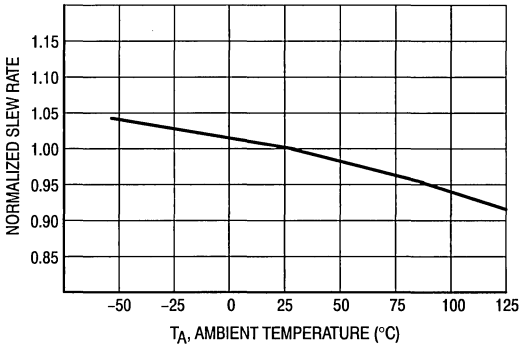


Figure 10. Equivalent Input Noise Voltage versus Frequency

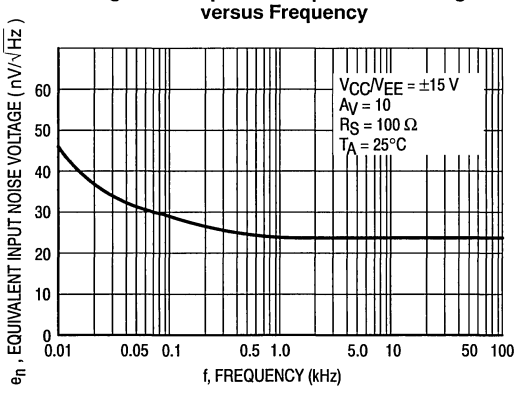
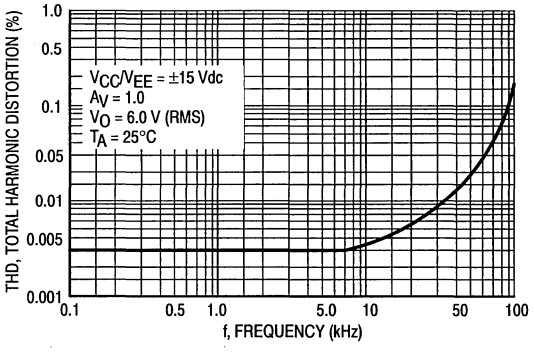


Figure 11. Total Harmonic Distortion versus Frequency



2

Representative Circuit Schematic
(Each Amplifier)

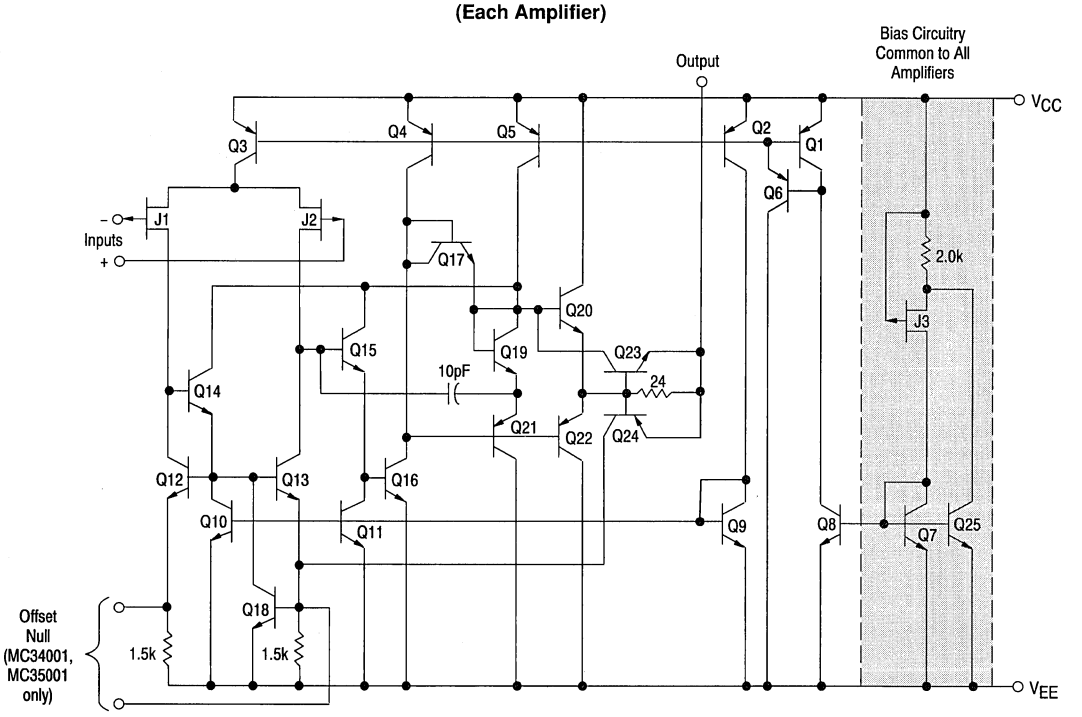
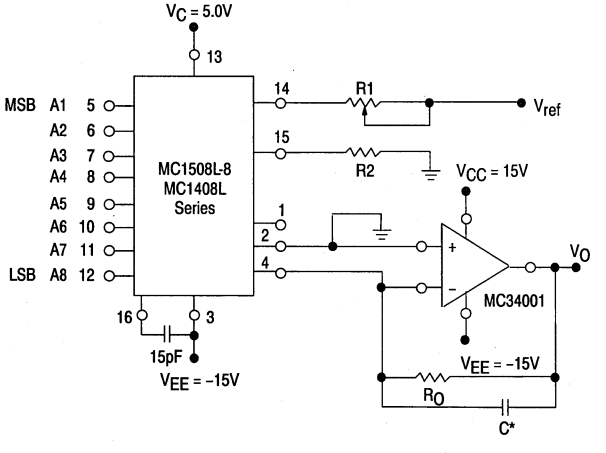


Figure 12. Output Current to Voltage Transformation for a D-to-A Converter



Settling time to within 1/2 LSB (±19.5 mV) is approximately 4.0 μs from the time all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF)

Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R_1 or R_O so that V_O with all digital inputs at high level is equal to 9.961 V.

V_{ref} = 2.0 Vdc
$R_I = R2 \approx 1.0\ k\Omega$
$R_O = 5.0\ k\Omega$

$$V_O = \frac{2.0\ V}{1.0\ k}(5\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

Figure 13. Positive Peak Detector

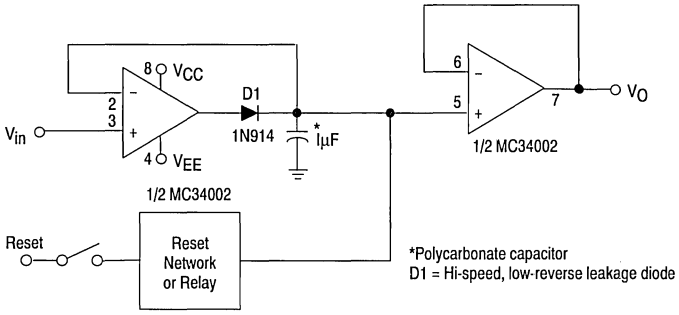
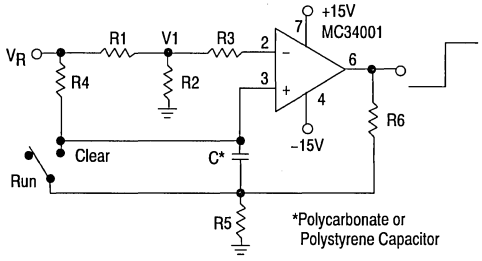


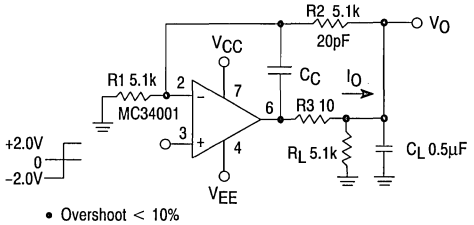
Figure 14. Long Interval RC Timer



Time (t) = R4 Cn (V_R/V_R-V_I), $R_3 = R_4$, $R_5 = 0.1\ R_6$
If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer
V_R = 10 V C = I.0 μF R3 = R4 = 144 M
R6 = 20 k R5 = 2.0 k R1 = R2 = 1.0 k

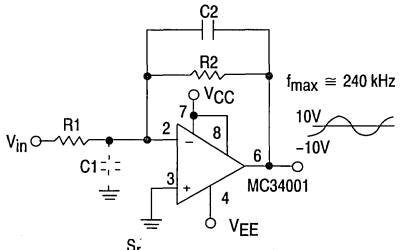
Figure 15. Isolating Large Capacitive Loads



- Overshoot < 10%
- t_S = 10 μs
- When driving large C_L, the V_O slew rate is determined by C_L and $I_{O(max)}$:

$$\frac{\Delta V_O}{\Delta t} = \frac{I_O}{C_L} = \frac{0.02}{0.5}\ \text{V/μs} = 0.04\ \text{V/μs (with } C_L \text{ shown)}$$

Figure 16. Wide BW, Low Noise, Low Drift Amplifier



- Power BW: $f_{max} = \frac{S_r}{2\pi V_p} \cong 240\ \text{kHz}$
- Parasitic input capacitance (C1 ≅ 3.0 pF plus any additional layout capacitance) interacts with feedback elements and creates undesirable high-frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

MC34071,2,4
MC35071,2,4
MC33071,2,4

2

High Slew Rate, Wide Bandwidth, Single Supply Operational Amplifiers

Quality bipolar fabrication with innovative design concepts are employed for the MC33071/72/74, MC34071/72/74, MC35071/72/74 series of monolithic operational amplifiers. This series of operational amplifiers offer 4.5 MHz of gain bandwidth product, 13 V/μs slew rate and fast setting time without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). With A Darlington input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33071/72/74, MC34071/72/73, MC35071/72/74 series of devices are available in standard or prime performance (A Suffix) grades and are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in the plastic, ceramic DIP and SOIC surface mount packages.

- Wide Bandwidth: 4.5 MHz
- High Slew Rate: 13 V/μs
- Fast Settling Time: 1.1 μs to 0.1%
- Wide Single Supply Operation: 3.0 V to 44 V
- Wide Input Common Mode Voltage Range: Includes Ground (V_{EE})
- Low Input Offset Voltage: 3.0 mV Maximum (A Suffix)
- Large Output Voltage Swing: −14.7 V to +14 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 pF to 10,000 pF
- Low Total Harmonic Distortion: 0.02%
- Excellent Phase Margin: 60°
- Excellent Gain Margin: 12 dB
- Output Short Circuit Protection
- ESD Diodes/Clamps Provide Input Protection for Dual, and Quad

ORDERING INFORMATION

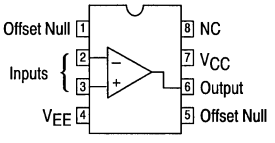
Op Amp Function	Device	Temperature Range	Package
Single	MC34071P, AP MC34071D, AD MC34071U, AU	0° to +70°C	Plastic DIP SO-8 Ceramic DIP
	MC33071P, AP MC33071D, AD MC33071U, AU	−40° to +85°C	Plastic DIP SO-8 Ceramic DIP
	MC35071U, AU	−55° to +125°C	Ceramic DIP
Dual	MC34072P, AP MC34072D, AD MC34072U, AU	0° to +70°C	Plastic DIP SO-8 Ceramic DIP
	MC33072P, AP MC33072D, AD MC33072U, AU	−40° to +85°C	Plastic DIP SO-8 Ceramic DIP
	MC35072U, AU	−55° to +125°C	Ceramic DIP
Quad	MC34074P, AP MC34074D, AD MC34074L, AL	0° to +70°C	Plastic DIP SO-14 Ceramic DIP
	MC33074P, AP MC33074D, AD MC33074L, AL	−40° to +85°C	Plastic DIP SO-14 Ceramic DIP
	MC35074L, AL	−55° to +125°C	Ceramic DIP

P SUFFIX
PLASTIC PACKAGE
CASE 626

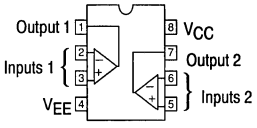
U SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

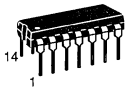
PIN CONNECTIONS



(Single, Top View)

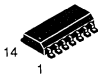


(Dual, Top View)



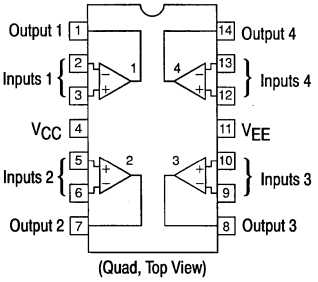
P SUFFIX
PLASTIC PACKAGE
CASE 646

L SUFFIX
CERAMIC PACKAGE
CASE 632



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



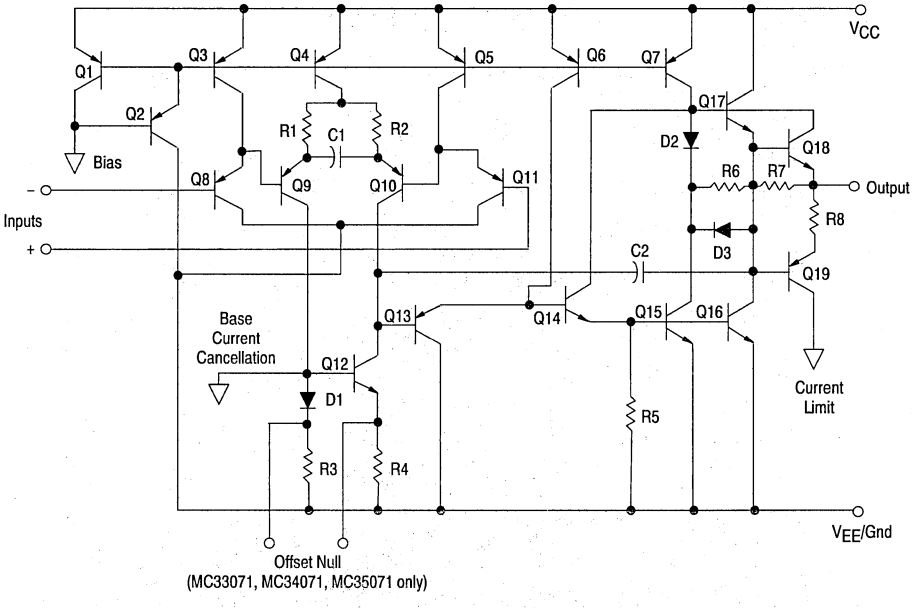
(Quad, Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{EE} to V_{CC})	V_S	+44	V
Input Differential Voltage Range	V_{IDR}	Note 1	V
Input Voltage Range	V_{IR}	Note 1	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 +160 +150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 −65 to +160 −60 to +150	°C

NOTES: 1. Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

Equivalent Circuit Schematic
(Each Amplifier)



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L = connected to ground, unless otherwise noted. See [Note 3] for $T_A = T_{low}$ to T_{high})

Characteristics	Symbol	A Suffix			Non-Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S = 100 Ω, V_{CM} = 0 V, V_O = 0 V) V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, $T_A = T_{low}$ to T_{high}	V_{IO}	— — —	0.5 0.5 —	3.0 3.0 5.0	— — —	1.0 1.5 —	5.0 5.0 7.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, $T_A = T_{low}$ to T_{high}	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	μV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C $T_A = T_{low}$ to T_{high}	I_{IB}	— —	100 —	500 700	— —	100 —	500 700	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0V) T_A = +25°C $T_A = T_{low}$ to T_{high}	I_{IO}	— —	6.0 —	50 300	— —	6.0 —	75 300	nA
Input Common Mode Voltage Range T_A = +25°C $T_A = T_{low}$ to T_{high}	V_{ICR}	V_{EE} to (V_{CC} −1.8) V_{EE} to (V_{CC} −2.2)			V_{EE} to (V_{CC} −1.8) V_{EE} to (V_{CC} −2.2)			V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ) T_A = +25°C $T_A = T_{low}$ to T_{high}	A_{VOL}	50 25	100 —	— —	25 20	100 —	— —	V/mV
Output Voltage Swing (V_{ID} = ±1.0 V) V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 kΩ, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kΩ, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 2.0 kΩ, $T_A = T_{low}$ to T_{high}	V_{OH}	3.7 13.6 13.4	4.0 14 —	— — —	3.7 13.6 13.4	4.0 14 —	— — —	V
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 kΩ, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 10 kΩ, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, R_L = 2.0 kΩ, $T_A = T_{low}$ to T_{high}	V_{OL}	— — —	0.1 −14.7 —	0.3 −14.3 −13.5	— — —	0.1 −14.7 —	0.3 −14.3 −13.5	V
Output Short Circuit Current (V_{ID} = 1.0 V, V_O = 0 V, T_A = 25°C) Source Sink	I_{SC}	10 20	30 30	— —	10 20	30 30	— —	mA
Common Mode Rejection R_S = 100 kΩ, $V_{CM} = V_{ICR}$, T_A = 25°C	CMR	80	97	—	70	97	—	dB
Power Supply Rejection (R_S = 100 Ω) V_{CC}/V_{EE} = +16.5 V/−16.5 V to +13.5 V/−13.5 V, T_A = 25°C	PSR	80	97	—	70	97	—	dB
Power Supply Current (Per Amplifier, No Load) V_{CC} = +5.0 V, V_{EE} = 0 V, V_O = +2.5 V, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, V_O = 0 V, T_A = +25°C V_{CC} = +15 V, V_{EE} = −15 V, V_O = 0 V, $T_A = T_{low}$ to T_{high}	I_D	— — —	1.6 1.9 —	2.0 2.5 2.8	— — —	1.6 1.9 —	2.0 2.5 2.8	mA

NOTES: 3. T_{low} = −55°C for MC35071 ,2 ,4, /A
= −40°C for MC33071, 2, 4, /A
= 0°C for MC34071, 2, 4, /A
T_{high} = +125°C for MC35071, 2, 4, /A
= +85°C for MC33071, 2, 4, /A
= +70°C for MC34071, 2, 4, /A

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L = connected to ground T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	A Suffix			Non-Suffix			Unit
		Min	Typ	Max	Min	Typ	Max	
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 500 pF) A_V = +1.0 A_V = −1.0	SR	 8.0 —	 10 13	 — —	 8.0 —	 10 13	 — —	V/μs
Setting Time (10 V Step, A_V = −1.0) To 0.1% (+1/2 LSB of 9-Bits) To 0.01% (+1/2 LSB of 12-Bits)	t_s	 — —	 1.1 2.2	 — —	 — —	 1.1 2.2	 — —	μs
Gain Bandwidth Product (f = 100 kHz)	GBW	3.5	4.5	—	3.5	4.5	—	MHz
Power Bandwidth A_V = +1.0, R_L = 2.0 kΩ, V_O = 20 V_{p-p}, THD = 5.0%	BW	—	160	—	—	160	—	kHz
Phase margin R_L = 2.0 kΩ R_L = 2.0 kΩ, C_L = 300 pF	ϕ_m	 — —	 60 40	 — —	 — —	 60 40	 — —	Deg
Gain Margin R_L = 2.0 kΩ R_L = 2.0 kΩ, C_L = 300 pF	A_m	 — —	 12 4.0	 — —	 — —	 12 4.0	 — —	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	32	—	—	32	—	nV/$\sqrt{Hz}$
Equivalent Input Noise Current f = 1.0 kHz	i_n	—	0.22	—	—	0.22	—	pA/$\sqrt{Hz}$
Differential Input Resistance V_{CM} = 0 V	R_{IN}	—	150	—	—	150	—	MΩ
Differential Input Capacitance V_{CM} = 0 V	C_{IN}	—	2.5	—	—	2.5	—	pF
Total Harmonic Distortion A_V = +10, R_L = 2.0 kΩ, 2.0 $V_{p-p} \le V_O \le$ 20 V_{p-p}, f = 10 kHz	THD	—	0.02	—	—	0.02	—	%
Channel Separation (f = 10 kHz)	—	—	120	—	—	120	—	dB
Open-Loop Output Impedance (f = 1.0 MHz)	$\|Z_O\|$	—	30	—	—	30	—	Ω

Figure 1. Power Supply Configurations

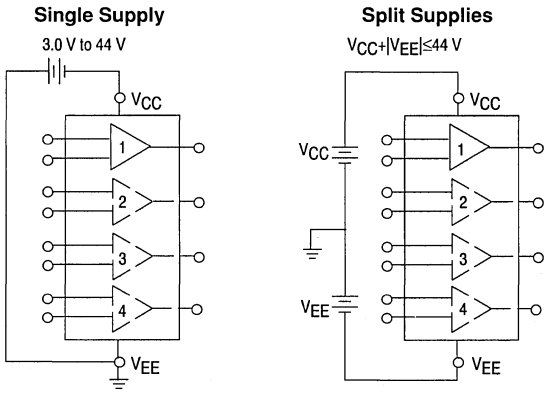
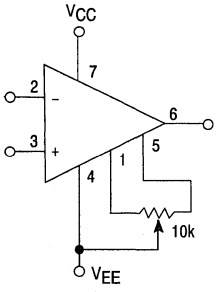


Figure 2. Offset Null Circuit



Offset nulling range is approximately ±80 mV with a 10 k potentiometer (MC33071, MC34071, MC35071 only).

2

Figure 3. Maximum Power Dissipation versus Temperature for Package Types

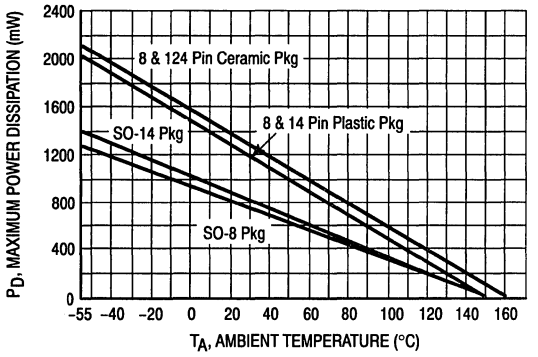


Figure 4. Input Offset Voltage versus Temperature for Representative Units

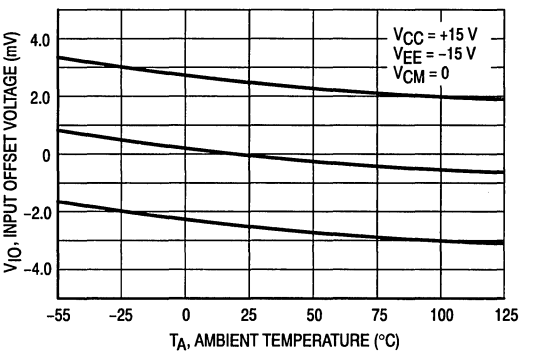


Figure 5. Input Common Mode Voltage Range versus Temperature

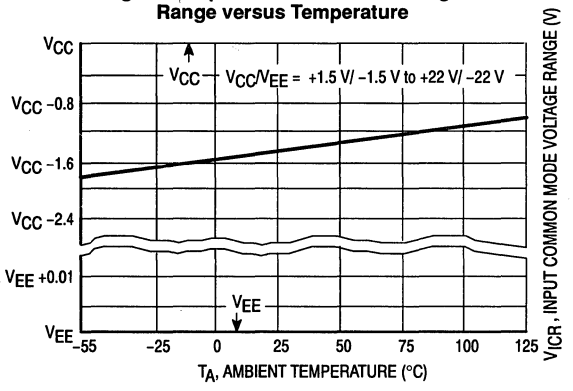


Figure 6. Normalized Input Bias Current versus Temperature

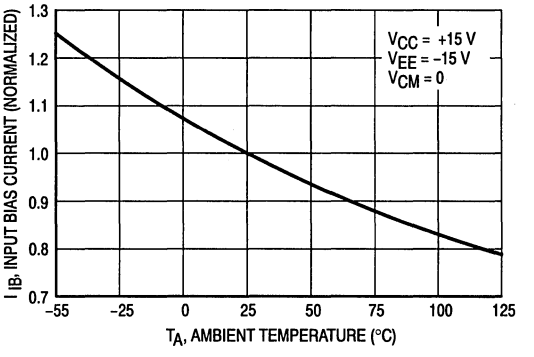


Figure 7. Normalized Input Bias Current versus Input Common Mode Voltage

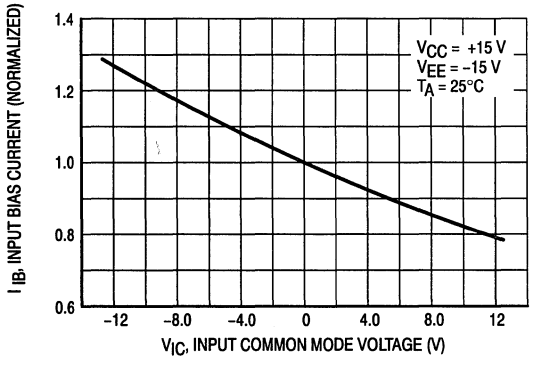


Figure 8. Split Supply Output Voltage Swing versus Supply Voltage

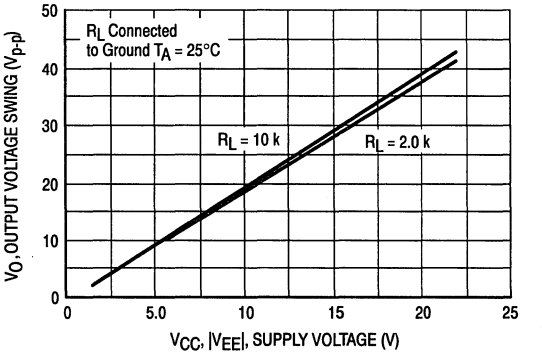


Figure 9. Split Supply Output Saturation versus Load Current

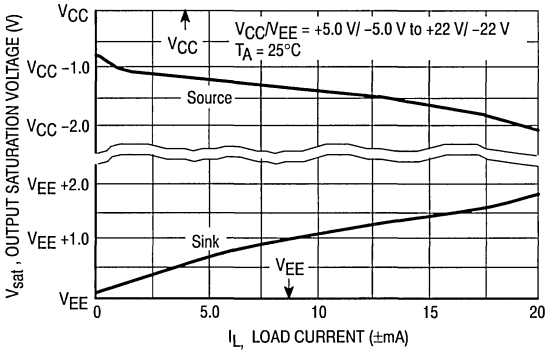


Figure 10. Single Supply Output Saturation versus Load Resistance to Ground

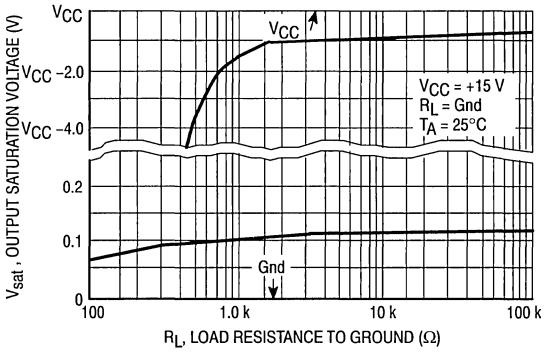


Figure 11. Single Supply Output Saturation versus Load Resistance to V_{CC}

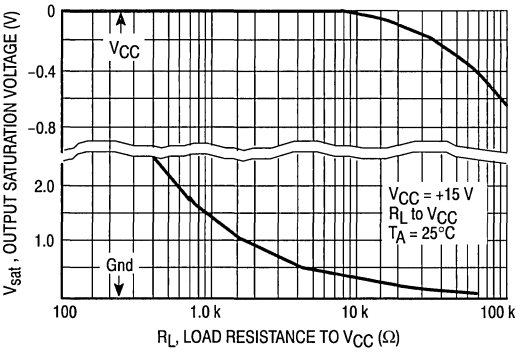


Figure 12. Output Short Circuit Current versus Temperature

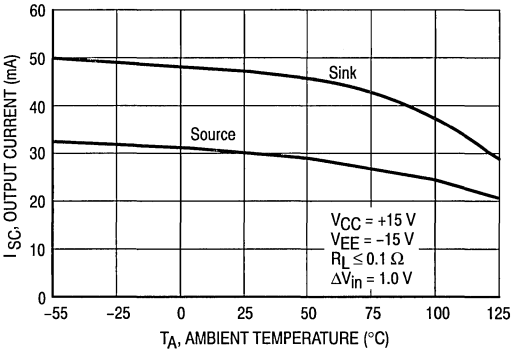


Figure 13. Output Impedance versus Frequency

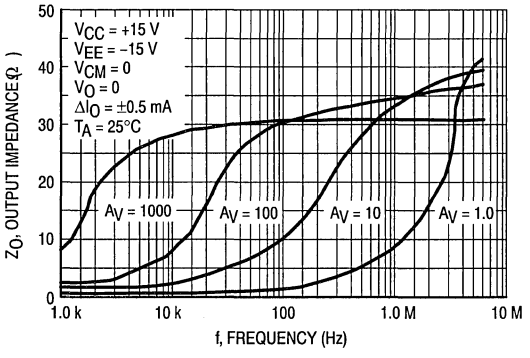
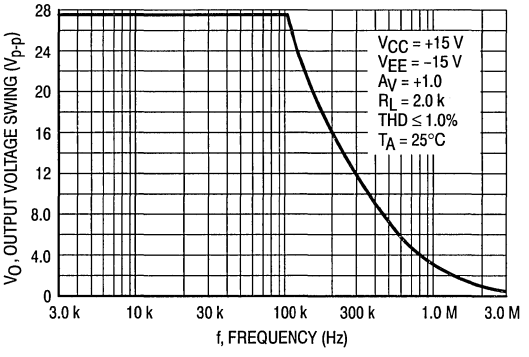


Figure 14. Output Voltage Swing versus Frequency



2

Figure 15. Output Distortion versus Frequency

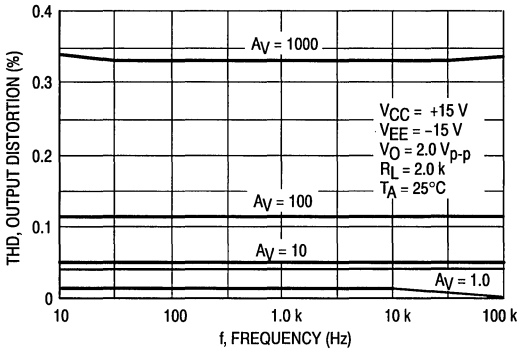


Figure 16. Output Distortion versus Output Voltage Swing

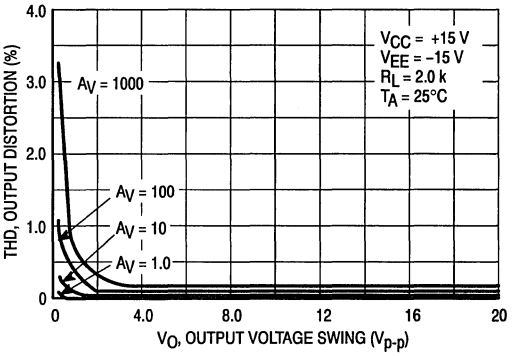


Figure 17. Open-Loop Voltage Gain versus Temperature

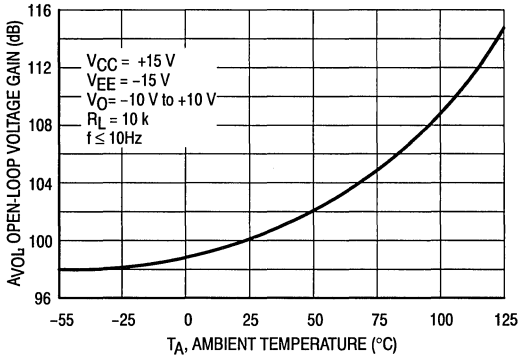


Figure 18. Open-Loop Voltage Gain and Phase versus Frequency

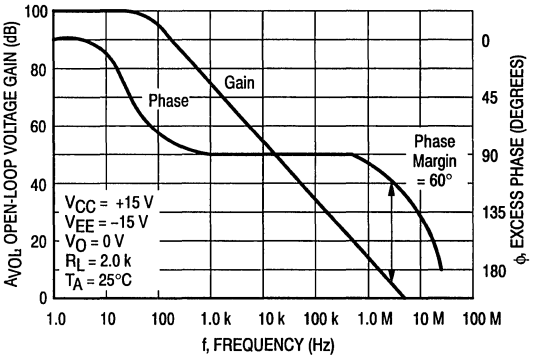


Figure 19. Open-Loop Voltage Gain and Phase versus Frequency

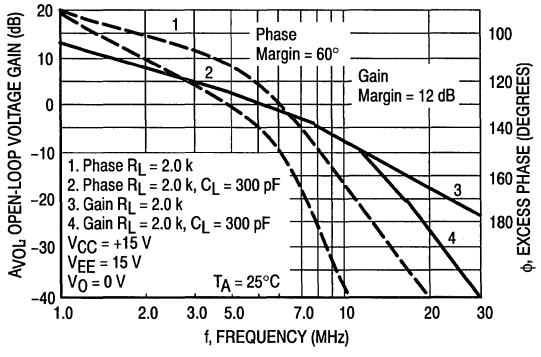


Figure 20. Normalized Gain Bandwidth Produt versus Temperature

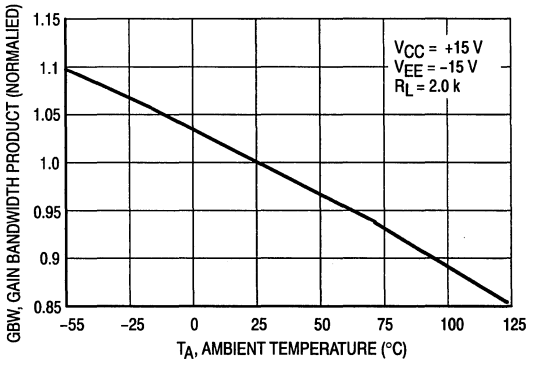


Figure 21. Percent Overshoot versus Load Capacitance

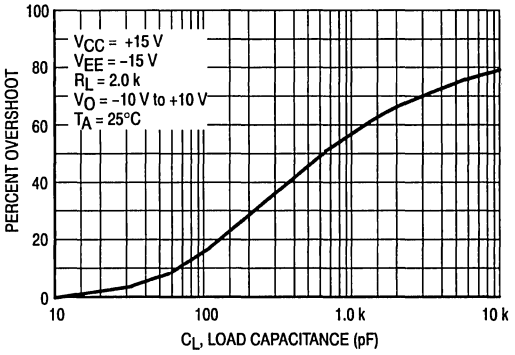


Figure 22. Phase Margin versus Load Capacitance

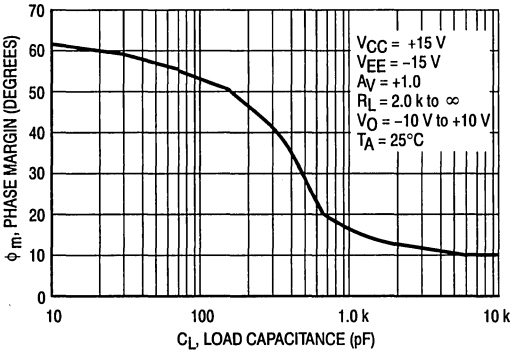


Figure 23. Gain Margin versus Load Capacitance

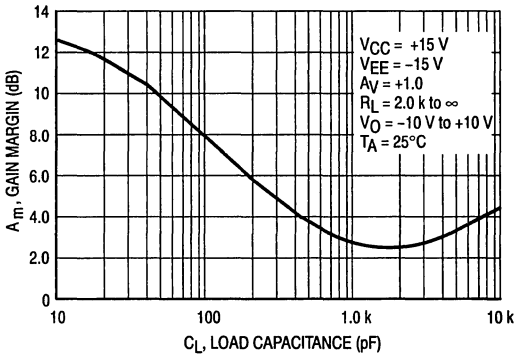


Figure 24. Phase Margin versus Temperature

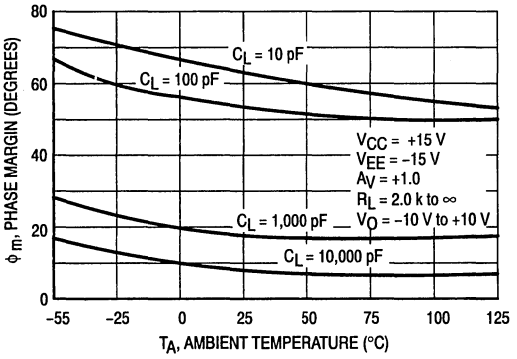


Figure 25. Gain Margin versus Temperature

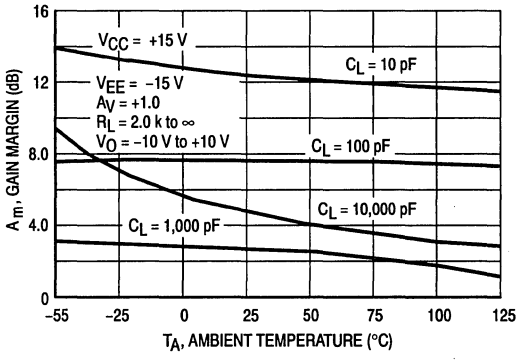


Figure 26. Phase Margin and Gain Margin versus Differential Source Resistance

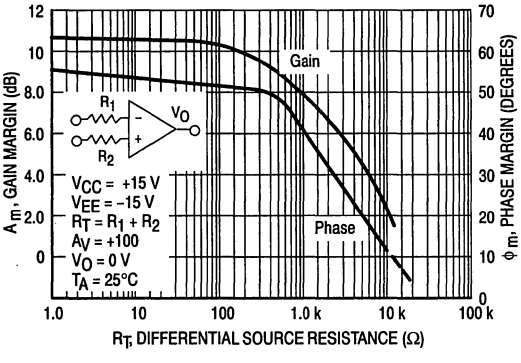


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Figure 27. Normalized Slew Rate versus Temperature

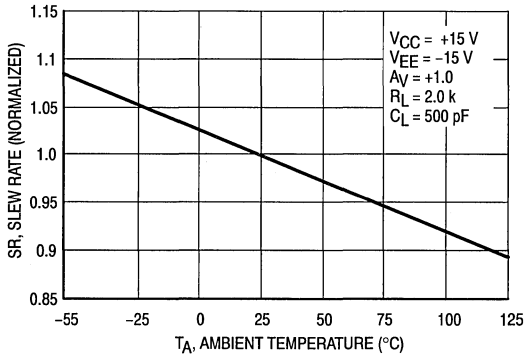


Figure 28. Output Settling Time

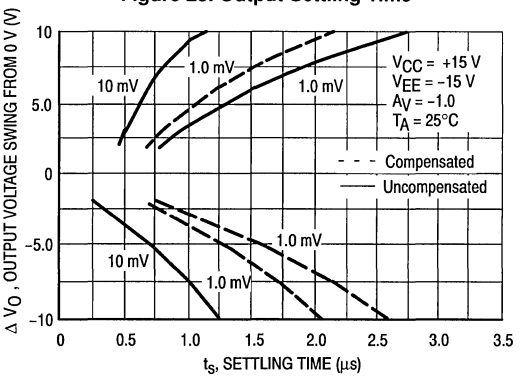


Figure 29. Small Signal Transient Response

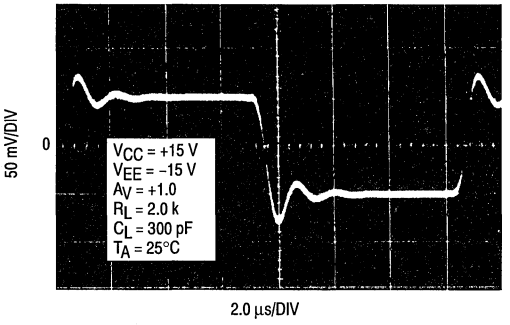


Figure 30. Large Signal Transient Reponse

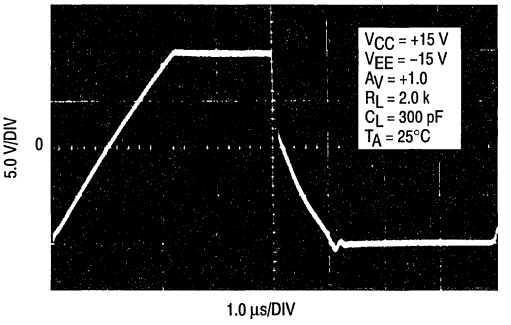


Figure 31. Common Mode Rejection versus Frequency

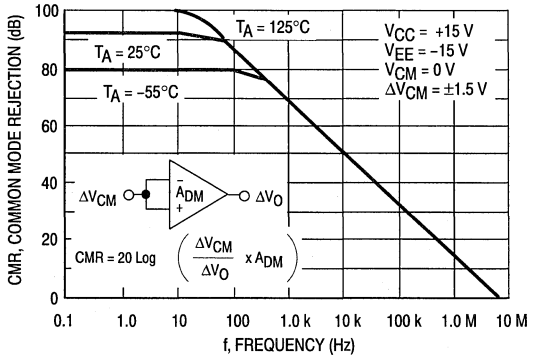


Figure 32. Power Supply Rejection versus Frequency

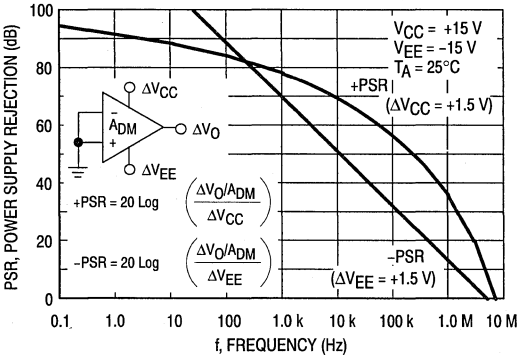


Figure 33. Supply Current versus Supply Voltage

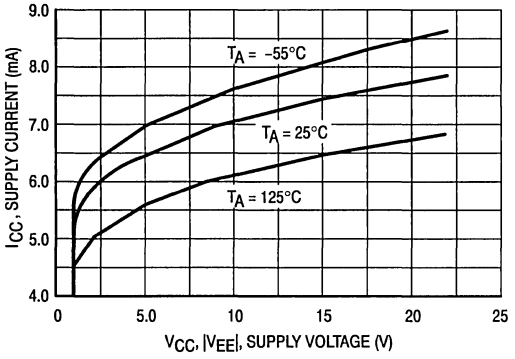


Figure 34. Power Supply Rejection versus Temperature

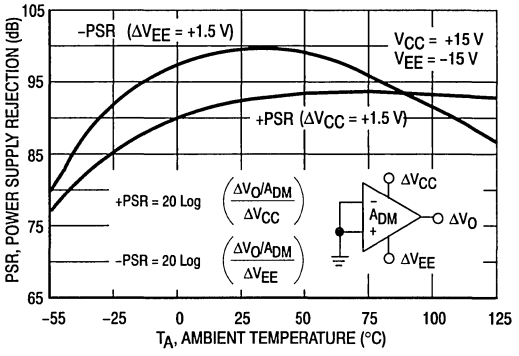


Figure 35. Channel Separation versus Frequency

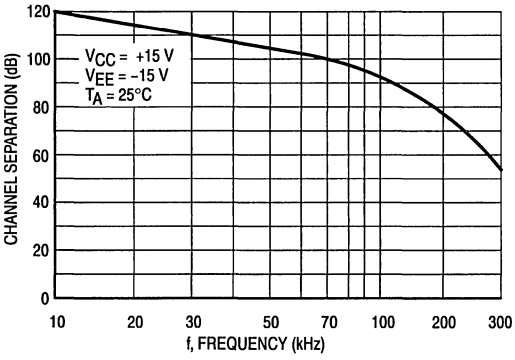
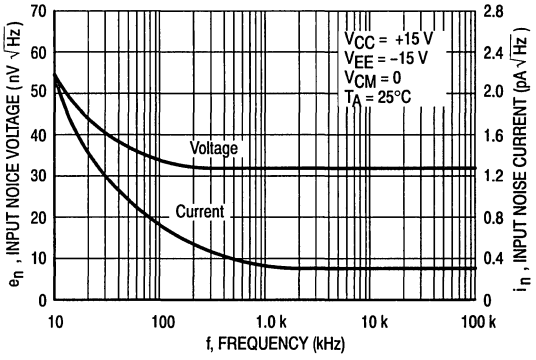


Figure 36. Input Noise versus Frequency



APPLICATIONS INFORMATION
CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC34071 amplifier series are similar to op amp products utilizing JFET input devices, these amplifiers offer other additional distinct advantages as a result of the PNP transistor differential input stage and an all NPN transistor output stage.

Since the input common mode voltage range of this input stage includes the V_{EE} potential, single supply operation is feasible to as low as 3.0 V with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 V, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between V_{EE} and V_{CC} supply voltages as shown by the maximum rating table. In practice, although not recommended, the input voltages can exceed the V_{CC} voltage by approximately 3.0 V and decrease below the V_{EE} voltage by 0.3 V without causing product damage, although output phase reversal may occur. It is also possible to source up to approximately 5.0 mA of current from V_{EE} through either inputs clamping diode without damage or latching, although phase reversal may again occur.

If one or both inputs exceed the upper common mode voltage limit the amplifier output is readily predictable and may be in a low or high state depending on the existing input bias conditions.

Since the input capacitance associated with the small geometry input device is substantially lower (2.5 pF) than the typical JFET input gate capacitance (5.0 pF), better frequency response for a given input source resistance can be achieved using the MC34071 series of amplifiers. This performance feature becomes evident, for example, in fast settling D-to-A current to voltage conversion applications where the feedback resistance can form an input pole with the input capacitance of the op amp. This input pole creates a 2nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DACs). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 2.0 kΩ of feedback resistance, the MC34071 series can settle to within 1/2 LSB of 8 bits in 1.0 μs, and within 1/2 LSB of 12-bits in 2.2 μs for a 10 V step. In a inverting unity gain fast settling configuration, the symmetrical slew rate is ±13 V/μs. In the classic noninverting unity gain configuration the output positive slew rate is +10 V/μs, and the corresponding negative slew rate will exceed the positive slew rate as a function of the fall time of the input waveform.

Since the bipolar input device matching characteristics are superior to that of JFETs, a low untrimmed maximum offset voltage of 3.0 mV prime and 5.0 mV downgrade can be economically offered with high frequency performance characteristics. This combination is ideal for low cost precision, high speed quad op amp applications.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 kΩ load resistance can swing within 1.0 V of the positive rail (V_{CC}), and within 0.3 V of the negative rail (V_{EE}), providing a 28.7 V_{p-p} swing from ±15 V supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q_7, and V_{BE} of the NPN pull up transistor Q_{17}, and the voltage drop associated with the short circuit resistance, R_7. The negative swing is limited by the saturation voltage of the pull-down transistor Q_{16}, the voltage drop $I_L R_6$, and the voltage drop associated with resistance R_7, where I_L is the sink load current. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of V_{EE}. For large valued sink currents (>5.0 mA), diode D3 clamps the voltage across R_6, thus limiting the negative swing to the saturation voltage of Q_{16}, plus the forward diode drop of D3 ($\approx V_{EE}$ +1.0 V). Thus for a given supply voltage, unprecedented peak-to-peak output voltage swing is possible as indicated by the output swing specifications.

If the load resistance is referenced to V_{CC} instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull up capability.

Because the PNP output emitter-follower transistor has been eliminated, the MC34071 series offers a 20 mA minimum current sink capability, typically to an output voltage of (V_{EE} +1.8 V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for fast high current switching applications.

In addition, the all NPN transistor output stage is inherently fast, contributing to the bipolar amplifier's high gain bandwidth product and fast settling capability. The associated high frequency low output impedance (30 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 pF to 10,000 pF without oscillation in the unity closed-loop gain configuration. The 60° phase margin and 12 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The high frequency characteristics of the MC34071 series also allow excellent high frequency active filter capability, especially for low voltage single supply applications.

Although the single supply specifications is defined at 5.0 V, these amplifiers are functional to 3.0 V @ 25°C although slight changes in parametrics such as bandwidth, slew rate, and DC gain may occur.

If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

Special static precautions are not necessary for these bipolar amplifiers since there are no MOS transistors on the die.

As usual with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input-output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ±15 V supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

TYPICAL SINGLE SUPPLY APPLICATIONS V_{CC} = 5.0 V

Figure 37. AC Coupled Noninverting Amplifer

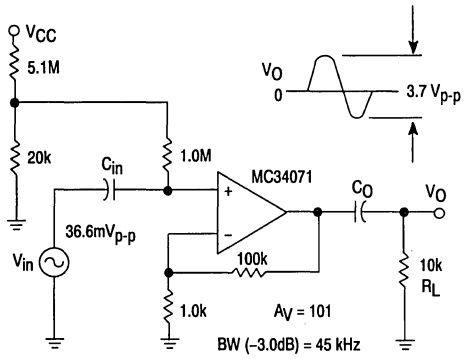


Figure 38. AC Coupled Inverting Amplifier

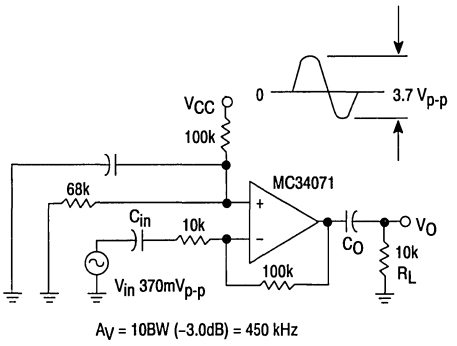


Figure 39. DC Coupled Inverting Amplifer Maximum Output Swing

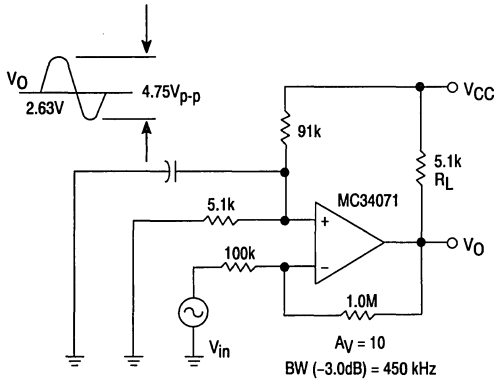


Figure 40. Unity Gain Buffer TTL Driver

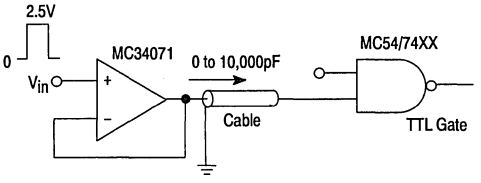


Figure 41. Active High-Q Notch Filter

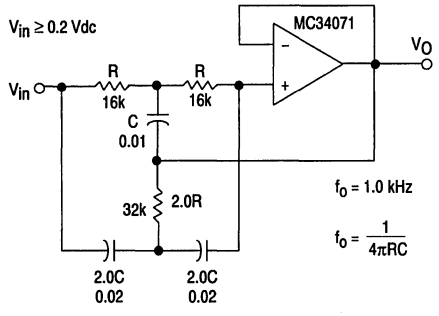
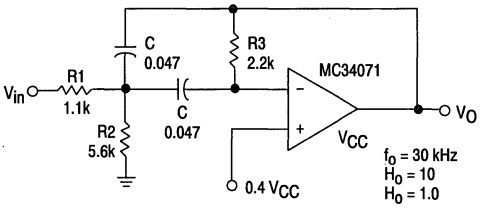


Figure 42. Active Bandpass Filter



Given f_0 = Center Frequency
A_O = Gain at Center Frequency
Choose Value f_0, Q, A_O, C
Then:

$$R3 = \frac{Q}{\pi f_0 C} \qquad R1 = \frac{R3}{2H_0} \qquad R2 = \frac{R1\,R3}{4Q^2R1 - R3}$$

For less than 10% error from operational amplifier

$$\frac{Q_0 f_0}{GBW} < 0.1$$

Where f_0 and GBW are expressed in Hz.
GBW = 4.5 MHz Typ.

2

Figure 43. Low Voltage Fast D/A Converter

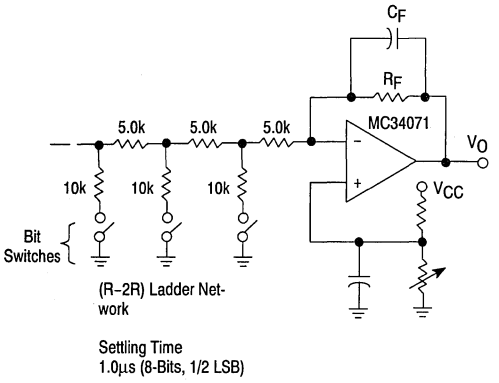


Figure 44. High Speed Low Voltage Comparator

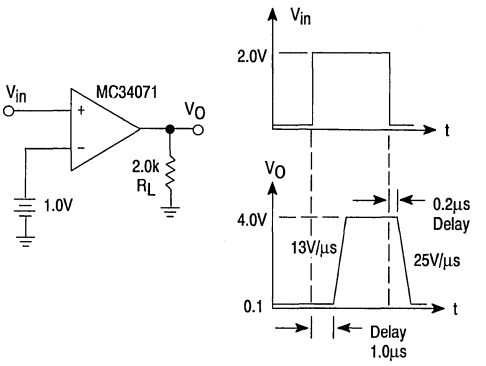


Figure 45. LED Driver

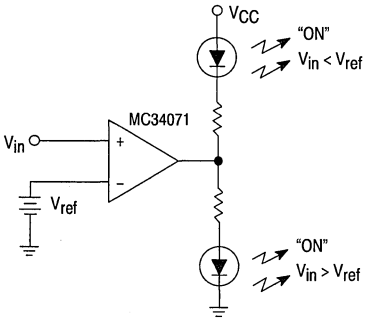


Figure 46. Transistor Driver

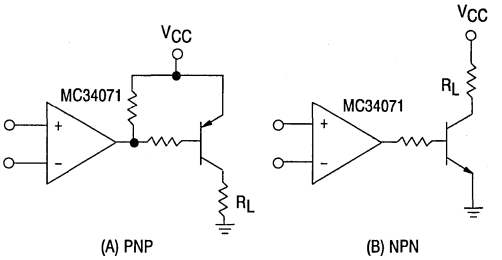


Figure 47. AC/DC Ground Current Monitor

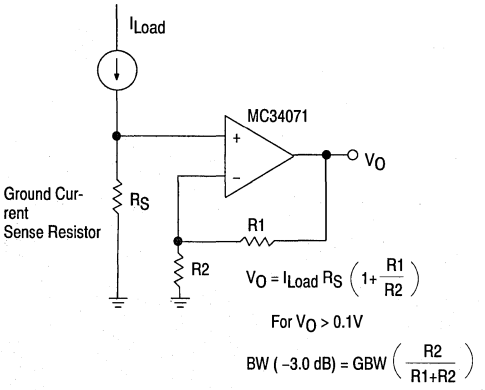


Figure 48. Photovoltaic Cell Amplifier

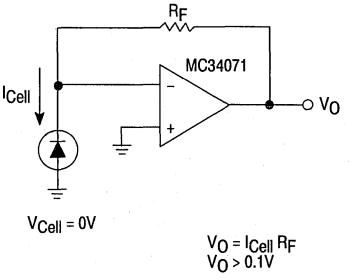
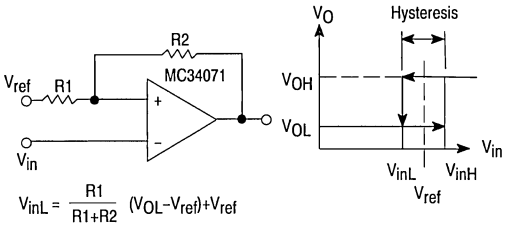


Figure 49. Low Input Voltage Comparator with Hysteresis

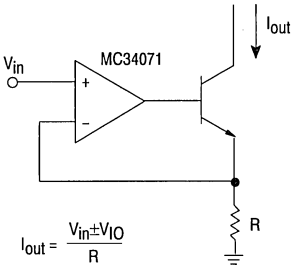


$$V_{inL} = \frac{R1}{R1+R2}(V_{OL}-V_{ref})+V_{ref}$$

$$V_{inH} = \frac{R1}{R1+R2}(V_{OH}-V_{ref})+V_{ref}$$

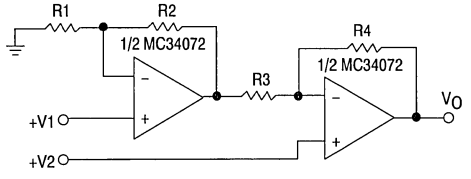
$$V_H = \frac{R1}{R1+R}(V_{OH}-V_{OL})$$

Figure 50. High Compliance Voltage to Sink Current Converter



$$I_{out} = \frac{V_{in} \pm V_{IO}}{R}$$

Figure 51. High Imput Impedance Differential Amplifier



$$\frac{R2}{R1} = \frac{R4}{R3} \text{ (Critical to CMRR)}$$

$$V_O = 1\left(+\frac{R4}{R3}\right)\left(V2-V1\,\frac{R4}{R3}\right)$$

For (V2 ≥ V1), V > 0

Figure 52. Bridge Current Amplifier

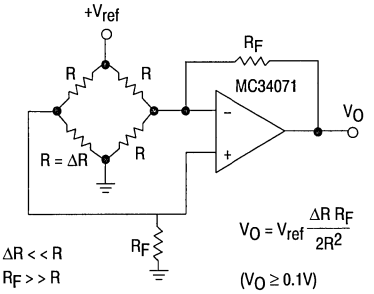


Figure 53. Low Voltage Peak Detector

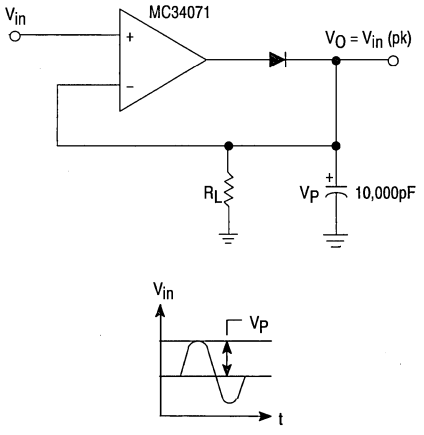
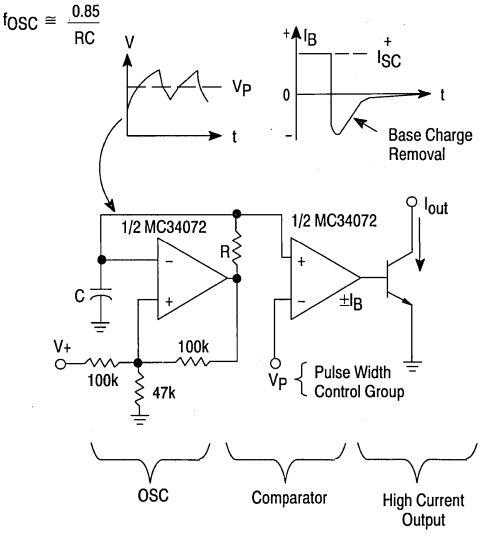


Figure 54. High Frequency Pulse Width Modulation

$$f_{OSC} \cong \frac{0.85}{RC}$$



GENERAL ADDITIONAL APPLICATIONS INFORMATION V_S = ±15.0 V

Figure 55. Second Order Low-Pass Active Filter

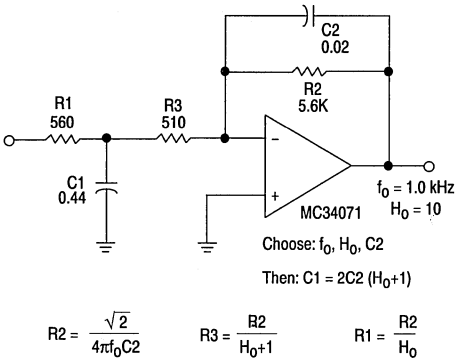


Figure 56. Second Order High-Pass Active Filter

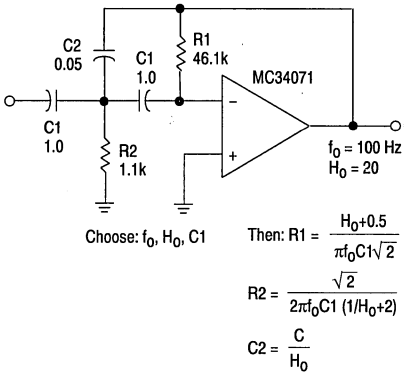


Figure 57. Fast Settling Inverter

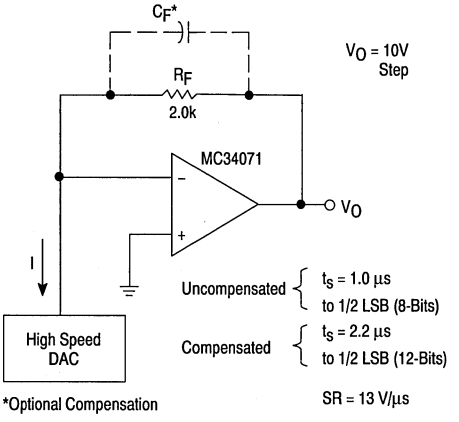


Figure 58. Basic Inverting Amplifier

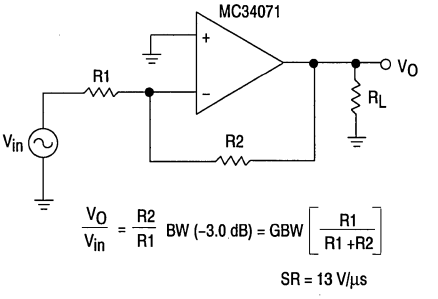


Figure 59. Basic Noninverting Amplifier

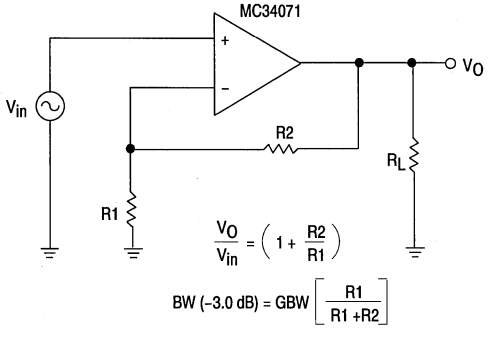


Figure 60. Unity Gain Buffer (A_V = +1.0)

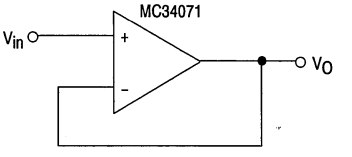


Figure 61. High Impedance Differential Amplifier

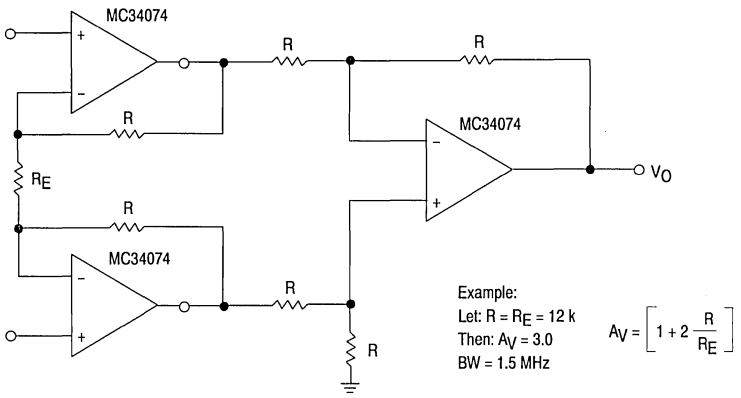
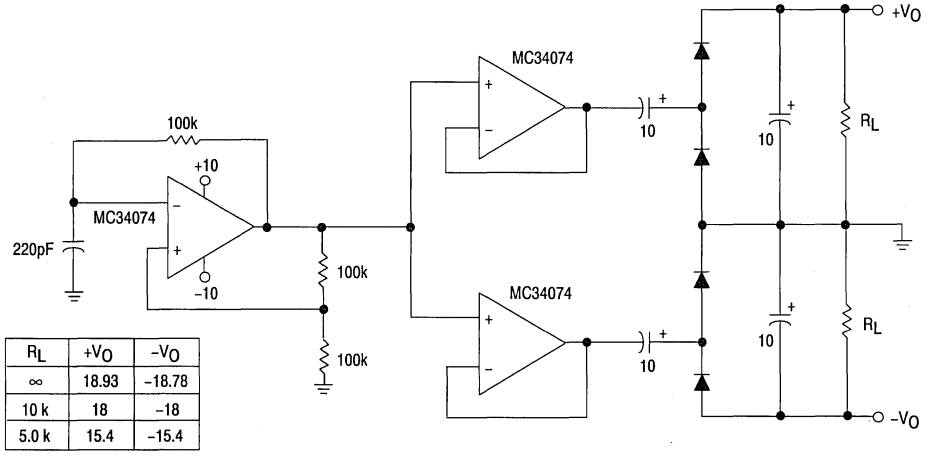


Figure 62. Dual Voltage Doubler



R_L	$+V_O$	$-V_O$
∞	18.93	-18.78
10 k	18	-18
5.0 k	15.4	-15.4

MC34080/MC35080 thru MC34085/MC35085

HIGH PERFORMANCE JFET INPUT OPERATIONAL AMPLIFIERS

High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifiers

These devices are a new generation of high speed JFET input monolithic operational amplifiers. Innovative design concepts along with JFET technology provide wide gain bandwidth product and high slew rate. Well matched JFET input devices and advanced trim techniques ensure low input offset errors and bias currents. The all NPN output stage features large output voltage swing, no deadband crossover distortion, high capacitive drive capability, excellent phase and gain margins, low open-loop output impedance, and symmetrical source/sink AC frequency response.

This series of devices are available in fully compensated or decompensated ($A_{VCL} \leq 2$) and are specified over commercial or Military temperature ranges. They are pin compatible with existing Industry standard operational amplifiers, and allow the designer to easily upgrade the performance of existing designs.

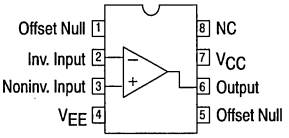
- Wide Gain Bandwidth: 8.0 MHz for Fully Compensated Devices
  16 MHz for Decompensated Devices
- High Slew Rate: 25 V/μs for Fully Compensated Devices
  50 V/μs for Decompensated Devices
- High Input Impedance: $10^{12}\Omega$
- Input Offset Voltage: 0.5 mV Maximum (Single Amplifier)
- Large Output Voltage Swing: −14.7 V to +14 V for
  $V_{CC}/V_{EE} = \pm 15$ V
- Low Open-Loop Output Impedance: 30 Ω @ 1.0 MHz
- Low THD Distortion: 0.01%
- Excellent Phase/Gain Margins: 55°/7.6 dB for Fully Compensated Devices

P SUFFIX
PLASTIC PACKAGE
CASE 626

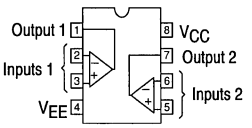
U SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



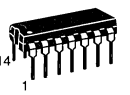
(Single, Top View)



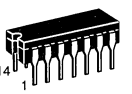
(Dual, Top View)

ORDERING INFORMATION

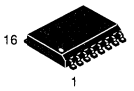
Op Amp Function	Fully Compensated	$A_{VCL} \geq 2$ Compensated	Temperature Range	Package
Single	MC35081BU	MC35080BU	− 55° to +125°C	Ceramic DIP
	MC34081BD	MC34080BD	0° to +70°C	SO-8
	MC34081BP	MC34080BP		Plastic DIP
Dual	MC34082P	MC34083P		Plastic DIP
Quad	MC35084L	MC35085L	− 55° to +125°C	Ceramic DIP
	MC34084DW	MC34085DW	0° to +70°C	SO-16L
	MC34084P	MC34085P		Plastic DIP



P SUFFIX
PLASTIC PACKAGE
CASE 646

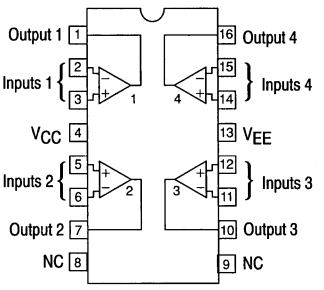


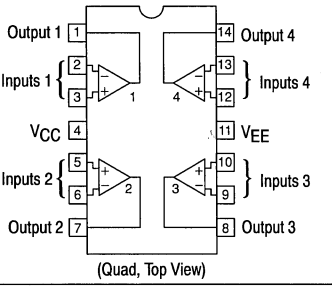
L SUFFIX
CERAMIC PACKAGE
CASE 632



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO-16L)

PIN CONNECTIONS





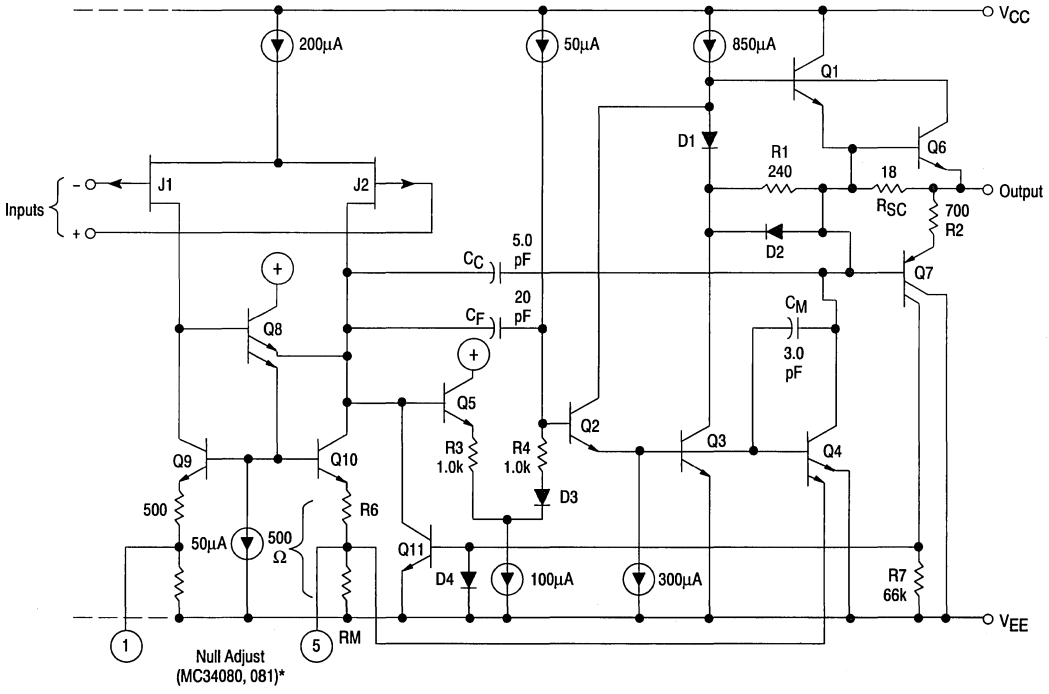
(Quad, Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+44	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Ambient Temperature Range MC35XXX MC34XXX	T_A	 – 55 to +125 0 to +70	°C
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 +165 +125	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 – 65 to +165 – 55 to +125	°C

NOTES: 1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

Equivalent Circuit Schematic
(Each Amplifier)



*Pins 1 & 5 (MC34080,081) should *not* be directly grounded or connected to V_{CC}.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = – 15 V, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (Note 4)	V_{IO}				mV
Single					
T_A = +25°C		—	0.5	2.0	
T_A = 0° to +70°C (MC34080B, MC34081B)		—	—	4.0	
T_A = – 55° to +125°C (MC35080B, MC35081B)		—	—	4.0	
Dual					
T_A = +25°C		—	1.0	3.0	
T_A = 0° to +70°C (MC34082, MC34083)		—	—	5.0	
Quad					
T_A = +25°C		—	6.0	12	
T_A = 0° to +70°C (MC34084, MC34085)		—	—	14	
T_A = – 55° to +125°C (MC35084, MC35085)		—	—	15	
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	10	—	μV/°C
Input Bias Current (V_{CM} = 0 Note 5)	I_{IB}				nA
T_A = +25°C		—	0.06	0.2	
T_A = 0° to +70°C		—	—	4.0	
T_A = – 55° to +125°C		—	—	50	
Input Offset Current (V_{CM} = 0 Note 5)	I_{IO}				nA
T_A = +25°C		—	0.02	0.1	
T_A = 0° to +70°C		—	—	2.0	
T_A = – 55° to +125°C		—	—	25	
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k)	A_{VOL}				V/mV
T_A = +25°C		25	80	—	
T_A = T_{low} to T_{high}		15	—	—	
Output Voltage Swing	V_{OH}				V
R_L = 2.0 k, T_A = +25°C		13.2	13.7	—	
R_L = 10 k, T_A = +25°C		13.4	13.9	—	
R_L = 10 k, T_A = T_{low} to T_{high}		13.4	—	—	
R_L = 2.0 k, T_A = +25°C	V_{OL}	—	–14.1	–13.5	
R_L = 10 k, T_A = +25°C		—	–14.7	–14.1	
R_L = 10 k, T_A = T_{low} to T_{high}		—	—	–14.0	
Output Short Circuit Current (T_A = +25°C)	I_{SC}				mA
Input Overdrive = 1.0 V, Output to Ground					
Source		20	31	—	
Sink		20	28	—	
Input Common Mode Voltage Range	V_{ICR}	(V_{EE} +4.0) to (V_{CC} – 2.0)			V
T_A = +25°C					
Common Mode Rejection Ratio (R_S ≤ 10 k, T_A = +25°C)	CMRR	70	90	—	dB
Power Supply Rejection Ratio (R_S = 100 Ω, T_A = 25°C)	PSRR	70	86	—	dB
Power Supply Current	I_D				mA
Single					
T_A = +25°C		—	2.5	3.4	
T_A = T_{low} to T_{high}		—	—	4.2	
Dual					
T_A = +25°C		—	4.9	6.0	
T_A = T_{low} to T_{high}		—	—	7.5	
Quad					
T_A = +25°C		—	9.7	11	
T_A = T_{low} to T_{high}		—	—	13	

NOTES: (continued)

3. T_{low} = – 55°C for MC35080B, MC35081B, MC35084, MC35085; T_{low} = 0°C for MC34080B, MC34081B, MC34084, MC34085; T_{high} = +125°C for MC35080B, MC35081B, MC35084, MC35085; T_{high} = +70°C for MC34080B, MC34081B, MC34084, MC34085
4. See application information for typical changes in input offset voltage due to solderability and temperature cycling.
5. Limits at T_A = +25°C are guaranteed by high temperature (T_{high}) testing.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = – 15 V, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF) Compensated A_V = +1.0 A_V = –1.0 Decompensated A_V = +2.0 A_V = –1.0	SR	 20 — 40 —	 25 30 50 50	 — — — —	V/μs
Settling Time (10 V Step, A_V = –1.0) To 0.10% (±1/2 LSB of 9-Bits) To 0.01% (±1/2 LSB of 12-Bits)	t_s	 — —	 0.72 1.6	 — —	μs
Gain Bandwidth Product (f = 200 kHz) Compensated Decompensated	GBW	 6.0 12	 8.0 16	 — —	MHz
Power Bandwidth (R_L = 2.0 k, V_O = 20 V_{p-p}, THD = 5.0%) Compensated A_V = +1.0 Decompensated A_V = – 1.0	BWp	 — —	 400 800	 — —	kHz
Phase margin (Compensated) R_L = 2.0 k R_L = 2.0 k, C_L = 100 pF	ϕ_m	 — —	 55 39	 — —	Degrees
Gain Margin (Compensated) R_L = 2.0 k R_L = 2.0 k, C_L = 100 pF	A_m	 — —	 7.6 4.5	 — —	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	30	—	nV/√Hz
Equivalent Input Noise Current (f = 1.0 kHz)	I_n	—	0.01	—	pA/√Hz
Input Capacitance	C_i	—	5.0	—	pF
Input Resistance	r_i	—	10^{12}	—	Ω
Total Harmonic Distortion A_V = +10, R_L = 2.0 k, 2.0 ≤ V_O ≤ 20 V_{p-p}, f = 10 kHz	THD	—	0.05	—	%
Channel Separation (f = 10 kHz)	—	—	120	—	dB
Open-Loop Output Impedance (f = 1.0 MHz)	Z_o	—	35	—	Ω

Figure 1. Input Common Mode Voltage Range versus Temperature

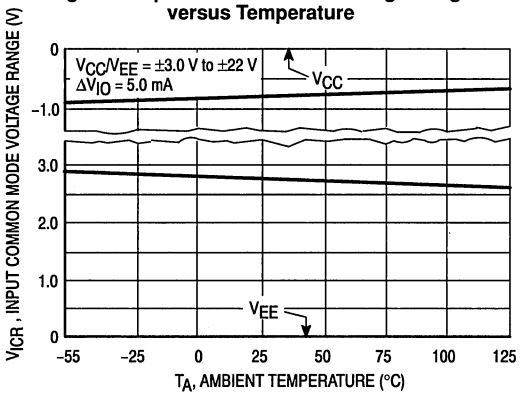


Figure 2. Input Bias Current versus Temperature

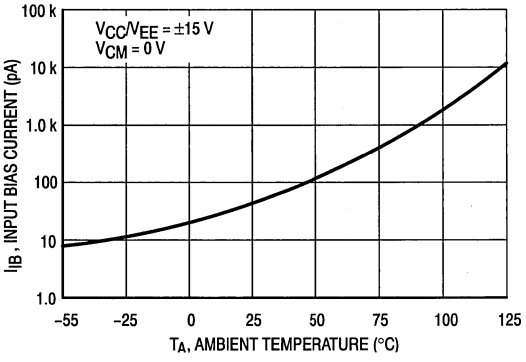


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Figure 3. Input Bias Current versus Input Common Mode Voltage

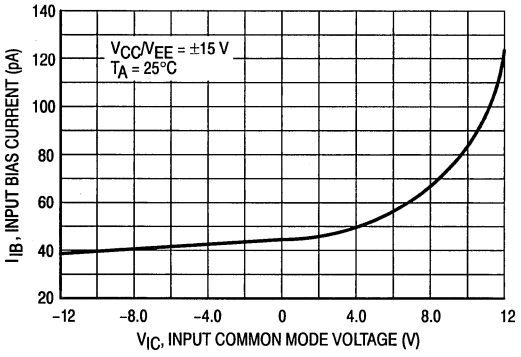


Figure 4. Output Voltage Swing versus Supply Voltage

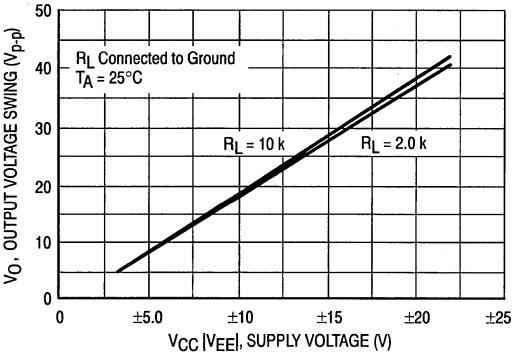


Figure 5. Output Saturation versus Load Current

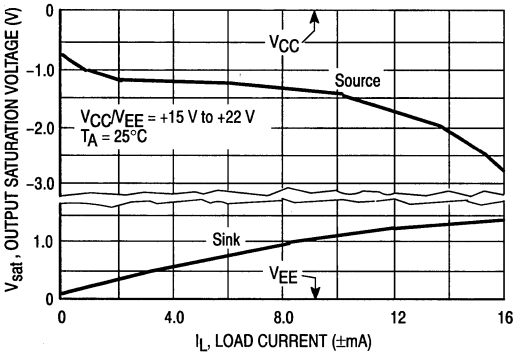


Figure 6. Output Saturation vesus Load Resistance to Ground

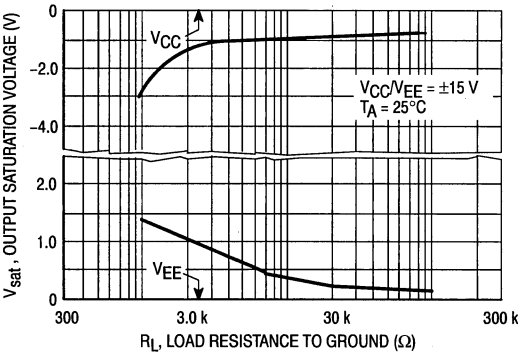


Figure 7. Output Saturation versus Load Resistance to V_{CC}

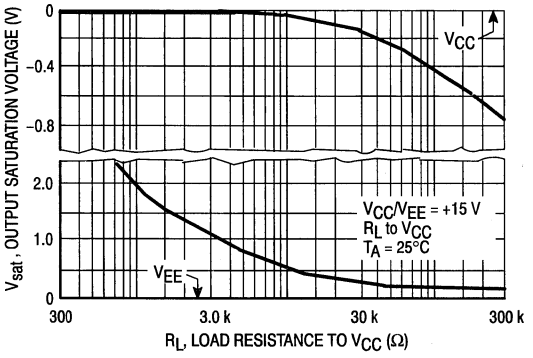


Figure 8. Output Short Circuit Current versus Temperature

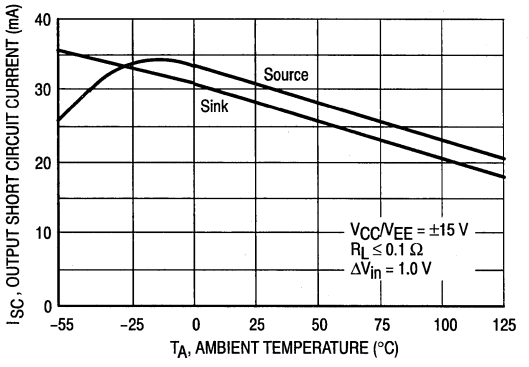


Figure 9. Output Impedance versus Frequency

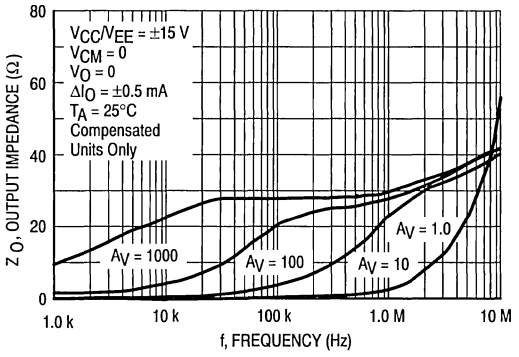


Figure 10. Output Impedance versus Frequency

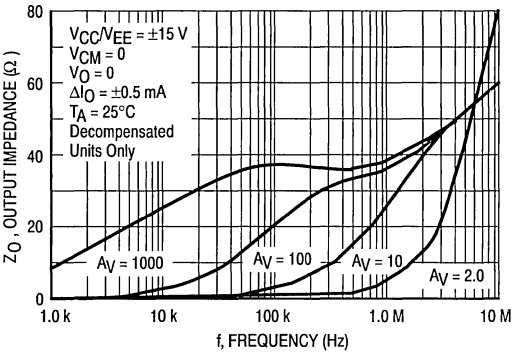


Figure 11. Output Voltage Swing versus Frequency

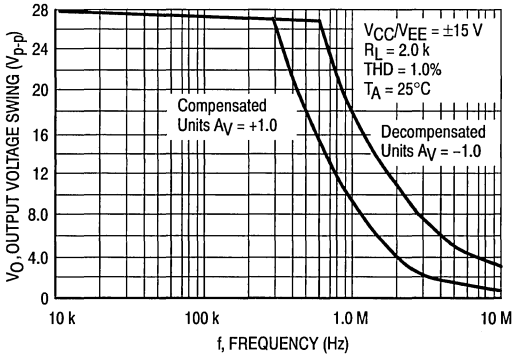


Figure 12. Output Distortion versus Frequency

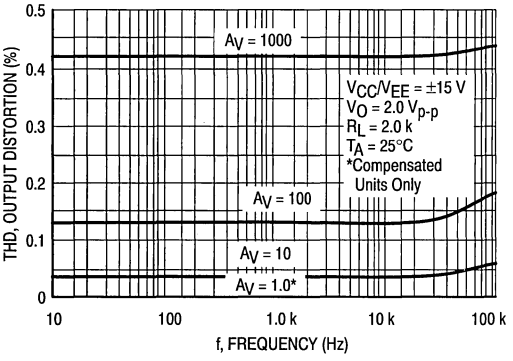
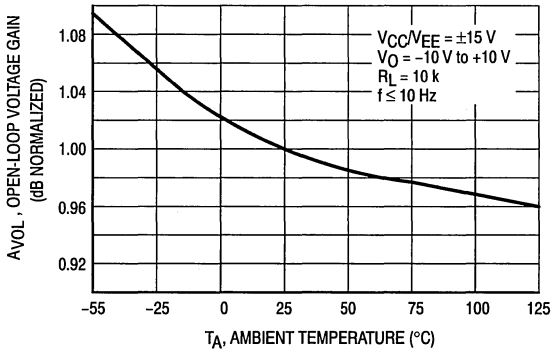


Figure 13. Open-Loop Voltage Gain versus Temperature



2

Figure 14. Open-Loop Voltage Gain and Phase versus Frequency

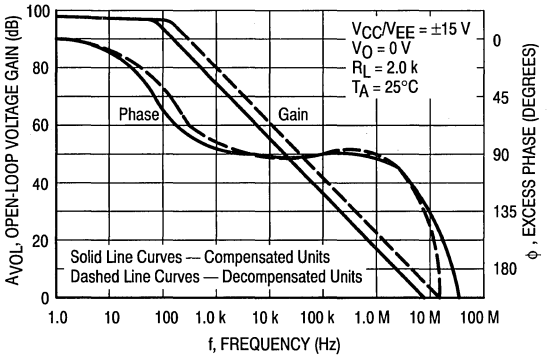


Figure 15. Open-Loop Voltage Gain and Phase versus Frequency

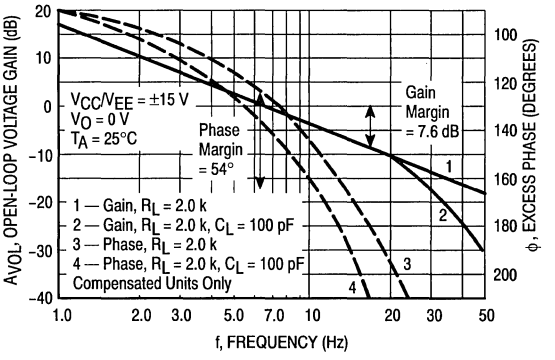


Figure 16. Open-Loop Voltage Gain and Phase versus Frequency

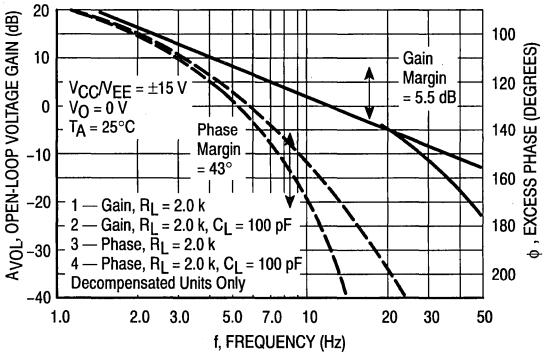


Figure 17. Normalized Gain Bandwidth Product versus Temperature

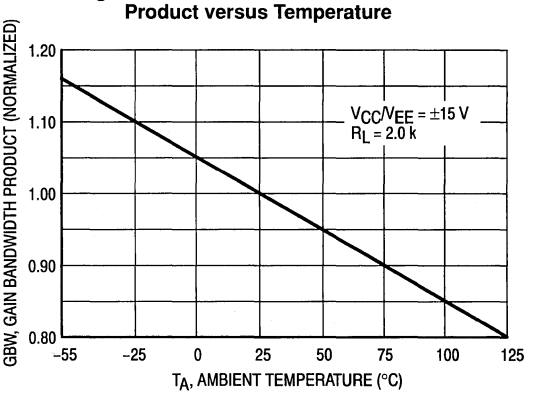


Figure 18. Percent Overshoot versus Load Capacitance

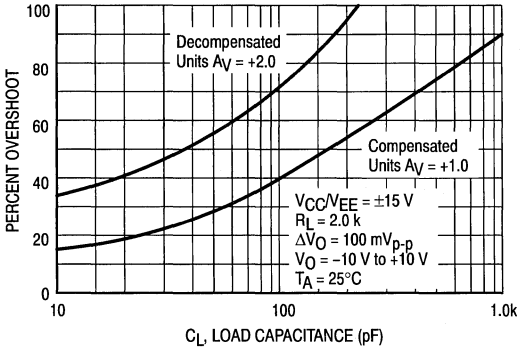


Figure 19. Phase Margin versus Load Capacitance

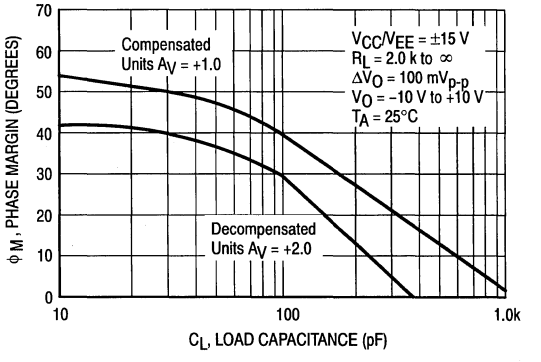


Figure 20. Gain Margin versus Load Capacitance

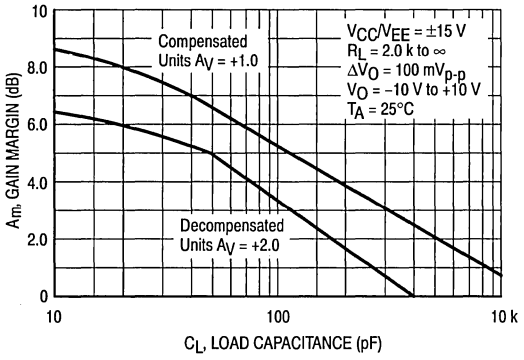


Figure 21. Phase Margin versus Temperature

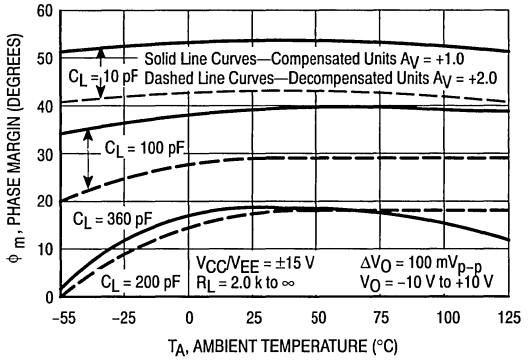


Figure 22. Gain Margin versus Temperature

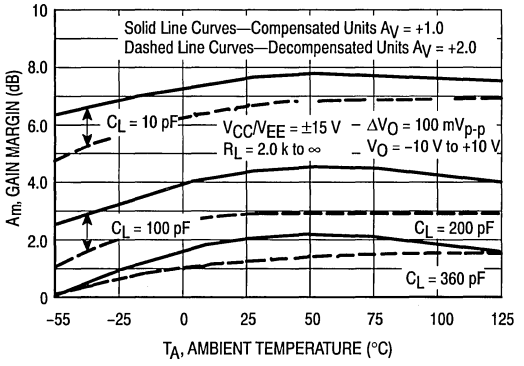
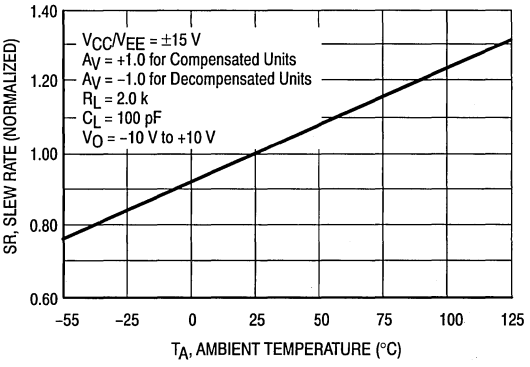


Figure 23. Normalized Slew Rate versus Temperature



2

MC34084 Transient Response
A_V = +1.0, R_L = 2.0 k, V_{CC}/V_{EE} = ±15 V, T_A = 25°C

Figure 24. Small-Signal

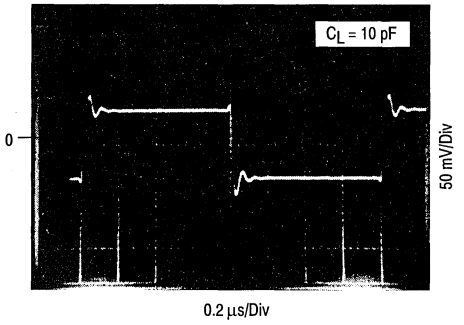
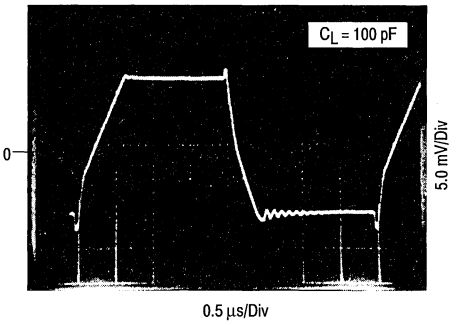


Figure 25. Large-Signal



MC34085 Transient Response
A_V = +2.0, R_L = 2.0 k, V_{CC}/V_{EE} = ±15 V, T_A = 25°C

Figure 26. Small-Signal

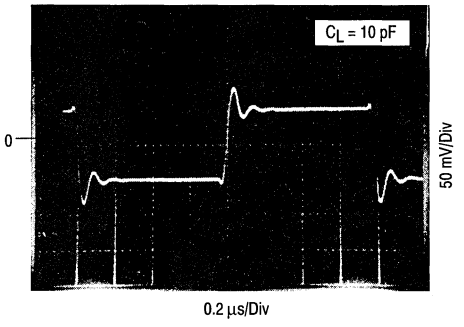


Figure 27. Large-Signal

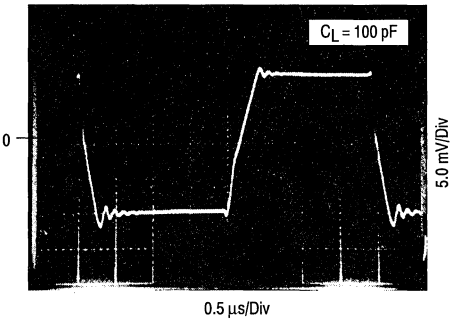


Figure 28. Common Mode Rejection Ratio versus Frequency

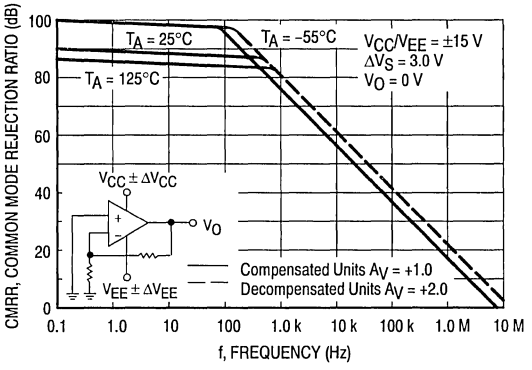


Figure 29. Power Supply Rejection Ratio versus Frequency

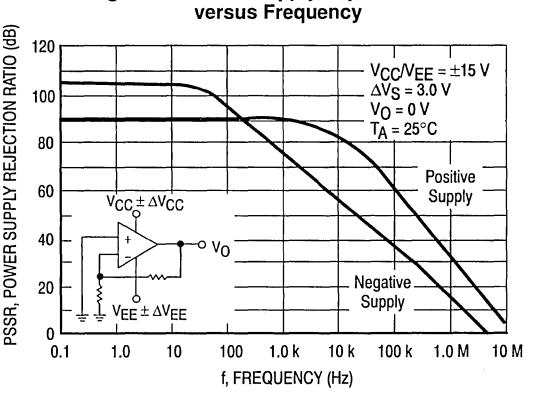


Figure 30. Power Supply Rejection Ratio versus Temperature

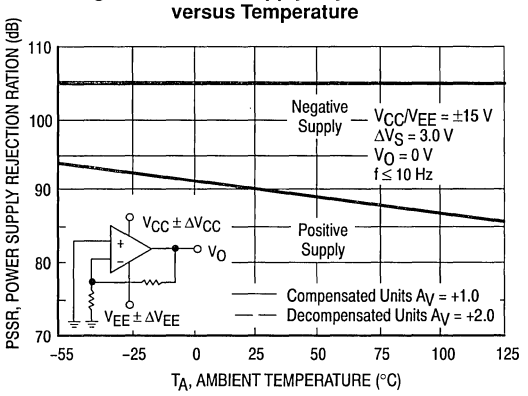


Figure 32. Normalized Supply Current versus Supply Voltage

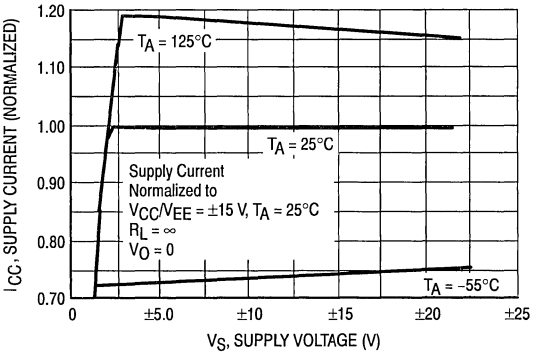


Figure 32. Channel Separation versus Frequency

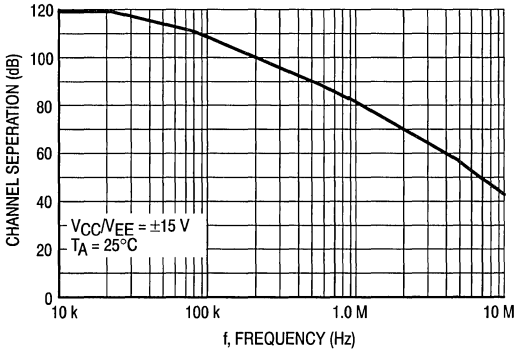
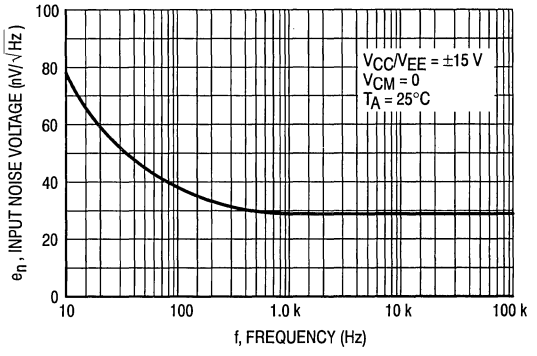


Figure 33. Spectral Noise Density



APPLICATIONS INFORMATION

The bandwidth and slew rate of the MC34080 series is nearly double that of currently available general purpose JFET op-amps. This improvement in AC performance is due to the P-channel JFET differential input stage driving a compensated miller integration amplifier in conjunction with an all NPN output stage.

The all NPN output stage offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. With a 10 k load resistance, the op amp can typically swing within 1.0 V of the positive rail (V_{CC}), and within 0.3 V of the negative rail (V_{EE}), providing a 28.7 p-p swing from ±15 V supplies. This large output swing becomes most noticeable at lower supply voltages. If the load resistance is referenced to V_{CC} instead of ground, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the NPN output transistor will pull the output very near V_{EE} during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull-up capability.

The all NPN transistor output stage is also inherently fast, contributing to the operation amplifier's high gain-bandwidth product and fast settling time. The associated high frequency output impedance is 50 Ω (typical) at 8.0 MHz. This allows driving capacitive loads from 0 pF to 300 pF without oscillations over the military temperature range, and over the full range of output swing. The 55°C phase margin and 7.6 dB gain margin as well as the general gain and phase characteristics are virtually independent of the sink/source output swing conditions. The high frequency characteristics of the MC34080 series is especially useful for active filter applications.

The common mode input range is from 2.0 V below the positive rail (V_{CC}) to 4.0 V above the negative rail (V_{EE}). The amplifier remains active if the inputs are biased at the positive rail. This may be useful for some applications in that single supply operation is possible with a single negative supply. However, a degradation of offset voltage and voltage gain may result.

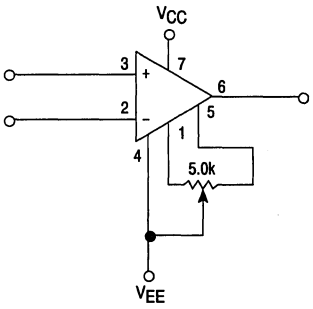
Phase reversal does not occur if either the inverting or noninverting input (or both) exceeds the positive common mode limit. If either input (or both) exceeds the negative common mode limit, the output will be in the high state. The input stage also allows a differential up to ±44 V, provided the maximum input voltage range is not exceeded. The supply voltage operating range is from ±5.0 V to ±22 V.

For optimum frequency performance and stability careful component placement and printed circuit board layout should be exercised. For example, long unshielded input or output leads may result in unwanted input-output coupling. In order to reduce the input capacitance, resistors connected to the input pins should be physically close to these pins. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pickup" at this node.

Supply decoupling with adequate capacitance close to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit large impedance changes over temperature.

Primarily due to the JFET inputs of the op amp, the input offset voltage may change due to temperature cycling and board soldering. After 20 temperature cycles (−55° to 165°C), the typical standard deviation for input offset voltage is 559 μV and 473 μV in the plastic and ceramic packages respectively. With respect to board soldering (260°C, 10 seconds) the typical standard deviation for input offset voltage is 525 μV and 227 μV in the plastic and ceramic package respectively. Socketed plastic or ceramic packaged devices should be used over a minimal temperature range for optimum input offset voltage performance.

Figure 34. Offset Nulling Circuit



MC34181,2,4
MC33181,2,4

2

LOW POWER JFET INPUT OPERATIONAL AMPLIFIERS

Low Power, High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifiers

Quality bipolar fabrication with innovative design concepts are employed for the MC33181/2/4, MC34181/2/4 series of monolithic operational amplifiers. This JFET input series of operational amplifiers operate at 210 μA per amplifier and offer 4.0 MHz of gain bandwidth product and 10 V/μs slew rate. Precision matching and an innovative trim technique of the single and dual versions provide low input offset voltages. With a JFET input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink AC frequency response.

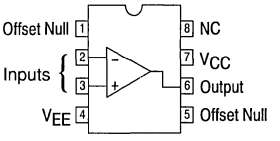
The MC33181/2/4, MC34181/2/4 series of devices are specified over the commercial, or industrial/vehicular temperature ranges. The complete series of single, dual and quad operational amplifiers are available in the plastic DIP as well as the SOIC surface mount packages.

- Low Supply Current: 210 μA (Per Amplifier)
- Wide Supply Operating Range: ±1.5 V to ±18 V
- Wide Bandwidth: 4.0 MHz
- High Slew Rate: 10 V/μs
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing: −14 V to +14 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 pF to 500 pF
- Low Total Harmonic Distortion: 0.04%
- Excellent Phase Margin: 67°
- Excellent Gain Margin: 6.7 dB
- Output Short Circuit Protection

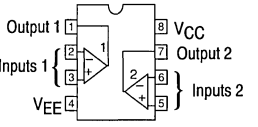
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

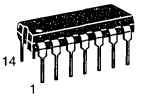
PIN CONNECTIONS



(Single, Top View)



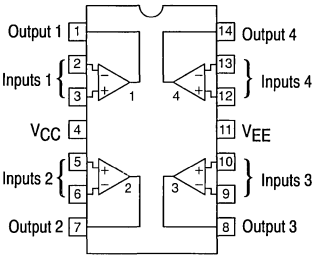
(Dual, Top View)



P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Quad, Top View)

ORDERING INFORMATION

Op Amp Function	Device	Test Temperature Range	Package
Single	MC34181P MC34181D	0° to +70°C	Plastic DIP SO-8
	MC33181P MC33181D	−40° to +85°C	Plastic DIP SO-8
Dual	MC34182P MC34182D	0° to +70°C	Plastic DIP SO-8
	MC33182P MC33182D	−40° to +85°C	Plastic DIP SO-8
Quad	MC34184P MC34184D	0° to +70°C	Plastic DIP SO-14
	MC33184P MC33184D	−40° to +85°C	Plastic DIP SO-14

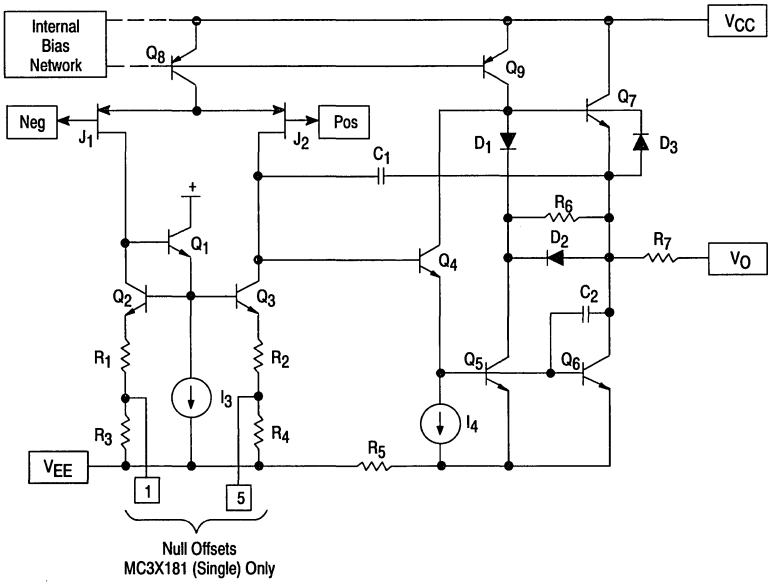
2

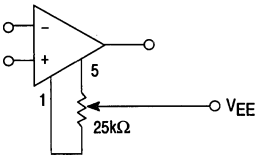
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	Note 1	V
Input Voltage Range	V_{IR}	Note 1	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–60 to +150	°C

NOTES: 1. Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

Equivalent Circuit Schematic
(Each Amplifier)





MC3X181 Input Offset
Voltage Null Circuit

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_O = 0 V)	V_{IO}				mV
Single					
T_A = +25°C		—	0.5	2.0	
T_A = 0° to +70°C (MC34181)		—	—	3.0	
T_A = −40° to +85°C (MC33181)		—	—	3.5	
Dual					
T_A = +25°C		—	1.0	3.0	
T_A = 0° to +70°C (MC34182)		—	—	4.0	
T_A = −40° to +85°C (MC33182)		—	—	4.5	
Quad					
T_A = +25°C		—	4.0	10	
T_A = 0° to +70°C (MC34184)		—	—	11	
T_A = −40° to +85°C (MC33184)		—	—	11.5	
Average Temperature Coefficient of V_{IO} (R_S = 50 Ω, V_O = 0V)	$\Delta V_{IO}/\Delta T$	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0V)	I_{IO}				nA
T_A = +25°C		—	0.001	0.05	
T_A = 0° to +70°C		—	—	1.0	
T_A = −40° to +85°C		—	—	2.0	
Input Bias Current (V_{CM} = 0 V, V_O = 0V)	I_{IB}				nA
T_A = +25°C		—	0.003	0.1	
T_A = 0° to +70°C		—	—	2.0	
T_A = −40° to +85°C		—	—	4.0	
Input Common Mode Voltage Range	V_{ICR}	(V_{EE} +4.0 V) to (V_{CC} −2.0 V)			V
Large Signal Voltage Gain (R_L = 10 kΩ, V_O = ±10 V)	A_{VOL}				V/mV
T_A = +25°C		25	60	—	
T_A = T_{low} to T_{high}		15	—	—	
Output Voltage Swing (V_{ID} = 1.0 V, R_L = 10 kΩ)	V_{O+}	+13.5	+14	—	V
T_A = +25°C	V_{O-}	—	−14	−13.5	
Common Mode Rejection (R_S = 50 Ω, V_{CM} = V_{ICR}, V_O = 0 V)	CMR	70	86	—	dB
Power Supply Rejection (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	PSR	70	84	—	dB
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground)	I_{SC}				mA
Source		3.0	8.0	—	
Sink		8.0	11	—	
Power Supply Current (No Load, V_O = 0 V)	I_D				μA
Single					
T_A = +25°C		—	210	250	
T_A = T_{low} to T_{high}		—	—	250	
Dual					
T_A = +25°C		—	420	500	
T_A = T_{low} to T_{high}		—	—	500	
Quad					
T_A = +25°C		—	840	1000	
T_A = T_{low} to T_{high}		—	—	1000	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 10 kΩ, C_L = 100 pF) A_V = +1.0 A_V = −1.0	SR	 7.0 —	 10 10	 — —	V/μs
Settling Time (A_V = −1.0, R_L = 10 kΩ, V_O = 0 V to +10 V Step) To Within 0.10% To Within 0.01%	t_s	 — —	 1.1 1.5	 — —	μs
Gain Bandwidth Product (f = 100 kHz)	GBW	3.0	4.0	—	MHz
Power Bandwidth (A_V = +1.0, R_L = 10 kΩ, V_O = 20 V_{p-p}, THD = 5.0%)	BW_p	—	120	—	kHz
Phase Margin (−10 V < V_O < +10 V) R_L = 10 kΩ R_L = 10 kΩ, C_L = 100 pF	ϕ_m	 — —	 67 34	 — —	Degrees
Gain Margin (−10 V < V_O < +10 V) R_L = 10 kΩ R_L = 10 kΩ, C_L = 100 pF	A_m	 — —	 6.7 3.4	 — —	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	38	—	nV/√Hz
Equivalent Input Noise Current f = 1.0 kHz	i_n	—	0.01	—	pA/√Hz
Differential Input Capacitance	C_i	—	3.0	—	pF
Differential Input Resistance	R_i	—	10^{12}	—	Ω
Total Harmonic Distortion A_V = 10, R_L = 10 kΩ, 2.0 V_{p-p} < V_O < 20 V_{p-p}, f = 1.0 kHz	THD	—	0.04	—	%
Channel Separation (R_L = 10 kΩ, −10 V < V_O < +10 V, 0 Hz < f < 10 kHz)	—	—	120	—	dB
Open-Loop Output Impedance (f = 1.0 MHz)	$\|Z_o\|$	—	200	—	Ω

Figure 1. Maximum Power Dissipation versus Temperature for Package Variations

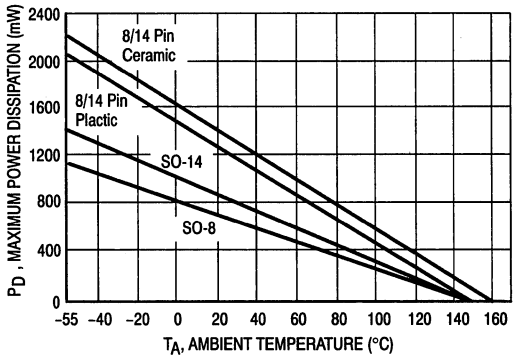


Figure 2. Input Common Mode Voltage Range versus Temperature

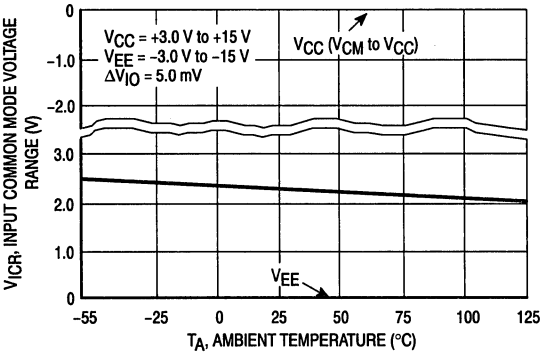


Figure 3. Input Bias Current versus Temperature

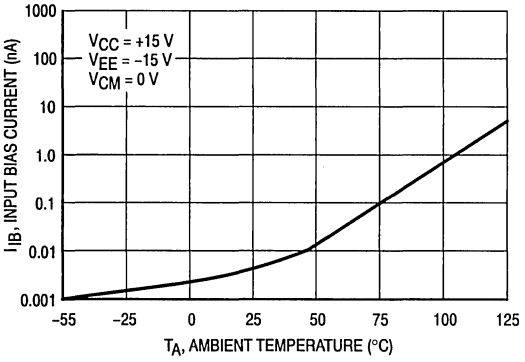


Figure 4. Input Bias Current versus Input Common Mode Voltage

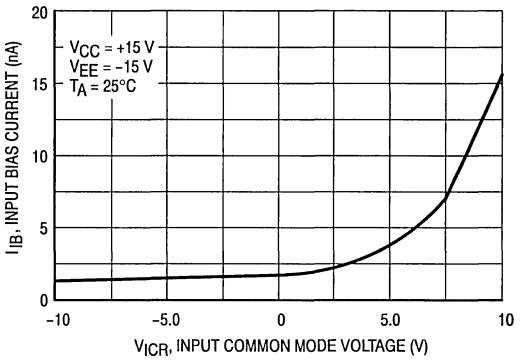


Figure 5. Output Voltage Swing versus Supply Voltage

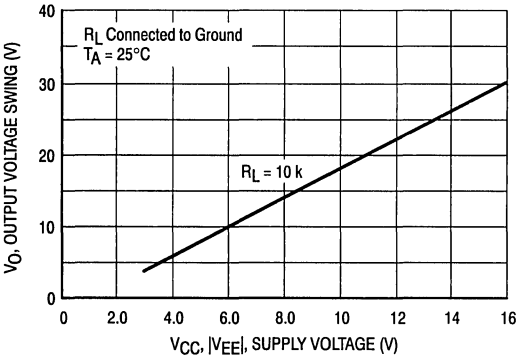


Figure 6. Output Saturation Voltage versus Load Current

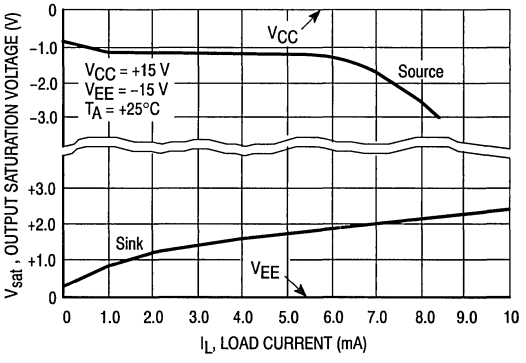


Figure 7. Output Saturation Voltage versus Load Resistance to Ground

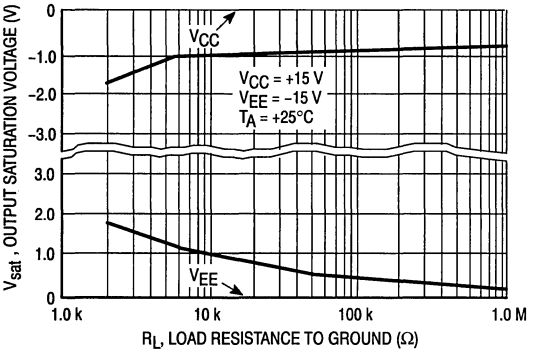


Figure 8. Output Saturation Voltage versus Load Resistance to V_{CC}

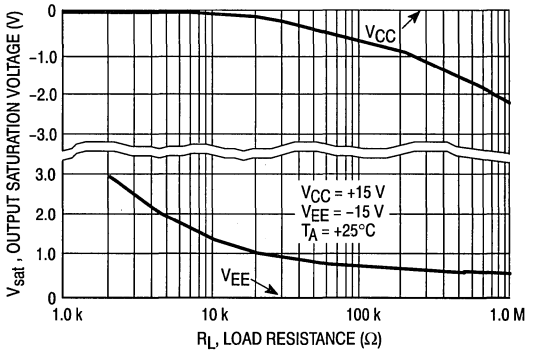


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Figure 9. Output Short Circuit Current versus Temperature

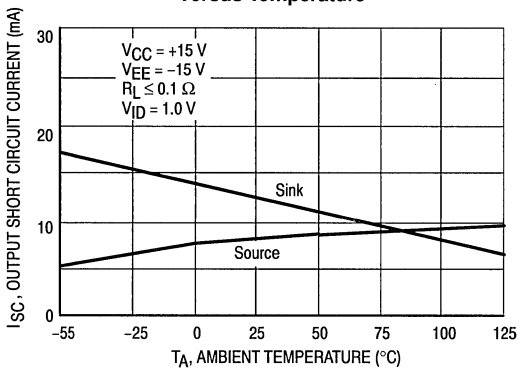


Figure 10. Output Impedance versus Frequency

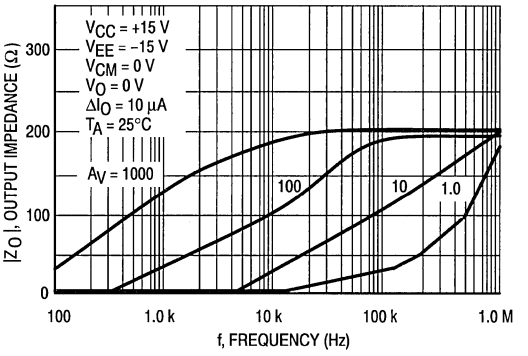


Figure 11. Output Voltage Swing versus Frequency

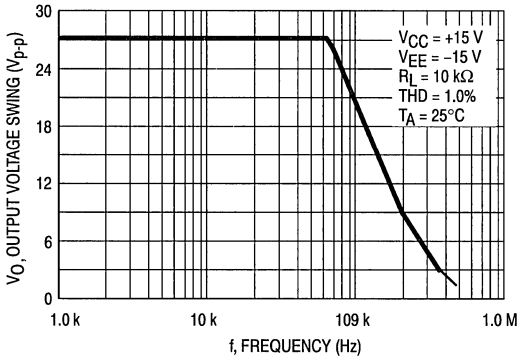


Figure 12. Output Distortion versus Frequency

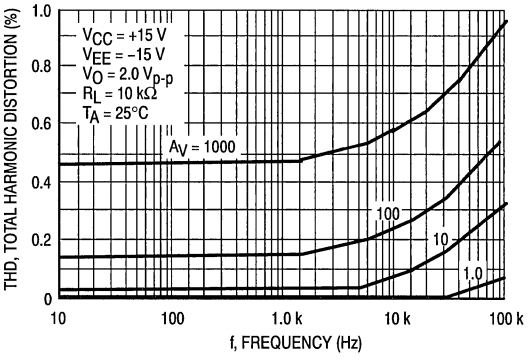


Figure 13. Open-Loop Voltage Gain versus Temperature

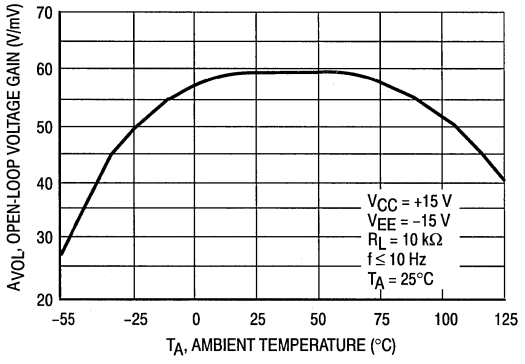


Figure 14. Open-Loop Voltage Gain and Phase versus Frequency

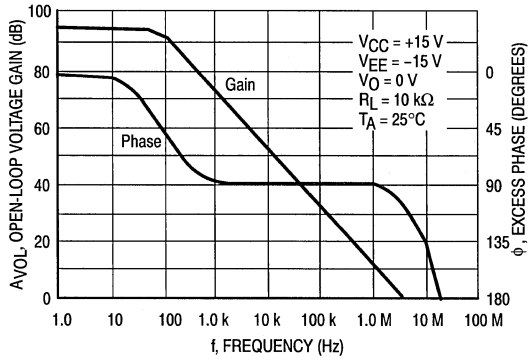


Figure 15. Normalized Gain Bandwidth Product versus Temperature

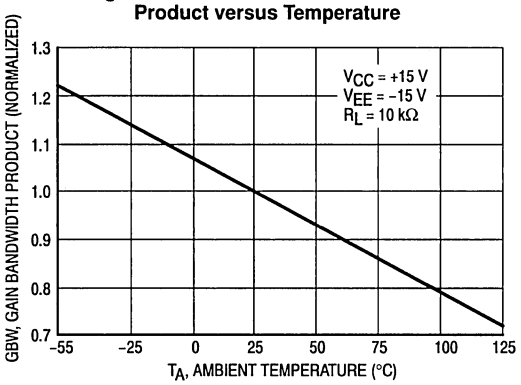


Figure 16. Output Voltage Overshoot versus Load Capacitance

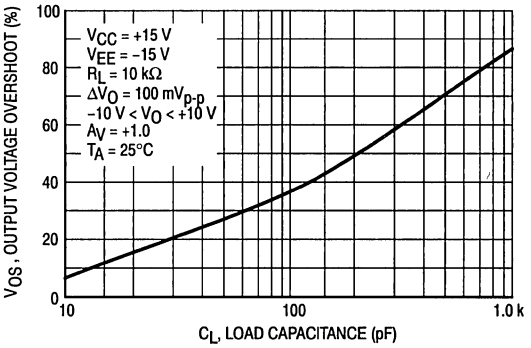


Figure 17. Phase Margin versus Load Capacitance

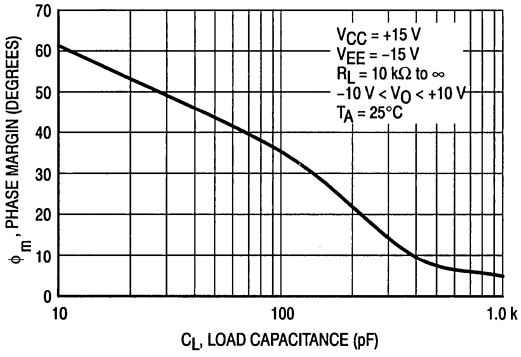


Figure 18. Gain Margin versus Load Capacitance

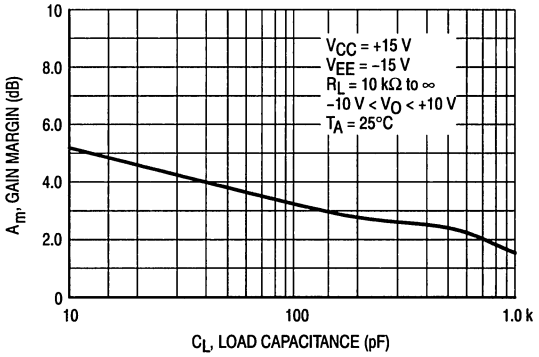


Figure 19. Phase Margin versus Temperature

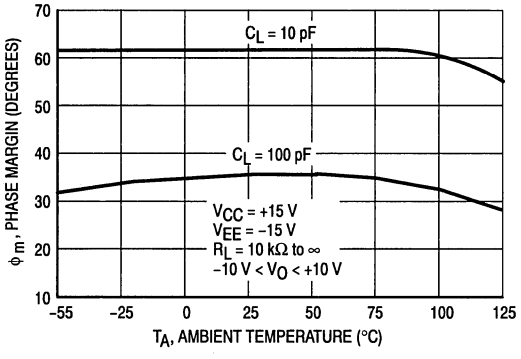
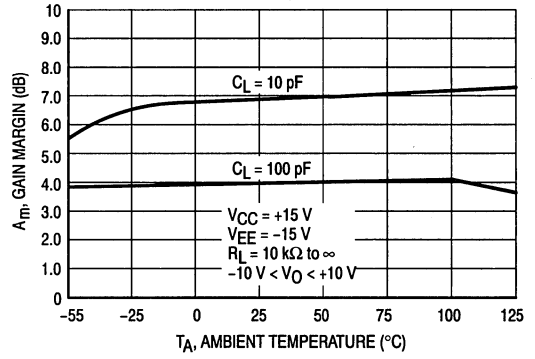


Figure 20. Gain Margin versus Temperature



2

Figure 21. Normalized Slew Rate versus Temperature

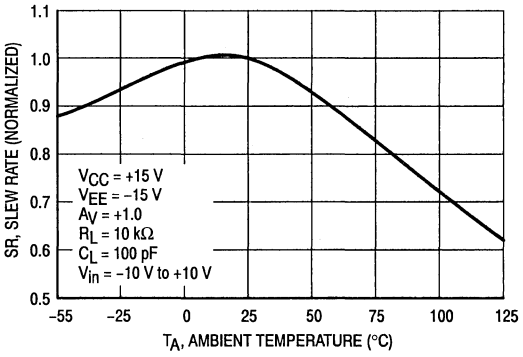


Figure 22. Common Mode Rejection versus Frequency

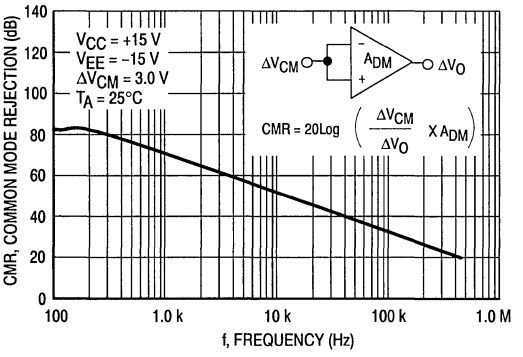


Figure 23. Input Noise Voltage versus Frequency

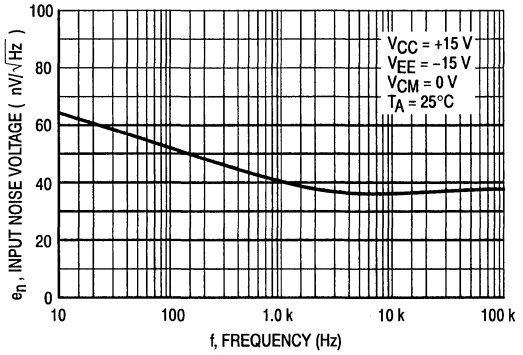


Figure 24. Power Supply Rejection versus Temperature

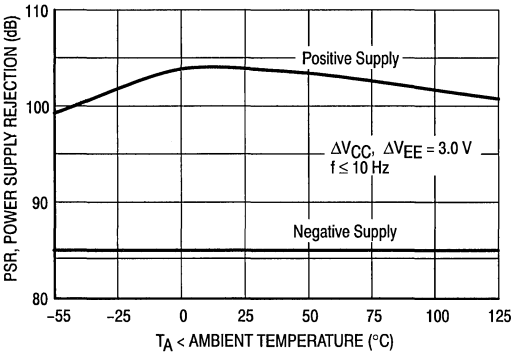


Figure 25. Power Supply Rejection versus Frequency

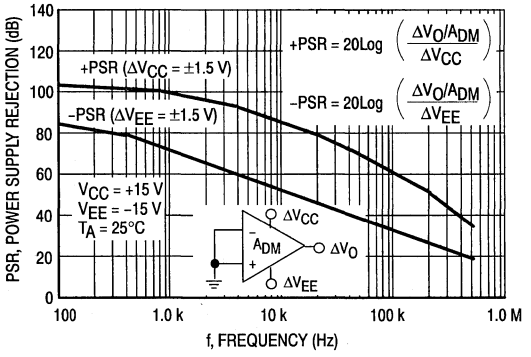


Figure 26. Normalized Supply Current versus Supply Voltage

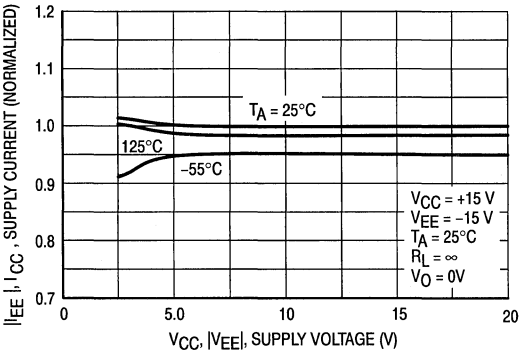


Figure 27. Channel Separation versus Frequency

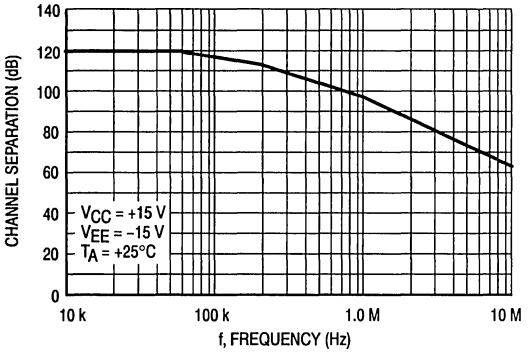


Figure 28. Transient Response

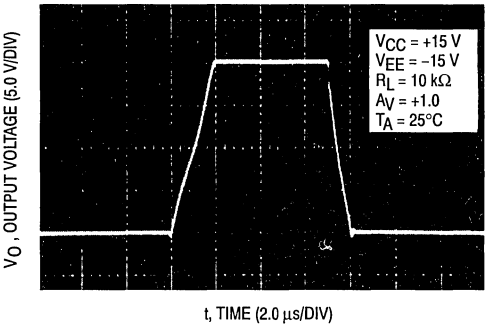
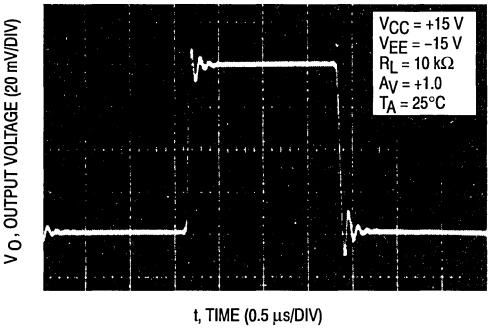


Figure 29. Small Signal Transient Reponse



TCA0372

2

Advance Information

Dual Power Operational Amplifier

The TCA0372 is a monolithic circuit intended for use as a power operational amplifier in a wide range of applications, including servo amplifiers and power supplies. No deadband crossover distortion provides better performance for driving coils.

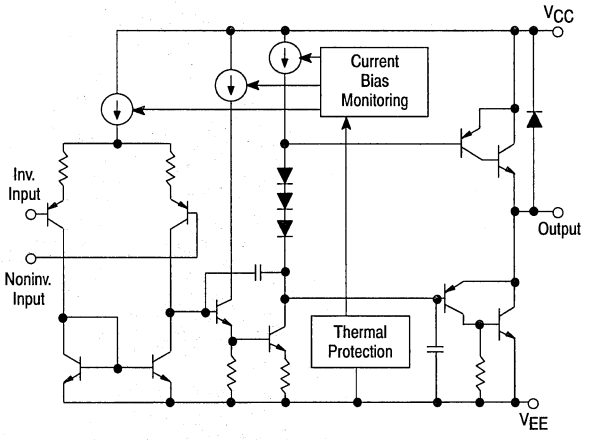
- Output Current to 1.0 A
- Slew Rate of 1.3 V/μs
- Wide Bandwidth of 1.1 MHz
- Internal Thermal Shutdown
- Single or Split Supply Operation
- Excellent Gain and Phase Margins
- Common Mode Input Includes Ground
- Zero Deadband Crossover Distortion

DW SUFFIX
PLASTIC PACKAGE
CASE 751G
SOP (12+2+2)L

DP2 SUFFIX
PLASTIC PACKAGE
CASE 648

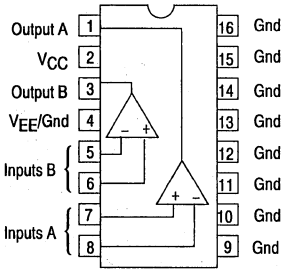
DP1 SUFFIX
PLASTIC PACKAGE
CASE 626

Simplified Block Diagram



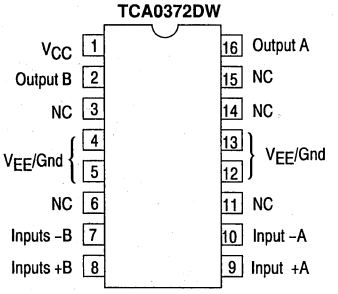
PIN CONNECTIONS

TCA0372DP2



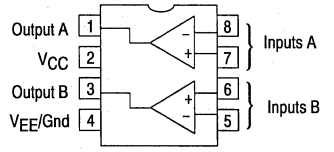
(Top View)

TCA0372DW



(Top View)

TCA0372DP1



(Top View)

ORDERING INFORMATION

Device	Operating Junction Temperature Range	Package
TCA0372DW	T_J = –40° to +150°C	SOP (12+2+2) L
TCA0372DP1		Plastic DIP
TCA0372DP2		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	40	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Operating Junction Temperature (Note 2)	T_J	+125	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
DC Output Current	I_O	1.0	A
Peak Output Current (Nonrepetitive)	$I_{(max)}$	1.5	A

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L connected to ground, T_J = −40° to +125°C.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} = 0) T_J = +25°C T_J, T_{low} to T_{high}	V_{IO}	 — —	 1.0 —	 15 20	mV
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	20	—	μV/°C
Input Bias Current (V_{CM} = 0)	I_{IB}	—	100	500	nA
Input Offset Current (V_{CM} = 0)	I_{IO}	—	10	50	nA
Large Signal Voltage Gain V_O = ±10 V, R_L = 2.0 k	A_{VOL}	30	100	—	V/mV
Output Voltage Swing (I_L = 100 mA) T_J = +25°C T_J = T_{low} to T_{high} T_J = +25°C T_J = T_{low} to T_{high}	V_{OH} V_{OL}	 14.0 13.9 — —	 14.2 — −14.2 —	 — — −14.0 −13.9	V
Output Voltage Swing (I_L = 1.0 A) V_{CC} = +24 V, V_{EE} = 0 V, T_J = +25°C V_{CC} = +24 V, V_{EE} = 0 V, T_J = T_{low} to T_{high} V_{CC} = +24 V, V_{EE} = 0 V, T_J = +25°C V_{CC} = +24 V, V_{EE} = 0 V, T_J = T_{low} to T_{high}	V_{OH} V_{OL}	 22.5 22.5 — —	 22.7 — 1.3 —	 — — 1.5 1.5	V
Input Common Mode Voltage Range T_J = +25°C T_J = T_{low} to T_{high}	V_{ICR}	V_{EE} to (V_{CC} −1.0) V_{EE} to (V_{CC} −1.3)			V
Common Mode Rejection Ratio (R_S = 10 k)	CMRR	70	90	—	dB
Power Supply Rejection Ratio (R_S = 100 Ω)	PSRR	70	90	—	dB
Power Supply Current T_J = +25°C T_J = T_{low} to T_{high}	I_D	 — —	 5.0 —	 10 14	mA

NOTES: 1. Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, R_L connected to ground, T_J = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 k, C_L = 100 pF) A_V = −1.0, T_J = T_{low} to T_{high}	SR	1.0	1.4	—	V/μs
Gain Bandwidth Product (f = 100 kHz, C_L = 100 pF, R_L = 2.0 k) T_J = 25°C T_J = T_{low} to T_{high}	GBW	 0.9 0.7	 1.4 —	 — —	MHz
Phase Margin T_J = T_{low} to T_{high} R_L = 2.0 k, C_L = 100 pF	ϕ_m	—	65	—	Degrees
Gain Margin R_L = 2.0 k, C_L = 100 pF	A_m	—	15	—	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 to 100 kHz	e_n	—	22	—	nV/$\sqrt{Hz}$
Total Harmonic Distortion A_V = −1.0, R_L = 50 Ω, V_O = 0.5 VRMS, f = 1.0 kHz	THD	—	0.02	—	%

NOTE: In case V_{EE} is disconnected before V_{CC}, a diode between V_{EE} and Ground is recommended to avoid damaging the device.

2

Figure 1. Supply Current versus Suppy Voltage with No Load

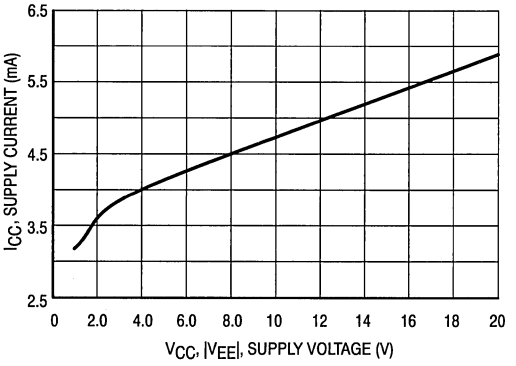


Figure 2. Output Saturation Voltage versus Load Current

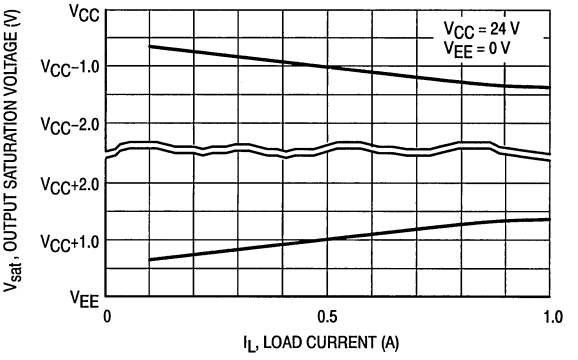


Figure 3. Voltage Gain and Phase versus Frequency

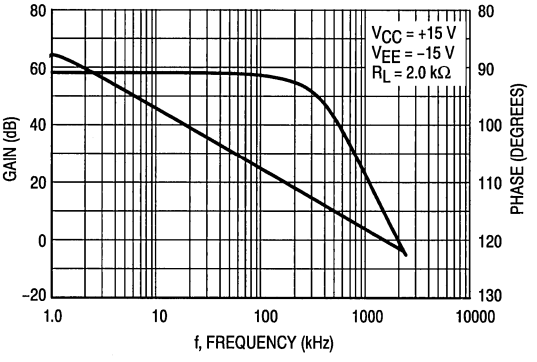


Figure 4. Phase Margin versus Output Load Capacitance

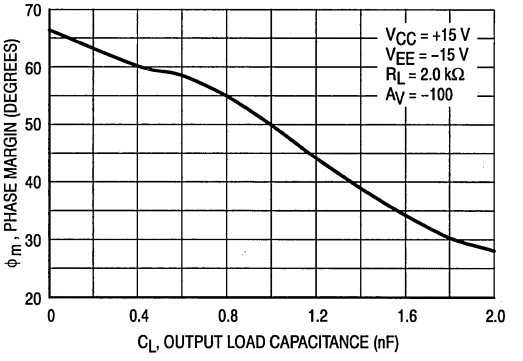


Figure 5. Small Signal Transient Response

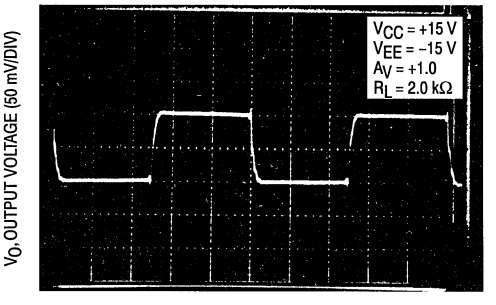


Figure 6. Large Signal Transient Response

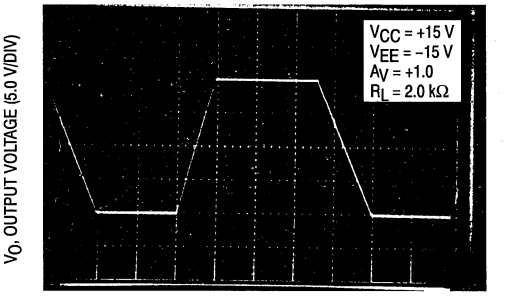


Figure 7. Sine Wave Reponse

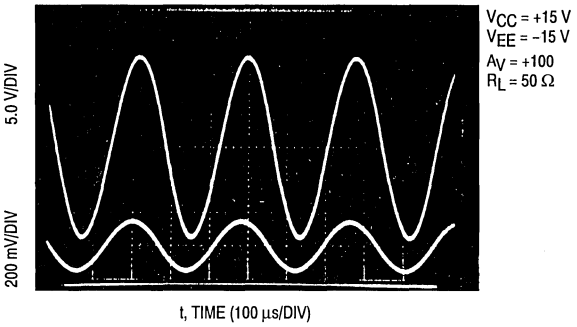


Figure 8. Bidirectional DC Motor Control with Microprocessor-Compatible Inputs

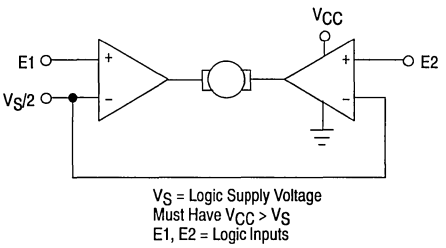
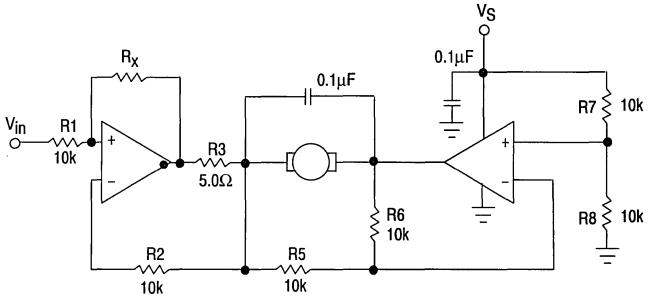


Figure 9. Bidirectional Speed Control of DC Motors

For circuit stability, ensure that $R_X > \frac{2R3 \bullet R1}{R_M}$ where, R_M = internal resistance of motor.

The voltage available at the terminals of the motor is: $V_M = 2\ (V_1 - \frac{V_S}{2}) + |R_o| \bullet I_M$

where, $|R_o| = \frac{2R3 \bullet R1}{R_X}$ and I_M is the motor current.



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equaiton:

$$P_{D(TA)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\ (typ)}$$

where, $P_{D(TA)}$ = power dissipation allowable at a given operating ambient temperature.

This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum operating junction temperature as listed in the maximum ratings section.

T_A = Maximum desired operating ambient temperature.

$R_{\theta JA(typ)}$ = Typical thermal resistance junction-to-ambient.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2

TL062
TL064

Low Power JFET Input Operational Amplifier

LOW POWER JFET INPUT OPERATIONAL AMPLIFIERS

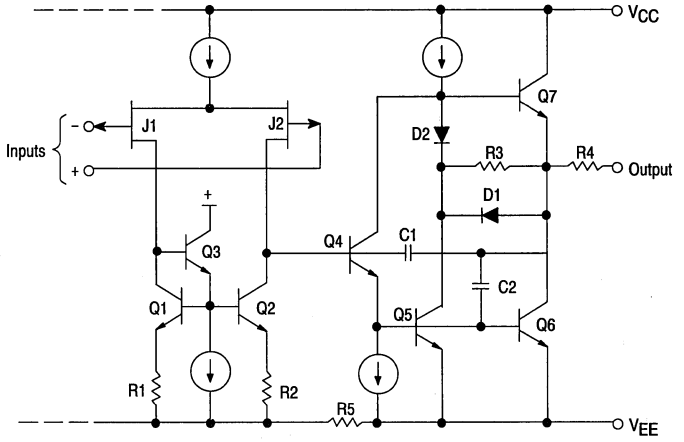
SILICON MONOLITHIC INTEGRATED CIRCUIT

These JFET input operational amplifiers are designed for low power applications. They feature high input impedance, low input bias current and low input offset current. Advanced design techniques allow for higher slew rates, gain bandwidth products and output swing.

These devices are specified over the commercial, vehicular and military temperature ranges. The commercial and vehicular devices are available in Plastic dual in-line and SOIC packages. The military devices are available in Ceramic dual in-line packages.

- Low Supply Current: 200 μA/Amplifier
- Low Input Bias Current: 5.0 pA
- High Gain Bandwidth: 2.0 MHz
- High Slew Rate: 6.0 V/μs
- High Input Impedance: 10^{12} Ω
- Large Output Voltage Swing: ±14 V
- Output Short Circuit Protection

Equivalent Circuit Schematic (Each Amplifier)



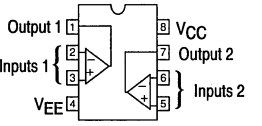
DUAL

P SUFFIX
PLASTIC PACKAGE
CASE 626

JG SUFFIX
CERAMIC PACKAGE
CASE 693

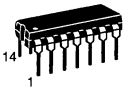
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS

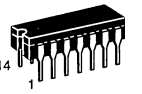


(Top View)

QUAD



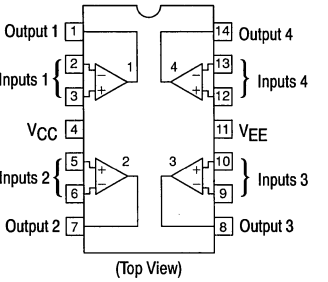
N SUFFIX
PLASTIC PACKAGE
CASE 646



J SUFFIX
CERAMIC PACKAGE
CASE 632

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Op Amp Function	Device	Tested Temperature Range	Package
Dual	TL062CD, ACD TL062CP, ACP	0° to +70°C	SO-8 Plastic DIP
	TLO62VD TL062VP	–40° to +85°C	SO-8 Plastic DIP
	TL062MJG	–55° to +125°C	Ceramic DIP
Quad	TL064CD, ACD TL064CN, ACN	0° to +70°C	SO-14 Plastic DIP
	TL064VD TLO64VN	–40° to +85°C	SO-14 Plastic DIP
	TL064MJ	–55° to +125°C	Ceramic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range (Note 1)	V_{IDR}	±30	V
Input Voltage Range (Notes 1 and 2)	V_{IR}	±15	V
Output Short Circuit Duration (Note 3)	t_{SC}	Indefinite	sec
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 +160 +150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 –65 to +160 –60 to +150	°C

NOTES: 1. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
2. The magnitude of the input voltage must never exceed the magnitude of the supply or 15 V, whichever is less.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See Figure 1.)

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 0° to +70°C, unless otherwise noted.)

Characteristics	Symbol	TL062AC TL064AC			TL062C TL064C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S = 50 Ω, V_O = 0V) T_A = 25°C T_A = 0° to +70°C	V_{IO}	 — —	 3.0 —	 6.0 7.5	 — —	 3.0 —	 15 20	mV
Average Temperature Coefficient for Offset Voltage (R_S = 50 Ω, V_O = 0 V)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	µV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V) T_A = 25°C T_A = 0° to +70°C	I_{IO}	 — —	 0.5 —	 100 2.0	 — —	 0.5 —	 200 2.0	 pA nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) T_A = 25°C T_A = 0° to +70°C	I_{IB}	 — —	 3.0 —	 200 2.0	 — —	 3.0 —	 200 10	 pA nA
Input Common Mode Voltage Range T_A = 25°C	V_{ICR}	— –11.5	+14.5 –12.0	+11.5 —	— –11	+14.5 –12.0	+11 —	V
Large Signal Voltage Gain (R_L = 10 kΩ, V_O = ±10 V) T_A = 25°C T_A = 0° to +70°C	A_{VOL}	 4.0 4.0	 58 —	 — —	 3.0 3.0	 58 —	 — —	V/mV
Output Voltage Swing (R_L = 10 kΩ, V_{ID} = 1.0 V) T_A = 25°C T_A = 0° to +70°C	 V_{O+} V_{O-} V_{O+} V_{O-}	 +10 — +10 —	 +14 –14 — —	 — –10 — –10	 +10 — +10 —	 +14 –14 — —	 — –10 — –10	V
Common Mode Rejection (R_S = 50 Ω, V_{CM} = V_{ICR} min, V_O = 0 V, T_A = 25°C)	CMR	80	84	—	70	84	—	dB
Power Supply Rejection (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0, T_A = 25°C)	PSR	80	86	—	70	86	—	dB
Power Supply Current (each amplifier) (No Load, V_O = 0 V, T_A = 25°C)	I_D	—	200	250	—	200	250	µA
Total Power Dissipation (each amplifier) (No Load, V_O = 0 V, T_A = 25°C)	P_D	—	6.0	7.5	—	6.0	7.5	mW

2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} (Note 4), unless otherwise noted.)

Characteristics	Symbol	TL062M,V			TL064M,V			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S = 50 Ω, V_O = 0V) T_A = 25°C T_A = T_{low} to T_{high}	V_{IO}	— —	3.0 —	6.0 9.0	— —	3.0 —	9.0 15	mV
Average Temperature Coefficient for Offset Voltage (R_S = 50 Ω, V_O = 0 V)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	µV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V) T_A = 25°C T_A = T_{low} to T_{high}	I_{IO}	— —	5.0 —	100 20	— —	5.0 —	100 20	pA nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) T_A = 25°C T_A = T_{low} to T_{high}	I_{IB}	— —	30 —	200 50	— —	30 —	200 50	pA nA
Input Common Mode Voltage Range (T_A = 25°C)	V_{ICR}	— −11.5	+14.5 −12.0	+11.5 —	— −11.5	+14.5 −12.0	+11.5 —	V
Large Signal Voltage Gain (R_L = 10 kΩ, V_O = ±10 V) T_A = 25°C T_A = T_{low} to T_{high}	A_{VOL}	4.0 4.0	58 —	— —	4.0 4.0	58 —	— —	V/mV
Output Voltage Swing (R_L = 10 kΩ, V_{ID} = 1.0 V) T_A = 25°C T_A = T_{low} to T_{high}	V_{O+} V_{O-} V_{O+} V_{O-}	+10 — +10 —	+14 −14 — —	— −10 — −10	+10 — +10 —	+14 −14 — —	— −10 — −10	V
Common Mode Rejection (R_S = 50 Ω, V_{CM} = V_{ICR} min, V_O = 0, T_A = 25°C)	CMR	80	84	—	80	84	—	dB
Power Supply Rejection (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0, T_A = 25°C)	PSR	80	86	—	80	86	—	dB
Power Supply Current (each amplifier) (No Load, V_O = 0 V, T_A = 25°C)	I_D	—	200	250	—	200	250	µA
Total Power Dissipation (each amplifier) (No Load, V_O = 0 V, T_A = 25°C)	P_D	—	6.0	7.5	—	6.0	7.5	mW

NOTE: 4. TL06XM T_{low} = −55°C T_{high} = +125°C
TL06XV T_{low} = −40°C T_{high} = +85°C

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 10 kΩ, C_L = 100 pF, A_V = +1.0)	SR	2.0	6.0	—	V/µs
Rise Time (V_{in} = 20 mV, R_L = 10 kΩ, C_L = 100 pF, A_V = +1.0)	t_r	—	0.1	—	µs
Overshoot (V_{in} = 20 mV, R_L = 10 kΩ, C_L = 100 pF, A_V = +1.0)	OS	—	10	—	%
Settling Time (V_{CC} = +15 V, V_{EE} = −15 V, A_V = −1.0, To within 10 mV R_L = 10 kΩ, V_O = 0 V to +10 V step) To within 1.0 mV	t_S	— —	1.6 2.2	— —	µs
Gain Bandwidth Product (f = 200 kHz)	GBW	—	2.0	—	MHz
Equivalent Input Noise (R_S = 100 Ω, f = 1.0 kHz)	e_n	—	47	—	nV/$\sqrt{Hz}$
Input Resistance	R_i	—	10^{12}	—	Ω
Channel Separation (f = 10 kHz)	CS	—	120	—	dB

TYPICAL PERFORMANCE CURVES

Figure 1. Maximum Power Dissipation versus Temperature for Package Variations

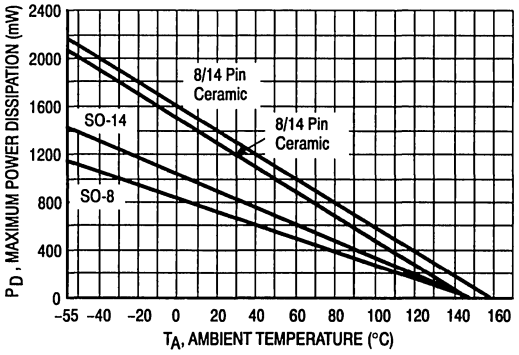


Figure 2. Output Voltage Swing versus Supply Voltage

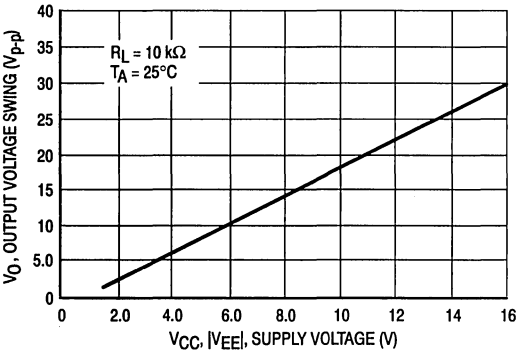


Figure 3. Output Voltage Swing versus Temperature

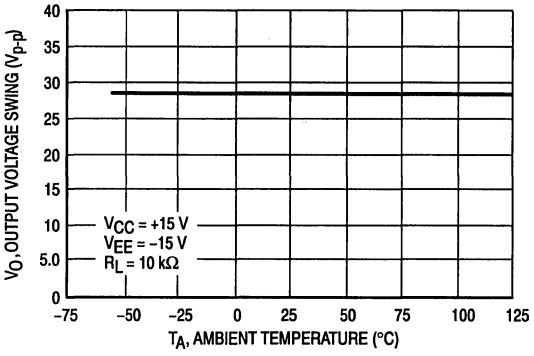


Figure 4. Output Voltage Swing versus Load Resistance

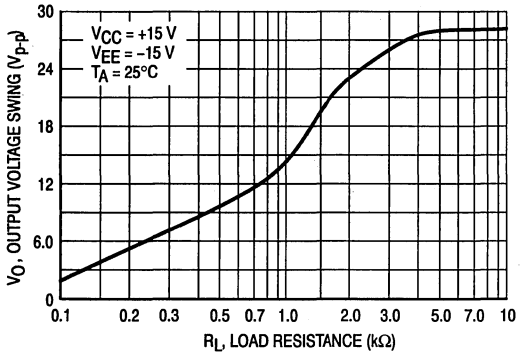


Figure 5. Output Voltage Swing versus Frequency

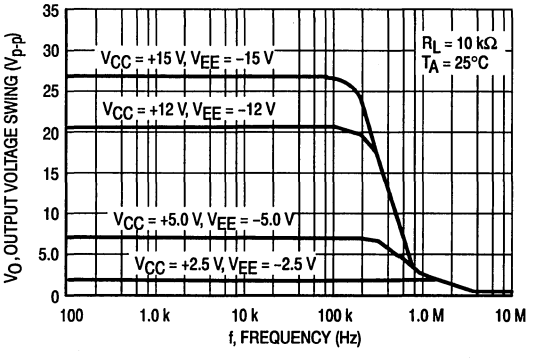


Figure 6. Large Signal Voltage Gain versus Temperature

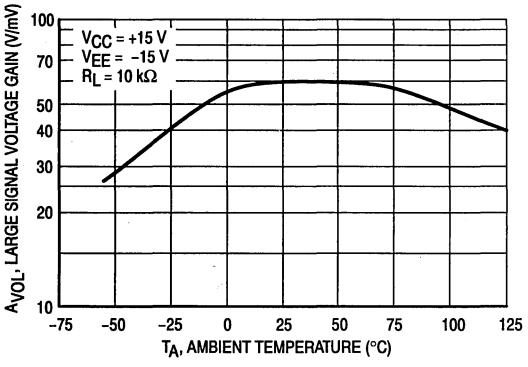


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Figure 7. Open-Loop Voltage Gain and Phase versus Freqeucny

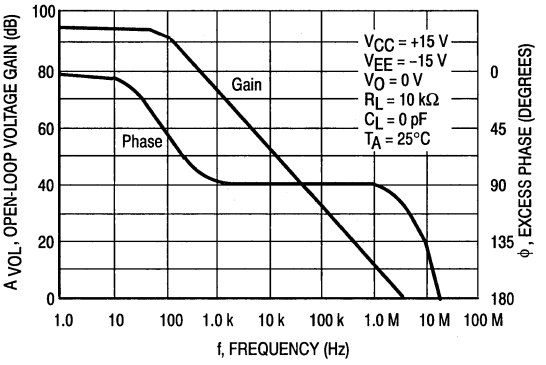


Figure 8. Supply Current per Amplifier versus Supply Voltage

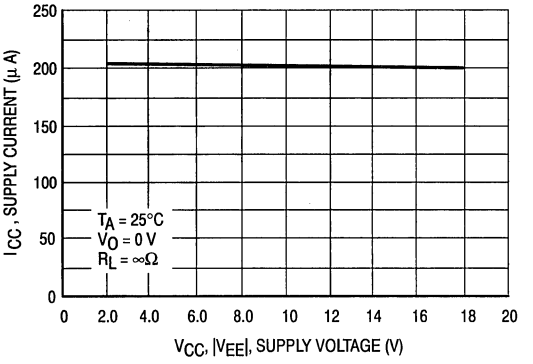


Figure 9. Supply Current per Amplifier versus Temperature

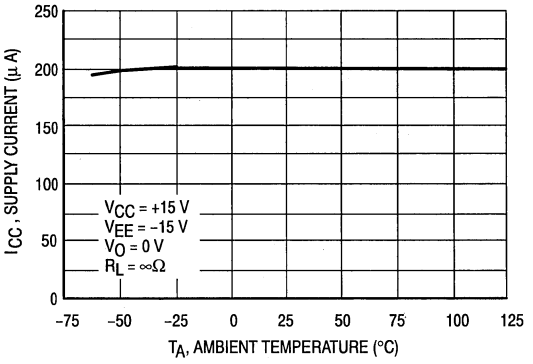


Figure 10. Total Power Dissipation versus Temperature

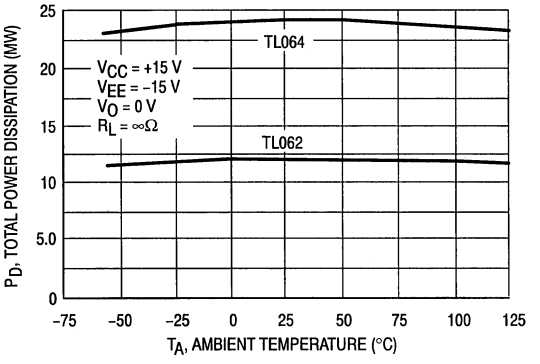


Figure 11. Common Mode Rejection versus Temperature

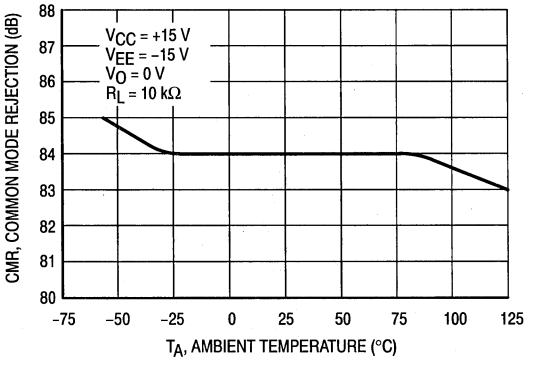


Figure 12. Common Mode Rejection versus Frequency

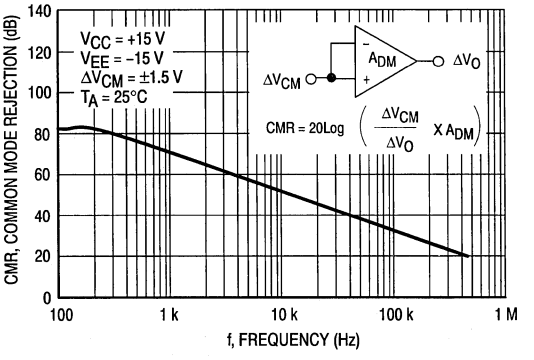


Figure 13. Power Supply Rejection versus Frequency

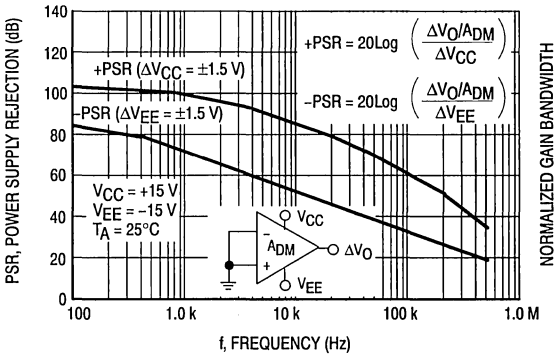


Figure 14. Normalized Gain Bandwidth Product, Slew Rate and Phase Margin versus Temperature

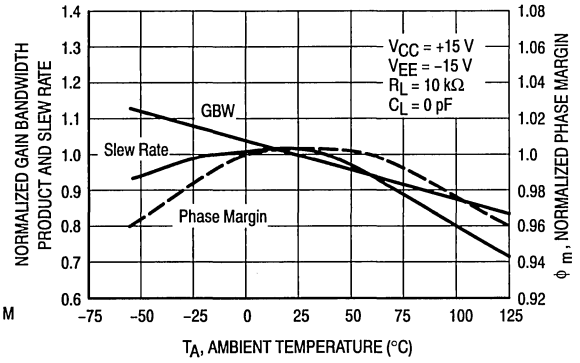


Figure 15. Input Bias Current versus Temperature

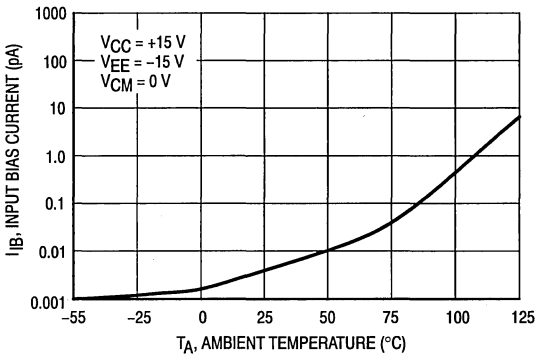


Figure 16. Input Noise Voltage versus Frequency

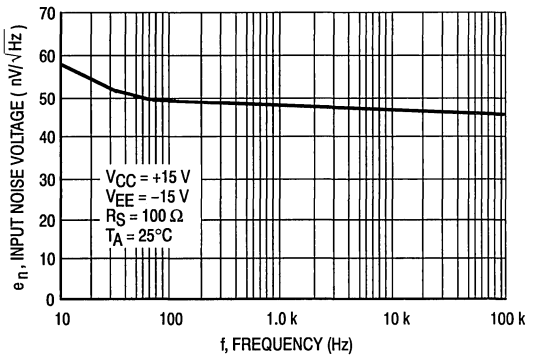


Figure 17. Small Signal Response

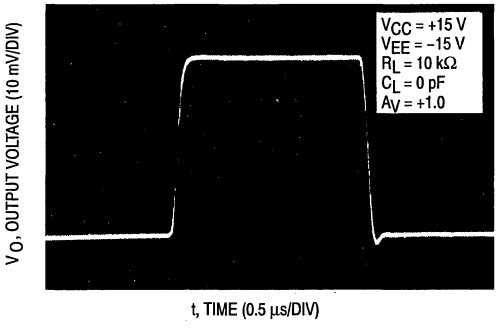
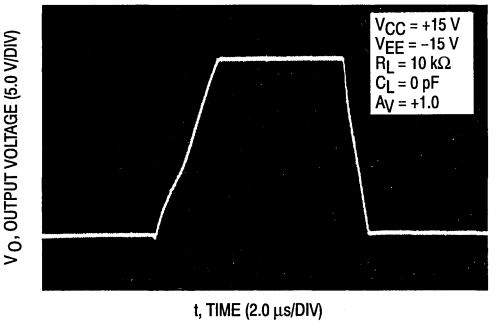


Figure 18. Large Signal Response



2

Figure 19. AC Amplifier

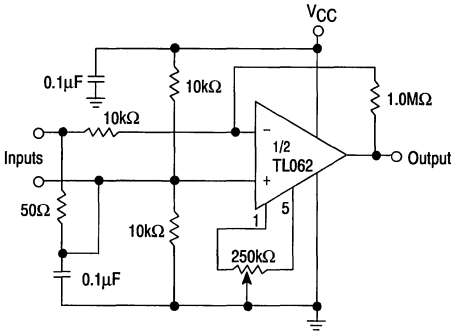


Figure 20. High-Q Notch Filter

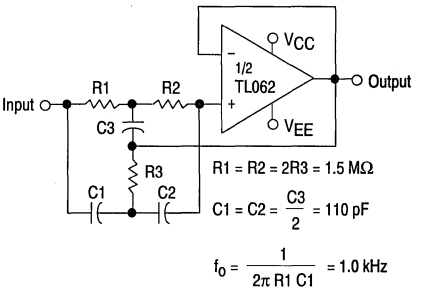


Figure 21. Instrumentation Amplifier

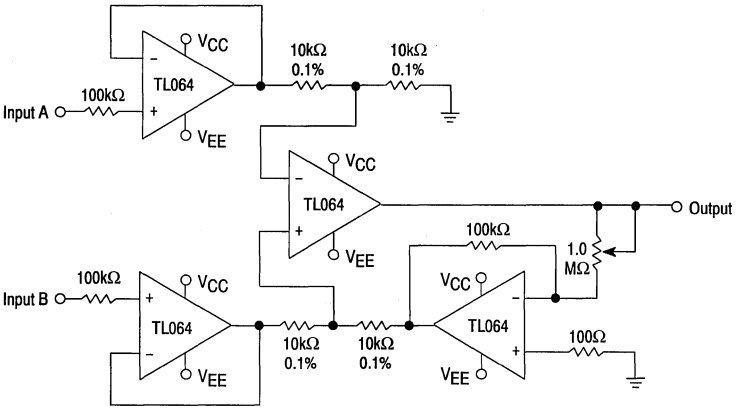


Figure 22. 0.5 Hz Square-Wave Oscillator

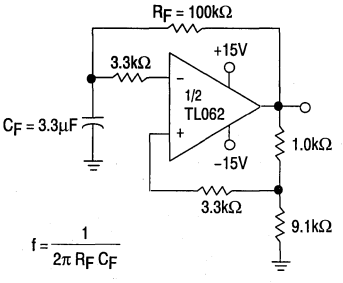
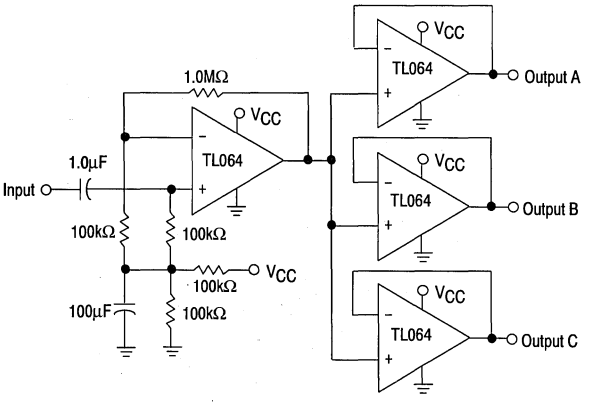


Figure 23. Audio Distribution Amplifier



TL071
TL072
TL074

LOW NOISE, JFET INPUT OPERATIONAL AMPLIFIERS

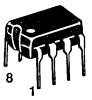
SILICON MONOLITH
INTEGRATED CIRCUIT

Low Noise, JFET Input Operational Amplifiers

These low noise JFET input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents. Moreover, the devices exhibit low noise and low harmonic distortion making them ideal for use in high fidelity audio amplifier applications.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products.

- Low Input Noise Voltage: 18 nV/$\sqrt{Hz}$ Typ
- Low Harmonic Distortion: 0.01% Typ
- Low Input Bias and Offset Currents
- High Input Impedance: 10^{12} Ω Typ
- High Slew Rate: 13 V/μs Typ
- Wide Gain Bandwidth: 4.0 MHz Typ
- Low Supply Current: 1.4 mA per Amp

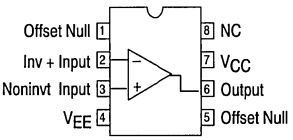


P SUFFIX
PLASTIC PACKAGE
CASE 626

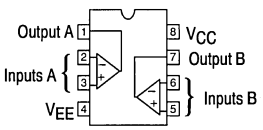
JG SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS

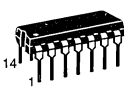


TL071 (Top View)



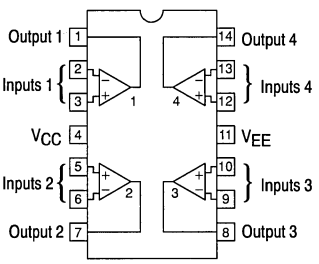
TL072 (Top View)

N SUFFIX
PLASTIC PACKAGE
CASE 646
(TL074 Only)



J SUFFIX
CERAMIC PACKAGE
CASE 632
(TL074 Only)

PIN CONNECTIONS



TL074 (Top View)

ORDERING INFORMATION

Op Amp Function	Device	Temperature Range	Package
Single	TL071ACD, CD	0° to +70°C	SO-8
	TL071ACJG, CJG		Ceramic DIP
	TL071ACP, CP		Plastic DIP
Dual	TL072ACD, CD	0° to +70°C	SO-8
	TL072ACJG, CJG		Ceramic DIP
	TL072ACP, CP		Plastic DIP
Quad	TL074ACJ, CJ	0° to +70°C	Ceramic DIP
	TL074ACN, CN		Plastic DIP

2

MAXIMUM RATINGS

Rating	Symbol	TL07_C TL07_AC	Unit
Supply Voltage	V_{CC} V_{EE}	+18 −18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Power Dissipation Plastic Package (N, P) Derate above T_A = +47°C Ceramic Package (J, JG) Derate above T_A = +82°C	 P_D $1/\theta_{JA}$ P_D $1/\theta_{JA}$	 680 10 680 10	 mW mW/°C mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES: 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 V, whichever is less.
2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{high} to T_{low} [Note 3])

Characteristics	Symbol	TL07_C TL07_AC Min	Typ	Max	Unit
Input Offset Voltage (R_S ≤ 10 k, V_{CM} = 0) TL071, TL072 TL074 TL07_A	V_{IO}	 — — —	 — — —	 13 13 7.5	mV
Input Offset Current (V_{CM} = 0) (Note 4) TL07_ TL07_A	I_{IO}	 — —	 — —	 2.0 2.0	nA
Input Bias Current (V_{CM} = 0) (Note 4) TL07_ TL07_A	I_{IB}	 — —	 — —	 7.0 7.0	nA
Large-Signal Voltage Gain (V_O = ±10 V, R_L ≥ 2.0 k) TL07_ TL07_A	A_{VOL}	 15 25	 — —	 — —	V/mV
Output Voltage Swing (Peak-to-Peak) (R_L ≥ 10 k) (R_L ≥ 2.0 k)	V_O	 24 20	 — —	 — —	V

NOTES: (continued)
3. T_{low} = 0°C for TL071C, TL071AC, TL072C, TL072AC, TL074C, TL074AC T_{high} = +70°C for TL071C, TL071AC, TL072C, TL072AC, TL074C, TL074AC
4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in Junction Temperature as shown in Figure 3. To maintain Junction Temperature as close to Ambient Temperature as possible, pulse techniques must be used during testing.

TEST CIRCUITS

Figure 1. Unity Gain Voltage Follower

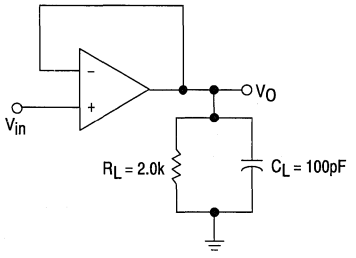
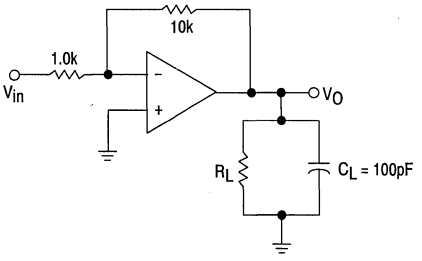


Figure 2. Inverting Gain of 10 Amplifier



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	TL07_C TL07_AC			Unit
		Min	Typ	Max	
Input Offset Voltage ($R_S \le 10$ k, V_{CM} = 0) TL071, TL072 TL074 TL07_A	V_{IO}	 — — —	 3.0 3.0 3.0	 10 10 6.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 50 Ω, T_A = T_{low} to T_{high} (Note 3)	$\Delta V_{IO}/\Delta T$	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0) (Note 4) TL07_ TL07_A	I_{IO}	 — —	 5.0 5.0	 50 50	pA
Input Bias Current (V_{CM} = 0) (Note 4) TL07_ TL07_A	I_{IB}	 — —	 30 30	 200 200	pA
Input Resistance	r_i	—	10^{12}	—	Ω
Common Mode Input Voltage Range TL07_ TL07_A	V_{ICR}	 ±10 ±11	 +15, −12 +15, −12	 — —	V
Large-Signal Voltage Gain (V_O = ±10 V, $R_L \ge$ 2.0 k) TL07_ TL07_A	A_{VOL}	 25 50	 150 150	 — —	V/mV
Output Voltage Swing (Peak-to-Peak) (R_L = 10 k)	V_O	24	28	—	V
Common Mode Rejection Ratio ($R_S \le 10$ k) TL07_ TL07_A	CMRR	 70 80	 100 100	 — —	dB
Supply Voltage Rejection Ratio ($R_S \le 10$ k) TL07_ TL07_A	PSRR	 70 80	 100 100	 — —	dB
Supply Current (Each Amplifier)	I_D	—	1.4	2.5	mA
Unity Gain Bandwidth	BW	—	4.0	—	MHz
Slew Rate (See Figure 1) V_{in} = 10 V, R_L = 2.0 k, C_L = 100 pF	SR	—	13	—	v/μs
Rise Time (See Figure 1)	t_r	—	0.1	—	μs
Overshoot Factor V_{in} = 20 mV, R_L = 2.0 k, C_L = 100 pF	—	—	10	—	%
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1000 Hz	e_n	—	18	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current R_S = 100 Ω, f = 1000 Hz	i_n	—	0.01	—	$pA/\sqrt{Hz}$
Total Harmonic Distortion V_O (RMS) = 10 V, $R_S \le$ 1.0 k $R_L \ge$ 2.0 k, f = 1000 Hz	THD	—	0.01	—	%
Channel Separation A_V = 100	—	—	120	—	dB

2

Figure 3. Input Bias Current versus Temperature

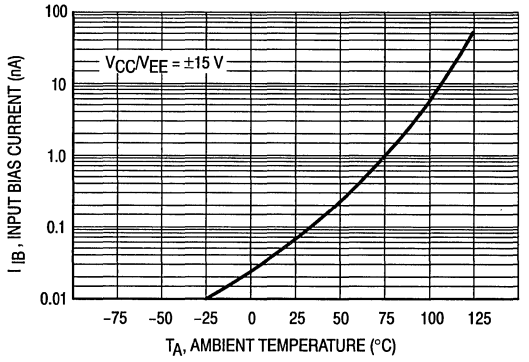


Figure 4. Output Voltage Swing versus Frequency

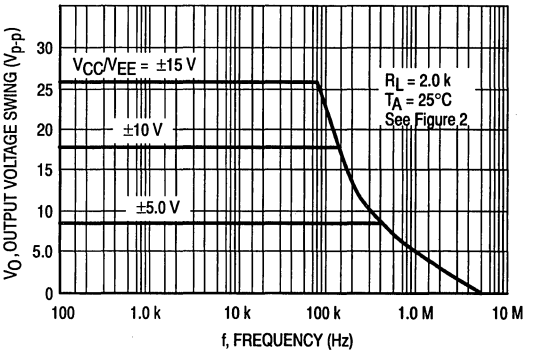


Figure 5. Output Voltage Swing versus Load Resistance

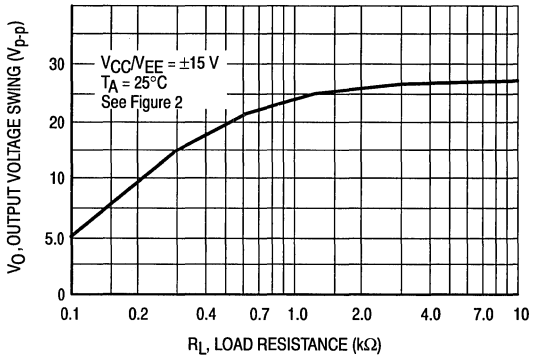


Figure 6. Output Voltage Swing versus Supply Voltage

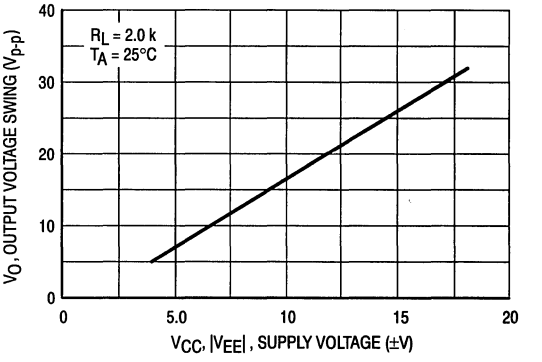


Figure 7. Output Voltage Swing versus Temperature

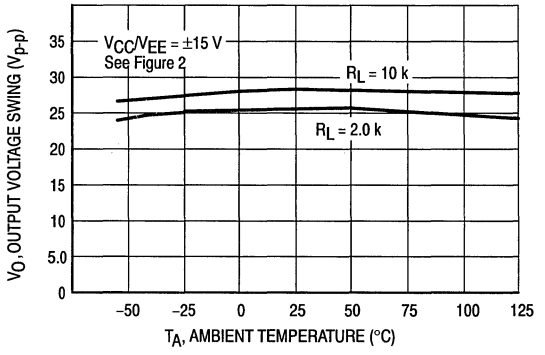


Figure 8. Supply Current per Amplifier versus Temperature

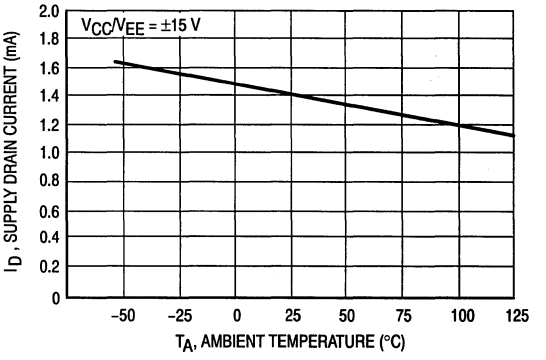


Figure 9. Large-Signal Voltage Gain and Phase Shift versus Frequency

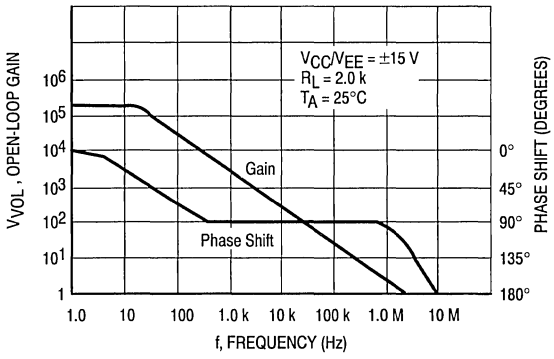


Figure 10. Large-Signal Voltage Gain versus Temperature

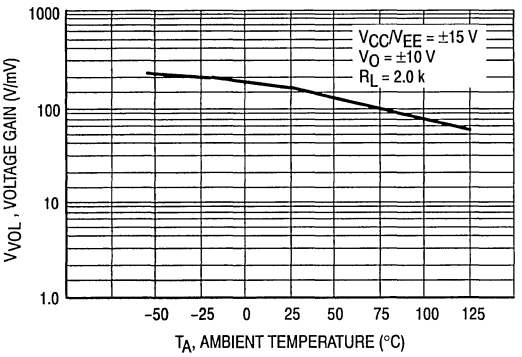


Figure 11. Normalized Slew Rate versus Temperature

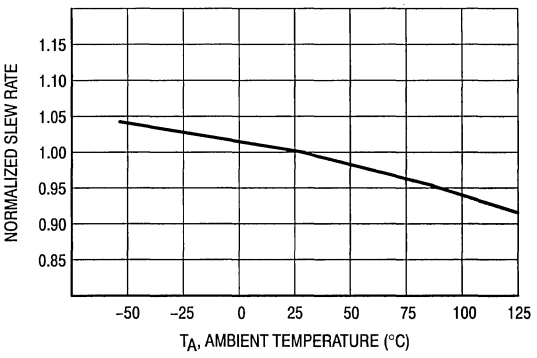


Figure 12. Equivalent Input Noise Voltage versus Frequency

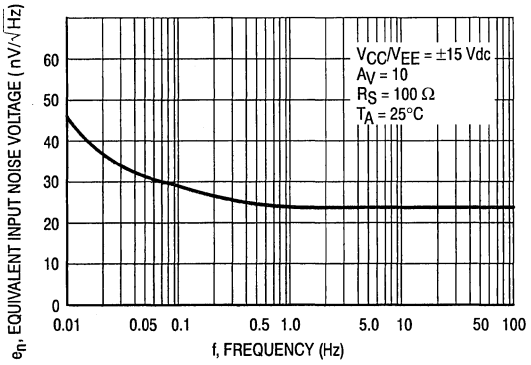
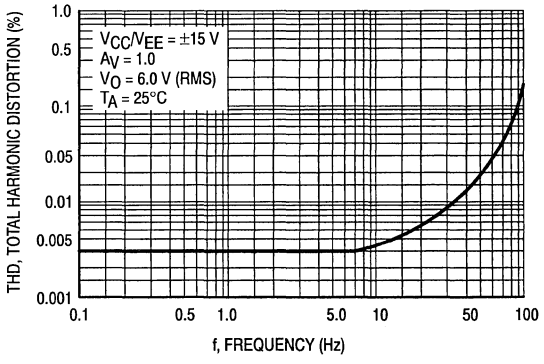


Figure 13. Total Harmonic Distortion versus Frequency



2

Representative Circuit Schematic
(Each Amplifier)

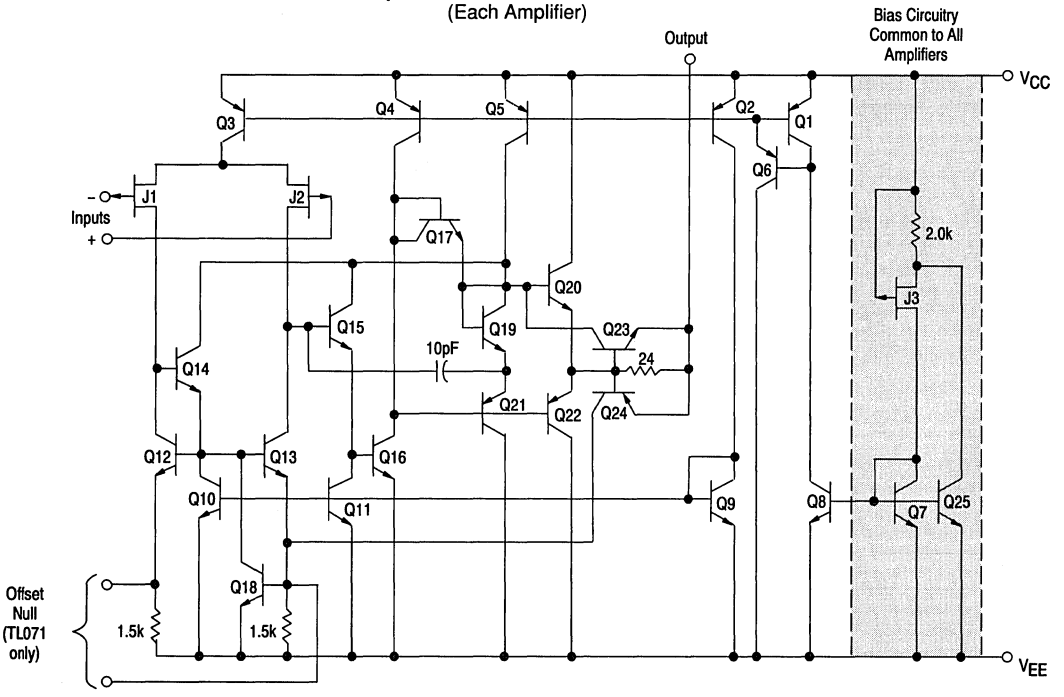


Figure 14. Audio Tone Control Amplifier

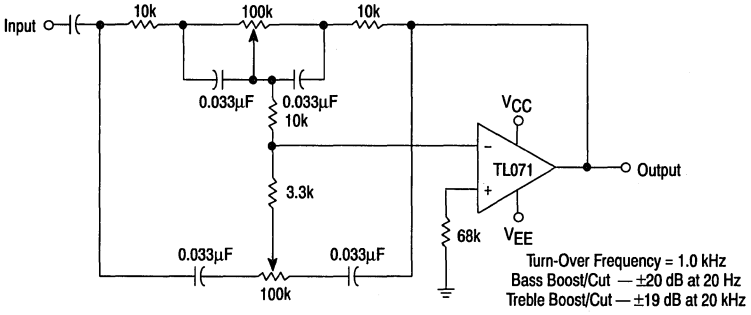
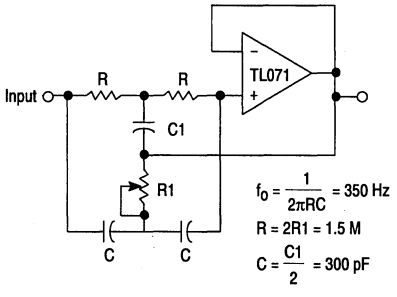


Figure 15. High Q Notch Filter



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

TL081
TL082
TL084

JFET INPUT OPERATIONAL AMPLIFIERS

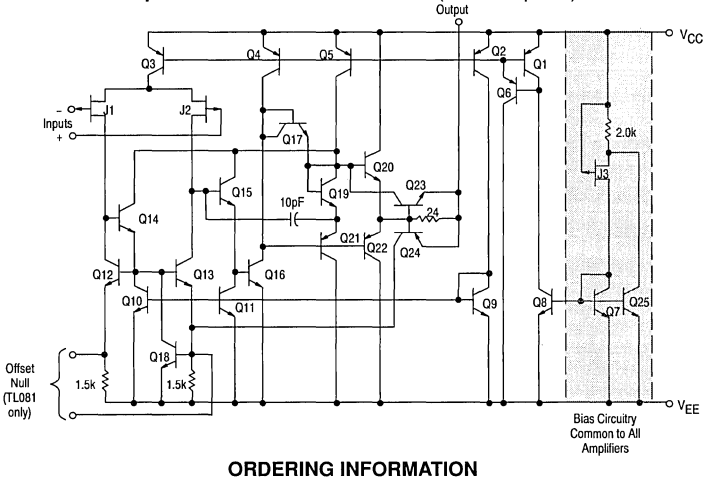
JFET Input Operational Amplifiers

These low-cost JFET input operational amplifiers combine two state-of- the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products. Devices with an "M" suffix are specified over the military operating temperature range of –55° to +125°C and those with a "C" suffix are specified from 0° to +70°C.

- Input Offset Voltage Options of 6.0 mV and 15 mV Max
- Low Input Bias Current: 30 pA
- Low Input Offset Current: 5.0 pA
- Wide Gain Bandwidth: 4.0 MHz
- High Slew Rate: 13 V/μs
- Low Supply Current: 1.4 mA per Amplifier
- High Input Impedance: 10^{12} Ω

Representative Circuit Schematic (Each Amplifier)



ORDERING INFORMATION

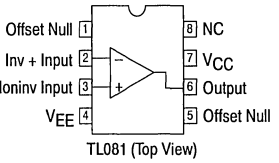
Op Amp Function	Device	Temperature Range	Package
Single	TL081ACD, CD	0° to +70°C	SO-8
	TL081ACJG, CJG		Ceramic DIP
	TL081ACP, CP		Plastic DIP
	TL081MJG	–55° to +125°C	Ceramic DIP
Dual	TL082ACD, CD	0° to +70°C	SO-8
	TL082ACJG, CJG		Ceramic DIP
	TL082ACP, CP		Plastic DIP
	TL082MJG	–55° to +125°C	Ceramic DIP
Quad	TL084ACJ, CJ	0° to +70°C	Ceramic DIP
	TL084ACN, CN		Plastic DIP
	TL084MJ	–55° to +125°C	Ceramic DIP

P SUFFIX
PLASTIC PACKAGE
CASE 626

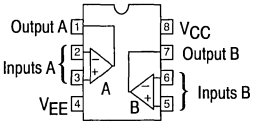
JG SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

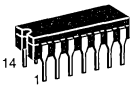
PIN CONNECTIONS



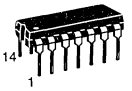
TL081 (Top View)



TL082 (Top View)

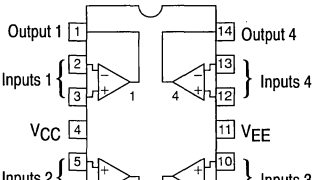


N SUFFIX
CERAMIC PACKAGE
CASE 632
(TL084 Only)



J SUFFIX
PLASTIC PACKAGE
CASE 646
(TL084 Only)

PIN CONNECTIONS



TL084 (Top View)

MAXIMUM RATINGS

Rating	Symbol	TL08_M	TL08_C TL08_AC	Unit
Supply Voltage	V_{CC} V_{EE}	+18 −18	+18 −18	V
Differential Input Voltage	V_{ID}	±30	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous		
Power Dissipation Plastic Package (N, P) Derate above T_A = +47°C Ceramic Package (J, JG) Derate above T_A = +82°C	 P_D $1/\theta_{JA}$ P_D $1/\theta_{JA}$	 — — 680 10	 680 10 680 10	 mW mW/°C mW mW/°C
Operating Ambient Temperature Range	T_A	−55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	−65 to +150	°C

NOTES: 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 V, whichever is less.
2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = T_{low} to T_{high} [Note 3].)

Characteristics	Symbol	TL08_M Min	TL08_M Typ	TL08_M Max	TL08_C TL08_AC Min	TL08_C TL08_AC Typ	TL08_C TL08_AC Max	Unit
Input Offset Voltage ($R_S \le 10$ k, V_{CM} = 0) TL081, TL082 TL084 TL08_A	V_{IO}	 — — —	 — — —	 9.0 15 —	 — — —	 — — —	 20 20 7.5	mV
Input Offset Current (V_{CM} = 0) (Note 4) TL08_ TL08_A	I_{IO}	 — —	 — —	 20 —	 — —	 — —	 5.0 3.0	nA
Input Bias Current (V_{CM} = 0) (Note 4) TL08_ TL08_A	I_{IB}	 — —	 — —	 50 —	 — —	 — —	 10 7.0	nA
Large-Signal Voltage Gain (V_O= ±10 V,$R_L \ge 2.0$ k) TL08_ TL08_A	A_{VOL}	 15 —	 — —	 — —	 15 25	 — —	 — —	V/mV
Output Voltage Swing (Peak-to-Peak) ($R_L \ge 10$ k) ($R_L \ge 2.0$ k)	V_O	 24 20	 — —	 — —	 24 20	 — —	 — —	V

NOTES: (continued)
3. T_{low} = −55°C for TL081M, TL082M, TL084M; 0°C for TL081C, TL081AC, TL082C, TL082AC, TL084C, TL084AC
T_{high} = +125°C for TL081M, TL082M, TL084M; T_{high} = +70°C for TL081C, TL081AC, TL082C, TL082AC, TL084C, TL084AC
4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in Junction Temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during testing.

Figure 1. Unity Gain Voltage Follower

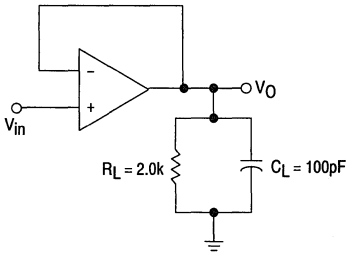
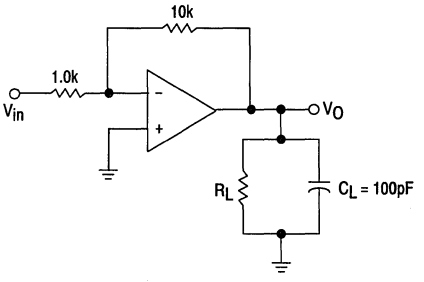


Figure 2. Inverting Gain of 10 Amplifier



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	TL08_M			TL08_C TL08_AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le 10$ k, V_{CM} = 0) TL081, TL082 TL084 TL08_A	V_{IO}	 — — —	 3.0 3.0 —	 6.0 9.0 —	 — — —	 5.0 5.0 3.0	 15 15 6.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 50 Ω, T_A = T_{low} to T_{high} (Note 3)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0) (Note 4) TL08_ TL08_A	I_{IO}	 — —	 5.0 —	 100 —	 — —	 5.0 5.0	 200 100	pA
Input Bias Current (V_{CM} = 0) (Note 4) TL08_ TL08_A	I_{IB}	 — —	 30 —	 200 —	 — —	 30 30	 400 200	pA
Input Resistance	r_i	—	10^{12}	—	—	10^{12}	—	Ω
Common Mode Input Voltage Range TL08_ TL08_A	V_{ICR}	 ±11 —	 +15, −12 —	 — —	 ±10 ±11	 +15, −12 +15, −12	 — —	V
Large-Signal Voltage Gain (V_O = ±10 V, $R_L \ge 2.0$ k) TL08_ TL08_A	A_{VOL}	 25 —	 150 —	 — —	 25 50	 150 150	 — —	V/mV
Output Voltage Swing (Peak-to-Peak) (R_L = 10 k)	V_O	24	28	—	24	28	—	V
Common Mode Rejection Ratio ($R_S \le 10$ k) TL08_ TL08_A	CMRR	 80 —	 100 —	 — —	 70 80	 100 100	 — —	dB
Supply Voltage Rejection Ratio ($R_S \le 10$ k) TL08_ TL08_A	PSRR	 80 —	 100 —	 — —	 70 80	 100 100	 — —	dB
Supply Current (Each Amplifier)	I_D	—	1.4	2.8	—	1.4	2.8	mA
Unity Gain Bandwidth	BW	—	4.0	—	—	4.0	—	MHz
Slew Rate (See Figure 1) V_{in} = 10 V, R_L = 2.0 k, C_L = 100 pF	SR	8.0	13	—	—	13	—	V/μs
Rise Time (See Figure 1)	t_r	—	0.1	—	—	0.1	—	μs
Overshoot Factor V_{in} = 20 mV, R_L = 2.0 k, C_L = 100 pF	—	—	10	—	—	10	—	%
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1000 Hz	e_n	—	25	—	—	25	—	$nV/\sqrt{Hz}$
Channel Separation A_V = 100	—	—	120	—	—	120	—	dB

2

Figure 3. Input Bias Current versus Temperature

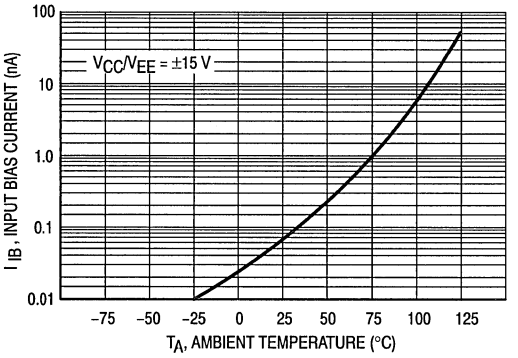


Figure 4. Output Voltage Swing versus Frequency

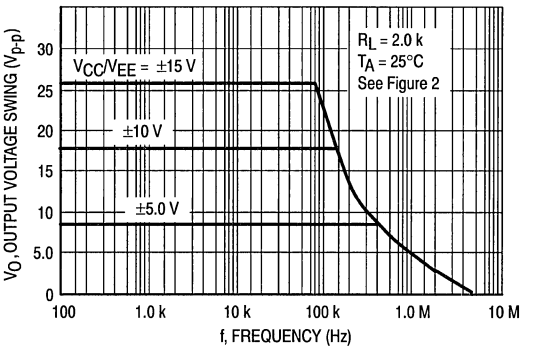


Figure 5. Output Voltage Swing versus Load Resistance

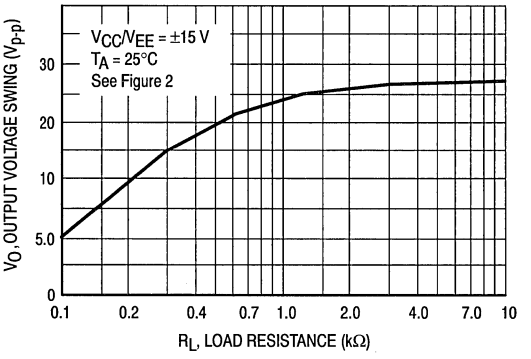


Figure 6. Output Voltage Swing versus Supply Voltage

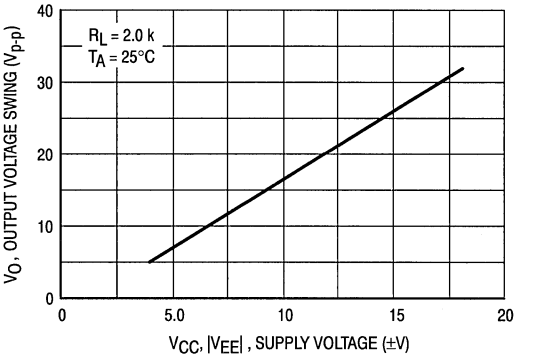


Figure 7. Output Voltage Swing versus Temperature

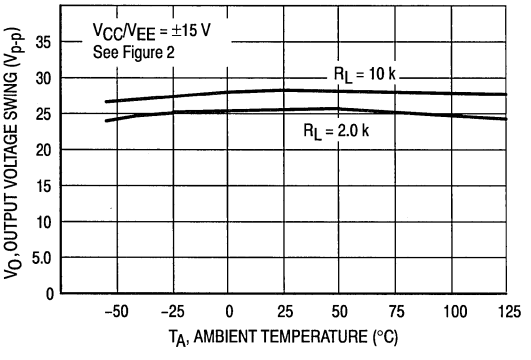


Figure 8. Supply Current per Amplifier versus Temperature

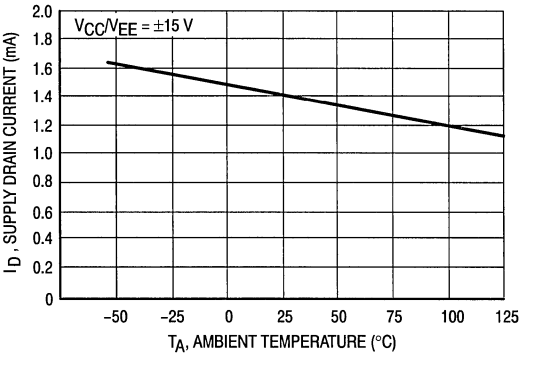


Figure 9. Large-Signal Voltage Gain and Phase Shift versus Frequency

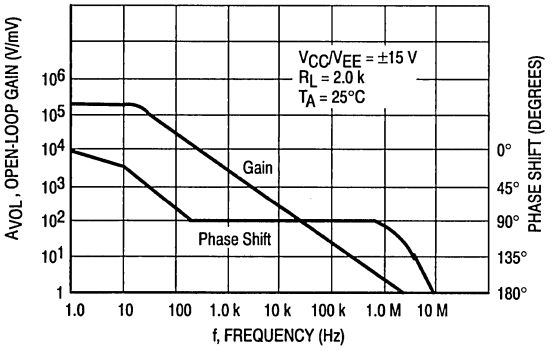


Figure 10. Large-Signal Voltage Gain versus Temperature

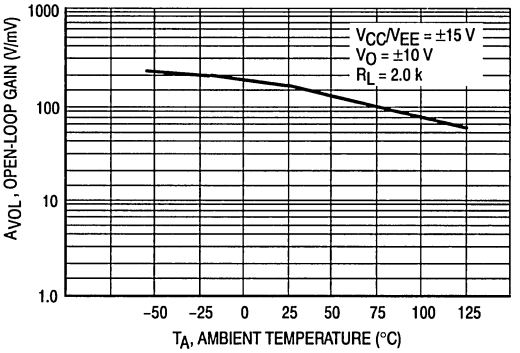


Figure 11. Normalized Slew Rate versus Temperature

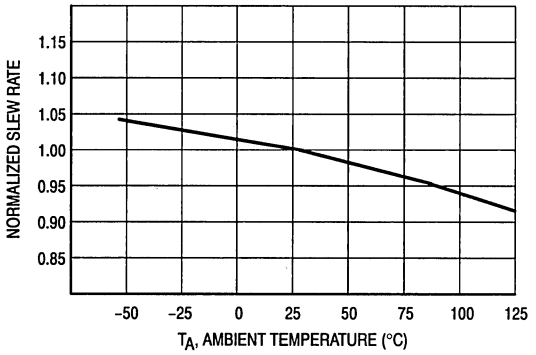


Figure 12. Equivalent Input Noise Voltage versus Frequency

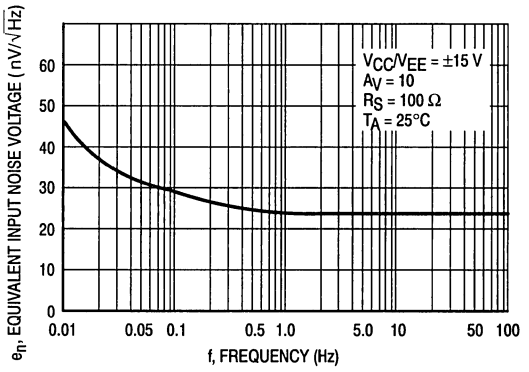
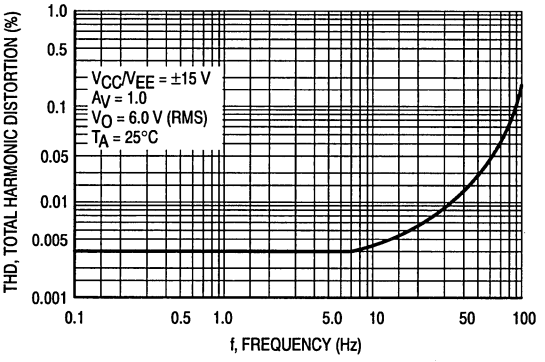
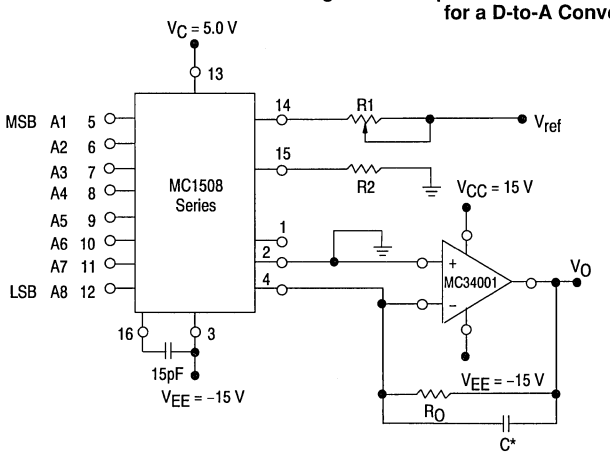


Figure 13. Total Harmonic Distortion versus Frequency



2

Figure 14. Output Current to Voltage Transformation for a D-to-A Converter



Settling time to within 1/2 LSB (+19.5 mV) is approximately 4.0 μs from the time all bits are switched.

*The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF)

Theoretical V_O

$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R14 or R_O so that V_O with all digital inputs at high level is equal to 9.961 V.

V_{ref} = 2.0 Vdc
$R_1 = R_2 \approx 1.0\ k\Omega$
$R_O = 5.0\ k\Omega$

$$V_O = \frac{2.0\ V}{1.0\ k}(5.0\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

Figure 15. Positive Peak Detector

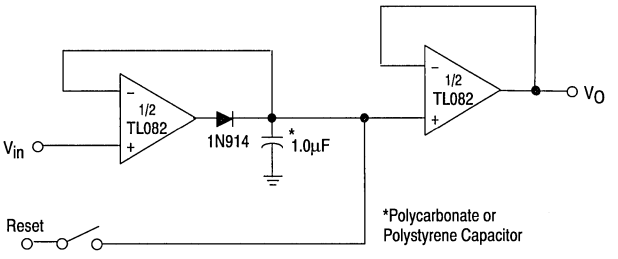
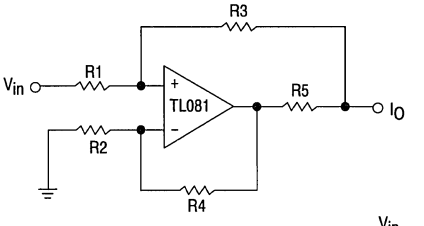
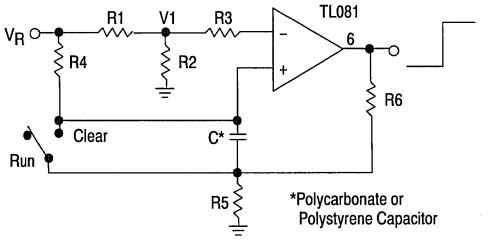


Figure 16. Voltage Controlled Current Source



If R1 through R4 > > R5 then $I_{out} = \frac{V_{in}}{R5}$

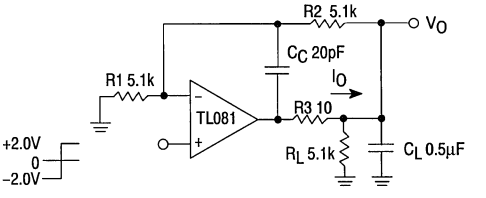
Figure 17. Long Interval RC Timer



Time (t) = R4 Cℓn (V_R/V_R-V_I), $R_3 = R_4$, $R_5 = 0.1\ R_6$
If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer
V_R = 10 V C = I.0 mF R3 = R4 = 144 M
R6 = 20 k R5 = 2.0 k R1 = R2 = 1.0 k

Figure 18. Isolating Large Capacitive Loads



- Overshoot < 10%
- t_s = 10 μs
- When driving large C_L, the V_O slew rate is determined by C_L and $I_{O(max)}$:

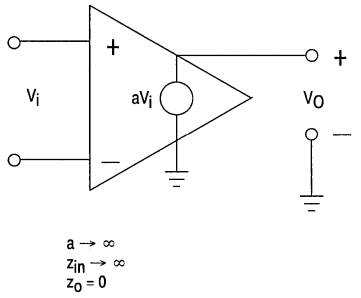
$$\frac{\Delta V_O}{\Delta t} = \frac{I_O}{C_L} \cong \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s \text{ (with } C_L \text{ shown)}$$

Addendum
Operational Amplifier
Application Information

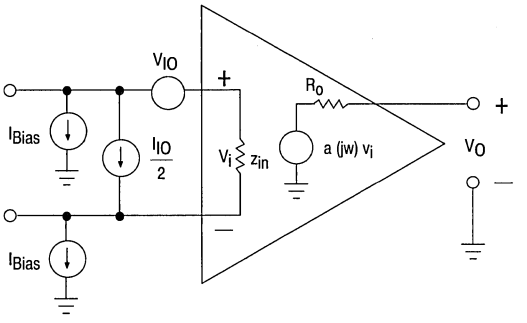
The Ideal Operational Amplifier

An ideal op amp has infinite input impedance, infinite gain, and zero output impedance. Its output is proportional to the differential voltage between the inputs. In reality, slight mismatches between the inputs create an error voltage and current, the input impedance is finite, requiring a small bias current, and gain and operating frequency are limited.

Ideal Op Amp



Equivalent Circuit for Actual Op Amp



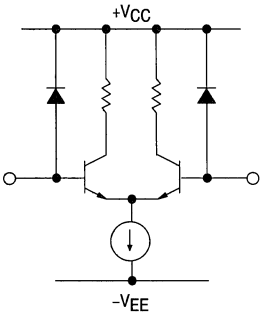
ESD Protection

Newer Motorola devices are equipped with either electrostatic discharge (ESD) diodes or CEO clamps on the inputs to increase their reliability. ESD diodes are connected with the anode attached to the input and the cathode to V_{CC}. During normal operation, the diode should be transparent to the user. However, if the input exceeds V_{CC} by more than a diode drop, the ESD diode will be forward biased and will provide a current path from the input to V_{CC}. Unless the current is limited externally the device could be damaged from overheating.

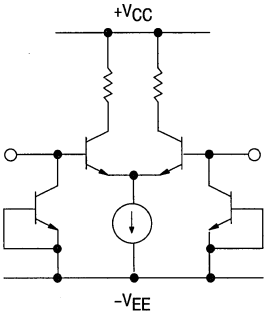
An alternate scheme uses a CEO transistor clamp with the collector connected to the input and the emitter and base connected to V_{EE}. This ESD protection method is totally transparent to the user. Although it is not recommended that the inputs be allowed to exceed V_{CC}, the CEO clamp will not affect device operation. The inputs should never exceed V_{EE}, with or without ESD protection. Single supply op amps are particularly sensitive to damage in a reverse bias condition.

If ESD protection is used on an amplifier, the ESD scheme used will be identified in the data sheet.

ESD Diodes



CEO Clamps

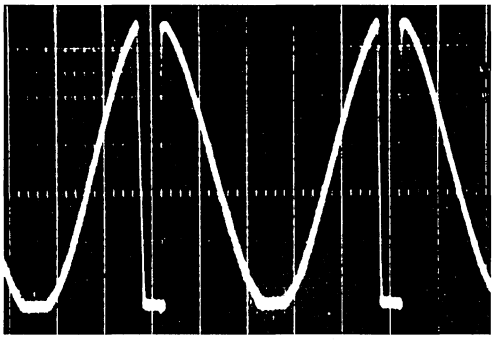


JFET Inputs versus Bipolar Inputs

Although JFET input op amps are generally associated with high speed, there are now bipolar input op amps with comparable slew rates. JFETS do offer higher input impedance and lower input bias current than a typical bipolar input. But for the lowest noise and offset voltage a bipolar input op amp is a better choice. A bipolar input is also required for true single supply operation. Any op amp can be operated with one supply. But the common mode input voltage range of a single supply op amp includes ground.

Phase Reversal

Most op amp data sheets describe both a maximum input voltage and a minimum common mode input voltage range for the device. The input voltage limit given in the Maximum Ratings Table is considered to be the highest voltage that can be applied without damaging the device. It does not guarantee the device will function normally or within the given electrical specifications. The input common mode voltage range (V_{ICR}), on the other hand, provides the maximum input voltage (for the conditions listed) for normal operation. Exceeding the input common mode range may cause the device to exceed the electrical specifications, latch or go into phase reversal. (As shown in figure at right.)



In a latch condition, the op amp output goes to one of the supply rails, and will remain in that state until the power is removed and reapplied with the error condition corrected. In phase reversal, a normal output low would be seen as an output high, but phase reversal will self correct once the input drops below a certain level. The input voltage required for phase reversal to occur varies, but it is usually seen if the input voltage approaches or exceeds the supply voltage. As you can see in the figure the output is clipping on the negative peaks, and phase reversing on the positive peaks. But as the input drops on the negative going part of the waveform, the output returns the the correct state without powering down the device.

Thermal Considerations

Thermal resistance (θ_{JA}) information is given on most packages in the back of the data book. Low power op amps can handle a short circuit current condition indefinitely. Since some of the higher current drive op amps can deliver a hundred milliamps to an amp in a short circuit condition, extra care is needed to ensure that the maximum junction temperature of the part is not exceeded.

$T_J = T_A + P_D Q_{JA}$

T_J = Junction Temperature (Should not exceed 150°C in a plastic package)

T_A = Ambient Temperature

P_D = Power Dissipation

Q_A = Package Thermal Impedance

Stability and Compensation

Most op amps are internally compensated, enabling them to be used in a unity gain configuration. Uncompensated or decompensated amplifiers have a higher slew rate if no external compensation capacitor is used, but must either be used in a gain of 2 or more or with positive feedback to ensure stable operation. When externally compensating an amplifier, use a capacitor equal or greater than the value recommended in the data sheet. Since the external loop affects the stability of the op amp, the amplifier needs to be evaluated in the circuit and over temperature to determine the minimum amount of compensation required.

Insufficient compensation will cause a high frequency oscillation — higher than the unity gain frequency of the device. This high frequency oscillation is indicative of an instability in the Miller loop, internal to the device. Lower frequency oscillation (below the unity gain frequency of the amplifier) is generally caused by an instability in the outer loop.

The two primary causes of low frequency oscillation are capacitive loading on the output and high differential source resistance. Capacitive loading, which can be either distributed capacitance or an actual load capacitor, can be a problem with as little as 100 pF. Sensitivity to load capacitance varies from op amp to op amp and is not always given in the data sheets. To compensate for capacitive loading, add a small resistor in series with the output. Depending on the load and the external loop, 10 Ω to 100 Ω is generally sufficient (see Figure A). For high capacitive loading, (C_L>1500 pF) a capacitor in the feedback loop may also be necessary (see Figure B).

Keeping the differential source resistance low not only limits the noise generated in the circuit, but avoids stability problems as well. Most op amps are stable with a source resistance of up to 2k Ω, but that varies from op amp to op amp. The differential source resistance (which includes any feedback resistance) combines with the input capacitance of the op amp to create a low frequency pole. The higher the resistance, the more likely you are to have an oscillation problem. Adding a small capacitor in parallel with the feedback resistor may solve the problem (see Figure C). The capacitor should be greater than the input capacitance of the op amp which is typically about 10 pF.

Figure A. Compensation Circuit for Moderate Capacitive Loads

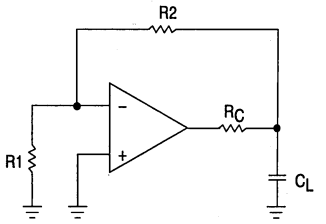


Figure B. Compensation Circuit for High Capacitive Loads

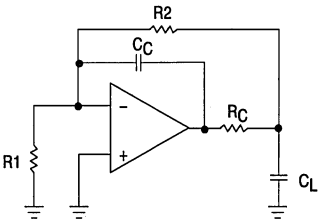
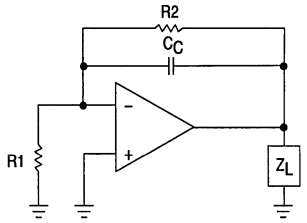


Figure C. Compensation for High Source Impedance



Layout Considerations

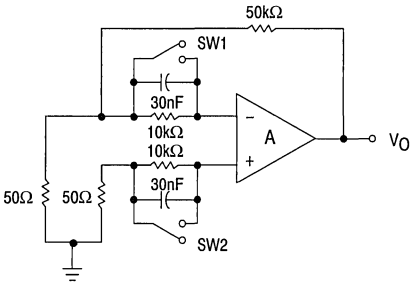
Higher frequency op amps may require special attention to layout. Since most layout problems are not reflected in computer simulations, it is worth it to follow proper layout rules consistently. Some suggestions:

- *Always* bypass the supply pins with at least 0.01 μF to ground, whether or not it is a high frequency application. Some amplifiers have a much lower power supply rejection with respect to the negative supply than to the positive supply due to the internal compensation. A larger bypass capacitor from V_{EE} to ground may be used to prevent high frequency transients from appearing on the output. Generally 10 μF to 20 μF is sufficient.
- Make sure you have a good ground plane.
- Keep AC and DC grounds separate.
- Don't use proto boards or wire wrap for high frequency circuits.
- Use appropriate external components — avoid electrolytics in high frequency paths.
- Keep high frequency paths short (including the leads on discrete components).
- Ground the inputs of unused op amps.

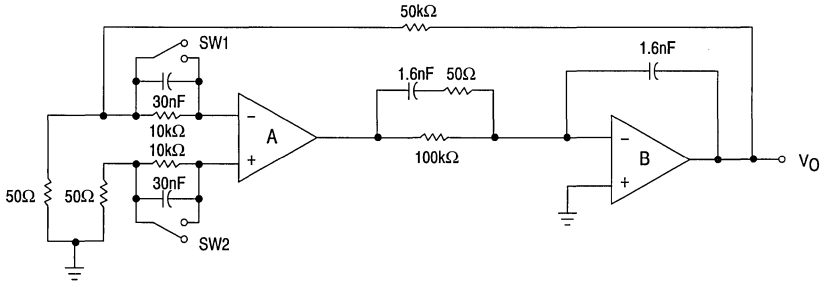
Test Information

The following circuit can be used to test V_{IO}, I_{IO}, and I_{IB}. Op Amp A is the device under test, and Op Amp B is a buffer amplifier which reduces CMRR errors and improves the accuracy of the measurement. The 30 nF capacitors across the 10k Ω source resistors are for stability and may not be needed.

A) Without Buffer Amplifier



B) With Buffer Amplifier



V_{IO} can be measured directly with SW1 and SW2 closed.

To determine I_{IB-}:

- Measure V_{IO} with both switches close,
- Open SW1 only; Measure V_{IO1}

To determine I_{IB+}:

- Close SW1 and open SW2; Measure V_{IO2}

I_{IO} equals the difference between I_{IB+} and I_{IB-}

GLOSSARY

2

Input Offset Voltage (V_{IO}) — The voltage which must be applied between the inputs of an op amp to obtain a zero output voltage. For an ideal op amp, V_{IO} would be zero. Some vendors abbreviate it V_{OS}.

Input Bias Current (I_{IB}) — The current flowing in or out of both inputs of an op amp. JFET input op amps provide the lowest input bias current; typically in the picoamp range. A bipolar input op amp is typically in nanoamps. I_{IB} is highly sensitive to slight process variations and can vary an order of magnitude.

Input Offset Current (I_{IO}) — Ideally, the bias currents on the two inputs are equal. The input offset current is the difference between the two currents when the output is at zero volts. Sometimes abbreviated I_{OS}. This should not be confused with the output short circuit current (I_{SC}).

Input Common Mode Voltage Range (V_{ICR}) — The maximum input voltage range for normal operation within given specifications. Exceeding the input common mode range generally will not damage the inputs if the maximum ratings are not exceeded. However, V_{IO} may not meet the specification given in the data sheet and phase reversal may occur as the input voltage approaches V_{CC} or V_{EE}. Sometimes abbreviated V_{CM}.

Common Mode Rejection Ratio (CMR or CMRR) — CMRR is defined as the ratio of the common mode gain to the differential mode gain. It is also equal to the ratio of the input common mode voltage to the peak-to-peak change in V_{IO}. Measures the ability of an op amp to reject a signal present at both inputs simultaneously. May be given in dB or volts per volt.

Power Supply Rejection Ratio (PSR or PSRR) — The ratio of the change in V_{IO} to the change in power supply voltage. Measures the immunity of the amplifier to changes in power supply voltage.

Output Short Circuit Current (I_{SC}) — The maximum current an amplifier can deliver into a short circuit. Care must be exercised to ensure the maximum junction temperature of the device is not exceeded to prevent damage to the device.

Supply Current (I_D or I_{CC}) — The operating current required with no load and with the output at zero volts.

Slew Rate (SR) — The rate of change of the output voltage in response to a large amplitude pulse applied to the input. The slew rate determines the power bandwidth of the device.

Gain Bandwidth Product (GBW) — The product of the closed loop gain times the frequency response at a given frequency. For an op amp with a single pole roll-off, the gain bandwidth product is equal to the unity gain frequency.

Phase Margin (ϕ_M) — 180° minus the phase shift at the unity gain frequency of the device. The phase margin must be positive for unconditionally stable operation. Phase margin (and stability) are affected by the external circuit, particularly the capacitive loading on the output and the differential source resistance on the input.

Channel Separation (CS) — A measurement of the immunity of one op amp to a signal present on another amplifier in a dual or quad.

Power Bandwidth (BWP) — The frequency at which the output starts to clip or distort at maximum peak to peak input voltage.

Power Supply Circuits

3

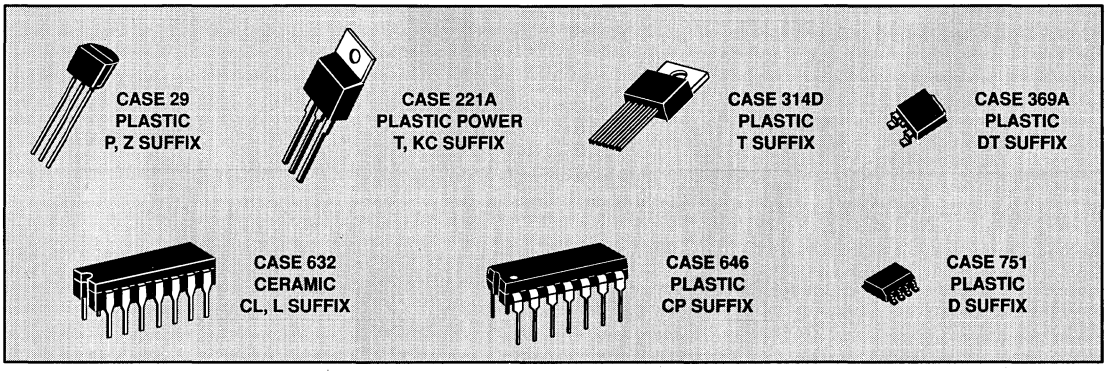
In Brief . . .

In most electronic systems some form of voltage regulation is required. In the past, the task of voltage regulator design was tediously accomplished with discrete devices, and the results were quite often complex and costly. Today, with bipolar monolithic regulators, this task has been significantly simplified. The designer now has a wide choice of fixed, low V_{diff}, adjustable, and tracking series-type voltage regulators. These devices incorporate many built-in protection features, making them virtually immune to the catastrophic failures encountered in older discrete designs.

The Switching Power Supply continues to increase in popularity and is one of the fastest growing markets in the world of power conversion. They offer the designer several important advantages over linear series-pass regulators. These advantages include significant advancements in the areas of size and weight reduction, improved efficiency, and the ability to perform voltage step-up, step-down, and voltage-inverting functions. Motorola offers a diverse portfolio of full featured switching regulator control circuits which meet the needs of today's modern compact electronic equipment.

Power supplies, MPU/MCU-based systems, indust- rial controls, computer systems and many other product applications are requiring power supervisory functions which monitor voltages to ensure proper system operation. Motorola offers a wide range of power supervisory circuits that fulfill these needs in a cost effective and efficient manner. MOSFET drivers are also provided to enhance the drive capabilities of first generation switching regulators or systems designed with CMOS/TTL logic devices. These drivers can also be used in DC-to-DC converters, motor controllers or virtually any other application requiring high speed operation of power MOSFETs.

Page



3

Linear Voltage Regulators

Fixed Output

These low cost monolithic circuits provide positive and/or negative regulation at currents from 100 mA to 3.0 A. They are ideal for on-card regulation employing current limiting and thermal shutdown. Low V_{diff} devices are offered for battery powered systems.

Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Fixed-Voltage, 3-Terminal Regulators for Positive or Negative Polarity Power Supplies

V_{out} (V)	Tol.(1) (V)	I_O (mA) Max	Output Device		V_{in} Min/Max	Reg_{line} (mV)	Reg_{load} (mV)	$\Delta V_O/\Delta T$ (mV/°C) Typ	Suffix/ Package
			Positive	Negative					
3.3	±0.03	800	MC33269-3.3	—	4.3/20	0.3%	0.5%	—	D, DT
5.0	±0.5	100	LM2931-5.0	—	5.6/40	30	50	1.0	Z,T
			MC78L05C	MC79L05C	6.7/30	200	60		P
	±0.25		LM2931A-5.0	—	5.6/40	30	50		Z, T
			MC78L05AC	MC79L05AC, AB	6.7/30	150	60		P, D
		500	MC78M05C	MC79M05C	7.0/35	100	100		DT, T
	±0.5	750, 10	LM2935	—	5.6/26	30	50		T/314D
	±0.25	1500	MC7805B(2)	—	8.0/35	100	100	1.0	T
			MC7805C	MC7905C	7.0/35				
	±0.2		MC7805AC	MC7905AC	7.5/35	10		0.6	
	±0.25		LM340-5	—	7.0/35	50	50		
	±0.2		LM340A-5	—		10	25		
	±0.1		TL780-05C	—		5.0		0.06	KC
	±0.25	3000	MC78T05C	—	7.3/35	25	30	0.1	T
	±0.2		MC78T05AC	—		10	25		
	±0.25		LM323	—	7.5/20	25	100		
	±0.2		LM323A	—		15	50		
	±0.05	800	MC33269–5	—	6.0/20	0.3%	0.5%	—	D, DT
5.2	±0.26	1500	—	MC7905.2C	7.2/35	105	105	1.0	T

(1) Output Voltage Tolerance for Worst Case
(2) T_J = –40° to +125°C

Fixed-Voltage, 3-Terminal Regulators for Positive or Negative Polarity Power Supplies (continued)

V_{out} (V)	Tol.(1) (V)	I_O (mA) Max	Output Device		V_{in} Min/Max	Reg_{line} (mV)	Reg_{load} (mV)	$\Delta V_O/\Delta T$ (mV/°C) Typ	Suffix/ Package
			Positive	Negative					
6.0	±0.3	500	MC78M06C	—	8.0/35	100	120	1.0	T
		1500	MC7806B(2)	—	9.0/35	120		0.7	
			MC7806C	MC7906C	8.0/35				
	±0.24		MC7806AC	—	8.6/35	11	100		
	±0.3		LM340-6	—	8.0/35	60	60		
8.0	±0.8	100	MC78L08C	—	9.7/30	200	80	—	P
			MC78L08AC	—		175			
	±0.4	500	MC78M08C	—	10/35	100	160	1.0	DT, T
		1500	MC7808B(2)	—	11.5/35	160			T
			MC7808C	MC7908C	10.5/35				
	±0.3		MC7808AC	—	10.6/35	13	100		
	±0.4		LM340-8	—	10.5/35	80	80		
		3000	MC78T08C	—	10.4/35	35	30	0.16	
9.0	±0.39	1500	MC7809C	—	11.5/35	50	50	1.0	T
12	±0.12	800	MC33269-12	—	13/20	0.3%	0.5%	—	D, DT
	±1.2	100	MC78L12C	MC79L12C	13.7/35	250	100	—	P, D
	±0.6		MC78L12AC	MC79L12AC, AB					
		500	MC78M12C	MC79M12C	14/35	100	240	1.0	DT, T
		1500	MC7812B(2)	—	15.5/35	240		1.5	T
			MC7812C	MC7912C	14.5/35				
	±0.5		MC7812AC	—	14.8/35	18	100		
	±0.6		LM340-12	—	14.5/35	120	120		
	±0.5		LM340A-12	—		18	32		
	±0.24		TL780-12C	—		5.0		0.15	KC
	±0.6	3000	MC78T12C	—		45	30	0.24	T
	±0.5		MC78T12AC	—		18	25		
15	±1.5	100	MC78L15C	MC79L15C	16.7/35	300	150	—	P, D
	±0.75		MC78L15AC	MC79L15AC, AB					
		500	MC78M15C	MC79M15C	17/35	100	300	1.0	DT, T
		1500	MC7815B(2)	—	18.5/35	300		1.8	T
			MC7815C	MC7915C	17.5/35				
	±0.6		MC7815AC	—	17.9/35	22	100		
	±0.75		LM340-15	—	17.5/35	150	150		
	±0.6		LM340A-15	—		22	35		
	±0.3		TL780-15C	—		15	60	0.18	KC
	±0.75	3000	MC78T15C	—	17.5/40	55	30	0.3	T
	±0.6		MC78T15AC	—		22	25		
18	±1.8	100	MC78L18C	MC79L18C	19.7/35	325	170	—	P
	±0.9		MC78L18AC	MC79L18AC					

Fixed-Voltage, 3-Terminal Regulators for Positive or Negative Polarity Power Supplies (continued)

V_{out} (V)	Tol.(1) (V)	I_O (mA) Max	Output Device		V_{in} Min/Max	Reg_{line} (mV)	Reg_{load} (mV)	$\Delta V_O/\Delta T$ (mV/°C) Typ	Suffix/ Package
			Positive	Negative					
18	±0.9	500	MC78M18C	—	20/35	100	360	1.0	T
		1500	MC7818B(2)	—	22/35	360		2.3	
	±0.7		MC7818C	MC7918C	21/35				
			MC7818AC	—		31	100		
	±0.9		LM340-18	—		180	180		
20	±1.0	500	MC78M20C	—	22/40	10	400	1.1	T
24	±2.4	100	MC78L24C	MC79L24C	25.7/40	350	200	—	P
	±1.2		MC78L24AC	MC79L24AC		300			
		500	MC78M24C	—	26/40	100	480	1.2	T
		1500	MC7824B(2)	—	28/40	480		3.0	
			MC7824C	MC7924C	27/40				
	±1.0		MC7824AC	—	27.3/40	36	100		
	±1.2		LM340-24	—		240	240		

(1) Output Voltage Tolerance for Worst Case
(2) T_J = −40° to +125°C

Adjustable Output

Motorola offers a broad line of adjustable output voltage regulators with a variety of output current capabilities. Adjustable voltage regulators provide users the capability of stocking a single integrated circuit offering a wide range of output voltages for industrial and communications applications. The three-terminal devices require only two external resistors to set the output voltage.

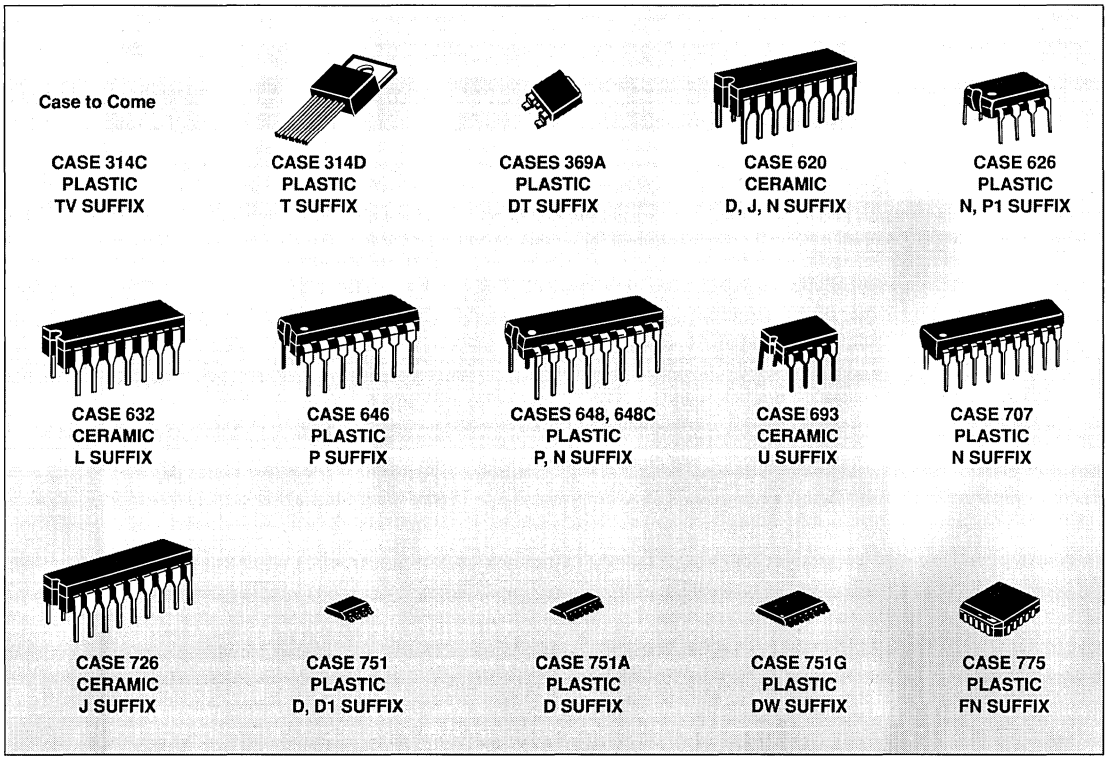
Adjustable Positive Output Regulators

I_O (mA) Max	Device	V_{out} (V)		V_{in} (V)		$V_{in} - V_{out}$ Differential (V) Min	P_D (W) Max		Regulation % V_{out} @ T_A = 25°C Max		T_C V_{out} Typ (%/°C)	T_J (°C) Max	Suffix/ Package
		Min	Max	Min	Max		T_A = 25°C	T_C = 25°C	Line	Load			
100	LM317L	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.006	125	Z
	LM2931C	3.0	24	3.16		0.6			0.15	1.0	—		T/314D
150	MC1723	2.0	37	9.5		3.0	1.25	—	0.1	0.3	0.003	150	CP
							1.5	—				175	CL
								—			0.002		L
500	LM317M	1.2		5.0			Internally Limited		0.04	0.5	0.0056	125	T
800	MC33269-ADJ	1.25	19	2.25	20	1.0			0.3		—	150	D, DT
1500	LM317	1.2	37	5.0	40	3.0			0.04		0.006	125	T
3000	LM350		33		36				0.03		0.008		

Adjustable Negative Output Regulators

500	LM337M	−1.2	−37	5.0	4.0	3.0	Internally Limited	0.04	1.0	0.0048	125	T
1500	LM337											

Special Regulators



Microprocessor Voltage Regulator/Supervisory Circuit

A 5.0 V fixed output with monitoring functions required in microprocessor-based systems.

Device	V_{out} (V) Min	V_{out} (V) Max	I_O (mA) Max	V_{in} (V) Min	V_{in} (V) Max	Reg_{line} (mV) Max	Reg_{load} (mV) Max	T_A (°C)	Suffix/ Package
MC34160	4.75	5.25	100	7.0	40	40	50	0 to + 70	P/648C
MC33160								–40 to + 85	
MC33267	4.9	5.2	500	6.0	26	50	50	–40 to +105	T, TV

SCSI Regulator

Device	V_{out} (V) Min	V_{out} (V) Max	I_{sink} (mA)	V_{in} (V) Min	V_{in} (V) Max	Reg_{line} (%)	Reg_{load} (%)	T_J (°C)	Suffix/ Package
MC34268	2.81	2.89	800	3.9	20	0.3	0.5	150	D/751, DT

Switching Regulator Control Circuits

These devices contain the primary building blocks which are required to implement a variety of switching power supplies. The product offerings fall into three major categories consisting of single-ended and double-ended controllers, plus single-ended ICs with on-chip power switch transistors. These circuits operate in voltage, current or resonant modes and are designed to drive many of the standard switching topologies. The single-ended configurations include buck, boost, flyback and forward converters. The double-ended devices control push-pull, half bridge and full bridge configurations.

Single-Ended Controllers

These single-ended voltage and current mode controllers are designed for use in buck, boost, flyback, and forward converters. They are cost effective in applications that range from 0.1 to 200 W power output.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	Suffix	T_A (°C)	Package
500 (Uncommitted Drive Output)	7.0 to 40	Voltage	5.0 ± 1.5%	200	MC34060A	D	0 to + 70	751A
						L		632
						P		646
					MC33060A	D	–40 to + 85	751A
						P		646
1000 (Totem Pole MOSFET Drive Output)	4.2 to 12	Current	1.25 ± 2.0%	300	MC34129	D	0 to + 70	751A
						P		646
					MC33129	D	–40 to + 85	751A
						P		646
	11.5 to 30		5.0 ± 2.0%	500 (Guaranteed at 250)	UC3842A	D	0 to + 70	751A
						N		626
	11 to 30		5.0 ± 1.0%		UC2842A	D	–25 to + 85	751A
						J		693
						N		626
	11.5 to 30		5.0 ± 2.0%		UC3842BV	D	–40 to +105	751A
						D1		751
						N		626
	8.2 to 30		5.0 ± 2.0%		UC3843A	D	0 to + 70	751A
						N		626
			5.0 ± 1.0%		UC2843A	D	–25 to + 85	751A
						J		693
						N		626
			5.0 ± 2.0%		UC3843BV	D	–40 to +105	751A
						D1		751
						N		626
	11.5 to 30		5.0 ± 2.0%	500 (50% Duty Cycle Limit)	UC3844	D	0 to + 70	751A
						N		626
	11 to 30	Current	5.0 ± 1.0%		UC2844	D	–25 to + 85	751A
						J		693
						N		626

Single-Ended Controllers (continued)

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	Suffix	T_A (°C)	Package
1000 (Totem Pole MOSFET Drive Output)	8.2 to 30	Current	5.0 ± 2.0%	500 (50% Duty Cycle Limit)	UC3845	D	0 to + 70	751A
						N		626
			5.0 ± 1.0%		UC2845	D	–25 to + 85	751A
						J		693
						N		626
	11.5 to 30		5.0 ± 2.0%	500 (Improved Oscillator Specifications with Frequency Guaranteed at 250 kHz)	UC3842B	D	0 to + 70	751A
						D1		751
						N		626
	11 to 30		5.0 ± 1.0%		UC2842B	D	–25 to + 85	751A
						D1		751
						N		626
	8.2 to 30		5.0 ± 2.0%		UC3843B	D	0 to + 70	751A
						D1		751
						N		626
			5.0 ± 1.0%		UC2843B	D	–25 to + 85	751A
						D1		751
						N		626
	11.5 to 30		5.0 ± 2.0%	500 (50% Duty Cycle Limit)	UC3844B	D	0 to + 70	751A
						D1		751
						N		626
					UC3844BV	D	–40 to +105	751A
						D1		751
						N		626
	11 to 30		5.0 ± 1.0%		UC2844B	D	–25 to + 85	751A
						D1		751
						N		626
	8.2 to 30		5.0 ± 2.0%		UC3845B	D	0 to + 70	751A
						D1		751
						N		626
					UC3845BV	D	–40 to +105	751A
						D1		751
						N		626
			5.0 ± 1.0%		UC2845B	D	–25 to + 85	751A
						D1		751
						N		626
1000 Source 1500 Sink (Split Totem Pole BIPOLAR Drive Output)	11 to 18		5.0 ± 6.0%	500 (50% Duty Cycle Limit)	MC44602	P2		648C

Single-Ended Controllers (continued)

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	Suffix	T_A (°C)	Package
2000 (Totem Pole MOSFET Drive Output)	9.2 to 30	Current	5.1 ± 1.0%	1000	MC34023	DW	0 to + 70	751G
						FN		775
						P		648
					MC33023	DW	–40 to + 85	751G
						FN		775
						P		648

Single-Ended Controllers with On-Chip Power Switch

These monolithic power switching regulators contain all the active functions required to implement standard DC-to-DC converter configurations with a minimum number of external components.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	Suffix	T_A (°C)	Package
1500 (Uncommitted Power Switch)	2.5 to 40	Voltage	1.25 ± 5.2%(1)	100	µA78S40	PC	0 to + 70	648
						DC		620
						PV	–40 to + 85	648
						DM	–55 to + 125	620
			1.25 ± 2.0%		MC34063A	D	0 to + 70	751
						P1		626
					MC33063A	D	–40 to + 85	751
						P1		626
					MC35063A	U	–55 to + 125	693
	3.0 to 65		1.25 ± 2.0% and 5.05 ± 3.0 %		MC34165	P	0 to + 70	648C
					MC33165		–40 to + 85	
3400 (Uncommitted Power Switch)	2.5 to 40				MC34163		0 to + 70	
					MC33163		–40 to + 85	
3400(2) (Dedicated Emitter Power Switch)	7.5 to 40		5.05 ± 2.0%	72 ± 12% Internally Fixed	MC34166	T	0 to + 70	314D
					MC33166		–40 to + 85	
5500(3) (Dedicated Emitter Power Switch)					MC34167		0 to + 70	
					MC33167		–40 to + 85	

(1) Tolerance applies over the specified operating temperature range.
(2) Guaranteed minimum, typically 4300 mA.
(3) Guaranteed minimum, typically 6500 mA.

Double-Ended Controllers

These double-ended voltage, current and resonant mode controllers are designed for use in push-pull, half-bridge, and full-bridge converters. They are cost effective in applications that range from 100 to 2000 watts power output.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	Suffix	T_A (°C)	Package
500 (Uncommitted Drive Outputs)	7.0 to 40	Voltage	5.0 ± 5.0%(1)	200	TL494	CN	0 to + 70	648
						CJ		620
						IN	–25 to + 85	648
						IJ		620
						MJ	–55 to + 125	
			5.0 ± 1.5%	300	TL594	CN	0 to + 70	648
						IN	–25 to + 85	
						MJ	–55 to + 125	620
± 500 (Totem Pole MOSFET Drive Outputs)	8.0 to 40		5.1 ± 2.0%	400	SG3525A	N	0 to + 70	648
						J		620
					SG3527A	N		648
						J		620
± 200 (Totem Pole MOSFET Drive Outputs)			5.0 ± 2.0%		SG3526	N	0 to +125(2)	707
						J		726
±1500 (Totem Pole MOSFET Drive Outputs)	9.6 to 20	Resonant (Zero Current Switch)	5.1 ± 2.0%	1000	MC34066	DW	0 to + 70	751G
						P		648
					MC33066	DW	–40 to + 85	751G
						P		648
				2000	MC34067	DW	0 to + 70	751G
						P		648
					MC33067	DW	–40 to + 85	751G
						P		648
2000 (Totem Pole MOSFET Drive Outputs)	9.2 to 30	Current	5.1 ± 1.0%	1000	MC34025	DW	0 to + 70	751G
						FN		775
						P		648
					MC33025	DW	–40 to + 85	751G
						FN		775
						P		648

(1) Tolerance applies over the specified operating temperature range.
(2) Junction Temperature Range.

Special Switching Regulator Controllers

Dual Channel Current Mode Controllers

These high performance dual channel controllers are optimized for off-line AC-to-DC power supplies and DC-to-DC converters in the flyback topology. The newer -H and -L versions have undervoltage lockout voltages which are optimized for off-line and lower voltage DC-to-DC converters respectively. Applications include desktop computers, peripherals, televisions, games, and various consumer appliances.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	Suffix	T_A (°C)	Package
±1000 (Totem Pole MOSFET Drive Outputs)	11 to 15.5	Current	5.0 ± 2.0%	500	MC34065	DW	0 to + 70	751G
						P		648
					MC33065	DW	–40 to + 85	751G
						P		648
	11 to 20		5.0 ± 2.6%		MC34065	DW-H	0 to + 70	751G
						P-H		648
					MC33065	DW-H	–40 to + 85	751G
						P-H		648
	8.2 to 20				MC34065	DW-L	0 to + 70	751G
						P-L		648
					MC33065	DW-L	–40 to + 85	751G
						P-L		648

Universal Microprocessor Power Supply Controller

A versatile power supply control circuit for microprocessor-based systems, this device is mainly intended for automotive applications and battery powered instruments. The circuit provides a power-on Reset delay and a Watchdog feature for orderly microprocessor operation.

Regulated Outputs	Output Current (mA)	V_{CC} (V)		Device	T_A (°C)	Reference (V)	Key Supervisory Features	Package
		Min	Max					
E^2PROM Programmable Output: 24 V (Write Mode) 5.0 V (Read Mode)	150 peak	6.0	35	TCF5600	–40 to + 85	2.5 ± 3.2%	MPU Reset and Watchdog Circuit	707
Fixed Linear Output: 5.0 V	10 to external buffer transistor			TCA5600	0 to + 75			

Power Factor Controllers

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Features	Device	Suffix	T_A (°C)	Package
± 500 (Totem Pole MOSFET Drive Outputs)	9.0 to 30	Current	± 2.5	Undervoltage Lockout, Internal Start-Up Timer	MC34261	D	0 to + 70	751
						P		626
					MC33261	D	– 40 to + 85	751
						P		626
				Overvoltage Comparator, Undervoltage Lockout, Internal Start-Up Timer	MC34262	D	0 to + 70	751
						P		626
					MC33262	D	– 40 to +105	751
						P		626

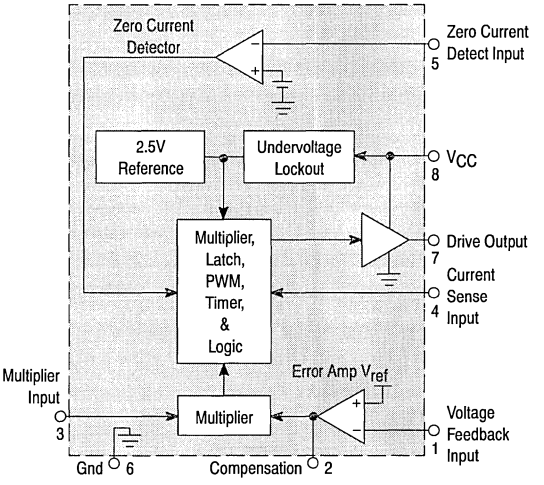
3

Power Factor Controllers

MC34261D, P T_A = 0° to +70°C, Case 751, 626
MC33261D, P T_A = – 40° to +85°C, Case 751, 626

The MC33261, MC34261 series are power factor controller circuits specifically designed for use as a preconverter in electronic ballast and in off-line converter applications. These integrated circuits feature an internal start-up timer, a one quadrant multiplier for near unit power factor, zero current detector to ensure critical conduction operation, high gain error amplifier, trimmed internal bandgap reference, current sensing comparator and a totem pole output ideally suited for driving a power MOSFET or an IGBT.

Also included are protective features consisting of input undervoltage lockout with hysteresis, cycle-by-cycle current limiting and a latch for single pulse metering.



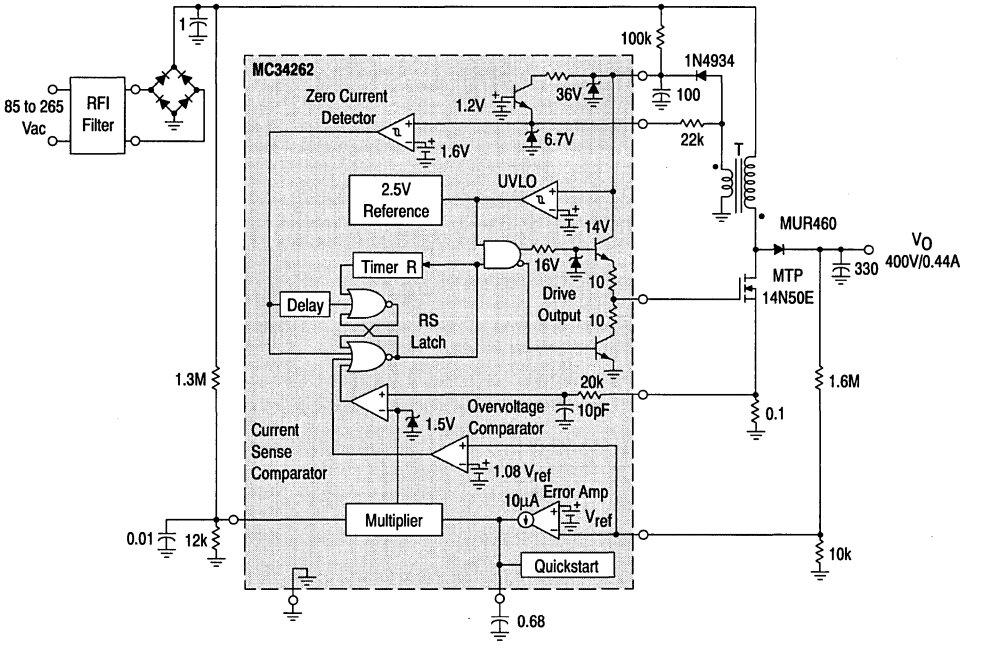
Power Factor Controllers

MC34262D, P T_A = 0° to + 85°C, Case 751, 626
MC33262D, P T_A = – 40° to +105°C, Case 751, 626

3

The MC34262, MC33262 series are active power factor controllers specifically designed for use as a preconverter in electronic ballast and in off-line power convertor applications. These integrated circuits feature an internal start-up timer for stand alone applications, a one quadrant multiplier for near unity power factor, zero current detector to ensure critical conduction operation, transconductance error amplifier, quickstart circuit for enhanced start-up, trimmed internal bandgap reference, current sensing comparator, and a totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of an overvoltage comparator to eliminate runaway output voltage due to load removal, input undervoltage lockout with hysteresis, cycle-by-cycle current limiting, multiplier output clamp that limits maximum peak switch current, an RS latch for single pulse metering, and a drive output high state clamp for MOSFET gate protection. These devices are available in dual-in-line and surface mount plastic packages.



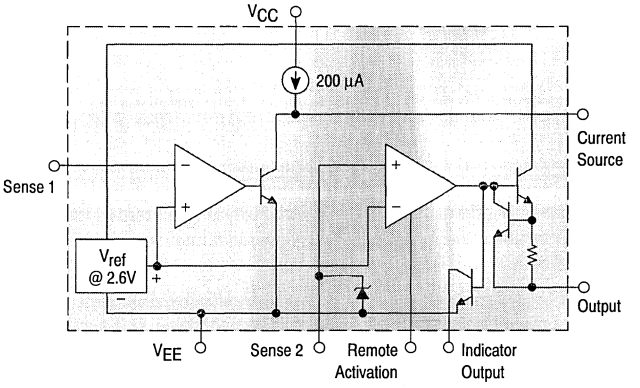
Power Supervisory Circuits

A variety of Power Supervisory Circuits are offered. Overvoltage sensing circuits which drive "Crowbar" SCRs are provided in several configurations from a low cost three-terminal version to 8-pin devices which provide pin-programmable trip voltages or additional features, such as an indicator output drive and remote activation capability. An over/undervoltage protection circuit is also offered.

Overvoltage Crowbar Sensing Circuit

MC3523U T_A = –55° to +125°C, Case 693
MC3423P1, U T_A = 0° to +70°C, Case 626, 693

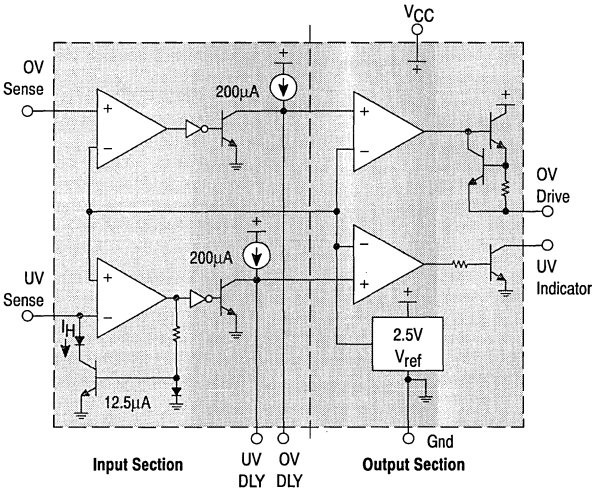
This device can protect sensitive circuitry from power supply transients or regulator failure when used with an external "Crowbar" SCR. The device senses voltage and compares it to an internal 2.6 V reference. Overvoltage trip is adjustable by means of an external resistive voltage divider. A minimum duration before trip is programmable with an external capacitor. Other features include a 300 mA high current output for driving the gate of a "Crowbar" SCR, an open-collector indicator output and remote activation capability.



Over/Undervoltage Protection Circuit

MC3425P1 T_A = 0° to +70°C, Case 626

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over and undervoltage fault conditions. This device features dedicated over and undervoltage sensing channels with independently programmable time delays. The overvoltage channel has a high current Drive Output for use in conjunction with an external SCR "Crowbar" for shutdown. The undervoltage channel input comparator has hysteresis which is externally programmable, and an open-collector output for fault indication.

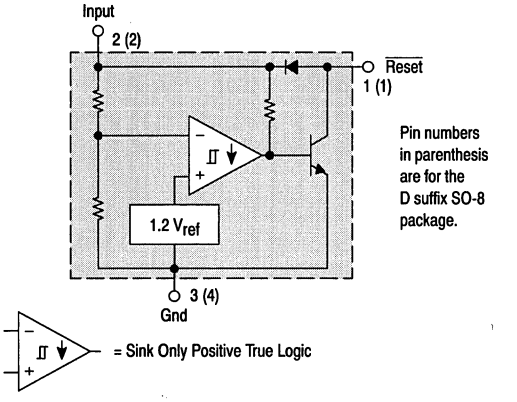


Undervoltage Sensing Circuit

MC34064P-5, D-5 T_A = 0° to +70°C, Case 29, 751
MC33064P-5, D-5 T_A = –40° to +85°C, Case 29, 751
MC34164P-3, P-5, D-3, D-5 T_A = –0° to +70°C, Case 29, 751
MC33164P-3, P-5, D-3, D-5 T_A = –40° to +85°C, Case 29, 751

The MC34064 and MC34164 are two families of undervoltage sensing circuits specifically designed for use as reset controllers in microprocessor-based systems. They offer the designer an economical solution for low voltage detection with a single external resistor. Both parts feature a trimmed bandgap reference, and a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation.

The two families of undervoltage sensing circuits taken together, cover the needs of the most commonly specified power supplies used in MCU/MPU systems. Key parameter specifications of the MC34164 family were chosen to complement the MC34064 series. The table summarizes critical parameters of both families. The MC34064 fulfills the needs of a 5.0 V ± 5% system and features a tighter hysteresis specification. The MC34164 series covers 5.0 V ± 10% and 3.0 V ± 5% power supplies with significantly lower power consumption, making them ideal for applications where extended battery life is required such as consumer products or hand held equipment.



Applications include direct monitoring of the 5.0 V MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment.

The MC34164 is specifically designed for battery powered applications where low bias current (1/25th of the MC34064's) is an important characteristic.

Undervoltage Sense/Reset Controller Features

Device	Suffix	Standard Power Supply Supported	Typical Threshold Voltage (V)	Typical Hysteresis Voltage (V)	Minimum Output Sink Current (mA)	Power Supply Input Voltage Range (V)	Maximum Quiescent Input Current	Package Type
MC34064/MC33064	P-5	5.0 V ± 5%	4.6	0.02	10	1.0 to 10	500 µA at V_{in} = 5.0 V	TO-92
	D-5							SO-8
MC34164/MC33164	P-5	5.0 V ±10%	4.3	0.09	7.0	1.0 to 12	20 µA at V_{in} = 5.0 V	TO-92
	D-5							SO-8
	P-3	3.0 V ± 5%	2.7	0.06	6.0	1.0 to 12	15 µA at V_{in} = 3.0 V	TO-92
	D-3							SO-8

Note: MC34X64 devices are specified to operate from 0° to +70°C, and MC33X64 devices operate from –40° to +85°C.

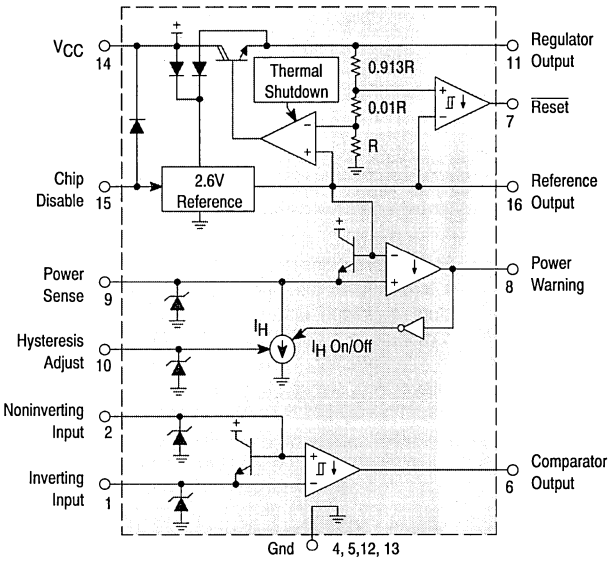
Microprocessor Voltage Regulator and Supervisory Circuit

MC34160P T_A = 0° to +70°C, Case 648C
MC33160P T_A = −40° to +85°C, Case 648C

The MC34160 Series is a voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a 5.0 V, 100 mA regulator with short circuit current limiting, pinned out 2.6 V bandgap reference, low voltage reset comparator, power warning comparator with programmable hysteresis, and an uncommitted comparator ideally suited for microprocessor line synchronization.

Additional features include a chip disable input for low standby current, and internal thermal shutdown for over temperature protection.

These devices are contained in a 16 pin dual-in-line heat tab plastic package for improved thermal conduction.

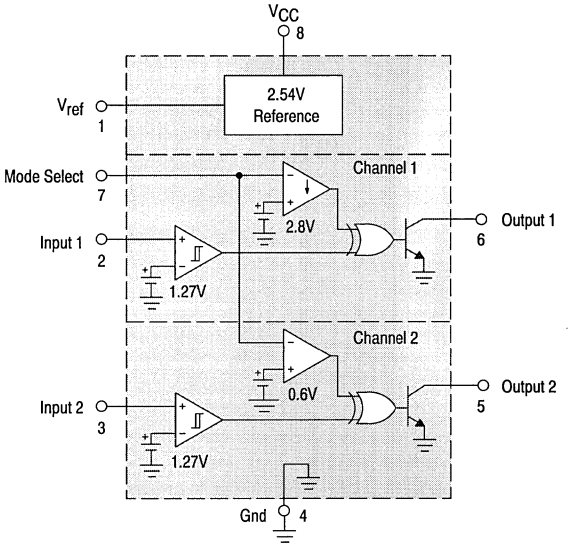


Universal Voltage Monitor

MC34161P, D T_A = 0° to +70°C, Case 626, 751
MC33161P, D T_A = −40° to +85°C, Case 626, 751

The MC34161 series of Universal Voltage Monitor ICs are capable of being used in a wide variety of voltage sensing applications. These versatile devices offer an economical solution for implementing over, under, and window detection of both positive and/or negative voltages.

The circuit consists of two comparator channels each with hysteresis, a pinned out 2.54 V reference, two open collector outputs capable of sinking in excess of 10 mA, and a "Mode Select" input for programming the functions of the two comparator channels. The devices are fully functional from 2.0 V to 40 V for positive voltage sensing and from 4.0 V to 40 V for negative voltage sensing.



MOSFET Drivers

High Speed Dual Drivers

Inverting

MC34151P, D T_A = 0° to +70°C, Case 626, 751
MC33151P, D T_A = –40° to +85°C, Case 626, 751

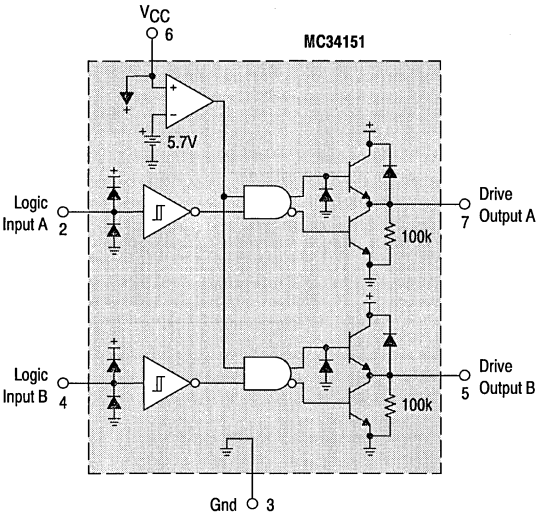
Noninverting

MC34152P, D T_A = 0° to +70°C, Case 626, 751
MC33152P, D T_A = –40° to +85°C, Case 626, 751

These two series of High Speed Dual MOSFET Driver ICs are specifically designed for applications requiring low current digital circuitry to drive large capacitive loads at high slew rates. Both series feature a unique undervoltage lockout function which puts the outputs in a defined low state in an undervoltage condition. In addition, the low on-state resistance of these bipolar drivers allows significantly higher output currents at lower supply voltages than with competing drivers using CMOS technology.

The MC34151 series is pin-compatible with the MMH0026 and DS0026 dual MOS clock drivers, and can be used as drop-in replacements to upgrade system performance. The MC34152 noninverting series is a mirror image of the inverting MC34151 series.

These devices can enhance the drive capabilities of first generation switching regulators or systems designed with CMOS/TTL logic devices. They can be used in DC-to-DC converters, motor controllers, capacitor charge pump converters, or virtually any other application requiring high speed operation of power MOSFETs.



Linear Voltage Regulators

Switching Regulator Control

*Selected voltages also available in D^2PAK as case number 936 or 936A.
#Also available with lead formed packages as case numbers 314A and 314B.

Switching Regulator Control (Continued)

Special Switching Regulator Controllers

Power Factor Correction Controllers

Power Drivers

Power Supervisory

ADDENDUM

RELATED APPLICATION NOTES

App Note	Title	Related Device
AN703	Designing Digitally-Controlled Power Supplies	**MC1466, MC1723**
AN719	A New Approach to Switching Regulators	**General**
AN1040	Mounting Techniques for Power Semiconductors	**LM317, LM337, MC7800, MC78M00, MC7900, MC78M00**
AN920	Theory and Applications of the MC34063 and μA78S40 Switching Regulator Control Circuits	**μA78S40**
AN976	A New High Performance Current-Mode Controller Teams Up with Current Sensing Power MOSFETs	**MC34129**
AN983	A Simplified Power Supply Design Using the TL494 Control Circuit	**TL494**
ANE424	50 W Current Mode Controlled Offline Switchmode Power Supply	**UC3842A, UC2842A UC3843A, UC2843A**

LM317

3

Three-Terminal Adjustable Output Positive Voltage Regulators

THREE-TERMINAL ADJUSTABLE POSITIVE VOLATGE REGULATOR

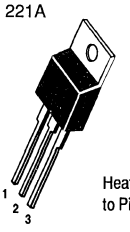
SILICON MONOLITHIC INTEGRATED CIRCUIT

The LM317 is an adjustable 3-terminal positive voltage regulator capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

The LM317 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317 can be used as a precision current regulator.

- Output Current in Excess of 1.5 A
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting Constant with Temperature
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Package
- Eliminates Stocking Many Fixed Voltages

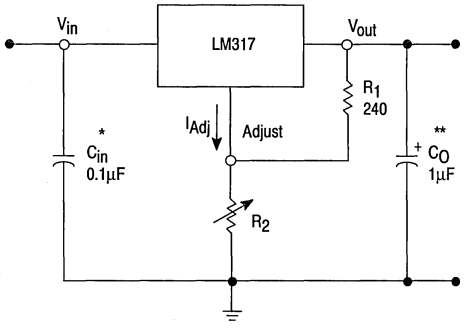
T SUFFIX
PLASTIC PACKAGE
CASE 221A



Pin 1. Adjust
2. V_{out}
3. V_{in}

Heatsink surface connected to Pin 2

STANDARD APPLICATION



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.
** = C_O is not needed for stability, however, it does improve transient response.

$$V_{out} = 1.25\ V\left(1 + \frac{R_2}{R_1}\right) + I_{Adj} R_2$$

Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications.

ORDERING INFORMATION

Device	Tested Opearting Temperature Range	Package
LM317T	T_J = 0° to +125°C	Plastic Power
LM317BT#	T_J = –40° to +125°C	Plastic Power

Automotive temperature range selections are available with special test conditions and additional tests.

Contact your local Motorola sales office for information.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature Range LM317	T_J	 0 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERICISTICS (V_I-V_O = 5.0 V; I_O = 0.5 A for K and T packages; T_J = T_{low} to T_{high} [see Note 1]; I_{max} and P_{max} per Note 2; unless otherwise noted.)

Characteristics	Figure	Symbol	LM317 Min	LM317 Typ	LM317 Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ V_I-V_O ≤ 40 V	1	Reg_{line}	—	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ I_{max} V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 5.0 0.1	 25 0.5	 mV %/V_O
Thermal Regulation (T_A = +25°C) 20 ms Pulse		—	—	0.03	0.07	%/W
Adjustment Pin Current	3	I_{Adj}	—	50	100	μA
Adjustment Pin Current Change 2.5 V ≤ V_I-V_O ≤ 40 V 10 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}	1,2	ΔI_{Adj}	—	0.2	5.0	μA
Reference Voltage 3.0 V ≤ V_I-V_O ≤ 40 V 10 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}	3	V_{ref}	1.2	1.25	1.3	V
Line Regulation (Note 3) 3.0 V ≤ V_I-V_O ≤ 40 V	1	Reg_{line}	—	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ I_{max} V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 20 0.3	 70 1.5	 mV %/V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.7	—	%/V_O
Minimum Load Current to Maintain Regulation (V_I-V_O = 40 V)	3	I_{Lmin}	—	3.5	10	mA
Maximum Output Current V_I-V_O ≤ 15 V, P_D ≤ P_{max} T Package V_I-V_O = 40 V, P_D ≤ P_{max}, T_A = 25°C T Package	3	I_{max}	 1.5 0.15	 2.2 0.4	 — —	A
RMS Noise, % of V_O T_A= 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	%/V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 4) Without C_{Adj} C_{Adj} = 10 μF	4	RR	 — 66	 65 80	 — —	dB
Long-Term Stability, T_J = T_{high} (Note 5) T_A= 25°C for Endpoint Measurements	3	S	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case T Package	—	$R_{\theta JC}$	 —	 5.0	 —	°C/W

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
2. I_{max} = 1.5 A P_{max} = 20 W
3. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
4. C_{Adj}, when used, is connected between the adjustment pin and ground.
5. Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

3

SCHEMATIC DIAGRAM

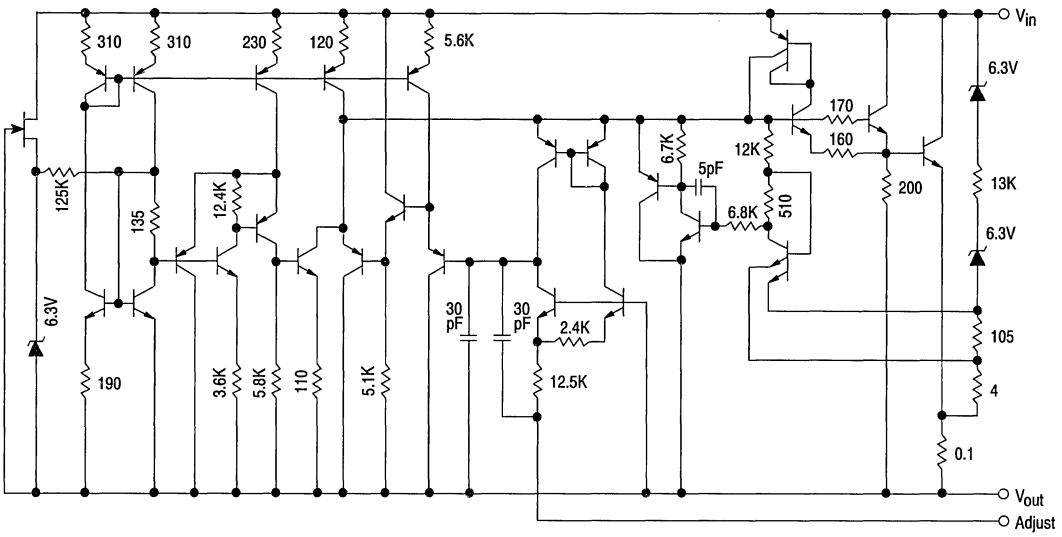


Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit

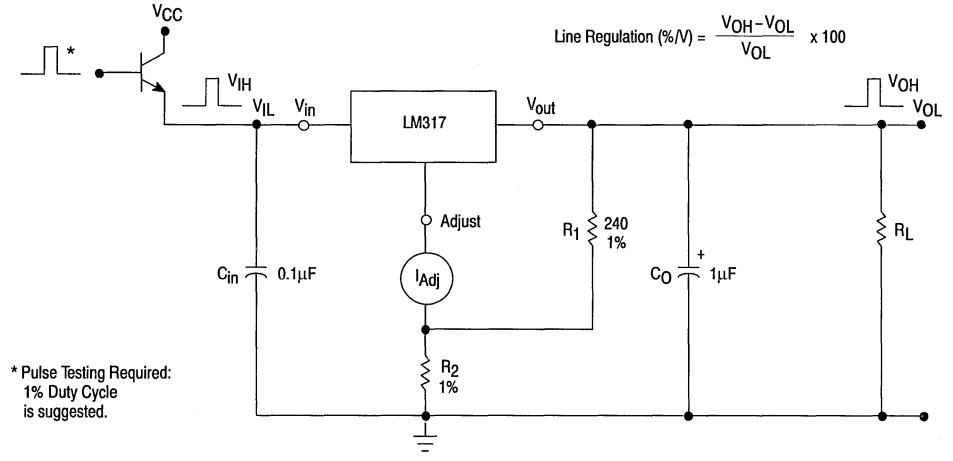
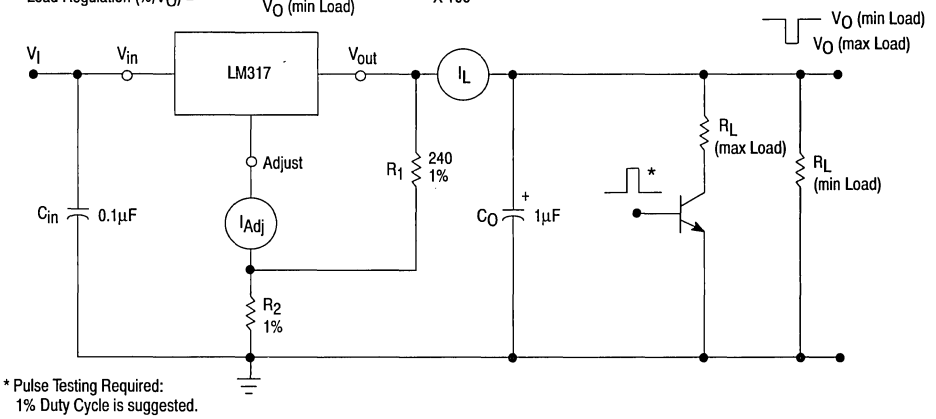


Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit

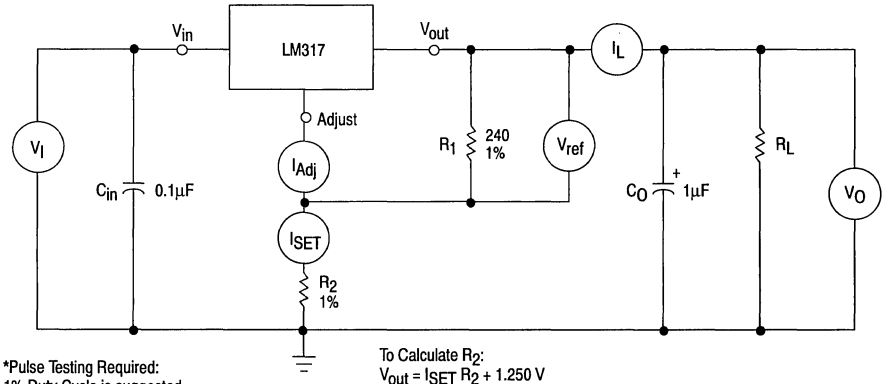
Load Regulation (mV) = V_O (min Load) − V_O (max Load)

Load Regulation (%/V_O) = $\frac{V_O \text{ (min Load)} - V_O \text{ (max Load)}}{V_O \text{ (min Load)}}$ X 100



* Pulse Testing Required:
1% Duty Cycle is suggested.

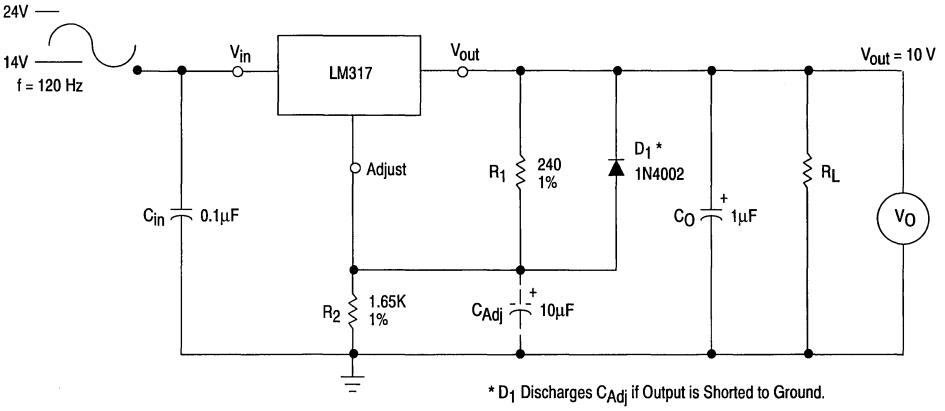
Figure 3. Standard Test Circuit



*Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate R_2:
$V_{out} = I_{SET} R_2 + 1.250$ V
Assume $I_{SET} = 5.25$ mA

Figure 4. Ripple Rejection Test Circuit



* D_1 Discharges C_{Adj} if Output is Shorted to Ground.

Figure 5. Load Regulation

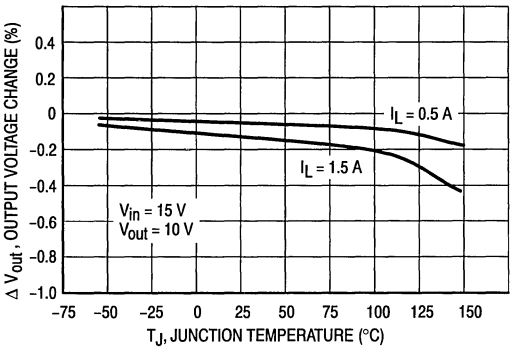


Figure 6. Current Limit

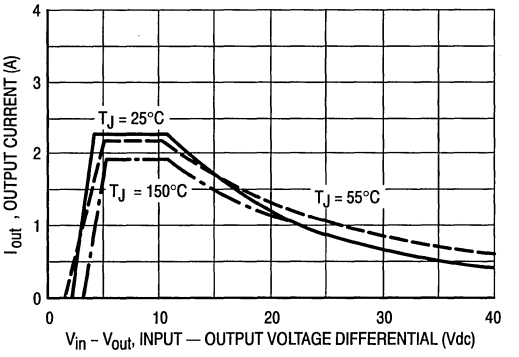


Figure 7. Adjustment Pin Current

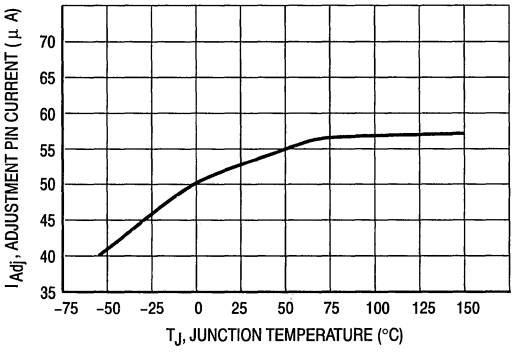


Figure 8. Dropout Voltage

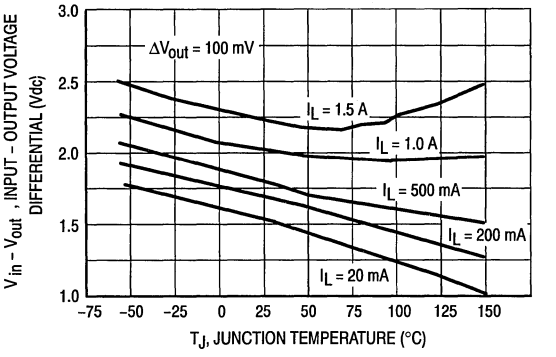


Figure 9. Temperature Stability

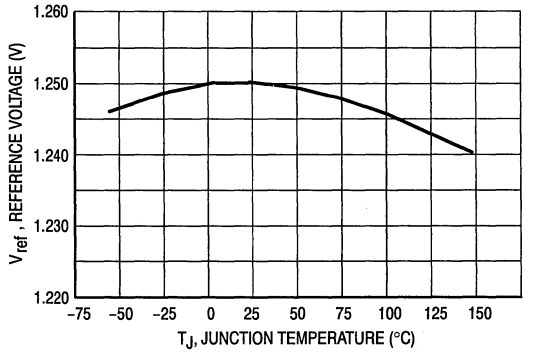


Figure 10. Minimum Operating Current

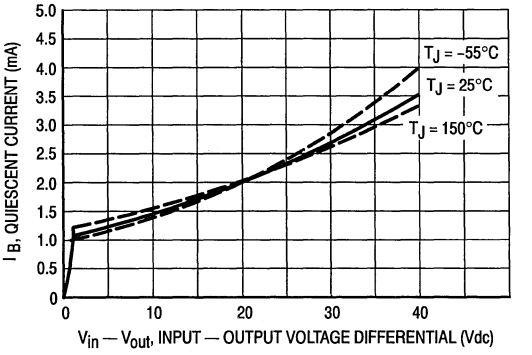


Figure 11. Ripple Rejection versus Output Voltage

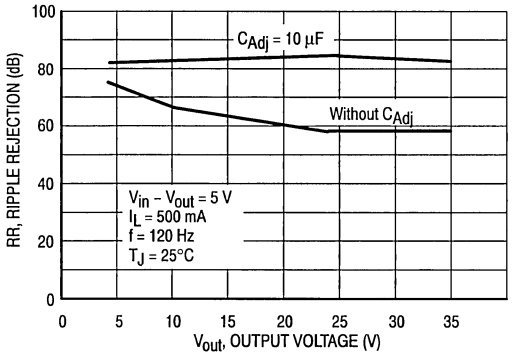


Figure 12. Ripple Rejection versus Output Current

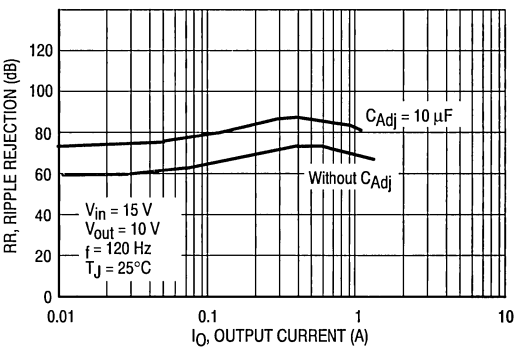


Figure 13. Ripple Rejection versus Frequency

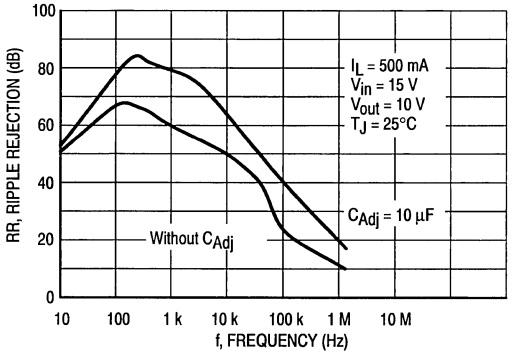


Figure 14. Output Impedance

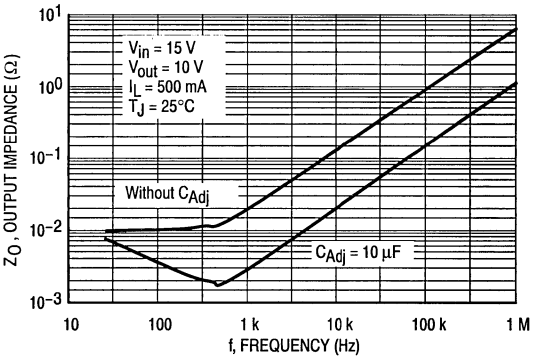


Figure 15. Line Transient Response

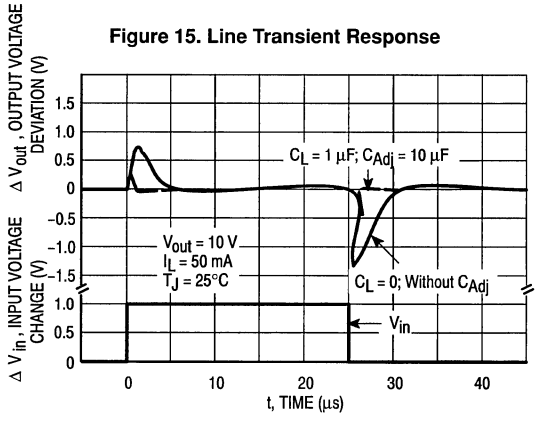
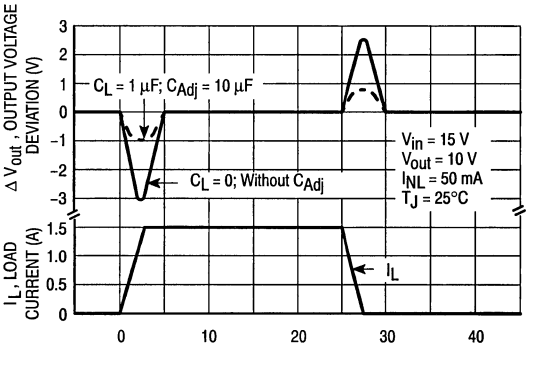


Figure 16. Load Transient Response



APPLICATIONS INFORMATION

Basic Circuit Operation

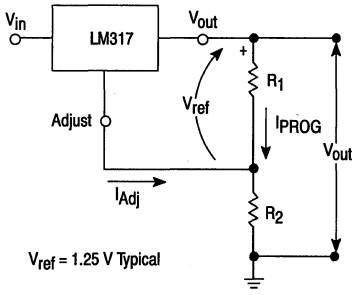
The LM317 is a 3-terminal floating regulator. In operation, the LM317 develops and maintains a nominal 1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM317 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



Load Regulation

The LM317 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM317 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM317 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values (C_O > 25 μF, C_{Adj} > 10 μF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D1 and D2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes

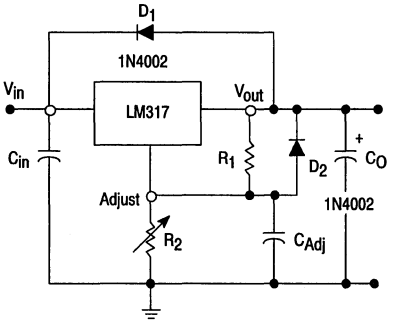
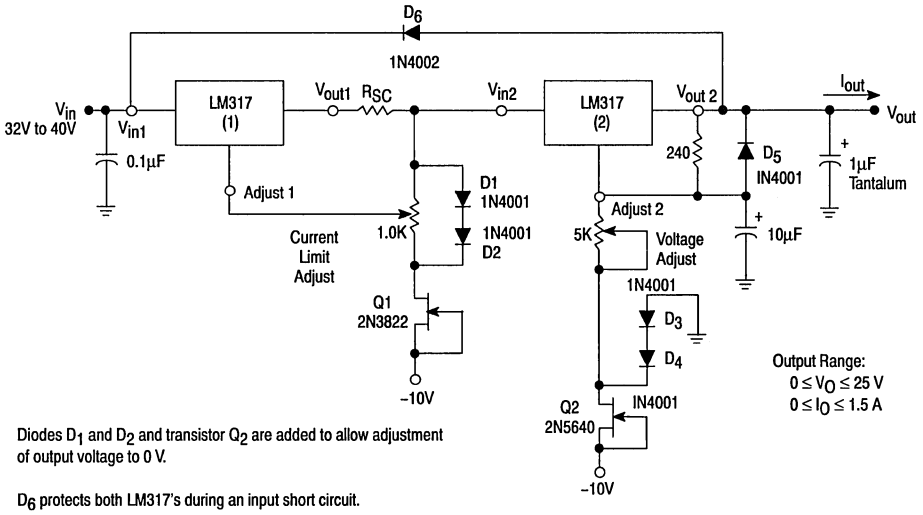


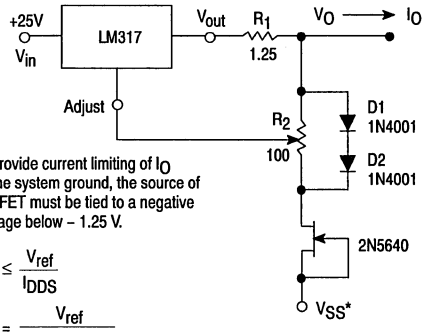
Figure 19. "Laboratory" Power Supply with Adjustable Current Limit and Output Voltage



Diodes D_1 and D_2 and transistor Q_2 are added to allow adjustment of output voltage to 0 V.

D_6 protects both LM317's during an input short circuit.

Figure 20. Adjustable Current Limiter



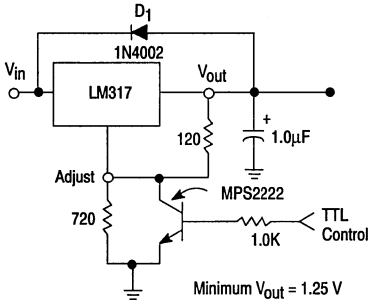
* To provide current limiting of I_O to the system ground, the source of the FET must be tied to a negative voltage below – 1.25 V.

$$R_2 \leq \frac{V_{ref}}{I_{DDS}}$$

$$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$$

$V_O < BV_{DSS} + 1.25\ V + V_{SS}$
$I_{Lmin} - I_{DSS} < I_O < 1.5\ A$
As shown $O < I_O < 1.0\ A$

Figure 21. 5.0 V Electronic Shutdown Regulator



D_1 protects the device during an input short circuit

Figure 22. Slow Turn-On Regulator

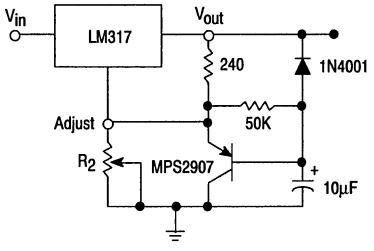
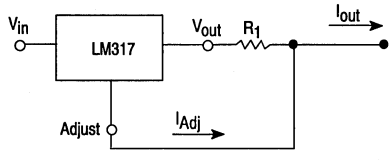


Figure 23. Current Regulator



$$I_{out} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj}$$

$$\cong \frac{1.25\ V}{R_1}$$

$10\ mA \leq I_{out} \leq 1.5\ A$

LM317L

3

Three-Terminal Adjustable Output Positive Voltage Regulator

LOW CURRENT THREE-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

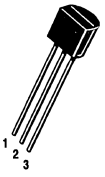
The LM317L is an adjustable 3-terminal positive voltage regulator capable of supplying in excess of 100 mA over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof.

The LM317L serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317L can be used as a precision current regulator.

- Output Current in Excess of 100 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Package
- Eliminates Stocking Many Fixed Voltages

Z SUFFIX
PLASTIC PACKAGE
CASE 29

PIN 1. Adjust
2. V_{out}
3. V_{in}

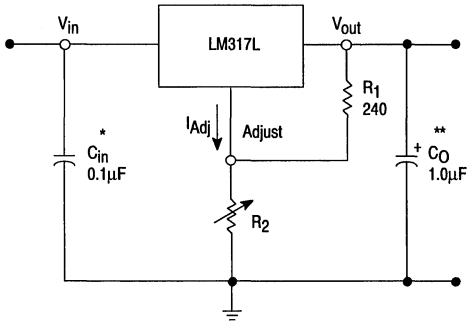


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP-8*)

PIN 1. V_{in}
2. V_{out}
3. V_{out}
4. Adjust
5. N.C.
6. V_{out}
7. V_{out}
8. N.C.

SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

Standard Application



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.
** = C_O is not needed for stability, however, it does improve transient response.

$$V_{out} = 1.25\ V\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}R_2$$

Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications.

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM317LD	T_J = 0° to +125°C	SOP-8
LM317LZ		Plastic
LM317LBD	T_J = –40° to +150°C	SOP-8
LM317LBZ		Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature Range	T_J	0 to +125 –40 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERICISTICS (V_I-V_O = 5.0 V; I_O = 40 mA; T_J = T_{low} to T_{high} (see Note 1); I_{max} and P_{max} per Note 2; unless otherwise noted.)

Characteristics	Figure	Symbol	LM317L, LB Min	LM317L, LB Typ	LM317L, LB Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ V_I – V_O ≤ 40 V	1	Reg_{line}	—	0.01	0.04	%/V
Load Regulation (Note 3), T_A = 25°C 10 mA ≤ I_O ≤ I_{max} — LM317L V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 5.0 0.1	 25 0.5	 mV % V_O
Adjustment Pin Current	3	I_{Adj}	—	50	100	µA
Adjustment Pin Current Change 2.5 V ≤ V_I – V_O ≤ 40 V, P_D ≤ P_{max} 10 mA ≤ I_O ≤ I_{max} — LM317L	1, 2	ΔI_{Adj}	—	0.2	5.0	µA
Reference Voltage 3.0 V ≤ V_I – V_O ≤ 40 V, P_D ≤ P_{max} 10 mA ≤ I_O ≤ I_{max} — LM317L	3	V_{ref}	1.20	1.25	1.30	V
Line Regulation (Note 3) 3.0 V ≤ V_I – V_O ≤ 40 V	1	Reg_{line}	—	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ I_{max} — LM317L V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.7	—	% V_O
Minimum Load Current to Maintain Regulation (V_I – V_O = 40 V)	3	I_{Lmin}	—	3.5	10	mA
Maximum Output Current V_I – V_O ≤ 6.25 V, P_D ≤ P_{max}, Z Package V_I – V_O ≤ 40 V, P_D ≤ P_{max}, T_A = 25°C, Z Package	3	I_{max}	 100 —	 200 20	 — —	mA
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	% V_O
Ripple Rejection (Note 4) V_O = 1.2 V, f = 120 Hz C_{Adj} = 10 µF V_O = 10.0 V	4	RR	 60 —	 80 80	 — —	dB
Long Term Stability, T_J = T_{high} (Note 5) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case Z Package	—	$R_{\Theta JC}$	—	83	—	°C/W
Thermal Resistance Junction to Air Z Package	—	$R_{\Theta JA}$	—	160	—	°C/W

NOTES: 1. T_{low} to T_{high} = 0° to +125°C for LM317L –40° to +125°C for LM317LB
2. I_{max} = 100 mA P_{max} = 625 mW
3. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
4. C_{Adj}, when used, is connected between the adjustment pin and ground.
5. Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

3

Schematic Diagram

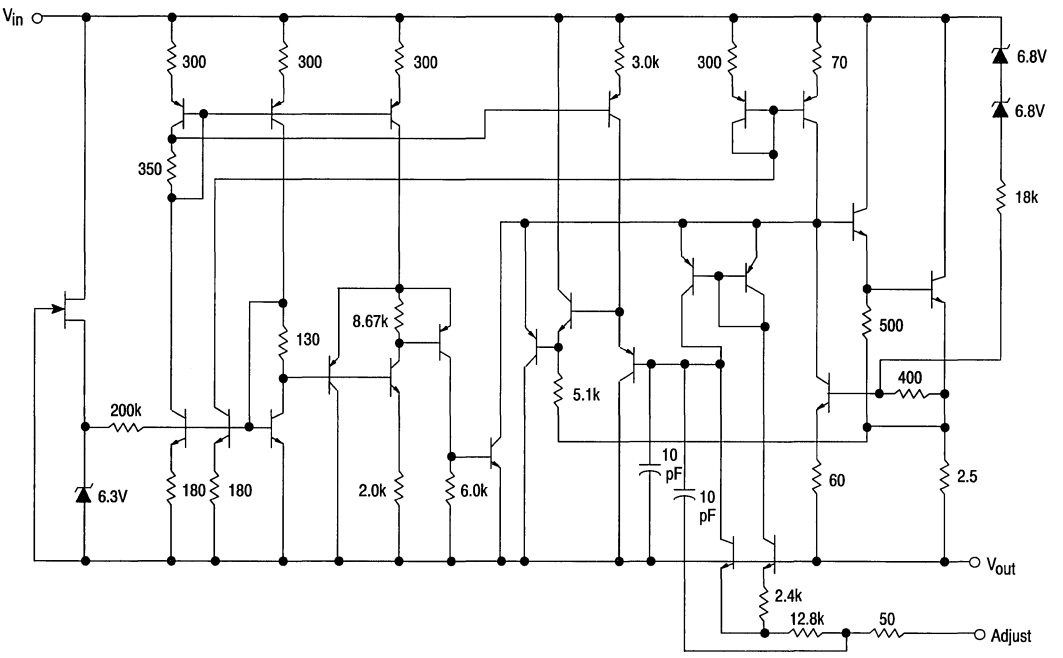


Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit

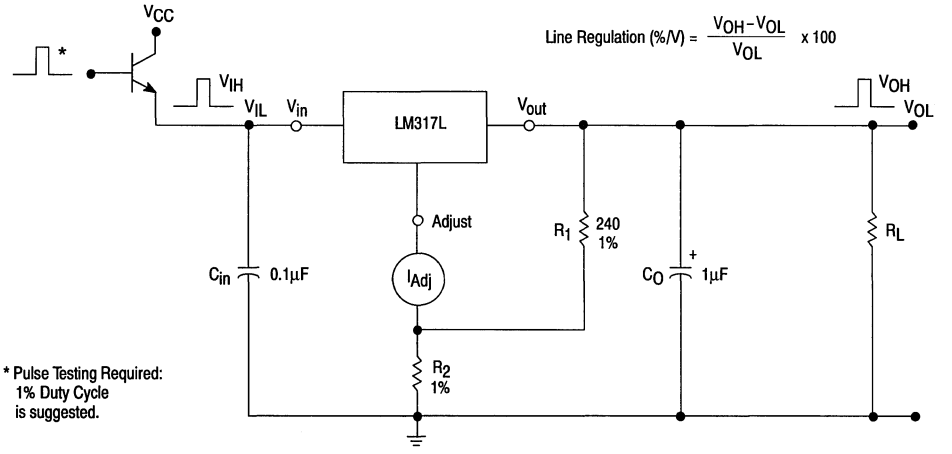
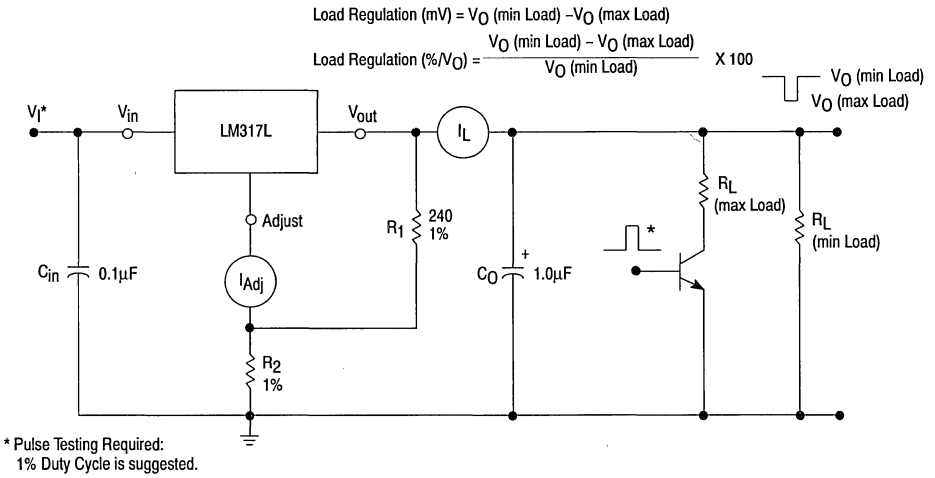
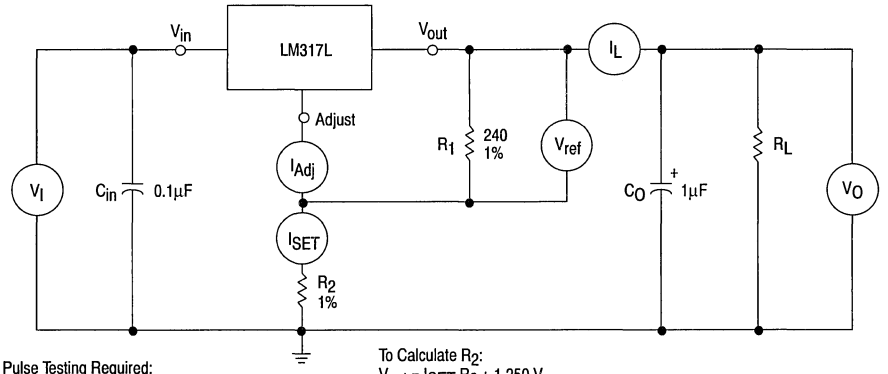


Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit



* Pulse Testing Required:
1% Duty Cycle is suggested.

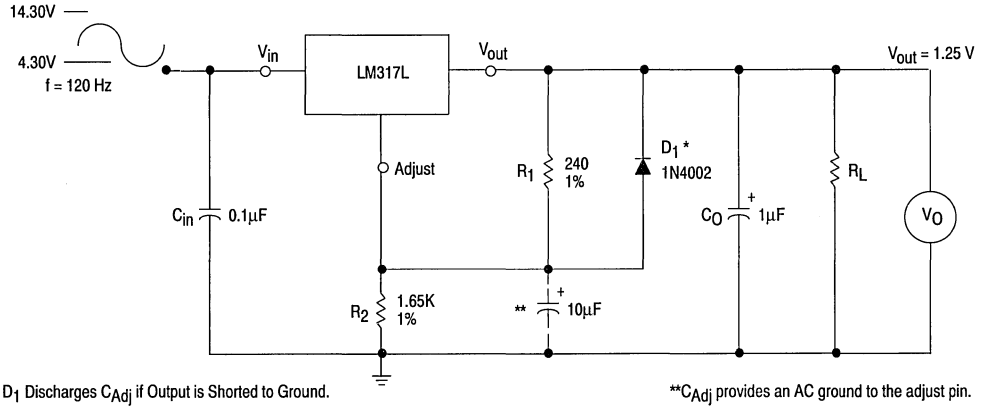
Figure 3. Standard Test Circuit



Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate R_2:
$V_{out} = I_{SET} R_2 + 1.250$ V
Assume $I_{SET} = 5.25$ mA

Figure 4. Ripple Rejection Test Circuit



* D_1 Discharges C_{Adj} if Output is Shorted to Ground.

**C_{Adj} provides an AC ground to the adjust pin.

Figure 5. Load Regulation

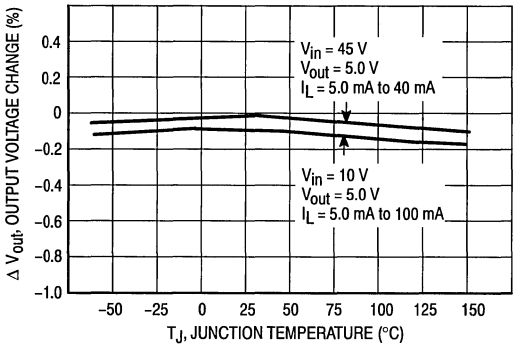


Figure 6. Ripple Rejection

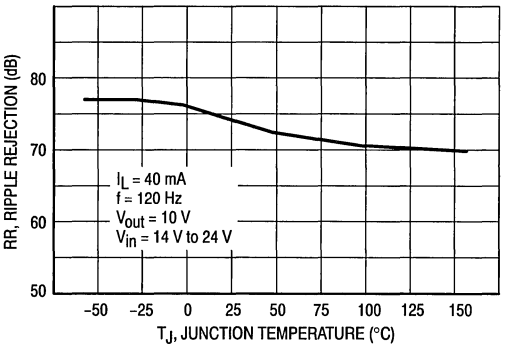


Figure 7. Current Limit

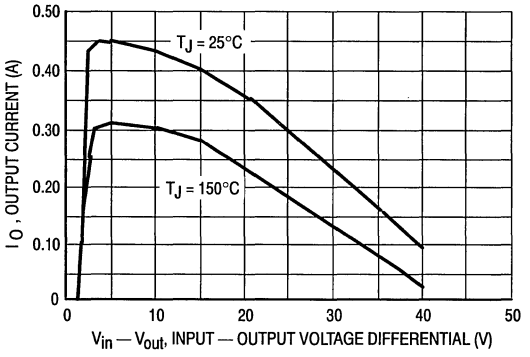


Figure 8. Dropout Voltage

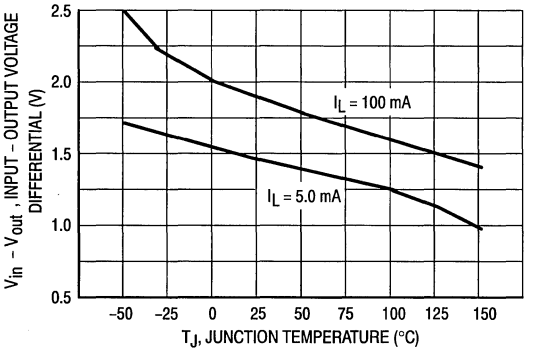


Figure 9. Minimum Operating Current

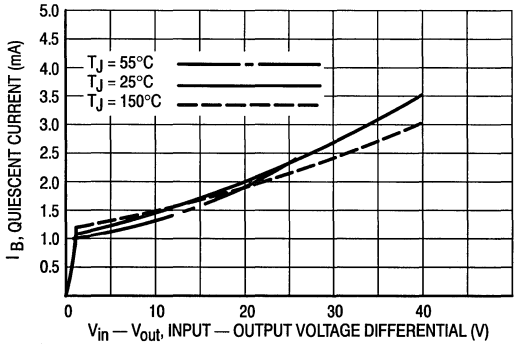


Figure 10. Ripple Rejection versus Frequency

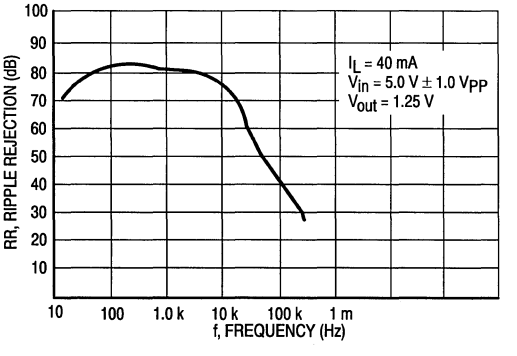


Figure 11. Temperature Stability

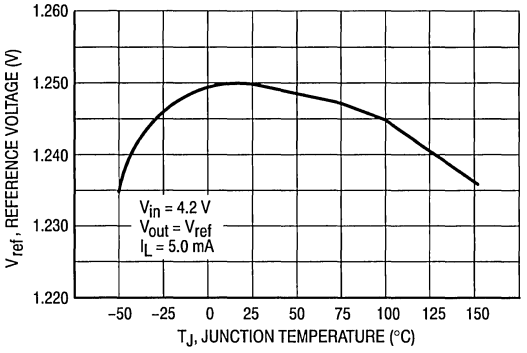


Figure 12. Adjustment Pin Current

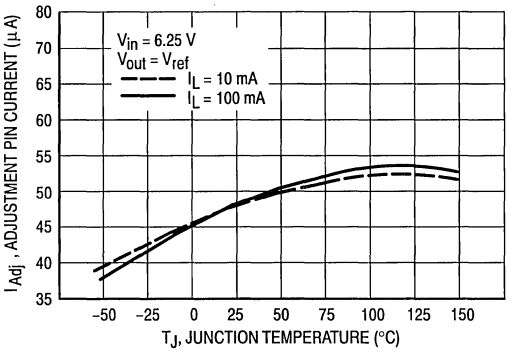


Figure 13. Line Regulation

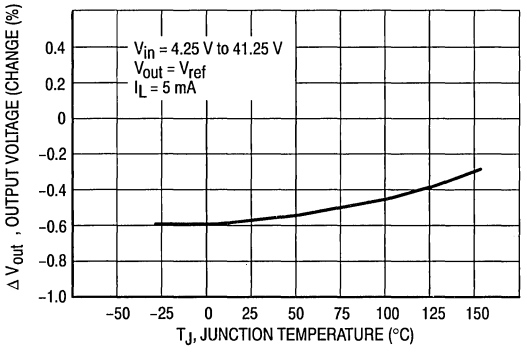


Figure 14. Output Noise

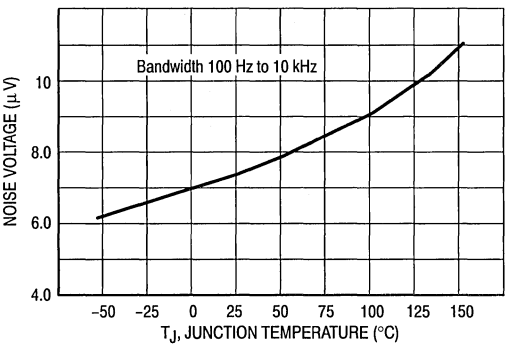


Figure 15. Line Transient Response

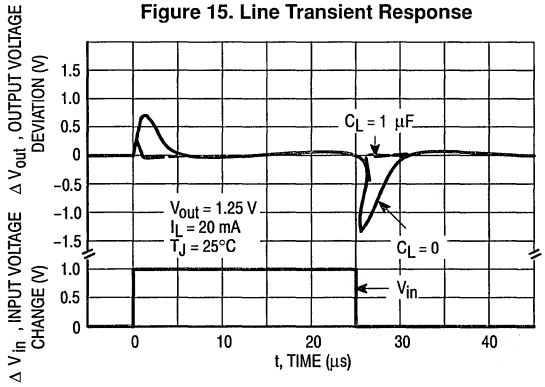
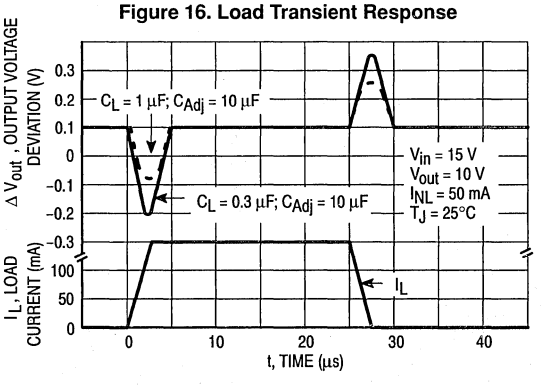


Figure 16. Load Transient Response



APPLICATIONS INFORMATION

Basic Circuit Operation

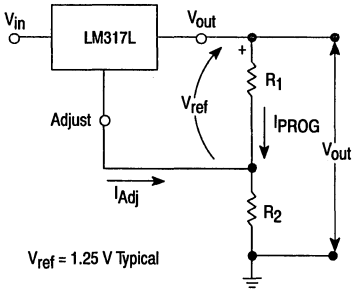
The LM317L is a 3-terminal floating regulator. In operation, the LM317L develops and maintains a nominal 1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 13), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM317L was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317L is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



Load Regulation

The LM317L is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 μF disc or 1.0 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM317L is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 14 shows the LM317L with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values (C_O > 10 μF, C_{Adj} > 5.0 μF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D1 and D2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes

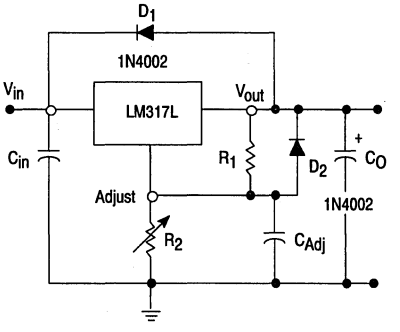
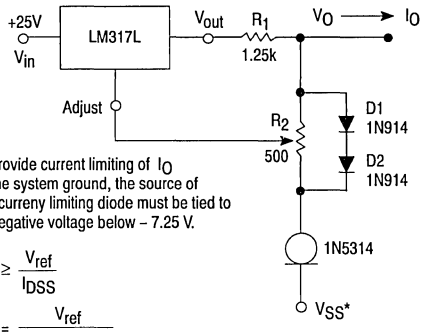


Figure 19. Adjustable Current Limiter



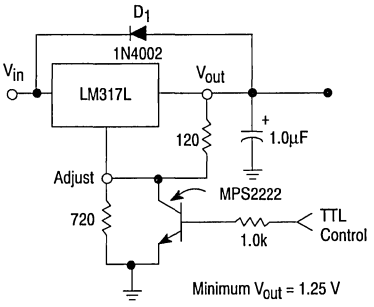
* To provide current limiting of I_O to the system ground, the source of the curreny limiting diode must be tied to a negative voltage below – 7.25 V.

$$R_2 \geq \frac{V_{ref}}{I_{DSS}}$$

$$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$$

$V_O < P_{OV} + 1.25\ V + V_{SS}$
$I_{Lmin} - I_P < I_O < 100\ mA - I_P$
As shown $O < I_O < 95\ mA$

Figure 20. 5 V Electronic Shutdown Regulator



D_1 protects the device during an input short circuit.

Figure 21. Slow Turn-On Regulator

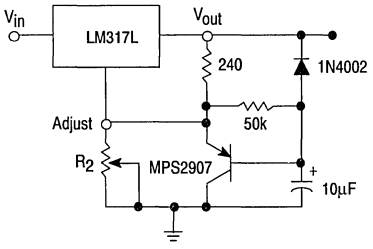
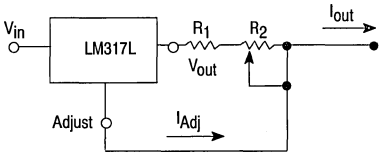


Figure 22. Current Regulator



$$I_{outmax} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj} \cong \frac{1.25\ V}{R_1}$$

$$I_{outmax} = \left(\frac{V_{ref}}{R_1 + R_2}\right) + I_{Adj} \cong \frac{1.25\ V}{R_1 + R_2}$$

$5.0\ mA < I_{out} < 100\ mA$

LM323, LM323A

3

Positive Voltage Regulators

The LM323,A are monolithic integrated circuits which supply a fixed positive 5.0 V output with a load driving capability in excess of 3.0 A. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. An improved device with superior electrical characteristics and a 2% output voltage tolerance is available with an A-suffix (LM323A). These regulators are offered with a 0° to +125°C temperature range in a low cost plastic power package.

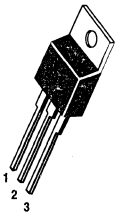
Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. These devices can be used with a series pass transistor to supply up to 15 A at 5.0 V.

- Output Current in Excess of 3.0 A
- Available with 2% Output Voltage Tolerance
- No external Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Thermal Regulation and Ripple Rejection Have Specified Limits

3-AMPERE, 5 VOLT POSITIVE VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

T SUFFIX
PLASTIC PACKAGE
CASE 221A



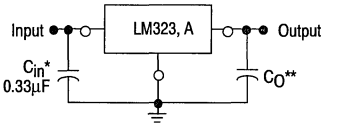
PIN 1. Input
2. Ground
3. Output

Heatsink surface connected to Pin 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	20	Vdc
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Lead Temperature (Soldering, 10 s)	T_{solder}	300	°C

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.5 V above the output voltage even during the low point on the input ripple voltage.

*= C_{in} is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details.)

**= C_O is not needed for stability; however, it does improve transient response.

ORDERING INFORMATION

Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
LM323T	4%	0° to +125°C	Plastic Power
LM323AT	2%		

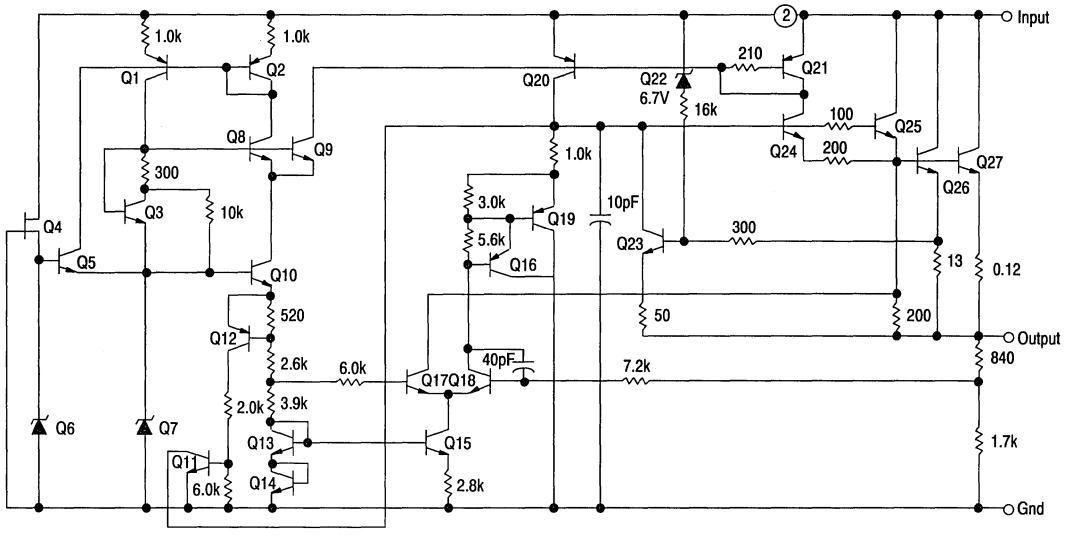
ELECTRICAL CHARACTERICISTICS ($T_J = T_{low}$ to T_{high} (see Note 1), unless otherwise noted.)

Characteristics	Symbol	LM323A			LM323			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (V_{in} = 7.5 V, 0 ≤ I_{out} ≤ 3.0 A, T_J = 25°C)	V_O	4.9	5.0	5.1	4.8	5.0	5.2	V
Output Voltage (7.5 V ≤ V_{in} ≤ 15 V, 0 ≤ I_{out} ≤ 3.0 A, P ≤ P_{max} [Note 2])	V_O	4.8	5.0	5.2	4.75	5.0	5.25	V
Line Regulation (7.5 V ≤ V_{in} ≤ 15 V, T_J = 25°C) (Note 3)	Reg_{line}	—	1.0	15	—	1.0	25	mV
Load Regulation (V_{in} = 7.5 V, 0 ≤ I_{out} ≤ 3.0 A, T_J = 25°C) (Note 3)	Reg_{load}	—	10	50	—	10	100	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = 25°C)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	%V_O/W
Quiescent Current (7.5 V ≤ V_{in} ≤ 15 V, 0 ≤ I_{out} ≤ 3.0 A)	I_B	—	3.5	10	—	3.5	20	mA
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = 25°C)	V_N	—	40	—	—	40	—	μV_{rms}
Ripple Rejection (8.0 V ≤ V_{in} ≤ 18 V, I_{out} = 2.0A, f = 120 Hz, T_J = 25°C)	RR	66	75	—	62	75	—	dB
Short Circuit Current Limit (V_{in} = 15 V, T_J = 25°C) (V_{in} = 7.5 V, T_J = 25°C)	I_{SC}	— —	4.5 5.5	— —	— —	4.5 5.5	— —	A
Long Term Stability	S	—	—	35	—	—	35	mV
Thermal Resistance Junction to Case (Note 4)	$R_{\Theta JC}$	—	2.0	—	—	2.0	—	°C/W

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
2. Although power dissipation is internally limited, specifications apply only for P ≤ P_{max} = 25 W.
3. Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width ≤ 1.0 ms and a duty cycle ≤ 5%.
4. Without a heatsink, the termal resistance ($R_{\theta JA}$ is 65°C/W). With a heatsink, the effective thermal resistance can approach the specified values of 2.0°C/W, depending on the efficiency of the heatsink.

3

Schematic Diagram



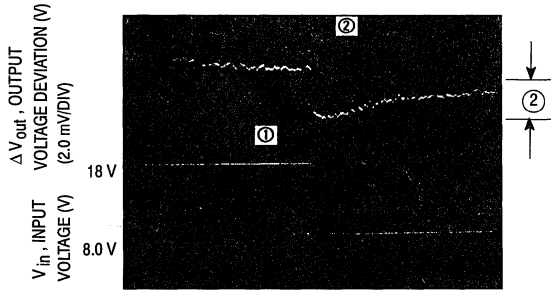
VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 µs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical LM323A to a 20 W input pulse. The variation of the output voltage due to line regulation is labeled À and the thermal regulation component is labeled Á. Figure 2 shows the load and thermal regulation response of a typical LM323A to a 20 W load pulse. The output voltage variation due to load regulation is labeled À and the thermal regulation component is labeled Á.

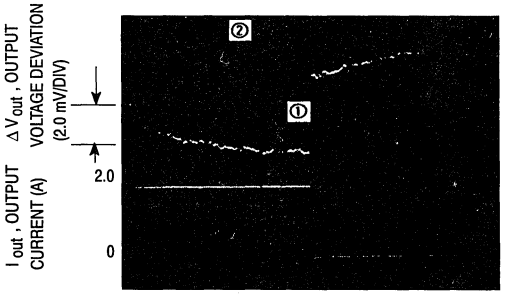
Figure 1. Line and Thermal Regulation



V_{out} = 5.0 V
V_{in} = 8.0 V → 18 V → 8.0 V
I_{out} = 2.0 A

① = Reg_{line} = 2.4 mV
② = Reg_{therm} = 0.0015% V_O/W

Figure 2. Load and Thermal Regulation



V_{out} = 5.0 V
V_{in} = 15 V
I_{out} = 0 A → 2.0 A → 0 A

① = Reg_{line} = 5.4 mV
② = Reg_{therm} = 0.0015% V_O/W

Figure 3. Temperature Stability

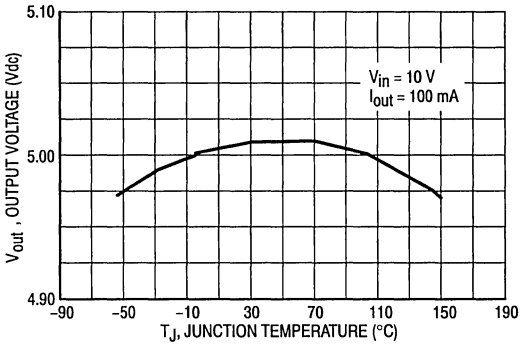


Figure 4. Output Impedance

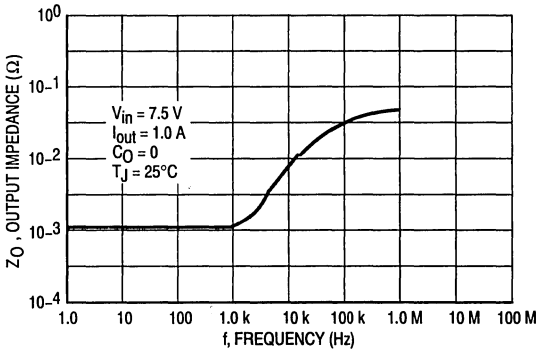


Figure 5. Ripple Rejection versus Frequency

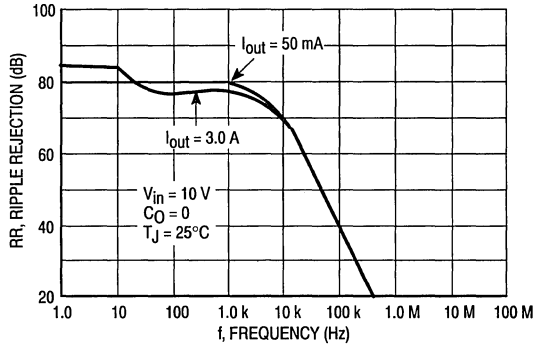


Figure 6. Ripple Rejection versus Output Current

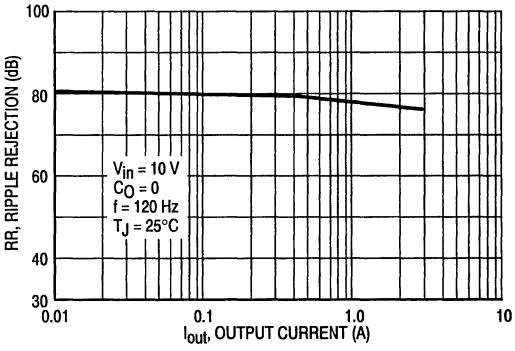


Figure 7. Quiescent Current versus Input Voltage

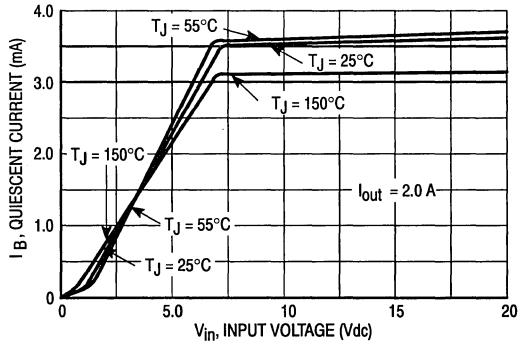
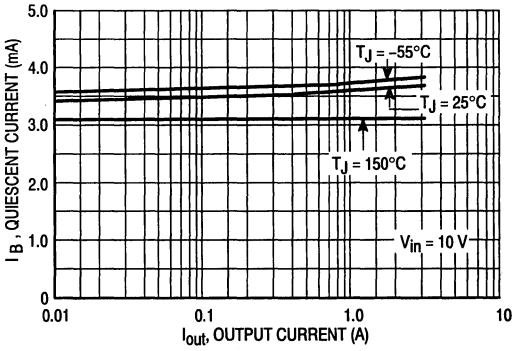


Figure 8. Quiescent Current versus Output Current



3

Figure 9. Dropout Voltage

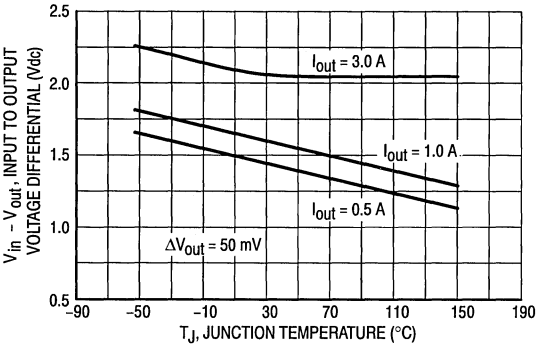


Figure 10. Short Circuit Current

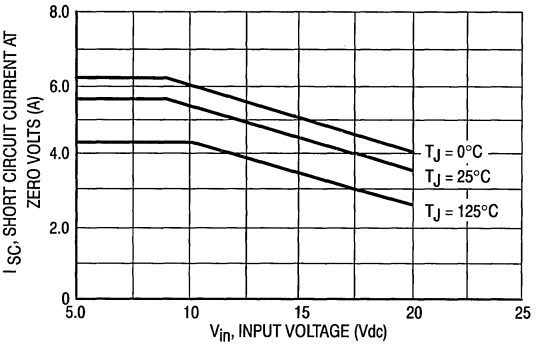


Figure 11. Line Transient Response

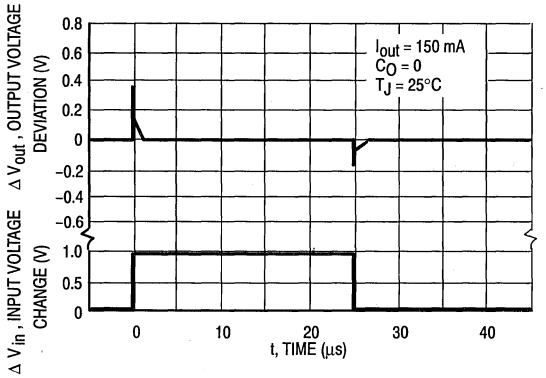
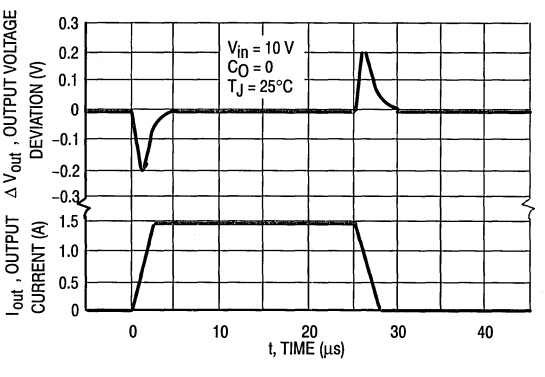


Figure 12. Load Transient Response



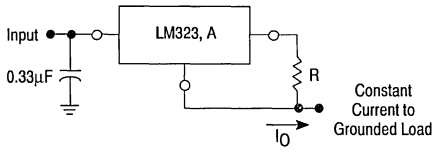
APPLICATIONS INFORMATION

Design Considerations

The LM323,A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 13. Current Regulator



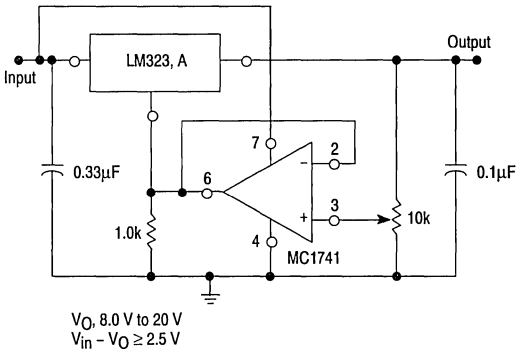
The LM323,A regulator can also be used as a current source when connected as above. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

$\Delta I_B \cong 0.7$ mA over line, load and temperature changes
$I_B \cong 3.5$ mA

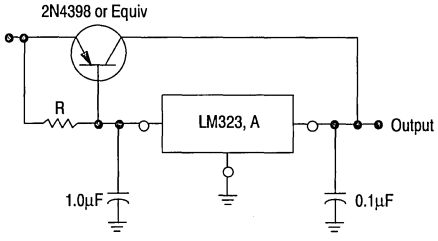
For example, a 2 A current source would require R to be a 2.5 Ω, 15 W resistor and the output voltage compliance would be the input voltage less 7.5 V.

Figure 14. Adjustable Output Regulator



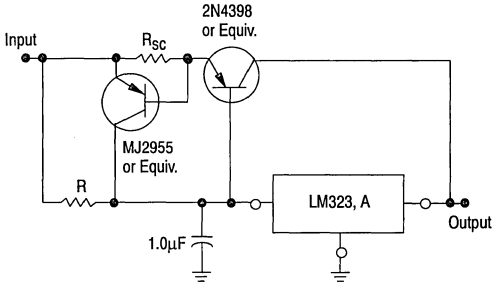
The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 V greater than the regulator voltage.

Figure 15. Current Boost Regulator



The LM323, A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 A. Resistor R in conjuction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input-output differential voltage minimum is increased by the V_{BE} of the pass transistor.

Figure 16. Current Boost With Short Circuit Protection



The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the shrot circuit current of the three-terminal regulator. Therefore, an eight-ampere power transistor is specified.

LM337

3

Three-Terminal Adjustable Output Negative Voltage Regulator

THREE-TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATOR

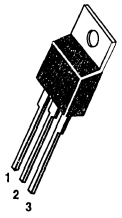
SILICON MONOLITHIC INTEGRATED CIRCUIT

The LM337 is an adjustable 3-terminal negative voltage regulator capable of supplying in excess of 1.5 A over an output voltage range of –1.2 V to –37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

The LM337 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator; or, by connecting a fixed resistor between the adjustment and output, the LM337 can be used as a precision current regulator.

- Output Current in Excess of 1.5 A
- Output Adjustable Between –1.2 V and –37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current-Limiting Constant with Temperature
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Package
- Eliminates Stocking Many Fixed Voltages

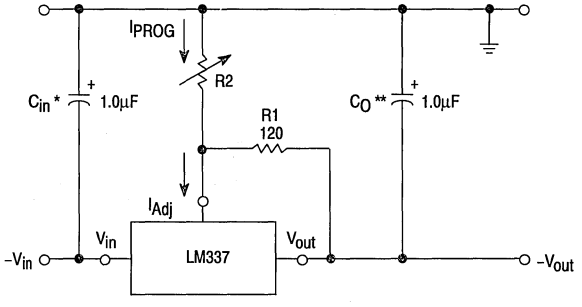
T SUFFIX
PLASTIC PACKAGE
CASE 221A



Pin 1. Adjust
2. V_{in}
3. V_{out}

Heatsink surface connected to Pin 2

Standard Application



*C_{in} is required if regulator is located more than 4 inches from power supply filter. A 1.0 µF solid tantalum or 10 µF aluminum electrolytic is recommended.

**C_O is necessary for stability. A 1.0 µF solid tantalum or 10 µF aluminum electrolytic is recommeded.

$$V_{out} = -1.25\ V\left(1 + \frac{R2}{R1}\right)$$

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM337T	T_J = 0° to +125°C	Plastic Power
LM337BT#	T_J = –40° to +150°C	Plastic Power

Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERICISTICS ($|V_I - V_O| = 5.0$ V, $I_O = 0.5$ A for T package; $T_J = T_{low}$ to T_{high} [see Note 1], I_{max} and P_{max} per Note 2, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3) $T_A = 25°C$, 3.0 V ≤ $\|V_I–V_O\|$ ≤ 40 V	1	Reg_{line}	—	0.01	0.04	%/V
Load Regulation (Note 3) $T_A = 25°C$, 10 mA ≤ I_O ≤ I_{max} $\|V_O\|$ ≤ 5.0V $\|V_O\|$ ≥ 5.0V	2	Reg_{load}	 — —	 15 0.3	 50 1.0	 mV % V_O
Thermal Regulation 10 ms Pulse, $T_A = 25°C$	—	Reg_{therm}	—	0.003	0.04	% V_O/W
Adjustment Pin Current	3	I_{Adj}	—	65	100	μA
Adjustment Pin Current Change 2.5 V ≤ $\|V_I–V_O\|$ ≤ 40 V 10 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}, $T_A = 25°C$	1, 2	ΔI_{Adj}	—	2.0	5.0	μA
Reference Voltage $T_A = +25°C$, 3.0 V ≤ $\|V_I–V_O\|$ ≤ 40 V, 10 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}, $T_J = T_{low}$ to T_{high}	3	V_{ref}	−1.213 −1.20	−1.250 −1.25	−1.287 −1.30	V
Line Regulation (Note 3) 3.0 V ≤ $\|V_I–V_O\|$ ≤ 40 V	1	Reg_{line}	—	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ I_{max} $\|V_O\|$ ≤ 5.0 V $\|V_O\|$ ≥ 5.0 V	2	Reg_{load}	 — —	 20 0.3	 70 1.5	 mV % V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.6	—	% V_O
Minimum Load Current to Maintain Regulation ($\|V_I–V_O\|$ ≤ 10 V) ($\|V_I–V_O\|$ ≤ 40 V)	3	I_{Lmin}	 — —	 1.5 2.5	 6.0 10	mA
Maximum Output Current $\|V_I–V_O\|$ ≤ 15 V, P_D ≤ P_{max} T Package $\|V_I–V_O\|$ ≤ 40 V, P_D ≤ P_{max}, $T_J = 25°C$ T Package	3	I_{max}	 — —	 1.5 0.15	 2.2 0.4	A
RMS Noise, % of V_O $T_A = 25°C$, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	% V_O
Ripple Rejection, V_O = −10 V, f = 120 Hz (Note 4) Without C_{Adj} C_{Adj} = 10 μF	4	RR	 — 66	 60 77	 — —	dB
Long-Term Stability, $T_J = T_{high}$ (Note 5) $T_A = 25°C$ for Endpoint Measurements	3	S	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case T Package	—	$R_{\theta JC}$	—	4.0	—	°C/W

NOTES:
1. T_{low} to T_{high} = 0° to +125°C
2. I_{max} = 1.5 A
P_{max} = 20 W
3. Load and line regulation are specified at constant junction temperature. Pulse testing with a low duty cycle is used. Change in V_O because of heating effects is covered under the Thermal Regulation specification.
4. C_{Adj}, when used, is connected between the adjustment pin and ground.
5. Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Power dissipation within an IC voltage regulator produces a temperature gradient on the die, affecting individual IC components on the die. These effects can be minimized by proper integrated circuit design and layout techniques. Thermal Regulation is the effect of these temperature gradients on the output voltage and is expressed in percentage of output change per watt of power change in a specified time.

3

Schematic Diagram

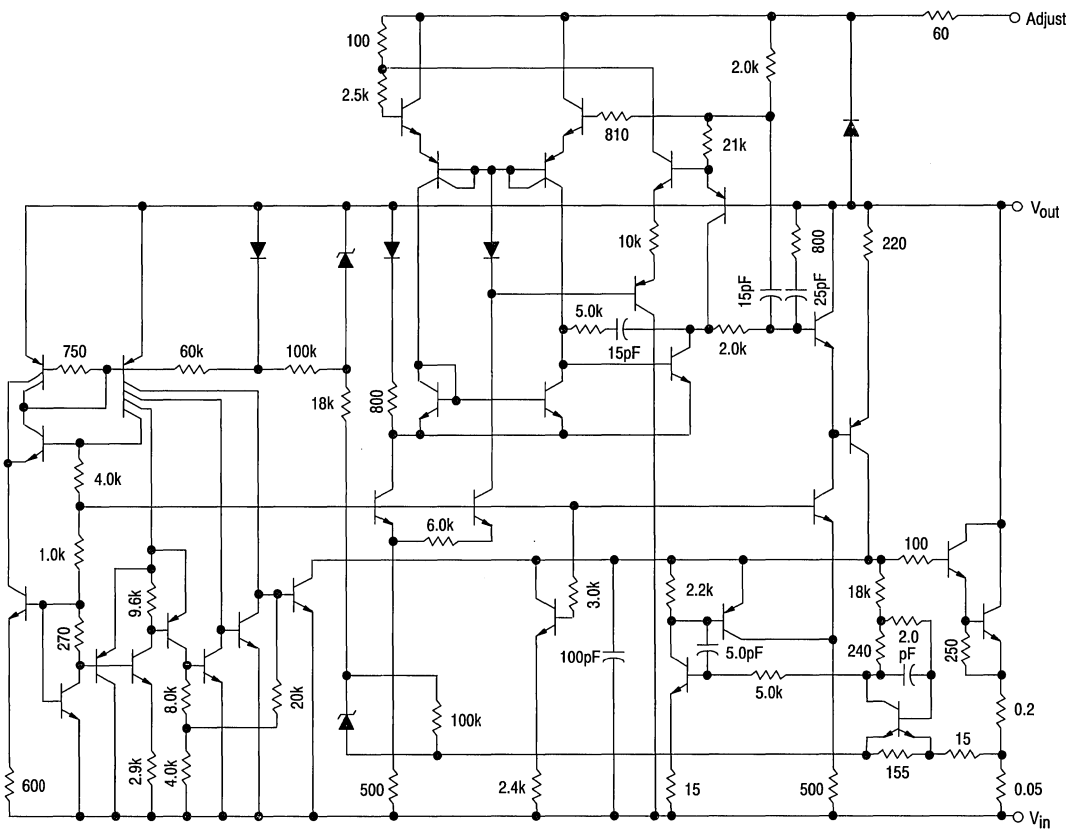


Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit

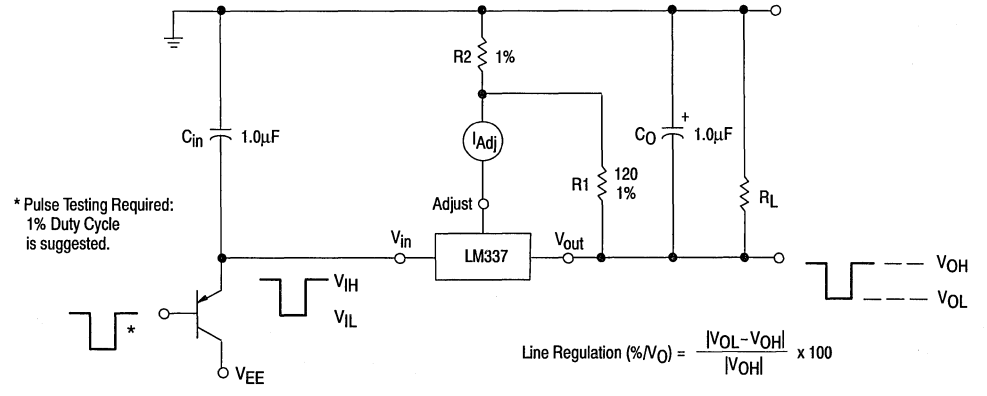
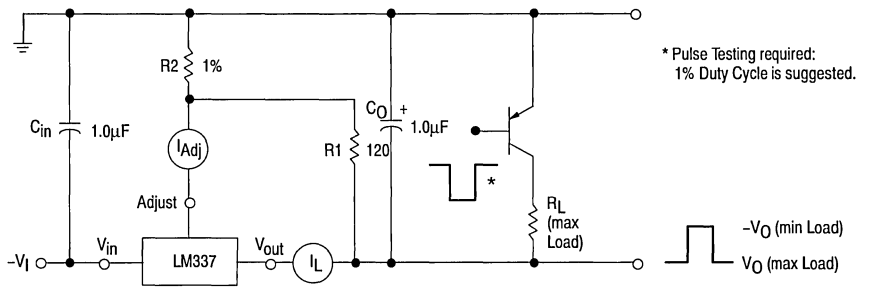


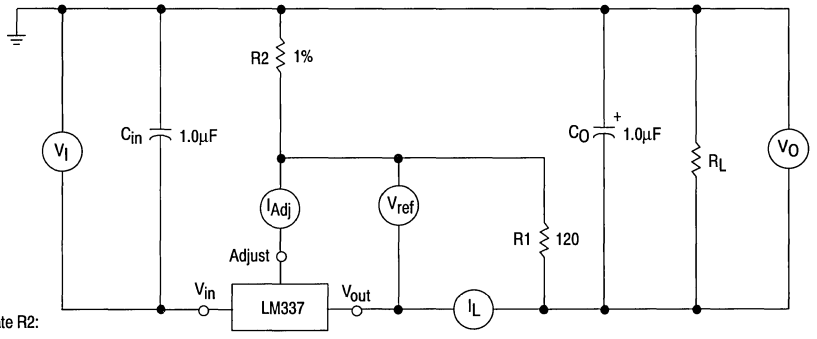
Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit



Load Regulation (mV) = V_O (min Load) − V_O (max Load)

Load Regulation (%/V_O) = $\frac{V_O \text{ (min Load)} - V_O \text{ (max Load)}}{V_O \text{ (min Load)}}$ x 100

Figure 3. Standard Test Circuit



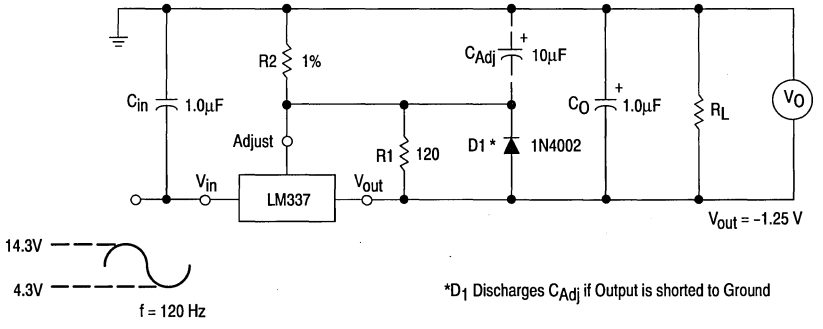
To Calculate R2:

$R2 = \left(\frac{V_O}{V_{ref}} - 1\right) R_1$

This assumes I_{Adj} is neglible.

Pulse Testing Required, 1% Duty Cycle is suggested.

Figure 4. Ripple Rejection Test Circuit



*D_1 Discharges C_{Adj} if Output is shorted to Ground

Figure 5. Load Regulation

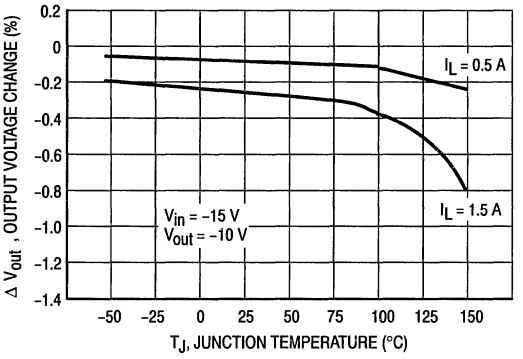


Figure 6. Current Limit

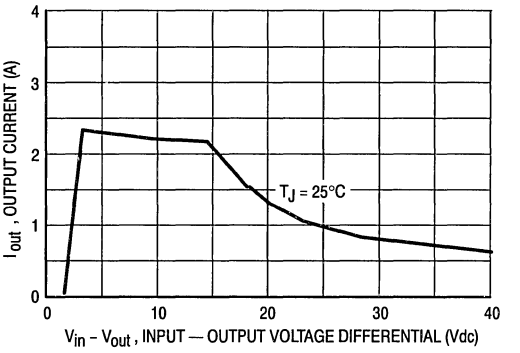


Figure 7. Adjustment Pin Current

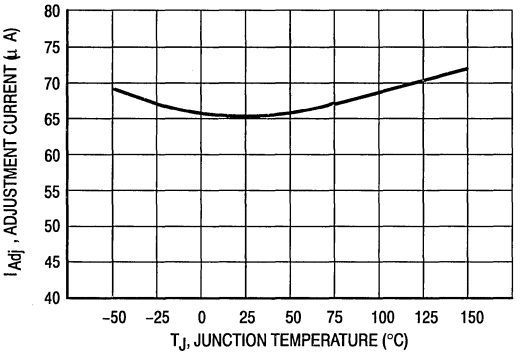


Figure 8. Dropout Voltage

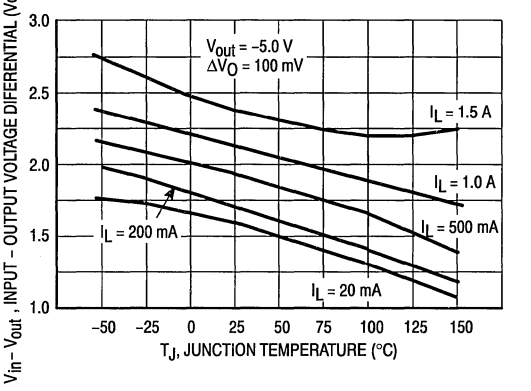


Figure 9. Temperature Stability

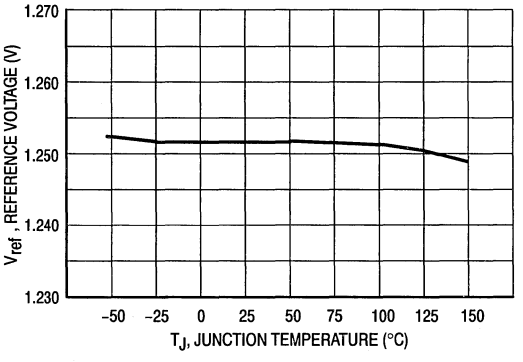


Figure 10. Minimum Operating Current

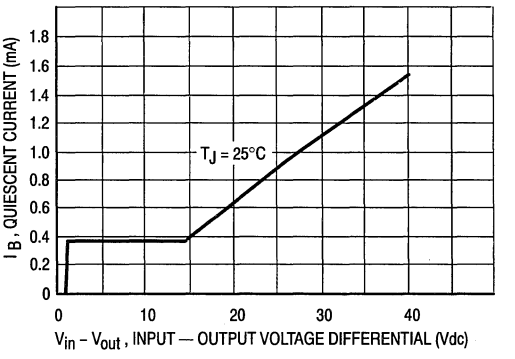


Figure 11. Ripple Rejection versus Output Voltage

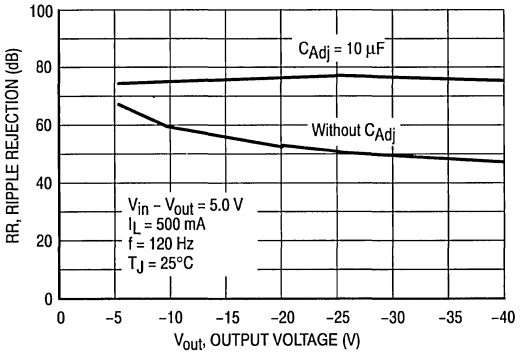


Figure 12. Ripple Rejection versus Output Current

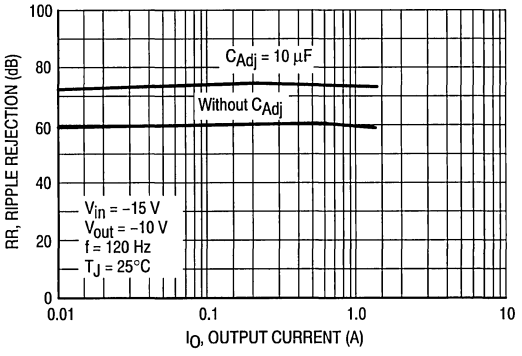


Figure 13. Ripple Rejection versus Frequency

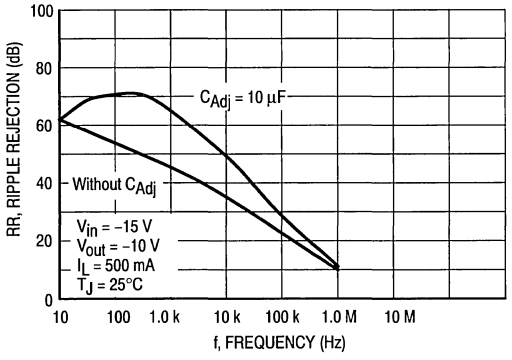


Figure 14. Output Impedance

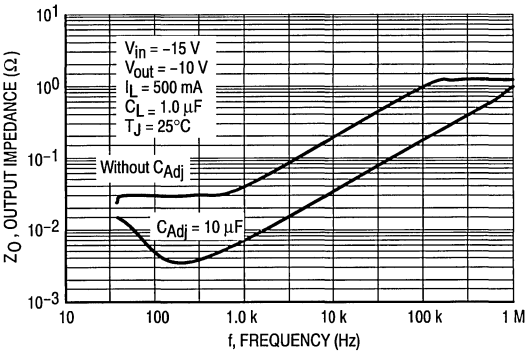


Figure 15. Line Transient Response

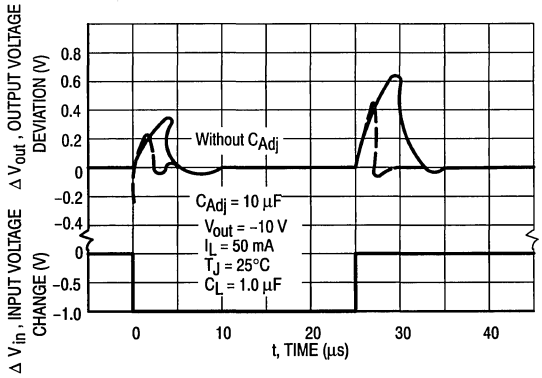
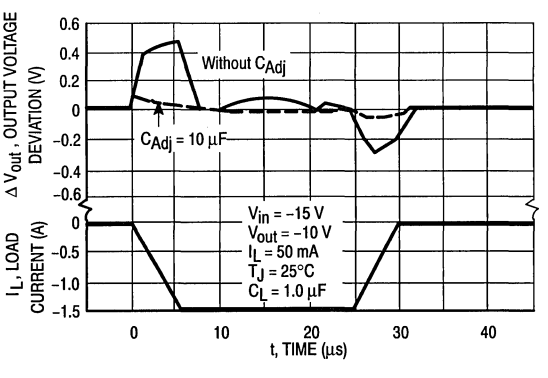


Figure 16. Load Transient Reponse



APPLICATIONS INFORMATION

Basic Circuit Operation

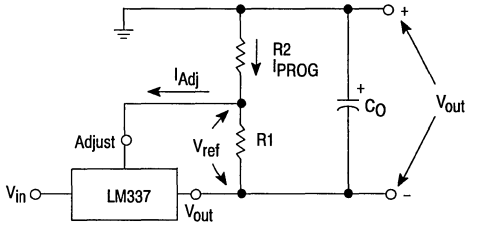
The LM337 is a 3-terminal floating regulator. In operation, the LM337 develops and maintains a nominal –1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 from ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2$$

Since the current into the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM337 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM337 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



V_{ref} = –1.25 V Typically

Load Regulation

The LM337 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 1.0 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

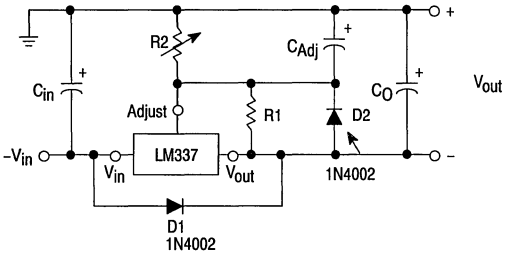
An output capacitance (C_O) in the form of a 1.0 μF tantalum or 10 μF aluminum electrolytic capacitor is required for stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM337 with the recommended protection diodes for output voltages in excess of –25 V or high capacitance values (C_O > 25 μF, C_{Adj} > 10 μF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D1 and D2 prevents C_{Adj} from the discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

LM340,A Series

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

3

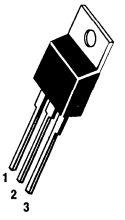
Three-Terminal Positive Voltage Regulators

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 1.0 A. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance, on A-suffix 5.0, 12 and 15 V device types.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series-pass transistor to boost output current capability at the nominal output voltage

- Output Current in Excess of 1.0 A
- No External Components Required
- Output Voltage Offered in 2% and 4% Tolerance*
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation

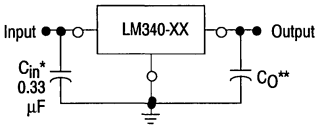
T SUFFIX
PLASTIC PACKAGE
CASE 221A



PIN 1. Input
2. Ground
3. Output

Heatsink surface connected to Pin 2

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 1.7 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

*= C_{in} is required if regulator is located an appreciable distance from power supply filter.

**= C_O is not needed for stability; however, it does improve transient response. If needed, use a 0.1 µF ceramic disc.

ORDERING INFORMATION

Device	Output Voltage and Tolerance	Tested Operating Junction Temp. Range	Package
LM340T-5.0	5.0 V ± 4%	0° to +125°C	Plastic Power
LM340AT-5.0	5.0 V ± 2%		
LM340T-6.0	6.0 V ± 4%		
LM340T-8.0	8.0 V ± 4%		
LM340T-12	12 V ± 4%		
LM340AT-12	12 V ± 2%		
LM340T-15	15 V ± 4%		
LM340AT-15	15 V ± 2%		
LM340T-18	18 V ± 4%		
LM340T-24	24 V ± 4%		

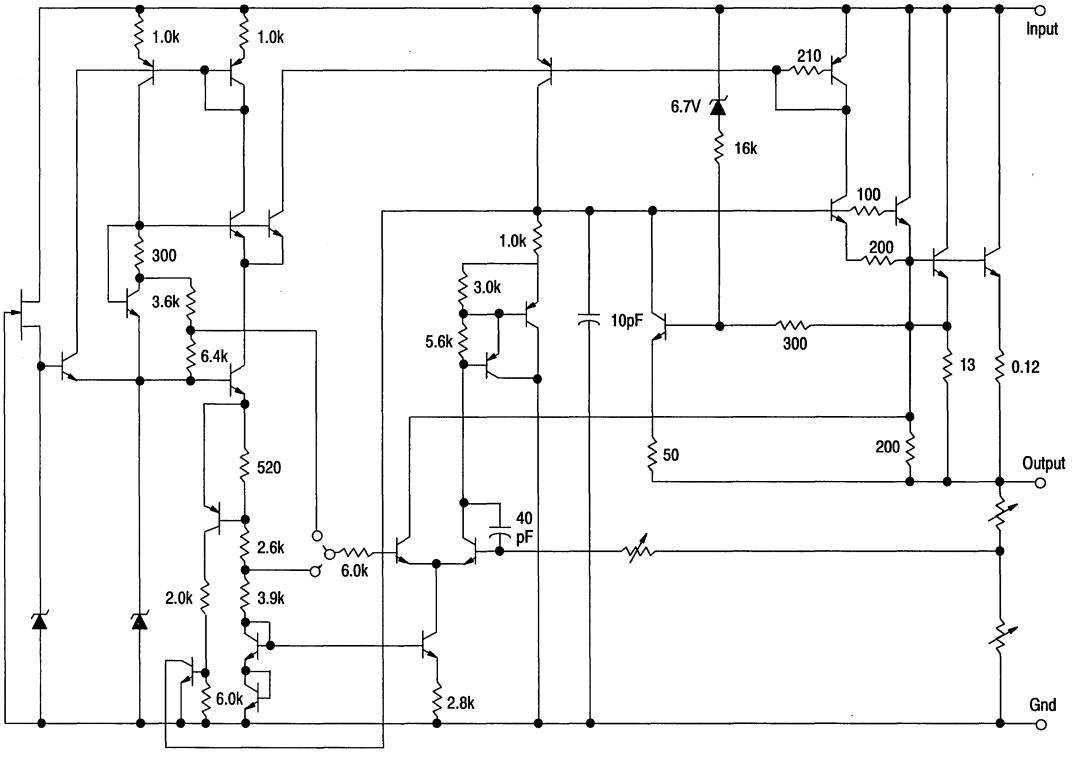
* 2% regulators are available in 5, 12 and 15 V devices.

3

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V – 18 V) (24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics Plastic Package T_A = +25°C Derate above T_A = +25°C Thermal Resistance, Junction-to-Air T_C= +25°C Derate above T_C = +75°C (See Figure 1) Thermal Resistance, Junction to Case	 P_D $1/\theta_{JA}$ θ_{JA} P_D $1/\theta_{JA}$ θ_{JC}	 Internally Limited 15.4 65 Internally Limited 200 5.0	 W mW/°C °C/W W mW/°C °C/W
Storage Junction Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

Equivalent Schematic Diagram



LM340-5.0

ELECTRICAL CHARACTERICISTICS (V_{in} = 10 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	4.8	5.0	5.2	Vdc
Line Regulation (Note 2) 8.0 Vdc to 20 Vdc 7.0 Vdc to 25 Vdc (T_J = +25°C) 8.0 Vdc to 12 Vdc, I_O = 1.0 A 7.3 Vdc to 20 Vdc, I_O = 1.0 A (T_J = +25°C)	Reg_{line}	 — — — —	 — — — —	 50 50 25 50	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)	Reg_{load}	 — — —	 — — —	 50 50 25	mV
Output Voltage 7.0 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	4.75	—	5.25	Vdc
Quiescent Current I_O = 1.0 A T_J = +25°C	I_B	 — —	 — 4.0	 8.5 8.0	mA
Quiescent Current Change 7.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 10 V 7.5 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A	ΔI_B	 — — —	 — — —	 1.0 0.5 1.0	mA
Ripple Rejection I_O = 1.0 A (T_J = +25°C)	RR	62	80	—	dB
Dropout Voltage	$V_I - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	—	2.0	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	40	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±0.6	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		7.3	—	—	Vdc

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

LM340A-5.0

ELECTRICAL CHARACTERICISTICS (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	4.9	5.0	5.1	Vdc
Line Regulation	Reg_{line}				mV
7.5 Vdc to 20 Vdc, I_O = 500 mA		—	—	10	
7.3 Vdc to 25 Vdc (T_J = +25°C)		—	3.0	10	
8.0 Vdc to 12 Vdc		—	—	12	
8.0 Vdc to 12 Vdc (T_J = +25°C)		—	—	4.0	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	25	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	25	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	15	
Output Voltage 7.5 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	4.8	—	5.2	Vdc
Quiescent Current	I_B	—	—	6.5	mA
T_J = +25°C		—	3.5	6.0	
Quiescent Current Change	ΔI_B				mA
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 10 V		—	—	0.5	
8.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		—	—	0.8	
7.5 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	0.8	
Ripple Rejection	RR				dB
8.0 ≤ V_{in} ≤ 18 Vdc, f = 120 Hz					
I_O = 500 mA		68	—	—	
I_O = 1.0 A (T_J = +25°C)		68	80	—	
Dropout Voltage	$V_I - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	—	2.0	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	40	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±0.6	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		7.3	—	—	Vdc

LM340-6.0

ELECTRICAL CHARACTERICISTICS (V_{in} = 11 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	5.75	6.0	6.25	Vdc
Line Regulation	Reg_{line}				mV
9.0 Vdc to 21 Vdc		—	—	60	
8.0 Vdc to 25 Vdc (T_J = +25°C)		—	—	60	
9.0 Vdc to 13 Vdc, I_O = 1.0 A		—	—	30	
8.3 Vdc to 21 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	60	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	60	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	60	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	30	
Output Voltage 8.0 ≤ V_{in} ≤ 21 Vdc, 6.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	5.7	—	6.3	Vdc
Quiescent Current	I_B				mA
I_O = 1.0 A		—	—	8.5	
T_J = +25°C		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
8.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 11 V		—	—	0.5	
8.6 ≤ V_{in} ≤ 21 Vdc, I_O = 1.0 A		—	—	1.0	
Ripple Rejection I_O = 1.0 A (T_J = +25°C)	RR	59	78	—	dB
Dropout Voltage	$V_I - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	—	1.9	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	45	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±0.7	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		8.3	—	—	Vdc

LM340-8.0

ELECTRICAL CHARACTERICISTICS (V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	7.7	8.0	8.3	Vdc
Line Regulation	Reg_{line}				mV
11 Vdc to 23 Vdc		—	—	80	
10.5 Vdc to 25 Vdc (T_J = +25°C)		—	—	80	
11 Vdc to 17 Vdc, I_O = 1.0 A		—	—	40	
10.5 Vdc to 23 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	80	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	80	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	80	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	40	
Output Voltage 10.5 ≤ V_{in} ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	7.6	—	8.4	Vdc
Quiescent Current	I_B				mA
I_O = 1.0 A		—	—	8.5	
T_J = +25°C		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
10.5 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 14 V		—	—	0.5	
10.6 ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A		—	—	1.0	
Ripple Rejection I_O = 1.0 A (T_J = +25°C)	RR	56	76	—	dB
Dropout Voltage	$V_I - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	—	1.5	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	52	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.0	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		10.5	—	—	Vdc

LM340-12

ELECTRICAL CHARACTERICISTICS (V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	11.5	12	12.5	Vdc
Line Regulation (Note 2) 15 Vdc to 27 Vdc 14.6 Vdc to 30 Vdc (T_J = +25°C) 16 Vdc to 22 Vdc, I_O = 1.0 A 14.6 Vdc to 27 Vdc, I_O = 1.0 A (T_J = +25°C)	Reg_{line}	 — — — —	 — — — —	 120 120 60 120	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)	Reg_{load}	 — — —	 — — —	 120 120 60	mV
Output Voltage 14.5 ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	11.4	—	12.6	Vdc
Quiescent Current I_O = 1.0 A T_J = +25°C	I_B	 — —	 — 4.0	 8.5 8.0	mA
Quiescent Current Change 14.5 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 19 V 14.8 ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A	ΔI_B	 — — —	 — — —	 1.0 0.5 1.0	mA
Ripple Rejection I_O = 1.0 A (T_J = +25°C)	RR	55	72	—	dB
Dropout Voltage	$V_I - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	—	1.1	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	75	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.5	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		14.6	—	—	Vdc

NOTES: 1. T_{low} to T_{high} = 0° to +125°C

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM340A-12

ELECTRICAL CHARACTERICISTICS (V_{in} = 19 V, I_O = 1.0 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	11.75	12	12.25	Vdc
Line Regulation	Reg_{line}				mV
14.8 Vdc to 27 Vdc, I_O = 500 mA		—	—	18	
14.5 Vdc to 30 Vdc (T_J = +25°C)		—	4.0	18	
16 Vdc to 22 Vdc		—	—	30	
16 Vdc to 22 Vdc (T_J = +25°C)		—	—	9.0	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	60	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	32	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	19	
Output Voltage 14.8 ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	11.5	—	12.5	Vdc
Quiescent Current	I_B	—	—	6.5	mA
T_J = +25°C		—	3.5	6.0	
Quiescent Current Change	ΔI_B				mA
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 19 V		—	—	0.5	
15 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		—	—	0.8	
14.8 ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A(T_J = +25°C)		—	—	0.8	
Ripple Rejection	RR				dB
15 ≤ V_{in} ≤ 25 Vdc, f = 120 Hz					
I_O = 500 mA		61	—	—	
I_O = 1.0 A (T_J = +25°C)		61	72	—	
Dropout Voltage	$V_I - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	—	1.1	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	75	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.5	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		14.5	—	—	Vdc

LM340-15

ELECTRICAL CHARACTERICISTICS (V_{in} = 23 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	14.4	15	15.6	Vdc
Line Regulation (Note 2) 18.5 Vdc to 30 Vdc 17.5 Vdc to 30 Vdc (T_J = +25°C) 20 Vdc to 26 Vdc, I_O = 1.0 A 17.7 Vdc to 30 Vdc, I_O = 1.0 A (T_J = +25°C)	Reg_{line}	 — — — —	 — — — —	 150 150 75 150	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)	Reg_{load}	 — — —	 — — —	 150 150 75	mV
Output Voltage 17.5 ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	14.25	—	15.75	Vdc
Quiescent Current I_O = 1.0 A T_J = +25°C	I_B	 — —	 — 4.0	 8.5 8.0	mA
Quiescent Current Change 17.5 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 23 V 17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A	ΔI_B	 — — —	 — — —	 1.0 0.5 1.0	mA
Ripple Rejection I_O = 1.0 mA (T_J = +25°C)	RR	54	70	—	dB
Dropout Voltage	$V_I - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	—	800	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	90	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.8	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		17.7	—	—	Vdc

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM340A-15

ELECTRICAL CHARACTERICISTICS (V_{in} = 23 V, I_O = 1.0 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	14.7	15	15.3	Vdc
Line Regulation	Reg_{line}				mV
17.9 Vdc to 30 Vdc, I_O = 500 mA		—	—	22	
17.5 Vdc to 30 Vdc (T_J = +25°C)		—	4.0	22	
20 Vdc to 26 Vdc, I_O = 1.0 A		—	—	30	
20 Vdc to 26 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	10	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	75	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	12	35	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	21	
Output Voltage 17.9 ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	14.4	—	15.6	Vdc
Quiescent Current	I_B	—	—	6.5	mA
T_J = +25°C		—	3.5	6.0	
Quiescent Current Change	ΔI_B				mA
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 23 V		—	—	0.5	
17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		—	—	0.8	
17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	0.8	
Ripple Rejection	RR				dB
18.5 ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz					
I_O = 500 mA		60	—	—	
I_O = 1.0 A (T_J = +25°C)		60	70	—	
Dropout Voltage	$V_I - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	—	800	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	90	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±1.8	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		17.5	—	—	Vdc

LM340-18

ELECTRICAL CHARACTERICISTICS (V_{in} = 27 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	17.3	18	18.7	Vdc
Line Regulation 21.5 Vdc to 33 Vdc 21 Vdc to 33 Vdc (T_J = +25°C) 24 Vdc to 30 Vdc, I_O = 1.0 A 21 Vdc to 33 Vdc, I_O = 1.0 A (T_J = +25°C)	Reg_{line}	 — — — —	 — — — —	 180 180 90 180	mV
Load Regulation 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C) 250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)	Reg_{load}	 — — —	 — — —	 180 180 90	mV
Output Voltage 21 ≤ V_{in} ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	17.1	—	18.9	Vdc
Quiescent Current I_O = 1.0 A T_J = +25°C	I_B	 — —	 — 4.0	 8.5 8.0	mA
Quiescent Current Change 21 ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 27 V 21 ≤ V_{in} ≤ 33 Vdc, I_O = 1.0 A	ΔI_B	 — — —	 — — —	 1.0 0.5 1.0	mA
Ripple Rejection I_O = 1.0 mA (T_J = +25°C)	RR	53	69	—	dB
Dropout Voltage	$V_I - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	—	500	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	110	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	—	±2.3	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		21	—	—	Vdc

LM340-24

ELECTRICAL CHARACTERICISTICS (V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} (Note 1), unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	23	24	25	Vdc
Line Regulation	Reg_{line}				mV
28 Vdc to 38 Vdc		—	—	240	
27 Vdc to 38 Vdc (T_J = +25°C)		—	—	240	
30 Vdc to 36 Vdc, I_O = 1.0 A		—	—	120	
27.1 Vdc to 38 Vdc, I_O = 1.0 A (T_J = +25°C)		—	—	240	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		—	—	240	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		—	—	240	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		—	—	120	
Output Voltage 27 ≤ V_{in} ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	22.8	—	25.2	Vdc
Quiescent Current	I_B				mA
I_O = 1.0 A		—	—	8.5	
T_J = +25°C		—	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
27 ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA		—	—	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 33 V		—	—	0.5	
27.3 ≤ V_{in} ≤ 38 Vdc, I_O = 1.0 A		—	—	1.0	
Ripple Rejection I_O = 1.0 mA (T_J = +25°C)	RR	50	66	—	dB
Dropout Voltage	$V_I - V_O$	—	1.7	—	Vdc
Output Resistance (f = 1.0 kHz)	r_O	—	2.0	—	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	—	200	—	mA
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	170	—	μV
Average Temperature Coefficient of Output Voltage I_O = 5.0 m_A	TCV_O	—	±3.0	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	2.4	—	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		27.1	—	—	Vdc

NOTES: 1. T_{low} to T_{high} = 0° to +125°C

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical LM340AK-5.0 to a 10 W input pulse. The variation of the output voltage due to line regulation is labeled À and the thermal regulation component is labeled Á. Figure 2 shows the load and thermal regulation response of a typical LM340AK-5.0 to a 15 W load pulse. The output voltage variation due to load regulation is labeled À and the thermal regulation component is labeled Á.

Figure 1. Line and Thermal Regulation

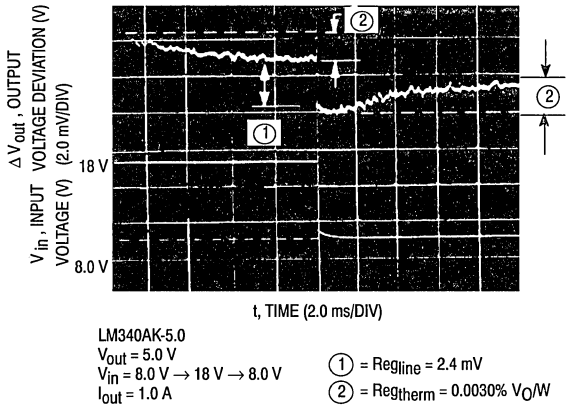


Figure 2. Load and Thermal Regulation

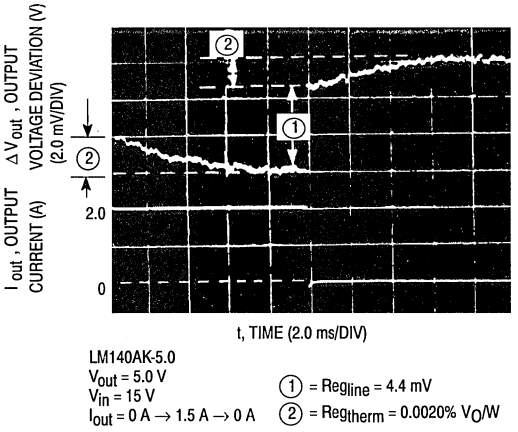


Figure 3. Temperature Stability

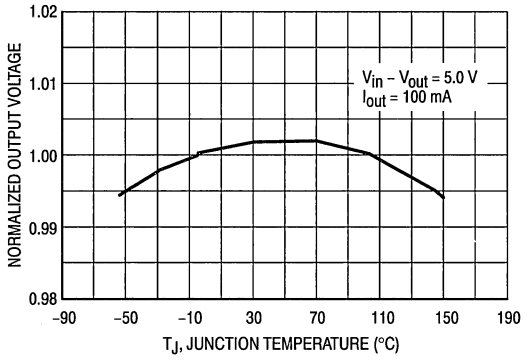


Figure 4. Output Impedance

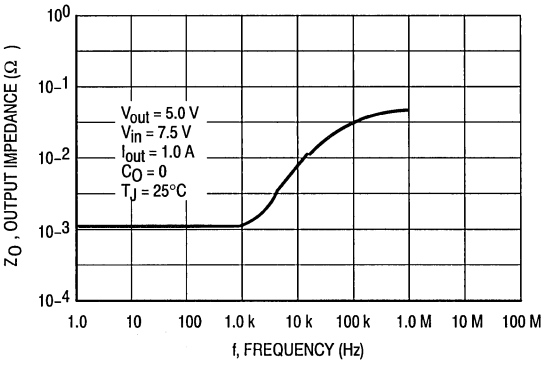


Figure 5. Ripple Rejection versus Frequency

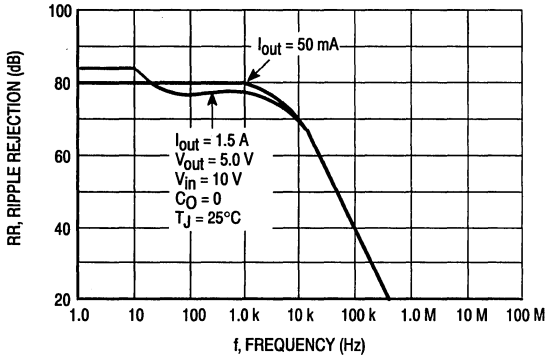


Figure 6. Ripple Rejection versus Output Current

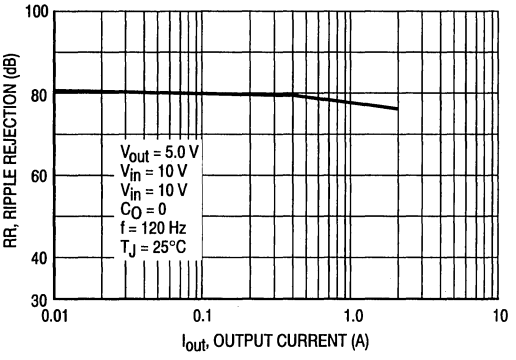


Figure 7. Quiescent Current versus Input Voltage

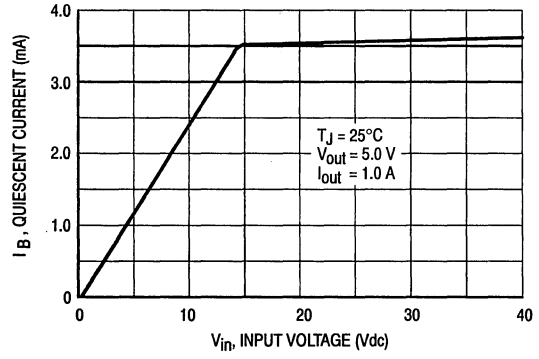


Figure 8. Quiescent Current versus Output Current

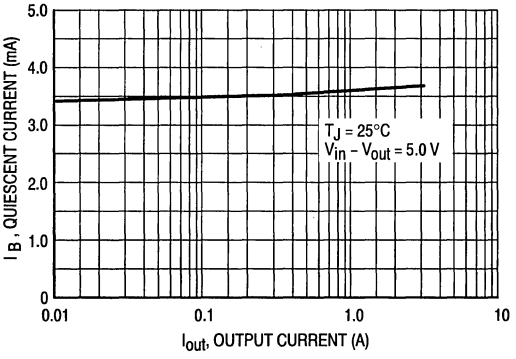


Figure 9. Dropout Voltage

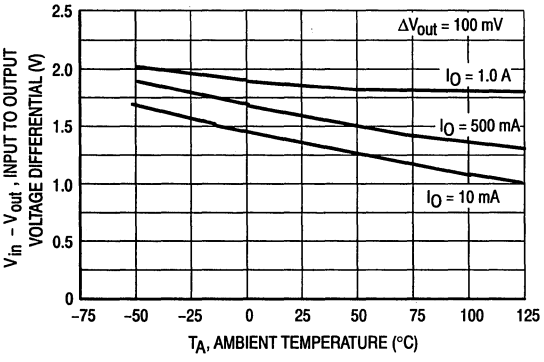


Figure 10. Peak Output Current

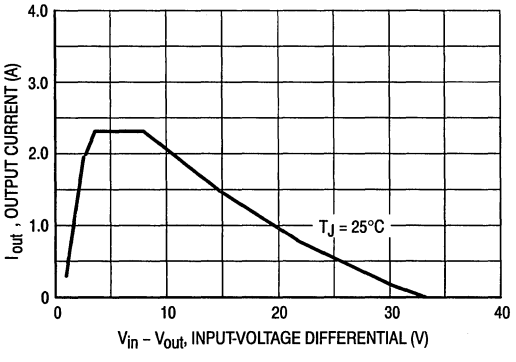


Figure 11. Line Transient Response

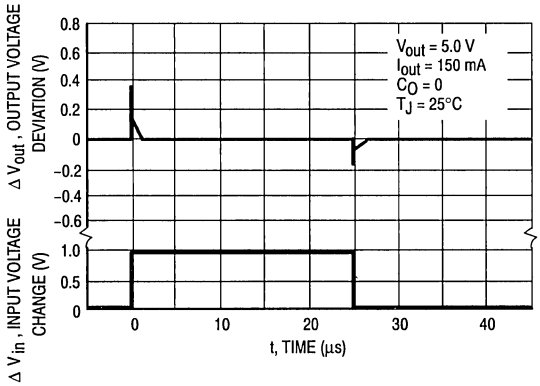


Figure 12. Load Transient Response

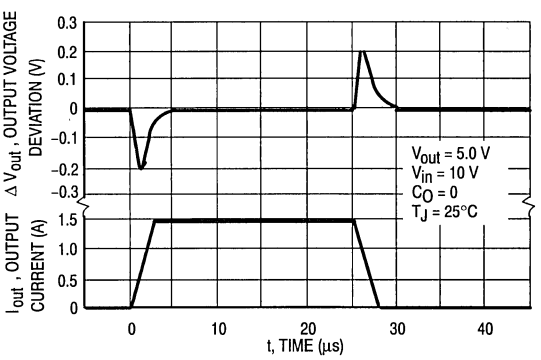
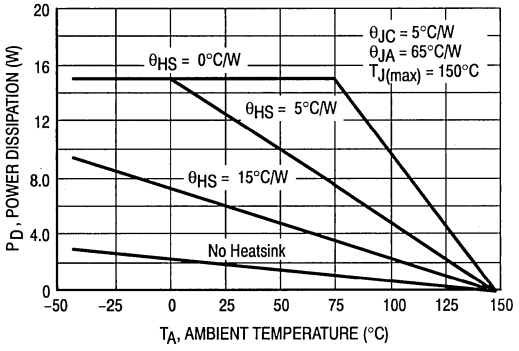


Figure 13. Worst Case Power Dissipation versus Ambient Temperature (Case 221A)



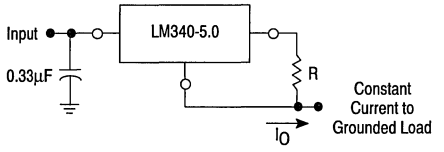
APPLICATIONS INFORMATION

Design Considerations

The LM340 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 14. Current Regulator



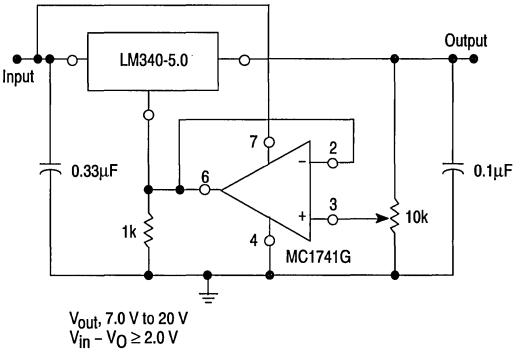
These regulators can also be used as a current source when connected as above. In order to minimize dissipation the LM340-5.0 is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_Q$$

$I_Q \cong 1.5$ mA over line and load changes

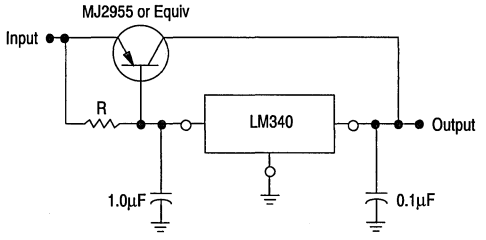
For example, a 1 A current source would require R to be a 5 Ω, 10 W resistor and the output voltage compliance would be the input voltage less 7.0 V.

Figure 15. Adjustable Output Regulator



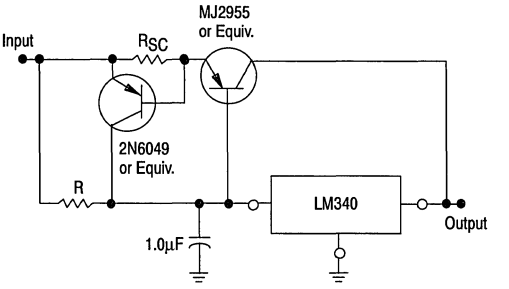
The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 V greater than the regulator voltage.

Figure 16. Current Boost Regulator



The LM340 a series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 A. Resistor R in conjuction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

Figure 17. Short Circuit Protection



The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three-terminal regulator. Therefore, 4 A plastic power transistor is specified.

LM350

Three-Terminal Adjustable Output Positive Voltage Regulator

THREE-TERMINAL ADJUSTABLE POSITIVE VOLATGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

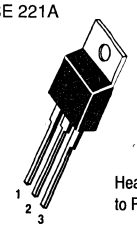
3

The LM350 is an adjustable three-terminal positive voltage regulator capable of supplying in excess of 3.0 A over an output voltage range of 1.2 V to 33 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

The LM350 serves a wide variety of applications including local, on card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM350 can be used as a precision current regulator.

- Guaranteed 3.0 A Output Current
- Output Adjustable between 1.2 V and 33 V
- Load Regulation Typically 0.1%
- Load Regulation Typically 0.005%/V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting Constant with Temperature
- Output Transistor Safe Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-lead Transistor Package
- Eliminates Stocking Many Fixed Voltages

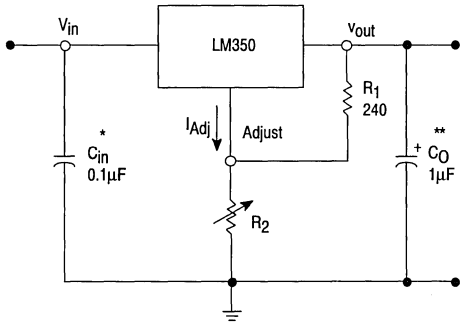
T SUFFIX
PLASTIC PACKAGE
CASE 221A



PIN 1. Adjust
2. V_{out}
3. V_{in}

Heatsink surface connected to Pin 2

Standard Application



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.
** = C_O is not needed for stability, however, it does improve transient response.

$$V_{out} = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{Adj}\ R_2$$

Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications.

ORDERING INFORMATION

Device	Tested Opearting Temperature Range	Package
LM350T	T_J = 0° to +125°C	Plastic Power
LM350BT#	T_J = –40° to +125°C	Plastic Power

Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	35	Vdc
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Soldering Lead Temperature (10 seconds)		300	°C

ELECTRICAL CHARACTERICISTICS (V_I-V_O = 5.0 V; I_L = 1.5 A; T_J = T_{low} to T_{high}; P_{max} [see Note 1], unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 2) T_A = 25°C, 3.0 V ≤ V_I-V_O ≤ 35 V	1	Reg_{line}	—	0.0005	0.03	%/V
Load Regulation (Note 2) T_A = 25°C, 10 mA ≤ I_l ≤ 3.0 A V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 5.0 0.1	 25 0.5	 mV %/V_O
Thermal Regulation, Pulse = 20 ms, (T_A = +25°C)	—	Reg_{therm}	—	0.002	—	% V_O/W
Adjustment Pin Current	3	I_{Adj}	—	50	100	µA
Adjustment Pin Current Change 3.0 V ≤ V_I-V_O ≤ 35 V 10 mA ≤ I_L ≤ 3.0 A, P_D ≤ P_{max}	1,2	ΔI_{Adj}	—	0.2	5.0	µA
Reference Voltage 3.0 V ≤ V_I-V_O ≤ 35 V 10 mA ≤ I_O ≤ 3.0 A, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	V
Line Regulation (Note 2) 3.0 V ≤ V_I-V_O ≤ 35 V	1	Reg_{line}	—	0.02	0.07	%/V
Load Regulation (Note 2) 10 mA ≤ I_L ≤ 3.0 A V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 20 0.3	 70 1.5	 mV %/V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	1.0	—	%/V_O
Minimum Load Current to Maintain Regulation (V_I-V_O = 35 V)	3	I_{Lmin}	—	3.5	10	mA
Maximum Output Current V_I-V_O ≤ 10 V, P_D ≤ P_{max} V_I-V_O = 30 V, P_D ≤ P_{max}, T_A = 25°C	3	I_{max}	 3.0 0.25	 4.5 1.0	 — —	A
RMS Noise, % of V_O T_A= 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	%/V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 3) Without C_{Adj} C_{Adj} = 10 µF	4	RR	 — 66	 65 80	 — —	dB
Long-Term Stability, T_J = T_{high} (Note 4) T_A= 25°C for Endpoint Measurements	3	S	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case Peak (Note 5) T Package Average (Note 6) T Package	—	$R_{\theta JC}$	 — —	 2.3 —	 — 1.5	°C/W

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
. P_{max} = 25 W
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
3. C_{Adj}, when used, is connected between the adjustment pin and ground.
4. Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
5. Thermal Resistance evaluated measuring the hottest temperature on the die using an infrared scanner. This method of evaluation yields very accurate thermal resistance values which are conservative when compared to the other measurement techniques.
6. The average die temperature is used to derive the value of thermal resistance junction to case (average).

Schematic Diagram

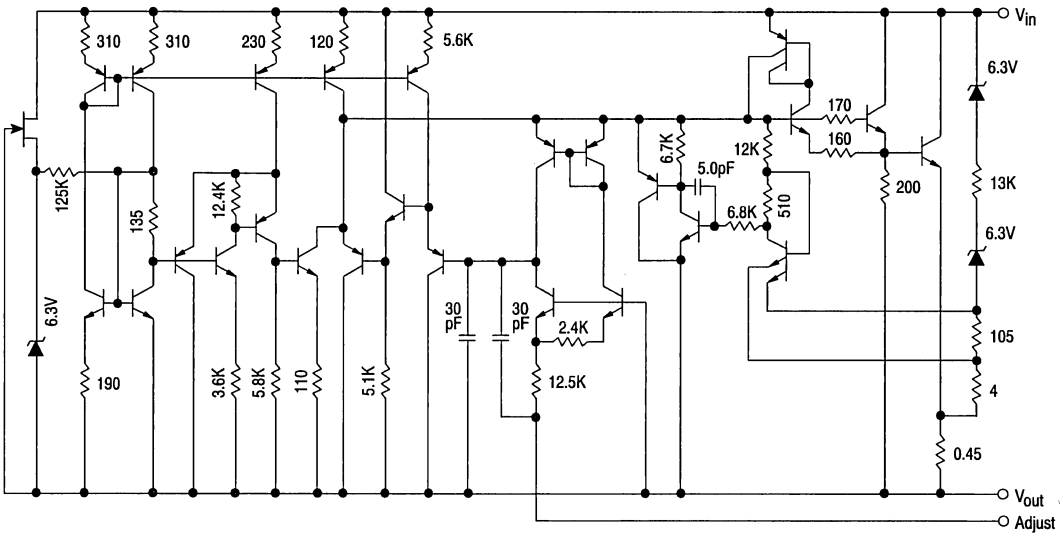


Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit

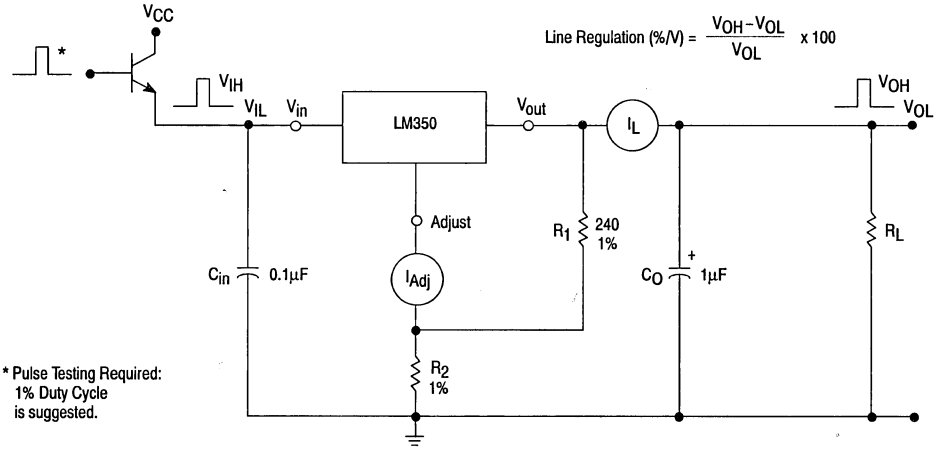


Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit

$$\text{Load Regulation } (\%/V_O) = \frac{V_O \text{ (min Load)} - V_O \text{ (max Load)}}{V_O \text{ (min Load)}} \times 100$$

$$\text{Load Regulation (mV)} = V_O \text{ (min Load)} - V_O \text{ (max Load)}$$

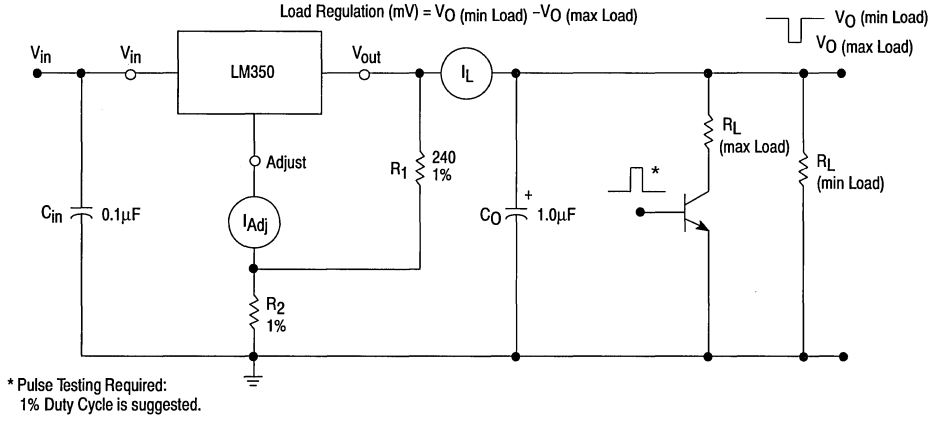


Figure 3. Standard Test Circuit

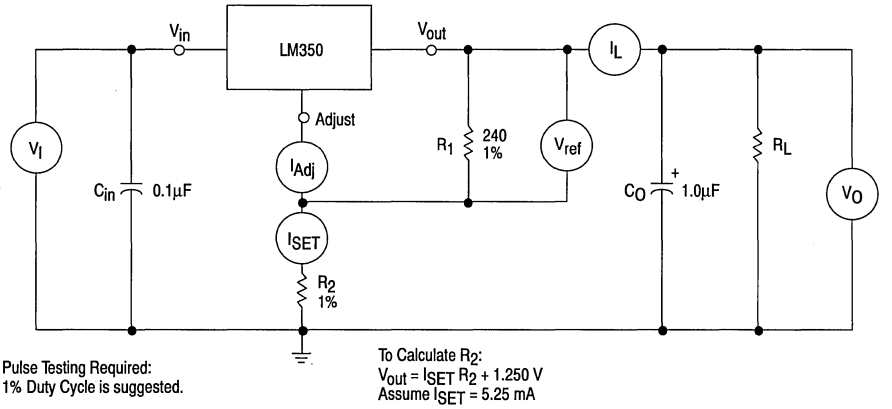


Figure 4. Ripple Rejection Test Circuit

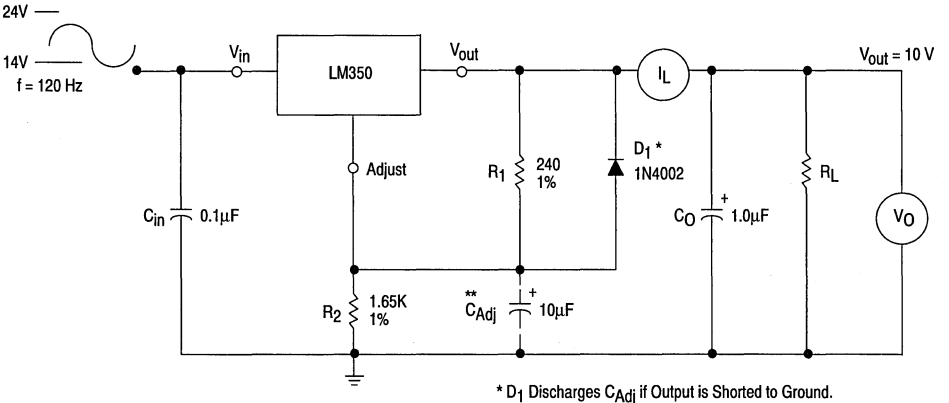


Figure 5. Load Regulation

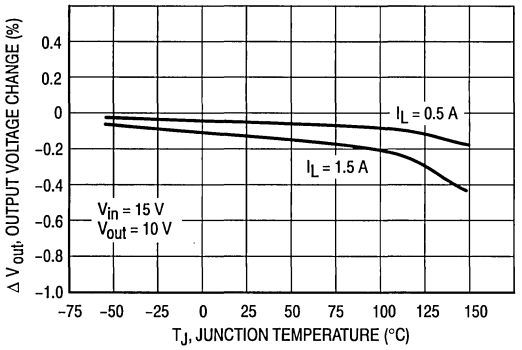


Figure 6. Current Limit

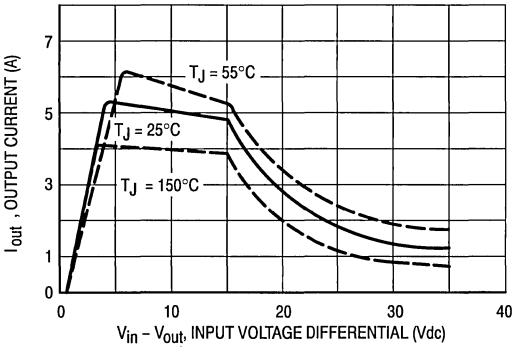


Figure 7. Adjustment Pin Current

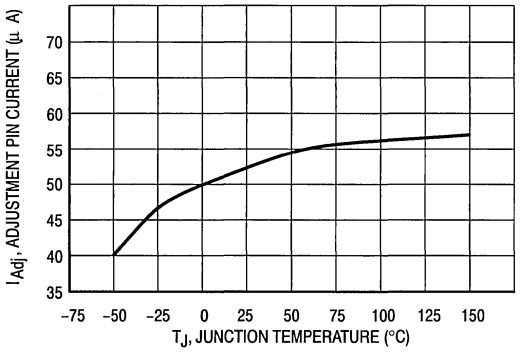


Figure 8. Dropout Voltage

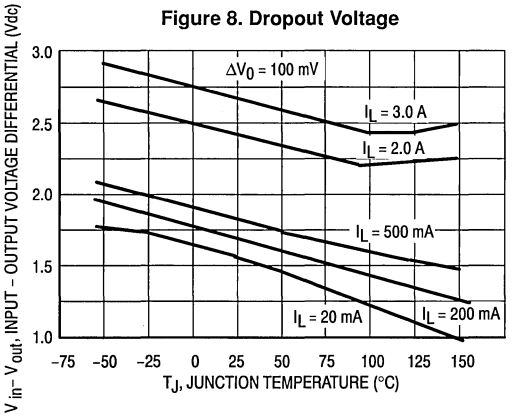


Figure 9. Temperature Stability

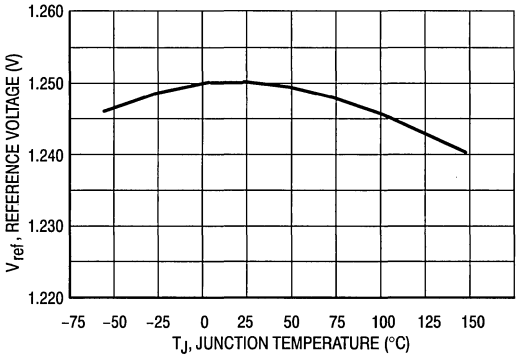


Figure 10. Minimum Operating Current

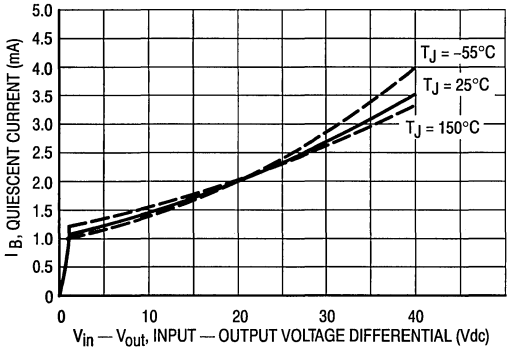


Figure 11. Ripple Rejection versus Output Voltage

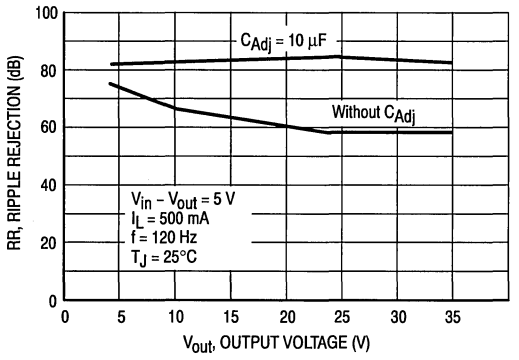


Figure 12. Ripple Rejection versus Output Current

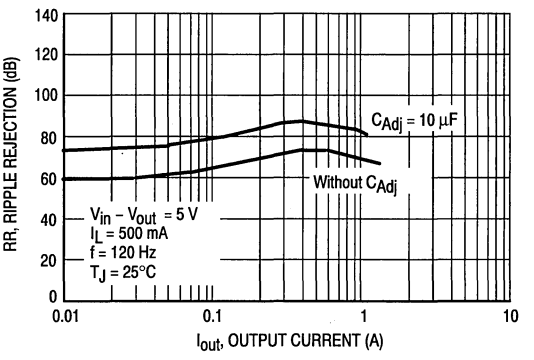


Figure 13. Ripple Rejection versus Frequency

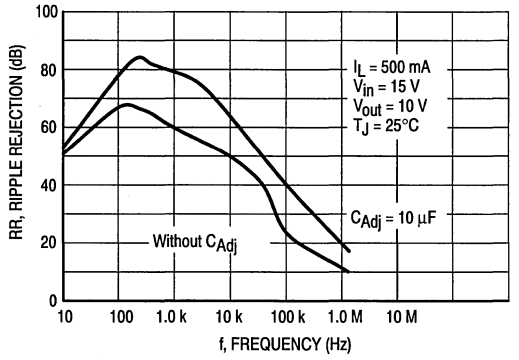


Figure 14. Output Impedance

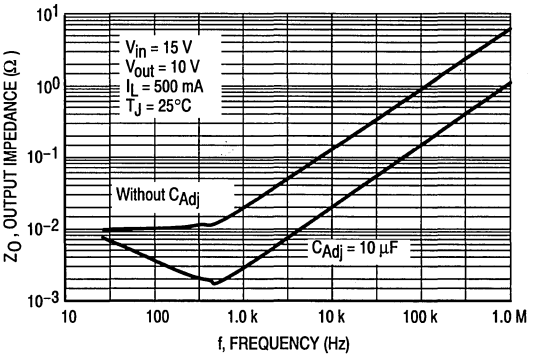


Figure 15. Line Transient Response

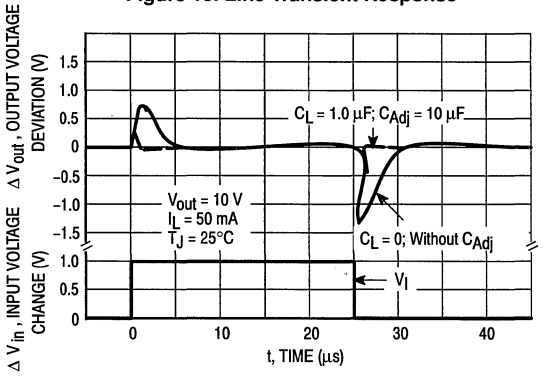
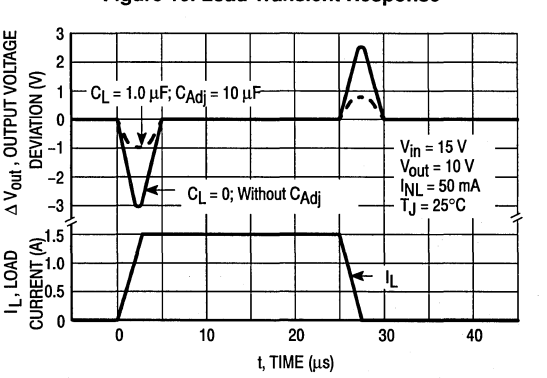


Figure 16. Load Transient Response



APPLICATIONS INFORMATION

Basic Circuit Operation

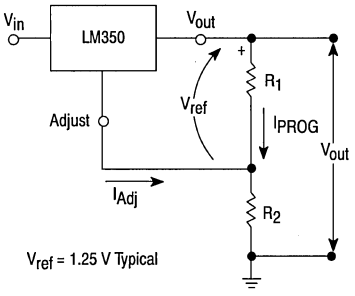
The LM350 is a three-terminal floating regulator. In operation, the LM350 develops and maintains a nominal 1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2$$

Since the current from the terminal (I_{Adj}) represents an error term in the equation, the LM350 was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM350 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



Load Regulation

The LM350 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 μF disc or 1 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM350 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator, it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM350 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values (C_O > 25 μF, C_{Adj} > 10 μF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D1 and D2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes

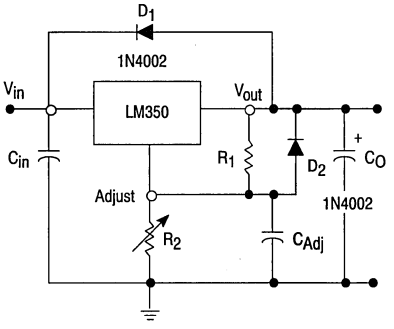
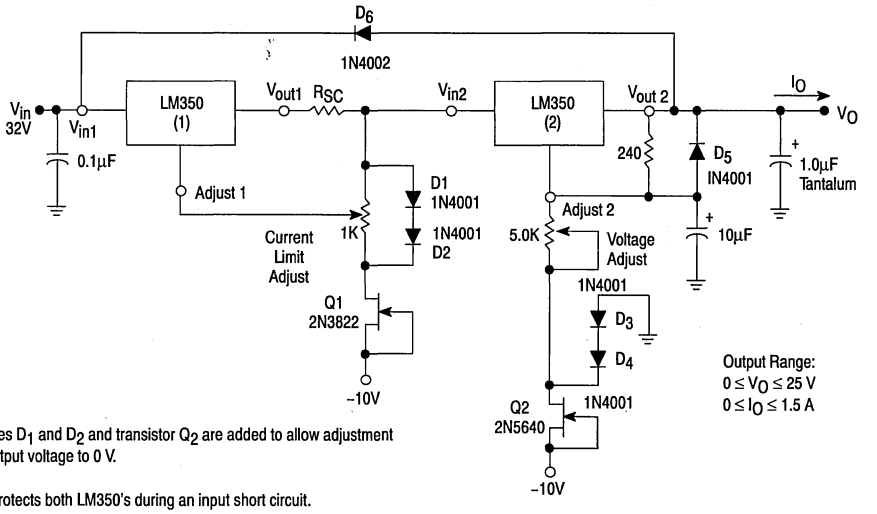


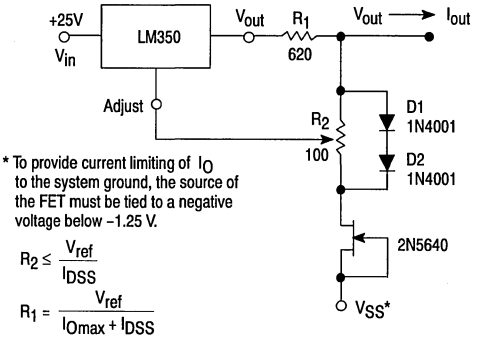
Figure 19. "Laboratory" Power Supply with Adjustable Current Limit and Output Voltage



Diodes D_1 and D_2 and transistor Q_2 are added to allow adjustment of output voltage to 0 V.

D_6 protects both LM350's during an input short circuit.

Figure 20. Adjustable Current Limiter



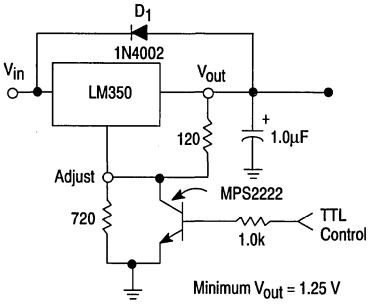
* To provide current limiting of I_O to the system ground, the source of the FET must be tied to a negative voltage below -1.25 V.

$$R_2 \leq \frac{V_{ref}}{I_{DSS}}$$

$$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$$

$V_O < V_{(BR)DSS} + 1.25\ V + V_{SS}$
$I_{Lmin} - I_{DSS} < I_O < 3.0\ A$
As shown $0 < I_O < 1.0\ A$

Figure 21. 5.0 V Electronic Shutdown Regulator



D_1 protects the device during an input short circuit.

Figure 22. Slow Turn-On Regulator

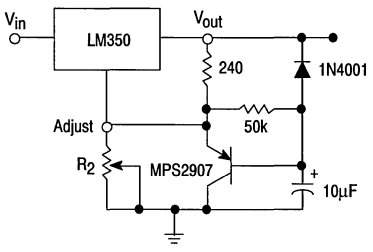
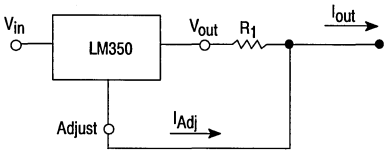


Figure 23. Current Regulator



$$I_{out} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj}$$

$$\cong \frac{1.25\ V}{R_1}$$

$10\ mA \leq I_{out} \leq 3.0\ A$

LM317M

Three-Terminal Adjustable Output Positive Voltage Regulator

MEDIUM-CURRENT THREE-TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

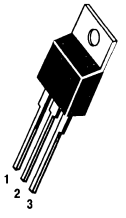
SILICON MONOLITHIC INTEGRATED CIRCUIT

The LM317M is an adjustable three-terminal positive voltage regulator capable of supplying in excess of 500 mA over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

The LM317M serves a wide variety of applications including local, on-card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317M can be used as a precision current regulator.

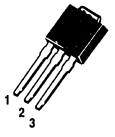
- Output Current in Excess of 500 mA
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

T SUFFIX
PLASTIC PACKAGE
CASE 221A



(All 3 Packages)
PIN 1. Adjust
2. V_{out}
3. V_{in}

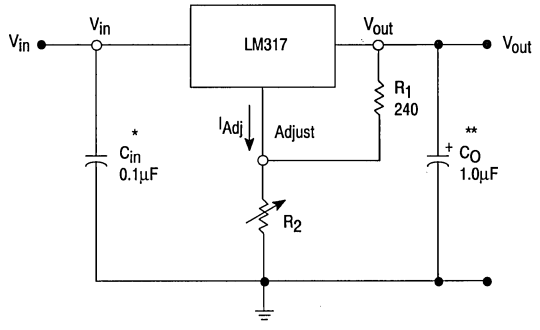
Heatsink surface connected to Pin 2



DT-1 SUFFIX
PLASTIC PACKAGE
CASE 369
(DPAK)

DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)

Standard Application



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.
** = C_O is not needed for stability, however, it does improve transient response.

$$V_{out} = 1.25\ V\ (1 + \frac{R_2}{R_1}) + I_{Adj}\ R_2$$

Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications.

ORDERING INFORMATION

Device	Tested Opearting Temperature Range	Package
LM317MT	0° to +125°C	Plastic Power
LM317MBT#	–40° to +125°C	Plastic Power
LM317MDT LM317MDT-1	0° to 125°C	DPAK

Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERICISTICS (V_I-V_O = 5.0 V; I_O = 0.1 A, T_J = T_{low} to T_{high} [see Note 1]; P_{max} per Note 2; unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ V_I-V_O ≤ 40 V	1	Reg_{line}	—	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ 0.5 A V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 5.0 0.1	 25 0.5	 mV %/V_O
Adjustment Pin Current	3	I_{Adj}	—	50	100	µA
Adjustment Pin Current Change 2.5 V ≤ V_I-V_O ≤ 40 V, 10 mA ≤ I_L ≤ 0.5 A, P_D ≤ P_{max}	1,2	ΔI_{Adj}	—	0.2	5.0	µA
Reference Voltage 3.0 V ≤ V_I-V_O ≤ 40 V, 10 mA ≤ I_O ≤ 0.5 A, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	V
Line Regulation (Note 3) 3.0 V ≤ V_I-V_O ≤ 40 V	1	Reg_{line}	—	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ 0.5 A V_O ≤ 5.0 V V_O ≥ 5.0 V	2	Reg_{load}	 — —	 20 0.3	 70 1.5	 mV %/V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.7	—	%/V_O
Minimum Load Current to Maintain Regulation (V_I-V_O = 40 V)	3	I_{Lmin}	—	3.5	10	mA
Maximum Output Current V_I-V_O ≤ 15 V, P_D ≤ P_{max} V_I-V_O = 40 V, P_D ≤ P_{max}, T_A = 25°C	3	I_{max}	 0.5 0.15	 0.9 0.25	 — —	A
RMS Noise, % of V_O T_A= 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	%/V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 4) Without C_{Adj} C_{Adj} = 10 µF	4	RR	 — 66	 65 80	 — —	dB
Long-Term Stability, T_J = T_{high} (Note 5) T_A= 25°C for Endpoint Measurements	3	S	—	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case, T Suffix Package	—	$R_{\theta JC}$	—	7.0	—	°C/W

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
2. P_{max} = 7.5 W
3. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
4. C_{Adj}, when used, is connected between the adjustment pin and ground.
5. Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

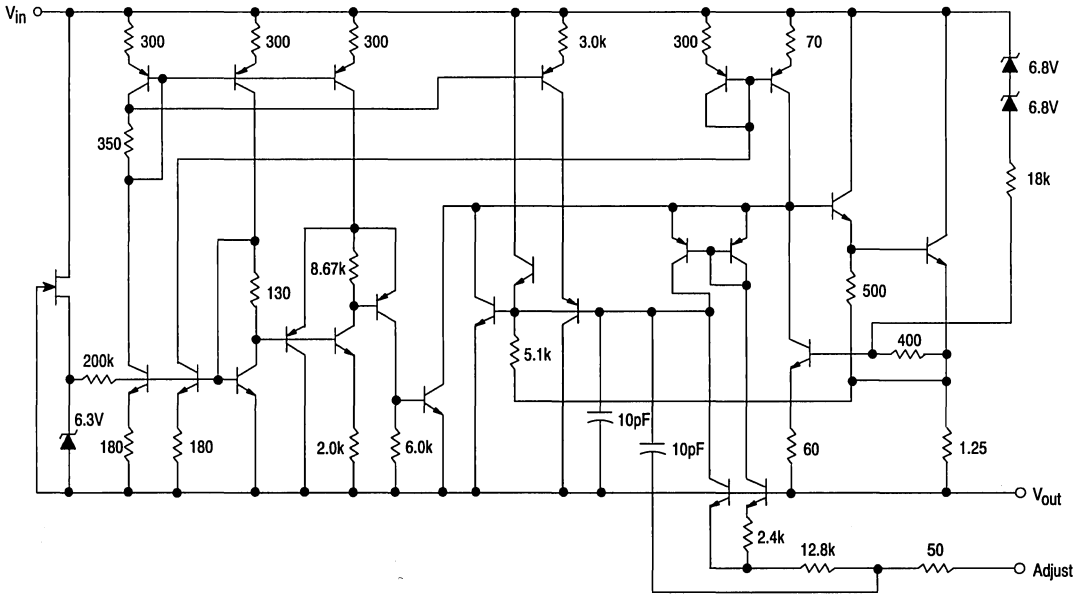
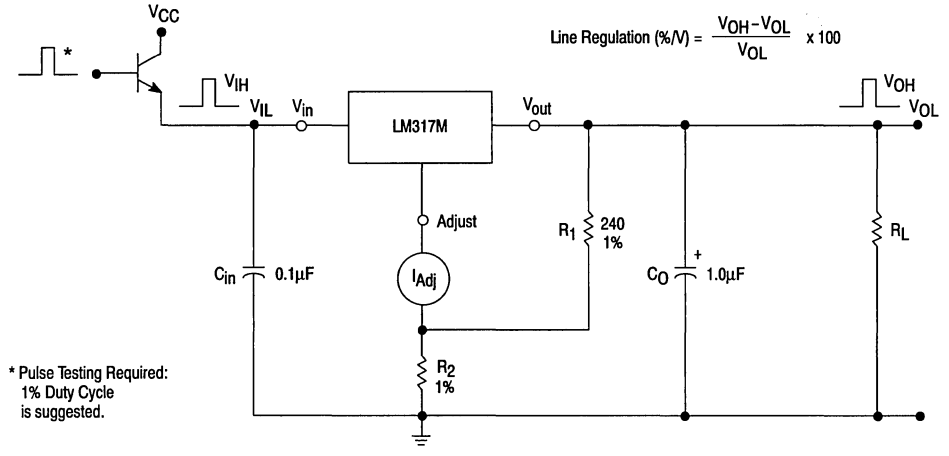
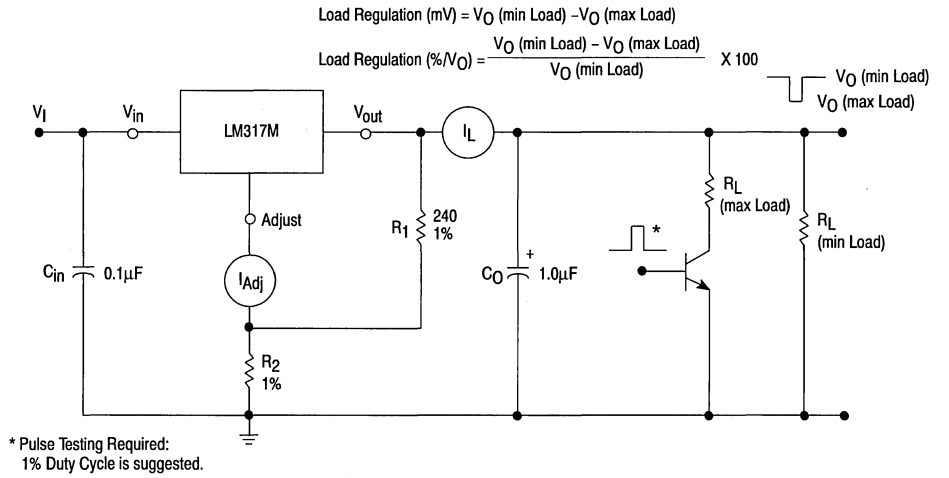


Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit



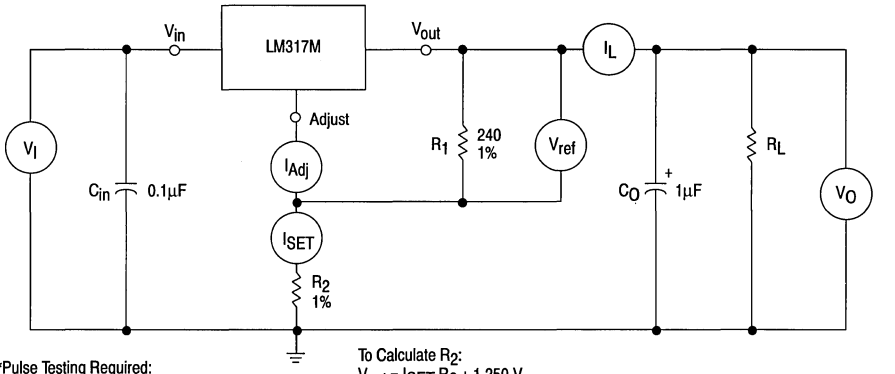
$$\text{Line Regulation (\%/V)} = \frac{V_{OH} - V_{OL}}{V_{OL}} \times 100$$

Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit



* Pulse Testing Required:
1% Duty Cycle is suggested.

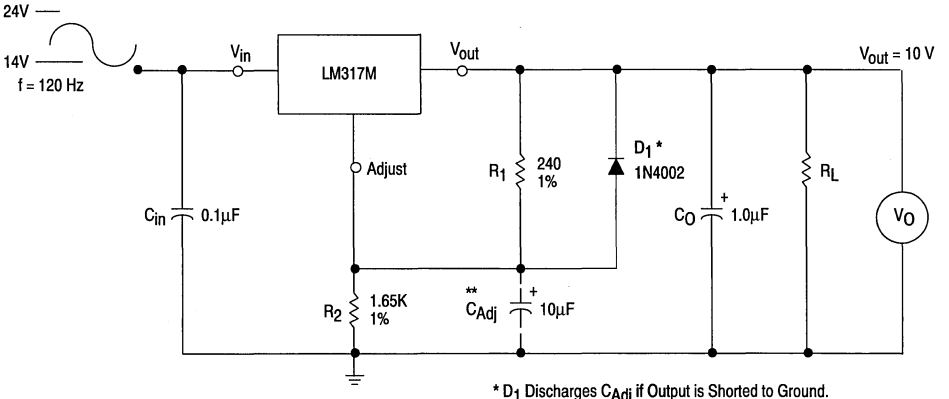
Figure 3. Standard Test Circuit



*Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate R_2:
$V_{out} = I_{SET} R_2 + 1.250$ V
Assume $I_{SET} = 5.25$ mA

Figure 4. Ripple Rejection Test Circuit



* D_1 Discharges C_{Adj} if Output is Shorted to Ground.
**C_{Adj} provides an AC ground to the adjust pin.

Figure 5. Load Regulation

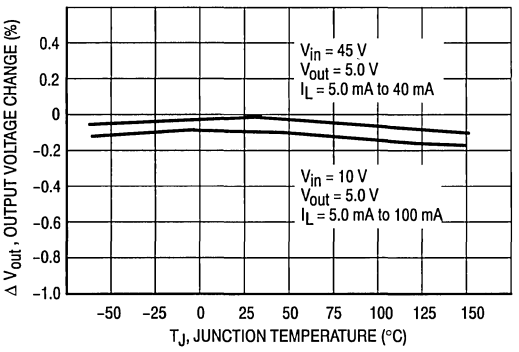


Figure 6. Ripple Rejection

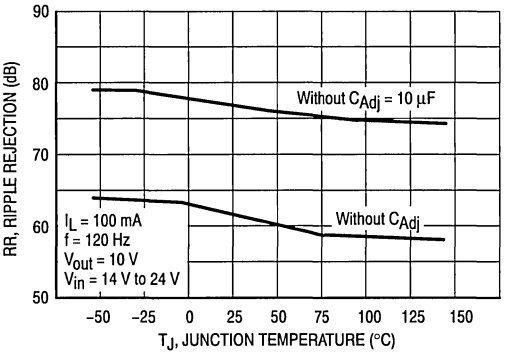


Figure 7. Current Limit

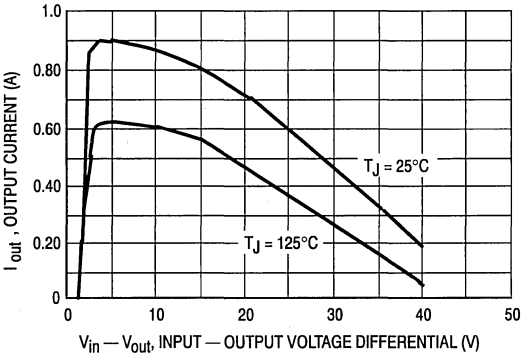


Figure 8. Dropout Voltage

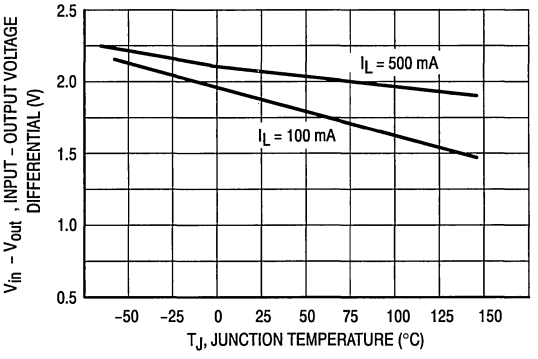


Figure 9. Minimum Operating Current

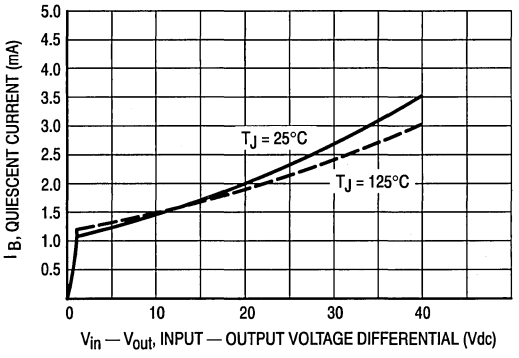


Figure 10. Ripple Rejection versus Frequency

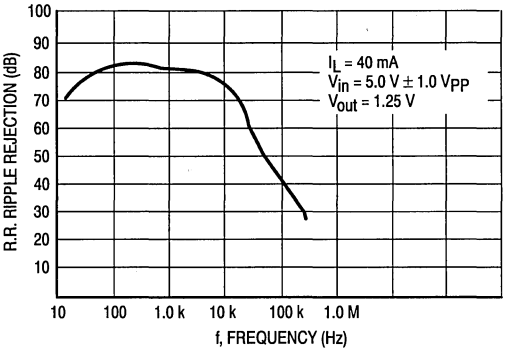


Figure 11. Temperature Stability

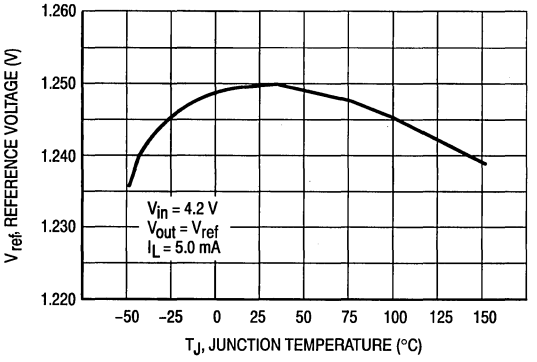


Figure 12. Adjustment Pin Current

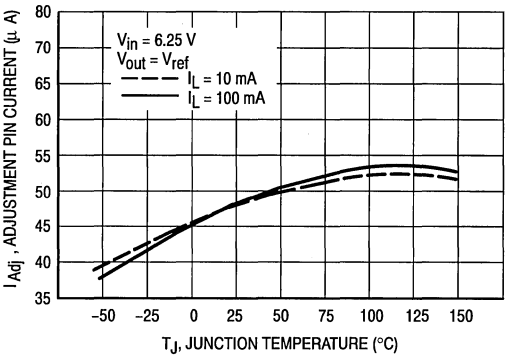


Figure 13. Line Regulation

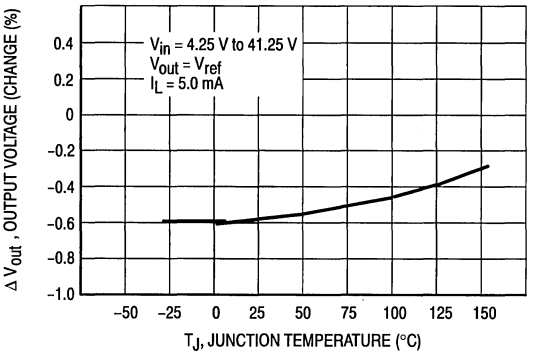


Figure 14. Output Noise

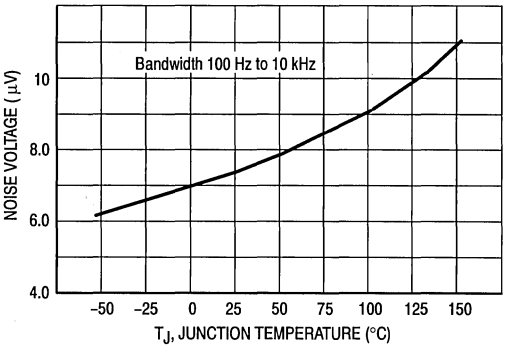


Figure 15. Line Transient Response

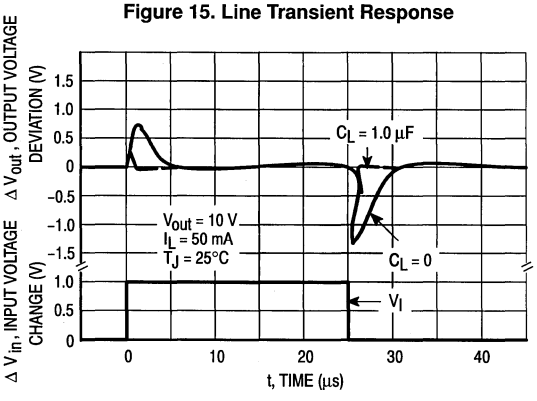
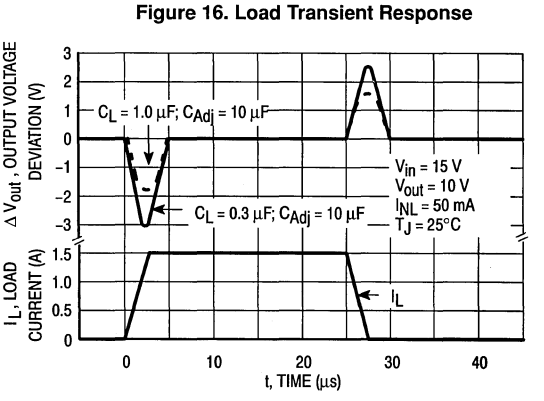


Figure 16. Load Transient Response



APPLICATIONS INFORMATION

Basic Circuit Operation

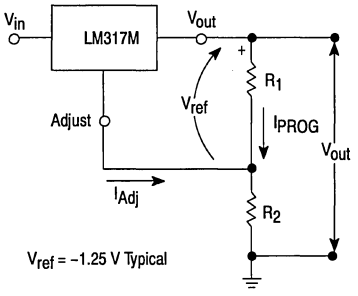
The LM317M is a three-terminal floating regulator. In operation, the LM317M develops and maintains a nominal 1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\,R2$$

Since the current from the terminal (I_{Adj}) represents an error term in the equation, the LM317M was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317M is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



Load Regulation

The LM317M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 μF disc or 1.0 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM317M is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM317M with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values (C_O > 25 μF, C_{Adj} > 5.0 μF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D1 and D2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes

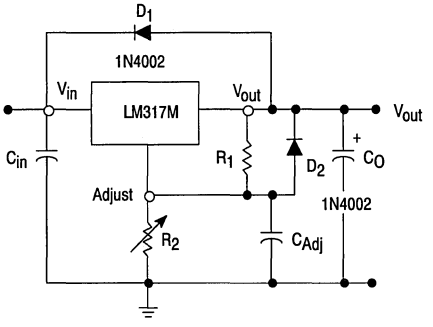
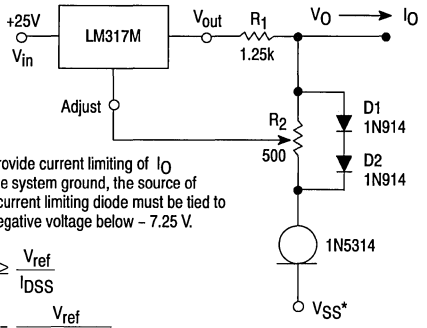


Figure 19. Adjustable Current Limiter



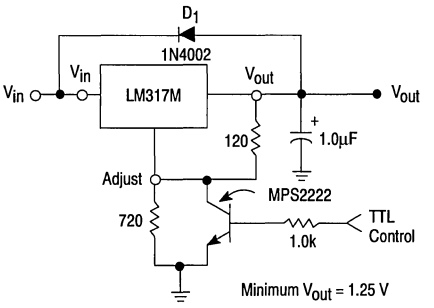
* To provide current limiting of I_O to the system ground, the source of the current limiting diode must be tied to a negative voltage below – 7.25 V.

$$R_2 \geq \frac{V_{ref}}{I_{DSS}}$$

$$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$$

$V_O < P_{OV} + 1.25\ V + V_{SS}$
$I_{Lmin} - I_P < I_O < 500\ mA - I_P$
As shown $0 < I_O < 495\ mA$

Figure 20. 5 V Electronic Shutdown Regulator



D_1 protects the device during an input short circuit.

Figure 21. Slow Turn-On Regulator

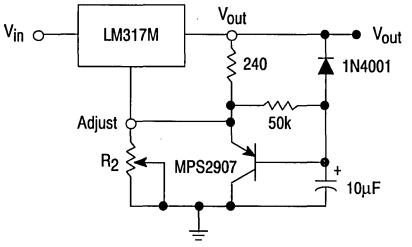
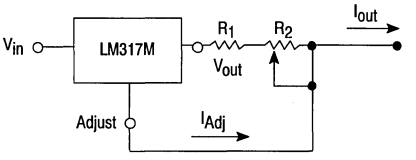


Figure 22. Current Regulator



$$I_{outmax} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj} \cong \frac{1.25\ V}{R_1}$$

$$I_{outmax} = \left(\frac{V_{ref}}{R_1 + R_2}\right) + I_{Adj} \cong \frac{1.25\ V}{R_1 + R_2}$$

$5.0\ mA < I_{out} < 100\ mA$

LM337M

Three-Terminal Adjustable Output Negative Voltage Regulator

MEDIUM-CURRENT THREE-TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATOR

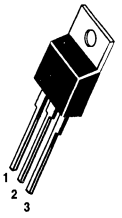
SILICON MONOLITHIC INTEGRATED CIRCUIT

The LM337M is an adjustable three-terminal negative voltage regulator capable of supplying in excess of 500 mA over an output voltage range of –1.2 V to –37 V. This voltage regulator is exceptionally easy to use and require only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow-out proof.

The LM337M serves a wide variety of applications including local, on-card regulation. This device can also be used to make a programmable output regulator; or, by connecting a fixed resistor between the adjustment and output, the LM337M can be used as a precision current regulator.

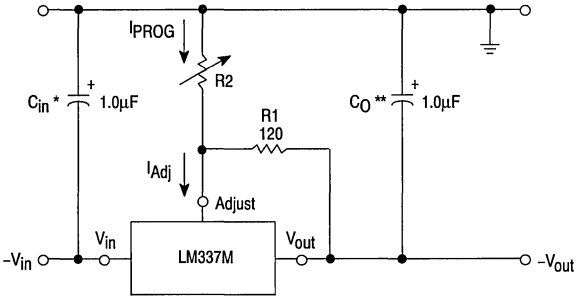
- Output Current in Excess of 500 mA
- Output Adjustable Between –1.2 V and –37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

T SUFFIX
PLASTIC PACKAGE
CASE 221A



Pin 1. Adjust
2. V_{in}
3. V_{out}

Standard Application



*C_{in} is required if regulator is located more than 4 inches from power supply filter. A 1.0 µF solid tantalum or 10 µF aluminum electrolytic is recommended.
**C_O is necessary for stability. A 1.0 µF solid tantalum or 10 µF aluminum electrolytic is recommeded.

$$V_{out} = -1.25\ V\left(1 + \frac{R2}{R1}\right)$$

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
LM337MT	T_J = 0° to +125°C	Plastic Power
LM337MBT#	T_J = –40° to +125°C	Plastic Power

Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_O	40	Vdc
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERICISTICS ($|V_I - V_O| = 5.0$ V, $I_O = 0.1$; $T_J = T_{low}$ to T_{high} [see Note 1], P_{max} per Note 2, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ $\|V_I–V_O\|$ ≤ 40 V	1	Reg_{line}	—	0.01	0.04	%/V
Load Regulation (Note 3) T_A = 25°C, 10 mA ≤ I_O ≤ 0.5 A $\|V_O\|$ ≤ 5.0V $\|V_O\|$ ≥ 5.0V	2	Reg_{load}	 — —	 15 0.3	 15 1.0	 mV %/V_O
Thermal Regulation 10 ms Pulse, T_A = 25°C	—	Reg_{therm}	—	0.03	0.04	% V_O/W
Adjustment Pin Current	3	I_{Adj}	—	65	100	µA
Adjustment Pin Current Change 2.5 V ≤ $\|V_I–V_O\|$ ≤ 40 V, 10 mA ≤ I_L ≤ 0.5 A, P_D ≤ P_{max}, T_A = 25°C	1, 2	ΔI_{Adj}	—	2.0	5.0	µA
Reference Voltage 3.0 V ≤ $\|V_I–V_O\|$ ≤ 40 V, 10 mA ≤ I_O ≤ 0.5 A, P_D ≤ P_{max}, T_A = 25°C T_{low} to T_{high}	3	V_{ref}	 –1.213 –1.20	 –1.250 –1.25	 –1.287 –1.30	V
Line Regulation (Note 3) 3.0 V ≤ $\|V_I–V_O\|$ ≤ 40 V	1	Reg_{line}	—	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ 0.5 A $\|V_O\|$ ≤ 5.0 V $\|V_O\|$ ≥ 5.0 V	2	Reg_{load}	 — —	 20 0.3	 70 1.5	mV %/V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	—	0.6	—	%/V_O
Minimum Load Current to Maintain Regulation ($\|V_I–V_O\|$ ≤ 10 V) ($\|V_I–V_O\|$ ≤ 40 V)	3	I_{Lmin}	 — —	 1.5 2.5	 6.0 10	mA
Maximum Output Current $\|V_I–V_O\|$ ≤ 15 V, P_D ≤ P_{max} $\|V_I–V_O\|$ ≤ 40 V, P_D ≤ P_{max}, T_J = 25°C	3	I_{max}	 0.5 0.1	 0.9 0.25	 — —	A
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz	—	N	—	0.003	—	%/V_O
Ripple Rejection, V_O = –10 V, f = 120 Hz (Note 4) Without C_{Adj} C_{Adj} = 10 µF	4	RR	 — 66	 60 77	 — —	dB
Long-Term Stability, T_J = T_{high} (Note 5) T_A = 25°C for Endpoint Measurements	3	S	—	0.3	1.0	%/1.0 k Hrs
Thermal Resistance Junction to Case	—	$R_{\Theta JC}$	—	7.0	—	°C/W

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
2. P_{max} = 7.5 W
3. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account seperately. Pulse testing with low duty cycle is used.
4. C_{Adj}, when used, is connected between the adjustment pin and ground.
5. Since Long-Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

SCHEMATIC DIAGRAM

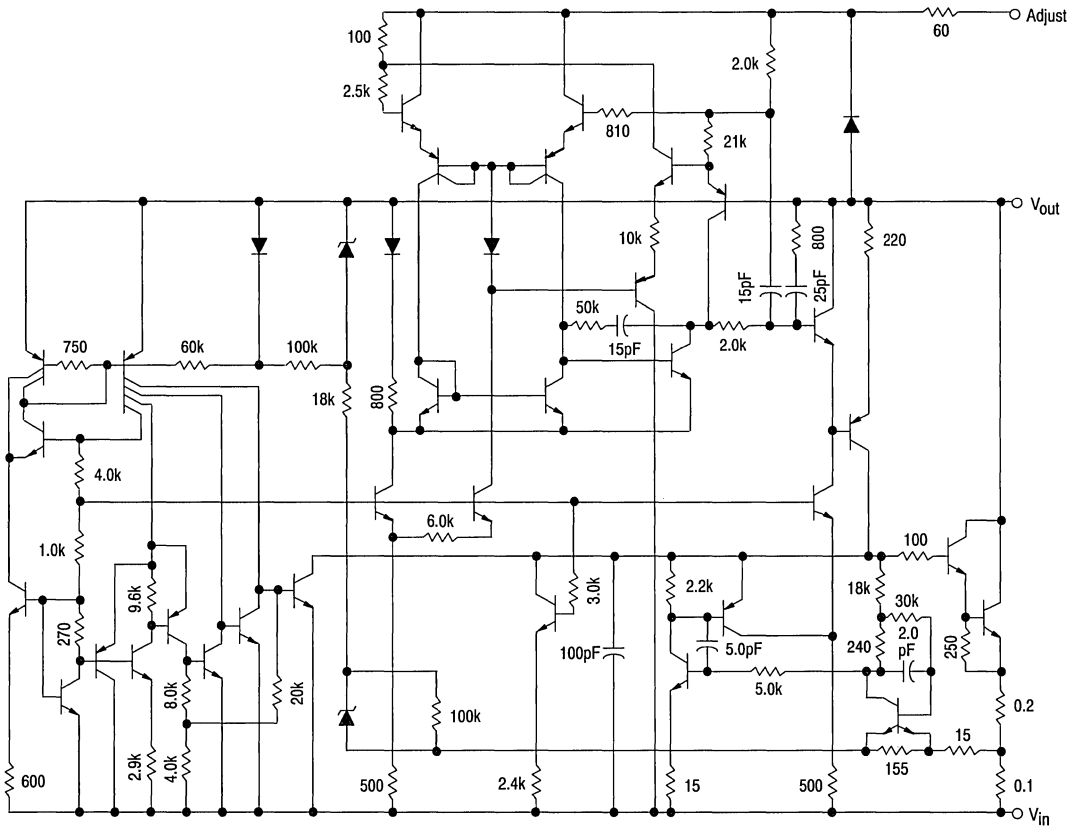


Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit

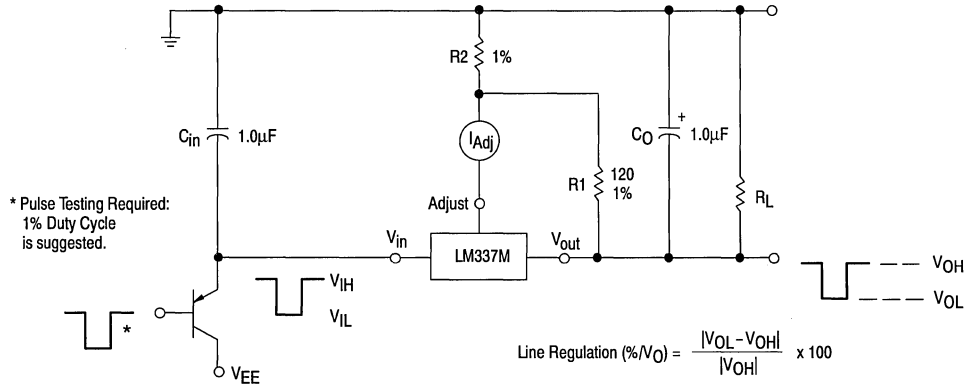
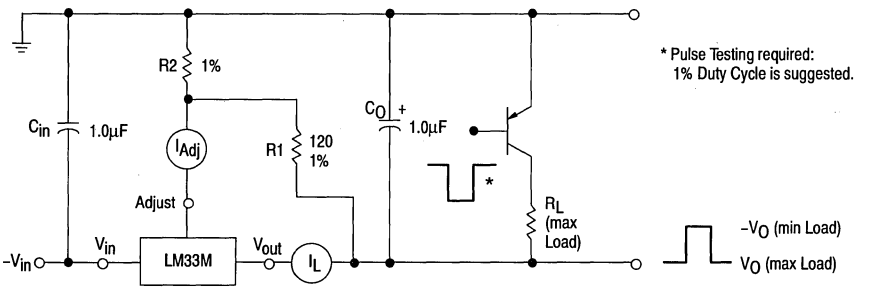


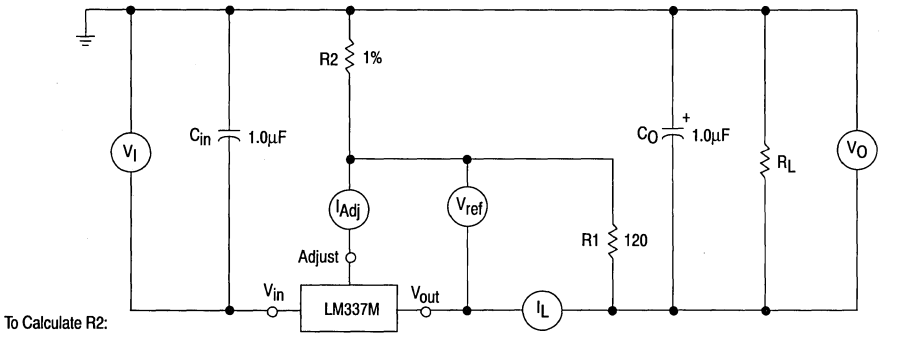
Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit



Load Regulation (mV) = V_O (min Load) − V_O (max Load)

Load Regulation (%/V_O) = $\frac{V_O \text{ (min Load)} - V_O \text{(max Load)}}{V_O \text{ (min Load)}}$ x 100

Figure 3. Standard Test Circuit



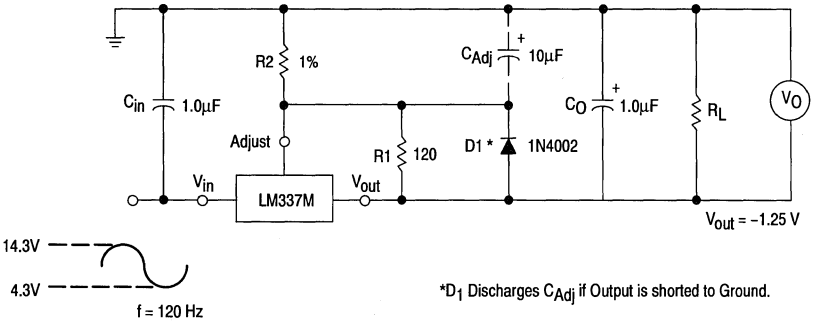
To Calculate R2:

$R2 = \left(\frac{V_O}{V_{ref}} - 1\right) R_1$

This assumes I_{Adj} is neglible.

Pulse Testing Required: 1% Duty Cycle is suggested.

Figure 4. Ripple Rejection Test Circuit



*D_1 Discharges C_{Adj} if Output is shorted to Ground.

Figure 5. Load Regulation

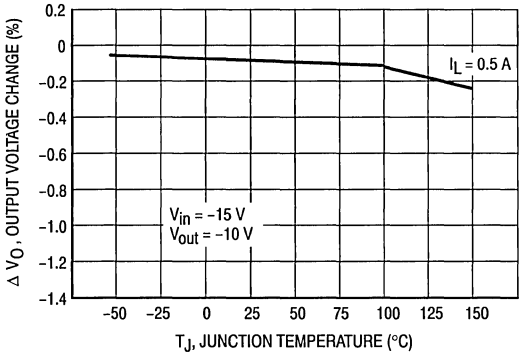


Figure 6. Current Limit

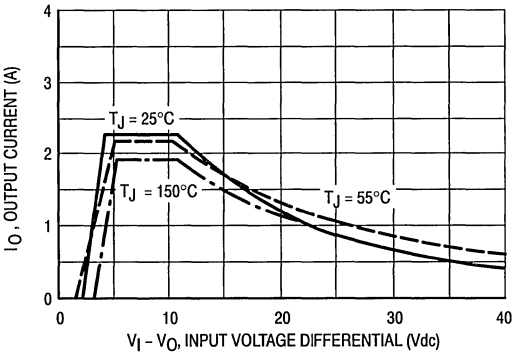


Figure 7. Adjustment Pin Current

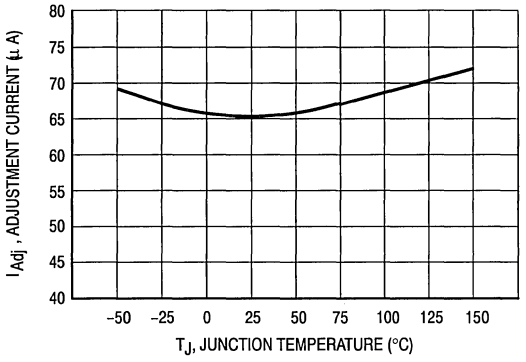


Figure 8. Dropout Voltage

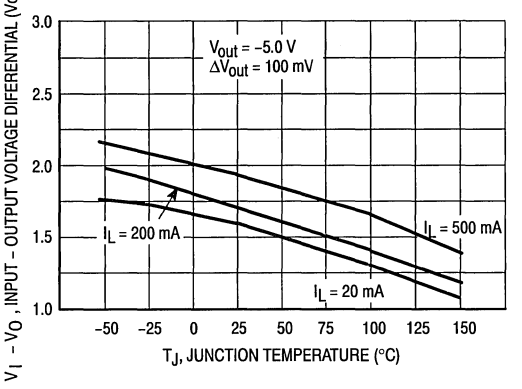


Figure 9. Temperature Stability

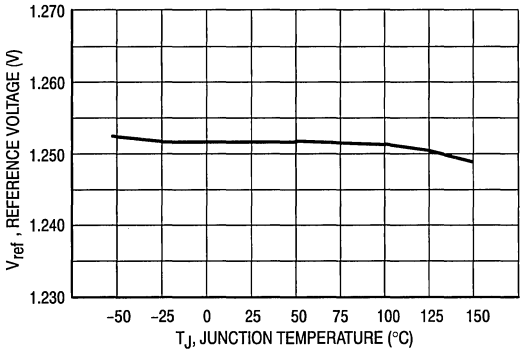


Figure 10. Minimum Operating Current

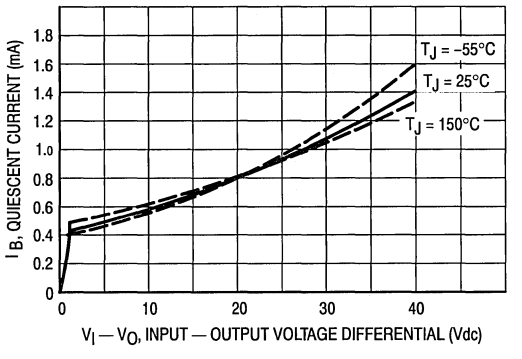


Figure 11. Ripple Rejection versus Output Voltage

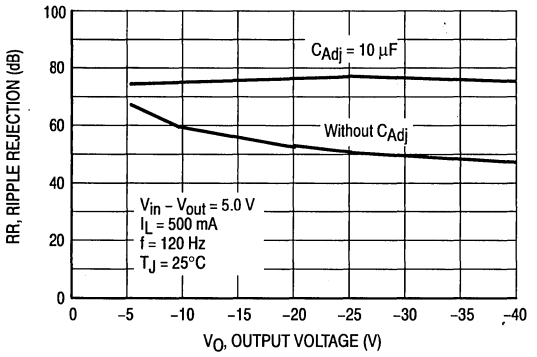


Figure 12. Ripple Rejection versus Output Current

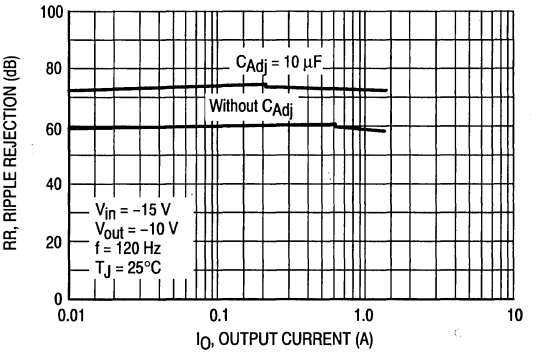


Figure 13. Ripple Rejection versus Frequency

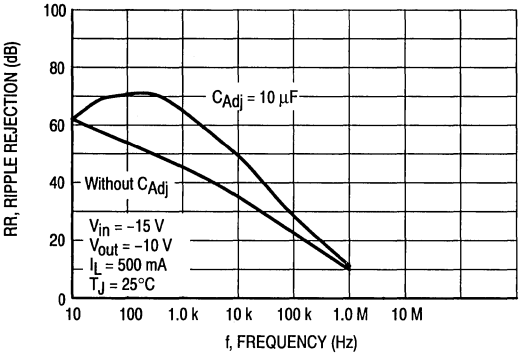


Figure 14. Output Impedance

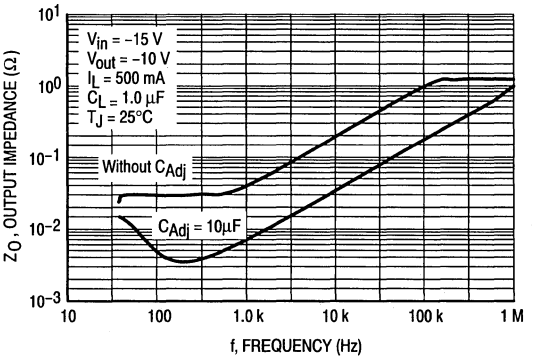


Figure 15. Line Transient Response

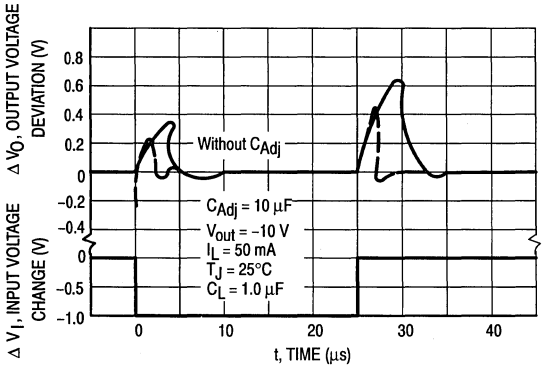
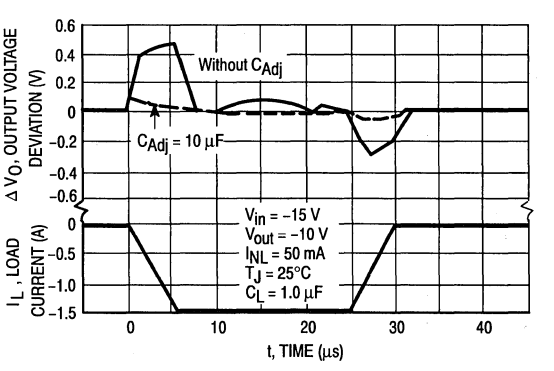


Figure 16. Load Transient Reponse



APPLICATIONS INFORMATION

Basic Circuit Operation

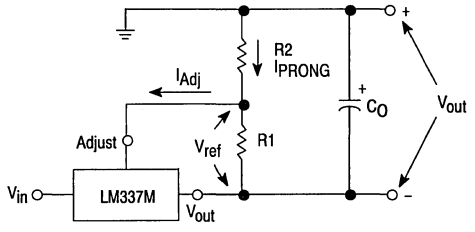
The LM337M is a three-terminal floating regulator. In operation, the LM337M develops and maintains a nominal –1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R1 (see Figure 17), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$Vout = Vref\ (1 + \frac{R2}{R1}) + I_{Adj}\ R2$$

Since the current into the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM337M was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM337M is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



V_{ref} = –1.25 V Typically

Load Regulation

The LM337M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 1.0 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

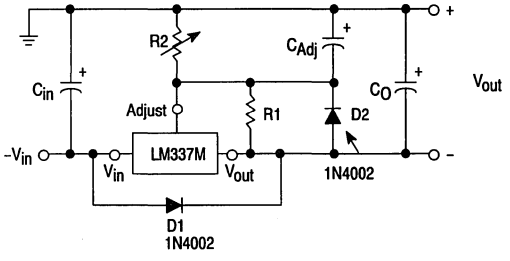
An output capacitance (C_O) in the form of a 1.0 μF tantalum or 10 μF aluminum electrolytic capacitor is required for stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM337M with the recommended protection diodes for output voltages in excess of –25 V or high capacitance values (C_O > 25 μF, C_{Adj} > 10 μF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D1 and D2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes



LM2931 Series

3

Low Dropout Voltage Regulators

The LM2931 series consists of positive fixed and adjustable output voltage regulators that are specifically designed to maintain proper regulation with an extremely low input-to-ouput voltage differential. These devices are capable of supplying output currents in excess of 100 mA and feature a low bias current of 0.4 mA at 10 mA output.

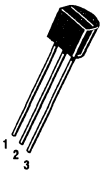
Designed primarily to survive in the harsh automotive environment, these devices will protect all external load circuitry from input fault conditions caused by reverse battery connection, two battery jump starts, and excessive line transients during load dump. This series also includes internal current limiting, thermal shutdown, and additionally, is able to withstand temporary power-up with mirror-image insertion.

Due to the low dropout voltage and bias current specifications, the LM2931 series is ideally suited for battery powered industrial and consumer equipment where an extension of useful battery life is desirable. The 'C' suffix adjustable output regulators feature an output inhibit pin which is extremely useful in microprocessor-based systems.

- Input-to-Output Voltage Differential of Less Than 0.6 V at 100 mA
- Output Current in Excess of 100 mA
- Low Bias Current
- 60 V Load Dump Protection
- –50 V Reverse Transient Protection
- Internal Current Limiting with Thermal Shutdown
- Temporary Mirror-Image Protection
- Ideally Suited for Battery Powered Equipment

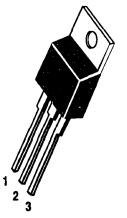
Z SUFFIX
PLASTIC PACKAGE
CASE 29

PIN 1. Output
2. Ground
3. Input

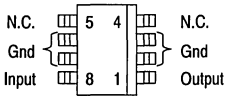


T SUFFIX
PLASTIC PACKAGE
CASE 221A
Heatsink surface
connected to Pin 2

PIN 1. Input
2. Ground
3. Output

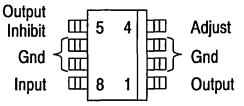


FIXED



(Top View)

ADJUSTABLE



(Top View)

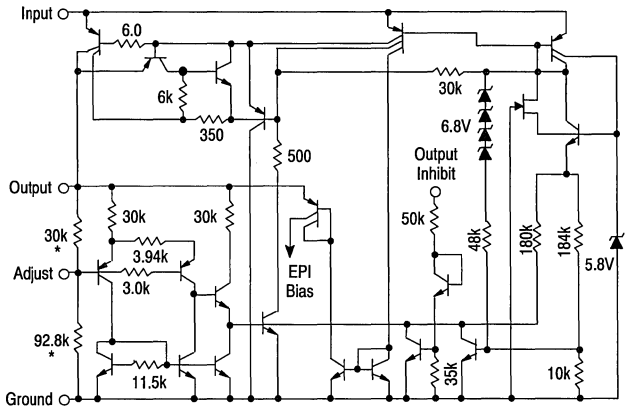
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP-8)

ADJUSTABLE

T SUFFIX
PLASTIC PACKAGE
CASE 314D
Heatsink surface
connected to Pin 2

PIN 1. Adjust
2. Output Inhibit
3. Ground
4. Input
5. Output

Internal Schematic



*Deleted on Adjustable Regulators

ORDERING INFORMATION

Device	Output Voltage	Output Tolerance	Package
LM2931AD-5.0	5.0 V	±3.8%	SO-8
LM2931AT-5.0	5.0 V	±3.8%	221A
LM2931AZ-5.0	5.0 V	±3.8%	29
LM2931D-5.0	5.0 V	±5.0%	SO-8
LM2931T-5.0	5.0 V	±5.0%	221A
LM2931Z-5.0	5.0 V	±5.0%	29
LM2931CD	Adjustable	±5.0%	SO-8
LM2931CT	Adjustable	±5.0%	314D

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Continuous	V_I	40	Vdc
Transient Input Voltage ($\tau \leq 100$ ms)	$V_I(\tau)$	60	Vpk
Transient Reverse Polarity Input Voltage 1.0% Duty Cycle, $\tau \leq 100$ ms	$-V_I(\tau)$	–50	Vpk
Power Dissipation			
Case 29 (TO-92)			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance Junction to Ambient	θ_{JA}	178	°C/W
Thermal Resistance Junction to Case	θ_{JC}	83	°C/W
Case 751 (SOP-8)			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance Junction to Ambient	θ_{JA}	180	°C/W
Thermal Resistance Junction to Case	θ_{JC}	45	°C/W
Case 221A and 314D (TO-220 Type)			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance Junction to Ambient	θ_{JA}	65	°C/W
Thermal Resistance Junction to Case	θ_{JC}	5.0	°C/W
Tested Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERICISTICS (V_{in} = 14 V, I_O = 10 mA, C_O = 100 µF, $C_{O(ESR)}$ = 0.3 Ω, T_J = 25°C, Note 1, unless otherwise noted.)

Characteristics	Symbol	LM2931A-5.0			LM2931-5.0			Unit
		Min	Typ	Max	Min	Typ	Max	
FIXED OUTPUT								
Output Voltage	V_O							V
V_{in} = 14 V, I_O = 10 mA, T_J = 25°C		4.81	5.0	5.19	4.75	5.0	5.25	
V_{in} = 6.0 V to 26 V, $I_O \leq 100$ mA, T_J = –40° to 125°C		4.75	—	5.25	4.50	—	5.50	
Line Regulation	Reg_{line}							mV
V_{in} = 9.0 V to 16 V		—	2.0	10	—	2.0	10	
V_{in} = 6.0 V to 26 V		—	4.0	30	—	4.0	30	
Load Regulation (I_O = 5.0 mA to 100 mA)	Reg_{load}	—	14	50	—	14	50	mV
Output Impedance I_O = 10 mA, ΔI_O = 1.0 mA, f = 100 Hz to 10 kHz	Z_O	—	200	—	—	200	—	mΩ
Bias Current	I_B							mA
V_{in} = 14 V, I_O = 100 mA, T_J = 25°C		—	5.8	30	—	5.8	30	
V_{in} = 6.0 V to 26 V, I_O = 10 mA, T_J = –40° to 125°C		—	0.4	1.0	—	0.4	1.0	
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	—	700	—	—	700	—	µVrms
Long-Term Stability	S	—	20	—	—	20	—	mV/kHR
Ripple Rejection (f = 120 Hz)	RR	60	90	—	60	90	—	dB
Dropout Voltage	V_I-V_O							V
I_O = 10 mA		—	0.015	0.2	—	0.015	0.2	
I_O = 100 mA		—	0.16	0.6	—	0.16	0.6	
Over-Voltage Shutdown Threshold	$V_{th(OV)}$	26	29.5	40	26	29.5	40	V
Output Voltage with Reverse Polarity Input (V_{in} = –15 V)	$-V_O$	–0.3	0	—	–0.3	0	—	V

NOTES: 1. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. The reference voltage on the adjustable device is measured from the output to the adjust pin across R_1.

ELECTRICAL CHARACTERICISTICS (V_{in} = 14 V, V_O = 3.0 V, I_O = 10 mA, R_1 = 27 k, C_O = 100 µF, $C_{O(ESR)}$ = 0.3 Ω, T_J = 25°C, Note 1, unless otherwise noted.)

Characteristics	Symbol	LM2931C Min	LM2931C Typ	LM2931C Max	Unit
ADJUSTABLE OUTPUT					
Reference Voltage (Note 2, Figure 18) I_O = 10 mA, T_J = 25°C $I_O \leq$ 100 mA, T_J = –40 to 125°C	V_{ref}	 1.14 1.08	 1.20 —	 1.26 1.32	V
Output Voltage Range	$V_{O\ range}$	3.0	2.7 to 29.5	24	V
Line Regulation (V_{in} = V_O + 0.6 V to 26 V)	Reg_{line}		0.2	1.5	mV/V
Load Regulation (I_O = 5.0 mA to 100 mA)	Reg_{load}	—	0.3	1.0	%/V
Output Impedance I_O = 10 mA, ΔI_O = 1.0 mA, f = 10 Hz to 10 kHz	Z_O	—	40	—	mΩ/V
Bias Current I_O = 100 mA I_O = 10 mA Output Inhibited ($V_{th(OI)}$ = 2.5 V)	I_B	 — — —	 6.0 0.4 0.2	 — 1.0 1.0	mA
Adjustment Pin Current	I_{Adj}	—	0.2	—	µA
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	—	140	—	µVrms/V
Long-Term Stability	S	—	0.4	—	%/kHR
Ripple Rejection (f = 120 Hz)	RR	0.10	0.003	—	%/V
Dropout Voltage I_O = 10 mA I_O = 100 mA	V_I-V_O	 — —	 0.015 0.16	 0.2 0.6	V
Over-Voltage Shutdown Threshold	$V_{th(OV)}$	26	29.5	40	V
Output Voltage with Reverse Polarity Input (V_{in} = –15 V)	$-V_O$	–0.3	0	—	V
Output Inhibit Threshold Voltages Output "On," T_J = 25°C T_J = –40° to 125°C Output "Off," T_J = 25°C T_J = –40° to 125°C	$V_{th(OI)}$	 — — 2.50 3.25	 2.15 — 2.26 —	 1.90 1.20 — —	V
Output Inhibit Threshold Current ($V_{th(OI)}$ = 2.5 V)	$I_{th(OI)}$	—	30	50	µA

NOTES: 1. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. The reference voltage on the adjustable device is measured from the output to the adjust pin across R_1.

DEFINITIONS

Dropout Voltage — The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output decreases 100 mV from nominal value at 14 V input, dropout voltage is affected by junction temperature and load current.

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Bias Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long-Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices electrical characteristics and maximum power dissipation.

Figure 1. Dropout Voltage versus Output Current

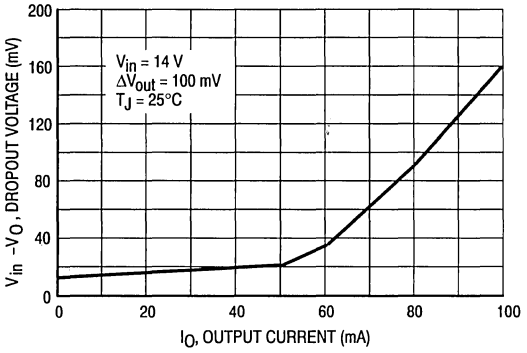


Figure 2. Dropout Voltage versus Junction Temperature

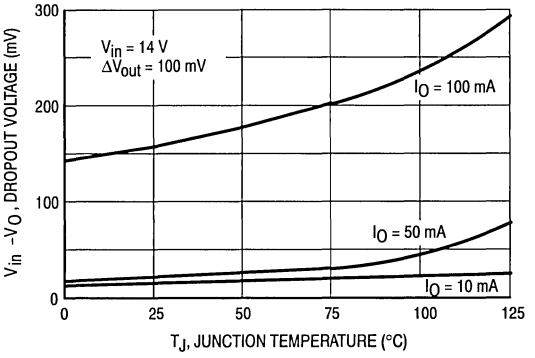


Figure 3. Peak Output Current versus Input Voltage

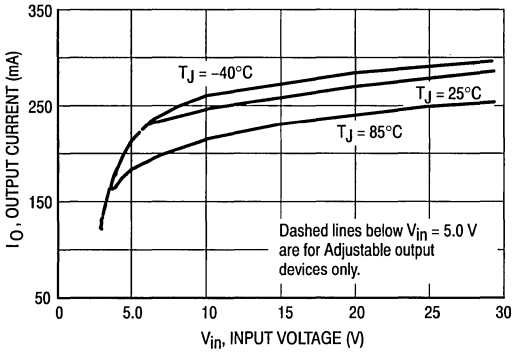


Figure 4. Output Voltage versus Input Voltage

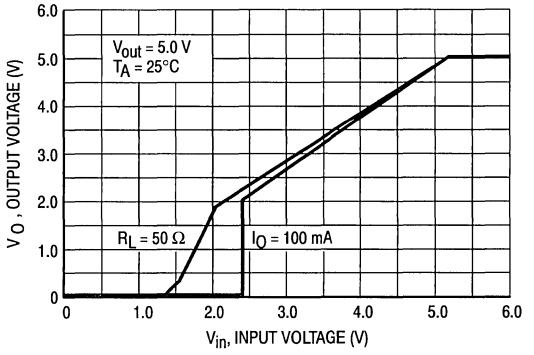


Figure 5. Output Voltage versus Input Voltage

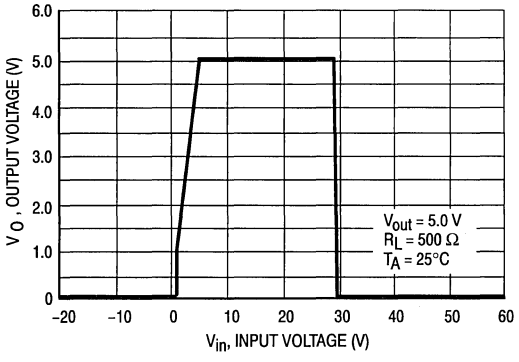


Figure 6. Load Dump Characteristics

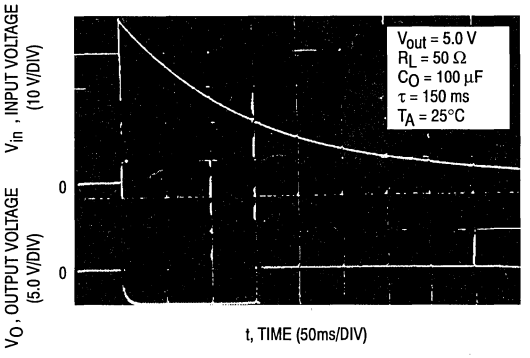


Figure 7. Bias Current versus Input Voltage

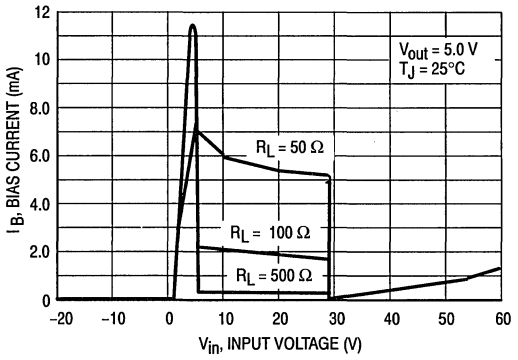


Figure 8. Bias Current versus Output Current

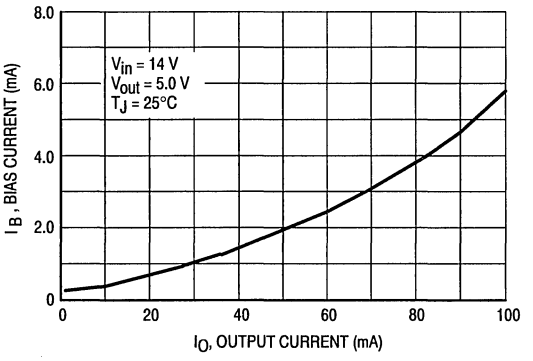


Figure 9. Bias Current versus Junction Temperature

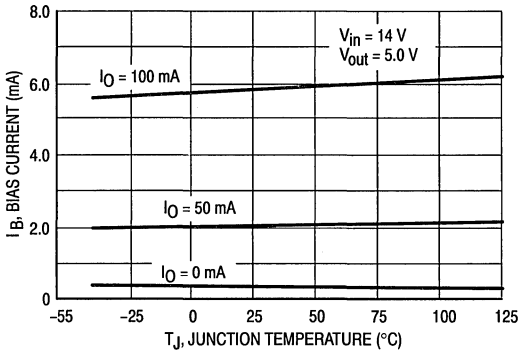


Figure 10. Output Impedance versus Frequency

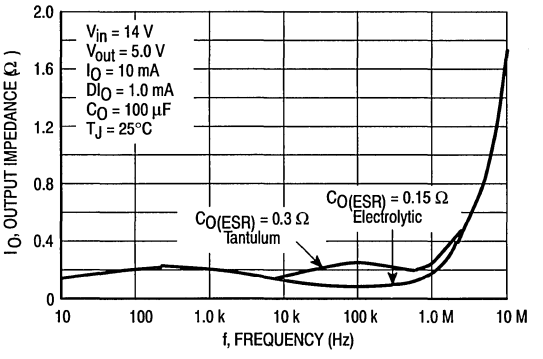


Figure 11. Ripple Rejection versus Frequency

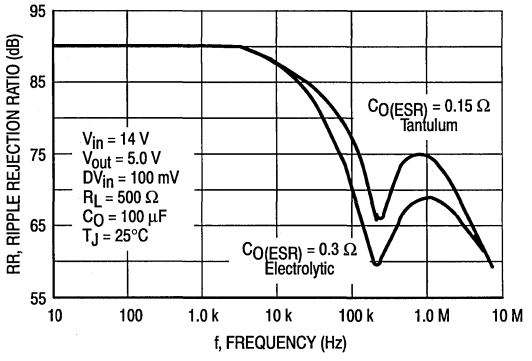


Figure 12. Ripple Rejection versus Output Current

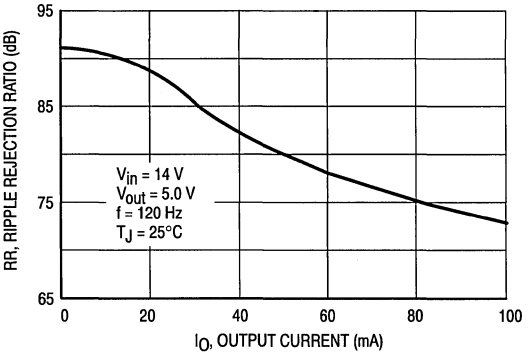


Figure 13. Line Regulation

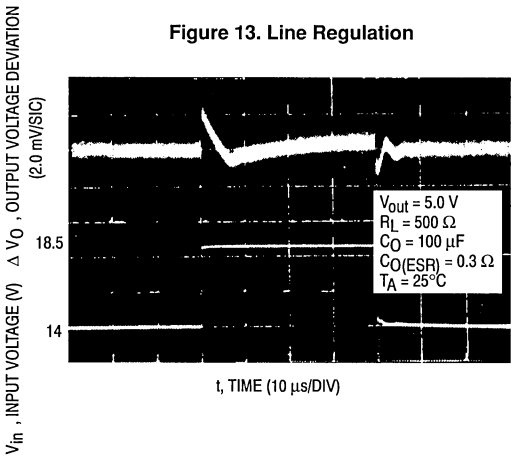


Figure 14. Load Regulation

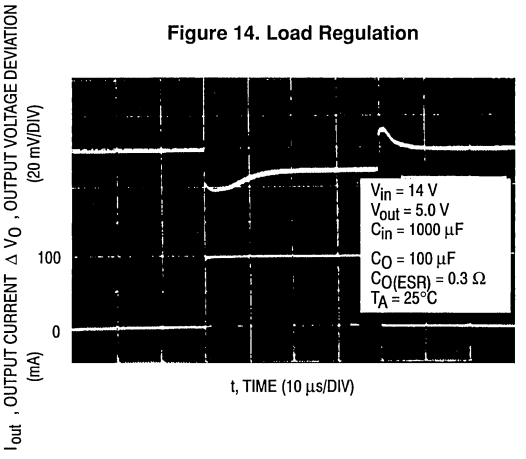


Figure 15. Reference Voltage versus Output Voltage

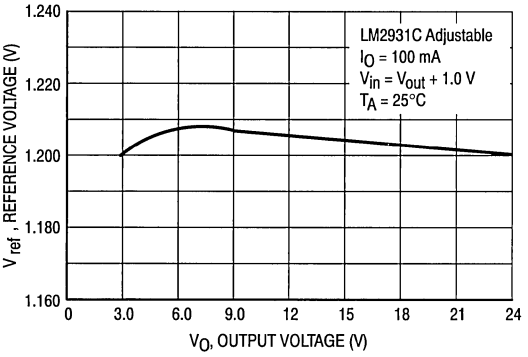
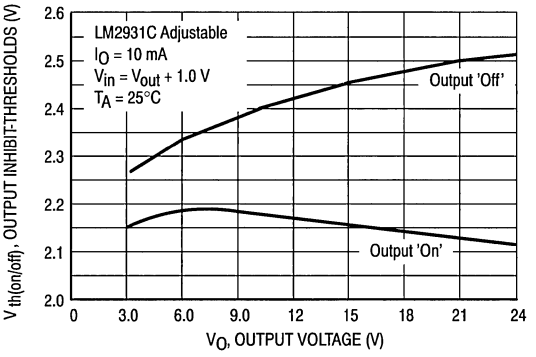


Figure 16. Output Inhibit-Thresholds versus Output Voltage



APPLICATIONS INFORMATION

The LM2931 series regulators are designed with many protection features making them essentially blow-out proof. These features include internal current limiting, thermal shutdown, overvoltage and reverse polarity input protection, and the capability to withstand temporary power-up with mirror-image insertion. Typical application circuits for the fixed and adjustable output device are shown in Figures 17 and 18.

The input bypass capacitor C_{in} is recommended if the regulator is located an appreciable distance (≥ 4″) from the supply input filter. This will reduce the circuit's sensitivity to the input line impedance at high frequencies.

This regulator series is not internally compensated and thus requires an external output capacitor for stability. The capacitance value required is dependent upon the load current, output voltage for the adjustable regulator, and the type of capacitor selected. The least-stable condition is encountered at maximum load current and minimum output voltage. Figure 22 shows that for operation in the "Stable" region, under the conditons specified, the magnitude of the output capacitor impedance $|Z_O|$ must not exceed 0.4 Ω. This limit must be observed over the entire operating temperature range of the regulator circuit.

With economical electrolytic capacitors, cold temperature operation can pose a serious stability problem. As the electrolyte freezes, around –30°C, the capacitance will decrease and the equivalent series resistance (ESR) will increase drastically, causing the circuit to oscillate. Quality electrolytic capacitors with extended temperature ranges of –40° to 85°C and –55° to 105°C are readily available. Solid tantalum capacitors may be a better choice if small size is a requirement, however, the maximum $|Z_O|$ limit over temperature must be observed.

Note that in the stable region, the output noise voltage is linearly proportional to $|Z_O|$. In effect, C_O dictates the high frequency roll-off point of the circuit. Operation in the area titled "Marginally Stable" will cause the output of the regulator to exhibit random bursts of oscillation that decay in an under-damped fashion. Continuous oscillation occurs when operating in the area titled "Unstable." It is suggested that oven testing of the entire circuit be performed with maximum load, minimum input voltage, and minimum ambient temperature.

Figure 17. Fixed Output Regulator

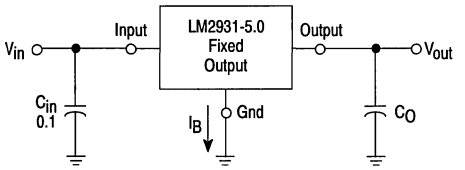
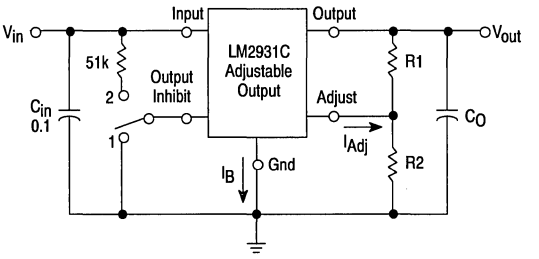


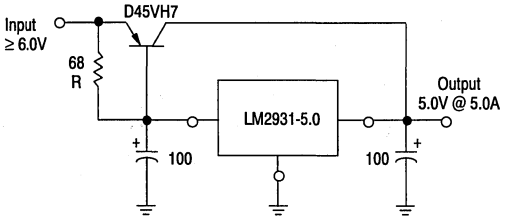
Figure 18. Adjustable Output Regulator



Switch Position 1 = Output "On," 2 = Output "Off"

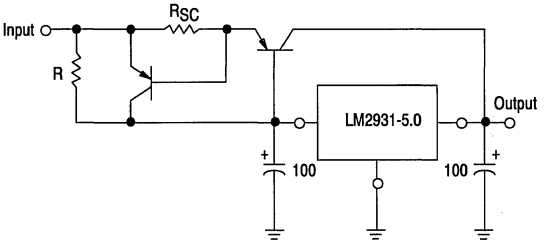
$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right) + I_{Adj}\ R2 \qquad 22.5\ k \geq \frac{R1\ R2}{R1 + R2}$$

Figure 19. 5.0 A Low Differential Voltage Regulator



The LM2931 series can be current boosted with a PNP transistor. The D45VH7, on a heatsink, will provide an output current of 5.0 A with an input to output voltage differential of approximately 1.0 V. Resistor R in conjuction with the V_{BE} of the PNP determines when the pass transistor begins conducting. This circuit is not short circuit proof.

Figure 20. Current Boost Regulator with Short Circuit Projection



The circuit of Figure 19 can be modified to provide supply protection against short circuits by adding the current sense resistor R_{SC} and an additional PNP transistor. The current sensing PNP must be capable of handling the short circuit current of the LM2931. Safe operating area of both transistors must be considered under worst case conditions.

Figure 21. Constant Intensity Lamp Flasher

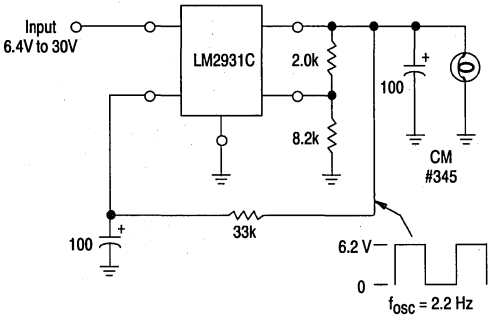
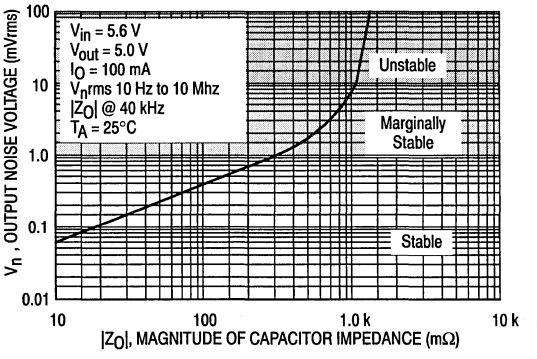


Figure 22. Output Noise Voltage versus Output Capacitor Impedance



LM2935

Advance Information

Low Dropout Dual Regulator

**LOW DROPOUT
DUAL REGULATOR**

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

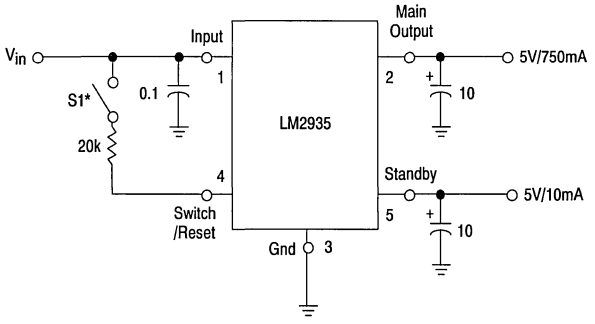
The LM2935 is a dual positive 5.0 V low dropout voltage regulator, designed for standby power systems. The Main Output is capable of supplying 750 mA for microprocessor power, and can be turned on and off by the Switch/Reset input. The other output is dedicated for standby operation of volatile memory, and is capable of supplying up to 10 mA loads. The total device features a low quiescent current of 3.0 mA or less when supplying 10 mA from the Standby Output.

This part was designed for harsh automotive environments and is therefore immune to many input supply voltage problems such as reverse battery (–12 V), double battery (+24 V), and load dump transients (+60 V).

- Two Regulated 5.0 V Outputs
- Main Output Current in Excess of 750 mA
- On/Off Control of Main Output
- Standby Output Current in Excess of 10 mA
- Low Input-Output Differential of Less Than 0.6 V at 500 mA
- Short Circuit Current Limiting
- Internal Thermal Shutdown
- Low Voltage Indicator Output
- Designed for Automotive Environment Including
  - Reverse Battery Protection
  - Double Battery Protection
  - Load Dump Protection
  - Reverse Transient Protection
- Five Pin TO-220 Package

T SUFFIX
PLASTIC PACKAGE
CASE 314D
(5 LEAD TO-220 TYPE)

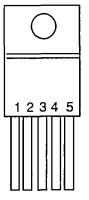
Typical Application Circuit



*Note: The Main Output is "OFF" with switch S1 open.

An input bypass capacitor is recommended if the regulator is located more than 4″ from the supply input filter. The LM2935 is not internally compensated and thus requires an external output capacitor for stability. A minimum capacitance of 10 μF is recommended. The actual capacitance value is dependent upon load current, temperature, and the capacitor's equivalent series resistance (ESR). The least stable condition is encountered at maximum load current and minimum ambient temperature.

PIN CONNECTIONS



PIN 1. Input
2. Main Output
3. Ground
4. Switch/Reset
5. Standby output

Heatsink surface connected to Pin 2

ORDERING INFORMATION

Device	Operating Junction Temperature Range	Package
LM2935	–40° to +125°C	Plastic Power

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Continuous	V_I	60	Vdc
Transient Reverse Polarity Input Voltage 1.0% Duty Cycle, $\tau \leq 100$ ms	$-V_I(\tau)$	–50	Vpk
Switch/Reset Input Current	I_{in}	5.0	mA
Power Dissipation and Thermal Characteristics Case 314D (TO-220) T Suffix Maximum Power Dissipation Thermal Resistance Junction to Air Thermal Resistance Junction to Case (Pin 3)	 P_D θ_{JA} θ_{JC}	 Internally Limited 62.5 1.9	 W °C/W °C/W
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERICISTICS (V_{in} = 14 V, I_O = 500 mA, I_{stby} = 0 mA, C_O = 10 µF, C_{stby} = 10 µF, T_J = 25°C, Note 1, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
MAIN OUTPUT					
Output Voltage V_{in} = 6.0 V to 26 V, I_O = 5.0 mA to 500 mA, T_J = –40 to 125°C	V_O	4.75	5.0	5.25	V
Line Regulation V_{in} = 9.0 V to 16 V, I_O = 5.0 mA V_{in} = 6.0 V to 26 V, I_O = 5.0 mA	Reg_{line}	 — —	 4.0 10	 25 50	mV
Load Regulation (I_O = 5.0 mA to 500 mA)	Reg_{load}	—	10	50	mV
Output Impedance I_O = 500 mAdc and 10 mArms, f = 100 Hz to 10 kHz	Z_O	—	200	—	mΩ
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	—	100	—	µVrms
Long Term Stability	S	—	20	—	mV/kHR
Ripple Rejection (f = 120 Hz)	RR	—	66	—	dB
Dropout Voltage I_O = 500 mA I_O = 750 mA	V_I-V_O	 — —	 0.45 0.82	 0.6 —	V
Short Circuit Current Limit	I_{SC}	0.75	1.2	—	A
Over-Voltage Shutdown Threshold	$V_{th(OV)}$	26	31	—	V
SWITCH/RESET					
Output Sink Current (V_{OL} = 1.2 V)	I_{Sink}	—	5.0	—	mA
Output Voltage ($R_{On/Off}$ = 20 kΩ) Low State, V_{in} = 4.0 V High State, V_{in} = 14 V	 V_{OL} V_{OH}	 — 4.5	 0.9 5.0	 1.2 6.0	V
Output Pull-Up Resistor, On/Off (Note 2)	$R_{On/Off}$	—	20	30	kΩ
Output Voltage with Reverse Polarity Input (V_{in} = –15 V, R_L = 10 Ω)	$-V_O$	–0.6	0	—	V

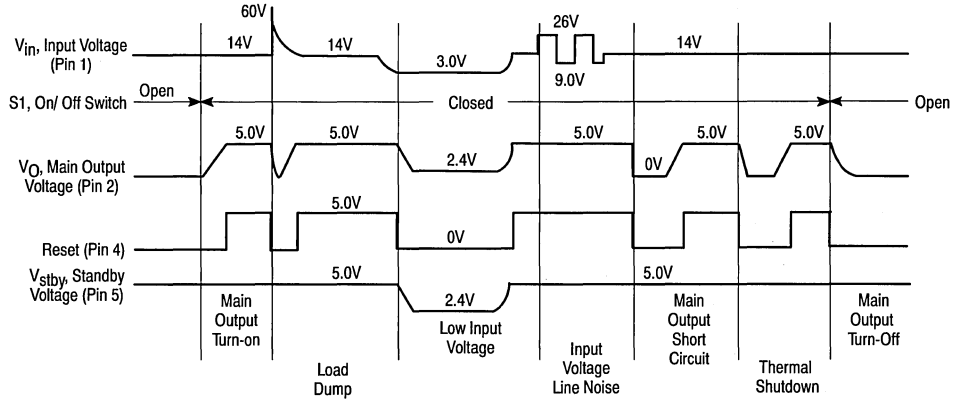
NOTES: 1. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. The maximum switch/reset current must not exceed 5.0 mA.

ELECTRICAL CHARACTERICISTICS (V_{in} = 14 V, I_O = 0 mA, I_{stby} = 10 mA, C_O = 10 µF, C_{stby} = 10 µF, T_J = 25°C, Note 1, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
STANDBY OUTPUT					
Output Voltage V_{in} = 6.0 V to 26 V, I_{stby} = 1.0 mA to 10 mA, T_J = –40 to 125°C	$V_{O(stby)}$	4.75	5.0	5.25	V
Tracking Voltage	V_O-$V_{O(stby)}$	–200	0	200	mV
Line Regulation (V_{in} = 6.0 V to 26 V)	Reg_{line}	—	4.0	50	mV
Load Regulation (I_{stby} = 1.0 mA to 10 mA)	Reg_{load}	—	10	50	mV
Output Impedance $I_{(stby)}$ = 10 mAdc and 1.0 mArms, f = 100 Hz to 10 kHz	$Z_{O(stby)}$	—	1.0	—	Ω
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	—	300	—	µVrms
Long Term Stability	S	—	20	—	mV/kHR
Ripple Rejection (f = 120 Hz)	RR	—	66	—	dB
Dropout Voltage (I_{stby} = 10 mA)	V_I-$V_{O(stby)}$	—	0.55	0.7	V
Short Circuit Current Limit	I_{SC}	25	70	—	mA
Output Voltage with Reverse Polarity Input (V_{in} = –15 V, R_L = 510 Ω)	$-V_O$	–0.3	0	—	V
Output Voltage with Maximum Positive Input V_{in} = 60 V, R_L = 510 Ω	$V_{O(max)}$	—	5.0	6.0	V
TOTAL DEVICE					
Bias Current	I_B				mA
I_O = 10 mA, I_{stby} = 0 mA		—	3.0	—	
I_O = 500 mA, I_{stby} = 0 mA		—	40	100	
I_O = 750 mA, I_{stby} = 0 mA		—	90	—	
Main Output "Off", I_{stby} = 10 mA		—	2.0	3.0	

NOTES: 1. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

TYPICAL CIRCUIT WAVEFORMS



LP2950
LP2951

3

Product Preview

Micropower Voltage Regulators

LOW DROPOUT MICROPOWER VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

The LP2950 and LP2951 are micropower voltage regulators that are specifically designed to maintain proper regulation with an extremely low input-to-output voltage differential. These devices feature a very low quiescent bias current of 75 μA and are capable of supplying output currents in excess of 100 mA. Internal current and thermal limiting protection is provided.

The LP2951 has three additional features. The first is the $\overline{\text{Error}}$ Output that can be used to signal external circuitry of an out of regulation condition, or as a microprocessor power-on reset. The second feature allows the output voltage to be preset to 5.0 V or programmed from 1.23 V to 29 V. It consists of a pinned-out resistor divider along with direct access to the Error Amplifier feedback input. The third feature is a Shutdown input that allows a logic level signal to turn-off or turn-on the regulator output.

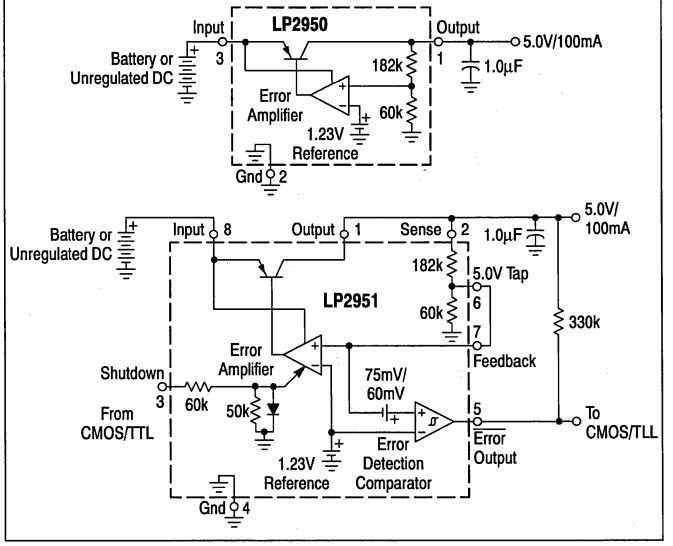
Due to the low input-to-output voltage differential and bias current specifications, these devices are ideally suited for battery powered computers, consumer and industrial equipment where an extension of useful battery life is desirable. The "A" suffix devices feature an initial output voltage tolerance ± 0.5%.

- Low Quiescent Bias Current of 75 μA
- Low Input-to-Output Voltage Differential: 50 mV @ 100 μA, 380 mV @ 100 mA
- 5.0 V ± 0.5% Allows Use as a Regulator or Reference
- Extremely Tight Line and Load Regulation
- Requires Only a 1.0 μF Output Capacitor for Stability
- Internal Current and Thermal Limiting

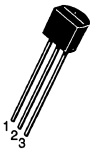
LP2951 Additional Features:

- $\overline{\text{Error}}$ Output Signals an Out of Regulation Condition
- Output Programmable from 1.23 V to 29 V
- Logic Level Shutdown Input

Simplified Block Diagrams



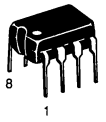
Z SUFFIX
PLASTIC PACKAGE
CASE 29
(TO-92)



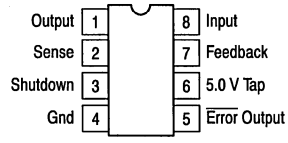
Pin 1. Output
2. Ground
3. Input

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

N SUFFIX
PLASTIC PACKAGE
CASE 626



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
LP2950ACZ – 5.0	– 40° to +125°C	TO-92
LP2950CZ – 5.0		TO-92
LP2951ACD – 5.0/ADJ		SO-8
LP2951CD – 5.0/ADJ		SO-8
LP2951ACN – 5.0/ADJ		Plastic
LP2951CN – 5.0/ADJ		Plastic

MC1468
MC1568

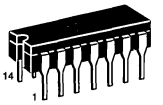
Dual ±15 Volt Tracking Regulator

The MC1468/1568 is a dual polarity tracking regulator designed to provide balanced positive and negative output voltages at currents to 100 mA. Internally, the device is set for ±15 V outputs but an external adjustment can be used to change both outputs simultaneously from 8.0 V to 20 V. Input voltages up to ±30 V can be used and there is provision for adjustable current limiting.

- Internally Set to ±15 V Tracking Outputs
- Output Currents to 100 mA
- Outputs Balanced to within 1.0% (MC1568)
- Line and Load Regulation of 0.06%
- 1.0% Max Output Variation Due to Temperature Changes
- Standby Current Drain of 3.0 mA
- Externally Adjustable Current Limit
- Remote Sensing Provisions

DUAL ±15 VOLT TRACKING REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

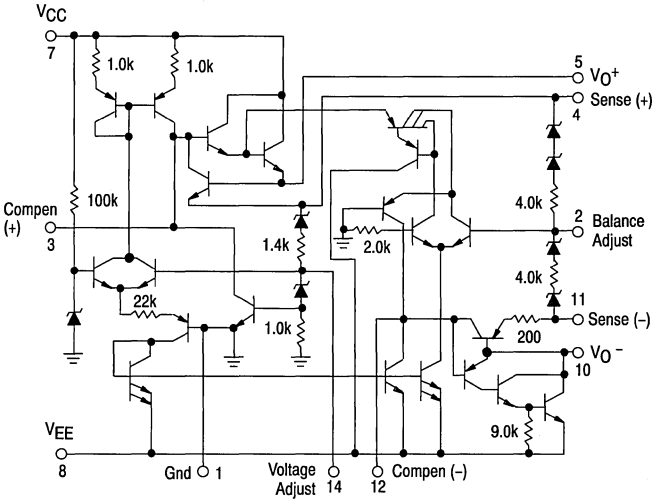


L SUFFIX
CERAMIC PACKAGE
CASE 632

ORDERING INFORMATION

Device	Temperature Range	Package
MC1468L	0° to + 70°C	Ceramic DIP
MC1568L	–55° to + 125°C	Ceramic DIP

Circuit Schematic



MAXIMUM RATINGS (T_C = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_{CC},$\lvert V_{EE}\rvert$	30	Vdc
Peak Load Current	I_{pk}	100	mA
Power Dissipation and Thermal Characteristics			
T_A = + 25°C	P_D	1.25	W
Derate above T_A = + 25°C	$1/\theta_{JA}$	10	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	100	°C/W
T_C = + 25°C	P_D	2.5	W
Derate above T_C = + 25°C	$1/\theta_{JC}$	20	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	50	°C/W
Storage Junction to Temperature Range	T_J, T_{stg}	−65 to +150	°C
Minimum Short Circuit Resistance	R_{SC}(min)	4.0	Ω
Ambient Temperature	T_A		°C
MC1468		0 to +70	
MC1568		−55 to +125	

ELECTRICAL CHARACTERICISTICS (V_{CC} = +20 V, V_{EE} = −20 V, C1 = C2 = 1500 pF, C3 = C4 = 1.0 µF, $R_{SC}+ = R_{SC}-$ = 4.0 Ω, $I_L+ = I_L-$ = 0, T_C = +25°C, unless otherwise noted, see Figure 1.)

Characteristics	Symbol	MC1568			MC1468			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	±14.5	±15	±15.5	±14.5	±15	±15.5	Vdc
Input Voltage	V_I	—	—	±30	—	—	±30	Vdc
Input-Output Voltage Differential	$\lvert V_I-V_O\rvert$	2.0	—	—	2.0	—	—	Vdc
Output Voltage Balance (L package only)	V_{Bal}	—	±50	±150	—	±50	±300	mV
Line Regulation Voltage	Reg_{line}							mV
(V_{in} = 18 V to 30 V)		—	—	10	—	—	10	
T_{low} to T_{high} (Note 1)		—	—	20	—	—	20	
Load Regulation Voltage	Reg_{load}							mV
(I_L = 0 mA to 50 mA, T_J = constant)		—	—	10	—	—	10	
(T_A = T_{low} to T_{high})		—	—	30	—	—	30	
Output Voltage Range	V_{OR}							Vdc
L Package (See Figure 4)		±8.0	—	±20	±8.0	—	±20	
Ripple Rejection (f = 120 Hz)	RR	—	75	—	—	75	—	dB
Output Voltage Temperature Stability (T_{low} to T_{high})	$\lvert TS_{VO}\rvert$	—	0.3	1.0	—	0.3	1.0	%
Short Circuit Current Limit (R_{SC} = 10 Ω)	I_{SC}	—	60	—	—	60	—	mA
Output Noise Voltage (BW = 100 Hz–10 kHz)	V_n	—	100	—	—	100	—	µV(RMS)
Positive Standby Current (V_{in} = +30 V)	I_{B+}	—	2.4	4.0	—	2.4	4.0	mA
Negative Standby Current (V_{in} = −30 V)	I_{B-}	—	1.0	3.0	—	1.0	3.0	mA
Long-Term Stability	$\Delta V_O/\Delta t$	—	0.2	—	—	0.2	—	%/k Hr.

NOTES: 1. T_{Low} to T_{High} = 0° to +70°C for MC1468
= −55° to +125°C for MC1568

APPLICATIONS INFORMATION

Compensation capacitors C1 and C2 must be located as close to the device as possible to prevent instablity due to noise pickup. Input bypass capacitors C_{in} are required if the device is located more than four inches from the power source filter capacitor. Output capacitor C4 is required for stability of the negative regulator. Capacitor C3 is used to improve the positive regulator load transient response. Low impedance quality capacitors are required when operating the MC1568 at its temperature extremes. Extended range ceramic, tantalum, and electrolytic capacitors are readily available from several manufacturers.

Capacitor values should be determined on a system by system basis. Input lead length, output load, temperature range, and printed circuit board layout are factors that will influence circuit performance. Typical values for capacitors C_{in}, C3, and C4 are 0.1 μF to 10 μF while C1 and C2 are 1500 pF.

The presence of Bal_{Adj}, pin 2, on devices housed in the dual in-line package (L suffix) allows the user to adjust the output voltages down to ±8.0 V. The required value of resistor R2 can be calculated from

$$R2 = \frac{R1\ R_{int}\ (\phi + V_Z)}{R_{int}\ (V_O - \phi - V_Z) - \phi\ R1}$$

where: R_{int} = An Internal Resistor = R1 = 1.0 kΩ
ϕ = 0.68 V
V_Z = 6.6 V

Some common design values are listed below:

±V_O(V)	R2	T_C V_O (%/°C)	I_B + (mA)
14	1.2 k	0.003	10
12	1.8 k	0.022	7.2
10	3.5 k	0.025	5.0
8.0	∞	0.028	2.6

Figure 1. Basic 50 mA Regulator

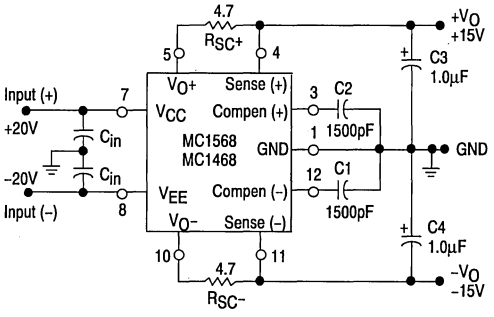
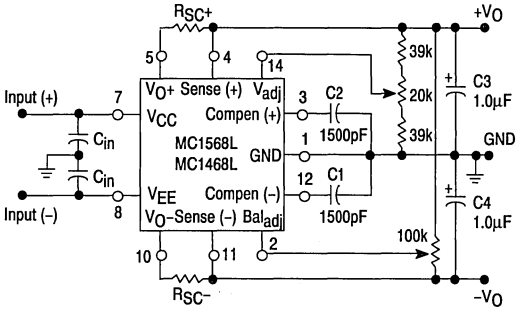


Figure 2. Voltage Adjust and Balance Adjust Circuit
(14.5 V ≤ V_{out} ≤ 20 V)



Balance adjust available in MC1568L, MC1468L ceramic dual-in-line package only.

Figure 3. ±1.5 A Regulator
(Short Circuit Protected, with Proper Heatsinking)

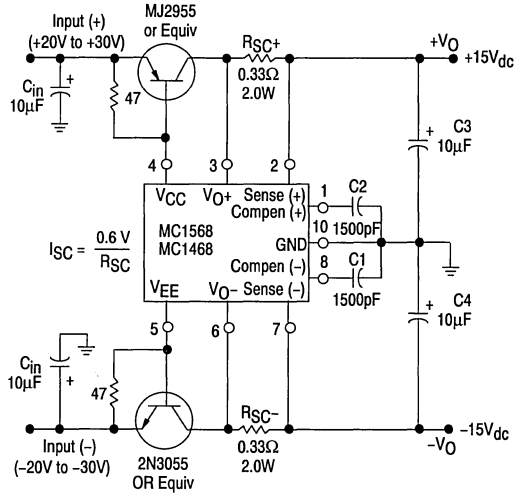
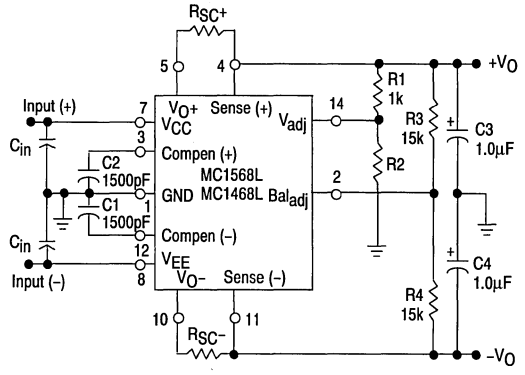


Figure 4. Output Voltage Adjustment for 8.0 V ≤ |±V_O| ≤ 14.5 V
(Ceramic-Packaged Devices Only)



3

Figure 5. Load Regulation

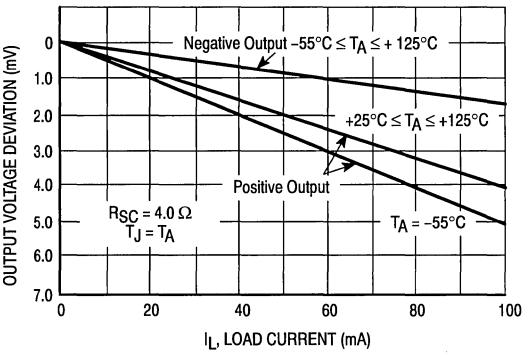


Figure 6. Regulator Dropout Voltage

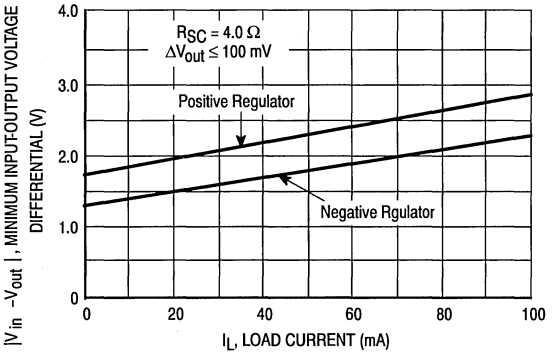


Figure 7. Maximum Current Capability

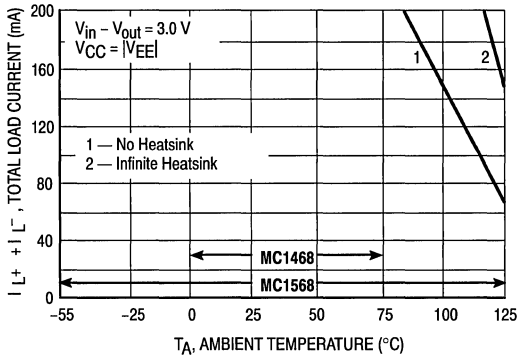


Figure 8. Maximum Current Capability

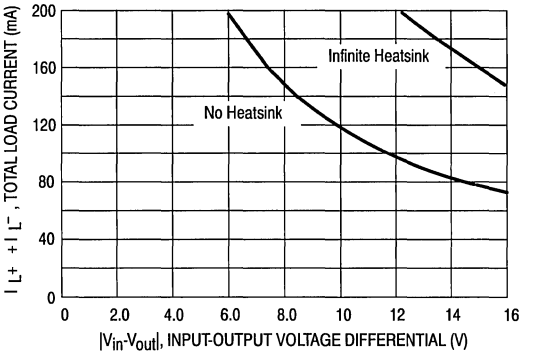


Figure 9. I_{SC} versus R_{SC}

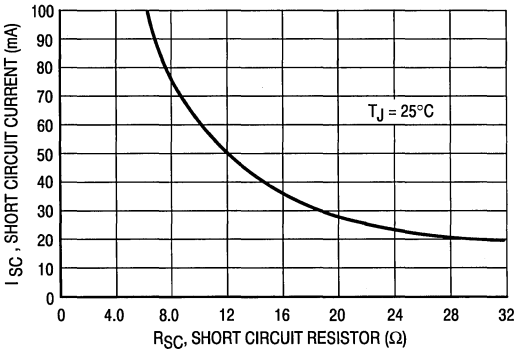


Figure 10. Current-Limiting Characteristics

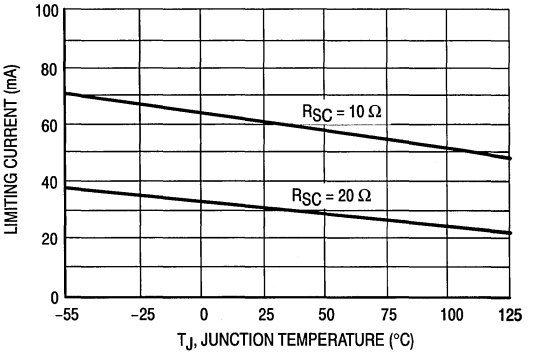


Figure 11. Standby Current Drain

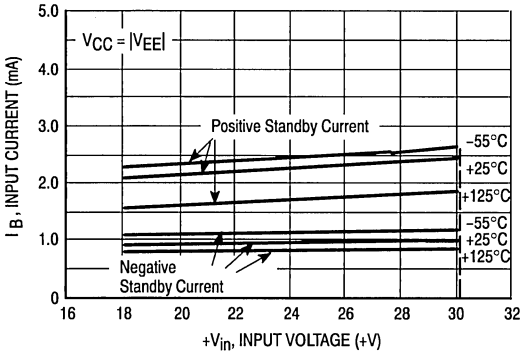


Figure 12. Standby Current Drain

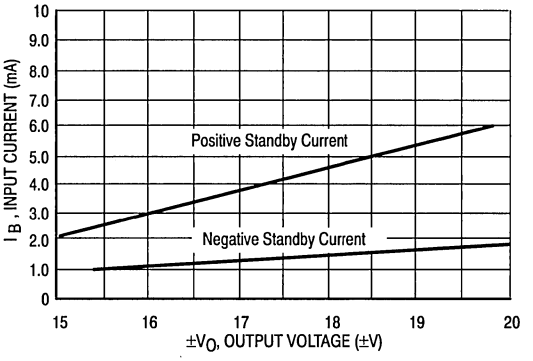


Figure 13. Temperature Coefficient of Output Voltage

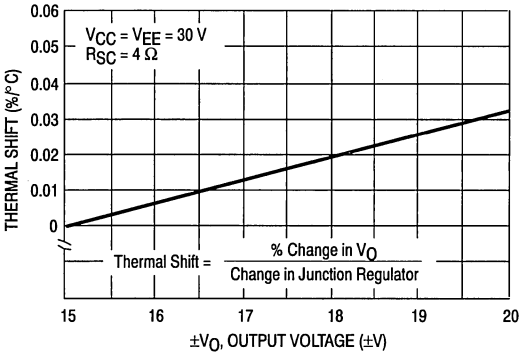


Figure 14. Load Transient Response

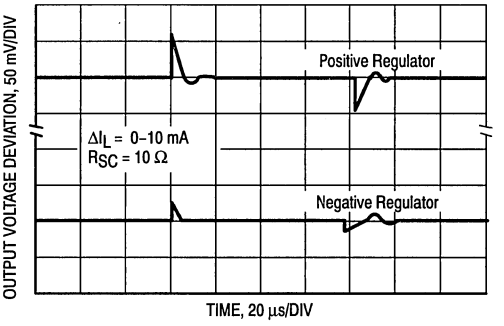


Figure 15. Line Transient Response

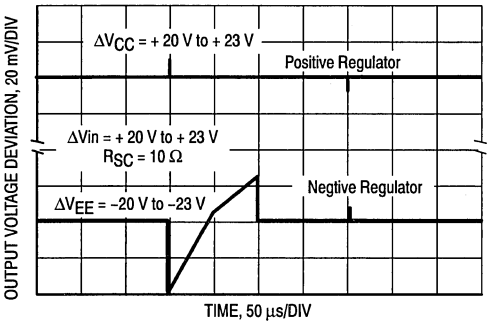


Figure 16. Ripple Rejection

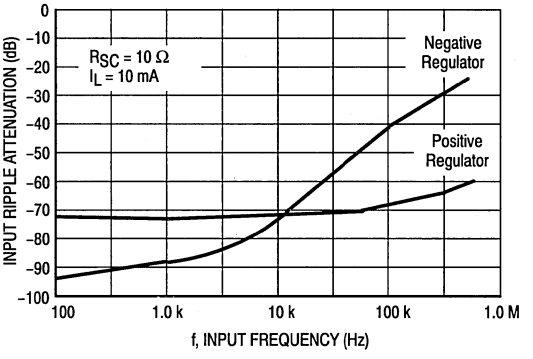
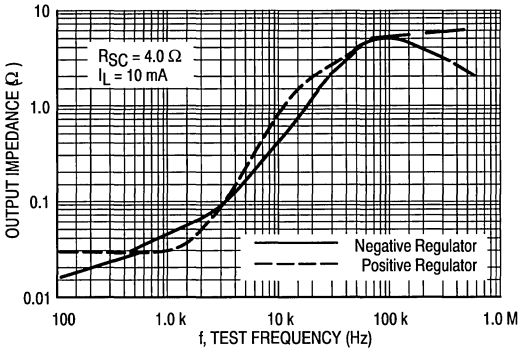


Figure 17. Output Impedance



MC1723
MC1723C

Voltage Regulator

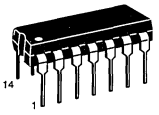
VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

3

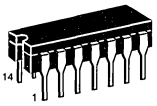
The MC1723 is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors. MC1723 is specified for operation over the military temperature range (–55° to +125°C) and the MC1723C over the commercial temperature range (0° to +70°C)

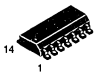
- Output Voltage Adjustable from 2.0 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line and 0.03% Load Regulation
- Adjustable Short Circuit Protection



P SUFFIX
PLASTIC PACKAGE
CASE 646

L SUFFIX
CERAMIC PACKAGE
CASE 632





D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

Figure 1. Circuit Schematic

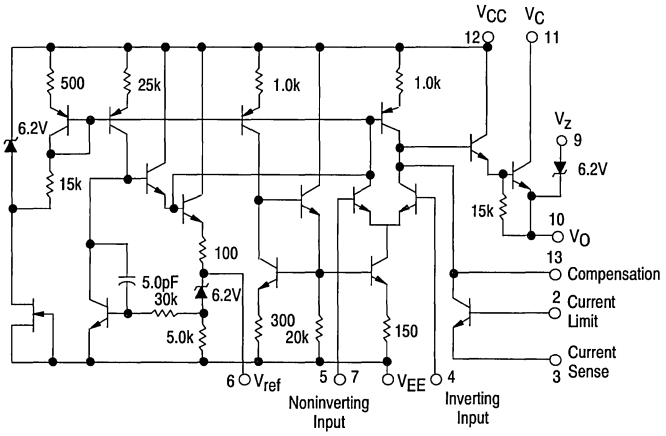
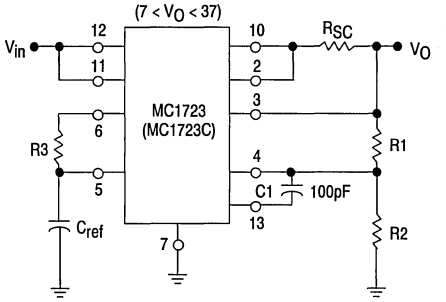


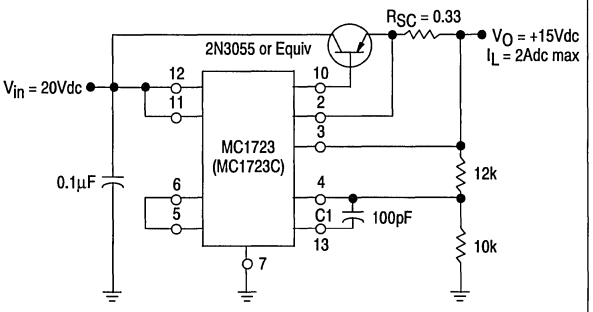
Figure 2. Typical Circuit Connection



$$V_O \cong 7\left(\frac{R1 + R2}{R2}\right) \quad I_{SC} = \frac{V_{sense}}{R_{SC}} = \frac{0.66}{R_{SC}} \text{ at } T_J = +25°C$$

For best results 10 k < R2 < 100 k
For minimum drift R3 = R1 | | R2

Figue 3. Typical NPN Current Boost Connection



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC1723CD		0° to +70°C	SO-14
MC1723CL	LM723CJ µA723DC		Ceramic DIP
MC1723CP	LM723CN µA723PC		Plastic DIP
MC1723L		–55° to +125°C	Ceramic DIP

3

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Pulse Voltage from V_{CC} to V_{EE} (50 ms)	$V_{I(p)}$	50	V_{pk}
Continuous Voltage from V_{CC} to V_{EE}	V_I	40	Vdc
Input-Output Voltage Differential	V_I–V_O	40	Vdc
Maximum Output Current	I_L	150	mAdc
Current from V_{ref}	I_{ref}	15	mAdc
Current from V_Z	I_Z	25	mA
Volatge Between Noninverting Input and V_{EE}	V_{ie}	8.0	Vdc
Differential Input Voltage	V_{id}	±5.0	Vdc
Power Dissipation and Thermal Characteristics Plastic Package T_A = +25°C Derate above T_A = +25°C Thermal Resistance, Junction to Air Ceramic Package Derate above T_A = +25°C Thermal Resistance, Junction to Air	 P_D $1/\theta_{JA}$ θ_{JA} P_D $1/\theta_{JA}$ θ_{JA}	 1.25 10 100 1.5 10 100	 W mW/°C °C/W W mW/°C °C/W
Operating and Storage Junction Temperature Range Plastic Package Ceramic Package	T_J, T_{stg}	–65 to +175	°C
Operating Ambient Temperature Range MC1723C MC1723	T_A	 0 to +70 –55 to +125	°C

ELECTRICAL CHARACTERICISTICS (T_A = +25°C, V_{in} 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, C1 = 100 pF, C_{ref} = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 2, unless otherwise noted.)

Characteristics	Symbol	MC1723 Min	MC1723 Typ	MC1723 Max	MC1723C Min	MC1723C Typ	MC1723C Max	Unit
Input Voltage Range	V_I	9.5	—	40	9.5	—	40	Vdc
Output Voltage Range	V_O	2.0	—	37	2.0	—	37	Vdc
Input-Output Voltage Differential	V_I-V_O	3.0	—	38	3.0	—	38	Vdc
Reference Voltage	V_{ref}	6.95	7.15	7.35	6.80	7.15	7.50	Vdc
Standby Current Drain (I_L = 0, V_{in} = 30 V)	I_{IB}	—	2.3	3.5	—	2.3	4.0	mAdc
Output Noise Voltage (f = 100 Hz to 10 kHz) C_{ref} = 0 C_{ref} = 5.0 µF	V_n	 — —	 20 2.5	 — —	 — —	 20 2.5	 — —	µV(RMS)
Average Temperatue Coefficient of Output Voltage (T_{low} À < T_A < T_{high} Á)	TCV_O	—	0.002	0.015	—	0.003	0.015	%/°C
Line Regulation (T_A = 25°C) { 12 V < V_{in} < 15 V 12 V < V_{in} < 40 V (T_{low} À < T_A < T_{high} Á) 12 V < V_{in} < 15 V	Reg_{line}	 — — —	 0.01 0.02 —	 0.1 0.2 0.3	 — — —	 0.01 0.1 —	 0.1 0.5 0.3	% V_O
Load Regulation (1.0 mA < I_L < 50 mA) T_A = 25°C T_{low} À < T_A < T_{high} Á	Reg_{load}	 — —	 0.03 —	 0.15 0.6	 — —	 0.03 —	 0.2 0.6	% V_O
Ripple Rejection (f = 50 Hz to 10 kHz) C_{ref} = 0 C_{ref} = 5.0 µF	RR	 — —	 74 86	 — —	 — —	 74 86	 — —	dB
Short Circuit Current Limit (R_{SC} = 10 Ω, V_O = 0)	I_{SC}	—	65	—	—	65	—	mAdc
Long Term Stability	$\Delta V_O/\Delta t$	—	0.1	—	—	0.1	—	%/1000 Hr.

NOTES: À T_{low} = 0° for MC1723C
= –55° for MC1723

Á T_{high} = +70°C for MC1723C
= +125°C for MC1723

Figure 4. Maximum Load Current as a Function of Input-Output Voltage Differential

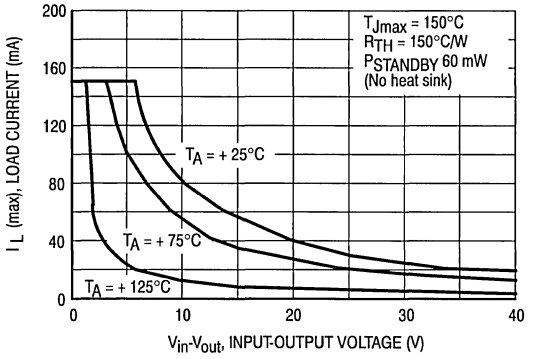


Figure 5. Load Regulation Characteristics Without Current Limiting

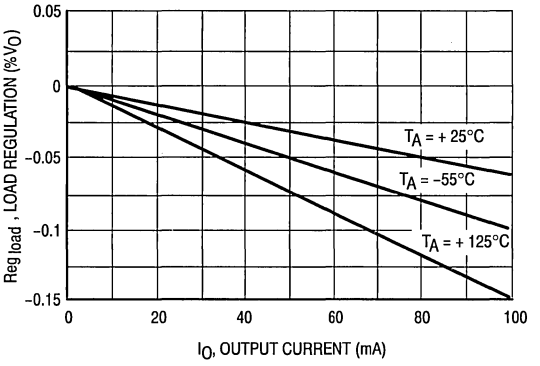


Figure 6. Load Regulation Characteristics With Current Limiting

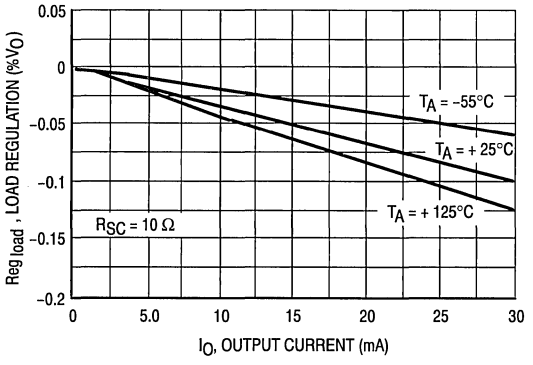


Figure 7. Load Regulation Characteristics With Current Limiting

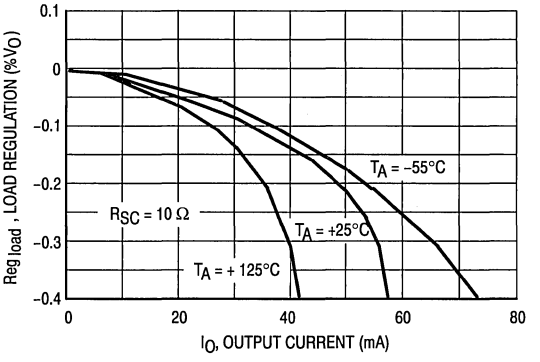


Figure 8. Current Limiting Characteristics

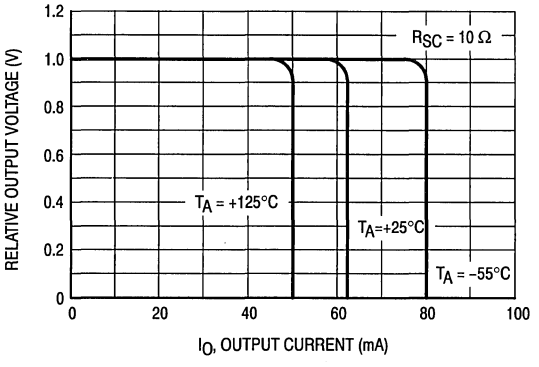
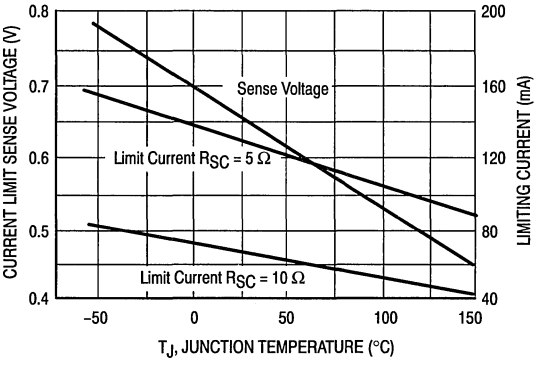


Figure 9. Current Limiting Characteristics as a Function of Junction Temperature



3

Figure 10. Line Regulation as a Function of Input-Output Voltage Differential

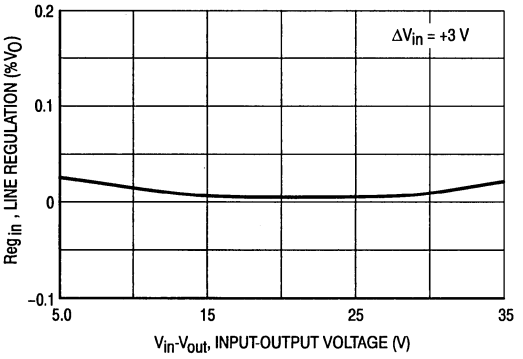


Figure 11. Load Regulation as a Function of Input-Output Voltage Differential

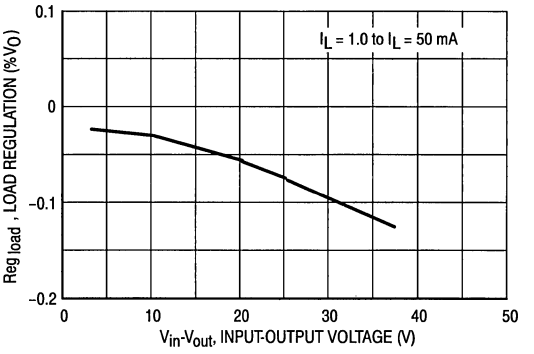


Figure 12. Standby Current Drain as a Function of Input Voltage

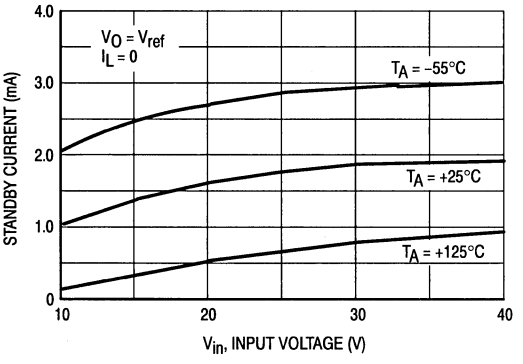


Figure 13. Line Transient Response

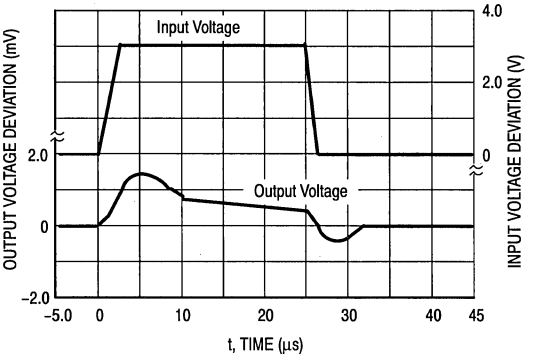


Figure 14. Load Transient Response

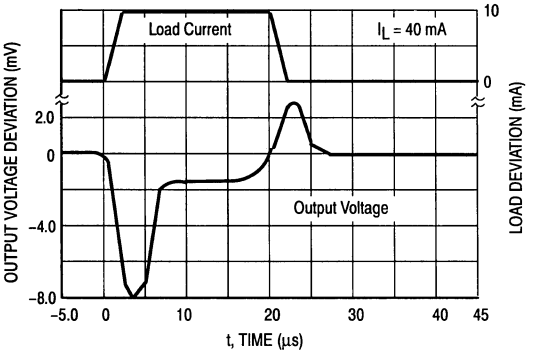


Figure 15. Output Impedance as Function of Frequency

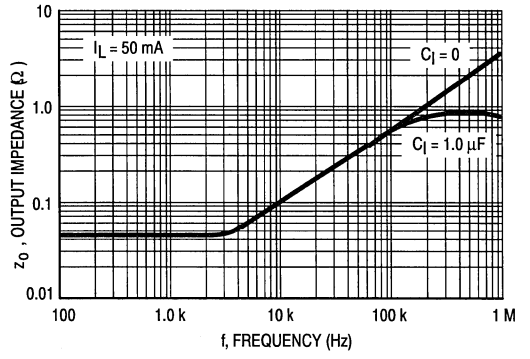
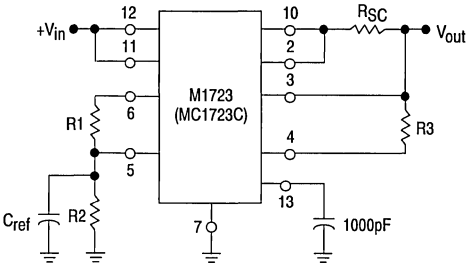


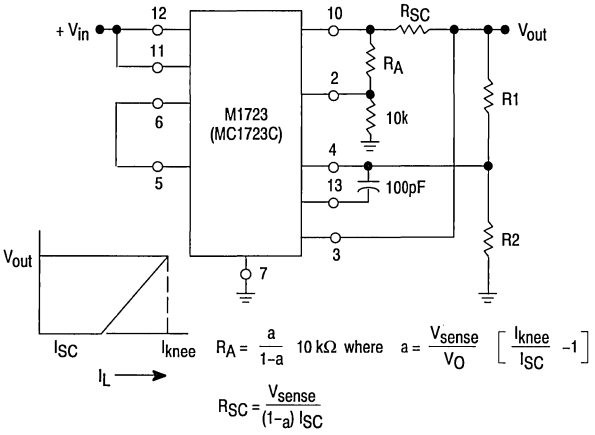
Figure 16. Typical Connection for 2 < V_O < 7



$V_O \cong 7\left[\frac{R2}{R1+R2}\right]$ $I_{SC} = \frac{V_{sense}}{R_{SC}} \cong \frac{0.66}{R_{SC}}$ at T_J = +25°C

For best results 10 k < R1 +R2 < 100 k
For minimum drift R3 = R1 R2

Figure 17. Foldback Connection



$R_A = \frac{a}{1-a}$ 10 kΩ where $a = \frac{V_{sense}}{V_O}\left[\frac{I_{knee}}{I_{SC}} - 1\right]$

$R_{SC} = \frac{V_{sense}}{(1-a)\ I_{SC}}$

Figure 18. +5.0 V, 1.0 A Switching Regulator

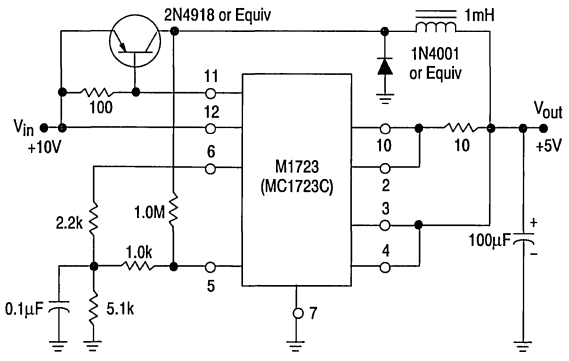


Figure 19. +5.0 V, 1.0 A High Efficiency Regulator

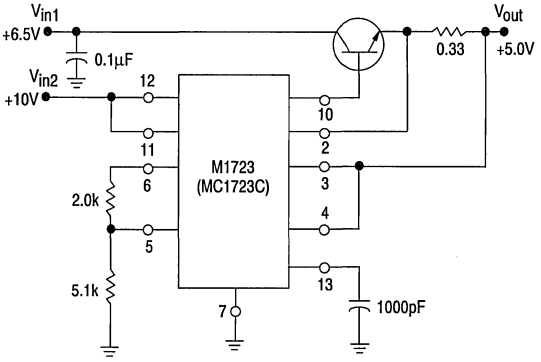


Figure 20. +15 V, 1.0 A Regulator with Remote Sense

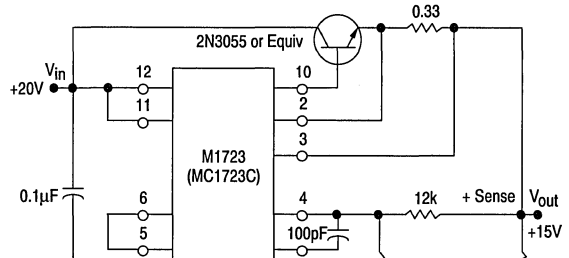


Figure 21. –15 V Negative Regulator

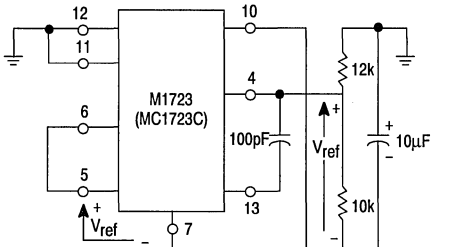
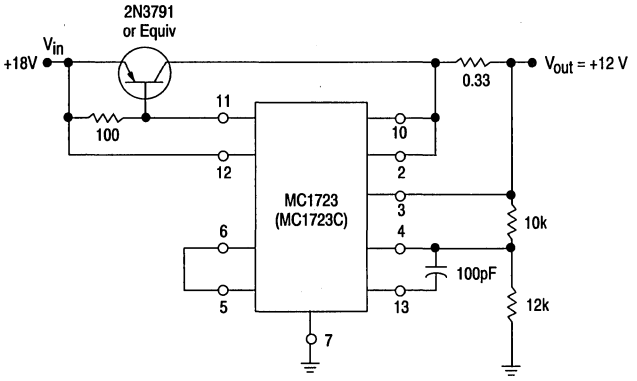


Figure 22. +12V, 1.0 A Regulator
(Using PNP Current Boost)



MC3423
MC3523

Overvoltage Crowbar Sensing Circuit

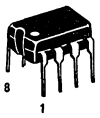
OVERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

These overvoltage protection circuits (OVP) protect sensitive electronic circuitry from overvoltage transients or regulator failures when used in conjunction with an external "crowbar" SCR. They sense the overvoltage condition and quickly "crowbar" or short circuit the supply, forcing the supply into current limiting or opening the fuse or circuit breaker.

The protection voltage threshold is adjustable and the MC3423/3523 can be programmed for minimum duration of overvoltage condition before tripping, thus supplying noise immunity.

The MC3423/3523 is essentially a "two terminal" system, therefore it can be used with either positive or negative supplies.



P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC3423 only)

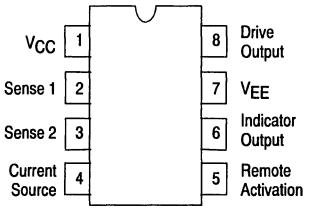
U SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP-8)

MAXIMUM RATINGS

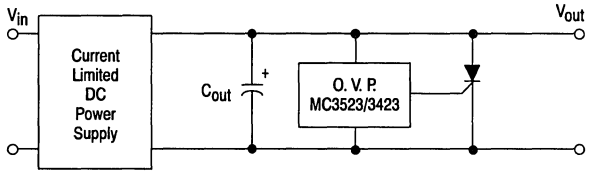
Rating	Symbol	Value	Unit
Differential Power Supply Voltage	V_{CC}–V_{EE}	40	Vdc
Sense Voltage (1)	V_{Sense1}	6.5	Vdc
Sense Voltage (2)	V_{Sense2}	6.5	Vdc
Remote Activation Input Voltage	V_{act}	7.0	Vdc
Output Current	I_O	300	mA
Operating Ambient Temperature Range MC3423 MC3523	T_A	 0 to +70 –55 to +125	°C
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 125 150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

PIN CONNECTIONS



(Top View)

Typical Application



ORDERING INFORMATION

Device	Temperature Range	Package
MC3423D	0° to +70°C	SO–8
MC3423P1		Plastic DIP
MC3423U		Ceramic DIP
MC3523U	–55° to +125°C	Ceramic DIP

3

ELECTRICAL CHARACTERICISTICS ($5\ V \le V_{CC} - V_{EE} \le 36\ V$, $T_{low} < T_A$, T_{high}, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}–V_{EE}	4.5	—	40	Vdc
Output Voltage (I_O = 100 mA)	V_O	V_{CC}–2.2	V_{CC}–1.8	—	Vdc
Indicator Output Voltage ($I_{O(Ind)}$ = 1.6 mA)	$V_{OL(Ind)}$	—	0.1	0.4	Vdc
Sense Trip Voltage (T_A = 25°C)	V_{Sense1}, V_{Sense2}	2.45	2.6	2.75	Vdc
Temperature Coefficient of V_{Sense1} (Figure 2)	TCV_{S1}	—	0.06	—	%/°C
Remote Activation Input Current (V_{IH} = 2.0 V, V_{CC} – V_{EE} = 5.0 V) (V_{IL} = 0.8 V, V_{CC} – V_{EE} = 5.0 V)	I_{IH} I_{IL}	— —	5.0 –120	40 –180	µA
Source Current	I_{Source}	0.1	0.2	0.3	mA
Output Current Risetime (T_A = 25°C)	t_r	—	400	—	mA/µs
Propagation Delay Time (T_A = 25°C)	t_{pd}	—	0.5	—	µs
Supply Current MC3423 MC3523	I_D	— —	6.0 5.0	10 7.0	mA

NOTES: T_{low} to T_{high} = –55° to +125°C for MC3523
= 0° to +70°C for MC3423

Figure 1. Block Diagram

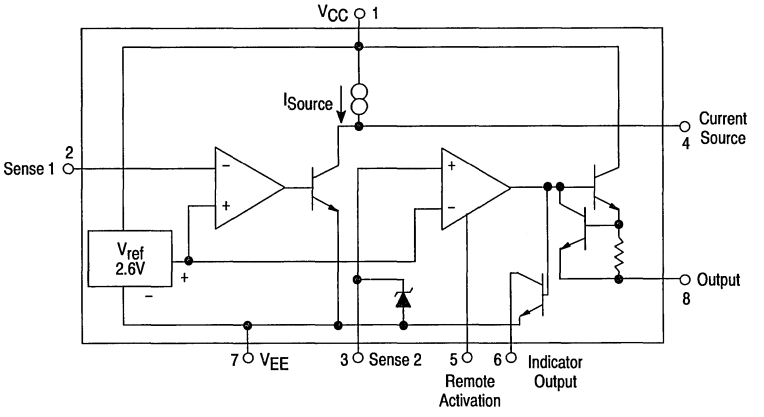
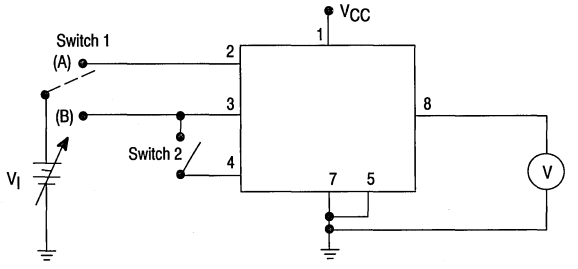


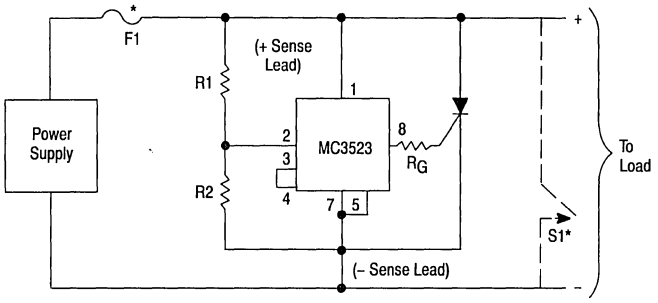
Figure 2. Sense Voltage Test Circuit



	Switch 1	Switch 2
$V_{Sense\ 1}$	Position A	Closed
$V_{Sense\ 2}$	Position B	Open

Ramp V_I until output goes high; this is the V_{Sense} threshold.

Figure 3. Basic Circuit Configuration



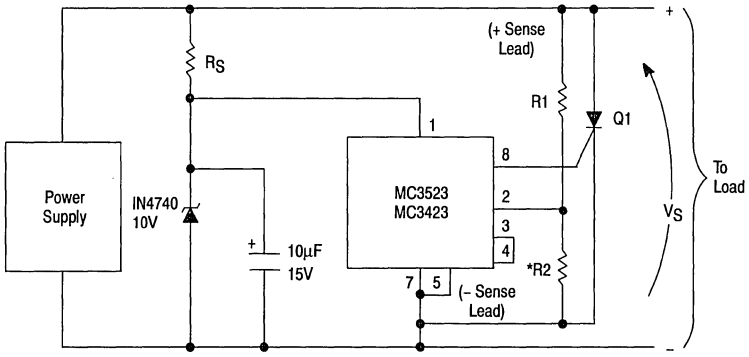
$$V_{trip} = V_{ref}\left(1 + \frac{R1}{R2}\right) \approx 2.6\ V\left(1 + \frac{R1}{R2}\right)$$

$R2 \leq 10\ k\Omega$ for minimum drift

For minimum value of R_G, see Figure 9

*See text for explanation

Figure 4. Circuit Configuration for Supply Voltage Above 36 V



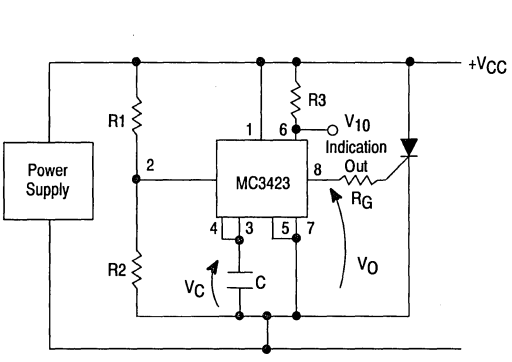
$$R_S = \left(\frac{V_S - 10}{25}\right)\ k\Omega$$

$$V_{trip} = V_{ref}\left(1 + \frac{R1}{R2}\right) \approx 2.6\ V\left(1 + \frac{R1}{R2}\right)$$

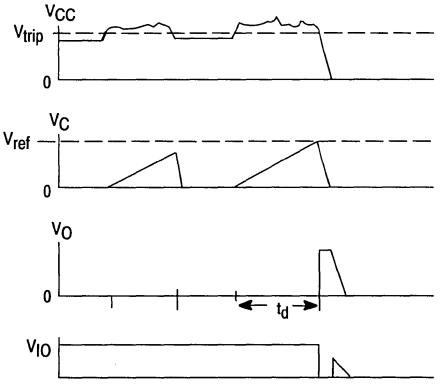
*$R2 \leq 10\ k\Omega$

Q1: $V_S \leq 50$ V; 2N6504 or equivalent
$V_S \leq 100$ V; 2N6505 or equivalent
$V_S \leq 200$ V; 2N6506 or equivalent
$V_S \leq 400$ V; 2N6507 or equivalent
$V_S \leq 600$ V; 2N6508 or equivalent
$V_S \leq 800$ V; 2N6509 or equivalent

Figure 5. Basic Configuration for Programmable Duration of Overvoltage Condition Before Trip



$$R3 \geq \frac{V_{trip}}{10\ mA}$$



$$t_d = \frac{V_{ref}}{I_{source}} \times C \approx [12 \times 10^3]\ C$$ (See Figure 10)

APPLICATION INFORMATION

Basic Circuit Configuration

The basic circuit configuration of the MC3423/3523 OVP is shown in Figure 3 for supply voltages from 4.5 V to 36 V, and in Figure 4 for trip voltages above 36 V. The threshold or trip voltage at which the MC3423/3523 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R1 and R2. Their values can be determined by the equation given in Figures 3 and 4, or by the graph shown in Figure 8. The minimum value of the gate current limiting resistor, R_G, is given in Figure 9. Using this value of R_G, the SCR, Q1, will receive the greatest gate current possible without damaging the MC3423/3523. If lower output currents are required, R_G can be increased in value. The switch, S1, shown in Figure 3 may be used to reset the crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current-limited supply is used, a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

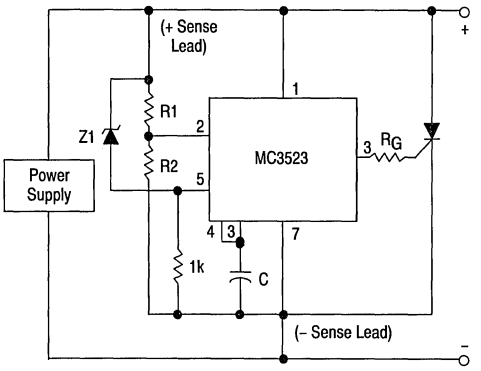
The circuit configurations shown in Figures 3 and 4 will have a typical propogation delay of 1.0 μs. If faster operation is desired, Pin 3 may be connected to Pin 2 with Pin 4 left floating. This will result in decreasing the propogation delay to approximately 0.5 μs at the expense of a slightly increased TC for the trip voltage value.

Configuration for Programmable Minimmum Duration of Overvoltage Condition Before Tripping

In many instances, the MC3423/3523 OVP will be used in a noise environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423/3523 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 5 is used. In this configuration, a capacitor is connected from Pin 3 to V_{EE}. The value of this capacitor determines the minimum duration of the overvoltage condition which is necessary to trip the OVP. The value of C can be found from Figure 10. The circuit operates in the following manner: When V_{CC} rises above the trip point set by R1 and R2, an internal current source (Pin 4) begins charging the capacitor, C, connected to Pin 3. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate ≅ 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

Occasionally, it is desired that immediate crowbarring of the supply occur when a high overvoltage condition occurs, while retaining the false tripping immunity of Figure 5. In this case, the circuit of Figure 6 can be used. The circuit will operate as previously described for small overvoltages, but will immediately trip if the power supply voltage exceeds V_{Z1} + 1.4 V.

Figure 6. Configuration for Programmable Duration of Overvoltage Condition Before Trip/With Immediate Trip at High Overvoltages



Additional Features

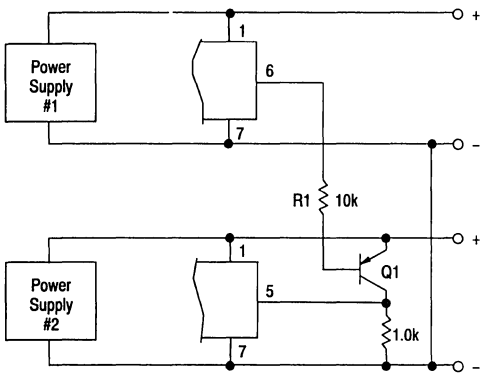
1. Activation Indication Output

An additional output for use as an indicator of OVP activation is provided by the MC3423/3523. This output is an open collector transistor which saturates when the OVP is activated. In addition, it can be used to clock an edge triggered flip-flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

2. Remote Activation Input

Another feature of the MC3423/3523 is its remote activation input, Pin 5. If the voltage on this CMOS/TTL compatible input is held below 0.8 V, the MC3423/3523 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present. It should be noted that Pin 5 has an internal pull-up current source. This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the activation indication output of one MC3423/3523 can be used to activate another MC3423/3523 if a single transistor inverter is used to interface the former's indication output to the latter's remote activation input, as shown in Figure 7. In this circuit, the indication output (pin 6) of the MC3423 on power supply 1 is used to activate the MC3423 associated with power supply 2. Q1 is any small PNP with adequate voltage rating.

Figure 7. Circuit Configuration for Activating One MC3523 from Another



Note that both supplies have their negative output leads tied together (i.e., both are positive supplies). If their positive leads are common (two negative supplies) the emitter of Q1 would be moved to the positive lead of supply 1 and R1 would therefore have to be resized to deliver the appropriate drive to Q1.

Crowbar SCR Considerations

Referring to Figure 11, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output caps, the load's decoupling caps, and in the case of Figure 11A, the supply's input filter caps. This surge current is illustrated in Figure 12, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

Figure 8. R1 versus Trip Voltage

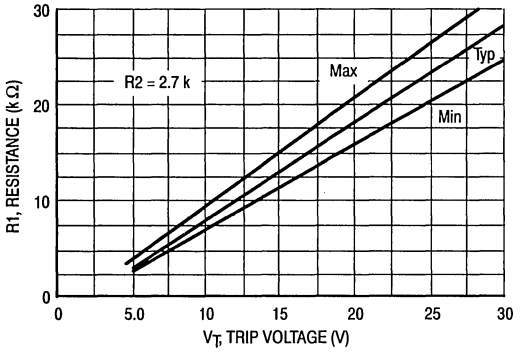


Figure 9. Minimum R_G versus Supply Voltage

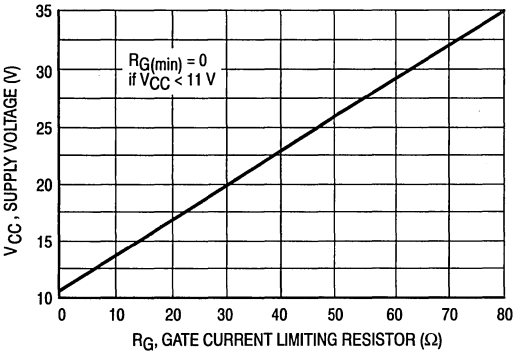


Figure 10. Capacitance versus Minimum Overvoltage Duration

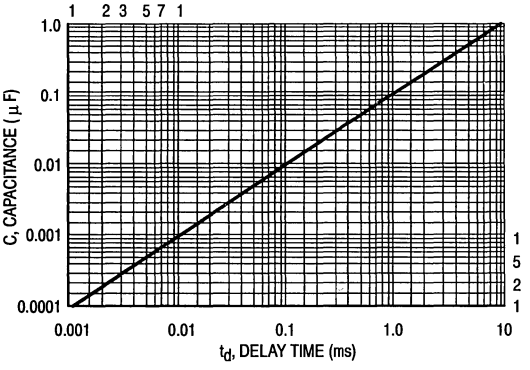
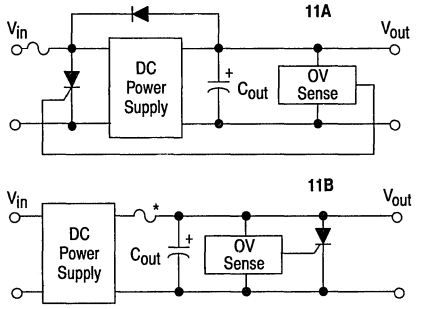


Figure 11. Typical Crowbar OVP Circuit Configurations



*Needed if supply not current limited

Figure 12. Crowbar SCR Surge Current Waveform

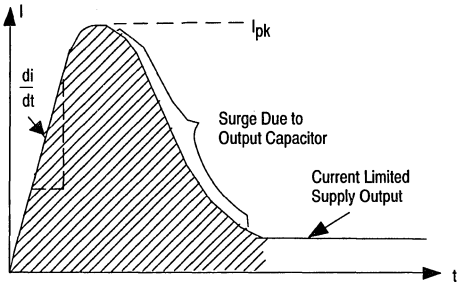
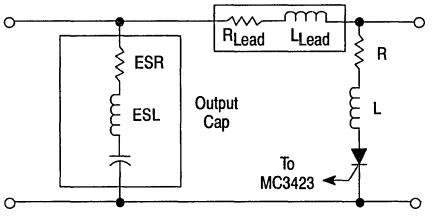


Figure 13. Circuit Elements Affecting SCR Surge & di/dt



R & L EMPIRICALLY DETERMINED!

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 11B.

For a complete and detailed treatment of SCR and fuse selection, refer to Motorola Application Note AN-789.

The Value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast < 1.0 µs rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/µs, assuming a gate current of five times I_{GT} and < 1.0 µs rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 13. Of course, this reduces the circuit's ability to rapidly reduce the DC bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 13) to a safe level which is consistent with the systems requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the DC power supply.

A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 11A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

Device	I_{RMS}	I_{FSM}	Package
2N6400 Series	16 A	160 A	TO220 Plastic
2N6504 Series	25 A	160 A	TO220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N2573 Series	25 A	260 A	Metal TO-3 Type
2N681 Series	25 A	200 A	Metal Stud
MCR3935-1 Series	35 A	350 A	Metal Stud
MCR81-5 Series	80 A	1000 A	Metal Stud

MC3425

Power Supply Supervisory/Over and Undervoltage Protection Circuit

POWER SUPPLY SUPERVISORY/ OVER AND UNDERVOLTAGE PROTECTION CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

3

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over and undervoltage fault conditions. These integrated circuits contain dedicated over and undervoltage sensing channels with independently programmable time delays. The overvoltage channel has a high current Drive Output for use in conjunction with an external SCR "Crowbar" for shutdown. The undervoltage channel input comparator has hysteresis which is externally programmable, and an open-collector output for fault indication.

- Dedicated Over And Undervoltage Sensing
- Programmable Hysteresis Of Undervoltage Comparator
- Internal 2.5 V Reference
- 300 mA Overvoltage Drive Output
- 30 mA Undervoltage Indicator Output
- Programmable Time Delays
- 4.5 V to 40 V Operation

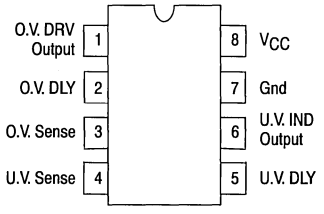
P1 SUFFIX
PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range (Note 1)	V_{IR}	−0.3 to +40	Vdc
Drive Output Short Circuit Current	$I_{OS(DRV)}$	Internally Limited	mA
Indicator Output Voltage	V_{IND}	0 to 40	Vdc
Indicator Output Sink Current	I_{IND}	30	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$	 1000 80	 mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTES: 1. The input signal voltage should not be allowed to go negative by more than 300 mV or positive by more than 40 V, independent of V_{CC}, without device destruction.

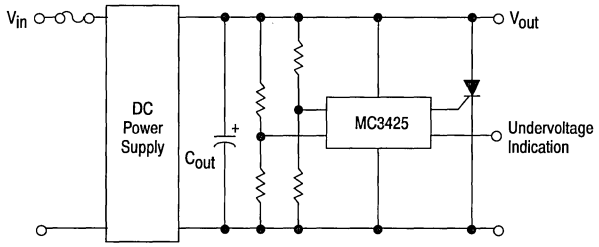
PIN CONNECTIONS



(Top View)

Typical Application

Overvoltage Crowbar Protection, Undervoltage Indication



ORDERING INFORMATION

Device	Temperature Range	Package
MC3425P1	0° to +70°C	Plastic DIP

ELECTRICAL CHARACTERICISTICS ($4.5\ V \le V_{CC} \le 40\ V$; $T_A = T_{low}$ to T_{high} [see Note 2], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Sense Trip Voltage (Referenced Voltage) V_{CC} = 15 V T_A = 25°C T_{low} to T_{high} (Note 2)	V_{Sense}	 2.4 2.33	 2.5 2.5	 2.6 2.63	Vdc
Line Regulation of V_{Sense} $4.5\ V \le V_{CC} \le 40\ V$; T_J = 25°C	Reg_{line}	—	7.0	15	mV
Power Supply Voltage Operating Range	V_{CC}	4.5	—	40	Vdc
Power Supply Current V_{CC} = 40 V; T_A = 25°C; No Output Loads O.V. Sense (Pin 3) = 0 V; U.V. Sense (Pin 4) = V_{CC}	$I_{CC(off)}$	—	8.5	10	mA
O.V. Sense (Pin 3) = V_{CC}; U.V. Sense (Pin 4) = 0 V	$I_{CC(on)}$	—	16.5	19	mA
INPUT SECTION					
Input Bias Current, O.V. and U.V. Sense	I_{IB}	—	1.0	2.0	µA
Hysteresis Activation Voltage, U.V. Sense V_{CC} = 15 V; T_A = 25°C; I_H = 10% I_H = 90%	$V_{H(act)}$	 — —	 0.6 0.8	 — —	V
Hysteresis Current, U.V. Sense V_{CC} = 15 V; T_A = 25°C; U.V. Sense (Pin 4) = 2.5 V	I_H	9.0	12.5	16	µA
Delay Pin Voltage (I_{DLY} = 0 mA) Low State High State	 $V_{OL(DLY)}$ $V_{OH(DLY)}$	 — V_{CC}–0.5	 0.2 V_{CC}–0.15	 0.5 —	V
Delay Pin Source Current V_{CC} = 15 V; V_{DLY} 0 V	$I_{DLY(source)}$	140	200	260	µA
Delay Pin Sink Current V_{CC} = 15 V; V_{DLY} 2.5V	$I_{DLY(sink)}$	1.8	3.0	—	mA
OUTPUT SECTION					
Drive Output Peak Current (T_A = 25°C)	$I_{DRV(peak)}$	200	300	—	mA
Drive Output Voltage I_{DRV} = 100 mA; T_A = 25° C	$V_{OH(DRV)}$	V_{CC}–2.5	V_{CC}–2.0	—	V
Drive Output Leakage Current V_{DRV} = 0 V	$I_{DRV(leak)}$	—	15	200	nA
Drive Output Current Slew Rate (T_A = 25°C)	di/dt	—	2.0	—	A/µs
Drive Output V_{CC} Transient Rejection V_{CC} = 0 V to 15 V at dV/dt = 200 V µs; O.V. Sense (Pin 3) = 0 V; T_A = 25°C	$I_{DRV(trans)}$	—	1.0	—	mA (Peak)
Indicator Output Saturation Voltage I_{IND} = 30 mA; T_A = 25°C	$V_{IND(sat)}$	—	560	800	mV
Indicator Output Leakage Current $V_{OH(IND)}$ = 40 V	$I_{IND(leak)}$	—	25	200	nA
Output Comparator Threshold Voltage (Note 3)	$V_{th(OC)}$	2.33	2.5	2.63	V
Propagation Delay Time (V_{CC} = 15 V; T_A = 25°C) Input to Drive Output or Indicator Output 100 mV Overdrive, C_{DLY} = 0 µF	$t_{PLH(IN/OUT)}$	—	1.7	—	µs
Input to Delay 2.5 V Overdrive (0 V to 5.0 V Step)	$t_{PLH(IN//DLY)}$	—	700	—	ns

NOTES: 2. T_{Low} to T_{High} = 0° to +70°C
3. The $V_{th(OC)}$ limits are approximately the V_{Sense} limits over the applicable temperature range.

Figure 1. Hysteresis Current versus Hysteresis Activation Voltage

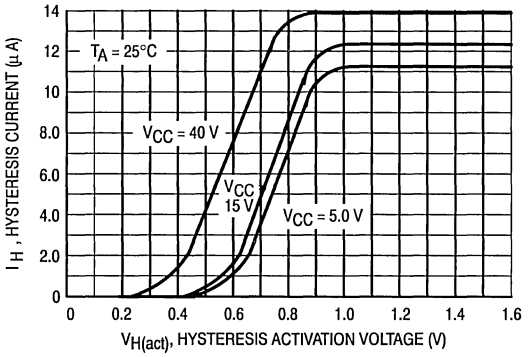


Figure 2. Hysteresis Activation Voltage versus Temperature

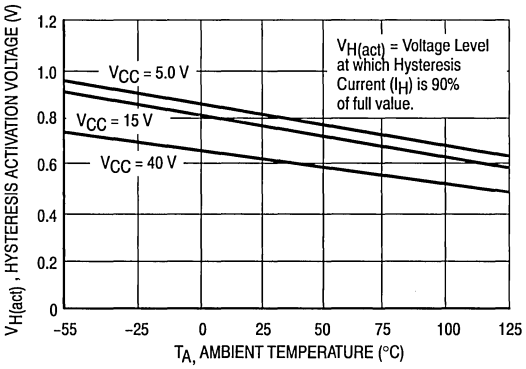


Figure 3. Hysteresis Current versus Temperature

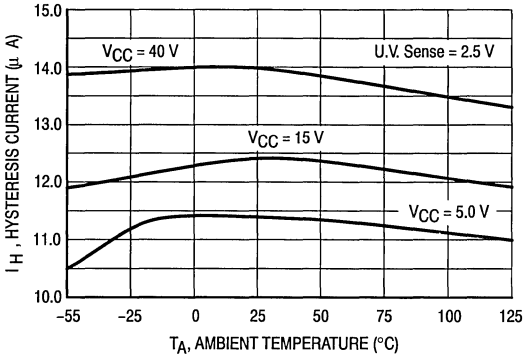


Figure 4. Sense Trip Voltage Change versus Temperature

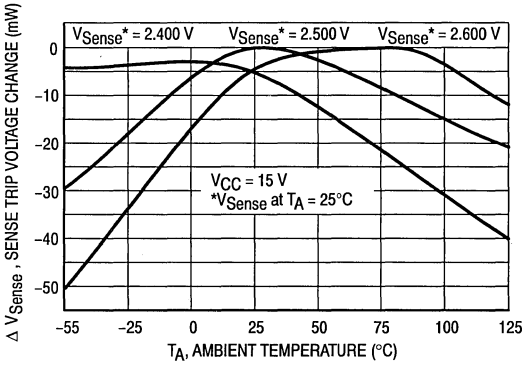


Figure 5. Output Delay Time versus Delay Capacitance

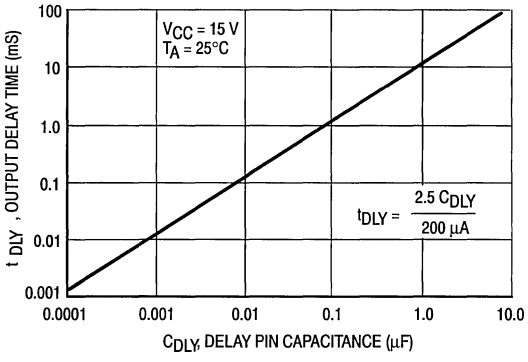


Figure 6. Delay Pin Source Current versus Temperature

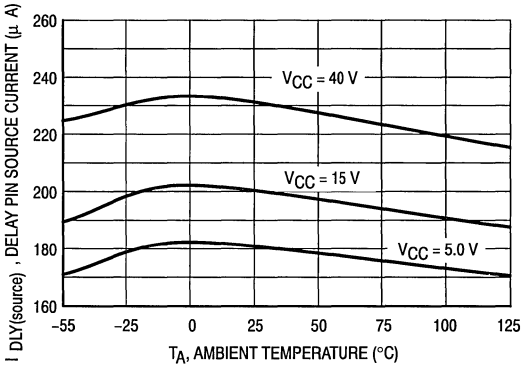


Figure 7. Drive Output Saturation Voltage versus Output Peak Current

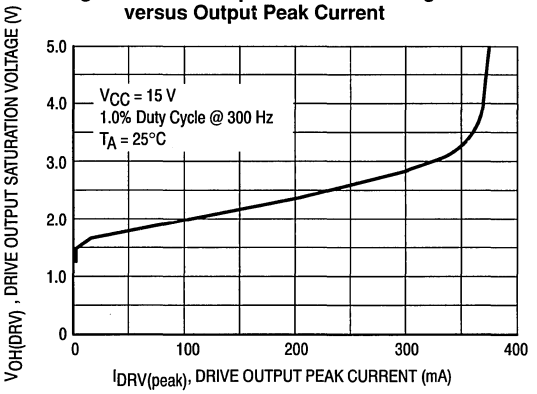


Figure 8. Indicator Output Saturation Voltage versus Output Sink Current

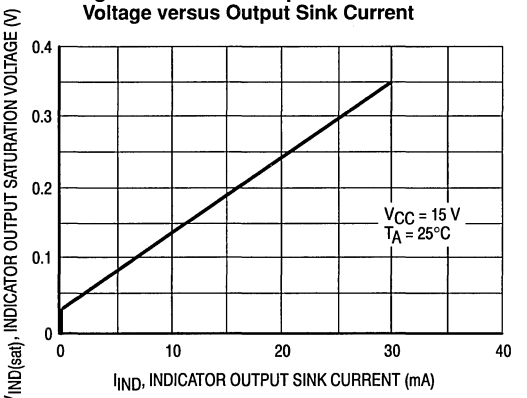


Figure 9. Drive Output Saturation Voltage versus Temperature

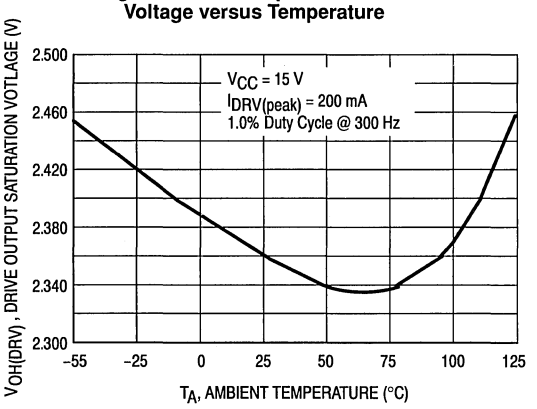
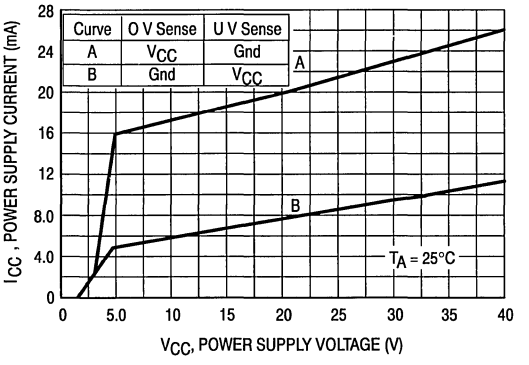
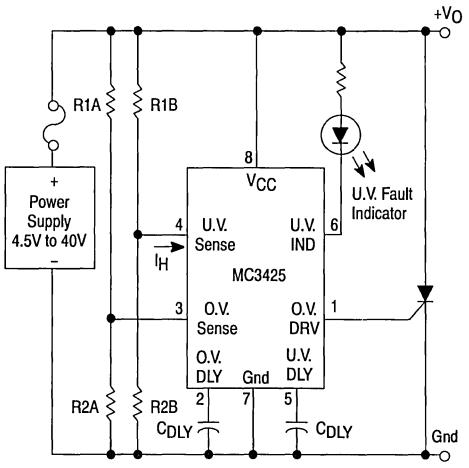


Figure 10. Power Supply Current versus Voltage



APPLICATIONS INFORMATION

Figure 11. Overvoltage Protection and Undervoltage Fault Indication with Programmable Delay



$$\text{U.V. Hysteresis} = I_H \left(\frac{R1B\ R2B}{R1B + R2B} \right) \quad V_{O(trip)} = 2.5\ V \left(1 - \frac{R1A}{R2A}\right)$$

$$t_{DLY} = 12500\ C_{DLY}$$

Figure 12. Overvoltage Protection of 5.0 V Supply with Line Loss Detector

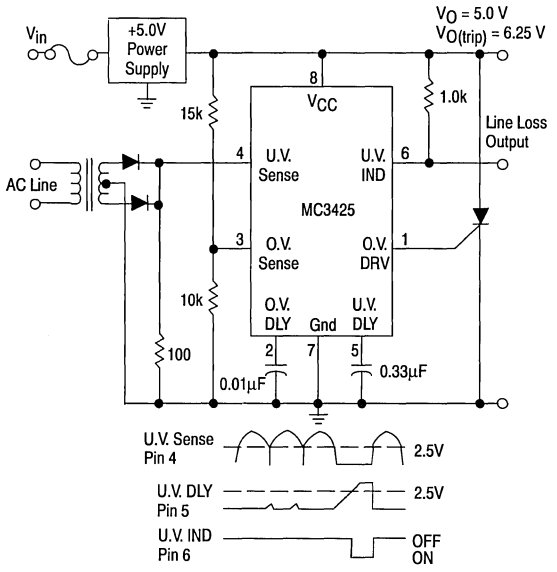


Figure 13. Overvoltage Audio Alarm Circuit

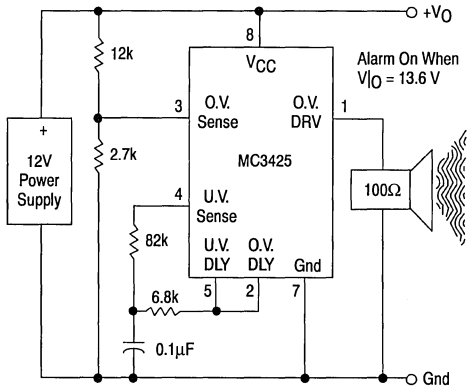
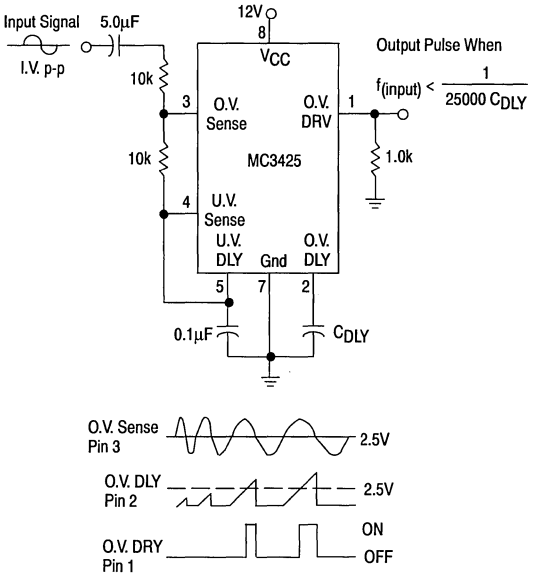


Figure 14. Programmable Frequency Switch



CIRCUIT DESCRIPTION

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over and undervoltage fault conditions. The block diagram is shown below in Figure 15. The Overvoltage (O.V.) and Undervoltage (U.V.) Input Comparators are both referenced to an internal 2.5 V regulator. The U.V. Input Comparator has a feedback activated 12.5 μA current sink (I_H) which is used for programming the input hysteresis voltage (V_H). The source resistance feeding this input (R_H) determines the amount of hysteresis voltage by $V_H = I_H R_H = 12.5 \times 10^{-6} R_H$.

Separate Delay pins (O.V. DLY, U.V. DLY.) are provided for each channel to independently delay the Drive and Indicator outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source, $I_{DLY(source)}$, of typically 200 μA when the noninverting input voltage is greater than the inverting input level. A capacitor connected from these Delay pins to ground, will establish a predictable delay time (t_{DLY}) for the Drive and Indicator outputs. The Delay pins are internally connected to the noninverting inputs of the O.V. and U.V. Output Comparators, which are referenced to the internal 2.5 V regulator. Therefore, delay time (t_{DLY}) is based on the constant current source, $I_{DLY(source)}$, charging the external delay capacitor (C_{DLY}) to 2.5 V.

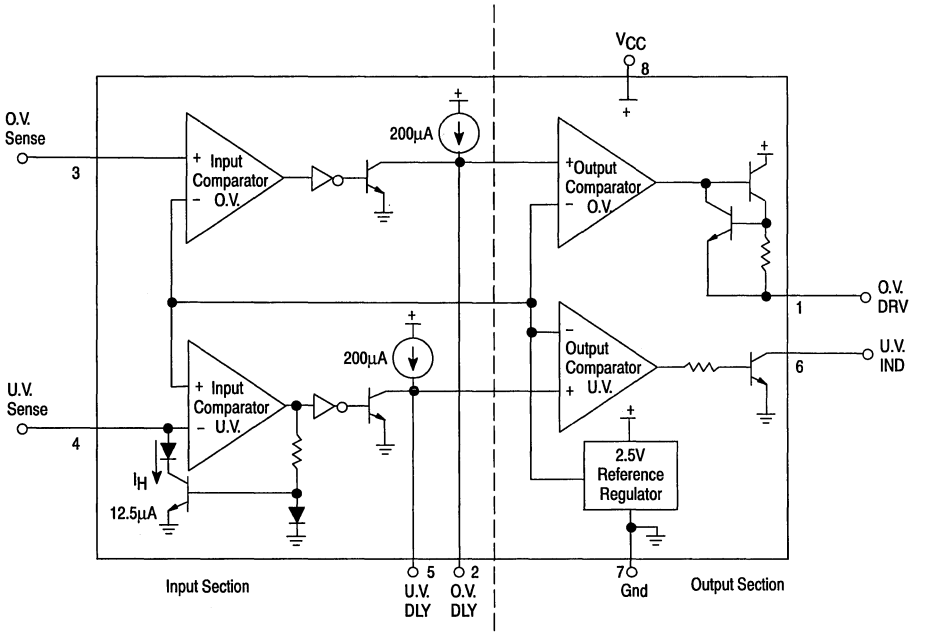
$$t_{DLY} = \frac{V_{ref}\, C_{DLY}}{I_{DLY(source)}} = \frac{2.5\, C_{DLY}}{200\ \mu A} = 12500\, C_{DLY}$$

Figure 5 provides C_{DLY} values for a wide range of time delays. The Delay pins are pulled low when the respective input comparator's noninverting input is less than the inverting input. The sink current, $I_{DLY(sink)}$, capability of the Delay pins is ≥ 1.8 mA and is much greater than the typical 200 μA source current, thus enabling a relatively fast delay capacitor discharge time.

The Overvoltage Drive Output is a current-limited emitter-follower capable of sourcing 300 mA at a turn-on slew rate at 2.0 A/μs, ideal for driving "Crowbar" SCR's. The Undervoltage Indicator Output is an open-collector, NPN transistor, capable of sinking 30 mA to provide sufficient drive for LED's, small relays or shut-down circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded.

The MC3425 has an internal 2.5 V bandgap reference regulator with an accuracy of ± 4.0% for the basic devices and ± 1.0% for the A-suffix device types at 25°C. The reference has a typical temperature coefficient of 30 ppm/°C for A-suffix devices.

Figure 15. Block Diagram



Note: All voltages and currents are nominal.

CROWBAR SCR CONSIDERATIONS

Referring to Figure 16, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 16A, the supply's input filter capacitors. This surge current is illustrated in Figure 17, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

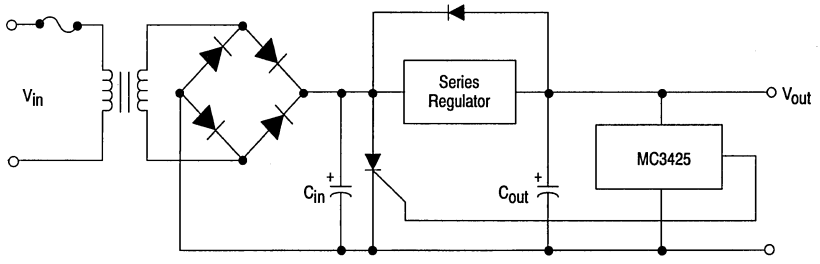
1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities — depending on the severity of the occasion.

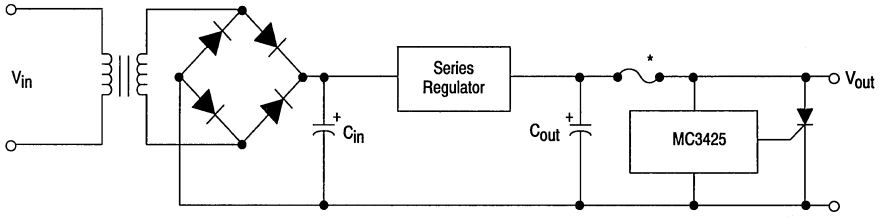
The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast < 1.0 µs rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/µs, assuming a gate current of five times I_{GT} and < 1.0 µs rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 18. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

Figure 16. Typical Crowbar Circuit Configurations

16A — SCR ACROSS INPUT OF REGULATOR

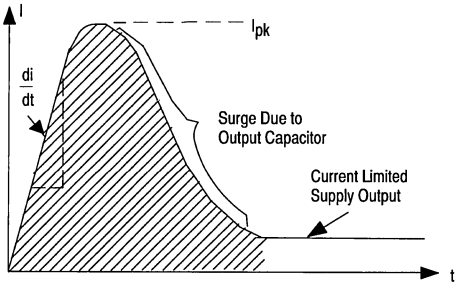


16B — SCR ACROSS OUTPUT OF REGULATOR



*Needed if supply is not current limited.

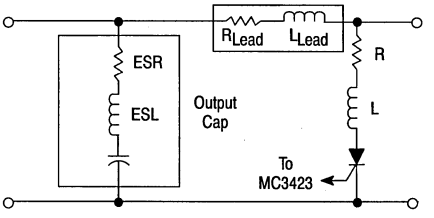
Figure 17. Crowbar SCR Surge Current Waveform



2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance — see Figure 18) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the DC power supply.

Figure 18. Circuit Elements Affecting SCR Surge & di/dt



R & L EMPIRICALLY DETERMINED

A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 16A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 11B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

Device	I_{RMS}	I_{FSM}	Package
MCR67 Series	12 A	100 A	Metal Stud
MCR68 Series	12 A	100 A	TO-220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N6400 Series	16 A	160 A	TO-220 Plastic
2N6504 Series	25 A	160 A	TO-220 Plastic
2N681 Series	25 A	200 A	Metal Stud
2N2573 Series	25 A	260 A	TO-3 Metal Can
MCR69 Series	25 A	300 A	TO-220 Plastic
MCR70 Series	35 A	350 A	Metal Stud
MCR71 Series	55 A	550 A	Metal Stud

For a complete and detailed treatment of SCR and fuse selection refer to Motorola Application Note AN789.

MC7800 Series

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

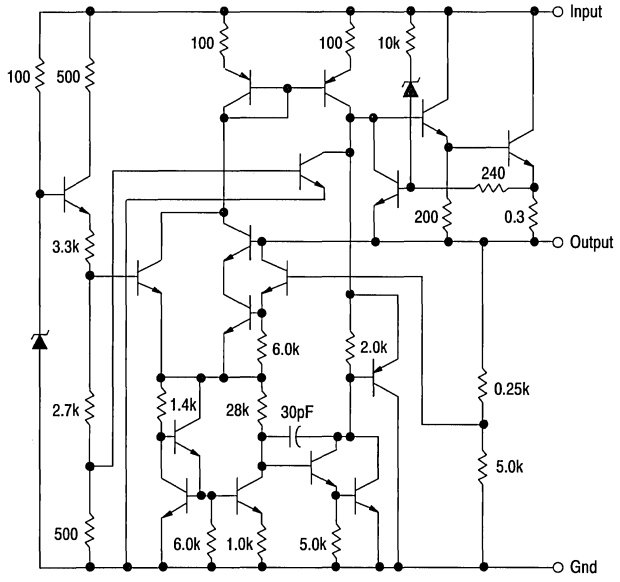
SILICON MONOLITHIC INTEGRATED CIRCUITS

Three-Terminal Positive Voltage Regulators

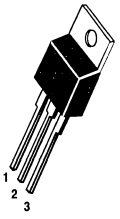
These voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. These regulators employ internal current limiting, thermal shutdown, and safe-area compensation. With adequate heatsinking they can deliver output currents in excess of 1.0 A. Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents.

- Output Current in Excess of 1.0 A
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Output Voltage Offered in 2% and 4% Tolerance

Representative Schematic Diagram



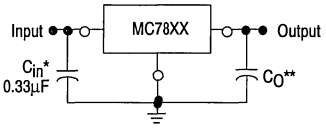
T SUFFIX
PLASTIC PACKAGE
CASE 221A



PIN 1. Input
2. Ground
3. Output

Heatsink surface connected to Pin 2

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

*= C_{in} is required if regulator is located an appreciable distance from power supply filter.

**= C_O is not needed for stability; however, it does improve transient response.

XX indicates nominal voltage

ORDERING INFORMATION

Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
MC78XXCT MC78XXACT	4% 2%	0° to +125°C	Plastic Power
MC78XXBT	4%	–40° to +125°C	

TYPE NO./VOLTAGE			
MC7805	5.0 V	MC7812	12 V
MC7806	6.0 V	MC7815	15 V
MC7808	8.0 V	MC7818	18 V
MC7809	9.0 V	MC7824	24 V

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 – 18 V) (24 V)	V_I	35 40	Vdc
Power Dissipation and Thermal Characteristics Plastic Package T_A = +25°C Derate above T_A = +25°C Thermal Resistance, Junction to Air T_C = + 25°C Derate above T_C = + 75°C (See Figure 1) Thermal Resistance, Junction to Case	 P_D $1/\theta_{JA}$ θ_{JA} P_D $1/\theta_{JC}$ θ_{JC}	 Internally Limited 15.4 65 Internally Limited 200 5.0	 W mW/°C °C/W W mW/°C °C/W
Storage Junction Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	+150	°C

DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

Figure 1. Worst Case Power Dissipation versus Ambient Temperature (Case 221A)

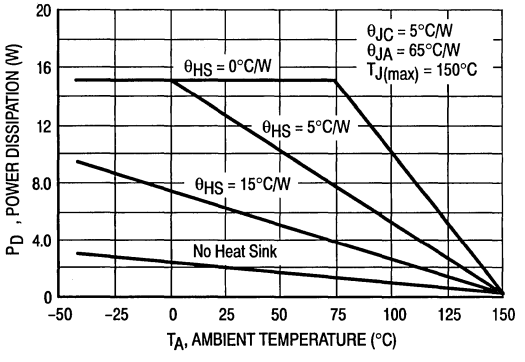
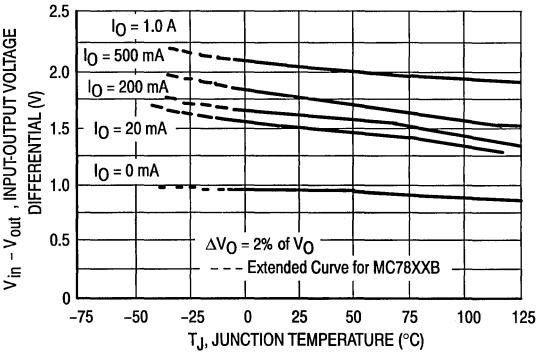


Figure 2. Input Output Differential as a Function of Junction Temperature (MC78XXC, AC, B)



MC7805B, C

ELECTRICAL CHARACTERICISTICS (V_{in} = 10 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC7805B			MC7805C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	4.8	5.0	5.2	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤15 W) 7.0 Vdc ≤ V_{in} ≤ 20 Vdc 8.0 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	 — 4.75	 — 5.0	 — 5.25	 4.75 —	 5.0 —	 5.25 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc	Reg_{line}	 — —	 7.0 2.0	 100 50	 — —	 7.0 2.0	 100 50	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ V_{in} ≤ 1.5 A 250 mA ≤ V_{in} ≤ 750 mA	Reg_{load}	 — —	 40 15	 100 50	 — —	 40 15	 100 50	mV
Quiescent Current (T_J = +25°C)	I_B	—	4.3	8.0	—	4.3	8.0	mA
Quiescent Current Change 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 — 1.3 0.5	 — — —	 — — —	 1.3 — 0.5	mA
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz	RR	—	68	—	—	68	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_I - V_O$	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	17	—	—	17	—	mΩ
Short Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{SC}	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	–1.1	—	—	–1.1	—	mV/°C

MC7805AC

ELECTRICAL CHARACTERICISTICS (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.9	5.0	5.1	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤15 W) 7.5 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	 4.8	 5.0	 5.2	Vdc
Line Regulation (Note 2) 7.5 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 8.0 Vdc ≤ V_{in} ≤ 12 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc, T_J = +25°C 7.3 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = +25°C	Reg_{line}	 — — — —	 7.0 10 2.0 7.0	 50 50 25 50	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — — —	 25 25 — 8.0	 100 100 — 50	mV
Quiescent Current (T_J = +25°C)	I_B	 —	 —	 6.0	mA
		—	4.3	6.0	
Quiescent Current Change 8.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 0.8 0.8 0.5	mA
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, T_J = +25°C 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, I_O = 500 mA	RR	 — —	 — 68	 — —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_I - V_O$	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	17	—	mΩ
Short Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{SC}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	–1.1	—	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXC, AC; T_{high} = +125°C for MC78XXC, AC, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7806B, C

ELECTRICAL CHARACTERICISTICS (V_{in} = 11 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC7806B			MC7806C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	5.75	6.0	6.25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤15 W) 8.0 Vdc ≤ V_{in} ≤ 21 Vdc 9.0 Vdc ≤ V_{in} ≤ 21 Vdc	V_O	 — 5.7	 — 6.0	 — 6.3	 5.7 —	 6.0 —	 6.3 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 9.0 Vdc ≤ V_{in} ≤ 13 Vdc	Reg_{line}	 — —	 9.0 3.0	 120 60	 — —	 9.0 3.0	 120 60	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ V_{in} ≤ 1.5 A 250 mA ≤ V_{in} ≤ 750 mA	Reg_{load}	 — —	 43 16	 120 60	 — —	 43 16	 120 60	mV
Quiescent Current (T_J = +25°C)	I_B	—	4.3	8.0	—	4.3	8.0	mA
Quiescent Current Change 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 9.0 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 — 1.3 0.5	 — — —	 — — —	 1.3 — 0.5	mA
Ripple Rejection 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz	RR	—	65	—	—	65	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_I - V_O$	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	17	—	—	17	—	mΩ
Short Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{SC}	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	–0.8	—	—	–0.8	—	mV/°C

MC7806AC

ELECTRICAL CHARACTERICISTICS (V_{in} = 11 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	5.88	6.0	6.12	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤15 W) 8.6 Vdc ≤ V_{in} ≤ 21 Vdc	V_O	 5.76	 6.0	 6.24	Vdc
Line Regulation (Note 2) 8.6 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 9.0 Vdc ≤ V_{in} ≤ 13 Vdc 9.0 Vdc ≤ V_{in} ≤ 13 Vdc, T_J = +25°C 8.3 Vdc ≤ V_{in} ≤ 21 Vdc, T_J = +25°C	Reg_{line}	 — — — —	 9.0 11 3.0 9.0	 60 60 30 60	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — — —	 43 43 — 16	 100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 4.3	6.0 6.0	mA
Quiescent Current Change 9.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 8.6 Vdc ≤ V_{in} ≤ 21 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 0.8 0.8 0.5	mA
Ripple Rejection 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz, T_J = +25°C 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz, I_O = 500 mA	RR	 — —	 — 65	 — —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_I - V_O$	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	17	—	mΩ
Short Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{SC}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	–0.8	—	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXC, AC; T_{high} = +125°C for MC78XXC, AC, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7808B, C

ELECTRICAL CHARACTERICISTICS (V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC7808B			MC7808C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	7.7	8.0	8.3	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤15 W) 10.5 Vdc ≤ V_{in} ≤ 23 Vdc 11.5 Vdc ≤ V_{in} ≤ 23 Vdc	V_O	 — 7.6	 — 8.0	 — 8.4	 7.6 —	 8.0 —	 8.4 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 10.5 Vdc ≤ V_{in} ≤ 25 Vdc 11 Vdc ≤ V_{in} ≤ 17 Vdc	Reg_{line}	 — —	 12 5.0	 160 80	 — —	 12 5.0	 160 80	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 45 16	 160 80	 — —	 45 16	 160 80	mV
Quiescent Current (T_J = +25°C)	I_B	—	4.3	8.0	—	4.3	8.0	mA
Quiescent Current Change 10.5 Vdc ≤ V_{in} ≤ 25 Vdc 11.5 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 — 1.0 0.5	 — — —	 — — —	 1.0 — 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz	RR	—	62	—	—	62	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_I - V_O$	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	18	—	—	18	—	mΩ
Short Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{SC}	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	–0.8	—	—	–0.8	—	mV/°C

MC7808AC

ELECTRICAL CHARACTERICISTICS (V_{in} = 14 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	7.84	8.0	8.16	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤15 W) 10.6 Vdc ≤ V_{in} ≤ 23 Vdc	V_O	 7.7	 8.0	 8.3	Vdc
Line Regulation (Note 2) 10.6 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 11 Vdc ≤ V_{in} ≤ 17 Vdc 11 Vdc ≤ V_{in} ≤ 17 Vdc, T_J = +25°C 10.4 Vdc ≤ V_{in} ≤ 23 Vdc, T_J = +25°C	Reg_{line}	 — — — —	 12 15 5.0 12	 80 80 40 80	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — — — —	 45 45 — 16	 100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 4.3	6.0 6.0	mA
Quiescent Current Change 11 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 10.6 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 0.8 0.8 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz, T_J = +25°C 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz, I_O = 500 mA	RR	 — —	 — 62	 — —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_I - V_O$	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	18	—	mΩ
Short Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{SC}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	–0.8	—	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXC, AC; T_{high} = +125°C for MC78XXC, AC, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7809CT

ELECTRICAL CHARACTERICISTICS (V_{in} = 15 V, I_O = 500 mA, T_J = 0° to +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	8.65	9.0	9.35	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤15 W) 11.5 Vdc ≤ V_{in} ≤ 24 Vdc	V_O	8.55	9.0	9.45	Vdc
Line Regulation (T_J = +25°C, Note 1) 11.5 Vdc ≤ V_{in} ≤ 26 Vdc 11.5 Vdc ≤ V_{in} ≤ 17 Vdc	Reg_{line}	— —	12 5.0	50 25	mV
Load Regulation (T_J = +25°C, Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	— —	35 12	50 25	mV
Quiescent Current (T_J = +25°C)	I_B	—	4.3	8.0	mA
Quiescent Current Change 11.5 Vdc ≤ V_{in} ≤ 26 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	— —	— —	1.0 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz	RR	—	61	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_I - V_O$	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	18	—	mΩ
Short Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{SC}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	–1.0	—	mV/°C

NOTES: 1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7812B, C

ELECTRICAL CHARACTERICISTICS (V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC7812B			MC7812C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	11.5	12	12.5	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤15 W) 14.5 Vdc ≤ V_{in} ≤ 27 Vdc 15.5 Vdc ≤ V_{in} ≤ 27 Vdc	V_O	 — 11.4	 — 12	 — 12.6	 11.4 —	 12 —	 12.6 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc	Reg_{line}	 — —	 13 6.0	 240 120	 — —	 13 6.0	 240 120	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 46 17	 240 120	 — —	 46 17	 240 120	mV
Quiescent Current (T_J = +25°C)	I_B	—	4.4	8.0	—	4.4	8.0	mA
Quiescent Current Change 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 15 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 — 1.0 0.5	 — — —	 — — —	 1.0 — 0.5	mA
Ripple Rejection 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz	RR	—	60	—	—	60	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_I - V_O$	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	18	—	—	18	-	mΩ
Short Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{SC}	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	–1.0	—	—	–1.0	—	mV/°C

MC7812AC

ELECTRICAL CHARACTERICISTICS (V_{in} = 19 V, I_O = 10 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.75	12	12.25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤15 W) 14.8 Vdc ≤ V_{in} ≤ 27 Vdc	V_O	11.5	12	12.5	Vdc
Line Regulation (Note 2) 14.8 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 16 Vdc ≤ V_{in} ≤ 22 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc, T_J = +25°C 14.5 Vdc ≤ V_{in} ≤ 27 Vdc, T_J = +25°C	Reg_{line}	 — — — —	 13 16 6.0 13	 120 120 60 120	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — — — —	 46 46 — 17	 100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 4.4	6.0 6.0	mA
Quiescent Current Change 15 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 14.8 Vdc ≤ V_{in} ≤ 27 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 0.8 0.8 0.5	mA
Ripple Rejection 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, T_J = +25°C 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, I_O = 500 mA	RR	 —	 —	 —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_I - V_O$	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	18	—	mΩ
Short Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{SC}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	–1.0	—	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXC, AC; T_{high} = +125°C for MC78XXC, AC, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7815B, C

ELECTRICAL CHARACTERICISTICS (V_{in} = 23 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC7815B Min	MC7815B Typ	MC7815B Max	MC7815C Min	MC7815C Typ	MC7815C Max	Unit
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	14.4	15	15.6	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤15 W) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 18.5 Vdc ≤ V_{in} ≤ 30 Vdc	V_O	 — 14.25	 — 15	 — 15.75	 14.25 —	 15 —	 15.75 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc	Reg_{line}	 — —	 13 6.0	 300 150	 — —	 13 6.0	 300 150	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ V_{in} ≤ 1.5 A 250 mA ≤ V_{in} ≤ 750 mA	Reg_{load}	 — —	 52 20	 300 150	 — —	 52 20	 300 150	mV
Quiescent Current (T_J = +25°C)	I_B	—	4.4	8.0	—	4.4	8.0	mA
Quiescent Current Change 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 18.5 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 — 1.0 0.5	 — — —	 — — —	 1.0 — 0.5	mA
Ripple Rejection 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz	RR	—	58	—	—	58	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_I - V_O$	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	19	—	—	19	-	mΩ
Short Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{SC}	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	–1.0	—	—	–1.0	—	mV/°C

MC7815AC

ELECTRICAL CHARACTERICISTICS (V_{in} = 23 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	14.7	15	15.3	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤15 W) 17.9 Vdc ≤ V_{in} ≤ 30 Vdc	V_O	 14.4	 15	 15.6	Vdc
Line Regulation (Note 2) 17.9 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 20 Vdc ≤ V_{in} ≤ 26 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc, T_J = +25°C 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C	Reg_{line}	 — — — —	 13 16 6.0 13	 150 150 75 150	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — — — —	 52 52 — 20	 100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	 —	 —	 6.0	mA
		—	4.4	6.0	
Quiescent Current Change 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA 17.5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 0.8 0.8 0.5	mA
Ripple Rejection 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, T_J = +25°C 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, I_O = 500 mA	RR	 —	 —	 —	dB
		—	58	—	
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_I - V_O$	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	19	—	mΩ
Short Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{SC}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	–1.0	—	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXC, AC; T_{high} = +125°C for MC78XXC, AC, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7818B, C

ELECTRICAL CHARACTERICISTICS (V_{in} = 27 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC7818B			MC7818C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	17.3	18	18.7	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤15 W) 21 Vdc ≤ V_{in} ≤ 33 Vdc 22 Vdc ≤ V_{in} ≤ 33 Vdc	V_O	 — 17.1	 — 18	 — 18.9	 17.1 —	 18 —	 18.9 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 21 Vdc ≤ V_{in} ≤ 33 Vdc 24 Vdc ≤ V_{in} ≤ 30 Vdc	Reg_{line}	 — —	 25 10	 360 180	 — —	 25 10	 360 180	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ V_{in} ≤ 1.5 A 250 mA ≤ V_{in} ≤ 750 mA	Reg_{load}	 — —	 55 22	 360 180	 — —	 55 22	 360 180	mV
Quiescent Current (T_J = +25°C)	I_B	—	4.5	8.0	—	4.5	8.0	mA
Quiescent Current Change 21 Vdc ≤ V_{in} ≤ 33 Vdc 22 Vdc ≤ V_{in} ≤ 33 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 — 1.0 0.5	 — — —	 — — —	 1.0 — 0.5	mA
Ripple Rejection 22 Vdc ≤ V_{in} ≤ 33 Vdc, f = 120 Hz	RR	—	57	—	—	57	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_{il}– V_O	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	19	—	—	19	—	mΩ
Short Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{SC}	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	–1.0	—	—	–1.0	—	mV/°C

MC7818AC

ELECTRICAL CHARACTERICISTICS (V_{in} = 27 V, I_O = 10 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	17.64	18	18.36	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤15 W) 21 Vdc ≤ V_{in} ≤ 33 Vdc	V_O	 17.3	 18	 18.7	Vdc
Line Regulation (Note 2) 21 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA 24 Vdc ≤ V_{in} ≤ 30 Vdc 24 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = +25°C 20.6 Vdc ≤ V_{in} ≤ 33 Vdc, T_J = +25°C	Reg_{line}	 — — — —	 25 28 10 25	 180 180 90 180	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — — — —	 55 55 — 22	 100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	— —	— 4.5	6.0 6.0	mA
Quiescent Current Change 21 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA 21 Vdc ≤ V_{in} ≤ 33 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 0.8 0.8 0.5	mA
Ripple Rejection 22 Vdc ≤ V_{in} ≤ 32 Vdc, f = 120 Hz, T_J = +25°C 22 Vdc ≤ V_{in} ≤ 32 Vdc, f = 120 Hz, I_O = 500 mA	RR	 —	 —	 —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	V_I – V_O	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	19	—	mΩ
Short Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{SC}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	–1.0	—	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXC, AC
= –40°C for MC78XXB
T_{high} = +125°C for MC78XXC, AC, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7824B, C

ELECTRICAL CHARACTERICISTICS (V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC7824B Min	MC7824B Typ	MC7824B Max	MC7824C Min	MC7824C Typ	MC7824C Max	Unit
Output Voltage (T_J = +25°C)	V_O	23	24	25	23	24	25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤15 W) 27 Vdc ≤ V_{in} ≤ 38 Vdc 28 Vdc ≤ V_{in} ≤ 38 Vdc	V_O	 — 22.8	 — 24	 — 25.2	 22.8 —	 24 —	 25.2 —	Vdc
Line Regulation (T_J = +25°C, Note 2) 27 Vdc ≤ V_{in} ≤ 38 Vdc 30 Vdc ≤ V_{in} ≤ 36 Vdc	Reg_{line}	 — —	 31 14	 480 240	 — —	 31 14	 480 240	mV
Load Regulation (T_J = +25°C, Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 60 25	 480 240	 — —	 60 25	 480 240	mV
Quiescent Current (T_J = +25°C)	I_B	—	4.6	8.0	—	4.6	8.0	mA
Quiescent Current Change 27 Vdc ≤ V_{in} ≤ 38 Vdc 28 Vdc ≤ V_{in} ≤ 38 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 — 1.0 0.5	 — — —	 — — —	 1.0 — 0.5	mA
Ripple Rejection 28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz	RR	—	54	—	—	54	—	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_I - V_O$	—	2.0	—	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	—	10	—	μV/V_O
Output Resistance f = 1.0 kHz	r_O	—	20	—	—	20	-	mΩ
Short Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{SC}	—	0.2	—	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	–1.5	—	—	–1.5	—	mV/°C

MC7824AC

ELECTRICAL CHARACTERICISTICS (V_{in} = 33 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	23.5	24	24.5	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_O ≤15 W) 27.3 Vdc ≤ V_{in} ≤ 38 Vdc	V_O	23	24	25	Vdc
Line Regulation (Note 2) 27 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA 30 Vdc ≤ V_{in} ≤ 36 Vdc 30 Vdc ≤ V_{in} ≤ 36 Vdc, T_J = +25°C 26.7 Vdc ≤ V_{in} ≤ 38 Vdc, T_J = +25°C	Reg_{line}	 — — — —	 31 35 14 31	 240 240 120 240	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — — — —	 60 60 — 25	 100 100 — 50	mV
Quiescent Current T_J = +25°C	I_B	 —	 —	 6.0	mA
		—	4.6	6.0	
Quiescent Current Change 27.3 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA 27.3 Vdc ≤ V_{in} ≤ 38 Vdc, T_J = +25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 — — —	 — — —	 0.8 0.8 0.5	mA
Ripple Rejection 28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz, T_J = +25°C 28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz, I_O = 500 mA	RR	 — —	 — 54	 — —	dB
Dropout Voltage (I_O = 1.0 A, T_J = +25°C)	$V_I - V_O$	—	2.0	—	Vdc
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	r_O	—	20	—	mΩ
Short Circuit Current Limit (T_A = +25°C) V_{in} = 35 Vdc	I_{SC}	—	0.2	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	2.2	—	A
Average Temperature Coefficient of Output Voltage	TCV_O	—	–1.5	—	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXC, AC; T_{high} = +125°C for MC78XXC, AC, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Figure 3. Peak Output Current as a Function of Input-Output Differential Voltage (MC78XXC, AC, B)

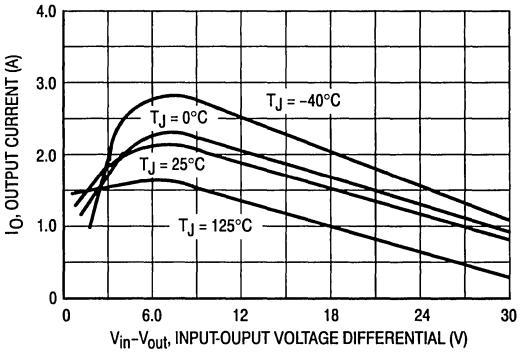


Figure 4. Ripple Rejection as a Function of Output Voltages (MC78XXC, AC)

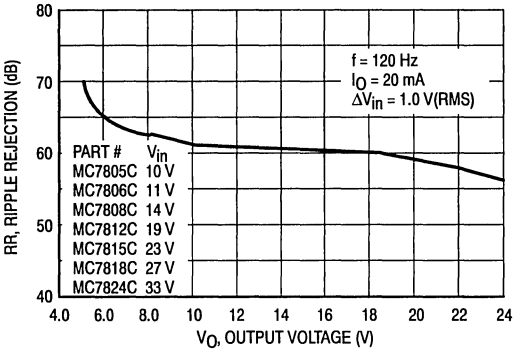


Figure 5. Ripple Rejection as a Function of Frequency (MC78XXC, AC)

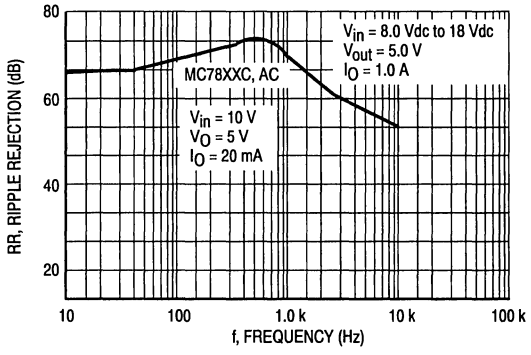


Figure 6. Output Voltage as a Function of Junction Temperature (MC78XXC, AC, B)

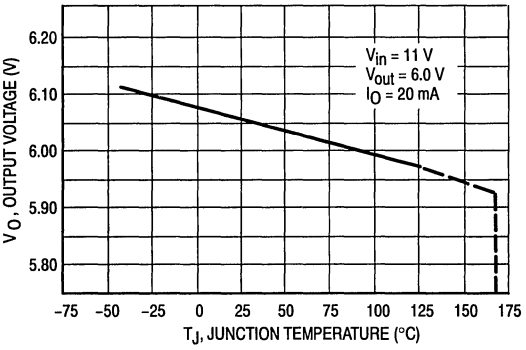


Figure 7. Output Impedance as a Function of Output Voltage (MC78XXC, AC)

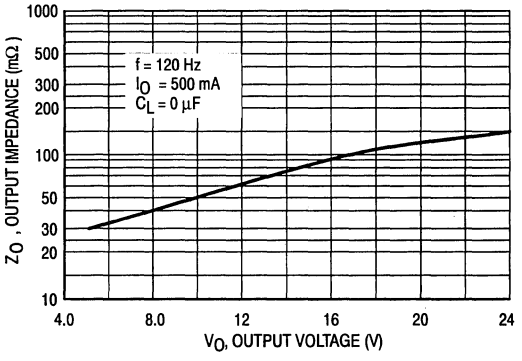
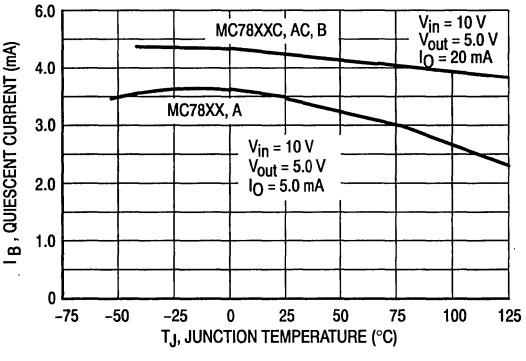


Figure 8. Quiescent Current as a Function of Temperature (MC78XXC, AC, B)



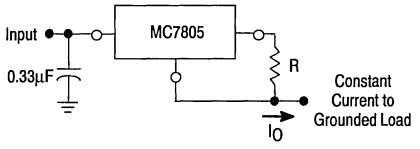
APPLICATIONS INFORMATION

Design Considerations

The MC7800 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 9. Current Regulator



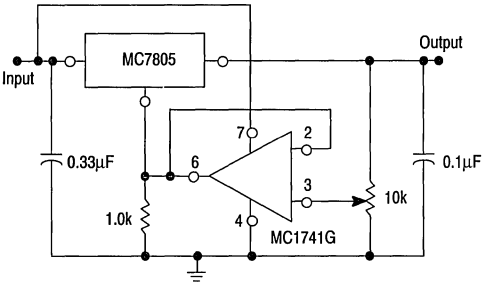
The MC7800 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5\ V}{R} + I_Q$$

$I_Q \cong 1.5$ mA over line and load changes.

For example, a 1 A current source would require R to be a 5 Ω, 10 W resistor and the output voltage compliance would be the input voltage less 7 V.

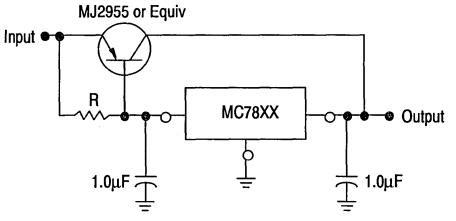
Figure 10. Adjustable Output Regulator



V_O, 7.0 V to 20 V
V_{IN} $V_O \geq 2.0$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 V greater than the regulator voltage.

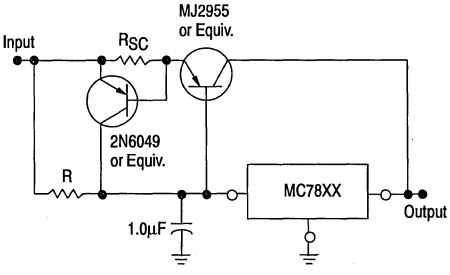
Figure 11. Current Boost Regulator



XX = 2 digits of type number indicating voltage.

The MC7800 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 A. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

Figure 12. Short Circuit Protection



XX = 2 digits of type number indicating voltage.

The circuit of Figure 11 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

MC78L00,A Series

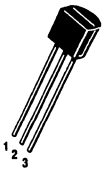
Three-Terminal Low Current Positive Voltage Regulators

The MC78L00 Series of positive voltage regulators are inexpensive, easy-to-use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

These devices offer a substantial performance advantage over the traditional zener diode-resistor combination, as output impedance and quiescent current are substantially reduced.

- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

P SUFFIX
CASE 29



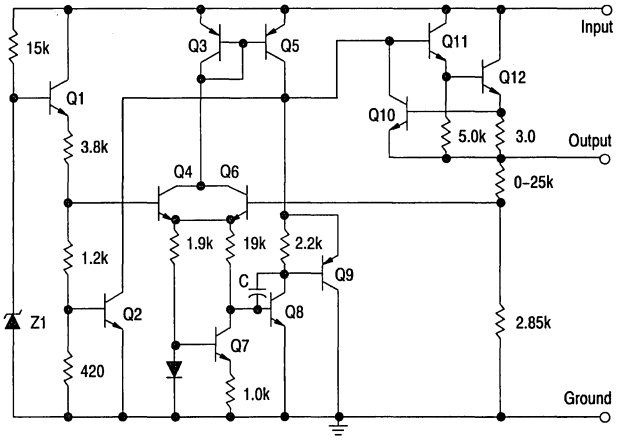
PIN 1. Output
2. GND
3. Input

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP-8)

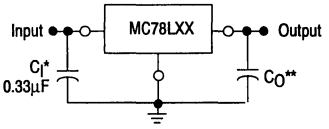
PIN 1. V_{out}
2. GND
3. GND
4. NC
5. NC
6. GND
7. GND
8. V_{in}

SOP-8 is an internally modified SO-8 Package Pins 2, 3, 6, and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

Representative Current Schematic



Standard Application



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

*= C_I is required if regulator is located an appreciable distance from power supply filter.

**= C_O is not needed for stability; however, it does improve transient response.

ORDERING INFORMATION

Device	Junction Temperature Range	Package
MC78LXXACD*	T_J = 0° to +125°C	SOP-8
MC78LXXACP		Plastic Power
MC78LXXCP		Plastic Power
MC78LXXABD*	T_J = –40° to +125°C	SOP-8
MC78LXXABP*		Plastic Power
XX indicates nominal voltage		

*Available in 5, 8, 9, 12 and 15 V devices.

Device No. 10%	Device No. 5%	Nominal Voltage
MC78L05C	MC78L05AC	5.0
MC78L08C	MC78L08AC	8.0
MC78L09C	MC78L09AC	9.0
MC78L12C	MC78L12AC	12
MC78L15C	MC78L15AC	15
MC78L18C	MC78L18AC	18
MC78L24C	MC78L24AC	24

MAXIMUM RATINGS (T_A = +125°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.6 V–8.0 V) (12 V–18 V) (24 V)	V_I	30 35 40	Vdc
Storage Junction Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

MC78L05C, MC78L05AC ELECTRICAL CHARACTERICISTICS (V_I = 10 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	MC78L05AC			MC78L05C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	4.6	5.0	5.4	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 7.0 Vdc ≤ V_I ≤ 20 Vdc 8.0 Vdc ≤ V_I ≤ 20 Vdc	Reg_{line}	 — —	 55 45	 150 100	 — —	 55 45	 200 150	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 1.1 5.0	 60 30	 — —	 11 5.0	 60 30	mV
Output Voltage (7.0 Vdc ≤ V_I ≤ 20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 10 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 4.75 4.75	 — —	 5.25 5.25	 4.5 4.5	 — —	 5.5 5.5	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 3.8 —	 6.0 5.5	 — —	 3.8 —	 6.0 5.5	mA
Input Bias Current Change (8.0 Vdc ≤ V_I ≤ 20 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	40	—	—	40	—	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 8.0 Vdc ≤ V_I ≤ 18 V, T_J = +25°C)	RR	41	49	—	40	49	—	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	—	1.7	—	—	1.7	—	Vdc

MC78L08C, MC78L08AC ELECTRICAL CHARACTERICISTICS (V_I = 14 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	MC78L08AC			MC78L08C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	7.36	8.0	8.64	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 10.5 Vdc ≤ V_I ≤ 23 Vdc 11 Vdc ≤ V_I ≤ 23 Vdc	Reg_{line}	 — —	 20 12	 175 125	 — —	 20 12	 200 150	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 15 8.0	 80 40	 — —	 15 6.0	 80 40	mV
Output Voltage (10.5 Vdc ≤ V_I ≤ 23 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 14 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 7.6 7.6	 — —	 8.4 8.4	 7.2 7.2	 — —	 8.8 8.8	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 3.0 —	 6.0 5.5	 — —	 3.0 —	 6.0 5.5	mA
Input Bias Current Change (11 Vdc ≤ V_I ≤ 23 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	60	—	—	52	—	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 12 V ≤ V_I ≤ 23 V, T_J = +25°C)	RR	37	57	—	36	55	—	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	—	1.7	—	—	1.7	—	Vdc

MC78L09C, MC78L09AC ELECTRICAL CHARACTERICISTICS (V_I = 15 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	MC78L09AC			MC78L09C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	8.6	9.0	9.4	8.3	9.0	9.7	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 11.5 Vdc ≤ V_I ≤ 24 Vdc 12 Vdc ≤ V_I ≤ 24 Vdc	Reg_{line}	 — —	 20 12	 175 125	 — —	 20 12	 200 150	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 15 8.0	 90 40	 — —	 15 6.0	 90 40	mV
Output Voltage (11.5 Vdc ≤ V_I ≤ 24 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 15 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 8.5 8.5	 — —	 9.5 9.5	 8.1 8.1	 — —	 9.9 9.9	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 3.0 —	 6.0 5.5	 — —	 3.0 —	 6.0 5.5	mA
Input Bias Current Change (11 Vdc ≤ V_I ≤ 23 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	60	—	—	52	—	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 13 V ≤ V_I ≤ 24 V, T_J = +25°C)	RR	37	57	—	36	55	—	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	—	1.7	—	—	1.7	—	Vdc

MC78L12C, MC78L12AC ELECTRICAL CHARACTERICISTICS (V_I = 19 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	MC78L12AC			MC78L12C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	11.1	12	12.9	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 14.5 Vdc ≤ V_I ≤ 27 Vdc 16 Vdc ≤ V_I ≤ 27 Vdc	Reg_{line}	 — —	 120 100	 250 200	 — —	 120 100	 250 200	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 20 10	 100 50	 — —	 20 10	 100 50	mV
Output Voltage (14.5 Vdc ≤ V_I ≤ 27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 19 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 11.4 11.4	 — —	 12.6 12.6	 10.8 10.8	 — —	 13.2 13.2	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 4.2 —	 6.5 6.0	 — —	 4.2 —	 6.5 6.0	mA
Input Bias Current Change (16 Vdc ≤ V_I ≤ 27 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	80	—	—	80	—	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = +25°C)	RR	37	42	—	36	42	—	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	—	1.7	—	—	1.7	—	Vdc

MC78L15C, MC78L15AC ELECTRICAL CHARACTERICISTICS (V_I = 23 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	MC78L15AC			MC78L15C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	13.8	15	16.2	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 17.5 Vdc ≤ V_I ≤ 30 Vdc 20 Vdc ≤ V_I ≤ 30 Vdc	Reg_{line}	 — —	 130 110	 300 250	 — —	 130 110	 300 250	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 25 12	 150 75	 — —	 25 12	 150 75	mV
Output Voltage (17.5 Vdc ≤ V_I ≤ 30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 23 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 14.25 14.25	 — —	 15.75 15.75	 13.5 13.5	 — —	 16.5 16.5	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 4.4 —	 6.5 6.0	 — —	 4.4 —	 6.5 6.0	mA
Input Bias Current Change (20 Vdc ≤ V_I ≤ 30 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	90	—	—	90	—	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = +25°C)	RR	34	39	—	33	39	—	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	—	1.7	—	—	1.7	—	Vdc

MC78L18C, MC78L18AC ELECTRICAL CHARACTERICISTICS (V_I = 27 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	MC78L18AC			MC78L18C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	16.6	18	19.4	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 21.4 Vdc ≤ V_I ≤ 33 Vdc 20.7 Vdc ≤ V_I ≤ 33 Vdc 22 Vdc ≤ V_I ≤ 33 Vdc 21 Vdc ≤ V_I ≤ 33 Vdc	Reg_{line}	 — —	 45 35	 325 275	 — —	 32 27	 325 275	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 30 15	 170 85	 — —	 30 15	 170 85	mV
Output Voltage (21.4 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (20.7 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA) (V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 17.1 17.1	 — —	 18.9 18.9	 16.2 16.2 	 — —	 19.8 19.8	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 3.1 —	 6.5 6.0	 — —	 3.1 —	 6.5 6.0	mA
Input Bias Current Change (22 Vdc ≤ V_I ≤ 33 Vdc) (21 Vdc ≤ V_I ≤ 33 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	150	—	—	150	—	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 23 V ≤ V_I ≤ 33 V, T_J = +25°C)	RR	33	48	—	32	46	—	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	—	1.7	—	—	1.7	—	Vdc

MC78L24C, MC78L24AC ELECTRICAL CHARACTERICISTICS (V_I = 33 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	MC78L24AC			MC78L24C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	23	24	25	22.1	24	25.9	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 27.5 Vdc ≤ V_I ≤ 38 Vdc 28 Vdc ≤ V_I ≤ 80 Vdc 27 Vdc ≤ V_I ≤ 38 Vdc	Reg_{line}	 — — —	 — 50 60	 — 300 350	 — — —	 35 30 —	 350 300 —	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 — —	 40 20	 200 100	 — —	 40 20	 200 100	mV
Output Voltage (28 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (27 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (28 Vdc ≤ V_I = 33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA) (27 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 22.8 22.8	 — —	 25.2 25.2	 21.6 21.6 	 — —	 26.4 26.4 	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 3.1 —	 6.5 6.0	 — —	 3.1 —	 6.5 6.0	mA
Input Bias Current Change (28 Vdc ≤ V_I ≤ 38 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 — —	 — —	 1.5 0.1	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	200	—	—	200	—	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 29 V ≤ V_I ≤ 35 V, T_J = +25°C)	RR	31	45	—	30	43	—	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	—	1.7	—	—	1.7	—	Vdc

Figure 1. Dropout Characteristics

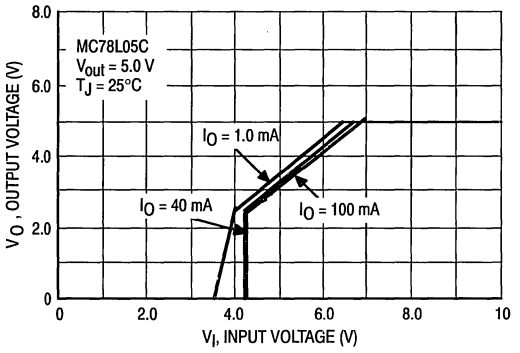


Figure 2. Dropout Voltage versus Junction Temperature

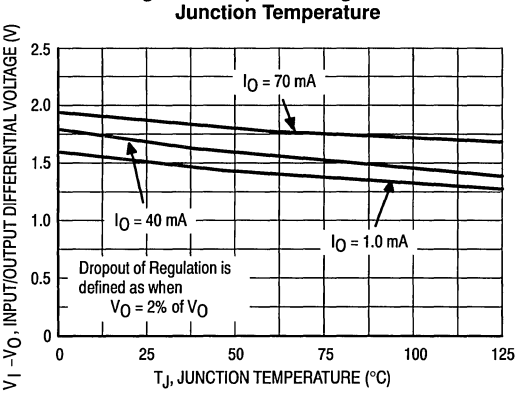


Figure 3. Input Bias Current versus Ambient Temperature

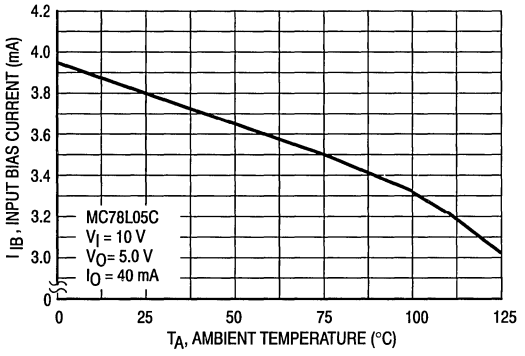


Figure 4. Input Bias Current versus Input Voltage

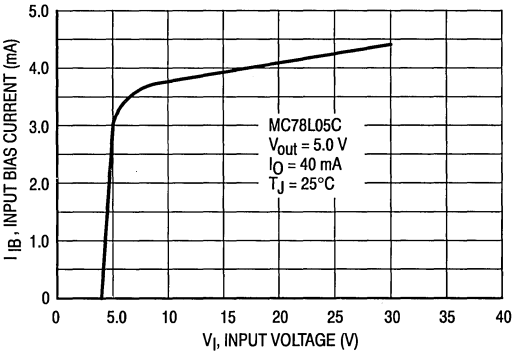
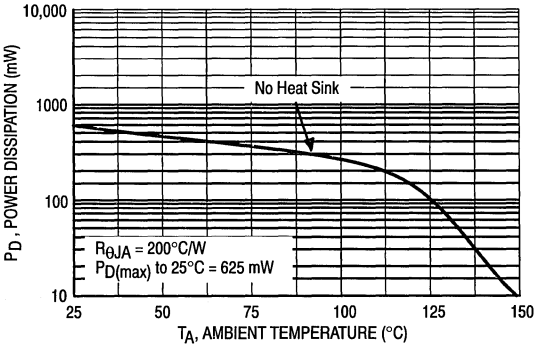


Figure 5. Maximum Average Power Dissipation versus Ambient Temperature — TO-92 Type Package



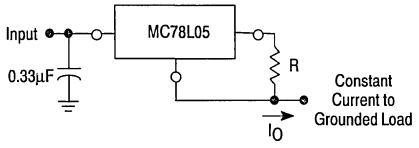
APPLICATIONS INFORMATION

Design Considerations

The MC78L00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short Circuit Protection limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. The input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen.The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Good construction techniques should be used to minimize ground loops and lead resistance drops since the regular has no external sense lead. Bypassing the output is also recommended.

Figure 6. Current Regulator



The MC78L00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

I_B = 3.8 mA over line and load changes

For example, a 100 mA current source would require R to be a 50 Ω, 1/2 W resistor and the output voltage compliance would be the input voltage less 7 V.

Figure 7. ± 15 V Tracking Voltage Regulator

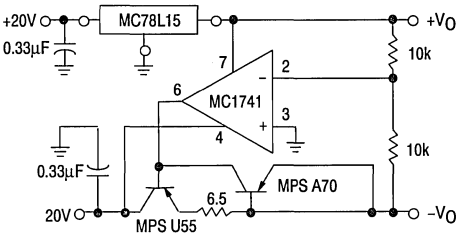
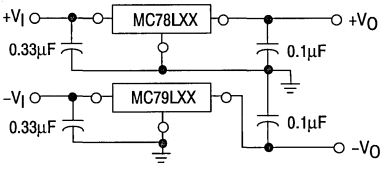


Figure 8. Positive and Negative Regulator



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC78M00 Series

3

Three-Terminal Medium Current Positive Voltage Regulators

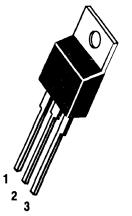
THREE-TERMINAL MEDIUM CURRENT POSITIVE FIXED VOLTAGE REGULATORS

The MC78M00 Series positive voltage regulators are identical to the popular MC7800 Series devices, except that they are specified for only half the output current. Like the MC7800 devices, the MC78M00 three-terminal regulators are intended for local, on-card voltage regulation.

Internal current limiting, thermal shutdown circuitry and safe-area compensation for the internal pass transistor combine to make these devices remarkably rugged under most operating conditions. Maximum output current, with adequate heatsinking is 500 mA.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation

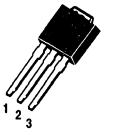
T SUFFIX
PLASTIC PACKAGE
CASE 221A



(All 3 Plastic Types)
Pin 1. Input
2. Ground
3. Output

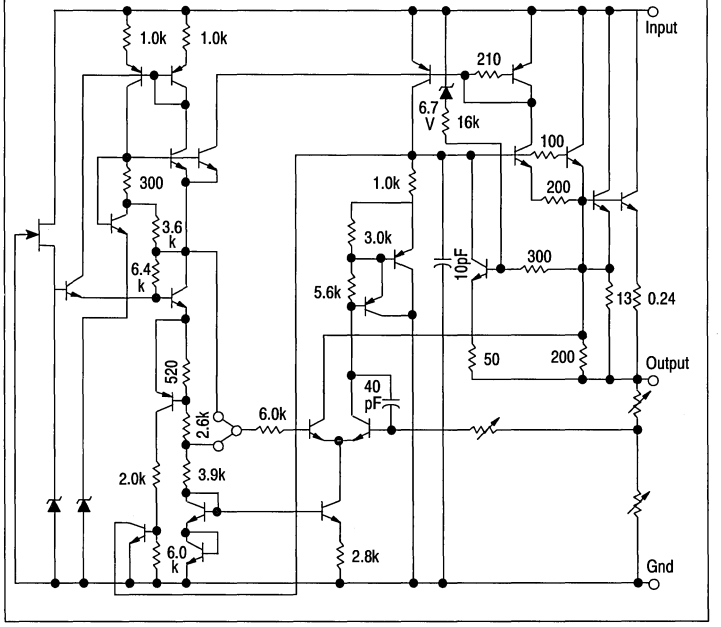
Heatsink surface connected to Pin 2

DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)



DT-1 SUFFIX
PLASTIC PACKAGE
CASE 369
(DPAK)

Equivalent Schematic Diagram



ORDERING INFORMATION

Device	Tested Operating Junction Temp. Range	Package
MC78MXXCDT* MC78MXXCDT-1*	T_J = 0° to +125°C	DPAK
MC78MXXCT		Plastic Power
MC78MXXBT#	T_J = −40° to +125°C	

TYPE NO./VOLTAGE		
MC78M05B,C 5.0 V	MC78M12B,C 12 V	MC78M20B,C 20 V
MC78M06B,C 6.0 V	MC78M15B,C 15 V	MC78M24B,C 24 V
MC78M08B,C 8.0 V	MC78M18B,C 18 V	

XX Indicates nominal voltage.
* Available in 5, 8, 12 and 15 V devices.
\# Automotive temperature range selections are available with special test conditions and additional tests in 5, 8, 12 and 15 V devices. Contact your local Motorola sales office for information.

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V–18 V) (20 V–24V)	V_I	35 40	Vdc
Power Dissipation (Package Limitation) Plastic Package, T Suffix T_A = 25°C Derate above T_A = 25°C T_C = 25°C Derate above T_C = 110°C	 P_D θ_{JA} P_D θ_{JC}	 Internally Limited 70 Internally Limited 5.0	 °C/W °C/W
Operating Junction Temperature Range	T_J	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

MC78M05B,C ELECTRICAL CHARACTERICISTICS (V_I = 10 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	Vdc
Line Regulation (T_J = +25°C, 7.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA)	Reg_{line}	—	3.0	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 20 10	 100 50	mV
Output Voltage (7.0 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA) (7.0 Vdc ≤ V_I ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	4.75	—	5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change (8.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	40	—	μV
Ripple Rejection (T, DT and DT-1 suffixes only) (I_O = 100 mA, f = 120 Hz, 8.0 V ≤ V_I ≤ 18 V) (I_O = 300 mA, f = 120 Hz, 8.0 ≤ V_I ≤ 18 V, T_J = 25°C)	RR	 62 62	 — 80	 — —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.2	—	mV/°C
Peak Output Current (T_J = +25°C)	I_O	—	700	—	mA

MC78M06C ELECTRICAL CHARACTERICISTICS (V_I = 11 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	5.75	6.0	6.25	Vdc
Line Regulation (T_J = +25°C, 8.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA)	Reg_{line}	—	5.0	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	— —	20 10	120 60	mV
Output Voltage (8.0 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA) (8.0 Vdc ≤ V_I ≤ 21 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	5.7	—	6.3	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change (9.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	45	—	μV
Ripple Rejection (T suffix only) (I_O = 100 mA, f = 120 Hz, 9.0 V ≤ V_I ≤ 19 V) (I_O = 300 mA, f = 120 Hz, 9.0 V ≤ V_I ≤ 19 V, T_J = 25°C)	RR	59 59	— 80	— —	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.2	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M08B,C ELECTRICAL CHARACTERICISTICS (V_I = 14 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	Vdc
Line Regulation (T_J = +25°C, 10.5 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA)	Reg_{line}	—	6.0	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	— —	25 10	160 80	mV
Output Voltage (10.5 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA) (10.5 Vdc ≤ V_I ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	7.6	—	8.4	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change (10.5 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	— —	— —	0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	52	—	μV
Ripple Rejection (T suffix only) (I_O = 100 mA, f = 120 Hz, 11.5 V ≤V_I ≤ 21.5 V) (I_O = 300 mA, f = 120 Hz, 11.5 V ≤V_I ≤ 21.5 V, T_J = 25°C)	RR	56 56	— 80	— —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.2	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M12B,C ELECTRICAL CHARACTERICISTICS (V_I = 19 V, I_O = 350 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	Vdc
Line Regulation (T_J = +25°C, 14.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA)	Reg_{line}	—	8.0	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 25 10	 240 120	mV
Output Voltage (14.5 Vdc ≤ V_I ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	11.4	—	12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change (14.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	75	—	μV
Ripple Rejection (T, DT and DT-1 suffixes only) (I_O = 100 mA, f = 120 Hz, 15 V ≤V_I ≤ 25 V) (I_O = 300 mA, f = 120 Hz, 15 V ≤V_I ≤ 25 V, T_J = 25°C)	RR	 55 55	 — 80	 — —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.3	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M15B,C ELECTRICAL CHARACTERICISTICS (V_I = 23 V, I_O = 350 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	Vdc
Input Regulation (T_J = +25°C, 17.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA)	Reg_{line}	—	10	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 25 10	 300 150	mV
Output Voltage (17.5 Vdc ≤ V_I ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	14.25	—	15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.0	mA
Quiescent Current Change (17.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	90	—	μV
Ripple Rejection (T, DT and DT-1 suffixes only) (I_O = 100 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V) (I_O = 300 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = 25°C)	RR	 54 54	 — 70	 — —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.3	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M18C ELECTRICAL CHARACTERICISTICS (V_I = 27 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	Vdc
Line Regulation (T_J = +25°C, 21 Vdc ≤ V_I ≤ 33 Vdc, I_O = 200 mA)	Reg_{line}	—	10	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 30 10	 360 180	mV
Output Voltage (21 Vdc ≤ V_I ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	17.1	—	18.9	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.5	mA
Quiescent Current Change (21 Vdc ≤ V_I ≤ 33 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	100	—	μV
Ripple Rejection (T suffix only) (I_O = 100 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V) (I_O = 300 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V, T_J = 25°C)	RR	 53 53	 — 70	 — —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.3	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M20C ELECTRICAL CHARACTERICISTICS (V_I = 29 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	19.2	20	20.8	Vdc
Line Regulation (T_J = +25°C, 23 Vdc ≤ V_I ≤ 35 Vdc, I_O = 200 mA)	Reg_{line}	—	10	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 30 10	 400 200	mV
Output Voltage (23 Vdc ≤ V_I ≤ 35 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	19	—	21	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	6.5	mA
Quiescent Current Change (23 Vdc ≤ V_I ≤ 35 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	110	—	μV
Ripple Rejection (T suffix only) (I_O = 100 mA, f = 120 Hz, 24 V ≤ V_I ≤ 34 V) (I_O = 300 mA, f = 120 Hz, 24 V ≤ V_I ≤ 34 V, T_J = 25°C)	RR	 52 52	 — 70	 — —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C, V_I = 35 V)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.5	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

MC78M24C ELECTRICAL CHARACTERICISTICS (V_I = 33 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	23	24	25	Vdc
Line Regulation (T_J = +25°C, 27 Vdc ≤ V_I ≤ 38 Vdc, I_O = 200 mA)	Reg_{line}	—	10	50	mV
Load Regulation (T_J = +25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = +25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 — —	 30 10	 480 240	mV
Output Voltage (27 Vdc ≤ V_I ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	22.8	—	25.2	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	3.2	7.0	mA
Quiescent Current Change (27 Vdc ≤ V_I ≤ 38 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 — —	 — —	 0.8 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	170	—	μV
Ripple Rejection (T suffix only) (I_O = 100 mA, f = 120 Hz, 28 V ≤ V_I ≤ 38 V) (I_O = 300 mA, f = 120 Hz, 28 V ≤ V_I ≤ 38 V, T_J = 25°C)	RR	 50 50	 — 70	 — —	dB
Dropout Voltage (T_J = +25°C)	V_I-V_O	—	2.0	—	Vdc
Short Circuit Current Limit (T_J = +25°C)	I_{OS}	—	50	—	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	—	±0.5	—	mV/°C
Peak Output Current (T_J = 25°C)	I_O	—	700	—	mA

DEFINTIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

Figure 1. Worst Case Power Dissipation versus Ambient Temperature

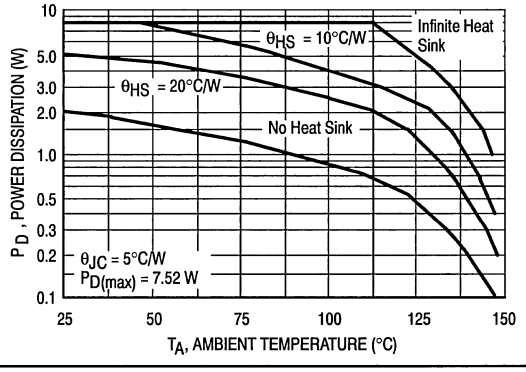


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Figure 2. Peak Output Current versus Dropout Voltage

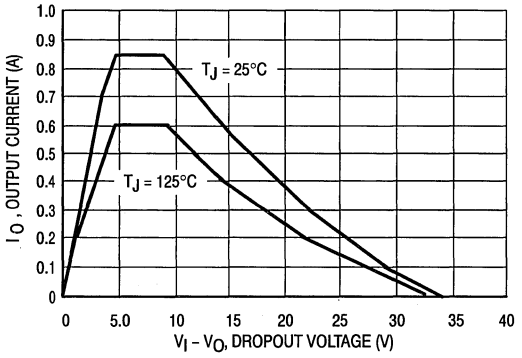


Figure 3. Dropout Voltage versus Junction Temperature

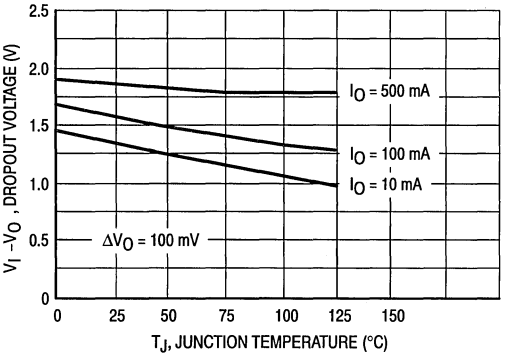


Figure 4. Ripple Rejection versus Frequency

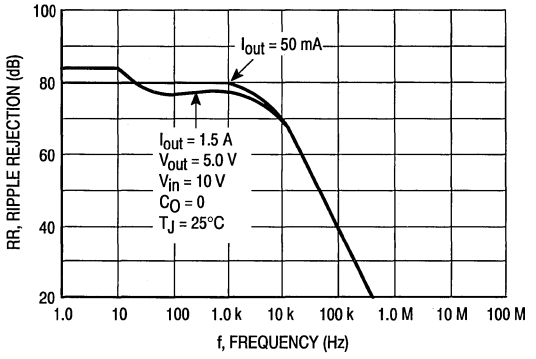


Figure 5. Ripple Rejection versus Output Current

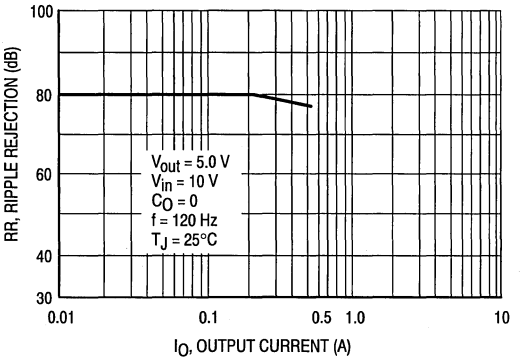


Figure 6. Bias Current versus Input Voltage

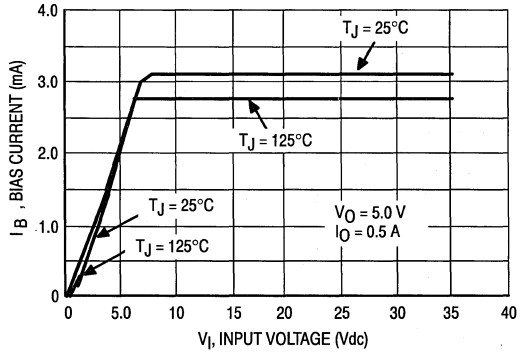
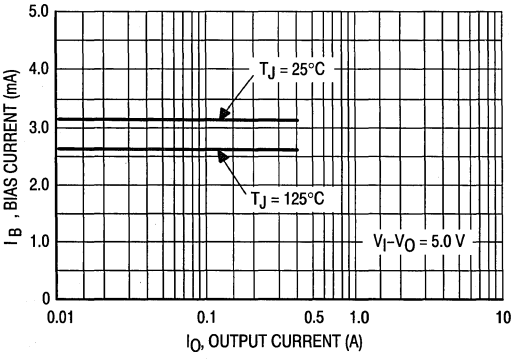


Figure 7. Bias Current versus Output Current



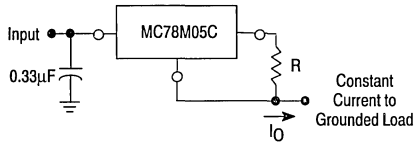
APPLICATIONS INFORMATION

Design Considerations

The MC78M00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 8. Current Regulator



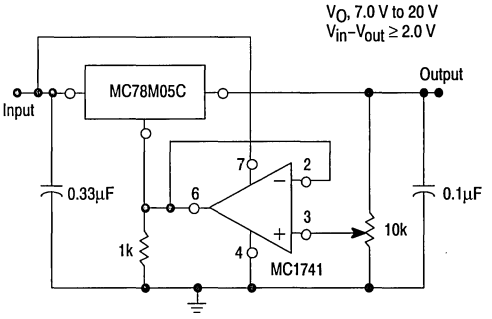
The MC78M00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78M05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_{IB}$$

I_{IB} = 1.5 mA over line and load changes.

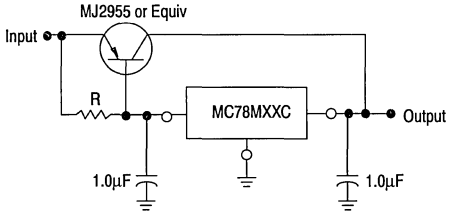
For example, a 500 mA current source would require R to be a 5 Ω, 10 W resistor and the output voltage compliance would be the input voltage less 7 V.

Figure 9. Adjustable Output Regulator



The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 V greater than the regulator voltage.

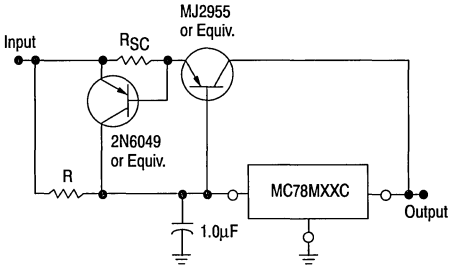
Figure 10. Current Boost Regulator



XX = 2 digits of type number indicating voltage.

The MC78M00 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 A. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input-output differential voltage minimum is increased by V_{BE} of the pass transistor.

Figure 11. Current Boost with Short Circuit Protection



XX = 2 digits of type number indicating voltage.

The circuit of Figure 10 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three-terminal regulator. Therefore, a 4 A plastic power transistor is specified.

MC78T00 Series

Three-Ampere Positive Voltage Regulators

THREE-AMPERE POSITIVE FIXED VOLTAGE REGULATORS

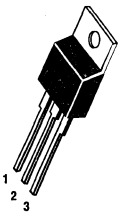
3

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 3.0 A. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance, on AC-suffix 5.0, 12 and 15 V device types.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series-pass transistor to supply up to 15 A at the nominal output voltage.

- Output Current in Excess of 3.0 A
- Power Dissipation: 25 W
- No External Components Required
- Output Voltage Offered in 2% and 4% Tolerance*
- Thermal Regulation is Specified
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation

T SUFFIX
PLASTIC PACKAGE
CASE 221A



Pin 1. Input
2. Ground
3. Output

Heatsink surface connected to Pin 2

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V – 12 V) (15 V)	V_I	35 40	Vdc
Power Dissipation and Thermal Characteristics Plastic Package (Note 1) T_A = +25°C Thermal Resistance, Junction to Air T_C = +25°C Thermal Resistance, Junction to Case	 P_D $R_{\theta JA}$ P_D $R_{\theta JC}$	 Internally Limited 65 Internally Limited 2.5	 °C/W °C/W
Storage Junction Temperature	T_{stg}	+150	°C
Operating Junction Temperature Range MC78T00C, AC	T_J	0 to +150	°C

NOTES: 1. Although power dissipation is internally limited, specifications apply only for $P_O \leq P_{max}$, P_{max} = 25 W.

ORDERING INFORMATION

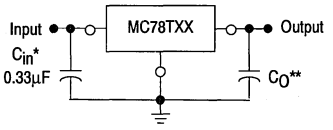
Device	V_O Tol.	Tested Operating Junction Temp. Range	Package
MC78TXXCT	4%	0° to	Plastic
MC78TXXACT	2%*	+125°C	Power
MC78TXXBT#	4%	–40° to	Plastic
MC78TXXABT#	2%*	+125°C	Power

XX Indicates nominal voltage.

* 2% regulators available in 5, 12 and 15 V devices.

\# Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

Standard Application



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.2 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details.)

** = C_O is not needed for stability; however, it does improve transient response.

TYPE NO./VOLTAGE			
MC78T05	5.0 V	MC78T12	12 V
MC78T08	8.0 V	MC78T15	15 V

MC78T05AC,C

ELECTRICAL CHARACTERICISTICS (V_{in} = 10 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC78T05AC			MC78T05C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 7.3 Vdc ≤ V_{in} ≤ 20Vdc)	V_O	 4.9 4.8	 5.0 5.0	 5.1 5.2	 4.8 4.75	 5.0 5.0	 5.2 5.25	Vdc
Line Regulation (Note 2) (7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C; 8.0 Vdc ≤ V_{in} ≤ 12 Vdc, I_O = 3.0 A, T_J = +25°C; 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A)	Reg_{line}	—	3.0	25	—	3.0	25	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	 — —	 10 15	 30 80	 — —	 10 15	 30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	 — —	 3.5 4.0	 5.0 6.0	 — —	 3.5 4.0	 5.0 6.0	mA
Quiescent Current Change (7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A)	ΔI_B	—	0.3	1.0	—	0.3	1.0	mA
Ripple Rejection (8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	62	75	—	62	75	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}–V_O	—	2.2	2.5	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	—	10	—	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	—	20	—	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	—	1.5	—	—	1.5	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	—	0.2	—	—	0.2	—	mV/°C

NOTES: 1. Although power dissipation is internally limited, specifications apply only for P_O ≤ P_{max}, P_{max} = 25 W.
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC78T08C

ELECTRICAL CHARACTERICISTICS (V_{in} = 13 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC78T08C Min	MC78T08C Typ	MC78T08C Max	Unit
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 10.4 Vdc ≤ V_{in} ≤ 23 Vdc)	V_O	 7.7 7.6	 8.0 8.0	 8.3 8.4	Vdc
Line Regulation (Note 2) (10.3 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C 10.3 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C 11 Vdc ≤ V_{in} ≤ 17 Vdc, I_O = 3.0 A, T_J = +25°C 10.7 Vdc ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A)	Reg_{line}	—	4.0	35	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	 — —	 10 15	 30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	 — —	 3.5 4.0	 5.0 6.0	mA
Quiescent Current Change (10.3 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 10.7 Vdc ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A)	ΔI_B	—	0.3	1.0	mA
Ripple Rejection (11 Vdc ≤ V_{in} ≤ 21 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	60	71	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}–V_O	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	—	1.5	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	—	0.3	—	mV/°C

MC78T12AC,C

ELECTRICAL CHARACTERICISTICS (V_{in} = 17 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC78T12AC			MC78T12C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A, 5.0 mA ≤ I_O ≤ 2.0 A, 14.5 Vdc ≤ V_{in} ≤ 27Vdc)	V_O	 11.75 11.5	 12 12	 12.25 12.5	 11.5 11.4	 12 12	 12.5 12.6	Vdc
Line Regulation (Note 2) (14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C; 16 Vdc ≤ V_{in} ≤ 22 Vdc, I_O = 3.0 A, T_J = +25°C; 14.9 Vdc ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A)	Reg_{line}	—	6.0	45	—	6.0	45	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	 — —	 10 15	 30 80	 — —	 10 15	 30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	 — —	 3.5 4.0	 5.0 6.0	 — —	 3.5 4.0	 5.0 6.0	mA
Quiescent Current Change (14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 14.9 Vdc ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A)	ΔI_B	—	0.3	1.0	—	0.3	1.0	mA
Ripple Rejection (15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	57	67	—	57	67	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	$V_{in} - V_O$	—	2.2	2.5	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	—	10	—	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	—	20	—	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	—	1.5	—	—	1.5	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	—	0.5	—	—	0.5	—	mV/°C

MC78T15AC,C

ELECTRICAL CHARACTERICISTICS (V_{in} = 20 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC78T15AC			MC78T15C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 17.5 Vdc ≤ V_{in} ≤ 30Vdc)	V_O	 14.7 14.4	 15 15	 15.3 15.6	 14.4 14.25	 15 15	 15.6 15.75	Vdc
Line Regulation (Note 2) (17.6 Vdc ≤ V_{in} ≤ 40 Vdc, I_O = 5.0 mA, T_J = +25°C; 17.6 Vdc ≤ V_{in} ≤ 40 Vdc, I_O = 1.0 A, T_J = +25°C; 20 Vdc ≤ V_{in} ≤ 26 Vdc, I_O = 3.0 A, T_J = +25°C; 18 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A)	Reg_{line}	—	7.5	55	—	7.5	55	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	 — —	 10 15	 30 80	 — —	 10 15	 30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	—	0.001	0.01	—	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	 — —	 3.5 4.0	 5.0 6.0	 — —	 3.5 4.0	 5.0 6.0	mA
Quiescent Current Change (17.6 Vdc ≤ V_{in} ≤ 40 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 18 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A)	ΔI_B	—	0.3	1.0	—	0.3	1.0	mA
Ripple Rejection (18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	55	65	—	55	65	—	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	V_{in}–V_O	—	2.2	2.5	—	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	—	10	—	—	10	—	μV/V_O
Output Resistance (f = 1.0 kHz)	R_O	—	2.0	—	—	20	—	mΩ
Short Circuit Current Limit (V_{in} = 40 Vdc, T_J = +25°C)	I_{SC}	—	1.0	—	—	1.0	—	A
Peak Output Current (T_J = +25°C)	I_{max}	—	5.0	—	—	5.0	—	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	—	0.6	—	—	0.6	—	mV/°C

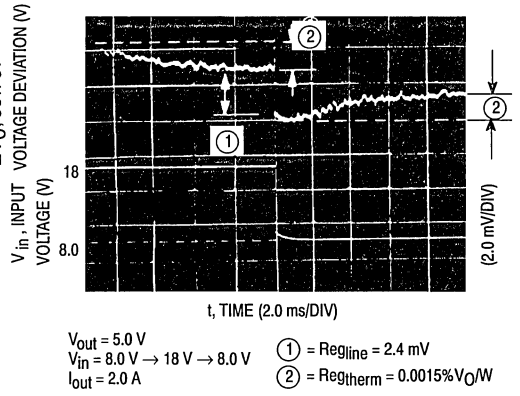
VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical MC78T05AC to a 20 W input pulse. The variation of the output voltage due to line regulation is labeled À and the thermal regulation component is labeled Á. Figure 2 shows the load and thermal regulation response of a typical MC78T05AC to a 20 W load pulse. The output voltage variation due to load regulation is labeled À and the thermal regulation component is labeled Á.

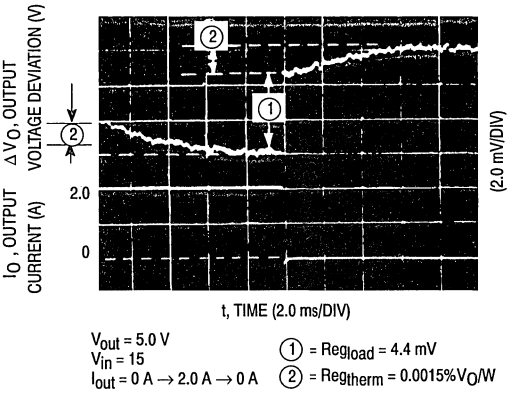
Figure 1. MC78T05AC Line and Thermal Regulation



V_{out} = 5.0 V
V_{in} = 8.0 V → 18 V → 8.0 V
I_{out} = 2.0 A

① = Reg_{line} = 2.4 mV
② = Reg_{therm} = 0.0015%V_O/W

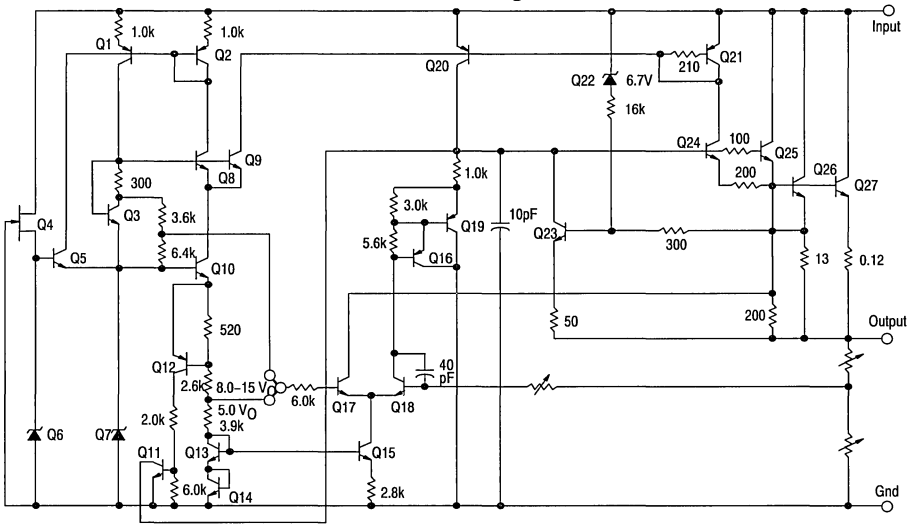
Figure 2. MC78T05AC Load and Thermal Regulation



V_{out} = 5.0 V
V_{in} = 15
I_{out} = 0 A → 2.0 A → 0 A

① = Reg_{load} = 4.4 mV
② = Reg_{therm} = 0.0015%V_O/W

Schematic Diagram



3

Figure 3. Temperature Stability

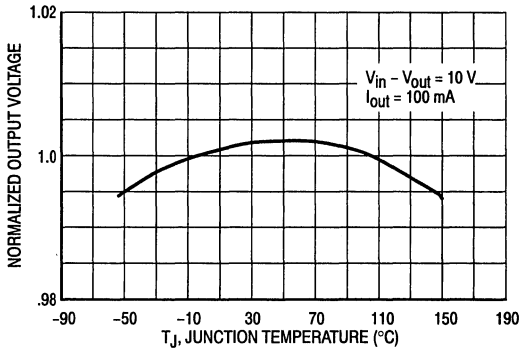


Figure 4. Output Impedance

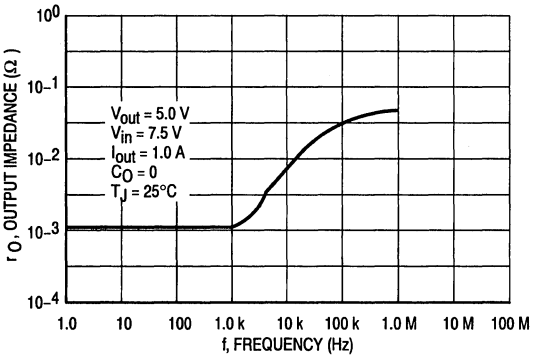


Figure 5. Ripple Rejection versus Frequency

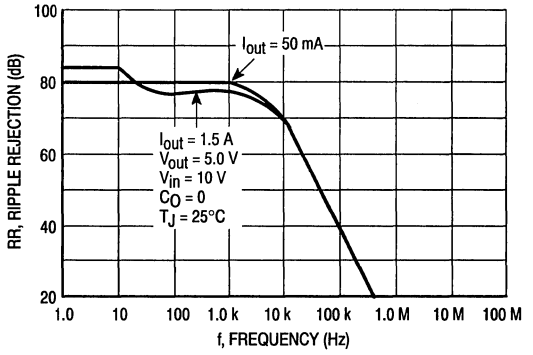


Figure 6. Ripple Rejection versus Output Current

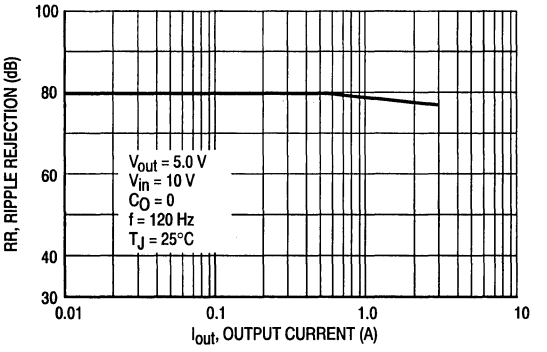


Figure 7. Quiescent Current versus Input Voltage

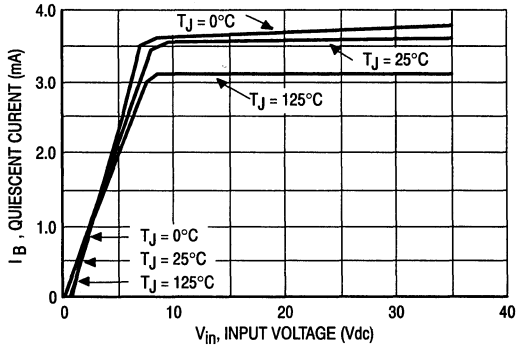


Figure 8. Quiescent Current versus Output Current

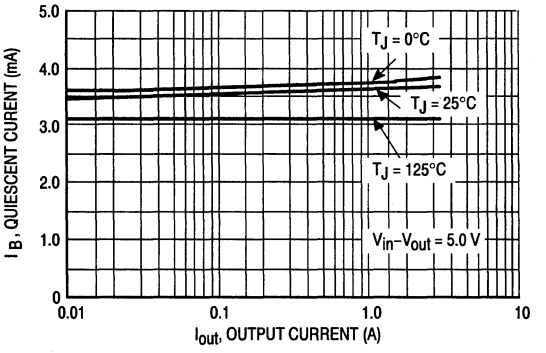


Figure 9. Dropout Voltage

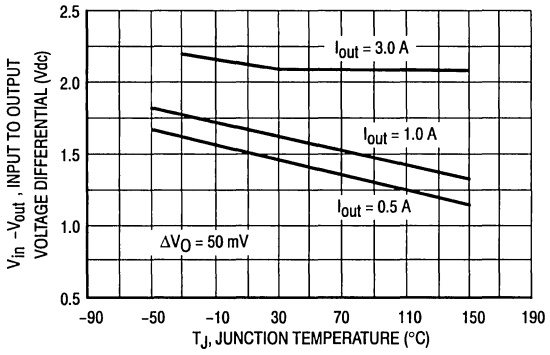


Figure 10. Peak Output Current

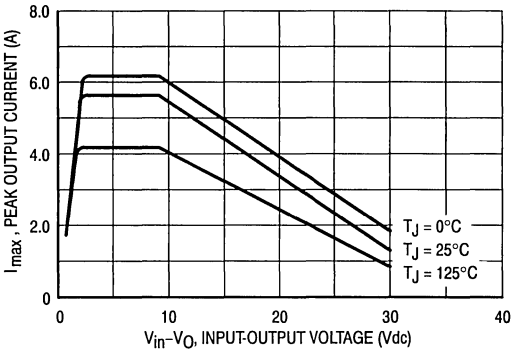


Figure 11. Line Transient Response

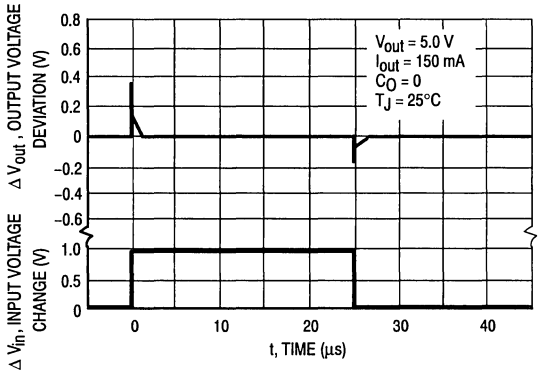


Figure 12. Load Transient Response

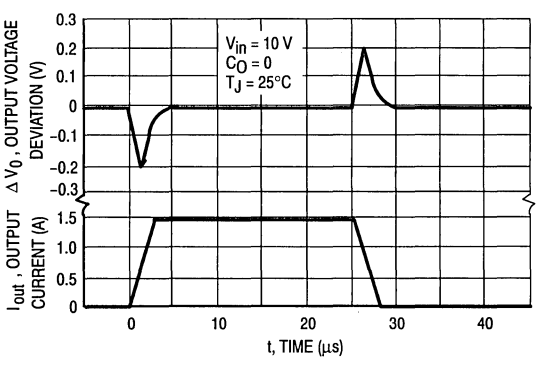


Figure 13. Maximum Average Power Dissipation for MC78T00CK, ACK

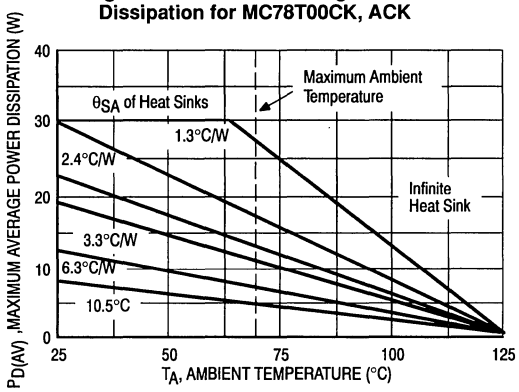
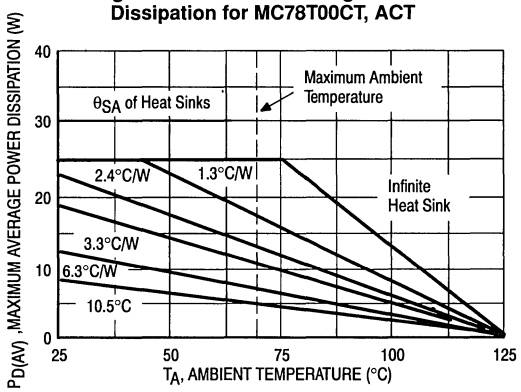


Figure 14. Maximum Average Power Dissipation for MC78T00CT, ACT



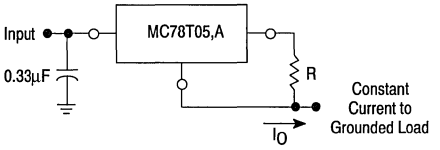
APPLICATIONS INFORMATION

Design Considerations

The MC78T00,A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high frequency characteristics to insure stable operation under all load conditions. A 0.33 µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 15. Current Regulator



The MC78T05 regulator can also be used as a current source when connected as above. In order to minimize dissipation the MC78T05 is chosen in this application. Resistor R determines the current as follows:

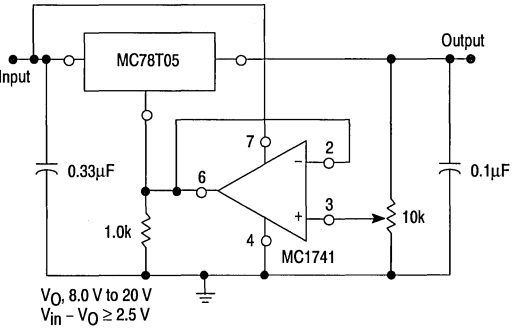
$$I_O = \frac{5.0\ V}{R} + I_B$$

$\Delta I_B \cong 0.7$ mA over line, load and Temperature changes

$I_B \cong 3.5$ mA

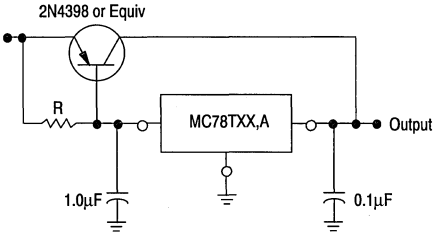
For example, a 2 A current source would require R to be a 2.5 Ω, 10 W resistor and the output voltage compliance would be the input voltage less 7.0 V.

Figure 16. Adjustable Output Regulator



The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 V greater than the regulator voltage.

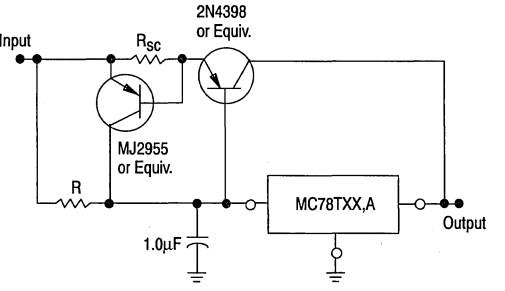
Figure 17. Current Boost Regulator



XX = 2 digits of type number indicating voltage.

The MC78T00,A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 A. Resistor R in conjuction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input-output differential voltage minimum is increased by the V_{BE} of the pass transistor.

Figure 18. Current Boost With Short Circuit Protection



XX = 2 digits of type number indicating voltage.

The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three-terminal regulator. Therefore, an eight-ampere power transistor is specified.

MC7900 Series

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

3

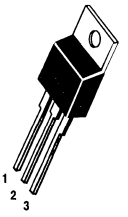
Three-Terminal Negative Voltage Regulators

The MC7900 Series of fixed output negative voltage regulators are intended as complements to the popular MC7800 Series devices. These negative regulators are available in the same seven-voltage options as the MC7800 devices. In addition, one extra voltage option commonly employed in MECL systems is also available in the negative MC7900 Series.

Available in fixed output voltage options from –5.0 V to –24 V, these regulators employ current limiting, thermal shutdown, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 A.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Available in 2% Voltage Tolerance (See Ordering Information)

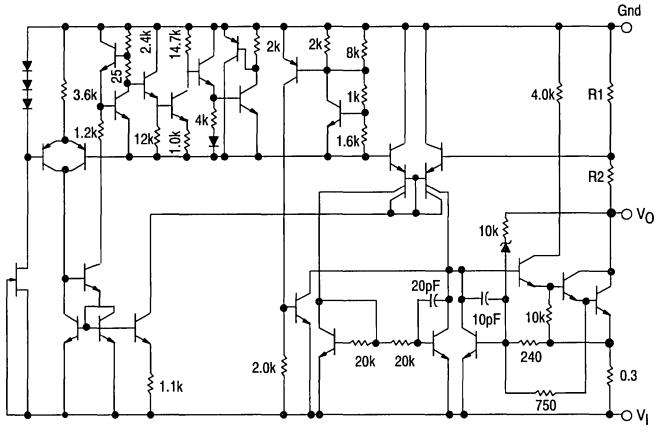
T SUFFIX
PLASTIC PACKAGE
CASE 221A



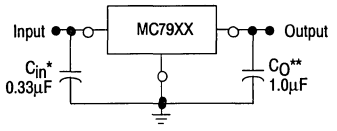
Pin 1. Ground
2. Input
3. Output

Heatsink surface connected to Pin 2

Schematic Diagram



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above more negative even during the high point of the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improve stability and transient response.

ORDERING INFORMATION

Device	Output Voltage Tolerance	Tested Operating Junction Temp. Range	Package
MC79XXCT	4%	T_J = 0° to +125°C	Plastic Power
MC79XXACT*	2%		
MC79XXBT#	4%	T_J = –40° to +125°C	

XX indicates nominal voltage

* 2% output voltage tolerance available in 5, 12 and 15 V devices.

Automotive temperature range selections are available with special test conditions and additional tests in 5, 12 and 15 V devices. Contact your local Motorola sales office for information

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE			
MC7905	5.0 V	MC7912	12 V
MC7905.2	5.2 V	MC7915	15 V
MC7906	6.0 V	MC7918	28 V
MC7908	8.0 V	MC7924	24 V

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (–5.0 V ≥ V_O ≥ –18 V) (24 V)	V_I	–35 –40	Vdc
Power Dissipation Plastic Package T_A = +25°C Derate above T_A = +25°C T_C = +25°C Derate above T_C = +95°C (See Figure 1)	 P_D $1/R_{\theta JC}$ P_D $1/R_{\theta JC}$	 Internally Limited 15.4 Internally Limited 200	 W mW/°C W mW/°C
Storage Junction Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	65	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	5.0	°C/W

MC7905C ELECTRICAL CHARACTERICISTICS (V_I = –10 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–4.8	–5.0	–5.2	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) –7.0 Vdc ≥ V_I ≥ –25 Vdc –8.0 Vdc ≥ V_I ≥ –12 Vdc (T_J = +25°C, I_O = 500 mA) –7.0 Vdc ≥ V_I ≥ –25 Vdc –8.0 Vdc ≥ V_I ≥ –12 Vdc	Reg_{line}	 — — — —	 7.0 2.0 35 8.0	 50 25 100 50	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 11 4.0	 100 50	mV
Output Voltage –7.0 Vdc ≥ V_I ≥ –20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	–4.75	—	–5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change –7.0 Vdc ≥ V_I ≥ –25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 — —	 — —	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	40	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	70	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	–1.0	—	mV/°C

NOTES: 1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7905AC ELECTRICAL CHARACTERICISTICS (V_I = –10 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–4.9	–5.0	–5.1	Vdc
Line Regulation (Note 1) –8.0 Vdc ≥ V_I ≥ –12 Vdc; I_O = 1.0 A, T_J = 25°C –8.0 Vdc ≥ V_I ≥ –12 Vdc; I_O = 1.0 A –7.5 Vdc ≥ V_I ≥ –25 Vdc; I_O = 500 mA –7.0 Vdc ≥ V_I ≥ –20 Vdc; I_O = 1.0 A, T_J = +25°C	Reg_{line}	 — — — —	 2.0 7.0 7.0 6.0	 25 50 50 50	mV
Load Regulation (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C 250 mA ≤ I_O ≤ 750 mA 5.0 mA ≤ I_O ≤ 1.0 A	Reg_{load}	 — — —	 11 4.0 9.0	 100 50 100	mV
Output Voltage –7.5 Vdc ≥ V_I ≥ –20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	–4.80	—	–5.20	Vdc
Input Bias Current	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change –7.5 Vdc ≥ V_I ≥ –25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C	ΔI_{IB}	 — — —	 — — —	 1.3 0.5 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	40	—	μV
Ripple Rejection (I_O = mA, f = 120 Hz)	RR	—	70	—	dB
Dropout Voltage I_O = 1.0 A. T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 A, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	–1.0	—	mV/°C

MC7905.2C ELECTRICAL CHARACTERICISTICS (V_I = –10 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–5.0	–5.2	–5.4	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) –7.2 Vdc ≥ V_I ≥ –25 Vdc –8.0 Vdc ≥ V_I ≥ –12 Vdc (T_J = +25°C, I_O = 500 mA) –7.2 Vdc ≥ V_I ≥ –25 Vdc –8.0 Vdc ≥ V_I ≥ –12 Vdc	Reg_{line}	 — — — —	 8.0 2.2 37 8.5	 52 27 105 52	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 12 4.5	 105 52	mV
Output Voltage –7.2 Vdc ≥ V_I ≥ –20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	–4.95	—	–5.45	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change –7.2 Vdc ≥ V_I ≥ –25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 — —	 — —	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	42	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	68	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	–1.0	—	mV/°C

MC7906C ELECTRICAL CHARACTERICISTICS (V_I = –11 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–5.75	–6.0	–6.25	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) –8.0 Vdc ≥ V_I ≥ –25 Vdc –9.0 Vdc ≥ V_I ≥ –13 Vdc (T_J = +25°C, I_O = 500 mA) –8.0 Vdc ≥ V_I ≥ –25 Vdc –9.0 Vdc ≥ V_I ≥ –13 Vdc	Reg_{line}	 — — — —	 9.0 3.0 43 10	 60 30 120 60	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 13 5.0	 120 60	mV
Output Voltage –8.0 Vdc ≥ V_I ≥ –21 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	–5.7	—	–6.3	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change –8.0 Vdc ≥ V_I ≥ –25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 — —	 — —	 1.3 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	45	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	65	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 A, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	–1.0	—	mV/°C

MC7908C ELECTRICAL CHARACTERICISTICS (V_I = –14 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–7.7	–8.0	–8.3	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) –10.5 Vdc ≥ V_I ≥ –25 Vdc –11 Vdc ≥ V_I ≥ –17 Vdc (T_J = +25°C, I_O = 500 mA) –10.5 Vdc ≥ V_I ≥ –25 Vdc –11 Vdc ≥ V_I ≥ –17 Vdc	Reg_{line}	 — — — —	 12 5.0 50 22	 80 40 160 80	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 26 9.0	 160 80	mV
Output Voltage –10.5 Vdc ≥ V_I ≥ –23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	–7.6	—	–8.4	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change –10.5 Vdc ≥ V_I ≥ –25 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 — —	 — —	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	52	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	62	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	–1.0	—	mV/°C

NOTES: 1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7915C ELECTRICAL CHARACTERICISTICS (V_I = –23 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–14.4	–15	–15.6	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) –17.5 Vdc ≥ V_I ≥ –30 Vdc –20 Vdc ≥ V_I ≥ –26 Vdc (T_J = +25°C, I_O = 500 mA) –17.5 Vdc ≥ V_I ≥ –30 Vdc –20 Vdc ≥ V_I ≥ –26 Vdc	Reg_{line}	 — — — —	 14 6.0 57 27	 150 75 300 150	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 68 25	 300 150	mV
Output Voltage –17.5 Vdc ≥ V_I ≥ –30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	–14.25	—	–15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change –17.5 Vdc ≥ V_I ≥ –30 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 — —	 — —	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	90	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	60	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 A, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	–1.0	—	mV/°C

MC7905AC ELECTRICAL CHARACTERICISTICS (V_I = –23 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–14.7	–15	–15.3	Vdc
Line Regulation (Note 1) –20 Vdc ≥ V_I ≥ –26 Vdc, I_O = 1.0 A, T_J = 25°C –20 Vdc ≥ V_I ≥ –26 Vdc, I_O = 1.0 A, –17.9 Vdc ≥ V_I ≥ –30 Vdc, I_O = 500 mA –17.5 Vdc ≥ V_I ≥ –30 Vdc, I_O = 1.0 A, T_J = 25°C	Reg_{line}	 — — — —	 27 57 57 57	 75 150 150 150	mV
Load Regulation (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 250 mA ≤ I_O ≤ 750 mA 5.0 mA ≤ I_O ≤ 1.0 A	Reg_{load}	 — — —	 68 25 40	 150 75 150	mV
Output Voltage –17.9 Vdc ≥ V_I ≥ –30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	–14.4	—	–15.6	Vdc
Input Bias Current	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change –17.5 Vdc ≥ V_I ≥ –30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C	ΔI_{IB}	 — — —	 — — —	 0.8 0.5 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	90	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	60	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	–1.0	—	mV/°C

MC7912C ELECTRICAL CHARACTERICISTICS (V_I = –19 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–11.5	–12	–12.5	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) –14.5 Vdc ≥ V_I ≥ –30 Vdc –16 Vdc ≥ V_I ≥ –22 Vdc (T_J = +25°C, I_O = 500 mA) –14.5 Vdc ≥ V_I ≥ –30 Vdc –16 Vdc ≥ V_I ≥ –22 Vdc	Reg_{line}	 — — — —	 13 6.0 55 24	 120 60 240 120	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 46 17	 240 120	mV
Output Voltage –14.5 Vdc ≥ V_I ≥ –27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	–11.4	—	–12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change –14.5 Vdc ≥ V_I ≥ –30 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 — —	 — —	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	75	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	61	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	–1.0	—	mV/°C

MC7912AC ELECTRICAL CHARACTERICISTICS (V_I = –19 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–11.75	–12	–12.25	Vdc
Line Regulation (Note 1) –16 Vdc ≥ V_I ≥ –22 Vdc; I_O = 1.0 A, T_J = 25°C –16 Vdc ≥ V_I ≥ –22 Vdc; I_O = 1.0 A –14.8 Vdc ≥ V_I ≥ –30 Vdc; I_O = 500 mA –14.5 Vdc ≥ V_I ≥ –27 Vdc; I_O = 1.0 A, T_J = 25°C	Reg_{line}	 — — — —	 6.0 24 24 13	 60 120 120 120	mV
Load Regulation (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 250 mA ≤ I_O ≤ 750 mA 5.0 mA ≤ I_O ≤ 1.0 A	Reg_{load}	 — — —	 46 17 35	 150 75 150	mV
Output Voltage –14.8 Vdc ≥ V_I ≥ –27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	–11.5	—	–12.5	Vdc
Input Bias Current	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change –15 Vdc ≥ V_I ≥ –30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C	ΔI_{IB}	 — — —	 — — —	 0.8 0.5 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	75	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	61	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 A, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	–1.0	—	mV/°C

NOTES: 1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7918C ELECTRICAL CHARACTERICISTICS (V_I = –27 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–17.3	–18	–18.7	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) –21 Vdc ≥ V_I ≥ –33 Vdc –24 Vdc ≥ V_I ≥ –30 Vdc (T_J = +25°C, I_O = 500 mA) –21 Vdc ≥ V_I ≥ –33 Vdc –24 Vdc ≥ V_I ≥ –30 Vdc	Reg_{line}	 — — — —	 25 10 90 50	 180 90 360 180	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 110 55	 360 180	mV
Output Voltage –21 Vdc ≥ V_I ≥ –33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	–17.1	—	–18.9	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.5	8.0	mA
Input Bias Current Change –21 Vdc ≥ V_I ≥ –33 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 — —	 — —	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	110	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	59	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	–1.0	—	mV/°C

MC7924C ELECTRICAL CHARACTERICISTICS (V_I = –33 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–23	–24	–25	Vdc
Line Regulation (Note 1) (T_J = +25°C, I_O = 100 mA) –27 Vdc ≥ V_I ≥ –38 Vdc –30 Vdc ≥ V_I ≥ –36 Vdc (T_J = +25°C, I_O = 500 mA) –27 Vdc ≥ V_I ≥ –38 Vdc –30 Vdc ≥ V_I ≥ –36 Vdc	Reg_{line}	 — — — —	 31 14 118 70	 240 120 470 240	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 150 85	 480 240	mV
Output Voltage –27 Vdc ≥ V_I ≥ –38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	–22.8	—	–25.2	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.6	8.0	mA
Input Bias Current Change –27 Vdc ≥ V_I ≥ –38 Vdc 5.0 mA ≤ I_O ≤ 1.5 A	ΔI_{IB}	 — —	 — —	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	e_{on}	—	170	—	μV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	—	56	—	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I-V_O	—	2.0	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	–1.0	—	mV/°C

Figure 1. Worst Case Power Dissipation as a Function of Ambient Temperature

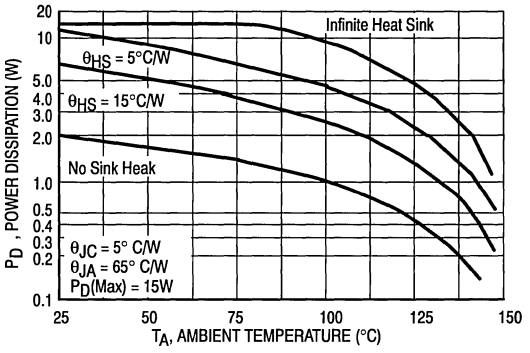


Figure 2. Peak Output Current as a Function of Input-Output Differential Voltage

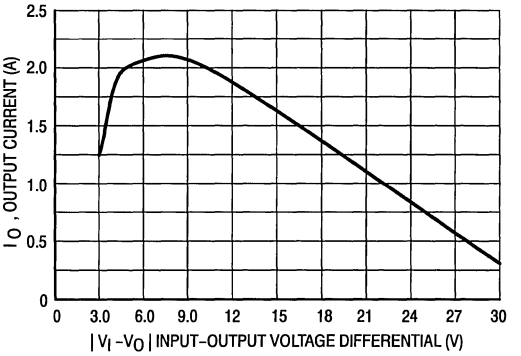


Figure 3. Ripple Rejection as a Function of Frequency

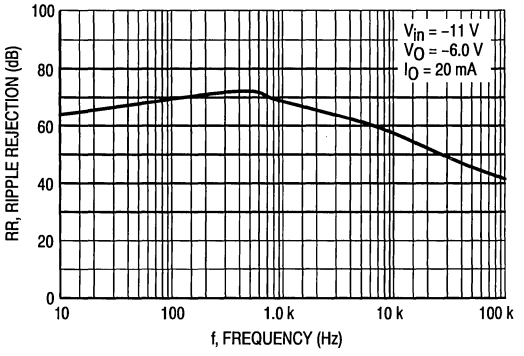


Figure 4. Ripple Rejection as a Function of Output Voltages

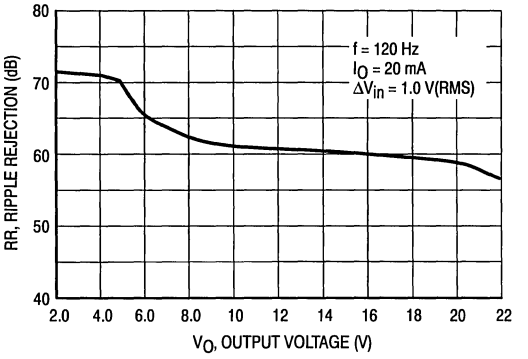


Figure 5. Output Voltage as a Function of Junction Temperature

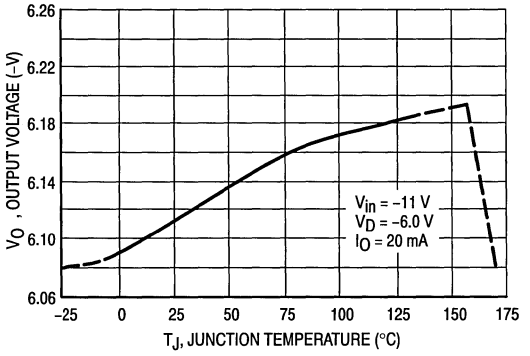
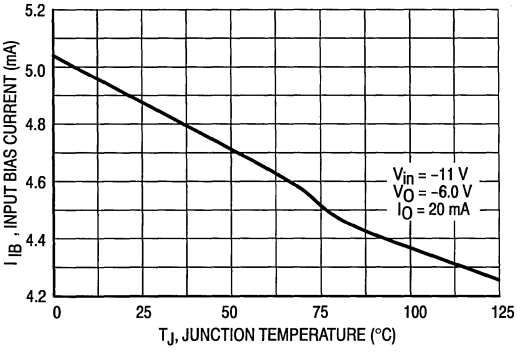


Figure 6. Quiescent Current as a Function of Temperature



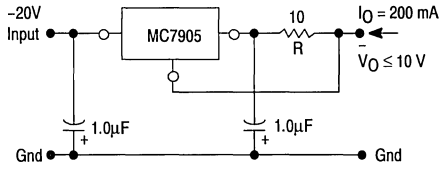
APPLICATIONS INFORMATION

Design Considerations

The MC7900 Series of fixed voltage regulators are designed with Thermal overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

Figure 7. Current Regulator

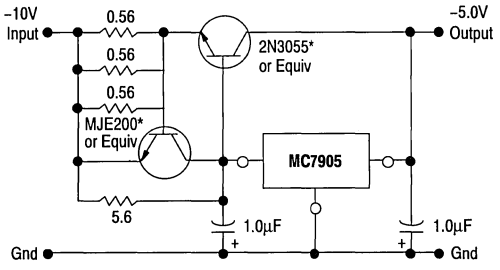


The MC7905, –5.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows.

$$I_O = \frac{5.0\ V}{R} + I_B$$

The quiescent current for this regulator is typically 4.3 mA. The 5.0 V regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

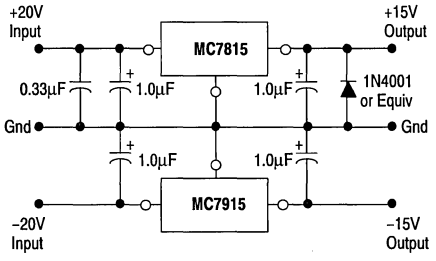
Figure 8. Current Boost Regulator
(–5.0V @ 4.0A, with 5.0A Current Limiting)



*Mounted on common heatsink, Motorola MS-10 or equivalent.

When a boost transistor is used, short circuit currents are equal to the sum of the series pass and regulator limits, which are measured at 3.2 A and 1.8 A respectively in this case. Series pass limiting is approximately equal to 0.6 V/R_{SC}. Operation beyond this point to the peak current capability of the MC7905C is possible if the regulator is mounted on a heat sink; otherwise thermal shutdown will occur when the additional load current is picked up by the regulator.

Figure 9. Operational Amplifier Supply
(±15 @ 1.0 A)



The MC7815 and MC7915 positive and negative regulators may be connected as shown to obtain a dual power supply for operational amplifiers. A clamp diode should be used at the output of the MC7815 to prevent potential latch-up problems whenever the output of the positive regulator (MC7815) is drawn below ground with an output current greater than 200 mA.

DEFINITIONS

Line Regulation — The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation — The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation — The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current — That part of the input current that is not delivered to the load.

Output Noise Voltage — The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability — Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

MC79L00,A Series

3

Three-Terminal Low Current Negative Voltage Regulators

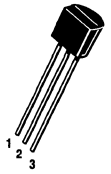
THREE-TERMINAL LOW CURRENT NEGATIVE FIXED VOLTAGE REGULATORS

The MC79L00 Series negative voltage regulators are inexpensive, easy-to-use devices suitable for numerous applications requiring up to100 mA. Like the higher powered MC7900 Series negative regulators, this series features thermal shutdown and current limiting, making them remarkably rugged. In most applications, no external components are required for operation.

The MC79L00 devices are useful for on-card regulation or any other application where a regulated negative voltage at a modest current level is needed. These regulators offer substantial advantage over the common resistor/zener diode approach.

- No External Components Required
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- Low Cost
- Complementary Positive Regulators Offered (MC78L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

P SUFFIX
PLASTIC PACKAGE
CASE 29



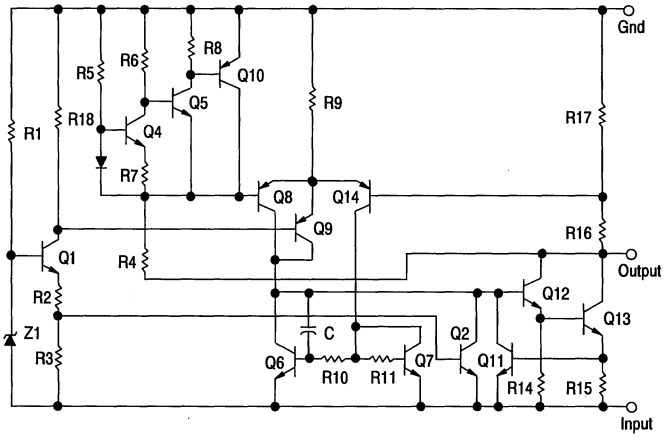
Pin 1. Ground
2. Input
3. Output

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP-8)

PIN 1. V_{out}
2. V_{in}
3. V_{in}
4. NC
5. GND
6. V_{in}
7. V_{in}
8. NC

SOP-8 is an internally modified SO-8 Package Pins 2, 3, 6, and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

Representative Circuit Schematic



Device No. ±10%	Device No. 5%	Nominal Voltage
MC79L05C	MC79L05AC	–5.0
MC79L12C	MC79L12AC	–12
MC79L15C	MC79L15AC	–15
MC79L18C	MC79L18AC	–18
MC79L24C	MC79L24AC	–24

ORDERING INFORMATION

Device	Testing Operating Temperature Range	Package
MC79LXXACD*	T_J = 0° to +125°C	SOP-8
MC79LXXACP		Plastic Power
MC79LXXCP		Plastic Power
MC79LXXABD*		SOP-8
MC79LXXABP*	T_J = –40° to +125°C	Plastic Power

XX indicates nominal voltage
*Available in 5, 12 and 15 V devices

Automotive temperature range selections are available with special test conditions and additional tests in 5, 12 and 15 V devices. Contact your local Motorola sales office for information.

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (–5 V) (–12, –15, –18 V) (–24 V)	V_I	–30 –35 –40	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	+150	°C

MC79L05C, AC SERIES ELECTRICAL CHARACTERICISTICS (V_I = –10 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted).

Characteristics	Symbol	MC79L05C			MC79L05AC, AB			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	–4.6	–5.0	–5.4	–4.8	–5.0	–5.2	Vdc
Input Regulation (T_J = +25°C) –7.0 Vdc ≥ V_I ≥ –20 Vdc –8.0 Vdc ≥ V_I ≥ –20 Vdc	Reg_{line}	 — —	 — —	 200 150	 — —	 — —	 150 100	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 — —	 — —	 60 30	 — —	 — —	 60 30	mV
Output Voltage –7.0 Vdc ≥ V_I ≥ –20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = –10 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 –4.5 –4.5	 — —	 –5.5 –5.5	 –4.75 –4.75	 — —	 –5.25 –5.25	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 — —	 6.0 5.5	 — —	 — —	 6.0 5.5	mA
Input Bias Current Change –8.0 Vdc ≥ V_I ≥ –20 Vdc 1.0 mA ≤ I_O ≤ 40 mA	I_{IB}	 — —	 — —	 1.5 0.2	 — —	 — —	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	40	—	—	40	—	µV
Ripple Rejection (–8.0 ≥ V_I ≥ –18 Vdc, f = 120 Hz, T_J = +25°C)	RR	40	49	—	41	49	—	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\|V_I-V_O\|$	—	1.7	—	—	1.7	—	Vdc

MC79L12C, AC ELECTRICAL CHARACTERICISTICS (V_I = –19 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted).

Characteristics	Symbol	MC79L12C			MC79L12AC, AB			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	–11.1	–12	–12.9	–11.5	–12	–12.5	Vdc
Input Regulation (T_J = +25°C) –14.5 Vdc ≥ V_I ≥ –27 Vdc –16 Vdc ≥ V_I ≥ –27 Vdc	Reg_{line}	 — —	 — —	 250 200	 — —	 — —	 250 200	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 — —	 — —	 100 50	 — —	 — —	 100 50	mV
Output Voltage –14.5 Vdc ≥ V_I ≥ –27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = –19 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 –10.8 –10.8	 — —	 –13.2 –13.2	 –11.4 –11.4	 — —	 –12.6 –12.6	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 — —	 6.5 6.0	 — —	 — —	 6.5 6.0	mA
Input Bias Current Change –16 Vdc ≥ V_I ≥ –27 Vdc 1.0 mA ≤ I_O ≤ 40 mA	I_{IB}	 — —	 — —	 1.5 0.2	 — —	 — —	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	80	—	—	80	—	µV
Ripple Rejection (–15 ≤ V_I ≤ –25 Vdc, f = 120 Hz, T_J = +25°C)	RR	36	42	—	37	42	—	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\|V_I-V_O\|$	—	1.7	—	—	1.7	—	Vdc

MC79L15C, AC ELECTRICAL CHARACTERICISTICS (V_I = –23 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted).

Characteristics	Symbol	MC79L15C			MC79L15AC, AB			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	–13.8	–15	–16.2	–14.4	–15	–15.6	Vdc
Input Regulation (T_J = +25°C) –17.5 Vdc ≥ V_I ≥ –30 Vdc –20 Vdc ≥ V_I ≥ –30 Vdc	Reg_{line}	 — —	 — —	 300 250	 — —	 — —	 300 250	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 — —	 — —	 150 75	 — —	 — —	 150 75	mV
Output Voltage –17.5 Vdc ≥ V_I ≥ –Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = –23 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 –13.5 –13.5	 — —	 –16.5 –16.5	 –14.25 –14.25	 — —	 –15.75 –15.75	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 — —	 6.5 6.0	 — —	 — —	 6.5 6.0	mA
Input Bias Current Change –20 Vdc ≥ V_I ≥ –30 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	 — —	 — —	 1.5 0.2	 — —	 — —	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	—	90	—	—	90	—	µV
Ripple Rejection (–18.5 ≤ V_I ≤ –28.5 Vdc, f = 120 Hz)	RR	33	39	—	34	39	—	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\lvert V_I\text{-}V_O \rvert$	—	1.7	—	—	1.7	—	Vdc

MC79L18C, AC ELECTRICAL CHARACTERICISTICS (V_I = –27 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted).

Characteristics	Symbol	MC79L18C			MC79L18AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	–16.6	–18	–19.4	–17.3	–18	–18.7	Vdc
Input Regulation (T_J = +25°C) –20.7 Vdc ≥ V_I ≥ –33 Vdc –21.4 Vdc ≥ V_I ≥ –33 Vdc –22 Vdc ≥ V_I ≥ –33 Vdc –21 Vdc ≥ V_I ≥ –33 Vdc	Reg_{line}	 — — — —	 — — — —	 — 325 275 —	 — — — —	 — — — —	 325 — — 275	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 — —	 — —	 170 85	 — —	 — —	 170 85	mV
Output Voltage –20.7 Vdc ≥ V_I ≥ –33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA –21.4 Vdc ≥ V_I ≥ –33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = –27 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 — –16.2 –16.2	 — — —	 — –19.8 –19.8	 –17.1 — –17.1	 — — —	 –18.9 — –18.9	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 — —	 6.5 6.0	 — —	 — —	 6.5 6.0	mA
Input Bias Current Change –21 Vdc ≥ V_I ≥ –33 Vdc –27 Vdc ≥ V_I ≥ –33 Vdc 1.0 mA ≤ I_O ≤ 40 mA	I_{IB}	 — — —	 — — —	 — 1.5 0.2	 — — —	 — — —	 1.5 — 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	150	—	—	150	—	µV
Ripple Rejection (–23 ≤ V_I ≤ –33 Vdc, f = 120 Hz, T_J = +25°C)	RR	32	46	—	33	48	—	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\lvert V_I\text{-}V_O \rvert$	—	1.7	—	—	1.7	—	Vdc

MC79L24C, AC ELECTRICAL CHARACTERICISTICS (V_I = –33 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted).

Characteristics	Symbol	MC79L24C			MC79L24AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	–22.1	–24	–25.9	–23	–24	–25	Vdc
Input Regulation (T_J = +25°C) –27 Vdc ≥ V_I ≥ –38 Vdc –27.5 Vdc ≥ V_I ≥ –38 Vdc –28 Vdc ≥ V_I ≥ –38 Vdc	Reg_{line}	 — — —	 — — —	 — 350 300	 — — —	 — — —	 350 — 300	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 — —	 — —	 200 100	 — —	 — —	 200 100	mV
Output Voltage –27 Vdc ≥ V_I ≥ –38 V, 1.0 mA ≤ I_O ≤ 40 mA –28 Vdc ≥ V_I ≥ –38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = –33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 — –21.4 –21.4	 — — —	 — –26.4 –26.4	 –22.8 — –22.8	 — — —	 –25.2 — –25.2	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 — —	 — —	 6.5 6.0	 — —	 — —	 6.5 6.0	mA
Input Bias Current Change –28 Vdc ≥ V_I ≥ –38 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	 — —	 — —	 1.5 0.2	 — —	 — —	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	200	—	—	200	—	µV
Ripple Rejection (–29 ≤ V_I ≤ –35 Vdc, f = 120 Hz, T_J = +25°C)	RR	30	43	—	31	47	—	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\|V_I-V_O\|$	—	1.7	—	—	1.7	—	Vdc

APPLICATIONS INFORMATION

Design Considerations

The MC79L00 Series of fixed voltage regulators are designed with Thermal Overload Protections that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire length, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

Figure 1. Positive and Negative Regulator

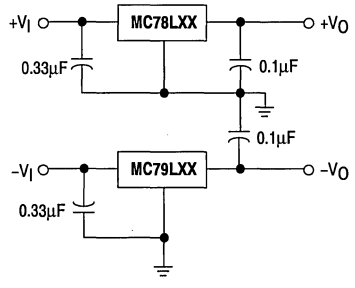
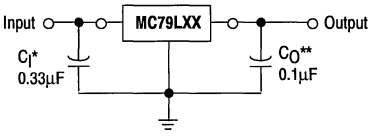


Figure 2. Standard Application



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the ripple voltage.

* = C_I is required if regulator is located an appreciable distance from the power supply filter

** = C_O improves stability and transient response.

3

TYPICAL CHARACTERISTICS

(T_A = +25°C, unless otherwise noted.)

Figure 3. Dropout Characteristics

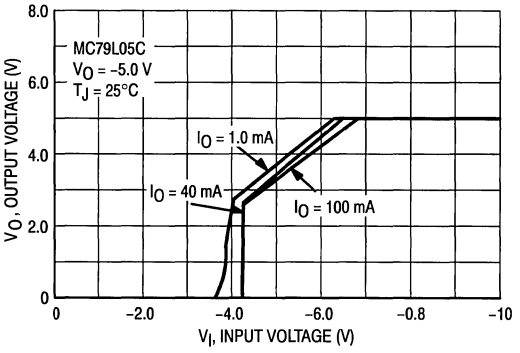


Figure 4. Dropout Voltage versus Junction Temperature

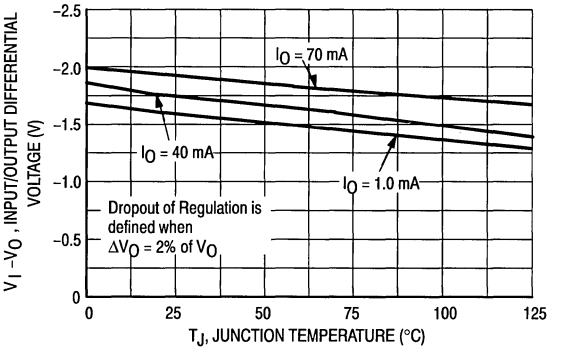


Figure 5. Input Bias Current versus Ambient Temperature

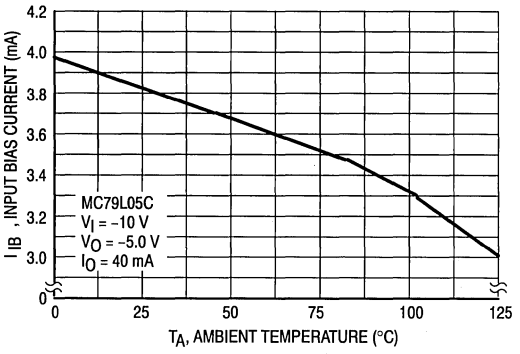


Figure 6. Input Bias Current versus Input Voltage

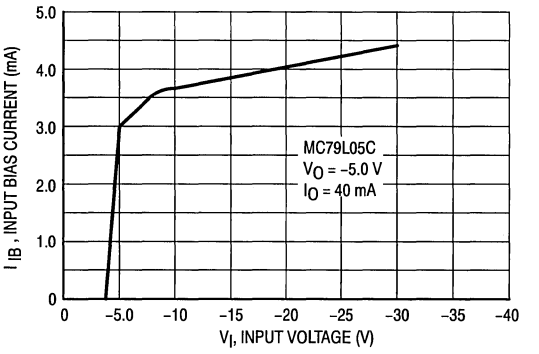
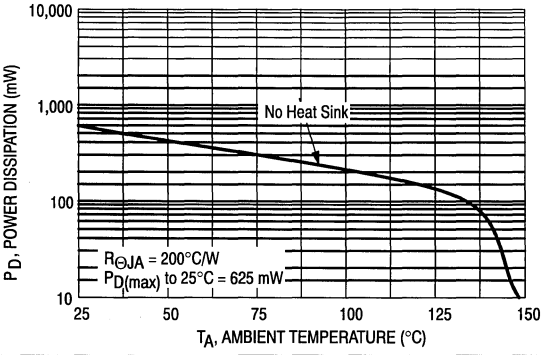


Figure 7. Maximum Average Power Dissipation versus Ambient Temperature — TO-92 Type Package



MC79M00 Series

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

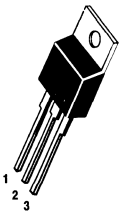
Three-Terminal Negative Voltage Regulators

The MC79M00 Series of fixed output negative voltage regulators are intended as complements to the popular MC78M00 Series devices.

Available in fixed output voltage options of –5.0, –12 and –15 V, these regulators employ current limiting, thermal shutdown, and safe-area compensation — making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 0.5 A.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation

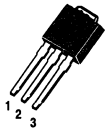
T SUFFIX
PLASTIC PACKAGE
CASE 221A



Pin 1. Ground
2. Input
3. Output

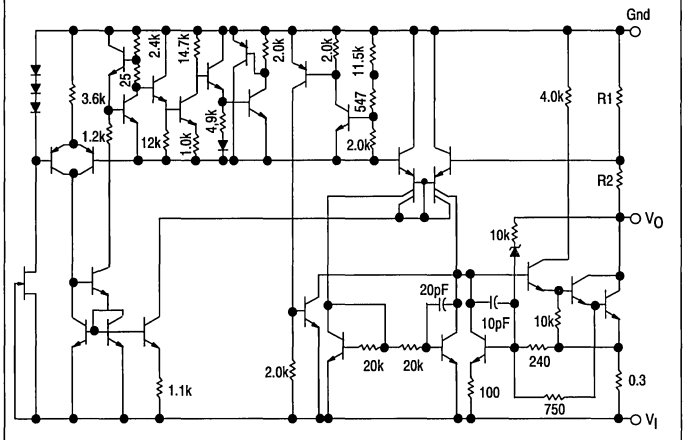
Heatsink surface connected to Pin 2

DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)

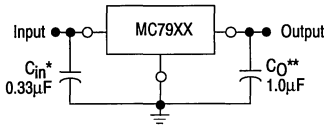


DT-1 SUFFIX
PLASTIC PACKAGE
CASE 369
(DPAK)

Equivalent Schematic Diagram



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 1.1 V more negative even during the high point of the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improve stability and transient response.

ORDERING INFORMATION

Device	Output Voltage	Testing Operating Junction Temp. Range	Package
MC79M05CDT, CDT-1	–5.0 V	0° to +125°C	DPAK
MC79M05CT			Plastic Power
MC79M12CDT, CDT-1	–12 V		DPAK
MC79M12CT			Plastic Power
MC79M15CDT, CDT-1	–15 V		DPAK
MC79M15CT			Plastic Power

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_I	–35	Vdc
Power Dissipation Plastic Package, T-Suffix T_A = +25°C Derate above T_C = +25°C T_C = +25°C Derate above T_C = +95°C	 P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JC}$	 Internally Limited 14.2 Internally Limited 200	 W mW/°C W mW/°C
Storage Junction Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	+150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	65	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	5.0	°C/W

MC79M05C ELECTRICAL CHARACTERICISTICS (V_I = –10 V, I_O = 350 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–4.8	–5.0	–5.2	Vdc
Line Regulation (T_J = +25°C) (Note 1) –7.0 Vdc ≥ V_I ≥ –25 Vdc –8.0 Vdc ≥ V_I ≥ –18 Vdc	Reg_{line}	 — —	 7.0 2.0	 50 30	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	—	30	100	mV
Output Voltage –7.0 Vdc ≥ V_I ≥ –25 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	–4.75	—	–5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.3	8.0	mA
Input Bias Current Change –8.0 Vdc ≥ V_I ≥ –25 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = –10 V	ΔI_{IB}	 — —	 — —	 0.4 0.4	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	40	—	μV
Ripple Rejection (f = 120 Hz)	RR	54	66	—	dB
Dropout Voltage I_O = 500 mA, T_J = +25°C	V_I-V_O	—	1.1	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	0.2	—	mV/°C

NOTES: 1. Load and line regulation are specified at constant temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC79M12C ELECTRICAL CHARACTERICISTICS (V_I = –19 V, I_O = 350 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–11.5	–12	–12.5	Vdc
Line Regulation (T_J = +25°C) (Note 1) –14.5 Vdc ≥ V_I ≥ –30 Vdc –15 Vdc ≥ V_I ≥ –25 Vdc	Reg_{line}	 — —	 5.0 3.0	 80 50	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	—	30	240	mV
Output Voltage –14.5 Vdc ≥ V_I ≥ –30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	–11.4	—	–12.6	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change –14.5 Vdc ≥ V_I ≥ –30 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = –19 V	ΔI_{IB}	 — —	 — —	 0.4 0.4	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	75	—	μV
Ripple Rejection (f = 120 Hz)	RR	54	60	—	dB
Dropout Voltage I_O = 500 mA, T_J = +25°C	V_I-V_O	—	1.1	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	–0.8	—	mV/°C

MC79M15C ELECTRICAL CHARACTERICISTICS (V_I = –23 V, I_O = 350 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–14.4	–15	–15.6	Vdc
Line Regulation (T_J = +25°C) (Note 1) –17.5 Vdc ≥ V_I ≥ –30 Vdc –18 Vdc ≥ V_I ≥ –28 Vdc	Reg_{line}	 — —	 5.0 3.0	 80 50	mV
Load Regulation (T_J = +25°C) (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	—	30	240	mV
Output Voltage –17.5 Vdc ≥ V_I ≥ –30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	–14.25	—	–15.75	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	—	4.4	8.0	mA
Input Bias Current Change –17.5 Vdc ≥ V_I ≥ –30 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = –23 V	ΔI_{IB}	 — —	 — —	 0.4 0.4	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	—	90	—	μV
Ripple Rejection (f = 120 Hz)	RR	54	60	—	dB
Dropout Voltage I_O = 500 mA, T_J = +25°C	V_I-V_O	—	1.1	—	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	—	–1.0	—	mV/°C

NOTES: 1. Load and line regulation are specified at constant temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC33267

3

Advance Information

Low Dropout Regulator

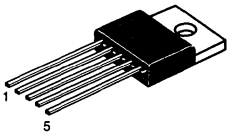
LOW DROPOUT REGULATOR with POWER-UP RESET

SILICON MONOLITHIC INTEGRATED CIRCUIT

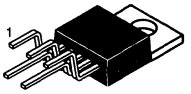
The MC33267 is a positive fixed 5.0 V regulator that is specifically designed to maintain proper voltage regulation with an extremely low input-to-output voltage differential. This device is capable of supplying output currents in excess of 500 mA and contains internal current limiting and thermal shutdown protection. Also featured is an on-chip power-up reset circuit that is ideally suited for use in microprocessor based systems. Whenever the regulator output voltage is below nominal, the reset output is held low. A programmable time delay is initiated after the regulator has reached its nominal level and upon timeout, the reset output is released.

Due to the low dropout voltage specifications, the MC33267 is ideally suited for use in battery powered industrial and consumer equipment where an extension of useful battery life is desirable. This device is contained in an economical five lead TO-220 type package.

- Low Input-to-Output Voltage Differential
- Output Current in Excess of 500 mA
- On-Chip Power-Up-Reset Circuit with Programmable Delay
- Internal Current Limiting with Thermal Shutdown
- Economical Five Lead TO-220 Type Package

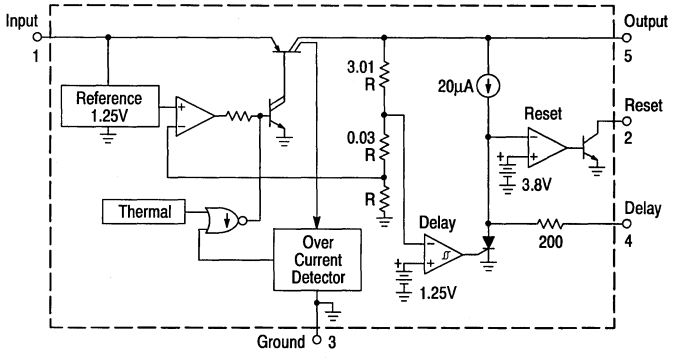


T SUFFIX
PLASTIC PACKAGE
CASE 314D

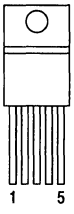


TV SUFFIX
PLASTIC PACKAGE
CASE 314B
(LEAD FORMED)

Simplified Block Diagram



PIN CONNECTIONS



Pin 1. V_{CC} Input
2. Reset
3. Ground
4. Delay
5. Output

(Heatsink surface connected to Pin 3)

ORDERING INFORMATION

Device	Temperature Range	Package
MC33267T	– 40° to +105°C	Plastic Pov
MC33267TV		Plastic Po

MAXIMUM RATINGS

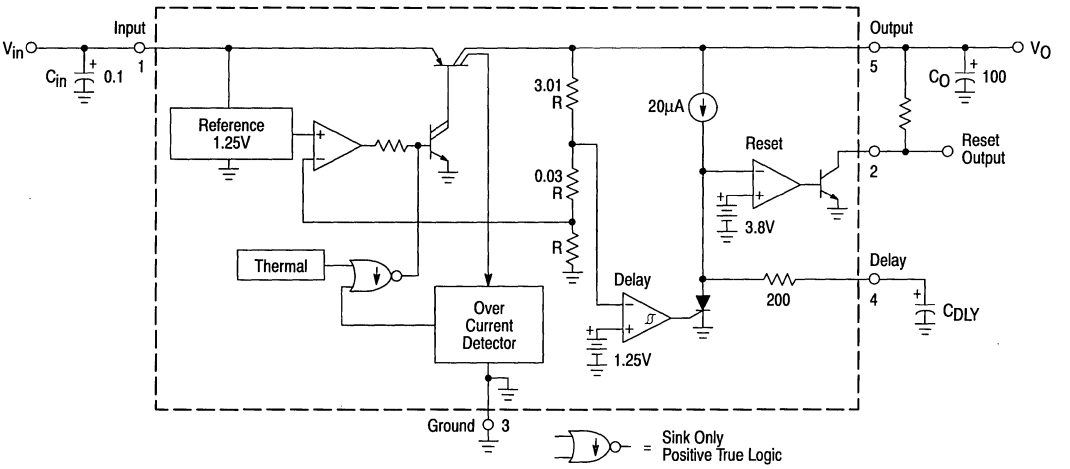
Rating	Symbol	Value	Unit
Input Voltage Range	V_{in}	– 20 to + 40	Vdc
Delay Voltage Range	V_{DLYR}	– 0.3 to V_O	V
Delay Sink Current	$I_{DLY(sink)}$	25	mA
Reset Voltage Range	V_{RR}	– 0.3 to +15	V
Reset Sink Current	$I_{R(sink)}$	50	mA
Power Dissipation and Thermal Characteristics T/TV Suffix, Plastic Package, Case 314 T_A = 25°C Thermal Resistance Junction-to-Ambient T/TV Suffix, Plastic Package, Case 314 T_C = 90°C Thermal Resistance Junction-to-Case	 P_D θ_{JA} P_D θ_{JC}	 2.0 62.5 15 4.0	 W °C/W W °C/W
Operating Junction Temperature Range	T_J	– 40 to +150	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{in} = 14.4 V, I_O = 5.0 mA, C_O = 100 µF, $C_{O(ESR)} \leq 0.3\ \Omega$, T_J = 25°C, Note 1, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 5.0 mA to 500 mA, V_{in} = 6.0 V to 28 V) T_J = 25°C T_J = – 40° to +125°C	V_O	 4.95 4.9	 5.05 —	 5.15 5.2	V
Line Regulation (V_{in} = 6.0 V to 26 V)	Reg_{line}	—	3.0	50	mV
Load Regulation (I_O = 5.0 mA to 500 mA)	Reg_{load}	—	1.0	50	mV
Bias Current I_O = 0 mA I_O = 150 mA I_O = 500 mA I_O = 500 mA, V_{in} = 6.2 V	I_B	 — — — —	 12 22 100 120	 20 40 200 300	mA
Ripple Rejection (f = 120 Hz, V_{in} = 7.0 V to 17 V, I_O = 350 mA, C_O = 100 µF)	RR	 60	 80	 —	dB
Dropout Voltage (I_O = 500 mA)	$V_{in} - V_O$	—	0.58	0.8	V
Delay Comparator Threshold (V_O Decreasing)	$V_{th(DLY)}$	4.8	V_O – 0.15	V_O – 0.08	V
Delay Pin Source Current	$I_{DLY(source)}$	12	20	28	µA
Reset Comparator Threshold	$V_{th(R)}$	3.6	3.8	4.0	V
Reset Sink Saturation (I_{sink} = 10 mA)	$V_{CE(sat)}$	—	0.2	0.8	V
Reset Off-State Leakage (V_{CE} = 5.0 V)	$I_{R(leak)}$	—	0.3	10	µA

NOTE: 1. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Figure 1. Typical Application Circuit



APPLICATION CIRCUIT INFORMATION

The MC33267 is a low dropout, positive fixed 5.0 V, 500 mA regulator. Protection features include output current limiting and thermal shutdown. System protection consists of an on-chip power-up microprocessor reset circuit.

A typical applications circuit is shown in Figure 1. The input bypass capacitor (C_{in}) is recommended if the regulator is located an appreciable distance (≥ 4″) from the supply input filter. This will reduce the circuit's sensitivity to the input line impedance at high frequencies.

These regulators are not internally compensated and thus require an external output capacitor (C_O) for stability. The recommended capacitance is 100 μF with an equivalent series resistance (ESR) of less than 0.3 Ω. A minimum capacitance of 33 μF with a maximum ESR of 3.0 Ω can be used in applications where space is a premium, however, these limits must be observed over the entire operating temperature range of the regulator circuit.

With economical electrolytic capacitors, cold temperature operation can pose a serious stability problem. As the electrolyte freezes, around – 30°C, the capacitance will decrease and the ESR will increase drastically, causing the circuit to oscillate. Quality electrolytic capacitors with extended temperature ranges of – 40°C to + 85°C and – 55°C to +105°C are readily available. It is suggested that oven testing of the entire circuit be performed with maximum load, minimum input voltage, and minimum ambient temperature.

Figure 2 shows the reset circuit timing relationship. Note that whenever the regulator's output is less than 4.9 V, the delay capacitor (C_{DLY}) is immediately discharged, and the reset output is held in a low state. As the regulator's output voltage increases beyond 4.97 V, the delay comparator will allow the 20 μA current source to charge C_{DLY}. The reset output will go to a high state when C_{DLY} crosses the 3.8 V threshold of the reset comparator. The reset delay time is controlled by the value selected for C_{DLY}. The required system reset time is governed by the microprocessor and usually a reset signal which lasts several machine cycles is sufficient.

Figure 2. Timing Waveforms

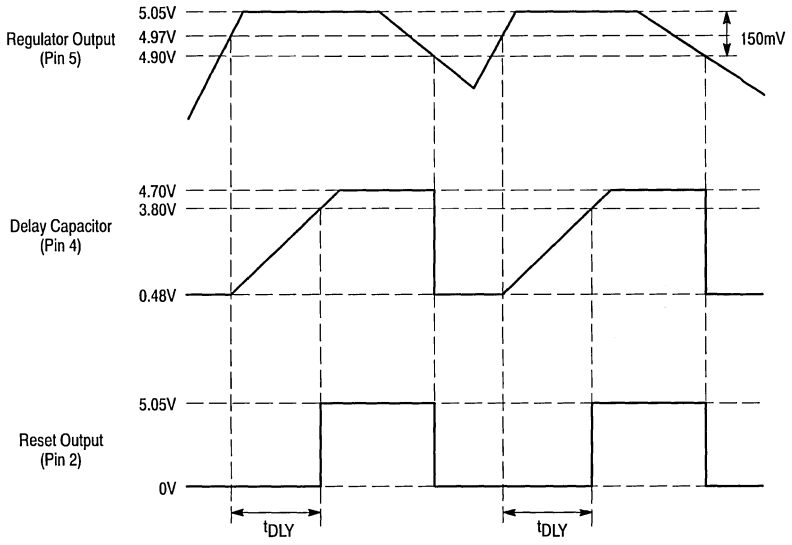


Figure 3. Reset Output versus Input Voltage

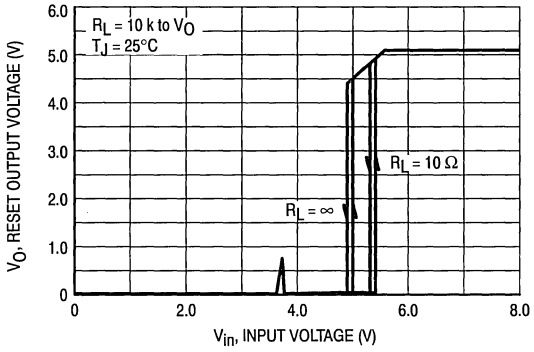


Figure 4. Output Voltage versus Input Voltage

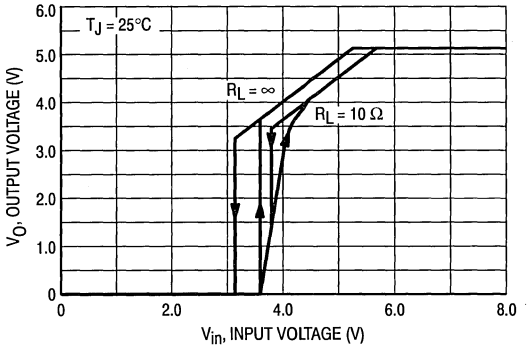


Figure 5. Dropout Voltage versus Output Current

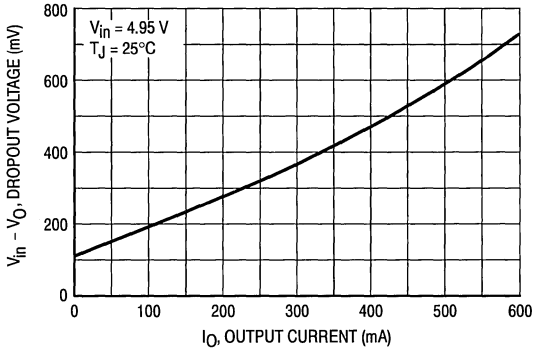
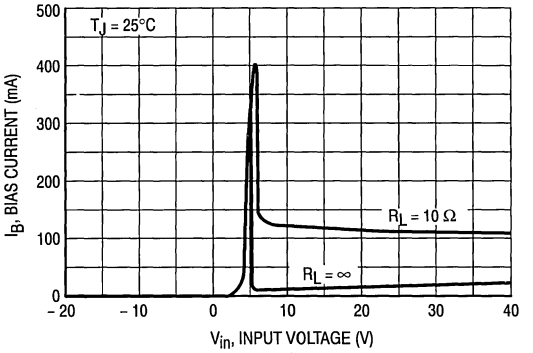


Figure 6. Bias Current versus Input Voltage



MC33269

3

Advance Information

Low Dropout Positive Voltage Regulator Series

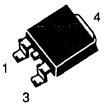
**800 mA
LOW DROPOUT
THREE-TERMINAL
VOLTAGE REGULATOR**

The MC33269 series are low dropout, medium current, positive voltage regulators specifically designed for use in low input voltage applications. These devices offer the circuit designer an economical solution for precision voltage regulation, while keeping power losses to a minimum.

The regulator consists of a 1.0 V dropout composite PNP-NPN pass transistor, current limiting, and thermal shutdown.

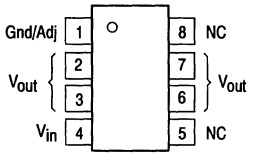
- 3.3 V, 5.0 V, 12 V, and Adjustable Versions
- Space Saving DPAK and SOP-8 Power Package
- 1.0 V Dropout
- Output Current in Excess of 800 mA
- Thermal Protection
- Short Circuit Protection
- Output Trimmed to 1.0% Tolerance
- No Minimum Load Required with the Fixed Voltage Output Devices

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP-8)

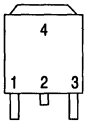


DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)

PIN CONNECTIONS



(Top View)

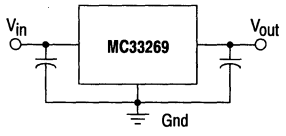


1. Gnd/Adj
2. V_{out}
3. V_{in}
4. V_{out}

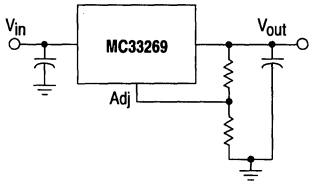
(Top View)

Simplified Block Diagrams

Fixed Output Version



Adjustable Version



ORDERING INFORMATION

Device	Ambient Temperature Range	Package
MC33269DT-3.3	– 40° to +125°C	DPAK
MC33269D-3.3		SOP-8
MC33269DT-5.0		DPAK
MC33269D-5.0		SOP-8
MC33269DT-12		DPAK
MC33269D-12		SOP-8
MC33269DT-ADJ		DPAK
MC33269D-ADJ		SOP-8

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{in}	20	V
Power Dissipation and Thermal Characteristics DT Suffix, Plastic Package, Case 369-A T_A = 25°C, Derate Above T_A = 25°C Thermal Resistance, Junction-to-Air D Suffix, Plastic Package, Case 751 T_A = 25°C, Derate Above T_A = 25°C Thermal Resistance, Junction-to-Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 Internally Limited See Figure 2 Internally Limited See Figure 1	 mW °C/W mW °C/W
Operating Junction Temperature Range	T_J	– 40 to +150	°C
Storage Temperature	T_{stg}	– 55 to +150	°C

ELECTRICAL CHARACTERISTICS (C_O = 10 µF, T_A = 25°C, for min/max values T_J = – 40°C to +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_{out} = 10 mA, T_J = 25°C) – 3.3 Suffix (V_{CC} = 5.3 V) – 5.0 Suffix (V_{CC} = 7.0 V) – 12 Suffix (V_{CC} = 14 V) Output Voltage (Line, Load, and Temperature) – 3.3 Suffix (V_{CC} = 4.6 to 20 V, I_{out} = 10 to 800 mA) – 5.0 Suffix (V_{CC} = 6.35 to 20 V, I_{out} = 10 to 800 mA) – 12 Suffix (V_{CC} = 13.5 to 20 V, I_{out} = 10 to 800 mA)	V_{out}	 3.27 4.95 11.88 3.23 4.9 11.76	 3.3 5.0 12 3.3 5.0 12	 3.33 5.05 12.12 3.37 5.1 12.24	V
Reference Voltage (I_{out} = 10 mA, V_{in} – V_{out} = 2.0 V, T_J = 25°C) Adjustable Reference Voltage (Line, Load, and Temperature) Adjustable	V_{ref}	 1.235 1.225	 1.25 1.25	 1.265 1.275	V
Line Regulation (T_J = 25°C, I_{out} = 10 mA, V_{in} = [V_{out} + 1.5 V] to V_{in} = 20 V)	Reg_{line}	—	—	0.3	%
Load Regulation (T_J = 25°C, I_{out} = 10 mA to 800 mA)	Reg_{load}	—	—	0.5	%
Dropout Voltage (I_{out} = 500 mA)	V_{in} – V_{out}	—	1.0	1.25	V
Ripple Rejection (10 V_{p-p}, 120 Hz Sinewave; I_{out} = 500 mA)	RR	55	—	—	dB
Current Limit	I_{Limit}	800	—	—	mA
Quiescent Current Fixed Output	I_Q	 —	 5.5	 8.0	mA
Minimum Required Load Current Fixed Output Adjustable	I_{Load}	 — 8.0	 — —	 0 —	mA
Adjustment Pin Current	I_{Adj}	—	—	120	µA

Internal Schematic

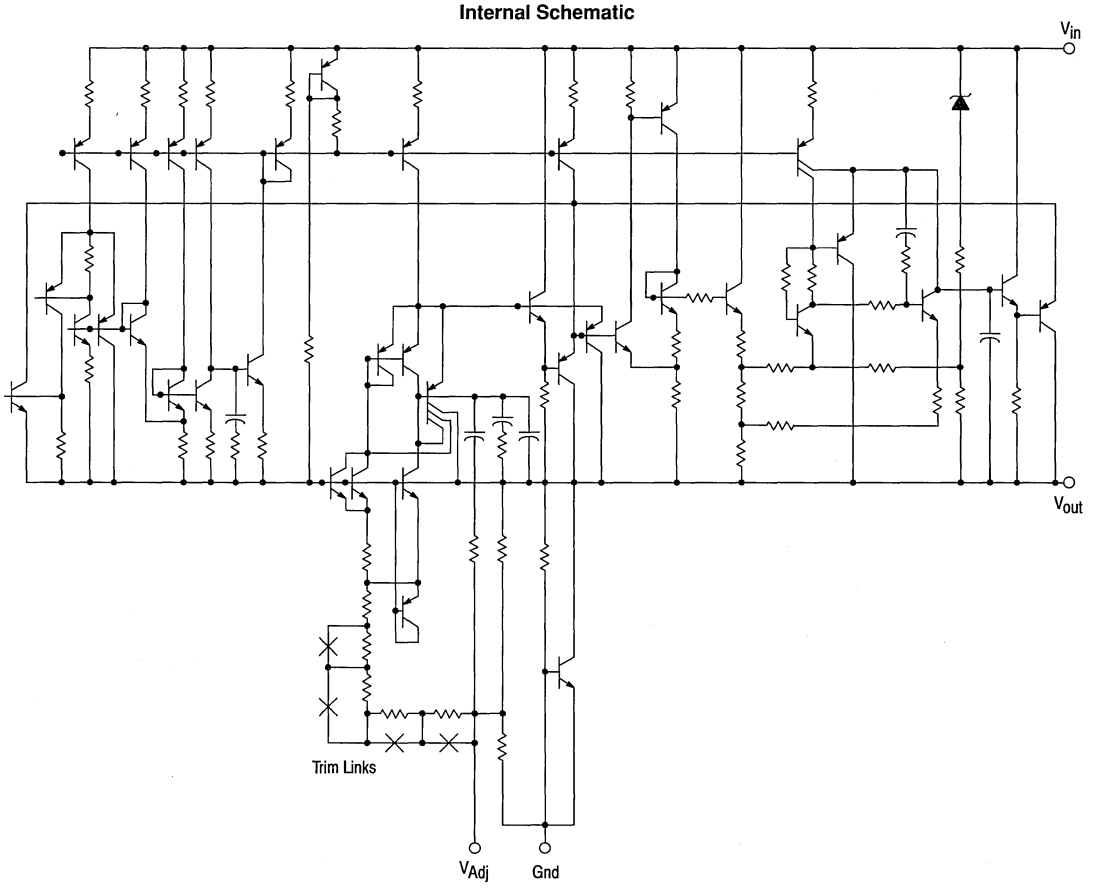


Figure 1. SOP-8 Thermal Resistance versus P.C.B. Copper Length

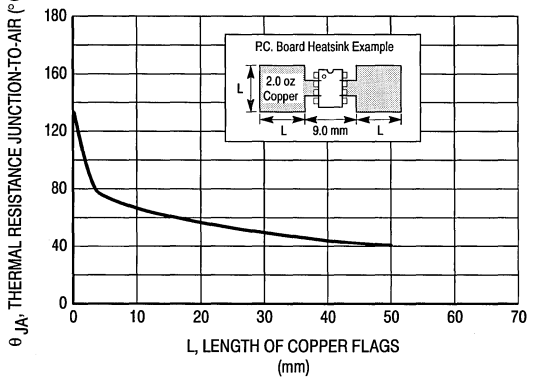


Figure 2. DPAK Thermal Resistance versus P.C.B. Copper Length

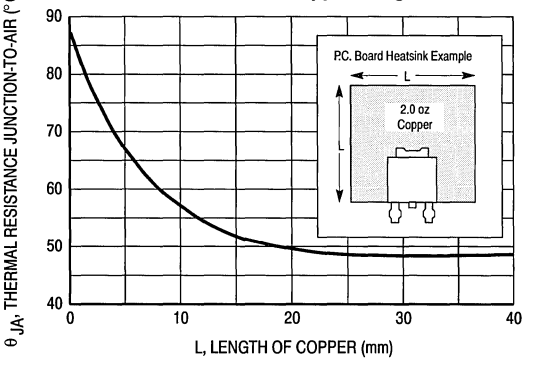


Figure 3. Dropout Voltage versus Output Load Current

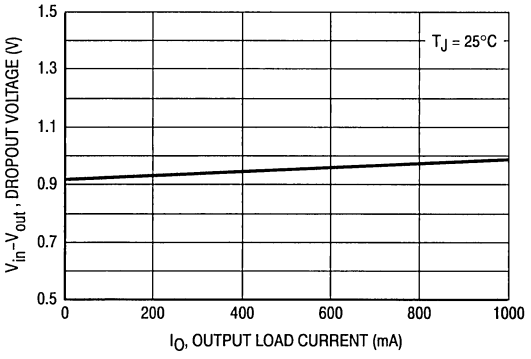


Figure 4. Transient Load Regulation

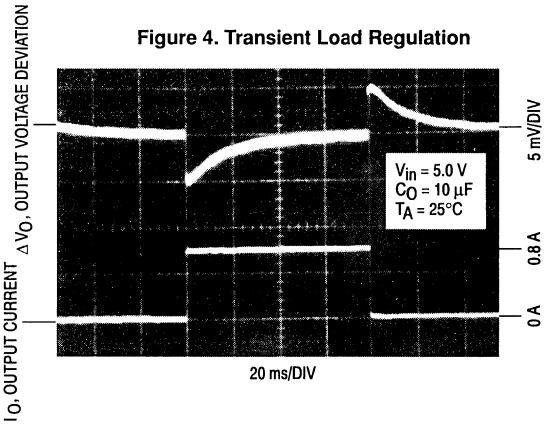


Figure 5. MC34269-3.3 Ripple Rejection versus Frequency

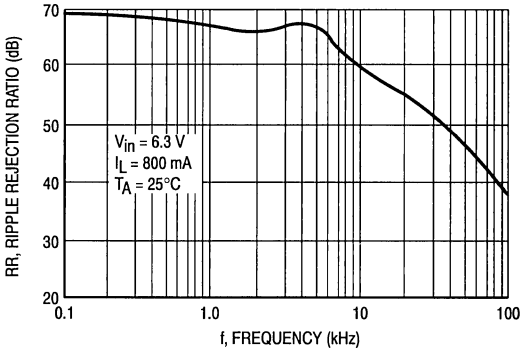


Figure 6. MC34269-5.0 Ripple Rejection versus Frequency

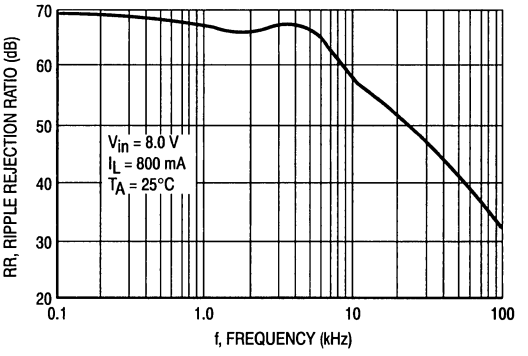


Figure 7. MC34269-12 Ripple Rejection versus Frequency

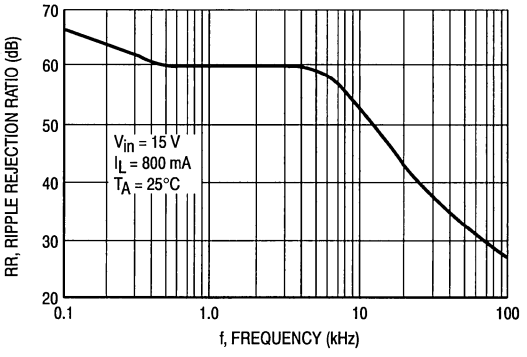
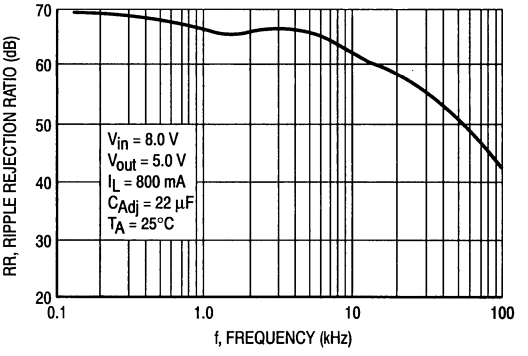


Figure 8. MC34269-ADJ Ripple Rejection versus Frequency



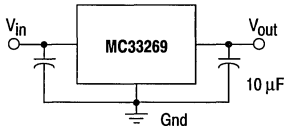
APPLICATIONS INFORMATION

Figures 9 through 13 are typical application circuits. The output current capability of the regulator is in excess of 800 mA, with a typical dropout voltage less than 1.0 V. Internal protective features include current and thermal limiting.

The MC33269 requires an external capacitor of at least 10 µF with an ESR of less than 10 Ω for stability over temperature. With economical electrolytic capacitors, cold temperature operation can pose a stability problem. As temperature decreases, the capacitance also decreases and the ESR increases, which could cause the circuit to oscillate. Tantalum capacitors may be a better choice if small size is a requirement. Also, the capacitance and ESR of a tantalum capacitor is more stable over temperature. An input capacitor is not necessary for stability, however, it will improve the overall performance of the part. **Applications should be tested over all operating conditions to insure stability.**

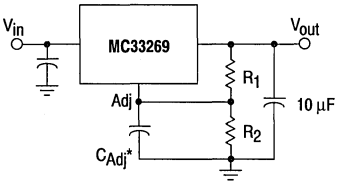
Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the output is disabled. There is no hysteresis built into the thermal limiting circuit. As a result, if the device is overheating, the output will appear to be oscillating. This feature is provided to prevent catastrophic failures from accidental device overheating.

Figure 9. Typical Fixed Output Application



An input capacitor is not necessary for stability, however it will improve the overall performance.

Figure 10. Typical Adjustable Output Application

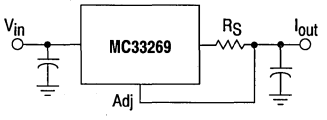


$$V_{out} = 1.25\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}R_2$$

*C_{Adj} is optional, however it will improve the ripple rejection.

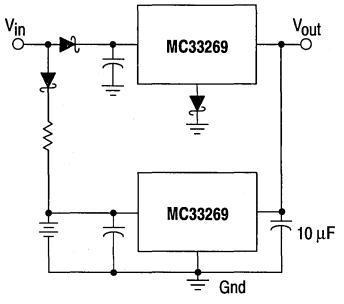
The MC34269-ADJ develops a 1.25 V reference voltage between the output and the adjust terminal. Resistor R_1, operates with constant current to flow through it and resistor R_2. This current should be set such that the Adjust Pin current causes negligible drop across resistor R_2. The total current with minimum load should be greater than 8.0 mA.

Figure 11. Current Regulator



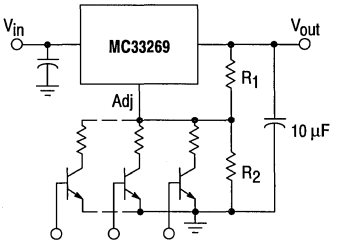
$$I_{out} = \frac{1.25}{R_S}$$

Figure 12. Battery Backed-Up Power Supply



The Schottky diode on the ground leg of the upper regulator shifts its output voltage higher by the forward voltage drop of the diode. This will cause the lower device to remain off until the input voltage is removed.

Figure 13. Digitally Controlled Voltage Regulator



R_2 sets the maximum output voltage. Each transistor reduces the output voltage when turned on.

MC34023
MC33023

Advance Information

High Speed Single-Ended PWM Controller

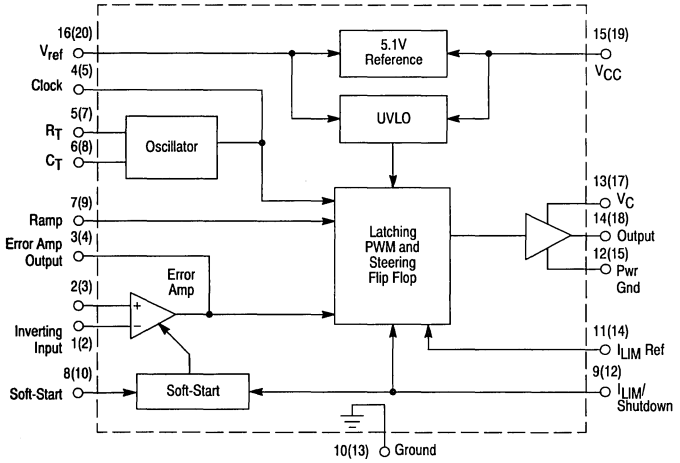
The MC34023 series are high speed, fixed frequency, single-ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost-effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, a wide bandwidth error amplifier, a high speed current sensing comparator, and a high current totem pole output ideally suited for driving power MOSFET.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, and a latch for single pulse metering.

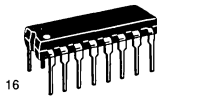
The flexibility of this series allows it to be easily configured for either current mode or voltage mode control.

- 50 ns Propagation Delay to Output
- High Current Totem Pole Output
- Wide Bandwidth Error Amplifier
- Fully-Latched Logic with Double Pulse Suppression
- Latching PWM for Cycle-By-Cycle Current Limiting
- Soft-Start Control with Latched Overcurrent Reset
- Input Undervoltage Lockout with Hysteresis
- Low Start-Up Current (400 µA Typ)
- Internally Trimmed Reference with Undervoltage Lockout
- 90% Maximum Duty Cycle (Externally Adjustable)
- Precision Trimmed Oscillator
- Voltage or Current Mode Operation to 1.0 MHz
- Designed Replacement for the UC3823

Simplified Block Diagram



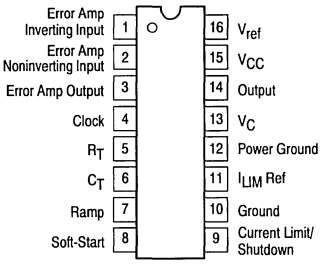
Pin numbers in parenthesis ( ) are for FN suffix, PLCC package.



P SUFFIX
PLASTIC PACKAGE
CASE 648

DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO-16L)

PIN CONNECTIONS

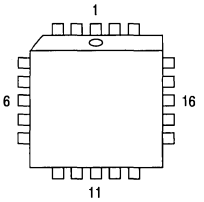


(Top View)

1. NC
2. Error Amp Inverting Input
3. Error Amp Noninverting Input
4. Error Amp Output
5. Clock
6. NC
7. R_T
8. C_T
9. Ramp
10. Soft-Start
11. NC
12. Current Limit/S.D.
13. Ground
14. I_{LIM} Ref
15. Power Gnd
16. NC
17. V_C
18. Output
19. V_{CC}
20. V_{ref}

FN SUFFIX
PLASTIC PACKAGE
CASE 775

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34023DW	0° to +70°C	SO-16L
MC34023P		Plastic DIP
MC34023FN		PLCC
MC33023DW	−40° to +105°C	SO-16L
MC33023P		Plastic DIP
MC33023FN		PLCC

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	30	V
Output Driver Supply Voltage	V_C	20	V
Output Current, Source or Sink (Note 1) DC Pulsed (0.5 μs)	I_O	 0.5 2.0	A
Current Sense, Soft-Start, Ramp, and Error Amp Inputs	V_{in}	– 0.3 to +7.0	V
Error Amp Output and Soft-Start Sink Current	I_O	10	mA
Clock and R_T Output Current	I_{CO}	5.0	mA
Power Dissipation and Thermal Characteristics SO-16L Package (Case 751G) Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction to Air DIP Package (Case 648) Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction to Air PLCC Package (Case 775) Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100 1.73 72	 mW °C/W W °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 2) MC34023 MC33023	T_A	 0 to +70 – 40 to + 105	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, R_T = 3.65 kΩ, C_T = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 2], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	5.05	5.1	5.15	V
Line Regulation (V_{CC} = 10 V to 30 V)	Reg_{line}	—	2.0	15	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	2.0	15	mV
Temperature Stability	T_S	—	0.2	—	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.45	—	5.25	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	—	50	—	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	—	5.0	—	mV
Output Short Circuit Current	I_{SC}	– 30	– 65	–100	mA
OSCILLATOR SECTION					
Frequency T_J = 25°C Line (V_{CC} = 10 V to 30 V) and Temperature (T_A = T_{low} to T_{high})	f_{osc}	 380 370	 400 400	 420 430	kHz
Frequency Change with Voltage (V_{CC} = 10 V to 30 V)	$\Delta f_{osc}/\Delta V$	—	0.2	1.0	%
Frequency Change with Temperature (T_A = T_{low} to T_{high})	$\Delta f_{osc}/\Delta T$	—	2.0	—	%
Sawtooth Peak Voltage	$V_{OSC(P)}$	2.6	2.8	3.0	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	0.7	1.0	1.25	V
Clock Output Voltage High State Low State	 V_{OH} V_{OL}	 3.9 —	 4.5 2.3	 — 2.9	V

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34023 = – 40°C for MC33023 T_{high} = +70°C for MC34023 = +105°C for MC33023

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, R_T = 3.65 kΩ, C_T = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 2], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION					
Input Offset Voltage	V_{IO}	—	—	15	mV
Input Bias Current	I_{IB}	—	0.6	3.0	μA
Input Offset Current	I_{IO}	—	0.1	1.0	μA
Open-Loop Voltage Gain (V_O = 1.0 V to 4.0 V)	A_{VOL}	60	95	—	dB
Gain Bandwidth Product (T_J = 25°C)	BW	4.0	8.3	—	MHz
Common Mode Rejection Ratio (V_{CM} = 1.5 V to 5.5 V)	CMRR	75	95	—	dB
Power Supply Rejection Ratio (V_{CC} = 10 V to 30 V)	PSRR	85	110	—	dB
Output Current, Source (V_O = 4.0 V) Sink (V_O = 1.0 V)	I_{Source} I_{Sink}	0.5 1.0	3.0 3.6	— —	mA
Output Voltage Swing, High State (I_O = –0.5 mA) Low State (I_O = 1 mA)	V_{OH} V_{OL}	4.5 0	4.75 0.4	5.0 1.0	V
Slew Rate	SR	6.0	12	—	V/μs
PWM COMPARATOR SECTION					
Ramp Input Bias Current	I_{IB}	—	–0.5	–5.0	μA
Duty Cycle, Maximum Minimum	$DC_{(max)}$ $DC_{(min)}$	80 —	90 —	— 0	%
Zero Duty Cycle Threshold Voltage Pin 3(4) (Pin 7(9) = 0 V)	V_{th}	1.1	1.25	1.4	V
Propagation Delay (Ramp Input to Output, T_J = 25°C)	$t_{PLH(in/out)}$	—	60	100	ns
SOFT-START SECTION					
Charge Current ($V_{Soft\text{-}Start}$ = 0.5 V)	I_{chg}	3.0	9.0	20	μA
Discharge Current ($V_{Soft\text{-}Start}$ = 1.5 V)	I_{dischg}	1.0	4.0	—	mA
CURRENT SENSE SECTION					
Input Bias Current (Pin 9(12) = 0 V to 4.0 V)	I_{IB}	—	—	15	μA
Current Limit Comparator Offset (Pin 11(14) = 1.1 V)	V_{IO}	—	—	15	mV
Current Limit Reference Input Common Mode Range (Pin 11(14))	V_{CMR}	1.0	—	1.25	V
Shutdown Comparator Threshold	V_{th}	1.25	1.40	1.55	V
Propagation Delay (Current Limit/Shutdown to Output, T_J = 25°C)	$t_{PLH(in/out)}$	—	50	80	ns
OUTPUT SECTION					
Output Voltage Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA) High State (I_{Source} = 20 mA) (I_{Source} = 200 mA)	 V_{OL} V_{OH} 	 — — 13 12	 0.25 1.2 13.5 13	 0.4 2.2 — —	V
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 0.5 mA)	$V_{OL(UVLO)}$	—	0.25	1.0	V
Output Leakage Current (V_C = 20 V)	I_L	—	100	500	μA
Output Voltage Rise Time (C_L = 1.0 nF, T_J =25°C)	t_r	—	30	60	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J =25°C)	t_f	—	30	60	ns
UNDERVOLTAGE LOCKOUT SECTION					
Start-Up Threshold (V_{CC} Increasing)	$V_{th(on)}$	8.8	9.2	9.6	V
UVLO Hysteresis	V_H	0.4	0.8	1.2	V
TOTAL DEVICE					
Power Supply Current Start-Up Operating	I_{CC} 	 — —	 0.5 20	 0.8 30	mA

3

Figure 1. Timing Resistor versus Oscillator Frequency

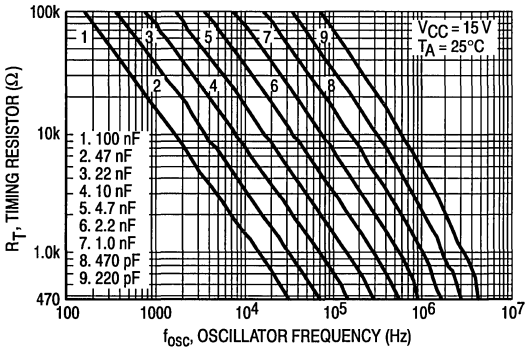

Figure 2. Oscillator Frequency versus Temperature

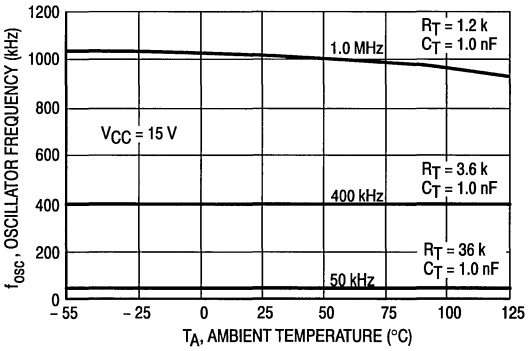

Figure 3. Error Amp Open-Loop Gain and Phase versus Frequency

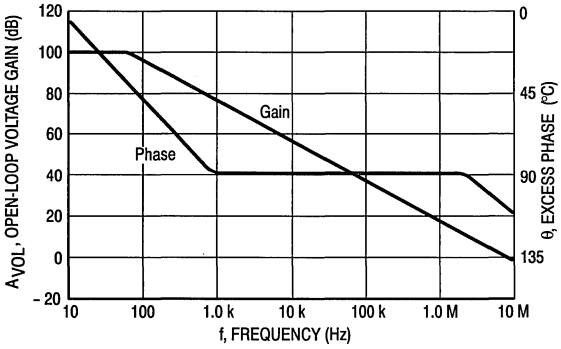

Figure 4. PWM Comparator Zero Duty Cycle Threshold Voltage versus Temperature

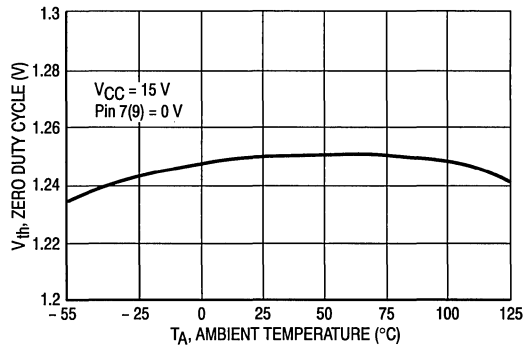

Figure 5. Error Amp Small Signal Transient Response

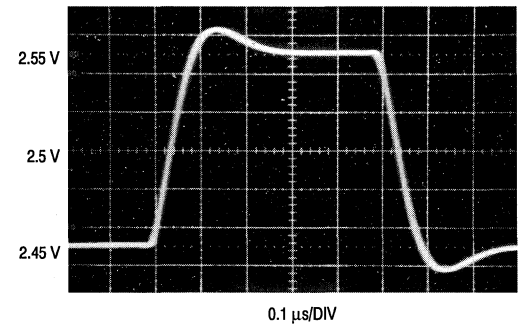

Figure 6. Error Amp Large Signal Transient Response

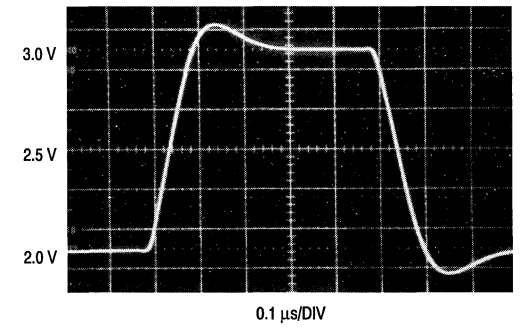

Figure 7. Reference Voltage Change versus Source Current

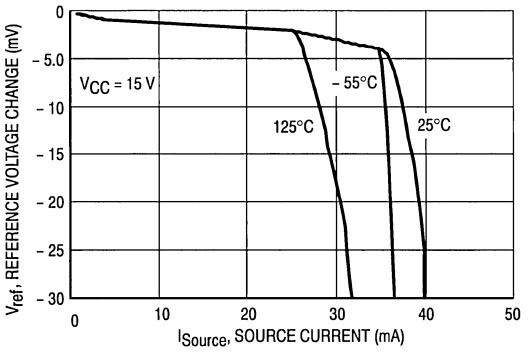

Figure 8. Reference Short Circuit Current versus Temperature

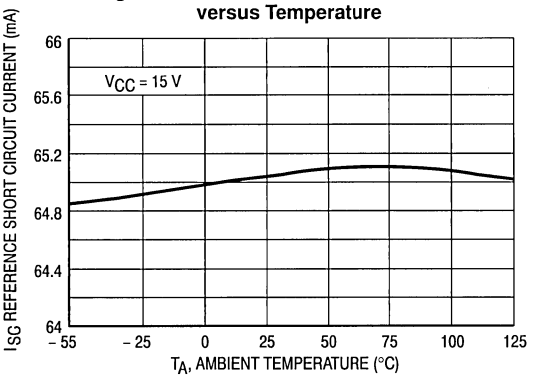

Figure 9. Reference Line Regulation

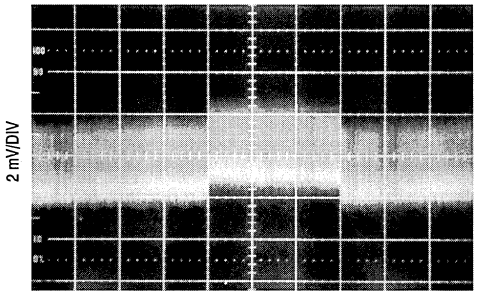

Figure 10. Reference Load Regulation

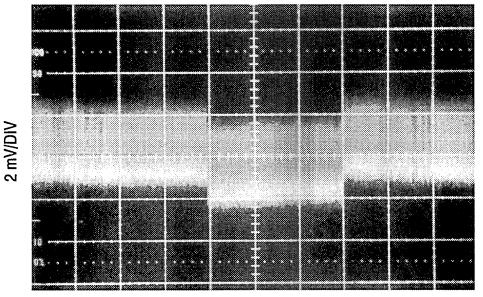

Figure 11. Current Limit Comparator Offset Voltage versus Temperature

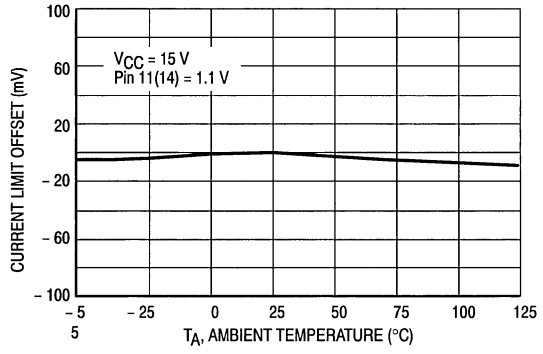

Figure 12. Shutdown Comparator Threshold versus Temperature

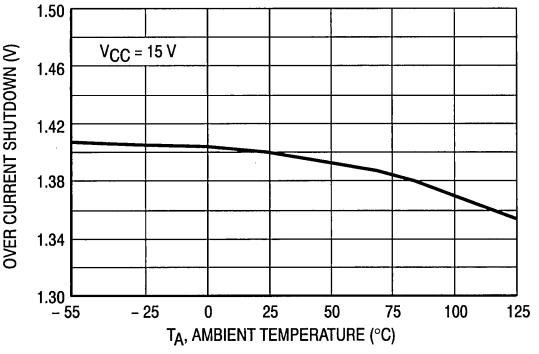

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Figure 13. Soft-Start Charge Current versus Temperature

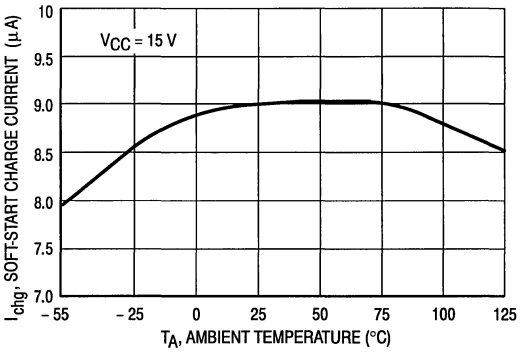


Figure 14. Output Saturation Voltage versus Load Current

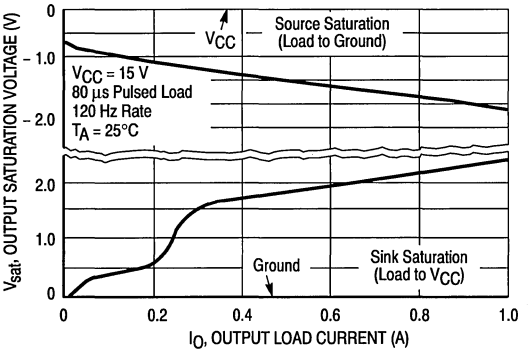
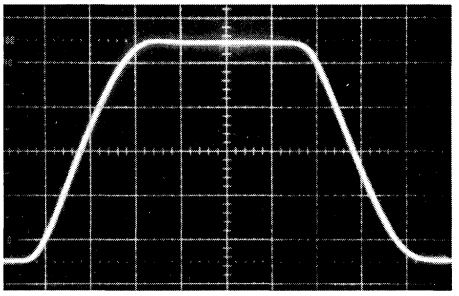
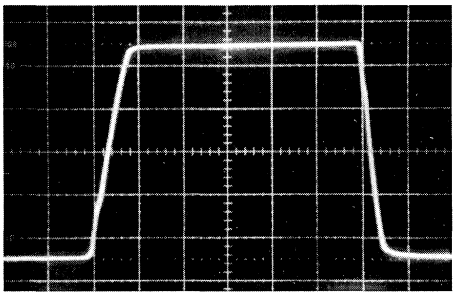


Figure 15. Drive Output Rise and Fall Time



OUTPUT RISE & FALL TIME 1.0 nF LOAD
50 ns/DIV

Figure 16. Drive Output Rise and Fall Time



OUTPUT RISE & FALL TIME 10.0 nF LOAD
50 ns/DIV

Figure 17. Supply Voltage versus Supply Current

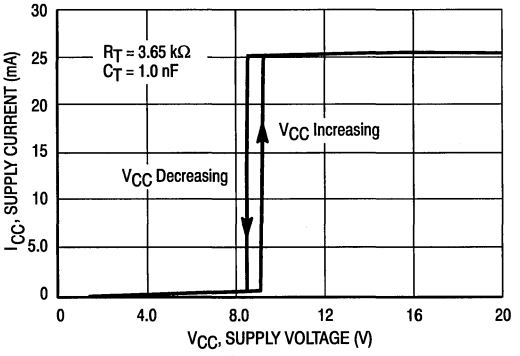
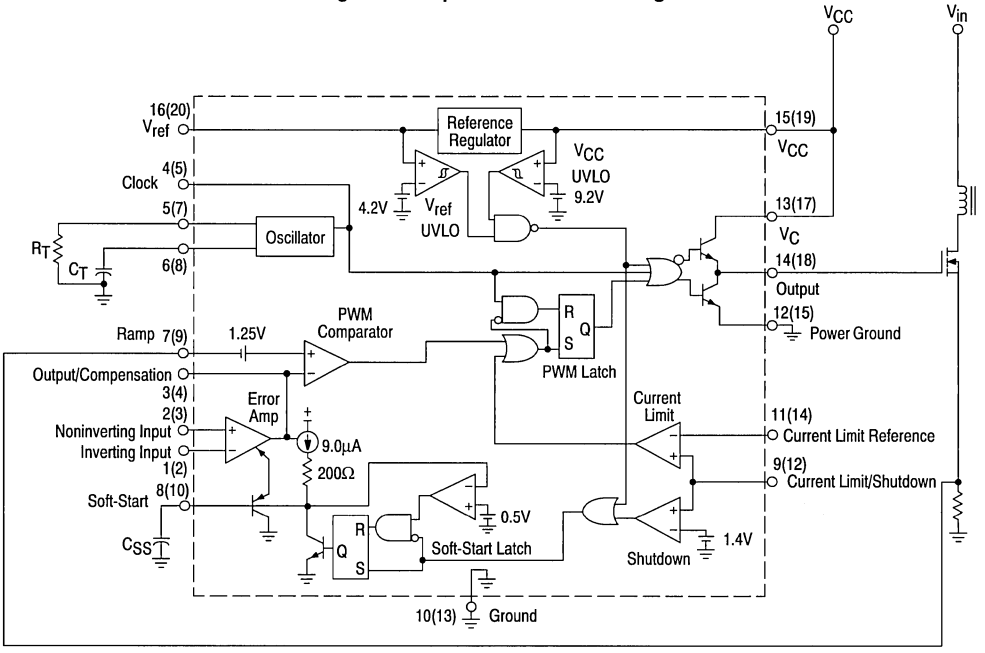
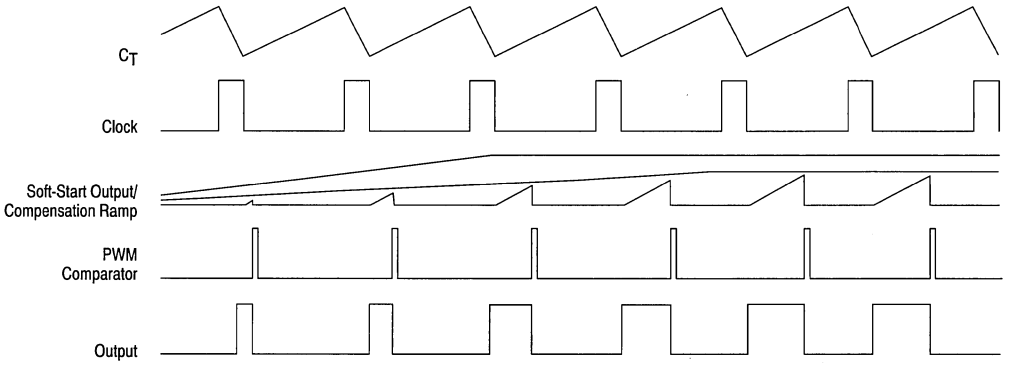


Figure 18. Representative Block Diagram



Pin numbers in parenthesis ( ) are for FN suffix, PLCC package.

Figure 19. Current Limit Operating Waveforms



OPERATING DESCRIPTION

The MC33023 and MC34023 series are high speed, fixed frequency, single-ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 18.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. The R_T pin is set to a temperature compensated 3.0 V. By selecting the value of R_T, the charge current is set through a current mirror for the timing component (C_T). This charge current runs continuously through C_T. The discharge current is ratioed to be 10 times the charge current, which yields the maximum duty cycle of 90%. C_T is charged to 2.8 V and discharged to 1.0 V. During the discharge of C_T, the oscillator generates an internal blanking pulse that resets the PWM Latch, inhibits the outputs, and toggles the steering flip-flop. The threshold voltages on the oscillator comparator is trimmed to guarantee an oscillator accuracy of 5.0% at 25°C.

Additional dead time can be added by externally increasing the charge current to C_T. This changes the charge to discharge ratio of C_T which is set internally to $I_{charge}/10$ I_{charge}. The new charge to discharge ratio will be:

$$\% \text{ Deadtime} = \frac{I_{additional} + I_{charge}}{10\ (I_{charge})}$$

A bidirectional clock pin is provided for synchronization or for master/slave operation. When synchronizing the MC34023 to an external clock source, the oscillator should be set about 10% less than the external clock frequency. If master/slave operation of more than one MC34023 is desired, the master IC should have the desired R_T, C_T values. The clock pin of the master is connected to the clock pin on the slave(s). The R_T pin on the slave(s) should be connected to V_{ref} and the C_T pin should be connected to ground. If the master IC is not close to the slave IC(s), the clock pin should be buffered. Refer to Figures 27, 28, and 29 for some application hints.

Error Amplifier

A fully compensated Error Amplifier is provided. It features a typical DC voltage gain of 95 dB and a unity gain bandwidth of 5.5 MHz with 75 degrees of phase margin (Figure 3). Typical application circuits will have the noninverting input tied to the reference. The inverting input will typically be connected to a feedback voltage generated from the output of the switching power supply. The Error Amplifier Output is provided for external loop compensation.

Soft-Start Latch

Soft-Start is accomplished in conjunction with an external capacitor. The Soft-Start capacitor is charged by an internal 10 μA current source. This capacitor clamps the output of the error amplifier to less than its normal output voltage, thus limiting the duty cycle. The time it takes for a capacitor to reach full charge is given by:

$$t \approx (4.5 \bullet 10^5) C_{Soft\text{-}Start}$$

A Soft-Start latch is incorporated to prevent erratic operation of this circuitry. Two conditions can cause the Soft-Start circuit to latch so that the Soft-Start capacitor stays discharged. The first condition is activation of an undervoltage lockout of either V_{CC} or V_{ref}. The second condition is when current sense input exceeds 1.4 V. Since this latch is "set dominant", it cannot be reset until either of these signals is removed and, the voltage at $C_{Soft\text{-}Start}$ is less than 1.0 V.

PWM Comparator and Latch

A PWM circuit typically compares an error voltage with a ramp signal. The outcome of this comparison determines the state of the output. In voltage mode operation the ramp signal is the voltage ramp of the timing capacitor. In current mode operation the ramp signal is the voltage ramp induced in a current sensing element. The ramp input of the PWM comparator is pinned out so that the user can decide which mode of operation best suits the application requirements. The ramp input has a 1.25 V offset such that whenever the voltage at this pin exceeds the error amplifier output voltage minus 1.25 V, the PWM comparator will cause the PWM latch to set, disabling the outputs. Once the PWM latch is set, only a blanking pulse by the oscillator can reset it, thus initiating the next cycle.

Current Limiting and Shutdown

A pin is provided to perform current limiting and shutdown operations. Two comparators are connected to the input of this pin. The reference voltage for the current limit comparator is not set internally. A pin is provided so the user can set the voltage. When the voltage at the current limit input pin exceeds the externally set voltage, the PWM latch is set, disabling the output. In this way cycle-by-cycle current limiting is accomplished. If a current limit resistor is used in series with the power devices, the value of the resistor is found by:

$$R_{Sense} = \frac{I_{Limit\ Reference\ Voltage}}{I_{pk(switch)}}$$

If the voltage at this pin exceeds 1.4 V, the second comparator is activated. This comparator sets a latch which, in turn, causes the soft start capacitor to be discharged. In this way a "hiccup" mode of recovery is possible in the case of output short circuits. If a current limit resistor is used in series with the output devices, the peak current at which the controller will enter a "hiccup" mode is given by:

$$I_{shutdown} = \frac{1.4\ V}{R_{Sense}}$$

Undervoltage Lockout

There are two undervoltage lockout circuits within the IC. The first senses V_{CC} and the second V_{ref}. During power-up, V_{CC} must exceed 9.2 V and V_{ref} must exceed 4.0 before the outputs can be enabled and the Soft-Start latch released. If V_{CC} falls below 8.4 V or V_{ref} falls below 3.6 V, the outputs are disabled and the soft start latch is activated. When the UVLO is active, the part is in a low current standby mode allowing the IC to have an off-line bootstrap start-up circuit. Typical start-up current is 400 μA.

Output

The MC34023 has a high current totem pole output specifically designed for direct drive of power MOSFETs. They are capable of up to ±2.0 A peak drive current with a typical rise and fall time of 30 ns driving a 1.0 nF load.

Separate pins for V_C and Power Ground are provided. With proper implementation, a significant reduction of switching transient noise imposed on the control circuitry is possible. The separate V_C supply input also allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}.

Reference

A 5.1 V bandgap reference is pinned out and is trimmed to an initial accuracy of ±1.0% at 25°C. This reference has short circuit protection and can source in excess of 10 mA for powering additional control system circuitry.

Design Considerations

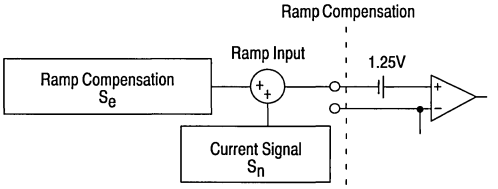
Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. With high frequency, high power, switching power supplies it is imperative to have separate current loops for the signal paths and for the power paths. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. Shown in Figure 35 is a printed circuit layout of the application circuit. Note how the power and ground traces are run. All bypass capacitors and snubbers should be connected as close as possible to the specific part in question. The PC board lead lengths must be less than 0.5 inches for effective bypassing for snubbing.

Instabilities

In current mode control, an instability can be encountered at any given duty cycle. The instability is caused by the current feedback loop. It has been shown that the instability is caused by a double pole at half the switching frequency. If an external ramp (S_e) is added to the on-time ramp (S_n) of the current-sense waveform, stability can be achieved (see Figure 20).

One must be careful not to add too much ramp compensation. If too much is added the system will start to perform like a voltage mode regulator. All benefits of current mode control will be lost. Figure 25 is an example of one way in which external ramp compensation can be implemented.

Figure 20. Ramp Compensation



A simple equation can be used to calculate the amount of external ramp necessary to add that will achieve stability in the current loop. For the following equations, the calculated values for the application circuit in Figure 34 are also shown.

$$S_e = \frac{V_{sec}(\partial(max) - 0.18)A_i}{L}$$

where: V_{sec} = minimum voltage at the input of the output inductor
$\partial(max)$ = maximum duty cycle
A_i = gain of the current sense network (see Figures 23, 24, and 25)
L = output inductor

For the application circuit: $S_e = \frac{7(0.8 - 0.18)0.075}{1.8\,\mu} = 18 \bullet 10^4$

As a sanity check, the modulator gain of the circuit can be calculated by:

$$m_{c1} = 1 + S_e/S_n$$

$$S_n = \frac{di}{dt} A_i$$

where: di = output inductor slope
dt = maximum on time
A_i = gain of the current sense network (see Figures 25, 26, 27).

For the application circuit:

$$S_n = \frac{3.0}{0.8 \bullet 10^6} \quad 0.075 = 22.5 \bullet 10^4$$

$$m_{c1} = 1 + \frac{18 \bullet 10^4}{22.5 \bullet 10^4} = 1.8$$

This can be compared against the maximum modulator gain necessary to make the system immune to audio susceptibility tests:

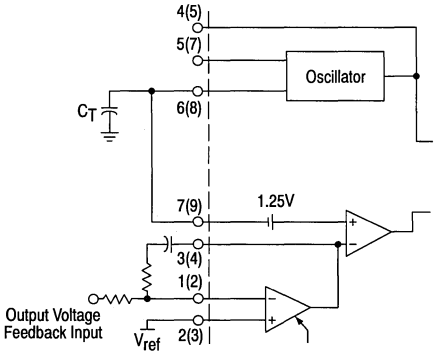
$$m_{c2} = \frac{2 - \partial}{2\partial'}, \text{ where: } \partial = \text{max duty cycle}, \quad \partial' = \text{1–max duty cycle}$$

For the application circuit: $m_{c2} = \frac{2 - 0.8}{2(0.2)} = 3$, m_{c2} should be larger than m_{c1}.

PIN FUNCTION DESCRIPTION

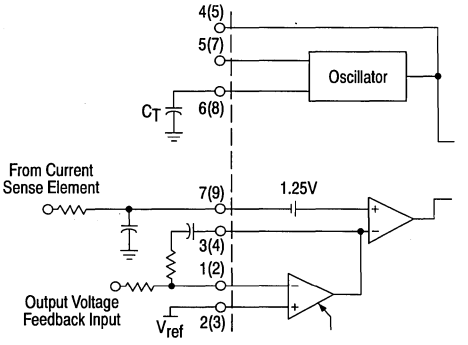
Pin		Function	Description
DIP/SOIC	PLCC		
1	2	Error Amp Inverting Input	This pin is usually used for feedback from the output of the power supply.
2	3	Error Amp Noninverting Input	This pin is used to provide a reference in which an error signal can be produced on the output of the error amp. Usually this is connected to V_{ref}, however an external reference can also be used.
3	4	Error Amp Output	This pin is provided for compensating the error amp for poles and zeros encountered in the power supply system, mostly the output LC filter.
4	5	Clock	This is a bidirectional pin used for synchronization.
5	7	R_T	The value of R_T sets the charge current through timing Capacitor, C_T.
6	8	C_T	In conjunction with R_T, the timing Capacitor sets the switching frequency. Because this part is a push-pull output, each output runs at one-half the frequency set at this pin.
7	9	Ramp Input	For voltage mode operation this pin is connected to C_T. For current mode operation this pin is connected through a filter to the current sensing element.
8	10	Soft-Start	A capacitor at this pin sets the Soft-Start time.
9	12	Current Limit/Shutdown	This pin has two functions. First, it provides cycle-by-cycle current limiting. Second, if the current is excessive, this pin will reinitiate a Soft-Start cycle.
10	13	Ground	This pin is the ground for the control circuitry.
11	14	Current Limit Reference Input	This is a high current dual totem pole output.
12	15	Power Ground	This is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
13	17	V_C	This is a separate power source connection for the outputs that is connected back to the power source input. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
14	18	Output	This is a high current dual totem pole output.
15	19	V_{CC}	This pin is the positive supply of the control IC.
16	20	V_{ref}	This is a 5.0 V reference. It is usually connected to the noninverting input of the error amplifier.

Figure 21. Voltage Mode Operation



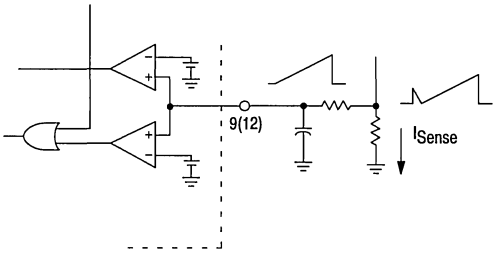
In voltage mode operation, the control range on the output of the Error Amplifier from 0% to 90% duty cycle is from 2.25 V to 4.05 V.

Figure 22. Current Mode Operation



In current mode control, an RC filter should be placed at the ramp input to filter the leading edge spike caused by turn-on of a power MOSFET.

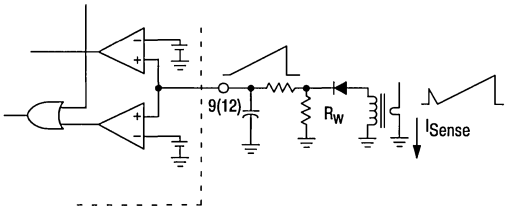
Figure 23. Resistive Current Sensing



The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. If a transformer is used, the gain can be calculated by:

$$A_i = \frac{R_{Sense}}{\text{turns ratio}}$$

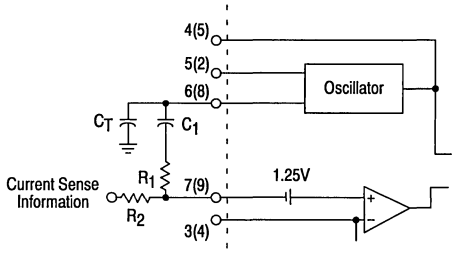
Figure 24. Primary Side Current Sensing



The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. The gain can be calculated by:

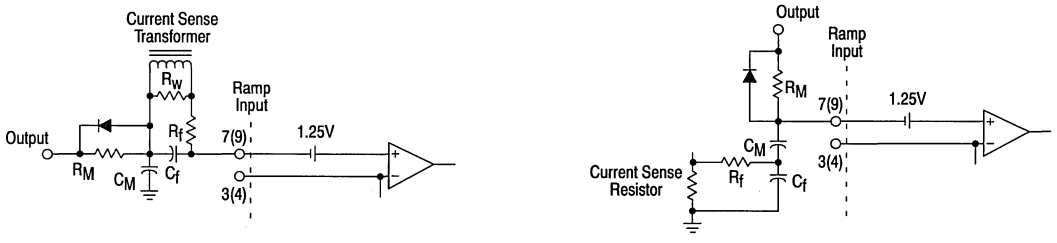
$$A_i = \frac{R_W}{\text{turns ratio}}$$

Figure 25A. Slope Compensation (Noise Sensitive)



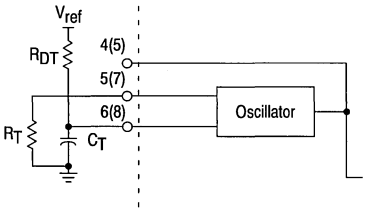
This method of slope compensation is easy to implement, however, it is noise sensitive. Capacitor C_1 provides AC coupling. The oscillator signal is added to the current signal by a voltage divider consisting of resistors R_1 and R_2.

Figure 25B. Slope Compensation (Noise Immune)



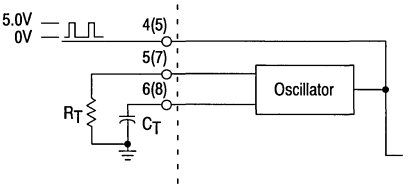
When only one output, this method of slope compensation can be used and it is relatively noise immune. Resistor R_M and capacitor C_M provide the added slope necessary. By choosing R_M and C_M with a larger time constant than the switching frequency, you can assume that its charge is linear. First choose C_M, then R_M can be adjusted to achieve the required slope. The diode provides a reset pulse the ramp inputs at the end of every cycle. The charge current I_M can be calculated by $I_M = C_M S_e$. Then R_M can be calculated by $R_M = V_{CC}/I_M$

Figure 26. Dead Time Addition



Additional dead time can be added by the addition of a dead time resistor from V_{ref} to C_T. See text on Oscillator section for more information.

Figure 27. External Clock Synchronization



The sync pulse fed into the clock pin must be at least 3.9 V. R_T and C_T need to be set 10% slower than the sync frequency. This circuit is also used in Voltage Mode operation for master/slave operation. The clock signal would be coming from the master which is set at the desired operating frequency, while the slave is set 10% slower.

Figure 28. Master/Slave Operation Over Short Distances

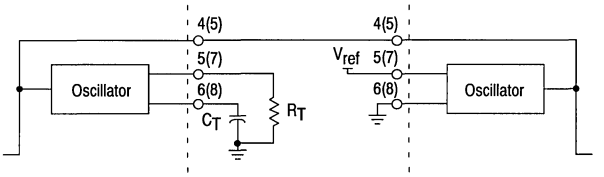


Figure 29. Master/Slave Operation Over Long Distances

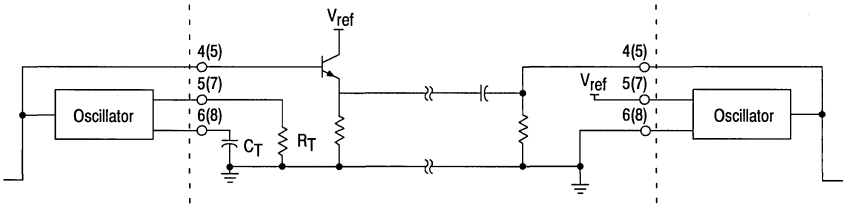
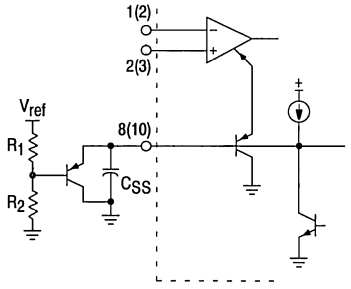


Figure 30. Buffered Maximum Clamp Level

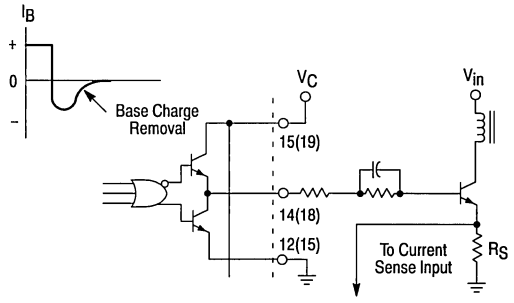


In voltage mode operation, the maximum duty cycle can be clamped. By the addition of a PNP transistor to buffer the clamp voltage, the Soft-Start current is not affected by R_1.

The new equation for Soft-Start is $t \approx \frac{V_{clamp} + 0.6}{9.0\ \mu A} (C_{SS})$

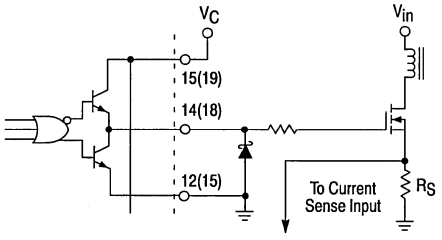
In current mode operation, this circuit will limit the maximum voltage allowed at the ramp input to end a cycle.

Figure 31. Bipolar Transistor Drive



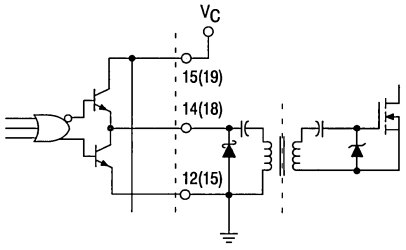
A series gate resistor may be needed to dampen high frequency parasitic oscillation caused by the MOSFET's input capacitance and any series wiring inductance in the gate-source circuit. The series resistor will also decrease the MOSFET switching speed. A Schottky diode can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground. The Schottky diode also prevents substrate injection when the output pin is driven below ground.

Figure 32. MOSFET Parasitic Oscillations



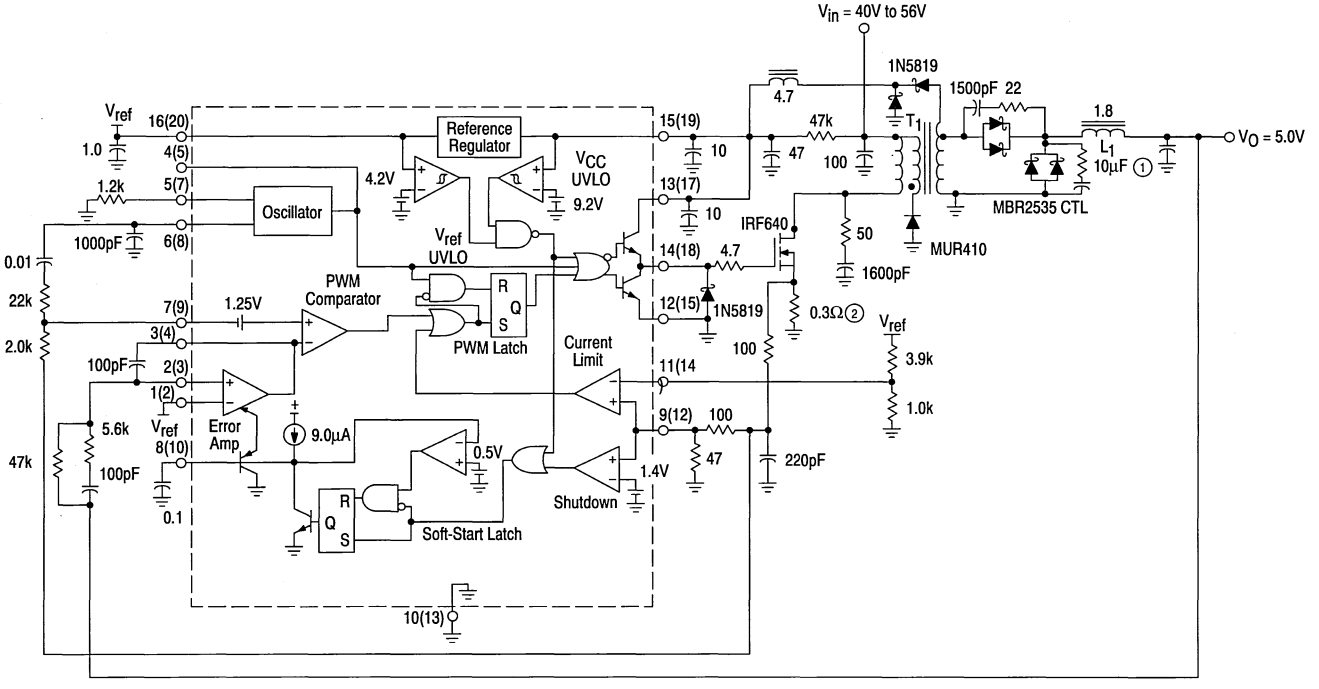
The totem pole output can furnish negative base current for enhanced transistor turn-off, with the addition of the capacitor in series with the base.

Figure 33. Isolated MOSFET Drive



The totem pole output can easily drive pulse transformers. A Schottky diode is recommended when driving inductive loads at high frequencies. The diode can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 34. Application Circuit



Pin numbers in parenthesis ( ) are FN suffix, PLCC package.

T_1 — Primary: 8 turns #48 AWG (1300 strands litz wire)
Secondary: 2 turns 0.003″ (2 layers) copper foil
Bootstrap: 1 turn added to secondary #36 AWG
Core: Philips 3F3, part #4312 020 4124
Bobbin: Philips part #4322 021 3525
Coilcraft P3269-A

L_1 — 2 turns #48 AWG (1300 strands litz wire)
Core: Philips 3F3, part #EP10-3F3
Bobbin: Philips part #EP10PCB1-8
L = 1.8 µH
Coilcraft P3270-A

Heatsinks — Power FET: AAVID Heatsink #533902B02554 with clip
Output Recitfiers: AAVID Heatsink #533402B02552 with clip

Insulators — All power devices are insulated with Berquist Sil-Pad 150

À — 10(1.0 µF) ceramic capacitors in parallel

Á — 5(1.5 Ω) resistors in parallel

Test	Condition	Results
Line Regulation	V_{in} = 40 V to 56 V, I_O = 7.5 A	14 mV = ± 0.275%
Load Regulation	V_{in} = 48 V, I_O = 4.0 A to 7.5 A	54 mV = ± 1.0%
Output Ripple	V_{in} = 48 V, I_O = 7.5 A	100 mVp-p
Efficiency	V_{in} = 48 V, I_O = 7.5 A	69.8%

Figure 35. PC Board With Components

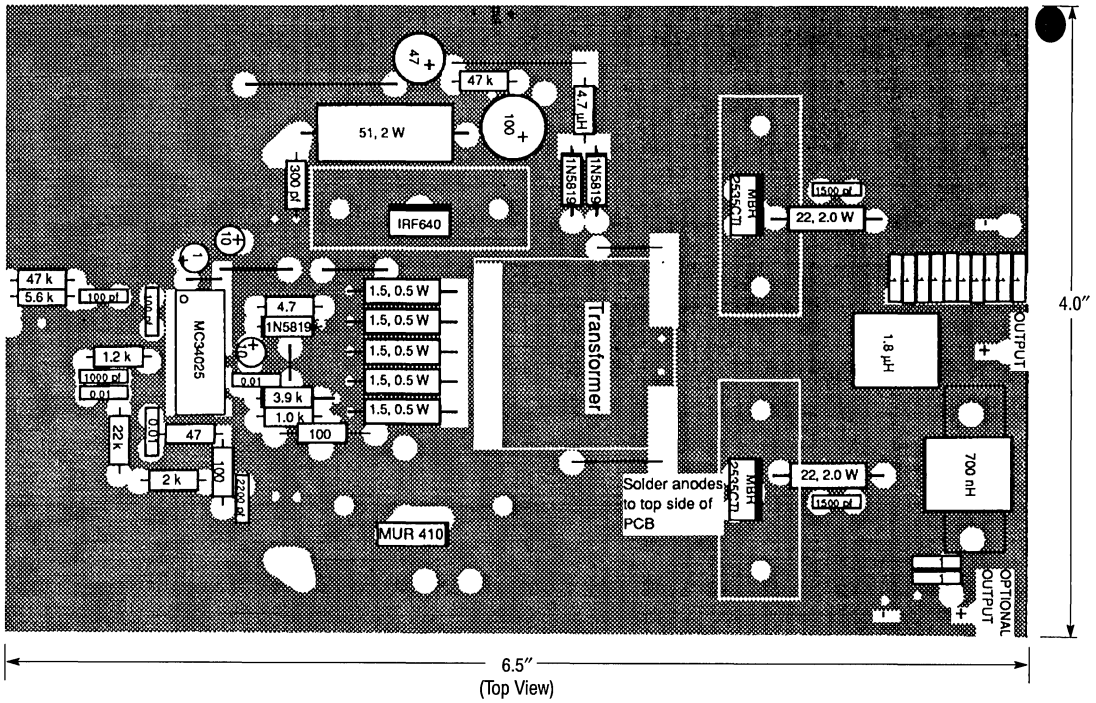
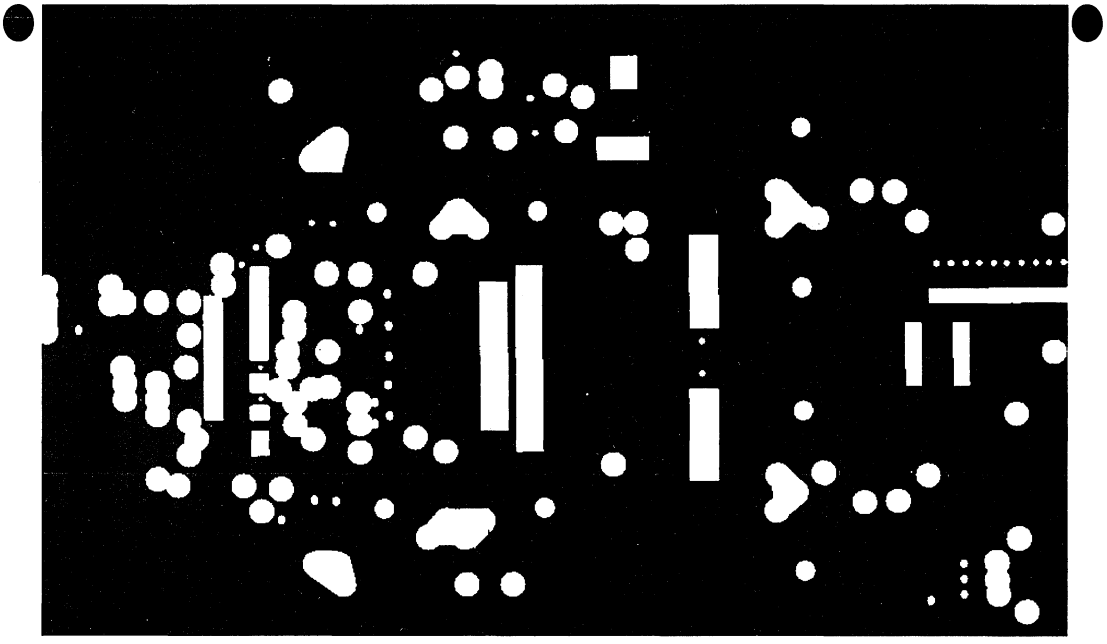
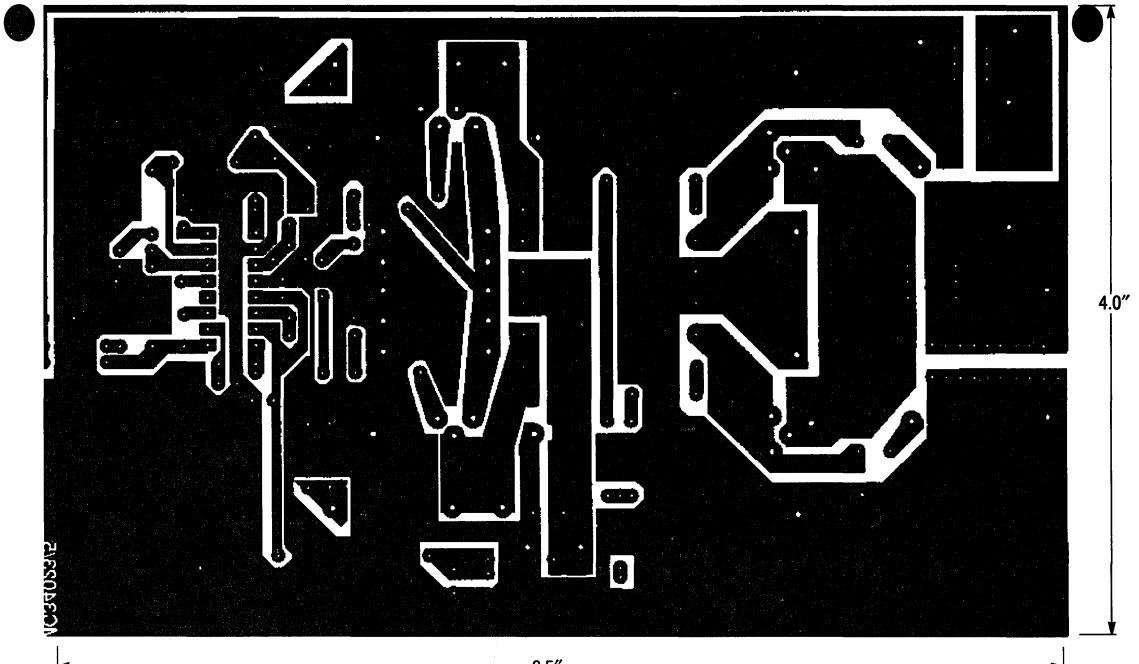


Figure 36. PC Board Without Components



(Top View)



(Bottom View)

MC34025
MC33025

3

Advance Information

High Speed Double-Ended PWM Controller

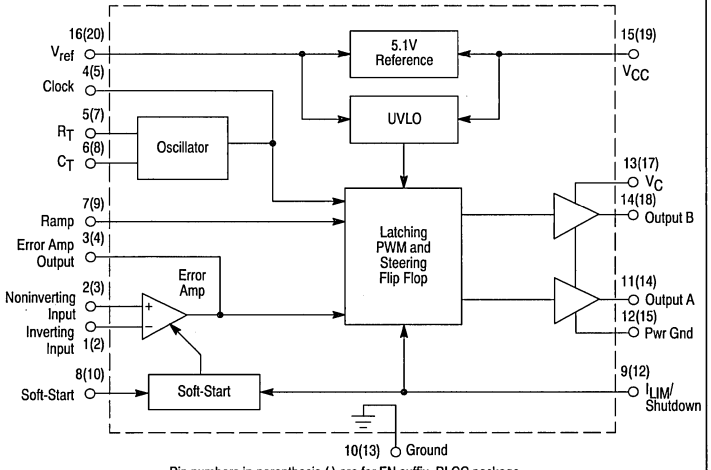
The MC34025 series are high speed, fixed frequency, double-ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, a wide bandwidth error amplifier, a high speed current sensing comparator, steering flip-flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, and a latch for single pulse metering.

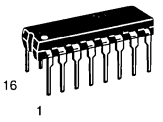
The flexibility of this series allows it to be easily configured for either current mode or voltage mode control.

- 50 ns Propagation Delay to Outputs
- Dual High Current Totem Pole Outputs
- Wide Bandwidth Error Amplifier
- Fully-Latched Logic with Double Pulse Suppression
- Latching PWM for Cycle-By-Cycle Current Limiting
- Soft-Start Control with Latched Overcurrent Reset
- Input Undervoltage Lockout with Hysteresis
- Low Start-Up Current (400 μA Typ)
- Internally Trimmed Reference with Undervoltage Lockout
- 90% Maximum Duty Cycle (Externally Adjustable)
- Precision Trimmed Oscillator
- Voltage or Current Mode Operation to 1.0 MHz
- Designed Replacement for the UC3825

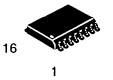
Simplified Block Diagram



Pin numbers in parenthesis ( ) are for FN suffix, PLCC package.

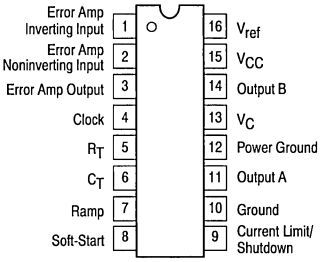


P SUFFIX
PLASTIC PACKAGE
CASE 648



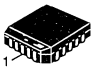
DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO-16L)

PIN CONNECTIONS



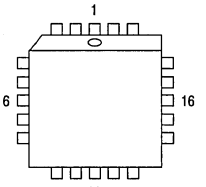
(Top View)

1. NC
2. Error Amp Inverting Input
3. Error Amp Noninverting Input
4. Error Amp Output
5. Clock
6. NC
7. R_T
8. C_T
9. Ramp
10. Soft-Start
11. NC
12. Current Limit/S.D.
13. Ground
14. Output A
15. Power Gnd
16. NC
17. V_C
18. Output
19. V_{CC}
20. V_{ref}



FN SUFFIX
PLASTIC PACKAGE
CASE 775

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34025DW	0° to +70°C	SO-16L
MC34025P		Plastic DIP
MC34025FN		PLCC
MC33025DW	−40° to +105°C	SO-16L
MC33025P		Plastic DIP
MC33025FN		PLCC

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	30	V
Output Driver Supply Voltage	V_C	20	V
Output Current, Source or Sink (Note 1) DC Pulsed (0.5 μs)	I_O	 0.5 2.0	A
Current Sense, Soft-Start, Ramp, and Error Amp Inputs	V_{in}	– 0.3 to +7.0	V
Error Amp Output and Soft-Start Sink Current	I_O	10	mA
Clock and R_T Output Current	I_{CO}	5.0	mA
Power Dissipation and Thermal Characteristics SO-16 Package (Case 751G) Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction-to-Air DIP Package (Case 648) Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction-to-Air PLCC Package (Case 775) Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction-to-Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100 1.73 72	 mW °C/W W °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 2) MC34025 MC33025	T_A	 0 to +70 – 40 to + 105	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, R_T = 3.65 kΩ, C_T = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 2], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	5.05	5.1	5.15	V
Line Regulation (V_{CC} = 10 V to 30 V)	Reg_{line}	—	2.0	15	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	2.0	15	mV
Temperature Stability	T_S	—	0.2	—	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.95	—	5.25	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	—	50	—	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	—	5.0	—	mV
Output Short Circuit Current	I_{SC}	–30	–65	–100	mA
OSCILLATOR SECTION					
Frequency T_J = 25°C Line (V_{CC} = 10 V to 30 V) and Temperature (T_A = T_{low} to T_{high})	f_{osc}	 380 370	 400 400	 420 430	kHz
Frequency Change with Voltage (V_{CC} = 10 V to 30V)	$\Delta f_{osc}/\Delta V$	—	0.2	1.0	%
Frequency Change with Temperature (T_A = T_{low} to T_{high})	$\Delta f_{osc}/\Delta T$	—	2.0	—	%
Clock Output Voltage High State Low State	 V_{OH} V_{OL}	 3.9 —	 4.5 2.3	 — 2.9	V
Sawtooth Peak Voltage	V_P	2.6	2.8	3.0	V
Sawtooth Valley Voltage	V_V	0.7	1.0	1.25	V

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34025 = – 40°C for MC33025 T_{high} = +70°C for MC34025 = +105°C for MC33025

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, R_T = 3.65 kΩ, C_T = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 2], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION					
Input Offset Voltage	V_{IO}	—	—	15	mV
Input Bias Current	I_{IB}	—	0.6	3.0	µA
Input Offset Current	I_{IO}	—	0.1	1.0	µA
Open-Loop Voltage Gain (V_O = 1.0 V to 4.0 V)	A_{VOL}	60	95	—	dB
Gain Bandwidth Product (T_J = 25°C)	GBW	4.0	8.3	—	MHz
Common Mode Rejection Ratio (V_{CM} = 1.5 V to 5.5 V)	CMRR	75	95	—	dB
Power Supply Rejection Ratio (V_{CC} = 10 V to 30 V)	PSRR	85	110	—	dB
Output Current, Source (V_O = 4.0 V) Sink (V_O = 1.0 V)	I_{Source} I_{Sink}	0.5 1.0	3.0 3.6	— —	mA
Output Voltage Swing, High State (I_O = – 0.5 mA) Low State (I_O = 1 mA)	V_{OH} V_{OL}	4.5 0	4.75 0.4	5.0 1.0	V
Slew Rate	SR	6.0	12	—	V/µs
PWM COMPARATOR SECTION					
Ramp Input Bias Current	I_{IB}	—	–0.5	–5.0	µA
Duty Cycle Maximum Minimum	 $DC_{(max)}$ $DC_{(min)}$	 80 —	 90 —	 — 0	%
Zero Duty Cycle Threshold Voltage Pin 3(4) (Pin 7(9) = 0 V)	V_{th}	1.1	1.25	1.4	V
Propagation Delay (Ramp Input to Output, T_J = 25°C)	$t_{PLH(in/out)}$	—	60	100	ns
SOFT-START SECTION					
Charge Current ($V_{Soft\text{-}Start}$ = 0.5 V)	I_{chg}	3.0	9.0	20	µA
Discharge Current ($V_{Soft\text{-}Start}$ = 1.5 V)	I_{dischg}	1.0	4.0	—	mA
CURRENT SENSE SECTION					
Input Bias Current (Pin 7(9) = 0 V to 4.0 V)	I_{IB}	—	—	15	µA
Current Limit Comparator Threshold Shutdown Comparator Threshold	V_{th} V_{th}	0.9 1.25	1.0 1.40	1.10 1.55	V
Propagation Delay (Current Limit/Shutdown to Output, T_J = 25°C)	$t_{PLH(in/out)}$	—	50	80	ns
OUTPUT SECTION					
Output Voltage, Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA) High State (I_{Source} = 20 mA) (I_{Source} = 200 mA)	V_{OL} V_{OH} 	— — 13 12	0.25 1.2 13.5 13	0.4 2.2 — —	V
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 0.5 mA)	$V_{OL(UVLO)}$	—	0.25	1.0	V
Output Leakage Current (V_C = 20 V)	I_L	—	100	500	µA
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	—	30	60	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	—	30	60	ns
UNDERVOLTAGE LOCKOUT SECTION					
Start-Up Threshold (V_{CC} Increasing)	$V_{th(on)}$	8.8	9.2	9.6	V
UVLO Hysteresis	V_H	0.4	0.8	1.2	V
TOTAL DEVICE					
Power Supply Current Start-Up Operating	I_{CC}	 — —	 0.5 25	 0.8 35	mA

3

Figure 1. Timing Resistor versus Oscillator Frequency

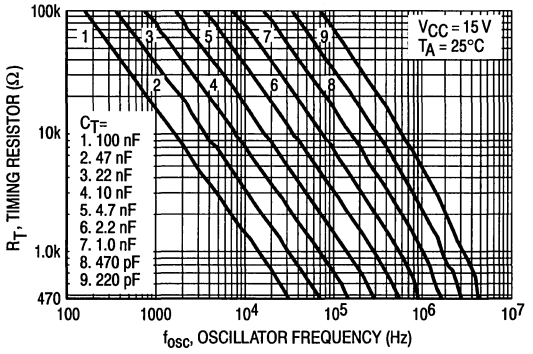


Figure 2. Oscillator Frequency versus Temperature

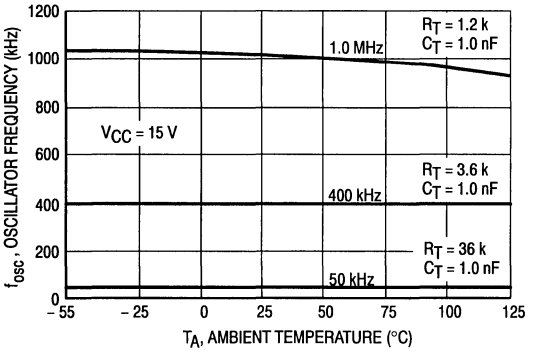


Figure 3. Error Amp Open-Loop Gain and Phase versus Frequency

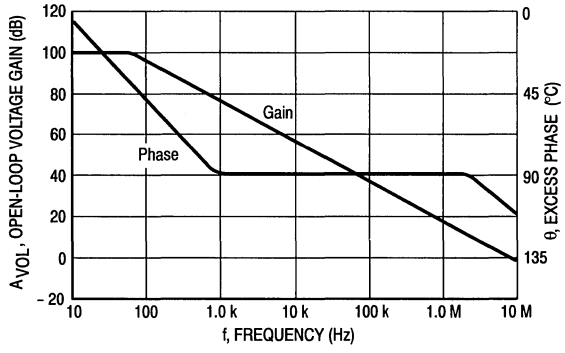


Figure 4. PWM Comparator Zero Duty Cycle Threshold Voltage versus Temperature

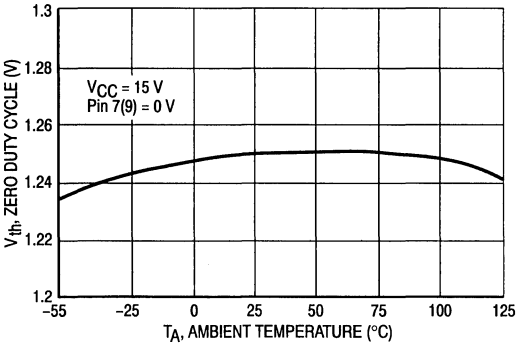


Figure 5. Error Amp Small Signal Transient Response

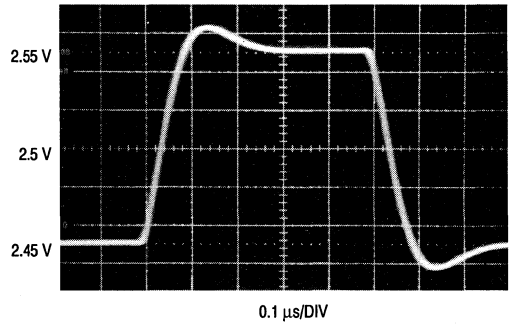


Figure 6. Error Amp Large Signal Transient Response

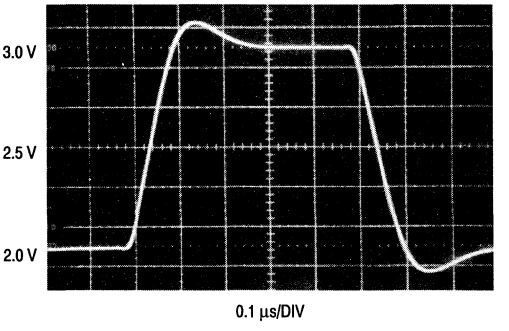


Figure 7. Reference Voltage Change versus Source Current

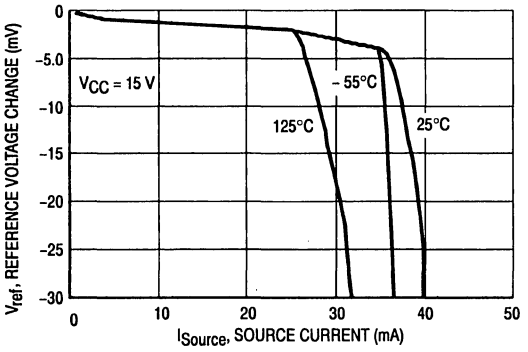


Figure 8. Reference Short Circuit Current versus Temperature

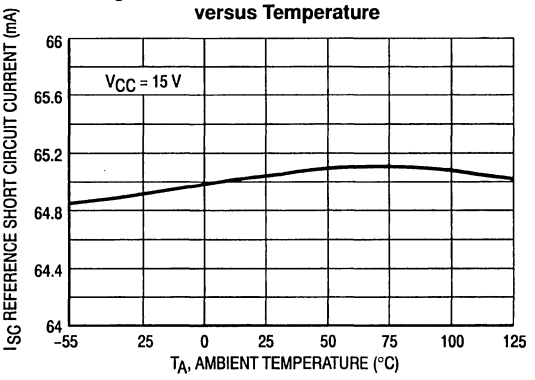


Figure 9. Reference Line Regulation

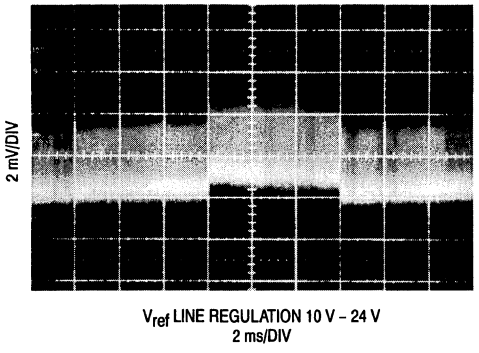


Figure 10. Reference Load Regulation

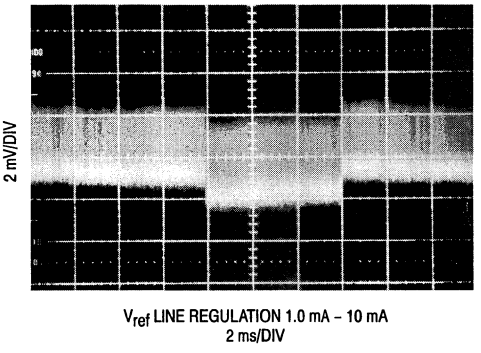


Figure 11. Current Limit Comparator Threshold versus Temperature

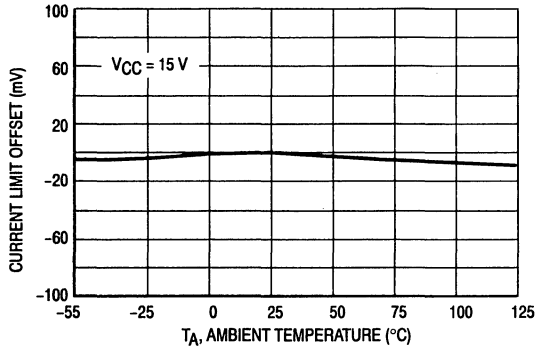


Figure 12. Shutdown Comparator Threshold versus Temperature

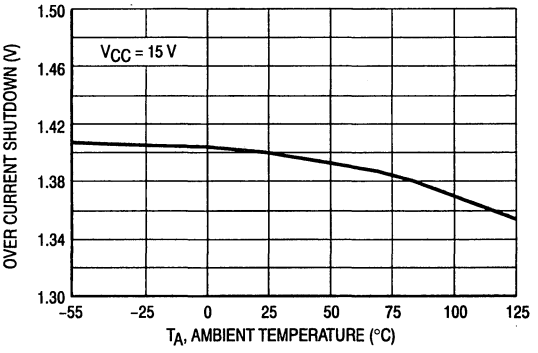


Figure 13. Soft-Start Charge Current versus Temperature

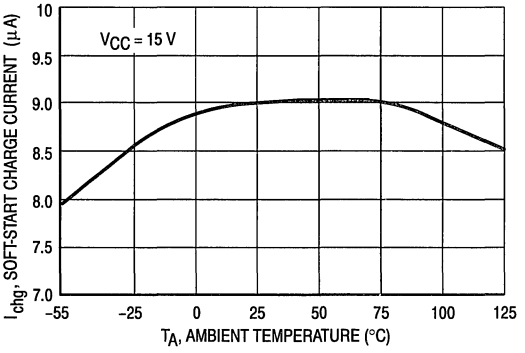


Figure 14. Output Saturation Voltage versus Load Current

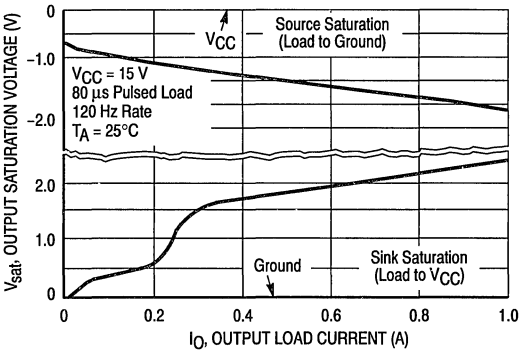
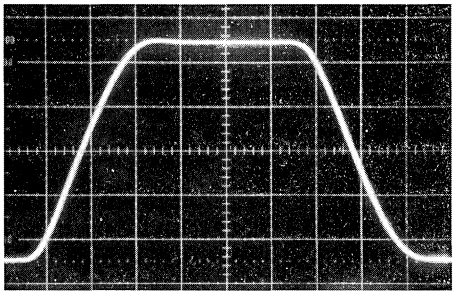
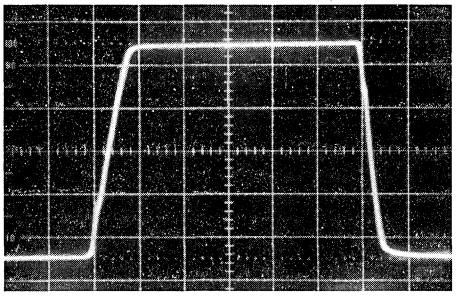


Figure 15. Drive Output Rise and Fall Time



OUTPUT RISE & FALL TIME 1.0 nF LOAD
50 ns/DIV

Figure 16. Drive Output Rise and Fall Time



OUTPUT RISE & FALL TIME 10.0 nF LOAD
50 ns/DIV

Figure 17. Supply Voltage versus Supply Current

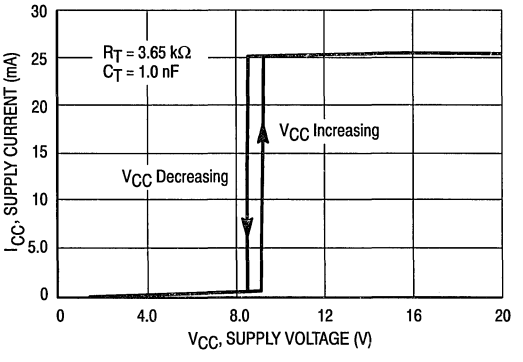
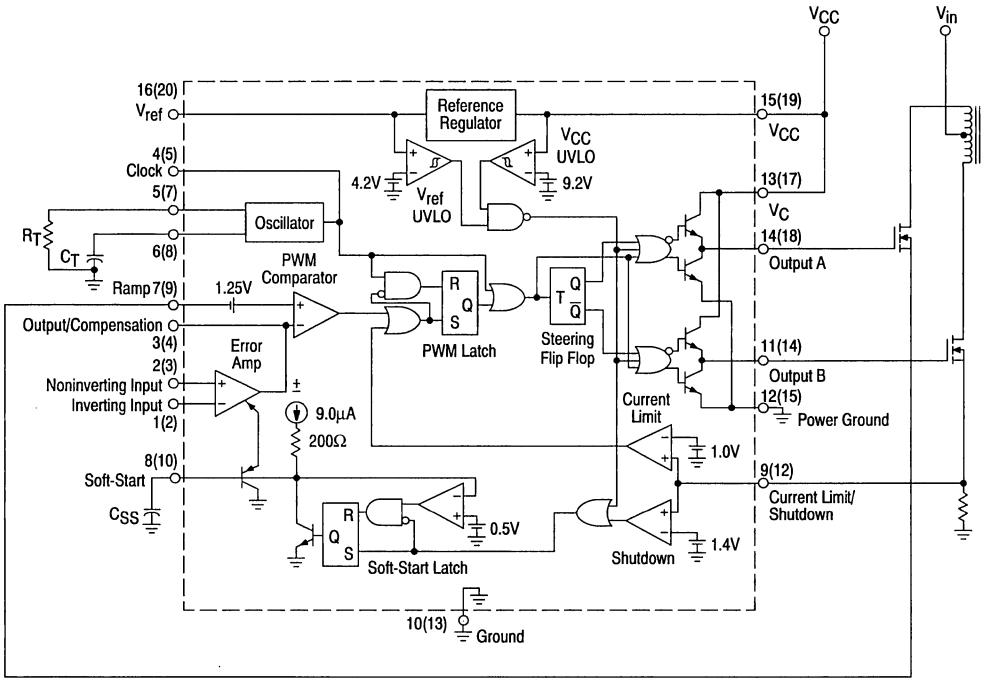
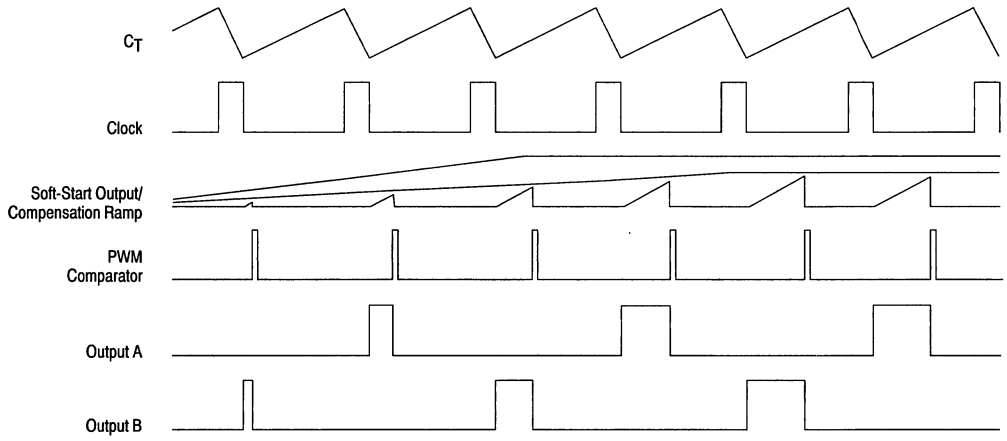


Figure 18. Representative Block Diagram



Pin numbers in parenthesis ( ) are for FN suffix, PLCC package.

Figure 19. Current Limit Operating Waveforms



OPERATING DESCRIPTION

The MC33025 and MC34025 series are high speed, fixed frequency, double-ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 18.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. The R_T pin is set to a temperature compensated 3.0 V. By selecting the value of R_T, the charge current is set through a current mirror for the timing component (C_T). This charge current runs continuously through C_T. The discharge current is ratioed to be 10 times the charge current, which yields the maximum duty cycle of 90%. C_T is charged to 2.8 V and discharged to 1.0 V. During the discharge of C_T, the oscillator generates an internal blanking pulse that resets the PWM Latch, inhibits the outputs, and toggles the steering flip-flop. The threshold voltages on the oscillator comparator is trimmed to guarantee an oscillator accuracy of 5.0% at 25°C.

Additional dead time can be added by externally increasing the charge current to C_T. This changes the charge to discharge ratio of C_T which is set internally to $I_{charge}/10$ I_{charge}. The new charge to discharge ratio will be:

$$\% \text{ Deadtime} = \frac{I_{additional} + I_{charge}}{10\ (I_{charge})}$$

A bidirectional clock pin is provided for synchronization or for master/slave operation. When synchronizing the MC34025 to an external clock source, the oscillator should be set about 10% less than the external clock frequency. If master/slave operation of more than one MC34025 is desired, the master IC should have the desired R_T, C_T values. The Clock pin of the master is connected to the Clock pin on the slave(s). The R_T pin on the slave(s) should be connected to V_{ref} and the C_T pin should be connected to ground. If the master IC is not close to the slave IC(s), the Clock pin should be buffered. Refer to Figures 23, 24, 29, and 30 for some application hints.

Error Amplifier

A fully compensated Error Amplifier is provided. It features a typical DC voltage gain of 95 dB and a unity gain bandwidth of 5.5 MHz with 75 degrees of phase margin (Figure 3). Typical application circuits will have the noninverting input tied to the reference. The inverting input will typically be connected to a feedback voltage generated from the output of the switching power supply. The Error Amplifier Output is provided for external loop compensation.

Soft-Start Latch

Soft-Start is accomplished in conjunction with an external capacitor. The soft start capacitor is charged by an internal 9.0 μA current source. This capacitor clamps the output of the error amplifier to less than its normal output voltage, thus limiting the duty cycle.

The time it takes for a capacitor to reach full charge is given by:

$$t \approx (4.5 \bullet 10^5) C_{Soft\text{-}Start}$$

A Soft-Start latch is incorporated to prevent erratic operation of this circuitry. Two conditions can cause the Soft-Start circuit to latch so that the Soft-Start capacitor stays discharged. The first condition is activation of an undervoltage lockout of either V_{CC} or V_{ref}. The second condition is when current sense input exceeds 1.4 V. Since this latch is "set dominant", it cannot be reset until either of these signals is removed, and the voltage at $C_{Soft\text{-}Start}$ is less than 1.0 V.

PWM Comparator and Latch

A PWM circuit typically compares an error voltage with a ramp signal. The outcome of this comparison determines the state of the output. In voltage mode operation the ramp signal is the voltage ramp of the timing capacitor. In current mode operation the ramp signal is the voltage ramp induced in a current sensing element. The ramp input of the PWM comparator is pinned out so that the user can decide which mode of operation best suits the application requirements. The ramp input has a 1.25 V offset such that whenever the voltage at this pin exceeds the Error Amplifier Output voltage minus 1.25 V, the PWM comparator will cause the PWM latch to set, disabling the outputs. Once the PWM latch is set, only a blanking pulse by the oscillator can reset it, thus initiating the next cycle.

A toggle flip flop connected to the output of the PWM latch controls which output is active. The flip flop is pulsed by an OR gate that gets its inputs from the oscillator clock and the output of the PWM latch. A pulse from either one will cause the flip flop to enable the other output.

Current Limiting and Shutdown

A pin is provided to perform current limiting and shutdown operations. Two comparators are connected to the input of this pin. When the voltage at this pin exceeds 1.0 V, one of the comparators is activated. The output of this comparator sets the PWM latch, which disables the output. In this way cycle-by-cycle current limiting is accomplished. If a current limit resistor is used in series with the power devices, the value of the resistor is found by:

$$R_{Sense} = \frac{1.0\ V}{I_{pk(switch)}}$$

If the voltage at this pin exceeds 1.4 V, the second comparator is activated. This comparator sets a latch which, in turn, causes the Soft-Start capacitor to be discharged. In this way a "hiccup" mode of recovery is possible in the case of output short circuits. If a current limit resistor is used in series with the output devices, the peak current at which the controller will enter a "hiccup" mode is given by:

$$I_{shutdown} = \frac{1.4\ V}{R_{Sense}}$$

Undervoltage Lockout

There are two undervoltage lockout circuits within the IC. The first senses V_{CC} and the second V_{ref}. During power-up, V_{CC} must exceed 9.2 V and V_{ref} must exceed 4.0 V before the outputs can be enabled and the Soft-Start latch released. If V_{CC} falls below 8.4 V or V_{ref} falls below 3.6 V, the outputs are disabled and the Soft-Start latch is activated. When the UVLO is active, the part is in a low current standby mode allowing the IC to have an off-line bootstrap start-up circuit. Typical start-up current is 400 μA.

Output

The MC34025 has two high current totem pole outputs specifically designed for direct drive of power MOSFETs. They are capable of up to ±2.0 A peak drive current with a typical rise and fall time of 30 ns driving a 1.0 nF load.

Separate pins for V_C and Power Ground are provided. With proper implementation, a significant reduction of switching transient noise imposed on the control circuitry is possible. The separate V_C supply input also allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}.

Reference

A 5.1 V bandgap reference is pinned out and is trimmed to an initial accuracy of ±1.0% at 25°C. This reference has short circuit protection and can source in excess of 10 mA for powering additional control system circuitry.

Design Considerations

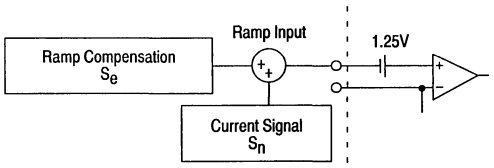
Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. With high frequency, high power, switching power supplies it is imperative to have separate current loops for the signal paths and for the power paths. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. All bypass capacitors and snubbers should be connected as close as possible to the specific part in question. The PC board lead lengths must be less than 0.5 inches for effective bypassing or snubbing.

Instabilities

In current mode control, an instability can be encountered at any given duty cycle. The instability is caused by the current feedback loop. It has been shown that the instability is caused by a double pole at half the switching frequency. If an external ramp (S_e) is added to the on-time ramp (S_n) of the current-sense waveform, stability can be achieved (see Figure 20).

One must be careful not to add too much ramp compensation. If too much is added, the system will start to perform like a voltage mode regulator. All benefits of current mode control will be lost. Figure 26 shows examples of two different ways in which external ramp compensation can be implemented.

Figure 20. Ramp Compensation



A simple equation can be used to calculate the amount of external ramp necessary to add that will achieve stability in the current loop. For the following equations, the calculated values for the application circuit in Figure 36 are also shown.

$$S_e = \frac{V_{sec}(\partial(max) - 0.18)A_i}{L}$$

where: V_{sec} = minimum voltage at the input of the output inductor
$\partial(max)$ = maximum duty cycle
A_i = gain of the current sense network (see Figures 25, 26, and 27)
L = output inductor

For the application circuit $S_e = \frac{7(0.8 - 0.18)0.075}{1.8\,\mu} = 18 \bullet 10^4$

As a sanity check, the modulator gain of the circuit can be calculated by:

$$m_{c1} = 1 + S_e/S_n$$

$$S_n = \frac{di}{dt} A_i$$

where: di = output inductor slope
dt = maximum on time
A_i = gain of the current sense network (see Figures 25, 26, 27).

For the application circuit:

$$S_n = \frac{3.0}{0.8 \bullet 10^6}\ 0.075 = 22.5 \bullet 10^4$$

$$m_{c1} = 1 + \frac{18 \bullet 10^4}{22.5 \bullet 10^4} = 1.8$$

This can be compared against the maximum modulator gain necessary to make the system immune to audio susceptibility tests:

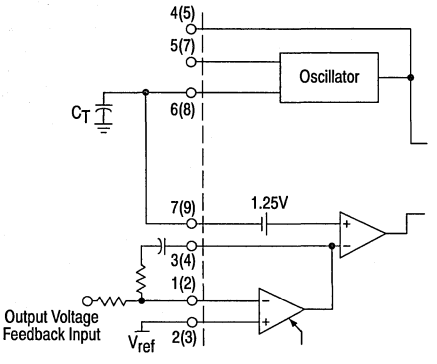
$$m_{c2} = \frac{2 - \partial}{2\partial'}, \text{ where: } \partial = \text{max duty cycle}, \quad \partial' = \text{1–max duty cycle}$$

For the application circuit: $m_{c2} = \frac{2 - 0.8}{2(0.2)} = 3$, m_{c2} should be larger than m_{c1}.

PIN FUNCTION DESCRIPTION

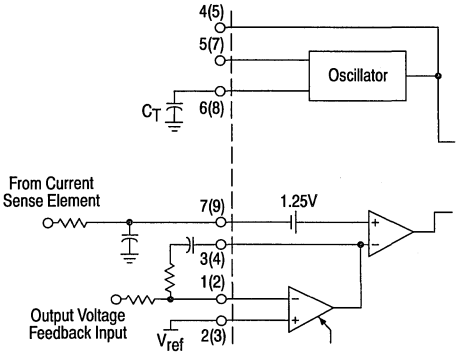
Pin		Function	Description
DIP/SOIC	PLCC		
1	2	Error Amp Inverting Input	This pin is usually used for feedback from the output of the power supply.
2	3	Error Amp Noninverting Input	This pin is used to provide a reference in which an error signal can be produced on the output of the error amp. Usually this is connected to V_{ref}, however an external reference can also be used.
3	4	Error Amp Output	This pin is provided for compensating the error amp for poles and zeros encountered in the power supply system, mostly the output LC filter.
4	5	Clock	This is a bidirectional pin used for synchronization.
5	7	R_T	The value of R_T sets the charge current through timing Capacitor, C_T.
6	8	C_T	In conjunction with R_T, the timing Capacitor sets the switching frequency. Because this part is a push-pull output, each output runs at one-half the frequency set at this pin.
7	9	Ramp Input	For voltage mode operation this pin is connected to C_T. For current mode operation this pin is connected through a filter to the current sensing element.
8	10	Soft-Start	A capacitor at this pin sets the Soft-Start time.
9	12	Current Limit/Shutdown	This pin has two functions. First, it provides cycle-by-cycle current limiting. Second, if the current is excessive, this pin will reinitiate a Soft-Start cycle.
10	13	Ground	This pin is the ground for the control circuitry.
11	14	Output A	This is a high current dual totem pole output.
12	15	Power Ground	This is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
13	17	V_C	This is a separate power source connection for the outputs that is connected back to the power source input. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
14	18	Output B	This is a high current dual totem pole output.
15	19	V_{CC}	This pin is the positive supply of the control IC.
16	20	V_{ref}	This is a 5.0 V reference. It is usually connected to the noninverting input of the error amplifier.

Figure 21. Voltage Mode Operation



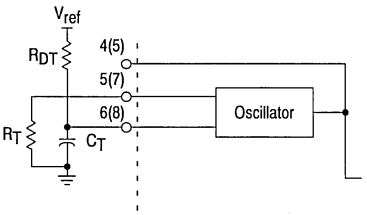
In voltage mode operation, the control range on the output of the Error Amplifier from 0% to 90% duty cycle is from 2.25 V to 4.05 V.

Figure 22. Current Mode Operation



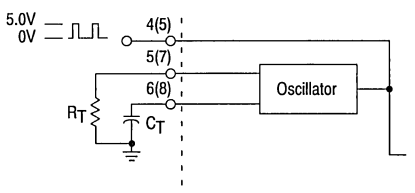
In current mode control, an RC filter should be placed at the ramp input to filter the leading edge spike caused by turn-on of a power MOSFET.

Figure 23. Dead Time Addition



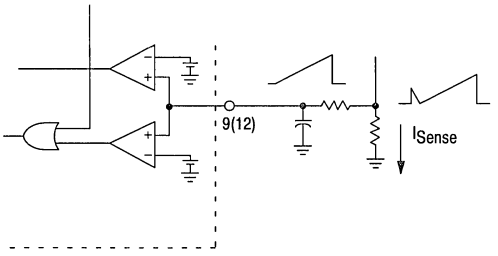
Additional dead time can be added by the addition of a dead time resistor from V_{ref} to C_T. See text on oscillator section for more information.

Figure 24. External Clock Synchronization



The sync pulse fed into the clock pin must be at least 3.9 V. R_T and C_T need to be set 10% slower than the sync frequency. This circuit is also used in voltage mode operation for master/slave operation. The clock signal would be coming from the master which is set at the desired operating frequency, while the slave is set 10% slower.

Figure 25. Resistive Current Sensing



The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. If a transformer is used, the gain can be calculated by:

$$A_i = \frac{R_{Sense}}{\text{turns ratio}}$$

Figure 26. Primary Side Current Sensing

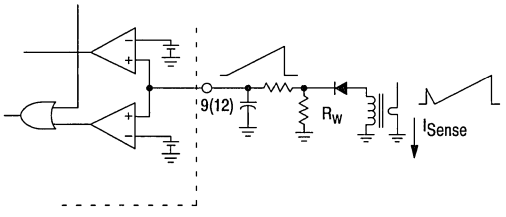
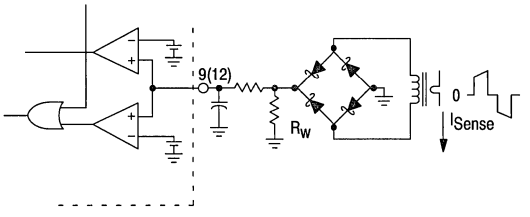


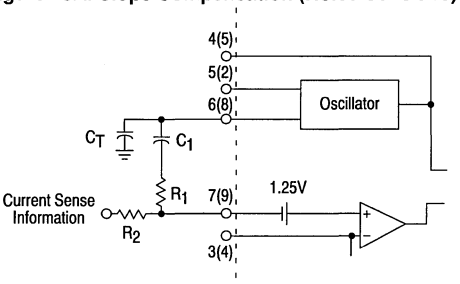
Figure 27. Primary or Secondary Side Current Sensing



The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. The gain can be calculated by:

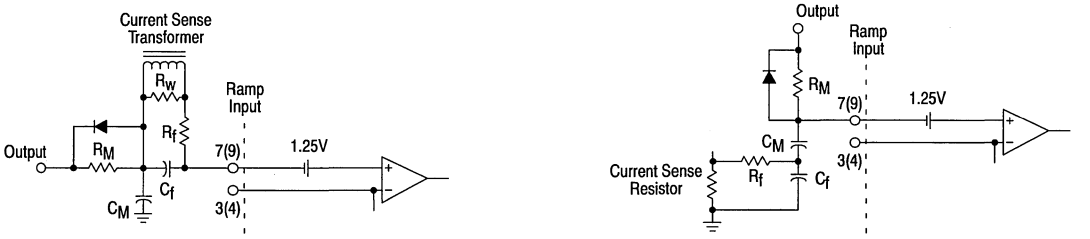
$$A_i = \frac{R_W}{\text{turns ratio}}$$

Figure 28A. Slope Compensation (Noise Sensitive)



This method of slope compensation is easy to implement, however, it is noise sensitive. Capacitor C_1 provides AC coupling. The oscillator signal is added to the current signal by a voltage divider consisting of resistors R_1 and R_2.

Figure 28B. Slope Compensation (Noise Immune)



When only one output, this method of slope compensation can be used and it is relatively noise immune. Resistor R_M and capacitor C_M provide the added slope necessary. By choosing R_M and C_M with a larger time constant than the switching frequency, you can assume that its charge is linear. First choose C_M, then R_M can be adjusted to achieve the required slope. The diode provides a reset pulse the ramp inputs at the end of every cycle. The charge current I_M can be calculated by $I_M = C_M S_e$. Then R_M can be calculated by $R_M = V_{CC}/I_M$

Figure 29. Master/Slave Operation Over Short Distances

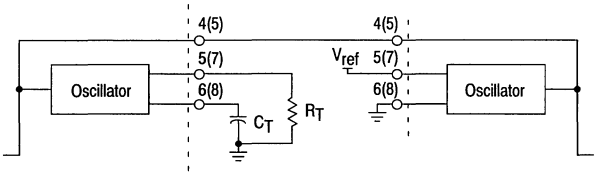


Figure 30. Master/Slave Operation Over Long Distances

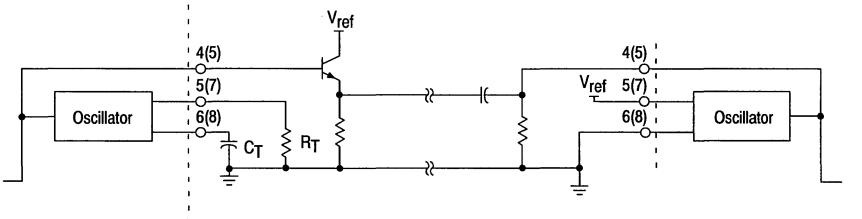
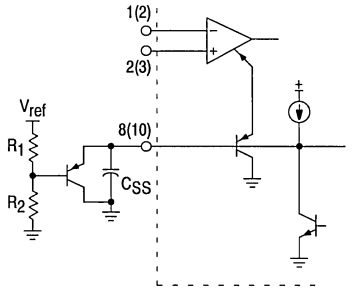


Figure 31. Buffered Maximum Clamp Level

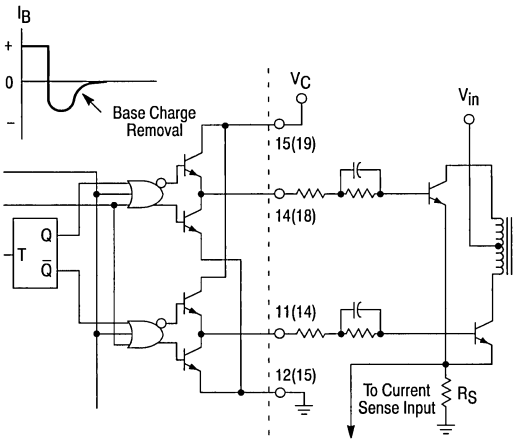


In voltage mode operation, the maximum duty cycle can be clamped. By the addition of a PNP transistor to buffer the clamp voltage, the Soft-Start current is not affected by R_1.

The new equation for Soft-Start is $t \approx \frac{V_{clamp} + 0.6}{9.0\ \mu A} (C_{SS})$

In current mode operation, this circuit will limit the maximum voltage allowed at the ramp input to end a cycle.

Figure 32. Bipolar Transistor Drive



The totem pole output can furnish negative base current for enhanced transistor turn-off, with the addition of the capacitor in series with the base.

Figure 33. Isolated MOSFET Drive

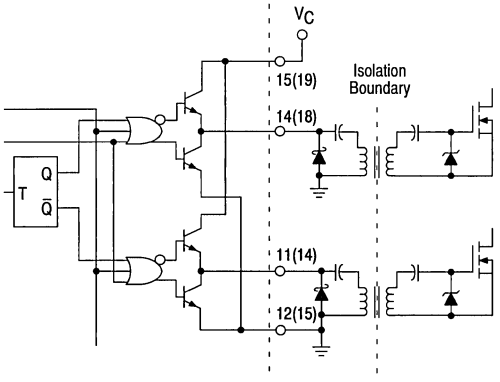
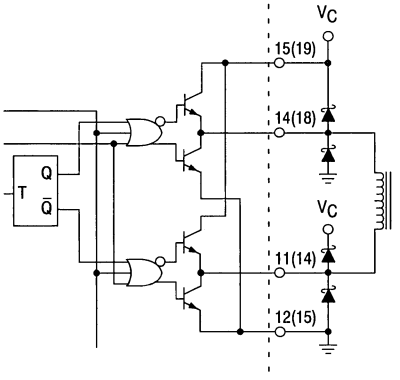
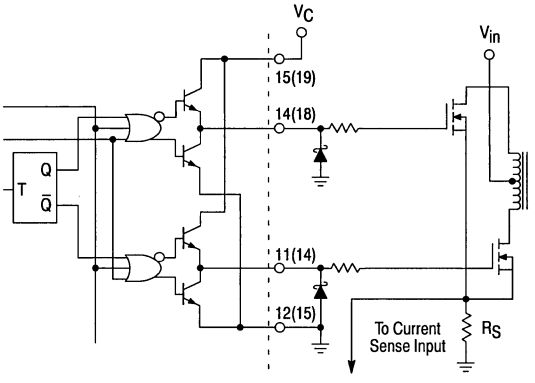


Figure 34. Direct Transformer Drive



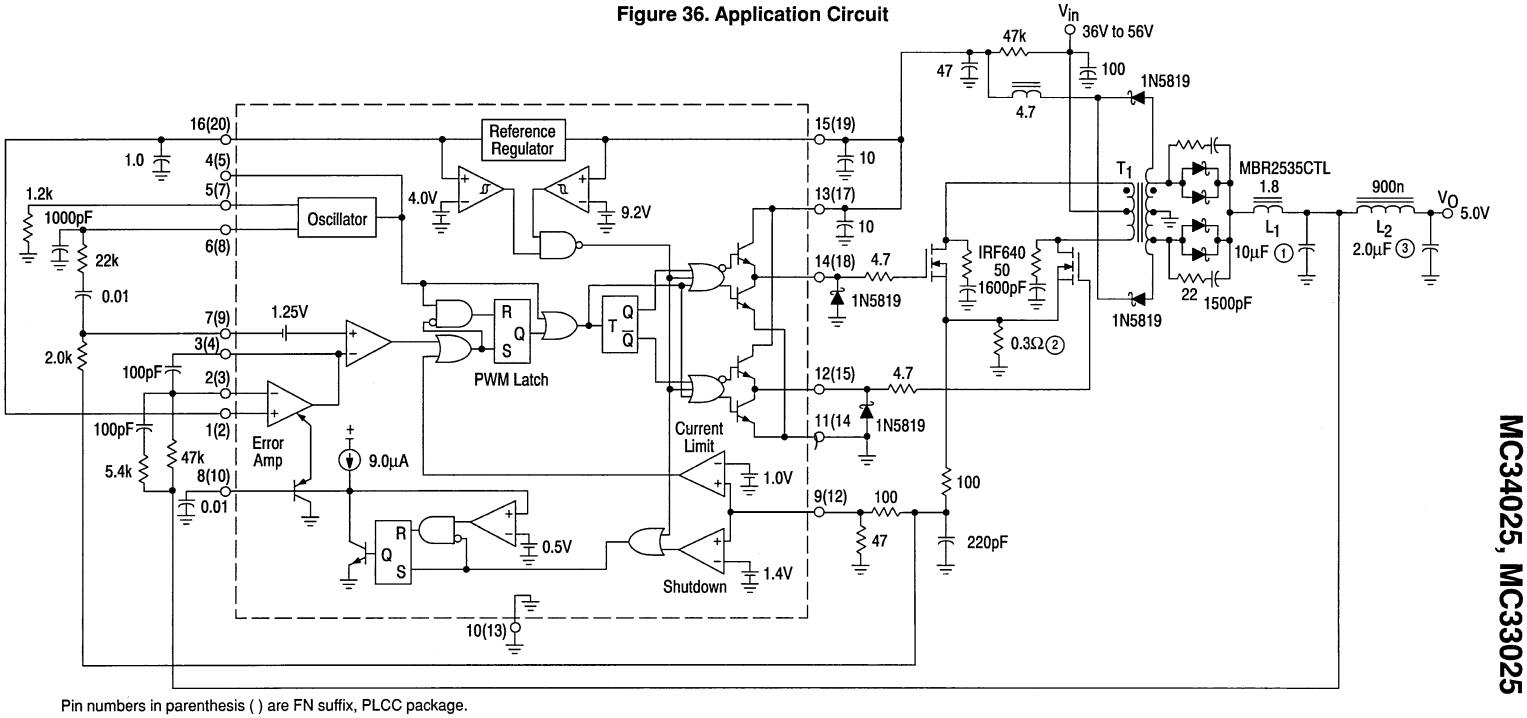
The totem pole output can easily drive pulse transformers. A Schottky diode is recommended when driving inductive loads at high frequencies. The diode can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 35. MOSFET Parasitic Oscillations



A series gate resistor may be needed to damp high frequency parasitic oscillation caused by a MOSFET's input capacitance and any series wiring inductance in the gate-source circuit. The series resistor will also decrease the MOSFET's switching speed. A Schottky diode can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground. The Schottky diode also prevents substrate injection when the output pin is driven below ground.

Figure 36. Application Circuit



Pin numbers in parenthesis ( ) are FN suffix, PLCC package.

T_1 — Primary16 turns #48 AWG (1300 strands litz wire)
Secondary: 4 turns center tapped 0.003″ (2 layers) copper foil
Bootstrap: 1 turn added to each secondary output #36 AWG
Core: Philips 3F3 part #4312 020 4124
Bobbin Philips part #4322 021 3525
Coilcraft P3269-A

L_1 — 2 turns #48 AWG (1300 strands litz wire)
Core: Philips 3F3 part #EP10-3F3
Bobbin: Philips part #EP10PCB1-8
L = 1.8 µH
Coilcraft P3270-A

L_2 — 7 turns #18 AWG, 1/2″ diameter air core
Coilcraft P3271-A

Heatsinks — Power FET: AAVID Heatsink #533902B02554 with clip
Output Recitfiers: AAVID Heatsink #533402B02552 with clip

Insulators — All power devices are insulated with Berquist Sil-Pad 1500

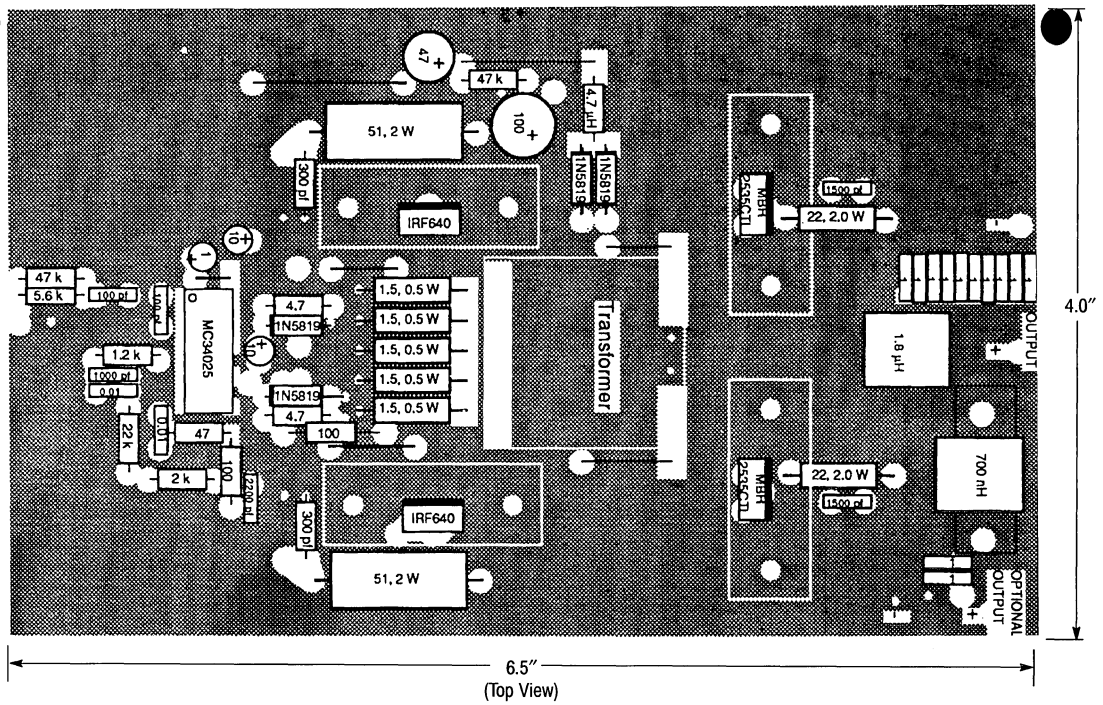
① — 10 (1.0 µF) ceramic capacitors in parallel

② — 5 (1.5 Ω) resistors in parallel

③ — 2(1.0 µF) ceramic capacitors in parallel

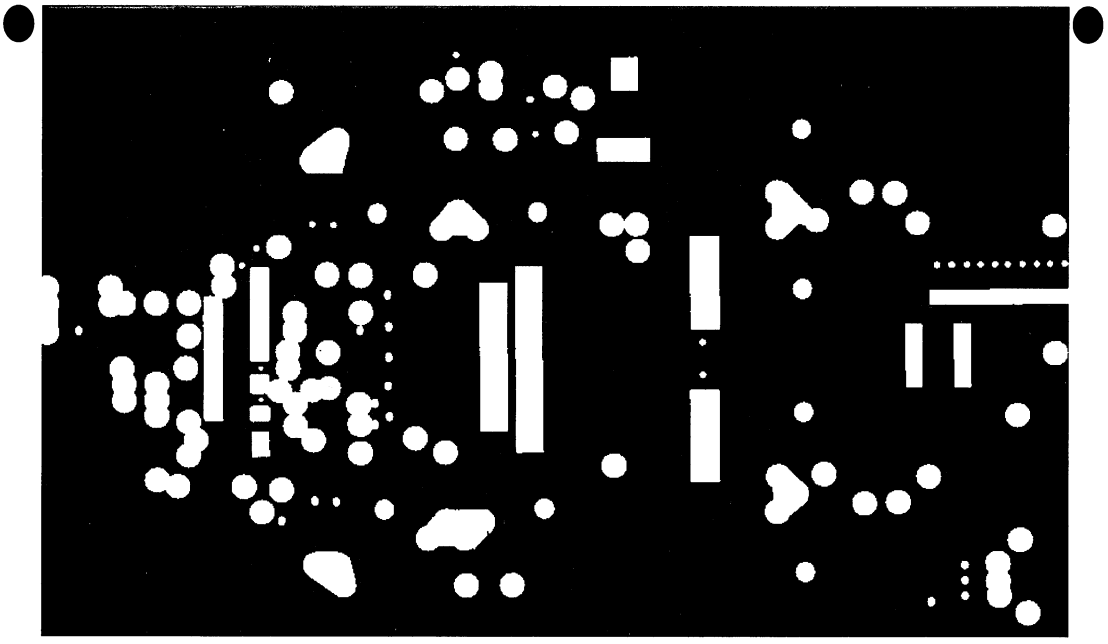
Test	Condition	Results
Line Regulation	V_{in} = 40 V to 56 V, I_O = 15 A	14 mV = ± 0.275%
Load Regulation	V_{in} = 48 V, I_O = 8.0 V to 15 A	54 mV = ± 1.0%
Output Ripple	V_{in} = 48 V, I_O = 15 A	50 mVp-p
Efficiency	V_{in} = 48 V, I_O = 15 A	71.2%

Figure 37. PC Board With Components

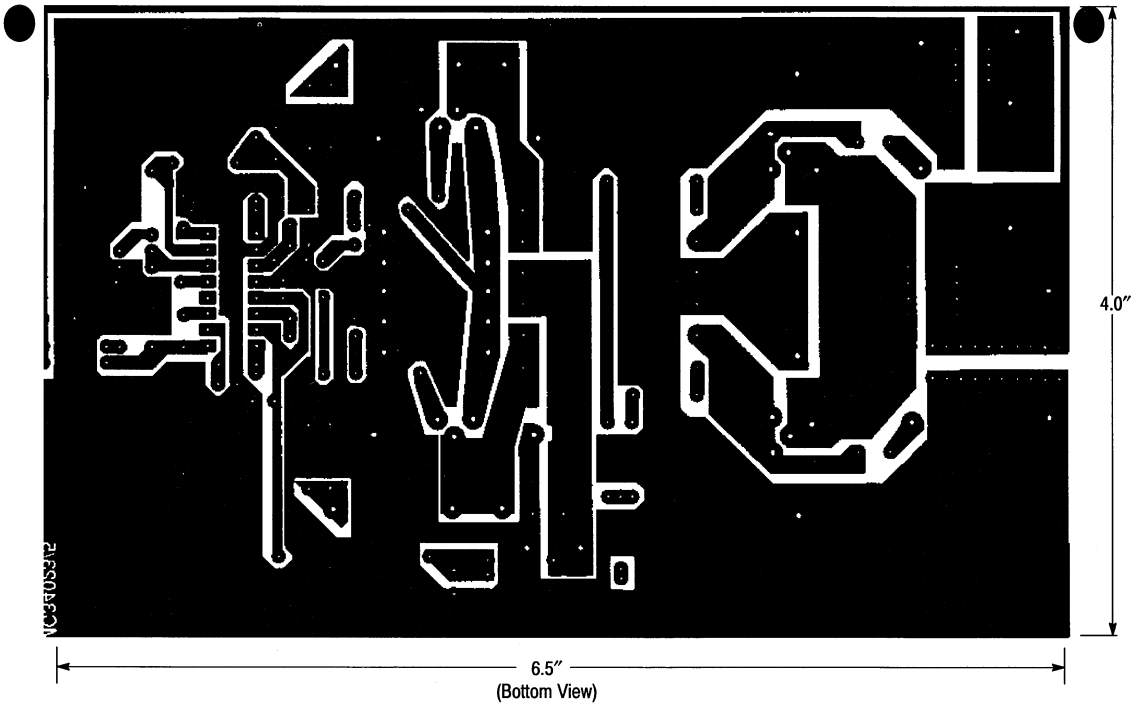


(Top View)

Figure 38. PC Board Without Components



(Top View)



(Bottom View)

MC34060

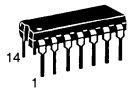
Switchmode Pulse Width Modulation Control Circuit

SWITCHMODE
PULSE WIDTH MODULATION
CONTROL CIRCUIT

SILICON MONOLITHIC
INTEGRATED CIRCUIT

The MC34060 is a low cost fixed frequency, pulse width modulation control circuit designed primarily for single ended SWITCHMODE power supply control. This device features:

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 V Reference
- Adjustable Dead Time Control
- Uncommitted Output Transistor for 200 mA Source or Sink



P SUFFIX
PLASTIC PACKAGE
CASE 646

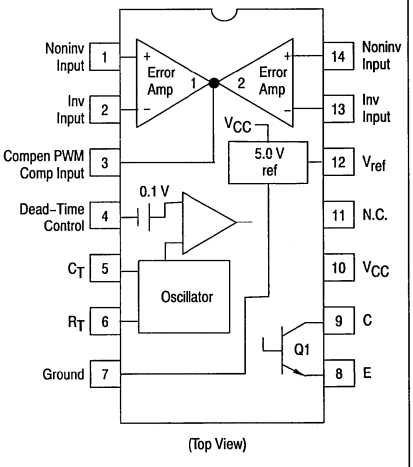
MAXIMUM RATINGS (Full operating ambient temperature range applies.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	42	V
Collector Output Voltage	V_C	42	V
Collector Output Current	I_C	250	mA
Amplifier Input Voltage	V_{in}	V_{CC} +0.3	V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000	mW
Operating Junction Temperature	T_J	125	°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	–55 to 125	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	80	°C/W
Power Derating Factor	$1/R_{\theta JA}$	12.5	mW/°C
Derating Ambient Temperature	T_A	45	°C

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34060P	0° to +70°C	Plastic DIP

RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_C	—	30	40	V
Collector Output Current	I_C	—	—	200	mA
Amplifier Input Voltage	V_{in}	–0.3	—	V_{CC} –2	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	47	500	kΩ
Timing Capacitor	C_T	0.00047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	25	200	kHz

ELECTRICAL CHARACTERISTICS V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ, unless otherwise noted.
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies.

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage (I_O = 1.0 mA)	V_{ref}	4.75	5.0	5.25	V
Input Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	—	2.0	25	mV
Output Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	3.0	15	mV
Short Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	mA
OUTPUT SECTION					
Collector Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	—	2.0	100	μA
Emitter Off-State Current (V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	—	—	–100	μA
Collector-Emitter Saturation Voltage					V
Common-Emitter (V_E = 0 V, I_C = 200 mA)	$V_{sat(C)}$	—	1.1	1.3	
Emitter-Follower (V_C = 15 V, I_E = –200 mA)	$V_{sat(E)}$	—	1.5	2.5	
Output Voltage Rise Time (T_A = 25°C)	t_r				ns
Common-Emitter (See Figure 12)		—	100	200	
Emitter-Follower (See Figure 13)		—	100	200	
Output Voltage Fall Time (T_A = 25°C)	t_f				ns
Common-Emitter (See Figure 12)		—	25	100	
Emitter-Follower (See Figure 13)		—	40	100	

ELECTRICAL CHARACTERISTICS V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted.
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies.

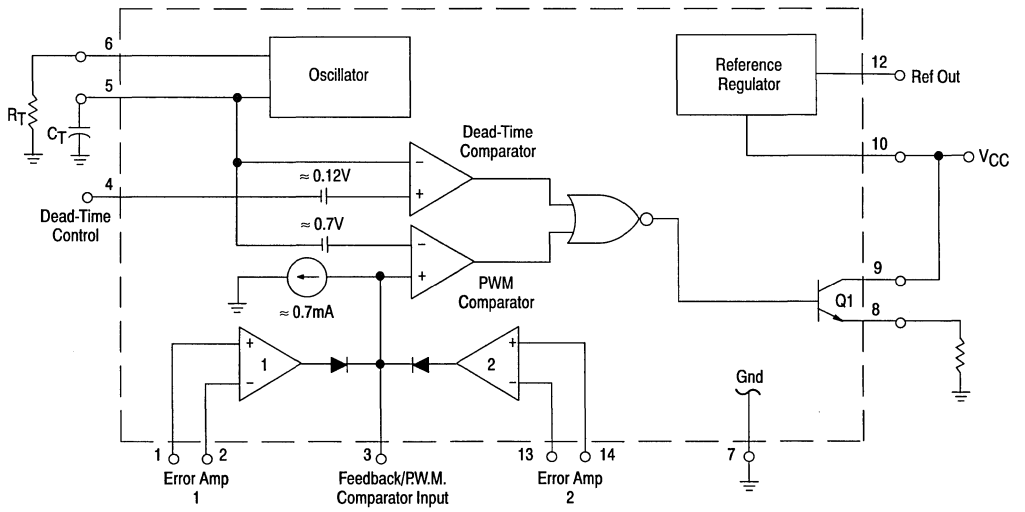
Characteristics	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTIONS					
Input Offset Voltage ($V_{O[Pin\ 3]}$ = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current ($V_{C[Pin\ 3]}$ = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias Current ($V_{O[Pin\ 3]}$ = 2.5 V)	I_{IB}	—	–0.1	–1.0	µA
Input Common Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)	V_{ICR}	–0.3 to V_{CC} –2.0	—	—	V
Open-Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	—	dB
Unity-Gain Crossover Frequency (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	f_c	—	350	—	kHz
Phase Margin at Unity-Gain (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	—	65	—	deg.
Common Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90	—	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	—	100	—	dB
Output Sink Current ($V_{O[Pin\ 3]}$ = 0.7 V)	I_{O-}	0.3	0.7	—	mA
Output Source Current ($V_{O[Pin\ 3]}$ = 3.5 V)	I_{O+}	–2.0	–4.0	—	mA
PWM COMPARATOR SECTION (Test circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	—	3.5	4.5	V
Input Sink Current ($V_{[Pin\ 3]}$ = 0.7 V)	I_{I-}	0.3	0.7	—	mA
OSCILLATOR SECTION					
Frequency (C_T = 0.001 µF, R_T = 47 kΩ)	f_{osc}	—	25	—	kHz
Frequency Deviation of Frequency* (C_T = 0.001 µF, R_T = 47 kΩ)	σf_{osc}	—	3.0	—	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	$\Delta f_{osc}(\Delta V)$	—	0.1	—	%
Frequency Change with Temperature ($\Delta T_A = T_{low}$ to T_{high}) (C_T = 0.01 µF, R_T = 12 kΩ)	$\Delta f_{osc}(\Delta T)$	— —	— —	12 —	%

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula; $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \bar{x})^2}{N-1}}$

ELECTRICAL CHARACTERISTICS V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies.

Characteristics	Symbol	Min	Typ	Max	Unit
DEAD-TIME CONTROL SECTION (Test circuit Figure 11)					
Input Bias Current (Pin 4) (V_{in} = 0 V to 5.25 V)	$I_{IB(DT)}$	—	–2.0	–10	µA
Maximum Output Duty Cycle (V_{in} = 0 V, C_T = 0.01 µF, R_T = 12 kΩ) (V_{in} = 0 V, C_T = 0.001 µF, R_T = 47 kΩ)	DC_{max}	 90 —	 96 92	 100 100	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	 — 0	 2.8 —	 3.3 —	V
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, all other inputs and outputs open) (V_{CC} = 15 V) (V_{CC} = 40 V)	I_{CC}	 — —	 5.5 7.0	 10 15	mA
Average Supply Current ($V_{[Pin\ 4]}$ = 2.0 V, C_T = 0.001, R_T = 47 kΩ). See Figure 11.	I_S	—	7.0	—	mA

Figure 1. Block Diagram



Description

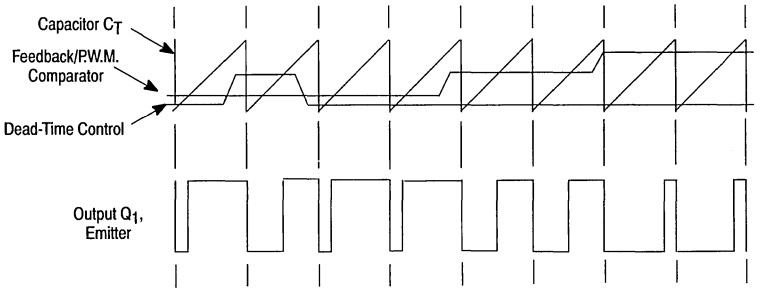
The MC34060 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply (see Figure 1). An internal-linear sawtooth oscillator is frequency- programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \cong \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The output is enabled only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

Figure 2. Timing Diagram



APPLICATIONS INFORMATION

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feed-back input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle of 96%. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 V to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common mode input range from –0.3 V to (V_{CC} –2 V), and may be used to sense power supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the noninverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

The MC34060 has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an internal accuracy of ±5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to +70°C.

Figure 3. Oscillator Frequency versus Timing Resistance

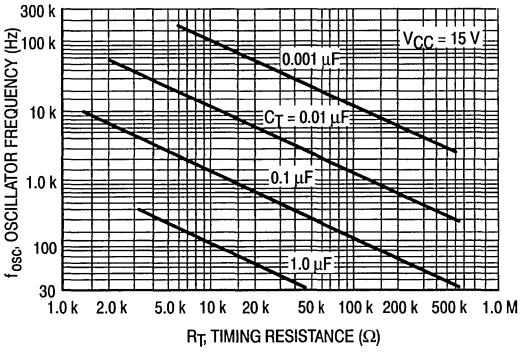


Figure 4. Open-Loop Voltage Gain and Phase versus Frequency

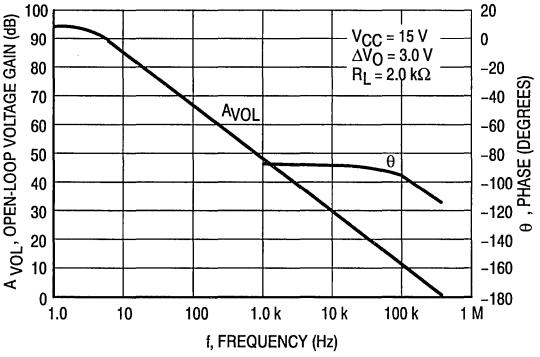


Figure 5. Percent Dead-Time versus Oscillator Frequency

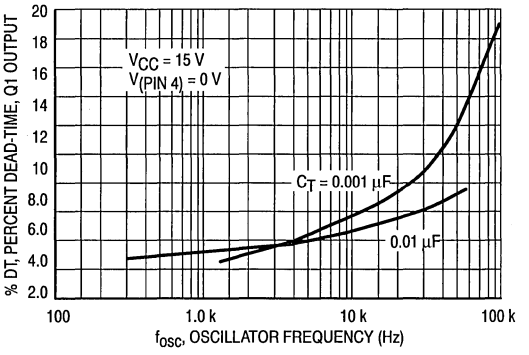


Figure 6. Percent Duty Cycle versus Dead-Time Control Voltage

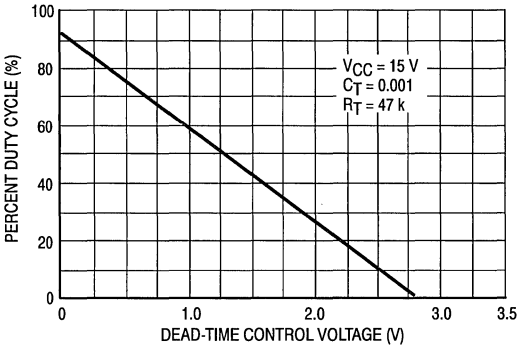


Figure 7. Emitter-Follower Configuration Output-Saturation Voltage versus Emitter Current

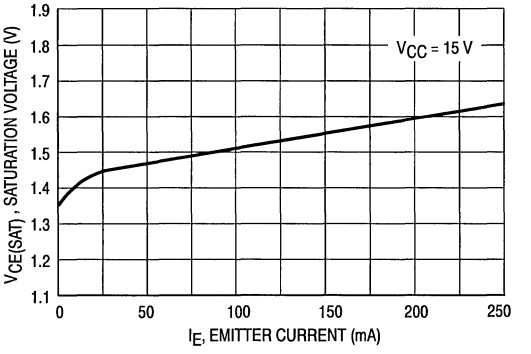


Figure 8. Common-Emitter Configuration Output-Saturation Voltage versus Collector Current

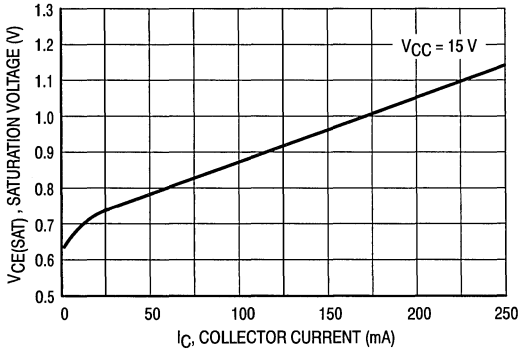


Figure 9. Standby-Supply Current versus Supply Voltage

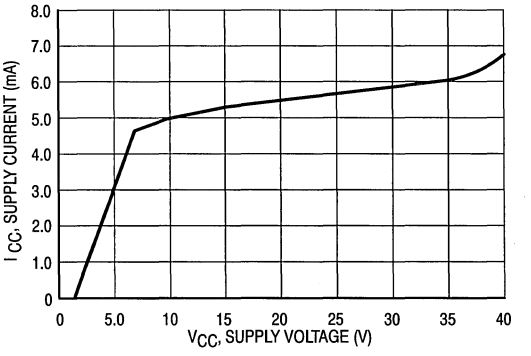


Figure 10. Error Amplifier Characteristics

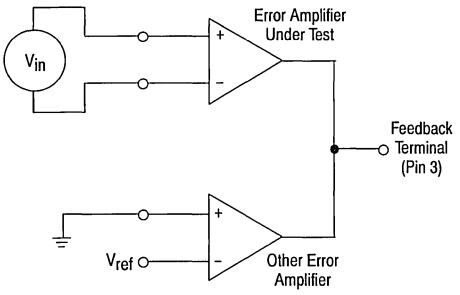


Figure 11. Dead-Time and Feedback Control

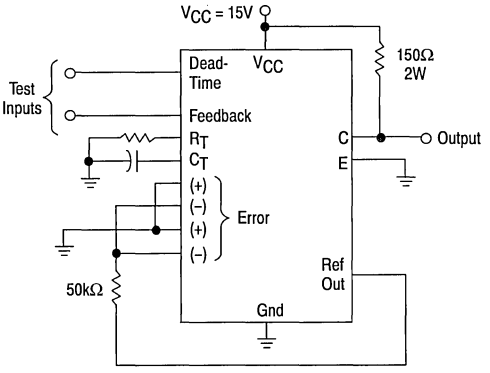


Figure 12. Common-Emitter Configuration and Waveform

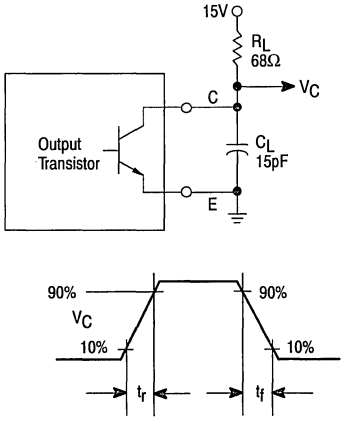


Figure 13. Emitter-Follower Configuration and Waveform

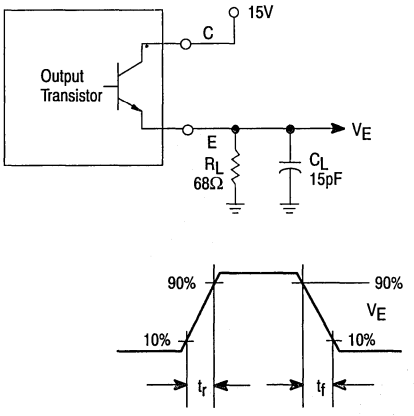


Figure 14. Error Amplifier Sensing Techniques

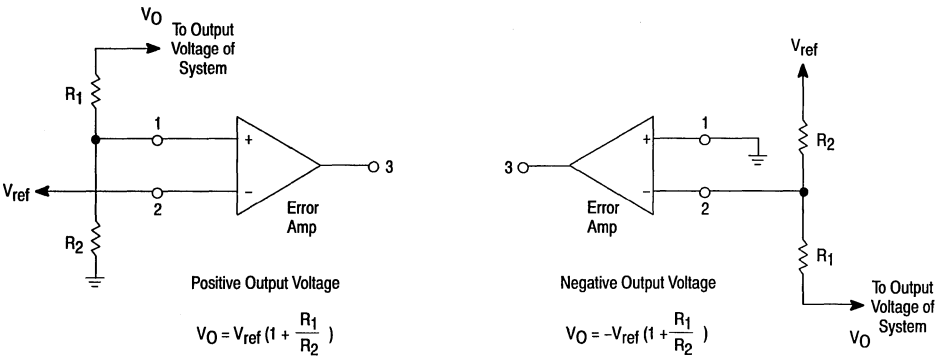


Figure 15. Dead-Time Control Circuit

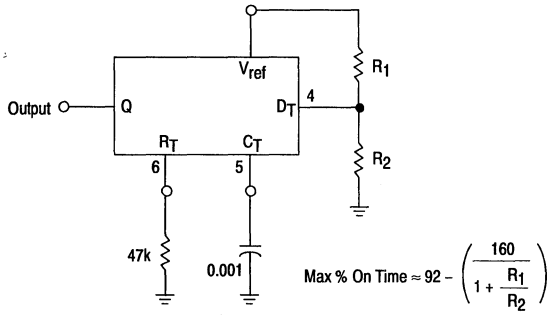


Figure 16. Soft-Start Circuit

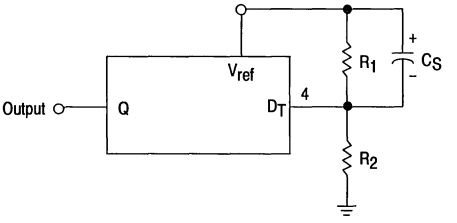


Figure 17. Slaving Two or More Control Circuits

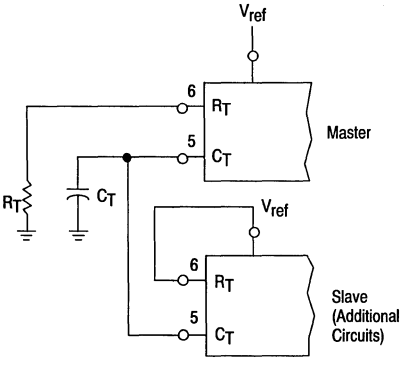
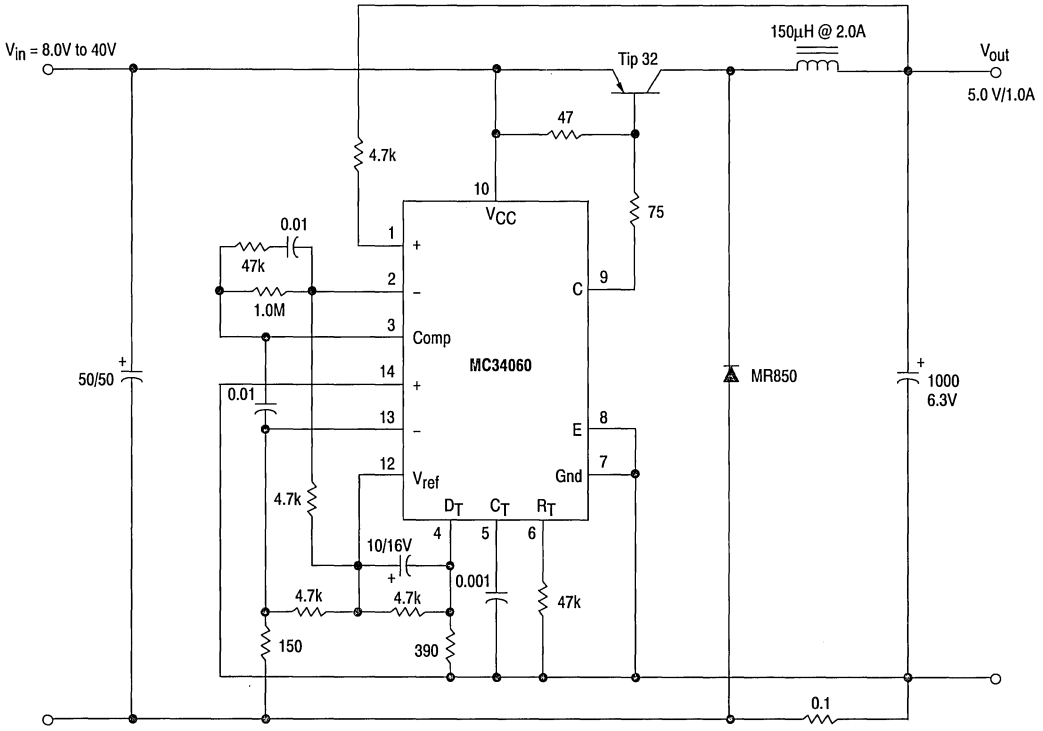
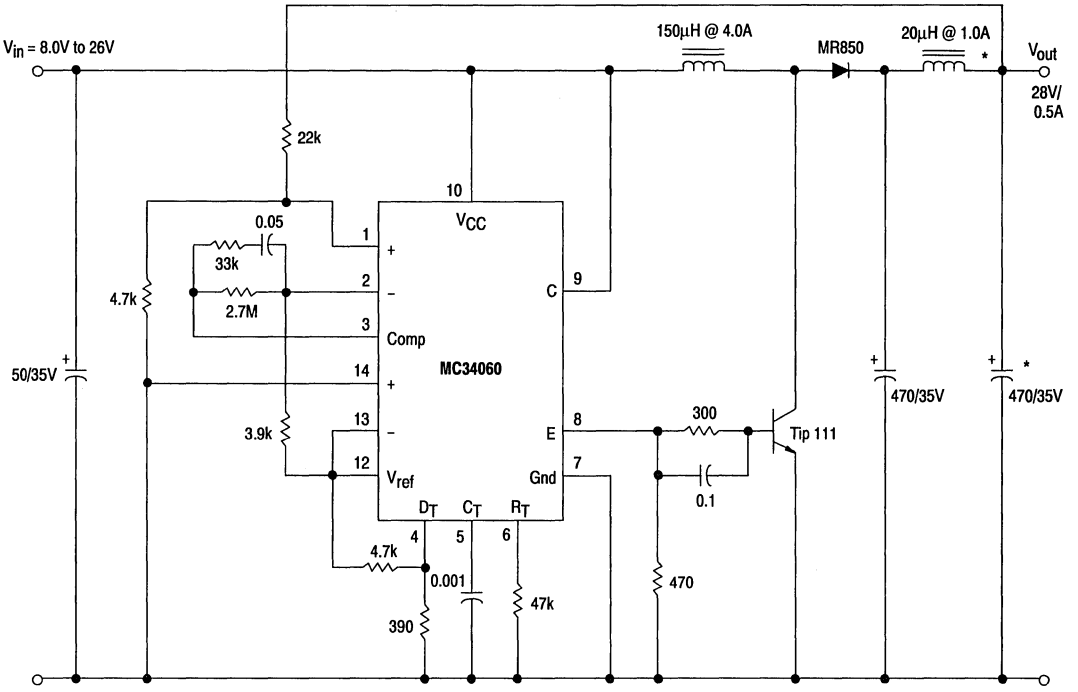


Figure 18. Step-Down Converter with Soft-Start and Output Current Limiting



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 1.0 A	25 mV 0.5%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	75 mV p-p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 12 V, I_O = 1.0 A	73%

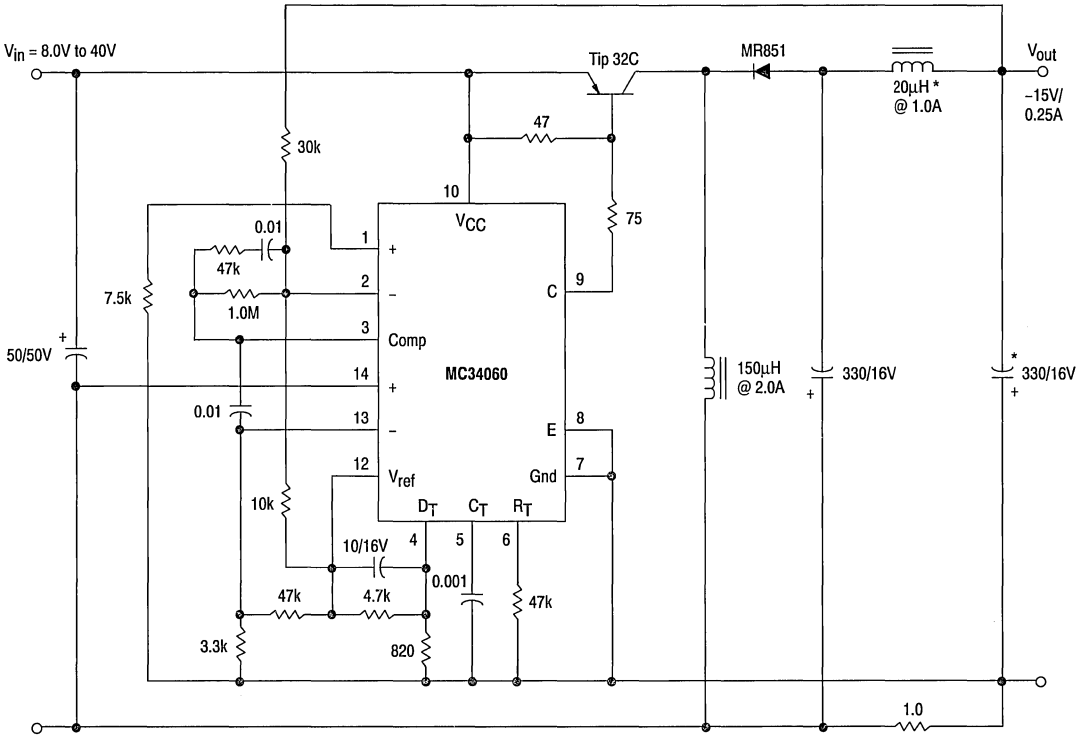
Figure 19. Step-Up Converter



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 26 V, I_O = 0.5 A	40 mV 0.14%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 0.5 A	5.0 mV 0.18%
Output Ripple	V_{in} = 12 V, I_O = 0.5 A	24 mV p-p P.A.R.D.
Efficiency	V_{in} = 12 V, I_O = 0.5 A	75%

* Optional circuit to minimize output ripple

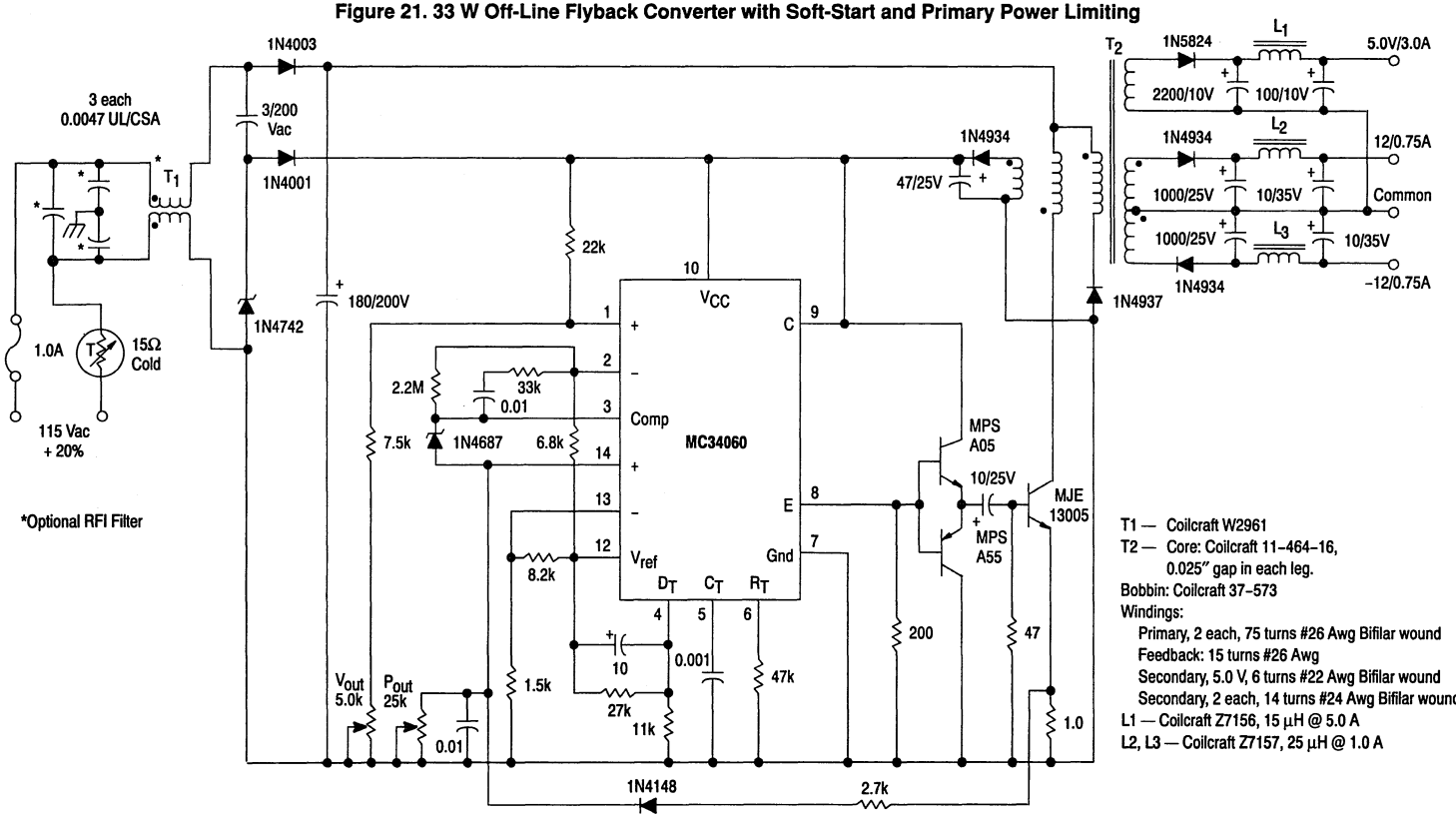
Figure 20. Step-Up/Down Voltage Inverting Converter with Soft-Start and Current Limiting



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 250 mA	52 mV 0.35%
Load Regulation	V_{in} = 12 V, I_O = 1 mA to 250 mA	47 mV 0.32%
Output Ripple	V_{in} = 12 V, I_O = 250 mA	10 mV p-p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	330 mA
Efficiency	V_{in} = 12 V, I_O = 250 mA	86%

* Optional circuit to minimize output ripple

Figure 21. 33 W Off-Line Flyback Converter with Soft-Start and Primary Power Limiting



T1 — Coilcraft W2961
T2 — Core: Coilcraft 11-464-16,
0.025″ gap in each leg.
Bobbin: Coilcraft 37-573
Windings:
Primary, 2 each, 75 turns #26 Awg Bifilar wound
Feedback: 15 turns #26 Awg
Secondary, 5.0 V, 6 turns #22 Awg Bifilar wound
Secondary, 2 each, 14 turns #24 Awg Bifilar wound
L1 — Coilcraft Z7156, 15 μH @ 5.0 A
L2, L3 — Coilcraft Z7157, 25 μH @ 1.0 A

TEST	CONDITIONS	RESULTS
Line Regulation 5.0 V	V_{in} = 95 Vac to 135 Vac, I_O = 3.0 A	20 mV 0.40%
Line Regulation ±12 V	V_{in} = 95 Vac to 135 Vac, I_O = ±0.75 A	52 mV 0.26%
Load Regulation 5.0 V	V_{in} = 115 Vac, I_O = 1.0 A to 4.0 A	476 mV 9.5%
Load Regulation ±12 V	V_{in} = 115 Vac, I_O = ± 0.4 A to ± 0.9 A	300 mV 2.5%
Output Ripple 5.0 V	V_{in} = 115 Vac, I_O = 3.0 A	45 mV p-p P.A.R.D.
Output Ripple ±12 V	V_{in} = 115 Vac, I_O = ±0.75 A	75 mV p-p P.A.R.D.
Efficiency	V_{in} = 115 Vac, I_O 5.0 V = 3.0 A I_O ±12 = ±0.75 A	74%

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC34060A
MC35060A
MC33060A

Precision Switchmode Pulse Width Modulator Control Circuits

PRECISION SWITCHMODE PULSE WIDTH MODULATOR CONTROL CIRCUITS

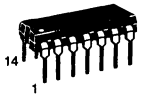
SILICON MONOLITHIC INTEGRATED CIRCUIT

3

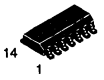
The MC35060A/MC34060A/MC33060A are low cost fixed frequency, pulse width modulation control circuits designed primarily for single ended SWITCHMODE power supply control.

The MC34060A is specified over the commercial operating temperature range of 0° to +70°C. The MC35060A is specified over the full military temperature range of −55° to +125°C, and the MC33060A is specified over an automotive temperature range of −40° to +85°C.

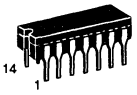
- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator with Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 V Reference, 1.5% Accuracy
- Adjustable Dead-Time Control
- Uncommitted Output Transistor Rated to 200 mA Source or Sink
- Undervoltage Lockout
- Available in Surface Mount Package



P SUFFIX
PLASTIC PACKAGE
CASE 646

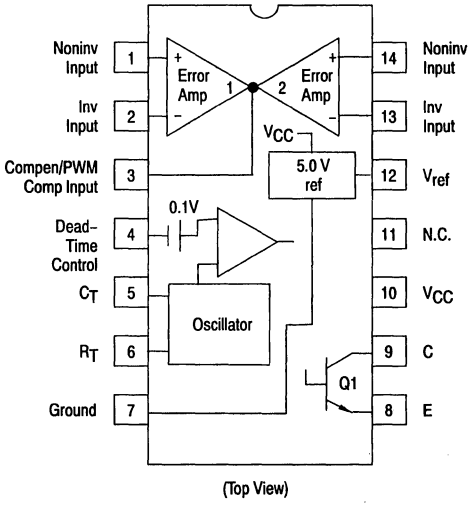


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



L SUFFIX
CERAMIC PACKAGE
CASE 632

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34060AD	0° to +70°C	SO-14
MC34060AP		Plastic DIP
MC33060AD	−40° to +85°C	SO-14
MC33060AP		Plastic DIP
MC34060AL	−55° to +125°C	Ceramic DIP

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	MC35060A	MC34060A	MC33060A	Unit
Power Supply Voltage	V_{CC}	42			V
Collector Output Voltage	V_C	42			V
Collector Output Current (Note 1)	I_C	500			mA
Amplifier Input Voltage Range	V_{in}	−0.3 to +42			V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000			mW
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 — 150	 125 —		°C
Storage Temperature Range Plastic Package Ceramic Package	T_{stg}	 — −65 to +150	 −55 to +125 —		°C
Operating Ambient Temperature Range	T_A	−55 to +125	0 to +70	−40 to +85	°C

NOTES: 1. Maximum thermal limits must be observed.

THERMAL CHARACTERISTICS

Characteristics	Symbol	L Suffix Ceramic Package	P Suffix Plastic Package	D Suffix Plastic Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	100	80	120	°C/W
Derating Ambient Temperature	T_A	50	45	45	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	MC35060A/MC34060A/MC33060A			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_C	—	30	40	V
Collector Output Current	I_C	—	—	200	mA
Amplifier Input Voltage	V_{in}	−0.3	—	V_{CC} −2	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	47	500	kΩ
Timing Capacitor	C_T	0.00047	0.001	10	µF
Oscillator Frequency	f_{osc}	1.0	25	200	kHz
PWM Input Voltage (Pins 3 and 4)	—	−0.3	—	5.3	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted.
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristics	Symbol	MC35060A/MC34060A/MC33060A			Unit
		Min	Typ	Max	
REFERENCE SECTION					
Reference Voltage (I_O = 1.0 mA, T_A 25°C) $T_A = T_{low}$ to T_{high} — MC34060A — MC33060A, MC35060A	V_{ref}	4.925 4.9 4.85	5.0 — —	6.075 5.1 5.1	V
Line Regulation (V_{CC} = 7.0 V to 40 V, I_O = 10 mA))	Reg_{line}	—	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	2.0	15	mV
Short Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted.
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristics	Symbol	MC35060A/MC34060A/MC33060A Min	Typ	Max	Unit
OUTPUT SECTION					
Collector Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	—	2.0	100	µA
Emitter Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V, V_E = 0 V)	$I_{E(off)}$	—	—	–100	µA
Collector-Emitter Saturation Voltage (Note 2) Common-Emitter (V_E = 0 V, I_C = 200 mA) Emitter-Follower (V_C = 15 V, I_E = –200 mA)	$V_{sat(C)}$ $V_{sat(E)}$	— —	1.1 1.5	1.5 2.5	V
Output Voltage Rise Time (T_A = 25°C) Common-Emitter (See Figure 12) Emitter-Follower (See Figure 13)	t_r	— —	100 100	200 200	ns
Output Voltage Fall Time (T_A = 25°C) Common-Emitter (See Figure 12 Emitter-Follower (See Figure 13)	t_r	— —	40 40	100 100	ns
ERROR AMPLIFIER SECTION					
Input Offset Voltage ($V_{O[Pin\ 3]}$ = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current ($V_{C[Pin\ 3]}$ = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias current ($V_{O[Pin\ 3]}$ = 2.5 V)	I_{IB}	—	–0.1	–2.0	µA
Input Common Mode Voltage Range (V_{CC} = 40 V)	V_{ICR}	0 to V_{CC} –2.0	—	—	V
Inverting Input Voltage Range	$V_{IR(INV)}$	–0.3 to V_{CC}–2.0	—	—	V
Open-Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	—	dB
Unity-Gain Crossover Frequency (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	f_c	—	600	—	kHz
Phase Margin at Unity-Gain (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	—	65	—	deg.
Common Mode Rejection Ratio (V_{CC} = 40 V, V_{in} = 0 V to 38 V))	CMRR	65	90	—	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	—	100	—	dB
Output Sink Current ($V_{O[Pin\ 3]}$ = 0.7 V)	I_{O-}	0.3	0.7	—	mA
Output Source Current ($V_{O[Pin\ 3]}$ = 3.5 V)	I_{O+}	–2.0	–4.0	—	mA

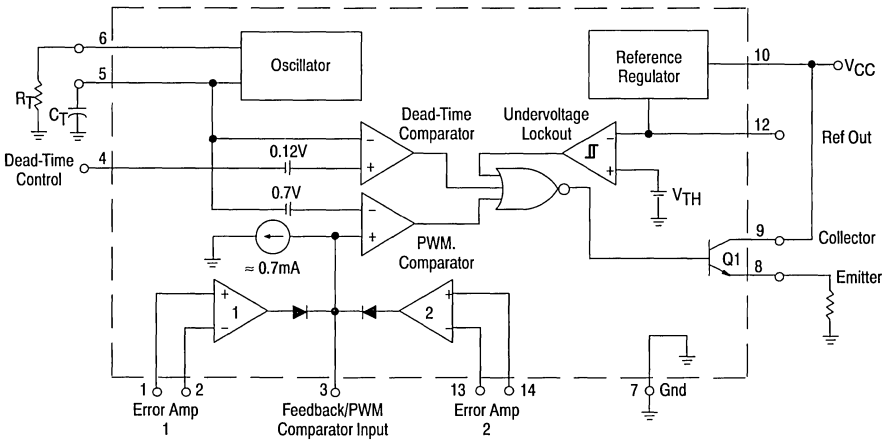
NOTES: 2. Low duty cycle techniques are used during test to maintain junction temperature as close to ambient temperatures as possible.
T_{low} = –55°C for MC35060A = –40°C for MC33060A = 0°C for MC34060A
T_{high} = +125°C for MC35060A = +85°C for MC33060A = +70°C for MC34060A

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted.
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristics	Symbol	MC35060A/MC34060A/MC33060A Min	Typ	Max	Unit
PWM COMPARATOR SECTION (Test circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	—	3.5	4.5	V
Input Sink Current ($V_{[Pin\ 3]}$ = 0.7 V)	I_I	0.3	0.7	—	mA
DEAD-TIME CONTROL SECTION (Test circuit Figure 11)					
Input Bias Current (Pin 4) (V_{in} = 0 V to 5.25 V)	$I_{IB(DT)}$	—	–1.0	–10	µA
Maximum Output Duty Cycle	DC_{max}				%
(V_{in} = 0 V, C_T = 0.01 µF, R_T = 12 kΩ)		90	96	100	
(V_{in} = 0 V, C_T = 0.001 µF, R_T = 47 kΩ)		—	92	—	
Input Threshold Voltage (Pin 4)	V_{TH}				V
(Zero Duty Cycle)		—	2.8	3.3	
(Maximum Duty Cycle)		0	—	—	
OSCILLATOR SECTION					
Frequency	f_{osc}				kHz
(C_T = 0.01 µF, R_T = 12 kΩ, T_A = 25°C)		9.7	10.5	11.3	
T_A = T_{low} to T_{high} — MC34060A		9.5	—	11.5	
— MC33060A, MC35060A		9.0	—	11.5	
(C_T = 0.001 µF, R_T = 47 kΩ)		—	25	—	
Standard Deviation of Frequency* (C_T = 0.001 µF, R_T = 47 kΩ)	σf_{osc}	—	1.5	—	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V)	$\Delta f_{osc}(\Delta V)$	—	0.5	2.0	%
Frequency Change with Temperature	$\Delta f_{osc}(\Delta T)$				%
(ΔT_A = T_{low} to T_{high})		—	4.0	—	
(C_T = 0.01 µF, R_T = 12 kΩ)		—	—	—	
UNDERVOLTAGE LOCKOUT SECTION					
Turn-On Threshold (V_{CC} increasing, I_{ref} = 1.0 mA)	V_{th}	4.0	4.7	5.5	V
Hysteresis	V_H	50	150	300	mV
TOTAL DEVICE					
Standby Supply Current	I_{CC}				mA
(Pin 6 at V_{ref}, all other inputs and outputs open)					
(V_{CC} = 15 V)		—	5.5	10	
(V_{CC} = 40 V)		—	7.0	15	
Average Supply Current ($V_{[Pin\ 4]}$ = 2.0 V, C_T = 0.001 µF, R_T = 47 kΩ). See Figure 11.	I_S	—	7.0	—	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula; $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - x)^2}{N-1}}$

Figure 1. Block Diagram



Description

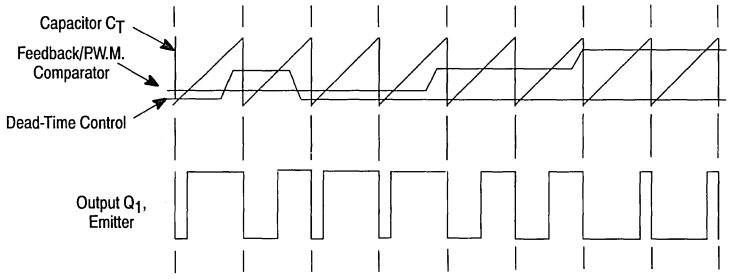
The MC34060A/35060A/33060A is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply (see Figure 1). An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \cong \frac{1.2}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The output is enabled only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

Figure 2. Timing Diagram



APPLICATIONS INFORMATION

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feed-back input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle of 96%. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 V to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common mode input range from –0.3 V to (V_{CC} –2.0 V), and may be used to sense power supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the noninverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

The MC34060A/MC35060A/33060A has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an internal accuracy of ±5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to +70°C.

Figure 3. Oscillator Frequency versus Timing Resistance

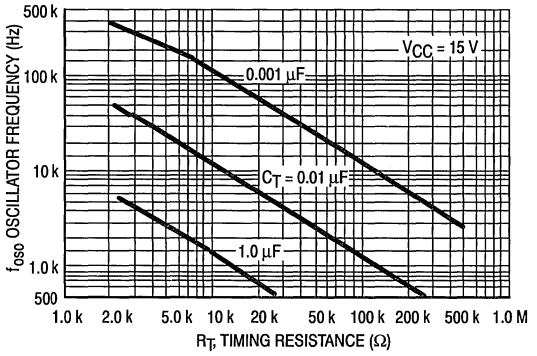


Figure 4. Open-Loop Voltage Gain and Phase versus Frequency

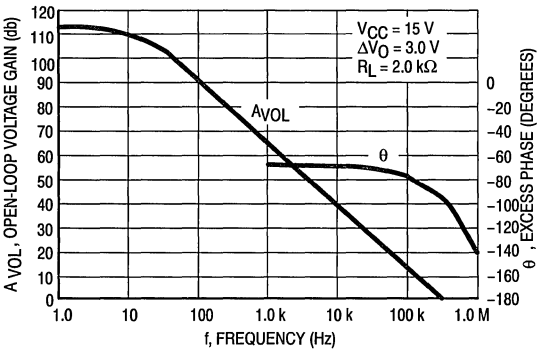


Figure 5. Percent Dead-Time versus Oscillator Frequency

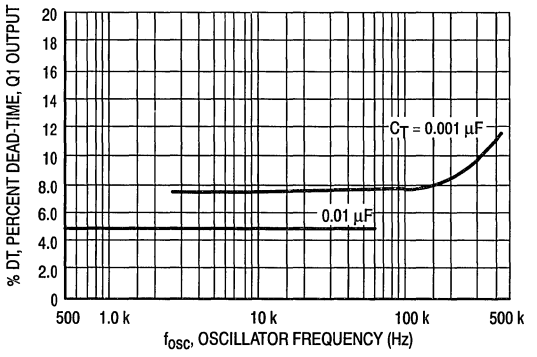


Figure 6. Percent Duty Cycle versus Dead-Time Control Voltage

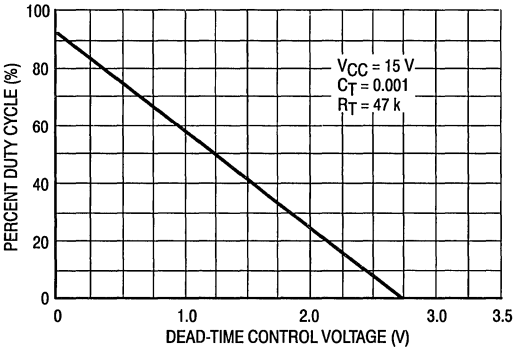


Figure 7. Emitter-Follower Configuration Output Saturation Voltage versus Emitter Current

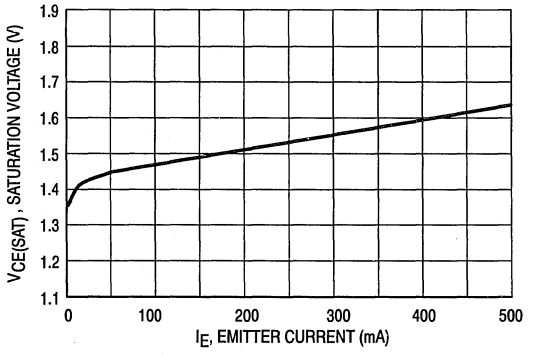


Figure 8. Common-Emitter Configuration Output Saturation Voltage versus Collector Current

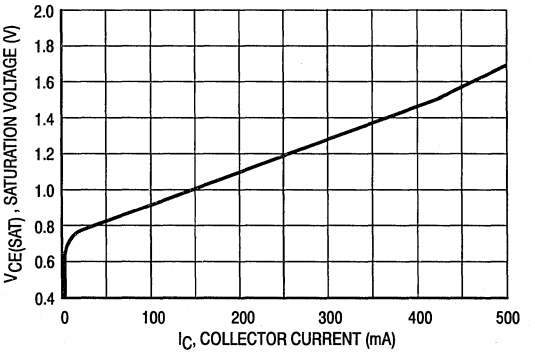


Figure 9. Standby Supply Current versus Supply Voltage

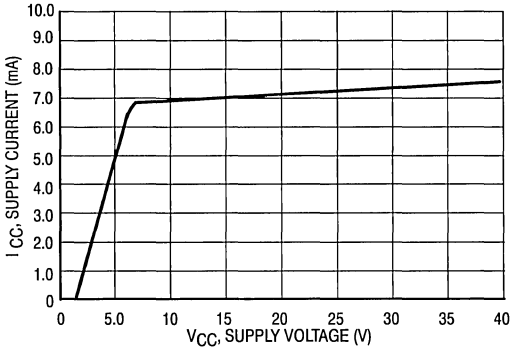


Figure 10. Undervoltage Lockout Thresholds versus Reference Load Current

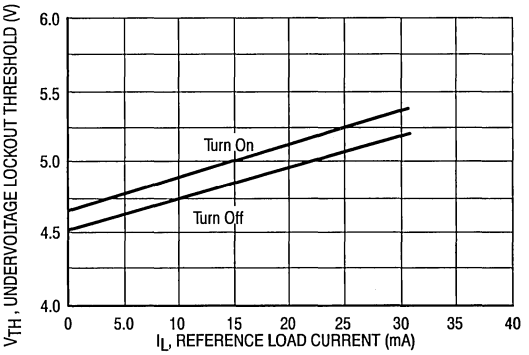


Figure 11. Error Amplifier Characteristics

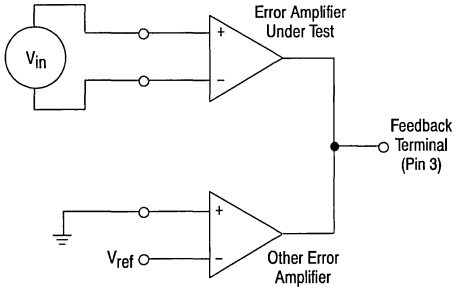


Figure 12. Dead-Time and Feedback Control

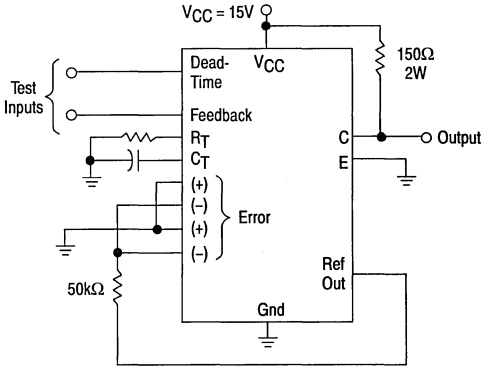


Figure 13. Common-Emitter Configuration and Waveform

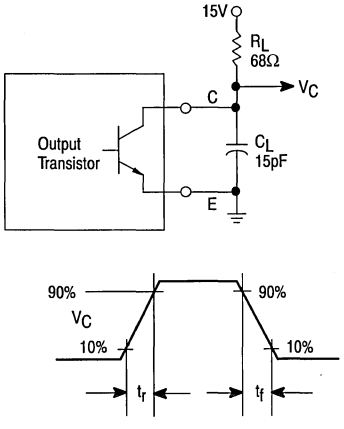


Figure 14. Emitter-Follower Configuration and Waveform

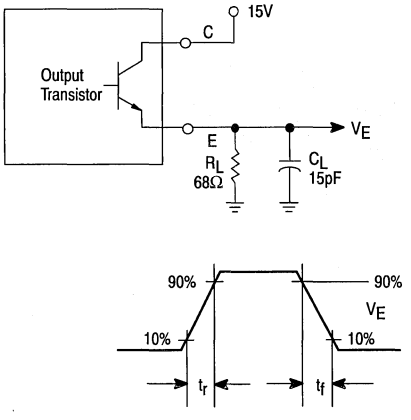


Figure 15. Error Amplifier Sensing Techniques

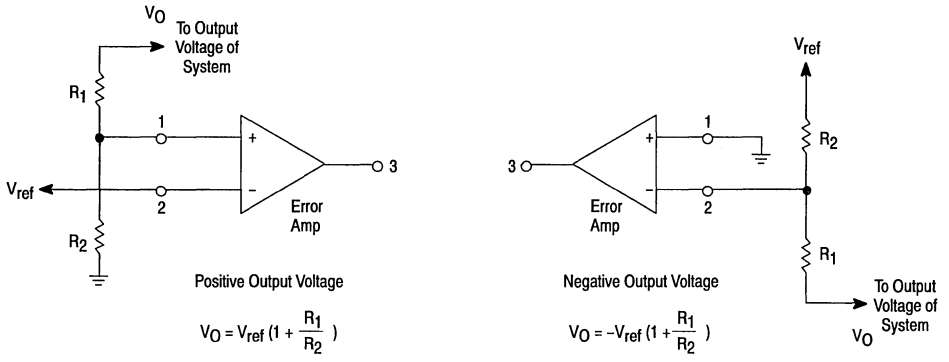


Figure 16. Dead-Time Control Circuit

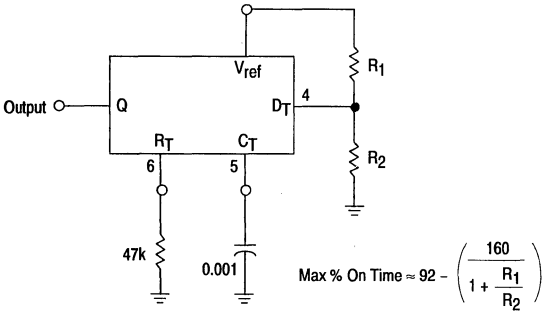


Figure 17. Soft-Start Circuit

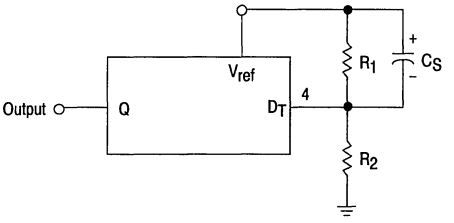


Figure 18. Slaving Two or More Control Circuits

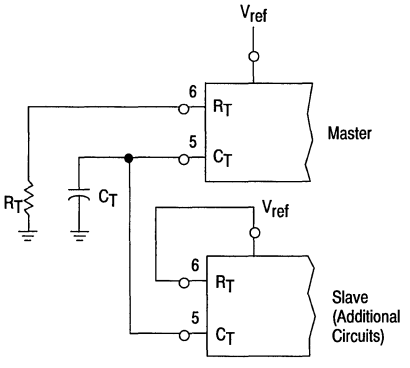
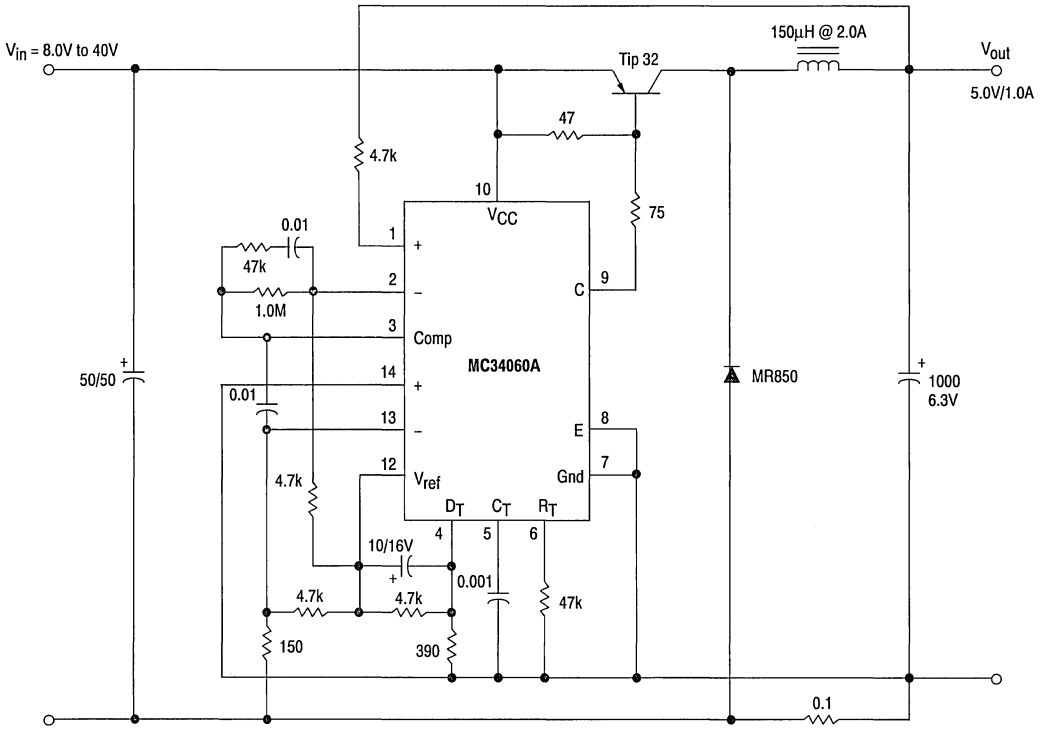


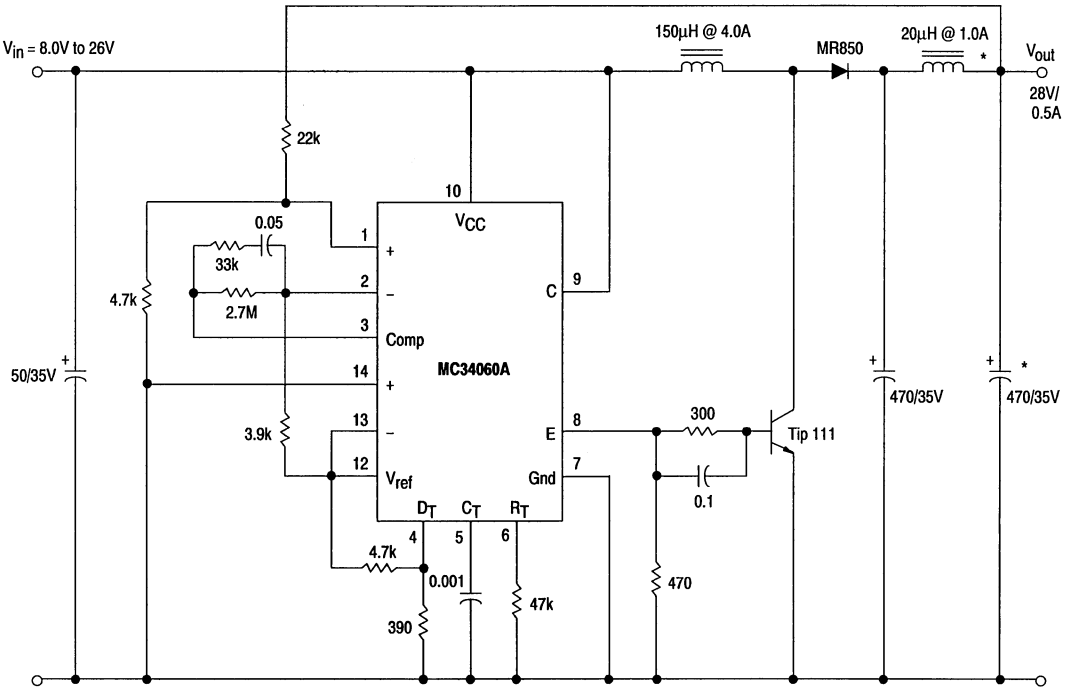
Figure 19. Step-Down Converter with Soft-Start and Output Current Limiting



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 1.0 A	25 mV 0.5%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	75 mV p-p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 12 V, I_O = 1.0 A	73%

3

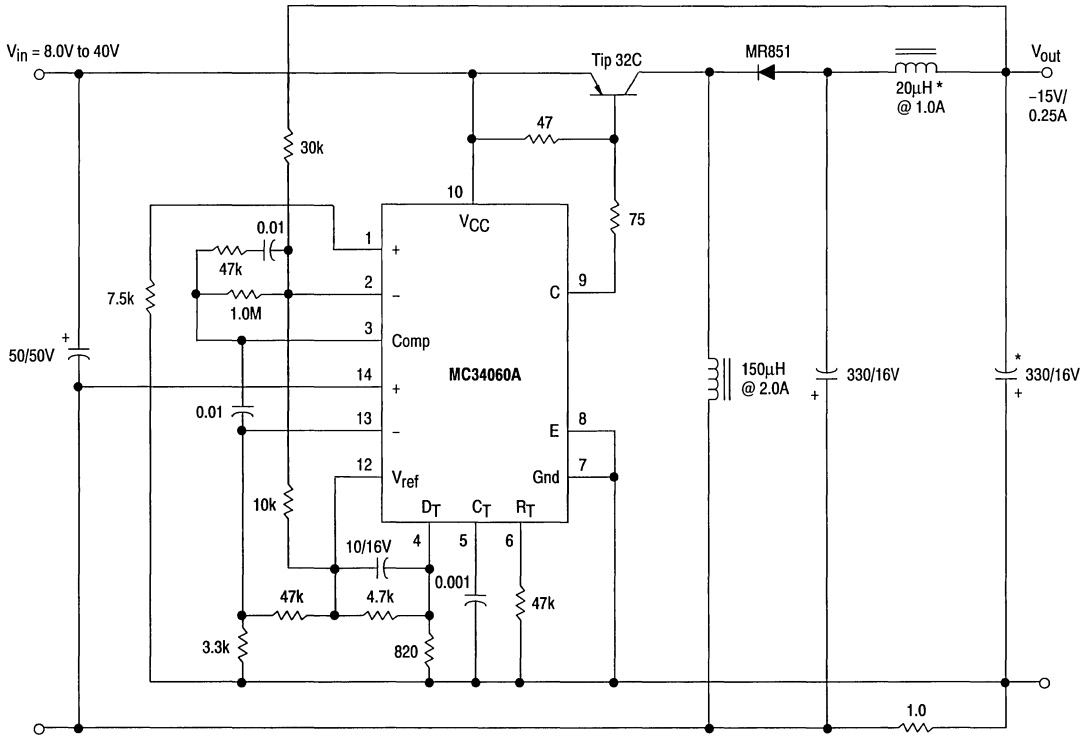
Figure 20. Step-Up Converter



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 26 V, I_O = 0.5 A	40 mV 0.14%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 0.5 A	5.0 mV 0.18%
Output Ripple	V_{in} = 12 V, I_O = 0.5 A	24 mV p-p P.A.R.D.
Efficiency	V_{in} = 12 V, I_O = 0.5 A	75%

* Optional circuit to minimize output ripple

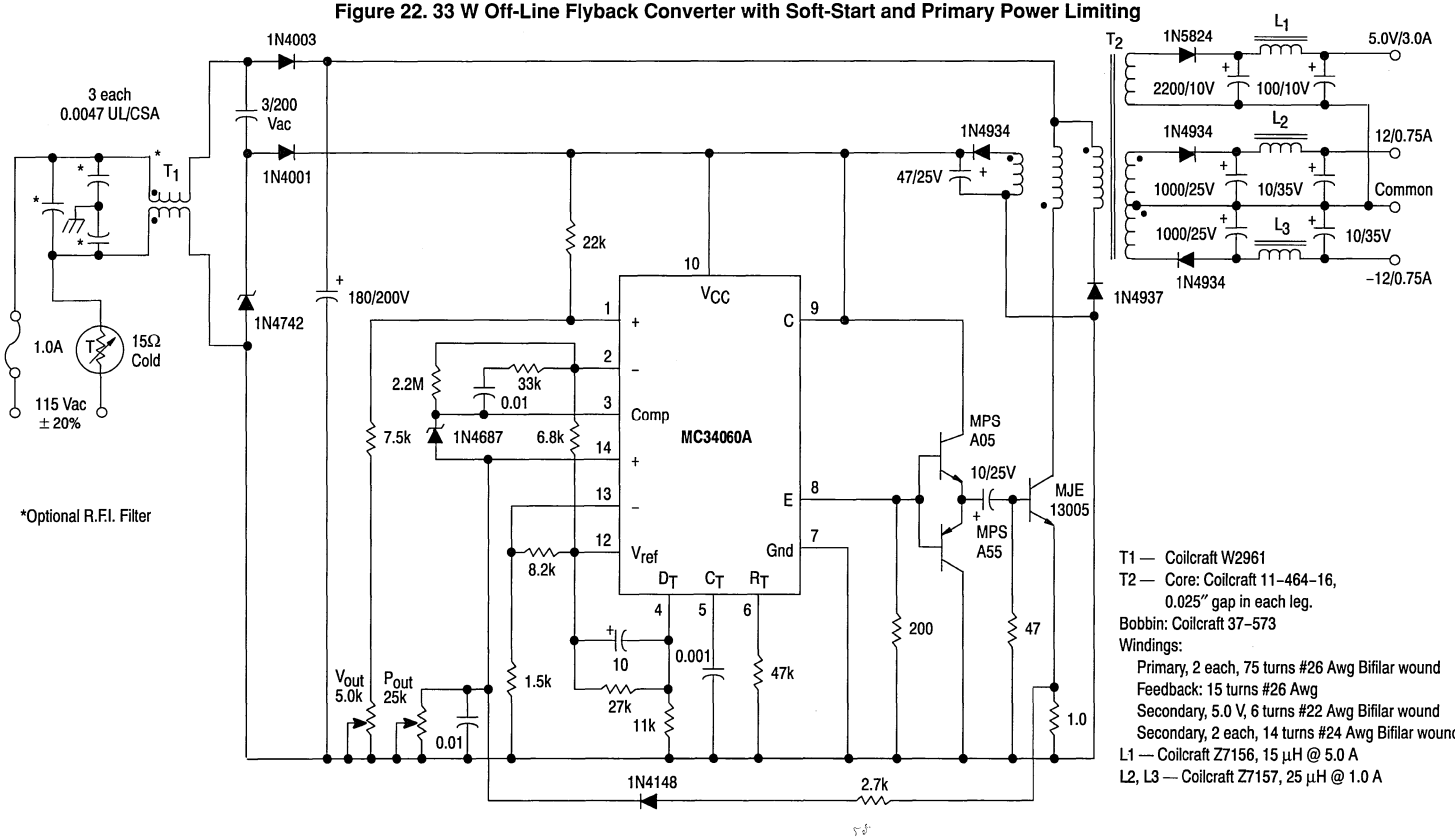
Figure 21. Step-Up/Down Voltage Inverting Converter with Soft-Start and Current Limiting



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 250 mA	52 mV 0.35%
Load Regulation	V_{in} = 12 V, I_O = 1.0 to 250 mA	47 mV 0.32%
Output Ripple	V_{in} = 12 V, I_O = 250 mA	10 mV p-p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	330 mA
Efficiency	V_{in} = 12 V, I_O = 250 mA	86%

* Optional circuit to minimize output ripple

Figure 22. 33 W Off-Line Flyback Converter with Soft-Start and Primary Power Limiting



T1 — Coilcraft W2961
T2 — Core: Coilcraft 11-464-16,
0.025″ gap in each leg.
Bobbin: Coilcraft 37-573
Windings:
Primary, 2 each, 75 turns #26 Awg Bifilar wound
Feedback: 15 turns #26 Awg
Secondary, 5.0 V, 6 turns #22 Awg Bifilar wound
Secondary, 2 each, 14 turns #24 Awg Bifilar wound
L1 — Coilcraft Z7156, 15 μH @ 5.0 A
L2, L3 — Coilcraft Z7157, 25 μH @ 1.0 A

Test	Conditions	Results
Line Regulation 5.0 V	V_{in} = 95 Vac to 135 Vac, I_O = 3.0 A	20 mV 0.40%
Line Regulation ±12 V	V_{in} = 95 Vac to 135 Vac, I_O = ±0.75 A	52 mV 0.26%
Load Regulation 5.0 V	V_{in} = 115 Vac, I_O = 1.0 A to 4.0 A	476 mV 9.5%
Load Regulation ±12 V	V_{in} = 115 Vac, I_O = ± 0.4 A to ± 0.9 A	300 mV 2.5%
Output Ripple 5.0 V	V_{in} = 115 Vac, I_O = 3.0 A	45 mV p-p P.A.R.D.
Output Ripple ±12 V	V_{in} = 115 Vac, I_O = ±0.75 A	75 mV p-p P.A.R.D.
Efficiency	V_{in} = 115 Vac, I_O 5.0 V = 3.0 A I_O ±12 V = ±0.75 A	74%

MC34063A
MC35063A
MC33063A

DC-to-DC Converter Control Circuits

The MC34063A/35063A/33063A is a series of monolithic control circuits containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components. Refer to Application Note AN920 R2 for additional design information.

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference

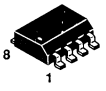
DC-TO-DC CONVERTER CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUIT

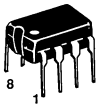
3

P1 SUFFIX
PLASTIC PACKAGE
CASE 626

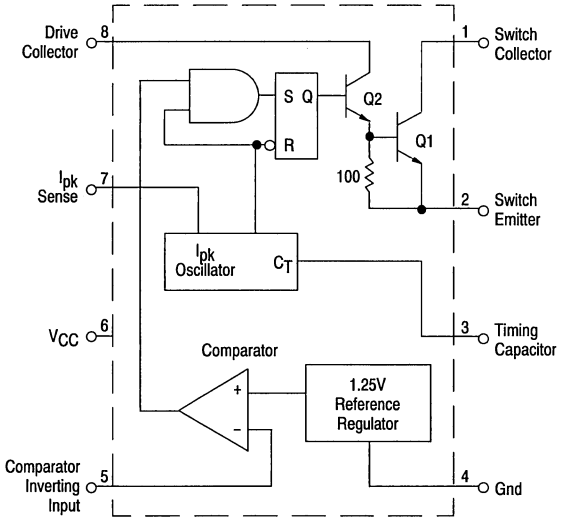
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)



U SUFFIX
CERAMIC PACKAGE
CASE 693

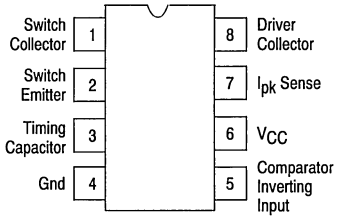


Functional Block Diagram



(Bottom View)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34063AD	0° to +70°C	SO-8
MC34063AP1		Plastic DIP
MC35063AU	–55° to +125°C	Ceramic DIP
MC33063AD	–40° to +85°C	SO-8
MC33063AP1		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	−0.3 to +40	Vdc
Switch Collector Voltage	$V_{C(switch)}$	40	Vdc
Switch Emitter Voltage ($V_{Pin\ 1}$ = 40 V)	$V_{E(switch)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Driver Collector Current (Note 1)	$I_{C(driver)}$	100	mA
Switch Current	I_{SW}	1.5	A
Power Dissipation and Thermal Characteristics Ceramic Package, U Suffix T_A = +25°C Thermal Resistance Plastic Package, P Suffix T_A = +25°C Thermal Resistance SOIC Package, D Suffix T_A = +25°C Thermal Resistance	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 1.25 100 1.25 100 625 160	 W °C/W W °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range MC35063A MC33063A MC34063A	T_A	 −55 to +125 −40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERICISTICS (V_{CC} = 5.0 V, T_A = T_{low} to T_{high} [Note 2], unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency ($V_{Pin\ 5}$ = 0 V, C_T = 1.0 nF, T_A = 25°C)	f_{osc}	24	33	42	kHz
Charge Current (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	I_{chg}	24	33	42	µA
Discharge Current (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	I_{dischg}	140	200	260	µA
Discharge to Charge Current Ratio (Pin 7 to V_{CC}, T_A = 25°C)	I_{dischg}/I_{chg}	5.2	6.2	7.5	—
Current Limit Sense Voltage (I_{chg} = I_{dischg}, T_A = 25°C)	$V_{Ipk(sense)}$	250	300	350	mV

NOTES: 1. Maximum package power dissipation limits must be observed.

2. T_{low} = −55°C for MC35063A; −40°C for MC33063A; 0°C for MC34063A
   T_{high} = +125°C for MC35063A; +85°C for MC33063A; +70°C for MC34063A

ELECTRICAL CHARACTERICISTICS — Continued (V_{CC} = 5.0 V; T_A = T_{low} to T_{high}, unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
OUTPUT SWITCH (Note 3)					
Saturation Voltage, Darlington Connection (I_{SW} = 1.0 A, Pins 1, 8 connected)	$V_{CE(sat)}$	—	1.0	1.3	V
Saturation Voltage (I_{SW} = 1.0 A, $R_{Pin\ 8}$ = 82 Ω to V_{CC}, Forced β ≃ 20)	$V_{CE(sat)}$	—	0.45	0.7	V
DC Current Gain (I_{SW} = 1.0 A, V_{CE} = 5.0 V, T_A = 25°C)	h_{FE}	50	120	—	—
Collector Off-State Current (V_{CE} = 40 V)	$I_{C(off)}$	—	0.01	100	μA
COMPARATOR					
Threshold Voltage (T_A = 25°C) (T_A = T_{low} to T_{high})	V_{th}	 1.225 1.21	 1.25 —	 1.275 1.29	V
Threshold Voltage Line Regulation (V_{CC} = 3.0 V to 40 V)	Reg_{line}	—	1.4	5.0	mV
Input Bias Current (V_{in} = 0 V)	I_{IB}	—	–40	–400	nA
TOTAL DEVICE					
Supply Current (V_{CC} = 5.0 V to 40 V, C_T = 1.0 nF, Pin 7 = V_{CC}, $V_{Pin\ 5}$ > V_{th}, Pin 2 = Gnd, Remaining pins open)	I_{CC}	—	2.5	4.0	mA

NOTES: 3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

4. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥30 mA), it may take up to 2.0 μs to come out of saturation. This condition will shorten the "off" time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended.

Forced β of output switch = I_C, output/(I_C, driver –7.0 mA*) ≥ 10

*The 100 Ω resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.

3

Figure 1. Output Switch On-Off Time versus Oscillator Timing Capacitor

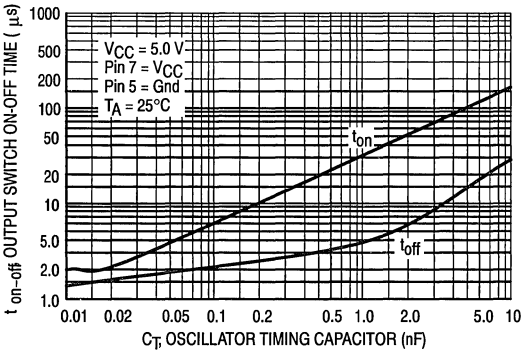


Figure 2. Timing Capacitor Waveform

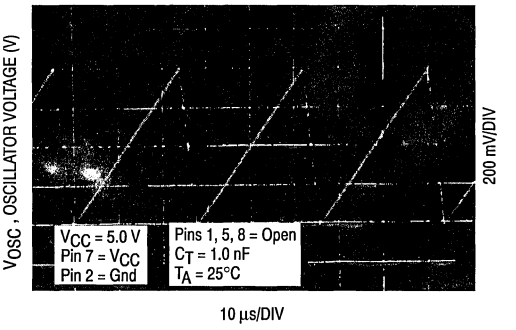


Figure 3. Emitter Follower Configuration Output Saturation Voltage versus Emitter Current

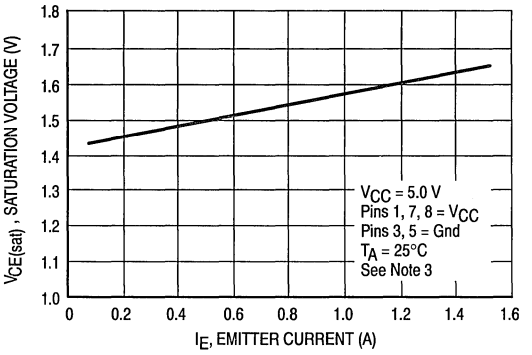


Figure 4. Common Emitter Configuration Output Switch Saturation Voltage versus Collector Current

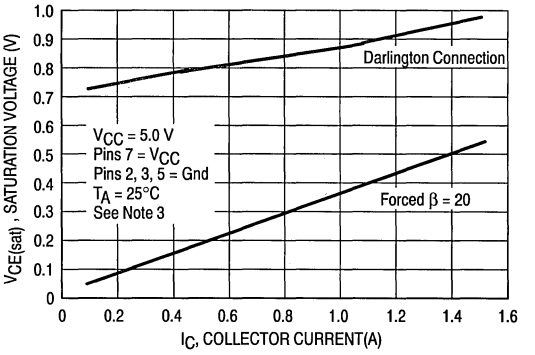


Figure 5. Current Limit Sense Voltage versus Temperature

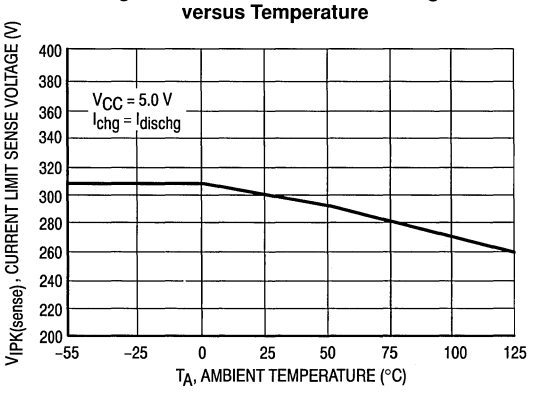


Figure 6. Standby Supply Current versus Supply Voltage

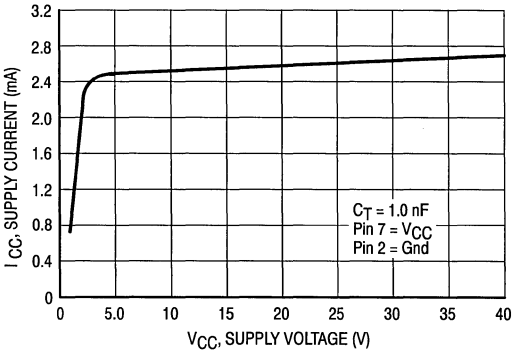
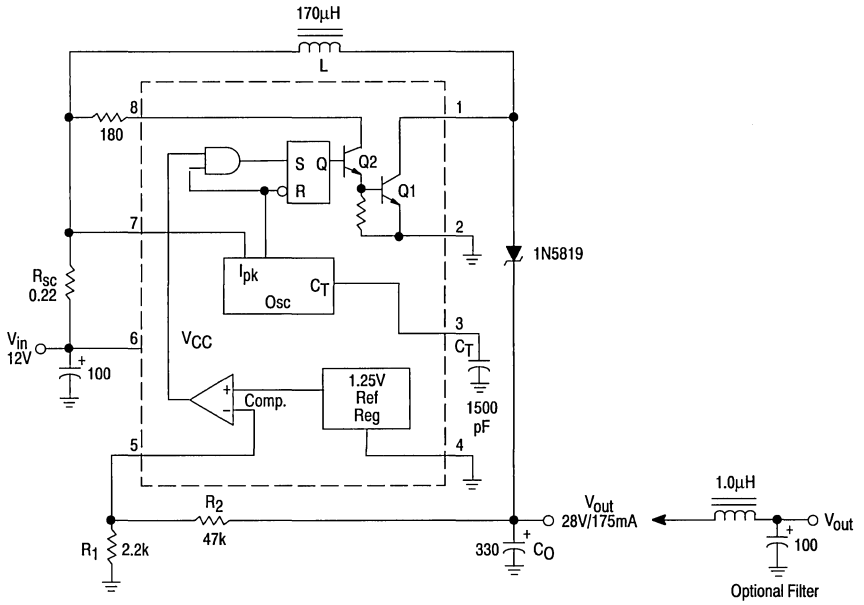


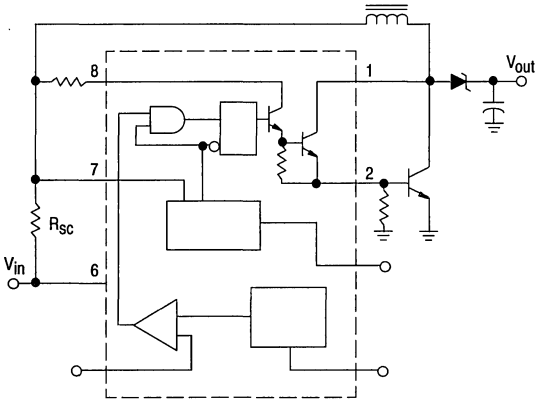
Figure 7. Step-Up Converter



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 16 V, I_O = 175 mA	30 mV = ±0.05%
Load Regulation	V_{in} = 12 V, I_O = 75 mA to 175 mA	10 mV = ±0.017%
Output Ripple	V_{in} = 12 V, I_O = 175 mA	400 mVp-p
Efficiency	V_{in} = 12 V, I_O = 175 mA	89.2%
Output Ripple With Optional Filter	V_{in} = 12 V, I_O = 175 mA	40 mVp-p

Figure 8. External Current Boost Connection for I_C Peak Greater than 1.5 A

External NPN Switch



External NPN Saturated Switch
(Refer to Note 4)

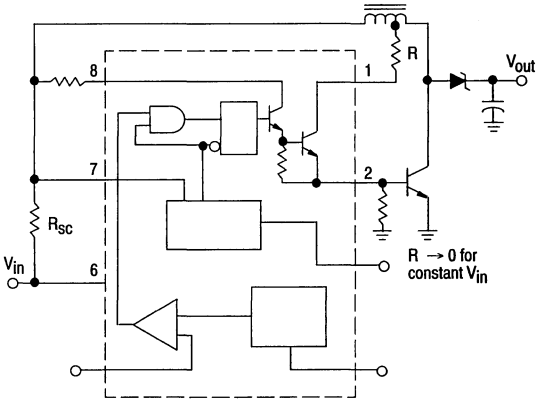


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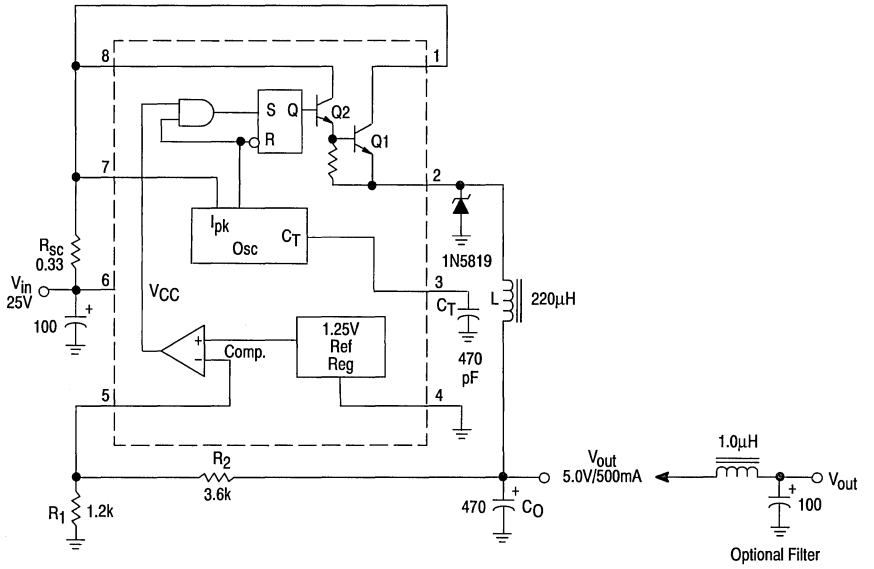
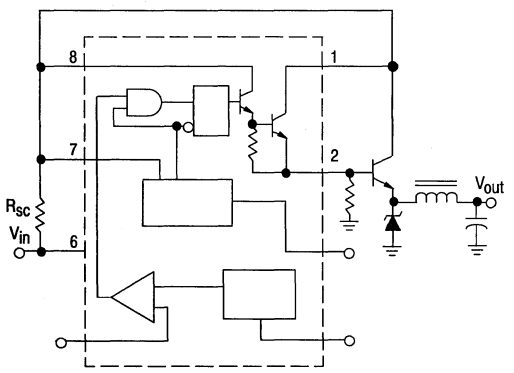
Figure 9. Step-Down Converter



Test	Conditions	Results
Line Regulation	V_{in} = 15 V to 25 V, I_O = 500 mA	12 mV = ±0.12%
Load Regulation	V_{in} = 25 V, I_O = 50 mA to 500 mA	3.0 mV = ±0.03%
Output Ripple	V_{in} = 25 V, I_O = 500 mA	120 mVp-p
Short Circuit Current	V_{in} = 25 V, R_L = 0.1 Ω	1.1 A
Efficiency	V_{in} = 25 V, I_O = 500 mA	82.5%
Output Ripple With Optional Filter	V_{in} = 25 V, I_O = 500 mA	40 mVp-p

Figure 10. External Current Boost Connections for I_C Peak Greater than 1.5 A

External NPN Switch



External PNP Saturated Switch

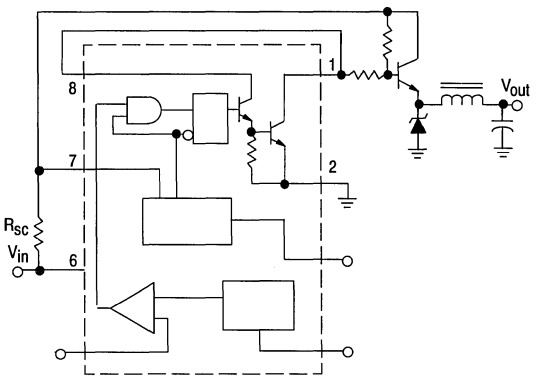
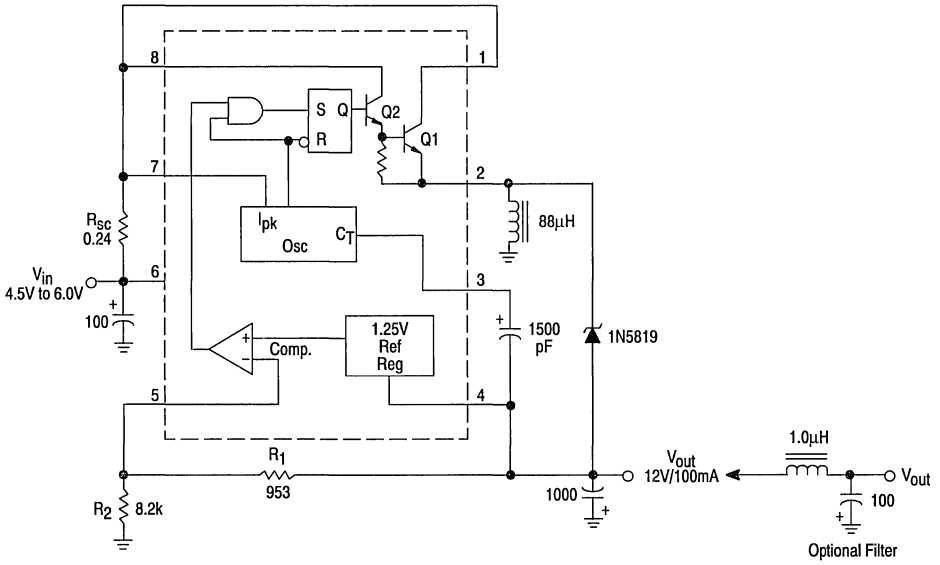


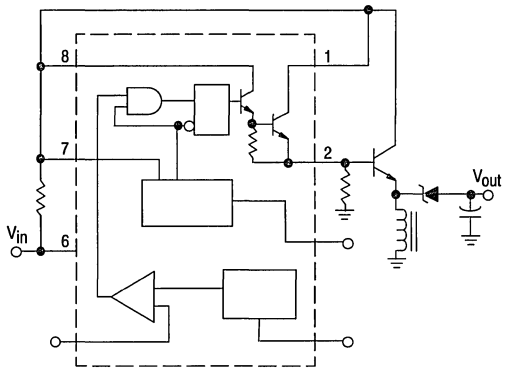
Figure 11. Voltage Inverting Converter



Test	Conditions	Results
Line Regulation	V_{in} = 4.5 V to 6.0 V, I_O = 100 mA	3.0 mV = ±0.012%
Load Regulation	V_{in} = 5.0 V, I_O = 10 mA to 100 mA	0.022 mV = ±0.09%
Output Ripple	V_{in} = 5.0 V, I_O = 100 mA	500 mVp-p
Short Circuit Current	V_{in} = 5.0 V, R_L = 0.1 Ω	910 mA
Efficiency	V_{in} = 5.0 V, I_O = 100 mA	64.5%
Output Ripple With Optional Filter	V_{in} = 5.0 V, I_O = 100 mA	70 mVp-p

Figure 12. External Current Boost Connections for I_C Peak Greater Than 1.5 A

External NPN Switch



External PNP Saturated Switch

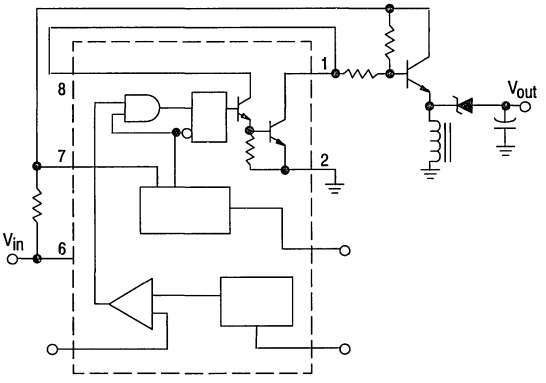
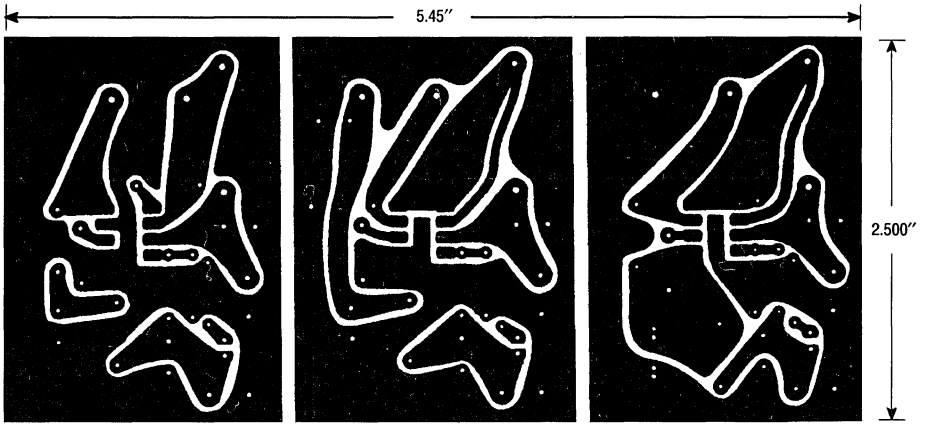
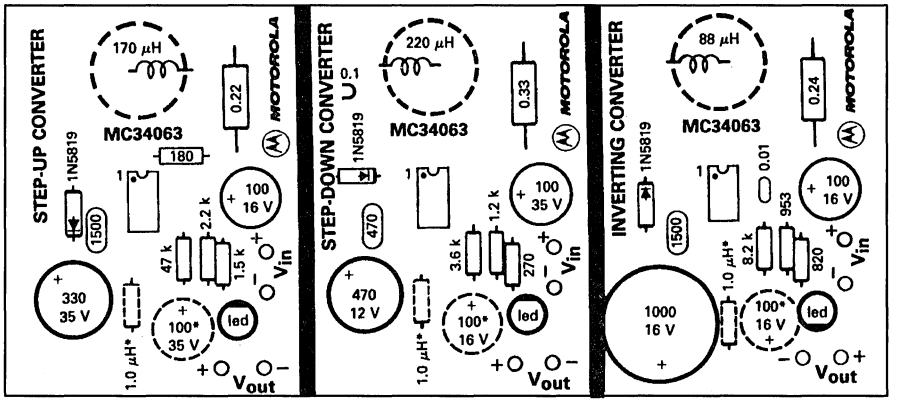


Figure 13. Printed Circuit Board and Component Layout
(Circuits of Figure 7, 9, 11)



(Top view, copper foil as seen through the board from the component side)



*Optional Filter.

Top View, Component Side

INDUCTOR DATA

Converter	Inductance (μH)	Turns/Wire
Step-Up	170	38 Turns of #22 AWG
Step-Down	220	48 Turns of #22 AWG
Voltage-Inverting	88	28 Turns of #22 AWG

All inductors are wound on Magnetics Inc. 55117 toroidal core.

Figure 14. Design Formula Table

Calculation	Step-Up	Step-Down	Voltage-Inverting
t_{on}/t_{off}	$\frac{V_{out}+V_F-V_{in(min)}}{V_{in(min)}-V_{sat}}$	$\frac{V_{out}+V_F}{V_{in(min)}-V_{sat}-V_{out}}$	$\frac{\lvert V_{out}\rvert+V_F}{V_{in}+V_{sat}}$
$(t_{on} + t_{off})$ max	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4.8 \times 10^{-5}\, t_{on}$	$4.8 \times 10^{-5}\, t_{on}$	$4.8 \times 10^{-5}\, t_{on}$
$I_{pk(switch)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$
R_{SC}	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{V_{in(min)}-V_{sat}}{I_{pk(switch)}} \right) t_{on(max)}$	$\left(\frac{V_{in(min)}-V_{sat}-V_{out}}{I_{pk(switch)}} \right) t_{on(max)}$	$\left(\frac{V_{in(min)}-V_{sat}}{I_{pk(switch)}} \right) t_{on(max)}$
C_O	$\approx \frac{I_{out}t_{on}}{V_{ripple(p-p)}}$	$\frac{I_{pk(switch)}(t_{on}+t_{off})}{8V_{ripple(p-p)}}$	$\approx \frac{I_{out}t_{on}}{V_{ripple(p-p)}}$

V_{sat} = Saturation voltage of the output switch.
V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{in} — Nominal input voltage.
V_{out} — Desired output voltage, $\lvert V_{out}\rvert = 1.25 \left(1 + \frac{R2}{R1}\right)$
I_{out} — Desired output current.
f_{min} — Minimum desired output switching frequency at the selected values of V_{in} and I_O.
$V_{ripple(p-p)}$ — Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

NOTE: For further information refer to Application Note AN920 Rev. 2.

MC34064
MC33064

3

Advance Information

Undervoltage Sensing Circuit

UNDERVOLTAGE SENSING CIRCUIT

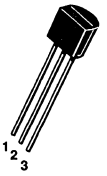
SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC34064 is an undervoltage sensing circuit specifically designed for use as a reset controller in microprocessor-based systems. It offers the designer an economical solution for low voltage detection with a single external resistor. The MC34064 features a trimmed-in-package bandgap reference, and a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation. The open collector reset output is capable of sinking in excess of 10 mA, and operation is guaranteed down to 1.0 V input with low standby current. These devices are packaged in 3-pin TO-226AA and 8-pin surface mount packages.

Applications include direct monitoring of the 5.0 V MPU/logic power supply used in appliance, automotive, consumer and industrial equipment.

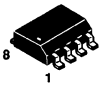
- Trimmed-In-Package Temperature Compensated Reference
- Comparator Threshold of 4.6 V at 25°C
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 10 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation with 1.0 V Input
- Low Standby Current
- Economical TO-226AA and SO-8 Surface Mount Packages

P SUFFIX
PLASTIC PACKAGE
CASE 29
(TO-226AA)



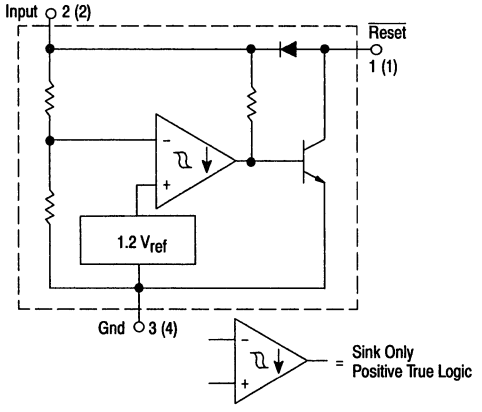
PIN 1. $\overline{\text{RESET}}$
2. Input
3. Ground

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)



PIN 1. $\overline{\text{RESET}}$
2. Input
3. N.C.
4. Ground
5. N.C.
6. N.C.
7. N.C.
8. N.C.

Representative Block Diagram



Pin numbers adjacent to terminals are for the 3-pin TO-226AA package.
Pin numbers in parenthesis are for the D suffix SO-8 package.

ORDERING INFORMATION

Device	Temperature Range	Package
MC34064D-5	0° to +70°C	SO-8
MC34064P-5		TO-226AA
MC33064D-5	–40° to +85°C	SO-8
MC33064P-5		TO-226AA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	V_{in}	–1.0 to 10	V
$\overline{\text{Reset}}$ Output Voltage	V_O	10	V
$\overline{\text{Reset}}$ Output Sink Current (Note 1)	I_{Sink}	Internally Limited	mA
Clamp Diode Forward Current, Pin 1 to 2 (Note 1)	I_F	100	mA
Power Dissipation and Thermal Characteristics			
P Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	625	mW
Thermal Resistance, Junction to Air	$R_{\theta JA}$	200	°C/W
D Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	625	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	200	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
MC34064		0 to +70	
MC33064		–40 to +85	
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERICISTICS (For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3].)

Characteristics	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage					V
High State Output (V_{in} Increasing)	V_{IH}	4.5	4.61	4.7	
Low State Output (V_{in} Decreasing)	V_{IL}	4.5	4.59	4.7	
Hysteresis	V_H	0.01	0.02	0.05	
$\overline{\text{RESET}}$ OUTPUT					
Output Sink Saturation	V_{OL}				V
(V_{in} = 4.0 V, I_{Sink} = 8.0 mA)		—	0.46	1.0	
(V_{in} = 4.0 V, I_{Sink} = 2.0 mA)		—	0.15	0.4	
(V_{in} = 1.0 V, I_{Sink} = 0.1 mA)		—	—	0.1	
Output Sink Current (V_{in}, $\overline{\text{Reset}}$ = 4.0 V)	I_{Sink}	10	27	60	mA
Output Off-State Leakage (V_{in}, $\overline{\text{Reset}}$ = 5.0 V)	I_{OH}	—	0.02	0.5	µA
Clamp Diode Forward Voltage, Pin 1 to 2 (I_F = 10 mA)	V_F	0.6	0.9	1.2	V
TOTAL DEVICE					
Operating Input Voltage Range	V_{in}	1.0 to 6.5	—	—	V
Quiescent Input Current (V_{in} = 5.0 V)	I_{in}	—	390	500	µA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34064, –40°C for MC33064 T_{high} = +70°C for MC34064, +85°C for MC33064

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Figure 1. $\overline{\text{RESET}}$ Output Voltage versus Input Voltage

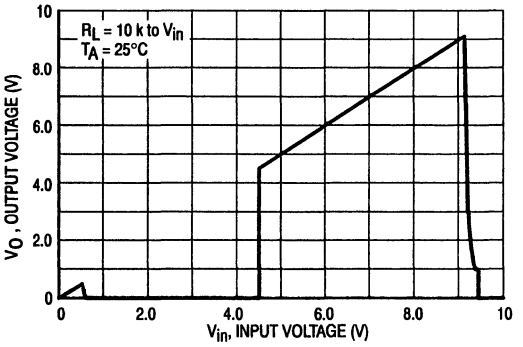


Figure 2. $\overline{\text{RESET}}$ Output Voltage versus Input Voltage

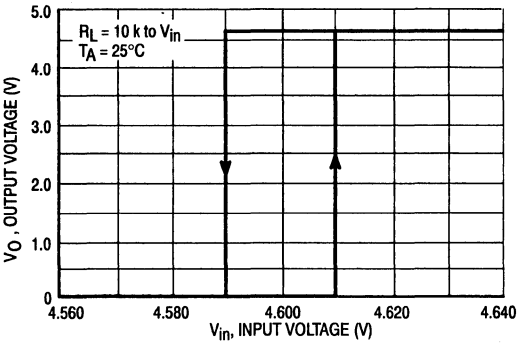


Figure 3. Comparator Threshold Voltage versus Temperature

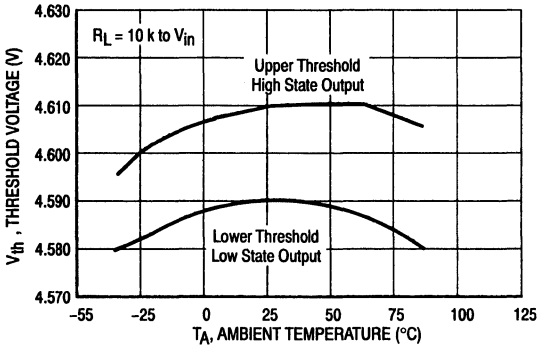


Figure 4. Input Current versus Input Voltage

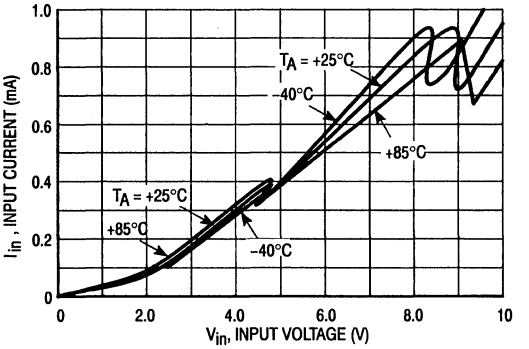


Figure 5. $\overline{\text{RESET}}$ Output Saturation versus Sink Curren

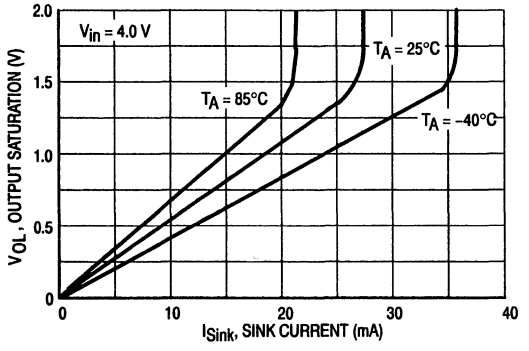


Figure 6. $\overline{\text{RESET}}$ Delay Time

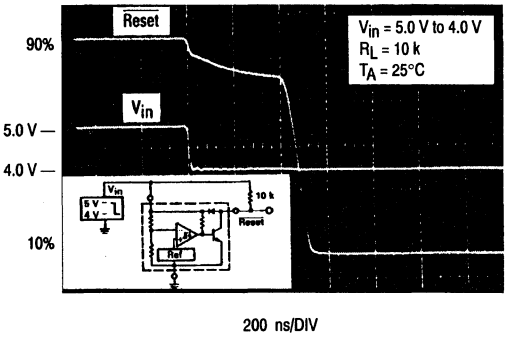


Figure 7. Clamp Diode Forward Current versus Voltage

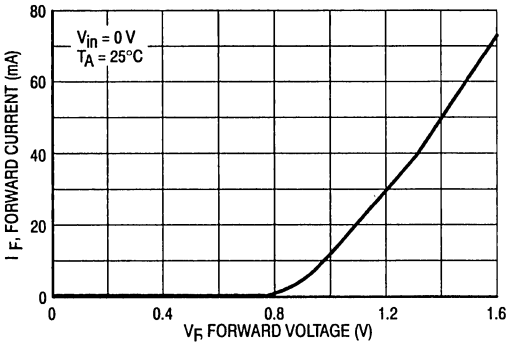
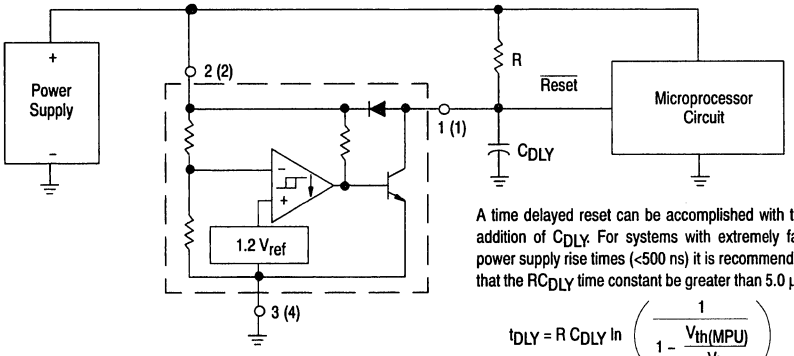


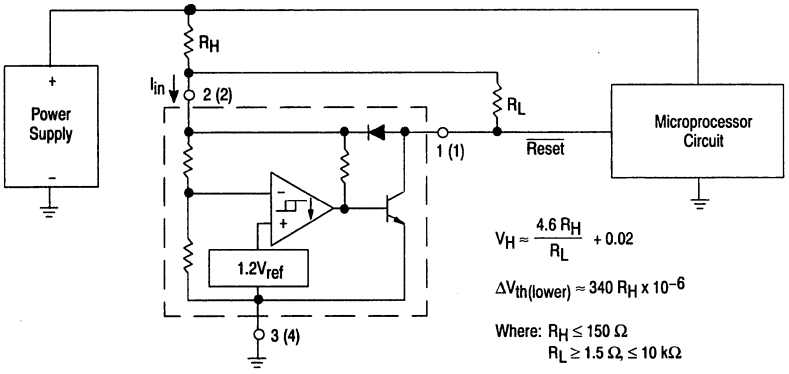
Figure 8. Low Voltage Microprocessor Reset



A time delayed reset can be accomplished with the addition of C_{DLY}. For systems with extremely fast power supply rise times (<500 ns) it is recommended that the RC_{DLY} time constant be greater than 5.0 µs.

$$t_{DLY} = R\,C_{DLY}\,\ln\left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{in}}}\right)$$

Figure 9. Low Voltage Microprocessor Reset with Additional Hysteresis



$$V_H \approx \frac{4.6\,R_H}{R_L} + 0.02$$

$$\Delta V_{th(lower)} \approx 340\,R_H \times 10^{-6}$$

Where: $R_H \leq 150\ \Omega$

$R_L \geq 1.5\ \Omega, \leq 10\ k\Omega$

Comparator hysteresis can be increased with the addition of resistor R_H. The hysteresis equation has been simplified and does not account for the change of input current I_{in} as V_{CC} crosses the comparator threshold (Figure 4). An increase of the lower threshold $\Delta V_{th(lower)}$ will be observed due to I_{in} which is typically 340 µA at 4.59 V. The equations are accurate to ±10% with R_H less than 150 Ω and R_L between 1.5 kΩ and 10 kΩ.

TEST DATA			
V_H (mV)	ΔV_{th} (mV)	R_H (Ω)	R_L (kΩ)
20	0	0	0
51	3.4	10	1.5
40	6.8	20	4.7
81	6.8	20	1.5
71	10	30	2.7
112	10	30	1.5
100	16	47	2.7
164	16	47	1.5
190	34	100	2.7
327	34	100	1.5
276	51	150	2.7
480	51	150	1.5

Figure 10. Voltage Monitor

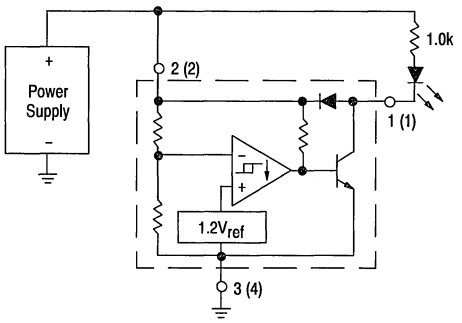


Figure 11. Solar Powered Battery Charger

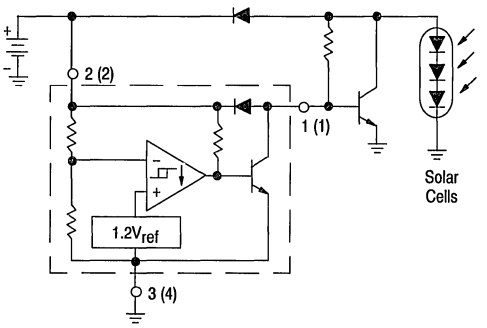
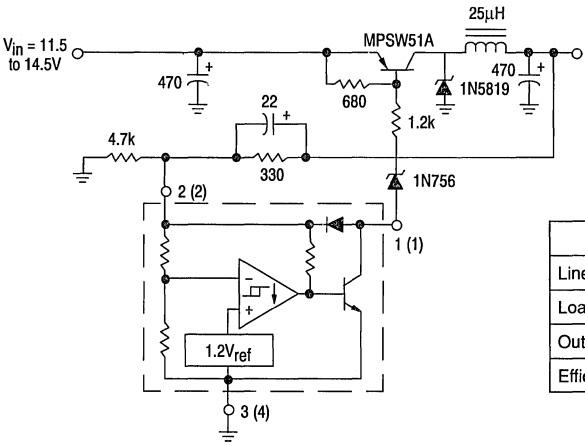
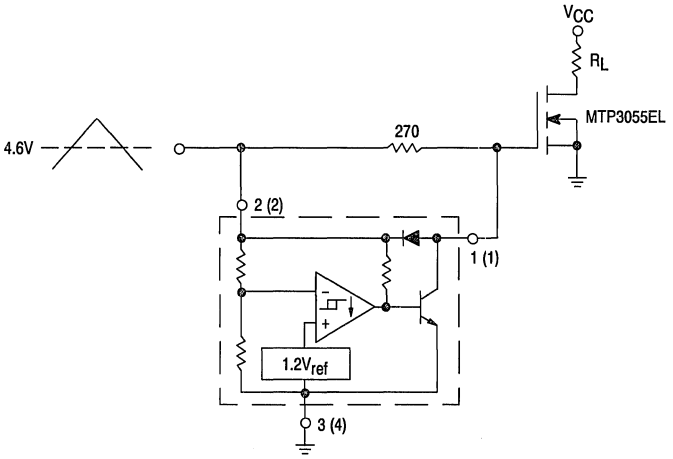


Figure 12. Low Power Switching Regulator



Test	Conditions	Results
Line Regulation	V_{in} = 11.5 V to 14.5 V, I_O = 50 mA	35 mV
Load Regulation	V_{in} = 12.6 V, I_O = 0 mA to 50 mA	12 mV
Output Ripple	V_{in} = 12.6 V, I_O = 50 mA	60 mV_{p-p}
Efficiency	V_{in} = 12.6 V, I_O = 50 mA	77%

Figure 13. MOSFET Low Voltage Gate Drive Protection



Overheating of the logic level power MOSFET due to insufficient gate voltage can be prevented with the above circuit. When the input signal is below the 4.6 V threshold of the MC34064, its output grounds the gate of the L^2 MOSFET.

MC34065-H,L
MC33065-H,L

Advance Information

High Performance Dual Channel Current Mode Controller

HIGH PERFORMANCE DUAL CHANNEL CURRENT MODE CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

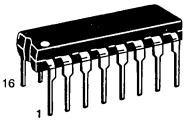
The MC34065-H,L series are high performance, fixed frequency, dual current mode controllers. They are specifically designed for off-line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a unique oscillator for precise duty cycle limit and frequency control, a temperature compensated reference, two high gain error amplifiers, two current sensing comparators, Drive Output 2 Enable pin, and two high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, and a latch for single pulse metering of each output. These devices are available in dual-in-line and surface mount packages.

The MC34065-H has UVLO thresholds of 14 V (on) and 10 V (off), ideally suited for off-line converters. The MC34065-L is tailored for lower voltage applications having UVLO thresholds of 8.4 V (on) and 7.8 V (off).

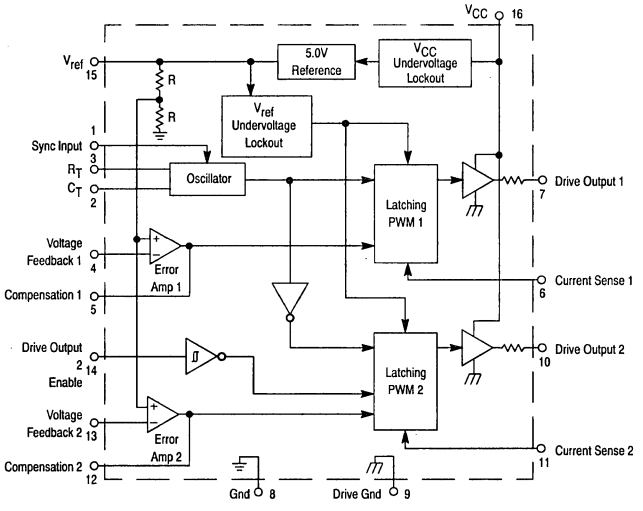
- Unique Oscillator for Precise Duty Cycle Limit and Frequency Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Separate Latching PWMs for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- Drive Output 2 Enable Pin
- Two High Current Totem Pole Outputs
- Input Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current

P SUFFIX
PLASTIC PACKAGE
CASE 648

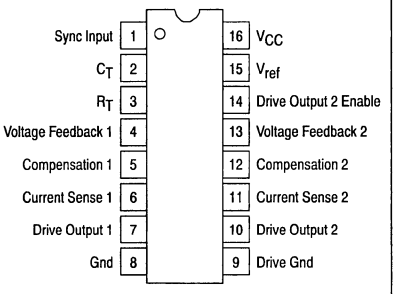


DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SOP-8+8L)

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34065DW-H	0° to +70°C	SOP-8+8L
MC34065DW-L		
MC34065P-H		Plastic DIP
MC34065P-L		
MC33065DW-H	– 40° to +85°C	SOP-8+8L
MC33065DW-L		
MC33065P-H		Plastic DIP
MC33065P-L		

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Output Current, Source or Sink (Note 1)	I_O	400	mA
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense, Enable, and Voltage Feedback Inputs	V_{in}	– 0.3 to +5.5	V
Sync Input High State (Voltage) Low State (Reverse Current)	 V_{IH} I_{IL}	 +5.5 – 5.0	 V mA
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics DW Suffix, Plastic Package Case 751G Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction to Air P Suffix, Plastic Package Case 648 Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34065 MC33065	T_A	0 to +70 – 40 to +85	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERICISTICS (V_{CC} = 15 V [Note 2], R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies to [Note 3].)

Characteristics		Symbol	Min	Typ	Max	Unit
REFERENCE SECTION						
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)		V_{ref}	4.85	5.0	5.13	V
Line Regulation (V_{CC} = 11 V to 20 V)		Reg_{line}	—	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 10 mA, V_{CC} = 20 V)		Reg_{load}	—	3.0	25	mV
Total Output Variation over Line, Load, and Temperature		V_{ref}	4.8	—	5.15	V
Output Short Circuit Current		I_{SC}	30	100	—	mA
OSCILLATOR AND PWM SECTIONS						
Total Frequency Variation over Line and Temperature V_{CC} = 11 V to 20 V, T_A = T_{low} to T_{high}	 MC34065 MC33065	f_{osc}	 46.5 45	 49 49	 51.5 53	kHz
Frequency Change with Voltage (V_{CC} = 11 V to 20 V)		$\Delta f_{osc}/\Delta V$	—	0.2	1.0	%
Duty Cycle at each Output	Maximum Minimum	DC_{max} DC_{min}	46 —	49.5 —	52 0	%
Sync Input Current High State (V_{in} = 2.4 V) Low State (V_{in} = 0.8 V)		 I_{IH} I_{IL}	 — —	 170 80	 250 160	μA
ERROR AMPLIFIERS						
Voltage Feedback Input (V_O = 2.5 V)		V_{FB}	2.45	2.5	2.55	V
Input Bias Current (V_{FB} = 5.0 V)		I_{IB}	—	– 0.1	– 1.0	μA
Open-Loop Voltage Gain (V_O = 2.0 V to 4.0 V)		A_{VOL}	65	100	—	dB
Unity Gain Bandwidth (T_J = 25°C)		BW	0.7	1.0	—	MHz
Power Supply Rejection Ratio (V_{CC} = 11 V to 20 V)		PSRR	60	90	—	dB
Output Current Source (V_O = 3.0 V, V_{FB} = 2.3 V) Sink (V_O = 1.2 V, V_{FB} = 2.7 V)		 I_{source} I_{sink}	 0.45 2.0	 1.0 12	 — —	mA
Output Voltage Swing High State (R_L = 15 k to ground, V_{FB} = 2.3 V) Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)		 V_{OH} V_{OL}	 5.0 —	 6.2 0.8	 — 1.1	V

ELECTRICAL CHARACTERICISTICS (V_{CC} = 15 V [Note 2], R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies to [Note 3].)

Characteristics	Symbol	Min	Typ	Max	Unit
CURRENT SENSE SECTION					
Current Sense Input Voltage Gain (Notes 4 and 5)	A_V	2.75	3.0	3.25	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	V
Input Bias Current	I_{IB}	—	– 2.0	– 10	μA
Propagation Delay (Current Sense Input to Output)	$t_{PLN(In/Out)}$	—	150	300	ns
DRIVE OUTPUT 2 ENABLE PIN					
Enable Pin Voltage — High State (Output 2 Enabled) — Low State (Output 2 Disabled)	V_{IH} V_{IL}	3.5 0	— —	V_{ref} 1.5	V
Low State Input Current (V_{IL} = 0 V)	I_{IB}	100	250	400	μA
DRIVE OUTPUTS					
Output Voltage — Low State (I_{sink} = 20 mA) (I_{sink} = 200 mA) — High State (I_{source} = 20 mA) (I_{source} = 200 mA)	V_{OL} V_{OH} 	— 1.6 12.8 10	0.3 2.4 13.3 11.2	0.5 3.0 — 12.3	V
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	—	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	—	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	—	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION					
Start-Up Threshold (V_{CC} Increasing) -L Suffix -H Suffix	V_{th}	 7.8 13	 8.4 14	 9.0 15	V
Minimum Operating Voltage After Turn-On (V_{CC} Decreasing) -L Suffix -H Suffix	$V_{CC(min)}$	 7.2 9.0	 7.8 10	 8.4 11	V
TOTAL DEVICE					
Power Supply Current Start-Up -L Suffix (V_{CC} = 6.0 V) -H Suffix (V_{CC} = 12 V) Operating (Note 2)	I_{CC}	 — — —	 0.4 0.6 20	 0.8 1.0 25	mA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the start-up threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible:
T_{low} = 0°C for the MC34065, T_{high} = +70°C for MC34065
T_{low} = −40°C for the MC33065, T_{high} = +85°C for MC33065
4. This parameter is measured at the latch trip point with V_{FB} = 0 V
5. Comparator gain is defined as AV = $\frac{\Delta V \text{ Compensation}}{\Delta V \text{ Current Sense}}$

Figure 1. Timing Resistor versus Oscillator Frequency

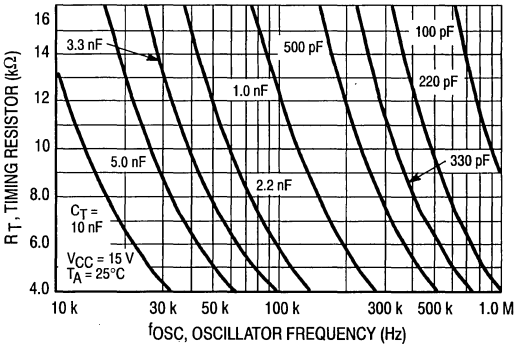


Figure 2. Maximum Output Duty Cycle versus Oscillator Frequency

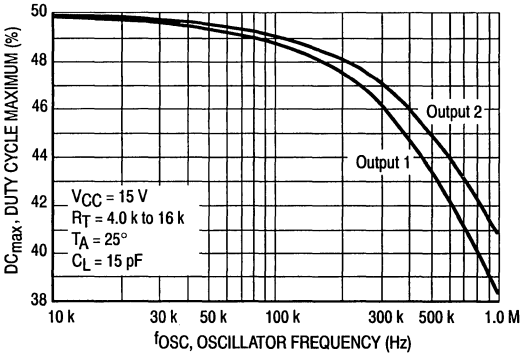


Figure 3. Error Amp Small-Signal Transient Response

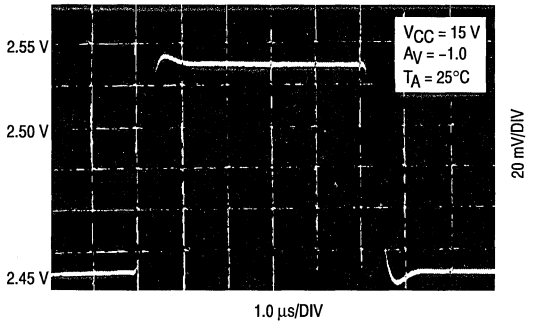


Figure 4. Error Amp Large-Signal Transient Response

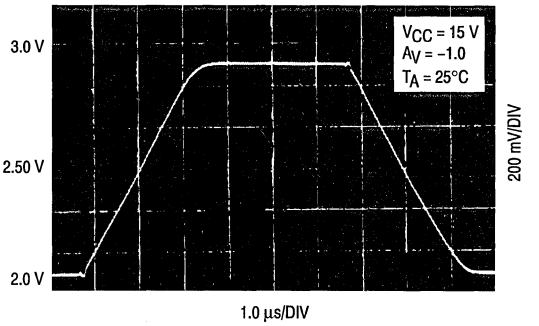


Figure 5. Error Amp Open-Loop Gain and Phase versus Frequency

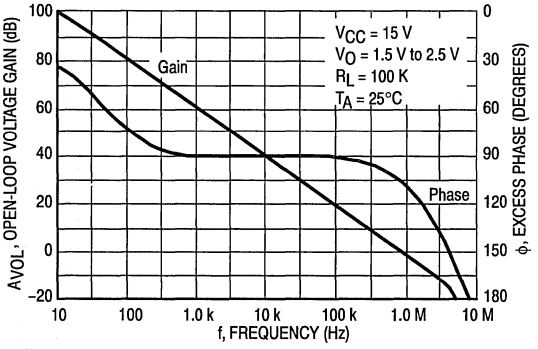


Figure 6. Current Sense Input Threshold versus Error Amp Output Voltage

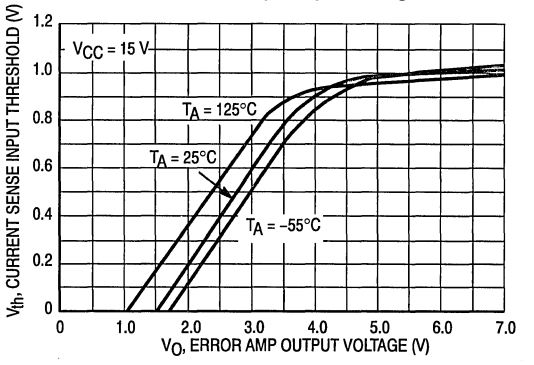


Figure 7. Reference Voltage Change versus Source Current

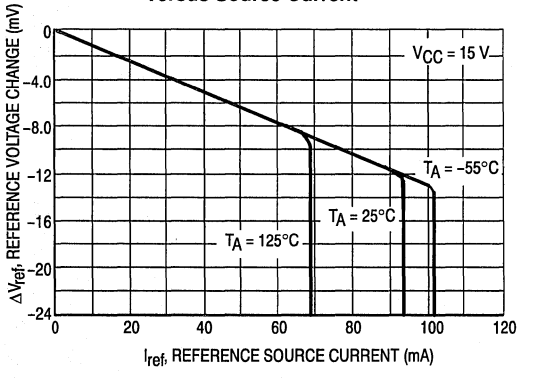


Figure 8. Reference Short Circuit Current versus Temperature

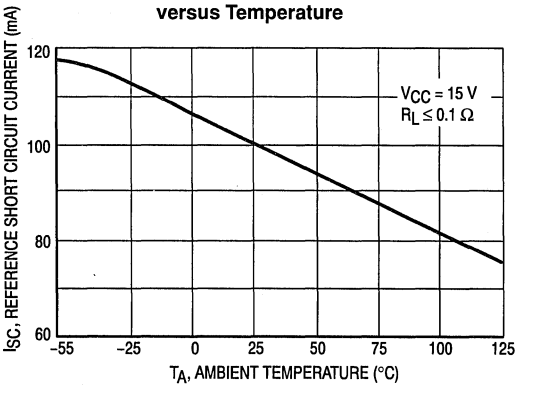


Figure 9. Reference Load Regulation

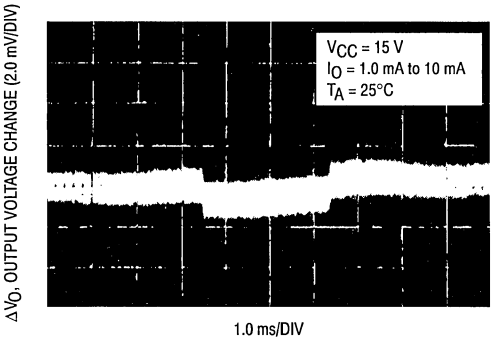


Figure 10. Reference Line Regulation

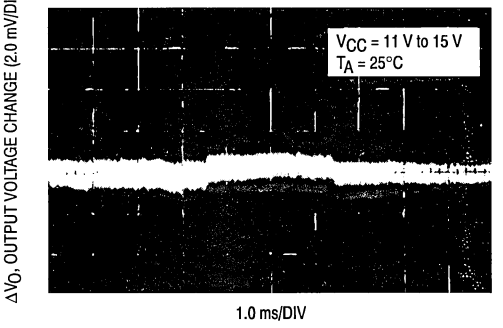


Figure 11. Output Saturation Voltage versus Load Current

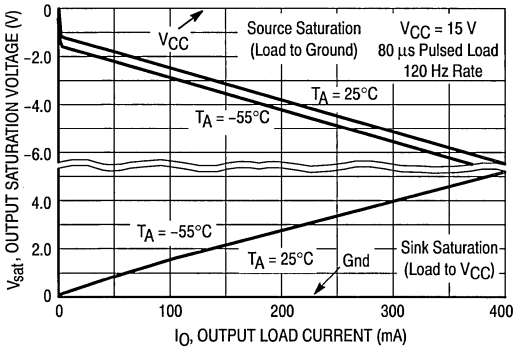


Figure 12. Output Waveform

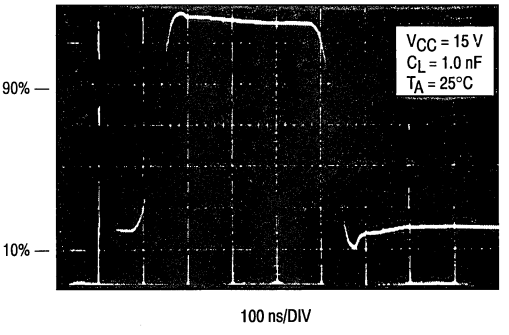


Figure 13. Output Cross Conduction Current

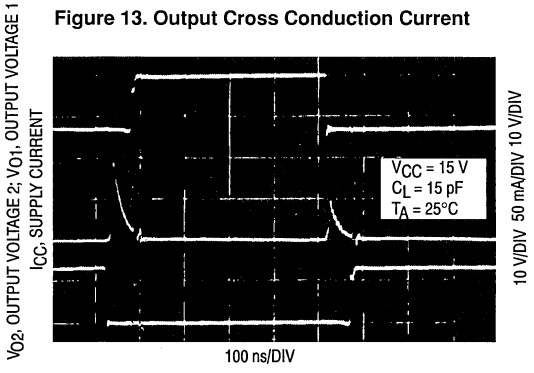
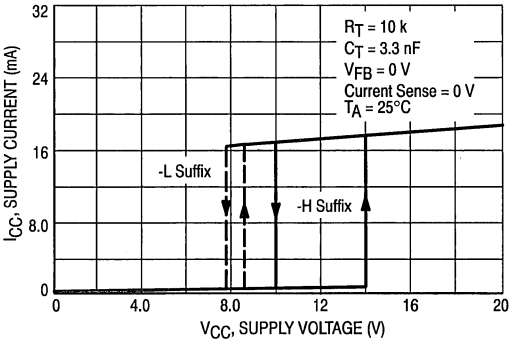


Figure 14. Supply Current versus Supply Voltage



OPERATING DESCRIPTION

The MC34065-H,L series are high performance, fixed frequency, dual channel current mode controllers specifically designed for Off-Line and DC-to-DC converter applications. These devices offer the designer a cost effective solution with minimal external components where independent regulation of two power converters is required. The Representative Block Diagram is shown in Figure 15. Each channel contains a high gain error amplifier, current sensing comparator, pulse width modulator latch, and totem pole output driver. The oscillator, reference regulator, and undervoltage lock-out circuits are common to both channels.

Oscillator

The unique oscillator configuration employed features precise frequency and duty cycle control. The frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink, generating a symmetrical 50 percent duty cycle waveform at Pin 2. The oscillator peak and valley thresholds are 3.5 V and 1.6 V respectively. The source/sink current magnitude is controlled by resistor R_T. For proper operation over temperature it must be in the range of 4.0 kΩ to 16 kΩ as shown in Figure 1.

As C_T charges and discharges, an internal blanking pulse is generated that alternately drives the center inputs of the upper and lower NOR gates high. This, in conjunction with a precise amount of delay time introduced into each channel, produces well defined non-overlapping output duty cycles. Output 2 is enabled while C_T is charging, and Output 1 is enabled during the discharge. Figure 2 shows the Maximum Output Duty Cycle versus Oscillator Frequency. Note that even at 500 kHz, each output is capable of approximately 44% on-time, making this controller suitable for high frequency power conversion applications.

In many noise sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal as shown in Figure 17. For reliable locking, the free-running oscillator frequency should be set about 10% less than the clock frequency. Referring to the timing diagram shown in Figure 16, the rising edge of the clock signal applied to the Sync input, terminates charging of C_T and Drive Output 2 conduction. By tailoring the clock waveform symmetry, accurate duty cycle clamping of either output can be achieved. A circuit method for this, and multi unit synchronization, is shown in Figure 18.

Error Amplifier

Each channel contains a fully-compensated Error Amplifier with access to the inverting input and output. The amplifier features a typical DC voltage gain of 100 dB, and a unity gain bandwidth of 1.0 MHz with 71° of phase margin (Figure 5). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input through a resistor divider. The maximum input bias current is –1.0 μA which will cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp output (Pin 5, 12) is provided for external loop compensation. The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no pulses appear at the Drive Output (Pin 7, 10) when the error amplifier output is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figures 20, 21).

The minimum allowable Error Amp feedback resistance is limited by the amplifier's source current (0.5 mA) and the output voltage (V_{OH}) required to reach the comparator's 1.0 V clamp level with the inverting input at ground. This condition happens during initial system startup or when the sensed output is shorted:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The MC34065 operates as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output. Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator-PWM Latch configuration used ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting a ground-referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 6, 11) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 5, 12 where:

$$I_{pk} = \frac{V_{(Pin\ 5,\ 12)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it may be desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense input with a time constant that approximates the spike duration will usually eliminate the instability, refer to Figure 24.

Undervoltage Lockout

Two Undervoltage Lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stages are enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 14 V/10 V for -H suffix, and 8.4 V/7.6 V for -L suffix. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V respectively. The large hysteresis and low start-up current of the -H suffix version makes it ideally suited in off-line converter applications where efficient bootstrap start-up techniques are required (Figure 28). The -L suffix version is intended for lower voltage DC-to-DC converter applications. The minimum operating voltage for the -H suffix is 11 V and 8.2 V for the -L suffix.

Drive Outputs and Drive Ground

Each section contains a single totem-pole output stage that is specifically designed for direct drive of power MOSFETs. The Drive Outputs are capable of up to ±400 mA peak current with a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the outputs in a sinking mode whenever an Undervoltage Lockout is active. This characteristic eliminates the need for an external pull-down resistor. The totem-pole output has been optimized to minimize cross-conduction current in high speed operation. The addition of two 10 Ω resistors, one in series with the source output transistor and one in series with the sink output transistor, reduces the cross-conduction current to minimal levels, as shown in Figure 13.

Although the Drive Outputs were optimized for MOSFETs, they can easily supply the negative base current required by bipolar NPN transistors for enhanced turn-off (Figure 25).

Figure 15. Representative Block Diagram

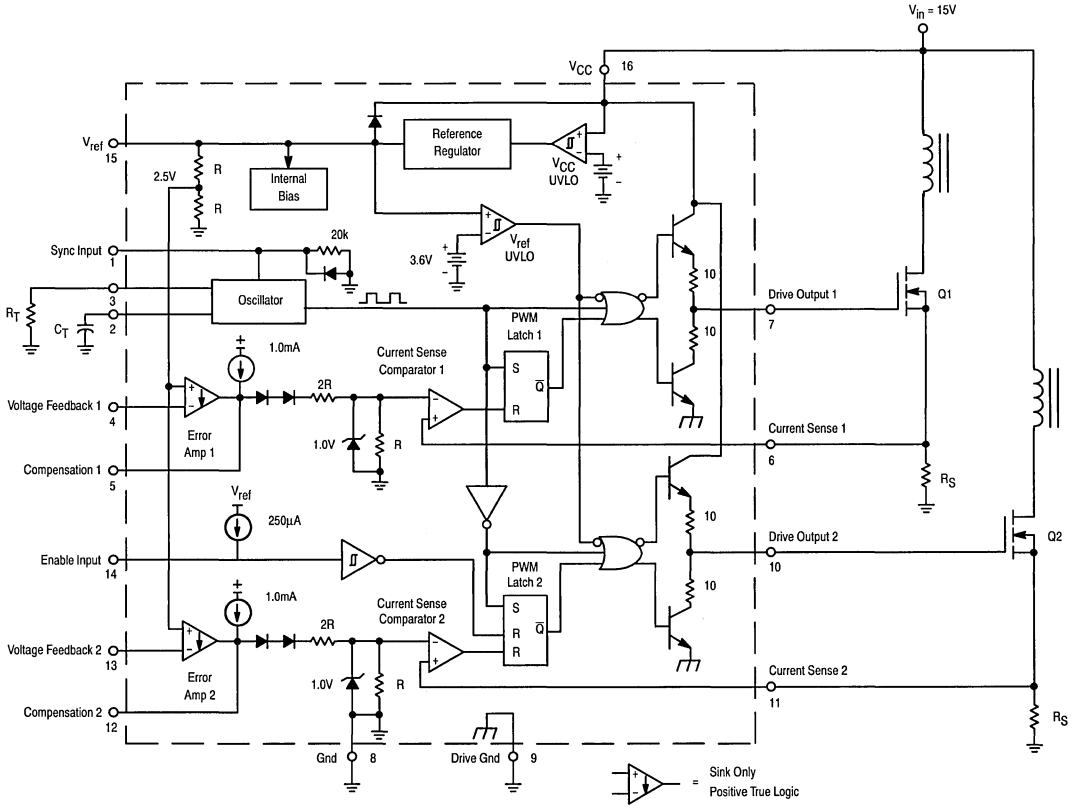
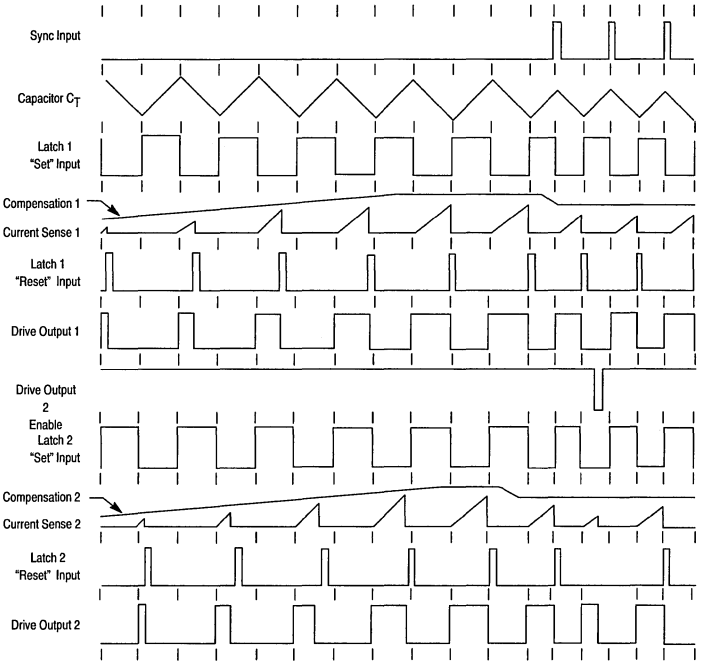


Figure 16. Timing Diagram



The outputs do not contain internal current limiting, therefore an external series resistor may be required to prevent the peak output current from exceeding the ±400 mA maximum rating. The sink saturation (V_{OL}) is less than 0.75 V at 50 mA.

A separate Drive Ground pin is provided and, with proper implementation, will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. Figure 23 shows the proper ground connections required for current sensing power MOSFET applications.

Drive Output 2 Enable Pin

This input is used to enable Drive Output 2. Drive Output 1 can be used to control circuitry that must run continuously such as volatile memory and the system clock, or a remote controlled receiver, while Drive Output 2 controls the high power circuitry that is occasionally turned off.

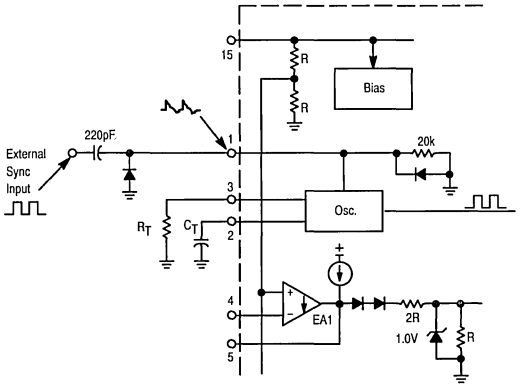
Reference

The 5.0 V bandgap reference is trimmed to ±2.0% tolerance at T_J = 25°C. The reference has short circuit protection and is capable of providing in excess of 30 mA for powering any additional control system circuitry.

Design Considerations

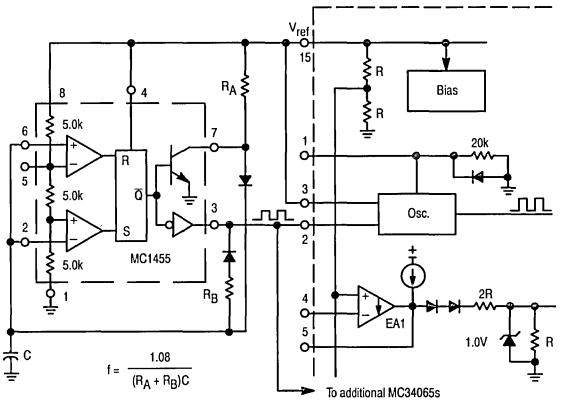
Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC} and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage-divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

Figure 17. External Clock Synchronization



The external diode clamp is required if the negative Sync current is greater than –5.0 mA.

Figure 18. External Duty Cycle Clamp and Multi Unit Synchronization



$$f = \frac{1.08}{(R_A + R_B)C}$$

$$D_{max}\ \text{Drive Output 1} = \frac{R_B}{R_A + R_B}$$

$$D_{max}\ \text{Drive Output 2} = \frac{R_A}{R_A + R_B}$$

PIN DESCRIPTION

Pin #	Function	Description
1	Sync Input	A narrow rectangular waveform applied to this input will synchronize the oscillator. A DC voltage within the range of 2.4 V to 5.5 V will inhibit the oscillator.
2	C_T	Timing capacitor C_T connects from this pin to ground setting the free-running oscillator frequency range.
3	R_T	Resistor R_T connects from this pin to ground precisely setting the charge current for C_T. R_T must be between 4.0 k and 16 k.
4	Voltage Feedback 1	This pin is the inverting input of Error Amplifier 1. It is normally connected to the switching power supply output through a resistor divider.
5	Compensation 1	This pin is the output of Error Amplifier 1 and is made available for loop compensation.
6	Current Sense 1	A voltage proportional to the inductor current is connected to this input. PWM 1 uses this information to terminate conduction of output switch Q1.
7	Drive Output 1	This pin directly drives the gate of a power MOSFET Q1. Peak currents up to 400 mA are sourced and sunk by this pin.
8	Gnd	This pin is the control circuitry ground return and is connected back to the source ground.
9	Drive Gnd	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
10	Drive Output 2	This pin directly drives the gate of a power MOSFET Q2. Peak currents up to 400 mA are sourced and sunk by this pin.
11	Current Sense 2	A voltage proportional to inductor current is connected to this input. PWM 2 uses this information to terminate conduction of output switch Q2.
12	Compensation 2	This pin is the output of Error Amplifier 2 and is made available for loop compensation.
13	Voltage Feedback 2	This pin is the inverting input of Error Amplifier 2. It is normally connected to the switching power supply output through a resistor divider.
14	Drive Output 2 Enable	A logic low at this input disables Drive Output 2.
15	V_{ref}	This is the 5.0 V reference output. It can provide bias for any additional system circuitry.
16	V_{CC}	This pin is the positive supply of the control IC. The minimum operating voltage range after start-up is 11 V to 15.5 V for the -H suffix, 8.2 V to 9.5 V for the -L suffix.

Figure 19. Adjustable Reduction of Clamp Level

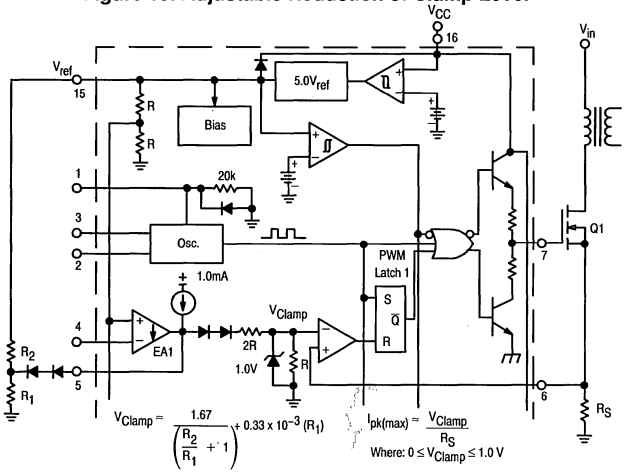


Figure 20. Soft-Start Circuit

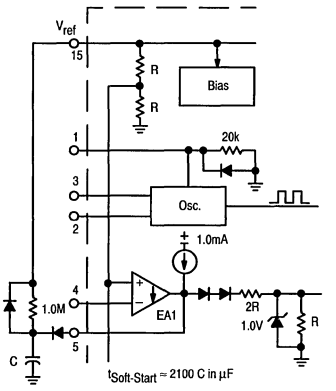


Figure 21. Adjustable Reduction of Clamp Level with Soft-Start

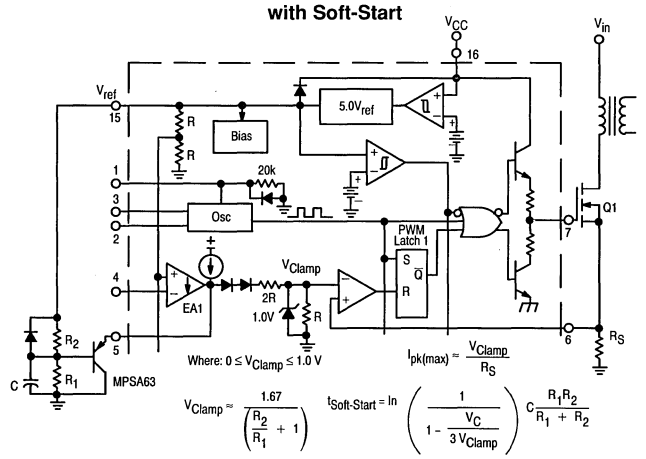
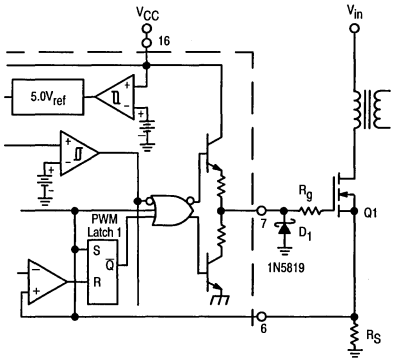
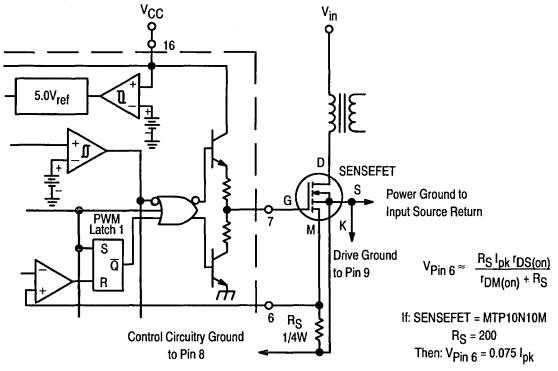


Figure 22. MOSFET Parasitic Oscillations



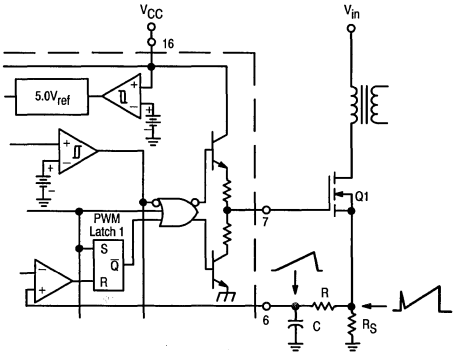
Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D_1 is required if circuit ringing drives the output pin below ground.

Figure 23. Current Sensing Power MOSFET



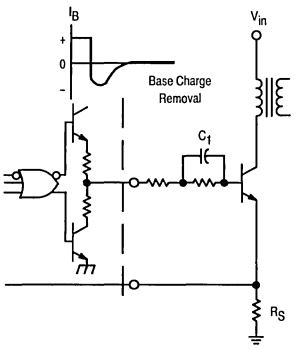
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 19 and 21.

Figure 24. Current Waveform Spike Suppression



The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 25. Bipolar Transistor Drive



The totem-pole outputs can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1.

Figure 26. Isolated MOSFET Drive

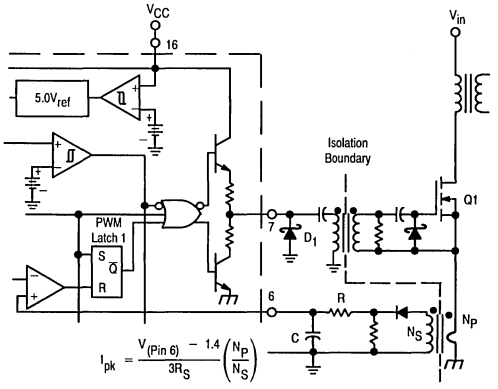
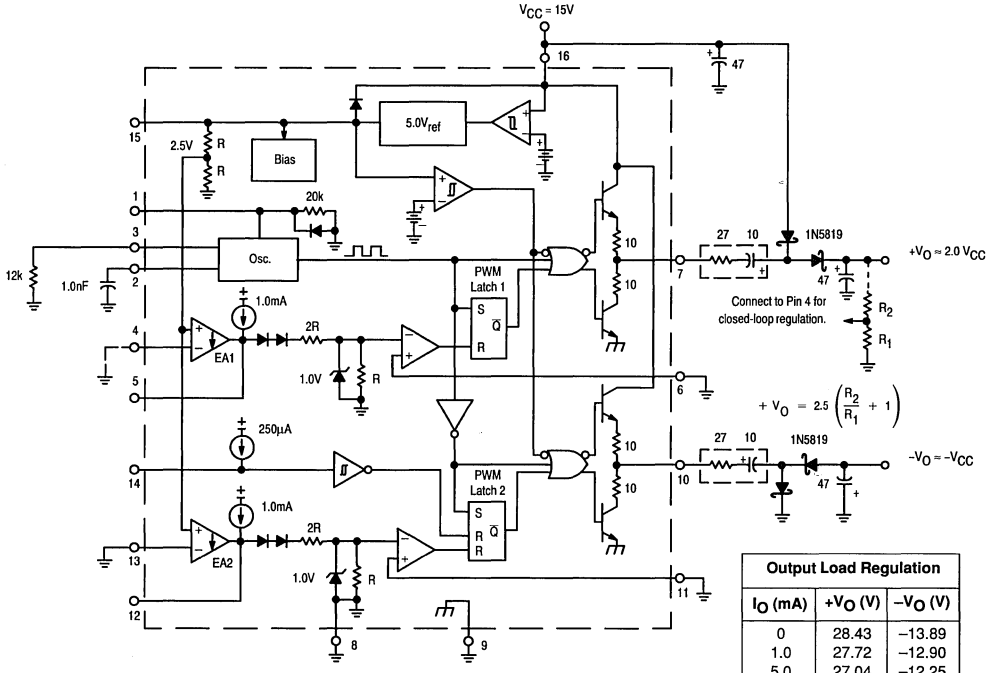


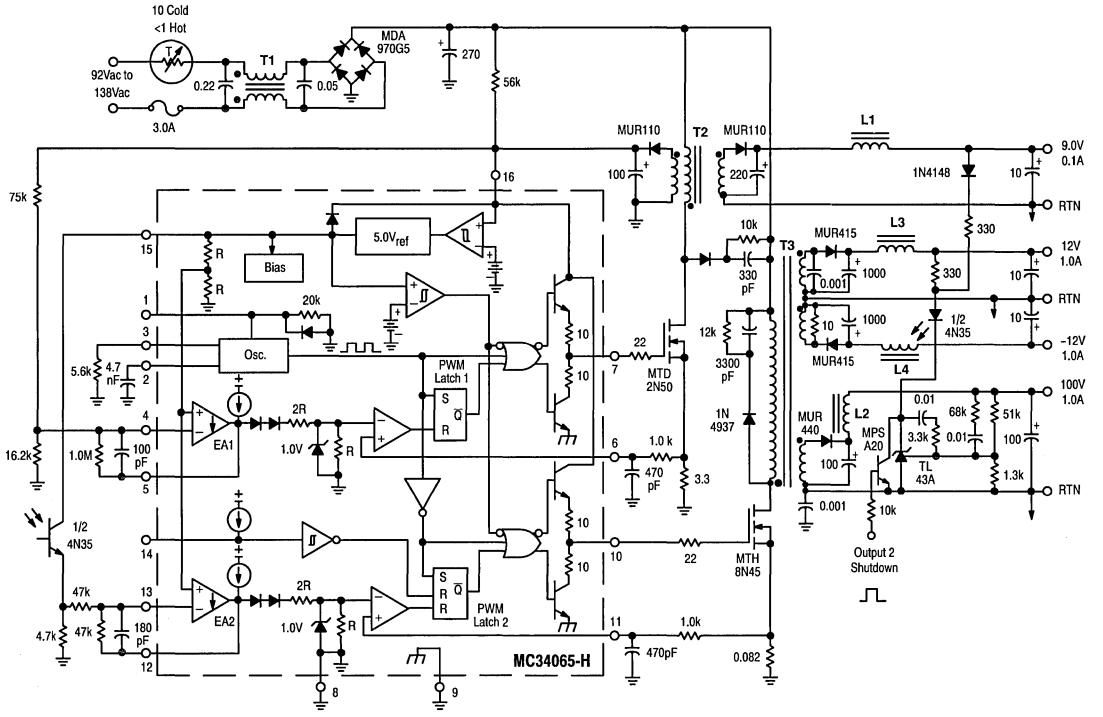
Figure 27. Dual Charge Pump Converter



Output Load Regulation		
I_O (mA)	$+V_O$ (V)	$-V_O$ (V)
0	28.43	–13.89
1.0	27.72	–12.90
5.0	27.04	–12.25
10	26.20	–11.44
50	20.52	–5.80

The capacitor's equivalent series resistance must limit the Drive Output current to 400 mA. An additional series resistor may be required when using tantalum or other low ESR capacitors. The positive output can provide excellent line and load regulation by connecting the R_2/R_1 resistor divider as shown.

Figure 28. 125 Watt Off-Line Converter



Test	Conditions	Results
Line Regulation 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 92 Vac to 138 Vac I_O = 1.0 A I_O = ±1.0 A I_O = 0.1 A	 Δ = 40 mV or ±0.02% Δ = 32 mV or ±0.13% Δ = 55 mV or ±0.31%
Load Regulation 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac I_O = 0.25 A to 1.0 A I_O = ±0.25 A to ±1.0 A I_O = 0.08 A to 0.1 A	 Δ = 50 mV or ±0.025% Δ = 320 mV or ±1.2% Δ = 234 mV or ±1.3%
Output Ripple 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac I_O = 1.0 A I_O = ±1.0 A I_O = 0.1 A	 40 mVp-p 100 mVp-p 60 mVp-p
Short Circuit Current 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac, R_L = 0.1 Ω	 4.3 A 17 A Output Hiccups
Efficiency	V_{in} = 115 Vac, P_O = 125 W	86%

T1 — 468 µH per section at 2.5 A, Coilcraft E3496A.

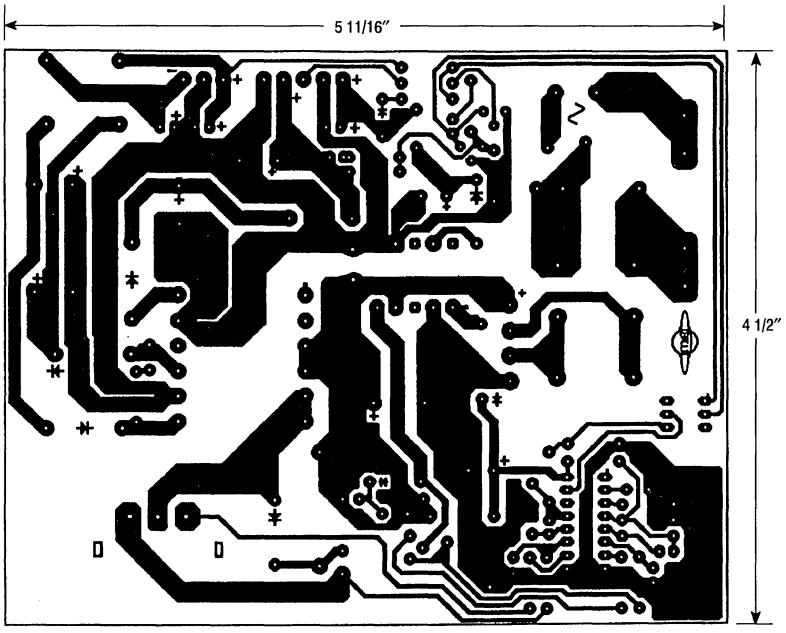
T2 — Primary: 156 Turns, #34 AWG
Primary Feedback: 19 Turns, #34 AWG
Secondary: 17 Turns, #28 AWG
Core: TDK PC30 EE22-Z
Bobbin: BE22-118CP
Gap: ≈0.001″ for a primary inductance of 6.8 mH

T3 — Primary: 56 Turns, #23 AWG (2 strands) Bifiliar Wound
Secondary: ±12 V, 4 Turns, #23 AWG (4 strands) Quadfiliar Wound
Secondary 100 V: 32 Turns, #23 AWG (2 strands) Bifiliar Wound
Core: TDK PC30 EER40 G0.76
Bobbin: BEER40-1112CP
Gap: ≈0.030″ for a primary inductance of 212 µH

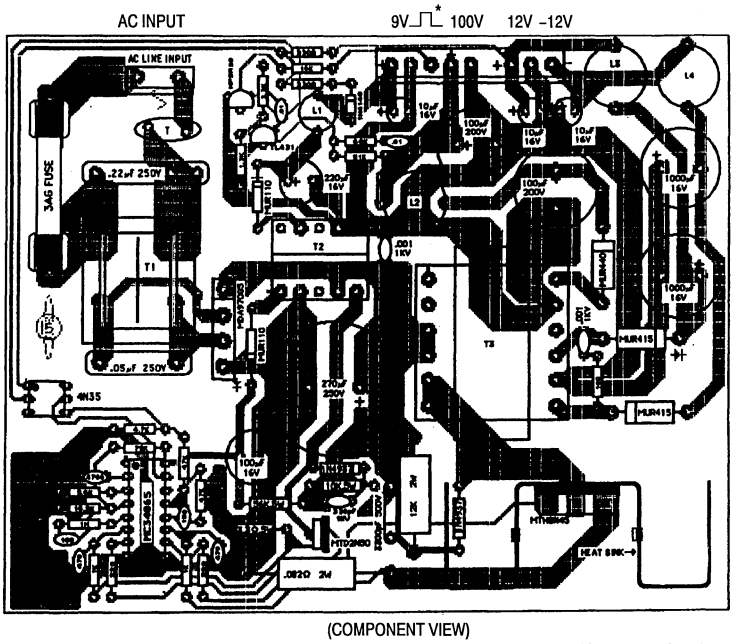
L1, L3, L4 — 25 µH at 1.0 A, Coilcraft Z7157.

L2 — 10 µH at 3.0 A, Coilcraft PCV-0-010-03.

Figure 29. PC Board Circuit Side and Component View



(CIRCUIT VIEW)



(COMPONENT VIEW)

*100 V and ±12 V Shutdown

MC34066
MC33066

3

Product Preview

High Performance Resonant Mode Controller

HIGH PERFORMANCE RESONANT MODE CONTROLLER

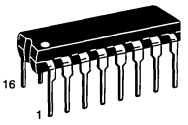
SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC34066 series are high performance resonant mode controllers designed for Off-Line and DC-to-DC converter applications that utilize frequency modulated constant on-time or constant off-time control. These integrated circuits feature a variable frequency oscillator with programmable deadtime, precision retriggerable one-shot timer, temperature compensated reference, high gain wide-bandwidth error amplifier with a precision output clamp, steering flip-flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

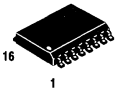
Also included are protective features consisting of a high speed fault comparator and latch, programmable soft-start circuitry, input undervoltage lockout with selectable thresholds, and reference undervoltage lockout.

These devices are available in dual-in-line and surface mount packages.

- Variable Frequency Oscillator with a Control Range Exceeding 1000:1
- Programmable Oscillator Deadtime Allows Constant Off-Time Operation
- Precision Retriggerable One-Shot Timer
- Internally Trimmed Bandgap Reference
- 5.0 MHz Error Amplifier with Precision Output Clamp
- Dual High Current Totem Pole Outputs
- Selectable Undervoltage Lockout Thresholds with Hysteresis
- Enable Input
- Programmable Soft-Start Circuitry
- Low Start-Up Current for Off-Line Operation

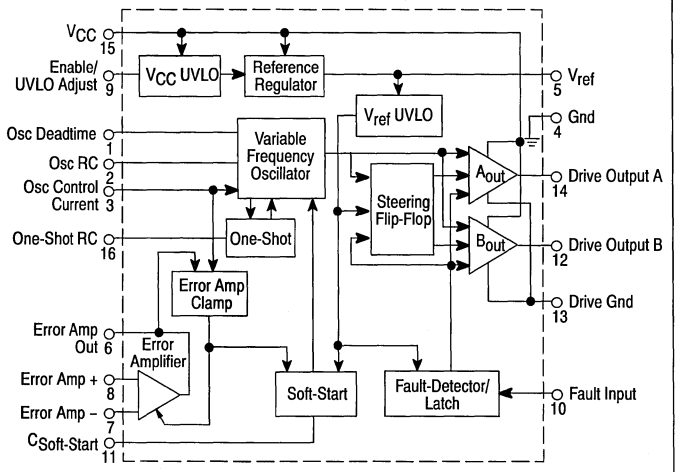


P SUFFIX
PLASTIC PACKAGE
CASE 648

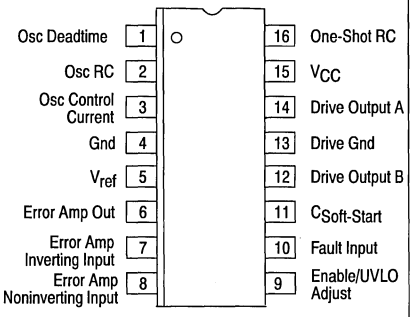


DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO-16)

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34066DW	0° to +70°C	SO-16
MC34066P		Plastic DIP
MC33066DW	–40° to +85°C	SO-16
MC33066P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	V_{CC}	20	V
Drive Output Current, Source or Sink (Note 1) Continuous Pulsed (0.5 μs, 25% Duty Cycle)	I_O	 0.3 1.5	A
Error Amplifier, Fault, One-Shot, Oscillator, and Soft-Start Inputs	V_{in}	−1.0 to +6.0	V
UVLO Adjust Input	$V_{in(UVLO)}$	−1.0 to V_{CC}	V
Power Dissipation and Thermal Characteristics DW Suffix Package SO-16 Case 751G Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction to Air P Suffix Package Case 648 Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34066 MC33066	T_A	 0 to +70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERICISTICS (V_{CC} = 12 V [Note 2], R_{OSC} = 95.3 k, R_{DT} = 0 Ω, R_{VFO} = 5.62 k, C_{OSC} = 300 pF, R_T = 14.3 k, C_T = 300 pF, C_L = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 0 mA, T_A = 25°C)	V_{ref}	5.0	5.1	5.2	V
Line Regulation (V_{CC} = 10 V to 18 V)	Reg_{line}	—	1.0	20	mV
Load Regulation (I_O = 0 mA to 10 mA)	Reg_{load}	—	1.0	20	mV
Total Output Variation Over Line, Load, and Temperature	V_{ref}	4.9	—	5.3	mV
Output Short Circuit Current	I_O	25	100	190	mA
Reference Undervoltage Lockout Threshold	V_{th}	3.8	4.3	4.8	V
ERROR AMPLIFIER					
Input Offset Voltage (V_{CM} = 1.5 V)	V_{IO}	—	1.0	10	mV
Input Bias Current (V_{CM} = 1.5 V)	I_{IB}	—	0.2	1.0	μA
Input Offset Current (V_{CM} = 1.5 V)	I_{IO}	—	0	0.5	μA
Open-Loop Voltage Gain (V_{CM} = 1.5 V, V_O = 2.0 V)	A_{VOL}	70	100	—	dB
Gain Bandwidth Product (f = 100 kHz)	GBW	2.5	4.2	—	MHz
Input Common Mode Rejection Ratio (V_{CM} = 1.5 V to 5.0 V)	CMRR	70	95	—	dB
Power Supply Rejection Ratio (V_{CC} = 10 V to 18 V, f = 120 Hz)	PSRR	80	100	—	dB
Output Voltage Swing High State with Respect to Pin 3 (I_{Source} = 2.0 mA) Low State with Respect to Ground (I_{Sink} = 1.0 mA)	 V_{OH} V_{OL}	 2.1 —	 2.5 0.4	 2.9 0.6	V

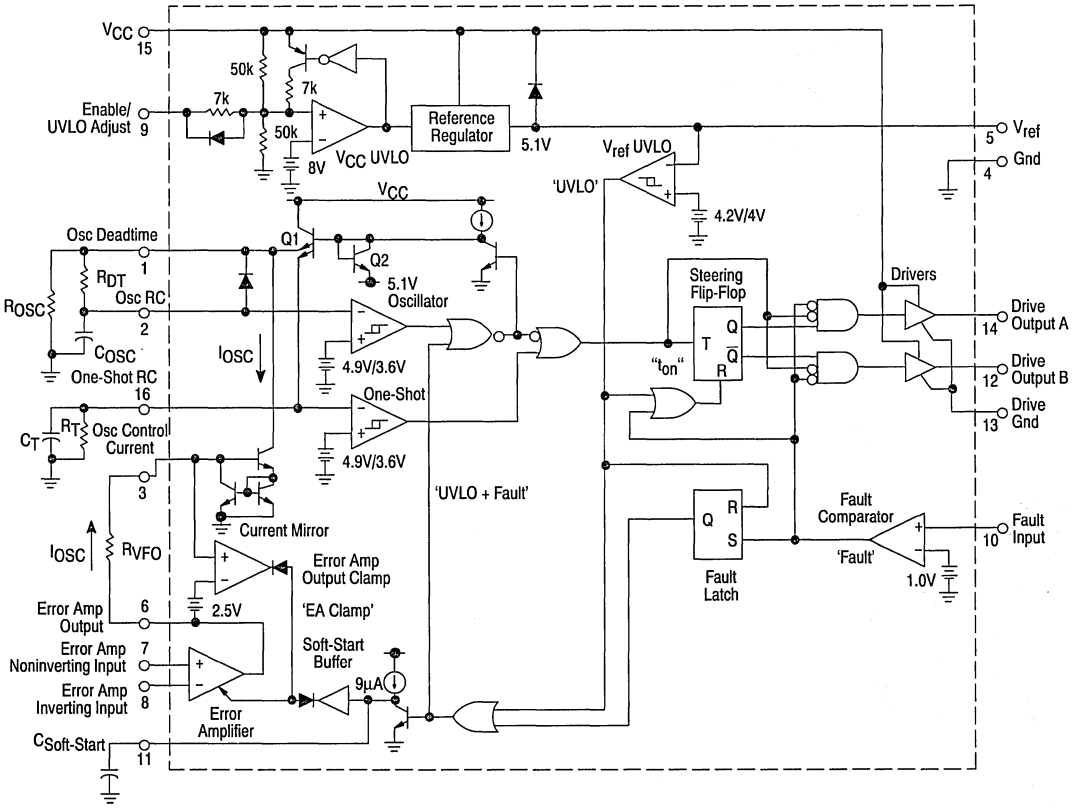
NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Start-Up threshold before setting to 12 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34066, −40°C for MC33066 T_{high} = +70°C for MC34066, +85°C for MC33066

ELECTRICAL CHARACTERICISTICS (Continued) (V_{CC} = 12 V [Note 2], R_{OSC} = 95.3 k, R_{DT} = 0 Ω, R_{VFO} = 5.62 k, C_{OSC} = 300 pF, R_T = 14.3 k, C_T = 300 pF, C_L = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (Error Amp Output Low) T_A = 25°C Total Variation (V_{CC} = 10 V to 18 V, T_A = T_{Low} to T_{High})	$f_{OSC(low)}$	 90 85	 100 —	 110 115	kHz
Frequency (Error Amp Output High) T_A = 25°C Total Variation (V_{CC} = 10 V to 18 V, T_A = T_{Low} to T_{High})	$f_{OSC(high)}$	 900 850	 1000 —	 1100 1150	kHz
Oscillator Control Input Voltage, Pin 3 (I_{Sink} = 0.5 mA, T_A = 25°C)	V_{in}	1.3	1.4	1.5	V
Output Deadtime (Error Amp Output High) R_{DT} = 0 Ω R_{DT} = 1.0 k	DT	 — 600	 70 700	 100 800	ns
ONE-SHOT					
Drive Output On-Time (R_{DT} = 1.0 k) T_A = 25°C Total Variation (V_{CC} = 10 V to 18 V, T_A = T_{Low} to T_{High})	t_{ON}	 1.43 1.4	 1.5 —	 1.57 1.6	µs
DRIVE OUTPUTS					
Output Voltage Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA) High State (I_{Source} = 20 mA) (I_{Source} = 200 mA)	 V_{OL} V_{OH}	 — — 9.5 9.0	 0.8 1.5 10.3 9.8	 1.2 2.0 — —	V
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	—	0.8	1.2	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	—	20	50	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	—	20	50	ns
FAULT COMPARATOR					
Input Threshold	V_{th}	0.95	1.0	1.05	V
Input Bias Current ($V_{Pin\ 10}$ = 0 V)	I_{IB}	—	–2.0	–10	µA
Propagation Delay to Drive Outputs (100 mV Overdrive)	$t_{PLH(IN/OUT)}$	—	60	100	ns
SOFT-START					
Capacitor Charge Current ($V_{Pin\ 11}$ = 2.5 V)	I_{chg}	4.5	9.0	14	µA
Capacitor Discharge Current ($V_{Pin\ 11}$ = 2.5 V)	I_{Idchg}	1.0	8.0	—	mA
UNDERVOLTAGE LOCKOUT					
Start-Up Threshold, V_{CC} Increasing Enable/UVLO Adjust Pin Open Enable/UVLO Adjust Pin Connected to V_{CC}	$V_{th(UVLO)}$	 14.8 8.0	 16 9.0	 17.2 10	V
Minimum Operating Voltage After Turn-On Enable/UVLO Adjust Pin Open Enable/UVLO Adjust Pin Connected to V_{CC}	$V_{CC(min)}$	 8.0 7.6	 9.0 8.6	 10 9.6	V
Enable/UVLO Adjust Shutdown Threshold Voltage	$V_{th(Enable)}$	6.0	7.0	—	V
Enable/UVLO Adjust Input Current (Pin 9 = 0V)	$I_{in(Enable)}$	—	–0.2	–1.0	mA
TOTAL DEVICE					
Power Supply Current (Enable/UVLO Adjust Pin Open) Start-Up (V_{CC} = 13.5 V) Operating (f_{OSC} = 100 kHz, Note 2)	I_{CC}	 — —	 0.45 21	 0.6 30	mA

NOTES: 2. Adjust V_{CC} above the Start-Up threshold before setting to 12 V.

Figure 1. MC34066 Functional Block Diagram



INTRODUCTION

As power supply designers have strived to increase power conversion efficiency and reduce passive component size, high frequency resonant mode power converters have emerged as attractive alternatives to conventional square-wave control. When compared to square-wave converters, resonant mode control offers several benefits including lower switching losses, higher efficiency, lower EMI emission, and smaller size. This integrated circuit has been developed to support new trends in power supply design. The MC34066 Resonant Mode Controller is a high performance bipolar IC dedicated to variable frequency power control at frequencies exceeding 1.0 MHz. This integrated circuit provides the features, performance and flexibility for a wide variety of resonant mode power supply applications.

The primary purpose of the control chip is to supply precise pulses to the gates of external power MOSFETs at a repetition rate regulated by a feedback control loop. The MC34066 can be operated in any of three modes as follows: 1) fixed on-time, variable frequency; 2) fixed off-time, variable frequency; and 3) combinations of 1 and 2 that change from fixed on-time to fixed off-time as the frequency increases. Additional features of the IC ensure that system start-up and fault conditions are administered in a safe, controlled manner.

A simplified block diagram of the IC is shown on the first page of this data sheet, which identifies the main functional blocks and the block-to-block interconnects. Figure 1 is a detailed functional diagram which accurately represents the internal circuitry. The various functions can be divided into two sections. The first section includes the primary control path which produces precise output pulses at the desired frequency Oscillator, a One-Shot, a pulse Steering Flip-Flop, a pair of power MOSFET Drivers, and a wide bandwidth Error Amplifier. The second section provides several peripheral support functions including a voltage reference, undervoltage lockout, Soft-Start circuit, and a fault detector.

PRIMARY CONTROL PATH

The output pulse width and repetition rate are regulated through the interaction of the variable frequency Oscillator, One-Shot timer and Error Amplifier. The Oscillator triggers the One-Shot which generates a pulse that is alternately steered to a pair of totem-pole output drivers by a toggle Flip-Flop. The Error Amplifier monitors the output of the regulator and modulates the frequency of the Oscillator. High-speed Schottky logic is used throughout the primary control channel to minimize delays and enhance high frequency characteristics.

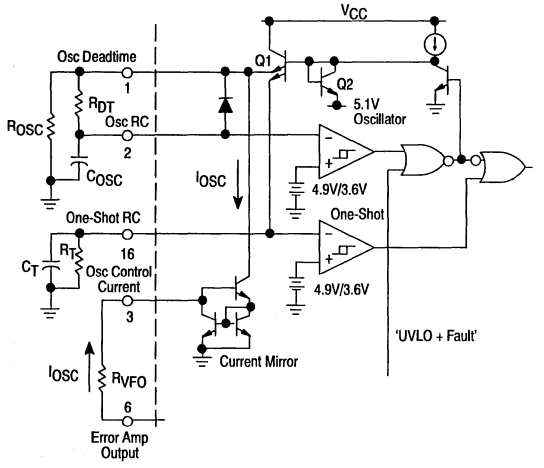
3

Oscillator

The characteristics of the variable frequency Oscillator are crucial for precise controller performance at high operating frequencies. In addition to triggering the One-Shot timer and initiating the output pulse, the Oscillator also determines the initial voltage for the One-Shot capacitor and defines the minimum deadtime between output pulses. The Oscillator is designed to operate at frequencies exceeding 1.0 MHz. The Error Amplifier can control the oscillator frequency over a 1000:1 frequency range, and both the minimum and maximum frequencies are easily and accurately programmed by the proper selection of external components. The Oscillator also includes an adjustable deadtime feature for applications requiring additional time between output pulses.

The functional diagram of the Oscillator and One-Shot timer is shown in Figure 2. The oscillator capacitor C_{OSC} is initially charged by transistor Q1 through the optional deadtime resistor R_{DT}. When C_{OSC} exceeds the 4.9 V upper threshold of the oscillator comparator, the base of Q1 is pulled low allowing C_{OSC} to discharge through the external resistors and the internal Current Mirror. When the voltage on C_{OSC} falls below the comparator's 3.6 V lower threshold, Q1 turns on and again charges C_{OSC}.

Figure 2. Oscillator and One-Shot Timer



If R_{DT} is zero ohms, C_{OSC} charges from 3.6 V to 5.1 V in less than 50 ns. The high slew rate of C_{OSC} and the propagation delay of the comparator make it difficult to control the peak voltage. This accuracy issue is overcome by clamping the base of Q1 through diode Q2 to a voltage reference. The peak voltage of the oscillator waveform is thereby precisely set at 5.1 V.

The frequency of the Oscillator is modulated by varying the current I_{OSC} flowing through R_{VFO} into the Osc Control Current pin. The control current drives a unity gain Current Mirror which pulls an identical current from the C_{OSC} capacitor. As I_{OSC} increases, C_{OSC} discharges faster thus decreasing the Oscillator period and increasing the frequency. The maximum frequency occurs when the Error Amplifier output is at the upper clamp level, nominally 2.5 V above the voltage at the Osc Control Current pin. The minimum discharge time for C_{OSC}, which corresponds to the maximum oscillator frequency, is given by Equation 1.

$$t_{dchg(min)} = (R_{DT} + R_{OSC})C_{OSC}\ln\left[\frac{\frac{2.5R_{OSC}}{R_{VFO}} + 5.1}{\frac{2.5R_{OSC}}{R_{VFO}} + 3.6}\right] \quad (1)$$

The minimum oscillator frequency will result when the I_{OSC} current is zero, and C_{OSC} is discharged through the external resistors R_{OSC} and R_{DT}. This occurs when the Error Amplifier output voltage is less than the two diode drops required to bias the input of the Current Mirror. The maximum oscillator discharge time is given by Equation 2.

$$t_{dchg(max)} = (R_{DT} + R_{OSC})\, C_{OSC}\ln\left(\frac{5.1}{3.6}\right) \quad (2)$$

The outputs of the control IC are off whenever the oscillator capacitor C_{OSC} is being charged by transistor Q1. The minimum time between output pulses (deadtime) can be programmed by controlling the charge time of C_{OSC}. Resistor R_{DT} reduces the current delivered by Q1 to C_{OSC}, thus increasing the charge time and output deadtime. Varying R_{DT} from 0 Ω to 1000 Ω will increase the output deadtime from 80 ns to 680 ns with C_{OSC} equal to 300 pF. The general expression for the oscillator charge time is give by Equation 3.

$$t_{chg(max)} = R_{DT}\, C_{OSC}\ln\left(\frac{5.1-3.6}{5.1-4.9}\right) + 80\text{ ns} \quad (3)$$

The minimum and maximum oscillator frequencies are programmed by the proper selection of resistor R_{OSC} and R_{VFO}. After selecting R_{DT} for the desired deadtime, the minimum frequency is programmed by R_{OSC} using Equations 2 and 3 in Equation 4:

$$\frac{1}{f_{OSC(min)}} = t_{dchg(max)} + t_{chg} \quad (4)$$

The maximum oscillator frequency is set by resistor R_{VFO} in a similar fashion using Equations 1 and 3 in Equation 5:

$$\frac{1}{f_{OSC(max)}} = t_{dchg(min)} + t_{chg} \quad (5)$$

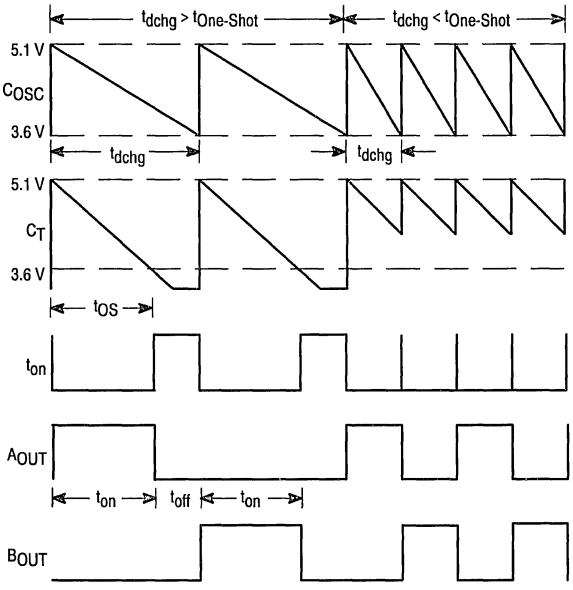
The value chosen for resistor R_{DT} will affect the peak voltage of the oscillator waveform. As R_{DT} is increased from zero, the time required to charge C_{OSC} becomes large with respect to the propagation delay through the oscillator comparator. Consequently, the overshoot of the upper threshold is reduced and the peak voltage on the oscillator waveform drops from 5.1 V to 4.9 V. The best frequency accuracy is achieved when R_{DT} is zero ohms.

One-Shot Timer

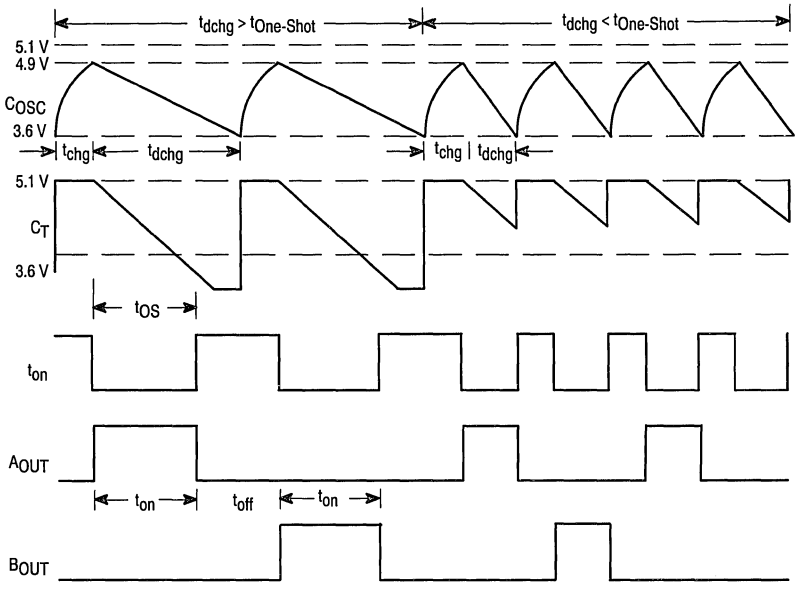
The One-Shot capacitor C_T is charged concurrently with the oscillator capacitor by transistor Q1, as shown in Figure 2. The One-Shot period begins when the oscillator comparator turns off Q1, allowing C_T to discharge. The period ends when resistor R_T discharges C_T to the threshold of the One-Shot comparator. Discharging C_T from an initial voltage of 5.1 V to a threshold voltage of 3.6 V results in the One-Shot period given by Equation 6.

Figure 3. Timing Waveforms

$R_{DT} = 0$



$R_{DT} = 1.0\ k$



$$t_{OS} = R_T C_T \ln \left(\frac{5.1}{3.6}\right) = 0.348\, R_T C_T \qquad (6)$$

Errors in the threshold voltage and propagation delays through the output drivers will affect the One-Shot period. To guarantee accuracy, the output pulse of the control ship is trimmed to within 5% of 1.5 µs with nominal values of R_T and C_T.

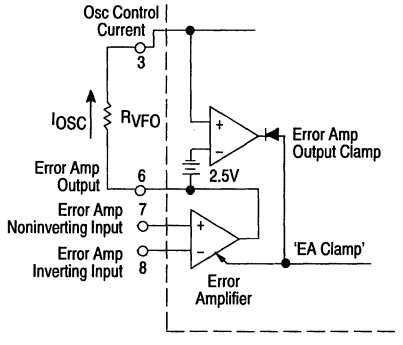
The outputs of the Oscillator and One-Shot comparators are OR'd together to produce the pulse 't_{on},' which drives the Flip-Flop and output drivers. The output pulse 't_{on}' is initiated by the Oscillator, but either the oscillator comparator or the One-Shot comparator can terminate the pulse. When the oscillator discharge time exceeds the one-shot period, the complete one-shot period is delivered to the output section. If the oscillator discharge time is less than the one-shot period, then the oscillator comparator terminates the pulse prematurely and retriggers the One-Shot. The waveforms on the left side of Figure 3 correspond to nonretriggered operation with constant on-time and variable off-times. The right side of Figure 3 represents retriggered operation with variable on-time and constant off-time.

Error Amplifier

A fully accessible high performance Error Amplifier is provided for feedback control of the power supply system. The Error Amplifier is internally compensated and features DC open-loop gain greater than 70 dB, input offset voltage less than 10 mV and guaranteed minimum gain-bandwidth product of 2.5 MHz. The input common mode range extends from 1.5 V to 5.1 V, which includes the reference voltage. For common mode voltages below 1.5 V, the Error Amplifier output is forced low providing minimum oscillator frequency.

The Oscillator Control Current pin is biased by the Error Amplifier output voltage through R_{VFO} as illustrated in Figure 4. The output swing of the Error Amplifier is restricted by a clamp circuit to limit the maximum oscillator frequency. The clamp circuit limits the voltage across R_{VFO} to 2.5 V, thus limiting I_{OSC} to 2.5 V/R_{VFO}. Oscillator accuracy is improved by trimming the clamp voltage to obtain the $f_{OSC(high)}$ specification of 1.0 MHz with nominal value external components.

Figure 4. Error Amplifier and Clamp

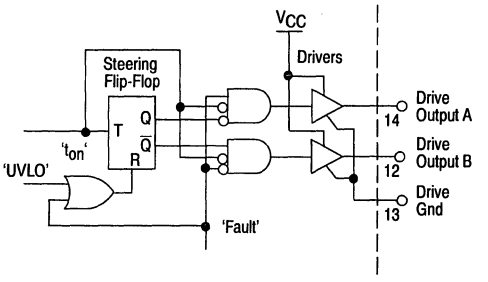


Output Section

The pulse, 't_{on},' generated by the Oscillator and One-Shot timer is gated to dual totem pole output drives by the Steering Flip-Flop shown in Figure 5. Positive transitions of 't_{on}' toggle the Flip-Flop, which causes the pulses to alternate between Output A and Output B. The flip-flop is reset by the undervoltage lockout circuit during start-up to guarantee that the first pulse appears at Output A.

The totem-pole output drives are ideally suited for driving power MOSFETs and are capable of sourcing and sinking 1.5 A. Rise and fall times are typically 20 ns when driving a 1.0 nF load. High source/sink capability in a totem-pole driver normally increases the risk of high cross conduction current during output transitions. The MC34066 utilizes a unique design that virtually eliminates cross conduction, thus controlling the chip power dissipation at high frequencies. A separate ground terminal is provided for the output drivers to isolate the sensitive analog circuitry from large transient currents.

Figure 5. Steering Flip-Flop and Output Drivers



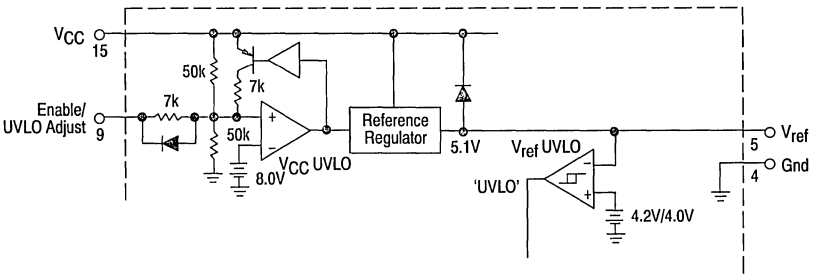
PERIPHERAL SUPPORT FUNCTIONS

The MC34066 Resonant Controller provides a number of support and protection functions including a precision voltage reference, undervoltage lockout comparators, soft-start circuitry, and a fault detector. These peripheral circuits ensure that the power supply can be turned on and off in a safe, controlled manner and that the system will be quickly disabled when a fault condition occurs.

Undervoltage Lockout and Voltage Reference

Separate undervoltage lockout comparators sense the input V_{CC} voltage and the regulated reference voltage as illustrated in Figure 6. When V_{CC} increases to the upper threshold voltage, the V_{CC} UVLO comparator enables the Reference Regulator. After the V_{ref} output of the Reference Regulator rises to 4.2 V, the V_{ref} UVLO comparator switches the 'UVLO' signal to a logic zero state enabling the primary control path. Reducing V_{CC} to the lower threshold voltage causes the V_{CC} UVLO comparator to disable the Reference Regulator. The V_{ref} UVLO comparator then switches the 'UVLO' output to a logic one state disabling the controller.

Figure 6. Undervoltage Lockout and Reference



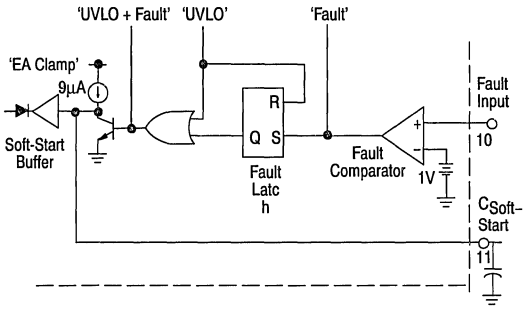
The Enable/UVLO Adjust terminal allows the power supply designer to select the V_{CC} UVLO threshold voltages. When this pin is open, the comparator switches the controller on at 16 V and off at 9.0 V. If this pin is connected to the V_{CC} terminal, the upper and lower thresholds are reduced to 9.0 V and 8.6 V, respectively. Forcing the Enable/UVLO Adjust pin low will pull the V_{CC} UVLO comparator input low (through an internal diode) turning off the controller.

The Reference Regulator provides a precise 5.1 V reference to internal circuitry and can deliver up to 10 mA to external loads. The reference is trimmed to better than 2% initial accuracy and includes active short circuit protection.

Fault Detector

The high-speed Fault Comparator and Latch illustrated in Figure 7 can protect a power supply from destruction under fault conditions. The Fault Input pin connects to the input of the Fault Comparator. If this input exceeds the 1.0 V threshold of the comparator, the Fault Latch is set and two logic signals simultaneously disable the primary control path. The signal labeled 'Fault' at the output of the Fault Comparator is connected directly to the output drivers. This direct path reduces the propagation delay from the Fault Input to the A and B outputs to typically 70 ns. The Fault Latch output is OR'd with 'UVLO' output from the V_{ref} UVLO comparator to produce the logic output labeled 'UVLO + Fault.' This signal disables the Oscillator and One-Shot by forcing both the C_{OSC} and C_T capacitors to be continually charged.

Figure 7. Fault Detector and Soft-Start



The Fault Latch is reset during start-up by a logic one at the 'UVLO' output of the V_{ref} UVLO comparator. The latch can also be reset after start-up by pulling the Enable/UVLO Adjust pin momentarily low to disable the Reference Regulator.

Soft-Start Circuit

The Soft-Start circuit shown in Figure 7 forces the variable frequency Oscillator to start at the minimum frequency and ramp upward until regulated by the feedback control loop. The external capacitor at the $C_{Soft\text{-}Start}$ terminal is initially discharged by the 'UVLO + Fault' signal. The low voltage on the capacitor pass through the Soft-Start Buffer to hold the Error Amplifier output low. After 'UVLO + Fault' switches to a logic zero, the soft-start capacitor is charged by a 9.0 μA current source. The buffer allows the Error Amplifier output to follow the soft-start capacitor until it is regulated by the Error Amplifier inputs (or reaches the 2.5 V clamp). The soft-start function is generally applicable to controllers operating below resonance and can be disabled by simply opening the $C_{Soft\text{-}Start}$ terminal.

APPLICATIONS

The MC34066 can be used for the control of series, parallel or higher order half/full bridge resonant converters. The IC is designed to provide control in discontinuous conduction mode (DCM) or continuous conduction mode (CCM) or a combination of the two. For example, in a parallel resonant converter (PRC) operating in the DCM, the IC is programmed to operate in fixed on-time, variable frequency mode of operation. For a PRC operating in the CCM, the IC can be programmed to operate in the variable frequency mode with a fixed off-time.

When operating with a wide input voltage range, such as a universal input power supply, a PRC can operate in the DCM for high input voltage and in the CCM for low input voltage. In this particular case, on-time is programmed corresponding to DCM. The deadtime of the chip is programmed to provide the desired off-time in the CCM. The frequency range is chosen to cover the complete frequency range from the DCM to the CCM. When programmed as such, the controller will operate in the fixed on-time, variable frequency mode at low frequencies. At the frequency which causes the Oscillator to retrigger the One-Shot, the control law changes to variable frequency with fixed off-time. At higher frequencies the supply will operate in the CCM with this control law.

Although the IC is designed and optimized for double ended push-pull type converters, it can also be used for single ended applications, such as forward and flyback resonant converters.

MC34067
MC33067

Advance Information

High Performance Resonant Mode Controller

3

The MC34067 series of high performance zero voltage switch resonant mode controllers are designed for Off-Line and DC-to-DC converter applications that utilize frequency modulated constant off-time or constant dead-time control. These integrated circuits feature a variable frequency oscillator, a precise retriggerable one-shot timer, temperature compensated reference, high gain wide bandwidth error amplifier, steering flip-flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of a high speed fault comparator and latch, programmable soft-start circuitry, input undervoltage lockout with selectable thresholds, and reference undervoltage lockout.

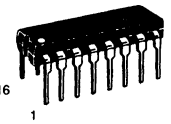
These devices are available in dual-in-line and surface mount packages.

- Zero Voltage Switch Resonant Mode Operation
- Variable Frequency Oscillator with a Control Range Exceeding 1000:1
- Precision One-Shot Timer for Controlled Off-Time
- Internally Trimmed Bandgap Reference
- 4.0 MHz Error Amplifier
- Dual High Current Totem Pole Outputs
- Selectable Undervoltage Lockout Thresholds with Hysteresis
- Enable Input
- Programmable Soft-Start Circuitry
- Low Start-Up Current for Off-Line Operation

HIGH PERFORMANCE ZERO VOLTAGE SWITCH RESONANT MODE CONTROLLER

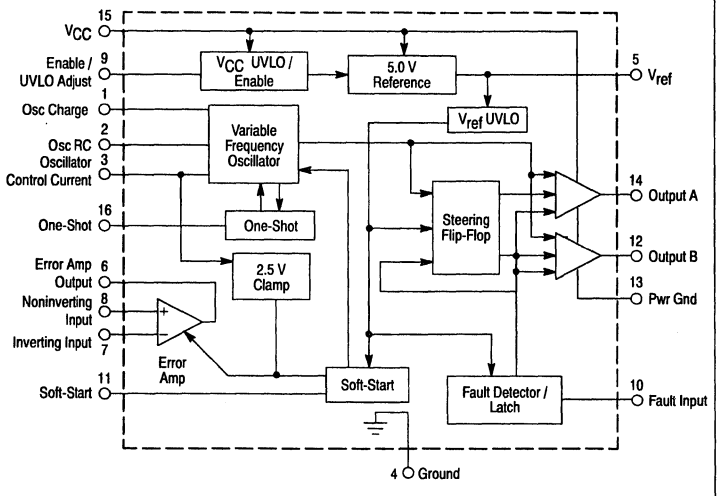
SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 648

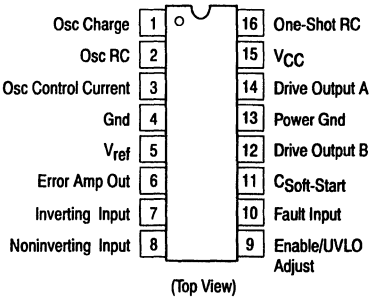


DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO-16L)

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34067DW	0 to + 70°C	SO-16L
MC34067P		Plastic DIP
MC33067DW	– 40° to + 85°C	SO-16L
MC33067P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Drive Output Current, Source or Sink (Note 1) Continuous Pulsed (0.5 μs, 25% Duty Cycle	I_O	 0.3 1.5	A
Error Amplifier, Fault, One-Shot, Oscillator and Soft-Start Inputs	V_{in}	– 1.0 to + 6.0	V
UVLO Adjust Input	$V_{in(UVLO)}$	– 1.0 to V_{CC}	V
Power Dissipation and Thermal Characteristics DW Suffix, Plastic Package SO-16L Case 751G T_A = 25°C Thermal Resistance, Junction-to-Air P Suffix, Plastic Package Case 648 T_A = 25°C Thermal Resistance, Junction-to-Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+ 150	°C
Operating Ambient Temperature MC34067 MC33067	T_A	 0 to + 70 – 40 to + 85	°C
Storage Temperature	T_{stg}	– 55 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V [Note 2], R_{OSC}= 18.2 k, R_{VFO} = 2940, C_{OSC} = 300 pF, R_T = 2370 k, C_T = 300 pF, C_L = 1.0 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 0 mA, T_J = 25°C)	V_{ref}	5.0	5.1	5.2	V
Line Regulation (V_{CC} = 10 TO 18 V)	Reg_{line}	—	1.0	20	mV
Load Regulation (I_O = 0 mA to 10 mA)	Reg_{load}	—	1.0	20	mV
Total Output Variation Over Line, Load, and Temperature	V_{ref}	4.9	—	5.3	V
Output Short Circuit Current	I_O	25	100	190	mA
Reference Undervoltage Lockout Threshold	V_{th}	3.8	4.3	4.8	V
ERROR AMPLIFIER					
Input Offset Voltage (V_{CM} = 1.5 V)	V_{IO}	—	1.0	10	mV
Input Bias Current (V_{CM} = 1.5 V)	I_{IB}	—	0.2	1.0	μA
Input Offset Current (V_{CM} = 1.5 V)	I_{IO}	—	0	0.5	μA
Open-Loop Voltage Gain (V_{CM} = 1.5 V, V_O = 2.0 V)	A_{VOL}	70	100	—	dB
Gain Bandwidth Product (f = 100 kHz)	GBW	3.0	5.0	—	MHz
Input Common Mode Rejection Ratio (V_{CM} = 1.5 to 5.0 V)	CMR	70	95	—	dB
Power Supply Rejection Ratio (V_{CC} = 10 to 18 V, f = 120 Hz)	PSR	80	100	—	dB
Output Voltage Swing High State Low State	 V_{OH} V_{OL}	 2.8 —	 3.2 0.6	 — 0.8	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V [Note 2], R_{OSC}= 18.2 k, R_{VFO} = 2940, C_{OSC} = 300 pF, R_T = 2370 k, C_T = 300 pF, C_L = 1.0 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (Error Amp Output High) T_A = 25°C Total Variation (V_{CC} = 10 to 18 V, T_A = T_{Low} to T_{High}	$f_{OSC(low)}$	500 490	525 —	540 550	kHz
Frequency (Error Amp Output Low) T_A = 25°C Total Variation (V_{CC} = 10 to 18 V, T_A = T_{Low} to T_{High}	$f_{OSC(high)}$	1900 1850	2050 —	2150 2200	kHz
Oscillator Control Input Voltage, Pin 3 @ 25°C	V_{in}	—	2.5	—	V
ONE-SHOT					
Drive Output Off-Time T_A = 25°C Total Variation (V_{CC} = 10 to 18 V, T_A = T_{Low} to T_{High}	t_{Blank}	235 225	250 —	270 280	ns
DRIVE OUTPUTS					
Output Voltage Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA) High State (I_{Source} = 20 mA) (I_{Source} = 200 mA)	 V_{OL} V_{OH} 	 — — 9.5 9.0	 0.8 1.5 10.3 9.7	 1.2 2.0 — —	V
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	—	0.8	1.2	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	—	20	50	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	—	15	50	ns
FAULT COMPARATOR					
Input Threshold	V_{th}	0.93	1.0	1.07	V
Input Bias Current ($V_{Pin\ 10}$ = 0 V)	I_{IB}	—	−2.0	−10	µA
Propagation Delay to Drive Outputs (100 mV Overdrive)	$t_{PLH(In/Out)}$	—	60	100	ns
SOFT-START					
Capacitor Charge Current ($V_{Pin\ 11}$ = 2.5 V)	I_{chg}	4.5	9.0	14	µA
Capacitor Discharge Current ($V_{Pin\ 11}$ = 2.5 V)	I_{dischg}	3.0	8.0	—	mA
UNDERVOLTAGE LOCKOUT					
Start-Up Threshold, V_{CC} Increasing Enable/UVLO Adjust Pin Open Enable/UVLO Adjust Pin Connected to V_{CC}	$V_{th(UVLO)}$	14.8 8.0	16 9.0	17.2 10	V
Minimum Operating Voltage After Turn-On Enable/UVLO Adjust Pin Open Enable/UVLO Adjust Pin Connected to V_{CC}	$V_{CC(min)}$	8.0 7.6	9.0 8.6	10 9.6	V
Enable/UVLO Adjust Shutdown Threshold Voltage	$V_{th(Enable)}$	6.0	7.0	—	V
Enable/UVLO Adjust Input Current (Pin 9 = 0 V)	$I_{in(Enable)}$	—	−0.2	−1.0	mA
TOTAL DEVICE					
Power Supply Current (Enable/UVLO Adjust Pin Open) Start-Up (V_{CC} = 13.5 V) Operating (f_{OSC} = 500 kHz, Note 2)	I_{CC}	— —	0.5 27	0.8 35	mA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Start-Up threshold before setting to 12 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for the MC34067 = −40°C for the MC33067 T_{high} = +70°C for MC34067 = +85°C for MC33067

Figure 1. Oscillator Timing Resistor versus Discharge Time

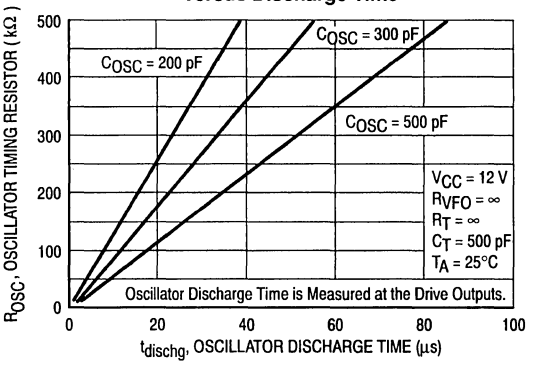


Figure 2. Oscillator Frequency versus Oscillator Control Current

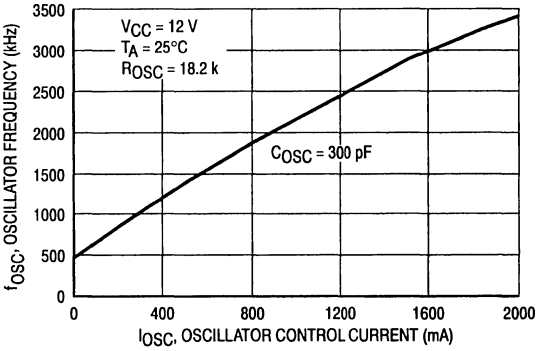


Figure 3. Error Amp Output Saturation Voltage versus Oscillator Control Current

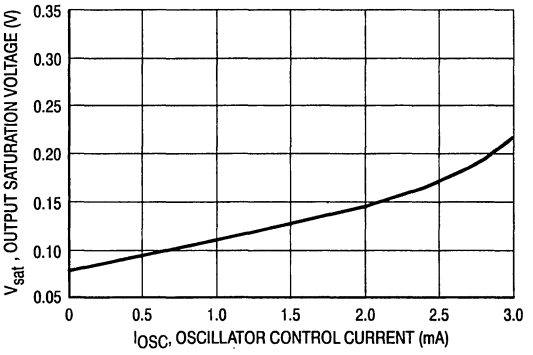


Figure 4. One-Shot Timing Resistor versus Period

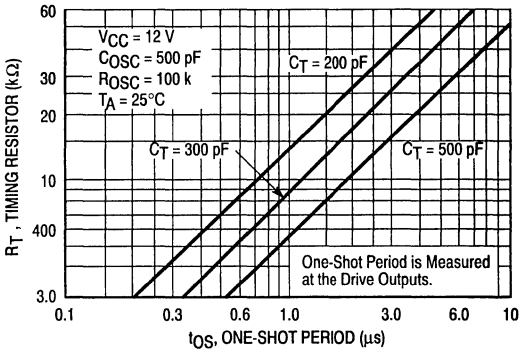


Figure 5. Open-Loop Voltage Gain and Phase versus Frequency

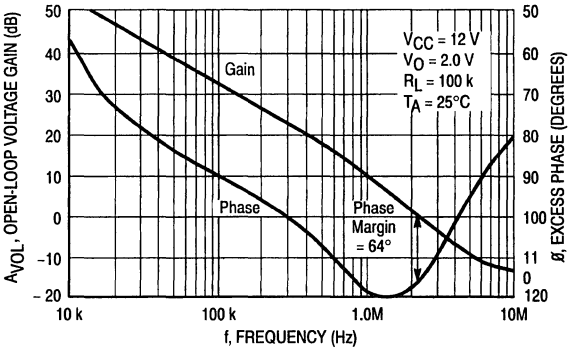
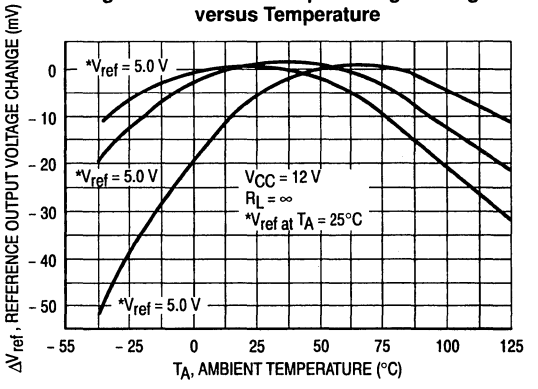


Figure 6. Reference Output Voltage Change versus Temperature



3

Figure 7. Reference Voltage Change versus Source Current

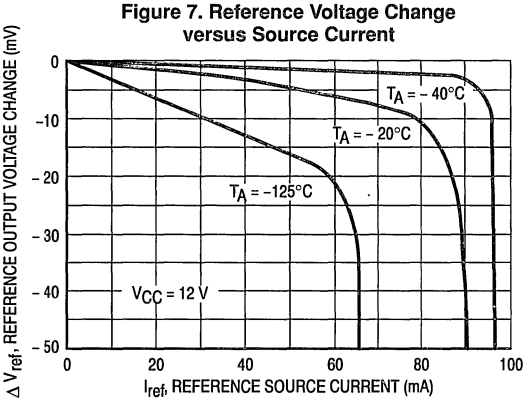


Figure 8. Drive Output Saturation Voltage versus Load Current

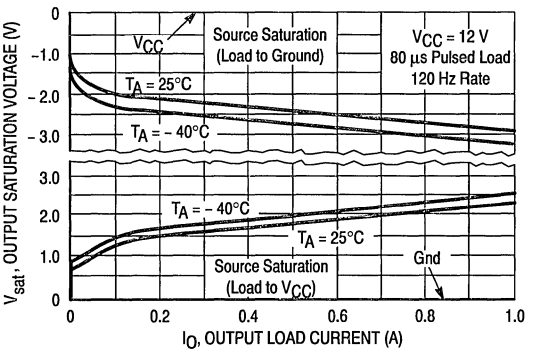


Figure 9. Drive Output Waveform

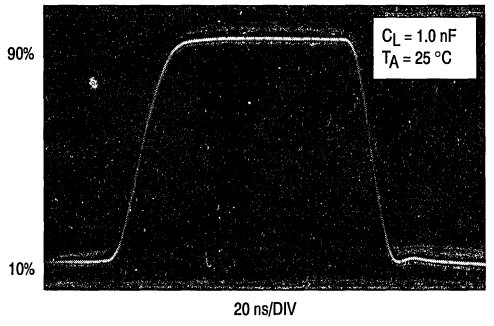


Figure 10. Soft-Start Saturation Voltage versus Capacitor Discharge Current

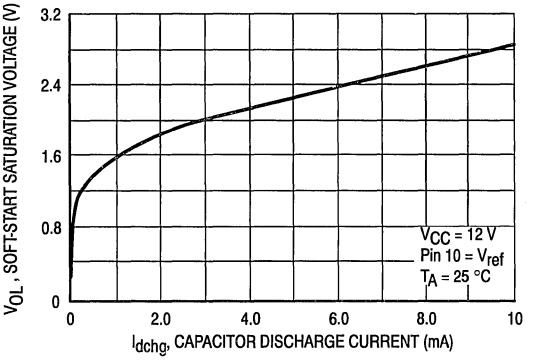


Figure 11. Operating Frequency versus Supply Current

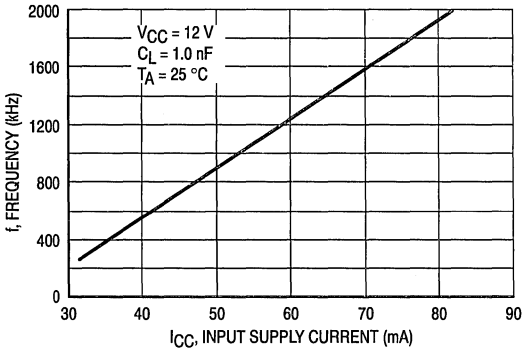


Figure 12. Supply Current versus Supply Voltage

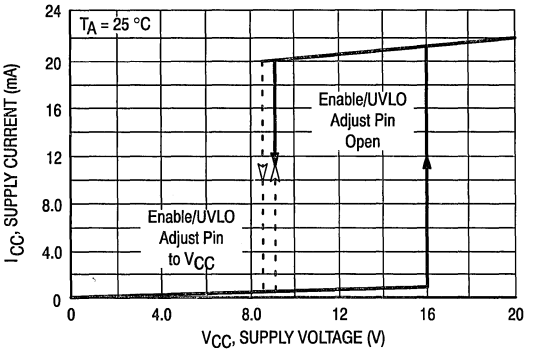
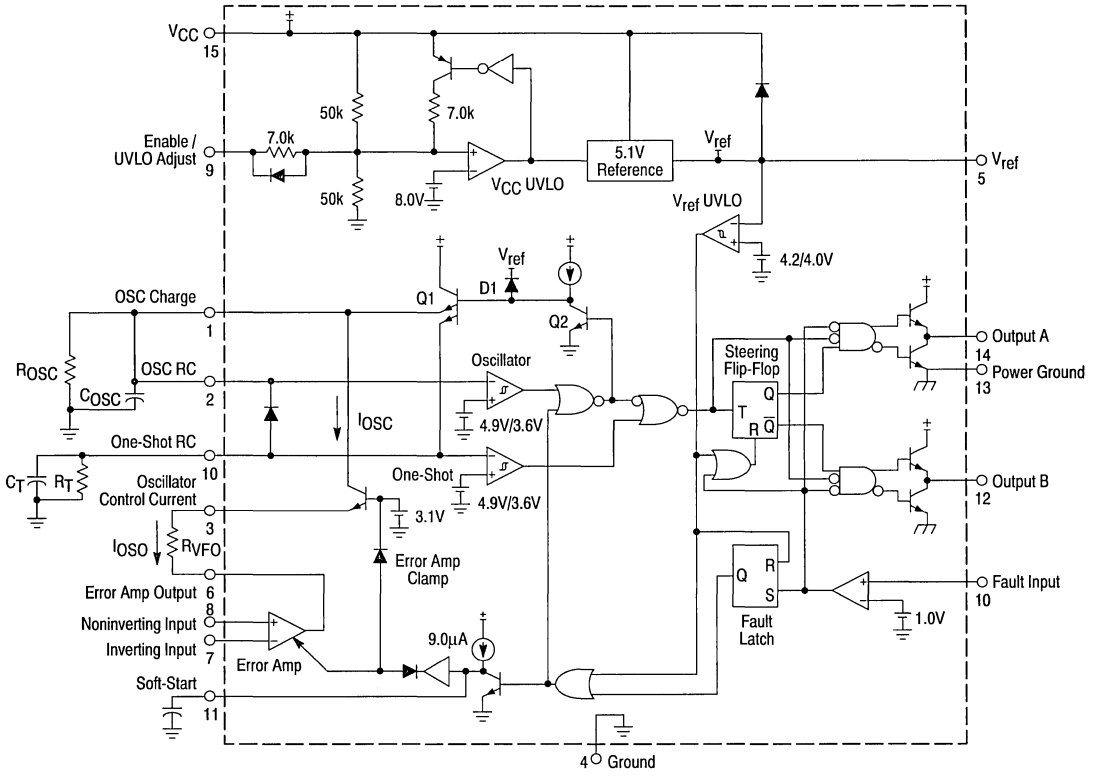
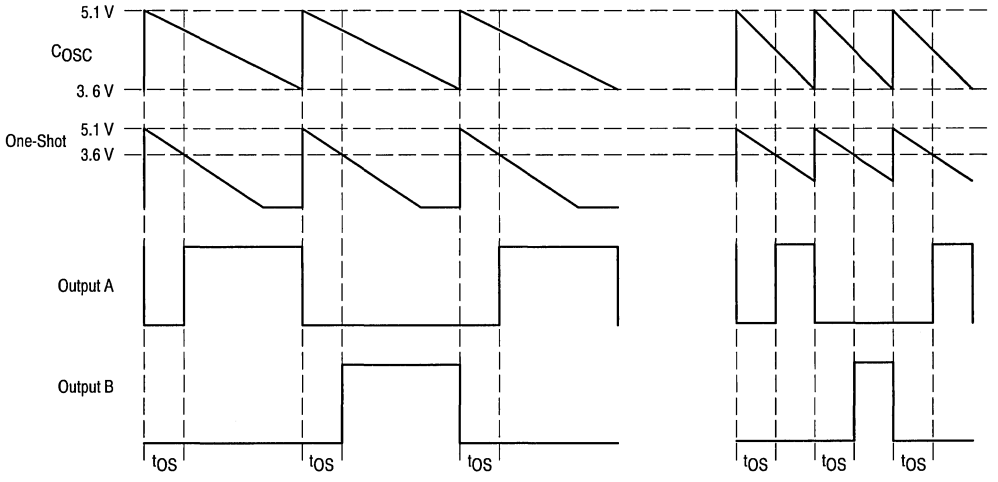


Figure 13. MC34067 Representative Block Diagram



Timing Diagram



Error Amp output high, minimum I_{OSC} current occurring at minimum input voltage, maximum load.

Error Amp output low, maximum I_{OSC} current occurring at maximum input voltage, minimum load.

OPERATING DESCRIPTION

Introduction

As power supply designers have strived to increase power conversion efficiency and reduce passive component size, high frequency resonant mode power converters have emerged as attractive alternatives to conventional pulse-width modulated control. When compared to pulse-width modulated converters, resonant mode control offers several benefits including lower switching losses, higher efficiency, lower EMI emission, and smaller size. A new integrated circuit has been developed to support this trend in power supply design. The MC34067 Resonant Mode Controller is a high performance bipolar IC dedicated to variable frequency power control at frequencies exceeding 1.0 MHz. This integrated circuit provides the features and performance specifically for zero voltage switching resonant mode power supply applications.

The primary purpose of the control chip is to provide a fixed off-time to the gates of external power MOSFETs at a repetition rate regulated by a feedback control loop. Additional features of the IC ensure that system start-up and fault conditions are administered in a safe, controlled manner.

A simplified block diagram of the IC is shown on the front page, which identifies the main functional blocks and the block-to-block interconnects. Figure 13 is a detailed functional diagram which accurately represents the internal circuitry. The various functions can be divided into two sections. The first section includes the primary control path which produces precise output pulses at the desired frequency. Included in this section are a variable frequency Oscillator, a One-Shot, a pulse Steering Flip-Flop, a pair of power MOSFET Drivers, and a wide bandwidth Error Amplifier. The second section provides several peripheral support functions including a voltage reference, undervoltage lockout, Soft-Start circuit, and a fault detector.

Primary Control Path

The output pulse width and repetition rate are regulated through the interaction of the variable frequency Oscillator, One-Shot timer and Error Amplifier. The Oscillator triggers the One-Shot which generates a pulse that is alternately steered to a pair of totem pole output drivers by a toggle Flip-Flop. The Error Amplifier monitors the output of the regulator and modulates the frequency of the Oscillator. High speed Schottky logic is used throughout the primary control channel to minimize delays and enhance high frequency characteristics.

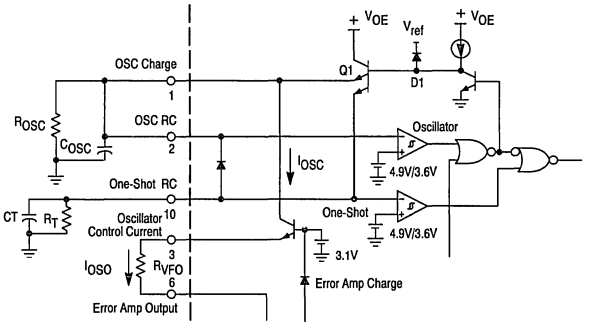
Oscillator

The characteristics of the variable frequency Oscillator are crucial for precise controller performance at high operating frequencies. In addition to triggering the One-Shot timer and initiating the output deadtime, the oscillator also determines the initial voltage for the one-shot capacitor. The Oscillator is designed to operate at frequencies exceeding 1.0 MHz. The Error Amplifier can control the oscillator frequency over a 1000:1 frequency range, and both the minimum and maximum frequencies are easily and accurately programmed by the proper selection of external components.

The functional diagram of the Oscillator and One-Shot timer is shown in Figure 14. The oscillator capacitor (C_{OSC}) is initially charged by transistor Q1. When C_{OSC} exceeds the 4.9 V upper threshold of the oscillator comparator, the base of Q1 is pulled low allowing C_{OSC} to discharge through the external resistor, (R_{OSC}), and the oscillator control current, (I_{OSC}). When the voltage on C_{OSC} falls below the comparator's 3.6 V lower threshold, Q1 turns on and again charges C_{OSC}.

C_{OSC} charges from 3.6 V to 5.1 V in less than 50 ns. The high slew rate of C_{OSC} and the propagation delay of the comparator make it difficult to control the peak voltage. This accuracy issue is overcome by clamping the base of Q1 through a diode to a voltage reference. The peak voltage of the oscillator waveform is thereby precisely set at 5.1 V.

Figure 14. Oscillator and One-Shot Timer



The frequency of the Oscillator is modulated by varying the current flowing out of the Oscillator Control Current (I_{OSC}) pin. The I_{OSC} pin is the output of a voltage regulator. The input of the voltage regulator is tied to the variable frequency oscillator. The discharge current of the Oscillator increases by increasing the current out of the I_{OSC} pin. Resistor R_{VFO} is used in conjunction with the Error Amp output to change the I_{OSC} current. Maximum frequency occurs when the Error Amplifier output is at its low state with a saturation voltage of 0.1 V at 1.0 mA.

The minimum oscillator frequency will result when the I_{OSC} current is zero, and C_{OSC} is discharged through the external resistor (R_{OSC}). This occurs when the Error Amplifier output is at its high state of 2.5 V. The minimum and maximum oscillator frequencies are programmed by the proper selection of resistor R_{OSC} and R_{VFO}. The minimum frequency is programmed by R_{OSC} using Equation 1:

$$R_{OSC} = \frac{\frac{1}{f_{(min)}} - t_{PD}}{C_{OSC}\,\ell n\left(\frac{5.1}{3.6}\right)} = \frac{t_{(max)} - 70\text{ ns}}{0.348\,C_{OSC}} \quad (1)$$

where t_{PD} is the internal propagation delay.

The maximum oscillator frequency is set by the current through resistor R_{VFO}. The current required to discharge C_{OSC} at the maximum oscillator frequency can be calculated by Equation 2:

$$I_{(max)} = C_{OSC}\frac{5.1 - 3.6}{\frac{1}{f_{(max)}}} = 1.5C_{OSC}f_{(max)} \quad (2)$$

The discharge current through R_{OSC} must also be known and can be calculated by Equation 3:

$$I_{R_{OSC}} = \frac{5.1 - 3.6}{R_{OSC}}\,\varepsilon^{\left(-\frac{\frac{1}{f_{(min)}}}{R_{OSC}C_{OSC}}\right)} = \frac{1.5}{R_{OSC}}\,\varepsilon^{\left(-\frac{1}{f_{(min)}R_{OSC}C_{OSC}}\right)} \quad (3)$$

Resistor R_{VFO} can now be calculated by Equation 4:

$$R_{VFO} = \frac{2.5 - V_{EAsat}}{I_{(max)} - I_{R_{OSC}}} \quad (4)$$

One-Shot Timer

The One-Shot is designed to disable both outputs simultaneously providing a dead time before either output is enabled. The One-Shot capacitor (C_T) is charged concurrently with the oscillator capacitor by transistor Q1, as shown in Figure 14. The one-shot period begins when the oscillator comparator turns off Q1, allowing C_T to discharge. The period ends when resistor R_T discharges C_T to the threshold of the One-Shot comparator. The lower threshold of the One-Shot is 3.6 V. By choosing C_T, R_T can by solved by Equation 5:

$$R_T = \frac{t_{OS}}{C_T\,\ell n\left(\frac{5.1}{3.6}\right)} = \frac{t_{OS}}{0.348\,C_T} \quad (5)$$

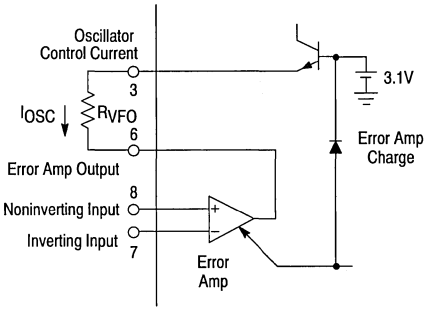
Errors in the threshold voltage and propagation delays through the output drivers will affect the One-Shot period. To guarantee accuracy, the output pulse of the control chip is trimmed to within 5% of 250 ns with nominal values of R_T and C_T.

The outputs of the Oscillator and One-Shot comparators are OR'd together to produce the pulse t_{OS}, which drives the Flip-Flop and output drivers. The output pulse (t_{OS}) is initiated by the Oscillator and terminated by the One-Shot comparator. With zero-voltage resonant mode converters, the oscillator discharge time should never be set less than the one-shot period.

Error Amplifier

A fully accessible high performance Error Amplifier is provided for feedback control of the power supply system. The Error Amplifier is internally compensated and features DC open loop gain greater than 70 dB, input offset voltage of less than 10 mV and a guaranteed minimum gain-bandwidth product of 2.5 MHz. The input common mode range extends from 1.5 V to 5.1 V, which includes the reference voltage.

Figure 15. Error Amplifier and Clamp

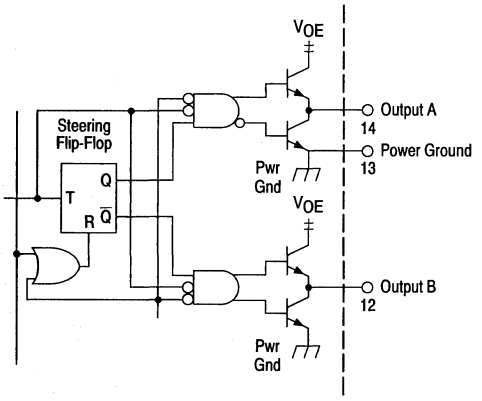


When the Error Amplifier output is coupled to the I_{OSC} pin by R_{VFO}, as illustrated in Figure 15, it provides the Oscillator Control Current, I_{OSC}. The output swing of the Error Amplifier is restricted by a clamp circuit to improve its transient recovery time.

Output Section

The pulse(t_{OS}), generated by the Oscillator and One-Shot timer is gated to dual totem-pole output drives by the Steering Flip-Flop shown in Figure 16. Positive transitions of t_{OS} toggle the Flip-Flop, which causes the pulses to alternate between Output A and Output B. The flip-flop is reset by the undervoltage lockout circuit during start-up to guarantee that the first pulse appears at Output A.

Figure 16. Steering Flip-Flop and Output Drivers



The totem-pole output drivers are ideally suited for driving power MOSFETs and are capable of sourcing and sinking 1.5 A. Rise and fall times are typically 20 ns when driving a 1.0 nF load. High source/sink capability in a totem-pole driver normally increases the risk of high cross conduction current during output transitions. The MC34067 utilizes a unique design that virtually eliminates cross conduction, thus controlling the chip power dissipation at high frequencies. A separate power ground pin is provided to isolate the sensitive analog circuitry from large transient currents.

PERIPHERAL SUPPORT FUNCTIONS

The MC34067 Resonant Controller provides a number of support and protection functions including a precision voltage reference, undervoltage lockout comparators, soft-start circuitry, and a fault detector. These peripheral circuits ensure that the power supply can be turned on and off in a controlled manner and that the system will be quickly disabled when a fault condition occurs.

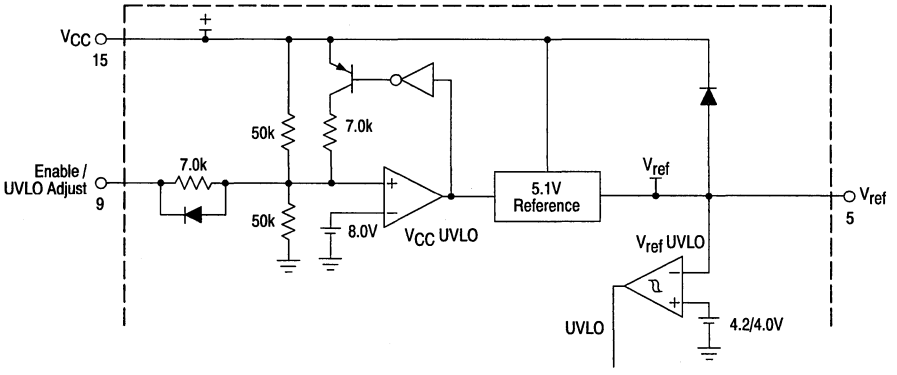
Undervoltage Lockout and Voltage Reference

Separate undervoltage lockout comparators sense the input V_{CC} voltage and the regulated reference voltage as illustrated in Figure 17. When V_{CC} increases to the upper threshold voltage, the V_{CC} UVLO comparator enables the Reference Regulator. After the V_{ref} output of the Reference Regulator rises to 4.2 V, the V_{ref} UVLO comparator switches the UVLO signal to a logic zero state enabling the primary control path. Reducing V_{CC} to the lower threshold voltage causes the V_{CC} UVLO comparator to disable the Reference Regulator. The V_{ref} UVLO comparator then switches the UVLO output to a logic one state disabling the controller.

The Enable/UVLO Adjust pin allows the power supply designer to select the V_{CC} UVLO threshold voltages. When this pin is open, the comparator switches the controller on at 16 V and off at 9.0 V. If this pin is connected to the V_{CC} terminal, the upper and lower thresholds are reduced to 9.0 V and 8.6 V, respectively. Forcing the Enable/UVLO Adjust pin low will pull the V_{CC} UVLO comparator input low (through an internal diode) turning off the controller.

The Reference Regulator provides a precise 5.1 V reference to internal circuitry and can deliver up to 10 mA to external loads. The reference is trimmed to better than 2% initial accuracy and includes active short circuit protection.

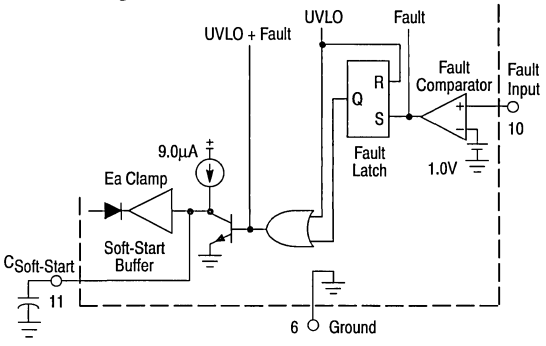
Figure 17. Undervoltage Lockout and Reference



Fault Detector

The high speed Fault Comparator and Latch illustrated in Figure 18 can protect a power supply from destruction under fault conditions. The Fault Input pin connects to the input of the Fault Comparator. If this input exceeds the 1.0 V threshold of the comparator, the Fault Latch is set and two logic signals simultaneously disable the primary control path.

Figure 18. Fault Detector and Soft-Start



The signal labeled "Fault" at the output of the Fault Comparator is connected directly to the output drivers. This direct path reduces the propagation delay from the Fault Input to the A and B outputs to typically 70 ns. The Fault Latch output is OR'd with the UVLO output from the V_{ref} UVLO comparator to produce the logic output labeled "UVLO+Fault". This signal disables the Oscillator and One-Shot by forcing both the C_{OSC} and C_T capacitors to be continually charged.

The Fault Latch is reset during start-up by a logic "1" at the UVLO output of the V_{ref} UVLO comparator. The latch can also be reset after start-up by pulling the Enable/ UVLO Adjust pin momentarily low to disable the Reference Regulator.

Soft-Start Circuit

The Soft-Start circuit shown in Figure 18 forces the variable frequency Oscillator to start at the maximum frequency and ramp downward until regulated by the feedback control loop. The external capacitor at the $C_{Soft\text{-}Start}$ terminal is initially discharged by the UVLO+Fault signal. The low voltage on the capacitor passes through the Soft-Start Buffer to hold the Error Amplifier output low. After UVLO+Fault switches to a logic zero, the soft-start capacitor is charged by a 9.0 μA current source. The buffer allows the Error Amplifier output to follow the soft-start capacitor until it is regulated by the Error Amplifier inputs. The soft-start function is generally applicable to controllers operating below resonance and can be disabled by simply opening the $C_{Soft\text{-}Start}$ terminal.

APPLICATIONS INFORMATION

The MC34067 is specifically designed for zero voltage switching (ZVS) quasi-resonant converter (QRC) applications. The IC is optimized for double-ended push-pull or bridge type converters operating in continuous conduction mode. Operation of this type of ZVS with resonant properties is similar to standard push-pull or bridge circuits in that the energy is transferred during the transistor on-time. The difference is that a series resonant tank is usually introduced to shape the voltage across the power transistor prior to turn-on. The resonant tank in this topology is not used to deliver energy to the output as is the case with zero current switch topologies. When the power transistor is enabled the voltage across it should already be zero, yielding minimal switching loss. Figure 19 shows a timing diagram for a half-bridge ZVS QRC. An application circuit is shown in Figure 20. The circuit built is a DC to DC half-bridge converter delivering 75 W to the output from a 48 V source.

When building a zero voltage switch (ZVS) circuit, the objective is to waveshape the power transistor's voltage waveform so that the voltage across the transistor is zero when the device is turned on. The purpose of the control IC is to allow a resonant tank to waveshape the voltage across the power transistor while still maintaining regulation. This is accomplished by maintaining a fixed dead time and by varying the frequency; thus the effective duty cycle is changed.

Primary side resonance can be used with ZVS circuits. In the application circuit, the elements that make the resonant tank are the primary leakage inductance of the transformer (L_L) and the average output capacitance (C_{OSS}) of a power MOSFET (C_R). The desired resonant frequency for the application circuit is calculated by Equation 6:

$$f_r = \frac{1}{2\pi\sqrt{L_L 2C_R}} \qquad (6)$$

In the application circuit, the operating voltage is low and the value of C_{OSS} versus Drain Voltage is known. Because the C_{OSS} of a MOSFET changes with drain voltage, the value of the C_R is approximated as the average C_{OSS} of the MOSFET. For the application circuit the average C_{OSS} can be calculated by Equation 7:

$$C_R = \sqrt{2} * C_{OSS} \text{ measured at } \frac{1}{2} V_{in} \qquad (7)$$

The MOSFET chosen fixes C_R and that L_L is adjusted to achieve the desired resonant frequency.

However, the desired resonant frequency is less critical than the leakage inductance. Figure 19 shows the primary current ramping toward its peak value during the resonant transition. During this time, there is circulating current flowing through the secondary inductance, which effectively makes the primary inductance appear shorted. Therefore, the current through the primary will ramp to its peak value at a rate controlled by the leakage inductance and the applied voltage. Energy is not transferred to the secondary during this stage, because the primary current has not overcome the circulating current in the secondary. The larger the leakage inductance, the longer it takes for the primary current to slew. The practical effect of this is to lower the duty cycle, thus reducing the operating range.

The maximum duty cycle is controlled by the leakage inductance, not by the MC34067. The One-Shot in the MC34067 only assures that the power switch is turned on under a zero voltage condition. Adjust the one-shot period so that the output switch is activated while the primary current is slewing but before the current changes polarity. The resonant stage should then be designed to be as long as the time for the primary current to go to zero amps.

Figure 19. Application Timing Diagram

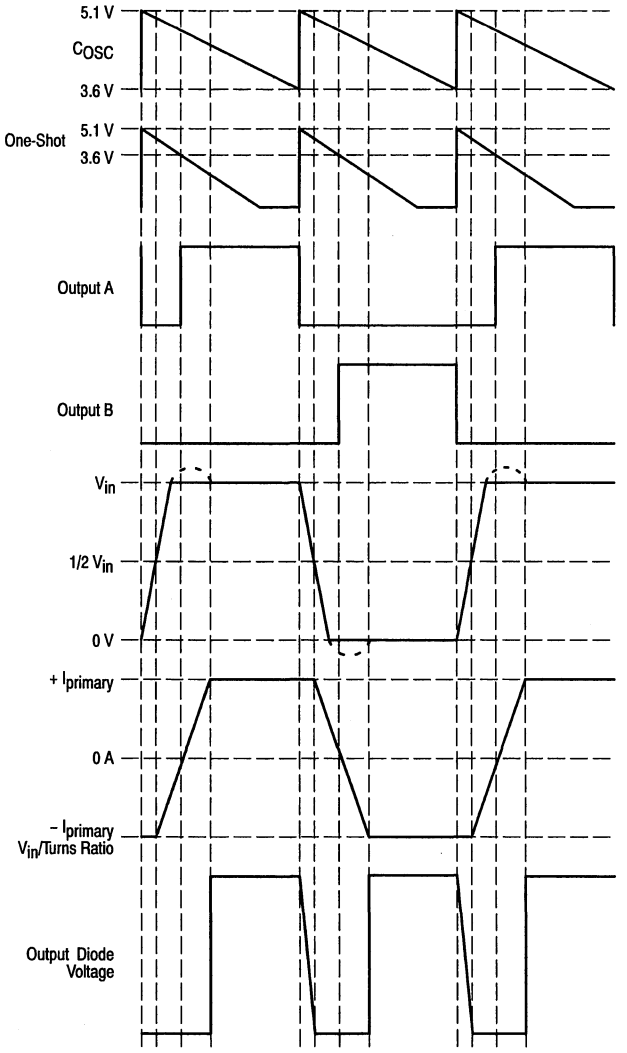
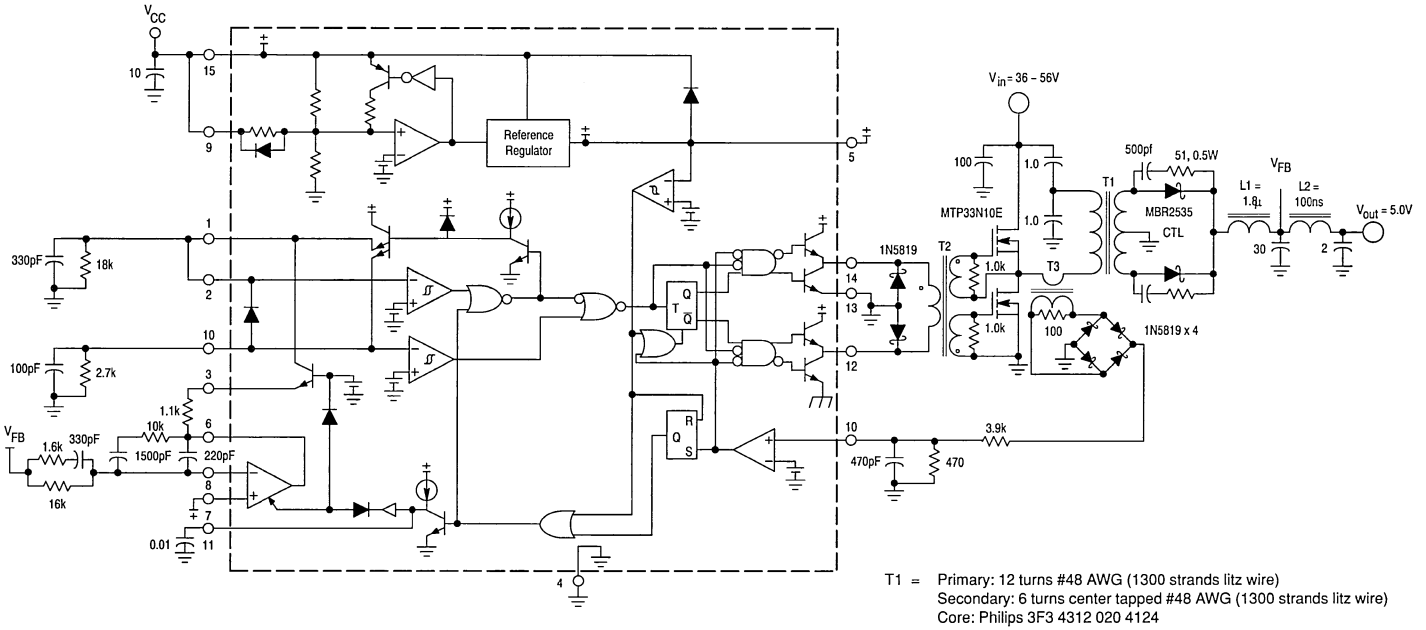


Figure 20. Application Circuit



Test	Conditions	Results
Line Regulation	V_{in} = 40 V to 56 V, I_O = 15 A	20 mV = ± 0.198%
Load Regulation	V_{in} = 48 V, I_O = 10 A to 15 A	4.0 mV = ± 0.039%
Output Ripple	V_{in} = 48 V, I_O = 15 A, f_{switch} = 1.0 MHz	26 mV_{p-p}
Efficiency	V_{in} = 48 V, I_O = 10 A, f_{switch} = 1.7 MHz V_{in} = 48 V, I_O = 15 A, f_{switch} = 1.0 MHz	83.5% 84.2%

T1 = Primary: 12 turns #48 AWG (1300 strands litz wire)
Secondary: 6 turns center tapped #48 AWG (1300 strands litz wire)
Core: Philips 3F3 4312 020 4124
Bobbin: Philips 4322 021 3525
Primary Leakage Inductance = 1.0 µH

T2 = All windings: 8 turns #36 AWG
Core: Philips 3F3 EP7-3F3
Bobbin: Philips EP7PCB1-6

T3 = Coilcraft D1870 (100 turns)

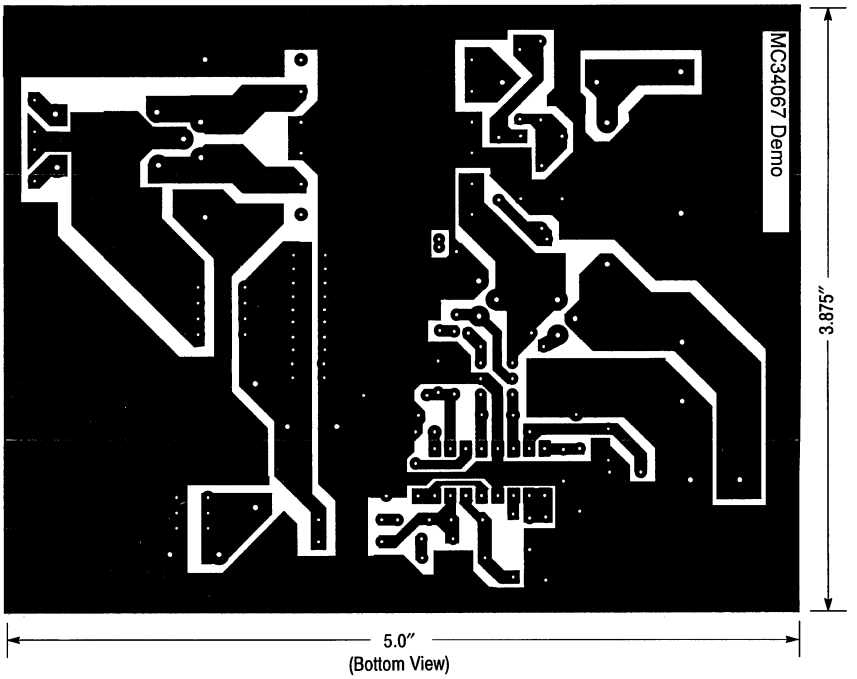
L1 = 2 turns #48 AWG (1300 strands litz wire)
Core: Philips 3F3 EP10-3F3
Bobbin: Philips EP10PCB1-8
Inductance = 1.8 µH

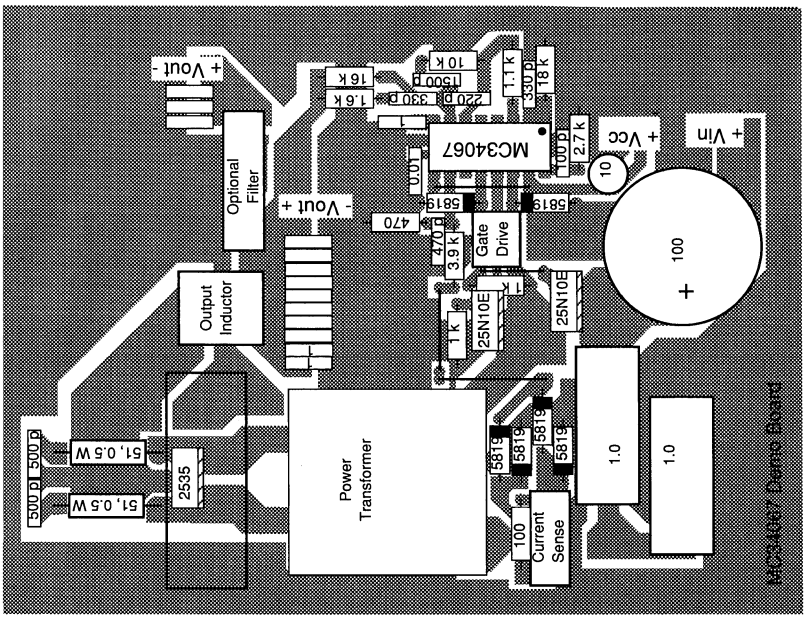
L2 = 5 turns #48 AWG (1300 strands litz wire)
Core: 0.5″ diameter air code
Inductance = 100 nH

Heatsinks = AAVID Engineering Inc. 533402B02552 with clip
MC34067–5803

Insulators = Berquist Sil-Pad 1500

Figure 21. Printed Circuit Board and Component Layout





(Top View)

MC34129
MC33129

HIGH PERFORMANCE CURRENT MODE CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

3

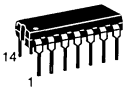
High Performance Current Mode Controller

The MC34129 series are high performance current mode switching regulators specifically designed for use in low power digital telephone applications. These integrated circuits feature a unique internal fault timer that provides automatic restart for overload recovery. For enhanced system efficiency, a start/run comparator is included to implement bootstrapped operation of V_{CC}. Other functions contained are a temperature compensated reference, reference amplifier, fully accessible error amplifier, sawtooth oscillator with sync input, pulse width modulator comparator, and a high current totem pole driver ideally suited for driving a power MOSFET.

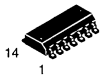
Also included are protective features consisting of soft-start, undervoltage lockout, cycle-by-cycle current limiting, adjustable dead time, and a latch for single pulse metering.

Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in many other applications.

- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-by-Cycle Current Limiting
- Continuous Retry after Fault Timeout
- Soft-Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- High Current Totem Pole Driver
- Input Undervoltage Lockout
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

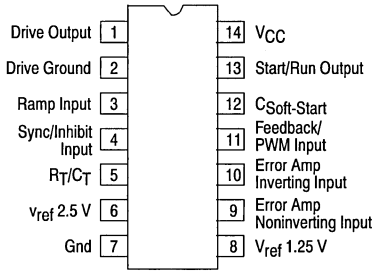


P SUFFIX
PLASTIC PACKAGE
CASE 646



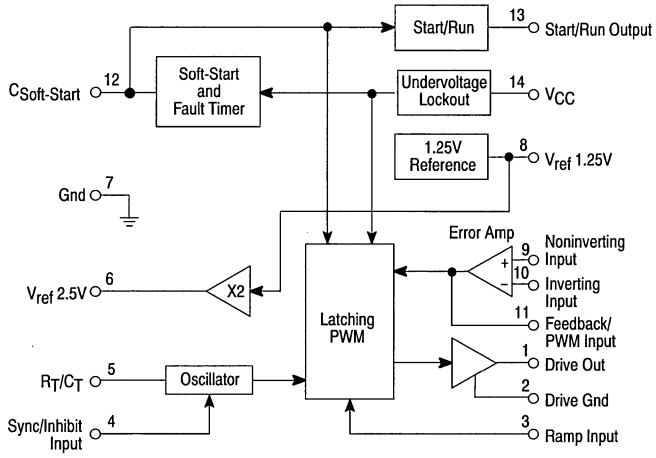
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram



ORDERING INFORMATION

Device	Temperature Range	Package
MC34129D	0° to +70°C	SO-14
MC34129P		Plastic DIP
MC33129D	–40° to +85°C	SO-14
MC33129P		Plastic DIP

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} Zener Current	$I_{Z(VCC)}$	50	mA
Start/Run Output Zener Current	$I_{Z(Start/Run)}$	50	mA
Analog Inputs (Pins 3, 5, 9, 10, 11, 12)	—	−0.3 to 5.5	V
Sync Input Voltage	V_{sync}	−0.3 to V_{CC}	V
Drive Output Current, Source or Sink	I_{DRV}	1.0	A
Current, Reference Outputs (Pins 6, 8)	I_{ref}	20	mA
Power Dissipation and Thermal Characteristics D Suffix Package SO-14 Case 751A-01 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air P Suffix Package Case 646-06 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 552 145 800 100	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34129 MC33129	T_A	 0 to +70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERICISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTIONS					
Reference Output Voltage, T_A = 25°C 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	V_{ref}	 1.225 2.375	 1.250 2.500	 1.275 2.625	V
Reference Output Voltage, T_A = T_{low} to T_{high} 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	V_{ref}	 1.200 2.250	 — —	 1.300 2.750	V
Line Regulation (V_{CC} = 4.0 V to 12 V) 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	Reg_{line}	 — —	 2.0 10	 12 50	mV
Load Regulation 1.25 V Ref., I_L = −10 μA to +500 μA 2.50 V Ref., I_L = −0.1 mA to +1.0 mA	Reg_{load}	 — —	 1.0 3.0	 12 25	mV
ERROR AMPLIFIER					
Input Offset Voltage (V_{in} = 1.25 V) T_A = 25°C T_A = T_{low} to T_{high}	V_{IO}	 — —	 1.5 —	 — 10	mV
Input Offset Current (V_{in} = 1.25 V)	I_{IO}	—	10	—	nA
Input Bias Current (V_{in} = 1.25 V) T_A = 25°C T_A = T_{low} to T_{high}	I_{IB}	 — —	 25 —	 — 200	nA
Input Common Mode Voltage Range	V_{ICR}	—	0.5 to 5.5	—	V
Open-Loop Voltage Gain (V_O = 1.25 V)	A_{VOL}	65	87	—	dB
Gain Bandwidth Product (V_O = 1.25 V, f = 100 kHz)	GBW	500	750	—	kHz
Power Supply Rejection Ratio (V_{CC} = 5.0 V to 10 V)	PSRR	65	85	—	dB
Output Source Current (V_O = 1.5 V)	I_{Source}	40	80	—	μA
Output Voltage Swing High State (I_{Source} = 0 μA) Low State (I_{Sink} = 500 μA)	 V_{OH} V_{OL}	 1.75 —	 1.96 0.1	 2.25 0.15	V

NOTE: 1. T_{low} = 0°C for MC34129, −40°C for MC33129; T_{high} = +70°C for MC34129, +85°C for MC33129

ELECTRICAL CHARACTERICISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR					
Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	150	275	400	mV
Input Bias Current	I_{IB}	—	–120	–250	µA
Propagation Delay, Ramp Input to Drive Output	$t_{PLH(IN/DRV)}$	—	250	—	ns
SOFT-START					
Capacitor Charge Current (Pin 12 = 0 V)	I_{chg}	0.75	1.2	1.50	µA
Buffer Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	—	15	40	mV
Buffer Output Voltage (I_{Sink} = 100 µA)	V_{OL}	—	0.15	0.225	V
FAULT TIMER					
Restart Delay Time	t_{DLY}	200	400	600	µs
START/RUN COMPARATOR					
Threshold Voltage (Pin 12)	V_{th}	—	2.0	—	V
Threshold Hysteresis Voltage (Pin 12)	V_H	—	350	—	mV
Output Voltage (I_{Sink} = 500 µA)	V_{OL}	9.0	10	10.3	V
Output Off-State Leakage Current (V_{OH} = 15 V)	$I_{S/R(leak)}$	—	0.4	2.0	µA
Output Zener Voltage (I_Z = 10 mA)	V_Z	—	(V_{CC} + 7.6)	—	V
OSCILLATOR					
Frequency (R_T = 25.5 kΩ, C_T = 390 pF)	f_{OSC}	80	100	120	kHz
Capacitor C_T Discharge Current (Pin 5 = 1.2 V)	I_{dischg}	240	350	460	µA
Sync Input Current High State (V_{in} = 2.0 V) Low State (V_{in} = 0.8 V)	 I_{IH} I_{IL}	 — —	 40 15	 125 35	µA
Sync Input Resistance	R_{in}	12.5	32	50	kΩ
DRIVE OUTPUT					
Output Voltage High State (I_{Source} = 200 mA) Low State (I_{Source} = 200 mA)	 V_{OH} V_{OL}	 8.3 —	 8.9 1.4	 — 1.8	V
Low State Holding Current	I_H	—	225	—	µA
Output Voltage Rise Time (C_L = 500 pF)	t_r	—	390	—	ns
Output Voltage Fall Time (C_L = 500 pF)	t_f	—	30	—	ns
Output Pull-Down Resistance	R_{PD}	100	225	350	kΩ
UNDERVOLTAGE LOCKOUT					
Start-Up Threshold	V_{th}	3.0	3.6	4.2	V
Hysteresis	V_H	5.0	10	15	%
TOTAL DEVICE					
Power Supply Current R_T = 25.5 kΩ, C_T = 390 pF, C_L = 500 pF	I_{CC}	1.0	2.5	4.0	mA
Power Supply Zener Voltage (I_Z = 10 mA)	V_Z	12	14.3	—	V

NOTE: 1. T_{low} = 0°C for MC34129, –40°C for MC33129 T_{high} = +70°C for MC34129, +85°C for MC33129

3

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Figure 1. Timing Resistor versus Oscillator Frequency

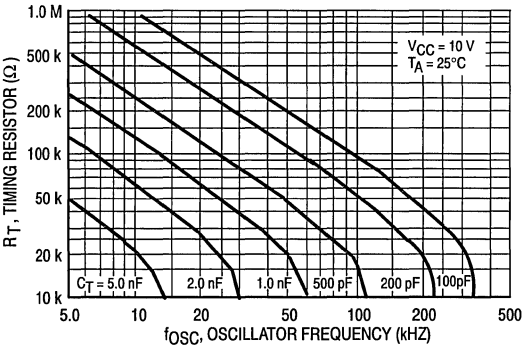

Figure 2. Output Dead-Time versus Oscillator Frequency

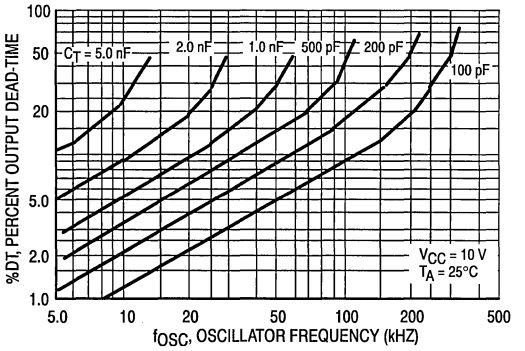

Figure 3. Oscillator Frequency Change versus Temperature

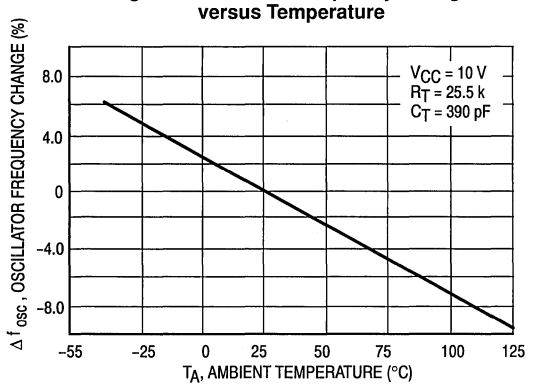

Figure 4. Error Amp Open-Loop Gain and Phase versus Frequency

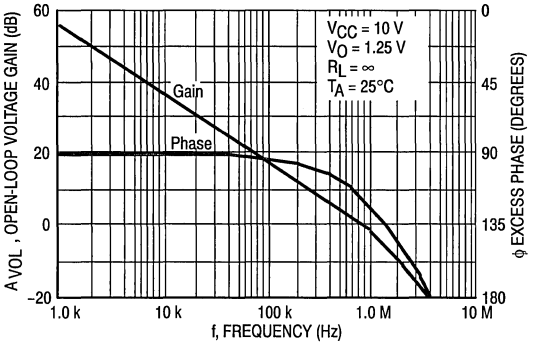

Figure 5. Error Amp Small-Signal Transient Response

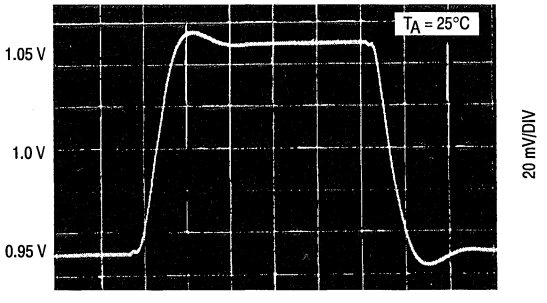

Figure 6. Error Amp Large-Signal Transient Response

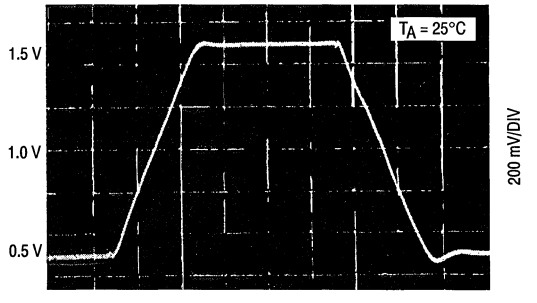

Figure 7. Error Amp Open-Loop DC Gain versus Load Resistance

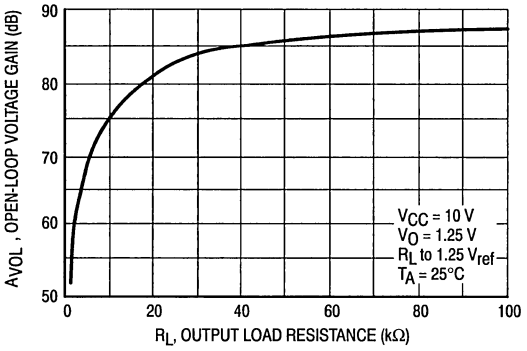

Figure 8. Error Amp Output Saturation versus Sink Current

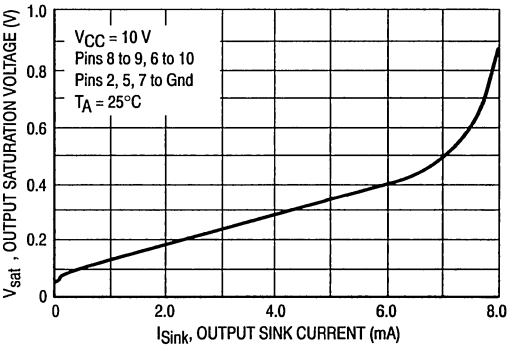

Figure 9. Soft-Start Buffer Output Saturation versus Sink Current

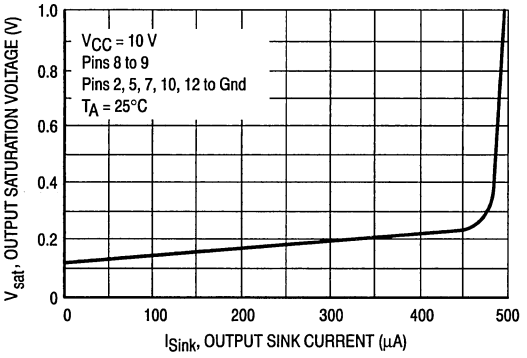

Figure 10. Reference Output Voltage versus Supply Voltage

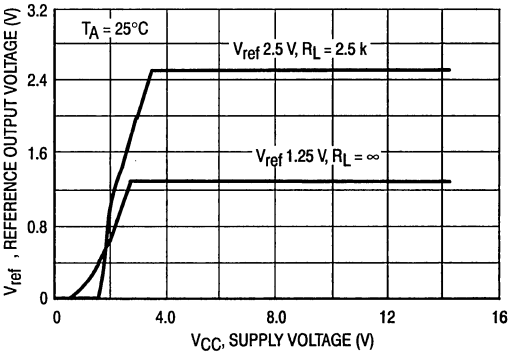

Figure 11. 1.25 V Reference Output Voltage Change versus Source Current

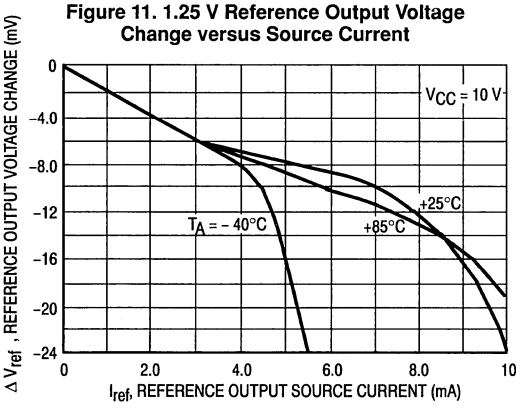

Figure 12. 2.5 V Reference Output Voltage Change versus Source Current

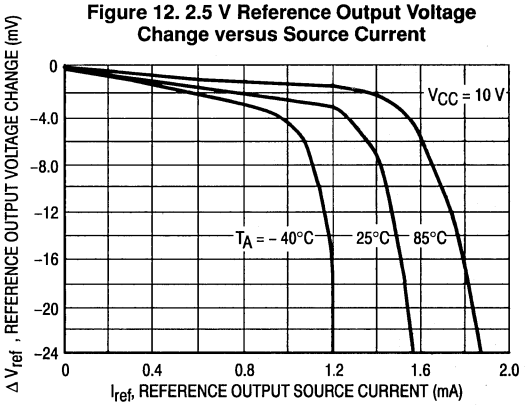

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Figure 13. 1.25 V Reference Output Voltage versus Temperature

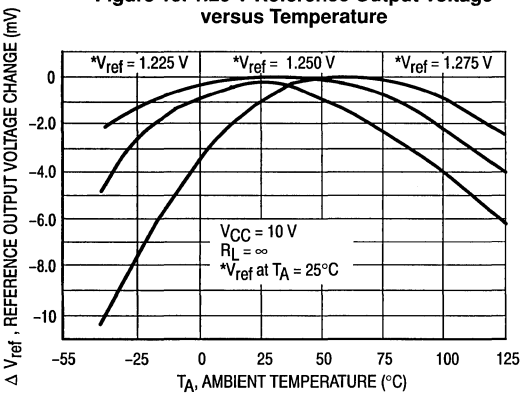


Figure 14. 2.5 V Reference Output Voltage versus Temperature

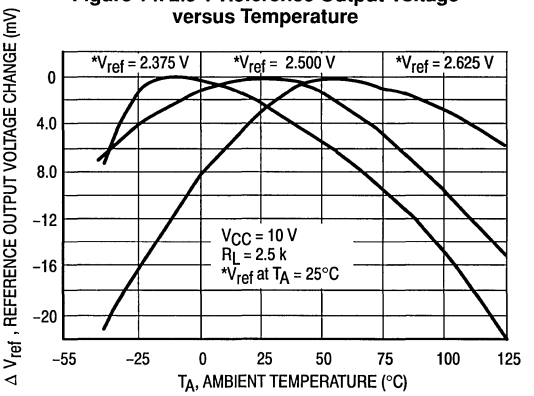


Figure 15. Drive Output Saturation versus Load Current

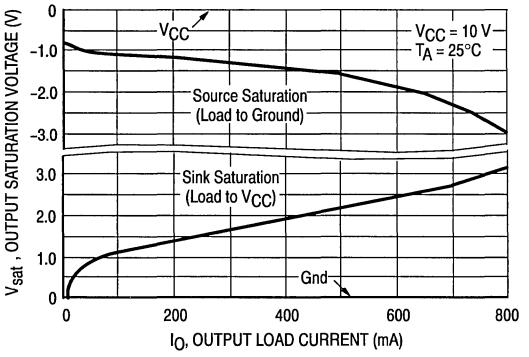


Figure 16. Drive Output Waveform

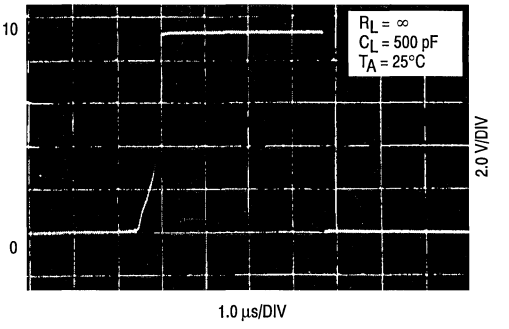
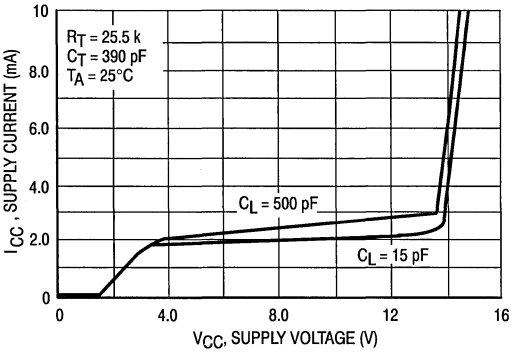


Figure 17. Supply Current versus Supply Voltage



PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	Drive Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sinked by this pin.
2	Drive Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
3	Ramp Input	A voltage proportional to the inductor current is connected to this input. The PWM uses this information to terminate output switch conduction.
4	Sync/Inhibit Input	A rectangular waveform applied to this input will synchronize the Oscillator and limit the maximum Drive Output duty cycle. A DC voltage within the range of 2.0 V to V_{CC} will inhibit the controller.
5	R_T/C_T	The free-running Oscillator frequency and maximum Drive Output duty cycle are programmed by connecting resistor R_T to V_{ref} 2.5 V and capacitor C_T to Ground. Operation to 300 kHz is possible.
6	V_{ref} 2.50 V	This output is derived from V_{ref} 1.25 V. It provides charging current for capacitor C_T through resistor R_T.
7	Ground	This pin is the control circuitry ground return and is connected back to the source ground.
8	V_{ref} 1.25 V	This output furnishes a voltage reference for the Error Amplifier noninverting input.
9	Error Amp Noninverting Input	This is the noninverting input of the Error Amplifier. It is normally connected to the 1.25 V reference.
10	Error Amp Inverting Input	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
11	Feedback/PWM Input	This pin is available for loop compensation. It is connected to the Error Amplifier and Soft-Start Buffer outputs, and the Pulse Width Modulator input.
12	$C_{Soft\text{-}Start}$	A capacitor $C_{Soft\text{-}Start}$ is connected from this pin to Ground for a controlled ramp-up of peak inductor current during start-up.
13	Start/Run Output	This output controls the state of an external bootstrap transistor. During the start mode, operating bias is supplied by the transistor from V_{in}. In the run mode, the transistor is switched off and bias is supplied by an auxiliary power transformer winding.
14	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a minimum V_{CC} range of 4.2 V to 12 V.

OPERATING DESCRIPTION

The MC34129 series are high performance current mode switching regulator controllers specifically designed for use in low power telecommunication applications. Implementation will allow remote digital telephones and terminals to shed their power cords and derive operating power directly from the twisted pair used for data transmission. Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in a wide range of converter applications. A representative block diagram is shown in Figure 18.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 2.5 V reference through resistor R_T to approximately 1.25 V and discharged by an internal current sink to ground. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the lower input of the NOR gate high. This causes the Drive Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows Oscillator Frequency versus R_T and Figure 2 Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a give frequency. In many noise sensitive applications it may be desirable to frequency-lock one or more switching regulators to an external system clock. This can be accomplished by applying the clock signal to the Synch/Inhibit Input. For reliable locking, the free-running oscillator frequency should be about 10% less than the clock frequency. Referring to the timing diagram shown Figure 19, the rising edge of the clock signal applied to the Sync/Inhibit Input, terminates charging of C_T and Drive Output conduction. By tailoring the clock waveform, accurate duty cycle clamping of the Drive Output can be achieved. A circuit method is shown in Figure 20. The Sync/Inhibit Input may also be used as a means for system shutdown by applying a DC voltage that is within the range of 2.0 V to V_{CC}.

PWM Comparator and Latch

The MC34129 operates as a current mode controller whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches a threshold level established by the output of the Error Amp or Soft-Start Buffer (Pin 11). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The PWM Comparator-Latch configuration used, ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground-referenced resistor R_S in series with the source of output switch Q_1. The Ramp Input adds an offset of 275 mV to this voltage to guarantee that no pulses appear at the Drive Output when Pin 11 is at its lowest state. This occurs at the beginning of the soft-start interval or when the power supply is operating and the load is removed. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 11 where:

$$I_{pk} = \frac{V_{(Pin\ 11)} - 0.275\ V}{R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the voltage at Pin 11 will be internally clamped to 1.95 V by the output of the Soft-Start Buffer. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.95\ V - 0.275}{R_S} = \frac{1.675\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method which adjusts this voltage in discrete increments is shown in Figure 22. This method is possible because the Ramp Input bias current is always negative (typically −120 μA). A positive temperature coefficient equal to that of the diode string will be exhibited by $I_{pk(max)}$. An adjustable method that is more precise and temperature stable is shown in Figure 23. Erratic operation due to noise pickup can result if there is an excessive reduction of the clamp voltage. In this situation, high frequency circuit layout techniques are imperative.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Ramp Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 25.

Error Amp and Soft-Start Buffer

A fully-compensated Error Amplifier with access to both inputs and output is provided for maximum design flexibility. The Error Amplifier output is common with that of the Soft-Start Buffer. These outputs are open-collector (sink only) and are ORed together at the inverting input of the PWM Comparator. With this configuration, the amplifier that demands lower peak inductor current dominates control of the loop. Soft-Start is mandatory for stable start-up when power is provided through a high source impedance such as the long twisted pair used in telecommunications. It effectively removes the load from the output of the switching power supply upon initial start-up. The Soft-Start Buffer is configured as a unity gain follower with the noninverting input connected to Pin 12. An internal 1.0 μA current source charges the soft-start capacitor ($C_{Soft\text{-}Start}$) to an internally clamped level of 1.95 V. The rate of change of peak inductor current, during start-up, is programmed by the capacitor value selected. Either the Fault Timer or the Undervoltage Lockout can discharge the soft-start capacitor.

Figure 18. Representative Block Diagram

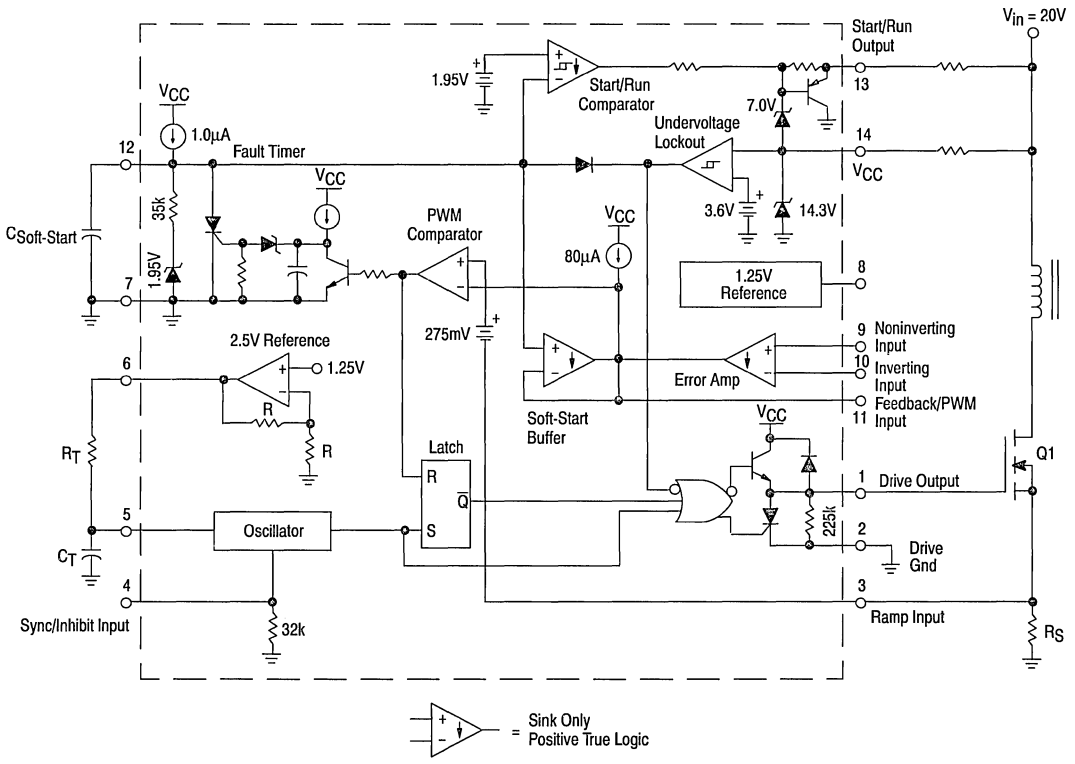
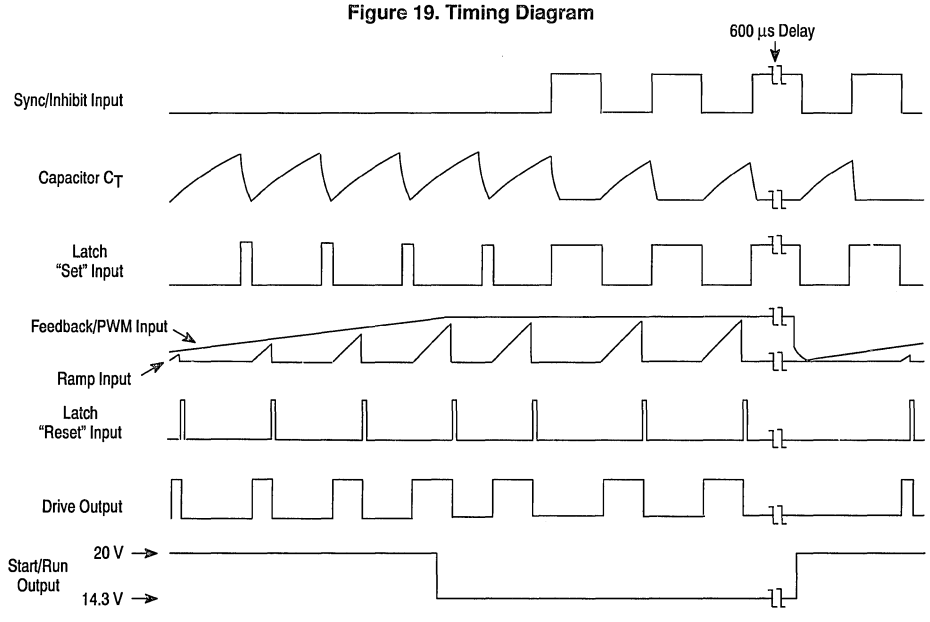


Figure 19. Timing Diagram



Fault Timer

This unique circuit prevents sustained operating in a lockout condition. This can occur with conventional switching control ICs when operating from a power source with a high series impedance. If the power required by the load is greater than that available from the source, the input voltage will collapse, causing the lockout condition. The Fault Timer provides automatic recovery when this condition is detected. Under normal operating conditions, the output of the PWM Comparator will reset the Latch and discharge the internal Fault Timer capacitor on a cycle-by-cycle basis. Under operating conditions where the required power into the load is greater than that available from the source (V_{in}), the Ramp Input voltage (plus offset) will not reach the comparator threshold level (Pin 11), and the output of the PWM Comparator will remain low. If this condition persists for more that 600 μs, the Fault Timer will active, discharging $C_{Soft\text{-}Start}$ and initiating a soft-start cycle. The power supply will operate in a skip cycle or hiccup mode until either the load power or source impedance is reduced. The minimum fault timeout is 200 μs, which limits the useful switching frequency to a minimum of 5.0 kHz.

Start/Run Comparator

A bootstrap start-up circuit is included to improve system efficiency when operating from a high input voltage. The output of the Start/Run Comparator controls the state of an external transistor. A typical application is shown in Figure 21. While $C_{Soft\text{-}Start}$ is charging, start-up bias is supplied to V_{CC} (Pin 14) from V_{in} through transistor Q2. When $C_{Soft\text{-}Start}$ reaches the 1.95 V clamp level, the Start-Run output switches low (V_{CC} = 50 mV), turning off Q2. Operating bias is now derived from the auxiliary bootstrap winding of the transformer, and all drive power is efficiently converted down from V_{in}. The start time must be long enough for the power supply output to reach regulation. This will ensure that there is sufficient bias voltage at the auxiliary bootstrap winding for sustained operation.

$$t_{Start} = \frac{1.95\ V\ C_{Soft\text{-}Start}}{1.0\ \mu A} = 1.95\ C_{Soft\text{-}Start\ in\ \mu F}$$

The Start/Run Comparator has 350 mV of hysteresis. The output off-state is clamped to V_{CC} + 7.6 V by the internal zener and PNP transistor base-emitter junction.

Drive Output and Drive Ground

The MC34129 contains a single totem-pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical fall time of 30 ns with a 500 pF load. The totem-pole stage consists of an NPN transistor for turn-on drive and a high speed SCR for turn-off. The SCR design requires less average supply current (I_{CC}) when compared to conventional switching control ICs that use an all NPN totem-pole. The SCR accomplishes this during turn-off of the MOSFET, by utilizing the gate charge as regenerative on-bias, whereas the conventional all transistor design requires continuous base current. Conversion efficiency in low power applications is greatly enhanced with this reduction of I_{CC}. The SCR's low-state holding current (I_H) is typically 225 μA. An internal 225 kΩ pull-down resistor is included to shunt the Drive Output off-state leakage to ground when the Undervoltage Lockout is active. A separate Drive Ground is provided to reduce the effects of switching transient noise imposed on the Ramp Input. This feature becomes particularly useful when the $I_{pk(max)}$ clamp level is reduced. Figure 24 shows the proper implementation of the MC34129 with a current sensing power MOSFET.

Undervoltage Lockout

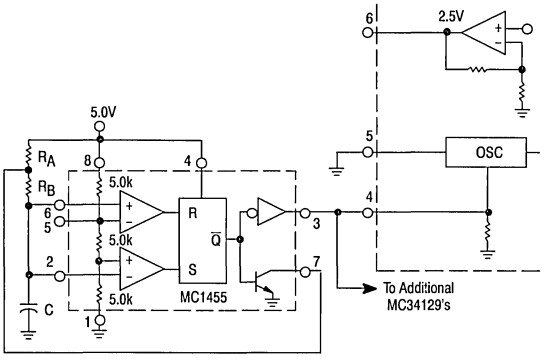
The Undervoltage Lockout comparator holds the Drive Output and $C_{Soft\text{-}Start}$ pins in the low state when V_{CC} is less than 3.6 V. This ensures that the MC34129 is fully functional before the output stage is enabled and a soft-start cycle begins. A built-in hysteresis of 350 mV prevents erratic output behavior as V_{CC} crosses the comparator threshold voltage. A 14.3 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the MOSFET gate from excessive drove voltage during system start-up. An external 9.1 V zener is required when driving low threshold MOSFETs. Refer to Figure 21. The minimum operating voltage range of the IC is 4.2 V to 12 V.

References

The 1.25 V bandgap reference is trimmed to ±2.0% tolerance at T_A = 25°C. It is intended to be used in conjunction with the Error Amp. The 2.50 V reference is derived from the 1.25 V reference by an internal op amp with a fixed gain of 2.0. It has an output tolerance of ±5.0% at T_A = 25°C and its primary purpose is to supply charging current to the oscillator timing capacitor.

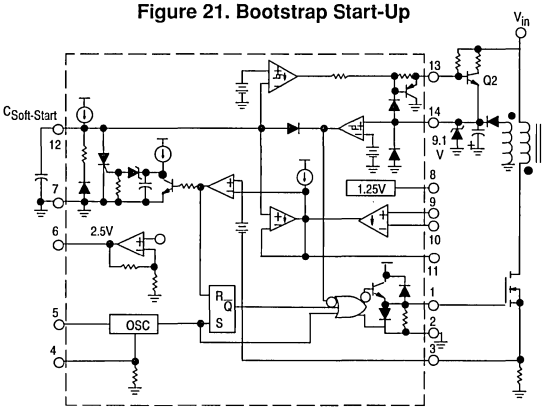
For further information, please refer to AN976.

Figure 20. External Duty Cycle Clamp and Multi Unit Synchronization



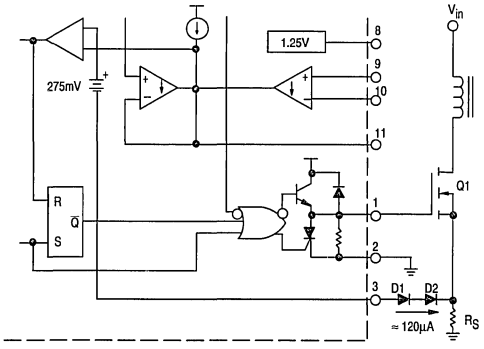
$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_B}{R_A + 2R_B}$$

Figure 21. Bootstrap Start-Up



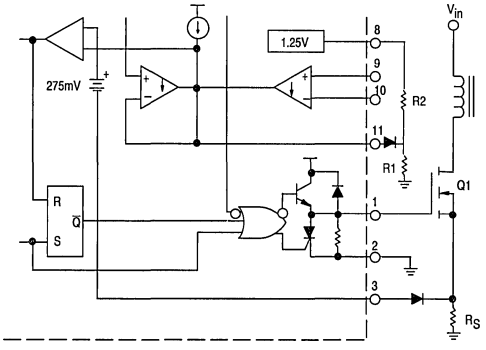
The external 9.1 V zener is required when driving low threshold MOSFETs.

Figure 22. Discrete Step Reduction of Clamp Level



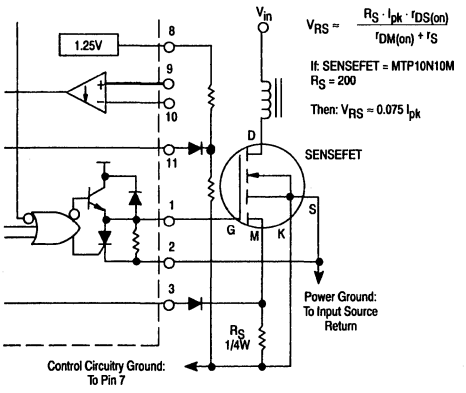
$$I_{pk(max)} = \frac{1.675 - (V_{F(D1)} + V_{F(D2)})}{R_S}$$

Figure 23. Adjustable Reduction of Clamp Level



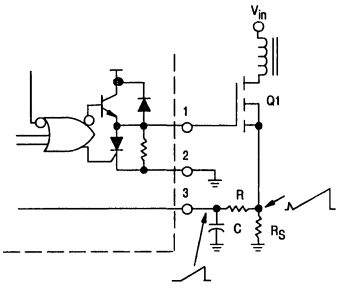
$$\text{If: } \frac{1.25\text{ V}}{R1 + R2} \geq 1.0\text{ mA} \qquad \text{Then: } I_{pk(max)} \approx \frac{\left(\frac{1.25}{\frac{R2}{R1} + 1}\right) - 0.275}{R_S}$$

Figure 24. Current Sensing Power MOSFET



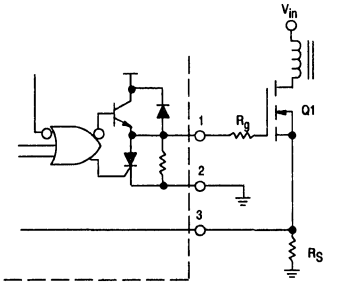
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch.

Figure 25. Current Waveform Spike Suppression



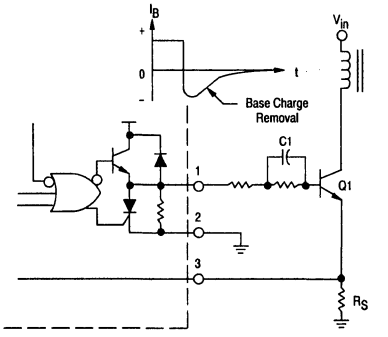
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 26. MOSFET Parasitic Oscillations



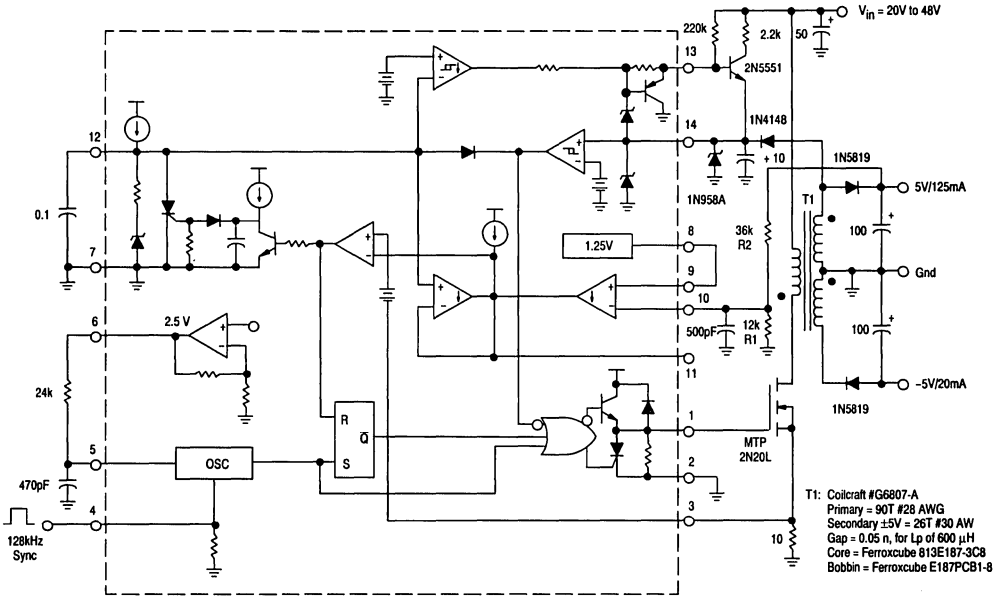
Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

Figure 27. Bipolar Transistor Drive



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C1.

Figure 28. Non-Isolated 725 mW Flyback Regulator

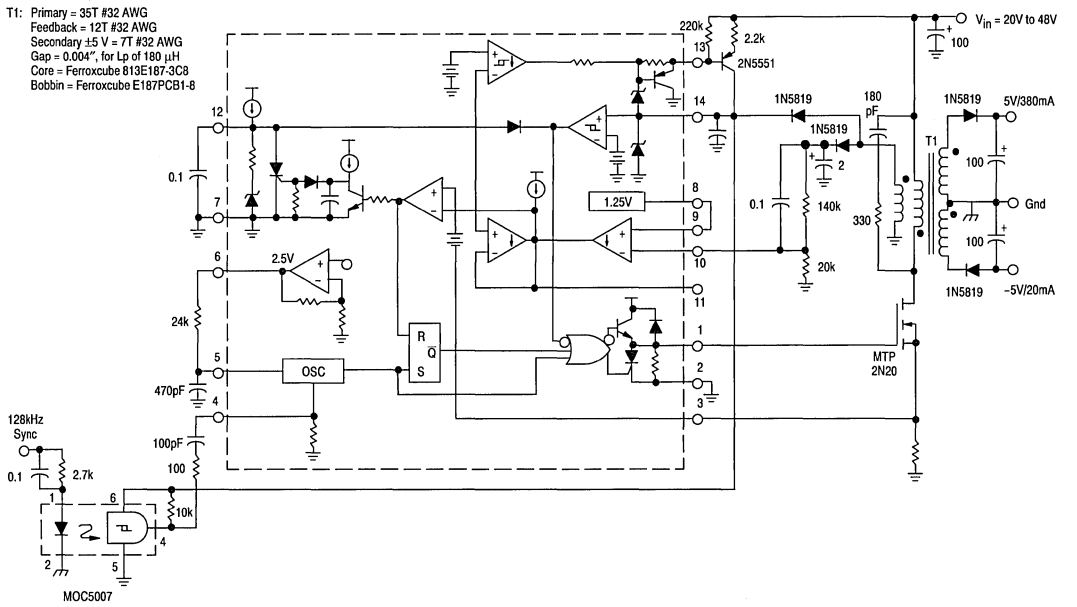


Test	Conditions	Results
Line Regulation 5 V	V_{in} = 20 V to 40 V, I_{out} 5 V = 125 mA, I_{out} −5 V = 20 mA	Δ = 1.0 mV
Load Regulation 5 V	V_{in} = 30 V, I_{out} 5 V = 0 mA to 150 mA, I_{out} −5 V = 20 mA	Δ = 2.0 mV
Output Ripple 5 V	V_{in} = 30 V, I_{out} 5 V = 125 mA, I_{out} −5 V = 20 mA	150 mVp-p
Efficiency	V_{in} = 30 V, I_{out} 5 V = 125 mA, I_{out} −5 V = 20 mA	77%

$$V_{out} = 1.25 \left(\frac{R2}{R1} + 1 \right)$$

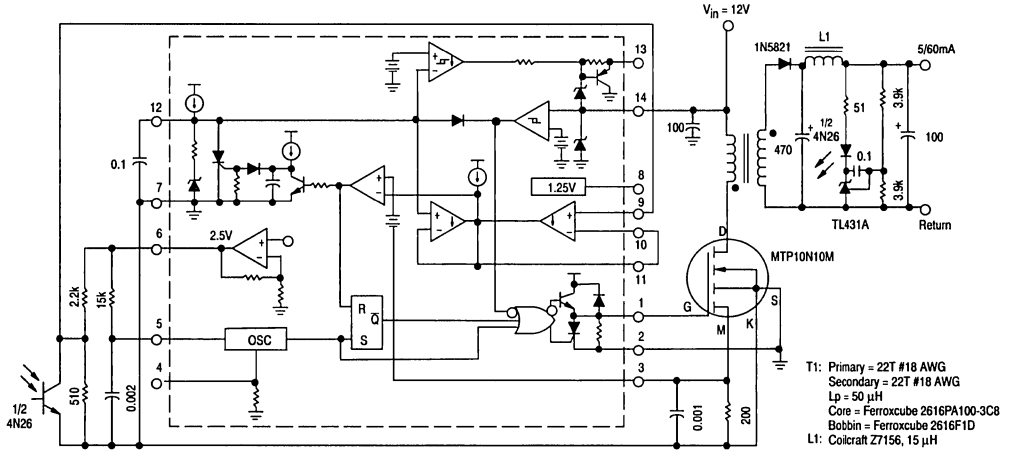
3

Figure 29. Isolated 2.0 W Flyback Regulator



Test	Conditions	Results
Line Regulation 5 V	V_{in} = 20 V to 40 V, I_{out} 5 V = 380 mA, I_{out} –5 V = 20 mA	Δ = 1 mV
Load Regulation 5 V	V_{in} = 30 V, I_{out} 5 V = 100 mA to 380 mA, I_{out} –5 V = 20 mA	Δ = 15 mV
Output Ripple 5 V	V_{in} = 30 V, I_{out} 5 V = 380 mA, I_{out} –5 V = 20 mA	150 mVp-p
Efficiency	V_{in} = 30 V, I_{out} 5 V = 380 mA, I_{out} –5 V = 20 mA	73%

Figure 30. Isolated 3.0 W Flyback Regulator with Secondary Side Sensing



Test	Conditions	Results
Line Regulation	V_{in} = 8 V to 12 V, I_{out} 600 mA	Δ = 1 mV
Load Regulation	V_{in} = 12 V, I_{out} = 100 mA to 600 mA	Δ = 8 mV
Output Ripple	V_{in} = 12 V, I_{out} = 600 mA	20 mVp-p
Efficiency	V_{in} = 12 V, I_{out} = 600 mA	81%

An economical method of achieving secondary sensing is to combine the TL431A with a 4N26 optocoupler.

MC34151
MC33151

3

Advance Information

High Speed Dual MOSFET Drivers

The MC34151/MC33151 is a dual inverting monolithic high speed driver specifically designed for applications that require low current digital circuitry to drive large capacitive loads with high slew rates. This device features low input current making it CMOS and LSTTL logic compatible, input hysteresis for fast output switching that is independent of input transition time, and two high current totem pole outputs ideally suited for driving power MOSFETs. Also included is an undervoltage lockout with hysteresis to prevent erratic system operation at low supply voltages.

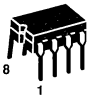
Typical applications include switching power supplies, DC to DC converters, capacitor charge pump voltage doublers/inverters, and motor controllers.

These devices are available in dual-in-line and surface mount packages.

- Two Independent Channels with 1.5 A Totem Pole Output
- Output Rise and Fall Times of 15 ns with 1000 pF Load
- CMOS/LSTTL Compatible Inputs with Hysteresis
- Undervoltage Lockout with Hysteresis
- Low Standby Current
- Efficient High Frequency Operation
- Enhanced System Performance with Common Switching Regulator Control ICs
- Pin Out Equivalent to DS0026 and MMH0026

HIGH SPEED
DUAL MOSFET DRIVERS

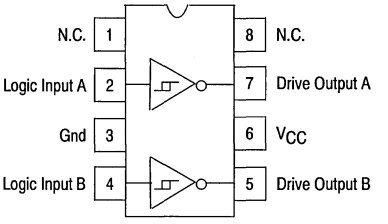
SILICON MONOLITHIC
INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 626

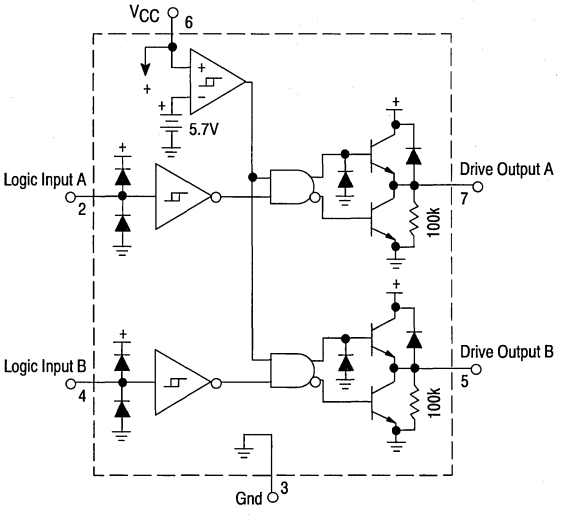
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



(Top View)

Block Diagram



ORDERING INFORMATION

Device	Temperature Range	Package
MC34151D	0° to +70°C	SO-8
MC34151P		Plastic DIP
MC33151D	–40° to +85°C	SO-8
MC33151P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Logic Inputs (Note 1)	V_{in}	−0.3 to V_{CC}	V
Drive Outputs (Note 2)			A
Totem Pole Sink or Source Current	I_O	1.5	
Diode Clamp Current (Drive Output to V_{CC})	$I_{O(clamp)}$	1.0	
Power Dissipation and Thermal Characteristics			
D Suffix SO-8 Package Case 751			
Maximum Power Dissipation @ T_A = 50°C	P_D	0.56	W
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	180	°C/W
P Suffix 8-Pin Package Case 626			
Maximum Power Dissipation @ T_A = 50°C	P_D	1.0	W
Thermal Resistance Junction-to-Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
MC34151		0 to +70	
MC33151		−40 to +85	
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERICISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the only operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Threshold Voltage — High State Logic 1	V_{IH}	2.6	1.75	—	V
— Low State Logic 0	V_{IL}	—	1.58	0.8	
Input Current — High State (V_{IH} = 2.6 V)	I_{IH}	—	200	500	μA
— Low State (V_{IL} = 0.8 V)	I_{IL}	—	20	100	
DRIVE OUTPUT					
Output Voltage — Low State (I_{Sink} = 10 mA)	V_{OL}	—	0.8	1.2	V
(I_{Sink} = 50 mA)		—	1.1	1.5	
(I_{Sink} = 400 mA)		—	1.7	2.5	
— High State (I_{Source} = 10 mA)	V_{OH}	10.5	11.2	—	
(I_{Source} = 50 mA)		10.4	11.1	—	
(I_{Source} = 400 mA)		9.5	10.9	—	
Output Pull-Down Resistor	R_{PD}	—	100	—	kΩ
SWITCHING CHARACTERISTICS (T_A = 25°C)					
Propagation Delay (10% Input to 10% Output, C_L = 1.0 nF)					ns
Logic Input to Drive Output Rise	$t_{PLH(in/out)}$	—	35	100	
Logic Input to Drive Output Fall	$t_{PHL(in/out)}$	—	36	100	
Drive Output Rise Time (10% to 90%) C_L = 1.0 nF	t_r	—	14	30	ns
C_L = 2.5 nF		—	31	—	
Drive Output Fall Time (90% to 10%) C_L = 1.0 nF	t_f	—	16	30	ns
C_L = 2.5 nF		—	32	—	
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Standby (Logic Inputs Grounded)		—	6.0	10	
Operating (C_L = 1.0 nF Drive Outputs 1 and 2, f = 100 kHz)		—	10.5	15	
Operating Voltage	V_{CC}	6.5	—	18	V

NOTES: 1. For optimum switching speed, the maximum input voltage should be limited to 10 V or V_{CC}, whichever is less.
2. Maximum package power dissipation limits must be observed.
3. T_{low} = 0°C for MC34151, −40°C for MC33151; T_{high} = +70°C for MC34151, +85°C for MC33151

3

Figure 1. Switching Characteristics Test Circuit

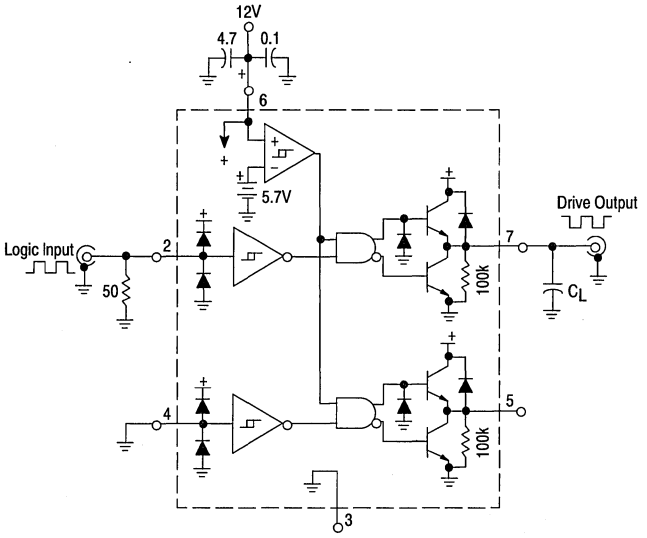


Figure 2. Switching Waveform Definitions

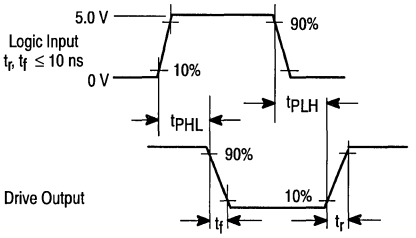


Figure 3. Logic Input Current versus Input Voltage

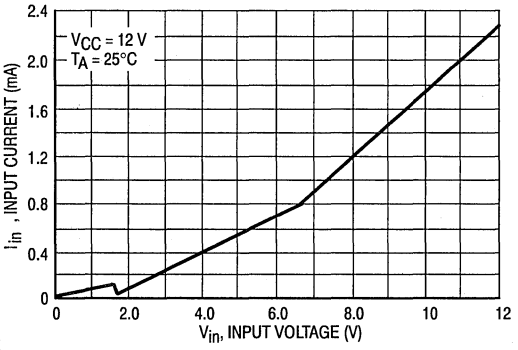


Figure 4. Logic Input Threshold Voltage versus Temperature

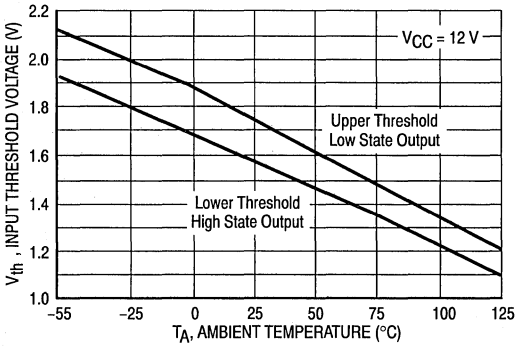


Figure 5. Drive Output Low-to-High Propagation Delay versus Logic Overdrive Voltage

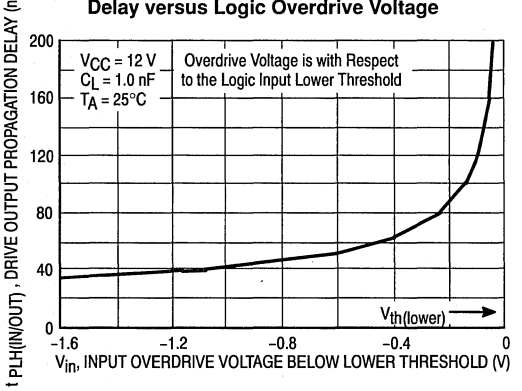


Figure 6. Drive Output High-to-Low Propagation Delay versus Logic Input Overdrive Voltage

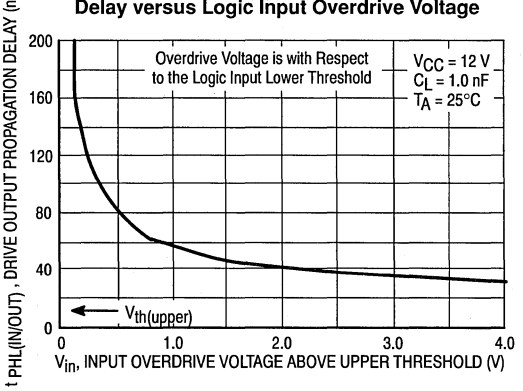


Figure 7. Propagation Delay

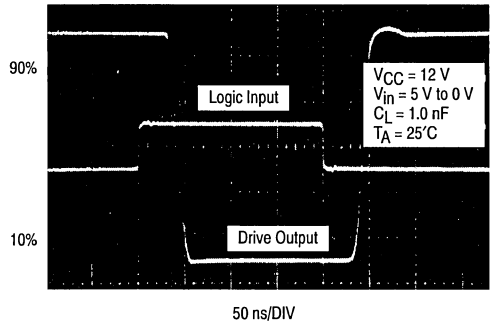


Figure 8. Drive Output Clamp Voltage versus Clamp Current

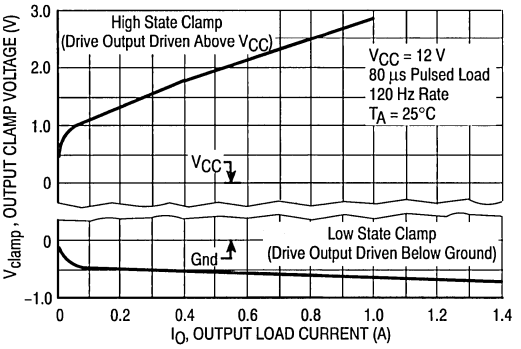


Figure 9. Drive Output Saturation Voltage versus Load Current

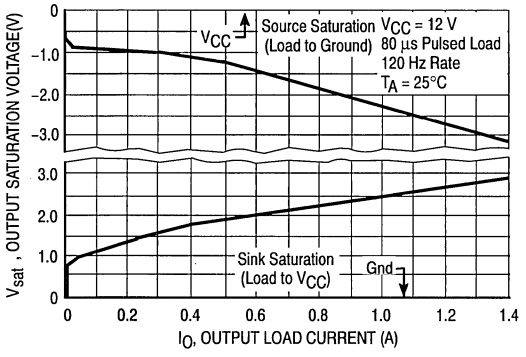


Figure 10. Drive Output Saturation Voltage versus Temperature

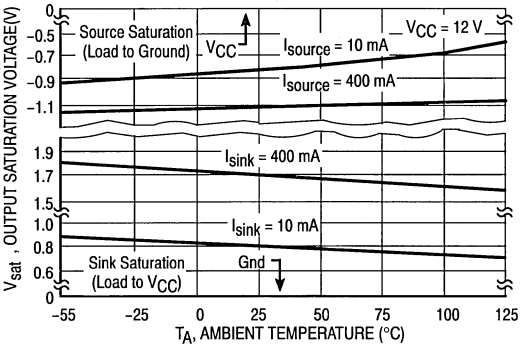


Figure 11. Drive Output Rise Time

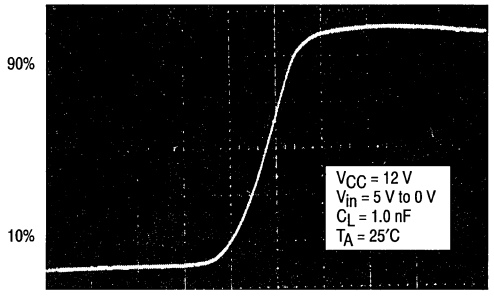


Figure 12. Drive Output Fall Time

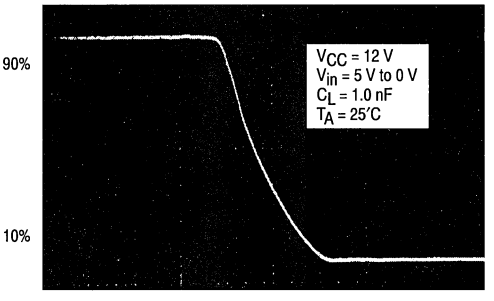


Figure 13. Drive Output Rise and Fall Time versus Load Capacitance

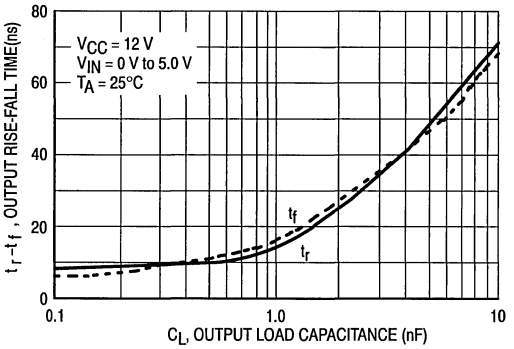


Figure 14. Supply Current versus Drive Output Load Capacitance

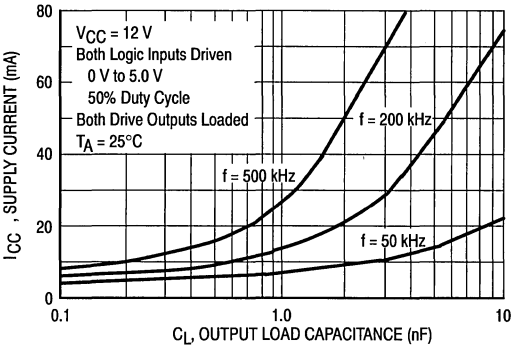


Figure 15. Supply Current versus Input Frequency

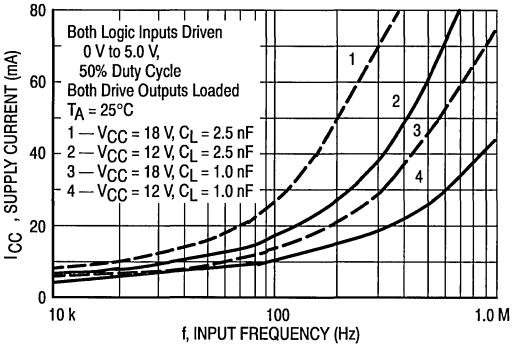
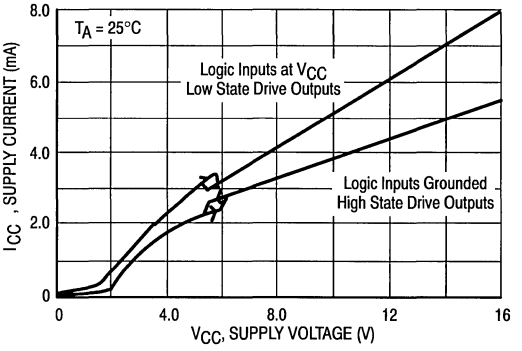


Figure 16. Supply Current versus Supply Voltage



APPLICATIONS INFORMATION

Description

The MC34151 is a dual inverting high speed driver specifically designed to interface low current digital circuitry with power MOSFETs. This device is constructed with Schottky clamped Bipolar Analog technology which offers a high degree of performance and ruggedness in hostile industrial environments.

Input Stage

The Logic Inputs have 170 mV of hysteresis with the input threshold centered at 1.67 V. The input thresholds are insensitive to V_{CC} making this device directly compatible with CMOS and LSTTL logic families over its entire operating voltage range. Input hysteresis provides fast output switching that is independent of the input signal transition time, preventing output oscillations as the input thresholds are crossed. The inputs are designed to accept a signal amplitude ranging from ground to V_{CC}. This allows the output of one channel to directly drive the input of a second channel for master-slave operation. Each input has a 30 kΩ pull-down resistor so that an unconnected open input will cause the associated Drive Output to be in a known high state.

Output Stage

Each totem pole Drive Output is capable of sourcing and sinking up to 1.5 A with a typical 'on' resistance of 2.4 Ω at 1.0 A. The low 'on' resistance allows high output currents to be attained at a lower V_{CC} than with comparative CMOS drivers. Each output has a 100 kΩ pull-down resistor to keep the MOSFET gate low when V_{CC} is less than 1.4 V. No over current or thermal protection has been designed into the device, so output shorting to V_{CC} or ground must be avoided.

Parasitic inductance in series with the load will cause the driver outputs to ring above V_{CC} during the turn-on transition, and below ground during the turn-off transition. With CMOS drivers, this mode of operation can cause a destructive output latch-up condition. The MC34151 is immune to output latch-up. The Drive Outputs contain an internal diode to V_{CC} for clamping positive voltage transients. When operating with V_{CC} at 18 V, proper power supply bypassing must be observed to prevent the output ringing from exceeding the maximum 20 V device rating. Negative output transients are clamped by the internal NPN pull-up transistor. Since full supply voltage is applied across the NPN pull-up during the negative output transient, power dissipation at high

frequencies can become excessive. Figures 19, 20, and 21 show a method of using external Schottky diode clamps to reduce driver power dissipation.

Undervoltage Lockout

An undervoltage lockout with hysteresis prevents erratic system operation at low supply voltages. The UVLO forces the Drive Outputs into a low state as V_{CC} rises from 1.4 V to the 5.8 V upper threshold. The lower UVLO threshold is 5.3 V, yielding about 500 mV of hysteresis.

Power Dissipation

Circuit performance and long term reliability are enhanced with reduced die temperature. Die temperature increase is directly related to the power that the integrated circuit must dissipate and the total thermal resistance from the junction to ambient. The formula for calculating the junction temperature with the package in free air is:

$$T_J = T_A + P_D (R_{\theta JA})$$

where: T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
$R_{\theta JA}$ = Thermal Resistance Junction to Ambient

There are three basic components that make up total power to be dissipated when driving a capacitive load with respect to ground. They are:

$$P_D = P_Q + P_C + P_T$$

where: P_Q = Quiescent Power Dissipation
P_C = Capacitive Load Power Dissipation
P_T = Transition Power Dissipation

The quiescent power supply current depends on the supply voltage and duty cycle as shown in Figure 16. The device's quiescent power dissipation is:

$$P_Q = V_{CC} \left(I_{CCL} (1-D) + I_{CCH} (D) \right)$$

where: I_{CCL} = Supply Current with Low State Drive Outputs
I_{CCH} = Supply Current with High State Drive Outputs
D = Output Duty Cycle

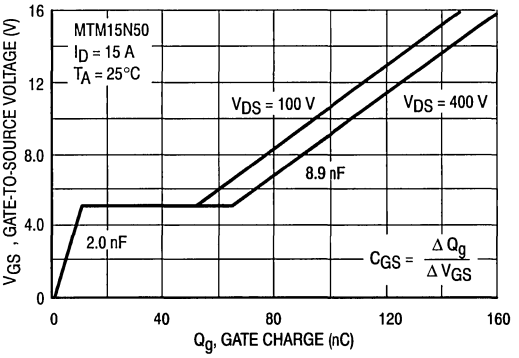
The capacitive load power dissipation is directly related to the load capacitance value, frequency, and Drive Output voltage swing. The capacitive load power dissipation per driver is:

$$P_C = V_{CC} (V_{OH} - V_{OL}) C_L f$$

where: V_{OH} = High State Drive Output Voltage
V_{OL} = Low State Drive Output Voltage
C_L = Load Capacitance
f = frequency

When driving a MOSFET, the calculation of capacitive load power P_C is somewhat complicated by the changing gate to source capacitance C_{GS} as the device switches. To aid in this calculation, power MOSFET manufacturers provide gate charge information on their data sheets. Figure 17 shows a curve of gate voltage versus gate charge for the Motorola MTM15N50. Note that there are three distinct slopes to the curve representing different input capacitance values. To completely switch the MOSFET 'on', the gate must be brought to 10 V with respect to the source. The graph shows that a gate charge Q_g of 110 nC is required when operating the MOSFET with a drain to source voltage V_{DS} of 400 V.

Figure 17. Gate-To-Source Voltage versus Gate Charge



The capacitive load power dissipation is directly related to the required gate charge, and operating frequency. The capacitive load power dissipation per driver is:

$$P_{C(MOSFET)} = V_C Q_g f$$

The flat region from 10 nC to 55 nC is caused by the drain-to-gate Miller capacitance, occuring while the MOSFET is in the linear region dissipating substantial amounts of power. The high output current capability of the MC34151 is able to quickly deliver the required gate charge for fast power efficient MOSFET switching. By operating the MC34151 at a higher V_{CC}, additional charge can be provided to bring the gate above 10 V. This will reduce the 'on' resistance of the MOSFET at the expense of higher driver dissipation at a given operating frequency.

The transition power dissipation is due to extremely short simultaneous conduction of internal circuit nodes when the Drive Outputs change state. The transition power dissipation per driver is approximately:

$$P_T \approx V_{CC} (1.08 V_{CC} C_L f - 8 \times 10^{-4})$$

P_T must be greater than zero.

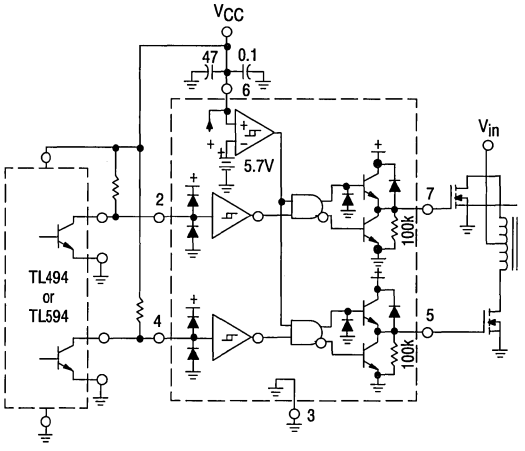
Switching time characterization of the MC34151 is performed with fixed capacitive loads. Figure 13 shows that for small capacitance loads, the switching speed is limited by transistor turn-on/off time and the slew rate of the internal nodes. For large capacitance loads, the switching speed is limited by the maximum output current capability of the integrated circuit.

LAYOUT CONSIDERATIONS

High frequency printed circuit layout techniques are imperative to prevent excessive output ringing and overshoot. **Do not attempt to construct the driver circuit on wire-wrap or plug-in prototype boards.** When driving large capacitive loads, the printed circuit board must contain a low inductance ground plane to minimize the voltage spikes induced by the high ground ripple currents. All high current loops should be kept as short as possible using heavy copper runs to provide a low impedance high frequency path. For optimum drive performance, it is recommended that the initial circuit design contains dual power supply bypass capacitors connected with short leads as close to the V_{CC} pin and ground as the layout will permit. Suggested capacitors are a low inductance 0.1 μF ceramic in parallel with a 4.7 μF tantalum. Additional bypass capacitors may be required depending upon Drive Output loading and circuit layout.

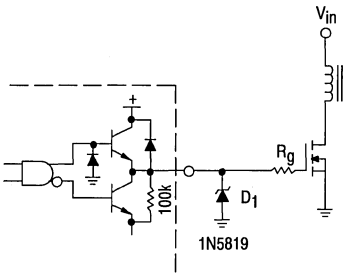
Proper printed circuit board layout is extremely critical and cannot be over emphasized.

Figure 18. Enhanced System Performance with Common Switching Regulators



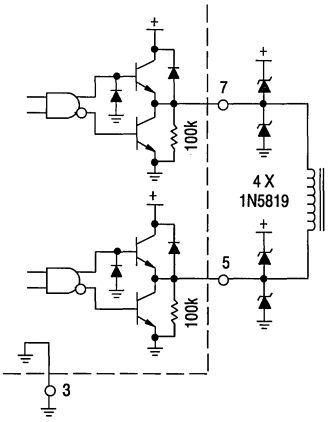
The MC34151 greatly enhances the drive capabilities of common switching regulators and CMOS/TTL logic devices.

Figure 19. MOSFET Parasitic Oscillations



Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D_1 can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 20. Direct Transformer Drive



Output Schottky diodes are recommended when driving inductive loads at high frequencies. The diodes reduce the driver's power dissipation by preventing the output pins from being driven above V_{CC} and below ground.

Figure 21. Isolated MOSFET Drive

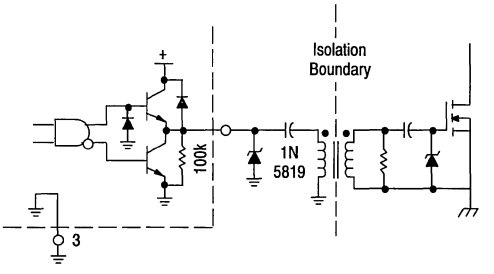
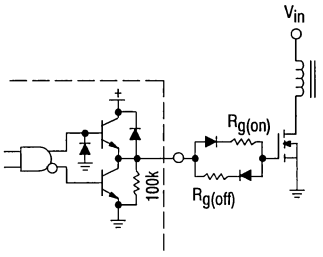
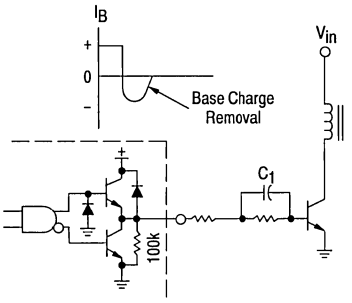


Figure 22. Controlled MOSFET Drive



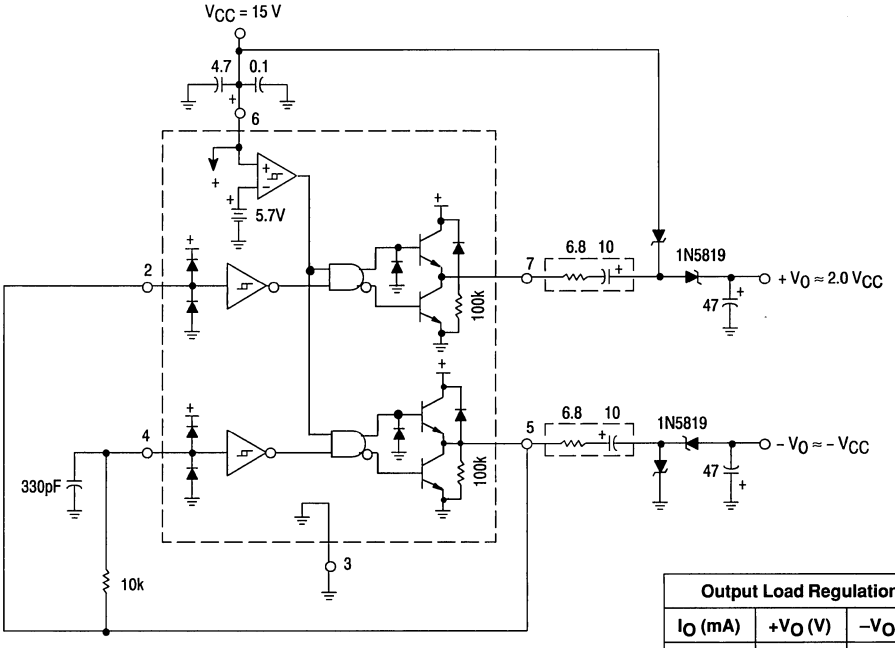
In noise sensitive applications, both conducted and radiated EMI can be reduced significantly by controlling the MOSFET's turn-on and turn-off times.

Figure 23. Bipolar Transistor Drive



The totem-pole outputs can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1.

Figure 24. Dual Charge Pump Converter



The capacitor's equivalent series resistance limits the Drive Output Current to 1.5 A. An additional series resistor may be required when using tantalum or other low ESR capacitors.

Output Load Regulation		
I_O (mA)	$+V_O$ (V)	$-V_O$ (V)
0	27.7	–13.3
1.0	27.4	–12.9
10	26.4	–11.9
20	25.5	–11.2
30	24.6	–10.5
50	22.6	–9.4

MC34152
MC33152

3

High Speed Dual MOSFET Drivers

The MC34152/MC33152 is a dual noninverting monolithic high speed driver specifically designed for applications that require low current digital signals to drive large capacitive loads with high slew rates. This device features low input current making it CMOS/LSTTL logic compatible, input hysteresis for fast output switching that is independent of input transition time, and two high current totem pole outputs ideally suited for driving power MOSFETs. Also included is an undervoltage lockout with hysteresis to prevent system erratic operation at low supply voltages.

Typical applications include switching power supplies, DC-to-DC converters, capacitor charge pump voltage doublers/inverters, and motor controllers.

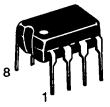
This device is available in dual-in-line and surface mount packages.

- Two Independent Channels with 1.5 A Totem Pole Outputs
- Output Rise and Fall Times of 15 ns with 1000 pF Load
- CMOS/LSTTL Compatible Inputs with Hysteresis
- Undervoltage Lockout with Hysteresis
- Low Standby Current
- Efficient High Frequency Operation
- Enhanced System Performance with Common Switching Regulator Control ICs

HIGH SPEED DUAL MOSFET DRIVERS

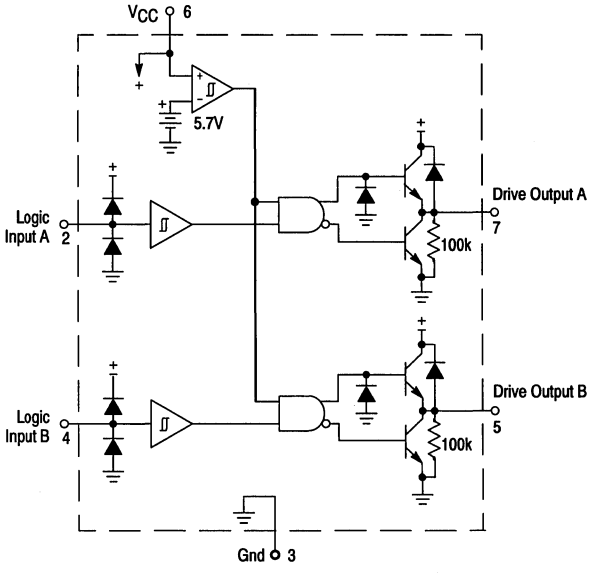
SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 626

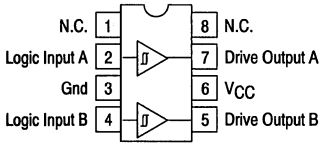


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34152D	0° to +70°C	SO-8
MC34152P		Plastic DIP
MC33152D	– 40° to +85°C	SO-8
MC33152P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Logic Inputs (Note 1)	V_{in}	–0.3 to +V_{CC}	V
Drive Outputs (Note 2)			A
Totem Pole Sink or Source Current	I_O	1.5	
Diode Clamp Current (Drive Output to V_{CC})	$I_{O(clamp)}$	1.0	
Power Dissipation and Thermal Characteristics			
D Suffix Package, SO-8 Case 751			
Maximum Power Dissipation @ T_A = 50°C	P_D	0.56	W
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	180	°C/W
P Suffix 8-Pin Package, Case 626			
Maximum Power Dissipation @ T_A = 50°C	P_D	1.0	W
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34152	T_A	0 to +70	°C
MC33152		–40 to +85	
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Threshold Voltage					V
High State Logic 1	V_{IH}	2.6	1.75	—	
Low State Logic 0	V_{IL}	—	1.58	0.9	
Input Current					μA
High State (V_{IH} = 2.6 V)	I_{IH}	—	100	300	
Low State (V_{IL} = 0.8 V)	I_{IL}	—	20	100	
DRIVE OUTPUT					
Output Voltage					V
Low State (I_{sink} = 10 mA)	V_{OL}	—	0.8	1.2	
(I_{sink} = 50 mA)		—	1.1	1.5	
(I_{sink} = 400 mA)		—	1.8	2.5	
High State (I_{source} = 10 mA)	V_{OH}	10.5	11.2	—	
(I_{source} = 50 mA)		10.4	11.1	—	
(I_{source} = 400 mA)		10	10.8	—	
Output Pull-Down Resistor	R_{PD}	—	100	—	kΩ
SWITCHING CHARACTERISTICS (T_A = 25°C)					
Propagation Delay (C_L = 1.0 nF)					ns
Logic Input to:					
Drive Output Rise (10% Input to 10% Output)	t_{PLH} (IN/OUT)	—	55	120	
Drive Output Fall (90% Input to 90% Output)	t_{PHL} (IN/OUT)	—	40	120	
Drive Output Rise Time (10% to 90%) C_L = 1.0 nF	t_r	—	14	30	ns
C_L = 2.5 nF		—	36	—	
Drive Output Fall Time (90% to 10%) C_L = 1.0 nF	t_f	—	15	30	ns
C_L = 2.5 nF		—	32	—	
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Standby (Logic Inputs Grounded)		—	6.0	8.0	
Operating (C_L = 1.0 nF Drive Outputs 1 and 2, f = 100 kHz)		—	10.5	15	
Operating Voltage	V_{CC}	6.5	—	18	V

NOTES: 1. For optimum switching speed, the maximum input voltage should be limited to 10 V or V_{CC}, whichever is less.
2. Maximum package power dissipation limits must be observed.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34152 = –40°C for MC33152 T_{high} = +70°C for MC34152 = +85°C for MC33152

3

Figure 1. Switching Characteristics Test Circuit

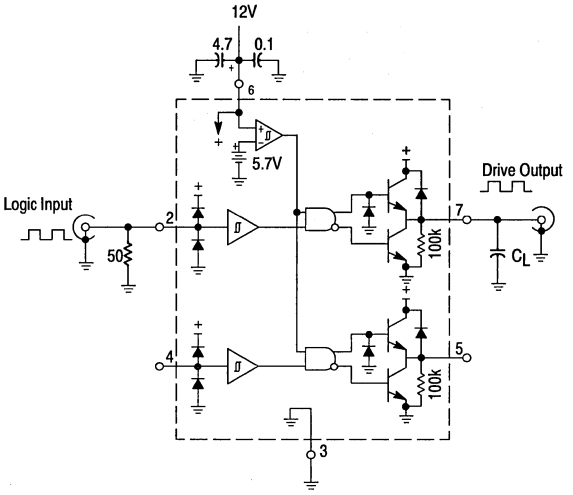


Figure 2. Switching Waveform Definitions

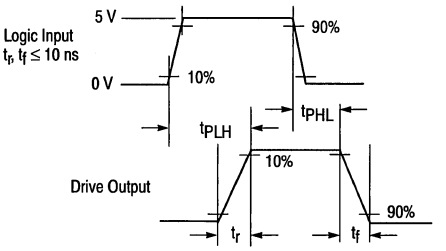


Figure 3. Logic Input Current versus Input Voltage

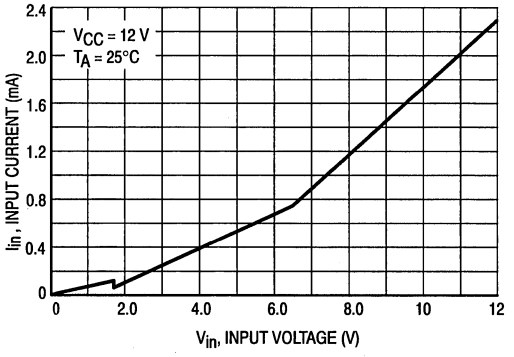


Figure 4. Logic Input Threshold Voltage versus Temperature

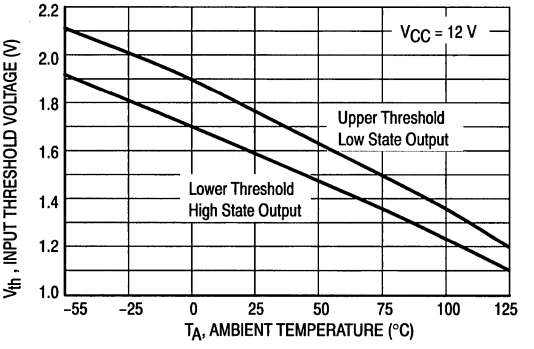


Figure 5. Drive Output High to Low Propagation Delay versus Logic Input Overdrive Voltage

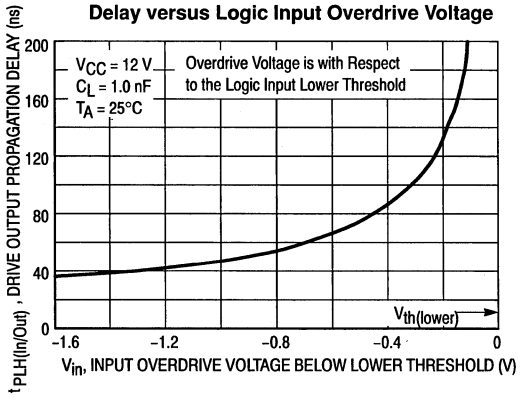


Figure 6. Drive Output Low to High Propagation Delay versus Logic Input Overdrive Voltage

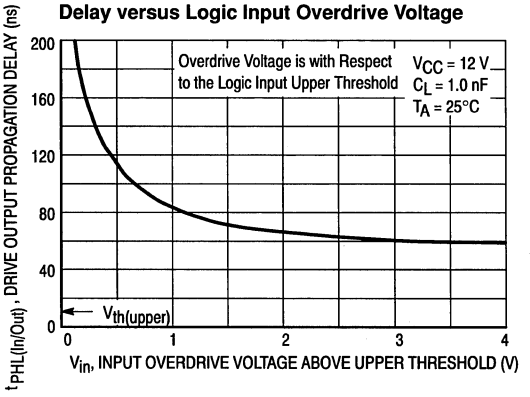


Figure 7. Propagation Delay

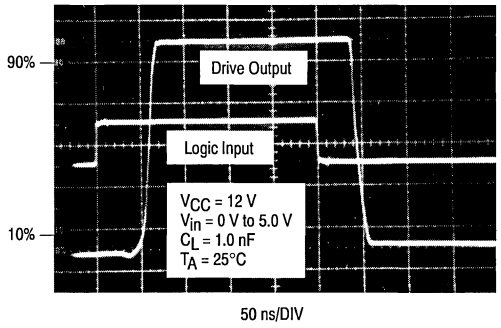


Figure 8. Drive Output Clamp Voltage versus Clamp Current

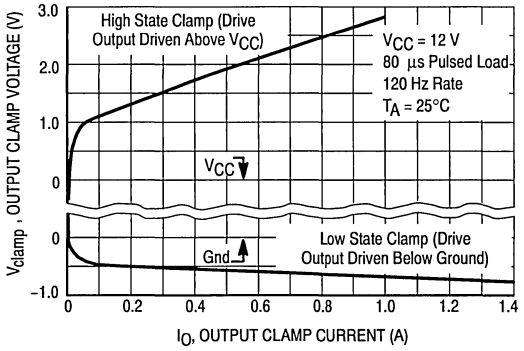


Figure 9. Drive Output Saturation Voltage versus Load Current

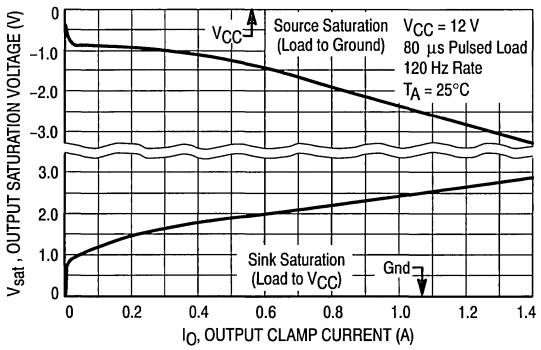


Figure 10. Drive Output Saturation Voltage versus Temperature

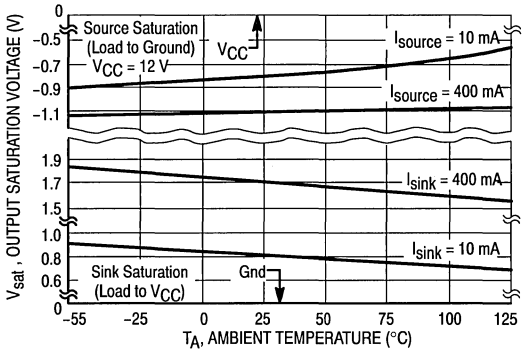


Figure 11. Drive Output Rise Time

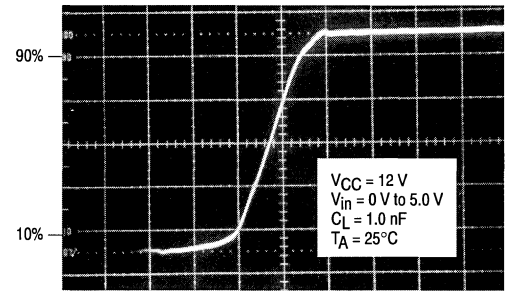


Figure 12. Drive Output Fall Time

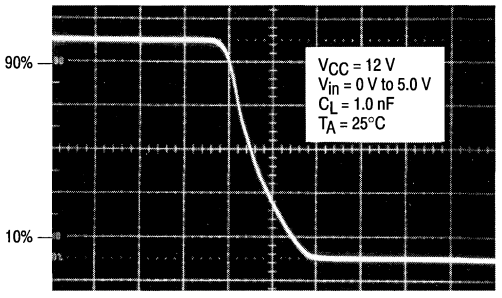


Figure 13. Drive Output Rise and Fall Time versus Load Capacitance

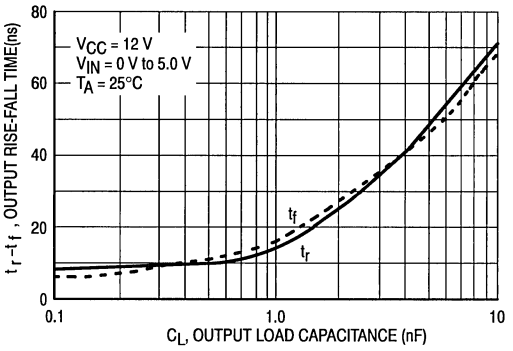


Figure 14. Supply Current versus Drive Output Load Capacitance

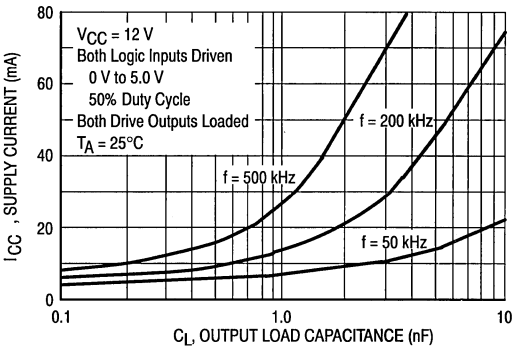


Figure 15. Supply Current versus Input Frequency

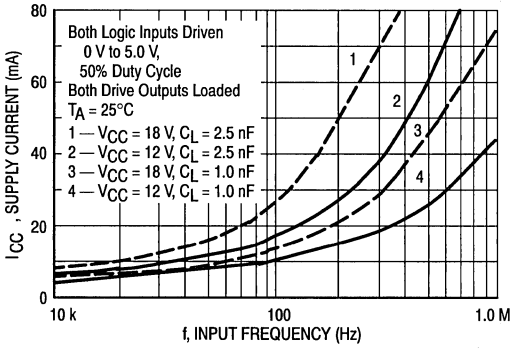
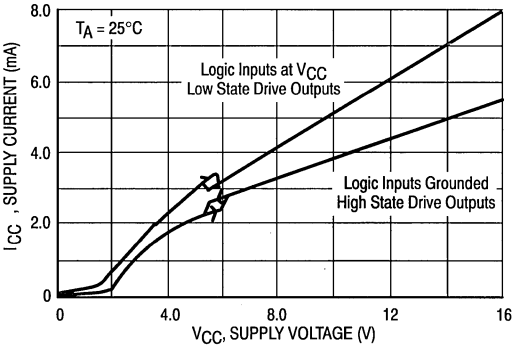


Figure 16. Supply Current versus Supply Voltage



APPLICATIONS INFORMATION

Description

The MC34152 is a dual noninverting high speed driver specifically designed to interface low current digital circuitry with power MOSFETs. This device is constructed with Schottky clamped Bipolar Analog technology which offers a high degree of performance and ruggedness in hostile industrial environments.

Input Stage

The Logic Inputs have 170 mV of hysteresis with the input threshold centered at 1.67 V. The input thresholds are insensitive to V_{CC} making this device directly compatible with CMOS and LSTTL logic families over its entire operating voltage range. Input hysteresis provides fast output switching that is independent of the input signal transition time, preventing output oscillations as the input thresholds are crossed. The inputs are designed to accept a signal amplitude ranging from ground to V_{CC}. This allows the output of one channel to directly drive the input of a second channel for master-slave operation. Each input has a 30 kΩ pull-down resistor so that an unconnected open input will cause the associated Drive Output to be in a known low state.

Output Stage

Each totem pole Drive Output is capable of sourcing and sinking up to 1.5 A with a typical 'on' resistance of 2.4 Ω at 1.0 A. The low 'on' resistance allows high output currents to be attained at a lower V_{CC} than with comparative CMOS drivers. Each output has a 100 kΩ pull-down resistor to keep the MOSFET gate low when V_{CC} is less than 1.4 V. No over current or thermal protection has been designed into the device, so output shorting to V_{CC} or ground must be avoided.

Parasitic inductance in series with the load will cause the driver outputs to ring above V_{CC} during the turn-on transition, and below ground during the turn-off transition. With CMOS drivers, this mode of operation can cause a destructive output latch-up condition. The MC34152 is immune to output latch-up. The Drive Outputs contain an internal diode to V_{CC} for clamping positive voltage transients. When operating with V_{CC} at 18 V, proper power supply bypassing must be observed to prevent the output ringing from exceeding the maximum 20 V device rating. Negative output transients are clamped by the internal NPN pull-up transistor. Since full supply voltage is applied across the NPN pull-up during the negative output transient, power dissipation at high

frequencies can become excessive. Figures 19, 20, and 21 show a method of using external Schottky diode clamps to reduce driver power dissipation.

Undervoltage Lockout

An undervoltage lockout with hysteresis prevents erratic system operation at low supply voltages. The UVLO forces the Drive Outputs into a low state as V_{CC} rises from 1.4 V to the 5.8 V upper threshold. The lower UVLO threshold is 5.3 V, yielding about 500 mV of hysteresis.

Power Dissipation

Circuit performance and long term reliability are enhanced with reduced die temperature. Die temperature increase is directly related to the power that the integrated circuit must dissipate and the total thermal resistance from the junction to ambient. The formula for calculating the junction temperature with the package in free air is:

$$T_J = T_A + P_D (R_{\theta JA})$$

where: T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
$R_{\theta JA}$ = Thermal Resistance Junction to Ambient

There are three basic components that make up total power to be dissipated when driving a capacitive load with respect to ground. They are:

$$P_D = P_Q + P_C + P_T$$

where: P_Q = Quiescent Power Dissipation
P_C = Capacitive Load Power Dissipation
P_T = Transition Power Dissipation

The quiescent power supply current depends on the supply voltage and duty cycle as shown in Figure 16. The device's quiescent power dissipation is:

$$P_Q = V_{CC} (I_{CCL} [1\text{-}D] + I_{CCH} [D])$$

where: I_{CCL} = Supply Current with Low State Drive Outputs
I_{CCH} = Supply Current with High State Drive Outputs
D = Output Duty Cycle

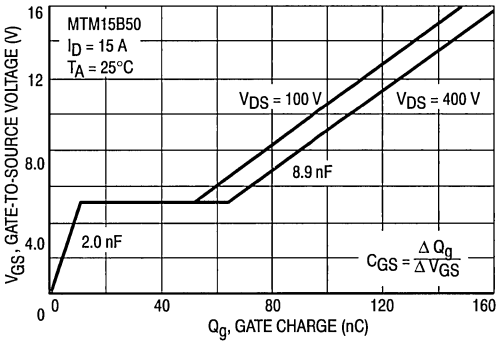
The capacitive load power dissipation is directly related to the load capacitance value, frequency, and Drive Output voltage swing. The capacitive load power dissipation per driver is:

$$P_C = V_{CC} (V_{OH} - V_{OL}) C_L f$$

where: V_{OH} = High State Drive Output Voltage
V_{OL} = Low State Drive Output Voltage
C_L = Load Capacitance
f = Frequency

When driving a MOSFET, the calculation of capacitive load power P_C is somewhat complicated by the changing gate to source capacitance C_{GS} as the device switches. To aid in this calculation, power MOSFET manufacturers provide gate charge information on their data sheets. Figure 17 shows a curve of gate voltage versus gate charge for the Motorola MTM15N50. Note that there are three distinct slopes to the curve representing different input capacitance values. To completely switch the MOSFET 'on,' the gate must be brought to 10 V with respect to the source. The graph shows that a gate charge Q_g of 110 nC is required when operating the MOSFET with a drain to source voltage V_{DS} of 400 V.

Figure 17. Gate-to-Source Voltage versus Gate charge



The capacitive load power dissipation is directly related to the required gate charge, and operating frequency. The capacitive load power dissipation per driver is:

$$P_{C(MOSFET)} = V_{CC} Q_g f$$

The flat region from 10 nC to 55 nC is caused by the drain-to-gate Miller capacitance, occurring while the MOSFET is in the linear region dissipating substantial amounts of power. The high output current capability of the MC34152 is able to quickly deliver the required gate charge for fast power efficient MOSFET switching. By operating the MC34152 at a higher V_{CC}, additional charge can be provided to bring the gate above 10 V. This will reduce the 'on' resistance of the MOSFET at the expense of higher driver dissipation at a given operating frequency.

The transition power dissipation is due to extremely short simultaneous conduction of internal circuit nodes when the Drive Outputs change state. The transition power dissipation per driver is approximately:

$$P_T \approx V_{CC} (1.08\ V_{CC}\ C_L\ f - 8 \times 10^{-4})$$

P_T must be greater than zero.

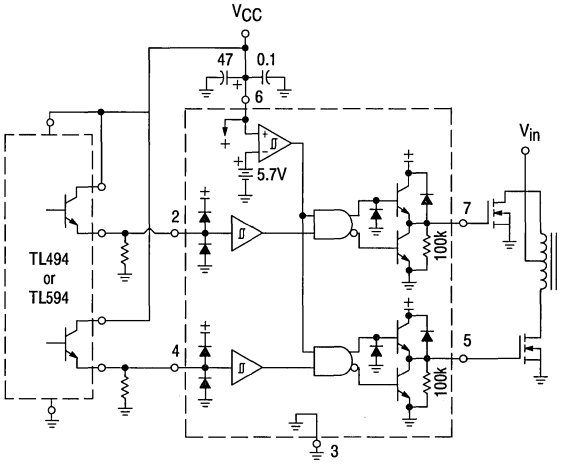
Switching time characterization of the MC34152 is performed with fixed capacitive loads. Figure 13 shows that for small capacitance loads, the switching speed is limited by transistor turn-on/off time and the slew rate of the internal nodes. For large capacitance loads, the switching speed is limited by the maximum output current capability of the integrated circuit.

LAYOUT CONSIDERATIONS

High frequency printed circuit layout techniques are imperative to prevent excessive output ringing and overshoot. **Do not attempt to construct the driver circuit on wire-wrap or plug-in prototype boards.** When driving large capacitive loads, the printed circuit board must contain a low inductance ground plane to minimize the voltage spikes induced by the high ground ripple currents. All high current loops should be kept as short as possible using heavy copper runs to provide a low impedance high frequency path. For optimum drive performance, it is recommended that the initial circuit design contains dual power supply bypass capacitors connected with short leads as close to the V_{CC} pin and ground as the layout will permit. Suggested capacitors are a low inductance 0.1 μF ceramic in parallel with a 4.7 μF tantalum. Additional bypass capacitors may be required depending upon Drive Output loading and circuit layout.

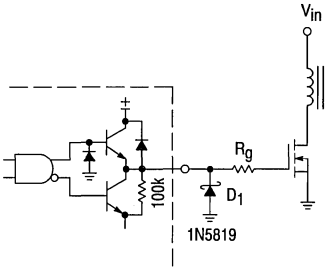
Proper printed circuit board layout is extremely critical and cannot be over emphasized.

Figure 18. Enhanced System Performance with Common Switching Regulators



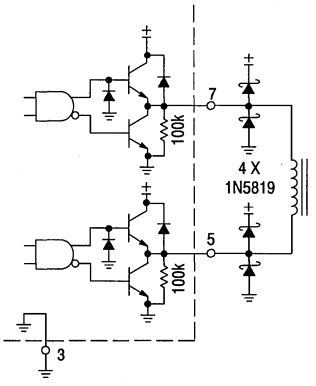
The MC34152 greatly enhances the drive capabilities of common switching regulators and CMOS/TTL logic devices.

Figure 19. MOSFET Parasitic Oscillations



Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D_1 can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 20. Direct Transformer Drive



Output Schottky diodes are recommended when driving inductive loads at high frequencies. The diodes reduce the driver's power dissipation by preventing the output pins from being driven above V_{CC} and below ground.

Figure 21. Isolated MOSFET Drive

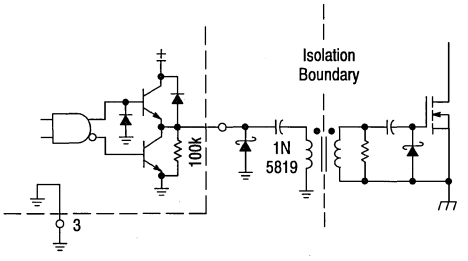
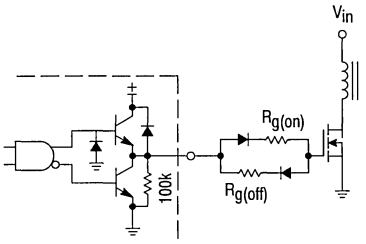
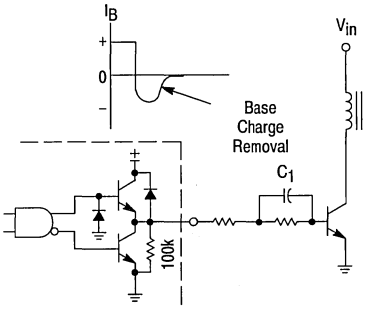


Figure 22. Controlled MOSFET Drive



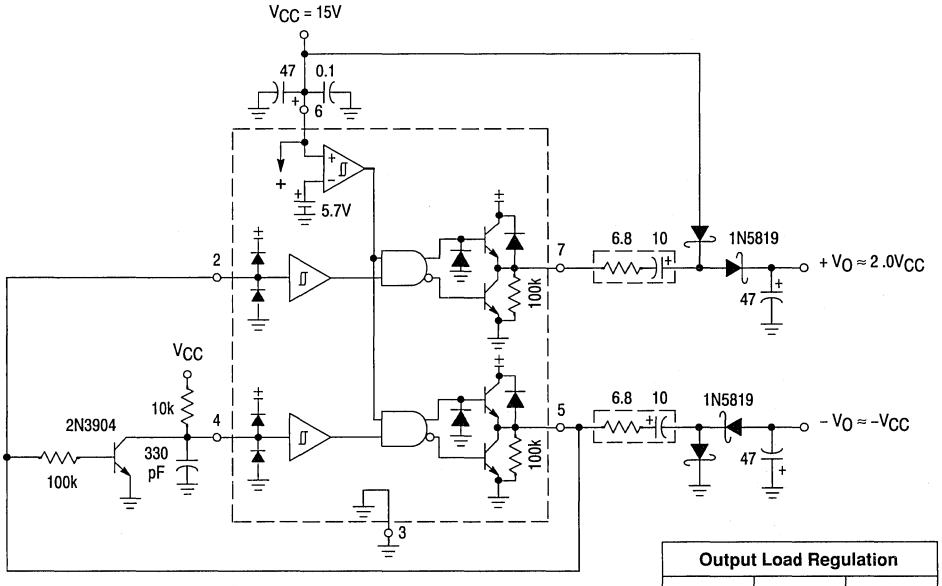
In noise sensitive applications, both conducted and radiated EMI can be reduced significantly by controlling the MOSFET's turn-on and turn-off times.

Figure 23. Bipolar Transistor Drive



The totem-pole outputs can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1.

Figure 24. Dual Charge Pump Converter



The capacitor's equivalent series resistance limits the Drive Output Current to 1.5 A. An additional series resistor may be required when using tantalum or other low ESR capacitors.

Output Load Regulation		
I_O (mA)	$+V_O$ (V)	$-V_O$ (V)
0	27.7	–13.3
1.0	27.4	–12.9
10	26.4	–11.9
20	25.5	–11.2
30	24.6	–10.5
50	22.6	–9.4

MC34160
MC33160

3

Advance Information

Microprocessor Voltage Regulator and Supervisory Circuit

MICROPROCESSOR VOLTAGE REGULATOR/ SUPERVISORY CIRCUIT

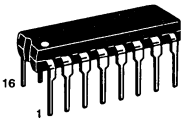
SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC34160 Series is a voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications, offering the designer a cost effective solution with minimal external components. These integrated circuits feature a 5.0 V/100 mA regulator with short circuit current limiting, pinned out 2.6 V bandgap reference, low voltage reset comparator, power warning comparator with programmable hysteresis, and an uncommitted comparator ideally suited for microprocessor line synchronization.

Additional features include a chip disable input for low standby current, and internal thermal shutdown for over temperature protection.

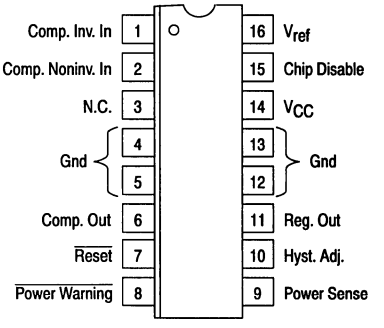
These devices are contained in a 16 pin dual-in-line heat tab plastic package for improved thermal conduction.

- 5.0 V Regulator Output Current in Excess of 100 mA
- Internal Short Circuit Current Limiting
- Pinned Out 2.6 V Reference
- Low Voltage Reset Comparator
- Power Warning Comparator with Programmable Hysteresis
- Uncommitted Comparator
- Low Standby Current
- Internal Thermal Shutdown Protection
- Heat Tab Power Package



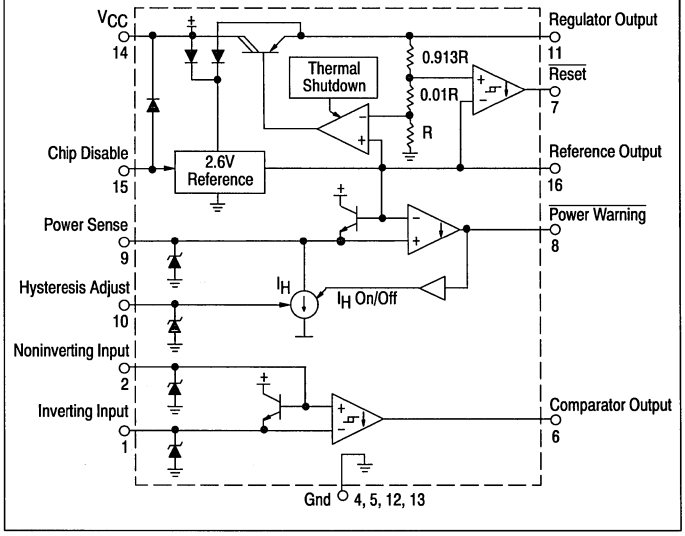
P SUFFIX
PLASTIC PACKAGE
CASE 648C

PIN CONNECTIONS



(Top View)

Representative Block Diagram



ORDERING INFORMATION

Device	Temperature Range	Package
MC34160P	0° to +70°C	Plastic DIP
MC33160P	–40° to +85°C	Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Chip Disable Input Voltage (Pin 15, Note 1)	V_{CD}	−0.3 to V_{CC}	V
Comparator Input Current (Pin 1, 2, 9)	I_{in}	−2.0 to +2.0	mA
Comparator Output Voltage (Pin 6, 7, 8)	V_O	40	V
Comparator Output Sink Current (Pin 6, 7, 8)	I_{Sink}	10	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air Thermal Resistance Junction to Case (Pin 4, 5, 12, 13)	 P_D $R\theta_{JA}$ $R\theta_{JC}$	 1000 80 15	 mW °C/W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34160 MC33160	T_A	 0 to +70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERICISTICS (V_{CC} = 30 V, I_O = 10 mA, I_{ref} = 100 µA) For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REGULATOR SECTION					
Total Output Variation (V_{CC} = 7.0 V to 40 V, I_O = 1.0 mA to 100 mA, T_A = T_{low} to T_{high}	V_O	4.75	5.0	5.25	V
Line Regulation (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Reg_{line}	—	5.0	40	mV
Load Regulation (I_O = 1.0 V to 100 mA, T_A = 25°C)	Reg_{load}	—	20	50	mV
Ripple Rejection (V_{CC} = 25 V to 35 V, I_O = 40 mA, f = 120 Hz, T_A = 25°C)	RR	50	6.5	—	dB
REFERENCE SECTION					
Total Output Variation (V_{CC} = 7.0 to 40 V, I_O = 0.1 mA to 2.0 mA, T_A = T_{low} to T_{high}	V_{ref}	2.47	2.6	2.73	V
Line Regulation (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	Reg_{line}	—	2.0	20	mV
Load Regulation (I_O = 0.1 mA to 2.0 mA, T_A = 25°C)	Reg_{load}	—	4.0	30	mV
RESET COMPARATOR					
Threshold Voltage High State Output (Pin 11 Increasing) Low State Output (Pin 11 Decreasing) Hysteresis	 V_{IH} V_{IL} V_H	 — 4.55 0.02	 (V_O−0.11) (V_O−0.18 0.07	 (V_O−0.05) — —	V
Output Sink Saturation (V_{CC} = 4.5 V, I_{Sink} = 2.0 mA)	V_{OL}	—	—	0.4	V
Output Off-State Leakage (V_{OH} = 40 V)	I_{OH}	—	—	4.0	µA

NOTES: 1. The maximum voltage range is −0.3 V to V_{CC} or +35 V, whichever is less.
2. T_{low} = 0°C for MC34160, −40°C for MC33160; T_{high} = 70°C for MC34160, 85°C for MC33160
2. Low duty cycle pulse testing techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERICISTICS (continued) (V_{CC} = 30 V, I_O = 10 mA, I_{ref} = 100 μA) For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER WARNING COMPARATOR					
Input Offset Voltage	V_{IO}	—	1.2	10	mV
Input Bias Current ($V_{Pin\ 9}$ = 3.0 V)	I_{IB}	—	—	0.5	μA
Input Hysteresis Current ($V_{Pin\ 9} = V_{ref} - 100$ mV) $R_{Pin\ 10}$ = 24 k $R_{Pin\ 10} = \infty$	I_H	 40 4.5	 50 7.5	 60 11	μA
Output Sink Saturation (I_{Sink} = 2.0 mA)	V_{OL}	—	0.13	0.4	V
Output Off-State Leakage (V_{OH} = 40 V)	I_{OH}	—	—	4.0	μA
UNCOMMITTED COMPARATOR					
Input Offset Voltage (Output Transition Low to High)	V_{IO}	—	—	20	mV
Input Hysteresis Voltage (Output Transition High to Low)	I_H	140	200	260	mV
Input Bias Current ($V_{Pin\ 1, 2}$ = 2.6 V)	I_{IB}	—	—	−1.0	μA
Input Common Mode Voltage Range	V_{ICR}	0.6 to 5.0	—	—	V
Output Sink Saturation (I_{Sink} = 2.0 mA)	V_{OL}	—	0.13	0.4	V
Output Off-State Leakage (V_{OH} = 40 V)	I_{OH}	—	—	4.0	μA
TOTAL DEVICE					
Chip Disable Threshold Voltage (Pin 15) High State (Chip Disabled) Low State (Chip Enabled)	 V_{IH} V_{IL}	 2.5 —	 — —	 — 0.8	V
Chip Disable Input Current (Pin 15) High State (V_{in} = 2.5 V) Low State (V_{in} = 0.8 V)	 I_{IH} I_{IL}	 — —	 — —	 100 30	μA
Chip Disable Input Resistance (Pin 15)	R_{in}	50	100	—	kΩ
Operating Voltage Range V_O (Pin 11) Regulated V_{ref} (Pin 16) Regulated	V_{CC}	 7.0 to 40 5.0 to 40	 — —	 — —	V
Power Supply Current Standby (Chip Disable High State) Operating (Chip Disable Low State)	I_{CC}	 — —	 0.18 1.5	 0.35 3.0	mA

Figure 1. Regulator Output Voltage Change versus Source Current

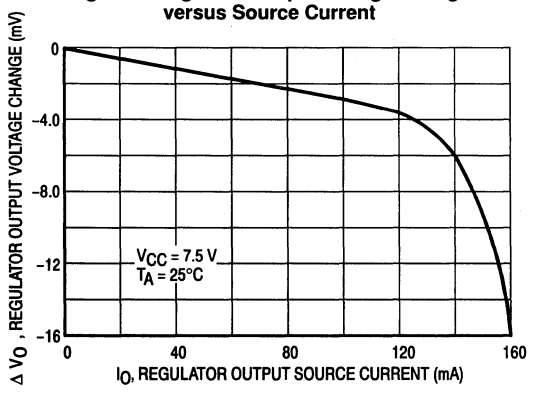


Figure 2. Reference and Regulator Output versus Supply Voltage

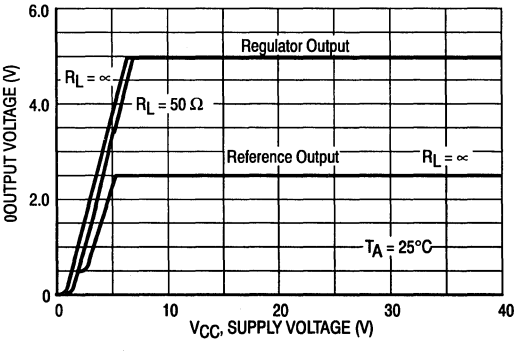


Figure 3. Reference Output Voltage Change versus Source Current

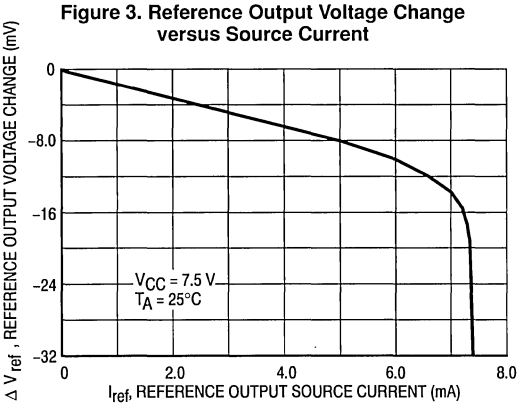


Figure 4. Power Warning Hysteresis Current versus Programming Resistor

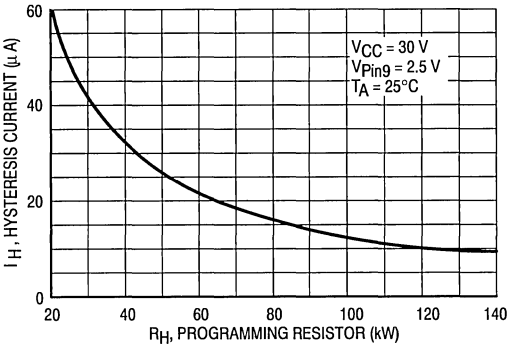


Figure 5. Power Warning Comparator Delay versus Temperature

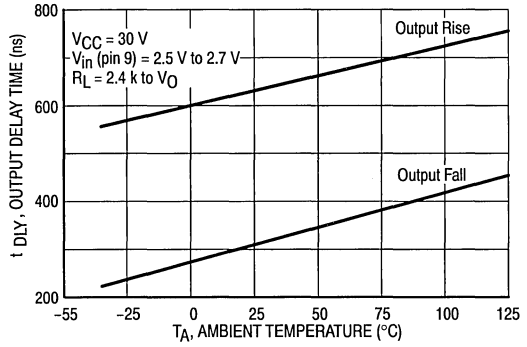


Figure 6. Uncommitted Comparator Delay versus Temperature

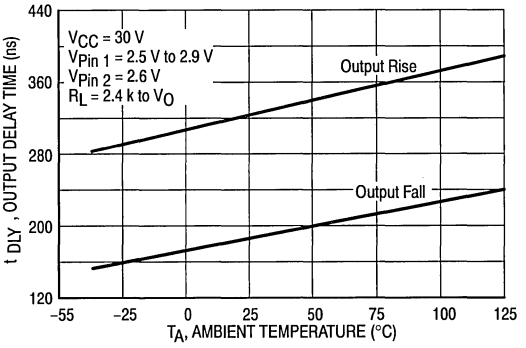


Figure 7. Comparator Output Saturation versus Sink Current

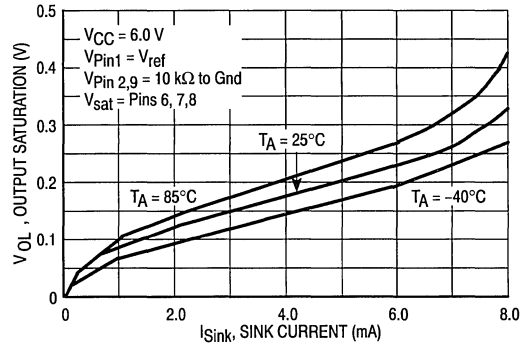
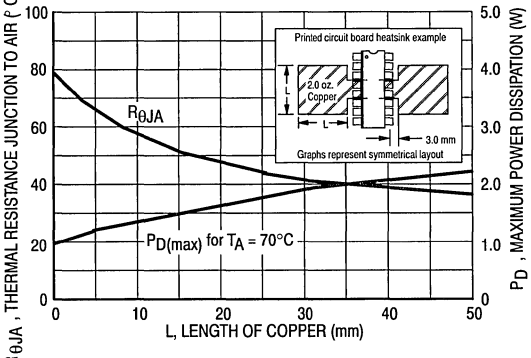


Figure 8. Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	Comparator Inverting Input	This is the Uncommitted Comparator Inverting input. It is typically connected to a resistor divider to monitor a voltage.
2	Comparator Noninverting Input	This is the Uncommitted Comparator Noninverting input. It is typically connected to a reference voltage.
3	N.C.	No connection. This pin is not internally connected.
4,5, 12,13	Gnd	These pins are the control circuit grounds and are connected to the source and load ground returns. They are part of the IC lead frame and can be used for heatsinking.
6	Comparator Output	This is the Uncommitted Comparator output. It is an open collector sink-only output requiring a pull-up resistor.
7	$\overline{\text{Reset}}$	This is the $\overline{\text{Reset}}$ Comparator output. It is an open collector sink-only output requiring a pull-up resistor.
8	$\overline{\text{Power Warning}}$	This is the $\overline{\text{Power Warning}}$ Comparator output. It is an open collector sink-only output requiring a pull-up resistor.
9	Power Sense	This is the $\overline{\text{Power Warning}}$ Comparator noninverting input. It is typically connected to a resistor divider to monitor the input power source voltage.
10	Hysteresis Adjust	The $\overline{\text{Power Warning}}$ Comparator hysteresis is programmed by a resistor connected from this pin to ground.
11	Regulator Output	This is the 5.0 V Regulator output.
14	V_{CC}	This pin is the positive supply input of the control IC.
15	Chip Disable	This input is used to switch the IC into a standby mode turning off all outputs.
16	V_{ref}	This is the 2.6 V Reference output. It is intended to be used in conjunction with the $\overline{\text{Power Warning}}$ and Uncommitted comparators.

OPERATING DESCRIPTION

The MC34160 series is a monolithic voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications, offering the designer a cost effective solution with minimal external components. These devices are specified for operation over an input voltage of 7.0 V to 40 V, and with a junction temperature of –40° to +150°C. A typical microprocessor application is shown in Figure 9.

Regulator

The 5.0 V regulator is designed to source in excess of 100 mA output current and is short circuit protected. The output has a guaranteed tolerance of ±5.0% over line, load, and temperature. Internal thermal shutdown circuitry is included to limit the maximum junction temperature to a safe level. When activated, typically at 170°C, the regulator output turns off.

In specific situations a combination of input and output bypass capacitors may be required for regulator stability. If the regulator is located an appreciable distance (≥4″) from the supply filter, an input bypass capacitor (C_{in}) of 0.33 μF or greater is suggested. Output capacitance values of less than 5.0 nF may cause regulator instability at light load (≤ 1.0 mA) and cold temperature. An output bypass capacitor of 0.1 μF or greater is recommended to ensure stability under all load conditions. The capacitors selected must provide good high frequency characteristics.

Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator does not have external sense inputs.

Reference

The 2.6 V bandgap reference is short circuit protected and has a guaranteed output tolerance of ±5.0% over line, load, and temperature. It is intended to be used in conjunction with the $\overline{\text{Power Warning}}$ and Uncommitted comparator. The reference can source in excess of 2.0 mA and sink a maximum of 10 μA. For additional current sinking capability, an external load resistor to ground must be used.

Reference biasing is internally derived from either V_{CC} or V_O, allowing proper operation if either drops below nominal.

Chip Disable

This input is used to switch the IC into a standby mode. When activated, internal biasing for the entire die is removed causing all outputs to turn off. This reduces the power supply current (I_{CC}) to less than 0.3 mA.

Comparators

Three separate comparators are incorporated for voltage monitoring. Their outputs can provide diagnostic information to the microprocessor, preventing system malfunctions.

The $\overline{\text{Reset}}$ Comparator Inverting Input is internally connected to the 2.6 V reference while the Noninverting Input

monitors V_O. The $\overline{\text{Reset}}$ Output is active low when V_O falls approximately 180 mV below its regulated voltage. To prevent erratic operation when crossing the comparator threshold, 70 mV of hysteresis is provided.

The $\overline{\text{Power Warning}}$ Comparator is typically used to detect an impending loss of system power. The Inverting Input is internally connected to the reference, fixing the threshold at 2.6 V. The input power source V_{in} is monitored by the Noninverting Input through the R_1/R_2 divider (Figure 9). This input features an adjustable 10 μA to 50 μA current sink I_H that is programmed by the value selected for resistor R_H. A default current of 6.5 μA is provided if R_H is omitted. When the comparator input falls below 2.6 V, the current sink is activated. This produces hysteresis if V_{in} is monitored through a series resistor (R_1). The comparator thresholds are defined as follows:

$$V_{th(lower)} = V_{ref}\left(1 + \frac{R_1}{R_2}\right) - I_{IB}\,R_1$$

$$V_{th(upper)} = V_{ref}\left(1 + \frac{R_1}{R_2}\right) + I_H\,R_1$$

The nominal hysteresis current I_H equals 1.2 V/R_H (Figure 4).

The Uncommitted Comparator can be used to synchronize the microprocessor with the ac line signal for timing functions, or for synchronous load switching. It can also be connected as a line loss detector as shown in Figure 10. The comparator contains 200 mV of hysteresis preventing erractic output behavior when crossing the input threshold.

The $\overline{\text{Power Warning}}$ and Uncommitted Comparators each have a transistor base-emitter connected across their inputs. The base input normally connects to a voltage reference while the emitter input connects to the voltage to be monitored. The transistor limits the negative excursion on the emitter input to −0.7 V below the base input by supply current from V_{CC}. This clamp current will prevent forward biasing the IC substrate. Zener diodes are connected to the comparator inputs to enhance the ICs electrostatic discharge capability. Resistors R_1 and R_{in} must limit the input current to a maximum of ±2.0 mA.

Each comparator output consists of an open collector NPN transistor capable of sinking 2.0 mA with a saturation voltage less than 0.4 V, and standing off 40 V with minimal leakage. Internal bias for the $\overline{\text{Reset}}$ and $\overline{\text{Power Warning}}$ Comparators is derived from either V_{CC} or the regulator output to ensure functionality when either is below nominal.

Heat Tab Package

The MC34160 is contained in a 16 lead plastic dual-in-line package in which the die is mounted on a special Heat Tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the surrounding air. The pictorial in Figure 8 shows a simple but effective method of utilizing the printed circuit board medium as a heat dissipator by soldering these tabs to an adequate area of copper foil. This permits the use of standard board layout and mounting practices while having the ability to more than halve the junction to air thermal resistance. The example and graph are for a symmetrical layout on a single sided board with one ounce per square foot copper.

Figure 9. Typical Microprocessor Application

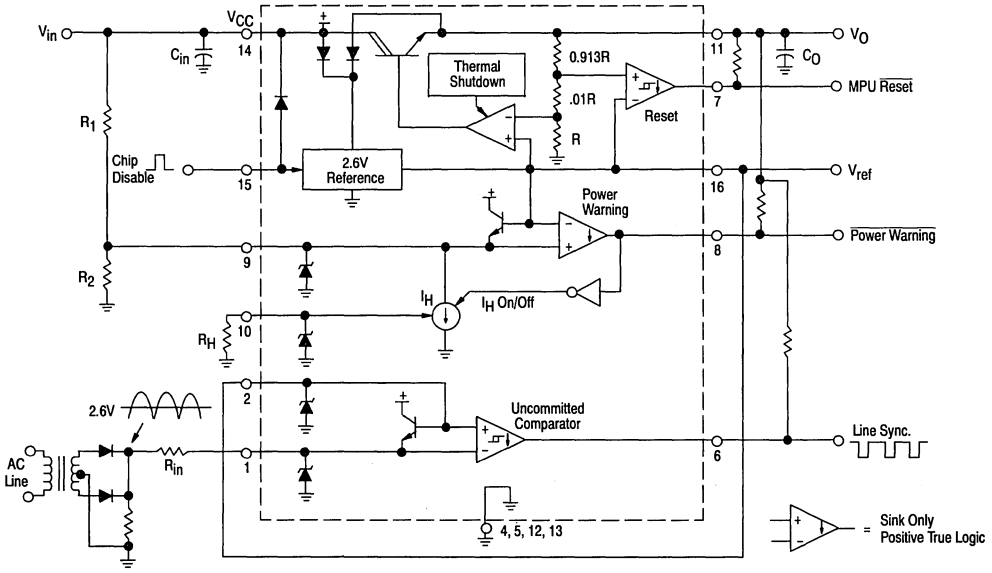


Figure 10. Line Loss Detector Application

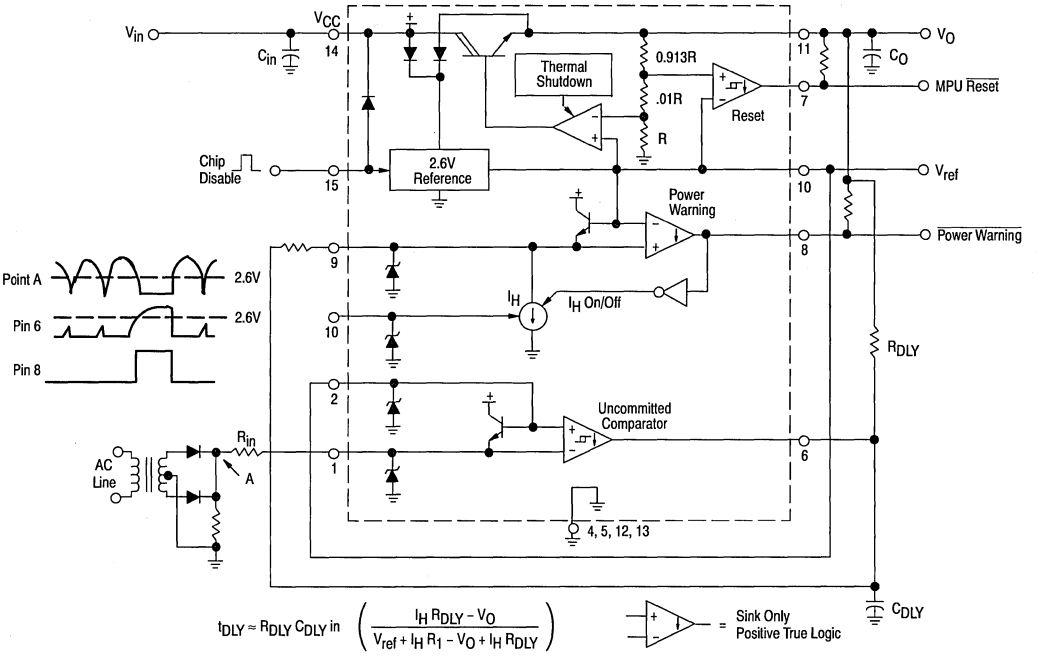
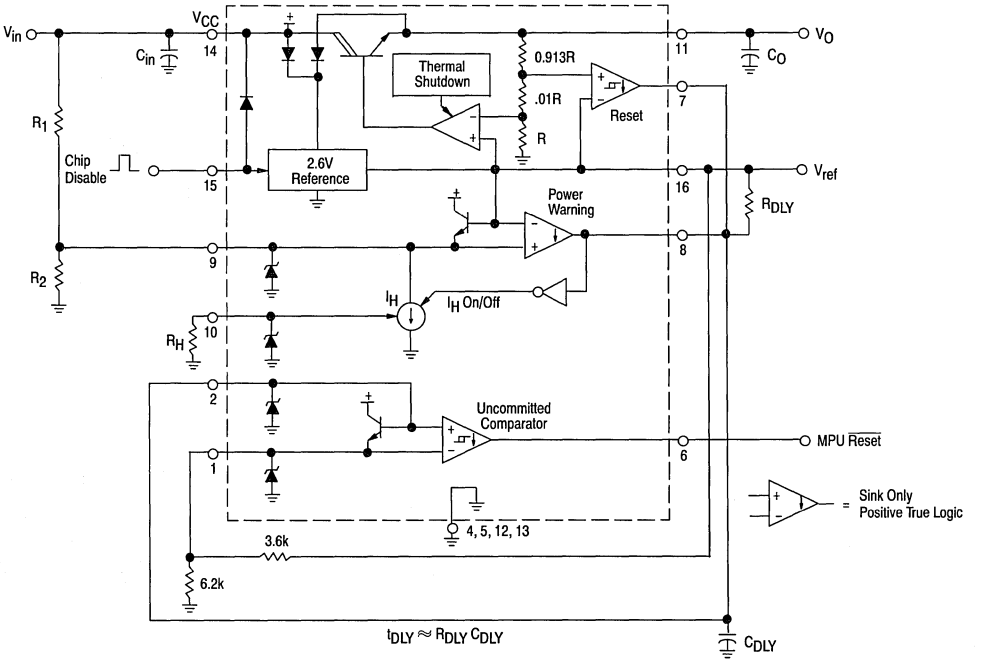


Figure 11. Time Delayed Microprocessor Reset



MC34161
MC33161

Advance Information

Universal Voltage Monitor

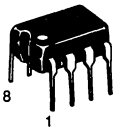
UNIVERSAL VOLTAGE MONITOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC34161, MC33161 series are universal voltage monitors intended for use in a wide variety of voltage sensing applications. These devices offer the circuit designer an economical solution for positive and negative voltage detection. The circuit consists of two comparator channels each with hysteresis, a unique Mode Select Input for channel programming, a pinned out 2.54 V reference, and two open collector outputs capable of sinking in excess of 10 mA. Each comparator channel can be configured as either inverting or noninverting by the Mode Select Input. This allows over, under, and window detection of positive and negative voltages. The minimum supply voltage needed for these devices to be fully functional is 2.0 V for positive voltage sensing and 4.0 V for negative voltage sensing.

Applications include direct monitoring of positive and negative voltages used in appliance, automotive, consumer, and industrial equipment.

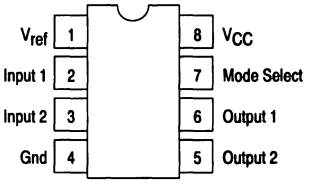
- Unique Mode Slect Input Allows Channel Programming
- Over, Under, and Window Voltage Detection
- Positive and Negative Voltage Detection
- Fully Functional at 2.0 V for Positve Voltage Sensing and 4.0 V for Negative Voltage Sensing
- Pinned Out 2.54 V Reference with Current Limit Protection
- Low Standby Current
- Open Collector Outputs for Enhanced Device Flexibility



P SUFFIX
PLASTIC PACKAGE
CASE 626

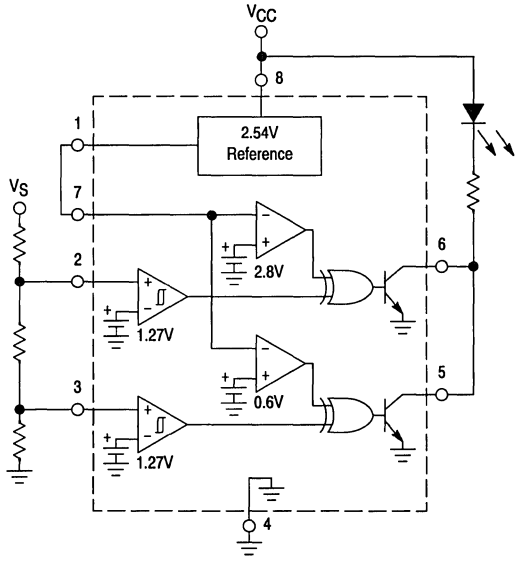
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



(TOP VIEW)

Simplified Block Diagram
(Positive Voltage Window Detector Application)



ORDERING INFORMATION

Device	Temperature Range	Package
MC34161D	0° to +70°C	SO-8
MC34161P		Plastic DIP
MC33161D	–40° to +85°C	SO-8
MC33161P		Plastic DIP

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	40	V
Comparator Input Voltage Range	V_{in}	– 1.0 to +40	V
Comparator Output Sink Current (Pins 5 and 6, Note 1)	I_{Sink}	20	mA
Comparator Output Voltage	V_{out}	40	V
Power Dissipation and Thermal Characteristics (Note 1) P Suffix, Plastic Package Case 626 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction to Air D Suffix, Plastic Package SO-8 Case 751 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction to Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 800 100 450 178	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34161 MC33161	T_A	0 to +70 – 40 to +85	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
COMPARATOR INPUTS					
Threshold Voltage, V_{in} Increasing (T_A = 25°C) (T_A = T_{min} to T_{max})	V_{th}	1.245 1.235	1.27 —	1.295 1.295	V
Threshold Voltage Variation (V_{CC} = 2.0 V to 40 V)	ΔV_{th}	—	7.0	15	mV
Threshold Hysteresis, V_{in} Decreasing	V_H	15	25	35	mV
Threshold Difference $\lvert V_{th1} - V_{th2} \rvert$	V_D	—	1.0	15	mV
Reference to Threshold Difference ($V_{ref} - V_{in1}$), ($V_{ref} - V_{in2}$)	V_{RTD}	1.20	1.27	1.32	V
Input Bias Current (V_{in} = 1.0 V) (V_{in} = 1.5 V)	I_{IB}	— —	40 85	200 400	nA
MODE SELECT INPUT					
Mode Select Threshold Voltage (Figure 5) Channel 1 Channel 2	$V_{th(CH\ 1)}$ $V_{th(CH\ 2)}$	V_{ref}+0.15 0.3	V_{ref}+0.23 0.63	V_{ref}+0.30 0.9	V
COMPARATOR OUTPUTS					
Output Sink Saturation Voltage (I_{Sink} = 2.0 mA) (I_{Sink} = 10 mA) (I_{Sink} = 0.25 mA, V_{CC} = 1.0 V)	V_{OL}	— — —	0.05 0.22 0.02	0.3 0.6 0.2	V
Off-State Leakage Current (V_{OH} = 40 V)	I_{OH}	—	0	1.0	µA
REFERENCE OUTPUT					
Output Voltage (I_O = 0 mA, T_A = 25°C)	V_{ref}	2.48	2.54	2.60	V
Load Regulation (I_O = 0 mA to 2.0 mA)	Reg_{load}	—	0.6	15	mV
Line Regulation (V_{CC} = 4.0 V to 40 V)	Reg_{line}	—	5.0	15	mV
Total Output Variation over Line, Load, and Temperature	ΔV_{ref}	2.45	—	2.60	V
Short Circuit Current	I_{SC}	—	8.5	30	mA
TOTAL DEVICE					
Power Supply Current (V_{Mode}, V_{in1}, V_{in2} = Gnd) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{CC}	— —	450 560	700 900	µA
Operating Voltage Range (Positive Sensing) (Negative Sensing)	V_{CC}	2.0 4.0	— —	40 40	V

NOTES:
1. Maximum package power dissipation must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34161, –40°C for MC33161; T_{high} = 70°C for MC34161, 85°C for MC33161

Figure 1. Comparator Input Threshold Voltage

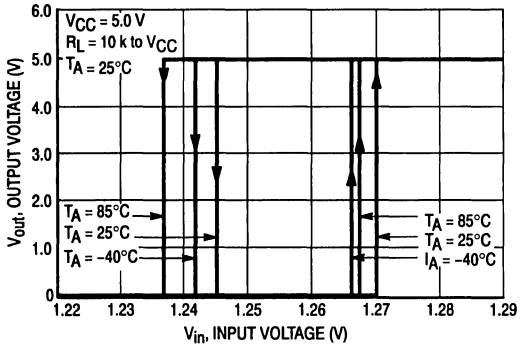


Figure 2. Comparator Input Bias Current Versus Input Voltage

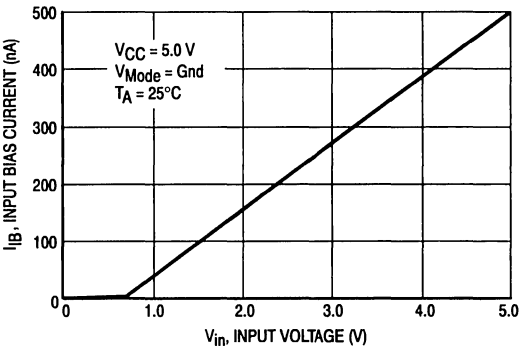


Figure 3. Output Propagation Delay Time versus Percent Overdrive

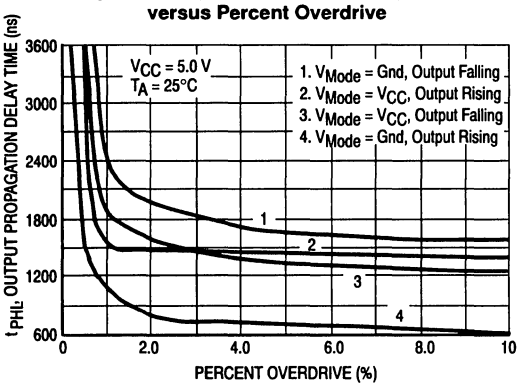


Figure 4. Output Voltage versus Supply Voltage

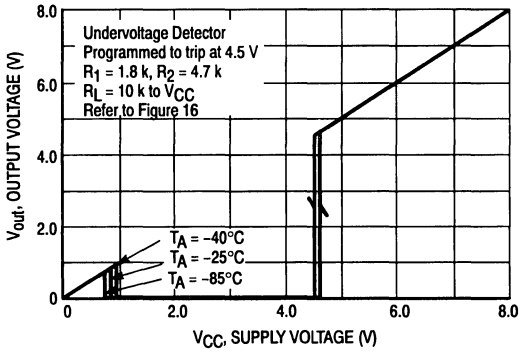


Figure 5. Mode Select Thresholds

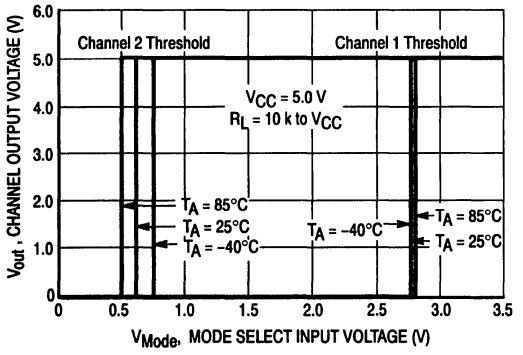


Figure 6. Mode Select Input Current versus Input Voltage

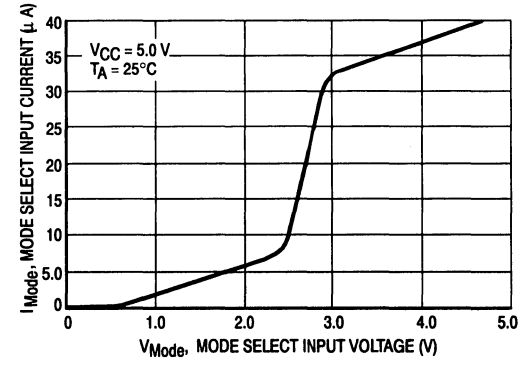


Figure 7. Reference Voltage versus Supply Voltage

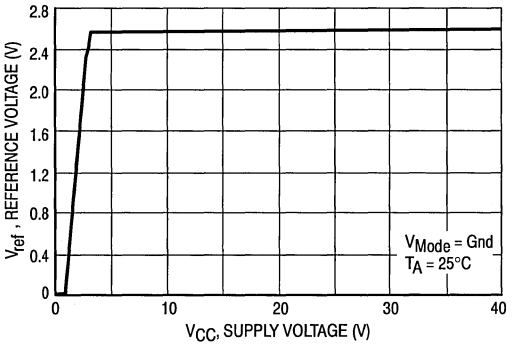


Figure 8. Reference Voltage versus Ambient Temperature

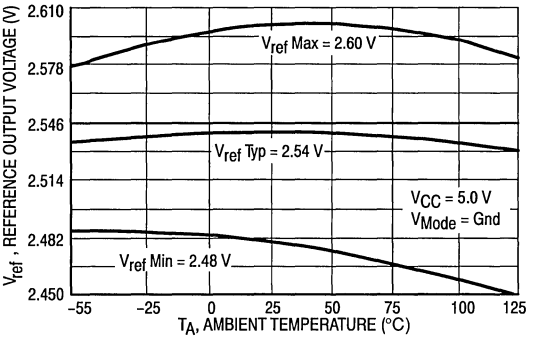


Figure 9. Reference Voltage Change versus Source Current

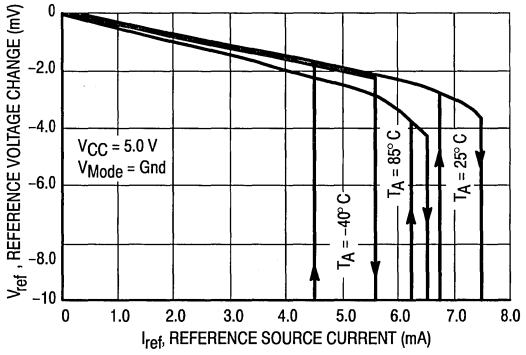


Figure 10. Output Saturation Voltage versus Output Sink Current

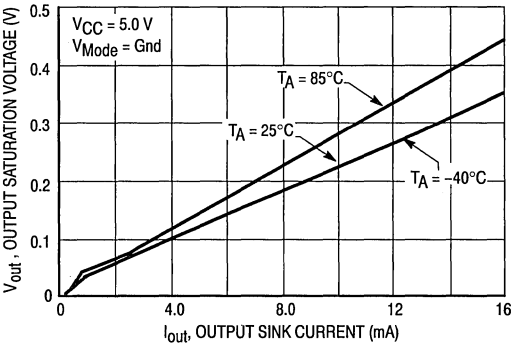


Figure 11. Supply Current versus Supply Voltage

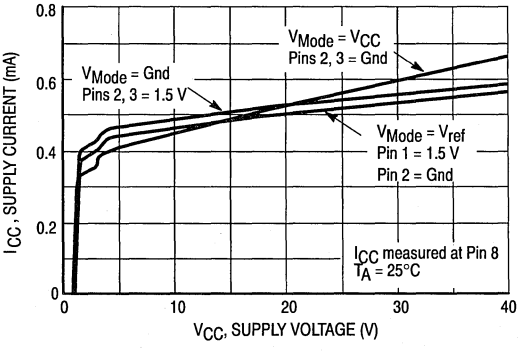


Figure 12. Supply Current versus Output Sink Current

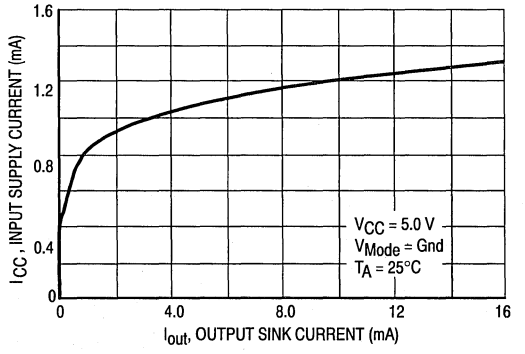


Figure 13. MC34161 Representative Block Diagram

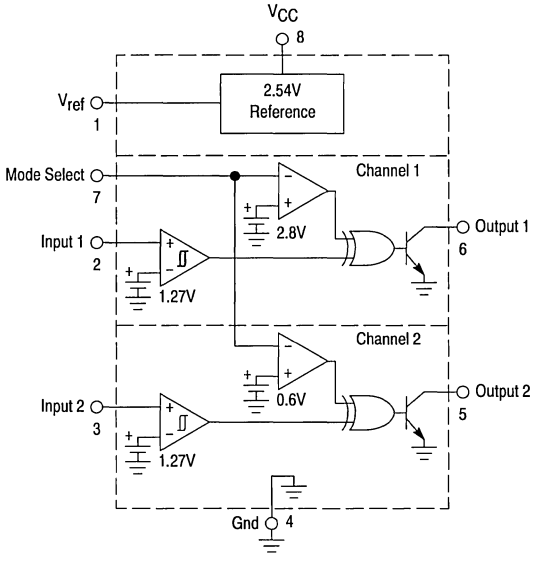


Figure 14. Truth Table

Mode Select Pin 7	Input 1 Pin 2	Output 1 Pin 6	Input 2 Pin 3	Output 2 Pin 5	Comments
GND	0 1	0 1	0 1	0 1	Channels 1 & 2: Noninverting
V_{ref}	0 1	0 1	0 1	1 0	Channel 1: Noninverting Channel 2: Inverting
V_{CC} (>2.0 V)	0 1	1 0	0 1	1 0	Channels 1 & 2: Inverting

FUNCTIONAL DESCRIPTION

Introduction

To be competitive in today's electronic equipment market, new circuits must be designed to increase system reliability with minimal incremental cost. The circuit designer can take a significant step toward attaining these goals by implementing economical circuitry that continuously monitors critical circuit voltages and provides a fault signal in the event of an out-of-tolerance condition. The MC34161, MC33161 series are universal voltage monitors intended for use in a wide variety of voltage sensing applications. The main objectives of this series was to configure a device that can be used in as many voltage sensing applications as possible while minimizing cost. The flexibility objective is achieved by the utilization of a unique Mode Select input that is used in conjunction with traditional circuit building blocks. The cost objective is achieved by processing the device on a standard Bipolar Analog flow, and by limiting the package to eight pins. The device consists of two comparator channels each with hysteresis, a mode select input for channel programming, a pinned out reference, and two open collector outputs. Each comparator channel can be configured as either inverting or noninverting by the Mode Select input. This allows a single device to perform over, under, and window detection of positive and negative voltages. A detailed description of each section of the device is given below with the representative block diagram shown in Figure 13.

Input Comparators

The input comparators of each channel are identical, each having an upper threshold voltage of 1.27 V ±2.0% with 25 mV of hysteresis. The hysteresis is provided to enhance output switching by preventing oscillations as the comparator thresholds are crossed. The comparators have an input bias current of 60 nA at their threshold which approximates a 21.2 MΩ resistor to ground. This high impedance minimizes loading of the external voltage divider for well defined trip points. For all positive voltage sensing applications, both comparator channels are fully functional at a V_{CC} of 2.0 V. In order to provide enhanced device ruggedness for hostile industrial environments, additional circuitry was designed into the inputs to prevent device latch-up as well as to suppress electrostatic discharges (ESD).

Reference

The 2.54 V reference is pinned out to provide a means for the input comparators to sense negative voltages, as well as a means to program the Mode Select input for window detection applications. The reference is capable of sourcing in excess of 2.0 mA output current and has built-in short circuit protection. The output voltage has a guaranteed tolerance of ±2.4% at room temperature.

The 2.54 V reference is derived by gaining up the internal 1.27 V reference by a factor of two. With a power supply voltage of 4.0 V, the 2.54 V reference is in full regulation, allowing the device to accurately sense negative voltages.

Mode Select Circuit

The key feature that allows this device to be flexible is the Mode Select input. This input allows the user to program each of the channels for various types of voltage sensing applications. Figure 14 shows that the Mode Select input has three defined states. These states determine whether Channel 1 and/or Channel 2 operate in the inverting or noninverting mode. The Mode Select thresholds are shown in Figure 5. The input circuitry forms a tristate switch with thresholds at 0.63 V and V_{ref} + 0.23 V. The mode select input current is 10 μA when connected to the reference output, and 42 μA when connected to a V_{CC} of 5.0 V, refer to Figure 6.

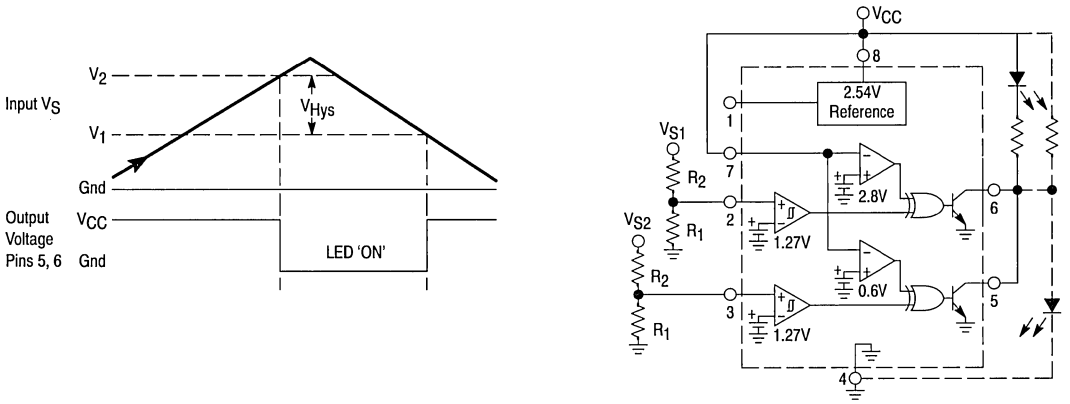
Output Stage

The output stage uses a positive feedback base boost circuit for enhanced sink saturation, while maintaining a relatively low device standby current. Figure 10 shows that the sink saturation voltage is about 0.2 V at 8.0 mA over temperature. By combining the low output saturation characteristics with low voltage comparator operation, this device is capable of sensing positive voltages at a V_{CC} of 1.0 V. These characteristics are important in undervoltage sensing applications where the output must stay in a low state as V_{CC} approaches ground. Figure 4 shows the Output Voltage versus Supply Voltage in an undervoltage sensing application. Note that as V_{CC} drops below the programmed 4.5 V trip point, the output stays in a well defined active low state until V_{CC} drops below 1.0 V.

APPLICATIONS

The following circuit figures illustrate the flexibility of this device. Included are voltage sensing applications for over, under, and window detectors, as well as three unique configurations. Many of the voltage detection circuits are shown with the open collector outputs of each channel connected together driving a light emitting diode (LED). This 'ORed' connection is shown for ease of explanation and it is only required for window detection applications. Note that many of the voltage detection circuits are shown with a dashed line output connection. This connection gives the inverse function of the solid line connection. For example, the solid line output connection of Figure 15 has the LED 'ON' when input voltage V_S is above trip voltage V_2, for overvoltage detection. The dashed line output connection has the LED 'ON' when V_S is below trip voltage V_2, for undervoltage detection.

Figure 15. Dual Postive Overvoltage Detector



The above figure shows the MC34161 configured as a dual positive overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when V_{S1} or V_{S2} exceeds V_2. With the dashed line output connection, the circuit becomes a dual positive undervoltage detector. As the input voltage decreases from the peak towards ground, the LED will turn 'ON' when V_{S1} or V_{S2} falls below V_1.

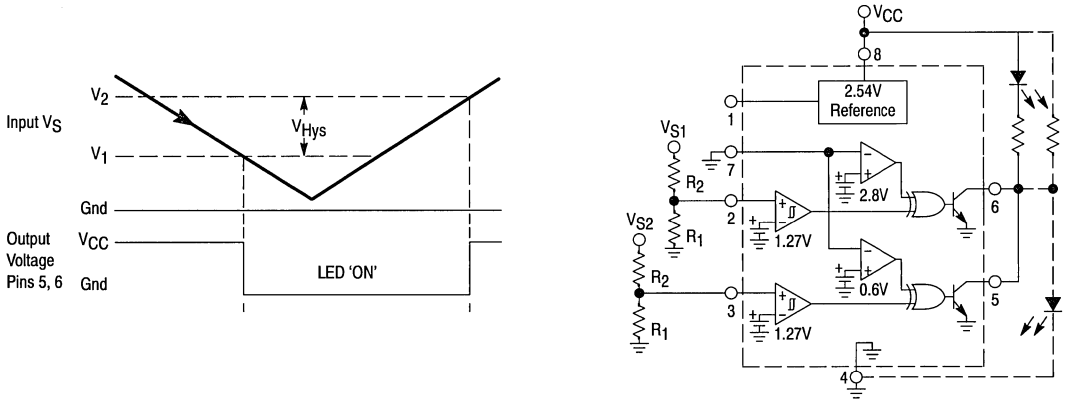
For known resistor values, the voltage trip points are:

$$V_1 = (V_{th} - V_H)\left(\frac{R_2}{R_1} + 1\right) \qquad V_2 = V_{th}\left(\frac{R_2}{R_1} + 1\right)$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_2}{R_1} = \frac{V_1}{V_{th} - V_H} - 1 \qquad \frac{R_2}{R_1} = \frac{V_2}{V_{th}} - 1$$

Figure 16. Dual Postive Undervoltage Detector



The above figure shows the MC34161 configured as a dual positive undervoltage detector. As the input voltage decreases towards ground, the LED will turn 'ON' when V_{S1} or V_{S2} falls below V_1. With the dashed line output connection, the circuit becomes a dual positive overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when V_{S1} or V_{S2} exceeds V_2.

For known resistor values, the voltage trip points are:

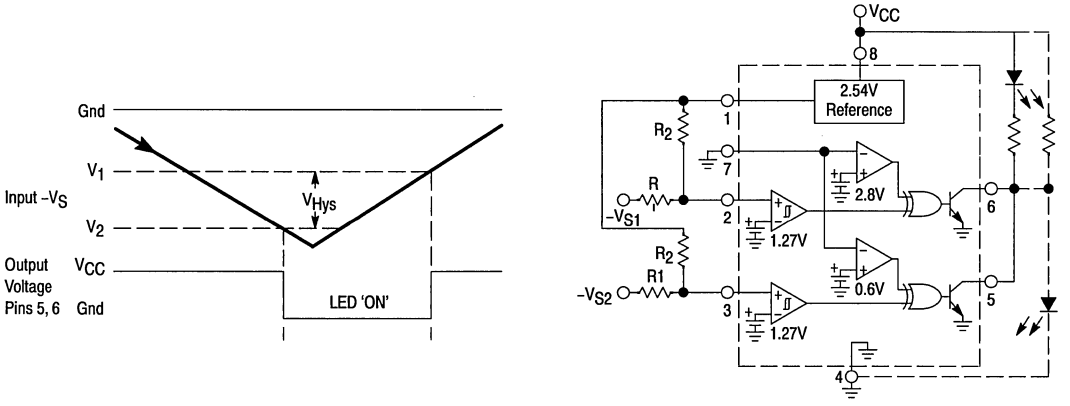
$$V_1 = (V_{th} - V_H)\left(\frac{R_2}{R_1} + 1\right) \qquad V_2 = V_{th}\left(\frac{R_2}{R_1} + 1\right)$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_2}{R_1} = \frac{V_1}{V_{th} - V_H} - 1 \qquad \frac{R_2}{R_1} = \frac{V_2}{V_{th}} - 1$$

3

Figure 17. Dual Negative Overvoltage Detector



The above figure shows the MC34161 configured as a dual negative overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when $-V_{S1}$ or $-V_{S2}$ exceeds V_2. With the dashed line output connection, the circuit becomes a dual negative undervoltage detector. As the input voltage decreases from the peak towards ground, the LED will turn 'ON' when $-V_{S1}$ or $-V_{S2}$ falls below V_1.

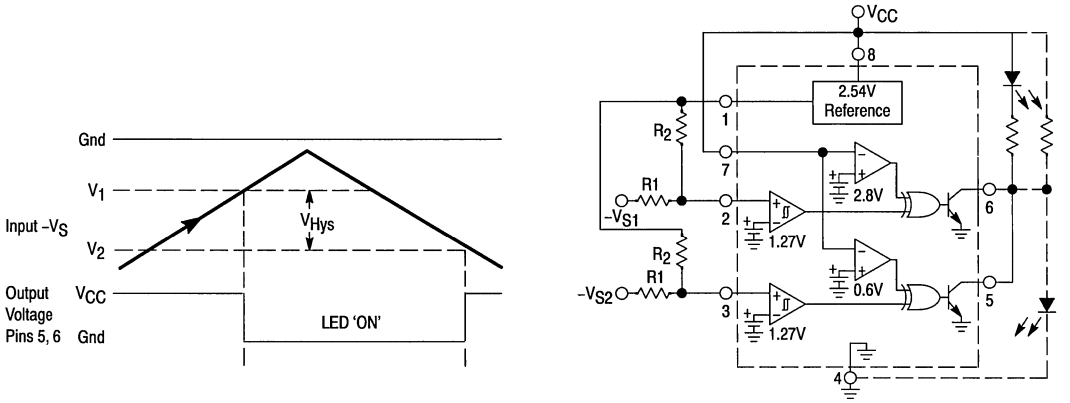
For known resistor values, the voltage trip points are:

$$V_1 = \frac{R_1}{R_2}(V_{th} - V_{ref}) + V_{th} \qquad V_2 = \frac{R_1}{R_2}(V_{th} - V_H - V_{ref}) + V_{th} - V_H$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_1}{R_2} = \frac{V_1 - V_{th}}{V_{th} - V_{ref}} \qquad \frac{R_1}{R_2} = \frac{V_2 - V_{th} + V_H}{V_{th} - V_H - V_{ref}}$$

Figure 18. Dual Negative Undervoltage Detector



The above figure shows the MC34161 configured as a dual negative undervoltage detector. As the input voltage decreases towards ground, the LED will turn 'ON' when $-V_{S1}$ or $-V_{S2}$ falls below V_1. With the dashed line output connection, the circuit becomes a dual negative overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when $-V_{S1}$ or $-V_{S2}$ exceeds V_2.

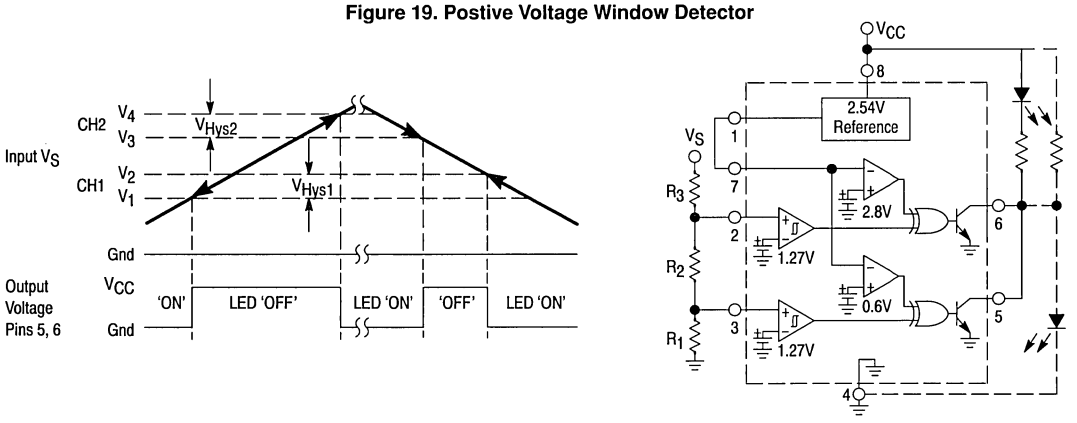
For known resistor values, the voltage trip points are:

$$V_1 = \frac{R_1}{R_2}(V_{th} - V_{ref}) + V_{th} \qquad V_2 = \frac{R_1}{R_2}(V_{th} - V_H - V_{ref}) + V_{th} - V_H$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_1}{R_2} = \frac{V_1 - V_{th}}{V_{th} - V_{ref}} \qquad \frac{R_1}{R_2} = \frac{V_2 - V_{th} + V_H}{V_{th} - V_H - V_{ref}}$$

Figure 19. Postive Voltage Window Detector



The above figure shows the MC34161 configured as a positive voltage window detector. This is accomplished by connecting channel 1 as an undervoltage detector, and channel 2 as an overvoltage detector. When the input voltage V_S falls out of the window established by V_1 and V_4, the LED will turn 'ON'. As the input voltage falls within the window, V_S increasing from ground and exceeding V_2, or VS decreasing from the peak towards ground and falling below V_3, the LED will turn 'OFF'. With the dashed line output connection, the LED will turn 'ON' when the input voltage V_S is within the window.

For known resistor values, the voltage trip points are:

$$V_1 = (V_{th1} - V_{H1})\left(\frac{R_3}{R_1 + R_2} + 1\right) \qquad V_3 = (V_{th2} - V_{H2})\left(\frac{R_2 + R_3}{R_1} + 1\right)$$

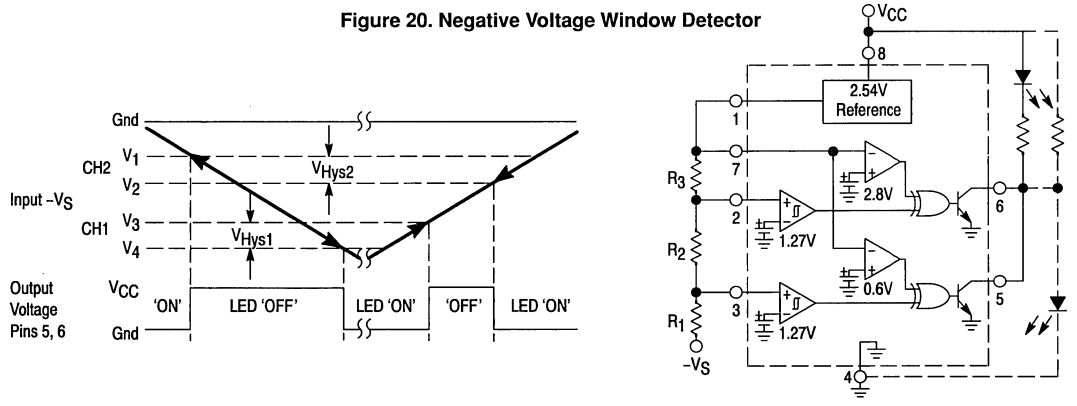
$$V_2 = V_{th1}\left(\frac{R_3}{R_1 + R_2} + 1\right) \qquad V_4 = V_{th2}\left(\frac{R_2 + R_3}{R_1} + 1\right)$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_2}{R_1} = \frac{V_3(V_{th2} - V_{H2})}{V_1(V_{th1} - V_{H1})} - 1 \qquad \frac{R_3}{R_1} = \frac{V_3(V_1 - V_{th1} + V_{H1})}{V_1(V_{th2} - V_{H2})}$$

$$\frac{R_2}{R_1} = \frac{V_4 \times V_{th2}}{V_2 \times V_{th1}} - 1 \qquad \frac{R_3}{R_1} = \frac{V_4(V_2 - V_{th1})}{V_2 \times V_{th2}}$$

Figure 20. Negative Voltage Window Detector



The above figure shows the MC34161 configured as a negative voltage window detector. When the input voltage $-V_S$ falls out of the window established by V_1 and V_4, the LED will turn 'ON'. As the input voltage falls within the window, $-V_S$ increasing from ground and exceeding V_2, or $-V_S$ decreasing from the peak towards ground and falling below V_3, the LED will turn 'OFF'. With the dashed line output connection, the LED will turn 'ON' when the input voltage $-V_S$ is within the window.

For known resistor values, the voltage trip points are:

$$V_1 = \frac{R_1(V_{th2} - V_{ref})}{R_2 + R_3} + V_{th2}$$

$$V_2 = \frac{R_1(V_{th2} - V_{H2} - V_{ref})}{R_2 + R_3} + V_{th2} - V_{H2}$$

$$V_3 = \frac{(R_1 + R_2)(V_{th1} - V_{ref})}{R_3} + V_{th1}$$

$$V_4 = \frac{(R_1 + R_2)(V_{th1} - V_{H1} - V_{ref})}{R_3} + V_{th1} - V_{H1}$$

For a specific trip voltage, the required resistor ratio is:

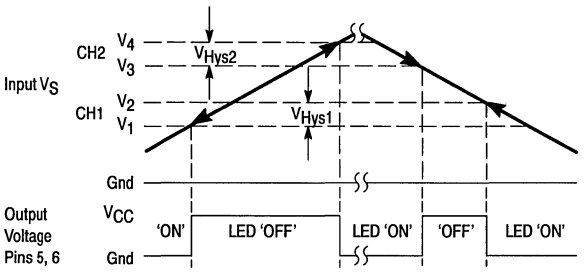
$$\frac{R_1}{R_2 + R_3} = \frac{V_1 - V_{th2}}{V_{th2} - V_{ref}}$$

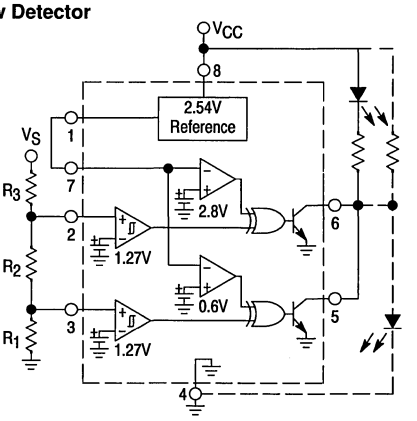
$$\frac{R_1}{R_2 + R_3} = \frac{V_2 - V_{th2} + V_{H2}}{V_{th2} - V_{H2} - V_{ref}}$$

$$\frac{R_3}{R_1 + R_2} = \frac{V_{th1} - V_{ref}}{V_3 - V_{th1}}$$

$$\frac{R_3}{R_1 + R_2} = \frac{V_{th1} - V_{H1} - V_{ref}}{V_4 + V_{H1} - V_{th1}}$$

Figure 19. Postive Voltage Window Detector





The above figure shows the MC34161 configured as a positive voltage window detector. This is accomplished by connecting channel 1 as an undervoltage detector, and channel 2 as an overvoltage detector. When the input voltage V_S falls out of the window established by V_1 and V_4, the LED will turn 'ON'. As the input voltage falls within the window, $V_S$increasing from ground and exceeding V_2, or VS decreasing from the peak towards ground and falling below V_3, the LED will turn 'OFF'. With the dashed line output connection, the LED will turn 'ON' when the input voltage V_S is within the window.

For known resistor values, the voltage trip points are:

$$V_1 = (V_{th1} - V_{H1})\left(\frac{R_3}{R_1 + R_2} + 1\right) \qquad V_3 = (V_{th2} - V_{H2})\left(\frac{R_2 + R_3}{R_1} + 1\right)$$

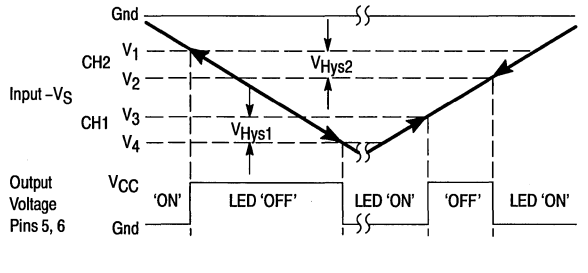
$$V_2 = V_{th1}\left(\frac{R_3}{R_1 + R_2} + 1\right) \qquad V_4 = V_{th2}\left(\frac{R_2 + R_3}{R_1} + 1\right)$$

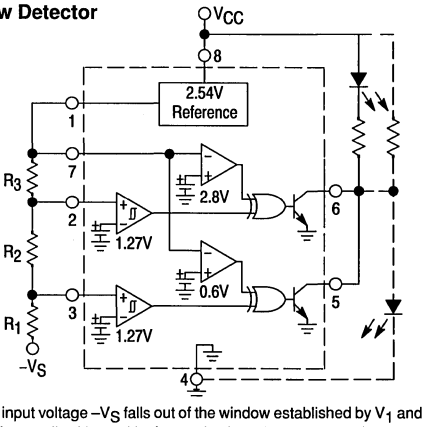
For a specific trip voltage, the required resistor ratio is:

$$\frac{R_2}{R_1} = \frac{V_3(V_{th2} - V_{H2})}{V_1(V_{th1} - V_{H1})} - 1 \qquad \frac{R_3}{R_1} = \frac{V_3(V_1 - V_{th1} + V_{H1})}{V_1(V_{th2} - V_{H2})}$$

$$\frac{R_2}{R_1} = \frac{V_4 \times V_{th2}}{V_2 \times V_{th1}} - 1 \qquad \frac{R_3}{R_1} = \frac{V_4(V_2 - V_{th1})}{V_2 \times V_{th2}}$$

Figure 20. Negative Voltage Window Detector





The above figure shows the MC34161 configured as a negative voltage window detector. When the input voltage $-V_S$ falls out of the window established by V_1 and V_4, the LED will turn 'ON'. As the input voltage falls within the window, $-V_S$ increasing from ground and exceeding V_2, or $-V_S$ decreasing from the peak towards ground and falling below V_3, the LED will turn 'OFF'. With the dashed line output connection, the LED will turn 'ON' when the input voltage $-V_S$ is within the window.

For known resistor values, the voltage trip points are:

$$V_1 = \frac{R_1(V_{th2} - V_{ref})}{R_2 + R_3} + V_{th2}$$

$$V_2 = \frac{R_1(V_{th2} - V_{H2} - V_{ref})}{R_2 + R_3} + V_{th2} - V_{H2}$$

$$V_3 = \frac{(R_1 + R_2)(V_{th1} - V_{ref})}{R_3} + V_{th1}$$

$$V_4 = \frac{(R_1 + R_2)(V_{th1} - V_{H1} - V_{ref})}{R_3} + V_{th1} - V_{H1}$$

For a specific trip voltage, the required resistor ratio is:

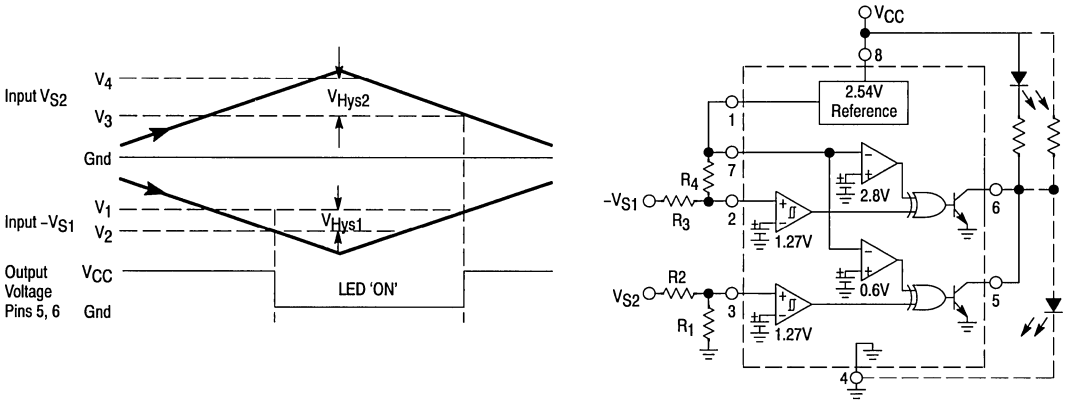
$$\frac{R_1}{R_2 + R_3} = \frac{V_1 - V_{th2}}{V_{th2} - V_{ref}}$$

$$\frac{R_1}{R_2 + R_3} = \frac{V_2 - V_{th2} + V_{H2}}{V_{th2} - V_{H2} - V_{ref}}$$

$$\frac{R_3}{R_1 + R_2} = \frac{V_{th1} - V_{ref}}{V_3 - V_{th1}}$$

$$\frac{R_3}{R_1 + R_2} = \frac{V_{th1} - V_{H1} - V_{ref}}{V_4 + V_{H1} - V_{th1}}$$

Figure 21. Positive and Negative Overvoltage Detector



The above figure shows the MC34161 configured as a positive and negative overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when either $-V_{S1}$ exceeds V_2, or V_{S2} exceeds V_4. With the dashed line output connection, the circuit becomes a positive and negative undervoltage detector. As the input voltage decreases from the peak towards ground, the LED will turn 'ON' when either V_{S2} falls below V_3, or $-V_{S1}$ falls below V_1.

For known resistor values, the voltage trip points are:

$$V_1 = \frac{R_3}{R_4}(V_{th1} - V_{ref}) + V_{th1} \qquad V_3 = (V_{th2} - V_{H2})\left(\frac{R_2}{R_1} + 1\right)$$

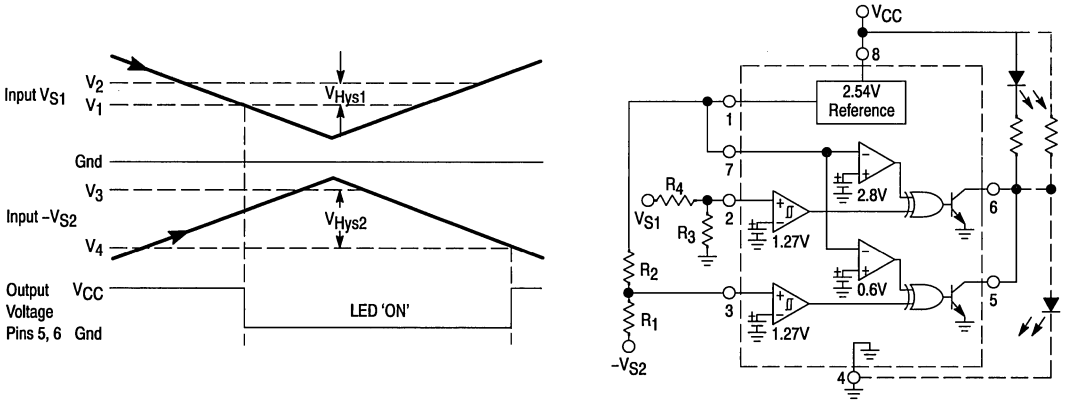
$$V_2 = \frac{R_3}{R_4}(V_{th1} - V_{H1} - V_{ref}) + V_{th1} - V_{H1} \qquad V_4 = V_{th2}\left(\frac{R_2}{R_1} + 1\right)$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_3}{R_4} = \frac{(V_1 - V_{th1})}{(V_{th1} - V_{ref})} \qquad \frac{R_2}{R_1} = \frac{V_4}{V_{th2}} - 1$$

$$\frac{R_3}{R_4} = \frac{(V_2 - V_{th1} + V_{H1})}{(V_{th1} - V_{H1} - V_{ref})} \qquad \frac{R_2}{R_1} = \frac{V_3}{V_{th2} - V_{H2}} - 1$$

Figure 22. Positive and Negative Undervoltage Detector



The above figure shows the MC34161 configured as a positive and negative undervoltage detector. As the input voltage decreases toward ground, the LED will turn 'ON' when either V_{S1} falls below V_1, or $-V_{S2}$ falls below V_3. With the dashed line output connection, the circuit becomes a positive and negative overvoltage detector. As the input voltage increases from the ground, the LED will turn 'ON' when either V_{S1} exceeds V_2, or $-V_{S1}$ exceeds V_1.

For known resistor values, the voltage trip points are:

$$V_1 = (V_{th1} - V_{H1})\left(\frac{R_4}{R_3} + 1\right) \qquad V_3 = \frac{R_1}{R_2}(V_{th} - V_{ref}) + V_{th2}$$

$$V_2 = V_{th1}\left(\frac{R_4}{R_3} + 1\right) \qquad V_4 = \frac{R_1}{R_2}(V_{th} - V_{H2} - V_{ref}) + V_{th2} - V_{H2}$$

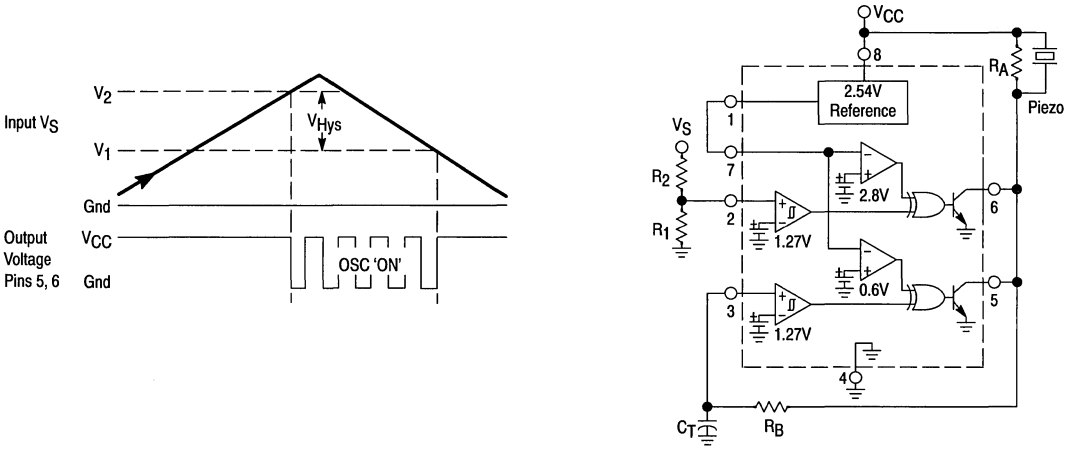
For a specific trip voltage, the required resistor ratio is:

$$\frac{R_4}{R_3} = \frac{V_2}{V_{th1}} - 1 \qquad \frac{R_1}{R_2} = \frac{V_4 + V_{H2} - V_{th2}}{V_{th2} - V_{H2} - V_{ref}}$$

$$\frac{R_4}{R_3} = \frac{V_1}{V_{th1} - V_{H1}} - 1 \qquad \frac{R_1}{R_2} = \frac{V_3 - V_{th2}}{V_{th2} - V_{ref}}$$

3

Figure 23. Overvoltage Detector with Audio Alarm



The above figure shows the MC34161 configured as an overvoltage detector with an audio alarm. Channel 1 monitors input voltage V_S while channel 2 is connected as a simple RC oscillator. As the input voltage increases from ground, the output of channel 1 allows the oscillator to turn 'ON' when V_S exceeds V_2.

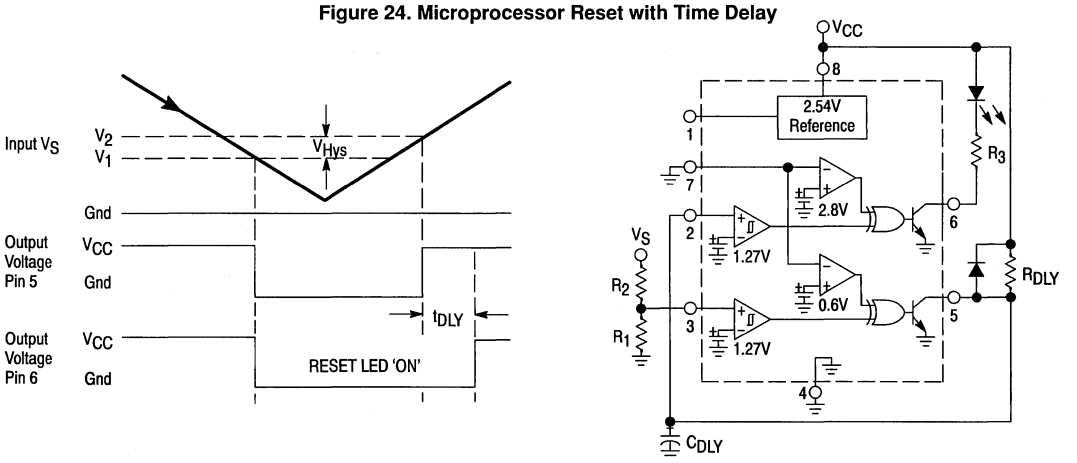
For known resistor values, the voltage trip points are:

$$V_1 = (V_{th} - V_H)\left(\frac{R_2}{R_1} + 1\right) \quad V_2 = V_{th}\left(\frac{R_2}{R_1} + 1\right)$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_2}{R_1} = \frac{V_1}{V_{th} - V_H} - 1 \qquad \frac{R_2}{R_1} = \frac{V_2}{V_{th}} - 1$$

Figure 24. Microprocessor Reset with Time Delay



The above figure shows the MC34161 configured as a microprocessor reset with a time delay. Channel 2 monitors input voltage V_S while channel 1 performs the time delay function. As the input voltage decreases towards ground, the output of channel 2 quickly discharges C_{DLY} when V_S falls below V_1. As the input voltage increases from ground, the output of channel 2 allows R_{DLY} to charge C_{DLY} when V_S exceeds V_2.

For known resistor values, the voltage trip points are:

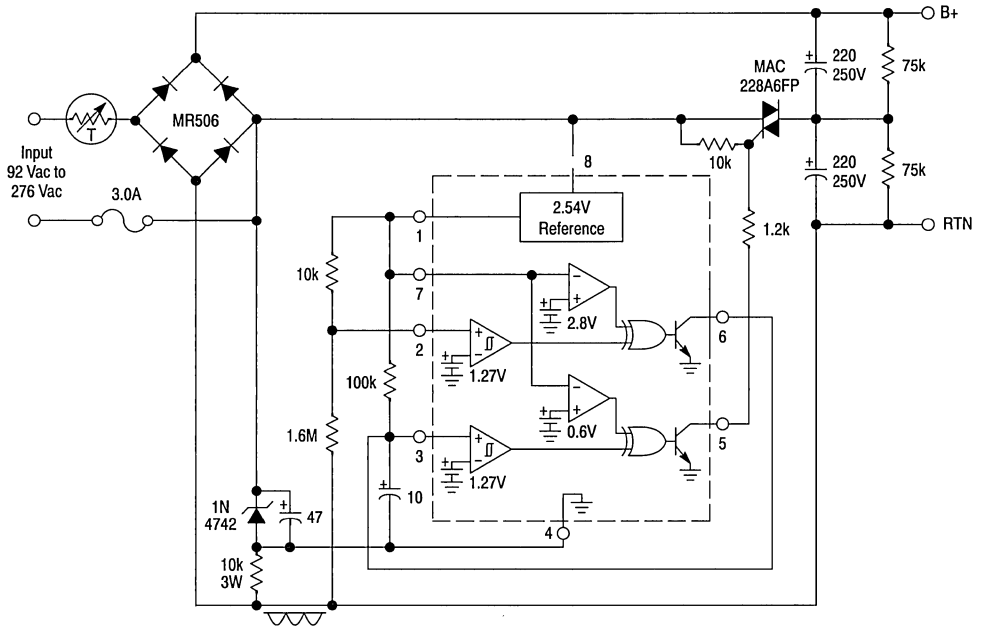
$$V_1 = (V_{th} - V_H)\left(\frac{R_2}{R_1} + 1\right) \quad V_2 = V_{th}\left(\frac{R_2}{R_1} + 1\right)$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_2}{R_1} = \frac{V_1}{V_{th} - V_H} - 1 \qquad \frac{R_2}{R_1} = \frac{V_2}{V_{th}} - 1$$

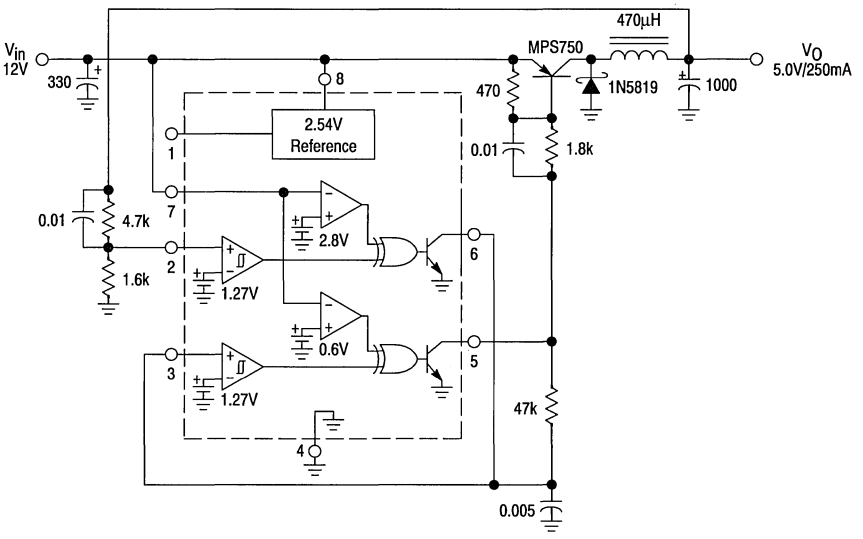
For known R_{DLY} C_{DLY} values, the reset time delay is: $t_{DLY} = R_{DLY}C_{DLY} \ln\left(\frac{1}{1 - \frac{V_{th}}{V_{CC}}}\right)$

Figure 25. Automatic AC Line Voltage Selector



The above circuit shows the MC34161 configured as an automatic line voltage selector. The IC controls the triac, enabling the circuit to function as a fullwave voltage doubler or a fullwave bridge. Channel 1 senses the negative half cycles of the AC line voltage. If the line voltage is less than150 V, the circuit will switch from bridge mode to voltage doubling mode after a preset time delay. The delay is controlled by the 100 kΩ resistor and the 10 µF capacitor. If the line voltage is greater than 150 V, the circuit will immediately return to fullwave bridge mode.

Figure 26. Step-Down Converter



Test	Conditions	Results
Line Regulation	V_{in} = 9.5 V to 24 V, I_O = 250 mA	40 mV = ±0.1%
Load Regulation	V_{in} = 12 V, I_O = 0.25 mA to 250 mA	2.0 mV = ±0.2%
Output Ripple	V_{in} = 12 V, I_O = 250 mA	50 mVp-p
Efficiency	V_{in} = 12 V, I_O = 250 mA	87.8%

The above figure shows the MC34161 configured as a step-down converter. Channel 1 monitors the output voltage while Channel 2 performs the oscillator function. Upon initial power-up, the converters output voltage will be below nominal, and the output of Channel 1 will allow the oscillator to run. The external switch transistor will eventually pump-up the output capacitor until its voltage exceeds the input threshold of Channel 1. The output of Channel 1 will then switch low and disable the oscillator. The oscillator will commence operation when the output voltage falls below the lower threshold of Channel 1.

MC34163
MC33163

Advance Information

Power Switching Regulators

POWER SWITCHING REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

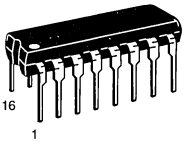
3

The MC34163 series are monolithic power switching regulators that contain the primary functions required for DC-to-DC converters. This series is specifically designed to be incorporated in step-up, step-down, and voltage-inverting applications with a minimum number of external components.

These devices consist of two high gain voltage feedback comparators, temperature compensated reference, controlled duty cycle oscillator, driver with bootstrap capability for increased efficiency, and a high current output switch. Protective features consist of cycle-by-cycle current limiting, and internal thermal shutdown. Also included is a low voltage indicator output designed to interface with microprocessor based systems.

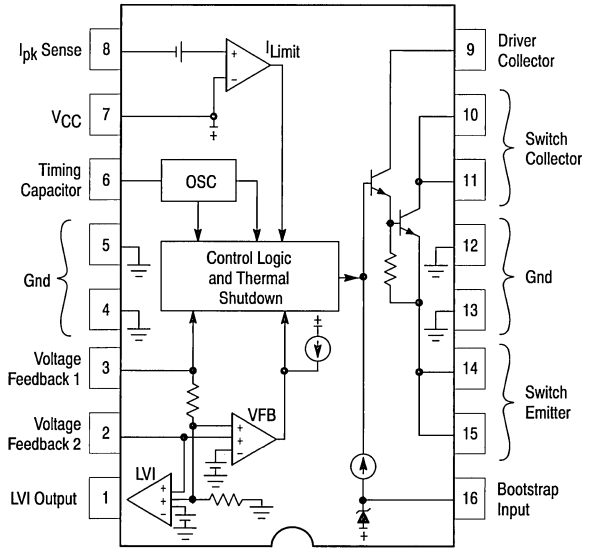
These devices are contained in a 16 pin dual-in-line heat tab plastic package for improved thermal conduction.

- Output Switch Current in Excess of 3.0 A
- Operation from 2.5 V to 40 V Input
- Low Standby Current
- Precision 2% Reference
- Controlled Duty Cycle Oscillator
- Driver with Bootstrap Capability for Increased Efficiency
- Cycle-by-Cycle Current Limiting
- Internal Thermal Shutdown Protection
- Low Voltage Indicator Output for Direct Microprocessor Interface
- Heat Tab Power Package



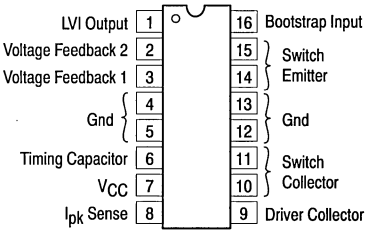
P SUFFIX
PLASTIC PACKAGE
CASE 648C

Simplified Block Diagram



(Bottom View)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34163P	0° to +70°C	16 Plastic DIP
MC33163P	– 40° to + 85°C	16 Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Switch Collector Voltage Range	$V_{C(switch)}$	–1.0 to + 40	V
Switch Emitter Voltage Range	$V_{E(switch)}$	– 2.0 to $V_{C(switch)}$	V
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	V
Switch Current (Note 1)	I_{SW}	3.4	A
Driver Collector Voltage	$V_{C(driver)}$	–1.0 to +40	V
Driver Collector Current	$I_{C(driver)}$	150	mA
Bootstrap Input Current Range (Note 1)	I_{BS}	–100 to +100	mA
Current Sense Input Voltage Range	$V_{Ipk(sense)}$	(V_{CC}–7.0) to (V_{CC}+1.0)	V
Feedback and Timing Capacitor Input Voltage Range	V_{in}	–1.0 to + 7.0	V
Low Voltage Indicator Output Voltage Range	$V_{C(LVI)}$	–1.0 to + 40	V
Low Voltage Indicator Output Sink Current	$I_{C(LVI)}$	10	mA
Power Dissipation and Thermal Characteristics P Suffix Package Case 648C Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction-to-Air Thermal Resistance Junction-to-Case (Pins 4, 5, 12, 13)	 P_D $R_{\theta JA}$ $R_{\theta JC}$	 1.56 80 15	 W °C/W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34163 MC33163	T_A	 0 to +70 – 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, Pin 16 = V_{CC}, C_T = 620 pF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency T_A = 25°C Total Variation over V_{CC} = 2.5 V to 40 V, and Temperature	f_{OSC}	 46 45	 50 —	 54 55	kHz
Charge Current	I_{chg}	—	225	—	µA
Discharge Current	I_{dischg}	—	25	—	µA
Charge to Discharge Current Ratio	I_{chg}/I_{dischg}	8.0	9.0	10	—
Sawtooth Peak Voltage	$V_{OSC(P)}$	—	1.25	—	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	—	0.55	—	V
FEEDBACK COMPARATOR 1					
Threshold Voltage T_A = 25°C Line Regulation (V_{CC} = 2.5 V to 40 V, T_A = 25°C) Total Variation over Line, and Temperature	$V_{th(FB1)}$	 4.9 — 4.85	 5.05 0.008 —	 5.2 0.03 5.25	 V %/V V
Input Bias Current (V_{FB1} = 5.05 V)	$I_{IB(FB1)}$	—	100	200	µA
FEEDBACK COMPARATOR 2					
Threshold Voltage T_A = 25°C Line Regulation (V_{CC} = 2.5 V to 40 V, T_A = 25°C) Total Variation over Line, and Temperature	$V_{th(FB2)}$	 1.225 — 1.213	 1.25 0.008 —	 1.275 0.03 1.287	 V %/V V
Input Bias Current (V_{FB2} = 1.25 V)	$I_{IB(FB2)}$	– 0.4	0	0.4	µA

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, Pin 16 = V_{CC}, C_T = 620 pF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT LIMIT COMPARATOR					
Threshold Voltage T_A = 25°C Total Variation over V_{CC} = 2.5 V to 40 V, and Temperature	$V_{th(Ipksense)}$	 — 230	 250 —	 — 270	mV
Input Bias Current ($V_{Ipk(sense)}$ = 15 V)	$I_{IB(sense)}$	—	1.0	20	μA
DRIVER AND OUTPUT SWITCH (Note 2)					
Sink Saturation Voltage (I_{SW} = 2.5 A, Pins 14, 15 grounded) Non-Darlington Connection ($R_{Pin\ 9}$ = 110 Ω to V_{CC}, I_{SW}/I_{DRV} ≈ 20) Darlington Connection (Pins 9, 10, 11 connected)	$V_{CE(sat)}$	 — —	 0.6 1.0	 1.0 1.4	V
Collector Off-State Leakage Current (V_{CE} = 40 V)	$I_{C(off)}$	—	0.02	100	μA
Bootstrap Input Current Source (V_{BS} = V_{CC} + 5.0 V)	$I_{source(DRV)}$	0.5	2.0	4.0	mA
Bootstrap Input Zener Clamp Voltage (I_Z = 25 mA)	V_Z	V_{CC} + 6.0	V_{CC} + 7.0	V_{CC} + 9.0	V
LOW VOLTAGE INDICATOR					
Input Threshold (V_{FB2} Increasing)	V_{th}	1.07	1.125	1.18	V
Input Hysteresis (V_{FB2} Decreasing)	V_H	—	15	—	mV
Output Sink Saturation Voltage (I_{sink} = 2.0 mA)	$V_{OL(LVI)}$	—	0.15	0.4	V
Output Off-State Leakage Current (V_{OH} = 15 V)	I_{OH}	—	0.01	5.0	μA
TOTAL DEVICE					
Standby Supply Current (V_{CC} = 2.5 V to 40 V, Pin 8 = V_{CC}, Pins 6, 14, 15 = Gnd, remaining pins open)	I_{CC}	—	6.0	10	mA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34163 = − 40°C for MC33163 T_{high} = + 70°C for MC34163 = + 85°C for MC33163

Figure 1. Output Switch On-Off Time versus Oscillator Timing Capacitor

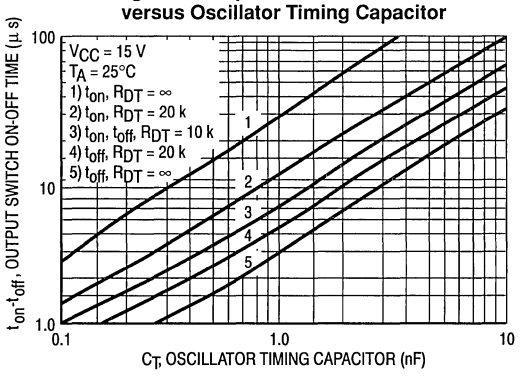


Figure 2. Oscillator Frequency Change versus Temperature

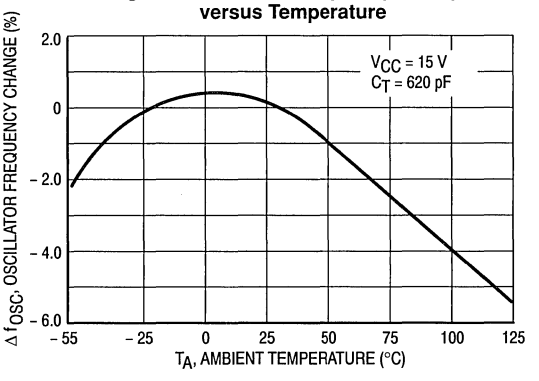


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Figure 3. Feedback Comparator 1 Input Bias Current versus Temperature

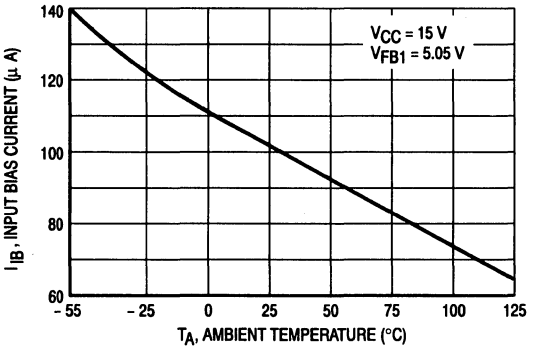

Figure 4. Feedback Comparator 2 Threshold Voltage versus Temperature

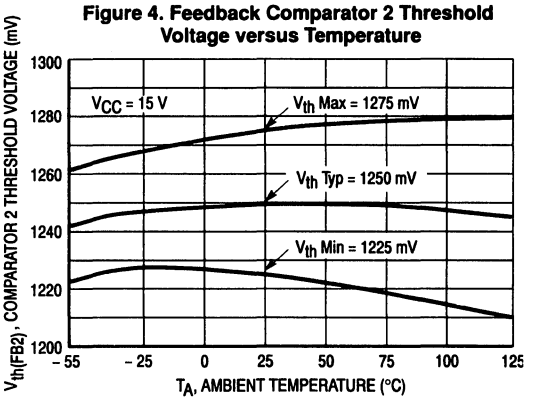

Figure 5. Bootstrap Input Current Source versus Temperature

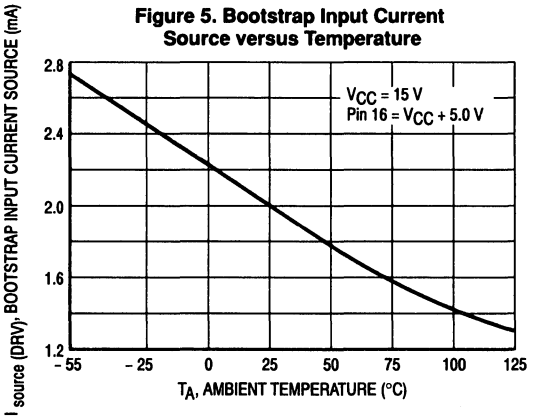

Figure 6. Bootstrap Input Zener Clamp Voltage versus Temperature

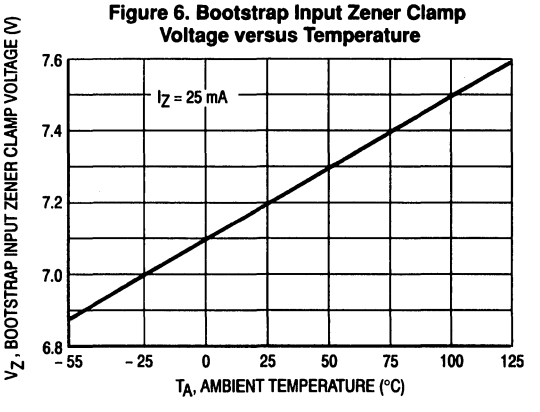

Figure 7. Output Switch Source Saturation versus Emitter Current

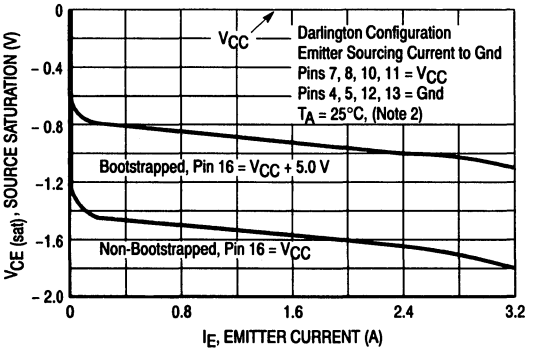

Figure 8. Output Switch Sink Saturation versus Collector Current

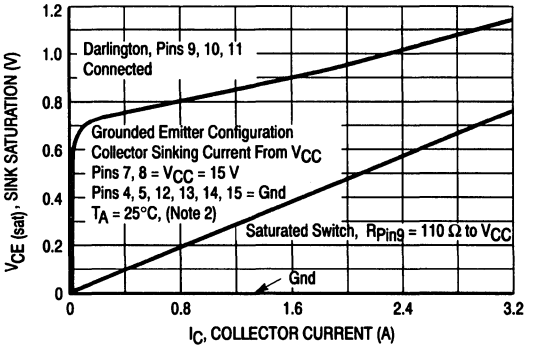

Figure 9. Output Switch Negative Emitter Voltage versus Temperature

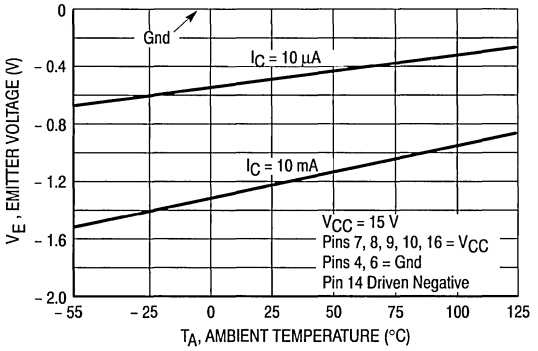

Figure 10. Low Voltage Indicator Output Sink Saturation Voltage versus Sink Current

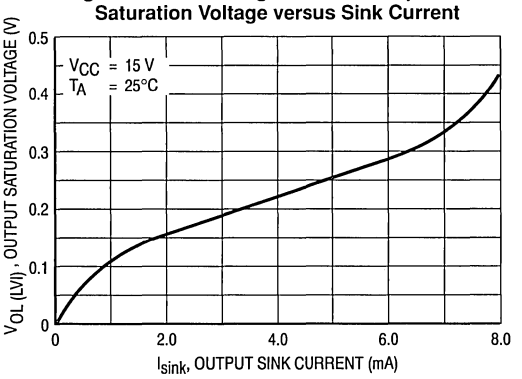

Figure 11. Current Limit Comparator Threshold Voltage versus Temperature

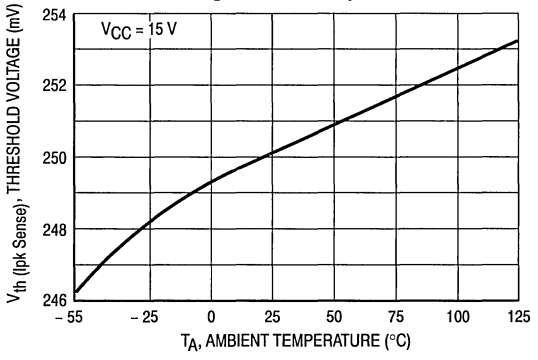

Figure 12. Current Limit Comparator Input Bias Current versus Temperature

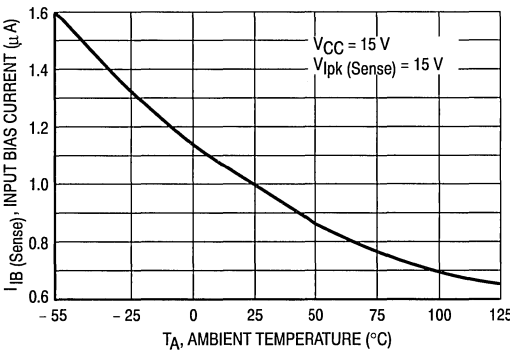

Figure 13. Standby Supply Current versus Supply Voltage

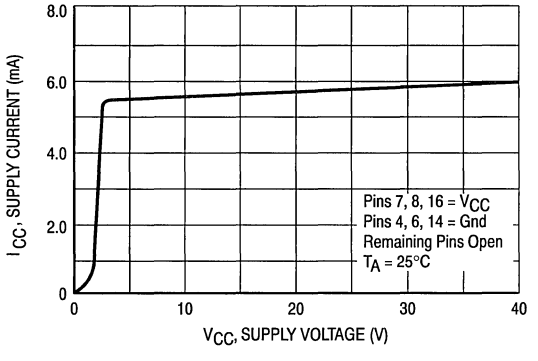

Figure 14. Standby Supply Current versus Temperature

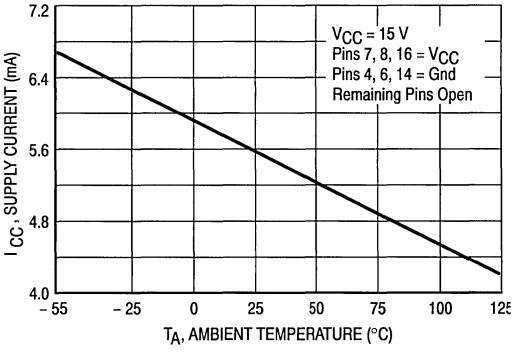

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Figure 15. Minimum Operating Supply Voltage versus Temperature

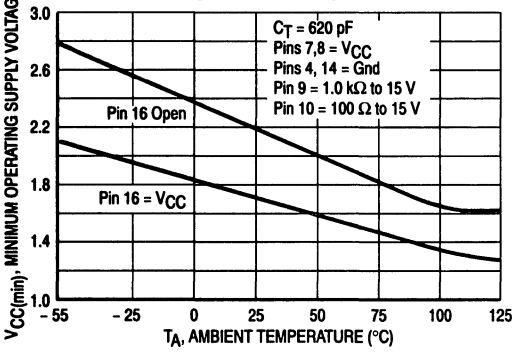


Figure 16. Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

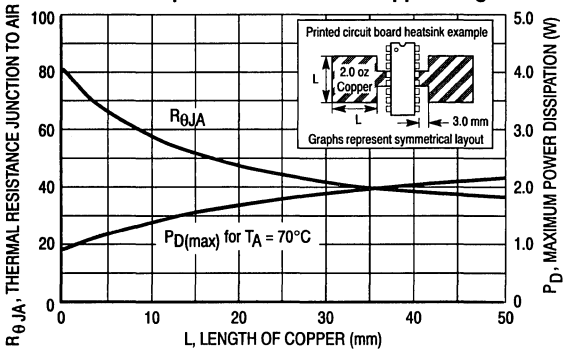


Figure 17. Representative Block Diagram

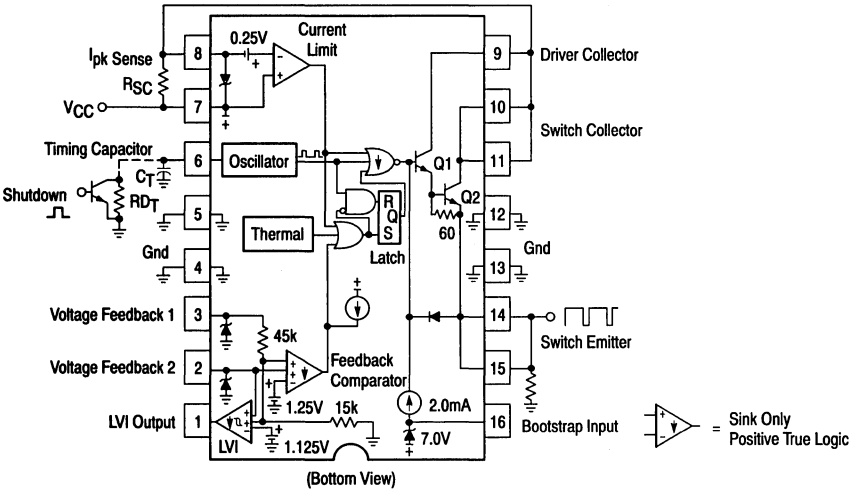
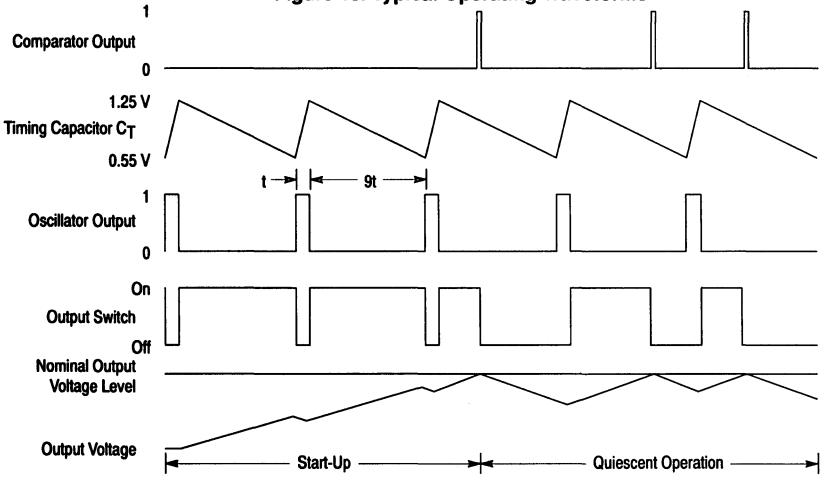


Figure 18. Typical Operating Waveforms



INTRODUCTION

The MC34163 series are monolithic power switching regulators optimized for DC-to-DC converter applications. The combination of features in this series enables the system designer to directly implement step-up, step-down, and voltage-inverting converters with a minimum number of external components. Potential applications include cost sensitive consumer products as well as equipment for the automotive, computer, and industrial markets. A Representative Block Diagram is shown in Figure 17.

Operating Description

The MC34163 operates as a fixed on-time, variable off-time voltage mode ripple regulator. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure 18. The output voltage waveform shown is for a step-down converter with the ripple and phasing exaggerated for clarity. During initial converter start-up, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the feedback comparator sets the latch, immediately terminating switch conduction. The feedback comparator will inhibit the switch until the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be inhibited for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles.

Oscillator

The oscillator frequency and on-time of the output switch are programmed by the value selected for timing capacitor C_T. Capacitor C_T is charged and discharged by a 9 to 1 ratio internal current source and sink, generating a negative going sawtooth waveform at Pin 6. As C_T charges, an internal pulse is generated at the oscillator output. This pulse is connected to the NOR gate center input, preventing output switch conduction, and to the AND gate upper input, allowing the latch to be reset if the comparator output is low. Thus, the output switch is always disabled during ramp-up and can be enabled by the comparator output only at the start of ramp-down. The oscillator peak and valley thresholds are 1.25 V and 0.55 V, respectively, with a charge current of 225 μA and a discharge current of 25 μA, yielding a maximum on-time duty cycle of 90%. A reduction of the maximum duty cycle may be required for specific converter configurations. This can be accomplished with the addition of an external dead-time resistor (R_{DT}) placed across C_T. The resistor increases the discharge current which reduces the on-time of the output switch. A graph of the Output Switch On-Off Time versus Oscillator Timing Capacitance for various values of R_{DT} is shown in Figure 1. Note that the maximum output duty cycle, $t_{on}/t_{on} + t_{off}$, remains constant for values of C_T greater than 0.2 nF. The converter output can be inhibited by clamping C_T to ground with an external NPN small-signal transistor.

Feedback and Low Voltage Indicator Comparators

Output voltage control is established by the Feedback comparator. The inverting input is internally biased at 1.25 V and is not pinned out. The converter output voltage is typically divided down with two external resistors and monitored by the high impedance noninverting input at Pin 2. The maximum input bias current is ±0.4 μA, which can cause an output voltage error that is equal to the product of the input bias current and the upper divider resistance value. For applications that require 5.0 V, the converter output can be directly connected to the noninverting input at Pin 3. The high impedance input, Pin 2, must be grounded to prevent noise pickup. The internal resistor divider is set for a nominal voltage of 5.05 V. The additional 50 mV compensates for a 1.0% voltage drop in the cable and connector from the converter output to the load. The Feedback comparator's output state is controlled by the highest voltage applied to either of the two noninverting inputs.

The Low Voltage Indicator (LVI) comparator is designed for use as a reset controller in microprocessor-based systems. The inverting input is internally biased at 1.125 V, which sets the noninverting input thresholds to 90% of nominal. The LVI comparator has 15 mV of hysteresis to prevent erratic reset operation. The Open Collector output is capable of sinking in excess of 6.0 mA (see Figure 10). An external resistor (R_{LVI}) and capacitor (C_{DLY}) can be used to program a reset delay time (t_{DLY}) by the formula shown below, where $V_{th(MPU)}$ is the microprocessor reset input threshold. Refer to Figure 19.

$$t_{DLY} = R_{LVI}\, C_{DLY} \ln \left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{out}}} \right)$$

Current Limit Comparator, Latch and Thermal Shutdown

With a voltage mode ripple converter operating under normal conditions, output switch conduction is initiated by the oscillator and terminated by the Voltage Feedback comparator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the Current Limit comparator will protect the Output Switch.

The switch current is converted to a voltage by inserting a fractional ohm resistor, R_{SC}, in series with V_{CC} and output switch transistor Q2. The voltage drop across R_{SC} is monitored by the Current Sense comparator. If the voltage drop exceeds 250 mV with respect to V_{CC}, the comparator will set the latch and terminate output switch conduction on a cycle-by-cycle basis. This Comparator/Latch configuration ensures that the Output Switch has only a single on-time during a given oscillator cycle. The calculation for a value of R_{SC} is:

$$R_{SC} = \frac{0.25\,V}{I_{pk(switch)}}$$

Figures 11 and 12 show that the Current Sense comparator threshold is tightly controlled over temperature and has a typical input bias current of 1.0 μA. The propagation delay from the comparator input to the Output Switch is typically 200 ns. The parasitic inductance associated with R_{SC} and the circuit layout should be minimized. This will prevent unwanted voltage spikes that may falsely trip the Current Limit comparator.

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the Latch is forced into the "Set" state, disabling the Output Switch. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.

Driver and Output Switch

To aid in system design flexibility and conversion efficiency, the driver current source and collector, and output switch collector and emitter are pinned out separately. This allows the designer the option of driving the output switch into saturation with a selected force gain or driving it near saturation when connected as a Darlington. The output switch has a typical current gain of 70 at 2.5 A and is designed to switch a maximum of 40 V collector to emitter, with up to 3.4 A peak collector current. The minimum value for R_{SC} is:

$$R_{SC(min)} = \frac{0.25\,V}{3.4\,A} = 0.0735\ \Omega$$

When configured for step-down or voltage-inverting applications, as in Figures 19 and 23, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn-on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency.

Figure 9 shows that by clamping the emitter to 0.5 V, the collector current will be in the range 10 μA over temperature. A 1N5822 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

A bootstrap input is provided to reduce the output switch saturation voltage in step-down and voltage-inverting converter applications. This input is connected through a series resistor and capacitor to the switch emitter and is used to raise the internal 2.0 mA bias current source above V_{CC}. An internal zener limits the bootstrap input voltage to V_{CC} + 7.0 V. The capacitor's equivalent series resistance must limit the zener current to less than 100 mA. An additional series resistor may be required when using tantalum or other low ESR capacitors. The equation below is used to calculate a minimum value bootstrap capacitor based on a minimum zener voltage and an upper limit current source.

$$C_{B(min)} = I\,\frac{\Delta t}{\Delta V} = 4.0\,mA\,\frac{t_{on}}{4.0\,V} = 0.001\,t_{on}$$

Parametric operation of the MC34163 is guaranteed over a supply voltage range of 2.5 V to 40 V. When operating below 3.0 V, the Bootstrap Input should be connected to V_{CC}. Figure 15 shows that functional operation down to 1.7 V at room temperature is possible.

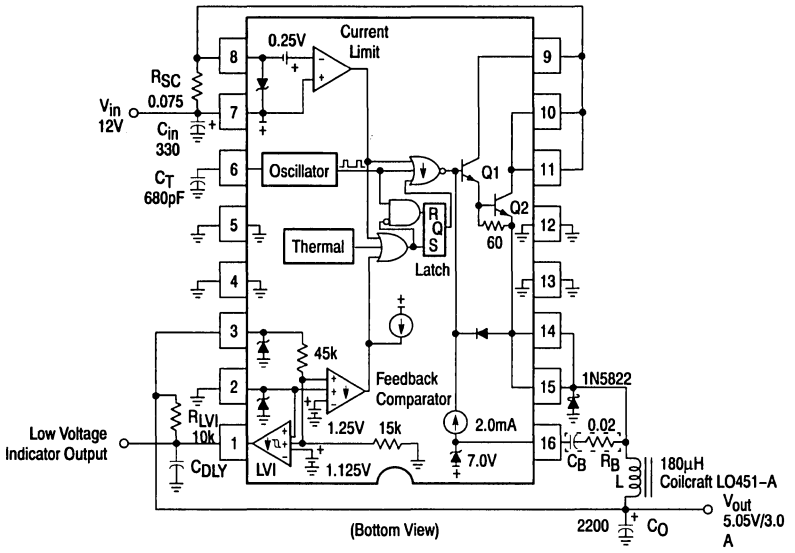
Package

The MC34163 is contained in a heatsinkable 16-lead plastic dual-in-line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figure 16 shows a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance. This example is for a symmetrical layout on a single-sided board with two ounce per square foot of copper.

APPLICATIONS

The following converter applications show the simplicity and flexibility of this circuit architecture. Three main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams.

Figure 19. Step-Down Converter



Test	Condition	Results
Line Regulation	V_{in} = 8.0 V to 24 V, I_O = 3.0 A	6.0 mV = ± 0.06%
Load Regulation	V_{in} = 12 V, I_O = 0.6 A to 3.0 A	2.0 mV = ± 0.02%
Output Ripple	V_{in} = 12 V, I_O = 3.0 A	36 mVp-p
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	3.3 A
Efficiency, Without Bootstrap	V_{in} = 12 V, I_O = 3.0 A	76.7%
Efficiency, With Bootstrap	V_{in} = 12 V, I_O = 3.0 A	81.2%

Figure 20. External Current Boost Connections for $I_{pk(switch)}$ Greater Than 3.4 A

Figure 20A. External NPN Switch

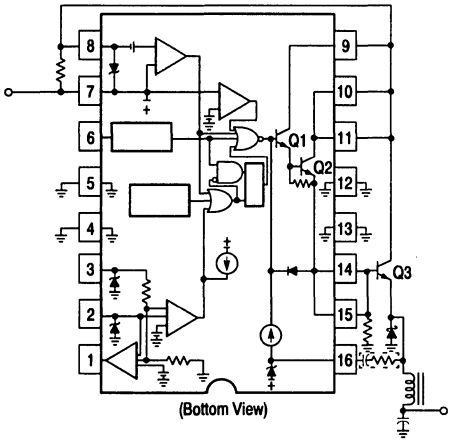


Figure 20B. External PNP Saturated Switch

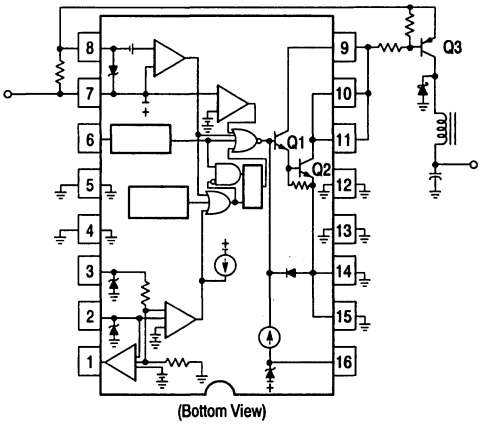


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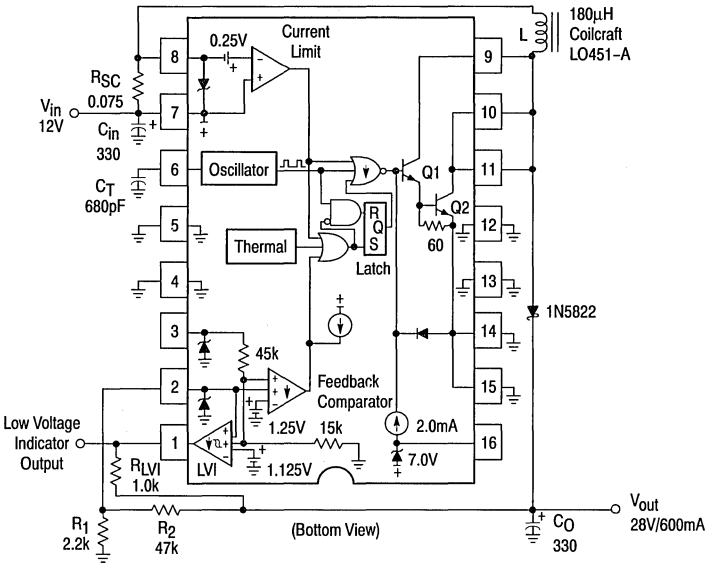
Figure 21. Step-Up Converter



Test	Condition	Results
Line Regulation	V_{in} = 9.0 V to 16 V, I_O = 0.6 A	30 mV = ± 0.05%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 0.6 A	50 mV = ± 0.09%
Output Ripple	V_{in} = 12 V, I_O = 0.6 A	140 mVp-p
Efficiency	V_{in} = 12 V, I_O = 0.6 A	88.1%

Figure 22. External Current Boost Connections for $I_{pk(switch)}$ Greater Than 3.4 A

Figure 22A. External NPN Switch

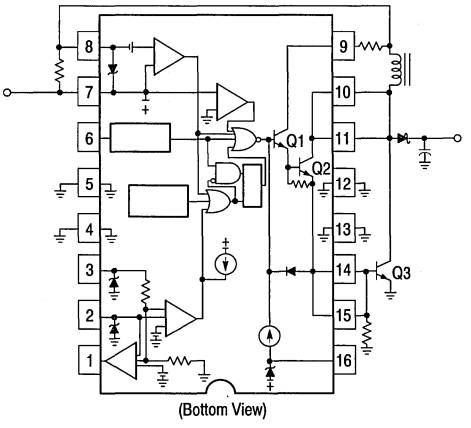


Figure 22B. External PNP Saturated Switch

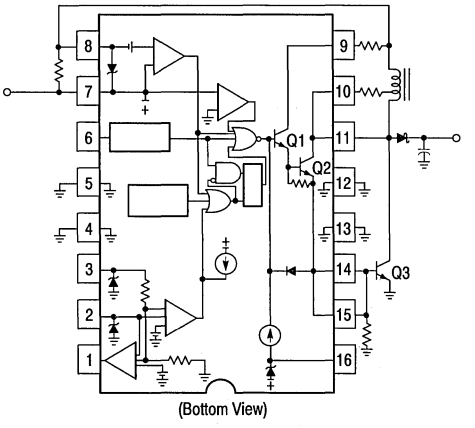
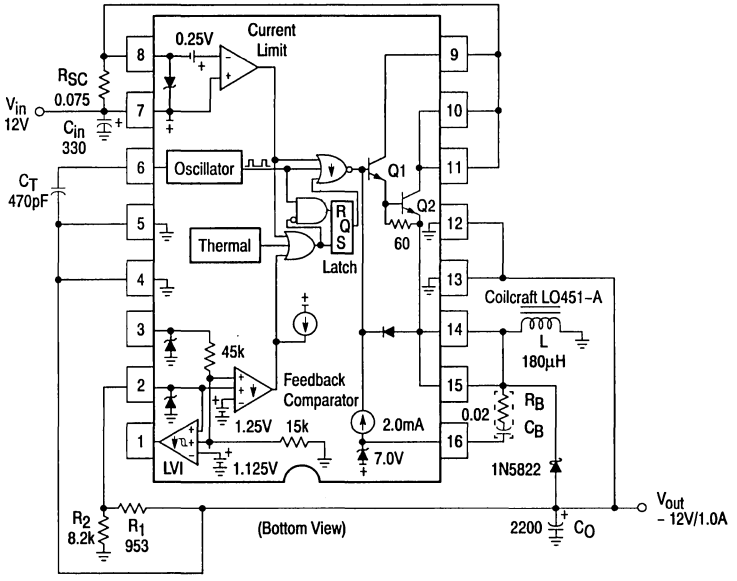


Figure 23. Voltage-Inverting Converter



Test	Condition	Results
Line Regulation	V_{in} = 9.0 V to 16 V, I_O = 1.0 A	5.0 mV = ± 0.02%
Load Regulation	V_{in} = 12 V, I_O = 0.6 A to 1.0 A	2.0 mV = ± 0.01%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	130 mVp-p
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	3.2 A
Efficiency, Without Bootstrap	V_{in} = 12 V, I_O = 1.0 A	73.1%
Efficiency, With Bootstrap	V_{in} = 12 V, I_O = 1.0 A	77.5%

Figure 24. External Current Boost Connections for $I_{pk(switch)}$ Greater Than 3.4 A

Figure 24A. External NPN Switch

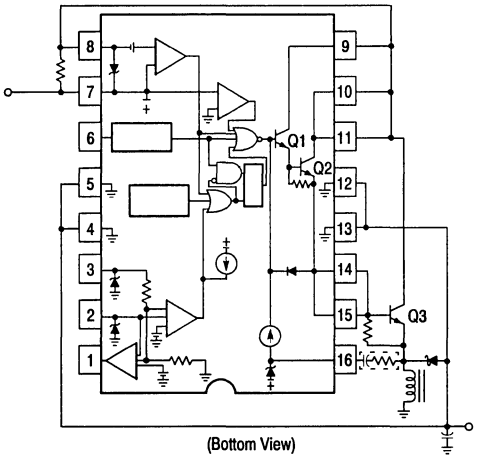


Figure 24B. External PNP Saturated Switch

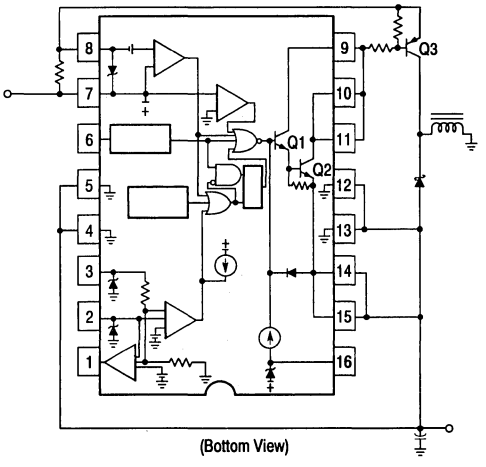
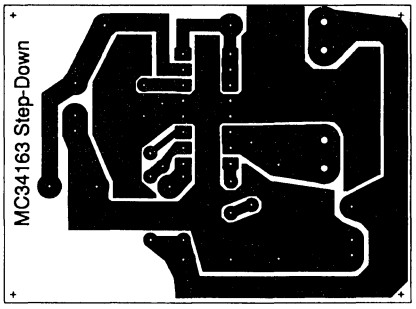
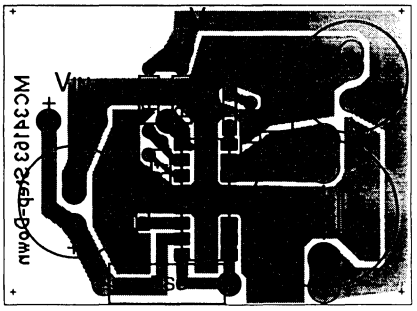


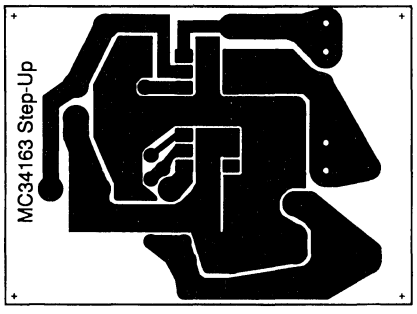
Figure 25. Printed Circuit Board and Component Layout (Circuits of Figures 19, 21, 23)



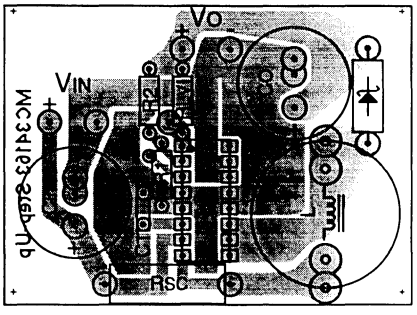
Bottom View



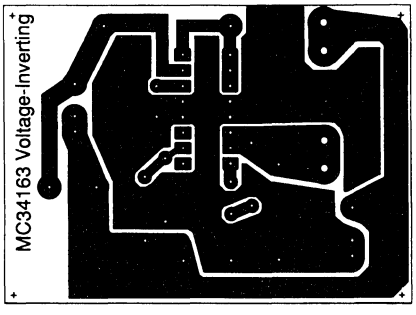
Top View



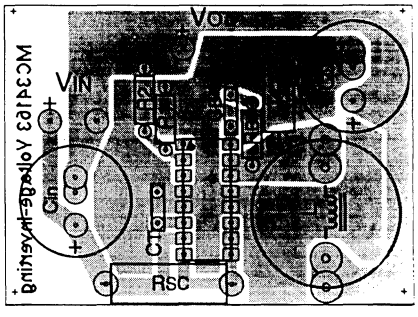
Bottom View



Top View



Bottom View



Top View

All printed circuit boards are 2.58" in width by 1.9" in height.

Figure 26. Design Equations

Calculation	Step-Down	Step-Up	Voltage-Inverting
$\frac{t_{on}}{t_{off}}$ (Notes 1, 2, 3)	$\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in} - V_{sat}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$
C_T	$35.7 \times 10^{-6}\, t_{on}$	$35.7 \times 10^{-6}\, t_{on}$	$35.7 \times 10^{-6}\, t_{on}$
$I_{L(avg)}$	I_{out}	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$
$I_{pk(switch)}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$
R_{SC}	$\frac{0.25}{I_{pk(switch)}}$	$\frac{0.25}{I_{pk(switch)}}$	$\frac{0.25}{I_{pk(switch)}}$
L	$\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right) t_{on}$
$V_{ripple(p\text{-}p)}$	$\Delta I_L \sqrt{\left(\frac{1}{8f\,C_O}\right)^2 + (ESR)^2}$	$\approx \frac{t_{on}\, I_{out}}{C_O}$	$\approx \frac{t_{on}\, I_{out}}{C_O}$
V_{out}	$V_{ref}\left(\frac{R2}{R1} + 1\right)$	$V_{ref}\left(\frac{R2}{R1} + 1\right)$	$V_{ref}\left(\frac{R2}{R1} + 1\right)$

The following Converter Characteristics must be chosen:

V_{in} — Nominal operating input voltage.

V_{out} — Desired output voltage.

I_{out} — Desired output current.

ΔI_L — Desired peak-to-peak inductor ripple current. For maximum output current it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L(avg)}$. This will help prevent $I_{pk(switch)}$ from reaching the current limit threshold set by R_{SC}. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2(I_{L(avg)})$. This will proportionally reduce converter output current capability.

f — Desired output switch frequency at the selected values of V_{in} and I_{out}.

$V_{ripple(p\text{-}p)}$ — Desired peak-to-peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

NOTES: 1. V_{sat} — Saturation voltage of the output switch, refer to Figures 7 and 8.

2. V_F — Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.5 V.

3. The calculated t_{on}/t_{off} must not exceed the minimum guaranteed oscillator charge to discharge ratio of 8, at the minimum operating input voltage.

MC34164
MC33164

3

Advance Information

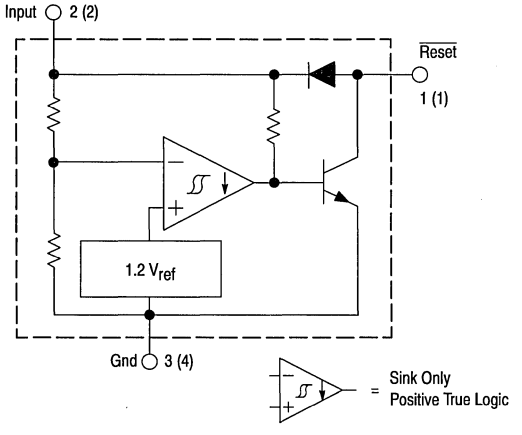
Micropower Undervoltage Sensing Circuits

The MC34164 series are undervoltage sensing circuits specifically designed for use as reset controllers in portable microprocessor based systems where extended battery life is required. These devices offer the designer an economical solution for low voltage detection with a single external resistor. The MC34164 series features a bandgap reference, a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation, an open collector reset output capable of sinking in excess of 6.0 mA, and guaranteed operation down to 1.0 V input with extremely low standby current. These devices are packaged in 3-pin TO-226AA and 8-pin surface mount packages.

Applications include direct monitoring of the 3.0 or 5.0 V MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment.

- Temperature Compensated Reference
- Monitors 3.0 V (MC34164-3) or 5.0 V (MC34164-5) Power Supplies
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 6.0 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation With 1.0 V Input
- Extremely Low Standby Current: As Low as 9.0 μA
- Economical TO-226AA and Surface Mount Packages

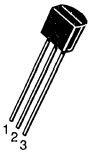
Representative Block Diagram



Pin numbers adjacent to terminals are for the 3-pin TO-226AA package.
Pin numbers in parenthesis are for the D suffix SO-8 package.

MICROPOWER UNDERVOLTAGE SENSING CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUIT



Pin 1. Reset
2. Input
3. Ground

P SUFFIX
PLASTIC PACKAGE
CASE 29
(TO-226AA)

Pin 1. Reset
2. Input
3. N.C.
4. Ground
5. N.C.
6. N.C.
7. N.C.
8. N.C.

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34164D-3	0° to + 70°C	SO-8
MC34164D-5		
MC34164P-3		TO-226AA
MC34164P-5		
MC33164D-3	– 40° to + 85°C	SO-8
MC33164D-5		
MC33164P-3		TO-226AA
MC33164P-5		

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	V_{in}	–1.0 to 12	V
$\overline{\text{Reset}}$ Output Voltage	V_O	–1.0 to 12	V
$\overline{\text{Reset}}$ Output Sink Current	I_{Sink}	Internally Limited	mA
Clamp Diode Forward Current, Pin 1 to 2 (Note 1)	I_F	100	mA
Power Dissipation and Thermal Characteristics P Suffix, Plastic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction to Air D Suffix, Plastic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 700 178 700 178	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range MC34164 Series MC33164 Series	T_A	 0 to +70 – 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C

MC34164-3, MC33164-3 SERIES

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Notes 2 & 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage High State Output (V_{in} Increasing) Low State Output (V_{in} Decreasing) Hysteresis (I_{Sink} = 100 µA)	 V_{IH} V_{IL} V_H	 2.55 2.55 0.03	 2.71 2.65 0.06	 2.80 2.80 —	V
$\overline{\text{RESET}}$ OUTPUT					
Output Sink Saturation (V_{in} = 2.4 V, I_{Sink} = 1.0 mA) (V_{in} = 1.0 V, I_{Sink} = 0.25 mA)	V_{OL}	 — —	 0.14 0.1	 0.4 0.3	V
Output Sink Current (V_{in}, $\overline{\text{Reset}}$ = 2.4 V)	I_{Sink}	6.0	12	30	mA
Output Off-State Leakage (V_{in}, $\overline{\text{Reset}}$ = 3.0 V) (V_{in}, $\overline{\text{Reset}}$ = 10 V)	$I_{\overline{R}(leak)}$	 — —	 0.02 0.02	 0.5 1.0	µA
Clamp Diode Forward Voltage, Pin 1 to 2 (I_F = 5.0 mA)	V_F	6.0	0.9	1.2	V
TOTAL DEVICE					
Operating Input Voltage Range	V_{in}	1.0 to 10	—	—	V
Quiescent Input Current V_{in} = 3.0 V V_{in} = 6.0 V	I_{in}	 — —	 9.0 24	 15 40	µA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34164, – 40°C for MC33164; T_{high} = + 70°C for MC34164, = + 80°C for MC34164

3

MC34164-5, MC33164-5 SERIES

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Notes 2 & 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage					V
High State Output (V_{in} Increasing)	V_{IH}	4.15	4.33	4.45	
Low State Output (V_{in} Decreasing)	V_{IL}	4.15	4.27	4.45	
Hysteresis (I_{Sink} = 100 μA)	V_H	0.02	0.09	—	
$\overline{\text{RESET}}$ OUTPUT					
Output Sink Saturation	V_{OL}				V
(V_{in} = 4.0 V, I_{Sink} = 1.0 mA)		—	0.14	0.4	
(V_{in} = 1.0 V, I_{Sink} = 0.25 mA)		—	0.1	0.3	
Output Sink Current (V_{in}, $\overline{\text{Reset}}$ = 4.0 V)	I_{Sink}	7.0	20	50	mA
Output Off-State Leakage	$I_{\overline{R}(leak)}$				μA
(V_{in}, $\overline{\text{Reset}}$ = 5.0 V)		—	0.02	0.5	
(V_{in}, $\overline{\text{Reset}}$ = 10 V)		—	0.02	2.0	
Clamp Diode Forward Voltage, Pin 1 to 2 (I_F = 5.0 mA)	V_F	0.6	0.9	1.2	V
TOTAL DEVICE					
Operating Input Voltage Range	V_{in}	1.0 to 10	—	—	V
Quiescent Input Current	I_{in}				μA
V_{in} = 5.0 V		—	12	20	
V_{in} = 10 V		—	32	50	

NOTES: 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

3. T_{low} = 0°C for MC34164, −40°C for MC33164; T_{high} = +70°C for MC34164, +80°C for MC34164

Figure 1. MC3X164-3 $\overline{\text{Reset}}$ Output Voltage versus Input Voltage

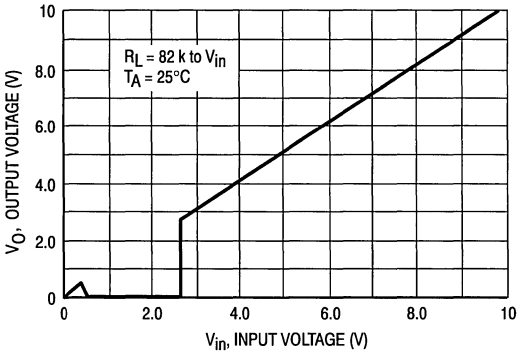


Figure 2. MC3X164-5 $\overline{\text{Reset}}$ Output Voltage versus Input Voltage

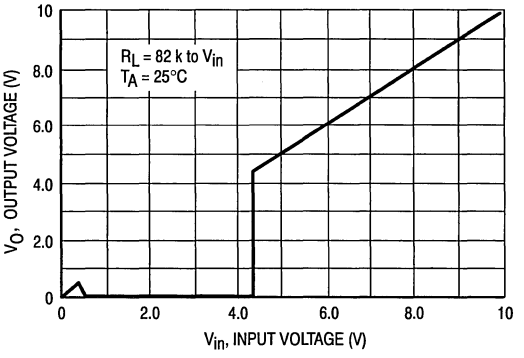


Figure 3. MC3X164-3 Reset Output Voltage versus Input Voltage

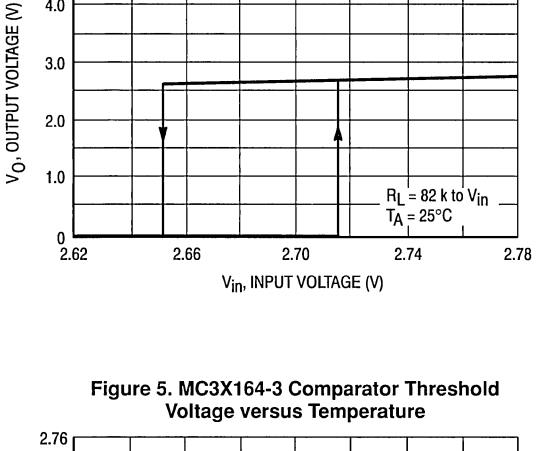


Figure 4. MC3X164-5 Reset Output Voltage versus Input Voltage

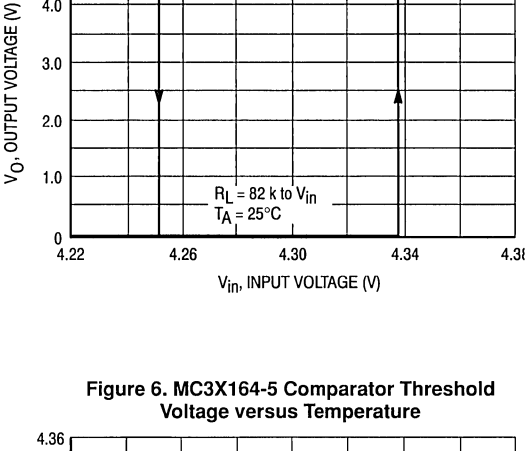


Figure 5. MC3X164-3 Comparator Threshold Voltage versus Temperature

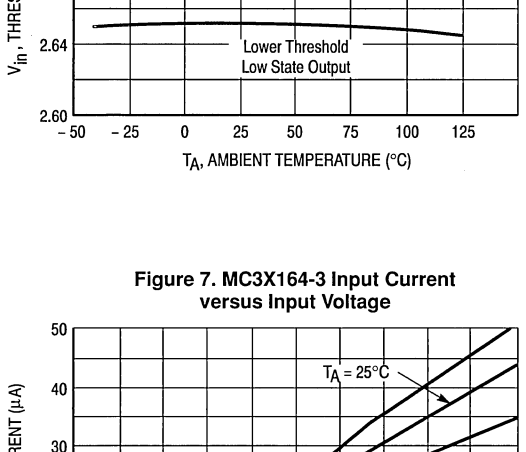


Figure 6. MC3X164-5 Comparator Threshold Voltage versus Temperature

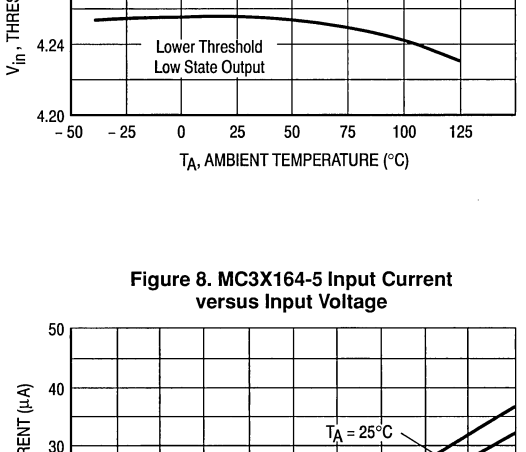


Figure 7. MC3X164-3 Input Current versus Input Voltage

Figure 8. MC3X164-5 Input Current versus Input Voltage

3

Figure 9. MC3X164-3 Reset Output Saturation versus Sink Current

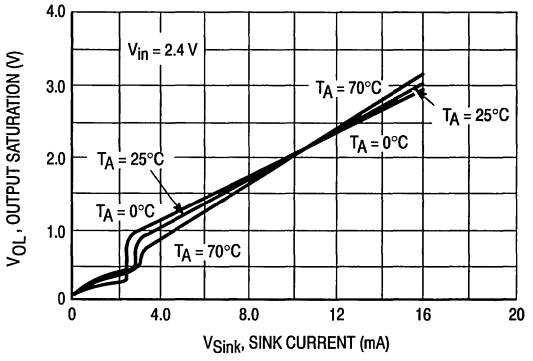


Figure 10. MC3X164-5 Reset Output Saturation versus Sink Current

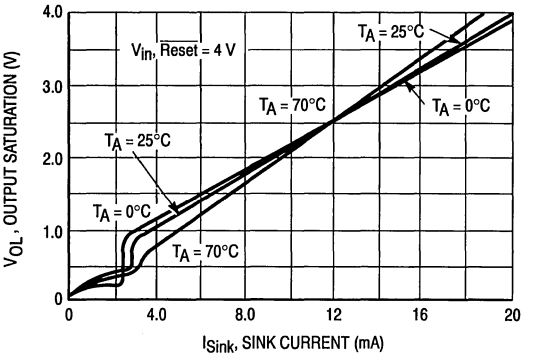


Figure 11. Clamp Diode Forward Current versus Voltage

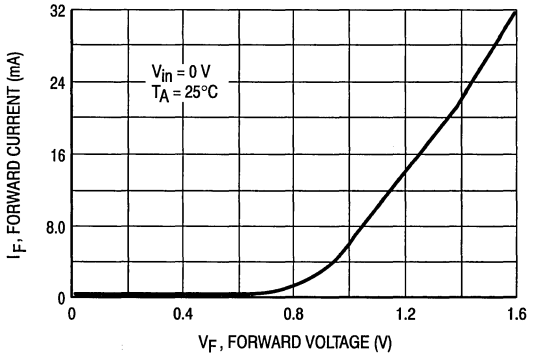


Figure 12. $\overline{Reset}$ Delay Time (MC3X164-5 Shown)

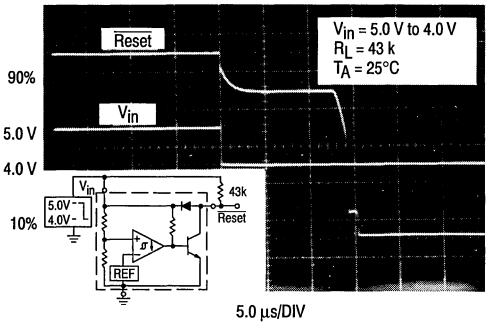
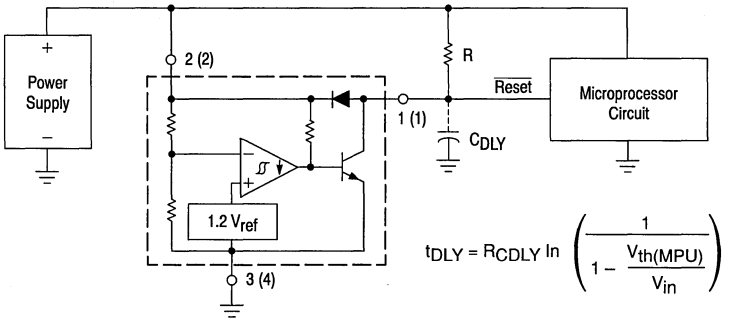
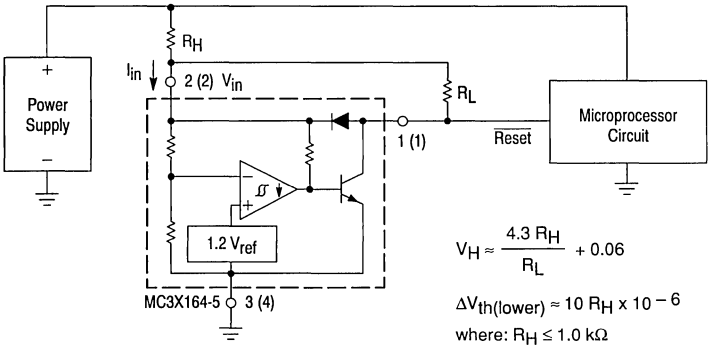


Figure 13. Low Voltage Microprocessor Reset



A time delayed reset can be accomplished with the addition of C_{DLY}. For systems with extremely fast power supply rise times (< 500 ns) it is recommended that the RCDLY time constant be greater than 5.0 µs. $V_{th(MPU)}$ is the microprocessor reset input threshold.

Figure 14. Low Voltage Microprocessor Reset With Additional Hysteresis (MC3X164-5 Shown)



$$V_H \approx \frac{4.3\ R_H}{R_L} + 0.06$$

$$\Delta V_{th(lower)} \approx 10\ R_H \times 10^{-6}$$

where: $R_H \leq 1.0\ k\Omega$

$43\ k\Omega \geq R_L \geq 4.3\ k\Omega$

Test Data			
V_H (mV)	ΔV_{th} (mV)	R_H (Ω)	R_L (kΩ)
60	0	0	43
103	1.0	100	10
123	1.0	100	6.8
160	1.0	100	4.3
155	2.2	220	10
199	2.2	220	6.8
280	2.2	220	4.3
262	4.7	470	10
306	4.7	470	8.2
357	4.7	470	6.8
421	4.7	470	5.6
530	4.7	470	4.3

Comparator hysteresis can be increased with the addition of resistor R_H. The hysteresis equation has been simplified and does not account for the change of input current I_{in} as V_{in} crosses the comparator threshold (Figure 8). An increase of the lower threshold $\Delta V_{th(lower)}$ will be observed due to I_{in} which is typically 10 μA at 4.3 V. The equations are accurate to ±10% with R_H less than 1.0 kΩ and R_L between 4.3 kΩ and 43 kΩ.

Figure 15. Voltage Monitor

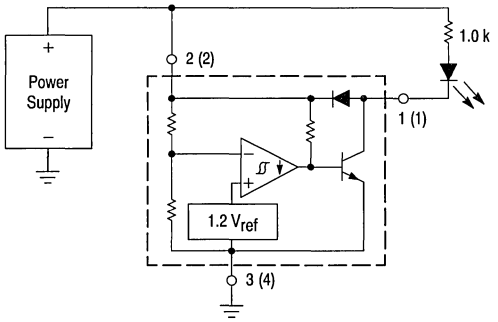


Figure 16. Solar Powered Battery Charger

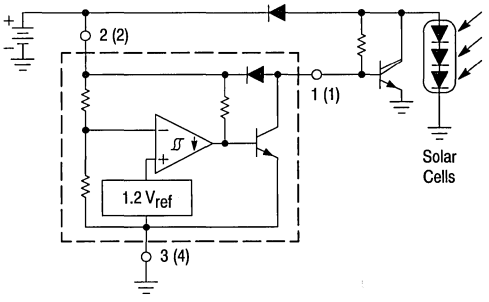
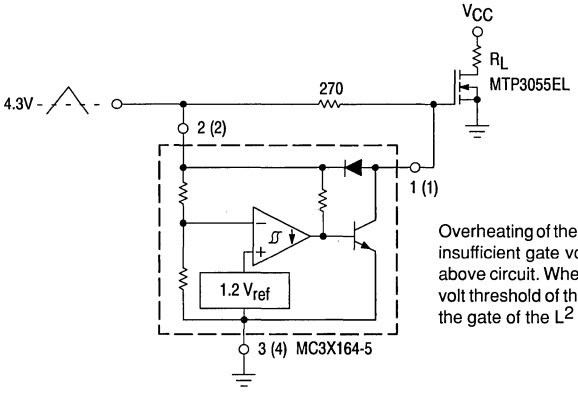


Figure 17. MOSFET Low Voltage Gate Drive Protection Using the MC3X164-5



Overheating of the logic level power MOSFET due to insufficient gate voltage can be prevented with the above circuit. When the input signal is below the 4.3 volt threshold of the MC3X164-5, its output grounds the gate of the L^2 MOSFET.

MC34166
MC33166

3

Advance Information

Power Switching Regulator

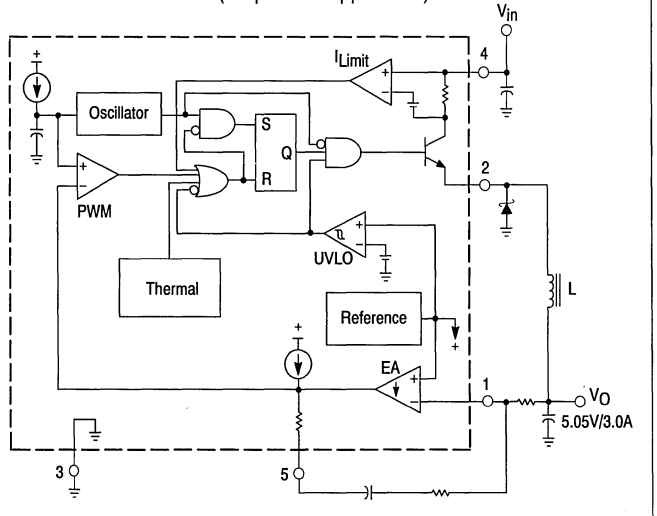
The MC34166, MC33166 series are high performance fixed frequency power switching regulators that contain the primary functions required for DC-to-DC converters. This series was specifically designed to be incorporated in step-down and voltage-inverting configurations with a minimum number of external components and can also be used cost effectively in step-up applications.

These devices consist of an internal temperature compensated reference, fixed frequency oscillator with on-chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch.

Protective features consist of cycle-by-cycle current limiting, undervoltage lockout, and thermal shutdown. Also included is a low power standby mode that reduces power supply current to 36 μA.

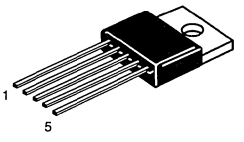
- Output Switch Current in Excess of 3.0 A
- Fixed Frequency Oscillator (72 kHz) with On-Chip Timing
- Provides 5.05 V Output Without External Resistor Divider
- Precision 2.0% Reference
- 0% to 95% Output Duty Cycle
- Cycle-by-Cycle Current Limiting
- Undervoltage Lockout with Hysteresis
- Internal Thermal Shutdown
- Operation from 7.5 V to 40 V
- Standby Mode Reduces Power Supply Current to 36 μA
- Economical Five Lead TO-220 Package

Simplified Block Diagram
(Step Down Application)

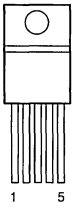


POWER SWITCHING REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



T SUFFIX
PLASTIC PACKAGE
CASE 314D



PIN CONNECTIONS

Pin 1. Voltage Feedback Input
2. Switch Output
3. Ground
4. Input Voltage/V_{CC}
5. Compensation/Standby

(Heatsink surface connected to Pin 3)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34166T	0° to + 70°C	Plastic Power
MC33166T	– 40° to + 85°C	Plastic Power

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	40	V
Switch Output Voltage Range	$V_{O(switch)}$	−1.5 to + V_{in}	V
Voltage Feedback and Compensation Input Voltage Range	V_{FB}, V_{Comp}	−1.0 to + 7.0	V
Power Dissipation and Thermal Characteristics (Note 1) Maximum Power Dissipation @ T_C = 70°C Thermal Resistance Junction to Case Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction-to-Air	 P_D θ_{JC} P_D θ_{JA}	 34.7 2.3 1.9 65	 W °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34166 MC33166	T_A	 0 to + 70 − 40 to + 85	°C
Storage Temperature Range	T_{stg}	− 65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 2, 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (V_{CC} = 7.5 V to 40 V) T_A = 25°C T_A = T_{low} to T_{high}	f_{OSC}	 65 62	 72 —	 79 81	kHz
ERROR AMPLIFIER					
Voltage Feedback Input Threshold T_A = 25°C T_A = T_{low} to T_{high}	$V_{FB(th)}$	 4.95 4.85	 5.05 —	 5.15 5.2	V
Line Regulation (V_{CC} = 7.5 V to 40 V, T_A = 25°C)	Reg_{line}	—	0.03	0.078	%/V
Input Bias Current (V_{FB} = $V_{FB(th)}$ + 0.15 V)	I_{IB}	—	0.15	1.0	µA
Power Supply Rejection Ratio (V_{CC} = 10 V to 20 V, f = 120 Hz)	PSRR	60	80	—	dB
Output Voltage Swing High State (I_{Source} = 75 µA, V_{FB} = 4.5 V) Low State (I_{Sink} = 0.4 mA, V_{FB} = 5.5 V)	 V_{OH} V_{OL}	 4.2 —	 4.9 1.6	 — 1.9	V
PWM COMPARATOR					
Duty Cycle Maximum (V_{FB} = 0 V) Minimum (V_{Comp} = 1.9 V)	 $DC_{(max)}$ $DC_{(min)}$	 92 0	 95 0	 98 0	%
SWITCH OUTPUT					
Output Voltage High State (V_{CC} = 7.5 V, I_{Source} = 3.0 A)	V_{OH}	—	(V_{CC} −1.5)	(V_{CC} −1.8)	V
Off-State Leakage (V_{CC} = 40 V, Pin 2 = Gnd)	$I_{sw(off)}$	—	0	100	µA
Current Limit Threshold	$I_{pk(switch)}$	3.3	4.3	5.3	A
Switching Times (V_{CC} = 40 V, I_{pk} = 3.0 A, L = 375 µH, T_A = 25°C) Output Voltage Rise Time Output Voltage Fall Time	 t_r t_f	 — —	 100 50	 200 100	ns
UNDERVOLTAGE LOCKOUT					
Start-Up Threshold (V_{CC} Increasing, T_A = 25°C)	$V_{th(UVLO)}$	5.5	5.9	6.3	V
Hysteresis (V_{CC} Decreasing, T_A = 25°C)	$V_{H(UVLO)}$	0.6	0.9	1.2	V
TOTAL DEVICE					
Power Supply Current (T_A = 25°C) Standby (V_{CC} = 12 V, V_{Comp} < 0.15 V) Operating (V_{CC} = 40 V, Pin 1 = Gnd for maximum duty cycle)	I_{CC}	 — —	 36 31	 100 42	µA mA

NOTES: 1. Maximum package power dissipation limits must be observed to prevent thermal shutdown activation.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34166 T_{high} = + 70°C for MC34166
= − 40°C for MC33166 = + 85°C for MC33166

Figure 1. Voltage Feedback Input Threshold versus Temperature

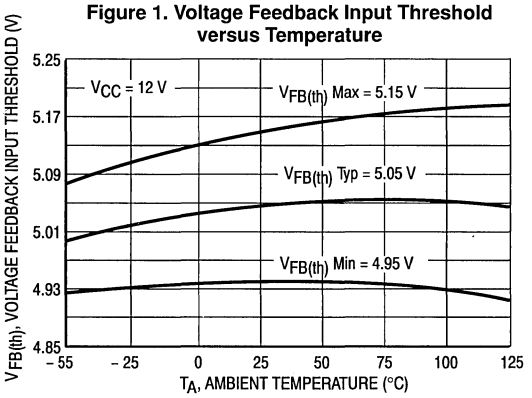


Figure 2. Voltage Feedback Input Bias Current versus Temperature

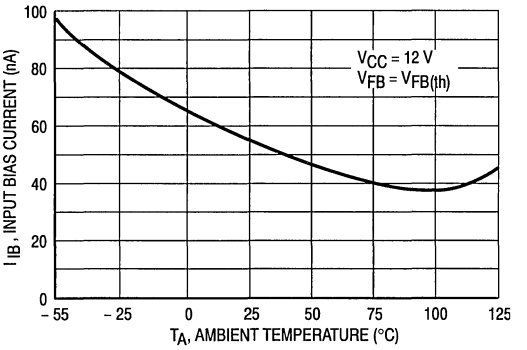


Figure 3. Error Amp Open-Loop Gain and Phase versus Frequency

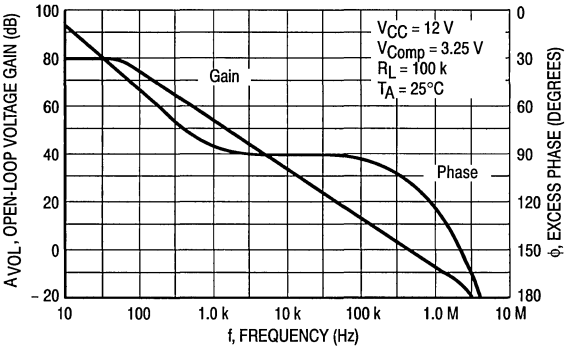


Figure 4. Error Amp Output Saturation versus Sink Current

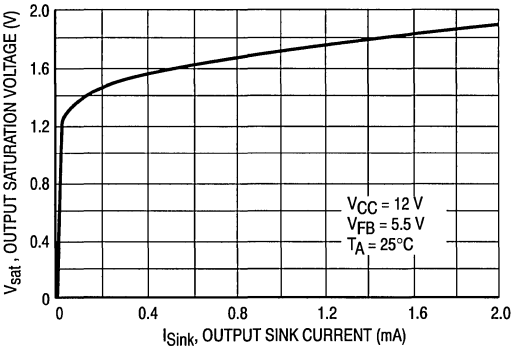


Figure 5. Oscillator Frequency Change versus Temperature

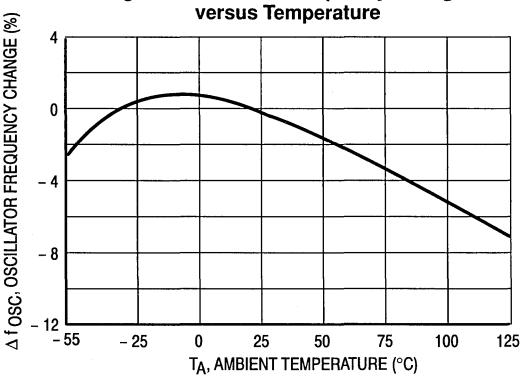


Figure 6. Switch Output Duty Cycle versus Compensation Voltage

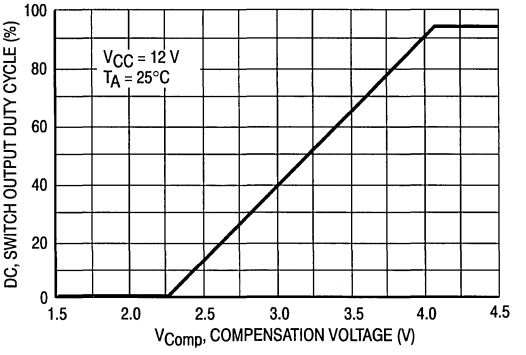


Figure 7. Switch Output Source Saturation versus Source Current

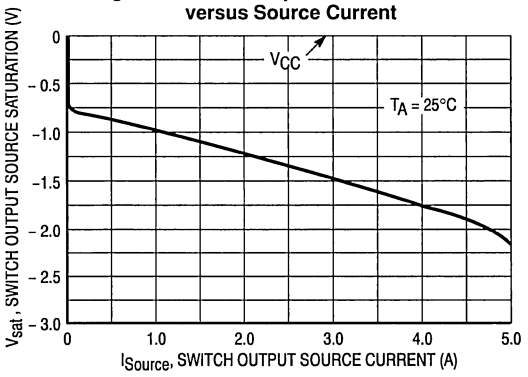


Figure 8. Negative Switch Output Voltage versus Temperature

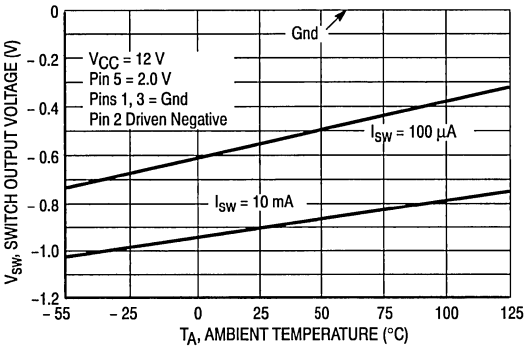


Figure 9. Switch Output Current Limit Threshold versus Temperature

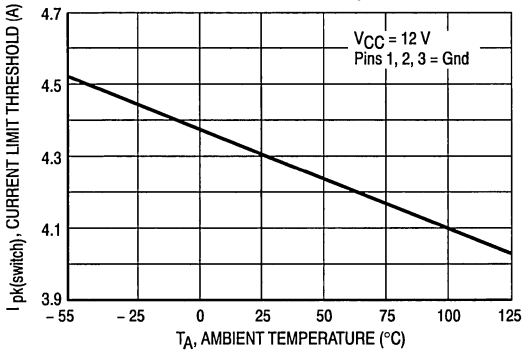


Figure 10. Standby Supply Current versus Supply Voltage

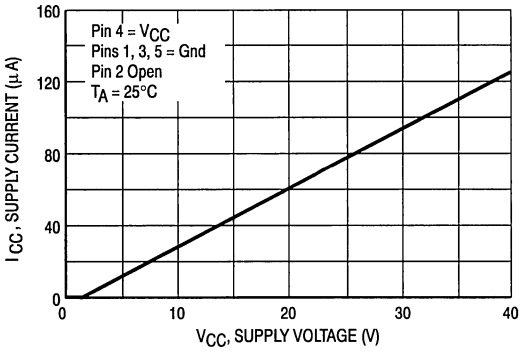


Figure 11. Undervoltage Lockout Thresholds versus Temperature

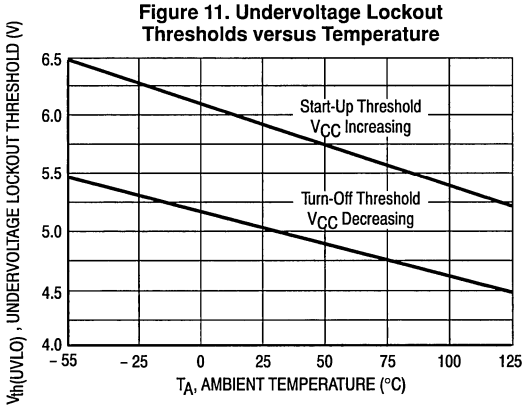


Figure 12. Operating Supply Current versus Supply Voltage

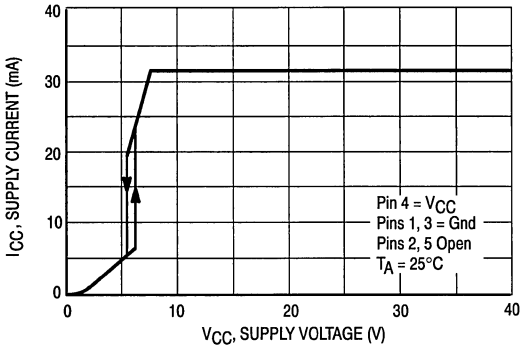


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Figure 13. MC34166 Representative Block Diagram

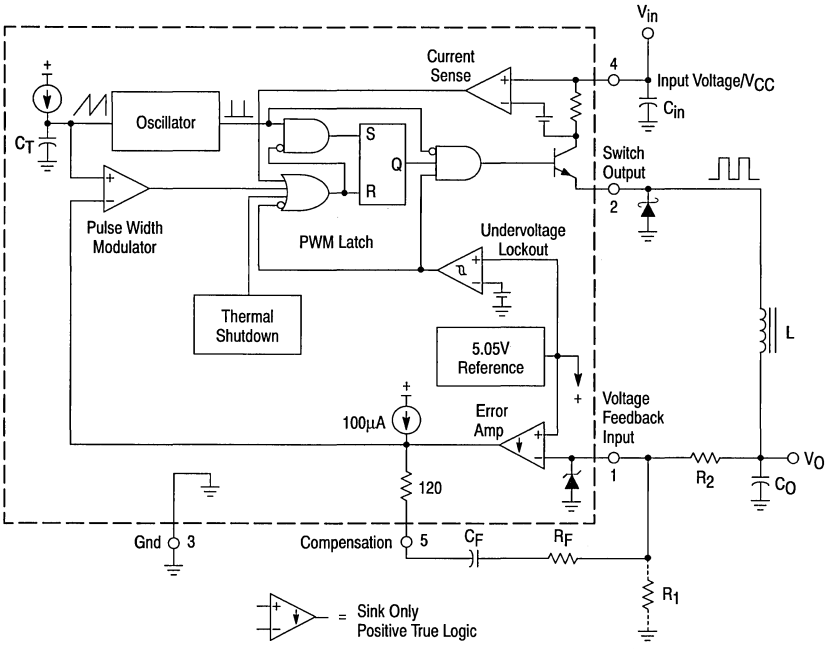
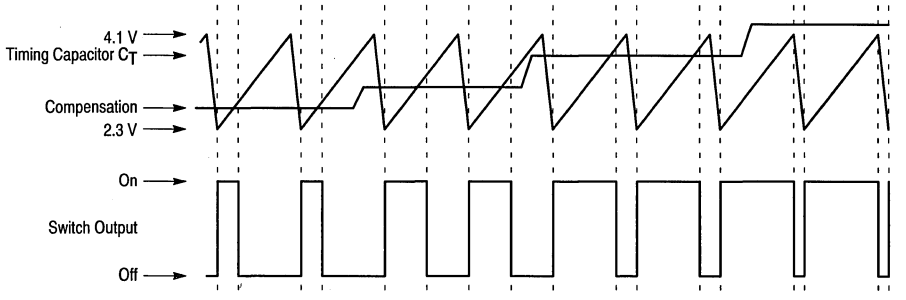


Figure 14. Timing Diagram



INTRODUCTION

The MC34166, MC33166 series are monolithic power switching regulators that are optimized for DC-to-DC converter applications. These devices operate as fixed frequency, voltage mode regulators containing all the active functions required to directly implement step-down and voltage-inverting converters with a minimum number of external components. They can also be used cost effectively in step-up converter applications. Potential markets include automotive, computer, industrial, and cost sensitive consumer products. A description of each section of the device is given below with the representative block diagram shown in Figure 13.

Oscillator

The oscillator frequency is internally programmed to 72 kHz by capacitor C_T and a trimmed current source. The charge to discharge ratio is controlled to yield a 95% maximum duty cycle at the Switch Output. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate high, disabling the output switch transistor. The nominal oscillator peak and valley thresholds are 4.1 V and 2.3 V respectively.

Pulse Width Modulator

The Pulse Width Modulator consists of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied into the inverting input. Output switch conduction is initiated when C_T is discharged to the oscillator valley voltage. As C_T charges to a voltage that exceeds the error amplifier output, the latch resets, terminating output transistor conduction for the duration of the oscillator ramp-up period. This PWM/Latch combination prevents multiple output pulses during a given oscillator clock cycle. Figures 6 and 14 illustrate the switch output duty cycle versus the compensation voltage.

Current Sense

The MC34166 series utilizes cycle-by-cycle current limiting as a means of protecting the output switch transistor from overstress. Each on-cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch transistor current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp-up period.

The collector current is converted to a voltage by an internal trimmed resistor and compared against a reference by the Current Sense comparator. When the current limit threshold is reached, the comparator resets the PWM latch. The current limit threshold is typically set at 4.3 A. Figure 9 illustrates switch output current limit threshold versus temperature.

Error Amplifier and Reference

A high gain Error Amplifier is provided with access to the inverting input and output. This amplifier features a typical DC voltage gain of 80 dB, and a unity gain bandwidth of 600 kHz with 70 degrees of phase margin (Figure 3). The noninverting input is biased to the internal 5.05 V reference and is not pinned out. The reference has an accuracy of ± 2.0% at room temperature. To provide 5.0 V at the load, the reference is programmed 50 mV above 5.0 V to compensate for a 1.0% voltage drop in the cable and connector from the converter output. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input as shown in Figures 13 and 18. The equation for determining the output voltage with the divider network is:

$$V_{out} = 5.05\left(\frac{R_2}{R_1} + 1\right)$$

External loop compensation is required for converter stability. A simple low-pass filter is formed by connecting a resistor (R_2) from the regulated output to the inverting input, and a series resistor-capacitor (R_F, C_F) between Pins 1 and 5. The compensation network component values shown in each of the applications circuits were selected to provide stability over the tested operating conditions. The step-down converter (Figure 18) is the easiest to compensate for stability. The step-up (Figure 20) and voltage-inverting (Figure 22) configurations operate as continuous conduction flyback converters, and are more difficult to compensate. The simplest way to optimize the compensation network is to observe the response of the output voltage to a step load change, while adjusting R_F and C_F for critical damping. The final circuit should be verified for stability under four boundary conditions. These conditions are minimum and maximum input voltages, with minimum and maximum loads.

By clamping the voltage on the error amplifier output (Pin 5) to less than 150 mV, the internal circuitry will be placed into a low power standby mode, reducing the power supply current to 36 μA with a 12 V supply voltage. Figure 10 illustrates the standby supply current versus supply voltage.

The Error Amplifier output has a 100 μA current source pull-up that can be used to implement soft-start. Figure 17 shows the current source charging capacitor C_{SS} through a series diode. The diode disconnects C_{SS} from the feedback loop when the 1.0 M resistor charges it above the operating range of Pin 5.

Switch Output

The output transistor is designed to switch a maximum of 40 V, with a minimum peak collector current of 3.3 A. When configured for step-down or voltage-inverting applications, as in Figures 18 and 22, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn-on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency. Figure 8 shows that by clamping the emitter to 0.5 V, the collector current will be in the range of 100 μA over temperature. A 1N5822 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit is fully functional before the output stage is enabled. The internal 5.05 V reference is monitored by the comparator which enables the output stage when V_{CC} exceeds 5.9 V. To prevent erratic output switching as the threshold is crossed, 0.9 V of hysteresis is provided.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the latch is forced into a 'reset' state, disabling the output switch. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heatsinking.** The MC34166 is contained in a heatsinkable 5-lead TO-220 type package. The tab of the package is common with the center pin (Pin 3) and is normally connected to ground.

DESIGN CONSIDERATIONS

Do not attempt to construct a converter on wire-wrap or plug-in prototype boards. Special care should be taken to separate ground paths from signal currents and ground paths from load currents. All high current loops should be kept as short as possible using heavy copper runs to minimize ringing and radiated EMI. For best operation, a tight component layout is recommended. Capacitors C_{IN}, C_O, and all feedback components should be placed as close to the IC as physically possible. It is also imperative that the Schottky diode connected to the Switch Output be located as close to the IC as possible.

Figure 15. Low Power Standby Circuit

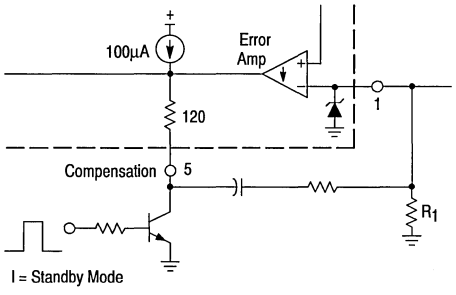
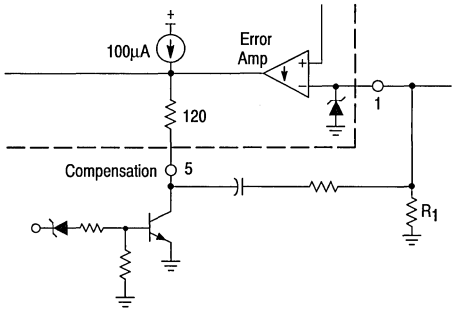
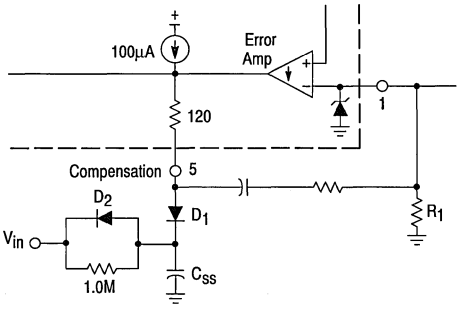


Figure 16. Over Voltage Shutdown Circuit



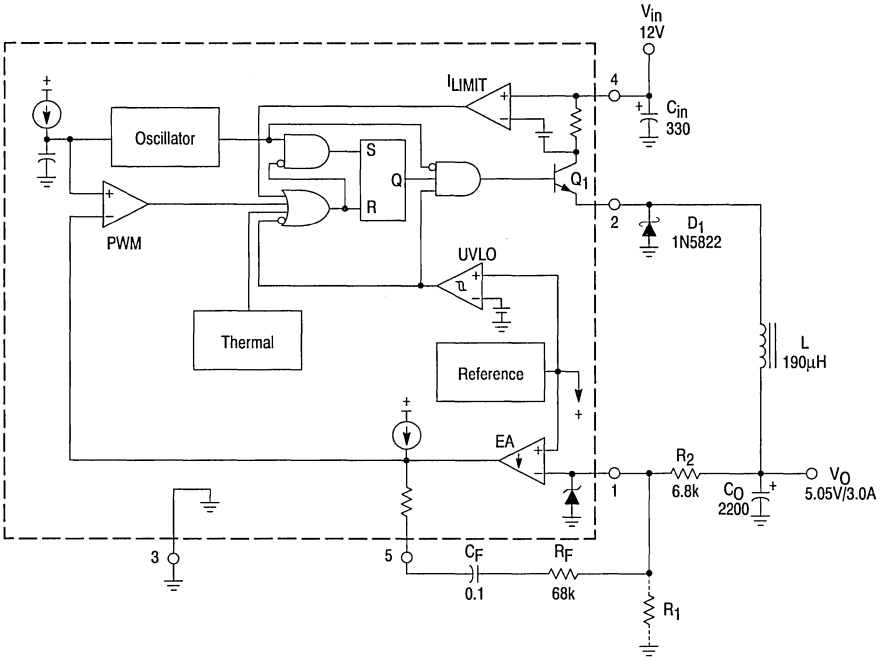
$V_{Shutdown} = V_{Zener} + 0.7$

Figure 17. Soft-Start Circuit



$t_{Soft\text{-}Start} \approx 35{,}000\ C_{SS}$

Figure 18. Step-Down Converter

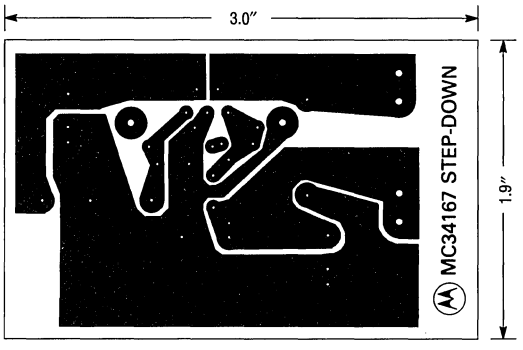


Test	Condition	Results
Line Regulation	V_{in} = 8.0 V to 36 V, I_O = 3.0 A	5.0 mV = ± 0.05%
Load Regulation	V_{in} = 12 V, I_O = 0.25 A to 3.0 A	2.0 mV = ± 0.02%
Output Ripple	V_{in} = 12 V, I_O = 3.0 A	10 mV_{p-p}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	4.3 A
Efficiency	V_{in} = 12 V, I_O = 3.0 A	82.8%

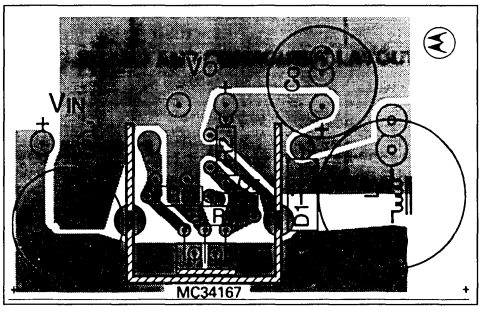
L = Coilcraft M1496-A or ELMACO CHK1050, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.
Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

The Step-Down Converter application is shown in Figure 18. The output switch transistor Q_1 interrupts the input voltage, generating a squarewave at the LC_O filter input. The filter averages the squarewaves, producing a DC output voltage that can be set to any level between V_{in} and V_{ref} by controlling the percent conduction time of Q_1 to that of the total oscillator cycle time. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input.

Figure 19. Step-Down Converter Printed Circuit Board and Component Layout

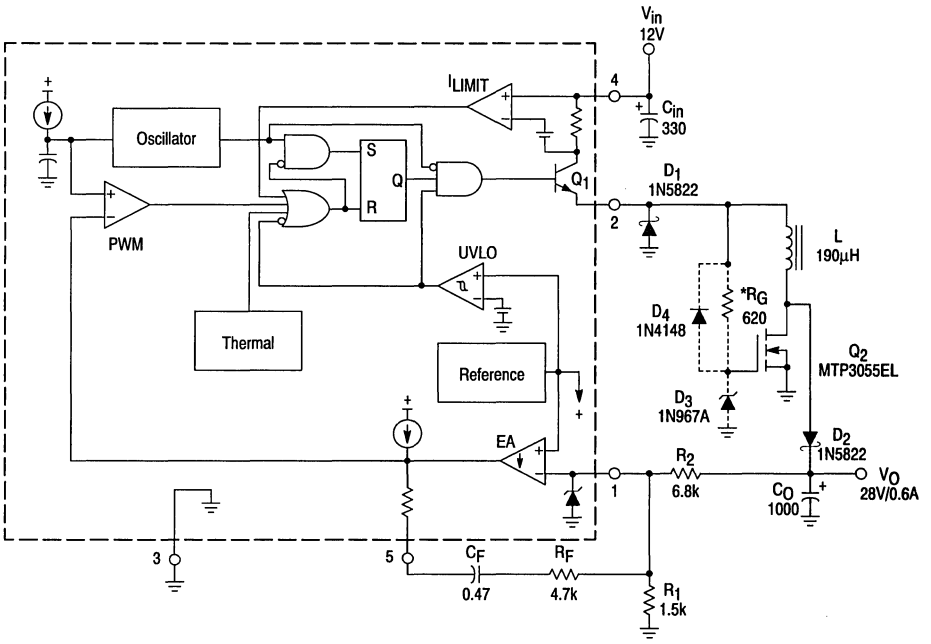


(Bottom View)



(Top View)

Figure 20. Step-Up/Down Converter



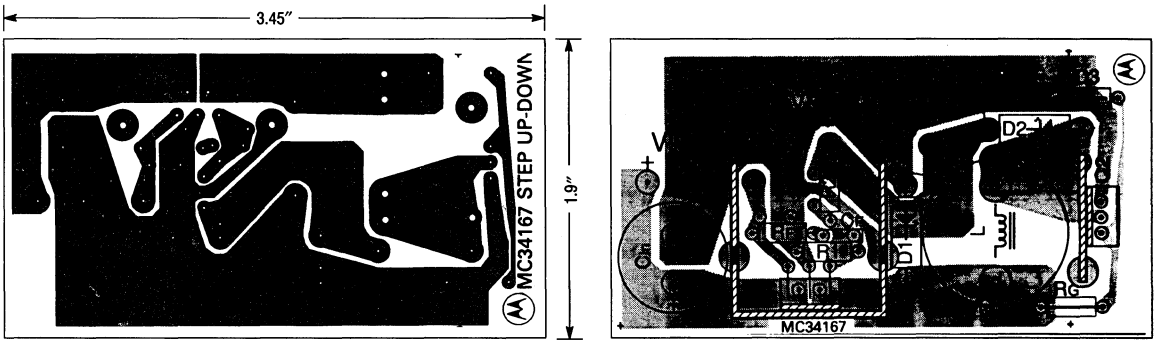
*Gate resistor R_G, zener diode D_3, and diode D_4 are required only when V_{in} is greater than 20 V.

Test	Condition	Results
Line Regulation	V_{in} = 8.0 V to 24 V, I_O = 0.6 A	23 mV = ± 0.41%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 0.6 A	3.0 mV = ± 0.005%
Output Ripple	V_{in} = 12 V, I_O = 0.6 A	100 mV_{p-p}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	4.0 A
Efficiency	V_{in} = 12 V, I_O = 0.6 A	82.8%

L = Coilcraft M1496-A or ELMACO CHK1050, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.
Heatsink = AAVID Engineering Inc.
MC34166: 5903B, or 5930B
MTP3055EL: 5925B

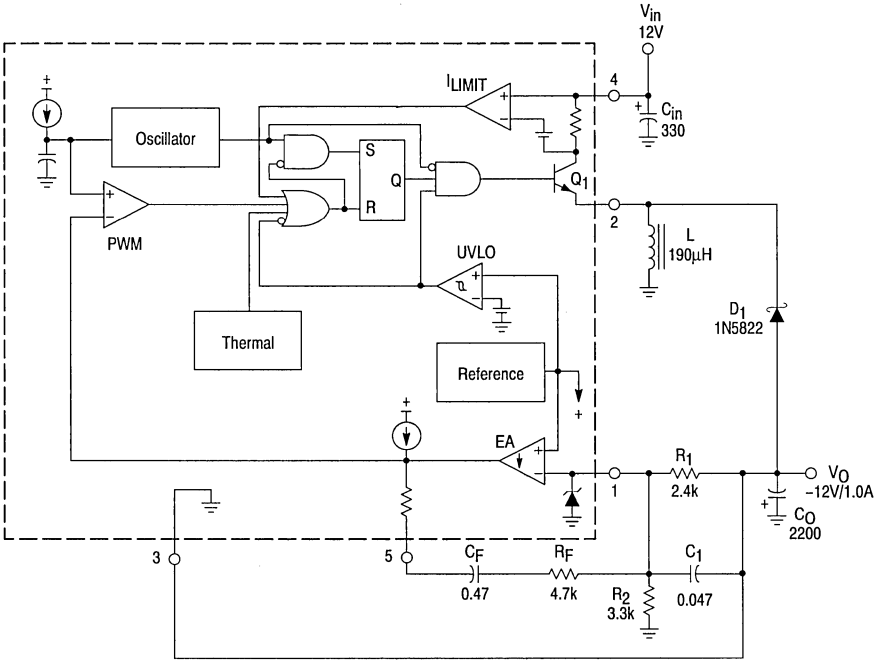
Figure 20 shows that the MC34166 can be configured as a step-up/down converter with the addition of an external power MOSFET. Energy is stored in the inductor during the on-time of transistors Q_1 and Q_2. During the off-time, the energy is transferred, with respect to ground, to the output filter capacitor and load. This circuit configuration has two significant advantages over the basic step-up converter circuit. The first advantage is that output short-circuit protection is provided by the MC34166, since Q_1 is directly in series with V_{in} and the load. Second, the output voltage can be programmed to be less than V_{in}. Notice that during the off-time, the inductor forward biases diodes D_1 and D_2, transferring its energy with respect to ground rather than with respect to V_{in}. When operating with V_{in} greater than 20 V, a gate protection network is required for the MOSFET. The network consists of components R_g, D_3, and D_4.

Figure 21. Step-Up/Down Converter Printed Circuit Board and Component Layout



(Bottom View) (Top View)

Figure 22. Voltage-Inverting Converter

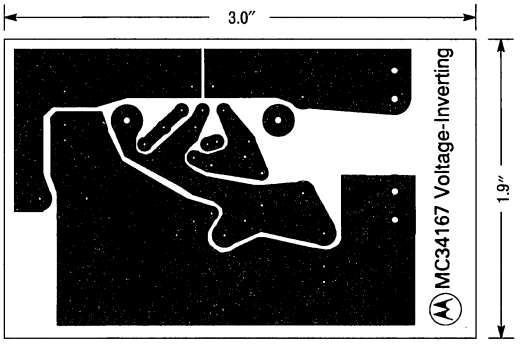


Test	Condition	Results
Line Regulation	V_{in} = 8.0 V to 24 V, I_O = 1.0 A	3.0 mV = ± 0.01%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 1.0 A	4.0 mV = ± 0.017%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	80 mV_{p-p}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	3.74 A
Efficiency	V_{in} = 12 V, I_O = 1.0 A	81.2%

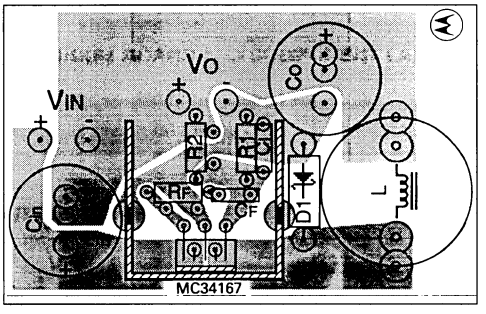
L = Coilcraft M1496-A or ELMACO CHK1050, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.
Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Two potential problems arise when designing the standard voltage-inverting converter with the MC34166. First, the Switch Output emitter is limited to –1.5 V with respect to the ground pin and second, the Error Amplifier's noninverting input is internally committed to the reference and is not pinned out. Both of these problems are resolved by connecting the IC ground pin to the converter's negative output as shown in Figure 22. This keeps the emitter of Q_1 positive with respect to the ground pin and has the effect of reversing the Error Amplifier inputs. Note that the voltage drop across R_1 is equal to 5.05 V when the output is in regulation.

Figure 23. Voltage-Inverting Converter Printed Circuit Board and Component Layout

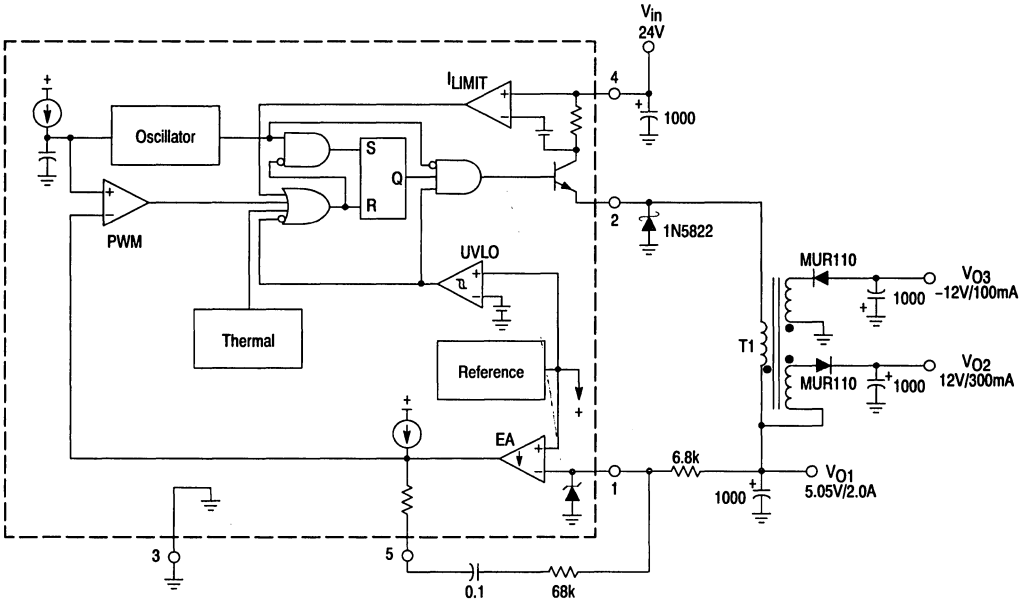


(Bottom View)



(Top View)

Figure 24. Triple Output Converter



Test		Condition	Results
Line Regulation	5.0 V 12 V −12 V	V_{in} = 15 V to 30 V, I_{O1} = 2.0 A, I_{O2} = 300 mA, I_{O3} = 100 mA	4.0 mV = ± 0.04% 450 mV = ±1.9% 350 mV = ±1.5%
Load Regulation	5.0 V 12 V −12 V	V_{in} = 24 V, I_{O1} = 500 mA to 2.0 A, I_{O2} = 300 mA, I_{O3} = 100 mA V_{in} = 24 V, I_{O1} = 2.0 A, I_{O2} = 100 mA to 300 mA, I_{O3} = 100 mA V_{in} = 24 V, I_{O1} = 2.0 A, I_{O2} = 300 mA, I_{O3} = 30 mA to 100 mA	2.0 mV = ± 0.02% 420 mV = ±1.7% 310 mV = ±1.3%
Output Ripple	5.0 V 12 V −12 V	V_{in} = 24 V, I_{O1} = 2.0 A, I_{O2} = 300 mA, I_{O3} = 100 mA	50 mV_{p-p} 25 mV_{p-p} 10 mV_{p-p}
Short Circuit Current	5.0 V 12 V −12 V	V_{in} = 24 V, R_L = 0.1 Ω	4.3 A 1.83 A 1.47 A
Efficiency	TOTAL	V_{in} = 24 V, I_{O1} = 2.0 A, I_{O2} = 300 mA, I_{O3} = 100 mA	83.3%

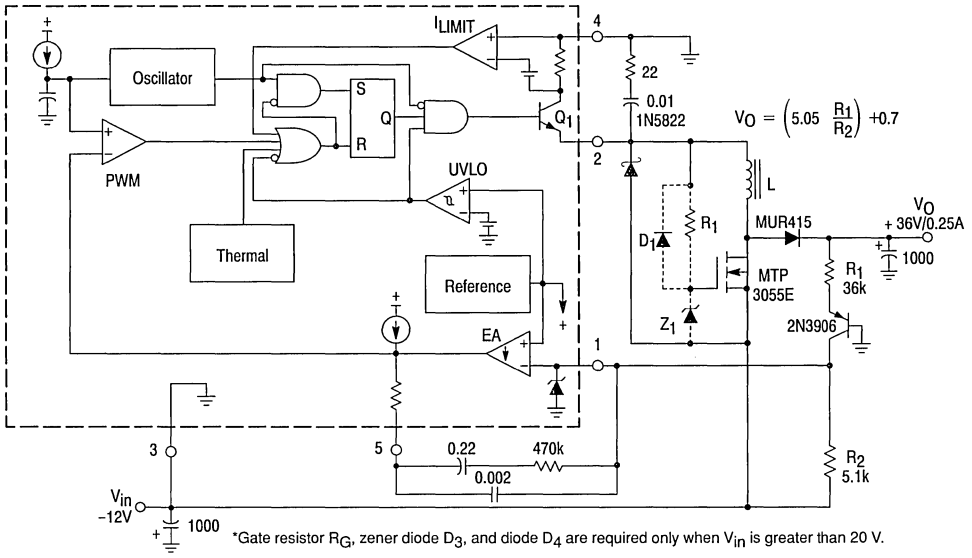
T1 = Primary: Coilcraft M1496-A or ELMACO CHK1050, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.
Secondary: V_{O2} — 65 turns of #26 AWG
V_{O3} — 96 turns of #28 AWG
Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Multiple auxiliary outputs can easily be derived by winding secondaries on the main output inductor to form a transformer. The secondaries must be connected so that the energy is delivered to the auxiliary outputs when the Switch Output turns off. During the off-time, the voltage across the primary winding is regulated by the feedback loop, yielding a constant Volts/Turn ratio. The number of turns for any given secondary voltage can be calculated by the following equation:

$$\#\,TURNS_{(SEC)} = \frac{V_{O(SEC)} + V_{F(SEC)}}{\left(\frac{V_{O(PRI)} + V_{F(PRI)}}{\#TURNS_{(PRI)}}\right)}$$

Note that the 12 V winding is stacked on top of the 5.0 V output. This reduced the number of secondary turns and improves lead regulation. For best auxiliary regulation, the auxiliary outputs should be less than 33% of the total output power.

Figure 25. Negative Input/Positive Output Regulator

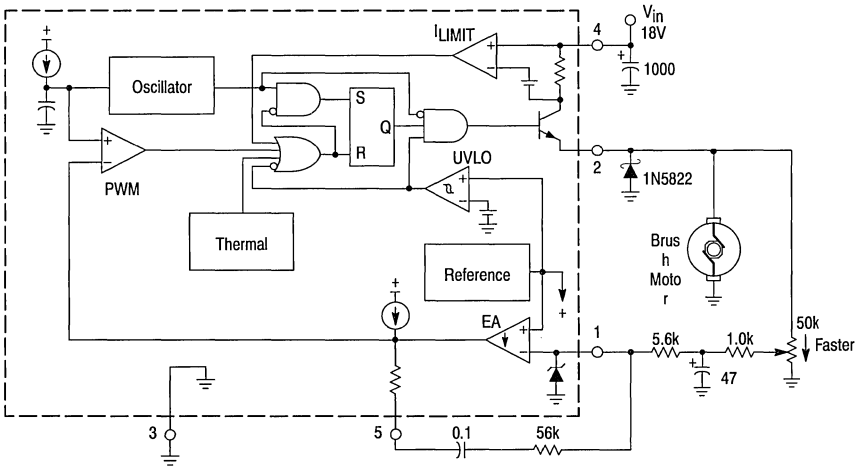


*Gate resistor R_G, zener diode D_3, and diode D_4 are required only when V_{in} is greater than 20 V.

Test	Condition	Results
Line Regulation	V_{in} = –10 V to – 20 V, I_O = 0.25 A	250 mV = ± 0.35%
Load Regulation	V_{in} = –12 V, I_O = 0.025 A to 0.25 A	790 mV = ±1.19%
Output Ripple	V_{in} = –12 V, I_O = 0.25 A	80 mV_{p-p}
Efficiency	V_{in} = –12 V, I_O = 0.25 A	79.2%

L = Coilcraft M1496-A or ELMACO CHK1050, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.
Heatsink = AAVID Engineering Inc. 5903B or 5930B

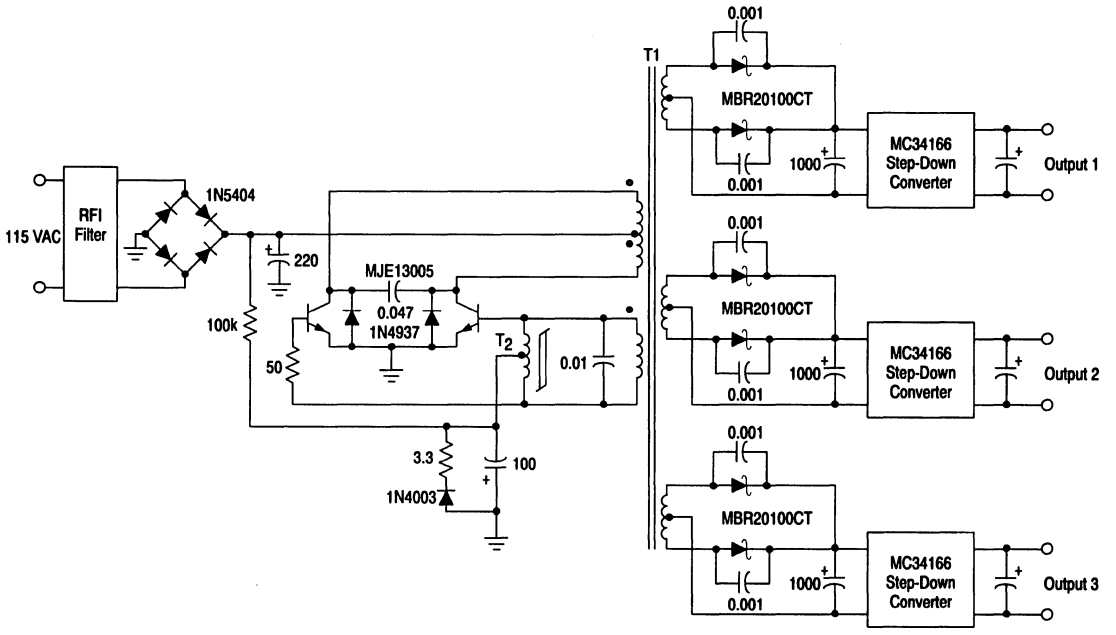
Figure 26. Variable Motor Speed Control with EMF Feedback Sensing



Test	Condition	Results
Low Speed Line Regulation	V_{in} = 12 V to 24 V	1760 RPM ±1%
High Speed Line Regulation	V_{in} = 12 V to 24 V	3260 RPM ± 6%

3

Figure 27. Off-Line Preconverter



T_1 = Core and Bobbin — Coilcraft PT3595
Primary — 104 turns #26 AWG
Base Drive — 3 turns #26 AWG
Secondaries — 16 turns #16 AWG
Total Gap — 0.002″

T_2 = Core — TDK T6 x 1.5 x 3 H5C2
14 turns center tapped #30 AWG

Heatsink = AAVID Engineering Inc.
MC34166 and MJE13005 — 5903B
MBR20100CT — 5925B

The MC34166 can be used cost effectively in off-line applications even though it is limited to a maximum input voltage of 40 V. Figure 27 shows a simple and efficient method for converting the AC line voltage down to 24 V. This preconverter has a total power rating of 125 W with a conversion efficiency of 90%. Transformer T_1 provides output isolation from the AC line and isolation between each of the secondaries. The circuit self-oscillates at 50 kHz and is controlled by the saturation characteristics of T_2. Multiple MC34166 post regulators can be used to provide accurate independently regulated outputs for a distributed power system.

MC34167
MC33167

Advance Information

Power Switching Regulator

POWER SWITCHING REGULATOR

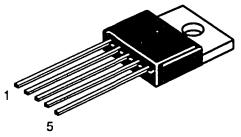
SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC34167, MC33167 series are high performance fixed frequency power switching regulators that contain the primary functions required for DC-to-DC converters. This series was specifically designed to be incorporated in step-down and voltage-inverting configurations with a minimum number of external components and can also be used cost effectively in step-up applications.

These devices consist of an internal temperature compensated reference, fixed frequency oscillator with on-chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch.

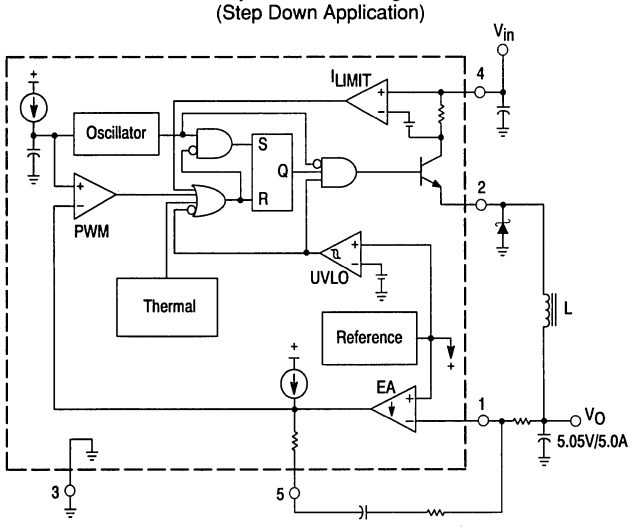
Protective features consist of cycle-by-cycle current limiting, undervoltage lockout, and thermal shutdown. Also included is a low power standby mode that reduces power supply current to 36 μA.

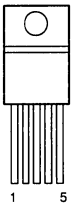
- Output Switch Current in Excess of 5.0 A
- Fixed Frequency Oscillator (72 kHz) with On-Chip Timing
- Provides 5.05 V Output Without External Resistor Divider
- Precision 2.0% Reference
- 0% to 95% Output Duty Cycle
- Cycle-by-Cycle Current Limiting
- Undervoltage Lockout with Hysteresis
- Internal Thermal Shutdown
- Operation from 7.5 V to 40 V
- Standby Mode Reduces Power Supply Current to 36 μA
- Economical Five Lead TO-220 Package



T SUFFIX
PLASTIC PACKAGE
CASE 314D

Simplified Block Diagram
(Step Down Application)





PIN CONNECTIONS

Pin 1. Voltage Feedback Input
2. Switch Output
3. Ground
4. Input Voltage/V_{CC}
5. Compensation/Standby

(Heatsink surface connected to Pin 3)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34167T	0° to + 70°C	Plastic Power
MC33167T	– 40° to + 85°C	Plastic Power

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	40	V
Switch Output Voltage Range	$V_{O(switch)}$	− 2.0 to + V_{in}	V
Voltage Feedback and Compensation Input Voltage Range	V_{FB}, V_{Comp}	−1.0 to + 7.0	V
Power Dissipation and Thermal Characteristics (Note 1) Maximum Power Dissipation @ T_C = 70°C Thermal Resistance Junction to Case (Pin 3) Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction-to-Air	 P_D θ_{JC} P_D θ_{JA}	 34.7 2.3 1.9 65	 W °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34167 MC33167	T_A	 0 to + 70 − 40 to + 85	°C
Storage Temperature Range	T_{stg}	− 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 2, 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (V_{CC} = 7.5 V to 40 V) T_A = 25°C T_A = T_{low} to T_{high}	f_{OSC}	 65 62	 72 —	 79 81	kHz
ERROR AMPLIFIER					
Voltage Feedback Input Threshold T_A = 25°C T_A = T_{low} to T_{high}	$V_{FB(th)}$	 4.95 4.85	 5.05 —	 5.15 5.20	V
Line Regulation (V_{CC} = 7.5 V to 40 V, T_A = 25°C)	Reg_{line}	—	0.03	0.078	%/V
Input Bias Current (V_{FB} = $V_{FB(th)}$ + 0.15 V)	I_{IB}	—	0.15	1.0	µA
Power Supply Rejection Ratio (V_{CC} = 10 V to 20 V)	PSRR	60	80	—	dB
Output Voltage Swing High State (I_{Source} = 75 µA, V_{FB} = 4.7 V) Low State (I_{Sink} = 0.4 mA, V_{FB} = 5.5 V)	 V_{OH} V_{OL}	 4.2 —	 4.9 1.6	 — 1.9	V
PWM COMPARATOR					
Duty Cycle (V_{CC} = 20 V) Maximum (V_{FB} = 0 V) Minimum (V_{Comp} = 1.9 V)	 $DC_{(max)}$ $DC_{(min)}$	 92 0	 95 0	 98 0	%
SWITCH OUTPUT					
Output Voltage Source Saturation (V_{CC} = 7.5 V, I_{Source} = 5.0 A)	V_{sat}	—	(V_{CC} −1.5)	(V_{CC} −1.8)	V
Off-State Leakage (V_{CC} = 40 V, Pin 2 = Gnd)	$I_{sw(off)}$	—	0	100	µA
Current Limit Threshold (V_{CC} = 7.5 V)	$I_{pk(switch)}$	5.5	6.5	7.5	A
Switching Times (V_{CC} = 40 V, I_{pk} = 5.0 A, L = 225 µH, T_A = 25°C) Output Voltage Rise Time Output Voltage Fall Time	 t_r t_f	 — —	 100 50	 200 100	ns
UNDERVOLTAGE LOCKOUT					
Start-Up Threshold (V_{CC} Increasing, T_A = 25°C)	$V_{th(UVLO)}$	5.5	5.9	6.3	V
Hysteresis (V_{CC} Decreasing, T_A = 25°C)	$V_{H(UVLO)}$	0.6	0.9	1.2	V
TOTAL DEVICE					
Power Supply Current (T_A = 25°C) Standby (V_{CC} = 12 V, V_{Comp} < 0.15 V) Operating (V_{CC} = 40 V, Pin 1 = Gnd for maximum duty cycle)	I_{CC}	 — —	 36 40	 100 53	 µA mA

NOTES: 1. Maximum package power dissipation limits must be observed to prevent thermal shutdown activation.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34167 T_{high} = + 70°C for MC34167
= − 40°C for MC33167 = + 85°C for MC33167

Figure 1. Voltage Feedback Input Threshold versus Temperature

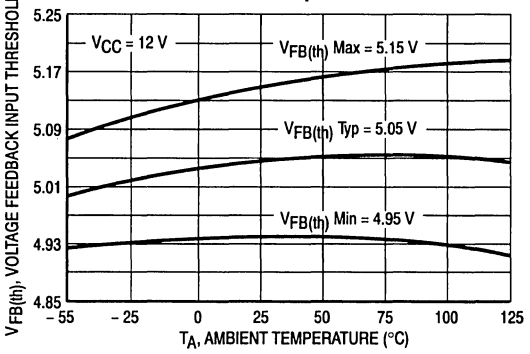


Figure 2. Voltage Feedback Input Bias Current versus Temperature

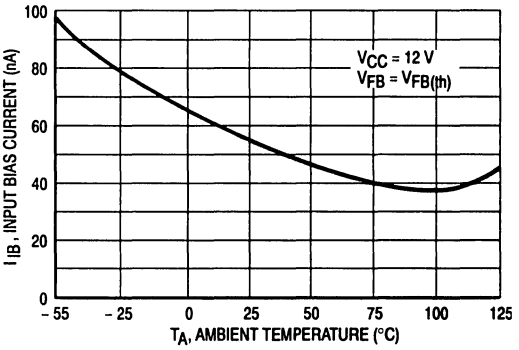


Figure 3. Error Amp Open-Loop Gain and Phase versus Frequency

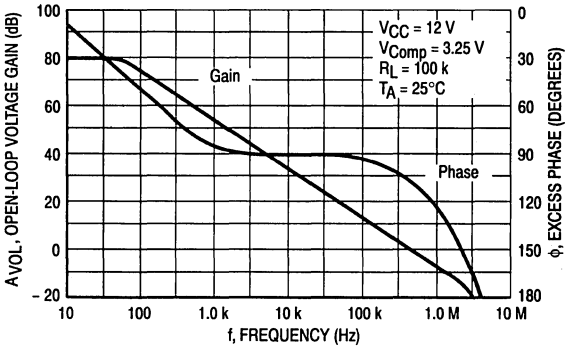


Figure 4. Error Amp Output Saturation versus Sink Current

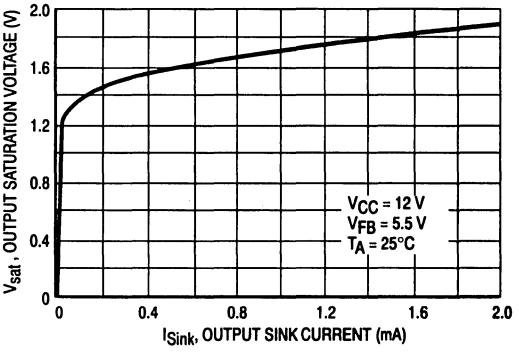


Figure 5. Oscillator Frequency Change versus Temperature

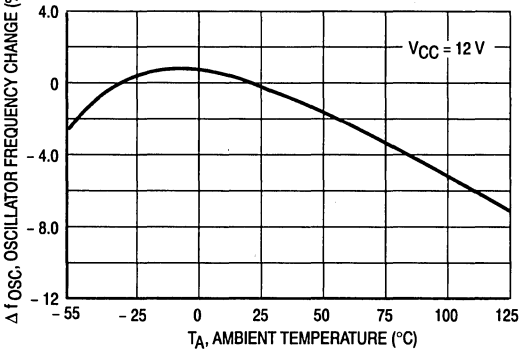


Figure 6. Switch Output Duty Cycle versus Compensation Voltage

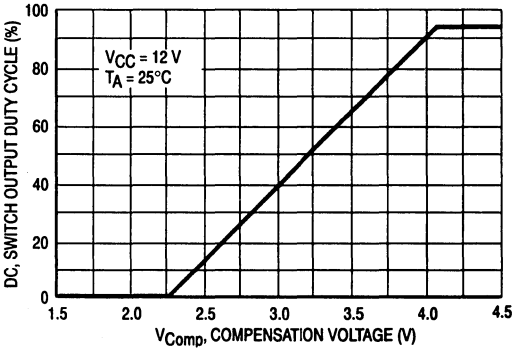


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Figure 7. Switch Output Source Saturation versus Source Current

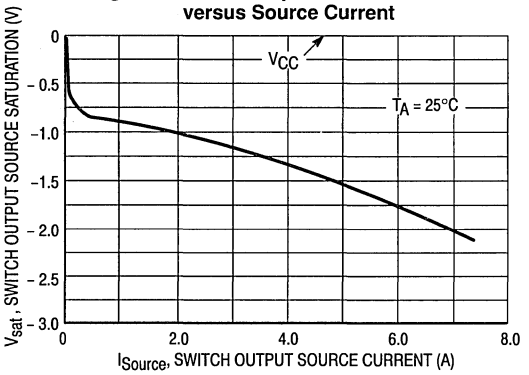


Figure 8. Negative Switch Output Voltage versus Temperature

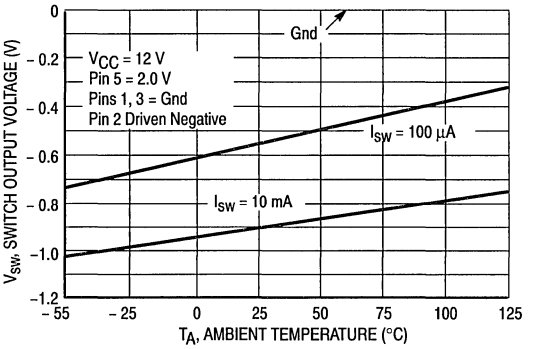


Figure 9. Switch Output Current Limit Threshold versus Temperature

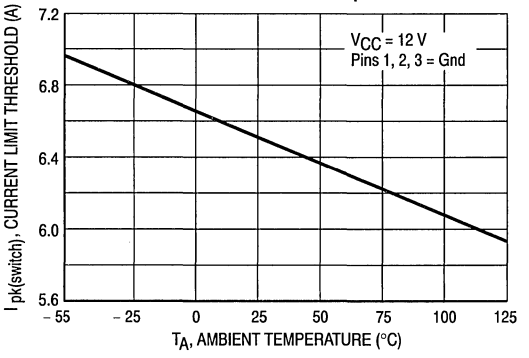


Figure 10. Standby Supply Current versus Supply Voltage

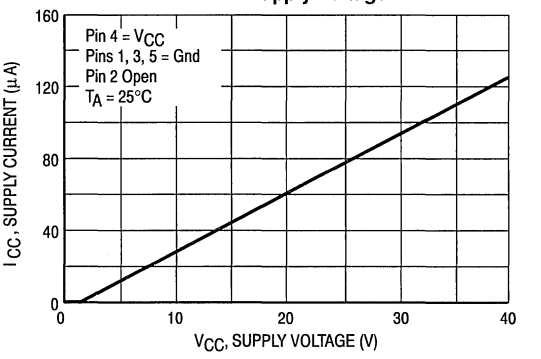


Figure 11. Undervoltage Lockout Thresholds versus Temperature

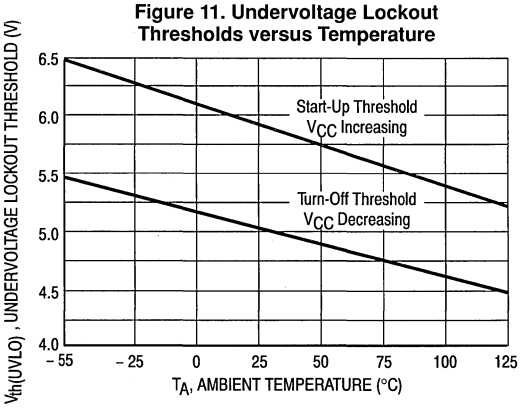


Figure 12. Operating Supply Current versus Supply Voltage

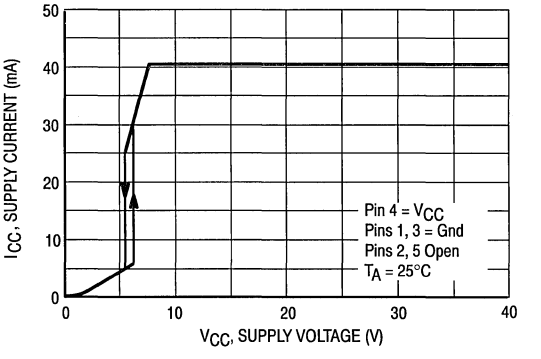


Figure 13. MC34167 Representative Block Diagram

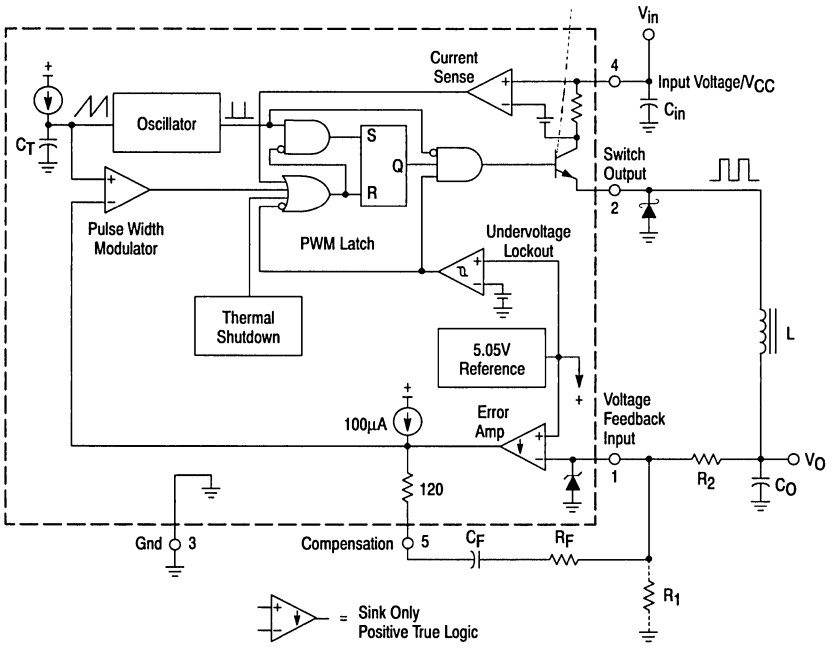
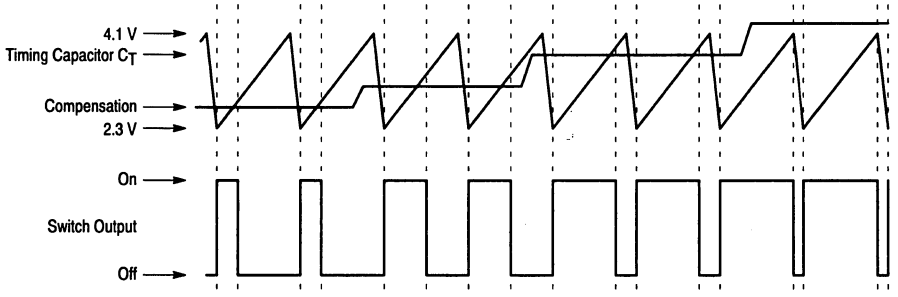


Figure 14. Timing Diagram



INTRODUCTION

The MC34167, MC33167 series are monolithic power switching regulators that are optimized for DC-to-DC converter applications. These devices operate as fixed frequency, voltage mode regulators containing all the active functions required to directly implement step-down and voltage-inverting converters with a minimum number of external components. They can also be used cost effectively in step-up converter applications. Potential markets include automotive, computer, industrial, and cost sensitive consumer products. A description of each section of the device is given below with the representative block diagram shown in Figure 13.

Oscillator

The oscillator frequency is internally programmed to 72 kHz by capacitor C_T and a trimmed current source. The charge to discharge ratio is controlled to yield a 95% maximum duty cycle at the Switch Output. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate high, disabling the output switch transistor. The nominal oscillator peak and valley thresholds are 4.1 V and 2.3 V respectively.

Pulse Width Modulator

The Pulse Width Modulator consists of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied into the inverting input. Output switch conduction is initiated when C_T is discharged to the oscillator valley voltage. As C_T charges to a voltage that exceeds the error amplifier output, the latch resets, terminating output transistor conduction for the duration of the oscillator ramp-up period. This PWM/Latch combination prevents multiple output pulses during a given oscillator clock cycle. Figures 6 and 14 illustrate the switch output duty cycle versus the compensation voltage.

Current Sense

The MC34167 series utilizes cycle-by-cycle current limiting as a means of protecting the output switch transistor from overstress. Each on-cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch transistor current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp-up period.

The collector current is converted to a voltage by an internal trimmed resistor and compared against a reference by the Current Sense comparator. When the current limit threshold is reached, the comparator resets the PWM latch. The current limit threshold is typically set at 6.5 A. Figure 9 illustrates switch output current limit threshold versus temperature.

Error Amplifier and Reference

A high gain Error Amplifier is provided with access to the inverting input and output. This amplifier features a typical DC voltage gain of 80 dB, and a unity gain bandwidth of 600 kHz with 70 degrees of phase margin (Figure 3). The noninverting input is biased to the internal 5.05 V reference and is not pinned out. The reference has an accuracy of ± 2.0% at room temperature. To provide 5.0 V at the load, the reference is programmed 50 mV above 5.0 V to compensate for a 1.0% voltage drop in the cable and connector from the converter output. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input as shown in Figures 13 and 18. The equation for determining the output voltage with the divider network is:

$$V_{out} = 5.05\left(\frac{R_2}{R_1} + 1\right)$$

External loop compensation is required for converter stability. A simple low-pass filter is formed by connecting a resistor (R_2) from the regulated output to the inverting input, and a series resistor-capacitor (R_F, C_F) between Pins 1 and 5. The compensation network component values shown in each of the applications circuits were selected to provide stability over the tested operating conditions. The step-down converter (Figure 18) is the easiest to compensate for stability. The step-up (Figure 20) and voltage-inverting (Figure 22) configurations operate as continuous conduction flyback converters, and are more difficult to compensate. The simplest way to optimize the compensation network is to observe the response of the output voltage to a step load change, while adjusting R_F and C_F for critical damping. The final circuit should be verified for stability under four boundary conditions. These conditions are minimum and maximum input voltages, with minimum and maximum loads.

By clamping the voltage on the error amplifier output (Pin 5) to less than 150 mV, the internal circuitry will be placed into a low power standby mode, reducing the power supply current to 36 μA with a 12 V supply voltage. Figure 10 illustrates the standby supply current versus supply voltage.

The Error Amplifier output has a 100 μA current source pull-up that can be used to implement soft-start. Figure 17 shows the current source charging capacitor C_{SS} through a series diode. The diode disconnects C_{SS} from the feedback loop when the 1.0 M resistor charges it above the operating range of Pin 5.

Switch Output

The output transistor is designed to switch a maximum of 40 V, with a minimum peak collector current of 5.5 A. When configured for step-down or voltage-inverting applications, as in Figures 18 and 22, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn-on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency. Figure 8 shows that by clamping the emitter to 0.5 V, the collector current will be in the range of 100 μA over temperature. A 1N5825 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit is fully functional before the output stage is enabled. The internal reference voltage is monitored by the comparator which enables the output stage when V_{CC} exceeds 5.9 V. To prevent erratic output switching as the threshold is crossed, 0.9 V of hysteresis is provided.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the latch is forced into a 'reset' state, disabling the output switch. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heatsinking.** The MC34167 is contained in a 5-lead TO-220 type package. The tab of the package is common with the center pin (Pin 3) and is normally connected to ground.

DESIGN CONSIDERATIONS

Do not attempt to construct a converter on wire-wrap or plug-in prototype boards. Special care should be taken to separate ground paths from signal currents and ground paths from load currents. All high current loops should be kept as short as possible using heavy copper runs to minimize ringing and radiated EMI. For best operation, a tight component layout is recommended. Capacitors C_{in}, C_O, and all feedback components should be placed as close to the IC as physically possible. It is also imperative that the Schottky diode connected to the Switch Output be located as close to the IC as possible.

Figure 15. Low Power Standby Circuit

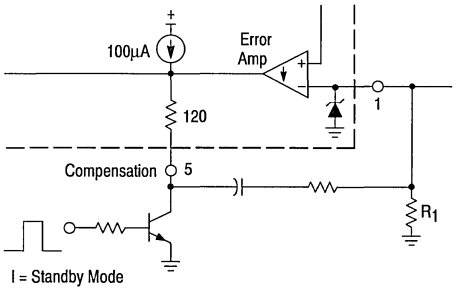
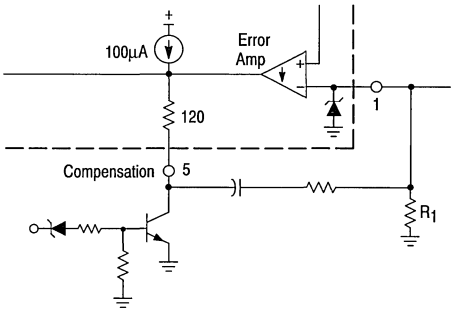
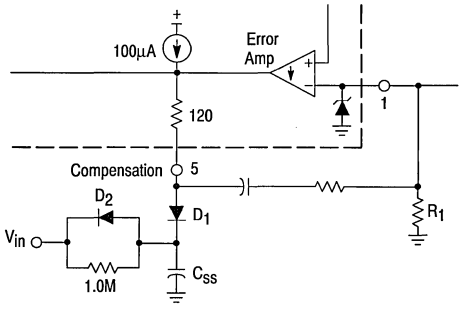


Figure 16. Over Voltage Shutdown Circuit



$V_{Shutdown} = V_{Zener} + 0.7$

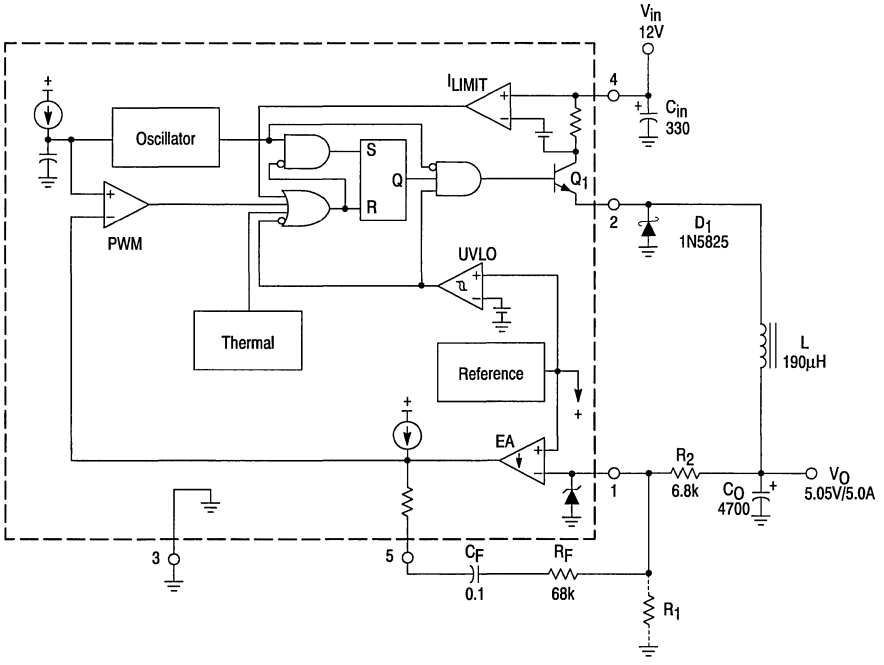
Figure 17. Soft-Start Circuit



$t_{Soft\text{-}Start} \approx 35{,}000\ C_{ss}$

3

Figure 18. Step-Down Converter

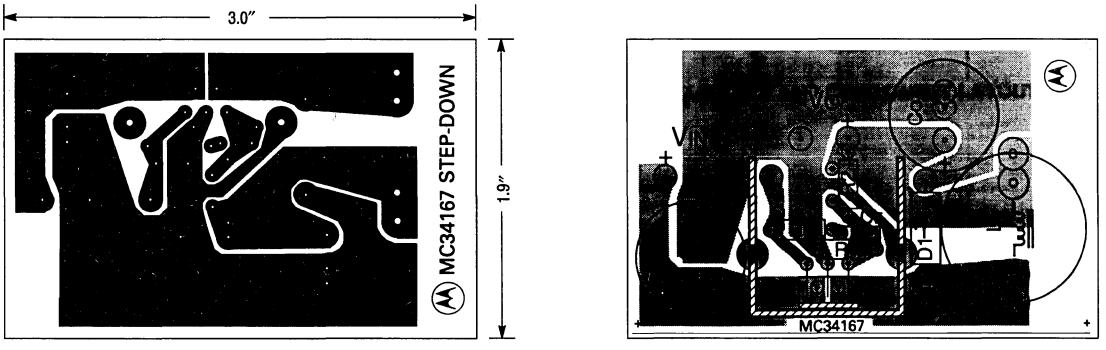


Test	Condition	Results
Line Regulation	V_{in} = 10 V to 36 V, I_O = 5.0 A	4.0 mV = ± 0.039%
Load Regulation	V_{in} = 12 V, I_O = 0.25 A to 5.0 A	1.0 mV = ± 0.01%
Output Ripple	V_{in} = 12 V, I_O = 5.0 A	20 mV_{p-p}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	6.5 A
Efficiency	V_{in} = 12 V, I_O = 5.0 A V_{in} = 24 V, I_O = 5.0 A	78.9% 82.6%

L = Coilcraft M1496-A or ELMACO CHK1050, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.
Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

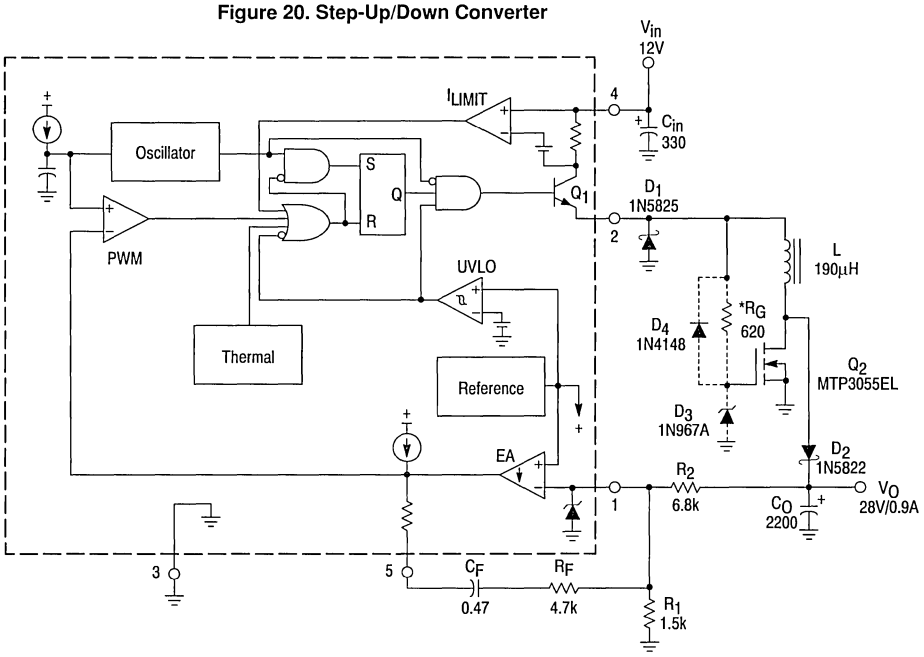
The Step-Down Converter application is shown in Figure 18. The output switch transistor Q_1 interrupts the input voltage, generating a squarewave at the LC_O filter input. The filter averages the squarewaves, producing a DC output voltage that can be set to any level between V_{in} and V_{ref} by controlling the percent conduction time of Q_1 to that of the total oscillator cycle time. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input.

Figure 19. Step-Down Converter Printed Circuit Board and Component Layout



(Bottom View) (Top View)

Figure 20. Step-Up/Down Converter



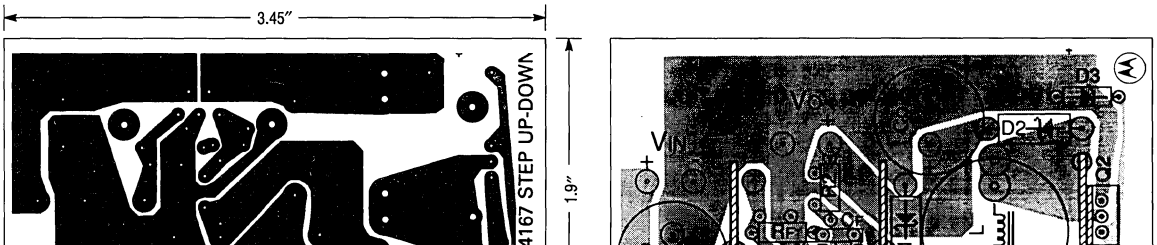
*Gate resistor R_G, zener diode D_3, and diode D_4 are required only when V_{in} is greater than 20 V.

Test	Condition	Results
Line Regulation	V_{in} = 10 V to 24 V, I_O = 0.9 A	10 mV = ± 0.017%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 0.9 A	30 mV = ± 0.053%
Output Ripple	V_{in} = 12 V, I_O = 0.9 A	140 mV_{p-p}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	6.0 A
Efficiency	V_{in} = 12 V, I_O = 0.9 A V_{in} = 24 V, I_O = 0.9 A	80.1% 87.8%

L = Coilcraft M1496-A or ELMACO CHK1050, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.
Heatsink = AAVID Engineering Inc.
MC34167: 5903B, or 5930B
MTP3055EL: 5925B

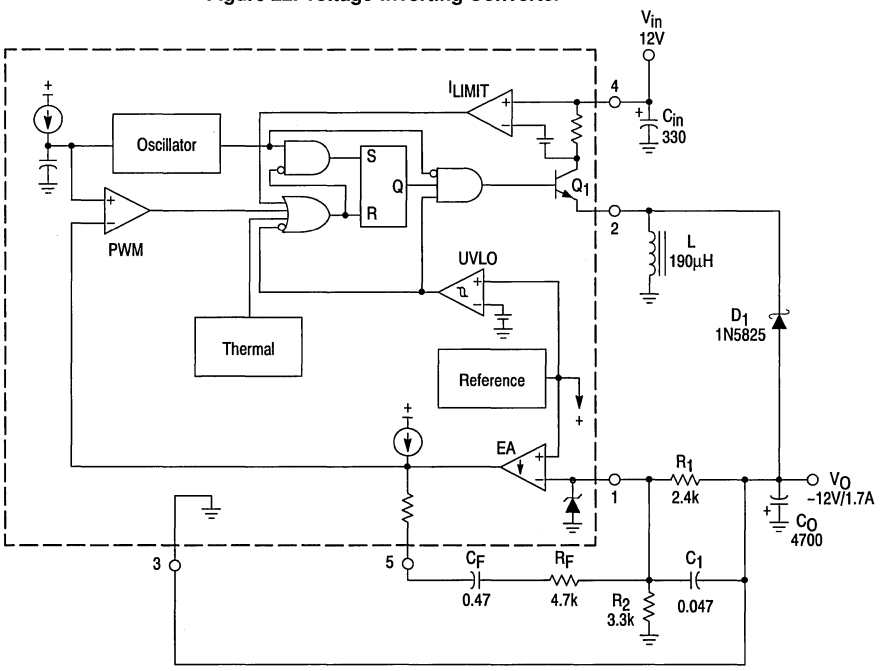
Figure 20 shows that the MC34167 can be configured as a step-up/down converter with the addition of an external power MOSFET. Energy is stored in the inductor during the on-time of transistors Q_1 and Q_2. During the off-time, the energy is transferred, with respect to ground, to the output filter capacitor and load. This circuit configuration has two significant advantages over the basic step-up converter circuit. The first advantage is that output short circuit protection is provided by the MC34167, since Q_1 is directly in series with V_{in} and the load. Second, the output voltage can be programmed to be less than V_{in}. Notice that during the off-time, the inductor forward biases diodes D_1 and D_2, transferring its energy with respect to ground rather than with respect to V_{in}. When operating with V_{in} greater than 20 V, a gate protection network is required for the MOSFET. The network consists of components R_g, D_3, and D_4.

Figure 21. Step-Up/Down Converter Printed Circuit Board and Component Layout



(Bottom View) (Top View)

Figure 22. Voltage-Inverting Converter

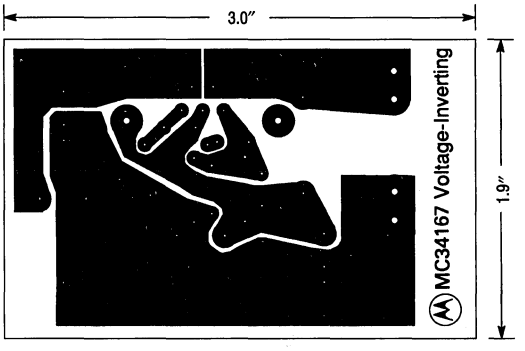


Test	Condition	Results
Line Regulation	V_{in} = 10 V to 24 V, I_O = 1.7 A	15 mV = ± 0.61%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 1.7 A	4.0 mV = ± 0.020%
Output Ripple	V_{in} = 12 V, I_O = 1.7 A	78 mV_{p-p}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	5.7 A
Efficiency	V_{in} = 12 V, I_O = 1.7 A V_{in} = 24 V, I_O = 1.7 A	79.5% 86.2%

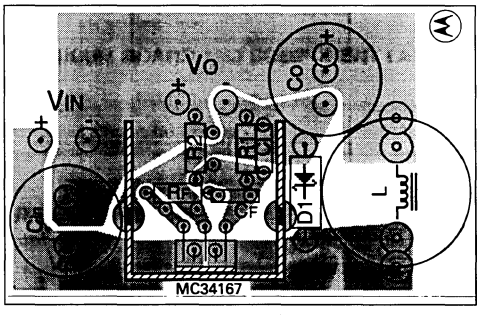
L = Coilcraft M1496-A or ELMACO CHK1050, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.
Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Two potential problems arise when designing the standard voltage-inverting converter with the MC34167. First, the Switch Output emitter is limited to –1.5 V with respect to the ground pin and second, the Error Amplifier's noninverting input is internally committed to the reference and is not pinned out. Both of these problems are resolved by connecting the IC ground pin to the converter's negative output as shown in Figure 22. This keeps the emitter of Q_1 positive with respect to the ground pin and has the effect of reversing the Error Amplifier inputs. Note that the voltage drop across R_1 is equal to 5.05 V when the output is in regulation.

Figure 23. Voltage-Inverting Converter Printed Circuit Board and Component Layout

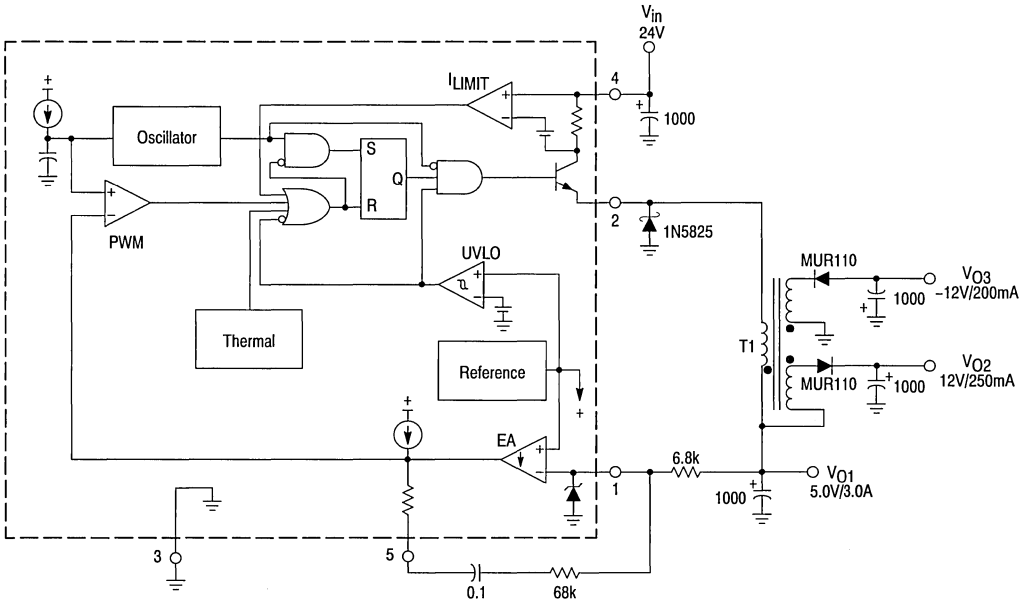


(Bottom View)



(Top View)

Figure 24. Triple Output Converter



Test		Condition	Results
Line Regulation	5.0 V 12 V –12 V	V_{in} = 15 V to 30 V, I_{O1} = 3.0 A, I_{O2} = 250 mA, I_{O3} = 200 mA	3.0 mV = ± 0.029% 572 mV = ± 2.4% 711 mV = ± 2.9%
Load Regulation	5.0 V 12 V –12 V	V_{in} = 24 V, I_{O1} = 30 mA to 3.0 A, I_{O2} = 250 mA, I_{O3} = 200 mA V_{in} = 24 V, I_{O1} = 3.0 A, I_{O2} = 100 mA to 250 mA, I_{O3} = 200 mA V_{in} = 24 V, I_{O1} = 3.0 A, I_{O2} = 250 mA, I_{O3} = 75 mA to 200 mA	1.0 mV = ± 0.009% 409 mV = ±1.5% 528 mV = ± 2.0%
Output Ripple	5.0 V 12 V –12 V	V_{in} = 24 V, I_{O1} = 3.0 A, I_{O2} = 250 mA, I_{O3} = 200 mA	75 mV_{p-p} 20 mV_{p-p} 20 mV_{p-p}
Short Circuit Current	5.0 V 12 V –12 V	V_{in} = 24 V, R_L = 0.1 Ω	6.5 A 2.7 A 2.2 A
Efficiency	TOTAL	V_{in} = 24 V, I_{O1} = 3.0 A, I_{O2} = 250 mA, I_{O3} = 200 mA	84.2%

T1 = Primary: Coilcraft M1496-A or ELMACO CHK1050, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.
Secondary: V_{O2} — 69 turns of #26 AWG
V_{O3} — 104 turns of #28 AWG
Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

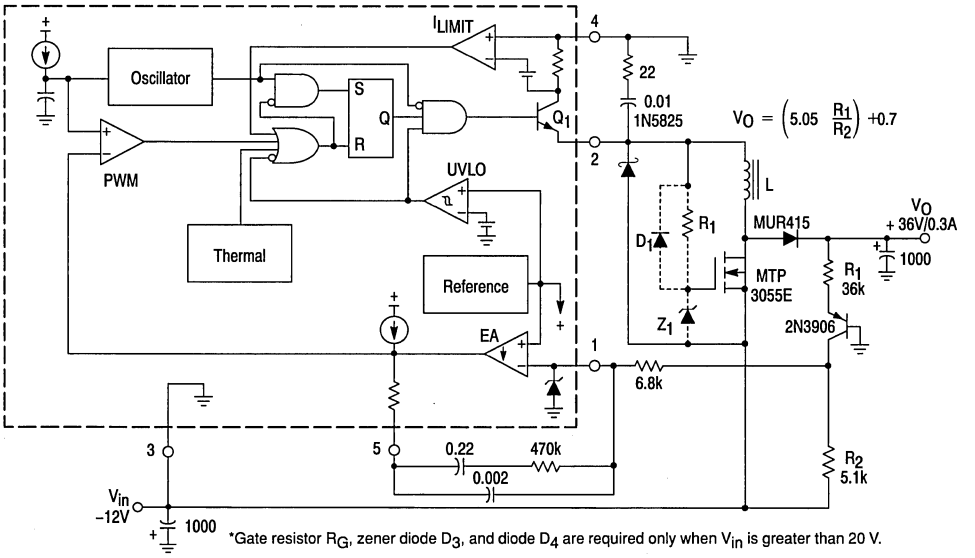
Multiple auxiliary outputs can easily be derived by winding secondaries on the main output inductor to form a transformer. The secondaries must be connected so that the energy is delivered to the auxiliary outputs when the Switch Output turns off. During the off-time, the voltage across the primary winding is regulated by the feedback loop, yielding a constant Volts/Turn ratio. The number of turns for any given secondary voltage can be calculated by the following equation:

$$\#\ TURNS_{(SEC)} = \frac{V_{O(SEC)} + V_{F(SEC)}}{\left(\frac{V_{O(PRI)} + V_{F(PRI)}}{\#TURNS_{(PRI)}}\right)}$$

Note that the 12 V winding is stacked on top of the 5.0 V output. This reduced the number of secondary turns and improves lead regulation. For best auxiliary regulation, the auxiliary outputs should be less than 33% of the total output power.

3

Figure 25. Negative Input/Positive Output Regulator

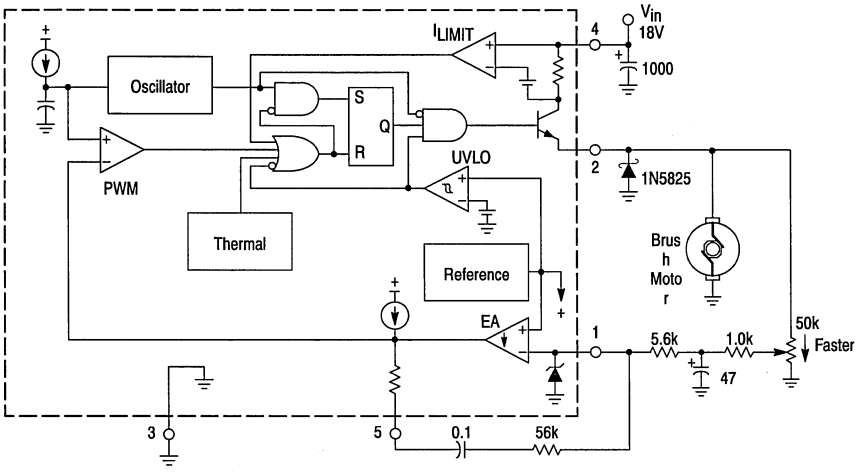


*Gate resistor R_G, zener diode D_3, and diode D_4 are required only when V_{in} is greater than 20 V.

Test	Condition	Results
Line Regulation	V_{in} = –10 V to – 20 V, I_O = 0.3 A	266 mV = ± 0.38%
Load Regulation	V_{in} = –12 V, I_O = 0.03 A to 0.3 A	7.90 mV = ±1.1%
Output Ripple	V_{in} = –12 V, I_O = 0.3 A	100 mV_{p-p}
Efficiency	V_{in} = –12 V, I_O = 0.3 A	78.4%

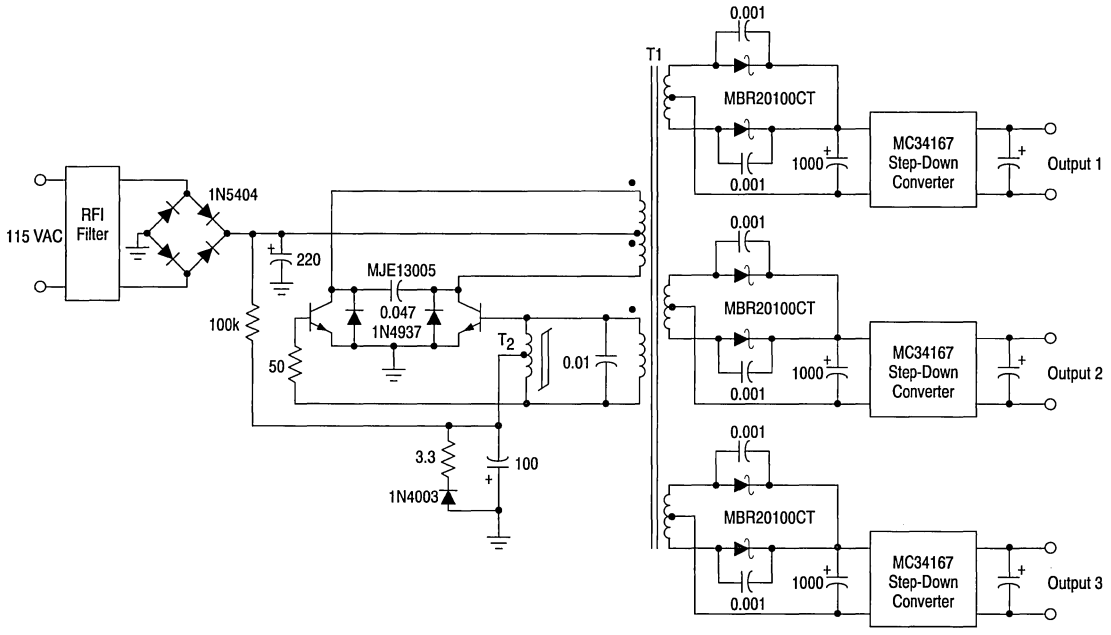
L = ELMACO CHK1050, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.
Heatsink = AAVID Engineering Inc. 5903B or 5930B

Figure 26. Variable Motor Speed Control with EMF Feedback Sensing



Test	Condition	Results
Low Speed Line Regulation	V_{in} = 12 V to 24 V	1760 RPM ±1%
High Speed Line Regulation	V_{in} = 12 V to 24 V	3260 RPM ± 6%

Figure 27. Off-Line Preconverter



T_1 = Core and Bobbin — Coilcraft PT3595
Primary — 104 turns #26 AWG
Base Drive — 3 turns #26 AWG
Secondaries — 16 turns #16 AWG
Total Gap — 0.002″

T_2 = Core — TDK T6 x 1.5 x 3 H5C2
14 turns center tapped #30 AWG

Heatsink = AAVID Engineering Inc.
MC34167 and MJE13005 — 5903B
MBR20100CT — 5925B

The MC34167 can be used cost effectively in off-line applications even though it is limited to a maximum input voltage of 40 V. Figure 27 shows a simple and efficient method for converting the AC line voltage down to 24 V. This preconverter has a total power rating of 125 W with a conversion efficiency of 90%. Transformer T_1 provides output isolation from the AC line and isolation between each of the secondaries. The circuit self-oscillates at 50 kHz and is controlled by the saturation characteristics of T_2. Multiple MC34167 post regulators can be used to provide accurate independently regulated outputs for a distributed power system.

MC33261
MC34261

3

Advance Information

Power Factor Controller

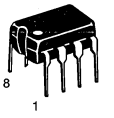
POWER FACTOR CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC34261, MC33261 series are active power factor controllers specifically designed for use as a preconverter in electronic ballast and in off-line power converter applications. These integrated circuits feature an internal start-up timer, a one quadrant multiplier for near unity power factor, zero current detector to ensure critical conduction operation, high gain error amplifier, trimmed internal bandgap reference, current sensing comparator, and a totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input undervoltage lockout with hysteresis, cycle-by-cycle current limiting, and a latch for single pulse metering. These devices are available in dual-in-line and surface mount plastic packages.

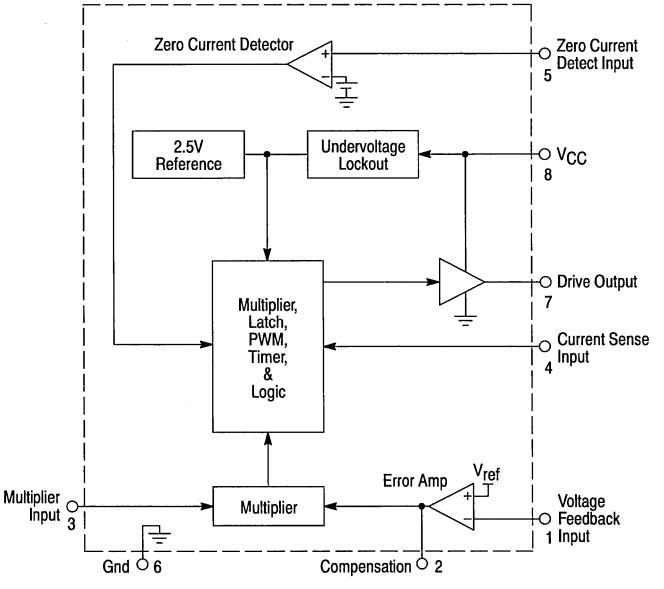
- Internal Start-Up Timer
- One Quadrant Multiplier
- Zero Current Detector
- Trimmed 2% Internal Bandgap Reference
- Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current
- Pinout Equivalent to the SG3561
- Functional Equivalent to the TDA 4817



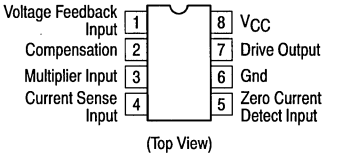
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34261D	0° to +70°C	SO-8
MC34261P		Plastic DIP
MC33261D	−40° to +85°C	SO-8
MC33261P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	500	mA
Current Sense, Multiplier, and Voltage Feedback Inputs	V_{in}	−1.0 to 10	V
Zero Current Detect Input High State Forward Current Low State Reverse Current	I_{in}	 50 −10	mA
Power Dissipation and Thermal Characteristics P Suffix, Plastic Package Case 626 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction-to-Air D Suffix, Plastic Package Case 626 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction-to-Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 800 100 450 178	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34261 MC33261	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Voltage Feedback Input Threshold T_A = 25°C $T_A = T_{low}$ to T_{high} (V_{CC} = 12 V to 28 V)	V_{FB}	 2.465 2.44	2.5	 2.535 2.54	V
Line Regulation (V_{CC} = 12 V to 28 V, T_A = 25°C)	Reg_{line}	—	1.0	10	mV
Input Bias Current (V_{FB} = 0 V)	I_{IB}	—	−0.3	−1.0	µA
Open Loop Voltage Gain	A_{VOL}	65	85	—	dB
Gain Bandwidth Product (T_A = 25°C)	GBW	0.7	1.0	—	MHz
Output Source Current (V_O = 4.0 V, V_{FB} = 2.3 V)	I_{Source}	0.25	0.5	0.75	mA
Output Voltage Swing High State (I_{Source} = 0.2 mA, V_{FB} = 2.3 V) Low State (I_{Sink} = 0.4 mA, V_{FB} = 2.7 V)	 V_{OH} V_{OL}	 5.0 —	 5.7 2.1	 — 2.44	V
MULTIPLIER					
Dynamic Input Voltage Range Multiplier Input (Pin 3) Compensation (Pin 2)	 $V_{Pin\ 3}$ $V_{Pin\ 2}$	 0 to 2.5 V_{FB} to (V_{FB} + 1.0)	 0 to 3.5 V_{FB} to (V_{FB} + 1.5)	 — —	V
Input Bias Current (V_{FB} = 0 V)	I_{IB}	—	−0.3	−1.0	µA
Multiplier Gain ($V_{Pin\ 3}$ = 0.5 V, $V_{Pin\ 2} = V_{FB}$ + 1.0 V, Note 2)	K	0.4	0.62	0.8	1/V
ZERO CURRENT DETECTOR					
Input Threshold Voltage (V_{in} Increasing)	V_{th}	1.3	1.6	1.8	V
Hysteresis (V_{in} Decreasing)	V_H	40	110	200	mV
Input Clamp Voltage High State (I_{DET} = 3.0 mA) Low State (I_{DET} = −3.0 mA)	 V_{IH} V_{IL}	 6.1 0.3	 6.7 0.7	 — 1.0	V
CURRENT SENSE COMPARATOR					
Input Bias Current ($V_{Pin\ 4}$ = 0 V)	I_{IB}	—	−0.5	−2.0	µA
Input Offset Voltage ($V_{Pin\ 2}$ = 1.1 V, $V_{Pin\ 3}$ = 0 V)	V_{IO}	—	3.5	15	mV
Delay to Output	$t_{PHL\ (in/out)}$	—	200	400	ns

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DRIVE OUTPUT					
Output Voltage (V_{CC} = 12 V)					V
Low State (I_{Sink} = 20 mA)	V_{OL}	—	0.3	0.8	
(I_{Sink} = 200 mA)		1.8	2.4	3.3	
High State (I_{Source} = 20 mA)	V_{OH}	9.8	10.3	—	
(I_{Source} = 200 mA)		7.8	8.3	8.8	
Output Voltage (V_{CC} = 30 V)					V
High State (I_{Source} = 20 mA, C_L = 15 pF)	$V_{O(max)}$	14	16	18	
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	—	50	120	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	—	50	120	ns
Output Voltage with UVLO Activated (V_{CC} = 7.0 V, I_{Sink} = 1.0 mA)	$V_{OH(UVLO)}$	—	0.2	0.8	V
RESTART TIMER					
Restart Time Delay	t_{DLY}	150	400	—	μs
UNDERVOLTAGE LOCKOUT					
Start-Up Threshold (V_{CC} Increasing)	V_{th}	9.2	10.0	10.8	V
Minimum Operating Voltage After Turn-On (V_{CC} Decreasing)	$V_{Shutdown}$	7.0	8.0	9.0	V
Hysteresis	V_H	1.75	2.0	2.5	V
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Start-Up (V_{CC} = 7.0 V)		—	0.3	0.5	
Operating		—	7.1	12	
Dynamic Operating (50 kHz, C_L = 1.0 nF)		—	9.0	20	
Power Supply Zener Voltage	V_Z	30	36	—	V

NOTES: 1. Maximum package power dissipation limits must be observed.

2. $K = \dfrac{\text{Pin 4 Threshold Voltage}}{V_{Pin\ 3}(V_{Pin\ 2} - V_{FB})}$

3. T_{low} = 0°C for MC34261, −40°C for MC33261; T_{high} = +70°C for MC34261, +85°C for MC33261

Figure 1. Current Sense Input Threshold versus Multiplier Input

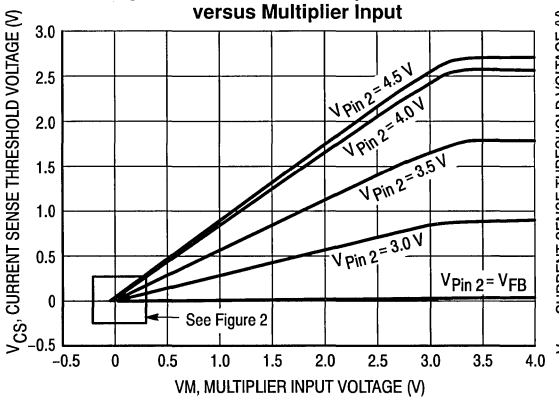


Figure 2. Current Sense Input Threshold versus Multiplier Input

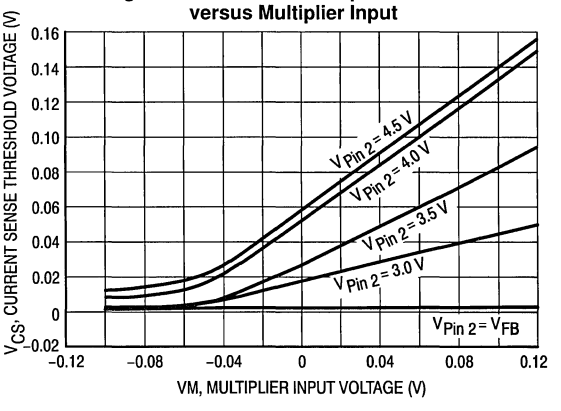


Figure 3. Voltage Feedback Input Threshold Change versus Temperature

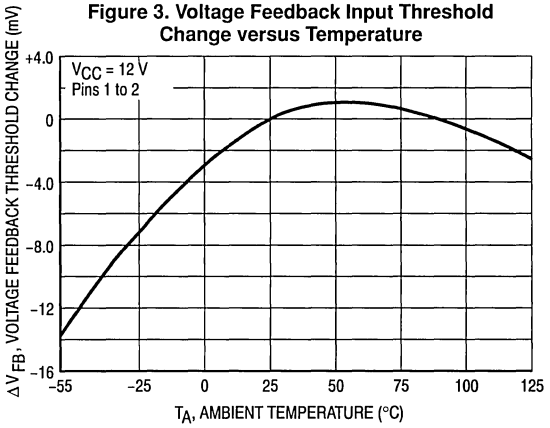


Figure 4. Error Amp Open-Loop Gain and Phase versus Frequency

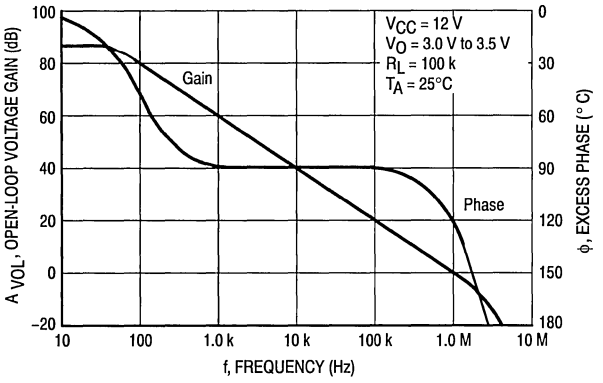


Figure 5. Error Amp Small Signal Transient Response

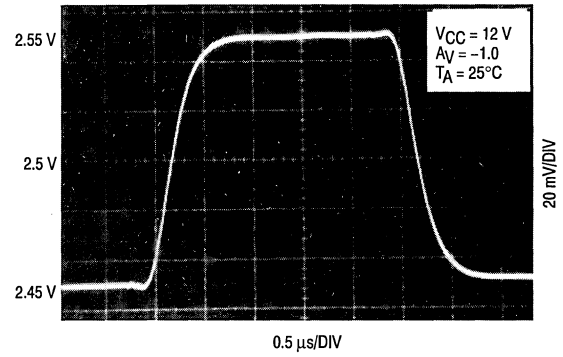


Figure 6. Error Amp Large Signal Transient Response

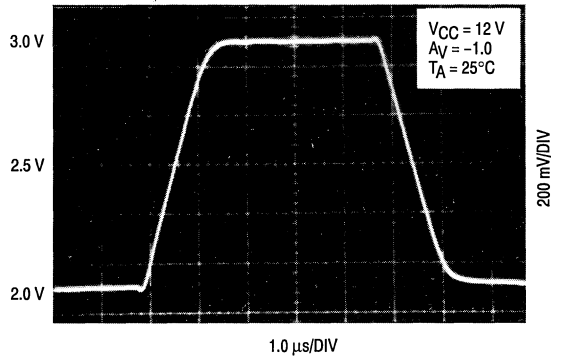


Figure 7. Error Amp Output Saturation versus Sink Current

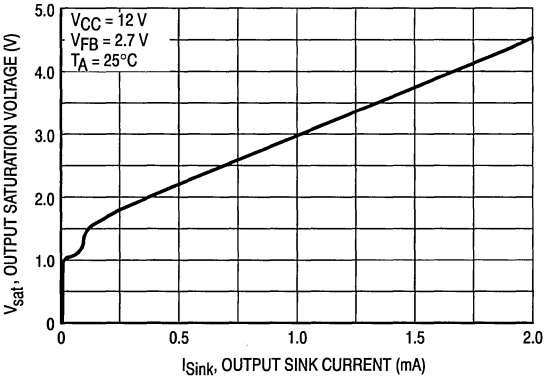


Figure 8. Restart Time Delay versus Temperature

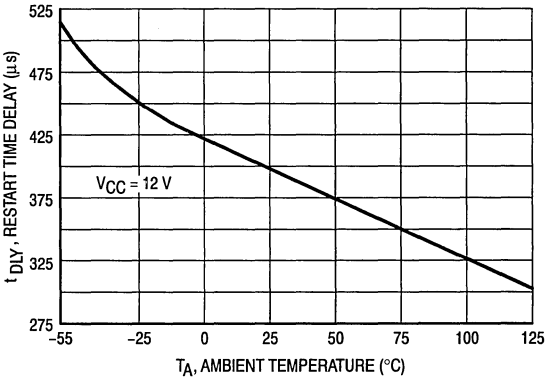


Figure 9. Zero Current Detector Input Threshold Voltage Change versus Temperature

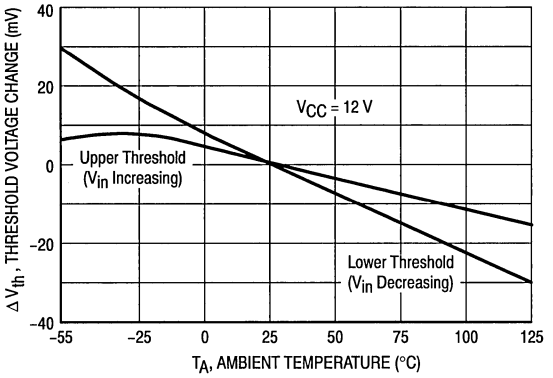


Figure 10. Output Saturation Voltage versus Load Current

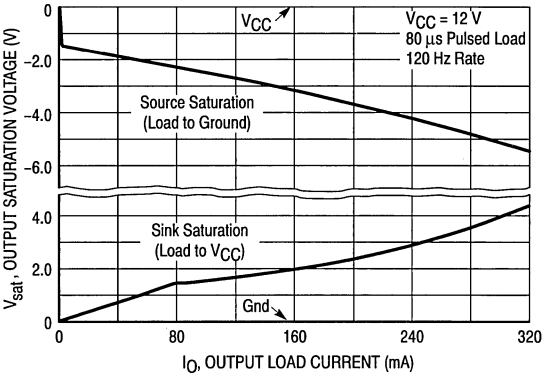


Figure 11. Drive Output Waveform

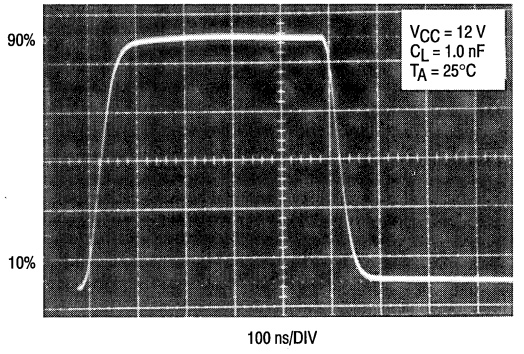


Figure 12. Drive Output Cross Conduction

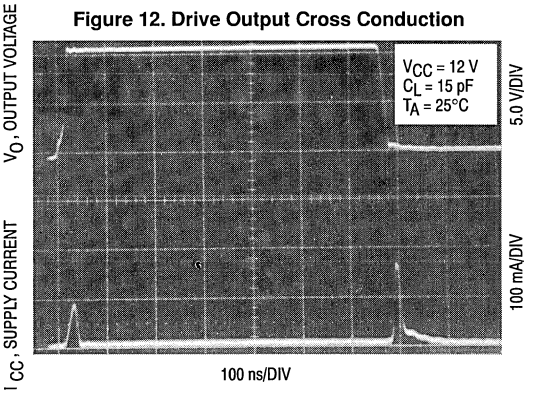


Figure 13. Supply Current versus Supply Voltage

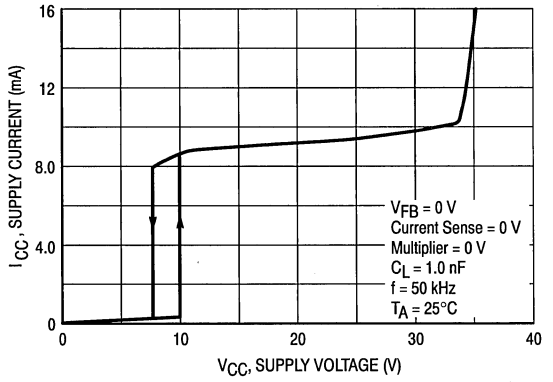
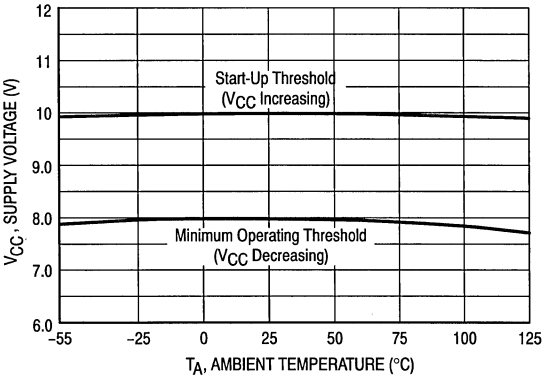


Figure 14. Undervoltage Lockout Thresholds versus Temperature



FUNCTIONAL DESCRIPTION

Introduction

Most electronic ballasts and switching power supplies use a bridge rectifier and a filter capacitor to derive raw DC voltage from the utility AC line. This simple rectifying circuit draws power from the line when the instantaneous AC voltage exceeds the capacitor's voltage. This occurs near the line voltage peak and results in a high charge current spike. Since power is only taken near the line voltage peaks, the resulting spikes of current are extremely nonsinusoidal with a high content of harmonics. This results in a poor power factor condition where the apparent input power is much higher than the real power.

The MC34261, MC33261 are high performance, critical conduction, current mode power factor controllers specifically designed for use in off-line active preconverters. These devices provide the necessary features required to significantly enhance poor power factor loads by keeping the AC line current sinusoidal and in phase with the line voltage. With proper control of the preconverter, almost any complex load can be made to appear resistive to the AC line, thus significantly reducing the harmonic current content.

Operating Description

The MC34261, MC33261 contains many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. There are, however, two areas where there is a major difference when compared to popular devices such as the UC3842 series. Referring to the block diagram in Figure 15, note that a multiplier has been added to the current sense loop and that this device does not contain an oscillator. A description of each of the functional blocks is given below.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 85 dB, and a unity gain bandwidth of 1.0 MHz with 58° of phase margin (Figure 4). The noninverting input is internally biased at 2.5 V ±2.0% and is not pinned out. The output voltage of the power factor converter is typically divided down and monitored by the inverting input. The maximum input bias current is –1.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the value of the upper divider resistor R_2. The Error Amp Output is internally connected to the Multiplier and is pinned out (Pin 2) for external loop compensation. Typically, the bandwidth is set below 20 Hz, so that the Error Amp output voltage is relatively constant over a given AC line cycle. The output stage consists of a 500 μA current source pull-up with a Darlington transistor pull-down. It is capable of swinging from 2.1 V to 5.7 V, assuring that the Multiplier can be driven over its entire dynamic range.

Multiplier

A single quadrant, two input multiplier is the critical element that enables this device to control power factor. The AC haversines are monitored at Pin 3 with respect to ground while the Error Amp output at Pin 2 is monitored with respect to the Voltage Feedback Input threshold. A graph of the Multiplier transfer curve is shown in Figure 1. Note that both inputs are extremely linear over a wide dynamic range, 0 V to 3.2 V for the Multiplier input (Pin 3), and 2.5 V to 4.0 V for the Error Amp output (Pin 2). The Multiplier output controls the Current Sense Comparator threshold (Pin 4) as the AC voltage traverses sinusoidally from zero to peak line. This has the effect of forcing the MOSFET peak current to track the input line voltage, thus making the preconverter load appear to be resistive.

$$\text{Pin 4 Threshold} \approx 0.62(V_{\text{Pin 2}} - V_{FB})V_{\text{Pin 3}}$$

Zero Current Detector

The MC34261 operates as a critical conduction current mode controller, whereby output switch conduction is initiated by the Zero Current Detector and terminated when the peak inductor current reaches the threshold level established by the Multiplier output. The Zero Current Detector initiates the next on-time by setting the RS Latch at the instant the inductor current reaches zero. This critical conduction mode of operation has two significant benefits. First, since the MOSFET cannot turn on until the inductor current reaches zero, the output rectifier's reverse recovery time becomes less critical allowing the use of an inexpensive rectifier. Second, since there are no deadtime gaps between cycles, the AC line current is continuous thus limiting the peak switch to twice the average input current.

The Zero Current Detector indirectly senses the inductor current by monitoring when the auxiliary winding voltage falls below 1.6 V. To prevent false tripping, 110 mV of hysteresis is provided. The Zero Current Detector input is internally protected by two clamps. The upper 6.7 V clamp prevents input overvoltage breakdown while the lower 0.7 V clamp prevents substrate injection. Device destruction can result if this input is shorted to ground. An external resistor must be used in series with the auxiliary winding to limit the current through the clamps.

Current Sense Comparator and RS Latch

The Current Sense Comparator RS Latch configuration ensures that only a single pulse appears at the Drive Output during a given cycle. The inductor current is converted to a voltage by inserting a ground referenced sense resistor R_9 in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input and compared to the Multiplier output voltage. The peak inductor current is controlled by the threshold voltage of Pin 4 where:

$$I_{pk} = \frac{\text{Pin 4 Threshold}}{R_9}$$

With the component values shown in Figure 16, the Current Sense Comparator threshold, at the peak of the haversine varies from 1.1 V at 90 Vac to 100 mV at 268 Vac. The Current Sense Input to Drive Output propagation delay is typically 200 ns.

Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand alone applications. The Timer provides a means to automatically start or restart the preconverter if the Drive Output has been off for more than 400 µs after the inductor current reaches zero.

Undervoltage Lockout

An Undervoltage Lockout comparator guarantees that the IC is fully functional before enabling the output stage. The positive power supply terminal (V_{CC}) is monitored by the UVLO comparator with the upper threshold set at 10 V and the lower threshold at 8.0 V (Figure 14). In the standby mode, with V_{CC} at 7.0 V, the required supply current is less than 0.5 mA (Figure 13). This hysteresis and low start-up current allow the implementation of efficient bootstrap start-up techniques, making these devices ideally suited for wide input range off line preconverter applications. An internal 36 V clamp has been added from V_{CC} to ground to protect the IC and capacitor C_5 from an overvoltage condition. This feature is desirable if external circuitry is used to delay the start-up of the preconverter.

Output

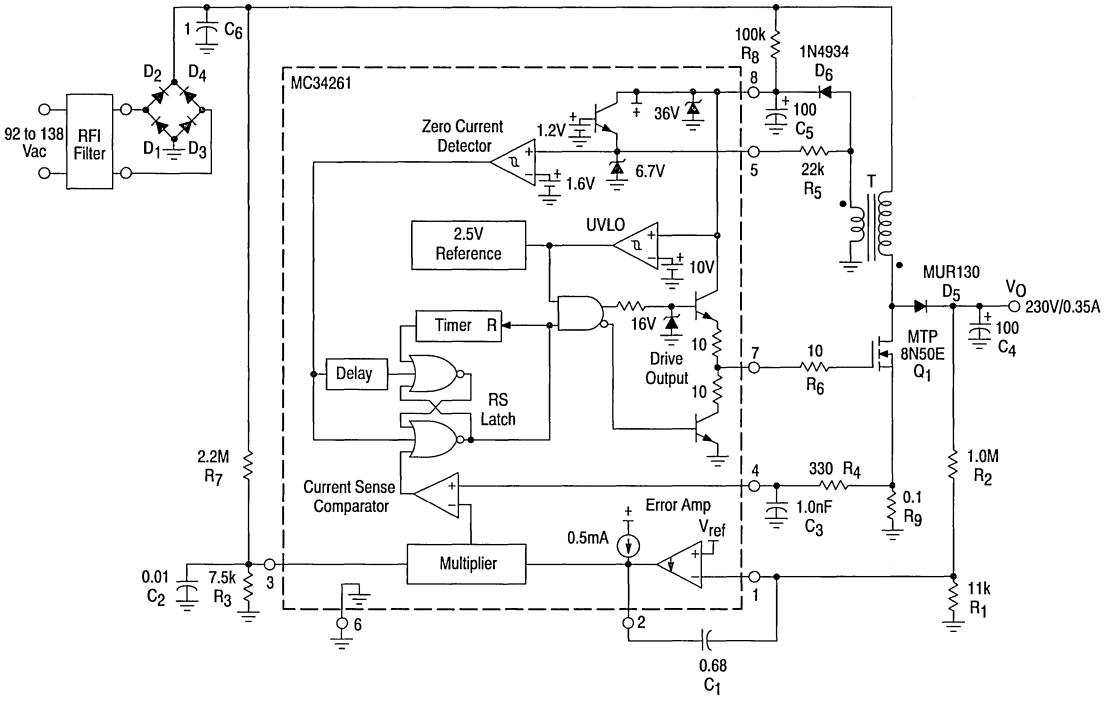
The MC34261/MC33261 contain a single totem pole output stage specifically designed for direct drive of power MOSFETs. The Drive Output is capable of up to ±500 mA peak current with a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Drive Output in a sinking mode whenever the Undervoltage Lockout is active. This characteristic eliminates the need for an external gate pull-down resistor. The totem pole output has been optimized to minimize cross conduction current during high speed operation. The addition of two 10 Ω resistors, one in series with the source output transistor and one in series with the sink output transistor, reduces the cross conduction current, as shown in Figure 12. A 16 V clamp has been incorporated into the output stage to limit the high state V_{OH}. This prevents rupture of the MOSFET gate when V_{CC} exceeds 20 V.

Table 1. Design Equations

Calculation	Formula	Notes
Required Converter Output Power	$P_O = V_O I_O$	Calculate the maximum required output power.
Peak Inductor Current	$I_{L(pk)} = \frac{2\sqrt{2}\,P_O}{\eta Vac_{(LL)}}$	Calculated at the minimum required AC line for regulation. Let the efficiency n = 0.95.
Inductance	$L = \frac{2t\left(\frac{V_O}{\sqrt{2}} - Vac\right) Vac^2}{V_O\, Vac_{(LL)}\, I_{L(pk)}}$	Let the switching cycle t = 20 µs.
Switch On-Time	$t_{on} = \frac{2\,P_O\,L}{\eta\, Vac^2}$	In theory the on-time t_{on} is constant. In practice t_{on} tends to increase at the AC line zero crossings due to the charge on capacitor C_6.
Switch Off-Time	$t_{off} = \frac{t_{on}}{\frolac{V_O}{\sqrt{2}\,Vac\,\lvert Sin\,\theta\rvert} - 1}$	The off-time t_{off} is greatest at peak AC line and approaches zero at the AC line zero crossings. Theta (θ) represents the angle of the AC line voltage.
Switching Frequency	$f = \frac{1}{t_{on} + t_{off}}$	The minimum switching frequency occurs at peak AC line and increases as t_{off} decreases.
Peak Switch Current	$R_9 = \frac{V_{CS}}{I_{L(pk)}}$	Set the current sense threshold V_{CS} to 1.0 V for universal input (85 Vac to 265 Vac) operation and to 0.5 V for fixed input (92 Vac to 138 Vac, or 184 to 276 Vac) operation.
Multiplier Input Voltage	$V_M = \frac{Vac\,\sqrt{2}}{\left(\frac{R_7}{R_3} + 1\right)}$	Set the multiplier input voltage V_M to 3.0 V at high line. Empirically adjust V_M for the lowest distortion over the AC line range while guaranteeing start-up at minimum line.
Converter Output Voltage	$V_O = V_{ref}\left(\frac{R_2}{R_1} + 1\right) - I_{IB}\,R_1$	The $I_{IB}\,R_1$ error term can be minimized with a divider current in excess of 100 µA.
Error Amplifier Bandwidth	$BW = \frac{1}{2\pi \frac{R_1\,R_2}{R_1 + R_2} C_1}$	The bandwidth is typically set to 20 Hz for minimum output ripple over the AC line haversine.

The following converter characteristics must be chosen:
- V_O — Desired output voltage
- I_O — Desired output current
- Vac — AC RMS line voltage
- $Vac_{(LL)}$ — AC RMS low line voltage

Figure 15. 80 W Power Factor Controller



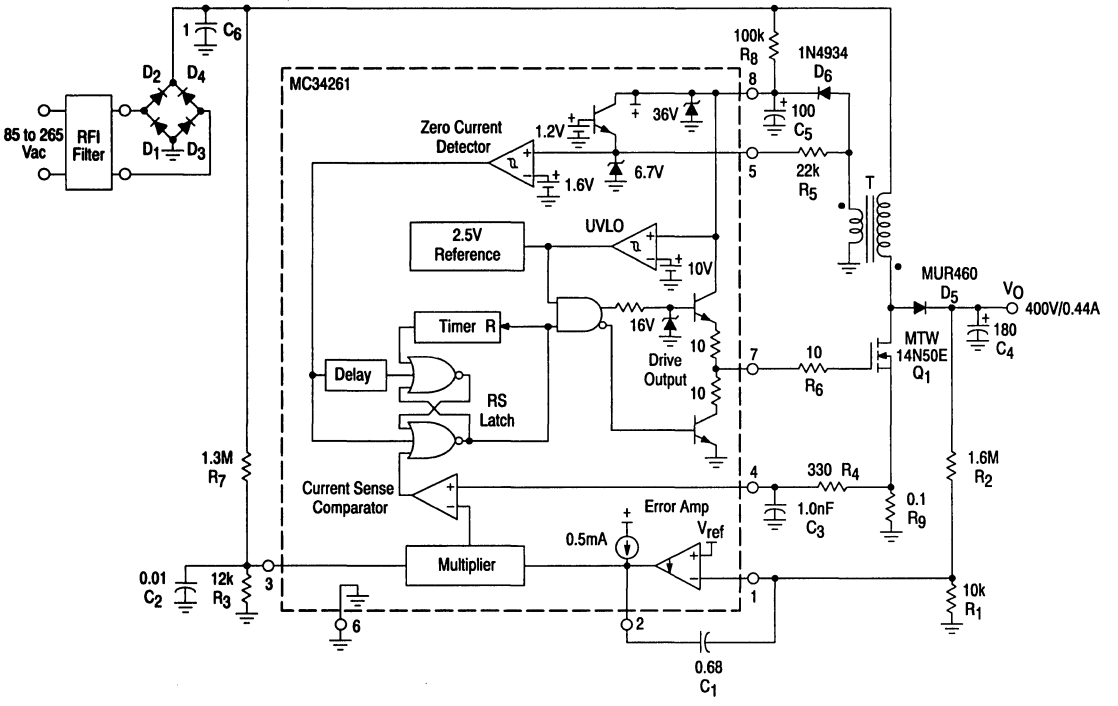
Power Factor Controller Test Data

AC Line Input								DC Output				
			Current Harmonic Distortion (%)									
V_{rms}	P_{in}	PF	THD	2	3	5	7	$V_{O(p-p)}$	V_O	I_O	P_O	n(%)
90	85.6	–0.998	2.4	0.11	0.52	1.3	0.67	10.0	230	0.350	80.5	94.0
100	85.1	–0.997	5.0	0.13	1.7	2.4	1.4	10.1	230	0.350	80.5	94.6
110	84.8	–0.997	5.3	0.12	2.5	2.6	1.5	10.2	230	0.350	80.5	94.9
120	84.5	–0.997	5.8	0.12	3.2	2.7	1.4	10.2	230	0.350	80.5	95.3
130	84.2	–0.996	6.6	0.12	4.0	2.8	1.5	10.2	230	0.350	80.5	95.6
138	84.1	–0.995	7.2	0.13	4.5	3.0	1.6	10.2	230	0.350	80.5	95.7

This data was taken with the test set-up shown in Figure 17.

T = Coilcraft N2881-A
Primary: 62 turns of # 22 AWG
Secondary: 5 turns of # 22 AWG
Core: Coilcraft PT2510, EE 25
Gap: 0.072″ total for a primary inductance of 320 μH
Heatsink = AAVID Engineering Inc. 5903B, or 5930B

Figure 16. 175 W Universal Input Power Factor Controller



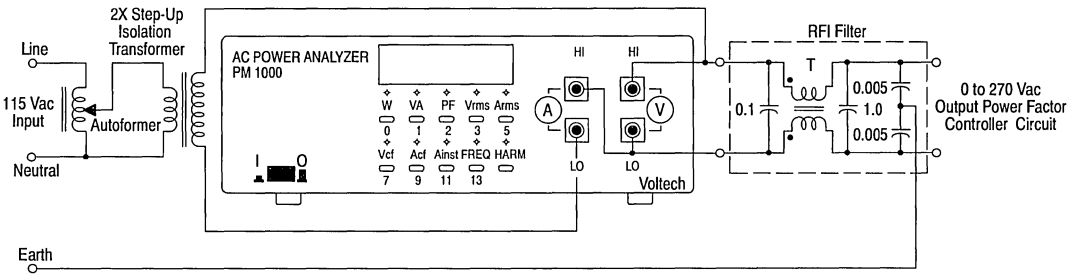
Power Factor Controller Test Data

AC Line Input								DC Output				
			Current Harmonic Distortion (%)									
V_{rms}	P_{in}	PF	THD	2	3	5	7	$V_{O(p-p)}$	V_O	I_O	P_O	n(%)
90	187.5	–0.998	2.0	0.10	0.98	0.90	0.78	8.0	400.7	0.436	174.7	93.2
120	184.6	–0.997	1.8	0.09	1.3	1.3	0.93	8.0	400.7	0.436	174.7	94.6
138	183.6	–0.997	2.3	0.05	1.6	1.5	1.0	8.0	400.7	0.436	174.7	95.2
180	181.0	–0.995	4.3	0.16	2.5	2.0	1.2	8.0	400.6	0.436	174.7	95.6
240	179.3	–0.993	6.0	0.08	3.7	2.7	1.4	8.0	400.6	0.436	174.7	97.4
268	178.6	–0.992	6.7	0.16	2.8	3.7	1.7	8.0	400.6	0.436	174.7	97.8

This data was taken with the test set-up shown in Figure 17.

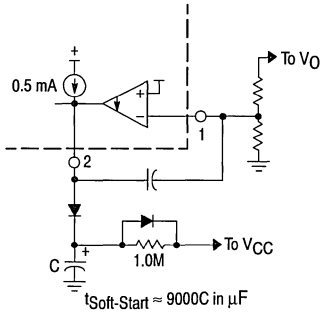
T = Coilcraft N2880-A
Primary: 78 turns of # 16 AWG
Secondary: 6 turns of # 18 AWG
Core: Coilcraft PT4215, EE 42-15
Gap: 0.104″ total for a primary inductance of 870 µH
Heatsink = AAVID Engineering Inc. 5903B

Figure 17. Power Factor Test Set-Up



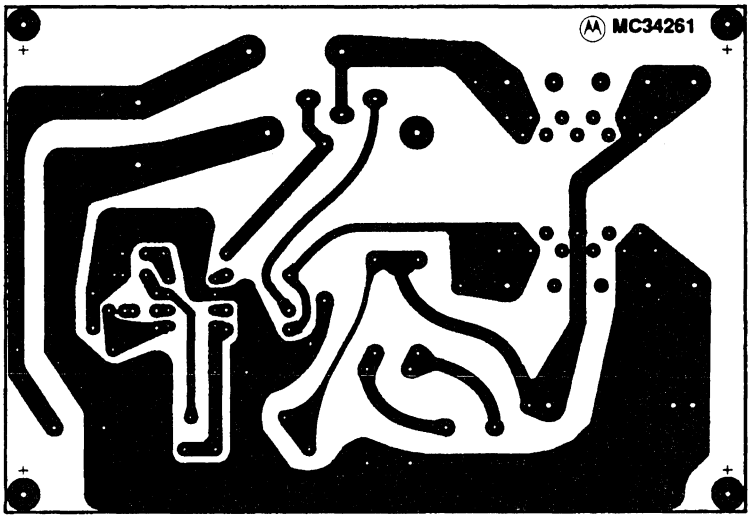
An RFI filter is required for best performance when connecting the preconverter directly to the AC line. Commercially available two stage filters such as the Delta Electronics 03DPCG5 work excellent. The simple single stage test filter shown above can easily be constructed with a common mode transformer. Transformer (T) is a Coilcraft CMT3-28-2 with 28 mH minimum inductance and a 2.0 A maximum current rating.

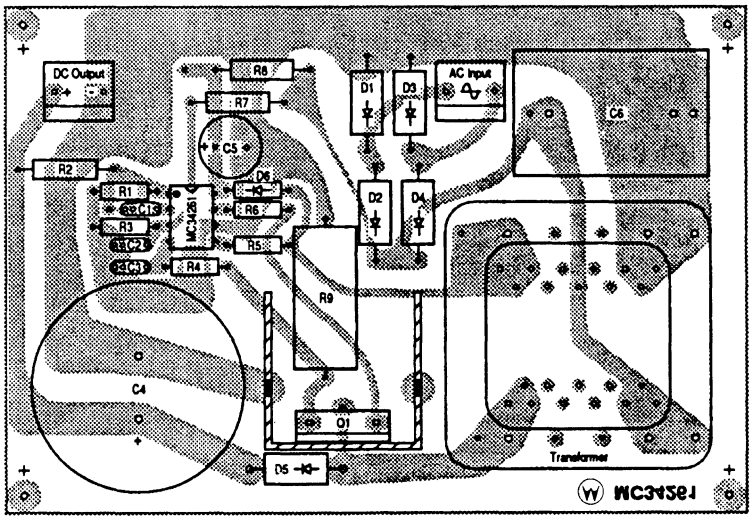
Figure 18. Soft-Start Circuit



Start-up overshoot can be eliminated with the addition of a Soft-Start circuit.

Figure 20. Printed Circuit Board and Component Layout
(Circuits of Figures 15 and 16)





Advance Information

Power Factor Controllers

MC34262
MC33262

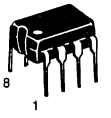
POWER FACTOR CONTROLLERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC34262, MC33262 series are active power factor controllers specifically designed for use as a preconverter in electronic ballast and in off-line power converter applications. These integrated circuits feature an internal start-up timer for stand-alone applications, a one quadrant multiplier for near unity power factor, zero current detector to ensure critical conduction operation, transconductance error amplifier, quickstart circuit for enhanced start-up, trimmed internal bandgap reference, current sensing comparator, and a totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of an overvoltage comparator to eliminate runaway output voltage due to load removal, input undervoltage lockout with hysteresis, cycle-by-cycle current limiting, multiplier output clamp that limits maximum peak switch current, an RS latch for single pulse metering, and a drive output high state clamp for MOSFET gate protection. These devices are available in dual-in-line and surface mount plastic packages.

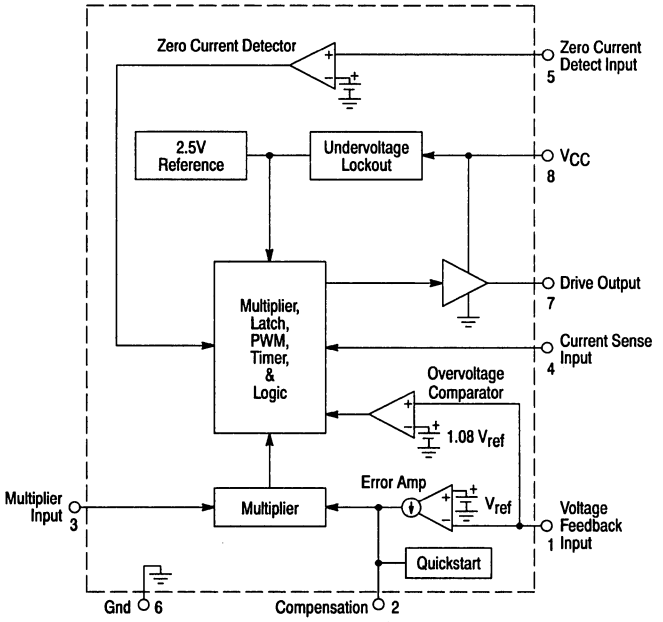
- Overvoltage Comparator Eliminates Runaway Output Voltage
- Internal Start-Up Timer
- One Quadrant Multiplier
- Zero Current Detector
- Trimmed 2% Internal Bandgap Reference
- Totem Pole Output with High State Clamp
- Undervoltage Lockout with 6.0 V of Hysteresis
- Low Start-Up and Operating Current
- Supersedes Functionality of SG3561 and TDA4817



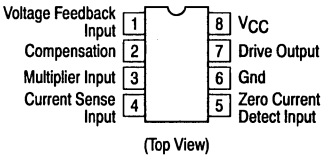
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34262D	0° to + 85°C	SO-8
MC34262P		Plastic DIP
MC33262D	– 40° to +105°C	SO-8
MC33262P		Plastic DIP

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	500	mA
Current Sense, Multiplier, and Voltage Feedback Inputs	V_{in}	–1.0 to +10	V
Zero Current Detect Input High State Forward Current Low State Reverse Current	I_{in}	 50 –10	mA
Power Dissipation and Thermal Characteristics P Suffix, Plastic Package, Case 626 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction-to-Air D Suffix, Plastic Package, Case 751 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction-to-Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 800 100 450 178	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34262 MC33262	T_A	 0 to + 85 – 40 to +105	°C
Storage Temperature	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V (Note 2), for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Voltage Feedback Input Threshold T_A = 25°C $T_A = T_{low}$ to T_{high} (V_{CC} = 12 V to 28 V)	V_{FB}	 2.465 2.44	 2.5 —	 2.535 2.54	V
Line Regulation (V_{CC} = 12 V to 28 V, T_A = 25°C)	Reg_{line}	—	1.0	10	mV
Input Bias Current (V_{FB} = 0 V)	I_{IB}	—	– 0.1	– 0.5	µA
Transconductance (T_A = 25°C)	g_m	80	100	130	µmho
Output Current Source (V_{FB} = 2.3 V) Sink (V_{FB} = 2.7 V)	I_O	 — —	 10 10	 — —	µA
Output Voltage Swing High State (V_{FB} = 2.3 V) Low State (V_{FB} = 2.7 V)	 $V_{OH(ea)}$ $V_{OL(ea)}$	 5.8 —	 6.4 1.7	 — 2.4	V
OVERVOLTAGE COMPARATOR					
Voltage Feedback Input Threshold	$V_{FB(OV)}$	1.065 V_{FB}	1.08 V_{FB}	1.095 V_{FB}	V
MULTIPLIER					
Input Bias Current, Pin 2 (V_{FB} = 0 V)	I_{IB}	—	– 0.1	– 0.5	µA
Input Threshold, Pin 2	$V_{th(M)}$	1.05 $V_{OL(EA)}$	1.2 $V_{OL(EA)}$	—	V
Dynamic Input Voltage Range Multiplier Input (Pin 3) Compensation (Pin 2)	 $V_{Pin\ 3}$ $V_{Pin\ 2}$	 0 to 2.5 $V_{th(M)}$ to ($V_{th(M)}$ + 1.0)	 0 to 3.5 $V_{th(M)}$ to ($V_{th(M)}$ + 1.5)	 — —	V
Multiplier Gain ($V_{Pin\ 3}$ = 0.5 V, $V_{Pin\ 2} = V_{th(M)}$ + 1.0 V, Note 4)	K	0.43	0.65	0.87	1/V
ZERO CURRENT DETECTOR					
Input Threshold Voltage (V_{in} Increasing)	V_{th}	1.33	1.6	1.87	V
Hysteresis (V_{in} Decreasing)	V_H	100	200	300	mV
Input Clamp Voltage High State (I_{DET} = + 3.0 mA) Low State (I_{DET} = – 3.0 mA)	 V_{IH} V_{IL}	 6.1 0.3	 6.7 0.7	 — 1.0	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V (Note 2), for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE COMPARATOR					
Input Bias Current ($V_{Pin\ 4}$ = 0 V)	I_{IB}	—	– 0.15	–1.0	µA
Input Offset Voltage ($V_{Pin\ 2}$ = 1.1 V, $V_{Pin\ 3}$ = 0 V)	V_{IO}	—	9.0	25	mV
Maximum Current Sense Input Threshold (Note 5)	$V_{th(max)}$	1.3	1.5	1.8	V
Delay to Output	$t_{PHL(in/out)}$	—	200	400	ns
DRIVE OUTPUT					
Output Voltage (V_{CC} = 12 V) Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA) High State (I_{Source} = 20 mA) (I_{Source} = 200 mA)	 V_{OL} V_{OH} 	 — — 9.8 7.8	 0.3 2.4 10.3 8.4	 0.8 3.3 — —	V
Output Voltage (V_{CC} = 30 V) High State (I_{Source} = 20 mA, C_L = 15 pF)	$V_{O(max)}$	14	16	18	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	—	50	120	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	—	50	120	ns
Output Voltage with UVLO Activated (V_{CC} = 7.0 V, I_{Sink} = 1.0 mA)	$V_{O(UVLO)}$	—	0.1	0.5	V
RESTART TIMER					
Restart Time Delay	t_{DLY}	200	620	—	µs
UNDERVOLTAGE LOCKOUT					
Start-Up Threshold (V_{CC} Increasing)	$V_{th(on)}$	11.5	13	14.5	V
Minimum Operating Voltage After Turn-On (V_{CC} Decreasing)	$V_{Shutdown}$	7.0	8.0	9.0	V
Hysteresis	V_H	3.8	5.0	6.2	V
TOTAL DEVICE					
Power Supply Current Start-Up (V_{CC} = 7.0 V) Operating Dynamic Operating (50 kHz, C_L = 1.0 nF)	I_{CC}	 — — —	 0.25 6.5 9.0	 0.4 12 20	mA
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	—	V

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the start-up threshold before setting to 12 V.
3. T_{low} = 0°C for MC34262 = – 40°C for MC33262 T_{high} = + 85°C for MC34262 = +105°C for MC33262
4. $K = \frac{\text{Pin 4 Threshold}}{V_{Pin\ 3}\,(V_{Pin\ 2} - V_{th(M)})}$
5. This parameter is measured with V_{FB} = 0 V, and $V_{Pin\ 3}$ = 3.0 V.

Figure 1. Current Sense Input Threshold versus Multiplier Input

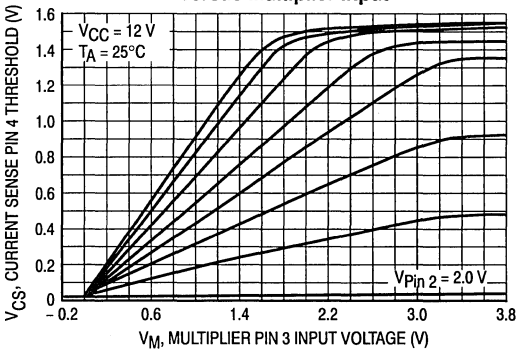

Figure 2. Current Sense Input Threshold versus Multiplier Input, Expanded View

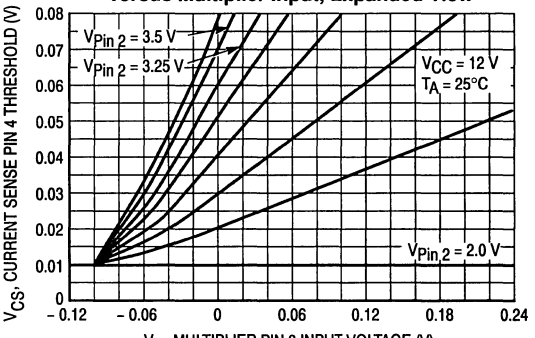

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Figure 3. Voltage Feedback Input Threshold Change versus Temperature

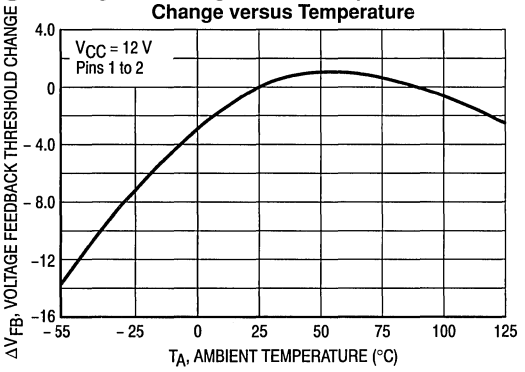


Figure 4. Overvoltage Comparator Input Threshold versus Temperature

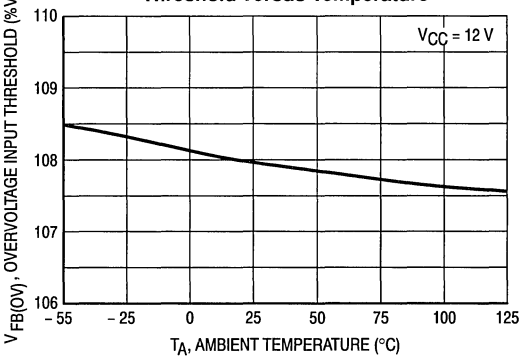


Figure 5. Error Amp Transconductance and Phase versus Frequency

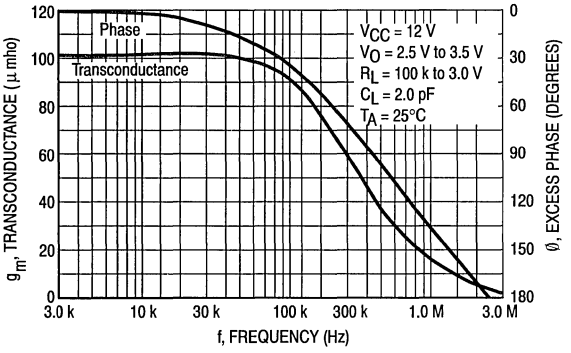


Figure 6. Error Amp Transient Response

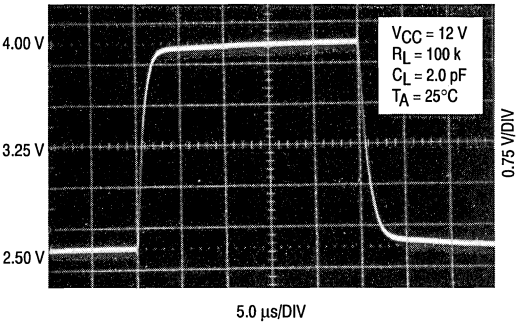


Figure 7. Quickstart Charge Current versus Temperature

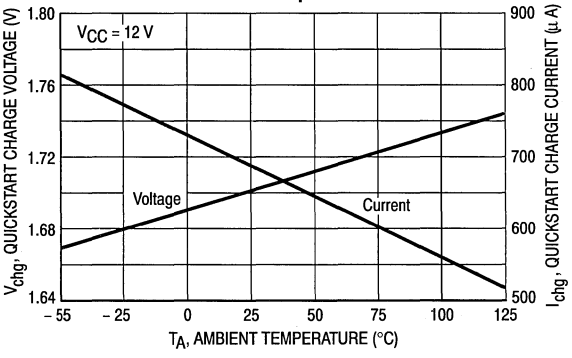


Figure 8. Restart Timer Delay versus Temperature

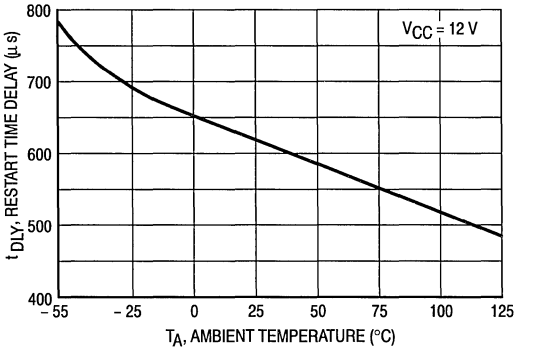


Figure 9. Zero Current Detector Input Threshold Voltage versus Temperature

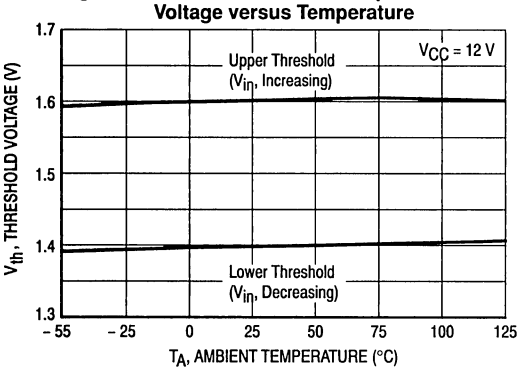


Figure 10. Output Saturation Voltage versus Load Current

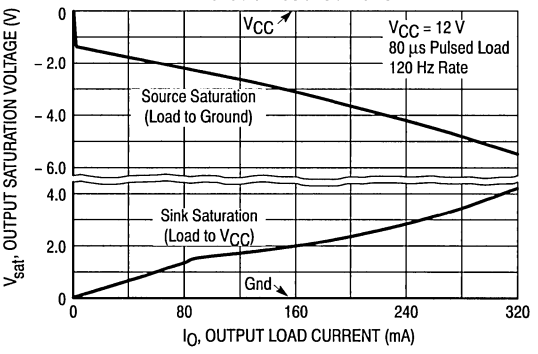


Figure 11. Drive Output Waveform

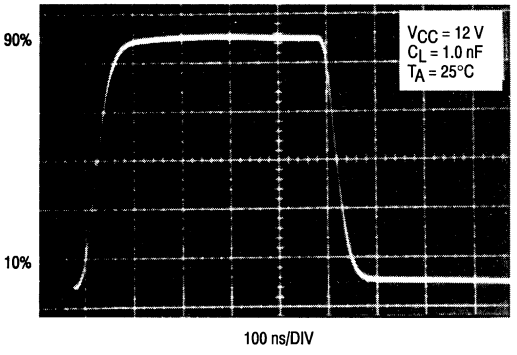


Figure 12. Drive Output Cross Conduction

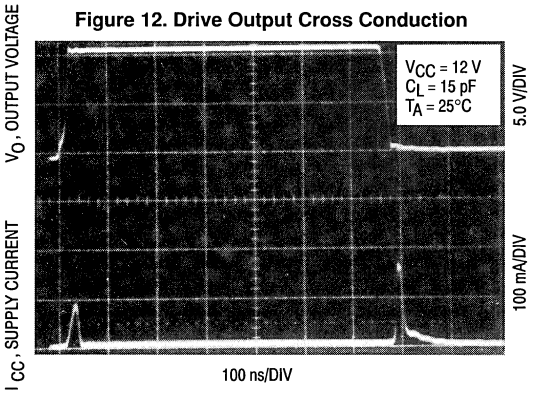


Figure 13. Supply Current versus Supply Voltage

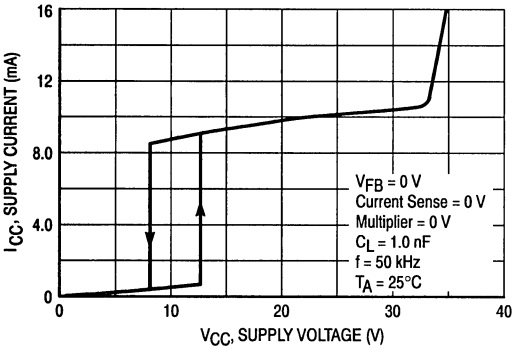
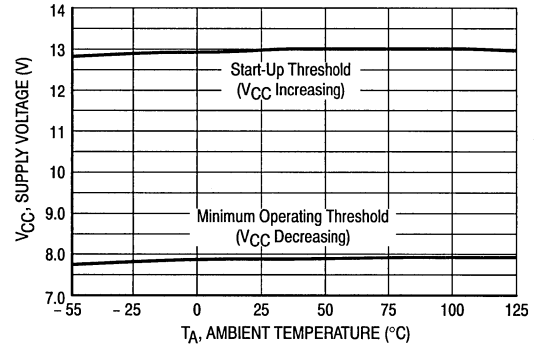


Figure 14. Undervoltage Lockout Thresholds versus Temperature



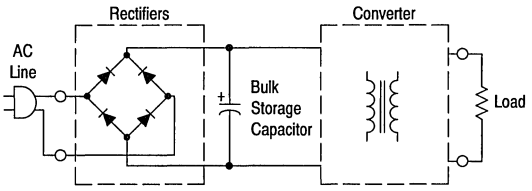
FUNCTIONAL DESCRIPTION

Introduction

With the goal of exceeding the requirements of legislation on line-current harmonic content, there is an ever increasing demand for an economical method of obtaining a unity power factor. This data sheet describes a monolithic control IC that was specifically designed for power factor control with minimal external components. It offers the designer a simple, cost-effective solution to obtain the benefits of active power factor correction.

Most electronic ballasts and switching power supplies use a bridge rectifier and a bulk storage capacitor to derive raw DC voltage from the utility AC line, Figure 15.

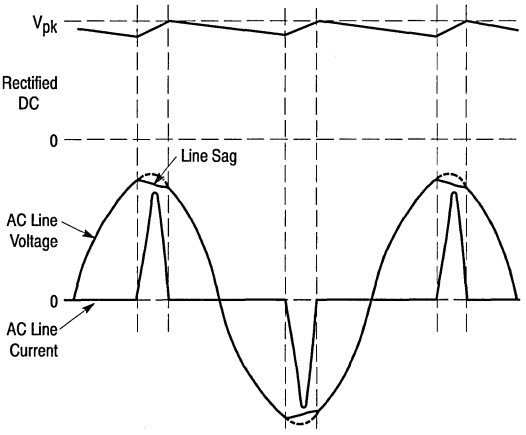
Figure 15. Uncorrected Power Factor Circuit



This simple rectifying circuit draws power from the line when the instantaneous AC voltage exceeds the capacitor voltage. This occurs near the line voltage peak and results in a high charge current spike, Figure 16. Since power is only taken near the line voltage peaks, the resulting spikes of current are extremely nonsinusoidal with a high content of harmonics. This results in a poor power factor condition where the apparent input power is much higher than the real power. Power factor ratios of 0.5 to 0.7 are common.

Power factor correction can be achieved with the use of either a passive or an active input circuit. Passive circuits usually contain a combination of large capacitors, inductors, and rectifiers that operate at the AC line frequency. Active circuits incorporate some form of a high frequency switching converter for the power processing, with the boost converter being the most popular topology, Figure 17. Since active input circuits operate at a frequency much higher than that of the AC line, they are smaller, lighter in weight, and more efficient than a passive circuit that yields similar results. With proper control of the preconverter, almost any complex load can be made to appear resistive to the AC line, thus significantly reducing the harmonic current content.

Figure 16. Uncorrected Power Factor Input Waveforms

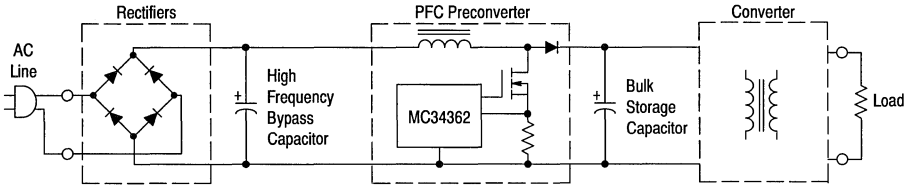


The MC34262, MC33262 are high performance, critical conduction, current-mode power factor controllers specifically designed for use in off-line active preconverters. These devices provide the necessary features required to significantly enhance poor power factor loads by keeping the AC line current sinusoidal and in phase with the line voltage.

Operating Description

The MC34262, MC33262 contain many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. There are, however, two areas where there is a major difference when compared to popular devices such as the UC3842 series. Referring to the block diagram in Figure 19, note that a multiplier has been added to the current sense loop and that this device does not contain an oscillator. The reasons for these differences will become apparent in the following discussion. A description of each of the functional blocks is given below.

Figure 17. Active Power Factor Correction Preconverter



Error Amplifier

An Error Amplifier with access to the inverting input and output is provided. The amplifier is a transconductance type, meaning that it has high output impedance with controlled voltage-to-current gain. The amplifier features a typical gm of 100 μmhos (Figure 5). The noninverting input is internally biased at 2.5 V ± 2.0% and is not pinned out. The output voltage of the power factor converter is typically divided down and monitored by the inverting input. The maximum input bias current is – 0.5 μA, which can cause an output voltage error that is equal to the product of the input bias current and the value of the upper divider resistor R_2. The Error Amp output is internally connected to the Multiplier and is pinned out (Pin 2) for external loop compensation. Typically, the bandwidth is set below 20 Hz, so that the amplifier's output voltage is relatively constant over a given AC line cycle. In effect, the error amp monitors the average output voltage of the converter over several line cycles. The Error Amp output stage was designed to have a relatively constant transconductance over temperature. This allows the designer to define the compensated bandwidth over the intended operating temperature range. The output stage can sink and source 10 μA of current and is capable of swinging from 1.7 V to 6.4 V, assuring that the Multiplier can be driven over its entire dynamic range.

A key feature to using a transconductance type amplifier, is that the input is allowed to move independently with respect to the output, since the compensation capacitor is connected to ground. This allows dual usage of of the Voltage Feedback Input pin by the Error Amplifier and by the Overvoltage Comparator.

Overvoltage Comparator

An Overvoltage Comparator is incorporated to eliminate the possibility of runaway output voltage. This condition can occur during initial startup, sudden load removal, or during output arcing and is the result of the low bandwidth that must be used in the Error Amplifier control loop. The Overvoltage Comparator monitors the peak output voltage of the converter, and when exceeded, immediately terminates MOSFET switching. The comparator threshold is internally set to 1.08 V_{ref}. In order to prevent false tripping during normal operation, the value of the output filter capacitor C_3 must be large enough to keep the peak-to-peak ripple less than 16% of the average DC output. The Overvoltage Comparator input to Drive Output turn-off propagation delay is typically 400 ns. A comparison of startup overshoot without and with the Overvoltage Comparator circuit is shown in Figure 23.

Multiplier

A single quadrant, two input multiplier is the critical element that enables this device to control power factor. The AC full wave rectified haversines are monitored at Pin 3 with respect to ground while the Error Amp output at Pin 2 is monitored with respect to the Voltage Feedback Input threshold. The Multiplier is designed to have an extremely linear transfer curve over a wide dynamic range, 0 V to 3.2 V for Pin 3, and 2.0 V to 3.75 V for Pin 2, Figure 1. The Multiplier output controls the Current Sense Comparator threshold as the AC voltage traverses sinusoidally from zero to peak line, Figure 18. This has the effect of forcing the MOSFET on-time to track the input line voltage, resulting in a fixed Drive Output on-time, thus making the preconverter load appear to be resistive to the AC line. An approximation of the Current Sense Comparator threshold can be calculated from the following equation. This equation is accurate only under the given test condition stated in the electrical table.

$$V_{CS}, \text{ Pin 4 Threshold} \approx 0.65 \, (V_{Pin\ 2} - V_{th(M)}) \, V_{Pin\ 3}$$

A significant reduction in line current distortion can be attained by forcing the preconverter to switch as the AC line voltage crosses through zero. The forced switching is achieved by adding a controlled amount of offset to the Multiplier and Current Sense Comparator circuits. The equation shown below accounts for the built-in offsets and is accurate to within ten percent. Let $V_{th(M)} = 1.991$ V

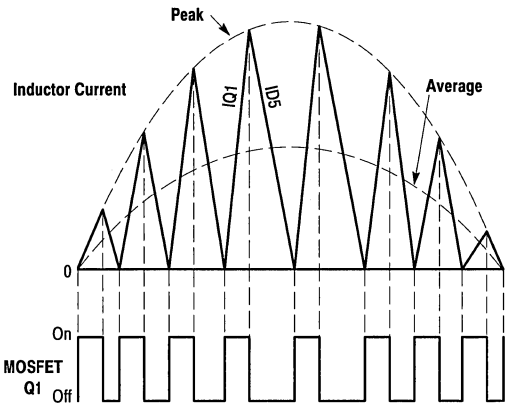
$$V_{CS}, \text{ Pin 4 Threshold} = 0.544 \, (V_{Pin\ 2} - V_{th(M)}) \, V_{Pin\ 3} + 0.0417 \, (V_{Pin\ 2} - V_{th(M)})$$

Zero Current Detector

The MC34262 operates as a critical conduction current mode controller, whereby output switch conduction is initiated by the Zero Current Detector and terminated when the peak inductor current reaches the threshold level established by the Multiplier output. The Zero Current Detector initiates the next on-time by setting the RS Latch at the instant the inductor current reaches zero. This critical conduction mode of operation has two significant benefits. First, since the MOSFET cannot turn-on until the inductor current reaches zero, the output rectifier reverse recovery time becomes less critical, allowing the use of an inexpensive rectifier. Second, since there are no deadtime gaps between cycles, the AC line current is continuous, thus limiting the peak switch to twice the average input current.

The Zero Current Detector indirectly senses the inductor current by monitoring when the auxiliary winding voltage falls below 1.4 V. To prevent false tripping, 200 mV of hysteresis is provided. Figure 9 shows that the thresholds are well-defined over temperature. The Zero Current Detector input is internally protected by two clamps. The upper 6.7 V clamp prevents input overvoltage breakdown while the lower 0.7 V clamp prevents substrate injection. Current limit protection of the lower clamp transistor is provided in the event that the input pin is accidentally shorted to ground. The Zero Current Detector input to Drive Output turn-on propagation delay is typically 320 ns.

Figure 18. Inductor Current and MOSFET Gate Voltage Waveforms



Current Sense Comparator and RS Latch

The Current Sense Comparator RS Latch configuration used ensures that only a single pulse appears at the Drive Output during a given cycle. The inductor current is converted to a voltage by inserting a ground-referenced sense resistor R_7 in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input and compared to a level derived from the Multiplier output. The peak inductor current under normal operating conditions is controlled by the threshold voltage of Pin 4 where:

$$I_{L(pk)} = \frac{\text{Pin 4 Threshold}}{R_7}$$

Abnormal operating conditions occur during preconverter startup at extremely high line or if output voltage sensing is lost. Under these conditions, the Multiplier output and Current Sense threshold will be internally clamped to 1.5 V. Therefore, the maximum peak switch current is limited to:

$$I_{pk(max)} = \frac{1.5\ V}{R_7}$$

An internal RC filter has been included to attenuate any high frequency noise that may be present on the current waveform. This filter helps reduce the AC line current distortion especially near the zero crossings. With the component values shown in Figure 20, the Current Sense Comparator threshold, at the peak of the haversine varies from 1.1 V at 90 Vac to 100 mV at 268 Vac. The Current Sense Input to Drive Output turn-off propagation delay is typically less than 200 ns.

Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand-alone applications. The Timer provides a means to automatically start or restart the preconverter if the Drive Output has been off for more than 620 μs after the inductor current reaches zero. The restart time delay versus temperature is shown in Figure 8.

Undervoltage Lockout and Quickstart

An Undervoltage Lockout comparator has been incorporated to guarantee that the IC is fully functional before enabling the output stage. The positive power supply terminal (V_{CC}) is monitored by the UVLO comparator with the upper threshold set at 13 V and the lower threshold at 8.0 V. In the stand-by mode, with V_{CC} at 7.0 V, the required supply current is less than 0.4 mA. This large hysteresis and low start-up current allow the implementation of efficient bootstrap start-up techniques, making these devices ideally suited for wide input range off-line preconverter applications. An internal 36 V clamp has been added from V_{CC} to ground to protect the IC and capacitor C_4 from an overvoltage condition. This feature is desirable if external circuitry is used to delay the startup of the preconverter. The supply current, startup, and operating voltage characteristics are shown in Figures 13 and 14.

A Quickstart circuit has been incorporated to optimize converter start-up. During initial start-up, compensation capacitor C_1 will be discharged, holding the error amp output below the Multiplier threshold. This will prevent Drive Output switching and delay bootstrapping of capacitor C_4 by diode D_6. If Pin 2 does not reach the multiplier threshold before C_4 discharges below the lower UVLO threshold, the converter will "hiccup" and experience a significant start-up delay. The Quickstart circuit is designed to precharge C_1 to 1.7 V, Figure 7. This level is slightly below the Pin 2 Multiplier threshold, allowing immediate Drive Output switching and bootstrap operation when C_4 crosses the upper UVLO threshold.

Drive Output

The MC34262/MC33262 contain a single totem-pole output stage specifically designed for direct drive of power MOSFETs. The Drive Output is capable of up to ± 500 mA peak current with a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Drive Output in a sinking mode whenever the Undervoltage Lockout is active. This characteristic eliminates the need for an external gate pull-down resistor. The totem-pole output has been optimized to minimize cross-conduction current during high speed operation. The addition of two 10 Ω resistors, one in series with the source output transistor and one in series with the sink output transistor, helps to reduce the cross-conduction current and radiated noise by limiting the output rise and fall time. A 16 V clamp has been incorporated into the output stage to limit the high state V_{OH}. This prevents rupture of the MOSFET gate when V_{CC} exceeds 20 V.

APPLICATIONS INFORMATION

The application circuits shown in Figures 19, 20 and 21 reveal that few external components are required for a complete power factor preconverter. Each circuit is a peak detecting current-mode boost converter that operates in critical conduction mode with a fixed on-time and variable off-time. A major benefit of critical conduction operation is that the current loop is inherently stable, thus eliminating the need for ramp compensation. The application in Figure 19 operates over an input voltage range of 90 Vac to 138 Vac and provides an output power of 80 W (230 V at 350 mA) with an associated power factor of approximately 0.998 at nominal line. Figures 20 and 21 are universal input preconverter examples that operate over a continuous input voltage range of 90 Vac to 268 Vac. Figure 20 provides an output power of 175 W (400 V at 440 mA) while Figure 21 provides 450 W (400 V at 1.125 A). Both circuits have an observed worst-case power factor of approximately 0.989. The input current and voltage waveforms of Figure 20 are shown in Figure 22 with operation at 115 Vac and 230 Vac. The data for each of the applications was generated with the test set-up shown in Figure 24.

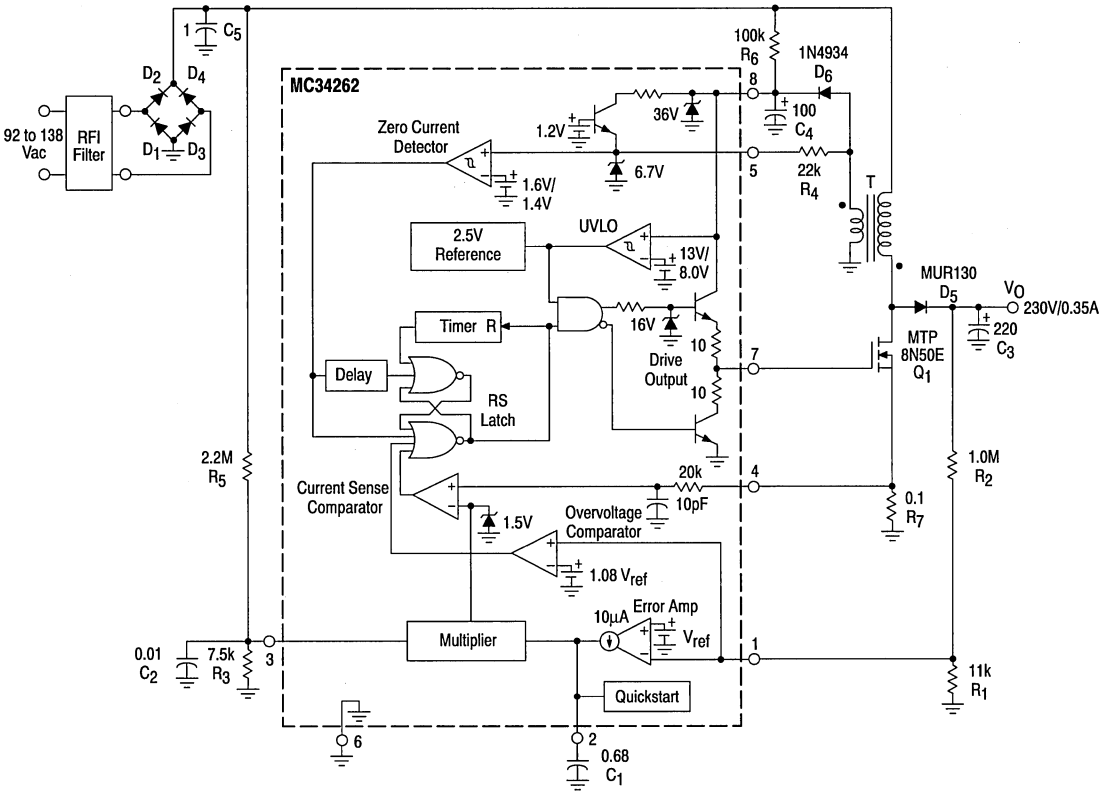
Table 1. Design Equations

Calculation	Formula	Notes
Required Converter Output Power	$P_O = V_O I_O$	Calculate the maximum required output power.
Peak Inductor Current	$I_{L(pk)} = \frac{2\sqrt{2}\,P_O}{\eta Vac_{(LL)}}$	Calculated at the minimum required AC line voltage for output regulation. Let the efficiency $\eta = 0.92$ for low line operation.
Inductance	$L_P = \frac{t\left(\frac{V_O}{\sqrt{2}} - Vac_{(LL)}\right)\eta\, Vac_{(LL)}^2}{\sqrt{2}\,V_O\,P_O}$	Let the switching cycle t = 40 μs for universal input (85 to 265 Vac) operation and 20 μs for fixed input (92 to 138 Vac, or 184 to 276 Vac) operation.
Switch On-Time	$t_{on} = \frac{2\,P_O\,L_P}{\eta\, Vac^2}$	In theory the on-time t_{on} is constant. In practice t_{on} tends to increase at the AC line zero crossings due to the charge on capacitor C_5. Let $Vac = Vac_{(LL)}$ for initial t_{on} and t_{off} calculations.
Switch Off-Time	$t_{off} = \frac{t_{on}}{\frac{V_O}{\sqrt{2}\,Vac\,\lvert Sin\,\theta\rvert} - 1}$	The off-time t_{off} is greatest at the peak of the AC line voltage and approaches zero at the AC line zero crossings. Theta (θ) represents the angle of the AC line voltage.
Switching Frequency	$f = \frac{1}{t_{on} + t_{off}}$	The minimum switching frequency occurs at the peak of the AC line voltage. As the AC line voltage traverses from peak to zero, t_{off} approaches zero producing an increase in switching frequency.
Peak Switch Current	$R_7 = \frac{V_{CS}}{I_{L(pk)}}$	Set the current sense threshold V_{CS} to 1.0 V for universal input (85 Vac to 265 Vac) operation and to 0.5 V for fixed input (92 Vac to 138 Vac, or 184 Vac to 276 Vac) operation. Note that V_{CS} must be <1.4 V.
Multiplier Input Voltage	$V_M = \frac{Vac\,\sqrt{2}}{\left(\frac{R_5}{R_3} + 1\right)}$	Set the multiplier input voltage V_M to 3.0 V at high line. Empirically adjust V_M for the lowest distortion over the AC line voltage range while guaranteeing start-up at minimum line.
Converter Output Voltage	$V_O = V_{ref}\left(\frac{R_2}{R_1} + 1\right) - I_{IB}\,R_1$	The $I_{IB}\,R_1$ error term can be minimized with a divider current in excess of 50 μA.
Converter Output Peak to Peak Ripple Voltage	$\Delta V_{O(p\text{-}p)} = I_O\sqrt{\left(\frac{1}{2\pi f_{ac}\,C_3}\right)^2 + ESR^2}$	The calculated peak-to-peak ripple must be less than 16% of the average DC output voltage to prevent false tripping of the Overvoltage Comparator. Refer to the Overvoltage Comparator text. ESR is the equivalent series resistance of C_3
Error Amplifier Bandwidth	$BW = \frac{gm}{2\,\pi\,C_1}$	The bandwidth is typically set to 20 Hz. When operating at high AC line, the value of C_1 may need to be increased. (See Figure 25)

The following converter characteristics must be chosen:

V_O — Desired output voltage
I_O — Desired output current
Vac — AC RMS operating line voltage
$Vac_{(LL)}$ — AC RMS minimum required operating line voltage for output regulation
ΔV_O — Converter output peak-to-peak ripple voltage

Figure 19. 80 W Power Factor Controller



Power Factor Controller Test Data

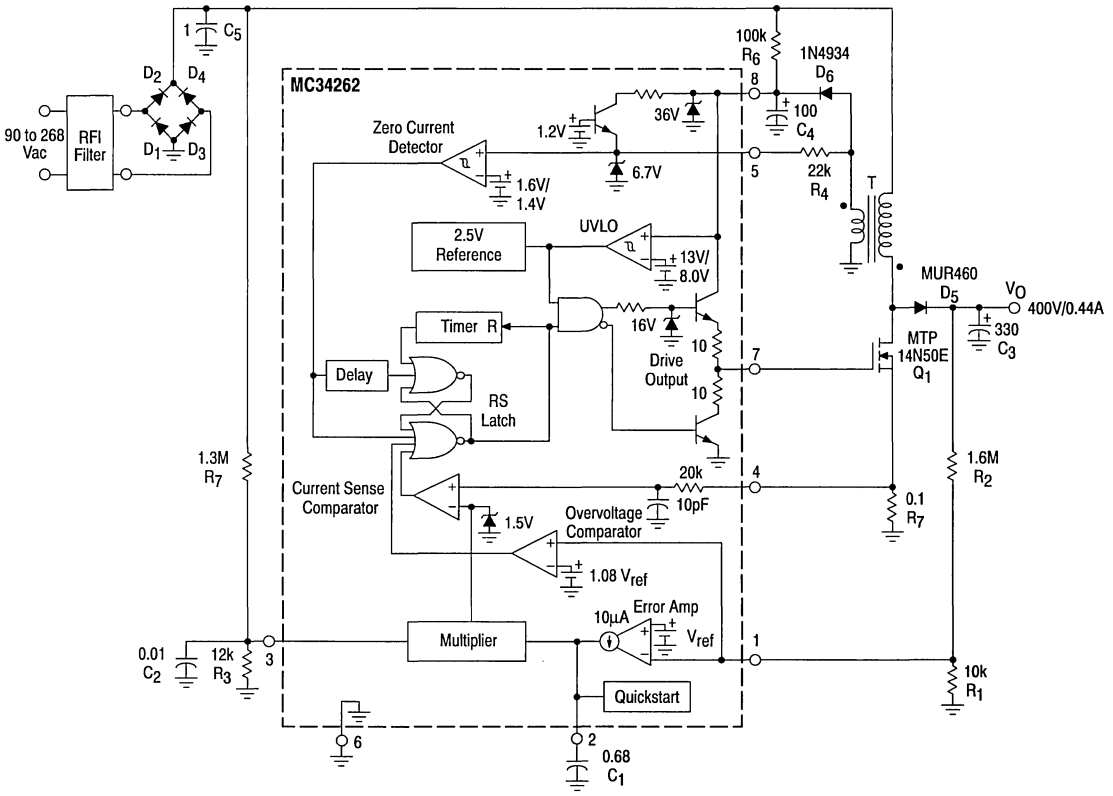
AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	P_{in}	PF	I_{fund}	THD	2	3	5	7	$V_{O(p-p)}$	V_O	I_O	P_O	η(%)
90	85.9	0.999	0.93	2.6	0.08	1.6	0.84	0.95	4.0	230.7	0.350	80.8	94.0
100	85.3	0.999	0.85	2.3	0.13	1.0	1.2	0.73	4.0	230.7	0.350	80.8	94.7
110	85.1	0.998	0.77	2.2	0.10	0.58	1.5	0.59	4.0	230.7	0.350	80.8	94.9
120	84.7	0.998	0.71	3.0	0.09	0.73	1.9	0.58	4.1	230.7	0.350	80.8	95.3
130	84.4	0.997	0.65	3.9	0.12	1.7	2.2	0.61	4.1	230.7	0.350	80.8	95.7
138	84.1	0.996	0.62	4.6	0.16	2.4	2.3	0.60	4.1	230.7	0.350	80.8	96.0

This data was taken with the test set-up shown in Figure 24.

T = Coilcraft N2881-A
Primary: 62 turns of # 22 AWG
Secondary: 5 turns of # 22 AWG
Core: Coilcraft PT2510, EE 25
Gap: 0.072″ total for a primary inductance (L_P) of 320 µH

Heatsink = AAVID Engineering Inc. 590302B03600, or 593002B03400

Figure 20. 175 W Universal Input Power Factor Controller



Power Factor Controller Test Data

AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	P_{in}	PF	I_{fund}	THD	2	3	5	7	$V_{O(p-p)}$	V_O	I_O	P_O	η(%)
90	193.3	0.991	2.15	2.8	0.18	2.6	0.55	1.0	3.3	402.1	0.44	176.9	91.5
120	190.1	0.998	1.59	1.6	0.10	1.4	0.23	0.72	3.3	402.1	0.44	176.9	93.1
138	188.2	0.999	1.36	1.2	0.12	1.3	0.65	0.80	3.3	402.1	0.44	176.9	94.0
180	184.9	0.998	1.03	2.0	0.10	0.49	1.2	0.82	3.4	402.1	0.44	176.9	95.7
240	182.0	0.993	0.76	4.4	0.09	1.6	2.3	0.51	3.4	402.1	0.44	176.9	97.2
268	180.9	0.989	0.69	5.9	0.10	2.3	2.9	0.46	3.4	402.1	0.44	176.9	97.8

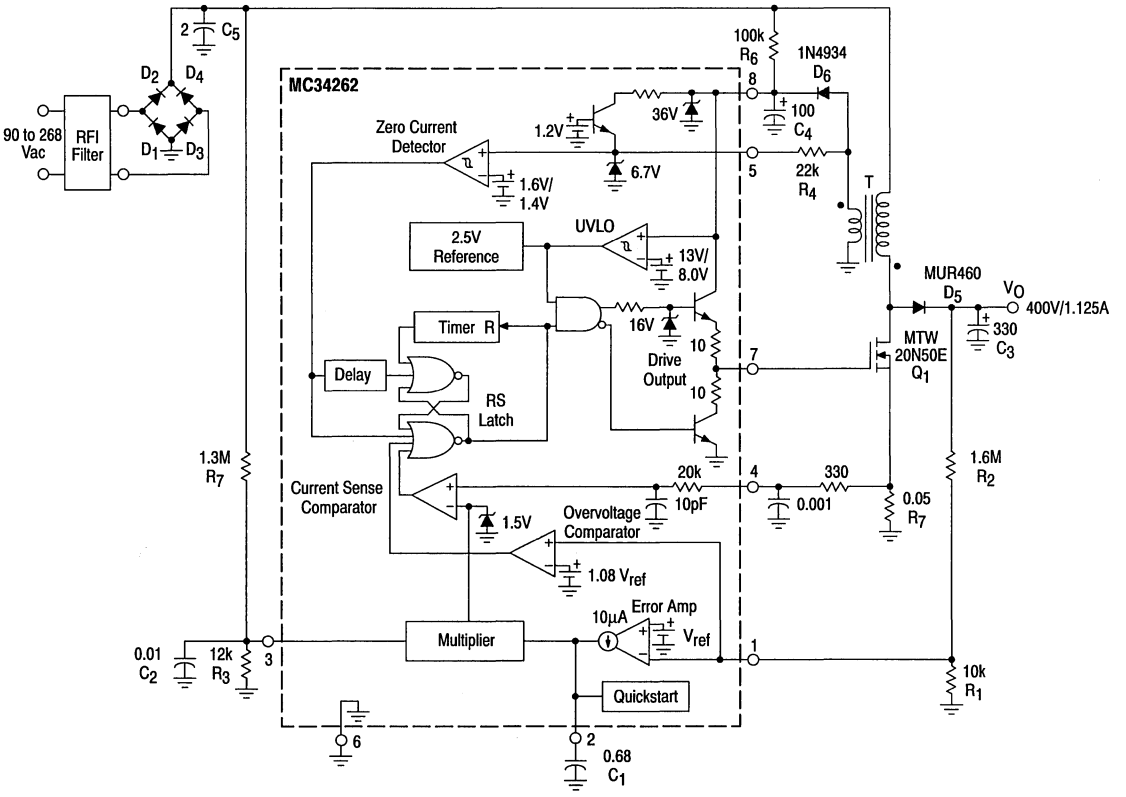
This data was taken with the test set-up shown in Figure 24.

T = Coilcraft N2880-A
Primary: 78 turns of # 16 AWG
Secondary: 6 turns of # 18 AWG
Core: Coilcraft PT4215, EE 42-15
Gap: 0.104″ total for a primary inductance (L_P) of 870 µH

Heatsink = AAVID Engineering Inc. 590302B03600

3

Figure 21. 450 W Universal Input Power Factor Controller



Power Factor Controller Test Data

AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	P_{in}	PF	I_{fund}	THD	2	3	5	7	$V_{O(p-p)}$	V_O	I_O	P_O	η(%)
90	489.5	0.990	5.53	2.2	0.10	1.5	0.25	0.83	8.8	395.5	1.14	450.9	92.1
120	475.1	0.998	3.94	2.5	0.12	0.29	0.62	0.52	8.8	395.5	1.14	450.9	94.9
138	470.6	0.998	3.38	2.1	0.06	0.70	1.1	0.41	8.8	395.5	1.14	450.9	95.8
180	463.4	0.998	2.57	4.1	0.21	2.0	1.6	0.71	8.9	395.5	1.14	450.9	97.3
240	460.1	0.996	1.91	4.8	0.14	4.3	2.2	0.63	8.9	395.5	1.14	450.9	98.0
268	459.1	0.995	1.72	5.8	0.10	5.0	2.5	0.61	8.9	395.5	1.14	450.9	98.2

This data was taken with the test set-up shown in Figure 24.

T = Coilcraft P3657-A
Primary: 38 turns Litz wire, 1300 strands of #48 AWG, Kerrigan-Lewis, Chicago, IL.
Secondary: 3 turns of # 20 AWG
Core: Coilcraft PT4220, EE 42-20
Gap: 0.180″ total for a primary inductance (L_P) of 190 µH

Heatsink = AAVID Engineering Inc. 604953B04000 Extrusion

Figure 22. Power Factor Corrected Input Waveforms (Figure 20 Circuit)

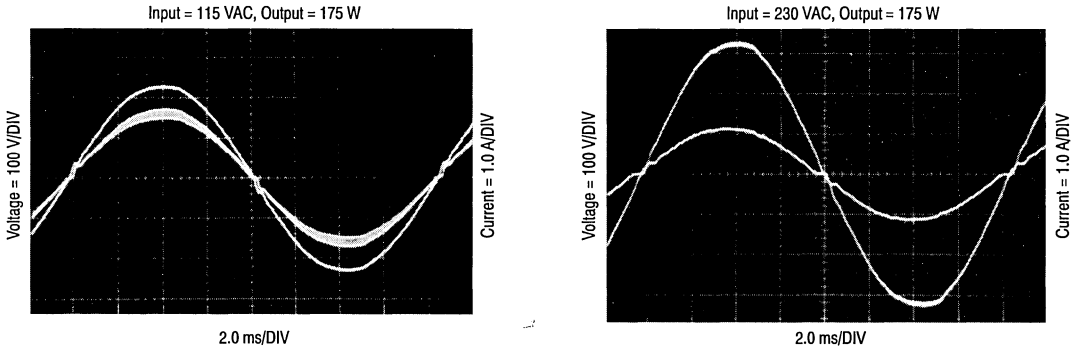


Figure 23. Output Voltage Start-Up Overshoot (Figure 20 Circuit)

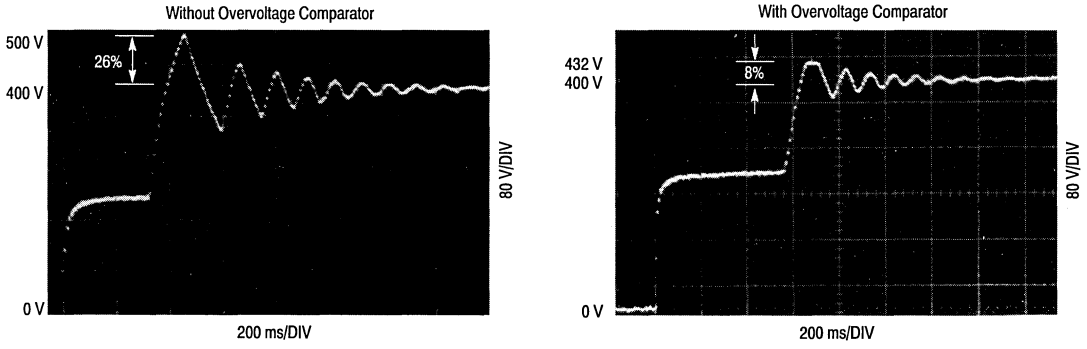
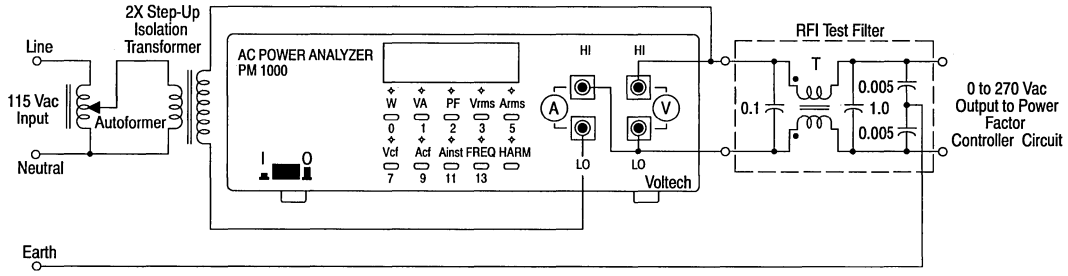
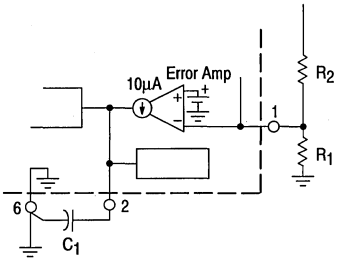


Figure 24. Power Factor Test Set-Up



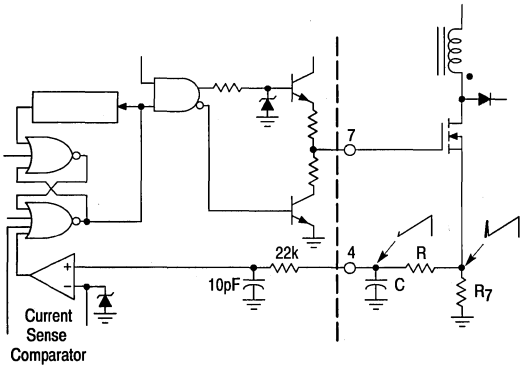
An RFI filter is required for best performance when connecting the preconverter directly to the AC line. The filter attenuates the level of high frequency switching that appears on the AC line current waveform. Figures 19 and 20 work well with commercially available two stage filters such as the Delta Electronics 03DPCG5. Shown above is a single stage test filter that can easily be constructed with four AC line rated capacitors and a common-mode transformer. Coilcraft CMT3-28-2 was used to test Figures 19 and 20. It has a minimum inductance of 28 mH and a maximum current rating of 2.0 A. Coilcraft CMT4-17-9 was used to test Figure 21. It has a minimum inductance of 17 mH and a maximum current rating of 9.0 A. Circuit conversion efficiency η (%) was calculated without the power loss of the RFI filter.

Figure 25. Error Amp Compensation



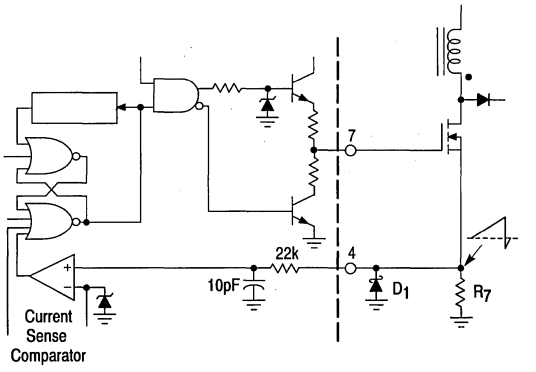
The Error Amp output is a high impedance node and is susceptible to noise pickup. To minimize pickup, compensation capacitor C_1 must be connected as close to Pin 2 as possible with a short, heavy ground returning directly to Pin 6. When operating at high AC line, the voltage at Pin 2 may approach the lower threshold of the Multiplier, ≈ 2.0 V. If there is excessive ripple on Pin 2, the Multiplier will be driven into cut-off causing circuit instability, high distortion and poor power factor. This problem can be eliminated by increasing the value of C_1.

Figure 26. Current Waveform Spike Suppression



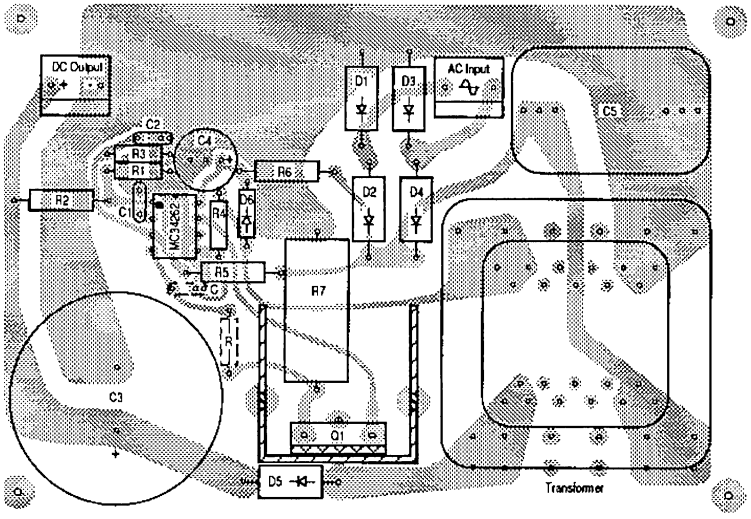
A narrow turn-on spike is usually present on the leading edge of the current waveform and can cause circuit instability. The MC34262 provides an internal RC filter with a time constant of 220 ns. An additional external RC filter may be required in universal input applications that are above 200 W. It is suggested that the external filter be placed directly at the Current Sense Input and have a time constant that approximates the spike duration.

Figure 27. Negative Current Waveform Spike Suppression

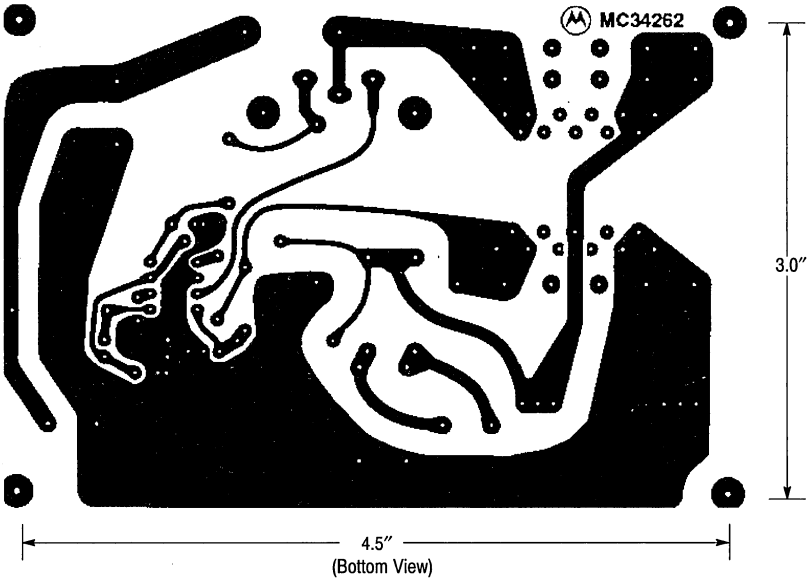


A negative turn-off spike can be observed on the trailing edge of the current waveform. This spike is due to the parasitic inductance of resistor R_7, and if it is excessive, it can cause circuit instability. The addition of Shottky diode D_1 can effectively clamp the negative spike. The addition of the external RC filter shown in Figure 26 may provide sufficient spike attenuation.

Figure 28. Printed Circuit Board and Component Layout (Circuits of Figures 15 and 16)



(Top View)



(Bottom View)

NOTE: Use 2 oz. copper laminate for optimum circuit performance.

MC34268

3

Advance Information

SCSI-2 Active Terminator Regulator Series

SCSI-2
THREE-TERMINAL
VOLTAGE REGULATOR

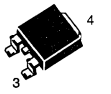
SILICON MONOLITHIC
INTEGRATED CIRCUIT

The MC34268 is a medium current, low dropout positive voltage regulator specifically designed for use in SCSI-2 active termination circuits. This device offers the circuit designer an economical solution for precision voltage regulation, while keeping power losses to a minimum. The regulator consists of a 1.0 V dropout composite PNP/NPN pass transistor, current limiting, and thermal limiting. These devices are packaged in the 8-pin SOP-8 and 3-pin DPAK surface mount power packages.

Applications include active SCSI-2 terminators and post regulation of switching power supplies.

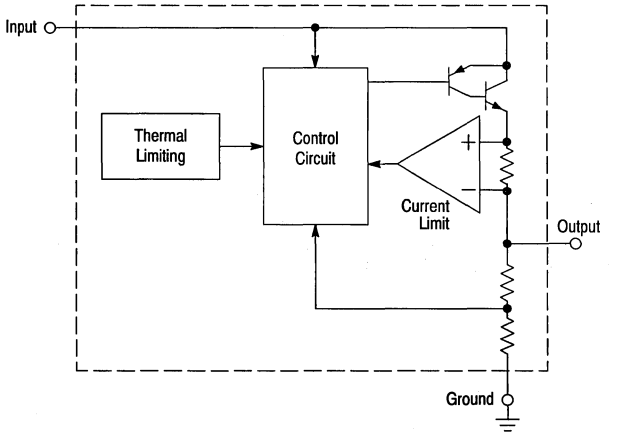
- 2.85 V Output Voltage for SCSI-2 Active Termination
- Space Saving DPAK and SOP-8 Surface Mount Power Packages
- 1.0 V Dropout
- Output Current in Excess of 800 mA
- Thermal Protection
- Short Circuit Protection
- Output Trimmed to 1.4% Tolerance
- No Minimum Load Required

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP-8)

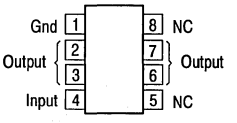


DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

Pin 1. Ground
2. Output
3. Input
4. Output

(Top View)

ORDERING INFORMATION

Device	Tested Operating Junction Temperature Range	Package
MC34268D	0 to +125°C	SOP-8
MC34268DT		DPAK

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{in}	15	V
Power Dissipation and Thermal Characteristics			
DT Suffix, Plastic Package, Case 369A			
T_A = 25°C, Derate Above T_A = 25°C	P_D	Internally Limted	W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	5.0	°C/W
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	87	°C/W
D Suffix, Plastic Package, Case 751			
T_A = 25°C, Derate Above T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	22	°C/W
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	140	°C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Storage Temperature	T_{stg}	– 55 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{in} = 4.25 V, C_O = 10 µF, for typical values T_J = 25°C, for min/max values T_J = 0°C to +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C, I_O = 0 mA) Output Voltage, over Line, Load, and Temperature (V_{in} = 3.9 V to 15 V, I_O = 0 mA to 490 mA)	V_O	2.81 2.76	2.85 2.85	2.89 2.93	V
Line Regulation (V_{in} = 4.25 V to 15 V, I_O = 0 mA, T_J = 25°C)	Reg_{line}	—	—	0.3	%
Load Regulation (I_O = 0 mA to 800 mA, T_J = 25°C)	Reg_{load}	—	—	0.5	%
Dropout Voltage (I_O = 490 mA)	$V_{in} - V_O$	—	0.95	1.1	V
Ripple Rejection (f = 120 Hz)	RR	55	—	—	dB
Maximum Output Current (V_{in} = 5.0 V)	$I_{(max)}$	800	—	—	mA
Bias Current (V_{in} = 4.25 V, I_O = 0 mA)	I_B	—	5.0 to 3.0	8.0	mA
Minimum Load Current to maintain Regulation (V_{in} = 15 V)	$I_{L(min)}$	—	—	0	mA

Figure 1. Dropout Voltage versus Output Load Current

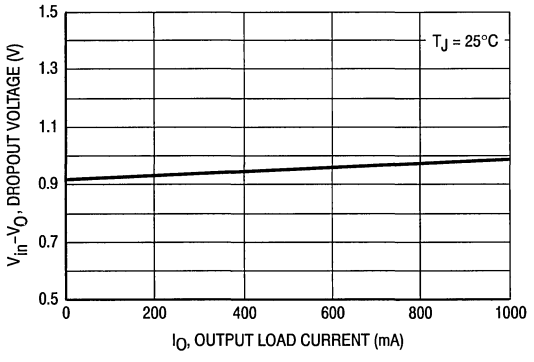


Figure 2. Transient Load Regulation

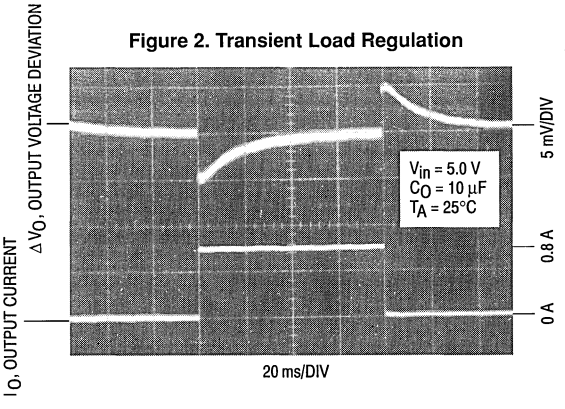


Figure 3. Typical SCSI Application

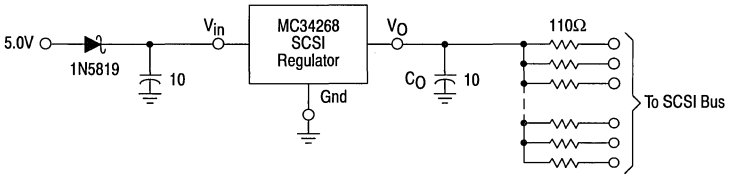


Figure 3 is a circuit of a typical SCSI terminator application. The MC34268 is designed specifically to provide 2.85 V required to drive a SCSI-2 bus. The output current capability of the regulator is in excess of 800 mA; enough to drive standard SCSI-2, fast SCSI-2, and some wide SCSI-2 applications. The typical dropout voltage is less than 1.0 V, allowing the IC to regulate to input voltages less than 4.0 V. Internal protective features include current and thermal limiting.

The MC34268 requires an external 10 μF capacitor with an ESR of less than 10 Ω for stability over temperature. With economical electrolytic capacitors, cold temperature operation can pose a stability problem. As temperature decreases, the capacitance also decreases and the ESR increases, which could cause the circuit to oscillate. Tantalum capacitors may be a better choice if small size is a requirement. Also, the capacitance and ESR of a tantalum capacitor is more stable over temperature.

Figure 4. SOP-8 Thermal Resistance versus P.C.B. Copper Length

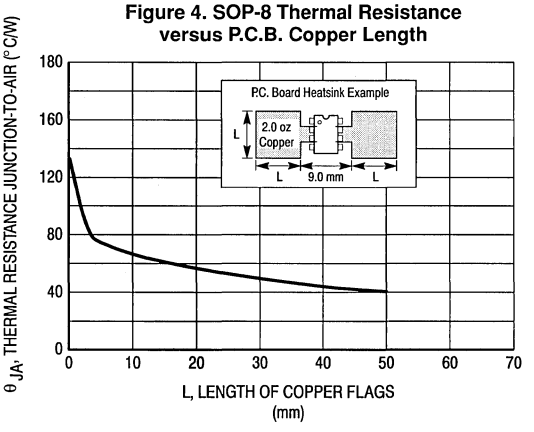
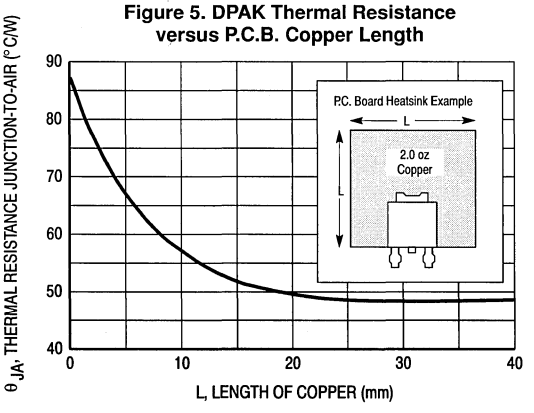


Figure 5. DPAK Thermal Resistance versus P.C.B. Copper Length



MC34360

Product Preview

High Voltage Switching Integrated Controller

HIGH VOLTAGE SWITCHING CONTROLLER

HIGH VOLTAGE MONOLITHIC INTEGRATED CIRCUIT

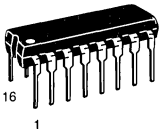
The MC34360 is a high performance, high voltage switching current regulator designed for off-line battery charger applications that utilize frequency modulated constant off-time or constant dead-time control.

This integrated circuit features a 500 V power SENSEFET, two independent programmable references: one controls peak switch current and fast charge current; the other controls the programmable timer and trickle charge current. Also included is a temperature compensated reference, a 4096 bit counter and a charge indicator output.

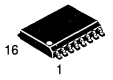
Protective features include input undervoltage lockout, input overvoltage protection, short circuit protection, and thermal shutdown.

This device is available in a dual-in-line and a surface mount package.

- 500 V, 300 mA Power SENSEFET
- Direct Off-Line Operation from 120 Vac
- Switching Current Regulator
- Programmable Time-Out
- Selectable 2 Different Power Levels
- Internal Thermal Shutdown
- Internal Current Limiting
- Overvoltage Protection
- LED Output Indicator

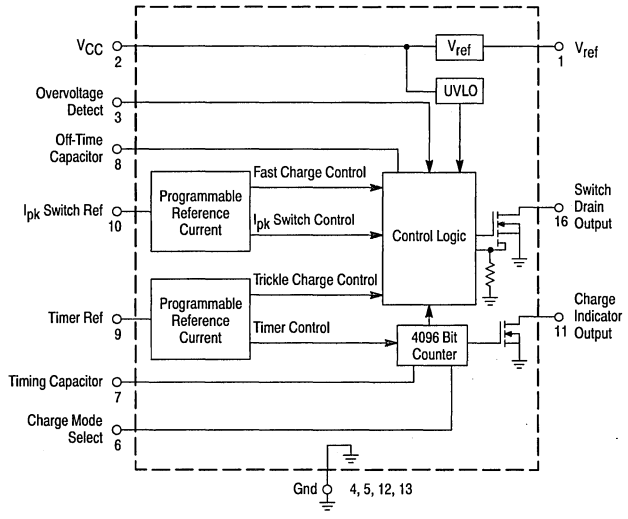


P SUFFIX
PLASTIC PACKAGE
CASE 648C

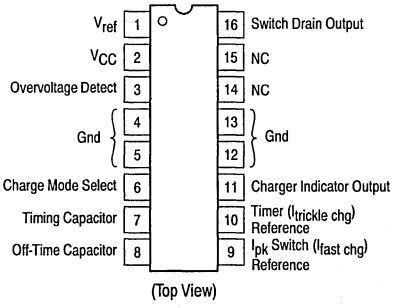


DW SUFFIX
PLASTIC PACKAGE
CASE 751G
SOP(12+2+2)L

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34360DW	0° to +70°C	SO-16L
MC34360P		Plastic DIP

MC34361

3

Product Preview

High Voltage Switching Integrated Controller

The MC34361 is a high performance, high voltage switching current regulator designed for off-line battery charger applications that utilize frequency modulated constant off-time or constant dead-time control.

This integrated circuit features a 800 V power SENSEFET, two independent programmable references: one controls peak switch current and fast charge current; the other controls the programmable timer and trickle charge current. Also included is a temperature compensated reference, a 4096 bit counter and a charge indicator output.

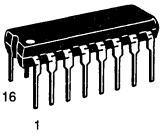
Protective features include input undervoltage lockout, input overvoltage protection, short circuit protection, and thermal shutdown.

This device is available in a dual-in-line and a surface mount package.

- 800 V, 300 mA Power SENSEFET
- Direct Off-Line Operation from 240 Vac
- Switching Current Regulator
- Programmable Time-Out
- Selectable 2 Different Power Levels
- Internal Thermal Shutdown
- Internal Current Limiting
- Overvoltage Protection
- LED Output Indicator

HIGH VOLTAGE SWITCHING CONTROLLER

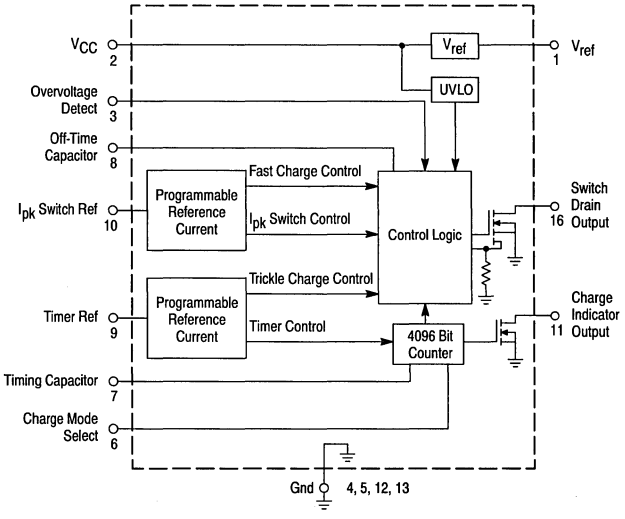
HIGH VOLTAGE MONOLITHIC INTEGRATED CIRCUIT



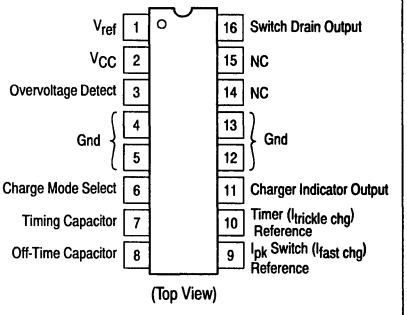
P SUFFIX
PLASTIC PACKAGE
CASE 648C

DW SUFFIX
PLASTIC PACKAGE
CASE 751G
SOP(12+2+2)L

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34361DW	0° to +70°C	SO-16L
MC34361P		Plastic DIP

MC44602

Advance Information

High Performance Current Mode Controller

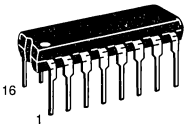
HIGH PERFORMANCE CURRENT MODE CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC44602 is an enhanced high performance fixed frequency current mode controller that is specifically designed for off-line and high voltage DC-to-DC converter applications. This device has the unique ability of changing operating modes if the converter output is overloaded or shorted, offering the designer additional protection for increased system reliability. The MC44602 has several distinguishing features when compared to conventional current mode controllers. These features consist of a foldback amplifier for overload detection, valid load and demag comparators with a fault latch for short circuit detection, thermal shutdown, and separate high current source and sink outputs that are ideally suited for driving a high voltage bipolar power transistor, such as the MJE18002, MJE18004, or MJE18006.

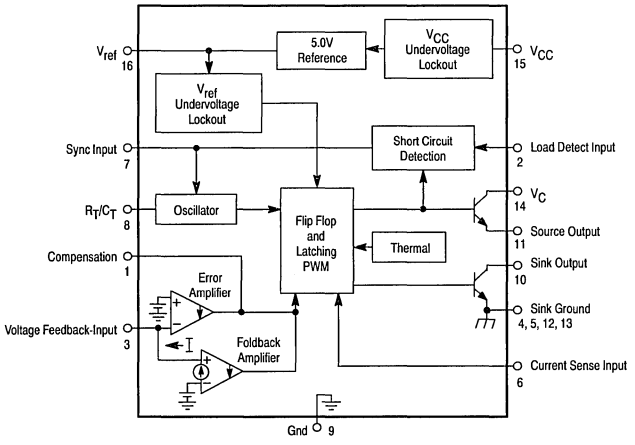
Standard features include an oscillator with a sync input, a temperature compensated reference, high gain error amplifier, and a current sensing comparator. Protective features consist of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, a latch for single pulse metering, and a flip-flop which blanks the output off every other oscillator cycle, allowing output deadtimes to be programmed from 50% to 70%. This device is manufactured in a 16 pin dual-in-line heat tab package for improved thermal conduction.

- Separate High Current Source and Sink Outputs Ideally Suited for Driving Bipolar Power Transistors: 1.0 A Source, 1.5 A Sink
- Unique Overload and Short Circuit Protection
- Thermal Protection
- Oscillator with Sync Input
- Current Mode Operation to 500 kHz Output Switching Frequency
- Output Deadtime Adjustable from 50% to 70%
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Input and Reference Undervoltage Lockouts with Hysteresis
- Low Start-Up and Operating Current

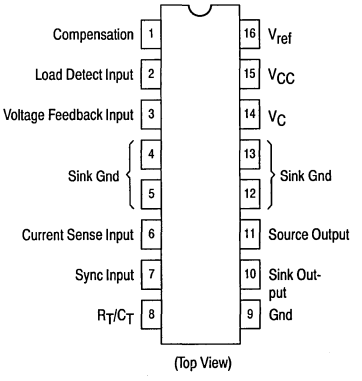


P2 SUFFIX
PLASTIC PACKAGE
CASE 648C

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Sink Ground Voltage with Respect to Gnd (Pin 9)	$V_{Sink(neg)}$	–5.0	V
Output Supply Voltage with Respect to Sink Gnd (Pins 4, 5, 12, 13)	V_C	20	V
Output Current (Note 1)			A
Source	$I_{O(Source)}$	1.0	
Sink	$I_{O(Sink)}$	1.5	
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	–0.3 to 5.5	V
Sync Input			
High State Voltage	V_{IH}	5.5	V
Low State Reverse Current	I_{IL}	–20	mA
Load Detect Input Current	I_{in}	–20 to +10	mA
Error Amplifier Output Sink Current	$I_{EA\ (Sink)}$	10	mA
Power Dissipation and Thermal Characteristics			
Maximum Power Dissipation at T_A = 25°C	P_D	2.5	W
Thermal Resistance Junction to Air	$R_{\theta JA}$	80	°C/W
Thermal Resistance Junction to Case	$R_{\theta JC}$	15	°C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	–25 to +85	°C

NOTE: 1. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS

(V_{CC} and V_C = 12 V [Note 2], R_T = 10k, C_T = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A = –25°C to +85°C [Note 3] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION					
Voltage Feedback Input (V_O = 2.5V)	V_{FB}	2.45	2.5	2.65	V
Input Bias Current (V_{FB} = 2.5 V)	I_{IB}	—	–0.6	–2.0	μA
Open-Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	—	dB
Unity Gain Bandwidth	BW				MHz
T_J = 25°C		1.0	1.4	1.8	
T_A = –25 to +85°C		0.8	—	2.0	
Power Supply Rejection Ratio (V_{CC} = 10 V to 16 V)	PSRR	65	70	—	dB
Output Current					mA
Sink (V_O = 1.5 V, V_{FB} = 2.7 V)	I_{Sink}				
T_J = 25°C		—	5.0	—	
T_A = –25 to +85°C		1.5	—	10	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)					
T_J = 25°C	I_{Source}				
T_A = –25 to +85°C		—	–1.1	—	
		–2.0	—	–0.2	
Output Voltage Swing					V
High State ($I_{O(Source)}$ = 0.5 mA, V_{FB} = 2.3 V)	V_{OH}	6.0	7.0	—	
Low State ($I_{O(Sink)}$ = 0.33 mA, V_{FB} = 2.7 V)	V_{OL}	—	1.0	1.1	

NOTES: 2. Adjust V_{CC} above the start-up threshold before setting to 12V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V [Note 2], R_T = 10k, C_T = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A = –25°C to +85°C [Note 3] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR SECTION					
Frequency T_J = 25°C T_A = –25°C to +85°C	f_{OSC}	 168 160	 180 —	 192 200	kHz
Frequency Change with Voltage (V_{CC} = 12 V to 18 V)	$\Delta f_{OSC}/\Delta V$	—	0.1	0.2	%/V
Frequency Change with Temperature	$\Delta f_{OSC}/\Delta T$	—	0.05	—	%/°C
Oscillator Voltage Swing (Peak-to-Peak)	$V_{OSC(p-p)}$	1.3	1.6	—	V
Discharge Current (V_{OSC} = 3.0 V) T_J = 25°C T_A = –25°C to +85°C	I_{dischg}	 6.5 6.0	 10 —	 13.5 14	mA
Sync Input Threshold Voltage High State Low State	 V_{IH} V_{IL}	 2.5 1.0	 2.8 1.3	 3.2 1.7	V
Sync Input Resistance T_J = 25°C T_A = –25°C to +85°C	R_{in}	 6.5 6.0	 10 —	 13.5 18	kΩ
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA)	V_{ref}	4.7	5.0	5.3	V
Line Regulation (V_{CC} = 12 V to 18 V)	Reg_{line}	—	1.0	10	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	—	3.0	15	mV
Temperature Stability	T_S	—	0.2	—	mV/°C
Total Output Variation over Line, Load and Temperature	V_{ref}	4.65	—	5.35	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	—	50	—	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	—	5.0	—	mV
Output Short Circuit Current T_J = 25°C T_A = –25°C to +85°C	I_{SC}	 — –70	 –130 —	 — –180	mA
CURRENT SENSE SECTION					
Current Sense Input Voltage Gain (Notes 4 & 5) T_J = 25°C T_A = –25°C to +85°C	A_V	 2.85 2.7	 3.0 —	 3.15 3.2	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	V
Input Bias Current	I_{IB}	—	–4.0	–10	μA
Propagation Delay (Current Sense Input to Sink Output)	$t_{PLH(in/out)}$	—	100	150	ns
UNDERVOLTAGE LOCKOUT SECTIONS					
Start-Up Threshold (V_{CC} Increasing)	V_{th}	13	14.1	15	V
Minimum Operating Voltage After Turn-On (V_{CC} Decreasing)	$V_{CC(min)}$	9.0	10.2	11	V
Reference Undervoltage Threshold (V_{ref} Decreasing)	$V_{ref(UVLO)}$	3.0	3.35	3.7	V

NOTES: 4. This parameter is measured at the latch trip point with I_{FB} = –5.0 μA, refer to Figure 9.

5. Comparator gain is defined as $A_V = \frac{\Delta V \text{ Compensation}}{\Delta V \text{ Current Sense Input}}$

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V [Note 2], R_T = 10k, C_T = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A = –25°C to +85°C [Note 3] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT SECTION					
Output Voltage (T_A = 25°C)					V
Low State (I_{Sink} = 100 mA)	V_{OL}	—	0.6	0.3	
(I_{Sink} = 1.0A)		—	1.8	2.0	
(I_{Sink} = 1.5 A)		—	2.1	2.6	
High State (I_{Source} = 50 mA)	(V_{CC}–V_{OH})	—	1.4	1.7	
(I_{Source} = 0.5 A)		—	1.7	2.0	
(I_{Source} = 0.75 A)		—	1.8	2.2	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	—	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	—	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	—	50	150	ns
PWM SECTION					
Duty Cycle					%
Maximum	$DC_{(max)}$	46	48	50	
Minimum	$DC_{(min)}$	—	—	0	
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Start-Up (V_{CC} = 5 V)		—	0.2	0.5	
Operating (Note 2)					
T_J = 25° C		—	17	20	
T_A = –25°C to +85° C		10	—	22	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	18	20	23	V
OVERLOAD AND SHORT CIRCUIT PROTECTION					
Foldback Amplifier Threshold (Figures 9,10)	ΔV_{FB}	(V_{FB}–100)	(V_{FB}-200)	(V_{FB}-300)	mV
Load Detect Input					
Valid Load Comparator Threshold ($V_{Pin\ 2}$ Increasing)	$V_{th(VL)}$	2.0	2.5	3.0	V
Demag Comparator Threshold ($V_{Pin\ 2}$ Decreasing)	$V_{th(Demag)}$	50	88	120	mV
Propagation Delay (Input to Sink or Source Output)	$t_{PLH(in/out)}$	—	1.1	1.6	µS
Input Resistance	R_{in}	12	18	30	kΩ

NOTES: 2. Adjust V_{CC} above the start-up threshold before setting to 12V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Figure 1. Timing Resistor versus Oscillator Frequency

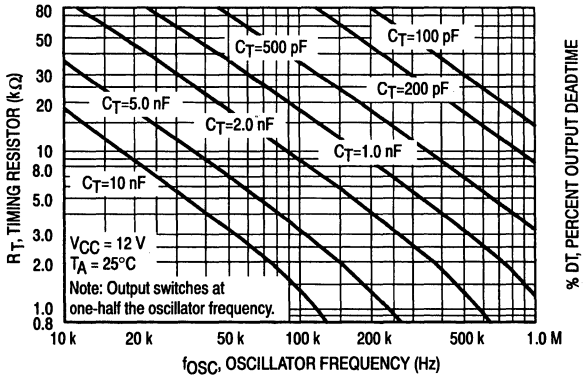


Figure 2. Output Deadtime versus Oscillator Frequency

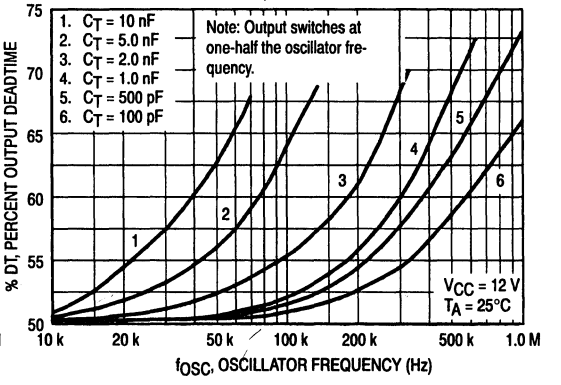


Figure 3. Oscillator Discharge Current versus Temperature

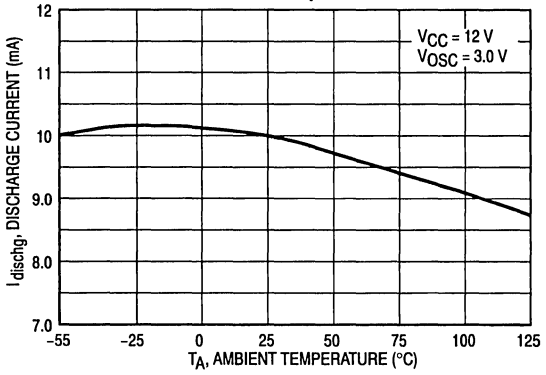


Figure 4. Oscillator Voltage Swing versus Temperature

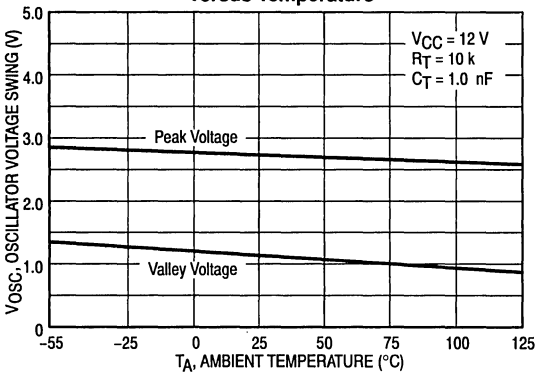


Figure 5. Error Amp Small Signal Transient Response

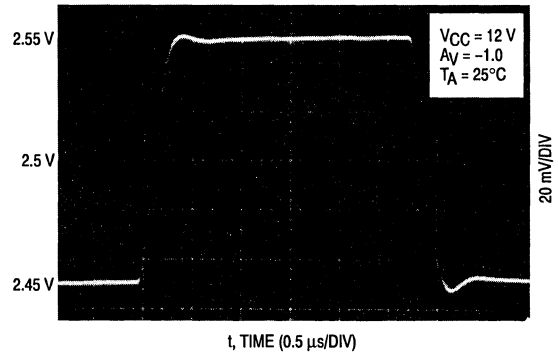


Figure 6. Error Amp Large Signal Transient Response

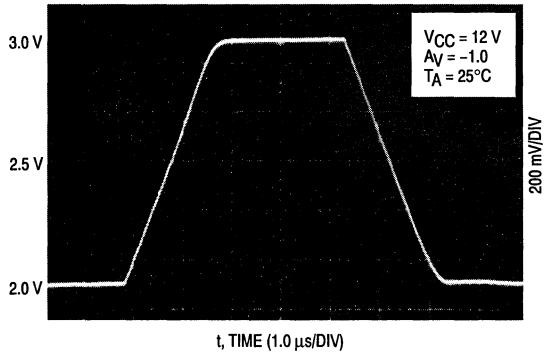


Figure 7. Error Amp Open-Loop Gain and Phase versus Frequency

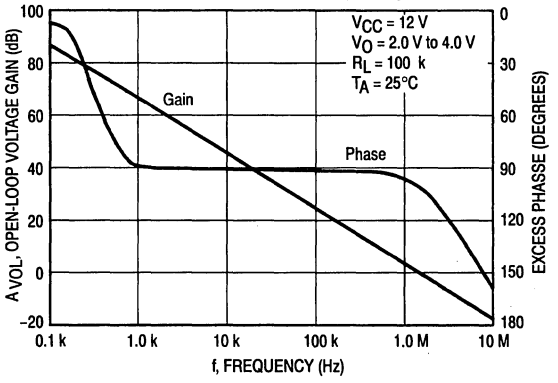


Figure 8. Current Sense Input Threshold versus Error Amp Output Voltage

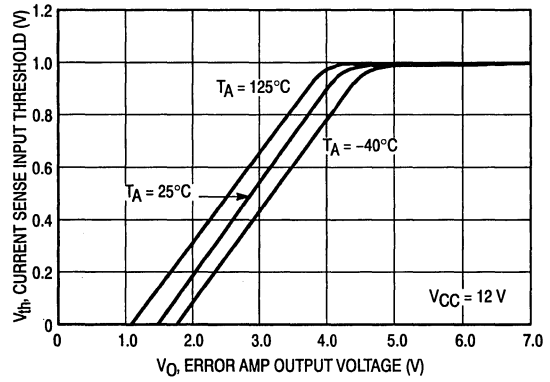


Figure 9. Voltage Feedback Input, Voltage versus Current

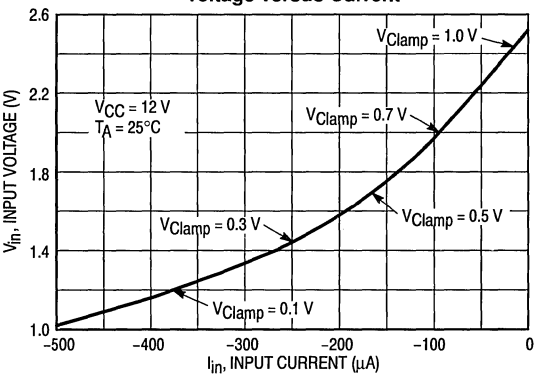


Figure 10. Voltage Feedback Input versus Current Sense Clamp Level

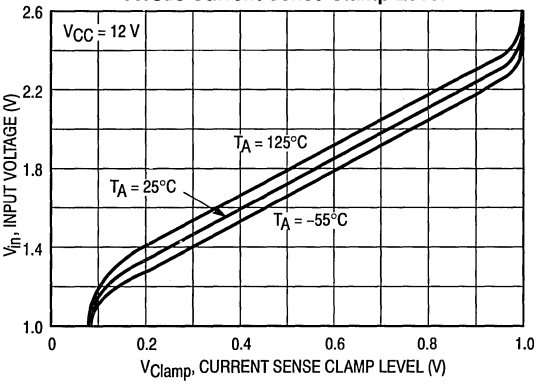


Figure 11. Reference Short Circuit Current versus Temperature

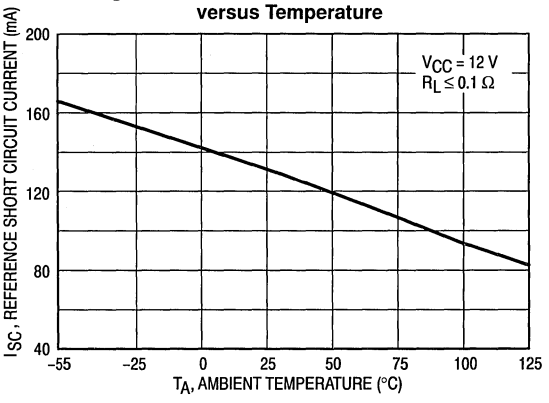


Figure 12. Reference Line and Load Regulation versus Temperature

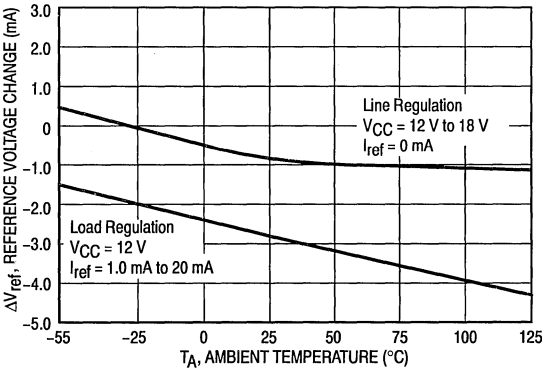


Figure 13. Reference Voltage Change versus Source Current

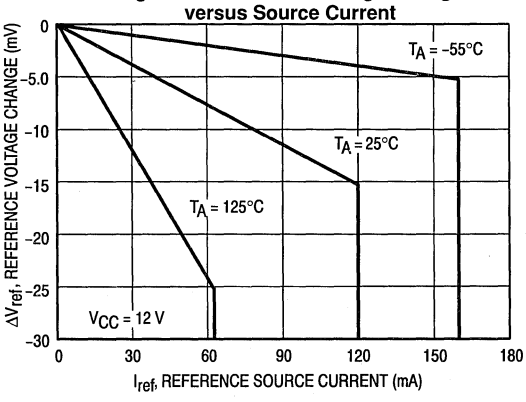


Figure 14. Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

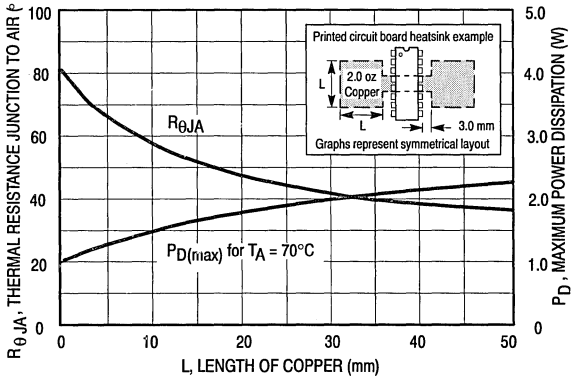


Figure 15. Output Waveform

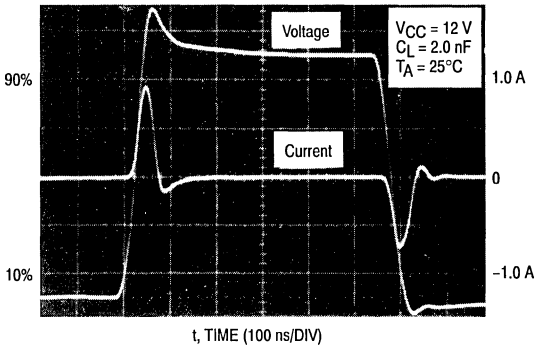


Figure 16. Output Cross Conduction

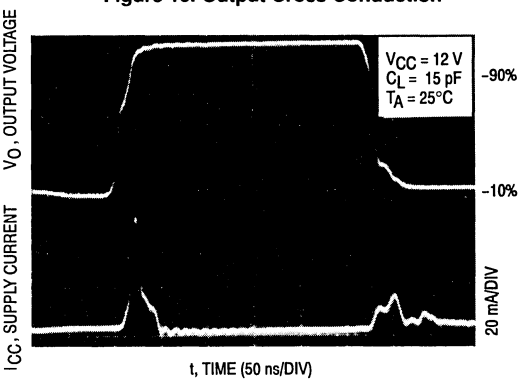


Figure 17. Sink Output Saturation Voltage versus Sink Current

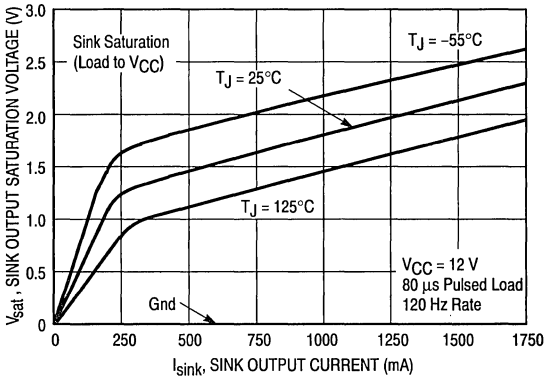


Figure 18. Source Output Saturation Voltage versus Load Current

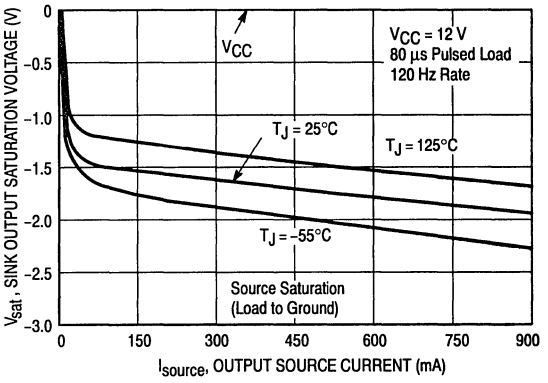


Figure 19. Supply Current versus Supply Voltage

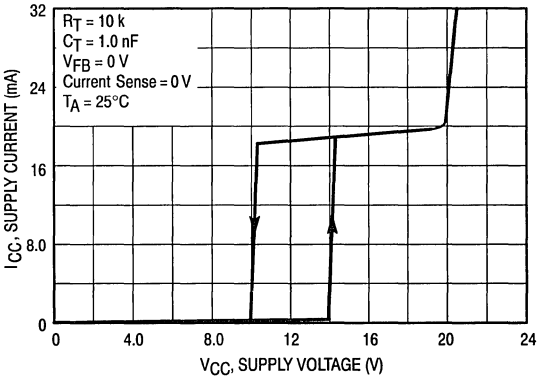


Figure 20. Power Supply Zener Voltage versus Temperature

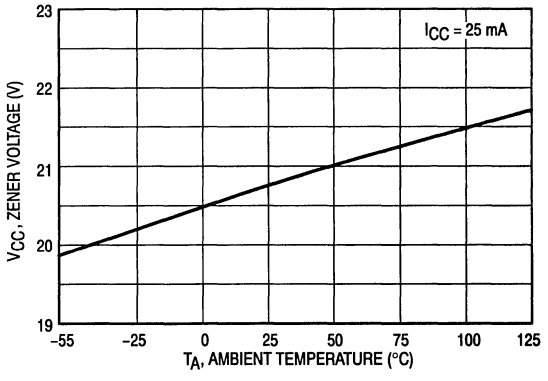


Figure 21. Valid Load Comparator Threshold versus Temperature

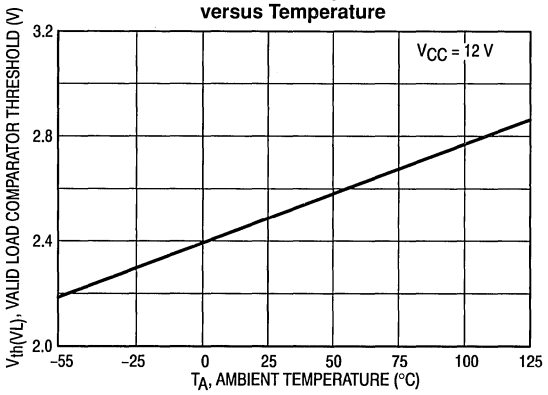


Figure 22. Demag Comparator Threshold versus Temperature

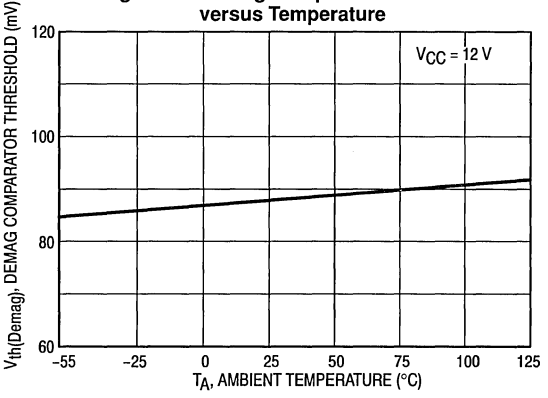


Figure 23. Load Detect Input Propagation Delay versus Temperature

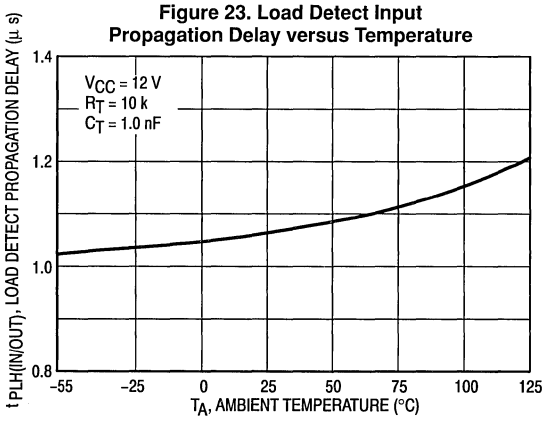


Figure 24. Start-Up Threshold Voltage versus Temperature

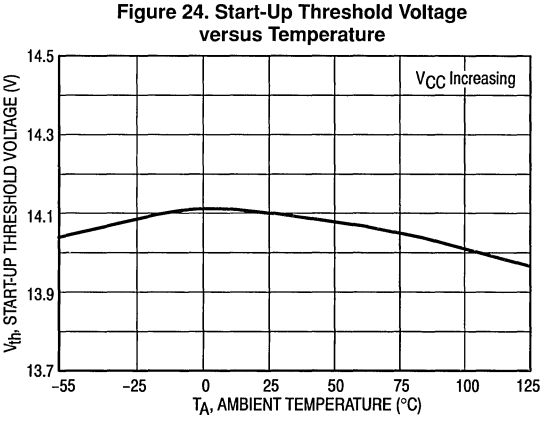


Figure 25. Minimum Operating Voltage After Turn-On versus Temperature

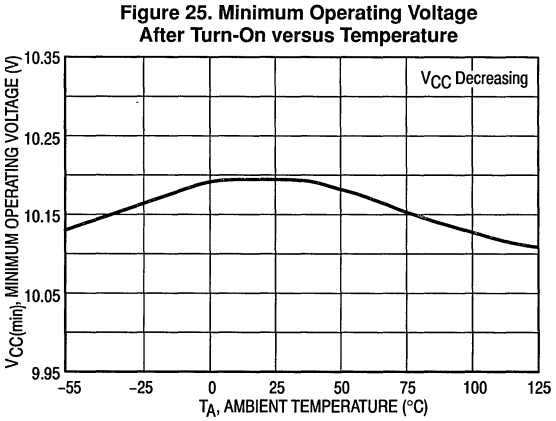


Figure 26. Reference Undervoltage Threshold versus Temperature

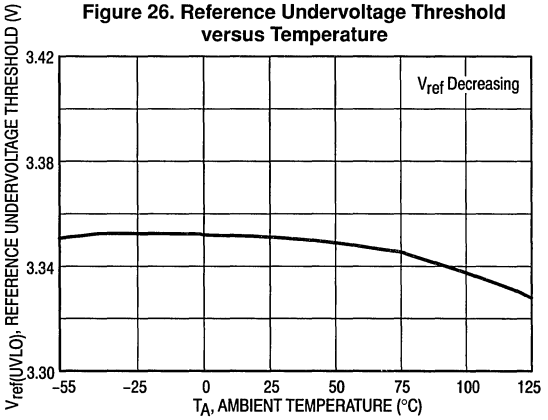


Figure 27. Representative Block Diagram

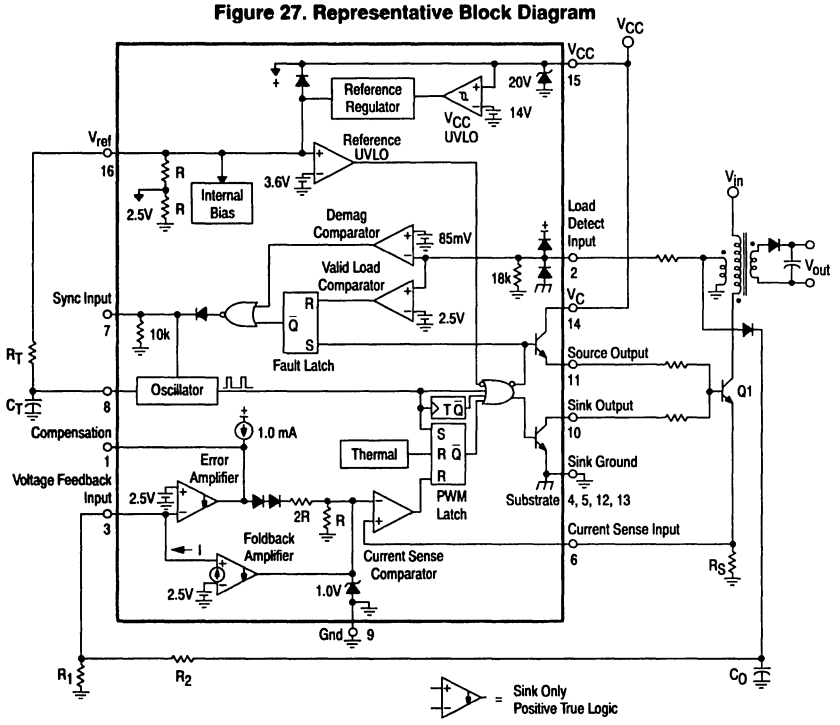
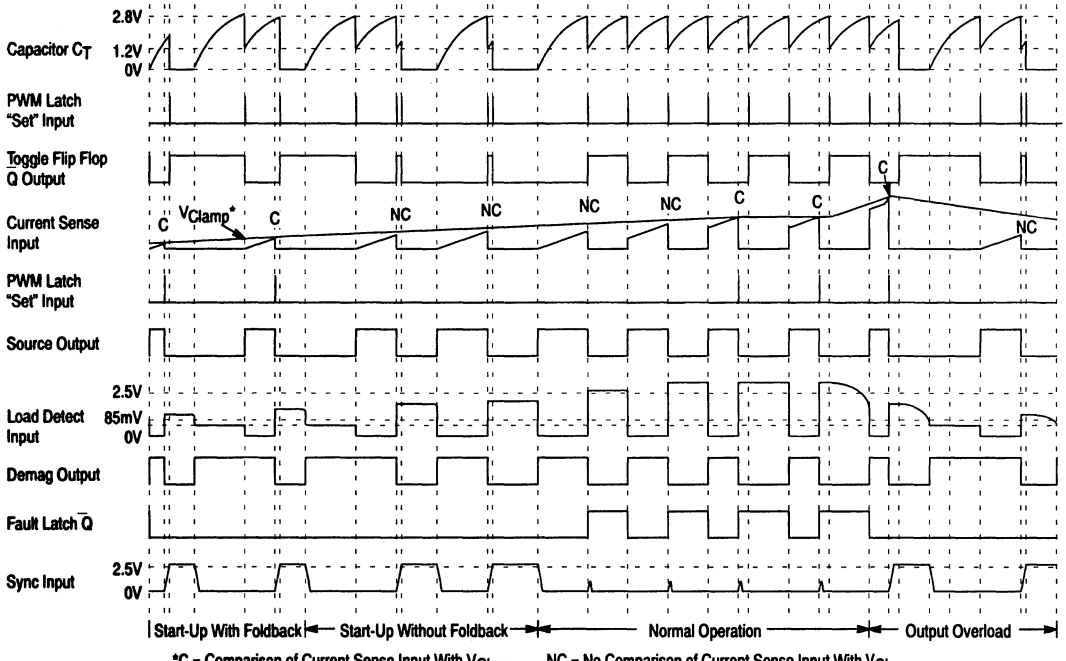


Figure 28. Timing Diagram



OPERATING DESCRIPTION

The MC44602 is a high performance, fixed frequency, current mode controller specifically designed to directly drive a bipolar power switch in off-line and high voltage DC-to-DC converter applications. This device offers the designer a cost effective solution with minimal external components. The representative block and timing diagrams are shown in Figures 27 and 28.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds one of the inputs of the NOR gate high. This causes the Source and Sink outputs to be in a low state, thus producing a controlled amount of output deadtime. An internal toggle flip-flop has been incorporated in the MC44602 which blanks the output off every other clock cycle by holding one of the inputs of the NOR gate high. This in combination with the C_T discharge period yields output deadtimes programmable from 50% to 70%. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for a given value of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency.

In many noise sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a narrow rectangular clock signal with an amplitude of 3.2 V to 5.5 V to the Sync Input (Pin 7). For reliable locking, the free-running oscillator frequency should be set about 10% less than the clock frequency. If the clock signal is AC coupled through a capacitor, an external clamp diode may be required if the negative sync input current is greater than –5.0 mA. Connecting Pin 7 to V_{ref} will cause C_T to discharge to 0 V, inhibiting the Oscillator and conduction of the Source Output. Multi-unit synchronization can be accomplished by connecting the C_T pin of each IC to a single MC1455 timer.

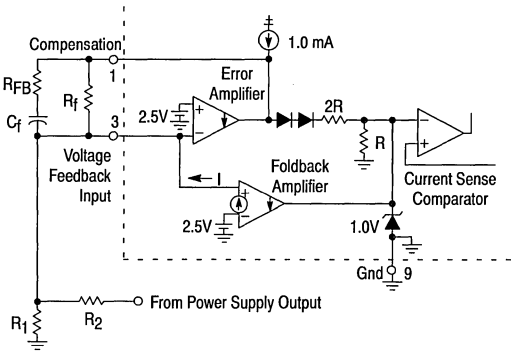
Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 90 dB, and a unity gain bandwith of 1.0 MHz with 57 degrees of phase margin (Figure 7). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current with the inverting input at 2.5 V is –2.0 µA. This can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 29). The output voltage is offset by two diodes drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Source Output (Pin 11) when Pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval. The Error Amp minimum feedback resistance is limited by the amplifier's minimum source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5mA} = 8800\ \Omega$$

Figure 29. Error Amplifier Compensation



Current Sense Comparator and PWM Latch

The MC44602 operates as a current mode controller, where output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output (Pin 1). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Source Output during the appropriate oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the emitter of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 6) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 1 where:

$$I_{pk} \approx \frac{V\ (Pin1) - 1.4V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} \approx \frac{1.0\ V}{R_S}$$

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and the output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 30.

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 14.1 V/10.2 V. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.3 V. The large hysteresis and low start-up current of the MC44602 make it ideally suited for off-line converter applications (Figures 33, 34) where efficient bootstrap start-up techniques are required.

A 20 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system start-up. The upper limit for the minimum operating voltage of the MC44602 is 11V.

Outputs

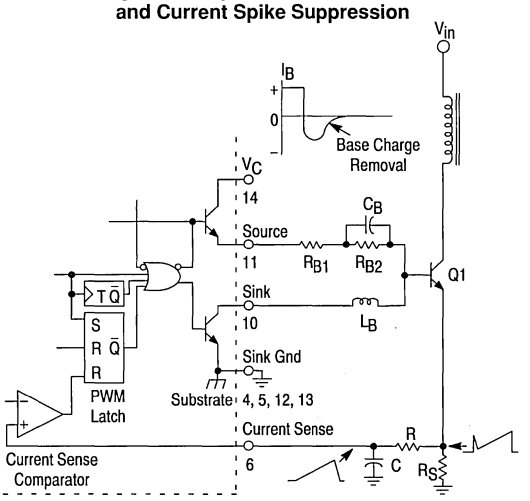
The MC44602 contains a high current split totem pole output that was specifically designed for direct drive of Bipolar Power Transistors. By splitting the totem pole into separate source and sink outputs, the power supply designer has the ability to independently adjust the turn-on and turn-off base drive to the external power transistor for optimal switching. The Source and Sink outputs are capable of up to 1.0 A and 1.5 A respectively and feature 50 ns switching times with a 1.0 nF load. Additional internal circuitry has been added to keep the Source Output "Off" and the Sink Output "On" whenever an undervoltage lockout is active. This feature eliminates the need for an external pull-down resistor and guarantees that the power transistor will be held in the "Off" state.

Separate output stage power and ground pins are provided to give the designer added flexibility in tailoring the base drive circuitry for a specific application. The Source Output high-state is controlled by applying a positive voltage to V_C (Pin 14) and is independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20V. The Sink Output low-state is controlled by applying a negative voltage to the Sink Ground (Pins 4, 5, 12, 13). The Sink Ground can be biased as much as 5.0 V negative with respect to Ground (Pin 7). Proper implementation of the V_C and Sink Ground pins will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level.

Reference

The 5.0 V bandgap reference has a tolerance of ±6.0% over a junction temperature range of –25°C to 85°C. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Figure 30. Bipolar Transistor Drive and Current Spike Suppression



Thermal Protection and Package

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 160°C, the PWM Latch is held in the "reset" state, forcing the Source Output "Off" and the Sink Output "On". This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

The MC44602 is contained in a heatsinkable 16-lead plastic dual-in-line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center Sink Ground pins that are specifically designed to improve the thermal conduction from the die to the circuit board. Figure 14 shows a simple and effective method of utilizing the printed circuit medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance. This example is for a symmetrical layout on a single-sided board with two ounce per square foot of copper.

Design Considerations

Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low-current signal, and high

current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

3

PROTECTION MODES

The MC44602 operates as a conventional fixed frequency current mode controller when the power supply output load is less than the design limit. For enhanced system reliability, this device has the unique ability of changing operating modes if the power supply output is overloaded or shorted.

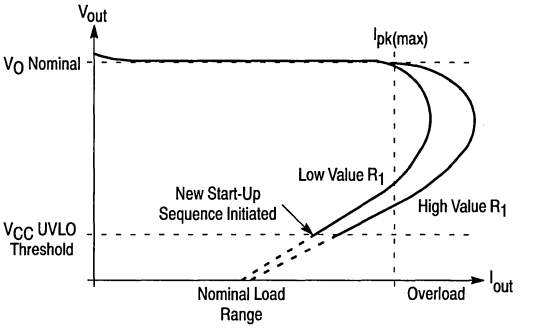
Overload Protection

Power supply overload protection is provided by the Foldback Amplifier. As the output load gradually increases, the Error Amplifier senses that the voltage at Pin 3 is less than the 2.5 V threshold. This causes the voltage at Pin 1 to rise, increasing the Current Sense Comparator threshold in order to maintain output regulation. As the load further increases, the inverting input of the Current Sense Comparator reaches the internal 1.0 V clamp level, limiting the switch current to the calculated $I_{pk(max)}$. At this point any further increase in load will cause the power supply output to fall out of regulation. As the voltage at Pin 3 falls below 2.5 V, current will flow out of the Foldback Amplifier input, and the internal clamp level will be proportionally reduced (Figures 9, 10). The increase in current flowing out of the Foldback Amplifier input in conjunction with the reduced clamp level, causes the power supply output voltage to fall at a faster rate than the voltage at Pin 3. This results in the output foldback characteristic shown in Figure 31. The shape of the current limit "knee" can be modified by the value of resistor R_1 in the feedback divider. Lower values of R_1 will reduce the $I_{pk(max)}$ clamp level at a faster rate.

Improper operation of the Foldback Amp can be encountered when the Error Amp compensation capacitor C_f exceeds 2.0 nF. The problem appears at Start-Up when the output voltage of the power supply is below nominal, causing the Error Amp output to rise quickly. The rapid change in output voltage will be coupled through C_f to the Inverting Input (Pin 3), keeping it at its 2.5 V threshold as the 1.0 mA Error Amp current source charges C_f. This has the effect of disabling the Foldback Amp by preventing Pin 3 and the clamp level at the inverting input of the Current Sense Comparator, from rising in proportion to the power supply output voltage. By adding resistor R_{FB} in series with C_f, the voltage at Pin 3 can be held to 1.0 V, corresponding to a Current Sense clamp level of 0.08 V (Figure 10), while allowing the Error Amp output to reach its high state V_{OH} of 7.0 V. The required resistor to keep Pin 3 below 1.0 V during initial Start-Up is:

$$\frac{R_{FB}\,R_f}{R_{FB}+R_f} \geq 6\left(\frac{R_1\,R_2}{R_1+R_2}\right)$$

Figure 31. Output Foldback Characteristic



Short Circuit Protection

Short circuit protection for the power supply is provided by the Valid Load Comparator, Fault Latch, and Demag Comparator. Figure 32 shows the logic truth table of the functional blocks. When operating the power supply with nominal output loading, the Fault Latch is "Set" by the NOR gate driver during the Power Transistor "On" time and "Reset" by the Fault Comparator during the "Off" time. When a severe overload or short circuit occurs on any output, the voltage during the "Off" time (flyback voltage) at the Load Detect Input, is unable to reach the 2.5 V threshold of the Valid Load Comparator. This causes the Fault Latch to remain in the "Set" state with output $\overline{Q}$ "Low". During the "Off" time the Demag Comparator output will also be "Low". This causes the NOR gate to internally hold the Sync Input "High", inhibiting the next fixed frequency Oscillator cycle and switching of the Power Transistor. As the load dissipates the stored transformer energy, the voltage at the Load Detect Input will fall. When this voltage reaches 85 mV, the Demag Comparator output goes "High", allowing the Sync Input to go "Low", and the Power Transistor to turn "On".

Note that as long as there is an output short, the switching frequency will shift to a much lower frequency than that set by R_T/C_T. The frequency shift has the effect of lowering the duty cycle, resulting in a significant reduction in Power Transistor and Output Rectifier heating when compared to conventional current mode controllers. The extended "On" time is the result of C_T charging from 0 V to 2.8 V instead of 1.2 V to 2.8 V. The extended "Off" time is the result of the output short time constant. The time constant consists of the output filter capacitance, and the equivalent series resistance (ESR) of the capacitor plus the associated wire resistance.

Figure 32. Logic Truth Table of Functional Blocks

Output Load	Power Transistor	Demag		Fault Latch			Sync	Operating Comments
		Input	Out	S	R	$\bar{Q}$	Input	
Nominal	On	<85mV	1	1	0	0	0	NOR gate driver sets Fault Latch.
	At Turn-Off	>85 mV, <2.5 V	0	0	0	0	⊥∧⊥	Narrow spike at Sync Input (<2.5 V) as transformer voltage rises quickly, Oscillator is not affected.
	Off	>2.5 V	0	0	1	1	0	Valid Load Comparator resets Fault Latch.
Short	On	<85 mV	1	1	0	0	0	Short is not detected until transistor turn-off.
	At Turn-Off	>85 mV, <2.5 V	0	0	0	0	1	Valid Load Comparator fails to reset Fault Latch, Pulse at Sync Input exceeds 2.5 V, Oscillator is disabled.
	Off	<85 mV	1	0	0	0	0	Load dissipates transformer energy, Oscillator enabled.

During the initial power supply startup the controller sequences through the Short Circuit and Overload Protection modes as the output filter capacitors charge-up. If an output is shorted and the auxiliary feedback winding is used to power the control IC as in Figure 33, the V_{CC} UVLO lower threshold level will be reached after several cycles, disabling the IC and initiating a new start-up sequence. The Short Circuit Protection mode can be disabled by grounding the Sync Input. Narrow switching spikes are present on this pin during normal operation. These spikes are caused by the rise time of the flyback voltage from the 85 mV Demag Comparator threshold to the 2.5 V Valid Load Comparator threshold. In high power applications, the increased negative current at the Load Detect Input can extend the switching spikes to the point where they exceed the Sync Input threshold. This problem can be eliminated by placing an external small signal clamp diode at the Load Detect Input. The diode is connected with the cathode at Pin 2 and the anode at ground.

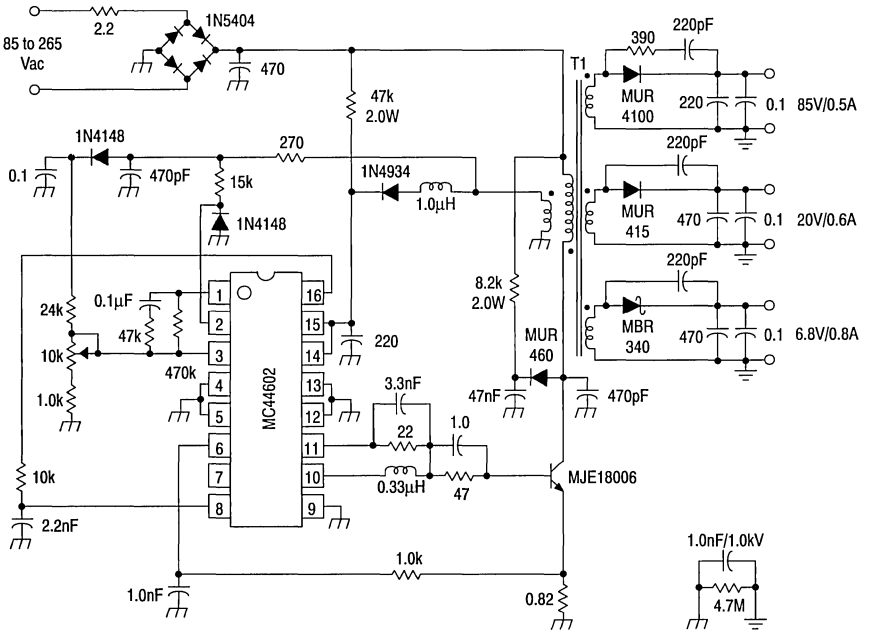
The divide-by-two toggle flip-flop will appear not to function properly during power supply start-up without foldback, or operation with an overloaded output. This phenomena appears at the end of the oscillator cycle if there was not a current sense comparison, and after the flyback voltage at the Load Detect Input failed to exceed 2.5 V. Under these conditions, the Sync input will go high approximately 1.0 μs after the Load Detect Input exceeds the 85 mV Demag Comparator threshold. This causes C_T to discharge down towards ground, generating a second negative going edge on the oscillator waveform. This second edge results in the divide-by-two flip-flop being clocked twice for each "On" time of the switch transistor. During initial start-up, this effect can be eliminated by insuring that the Foldback Amplifier is fully active with the addition of resistor R_{FB}. With the Foldback Amplifier active, the clamp level at the inverting input of the Current Sense Comparator will be low, allowing a comparison to take place during the switch transistor "On" time. When the Load Detect Input exceeds 85 mV, the Sync Input will go high, discharging C_T to ground after 1.0 μs, thus eliminating the second negative edge. Operation with the output overloaded will cause the toggle flip-flop to be clocked twice for each "On" time. This should not be a problem since the next "On" time is delayed by the Demag Comparator until the load dissipates the transformers energy.

The point where the IC detects that there is a severe output overload, or that the transformer has reached zero current, is controlled by the voltage of the auxiliary winding and a resistor divider. The divider consists of an external series resistor and an internal shunt resistor. The shunt resistor is nominally 18 kΩ but can range from 12 kΩ to 30 kΩ due to process variations. If more precise overload and zero current detection is required, the internal resistor variations can be swamped out by connecting a low value external resistor (≤2.7 kΩ) from Pin 2 to ground.

PIN DESCRIPTION

Pin No.	Name	Description
1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	Load Detect Input	A voltage indicating a severe overload or short circuit condition at any output of the switching power supply is connected to this input. The Oscillator is controlled by this information making the power supply short circuit proof.
3	Voltage Feedback Input	This is the inverting input of the Error Amplifier and the noninverting input of the Foldback Amplifier. It is normally connected to the switching power supply output through a resistor divider.
4, 5, 12, 13	Sink Ground	The Sink Ground pins form a single power return that is typically connected back to the power source on a separate path from Pin 9 Ground, to reduce the effects of switching transient noise on the control circuitry. These pins can be used to enhance the package power capabilities (Figure 14). The Sink Output low state (V_{OL}) can be modified by applying a negative voltage to these pins with respect to Ground (Pin 9) to optimize turn-off of a bipolar junction transistor.
6	Current Sense Input	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate conduction of the output switch transistor.
7	Sync Input	A narrow rectangular waveform applied to this input will synchronize the Oscillator. A DC voltage within the range of 3.2 V to 5.5 V will inhibit the Oscillator.
8	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed at this pin by connecting resistor R_T to V_{ref} and capacitor C_T to ground.
9	Ground	This pin is the control circuitry ground and is typically connected back to the power source on a separate path from the Sink Ground (Pins 4, 5, 12, 13).
10	Sink Output	Peak currents up to 1.5 A are sunk by this output suiting it ideally for turning-off a bipolar junction transistor. The output switches at one-half the oscillator frequency.
11	Source Output	Peak currents up to 1.0 A are sourced by this output suiting it ideally for turning-on a bipolar junction transistor. The output switches at one-half the oscillator frequency.
14	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin. With a separate connection to the power source, it can reduce the effects of switching transient noise on the control circuitry.
15	V_{CC}	This pin is the positive supply of the control IC. The minimum operating voltage range after start-up is 11 V to 18 V.
16	V_{ref}	This is the 5.0 V reference output. It provides charging current for capacitor C_T through resistor R_T and can be used to bias any additional system circuitry.

Figure 33. 60 Watt Off-Line Flyback Regulator

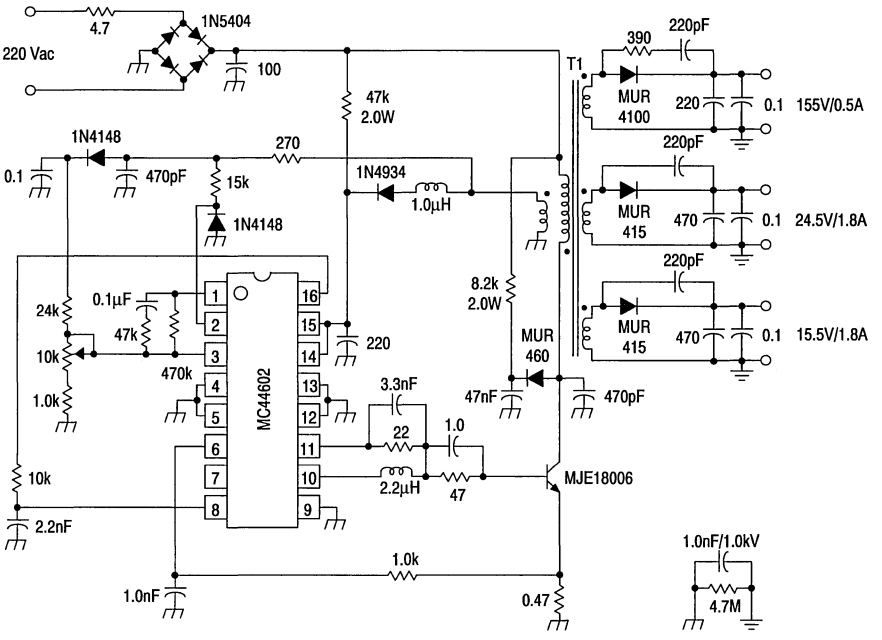


TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 85 Vac to 265 Vac	
85V	I_O = 0.5 A	Δ = 1.0 V or ± 0.6%
20V	I_O = 0.5 A	Δ = 0.04 V or ± 0.1%
6.8V	I_O = 0.8 A	Δ = 0.07 V or ± 0.5%
Load Regulation	V_{in} = 220 Vac	
85V	I_O = 0.1 A to 0.5 A	Δ = 1.0 V or ± 0.6%
20V	I_O = 0.1 A to 0.5 A	Δ = 0.4 V or ± 1.0%
6.8V	I_O = 0.1 A to 0.8 A	Δ = 0.2 V or ± 1.5%
Efficiency	V_{in} = 110 Vac, P_O = 58 W	81%
Standby Power	V_{in} = 110 Vac, P_O = 0 W	2.0 W

T1 – Orega SMT2 (G4787-01)
Primary: 41 Turns, #25AWG
Auxiliary Feedback: 12 Turns, #25AWG
Secondary: 85 V - 60 Turns, #25AWG
20 V - 15 Turns, #25AWG (2 Strands) Bifiliar Wound
6.8 V - 5 Turns, #25AWG (2 Strands) Bifiliar Wound
Core – ETD39 34x17x11 B52
Gap – ≈ 0.020″ for a primary inductance of 750 µH, A_L = 500 nH/Turn^2

3

Figure 34. 150 Watt Off-Line Flyback Regulator



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 185 Vac to 265 Vac	
155V	I_O = 0.5 A	Δ = 1.0 V or ± 0.3%
24.5V	I_O = 1.0. A	Δ = 0.4 V or ± 0.8%
15.5V	I_O = 1.0 A	Δ = 0.3 V or ± 1.0%
Load Regulation	V_{in} = 220 Vac	
155V	I_O = 0.1 A to 0.5 A	Δ = 2.0 V or ± 0.7%
24.5V	I_O = 0.1 A to 1.0 A	Δ = 0.4 V or ± 0.8%
15.5V	I_O = 0.1 A to 1.0 A	Δ = 0.2 V or ± 0.7%
Efficiency	V_{in} = 220 Vac, P_O = 117.5 W	83%
Standby Power	V_{in} = 220 Vac, P_O = 0 W	5.0 W

T1 – Orega SMT2 (G4717-01)
Primary: 55 Turns, #25AWG
Auxiliary Feedback: 6 Turns, #25AWG
Secondary: 155 V - 52 Turns, #25AWG
24.5 V - 9 Turns, #25AWG (2 Strands) Bifiliar Wound
15.5 V - 6 Turns, #25AWG (2 Strands) Bifiliar Wound
Core – GETV 53x18x18 B52
Gap – ≈ 0.020″ for a primary inductance of 1.35 µH, A_L = 450 nH/Turn^2

SG3525A/SG3527A

Pulse Width Modulator Control Circuits

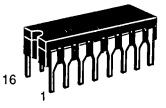
PULSE WIDTH MODULATOR CONTROL CIRCUITS

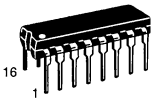
SILICON MONOLITHIC INTEGRATED CIRCUITS

The SG3525A/3527A series of pulse width modulator control-circuits offer improved performance and lower external parts count when implemented for controlling all types of switching power supplies. The on-chip +5.1 V reference is trimmed to ±1% and the error amplifier has an input common-mode voltage range that includes the reference voltage, thus eliminating the need for external divider resistors. A sync input to the oscillator enables multiple units to be slaved or a single unit to be synchronized to an external system clock. A wide range of dead time can be programmed by a single resistor connected between the C_T and Discharge pins. These devices also feature built-in soft-start circuitry, requiring only an external timing capacitor. A shut-down pin controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. The under voltage lockout inhibits the outputs and the changing of the soft-start capacitor when V_{CC} is below nominal. The output stages are totem-pole design capable of sinking and sourcing in excess of 200 mA. The output stage of the SG3525A series features NOR Logic resulting in a low output for an off state while the SG3527A series utilized OR Logic which gives a high output when off.

- 8.0 V to 35 V Operation
- 5.1 V ± 1.0% Trimmed Reference
- 100 Hz to 400 kHz Oscillator Range
- Separate Oscillator Sync Pin
- Adjustable Dead Time Control
- Input Undervoltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Pulse-by-Pulse Shutdown
- Dual Source/Sink Outputs: ±400 mA Peak

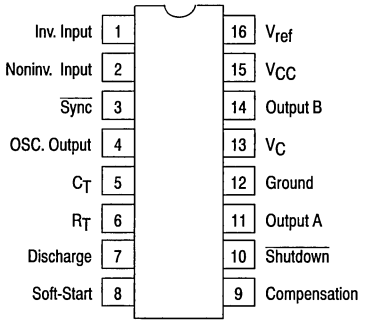
J SUFFIX
CERAMIC PACKAGE
CASE 620



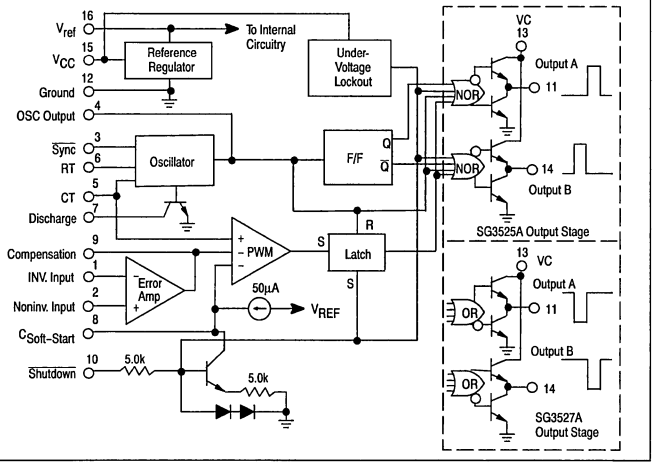


N SUFFIX
PLASTIC PACKAGE
CASE648

PIN CONNECTIONS



Functional Block Diagram



ORDERING INFORMATION

Device	Temperature Range	Package
SG3525AJ	0° to +70°C	Ceramic DIP
SG3525AN		Plastic Dip
SG3527AJ		Ceramic DIP
SG3527AN		Plastic Dip

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs	—	−0.3 to +5.5	V
Analog Inputs	—	−0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±500	mA
Reference Output Current	I_{ref}	50	mA
Oscillator Charging Current	—	5.0	mA
Power Dissipation (Plastic & Ceramic Package) T_A = +25°C (Note 2) T_C = +25°C (Note 3)	P_D	 1000 2000	mW
Thermal Resistance Junction-to-Air (Plastic and Ceramic Package)	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction-to-Case (Plastic and Ceramic Package)	$R_{\theta JC}$	60	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	−65 to +150 −55 to +125	°C
Lead Temperature (Soldering, 10 seconds)	T_{Solder}	+300	°C

NOTES: 1. Values beyond which damage may occur.
2. Derate at 10 mW/°C for ambient temperatures above +50°C.
3. Derate at 16 mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	+8.0	+35	Vdc
Collector Supply Voltage	V_C	+4.5	+35	Vdc
Output Sink/Source Current (Steady State) (Peak)	I_O	 0 0	 ±100 ±400	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.1	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	0.2	µF
Deadtime Resistor Range	R_D	0	500	Ω
Operating Ambient Temperature Range	T_A	0	+70	°C

APPLICATION INFORMATION

Shutdown Options (See Block diagram, front page)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 µA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150 µA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

ELECTRICAL CHARACTERICISTICS (V_{CC} = +20 Vdc, T_A = T_{low} to T_{high} [Note 4], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (T_J = +25°C)	V_{ref}	5.00	5.10	5.20	Vdc
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	—	10	20	mV
Load Regulation (0 mA ≤ I_L ≤ 20 mA)	Reg_{load}	—	20	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T$	—	20	—	mV
Total Output Variation Includes Line and Load Regulation over Temperature	ΔV_{ref}	4.95	—	5.25	Vdc
Short Circuit Current (V_{ref} = 0 V, T_J = +25°C)	I_{SC}	—	80	100	mA
Output Noise Voltage (10 Hz ≤ f ≤ 10 kHz, T_J = +25°C)	V_n	—	40	200	μV_{rms}
Long Term Stability (T_J = +125°C) (Note 5)	S	—	20	50	mV/khr
OSCILLATOR SECTION (Note 6, unless otherwise noted.)					
Initial Accuracy (T_J = +25°C)	—	—	±2.0	±6.0	%
Frequency Stability with Voltage (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	—	±1.0	±2.0	%
Frequency Stability with Temperature	$\frac{\Delta f_{osc}}{\Delta T}$	—	±0.3	—	%
Minimum Frequency (R_T = 150 kΩ, C_T = 0.2 µF)	f_{min}	—	50	—	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 1.0 nF)	f_{max}	400	—	—	kHz
Current Mirror (I_{RT} = 2.0 mA)	—	1.7	2.0	2.2	mA
Clock Amplitude	—	3.0	3.5	—	V
Clock Width (T_J = +25°C)	—	0.3	0.5	1.0	µs
Sync Threshold	—	1.2	2.0	2.8	V
Sync Input Current (Sync Voltage = +3.5 V)	—	—	1.0	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = +5.1 V)					
Input Offset Voltage	V_{IO}	—	2.0	10	mV
Input Bias Current	I_{IB}	—	1.0	10	µA
Input Offset Current	I_{IO}	—	—	1.0	µA
DC Open-Loop Gain (R_L ≥ 10 MΩ)	A_{VOL}	60	75	—	dB
Low Level Output Voltage	V_{OL}	—	0.2	0.5	V
High Level Output Voltage	V_{OH}	3.8	5.6	—	V
Common Mode Rejection Ratio (+1.5 V ≤ V_{CM} ≤ +5.2 V)	CMRR	60	75	—	dB
Power Supply Rejection Ratio (+8.0 V ≤ V_{CC} ≤ +35 V)	PSRR	50	60	—	dB
PWM COMPARATOR SECTION					
Minimum Duty Cycle	DC_{min}	—	—	0	%
Maximum Duty Cycle	DC_{max}	45	49	—	%
Input Threshold, Zero Duty Cycle (Note 6)	V_{TH}	0.6	0.9	—	V
Input Threshold, Maximum Duty Cycle (Note 6)	V_{TH}	—	3.3	3.6	V
Input Bias Current	I_{IB}	—	0.05	1.0	µA

NOTES: 4. T_{low} = 0° for SG3525A/3527A T_{high} = +70°C for SG3525A/3527A
5. SInce long term stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Tested at f_{osc} = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 µF, R_D = 0Ω).
7. Applies to SG3525A only, due to polarity of output pulses.

3

ELECTRICAL CHARACTERICISTICS (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit
SOFT-START SECTION					
Soft-Start Current ($V_{shutdown}$ = 0 V)	—	25	50	80	µA
Soft-Start Voltage ($V_{shutdown}$ = 2.0 V)	—	—	0.4	0.6	V
Shutdown Input Current ($V_{shutdown}$ = 2.5 V)	—	—	0.4	1.0	mA
OUTPUT DRIVERS (Each Output, V_{CC} = +20 V)					
Output Low Level (I_{sink} = 20 mA) (I_{sink} = 100 mA)	V_{OL}	 — —	 0.2 1.0	 0.4 2.0	V
Output High Level (I_{source} = 20 mA) (I_{source} = 100 mA)	V_{OH}	 18 17	 19 18	 — —	V
Under Voltage Lockout (V8 and V9 = High)	V_{UL}	6.0	7.0	8.0	V
Collector Leakage, V_C = +35 V (Note 7)	$I_{C(leak)}$	—	—	200	µA
Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	—	100	600	ns
Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	—	50	300	ns
Shutdown Delay (V_{DS} = +3.0 V, C_S = 0, T_J = +25°C)	t_{ds}	—	0.2	0.5	µs
Supply Current (V_{CC} = +35 V)	I_{CC}	—	14	20	mA

Lab Test Fixture

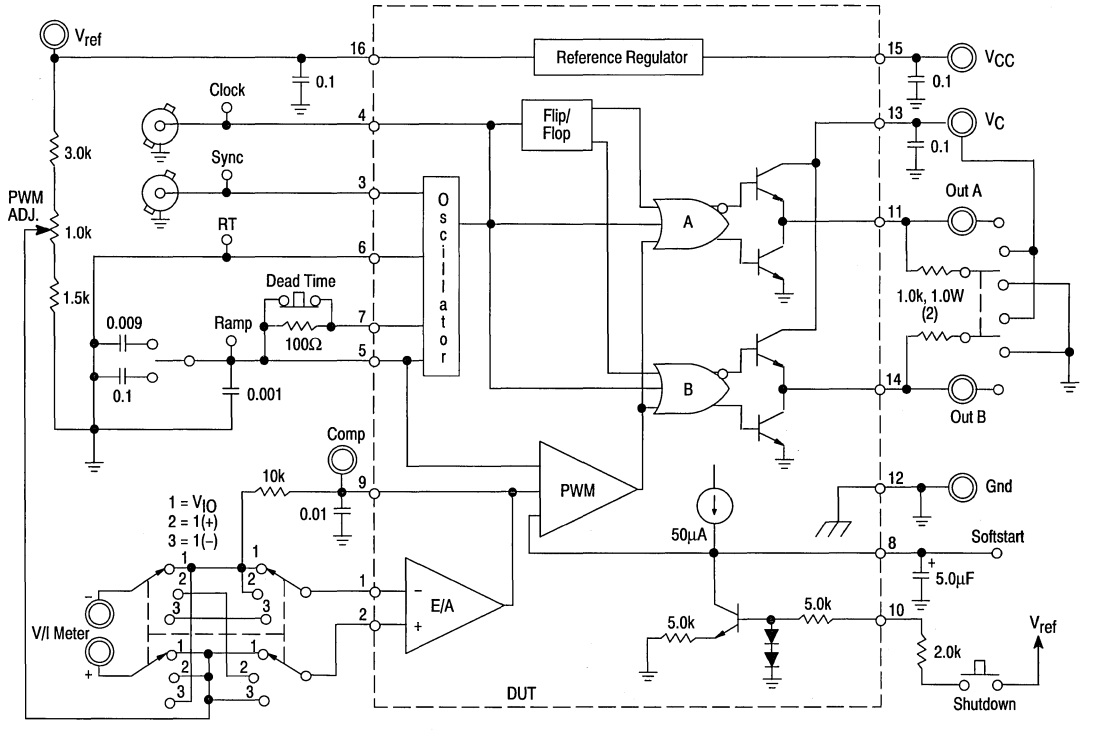


Figure 1. Oscillator Charge Time versus R_T

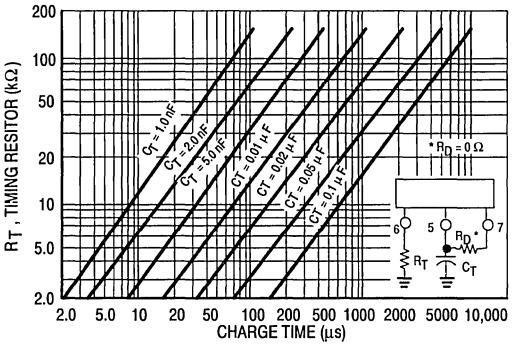


Figure 2. Oscillator Discharge Time versus R_D

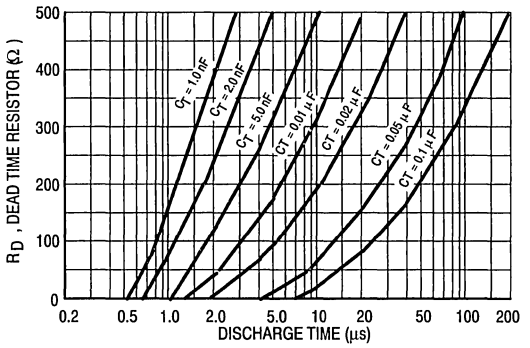


Figure 3. Error Amplifier Open-Loop Frequency Response

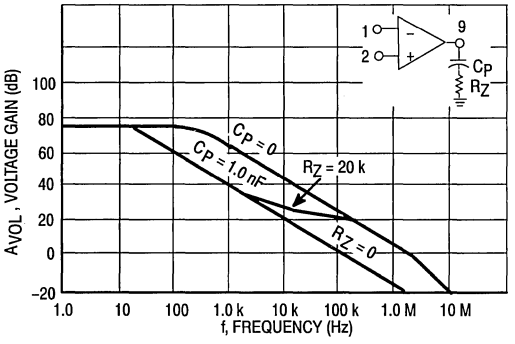


Figure 4. SG3525A Output Saturation Characteristics

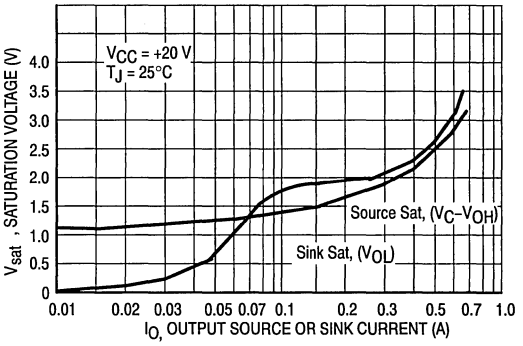


Figure 5. SG3525A Oscillator Schematic

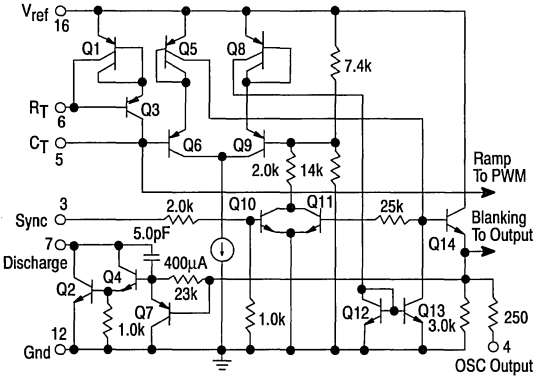


Figure 6. SG3525A Error Amplifier Schematic

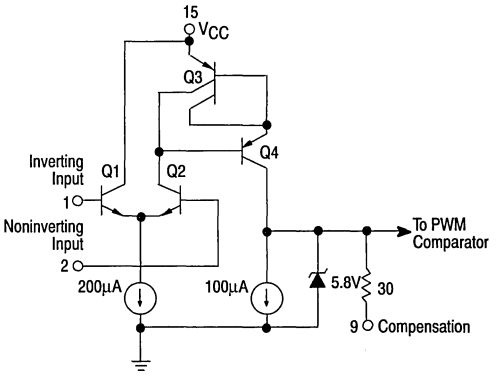


Figure 7. SG3525A Output Circuit
(1/2 Circuit Shown)

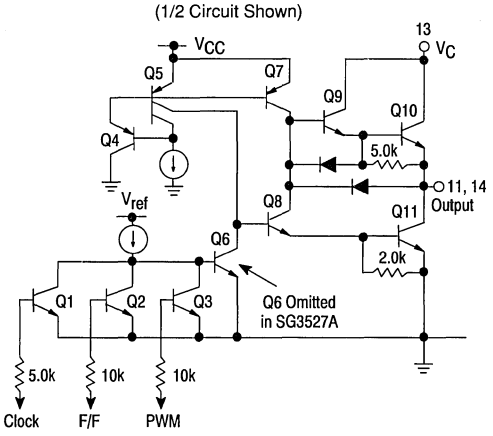
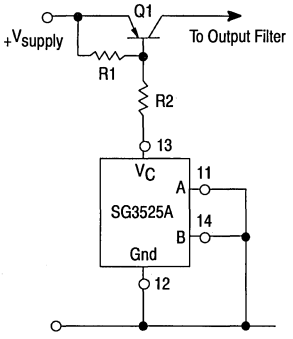
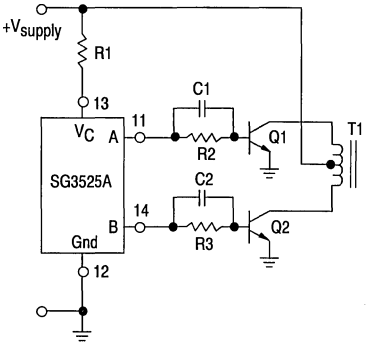


Figure 8. Single-Ended Supply



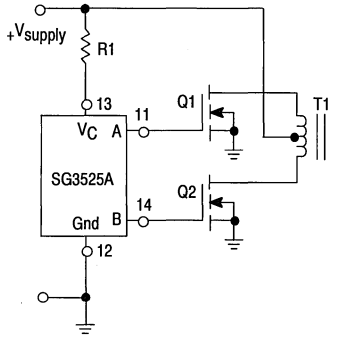
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

Figure 9. Push-Pull Configuration



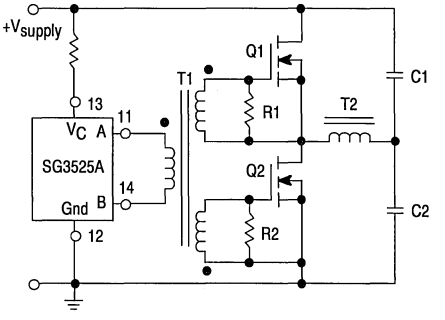
In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C1 and C2.

Figure 10. Driving Power FETS



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

Figure 11. Driving Transformers in a Half-Bridge Configuration



Low power transformers can be driven directly by the SG3525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

SG3526

Pulse Width Modulation Control Circuit

PULSE WIDTH MODULATION CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATE CIRCUIT

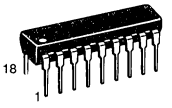
3

The SG3526 is a high performance pulse width modulator integrated circuit intended for fixed frequency switching regulators and other power control applications.

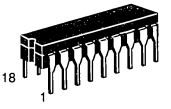
Functions included in this IC are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two high current totem pole outputs ideally suited for driving the capacitance of power FETs at high speeds.

Additional protective features include soft start and undervoltage lockout, digital current limiting, double pulse inhibit, adjustable dead time and a data latch for single pulse metering. All digital control ports are TTL and B-series CMOS compatible. Active low logic design allows easy wired-OR connections for maximum flexibility. The versatility of this device enables implementation in single-ended or push-pull switching regulators that are transformerless or transformer coupled. The SG3526 is specified over a junction temperature range of 0° to +125°C.

- 8.0 V to 35 V Operation
- 5.0 V ±1% Trimmed Reference
- 1.0 Hz to 400 kHz Oscillator Range
- Dual Source/Sink Current Outputs: ±100 mA
- Digital Current Limiting
- Programmable Dead Time
- Undervoltage Lockout
- Single Pulse Metering
- Programmable Soft-Start
- Wide Current Limit Common Mode Range
- Guaranteed 6 Unit Synchronization

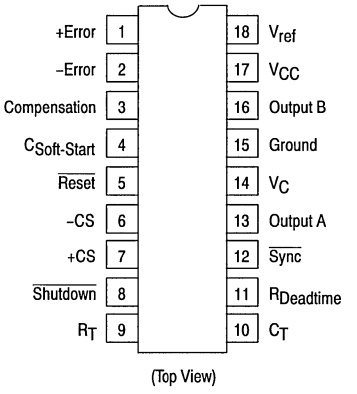


N SUFFIX
PLASTIC PACKAGE
CASE 707



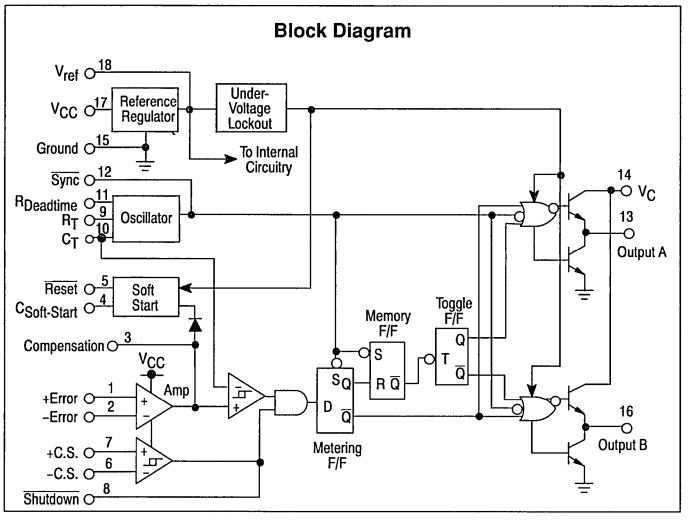
J SUFFIX
PLASTIC PACKAGE
CASE 726

PIN CONNECTIONS



(Top View)

Block Diagram



ORDERING INFORMATION

Device	Junction Temperature Range	Package
SG3526J	0° to +125°C	Ceramic DIP
SG3526N		Plastic DIP

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs	—	−0.3 to +5.5	V
Analog Inputs	—	−0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±200	mA
Reference Load Current (V_{CC} = 40 V, Note 2)	I_{ref}	50	mA
Logic Sink Current	—	15	mA
Power Dissipation (Plastic & Ceramic Package) T_A = +25°C (Note 3) T_C = +25°C (Note 4)	P_D	 1000 3000	mW
Thermal Resistance Junction-to-Air (Plastic and Ceramic Package)	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction-to-Case (Plastic and Ceramic Package)	$R_{\theta JC}$	42	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)	$T_{Soldier}$	±300	°C

NOTES: 1. Values beyond which damage may occur.
2. Maximum junction temperature must be observed.
3. Derate at 10 mW/°C for ambient temperatures above +50°C.
4. Derate at 24 mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	+8.0	+35	Vdc
Collector Supply Voltage	V_C	+4.5	+35	Vdc
Output Sink/Source Current (Each Output)	I_O	0	±100	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.001	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	20	µF
Available Deadtime Range (40 kHz)		3.0	50	%
Operating Junction Temperature Range	T_J	0	+125	°C

ELECTRICAL CHARACTERICISTICS (V_{CC} = +15 Vdc, T_J = T_{low} to T_{high} [Note 5], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION (Note 6)					
Reference Output Voltage (T_J = +25°C)	V_{ref}	4.90	5.00	5.10	V
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	—	10	30	mV
Load Regulation (0 mA ≤ I_L ≤ 20 mA)	Reg_{load}	—	10	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T$	—	10	—	mV
Total Reference Output Voltage Variation (+8.0 V ≤ V_{CC} ≤ +35 V, 0 mA ≤ I_L ≤ 20 mA))	ΔV_{ref}	4.85	5.00	5.15	V
Short Circuit Current (V_{ref} = 0 V, Note 2)	I_{SC}	25	80	125	mA
UNDERVOLTAGE LOCKOUT					
$\overline{Reset}$ Output Voltage (V_{ref} = +3.8 V)	—	—	0.2	0.4	V
$\overline{Reset}$ Output Voltage (V_{ref} = +4.8 V)	—	2.4	4.8	—	V
OSCILLATOR SECTION (Note 7)					
Initial Accuracy (T_J = +25°C)	—	—	±3.0	±8.0	%
Frequency Stability over Power Supply Range (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	—	0.5	1.0	%
Frequency Stability over Temperature (ΔT_J = T_{low} to T_{high})	$\frac{\Delta f_{osc}}{\Delta T_J}$	—	2.0	—	%
Minimum Frequency (R_T = 150 kΩ, C_T = 20 μF)	f_{min}	—	0.5	—	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 0.001 μF)	f_{max}	400	—	—	kHz
Sawtooth Peak Voltage (V_{CC} = +35 V)	$V_{osc}(P)$	—	3.0	3.5	V
Sawtooth Valley Voltage (V_{CC} = +8.0 V)	$V_{osc}(V)$	0.45	0.8	—	V
ERROR AMPLIFIER SECTION (Note 8)					
Input Offset Voltage (R_S ≤ 2.0 kΩ)	V_{IO}	—	2.0	10	mV
Input Bias Current	I_{IB}	—	–350	–2000	nA
Input Offset Current	I_{IO}	—	35	200	nA
DC Open-Loop Gain (R_L ≥ 10 MΩ)	A_{VOL}	60	72	—	dB
High Output Voltage ($V_{Pin\ 1}$–$V_{Pin\ 2}$ ≥ +150 mV, I_{source} = 100 μA)	V_{OH}	3.6	4.2	—	V
Low Output Voltage ($V_{Pin\ 2}$–$V_{Pin\ 1}$ ≥ +150 mV, I_{sink} = 100 μA)	V_{OL}	—	0.2	0.4	V
Common Mode Rejection Ratio (R_S ≤ 2.0 kΩ)	CMRR	70	94	—	dB
Power Supply Rejection Ratio (+12 V ≤ V_{CC} ≤ +18 V)	PSRR	66	80	—	dB

NOTES: 5. T_{low} = 0°C for SG3526 T_{high} = +125°C for SG3526
6. I_L = 0 mA unless otherwise noted.
7. f_{osc} = 40 kHz (R_T = 4.12 kΩ ± 1%, C_T = 0.01 μF ± 1%, R_D = 0 Ω)
8. 0 V ≤ V_{CM} ≤ +5.2 V.

ELECTRICAL CHARACTERICISTICS (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR SECTION (Note 7)					
Minimum Duty Cycle ($V_{Compensation}$ = +0.4 V)	DC_{min}	—	—	0	%
Maximum Duty Cycle ($V_{Compensation}$ = +3.6 V)	DC_{max}	45	49	—	%
DIGITAL PORTS ($\overline{SYNC}$, $\overline{SHUTDOWN}$, $\overline{RESET}$)					
Output Voltage					V
(High Logic Level) (I_{source} = 40 μA)	V_{OH}	2.4	4.0	—	
(Low Logic Level) (I_{sink} = 3.6 mA)	V_{OL}	—	0.2	0.4	
Input Current — High Logic Level					μA
(High Logic Level) (V_{IH} = +2.4 V)	I_{IH}	—	–125	–200	
(Low Logic Level) (V_{IL} = +0.4 V)	I_{IL}	—	–225	–360	
CURRENT LIMIT COMPARATOR SECTION (Note 9)					
Sense Voltage ($R_S \leq 50\ \Omega$)	V_{sense}	80	100	120	mA
Input Bias Current	I_{IB}	—	–3.0	–10	μA
SOFT-START SECTION					
Error Clamp Voltage ($\overline{Reset}$ = +0.4 V)	—	—	0.1	0.4	V
$C_{Soft\text{-}Start}$ Charging Current ($\overline{Reset}$ = +2.4 V)	I_{CS}	50	100	150	μA
OUTPUT DRIVERS (Each Output, V_C = +15 Vdc, unless otherwise noted.)					
Output High Level	V_{OH}				V
I_{source} = 20 mA		12.5	13.5	—	
I_{source} = 100 mA		12	13	—	
Output Low Level	V_{OL}				V
I_{sink} = 20 mA		—	0.2	0.3	
I_{sink} = 100 mA		—	1.2	2.0	
Collector Leakage, V_C = +40 V	$I_{C(leak)}$	—	50	150	μA
Rise Time (C_L = 1000 pF)	t_r	—	0.3	0.6	μs
Fall Time (C_L = 1000 pF)	t_f	—	0.1	0.2	μs
Supply Current ($\overline{Shutdown}$ = +0.4 V, V_{CC} = +35 V, R_T = 4.12 kΩ)	I_{CC}	—	18	30	mA

NOTES: 7. f_{osc} = 40 kHz (R_T = 4.12 kΩ ± 1%, C_T = 0.01 μF ± 1%, R_D = 0 Ω)
8. $0\ V \leq V_{CM} \leq +5.2\ V$
9. $0\ V \leq V_{CM} \leq +12\ V$

TYPICAL CHARACTERISTICS

Figure 1. SG3526 Reference Stability Over Temperature

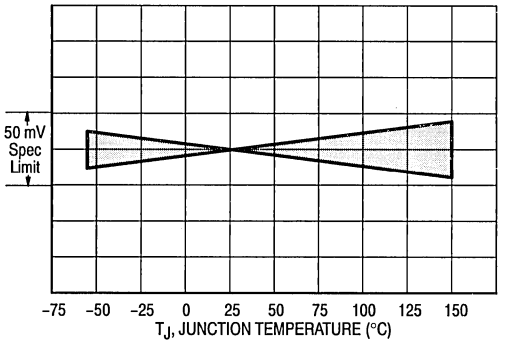


Figure 2. Reference Voltage as a Function Supply Voltage

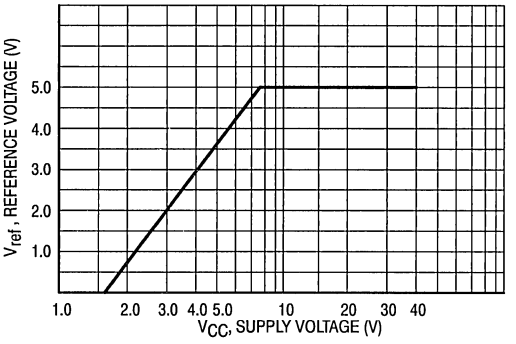


Figure 3. Error Amplifier Open-Loop Frequency Response

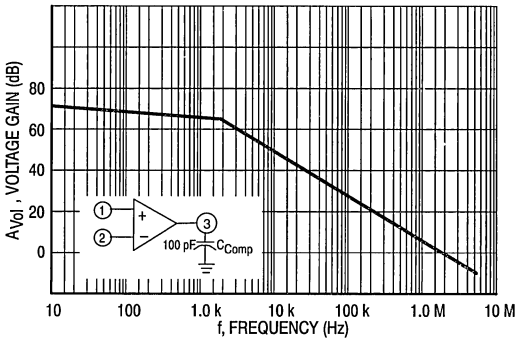


Figure 4. Current Limit Comparator Threshold

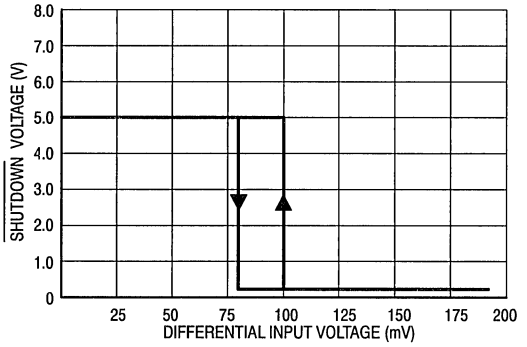


Figure 5. Undervoltage Lockout Characteristic

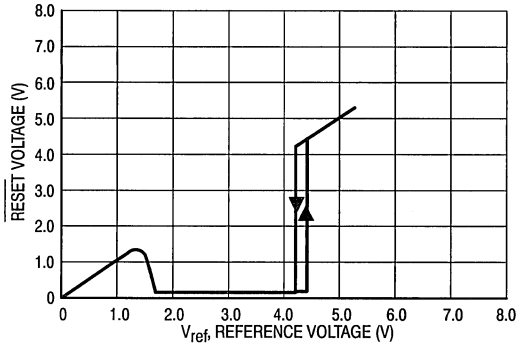


Figure 6. Output Driver Saturation Voltage as a Function of Sink Current

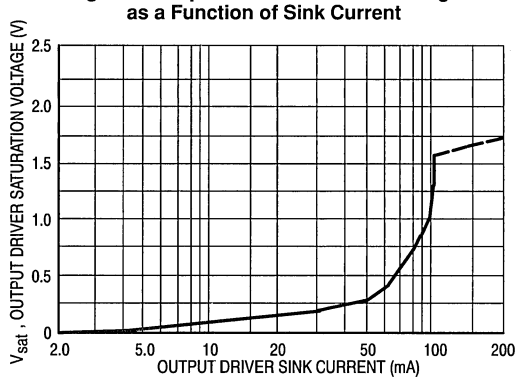


Figure 7. V_C Saturation Voltage as a Function of Sink Current

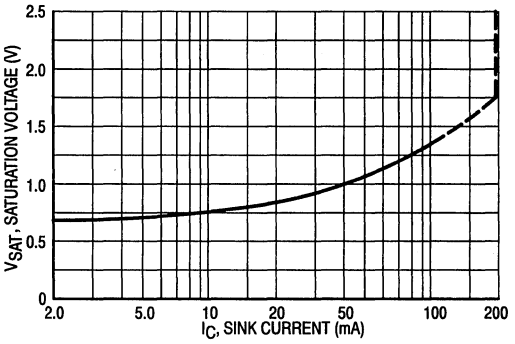


Figure 8. SG3526 Oscillator Period

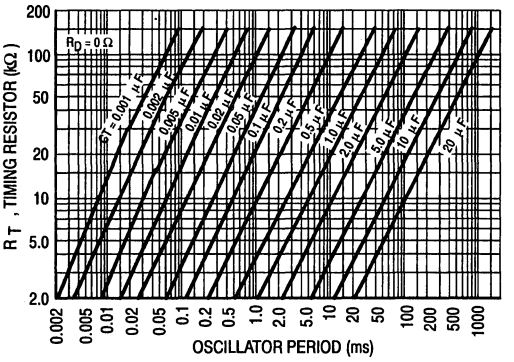


Figure 9. SG3526 Error Amplifier

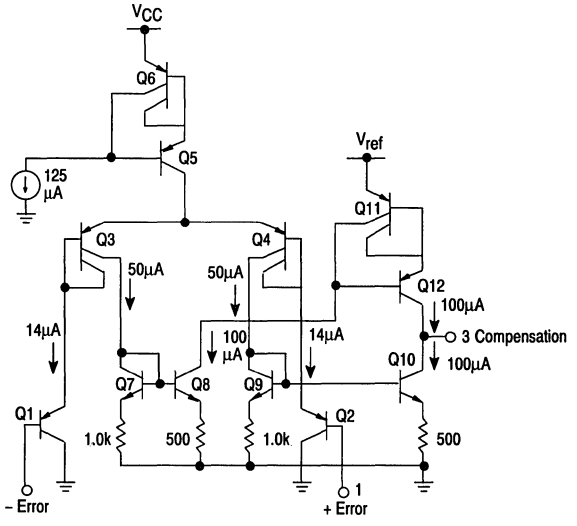


Figure 10. SG3526 Undervoltage Lockout

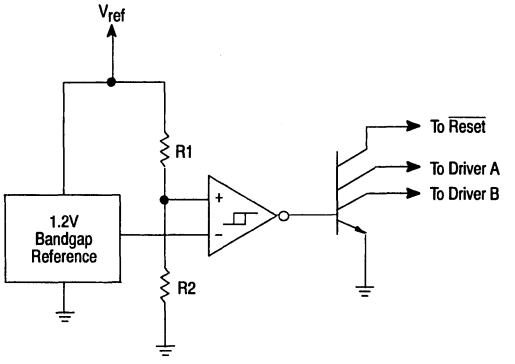
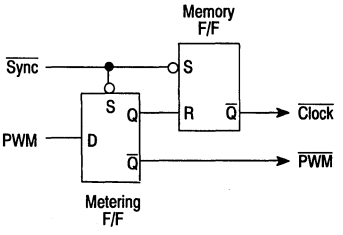


Figure 11. SG3526 Pulse Processing Logic

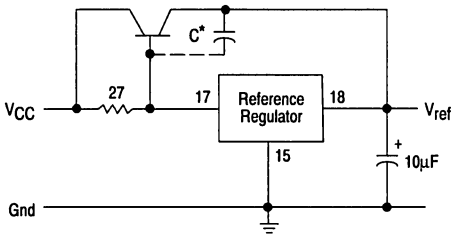


The metering Flip-Flop is an asynchronous data latch which suppresses high frequency oscillations by allowing only one PWM pulse per oscillator cycle.

The memory Flip-Flop prevents double pulsing in a push-pull configuration by remembering which output produced the last pulse.

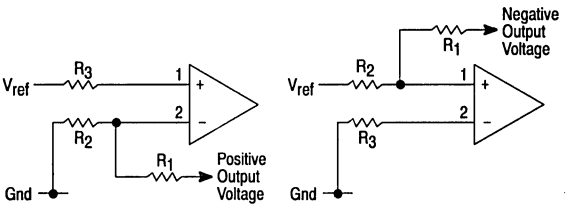
APPLICATIONS INFORMATION

Figure 12. Extending Reference Output Current Capability



* May be required with some types of transistors

Figure 13. Error Amplifier Connections



$$V_{out} = V_{ref}\left(\frac{R_1 + R_2}{R2}\right) \qquad V_{out} = V_{ref}\left(\frac{R_1}{R_2}\right)$$

$$R_3 = \left(\frac{R_1 R_2}{R_1 + R_2}\right)$$

Figure 14. Oscillator Connections

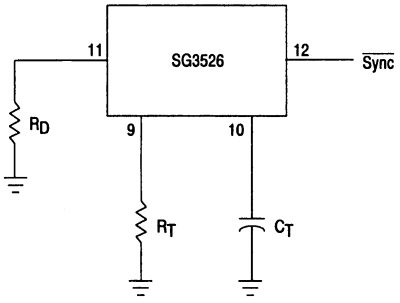
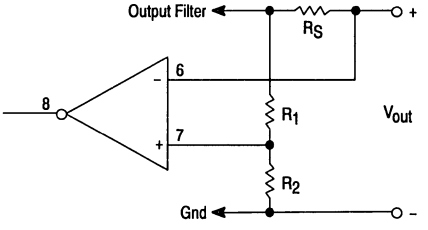


Figure 15. Foldback Current Limiting



$$I_{(max)} = \frac{\left(0.1\,V + \frac{V_{out} R_1}{R1 + R2}\right)}{R_S} \qquad I_{SC} = \left(\frac{0.1\,V}{R_S}\right)$$

Figure 16. SG3526 Soft-Start Circuity

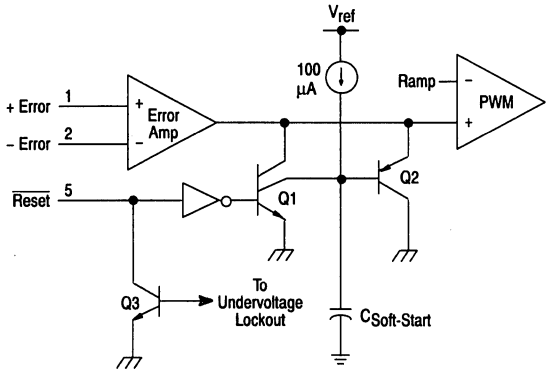
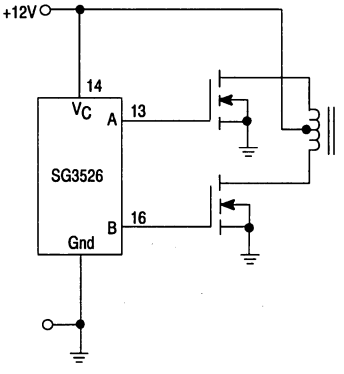


Figure 17. Driving VMOS Power FETs



The totem pole output drivers of the SG3526 are ideally suited for driving the input capacitance of power FETs at high speeds.

Figure 18. Half-Bridge Configuration

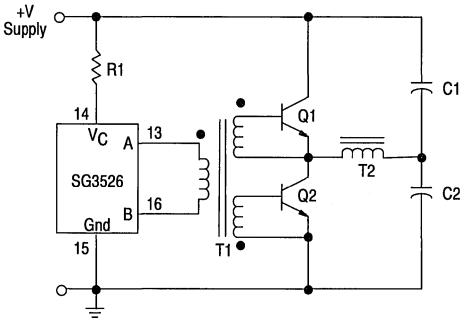
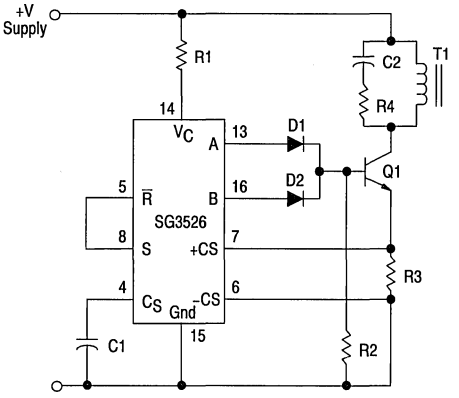


Figure 19. Flyback Converter with Current Limiting



In the above circuit, current limiting is accomplished by using the current limit comparator output to reset the soft-start capacitor.

Figure 20. Single-Ended Configuration

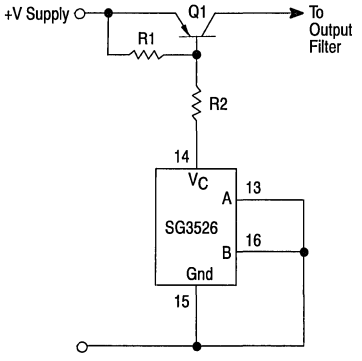
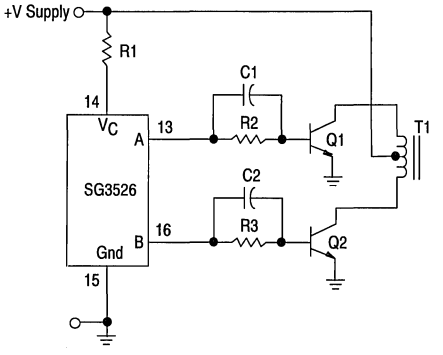


Figure 21. Push-Pull Configuration



TCA5600
TCF5600

Advance Information

Universal Microprocessor Power Supply/Controller

UNIVERSAL MICROPROCESSOR POWER SUPPLY CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

3

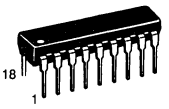
The TCA5600/TCF5600 is a versatile power supply control circuit for microprocessor based systems and mainly intended for automotive applications and battery powered instruments. To cover a wide range of applications, the device offers high circuit flexibility with minimum of external components.

Functions included in this IC are a temperature compensated voltage reference, on-chip DC/DC converter, programmable and remote controlled voltage regulator, fixed 5.0 V supply voltage regulator with external PNP power device, undervoltage detection circuit, power-on RESET delay and watchdog feature for safe and hazard free microprocessor operations.

- 6.0 V to 30 V Operation Range
- 2.5 V Reference Voltage Accessible for Other Tasks
- Fixed 5.0 V ± 4% Microprocessor Supply Regulator Including Current Limitation, Overvoltage Protection and Undervoltage Monitor.
- Programmable 6.0 V to 30 V Voltage Regulator Exhibiting High Peak Current (150mA), Current Limiting and Thermal Protection.
- Two Remote Inputs to Select the Regulator's Operation Mode:
  OFF = 5.0 V, 5.0 V Standby
  Programmable Output Voltage
- Self Contained DC/DC Converter Fully Controlled by the Programmable Regulator to Guarantee Safe Operation Under All Working Conditions
- Programmable Power-On RESET Delay
- Watchdog Select Input
- Negative Edge Triggered Watchdog Input
- Low Current Consumption in the V_{CC1} Standby Mode
- All Digital Control Ports are TTL and MOS-Compatible

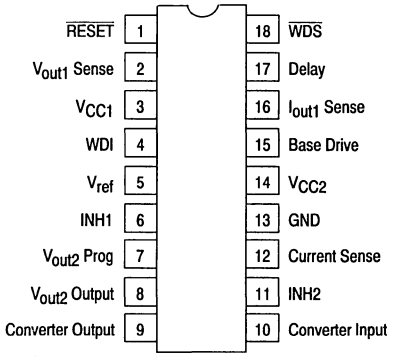
Applications Include:

- Microprocessor Systems with E^2PROMs
- High Voltage Crystal and Plasma Displays
- Decentralized Power Supplies in Computer and Telecommunication Systems



PLASTIC PACKAGE
CASE 707

PIN CONNECTIONS



(Top View)

RECOMMENDED OPERATION CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC1} V_{CC2}	5.0 5.5	30 30	V
Collector Current	I_C	—	800	mA
Output Voltage	V_{out2}	6.0	30	V
Reference Source Current	I_{ref}	0	2.0	mA

ORDERING INFORMATION

Device	Operating Junction Temperature Range	Package
TCA5600	0° to +125°C	Plastic DIP
TCF5600	–40° to +150°C	Plastic DIP

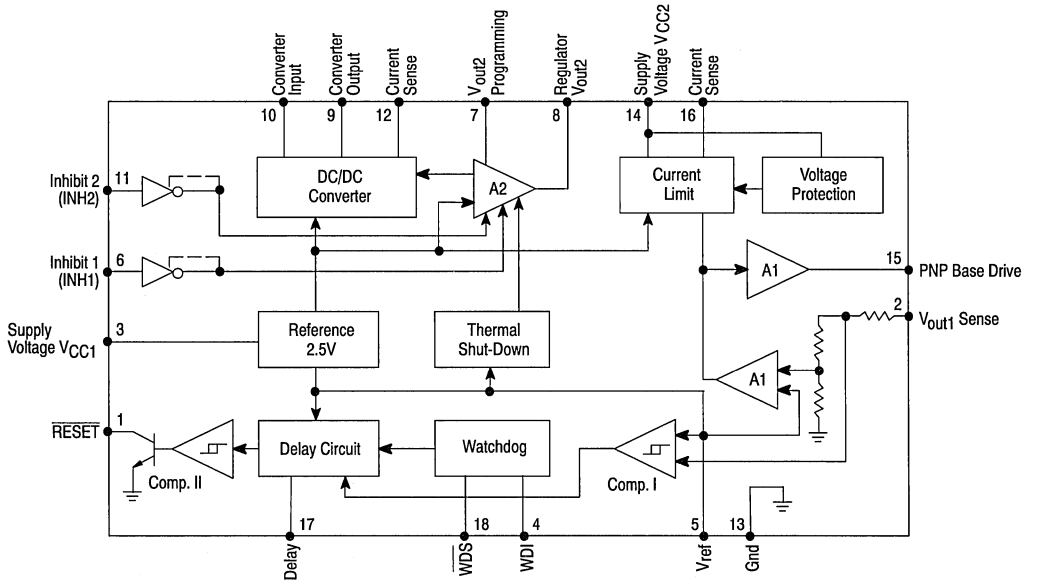
3

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted, Note 1.)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 3,14)	V_{CC1}, V_{CC2}	35	Vdc
Base Drive Current (Pin 15)	I_B	20	mA
Collector Current (Pin 10)	I_C	1.0	A
Forward Rectifier Current (Pin 10 to Pin 9)	I_F	1.0	A
Logic Inputs INH1, INH2, $\overline{WDS}$ (Pin 6, 11, 18)	V_{INP}	−0.3 V to V_{CC1}	Vdc
Logic Input Current WDI (Pin 4)	I_{WDI}	±0.5	mA
Output Sink Current $\overline{RESET}$ (Pin 1)	$I_{\overline{RES}}$	10	mA
Analog Inputs (Pin 2) (Pin 7)	— —	−0.3 to 10 −0.3 to 5.0	V
Reference Source Current (Pin 5)	I_{ref}	5.0	mA
Power Dissipation (Note 2) T_A = +75°C TCA5600 T_A = +85°C TCF5600	P_D	 500 650	mW
Thermal Resistance (Junction-to-Air)	$R_{\theta JA}$	100	°C/W
Operating Temperature Range TCA5600 TCF5600	T_A	 0 to +75 −40 to +85	°C
Operating Junction Temperature TCA5600 TCF5600	T_J	 +125 +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES: 1. Values beyond which damage may occur.
2. Derate at 10 mW/°C for junction temperature above +75°C (TCA5600).
Derate at 10 mW/°C for junction temperature above +85°C (TCF5600).

Functional Block Diagram



ELECTRICAL CHARACTERICISTICS ($V_{CC1} = V_{CC2} = 12$ V; $T_J = 25°C$; $I_{ref} = 0$; $I_{out1} = 0$ (Note 3); $R_{SC} = 0.5\ \Omega$; INH = HIGH INH2 = HIGH; $\overline{WDS}$ = HIGH; $I_{out2} = 0$ (Note 4); unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION						
Nominal Reference Voltage	1	$V_{ref\ nom}$	2.42	2.5	2.58	V
Reference Voltage $I_{ref} = 0.5$ mA, $T_{low} \le T_J \le T_{high}$ (Note 5), $6.0\ V \le V_{CC1} \le 18$ V		V_{ref}	2.4	—	2.6	V
Line Regulation ($6.0\ V \le V_{CC2} \le 18$ V)		Reg_{line}	—	2.0	15	mV
Average Temperature Coefficient $T_{low} \le T_J \le T_{high}$ (Note 5)	2	$\frac{\Delta V_{ref}}{\Delta T_J}$	—	—	+/– 0.5	mV/°C
Ripple Rejection Ratio f = 1.0 kHz, $V_{sin} = 1.0\ V_{pp}$	3	RR	60	70	—	dB
Output Impedance $0 \le I_{ref} \le 2.0$ mA		Z_O	—	1.0	—	Ω
Standby Current Consumption V_{CC2} = Open	4	I_{CC1}	—	3.0	—	mA
5.0 V MICROPROCESSOR VOLTAGE REGULATOR SECTION						
Nominal Output Voltage		$V_{out1(nom)}$	4.8	5.0	5.2	V
Output Voltage $5.0\ mA \le I_{out1} \le 300$ mA, $T_{low} \le T_J \le T_{high}$ (Note 5) $6.0\ V \le V_{CC2} \le 18$ V	5 6	V_{out1}	4.75	—	5.25	V
Line Regulation ($6.0\ V \le V_{CC2} \le 18$ V)		Reg_{line}	—	10	50	mV
Load Regulation ($5.0\ mA \le I_{out1} \le 300$ mA)		Reg_{load}	—	20	100	mV
Base Current Drive ($V_{CC2} = 6.0$ V, $V_{15} = 4.0$ V)		I_B	10	15	—	mA
Ripple Rejection Ratio f = 1.0 kHz, $V_{sin} = 1.0\ V_{pp}$	3	RR	50	65	—	dB
Undervoltage Detection Level ($R_{SC} = 5.0\ \Omega$)	7	V_{low}	4.5	$0.93 \times V_{out1}$	—	V
Current Limitation Threshold ($R_{SC} = 5.0\ \Omega$)		V_{RSC}	210	250	290	mV
Average Temperature Coefficient $T_{low} \le T_J \le T_{high}$ (Note 5)		$\frac{\Delta V_{out1}}{\Delta T_J}$	—	—	±1.0	mV/°C
DC/DC CONVERTER SECTION						
Collector Current Detection Level HIGH RC = 10 k LOW	9	$V_{12(H)}$ $V_{12(L)}$	350 —	400 50	450 —	mV
Collector Saturation Voltage $I_C = 600$ mA (Note 7)	10	$V_{CE(sat)}$	—	—	1.6	V
Rectifier Forward Voltage Drop $I_F = 600$ mA (Note 7)	11	V_F	—	—	1.4	V

NOTES: 3. The external PNP power transistor satisfies the following minimum specifications:
$h_{FE} \ge 60$ at $I_C = 500$ mA and $V_{CE} = 5.0$ V; $V_{CE(sat)} \le 300$ mV at $I_B = 10$ mA and $I_C = 300$ mA
4. Regulator V_{out2} programmed for nominal 24 V output by means of R4, R5 (see Figure 1).
5. T_{low} = 0°C for TCA5600 T_{low} = –40°C for TCF5600
T_{high} = +125°C for TCA5600 T_{high} = +150°C for TCF5600
7. Pulse tested $t_p \le 300\ \mu s$.

ELECTRICAL CHARACTERICISTICS (V_{CC1} = V_{CC2} = 12 V; T_J = 25°C; I_{ref} = 0; I_{out1} = 0 (Note 3); R_{SC} = 0.5 Ω; INH = HIGH INH2 = HIGH; $\overline{WDS}$ = HIGH; I_{out2} = 0 (Note 4); unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
PROGRAMMABLE VOLTAGE REGULATOR SECTION (Note 6)					
Nominal Output Voltage	$V_{out2(nom)}$	23	24	25	V
Output Voltage (Figure 8) 1.0 mA ≤ I_{out2} ≤ 100 mA, T_{low} ≤ T_J ≤ T_{high} (Notes 5, 7)	V_{out2}	22.8	—	25.2	V
Load Regulation 1.0 mA ≤ I_{out2} ≤ 100 mA (Note 7)	Reg_{load}	—	40	200	mV
DC Output Current	I_{out2}	100	—	—	mA
Peak Output Current (Internally Limited)	$I_{out2\ p}$	150	200	—	mA
Ripple Rejection Ratio f = 20 kHz, V = 0.4 V_{pp}	RR	45	55	—	dB
Output Voltage (Fixed 5.0 V) 1.0 mA ≤ I_{out2} ≤ 20 mA, T_{low} ≤ T_J ≤ T_{high} INH1 = HIGH (Note 5)	$V_{out2(5.0\ V)}$	4.75	—	5.25	V
Off State Output Impedance (INH2 = LOW)	R_{out1}	—	10	—	kΩ
Average Temperature Coefficient T_{low} ≤ T_J ≤ T_{high} (Note 5)	$\frac{\Delta V_{out2}}{\Delta T_J V_{out2}}$	—	—	±0.25	mV/°C V
WATCHDOG AND $\overline{RESET}$ CIRCUIT SECTION					
Threshold Voltage HIGH (Static) LOW	$V_{C5(H)}$ $V_{C5(L)}$	— —	2.5 1.0	— —	V
Current Source T_{low} ≤ T_J ≤ T_{high} (Note 5) Power-Up $\overline{RESET}$ Watchdog Time Out Watchdog $\overline{RESET}$	I_{C5}	 −1.8 — —	 −2.5 5×I_{C5} −50×I_{C5}	 −3.2 — —	µA
Watchdog Input Voltage Swing	V_{WDI}	—	—	±5.5	V
Watchdog Input Impedance	r_i	12	15	—	kΩ
Watchdog Reset Pulse Width (C8 = 1.0 nF) (Note 9)	t_p	—	—	10	µs
DIGITAL PORTS: $\overline{WDS}$, INH 1, INH 2, $\overline{RESET}$ (Note 8)					
Input Voltage Range	V_{INP}	—	—	−0.3 to V_{CC1}	V
Input HIGH Current 2.0 V ≤ V_{IH} ≤ 5.5 V 5.5 V ≤ V_{IH} ≤ V_{CC1}	I_{IH}	 — —	 — —	 100 150	µA
Input LOW Current −0.3 V ≤ V_{IL} ≤ 0.8 V for INH1, INH2, −0.3 V ≤ V_{IL} ≤ 0.4 V for $\overline{WDS}$	I_{IL}	—	—	−100	µA
Leakage Current Immunity (INH2, High "Z" State) (Figure 12)	I_Z	±20	—	—	µA
Output LOW Voltage $\overline{RESET}$ (I_{OL} = 6.0 mA)	V_{OL}	—	—	0.4	V
Output HIGH Voltage $\overline{RESET}$ (V_{OH} = 5.5 V)	V_{OH}	—	—	20	µA

NOTES: 6. V_9 = 28 V, INH1 = LOW for this Electrical Characteristic section unless otherwise noted.
7. Pulse tested t_p ≤ 300 µs.
8. Temperature range T_{low} ≤ T_J ≤ T_{high} applies to this Electrical Characteristics section.
9. For test purposes, a negative pulse is applied to Pin 4 (−2.5 V ≥ V_4 ≥ −5.5 V).

Figure 1. Reference Voltage versus Supply Voltage

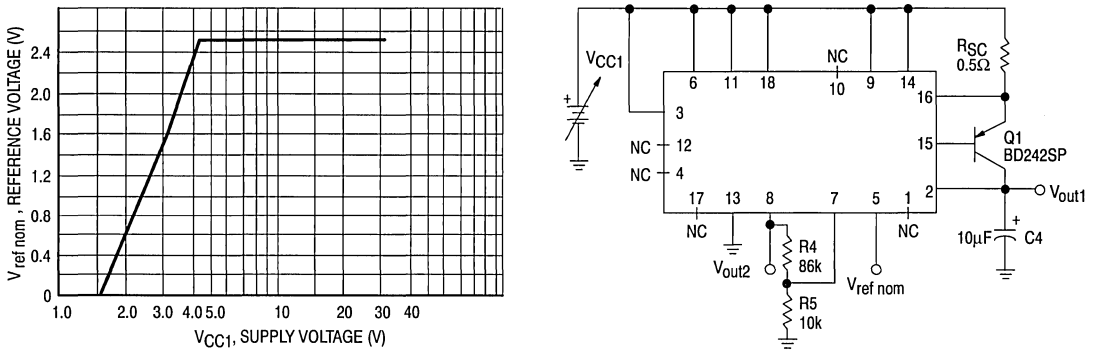


Figure 2. Reference Stability versus Temperature

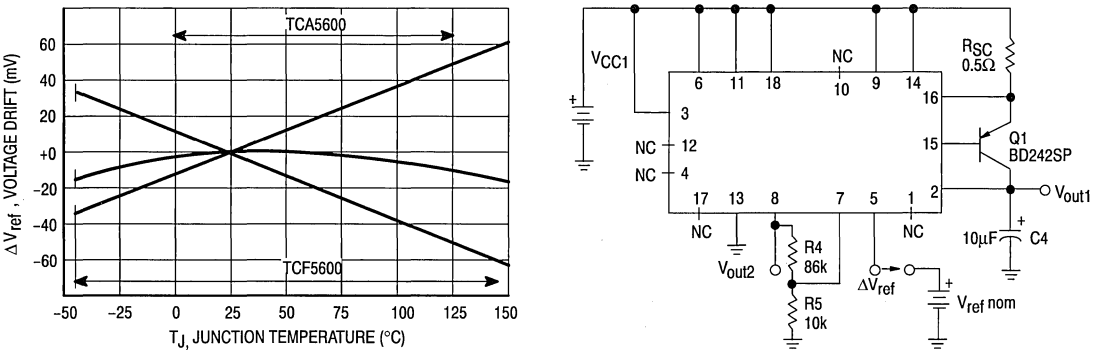


Figure 3. Ripple Rejection versus Frequency

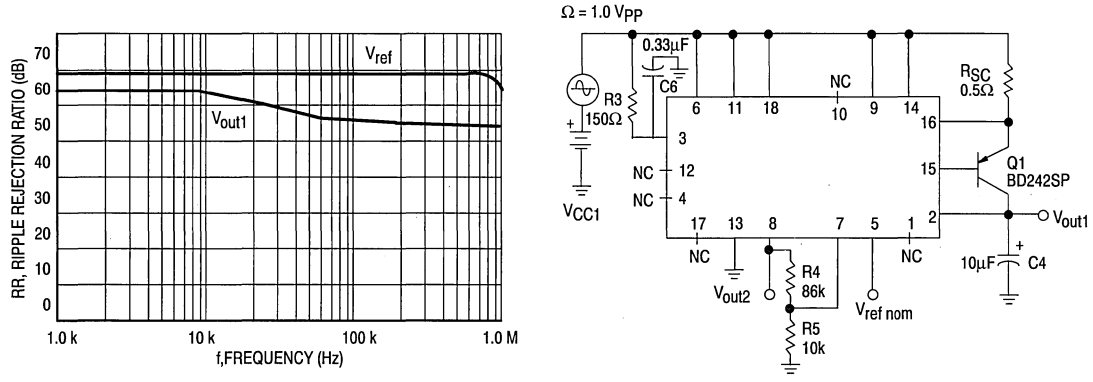


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Figure 4. Stand-By Current versus Supply Voltage

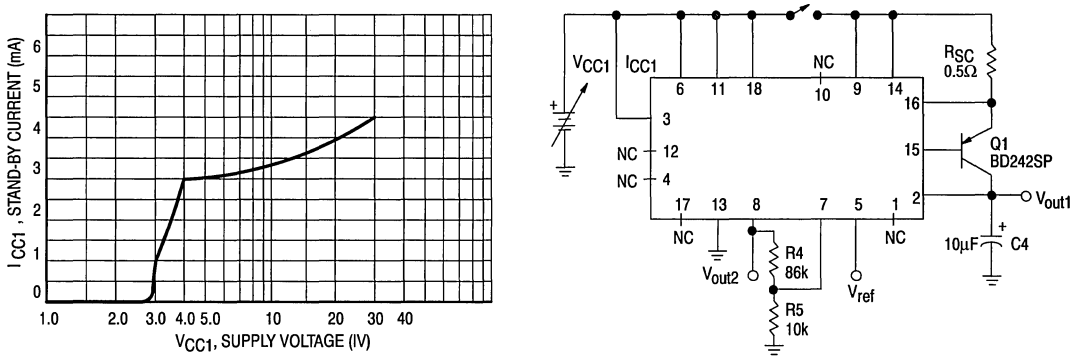


Figure 5. Power-Up Behavior of the 5.0 V Regulator

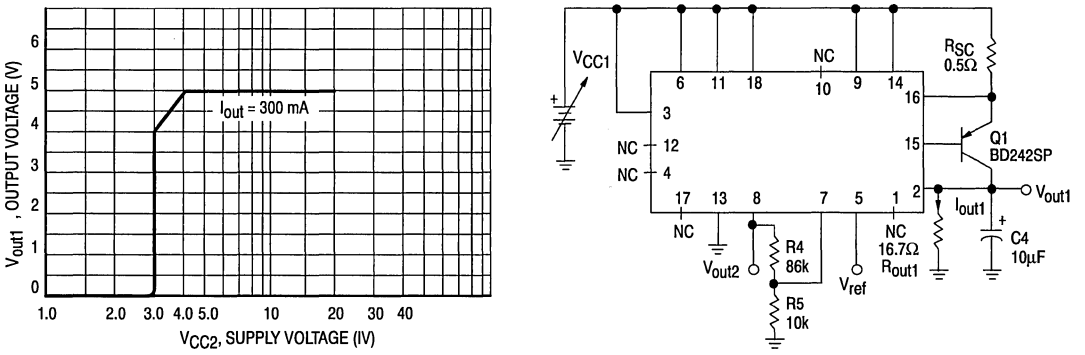


Figure 6. Foldback Characteristics of the 5.0 V Regulator

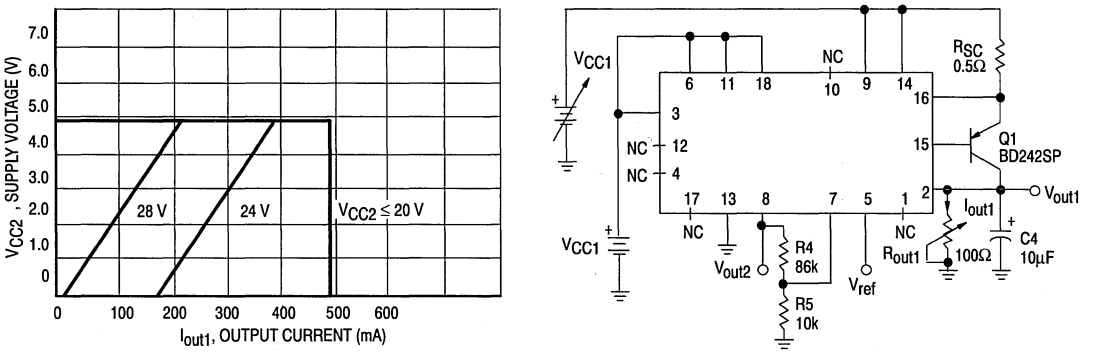
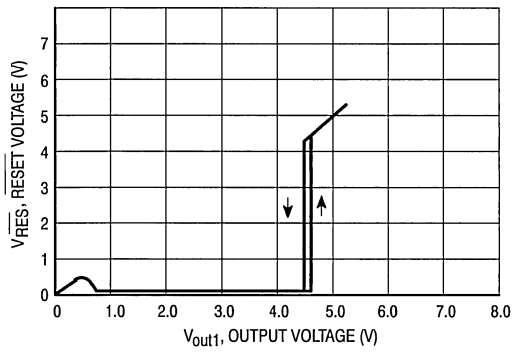


Figure 7. Undervoltage Lockout Characteristics



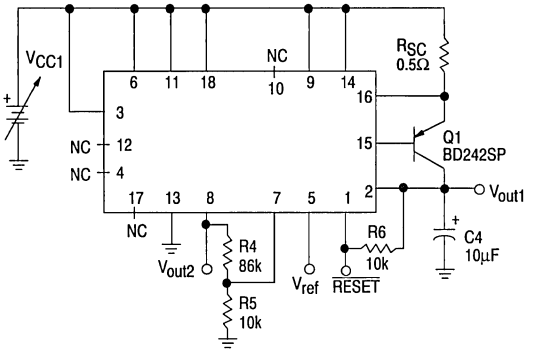
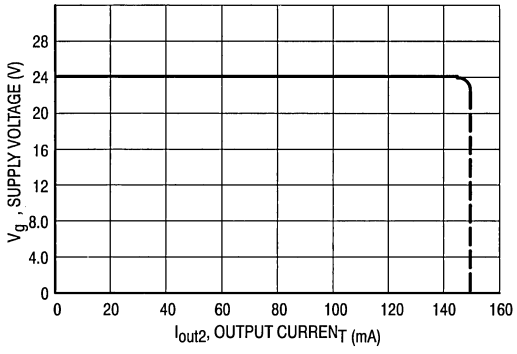


Figure 8. Output Current Capability of the Programming Regulator



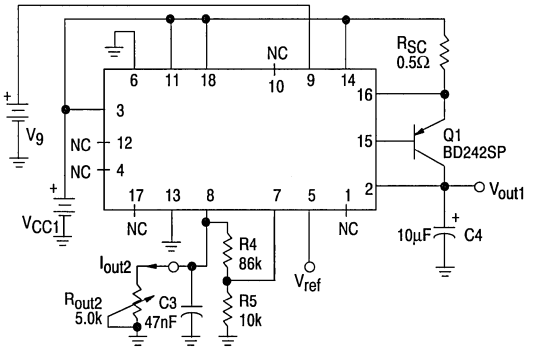
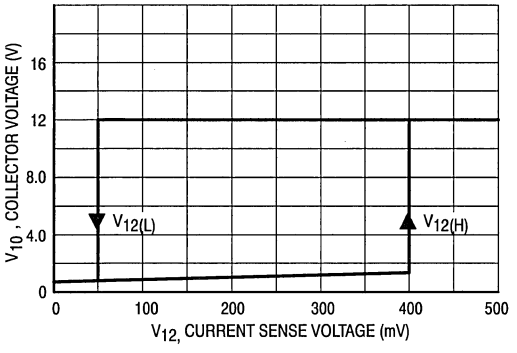
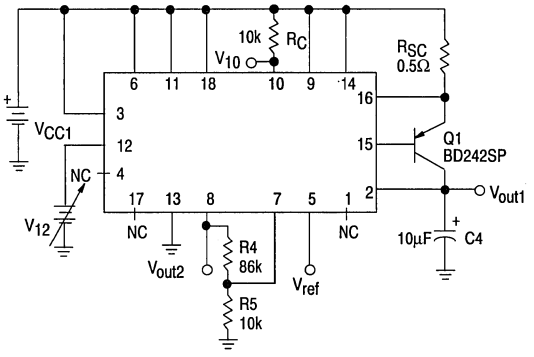


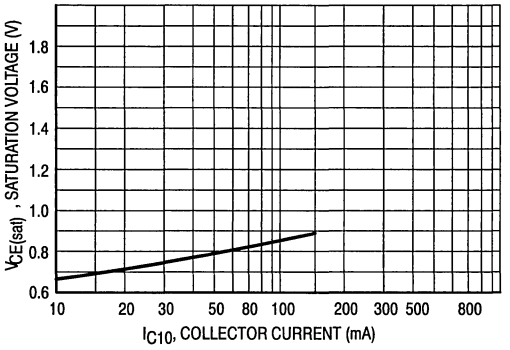
Figure 9. Collector Current Detection Level





3

Figure 10. Power Switch Characteristics



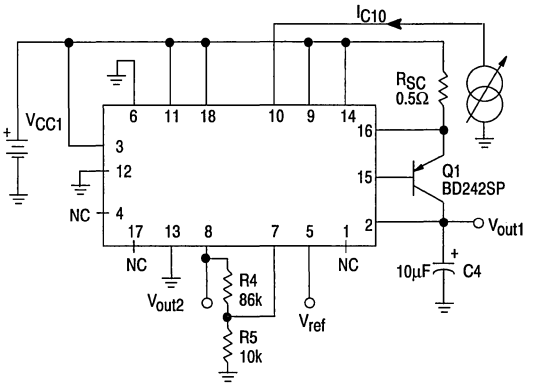
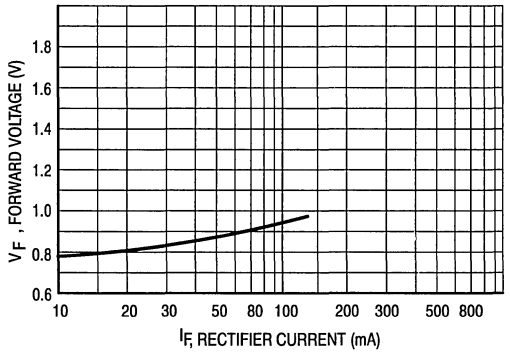


Figure 11. Rectifier Characteristics



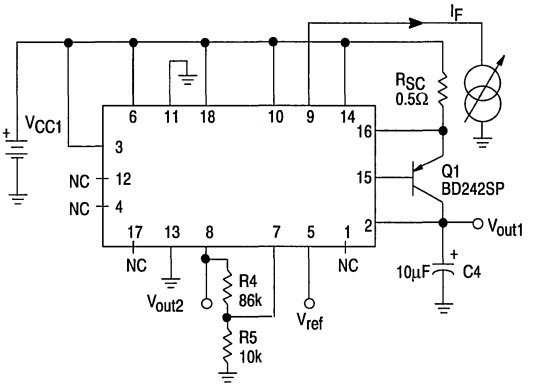
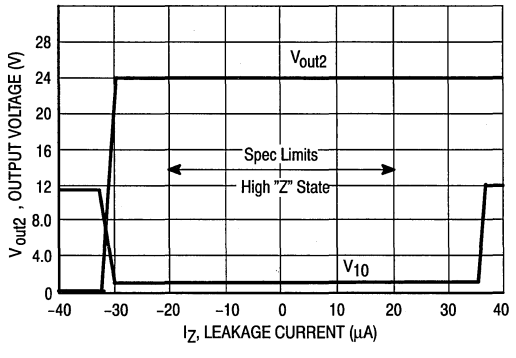
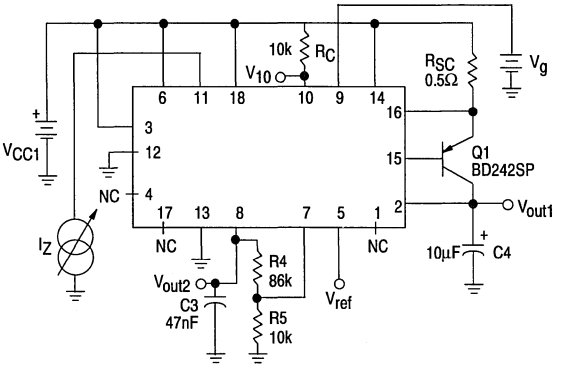


Figure 12. INH 2 Leakage Current Immunity





APPLICATION INFORMATION

(See Figure 18)

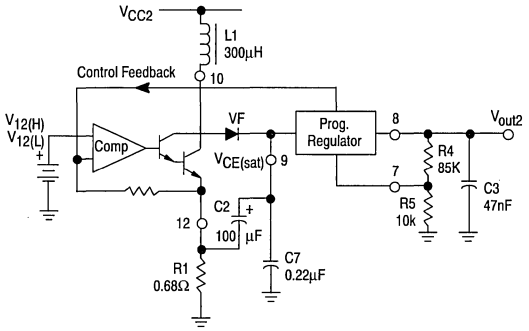
Voltage Reference (V_{ref})

The voltage reference V_{ref} is based upon a highly stable bandgap voltage reference and is accessible on Pin 5 for additional tasks. This circuit part has its own supply connection on Pin 3 and is, therefore, able to operate in standby mode. The RC network R3, C6 improves the ripple rejection on both regulators.

DC/DC Converter

The DC/DC converter performs according to the flyback principle and does not need a time base circuit. The maximum coil current is well defined by means of the current sensing resistor R1 under all working conditions (start-up phase, circuit overload, wide supply voltage range and extreme load current change). Figure 13 shows the Simplified Converter Schematic.

Figure 13. Simplified Converter Schematic



A simplified method on "how to calculate the coil inductance" is given below. The operation point at minimum supply voltage (V_{CC2}) and max. output current (I_{out2}) for a fixed output voltage (V_{out2}) determines the coil data. Figure 14 shows the typical voltage and current waveforms on the coil L1 (coil losses neglected).

Equations (1) and (2) yield the respective coil voltage V_L- and V_L+ (see Figure 14):

$$V_L+ = V_{out2} + \Delta V_{(Pin\ 9\ -\ Pin\ 8)} + V_F - V_{CC2} \quad (1)$$

$$V_L- = V_{CC2} - V_{CE(sat)} - V_{12(H)} \quad (2)$$

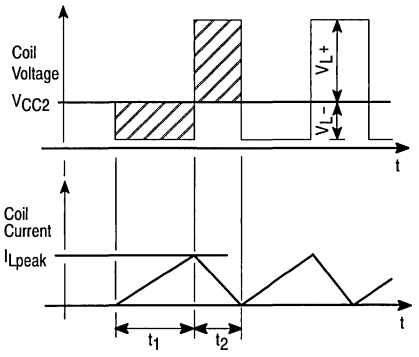
[$\Delta V_{(Pin\ 9\ -\ Pin\ 8)}$: input/output voltage drop of the regulator, 2.5 V typical]

[V_F, $V_{CE(sat)}$, $V_{12(H)}$: see Electrical Characteristics Table]

The time ratio α for the charging time to dumping time is defined by Equation (3):

$$\alpha = \frac{t_1}{t_2} = \frac{V_L+}{V_L-} \quad (3)$$

Figure 14. Voltage and Current Waveform on the Coil (not to scale)



The coil charging time t_1 is found using Equation (4):

$$t_1 = \frac{1}{(1 + \frac{1}{\alpha}) \cdot f} \quad (4)$$

[f : minimum oscillation frequency which should be chosen above the audio frequency band (e.g. 20 kHz)]

Knowing the DC output current I_{out2} of the programmable regulator, the peak coil current $I_{L(peak)}$ can now be calculated:

$$I_{L(peak)} = 2 \cdot (I_{out2})\ (1 + \alpha) \quad (5)$$

The coil inductance L1 of the nonsaturated coil is given by Equation (6):

$$L1 = \frac{t_1}{I_{L(peak)}}\ (V_L-) \quad (6)$$

The formula (6a) yields the current sensing resistor R1 for a defined peak coil current $I_{L(peak)}$:

$$R1 = \frac{V_{12(H)}}{I_{L(peak)}} \quad (6a)$$

In order to limit the by-pass current through capacitor C7 during the energy dumping phase the value C2>>C7 should be implemented.

For all other operation conditions, the feedback signal from the programmable voltage regulator controls the activity of the converter.

3

Programmable Voltage Regulator

This series voltage regulator is programmable by the voltage divider R4, R5 for a nominal output voltage of 6.0 V ≤ V_{out2} ≤ 30 V.

$$R4 = \frac{(V_{out2} - V_{ref\ nom}) \bullet R5}{V_{ref\ nom}} \quad (7)$$

[R5 = 10 k, $V_{ref\ nom}$ = 2.5 V]

Current limitation and thermal shutdown capability are standard features of this regulator. The voltage drop $\Delta V_{(Pin\ 9 - Pin\ 8)}$ across the series pass transistor generates the feedback signal to control the DC/DC converter (see Figure 13).

Control Inputs INH1, INH2

The DC/DC converter and/or the regulator V_{out2} are remote controllable through the TTL, MOS compatible inhibit inputs INH1 and INH2 where the latter is a three-level detector (Logic "0", High Impedance "Z", Logic "1"). Both inputs are set-up to provide the following truth table:

Figure 15. INH1, INH2 TruthTable

Mode	INH1	INH2	V_{out2}	DC/DC
1	0	0	OFF	INT
2	0	High "Z"	V_{out2}	ON
3	0	1	V_{out2}	INT
4	1	0	OFF	INT
5	1	High "Z"	5.0 V	ON
6	1	1	5.0 V	INT

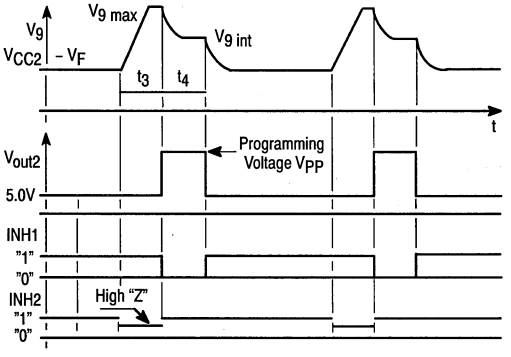
INT: Intermittent operation of the converter means that the converter operates only if $V_{CC2} < V_{out2}$.

ON: The converter loads the storage capacitor C2 to its full charge (V_9 = 33 V), allowing fast response time of the regulator V_{out2} when addressed by the control software.

OFF: High impedance (internal resistor 10 k to ground)

Figure 16 represents a typical timing diagram for an E²PROM programming sequence in a microprocessor based system. The High "Z" state enables the DC/DC converter to ramp during t_3 to the voltage V_9 at Pin 9 to a high level before the write cycle takes place in the memory.

Figure 16. Typical E²PROM Programming Sequence
(not to scale)



Microprocessor Supply Regulator

Together with an external PNP power transistor (Q1), a 5.0 V supply exhibiting low voltage drop is obtained to power microprocessor systems and auxiliary circuits. Using a power Darlington with adequate heat sink in the output stage boosts the output current I_{out1} above 1.0 A.
The current limitation circuit measures the emitter current of Q1 by means of the sensing resistor, R_{SC}:

$$R_{SC} = \frac{V_{RSC}}{I_E} \quad (8)$$

[I_E: emitter current of Q1]

[V_{RSC}: threshold voltage (see Electrical Characteristics Table)]

The voltage protection circuit performs a foldback characteristic above a nominal operating voltage, $V_{CC2} \geq 18$ V.

Delay and Watchdog Circuit

The undervoltage monitor supervises the power supply V_{out1} and releases the delay circuit $\overline{RESET}$ as soon as the regulator output reaches the microprocessor operating a range [e.g., $V_{low} \geq 0.93 \bullet V_{out1(nom)}$]. The $\overline{RESET}$ output has an open-collector and may be connected in a "wired-OR" configuration.

The watchdog circuit consists of a retriggerable monostable with a negative edge sensitive control input WDI. The watchdog feature may be disabled by means of the watchdog select input $\overline{WDS}$ driven to a "1". Figure 17 displays the Typical $\overline{RESET}$ Timing Diagram.

The commuted current source I_{C5} on Pin 17, threshold voltage $V_{C5(L)}$, $V_{C5(H)}$ and an external capacitor C5 define the $\overline{RESET}$ delay and the watchdog timing. The relationship of the timing signals are indicated by the Equations (9) to (11).

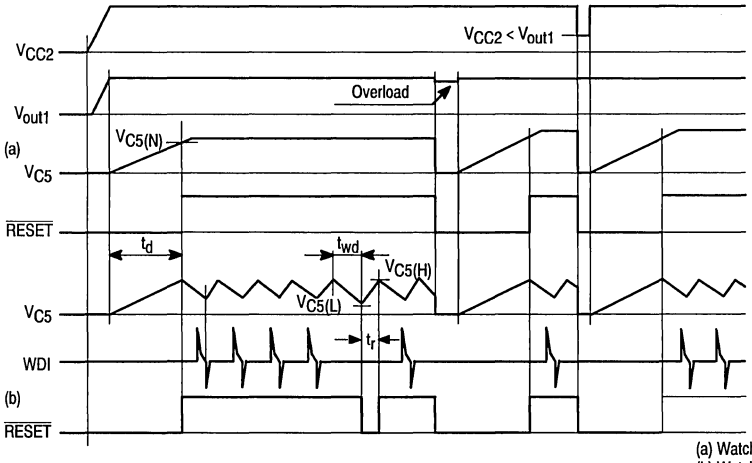
$$\overline{RESET}\ \text{delay:}\quad t_d = \frac{C5 \bullet V_{C5(H)}}{|I_{C5}|} \quad (9)$$

$$\text{Watchdog timeout:}\quad t_{wd} = \frac{C5 \bullet (V_{C5(H)} - V_{C5(L)})}{5 \bullet I_{C5}} \quad (10)$$

$$\text{Watchdog } \overline{RESET}\text{:}\quad t_r = \frac{C5 \bullet (V_{C5(H)} - V_{C5(L)})}{50 \bullet |I_{C5}|} \quad (11)$$

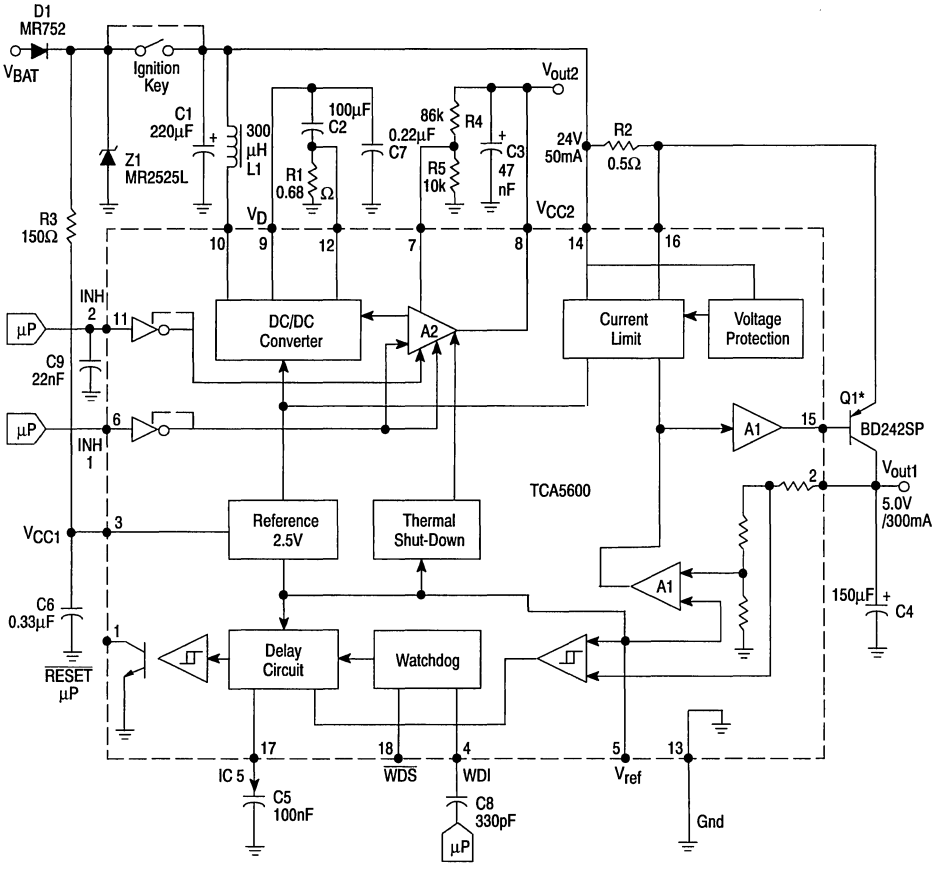
[I_{C5}, $V_{C5(H)}$, $V_{C5(L)}$: see Electrical Characteristics Table]

Figure 17. Typical $\overline{\text{RESET}}$ Timing Diagram (not to scale)



(a) Watchdog inhibited, $\overline{\text{WDS}}$ = "1"
(b) Watchdog operational, $\overline{\text{WDS}}$ = "0"

Figure 18. Typical Automative Application



TL494

3

Switchmode Pulse Width Modulation Control Circuit

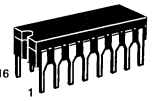
The TL494 is a fixed frequency, pulse width modulation control circuit designed primarily for SWITCHMODE power supply control.

This device features:

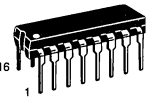
- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator with Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 V Reference
- Adjustable Dead-Time Control
- Uncommitted Output Transistors Rated to 500 mA Source or Sink
- Output Control for Push-Pull or Single-Ended Operation
- Undervoltage Lockout

SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUITS

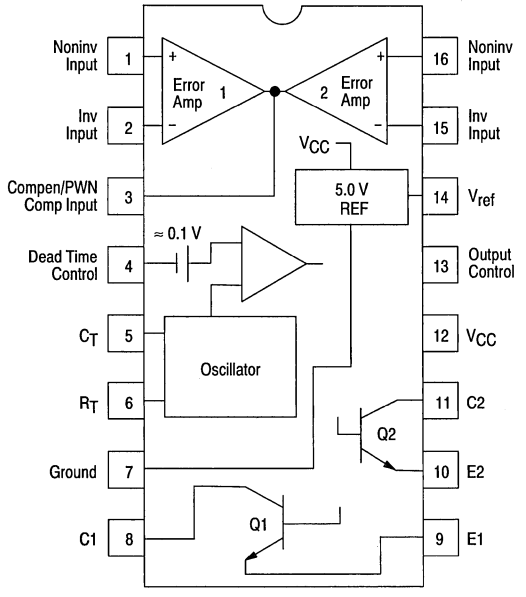


J SUFFIX
CERAMIC PACKAGE
CASE 620



N SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
TL494CN	0° to +70°C	Plastic
TL494CJ		Ceramic
TL494IN	–25° to +85°C	Plastic
TL494IJ		Ceramic
TL494MJ	–55° to +125°C	Ceramic

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	TL494C	TL494I	TL494M	Unit
Power Supply Voltage	V_{CC}	42			V
Collector Output Voltage	V_{C1}, V_{C2}	42			V
Collector Output Current (Each transistor) (Note 1)	I_{C1}, I_{C2}	500			mA
Amplifier Input Voltage Range	V_{IR}	−0.3 to +42			V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000			mW
Operating Junction Temperature Plastic Package	T_J	125		—	°C
Ceramic Package		150			
Storage Temperature Range Plastic Package	T_{stg}	−55 to +125		—	°C
Ceramic Package		−65 to +150			
Operating Ambient Temperature Range	T_A	0 to +70	−25 to +85	−55 to +125	°C

NOTES: 1. Maximum thermal limits must be observed.

THERMAL CHARACTERISTICS

Characteristics	Symbol	N Suffix	J Suffix	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	80	100	°C/W
Derating Ambient Temperature	T_A	45	50	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	TL494			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	—	30	40	V
Collector Output Current (Each transistor)	I_{C1}, I_{C2}	—	—	200	mA
Amplified Input Voltage	V_{in}	−0.3	—	V_{CC} − 2.0	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	30	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz

ELECTRICAL CHARACTERICISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ, unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating abmient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	TL494C,I			TL494M			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Voltage (I_O = 1.0 mA)	V_{ref}	4.75	5.0	5.25	4.75	5.0	5.25	V
Line Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	—	2.0	25	—	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	3.0	15	—	3.0	15	mV
Short Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	15	35	75	mA
OUTPUT SECTION								
Collector Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	—	2.0	100	—	2.0	100	μA
Emitter Off-State Current V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	—	—	–100	—	—	–150	μA
Collector-Emitter Saturation Voltage (Note 2)								V
Common-Emitter (V_E = 0 V, I_C = 200 mA)	$V_{sat(C)}$	—	1.1	1.3	—	1.1	1.5	
Emitter-Follower (V_C = 15 V, I_E = –200 mA)	$V_{sat(E)}$	—	1.5	2.5	—	1.5	2.5	
Output Control Pin Current								
Low State (V_{OC} ≤ 0.4 V)	I_{OCL}	—	10	—	—	10	—	μA
High State (V_{OC} = V_{ref})	I_{OCH}	—	0.2	3.5	—	0.2	3.5	mA
Output Voltage Rise Time	t_r							ns
Common-Emitter (See Figure 12)		—	100	200	—	100	200	
Emitter-Follower (See Figure 13)		—	100	200	—	100	200	
Output Voltage Fall Time	t_f							ns
Common-Emitter (See Figure 12)		—	25	100	—	25	100	
Emitter-Follower (See Figure 13)		—	40	100	—	40	100	

NOTE: 2.Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

Characteristics	Symbol	TL494 Min	TL494 Typ	TL494 Max	Unit
ERROR AMPLIFIER SECTION					
Input Offset Voltage ($V_{O\ (Pin\ 3)}$ = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current ($V_{O\ (Pin\ 3)}$ = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias Current ($V_{O\ (Pin\ 3)}$ = 2.5 V)	I_{IB}	—	–0.1	–1.0	µA
Input Common Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)	V_{ICR}	–0.3 to V_{CC}–2.0			V
Open-Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	—	dB
Unity-Gain Crossover Frequency (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	f_{C-}	—	350	—	kHz
Phase Margin at Unity-Gain (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	—	65	—	deg.
Common Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90	—	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	—	100	—	dB
Output Sink Current ($V_{O\ (Pin\ 3)}$ = 0.7 V)	I_{O-}	0.3	0.7	—	mA
Output Source Current ($V_{O\ (Pin\ 3)}$ = 3.5 V)	I_{O+}	2.0	–4.0	—	mA
PWM COMPARATOR SECTION (Test Circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	—	2.5	4.5	V
Input Sink Current ($V_{(Pin\ 3)}$ = 0.7 V)	I_{I-}	0.3	0.7	—	mA
DEAD-TIME CONTROL SECTION (Test Circuit Figure 11)					
Input Bias Current (Pin 4) ($V_{Pin\ 4}$ = 0 V to 5.25 V)	$I_{IB\ (DT)}$	—	–2.0	–10	µA
Maximum Duty Cycle, Each Output, Push-Pull Mode ($V_{Pin\ 4}$ = 0 V, C_T = 0.01 µF, R_T = 12 kΩ) ($V_{Pin\ 4}$ = 0 V, C_T = 0.001 µF, R_T = 30 kΩ)	DC_{max}	 45 —	 48 45	 50 50	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	 — 0	 2.8 —	 3.3 —	V
OSCILLATOR SECTION					
Frequency (C_T = 0.001 µF, R_T = 30 kΩ)	f_{osc}	—	40	—	kHz
Standard Deviation of Frequency* (C_T = 0.001 µF, R_T = 30 kΩ)	σf_{osc}	—	3.0	—	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Δf_{osc} (ΔV)	—	0.1	—	%
Frequency Change with Temperature ($\Delta T_A = T_{low}$ to T_{high}) (C_T = 0.01 µF, R_T = 12 kΩ)	Δf_{osc} (ΔT)	—	—	12	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn-On Threshold (V_{CC} increasing, I_{ref} = 1.0 mA)	V_{th}	5.5	6.43	7.0	V
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, All other inputs and outputs open) (V_{CC} = 15 V) (V_{CC} = 40 V)	I_{CC}	 — —	 5.5 7.0	 10 15	mA
Average Supply Current (C_T = 0.01 µF, R_T = 12 kΩ, ($V_{(Pin\ 4)}$ = 2.0 V) V_{CC} = 15 V) (See Figure 12)	—	—	7.0	—	mA

* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \overline{X})^2}{N-1}}$

Figure 1. Block Diagram

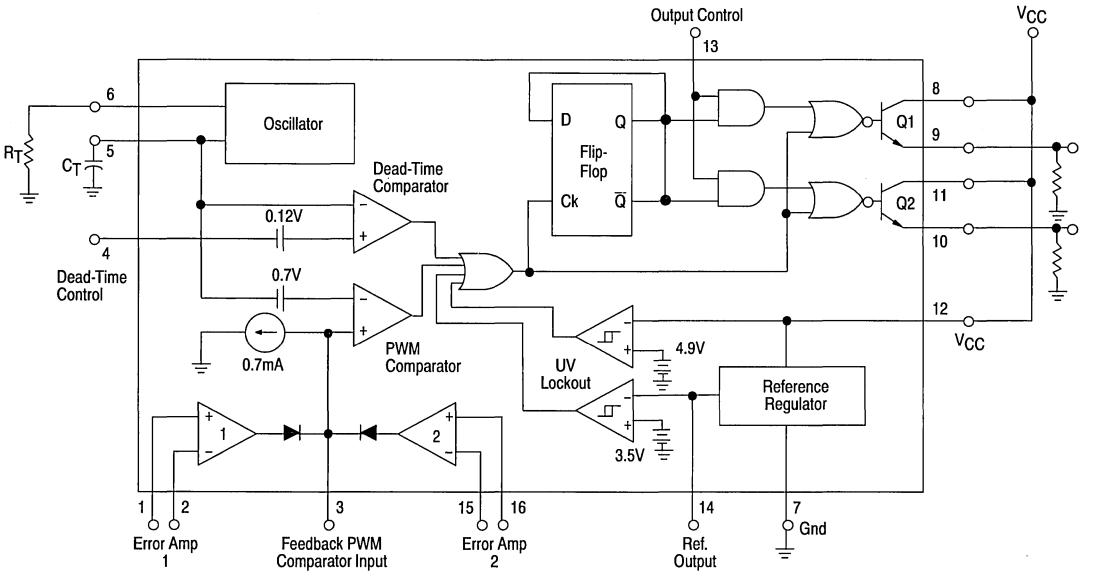
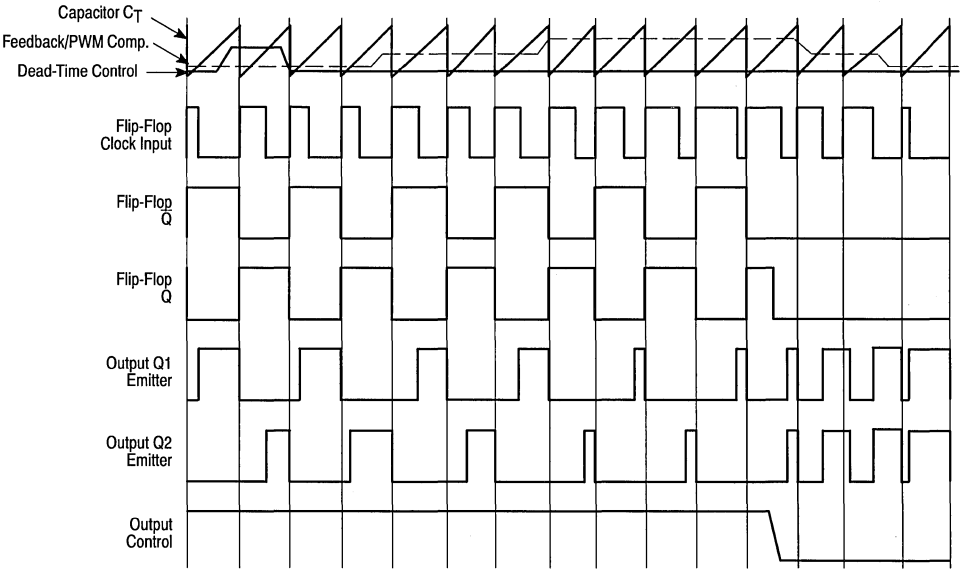


Figure 2. Timing Diagram



APPLICATIONS INFORMATION

Description

The TL494 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 V to 3.3 V.

Functional Table

Input/Output Controls	Output Function	$\frac{f_{out}}{f_{osc}}$ =
Grounded	Single-ended PWM @ Q1 and Q2	1.0
@ V_{ref}	Push-pull Operation	0.5

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common mode input range from –0.3 V to (V_{CC} – 2V), and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the noninverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the dead-time comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on-time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The TL494 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±5.0% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to 70°C.

Figure 3. Oscillator Frequency versus Timing Resistance

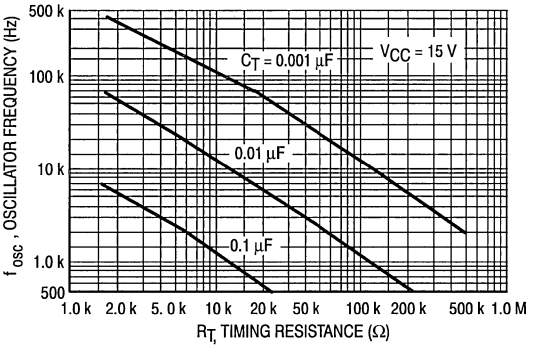


Figure 4. Open-Loop Voltage Gain and Phase versus Frequency

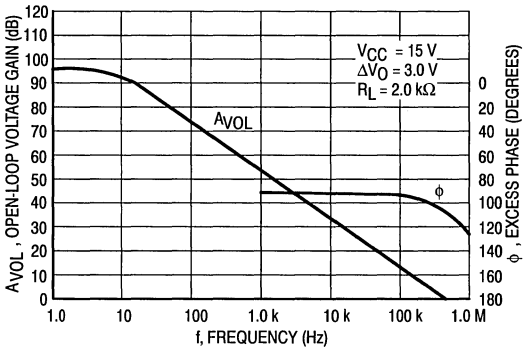


Figure 5. Percent Dead-Time versus Oscillator Frequency

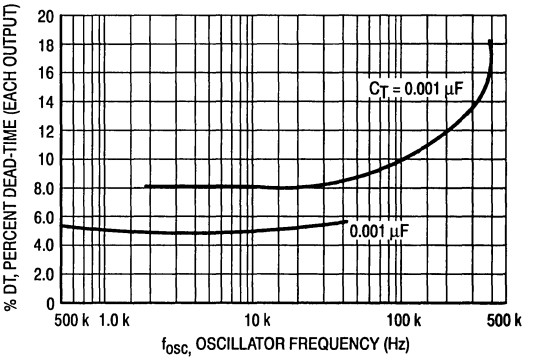


Figure 6. Percent Duty Cycle versus Dead-Time Control Voltage

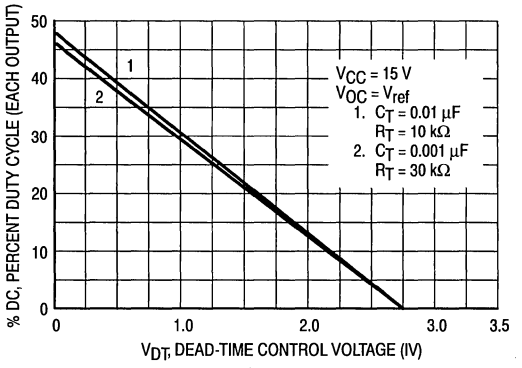


Figure 7. Emitter-Follower Configuration Output Saturation Voltage versus Emitter Current

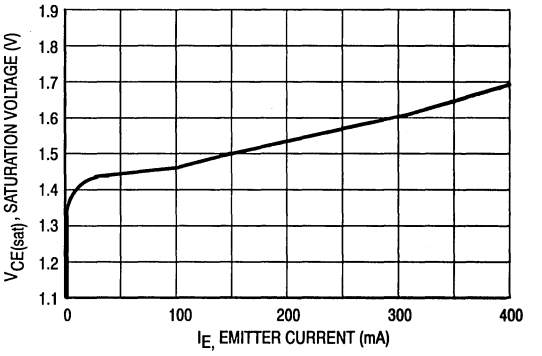


Figure 8. Common-Emitter Configuration Output Saturation Voltage versus Collector Current

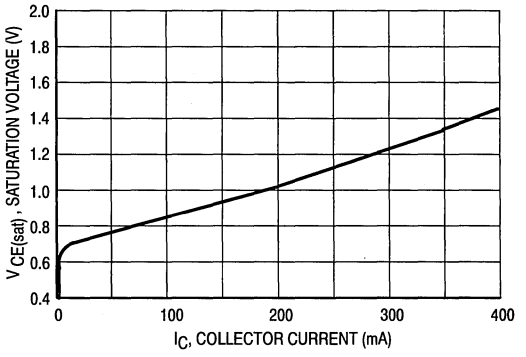


Figure 9. Standby Supply Current versus Supply Voltage

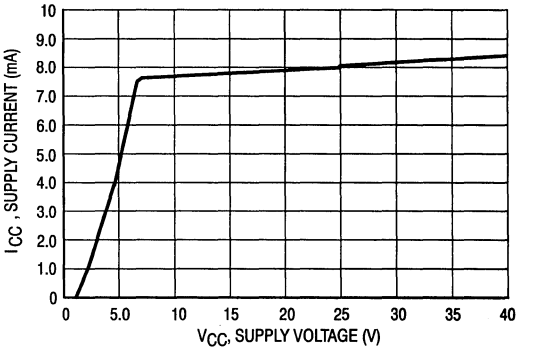


Figure 10. Error-Amplifier Characteristics

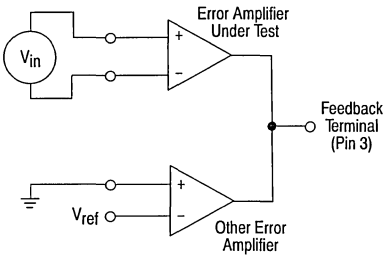


Figure 11. Dead-Time and Feedback Control Circuit

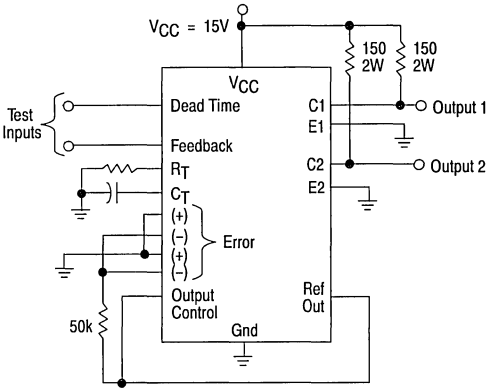


Figure 12. Common-Emitter Configuration Test Circuit and Waveform

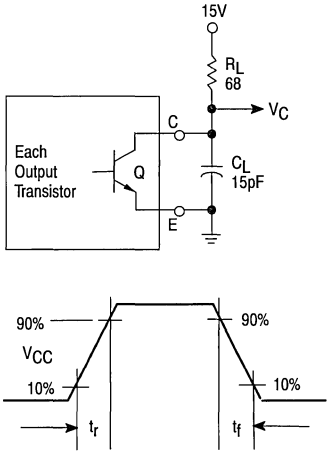


Figure 13. Emitter-Follower Configuration Test Circuit and Waveform

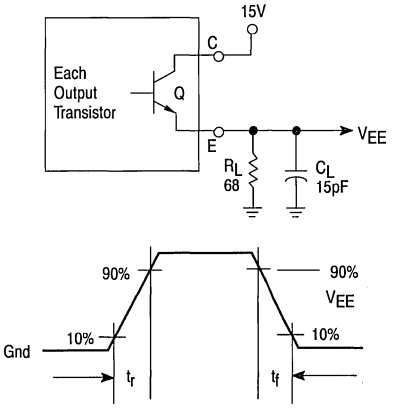
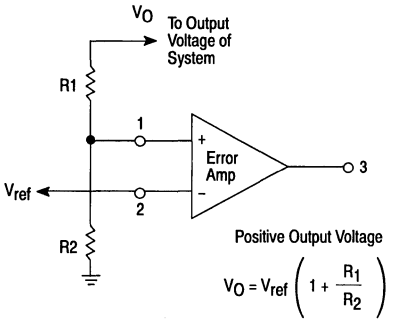


Figure 14. Error-Amplifier Sensing Techniques



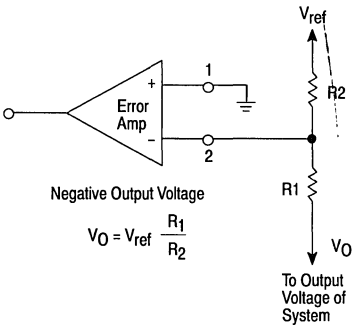


Figure 15. Dead-Time Control Circuit

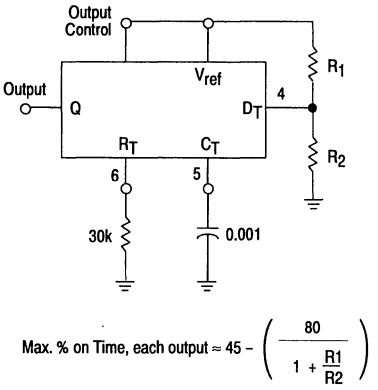


Figure 16. Soft-Start Circuit

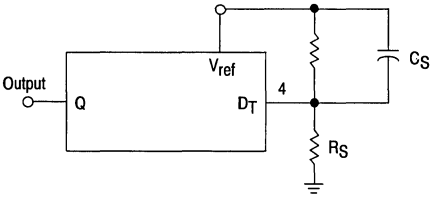
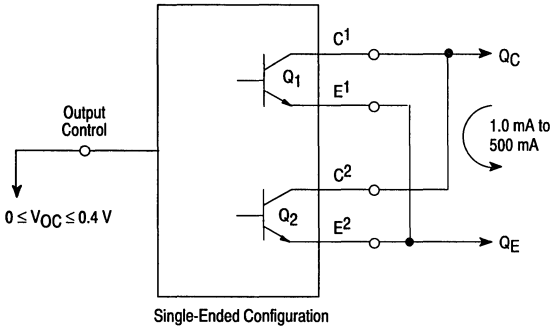


Figure 17. Output Connections for Single-Ended and Push-Pull Configurations



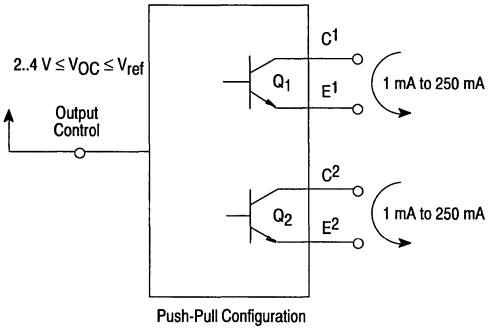


Figure 18. Slaving Two or More Control Circuits

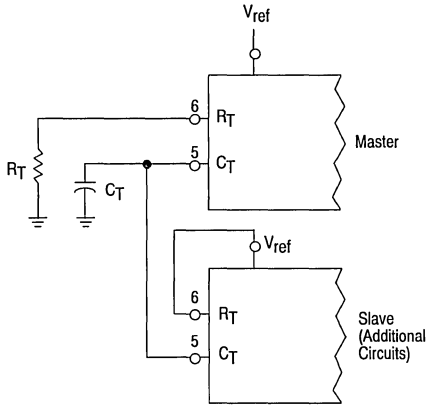


Figure 19. Operation with V_{in} > 40 V Using External Zener

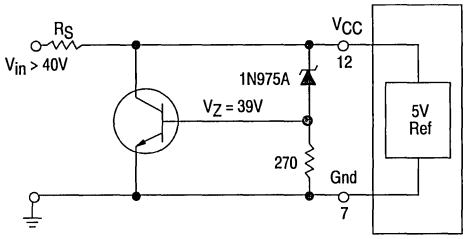
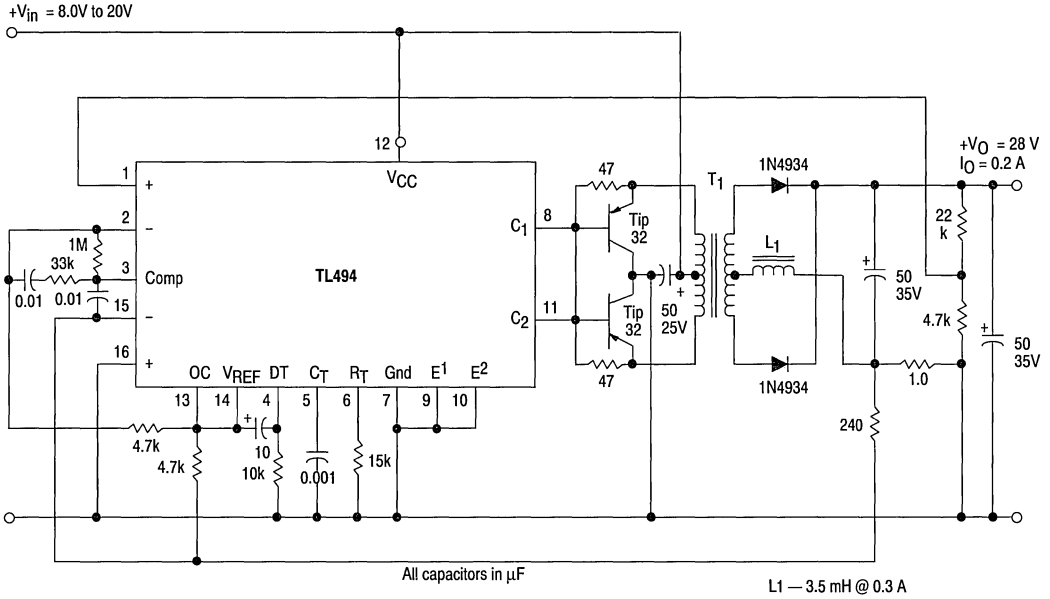


Figure 20. Pulse Width Modulated Push-Pull Converter

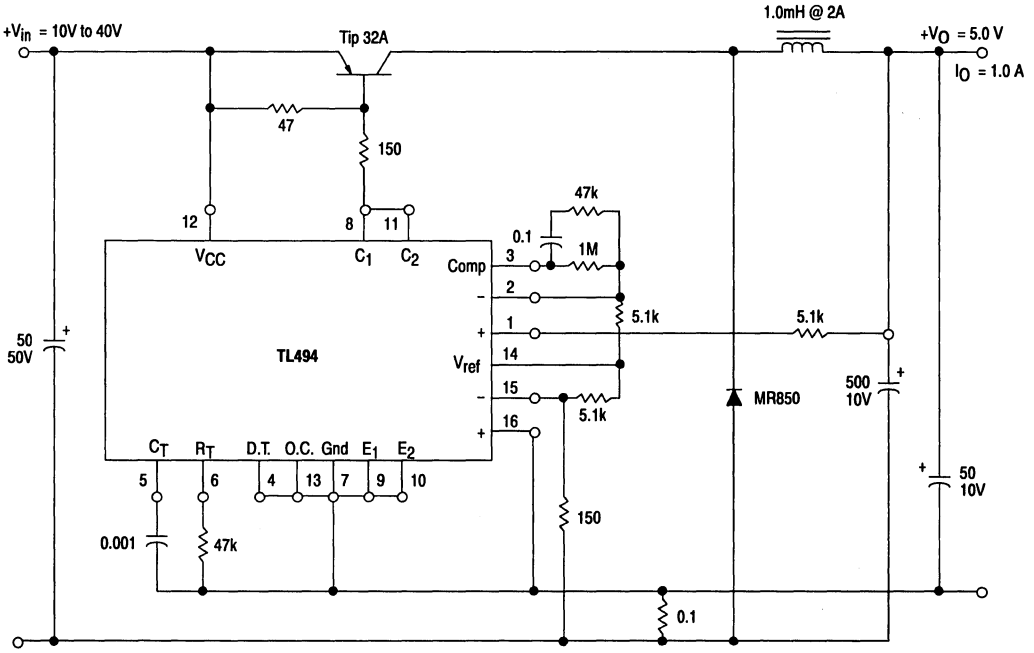


All capacitors in μF

L1 — 3.5 mH @ 0.3 A
T1 — Primary: 20T C.T. #28 AWG
Secondary: 12OT C.T. #36 AWG
Core: Ferroxcube 1408P-L00-3CB

TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 10 V to 40 V	14 mV 0.28%
Load Regulation	V_{in} = 28 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 28 V, I_O = 1.0 A	65 mV P-P P.A.R.D.
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 28 V, I_O = 1.0 A	71%

Figure 21. Pulse Width Modulated Step-Down Converter



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 8.0 V to 40 V	3.0 mV 0.01%
Load Regulation	V_{in} = 12.6 V, I_O = 0.2 mA to 200 mA	5.0 mV 0.02%
Output Ripple	V_{in} = 12.6 V, I_O = 200 mA	40 mV P-P P.A.R.D.
Short Circuit Current	V_{in} = 12.6 V, R_L = 0.1 Ω	250 mA
Efficiency	V_{in} = 12.6 V, I_O = 200 mA	72%

TL594

Precision Switchmode Pulse Width Modulation Control Circuit

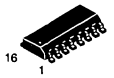
The TL594 is a fixed frequency, pulse width modulation control circuit designed primarily for SWITCHMODE power supply control.

This device features:

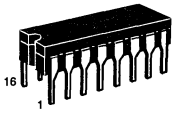
- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator with Master or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5.0 V Reference, 1.5% Accuracy
- Adjustable Dead-Time Control
- Uncommitted Output Transistors Rated to 500 mA Source or Sink
- Output Control for Push-Pull or Single-Ended Operation
- Undervoltage Lockout

PRECISION SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUIT

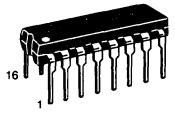
SILICON MONOLITHIC INTEGRATED CIRCUIT



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

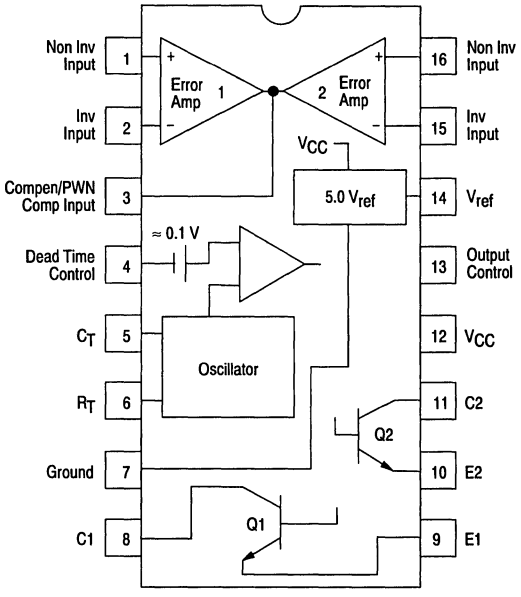


J SUFFIX
CERAMIC PACKAGE
CASE 620



N SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
TL594ID	0° to +70°C	SO-16
TL594CN		Plastic
TL594CD	–25° to +85°C	SO-16
TL594IN		Plastic
TL594MJ	–55° to +125°C	Ceramic

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	TL594C	TL594I	TL594M	Unit
Power Supply Voltage	V_{CC}	42			V
Collector Output Voltage	V_{C1}, V_{C2}	42			V
Collector Output Current (each transistor) (Note 1)	I_{C1}, I_{C2}	500			mA
Amplifier Input Voltage Range	V_{IR}	−0.3 to +42			V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000			mW
Operating Junction Temperature Plastic Package	T_J	125		—	°C
Ceramic Package		—		150	
Storage Temperature Range Plastic Package	T_{stg}	−55 to +125		—	°C
Ceramic Package		—		−65 to +150	
Operating Ambient Temperature Range	T_A	0 to +70	−25 to +85	−55 to +125	°C

NOTES: 1. Maximum thermal limits must be observed.

THERMAL CHARACTERISTICS

Characteristics	Symbol	N Suffix	J Suffix	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	80	100	°C/W
Derating Ambient Temperature	T_A	45	50	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	TL594			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	—	30	40	V
Collector Output Current (Each transistor)	I_{C1}, I_{C2}	—	—	200	mA
Amplified Input Voltage	V_{in}	0.3	—	V_{CC} − 2.0	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	30	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz
PWM Input Voltage (Pins 3, 4, & 13)	—	0.3	—	5.3	V

ELECTRICAL CHARACTERICISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating abmient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	TL594C,I			TL594M			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Voltage (I_O = 1.0 mA, T_A = 25°C) (I_O = 1.0 mA)	V_{ref}	 4.925 4.9	 5.0 —	 5.075 5.1	 4.925 4.9	 5.0 —	 5.075 5.1	V
Line Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	—	2.0	25	—	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	2.0	15	—	2.0	15	mV
Short Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	40	75	15	40	75	mA
OUTPUT SECTION								
Collector Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	—	2.0	100	—	2.0	100	µA
Emitter Off-State Current V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	—	—	–100	—	—	–100	µA
Collector-Emitter Saturation Voltage (Note 2) Common-Emitter (V_E = 0 V, I_C = 200 mA) Emitter-Follower (V_C = 15 V, I_E = –200 mA)	 $V_{SAT(C)}$ $V_{SAT(E)}$	 — —	 1.1 1.5	 1.3 2.5	 — —	 1.1 1.5	 1.5 2.5	V
Output Control Pin Current Low State ($V_{OC} \leq$ 0.4 V) High State (V_{OC} = V_{ref})	 I_{OCL} I_{OCH}	 — —	 0.1 2.0	 — 20	 — —	 0.1 2.0	 — 20	µA
Output Voltage Rise Time Common-Emitter (See Figure 13) Emitter-Follower (See Figure 14)	t_r	 — —	 100 100	 200 200	 — —	 100 100	 200 200	ns
Output Voltage Fall Time Common-Emitter (See Figure 13) Emitter-Follower (See Figure 14)	t_f	 — —	 40 40	 100 100	 — —	 40 40	 100 100	ns

NOTE: 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

Characteristics	Symbol	TL594 Min	TL594 Typ	TL594 Max	Unit
ERROR AMPLIFIER SECTION					
Input Offset Voltage ($V_{O\ (Pin\ 3)}$ = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current ($V_{O\ (Pin\ 3)}$ = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias Current ($V_{O\ (Pin\ 3)}$ = 2.5 V)	I_{IB}	—	–0.1	–1.0	μA
Input Common Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)	V_{ICR}	0 to V_{CC}–2.0			V
Inverting Input Voltage Range	$V_{IR(INV)}$	–0.3 to V_{CC}–2.0			V
Open-Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	—	dB
Unity-Gain Crossover Frequency (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	f_C	—	700	—	kHz
Phase Margin at Unity-Gain (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	ϕm	—	65	—	deg.
Common Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90	—	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	—	100	—	dB
Output Sink Current ($V_{O\ (Pin\ 3)}$ = 0.7 V)	I_{O-}	0.3	0.7	—	mA
Output Source Current ($V_{O\ (Pin\ 3)}$ = 3.5 V)	I_{O+}	–2.0	–4.0	—	mA
PWM COMPARATOR SECTION (Test Circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	—	3.6	4.5	V
Input Sink Current ($V_{Pin\ 3}$ = 0.7 V)	I_{I-}	0.3	0.7	—	mA
DEAD-TIME CONTROL SECTION (Test Circuit Figure 11)					
Input Bias Current (Pin 4) ($V_{Pin\ 4}$ = 0 V to 5.25 V)	$I_{IB\ (DT)}$	—	–2.0	–10	μA
Maximum Duty Cycle, Each Output, Push-Pull Mode ($V_{Pin\ 4}$ = 0 V, C_T = 0.01 μF, R_T = 12 kΩ) ($V_{Pin\ 4}$ = 0 V, C_T = 0.001 μF, R_T = 30 kΩ)	DC_{max}	 45 —	 48 45	 50 —	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	 — 0	 2.8 —	 3.3 —	V
OSCILLATOR SECTION					
Frequency (C_T = 0.001 μF, R_T = 30 kΩ) (C_T = 0.01 μF, R_T = 12 kΩ, T_A = 25°C) (C_T = 0.01 μF, R_T = 12 kΩ, T_A = T_{low} to T_{high})	f_{osc}	 — 9.2 9.0	 40 10 —	 — 10.8 12	kHz
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 30 kΩ)	σf_{osc}	—	1.5	—	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Δf_{osc} (ΔV)	—	0.2	1.0	%
Frequency Change with Temperature (ΔT_A = T_{low} to T_{high}, C_T = 0.01 μF, R_T = 12 kΩ)	Δf_{osc} (ΔT)	—	4.0	—	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn-On Threshold (V_{CC} Increasing, I_{ref} = 1.0 mA) T_A = 25°C T_A = T_{low} to T_{high}	V_{th}	 4.0 3.5	 5.2 —	 6.0 6.5	V
Hysteresis TL594C,I TL594M	V_H	 100 50	 150 150	 300 300	mV
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, All other inputs and outputs open) (V_{CC} = 15 V) (V_{CC} = 40 V)	I_{CC}	 — —	 8.0 8.0	 15 18	mA
Average Supply Current ($V_{Pin\ 4}$ = 2.0 V, C_T = 0.01 μF, R_T = 12 kΩ, V_{CC} = 15 V, See Figure 11)	—	—	11	—	mA

* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \bar{X})^2}{N-1}}$

Figure 1. Block Diagram

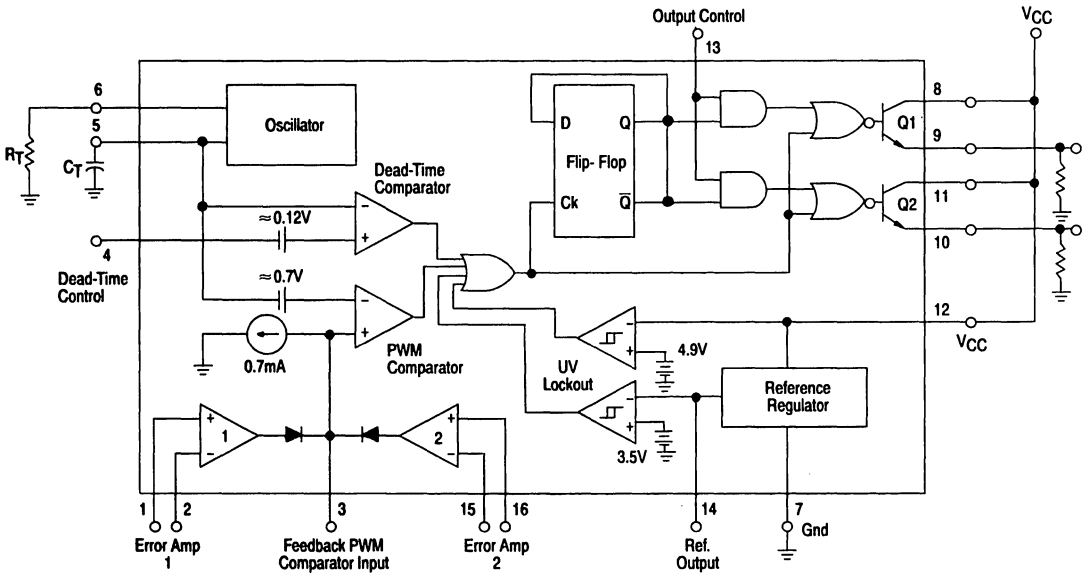
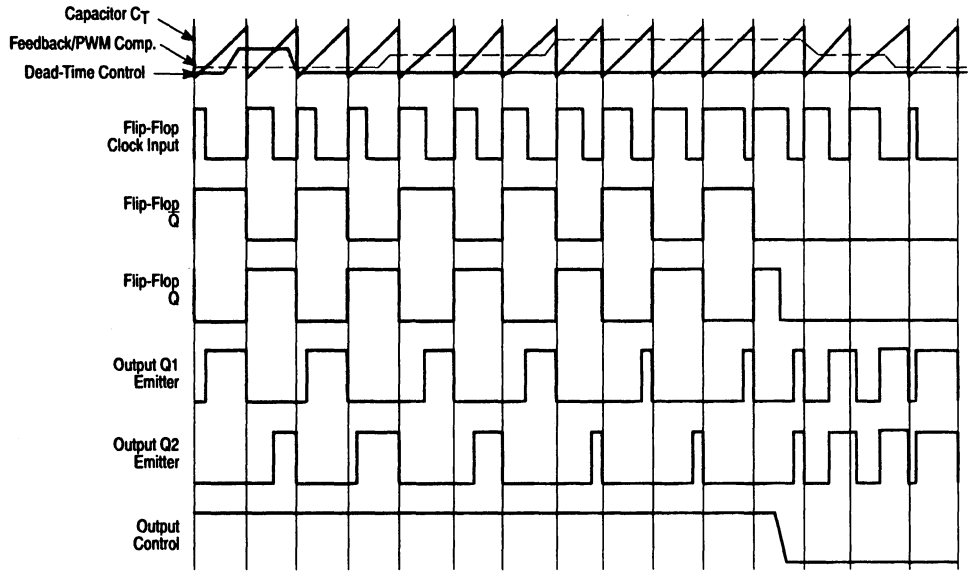


Figure 2. Timing Diagram



APPLICATIONS INFORMATION

Description

The TL594 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 V to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common-mode input range from –0.3 V to (V_{CC} – 2 V), and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the noninverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

Functional Table

Input/Output Controls	Output Function	$\frac{f_{out}}{f_{osc}}$ =
Grounded	Single-ended PWM @ Q1 and Q2	1.0
@ V_{ref}	Push-pull Operation	0.5

When capacitor C_T is discharged, a positive pulse is generated on the output of the dead-time comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on-time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The TL594 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±1.5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to 70°C.

Figure 3. Oscillator Frequency versus Timing Resistance

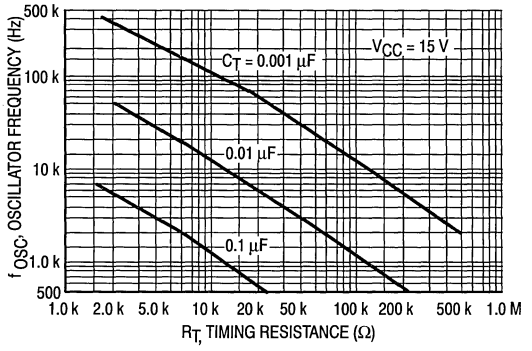


Figure 4. Open-Loop Voltage Gain and Phase versus Frequency

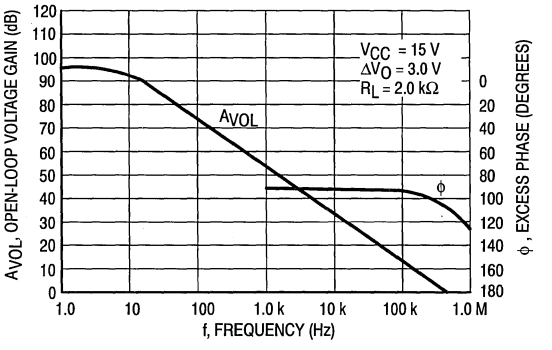


Figure 5. Percent Dead-Time versus Oscillator Frequency

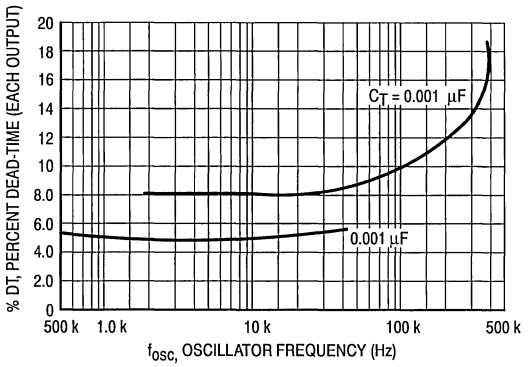


Figure 6. Percent Duty Cycle versus Dead-Time Control Voltage

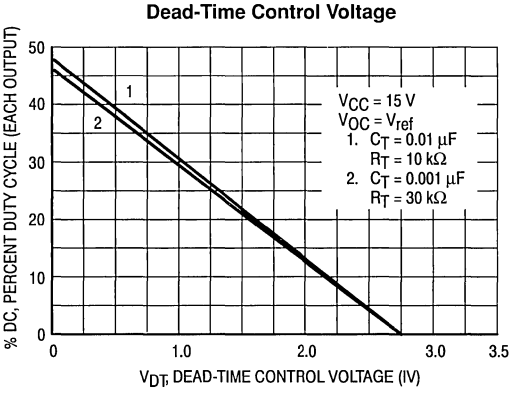


Figure 7. Emitter-Follower Configuration Output Saturation Voltage versus Emitter Current

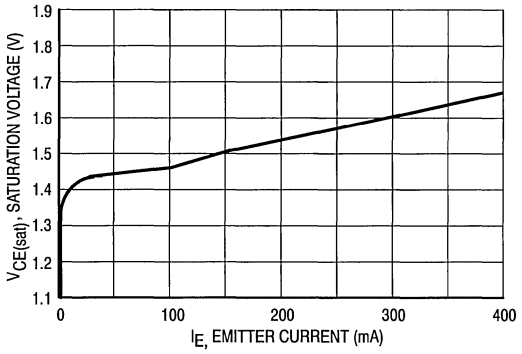


Figure 8. Common-Emitter Configuration Output Saturation Voltage versus Collector Current

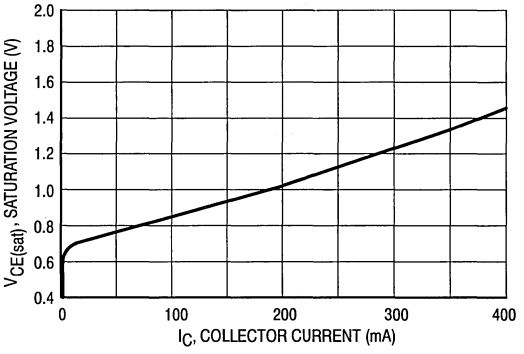


Figure 9. Standby Supply Current versus Supply Voltage

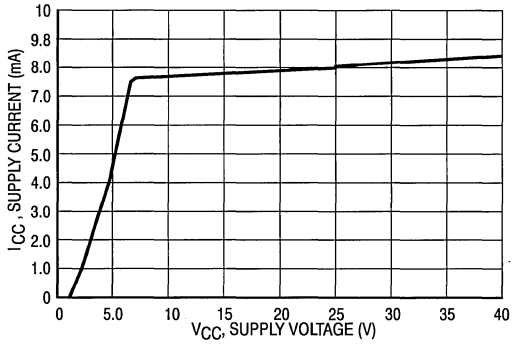


Figure 10. Undervoltage Lockout Thresholds versus Reference Load Current

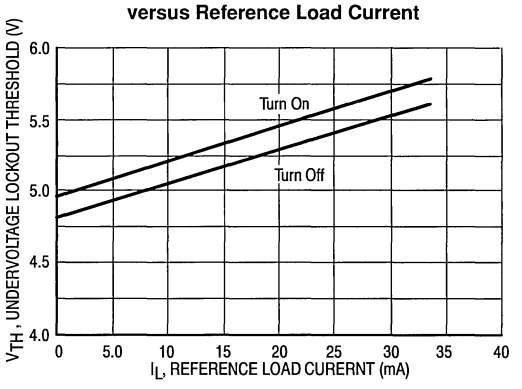


Figure 11. Error Amplifier Characteristics

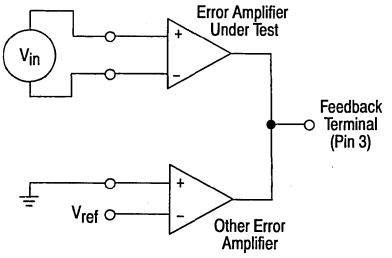


Figure 12. Dead-Time and Feedback Control Circuit

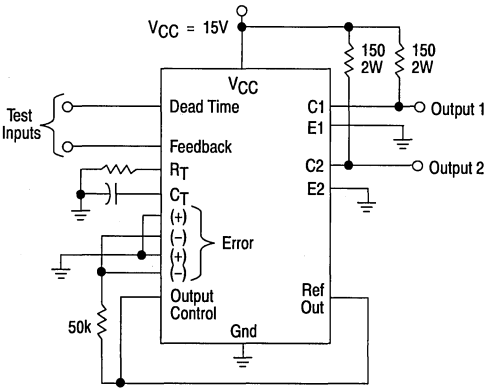


Figure 13. Common-Emitter Configuration Test Circuit and Waveform

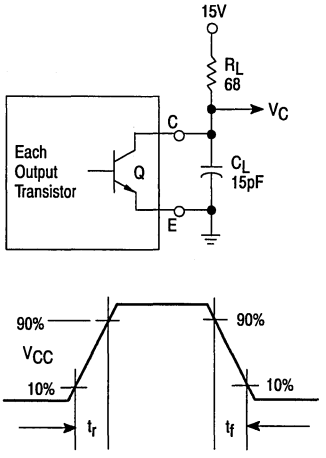


Figure 14. Emitter-Follower Configuration Test Circuit and Waveform

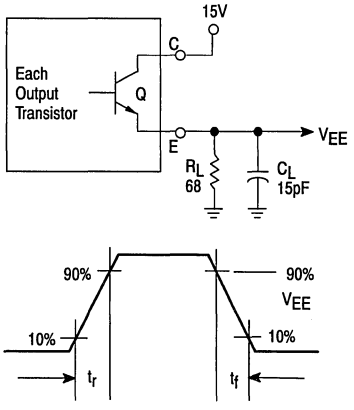
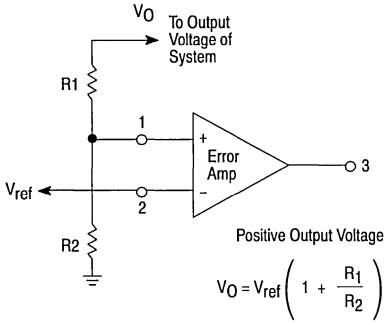


Figure 15. Error-Amplifier Sensing Techniques



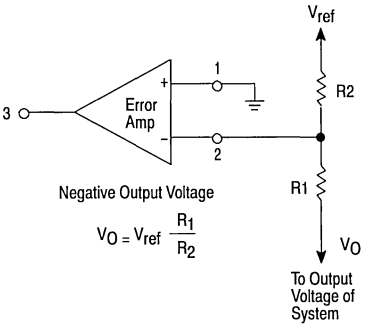


Figure 16. Dead-Time Control Circuit

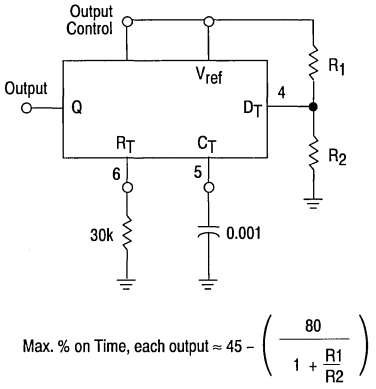


Figure 17. Soft-Start Circuit

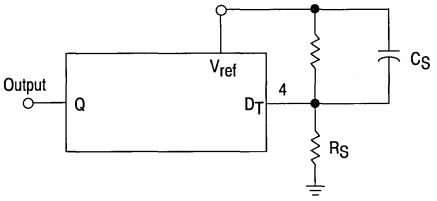
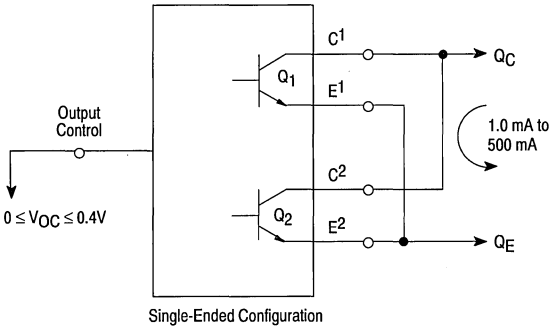


Figure 18. Output Connections for Single-Ended and Push-Pull Configurations



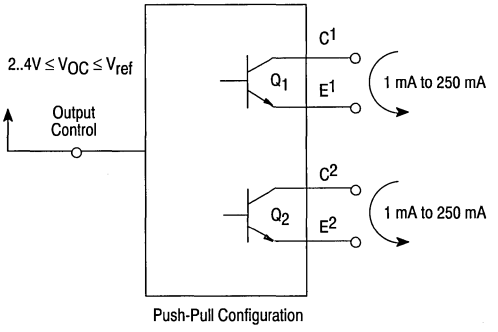


Figure 19. Slaving Two or More Control Circuits

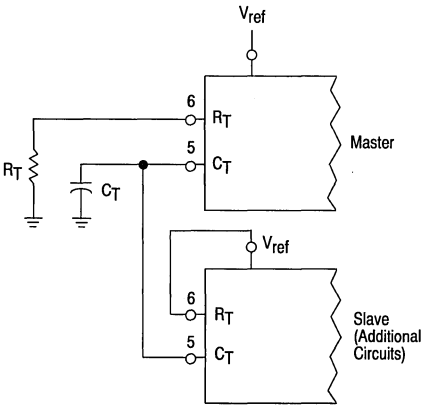


Figure 20. Operation with V_{in} > 40 V Using External Zener

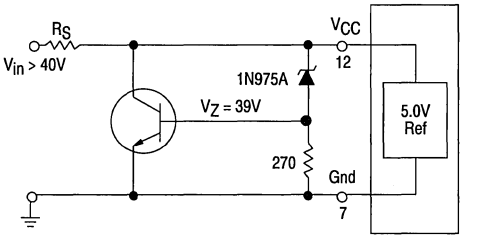
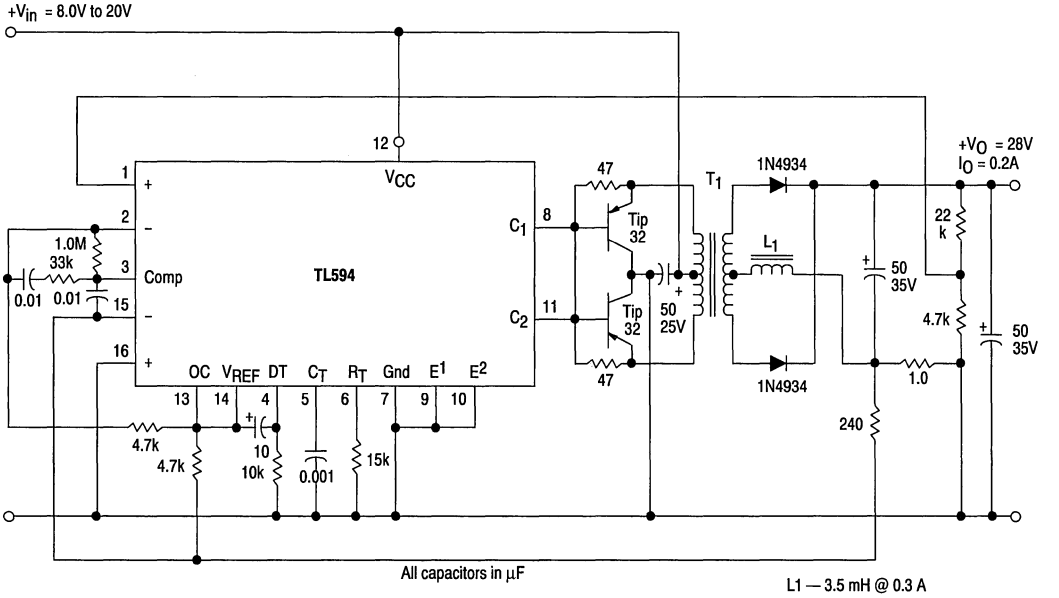


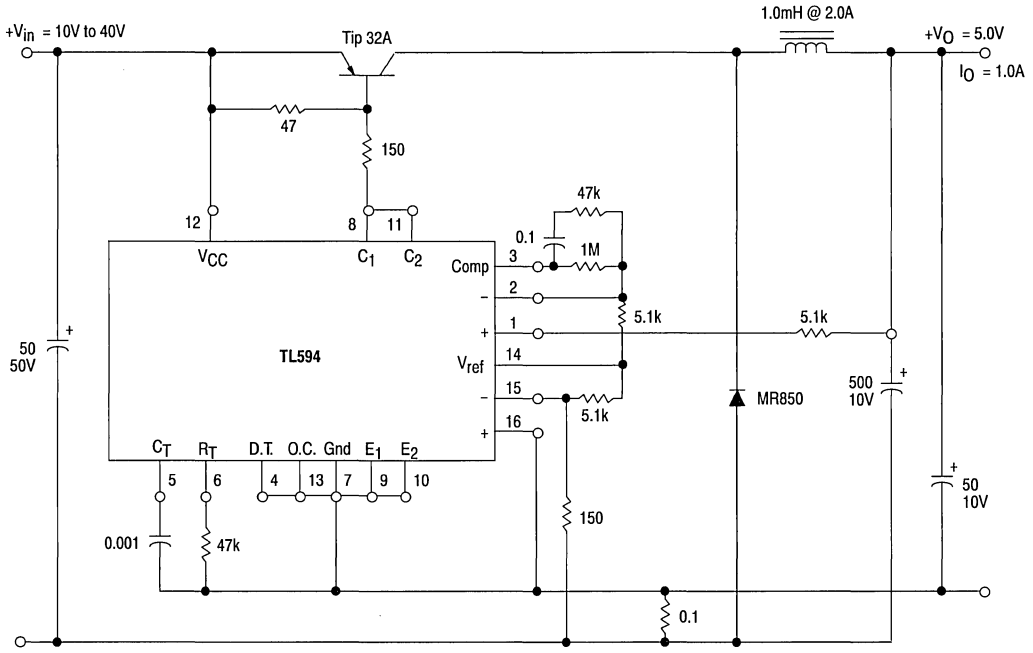
Figure 21. Pulse Width Modulated Push-Pull Converter



L1 — 3.5 mH @ 0.3 A
T1 — Primary: 20T C.T. #28 AWG
Secondary: 12OT C.T. #36 AWG
Core: Ferroxcube 1408P-L00-3CB

Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 40 V	14 mV 0.28%
Load Regulation	V_{in} = 28 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 28 V, I_O = 1.0 A	65 mV P-P PARD
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	1.6 amps
Efficiency	V_{in} = 28 V, I_O = 1.0 A	71%

Figure 22. Pulse Width Modulated Step-Down Converter



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V	3.0 mV 0.01%
Load Regulation	V_{in} = 12.6 V, I_O = 0.2 mA to 200 mA	5.0 mV 0.02%
Output Ripple	V_{in} = 12.6 V, I_O = 200 mA	40 mV P-P PARD
Short Circuit Current	V_{in} = 12.6 V, R_L = 0.1 Ω	250 mA
Efficiency	V_{in} = 12.6 V, I_O = 200 mA	72%

TL780 Series

3

Three-Terminal Positive Fixed Voltage Regulators

This family of precision fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 1.5 A. Innovative design concepts, coupled with advanced thermal layout techniques has resulted in improved accuracy and excellent load, line and thermal regulation characteristics. Internal current limiting, thermal shutdown and safe-area compensation are employed, making these devices extremely rugged and virtually immune to overload.

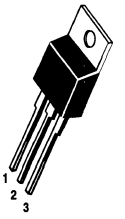
- ±1% Output Voltage Tolerance @ 25°C
- ±2% Output Voltage Tolerance Over Full Operating Temperature Range
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- Output Transistor Safe-Area Compensation
- No External Components Required
- Pinout Compatible with MC7800 Series

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SILICON MONOLITHIC INTEGRATED CIRCUIT

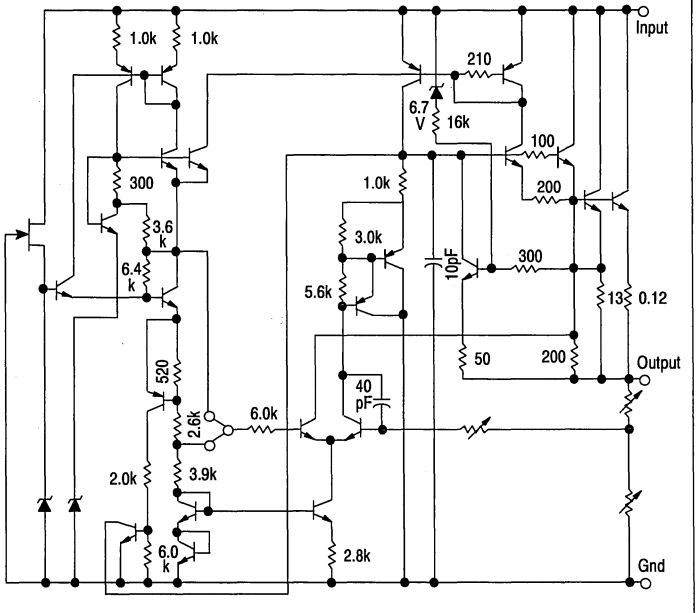
KC SUFFIX
PLASTIC PACKAGE
CASE 221A

PIN 1. Input
2. Ground
3. Output

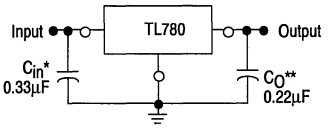


Heatsink surface connected to Pin 2.

Equivalent Schematic Diagram



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX= these two digits of the type number indicate voltage.

*= C_{in} is required if regulator is located an appreciable distance from power supply filter.

**= C_O is not needed for stability; however, it does improve transient response.

ORDERING INFORMATION

Nominal Output Voltage	Device
5.0	TL780-05CKC
12	TL780-12CKC
15	TL780-15CKC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	35	Vdc
Power Dissipation and Thermal Characteristics T_A = +25°C Derate above T_A = +25°C Thermal Resistance, Junction to Air T_A = +25°C Derate above T_C = +75°C (See Figure 1) Thermal Resistance, Junction to Case	 P_D $1/\theta_{JA}$ θ_{JA} P_D $1/\theta_{JC}$ θ_{JC}	 2.0 16 62.5 15 200 5.0	 W mW/°C °C/W W mW/°C °C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERICISTICS (V_{in} = 10 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C, unless otherwise noted [Note 1].)

Characteristics	Symbol	TL780-05C			Unit
		Min	Typ	Max	
Output Voltage 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W 7.0 V ≤ V_{in} ≤ 20 V T_J = +25°C 0°C ≤ T_J ≤ +125°C	V_O	 4.95 4.90	 5.0 —	 5.05 5.10	V
Line Regulation (T_J = +25°C) 7.0 V ≤ V_{in} ≤ 25 V 8.0 V ≤ V_{in} ≤ 12 V	Reg_{line}	 — —	 0.5 0.5	 5.0 5.0	mV
Load Regulation (T_J = +25°C) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 4.0 1.5	 25 15	mV
Ripple Rejection 8.0 V ≤ V_{in} ≤ 18 V, f = 120 Hz	RR	 70	 80	 —	dB
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	Ω
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	 —	 0.06	 —	mV°C
Output Noise Voltage (T_J = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	 —	 75	 —	μV
Dropout Voltage (T_J = +25°C) I_O = 1.0 mA	V_{in}–V_O	 —	 2.0	 —	V
Bias Current (T_J = +25°C)	I_B	—	3.5	8.0	mA
Bias Current Change 7.0 V ≤ V_{in} ≤ 25 V, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} ≤ 10 V	ΔI_B	 — —	 0.7 0.03	 1.3 0.5	mA
Short Circuit Output Current (T_J = +25°C) V_{in} = 35 V	I_{SC}	 —	 200	 —	mA
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

NOTE: 1. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERICISTICS (V_{in} = 19 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C, unless otherwise noted [Note 1].)

Characteristics	Symbol	TL780-12C			Unit
		Min	Typ	Max	
Output Voltage 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W, 14.5 ≤ V_{in} ≤ 27 V T_J = +25°C 0°C ≤ T_J ≤ +125°C	V_O	 11.88 11.76	 12 —	 12.12 12.24	V
Line Regulation (T_J = +25°C) 14.5 V ≤ V_{in} ≤ 30 16 V ≤ V_{in} ≤ 22	Reg_{line}	 — —	 1.2 1.2	 12 12	mV

ELECTRICAL CHARACTERICISTICS (V_{in} = 19 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C, unless otherwise noted [Note 1].)

Characteristics	Symbol	TL780-12C			Unit
		Min	Typ	Max	
Load Regulation (T_J = +25°C) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 6.5 2.5	 60 36	mV
Ripple Rejection 15 V ≤ V_{in} ≤ 25 V, f = 120 Hz	RR	 65	 77	 —	dB
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	Ω
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	 —	 0.15	 —	mV°C
Output Noise Voltage (T_J = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	 —	 180	 —	μV
Dropout Voltage (T_J = +25°C) I_O = 1.0 mA	V_{in}–V_O	 —	 2.0	 —	V
Bias Current (T_J = +25°C)	I_B	—	3.5	8.0	mA
Bias Current Change 14.5 V ≤ V_{in} ≤ 30 V, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} ≤ 19 V	ΔI_B	 — —	 0.4 0.03	 1.3 0.5	mA
Short Circuit Output Current (T_J = +25°C) V_{in} = 35 V	I_{SC}	 —	 200	 —	mA
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

ELECTRICAL CHARACTERICISTICS (V_{in} = 23 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C, unless otherwise noted [Note 1].)

Characteristics	Symbol	TL780-15C			Unit
		Min	Typ	Max	
Output Voltage 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W, 17.5 V ≤ V_{in} ≤ 30 V T_J = +25°C 0°C ≤ T_J ≤ +125°C	V_O	 14.85 14.70	 15 —	 15.15 15.30	V
Line Regulation (T_J = +25°C) 17.5 V ≤ V_{in} ≤ 30 V 20 V ≤ V_{in} ≤ 26 V	Reg_{line}	 — —	 1.5 1.5	 15 15	mV
Load Regulation (T_J = +25°C) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 — —	 7.0 2.5	 75 45	mV
Ripple Rejection 18.5 V ≤ V_{in} ≤ 28.5 V, f = 120 Hz	RR	 60	 75	 —	dB
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	Ω
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	 —	 0.18	 —	mV°C
Output Noise Voltage (T_J = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	 —	 225	 —	μV
Dropout Voltage (T_J = +25°C) I_O = 1.0 A	V_{in}–V_O	 —	 2.0	 —	V
Bias Current (T_J = +25°C)	I_B	—	3.6	8.0	mA
Bias Current Change 17.5 V ≤ V_{in} ≤ 30 V, I_O = 500 mA 5.0 mA ≤ I_O ≤ 1.0 A, V_{in} ≤ 23 V	ΔI_B	 — —	 0.4 0.02	 1.3 0.5	mA
Short Circuit Output Current (T_J = +25°C) V_{in} = 35 V	I_{SC}	 —	 200	 —	mA
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

NOTE: 1. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

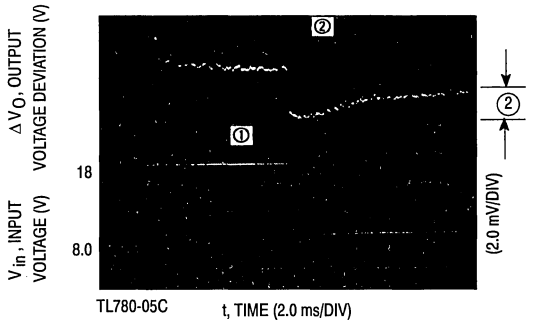
VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical TL780-05C to a 10 W input pulse. The variation of the output voltage due to line regulation is labeled À and the thermal regulation component is labeled Á. Figure 2 shows the load and thermal regulation response of a typical TL780-05C to a 15 W load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

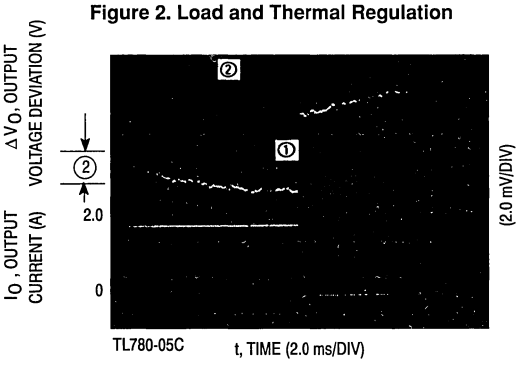
Figure 1. Line and Thermal Regulation



V_{out} = 5.0 V
V_{in} = 8.0 V → 18 V → 8.0 V
I_{out} = 1.0 A

① = Reg_{line} = 2.4 mV
② = Reg_{therm} = 0.0030% V_O/W

Figure 2. Load and Thermal Regulation



V_{out} = 5.0 V
V_{in} = 15 V
I_{out} = 0 A → 1.5 A → 0 A

① = Reg_{line} = 4.4 mV
② = Reg_{therm} = 0.0020% V_O/W

Figure 3. Temperature Stability

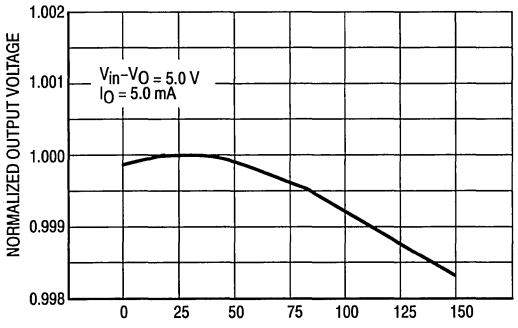


Figure 4. Output Impedance

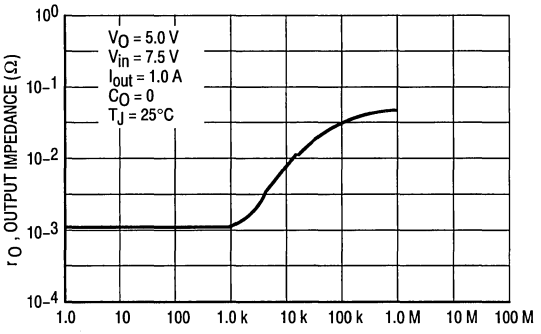


Figure 5. Ripple Rejection versus Frequency

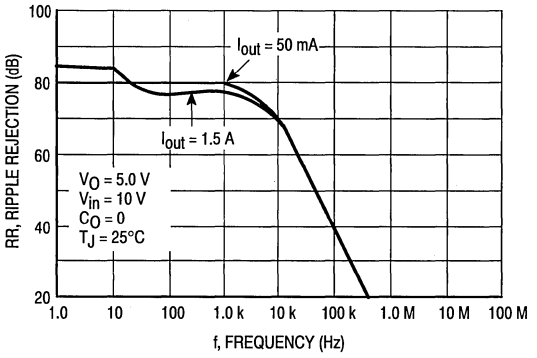


Figure 6. Ripple Rejection versus Output Current

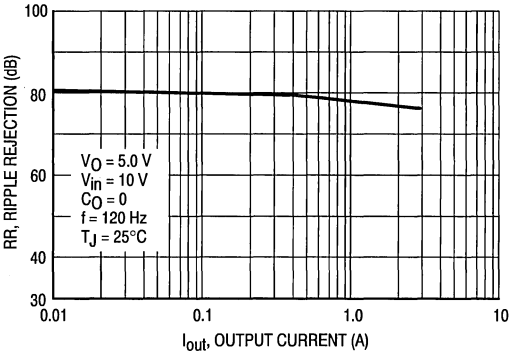


Figure 7. Bias Current versus Input Voltage

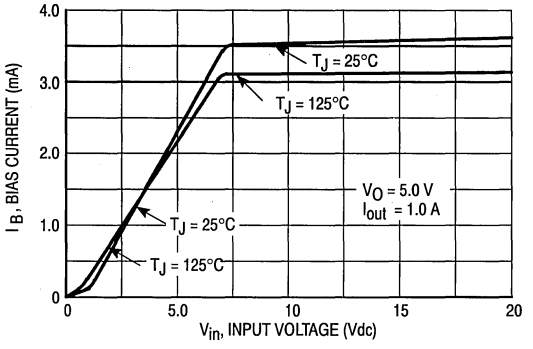


Figure 8. Bias Current versus Output Current

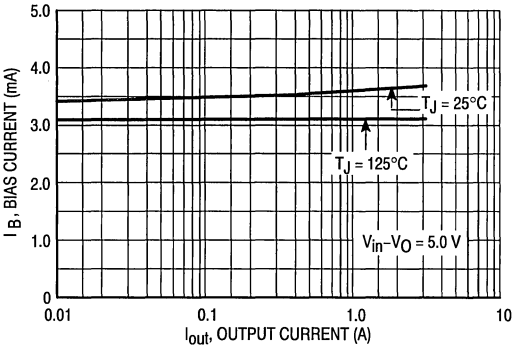


Figure 9. Dropout Voltage

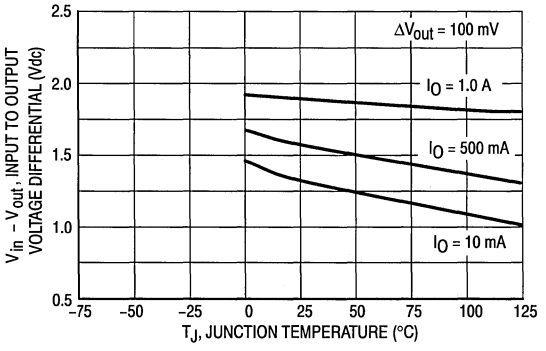


Figure 10. Peak Output Current

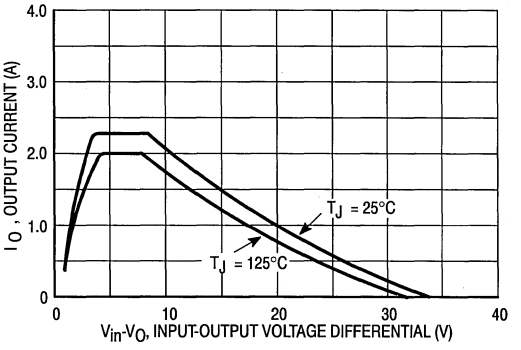


Figure 11. Line Transient Response

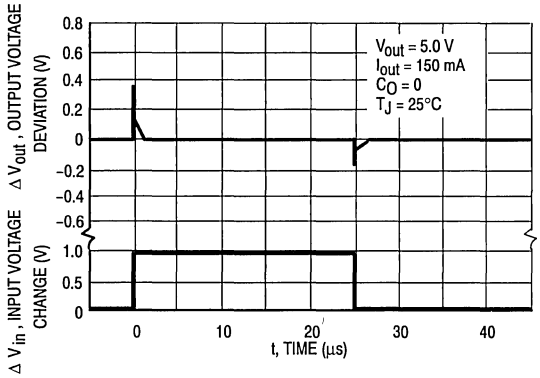


Figure 12. Load Transient Response

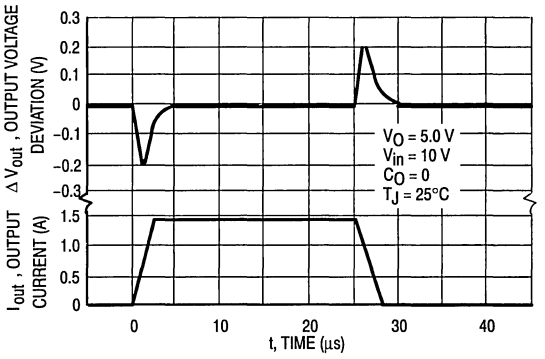
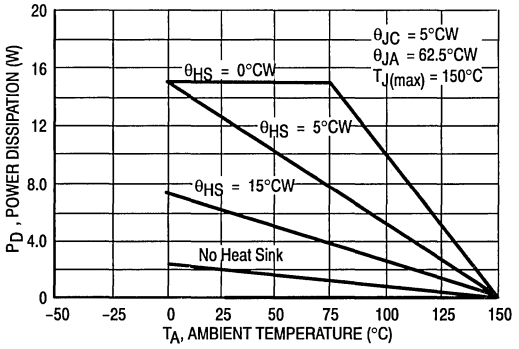


Figure 13. Worst Case Power Dissipation versus Ambient Temperature



UC3842A, 43A
UC2842A, 43A

HIGH PERFORMANCE CURRENT MODE CONTROLLER

3

Advance Information

High Performance Current Mode Controller

The UC3842A, UC3843A series are high performance fixed frequency current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

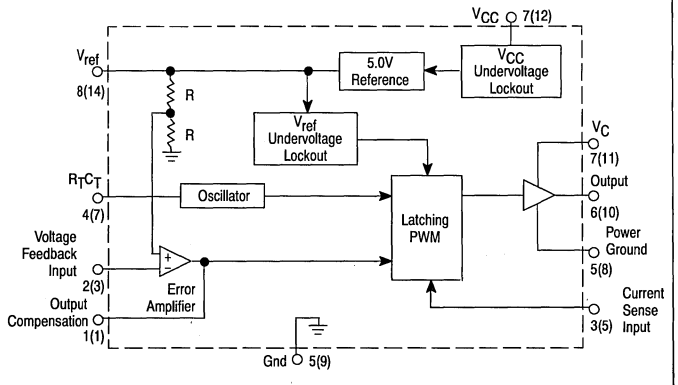
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

These devices are available in 8-pin dual-in-line ceramic and plastic packages as well as the 14-pin plastic surface mount (SO-14). The SO-14 package has separate power and ground pins for the totem pole output stage.

The UCX842A has UYLO thresholds of 16 V (on) and 10 V (off), ideally suited for off-line converters. The UCX843A is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

- Trimmed Oscillator Discharge Current for Precise Duty Cycle Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

Simplified Block Diagram

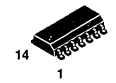


Pin numbers adjacent to terminals are for the 8-pin dual-in-line package.
Pin numbers in parenthesis are for the D suffix SO-14 package.

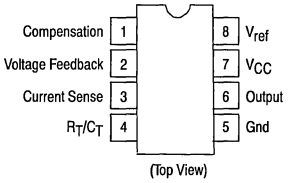
N SUFFIX
PLASTIC PACKAGE
CASE 626

J SUFFIX
CERAMIC PACKAGE
CASE 693

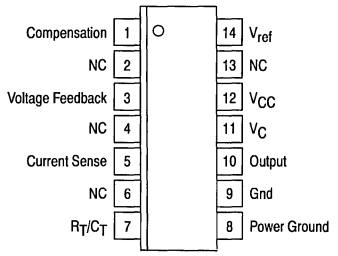
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



PIN CONNECTIONS



(Top View)



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
UC3842AD	0° to + 70°C	SO–14
UC3843AD		SO–14
UC3842AN		Plastic
UC2843AN		Plastic
UC2842AD	–25° to + 85°C	SO–14
UC2843AD		SO–14
UC2842AJ		Ceramic
UC2843AJ		Ceramic
UC2842AN		Plastic
UC2843AN		Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	− 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction-to-Air N Suffix, Plastic and J Suffix, Ceramic Packages Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction-to-Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+ 150	°C
Operating Ambient Temperature UC3842A, UC3843A UC2842A, UC2843A	T_A	 0 to + 70 − 25 to + 85	°C
Storage Temperature Range	T_{stg}	− 65 to + 150	°C

ELECTRICAL CHARACTERICISTICS (V_{CC} = 15 V, [Note 2], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284XA			UC384XA			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	—	2.0	20	—	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	—	3.0	25	—	3.0	25	mV
Temperature Stability	T_S	—	0.2	—	—	0.2	—	mV/°C
Total Output Variation over Line, Load, Temperature	V_{ref}	4.9	—	5.1	4.82	—	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	—	50	—	—	50	—	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	—	5.0	—	—	5.0	—	mV
Output Short Circuit Current	I_{SC}	− 30	− 85	− 180	− 30	− 85	− 180	mA
OSCILLATOR SECTION								
Frequency T_J = 25°C T_A = T_{low} to T_{high}	f_{osc}	 47 46	 52 —	 57 60	 47 46	 52 —	 57 60	kHz
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{osc}/\Delta V$	—	0.2	1.0	—	0.2	1.0	%
Frequency Change with Temperature T_A = T_{low} to T_{high}	$\Delta f_{osc}/\Delta T$	—	5.0	—	—	5.0	—	%
Oscillator Voltage Swing (Peak-to-Peak)	V_{osc}	—	1.6	—	—	1.6	—	V
Discharge Current (V_{osc} = 2.0 V) T_J = 25°C T_A = T_{low} to T_{high}	I_{dischg}	 7.5 7.2	 8.4 —	 9.3 9.5	 7.5 7.2	 8.4 —	 9.3 9.5	mA

NOTES: 1. Maximum Package power dissipation limits must be observed.
2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible
T_{low} = 0°C for UC3842A, UC3843A; −25°C for UC2842A, UC2843A
T_{high} = +70°C for UC3842A, UC3843A; +85°C for UC2842A, UC2843A

ELECTRICAL CHARACTERICISTICS (V_{CC} = 15 V, [Note 2], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284XA Min	UC284XA Typ	UC284XA Max	UC384XA Min	UC384XA Typ	UC384XA Max	Unit
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 2.7 V)	I_{IB}	—	–0.1	–1.0	—	–0.1	–2.0	µA
Open-Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	—	65	90	—	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	—	0.7	1.0	—	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	—	60	70	—	dB
Output Current								mA
Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	—	2.0	12	—	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	–0.5	–1.0	—	–0.5	–1.0	—	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	—	5.0	6.2	—	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}	—	0.8	1.1	—	0.8	1.1	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V	2.85	3.0	3.15	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	0.9	1.0	1.1	V
Power Supply Rejection Ratio	PSRR							dB
V_{CC} = 12 to 25 V (Note 4)		—	70	—	—	70	—	
Input Bias Current	I_{IB}	—	–2.0	–10	—	–2.0	–10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(in/out)}$	—	150	300	—	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	—	0.1	0.4	—	0.1	0.4	
(I_{Sink} = 200 mA)		—	1.6	2.2	—	1.6	2.2	
High State (I_{Sink} = 20 mA)	V_{OH}	13	13.5	—	13	13.5	—	
(I_{Sink} = 200 mA)		12	13.4	—	12	13.4	—	
Output Voltage with UVLO Activated	$V_{OL(UVLO)}$							V
V_{CC} = 6.0 V, I_{Sink} = 1.0 mA		—	0.1	1.1	—	0.1	1.1	
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	—	50	150	—	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_r	—	50	150	—	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Start-Up Threshold	V_{th}							V
UCX842A		15	16	17	14.5	16	17.5	
UCX843A		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn-On	$V_{CC(min)}$							V
UCX842A		9.0	10	11	8.5	10	11.5	
UCX843A		7.0	7.6	8.2	7.0	7.6	8.2	
PWM SECTION								
Duty Cycle								%
Maximum	DC_{max}	94	96	—	94	96	—	
Minimum	DC_{min}	—	—	0	—	—	0	
TOTAL DEVICE								
Power Supply Current (Note 2)	I_{CC}							mA
Start-Up:								
(V_{CC} = 6.5 V for UCX843A,		—	0.5	1.0	—	0.5	1.0	
14 V for UCX842A) Operating		—	12	17	—	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	—	30	36	—	V

NOTES: 4. This parameter is measured at the latch trip point with V_{FB} = 0 V.

5. Comparator gain is defined as: $A_V \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$

Figure 1. Timing Resistor versus Oscillator Frequency

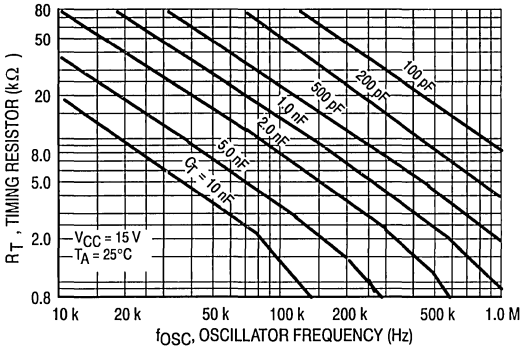


Figure 2. Output Dead Time versus Oscillator Frequency

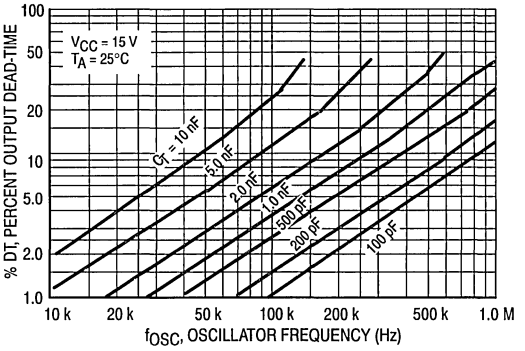


Figure 3. Oscillator Discharge Current versus Temperature

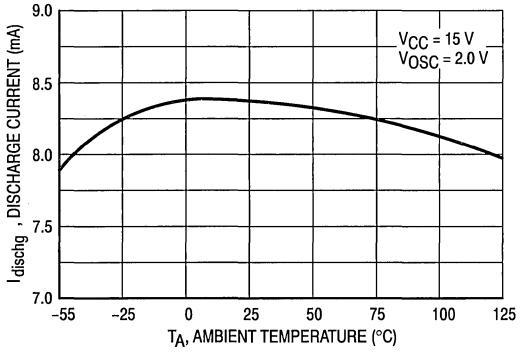


Figure 4. Maximum Output Duty Cycle versus Timing Resistor

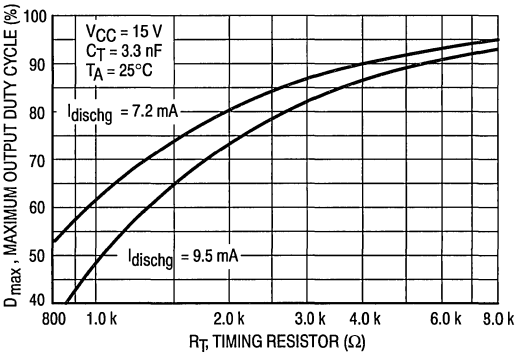


Figure 5. Error Amp Small Signal Transient Response

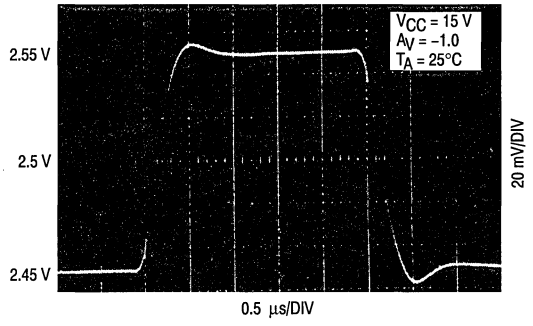


Figure 6. Error Amp Large Signal Transient Response

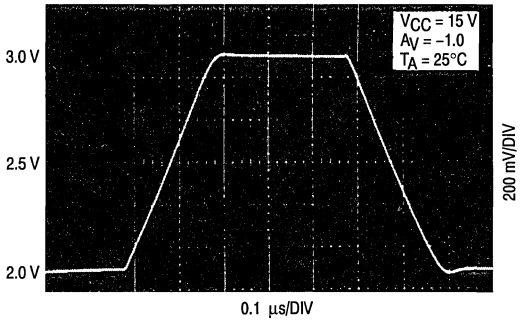


Figure 7. Error Amp Open-Loop Gain and Phase versus Frequency

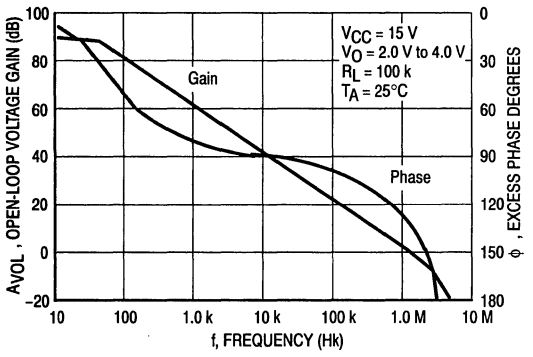


Figure 8. Current Sense Input Threshold versus Error Amp Output Voltage

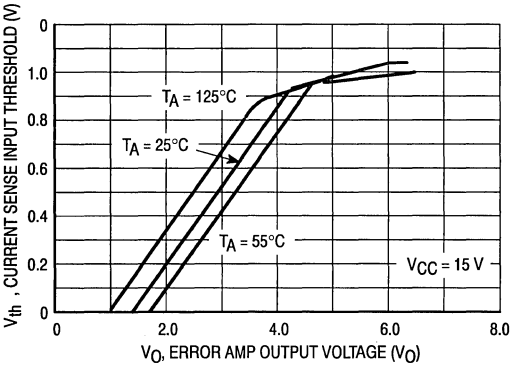


Figure 9. Reference Voltage Change versus Source Current

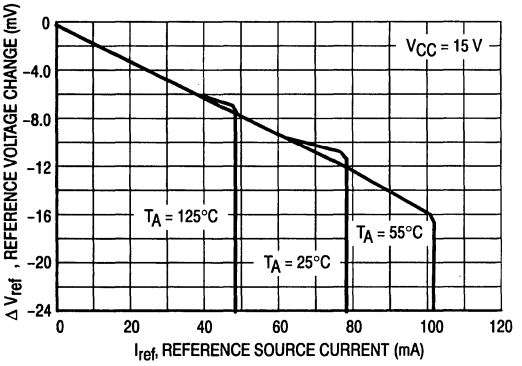


Figure 10. Reference Short Circuit Current versus Temperature

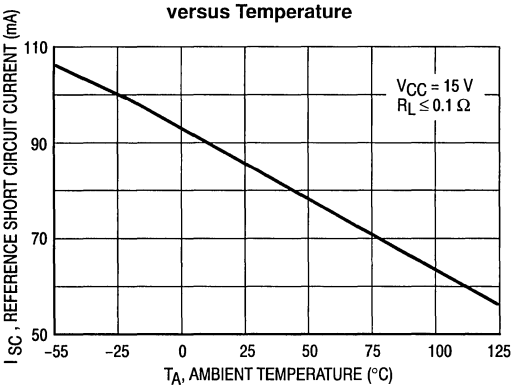


Figure 11. Reference Load Regulation

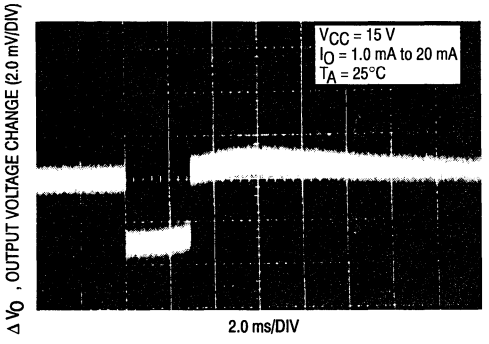


Figure 12. Reference Line Regulation

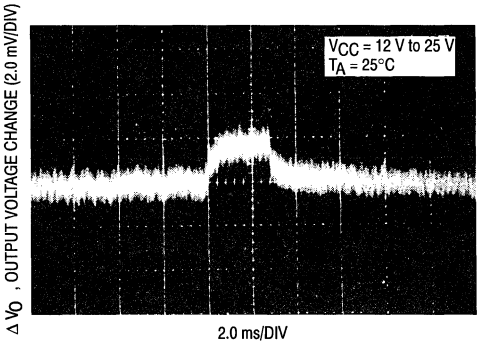


Figure 13. Output Saturation Voltage versus Load Current

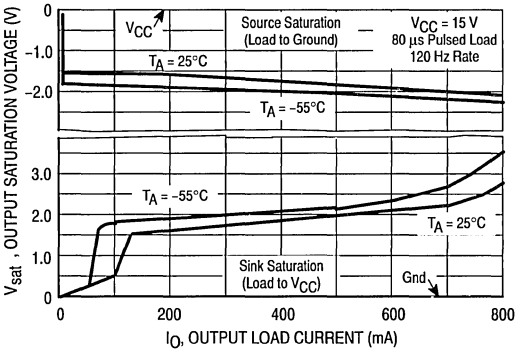


Figure 14. Output Waveform

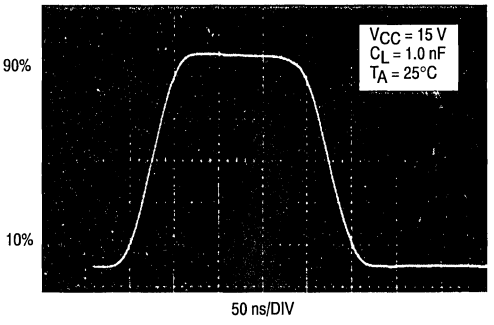


Figure 15. Output Cross Conduction

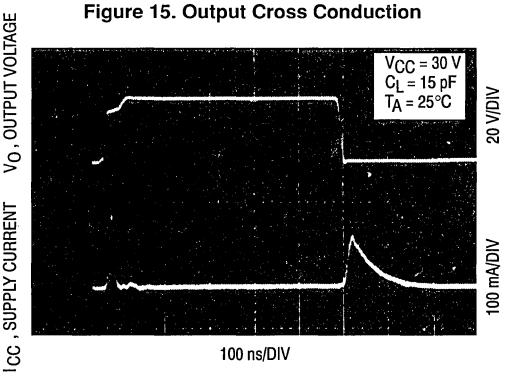


Figure 16. Supply Current versus Supply Voltatage

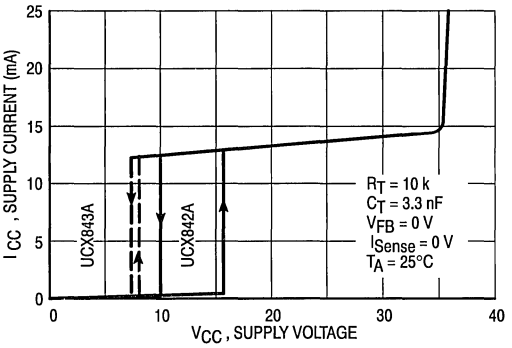
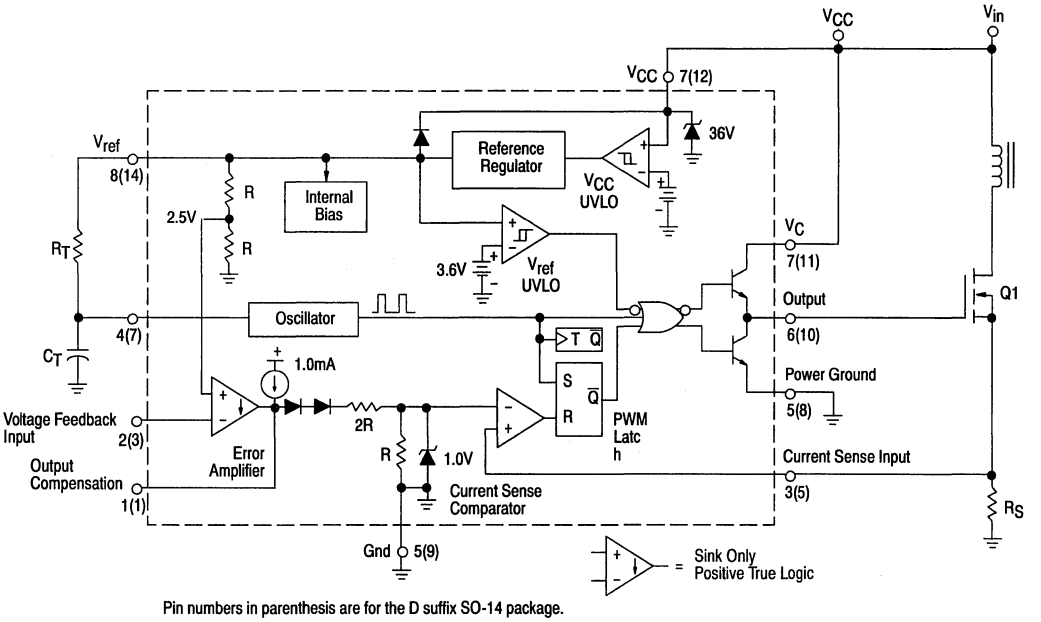
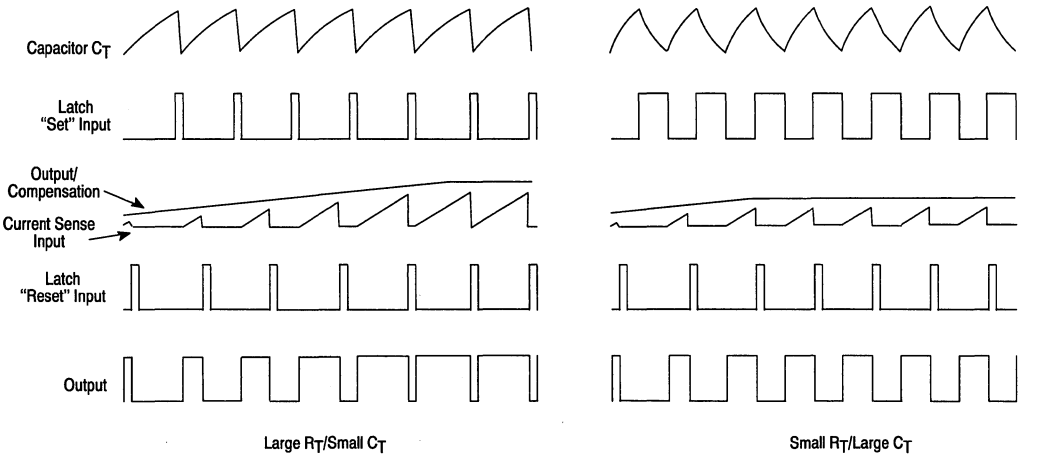


Figure 17. Representative Block Diagram



Pin numbers in parenthesis are for the D suffix SO-14 package.

Figure 18. Timing Diagram



OPERATING DESCRIPTION

The UC3842A, UC3843A series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 17.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates and internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated, and the discharge current is trimmed and guaranteed to within ± 10% at T_J = 25°C. These internal circuit refinements minimize variations of oscillator frequency and maximum output duty cycle. The results are shown in Figures 3 and 4.

In many noise sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 19. For reliable locking, the free-running oscillator frequency should be set about 10% less than the clock frequency. A method for multi unit synchronization is shown in Figure 20. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 7). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is –2.0 µA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provide for external loop compensation (Figure 30). The output voltage is offset by two diode drops (≈ 1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figures 22, 23). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3842A, UC3843A operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin1). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 21. The two external diodes are used to compensate the internal diodes yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to figure 25.

PIN FUNCTION DESCRIPTION

Pin No.		Function	Description
8-Pin	14-Pin		
1	1	Compensation	This pin is Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 500 kHz is possible.
5	—	Gnd	This pin is the combined control circuitry and power ground (8-pin package only).
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
—	8	Power Ground	This pin is a separate power ground return (14-pin package only) that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
—	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin (14-pin package only). With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
—	9	Gnd	This pin is the control circuitry ground return (14-pin package only) and is connected back to the power source ground.
—	2,4,6,13	NC	No connection (14-pin package only). These pins are not internally connected.

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX842A, and 8.4 V/7.6 V for the UCX843A. The V_{ref} comparator upper and lower thresholds are 3.6V/3.4 V. The large hysteresis and low start-up current of the UCX842A makes it ideally suited in off-line converter applications where efficient bootstrap start-up techniques are required (Figure 32). The UCX843A is intended for lower voltage DC to DC converter applications. A 36 V zener is connected as a shunt regulator form V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system start-up. The minimum operating voltage for the UCX842A is 11 V and 8.2 V for the UCX843A.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull-down resistor.

The SO-14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater that 20 V. Figure 24 shows proper power and control ground connections in a current sensing power MOSFET application.

Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the UC284XA, and ± 2.0% on the UC384XA. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

DESIGN CONSIDERATIONS

Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High Frequency circuit layout techniques are imperative to prevent pulsewidth jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low-current signal and high-current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than 50% with continuous inductor current. This instability is independent of the regulators closed-loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 33A shows the phenomenon graphically. At t_0, switch conduction begins, causing the inductor current to rise at a slope of m_1. This slope is a function of the input voltage divided by the inductance. At t_1, the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of m_2 until the next oscillator cycle. The unstable condition can be shown if a pertubation is added to the control voltage, resulting in a small ΔI (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn-on (t_2) is increased by ΔI + ΔI m2/m1. The minimum current at switch turn-on (t_3) decreases to (ΔI + ΔI m_2/m_1) (m_2/m_1). This pertubation is multiplied by $m_2.m_1$ on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn-on. Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If m_2/m_1 is greater than 1, the converter will be unstable. Figure 19B shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage, the ΔI pertubation will decrease to zero on succeeding cycles. This compensation ramp (m_3) must have a slope equal to or slightly greater than $m_2/2$ for stability. With $m_2/2$ slope compensation, the average inductor current follows the control voltage yielding true current mode operation. The compensating ramp can be derived from the oscillator and added to either the Voltage Feedback or Current Sense inputs (Figure 31).

Figure 33. Continuous Current Waveforms

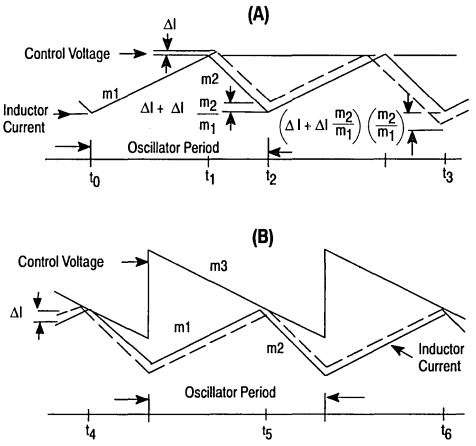
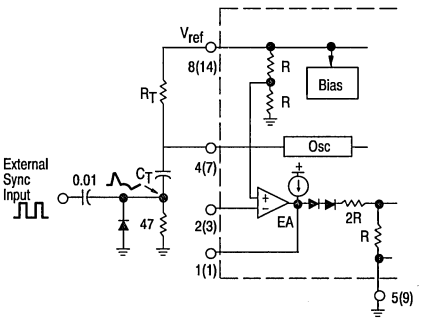
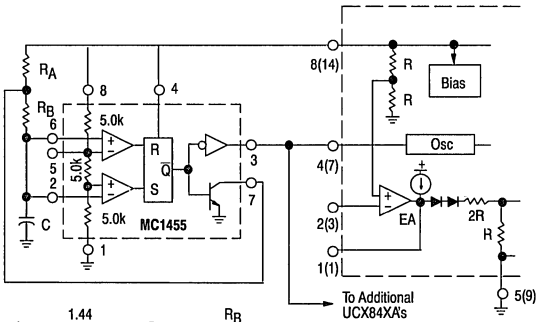


Figure 19. External Clock Synchronization



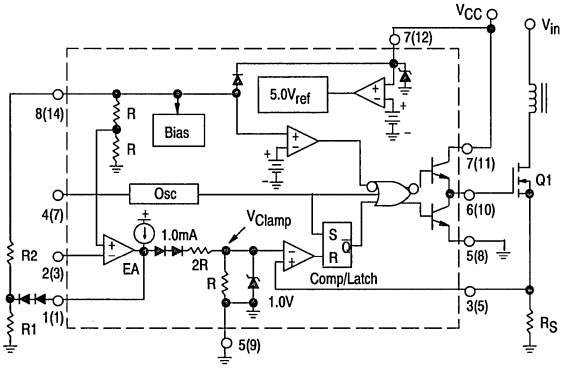
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

Figure 20. External Duty Cycle Clamp and Multi Unit Synchronization



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_B}{R_A + 2R_B}$$

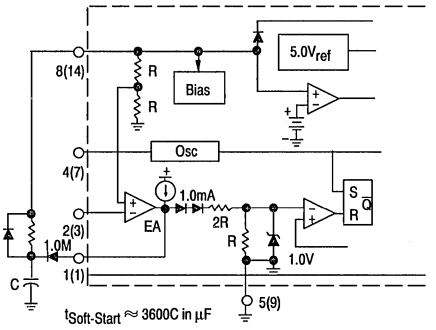
Figure 21. Adjustable Reduction of Clamp Level



$$V_{Clamp} \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} + 0.33 \times 10^{3}\left(\frac{R_1 R_2}{R_1 + R_2}\right) \qquad I_{pk(max)} \frac{V_{Clamp}}{R_S}$$

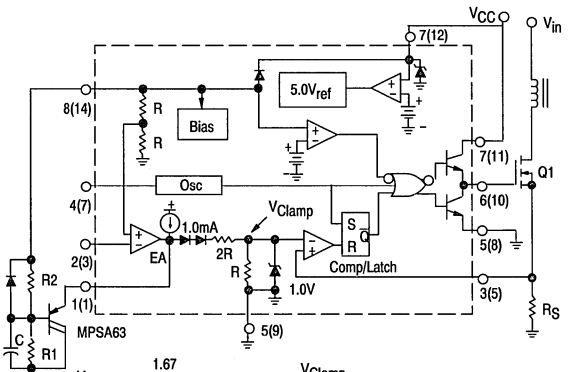
Where: $0 \le V_{Clamp} \le 1.0$ V

Figure 22. Soft-Start Circuit



$t_{Soft\text{-}Start} \approx 3600C$ in μF

Figure 23. Adjustable Buffered Reduction of Clamp Level with Soft-Start

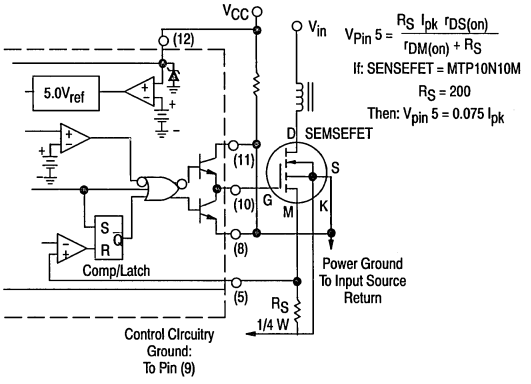


$$V_{Clamp} \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} \qquad I_{pk(max)} \frac{V_{Clamp}}{R_S}$$

Where: $0 \le V_{Clamp} \le 1.0$ V

$$t_{Softstart} = -\ln\left[1 - \frac{V_C}{3V_{Clamp}}\right] C \frac{R_1 R_2}{R_1 + R_2}$$

Figure 24. Current Sensing Power MOSFET



$$V_{Pin\,5} = \frac{R_S\, I_{pk}\, r_{DS(on)}}{r_{DM(on)} + R_S}$$

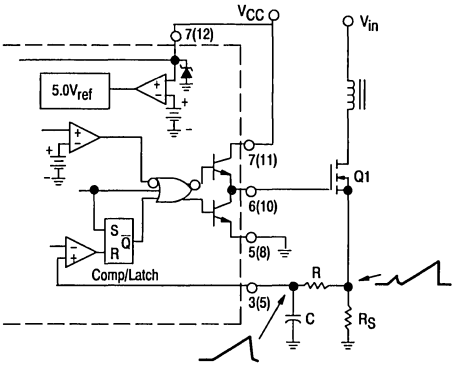
If: SENSEFET = MTP10N10M

R_S = 200

Then: $V_{pin}\,5 = 0.075\, I_{pk}$

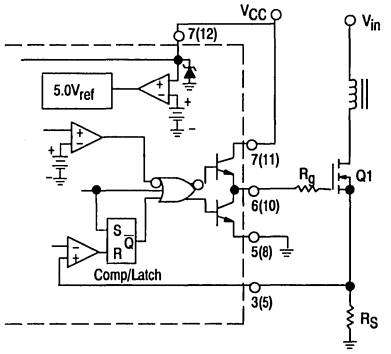
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 22 and 24.

Figure 25. Current Waveform Spike Suppression



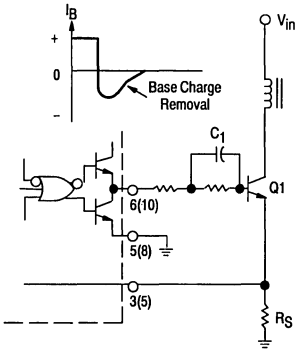
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 26. MOSFET Parasitic Oscillations



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

Figure 27. Bipolar Transistor Drive



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1.

Figure 28. Isolated MOSFET Drive

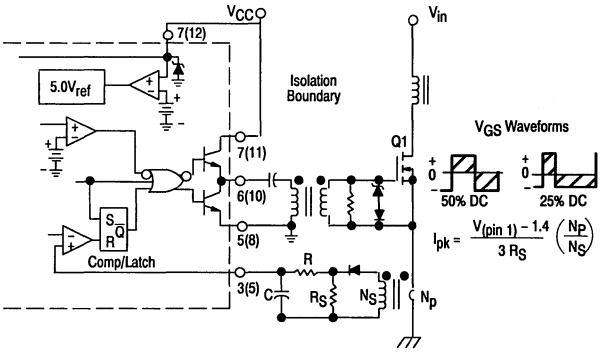
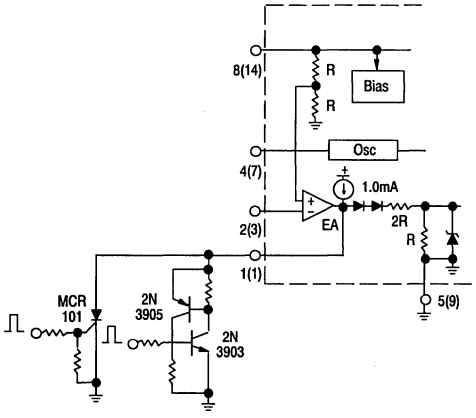
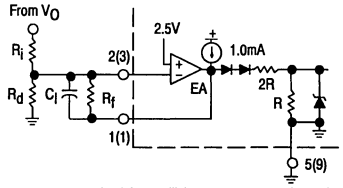


Figure 29. Latched Shutdown

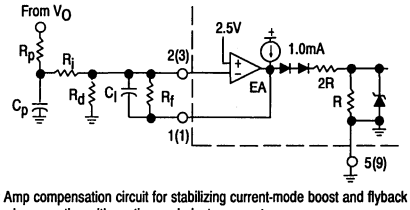


The MCR101 SCR must be selected for a holding of less than 0.5 mA at $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

Figure 30. Error Amplifier Compensation

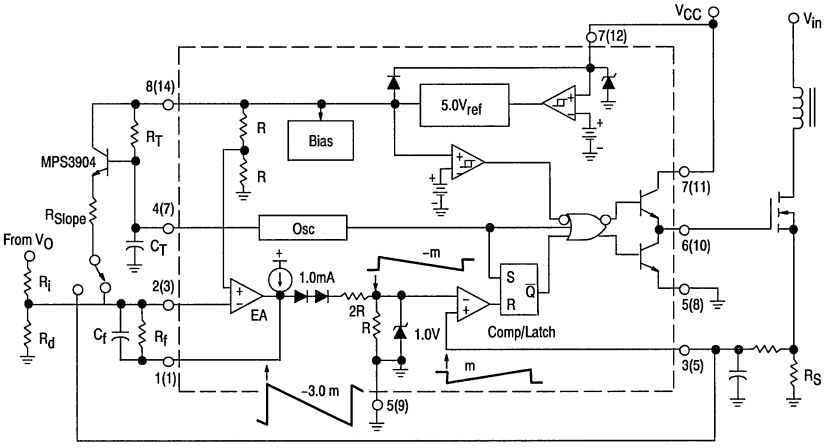


Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



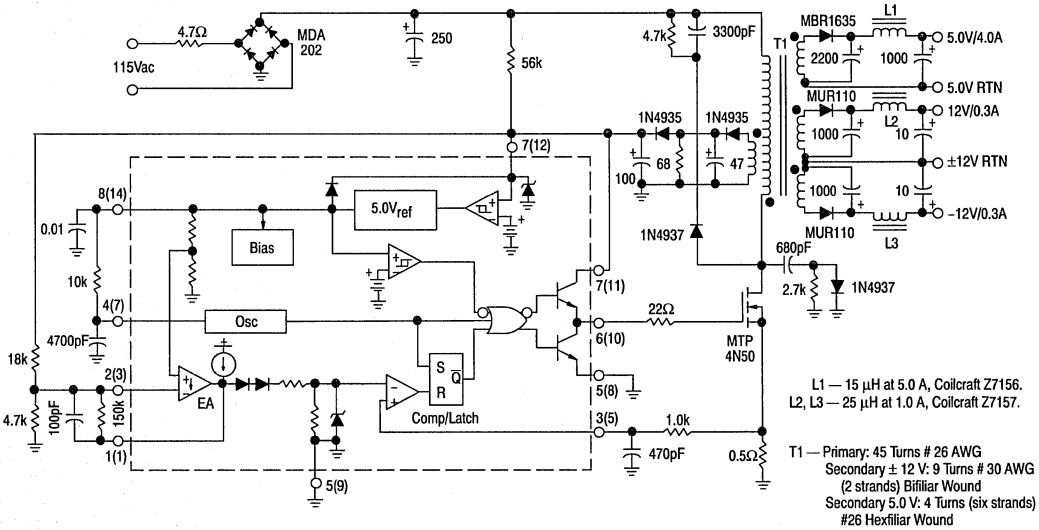
Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Figure 31. Slope Compensation



The buffered oscillator ramp can be resistively summed with either the voltage feedback or current sense inputs to provide slope compensation.

Figure 32. 27 Watt Off-Line Flyback Regulator



L1 — 15 µH at 5.0 A, Coilcraft Z7156.
L2, L3 — 25 µH at 1.0 A, Coilcraft Z7157.

T1 — Primary: 45 Turns # 26 AWG
Secondary ± 12 V: 9 Turns # 30 AWG
(2 strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands)
#26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG
(2 strands) Bifiliar Wound
Core: Ferroxcube EC35-3C8
Bobbin: Ferroxcube EC35PCB1
Gap ≈ 0.01" for a primary inductance of 1.0 mH

Line Regulation:	5.0 V ± 12 V	V_{in} = 95 Vac to 130 Vac	Δ = 50 mV or ± 0.5% Δ = 24 mV or ± 0.1%
Load Regulation:	5.0 V ± 12 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 300 mV or ± 3.0% Δ = 60 mV or ± 0.25%
Output Ripple:	5.0 V ± 12 V	V_{in} = 115 Vac	40 mV_{p-p} 80 mV_{p-p}
Efficiency		V_{in} = 115 Vac	70%

All outputs are at nominal load currents, unless otherwise noted.

UC3842B, 43B
UC2842B, 43B

HIGH PERFORMANCE CURRENT MODE CONTROLLERS

3

Advance Information

High Performance Current Mode Controllers

The UC3842B, UC3843B series are high performance fixed frequency current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost-effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

These devices are available in an 8-pin dual-in-line and surface mount (SO-8) plastic package as well as the 14-pin plastic surface mount (SO-14). The SO-14 package has separate power and ground pins for the totem pole output stage.

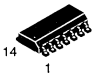
The UCX842B has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off-line converters. The UCX843B is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250 kHz
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current

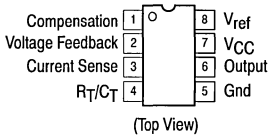
N SUFFIX
PLASTIC PACKAGE
CASE 626

D1 SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

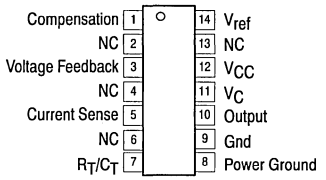
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



PIN CONNECTIONS

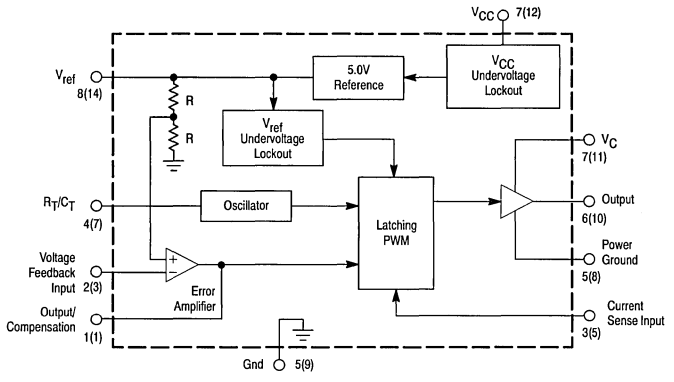


(Top View)



(Top View)

Simplified Block Diagram



Pin numbers adjacent to terminals are for the 8-pin dual-in-line package.
Pin numbers in parenthesis are for the D suffix SO-14 package.

ORDERING INFORMATION

Device	Temperature Range	Package
UC384XBD	0° to + 70°C	SO-14
UC384XBD1		SO-8
UC384XBN		Plastic
UC284XBD	– 25° to + 85°C	SO-14
UC284XBD1		SO-8
UC284XBN		Plastic
UC384XBVD	– 40° to +105°C	SO-14
UC384XBVD1		SO-8
UC384XBVN		Plastic

X indicates either a 2 or 3 to define specific device part numbers.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	– 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics			
D Suffix, Plastic Package, SO-14 Case 751A			
Maximum Power Dissipation @ T_A = 25°C	P_D	862	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	145	°C/W
D1 Suffix, Plastic Package, SO-8 Case 751			
Maximum Power Dissipation @ T_A = 25°C	P_D	702	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	178	°C/W
N Suffix, Plastic Package, Case 626			
Maximum Power Dissipation @ T_A = 25°C	P_D	1.25	W
Thermal Resistance Junction to Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
UC3842B, UC3843B		0 to + 70	
UC2842B, UC2843B		– 25 to + 85	
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	UC284XB			UC384XB, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	—	2.0	20	—	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	—	3.0	25	—	3.0	25	mV
Temperature Stability	T_S	—	0.2	—	—	0.2	—	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.9	—	5.1	4.82	—	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	—	50	—	—	50	—	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	—	5.0	—	—	5.0	—	mV
Output Short Circuit Current	I_{SC}	– 30	– 85	–180	– 30	– 85	–180	mA
OSCILLATOR SECTION								
Frequency	f_{OSC}							kHz
T_J = 25°C		49	52	55	49	52	55	
$T_A = T_{low}$ to T_{high}		48	—	56	48	—	56	
T_J = 25°C (R_T = 6.2 k, C_T = 1.0 nF)		225	250	275	225	250	275	
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{OSC}/\Delta V$	—	0.2	1.0	—	0.2	1.0	%
Frequency Change with Temperature $T_A = T_{low}$ to T_{high}	$\Delta f_{OSC}/\Delta T$	—	1.0	—	—	0.5	—	%
Oscillator Voltage Swing (Peak-to-Peak)	V_{OSC}	—	1.6	—	—	1.6	—	V
Discharge Current (V_{OSC} = 2.0 V)	I_{dischg}							mA
T_J = 25°C		7.8	8.3	8.8	7.8	8.3	8.8	
$T_A = T_{low}$ to T_{high} (UC284XB, UC384XB)		7.5	—	8.8	7.6	—	8.8	
(UC384XBV)		—	—	—	7.2	—	8.8	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for UC3842B, UC3843B; T_{high} = + 70°C for UC3842B, UC3843B
= – 25°C for UC2842B, UC2843B; = + 85°C for UC2842B, UC2843B
= – 40°C for UC3842BV, UC3843BV; = +105°C for UC3842BV, UC3843BV

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	UC284XB			UC384XB, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	—	– 0.1	–1.0	—	– 0.1	– 2.0	µA
Open-Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	—	65	90	—	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	—	0.7	1.0	—	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	—	60	70	—	dB
Output Current								mA
Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	—	2.0	12	—	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	– 0.5	–1.0	—	– 0.5	–1.0	—	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	—	5.0	6.2	—	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}							
(UC284XB, UC384XB)		—	0.8	1.1	—	0.8	1.1	
(UC384XBV)		—	—	—	—	0.8	1.2	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V							V/V
(UC284XB, UC384XB)		2.85	3.0	3.15	2.85	3.0	3.15	
(UC384XBV)		—	—	—	2.85	3.0	3.25	
Maximum Current Sense Input Threshold (Note 4)	V_{th}							V
(UC284XB, UC384XB)		0.9	1.0	1.1	0.9	1.0	1.1	
(UC384XBV)		—	—	—	0.85	1.0	1.1	
Power Supply Rejection Ratio V_{CC} = 12 V to 25 V, Note 4	PSRR	—	70	—	—	70	—	dB
Input Bias Current	I_{IB}	—	– 2.0	–10	—	– 2.0	–10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(In/Out)}$	—	150	300	—	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	—	0.1	0.4	—	0.1	0.4	
(I_{Sink} = 200 mA) (UC284XB, UC384XB)		—	1.6	2.2	—	1.6	2.2	
(UC384XBV)		—	—	—	—	1.6	2.3	
High State (I_{Source} = 20 mA) (UC284XB, UC384XB)	V_{OH}	13	13.5	—	13	13.5	—	
(UC384XBV)		—	—	—	12.9	13.5	—	
(I_{Source} = 200 mA)		12	13.4	—	12	13.4	—	
Output Voltage with UVLO Activated V_{CC} = 6.0 V, I_{Sink} = 1.0 mA	$V_{OL(UVLO)}$	—	0.1	1.1	—	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	—	50	150	—	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	—	50	150	—	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Start-Up Threshold (V_{CC})	V_{th}							V
UCX842B, BV		15	16	17	14.5	16	17.5	
UCX843B, BV		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn-On (V_{CC})	$V_{CC(min)}$							V
UCX842B, BV		9.0	10	11	8.5	10	11.5	
UCX843B, BV		7.0	7.6	8.2	7.0	7.6	8.2	

NOTES: 4. This parameter is measured at the latch trip point with V_{FB} = 0 V.

5. Comparator gain is defined as: $A_V = \frac{\Delta V \text{ Output/Compensation}}{\Delta V \text{ Current Sense Input}}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	UC284XB Min	UC284XB Typ	UC284XB Max	UC384XB, BV Min	UC384XB, BV Typ	UC384XB, BV Max	Unit
PWM SECTION								
Duty Cycle								%
Maximum (UC284XB, UC384XB)	$DC_{(max)}$	94	96	—	94	96	—	
(UC384XBV)		—	—	—	93	96	—	
Minimum	$DC_{(min)}$	—	—	0	—	—	0	
TOTAL DEVICE								
Power Supply Current	$I_{CC} + I_C$							mA
Start-Up (V_{CC} = 6.5 V for UCX843B, 14 V for UCX842B, BV)		—	0.3	0.5	—	0.3	0.5	
Operating (Note 2)		—	12	17	—	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	—	30	36	—	V

NOTES: 2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for UC3842B, UC3843B; = – 25°C for UC2842B, UC2843B; = – 40°C for UC3842BV, UC3843BV
T_{high} = + 70°C for UC3842B, UC3843B; = + 85°C for UC2842B, UC2843B; = +105°C for UC3842BV, UC3843BV

Figure 1. Timing Resistor versus Oscillator Frequency

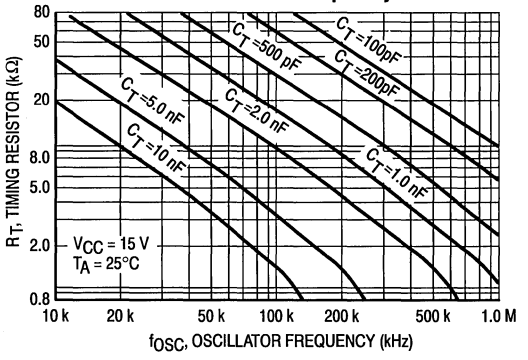


Figure 2. Output Dead-Time versus Oscillator Frequency

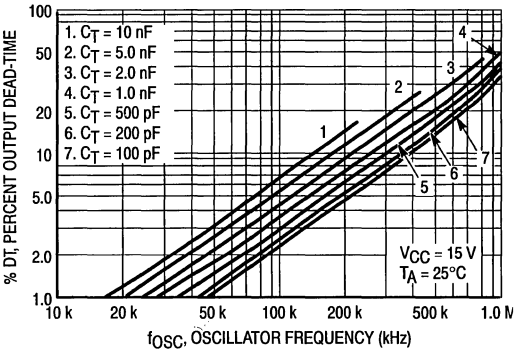


Figure 3. Oscillator Discharge Current versus Temperature

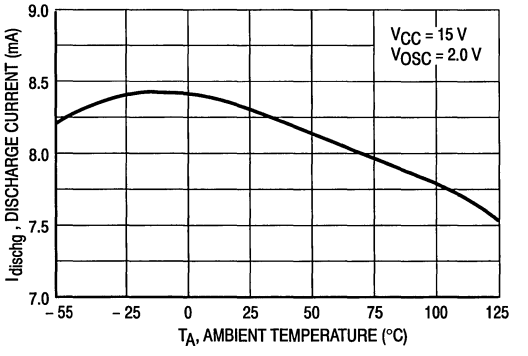


Figure 4. Maximum Output Duty Cycle versus Timing Resistor

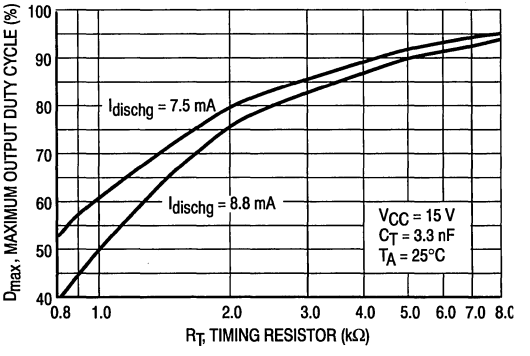


Figure 5. Error Amp Small Signal Transient Response

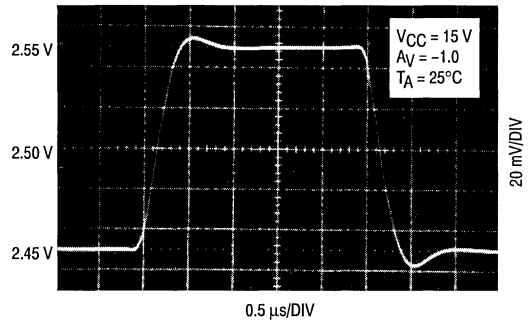


Figure 6. Error Amp Large Signal Transient Response

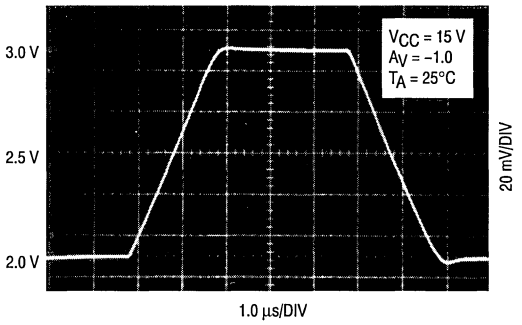


Figure 7. Error Amp Open-Loop Gain and Phase versus Frequency

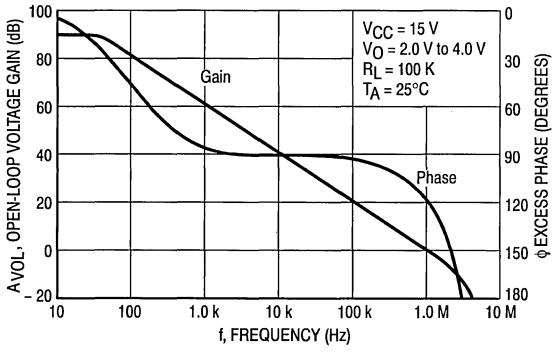


Figure 8. Current Sense Input Threshold versus Error Amp Output Voltage

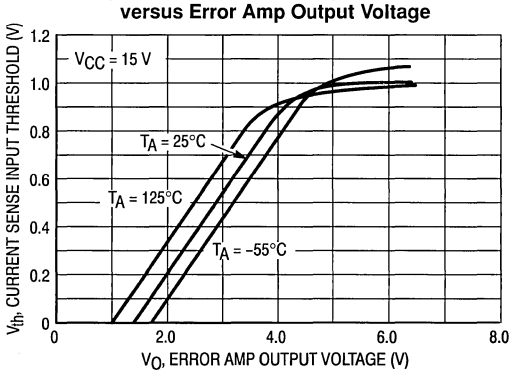


Figure 9. Reference Voltage Change versus Source Current

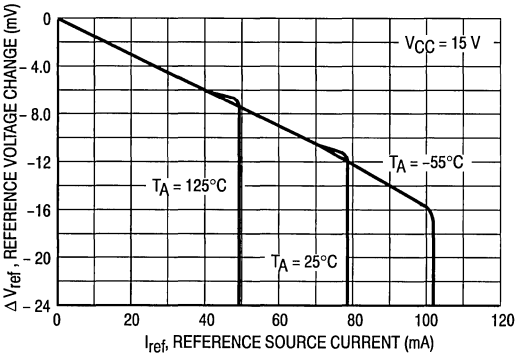


Figure 10. Reference Short Circuit Current versus Temperature

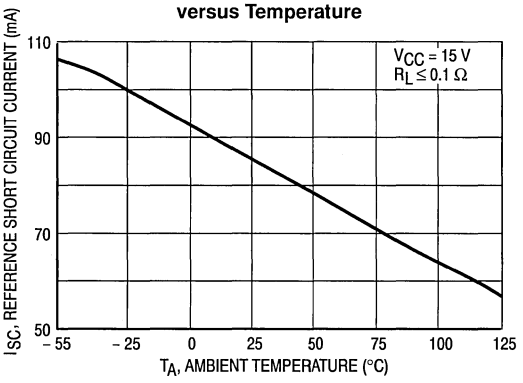


Figure 11. Reference Load Regulation

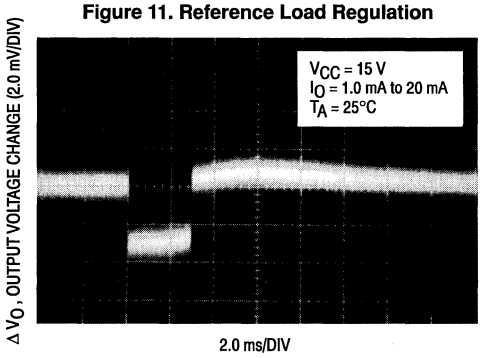


Figure 12. Reference Line Regulation

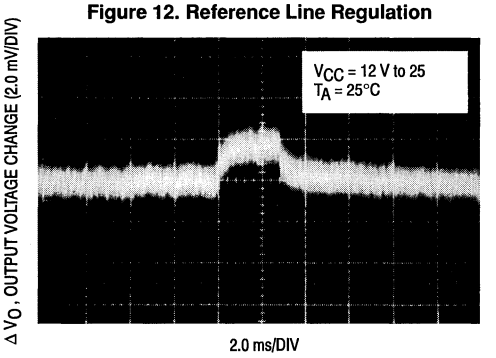


Figure 13. Output Saturation Voltage versus Load Current

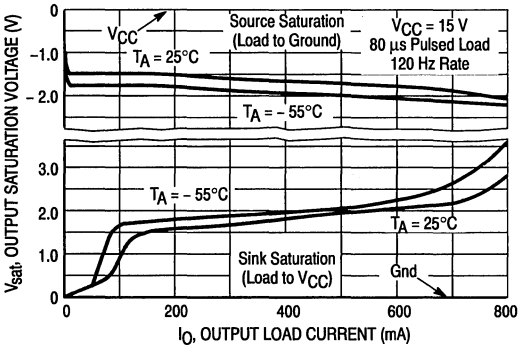


Figure 14. Output Waveform

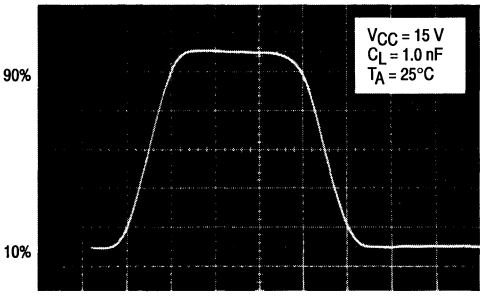


Figure 15. Output Cross Conduction

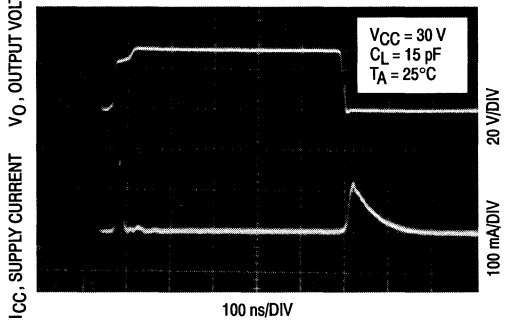
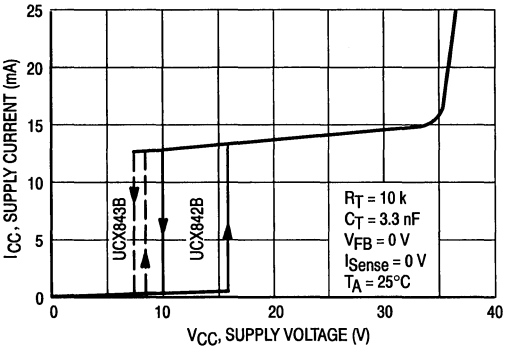


Figure 16. Supply Current versus Supply Voltage



Pin No.		Function	Description
8-Pin	14-Pin		
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 500 kHz is possible.
5		Gnd	This pin is the combined control circuitry and power ground.
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
	8	Power Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
	9	Gnd	This pin is the control circuitry ground return and is connected back to the power source ground.
	2,4,6,13	NC	No connection. These pins are not internally connected.

OPERATING DESCRIPTION

The UC3842B, UC3843B series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost-effective solution with minimal external components. A representative block diagram is shown in Figure 17.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated to within ±6% at 50 kHz. Also because of industry trends moving the UC384X into higher and higher frequency applications, the UC384XB is guaranteed to within ±10% at 250 kHz. These internal circuit refinements minimize variations of oscillator frequency and maximum output duty cycle. The results are shown in Figures 3 and 4.

In many noise-sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 20. For reliable locking, the free-running oscillator frequency should be set about 10% less than the clock frequency. A method for multi-unit synchronization is shown in Figure 21. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 7). The non-inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is –2.0 µA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 31). The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the non-inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figures 23, 24). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3842B, UC3843B operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground-referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 22. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability (refer to Figure 26).

Figure 17. Representative Block Diagram

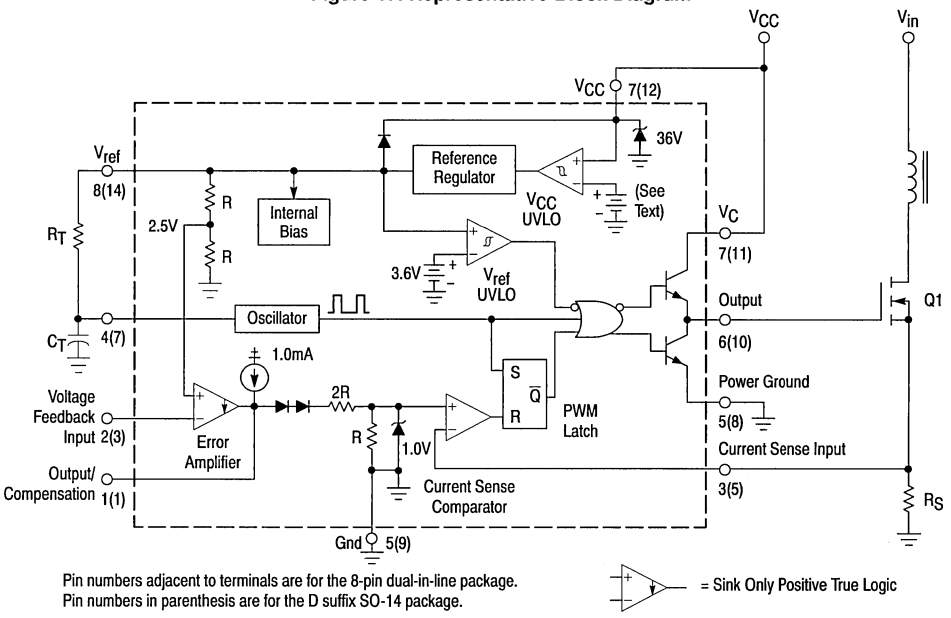
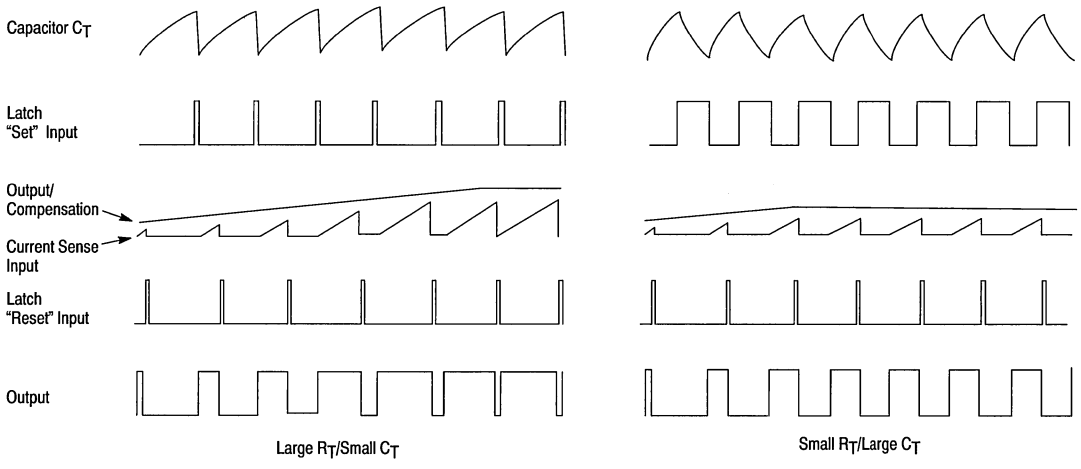


Figure 18. Timing Diagram



Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX842B, and 8.4 V/7.6 V for the UCX843B. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low start-up current of the UCX842B makes it ideally suited in off-line converter applications where efficient bootstrap start-up techniques are required (Figure 33). The UCX843B is intended for lower voltage DC-to-DC converter applications. A 36 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system start-up. The minimum operating voltage (V_{CC}) for the UCX842B is 11 V and 8.2 V for the UCX843B.

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull-down resistor.

The SO-14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 25 shows proper power and control ground connections in a current-sensing power MOSFET application.

Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the UC284XB, and ±2.0% on the UC384XB. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short-circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low-current signal and high-current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 µF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise-generating components.

Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than 50% with continuous inductor current. This instability is independent of the regulator's closed loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 19A shows the phenomenon graphically. At t_0, switch conduction begins, causing the inductor current to rise at a slope of m_1. This slope is a function of the input voltage divided by the inductance. At t_1, the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of m_2, until the next oscillator cycle. The unstable condition can be shown if a perturbation is added to the control voltage, resulting in a small ΔI (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn-on (t_2) is increased by $\Delta I + \Delta I\, m_2/m_1$. The minimum current at the next cycle (t_3) decreases to $(\Delta I + \Delta I\, m_2/m_1)(m_2/m_1)$. This perturbation is multiplied by m_2/m_1 on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn-on. Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If m_2/m_1 is greater than 1, the converter will be unstable. Figure 19B shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage, the ΔI perturbation will decrease to zero on succeeding cycles. This compensating ramp (m_3) must have a slope equal to or slightly greater than $m_2/2$ for stability. With $m_2/2$ slope compensation, the average inductor current follows the control voltage, yielding true current mode operation. The compensating ramp can be derived from the oscillator and added to either the Voltage Feedback or Current Sense inputs (Figure 32).

Figure 19. Continuous Current Waveforms

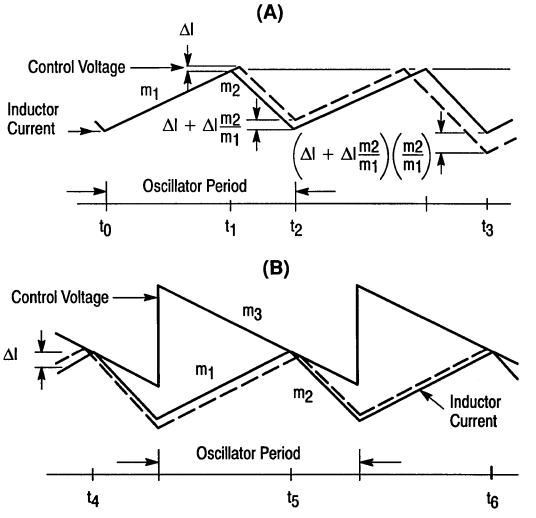
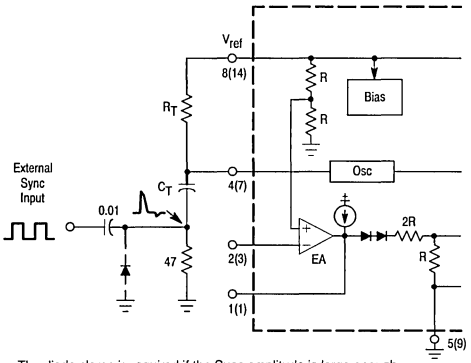
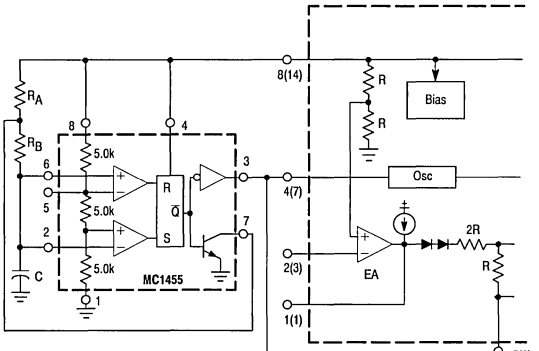


Figure 20. External Clock Synchronization



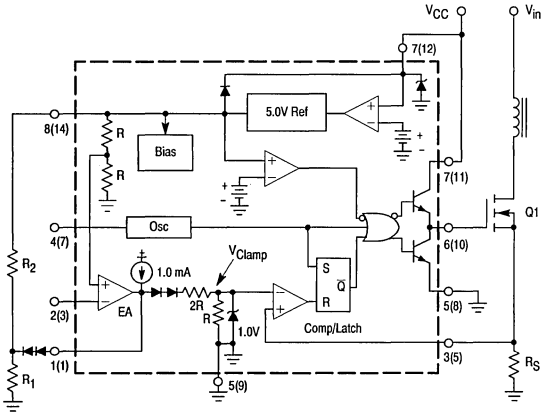
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

Figure 21. External Duty Cycle Clamp and Multi-Unit Synchronization



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D(max) = \frac{R_B}{R_A + 2R_B}$$

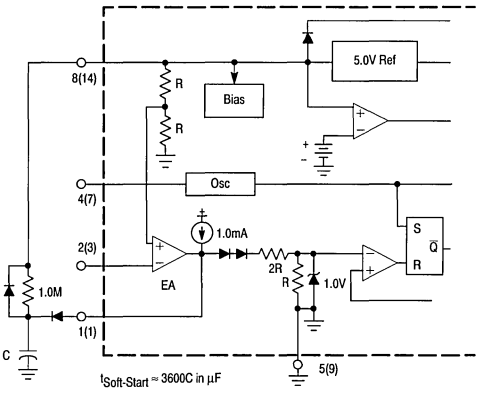
Figure 22. Adjustable Reduction of Clamp Level



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} + 0.33 \times 10^{-3}\left(\frac{R_1 R_2}{R_1 + R_2}\right) \qquad \text{Where: } 0 \le V_{Clamp} \le 1.0\ V$$

$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

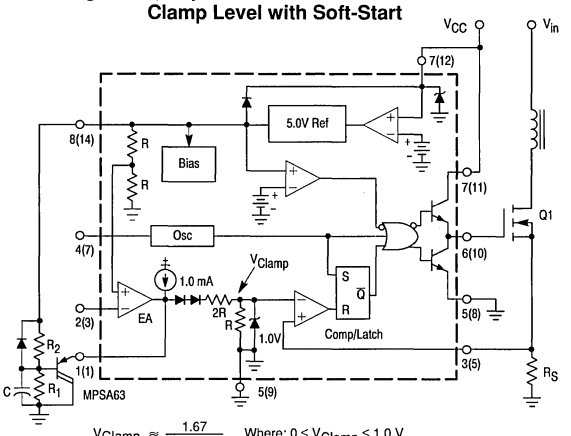
Figure 23. Soft-Start Circuit



$t_{Soft\text{-}Start} \approx 3600C$ in µF

3

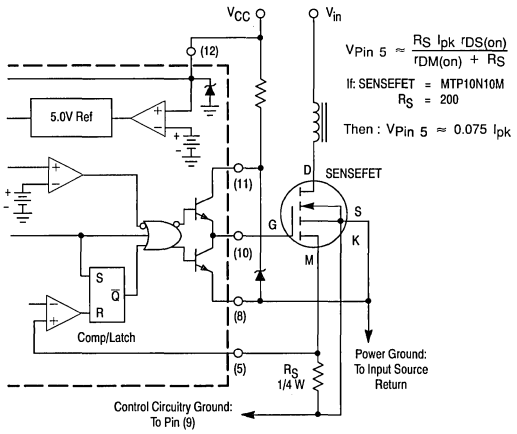
Figure 24. Adjustable Buffered Reduction of Clamp Level with Soft-Start



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R2}{R1} + 1\right)} \quad \text{Where: } 0 \le V_{Clamp} \le 1.0\ V$$

$$t_{Soft\text{-}Start} = -\ln\left[1 - \frac{VC}{3\ V_{Clamp}}\right] C\frac{R1\ R2}{R1 + R2} \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{RS}$$

Figure 25. Current Sensing Power MOSFET



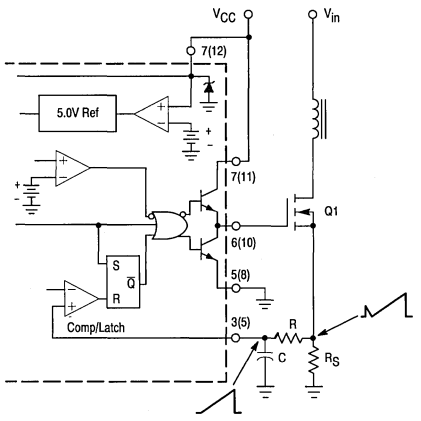
$$V_{Pin\ 5} \approx \frac{R_S\ I_{pk}\ r_{DS(on)}}{r_{DM(on)} + R_S}$$

If: SENSEFET = MTP10N10M
R_S = 200

Then : $V_{Pin\ 5} \approx 0.075\ I_{pk}$

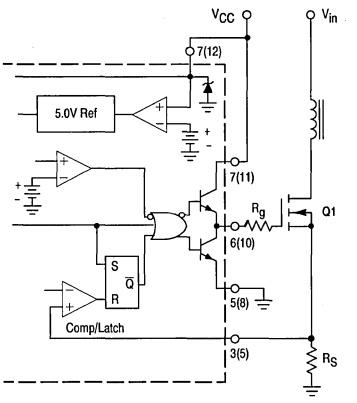
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over-current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 22 and 24.

Figure 26. Current Waveform Spike Suppression



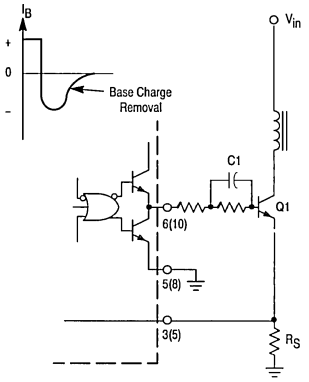
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 27. MOSFET Parasitic Oscillations



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

Figure 28. Bipolar Transistor Drive



The totem pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1.

Figure 29. Isolated MOSFET Drive

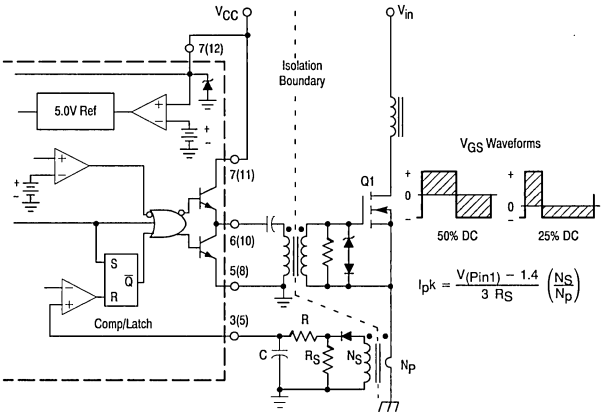
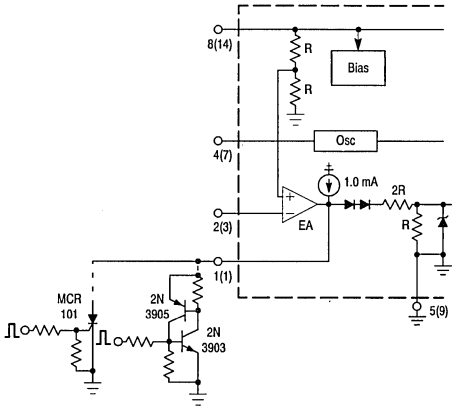
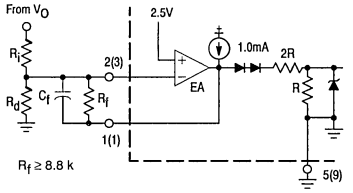


Figure 30. Latched Shutdown

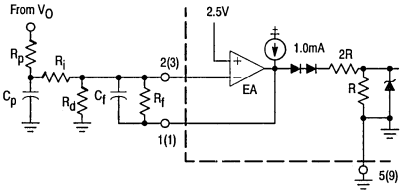


The MCR101 SCR must be selected for a holding of < 0.5 mA @ $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

Figure 31. Error Amplifier Compensation



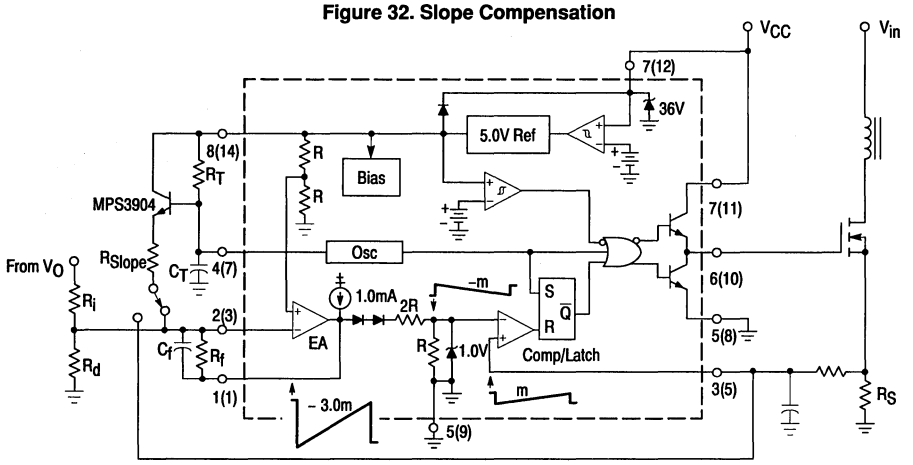
Error Amp compensation circuit for stabilizing any current mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current mode boost and flyback topologies operating with continuous inductor current.

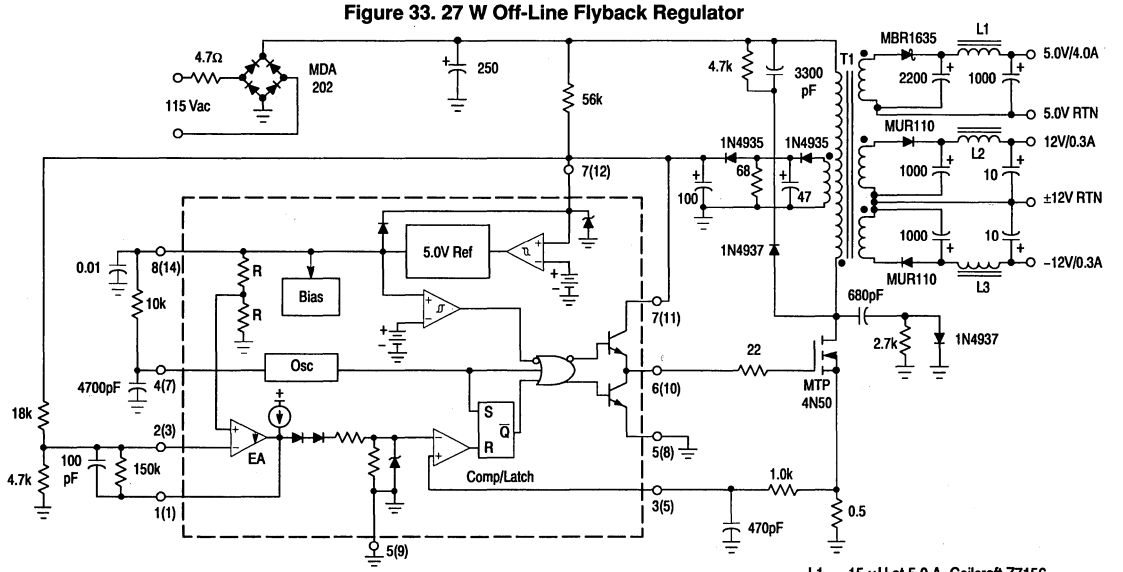
3

Figure 32. Slope Compensation



The buffered oscillator ramp can be resistively summed with either the voltage feedback or current sense inputs to provide slope compensation.

Figure 33. 27 W Off-Line Flyback Regulator



Line Regulation: 5.0 V ±12 V	V_{in} = 95 to 130 Vac	Δ = 50 mV or ± 0.5% Δ = 24 mV or ± 0.1%
Load Regulation: 5.0 V ±12 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 300 mV or ± 3.0% Δ = 60 mV or ± 0.25%
Output Ripple: 5.0 V ±12 V	V_{in} = 115 Vac	40 mV_{p-p} 80 mV_{p-p}
Efficiency	V_{in} = 115 Vac	70%

All outputs are at nominal load currents, unless otherwise noted

L1 — 15 µH at 5.0 A, Coilcraft Z7156
L2, L3 — 25 µH at 5.0 A, Coilcraft Z7157

T1 — Primary: 45 Turns #26 AWG
Secondary ±12 V: 9 Turns #30 AWG (2 Strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands) #26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EC35-3C8
Bobbin: Ferroxcube EC35PCB1
Gap: ≈ 0.10" for a primary inductance of 1.0 mH

UC3844, 45
UC2844, 45

HIGH PERFORMANCE CURRENT MODE CONTROLLER

3

Advance Information

High Performance Current Mode Controller

The UC3844, UC3845 series are high performance fixed frequency current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, a latch for single pulse metering, and a flip-flop which blanks the output off every other oscillator cycle, allowing output deadtimes to be programmed for 50% to 70%.

These devices are available in 8-pin dual-in-line ceramic and plastic packages as well as the 14-pin plastic surface mount (SO-14). The SO-14 package has separate power and ground pins for the totem pole output stage.

The UCX844 has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off-line converters. The UCX845 is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

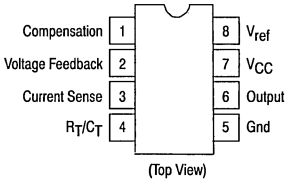
- Current Mode Operation to 500 kHz Output Switching Frequency
- Output Dead Time Adjustable from 50% to 70%
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Input Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

N SUFFIX
PLASTIC PACKAGE
CASE 626

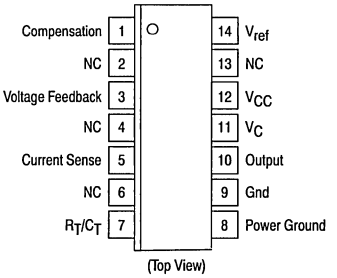
J SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS

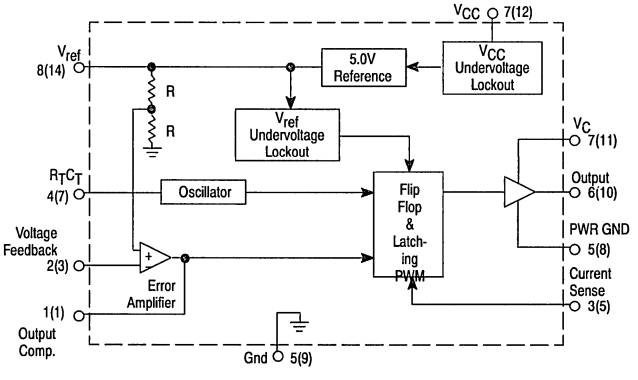


(Top View)



(Top View)

Simplified Block Diagram



Pin numbers adjacent to terminals are for the 8-pin dual-in-line package.
Pin numbers in parenthesis are for the D suffix SO-14 package.

ORDERING INFORMATION

Device	Temperature Range	Package
UC3844D	0° to + 70°C	SO–14
UC3845D		SO–14
UC3844N		Plastic
UC3845N		Plastic
UC2844D	–25° to + 85°C	SO–14
UC2845D		SO–14
UC2844J		Ceramic
UC2845J		Ceramic
UC2844N		Plastic
UC2845N		Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	− 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction-to-Air N Suffix, Plastic and J Suffix, Ceramic Packages Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction-to-Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+ 150	°C
Operating Ambient Temperature UC3844, UC3845 UC2844, UC2845	T_A	 0 to + 70 − 25 to + 85	°C
Storage Temperature Range	T_{stg}	− 65 to + 150	°C

ELECTRICAL CHARACTERICISTICS (V_{CC} = 15 V, [Note 2], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284X Min	UC284X Typ	UC284X Max	UC384X Min	UC384X Typ	UC384X Max	Unit
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	—	2.0	20	—	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	—	3.0	25	—	3.0	25	mV
Temperature Stability	T_S	—	0.2	—	—	0.2	—	mV/°C
Total Output Variation over Line, Load, Temperature	V_{ref}	4.9	—	5.1	4.82	—	5.18	V
Output Noise Voltage (f = 10 Hz to kHz, T_J = 25°C)	V_n	—	50	—	—	50	—	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	—	5.0	—	—	5.0	—	mV
Output Short Circuit Current	I_{SC}	− 30	− 85	− 180	− 30	− 85	− 180	mA
OSCILLATOR SECTION								
Frequency T_J = 25°C T_A = T_{low} to T_{high}	f_{osc}	 47 46	 52 —	 57 60	 47 46	 52 —	 57 60	kHz
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{osc}/\Delta V$	—	0.2	1.0	—	0.2	1.0	%
Frequency Change with Temperature T_A = T_{low} to T_{high}	$\Delta f_{osc}/\Delta T$	—	5.0	—	—	5.0	—	%
Oscillator Voltage Swing (Peak-to-Peak)	V_{osc}	—	1.6	—	—	1.6	—	V
Discharge Current (V_{osc} = 2.0 V, T_J = 25°C)	I_{dischg}	—	10.8	—	—	10.8	—	mA

NOTES: 1. Maximum Package power dissipation limits must be observed.
2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for UC3844, UC3845; −25°C for UC2844, UC2845 T_{high} = +70°C for UC3844, UC3845; +85°C for UC2844, UC2845

ELECTRICAL CHARACTERICISTICS (V_{CC} = 15 V, [Note 2], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted,)

Characteristics	Symbol	UC284X Min	UC284X Typ	UC284X Max	UC384X Min	UC384X Typ	UC384X Max	Unit
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 2.7 V)	I_{IB}	—	–0.1	–1.0	—	–0.1	–2.0	µA
Open-Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	—	65	90	—	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	—	0.7	1.0	—	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	—	60	70	—	dB
Output Current								mA
Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	—	2.0	12	—	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	–0.5	–1.0	—	–0.5	–1.0	—	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	—	5.0	6.2	—	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}	—	0.8	1.1	—	0.8	1.1	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V	2.85	3.0	3.15	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	0.9	1.0	1.1	V
Power Supply Rejection Ratio V_{CC} = 12 V to 25 V (Note 4)	PSRR	—	70	—	—	70	—	dB
Input Bias Current	I_{IB}	—	–2.0	–10	—	–2.0	–10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(IN/OUT)}$	—	150	300	—	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	—	0.1	0.4	—	0.1	0.4	
(I_{Sink} = 200 mA)		—	1.6	2.2	—	1.6	2.2	
High State (I_{Sink} = 20 mA)	V_{OH}	12	13.5	—	13	13.5	—	
(I_{Sink} = 200 mA)		12	13.4	—	12	13.4	—	
Output Voltage with UVLO Activated V_{CC} = 6.0 V, I_{Sink} = 1.0 mA	$V_{OL(UVLO)}$	—	0.1	1.1	—	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	—	50	150	—	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	—	50	150	—	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Start-Up Threshold	V_{th}							V
UCX844		15	16	17	14.5	16	17.5	
UCX845		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn-On	$V_{CC(min)}$							V
UCX844		9.0	10	11	8.5	10	11.5	
UCX845		7.0	7.6	8.2	7.0	7.6	8.2	
PWM SECTION								
Duty Cycle								%
Maximum	DC_{max}	46	48	50	47	48	50	
Minimum	DC_{min}	—	—	0	—	—	0	
TOTAL DEVICE								
Power Supply Current (Note 2)	I_{CC}							mA
Start-Up:								
(V_{CC} = 6.5 V for UCX845A,		—	0.5	1.0	—	0.5	1.0	
14 V for UCX844) Operating		—	12	17	—	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	—	30	36	—	V

NOTES: 4. This parameter is measured at the latch trip point with V_{FB} = 0 V.

5. Comparator gain is defined as: $A_V \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$

Figure 1. Timing Resistor versus Oscillator Frequency

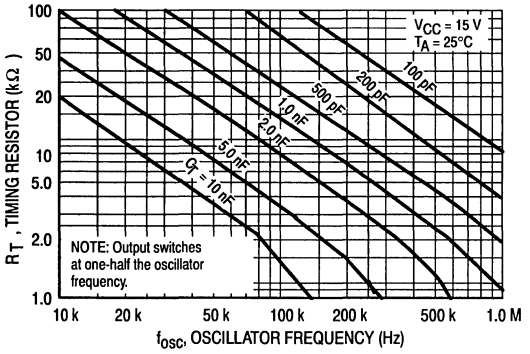


Figure 2. Output Dead Time versus Oscillator Frequency

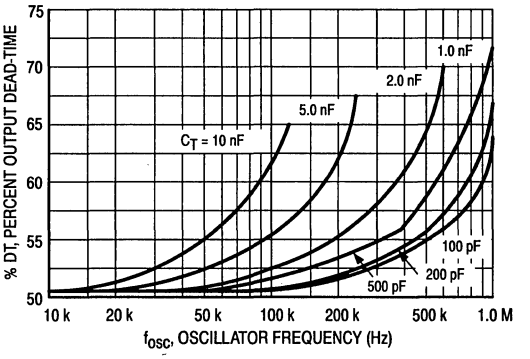


Figure 3. Error Amp Small Signal Transient Response

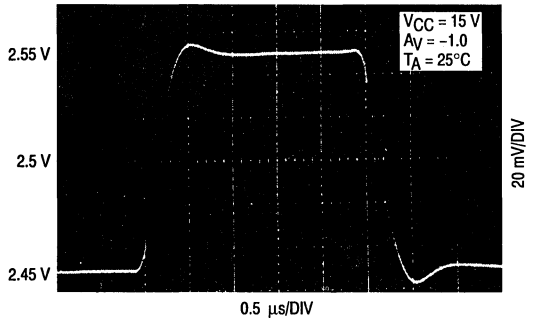


Figure 4. Error Amp Large Signal Transient Response

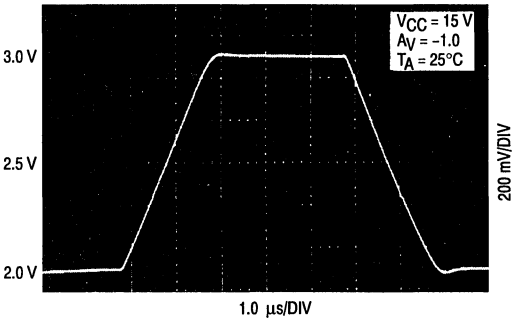


Figure 5. Error Amp Open-Loop Gain and Phase versus Frequency

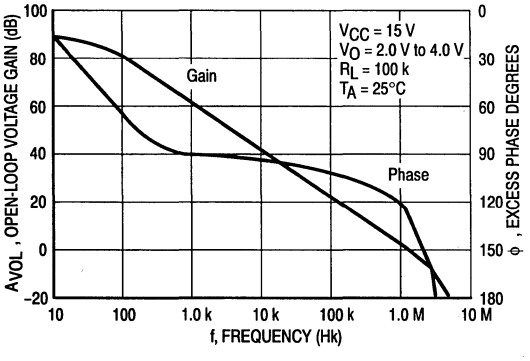


Figure 6. Current Sense Input Threshold versus Error Amp Output Voltage

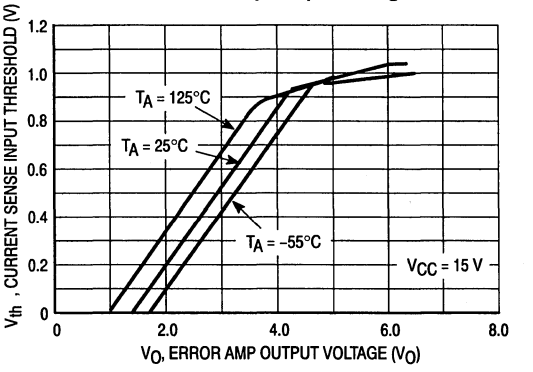


Figure 7. Reference Voltage Change versus Source Current

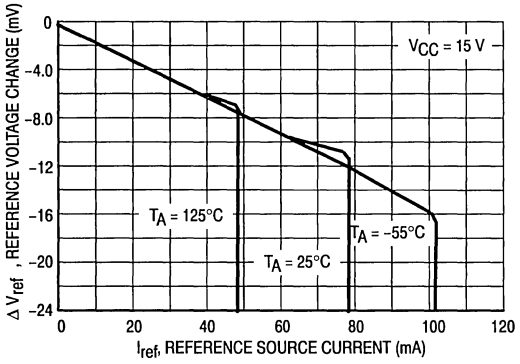


Figure 8. Reference Short Circuit Current versus Temperature

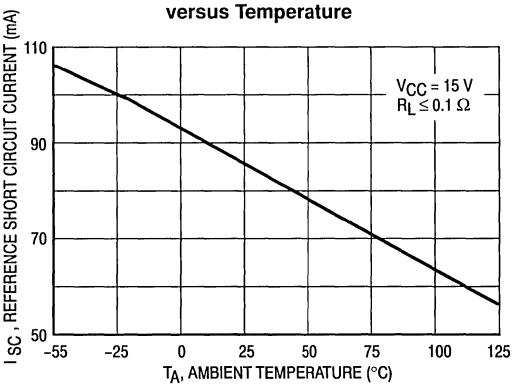


Figure 9. Reference Load Regulation

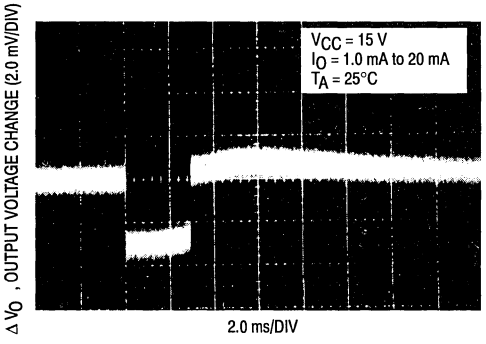


Figure 10. Reference Line Regulation

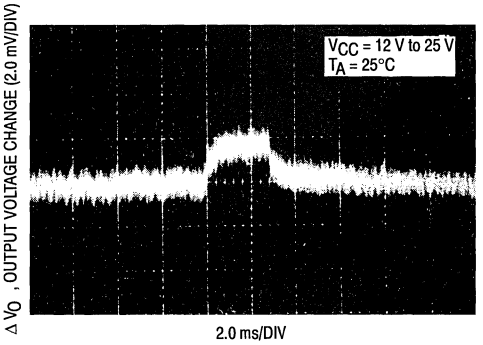


Figure 11. Output Saturation Voltage versus Load Current

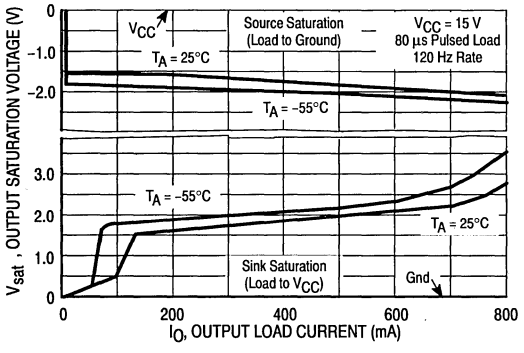


Figure 12. Output Waveform

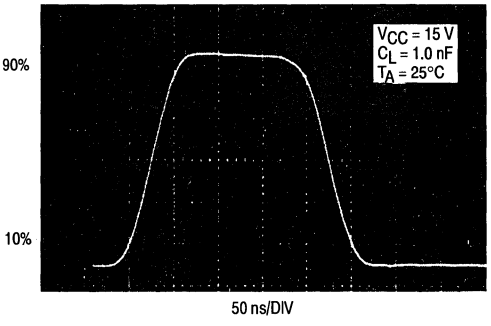


Figure 13. Output Cross Conduction

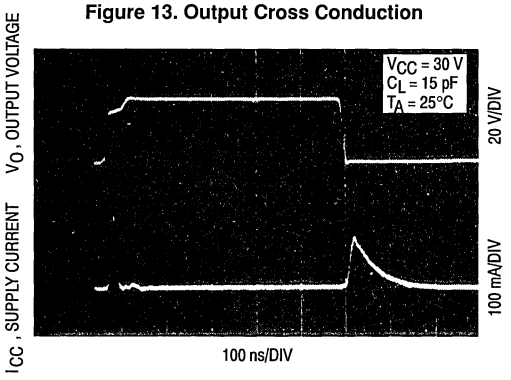
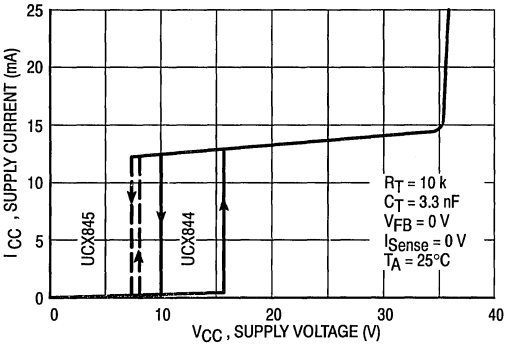


Figure 14. Supply Current versus Supply Voltatage



PIN FUNCTION DESCRIPTION

Pin No.			
8-Pin	14-Pin	Function	Description
1	1	Compensation	This pin is Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 1.0 MHz is possible.
5	—	Gnd	This pin is combined control circuitry and power ground (8-pin package only).
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin. The output switches at one-half the oscillator frequency.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
—	8	Power Ground	This pin is a separate power ground return (14-pin package only) that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
—	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin (14-pin package only). With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
—	9	Gnd	This pin is the control circuitry ground return (14-pin package only) and is connected to back to the power source ground.
—	2,4,6,13	NC	No connection (14-pin package only). These pins are not internally connected.

OPERATING DESCRIPTION

The UC3844, UC3845 series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 15.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. An internal flip-flop has been incorporated in the UCX844/5 which blanks the output off every other clock cycle by holding one of the inputs of the NOR gate high. This in combination with the C_T discharge period yields output deadtimes programmable from 50% to 70%. Figure 1 shows R_T versus Oscillator Frequency and figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency.

In many noise sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 17. For reliable locking, the free-running oscillator frequency should be set about 10% less than the clock frequency. A method for multi unit synchronization is shown in Figure 18. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved to realize output deadtimes of greater than 70%

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 5). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is –2.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provide for external loop compensation (Figure 28). The output voltage is offset by two diode drops (≈ 1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figures 20, 21). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\,(1.0\text{ V}) + 1.4\text{ V}}{0.5\text{ mA}} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3844, UC3845 operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin1). Thus the error signal controls the inductor current on a cycle-by-cycle basis. The current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V_{(Pin\,1)} - 1.4\text{ V}}{3\,R_S}$$

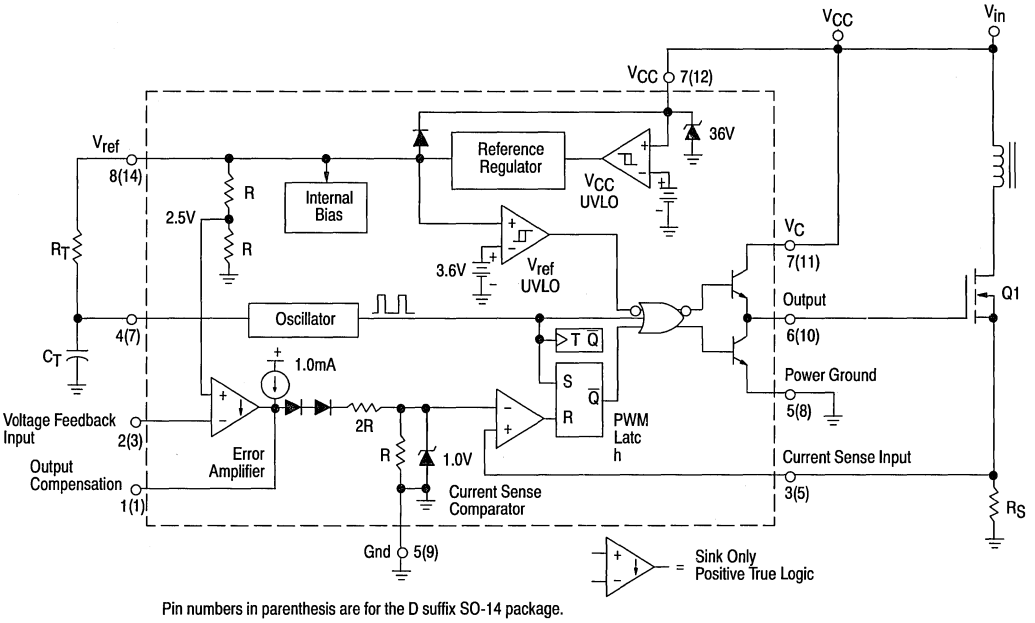
Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\text{ V}}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

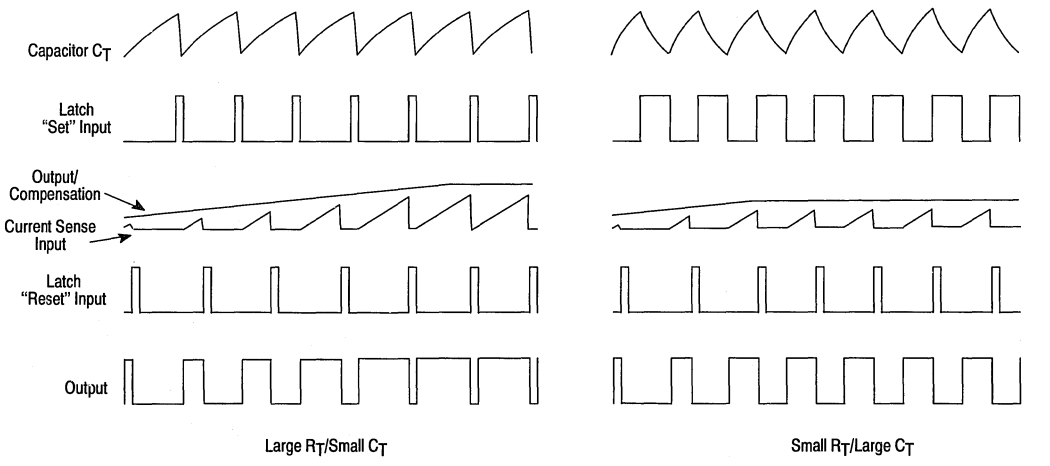
A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 23.

Figure 15. Representative Block Diagram



Pin numbers in parenthesis are for the D suffix SO-14 package.

Figure 16. Timing Diagram



Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guartantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC} and the reference output (V_{ref}) are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX844, and 8.4 V/7.6 V for the UCX845. The V_{ref} comparator upper and lower thresholds are 3.6 V/3/4 V. The large hysteresis and low start-up current of the UCX844 makes it ideally suited in off-line converter applications where efficient bootstrap start-up techniques later required (Figure 29). The UCX845 is intended for lower voltage DC-to-DC converter applications. A 36 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system start-up. The minimum operating voltage for the UCX844 is 11 V and 8.2 V for the UCX845.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ± 1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever and undervoltage lockout is active. This characteristic eliminates the need for an external pull-down resistor.

The SO-14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater the 20 V. Figure 22 shows proper power and control ground connections in a current sensing power MOSFET application.

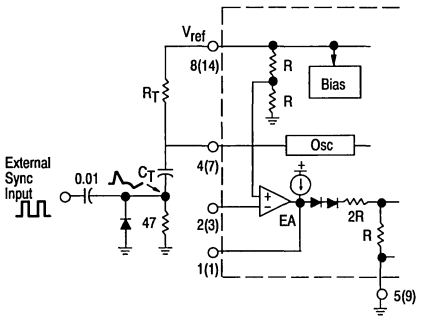
Reference

The 5.0 V bandgap reference is trimmed to ± 1.0% tolerance at T_J = 25°C on the UC284X, and ± 2.0% on the UC384X. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

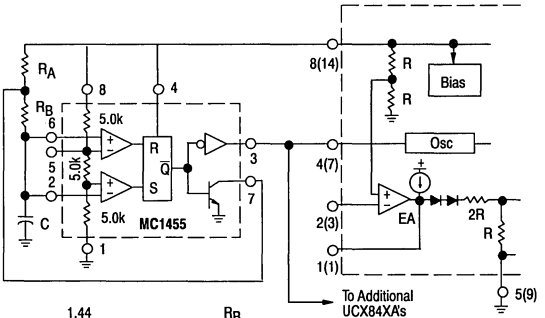
Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulsewidth jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low-current signal and high-current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 µF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

Figure 17. External Clock Synchronization



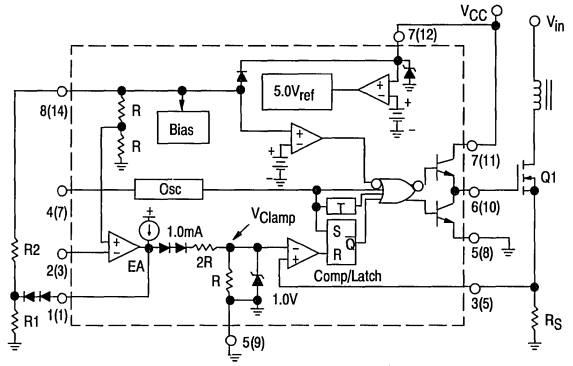
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

Figure 18. External Duty Cycle Clamp and Multi Unit Synchronization



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_B}{R_A + 2R_B}$$

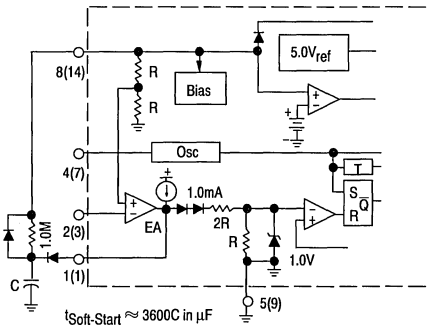
Figure 19. Adjustable Reduction of Clamp Level



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1}+1\right)} + 0.33 \times 10^{-3}\left(\frac{R_1 R_2}{R_1+R_2}\right) \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

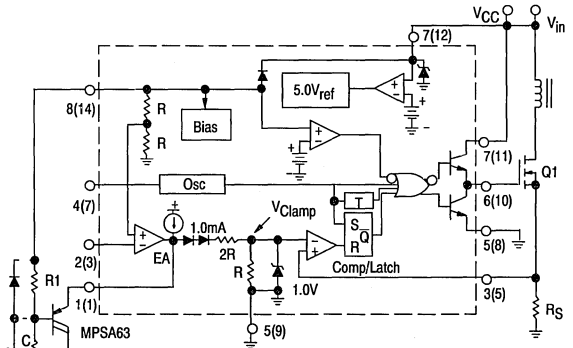
Where: $0 \le V_{Clamp} \le 1.0\ V$

Figure 20. Soft-Start Circuit



$t_{Soft\text{-}Start} \approx 3600C$ in μF

Figure 21. Adjustable Buffered Reduction of Clamp Level with Soft-Start

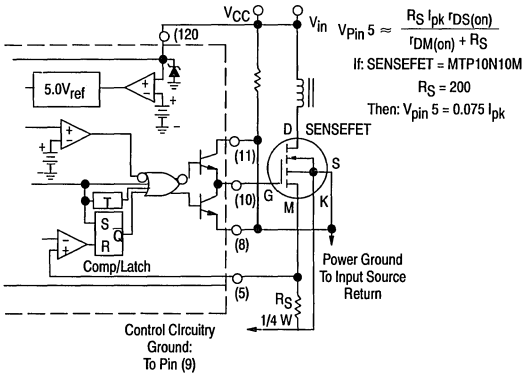


$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1}+1\right)} + 0.33 \times 10^{-3}\left(\frac{R_1 R_2}{R_1+R_2}\right) \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Where: $0 \le V_{Clamp} \le 1.0\ V$

$$t_{Softstart} = -\ln\left[1 - \frac{V_C}{3V_{Clamp}}\right] C\left(\frac{R_1 R_2}{R_1+R_2}\right)$$

Figure 22. Current Sensing Power MOSFET



$$V_{Pin\,5} \approx \frac{R_S I_{pk} r_{DS(on)}}{r_{DM(on)} + R_S}$$

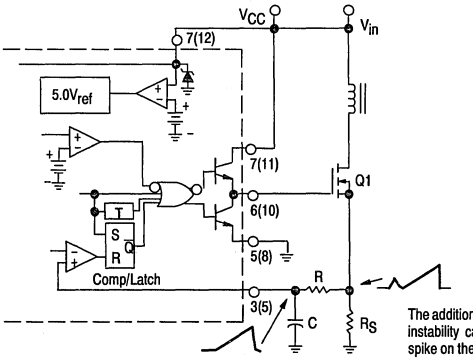
If: SENSEFET = MTP10N10M

$R_S = 200$

Then: $V_{pin\,5} = 0.075\ I_{pk}$

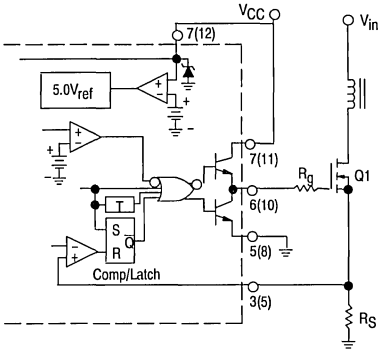
Virtually lossless current sensing can be achieved with the implement of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 19 and 21.

Figure 23. Current Waveform Spike Suppression



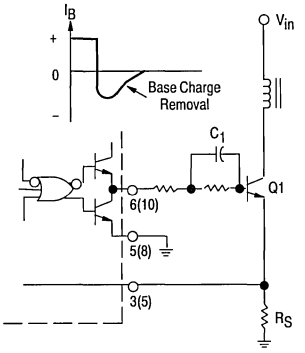
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 24. MOSFET Parasitic Oscillations



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

Figure 25. Bipolar Transistor Drive



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1.

Figure 26. Isolated MOSFET Drive

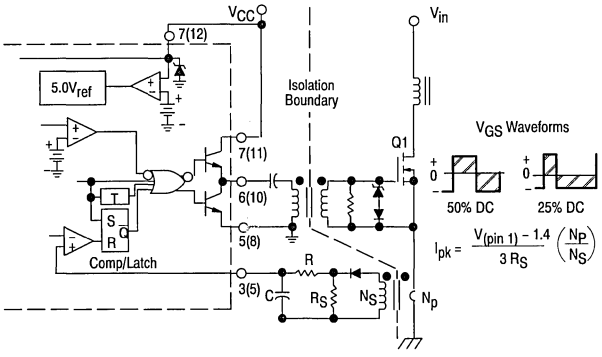
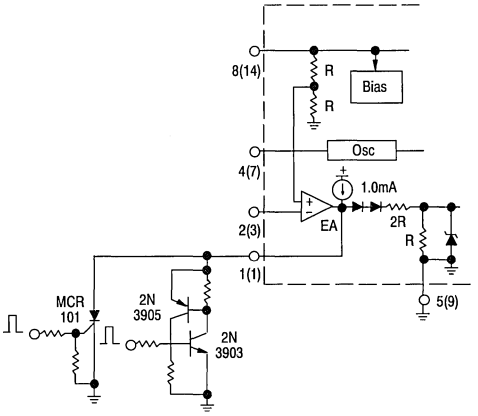
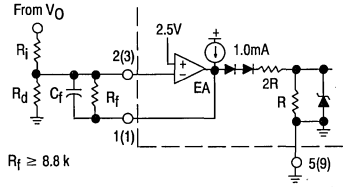


Figure 27. Latched Shutdown

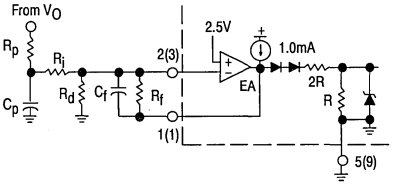


The MCR101 SCR must be selected for a holding of less than 0.5 mA at $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

Figure 28. Error Amplifier Compensation

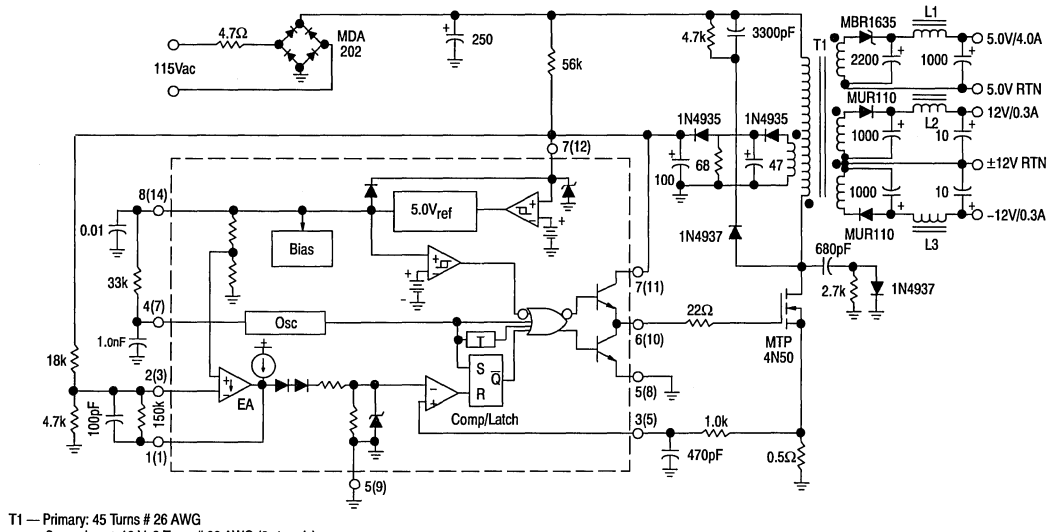


Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Figure 29. 27 Watt Off-Line Flyback Regulator



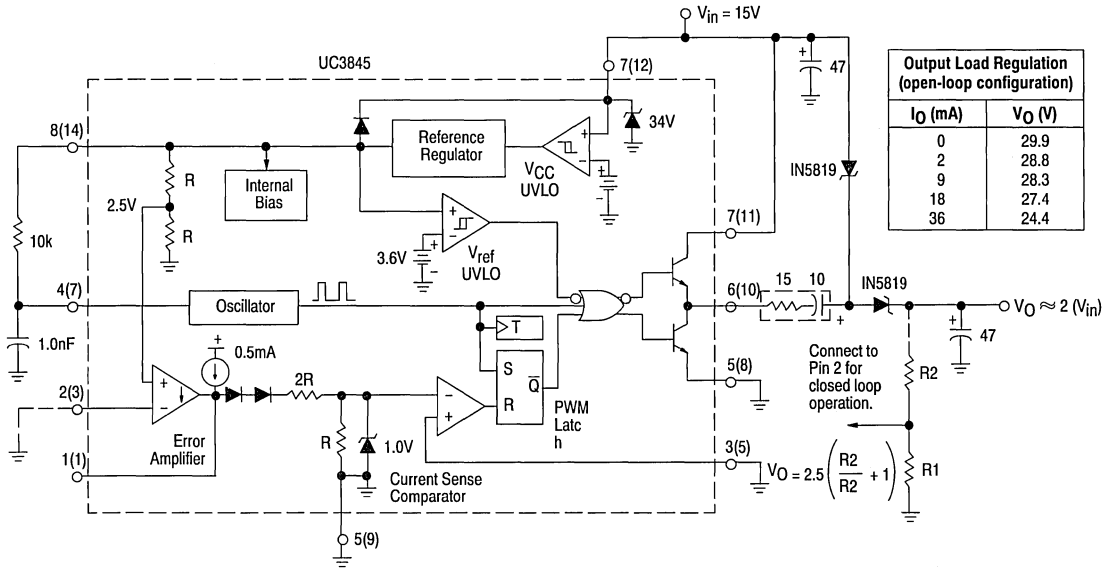
T1 — Primary: 45 Turns # 26 AWG
Secondary ± 12 V: 9 Turns # 30 AWG (2 strands)
Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands)
#26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG (2 strands)
Bifiliar Wound
Core: Ferroxcube EC35-3C8
Bobbin: Ferroxcube EC35PCB1
Gap ≈ 0.10" for a primary inductance of 1.0 mH

L1 — 15 μH at 5.0 A, Coilcraft Z7156.
L2, L3 — 25 μH at 1.0 A, Coilcraft Z7157.

Line Regulation:	5.0 V ± 12 V	V_{in} = 95 Vac to 130 Vac	Δ = 50 mV or ± 0.5% Δ = 24 mV or ± 0.1%
Load Regulation:	5.0 V ± 12 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 300 mV or ± 3.0% Δ = 60 mV or ± 0.25%
Output Ripple:	5.0 V ± 12 V	V_{in} = 115 Vac	40 mV_{p-p} 80 mV_{p-p}
Efficiency		V_{in} = 115 Vac	70%

All outputs are at nominal load currents, unless otherwise noted.

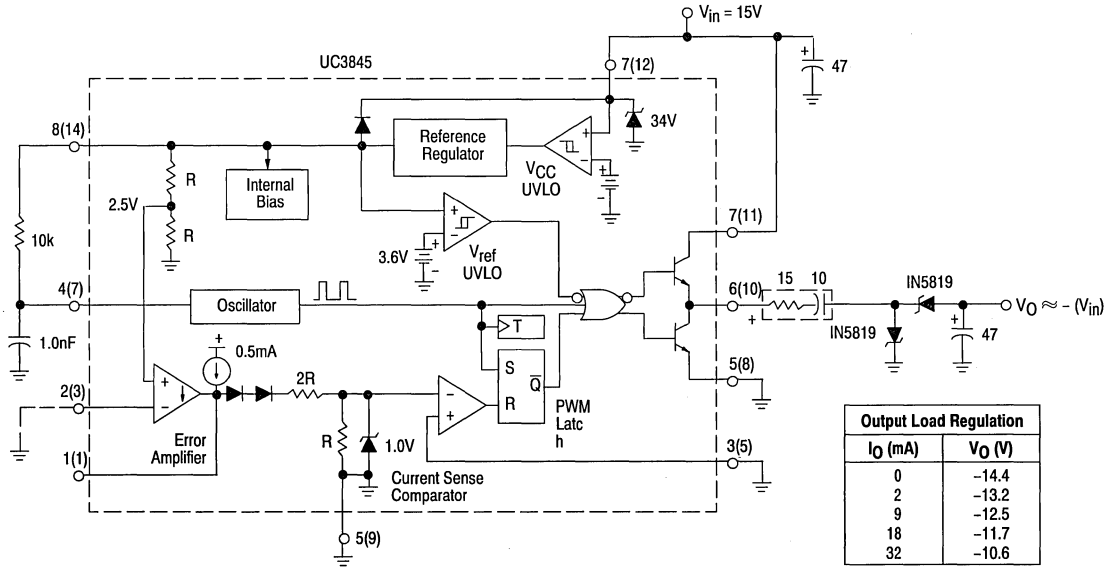
Figure 30. Step-Up Charge Pump Converter



Output Load Regulation (open-loop configuration)	
I_O (mA)	V_O (V)
0	29.9
2	28.8
9	28.3
18	27.4
36	24.4

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A. An additional series resistor may be required when using tantalum or other low ESR capacitors. The converter's output can provide excellent line and load regulation by connecting the R2/R1 resistor divider as shown.

Figure 31. Voltage-Inverting Charge Pump Converter



Output Load Regulation	
I_O (mA)	V_O (V)
0	-14.4
2	-13.2
9	-12.5
18	-11.7
32	-10.6

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A.
An additional series resistor may be required when using tantalum or other low ESR capacitors.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

UC3844B, 45B
UC2844B, 45B

3

Advance Information

High Performance Current Mode Controllers

HIGH PERFORMANCE CURRENT MODE CONTROLLERS

The UC3844B, UC3845B series are high performance fixed frequency current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost-effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

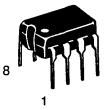
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, a latch for single pulse metering, and a flip-flop which blanks the output off every other oscillator cycle, allowing output deadtimes to be programmed from 50% to 70%.

These devices are available in an 8-pin dual-in-line and surface mount (SO-8) plastic package as well as the 14-pin plastic surface mount (SO-14). The SO-14 package has separate power and ground pins for the totem pole output stage.

The UCX844B has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off-line converters. The UCX845B is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

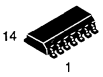
- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250 kHz
- Current Mode Operation to 500 kHz Output Switching Frequency
- Output Deadtime Adjustable from 50% to 70%
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current

N SUFFIX
PLASTIC PACKAGE
CASE 626

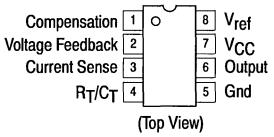


D1 SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

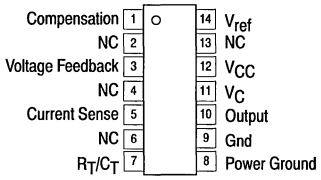
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



PIN CONNECTIONS

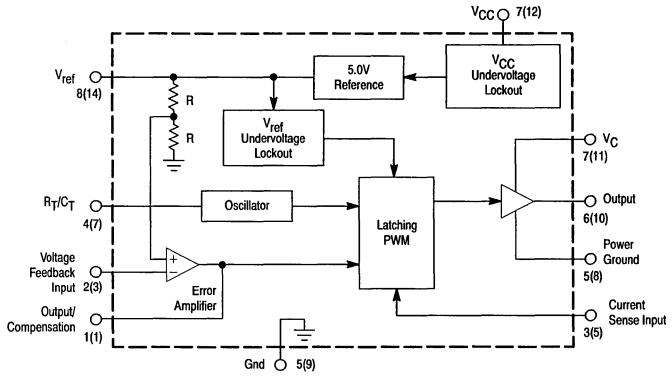


(Top View)



(Top View)

Simplified Block Diagram



Pin numbers adjacent to terminals are for the 8-pin dual-in-line package.
Pin numbers in parenthesis are for the D suffix SO-14 package.

ORDERING INFORMATION

Device	Temperature Range	Package
UC384XBD	0° to + 70°C	SO-14
UC384XBD1		SO-8
UC384XBN		Plastic
UC284XBD	– 25° to + 85°C	SO-14
UC284XBD1		SO-8
UC284XBN		Plastic
UC384XBVD	– 40° to +105°C	SO-14
UC384XBVD1		SO-8
UC384XBVN		Plastic

X indicates either a 4 or 5 to define specific device part numbers.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	− 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics			
D Suffix, Plastic Package, SO-14 Case 751A			
Maximum Power Dissipation @ T_A = 25°C	P_D	862	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	145	°C/W
D1 Suffix, Plastic Package, SO-8 Case 751			
Maximum Power Dissipation @ T_A = 25°C	P_D	702	mW
Thermal Resistance Junction to Air	$R_{\theta JA}$	178	°C/W
N Suffix, Plastic Package, Case 626			
Maximum Power Dissipation @ T_A = 25°C	P_D	1.25	W
Thermal Resistance Junction to Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
UC3844B, UC3845B		0 to + 70	
UC2844B, UC2845B		− 25 to + 85	
Storage Temperature Range	T_{stg}	− 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	UC284XB			UC384XB, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	—	2.0	20	—	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	—	3.0	25	—	3.0	25	mV
Temperature Stability	T_S	—	0.2	—	—	0.2	—	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.9	—	5.1	4.82	—	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	—	50	—	—	50	—	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	—	5.0	—	—	5.0	—	mV
Output Short Circuit Current	I_{SC}	− 30	− 85	−180	− 30	− 85	−180	mA
OSCILLATOR SECTION								
Frequency	f_{OSC}							kHz
T_J = 25°C		49	52	55	49	52	55	
T_A = T_{low} to T_{high}		48	—	56	48	—	56	
T_J = 25°C (R_T = 6.2 k, C_T = 1.0 nF)		225	250	275	225	250	275	
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{OSC}/\Delta V$	—	0.2	1.0	—	0.2	1.0	%
Frequency Change with Temperature T_A = T_{low} to T_{high}	$\Delta f_{OSC}/\Delta T$	—	1.0	—	—	0.5	—	%
Oscillator Voltage Swing (Peak-to-Peak)	V_{OSC}	—	1.6	—	—	1.6	—	V
Discharge Current (V_{OSC} = 2.0 V)	I_{dischg}							mA
T_J = 25°C		7.8	8.3	8.8	7.8	8.3	8.8	
T_A = T_{low} to T_{high} (UC284XB, UC384XB)		7.5	—	8.8	7.6	—	8.8	
(UC384XBV)		—	—	—	7.2	—	8.8	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for UC3844B, UC3845B; T_{high} = + 70°C for UC3844B, UC3845B
= − 25°C for UC2844B, UC2845B; = + 85°C for UC2844B, UC2845B
= − 40°C for UC3844BV, UC3845BV; = +105°C for UC3844BV, UC3845BV

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25° C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	UC284XB Min	UC284XB Typ	UC284XB Max	UC384XB, XBV Min	UC384XB, XBV Typ	UC384XB, XBV Max	Unit
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	—	– 0.1	–1.0	—	– 0.1	– 2.0	µA
Open-Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	—	65	90	—	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	—	0.7	1.0	—	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	—	60	70	—	dB
Output Current								mA
Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	—	2.0	12	—	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	– 0.5	–1.0	—	– 0.5	–1.0	—	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	—	5.0	6.2	—	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}							
(UC284XB, UC384XB)		—	0.8	1.1	—	0.8	1.1	
(UC384XBV)		—	—	—	—	0.8	1.2	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V							V/V
(UC284XB, UC384XB)		2.85	3.0	3.15	2.85	3.0	3.15	
(UC384XBV)		—	—	—	2.85	3.0	3.25	
Maximum Current Sense Input Threshold (Note 4)	V_{th}							V
(UC284XB, UC384XB)		0.9	1.0	1.1	0.9	1.0	1.1	
(UC384XBV)		—	—	—	0.85	1.0	1.1	
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V, Note 4)	PSRR	—	70	—	—	70	—	dB
Input Bias Current	I_{IB}	—	– 2.0	–10	—	– 2.0	–10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(In/Out)}$	—	150	300	—	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	—	0.1	0.4	—	0.1	0.4	
(I_{Sink} = 200 mA, UC284XB, UC384XB)		—	1.6	2.2	—	1.6	2.2	
(I_{Sink} = 200 mA, UC384XBV)		—	—	—	—	1.6	2.3	
High State (I_{Source} = 20 mA, UC284XB, UC384XB)	V_{OH}	13	13.5	—	13	13.5	—	
(I_{Source} = 20 mA, UC384XBV)		—	—	—	12.9	—	—	
(I_{Source} = 200 mA)		12	13.4	—	12	13.4	—	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA	$V_{OL(UVLO)}$	—	0.1	1.1	—	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	—	50	150	—	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	—	50	150	—	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Start-Up Threshold	V_{th}							V
UCX844B, BV		15	16	17	14.5	16	17.5	
UCX845B, BV		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn-On	$V_{CC(min)}$							V
UCX844B, BV		9.0	10	11	8.5	10	11.5	
UCX845B, BV		7.0	7.6	8.2	7.0	7.6	8.2	

NOTES: 4. This parameter is measured at the latch trip point with V_{FB} = 0 V.

5. Comparator gain is defined as: $A_V = \frac{\Delta V \text{ Output/Compensation}}{\Delta V \text{ Current Sense Input}}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25° C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	UC284XB			UC384XB, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
PWM SECTION								
Duty Cycle								%
Maximum (UC284XB, UC384XB)	$DC_{(max)}$	47	48	50	47	48	50	
(UC384XBV)		—	—	—	46	48	50	
Minimum	$DC_{(min)}$	—	—	0	—	—	0	
TOTAL DEVICE								
Power Supply Current	I_{CC}							mA
Start-Up (V_{CC} = 6.5 V for UCX845B, 14 V for UCX844B, BV)		—	0.3	0.5	—	0.3	0.5	
Operating (Note 2)		—	12	17	—	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	—	30	36	—	V

NOTES: 2. Adjust V_{CC} above the Start-Up threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for UC3844B, UC3845B; = −25°C for UC2844B, UC2845B; = −40°C for UC3844BV, UC3845BV
T_{high} = +70°C for UC3844B, UC3845B; = +85°C for UC2844B, UC2845B; = +105°C for UC3844BV, UC3845BV

Figure 1. Timing Resistor versus Oscillator Frequency

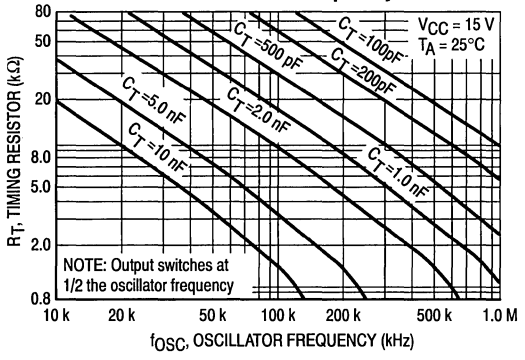


Figure 2. Output Dead-Time versus Oscillator Frequency

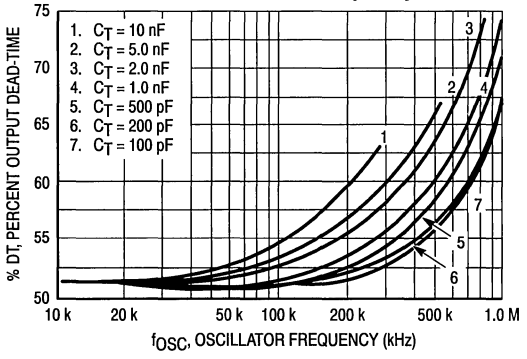


Figure 3. Error Amp Small Signal Transient Response

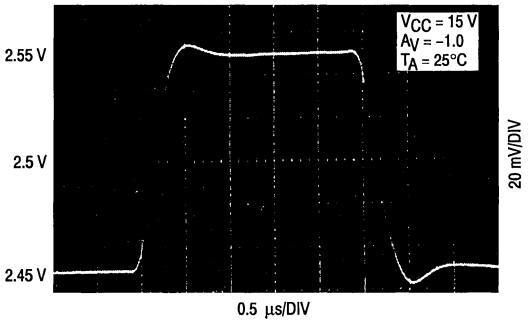
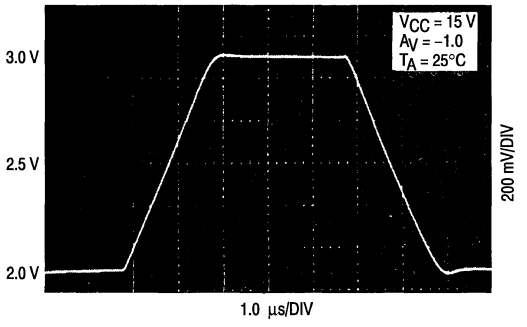


Figure 4. Error Amp Large Signal Transient Response



3

Figure 5. Error Amp Open-Loop Gain and Phase versus Frequency

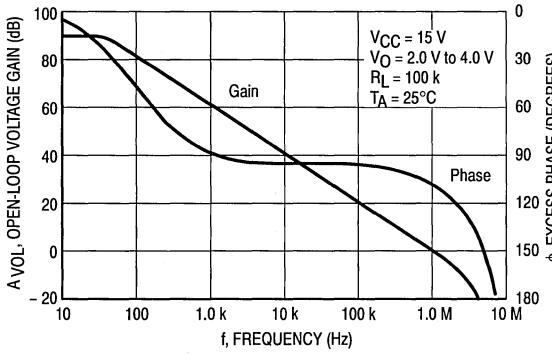


Figure 6. Current Sense Input Threshold versus Error Amp Output Voltage

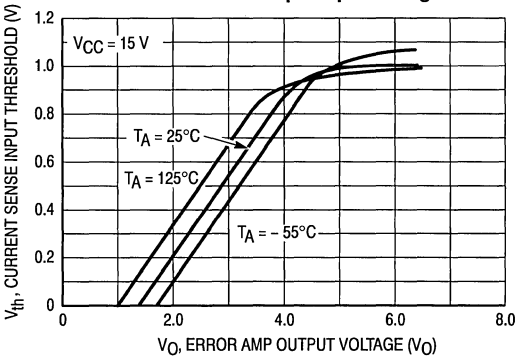


Figure 7. Reference Voltage Change versus Source Current

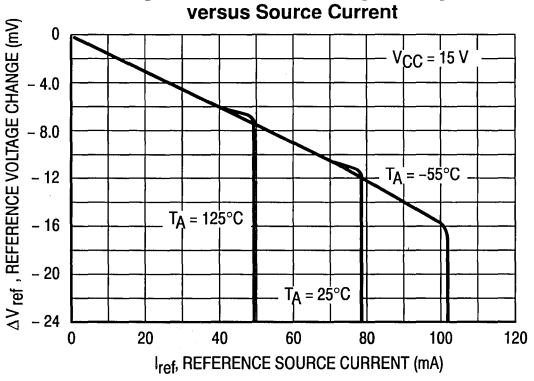


Figure 8. Reference Short Circuit Current versus Temperature

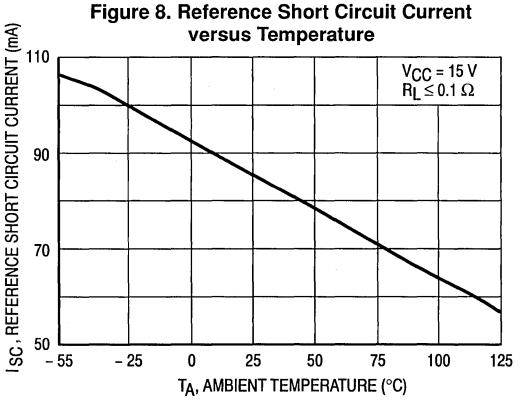


Figure 9. Reference Load Regulation

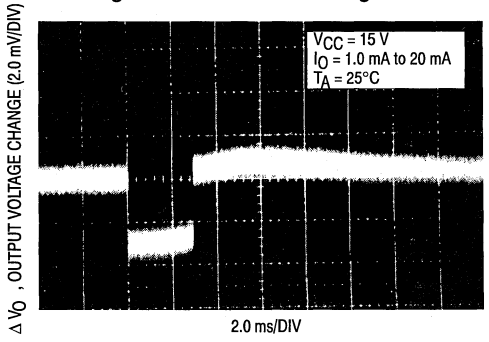


Figure 10. Reference Line Regulation

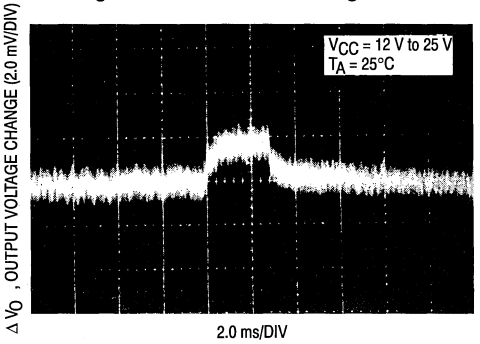


Figure 11. Output Saturation Voltage versus Load Current

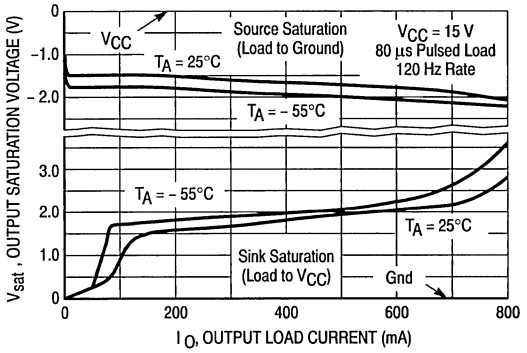


Figure 12. Output Waveform

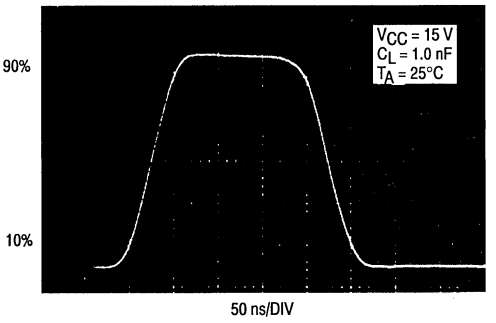


Figure 13. Output Cross Conduction

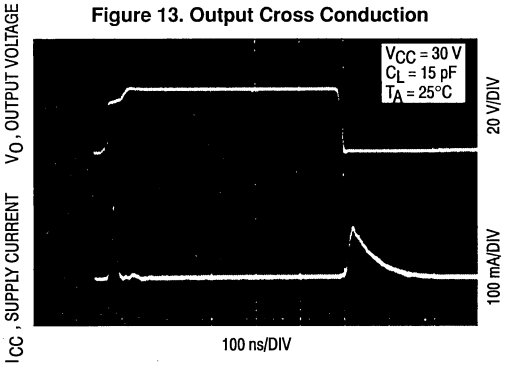
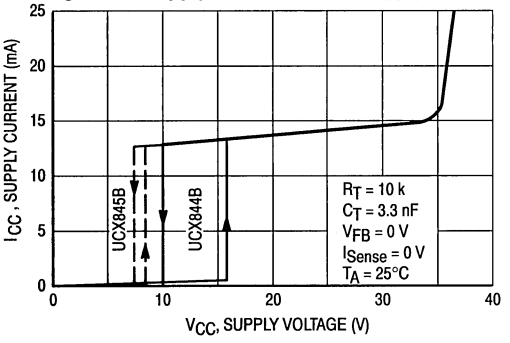


Figure 14. Supply Current versus Supply Voltage



PIN FUNCTION DESCRIPTION

Pin No.		Function	Description
8-Pin	14-Pin		
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Oscillator operation to 1.0 kHz is possible.
5		Gnd	This pin is the combined control circuitry and power ground.
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin. The output switches at one-half the oscillator frequency.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
	8	Power Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
	9	Gnd	This pin is the control circuitry ground return and is connected back to the power source ground.
	2,4,6,13	NC	No connection. These pins are not internally connected.

OPERATING DESCRIPTION

The UC3844B, UC3845B series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off-Line and DC-to-DC converter applications offering the designer a cost-effective solution with minimal external components. A representative block diagram is shown in Figure 15.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. An internal flip-flop has been incorporated in the UCX844/5B which blanks the output off every other clock cycle by holding one of the inputs of the NOR gate high. This in combination with the C_T discharge period yields output deadtimes programmable from 50% to 70%. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated to within ±6% at 50 kHz. Also, because of industry trends moving the UC384X into higher and higher frequency applications, the UC384XB is guaranteed to within ±10% at 250 kHz.

In many noise-sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 17. For reliable locking, the free-running oscillator frequency should be set about 10% less than the clock frequency. A method for multi-unit synchronization is shown in Figure 18. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved to realize output deadtimes of greater than 70%.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 5). The non-inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is –2.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 28). The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Figures 20, 21). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3844B, UC3845B operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground-referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability (refer to Figure 23).

Figure 15. Representative Block Diagram

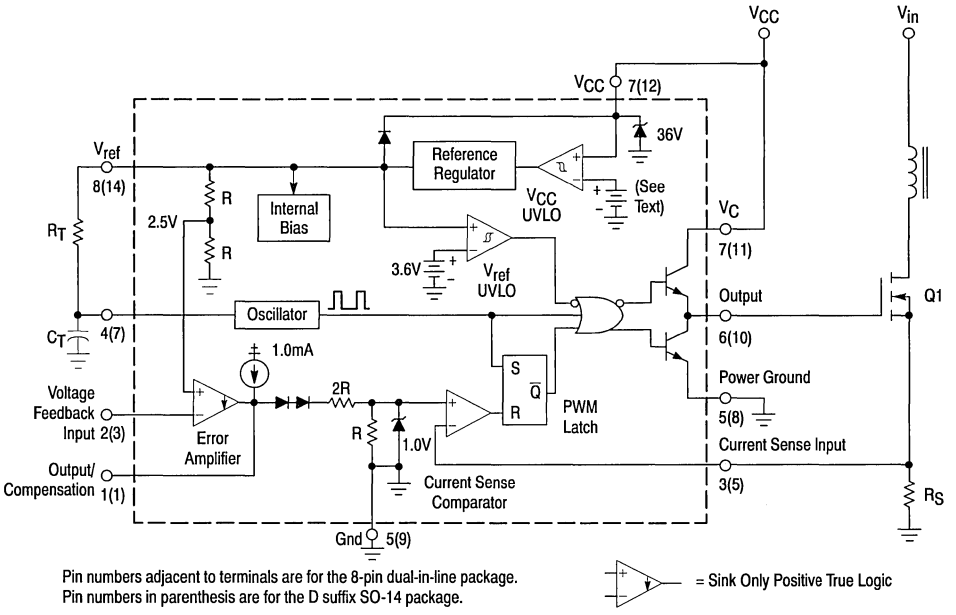
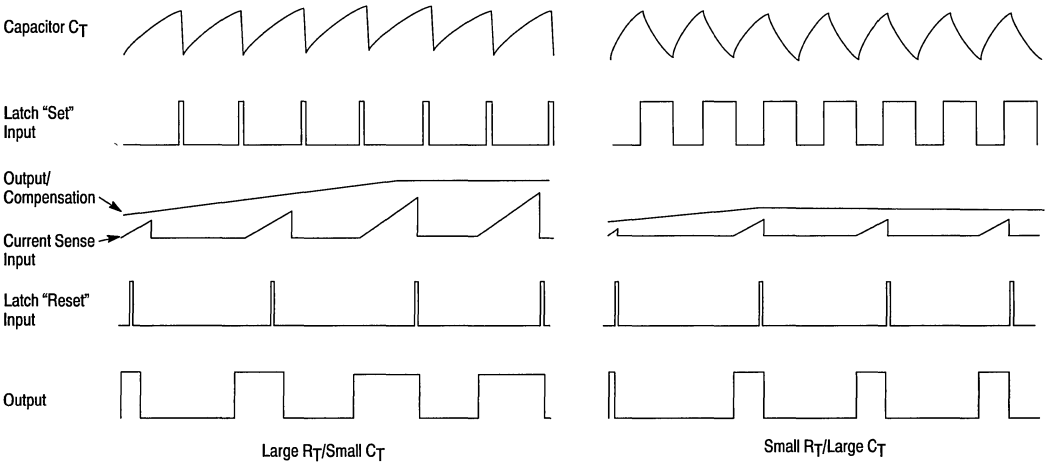


Figure 16. Timing Diagram



Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX844B, and 8.4 V/7.6 V for the UCX845B. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low start-up current of the UCX844B makes it ideally suited in off-line converter applications where efficient bootstrap start-up techniques are required (Figure 29). The UCX845B is intended for lower voltage DC-to-DC converter applications. A 36 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system start-up. The minimum operating voltage for the UCX844B is 11 V and 8.2 V for the UCX845B.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull-down resistor.

The SO-14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 22 shows proper power and control ground connections in a current-sensing power MOSFET application.

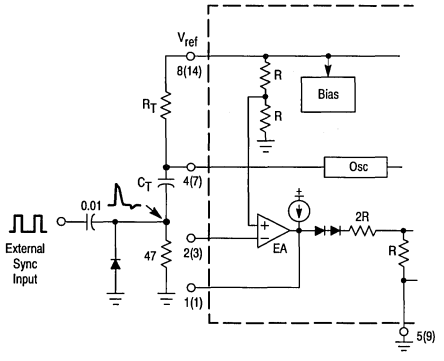
Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the UC284XB, and ±2.0% on the UC384XB. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short-circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

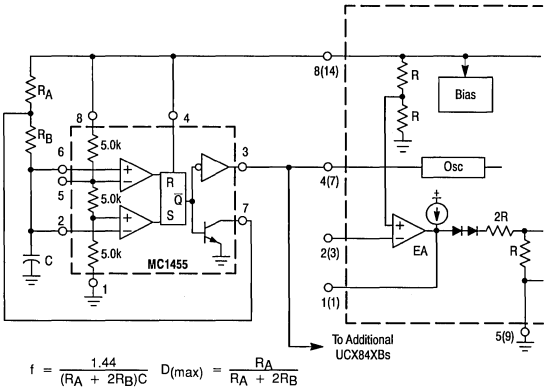
Do not attempt to construct the converter on wire-wrap or plug-in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse-width jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low-current signal and high-current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 µF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise-generating components.

Figure 17. External Clock Synchronization



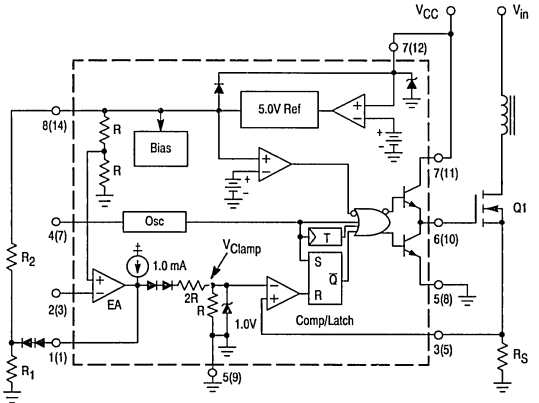
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

Figure 18. External Duty Cycle Clamp and Multi-Unit Synchronization



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D(max) = \frac{R_A}{R_A + 2R_B}$$

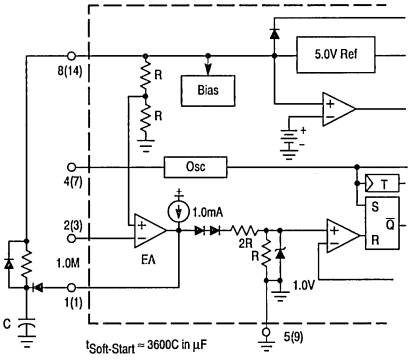
Figure 19. Adjustable Reduction of Clamp Level



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} + 0.33 \times 10^{-3} \left(\frac{R_1 R_2}{R_1 + R_2}\right) \quad \text{Where: } 0 \le V_{Clamp} \le 1.0\ V$$

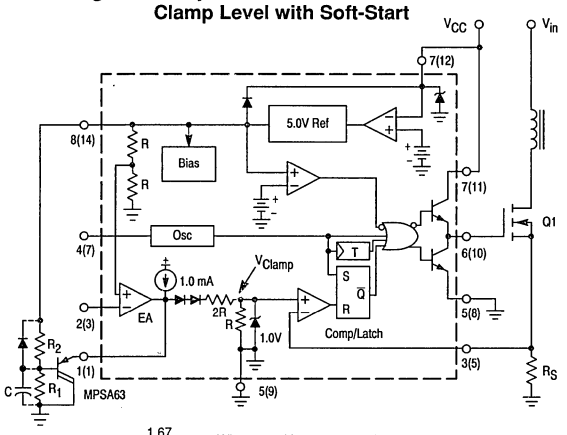
$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Figure 20. Soft-Start Circuit



$t_{Soft\text{-}Start} \approx 3600C$ in µF

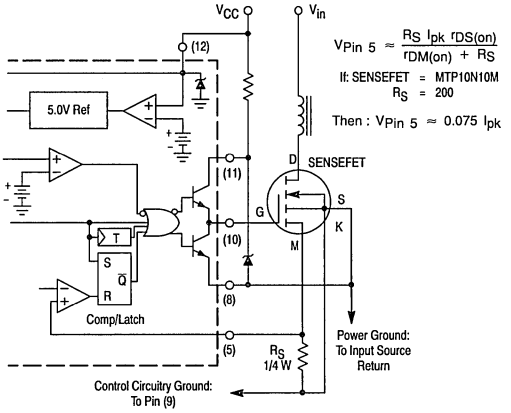
Figure 21. Adjustable Buffered Reduction of Clamp Level with Soft-Start



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} \quad \text{Where: } 0 \le V_{Clamp} \le 1.0\ V$$

$$t_{Soft\text{-}Start} = -\ln\left[1 - \frac{V_C}{3V_{Clamp}}\right] C \frac{R_1 R_2}{R_1 + R_2} \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Figure 22. Current Sensing Power MOSFET



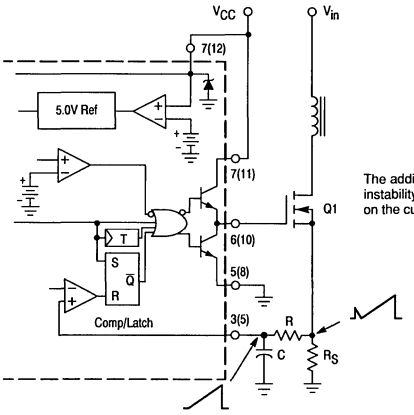
$$V_{Pin\ 5} \approx \frac{R_S\ I_{pk}\ r_{DS(on)}}{r_{DM(on)} + R_S}$$

If: SENSEFET = MTP10N10M
R_S = 200

Then : $V_{Pin\ 5} \approx 0.075\ I_{pk}$

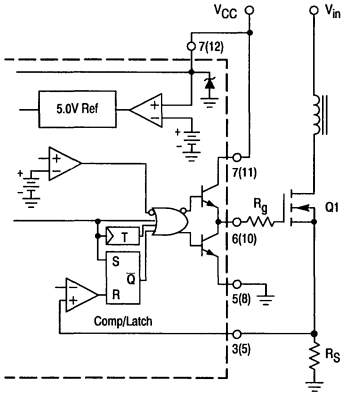
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over-current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 19 and 21.

Figure 23. Current Waveform Spike Suppression



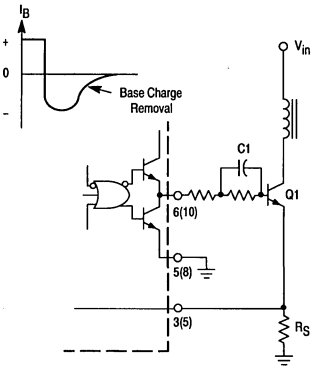
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 24. MOSFET Parasitic Oscillations



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

Figure 25. Bipolar Transistor Drive



The totem pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1.

Figure 26. Isolated MOSFET Drive

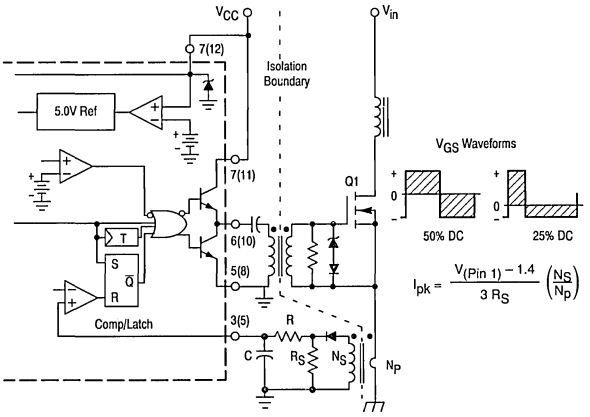
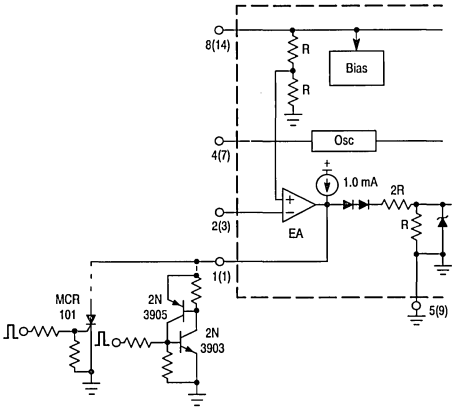
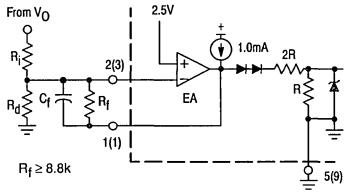


Figure 27. Latched Shutdown

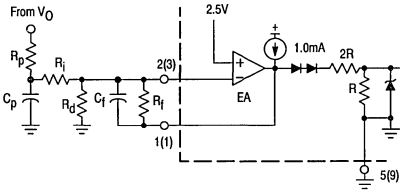


The MCR101 SCR must be selected for a holding of < 0.5 mA @ $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

Figure 28. Error Amplifier Compensation

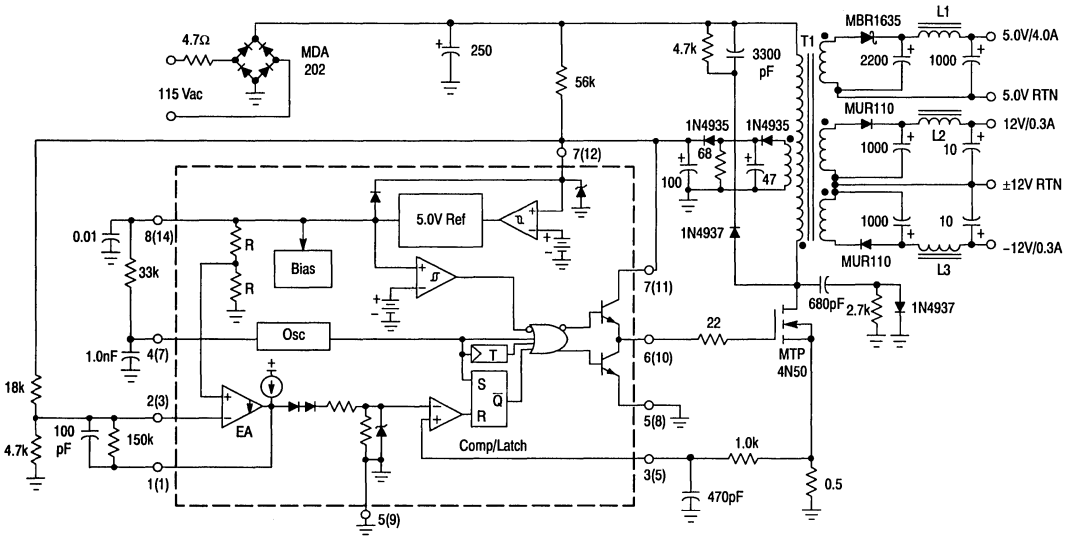


Error Amp compensation circuit for stabilizing any current mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current mode boost and flyback topologies operating with continuous inductor current.

Figure 29. 27 W Off-Line Flyback Regulator



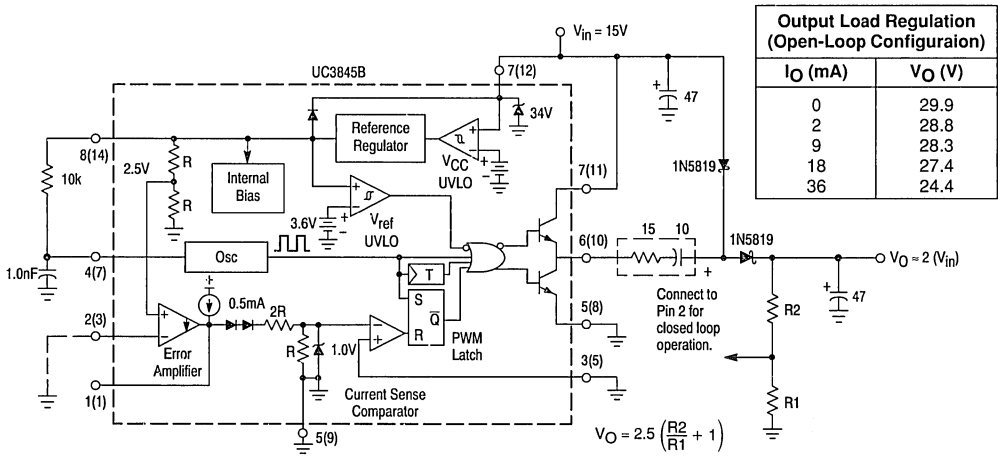
T1 — Primary: 45 Turns #26 AWG
Secondary ±12 V: 9 Turns #30 AWG (2 Strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands) #26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EC35-3C8
Bobbin: Ferroxcube EC35PCB1
Gap: ≈ 0.10" for a primary inductance of 1.0 mH

L1 — 15 μH at 5.0 A, Coilcraft Z7156
L2, L3 — 25 μH at 5.0 A, Coilcraft Z7157

Line Regulation: 5.0 V ±12 V	V_{in} = 95 Vac to 130 Vac	Δ = 50 mV or ±0.5% Δ = 24 mV or ±0.1%
Load Regulation: 5.0 V ±12 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 300 mV or ±3.0% Δ = 60 mV or ±0.25%
Output Ripple: 5.0 V ±12 V	V_{in} = 115 Vac	40 mV_{p-p} 80 mV_{p-p}
Efficiency	V_{in} = 115 Vac	70%

All outputs are at nominal load currents unless otherwise noted.

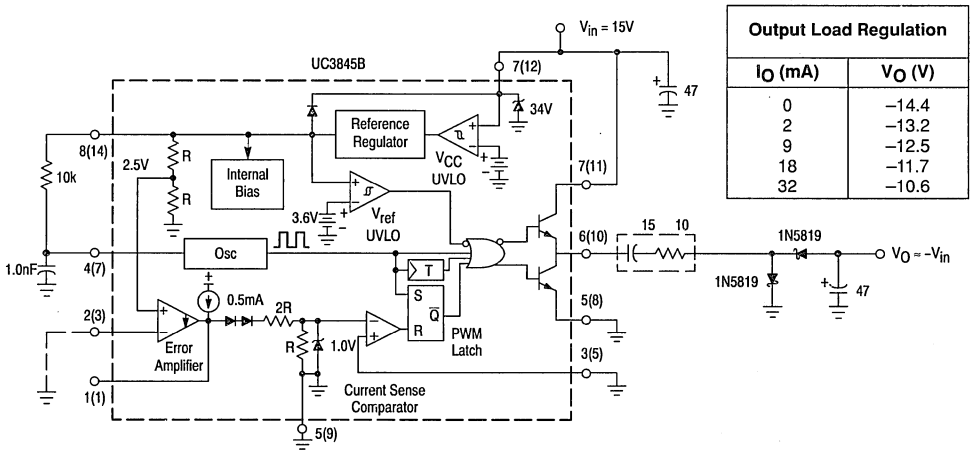
Figure 30. Step-Up Charge Pump Converter



Output Load Regulation (Open-Loop Configuraion)	
I_O (mA)	V_O (V)
0	29.9
2	28.8
9	28.3
18	27.4
36	24.4

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A. An additional series resistor may be required when using tantalum or other low ESR capacitors. The converter's output can provide excellent line and load regulation by connecting the R2/R1 resistor divider as shown.

Figure 31. Voltage-Inverting Charge Pump Converter



Output Load Regulation	
I_O (mA)	V_O (V)
0	−14.4
2	−13.2
9	−12.5
18	−11.7
32	−10.6

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A.
An additional series resistor may be required when using tantalum or other low ESR capacitors.

μA78S40

3

Universal Switching Regulator Subsystem

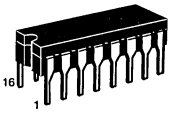
UNIVERSAL SWITCHING REGULATOR SUBSYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT

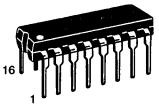
The μA78S40 is a switching regulator subsystem, consisting of a temperature compensated voltage reference, controlled-duty cycle oscillator with an active current limit circuit, comparator, high-current and high-voltage output switch, capable of 1.5 A and 40 V, pinned-out power diode and an uncommitted operational amplifier, which can be powered up or down independent of the IC supply. The switching output can drive external NPN or PNP transistors when voltages greater the 40 V, or currents in excess of 1.5 A, are required. Some of the features are wide-supply voltage range, low standby current, high efficiency and low drift. The μA78S40 is available in commercial (0° to + 70°C), automotive (–40° to + 85°C), and military (–55° to +125°C) temperature ranges.

Some of the applications include use in step-up, step-down, and inverting regulators, with extremely good results obtained in battery-operated systems.

- Output Adjustable from 1.25 V to 40 V
- Peak Output Current of 1.5 A Without External Transistor
- 80 dB Line and Load Regulation
- Operation from 2.5 V to 40 V Supply
- Low Standby Current Drain
- High Gain, High Output Current, Uncommitted Op Amp

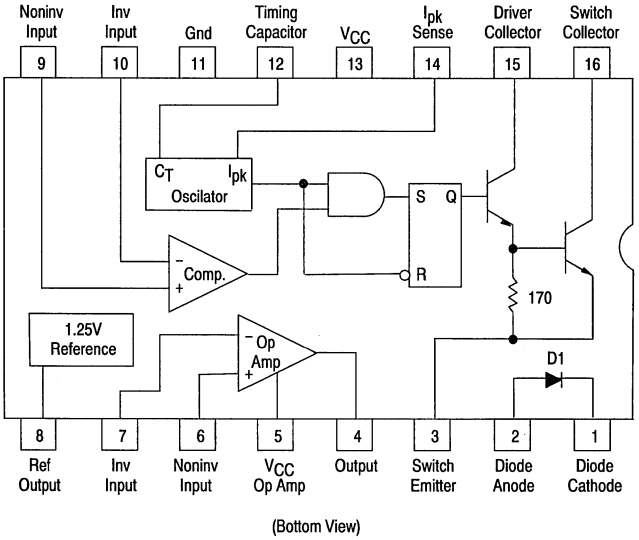


D SUFFIX
CERAMIC PACKAGE
CASE 620



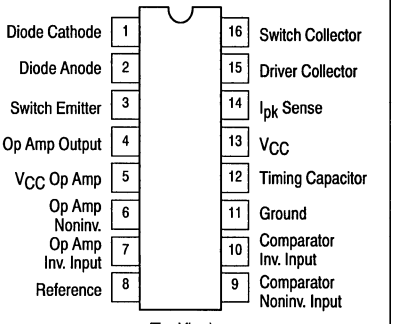
P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



(Bottom View)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
μA78S40PC	0° to + 70°C	Plastic
μA78S40PV	–40° to + 85°C	Plastic
μA78S40DC	0° to + 70°C	Ceramic
μA78S40DM	–55° to +125°C	Ceramic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Op Amp Power Supply Voltage	V_{CC} (Op Amp)	40	V
Common Mode Input Range (Comparator and Op Amp)	V_{ICR}	–0.3 to V_{CC}	V
Differential Input Voltage (Note 2)	V_{ID}	± 30	V
Output Short Circuit Duration (Op Amp)	—	Continuous	—
Reference Output Current	I_{ref}	10	mA
Voltage from Switch Collectors to Gnd	—	40	V
Voltage from Switch Emitters to Gnd	—	40	V
Voltage from Switch Collectors to Emitter	—	40	V
Voltage from Power Diode to Gnd	—	40	V
Reverse-Power Diode Voltage	V_{DR}	40	V
Current through Power Switch	I_{SW}	1.5	A
Current through Power Diode	I_D	1.5	A
Power Dissipation and Thermal Characteristics: Plastic Package (T_A = + 25°C) Derate above + 25°C (Note 1) Ceramic Package (T_A = 25°C) Derate above + 25°C (Note 1)	 P_D $1/R_{\theta JA}$ P_D $1/R_{\theta JA}$	 1500 14 1000 8.0	 mW mW/°C mW mW/°C
Storage Temperature Range	T_{stg}	–65 to + 150	°C
Operating Temperature Range μA78S40M μA78S40V μA78S40C	T_A	 –55 to +125 –40 to +85 0 to +70	°C

NOTES: 1. T_{low} = –55° for μA78S40DM = –40° for μA78S40PV = 0° for μA78S40DC and μA78S40PC; T_{high} = +125° for μA78S40DM = +85° for μA78S40PV = +70° for μA78S40DC and μA78S40PC

2. For supply voltages less than 30 V the maximum differential input voltage (Error Amp and Op Amp) is equal to the supply voltage.

ELECTRICAL CHARACTERICISTICS (V_{CC} = V_{CC} (Op Amp) 5.0 V, T_A = T_{low} to T_{high}, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
GENERAL					
Supply Voltage	V_{CC}	2.5	—	40	V
Supply Current (Op Amp V_{CC}, disconnected) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{CC}	 — —	 1.8 2.3	 3.5 5.0	mA
Supply Current (Op Amp V_{CC}, connected) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{CC}	 — —	 — —	 4.0 5.5	mA
REFERENCE					
Reference Voltage (I_{ref} = 1.0 mA)	V_{ref}	1.180	1.245	1.310	V
Reference Voltage Line Regulation (3.0 V ≤ V_{CC} ≤ 40 V, I_{ref} = 1.0 mA, T_A = 25°C)	Reg_{line}	—	0.04	0.2	mV/V
Reference Voltage Load Regulation (1.0 mA ≤ I_{ref} ≤ 10 mA, T_A = 25°C)	Reg_{load}	—	0.2	0.5	mV/mA

ELECTRICAL CHARACTERICISTICS (V_{CC} = V_{CC} (Op Amp) 5.0 V, T_A = T_{low} to T_{high}, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Charging Current (T_A = 25°C) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{chg}	 20 20	 — —	 50 70	μA
Discharging Current (T_A = 25°C) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{dis}	 150 150	 — —	 250 350	μA
Oscillator Voltage Swing (T_A = 25°C) (V_{CC} = 5.0 V)	V_{osc}	—	0.5	—	V
Ratio of Charge/Discharge Time	t_{chg}/t_{dis}	—	6.0	—	—
CURRENT LIMIT					
Current-Limit Sense Voltage (T_A = 25°C) (V_{CC} – V_{Ipk} Sense)	V_{CLS}	250	—	350	mV
OUTPUT SWITCH					
Output Saturation Voltage 1 (I_{SW} = 1.0 A, Pin 15 tied to Pin 16)	V_{sat1}	—	0.93	1.3	V
Output Saturation Voltage 2 (I_{SW} = 1.0 A, I_{15} = 50 mA)	V_{sat2}	—	0.5	0.7	V
Output Transistor Current Gain (T_A = 25°C) (I_C = 1.0 A, V_{CE} = 5.0 V)	h_{FE}	—	70	—	—
Output Leakage Current (T_A = 25°C) (V_{CE} = 40 V)	$I_{C(off)}$	—	10	—	nA
POWER DIODE					
Forward Voltage Drop (I_D = 1.0 A)	V_D	—	1.25	1.5	V
Diode Leakage Current (T_A = 25°C) (V_{DR} = 40 V)	I_{DR}	—	10	—	nA
COMPARATOR					
Input Offset Voltage (V_{CM} = V_{ref})	V_{IO}	—	1.5	15	mV
Input Bias Current (V_{CM} = V_{ref})	I_{IB}	—	35	200	nA
Input Offset Current (V_{CM} = V_{ref})	I_{IO}	—	5.0	75	nA
Common Mode Voltage Range (T_A = 25°C)	V_{ICR}	0	—	V_{CC} – 2.0	V
Power-Supply Rejection Ration (T_A = 25°C) (3.0 ≤ V_{CC} ≤ 40 V)	PSRR	70	96	—	dB
OUTPUT OPERATION AMPLIFIER					
Input Offset Voltage (V_{CM} = 2.5 V)	V_{IO}	—	4.0	15	mV
Input Bias Current (V_{CM} = 2.5 V)	I_{IB}	—	30	200	nA
Input Offset Current (V_{CM} = 2.5 V)	I_{IO}	—	5.0	75	nA
Voltage Gain + (T_A = 25°C) (R_L = 2.0 kΩ to Gnd, 1.0 V ≤ V_O ≤ 2.5 V)	A_{VOL+}	25	250	—	V/mV
Voltage Gain – (T_A = 25°C) (R_L = 2.0 kΩ to V_{CC} (Op Amp), 1.0 V ≤ V_O ≤ 2.5 V)	A_{VOL-}	25	250	—	V/mV
Common Mode Voltage Range (T_A = 25°C)	V_{ICR}	0	—	V_{CC} – 2.0	V
Common Mode Rejection Ratio (T_A = 25°C) (V_{CM} = 0 V to 3.0 V)	CMRR	76	100	—	dB
Power-Supply Rejection Ratio (T_A = 25°C) (3.0 V ≤ V_{CC} (Op Amp) ≤ 40 V)	PSRR	76	100	—	dB
Output Source Current (T_A = 25°C)	I_{Source}	75	150	—	mA
Output Sink Current (T_A = 25°C)	I_{Sink}	10	35	—	mA
Slew Rate (T_A = 25°C)	SR	—	0.6	—	V/μs
Output Low Voltage (T_A = 25°C, I_L = –5.0 mA)	V_{OL}	—	—	1.0	V
Output High Voltage (T_A = 25°C, I_L = 50 mA)	V_{OH}	V_{CC}(Op Amp) – 3.0	—	—	V

Figure 1. Output Switch On/Off Time versus Oscillator Timing Capacitor

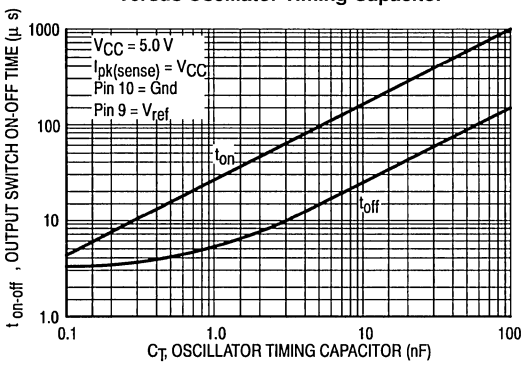


Figure 2. Standby Supply Current versus Supply Voltage

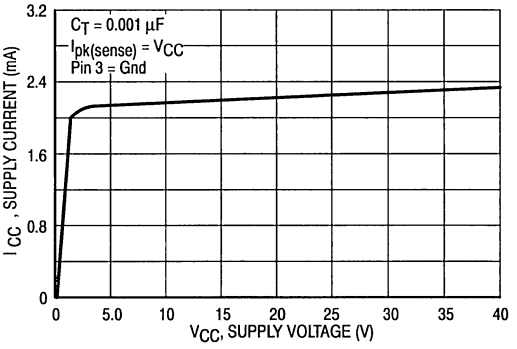


Figure 3. Emitter- Follower Configuration Output Switch Saturation Voltage versus Emitter Current

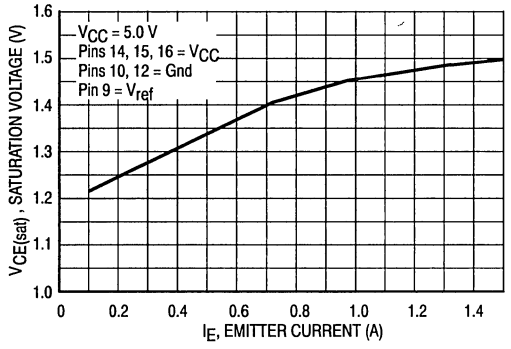


Figure 4. Common-Emitter Configuration Output Switch Saturation Voltage versus Collector Current

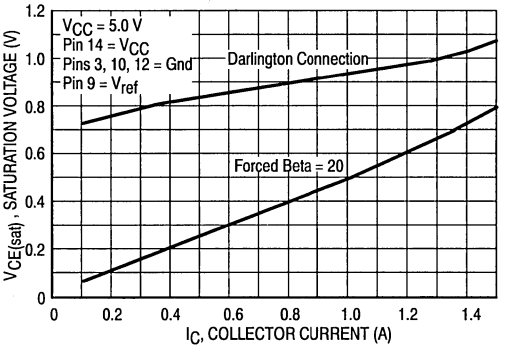


Figure 5. Step-Down Converter

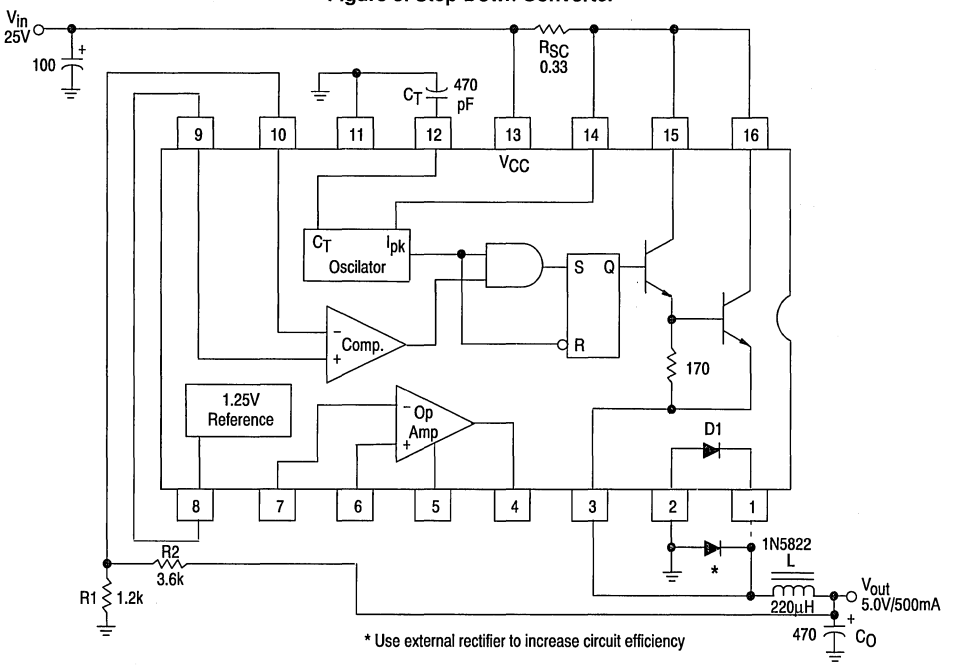


Figure 6. Step-Up Converter

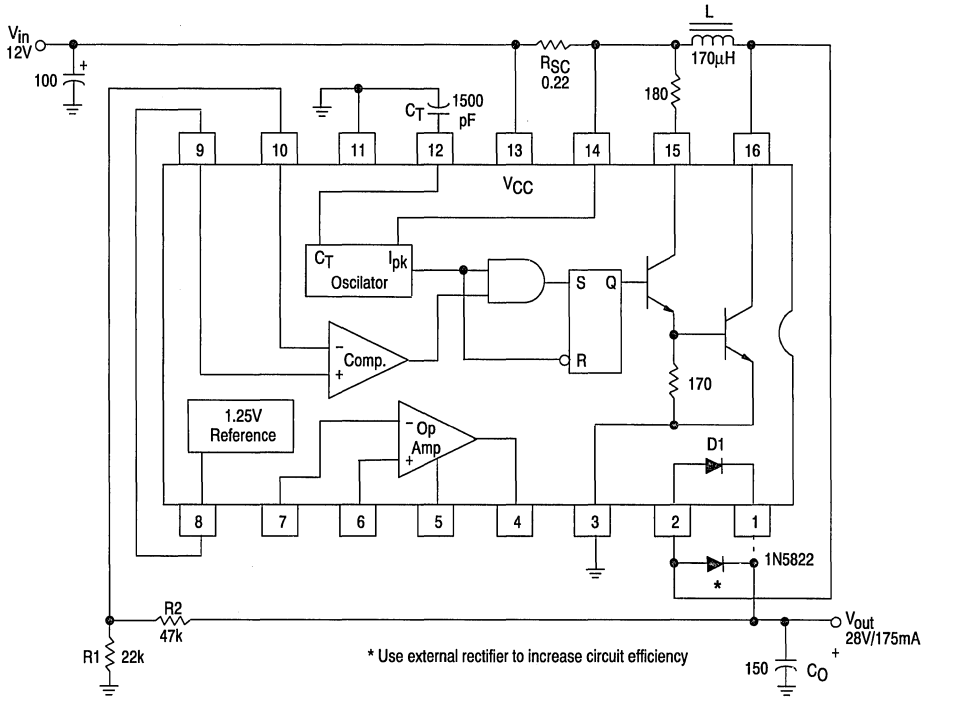
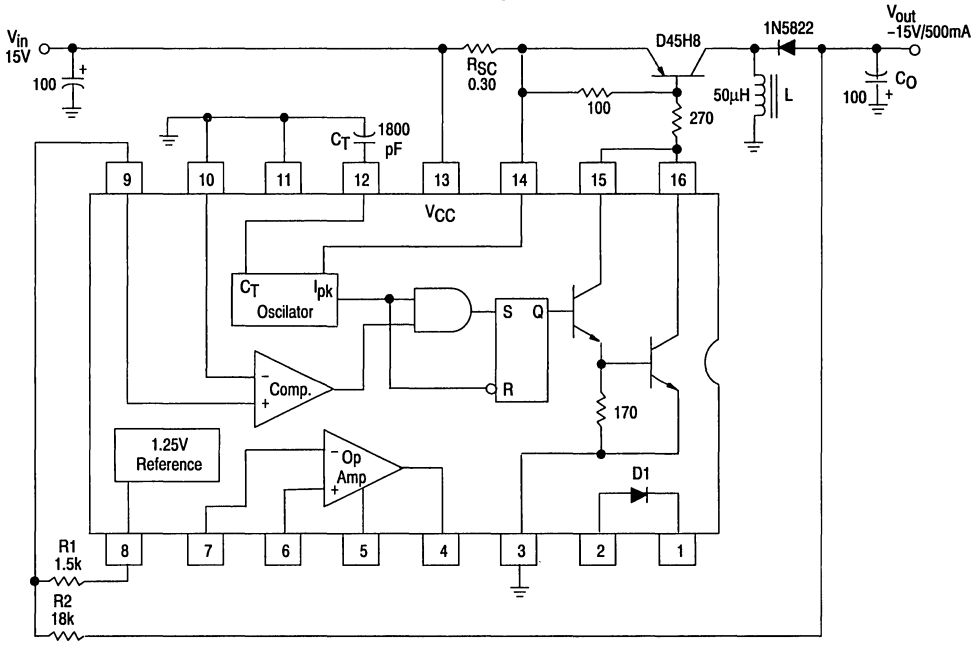


Figure 7. Inverting Converter



Design Formula Table

Calculation	Step-Down	Step-Up	Inverting
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{V_{out} - V_F}{V_{in(min)}} \frac{V_{in(min)}}{V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat}}$
$(t_{on} + t_{off})$ max	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$	$\frac{1}{f_{min}}$
C_T	$4 \times 10^5 t_{on}$	$4 \times 10^5 t_{on}$	$4 \times 10^5 t_{on}$
$I_{pk(switch)}$	$2 I_{out(max)}$	$2 I_{out(max)} \left(\frac{t_{on} - t_{off}}{t_{off}}\right)$	$2 I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}}\right)$
R_{SC}	$\frac{0.33}{I_{pk(switch)}}$	$\frac{0.33}{I_{pk(switch)}}$	$\frac{0.33}{I_{pk(switch)}}$
$L_{(min)}$	$\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$
C_O	$\frac{I_{pk(switch)} (t_{on} + t_{off})}{8 V_{ripple(p-p)}}$	$\approx \frac{I_{out} t_{on}}{V_{ripple}}$	$\approx \frac{I_{out} t_{on}}{V_{ripple}}$

V_{sat} = Saturation voltage of the output switch. V_F = Forward voltage drop of the ringback rectifier.

The following power supply characteristics must be chosen:

V_{in} — Nominal input voltage. If this voltage is not constant, then use $V_{in(max)}$ for step-down and $V_{in(min)}$ for step-up and inverting convertor.

V_{out} — Desired output voltage: $V_{out} = 1.25 \left(1 + \frac{R_2}{R_1}\right)$ for step-down and step-up: $V_{out} = \frac{1.25 R_2}{R_1}$ for inverting.

I_{out} — Desired output current.

f_{min} — Minimum desired output switching frequency at the selected values for V_{in} and I_O.

$V_{ripple(p-p)}$ — Desired peak-to-peak output ripple voltage. In practice, the calculated value will need to be increased due to the capacitor's equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly effect the line and load regulation.

See Application Note AN920R2 for further information

Addendum
Linear & Switching Voltage Regulator Applications Information

In Brief . . .

In most electronic systems, voltage regulation is required for various functions. Today's complex electronic systems are requiring greater regulating performance, higher efficiency and lower parts count. Present integrated circuit and power package technology have produced IC voltage regulators which can ease the task of regulated power supply design, provide the performance required and remain cost effective. Available in a growing variety, Motorola offers a wide range of regulator products from fixed and adjustable voltage types to special-function and switching regulator control ICs.

This handbook describes Motorola's voltage regulator products and provides information on applying these products. Basic Linear regulator theory and switching regulator topologies have been included along with practical design examples. Other relevant topics include trade-offs of Linear versus switching regulators, series pass elements for Linear regulators, switching regulator component design considerations, heatsinking, construction and layout, power supply supervision and protection, and reliability.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

SECTION 1
BASIC LINEAR REGULATOR THEORY

3

A. The IC Voltage Regulator

The basic functional block diagram of an integrated circuit voltage regulator is shown in Figure 1-1. It consists of a stable reference, whose output voltage is V_{ref}, and a high gain error amplifier. The output voltage (V_O), is equal to or a multiple of V_{ref}. The regulator will tend to keep V_O constant by sensing any changes in V_O and trying to return it to its original value. Therefore, the ideal voltage regulator could be considered a voltage source with a constant output voltage. However, in practice the IC regulator is better represented by the model shown in Figure 1-2.

In this figure, the regulator is modeled as a voltage source with a positive output impedance (Z_O). The value of the voltage source (V) is not constant; instead it varies with changes in supply voltage (V_{CC}) and with changes in IC junction temperature (T_J) induced by changes in ambient temperature and power dissipation. Also, the regulator output voltage (V_O) is affected by the voltage drop across Z_O, caused by the output current (I_O). In the following text, the reference and amplifier sections will be described, and their contributions to the changes in the output voltage analyzed.

B. The Voltage Reference

Naturally, the major requirement for the reference is that it be stable; variations in supply voltage or junction temperature should have little or no effect on the value of the reference voltage (V_{ref}).

The Zener Diode Reference

The simplest form of a voltage reference is shown in Figure 1-3a. It consists of a resistor and a zener diode. The zener voltage (V_Z) is used as the reference voltage. In order to determine V_Z, consider Figure 1-3b. The zener diode (VR1) of Figure 1-3a has been replaced with its equivalent circuit model and the value of V_Z is therefore given by (at a constant junction temperature):

$$V_Z = V_{BZ} + I_Z Z_Z = V_{BZ} + \left(\frac{V_{CC} - V_{BZ}}{R + Z_Z}\right) Z_Z \qquad (1)$$

where: V_{BZ} = zener breakdown voltage
I_Z = zener current
Z_Z = zener impedance at I_Z.

Note that changes in the supply voltage give rise to changes in the zener current, thereby changing the value of the reference voltage (V_Z).

Figure 1-1. Voltage Regulator Functional Block Diagram

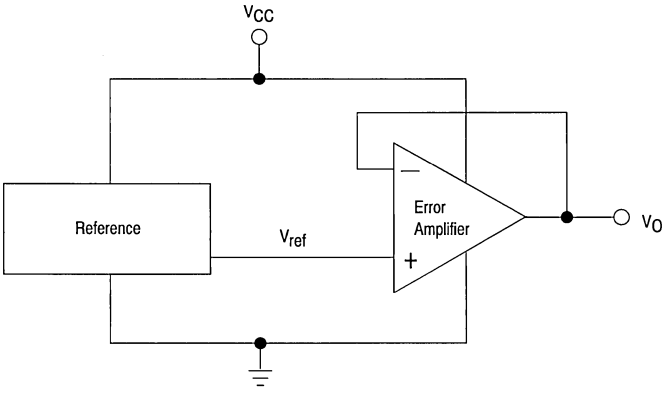


Figure 1-2. Voltage Regulator Equivalent Circuit Model

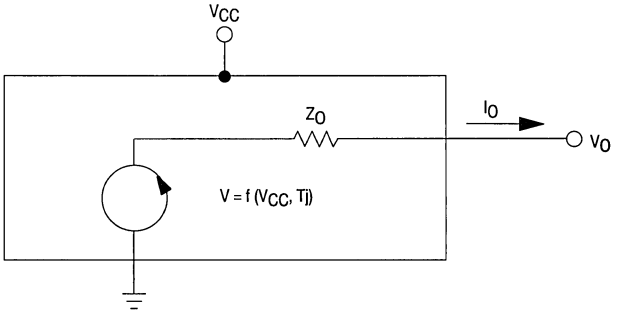
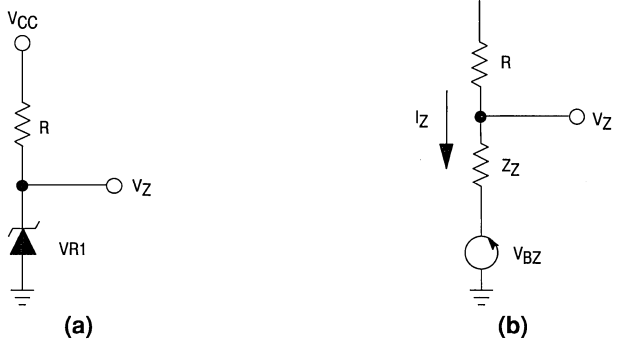


Figure 1-3. Zoner Diode Reference



The Constant Current — Zener Reference

The effect of zener impedance can be minimized by driving the zener diode with a constant current as shown in Figure 1-4. The value of the zener current is largely independent of V_{CC} and is given by:

$$I_Z = \frac{V_{BEQ1}}{R_{SC}} \quad (2)$$

where: V_{BEQ1} = base-emitter voltage of Q1.

3

This gives a reference voltage of:

$$V_{ref} = V_Z + V_{BEQ1} = V_{BZ} + I_Z Z_Z + V_{BEQ1} \quad (3)$$

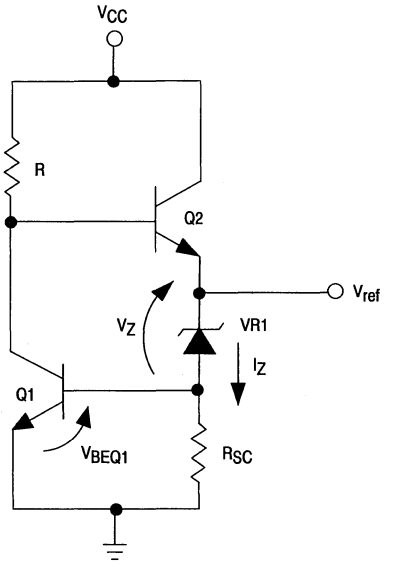
where I_Z is constant and given by equation 2.

The reference voltage (about 7.0 V) of this configuration is therefore largely independent of supply voltage variations. This configuration has the additional benefit of better temperature stability than that of a simple resistor-zener reference.

Referring back to Figure 1-3a, it can be seen that the reference voltage temperature stability is equal to that of the zener diode, VR1. The stability of zener diodes used in most integrated circuitry is about + 2.2 mV/°C or ≃ 0.04%/°C (for a 6.2 V zener). If the junction temperature varies 100°C, the zener or reference voltage would vary 4%. A variation this large is usually unacceptable.

However, the circuit of Figure 1-4 does not have this drawback. Here the positive 2.2 mV/°C temperature coefficient (TC) of the zener diode is offset by the negative 2.2 mV/°C TC of the V_{BE} of Q1. This results in a reference voltage with very stable temperature characteristics.

Figure 1-4. Constant Current — Zener Reference



The Bandgap Reference

Although very stable, the circuit of Figure 1-4 does have a disadvantage in that it requires a supply voltage of 9.0 V or more. Another type of stable reference which requires only a few volts to operate was described by Widlar[1] and is shown in Figure 1-5. In this circuit V_{ref} is given by:

$$V_{ref} = V_{BEQ3} + I_2R_2 \tag{4}$$

where: $$I_2 = \frac{V_{BEQ1} - V_{BEQ2}}{R_1}$$ (neglecting base currents)

The change in V_{ref} with junction temperature is given by:

$$\Delta V_{ref} = \Delta V_{BE3} + \left\{\frac{\Delta V_{BEQ1} - \Delta V_{BEQ2}}{R_1}\right\} R_2 \tag{5}$$

It can be shown that,

$$\Delta V_{BEQ1} = \Delta T_J K \ln I_1 \tag{6}$$

and, $$\Delta V_{BEQ2} = \Delta T_J K \ln I_2 \tag{7}$$

where: K = a constant

ΔT_J = change in junction temperature

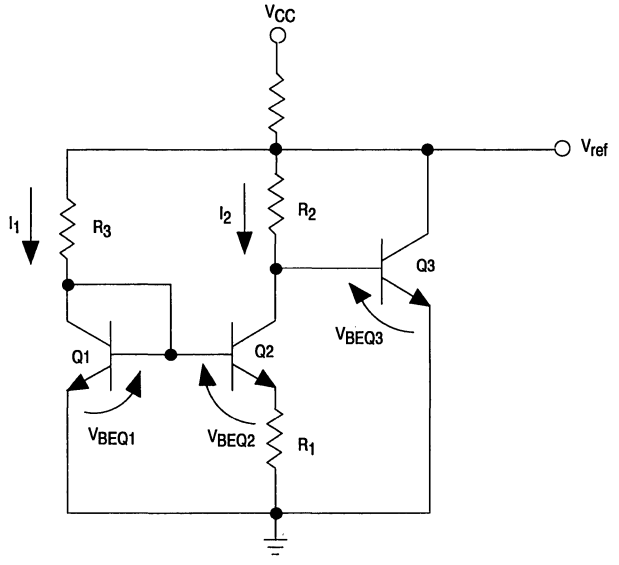
and, $I_1 > I_2$

Combining (5), (6), and (7)

$$\Delta V_{ref} = \Delta V_{BEQ3} + \Delta T_J K \left(\frac{R_2}{R_1}\right) \ln \frac{I_1}{I_2} \tag{8}$$

Since ΔV_{BEQ3} is negative, and with $I_1 > I_2$, $\ln I_1/I_2$ is positive, the net change in V_{ref} with temperature variations can be made to equal zero by appropriately selecting the values of I_1, R_1, and R_2.

Figure 1-5. Bandgap Reference



C. The Error Amplifier

Given a stable reference, the error amplifier becomes the determining factor in integrated circuit voltage regulator performance. Figure 1-6 shows a typical differential error amplifier in a voltage regulator configuration. With a constant supply voltage (V_{CC}) and junction temperature, the output voltage is given by:

$$V_O = A_{VOL}\, \upsilon_i - Z_{OL}\, I_O = A_{VOL}\, \{(V_{ref} \pm V_{IO}) - V_O\, \beta\} - Z_{OL}\, I_O \qquad (9)$$

3

where: A_{VOL} = amplifier open-loop gain

V_{IO} = input offset voltage

Z_{OL} = open-loop output impedance

$\beta = \dfrac{R_1}{R_1 + R_2}$ = feedback ratio (β is always ≤ 1)

I_O = output current

υ_i = true differential input voltage

Manipulating (9)

$$V_O = \frac{(V_{ref} \pm V_{IO}) - \dfrac{Z_{OL}}{A_{VOL}}\, I_O}{\beta + \dfrac{1}{A_{VOL}}} \qquad (10)$$

Note that if the amplifier open-loop gain is infinite, this expression reduces to:

$$V_O = \frac{1}{\beta}\, (V_{ref} \pm V_{IO}) = (V_{ref} \pm V_{IO})\, (1 + \frac{R_2}{R_1}) \qquad (11)$$

The output voltage can thus be set any value equal to or greater than ($V_{ref} \pm V_{IO}$). Note also that if A_{VOL} is not infinite, with constant output current (a non-varying output load), the output voltage can still be "tweaked in" by varying R_1 and R_2, even though V_O will not exactly equal that given by equation 11.

Assuming a stable reference and a finite value of A_{VOL}, inaccuracy of the output voltage can be traced to the following amplifier characteristics:

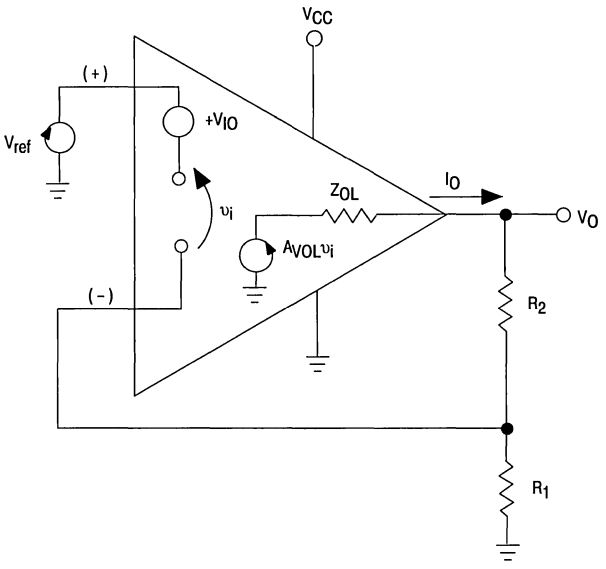
1. Amplifier Input Offset Voltage Drift

The input transistors of integrated circuit amplifiers are usually not perfectly matched. As in operational amplifiers, this is expressed in terms of an input offset voltage (V_{IO}). At a given temperature, this effect can be nulled out of the desired output voltage by adjusting V_{ref} or $1/\beta$. However, V_{IO} drifts with temperature, typically $\pm 5.0\ \mu V/°C$ to $+15\ \mu V/°C$, causing a proportional change in the output voltage. Closer matching of the internal amplifier input transistors minimizes this effect, as does selecting a feedback ratio (β) to be close to unity.

2. Amplifier Power Supply Sensitivity

Changes in regulator output voltage due to power supply voltage variations can be attributed to two amplifier performance parameters: power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR). In modern integrated circuit regulator amplifiers, the utilization of constant current sources gives such large values of PSRR that this effect on V_O can usually be neglected. However, supply voltage changes can affect the output voltage since these changes appear as common mode voltage changes, and they are best measured by the CMRR.

Figure 1-6. Typical Voltage Regulator Configuration



The definition of common mode voltage, V_{CM}, illustrated by Figure 1-7a, is:

$$V_{CM} = \left(\frac{V_1 + V_2}{2}\right) - \left(\frac{V_+ + V_-}{2}\right) \quad (12)$$

where: V_1 = voltage on amplifier noninverting input
V_2 = voltage on amplifier inverting input
$V+$ = positive supply voltage
$V-$ = negative supply voltage

Figure 1-7. Definition of Common Mode Voltage Error

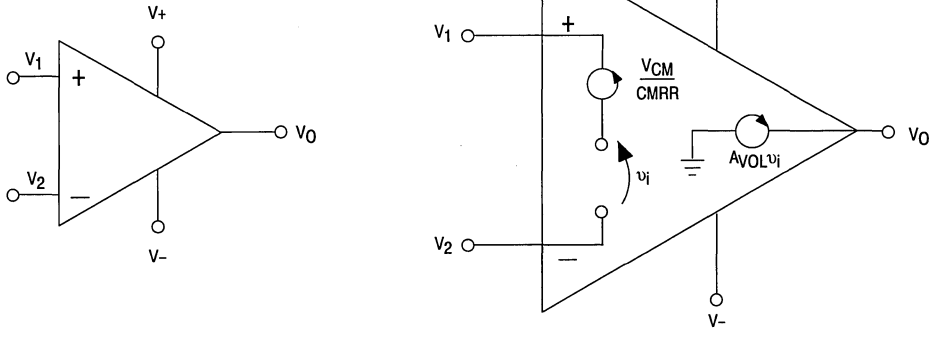
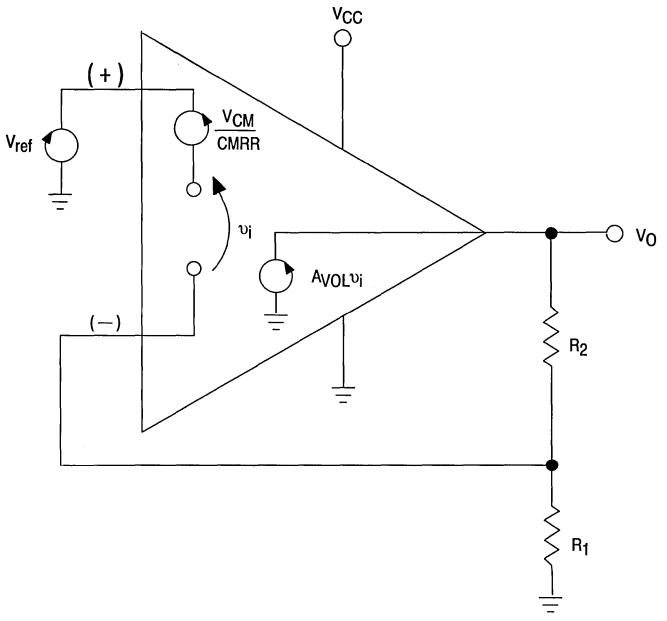


Figure 1-8. Common Mode Regulator Effects



In an ideal amplifier, only the differential input voltage ($V_1 - V_2$) has any effect on the output voltage; the value of V_{CM} would not effect the output. In fact, V_{CM} does influence the amplifier output voltage. This effect can be modeled as an additional voltage offset at the amplifier input equal to $V_{CM}/CMRR$ as shown in Figures 1-7b and 1-8. The latter figure is the same configuration as Figure 1-6, with amplifier input offset voltage and output impedance deleted for clarity and common mode voltage effects added. The output voltage of this configuration is given by:

$$V_O = A_{VOL}\,\upsilon_i = A_{VOL}\left(V_{ref} - \frac{V_{CM}}{CMRR} - \beta V_O\right) \tag{13}$$

Manipulating,

$$V_O = \frac{\left(V_{ref} - \frac{V_{CM}}{CMRR}\right)}{\beta + \frac{1}{A_{VOL}}} \tag{14}$$

where: $$V_{CM} = V_{ref} - \frac{V_{CC}}{2} \tag{15}$$

and, CMRR = common mode rejection ratio

It can be seen from equations (14) and (15) that the output can vary when V_{CC} varies. This can be reduced by designing the amplifier to have a high A_{VOL}, a high CMRR, and by choosing the feedback ratio, β, to be unity.

3. Amplifier Output Impedance

Referring back to equation (9), it can be seen that the equivalent regulator output impedance (Z_O) is given by:

$$Z_O = \frac{\Delta V_O}{\Delta I_O} \simeq \frac{Z_{OL}}{\beta A_{VOL}} \tag{16}$$

This impedance must be as low as possible, in order to minimize load current effects on the output voltage. This can be accomplished by lowering Z_{OL}, choosing an amplifier with high A_{VOL}, and by selecting the feedback ratio (β) to be unity.

A simple way of lowering the effective value of Z_{OL} is to make an impedance transformation with an emitter follower, as shown in Figure 1-9. Given a change in output current (ΔI_O) the amplifier will see a change of only $\Delta I_O/h_{FEQ1}$ in its output current (I_O'). Therefore, (Z_{OL}) in equation (16) has been effectively reduced to Z_{OL}/h_{FEQ1}, reducing the overall regulator output impedance (Z_O).

D. The Regulator within a Regulator Approach

In the preceding text, we have analyzed the sections of an integrated circuit voltage regulator and determined how they contribute to its non-ideal performance characteristics. These are shown in Table 1-1 along with procedures which minimize their effects.

It can be seen that in all cases regulator performance can be improved by selecting A_{VOL} as high as possible and $\beta = 1$. Since a limit is soon approached in how much A_{VOL} can be practically obtained in an integrated circuit amplifier, selecting a feedback ratio (β) equal to unity is the only viable way of improving total regulator performance, especially in reducing regulator output impedance. However, this method presents a basic problem to the regulator designer. If the configuration of Figure 1-6 is used, the output voltage cannot be adjusted to a value other than V_{ref}. The solution is to utilize a different regulator configuration known as the *regulator within a regulator* approach.[2] Its greatest benefit is in reducing total regulator output impedance.

Figure 1-9. Emitter Follower Output

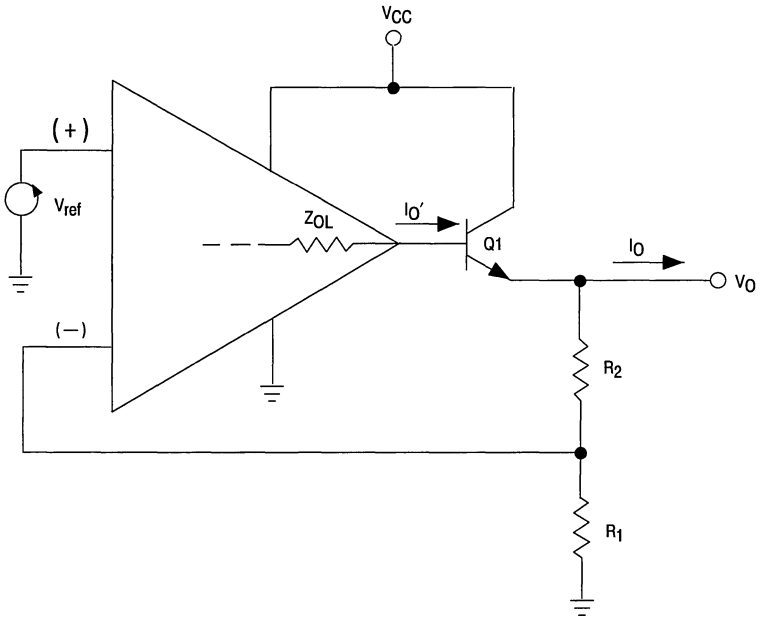


Table 1-1

V_O CHANGES SECTION	EFFECT CAN BE INDUCED BY	MINIMIZED BY SELECTING
Reference	V_{CC}	• Constant current-zener method • Bandgap reference
	T_J	• Bandgap reference • TC compensated zener method
Amplifier	V_{CC}	• High CMRR amplifier • High A_{VOL} amplifier • $\beta = 1$
	T_J	• Low V_{IO} drift amplifier • High A_{VOL} amplifier • $\beta = 1$
	I_O	• Low Z_{OL} amplifier • High A_{VOL} amplifier • Additional emitter follower output • $\beta = 1$

3

As shown in Figure 1-10, amplifier A1 sets up a voltage (V_1) given by:

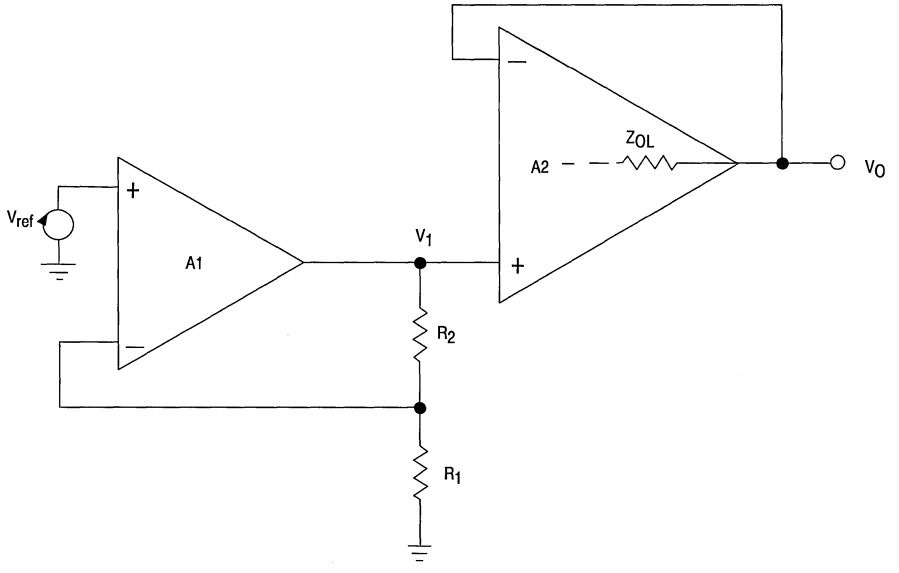
$$V_1 \simeq V_{ref} \left(1 + \frac{R_2}{R_1}\right) \tag{17}$$

V_1 now serves as the reference voltage for amplifier A2, whose output voltage (V_O) is given by:

$$V_O \simeq V_1 \simeq V_{ref} \left(1 + \frac{R_2}{R_1}\right) \tag{18}$$

Note that the output impedance of A2, and therefore the regulator output impedance, has been minimized by selecting A2's feedback factor to be unity; and that output voltage can still be set at voltages greater than V_{ref} by adjusting R_1 and R_2.

Figure 1-10. The "Regulator within a Regulator" Configuration



[1]Widlar, R. J., *New Developments in IC Voltage Regulators*, IEEE Journal of Solid State Circuits, Feb.1971, Vol. SC-6, pgs. 2-7.
[2]Tom Fredericksen, IEEE Journal of Solid State Circuits, Vol. SC-3, Number 4, Dec. 1968, *A Monolithic High Power Series Voltage Regulator.*

SECTION 2
SELECTING A LINEAR IC VOLTAGE REGULATOR

A. Selecting the Type of Regulator

There are five basic linear regulator types; positive, negative, fixed output, tracking and floating regulators. Each has its own particular characteristics and best uses, and selection depends on the designer's needs and trade-offs in performance and cost.

1. Positive Versus Negative Regulators

In most cases, a positive regulator is used to regulate positive voltages and a negative regulator negative voltages. However, depending on the system's grounding requirements, each regulator type may be used to regulate the "opposite" voltage.

Figures 2-1a and 2-1b show the regulators used in the conventional and obvious mode. Note that the ground reference for each (indicated by the heavy line) is continuous. Several positive regulators could be used with the same input supply to deliver several voltages with common grounds; negative regulators may be utilized in a similar manner.

If no other common supplies or system components operate off the input supply to the regulator, the circuits of Figures 2-1c and 2-1d may be used to regulate positive voltages with a negative regulator and vice versa. In these configurations, the input supply is essentially floated, i.e., neither side of the input is tied to the system ground.

There are methods of utilizing positive regulators to obtain negative output voltages without sacrificing ground bus continuity. However, these methods are only possible at the expense of increased circuit complexity and cost. An example of this technique is shown in Section 3.

2. Three-Terminal, Fixed Output Regulators

These regulators offer the designer a simple, inexpensive way to obtain a source of regulated voltage. They are available in a variety of positive or negative output voltages and current ranges.

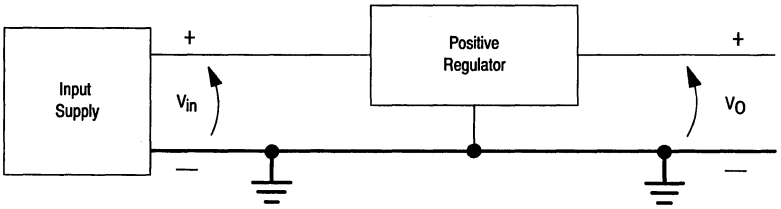
The advantages of these regulators are:

a) Easy to use.
b) Internal overcurrent and thermal protection.
c) No circuit adjustments necessary.
d) Low cost.

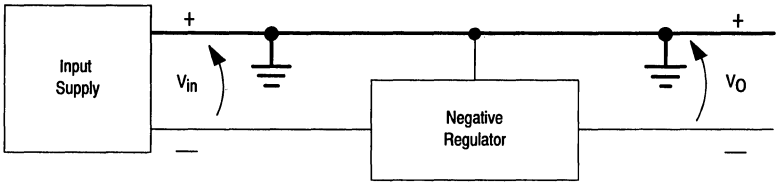
Their disadvantages are:

a) Output voltage cannot be precisely adjusted. (Methods for obtaining adjustable outputs are shown in Section 3).
b) Available only in certain output voltages and currents.
c) Obtaining greater current capability is more difficult than with other regulators. (Methods for obtaining greater output currents are shown in Section 3.)

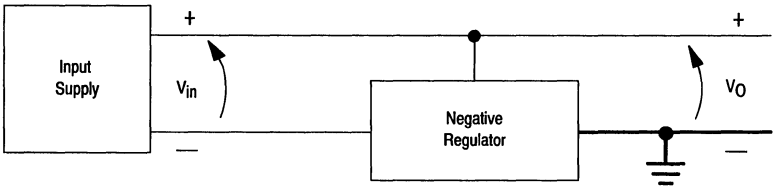
Figure 2-1. Regulator Configurations



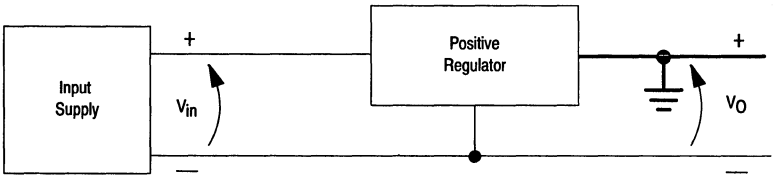
(a) Positive Output Using Positive Regulator



(b) Negative Output Using Negative Regulator



(c) Positive Output Using Negative Regulator



(d) Negative Output Using Positive Regulator

3. Three-Terminal, Adjustable Output Regulators

Like the three-terminal fixed regulators, the three-terminal adjustable regulators are easy and inexpensive to use. These devices provide added flexibility with output voltage adjustable over a wide range, from 1.2 V to nearly 40 V, by means of an external, two-resistor voltage divider. A variety of current ranges from 100 mA to 3.0 A are available.

4. Tracking Regulators

Often a regulated source of symmetrical positive and negative voltage is required for supplying op amps, etc. In these cases, a tracking regulator is required. In addition to supplying regulated positive and negative output voltages, the tracking regulator assures that these voltages are balanced; in other words, the midpoint of the positive and negative output voltages is at ground potential.

This function can be implemented using a positive output regulator together with an op amp or negative output regulator. However, this method results in the use of two IC packages and a multitude of external components. To minimize component count, an IC is offered which performs this function in a single package, the MC1568/MC1468 ± 15 V tracking regulator.

B. Selecting an IC Regulator

Once the type of regulator is decided upon, the next step is to choose a specific device. To provide higher currents than are available from monolithic technologies, an IC regulator will often be used as a driver to a boost transistor. This complicates the selection and design task, as there are now several overlapping solutions to many of the design problems.

Unfortunately, there is no exact step-by-step procedure that can be followed which will lead to the ideal regulator and circuit configuration for a specific application. The regulating circuit that is finally accepted will be a compromise between such factors as performance, cost, size and complexity. Because of this, the following general design procedure is suggested:

1. Select the regulators which meet or exceed the requirements for line regulation, load regulation, TC of the output voltage and operating ambient temperature range. At this point, do not be overly concerned with the regulator capabilities in terms of output voltage, output current, SOA and special features.

2. Next, select application circuits from Section 3 which meet the requirements for output current, output voltage, special features, etc. Preliminary designs using the chosen regulators and circuit configurations are then possible. From these designs a judgement can be made by the designer as to which regulator — circuit configuration combination best meets his requirements in terms of cost, size and complexity.

SECTION 3
LINEAR REGULATOR CIRCUIT CONFIGURATION AND DESIGN CONSIDERATIONS

3

Once the IC regulators, which meet the designer's performance requirements, have been selected, the next step is to determine suitable circuit configurations. Initial designs are devised and compared to determine the IC regulator/circuit configuration that best meets the designer's requirements. In this section, several circuit configurations and design equations are given for the various regulator ICs. Additional circuit configurations can be found on the device data sheets. Organization is first by regulator type and then by variants, such as current boost. Each circuit diagram has component values for a particular voltage and current regulator design.

A. Positive, Adjustable
B. Negative, Adjustable
C. Positive, Fixed
D. Negative, Fixed
E. Tracking
F. Special
    1. Obtaining Extended Output Voltage Range
    2. Electronic Shutdown
G. General Design Considerations

It should be noted that all circuit configurations shown have constant current limiting. If foldback limiting is desired, see Section 4C for techniques and design equations.

A. Positive, Adjustable Output IC Regulator Configurations

1. Basic Regulator Configurations

Positive Three-Terminal Adjustables

These adjustables, comprised of the LM317L, LM317, and LM350 series devices range in output currents of 100 mA, 500 mA, 1.5 A, and 3.0 A respectively. All of these devices utilize the same basic circuit configuration as shown in Figure 3-1A.

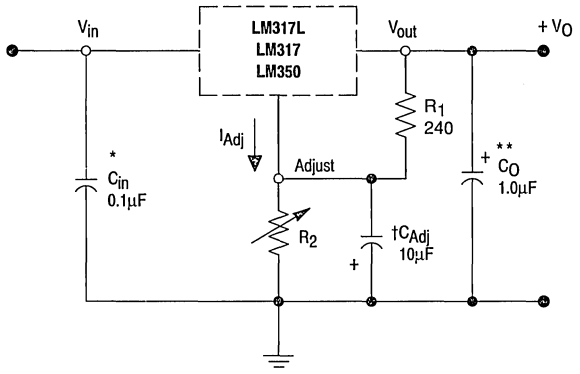
MC1723C

The basic circuit configurations for the MC1723C regulator are shown in Figures 3-2A and 3-3A. For output voltages from ≃ 7.0 V to 37 V the configuration of Figure 3-2A can be used, while Figure 3-3A can be used to obtain output voltages from 2.0 V to ≃ 7.0 V.

2. Output Current Boosting

If output currents greater than those available from the basic circuit configurations are desired, the current boost circuits shown in this section can be used. The output currents which can be obtained with this configurations are limited only by capabilities of the external pass element(s).

Figure 3-1A. Basic Configuration for Positive, Adjustable Output Three-Terminal Regulators



* C_{in} is required if regulator is located an appreciable distance from power supply filter.

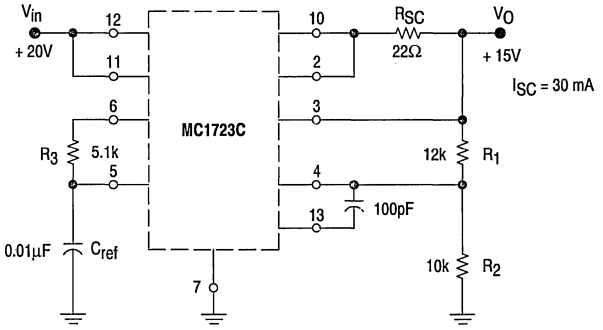
** C_O is not needed for stability, however it does improve transient response.

† C_{Adj} is not required. However, it does improve Ripple Rejection.

$$V_{out} = 1.25\ V\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\ R_2$$

Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications.

Figure 3-2A. MC1723C Basic Circuit Configuration for $V_{ref} \le V_O \le 37$ V



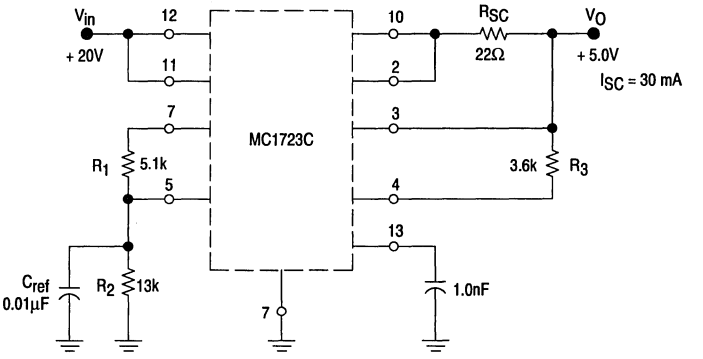
$$R_{SC} \cong \frac{0.66\ V}{I_{SC}}\ ;\ 10\ k\Omega < R_1 + R_2 < 100\ k\Omega$$

$$R_3 \cong R_1 \parallel R_2\ ;\ 0 \le C_{ref} \le 0.1\ \mu F$$

$$R_2 = \frac{V_{ref}}{V_O}\ (R_1 + R_2) \approx \frac{7.0\ V}{V_O}\ (R_1 + R_2)$$

Values shown are for a 15 V, 30 mA regulator using an MC1723CP for a $T_{A(max)} = 25°C$.

Figure 3-3A. MC1723C Basic Circuit Configuration for 2.0 V ≤ V_O ≤ V_{ref}



$$R_{SC} \simeq \frac{0.66V}{I_{SC}} \; ; \; 10\ k\Omega < R_1 + R_2 < 100\ k\Omega$$

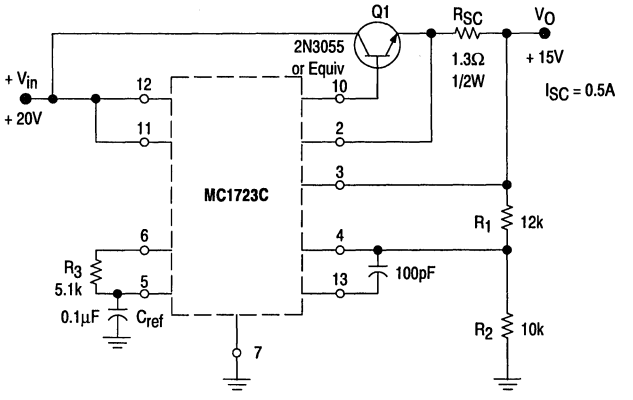
$$R_2 = \frac{V_O}{V_{ref}} \; (R_1 + R_2) \simeq \frac{V_O}{7.0\ V} \; (R_1 + R_2) \colon R_3 = R_1 \parallel R_2$$

$$0 \le C_{ref} \le 0.1\ \mu F$$

Values shown are for a 5.0 V, 30 mA regulator using an MC1723CP for a $T_{A(max)}$ = 705C.

To obtain greater output currents with the MC1723C the configurations shown in Figures 3-4A and 3-5A can be used. Figure 3-4A uses an NPN external pass element, while a PNP is used in Figure 3-5A.

Figure 3-4A. MC1723C NPN Boost Configuration



$$R_{SC} \cong \frac{0.66\ V}{I_{SC}} \; ; \; 10\ k\Omega < R_1 + R_2 < 100\ k\Omega$$

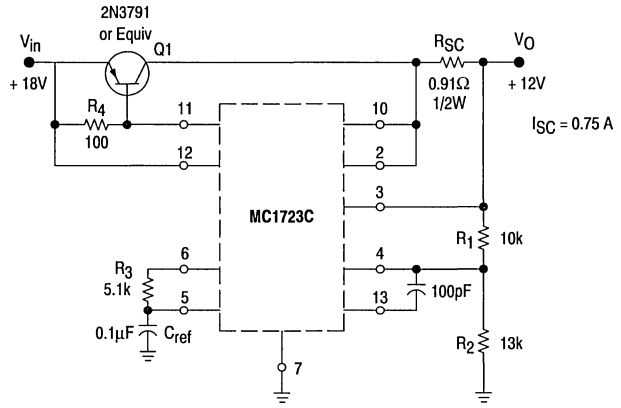
$$R_2 = \frac{V_{ref}}{V_O} \; (R_1 + R_2) \cong \frac{7.0\ V}{V_O} \; (R_1 + R_2)$$

$$0 \le C_{ref} \le 0.1\ \mu F \; ; \; R_3 \cong R_1 \parallel R_2$$

Selection of Q1 based on considerations of Section 4.

Values shown are for a 15 V, 500 mA regulator using an unheatsinked MC1723CP and a 2N3055 on a 6°C/W heatsink for T_A up to + 70°C.

Figure 3-5A. MC1723C PNP Boost Configuration



$$R_{SC} \cong \frac{0.66\ V}{I_{SC}} \ ; \ 10\ k\Omega < R_1 + R_2 < 100\ k\Omega \ ; \ 0 \le C_{ref} \le 0.1\ \mu F$$

$$R_2 = \frac{V_{ref}}{V_O} (R_1 + R_2) \cong \frac{7.0\ V}{V_O} (R_1 + R_2) \ ; \ R_3 = R_1 \parallel R_2$$

$$0 < R_4 \le V_{BE_{on}\ (Q1)} / 5.0\ mA$$

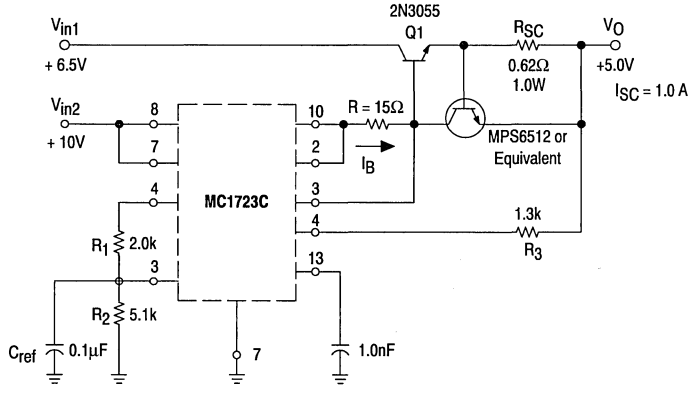
Selection of Q1 based on considerations of Section 4.

Values shown are for a 12 V, 750 mA regulator using an unheatsinked MC1723CP and a 2N3791 on a 4°C/W heatsink for T_A up to + 70°C.

3. High Efficiency Regulator Configurations

When large output currents at voltages under approximately 9.0 V are desired, the configuration of Figure 3-6A can be utilized to obtain increased operating efficiency. This is accomplished by providing a separate low voltage input supply for the pass element. This method, however, usually necessitates that separate short circuit protection be provided for the IC regulator and external pass element. Figure 3-6A shows a high efficiency regulator configuration for the MC1723C.

Figure 3-6A. MC1723C High Efficiency Regulator Configuration



$$R_{SC} \cong \frac{0.6\ V}{I_{SC}} \ ; \ R \cong \frac{0.66\ V}{I_{b(max)}} \ ; \ 10\ k\Omega < R_1 + R_2 < 100\ k\Omega; \ R_2 = \frac{V_O}{V_{ref}} (R_1 + R_2) \cong \frac{V_O}{7.0\ V} (R_1 + R_2)$$

$0 \le C_{ref} \le 0.1\ \mu F$; $R_3 \cong R_1 \parallel R_2$; see Section 3F for general design considerations.

Selection of Q1 based on considerations of Section 4.

Values shown for a 5.0 V, 1.0 A regulator using an unheatsinked MC1723CP and a 2N3055 on a 10°C/W heatsink for T_A up to + 70°C.

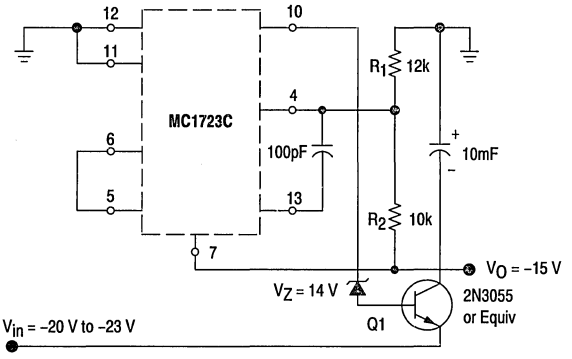
B. Negative, Adjustable Output IC Regulator Configurations

1. Basic Regulator Configurations

MC1723C

Although a positive regulator, the MC1723C can be used in a negative regulator circuit configuration. This is done by using an external pass element and a zener level shifter as shown in Figure 3-1B. It should be noted that for proper operation, the input supply must not vary over a wide range, since the correct value for V_Z depends directly on this voltage. In addition, it should be noted that this circuit will not operate with a shorted output.

Figure 3-1B. MC1723C Negative Regulator Configuration



$$|V_O| \geq 10\ V;\ 10\ k\Omega \leq R_1 + R_2 \leq 100\ k\Omega;\ R_2 = \frac{V_{ref}}{|V_O|}(R_1 + R_2) \cong \frac{7.0\ V}{|V_O|}(R_1 + R_2)$$

$$V_Z \leq |V_{in}| - V_{BE(Q1)} - 3.0\ V;\ V_Z \geq |V_{in}| - |V_O| - V_{BE(Q1)} + 6.0\ V$$

Selection of Q1 based on considerations of Section 4.

Values shown are for a −15 V, 750 mA regulator using the MC1723CP with Q1 mounted on a 20°C/W heatsink at T_A up to +70°C. **Do not short circuit output.**

C. Positive, Fixed Output IC Regulator Configurations

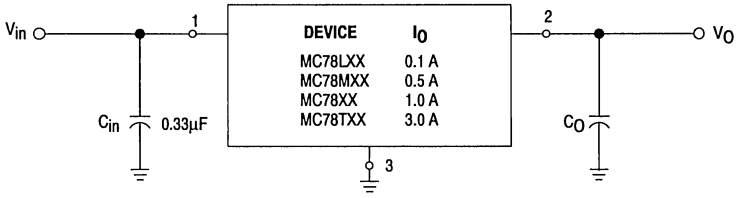
1. Basic Regulator Configuration

The basic current configuration for the positive three-terminal regulators is shown in Figure 3-1C. Depending on which regulator type is used, this configuration can provide output currents in excess of 3.0 A.

2. Output Current Boosting

Figure 3-2C illustrates a method for obtaining greater output currents with the three-terminal positive regulators. Although any of these regulators may be used, usually it is most economical to use the 1.0 A MC7800C in this configuration.

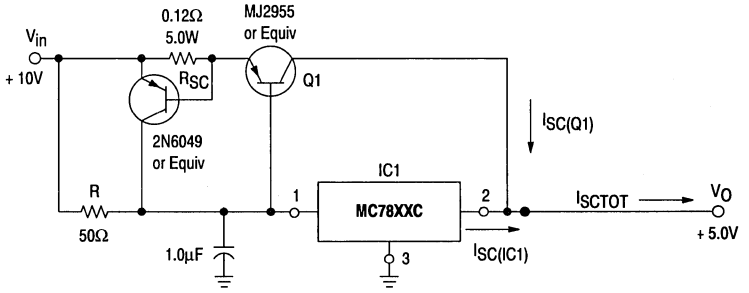
Figure 3-1C. Basic Circuit Configuration for the Positive, Fixed Output Three-Terminal Regulators



C_{in}: required if regulator is located more than a few (≈2 to 4) inches away from input supply capacitor; for long input leads to regulator, up to 1.0 µF may be needed for C_{in}. C_{in} should be a high frequency type capacitor.
C_O: improves transient response.
XX: two digits of type number indicating nominal output voltage.

See Section 15 for heatsinking.

Figure 3-2C. Current Boost Configuration for Positive Three-Terminal Regulators



XX: two digits of type number indicating nominal output voltage.
R: used to divert IC regulator bias current and determines at what output current level Q1 begins conducting.

$$0 < R \leq \frac{V_{BE\,on(Q1)}}{I_{Bias\,(IC1)}} \; ; \; R_{SC} \approx \frac{0.6\ V}{I_{SC(Q1)}} \; ; \; I_{SCTOT} = I_{SC(Q1)} + I_{SC(IC1)}$$

Selection of Q1 based on considerations of Section 4.

Values shown are for a 5.0 V, 5.0 A regulator using an MC7805CT on a 2.5°C/W heatsink and Q1 on a 1°C/W heatsink for T_A up to 70°C.

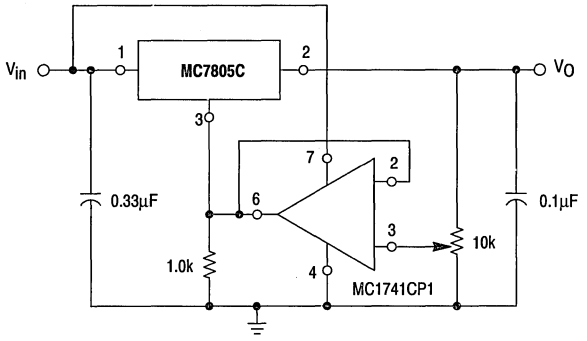
3. Obtaining an Adjustable Output Voltage

With the addition of an op amp, an adjustable output voltage supply can be obtained with the MC7805C. Regulation characteristics of the three-terminal regulators are retained in this configuration, shown in Figure 3-3C. If lower output currents are required, then an MC78MO5C (0.5 A) could be used in place of the MC7805C.

4. Current Regulator

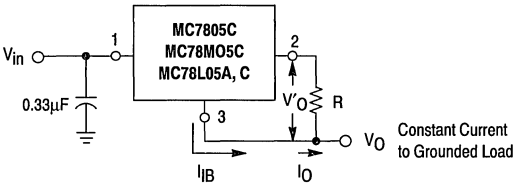
In addition to providing voltage regulation, the three-terminal positive regulators can also be used as current regulators to provide a constant current source. Figure 3-4C shows this configuration. The output current can be adjusted to any value from ≈ 8.0 mA (I_Q, the regulator bias current) up to the available output current of the regulator. Five volt regulators should be used to obtain the greatest output voltage compliance range for a given input voltage.

Figure 3-3C. Adjustable Output Voltage Configuration Using a Three-Terminal Positive Regulator



V_O = 7.0 V to 33 V; $V_{in} - V_O \geq 2.0$ V; $V_{in} \geq 35$ V

Figure 3-4C. Current Regulator Configuration



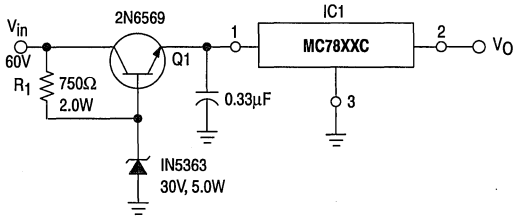
$$I_O = \frac{V'_O}{R} + I_{IB};\ \text{Current Reg}\ \Delta I_O = \frac{\Delta V'_O}{R} + \Delta I_{IB}$$

$V_O + V'_O + 2.0\ V \leq V_{in} \leq 35\ V$

5. High Input Voltage

Occasionally, it may be necessary to power a three-terminal regulator from a supply voltage greater than $V_{in(max)}$, 35 V or 40 V. In these cases a preregulator circuit, as shown in Figure 3-5C, may be used.

Figure 3-5C. Preregulator for Input Voltages Above $V_{in(max)}$



$$R_1 = \left(\frac{V_{in} - 30}{1.5}\right) \bullet h_{fe(Q1)};\ V_{CEO(Q1)} \leq V_{in}$$

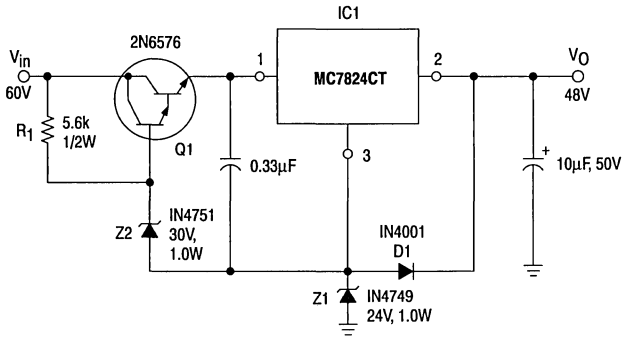
XX: two digits of type number indicating nominal output voltage.

Values shown for V_{in} = 60 V; Q1 should be mounted on a 2°C/W heatsink for operation at T_A up to +70°C. IC1 should be appropriately heatsinked for the package type used.

6. High Output Voltage

If output voltages above 24 V are desired, the circuit configuration of Figure 3-6C may be used. Zener diode Z1 sets the output voltage, while Q1, Z2, and D1 assure that the MC7824C does not have more than 30 V across it during short circuit conditions.

Figure 3-6C. High Output Voltage Configuration for Three-Terminal Positive Regulators



$$V_O = V_{Z1} + 24;\ R_1 = \left(\frac{V_{in} - (V_{Z1} + V_{Z2})}{1.5}\right) \bullet h_{fe(Q2)}$$

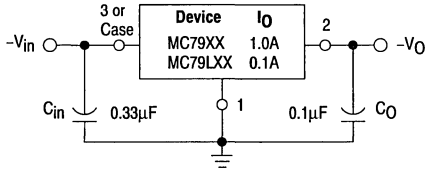
Values shown are for a 48 V, 1.0 A regulator; Q1 mounted on a 10°C/W heatsink and IC1 mounted on a 2°C/W heatsink for T_A up to +70°C.

D. Negative, Fixed Output IC Regulator Configurations

1. Basic Regulator Configurations

Figure 3-1D gives the basic circuit configuration for the MC79XX and MC79LXX three-terminal negative regulators.

Figure 3-1D. Basic Circuit Configuration for the Negative Three-Terminal Regulators



C_{in}: required if regulator is located more than a few (≈ 2 to 4) inches away from input supply capacitor; for long input leads to regulator, up to 1.0 µF may be required. C_{in} should be a high frequency type capacitor.

C_O: improves stability and transient response.

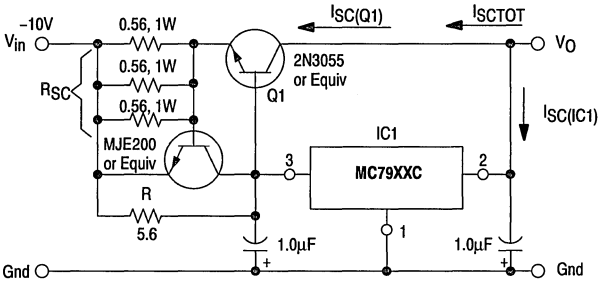
XX: two digits of type number indicating nominal output voltage.

See Section 15 for heatsinking.

Output Current Boosting

In order to obtain increased output current capability from the negative three-terminal regulators, the current boost configuration of Figure 3-2D may be used. Currents which can be obtained with this configuration are limited only by the capabilities of the external pass transistor(s).

Figure 3-2D. Output Current Boost Configuration for Three-Terminal Negative Regulators



XX: two digits of type number indicating output voltage. See Section 2 for available voltages.
R: used to divert regulator bias current and determine at what output current level Q1 begins conducting.

$$O < R \leq \frac{V_{BE\,on(Q1)}}{I_{Bias(IC1)}}$$

$$I_{SCTOT} = I_{SC(Q1)} + I_{SC(IC1)}$$

$$R_{SC} \approx \frac{0.6\ V}{I_{SC(Q1)}}$$

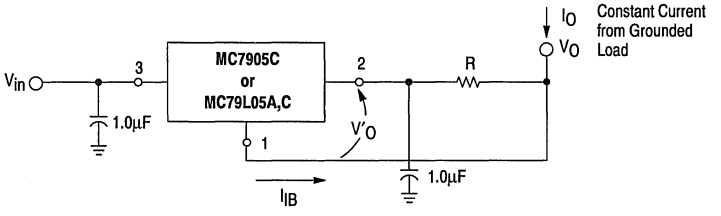
Selection of Q1 based on considerations of Section 4.

Values shown are for a –5.0 V, +4.0 A regulator; using an MC7905CT on a 1.5°C/W heatsink with Q1 mounted on a 1°C/W heatsink for T_A up to +70°C.

2. Current Regulator

The three-terminal negative regulators may also be used to provide a constant current sink, as shown in Figure 3-3D. In order to obtain the greatest output voltage compliance range at a given input voltage, the MC7905 or MC79L05 should be used in this configuration.

Figure 3-3D. Current Regulator Configuration for the Three-Terminal Negative Regulators



$V_{in} \geq -35$ V for MC7905C
$V_{in} \geq -30$ V for MC79L05C
$V_{in} \leq V_O + V_O - 2.0$ V

$$I_O = \frac{V_{O'}}{R} + I_{IB}$$

$$\text{Current regulation, } \Delta I_O = \frac{\Delta V_{O'}}{R} + \Delta I_{IB}$$

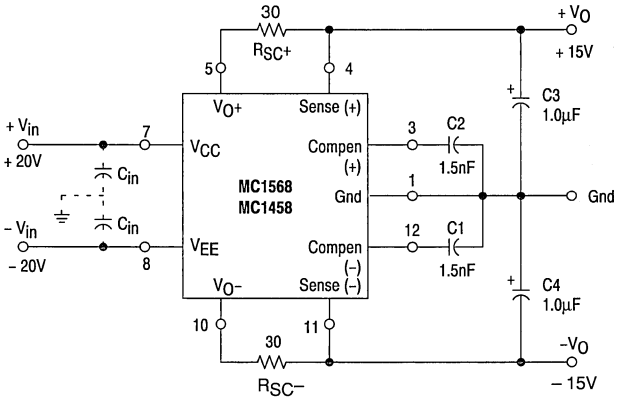
E. Tracking IC Regulator Configurations

MC1568, MC1468

Figure 3-1E shows the basic circuit configuration for the MC1568, MC1468 Dual Tracking Regulator. The outputs of this device are internally set at ± 15 V. (The output voltage can be externally adjusted with some accompanying loss of temperature performance; see device data sheet.) This configuration is capable of providing up to ± 100 mA of load current, depending on operating conditions and package style chosen. If greater output currents are desired, the current boost configuration shown in Figure 3-2E can be used.

It should be noted that in this configuration, when the positive output of the MC1568, MC1468 drops below approximately 14.5 V, e.g. during a short circuit, the negative output will not drop proportionally. Instead, it collapses to ≈ 0 V. This can create a latch condition, depending on the type of load.

Figure 3-1E. MC1568, MC1468 Basic Regulator Configuration

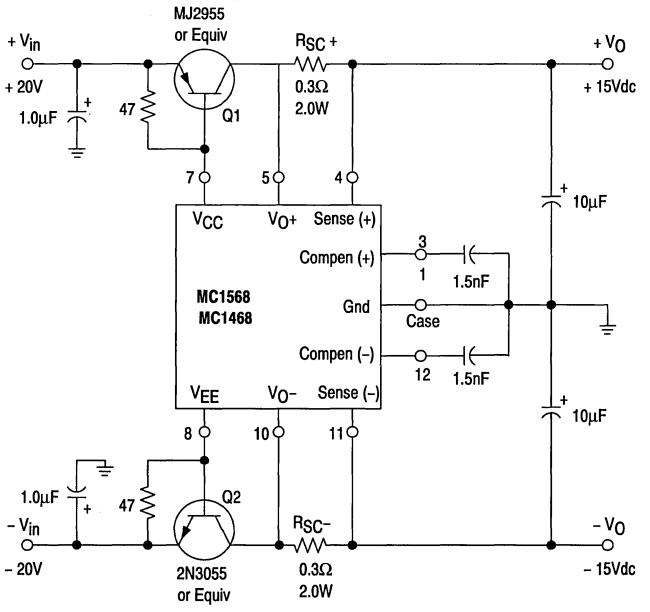


C1 and C2 should be located as close to the device as possible. A 0.1 µF ceramic capacitor (C_{in}) may be required on the input lines if the device is located an appreciable distance from the rectifier filter capacitors. C3 and C4 may be increased to improve load transient response and to reduce the output noise voltage. At low temperature operation, it may be necessary to bypass C4 with a 0.1 µF ceramic disc capacitor.

$$R_{SC+} \cong \frac{0.6\ V}{I_{SC+}} \; ; R_{SC-} \cong \frac{0.6\ V}{I_{SC-}}$$

Values shown are for a ± 15 V, 20 mA regulator using an MC1468 regulator for $T_A \leq 75°C$.

Figure 3-2E. MC1568, MC1468 Current Boost Configuration



$$R_{SC+} \approx \frac{0.6\ V}{I_{SC+}}\ ;\ R_{SC-} \approx \frac{0.6\ V}{I_{SC-}}$$

Selection of Q1 based on considerations of Section 4.

Values shown are for a ± 15 V, ± 2.0 A regulator using an MC1468 on a 2°C/W heatsink with Q1 & Q2 mounted on a 1°C/W heatsink for $T_A \leq 70°C$.

F. General Design Considerations

In addition to the design equations given in the regulator circuit configuration panels of Sections 3A-E, there are a few general design considerations which apply to all regulator circuits. These considerations are given below.

1. Regulator Voltages

For any circuit configuration, the worse-case voltages present on each pin of the IC regulator must be within the maximum and/or minimum limits specified on the device data sheets. These limits are instantaneous values, not averages.

They include: a. $V_{in(min)}$
b. $V_{in(max)}$
c. $(V_{in} - V_{out})$ min
d. $V_{out(min)}$
e. $V_{out(max)}$

For example, the voltage between Pins 12 and 7 (V_{in}) of an MC1723CP must never fall below 9.5 V, even instantaneously, or the regulator will not function properly (see Figure 3-1B).

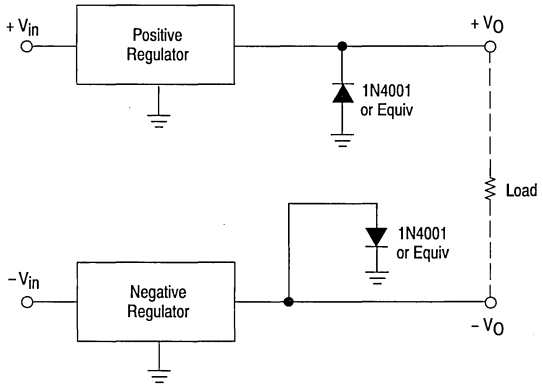
2. Regulator Power Dissipation, Junction Temperature and Safe Operating Area

The junction temperature, power dissipation output current or safe operating area limits of the IC regulator *must never be exceeded.*

3. Operation with a Load Common to a Voltage of Opposite Polarity

In many cases, a regulator powers a load which is not connected to ground but instead is connected to a voltage source of opposite polarity (e.g. op amps, level shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 3-1F. This protects the regulator, during startup and short circuit operation, from output polarity reversals.

Figure 3-1F. Output Polarity Reversal Protection



4. Reverse Bias Protection

Occasionally, there exists the possibility that the input voltage to the regulator can collapse faster than the output voltage. This could occur, for example, if the input supply is "crowbarred" during an output overvoltage condition. If the output voltage is greater ≈ 7.0 V, the emitter-base junction of the series pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed, as shown in Figure 3-2F.

Figure 3-3F shows a three-terminal positive-adjustable regulator with the recommended protection diodes for output voltages in excess of 25 V, or high output capacitance values (C_O > 25 μF, C_{Adj} >10 μF). Diode D1 prevents C_O from discharging through the regulator during an input short circuit. Diode D2 protects against capacitor C_{Adj} from discharging through the regulator during an output short circuit. The combination of diodes D1 and D2 prevents C_{Adj} from discharging through the regulator during an input short circuit.

Figure 3-2F. Reverse Bias Protection

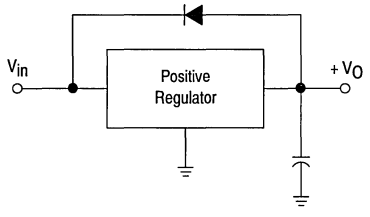
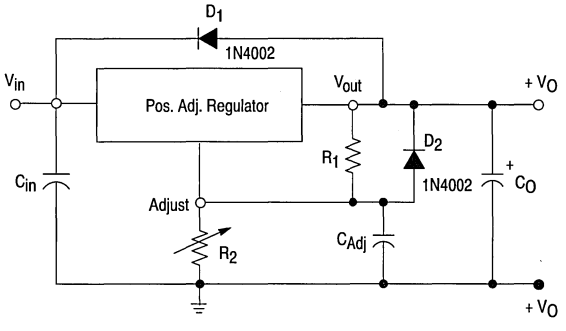


Figure 3-3F. Reverse Bias Protection for Three-Terminal Adjustable Regulators



SECTION 4

SERIES PASS ELEMENT CONSIDERATIONS FOR LINEAR REGULATORS

3

Presently, most monolithic IC voltage regulators that are available have output current capabilities from 100 mA to 3.0 A. If greater current capability is required, or if the IC regulator does not possess sufficient safe-operating-area (SOA), the addition of an external series pass element is necessary.

In this section, configurations, specifications and current limit techniques for external series pass elements will be considered. For illustrative purposes, pass elements for only positive regulator types will be discussed. However, the same considerations apply for pass elements used with negative regulators.

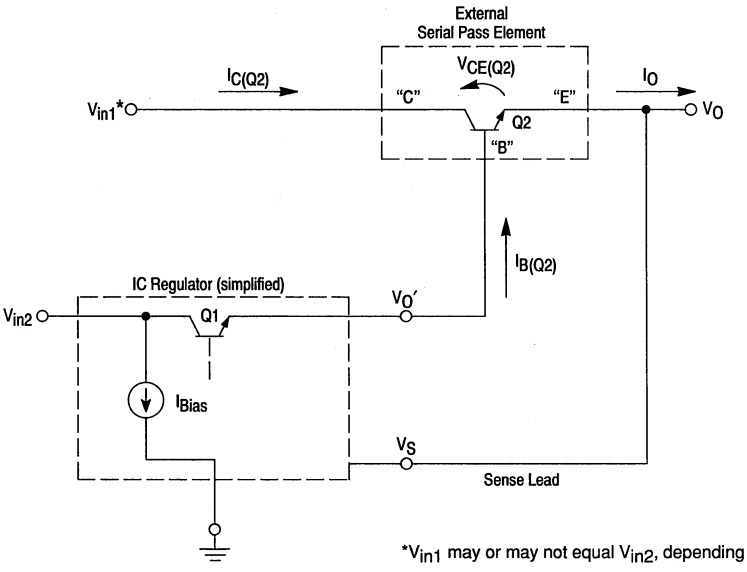
A. Series Pass Element Configurations

Using an NPN Type Transistor

If the IC regulator has an external sense lead, an NPN type series pass element may be used, as shown in Figure 4-1 A. This pass element could be a single transistor or multiple transistors arranged in Darlington and/or paralleled configurations.

In this configuration, the IC regulator supplies the base current (I_B) to the pass element (Q2) which acts as a current amplifier and provides the increased output current (I_O) capability.

Figure 4-1A. NPN Type Series Pass Element Configuration

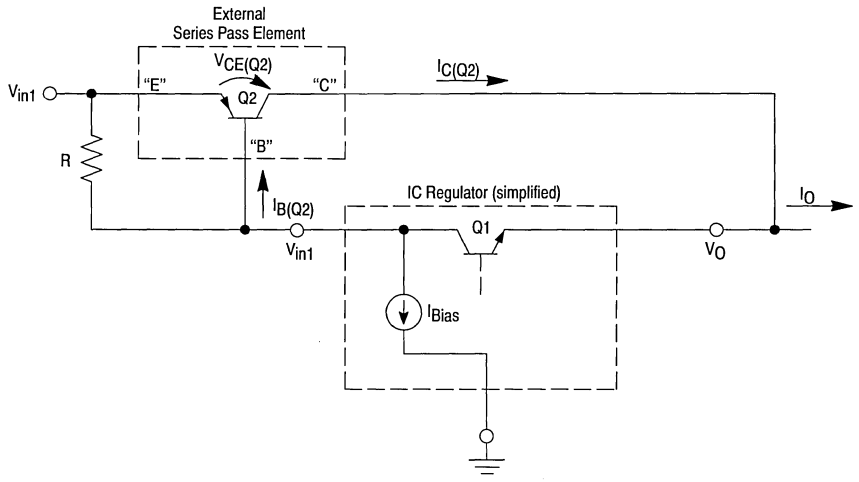


*V_{in1} may or may not equal V_{in2}, depending on the application.

Using a PNP Type Transistor

If the IC regulator does not have an external sense lead, as in the case of the three-terminal fixed output regulators, the configuration of Figure 4-1B can be used. (Regulators which possess an external sense lead may also be used with this configuration.) As before, the PNP type pass element can be a single transistor or multiple transistors.

Figure 4-1B. PNP Type Series Pass Element Configuration



This configuration functions in a similar manner to that of Figure 4-1A, in that the regulator supplies base current to pass element. The resistor (R) serves to route the IC regulator bias current (I_{Bias}) away from the base of Q2. If not included, regulation would be lost at low output currents. The value of R is low enough to prevent Q2 from turning on when I_{Bias} flows through this resistor, and is given by:

$$0 < R \leq \frac{V_{BEon(Q2)}}{I_{Bias}} \qquad (4.0)$$

B. Series Pass Element Specifications

Independent of which configuration is utilized, the transistor or transistors that compose the pass element must have adequate ratings for $I_{C(max)}$, V_{CEO}, h_{fe}, power dissipation, and safe operating area.

1. $I_{C(max)}$ — for the pass element of Figure 4-1A, $I_{C(max)}$ is given by:

$$I_{C(max)(Q2)} \geq I_{O(max)} - I_{B(max)(Q2)} = I_{O(max)} - \frac{I_{C(max)(Q2)}}{h_{fe(Q2)}} \geq I_{O(max)} \qquad (4.1)$$

(4.2)

For the configuration of Figure 4-1B:

$$I_{C(max)(Q2)} \geq I_{O(max)} + I_{B(max)(Q2)} \geq I_{O(max)} \qquad (4.3)$$

(4.4)

2. V_{CEO} — since $V_{CE(Q2)}$ is equal to $V_{in1(max)}$ when the output is shorted or during start up:

$$V_{CEO(Q2)} \leq V_{in1(max)} \tag{4.5}$$

3. h_{fe} — the minimum DC current gain for Q2 in Figures 4-1A and 4-1B is given by:

$$h_{fe(min)(Q2)} \geq \frac{I_{C(max)(Q2)}}{I_{B(max)(Q2)}} @ V_{CE} = (V_{in1(min)} - V_O) \tag{4.6}$$

3

4. Maximum Power Dissipation $P_{D(max)}$, and Safe Operating Area (SOA)

For any transistor there are certain combinations of I_C and V_{CE} at which it may safely be operated. When plotted on a graph, whose axes are V_{CE} and I_C, a safe-operating region is formed.

As an example, the safe-operating-area (SOA) curve for the well known 2N3055 NPN silicon power transistor is shown in Figure 4-2. The boundaries of the SOA curve are formed by $I_{C(max)}$, power dissipation, second breakdown and V_{CEO} ratings of the transistor. Notice that the power dissipation and second breakdown ratings are given for a case temperature of +25°C and must be derated at higher case temperatures. (Derating factors may be found in the transistors' data sheets.) These boundaries must never be exceeded during operation, or destruction of the transistor(s) which constitute the pass element may result. (In addition, the maximum operating junction temperature *must not be exceeded*, see Section 15.)

C. Current Limiting Techniques

In order to select a transistor or transistors with adequate SOA, the locus of pass element I_C and V_{CE} operating points must be known. This locus of points is determined by the input voltage (V_{in1}, output voltage (V_O), output current (I_O) and the type of output current limiting technique employed.

In most cases, V_{in1}, V_O, and the required output current are already known. All that is left to determine is how the chosen current limit scheme affects required pass element SOA.

Note: Since the external pass element is merely an extension of the IC regulator, the following discussions apply equally well to IC regulators not using an external pass element.

1. Constant Current Limiting

This method is the simplest to implement and is extensively used, especially at the lower output current levels. The basic circuit configuration is shown in Figure 4-3A, and operates in the following manner.

As the output current increases, the voltage drop across R_{SC} increases, proportionately. When the output current has increased to the point that the voltage drop across R_{SC} is equal to the base-emitter ON voltage of Q3 ($V_{BEon(Q3)}$), Q3 conducts. This diverts base current (I_{Drive}) away from Q1, the IC regulator's internal series pass element. Base drive ($I_{B(Q2)}$) of Q2 is therefore reduced and its collector-emitter voltage increases, thereby reducing the output voltage below its regulated value, V_{out}. The resulting output voltage-current characteristic is shown in Figure 4-3B.

The value of I_{SC} is given by:

$$I_{SC} = \frac{V_{BEon(Q3)}}{R_{SC}} \tag{4.7}$$

Figure 4-2. 2N3055 Safe Operating Area (SOA)

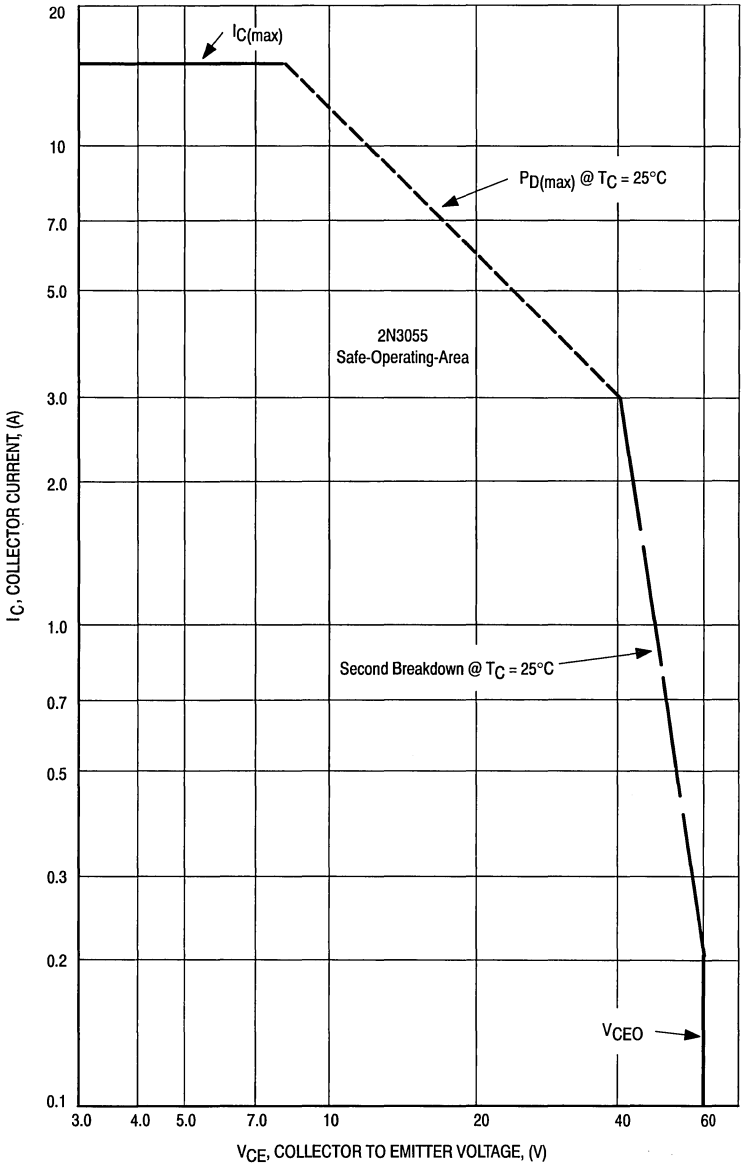
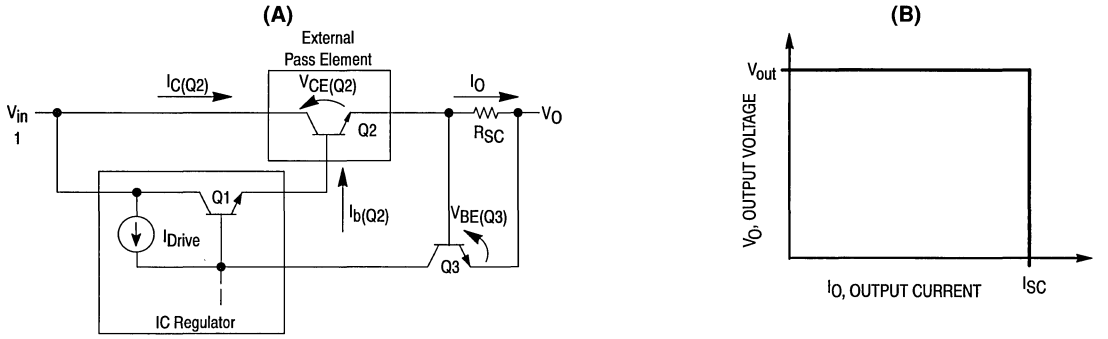


Figure 4-3. Constant Current Limiting



By using the base of Q1 in the IC regulator as a control point, this configuration has the added benefit of limiting the IC regulator output current ($I_{B(Q2)}$) to $I_{SC}/h_{fe(Q2)}$, as well as limiting the collector current of Q2 to I_{SC}. Of course, access to this point is necessary. Fortunately, it is usually available in the form of a separate pin or as the regulator's compensation terminal.(1)

The required safe-operating-area for Q2 can be obtained by plotting the V_{CE} and I_C of Q2 given by:

$$V_{CE(Q2)} = V_{in1} - V_O - I_O R_{SC} \simeq V_{in1} - V_O \quad (4.8)$$

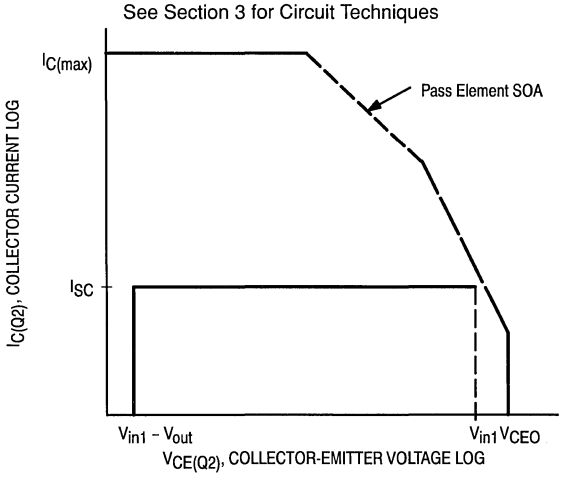
$$I_{C(Q2)} \simeq I_O \quad (4.9)$$

$$\text{where, } V_O = V_{out} \text{ for } 0 \leq I_O \leq I_{SC} \quad (4.10)$$

$$\text{and, } I_O = I_{SC} \text{ for } 0 \leq V_O \leq V_{out} \quad (4.11)$$

The resulting plot is shown in Figure 4-4. The transistor chosen for Q2 must have an SOA which encloses this plot, see Figure 4-4. Note that the greatest demand on the transistor's SOA capability occurs when the output of the regulator is short circuited and the pass element must support the full input voltage and short circuit current simultaneously.

Figure 4-4. Constant Current Limit SOA Requirements
See Section 3 for Circuit Techniques



(1) The three-terminal regulators have internal current limiting and therefore do not provide access to this point. If an external pass element is used with these regulators, constant current limiting can still be accomplished by diverting pass element drive.

2. Foldback Current Limiting

A disadvantage of the constant current limit technique is that in order to obtain sufficient SOA the pass element must have a much greater collector current capability than is actually needed. If the short circuit current could be reduced, while still allowing full output current to be obtained during normal regulator operation, more efficient utilization of the pass elements SOA capability would result. This can be done by using a "foldback" current limiting technique instead of constant current limiting.

The basic circuit configuration for this method is shown in Figure 4-5(A). The circuit operates in a manner similar to that of the constant current limiting circuit, in that output current control is obtained by diverting base drive away from Q1 with Q3.

At low output currents, V_A approximately equals V_O and V_{R2} is less than than V_O. Q3 is therefore non-conducting and the output voltage remains constant. As the output current increases, the voltage drop across R_{SC} increases until V_A and V_{R2} are great enough to bias Q3 on. The output current at which this occurs is I_K, the "knee" current.

Figure 4-5. Foldback Current Limiting

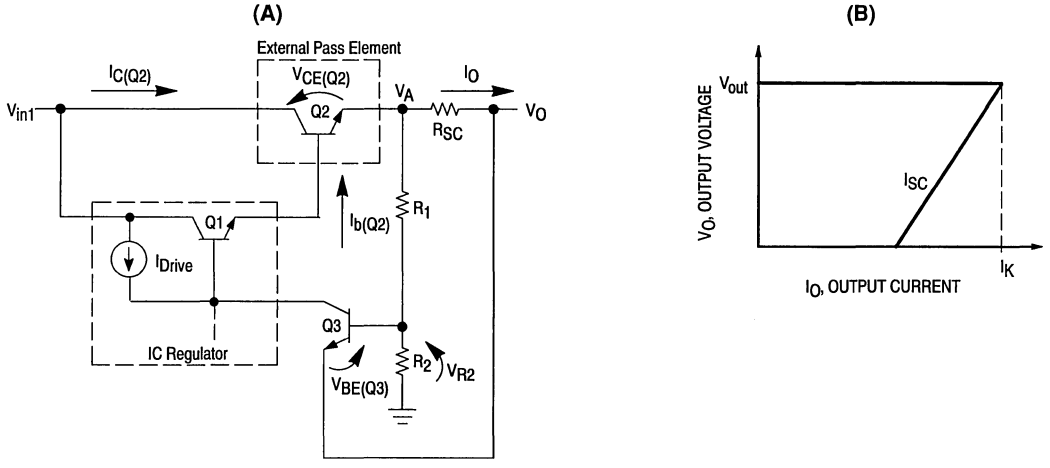
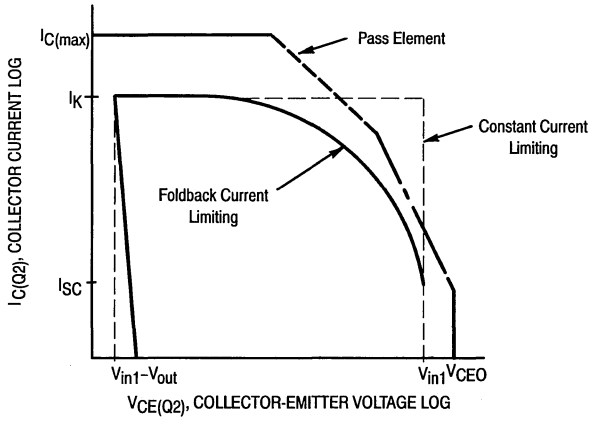


Figure 4-6. Foldback Current Limit SOA Requirements



The output voltage will now decrease. Less output current is now required to keep V_A and V_{R2} at a level sufficient to bias Q3 on since the voltage at its emitter has the tendency to decrease faster than that at its base. The output current will continue to "foldback" as the output voltage decreases, until an output short circuit current level (I_{SC}) is reached when the output voltage is zero. The resulting output current-voltage characteristic is shown in Figure 4-5B. The values for R_1, R_2, and R_{SC} (neglecting base current of Q3) are given by:

$$R_{SC} = \frac{V_{out}/I_{SC}}{(1 + \frac{V_{out}}{V_{BEon(Q3)}}) - \frac{I_K}{I_{SC}}} \quad (4.12)$$

$$\frac{R_2}{R_1 + R_2} = \frac{V_{BEon(Q3)}}{I_{SC}\, R_{SC}} \quad (4.13)$$

$$\text{and, } R_1 + R_2 \leq \frac{V_{out}}{I_{Drive}} \quad (4.14)$$

where: V_{out} = normal regulator output voltage
I_K = knee current
I_{SC} = short circuit current
I_{Drive} = base drive to regulator's internal pass element(s)

A plot of Q2 operating points, which result when using this technique, is shown in Figure 4-6. Note that the pass element is required to operate with a collector current of only I_{SC} during short circuit conditions, not the full output current, I_K. This results in a more efficient utilization of the SOA of Q2 allowing the use of a smaller transistor than if constant current limiting were used. Although foldback current limiting allows use of smaller pass element transistors for a given regulator output current than does constant current limiting, it does have a few disadvantages.

Referring to Equation (4.12), as the foldback ratio (I_K/I_{SC}) is increased, the required value of R_{SC} increases. This results in a greater input voltage at higher foldback ratios. In addition, it can be seen for Equation (4.12) that there exists an absolute limit to the foldback ratio equal to:

$$\left(\frac{I_K}{I_{SC(max)}}\right) = 1 + \frac{V_{out}}{V_{BEon(Q3)}} \text{ for } R_{SC} = \infty \quad (4.15)$$

For these reasons, foldback ratios greater than 2:1 or 3:1 are not usually practical for the lower output voltage regulators.

D. Paralleling Pass Element Transistors

Occasionally, it will not be possible to obtain a transistor with sufficient safe-operating-area. In these cases it is necessary to parallel two or more transistors. Even if a single transistor with sufficient capability is available, it is possible that paralleling two smaller transistors is more economical.

In order to insure that the collector currents of the paralleled transistors are approximately equal, the configuration of Figure 4-7 can be used. Emitter-ballasting resistors are used to force collector-current sharing between Q1 and Q2. The collector-current mismatch can be determined by considering the following, from Figure 4-7,

$$V_{BE1} + V_1 = V_{BE2} + V_2 \tag{4.16}$$

$$\text{and, } \Delta V_{BE} = \Delta V \tag{4.17}$$

where: $V_{BE} = V_{BE1} - V_{BE2}$

and, $\Delta V = V_2 - V_1$

Assuming $I_{E1} \simeq I_{C1}$ and $I_{E2} \simeq O_{C2}$, the collector-current mismatch is given by,

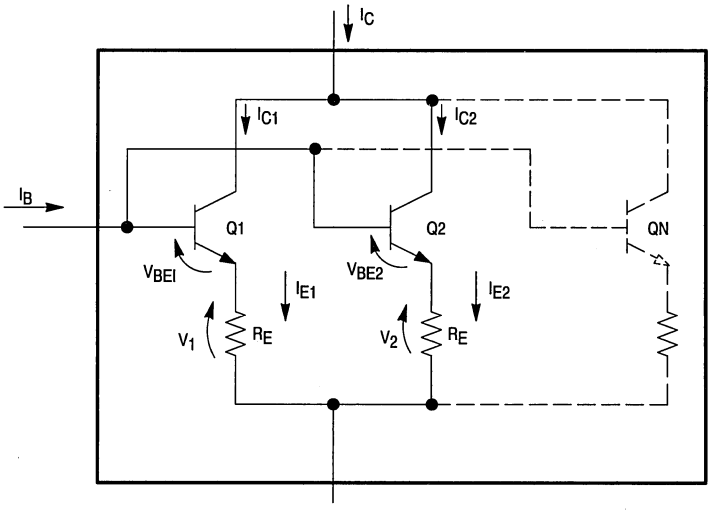
$$\frac{I_{C2} - I_{C1}}{I_{C2}} = \frac{\left(\frac{V_2}{R_E}\right) - \left(\frac{V_1}{R_E}\right)}{\left(\frac{V_2}{R_E}\right)} = \frac{V_2 - V_1}{V_2} = \frac{\Delta V}{V_2} = \frac{\Delta V_{BE}}{V_2} \tag{4.18}$$ (4.19)

$$\text{and, percent collector-current mismatch} = \frac{\Delta V_{BE}}{V_2} \times 100\% \tag{4.20}$$

From Equation (4.20), the collector-current mismatch is dependent on ΔV_{BE} and V_2. Since ΔV_{BE} is usually acceptable, V_2 should be 1.0 V to 0.5 V, respectively. R_E is therefore given by:

$$R_E = \frac{0.5 \text{ V to } 1.0 \text{ V}}{I_{C1}} = \frac{0.5 \text{ V to } 1.0 \text{ V}}{I_{C2}} = \frac{0.5 \text{ V to } 1.0 \text{ V}}{I_{C/2}} \tag{4.21}$$

Figure 4-7. Paralleling Pass Element Transistors



SECTION 5
LINEAR REGULATOR CONSTRUCTION AND LAYOUT

3

An important, and often neglected, aspect of the total regulator circuit design is the actual layout and component placement of the circuit. In order to obtain excellent transient response performance, high frequency transistors are used in modern integrated circuit voltage regulators. Proper attention to circuit layout is therefore necessary to prevent regulator instability or oscillations, or degraded performance.

In this section, guidelines will be given on proper regulator layout and placement of circuit components. In addition, topics such as remote voltage sensing, semiconductor mounting techniques, and thermal system evaluations will also be discussed.

1. General Layout and Component Placement Considerations

As mentioned previously, modern integrated circuit regulators are necessarily high bandwidth devices in order to obtain good transient response characteristics. To insure stable closed-loop operation, all these devices are frequency compensated, either internally or externally. This compensation can easily be upset by unwanted stray circuit capacitances and lead inductances, resulting in spurious oscillations. Therefore, it is important that the circuit lead lengths be short and the layout as tight as possible. Particular attention should be paid to locating the compensation and bypass capacitors as close to the IC as possible. Lead lengths associated with the external pass element(s), if used, should also be minimized.

Often overlooked is the stray inductance associated with the input leads to the regulator circuit. If the lead length from the input supply filter capacitor to the regulator input is more than a couple of inches, a 0.01 μF to 1.0 μF high frequency type capacitor (tantalum, ceramic, etc.) should be used to bypass the supply leads close to the regulator input pins.

2. Ground Loops and Remote Voltage Sensing

Ground Loops — Regulator performance can also suffer if ground loops in the circuit wiring are not avoided. The most common ground loop problem occurs when the return lead of the input supply filter capacitor is improperly located, as shown in Figure 5-1. If this return lead is physically connected between the load return and the regulator circuit ground point ("B"), a ripple voltage component (60 Hz or 120 Hz) can be induced on the load voltage (V_L). This is due to the high peaks of the filter capacitor ripple current (I_{ripple}) flowing through the lead resistance between the load and regulator. These peaks can be 5 to 15 times the value of load current. Since the regulator will only keep constant the voltage between its sense lead and ground point, points "A" and "B" in Figure 5-1, this additional ripple voltage, V_{lead}, will appear at the load.

This problem can be avoided by proper placement and connection of the filter capacitor return load as shown in Figure 5-2.

Remote Voltage Sensing — Closely related to the above ground loop problem is resistance in the current carrying leads to the load. This can cause poorer than expected load regulation in cases where the load currents are large or where the load is located some distance from the regulator. This is illustrated in Figure 5-3. As stated previously, the regulator circuit will keep the voltage present between its sense and ground pins constant. From Figure 5-3 we can see that any lead resistance between these points and the load will cause the load voltage (V_L) to vary with varying load current, I_L. This effectively lowers the load regulation of the circuit.

Figure 5-1. Filter Capacitor Ground Loop — WRONG!

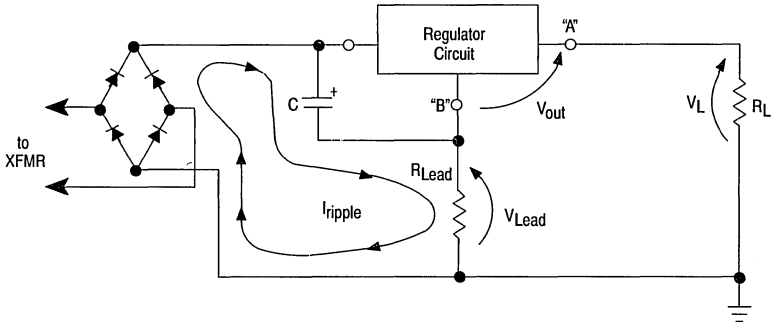
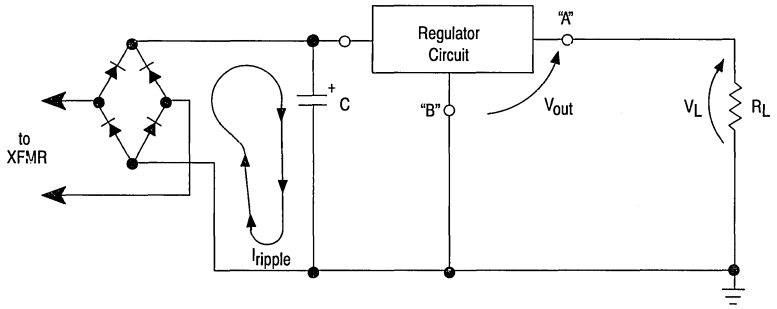


Figure 5-2. Filter Capacitor Ground Loop — RIGHT!



This problem can be avoided by the use of remote Sense leads, as shown in Figure 5-4. The voltage drops in the high current carrying leads now have no effect on the load voltage (V_L). However, since the Sense and Ground leads are usually rather long, care must be exercised that their associated lead inductance is minimized, or loop instability may result. The Ground and Sense leads should be formed into a twisted pair lead to minimize their lead inductance and noise pickup.

Figure 5-3. Effects of Resistance In Output Leads

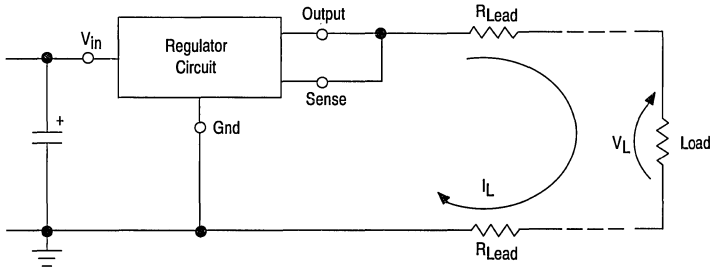
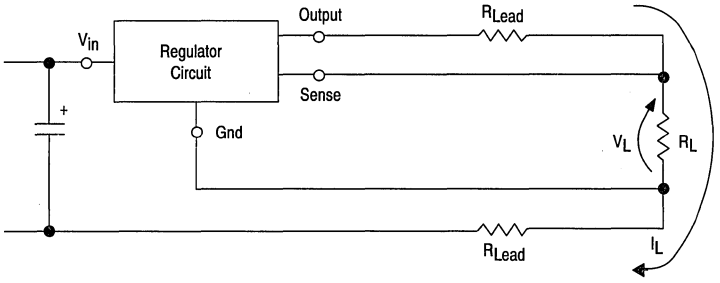


Figure 5-4. Remote Voltage Sensing



3. Mounting Considerations for Power Semiconductors

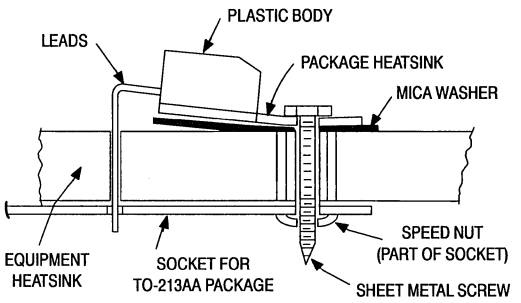
Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead-mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one-half for a decrease in junction temperature from 160° to 135°C.(1) Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.(2) Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger.

3

Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

Figure 5-5 shows an example of doing nearly everything wrong. A tab mount TO-220 package is shown being used as a replacement for a TO-213AA (TO-66) part which was socket mounted. To use the socket, the leads are bent — an operation which, if not properly done, can crack the package, break the internal bonding wires, or crack the die. The package is fastened with a sheet metal screw through a 1/4″ hole containing a fiber-insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, possibly causing enough distortion to crack the die. In addition the contact area is small because of the area consumed by the large hole and the bowing of the package, the result is a much higher junction temperature than expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all poor mounting practices would be covered.

Figure 5-5. Extreme Case of Improperly Mounting A Semiconductor (Distortion Exaggerated)



(1) MIL-HANDBOOK — 2178, SECTION 2.2.
(2) *Navy Power Supply Reliability — Design and Manufacturing Guidelines* NAVMAT P4855-1, Dec. 1982 NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.

In many situations the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc-over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:

1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:

Flange Mount
Plastic Body Mount
Tab Mount
Surface Mount

Appendix A contains a brief review of thermal resistance concepts.

Appendix B discusses measurement difficulties with interface thermal resistance tests.

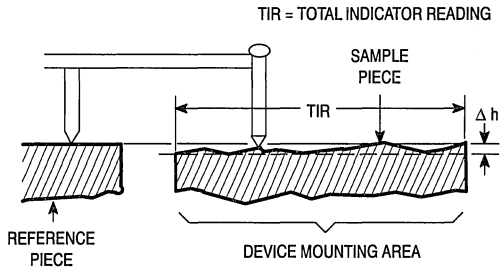
Mounting Surface Preparation

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 5-6. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness (i.e, $\Delta h/TIR$) if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.

Figure 5-6. Surface Flatness Measurement



Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 μin. to 60 μin. is satisfactory. A finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy using a copper TO-204 (TO-3) package with a typical 32-μin. finish, showed that heatsink finishes between 16 μin. and 64 μin. caused less than ±2.5% difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.(3) Most commercially available cast or extruded heatsinks will require spotfacing when used in high power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO-204AA, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This "crater" in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat-dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early-life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine-edge blanking or sheared-through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four-post die sets equipped with proper pressure pads and holding fixtures.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

Surface Treatment

Many aluminum heatsinks are black-anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromate-acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of the paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 V.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

(3) Catalog #87-HS-9 (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381-0839.

Interface Decisions

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise, the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pockmarked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section. To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal and therefore partially fill voids when under pressure.

Thermal Compounds (Grease)

Joint compounds are a formulation of fine zinc or other conductive particles in a silicone oil or other synthetic base fluid which maintains a grease-like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct, a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic-encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the semiconductor chip.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 5-1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

Table 5-1. Approximate Values for Interface Thermal Resistance Data from Measurements Performed In Motorola Applications Engineering Laboratory

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink. (See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

Package Type and Data		Interface Thermal Resistance (°C/W)						
			Metal-to-Metal		With Insulator			
JEDEC Outlines	Description	Test Torque In-Lb	Dry	Lubed	Dry	Lubed	Type	See Note
TO-204AA (TO-3)	Diamond Flange	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO-220AB	Thermowatt	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

NOTES:1. See Figures 5-7 and 5-8 for additional data on TO-204AA and TO-220 packages.
2. Screw not insulated. See Figure 5-12.

Conductive Pads

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a greased bare joint and a joint using Grafoil, a dry graphite compound, is shown in the data of Figure 5-7. Grafoil is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from AAVID is called KON-DUX. It is made with a unique, grain oriented, flake-like structure (patent pending). Highly compressible, it becomes formed to the surface roughness of both the heatsink and semiconductor. Manufacturer's data shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers. They are a fairly recent development; long term problems, if they exist, have not yet become evident.

Insulation Considerations

Since most power semiconductors use are vertical device construction it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non-isolated packages. In these situations insulators are used to isolate the individual components from the heatsink. Newer packages, such as the Motorola Full Pak and EMS modules, contain the electrical isolation material within, thereby saving the equipment manufacturer the burden of addressing the isolation problem.

Insulator Thermal Resistance

When an insulator is used, thermal grease is of greater importance than with a metal-to-metal contact, because two interfaces exist instead of one and some materials, such as mica, have a hard, markedly uneven surface. With many isolation materials reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

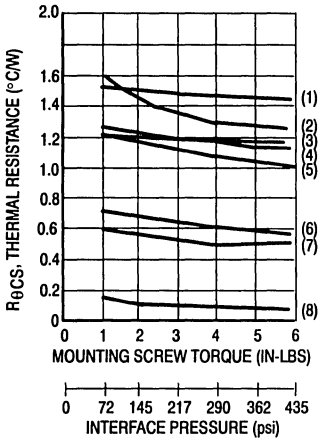
Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO-204 (TO-3) and TO-220 packages, is shown in Figure 5-7, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction-to-case).

Referring to Figure 5-7, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraided, as the dust is highly toxic.) Thermafilm is a filled polyimide material which is used for isolation (variation of Kapton). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high break down voltage and fairly low thermal resistance at a low cost but it certainly should be used with grease.

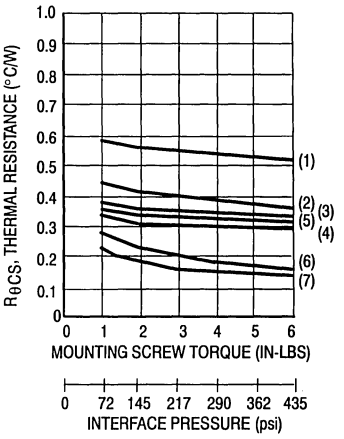
Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut-through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton or fiberglass. By comparing Figures 5-7(c) and 5-7(d), it can be noted that Thermasil, a filled silicone rubber without grease, has about the same interface thermal resistance as greased mica for the TO-220 package.

Figure 5-7. Interface Thermal Resistance Using Different Insulating Materials as a Function of Mounting Screw Torque

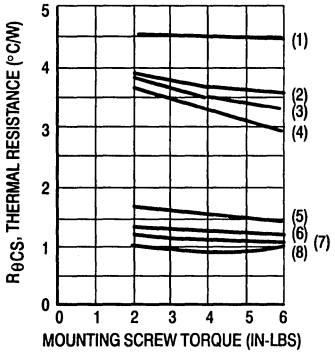


(a) TO-204AA (TO-3) Without Thermal Grease

(1) **Thermalfilm,** .002 (.05) thick
(2) **Mica,** .003 (.08) thick
(3) **Mica,** .002 (.05) thick
(4) **Hard anodized,** .020 (.51) thick
(5) **Aluminum oxide,** .062 (1.57) thick
(6) **Berylium oxide,** .062 (1.57) thick
(7) **Bare joint** — no finish
(8) **Grafoil,** .005 (.13) thick*
*Grafoil is not an insulating material

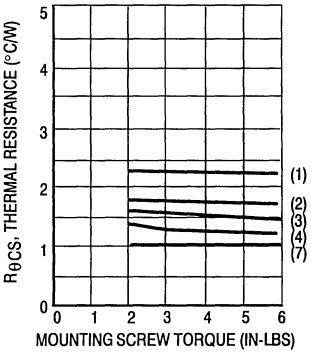


(b) TO-204AA (TO-3) With Thermal Grease



(c) TO-220 Without Thermal Grease

(1) **Thermalfilm,** .022 (.05) thick
(2) **Mica,** .003 (.08) thick
(3) **Mica,** .002 (.05) thick
(4) **Hard anodized,** .020 (.51) thick
(5) **Thermalsil II,** .009 (.23) thick
(6) **Thermalsil II,** .006 (.15) thick
(7) **Bare joint** — no finish
(8) **Grafoil,** .005 (.13) thick*
*Grafoil is not an insulating material



(d) TO-220 With Thermal Grease

Data Courtesy of Thermalloy

3

A number of manufacturers offer silicone rubber insulators. Table 5-2 shows measured performance of a number of these insulators under carefully controlled, nearly identical conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out-of-flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K-10 pad, for example, is described as having about 2/3 the interface resistance of the Sil Pad 1000 which would place its performance close to the Chomerics 1671 pad. AAVID also offers an isolated pad called Rubber-Duc, however it is only available vulcanized to a heatsink and therefore was not included in the comparison. Published data from AAVID shows $R\theta CS$ below 0.3°C/W for pressures above 500 psi. However, surface flatness and other details are not specified so a comparison cannot be made with other data in this note.

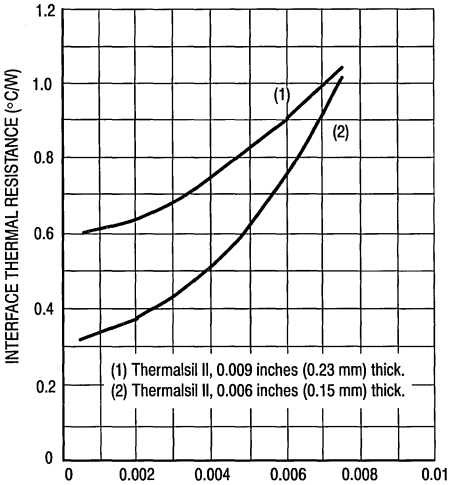
Table 5-2. Thermal Resistance of Silicone Rubber Pads

Manufacturer	Product	$R\theta CS$ @ 3 Mils*	$R\theta CS$ @ 7.5 Mils*
Wakefield	Delta Pad 173-7	0.790	1.175
Bergquist	Sil Pad K-4	0.752	1.470
Stockwell Rubber	1867	0.742	1.015
Bergquist	Sil Pad 400-9	0.735	1.205
Thermalloy	Thermalsil II	0.680	1.045
Shin-Etsu	TC-30AG	0.664	1.260
Bergquist	Sil Pad 400-7	0.633	1.060
Chomerics	1674	0.592	1.190
Wakefield	Delta Pad 174-9	0.574	0.755
Bergquist	Sil Pad 1000	0.529	0.935
Ablestik	Thermal Wafers	0.500	0.990
Thermalloy	Thermalsil III	0.440	1.035
Chomerics	1671	0.367	0.655

*Test Fixture Deviation from flat Thermalloy EIR86-1010.

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO-204AA (TO-3) package insulated with Thermasil is shown on Figure 5-8. Observe that the "worst case" encountered (7.5 mils) yields results having about twice the thermal resistance of the "typical case" (3 mils), for the more conductive insulator. In order for Thermasil III to exceed the performance of greased mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.

Figure 5-8. Effect of Total Surface Flatness on Interface Resistance Using Silicon Rubber Insulators



Data Courtesy of Thermalloy

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the Cho-Therm 1688 pad thermal interface impedance dropped from 0.90°C/W to 0.70°C/W at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R\theta_{CS}$ measured 0.74°C/W. The torque on the conventional mounting hardware had decreased to 3 in-lb from an initial 6 in-lb. With non-conformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Table 5-3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing ASTM Committee D9 is developing a standard for interface measurements.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will out perform the commonly used mica with grease. Cost may be a determining factor in making a selection.

Table 5-3. Performance of Silicon Rubber Insulators Tested per MIL-I-49456

Material	Measured Thermal Resistance (°C/W)	
	Thermalloy Data(1)	Bergquist Data(2)
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	—
Cho-Therm, 1617	0.233	—
Q Pad (non-insulated)	—	0.009
Sil-Pad, K-10	0.263	0.200
Thermasil III	0.267	—
Mica, greased	0.329	0.400
Sil-Pad 1000	0.400	0.300
Cho-therm 1674	0.433	—
Thermasil II	0.500	—
Sil-Pad 400	0.533	0.440
Sil-Pad K-4	0.583	0.440

(1) From Thermalloy EIR 87-1030
(2) From Bergquist Data Sheet

Insulation Resistance

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly, so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi-pot testing should be done on prototypes and a large margin of safety employed.

Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost-effective insulated packages since the 1950s. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late eighties, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The second category contains parts which have a plastic overmold covering the metal mounting base. The Full Pak (Case 221C) illustrated in Figure 5-13, is an example of parts in the second category.

Parts in the first category — those with an exposed metal flange or tab — are mounted the same as their non-insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the overmolded type should be used with a conical compression washer, described later in this note.

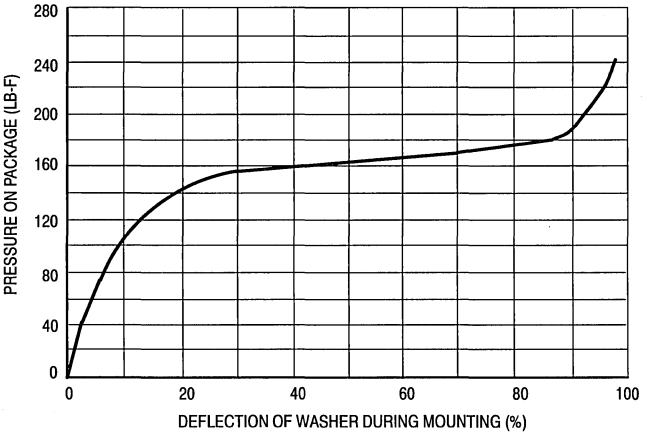
Fastener and Hardware Characteristics

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 5-9, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection — generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A new variation of the conical washer includes it as part of a nut assembly. Called a Sync Nut, the patented device can be soldered to a PC board and the semiconductor mounted with a 6-32 machine screw.(4)

Figure 5-9. Characteristics of the Conical Compression Washers Designed for Use with Plastic Body Mounted Semiconductors



(4) ITW Shakeproof, St. Charles Road, Elgin, IL 60120.

Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small board-mounted or free-standing heat dissipators with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO-220 and TO-126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO-220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

Machine Screws

Machine screws, conical washers, and nuts (or sync-nuts) can form a trouble-free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case may occur.

Self-Tapping Screws

Under carefully controlled conditions, sheet metal screws are acceptable. However, during the tapping process with a standard screw, a volcano-like protrusion will develop in the metal being threaded; an unacceptable surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speed nut. If a self tapping process is desired, the screw type must be used which roll-forms machine screw threads.

Rivets

Rivets are not a recommended fastener for any of the plastic packages. When a rugged metal flange-mount package is being mounted directly to a heatsink, rivets can be used provided press-riveting is used. Crimping force must be applied slowly and evenly. Pop-riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional belt-furnace, irons, vapor-phase reflow, and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

Adhesives

Adhesives are available which have coefficients of expansion compatible with copper and aluminum.(5) Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non-field-serviceable systems or low strength types for field-serviceable systems. Adhesive bonding is attractive when case mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

Plastic Hardware

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.

Fastening Techniques

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel or gold-plated. Consequently, precautions must be taken not to mar the finish.

Another factor to be considered is that when a copper based part is rigidly mounted to an aluminum heatsink, a bimetallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminum, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws the semiconductor chip could be damaged. Bending can be minimized by:

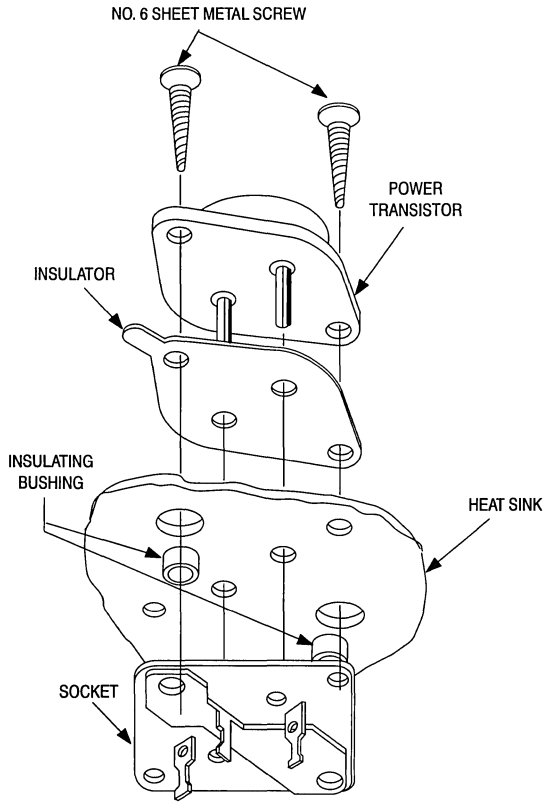
1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some slip between surfaces can occur as temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semiconductor to minimize the temperature gradient and allow for movement.

Flange Mount

Few known mounting difficulties exist with the smaller flange mount packages, such as the TO-204 (TO-3). The rugged base and distance between die and mounting hose combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. It is therefore good practice to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger-tight the hardware should be torqued to its final specification in at least two sequential steps. A typical mounting installation for a popular flange type part is shown in Figure 5-10. Machine screws (preferred), self-tapping screws, islets or rivets may be used to secure the package using guidelines in the previous section, (**Fastener and Hardware Characteristics**).

(5) Robert Batson, Elliot Fraunglass and James P. Moran, *Heat Dissipation Through Thermalloy Conductive Adhesives*, EMTAS '83 Conference, February 1–3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI 48128.

Figure 5-10. Hardware Used for a TO-204AA (TO-3) Flange Mount Part



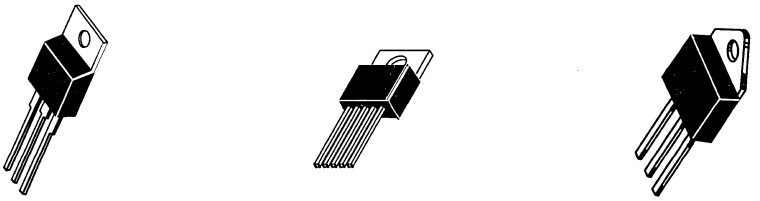
Tab Mount

The tab mount class is composed of a wide array of packages as illustrated in Figure 5-11. Mounting considerations for all varieties are similar to that for the popular TO-220 package, whose suggested mounting arrangements and hardware are shown in Figure 5-12. The rectangular washer shown in Figure 5-12a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is suggested when using a 6-32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, Motorola TO-220 packages have a chamfer on one end. TO-220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

The popular TO-220 package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure B1.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab.(6) In addition, it separates the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 5-14(c). To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

Figure 5-11. Several Types of Tab Mounted Parts



CASE 221A (TO-220AB) **CASE 314D** **CASE 340 (TO-218)**

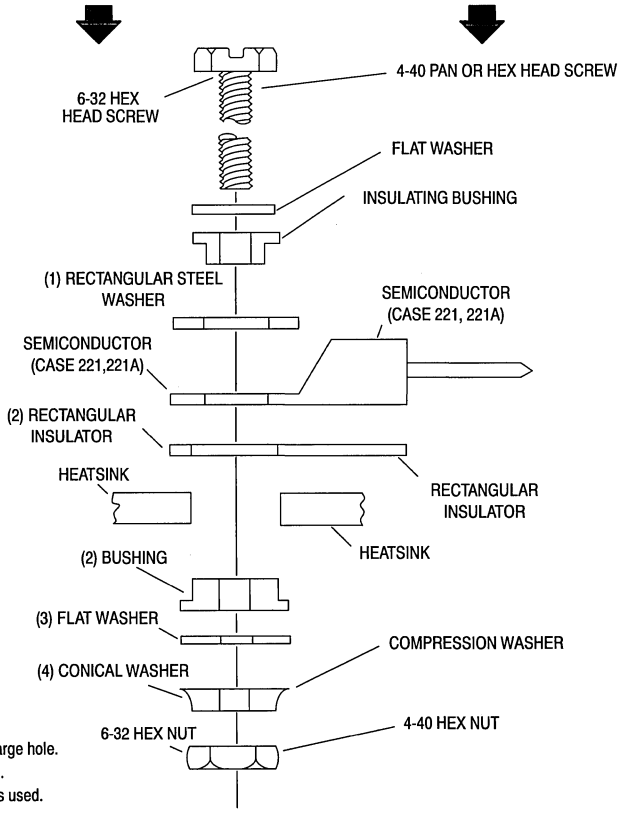
Figure 5-12. Mounting Arrangements for Tab Mount TO-220

a) Preferred Arrangement for Isolated or Non-isolated Mounting. Screw is at Semiconductor Case Potential. 6-32 Hardware is Used.

Choose from Parts Listed Below.

b) Alternate Arrangement for Isolated Mounting when Screw must be at Heatsink Potential. 4-40 Hardware is Used.

Use Parts Listed Below.



(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing is used.

(6) Catalog, Edition 18, Richco Plastic Company, 5825 N. Tripp Ave., Chicago, IL 60546.

Plastic Body Mount

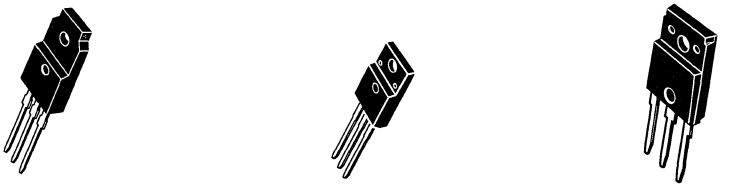
The Full Pak plastic power packages shown in Figure 5-13 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance.

The Full Pak (Case 221C) is similar to a TO-220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO-220 and is similar to that of the Thermopad.

Several types of fasteners may be used to secure these packages; machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air-driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 5-9.

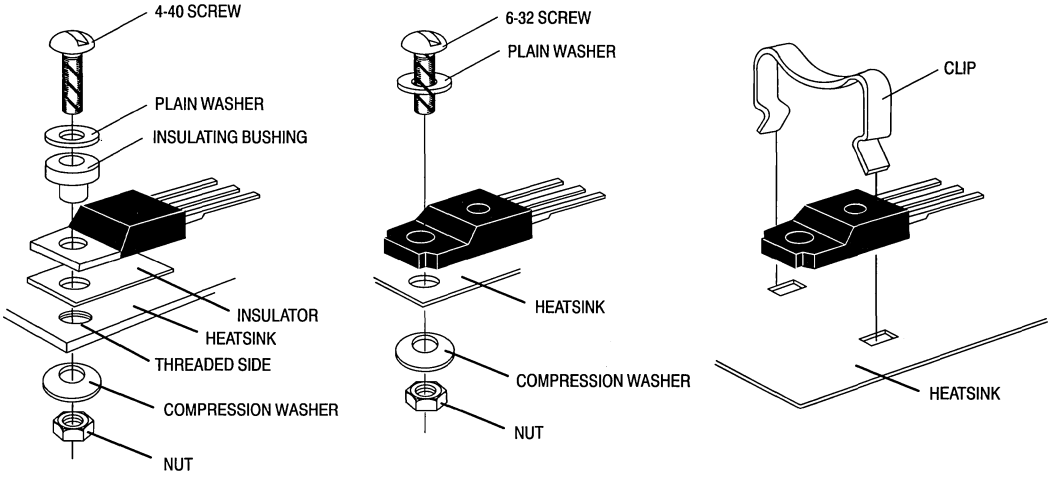
The Full Pak (Case 221C, 221D and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO-220. As shown in Figure 5-14(c), one properly chosen clip, inserted into two slotted holes in the heatsink, is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure B1 of Appendix B.) The interface should consist of a layer of thermal grease or a highly conductive thermal pad. Of course, screw mounting shown in Figure 5-14(b) may also be used but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO-220 package which is shown in Figure 5-14(a).

Figure 5-13. Plastic Body Mounted Packages



CASE 221C (Full Pak) | **CASE 221D (Full Pak)** | **CASE 340B (Full Pak)**

Figure 5-14. Mounting Arrangements for the Full Pak as Compared to a Conventional TO-220



(a) Screw Mounted TO-220 | **(b) Screw Mounted Full Pak** | **(c) Clip Mounted Full Pak**

Surface Mount

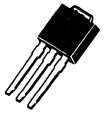
Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 5-15, for example, will accommodate a die up to 112 mils × 112 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resistance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.

Standard Glass-Epoxy 2-ounce boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 5-16 shows, thermal resistance assymtotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

Boards are offered that have thick aluminum or copper substrates. A dielectric coating designed for low thermal resistance is overlayed with one or two ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type.(7) The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

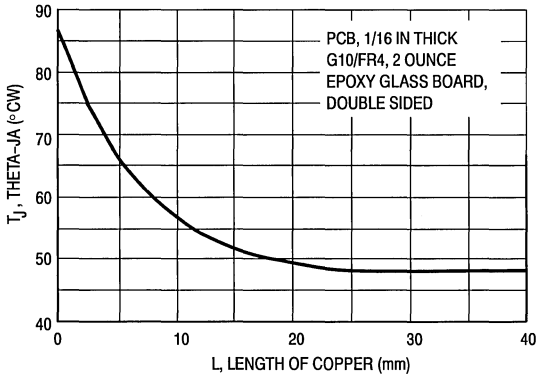
Figure 5-15. Surface Mounted DPAK Packages



CASE 369

CASE 369A

Figure 5-16. Effect of Footprint Area on Thermal Resistance of DPAK Mounted on a Glass-Epoxy Board



(7) Herb Fick, *Thermal Management of Surface Mount Power Devices*, Powerconversion and Intelligent Motion, August 1987.

Free Air and Socket Mounting

In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice however, it is better to support the package. A plastic support for the TO-220 Package and other similar types is offered by heatsink accessory vendors.

In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from Motorola. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

Connecting and Handling Terminals

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions as a result of thermal cycling over operating temperature extremes must be considered. Standard metal, plastic, and RF stripline packages each have some special considerations.

Metal Packages

The pins of metal packaged devices using glass to metal seals are not designed to handle any significant bending or stress. If abused, the seals could crack. Wires may be attached using sockets, crimp connectors or solder, provided the data sheet ratings are observed. When wires are attached directly to the pins, flexible or braided leads are recommended in order to provide strain relief.

Plastic Packages

The leads of the plastic packages are somewhat flexible and can be reshaped although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead-bending unnecessary. Numerous lead and tab-forming options are available from Motorola on large quantity orders. Preformed leads remove the users risk of device damage caused by bending.

If, however, lead-bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A leadbend radius greater than 1/32 inch for TO-220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case.

Cleaning Circuit Boards

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol and unchlorinated freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline and chlorinated freon may cause the encapsulant to swell, possibly damaging the transistor die.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free-standing without support.

3

Thermal System Evaluation

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see Motorola Application Note, AN569.

Other applications, notably switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where, T_J = junction temperature (°C),
T_C = case temperature (°C),
$R_{\theta JC}$ = thermal resistance junction-to-case as specified on the data sheet (°C/W),
P_D = power dissipated in the device (W).

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

Substitution

This method is based upon substituting an easily measurable, smooth DC source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the "test" position, the device under test is connected to a DC power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The DC supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The DC voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

Appendix A
Thermal Resistance Concepts

The basic equation for heat transfer under steady-state conditions is generally written as:

$$q = hA\Delta T \quad (1)$$

where, q = rate of heat transfer or power dissipation (P_D),
h = heat transfer coefficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

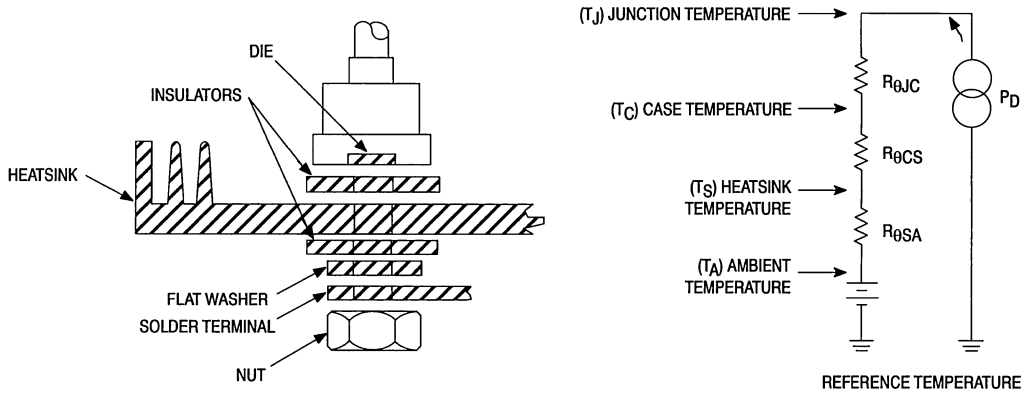
However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance (R_θ) is

$$R_\theta = \Delta T/q = 1/hA \quad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that T could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A-1.

Figure A-1. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor



The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D(R_\theta JC + R_\theta CS + R_\theta SA) + T_A \quad (3)$$

where, T_J = junction temperature,
P_D = power dissipation,
$R_\theta JC$ = semiconductor thermal resistance (junction-to-case),
$R_\theta CS$ = interface thermal resistance (case-to-heatsink),
$R_\theta SA$ = heatsink thermal resistance (heatsink-to-ambient),
T_A = ambient temperature.

The thermal resistance junction-to-ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance ($R_\theta CS$) may be significant compared to the other thermal resistance terms. A proper mounting procedure can minimize $R_\theta CS$.

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications such as in RF power amplifiers and short-pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.

Appendix B
Measurement of Interface Thermal Resistance

Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring DC power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

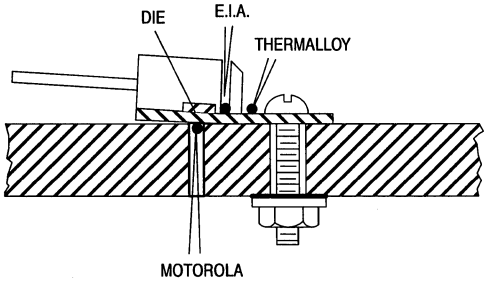
When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO-204AA package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL-I-49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is "application oriented."

Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The Motorola fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path.

As described previously, some packages, such as a TO-220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15% to 20% error in $R_{\theta CS}$ can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure the semiconductor case temperature. Consider the TO-220 package shown in Figure B-1. The mounting pressure at one end causes the other end — where the die is located — to lift off the mounting surface slightly. To improve contact, Motorola TO-220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure.

B-1. JEDEC TO-220 Package Mounted to Heatsink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End



Three thermocouple locations are shown.

a) The Motorola location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

b) The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

c) The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

Temperatures at the three locations are generally not the same. Consider the situation depicted in Figure B-1. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the Motorola location is even hotter. Since junction-to-sink thermal resistance must be constant for a given test setup, the calculated junction-to-case thermal resistance values decrease and case-to-sink values increase as the case temperature thermocouple readings become warmer. Thus the choice of reference point for the case temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower but close to the temperature at the EIA location as the lateral heat flow is generally small. The Motorola location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The Motorola location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO-220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified junction-to-case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heatsink. The washer is flat to within 1.0 mil/inch, has a finish better than 63 μin., and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application-oriented. It is also easy to use but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction-to-case thermal resistance while testing for interface thermal resistance. If the junction-to-case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

SECTION 6
LINEAR REGULATOR DESIGN EXAMPLE

3

As an illustration of the use of the material contained in the preceding sections, the following regulator design example is given.

Regulator Performance Requirements:

Output Voltage, V_O = +10 V ± 0.1 V
Output Current, I_O = 1.0 A, current limited
Load Regulation, ≤ 0.1% for I_O = 10 mA to 750 mA
Line Regulation, ≤ 0.1%
Output ripple, ≤ 2.0 mVp-p
Max Ambient Temperature, T_A ≤ +70°C
Supply will have common loads to a negative supply.

1. IC Regulator Selection

Study of the available regulators given in the selection guide reveals that the MC1723C would meet the regulation performance requirements. This regulator must be current boosted to obtain the required 1.0 A output current. A rough cost estimate shows that an MC1723C series pass element combination is the most economical approach.

2. Circuit Configuration

In Section 3, an appropriate circuit configuration is found. This is the MC1723C NPN boost configuration of Figure 3-4A.

3. Determination of Component Values

Using the equations given in Figure 3-4A, the values of C_{ref}, R_1, R_2, R_3 and R_{SC} are determined.

a) C_{ref} is chosen to be 0.1 μF for low noise operation.

b) $R_1 + R_2$ is chosen to be ≈ 10 k.

c) R_2 is then given by: $R_2 \approx \frac{7.0\ V}{V_O} (R_1 + R_2) = 0.7\ (10\ k) = 7.0\ k$

d) Since V_{ref} can vary by as much as ± 5% for the MC1723C, R_2 should be made variable by at least that much, so that V_O can be set to the required value of +10 V ± 0.1 V. R_2 is therefore chosen to consist of a 62 k resistor and a 2.0 k trimpot.

e) $R_1 = 10\ k - R_2 = 10\ k - 7.0\ k = 3.0\ k$

f) $R_{SC} \approx \frac{0.6\ V}{I_{SC}} = \frac{0.6\ V}{1.0\ A} = 0.6\ \Omega$; 0.56 Ω, 1.0 W chosen for R_{SC}.

g) $R_3 = R_1 \,||\, R_2 \cong 2.2\ k$

4. Determination of Input Voltage, V_{in}

There are two basic constraints on the input voltage: (1) the device limits for minimum and maximum V_{in} and (2) the minimum input-output voltage differential. These limits are found on the device data sheet to be:

$$9.5\ V \le V_{in} \le 40\ V \text{ and } (V_{in} - V_O) \ge 3.0\ V$$

For the configuration of Figure 3-5A, $(V_{in} - V_O)$ is given by:

$$(V_{in} - V_O) = [V_{in} - (V_O + 2\phi)] \ge 3.0\ V, \text{ where } \phi = V_{BEon} \approx 0.6\ V$$

Note that $(V_{in} - V_O)$ is defined on the device data sheet to be the differential between the input and output pins. Since the base-emitter junction drops of Q1 and R_{SC} have been added to the circuit, they must be added to the minimum value of $(V_{in} - V_O)$. Therefore,

$$V_{in} \ge V_O + 2\phi + 3.0\ V = 10 + 1.2 + 3$$

$$V_{in} \ge 14.2\ V$$

This condition also satisfies the requirement for a minimum V_{in} of 9.5 V.

In order to simplify the design of the input supply (see Section 8), V_{in} is chosen to be 16 V average with a 3.0 Vp-p ripple at full load and up to 25 V at no load. This assures that the input voltage is always above the required minimum value of 14.2 V. Now, the output ripple can be determined. The MC1723C has a typical ripple rejection ratio of –74 db, as given on its data sheet. With an input ripple of 3.0 Vp-p, the output ripple would be less than 1.0 mVp-p, which meets the regulator output ripple requirements.

5. Selection of the Series Pass Element, Q1

The transistor type chosen for Q1 must have the following characteristics (see Section 4):

a) $V_{CEO} \ge V_{in(max)}$

b) $I_{C(max)} \ge I_{SC}$

c) $h_{fe} \ge \frac{I_{SC}}{I_O}$ @ $V_{CE} = V_{in} - V_O - \phi$, where $\phi = V_{BEon} \approx 0.6\ V$

d) $P_{D(max)} \ge V_{in,} \times I_{SC}$

e) θ_{JC} such to allow practical heatsinking

f) SOA such that it can withstand $V_{CE} = V_{in}$ @ $I_C = I_{SC}$

For this example: $V_{CEO} \ge 25\ V$

$I_{C(max)} \ge 1.0\ A$

$h_{fe} \ge 25$ @ $V_{CE} = 5.0\ V$ @ $I_C = 1.0\ A$

$P_{D(max)} \ge 16\ W$

$\theta_{JC} = 1.52°C/W$

SOA = 1.0 A @ 16 V

A 2N3055 transistor is chosen as a suitable device for Q1 using the selection guide of Section 4 and the transistor data sheets (available from the device manufacturer).

6. Q1 Heatsink Calculation

$$T_J = T_A + P_D\,\theta_{JA} \text{ (Eq 15.1 from Section 15)}$$

where, $P_D = V_{in} \times I_{SC}$

$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ (Eq 6.2)

Solving for θ_{SA}:

$$\theta_{SA} = \left[\frac{T_J - T_A}{P_D}\right] - (\theta_{JC} + \theta_{CS}) \qquad (6.2)$$

From the 2N3055 data sheet, $T_J = 200°C$ and $\theta_{JC} = 1.52°C/W$. The transistor will be mounted with thermal grease directly to the heatsink. Therefore, θ_{CS} is found to be 0.1°C/W from Table 15-1.
Solving (Eq. 6.2):

$$\theta_{SA} = \left[\frac{200°C - 70°C}{16\ V \times 1.0\ A}\right] - (1.52 + 0.1)\ °C/W$$

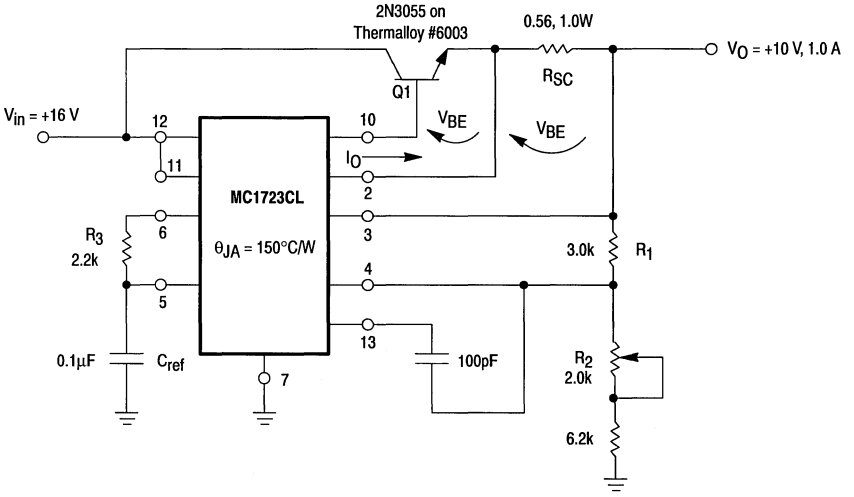
$$\leq 6.6°C/W$$

A commercial heatsink is now chosen from Table 15-2 or one custom designed using the methods given in Section 15. For this example, a Thermalloy #6003 heatsink, having a θ_{CS} of 6.2°C/W, was used.

7. Clamp Diode

Since the regulator can power a load which is also connected to a negative supply, a 1N4001 diode is connected to the output for protection. The complete circuit schematic is shown in Figure 6-1.

Figure 6-1. +10 V, 1.0 A Design Example



8. Construction Input Supply Design

The input supply is now designed using the information contained in Section 8 and the regulator circuit is constructed using the guidelines given in Section 5.

SECTION 7

LINEAR REGULATOR CIRCUIT TROUBLESHOOTING CHECKLIST

Occasionally, the designer's prototype regulator circuit will not operate properly. If problems do occur, the trouble can be traced to a design error in 99.9% of the cases. As a troubleshooting aid to the designer, the following guide is presented.

Of course, it would be difficult, if not impossible, to devise a troubleshooting guide which would cover all possible situations. However, the checklist provided will help the designer pinpoint the problem in the majority of cases. To use the guide, first locate the problem's symptom(s) and then carefully recheck the regulator design in the area indicated using the information contained in the referenced handbook section.

If, after carefully rechecking the circuit, the designer is not successful in resolving the problem, seek assistance from the factory by contacting the nearest Motorola Sales office.

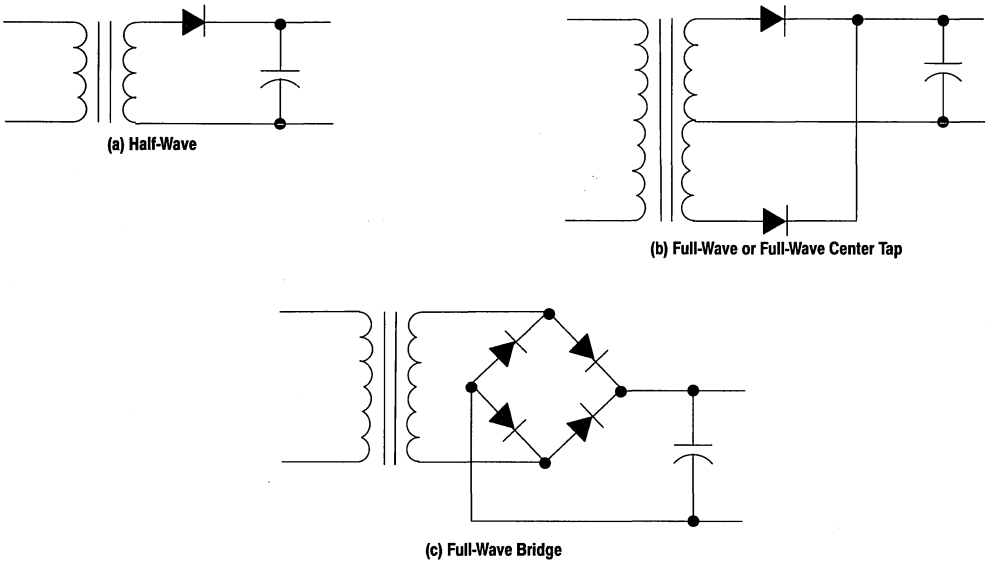
SYMPTOMS	DESIGN AREA TO CHECK	SECTION
Regulator oscillates	1. Layout 2. Compensation capacitor too small 3. Input leads not bypassed 4. External pass element parasitically oscillating	5 3 5 5
Loss of regulation at light loads	1. Emitter-Base resistor in "PNP" type boost configuration too large 2. Absence of 1.0 mA "minimum" load (see load regulation test spec on device data sheet) 3. Improper circuit configuration	4 3
Loss of regulation at heavy loads	1. Input Voltage too low [$V_{in(min)}$, $\lvert V_{in} - V_O \rvert_{min}$] 2. External pass element gain too low 3. Current limit too low 4. Line resistance between sense points and load 5. Inadequate heatsinking	2, 3 4 3 5 15
IC Regulator or Pass Element fails after warm-up or at high T_A	1. Inadequate heatsinking 2. Input Voltage Transient $V_{in(max)}$, V_{CEO}	15 2, 4, 5
Pass Element fails during short circuit	1. Insufficient pass element ratings SOA, $I_{C(max)}$ 2. Inadequate heatsinking	4 15
IC Regulator fails during short circuit	1. IC current or SOA capability exceeded 2. Inadequate heatsinking	2
IC Regulator fails during power-up	1. Input voltage transient $V_{in(max)}$ 2. IC current or SOA capability exceeded as load (capacitor) is charged up.	2 2
IC Regulator fails during power-down	1. Regulator reverse biased	3
Output Voltage does not come up during power-up or after short circuit	1. Out polarity reversal 2. Load has "latched-up" in some manner (usually seen with op amps, current sources, etc.)	3
Excessive 60 Hz or 120 Hz Output Ripple	1. Input supply filter capacitor ground loop	5

SECTION 8
DESIGNING THE INPUT SUPPLY

3

Most input supplies used to power series pass regulator circuits consist of a 60 Hz, single phase step-down transformer followed by a rectifier circuit whose output is smoothed by a choke or capacitor input filter. The type of rectifier circuit used can be either a half-wave, full-wave, or full-wave bridge type, as shown in Figure 8-1. The half-wave circuit is used in low current applications, while the full-wave is preferable in high-current, low output voltage cases. The full-wave bridge is usually used in all other high-current applications.

Figure 8-1. Rectification Schemes



In this section, specification of the filter capacitor, rectifier and transformer ratings will be discussed. The specifications for the choke input filter will not be considered since the simpler capacitor input type is more commonly used in series regulated circuits. A detailed description of this type of filter can be found in the reference listed at the end of this section.

(1)From O. H. Schade, Proc. IRE, Vol. 31, p. 356, 1943.

1. Design of Capacitor-Input Filters

The best practical procedure for the design of capacitor-input filters still remains based on the graphical data presented by Schade[1] in 1943. The curves shown in Figures 8-2 through 8-5 give all the required design information for half-wave and full-wave rectifier circuits. Whereas Schade originally also gave curves for the impedance of vacuum-tube rectifiers, the equivalent values for semiconductor diodes must be substituted. However, the rectifier forward drop often assumes more significance than the dynamic resistance in low-voltage supply applications, as the dynamic resistance can generally be neglected when compared with the sum of the transformer secondary-winding resistance plus the reflected primary-winding resistance. The forward drop may be of considerable importance, however, since it is about 1.0 V, which clearly cannot be ignored in supplies of 12 V or less.

Figure 8-2. Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Half-Wave Capacitor-Input Circuits

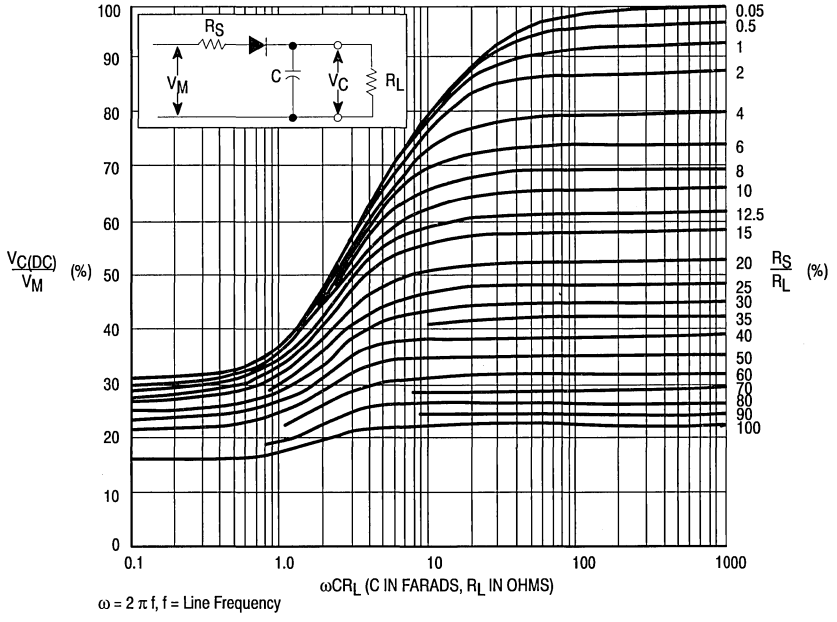
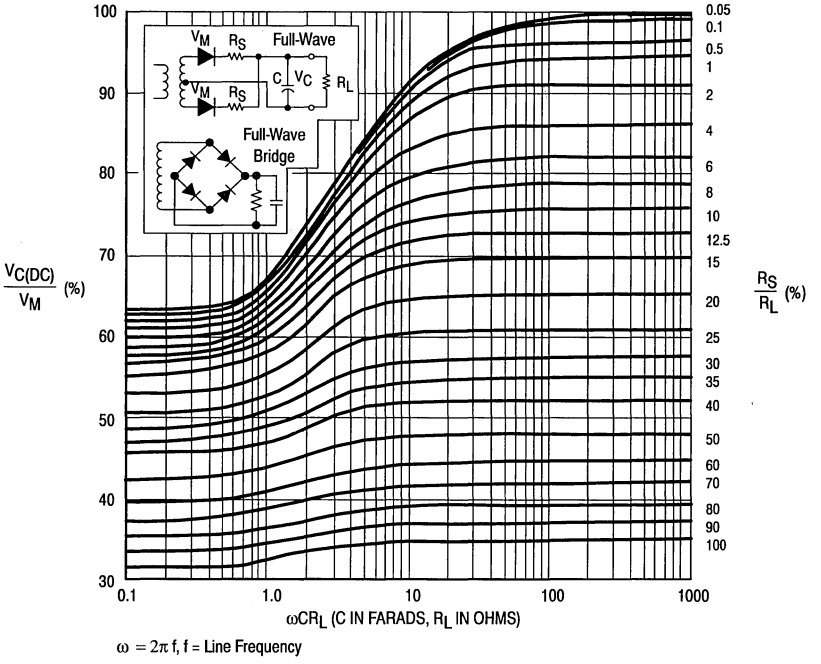
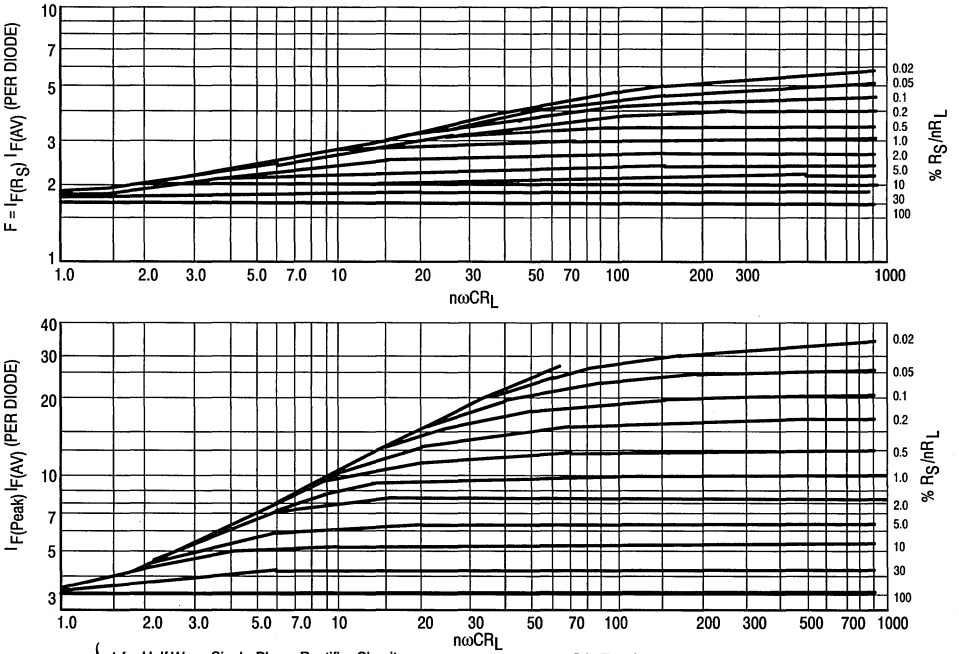


Figure 8-3. Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Full-Wave Capacitor-Input Circuits



$\omega = 2\pi f$, f = Line Frequency

Figure 8-4. Relation of RMS and Peak-to-Average Diode Current in Capacitor-Input Circuits



n = { 1 for Half-Wave Single-Phase Rectifier Circuits
2 for Full-Wave Single-Phase Rectifier Circuits

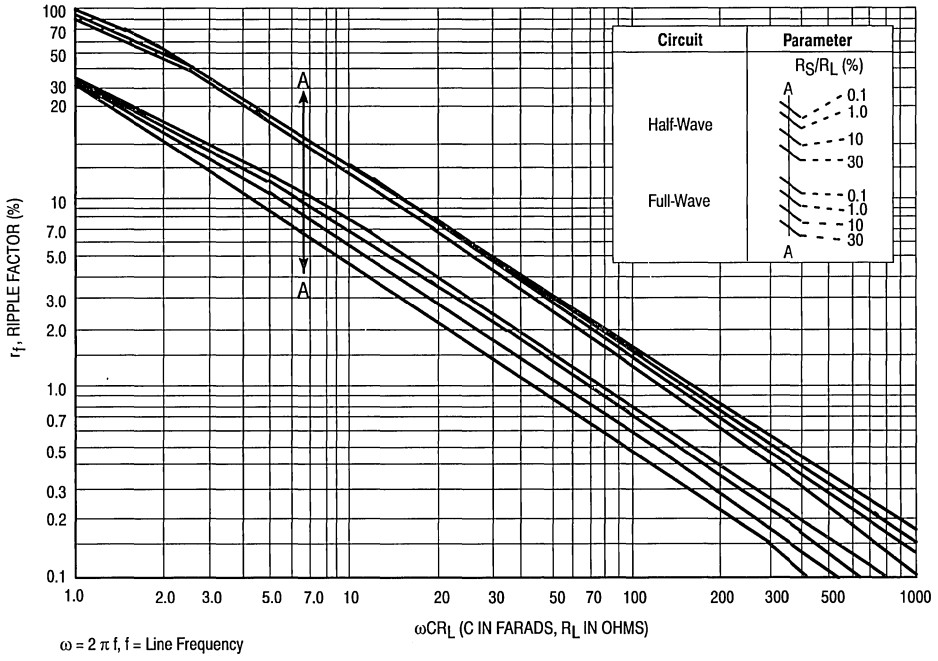
$\omega = 2\pi f$, where f = Line Frequency

C in Farads

R_L in Ohms

R_S = RMS Equivalent Source Resistance

Figure 8-5. Root-Mean-Square Ripple Voltage for Capacitor-Input Circuits



Returning to the above curves, the full-wave circuit will be considered. Figure 8-3 shows that a circuit must operate with $\omega C R_L \geq 10$ in order to hold the voltage reduction to less than 10% and $\omega C R_L \geq 40$ to obtain less than 2.0% reduction. However, it will also be seen that these voltage reduction figures require R_S/R_L, where R_S is now the total series resistance, to be about 0.1% which, if attainable, causes repetitive peak-to-average current ratios from 10 to 17 respectively, as can be seen from Figure 8-4. These ratios can be satisfied by many diodes; however, they may not be able to tolerate the turn-on surge current generated when the input-filter capacitor is discharged and the transformer primary is energized at the peak of the input waveform. The rectifier is then required to pass a surge current determined by the peak secondary voltage less the rectifier forward drop and limited only by the series resistance R_S. In order to control this turn-on surge, additional resistance must often be provided in series with each rectifier. It becomes evident, then, that a compromise must be made between voltage reduction on the one hand and diode surge rating and hence average current-carrying capacity on the other hand. If small voltage reduction, that is good voltage regulation, is required, a much larger diode is necessary than that demanded by the average current rating.

Surge Current

The capacitor-input filter allows a large surge to develop, because the reactance of the transformer leakage inductance is rather small. The maximum instantaneous surge current is approximately V_M/R_S and the capacitor charges with a time constant $\tau \approx R_S C_1$. As a rough — but conservative — check, the surge will not damage the diode if V_M/R_S is less than the diode I_{FSM} rating and τ is less than 8.3 ms. It is wise to make R_S as large as possible and not pursue tight voltage regulation; therefore, not only will the surge be reduced but rectifier and transformer ratings will more nearly approach the DC power requirements of the supply.

2. Design Procedure

A) From the regulator circuit design (see Section 6), we know:

$V_{C(DC)}$ = the required full load average DC output voltage of the capacitor input filter
$V_{Ripple(p-p)}$ = the maximum no load peak-to-peak ripple voltage
V_m = the maximum no load output voltage
I_O = the full-load filter output current
f = the input AC line frequency

3

B) From Figure 8-5, we can determine a range of minimum capacitor values to obtain sufficient ripple attenuation. First determine r_f:

$$r_f = \frac{V_{Ripple(p-p)}}{2\sqrt{2}\,V_{C(DC)}} \times 100\% \qquad (8.1)$$

A range for $\omega C R_L$ can now be found from Figure 8-5.

C) Next, determine the range of R_S/R_L from Figure 8-2 or 8-3 using $V_{C(DC)}$ and the values for $\omega C R_L$ found in part B. If the range of $\omega C R_L$ values initially determined from Figure 8-5 is above $\simeq 10$, R_S/R_L can be found from Figures 8-2 and 8-3 using the lowest $\omega C R_L$ value. Otherwise, several iterations between Figures 8-2 or 8-3 and 8-5 may be necessary before an exact solution for R_S/R_L and $\omega C R_L$ for a given r_f and $V_{C(DC)}/V_m$ can be found.

D) Once $\omega C R_L$ is found, the value of the filter capacitor (C) can be determined from:

$$C = \frac{\omega C R_L}{2\pi f \left(\frac{V_{C(DC)}}{I_O}\right)} \qquad (8.2)$$

E) The rectifier requirements may now be determined:

1. Average current per diode;

$$I_{F(avg)} = I_O \text{ for half-wave rectification} = I_O/2 \text{ for full-wave rectification} \qquad (8.3)$$

2. RMS and Peak repetitive rectifier current ratings can be determined from Figure 8-4.
3. The rectifier PIV rating is 2 V_m for the half-wave and full-wave circuits, V_m for the full-wave bridge circuit. In addition, a minimum safety margin of 20% to 50% is advisable due to the possibility of line transients.
4. Maximum surge current, $I_{surge} = V_m/(R_S + ESR)$ (8.4)
   where, ESR = minimum equivalent series resistance of filter capacitor from its data sheet.

F) Transformer Specification

1. Secondary leg RMS voltage, $V_S = \{V_m + (n)\ 1.0\}/\sqrt{2}$ (8.5)
   where; n = 1 for half-wave and full-wave
   n = 2 for full-wave bridge
2. Total resistance of secondary and any external resistors to be equal to R_S found from Figures 8-2, 8-3, and 8-4 (see Part C).
3. Secondary RMS current;

$$\text{half-wave} = I_{rms} \quad \text{full-wave} = I_{rms} \quad \text{full-wave bridge} = \sqrt{2}\, I_{rms} \qquad (8.6)$$

   where, I_{rms} = rms rectifier current (from part E.1 and E.2).
4. Transformer VA rating;

$$\text{half-wave} = V_S I_{rms} \quad \text{full-wave} = 2 V_S I_{rms} \quad \text{full-wave bridge} = V_S I_{rms} (\sqrt{2}) \qquad (8.7)$$

   where, I_{rms} = rms rectifier current (from part E.1 and E.2) and, V_S = secondary leg RMS voltage.

3. Design Example

A) Find the values for the filter capacitor, transformer rectifier ratings, given:
Full-Wave Bridge Rectification;

$$V_{C(DC)} = 16\ V$$
$$V_{Ripple(p\text{-}p)} = 3.0\ V$$
$$V_M = 25\ V$$
$$I_O = 1.0\ A$$
$$f = 60\ Hz$$

B) Using Equation (8.1),

$$r_f = \frac{3}{2\sqrt{2}\,(16)} \times 100\% = 6.6\%$$

from Figure 8.5, $\omega C R_L \simeq 7$ to 15

C) Using $\omega C R_L = 10$, R_S/R_L is found from Figure 8-3 using,

$$\frac{V_{C(DC)}}{V_M} = \frac{16}{25} = 0.64 = 64\%$$

$$R_S/R_L = 20\% \text{ or } R_S = 0.2 \times R_L = 0.2\left(\frac{V_{C(DC)}}{I_O}\right) = 0.2\,(16)$$

$$R_S = 3.2\ \Omega$$

D) From Equation (8.2), the filter capacitor size is found:

$$C = \frac{\omega C R_L}{2\pi f\left(\frac{V_{C(DC)}}{I_O}\right)} = \frac{10}{2\pi f(60)16} = 1658\ \mu F$$

E) The rectifier ratings are now specified:
1. $I_{F(avg)} = I_O/2 = 0.5$ A from Equation (8.3)
2. $I_{F(rms)} = 2 \times I_{F(AVG)} = 1.0$ A from Figure 8-4
3. $I_{F(Peak)} = 5.2 \times I_{F(AVG)} = 2.6$ A from Figure 8-4
4. $PIV = V_M = 25$ V (use 50 V for safety margin)
5. $I_{surge} = V_M/(R_S + ESR) \simeq 25/3.2 = 7.8$ A from Equation (8.4) (neglecting capacitor ESR)

F) The transformer should have the following ratings:
1. $V_S = \{V_M + n(1.0)\}/\sqrt{2} = (25 + 2)/\sqrt{2} = 19$ VRMS {from Equation (8.5)}
2. Secondary Resistance should be 3.2 Ω
3. Secondary RMS current rating should be 1.4 A {from Equation (8.6)}
4. From Equation (8.7), the transformer should have a 27 VA rating.

It should be noted that, in order to simplify the procedure, the above design does not allow for line voltage variations or component tolerances. The designer should take these factors into account when designing his input supply. Typical tolerances would be: line voltage = +10% to −15% and filter capacitors = +75% to −10%.

REFERENCES
1. O. H. Schade, Proc. IRE, Vol. 31, 1943.
2. Motorola Silicon Rectifier Manual, 1980.

SECTION 9
AN INTRODUCTION TO SWITCHING POWER SUPPLIES

3

The Switching Power Supply continues to increase in popularity and is one of the fastest growing markets in the world of power conversion. Its performance and size advantages meet the needs of today's modern and compact electronic equipment and the increasing variety of components directed at these applications makes new designs even more practical.

This guide is intended to provide the designer with an overview of the more popular inverter circuits, their basic theory of operation, and some of the subtle characteristics involved in selecting a circuit and the appropriate components. Also included are valuable design tips on both the major passive and active components needed for a successful design. Finally, a complete set of selector guides to Motorola's Switchmode components is provided which gives a detailed listing of the industry's most comprehensive line of semiconductor products for switching power supplies.

Comparison with Linear Regulators

The primary advantages of a switching power supply are efficiency, size,and weight. It is also a more complex design, cannot meet some of the performance capabilities of linear supplies and generates a considerable amount of electrical noise. However switchers are being accepted in the industry, particularly where size and efficiency are of prime importance. Performance continues to improve and for most applications they are usually cost competitive down to the 20 W power level.

In the past the switcher's advantage versus the linear regulator was in the high power arena where passive components such as transformers and filters were small compared to the linear regulator at the same power level. However, active component count was high and tended to make the switcher less cost effective at low power levels. In recent years, Switchers have been significantly cost reduced because designers have been able to simplify the control circuits with new, cost effective integrated circuits and have found even lower cost alternatives in the passive component area.

A performance comparison chart of switching versus linear supplies is shown in Table 9-1. Switcher efficiencies run from 70% to 80% but occasionally fall to (60%–65%) when linear post regulators are used for the auxiliary outputs. Some linear power supplies on the other hand, are operated with up to 50% efficiency but these are areas where line variations or hold-up time problems are minimal. Most linears operate with typical efficiencies of only 30%. The overall size reduction of a 20 kHz switcher is about 4:1 and newer designs in the 100 kHz to 200 kHz region end up at about 8:1 (versus a linear). Other characteristics such as static regulation specs are comparable, while ripple and load transient response are usually worse. Output noise specs can be somewhat misleading. Very often a 500 mV switching spike at the output may be attenuated considerably at the load itself due to the series inductance of the connecting cables and the additional filter capacitors found in many logic circuits. In the future, the noise generated at higher switching frequencies (100 kHz–500 kHz) will probably be easier to filter and the transient response will be faster. Hold-up time is greater for switchers because it is easier to store energy in high voltage capacitors (200 V–400 V) than in the lower voltage (20 V–50 V) filter capacitors common to linear power supplies. This is due to the fact that the physical size of a capacitor is dependent on its CV product while energy storage is proportional to CV^2.

Table 9-1. 20 kHz Switcher versus Linear Performance

Parameter	Switcher	Linear
Efficiency	75%	30%
Size	2.0 W/in^3	0.5 W/in^3
Weight	40 W/lb	10 W/lb
Line and Load Regulation	0.1%	0.1%
Output Ripple V_{p-p}	50 mV	5.0 mV
Noise V_{p-p}	50 mV to 200 mV	—
Transient Response	1.0 ms	20 μs
Hold-Up Time	20 ms to 30 ms	1.0 ms to 2.0 ms

Basic Configurations

A switching power supply is a relatively complex circuit as is shown by the four basic building blocks of Figure 9-1. It is apparent here that the heart of the supply is really the high frequency inverter. It is here that the work of chopping the rectified line at a high frequency (20 kHz–200 kHz) is done. It is here also that the line voltage is transformed down to the correct output level for use by logic or other electronic circuits. The remaining blocks support this basic function. The 60 Hz input line is rectified and filtered by one block and after the inverter steps this voltage down, the output is again rectified and filtered by another. The task of regulating the output voltage is left to the control circuit which closes the loop from the output to the inverter. Most control circuits generate a fixed frequency internally and utilize pulse width modulation techniques to implement the desired regulation. Basically, the on-time of the square wave drive to the inverter is controlled by the output voltage. As load is removed or input voltage increases,the slight rise in output voltage will signal the control circuit to deliver shorter pulses to the inverter and conversely as the load is increased or input voltage decreases, wider pulses will be fed to the inverter.

The inverter configurations used in today's switchers actually evolved from the buck and boost circuits shown in Figures 9-2a and 9-2b. In each case the regulating means and loop analysis will remain the same but a transformer is added in order to provide electrical isolation between the line and load. The forward converter family which includes the push-pull and half bridge circuits evolved from the buck regulator (Figure 9-2a). And the newest switcher, the flyback converter, actually evolved from the boost regulator. The buck circuit interrupts the line and provides a variable pulse width square wave to a simple averaging LC filter. In this case, the first order approximation of the output voltage is $V_{out} = V_{in} \times$ duty cycle and regulation is accomplished by simply varying the duty cycle. This is satisfactory for most analysis work and only the transformer turns ratio will have to be adjusted slightly to compensate for IR drops, diode drops, and transistor saturation voltages.

Operation of the boost circuit is more subtle in that it first stores energy in a choke and then delivers this energy plus the input line to the load. However, the flyback regulators which evolved from this configuration delivers only the energy stored in the choke to the load. This method of operation is actually based on the buck boost model shown in Figure 9-2c. Here, when the switch is opened, only the stored inductive energy is delivered to the load. The true boost circuit can also regulate by stepping up (or boosting) the input voltage whereas the buck-boost or flyback regulator can step the input voltage up or down. Analysis of the boost regulator begins by dealing with the choke as an energy storage element which delivers a fixed amount of power to the load: $P_O = 1/2\ L\ If_O$ where, I = the peak choke current; f_O = the operating frequency; and, L = the inductance.

Because it delivers a fixed amount of power to the load regardless of load impedance (except for short circuits), the boost regulator is the designer's first choice in photoflash and capacitive-discharge (CD) automotive ignition circuits to recharge the capacitive load. It also makes a good battery charger. For an electronic circuit load, however, the load resistance must be known in order to determine the output voltage:

$$V_O = \sqrt{P_O R_L} = I \sqrt{\frac{Lf_O R_L}{2}}$$ where, R_L = the load resistance.

In this case, the choke current is proportional to the on-time or duty cycle of the switch and regulation for fixed loads simply involves varying the duty cycle as before. However, the output also depends on the load which was not the case with buck regulators and results in a variation of loop gain with load.

Figure 9-1. Functional Block Diagram — Switching Power Supply

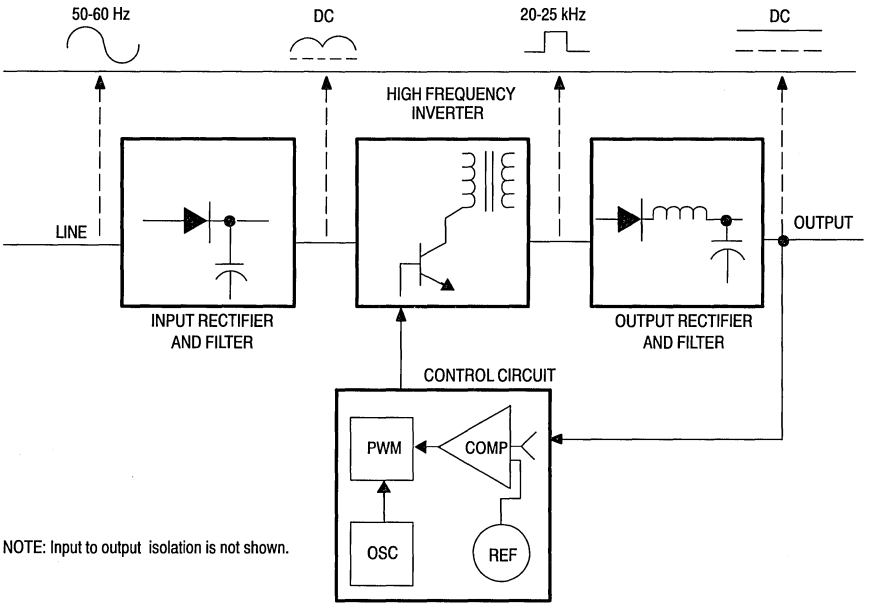
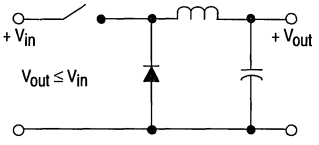
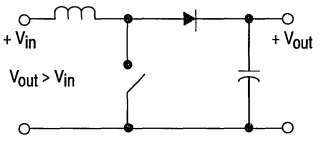


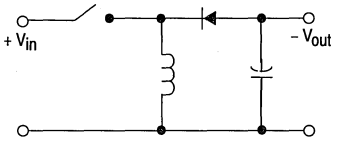
Figure 9-2. Nonisolated DC-DC Converters



(a) Buck (Step-Down)



(b) Boost (Step-Up)



(c) Buck-Boost Regulator which Resembles the Flyback Regulator (Step-Up or Down)

For both regulators, transient response or responses to step changes in load are very difficult to analyze. They lead to what is termed a "load dump" problem. This requires that energy already stored in the choke or filter be provided with a place to go when load is abruptly removed. Practical solutions to this problem include limiting the minimum load and using the right amount of filter capacitance to give the regulator time to respond to this change.

The Future

The future offers a lot of growth potential for switchers in general and low power switchers (20 W–100 W) in particular. The latter are responding to the growth in microprocessor based equipment as well as computer peripherals. Today's configurations have already been challenged by the sine wave inverter which reduces noise and improves transistor reliability but does effect a cost penalty. Also, a trend to higher switching frequencies to reduce size and cost even further has begun. The latest bipolar designs operate efficiently up to 100 kHz and the FET seems destined to own the 200 kHz to 500 kHz range.

At this time there are a lot of safety and noise specifications. Originally governed only by MIL specs and the VDE in Europe, now both UL and the FCC have released a set of specifications that apply to electronic systems which often include switchers (see Table 9-2). It seems probable, however, that system engineers or power supply designers will be able to add the necessary line filters and EMI shields without evoking a significant cost penalty in the design.

The most optimistic note concerning switchers is in the component area. Switching power supply components have actually evolved from components used in similar applications. And it is very likely that newer and more mature products specifically for switchers will continue to appear over the next several years. The ultimate effect of this evolution will be to further simplify, cost reduce and increase the reliability of these designs.

Table 9-2. SMPS Specifications

Specification	Area
UL 478, VDE 0730, VDE 0806	Safety
VDE 0871, VDE 0875	EMI
MIL-STD-217D	Reliability
MIL-STD-461A	EMI
DOD-STD-1399	Harmonic Content
FCC Class A & B	EMI
CSA C22.2, IEC 380	Safety

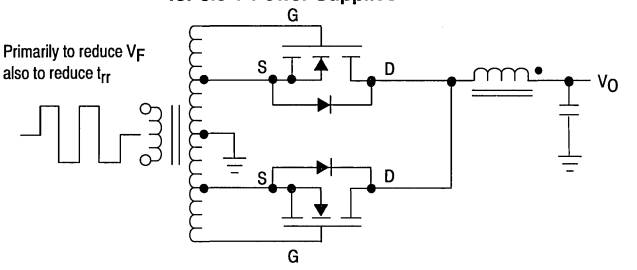
The synchronous rectifier is one example of a new component developed specifically for low voltage switchers. As requirements for 2.0 V and 3.0 V supplies emerge for use by fine geometry VLSI chips, the only way to maintain decent conversion efficiency is to develop lower forward drop rectifiers. The differences in 3.0 V and 5.0 V rectifier requirements are shown in Table 9-3. At this time, Motorola offers low V_F Schottky and area efficient TMOS III FETs for this task and is considering a variety of additional technology options. The direct approach involves using low V_F Schottkys or pinch rectifiers which will feature V_Fs of 0.3 V to 0.4 V. The indirect approach involves using FETs or bipolar transistors and slightly more complex circuitry like that shown in Figure 9-3. Both transistors will feature V_Fs of 0.2 V and, in addition, the bipolar will have high EBOs (30 V) and high gain (100) with a recovery time of 100 ns.

And for designers who are not satisfied with the relatively low frequency limitations of square wave switchers, there is the SRPS. The series resonant power supply topology seems to offer the possibility of working in the 1.0 MHz region. If components like the relatively exotic power transformer can be cost reduced, then it will be possible for this topology to become dominant in the market. The features generally associated with this type of power supply are listed in Table 9-4 and a typical half bridge circuit is shown in Figure 9-4. In a design now being studied in Motorola's advanced products laboratory, standard FETs, Schottkys and ultrafast rectifiers all appear to work very well at 1.0 MHz.

Table 9-3. Synchronous Rectifier Requirements

Output Voltage	Rectifier Characteristics	
	V_F	V_R
5.0 V	0.5 V–1.0 V	30 V–60 V
3.0 V	0.3 V–0.6 V	20 V–40 V

Figure 9-3. Synchronous Rectifiers for 3.0 V Power Supplies

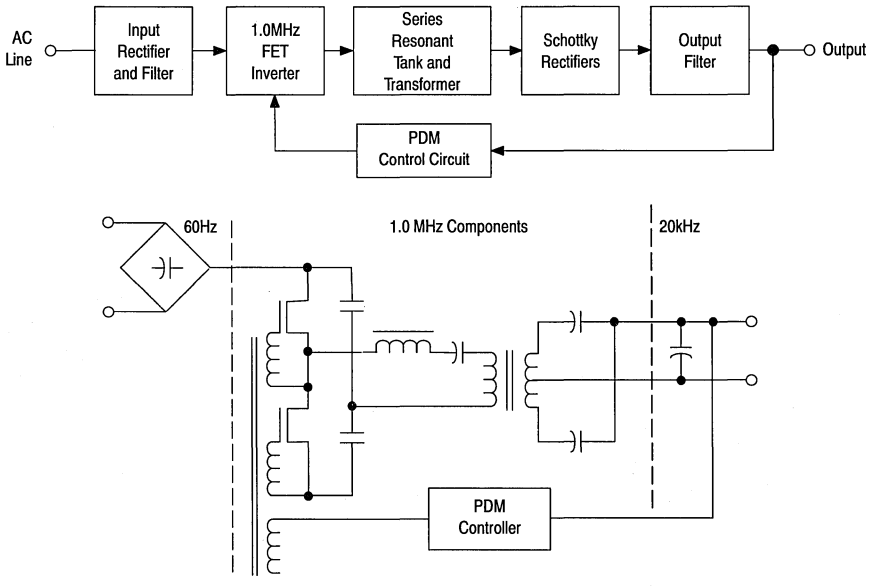


NOTE: The FET must be operated below V_F of the diode in order to gain the t_{rr} advantage.

Table 9-4. SRPS Features

Feature	Description
High Frequency	Today's line operated designs use sine waves in the 500 kHz to 1.0 MHz range.
Small Size	The ferrite transformer and polypropylene coupling capacitor are smaller than those found in lower frequency square wave designs.
Low Noise	Switching occurs at zero crossings which reduces component stress and lowers EMI.
Efficient	Because switching losses are reduced, efficiency is high (typically 80%).
High Peak to Average Current Ratios	Current ratings of the transistors and rectifiers are twice as high as similar flyback designs.
Special Control Circuit	PDM (density) rather than PWM (width) control is used and requires a control IC with a programmable VCO.
Market	The SRPS is expected to own 15% of the power supply market by 1990.

Figure 9-4. SRPS Block Diagram



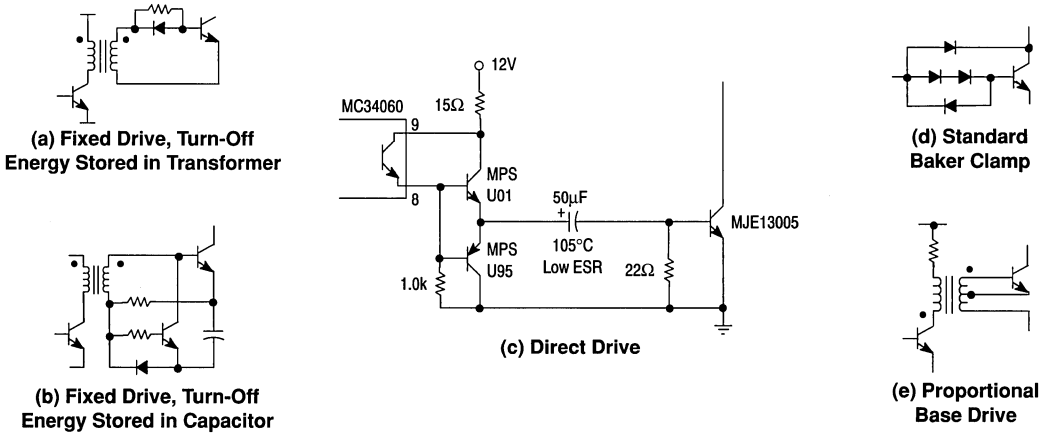
SECTION 10
SWITCHING REGULATOR TOPOLOGIES

FET and Bipolar Drive Considerations

There are probably as many base drive circuits for bipolars as there are designers. Ideally, the transistor would like just enough forward drive (current) to stay in or near saturation and reverse drive that varies with the amount of stored base charge such as a low impedance reverse voltage. Many of today's common drive circuits are shown in Figure 10-1. The fixed drive circuits of Figure 10(a), (b) and (c) tend to emphasize economy, while the Baker clamp and proportional drive circuits of Figure 10(d) and (e) emphasize performance over cost.

FET drive circuits are another alternative. The standard that has evolved at this time is shown in Figure 10-2A. This transformer coupled circuit will produce forward and reverse voltages applied to the FET gate which vary with the duty cycle as shown. For this example, a V_{GS} rating of 20 V would be adequate for the worst case condition of high logic supply (12 V) and minimum duty cycle. And yet, minimum gate drive levels of 10 V are still available with duty cycles up to 50%. If wide variations in duty cycle are anticipated, it might be wise to consider using a semi-regulated logic supply for these situations. Finally, one point that is not obvious when looking at the circuit is that FETs can be directly coupled to many ICs with only 100 mA of sink and source capability and still switch efficiently at 20 kHz. However, to achieve switching efficiently at higher frequencies, 1.0 A to 2.0 A of drive may be required on a pulsed basis in order to quickly charge and discharge the gate capacitances. A simple example will serve to illustrate this point and also show that the Miller effect, produced by C_{DG}, is the predominant speed limitation when switching high voltages (see Figure 10-2B). A FET responds instantaneously to changes in gate voltage and will begin to conduct when the threshold is reached (V_{GS} = 2.0 V to 3.0 V) and be fully on with V_{GS} = 7.0 V to 8.0 V. Gate waveforms will show a porch at a point just above the threshold voltage which varies in duration depending on the amount of drive current available and this determines both the rise and fall times for the drain current.

Figure 10-1. Typical Bipolar Base Drive Circuits



(a) Fixed Drive, Turn-Off Energy Stored in Transformer

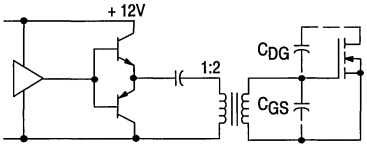
(b) Fixed Drive, Turn-Off Energy Stored in Capacitor

(c) Direct Drive

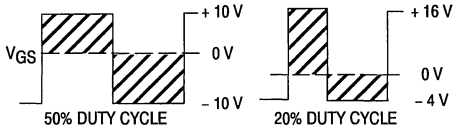
(d) Standard Baker Clamp

(e) Proportional Base Drive

Figure 10-2A. Typical Transformer Coupled FET Drive

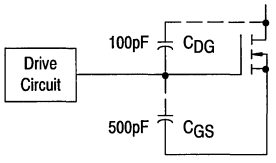


Wave Forms



V_{GS} Wave Forms

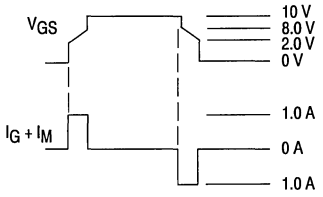
Figure 10-2B. FET Drive Current Requirements



1. Miller Current for 30 ns

$I_M = C_{DG}\, dv/dt$

$= 100\ pF \times \frac{300\ V}{30\ ns} = 1.0\ A$



2. Gate Cap Current for 30 ns

$I_G = C_{GS}\, dv/dt$

$= 500\ pF \times \frac{6.0\ V}{30\ ns} = 0.1\ A$

To estimate drive current requirements, two simple calculations with gate capacitances can be made:

1. $I_M = C_{DG} dv/dt$ and,
2. $I_G = C_{GS} dv/dt$

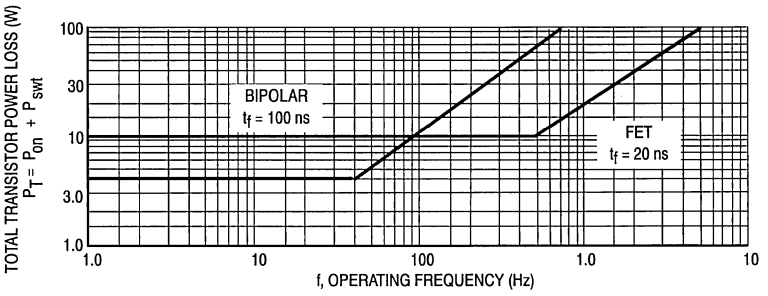
I_M is the current required by the Miller Effect to charge the drain-to-gate capacitance at the rate it is desired to move the drain voltage (and current). And I_G is usually the lesser amount of current required to charge the gate-to-source capacitance through the linear region (2.0 V to 8.0 V). As an example, if 30 ns switching times are desired at 300 V, where C_{DG} = 100 pF and C_{GS} = 500 pF, then:

1. $I_M = 100\ pF \times 300\ V/30\ ns = 1.0\ A$ and,
2. $I_G = 500\ pF \times 6.0\ V/30\ ns = 0.1\ A$

This example shows the direct proportion of drive current capability to speed and also illustrates that for most devices, C_{DG} will have the greatest effect on switching speed and that C_{GS} is important only in estimating turn-on and turn-off delays.

Aside from its unique drive requirements, a FET is very similar to a bipolar transistor. Today's 400 V FETs compete with bipolar transistors in many switching applications. They are faster and easier to drive, but do cost more and have higher saturation, or more accurately, "on" voltages. The performance or efficiency tradeoffs are analyzed using Figure 10-3, where typical power losses for switching transistors versus frequency are shown. The FET (and bipolar) losses were calculated at 100°C rather than 25°C because on resistance and switching times are highest here and 100°C is typical of many applications. These curves are asymptotes of the actual device performance, but are useful in establishing the "breakpoint" of various devices, which is the point where saturation and switching losses are equal.

Figure 10-3. Typical Switching Losses at 300 V and 5.0 A (T_J = 100°C)



Control Circuits

Over the past ten years, a variety of control ICs for SMPS have been introduced. The voltage mode controllers diagramed in Table 10-1 still dominate this market. The basic regulating function is performed in the pulse width modulator (PWM) section. Here, the DC feedback signal is compared to a fixed frequency sawtooth waveform. The result is a variable duty cycle pulse train which, with suitable buffer or interface circuits, can be used to drive the power switching transistor. Some ICs provide only a single output while others provide a phase splitter or flip-flop to alternately pulse two output channels. Additionally, most ICs provide an error amplifier and reference section shown as a means to process, compare and amplify the feedback signal.

Features required by a control IC vary to some extent because of the particular needs of a designer and on the circuit configuration chosen. However, most of today's current generation ICs have evolved with the following capabilities or features:

- Programmable (to 500 kHz) Fixed Frequency Oscillator
- Linear PWM Section with Duty Cycle from 0% to 100%
- On Board Error Amplifiers
- On Board Reference Regulator
- Adjustable Dead Time
- Under Voltage (low V_{CC}) Inhibit
- Good Output Drive (100 mA to 200 mA)
- Option of Single or Dual Channel Output
- Uncommitted Output Collector and Emitter or Totem Pole Drive Configuration
- Soft-Start
- Digital Current Limiting
- Oscillator Sync Capability

It is primarily the cost differences in these parts that determine whether all or only part of these features will be incorporated. Most of these are evident to the designer who has already started comparing competitive device data sheets.

In addition to the control circuits listed in Table 10-2, Motorola also has two DC converter control chips, the μA78S40 and the MC34063A. These chips feature an on-board 40 V, 2.0 A switching transistor and operate by dropping pulses from a fixed frequency, fixed duty cycle oscillator depending on load demand.

Today there is a demand for simple, low cost, single control ICs. These ICs, like Motorola's MC34060A and MC34063A components, are used to run the low-power flyback type configurations and are usually part of a three chip rather than a single chip system. The differences in these two approaches are illustrated in Figure 10-6.

When it is necessary to drive two or more power transistors, drive transformers are a practical interface element and are driven by the conventional dual channel ICs. In the case of a single transistor converter, however, it is usually more cost effective to directly drive the transistor from the IC. In this situation, an optocoupler is commonly used to couple the feedback signal from the output back to this control IC. And the error amplifier in this case is nothing more than a programmable zener like Motorola's TL431.

Overvoltage Protection

Linear and switching power supplies can be protected from overvoltage with a crowbar circuit. For linear supplies, the pass transistor can fail shorted, allowing high line transformer voltage to the load. For switching power supplies, a loose or disconnected remote sense lead can allow high voltage to the load.

Table 10-1. Basic SM Control ICs

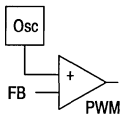
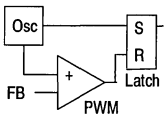
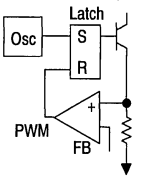
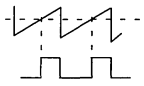
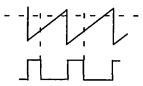
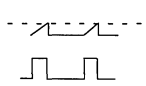
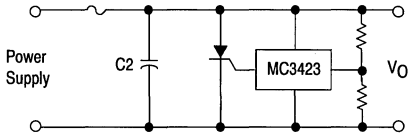
CONTROL TECHNIQUE	Type A Voltage Mode	Type B Voltage Mode w/Latch	Type C Current Mode
SCHEMATIC			
SINGLE CHANNEL PARTS	MC34060A	—	UC3842 MC34129
DUAL CHANNEL PARTS	TL494/594	SG3525A/27A SG3526	—
FEATURES	Low Cost	Digital Current Limiting, Good Noise Immunity	Designed for Flyback, Inherent Feed Forward
PWM WAVEFORMS OUTPUT			

Table 10-2. Control Circuits

Overvoltage Protection (OVP)		Over/Undervoltage Protection (O/UVP)	Undervoltage Sense MPU/MCU Reset
Standard	High Performance		
TL431	MC3423 TL431A	MC3425 MC34161	MC34064-5 MC34164-3 MC34164-5

The list of available circuits is shown in Table 10-2 and a typical 0 V application is shown in Figure 10-4. This crowbar circuit ignores noise spikes but will fire the SCR when a valid overvoltage condition is detected. The SCR will discharge C2 and either blow the fuse or cause the power supply to shut down.

Figure 10-4. Crowbar Circuit



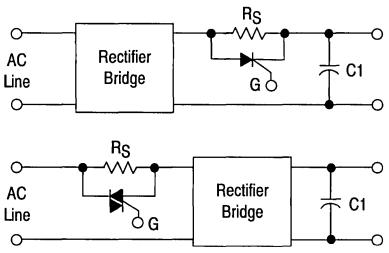
For further information, see the MC3423 data sheet.

Surge Current Protection

Many high current PWM switching supplies operate directly off the AC line. They have very large capacitive input filters with high inrush surge currents. The line circuit breaker and the rectifier bridge must be protected during turn-on.

Surge current limiting can be accomplished by adding R_S and an SCR short after charging C1, as shown in Figure 10-5, or by phase controlling the line voltage with a Triac.

Figure 10-5. Surge Current Limiting for a Switching Power Supply



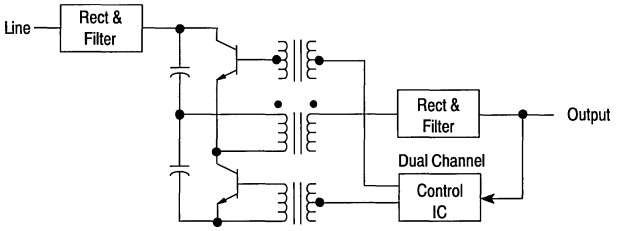
Transformer Design

With respect to transformer design, many of today's designers would say don't try it. They'd advise using a consultant or winding house to perform this task and with good reason. It takes quite a bit of time to develop a feel for this craft and be able to use both experience and intuition to find solutions to second and third order problems. Because of these subtle problems, most designers find that after the first paper design is done, as many as four or five lab iterations may be necessary before the transformer meets the design goals. However, there is a considerable design challenge in this area and a great deal of satisfaction can be obtained by mastering it.

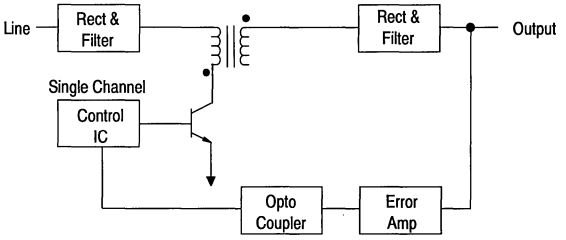
This component design, as do all others, begins by requesting all available literature from the appropriate manufacturers and then following this up with phone calls when specific questions arise. A partial list of companies is shown in Table 10-3. Designs below 20 W generally use pot cores but for 20 W and above E cores are preferred. E cores expose the windings to air so that heat is not trapped inside and make it easier to bring out connections for several windings. Remember that flyback designs require lower permeability cores than the others. The classic approach is to consult manufacturers charts like the one shown in Figure 10-8 and then to pick a core with the required power handling ability. Both E and EC (E cores with a round center leg) are popular now and they are available from several manufacturers. EC cores offer a performance advantage (better coupling) but standard E cores cost less and are also used in these applications. Another approach that seems to work equally well is to do a paper design of the estimated windings and turns required. Size the wire for 500 circular mils (CM) per amp and then find a core that has the required window area for this design. Now, before the windings are put on, it is a good idea to modify the turns so that they fit on one layer or an integral number of layers on that bobbin. This involves checking the turns per inch of the wire against the bobbin length. The primary generally goes on first and then the secondaries. If the primary hangs over an extra half layer, try reducing the turns or the wire size. Conversely, if the secondary does not take up a full layer, try bifilar winding (parallel) using wire half the size originally chosen; i.e., 3 wire sizes smaller like 23 versus 20. This technique ultimately results in the use of foil for the higher current (20 A) low voltage windings. Most windings can be separated with 3 mil mylar (yellow) tape but for good isolation, cloth is recommended between primary and secondary.

Finally, once a mechanical fit has been obtained, it is time for the circuit tests. The isolation voltage rating is strictly a mechanical problem and is one of the reasons why cloth is preferred over tape between the primary and secondary. The inductance and saturating current level of the primary are inherent to the design, and should be checked in the circuit or other suitable test fixture. Such a fixture is shown in Figure 10-7 where the transistor and diode are sized to handle the anticipated currents. The pulse generator is run at a low enough duty cycle to allow the core to reset. Pulse width is increased until the start of saturation is observed (I_{sat}). Inductance is found using $L = E/(di/dt)$

Figure 10-6. Control Circuit Topologies



(a) Single Chip System — Drive Transformer Isolation



(b) Three Chip System — Opto Coupler Isolation

In forward converters, the transformer generally has no gap in order to minimize the magnetizing current (I_M). For these applications the core should be chosen large enough so that the resulting LI product insures that I_M at operating voltages is less than I_{SAT}. For flyback designs, a gap is necessary and the test circuit is useful again to evaluate the effect of the gap. The gap will normally be quite large, $Lg >> L_m/u$,

where, Lg = gap length
L_m = magnetic path length, and
u = permeability.

Under this stipulation, the gap directly controls the LI parameters and doubling it will decrease L by two and increase I_{sat} by two until fringing effects occur. Gaps of 5 mils to 20 mils are common. Again, the anticipated switching currents must be less than I_{sat} when the core is gapped for the correct inductance.

Table 10-3. Partial List of Core (C) and Transformer (T) Manufacturers

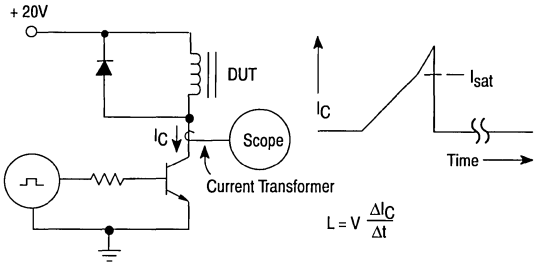
Company	Location	Code
Ferroxcube Inc.	Sauggerties, NY	C
Indiana General	Keasby, NJ	C
Stackpole	St. Marys, PA	C
TDK	El Segundo, CA	C
Pulse Engineering	San Diego, CA	T
Coilcraft	Cary, IL	T

Transformer tests in the actual supply are usually done with a high voltage DC power supply on the primary and with a pulse generator or other manual control for the pulse width (such as using the control IC in the open-loop configuration). Here the designer must recheck three areas:

1. Core saturation
2. Correct amount of secondary voltage
3. Transformer heat rise

If problems are detected in any of these areas, the ultimate fix may be to redesign using the next larger core size. However, if problems are minimal, or none exist, it is possible to stay with the same core or even consider using the next smaller size.

Figure 10-7. Simple Coil Tester



Filter Capacitor Considerations

In today's 20 kHz switchers, aluminum electrolytics still predominate. The good news is that most have been characterized, improved, and cost reduced for this application. The input filter requires a voltage rating that depends on the peak line voltage; i.e., 400 V to 450 V for a 220 V switcher. If voltage is increased beyond this point, the capacitor will begin to act like a zener and be thermally destroyed from high leakage currents if the rating is exceeded for enough time. In doubler circuits, voltage sharing of the two capacitors in series can be a problem. Here extra voltage capability may be needed to make up for the imbalances caused by different values of capacitance and leakage current. A bleeder resistor is normally used here not only for safety but to mask the differences in leakage current. The RMS current rating is also an important consideration for input capacitors and is an example of improvements offered by today's manufacturers. Earlier "lytics" usually lacked this rating and often overheated. Large capacitors that were not needed for performance were used just to reduce this heating. However, today's devices offer lower thermal resistance, improved connection to the foil and good RMS ratings. A partial list of manufacturers that supply both high voltage input and the lower voltage output capacitors for switchers is shown in Table 10-4. Most of the companies offer not only the standard 85°C components, but devices with up to 125°C ratings which are required because of the high ambient temperatures (55° to 85°C) that many switchers have to operate in, many times without the benefit of fans.

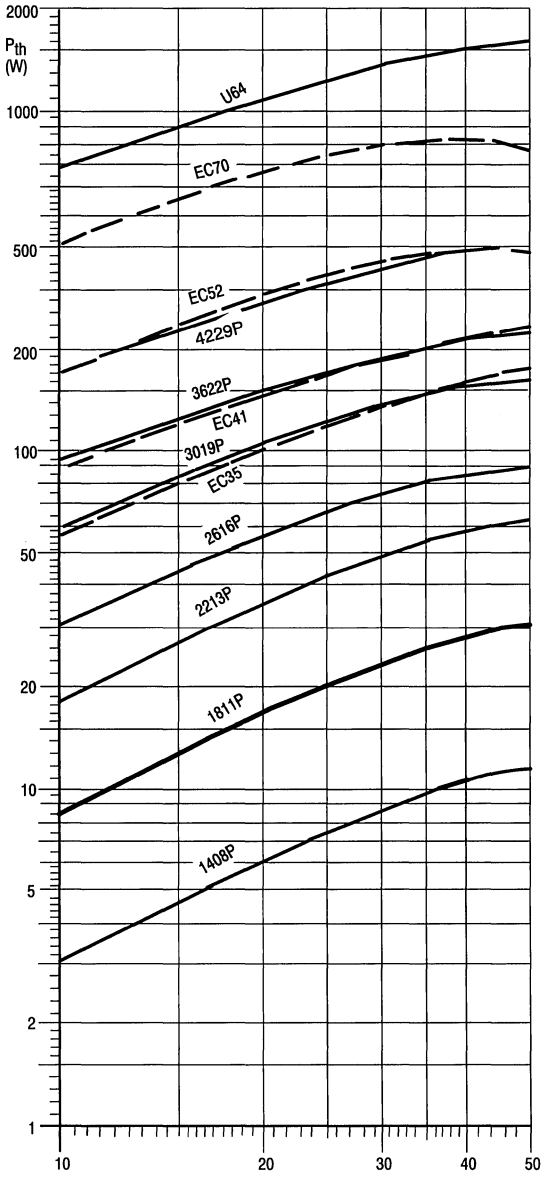
Table 10-4. Partial List of Capacitor Companies

Company (U.S.)	Location
MEPCO/Electra	Columbia, SC
Cornell-Dublier	Sanford, NC
Sangamo	Pickens, SC
Mallory	Indianapolis, IN

For output capacitors the buzz word is low ESR (equivalent series resistance). It turns out that for most capacitors even in the so-called "low ESR" series, the output ripple depends more on this resistance than on the capacitor value itself. Although typical and maximum ESR ratings are now available on most capacitors designed for switchers, the lead inductance generally is not specified except for the ultra-high frequency four terminal capacitors from some vendors. This parameter is responsible for the relatively high switching spikes that appear at the output. However, at this point in time, most designers find it less costly and more effective to add a high frequency noise filter rather than use a relatively expensive capacitor with low equivalent series inductance (ESL).

These LC noise or spike filters are made using small powdered iron toroids (1/2″ to 1″ OD) with distributed windings to minimize interwinding capacitance. And the output is bypassed using a small 0.1 μF ceramic or a 10 μF to 50 μF tantalum or both. Larger powered iron toroids are often used in the main LC output filter although the higher permeability ferrite EC and E cores with relatively large gaps can also be used. Calculations for the size of this component should take into account the minimum load so that the choke will not run "dry" as stated earlier.

Figure 10-8. Core Selection for Bridge Configurations (Reprinted from Ferroxcube Design Manual)



NOTE: Power handling decreases by a factor of 2 in forward and 4 in flyback configurations.

SECTION 11
SWITCHING REGULATOR COMPONENT DESIGN TIPS

Transistors

The initial selection of a transistor for a switcher is basically a problem of finding the one with voltage and current capabilities that are compatible with the application. For the final choice performance and cost tradeoffs among devices from the same or several manufacturers have to be weighed. Before these devices can be put in the circuit, both protective and drive circuits will have to be designed.

Motorola's first line of devices for switchers were trademarked "Switchmode" transistors and introduced in the early 70's with data sheets that provided all the information that a designer would need including reverse bias safe operating area (RBSOA) and performance at elevated temperature (100°C). The first series was the 2N6542 through 2N6547, TO-204 (TO-3) and was followed by the MJE13002 through MJE13009 series in a plastic TO-220 package. Finally, high voltage (1.0 kV) requirements were met by the metal MJ8500 thru MJ8505 series and the plastic MJE8500 series. The Switchmode II series is an advanced version of Switchmode I that features faster switching. Switchmode III is a state of the art bipolar with exceptional speed, RBSOA, and up to 1.5 kV blocking capacity. Here, device cost is somewhat higher, but system costs may be lowered because of reduced snubber requirements and higher operating frequencies. A similar argument applies to Motorola TMOS Power FETs. These devices make it possible to switch efficiently at higher frequencies (200 kHz to 500 kHz) but the main selling point is that they are easier to drive. This latter point is the one most often made to show that systems savings are again quite possible even though the initial device cost is higher.

Table 11-1. Motorola High Voltage Switching Transistor Technologies

Family	Typical Device	Typical Fall Time	Approximate Switching Frequency
SWITCHMODE I	2N6545 MJE13005 MJE12007	200 ns–500 ns	20 k
SWITCHMODE II	MJ13081	100 ns	100 k
SWITCHMODE III	MJ16010	50 ns	200 k
TMOS	MTP5N40	20 ns	500 k

Table 11-2 is a chart of the transistor voltage requirements for the various off-line converter circuits. As illustrated, the most stringent requirement for single transistor circuits (flyback and forward) is the blocking or V_{CEV} rating. Bridge circuits, on the other hand, turn on and off from the DC bus and their most critical voltage is the turn-on or $V_{CEO(sus)}$ rating.

Table 11-2. Power Transistor Voltage Chart

Line Voltage	Circuit			
	Flyback, Forward or Push-Pull		Half or Full-Bridge	
	V_{CEV}	$V_{CEO(sus)}$	$V_{CEO(sus)}$	V_{CEV}
220 120	850 kV–1.0 kV 450	450 250	450 250	450 250

Most switchmode transistor load lines are inductive during turn-on and turn-off. Turn-on is generally inductive because the short circuit created by output rectifier reverse recovery times is isolated by leakage inductance in the transformer. This inductance effectively snubs most turn-on load lines so that the rectifier recovery (or short circuit) current and the input voltage are not applied simultaneously to the transistor. Sometimes primary interwinding capacitance presents a small current spike but usually turn-on transients are not a problem. Turn-off transients due to this same leakage inductance, however, are almost always a problem. In bridge circuits, clamp diodes can be used to limit these voltage spikes. If the resulting inductive load line exceeds the transistor's reverse bias switching capability (RBSOA) then an RC network may also be added across the primary to absorb some of this transient energy. The time constant of this network should equal the anticipated switching time of the transistor (50 ns to 500 ns). Resistance values of 100 Ω to 1000 Ω in this RC network are generally appropriate. Trial and error will indicate how low the resistor has to be to provide the correct amount of snubbing. For single transistor converters, the circuits shown in Figure 11-1 are generally used.

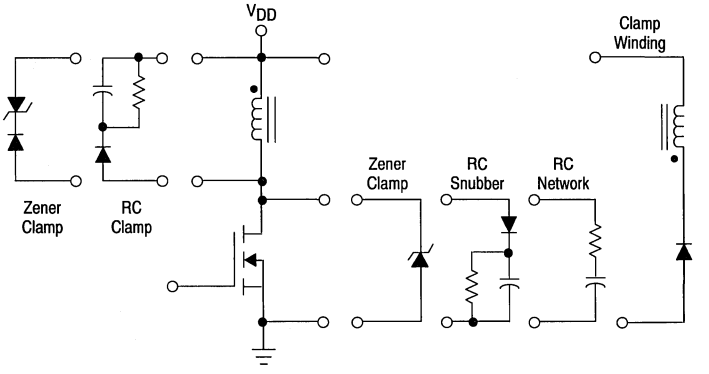
Here slightly different criteria are used to define the R and C snubber values:

$$C = \frac{I\, t_f}{V}$$

where; I = the peak switching current
t_f = the transistor fall time
V = the peak switching voltage (Approximately twice the DC bus)
also $R = t_{on}/C$ (it is not necessary to completely discharge this capacitor in order to obtain the desired effects of this circuit)
where, t_{on} = the minimum on-time or pulse width
and $P_R = \frac{CV^2 f}{2}$
where, P_R = the power rating of the resistor
and f = the operating frequency.

In most of today's designs snubber elements are small or nonexistent and voltage spikes from energy left in the leakage inductance a more critical problem depending on how good the coupling is between the primary and clamp windings and how fast the clamp diode turns on. FETs often have to be slowed down to prevent self destruction from this spike.

Figure 11-1. Protection Circuits for Switching Transistors



Zener and Mosorb Transient Suppressors

If necessary, protection from voltage spikes may be obtained by adding a zener and rectifier across the primary as shown in Figure 11-1. Here Motorola's 5.0 W zener lines with ratings up to 200 V, and 10 W TO-220 Mosorbs with ratings up to 250 V can provide the clamping or spike limiting function. If the zener must handle most of the power, its size can be estimated using:

$$P_Z = \frac{L_L I^2 f}{2}$$

where, P_Z = the zener power rating
and L_L = the leakage inductance (measured with the clamp winding or secondary shorted)
I = peak collector current
f = operating frequency

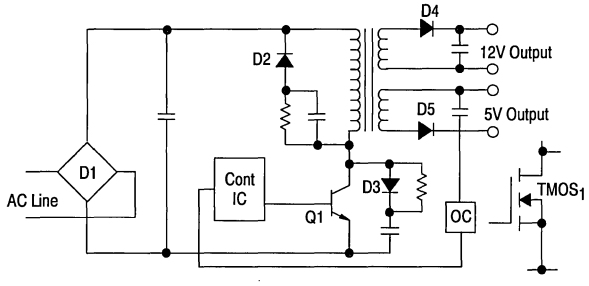
Distinction is sometimes made between devices trademarked Mosorb (by Motorola, Inc.), and standard zener/avalanche diodes used for reference, low-level regulation and low-level protection purposes. It must be emphasized that Mosorb devices are, in fact, zener diodes. The basic semiconductor technology and processing are identical. The primary difference is in the applications for which they are designed. Mosorb devices are intended specifically for transient protection purposes and are designed, therefore, with a large effective junction area that provides high pulse power capability while minimizing the total silicon use. Thus, Mosorb pulse power ratings begin at 600 W — well in excess of low power conventional zener diodes which in many cases do not even include pulse power ratings among their specifications.

MOVs, like Mosorbs, do have the pulse power capabilities for transient suppression. They are metal oxide varistors (not semiconductors) that exhibit bidirectional avalanche characteristics, similar to those of back-to-back connected zeners. The main attributes of such devices are low manufacturing cost, the ability to absorb high energy surges (up to 600 joules) and symmetrical bidirectional "breakdown" characteristics. Major disadvantages are: high clamping factor, an internal wear-out mechanism and an absence of low-end voltage capability. These limitations restrict the use of MOVs primarily to the protection of insensitive electronic components against high energy transients in applications above 20 V, whereas, Mosorbs are best suited for precise protection of sensitive equipment even in the low voltage range the same range covered by conventional zener diodes.

Rectifiers

Once components for the inverter section of a switcher have been chosen, it is time to determine how to get power into and out of this section. This is where the all-important rectifier comes into play. (See Figure 11-2.) The input rectifier is generally a standard recovery bridge that operates off the AC line and into a capacitive filter. For the output section, most designers use Schottkys for efficient rectification of the low voltage, 5.0 V output windings and for the higher voltage, 12 V to 15 V outputs, the more economical fast recovery or ultrafast diodes are used.

Figure 11-2. Switchmode Power Supply Flyback or Boost Design



D1 — Bridge Rectifier — Line Voltage
D2 — Clamp Diode — HV/Fast-Ultrafast
D3 — Snubber Diode — HV/Fast-Ultrafast
D4 — Output Rectifier — Fast/Ultrafast
D5 — Output Rectifier — Schottky

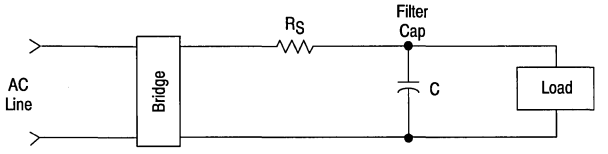
For the process of choosing an input rectifier, it is useful to visualize the circuit shown in Figure 11-3. To reduce cost, most earlier approaches of using choke input filters, soft start relays (Triacs), or SCRs to bypass a large limiting resistor have been abandoned in favor of using small limiting resistors or thermistors and a large bridge. The bridge must be able to withstand the surge currents that exist from repetitive starts at peak line. The procedure for finding the right component and checking its fit is as follows:

1. Choose a rectifier with 2 to 5 times the average I_O required.
2. Estimate the peak surge current (I_p) and time (t) using:

$$I_p = \frac{1.4\ V_{in}}{R_S} \qquad t = R_S C$$

Where V_{in} is the RMS input voltage; R_S is the total series resistance; and C is the filter capacitor size.

Figure 11-3. Choosing Input Rectifiers



3. Compare this current pulse to the sub cycle surge current rating (I_S) of the diode itself. If the curve of I_S versus time is not given on the data sheet, the approximate value for I_S at a particular pulse width (t) may be calculated knowing:
   - I_{FSM} — the single cycle (8.3 ms) surge current rating and using.
   - $I^2\sqrt{t}$ = K, which applies when the diode temperature rise is controlled by its thermal response as well as power (i.e., $T = K'P\sqrt{t}$ for t < 8.0 ms).

This gives:

$$I_S{}^2\sqrt{t} = I^2_{FSM}\sqrt{8.3\ ms} \quad \text{or,} \quad I_S = I_{FSM}\left(\frac{8.3\ ms}{t}\right)^{1/4}, \text{ t is in milliseconds.}$$

4. If $I_S < I_P$, consider either increasing the limiting resistor (R_S) or utilizing a larger diode.

In the output section where high frequency rectifiers are needed, there are several types available to the designer. In addition to the Schottky (SBR) and fast recovery (FR), there is also an ultrafast recovery (UFR). Comparative performance for devices with similar current ratings is shown in Table 11-3. The obvious point here is that lower forward voltage improves efficiency and lower recovery times reduce turn-on losses in the switching transistors, but the tradeoff is higher cost. As stated earlier, Schottkys are generally used for 5.0 V outputs and fast recovery and ultrafast devices for 12 V outputs and greater. The ultrafast is competing both with the Schottky where higher breakdown is needed and with the fast recovery in those applications where performance is more important than cost. Ten years ago Schottkys were very fragile and could fail short from either excessive dv/dt (1.0 V to 5.0 V per nanosecond) or reverse avalanche. Since that time, Motorola has incorporated a "guard ring" or internal zener which minimizes these earlier problems and reduces the need for RC snubbers and other external protective networks.

Table 11-3. Motorola Rectifier Product Portfolio

Parameter	Schottky	Ultrafast	Fast Recovery	Standard Recovery
Forward Voltage (V_F)	0.5 V–0.6 V	0.9 V–1.0 V	1.2 V–1.4 V	1.2 V–1.4 V
Reverse Recovery Time (t_{rr})	<10 ns	25 ns–100 ns	150 ns	1.0 µs
t_{rr} Form	Soft	Soft	Soft	Soft
dc Blocking Voltage (V_R)	20 V–60 V	50 V–1000 V	50 V–1000 V	50 V–1000 V
Cost Ratio	3:1	3:1	2:1	1:1

SECTION 12
BASIC SWITCHING POWER SUPPLY CONFIGURATIONS

3

The implementation of switching power supplies by the non-specialist is becoming increasingly easy due to the availability of power devices and control ICs especially developed for this purpose by the semiconductor manufacturer.

This section is meant to help in the preliminary selection of the devices required for the implementation of the listed switching power supplies.

Flyback and Forward Converter Switching Power Supplies (50 W to 250 W)

- Input line variation: V_{in} + 10%, – 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ variation: $\delta_{(max)}$ = 0.4)
- Maximum Transistor working current:

$$I_W = \frac{2.0\ P_{out}}{\eta \bullet \delta_{(max)} \bullet V_{in(min)} \bullet \sqrt{2}} = \frac{5.5\ P_{out}}{V_{in}} \text{ (Flyback)}$$

$$= \frac{P_{out}}{\eta \bullet \delta_{(max)} \bullet V_{in(min)} \bullet \sqrt{2}} = \frac{2.25\ P_{out}}{V_{in}} \text{ (Forward)}$$

- Maximum transistor working voltage: $V_W = 2 \bullet V_{in(max)} \bullet \sqrt{2}$ + guardband
- Working frequency: f = 20 kHz to 200 kHz

Basic Flyback Configuration

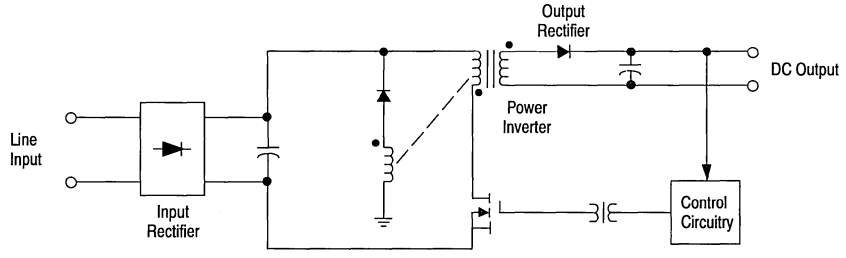


Table 12-1. Flyback and Forward Converter Semiconductor Selection Chart

Output Power	50 W		100 W		175 W		250 W
Input Line Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V	120 V
MOSFET Requirements: Max Working Current (I_W) Max Working Voltage (V_W)	 2.25 A 380 V	 1.2 A 750 V	 4.0 A 380 V	 2.5 A 750 V	 8.0 A 380 V	 4.4 A 750 V	 11.4 A 380 V
Power MOSFETs Recommended: Metal (TO-204AA) (TO-3) Plastic (TO-220AB) Plastic (TO-218AC)	 MTM4N45 MTP4N45 —	 MTM2N90 MTP2N90 —	 MTM4N45 MTP4N45 —	 MTM2N90 MTP2N90 —	 MTM7N45 — MTH7N45	 MTM4N90 — —	 MTM15N45 — —
Input Rectifiers: Max Working Current (I_W) Recommended Types	 0.4 A MDA104A	 0.25 A MDA106A	 0.4 A MDA206	 0.5 A MDA210	 2.35 A MDA970	 1.25 A MDA210	 4.6 A MDA3506
Output Rectifiers: Recommended types for Output Voltage of: 5.0 V 10 V 20 V 50 V 100 V	 MBR3035PT MUR3010PT MUR1615CT MUR1615CT MUR 440, MUR840A		 MBR3035PT MUR3010PT MUR1615CT MUR1615CT MUR840A		 MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual-LM358 Quad MC3403, LM324, LM2902						

Flyback and Forward Converters

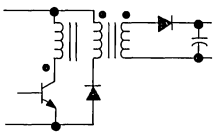
To take advantage of the regulating techniques discussed earlier and also provide isolation, a total of seven popular configurations have evolved and are listed below. Each circuit has a practical power range or capability associated with it as follows:

Circuit	Power Range	Parts Cost
DC Converter	5.0 W	$ 4.00
Converter w/30 V Transformer	10 W	7.00
Blocking OSC	20 W	10.00
Flyback	50 W	15.00
Forward	100 W	20.00
Half-Bridge	200 W	30.00
Full-Bridge	500 W	75.00

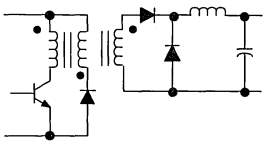
First to be discussed will be the low power (20 W–200 W) converters which are dominated by the single transistor circuits shown in Figure 12-1. All of these circuits operate the magnetic element in the unipolar rather than bipolar mode. This means that transformer size is sacrificed for circuit simplicity.

The flyback (alternately known as the "ringing choke") regulator stores energy in the primary winding and dumps it into the secondary windings, see Figure 12-1(a). A clamp winding is usually present to allow energy stored in the leakage reactance to return safely to the line instead of avalanching the switching transistor. The operating model for this circuit is the buck-boost discussed earlier. The flyback is the lowest cost regulator because output filter chokes are not required since the output capacitors feed from a current source rather than a voltage source. It does have higher output ripple than the forward converters because of this. However, it is an excellent choice when multiple output voltages are required and does tend to provide better cross regulation than the other types. In other words changing the load on one winding will have little effect on the output voltage of the others.

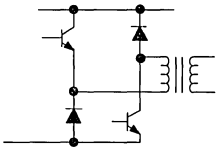
Figure 12-1. Low Power Popular (20-200 W) Converter Configurations



(a) Flyback (Clamp Winding is Optional)



(b) Forward (Clamp Winding is Necessary)

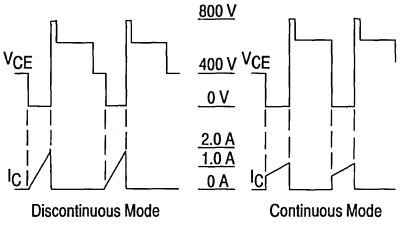


(c) Two Transistor Forward or Flyback
(Clamp Winding is not Needed)

A 120/220 Vac flyback design requires transistors that block twice the peak line plus transients or about 1.0 kV. Motorola's MJE13000 and 16000A series with ratings of 750 V to 1000 V are normally used here. These bipolar devices are relatively fast (100 ns) and are typically used in the 20 kHz to 50 kHz operating frequency range. The recent availability of 900 V and 1000 V TMOS FETs allows designers to operate in the next higher range (50 kHz to 80 kHz) and some have even gone as high as 300 kHz with square wave designs and FETs. Faster 1.0 kV bipolar transistors are also planned in the future and will provide another design alternative. The two transistor variations of this circuit, Figure 12-1(c), eliminate the clamp winding and add a transistor and diode to effectively clamp peak transistor voltages to the line. With this circuit a designer can use the faster 400 V to 500 V FET transistors and push operating frequencies considerably higher. There is a cost penalty here over the single transistor circuit due to the extra transistor, diodes and gate drive circuitry.

A subtle variation in the method of operation can be applied to the flyback regulator. The difference is referred to as operation in the discontinuous or continuous mode and the waveform diagrams are shown in Figure 12-2. The analysis given in the earlier section on boost regulators dealt strictly with the discontinuous mode where all the energy is dumped from the choke before the transistor turns on again. If the transistor is turned on while energy is still being dumped into the load, the circuit is operating in the continuous mode. This is generally an advantage for the transistor in that it needs to switch only half as much peak current in order to deliver the same power to the load.

Figure 12-2. Flyback Transistor Waveforms

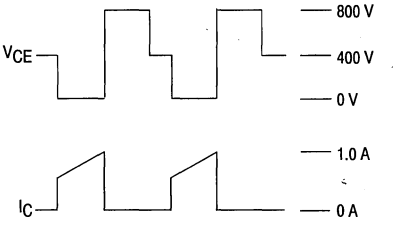


In many instances, the same transformer may be used with only the gap reduced to provide more inductance. Sometimes the core size will need to be increased to support the higher LI product (2 to 4 times) now required because the inductance must increase by almost 10 times to effectively reduce the peak current by two. In dealing with the continuous mode, it should also be noted that the transistor must now turn on from 500 V to 600 V rather than 400 V level because there no longer is any dead time to allow the flyback voltage to settle back down in the input voltage level. Generally, it is advisable to have $V_{CEO(sus)}$ ratings comparable to the turn-on requirements except for SMIII where turn-on up to V_{CEV} is permitted.

The flyback converter stands out from the others in its need for a low inductance, high current primary. Conventional E and pot core ferrites are difficult to work with because their permeability is too high even with relatively large gaps (50 to 100 milli-inches). The industry needs something better that will provide permeabilities of 60 to 120 instead of 2000 to 3000 for this application.

The single transistor forward converter is shown in Figure 12-1(b). Although it initially appears very similar to the flyback, it is not. The operating model for this circuit is actually the buck regulator discussed earlier. Instead of storing energy in the transformer and then delivering it to the load, this circuit uses the transformer in the active or forward mode and delivers power to the load while the transistor is on. The additional output rectifier is used as a freewheeling diode for the LC filter and the third winding is actually a reset winding. It generally has the same turns as the primary, (is usually bifilar wound) and does clamp the reset voltage to twice the line. However, its main function is to return energy stored in the magnetizing inductance to the line and thereby reset the core after each cycle of operation. Because it takes the same time to set and reset the core, the duty cycle of this circuit cannot exceed 50%. This also is a very popular low power converter and like the flyback is practically immune from transformer saturation problems. Transistor waveforms shown in Figure 12-3 illustrate that the voltage requirements are identical to the flyback. For the single transistor versions, 400 V turn-on and 1.0 kV blocking devices like the MJE13000 and MJE16000 transistors are required. The two transistor circuit variations shown in Figure 12-1(b) again adds a cost penalty but allows a designer to use the faster 400 V to 500 V devices. With this circuit, operation in the discontinuous mode refers to the time when the load is reduced to a point where the filter choke runs "dry." This means that choke current starts at and returns to zero during each cycle of operation. Most designers prefer to avoid this type of mode because of higher ripple and noise even though there are no adverse effects on the components themselves. Standard ferrite cores work fine here and in the high power converters as well. In these applications, no gap is used as the high permeability (3000) results in the desirable effect of very low magnetizing current levels. And, zeners or RC clamps may be used to reset the core in lieu of the clamp winding to lower the voltage stress on the switching transistors.

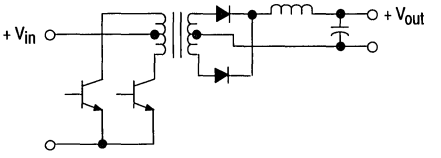
Figure 12-3. Forward Converter Transistor Waveforms



Push-Pull and Bridge Converters

The high power circuits shown in Figures 12-4 to 12-7 all operate the magnetic element in the bipolar or push-pull mode and require 2 to 4 inverter transistors. Because the transformers operate in this mode they tend to be almost half the size of the equivalent single transistor converters and thereby provide a cost advantage over their counterparts at power levels of 200 kW to 1.0 kW.

Figure 12-4. Push-Pull Converter (200 W to 1.0 kW)



The push-pull converter shown in Figure 12-4 is one of the oldest converter circuits around. Its early use was in low voltage inverters such as the 12 Vdc to 120 Vdc power source for recreational vehicles and in DC to DC converters. Because these converters are free running rather than driven and operate from low voltages, transformer saturation problems are minimal. In the high voltage off-line switchers, saturation problems are common and were difficult to solve. The transistors are also subjected to twice the peak line voltage which requires the use of high voltage (1.0 kV) transistors. Both of these drawbacks have tended to discourage designers of off-line switchers from using this configuration until current mode control ICs were introduced. Now these circuits are being looked at with renewed interest.

Push-Pull Switching Power Supplies (100 W to 500 W)

- Input line variation: V_{in} + 10%, – 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ) variation: $\delta_{(max)}$ = 0.8
- Maximum transistor working current:

$$I_W = \frac{P_{out}}{\eta \bullet \delta_{(max)} \bullet V_{in(min)} \bullet \sqrt{2}} = \frac{1.4\ P_{out}}{V_{in}}$$

- Maximum transistor working voltage: $V_W = 2 \bullet V_{in(max)} \bullet \sqrt{2}$ + guardband
- Working frequency: f = 20 kHz to 200 kHz

Basic Push-Pull Configuration

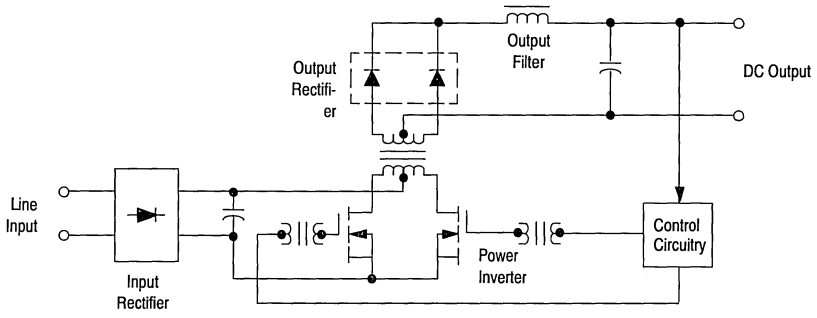


Table 12-2. Push-Pull Semiconductor Selection Chart

Output Power	100 W		250 W		500 W	
Input Line Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements: Max Working Current (I_W) Max Working Voltage (V_W)	 1.2 A 380 V	 0.6 A 750 A	 2.9 A 380 V	 1.6 A 750 V	 5.7 A 380 V	 3.1 A 750 V
Power MOSFETs Recommended: Metal (TO-204AA) (TO-3) Plastic (TO-220AB) Plastic (TO-218AC)	 MTM2N50 MTP2N45 —	 MTM2N90 MTP2N90 —	 MTM4N45 MTP4N45 —	 MTM2N90 MTP2N94 —	 MTM7N45 — MTH7N45	 MTM4N90 — —
Input Rectifiers: Max Working Current (I_W) Recommended Types	 0.9 A MDA206	 0.5 A MDA210	 2.35 A MDA970-5	 1.25 A MDA210	 4.6 A MDA3506	 2.5 A MDA3510
Output Rectifiers: Recommended types for output voltages of: 5.0 V 10 V 20 V 50 V 100 V	 MBR3035PT MBR3045PT, MUR3010PT MUR1615CT MUR1615CT MUR840A, MUR440		 MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A	
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual-LM358 Quad MC3403, LM324, LM2902					

Half-Bridge/Full-Bridge Switching Power Supplies (100 W to 500 W/500 W to 1000 W)

- Input line variation: V_{in} + 10%, – 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ) variation: $\delta_{(max)}$ = 0.8
- Maximum working current:

$$I_W = \frac{2\,P_{out}}{\eta \bullet \delta(max) \bullet V_{in(min)} \bullet \sqrt{2}} = \frac{2.8\,P_{out}}{V_{in}} \quad \text{(Half-Bridge)}$$

$$= \frac{P_{out}}{\eta \bullet \delta(max) \bullet V_{in(min)} \bullet \sqrt{2}} = \frac{1.4\,P_{out}}{V_{in}} \quad \text{(Full-Bridge)}$$

- Maximum transistor working voltage: $V_W = V_{in(max)} \bullet \sqrt{2}$ + guardband
- Working frequency: f = 20 kHz to 200 kHz

Basic Half-Bridge Configuration

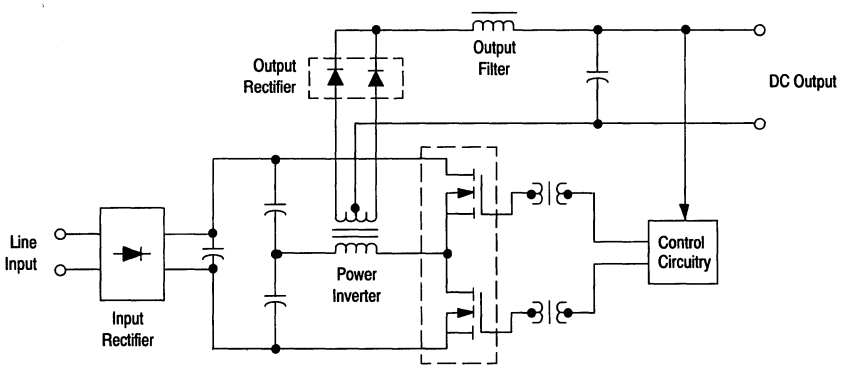


Table 12-3. Half-Bridge Semiconductor Selection Chart

Output Power	100 W		350 W		500 W	
Input Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements: Max Working Current (I_W) Max Working Voltage (V_W)	 2.3 A 190 V	 1.25 A 380 V	 5.7 A 190 V	 3.1 A 380 V	 11.5 A 190 V	 6.25 A 380 V
Power MOSFETs Recommended: Metal (TO-204AA) (TO-3) Plastic (TO-220AB) Plastic (TO-218AC)	 MTM5N35 MTP3N40 —	 MTM2N45 MTP2N45 —	 MTM8N40 — MTH8N40	 MTM4N45 MTP4N45 —	 MTM10N25 MTP10N25 —	 MTM7N45 — MTH7N45
Input Rectifiers: Max Working Current (I_W) Recommended Types	 0.9 A MDA206	 0.5 A MDA210	 2.3 A MDA970-5	 1.25 A MDA210	 4.6 A MDA3506	 2.5 A MDA3510
Output Rectifiers: Recommended types for output voltage of: 5.0 V 10 V 20 V 50 V 100 V	 MBR3035PT MBR3045PT, MUR3010PT MUR1615CT MUR1615CT MUR840A, MUR440		 MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A	
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual-LM358 Quad MC3403, LM324, LM2902					

Half and Full-Bridge

The most popular high power converter is the half-bridge (Figure 12-6). It has two clear advantages over the push-pull and became the favorite rather quickly. First, the transistors never see more than the peak line voltage and the standard 400 V fast switchmode transistors that are readily available may be used. And second, and probably even more important, transformer saturation problems are easily minimized by use of a small coupling capacitor (about 2.0 μF to 5.0 μF) as shown above. Because the primary winding is driven in both directions, a full-wave output filter, rather than half, is now used and the core is actually utilized more effectively. Another more subtle advantage of this circuit is that the input filter capacitors are placed in series across the rectified 220 V line which allows them to be used as the voltage doubler elements on a 120 V line. This still allows the inverter transformer to operate from a nominal 320 V bus when the circuit is connected to either 120 V or 220 V. Finally, this topology allows diode clamps across each transistor to contain destructive switching transients. The designer's dream, of course, is for fast transistors that can handle a clamped inductive load line at rated current. And a few (like the MJE16000 series from Motorola) are beginning to appear on the market. With the improved RBSOA that these transistors feature, less snubbing is required and this improves both the cost and efficiency of these designs.

Figure 12-5. Half-Bridge Converter with Split Windings

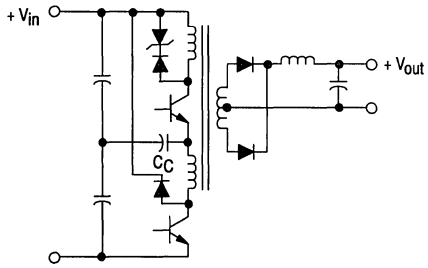
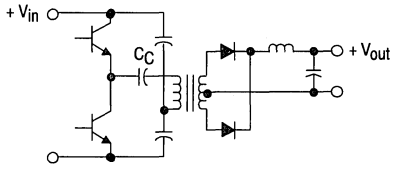


Figure 12-6. Half-Bridge Converter (200 W to 1.0 kW)



Basic Full-Bridge Configuration

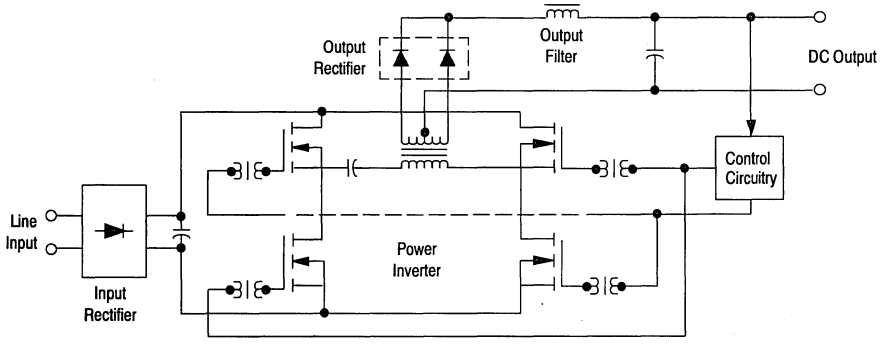


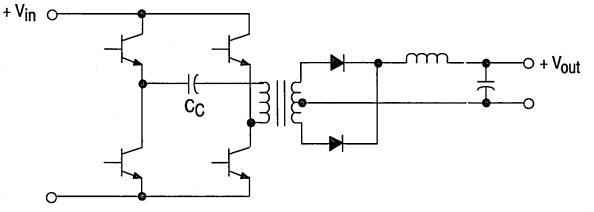
Table 12-4. Full-Bridge Semiconductor Selection Chart

Output Power	500 W		750 W		1000 W	
Input Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements: Max Working Curren (I_W) Max Working Voltage (V_W)	 5.7 A 190 V	 3.1 A 380 V	 8.6 A 190 V	 4.7 A 380 V	 11.5 A 190 V	 6.25 A 380 V
Power MOSFETs Recommended: Metal (TO-204AA) (TO-3) Plastic (TO-220AB) Plastic (TO-218AC)	 MTM8N20 MTP8N20 —	 MTM4N45 MTP4N45 —	 MTM10N25 MTP10N25 —	 MTM7N45 MTP4N45 MTH7N45	 MTM15N20 MTP12N20 MTH15N20	 MTM7N45 — MTH7N45
Input Rectifiers: Max Working Current (I_W) Recommended Types	 4.6 A MDA3506	 2.5 A MDA3510	 7.0 A	 3.8 A	 9.25 A	 5.0 A
Output Rectifiers: Recommended types for output voltage of: 5.0 V 10 V 20 V 50 V 100 V	 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR804PT		 MBR30035CT MUR10010CT* MUR10015CT MUR3015PT* MUR3040PT		 MBR30035CT* MUR10010CT* MUR10015CT* MUR10015CT MUR3040PT	
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual-LM358 Quad MC3403, LM324, LM2902					

*More than one device per leg, matched.

The effective current limit of today's low cost TO-218 discrete transistors (250 mil die) is somewhere in the 10 A to 20 A area. Once this limit is reached, the designer generally changes to the full-bridge configurations shown in Figure 12-7. Because full line rather than half is applied to the primary winding, the power out can be almost double that of the half-bridge with the same switching transistors. Power Darlington transistors are a logical choice for higher power control with current, voltage and speed capabilities allowing very high performance and cost effective designs. Another variation of the half-bridge is the split winding circuit, shown in Figure 12-5. A diode clamp can protect the lower transistor but a snubber or zener clamp must still be used to protect the top transistor from switching transients. Because both emitters are at an AC ground point, expensive drive transformers can now be replaced by lower cost capacitively-coupled drive circuits.

Figure 12-7. Full-Bridge Converter (200 W to 1.0 kW)



SECTION 13
SWITCHING REGULATOR DESIGN EXAMPLES

In addition to the application materials in this data book, Motorola publishes several application notes which contain basic information on the design of power supplies using a variety of Motorola Analog ICs. AN920 Rev. 2 describes in detail the principles of operation of the MC34063A and μA78S40 Switching Regulator Subsystems. Several converter design examples and numerous applications circuits with test data are included in this 38-page application note. The circuit techniques described in this note are also applicable to the MC34163 and MC34165 Power Switching Regulators.

Operating details of the MC34129 Current Mode Switching Regulator Controller, and examples of its use with Motorola SENSEFET™ products, are provided in AN976. The application note AN983 focuses on a 400 W half-bridge power supply design which uses the TL494 PWM control circuit. The TL594 can be used in this same application.

Essentially all of the data sheets for newer power supply control and supervisory circuits include extensive applications information with test conditions and performance results. Many data sheets also include printed circuit board layouts for some key applications so that the designer can evaluate the integrated circuits in an actual power supply. This data book presents all data sheets in their entirety so that the applications information is readily available for each device.

SECTION 14

POWER SUPPLY SUPERVISORY AND PROTECTION CONSIDERATIONS

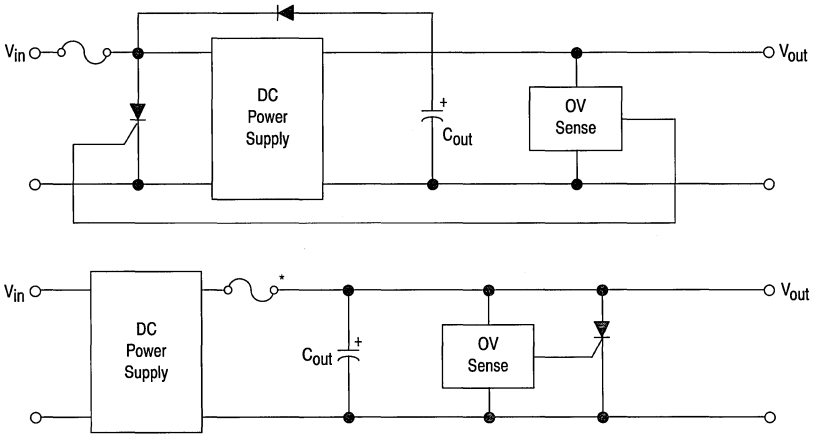
3

The use of SCR crowbar overvoltage protection (OVP) circuits has been, for many years, a popular method of providing protection from accidental overvoltage stress for the load. In light of the recent advances in LSI circuitry, this technique has taken on added importance. It is not uncommon to have several hundred dollars worth of electronics supplied from a single low voltage supply. If this supply were to fail due to component failure or other accidental shorting of higher voltage supply busses to the low voltage bus, several hundred dollars worth of circuitry could literally go up in smoke. The small additional investment in protection circuitry can easily be justified in such applications.

A. The Crowbar Technique

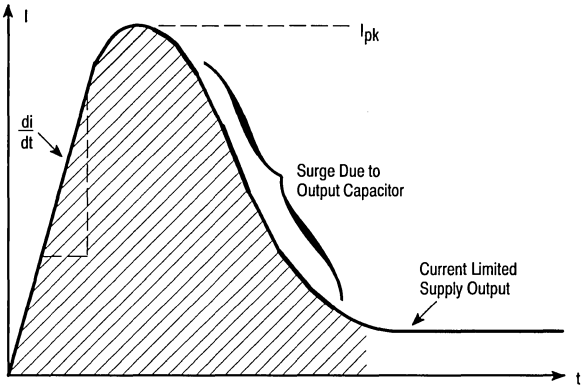
One of the simplest and most effective methods of obtaining overvoltage protection is to use a "crowbar" SCR placed across the equipment's DC power supply bus. As the name implies, the SCR is used much like a crowbar would be, to short the DC supply when an overvoltage condition is detected. Typical circuit configurations for this circuit are shown on Figure 14-1. This method is very effective in eliminating the destructive overvoltage condition. However, the effectiveness is lost if the OVP circuitry is not reliable.

Figure 14-1. Typical Crowbar OVP Circuit Configurations



*Needed if supply not current-limited.

Figure 14-2. Crowbar SCR Surge Current Waveform



B. SCR Considerations

Referring to Figure 14-1, it can easily be seen that, when activated, the crowbar SCR is subjected to a large current surge from the filter and output capacitors. This large current surge, illustrated in Figure 14-2, can cause SCR failure or degradation by any one of three mechanisms: di/dt, peak surge current, or I2t. In many instances the designer must empirically determine the SCR and circuit elements which will result in reliable and effective OVP operation. To aid in the selection of devices for this application, Motorola has characterized several devices specifically for crowbar applications. A summary of these specifications and a selection guide for this application is shown in Table 14-1. This significantly reduces the amount of empirical testing that must be done by the designer. A good understanding of the factors that influence the SCR's di/dt and surge current capability will greatly simplify the total circuit design task.

Table 14-1. Crowbar SCRs

Device Type**	Peak Discharge Current*	di/dt*
MCR67	300 A	75 A/μs
MCR68	300 A	75 A/μs
MCR69	750 A	100 A/μs
MCR70	850 A	100 A/μs
MCR71	1700 A	200 A/μs

* tw = 1.0 μs, exponentially decaying

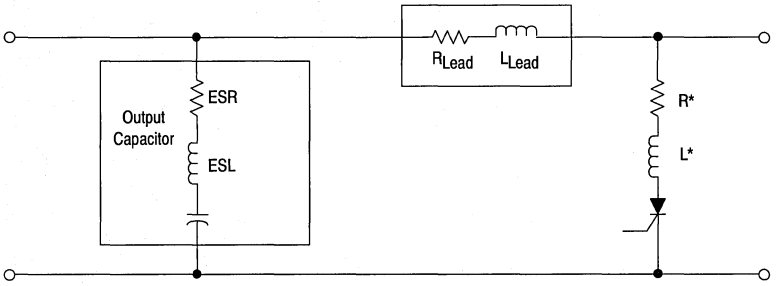
** All devices available with 25, 50, and 100 V ratings

1. di/dt — As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities, depending upon the severity of the occasion.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast <1.0 μs rise time signal will maximize its di/dt capability. A typical maximum di/dt in phase control SCRs of less than 50 A rms rating might be 200 A/μs, assuming a gate current of five times IGT and <1.0 μs rise time. If having done this, a di/dt problem still exists, the designer can also decrease the di/dt of the current saveform by adding inductance in series with the SCR, as shown in Figure 14-3. Of course, this reduces the circuit's ability to rapidly reduce the DC bus voltage, and a tradeoff must be made between speedy voltage reduction and di/dt.

2. Surge Current — If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance, see Figure 14-3) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the DC power supply.

Figure 14-3. Circuit Elements Affecting SCR Surge & di/dt



*R & L empirically determined!

(For additional information on SCRs in crowbar applications refer to *Characterizing the SCR for Crowbar Applications*, Al Pshaenich, Motorola AN789).

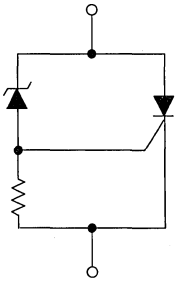
C. The Sense and Drive Circuit

In order to maximize the crowbar SCR's di/dt capability, it should receive a fast rise time high-amplitude gate-drive signal. This must be one of the primary factors considered when selecting the sensing and drive circuitry. Also important is the sense circuitry's noise immunity.

Noise immunity can be a major factor in the selection of the sense circuitry employed. If the sensing circuit has low immunity and is operated in a noisy environment, nuisance tripping of the OVP circuit can occur on short localized noise spikes, which would not normally damage the load. This results in excessive system down time. There are several types of sense circuits presently being used in OVP applications. These can be classified into three types: zener, discrete, and "723."

1. The Zener Sense Circuit — Figure 14-4 shows the use of a zener to trigger the crowbar SCR. This method is NOT recommended since it provides very poor gate drive and greatly decreases the SCR's di/dt handling capability, especially since the SCR steals its own very necessary gate drive as it turns on. Additionally, this method does not allow the trip point to be adjusted except by zener replacement.

Figure 14-4. The Zener Sense Circuit



NO!

2. The Discrete Sense Circuit — A technique which can provide adequate gate drive and an adjustable, low temperature coefficient trip point is shown in Figure 14-5. While overcoming the disadvantages of the zener sense circuit, this technique requires many components and is more costly. In addition, this method is not particularly noise immune and often suffers from nuisance tripping.

3. The "723" Sense Circuit — By using an integrated circuit voltage regulator, such as the industry standard "723" type, a considerable reduction in component count can be achieved. This is illustrated in Figure 14-6. Unfortunately, this technique is not noise immune, and suffers an additional disadvantage in that it must be operated at voltages above 9.5 V.

Figure 14-5. The Discrete Sense Circuit

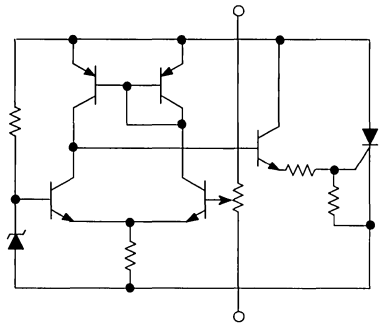
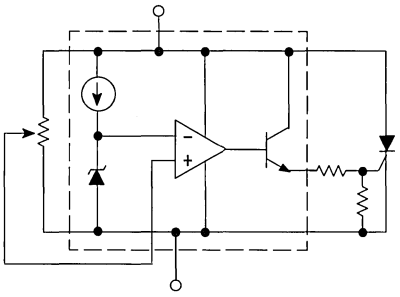


Figure 14-6. The "723" Sense Circuit



4. The MC3423 — To fill the need for a low cost, low complexity method of implementing crowbar overvoltage protection which does not suffer the disadvantages of previous techniques, an IC has been developed for use as an OVP sense and drive circuit, the MC3423.

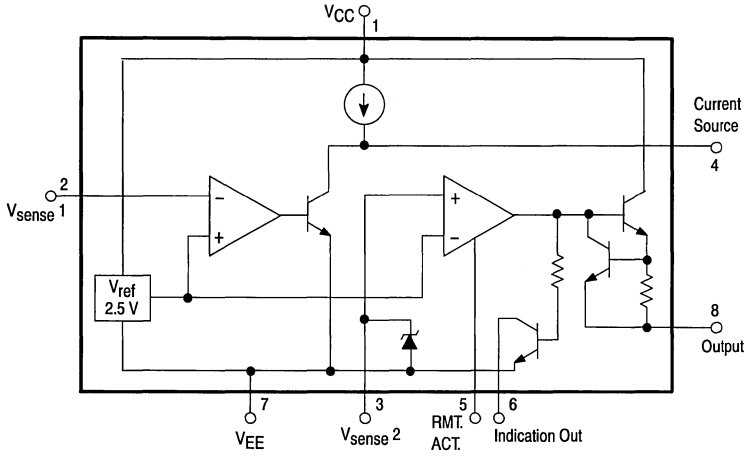
The MC3423 was designed to provide output currents of up to 300 mA with a 400 mA/μs rise time in order to maximize the di/dt capabilities of the crowbar SCR. In addition, its features include:

1. Operation off 4.5 V to 40 V supply voltages.
2. Adjustable low temperature coefficient trip point.
3. Adjustable minimum overvoltage duration before actuation to reduce nuisance tripping in noisy environments.
4. Remote activation input.
5. Indication output.

5. Block Diagram — The block diagram of the MC3423 is shown in Figure 14-7. It consists of a stable 2.6 V reference, two comparators and a high current output. This output, together with the indication output transistor, is activated either by a voltage greater than 2.6 V on Pin 3 or by a TTL/5.0 V CMOS high logic level on the remote activation input, Pin 5.

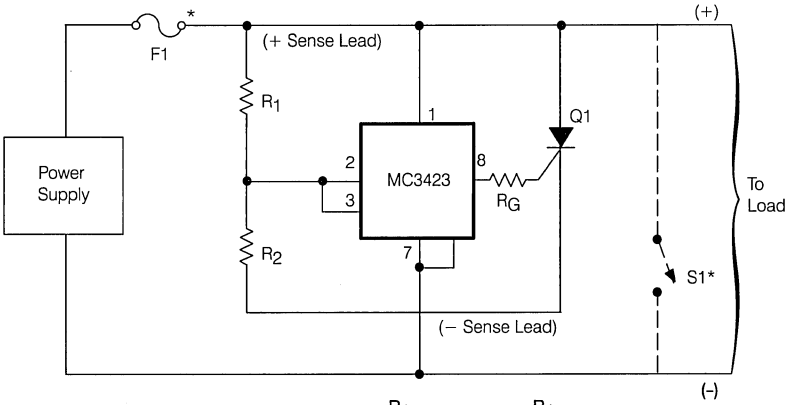
The circuit also has a comparator-controlled current source which can be used in conjunction with and external timing capacitor to set a minimum overvoltage duration (0.5 μs to 1.0 ms) before actuation occurs. This feature allows the OVP circuit to operate in noisy environments without nuisance tripping.

Figure 14-7. MC3423 Block Diagram



6. Basic Circuit Configuration — The basic circuit configuration of the MC3423 OVP is shown in Figure 14-8. In this circuit the voltage sensing inputs of both the internal amplifiers are tied together for sensing the overvoltage condition. The shortest possible propagation delay is thus obtained. The threshold or trip voltage at which the MC3423 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R_1 and R_2. Their values can be determined by the equations given in Figure 14-8 or by the graph shown in Figure 14-9. The switch (S1) shown in Figure 14-8 may be used to reset the SCR crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current-limited supply is used a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

Figure 14-8. MC3423 Basic Circuit Configuration



$$V_{trip} = V_{ref}\left(1 + \frac{R_1}{R_2}\right) \approx 2.6\ V\left(1 + \frac{R_1}{R_2}\right)$$

$R_2 \leq 10\ k\Omega$ for minimum drift

*Needed if supply is not current-limited

7. MC3423 Programmable Configuration — In many instances, MC3423 OVP will be used in a noisy environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 14-10 is used.

Here a capacitor is connected from Pin 3 and Pin 4 to V_{EE}. The value of this capacitor determines the minimum duration of the overvoltage condition (t_D) which is necessary to trip the OVP. The value of C_D can be found from Figure 14-11. The circuit operates in the following manner: when V_{CC} rises above the trip point set by R_1 and R_2, the internal current source begins charging the capacitor, C_D, connected to Pins 3 and 4. If the overvoltage condition remains present long enough for the capacitor voltage, V_{CD} to reach V_{ref}, the output is activated. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

8. Indication Output — An additional output for use as an indicator of OVP activation is provided by the MC3423. This output (Pin 6) is an open-collector transistor which saturates when the MC3423 OVP is activated. It will remain in a saturated state until the SCR crowbar pulls the supply voltage, V_{CC}, below 4.5 V as in Figure 14-10. This output can be used to clock an edge triggered flip-flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

Figure 14-9. R_1 versus Trip Voltage for the MC3423 OVP

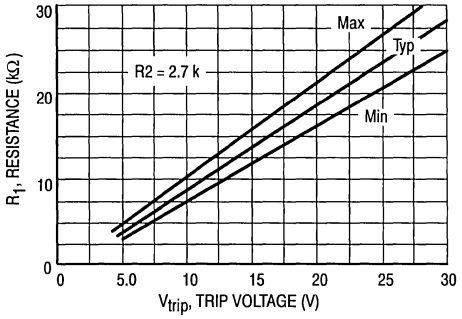
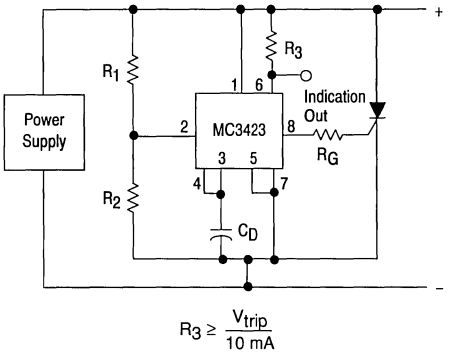


Figure 14-10. MC3423 Configuration for Programmable Minimum Duration of Overvoltage Condition Before Tripping



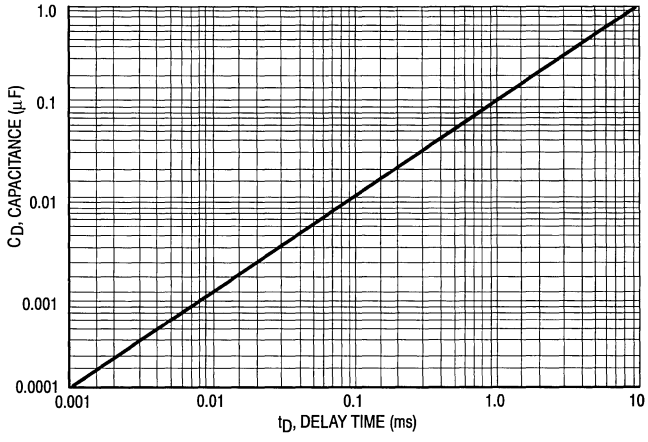
9. Remote Activation Input — Another feature of the MC3423 is its Remote Activation Input, Pin 5. If the voltage on this CMOS/TTL compatible input is held below 0.7 V, the MC3423 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present.

This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the Indication Output of one MC3423 can be used to activate another MC3423, if a single transistor inverter is used to interface the former's Indication Output to the latter's Remote Activation Input.

D. MC3425 Power Supply Supervisory Circuit

In addition to the MC3423 a second IC, the MC3425 has been developed. Similar in many respects to the MC3423, the MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over and undervoltage fault conditions. The block diagram is shown below in Figure 14-12. The Overvoltage (OV) and Undervoltage (UV) Input Comparators are both referenced to an internal 2.5 V regulator. The UV Input Comparator has a feedback activated 12.5 μA current sink (I_H) which is used for programming the input hysteresis voltage (V_H). The source resistance feeding this input (R_H) determines the amount of hysteresis voltage by $V_H = I_H R_H = 12.5 \times 10^{-6} R_H$.

Figure 14-11. C_D versus Minimum Overvoltage Duration, t_D for The MC3423 OVP



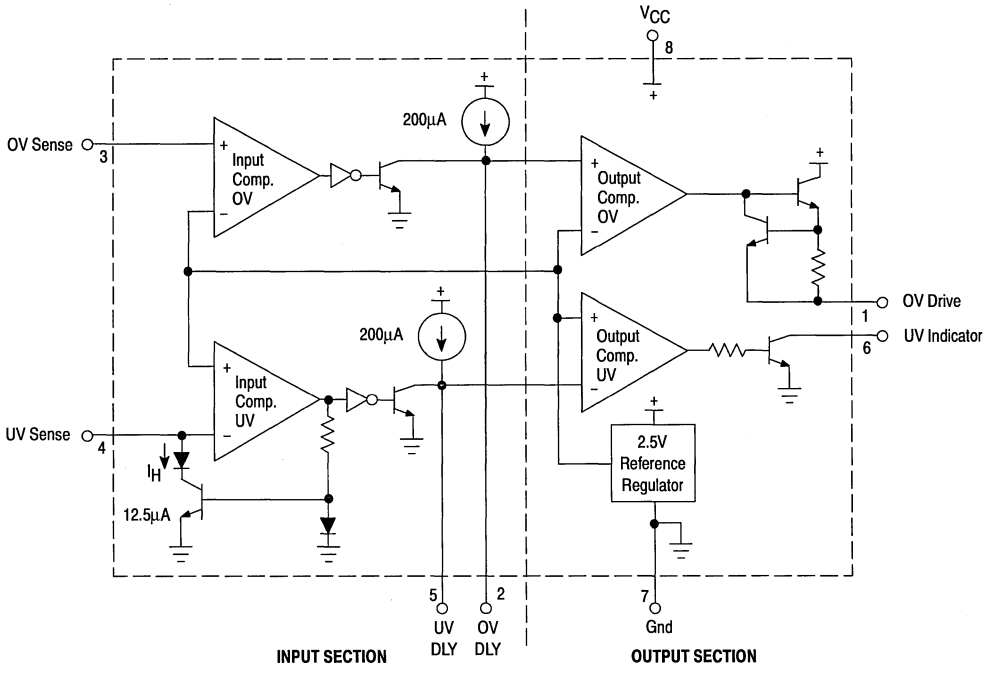
Separate Delay pins (OV DLY, UV DLY) are provided for each channel to independently delay the Drive and Indicator outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source, $I_{DLY(source)}$, of typically 200 μA when the noninverting input voltage is greater than the inverting input level. A capacitor connected from these Delay pins to ground, will establish a predictable delay time (t_{DLY}) for the Drive and Indicator outputs. The Delay pins are internally connected to the non-inverting inputs of the OV and UV Output Comparators, which are referenced to the internal 2.5 V regulator. Therefore, delay time (t_{DLY}) is based on the constant current source, $I_{DLY(source)}$, charging the external delay capacitor (C_{DLY}) to 2.5 V.

$$t_{DLY} = \frac{V_{ref}\, C_{DLY}}{I_{DLY(source)}} = \frac{2.5\, C_{DLY}}{200\ \mu A} = 12500\, C_{DLY}$$

Figure 14-13 provides C_{DLY} values for a wide range of time delays. The Delay pins are pulled low when the respective input comparator's non-inverting input is less than the inverting input. The sink current $I_{DLY(sink)}$ capability of the Delay pins is ≥1.8 mA and is much greater than the typical 200 μA source current, thus enabling a relatively fast delay capacitor discharge time.

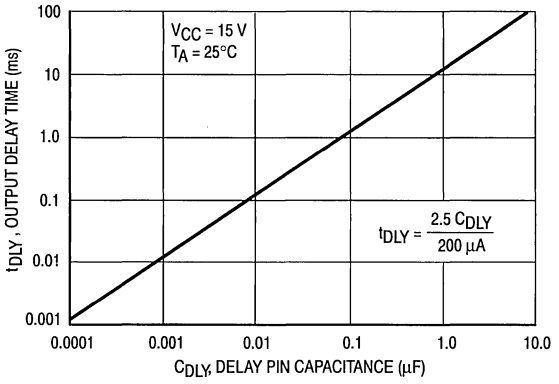
The Overvoltage Drive Output is a current-limited emitter-follower capable of sourcing 300 mA at a turn-on slew rate of 2.0 A/μs, ideal for driving "Crowbar" SCRs. The Undervoltage Indicator Output is an open-collector NPN transistor, capable of sinking 30 mA to provide sufficient drive for LEDs, small relays or shutdown circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded. The MC3425 has an internal 2.5 V bandgap reference regulator with an accuracy of ± 4.0% for the basic devices.

Figure 14-12. Block Diagram



Note: All voltages and currents are nominal.

Figure 14-13. Output Delay Time versus Delay Capacitance



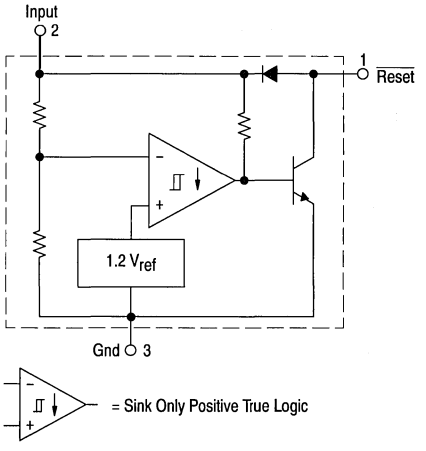
3

E. MC34064 and MC34164 Series

The MC34064 and MC34164 series are two families of undervoltage sensing circuits specifically designed for use as reset controllers in microprocessor-based systems. They offer the designer an economical solution for low voltage detection with a single external resistor. Both parts feature a trimmed bandgap reference, and a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation.

The two families of undervoltage sensing circuits, taken together, cover the needs of the most commonly specified power supplies used in MCU/MPU systems. Key parameter specifications of the MC34164 family were chosen to complement the MC34064 series. The table summarizes critical parameters of both families. The MC34064 fulfills the needs of a 5.0 V ± 5% system and features a tighter hysteresis specification. The MC34164 series covers 5.0 V ± 10% and 3.0 V ± 5% power supplies with significantly lower power consumption, making them ideal for applications where extended battery life is required such as consumer products or hand held equipment.

Applications include direct monitoring of the 5.0 V MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment. The MC34164 is specifically designed for battery powered applications where low bias current (1/25th of the MC34064's) is an important characteristic.



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1. *Characterizing the SCR for Crowbar Applications*, Al Pshaenich, Motorola AN789. **(Out of Print)**
2. *Semiconductor Considerations for DC Power Supply SCR Crowbar Circuits*, Henry Wurzburg, Third National Sold-State Power Conversion Conference, June 25, 1976.
3. *Is a Crowbar Enough?* Willis C. Pierce Jr., Hewlett-Packard, Electronic Design 20, Sept. 27, 1974.
4. *Transient Thermal Response — General Data and Its Use*, Bill Roehr and Brice Shiner, Motorola AN569. **(Out of Print)**

SECTION 15
HEATSINKING

3

A. The Thermal Equation

A necessary and primary requirement for the safe operation of any semiconductor device, whether it be an IC or a transistor, is that its junction temperature be kept below the specified maximum value given on its data sheet. The operating junction temperature is given by:

$$T_J = T_A + P_D \theta_{JA} \quad (15.1)$$

where: T_J = junction temperature (°C)
T_A = ambient air temperature (°C)
P_D = power dissipated by device (W)
θ_{JA} = thermal resistance from junction to ambient air (°C/W)

The junction-to-ambient thermal resistance (θ_{JA}) in Equation (15.1), can be expressed as a sum of thermal resistances as shown below:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \quad (15.2)$$

where: θ_{JC} = junction-to-case thermal resistance
θ_{CS} = case-to-heatsink thermal resistance
θ_{SA} = heatsink-to-ambient thermal resistance

Equation (15.2) applies only when an external heatsink is used. If no heatsink is used, θ_{JA} is equal to the device package θ_{JA} given on the data sheet.

θ_{JC} depends on the device and its package (case) type, while θ_{SA} is a property of the heatsink and θ_{CS} depends on the type of package/heatsink interface employed. Values for θ_{JC} and θ_{SA} are found on the device and heatsink data sheets, while θ_{CS} is given in Table 15-1.

Table 15-1. θ_{CS} For Various Packages & Mounting Arrangements

	θ_{CS}			
	Metal-to-Metal*		Using an Insulator*	
Case	Dry	With Heatsink Compound	With Heatsink Compound	Type
TO-204	0.5°C/W	0.1°C/W	0.36°C/W 0.28°C/W	3 mil MICA Anodized Aluminum
TO-220	1.2°C/W	1.0°C/W	1.6°C/W	2 mil MICA

*Typical values; heatsink surface should be free of oxidation, paint, and anodization

Examples showing the use of Equations (15.1) and (15.2) in thermal calculations are as follows:

Example 1: Find required heatsink θ_{SA} for an MC7805CT, given:

$$T_{J(max)} \text{ (desired)} = +125°C$$
$$T_{A(max)} = +70°C$$
$$P_D = 2.0 \text{ W}$$

Mounted directly to heatsink with silicon thermal grease at interface

1. From MC7805CT data sheet, θ_{JC} = 5°C/W
2. From Table 15-1. θ_{CS} = 1.6°C/W
3. Using Equation (15.1) and (15.2), solve for θ_{SA}:

$$\theta_{SA} = \frac{(T_J - T_A)}{P_D} - \theta_{CS} - \theta_{JC}$$

$$\theta_{SA} = \frac{(125 - 70)}{2} - 5.0 - 1.6 \; (\leq 20.9°C/W \text{ required})$$

Example 2: Find the maximum allowable T_A for an unheatsinked MC78L15CT, given:

$$T_{J(max)} \text{ (desired)} = +125°C$$
$$P_D = 0.25 \text{ W}$$

1. From MC78L15CT data sheet, θ_{JA} = 200°C/W
2. Using Equation (15.1), find T_A:

$$T_A = T_j - P_D \theta_{JA}$$
$$= 125 - 0.25 \; (200)$$
$$= +75°C$$

B. Selecting a Heatsink

Usually, the maximum ambient temperature, power being dissipated, the $T_{J(max)}$, and θ_{JC} for the device being used are known. The required θ_{SA} for the heatsink is then determined using Equations (15.1) and (15.2), as in Example 1. The designer may elect to use a commercially available heatsink, or if packaging or economy demands it, design his own.

1. Commercial Heatsinks

As an aid in selecting a heatsink, a representative listing is shown in Table 15-2. This listing is by no means complete and is only included to give the designer an idea of what is available.

Table 15-2. Commercial Heatsink Selection Guide

TO-204AA (TO-3)	
θ_{SA}*(°C/W)	**Manufacturer/Series or Part Number**
0.3-1.0	Thermalloy — 6441, 6443, 6450, 6470, 6560, 6590, 6660, 6690
1.0-3.0	Wakefield — 641 Thermalloy — 6123, 6135, 6169, 6306, 6401, 6403, 6421, 6423, 6427, 6442, 6463, 6500
3.0-5.0	Wakefield — 621, 623 Thermalloy — 6606, 6129, 6141, 6303 IERC — HP Staver — V3-3-2
5.0-7.0	Wakefield — 690 Thermalloy — 6002, 6003, 6004, 6005, 6052, 6053, 6054, 6176, 6301 IERC — LB Staver — V3-5-2
7.0-10	Wakefield — 672 Thermalloy — 6001, 6016, 6051, 6105, 6601 IERC — LA μP Staver — V1-3, V1-5, V3-3, V3-5, V3-7
10-25	Thermalloy — 6013, 6014, 6015, 6103, 6104, 6105, 6117

*All values are typical as given by the manufacturer or as determined from characteristic curves supplied by the manufacturer.

Table 15-2. Commercial Heatsink Selection Guide (continued)

TO-204AA (TO-5)	
θ_{SA}*(°C/W)	Manufacturer/Series or Part Number
12-20	Wakefield — 260 Thermalloy — 1101, 1103 Staver — V3A-5
20-30	Wakefield — 209 Thermalloy — 1116, 1121, 1123, 1130, 1131, 1132, 2227, 3005 IERC — LP Staver — F5-5
30-50	Wakefield — 207 Thermalloy — 2212, 2215, 225, 2228, 2259, 2263, 2264 Staver — F5-5, F6-5
	Wakefield — 204, 205, 208 Thermalloy — 1115, 1129, 2205, 2207, 2209, 2210, 2211, 2226, 2230, 2257, 2260, 2262 Staver — F1-5, F5-5

TO-204AB	
θ_{SA}*(°C/W)	Manufacturer/Series or Part Number
5.0-10	IERC H P3 Series Staver — V3-7-225, V3-7-96
10-15	Thermalloy — 6030, 6032, 6034 Staver — V4-3-192, V-5-1
20-30	Wakefield — 295 Thermalloy — 6025, 6107
15-20	Thermalloy — 6106 Staver — V4-3-128, V6-2

TO-226AA (TO-92)	
θ_{SA}*(°C/W)	Manufacturer/Series or Part Number
46	Staver F5-7A, F5-8
50	IERC AUR
57	Staver F5-7D
65	IERC RU
72	Staver F1-8, F2-7
80–90	Wakefield 292
85	Thermalloy 2224
DUAL-INLINE-PACKAGE ICs	
20	Thermalloy — 6007
30	Thermalloy — 6010
32	Thermalloy — 6011
34	Thermalloy — 6012
45	IERC — LIC
60	Wakefield — 650, 651

*All values are typical as given by the manufacturer or as determined from characteristic curves supplied by the manufacturer.

Staver Co., Inc.: 41-51 N. Saxon Ave., Bay Shore, NY 11706
IERC: 135 W. Magnolia Blvd., Burbank, CA 91502
Thermalloy: P.O. Box 34829, 2021 W. Valley View Ln. Dallas, TX
Wakefield Engin Ind: Wakefield, MA 01880

2. Custom Heatsink Design

Custom heatsinks are usually either forced air cooled or convection cooled. The design of forced air cooled heatsinks is usually done empirically, since it is difficult to obtain accurate air flow measurements. On the other hand, convection cooled heatsinks can be designed with fairly predictable characteristics. It must be emphasized, however, that any custom heatsink design should be thoroughly tested in the actual equipment configuration to be certain of its performance. In the following sections, a design procedure for convection cooled heatsinks is given.

Obviously, the basic goal of any heatsink design is to produce a heatsink with an adequately low thermal resistance, θ_{SA}. Therefore, a means of determining θ_{SA} is necessary in the design. Unfortunately, a precise calculation method for θ_{SA} is beyond the scope of this book.* However, a first order approximation can be calculated for a convection cooled heatsink if the following conditions are met:

1. The heatsink is a flat rectangular or circular plate whose thickness is smaller than its length or width.
2. The heatsink will not be located near other heat radiating surfaces.
3. The aspect ratio of a rectangular heatsink (length:width) is not greater than 2:1.
4. Unrestricted convective air flow.

For the above conditions, the heatsink thermal resistance can be approximated by:

$$\theta_{SA} \simeq \frac{1}{A\eta\,(F_C h_C + \epsilon H_r)} \quad (°C/W) \tag{15.3}$$

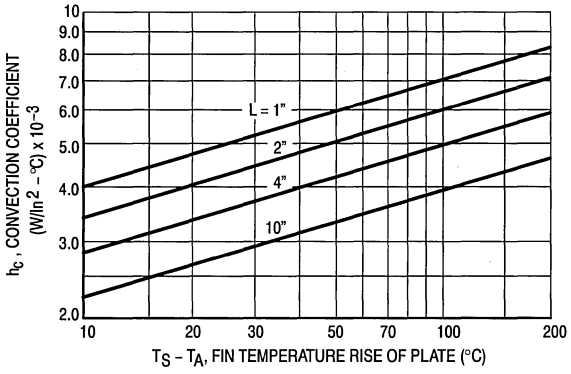
where: A = area of the heatsink surface
η = heatsink effectiveness
F_C = convective correction factor
h_C = convection heat transfer coefficient
ϵ = emissivity
H_r = normalized radiation heat transfer coefficient

The convective heat transfer coefficient, h_C, can be found from Figure 15-1. Note that it is a function of the heatsink fin temperature rise, $T_S - T_A$, and the heatsink significant dimension, L. The fin temperature rise, $T_S - T_A$, is given by:

$$T_S - T_A = \theta_{SA}\, P_D \tag{15.4}$$

where: T_S = heatsink temperature
T_A = ambient temperature
θ_{SA} = heatsink-to-ambient thermal resistance
P_D = power dissipated

Figure 15-1. Convection Coefficient (h_C)



*If greater precision is desired, or more information on heat flow and heatsinking is sought, consult the references list at the end of this section.

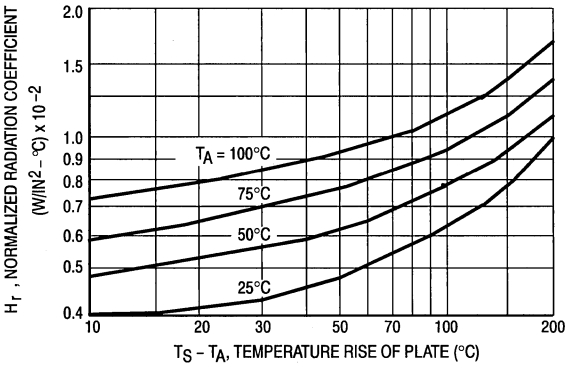
The significant heatsink dimension (L) is dependent on the heatsink shape and mounting place and is given in Table 15-3. The convective correction factor (F_C) is likewise dependent on shape and mounting plane of the heatsink and is also given in Table 15-3.

Table 15-3. Significant Dimension (L) and Correction Factor (F_C) for Convection Thermal Resistance

Surface	Significant Dimension L		Correction Factor F_C	
	Position	L	Position	F_C
Rectangular Plane	Vertical	Height (max 2 ft)	Vertical Plane	1.0
	Horizontal	$\frac{\text{length} \times \text{width}}{\text{length} + \text{width}}$	Horizontal Plane both surfaces exposed	1.35
Circular Plane	Vertical	$\pi / 1 \times$ diameter	Top only exposed	0.9

The normalized radiation heat transfer coefficient (H_r) is dependent on the ambient temperature (T_A) and the heatsink temperature rise ($T_S - T_A$) given by Equation (15.4). H_r can be determined from Figure 15-2.

Figure 15-2. Normalized Radiation Coefficient (H_r)



The emissivity (ϵ) can be found in Table 15-4 for various heatsink surfaces.

Table 15-4. Typical Emissivities of Common Surfaces

Surface	Emissivity (ϵ)
Alodine on Aluminum	0.15
Aluminum, Anodized	0.7 to 0.9
Aluminum, Polished	0.05
Copper, Polished	0.07
Copper, Oxidized	0.70
Rolled Sheet Steel	0.66
Air Drying Enamel (any color)	0.85 to 0.91
Oil Paints (any color)	0.92 to 0.96
Varnish	0.89 to 0.93

Finally, the heatsink efficient, η, can be found from the nomograph of Figure 15-3. Use of the nomograph is as follows:

a) Find $h_T = Fchc + \epsilon H_r$ from Figures 15-1, 15-2 and Tables 15-3 and 15-4, and locate this point on the nomograph.

b) Draw a line from h_T through chosen heatsink fin thickness (x) to find α.

c) Determine D for the heatsink shape as given in Figure 15-4 and draw a line from this point through α, which was found in (b), to determine η.

d) If power dissipating element is not located at heatsink's center of symmetry, multiply η by 0.7 (for vertically mounted plates only).

Note that in order to calculate θ_{SA} from Equation (15.3), it is necessary to know the heatsink size. Therefore, in order to arrive at a suitable heatsink design, a trial size is selected, its θ_{SA} evaluated, and the original size reduced or enlarged as necessary. This process is iterated until the smallest heatsink is obtained that has the required θ_{SA}. The following design example is given to illustrate this procedure.

Figure 15-3. Fin Effectiveness Nomogram for Symmetrical Flat, Uniformly Thick Fins

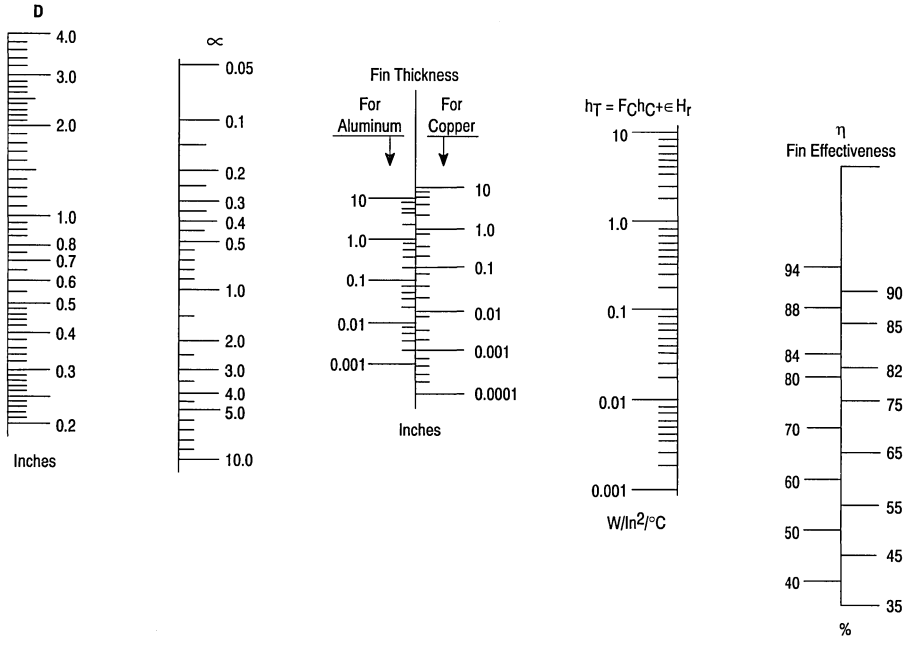


Figure 15-4. Determination of D for Use in η Nomograph of Figure 15-3

$D \cong \sqrt{\frac{ab}{\pi}}$, if $a,b \geq S$ & $b \leq 2a$

$D \simeq \frac{d}{2}$, if $d \gg s$

Heatsink Design Example

Design a flat rectangular heatsink for use with a horizontally mounted power device on a PC card, given the following:

1. Heatsink θ_{SA} = 25°C/W
2. Power to be dissipated, P_D = 2.0 W
3. Maximum ambient temperature, T_A = 50°C
4. Heatsink to be constructed from 1/8″ (0.125″) thick anodized aluminum.

3

a) First, a trial heatsink is chosen: 2″ × 3″ (experience will simplify this selection and reduce the number of necessary iterations.)

b) The factors in Equation (15.3) are evaluated by using the Figures and Tables given:

A = 2″ × 3″ = 6 sq. in.

L = 6/5″ = 1.2 in. (from Table 15-3)

$T_S - T_A$ = 50°C (from Figure 15-4)

h_C = 5.8×10^{-3} W/in^2 – °C (from Figure 15-1)

F_C = 0.9 (from Table 15-3)

H_r = 6.1×10^{-3} W/in^2 – °C (from Figure 15-2)

ϵ = 0.9 (from Table 15-4)

h_T = $Fchc + H_{r\epsilon}$ = 10.7×10^{-3} W/in^2 – °C

α = 0.13 (from Figure 15-3)

D = 1.77 (from Figure 15-4)

$\eta > 0.94 \simeq 1$ (from Figure 15-3)

c) Using Equation (15.3), find θ_{SA}:

$$\theta_{SA} \simeq \frac{1}{A\eta\,(Fchc + \epsilon H_r)} = 16.66°C/W < 25°C/W$$

d) Since 2″ × 3″ is too large, try 2″ × 2″. Following the same procedure, θ_{SA} is found to be 25°C/W, which exactly meets the design requirements.

SOIC MINIATURE IC PLASTIC PACKAGE

Thermal Information

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\,(typ)}$$

where: $P_{D(T_A)}$ = power dissipation allowable at a given operating ambient temperature,

$T_{J(max)}$ = maximum operating junction temperature as listed in the maximum ratings section,

T_A = desired operating ambient temperature,

$R_{\theta JA}$ (typ) = typical thermal resistance junction-to-ambient.

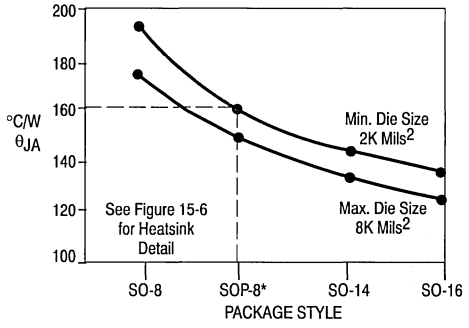
Maximum Ratings

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70 – 40 to +85	°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C

THERMAL RESISTANCE OF SOIC PACKAGES

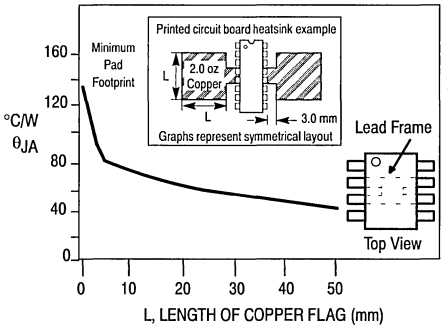
Measurement specimens are solder mounted on a Philips SO test board #7322-078, 80873 in still air. No auxiliary thermal conduction aids are used. As thermal resistance varies inversely with die area, a given package takes thermal resistance values between the max and min curves shown. These curves represent the smallest (2000 square mils) and largest (8000 square mils) die areas expected to be assembled in the SOIC package.

Figure 15-5. Thermal Resistance, Junction-to-Ambient (°C/W)



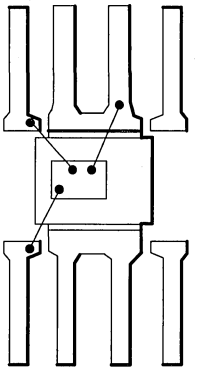
Data taken using Philips SO test board #7322-078, 80873
*SOP-8 using standard SO-8 footprint — minimum pad size

Figure 15-6. Thermal Resistance for SOP-8 Package Die 2K mils²



SOP-8 Packaged Devices

Three families of voltage regulators and one family of programmable precision references have been introduced in a surface mounted package which was developed by the Bipolar Analog IC Division. The SOP-8 package has external dimensions which are identical to the standard SO-8 surface mount device, but the center four leads of the 8-lead device are all connected to the leadframe die flag. This internal modification decreases the package thermal resistance and therefore increases its power dissipation capability. This advantage is fully realized when the package is mounted on a printed circuit board with a single pad for the four center leads. This large area of copper then acts as an external heat spreader, efficiently conducting heat away from the package.



The 100 mA output current MC78LXX series of positive voltage regulators (in four voltages), the 100 mA MC79LXX series of negative regulators (in three voltages), and the 100 mA LM317L positive adjustable voltage regulator have been introduced in the SOP-8. In addition, the TL431 family of precision voltage references (in two temperature ranges) is available in the SOP-8 package.

THERMAL RESISTANCE OF DPAK PACKAGE

The evaluation was performed using an active device (4900 square mils) mounted on 2.0 ounce copper foil epoxied to a GIO type printed circuit board. Measurements were made in still air and no auxiliary thermal conduction aids were used. The size of a square copper pad was varied, and all measurements were made with the unit mounted as shown in Figure 15-7. The curve shown in Figure 15-8 is a plot of junction-to-air thermal resistance versus the length of the square copper pad in millimeters. This shows that when the DPAK is mounted on a 10 mm × 10 mm square pad of 2.0 ounce copper it has a thermal resistance which is comparable to a TO-220 device mounted vertically without additional heatsinking.

Figure 15-7. PC Board Heatsink Example

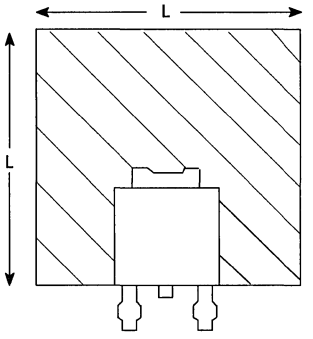
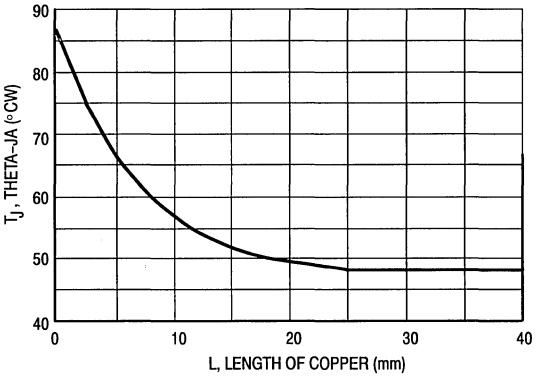
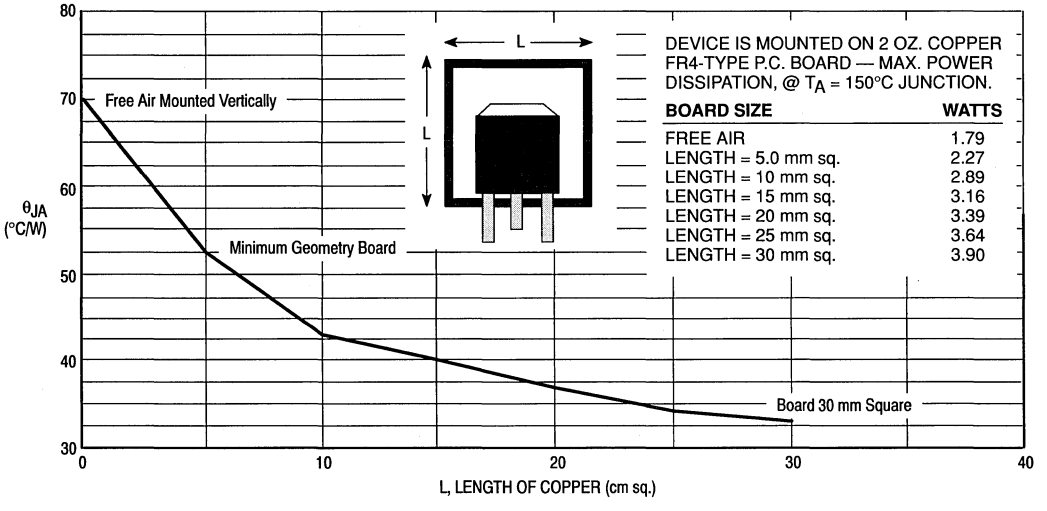


Figure 15-8. DPAK Thermal Evaluation



IC D^2PAK THERMAL EVALUATION



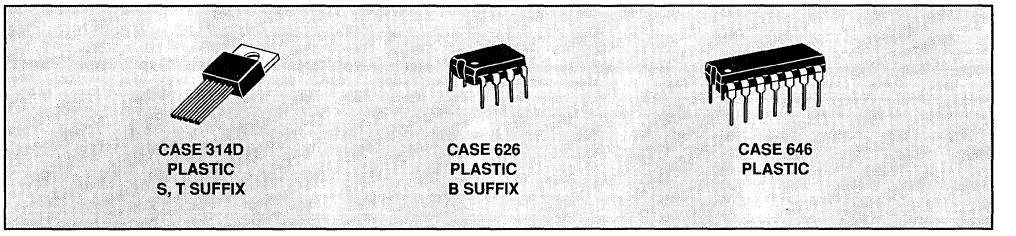
Power/Motor Control Circuits

In Brief . . .

With the expansion of electronics into more and more mechanical systems there comes an increasing demand for simple but intelligent circuits that can blend these two technologies. In the past, the task of power/motor control was once accomplished with discrete devices. But today this task is being performed by bipolar IC technology due to cost, size, and reliability constraints. Motorola offers integrated circuits designed to anticipate the requirements for both simple and sophisticated control systems, while providing cost effective solutions to meet the needs of the applications.

Power Controllers

An assortment of battery and AC line-operated control ICs for specific applications is shown. They are designed to enhance system performance and reduce complexity in a wide variety of control applications.



CASE 314D
PLASTIC
S, T SUFFIX

CASE 626
PLASTIC
B SUFFIX

CASE 646
PLASTIC

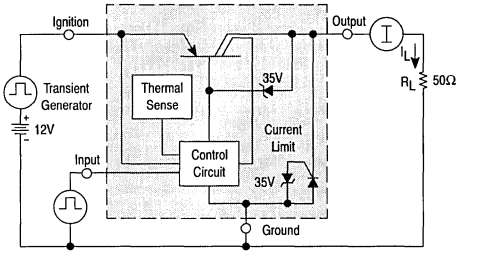
4

High Side Driver Switch

MC3399T T_J = −40° to +150°C, Case 314D

The MC3399T is a high side driver switch that is designed to drive loads from the positive side of the power supply. The output is controlled by a TTL compatible Enable pin. In the ON state, the device exhibits very low saturation voltages for load currents in excess of 750 mA. The device also protects the load from positive or negative-going high voltage transients by becoming an open circuit and isolating the transient for its duration from the load.

The MC3399T is fabricated on a power BiMOS process which combines the best features of Bipolar and MOS technologies.



The mixed technology provides higher gain PNP output devices and results in Power Integrated Circuits with reduced quiescent current.

Zero Voltage Switches

CA3079/CA3059 T_A = −40° to +85°C, Case 646

These devices are designed for thyristor control in a variety of AC power switching applications for AC input voltages of 24 V, 120 V, 208/230 V, and 227 V at 50/60 Hz.

Limiter-Power Supply — Allows operation directly from an AC line.

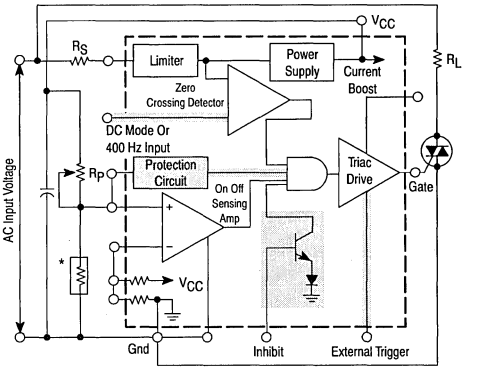
Differential On/Off Sensing Amplifier — Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented.

Zero-Crossing Detector — Synchronizes the output pulses to the zero voltage point of the AC cycle. Eliminates RFI when used with resistive loads.

Triac Drive — Supplies high-current pulses to the external power controlling thyristor.

Protection Circuit (CA3059 only) — A built-in circuit may be actuated, if the sensor opens or shorts, to remove the drive circuit from the external triac.

Inhibit Capability (CA3059 only) — Thyristor firing may be inhibited by the action of an internal diode gate.



* NTC Sensor
NOTE: Shaded area not included with CA3079.

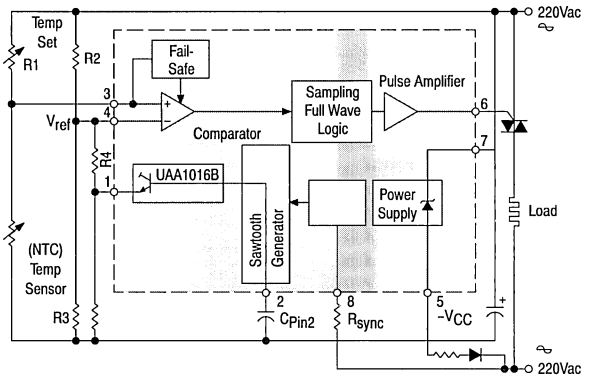
High Power DC Comparator Operation (CA3059 only) Operation in this mode is accomplished by connecting Pin 7 to Pin 12 (thus overriding the action of the zero-crossing detector).

Zero Voltage Controller

UAA1016B T_A = –20° to +100°C, Case 626

This device is designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. They provide the following features:
They provide the following features:

- Proportional Temperature Control over an Adjustable Band
- Adjustable Burst Frequency (to Comply with Standards)
- Sensor Fail-Safe
- No DC Current Component through the Main Line (to Comply with Standards)
- Negative Output Current Pulses (Triac Quadrants 2 and 3)
- Direct AC Line Operation
- Low External Components Count

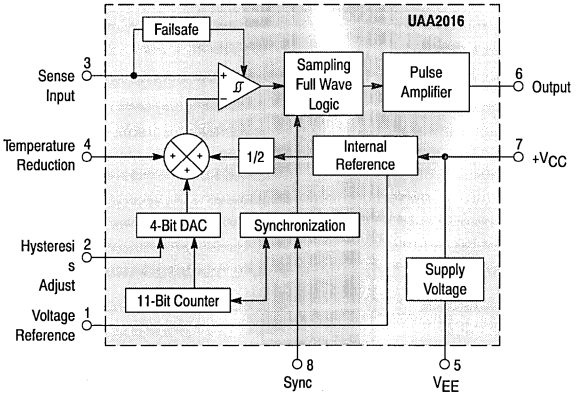


Zero Voltage Switch Power Controller

UAA2016P, D T_A = –20° to +85°C, Case 626, 751

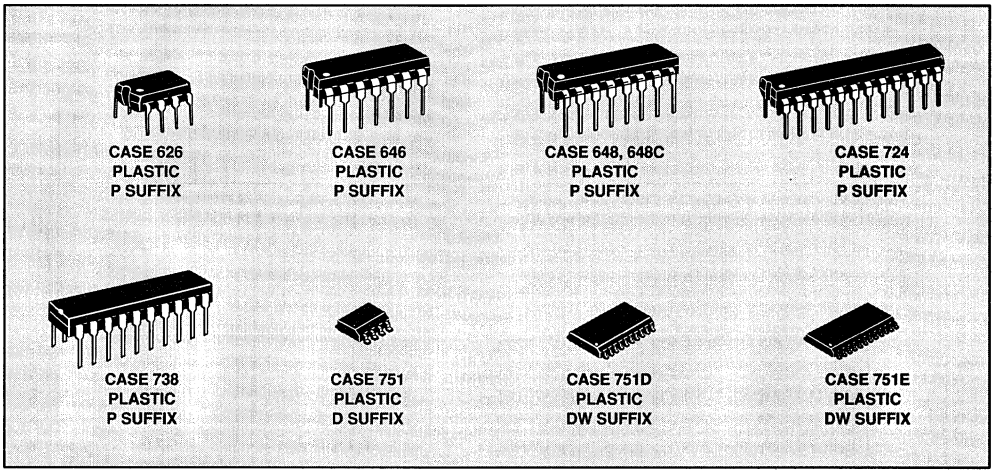
The UAA2016 is designed to drive triacs with the Zero Voltage technique which allows RFI-free power regulation of resistive loads. Operating directly on the AC power line its main application is the precision regulation of electrical heating systems such as panel heaters or irons.

A built-in digital sawtooth waveform permits proportional temperature regulation action over a ±1°C band around the set point. For energy savings there is a programmable temperature reduction function, and for security a sensor failsafe inhibits output pulses when the sensor connection is broken. Preset temperature (i.e. defrost) application is also possible. In applications where high hysteresis is needed, its value can be adjusted up to 5°C around the set point. All these features are implemented with a very low external component count.



Motor Controllers

This section contains integrated circuits designed for cost effective control of specific motor families. Included are controllers for brushless, dc servo, stepper, and universal type motors.



4

Brushless DC Motor Controllers

Advances in magnetic materials technology and integrated circuits have contributed to the unprecedented rise in popularity of brushless DC motors. Linear control ICs are making the many features and advantages of brushless motors available at a much more economical price. Motorola offers a family of monolithic integrated brushless DC motor controllers. These ICs provide a choice of control functions which allow many system features to be easily implemented at a fraction of the cost of discrete solutions. The following table summarizes and compares the features of Motorola's brushless motor controllers.

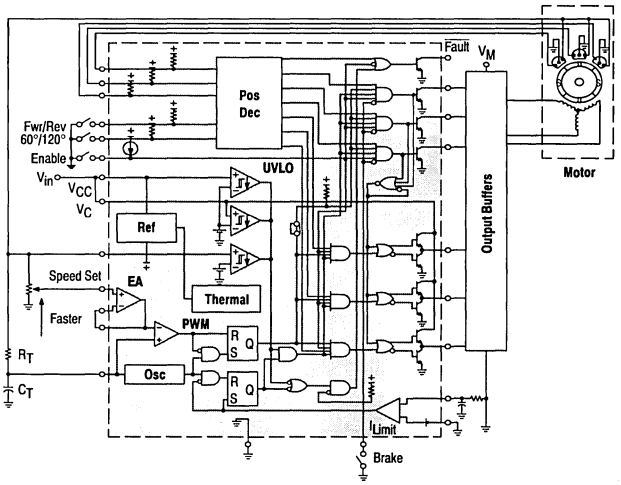
Features Summary for Motorola Brushless DC Motor Controllers

	Operating Voltage Range (V)		Undervoltage Lockout	Internal Thermal Shutdown	Fwd/Rev Control	Sensor Electrical Phasing	Output Enable	Output Drivers		6.25 V Reference Output	Current Sense Comparator Input(s)	Error Amplifier	FAULT Output	Separate Drive V_C	Brake Input	Suffix/ Package
Device	V_{CC}	V_C	Undervoltage Lockout	Internal Thermal Shutdown	Fwd/Rev Control	Sensor Electrical Phasing	Output Enable	Totem Pole (Bottom)	Open Collector (Top)	6.25 V Reference Output	Current Sense Comparator Input(s)	Error Amplifier	FAULT Output	Separate Drive V_C	Brake Input	Suffix/ Package
MC33033	10-30		✓	✓	✓	60°/300° and 120°/240°	✓	✓	✓	✓	Noninv. Only	✓				P/738 DW/751D
MC33035	10-40	10-30	✓	✓	✓	60°/300° and 120°/240°	✓	✓	✓	✓	Noninv. and Inv.	✓	✓	✓	✓	P/724 DW/751E

High Performance DC Brushless Motor Controller

MC33035P, DW T_A = −40° to +85°C, Case 724, 751E

The MC33035 is a second generation high performance brushless DC motor controller which contains all of the active functions required to implement a full featured open-loop motor control system. While being pin-compatible with its MC33034 predecessor, the MC33035 offers additional features at a lower price. The two additional features provided by the MC33035 are a pin which allows the user to select 60°/300° or 120°/240° sensor electrical phasings, and access to both inverting and noninverting inputs of the current sense comparator. The earlier devices had two part numbers which were needed to support the different sensor phasings, and the inverting input to the current sense comparator was internally grounded. All of the control and protection features of the MC33034 are also provided in the MC33035.



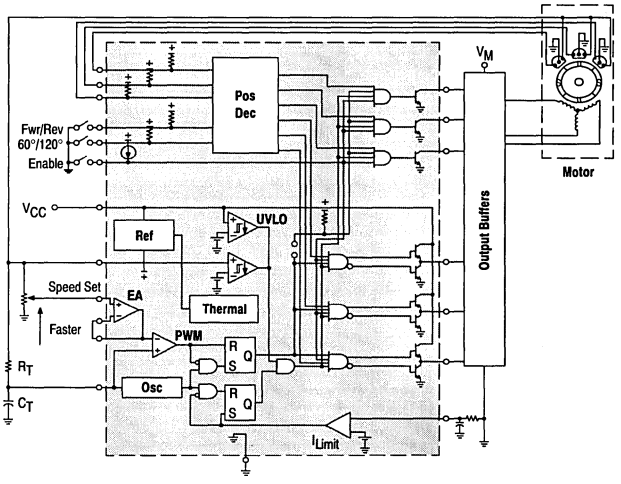
4

Brushless DC Motor Controller

MC33033P, DW T_A = −40° to +85°C, Case 738, 751D

The MC33033 is a lower cost second generation brushless DC motor controller which has evolved from the full featured MC33034 and MC33035 controllers. The MC33033 contains all of the active functions needed to implement a low cost open-loop motor control system. This IC has all of the key control and protection functions of the two full featured devices with the following secondary features deleted: separate drive-circuit supply and ground pins, the brake input, and the fault output signal. Like its MC33035 predecessor, the MC33033 has a control pin which allows the user to select 60°/300° or 120°/240° sensor electrical phasings.

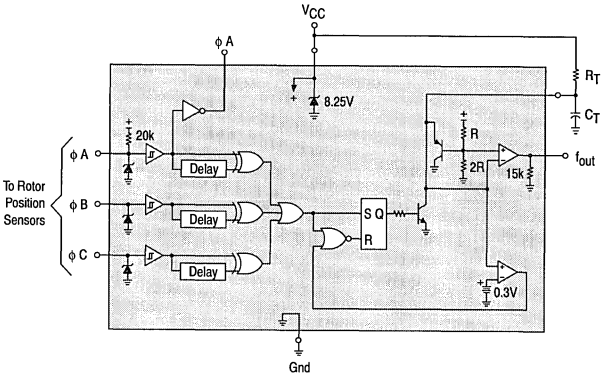
Because of its low cost, the MC33033 can efficiently be used to control brush DC motors as well as brushless. A brush DC motor can be driven using two of the three drive output phases provided in the MC33033, while the Hall sensor input pins are selectively tied to V_{ref} or ground. Other features such as forward/reverse, output enable, speed control, current limiting, undervoltage lockout and internal thermal shutdown will still remain functional.



Closed-Loop Brushless Motor Adapter

MC33039P, D T_A = −40° to +85°C, Case 626, 751

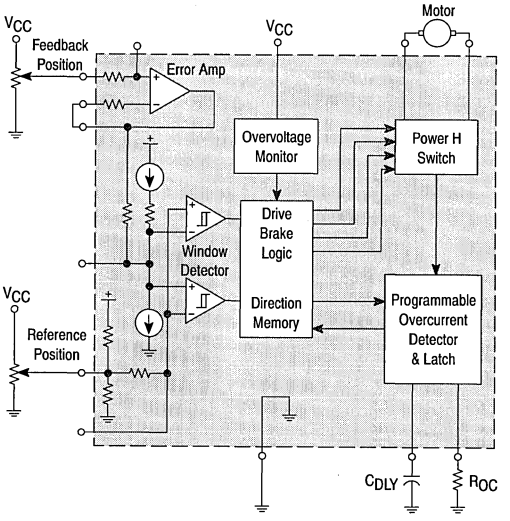
The MC33039P,D is a high performance close-loop speed control adapter specifically designed for use in brushless dc motor control systems. Implementation will allow precise speed regulation without the need for a magnetic or optical tachometer. These devices contain three input buffers each with hysteresis for noise immunity, three digital edge detectors, a programmable monostable, and an internal shunt regulator. Also included is an inverter output for use in systems that require conversion of sensor phasing. Although this device is primarily intended for use with the MC33033/35 brushless motor controllers, it can be used cost effectively in many other closed-loop speed control applications.



DC Servo Motor Controller/Driver

MC33030P T_A = −40° to +85°C, Case 648C

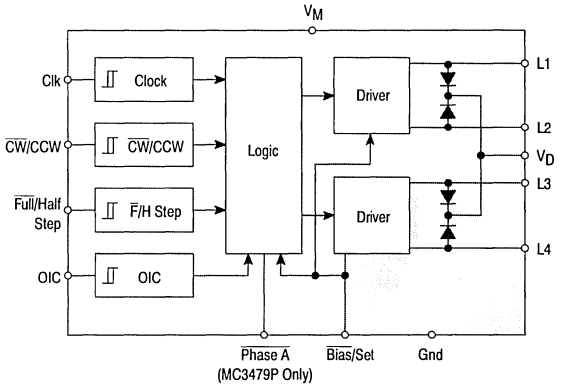
A monolithic dc servo motor controller providing all active functions necessary for a complete closed loop system. This device consists of an on-chip op amp and window comparator with wide input common mode range, drive and brake logic with direction memory, a power H switch driver capable of 1.0 A, independently programmable over current monitor and shutdown delay, and over voltage monitor. This part is ideally suited for almost any servo positioning application that requires sensing of temperature, pressure, light, magnetic flux, or any other means that can be converted to a voltage.



Stepper Motor Driver

MC3479P T_A = 0° to +70°C, Case 648C
SAA1042V, AV T_A = 0° to +70°C, Case 648C

These Stepper Motor Drivers provide up to 500 mA of drive per coil for two phase 6.0 V to 24 V stepper motors. Control logic is provided to accept commands for clockwise, counter clockwise and half or full step operation. The MC3479P has an added Output Impedance Control (OIC) and a $\overline{\text{Phase A}}$ drive state indicator (not available on SAA1042 devices).



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Universal Motor Speed Controllers

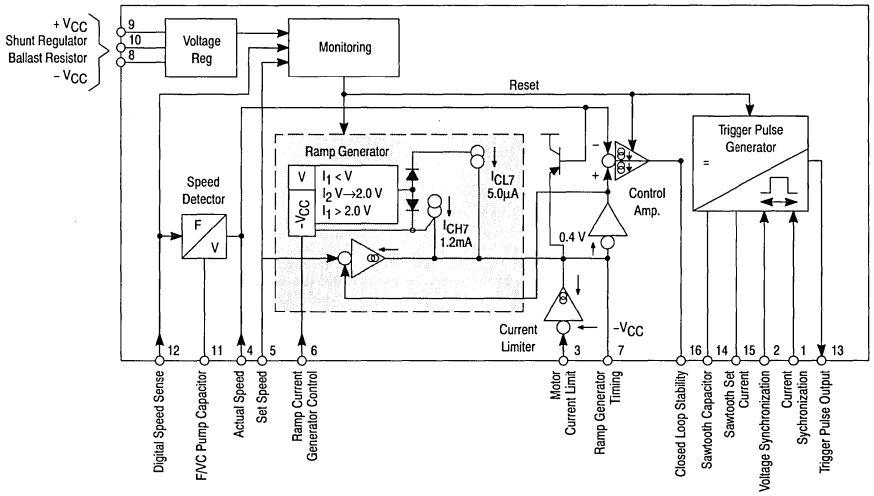
TDA1085A T_A = 0° to +70°C, Case 648

This device contains all the necessary functions for the speed control of universal (ac/dc) motors in an open or closed loop configuration. Facility for defining the initial speed/time characteristic. The circuit provides a phase angle varied trigger pulse to the motor control triac.

- Guaranteed Full Wave Triac Drive
- Soft-Start from Power-up
- On-Chip Frequency/Voltage Converter and Ramp Generator
- Current Limiting Incorporated
- Direct Drive from AC Line

TDA1085C T_A = −10° to +120°C, Case 648

Similar to the TDA1085A, but designed for commercial washing machine service.

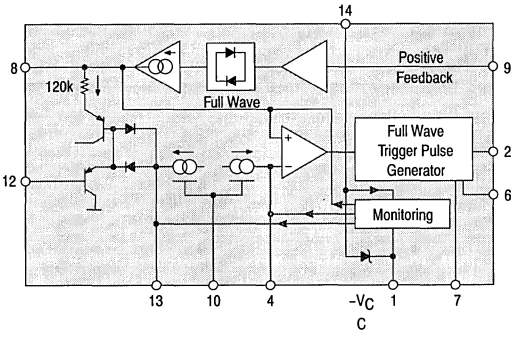


Triac Phase Angle Controller

TDA1185A T_A = 0° to +70°C, Case 646

This device generates controlled triac triggering pulses and allows tacholess speed stabilization of universal motors by an integrated positive feedback function.

- Low Cost External Components Count
- Optimum Triac Firing (2nd and 3rd Quadrants)
- Repetitive Trigger Pulses when Triac Current is Interrupted by Motor Brush Bounce
- Triac Current Sensed to Allow Inductive Loads
- Soft-Start
- Power Failure Detection and General Circuit Reset
- Low Power Consumption: 1.0 mA



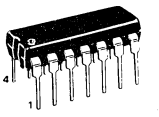
Power Controller

Motor Controllers

CA3059
CA3079

ZERO VOLTAGE SWITCHES

SILICON MONOLITHIC INTEGRATED CIRCUITS



PLASTIC PACKAGE
CASE 646

4

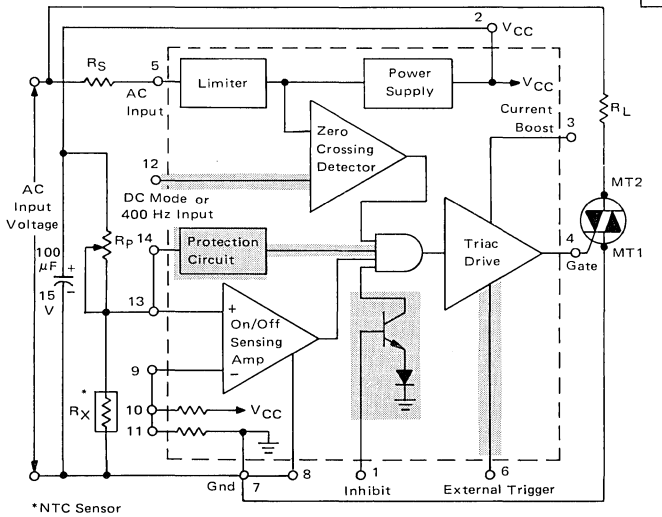
ZERO VOLTAGE SWITCHES

This series is designed for thyristor control in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 277 V @ 50/60 Hz.

Applications:

- Relay Control
- Heater Control
- Valve Control
- Lamp Control
- Synchronous Switching of Flashing Lights
- On-Off Motor Switching
- Differential Comparator With Self-Contained Power Supply for Industrial Applications
- Photosensitive Control
- Power One-Shot Control

FIGURE 1 – FUNCTIONAL BLOCK DIAGRAM



*NTC Sensor
NOTE: Shaded Area Not Included With CA3079.

AC Input Voltage (50/60 Hz) vac	Input Series Resistor (R_S) kΩ	Dissipation Rating for R_S W
24	2.0	0.5
120	10	2.0
208/230	20	4.0
277	25	5.0

FUNCTIONAL BLOCK DESCRIPTION

1. **Limiter-Power Supply** — Allows operation of the CA3059/79 directly from an ac line. Suggested dropping resistor (R_S) values are given in the table below.
2. **Differential On/Off Sensing Amplifier** — Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented using this block.
3. **Zero-Crossing Detector** — Synchronizes the output pulses to the zero voltage point of the ac cycle. This synchronization eliminates RFI when used with resistive loads.
4. **Triac Drive** — Supplies high-current pulses to the external power controlling thyristor.
5. **Protection Circuit (CA3059 only)** — A built-in circuit may be actuated, if the sensor opens or shorts, to remove the drive current from the external triac.
6. **Inhibit Capability (CA3059 only)** — Thyristor firing may be inhibited by the action of an internal diode gate at Pin 1.
7. **High Power DC Comparator Operation (CA3059 only)** — Operation in this mode is accomplished by connecting Pin 7 to Pin 12 (thus overriding the action of the zero-crossing detector). When Pin 13 is positive with respect to Pin 9, current to the thyristor is continuous.

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
DC Supply Voltage (Between Pins 2 and 7)	CA3059 CA3079	V_{CC}	 12 10	Vdc
DC Supply Voltage (Between Pins 2 and 8)	CA3059 CA3079	V_{CC}	 12 10	Vdc
Peak Supply Current (Pins 5 and 7)		$I_{5,7}$	±50	mA
Fail-Safe Input Current (Pin 14)		I_{14}	2.0	mA
Output Pulse Current (Pin 4) (Note 1)		I_{out}	150	mA
Junction Temperature		T_J	150	°C
Operating Temperature Range		T_A	−40 to +85	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (Operation @ 120 Vrms, 50–60 Hz, T_A = 25°C, [Note 2])

Characteristic	Test Circuits	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	Fig. 2	V_S				Vdc
Inhibit Mode						
R_S = 10 k, I_L = 0			6.1	6.5	7.0	
R_S = 5.0 k, I_L = 2.0 mA			—	6.1	—	
Pulse Mode						
R_S = 10 k, I_L = 0			6.0	6.4	7.0	
R_S = 5.0 k, R_L = 2.0 mA			—	6.2	—	
Gate Trigger Current (V_{GT} = 1.0 V, Pins 3 and 2 connected)	Fig. 3	I_{GT}	—	160	—	mA
Peak Output Current, Pulsed	Fig. 3	I_{OM}				mA
With Internal Power Supply, V_{GT} = 0						
Pin 3 Open			50	125	—	
Pins 3 and 2 Connected			90	190	—	
With External Power Supply, V_{CC} = 12 V, V_{GT} = 0	Fig. 4					
Pin 3 Open			—	230	—	
Pins 3 and 2 Connected			—	300	—	
Inhibit Input Ratio (Ratio of Voltage @ Pin 9 to Pin 2)	Fig. 5	V_9/V_2	0.465	0.485	0.520	—
Total Gate Pulse Duration (C_{Ext} = 0)	Fig. 6					μs
Positive dv/dt		t_p	70	100	140	
Negative dv/dt		t_n	70	100	140	
Pulse Duration After Zero Crossing (C_{Ext} = 0, R_{Ext} = ∞)	Fig. 6					μs
Positive dv/dt		t_{p1}	—	50	—	
Negative dv/dt		t_{n1}	—	60	—	
Output Leakage Current Inhibit Mode (Note 3)	Fig. 3	I_4	—	0.001	10	μA
Input Bias Current CA3059 CA3079	Fig. 7	I_{IB}	— —	0.15 0.15	1.0 2.0	μA
Common Mode Input Voltage Range (Pins 9 and 13 Connected)	—	V_{CMR}	—	1.4 to 5.0	—	Vdc
Inhibit Input Voltage CA3059 only	Fig. 8	V_1	—	1.4	1.6	Vdc
External Trigger Voltage CA3059 only	—	V_6–V_4	—	1.4	—	Vdc

NOTES: 1. Care must be taken, especially when using an external power supply, that total package dissipation is not exceeded.
2. The values given in the Electrical Characteristics Chart at 120 V also apply for operation at input voltages of 24 V, 208/230 V, and 277 V, except for Pulse Duration test. However, the series resistor (R_S) must have the indicated value, shown in Table A for the specified input voltage.
3. I_4 out of Pin 4, 2.0 V on Pin 1, S1 position 2.

4

TEST CIRCUITS

(All resistor values are in ohms)

FIGURE 2 – DC SUPPLY VOLTAGE

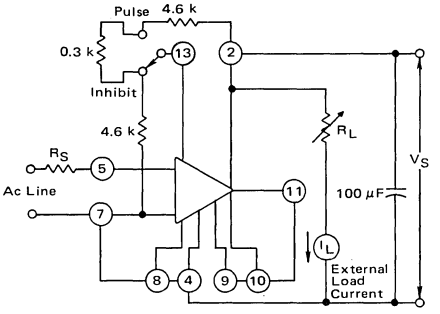


FIGURE 3 – PEAK OUTPUT (PULSED) AND GATE TRIGGER CURRENT WITH INTERNAL POWER SUPPLY

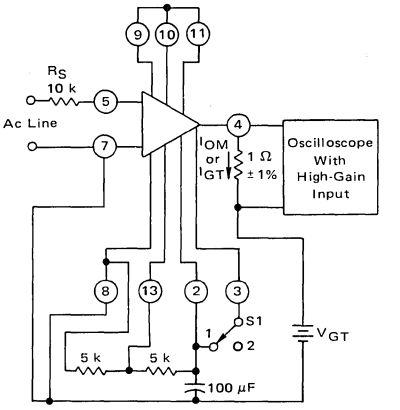


FIGURE 4 – PEAK OUTPUT CURRENT (PULSED) WITH EXTERNAL POWER SUPPLY

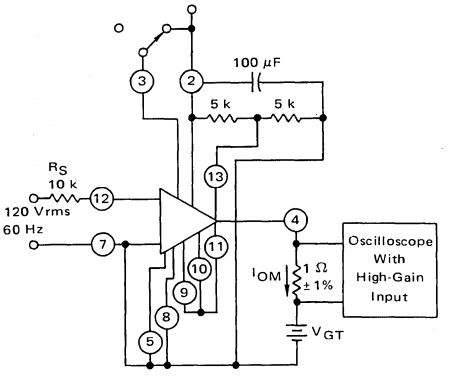


FIGURE 5 – INPUT INHIBIT RATIO

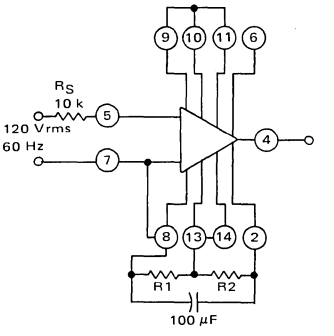


FIGURE 6 – GATE PULSE DURATION TEST CIRCUIT WITH ASSOCIATED WAVEFORM

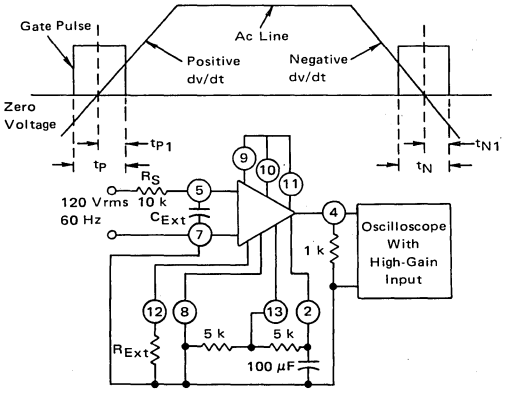
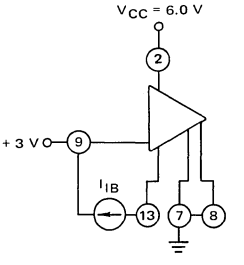


FIGURE 7 – INPUT BIAS CURRENT TEST CIRCUIT



TYPICAL CHARACTERISTICS

FIGURE 8 – INHIBIT INPUT VOLTAGE TEST

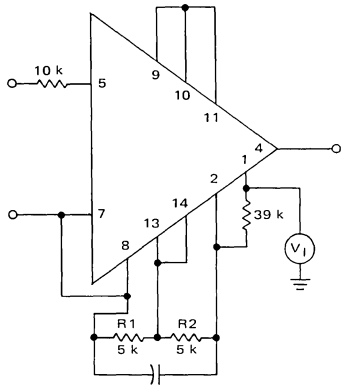


FIGURE 9 – PEAK OUTPUT CURRENT (PULSED) versus EXTERNAL POWER SUPPLY VOLTAGE

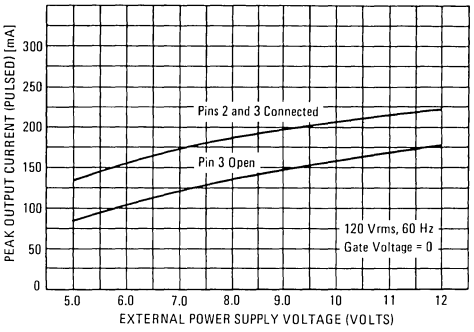


FIGURE 10 – PEAK OUTPUT CURRENT (PULSED) versus AMBIENT TEMPERATURE

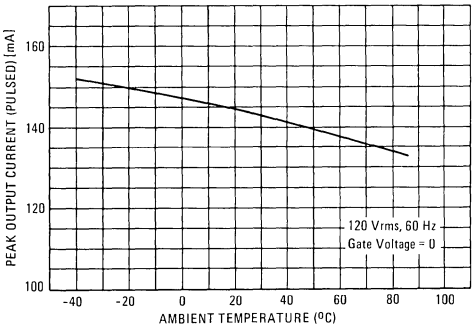


FIGURE 11 – TOTAL PULSE WIDTH versus AMBIENT TEMPERATURE

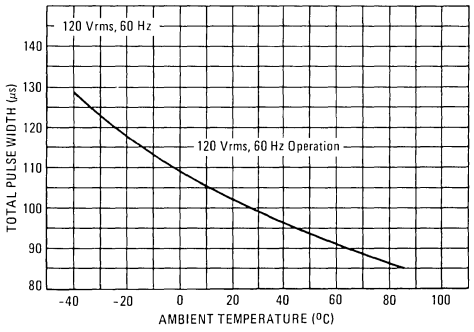


FIGURE 12 – INTERNAL SUPPLY versus AMBIENT TEMPERATURE

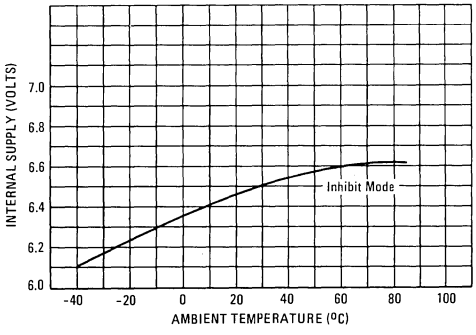


FIGURE 13 – INHIBIT VOLTAGE RATIO versus AMBIENT TEMPERATURE

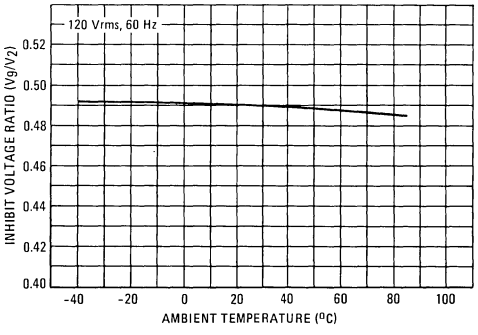
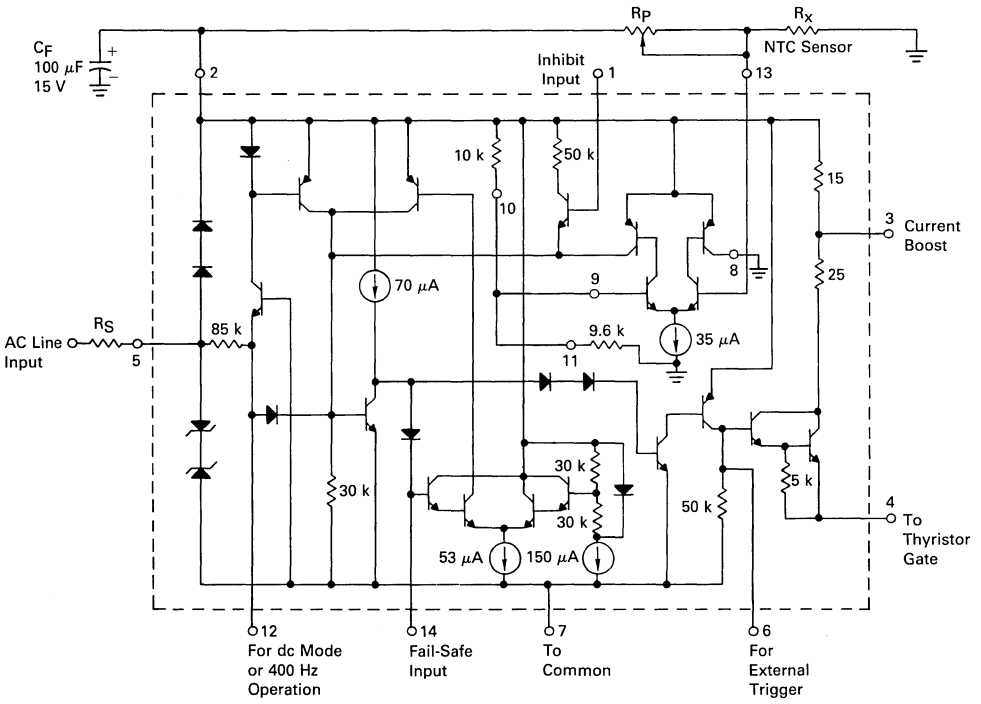


FIGURE 14 – CIRCUIT SCHEMATIC



NOTE: Current sources are established by an internal reference.
Pins 1, 6, 12, and 14 are not used with CA3079.

APPLICATION INFORMATION

Power Supply

The CA3059 and CA3079 are self-powered circuits, powered from the ac line through an appropriate dropping resistor (see Table A). The internal supply is designed to power the auxiliary power circuits.

In applications where more output current from the internal supply is required, an external power supply of higher voltage should be used. To use an external power supply, connect pin 5 and pin 7 together and apply the synchronizing voltage to pin 12 and the dc supply voltage to pin 2 as shown in Figure 4.

Operation of Protection Circuit (CA3059 Only)

The protection circuit, when connected, will remove current drive from the triac if an open or shorted sensor is detected. This circuit is activated by connecting pin 13 to pin 14 (see Figure 1).

The following conditions should be observed when the protection circuit is utilized:

A. The internal supply should be used and the external load current must be limited to 2 mA with a 5 kΩ dropping resistor.

B. Sensor Resistance (R_X) and R_P values should be between 2 kΩ and 100 kΩ.

C. The relationship $0.33 < R_X/R_P < 3$ must be met over the anticipated temperature range to prevent undesired activation of the circuit. A shunt or series resistor may have to be added.

External Inhibit Function (CA3059 Only)

A priority inihibit command applied to pin 1 will remove current drive from the thyristor. A command of at least +1.2 V @ 10 μA is required. A DTL or T^2L logic 1 applied to pin 1 will activate the inhibit function.

DC Gate Current Mode (CA3059 Only)

When comparator operation is desired or inductive loads are being switched, pins 7 and 12 should be connected. This connection disables the zero-crossing detector to permit the flow of gate current from the differential sensing amplifier on demand. Care should be exercised to avoid possible overloading of the internal power supply when operating the device in this mode. A resistor should be inserted between pin 4 and the thyristor gate in order to limit the current.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3479

STEPPER MOTOR DRIVER

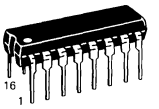
SILICON MONOLITHIC
INTEGRATED CIRCUIT

4

STEPPER MOTOR DRIVER

The MC3479 is designed to drive a two-phase stepper motor in the bipolar mode. The circuit consists of four input sections, a logic decoding/sequencing section, two driver-stages for the motor coils, and an output to indicate the $\overline{\text{Phase A}}$ drive state.

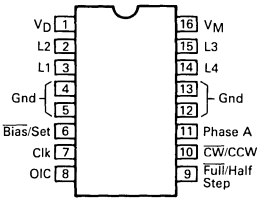
- Single Supply Operation — +7.2 to +16.5 Volts
- 350 mA/Coil Drive Capability
- Clamp Diodes Provided for Back-EMF Suppression
- Selectable $\overline{\text{CW}}$/CCW and $\overline{\text{Full}}$/Half Step Operation
- Selectable High/Low Output Impedance (Half Step Mode)
- TTL/CMOS Compatible Inputs
- Input Hysteresis — 400 mV Minimum
- Phase Logic Can Be Initialized to $\overline{\text{Phase A}}$
- $\overline{\text{Phase A}}$ Output Drive State Indication (Open-Collector)
- Available in Standard DIP and Surface Mount



P SUFFIX
PLASTIC PACKAGE
CASE 648C

FN SUFFIX
PLASTIC PACKAGE
CASE 775
(PLCC 20)

PIN ASSIGNMENTS



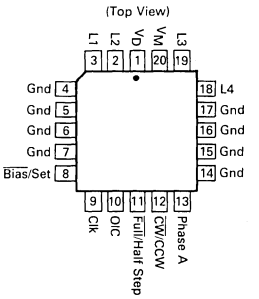
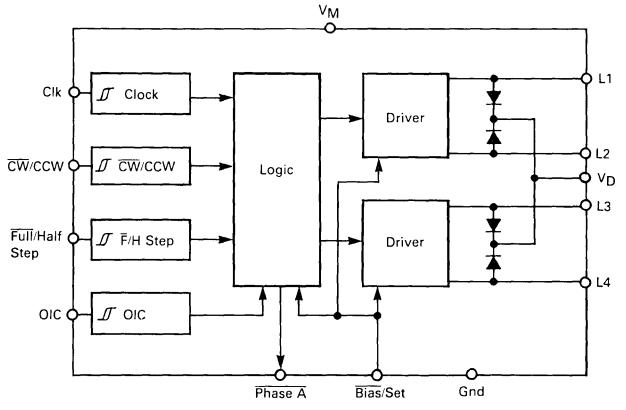


FIGURE 1 — BLOCK DIAGRAM



INPUT TRUTH TABLE

	Input Low	Input High
$\overline{\text{CW}}$/CCW	CW	CCW
$\overline{\text{Full}}$/Half Step	Full Step	Half Step
OIC	Hi Z	Low Z
Clk	Positive Edge Triggered	

ORDERING INFORMATION

Device	Operating Junction Temperature Range	Package
MC3479P	−65° to +150°C	Plastic
MC3479FN		Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_M	+18	Vdc
Clamp Diode Cathode Voltage (Pin 1)	V_D	V_M + 5.0	Vdc
Driver Output Voltage	V_{OD}	V_M + 6.0	Vdc
Drive Output Current/Coil	I_{OD}	±500	mA
Input Voltage (Logic Controls)	V_{in}	−0.5 to +7.0	Vdc
$\overline{\text{Bias}}$/Set Current	I_{BS}	−10	mA
$\overline{\text{Phase A}}$ Output Voltage	V_{OA}	+18	Vdc
$\overline{\text{Phase A}}$ Sink Current	I_{OA}	20	mA
Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_M	+7.2	+16.5	Vdc
Clamp Diode Cathode Voltage	V_D	V_M	V_M+4.5	Vdc
Driver Output Current (Per Coil) (Note 5)	I_{OD}	—	350	mA
Input Voltage (Logic Controls)	V_{in}	0	+5.5	Vdc
$\overline{\text{Bias}}$/Set Current (Outputs Active)	I_{BS}	−300	−75	μA
$\overline{\text{Phase A}}$ Output Voltage	V_{OA}	—	V_M	Vdc
$\overline{\text{Phase A}}$ Sink Current	I_{OA}	0	8.0	mA
Operating Ambient Temperature	T_A	0	+70	°C

NOTE:
5. See section on Power Dissipation in Application Information.

DC ELECTRICAL CHARACTERISTICS *(Pin numbers refer to the DIP Package)

(Specifications apply over the recommended supply voltage and temperature ranges unless otherwise noted.) (See Notes 1, 2)

Characteristic	*Pins	Symbol	Min	Typ	Max	Unit
INPUT LOGIC LEVELS						
Threshold Voltage (Low-to-High)	7, 8, 9, 10	V_{TLH}	—	—	2.0	Vdc
Threshold Voltage (High-to-Low)		V_{THL}	0.8	—	—	Vdc
Hysteresis		V_{HYS}	0.4	—	—	Vdc
Current (V_I = 0.4 V)		I_{IL}	−100	—	—	μA
(V_I = 5.5 V)		I_{IH1}	—	—	+100	
(V_I = 2.7 V)		I_{IH2}	—	—	+20	
DRIVER OUTPUT LEVELS						
Output High Voltage (I_{BS} = −300 μA) (I_{OD} = −350 mA)	2, 3, 14, 15	V_{OHD}	V_M−2.0	—	—	Vdc
(I_{OD} = −0.1 mA)			V_M−1.2	—	—	
Output Low Voltage (I_{BS} = −300 μA, I_{OD} = 350 mA)		V_{OLD}	—	—	0.8	Vdc
Differential Mode Output Voltage Difference (Note 3) (I_{BS} = −300 μA, I_{OD} = 350 mA)		DV_{OD}	—	—	0.15	Vdc
Common Mode Output Voltage Difference (Note 4) (I_{BS} = −300 μA, I_{OD} = −0.1 mA)		CV_{OD}	—	—	0.15	Vdc
Output Leakage — Hi Z State						μA
(0 ≤ V_{OD} ≤ V_M, I_{BS} = −5.0 μA)		I_{OZ1}	−100	—	+100	
(0 ≤ V_{OD} ≤ V_M, I_{BS} = −300 μA, F/H = 2.0 V, OIC = 0.8 V)		I_{OZ2}	−100	—	+100	

NOTES:
1. Algebraic convention rather than absolute values is used to designate limit values.
2. Current into a pin is designated as positive. Current out of a pin is designated as negative.
3. $DV_{OD} = |V_{OD1,2} - V_{OD3,4}|$ where: $V_{OD1,2} = (V_{OHD1} - V_{OLD2})$ or $(V_{OHD2} - V_{OLD1})$, and $V_{OD3,4} = (V_{OHD3} - V_{OLD4})$ or $(V_{OHD4} - V_{OLD3})$.
4. $CV_{OD} = |V_{OHD1} - V_{OHD2}|$ or $|V_{OHD3} - V_{OHD4}|$.

DC ELECTRICAL CHARACTERISTICS (continued) *(Pin numbers refer to the DIP Package)
(Specifications apply over the recommended supply voltage and temperature ranges unless otherwise noted.) (See Notes 1, 2)

Characteristic	*Pins	Symbol	Min	Typ	Max	Unit
CLAMP DIODES						
Forward Voltage (I_D = 350 mA)	1, 2, 3, 14, 15	V_{DF}	—	2.5	3.0	Vdc
Leakage Current (Per Diode) (Pin 1 = 21 V; Outputs = 0 V; I_{BS} = 0 μA)		I_{DR}	—	—	100	μA
$\overline{\text{PHASE A}}$ OUTPUT						
Output Low Voltage (I_{OA} = 8.0 mA)	11	V_{OLA}	—	—	0.4	Vdc
Off State Leakage Current (V_{OHA} = 16.5 V)		I_{OHA}	—	—	100	μA
POWER SUPPLY						
Power Supply Current (I_{OD} = 0 μA, I_{BS} = −300 μA)	16					mA
(L1 = V_{OHD}, L2 = V_{OLD}, L3 = V_{OHD}, L4 = V_{OLD})		I_{MW}	—	—	70	
(L1 = V_{OHD}, L2 = V_{OLD}, L3 = Hi Z, L4 = Hi Z)		I_{MZ}	—	—	40	
(L1 = V_{OHD}, L2 = V_{OLD}, L3 = V_{OHD}, L4 = V_{OHD})		I_{MN}	—	—	75	
$\overline{\text{BIAS}}$/SET CURRENT						
To Set $\overline{\text{Phase A}}$	6	I_{BS}	−5.0	—	—	μA

PACKAGE THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction to Ambient — No Heatsink	$R_{\theta JA}$	—	45	—	°C/W

AC SWITCHING CHARACTERISTICS (T_A = +25°C, V_M = 12 V) (See Figures 2, 3, 4)

Characteristic	*Pins	Symbol	Min	Typ	Max	Unit
Clock Frequency	7	f_{CK}	0	—	50	kHz
Clock Pulse Width — High	7	PW_{CKH}	10	—	—	μs
Clock Pulse Width — Low	7	PW_{CKL}	10	—	—	μs
$\overline{\text{Bias}}$/Set Pulse Width	6	PW_{BS}	10	—	—	μs
Setup Time — $\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS	10–7 9–7	t_{su}	5.0	—	—	μs
Hold Time — $\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS	10–7 9–7	t_h	10	—	—	μs
Propagation Delay — Clk-to-Driver Output		t_{PCD}	—	8.0	—	μs
Propagation Delay — $\overline{\text{Bias}}$/Set-to-Driver Output		t_{PBSD}	—	1.0	—	μs
Propagation Delay — Clk-to-$\overline{\text{Phase A}}$ Low	7–11	t_{PHLA}	—	12	—	μs
Propagation Delay — Clk-to-$\overline{\text{Phase A}}$ High	7–11	t_{PLHA}	—	5.0	—	μs

NOTES:
1. Algebraic convention rather than absolute values is used to designate limit values.
2. Current into a pin is designated as positive. Current out of a pin is designated as negative.

FIGURE 2 — AC TEST CIRCUIT

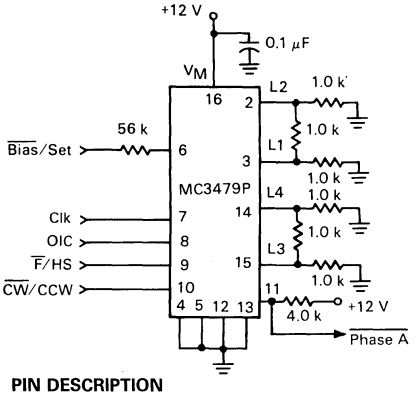
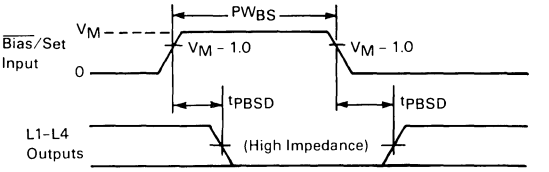


FIGURE 3 — BIAS/SET TIMING (Refer to Figure 2)



Note: t_r, t_f (10%-90%) for input signals are ⩽ 25 ns.

PIN DESCRIPTION

Name	Symbol	Pin # FN	Pin # DIP	Description
Power Supply	V_M	20	16	Power supply pin for both the logic circuit and the motor coil current. Voltage range is +7.2 to +16.5 volts.
Ground	Gnd	4, 5, 6, 7, 14, 15, 16, 17	4, 5, 12, 13	Ground pins for the logic circuit and the motor coil current. The physical configuration of the pins aids in dissipating heat from within the IC package.
Clamp Diode Voltage	V_D	1	1	This pin is used to protect the outputs where large voltage spikes may occur as the motor coils are switched. Typically a diode is connected between this pin and Pin 16. See Figure 11.
Driver Outputs	L1, L2 L3, L4	2, 3, 18, 19	2, 3, 14, 15	High current outputs for the motor coils. L1 and L2 are connected to one coil, and L3 and L4 to the other coil.
$\overline{\text{Bias}}$/Set	$\overline{B}$/S	8	6	This pin is typically 0.7 volts below V_M. The current out of this pin (through a resistor to ground) determines the maximum output sink current. If the pin is opened (I_{BS} < 5.0 μA) the outputs assume a high impedance condition, while the internal logic presets to a $\overline{\text{Phase A}}$ condition.
Clock	Clk	9	7	The positive edge of the clock input switches the outputs to the next position. This input has no effect if Pin 6 is open.
$\overline{\text{Full}}$/Half Step	$\overline{F}$/HS	11	9	When low (Logic "0"), each clock pulse will cause the motor to rotate one full step. When high, each clock pulse will cause the motor to rotate one-half step. See Figure 7 for sequence.
$\overline{\text{Clockwise}}$/ Counterclockwise	$\overline{CW}$/CCW	12	10	This input allows reversing the rotation of the motor. See Figure 7 for sequence.
Output Impedance Control	OIC	10	8	This input is relevant only in the half step mode (Pin 9 > 2.0 V). When low (Logic "0") the two driver outputs of the non-energized coil will be in a high impedance condition. When high the same driver outputs will be at a low impedance referenced to V_M. See Figure 7.
$\overline{\text{Phase A}}$	$\overline{\text{Ph A}}$	13	11	This open-collector output indicates (when low) that the driver outputs are in the $\overline{\text{Phase A}}$ condition (L1 = L3 = V_{OHD}, L2 = L4 = V_{OLD}).

APPLICATION INFORMATION

GENERAL

The MC3479 integrated circuit is designed to drive a stepper positioning motor in applications such as disk drives and robotics. The outputs can provide up to 350 mA to each of two coils of a two-phase motor. The outputs change state with each low-to-high transition of the clock input, with the new output state depending on the previous state, as well as the input conditions at the logic controls.

OUTPUTS

The outputs (L1–L4) are high current outputs (see Figure 5), which when connected to a two-phase motor, provide two full-bridge configurations (L3 and L4 are not shown in Figure 5). The polarities applied to the motor coils depend on which transistor (Q_H or Q_L) of each output is on, which in turn depends on the inputs and the decoding circuitry.

FIGURE 4 — CLOCK TIMING (Refer to Figure 2)

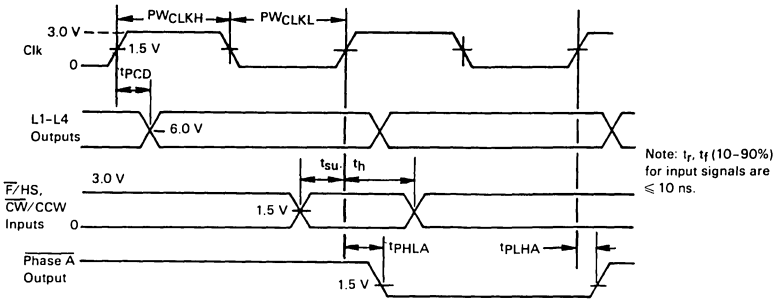
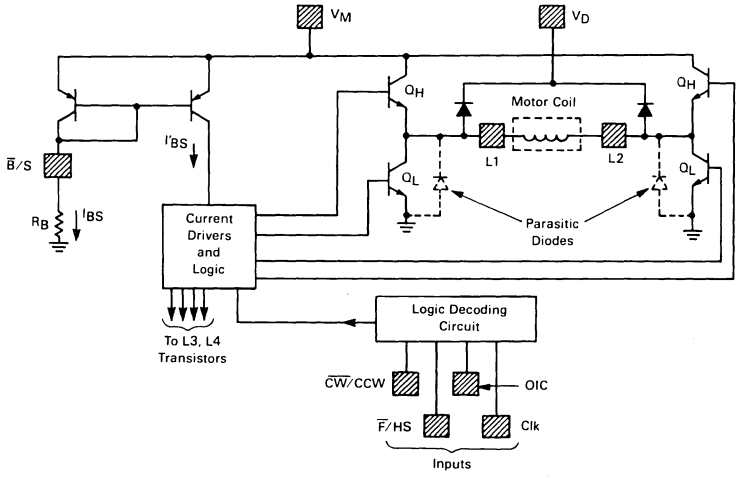


FIGURE 5 — OUTPUT STAGES

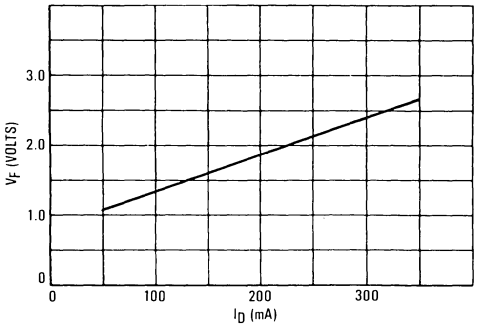


The maximum sink current available at the outputs is a function of the resistor connected between Pin 6 and ground (see section on Bias/Set operation). Whenever the outputs are to be in a high impedance state, both transistors (Q_H and Q_L of Figure 5) of each output are off.

V_D

This pin allows for provision of a current path for the motor coil current during switching, in order to suppress back-EMF voltage spikes. V_D is normally connected to V_M (Pin 16) through a diode (zener or regular), a resistor, or directly. The peaks instantaneous voltage at the outputs must not exceed V_M by more than 6.0 volts. The voltage drop across the internal clamping diodes must be included in this portion of the design (see Figure 6). Note the parasitic diodes (Figure 5) across each Q_L of each output provide for a complete circuit path for the switched current.

FIGURE 6 — CLAMP DIODE CHARACTERISTICS



FULL/HALF STEP

When this input is at a Logic "0" (<0.8 volts), the outputs change a full step with each clock cycle, with the sequence direction depending on the CW/CCW input. There are four steps (Phase A, B, C, D) for each complete cycle of the sequencing logic. Current flows through both motor coils during each step, as shown in Figure 7.

When taken to a Logic "1" (>2.0 volts), the outputs change a half step with each clock cycle, with the sequence direction depending on the CW/CCW input. Eight steps (Phase A–H) result for each complete cycle of the sequencing logic. Phase A, C, E and G correspond (in polarity) to Phase A, B, C, and D, respectively, of the full step sequence. Phase B, D, F and H provide current to one motor coil, while de-energizing the other coil. The condition of the outputs of the de-energized coil depends on the OIC input. See Figure 7 for timing diagram.

OIC

The output impedance control input determines the output impedance to the de-energized coil when operating in the half-step mode. When the outputs are in Phase B, D, F or H (Figure 7) and this input is at a Logic "0" (<0.8 V), the two outputs to the de-energized coil are in a high impedance condition — Q_L and Q_H of both outputs (Figure 5) are off. When this input is at a Logic "1" (>2.0 V), a low impedance output is provided to the de-energized coil as both outputs have Q_H on (Q_L off). To complete the low impedance path requires connecting V_D to V_M as described elsewhere in this data sheet.

BIAS/SET

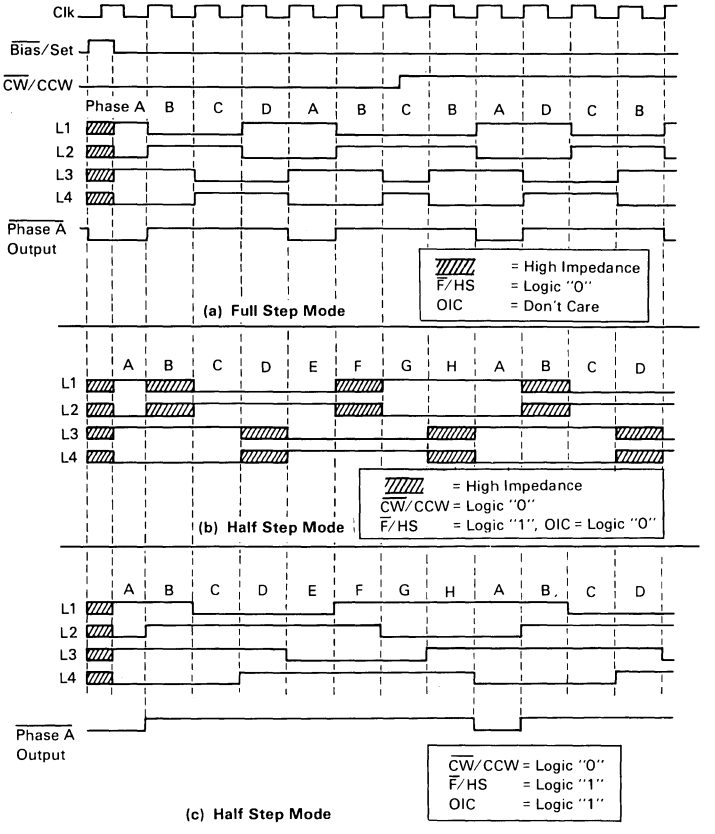
This pin can be used for three functions: a) determining the maximum output sink current; b) setting the internal logic to a known state; and c) reducing power consumption.

a) The maximum output sink current is determined by the base drive current supplied to the lower transistors (Q_Ls of Figure 5) of each output, which in turn, is a function of I_{BS}. The appropriate value of I_{BS} is determined by:

$$I_{BS} = I_{OD} \times 0.86$$

where I_{BS} is in microamps, and I_{OD} is the motor current/coil in milliamps.

FIGURE 7 — OUTPUT SEQUENCE



The value of R_B (between this pin and ground) is then determined by:

$$R_B = \frac{V_M - 0.7\ V}{I_{BS}}$$

b) When this pin is opened (raised to V_M) such that I_{BS} is <5.0 μA, the internal logic is set to the Phase $\overline{A}$ condition, and the four driver outputs are put into a high impedance state. The Phase $\overline{A}$ output (Pin 11) goes active (low), and input signals at the controls are ignored during this time. Upon re-establishing I_{BS}, the driver outputs become active, and will be in the Phase $\overline{A}$ position (L1 = L3 = V_{OHD}, L2 = L4 = V_{OLD}). The circuit will then respond to the inputs at the controls.

The Set function (opening this pin) can be used as a power-up reset while supply voltages are settling. A CMOS logic gate (powered by V_M) can be used to control this pin as shown in Figure 11.

c) Whenever the motor is not being stepped, power dissipation in the IC and in the motor may be lowered by reducing I_{BS}, so as to reduce the output (motor) current. Setting I_{BS} to 75 μA will reduce the motor current, but will not reset the internal logic as described above. See Figure 12 for a suggested circuit.

POWER DISSIPATION

The power dissipated by the MC3479 must be such that the junction temperature (T_J) does not exceed 150°C. The power dissipated can be expressed as:

$$P = (V_M \times I_M) + (2 \times I_{OD})\ [(V_M - V_{OHD}) + V_{OLD}]$$

where V_M = Supply voltage;
I_M = Supply current other than I_{OD};
I_{OD} = Output current to each motor coil;
V_{OHD} = Driver output high voltage;
V_{OLD} = Driver output low voltage.

The power supply current (I_M) is obtained from Figure 8. After the power dissipation is calculated, the junction temperature can be calculated using:

$$T_J = (P \times R_{\theta JA}) + T_A$$

where $R_{\theta JA}$ = Junction to ambient thermal resistance; (52°C/W for the DIP, 72°C/W for the FN Package)
T_A = Ambient Temperature.

For example, assume an application where V_M = 12 V, the motor requires 200 mA/coil, operating at room temperature with no heatsink on the IC. I_{BS} is calculated:

$I_{BS} = 200 \times 0.86$
$I_{BS} = 172\ \mu A$

R_B is calculated:

$R_B = (12 - 0.7)\ V/172\ \mu A$
$R_B = 65.7\ k\Omega$

From Figure 8, I_M (max) is determined to be 40 mA. From Figure 9, V_{OLD} is 0.46 volts, and from Figure 10, ($V_M - V_{OHD}$) is 1.4 volts.

$P = (12 \times 0.040) + (2 \times 0.2)\ (1.4 + 0.46)$
$P = 1.22\ W$

$T_J = (1.22\ W \times 52°C/W) + 25°C$
$T_J = 88°C$

This temperature is well below the maximum limit. If the calculated T_J had been higher than 150°C, a heatsink such as the Staver Co. V-7 Series, Aavid #5802, or Thermalloy #6012 could be used to reduce $R_{\theta JA}$. In extreme cases forced air cooling should be considered.

The above calculation, and $R_{\theta JA}$, assumes that a ground plane is provided under the MC3479 (either or both sides of the PC board) to aid in the heat dissipation. Single nominal width traces leading from the four ground pins should be avoided as this will increase T_J, as well as provide potentially disruptive ground noise and I_R drops when switching the motor current.

FIGURE 8 — POWER SUPPLY CURRENT

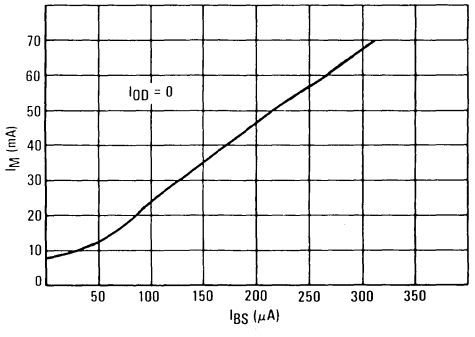


FIGURE 9 — MAXIMUM SATURATION VOLTAGE — DRIVER OUTPUT LOW

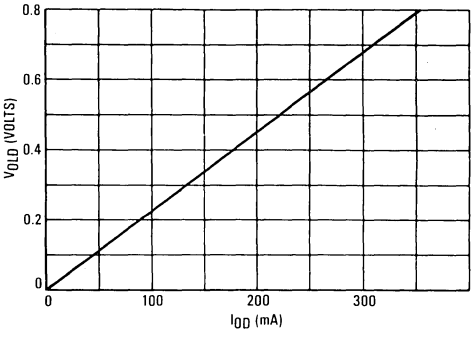


FIGURE 10 — MAXIMUM SATURATION VOLTAGE — DRIVER OUTPUT HIGH

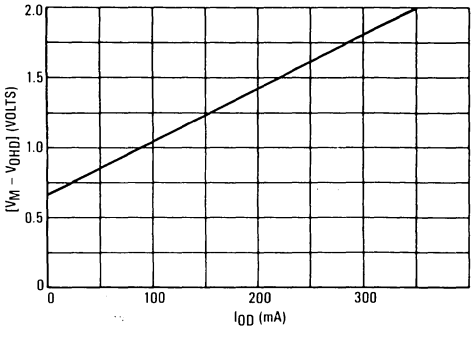


FIGURE 11 — TYPICAL APPLICATIONS CIRCUIT

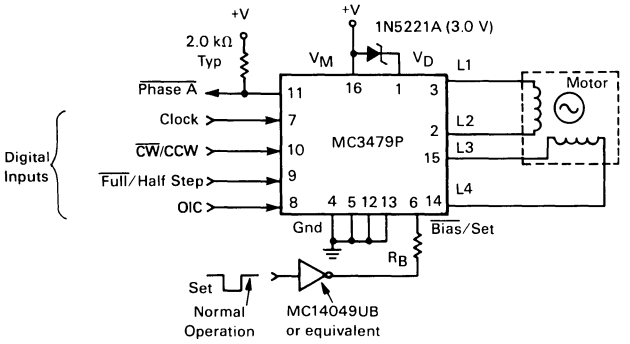
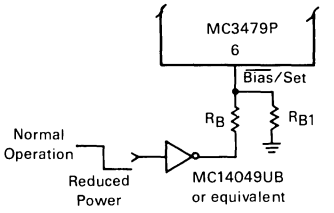


FIGURE 12 — POWER REDUCTION



— Suggested value for R_{B1} (V_M = 12 V) is 150 kΩ.
— R_B calculation (see text) must take into account the current through R_{B1}.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC33030

DC SERVO MOTOR CONTROLLER/DRIVER

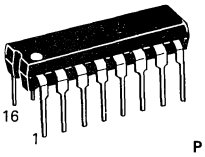
The MC33030 is a monolithic dc servo motor controller providing all active functions necessary for a complete closed loop system. This device consists of an on-chip op amp and window comparator with wide input common-mode range, drive and brake logic with direction memory, power H switch driver capable of 1.0 A, independently programmable over-current monitor and shutdown delay, and over-voltage monitor. This part is ideally suited for almost any servo positioning application that requires sensing of temperature, pressure, light, magnetic flux, or any other means that can be converted to a voltage.

Although this device is primarily intended for servo applications, it can be used as a switchmode motor controller.

- On-Chip Error Amp for Feedback Monitoring
- Window Detector with Deadband and Self Centering Reference Input
- Drive/Brake Logic with Direction Memory
- 1.0 A Power H Switch
- Programmable Over-Current Detector
- Programmable Over-Current Shutdown Delay
- Over-Voltage Shutdown

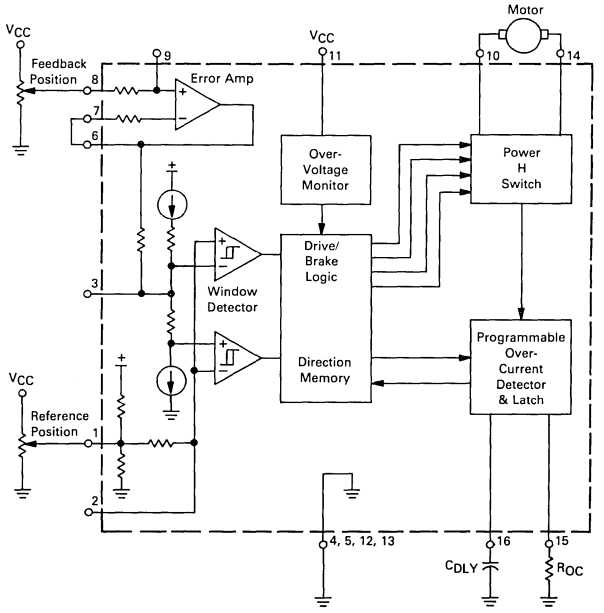
DC SERVO MOTOR CONTROLLER/DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

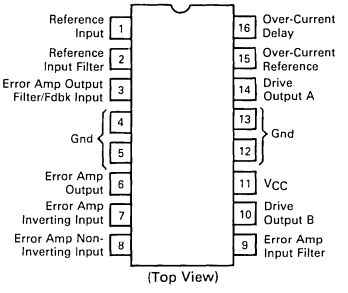


P SUFFIX
PLASTIC PACKAGE
CASE 648C

SIMPLIFIED BLOCK DIAGRAM



PIN CONNECTIONS



(Top View)

Pins 4, 5, 12 and 13 are electrical ground and heat sink pins for IC

ORDERING INFORMATION

Device	Temperature Range	Package
MC33030P	−40°C to +85°C	Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	36	V
Input Voltage Range Op Amp, Comparator, Current Limit. Pins 1, 2, 3, 6, 7, 8, 9, 15.	V_{IR}	−0.3 to V_{CC}	V
Input Differential Voltage Range Op Amp, Comparator. Pins 1, 2, 3, 6, 7, 8, 9.	V_{IDR}	−0.3 to V_{CC}	V
Delay Pin Sink Current (Pin 16)	$I_{DLY(sink)}$	20	mA
Output Source Current (Op Amp)	I_{source}	10	mA
Drive Output Voltage Range (Note 1)	V_{DRV}	−0.3 to (V_{CC} + V_F)	V
Drive Output Source Current (Note 2)	$I_{DRV(source)}$	1.0	A
Drive Output Sink Current (Note 2)	$I_{DRV(sink)}$	1.0	A
Brake Diode Forward Current (Note 2)	I_F	1.0	A
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air Thermal Resistance Junction to Case. Pins 4, 5, 12, 13.	 P_D $R_{\theta JA}$ $R_{\theta JC}$	 1000 80 15	 mW °C/W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES:
1. The upper voltage level is clamped by the forward drop, V_F, of the brake diode.
2. These values are for continuous dc current. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (V_{CC} = 14 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMP					
Input Offset Voltage (−40°C ≤ T_A ≤ +85°C) $V_{Pin\ 6}$ = 7.0 V, R_L = 100 k	V_{IO}	—	1.5	10	mV
Input Offset Current $V_{Pin\ 6}$ = 1.0 V, R_L = 100 k	I_{IO}	—	0.7	—	nA
Input Bias Current $V_{Pin\ 6}$ = 7.0 V, R_L = 100 k	I_{IB}	—	7.0	—	nA
Input Common-Mode Voltage Range ΔV_{IO} = 20 mV, R_L = 100 k	V_{ICR}	—	0 to (V_{CC} −1.2)	—	V
Slew Rate, Open Loop (V_{ID} = 0.5 V, C_L = 15 pF)	SR	—	0.40	—	V/μs
Unity-Gain Crossover Frequency	f_c	—	550	—	kHz
Unity-Gain Phase Margin	ϕ_m	—	63	—	deg.
Common-Mode Rejection Ratio $V_{Pin\ 6}$ = 7.0 V, R_L = 100 k	CMRR	50	82	—	dB
Power Supply Rejection Ratio V_{CC} = 9.0 to 16 V, $V_{Pin\ 6}$ = 7.0 V, R_L = 100 k	PSRR	—	89	—	dB
Output Source Current ($V_{Pin\ 6}$ = 12 V)	I_{O+}	—	1.8	—	mA
Output Sink Current ($V_{Pin\ 6}$ = 1.0 V)	I_{O-}	—	250	—	μA
Output Voltage Swing (R_L = 17 k to Ground)	V_{OH} V_{OL}	12.5 —	13.1 0.02	— —	V V

(Continued)

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
WINDOW DETECTOR					
Input Hysteresis Voltage ($V_1 - V_4$, $V_2 - V_3$, Figure 17)	V_H	25	35	45	mV
Input Dead Zone Range ($V_2 - V_4$, Figure 17)	V_{IDZ}	166	210	254	mV
Input Offset Voltage ($\|[V_2 - V_{Pin\ 2}] - [V_{Pin\ 2} - V_4]\|$, Figure 17)	V_{IO}	—	25	—	mV
Input Functional Common-Mode Range (Note 3) Upper Threshold Lower Threshold	 V_{IH} V_{IL}	 — —	 (V_{CC} – 1.05) 0.24	 — —	V
Reference Input Self Centering Voltage Pins 1 and 2 Open	V_{RSC}	—	(1/2 V_{CC})	—	V
Window Detector Propagation Delay Comparator Input, Pin 3, to Drive Outputs V_{ID} = 0.5 V, $R_{L(DRV)}$ = 390 Ω	$t_{p(IN/DRV)}$	—	2.0	—	μs
OVER-CURRENT MONITOR					
Over-Current Reference Resistor Voltage (Pin 15)	R_{OC}	3.9	4.3	4.7	V
Delay Pin Source Current V_{DLY} = 0 V, R_{OC} = 27 k, I_{DRV} = 0 mA	$I_{DLY(source)}$	—	5.5	6.9	μA
Delay Pin Sink Current (R_{OC} = 27 k, I_{DRV} = 0 mA) V_{DLY} = 5.0 V V_{DLY} = 8.3 V V_{DLY} = 14 V	$I_{DLY(sink)}$	 — — —	 0.1 0.7 16.5	 — — —	mA
Delay Pin Voltage, Low State (I_{DLY} = 0 mA)	$V_{OL(DLY)}$	—	0.3	0.4	V
Over-Current Shutdown Threshold V_{CC} = 14 V V_{CC} = 8.0 V	$V_{th(OC)}$	 6.8 5.5	 7.5 6.0	 8.2 6.5	V
Over-Current Shutdown Propagation Delay Delay Capacitor Input, Pin 16, to Drive Outputs V_{ID} = 0.5 V	$t_{p(DLY/DRV)}$	—	1.8	—	μs
POWER H-SWITCH					
Drive-Output Saturation (–40°C ≤ T_A ≤ +85°C, Note 4) High State (I_{source} = 100 mA) Low State (I_{sink} = 100 mA)	 $V_{OH(DRV)}$ $V_{OL(DRV)}$	 (V_{CC} – 2) —	 (V_{CC} – 0.85) 0.12	 — 1.0	V
Drive-Output Voltage Switching Time (C_L = 15 pF) Rise Time Fall Time	 t_r t_f	 — —	 200 200	 — —	ns
Brake Diode Forward Voltage Drop (I_F = 200 mA, Note 4)	V_F	—	1.04	2.5	V
TOTAL DEVICE					
Standby Supply Current	I_{CC}	—	14	25	mA
Over-Voltage Shutdown Threshold (–40°C ≤ T_A ≤ +85°C)	$V_{th(OV)}$	16.5	18	20.5	V
Over-Voltage Shutdown Hysteresis (Device off to on)	$V_{H(OV)}$	0.3	0.6	1.0	V
Operating Voltage Lower Threshold (–40°C ≤ T_A ≤ +85°C)	V_{CC}	—	7.5	8.0	V

NOTES:

3. The upper or lower hysteresis will be lost when operating the Input, Pin 3, close to the respective rail. Refer to Figure 4.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

FIGURE 1 — ERROR AMP INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

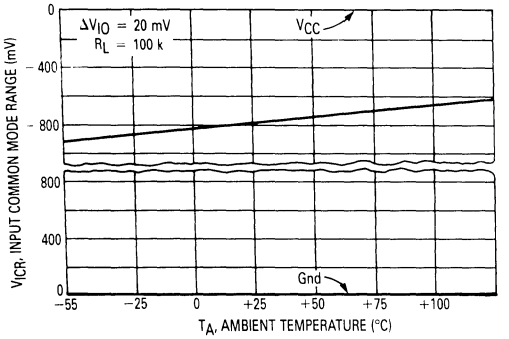


FIGURE 2 — ERROR AMP OUTPUT SATURATION versus LOAD CURRENT

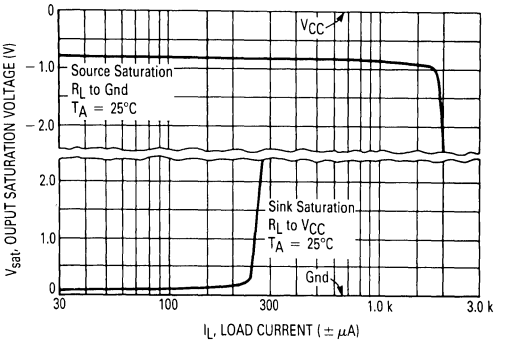


FIGURE 3 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

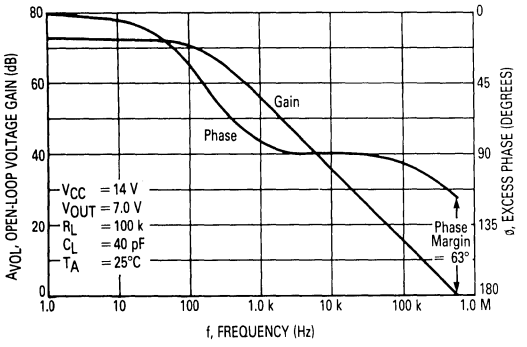


FIGURE 4 — WINDOW DETECTOR REFERENCE-INPUT COMMON-MODE VOLTAGE RANGE versus TEMPERATURE

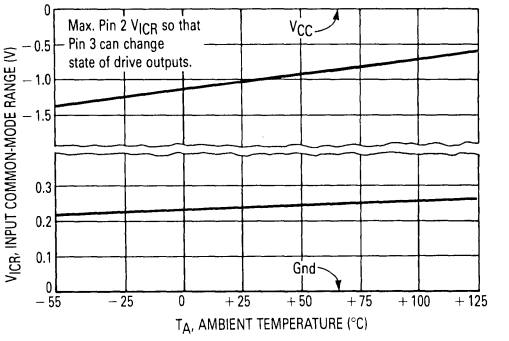


FIGURE 5 — WINDOW DETECTOR FEEDBACK-INPUT THRESHOLDS versus TEMPERATURE

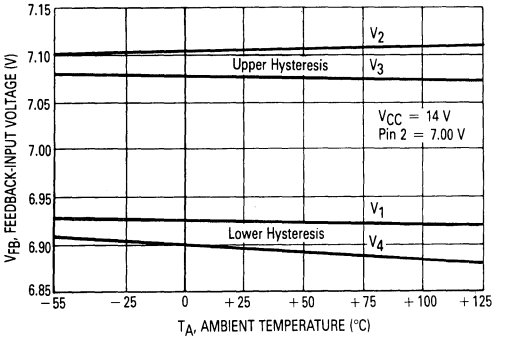


FIGURE 6 — OUTPUT DRIVE SATURATION versus LOAD CURRENT

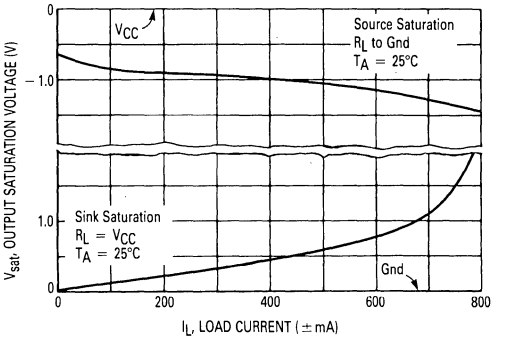


FIGURE 7 — BRAKE DIODE FORWARD CURRENT versus FORWARD VOLTAGE

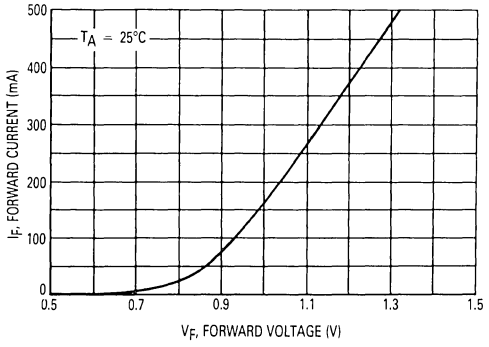


FIGURE 8 — OUTPUT SOURCE CURRENT-LIMIT versus OVER-CURRENT REFERENCE RESISTANCE

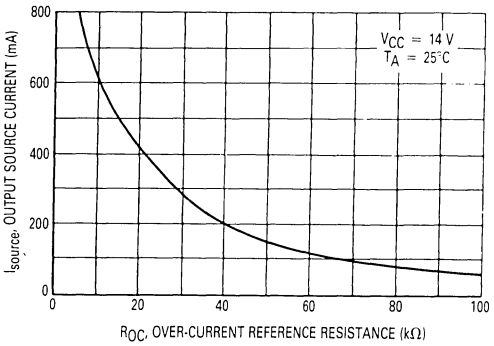


FIGURE 9 — OUTPUT SOURCE CURRENT-LIMIT versus TEMPERATURE

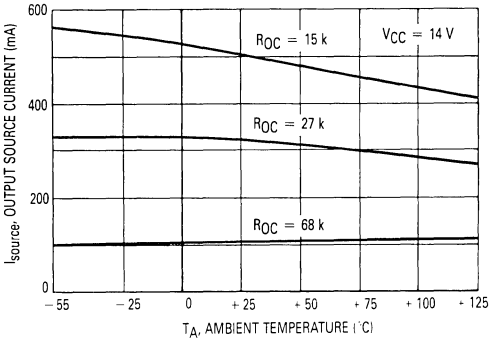


FIGURE 10 — NORMALIZED DELAY PIN SOURCE CURRENT versus TEMPERATURE

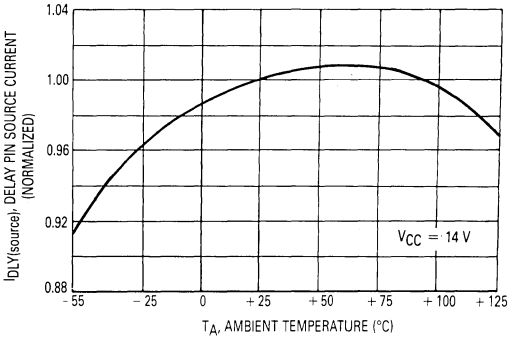


FIGURE 11 — NORMALIZED OVER-CURRENT DELAY THRESHOLD VOLTAGE versus TEMPERATURE

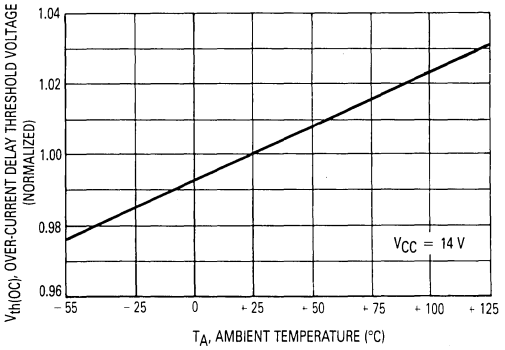


FIGURE 12 — SUPPLY CURRENT versus SUPPLY VOLTAGE

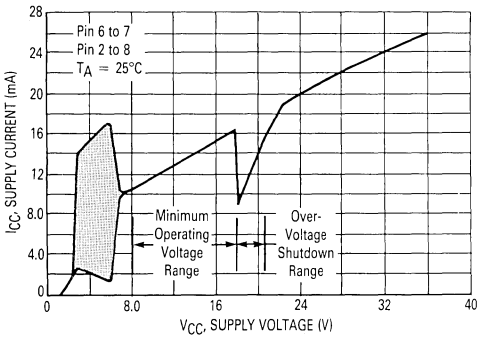


FIGURE 13 — NORMALIZED OVER-VOLTAGE SHUTDOWN THRESHOLD versus TEMPERATURE

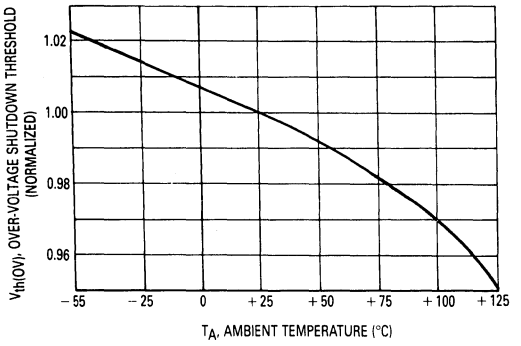


FIGURE 14 — NORMALIZED OVER-VOLTAGE SHUTDOWN HYSTERESIS versus TEMPERATURE

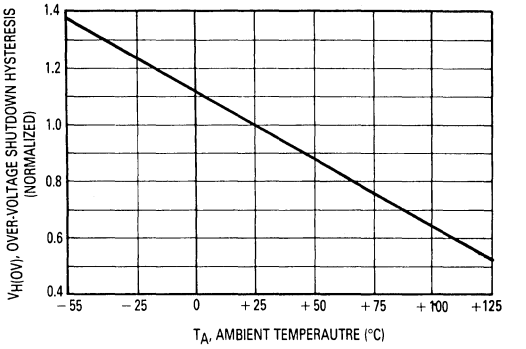
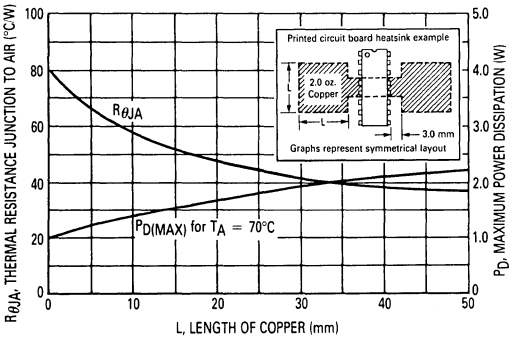


FIGURE 15 — THERMAL RESISTANCE AND MAXIMUM POWER DISSIPATION versus P.C.B. COPPER LENGTH



OPERATING DESCRIPTION

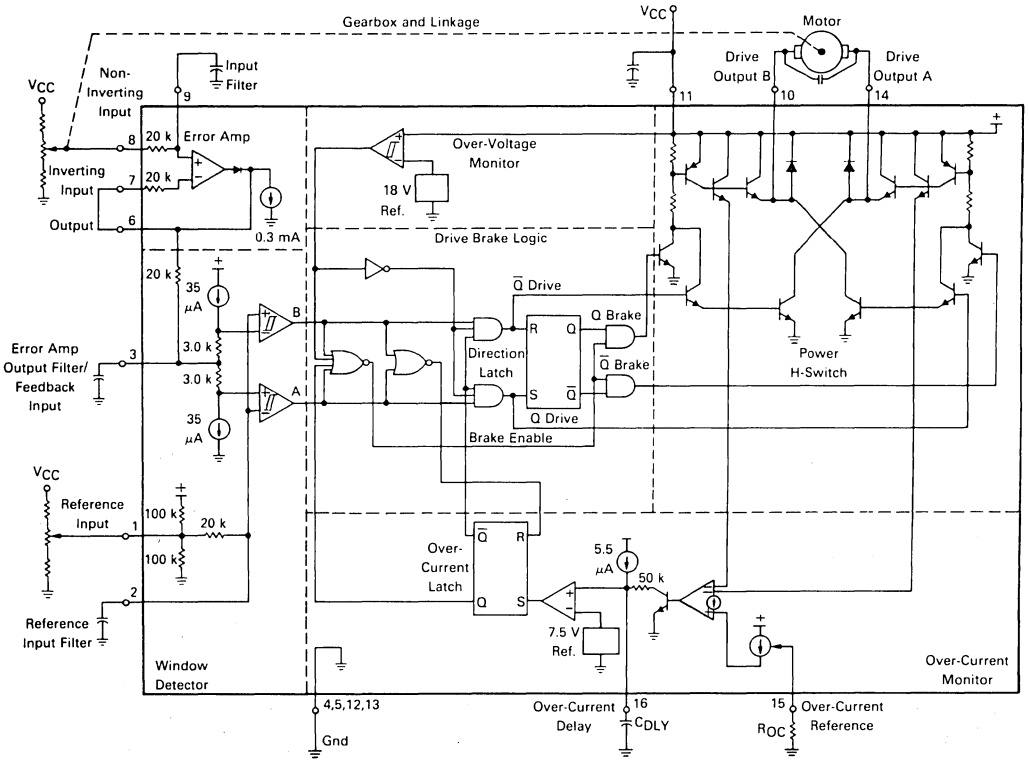
The MC33030 was designed to drive fractional horsepower dc motors and sense actuator position by voltage feedback. A typical servo application and representative internal block diagram are shown in Figure 16. The system operates by setting a voltage on the reference input of the Window Detector (Pin 1) which appears on (Pin 2). A dc motor then drives a position sensor, usually a potentiometer driven by a gear box, in a corrective fashion so that a voltage proportional to position is present at Pin 3. The servo motor will continue to run until the voltage at Pin 3 falls within the dead zone, which is centered about the reference voltage.

The Window Detector is composed of two comparators, A and B, each containing hysteresis. The reference input, common to both comparators, is pre-biased at 1/2 V_{CC} for simple two position servo systems and can easily be overriden by an external voltage divider. The feedback voltage present at Pin 3 is connected to the center of two resistors that are driven by an equal magnitude current source and sink. This generates an offset voltage at the input of each comparator which is centered about Pin 3 that can float virtually from V_{CC} to ground. The sum of the upper and lower offset voltages is defined as the window detector input dead zone range.

To increase system flexibility, an on-chip Error Amp is provided. It can be used to buffer and/or gain-up the actuator position voltage which has the effect of narrowing the dead zone range. A PNP differential input stage is provided so that the input common-mode voltage range will include ground. The main design goal of the error amp output stage was to be able to drive the window detector input. It typically can source 1.8 mA and sink 250 μA. Special design considerations must be made if it is to be used for other applications.

The Power H-Switch provides a direct means for motor drive and braking with a maximum source, sink, and brake current of 1.0 A continuous. Maximum package power dissipation limits must be observed. Refer to Figure 15 for thermal information. For greater drive current requirements, a method for buffering that maintains all the system features is shown in Figure 29.

FIGURE 16 — REPRESENTATIVE BLOCK DIAGRAM AND TYPICAL SERVO APPLICATION



The Over-Current Monitor is designed to distinguish between motor start-up or locked rotor conditions that can occur when the actuator has reached its travel limit. A fraction of the Power H-Switch source current is internally fed into one of the two inverting inputs of the current comparator, while the non-inverting input is driven by a programmable current reference. This reference level is controlled by the resistance value selected for R_{OC}, and must be greater than the required motor run-current with its mechanical load over temperature; refer to Figure 8. During an over-current condition, the comparator will turn off and allow the current source to charge the delay capacitor, C_{DLY}. When C_{DLY} charges to a level of 7.5 V, the set input of the over-current latch will go high, disabling the drive and brake functions of the Power H-Switch. The programmable time delay is determined by the capacitance value-selected for C_{DLY}.

$$t_{DLY} = \frac{V_{ref}\, C_{DLY}}{I_{DLY(source)}} = \frac{7.5\, C_{DLY}}{5.5\ \mu A} = 1.36\, C_{DLY} \text{ in } \mu F$$

This system allows the Power H-Switch to supply motor start-up current for a predetermined amount of time. If the rotor is locked, the system will time-out and shutdown. This feature eliminates the need for servo end-of-travel or limit switches. Care must be taken so as not to select too large of a capacitance value for C_{DLY}. An over-current condition for an excessively long time-out period can cause the integrated circuit to overheat and eventually fail. Again, the maximum package power dissipation limits must be observed. The over-current latch is reset upon power-up or by readjusting $V_{pin\ 2}$ as to cause $V_{pin\ 3}$ to enter or pass through the dead zone. This can be achieved by requesting the motor to reverse direction.

An Over-Voltage Monitor circuit provides protection for the integrated circuit and motor by disabling the Power H-Switch functions if V_{CC} should exceed 18 V. Resumption of normal operation will commence when V_{CC} falls below 17.4 V.

A timing diagram that depicts the operation of the Drive/Brake Logic section is shown in Figure 17. The waveforms grouped in [1] show a reference voltage that was preset, appearing on Pin 2, which corresponds to the desired actuator position. The true actuator position is represented by the voltage on Pin 3. The points V_1 through V_4 represent the input voltage thresholds of comparators A and B that cause a change in their respective output state. They are defined as follows:

V_1 = Comparator B turn-off threshold
V_2 = Comparator A turn-on threshold
V_3 = Comparator A turn-off threshold
V_4 = Comparator B turn-on threshold

V_1–V_4 = Comparator B input hysteresis voltage
V_2–V_3 = Comparator A input hysteresis voltage
V_2–V_4 = Window detector input dead zone range
$|(V_2 - V_{pin2}) - (V_{pin2} - V_4)|$ = Window detector input offset voltage

It must be remembered that points V_1 through V_4 always try to follow and center about the reference voltage setting if it is within the input common-mode voltage range of Pin 3; Figures 4 and 5. Initially consider that the feedback input voltage level is somewhere on the dashed line between V_2 and V_4 in [1]. This is within the dead zone range as defined above and the motor will be off. Now if the reference voltage is raised so that $V_{pin\ 3}$ is less than V_4, comparator B will turn-on [3] enabling $\overline{Q}$ Drive, causing Drive Output A to sink and B to source motor current [8]. The actuator will move in Direction B until $V_{pin\ 3}$ becomes greater than V_1. Comparator B will turn-off, activating the brake enable [4] and $\overline{Q}$ Brake [6] causing Drive Output A to go high and B to go into a high impedance state. The inertia of the mechanical system will drive the motor as a generator creating a positive voltage on Pin 10 with respect to Pin 14. The servo system can be stopped quickly, so as not to over-shoot through the dead zone range, by braking. This is accomplished by shorting the motor/generator terminals together. Brake current will flow into the diode at Drive Output B, through the internal V_{CC} rail, and out the emitter of the sourcing transistor at Drive Output A. The end of the solid line and beginning of the dashed for $V_{pin\ 3}$ [1] indicates the possible resting position of the actuator after braking.

If $V_{pin\ 3}$ should continue to rise and become greater than V_2, the actuator will have over shot the dead zone range and cause the motor to run in Direction A until $V_{pin\ 3}$ is equal to V_3. The Drive/Brake behavior for Direction A is identical to that of B. Overshooting the dead zone range in both directions can cause the servo system to continuously hunt or oscillate. Notice that the last motor run-direction is stored in the direction latch. This information is needed to determine whether Q or $\overline{Q}$ Brake is to be enabled when $V_{pin\ 3}$ enters the dead zone range. The dashed lines in [8,9] indicate the resulting waveforms of an over-current condition that has exceeded the programmed time delay. Notice that both Drive Outputs go into a high impedance state until $V_{pin\ 2}$ is readjusted so that $V_{pin\ 3}$ enters or crosses through the dead zone [7,4].

The inputs of the Error Amp and Window Detector can be susceptible to the noise created by the brushes of the dc motor and cause the servo to hunt. Therefore, each of these inputs are provided with an internal series resistor and are pinned out for an external bypass capacitor. It has been found that placing a capacitor with *short leads* directly across the brushes will significantly reduce noise problems. Good quality RF bypass capacitors in the range of 0.001 to 0.1 μF may be required. Many of the more economical motors will generate significant levels of RF energy over a spectrum that extends from dc to beyond 200 MHz. The capacitance value and method of noise filtering must be determined on a system by system basis.

Thus far, the operating description has been limited to servo systems in which the motor mechanically drives a potentiometer for position sensing. Figures 18, 19, 26, and 30 show examples that use light, magnetic flux, temperature, and pressure as a means to drive the feedback element. Figures 20, 21 and 22 are examples of two position, open-loop servo systems. In these systems, the motor runs the actuator to each end of its travel limit where the Over-Current Monitor detects a locked rotor condition and shuts down the drive. Figures 31 and 32 show two possible methods of using the MC33030 as a switching motor controller. In each example a fixed reference voltage is applied to Pin 2. This causes $V_{pin\ 3}$ to be less than V_4 and Drive Output A, Pin 14, to be in a low state saturating the TIP42 transistor. In Figure 31, the motor drives a tachometer that generates an ac voltage proportional to RPM. This voltage is rectified, filtered, divided down by the speed set potentiometer, and applied to Pin 8. The motor will accelerate until $V_{pin\ 3}$ is equal to V_1 at which time Pin 14 will go to a high state and terminate the motor drive. The motor will now coast until $V_{pin\ 3}$ is less than V_4 where upon drive is then reapplied. The system operation of Figure 32 identical to that of 31 except the signal at Pin 3 is an amplified average of the motors drive and back EMF voltages. Both systems exhibit excellent control of RPM with variations of V_{CC}; however, Figure 31 has somewhat better torque characteristics at low RPM.

FIGURE 17 — TIMING DIAGRAM

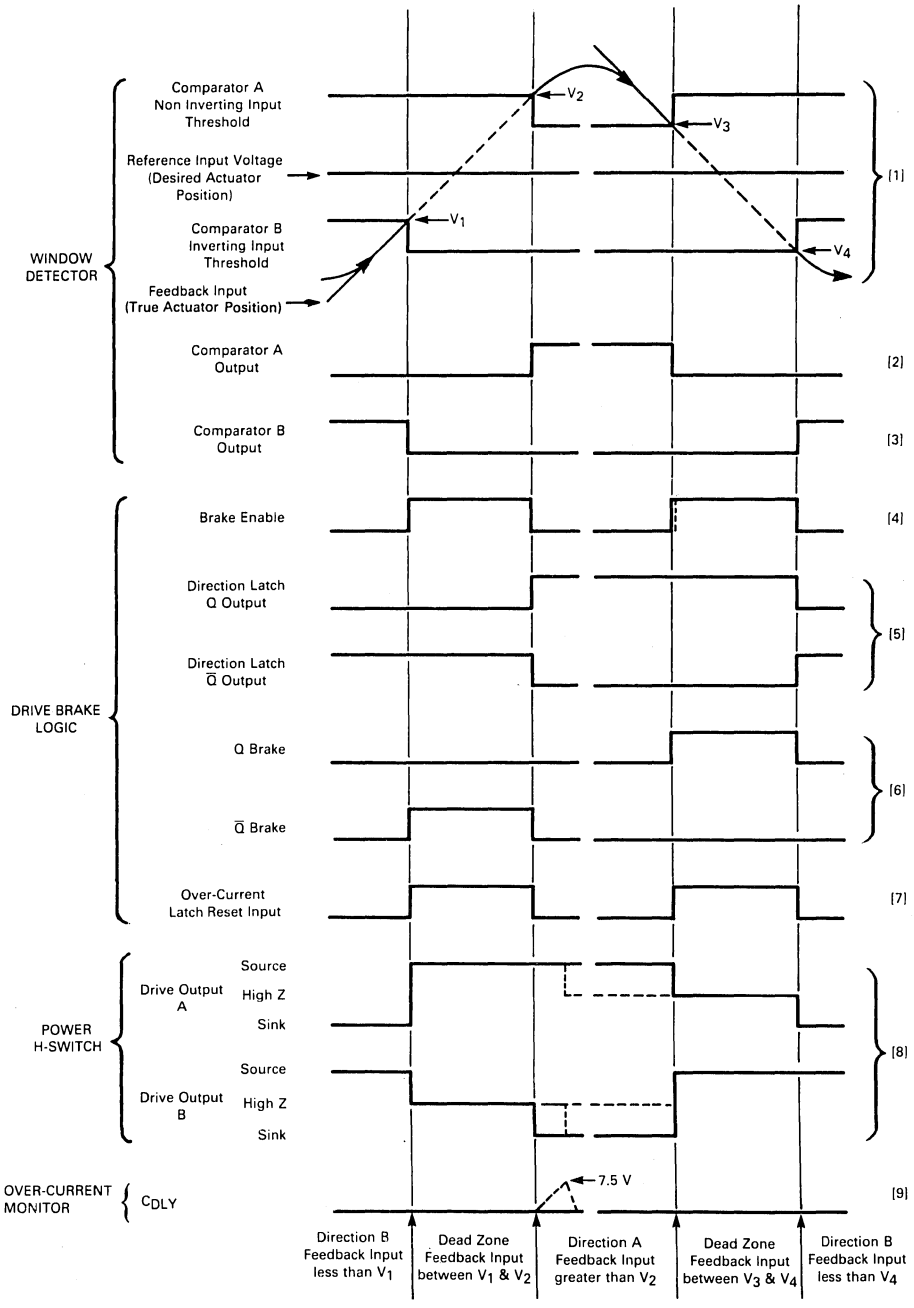


FIGURE 18 — SOLAR TRACKING SERVO SYSTEM

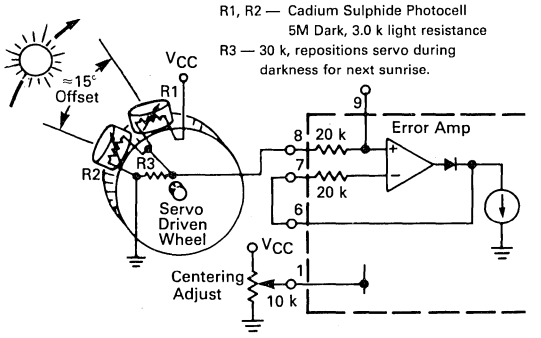
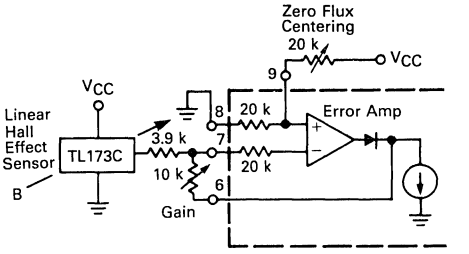
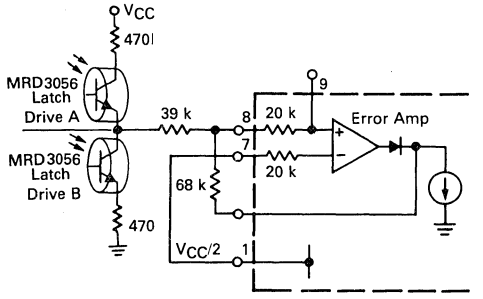


FIGURE 19 — MAGNETIC SENSING SERVO SYSTEM



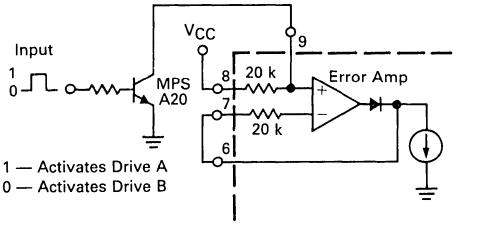
Typical sensitivity with gain set at 3.9 k is 1.5 mV/gauss. Servo motor controls magnetic field about sensor.

FIGURE 20 — INFRARED LATCHED TWO POSITION SERVO SYSTEM



Over-current monitor (not shown) shuts down servo when end stop is reached.

FIGURE 21 — DIGITAL TWO POSITION SERVO SYSTEM



Over-Current monitor (not shown) shuts down servo when end stop is reached.

FIGURE 22 — 0.25 Hz SQUARE-WAVE SERVO AGITATOR

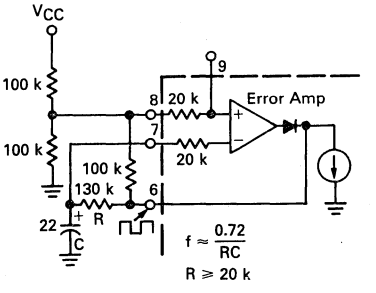


FIGURE 23 — SECOND ORDER LOW-PASS ACTIVE FILTER

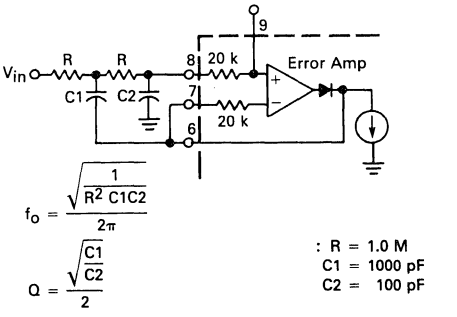
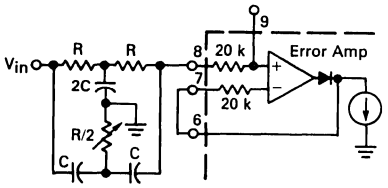


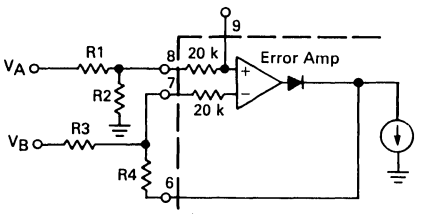
FIGURE 24 — NOTCH FILTER



$$f_{notch} = \frac{1}{2\pi RC}$$

For 60 Hz R = 53.6 k, C = 0.05

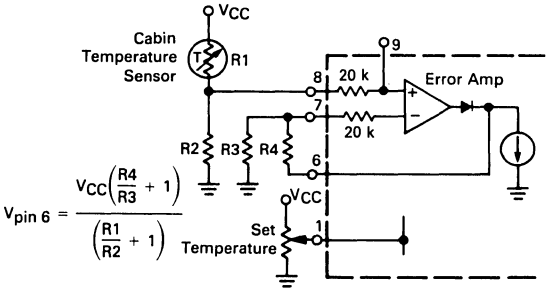
FIGURE 25 — DIFFERENTIAL INPUT AMPLIFIER



$$V_{pin6} = V_A\left(\frac{R3+R4}{R1+R2}\frac{R2}{R3}\right) - \left(\frac{R4}{R3}V_B\right)$$

4

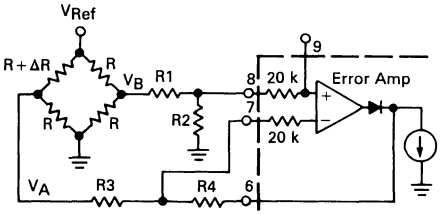
FIGURE 26 — TEMPERATURE SENSING SERVO SYSTEM



$$V_{pin\ 6} = \frac{V_{CC}\left(\frac{R4}{R3}+1\right)}{\left(\frac{R1}{R2}+1\right)}$$

In this application the servo motor drives the heat/air conditioner modulator door in a duct system.

FIGURE 27 — BRIDGE AMPLIFIER

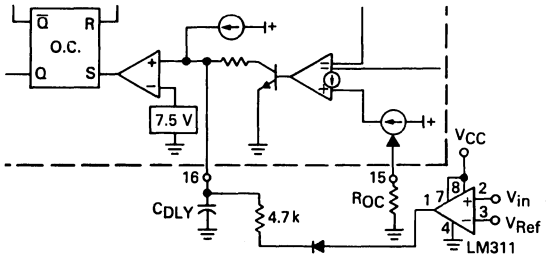


$$V_A - V_B = V_{Ref}\left(\frac{\Delta R}{4R+2\Delta R}\right)$$

R1 = R3, R2 = R4, R1 >>R

$$V_{pin6} = \frac{R4}{R3}(V_A - V_B)$$

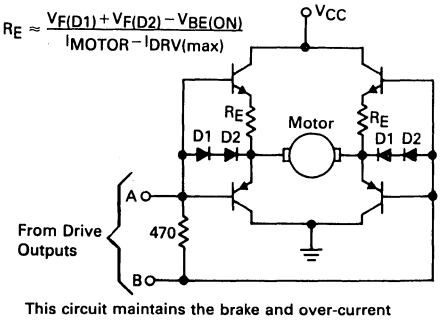
FIGURE 28 — REMOTE LATCHED SHUTDOWN



A direction change signal is required at Pins 2 or 3 to reset the over-current latch.

FIGURE 29 — POWER H-SWITCH BUFFER

$$R_E \approx \frac{V_{F(D1)} + V_{F(D2)} - V_{BE(ON)}}{I_{MOTOR} - I_{DRV(max)}}$$



This circuit maintains the brake and over-current features of the MC33030. Set R_{OC} to 15 k for $I_{DRV(max)} \approx 0.5$ A.

FIGURE 30 — ADJUSTABLE PRESSURE DIFFERENTIAL REGULATOR

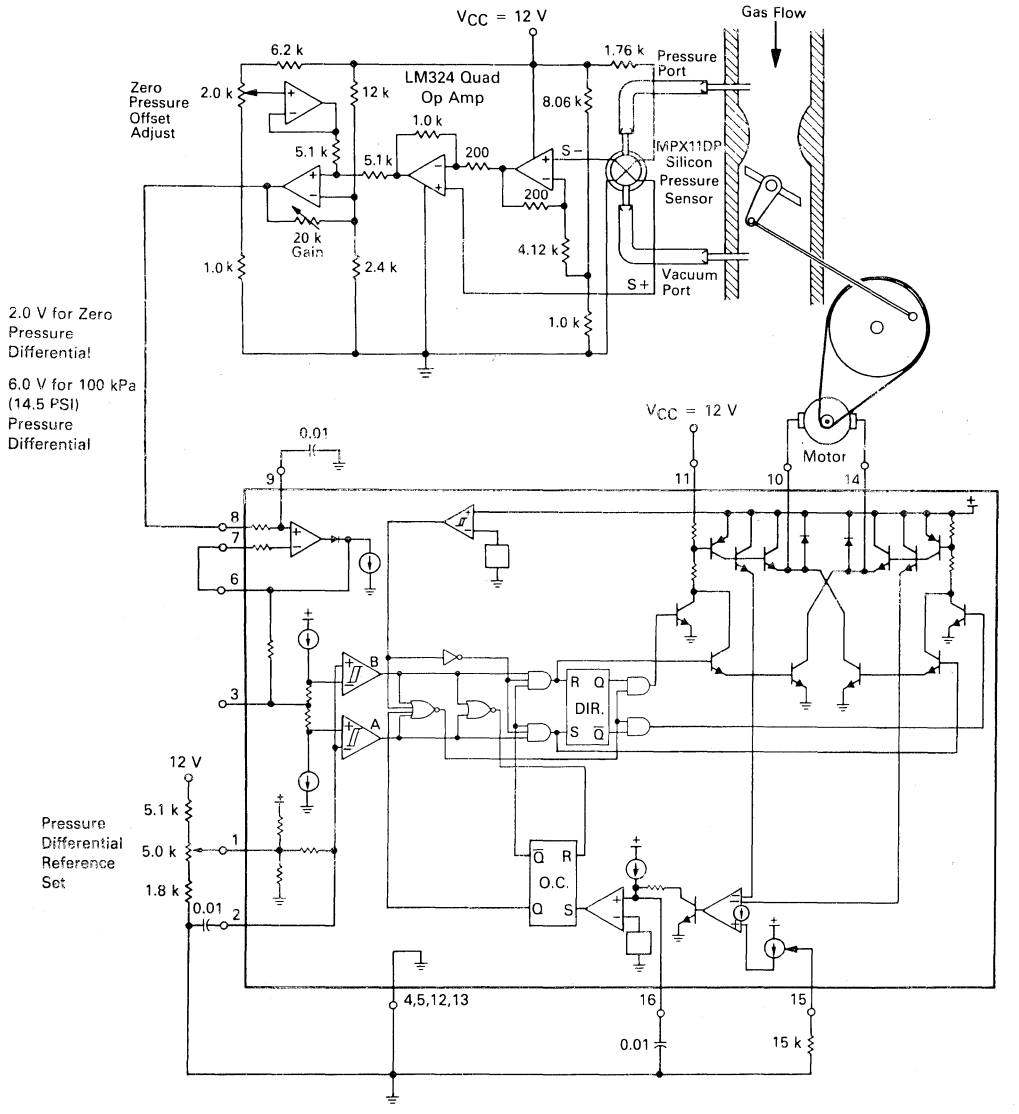


FIGURE 31 — SWITCHING MOTOR CONTROLLER WITH BUFFERED OUTPUT AND TACH FEEDBACK

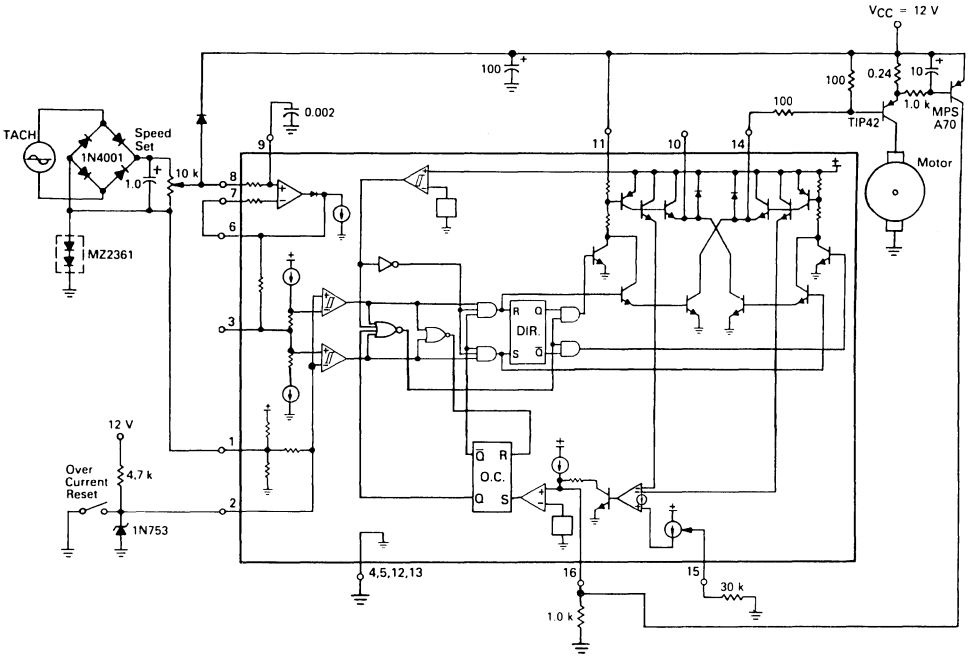
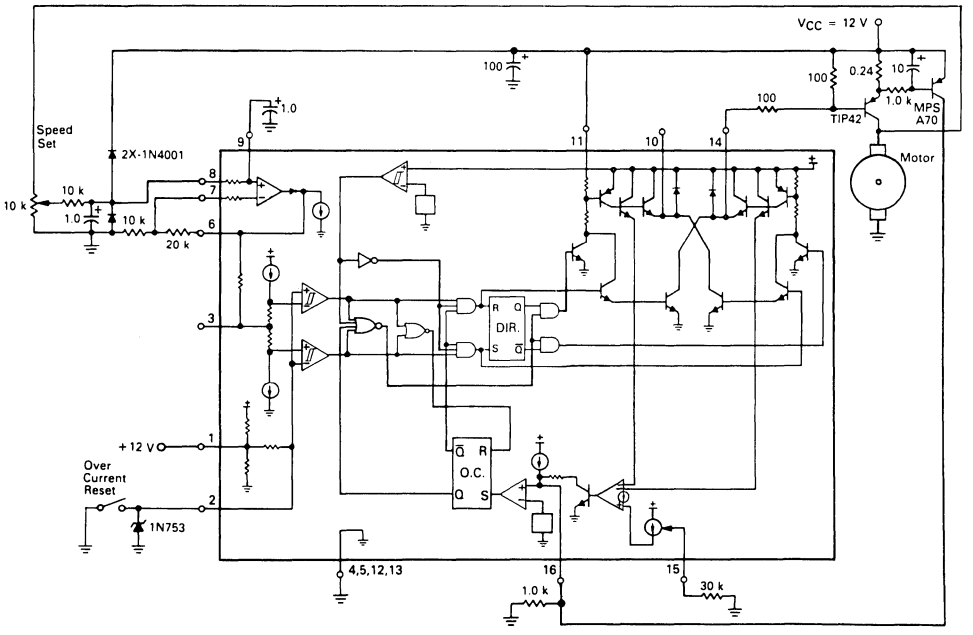


FIGURE 32 — SWITCHING MOTOR CONTROLLER WITH BUFFERED OUTPUT AND BACK EMF SENSING



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC33033

Advance Information

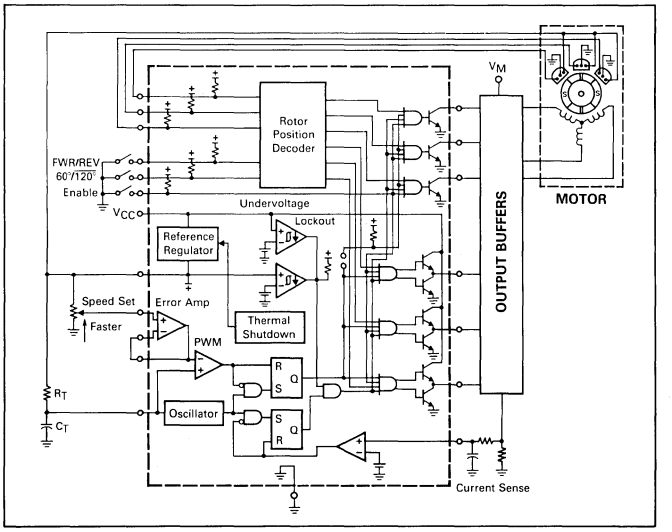
BRUSHLESS DC MOTOR CONTROLLER

The MC33033 is a high performance second generation, limited feature, monolithic brushless DC motor controller which has evolved from Motorola's full featured MC33034 and MC33035 controllers. It contains all of the active functions required for the implementation of open-loop, three or four phase motor control. The device consists of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, fully accessible error amplifier, pulse width modulator comparator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs. Unlike its predessors, it does not feature separate drive circuit supply and ground pins, brake input, or fault output signal.

Included in the MC33033 are protective features consisting of undervoltage lockout, cycle-by-cycle current limiting with a selectable time delayed latched shutdown mode, and internal thermal shutdown.

Typical motor control functions include open-loop speed, forward or reverse direction, and run enable. The MC33033 is designed to operate brushless motors with electrical sensor phasings of 60°/300° or 120°/240°, and can also efficiently control brush DC motors.

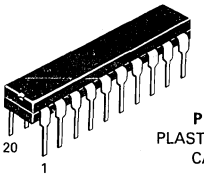
- 10 V to 30 V Operation
- Undervoltage Lockout
- 6.25 V Reference Capable of Supplying Sensor Power
- Fully Accessible Error Amplifier for Closed-Loop Servo Applications
- High Current Drivers can Control MPM3003 MOSFET 3-Phase Bridge
- Cycle-By-Cycle Current Limiting
- Internal Thermal Shutdown
- Selectable 60°/300° or 120°/240° Sensor Phasings
- Also Efficiently Controls Brush DC Motors with MPM3002 MOSFET H-Bridge



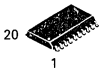
This document contains information on a new product. Specifications and information herein are subject to change without notice.

BRUSHLESS DC MOTOR CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

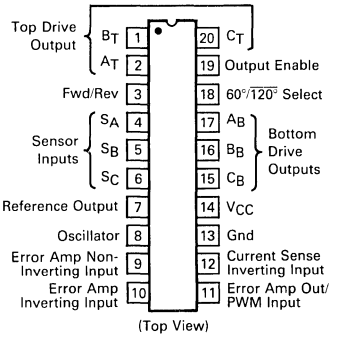


P SUFFIX
PLASTIC PACKAGE
CASE 738



DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20L)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Ambient Temperature Range	Package
MC33033P	−40°C to +85°C	Plastic DIP
MC33033DW	−40°C to +85°C	SO-20L

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	30	V
Digital Inputs (Pins 3, 4, 5, 6, 18, 19)	—	V_{ref}	V
Oscillator Input Current (Source or Sink)	I_{OSC}	30	mA
Error Amp Input Voltage Range (Pins 9, 10, Note 1)	V_{IR}	−3.0 to V_{ref}	V
Error Amp Output Current (Source or Sink, Note 2)	I_{Out}	10	mA
Current Sense Input Voltage Range	V_{Sense}	−0.3 to 5.0	V
Top Drive Voltage (Pins 1, 2, 20)	$V_{CE(top)}$	40	V
Top Drive Sink Current (Pins 1, 2, 20)	$I_{Sink(Top)}$	50	mA
Bottom Drive Output Current (Source or Sink, Pins 15, 16, 17)	I_{DRV}	100	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 85°C Thermal Resistance, Junction to Air	 P_D $R_{\theta JA}$	 867 75	 mW °C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 20 V, R_T = 4.7 k, C_T = 10 nF, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_{ref} = 1.0 mA) T_A = 25°C T_A = −40°C to +85°C	V_{ref}	 5.9 5.82	 6.24 —	 6.5 6.57	V
Line Regulation (V_{CC} = 10 V to 30 V, I_{ref} = 1.0 mA)	Reg_{line}	—	1.5	30	mV
Load Regulation (I_{ref} = 1.0 mA to 20 mA)	Reg_{load}	—	16	30	mV
Output Short-Circuit Current (Note 3)	I_{SC}	40	75	—	mA
Reference Under Voltage Lockout Threshold	V_{th}	4.0	4.5	5.0	V
ERROR AMPLIFIER					
Input Offset Voltage (T_A = −40°C to +85°C)	V_{IO}	—	0.4	10	mV
Input Offset Current (T_A = −40°C to +85°C)	I_{IO}	—	8.0	500	nA
Input Bias Current (T_A = −40°C to +85°C)	I_{IB}	—	−46	−1000	nA
Input Common Mode Voltage Range	V_{ICR}	(0 V to V_{ref})			V
Open-Loop Voltage Gain (V_O = 3.0 V, R_L = 15 k)	A_{VOL}	70	80	—	dB
Input Common Mode Rejection Ratio	CMRR	55	86	—	dB
Power Supply Rejection Ratio (V_{CC} = 10 V to 30 V)	PSRR	65	105	—	dB
Output Voltage Swing High State (R_L = 15 k to Ground) Low State (R_L = 15 k to V_{ref})	 V_{OH} V_{OL}	 4.6 —	 5.3 0.5	 — 1.0	V

NOTES:
1. The input common mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V.
2. The compliance voltage must not exceed the range of −0.3 to V_{ref}.
3. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 20 V, R_T = 4.7 k, C_T = 10 nF, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR SECTION					
Oscillator Frequency	f_{OSC}	22	25	28	kHz
Frequency Change with Voltage (V_{CC} = 10 V to 30 V)	$\Delta f_{OSC}/\Delta V$	—	0.01	5.0	%
Sawtooth Peak Voltage	$V_{OSC(P)}$	—	4.1	4.5	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	1.2	1.5	—	V
LOGIC INPUTS					
Input Threshold Voltage (Pins 3, 4, 5, 6, 18, 19) High State Low State	 V_{IH} V_{IL}	 3.0 —	 2.2 1.7	 — 0.8	V
Sensor Inputs (Pins 4, 5, 6) High State Input Current (V_{IH} = 5.0 V) Low State Input Current (V_{IL} = 0 V)	 I_{IH} I_{IL}	 −150 −600	 −70 −337	 −20 −150	μA
Forward/Reverse, 60°/120° Select and Output Enable (Pins 3, 18, 19) High State Input Current (V_{IH} = 5.0 V) Low State Input Current (V_{IL} = 0 V)	 I_{IH} I_{IL}	 −75 −300	 −36 −175	 −10 −75	μA
CURRENT-LIMIT COMPARATOR					
Threshold Voltage	V_{th}	85	101	115	mV
Input Common Mode Voltage Range	V_{ICR}	—	3.0	—	V
Input Bias Current	I_{IB}	—	−0.9	−5.0	μA
OUTPUTS AND POWER SECTIONS					
To Drive Output Sink Saturation (I_{sink} = 25 mA)	$V_{CE(sat)}$	—	0.5	1.5	V
Top Drive Output Off-State Leakage (V_{CE} = 30 V)	$I_{DRV(leak)}$	—	0.06	100	μA
Top Drive Output Switching Time (C_L = 47 pF, R_L = 1.0 k) Rise Time Fall Time	 t_r t_f	 — —	 107 26	 300 300	ns
Bottom Drive Output Voltage High State (V_{CC} = 30 V, I_{source} = 50 mA) Low State (V_{CC} = 30 V, I_{sink} = 50 mA)	 V_{OH} V_{OL}	 (V_{CC} − 2.0) —	 (V_{CC} − 1.1) 1.5	 — 2.0	V
Bottom Drive Output Switching Time (C_L = 1000 pF) Rise Time Fall Time	 t_r t_f	 — —	 38 30	 200 200	ns
Under Voltage Lockout Drive Output Enabled (V_{CC} Increasing) Hysteresis	 $V_{th(on)}$ V_H	 8.2 0.1	 8.9 0.2	 10 0.3	V
Power Supply Current	I_{CC}	—	15	22	mA

FIGURE 1 — OSCILLATOR FREQUENCY versus TIMING RESISTOR

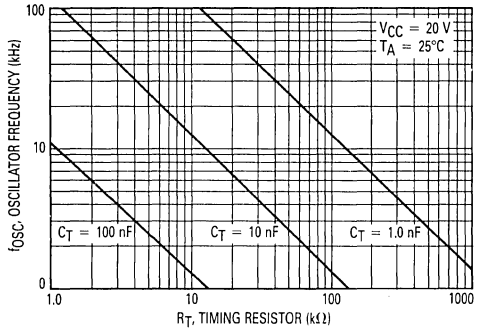


FIGURE 2 — OSCILLATOR FREQUENCY CHANGE versus TEMPERATURE

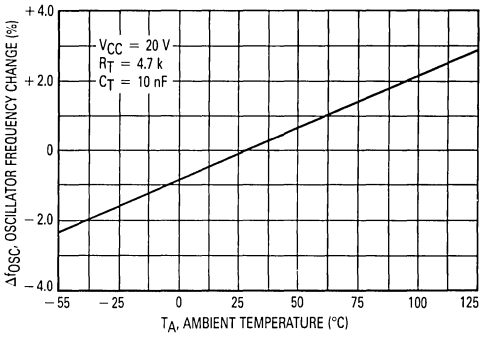


FIGURE 3 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

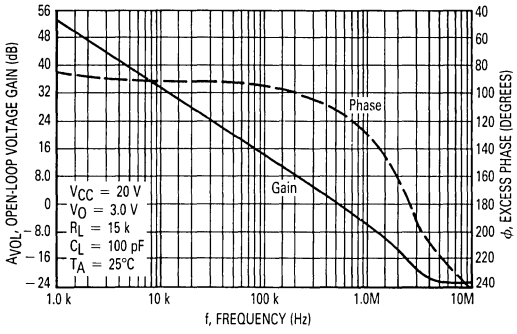


FIGURE 4 — ERROR AMP OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

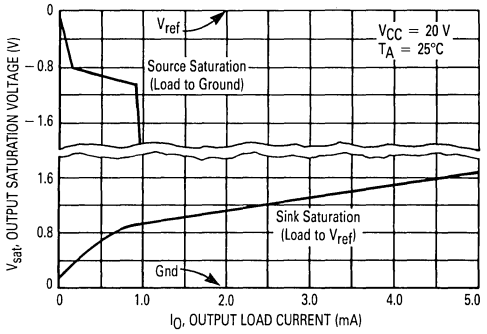


FIGURE 5 — ERROR AMP SMALL-SIGNAL TRANSIENT RESPONSE

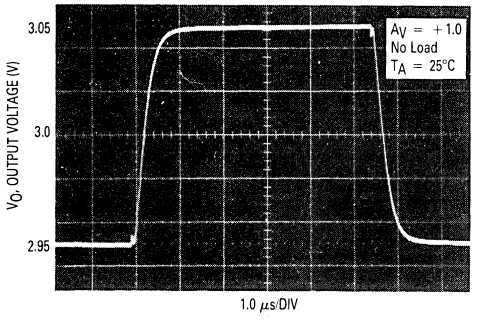


FIGURE 6 — ERROR AMP LARGE-SIGNAL TRANSIENT RESPONSE

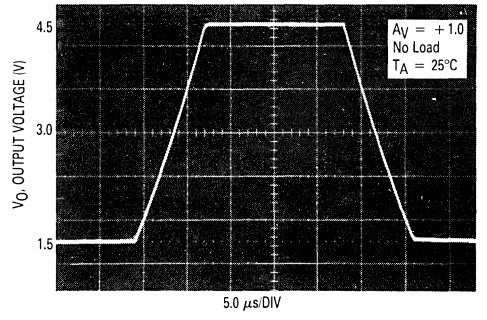


FIGURE 7 — REFERENCE OUTPUT VOLTAGE CHANGE versus OUTPUT SOURCE CURRENT

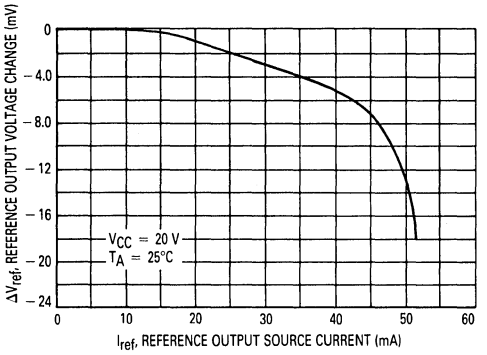


FIGURE 8 — REFERENCE OUTPUT VOLTAGE versus SUPPLY VOLTAGE

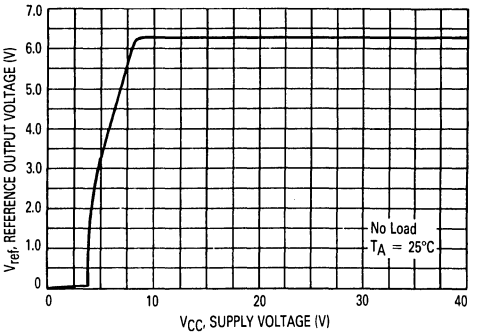


FIGURE 9 — REFERENCE OUTPUT VOLTAGE versus TEMPERATURE

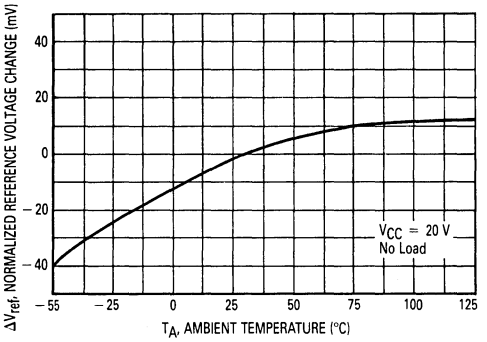


FIGURE 10 — OUTPUT DUTY CYCLE versus PWM INPUT VOLTAGE

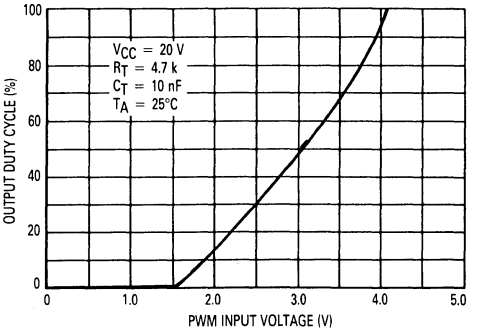


FIGURE 11 — BOTTOM DRIVE RESPONSE TIME versus CURRENT SENSE INPUT VOLTAGE

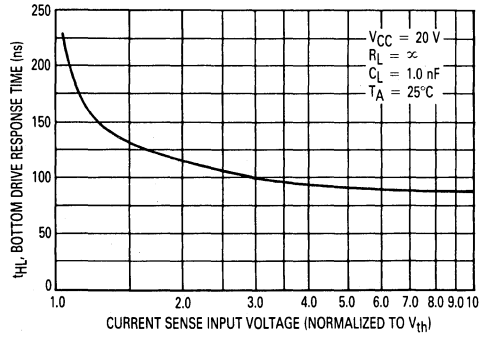


FIGURE 12 — TOP DRIVE OUTPUT SATURATION VOLTAGE versus SINK CURRENT

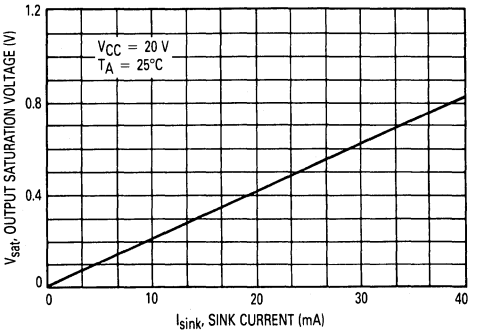


FIGURE 13 — TOP DRIVE OUTPUT WAVEFORM

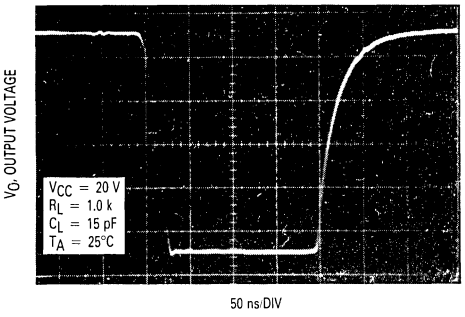


FIGURE 14 — BOTTOM DRIVE OUTPUT WAVEFORM

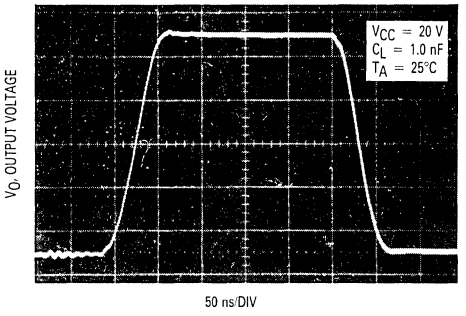


FIGURE 15 — BOTTOM DRIVE OUTPUT WAVEFORM

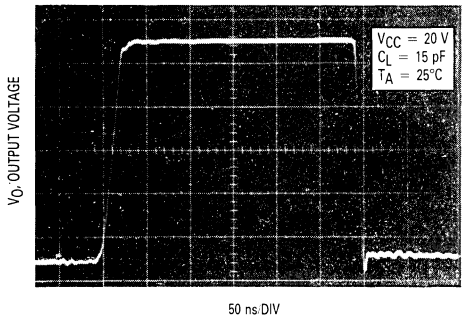


FIGURE 16 — BOTTOM DRIVE OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

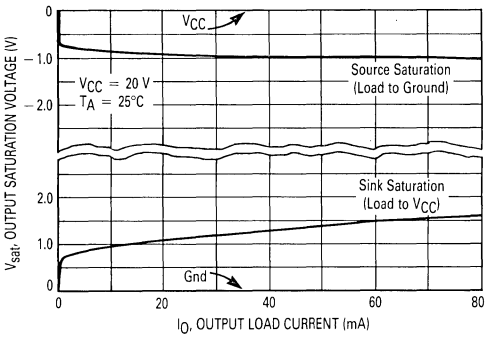
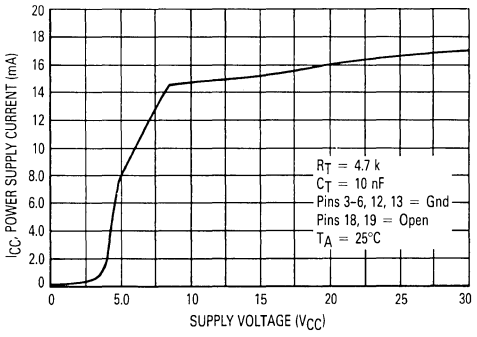


FIGURE 17 — SUPPLY CURRENT versus VOLTAGE



PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1, 2, 20	B_T, A_T, C_T	These three open collector Top Drive Outputs are designed to drive the external upper power switch transistors.
3	FWD/REV	The Forward/Reverse Input is used to change the direction of motor rotation.
4, 5, 6	S_A, S_B, S_C	These three Sensor Inputs control the commutation sequence.
7	Reference Output	This output provides charging current for the oscillator timing capacitor C_T and a reference for the error amplifier. It may also serve to furnish sensor power.
8	Oscillator	The Oscillator frequency is programmed by the values selected for the timing components, R_T and C_T.
9	Error Amp (Noninverting Input)	This input is normally connected to the speed set potentiometer.
10	Error Amp (Inverting Input)	This input is normally connected to the Error Amp Output in open-loop applications.
11	Error Amp Output/PWM Input	This pin is available for compensation in closed-loop applications.
12	Current Sense (Noninverting Input)	A 100 mV signal, with respect to Pin 13, at this input terminates output switch conduction during a given oscillator cycle. This pin normally connects to the top side of the current sense resistor.
13	Ground	This pin supplies a separate ground return for the control circuit and should be referenced back to the power source ground.
14	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a V_{CC} range of 10 V to 30 V.
15, 16, 17	C_B, B_B, A_B	These three totem pole Bottom Drive Outputs are designed for direct drive of the external bottom power switch transistors.
18	60°/$\overline{120°}$ Select	The electrical state of this pin configures the control circuit operation for either 60° (high state) or 120° (low state) sensor electrical phasing inputs.
19	Output Enable	A logic high at this input causes the motor to run, while a low causes it to coast.

INTRODUCTION

The MC33033 is one of a series of high performance monolithic DC brushless motor controllers produced by Motorola. It contains all of the functions required to implement a limited-feature, open-loop, three or four phase motor control system. Constructed with Bipolar Analog technology, it offers a high degree of performance and ruggedness in hostile industrial environments. The MC33033 contains a rotor position decoder for proper commutation sequencing, a temperature compensated reference capable of supplying sensor power, a frequency programmable sawtooth oscillator, a fully accessible error amplifier, a pulse width modulator comparator, three open collector top drive outputs, and three high current totem pole bottom driver outputs ideally suited for driving power MOSFETs.

Included in the MC33033 are protective features consisting of undervoltage lockout, cycle by cycle current limiting with a latched shutdown mode, and internal thermal shutdown.

Typical motor control functions include open-loop speed control, forward or reverse rotation, and run enable. In addition, the MC33033 has a 60°/120° select pin which configures the rotor position decoder for either 60° or 120° sensor electrical phasing inputs.

FUNCTIONAL DESCRIPTION

A representative internal block diagram is shown in Figure 18, with various applications shown in Figures 34, 36, 37, 41, 43, and 44. A discussion of the features and function of each of the internal blocks given below and referenced to Figures 18 and 36.

Rotor Position Decoder

An internal rotor position decoder monitors the three sensor inputs (Pins 4, 5, 6) to provide the proper sequencing of the top and bottom drive outputs. The sensor inputs are designed to interface directly with open collector type Hall Effect switches or opto slotted couplers. Internal pull-up resistors are included to minimize the required number of external components. The inputs are TTL compatible, with their thresholds typically at 2.2 volts. The MC33033 series is designed to control three phase motors and operate with four of the most common conventions of sensor phasing. A 60°/120° select (Pin 18) is conveniently provided which affords the MC33033 to configure itself to control motors having either 60°, 120°, 240° or 300° electrical sensor phasing. With three sensor inputs there are eight possible input code combinations, six of which are valid rotor positions. The remaining two codes are invalid and are usually caused by an open or shorted sensor line. With six valid input codes, the decoder can resolve the motor rotor position to within a window of 60 electrical degrees.

The forward/reverse input (Pin 3) is used to change the direction of motor rotation by reversing the voltage across the stator winding. When the input changes state, from high to low with a given sensor input code (for example 100), the enabled top and bottom drive outputs with the same alpha designation are exchanged (A_T to A_B, B_T to B_B, C_T to C_B). In effect the commutation sequence is reversed and the motor changes directional rotation.

Motor on/off control is accomplished by the output enable (Pin 19). When left disconnected, an internal pull-up resistor to a positive source, enables sequencing of the top and bottom drive outputs. When grounded, the top drive outputs turn off and the bottom drives are forced low, causing the motor to coast.

The commutation logic truth table is shown in Figure 19. In half wave motor drive applications, the top drive outputs are not required and are typically left disconnected.

Error Amplifier

A high performance, fully compensated error amplifier with access to both inputs and output (Pins 9, 10, 11) is provided to facilitate the implementation of closed-loop motor speed control. The amplifier features a typical DC voltage gain of 80 dB, 0.6 MHz gain bandwidth, and a wide input common mode voltage range that extends from ground to V_{ref}. In most open-loop speed control applications, the amplifier is configured as a unity gain voltage follower with the non-inverting input connected to the speed set voltage source. Additional configurations are shown in Figures 29 through 33.

Oscillator

The frequency of the internal ramp oscillator is programmed by the values selected for timing components R_T and C_T. Capacitor C_T is charged from the reference output (Pin 7) through resistor R_T and discharged by an internal discharge transistor. The ramp peak and valley voltages are typically 4.1 V and 1.5 V respectively. To provide a good compromise between audible noise and output switching efficiency, an oscillator frequency in the range of 20 kHz to 30 kHz is recommended. Refer to Figure 1 for component selection.

Pulse Width Modulator

The use of pulse width modulation provides an energy efficient method of controlling the motor speed by varying the average voltage applied to each stator winding during the commutation sequence. As C_T discharges, the oscillator sets both latches, allowing conduction of the top and bottom drive outputs. The PWM comparator resets the upper latch, terminating the bottom drive output conduction when the positive-going ramp of C_T becomes greater than the error amplifier output. The pulse width modulator timing diagram is shown in Figure 20. Pulse width modulation for speed control appears only at the bottom drive outputs.

Current Limit

Continuous operation of a motor that is severely overloaded results in overheating and eventual failure. This destructive condition can best be prevented with the use of cycle-by-cycle current limiting. That is, each on-cycle is treated as a separate event. Cycle-by-cycle current limiting is accomplished by monitoring the stator

FIGURE 18 — REPRESENTATIVE BLOCK DIAGRAM

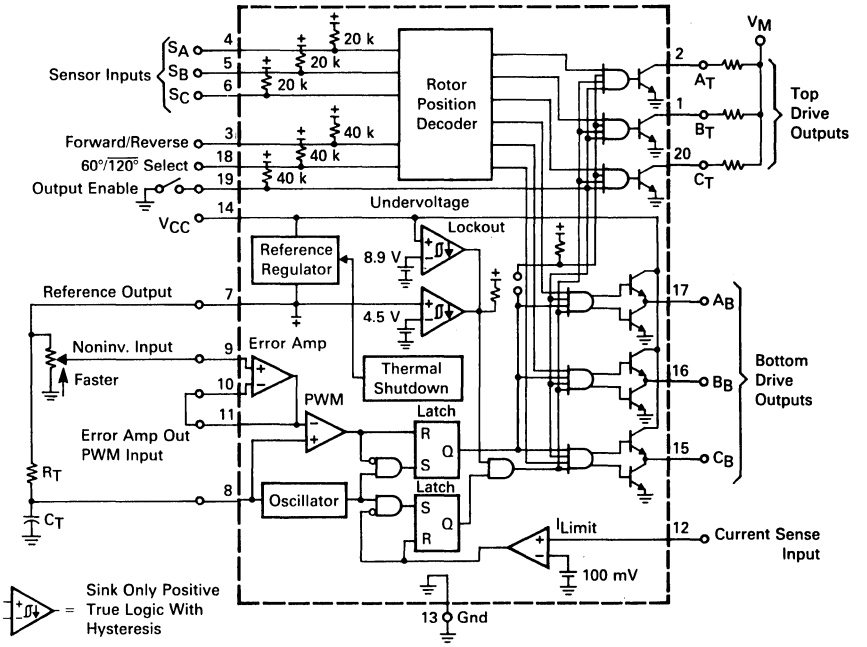


FIGURE 19 — THREE PHASE, SIX STEP COMMUTATION TRUTH TABLE (Note 1)

Inputs (Note 2)									Outputs (Note 3)						
Sensor Electrical Phasing (Note 4)									Top Drives			Bottom Drives			
60°			120°					Current							
S_A	S_B	S_C	S_A	S_B	S_C	F/R	Enable	Sense	A_T	B_T	C_T	A_B	B_B	C_B	
1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	**(Note 5)**
1	1	0	1	1	0	1	1	0	1	0	1	0	0	1	F/R = 1
1	1	1	0	1	0	1	1	0	1	0	1	1	0	0	
0	1	1	0	1	1	1	1	0	1	1	0	1	0	0	
0	0	1	0	0	1	1	1	0	1	1	0	0	1	0	
0	0	0	1	0	1	1	1	0	0	1	1	0	1	0	
1	0	0	1	0	0	0	1	0	1	1	0	1	0	0	**(Note 5)**
1	1	0	1	1	0	0	1	0	1	1	0	0	1	0	F/R = 0
1	1	1	0	1	0	0	1	0	0	1	1	0	1	0	
0	1	1	0	1	1	0	1	0	0	1	1	0	0	1	
0	0	1	0	0	1	0	1	0	1	0	1	0	0	1	
0	0	0	1	0	1	0	1	0	1	0	1	1	0	0	
1	0	1	1	1	1	X	X	X	1	1	1	0	0	0	**(Note 6)**
0	1	0	0	0	0	X	X	X	1	1	1	0	0	0	
V	V	V	V	V	V	X	0	X	1	1	1	0	0	0	**(Note 7)**
V	V	V	V	V	V	X	1	1	1	1	1	0	0	0	**(Note 8)**

NOTES:

1. V = Any one of six valid sensor or drive combinations.
   X = Don't care.
2. The digital inputs (Pins 3, 4, 5, 6, 18, 19) are all TTL compatible. The current sense input (Pin 12) has a 100 mV threshold with respect to Pin 13. A logic 0 for this input is defined as < 85 mV, and a logic 1 is > 115 mV.
3. The top drive outputs are open collector design and active in the low (0) state.
4. With 60°/120° select (Pin 18) in the high (1) state, configuration is for 60° sensor electrical phasing inputs. With Pin 18 in the low (0) state, configuration is for 120° sensor electrical phasing inputs.
5. Valid 60° or 120° sensor combinations for corresponding valid top and bottom drive outputs.
6. Invalid sensor inputs; All top and bottom drives are off.
7. Valid sensor inputs with enable = 0; All top and bottom drives are off.
8. Valid sensor inputs with enable and current sense = 1; All top and bottom drives are off.

current build-up each time an output switch conducts, and upon sensing an over current condition, immediately turning off the switch and holding it off for the remaining duration of the oscillator ramp-up period. The stator current is converted to a voltage by inserting a ground-referenced sense resistor R_S (Figure 34) in series with the three bottom switch transistors (Q4, Q5, Q6). The voltage developed across the sense resistor is monitored by the current sense input (Pin 12), and compared to the internal 100 mV reference. If the current sense threshold is exceeded, the comparator resets the lower latch and terminates output switch conduction. The value for the sense resistor is:

$$R_S = \frac{0.1}{I_{stator(max)}}$$

The dual-latch PWM configuration ensures that only one single output conduction pulse occurs during any given oscillator cycle, whether terminated by the output of the error amp or the current limit comparator.

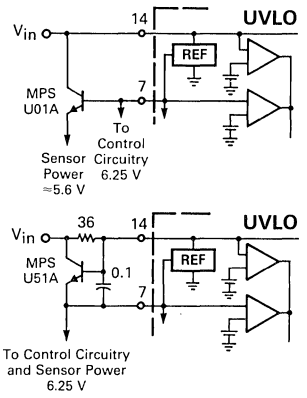
Reference

The on-chip 6.25 V regulator (Pin 7) provides charging current for the oscillator timing capacitor, a reference for the error amplifier, and can supply 20 mA of current suitable for directly powering sensors in low voltage applications. In higher voltage applications it may become necessary to transfer the power dissipated by the regulator off the IC. This is easily accomplished with the addition of an external pass transistor as shown in Figure 21. A 6.25 V reference level was chosen to allow implementation of the simpler NPN circuit, where $V_{ref} - V_{BE}$ exceeds the minimum voltage required by Hall Effect sensors over temperature. With proper transistor selection, and adequate heatsinking, up to one amp of load current can be obtained.

Undervoltage Lockout

A dual Undervoltage Lockout has been incorporated to prevent damage to the IC and the external power switch transistors. Under low power supply conditions, it guarantees that the IC and sensors are fully functional, and that there is sufficient bottom drive output voltage. The positive power supply to the IC (V_{CC}) is monitored to a threshold of 8.9 V. This level ensures sufficient gate drive necessary to attain low $r_{DS(on)}$ when interfacing with standard power MOSFET devices. When directly powering the Hall sensors from the reference, improper sensor operation can result if the reference output voltage should fall below 4.5 V. If one or both of the comparators detects an undervoltage condition, the top drives are turned off and the bottom drive outputs are held in a low state. Each of the comparators contain hysteresis to prevent oscillations when crossing their respective thresholds.

FIGURE 21 — REFERENCE OUTPUT BUFFERS



The NPN circuit is recommended for powering Hall or opto sensors, where the output voltage temperature coefficient is not critical. The PNP circuit is slightly more complex, but also more accurate. Neither circuit has current limiting.

FIGURE 20 — PWM TIMING DIAGRAM

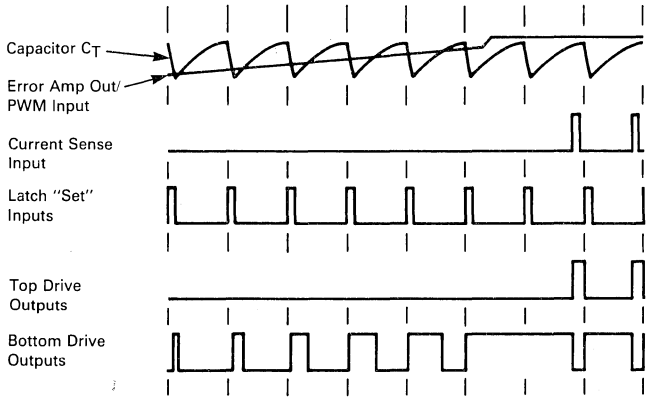
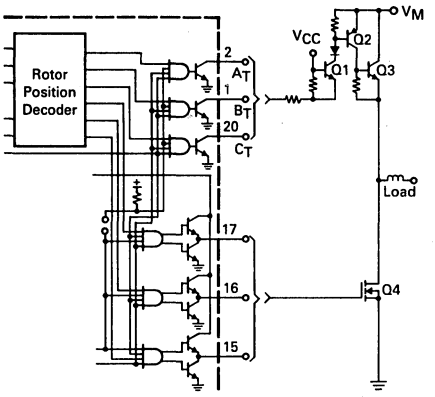


FIGURE 22 — HIGH VOLTAGE INTERFACE WITH NPN POWER TRANSISTORS



Transistor Q1 is a common base stage used to level shift from V_{CC} to the high motor voltage, V_M. The collector diode is required if V_{CC} is present while V_M is low.

FIGURE 23 — HIGH VOLTAGE INTERFACE WITH 'N' CHANNEL POWER MOSFETs

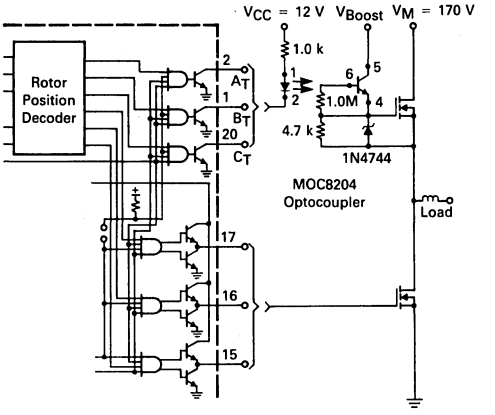
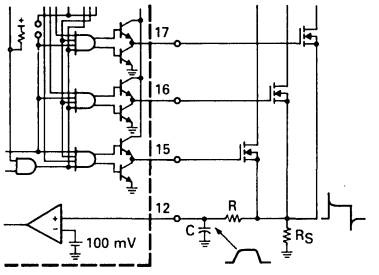
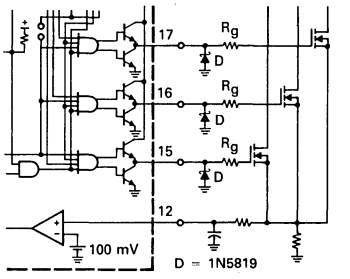


FIGURE 24 — CURRENT WAVEFORM SPIKE SUPPRESSION



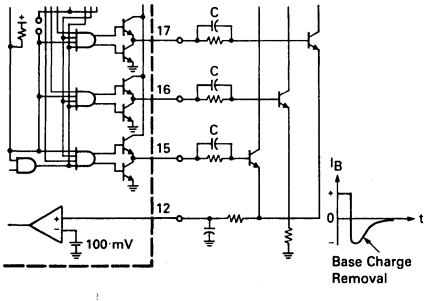
The addition of the RC filter will eliminate current-limit instability caused by the leading edge spike on the current waveform. Resistor R_S should be a low inductance type.

FIGURE 25 — MOSFET DRIVE PRECAUTIONS



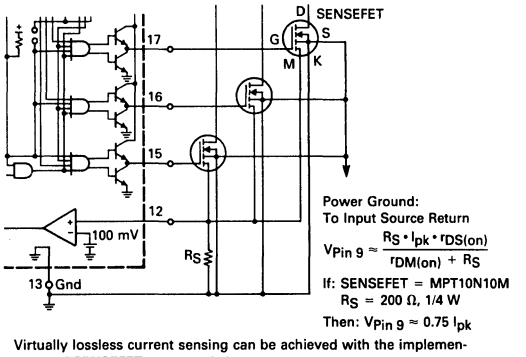
Series gate resistor R_g will damp any high frequency oscillations caused by the MOSFET input capacitance and any series wiring induction in the gate-source circuit. Diode D is required if the negative current into the Bottom Drive Outputs exceeds 50 mA.

FIGURE 26 — BIPOLAR TRANSISTOR DRIVE



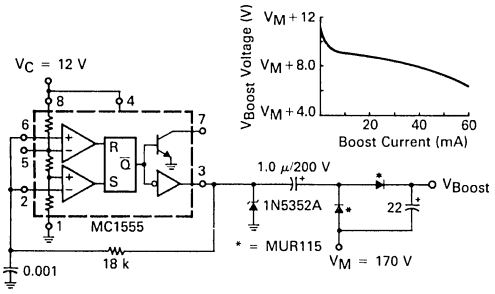
The totem pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C.

FIGURE 27 — CURRENT SENSING POWER MOSFETs



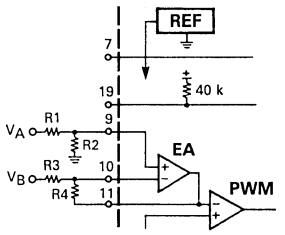
Virtually lossless current sensing can be achieved with the implementation of SENSEFET power switches.

FIGURE 28 — HIGH VOLTAGE BOOST SUPPLY



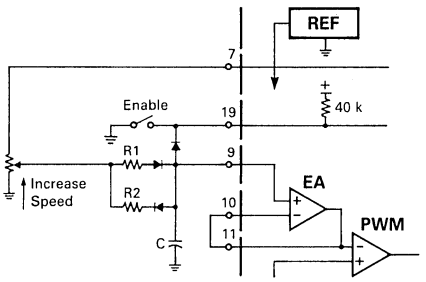
This circuit generates V_{Boost} for Figure 23.

FIGURE 29 — DIFFERENTIAL INPUT SPEED CONTROLLER



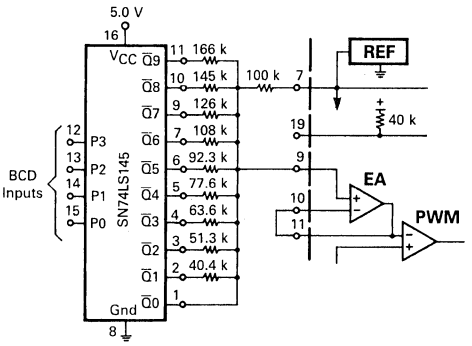
$$V_{pin\ 11} = V_A\left(\frac{R3 + R4}{R1 + R2}\right)\frac{R2}{R3} - \left(\frac{R4}{R3}V_B\right)$$

FIGURE 30 — CONTROLLED ACCELERATION/DECELERATION



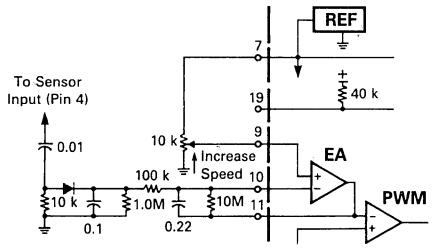
Resistor R1 with capacitor C sets the acceleration time constant while R2 controls the deceleration. The values of R1 and R2 should be at least ten times greater than the speed set potentiometer to minimize time constant variations with different speed settings.

FIGURE 31 — DIGITAL SPEED CONTROLLER



The SN74LS145 is an open collector BCD to One of Ten decoder. When connected as shown, input codes 0000 through 1001 steps the PWM in increments of approximately 10% from 0 to 90% on-time. Input codes 1010 through 1111 will produce 100% on-time or full motor speed.

FIGURE 32 — CLOSED LOOP SPEED CONTROL



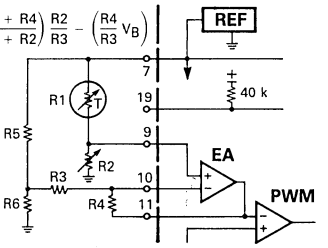
The rotor position sensors can be used as a tachometer. By differentiating the positive-going edges and then integrating them over time, a voltage proportional to speed can be generated. The error amp compares this voltage to that of the speed set to control the PWM.

FIGURE 33 — CLOSED LOOP TEMPERATURE CONTROL

$$V_{pin\ 11} = V_{ref}\left(\frac{R3 + R4}{R1 + R2}\right)\frac{R2}{R3} - \left(\frac{R4}{R3}V_B\right)$$

$$V_B = \frac{V_{ref}}{\left(\frac{R5}{R6} + 1\right)}$$

$R3 \gg R6 \parallel R6$



This circuit can control the speed of a cooling fan proportional to the difference between the sensor and set temperatures. The control loop is closed as the forced air cools the NTC thermistor. For controlled heating applications, exchange the positions of R1 and R2.

Drive Outputs

The three top drive outputs (Pins 1, 2, 20) are open collector NPN transistors capable of sinking 50 mA with a minimum breakdown of 30 volts. Interfacing into higher voltage applications is easily accomplished with the circuits shown in Figures 22 and 23.

The three totem pole bottom drive outputs (Pins 15, 16, 17) are particularly suited for direct drive of 'N' channel MOSFETs or NPN bipolar transistors (Figures 24, 25, 26 and 27). Each output is capable of sourcing and sinking up to 100 mA.

4

Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC in the event the maximum junction temperature is exceeded. When activated, typically at 170°C, the IC acts as though the regulator was disabled, in turn shutting down the IC.

SYSTEM APPLICATIONS

Three Phase Motor Commutation

The three phase application shown in Figure 34 is an open-loop motor controller with full wave, six step drive. The upper power switch transistors are Darlington PNPs while the lower switches are 'N' channel power MOSFETs. Each of these devices contains an internal parasitic catch diode that is used to return the stator inductive energy back to the power supply. The outputs are capable of driving a delta or wye connected stator, and a grounded neutral wye if split supplies are used. At any given rotor position, only one top and one bottom power switch (of different totem poles) is enabled. This configuration switches both ends of the stator winding from supply to ground which causes the current flow to be bidirectional or full wave. A leading edge spike is usually present on the current waveform and can cause a current-limit error. The spike can be eliminated by adding an RC filter in series with the current sense input. Using a low inductance type resistor for R_S will also aid in spike reduction. Figure 35 shows the commutation waveforms over two electrical cycles. The first cycle (0° to 360°) depicts motor operation at full speed while the second cycle (360° to 720°) shows a reduced speed with about 50 percent pulse width modulation. The current waveforms reflect a constant torque load and are shown synchronous to the commutation frequency for clarity.

FIGURE 34 — THREE PHASE, SIX STEP, FULL WAVE MOTOR CONTROLLER

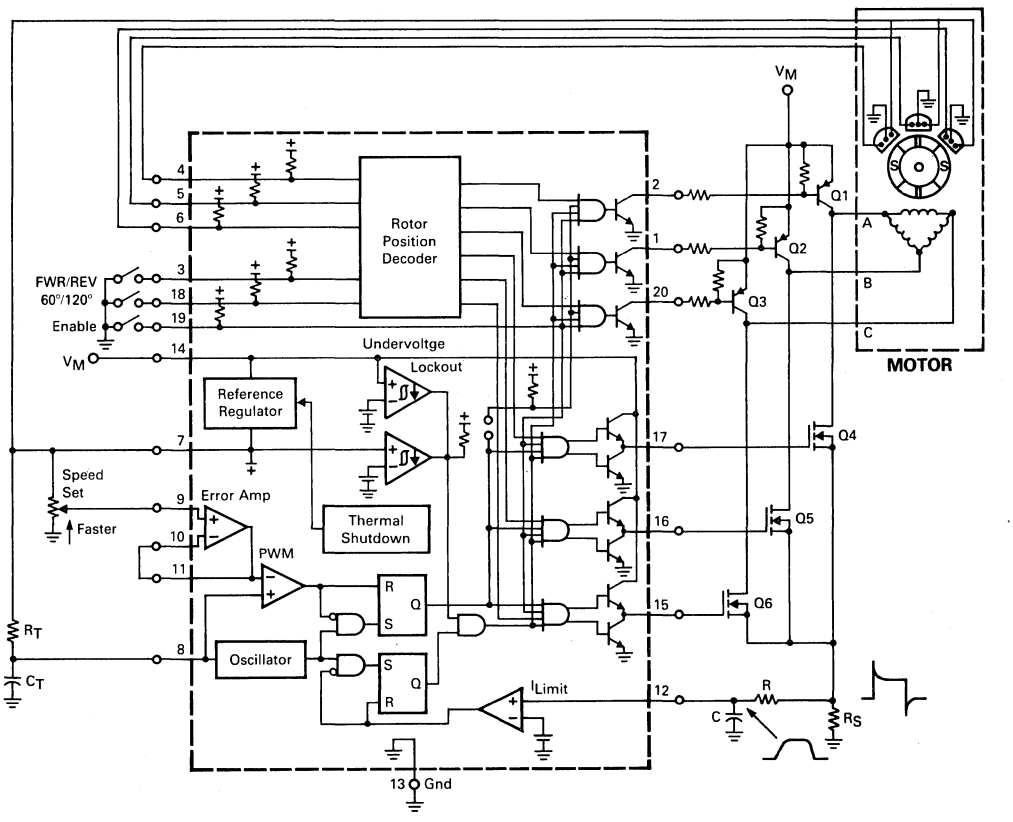


FIGURE 35 — THREE PHASE, SIX STEP, FULL WAVE COMMUTATION WAVEFORMS

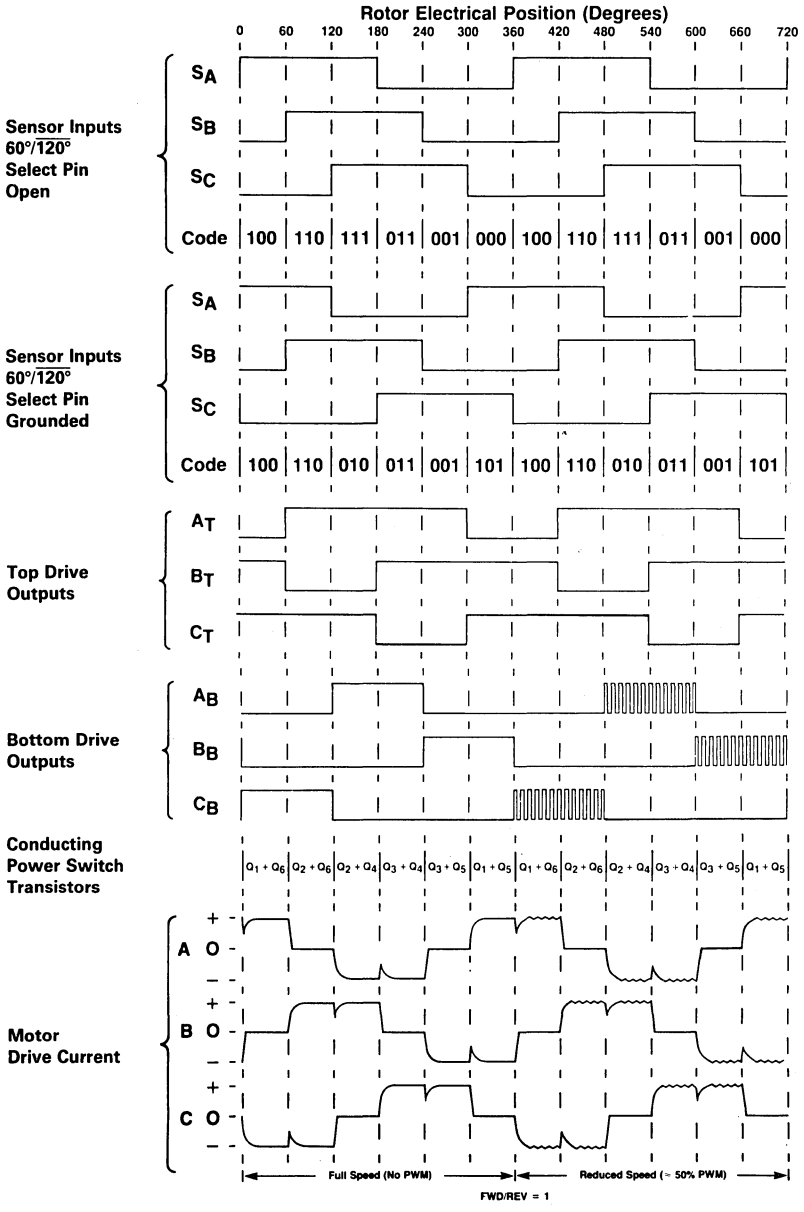
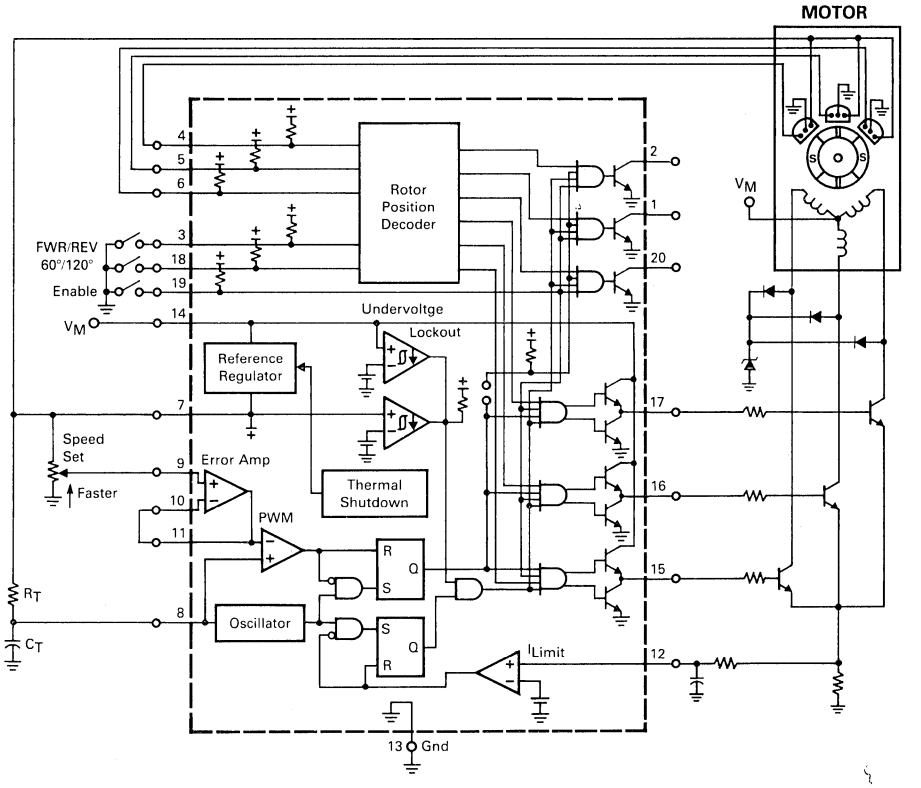


Figure 36 shows a three phase, three step, half wave motor controller. This configuration is ideally suited for automobile and other low voltage applications since there is only one power switch voltage drop in series with a given stator winding. Current flow is unidirectional or half wave because only one end of each winding is switched. The stator flyback voltage is clamped by a single zener and three diodes.

4

FIGURE 36 — THREE PHASE, THREE STEP, HALF WAVE MOTOR CONTROLLER

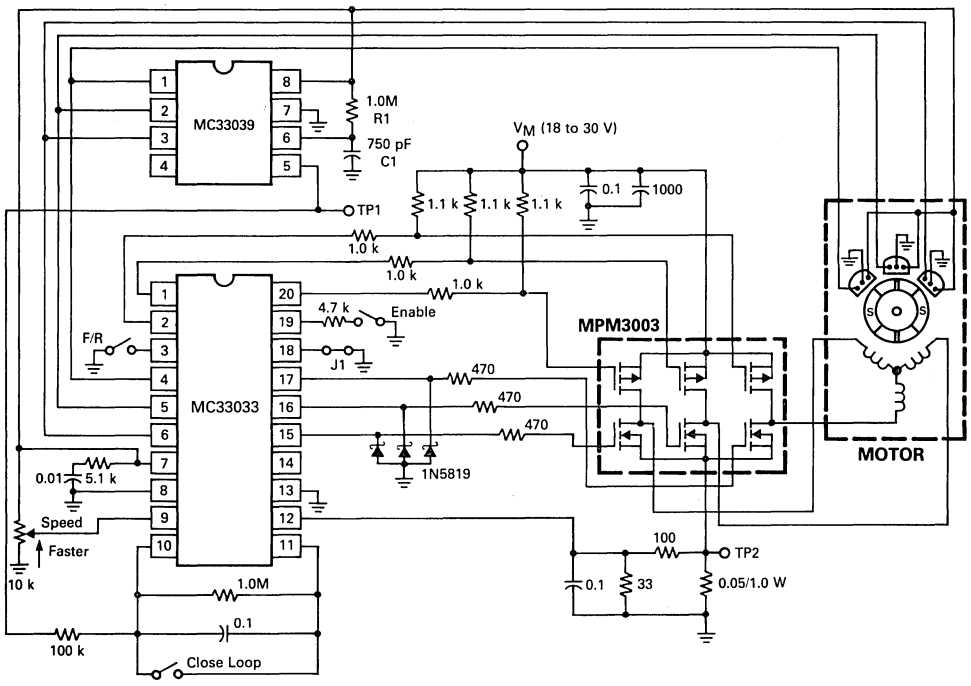


Three Phase Closed Loop Controller

The MC33033, by itself, is capable of open loop motor speed control. For closed loop speed control, the MC33033 requires an input voltage proportional to the motor speed. Traditionally this has been accomplished by means of a tachometer to generate the motor speed feedback voltage. Figure 37 shows an application whereby an MC33039, powered from the 6.25 volt reference (Pin 7) of the MC33033, is used to generate the required feedback voltage without the need of a costly tachometer. The same Hall sensor signals used by the MC33033 for rotor position decoding are utilized by the MC33039. Every positive or negative going transition of the Hall sensor signals on any of the sensor lines causes the MC33039 to produce an output pulse of defined amplitude and time duration, as determined by the external resistor R1 and capacitor C1. The resulting output train of pulses present at Pin 5 of the MC33039 are integrated by the error amplifier of the MC33033 configured as an integrator, to produce a DC voltage level which is proportional to the motor speed. This speed proportional voltage establishes the PWM reference level at Pin 11 of the MC33033 motor controller and completes or closes the feedback loop. The MC33033 outputs drive an MPM3003 TMOS power MOSFET 3-phase bridge circuit which is capable of delivering up to 25 Amperes of surge current. High current can be expected during conditions of start-up and when changing direction of the motor.

The system shown in Figure 37 is designed for a motor having 120/240 degrees Hall sensor electrical phasing. The system can easily be modified to accommodate 60/300 degree Hall sensor electrical phasing by removing the jumper (J1) at Pin 18 of the MC33033.

FIGURE 37 — CLOSED LOOP BRUSHLESS DC MOTOR CONTROL WITH THE MC33033 USING THE MC33039 AND MC3003



4

Sensor Phasing Comparison

There are four conventions used to establish the relative phasing of the sensor signals in three phase motors. With six step drive, an input signal change must occur every 60 electrical degrees, however, the relative signal phasing is dependent upon the mechanical sensor placement. A comparison of the conventions in electrical degrees is shown in Figure 38. From the sensor phasing table (Figure 39), note that the order of input codes for 60° phasing is the reverse of 300°. This means the MC33033, when the 60°/120° select (Pin 18) and the FWD/REV (Pin 3) both in the high state (open), is configured to operate a 60° sensor phasing motor in the forward direction. Under the same conditions a 300° sensor phasing motor would operate equally well but in the reverse direction. One would simply have to reverse the FWD/REV switch (FWD/REV closed) in order to cause the 300° motor to also operate in the same direction. The same difference exists between the 120° and 240° conventions.

FIGURE 38 — SENSOR PHASING COMPARISON

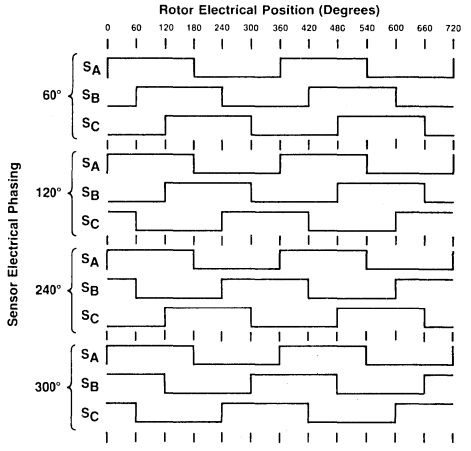


FIGURE 39 — SENSOR PHASING TABLE

Sensor Electrical Phasing (Degrees)												
60°			120°			240°			300°			
S_A	S_B	S_C	S_A	S_B	S_C	S_A	S_B	S_C	S_A	S_B	S_C	
1	0	0	1	0	1	1	1	0	1	1	1	
1	1	0	1	0	0	1	0	0	1	1	0	
1	1	1	1	1	0	1	0	1	1	0	0	
0	1	1	0	1	0	0	0	1	0	0	0	
0	0	1	0	1	1	0	1	1	0	0	1	
0	0	0	0	0	1	0	1	0	0	1	1	

In this data sheet, the rotor position has always been given in electrical degrees since the mechanical position is a function of the number of rotating magnetic poles. The relationship between the electrical and mechanical position is:

$$\text{Electrical Degrees} = \text{Mechanical Degrees}\left(\frac{\#\text{Rotor Poles}}{2}\right)$$

An increase in the number of magnetic poles causes more electrical revolutions for a given mechanical revolution. General purpose three phase motors typically contain a four pole rotor which yields two electrical revolutions for one mechanical.

Two and Four Phase Motor Commutation

The MC33033 configured for 60° sensor inputs is capable of providing a four step output that can be used to drive two or four phase motors. The truth table in Figure 40 shows that by connecting sensor inputs S_B and S_C together, it is possible to truncate the number of drive output states from six to four. The output power switches are connected to B_T, C_T, B_B, and C_B. Figure 41 shows a four phase, four step, full wave motor control application. Power switch transistors Q1 through Q8 are Darlington type, each with an internal parasitic catch diode. With four step drive, only two rotor position sensors spaced at 90 electrical degrees are required. The commutation waveforms are shown in Figure 42.

Figure 43 shows a four phase, four step, half wave motor controller. It has the same features as the circuit in Figure 36, except for the deletion of speed adjust.

FIGURE 40 — TWO AND FOUR PHASE, FOUR STEP, COMMUTATION TRUTH TABLE

MC33033 (60°/$\overline{120°}$ Select Pin Open)						
Inputs			Outputs			
Sensor Electrical Spacing* = 90°			Top Drives		Bottom Drives	
S_A	S_B	F/R	B_T	C_T	B_B	C_B
1	0	1	1	1	0	1
1	1	1	0	1	0	0
0	1	1	1	0	0	0
0	0	1	1	1	1	0
1	0	0	1	0	0	0
1	1	0	1	1	1	0
0	1	0	1	1	0	1
0	0	0	0	1	0	0

*With MC33033 sensor input S_B connected to S_C

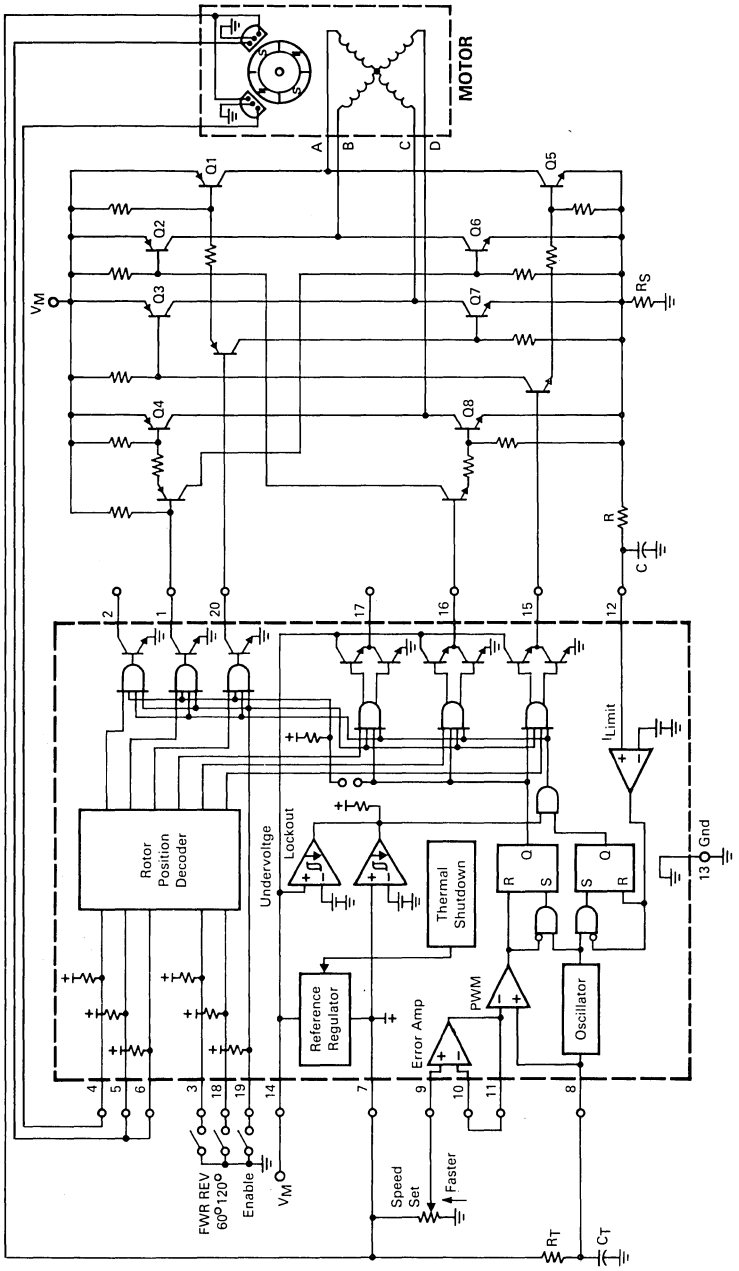
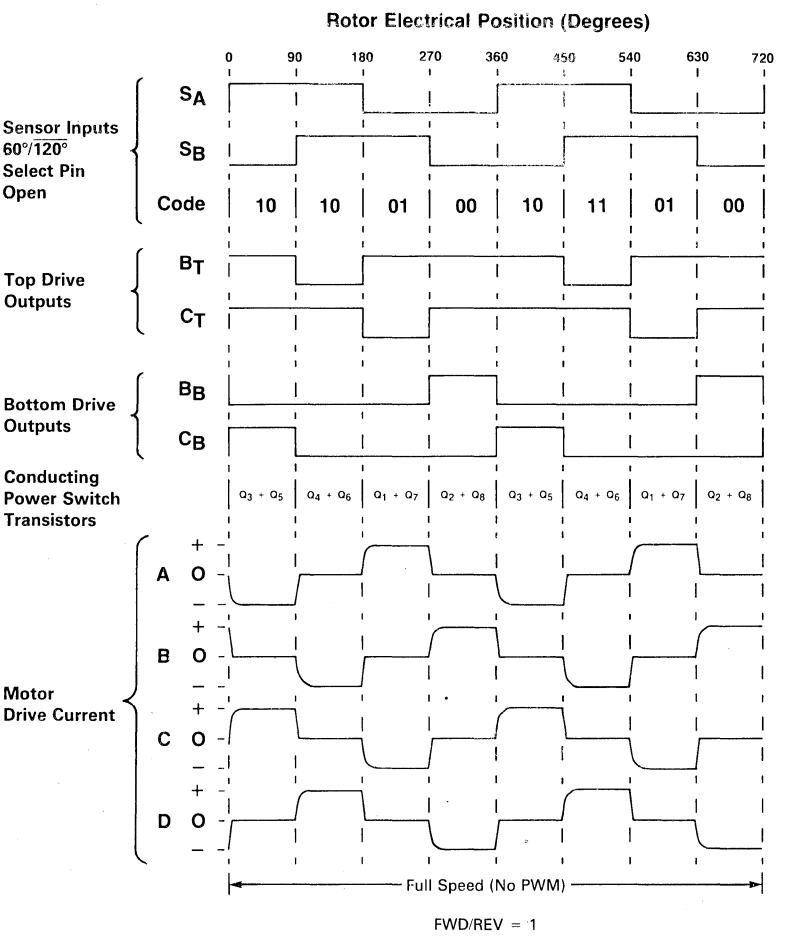


FIGURE 41 — FOUR PHASE, FOUR STEP, FULL WAVE CONTROLLER

FIGURE 42 — FOUR PHASE, FOUR STEP, FULL WAVE COMMUTATION WAVEFORMS



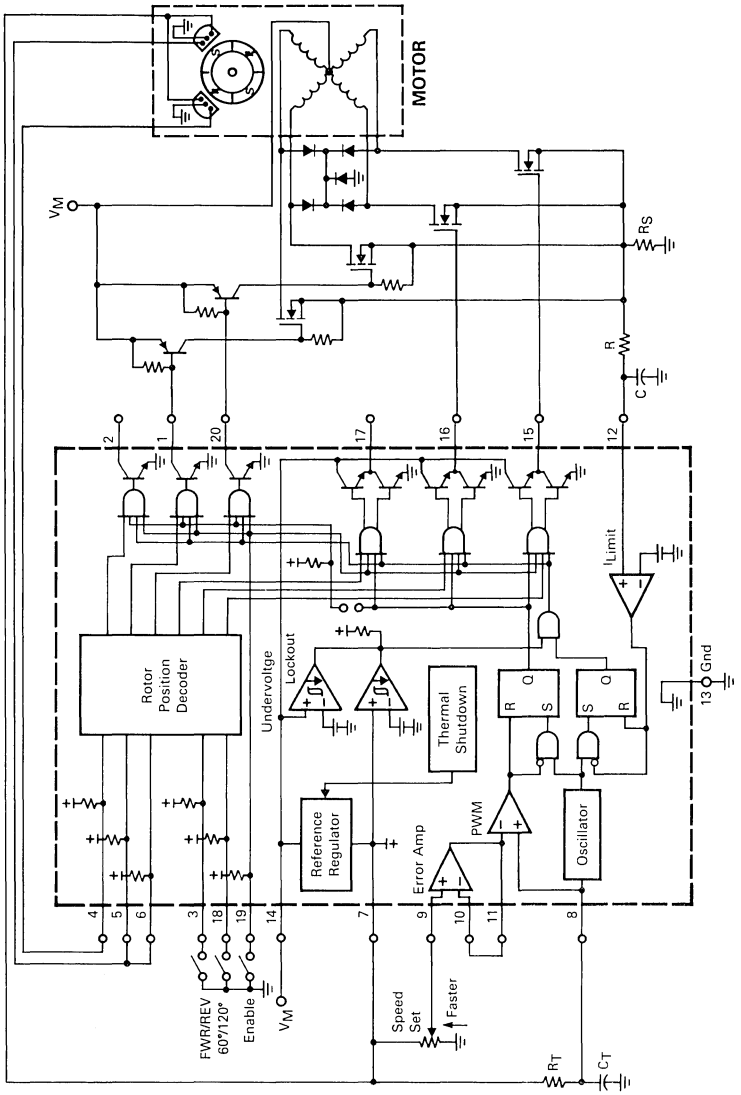


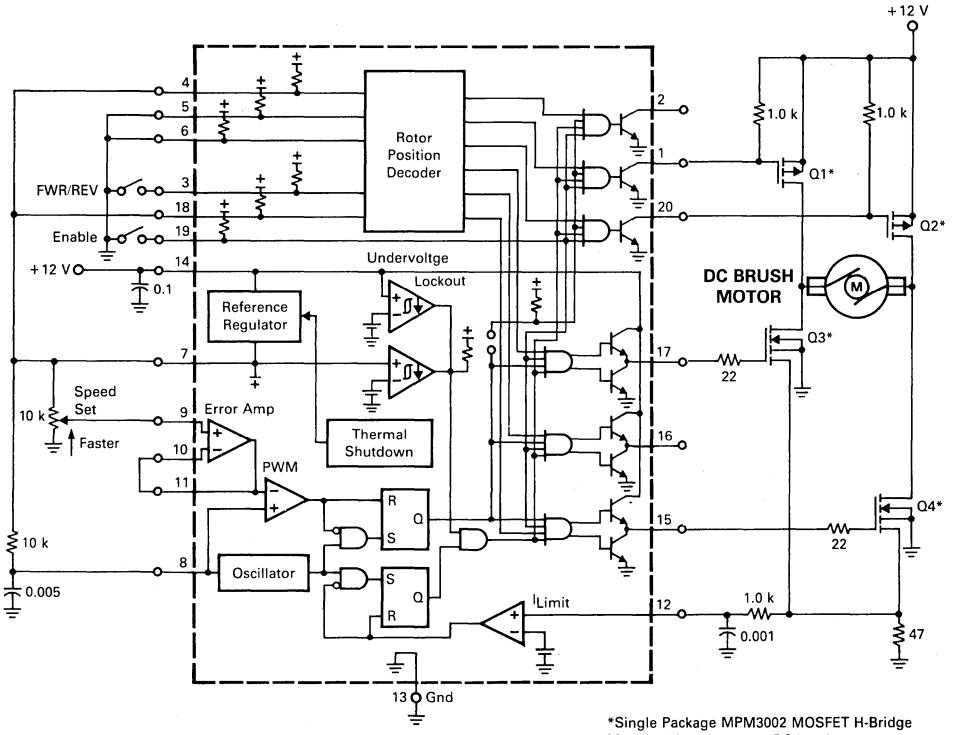
FIGURE 43 — FOUR PHASE, FOUR STEP, HALF WAVE MOTOR CONTROLLER

Brush Motor Control

Though the MC33033 was designed to control brushless DC motors, it may also be used to control DC brush-type motors. Figure 44 shows an application of the MC33033 driving a Motorola MPM3002 H-bridge affording minimal parts count to operate a one-tenth horsepower brush-type motor. Key to the operation is the input sensor code [100] which produces a top-left (Q1) and a bottom-right (Q4) drive when the controller's forward/reverse pin is at logic [1]; top-right (Q2), bottom-left (Q3) drive is realized when the forward/reverse pin is at logic [0]. This code supports the requirements necessary for H-bridge drive accomplishing both direction and speed control.

The controller functions in a normal manner with a pulse-width-modulated frequency of approximately 25 kHz. Motor speed is controlled by adjusting the voltage presented to the non-inverting input of the error amplifier establishing the PWM's slice or reference level. Cycle-by-cycle current limiting of 3.0 amperes motor current is accomplished by sensing the voltage (100 mV threshold) across the 47 Ohm resistor to ground of the H-bridge motor current. The over current sense circuit makes it possible to reverse the direction of the motor, on the fly, using the normal forward/reverse switch, and not have to completely stop before reversing.

FIGURE 44 — H-BRIDGE BRUSH-TYPE CONTROLLER



*Single Package MPM3002 MOSFET H-Bridge
M = 1/10th horsepower DC brush-type motor

LAYOUT CONSIDERATIONS

Do not attempt to construct any of the motor control circuits on wire-wrap or plug-in prototype boards. High frequency printed circuit layout techniques are imperative to prevent pulse jitter. This is usually caused by excessive noise pick-up imposed on the current sense or error amp inputs. The printed circuit layout should contain a ground plane with low current signal and high drive and output buffer grounds returning on separate paths back to the power supply input filter capacitor V_M. Ceramic bypass capacitors (0.01 μF) connected close to the integrated circuit at V_{CC}, V_{ref} and error amplifliier non-inverting input may be required depending upon circuit layout. This provides a low impedance path for filtering any high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC33035

Advance Information

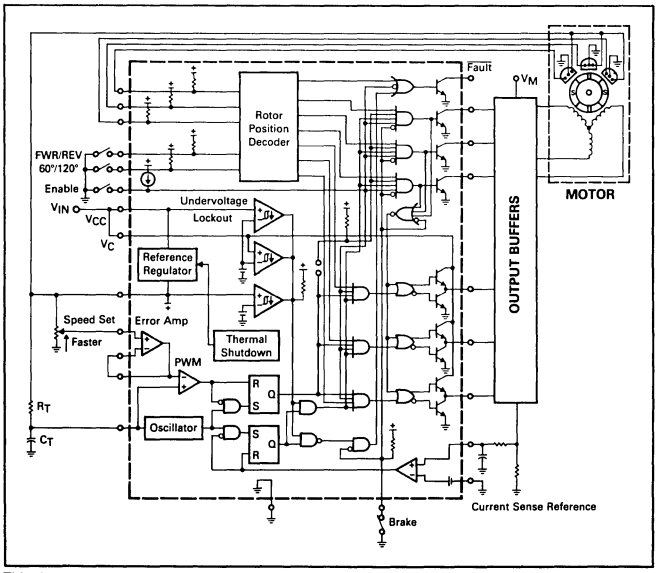
BRUSHLESS DC MOTOR CONTROLLER

The MC33035 is a high performance second generation monolithic brushless DC motor controller containing all of the active functions required to implement a full featured open-loop, three or four phase motor control system. This device consists of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, fully accessible error amplifier, pulse width modulator comparator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs.

Also included are protective features consisting of undervoltage lockout, cycle-by-cycle current limiting with a selectable time delayed latched shutdown mode, internal thermal shutdown, and a unique fault output that can be interfaced into microprocessor controlled systems.

Typical motor control functions include open-loop speed, forward or reverse direction, run enable, and dynamic braking. The MC33035 is designed to operate with electrical sensor phasings of 60°/300° or 120°/240°, and can also efficiently control brush DC motors.

- 10 V to 30 V Operation
- Undervoltage Lockout
- 6.25 V Reference Capable of Supplying Sensor Power
- Fully Accessible Error Amplifier for Closed-Loop Servo Applications
- High Current Drivers can Control MPM3003 MOSFET 3-Phase Bridge
- Cycle-By-Cycle Current Limiting
- Pinned-Out Current Sense Reference
- Internal Thermal Shutdown
- Selectable 60°/300° or 120°/240° Sensor Phasings
- Can Efficiently Control Brush DC Motors with MPM3002 MOSFET H-Bridge

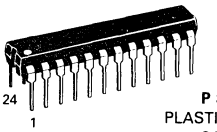


This document contains information on a new product. Specifications and information herein are subject to change without notice.

BRUSHLESS DC MOTOR CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

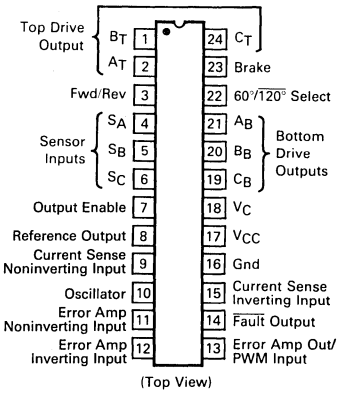
4



P SUFFIX
PLASTIC PACKAGE
CASE 724

DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO-24L)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Ambient Temperature Range	Package
MC33035P	−40°C to +85°C	Plastic DIP
MC33035DW	−40°C to +85°C	SO-24L

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Digital Inputs (Pins 3, 4, 5, 6, 22, 23)	—	V_{ref}	V
Oscillator Input Current (Source or Sink)	I_{OSC}	30	mA
Error Amp Input Voltage Range (Pins 11, 12, Note 1)	V_{IR}	−3.0 to V	V
Error Amp Output Current (Source or Sink, Note 2)	I_{Out}	10	mA
Current Sense Input Voltage Range (Pins 9, 15)	V_{Sense}	−0.3 to 5.0	V
$\overline{\text{Fault}}$ Output Voltage	$V_{CE(\overline{Fault})}$	20	V
$\overline{\text{Fault}}$ Output Sink Current	$I_{Sink(\overline{Fault})}$	20	mA
Top Drive Voltage (Pins 1, 2, 24)	$V_{CE(top)}$	40	V
Top Drive Sink Current (Pins 1, 2, 24)	$I_{Sink(Top)}$	50	mA
Bottom Drive Supply Voltage (Pin 18)	V_C	30	V
Bottom Drive Output Current (Source or Sink, Pins 19, 20, 21)	I_{DRV}	100	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 85°C	P_D	867	mW
Thermal Resistance, Junction to Air	$R_{\theta JA}$	75	°C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = V_C = 20 V, R_T = 4.7 k, C_T = 10 nF, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_{ref} = 1.0 mA)	V_{ref}				V
T_A = 25°C		5.9	6.24	6.5	
T_A = −40°C to +85°C		5.82	—	6.57	
Line Regulation (V_{CC} = 10 V to 30 V, I_{ref} = 1.0 mA)	Reg_{line}	—	1.5	30	mV
Load Regulation (I_{ref} = 1.0 mA to 20 mA)	Reg_{load}	—	16	30	mV
Output Short Circuit Current (Note 3)	I_{SC}	40	75	—	mA
Reference Under Voltage Lockout Threshold	V_{th}	4.0	4.5	5.0	V
ERROR AMPLIFIER					
Input Offset Voltage (T_A = −40°C to +85°C)	V_{IO}	—	0.4	10	mV
Input Offset Current (T_A = −40°C to +85°C)	I_{IO}	—	8.0	500	nA
Input Bias Current (T_A = −40°C to +85°C)	I_{IB}	—	−46	−1000	nA
Input Common Mode Voltage Range	V_{ICR}		(0 V to V_{ref})		V
Open-Loop Voltage Gain (V_O = 3.0 V, R_L = 15 k)	A_{VOL}	70	80	—	dB
Input Common Mode Rejection Ratio	CMRR	55	86	—	dB
Power Supply Rejection Ratio (V_{CC} = V_C = 10 V to 30 V)	PSRR	65	105	—	dB
Output Voltage Swing					V
High State (R_L = 15 k to Ground)	V_{OH}	4.6	5.3	—	
Low State (R_L = 15 k to V_{ref})	V_{OL}	—	0.5	1.0	

NOTES:
1. The input common mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V.
2. The compliance voltage must not exceed the range of −0.3 to V_{ref}.
3. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = V_C = 20 V, R_T = 4.7 k, C_T = 10 nF, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR SECTION					
Oscillator Frequency	f_{OSC}	22	25	28	kHz
Frequency Change with Voltage (V_{CC} = 10 V to 30 V)	$\Delta f_{OSC}/\Delta V$	—	0.01	5.0	%
Sawtooth Peak Voltage	$V_{OSC(P)}$	—	4.1	4.5	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	1.2	1.5	—	V
LOGIC INPUTS					
Input Threshold Voltage (Pins 3, 4, 5, 6, 7, 22, 23) High State Low State	 V_{IH} V_{IL}	 3.0 —	 2.2 1.7	 — 0.8	V
Sensor Inputs (Pins 4, 5, 6) High State Input Current (V_{IH} = 5.0 V) Low State Input Current (V_{IL} = 0 V)	 I_{IH} I_{IL}	 −150 −600	 −70 −337	 −20 −150	μA
Forward/Reverse and 60°/120° Select (Pins 3, 22, 23) High State Input Current (V_{IH} = 5.0 V) Low State Input Current (V_{IL} = 0 V)	 I_{IH} I_{IL}	 −75 −300	 −36 −175	 −10 −75	μA
Output Enable High State Input Current (V_{IH} = 5.0 V) Low State Input Current (V_{IL} = 0 V)	 I_{IH} I_{IL}	 −60 −60	 −29 −29	 −10 −10	μA
CURRENT-LIMIT COMPARATOR					
Threshold Voltage	V_{th}	85	101	115	mV
Input Common Mode Voltage Range	V_{ICR}	—	3.0	—	V
Input Bias Current	I_{IB}	—	−0.9	−5.0	μA
OUTPUTS AND POWER SECTIONS					
To Drive Output Sink Saturation (I_{sink} = 25 mA)	$V_{CE(sat)}$	—	0.5	1.5	V
Top Drive Output Off-State Leakage (V_{CE} = 30 V)	$I_{DRV(leak)}$	—	0.06	100	μA
Top Drive Output Switching Time (C_L = 47 pF, R_L = 1.0 k) Rise Time Fall Time	 t_r t_f	 — —	 107 26	 300 300	ns
Bottom Drive Output Voltage High State (V_{CC} = 20 V, V_C = 30 V, I_{source} = 50 mA) Low State (V_{CC} = 20 V, V_C = 30 V, I_{sink} = 50 mA)	 V_{OH} V_{OL}	 (V_{CC} − 2.0) —	 (V_{CC} − 1.1) 1.5	 — 2.0	V
Bottom Drive Output Switching Time (C_L = 1000 pF) Rise Time Fall Time	 t_r t_f	 — —	 38 30	 200 200	ns
$\overline{\text{Fault}}$ Output Sink Saturation (I_{sink} = 16 mA)	$V_{CE(sat)}$	—	225	500	mV
$\overline{\text{Fault}}$ Output Off-State Leakage (V_{CE} = 20 V)	$I_{FLT(leak)}$	—	1.0	100	μA
Under Voltage Lockout Drive Output Enabled (V_{CC} or V_C Increasing) Hysteresis	 $V_{th(on)}$ V_H	 8.2 0.1	 8.9 0.2	 10 0.3	V
Power Supply Current Pin 17 (V_{CC} = V_C = 20 V) Pin 17 (V_{CC} = 20 V, V_C = 30 V) Pin 18 (V_{CC} = V_C = 20 V) Pin 18 (V_{CC} = 20 V, V_C = 30 V)	 I_{CC} I_C 	 — — — —	 12 14 3.5 5.0	 16 20 6.0 10	mA

FIGURE 1 — OSCILLATOR FREQUENCY versus TIMING RESISTOR

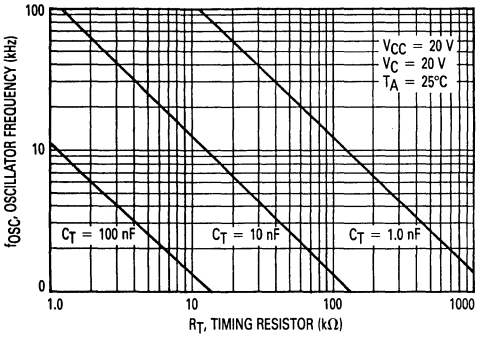


FIGURE 2 — OSCILLATOR FREQUENCY CHANGE versus TEMPERATURE

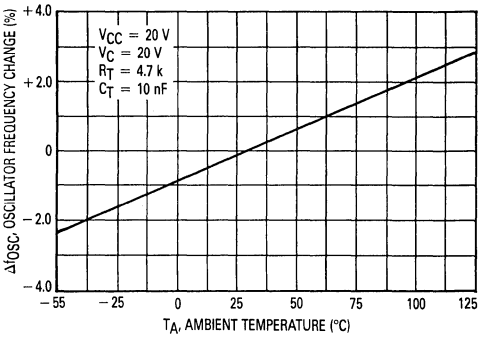


FIGURE 3 — ERROR AMP OPEN LOOP GAIN AND PHASE versus FREQUENCY

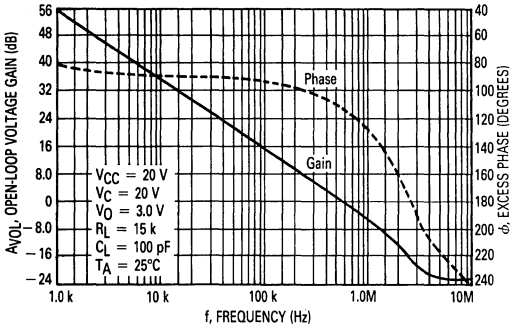


FIGURE 4 — ERROR AMP OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

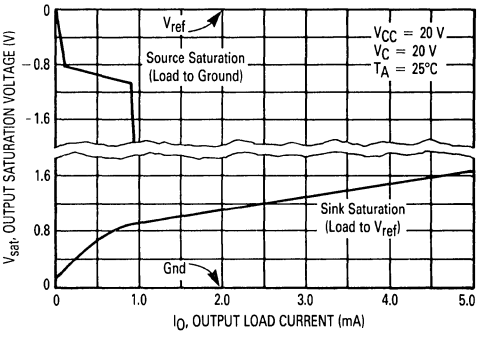


FIGURE 5 — ERROR AMP SMALL-SIGNAL TRANSIENT RESPONSE

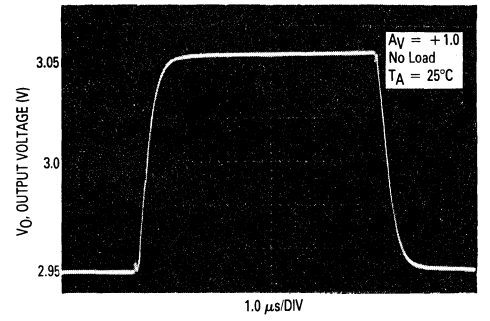


FIGURE 6 — ERROR AMP LARGE-SIGNAL TRANSIENT RESPONSE

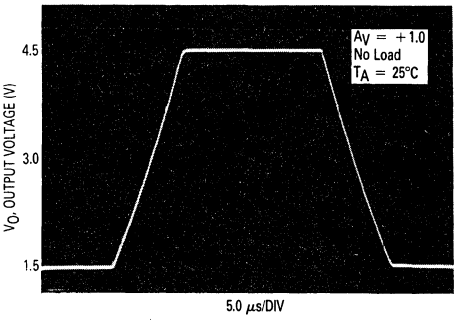


FIGURE 7 — REFERENCE OUTPUT VOLTAGE CHANGE versus OUTPUT SOURCE CURRENT

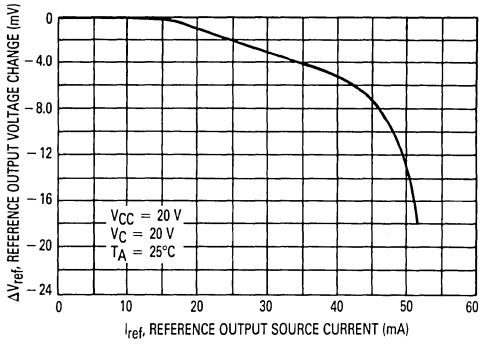


FIGURE 8 — REFERENCE OUTPUT VOLTAGE versus SUPPLY VOLTAGE

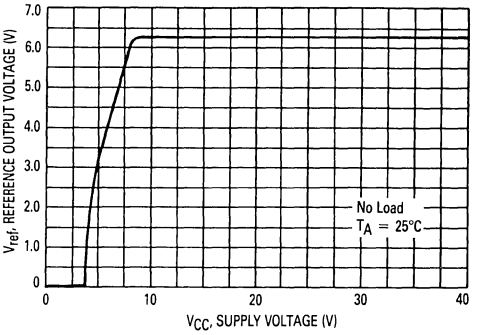


FIGURE 9 — REFERENCE OUTPUT VOLTAGE versus TEMPERATURE

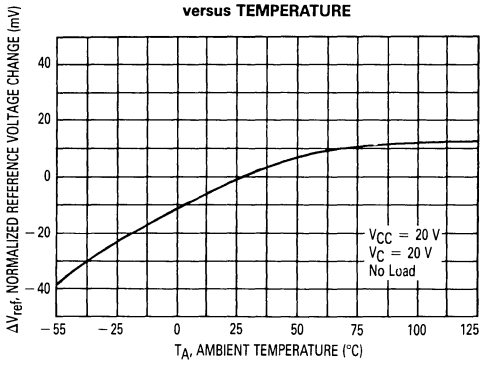


FIGURE 10 — OUTPUT DUTY CYCLE versus PWM INPUT VOLTAGE

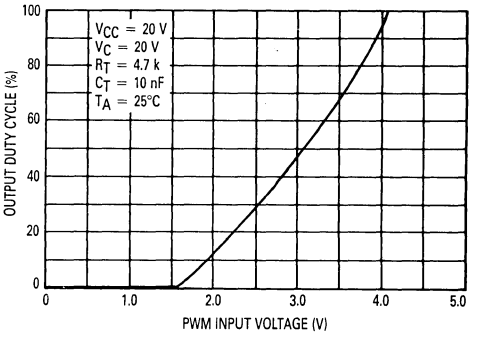


FIGURE 11 — BOTTOM DRIVE RESPONSE TIME versus CURRENT SENSE INPUT VOLTAGE

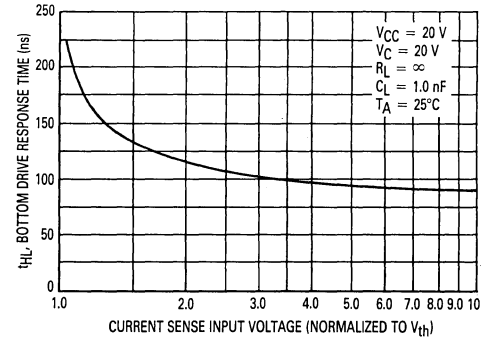


FIGURE 12 — $\overline{\text{FAULT}}$ OUTPUT SATURATION versus SINK CURRENT

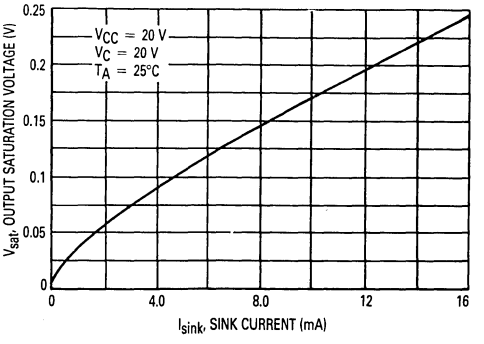


FIGURE 13 — TOP DRIVE OUTPUT SATURATION VOLTAGE versus SINK CURRENT

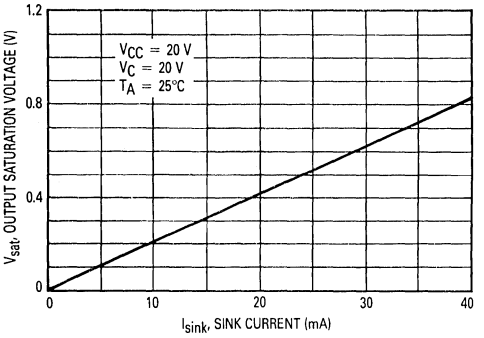


FIGURE 14 — TOP DRIVE OUTPUT WAVEFORM

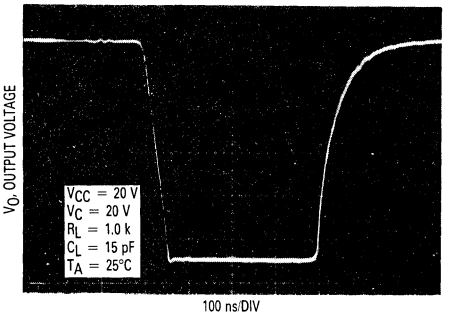


FIGURE 15 — BOTTOM DRIVE OUTPUT WAVEFORM

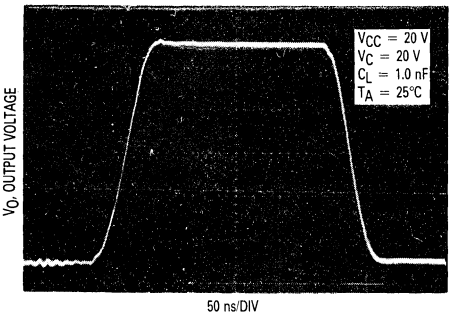


FIGURE 16 — BOTTOM DRIVE OUTPUT WAVEFORM

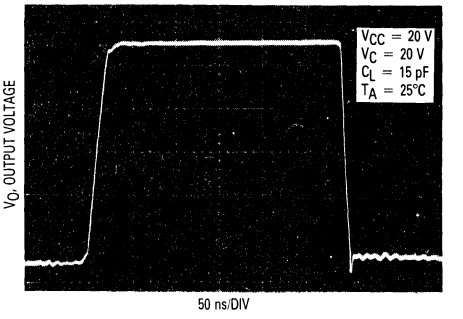


FIGURE 17 — BOTTOM DRIVE OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

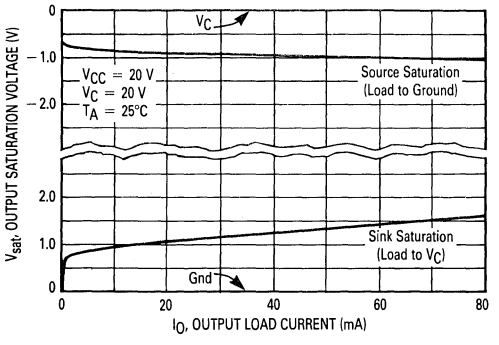
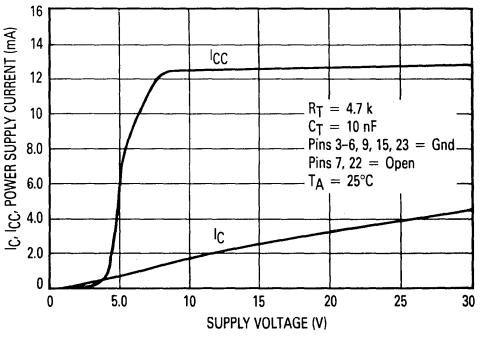


FIGURE 18 — POWER AND BOTTOM DRIVE SUPPLY CURRENT versus SUPPLY VOLTAGE



PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1, 2, 24	B_T, A_T, C_T	These three open collector Top Drive Outputs are designed to drive the external upper power switch transistors.
3	FWD/REV	The Forward/Reverse Input is used to change the direction of motor rotation.
4, 5, 6	S_A, S_B, S_C	These three Sensor Inputs control the commutation sequence.
7	Output Enable	A logic high at this input causes the motor to run, while a low causes it to coast.
8	Reference Output	This output provides charging current for the oscillator timing capacitor C_T and a reference for the error amplifier. It may also serve to furnish sensor power.
9	Current Sense (Noninverting Input)	A 100 mV signal, with respect to pin 15, at this input terminates output switch conduction during a given oscillator cycle. This pin normally connects to the top side of the current sense resistor.
10	Oscillator	The Oscillator frequency is programmed by the values selected for the timing components, R_T and C_T.
11	Error Amp (Noninverting Input)	This input is normally connected to the speed set potentiometer.
12	Error Amp (Inverting Input)	This input is normally connected to the Error Amp Output in open-loop applications.
13	Error Amp Output/PWM Input	This pin is available for compensation in closed-loop applications.
14	$\overline{\text{Fault}}$ Output	This open collector output is active low during one or more of the following conditions: Invalid Sensor Input code, Enable Input at logic 0, Current Sense Input greater than 100 mV (pin 9 with respect to pin 15), Undervoltage Lockout activation, and Thermal Shutdown.
15	Current Sense (Inverting Input)	Reference pin for internal 100 mV threshold. This pin is normally connected to the bottom side of the current sense resistor.
16	Ground	This pin supplies a ground for the control circuit and should be referenced back to the power source ground.
17	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a minimum V_{CC} range of 10 V to 30 V.
18	V_C	The high state (V_{OH}) of the Bottom Drive Outputs is set by the voltage applied to this pin. The controller is operational over a minimum V_C range of 10 V to 30 V.
19, 20, 21	C_B, B_B, A_B	These three totem pole Bottom Drive Outputs are designed for direct drive of the external bottom power switch transistors.
22	60°/$\overline{120°}$ Select	The electrical state of this pin configures the control circuit operation for either 60° (high state) or 120° (low state) sensor electrical phasing inputs.
23	Brake Input	A logic low state at this input allows the motor to run, while a high state does not allow motor operation and if operating causes rapid deceleration.

INTRODUCTION

The MC33035 is one of a series of high performance monolithic DC brushless motor controllers produced by Motorola. It contains all of the functions required to implement a full-featured, open-loop, three or four phase motor control system. In addition, the controller can be made to operate DC brush motors. Constructed with Bipolar Analog technology, it offers a high degree of performance and ruggedness in hostile industrial environments. The MC33035 contains a rotor position decoder for proper commutation sequencing, a temperature compensated reference capable of supplying a sensor power, a frequency programmable sawtooth oscillator, a fully accessible error amplifier, a pulse width modulator comparator, three open collector top drive outputs, and three high current totem pole bottom driver outputs ideally suited for driving power MOSFETs.

Included in the MC33035 are protective features consisting of undervoltage lockout, cycle by cycle current limiting with a selectable time delayed latched shutdown mode, internal thermal shutdown, and a unique fault output that can easily be interfaced to a microprocessor controller.

Typical motor control functions include open-loop speed control, forward or reverse rotation, run enable, and dynamic braking. In addition, the MC33035 has a 60°/$\overline{120°}$ select pin which configures the rotor position decoder for either 60° or 120° sensor electrical phasing inputs.

FUNCTIONAL DESCRIPTION

A representative internal block diagram is shown in Figure 19 with various applications shown in Figures 36, 38, 42, 44, 45, and 46. A discussion of the features and function of each of the internal blocks given below is referenced to Figures 19 and 36.

Rotor Position Decoder

An internal rotor position decoder monitors the three sensor inputs (Pins 4, 5, 6) to provide the proper sequencing of the top and bottom drive outputs. The sensor inputs are designed to interface directly with open collector type Hall Effect switches or opto slotted couplers. Internal pull-up resistors are included to minimize the required number of external components. The inputs are TTL compatible, with their thresholds typically at 2.2 volts. The MC33035 series is designed to control three phase motors and operate with four of the most common conventions of sensor phasing. A 60°/$\overline{120°}$ select (Pin 22) is conveniently provided which affords the MC33035 to configure itself to control motors having either 60°, 120°, 240° or 300° electrical sensor phasing. With three sensor inputs there are eight possible input code combinations, six of which are valid rotor positions. The remaining two codes are invalid and are usually caused by an open or shorted sensor line. When an invalid input condition exists, the $\overline{\text{Fault}}$ output is activated and the drive outputs are disabled. With six valid input codes, the decoder can resolve the motor rotor position to within a window of 60 electrical degrees.

The forward/reverse input (Pin 3) is used to change the direction of motor rotation by reversing the voltage across the stator winding. When the input changes state, from high to low with a given sensor input code (for example 100), the enabled top and bottom drive outputs with the same alpha designation are exchanged (A_T to A_B, B_T to B_B, C_T to C_B). In effect the commutation sequence is reversed and the motor changes directional rotation.

Motor on/off control is accomplished by the output enable (Pin 7). When left disconnected, an internal 25 μA current source enables sequencing of the top and bottom drive outputs. When grounded, the top drive outputs turn off and the bottom drives are forced low, causing the motor to coast and the $\overline{\text{Fault}}$ output to activate.

Dynamic motor braking allows an additional margin of safety to be designed into the final product. Braking is accomplished by placing the brake input (Pin 23) in a high state. This causes the top drive outputs to turn off and the bottom drives to turn on, shorting the motor-generated back EMF. The brake input has unconditional priority over all other inputs. The internal 40 kΩ pull-up resistor simplifies interfacing with the system safety-switch by insuring brake activation if opened or disconnected. The commutation logic truth table is shown in Figure 20. A four input NOR gate is used to monitor the brake input and the inputs to the three top drive output transistors. Its purpose is to disable braking until the top drive outputs attain a high state. This helps to prevent simultaneous conduction of the top and bottom power switches. In half wave motor drive applications, the top drive outputs are not required and are normally left disconnected. Under these conditions braking will still be accomplished since the NOR gate senses the base voltage to the top drive output transistors.

Error Amplifier

A high performance, fully compensated error amplifier with access to both inputs and output (Pins 11, 12, 13) is provided to facilitate the implementation of closed-loop motor speed control. The amplifier features a typical DC voltage gain of 80 dB, 0.6 MHz gain bandwidth, and a wide input common mode voltage range that extends from ground to V_{ref}. In most open-loop speed control applications, the amplifier is configured as a unity gain voltage follower with the non-inverting input connected to the speed set voltage source. Additional configurations are shown in Figures 31 through 35.

Oscillator

The frequency of the internal ramp oscillator is programmed by the values selected for timing components R_T and C_T. Capacitor C_T is charged from the reference output (Pin 8) through resistor R_T and discharged by an internal discharge transistor. The ramp peak and valley voltages are typically 4.1 V and 1.5 V respectively. To provide a good compromise between audible noise and output switching efficiency, an oscillator frequency in the range of 20 kHz to 30 kHz is recommended. Refer to Figure 1 for component selection.

FIGURE 19 — REPRESENTATIVE BLOCK DIAGRAM

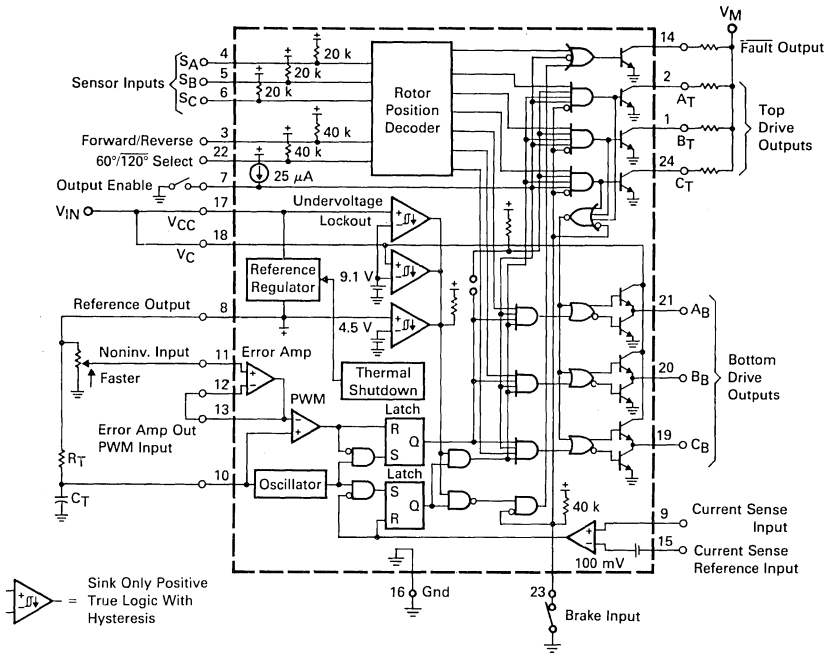


FIGURE 20 — THREE PHASE, SIX STEP COMMUTATION TRUTH TABLE (Note 1)

Inputs (Note 2)										Outputs (Note 3)							
Sensor Electrical Phasing (Note 4)										Top Drives			Bottom Drives				
60°			120°						Current								
S_A	S_B	S_C	S_A	S_B	S_C	F/R	Enable	Brake	Sense	A_T	B_T	C_T	A_B	B_B	C_B	Fault	
1	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1	1	(Note 5)
1	1	0	1	1	0	1	1	0	0	1	0	1	0	0	1	1	F/R = 1
1	1	1	0	1	0	1	1	0	0	1	0	1	1	0	0	1	
0	1	1	0	1	1	1	1	0	0	1	1	0	1	0	0	1	
0	0	1	0	0	1	1	1	0	0	1	1	0	0	1	0	1	
0	0	0	1	0	1	1	1	0	0	0	1	1	0	1	0	1	
1	0	0	1	0	0	0	1	0	0	1	1	0	1	0	0	1	(Note 5)
1	1	0	1	1	0	0	1	0	0	1	1	0	0	1	0	1	F/R = 0
1	1	1	0	1	0	0	1	0	0	0	1	1	0	1	0	1	
0	1	1	0	1	1	0	1	0	0	0	1	1	0	0	1	1	
0	0	1	0	0	1	0	1	0	0	1	0	1	0	0	1	1	
0	0	0	1	0	1	0	1	0	0	1	0	1	1	0	0	1	
1	0	1	1	1	1	X	X	0	X	1	1	1	0	0	0	0	(Note 6)
0	1	0	0	0	0	X	X	0	X	1	1	1	0	0	0	0	Brake = 0
1	0	1	1	1	1	X	X	1	X	1	1	1	1	1	1	0	(Note 7)
0	1	0	0	0	0	X	X	1	X	1	1	1	1	1	1	0	Brake = 1
V	V	V	V	V	V	X	1	1	X	1	1	1	1	1	1	1	(Note 8)
V	V	V	V	V	V	X	0	1	X	1	1	1	1	1	1	0	(Note 9)
V	V	V	V	V	V	X	0	0	X	1	1	1	0	0	0	0	(Note 10)
V	V	V	V	V	V	X	1	0	1	1	1	1	0	0	0	0	(Note 11)

NOTES:
1. V = Any one of six valid sensor or drive combinations.
   X = Don't care.
2. The digital inputs (Pins 3, 4, 5, 6, 7, 22, 23) are all TTL compatible. The current sense input (Pin 9) has a 100 mV threshold with respect to Pin 15. A logic 0 for this input is defined as < 85 mV, and a logic 1 is > 115 mV.
3. The fault and top drive outputs are open collector design and active in the low (0) state.
4. With 60°/120° select (Pin 22) in the high (1) state, configuration is for 60° sensor electrical phasing inputs. With Pin 22 in low (0) state, configuration is for 120° sensor electrical phasing inputs.
5. Valid 60° or 120° sensor combinations for corresponding valid top and bottom drive outputs.
6. Invalid sensor inputs with brake = 0; All top and bottom drives off, Fault low.
7. Invalid sensor inputs with brake = 1; All top drives off, all bottom drives on, Fault low.
8. Valid 60° or 120° sensor inputs with brake = 1; All top drives off, all bottom drives on, Fault high.
9. Valid sensor inputs with brake = 1 and enable = 0; All top drives off, all bottom drives on, Fault low.
10. Valid sensor inputs with brake = 0 and enable = 0; All top and bottom drives off, Fault low.
11. All bottom drives off, Fault low.

Pulse Width Modulator

The use of pulse width modulation provides an energy efficient method of controlling the motor speed by varying the average voltage applied to each stator winding during the commutation sequence. As C_T discharges, the oscillator sets both latches, allowing conduction of the top and bottom drive outputs. The PWM comparator resets the upper latch, terminating the bottom drive output conduction when the positive-going ramp of C_T becomes greater than the error amplifier output. The pulse width modulator timing diagram is shown in Figure 21. Pulse width modulation for speed control appears only at the bottom drive outputs.

Current Limit

Continuous operation of a motor that is severely overloaded results in overheating and eventual failure. This destructive condition can best be prevented with the use of cycle-by-cycle current limiting. That is, each on-cycle is treated as a separate event. Cycle-by-cycle current limiting is accomplished by monitoring the stator current build-up each time an output switch conducts, and upon sensing an over current condition, immediately turning off the switch and holding it off for the remaining duration of the oscillator ramp-up period. The stator current is converted to a voltage by inserting a ground-referenced sense resistor R_S (Figure 36) in series with the three bottom switch transistors (Q_4, Q_5, Q_6). The voltage across the sense resistor is directly monitored by the current sense comparator inputs (Pins 9 and 15) and compared to the internal 100 mV reference. The current sense comparator inputs have an input common mode input range of approximately 3.0 volts. If the 100 mV current sense threshold is exceeded, the comparator resets the lower sense latch and terminates output switch conduction. The value for the current sense resistor is:

$$R_S = \frac{0.1}{I_{stator(max)}}$$

The $\overline{Fault}$ output activates during an over current condition. The dual-latch PWM configuration ensures that only one single output conduction pulse occurs during any given oscillator cycle, whether terminated by the output of the error amp or the current limit comparator.

Reference

The on-chip 6.25 V regulator (Pin 8) provides charging current for the oscillator timing capacitor, a reference for the error amplifier, and can supply 20 mA of current suitable for directly powering sensors in low voltage applications. In higher voltage applications it may become necessary to transfer the power dissipated by the regulator off the IC. This is easily accomplished with the addition of an external pass transistor as shown in Figure 22. A 6.25 V reference level was chosen to allow implementation of the simpler NPN circuit, where $V_{ref} - V_{BE}$ exceeds the minimum voltage required by Hall Effect sensors over temperature. With proper transistor selection, and adequate heatsinking, up to one amp of load current can be obtained.

FIGURE 22 — REFERENCE OUTPUT BUFFERS

The NPN circuit is recommended for powering Hall or opto sensors, where the output voltage temperature coefficient is not critical. The PNP circuit is slightly more complex, but is also more accurate over temperature. Neither circuit has current limiting.

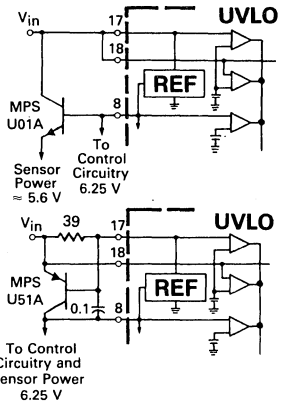
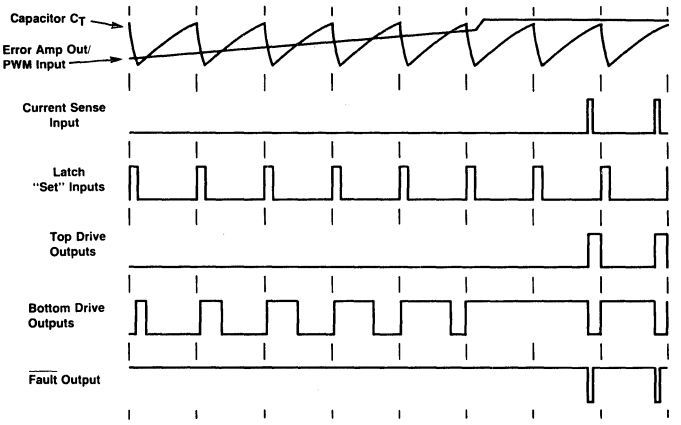


FIGURE 21 — PULSE WIDTH MODULATOR TIMING DIAGRAM



Undervoltage Lockout

A triple Undervoltage Lockout has been incorporated to prevent damage to the IC and the external power switch transistors. Under low power supply conditions, it guarantees that the IC and sensors are fully functional, and that there is sufficient bottom drive output voltage. The positive power supplies to the IC (V_{CC}) and the bottom drives (V_C) are each monitored by separate comparators that have their thresholds at 9.1 V. This level ensures sufficient gate drive necessary to attain low $r_{DS(on)}$ when driving standard power MOSFET devices. When directly powering the Hall sensors from the reference, improper sensor operation can result, if the reference output voltage falls below 4.5 V. A third comparator is used to detect this condition. If one or more of the comparators detects an undervoltage condition, the $\overline{\text{Fault}}$ output is activated, the top drives are turned off and the bottom drive outputs are held in a low state. Each of the comparators contain hysteresis to prevent oscillations when crossing their respective thresholds.

$\overline{\text{Fault}}$ Output

The open collector $\overline{\text{Fault}}$ output (Pin 14) was designed to provide diagnostic information in the event of a system malfunction. It has a sink current capability of 16 mA and can directly drive a light emitting diode for visual indication. Additionally, it is easily interfaced with TTL/CMOS logic for use in a microprocessor controlled system. The $\overline{\text{Fault}}$ output is active low when one or more of the following conditions occur:

1) Invalid Sensor Input code.
2) Enable Input at logic [0].
3) Current Sense Input greater than 100 mV.
4) Undervoltage Lockout, activation of one or more of the comparators.
5) Thermal Shutdown, maximum junction temperature being exceeded.

This unique output can also be used to distinguish between motor start-up or sustained operation in an overloaded condition. With the addition of an R/C network between the $\overline{\text{Fault}}$ output and the enable input, it is possible to create a time-delayed latched shutdown for overcurrent. The added circuitry shown in Figure 23, makes easy starting of motor systems which have high inertial loads by providing additional starting torque, while still preserving overcurrent protection. This task is accomplished by setting the current limit to a higher than nominal value for a predetermined time. During an excessively long overcurrent condition, capacitor C_{DLY} will charge causing the enable input to cross its threshold to a low state. A latch is then formed by the positive feedback loop from the $\overline{\text{Fault}}$ output to the enable input. Once set, by the current sense input, it can only be reset by shorting C_{DLY} or cycling the power supplies.

Drive Outputs

The three top drive outputs (Pins 1, 2, 24) are open collector NPN transistors capable of sinking 50 mA with a minimum breakdown of 30 volts. Interfacing into higher voltage applications is easily accomplished with the circuits shown in Figures 24 and 25.

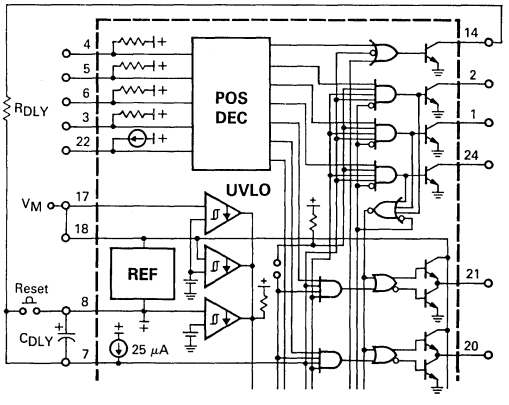
The three totem pole bottom drive outputs (Pins 19, 20, 21) are particularly suited for direct drive of 'N' channel MOSFETs or NPN bipolar transistors (Figures 26, 27, 28 and 29). Each output is capable of sourcing and sinking up to 100 mA. Power for the bottom drives is supplied from V_C (Pin 18). This separate supply input allows the designer added flexibility in tailoring the drive voltage, independent of V_{CC}. A zener clamp should be connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V so as to prevent rupture of the MOSFET gates.

The control circuitry ground (Pin 16) and current sense inverting input (Pin 15) must return on separate paths to the central input source ground.

Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC in the event the maximum junction temperature is exceeded. When activated, typically at 170°C, the IC acts as though the enable input was grounded.

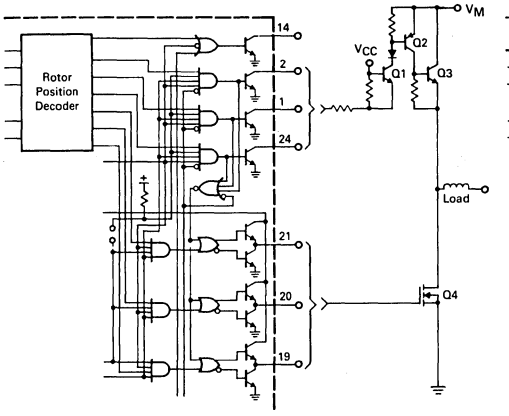
FIGURE 23 — TIMED DELAYED LATCHED OVER CURRENT SHUTDOWN



$$t_{DLY} \approx R_{DLY}\, C_{DLY} \ln\left(\frac{V_{ref} - (I_{IL}\ \text{enable}\ R_{DLY})}{V_{th}\ \text{enable} - (I_{IL}\ \text{enable}\ R_{DLY})}\right)$$

$$\approx R_{DLY}\, C_{DLY} \ln\left(\frac{6.25 - (20 \times 10^{-6} R_{DLY})}{1.4 - (20 \times 10^{-6} R_{DLY})}\right)$$

FIGURE 24 — HIGH VOLTAGE INTERFACE WITH NPN POWER TRANSISTORS



Transistor Q1 is a common base stage used to level shift from V_{CC} to the high motor voltage, V_M. The collector diode is required if V_{CC} is present while V_M is low.

FIGURE 25 — HIGH VOLTAGE INTERFACE WITH 'N' CHANNEL POWER MOSFETs

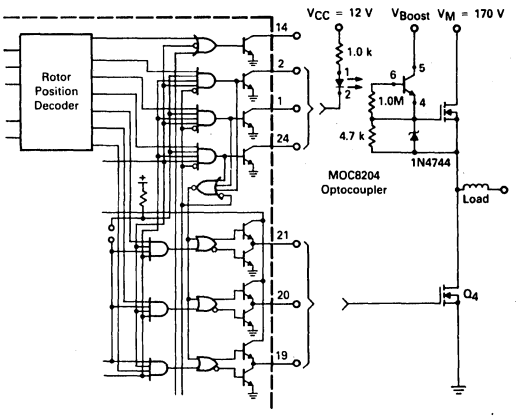
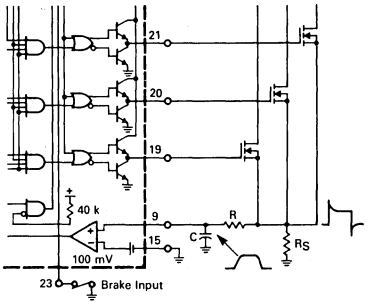
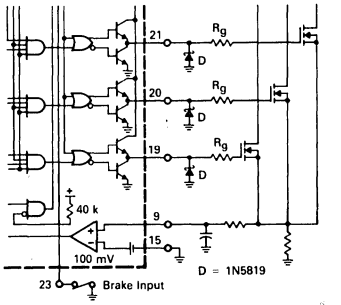


FIGURE 26 — CURRENT WAVEFORM SPIKE SUPPRESSION



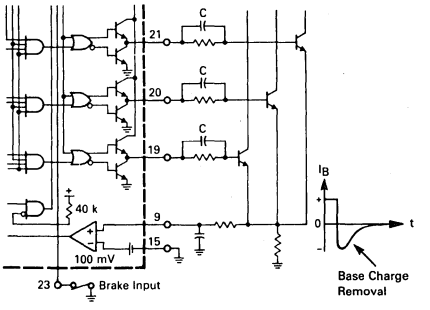
The addition of the RC filter will eliminate current-limit instability caused by the leading edge spike on the current waveform. Resistor R_S should be a low inductance type.

FIGURE 27 — MOSFET DRIVE PRECAUTIONS



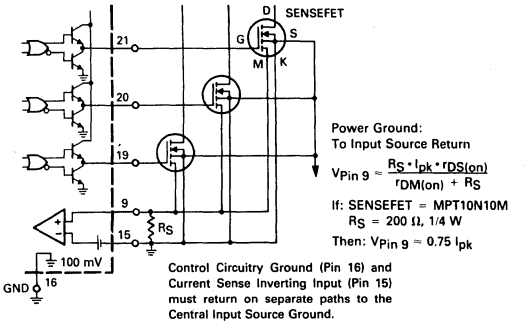
Series gate resistor R_g will damp any high frequency oscillations caused by the MOSFET input capacitance and any series wiring induction in the gate-source circuit. Diode D is required if the negative current into the Bottom Drive Outputs exceeds 50 mA.

FIGURE 28 — BIPOLAR TRANSISTOR DRIVE



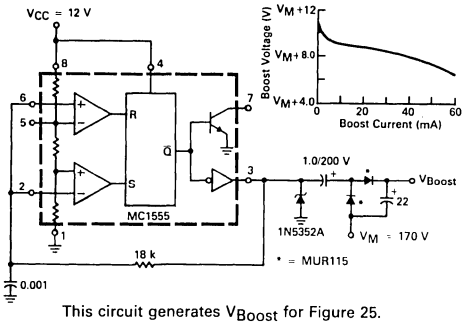
The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C.

FIGURE 29 — CURRENT SENSING POWER MOSFETs



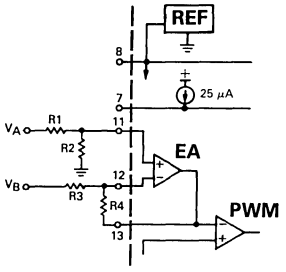
Virtually lossless current sensing can be achieved with the implementation of SENSEFET power switches.

FIGURE 30 — HIGH VOLTAGE BOOST SUPPLY



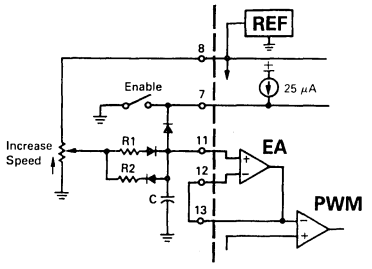
This circuit generates V_{Boost} for Figure 25.

FIGURE 31 — DIFFERENTIAL INPUT SPEED CONTROLLER



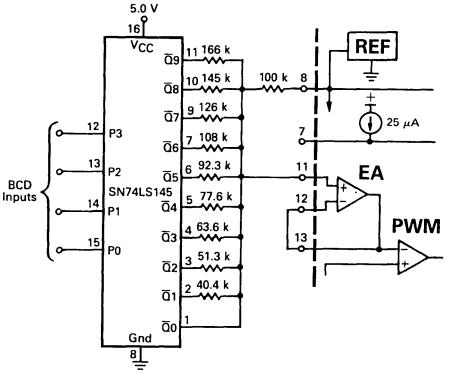
$$V_{pin\ 13} = V_A\left(\frac{R3+R4}{R1+R2}\right)\frac{R2}{R3} - \left(\frac{R4}{R3}V_B\right)$$

FIGURE 32 — CONTROLLED ACCELERATION/DECELERATION



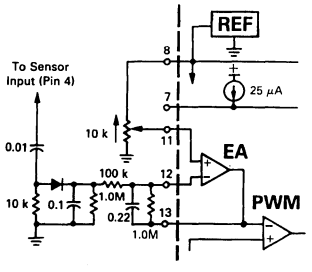
Resistor R1 with capacitor C sets the acceleration time constant while R2 controls the deceleration. The values of R1 and R2 should be at least ten times greater than the speed set potentiometer to minimize time constant variations with different speed settings.

FIGURE 33 — DIGITAL SPEED CONTROLLER



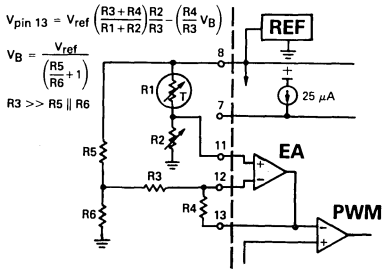
The SN74LS145 is an open collector BCD to One of Ten decoder. When connected as shown, input codes 0000 through 1001 steps the PWM in increments of approximately 10% from 0 to 90% on-time. Input codes 1010 through 1111 will produce 100% on-time or full motor speed.

FIGURE 34 — CLOSED LOOP SPEED CONTROL



The rotor position sensors can be used as a tachometer. By differentiating the positive-going edges and then integrating them over time, a voltage proportional to speed can be generated. The error amp compares this voltage to that of the speed set to control the PWM.

FIGURE 35 — CLOSED LOOP TEMPERATURE CONTROL



This circuit can control the speed of a cooling fan proportional to the difference between the sensor and set temperatures. The control loop is closed as the forced air cools the NTC thermistor. For controlled heating applications, exchange the positions of R1 and R2.

SYSTEM APPLICATIONS

Three Phase Motor Commutation

The three phase application shown in Figure 36 is a full-featured open-loop motor controller with full wave, six step drive. The upper power switch transistors are Darlingtons while the lower devices are power MOSFETs. Each of these devices contains an internal parasitic catch diode that is used to return the stator inductive energy back to the power supply. The outputs are capable of driving a delta or wye connected stator, and a grounded neutral wye if split supplies are used. At any given rotor position, only one top and one bottom power switch (of different totem poles) is enabled. This configuration switches both ends of the stator winding from supply to ground which causes the current flow to be bidirectional or full wave. A leading edge spike is usually present on the current waveform and can cause a current-limit instability. The spike can be eliminated by adding an RC filter in series with the current sense input. Using a low inductance type resistor for R_S will also aid in spike reduction. Care must be taken in the selection of the bottom power switch transistors so that the current during braking does not exceed the device rating. During braking, the peak current generated is limited only by the series resistance of the conducting bottom switch and winding.

$$I_{peak} = \frac{V_M + EMF}{R_{switch} + R_{winding}}$$

If the motor is running at maximum speed with no load, the generated back EMF can be as high as the supply voltage, and at the onset of braking the peak current may approach twice the motor stall current. Figure 37 shows the commutation waveforms over two electrical cycles. The first cycle (0° to 360°) depicts motor operation at full speed while the second cycle (360° to 720°) shows a reduced speed with about 50 percent pulse width modulation. The current waveforms reflect a constant torque load and are shown synchronous to the commutation frequency for clarity.

FIGURE 36 — THREE PHASE, SIX STEP, FULL WAVE MOTOR CONTROLLER

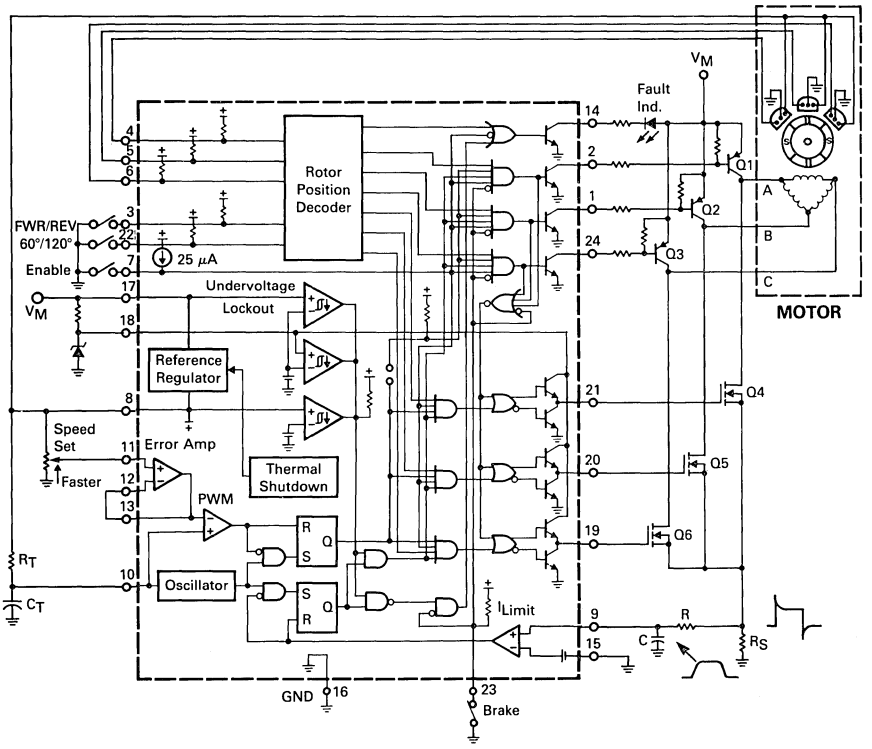


FIGURE 37 — THREE PHASE, SIX STEP, FULL WAVE COMMUTATION WAVEFORMS

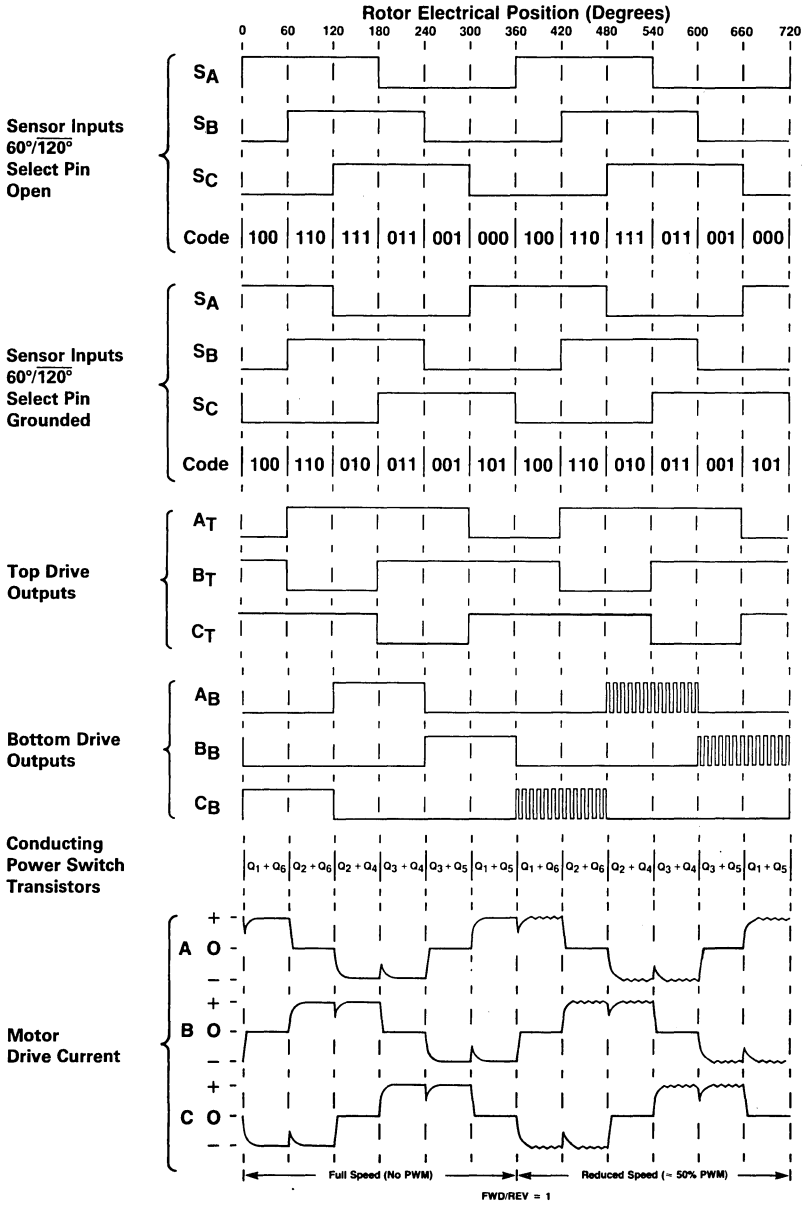
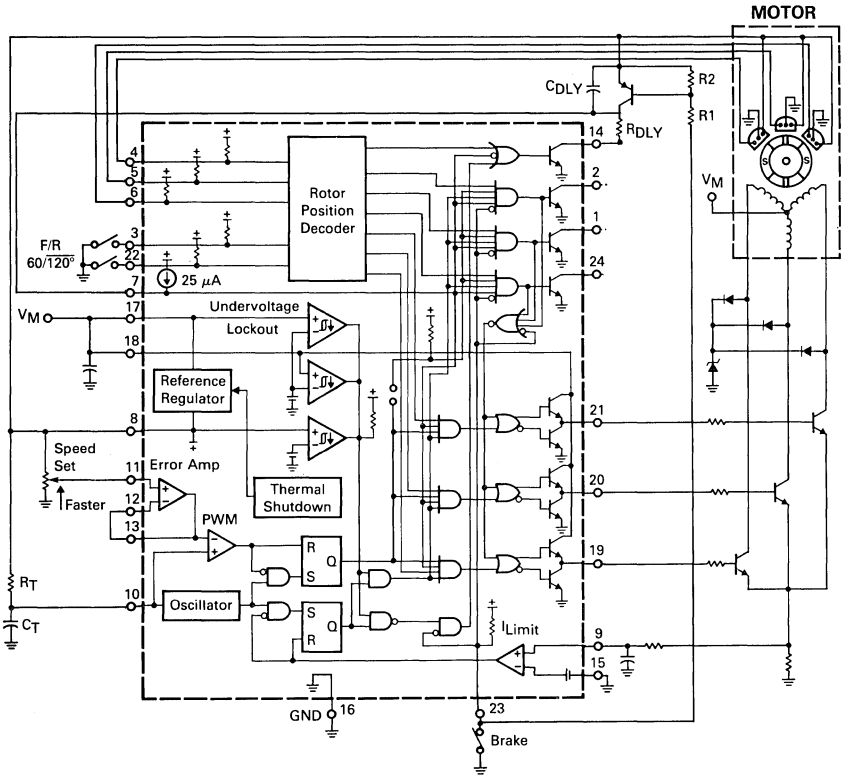


Figure 38 shows a three phase, three step, half wave motor controller. This configuration is ideally suited for automotive and other low voltage applications since there is only one power switch voltage drop in series with a given stator winding. Current flow is unidirectional or half wave because only one end of each winding is switched. Continuous braking with the typical half wave arrangement presents a motor overheating problem since stator current is limited only by the winding resistance. This is due to the lack of upper power switch transistors, as in the full wave circuit, used to disconnect the windings from the supply voltage V_M. A unique solution is to provide braking until the motor stops and then turn off the bottom drives. This can be accomplished by using the Fault output in conjunction with the Enable input as an over current timer. Components R_{DLY} and C_{DLY} are selected to give the motor sufficient time to stop before latching the Enable input and the top drive AND gates low. When enabling the motor, the brake switch is closed and the PNP transistor along with resistors R1 and R_{DLY} are used to reset the latch by discharging C_{DLY}. The stator flyback voltage is clamped by a single zener and three diodes.

FIGURE 38 — THREE PHASE, THREE STEP, HALF WAVE MOTOR CONTROLLER



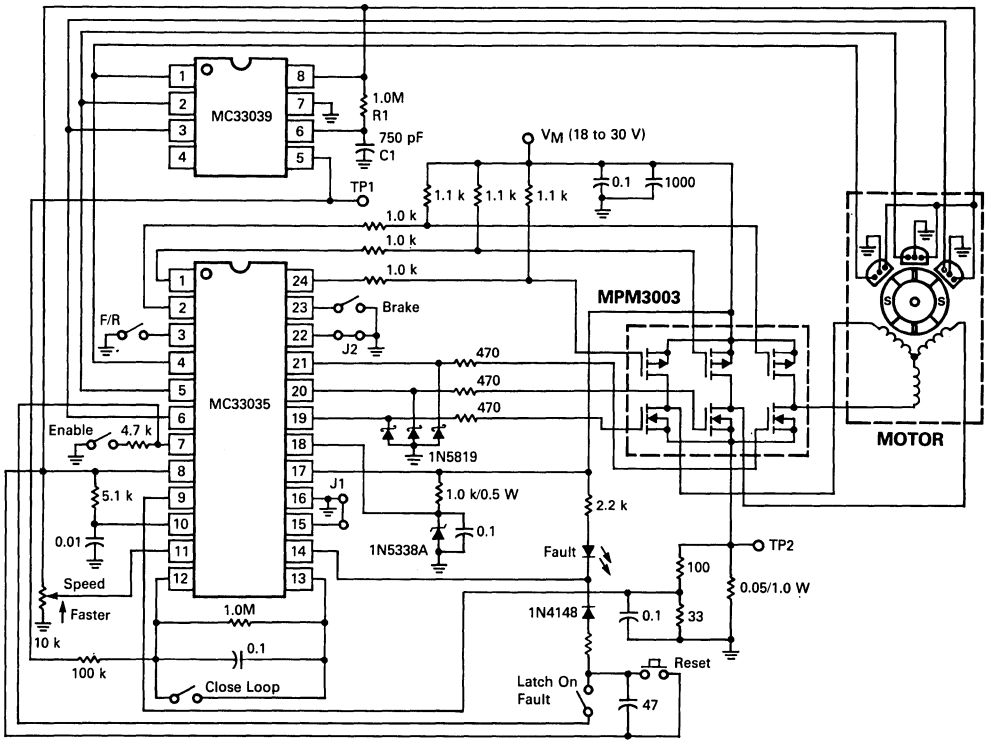
Three Phase Closed Loop Controller

The MC33035, by itself, is only capable of open loop motor speed control. For closed loop motor speed control, the MC33035 requires an input voltage proportional to the motor speed. Traditionally this has been accomplished by means of a tachometer to generate the motor speed feedback voltage. Figure 39 shows an application whereby an MC33039, powered from the 6.25 volt reference (Pin 8) of the MC33035, is used to generate the required feedback voltage without the need of a costly tachometer. The same Hall sensor signals used by the MC33035 for rotor position decoding are utilized by the MC33039. Every positive or negative going transition of the Hall sensor signals on any of the sensor lines causes the MC33039 to produce an output pulse of defined amplitude and time duration, as determined by the external resistor R1 and capacitor C1. The output train of pulses at Pin 5 of the MC33039 are integrated by the error amplifier of the MC33035 configured as an integrator to produce a DC voltage level which is proportional to the motor speed. This speed proportional voltage establishes the PWM reference level at pin 13 of the MC33035 motor controller and closes the feedback loop. The MC33035 outputs drive an MPM3003 TMOS power MOSFET 3-phase bridge circuit capable of delivering up to 25 Amperes of surge current. High currents can be expected during conditions of start-up, breaking, and change of direction of the motor.

The system shown in Figure 39 is designed for a motor having 120/240 degrees Hall sensor electrical phasing. The system can easily be modified to accommodate 60/300 degree Hall sensor electrical phasing by removing the jumper (J2) at Pin 22 of the MC33035.

4

FIGURE 39 — CLOSED LOOP BRUSHLESS DC MOTOR CONTROL USING THE MC33035, MPM3003, AND MC33039



4

Sensor Phasing Comparison

There are four conventions used to establish the relative phasing of the sensor signals in three phase motors. With six step drive, an input signal change must occur every 60 electrical degrees, however, the relative signal phasing is dependent upon the mechanical sensor placement. A comparison of the conventions in electrical degrees is shown in Figure 40. From the sensor phasing table, Figure 41, note that the order of input codes for 60° phasing is the reverse of 300°. This means the MC33035, when configured for 60° sensor electrical phasing, will equally operate a motor with either 60° or 300° sensor electrical phasing, but resulting in opposite directions of rotation. The same is true for the part when it is configured for 120° sensor electrical phasing; the motor will equally operate, but will result in opposite directions of rotation for 120° for 240° conventions.

FIGURE 40 — SENSOR PHASING COMPARISON

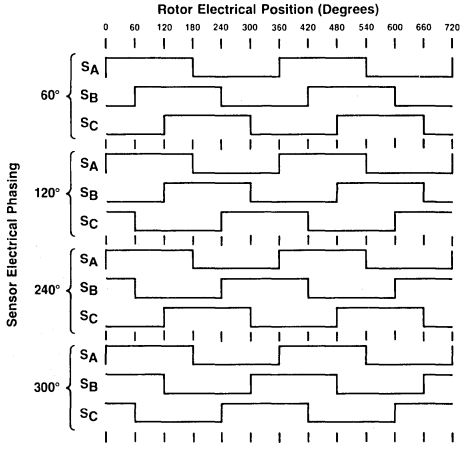


FIGURE 41 — SENSOR PHASING TABLE

Sensor Electrical Phasing (Degrees)												
60°			120°			240°			300°			
S_A	S_B	S_C	S_A	S_B	S_C	S_A	S_B	S_C	S_A	S_B	S_C	
1	0	0	1	0	1	1	1	0	1	1	1	
1	1	0	1	0	0	1	0	0	1	1	0	
1	1	1	1	1	0	1	0	1	1	0	0	
0	1	1	0	1	0	0	0	1	0	0	0	
0	0	1	0	1	1	0	1	1	0	0	1	
0	0	0	0	0	1	0	1	0	0	1	1	

In this data sheet, the rotor position is always given in electrical degrees since the mechanical position is a function of the number of rotating magnetic poles. The relationship between the electrical and mechanical position is:

$$\text{Electrical Degrees} = \text{Mechanical Degrees}\left(\frac{\#\text{Rotor Poles}}{2}\right)$$

An increase in the number of magnetic poles causes more electrical revolutions for a given mechanical revolution. General purpose three phase motors typically contain a four pole rotor which yields two electrical revolutions for one mechanical.

Two and Four Phase Motor Commutation

The MC33035 is also capable of providing a four step output that can be used to drive two or four phase motors. The truth table in Figure 42 shows that by connecting sensor inputs S_B and S_C together, it is possible to truncate the number of drive output states from six to four. The output power switches are connected to B_T, C_T, B_B, and C_B. Figure 43 shows a four phase, four step, full wave motor control application. Power switch transistors Q1 through Q8 are Darlington type, each with an internal parasitic catch diode. With four step drive, only two rotor position sensors spaced at 90 electrical degrees are required. The commutation waveforms are shown in Figure 44.

Figure 45 shows a four phase, four step, half wave motor controller. It has the same features as the circuit in Figure 38, except for the deletion of speed control and braking.

FIGURE 42 — TWO AND FOUR PHASE, FOUR STEP, COMMUTATION TRUTH TABLE

MC33035 (60°/$\overline{120°}$ Select Pin Open)						
Inputs			Outputs			
Sensor Electrical Spacing* = 90°			Top Drives		Bottom Drives	
S_A	S_B	F/R	B_T	C_T	B_B	C_B
1	0	1	1	1	0	1
1	1	1	0	1	0	0
0	1	1	1	0	0	0
0	0	1	1	1	1	0
1	0	0	1	0	0	0
1	1	0	1	1	1	0
0	1	0	1	1	0	1
0	0	0	0	1	0	0

*With MC33035 sensor input S_B connected to S_C

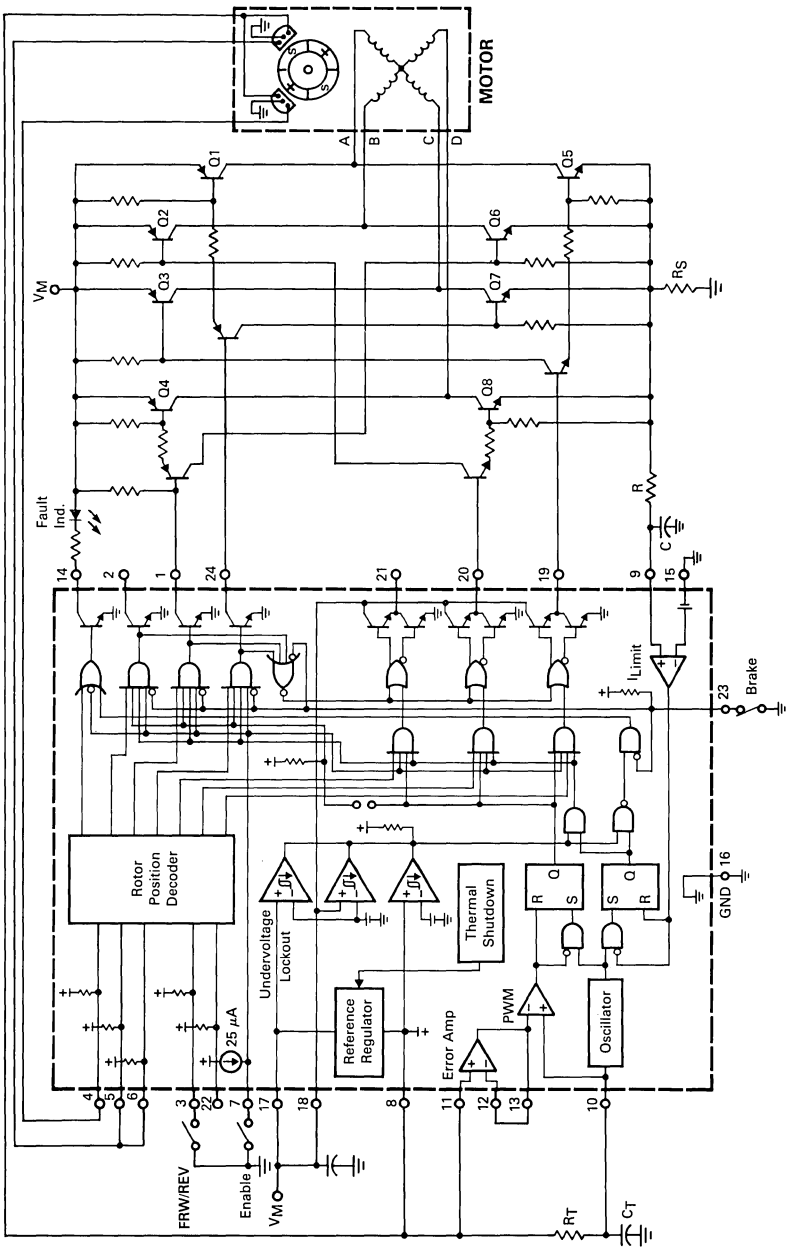
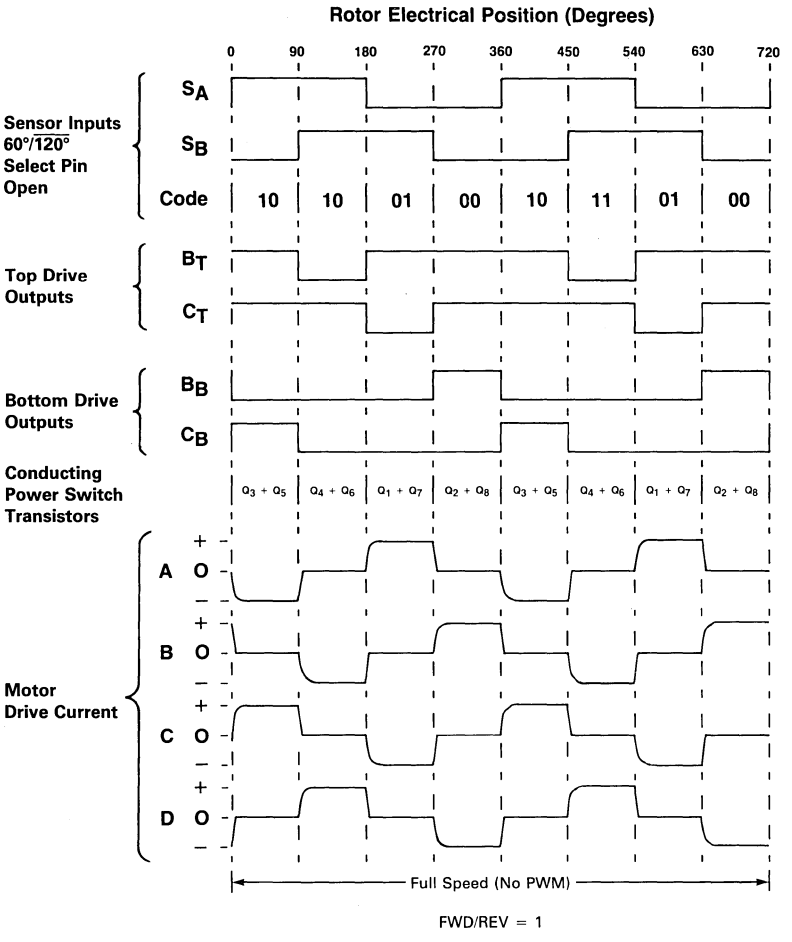


FIGURE 43 — FOUR PHASE, FOUR STEP, FULL WAVE CONTROLLER

FIGURE 44 — FOUR PHASE, FOUR STEP, FULL WAVE MOTOR CONTROLLER



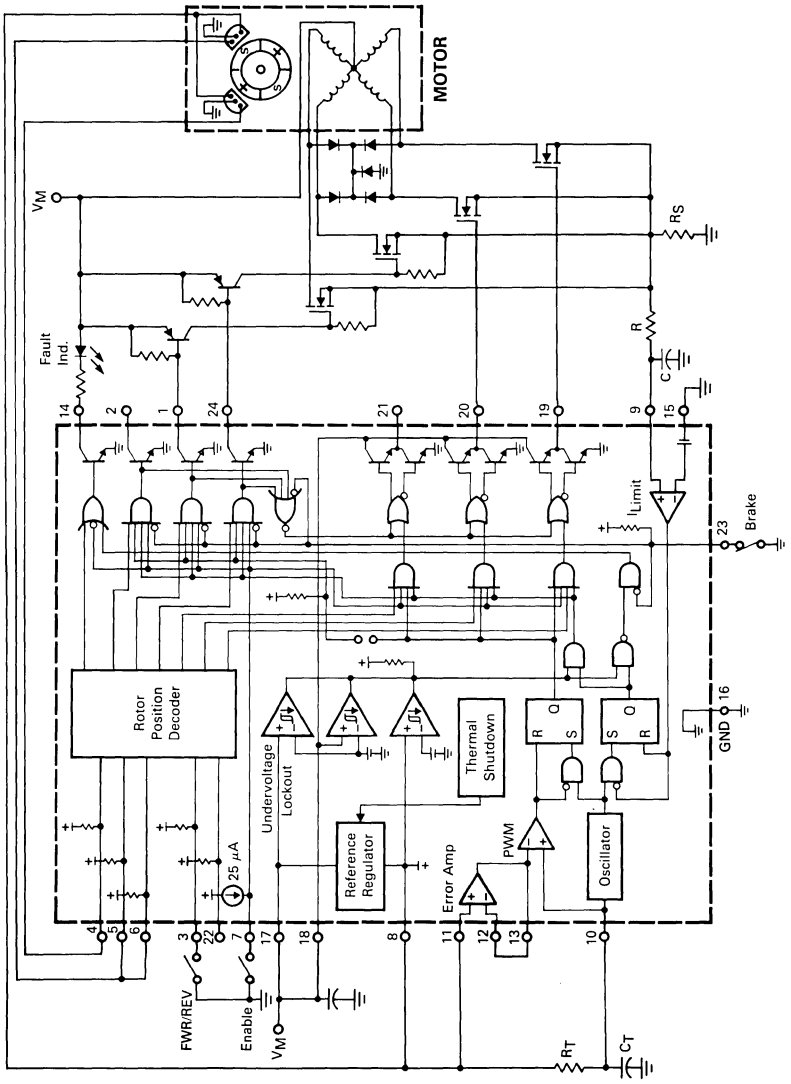


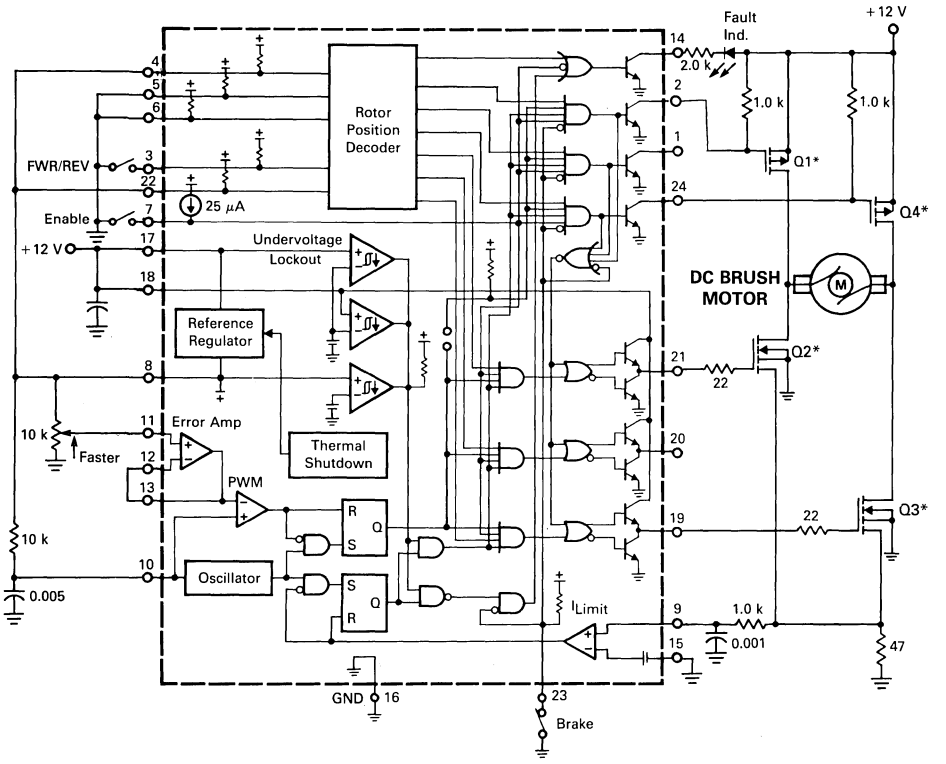
FIGURE 45 — FOUR PHASE, FOUR STEP, HALF WAVE MOTOR CONTROLLER

Brush Motor Control

Though the MC33035 was designed to control brushless DC motors, it may also be used to control DC brush-type motors. Figure 46 shows an application of the MC33035 driving a Motorola MPM3002 MOSFET H-bridge affording minimal parts count to operate a one-tenth horsepower brush-type motor. Key to the operation is the input sensor code [100] which produces a top-left (Q1) and a bottom-right (Q3) drive when the controller's forward/reverse pin is at logic [1]; top-right (Q4), bottom-left (Q2) drive is realized when the forward/reverse pin is at logic [0]. This code supports the requirements necessary for H-bridge drive accomplising both direction and speed control.

The controller functions in a normal manner with a pulse width modulated-frequency of approximately 25 kHz. Motor speed is controlled by adjusting the voltage presented to the noninverting input of the error amplifier establishing the PWM's slice or reference level. Cycle-by-cycle current limiting of 3.0 amperes motor current is accomplished by sensing the voltage (100 mV) across the 47 Ohm resistor to ground of the H-bridge motor current. The over current sense circuit makes it possible to reverse the direction of the motor, using the normal forward/reverse switch, on the fly and not have to completely stop before reversing.

FIGURE 46 — H-BRIDGE BRUSH-TYPE CONTROLLER



*Single Package MPM3002 MOSFET H-Bridge
M = 1/10th horsepower DC brush-type motor

LAYOUT CONSIDERATIONS

Do not attempt to construct any of the brushless motor control circuits on wire-wrap or plug-in prototype boards. High frequency printed circuit layout techniques are imperative to prevent pulse jitter. This is usually caused by excessive noise pick-up imposed on the current sense or error amp inputs. The printed circuit layout should contain a ground plane with low current signal and high drive and output buffer grounds returning on separate paths back to the power supply input filter capacitor V_M. Ceramic bypass capacitors (0.1 μF) connected close to the integrated circuit at V_{CC}, V_C, V_{ref} and the error amp noninverting input may be required depending upon circuit layout. This provides a low impedance path for filtering any high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI.

MC33039

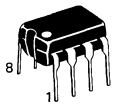
CLOSED-LOOP BRUSHLESS MOTOR ADAPTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

CLOSED-LOOP BRUSHLESS MOTOR ADAPTER

The MC33039 is a high performance closed-loop speed control adapter specifically designed for use in brushless dc motor control systems. Implementation will allow precise speed regulation without the need for a magnetic or optical tachometer. This device contains three input buffers each with hysteresis for noise immunity, three digital edge detectors, a programmable monostable, and an internal shunt regulator. Also included is an inverter output for use in systems that require conversion of sensor phasing. Although this device is primarily intended for use with the MC33034 brushless motor controller, it can be used cost effectively in many other closed-loop speed control applications.

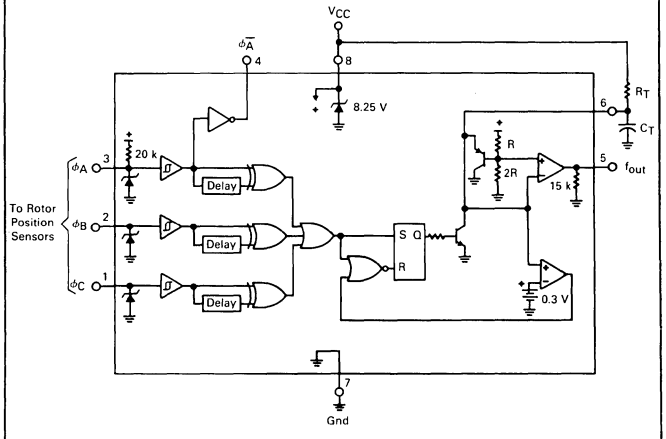
- Digital Detection of Each Input Transition for Improved Low Speed Motor Operation
- TTL Compatible Inputs With Hysteresis
- Operation Down to 5.5 V for Direct Powering from MC33034 Reference
- Internal Shunt Regulator Allows Operation from a Non-Regulated Voltage Source
- Inverter Output for Easy Conversion Between 60°/300° and 120°/240° Sensor Phasing Conventions



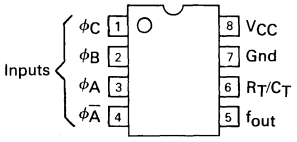
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

REPRESENTATIVE BLOCK DIAGRAM



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC33039D	−40°C to +85°C	SO-8
MC33039P		Plastic DIP

MAXIMUM RATINGS

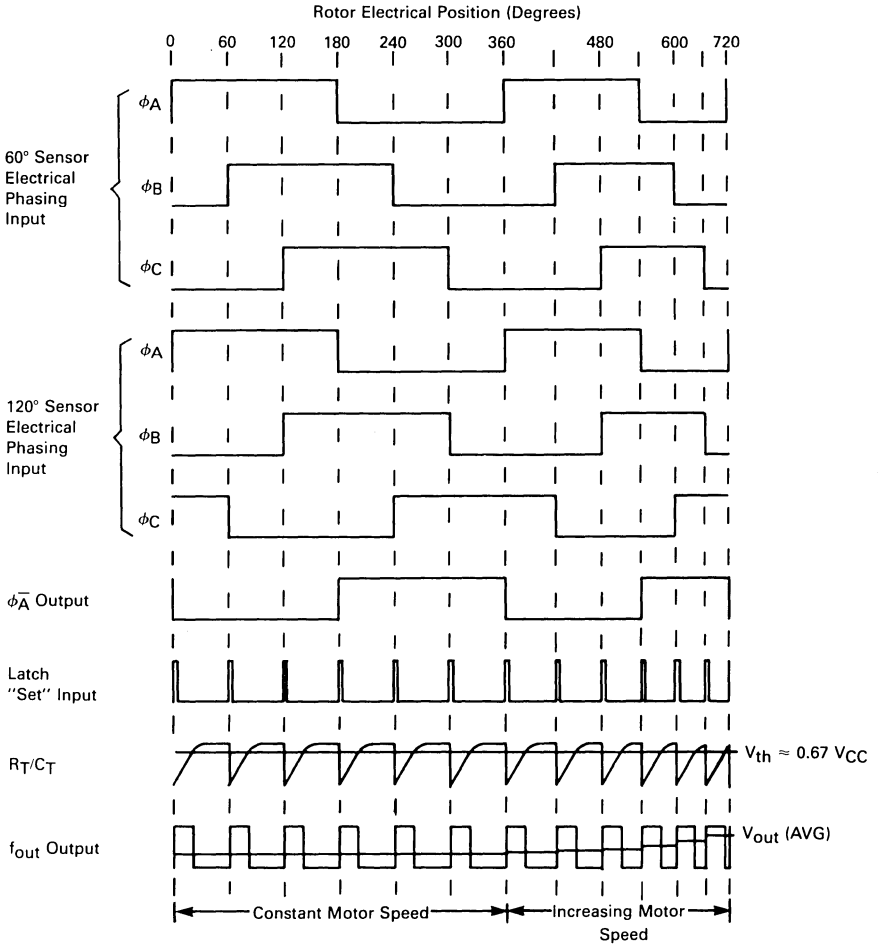
Rating	Symbol	Value	Unit
V_{CC} Zener Current	$I_{Z(V_{CC})}$	30	mA
Logic Input Current (Pins 1, 2, 3)	I_{IH}	5.0	mA
Output Current (Pin 4, 5), Sink or Source	I_{DRV}	20	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = +85°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$	 650 100	 mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

4

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.25 V, R_T = 10 k, C_T = 22 nF, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Threshold Voltage					V
High State	V_{IH}	2.4	2.1	—	
Low State	V_{IL}	—	1.4	1.0	
Hysteresis	V_H	0.4	0.7	0.9	
Input Current					μA
High State (V_{IH} = 5.0 V)	I_{IH}				
ϕA		−40	−60	−80	
ϕB, ϕC		—	−0.3	−5.0	
Low State (V_{IL} = 0 V)	I_{IL}				
ϕA		−190	−300	−380	
ϕB, ϕC		—	−0.3	−5.0	
MONOSTABLE AND OUTPUT SECTIONS					
Output Voltage					V
High State	V_{OH}				
f_{out} (I_{source} = 5.0 mA)		3.60	3.95	4.20	
$\overline{\phi A}$ (I_{source} = 2.0 mA)		4.20	4.75	—	
Low State	V_{OL}				
f_{out} (I_{sink} = 10 mA)		—	0.25	0.50	
$\overline{\phi A}$ (I_{sink} = 10 mA)		—	0.25	0.50	
Capacitor C_T Discharge Current	I_{dischg}	20	35	60	mA
Output Pulse Width (Pin 5)	t_{PW}	205	225	245	μs
POWER SUPPLY SECTION					
Power Supply Operating Voltage Range (T_A = −40°C to +85°C)	V_{CC}	5.5	—	V_Z	V
Power Supply Current	I_{CC}	1.8	3.9	5.0	mA
Zener Voltage (I_Z = 10 mA)	V_Z	7.5	8.25	9.0	V
Zener Dynamic Impedance (ΔI_Z = 10 mA to 20 mA, f ≤ 1.0 kHz)	$\lvert Z_{ka} \rvert$	—	2.0	5.0	Ω

FIGURE 1 — TYPICAL THREE PHASE, SIX STEP MOTOR APPLICATION



OPERATING DESCRIPTION

The MC33039 provides an economical method of implementing closed-loop speed control of brushless dc motors by eliminating the need for a magnetic or optical tachometer. Shown in the timing diagram of Figure 1, the three inputs (Pins 1, 2, 3) monitor the brushless motor rotor position sensors. Each sensor signal transition is digitally detected, OR'ed at the Latch 'Set' Input, and causes C_T to discharge. A corresponding output pulse is generated at f_{out} (Pin 5) of a defined amplitude, and programmable width determined by the values selected for R_T and C_T (Pin 6). The average voltage of the output pulse train increases with motor speed. When fed through a low pass filter or integrator, a dc voltage proportional to speed is generated. Figure 2 shows the proper connections for a typical closed loop application using the MC33034 brushless motor controller. Constant speed operation down to 100 RPM is possible with economical three phase four pole motors.

The ϕ_A inverter output (Pin 4) is used in systems where the controller and motor sensor phasing conventions are not compatible. A method of converting from either convention to the other is shown in Figure 3. For a more detailed explanation of this subject, refer to the text above Figure 39 on the MC33034 data sheet.

The output pulse amplitude V_{OH} is constant with temperature and controlled by the supply voltage on V_{CC} (Pin 8). Operation down to 5.5 V is guaranteed over temperature. For systems without a regulated power supply, an internal 8.25 V shunt regulator is provided.

FIGURE 2 — TYPICAL CLOSED-LOOP SPEED CONTROL APPLICATION

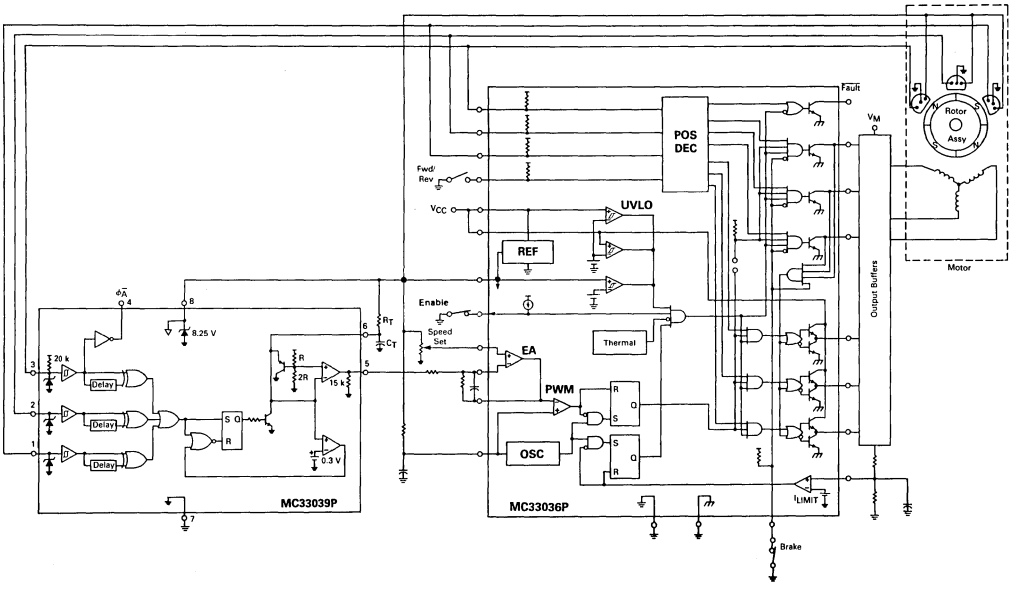


FIGURE 3 — f_{out} PULSE WIDTH versus TIMING RESISTOR

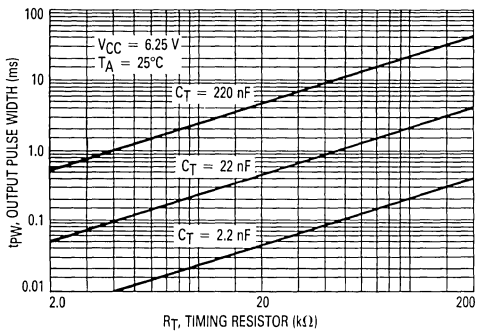


FIGURE 4 — f_{out}, PULSE WIDTH CHANGE versus TEMPERATURE

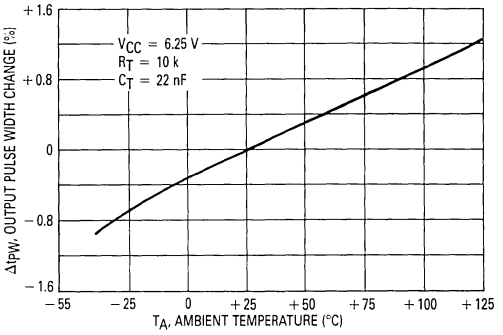


FIGURE 5 — f_{out} PULSE WIDTH CHANGE versus SUPPLY VOLTAGE

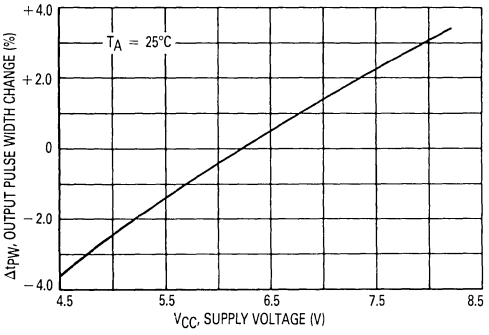


FIGURE 6 — SUPPLY CURRENT versus SUPPLY VOLTAGE

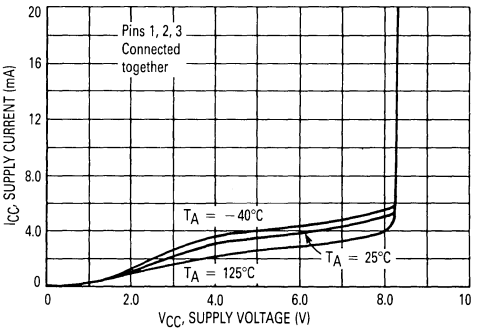


FIGURE 7 — f_{out}, SATURATION versus LOAD CURRENT

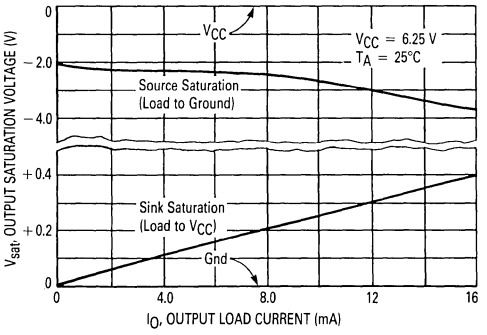
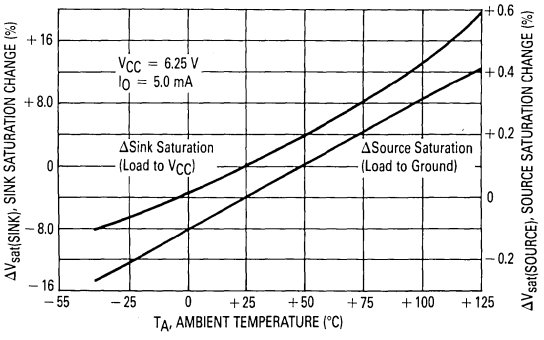


FIGURE 8 — f_{out}, SATURATION CHANGE versus TEMPERATURE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

SAA1042
SAA1042A

Advance Information

Stepper Motor Driver

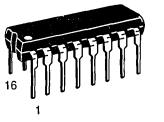
STEPPER MOTOR DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

4

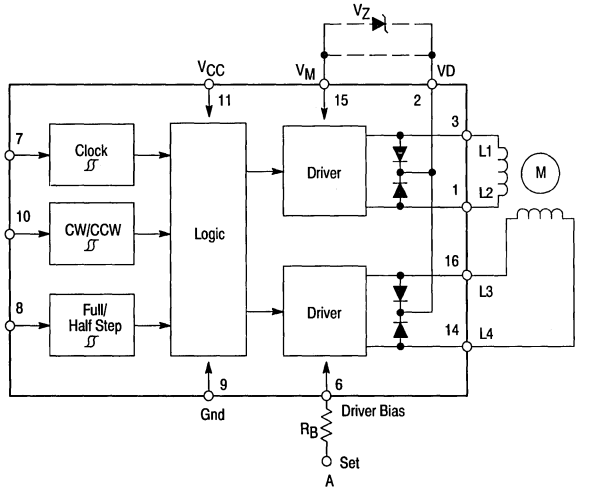
The SAA1042 drives a two-phase stepper motor in the bipolar mode. The device contains three input stages, a logic section and two output stages. The IC is contained in a 16 pin dual-in-line heat tab plastic package for improved heat sinking capability. The center four ground pins are connected to the copper alloy heat tab and improve thermal conduction from the die to the circuit board.

- Drive Stages Designed for Motors: 6.0 V and 12 V: SAA1042V
  24 V: SAA1042AV
- 500 mA/Coil Drive Capability
- Built-In Clamp Diodes for Overvoltage Suppression
- Wide Logic Supply Voltage Range
- Accepts Commands for CW/CCW and Half/Full Step Operation
- Inputs Compatible with Popular Logic Families: MOS, TTL, DTL
- Set Input Defined Output State
- Drive Stage Bias Adaptable to Motor Power Dissipation for Optimum Efficiency

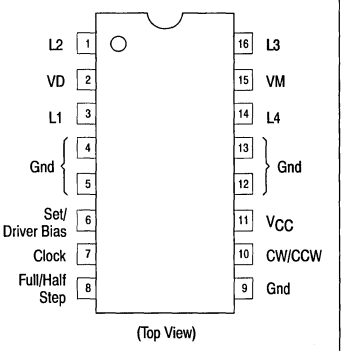


V SUFFIX
PLASTIC PACKAGE
CASE 648C

Figure 1. SAA1042 Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
SAA1042V	–30° to +125°C	Plastic DIP
SAA1042AV		Plastic DIP

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	SAA1042V	SAA1042AV	Unit
Clamping Voltage (Pins 1, 3, 14 and 16)	V_{clamp}	20	30	V
Over Voltage ($V_{OV} = V_{clamp} - V_M$)	V_{OV}	6.0	6.0	V
Supply Voltage	V_{CC}	20	30	V
Switching or Motor Current/Coil	I_M	500	500	mA
Input Voltage (Pins 7, 8 and 10)	V_{in} clock V_{in} Full/Half V_{in} CW/CCW	V_{CC}		V
Power Dissipation (Note 1) Thermal Resistance, Junction-to-Air Thermal Resistance, Junction-to-Case	P_D θJA θJC	2.0 80 15		W °C/W
Operating Junction Temperature Range	T_J	−30 to +125		°C
Storage Temperature Range	T_{stg}	−65 to +150		°C

NOTE: 1. The power dissipation (P_D) of the circuit is given by the supply voltage (V_M and V_{CC}) and the motor current (I_M), and can be determined from Figures 3 and 5. $P_D = P_{drive} - P_{logic}$.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristics	Pin(s)	Symbol	V_{CC}	Min	Typ	Max	Unit
Supply Current	11	I_{CC}	5.0 V	—	—	3.5	mA
			20 V	—	—	8.5	
Motor Supply Current ($I_{Pin\ 6}$ = −400 µA, Pins 1, 3, 14, 16 Open)	15	I_M					
V_M = 6.0 V			5.0 V	—	25	—	
V_M = 12 V			5.0 V	—	30	—	
V_M = 24 V			5.0 V	—	40	—	
Input High Voltage — High State	7, 8, 10	V_{IH}	5.0 V	2.0	—	—	V
			10 V	7.0	—	—	
			15 V	10	—	—	
			20 V	14	—	—	
Input Voltage — Low State		V_{IL}	5.0 V	—	—	0.8	
			10 V	—	—	1.5	
			15 V	—	—	2.5	
			20 V	—	—	3.5	
Input Reverse Current — High State ($V_{in} = V_{CC}$)	7, 8, 10	I_{IR}	5.0 V	—	—	2.0	µA
			10 V	—	—	2.0	
			15 V	—	—	3.0	
			20 V	—	—	5.0	
Input Forward Current — Low State (V_{in} = Gnd)		I_{IF}	5.0 V	−10	—	—	
			10 V	−25	—	—	
			15 V	−40	—	—	
			20 V	−55	—	—	
Output Voltage — High State (V_M = 12 V)	1, 3, 14, 16	V_{OH}	5.0 – 20 V				V
I_{out} = −500 mA				—	V_M − 2.0	—	
I_{out} = −50 mA				—	V_M − 1.2	—	
Output Voltage — Low State		V_{OL}	5.0 – 20 V				
I_{out} = 500 mA				—	0.7	—	
I_{out} = 50 mA				—	0.2	—	
Output Leakage Current, Pin 6 = Open ($V_M = V_D = V_{clamp\ max}$)	1, 3, 14, 16	I_{DR}	5.0 – 20 V	−100	—	—	µA
Clamp Diode Forward Voltage (Drop at I_M = 500 mA)	2	V_F	—	—	2.5	3.5	V
Clock Frequency	7	f_c	5.0 – 20 V	0	—	50	kHz
Clock Pulse Width		t_w	5.0 – 20 V	10	—	—	µs
Set Pulse Width	6	t_s	—	10	—	—	µs
Set Control Voltage — High State		—	—	V_M	—	—	V
Low State				—	—	0.5	

INPUT/OUTPUT FUNCTIONS

Clock — (Pin 7) This input is active on the positive edge of the clock pulse and accepts Logic '1' input levels dependant on the supply voltage and includes hysteresis for noise immunity.

CW/CCW — (Pin 10) This input determines the motor's rotational direction. When the input is held low, (OV, see the electrical characteristics) the motor's direction is nominally clockwise (CW). When the input is in the high state, Logic '1', the motor direction is nominally counter clockwise (CCW), depending on the motor connections.

4

Full/Half Step — (Pin 8) This input determines the angular rotation of the motor for each clock pulse. In the low state the motor will make a full step for each applied clock pulse, while in the high state, the motor will make half a step.

V_D — (Pin 2) This pin is used to protect the outputs (1, 3, 14, 16) where large positive spikes occur due to switching the motor coils. The maximum allowable voltage on these pins is the clamp voltage (V_{clamp}). Motor performance is improved if a zener diode is connected between Pin 2 and 15, as shown in Figure 1.

The following conditions have to be considered when selecting the zener diode:

$$V_{clamp} = V_M + 6.0\ V$$
$$V_Z = V_{clamp} - V_M - V_F$$

where: V_F = clamp diodes forward voltage drop (see Figure 4)
V_{clamp}: ≤ 20 V for SAA1042V ≤ 30 V for SAA1042AV
Pins 2 and 15 can be linked, in this case $V_Z = 0$ V.

Set/Bias Input — (Pin 6) This input has two functions:
1) The resistor R_B adapts the drivers to the motor current.
2) A pulse via the resistor R_B sets the outputs (1, 3, 14, 16) to a defined state.

The resistor R_B can be determined from the graph of Figure 2 according to the motor current and voltage. Smaller values of R_B will increase the power dissipation of the circuit and larger values of R_B may increase the saturation voltage of the driver transistors.

When the "set" function is not used, terminal A of the resistor R_B must be grounded. When the set function is used, terminal A has to be connected to an open-collector (buffer) circuit. Figure 7 shows this configuration. The buffer circuit (off-state) has to sustain the motor voltage (V_M). When a pulse is applied via the buffer and the bias resistor (R_B), the motor driver transistors are turned off during the pulse and after the pulse has ended, the outputs will be in defined states. Figure 6 shows the timing diagram.

Figure 7 illustrates a typical application in which the SAA1042 drives a 12 V stepper motor with a current consumption of 200 mA/coil. A bias resistor (R_B) of 56 kΩ is chosen according to Figure 2.

The maximum voltage permitted at the output pin is $V_M + 6.0$ V (see Maximum Ratings table), in this application $V_M = 12$ V, therefore the maximum voltage is 18 V. The outputs are protected by the internal diodes and an external zener connected between Pins 2 and 15.

From Figure 4, it can be seen that the voltage drop across the internal diodes is about 1.7 V at 200 mA. This results in a zener voltage between Pins 2 and 15 of:

$$V_Z = 6.0\ V - 1.7\ V = 4.3\ V.$$

To allow for production tolerances and a safety margin, a 3.9 V zener has been chosen for this example.

The clock is derived from the line frequency which is phase-locked by the MC14046B and the MC14024. The voltage on the clock input is normally low (Logic '0'). The motor steps on the positive going transition of the clock pulse.

The Logic '0' applied to the Full/Half input (Pin 8) operates the motor in Full Step mode. A Logic '1' at this input will result in Half Step mode. The logic level state on the CW/CCW input (Pin 10), and the connection of the motor coils to the outputs determines the rotational direction of the motor.

These two inputs should be biased to a Logic '0' or '1' and not left floating. In the event of non-use, they should be tied to ground or the logic supply line, V_{CC}.

The output drivers can be set to a fixed operating point by use of the Set input and a bias resistor, R_B. A positive pulse to this input turns the drivers off and sets the logic state of the outputs.

After the negative going transition of the Set pulse, and until the first positive going transition of the clock, the outputs will be:

L1 = L3 = high and L2 = L4 = low, (see Figure 6).

The Set input can be driven by a MC14007B or a transistor whose collector resistor is R_B. **If the input is not used, the bottom of R_B must be grounded.**

The total power dissipation of the circuit can be determined from Figures 3 and 5:

$$P_D = 0.9\ W + 0.08\ W = 0.98\ W.$$

The junction temperature can then be computed using Figure 8.

Figure 2. Bias Resistor R_B versus Motor Current

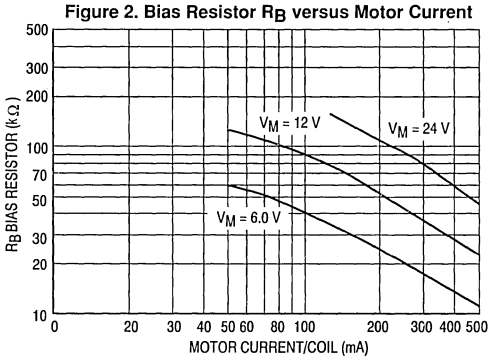


Figure 3. Drive Stage Power Dissipation

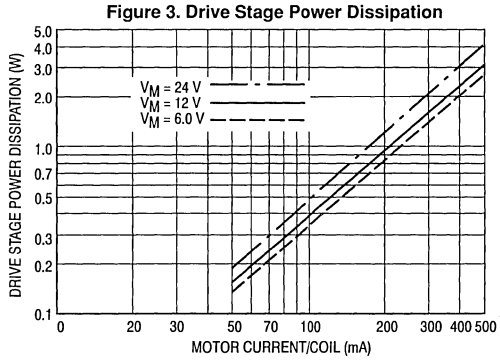


Figure 4. Clamp Diode Forward Current versus Forward Voltage

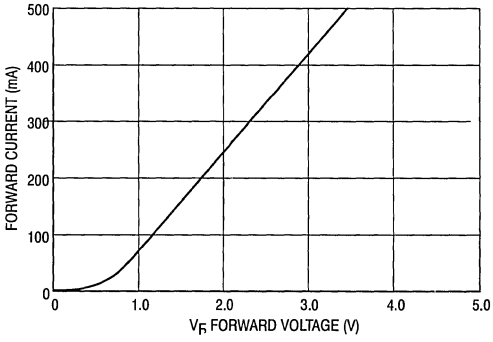


Figure 5. Power Dissipation versus Logic Supply Voltage

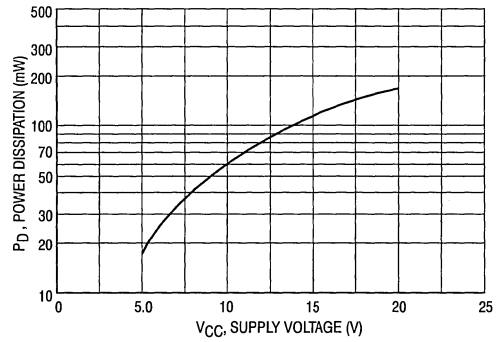


Figure 6. Timing Diagram

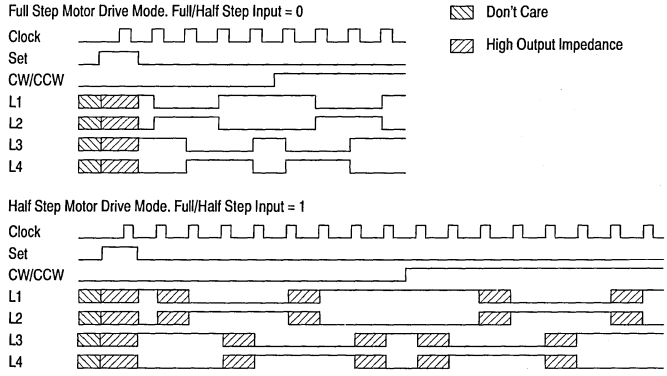


Figure 7. Typical Application
Selectable Step Rates with the Time Base Derived from the Line Frequency

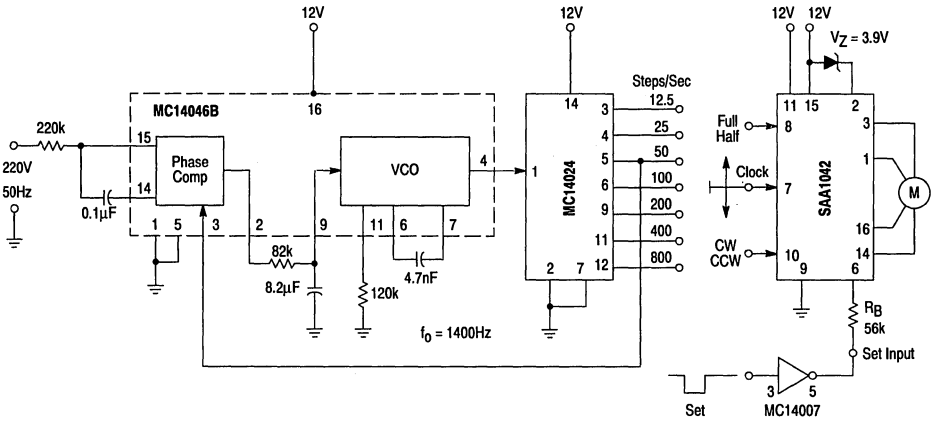
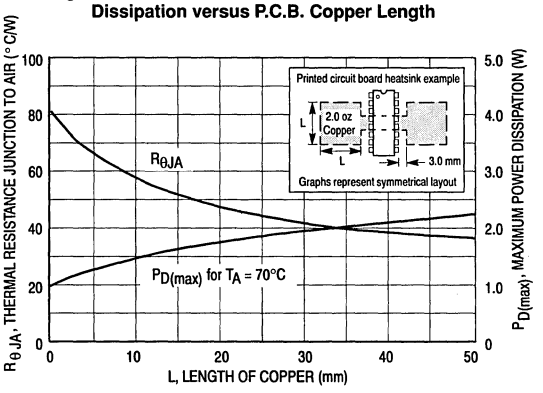


Figure 8. Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

TDA1085A

UNIVERSAL MOTOR SPEED CONTROLLER

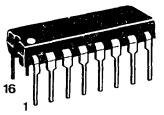
SILICON MONOLITHIC INTEGRATED CIRCUIT

4

UNIVERSAL MOTOR SPEED CONTROLLER

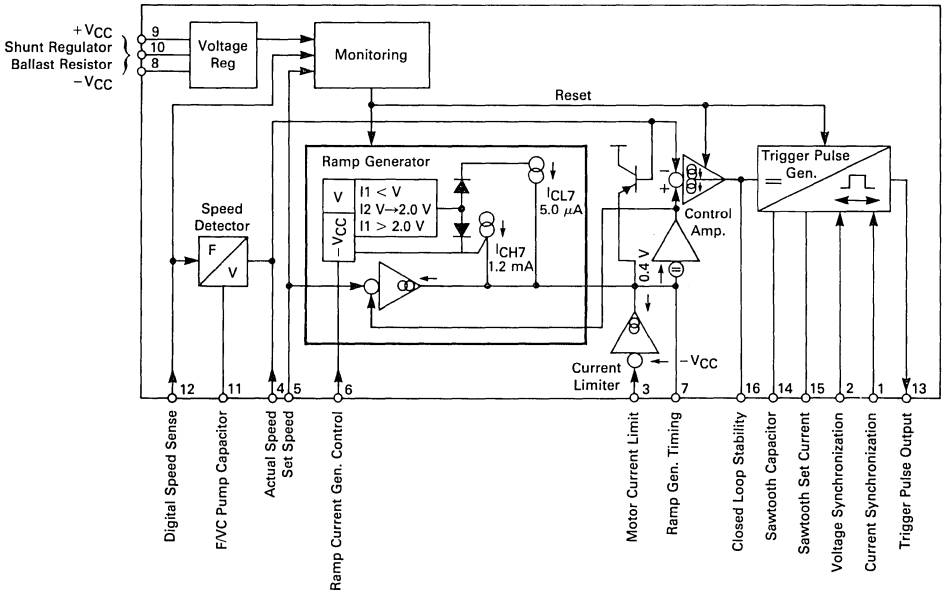
The TDA1085A has all the necessary functions for the speed control of universal (ac/dc) motors in an open or closed loop configuration. Additionally it has the facility for defining the initial speed/time characteristic. The circuit provides a phase angle varied trigger pulse to the motor control triac.

- Guaranteed Full Wave Triac Drive
- Soft Start from Powerup
- On-Chip Frequency/Voltage Convertor and Ramp Generator
- Current Limiting Incorporated
- Direct Drive from ac Line



PLASTIC PACKAGE
CASE 648

FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT



MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage	$V_{Pin\ 9-8}$	17	V
Power Supply Current (Pin 10 Open)	$I_{Pin\ 9}$	15	mA
Peak Power Supply Regulation Current	$I_{Pin\ 9} + I_{Pin\ 10}$	35	mA
Peak ac Synchronization Input Current	$I_{Pin\ 1}$ $I_{Pin\ 2}$	±1.0	mA
Peak Output Triggering Current (Pulse Width 300 μs; Duty Cycle ≤ 3%)	$I_{Pin\ 13}$	200	mA
Current Drain per Listed Pin	I_{15} I_3 I_{12}	1.0 −5.0 −3.0, +0.1	mA
Power Dissipation (T_A = 25°C) Derate above 25°C	P_D $1/R_{\theta JA}$	625 6.8	mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REGULATOR					
Regulated Voltage* ($I_9 + I_{10}$ = 10 mA)	V_{CC}	—	15.5	—	V
Monitoring Enable Level*	V_{ME}	—	15.1	—	V
Monitoring Disable Level*	V_{MD}	—	14.5	—	V
Internal Current Consumption (Note 1)	$I_{Pin\ 9}$	—	4.2	—	mA
RAMP GENERATOR					
Reference Input Voltage Range (Note 2)	$V_{Pin\ 5-8}$	0.08	—	13.5	V
Reference Input Bias Current	$I_{Pin\ 5}$	—	—	−20	μA
Distribute Low Level Voltage Range	$V_{Pin\ 6}$	0	—	2.0	V
Distribute — Low Level (Figure 2)	V_{DL}	—	$V_{Pin\ 6}$	—	V
Distribute — Upper Level* (Figure 2) ($V_{Pin\ 6}$ = 950 mV)	V_{DU}	1.9 V_6	2.0 V_6	2.1 V_6	V
Low–High Acceleration Range (Figure 2)	ΔV_{DA}	—	400	—	mV
High Acceleration Charging Current	I_{CH7}	—	1.2	—	mA
Low Charging Current (Note 3)	I_{CL7}	—	5.0	—	μA

NOTES:
1. Pins 1, 2, 11, 12, 14 and 15 not connected; Pins 4, 5, 6 and 7 grounded to Pin 8: V_{CC} = 15.5 V.
2. When $V_{Pin\ 5}$ is ≤ 80 mV, the internal monitoring circuit interprets it as a true zero, thus minimizing the effects of control amplifier offsets.
3. This value should be accounted for when externally setting the distribute acceleration charging current.

* These figures apply for the application shown in Figure 4.

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT LIMITER					
Stage Current Gain	$\frac{I_{DL7}}{\Delta I_3}$	—	170	—	—
Output Discharge Current Swing	I_{DL7}	—	35	—	mA
CONTROL AMPLIFIER					
Actual Speed Voltage Range	$V_{Pin\ 4\text{-}8}$	0	—	13.5	V
Actual Speed Input Bias Current	$I_{Pin\ 4}$	—	—	−350	nA
Total Input Offset Voltage (Note 4)	V_{off}	−60	—	20	mV
Transconductance $\left(\frac{\Delta I_{Pin\ 16}}{V_{Pin\ 4} - V_{Pin\ 7}}\right)$	g_m	—	300	—	μA/V
Output Current Swing	$I_{Pin\ 16}$	—	±100	—	μA
FREQUENCY/VOLTAGE CONVERTER					
Input Signal Low Voltage (Note 5)	V_{L12}	−0.1	—	—	V
Input Signal High Voltage	V_{H12}	0.1	—	5.0	V
Polarization Current	$I_{Pin\ 12}$	—	−25	—	μA
Conversion Rate* (Note 6)	K_C	—	15	—	mV/Hz
Linearity* (Figure 3)	K_L	—	±4.0	—	%
TRIGGER PULSE GENERATOR					
Voltage Synchronization Levels	$V_{Pin\ 2}$	—	±50	—	μA
Current Synchronization Levels	$I_{Pin\ 1}$	—	±50	—	μA
Input Voltage Swing (for full angle swing)	V	—	11.7	—	V
Trigger Pulse Width (Note 7)	t_p	—	55	—	μs
Trigger Pulse Repetition Period	t_{prp}	—	215	—	μs
Trigger Pulse High Level ($I_{Pin\ 13}$ = 150 mA)	$V_{Pin\ 13}$	$V_{CC}-4$	—	—	V
Output Leakage Current ($V_{Pin\ 13}$ = 0 V)	$I_{OPin\ 13}$	—	—	30	μA

4. V_{off} is defined as being the voltage difference between Pin 5 and 4 with no current flow on Pin 16.
5. The negative swing is clamped to −0.3 V.
6. $V_{Pin\ 4} = k \cdot C_{Pin\ 11} \cdot (V_{CC} - V_a) \cdot R_{Pin\ 4} \cdot \left(1 + \frac{180 \times 10^3}{R_{Pin\ 11}}\right) - 1 \cdot \text{freq in.}$

   Where: $9 < K < 13$ & V_a = 1.3 V.
7. The timing given is when $C_{Pin\ 14}$ = 47 nF.

* These figures apply for the application shown in Figure 4.

INPUT/OUTPUT FUNCTIONS

VOLTAGE REGULATOR — (Pins 8, 9, 10). This is a parallel type voltage regulator able to sink a large amount of current while offering good regulation characteristics.

A resistor between Pins 9 and 10 reduces the internal power dissipation. Under minimal current sink conditions (min. current from the unregulated supply, max. consumption by the circuitry), at least 1.0 mA should flow through this resistor. Under max. sink conditions (max. current from the unregulated supply, min. consumption by the circuitry), the maximum resistor value is chosen so that the voltage at Pin 10 falls towards 3.0 V, but not lower. The above, fixed dynamic range of the regulator must not be exceeded within one line cycle.

A power supply failure causes shutdown.

For operation from an externally regulated voltage, Pin 10 is not connected.

SPEED SENSING — (Pins 4, 11, 12). Speed sensing can be achieved either digitally (tachogenerator frequency) or analogically (tachogenerator amplitude).

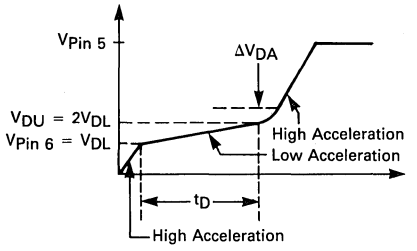
For digital sensing, a bipolar signal with respect to ground is applied to Pin 12. During positive excursions $C_{Pin\ 11}$ is charged. An internal mirror delivers ten times the charge on $C_{Pin\ 11}$ via Pin 4. However, due to internal circuitry, the charge on Pin 4 can vary in the region of 9 to 13 times the charge on $C_{Pin\ 11}$. For that reason it is necessary to calibrate the Frequency/Voltage Convertor (F/VC) with a variable resistor on Pin 4. Thus the relationship between speed and $V_{Pin\ 4}$ is defined by $R_{Pin\ 4}$ and $C_{Pin\ 11}$.

To maintain linearity in the high speed ranges it is important that $C_{Pin\ 11}$ is fully charged across an equivalent resistor of about 180 kΩ. It should be borne in mind that the impedance on Pin 11 should be kept as low as possible as $C_{Pin\ 11}$ has a large influence on the temperature coefficient of the FV/C. The time constant on Pin 4 should also be kept as low as possible.

Pin 12 is also an impedance monitoring input; at high impedances $V_{Pin\ 12}$ increases. Should $V_{Pin\ 12}$ exceed 5.0 V the triac trigger pulses are inhibited and the circuit resets.

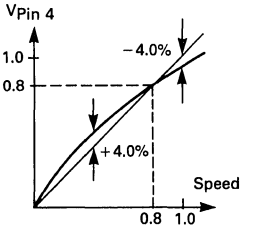
A 470 kΩ resistor from Pin 11 to $+V_{CC}$ significantly reduces the leakage current and reduces the device temperature coefficient to almost zero.

FIGURE 2 — RAMP GENERATOR TRANSFER CHARACTERISTIC



The shape of the curve is determined by $CR_{Pin\ 7}$; where $C_{Pin\ 7}$ defines the high acceleration slope and $R_{Pin\ 7}$ defines that of the low acceleration.

FIGURE 3 — FREQUENCY/VOLTAGE CONVERTER OUTPUT CHARACTERISTIC



INPUT/OUTPUT FUNCTIONS (continued)

For analog sensing input 12 should be grounded and a positive signal, with respect to ground, Pin 8, applied to Pin 4.

RAMP GENERATOR — (Pins 5, 6, 7) (refer to Figure 2). A preset voltage applied to Pin 5 will initiate the generation of a ramp whose final value is determined by the voltage applied to Pin 5. The voltage applied to Pin 6 will determine how much of the full ramp, shown in Figure 2, is used. The charging current passing through Pin 7 to the ramp generator timing capacitor determines the ramp slope.

When Pin 6 is held at $-V_{CC}$ a charging current of 1.2 mA is delivered to Pin 7, regardless of the voltage of Pin 5. This represents the high acceleration period shown in Figure 2.

If the preset voltage applied to Pin 5 is equal to or less than the voltage on Pin 6 the charging current will be 1.2 mA, or high acceleration.

If the preset voltage applied to Pin 5 is between $V_{Pin\ 6}$ and 2 $V_{Pin\ 6}$ the charging current is 1.2 mA (high acceleration) until the voltage at the reference input of the control amplifier equals $V_{Pin\ 6}$. At this point the charging current will switch to 5.0 μA; i.e. low acceleration.

If the preset voltage applied to Pin 5 is greater than 2 $V_{Pin\ 6}$ the charging current will be 1.2 mA (high acceleration) until the control amplifier's reference input reaches $V_{Pin\ 6}$ when it will switch to 5.0 μA (low acceleration) until 2 $V_{Pin\ 6}$ is reached. At this point the charging current will revert to 1.2 mA, high acceleration, until the final value of $V_{Pin\ 5}$ is reached.

Should the preset voltage at Pin 5 fall below 80 mV, the triac trigger pulses are inhibited and the circuit resets. This fact should be borne in mind when switching from one preset value to another.

As long as the voltages applied at Pins 5 and 6 are derived from the internal voltage regulator, they and the voltage on Pin 4 are ratioed and thus independent of the voltage regulator spread and temperature coefficient.

CURRENT LIMITER — (Pin 3). Safe operation of the motor and triac under all conditions is ensured by reducing the motor speed if a preset current limit is exceeded.

This is achieved as follows: The motor current will set up an alternating current, consisting of positive and negative peaks through the shunt resistor (0.05 Ω in Figure 4).

The negative peaks of this current are fed through a resistor to Pin 3 where they are compared with a preset current defined by a resistor between Pin 3 and $+V_{CC}$. An excessive shunt current will try to pull Pin 3 below $-V_{CC}$, but the current limiter becomes active at this point and reduces the charge on $C_{Pin\ 7}$, consequently reducing the motor speed.

Thus the value of the shunt and the ratio of the two resistors to Pin 3 fix the level at which the limiter becomes active, while the parallel equivalent of the two resistors determines the magnitude of the discharge current and thus how rapidly the circuit responds to an overcurrent condition.

CONTROL AMPLIFIER — (Pin 16). Connected to this pin is a network which compensates electrically for the mechanical characteristics of the motor and its load to give the circuit optimum closed loop stability and transient response.

The component values are best determined empirically by connecting R and C substitution boxes and looking for the best results.

TRIGGER PULSE GENERATOR — (Pins 1, 2, 13, 14, 15). This circuit performs four functions:

1. The conversion of the control amplifier's dc output level to a proportional firing angle positioned to within half a line cycle.
2. The calibration of the pulse width.
3. The repetition of the firing pulse if the triac fails to latch, or if the current is interrupted by brush bounce.
4. To delay the firing pulse until the current crosses zero at wide firing angles.

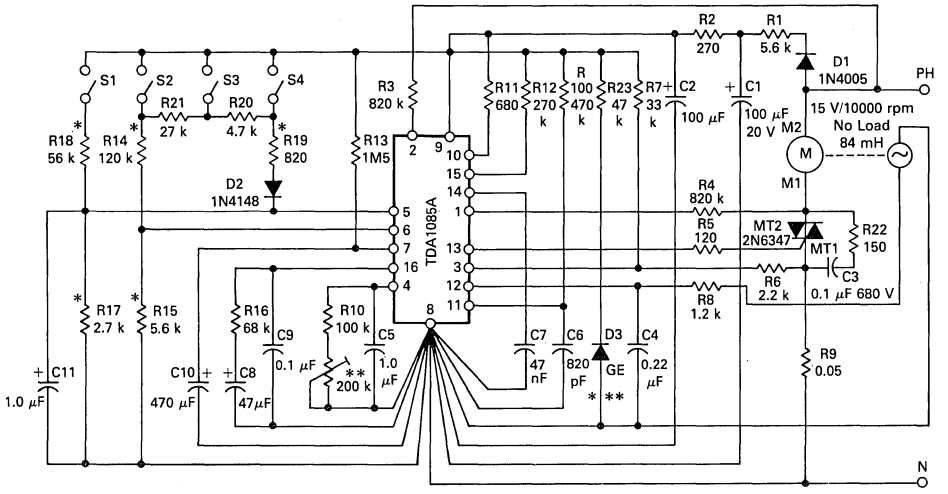
$R_{Pin\ 15}$ and $C_{Pin\ 14}$ fix the sawtooth while $C_{Pin\ 14}$ also determines the pulse width.

Pin 13 is the trigger pulse output. A current limiting resistor is essential on this pin. This configuration will drive two thyristors controlling a bridge if the supply for the speed controller is isolated.

4

TYPICAL APPLICATIONS

FIGURE 4 — CLOSED LOOP, FULLY PROGRAMMED, MULTI-SPEED SYSTEM WITH CURRENT LIMITING



* Chosen to suit the speeds required
** Adjust for the highest speed
*** Required only with 'A' suffix device

Speed Control Resistor Network Equations

R17	=	given
R18	=	$R17\ (\frac{15.5\ V}{V_W} - 1)$
R19	=	$R17\ (\frac{14.8\ V}{V_{spin\ 2}} - 1)$
R20	=	$R17\ (\frac{14.8\ V}{V_{spin\ 1}} - 1) - R19$
R21	=	$R17\ (\frac{14.8\ V}{k.V_W} - 1) - R19 - R20$
R15	=	$R21\ (\frac{K.V_W}{15.5\ V\ (2\text{-}K)})$
R14	=	$R15\ (\frac{15.5\ V}{V_W} - 1)$

The ratio distribute speed to wash speed can be chosen as:

$$\frac{V_{DIST}}{V_{WASH}} \leq 2 = K$$

	S1	S2	S3	S4	$V_{Pin\ 5}$	$V_{Pin\ 6}$
Wash	sc	oc	oc	oc	V_W	0
Distribute	oc	sc	oc	oc	KV_W	V_W
Spin 1	oc	oc	sc	oc	$>KV_W$	$\frac{K}{2}V_W$
Spin 2	oc	oc	oc	sc	$>>KV_W$	$\simeq\frac{K}{2}V_W$

sc = switch closed
oc = switch open

Note:
When changing from one speed to another $V_{Pin\ 5}$ must not be allowed to fall below 80 mV — otherwise the circuit will reset and restart from zero.

The component values given in Figure 4 correspond to:

V_W = 0.7 V
V_D = 1.13 V
$V_{spin\ 1}$ = 5.0 V
$V_{spin\ 2}$ = 11 V
K = 1.6

FIGURE 5 — OPEN LOOP, SOFT START — WITH PROGRAMMED TIME TO MAX. SPEED
($t = C_{Pin\ 7} \cdot 65 \times 10^5$)

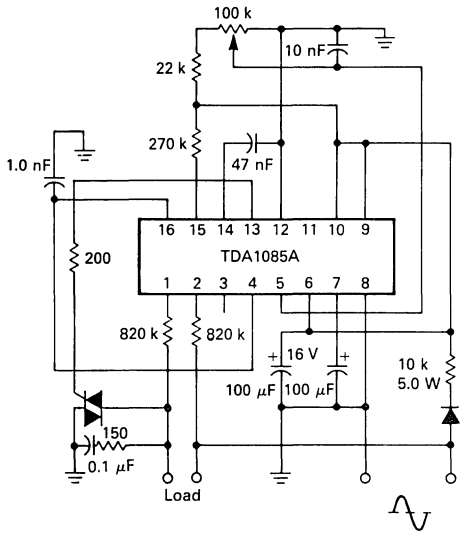
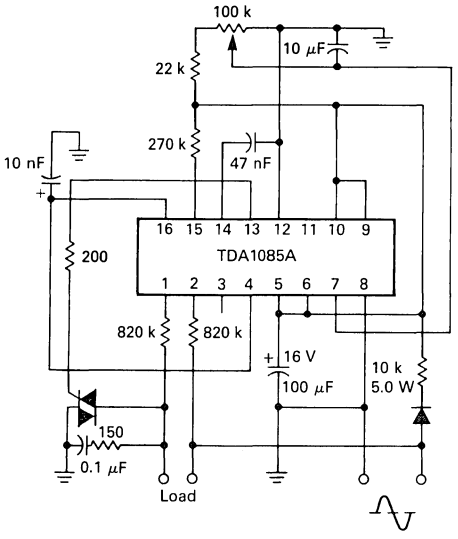


FIGURE 6 — OPEN LOOP, SOFT-START/SOFT-STOP, LIGHTING/INDUCTIVE LOAD CONTROLLER



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

TDA1085C

UNIVERSAL MOTOR SPEED CONTROLLER

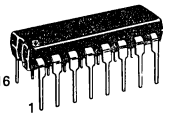
LINEAR INTEGRATED CIRCUIT

4

UNIVERSAL MOTOR SPEED CONTROLLER

The TDA1085C is a phase angle triac controller having all the necessary functions for universal motor speed control in washing machines. It operates in closed loop configuration and provides two ramps possibilities.

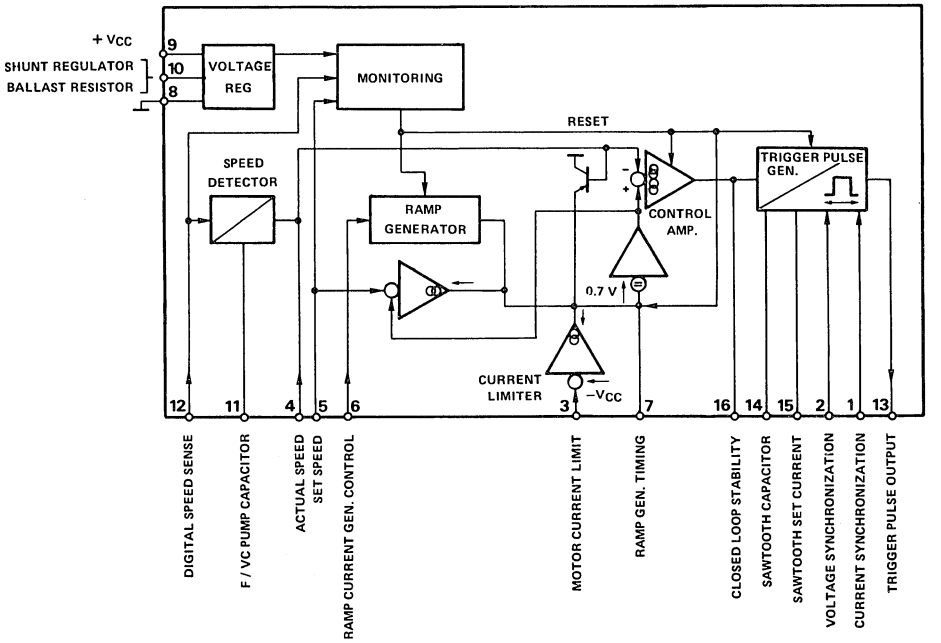
- On-Chip Frequency to Voltage Converter
- On-Chip Ramps Generator
- Soft Start
- Load Current Limitation
- Tachogenerator Circuit Sensing
- Direct Supply from AC Line
- Security Functions Performed by Monitor



PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

FIGURE 1 – BLOCK DIAGRAM AND PIN ASSIGNMENT



MAXIMUM RATINGS (T_A = 25°C, Voltages are referred to pin 8, Ground)

Rating	Symbol	Value	Unit
Power Supply, when externally regulated, V_{Pin9}	V_{CC}	15	V
Maximum Voltage per listed pin Pin 3 Pin 4-5-6-7-13-14-16 Pin 10	V_{pin}	 +5.0 0 to +V_{CC} 0 to +17	V
Maximum Current per listed pin Pin 1 and 2 Pin 3 Pin 9 (V_{CC}) Pin 10 shunt regulator Pin 12 Pin 13	I_{pin}	 −3.0 to +3.0 −1.0 to +0 15 35 −1.0 to +1.0 −200	mA
Maximum Power Dissipation	P_D	1.0	W
Junction to Air Thermal Resistance	$R_{\theta JA}$	65	°C/W
Operating Junction Temperature	T_A	−10 to +120	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REGULATOR					
Internally Regulated Voltage (V_{Pin9}) (I_{Pin7} = 0, I_{Pin9} + I_{Pin10} = 15 mA, I_{Pin13} = 0)	V_{CC}	15	15.3	15.6	V
V_{CC} Temperature Factor	TF	—	−100	—	ppm/°C
Current Consumption (I_{Pin9}) (V_9 = 15 V, V_{12} = V_8 = 0, I_1 = I_2 = 100 μA, all other pins not connected)	I_{CC}	—	4.5	6.0	mA
V_{CC} Monitoring Enabling Level Disable Level	V_{CC} EN V_{CC} DIS	— —	V_{CC}−0.4 V_{CC}−1.0	— —	V
RAMP GENERATOR					
Reference Speed Input Voltage Range	V_{Pin5}	0.08	—	13.5	V
Reference Input Bias Current	−I_{Pin5}	0	0.8	1.0	μA
Ramp Selection Input Bias Current	−I_{Pin6}	0	—	1.0	μA
Distribution Starting Level Range	V_{DS}	0	—	2.0	V
Distribution Final Level V_{Pin6} = 0.75 V	V_{DF}/V_{DS}	2.0	2.09	2.2	
High Acceleration Charging Current V_{Pin7} = 0 V V_{Pin7} = 10 V	−I_{Pin7}	 1.0 1.0	 — 1.2	 1.7 1.4	mA
Distribution Charging Current V_{Pin7} = 2.0 Volts	−I_{Pin7}	4.0	5.0	6.0	μA

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT LIMITER					
Limiter Current Gain — I_{Pin7}/I_{Pin3} (I_{Pin3} = −300 μA)	C_g	130	180	250	
Detection Threshold Voltage I_{Pin3} = −10 μA	$V_{Pin3\ TH}$	50	65	80	mV
FREQUENCY TO VOLTAGE CONVERTER					
Input Signal "Low Voltage" Input Signal "High Voltage" Monitoring Reset Voltage	$V_{12\ L}$ $V_{12\ H}$ $V_{12\ R}$	−100 +100 5.0	— — —	— — —	mV mV V
Negative Clamping Voltage I_{Pin12} = −200 μA	$-V_{12\ CL}$	—	0.6	—	V
Input Bias Current	$-I_{Pin12}$	—	25	—	μA
Internal Current Source Gain $G = \frac{I_{Pin4}}{I_{Pin11}}$, $V_{Pin4} = V_{Pin11} = 0$	G.0	9.5	—	11	
Gain Linearity versus Voltage on Pin 4 ($G_{8.6}$ = Gain for V_{Pin4} = 8.6 Volts) V_4 = 0 V V_4 = 4.3 V V_4 = 12 V	$G/G_{8.6}$	 1.04 1.015 0.965	 1.05 1.025 0.975	 1.06 1.035 0.985	
Gain Temperature Effect (V_{Pin4} = 0)	TF	—	350	—	ppm/°C
Output Leakage Current (I_{Pin11} = 0)	$-I_{Pin4}$	0	—	100	nA
CONTROL AMPLIFIER					
Actual Speed Input Voltage Range	V_{Pin4}	0	—	13.5	V
Input Offset Voltage $V_{Pin5} - V_{Pin4}$ (I_{Pin16} = 0, V_{Pin16} = 3.0 and 8.0 Volts)	V_{off}	0	—	50	mV
Amplifier Transconductance $(I_{Pin16}/\Delta\ (V_5 - V_4))$ (I_{Pin16} = + and −50 μA, V_{Pin16} = 3.0 Volts)	T	270	340	400	μA/V
Output Current Swing Capability Source Sink	I_{Pin16}	 −200 50	 −100 100	 −50 200	μA
Output Saturation Voltage	$V_{16\ sat}$	—	—	0.8	V
TRIGGER PULSE GENERATOR					
Synchronization Level Currents Voltage Line Sensing Triac Sensing	 I_{Pin2} I_{Pin1}	 — —	 ±50 ±50	 ±100 ±100	μA
Trigger Pulse Duration (C_{Pin14} = 47 nF, R_{Pin15} = 270 kΩ)	T_p	—	55	—	μs
Trigger Pulse Repetition Period, conditions as a.m.	T_R	—	220	—	μs
Output Pulse Current $V_{Pin13} = V_{CC}$ −4.0 Volts	$-I_{Pin13}$	180	192	—	mA
Output Leakage Current V_{Pin13} = −3.0 Volts	$I_{13\ L}$	—	—	30	μA
Full Angle Conduction Input Voltage	V_{14}	—	11.7	—	V
Saw Tooth "High" Level Voltage	$V_{14\ H}$	12	—	12.7	V
Saw Tooth Discharge Current, I_{Pin15} = 100 μA	I_{Pin14}	95	—	105	μA

GENERAL DESCRIPTION

The TDA 1085C triggers a triac accordingly to the speed regulation requirements. Motor speed is digitally sensed by a tachogenerator and then converted into an analog voltage.

The speed set is externally fixed and is applied to the internal linear regulation input after having been submitted to programmable acceleration ramps. The overall result consists in a full motor speed range with two acceleration ramps which allow efficient washing machine control (Distribute function).

Additionnally, the TDA 1085C protects the whole system against AC line stop or variations, overcurrent in the motor and tachogenerator failure.

INPUT/OUTPUT FUNCTIONS
(Referred to Figures 1 and 8)

VOLTAGE REGULATOR — (pins 9 and 10) This is a parallel type regulator able to sink a large amount of current and offering good characteristics. Current flow is provided from AC line by external dropping resistors R1, R2, and rectifier: This half wave current is used to feed a smoothering capacitor, the voltage of which is checked by the IC.

When V_{CC} is reached, the excess of current is derived by another dropping resistor R10 and by pin 10. These three resistors must be determined in order:

- to let 1mA flow through pin 10 when AC line is minimum and V_{CC} consumption is maximum (fast ramps and pulses present).
- to let V_{10} reach 3V when AC line provides maximum current and V_{CC} consumption is minimum (no ramps and no pulses).
- all along the main line cycle, the pin 10 dynamic range must not be exceeded unless loss of regulation.

An AC line supply failure would cause shut down.

The double capacitive filter built with R_1 and R_2 gives an efficient V_{CC} smoothing and helps to remove noise from set speeds.

SPEED SENSING — (pins 4-11-12) The IC is compatible with an external analog speed sensing: its output must be applied to pin 4, and pin 12 connected to pin 8.

In most of the applications it is more convenient to use a digital speed sensing with an unexpensive tachogenerator which doesn't need any tuning. During every positive cycle at pin 12, the capacitor $C_{pin\ 11}$ is charged to almost V_{CC} and during this time, pin 4 delivers a current which is 10 time the one charging $C_{pin\ 11}$. The current source gain is called G and is tightly specified, but nevertheless requires an adjustment on $R_{pin\ 4}$. The current into this resistor is proportional to $C_{pin\ 11}$ and to the motor speed; being filtered by a capacitor, $V_{pin\ 4}$ becomes smoothered and represents the "true actual motor speed".

To maintain linearity into the high speed range, it is important to verify that $C_{pin\ 11}$ is fully charged: the internal source on pin 11 has 100 KΩ impedance. Nevertheless $C_{pin\ 11}$ has to be as high as possible as it has a large influence on FV/C temperature factor. A 470 KΩ resistor between pins 11 and 9 reduces leakage currents and temperature factor as well, down to neglectable effects.

Pin 12 has also a monitoring function: when its voltage is above 5V, the trigger pulses are inhibited and the IC is reset. It also senses the tachogenerator continuity and in case of any circuit aperture, it inhibits pulse, avoiding the motor to run out of control. In the TDA 1085C, pin 12 is negatively clamped by an internal diode which removes the necessity of the external one used in the former circuit.

RAMP GENERATOR — (pins 5-6-7) The true Set Speed value taken in consideration by the regulation is the output of the ramp generator (pin 7). With a given value of speed set input (pin 5), the ramp generator charges an external capacitor $C_{pin\ 7}$ up to the moment $V_{pin\ 5}$ (set speed) equals $V_{pin\ 4}$ (true speed), see fig. 2. The IC has an internal charging current source of 1.2mA and delivers it from 0 to 12 V at pin 7. It is the high acceleration ramp (5 seconds typ.) which allows rapid motor speed changes without excessive strains on the mechanics. The TDA 1085C offers in addition the possibility to break this high acceleration with the introduction of a low acceleration ramp (called Distribution) by reducing the pin 7 source current down to 5 µA under pin 6 full control, as shown by following conditions:

- Presence of high acceleration ramp $V_{pin\ 5} > V_{pin\ 4}$
- Distribution occurs in the $V_{pin\ 4}$ range (true motor speed) defined by $V_{pin\ 6} \leqq V_{pin\ 4} \leqq 2V_{pin\ 6}$

For two fixed values of $V_{pin\ 5}$ and $V_{pin\ 6}$, the motor speed will have high acceleration, excluding the time for $V_{pin\ 4}$ to go from $V_{pin\ 6}$ to two times this value, high acceleration again, up to the moment the motor has reached the set speed value, at which it will stay, see fig. 3.

Should a reset happen (whatever the cause would be), the above mentionned successive ramps will be fully reprocessed from 0 to the max. speed. If $V_{pin\ 6} = 0$, only the high acceleration ramp occurs.

To get a real zero speed position, pin 5 has been designed in such a way that its voltage from 0 to 80 mV is interpreted as a true zero. As a consequence, when changing the speed set position, the designer must be sure that any transient zero would not occur: if any, the entire circuit will be reset.

As the voltages applied by pins 5 and 6, are derived from the internal voltage regulator supply and pin 4 voltage is also derived from the same source, motor speed, which is determined by the ratios between above mentioned voltages, is totally independent from V_{CC} variations and temperature factor.

CONTROL AMPLIFIER — (pin 16) It amplifies the difference between true speed (pin 4) and set speed (pin 5), through the ramp generator. Its output available at pin 16 is a double sense current source with a max. capability of ± 100 µA and a specified transconductance (340 µA/v.typ.). Pin 16 drives directly the trigger pulse generator, and must be loaded by an electrical network which compensates the mechanical characteristics of the motor and its load, in order to provide stability in any condition and shortest transient response, see fig. 4.

This network must be adjusted experimentally.

In case of a periodic torque variations, pin 16 provides directly the phase angle oscillations.

TRIGGER PULSE GENERATOR — (pins 5 1-2-13-14-15)
This circuit performs four functions:

- The conversion of the control amplifier DC output level to a proportionnal firing angle at every main line half cycle.
- The calibration of pulse duration.
- The repetition of the pulse if the triac fails to latch on if the current has been interrupted by brush bounce.
- The delay of firing pulse until the current crosses zero at wide firing angles and inductive loads.

$R_{pin\ 15}$ programs the pin 14 discharging current. Saw-tooth signal is then fully determined by R15 and C14 (usually 47 nF). Firing pulse duration and repetition period are in inverse ratio to the saw-tooth slope.

Pin 13 is the pulse output and an external limiting resistor is mandatory. Max current capability is 200 mA.

CURRENT LIMITER — (pin 3) Safe operation of the motor and triac under all conditions is ensured by limiting the peak current. The motor current develops an alternative voltage in the shunt resistor (0.05 ohm in fig. 4). The negative half waves are transferred to pin 3 which is positively preset at a voltage determined by resistors R_3 and R_4. As motor current increases, the dynamical voltage range of pin 3 increases and when pin 3 becomes slightly negative in respect of pin 8 a current starts to circulate in it. This current, amplified typically 180 times, is then used to discharge pin 7 capacitor and, as a result, reduces firing angle down to a value where an equilibrium is reached. The choice of resistors R_3, R_4 and shunt determines the magnitude of the discharge current signals on C_{pin7}.

Notice that the current limiter acts only on peak Triac current.

APPLICATION NOTES
(Referred to Figure 4)

PRINTED CIRCUIT LAYOUT RULES
In the common applications, where TDA1085C is used, there is on the same board, presence of high voltage, high currents as well as low voltage signals where millivolts count. It is of first magnitude importance to separate them each other and to respect following rules:

- Capacitors decoupling pins which are the inputs of the same comparator, must be physically close to the IC, close to each other and grounded in the same point.
- Ground connexion for tachogenerator must be directly connected to pin 8 and should ground only the tacho. In effect the latter is a first magnitude noise generator due to its proximity of the motor which induces high dø/dt signals.
- The ground pattern must be in the "star style", in order to fully eliminate power currents flowing in the ground network devoted to capacitors decoupling sensitive pins: (4-5-7-11-12-14-16).

As an example, fig. 5 presents a PC board pattern which concerns the group of sensitive pins and their associated capacitors into which the a.m. rules have been implemented. Notice the full separation of "Signal World" from "Power" one by line AB and their communication by a unique strip.

These rules will lead to much satisfactory volume production in the sense that speed adjustment will stay valid in the entire speed range.

POWER SUPPPLY
As dropping resistor dissipates noticeable power, it is necessary to reduce the I_{cc} needs down to a minimum. Triggering pulses, if a certain number of repetition is in reserve to cope with motor brush wearing at end of its life, are the largest I_{cc} user. Classical worst case configuration have to be considered to select dropping resistor. In addition the parallel regulator must be always into its dynamic range, i.e. $I_{pin\ 10}$ over 1 mA and $V_{pin\ 10}$ over 3 volt in any extreme configuraton. The double filtering cell is mandatory.

TACHOGENERATOR CIRCUIT
The tacho signal voltage is proportional to the motor speed. Stability considerations, in addition, require a RC filter the pole of which must be looked at. The combination of both elements yield a constant amplitude signal on pin 12 in most of the speed range. It is recommended to verify this maximum amplitude to be within 1 volt peak in order to have the largest signal/noise ratio without resetting the integrated circuit (which occurs if $V_{pin\ 12}$ reaches 5.5 V). It must be also verified that the pin 12 signal is approximately balanced between "High" (over 300 mV) and "Low". A 8 poles tacho is a minimum for low speed stability and a 16 poles is even better.

The RC pole of the tacho circuit should be chosen within 30 Hz in order to be as far as possible from the 150 Hz which corresponds to the AC line 3rd harmonic generated by the motor during starting procedure. In addition, a high value resistor coming from V_{cc} introduces a positive offset at pin 12, removes noise to be interpreted as a tacho signal. This offset should be designed in order to let pin 12 to reach at least − 200 mV (negative voltage) at the lowest motor speed. We remember the necessity of an individual tacho ground connection.

FREQUENCY TO VOLTAGE CONVERTER — F V/C
$C_{pin\ 11}$ has a recommended value of 820 pF for 8 poles tachos and max. motor rpm of 15000, and $R_{Pin\ 11}$ must be always 470 K.
$R_{Pin\ 4}$ should be choosen to deliver within 12 volts at maximum motor speed in order to maximize signal/noise ratio. As the FV/C ratio as well as the $C_{pin\ 11}$ value are dispersed, $R_{Pin\ 4}$ must be adjustable and should be made of a fixed resistor in serice with a trimmer representing 25% of the total. Adjustment would become easier.
Once adjusted, for instance at maximum motor speed, the F V/C presents a residual non linearity; the conversion factor (mV per R.P.M.) increases by within 7.7% as speed tends to zero. The guaranteed dispersion of the latter being very narrow, a maximum 1% speed error is guaranteed if during pin 5 network design the small set vlues are modified, once for ever, according this increase.

The following formulae give $V_{pin\ 4}$:

$$V_{Pin\ 4} = G.0 \cdot (V_{CC} - V_a) \cdot C_{Pin\ 11} \cdot R_4 \cdot f \cdot \frac{1}{\left(1 + \frac{120k}{R_{Pin11}}\right)}$$

In Volts ·
$G.0 \cdot (V_{CC} - V_a) \simeq 140$
$V_a = 2.0\ V_{BE}$
$120k = R_{int}$, on Pin 11

SPEED SET — (pin 5) Upon designer choice, a set of external resistors apply a serie of various voltages corresponding to the various motor speeds. When switching external resistors, verify that a voltage below 80 mV in never applied to pin 5, if no, a full circuit reset will occur.

RAMPS GENERATOR — (pin 6) If only a high acceleration ramp is needed, connect pin 6 to ground.

When a Distribute ramp should occur, pre-set a voltage on pin 6 to which corresponds the motor speed starting ramp point. Distribution (or low ramp) will continue up to the moment the motor speed would have reached twice the starting value.

The ratio of two is imposed by the IC. Nevertheless it could be externally changed downwards (fig. 6) or upwards (fig. 7).

The distribution ramp can be shortened by an external resistor from V_{CC} charging $C_{pin\ 7}$, adding its current to the internal 5 μA generator.

POWER CIRCUITS
Triac Triggering pulse amplitude must be determined by Pin 13 resistor according the needs in Quadrant IV. Trigger pulses duration can be disturbed by noise signals, generated by the triac itself, which interfere within pins 14 and 16, precisely those which determine it. While easily visible this effect is harmless.

Triac must be protected from high AC line dV/dt during external disturbances by 100 nF × 100 Ω network.

Shunt resistor must be as non selfic as possible. It can be made locally by Constantan alloy wiring.

When the load is a DC fed universal motor through a rectifier bridge, the triac must be protected from commutating dV/dt by a 1 to 2 mH coil in serie with MT_2.

Synchronisation functions are performed by resistors sensing AC line and triac conduction. 820 K values are usual but could be reduced down to 330 K in order to detect the Zeros with accuracy and to reduce the residual DC line component below 20 mA.

CURRENT LIMITATION
The current limiter starts to discharge pin 7 capacitor (reference speed) as Motor current reaches the designed threshold level. The loop gain is determined by the resistor connecting pin 3 to the serie shunt. Experience has shown that its optimal value for a 10 A rms limitation is within 2 KΩ. Pin 3 input has a sensitivity in current which is limited to reasonable values and should not react to spikes.

If not used, pin 3 must be connected to a max. positive voltage of 5 V rather to be left open.

LOOP STABILITY
The pin 16 network is predominant and must be adjusted experimentally during module development. The values indicated in fig. 4 are typical for washing machines applications but accept large modifications from one model to another. R16, it is the sole restriction, should not be below 33 k otherwise slew rate limitation will cause large transient errors for load steps.

FIGURE 2 — ACCELERATION RAMP

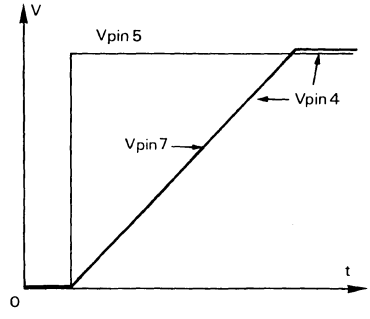


FIGURE 3 — PROGRAMMABLE DOUBLE ACCELERATION RAMP

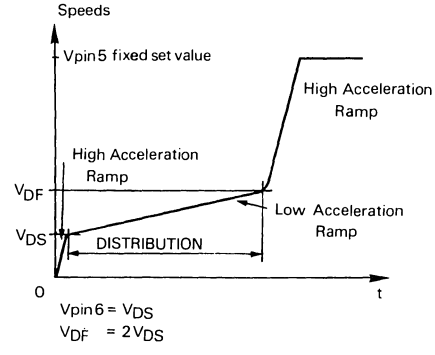
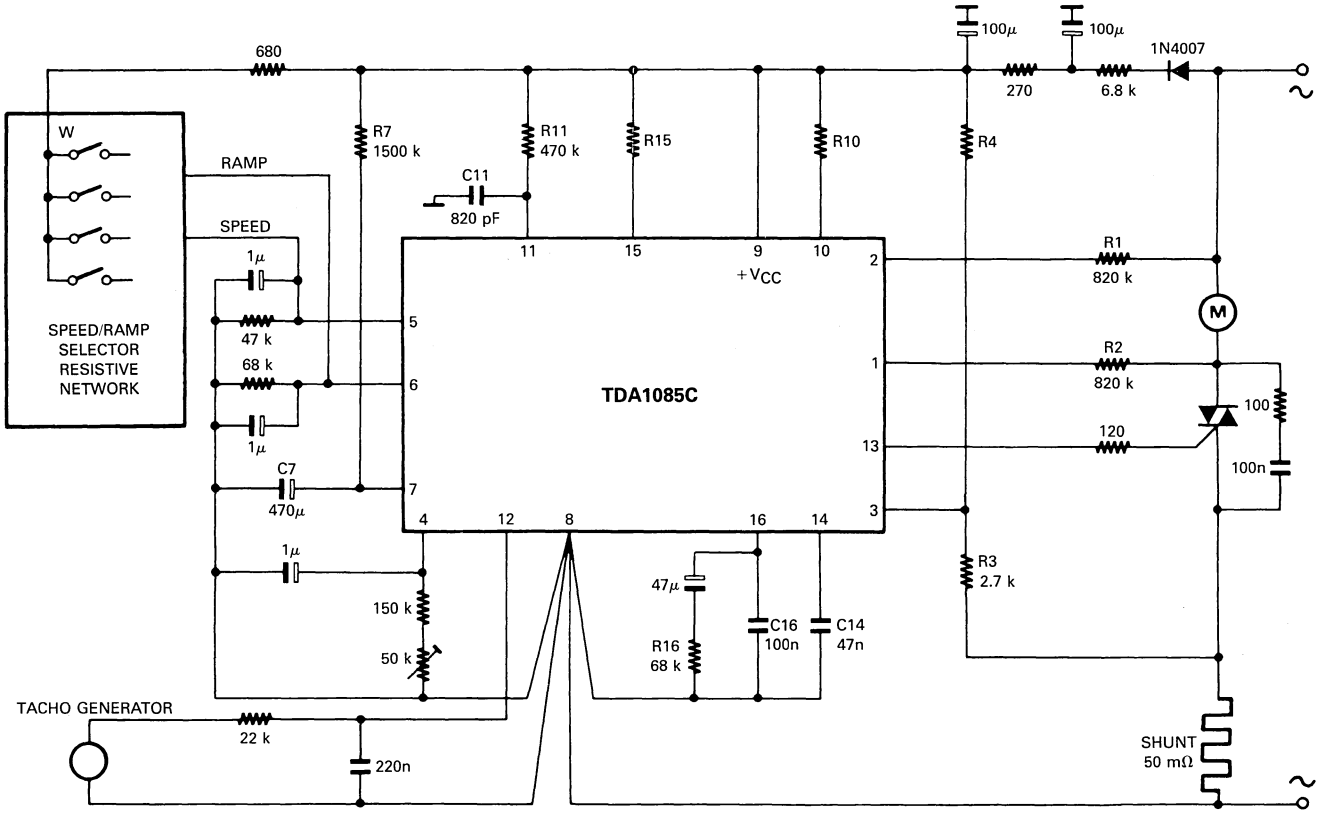


FIGURE 4 — BASIC APPLICATION CIRCUIT



Current limitation: 10 A adjusted by R_4 experimentally

Ramps High acceleration: 3200 rpm per second

Distribution ramp: 10 s from 850 to 1300 rpm

Speeds:	**Pin 5 voltage**	**Set:**
Wash 800 rpm	609 mV	Including nonlinearity corrections
Distribution 1300	996 mV	Including nonlinearity corrections
Spin 1: 7500	5,912 V	Including nonlinearity corrections
Spin 2: 15,000	12,000 V	Adjustment point

Motor Speed Range: 0 to 15,000 rpm

Tachogenerator 8 poles
delivering 30 V peak to peak at 6000 rpm, in open circuit

FV/C Factor: 8 mV per rpm (12 V full speed) C_{pin11} = 680 pF V_{CC} = 15.3 V

TRIAC MAC15A-8 15 A 600 V

Igt min = 90 mA to cover Quad IV at −10°C

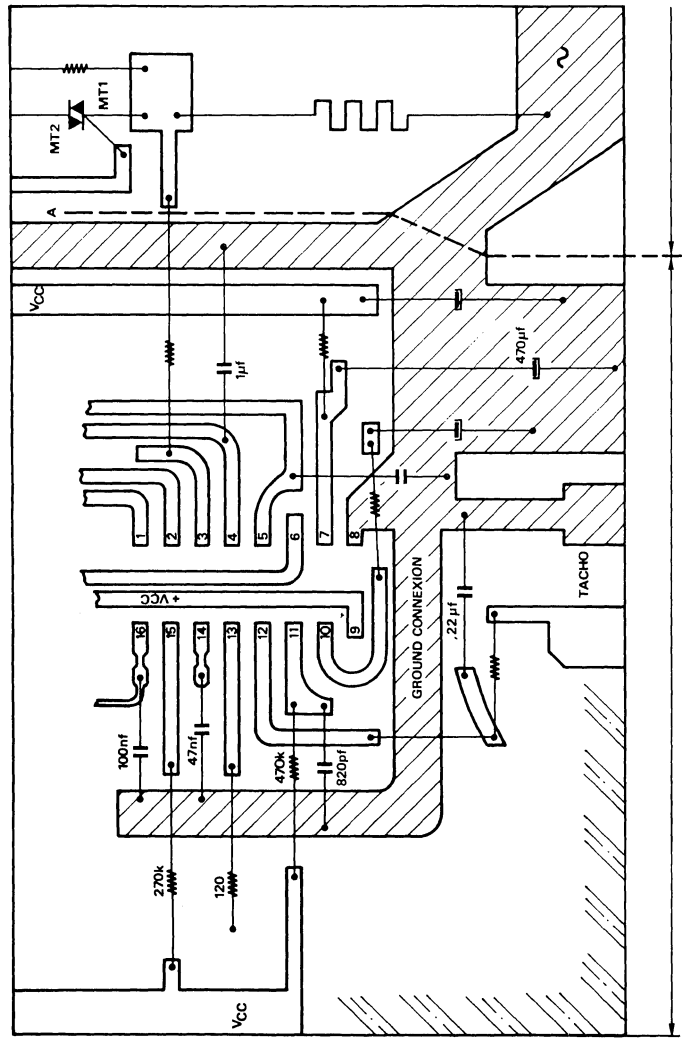


FIGURE 5 — PC BOARD LAYOUT

4

FIGURE 6 – DISTRIBUTION SPEED k < 2

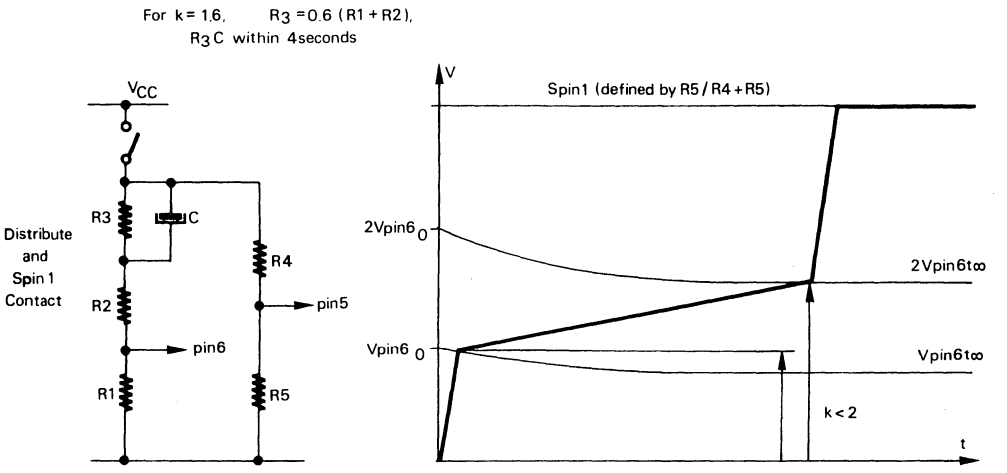
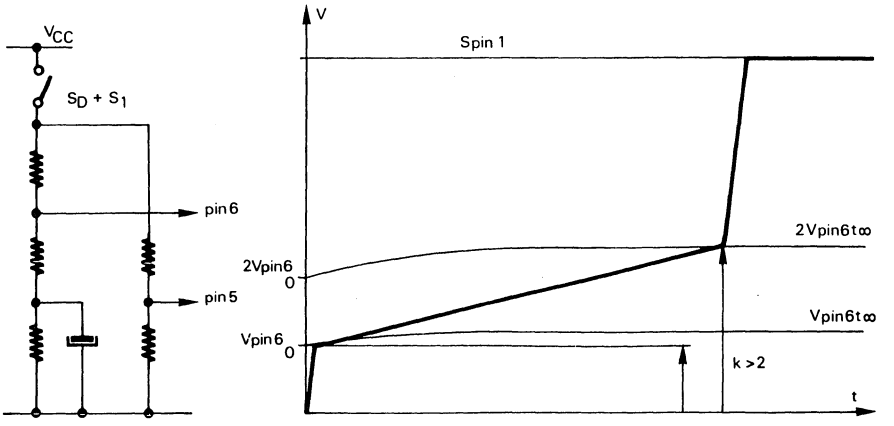


FIGURE 7 – DISTRIBUTON SPEED k > 2



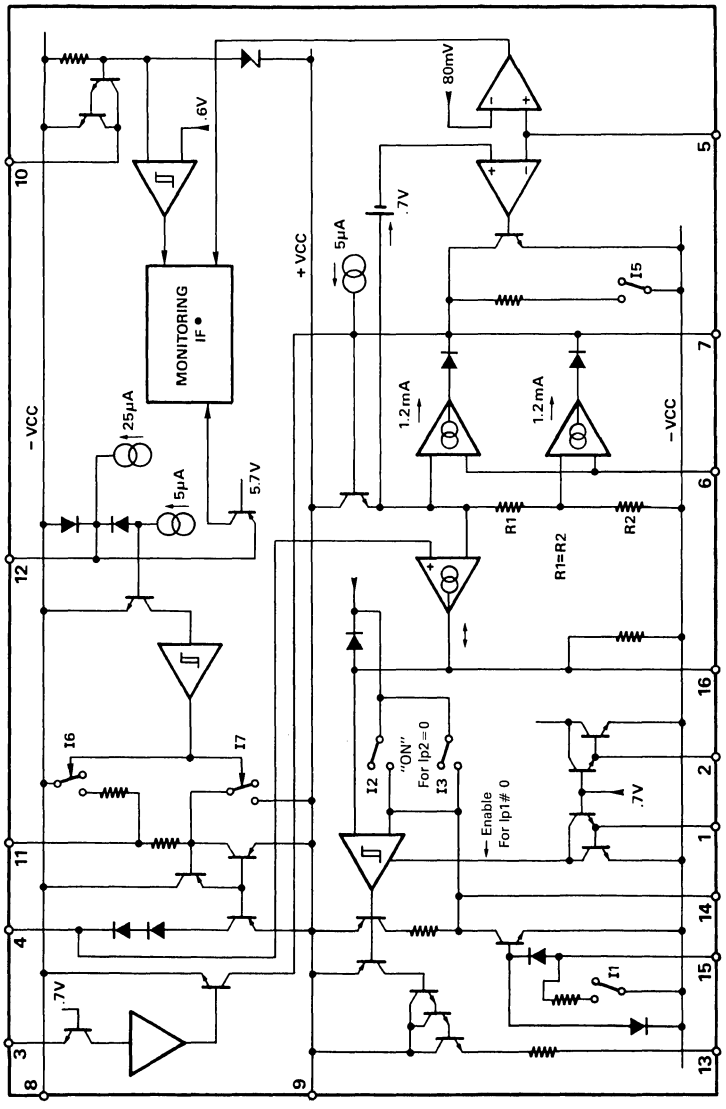


FIGURE 8 — SIMPLIFIED SCHEMATIC

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

TDA1185A

TRIAC PHASE ANGLE CONTROLLER

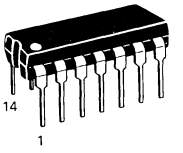
4

The TDA1185A generates controlled TRIAC triggering pulses and allows tachless speed stabilization of universal motors by an integrated positive feedback function. Typical applications are power hand tools, vacuum cleaners, mixers, light dimmer and other small appliances.

- Supply Power Obtained From AC Line
- Can Be Used with 220 V/50 Hz or 110 V/60 Hz
- Low Count/Cost External Components
- Optimum TRIAC Firing (2nd and 3rd Quadrants)
- Repetitive Trigger Pulses When TRIAC Current is Interrupted by Motor Brush Bounce
- TRIAC Current Sensing to Allow Inductive Loads
- Programmable Soft-Start
- Power Failure Detection and General Circuit Reset
- Low Power Consumption: 6.0 mA

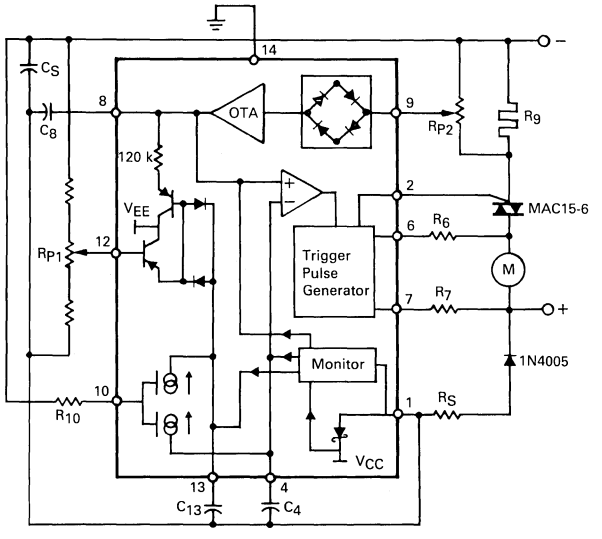
TRIAC PHASE ANGLE CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

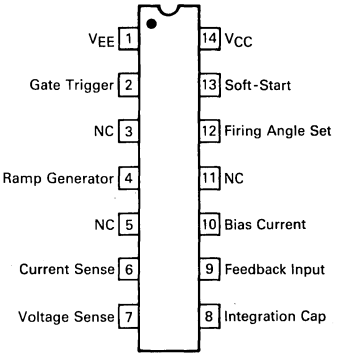


PLASTIC PACKAGE
CASE 646

FIGURE 1 — TYPICAL SYSTEM CONFIGURATION



PIN CONNECTIONS



MAXIMUM RATINGS (Voltages are referenced to Pin 14 (ground) unless otherwise noted)

Rating	Symbol	Value	Unit
Maximum Voltage Range per Listed Pin	V_{Pin}		V
Pins 3-5-11 (not connected)		−20 to +20	
Pins 4-8-13		$-V_{CC}$ to 0	
Pin 2		−3.0 to +3.0	
Maximum Positive Voltage (No minimum value allowed; see current ratings)	$V_{Pin\ 12}$ $V_{Pin\ 1}$	0 0.5	
Maximum Current per Listed Pin	I_{Pin}		
Pin 1		±20	mA
Pins 6 and 7		±2.0	mA
Pin 9		±0.5	mA
Pin 10		±300	μA
Pin 12		−500	μA
Maximum Power Dissipation (@ T_A = 25°C)	P_D	250	mW
Maximum Junction to Ambient Thermal Resistance	$R_{\theta JA}$	100	°C/W
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, voltages are referenced to Pin 14 (ground), unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply					
Zener Regulated Voltage, ($V_{Pin\ 1}$) $I_{Pin\ 1}$ = 2.0 mA	$-V_{CC}$	−9.6	−8.6	−7.6	V
Circuit Current Consumption, $I_{Pin\ 1}$					
$V_{Pin\ 1}$ = −6.0 V, $I_{Pin\ 2}$ = 0 A	$-I_{CC}$	−2.0	−1.0	—	mA
Monitoring Enable Supply Voltage (V_{EN})	$V_{Pin\ 1EN}$	V_{CC} + 0.2	—	V_{CC} + 0.5	V
Monitoring Disable Supply Voltage (V_{DIS})	$V_{Pin\ 1DIS}$	V_{EN} + 0.12	—	V_{EN} + 0.3	
Phase Set					
Control Voltage Static Offset $V_{Pin\ 8}$ − $V_{Pin\ 12}$	V_{off}	1.2	—	2.0	V
Pin 12 Input Bias Current	$I_{Pin\ 12}$	−200	—	0	nA
$V_{Pin\ 4}$ − $V_{Pin\ 12}$ Residual Offset		—	180	—	mV
Soft-Start	$I_{Pin\ 13}$	−17	−14	−11	μA
Capacitor Charging Current					
$R_{Pin\ 10}$ = 100 kΩ, $V_{Pin\ 13}$ from $-V_{CC}$ to −3.0 V					
Sawtooth Generator					
Sawtooth Capacitor Discharge Current					
R_{10} = 100 kΩ $V_{Pin\ 4}$ from −2.0 to −6.0 V	$I_{Pin\ 4}$	67	70	73	μA
Capacitor Charging Current	$I_{Pin\ 4}$	−10	—	−1.5	mA
Sawtooth "High" Voltage ($V_{Pin\ 4}$)	V_{HTH}	−2.5	−1.6	−1.0	V
Sawtooth Minimum "Low" Voltage ($V_{Pin\ 4}$)	V_{LTH}	—	−7.1	—	V
Positive Feedback					
Pin 9 Input Bias Current, $V_{Pin\ 9}$ = 0	$I_{Pin\ 9}$	—	2 x $I_{Pin\ 10}$	—	
Programming Pin Voltage Related to Pin 1	$V_{Pin\ 10}$	1.0	1.25	1.5	V
Transfer Function Gain $\Delta V_{Pin\ 8}/\Delta V_{Pin\ 9}$					
R_{10} = 100 kΩ, $\Delta V_{Pin\ 9}$ = 50 mV	A	—	75	—	
R_{10} = 270 kΩ, $\Delta V_{Pin\ 9}$ = 50 mV	A	—	36	—	
Pin 8 Output Internal Impedance	$Z_{Pin\ 8}$	—	120	—	kΩ
Trigger Pulse Generator					
Output Current (Sink) $V_{Pin\ 2}$ = 0 V	$I_{Pin\ 2}$	60	—	80	mA
Output Leakage Current $V_{Pin\ 2}$ = +2.0 V		—	—	4.0	μA
Output Pulse Width					
C_4 = 47 nF R_{10} = 270 kΩ	t_P	—	55	—	μs
Output Pulse Repetition Period					
C_4 = 47 nF R_{10} = 270 kΩ	t	—	420	—	μs
Current Synchronization Threshold Levels $I_{Pin\ 6}$, $I_{Pin\ 7}$	I_{SYNC}	−40	—	+40	μA

PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	V_{EE}	This pin is the negative supply for the chip and is clamped at −8.6 V by an internal zener.
2	Gate Trigger Pulse	This pin supplies −1.0 V TRIAC trigger pulse at twice the line frequency.
3	NC	Not connected
4	Ramp Generator	The value of the capacitor at this pin determines the slope of the ramp.
5	NC	Not connected
6	Current Sense	This pin senses if the TRIAC is on, and if so, will disable the gate trigger pulse.
7	Voltage Sense	The internal timing of the chip is set by the frequency of the voltage at this pin.
8	Integration Capacitor	This pin is the output of the feedback and the variation in voltage is averaged out by the capacitor.
9	Feedback Input	The change in load current is detected by the change in voltage across R9.
10	Current Program	The bias current for the circuit is determined by the resistor value at this pin.
11	NC	Not connected
12	Phase Angle Set	The voltage at this pin sets the no-load firing angle.
13	Soft-Start	The firing angle is slowly increased from 180° to the set value of Pin 12.
14	V_{CC}	Ground

4

INTRODUCTION

The Motorola TDA1185A generates trigger pulses (Pin 2) for TRIAC control of power into an AC load. The TRIAC trigger pulse is determined by generating a ramp voltage (Pin 4) synchronized to twice the AC line frequency and compared to an external set voltage (Pin 12) representing the conduction angle. Gate pulses are negative (sink current) and thus the TRIAC is driven into its most effective quadrants (Q2–Q3).

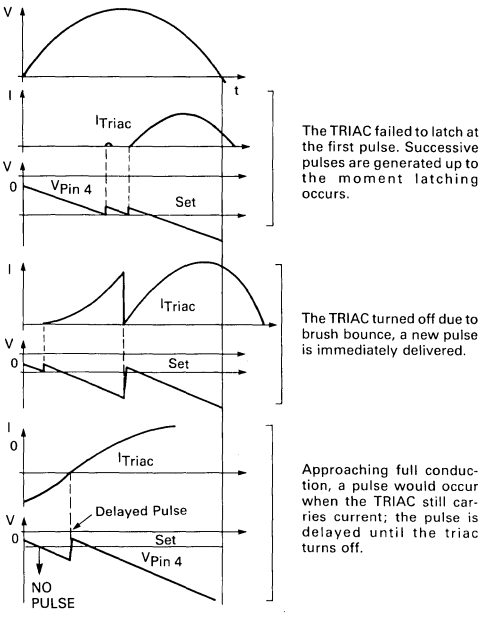
If the load is a Universal motor (the speed of which decreases as torque increases), the TDA1185A allows to increase the conduction angle proportionally to the motor current, sensed (Pin 9) by a low value resistor in series with the load.

FUNCTIONAL DESCRIPTION

DC POWER SUPPLY — DC power is directly derived from the AC line through a 2.0 watt resistor, half-wave rectifier and filtering capacitor circuit. The V_{EE} voltage is internally regulated by an integrated zener. Referenced to ground (Pin 14), the power supply voltage is −8.6 V. The TDA1185A internal consumption is 6.0 mA.

TRIGGER PULSE GENERATOR — It delivers a 60 mA minimum sink current pulse (Pin 2) through an internally short circuit protected output. Pulse width is roughly proportional to $R_{10} \times C_4$ and is repeated every 420 μs if TRIAC fails to latch or is switched off by brush bounce. With inductive loads, the current lags in respect to the voltage. Pin 6 delays the triggering pulse up to the moment the TRIAC is off, in order to prevent erratic power control (see Figure 2).

FIGURE 2 — MULTIPULSE GENERATION DELAYED PULSE



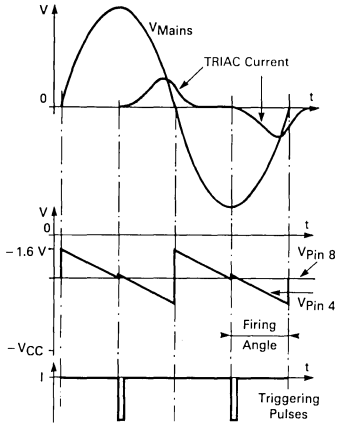
RAMP GENERATOR — A constant current sink discharges capacitor C_4 producing a negative voltage ramp synchronized with the main line. Pin 4 voltage is reset to −1.6 volts at every AC line zero crossing (see Figure 3) and ramps down to −7.1 volts. The constant current sink is externally programmable by R_{10} using the equation below.

$$I_4 = I_{10} \pm 5\%$$

$$I_{10} = \frac{|V_{EE} + 1.25|}{R_{10}}$$

MAIN COMPARATOR — Its role is to determine the trigger pulse which occurs when the ramp voltage equals the phase angle set voltage at Pin 12. Fixed phase angle set voltage values lead to a constant TRIAC conduction angle unless positive current feedback (Pin 9) is connected or the Soft-Start capacitor (Pin 13) is not charged.

FIGURE 3 — TRIGGERING PULSE TIMING



SOFT-START — The TDA1185A allows the user to avoid any abrupt inrush of current into the load. This provides protection for fragile loads, light bulbs or tubes. Another advantage is that the AC line disturbance is minimized.

The conduction angle is established from zero to the set value at Pin 12 according to a voltage ramp generated by a constant current delivered to C_{13}. The value of current I_{13} can be expressed by the following equation:

$$I_{13} = 0.2 \times I_{10} \pm 10\%$$

The voltage ramp lasts as long as V_{13} is lower than the set voltage V_{12}. Upon reset, V_{13} is forced to V_{EE} as shown in Figure 4. If the load is a universal motor, it will not turn until a minimum conduction angle is achieved to overcome friction. The time the voltage ramp requires to reach its threshold value is considered "dead" time, and can be eliminated by an appropriate series resistor at Pin 13. The voltage drop developed by I_{13} thru the resistor causes the conduction angle to immediately reach the threshold value and have the Soft-Start function without dead time (see Figure 5).

FIGURE 4 — SOFT START

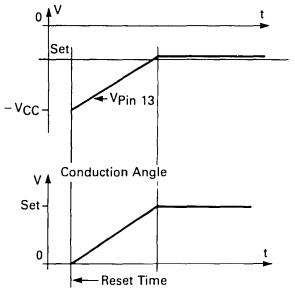


FIGURE 5 — SOFT-START WITHOUT DEAD TIME

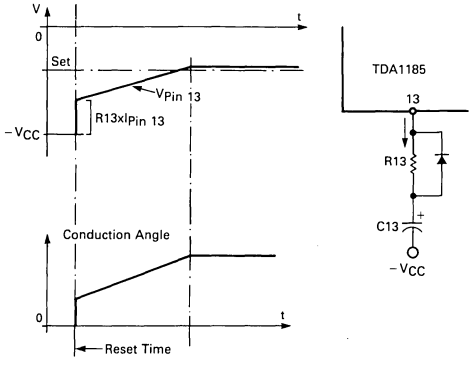
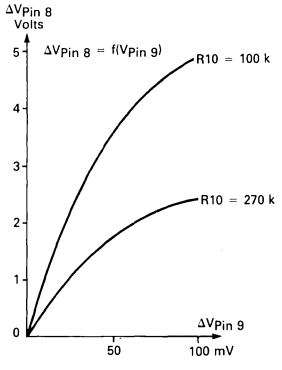


FIGURE 6 — TRANSFER FUNCTION



POSITIVE CURRENT FEEDBACK — The Universal motor speed drops as load increases. To maintain the speed, the TRIAC conduction angle must be increased. For this purpose, Pin 9 senses the motor current as a **voltage** developed in a low value resistor, R_9, amplifies, rectifies and adds it internally to the set voltage at Pin 12. Any voltage variation at the output of the feedback, Pin 8, is smoothed out by capacitor C_8. The transfer function, $\Delta V_8 = f(\Delta V_9)$, is shown in Figure 6.

The gain in the linear region is dependent on R_{10}. The voltage transferred to Pin 8 is proportional to the current RMS value, as motor current is not far from a sine wave. This averaging effect is shown in Figure 7.

With large amplitude signals at Pin 9, the change in voltage at Pin 8 reaches a maximum value. This saturation effect limits the maximum conduction angle increase. This effect is illustrated in Figure 8 where the total Pin 8 voltage can be written as follows:

$$V_8 = V_{12} + f(|V_9|, R_{10}) + 1.25$$

The effect of the feedback is illustrated in Figure 9.

MONITORING — A central logic block performs the ENABLE/DISABLE function of the IC with respect to power supply voltage. Under DISABLE conditions, Pin 4, 8, 12 and 13 are forced to appropriate voltages to prepare for the next reset. Refer to the block diagram in Figure 10.

APPLICATION CONSIDERATIONS

COMPONENT SELECTION — To regulate the speed of a universal motor it is necessary to determine how much gain in the feedback is needed. A change in motor current (due to load increase) causes the conduction angle to change by the appropriate amount to keep the speed constant. This entails, through trial and error, choosing an appropriate resistor value for R_{10}, since the gain of the feedback is determined by value of R_{10} as shown in Figure 8.

FIGURE 7 — AVERAGING EFFECT OF TRANSFER FUNCTION

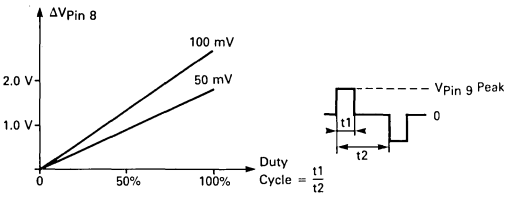
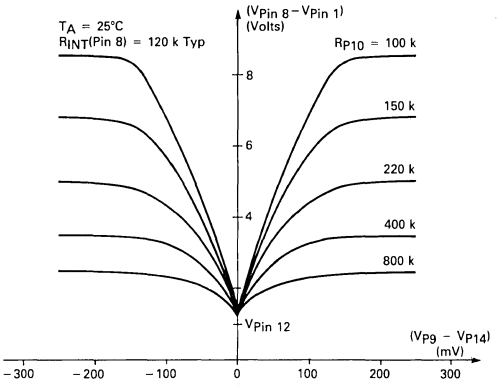


FIGURE 8 — TRANSFER FUNCTION (Pin 8/Pin 9)



Once R_{10} is picked, C_4 can be calculated from the following equation:

$$C_4 \approx \frac{.672}{f_{line} \times R_{10}}$$

where f_{line} is the line frequency.

FIGURE 9 — POSITIVE FEEDBACK EFFECT
(Offset voltages have been neglected)

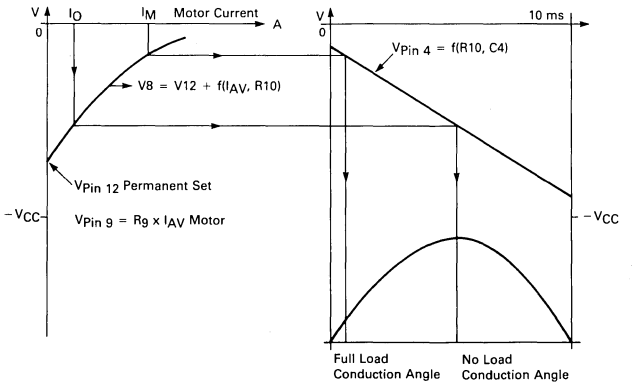
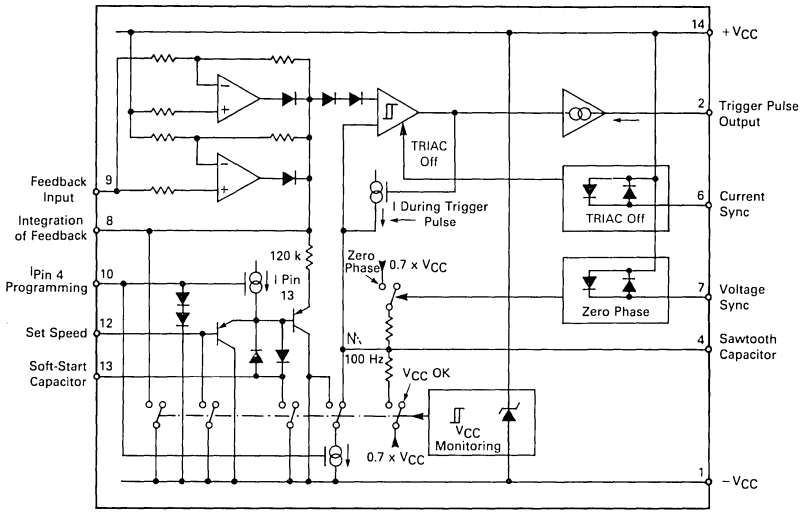


FIGURE 10 — INTERNAL BLOCK DIAGRAM



Capacitor C_8 is an integration cap used to smooth out the voltage at Pin 8. The value should be large enough to accomplish this task yet not too large to slow the response of the system.

Capacitor C_{13} determines how fast the conduction angle reaches the set value programmed at Pin 12. To achieve a desired delay, the value for C_{13} can be calculated by the following equation:

$$C_{13} \approx \frac{8 \times t_d}{|8.6 - V_{12}| \times R_{10}}$$

The remaining component values have experimentally been determined and are constant, regardless of application. The following table lists typical values for 110 volt application.

Component	Value	Units
R_S	10/2.0 W	kΩ
R_{P1}	100	kΩ
R_{P2}	100	Ω
R_6	330/0.5 W	kΩ
R_7	330/0.5 W	kΩ
R_9	0.05/5.0 W	Ω
R_{10}	100	kΩ
C_4	0.1	μF
C_8	0.22	μF
C_{13}	10	μF

Using an oscilloscope, it should be verified that the ramp generator is ramping down from −1.6 to −7.1 volts. The slope of the ramp can be changed by C_4 and the DC level of the waveform can be adjusted by R_7.

Pin 9 has a low internal impedance and requires R_{P2} to adjust the feedback level. Pin 8 must always be connected to V_{EE} through a filtering capacitor. For values of R_{10} less than 100 kΩ, the circuit becomes sensitive and could become unstable. Figures 11 and 12 show typical waveforms. As shown, the increase in motor current has resulted in the firing angle to decrease. This translates to an increase in the average power delivered to the load.

FIGURE 11 — NO LOAD APPLIED

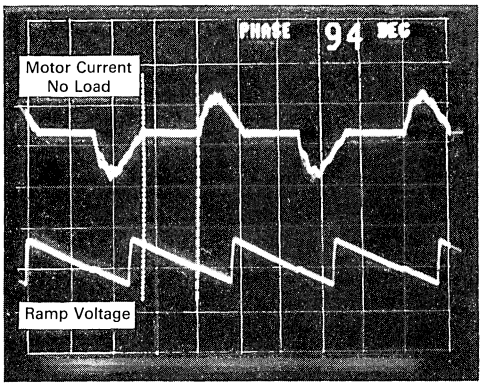
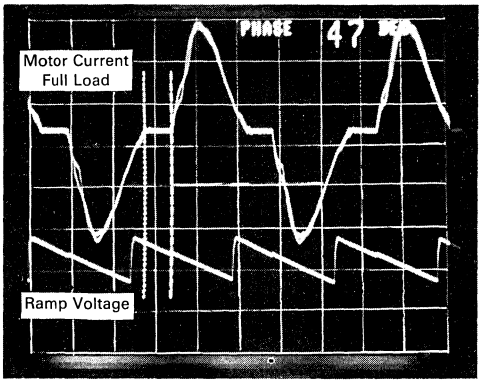


FIGURE 12 — LOAD APPLIED



TEMPERATURE EFFECTS — The TDA1185A has a very efficient internal temperature compensation. If the current feedback is not connected, the RMS power delivered to the load is stabilized within ±0.2% over a temperature range of +20 to +70°C. The feedback introduces, in the same temperature range, a drift of 250 mV on the voltage of Pin 8; this slight increase in conduction angle may be successfully used to compensate a motor ohmic resistance increase with temperature.

MAIN LINE VOLTAGE COMPENSATION — As the conduction angle is independent of main line voltage, any change in the latter induces a power variation to the load. A resistor connected to the rectifier anode and to Pin 12 with a capacitor to V_{EE} will introduce a decrease in voltage at Pin 12 as the line voltage is increasing. The values of the RC network can experimentally be determined.

FIRING ANGLE DYNAMICS — With purely resistive loads, the effective RMS applied voltage to the load is directly proportional to the firing angle (Figure 13). With inductive loads, since the current lags with respect to voltage, 100% power corresponds to a firing angle which is less than 180°.

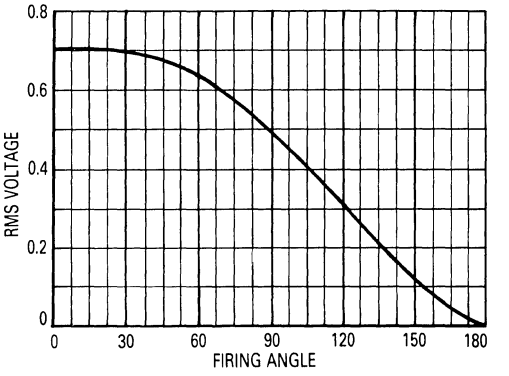
APPLICATION IDEAS

SOFT-START — The Soft-Start feature of the TDA1185A in itself opens the door to a lot of interesting applications. For example, the TDA1185A can be used to bring up fragile loads slowly. Expensive and sensitive tubes can be turned on slowly thus eliminating the inrush of current that could lead to burn out. In this application R_{P1} is replaced with a resistor divider such that the voltage at Pin 12 results in a conduction angle of 180°. Pin 9 should be grounded, since the feedback portion of the TDA1185A is not necessary (see Figure 14). The time to achieve full conduction is found by the equation below:

$$\Delta t \approx 8.71 \times R_{10} \times C_{13}$$

LIGHT DIMMER — With practically no modification the TDA1185A can be used in a light dimmer application. All that is required is to ground the input to the feedback, Pin 9. By grounding Pin 9 we have disconnected the feedback loop and the conduction angle is controlled solely by R_{P1}. Further, since the feedback is disconnected, R_9 and R_{P2} are no longer necessary. The Soft-Start feature can still be used to protect the bulb from an inrush of current. This setup can be used in any application that requires manual control of the power delivered to the load (see Figure 15).

FIGURE 13 — RMS VOLTAGE versus FIRING ANGLE

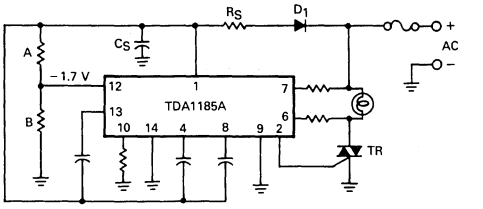


SOFT SHUT-OFF — Once again with little modification, the TDA1185A can be used to turnoff the load slowly. An example of this is in automatic garage lighting. Typically, lights that are on a timer go off without a warning, usually in the most inopportune time (like when you're about to step over the dog). With a soft shut-off, the light dims out slowly, alerting you that it is about to go off. As in the previous case, the feedback is disconnected and R_{P1} is replaced with capacitor C_{12} and a switch (see Figure 16). The turn-off time can be calculated by the following equation.

$$\Delta t \approx R_{12} \times C_{12}$$

R_{12} is the sum of the two resistors on both sides of C_{12}.

FIGURE 14 — SOFT-START CIRCUIT



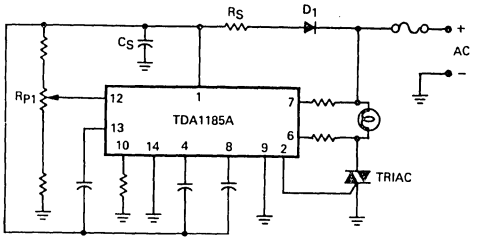
R_S = 10 kΩ 2 W
R_6 = 470 kΩ 1/2 W
R_7 = 470 kΩ 1/2 W
R_{10} = 200 kΩ
$R_{12A} = 4 \times R_{12B}$

C_4 = 44 nF
C_{13} = 10 μF
C_S = 100 μF
Turn-off time = $8.71 \times R_{10} \times C_{13}$

PC BOARD — The printed circuit board in Figure 17 is included for the designers convenience to evaluate the TDA1185A. The size of the board is intentionally small to show the compactness that can be achieved. Figure 18 shows the component layout for the PC board. R_{P1} has one of the outer leads connected to V_{EE} and the other to R_{12}. The center lead of R_{P1} is connected to Pin 12.

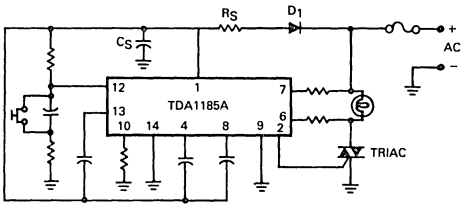
WARNING SHOCK HAZARD: IT IS HIGHLY RECOMMENDED THAT AN ISOLATION TRANSFORMER BE USED. REMOVE THE CHASSIS GROUND FOR ALL TEST EQUIPMENT.

FIGURE 15 — LIGHT DIMMER CIRCUIT



R_P = 100 k
R_S = 10 k 2 W
R_6 = 470 k 1/2 W
R_7 = 470 k 1/2 W
R_{10} = 200 k
C_4 = 44 nF
C_8 = 0.22 μF
C_{13} = 4.7 μF
C_S = 100 μF 16 V

FIGURE 16 — SOFT SHUT-OFF CIRCUIT



R_S = 10 k 2 W
R_6 = 470 k 1/2 W
R_7 = 470 k 1/2 W
R_{12} = Designer's Choice
R_{10} = 200 k
C_4 = 44 nF
C_{12} = Designer's Choice
C_{13} = 0.47 μF
C_S = 100 μF
Turn-off time = $R_{12} \times C_{12}$

FIGURE 17 — TDA1185A EVALUATION BOARD COMPONENT SIDE

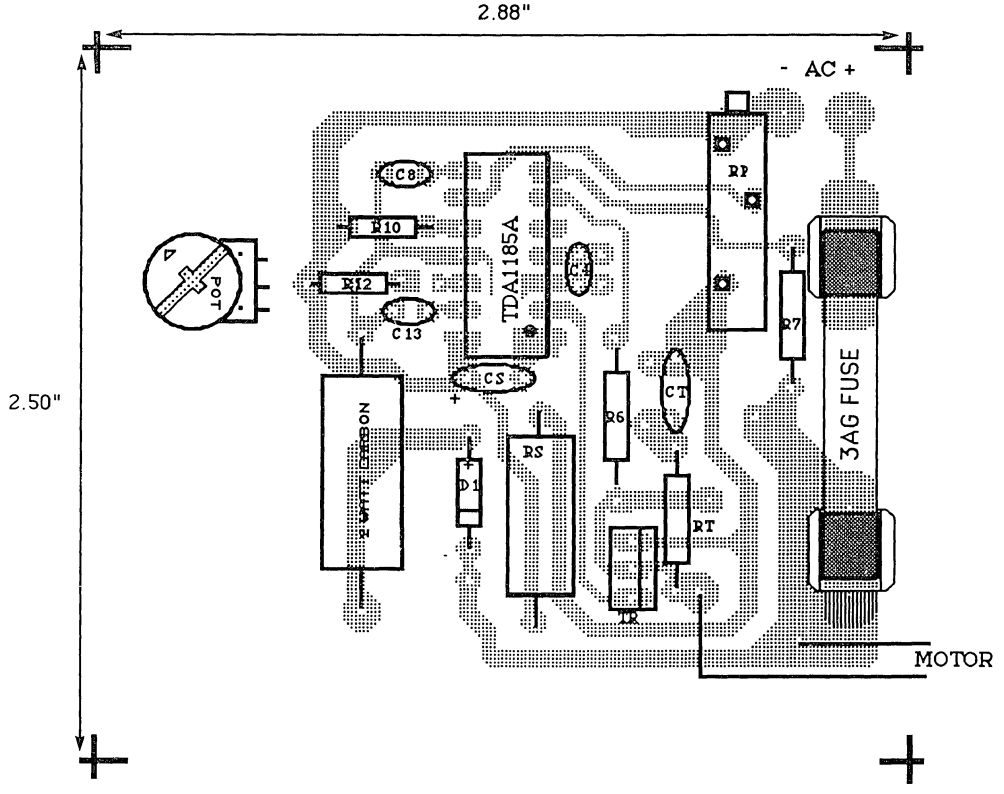
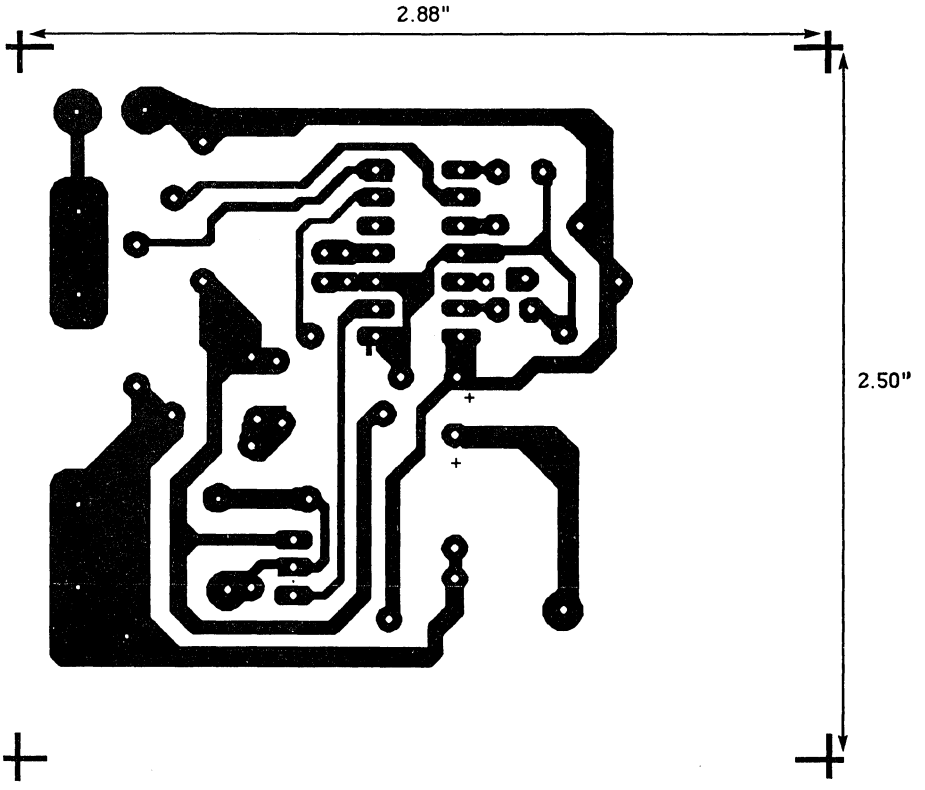


FIGURE 18 — TDA1185A EVALUATION BOARD COPPER SIDE



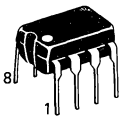
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

UAA1016B

ZERO VOLTAGE SWITCH
PROPORTIONAL BAND
TEMPERATURE CONTROLLER

SILICON MONOLITHIC
INTEGRATED CIRCUITS

4



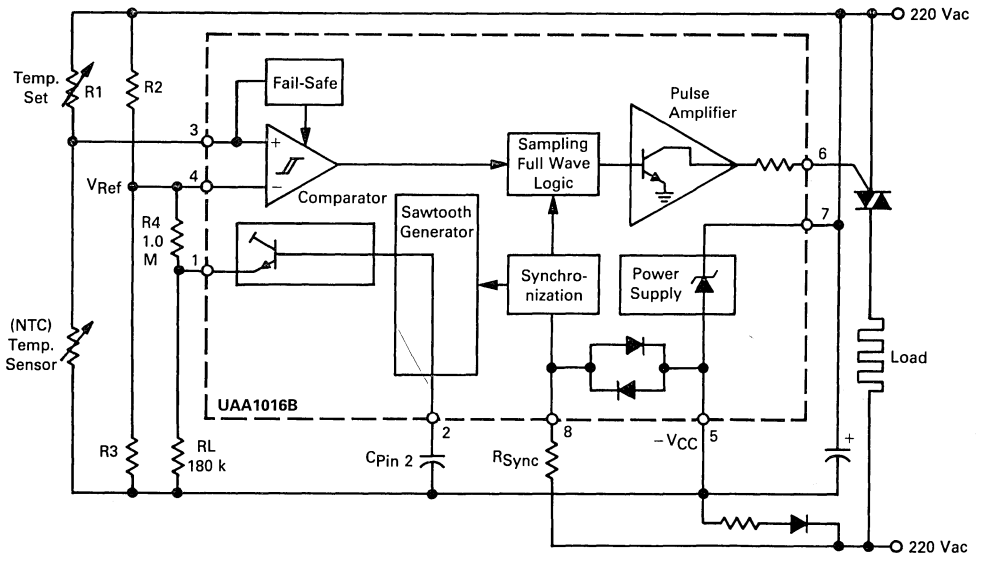
PLASTIC PACKAGE
CASE 626

ZERO VOLTAGE CONTROLLER

The UAA1016B is designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. It provides the following features:

- Proportional Temperature Control Over an Adjustable Band
- Adjustable Burst Frequency (to Comply with Standards)
- Sensor Fail-Safe
- No dc Current Component Through the Main Line (to Comply with Standards)
- Negative Output Current Pulses (TRIAC Quadrants 2 and 3)
- Direct ac Line Operation
- Low External Components Count

FIGURE 1 — BLOCK DIAGRAM AND PIN ASSIGNMENT



Design Notes: 1. Let R4 ≥ 5RL

2. Select $\frac{R2}{R3}$ Ratio for a symmetrical reference deviation centered about Pin 1 output swing, R2 will be slightly greater than R3.

3. Select R2 and R3 values for the desired reference deviation where $\Delta V_{REF} = \frac{\Delta V_{Pin\ 1}}{\frac{R4}{R2 \,||\, R3} + 1}$

MAXIMUM RATINGS (Voltages referred to Pin 7)

Parameter	Symbol	Max. Rating	Unit
Supply Current ($I_{Pin\ 5}$)	I_{CC}	15	mA
Nonrepetitive Supply Current ($I_{Pin\ 5}$)	I_{CCP}	200	mA
AC Synchronization Current (Pin 8)	I_{syn}	3.0	mA (RMS)
Maximum Pin Voltages	$V_{Pin\ 1}$ $V_{Pin\ 2}$ $V_{Pin\ 3}$ $V_{Pin\ 4}$ $V_{Pin\ 6}$	0; $-V_{CC}$ 0; $-V_{CC}$ 0; $-V_{CC}$ 0; $-V_{CC}$ +2.0; $-V_{CC}$	Volt
Maximum Current Drain	$I_{Pin\ 1}$	1.0	mA
Power Dissipation T_A = 25°C	P_D	625	mW
Maximum Thermal Resistance	$R_{\theta JA}$	100	°C/W
Operating Temperature Range	T_A	−20 to +100	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Voltages referred to Pin 7 unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
Current Consumption (Pins 6 and 8 not connected)	I_{CC}	—	0.8	1.5	mA
Stabilized Supply Voltage ($V_{Pin\ 5}$) I_{CC} = 2.0 mA max	$-V_{CC}$	−9.6	−8.6	−7.6	V
Output Pulse Current ($V_{Pin\ 6}$ from −1.0 to +1.0 Volt)	I_{out}	60	90	120	mA
Output Pulse Width $R_{Pin\ 8}$ = 220 kΩ, V_{mains} = 220 Vac/50 Hz, (Figures 4 and 5)	t_{p1} t_{p2}	58 160	60 220	120 320	μs
Comparator Input Offset Voltage ($V_{Pin\ 3} - V_{Pin\ 4}$)	V_{off}	−10	—	+10	mV
Comparator Common Mode Voltage Range	V_{CM}	$-V_{CC}+1$	—	−1.5	V
Input Bias Current (Pins 3 and 4)	I_{IB}	—	—	1.0	μA
Output Leakage Current ($I_{Pin\ 6}$) $V_{Pin\ 6}$ = +2.0 V	I_{outL}	—	—	10	μA
Fail-safe Threshold Voltage ($V_{Pin\ 3}$)	V_{FSTH}	—	−0.7	—	V
Capacitor Charging Current (Source)	$I_{Pin\ 2}$	−20	−16	−12	μA
Capacitor Discharge Current (Sink)	$I'_{Pin\ 2}$	—	6.4	—	mA
Sawtooth Pulse Length ($C_{Pin\ 2}$ = 1.0 μF)	t_{saw}	—	0.85	—	S
Output Threshold Sawtooth Levels ($V_{Pin\ 2}$)	V_{TH1} V_{TH2}	— —	−1.0 $-V_{CC}+1.25$	— —	V
Output Voltage Pin 1	$V_{Pin\ 1}$	—	$V_{Pin\ 2}-0.75$	—	V

CIRCUIT DESCRIPTION

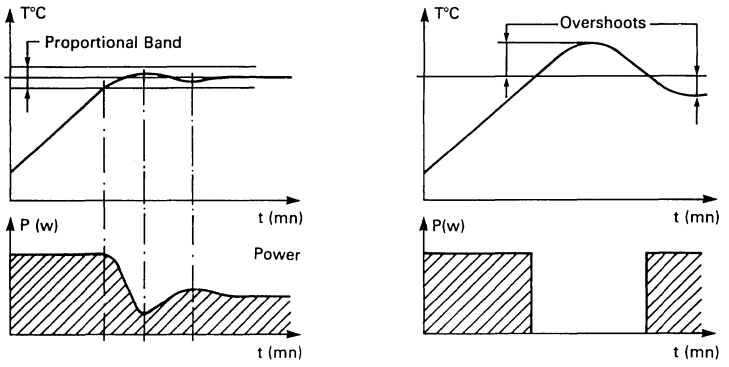
The circuit delivers current pulses to the triac at zero crossings of the main line sensed by Pin 8 through R_{sync}. An internal full wave logic allows the triac to latch during full wave periods in order to avoid any dc component in the main line, in compliance with European regulations. Trigger pulses are generated when the comparator detects $V_{Pin\ 3}$ is above $V_{Pin\ 4}$ (or $V_{reference}$) as sensed temperature through the NTC is then lower than the set value (V_{REF} corresponding to the external Wheatstone bridge equilibrium).

In order to comply with norms limiting the frequency at which a kW sized load, or above, may be connected to the main line (fluorescent tubes "flickering"), the UAA1016B has an internal time base providing (power is delivered by bursts to the load) a proportional temperature band control. In fact, most of the heating regulation systems require low temperature overshoot for more precision and stability which cannot be accomplished by direct on/off regulation (see Figure 2). An internal low frequency sawtooth generator whose output is available at Pin 1, allows the designer to introduce a periodic linear change of V_{Ref}. This deviation defines the temperature band allowing proportional power control (see Figure 3).

A fail-safe circuit inhibits output pulses when the sensor circuit has a fault (open or short circuit).

The IC is directly powered from the mains by a dropping resistor, a diode and a filter capacitor.

FIGURE 2 — PROPORTIONAL TEMPERATURE CONTROL versus ON/OFF CONTROL



PROPORTIONAL TEMPERATURE CONTROL

Reduced Overshoot

Stability

ON/OFF CONTROL

Large Overshoot

Marginal Stability

KEY CIRCUIT FUNCTIONS DESCRIPTION

POWER SUPPLY — The rectified supply current is Zener regulated to 8.6 V. Current consumption of the UAA1016B is typically less than 1.0 mA. The major part of the current fed by the dropping resistor is used for the sensor bridge and triac gate pulses. Any excess of supply current is excess power dissipation into the integrated Zener. Current consumption of the triac pulses may be derived from Figure 4 and 5 (Igt max. and pulse duration). Usually an 18 kΩ, 2.0 W dropping resistor is convenient to feed the UAA1016.

COMPARATOR — When $V_{Pin\ 3}$ is higher than $V_{Pin\ 4}$ (V_{Ref}), the comparator allows the triggering logic to deliver pulses to the triac (Figure 3). The offset hysteresis input voltage has been designed to be as low as possible (±10 mV max) in order to minimize the uncontrollable temperature band (proportional to the hysteresis) as per Figure 6. Noise rejection is performed by a synchronous sampling of the comparator output during very short times (typ. less than 100 ns).

SAWTOOTH GENERATOR — A sawtooth voltage signal is generated by a constant current source (typ. 7.5 μA), charging an external capacitor $C_{Pin\ 2}$ between two threshold levels, V_{TH1} and V_{TH2}, which are respectively:

$V_{TH1} = -1.0$ V

$V_{TH2} = -V_{CC} + 1.25$ V.

Charging and discharging currents occur only with negative halfcycles of the line.

In the UAA1016B, the sawtooth signal is available at Pin 1 as a voltage source $V_{Pin\ 1} = V_{Pin\ 2} - 0.75$ V. Maximum source current is 1.0 mA, but to keep good linearity of sawtooth signal, a source current of 40 μA is recommended (see Figure 7).

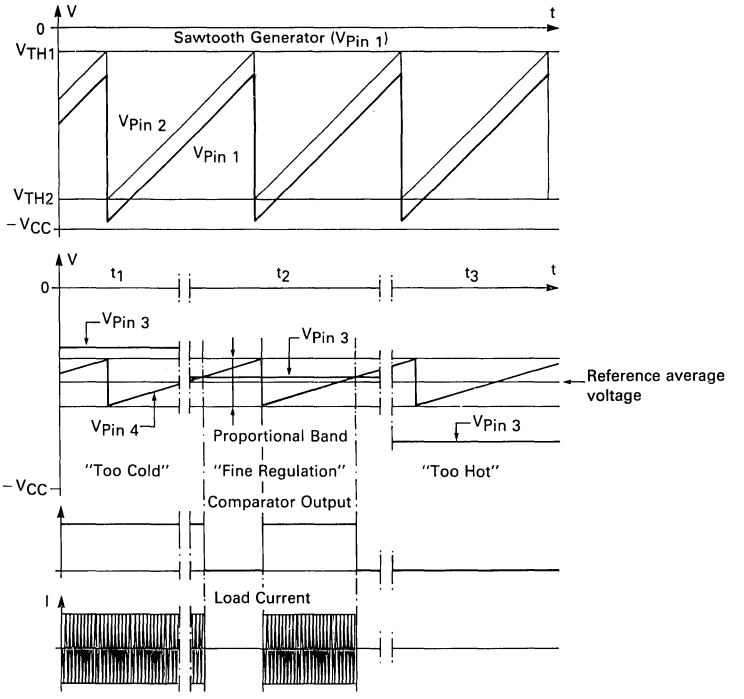
FAIL-SAFE — Output pulses are inhibited by the "fail-safe" circuit if the comparator input voltage exceeds the specified threshold voltage. This would occur if the temperature sensor circuit had a fault.

SAMPLING FULL WAVE LOGIC — Two consecutive zero-crossing trigger pulses are generated at every positive mains half-cycle of the line to minimize generation of noise (as per Figure 8). Within every zero-crossing the pulses are positioned as per Figure 4. Pulse length is also adjustable by R_{sync} on Pin 8 to allow positive triggering of the triac at this critical moment (firing with low voltage between main terminals requires long pulses).

PULSE AMPLIFIER — The pulse amplifier circuit delivers minimum current pulses of 60 mA (sink). The triac is triggered in quadrants II and III.

SYNCHRONIZATION CIRCUIT — This circuit detects mains zero-crossings through R_{sync} and the value selected determines the trigger pulse length. A zero crossing current detector is employed with typical thresholds of ∓27 μA to ±98 μA (see Figures 4 and 5).

FIGURE 3 — SAWTOOTH GENERATOR AND PROPORTIONAL BAND



COMMENTS TO FIGURE 3

Referring to Figure 1, the average value of V_{Ref} is set by R_2 and R_3. R_4 defines the amplitude of the sawtooth signal superimposed on V_{Ref}, defining the Proportional Band.

Figure 3 shows three conditions:

1) During time t_1 we always have $V_{Pin\ 3} > V_{Ref}$, and as a result, the comparator is always "on" and the triac fired (100% max. power)
2) During time t_2, $V_{Pin\ 3}$ is in the proportional band, and the average power delivered to the load is a fraction of maximum power.
3) During time t_3, $V_{Pin\ 3} < V_{Ref}$, and the triac is always "off."

When the sensor temperature is above the set value and is slowly decreasing as no heating occurs, $V_{Pin\ 3} - V_{Pin\ 4}$ must exceed half the hysteresis value before power is applied again (1). A similar effect occurs in the opposite direction when temperature sensor is below the set value and can remain stable as position (2). This defines the "uncontrollable temperature band" which will be very small if hysteresis is also very small.

SUGGESTIONS FOR USE

The temperature sensor circuit is a Wheatstone bridge including the sensor element. Comparator inputs may be free from power line noise only if the sensor element is purely resistive (NTC resistor). Usage of any P-N junction sensor would drastically reduce noise rejection.

Fixed phase sensing of the internal comparator output eliminates parasitic signals.

Some loads, even designed to be resistive, have in fact a slight inductive component. A phase shift at Pin 8 can be achieved with external capacitor C_3 connected to Pin 8 network (see Figure 9).

Suggested maximum source current at Pin 1 is 40 μA, in order to have acceptable sawtooth signal linearity.

FIGURE 4 — OUTPUT PULSE WIDTH DEFINITIONS

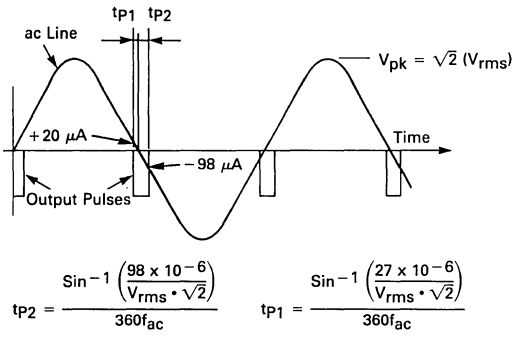


FIGURE 5 — TYPICAL OUTPUT PULSE LENGTH versus SYNCHRONIZATION RESISTOR

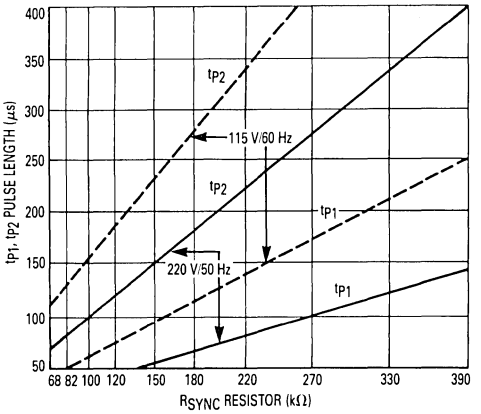


FIGURE 6 — EFFECTS OF INPUTS COMPARATOR HYSTERESIS

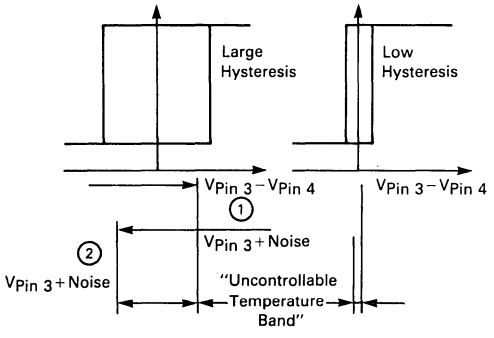


FIGURE 7 — PIN 1 INTERNAL NETWORK

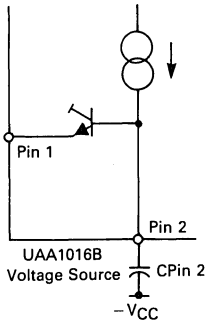
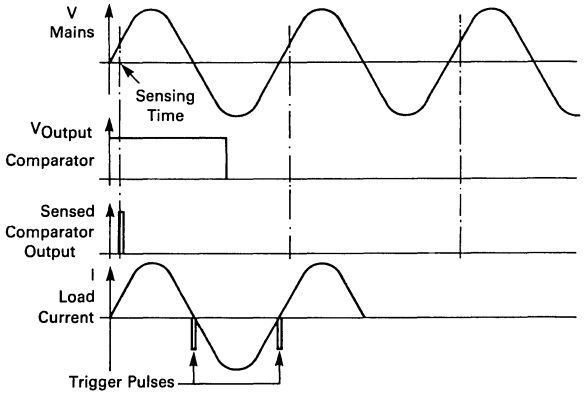


FIGURE 8 — TRIGGER PULSE GENERATION



APPLICATION CIRCUITS

Figure 9 shows a very simple application of the UAA1016B as an electronic rheostat having 100% efficiency. C_3 is required only if load has an inductive component. Figure 10 shows a typical application as a panel heater thermostat with a proportional temperature band of 1°C at 25°C.

FIGURE 9 — APPLICATION CIRCUIT — ELECTRONIC RHEOSTAT

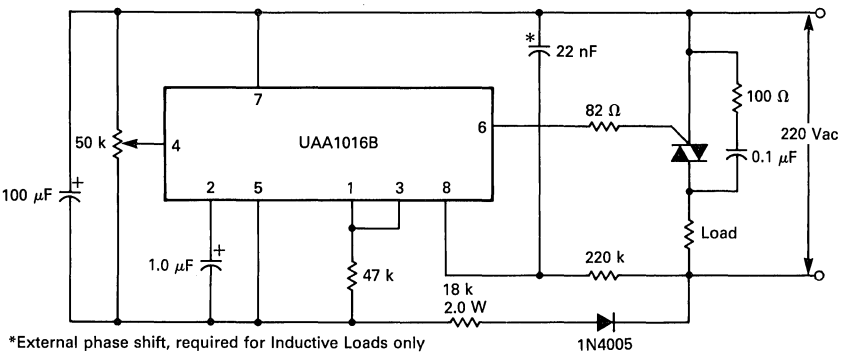
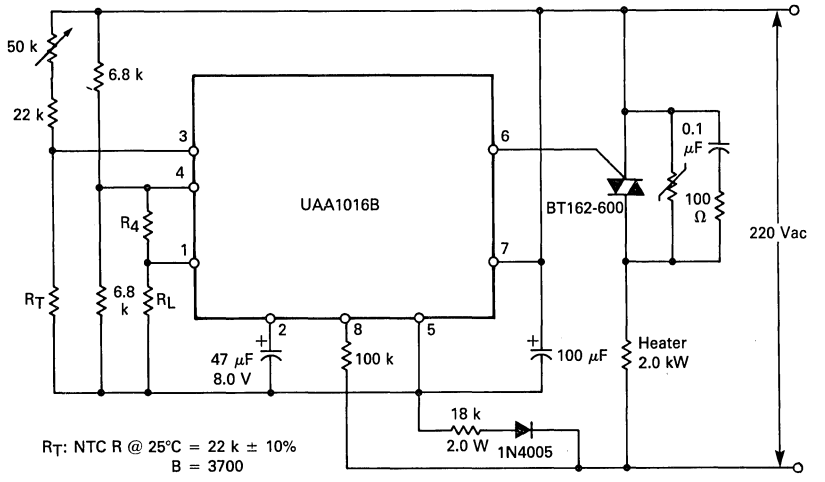


FIGURE 10 — APPLICATION CIRCUIT — ELECTRIC RADIATOR WITH PROPORTIONAL BAND THERMOSTAT, PROPORTIONAL BAND 1°C AT 25°C



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

UAA2016

4

Product Preview

Zero Voltage Switch Power Controller

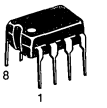
The UAA2016 is designed to drive triacs with the Zero Voltage technique which allows RFI-free power regulation of resistive loads. Operating directly on the AC power line its main application is the precision regulation of electrical heating systems such as panel heaters or irons.

A built-in digital sawtooth waveform permits proportional temperature regulation action over a ±1°C band around the set point. For energy savings there is a programmable temperature reduction function, and for security a sensor failsafe inhibits output pulses when the sensor connection is broken. Preset temperature (i.e. defrost) application is also possible. In applications where high hysteresis is needed, its value can be adjusted up to 5°C around the set point. All these features are implemented with a very low external component count.

- Zero Voltage Switch for Triacs, up to 2.0 kW (MAC212A8)
- Direct AC Line Operation
- Proporational Regulation of Temperature over a 1°C Band
- Programmable Temperature Reduction
- Preset Temperature (i.e. Defrost)
- Sensor Failsafe
- Adjustable Hysteresis
- Low External Component Count

ZERO VOLTAGE SWITCH POWER CONTROLLER

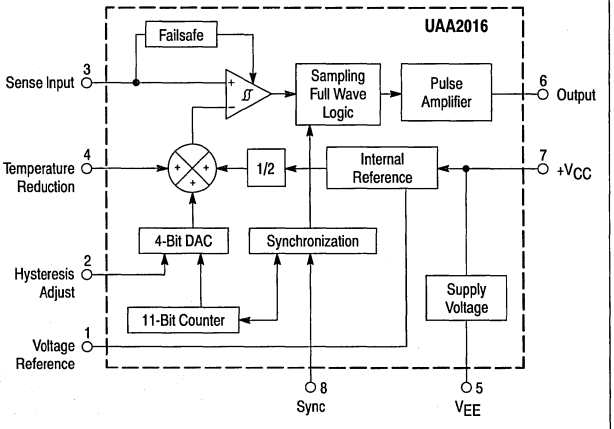
SILICON MONOLITHIC INTEGRATED CIRCUIT



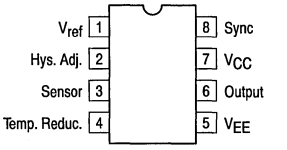
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
UAA2016D	– 20° to + 85°C	SO-8
UAA2016P		Plastic DIP

MAXIMUM RATINGS (Voltages referenced to Pin 7)

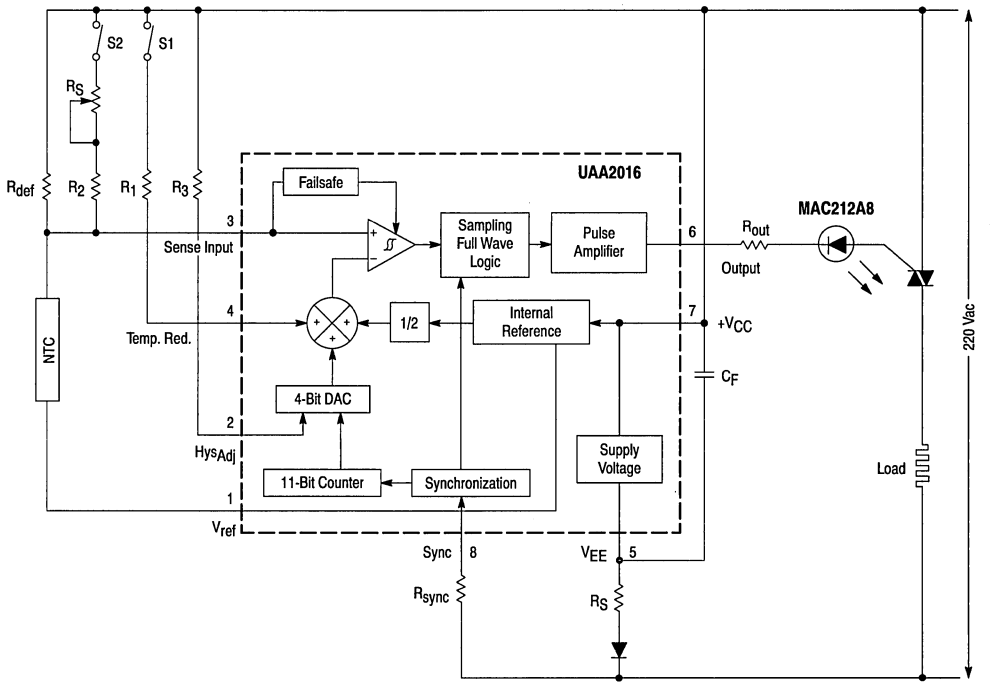
Rating	Symbol	Value	Unit
Supply Current (I_{PIN5})	I_{CC}	15	mA
Non-Repetitive Supply Current (Pulse Width = 1.0 µs)	I_{CCP}	200	mA
AC Synchronization Current	I_{sync}	3.0	mA
Pin Voltages	$V_{Pin\ 2}$ $V_{Pin\ 3}$ $V_{Pin\ 4}$ $V_{Pin\ 6}$	0; V_{ref} 0; V_{ref} 0; V_{ref} 0; V_{EE}	V
V_{ref} Current Sink	$I_{Pin\ 1}$	1.0	mA
Output Current (Pin 6) (Pulse Width < 400 µs)	I_O	150	mA
Power Dissipation	P_D	625	mW
Thermal Resistance	$R_{\theta JA}$	100	°C/W
Operating Temperature Range	T_A	– 20 to + 85	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{EE} = –7.0 V, voltages referred to Pin 7, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Pins 6, 8 Not Connected) (T_A = – 20° to + 85°C)	I_{CC}	—	0.9	1.5	mA
Stabilized Supply Voltage (Pin 5) (I_{CC} = 2.0 mA)	V_{EE}	–10	– 9.0	– 8.0	V
Reference Voltage (Pin 1)	V_{ref}	– 6.5	– 5.5	– 4.5	V
Output Pulse Current (T_A = – 20°C to + 85°C) (R_{out} = 60 W, V_{EE} = – 8.0 V)	I_O	90	100	130	mA
Output Leakage Current (V_{out} = 0 V)	I_{OL}	—	—	10	µA
Output Pulse Width (T_A = – 20°C to + 85°C) (Note 1) (Mains = 220 Vrms, R_{sync} = 220 kΩ)	T_P	50	—	100	µs
Comparator Offset (Note 5)	V_{off}	–10	—	+10	mV
Sensor Input Bias Current	I_{IB}	—	—	0.1	µA
Sawtooth Period (Note 2)	T_S	—	40.96	—	sec
Sawtooth Amplitude (Note 6)	A_S	50	70	90	mV
Temperature Reduction Voltage (Note 3) (Pin 4 Connected to V_{CC})	V_{TR}	280	350	420	mV
Internal Hysteresis Voltage (Pin 2 Not Connected)	V_{IH}	—	10	—	mV
Additional Hysteresis (Note 4) (Pin 2 Connected to V_{CC})	V_H	280	350	420	mV
Failsafe Threshold (T_A = – 20°C to + 85°C) (Note 7)	V_{FSth}	180	—	300	mV

NOTES: 1. Output pulses are centered with respect to zero crossing point. Pulse width is adjusted by the value of R_{sync}. Refer to application curves.
2. The actual sawtooth period depends on the AC power line frequency. It is exactly 2048 times the corresponding period. For the 50 Hz case it is 40.96 sec. For the 60 Hz case it is 34.13 sec. This is to comply with the European standard, namely that 2.0 kW loads cannot be connected or removed from the line more than once every 30 sec.
3. 350 mV corresponds to 5°C temperature reduction. This is tested at probe using internal test pad. Smaller temperature reduction can be obtained by adding an external resistor between Pin 4 and V_{CC}. Refer to application curves.
4. 350 mV corresponds to a hysteresis of 5°C. This is tested at probe using internal test pad. Smaller additional hysteresis can be obtained by adding an external resistor between Pin 2 and V_{CC}. Refer to application curves.
5. Parameter guaranteed but not tested. Worst case 10 mV corresponds to 0.15°C shift on set point.
6. Measured at probe by internal test pad. 70 mV corresponds to 1°C. Note that the proportional band is independent of the NTC value.
7. At very low temperature the NTC resistor increases quickly. This can cause the sensor input voltage to reach the failsafe threshold, thus inhibiting output pulses; refer to application schematics. The corresponding temperature is the limit at which the circuit works in the typical application. By setting this threshold at 0.05 V_{ref}, the NTC value can increase up to 20 times its nominal value, thus the application works below – 20°C.

Figure 1. Application Schematic



APPLICATION INFORMATION

(For simplicity, the LED in series with R_{out} is omitted in the following calculations)

Triac Choice and R_{out} Determination

Depending on the power in the load, choose the triac that has the lowest peak gate trigger current. This will limit the output current of the UAA2016 and thus its power consumption. Use Figure 4 to determine R_{out} according to the triac maximum gate current (I_{GT}) and the application low temperature limit. For a 2.0 kW load at 220 Vrms, a good triac choice is the Motorola MAC212A8. Its maximum peak gate trigger current at 25°C is 50 mA.

For an application to work down to – 20°C, R_{out} should be 60 Ω. It is assumed that: $I_{GT}(T) = I_{GT}(25°C) \times \exp(-T/125)$ with T in °C, which applies to the MAC212A8.

Output Pulse Width, R_{sync}

The pulse width T_P is determined by the triac's I_{Hold}, I_{Latch} together with the load value and working conditions (frequency and voltage):

Given the RMS AC voltage and the load power, the load value is:

$$R_L = V^2_{rms}/POWER$$

The load current is then:

$$I_{Load} = (Vrms \times \sqrt{2} \times \sin(2\pi ft) - V_{TM})/R_L$$

where V_{TM} is the maximum on state voltage of the triac, f is the line frequency.

Set $I_{Load} = I_{Latch}$ for $t = T_P/2$ to calculate T_P.

Figures 6 and 7 give the value of T_P which corresponds to the higher of the values of I_{Hold} and I_{Latch}, assuming that V_{TM} = 1.6 V. Figure 8 gives the R_{sync} that produces the corresponding T_P.

R_{Supply} and Filter Capacitor

With the output current and the pulse width determined as above, use Figures 9 and 10 to determine R_{Supply}, assuming that the sinking current at V_{ref} pin (including NTC bridge current) is less than 0.5 mA. Then use Figures 11 and 12 to determine the filter capacitor (C_F) according to the ripple desired on supply voltage. The maximum ripple allowed is 1.0 V.

Temperature Reduction Determined by R_1

(Refer to Figures 13 and 14.)

Figure 2. Comparison Between Proportional Control and ON/OFF Control

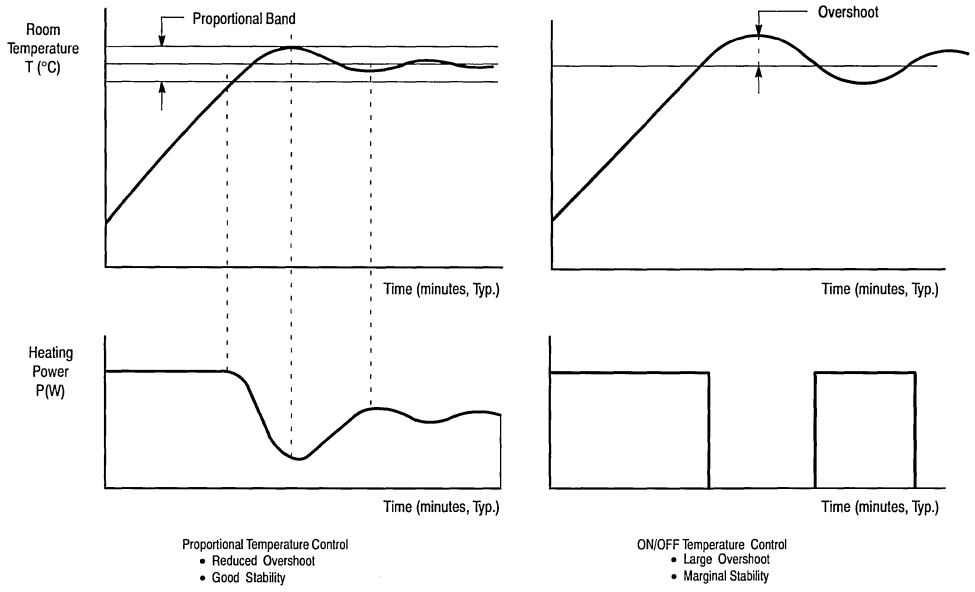
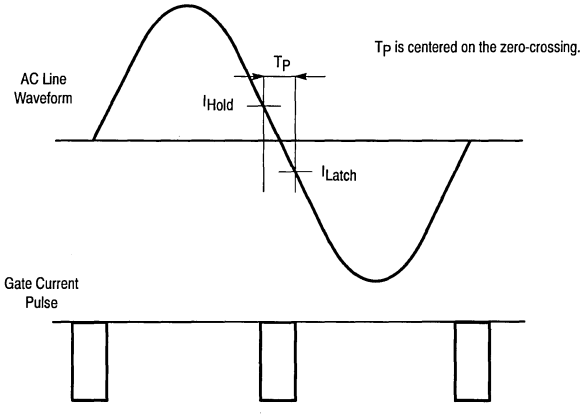


Figure 3. Zero Voltage Technique



$$T_P = \frac{14 \times R_{sync} + 7 \times 10^5}{Vrms \times \sqrt{2} \times \pi f} \ (\mu s)$$

f = AC Line Frequency (Hz)
Vrms = AC Line RMS Voltage (V)
R_{sync} = Synchronization Resistor (Ω)

CIRCUIT FUNCTIONAL DESCRIPTION

Power Supply – Pin 5 and Pin 7

The application uses a current source supplied by a single high voltage rectifier in series with a power dropping resistor. An integrated shunt regulator delivers a V_{EE} voltage of – 8.6 V with respect to Pin 7. The current used by the total regulating system can be shared in four functional blocks: IC supply, sensing bridge, triac gate firing pulses and zener current. The integrated zener, as in any shunt regulator, absorbs the excess supply current. The 50 Hz pulsed supply current is smoothed by the large value capacitor connected between Pins 5 and 7.

Temperature Sensing – Pin 3

The actual temperature is sensed by a negative temperature coefficient element connected in a resistor divider fashion. This two element network is connected between the ground terminal Pin 5 and the reference voltage – 5.5 V available on Pin 1. The resulting voltage, a function of the measured temperature, is applied to Pin 3 and internally compared to a control voltage whose value depends on several elements: Sawtooth, Temperature Reduction and Hysteresis Adjust. (Refer to Application Information.)

Temperature Reduction

For energy saving, a remotely programmable temperature reduction is available on Pin 4. The choice of resistor R_1 connected between Pin 4 and V_{CC} sets the temperature reduction level.

Comparator

When the positive input (Pin 3) receives a voltage greater than the internal reference value, the comparator allows the triggering logic to deliver pulses to the triac gate. To improve the noise immunity the comparator has an adjustable hysteresis. The external resistor R_3 connected to Pin 2 sets the hysteresis level. Setting Pin 2 open makes a 10 mV hysteresis level, corresponding to 0.15°C. Maximum hysteresis is obtained by connecting Pin 2 to V_{CC}. In that case the level is set at 5°C. This configuration can be useful for low temperature inertia systems.

Sawtooth Generator

In order to comply with European norms the ON/OFF period on the load must exceed 30 seconds. This is achieved by an internal digital sawtooth which performs the proportional regulation without any additional component. The sawtooth signal is added to the reference applied to the comparator negative input. Figure 2 shows the regulation improvement using the proportional band action.

Noise Immunity

The noisy environment requires good immunity. Both the voltage reference and the comparator hysteresis minimize the noise effect on the comparator input. In addition the effective triac triggering is enabled every 1/3 sec.

Failsafe

Output pulses are inhibited by the "failsafe" circuit if the comparator input voltage exceeds the specified threshold voltage. This would occur if the temperature sensor circuit is open.

Sampling Full Wave Logic

Two consecutive zero-crossing trigger pulses are generated at every positive mains half-cycle. This ensures that the number of delivered pulses is even in every case. The pulse length is selectable by R_{sync} connected on Pin 8. The pulse is centered on the zero-crossing mains waveform.

Pulse Amplifier

The pulse amplifier circuit sinks current pulses from Pin 6 to V_{EE}. The minimum amplitude is 70 mA. The triac is then triggered in quadrants II and III. The effective output current amplitude is given by the external resistor R_{out}. Eventually, an LED can be inserted in series with the Triac gate (see Figure 1).

Figure 4. Output Resistor versus Triac Gate Current

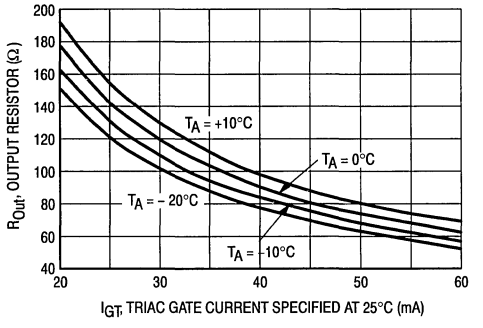


Figure 5. Minimum Output Current versus Output Resistor

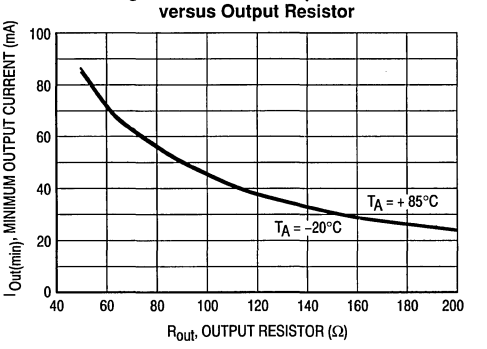


Figure 6. Output Pulse Width versus Maximum Triac Latch Current

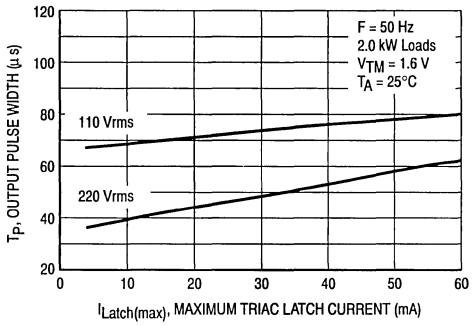


Figure 7. Output Pulse Width versus Maximum Triac Latch Current

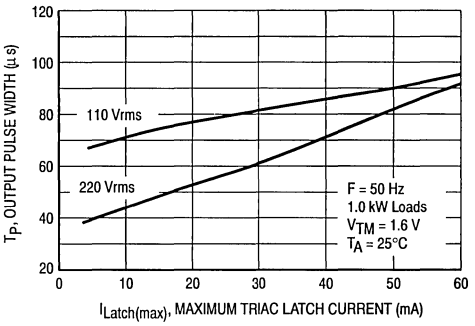


Figure 8. Synchronization Resistor versus Output Pulse Width

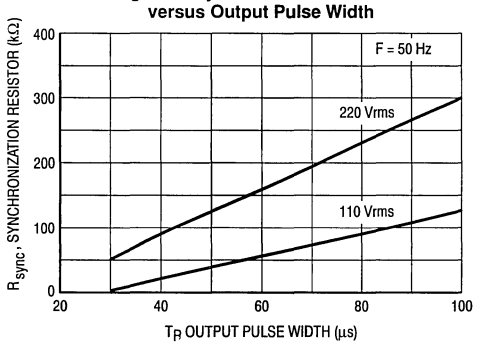


Figure 9. Maximum Supply Resistor versus Output Current

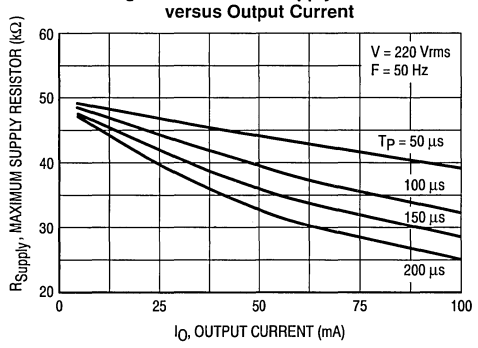


Figure 10. Maximum Supply Resistor versus Output Current

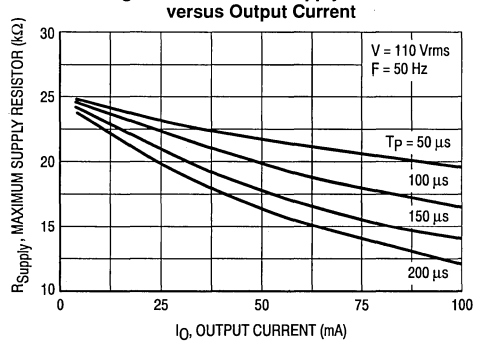


Figure 11. Minimum Filter Capacitor versus Output Current

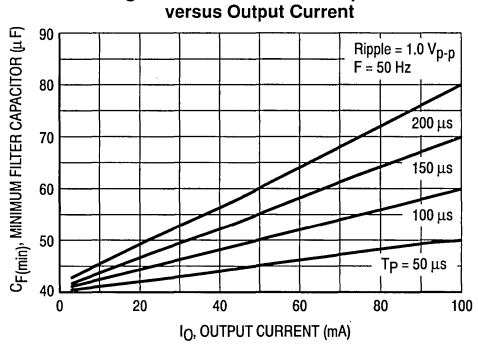


Figure 12. Minimum Filter Capacitor versus Output Current

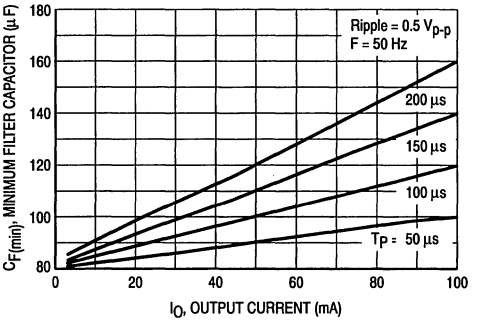


Figure 13. Temperature Reduction versus R_1

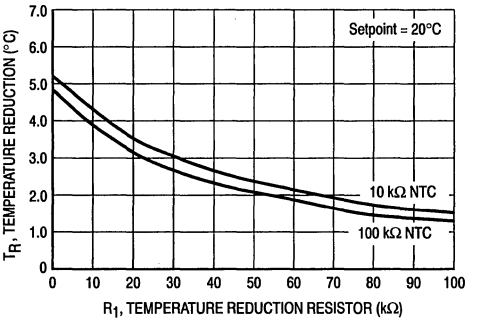


Figure 14. Temperature Reduction versus Temperature Setpoint

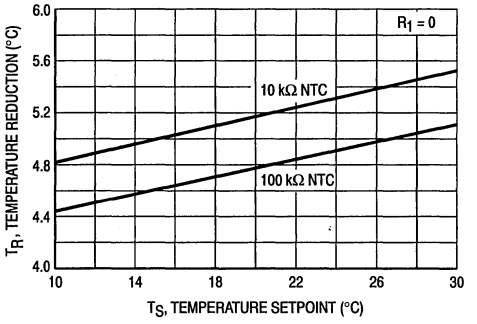


Figure 15. R_{DEF} versus Preset Temperature

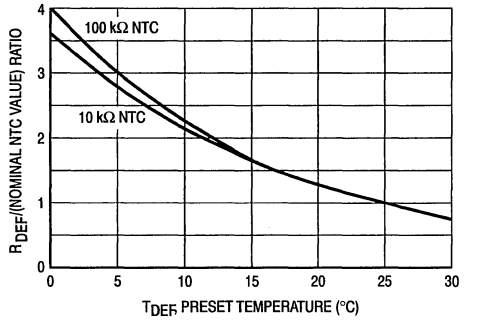


Figure 16. $R_S + R_2$ versus Preset Setpoint

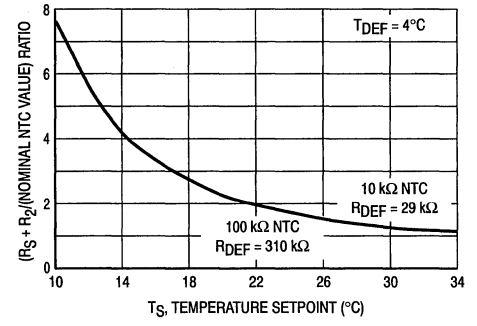
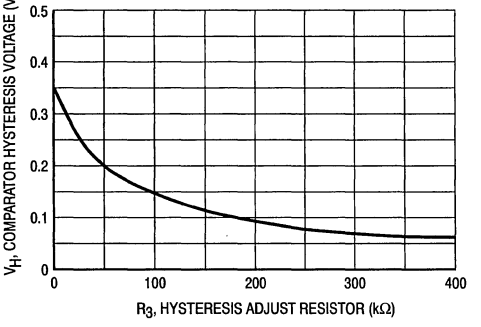


Figure 17. Comparator Hysteresis versus R_3



Surface Mount Technology

In Brief . . .

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of Insertion Technology. Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance state-of-the-art designs that cannot be accomplished with Insertion Technology.

Surface Mount packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance, have been reduced. The lower profile of Surface Mount packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated-through-holes in the board, contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are set directly to the assembly line, eliminating an intermediate step. Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and offer increased functions with the same size product.

Linear and Interface

Bipolar

All the major bipolar analog families are now represented in surface mount packaging. Standard SOIC and PLCC packages are augmented by SOP-8 and DPAK for Linear regulators. In addition, tape and reel shipping to the updated EIA-481A is now on line for the industry's largest array of operational amplifiers, regulators, interface, data conversion, consumer, telecom and automotive Linear ICs.

Device	Function	Package
CA3146D	Transistor Array	SO-14
DAC-08CD, ED	High-Speed 8-Bit Multiplying D-to-A Converter	SO-16
LF351D	Single JFET Operational Amplifier	SO-8
LF353D	Dual JFET Operational Amplifiers	SO-8
LF411CD	Single/Dual JFET Operational Amplifier	SO-8
LF412CD	Dual JFET Operational Amplifiers	SO-8
LF441CD	Single JFET Low Power Operational Amplifier	SO-8
LF442CD	Dual JFET Low Power Operational Amplifiers	SO-8
LF444CD	Quad JFET Low Power Operational Amplifiers	SO-14
LM201AD	General Purpose Adjustable Operational Amplifier	SO-8
LM211D	High Performance Voltage Comparator	SO-8
LM224D	Quad Low Power Operational Amplifiers	SO-14
LM239D,AD	Quad Single Supply Comparators	SO-14
LM258D	Dual Low Power Operational Amplifiers	SO-8
LM285D-1.2	Micropower Voltage Reference Diode	SO-8
LM285D-2.5	Micropower Voltage Reference Diode	SO-8
LM293D	Dual Comparators	SO-8
LM301AD	General Purpose Adjustable Operational Amplifier	SO-8
LM311D	High Performance Voltage Comparator	SO-8
LM317LD	Positive Adjustable 100 mA Voltage Regulator	SOP-8
LM317MDT	Positive Adjustable 500 mA Voltage Regulator	DPAK
LM324D,AD	Quad Low Power Operational Amplifiers	SO-14
LM339D,AD	Quad Single Supply Comparators	SO-14
LM348D	Quad MC1741 Operational Amplifiers	SO-14
LM358D	Dual Low Power Operational Amplifiers	SO-8
LM385D-1.2	Micropower Voltage Reference Diode	SO-8
LM385D-2.5	Micropower Voltage Reference Diode	SO-8
LM393D	Dual Comparators	SO-8
LM833D	Dual Audio Amplifiers	SO-8
LM2901D	Quad Single Supply Comparators	SO-14
LM2902D	Quad Low Power Operational Amplifiers	SO-14
LM2903D	Dual Comparators	SO-8
LM2904D	Dual Low Power Operational Amplifiers	SO-8
LM2931AD-5.0,D-5.0	Low Dropout Voltage Regulator	SOP-8
LM2931CD	Adjustable Low Dropout Voltage Regulator	SOP-8
LM3900D	Quad Single Supply Operational Amplifiers	SO-14
MC1350D	IF Amplifier	SO-8
MC1357D	FM IC with Quadrature Detector	SO-14
MC1377DW	Color Television RGB to PAL/NTSC Encoder	SO-20L
MC1378FN	Video Overlay Synchronizer	PLCC-44
MC1382DW	Multimode Monitor TTL To Analog Video	SO-24L
MC1403D	Precision Low Voltage Reference	SO-8
MC1413D	Peripheral Driver Array	SO-16
MC1436D,CD	High Voltage Operational Amplifier	SO-8
MC1455D	Timing Circuit	SO-8
MC1458D,CD	Dual Operational Amplifiers	SO-8
MC14C88BD	Quad EIA-232-D/EIA-562 Drivers	SO-14
MC1488D	Quad EIA-232-D Drivers	SO-14

Bipolar (continued)

Device	Function	Package
MC14C89ABD,BD	Quad EIA-232-D/EIA-562 Receivers	SO-14
MC1489D	Quad EIA-232-D Receivers	SO-14
MC1495D	Four-Quadrant Multiplier	SO-14
MC1496D	Balanced Modulator/Demodulator	SO-14
MC1723CD	Adjustable Positive or Negative Voltage Regulator	SO-14
MC1741CD	General Purpose Operational Amplifier	SO-8
MC1747CD	Dual MC1741 Operational Amplifiers	SO-14
MC1776CD	Programmable Operational Amplifier	SO-8
MC26LS31D	Quad EIA-422/23 Drivers	SO-16
MC26LS32D	Quad EIA-422 Receivers	SO-16
MC26S10D	Quad Bus Transceiver	SO-16
MC2831AD	FM Transmitter	SO-16
MC3303D	Quad Differential-Input Operational Amplifier	SO-14
MC3335DW	Basic Dual Conversion Receiver	SO-20L
MC3346D	General Purpose Transistor Array	SO-14
MC3356DW	FSK Receiver	SO-20L
MC3359DW	Low Power Narrowband FM IF Amplifier	SO-20L
MC3361AD	Low Voltage Narrowband FM IF Amplifier	SO-16
MC3362DW	Dual Conversion Receivers	SO-28L
MC3363DW	Dual Conversion Receivers	SO-28L
MC3367DW	Low Voltage VHF Receiver	SO-28L
MC3371D	Low Voltage FM Receiver with RSSI, LC Quadrature Detector	SO-16
MC3372D	Low Voltage FM Receiver with RSSI, Ceramic Quadrature Detector	SO-16
MC3391DW	Low Side Protected Switch	SOP-8+8L
MC3401D	Quad Operational Amplifiers	SO-14
MC3403D	Quad Differential-Input Operational Amplifier	SO-14
MC3418DW	CVSD	SO-16L
MC3423D	Overvoltage Sensing Circuit	SO-8
MC3448AD	Quad GPIB Transceivers	SO-16
MC3450D	Quad Line Receivers	SO-16
MC3452D	Quad Line Receivers	SO-16
MC3456D	Dual Timing Circuit	SO-14
MC3458D	Dual Low Power Operational Amplifiers	SO-8
MC3486D	Quad EIA-422/23 Receivers	SO-16
MC3487D	Quad EIA-422 Drivers	SO-16
MC4558CD	Dual High Frequency Operational Amplifiers	SO-8
MC4741CD	Quad MC1741 Operational Amplifiers	SO-14
MC78L05ACD	Positive Voltage Regulator, 5 V, 100 mA	SOP-8
MC78L08ACD	Positive Voltage Regulator, 8 V, 100 mA	SOP-8
MC78L12ACD	Positive Voltage Regulator, 12 V, 100 mA	SOP-8
MC78L15ACD	Positive Voltage Regulator, 15 V, 100 mA	SOP-8
MC78M05CDT	Positive Voltage Regulator, 5 V, 500 mA	DPAK
MC78M08CDT	Positive Voltage Regulator, 8 V, 500 mA	DPAK
MC78M12CDT	Positive Voltage Regulator, 12 V, 500 mA	DPAK
MC78M15CDT	Positive Voltage Regulator, 15 V, 500 mA	DPAK
MC79L05ACD	3-Terminal Negative Fixed Voltage Regulator, –5 V, 100 mA	SOP-8
MC79L12ACD	3-Terminal Negative Fixed Voltage Regulator, –12 V, 100 mA	SOP-8
MC79L15ACD	3-Terminal Negative Fixed Voltage Regulator, –15 V, 100 mA	SOP-8
MC79M05CDT	3-Terminal Negative Fixed Voltage Regulator, –5 V, 500 mA	DPAK
MC79M12CDT	3-Terminal Negative Fixed Voltage Regulator, –12 V, 500 mA	DPAK
MC79M15CDT	3-Terminal Negative Fixed Voltage Regulator, –15 V, 500 mA	DPAK
MC10319DW	8-Bit A/D Flash Converter	SO-24L
MC10321DW	7-Bit A/D Flash Converter	SO-20L
MC13022DW(1)	Medium Voltage AM Stereo C-QUAM® Decoder	SO-28L

(1)To be introduced.

Bipolar (continued)

Device	Function	Package
MC13024DW	Low Voltage C-QUAM® Receiver	SO-24L
MC13055D	VHF LAN Receiver — FSK	SO-16
MC13060D	1 Watt Audio Amplifier	SOP-8
MC33023DW,FN	High Speed (1.0 MHz) Single-Ended PWM Controller	SO-16L, PLCC-20
MC33025DW,FN	High Speed (1.0 MHz) Double-Ended PWM Controller	SO-16L, PLCC-20
MC33033DW	Brushless DC Motor Controller	SO-20L
MC33035DW	Brushless DC Motor Controller	SO-24L
MC33039D	Closed Loop Brushless Motor Adaptor (5 V ± 5% Supply)	SO-8
MC33060AD	Precision Switchmode Pulse Width Modulator	SO-14
MC33064D-5	Undervoltage Sensing Circuit	SO-8
MC33065DW	Dual Current Mode PWM Controller	SO-16L
MC33065DW-H	Dual Current Mode PWM Controller (Off-Line)	SO-16L
MC33065DW-L	Dual Current Mode PWM Controller (DC-to-DC Converters)	SO-16L
MC33066DW	Resonant Mode (ZCS) Controller	SO-16L
MC33067DW	Resonant Mode (ZVS) Controller	SO-16L
MC33071D,AD	Single, High Speed Single Supply Operational Amplifiers	SO-8
MC33072D,AD	Dual, High Speed Single Supply Operational Amplifiers	SO-8
MC33074D,AD	Quad, High Speed Single Supply Operational Amplifiers	SO-14
MC33076D	Dual High Output Current Operational Amplifiers	SO-8
MC33077D	Dual, Low Noise High Frequency Operational Amplifiers	SO-8
MC33078D	Dual Audio, Low Noise Operational Amplifiers	SO-8
MC33079D	Low Power, Single Supply Operational Amplifier	SO-14
MC33091D	High Side TMOS Driver	SO-8
MC33102D	Sleep-Mode™ 2-State, µProcessor Operational Amplifier	SO-8
MC33110D	Low Voltage Compander	SO-14
MC33120FN	SLIC II	PLCC-28
MC33121FN	Low Voltage Subscriber Loop Interface Circuit	PLCC-28
MC33129D	High Performance Current Mode Controller	SO-14
MC33151D	Dual Inverting MOSFET Drivers	SO-8
MC33152D	Dual Noninverting MOSFET Drivers	SO-8
MC33161D	Universal Voltage Monitor	SO-8
MC33164D-3	Micropower Undervoltage Sensing Circuit (3 V ± 5% Supply)	SO-8
MC33164D-5	Micropower Undervoltage Sensing Circuit (5 V ± 10% Supply)	SO-8
MC33171D	Single, Low Power, Single Supply Operational Amplifier	SO-8
MC33172D	Dual, Low Power, Single Supply Operational Amplifiers	SO-8
MC33174D	Quad, Low Power, Single Supply Operational Amplifiers	SO-14
MC33178D	Dual Precision Operational Amplifiers	SO-8
MC33179D	Quad Precision Operational Amplifiers	SO-14
MC33218DW	Voice-Switched Speakerphone with µProcessor Interface	SO-24L
MC33261D	Power Factor Controller	SO-8
MC33272D	Dual Precision Bipolar Operational Amplifiers	SO-8
MC33274D	Quad Precision Bipolar Operational Amplifiers	SO-14
MC33282D	Dual Precision Low Input JFET Operational Amplifiers (Trim-in-the-Package)	SO-8
MC33284D	Quad Precision JFET Operational Amplifiers (Trim-in-the-Package)	SO-14
MC34001D,BD	Single JFET Input Operational Amplifier	SO-8
MC34002D,BD	Dual JFET Input Operational Amplifiers	SO-8
MC34010FN	Electronic Telephone Circuit	PLCC-44
MC34012-1D	Telephone Tone Ringer	SO-8
MC34012-2D	Telephone Tone Ringer	SO-8
MC34012-3D	Telephone Tone Ringer	SO-8
MC34014DW	Telephone Speech Network with Dialer Interface	SO-20L
MC34017-1D	Telephone Tone Dialer	SO-8
MC34017-2D	Telephone Tone Dialer	SO-8
MC34017-3D	Telephone Tone Dialer	SO-8
MC34018DW	Voice Switched Speakerphone Circuit	SO-28L
MC34023DW,FN	High Speed (1.0 MHz) Single-Ended PWM Controller	SO-16L, PLCC-20

Bipolar (continued)

Device	Function	Package
MC34025DW,FN	High Speed (1.0 MHz) Double-Ended PWM Controller	SO-16L, PLCC-20
MC34050D	EIA-422/23 Transceivers	SO-16
MC34051D	EIA-422/23 Transceivers	SO-16
MC34060AD	Switchmode Pulse Width Modulation Control Circuit	SO-14
MC34063AD	Precision DC-to-DC Converter Control Circuit	SO-8
MC34064D-5	Undervoltage Sensing Circuit (5 V ± 5% Supply)	SO-8
MC34065DW	Dual Current Mode PWM Controller	SO-16L
MC34065DW-H	Dual Current Mode PWM Controller (Off-Line)	SO-16L
MC34065DW-L	Dual Current Mode PWM Controller (DC-to-DC Converter)	SO-16L
MC34066DW	Resonant Mode (ZCS) Controller	SO-16L
MC34067DW	Resonant Mode (ZVS) Controller	SO-16L
MC34071D,AD	Single, High Speed, Single Supply Operational Amplifier	SO-8
MC34072D,AD	Dual, High Speed, Single Supply Operational Amplifiers	SO-8
MC34074D,AD	Quad, High Performance, Single Supply Operational Amplifiers	SO-14
MC34080D	High Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier	SO-8
MC34081D	High Speed JFET Input Operational Amplifier	SO-8
MC34084DW,ADW	Quad High Speed, JFET Operational Amplifier	SO-16L
MC34085DW,ADW	Quad High Speed, JFET Operational Amplifier	SO-16L
MC34114DW	Speech Network II	SO-18L
MC34115DW	CVSD	SO-16L
MC34118DW	Speakerphone II	SO-28L
MC34119D	Telephone Speaker Amplifier	SO-8
MC34129D	Power Supply Controller	SO-14
MC34151D	Dual Inverting MOSFET Drivers	SO-8
MC34152D	Dual Noninverting MOSFET Drivers	SO-8
MC34161D	Universal Voltage Monitor	SO-8
MC34164D-3	Micropower Undervoltage Sensing Circuit (3 V ± 5% Supply)	SO-8
MC34164D-5	Micropower Undervoltage Sensing Circuit (5 V ± 10% Supply)	SO-8
MC34181D	Single, Low Power, High Speed JFET Operational Amplifier	SO-8
MC34182D	Dual, Low Power, High Speed JFET Operational Amplifiers	SO-8
MC34184D	Quad, Low Power, High Speed JFET Operational Amplifiers	SO-14
MC34217D	Adjustable Toner Ringer	SO-8
MC34261D	Power Factor Controller	SO-8
MC44301DW	High Performance Video IF	SO-28L
MC75172BDW	Quad EIA-485 Line Drivers w/3-State Outputs	SO-20L
MC75174BDW	Quad EIA-485 Line Drivers w/3-State Outputs	SO-20L
NE556D	Dual Timing Circuit	SO-14
TL064CD	Quad JFET Low Power Operational Amplifiers	SO-14
TL071CD,ACD	Single, Low Noise JFET Input Operational Amplifier	SO-8
TL072CD,ACD	Dual, Low Noise JFET Input Operational Amplifiers	SO-8
TL081CD,ACD	Single, JFET Input Operational Amplifier	SO-8
TL082CD,ACD	Dual, JFET Input Operational Amplifiers	SO-8
TL431ACD,AID,CD,ID	Programmable Precision Reference	SOP-8
UAA1041BD	Automotive Direction Indicator	SO-8
UC2842AD, BD, BD1	Off-Line Current Mode PWM Controller	SO-14, SO-8
UC2843AD, BD, BD1	Current Mode PWM Controller	SO-14, SO-8
UC2844D, BD, BD1	Off-Line Current Mode PWM Controller (DC ≤ 50%)	SO-14, SO-8
UC2845D, BD, BD1	Current Mode PWM Controller (DC ≤ 50%)	SO-14, SO-8
UC3842AD, BD, BD1	Off-Line Current Mode PWM Controller	SO-14, SO-8
UC3843AD, BD, BD1	Current Mode PWM Controller	SO-14, SO-8
UC3844D, BD, BD1	Off-Line Current Mode PWM Controller (DC ≤ 50%)	SO-14, SO-8
UC3845D, BD, BD1	Current Mode PWM Controller (DC ≤ 50%)	SO-14, SO-8

MOS Digital-Analog

Device	Function	Package
A/D and D/A Converters		
MC14433DW	3-1/2 Digit A/D Converter	SO-24L
MC14442FN	11-Channel 8-Bit A/D Converter with Parallel Interface	PLCC-28
MC14443DW	6-Channel A/D Converter Subsystem	SO-16L
MC14447DW	6-Channel A/D Converter Subsystem	SO-16L
MC44250FN	Triple 8-Bit Video A/D Converter	PLCC-44
MC144110DW	Hex D/A Converter with Serial Interface	SO-20L
MC144111DW	Quad D/A Converter with Serial Interface	SO-16L
MC145040FN1(2)	11-Channel, 8-Bit A/D Converter with Serial Interface	PLCC-20
MC145040FN2(2)	11-Channel, 8-Bit A/D Converter with Serial Interface	PLCC-20
MC145041FN1(2)	11-Channel, 8-Bit A/D Converter with Serial Interface	PLCC-20
MC145041FN2(2)	11-Channel, 8-Bit A/D Converter with Serial Interface	PLCC-20
MC145050DW	11-Channel, 10-Bit A/D Converter with Serial Interface	SO-20L
MC145051DW	11-Channel, 10-Bit A/D Converter with Serial Interface	SO-20L
MC145053D	11-Channel, 10-Bit A/D Converter with Serial Interface	SO-14
Display Drivers		
MC14489DW	Multi-Character LED Display/Lamp Driver	SO-20L
MC14495DW1(2)	Hex-to-7 Segment Latch/Decoder ROM/Driver	SO-16L
MC14499DW	7-Segment LED Display Decoder/Driver with Serial Interface	SO-20L
MC145000FN	48-Segment Multiplexed LCD Driver (Master)	PLCC-28
MC145001FN	44-Segment Multiplexed LCD Driver (Slave)	PLCC-28
MC145453FN	33-Segment LCD Driver with Serial Interface	PLCC-44
Operational Amplifiers/Comparators		
MC14573D	Quad Programmable Operational Amplifier	SO-16
MC14574D	Quad Programmable Comparator	SO-16
MC14575D	Dual Programmable Operational Amplifier and Dual Comparator	SO-16
MC14576BF	Dual Video Amplifier	SO-8 (EIAJ)
MC14577BF	Dual Video Amplifier	SO-8 (EIAJ)
MC14578D	Micro-Power Comparator Plus Voltage Follower	SO-16
Phase-Locked Loop Frequency Synthesizers		
MC145106FN	PLL Frequency Synthesizer	PLCC-20
MC145145DW1	4-Bit Data Bus Input PLL Frequency Synthesizer	SO-20L
MC145146DW1	4-Bit Data Bus Input PLL Frequency Synthesizer	SO-20L
MC145149DW	Serial Input Dual PLL Frequency Synthesizer	SO-20L
MC145151DW2	Parallel Input PLL Frequency Synthesizer	SO-28L
MC145151FN2	Parallel Input PLL Frequency Synthesizer	PLCC-28
MC145152DW2	Parallel Input PLL Frequency Synthesizer	SO-28L
MC145152FN2	Parallel Input PLL Frequency Synthesizer	PLCC-28
MC145155FN2	Serial Input PLL Frequency Synthesizer	PLCC-20
MC145155DW2	Serial Input PLL Frequency Synthesizer	SO-20L
MC145156FN2	Serial Input PLL Frequency Synthesizer	PLCC-20
MC145156DW2	Serial Input PLL Frequency Synthesizer	SO-20L
MC145157FN2	Serial Input PLL Frequency Synthesizer	PLCC-20
MC145157DW2	Serial Input PLL Frequency Synthesizer	SO-16L
MC145158FN2	Serial Input PLL Frequency Synthesizer	PLCC-20
MC145158DW2	Serial Input PLL Frequency Synthesizer	SO-16L
MC145159DW1	Serial Input PLL Frequency Synthesizer with Analog Phase Detector	SO-20L
MC145159FN(3)	Serial Input PLL Frequency Synthesizer with Analog Phase Detector	PLCC-20
MC145160DW	Dual PLL for Cordless Telephones	SO-20L
MC145161DW	Dual PLL for Cordless Telephones	SO-16L
MC145166DW	Dual PLL for Cordless Telephones	SO-16L
MC145167DW	Dual PLL for Cordless Telephones	SO-16L
MC145168DW	Dual PLL for Cordless Telephones	SO-16L
MC145170D	Serial Interface PLL Frequency Synthesizer	SO-16

(2)The digit 1 or 2 after the package designator is not a part of the package definition, but describes the electrical capability of the device.
(3)Electrical variations may require a numerical suffix after the package suffix. Contact your Motorola representative for details.
(4)Introduction of this device in surface mount packages is dependent on market demand.

MOS Digital-Analog (continued)

Device	Function	Package
Remote Control Functions		
MC14469FN	Addressable Asynchronous Receiver/Transmitter	PLCC-44
MC14497	PCM Remote Control Transmitter	(3)
MC145026D	Remote Control Encoder	SO-16
MC145027DW	Remote Control Decoder	SO-16L
MC145028DW	Remote Control Decoder	SO-16L
MC145030DW	Remote Control Encoder/Decoder	SO-20
MC145033DW	Remote Control Encoder/Decoder	SO-28L
MC145034DW	Remote Control Encoder	SO-28L
MC145035DW	Remote Control Decoder	SO-28L
Smoke Detectors		
MC14467	Low-Cost Smoke Detector	(3)
MC14468	Interconnectable Smoke Detector	(3)
MC145010DW	Photoelectric Smoke Detector with I/O	SO-16L
MC145011DW	Photoelectric Smoke Detector with I/O	SO-16L
Telecommunications Devices		
MC14410DW	2-of-8 Tone Encoder	SO-16L
MC14411DW	Bit Rate Generator	SO-24L
MC142100DW	Crosspoint Switch with Control Memory (4 × 4 × 1)	SO-16L
MC142103	Transcoder HDB31 AMI to NRZ	(3)
MC143403D	Quad Line Driver (Op Amp)	SO-14
MC145403DW	EIA-232/V.28 CMOS Driver/Receiver	SO-20L
MC145404DW	EIA-232/V.28 CMOS Driver/Receiver	SO-20L
MC145405DW	EIA-232/V.28 CMOS Driver/Receiver	SO-20L
MC145406DW	EIA-232/V.28 CMOS Driver/Receiver	SO-16L
MC145407DW	EIA-232/V.28 CMOS Driver/Receiver, 5.0 V Only	SO-20L
MC145408DW	EIA-232/V.28 CMOS Driver/Receiver	SO-20L
MC145412	Pulse/Tone Repertory Dialer (Nine 18-Digit Memory)	(3)
MC145416DW	Pulse/Tone Repertory Dialer (13 18-Digit Memory)	SO-20L
MC145421DW	UDLT II Master	SO-24L
MC145422DW	UDLT Master	SO-24L
MC145425DW	UDLT II Slave	SO-24L
MC145426DW	UDLT Slave	SO-24L
MC145428DW	Data Set Interface Circuit	SO-20L
MC145436DW	DTMF Decoder	SO-16L
MC145439	Transcoder B8ZS, B6ZS, HDB3 to NRZ	(3)
MC145442DW	300-Baud CCITT V.21 Single-Chip Modem	SO-20L
MC145443DW	300-Baud Bell 103 Single-Chip Modem	SO-20L
MC145447DW	Calling Line I.D. Receiver with Ring Detector	SO-16L
MC145472FE	ISDN U-Interface Transceiver	CQFP-68L
MC145472FU	ISDN U-Interface Transceiver	PQFP-68L
MC145475DW	ISDN S/T Transceiver	SO-28L
MC145480DW	+5.0 V PCM Codec/Filter	SO-20L
MC145488	Dual Data Link Controller	(3)
MC145502	PCM Codec/Filter	(3)
MC145503DW	PCM Codec/Filter	SO-16L
MC145505DW	PCM Codec/Filter	SO-16L
MC145532DW	ADPCM Transcoder	SO-16L
MC145540DW	ADPCM Codec	SO-28L
MC145554DW	PCM Codec/Filter (TP3054 Compatible)	SO-16L
MC145557DW	PCM Codec/Filter (TP3057 Compatible)	SO-16L
MC145564DW	PCM Codec/Filter (TP3064 Compatible)	SO-20L
MC145567DW	PCM Codec/Filter (TP3067 Compatible)	SO-20L
MC145705DW	EIA-232/V.28 CMOS Driver/Receiver, 5.0 V Only	SO-20L
MC145706DW	EIA-232/V.28 CMOS Driver/Receiver, 5.0 V Only	SO-20L
MC145707DW	EIA-232/V.28 CMOS Driver/Receiver, 5.0 V Only	SO-20L

Surface Mount Technology Package Overview

CASE 369A
PLASTIC
DPAK
DT SUFFIX

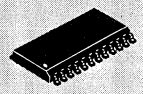
CASE 751
PLASTIC
SO-8, SOP-8
D. D1 SUFFIX

CASE 751A
PLASTIC
SO-14
D SUFFIX

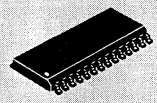
CASE 751B
PLASTIC
SO-16
D SUFFIX

CASE 751C
PLASTIC
SO-18L
DW SUFFIX

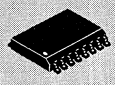
CASE 751D
PLASTIC
SO-20L
DW SUFFIX



CASE 751E
PLASTIC
SO-24L
DW SUFFIX



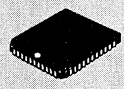
CASE 751F
PLASTIC
SO-28L
DW SUFFIX



CASE 751G
PLASTIC
SO-8+8L, SO-16L
DW SUFFIX

CASE 775
PLASTIC
PLCC-20
FN SUFFIX

CASE 776
PLASTIC
PLCC-28
FN SUFFIX



CASE 777
PLASTIC
PLCC-44
FN SUFFIX

12

Analog MPQ Table

Tape/Reel and Ammo Pack

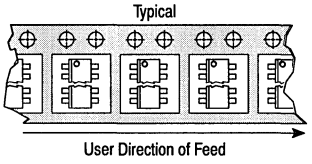
Package Type	Package Code	MPQ
PLCC		
Case 775	0802	1000/reel
Case 776	0804	500/reel
Case 777	0801	500/reel
Case 778	0805	450/reel
Case 779	0803	250/reel
Case 780	0806	250/reel
SOIC		
Case 751	0095	2500/reel
Case 751A	0096	2500/reel
Case 751B	0097	2500/reel
Case 751G	2003	1000/reel
Case 751C	2004	1000/reel
Case 751D	2005	1000/reel
Case 751E	2008	1000/reel
Case 751F	2009	1000/reel
TO-92		
Case 29	0031	2000/reel
Case 29	0031	2000/Ammo Pack

Tape and Reel
Logic and Analog Technologies, and MOS Integrated Circuits

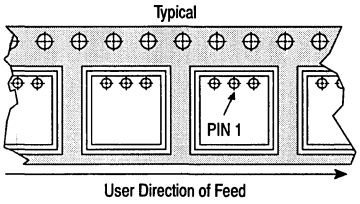
Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. Three reel sizes are available, for all but the largest types, to support the requirements of both first and second generation pick-and-place equipment. The packaging fully conforms to the latest EIA-481A specification. The antistatic embossed tape provides a secure cavity, sealed with a peel-back cover tape.

Mechanical Polarization

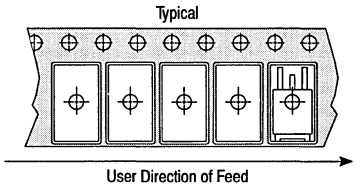
SOIC DEVICES



PLCC DEVICES



DPAK DEVICES

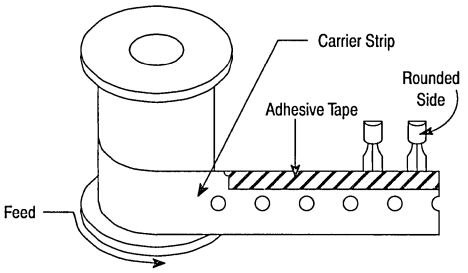


Package	Tape Width (mm)	Device(1) per Reel	Reel Size (inch)	Device Suffix
SO-8, SOP-8	12	2,500	13	R2
SO-14	16	2,500	13	R2
SO-16	16	2,500	13	R2
SO-16L, SO-8+8L WIDE	16	1,000	13	R2
SO-20L WIDE	24	1,000	13	R2
SO-24L WIDE	24	1,000	13	R2
SO-28L WIDE	24	1,000	13	R2
SO-28L WIDE	32	1,000	13	R3
PLCC-20	16	1,000	13	R2
PLCC-28	24	500	13	R2
PLCC-44	32	500	13	R2
PLCC-52	32	500	13	R2
PLCC-68	44	250	13	R2
PLCC-84	44	250	13	R2
TO-226AA (TO-92)(2)	18	2,000	13	RA, RB, RE, RM, or RP (Ammo Pack) only
DPAK	16	2,500	13	RK

(1)Minimum order quantity is 1 reel. Distributors/OEM customers may break lots or reels at their option, however broken reels may not be returned.
(2)Integrated circuits in TO-226AA packages are available in Styes A, B and E only, with optional "Ammo Pack" (Suffix RM or RP). For ordering information please contact your local Motorola Semiconductor Sales Office.

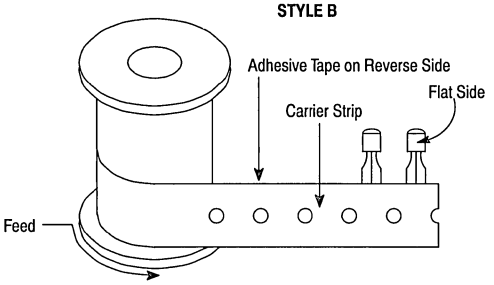
TO-92 Reel Styles

STYLE A



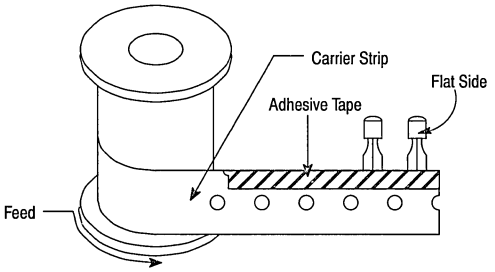
Rounded Side of Transistor and Adhesive Tape Visible.

STYLE B



Flat Side of Transistor and Carrier Strip Visible (Adhesive Tape on Reverse Side).

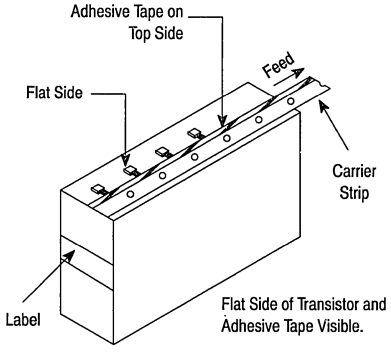
STYLE E



Flat Side of Transistor and Adhesive Tape Visible.

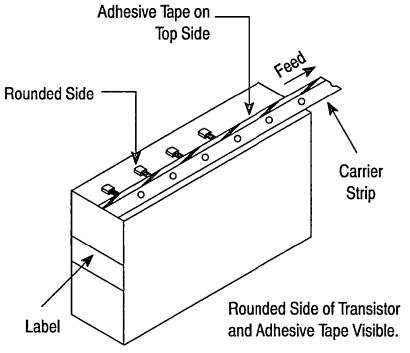
TO-92 Ammo Pack Styles

STYLE M



Style M Ammo Pack Is Equivalent to Style E of Reel Pack Dependent on Feed Orientation From Box.

STYLE P



Style P Ammo Pack Is Equivalent to Styles A and B of Reel Pack Dependent on Feed Orientation From Box.

12

Packaging Information

In Brief . . .

The packaging availability for each device type is indicated on the individual data sheets and the Selector Guide. All of the outline dimensions for the packages are given in this section.

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(TA)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

where:

$P_{D(TA)}$ = *Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.*

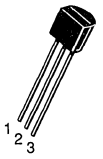
$T_{J(max)}$ = *Maximum operating Junction Temperature as listed in the Maximum Ratings Section. See individual data sheets for $T_{J(max)}$ information.*

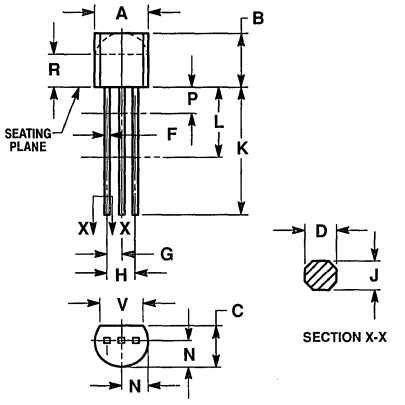
T_A = *Maximum desired operating Ambient Temperature*

$R_{\theta JA(Typ)}$ = *Typical Thermal Resistance Junction-to-Ambient*

Case Outline Dimensions

LP, P, Z SUFFIX
CASE 29-04
Plastic Package
$R_{\theta JA}$ = 200°C/W
(TO-226AA/TO-92)

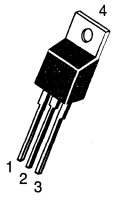


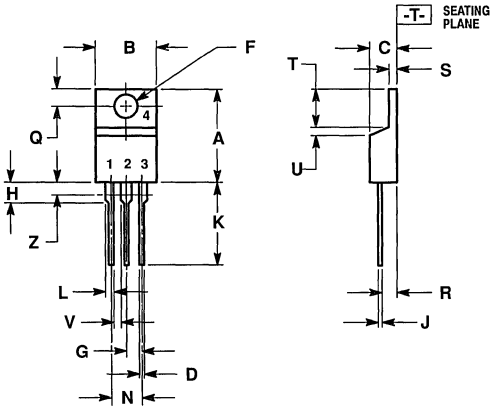


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIM R IS UNCONTROLLED.
4. DIM F APPLIES BETWEEN P AND L. DIM D AND J APPLIES BETWEEN L AND K MINIMUM. LEAD DIM IS UNCONTROLLED IN P AND BEYOND DIM K MINIMUM.
5. 029-01 AND -02 OBSOLETE, NEW STANDARD 029-04.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.45	5.20	0.175	0.205
B	4.32	5.33	0.170	0.210
C	3.18	4.19	0.125	0.165
D	0.41	0.55	—	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
H	2.42	2.66	0.095	0.105
J	0.39	0.50	0.015	0.020
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.04	2.66	0.080	0.105
P	—	2.54	—	0.100
R	2.93	—	0.115	—
V	3.43	—	0.135	—

KC, T SUFFIX
CASE 221A-06
Plastic Package
$R_{\theta JA}$ = 65°C/W (Typ)
(TO-220AB)



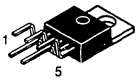


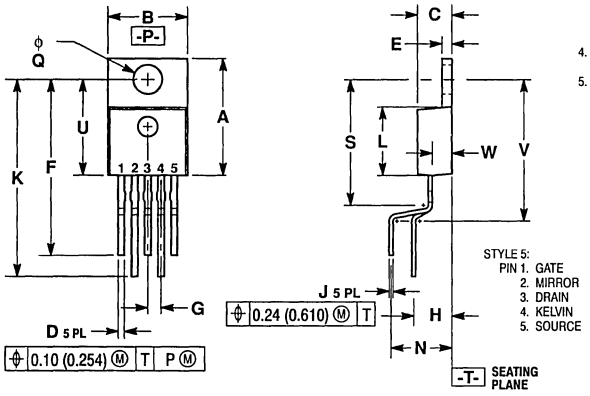
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.64	0.018	0.025
K	12.70	14.27	0.500	0.562
L	1.15	1.52	0.045	0.060
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

13

T, TV SUFFIX
CASE 314B-04
Plastic Package

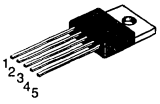


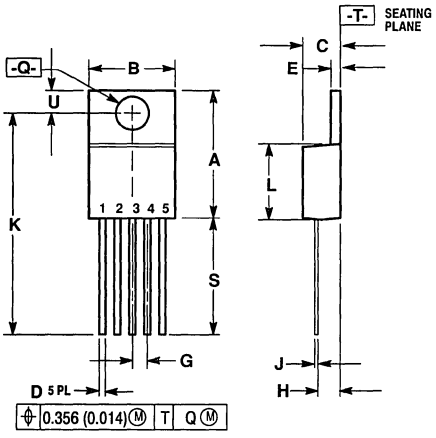


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONECT BAR (DAM BAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 0.043 (1.092) MAXIMUM.
4. 314B-01, 314B-02 AND 314B-03 OBSOLETE, NEW STANDARD 314B-04.
5. STYLE 1 THRU 4: OBSOLETE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.529	15.570	0.572	0.613
B	9.906	10.541	0.390	0.415
C	4.318	4.572	0.170	0.180
D	0.635	0.965	0.025	0.038
E	1.219	1.397	0.048	0.055
F	21.590	23.749	0.850	0.935
G	1.702 BSC		0.067 BSC	
H	4.216 BSC		0.166 BSC	
J	0.381	0.635	0.015	0.025
K	22.860	27.940	0.900	1.100
L	8.128	9.271	0.320	0.365
N	8.128 BSC		0.320 BSC	
Q	3.556	3.886	0.140	0.153
S	—	15.748	—	0.620
U	11.888	12.827	0.468	0.505
V	—	18.669	—	0.735
W	2.286	2.794	0.090	0.110

T, T1 SUFFIX
CASE 314D-03
Plastic Package
$R_{\theta JA}$ = 65°C/W (Typ)

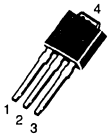


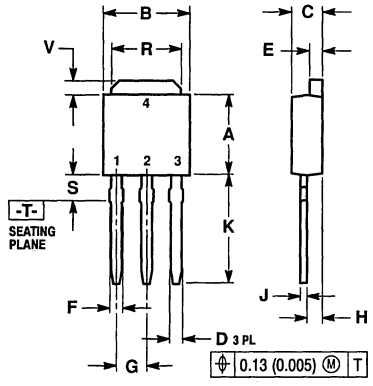


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.529	15.570	0.572	0.613
B	9.906	10.541	0.390	0.415
C	4.318	4.572	0.170	0.180
D	0.635	0.965	0.025	0.038
E	1.219	1.397	0.048	0.055
G	1.702 BSC		0.067 BSC	
H	2.210	2.845	0.087	0.112
J	0.381	0.635	0.015	0.025
K	25.908	27.051	1.020	1.065
L	8.128	9.271	0.320	0.365
Q	3.556	3.886	0.140	0.153
U	2.667	2.972	0.105	0.117
S	13.792	14.783	0.543	0.582

DT-1 SUFFIX
CASE 369-06
Plastic Package



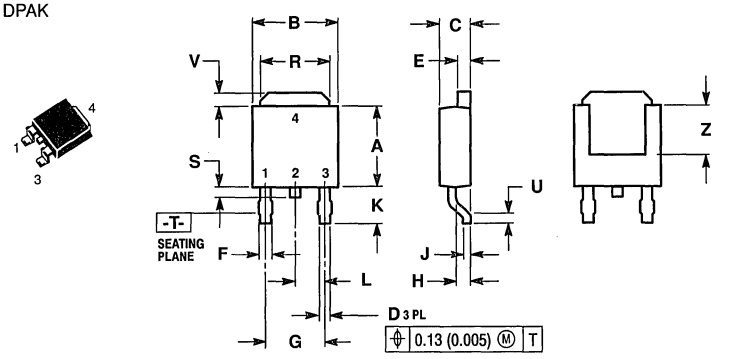


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 369-01 THRU -05 OBSOLETE, NEW STANDARD 369-06.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.84	1.01	0.033	0.040
F	0.94	1.19	0.037	0.047
G	2.29 BSC		0.090 BSC	
H	0.87	1.01	0.034	0.040
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
R	4.45	5.46	0.175	0.215
S	1.27	2.28	0.050	0.090
V	0.77	1.27	0.030	0.050

13

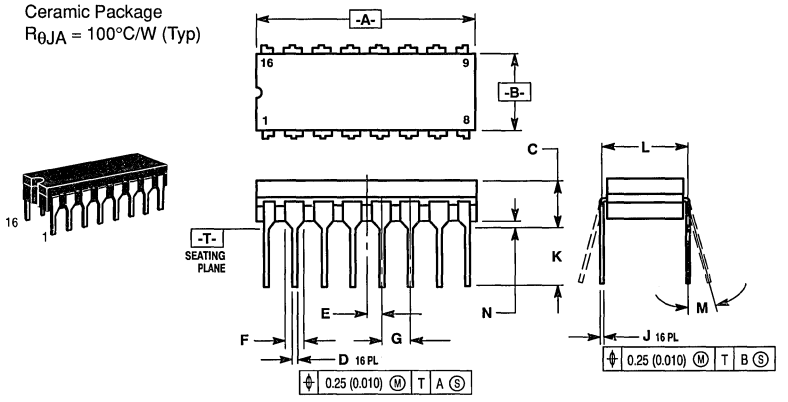
DT SUFFIX
CASE 369A-10
Plastic Package
DPAK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 369A-01 THRU -03 OBSOLETE.
4. 369A-04 THRU -09 OBSOLETE, NEW STANDARD 369A-10.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.84	1.01	0.033	0.040
F	0.94	1.19	0.037	0.047
G	4.58 BSC		0.180 BSC	
H	0.87	1.01	0.034	0.040
J	0.46	0.58	0.018	0.023
K	2.60	2.89	0.102	0.114
L	2.29 BSC		0.090 BSC	
R	4.45	5.46	0.175	0.215
S	0.51	1.27	0.020	0.050
U	0.51	—	0.020	—
V	0.77	1.27	0.030	0.050
Z	3.51	—	0.138	—

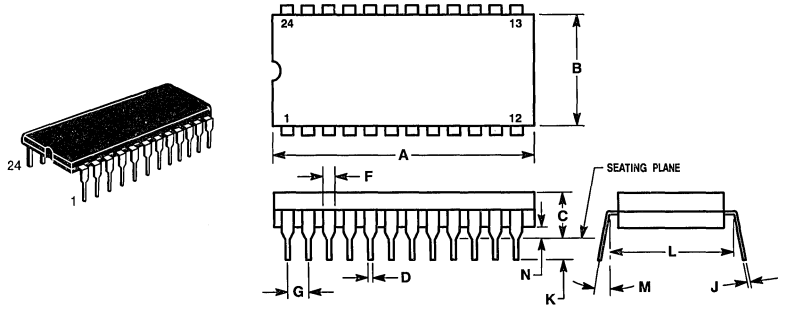
D, J, L, N SUFFIX
CASE 620-10
Ceramic Package
$R_{\theta JA}$ = 100°C/W (Typ)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.93	0.750	0.785
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.39	0.50	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.003	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

L SUFFIX
CASE 623-05
Ceramic Package
$R_{\theta JA}$ = 53°C/W (Typ)

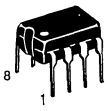


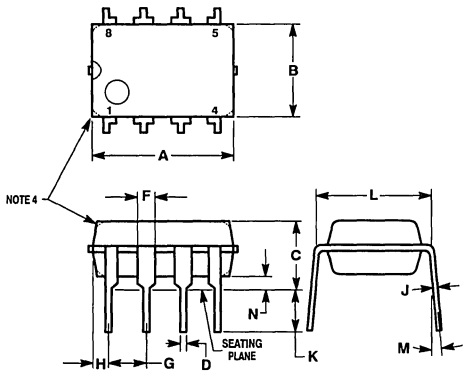
NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

13

DP1, N, P, P1 SUFFIX
CASE 626-05
Plastic Package
$R_{\theta JA}$ = 100°C/W (Typ)

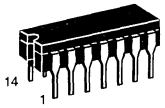


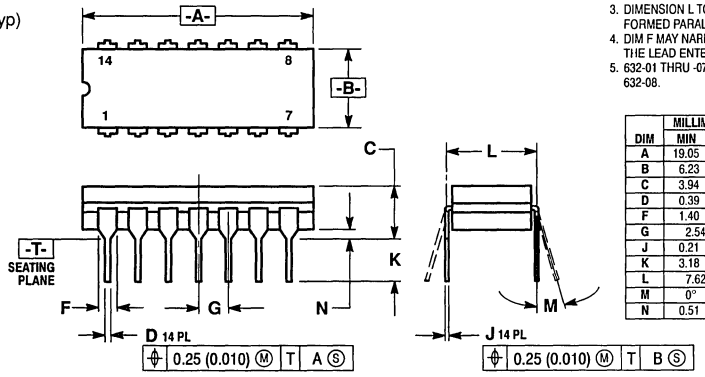


NOTES:
1. LEAD POSITIONAL TOLERANCE:
   ⌖ | ϕ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

J, F, L SUFFIX
CASE 632-08
Ceramic Package
$R_{\theta JA}$ = 100°C/W (Typ)
(TO-116)

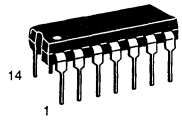


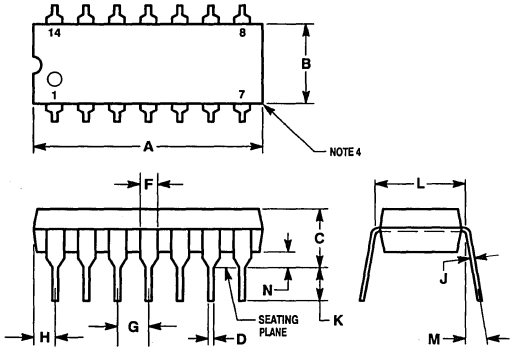


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. 632-01 THRU -07 OBSOLETE, NEW STANDARD 632-08.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

N, P, N-14, P2 SUFFIX
CASE 646-06
Plastic Package
$R_{\theta JA}$ = 100°C/W (Typ)



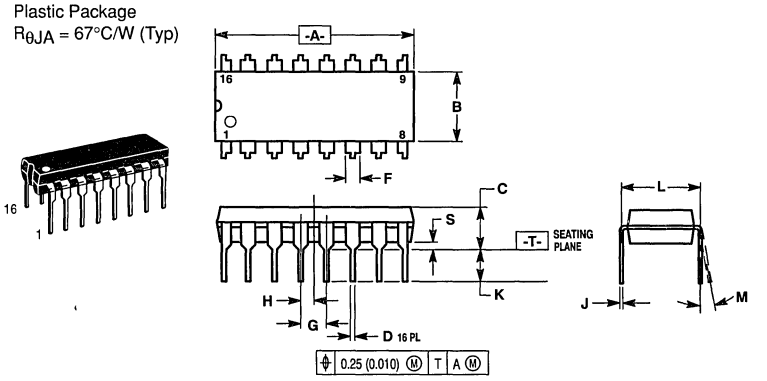


NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

13

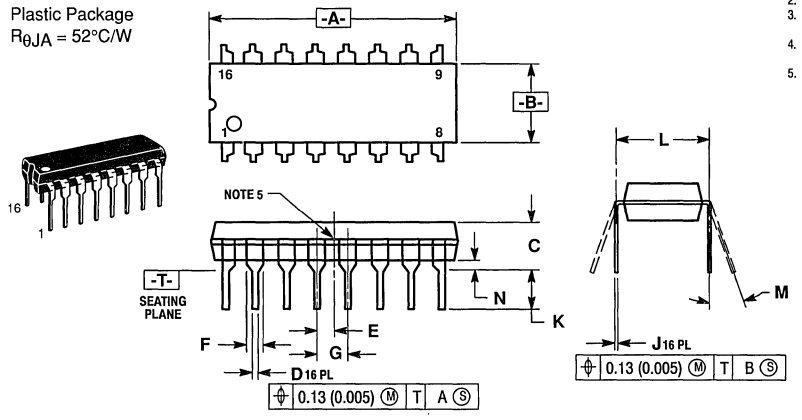
DP2, N, P, PC SUFFIX
CASE 648-08
Plastic Package
$R_{\theta JA}$ = 67°C/W (Typ)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

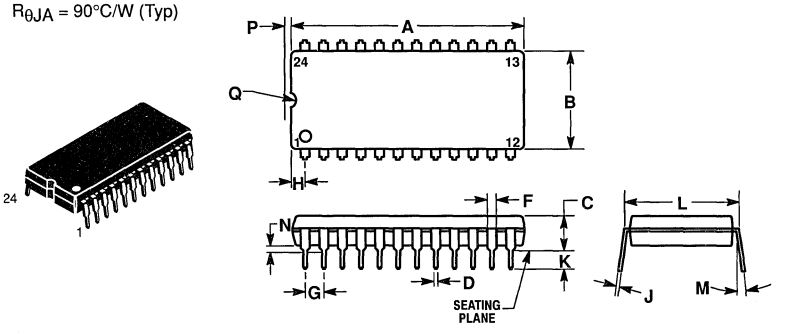
P, V SUFFIX
CASE 648C-03
Plastic Package
$R_{\theta JA}$ = 52°C/W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. INTERNAL LEAD CONNECTION, BETWEEN 4 AND 5, 12 AND 13.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.040

P SUFFIX
CASE 649-03
Plastic Package
$R_{\theta JA}$ = 90°C/W (Typ)

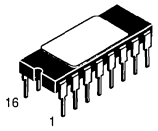


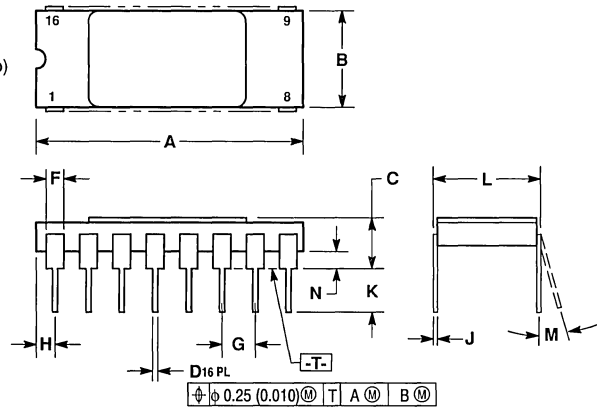
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. 649-02 OBSOLETE, NEW STD 649-03 SEE ISSUE "C" FOR REFERENCE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

13

L SUFFIX
CASE 690-13
Ceramic Package
$R_{\theta JA}$ = 100°C/W (Typ)

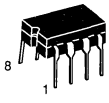


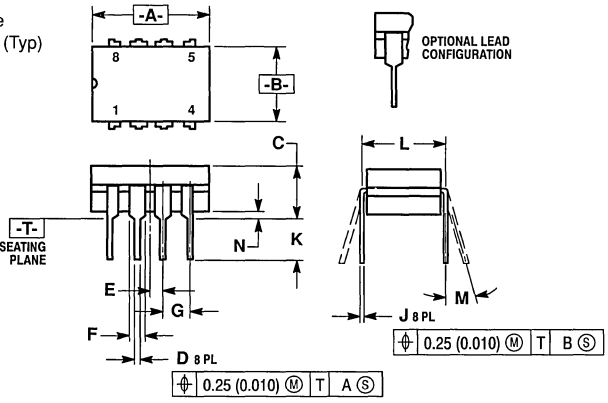


NOTES:
1. -A- AND -B- ARE DATUMS.
2. -T- IS SEATING PLANE.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.
5. 690-11 AND 690-12 OBSOLETE. NEW STANDARD 690-13.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.07	20.57	0.790	0.810
B	7.11	7.74	0.280	0.305
C	2.67	4.19	0.105	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.38	1.52	0.015	0.060

J-8, J, JG, U, Z SUFFIX
CASE 693-03
Ceramic Package
$R_{\theta JA}$ = 100°C/W (Typ)

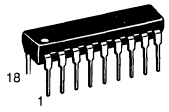


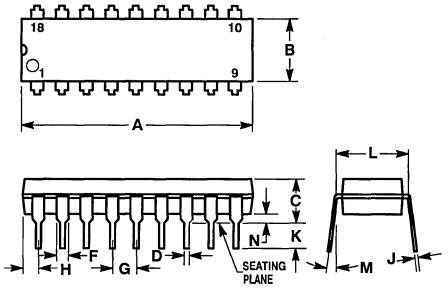


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS AT LEAD POSITIONS 1, 4, 5, AND 8.
5. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
6. 693-01 AND -02 OBSOLETE, NEW STANDARD 693-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.98	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
E	1.27 BSC		0.050 BSC	
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

A, B, N, P SUFFIX
CASE 707-02
Plastic Package
$R_{\theta JA}$ = 100°C/W (Typ)



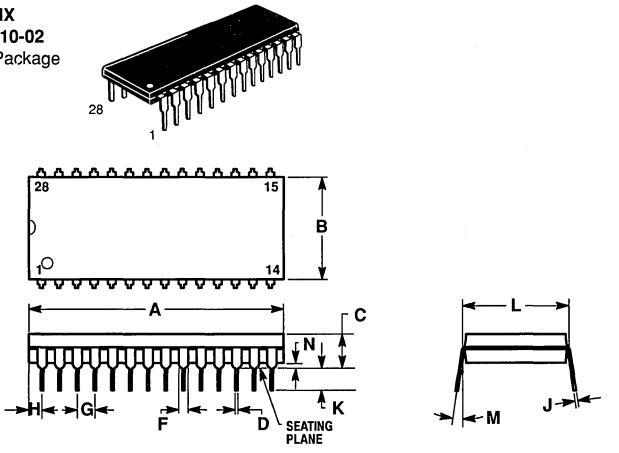


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

13

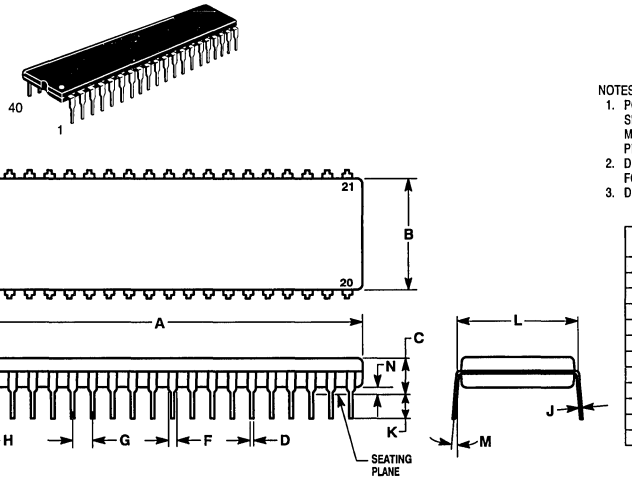
P SUFFIX
CASE 710-02
Plastic Package



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. 710-01 OBSOLETE, NEW STANDARD 710-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

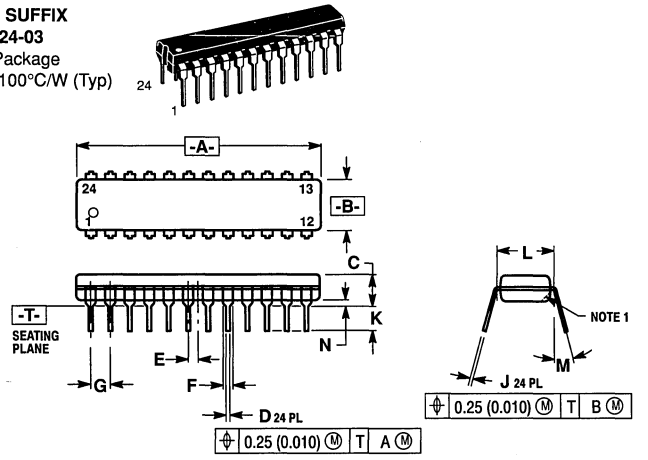
P SUFFIX
CASE 711-03
Plastic Package



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

F, P, P-3 SUFFIX
CASE 724-03
Plastic Package
$R_{\theta JA}$ = 100°C/W (Typ)

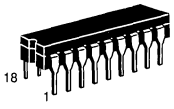


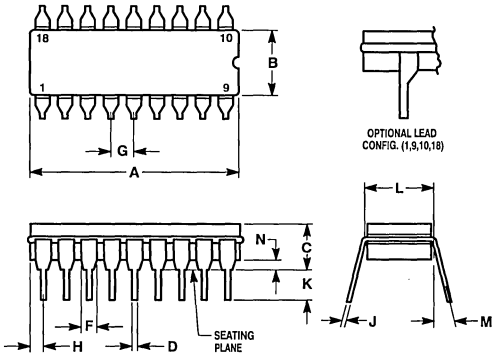
NOTES:
1. CHAMFERRED CONTOUR OPTIONAL.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

13

J, L SUFFIX
CASE 726-04
Ceramic Package
$R_{\theta JA}$ = 100°C/W (Typ)

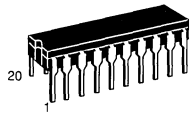


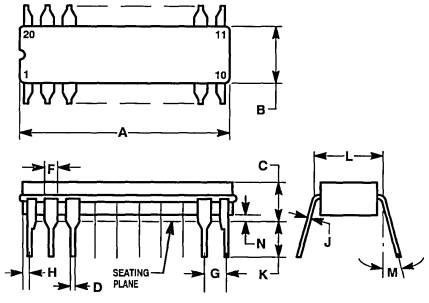


NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0 °	15 °	0 °	15 °
N	0.51	1.02	0.020	0.040

L SUFFIX
CASE 732-03
Ceramic Package
$R_{\theta JA}$ = 75°C/W (Typ)

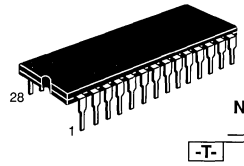


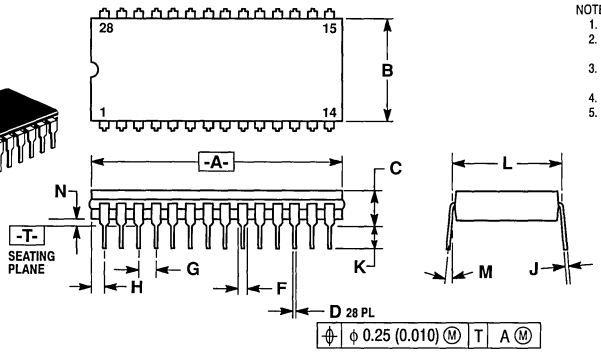


NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

L SUFFIX
CASE 733-04
Ceramic Package



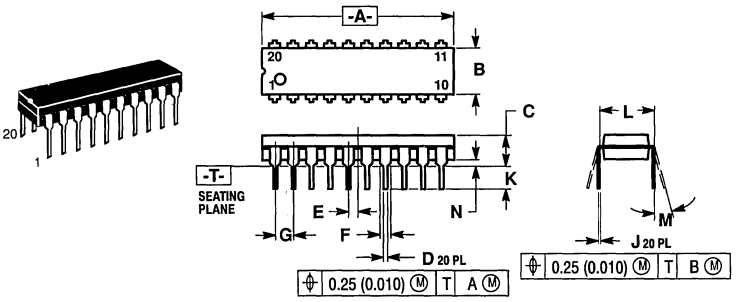


NOTES:
1. DIM A AND B INCLUDES MENISCUS.
2. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
4. CONTROLLING DIM: INCH.
5. 733-03 OBSOLETE, NEW STANDARD 733-04.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.84	1.435	1.490
B	12.70	15.36	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.55	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

13

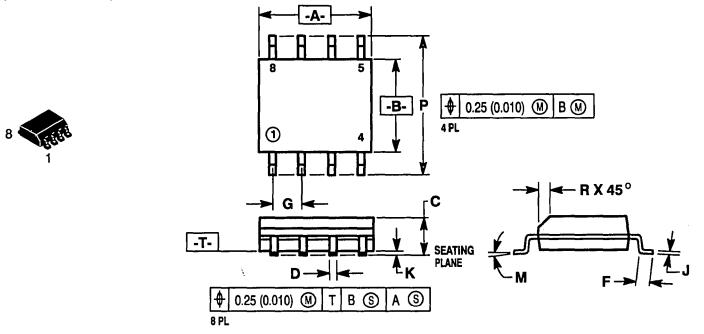
P SUFFIX
CASE 738-03
Plastic Package
$R_{\theta JA}$ = 75°C/W (Typ)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. 738-02 OBSOLETE, NEW STANDARD 738-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

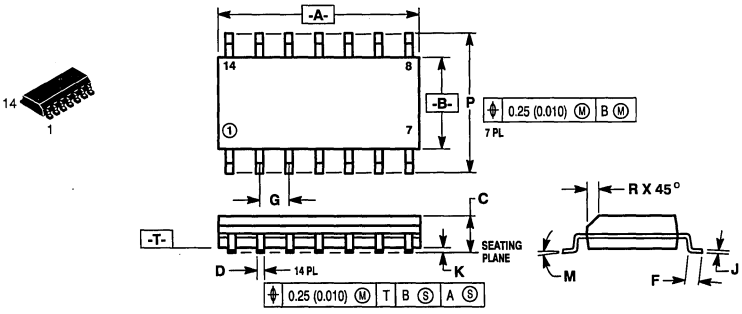
D SUFFIX
CASE 751-03
Plastic Package
(SO-8, SOP-8)



NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIM: MILLIMETER.
4. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

D SUFFIX
CASE 751A-02
Plastic Package
(SO-14)

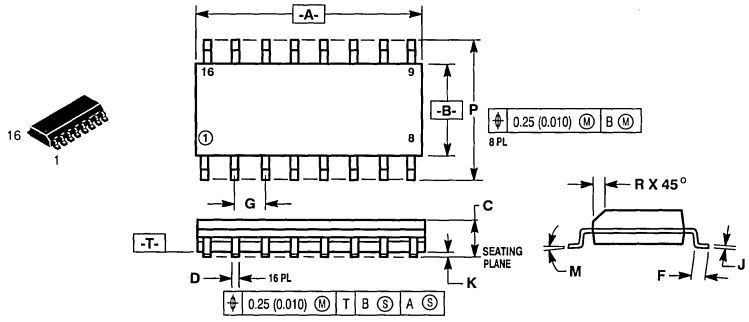


NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

13

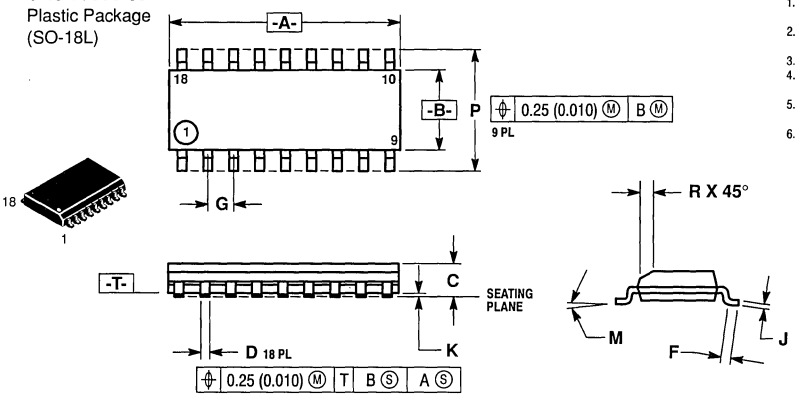
D SUFFIX
CASE 751B-03
Plastic Package
(SO-16)



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

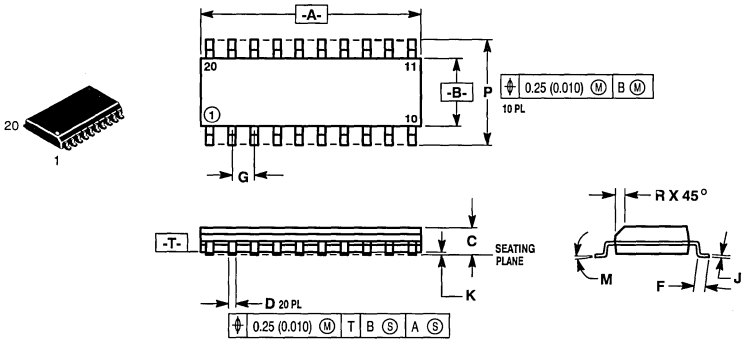
DW SUFFIX
CASE 751C-03
Plastic Package
(SO-18L)



NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIM: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
6. 751C-01, AND 02 OBSOLETE, NEW STANDARD 751C-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.40	11.70	0.449	0.460
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DW SUFFIX
CASE 751D-03
Plastic Package
(SO-20L)

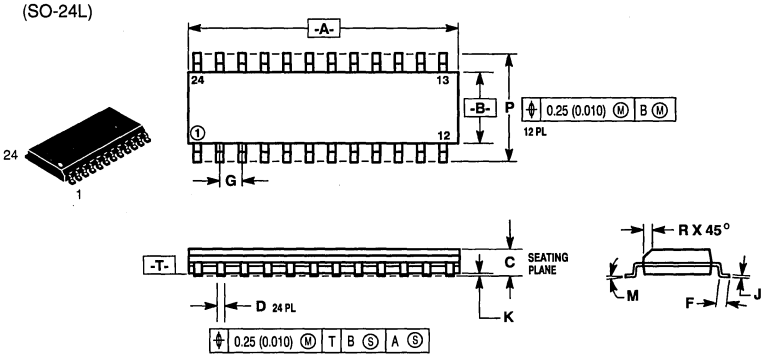


NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

13

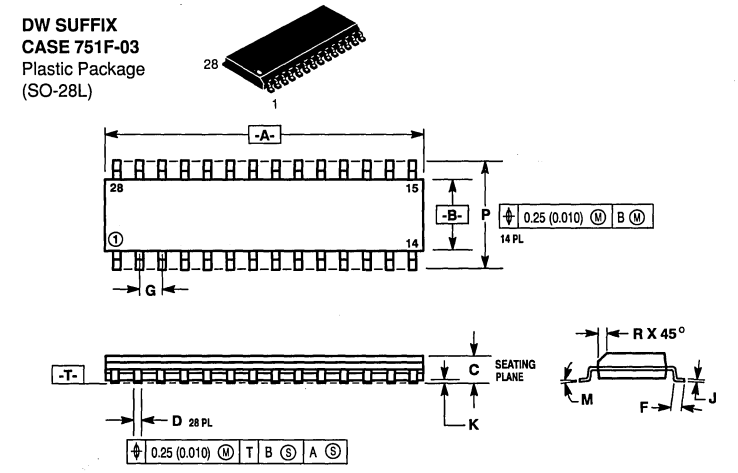
DW SUFFIX
CASE 751E-03
Plastic Package
(SO-24L)



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.229	0.317	0.0090	0.0125
K	0.127	0.292	0.0050	0.0115
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

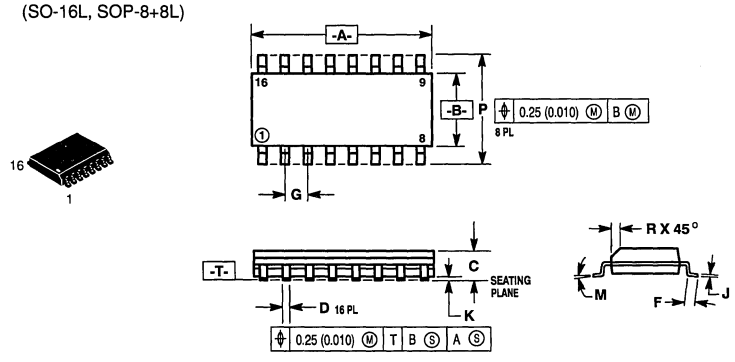
DW SUFFIX
CASE 751F-03
Plastic Package
(SO-28L)



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.229	0.317	0.0090	0.0125
K	0.127	0.292	0.0050	0.0115
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DW SUFFIX
CASE 751G-01
Plastic Package
(SO-16L, SOP-8+8L)

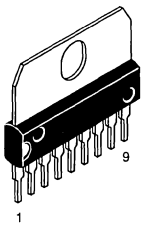


NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

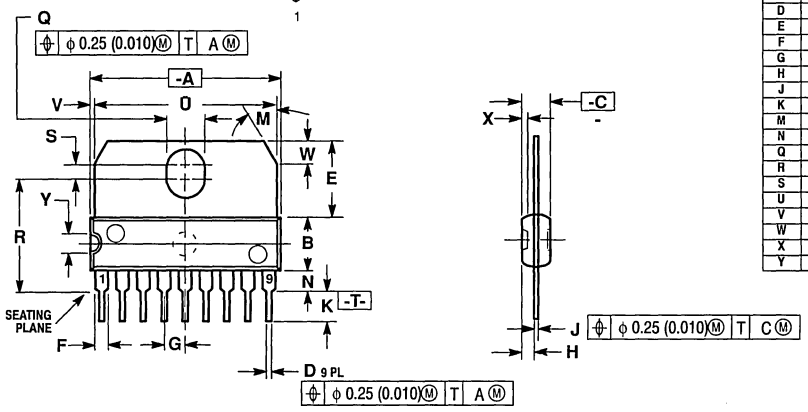
13

CASE 762-01
Plastic Medium Power Package
(SIP-9)
$R_{\theta JA}$ = 70°C/W(Typ)
$R_{\theta JC}$ = 15°C/W(Typ)



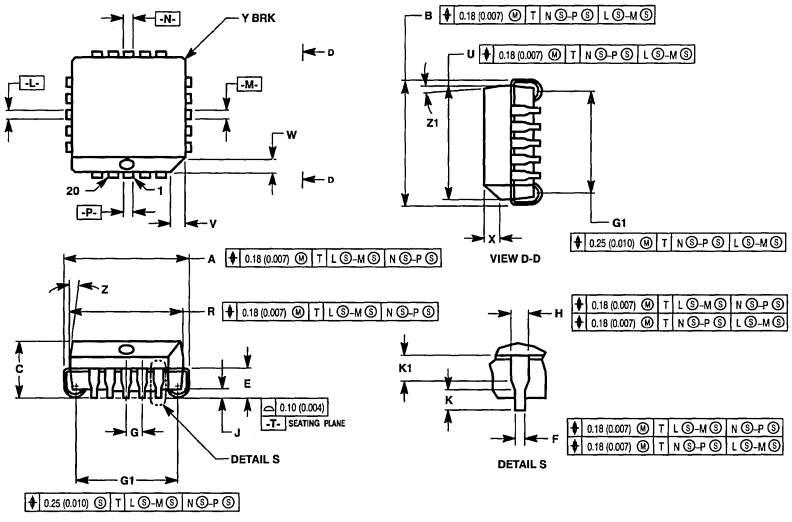
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
2. CONTROLLING DIMENSION: MILLIMETER

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.40	23.00	0.873	0.897
B	6.40	6.60	0.252	0.260
C	3.45	3.65	0.135	0.143
D	0.40	0.55	0.015	0.021
E	9.35	9.60	0.368	0.377
F	1.40	1.60	0.055	0.062
G	2.54 BSC		0.100 BSC	
H	1.51	1.71	0.059	0.067
J	0.360	0.400	0.014	0.015
K	3.95	4.20	0.155	0.165
M	30° BAC		30° BAC	
N	2.50	2.70	0.099	0.106
Q	3.15	3.45	0.124	0.135
R	13.60	13.90	0.535	0.547
S	1.65	1.95	0.064	0.076
U	22.00	22.20	0.866	0.874
V	0.55	0.75	0.021	0.029
W	2.89 BSC		0.113 BSC	
X	0.65	0.75	0.025	0.029
Y	2.70	2.80	0.106	0.110



FN SUFFIX
CASE 775-02
Plastic Package
(PLCC-20)
$R_{\theta JA}$ = 72°C/W(Typ)
(5k SQML)

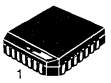
NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
2. DIM GI, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

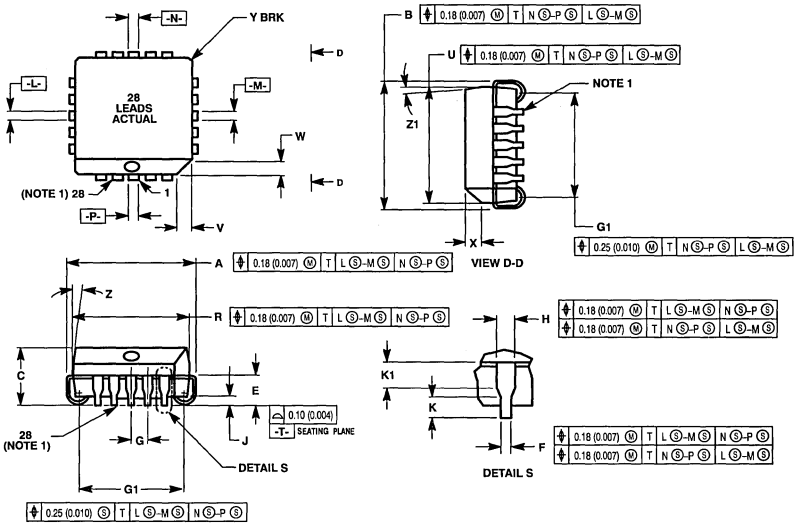


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.78	10.03	0.385	0.395
B	9.78	10.03	0.385	0.395
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	8.89	9.04	0.350	0.356
U	8.89	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	7.88	8.38	0.310	0.330
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

13

FN SUFFIX
CASE 776-02
Plastic Package
(PLCC–28)
$R_{\theta JA}$ = 66°C/W(Typ)
(5k SQML)

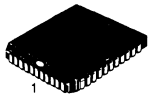


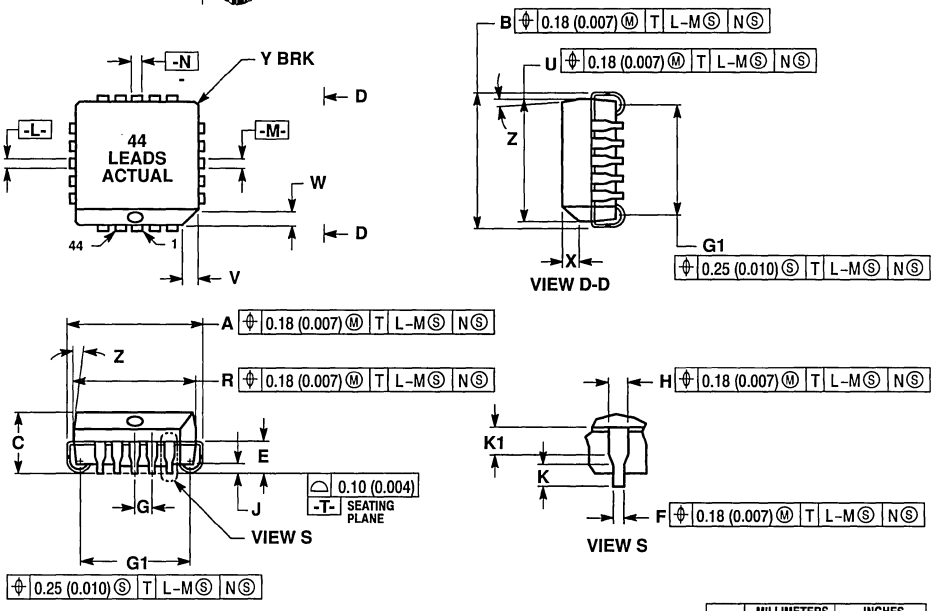


NOTES:
1. **DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	10.42	10.92	0.410	0.430
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

FN SUFFIX
CASE 777-02
Plastic Package

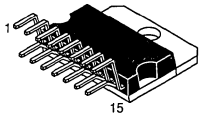


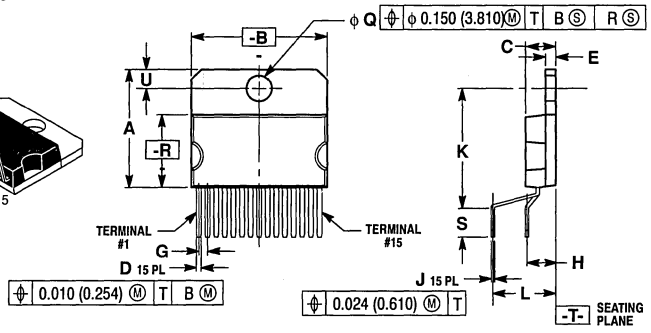


NOTES:
1. **DUE TO SPACE LIMITATION, CASE 777-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 44 LEADS.**
2. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO .012 (.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
8. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN .037 (.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN .025 (.635).
9. 777-01 IS OBSOLETE, NEW STANDARD 777-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.40	17.65	0.685	0.695
B	17.40	17.65	0.685	0.695
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	16.51	16.66	0.650	0.656
U	16.51	16.66	0.650	0.656
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	15.50	16.00	0.610	0.630
K1	1.02	—	0.040	—

T SUFFIX
CASE 821C-02
Plastic Package
(15-Pin ZIP)





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION R DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 (0.250).
6. 821C-01 OBSOLETE, NEW STANDARD 821C-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.374	17.627	0.684	0.694
B	19.914	20.116	0.784	0.792
C	4.395	4.597	0.173	0.181
D	0.610	0.787	0.024	0.031
E	1.473	1.574	0.058	0.062
G	1.270 BSC		0.050 BSC	
H	4.293 BSC		0.169 BSC	
J	0.458	0.609	0.018	0.024
K	17.526	18.034	0.690	0.710
L	9.373 BSC		0.369 BSC	
Q	3.760	3.835	0.148	0.151
R	10.567	10.820	0.416	0.426
S	4.141	4.470	0.163	0.176
U	2.794 BSC		0.110 BSC	

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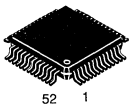
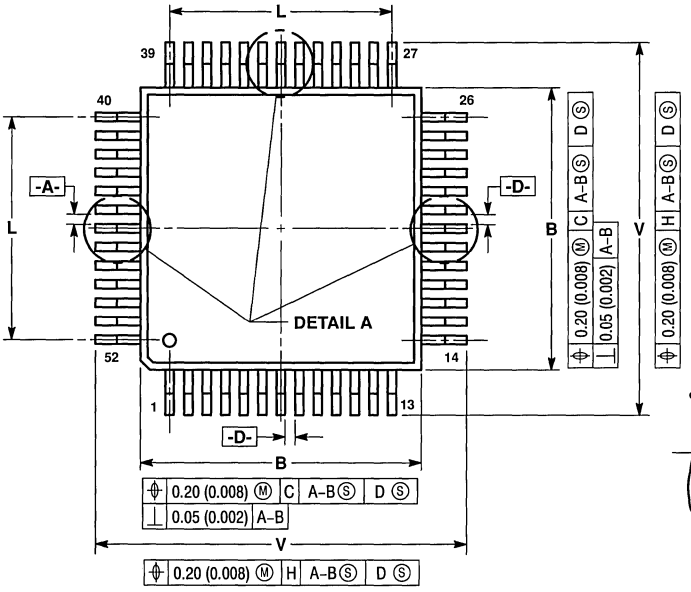
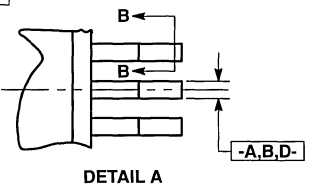
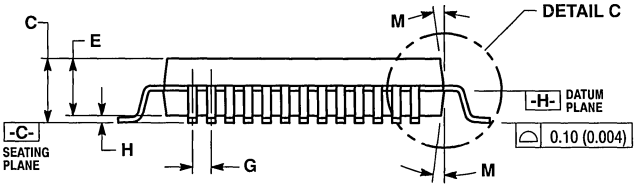
FU SUFFIX
CASE 848B-02
Plastic Package
(52 Pin Thin
Quad Flat Pack)

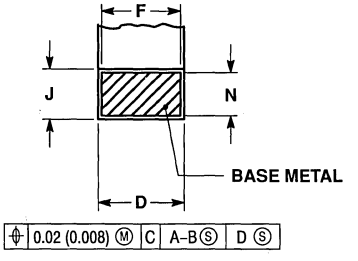




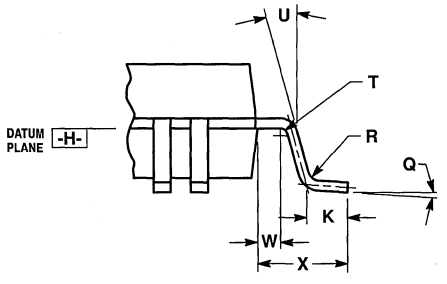


DETAIL A





SECTION B–B



DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.22	0.38	0.009	0.015
E	2.00	2.10	0.079	0.083
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	7.80 REF		0.307 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	—	0.005	—
U	0°	—	0°	—
V	12.95	13.45	0.510	0.530
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.063 REF	

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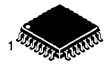
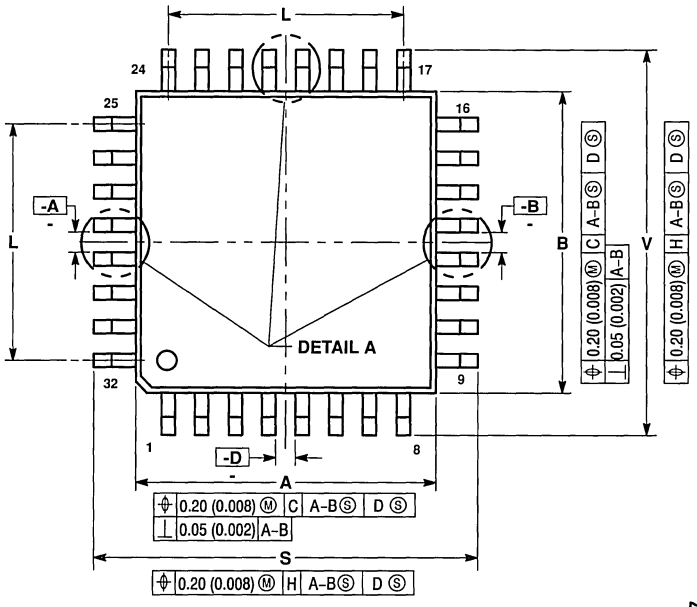
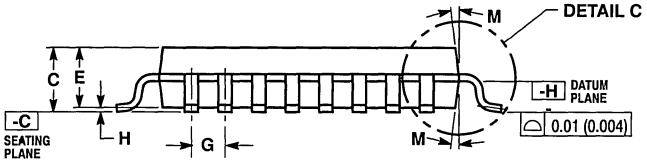
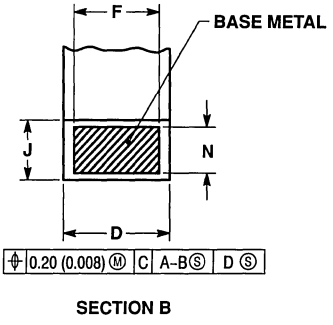
FU SUFFIX
CASE 873-01
Plastic Package
(32 Pin Flat Pack)

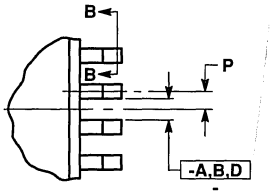




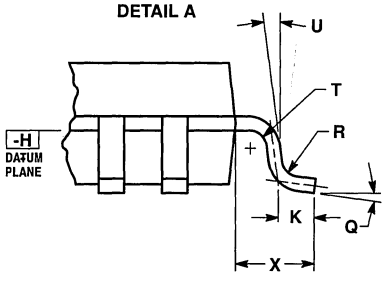




SECTION B



DETAIL A



DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	—	0.010	—
G	0.80 BSC		0.031 BSC	
H	—	0.20	—	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.0 REF		0.039 REF	

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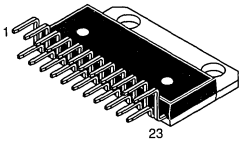
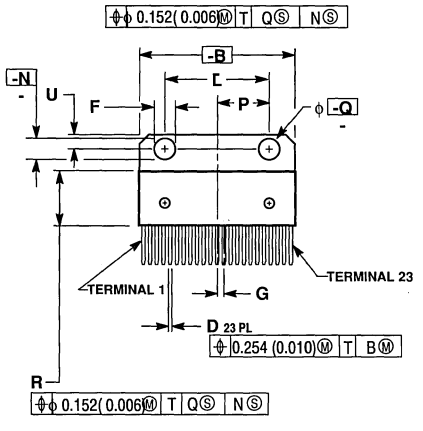
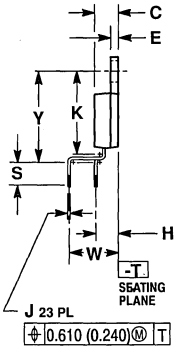
T SUFFIX
CASE 894-01
Plastic Package
(23-Pin ZIP)



NOTES:
1. DIMENSIONING AND TOLERANCEING PER ANSI Y14.5M, 1982.
2. CONTROLING DIMENSION INCH.
3. DIMENSION R DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.250 (0.010).
6. OVERALL LEAD LENGTH DOES NOT INCLUDE LEAD FINISH.

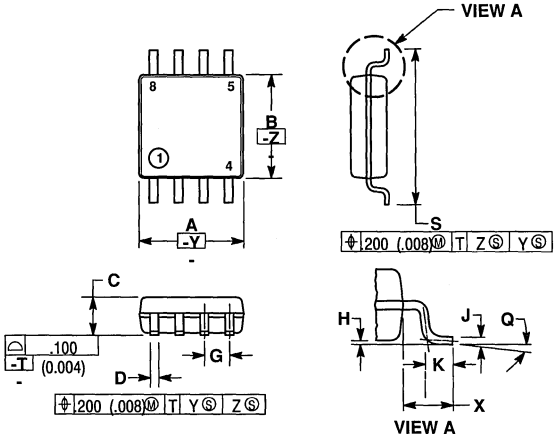




DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	17.374	17.627	0.684	0.694
B	30.048	30.302	1.183	1.193
C	4.445	4.547	0.175	0.179
D	0.660	0.787	0.026	0.031
E	1.473	1.574	0.058	0.062
F	4.191	4.445	0.165	0.175
G	1.270 BSC		0.050 BSC	
H	4.293 BSC		0.169 BSC	
J	0.356	0.508	0.014	0.020
K	15.875	16.231	0.625	0.639
L	19.558	20.066	0.770	0.790
M	4.039 BSC		0.159 BSC	
N	3.760	3.861	0.148	0.152
P	9.906 BSC		0.390 BSC	
Q	3.760	3.861	0.148	0.152
R	10.566	10.770	0.416	0.424
S	4.089	4.394	0.161	0.173
U	2.667	2.921	0.105	0.115
Y	17.577	17.932	0.692	0.706
W	9.373 BSC		0.369 BSC	

F SUFFIX
CASE 904-01
Plastic Package

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED .150 (.006) PER SIDE.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.100	5.450	0.201	0.214
B	5.100	5.400	0.201	0.216
C	—	2.050	—	0.080
D	0.350	0.500	0.014	0.001
G	1.270 BASIC		0.050 BASIC	
H	0.050	0.200	0.002	0.007
J	0.180	0.270	0.008	0.010
K	0.500	0.850	0.020	0.033
Q	0°	10°	0°	10°
S	7.400	8.200	0.292	0.322
X	1.260 REF		0.0496 REF	

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